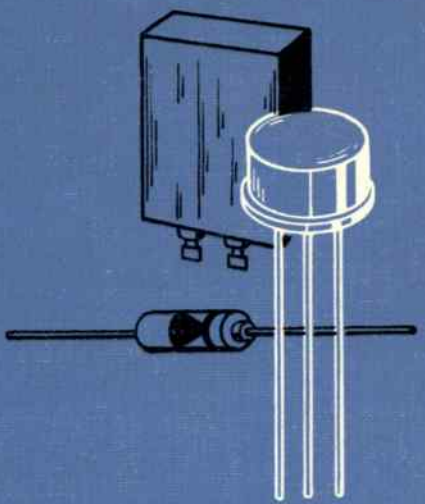
Workshop
In
SOLID STATE



by Harold E. Ennes

Workshop in Solid State

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Preface

The purpose of this book is to provide a rapid, practical, and effective transition from vacuum-tube circuitry to solid-state circuitry. Thus, it is assumed that the student already has received basic electronics training. The material was originally developed for use in training broadcast technicians. Therefore, broadcast circuits and applications have been emphasized. However, the training is just as useful to students of commercial and industrial applications as to broadcast personnel. Many of the specialized applications included in this training are covered only briefly elsewhere.

For the purpose intended, there was no existing course that suited the immediate need. For the most part, two approaches exist: the completely simplified, or "serviceman," approach, and the sophisticated mathematical and equivalent-circuit approach. This volume is aimed at a level between these two extremes. It is slanted for a learning pace that is as rapid as possible consistent with a practical study of circuit analysis and fundamental design.

I am indebted to a number of previous authors in several ways:

The oscillator coverage in Chapter 13 is taken with a few minor changes from Department of the Army Technical Manual TM11-690, *Basic Theory and Application of Transistors*. This treatment is, in my opinion, the best possible presentation for a basic approach to the subject of sine-wave oscillators.

The terms "transresistance" and "transimpedance" have appeared in numerous scattered references, but they have not been developed to the degree of use in this book. I have found the concept of "transfer resistance" (transresistance) as developed in this volume to be highly effective for the audience intended, those who must be reoriented from vacuum-tube to solid-state technology as quickly as possible, but on a level adequate for working with modern equipment.

RCA Corporation and the General Electric Company, Semiconductor Products Department, have contributed certain illustrations and text material as acknowledged in specific portions of the text.

Finally, I extend my warm appreciation to former students of the Harold E. Ennes Broadcasting Workshop for their insistence on clarification of every subject of that program. This book is far the better because of the resulting revisions and expansion of the original material.

I hope this book will serve as a solid stepping stone for the great majority of men and women who are suddenly in the middle of a brand new world of tubeless circuitry.

HAROLD E. ENNES

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CHAPTER 1

Orientation in Solid State

All diodes and transistors can be described by a common term, "solid-state." "Solid-state"—what does it mean? A logical way to begin a study of diodes and transistors is to look briefly into this terminology.

What is so different about these solid-state devices? Does not a solid conductor of copper carry electricity quite easily? Yes! But the solid-state devices we are going to examine can provide rectification (pass current in only one direction) or provide current, voltage, and power amplification.

The term solid-state implies matter. Matter is the world around us, the world within us, the universe. A basic understanding of matter should be gained for two reasons: (1) for the sheer pleasure of looking into the "fantastic" reality of matter, and (2) for the understanding of solid-state devices used in our particular field of study; when the "why" as well as the "how" is known, we can more readily master circuit analysis (and design) of any *future* developments in solid-state technology.

Some readers may feel they are too advanced to make a study of this first chapter necessary. They should read it anyway, because the method of attack in this book consists of a disciplined progression from chapter to chapter, regardless of previous exposure to "solid-state."

1-1. COSMOS AND MICROCOSMOS

The physical universe is matter. The earth, the sun, the stars, the seas, the breeze—all things we see or touch—are matter.

In the universe, matter in each of its three states—solid, liquid, and gaseous—can change into its other states at different temperatures or pressures. But whatever its state—as hard as steel, as fluid as water, or as formless as the invisible air—matter is made up of basic entities called *molecules*. And molecules are, in turn, made up of *atoms*.

In the universe, light travels at the fantastic speed of 186,000 miles per second. But we know that it takes light from the sun about eight minutes to reach the earth and that it takes thousands of years for the light emitted from distant stars to travel to the earth. So we conclude the universe is mostly empty space.

Now let us travel in the other direction. Suppose we crush a single common brick into a powder, small grains of sand and clay. We have not made any changes in the basic matter. The powder can be remolded and baked to form brick again.

If we could see into one grain of sand (without destroying the sand) we would see billions upon billions of molecules. A *single* molecule is the smallest particle of any compound that can exist and still be the same kind of compound (sand in this case).

However, the molecule is not the smallest particle of matter. A molecule can be broken down into still smaller particles called atoms. But we no longer have the same kind of material. In the break-up of a sand molecule, we obtain two entirely different substances, a gas (oxygen) and a solid (silicon).

These substances are *elements*, the "building materials of matter." The smallest particle of each of the different elements (there are over 100 different elements now known) is an atom. A single atom contains a central core, or nucleus, composed of positively charged *protons* and other particles. (For our purposes, only the protons will be considered.) Around

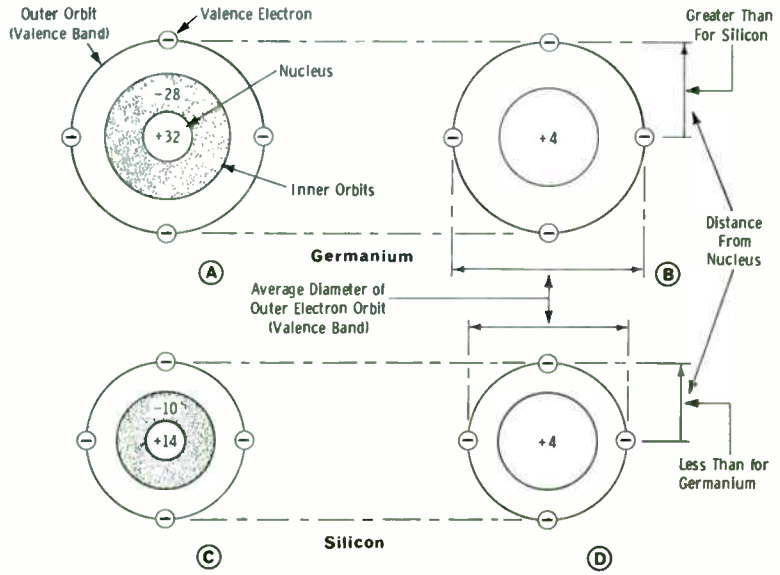


Fig. 1-1. Basic atomic structure of germanium and silicon.

the nucleus whirl electrons (negatively charged). We know that unlike charges attract, but the positive nucleus cannot draw in the negative electrons because the electrons are so far away and travel at such speeds as to prevent it.

Yes, the electrons are "far away" from the nucleus! And they are "far away" from each other! If a typical atom were expanded so that the electrons would become about the size of basketballs, an orbital spacing of some 12 to 15 miles would exist. So we reach another conclusion: Even the atom is mostly empty space.

1-2. THE SINGLE ATOM

In solid-state technology, we are chiefly concerned with crystals of germanium (Ge) and silicon (Si). A single atom of germanium consists of a nucleus charged to + 32 (this means there are 32 protons), surrounded with just enough electrons (32 in this case) to make the atom electrically neutral. Actual electron orbits are quite complex and difficult to visualize, but we can consider the atom in a simplified way that will help in studying the behavior of semiconductors. To do this, we can picture the germanium atom as having 28 of its electrons in several inner orbits, or shells, and the other four electrons in an *outer orbit* (see diagram A in Fig. 1-1).

Since the electrons are a definite mass in motion, they possess energy. Each electron functions at a distinct *energy level* which is fixed at any instant by the momentum of the electron and its physical proximity to the pulling power of the positive nucleus. The farther the electron is from the nucleus, the less control the nucleus has on the electron; thus the outer-orbit electrons have greater ability to break away from the parent atom than the inner-orbit electrons have.

The outer-orbit electrons are termed *valence electrons*, and the orbit of the valence electrons is termed the *valence band*. Both germanium and silicon have four valence electrons. It is these valence electrons we are primarily concerned with in our practical discussion of solid-state physics and applications.

The germanium atom can be represented in further simplified form in terms of "effective nucleus" and valence electrons only (B in Fig. 1-1). Thus the valence electrons of a germanium atom have a definite energy level dictated by the average diameter of the outer electron orbit, or, more specifically, by the distance of the valence band from the nucleus.

A diagram of a single silicon atom is shown at C in Fig. 1-1. The nucleus contains a charge of + 14. Around the nucleus are ten electrons in inner orbits and four electrons in an outer orbit (valence band). In this case, we have + 14 and − 14; the total charge is again neutral.

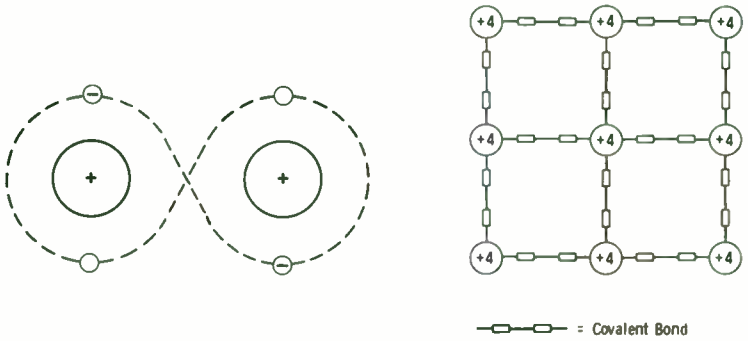
The important difference between the atoms of germanium and silicon can be seen by comparing B and D of Fig. 1-1. Note that the silicon nucleus exerts greater holding power on the valence band than is the case for

germanium. One practical effect of this difference is that silicon is much less affected by increased temperature than is germanium. Also, "leakage current" is much less for silicon than for germanium for any given temperature range. These are characteristics that will become more evident as we progress.

1-3. GROUPS OF ATOMS

In a piece of silicon or germanium, every atom tends to share one of its own valence electrons with each of its neighbor atoms, and also to take one electron from each such neighbor. Fig. 1-2A is a simple representation of this basic atomic action. This orbit sharing, or interchange of orbital energy, which binds the atoms together in a tightly locked action, is said to be the result of a *covalent bond*, or *electron-pair bond*.

Atoms that form solids (except those solids exhibiting a biological structure of cells) most often take up a three-dimensional orderly array that defines a *crystal structure*. Even rocks and metals reveal specific crystal patterns when studied under the microscope. Fig. 1-2B illustrates a highly simplified, two-dimensional, single pure-crystal structure. Each circle represents the effective nucleus of germanium or silicon (B and D of Fig. 1-1).



(*A*) *Orbit sharing.* (*B*) *Simplified crystal.*

Fig. 1-2. Fundamentals of crystal lattice structure.

The four valence electrons are represented in the covalent-bond symbol. In a *pure* germanium or silicon crystal, the covalent bondage (termed "lattice structure") holds the valence electrons tightly in their orbits. Therefore, pure germanium or silicon material is a poor conductor (with resistivity between that of a good conductor and that of an insulator).

The covalent-bond connecting bars can be thought of as tracks along which electrons can shuttle back and forth in opposite directions between adjacent atoms. This type of structure is referred to as a *valence crystal*, or

single crystal structure, and is the type involved in all solid-state devices. This is contrasted to *polycrystalline* materials such as copper, silver, and aluminum, which are very good conductors.

Atoms of substances other than the intended substance (germanium or silicon) do join the crystal-lattice structure. Whether found in the natural state or added intentionally, such substances are termed *impurities*. Both *donor* and *acceptor* impurities can exist.

1-4. DONOR AND ACCEPTOR IMPURITIES

See Table 1-1. Note that an acceptor impurity is from Group III in the periodic table and its atoms have three valence electrons. A donor impurity is from Group V in the periodic table, and its atoms have five valence electrons.

Table 1-1. Basic Materials Used in Solid-State Devices

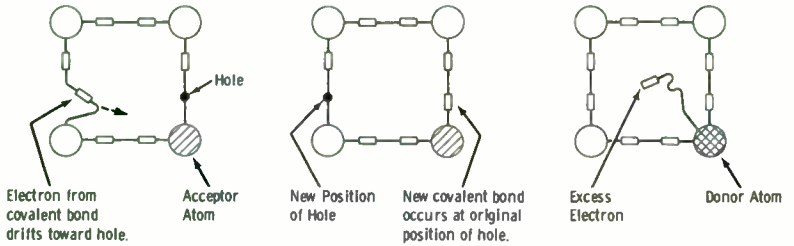
Element	Group in Periodic Table	Number of Valence Electrons	Applications in Solid-State Devices
Boron (B) Aluminum (Al) Gallium (Ga) Indium (In)	III	3	Acceptor elements. Form p-type semiconductors. Can take on (accept) extra electron, thus creating a hole.
Germanium (Ge) Silicon (Si)	IV	4	Basic semiconductor materials. Single-crystal form. Have controlled amounts of acceptor or donor impurities added.
Phosphorous (P) Arsenic (As) Antimony (Sb)	V	5	Donor elements. Form n-type semiconductors. Can give up (donate) extra electron to the crystal structure.

Now study Fig. 1-3A. One of the germanium or silicon atoms has been replaced with an acceptor atom. (This process is termed *doping*.) Since the acceptor has just three valence electrons, one valence electron of one of the neighbor atoms cannot form a covalent bond. The resultant vacancy in the covalent bond behaves as if it were a new free particle with a positive charge. This vacancy is quite logically termed a *hole*.

In Fig. 1-3A, an electron from one of the neighbor atoms begins to break away and drift toward the attraction of the hole. Fig. 1-3B shows the result. The electron has filled the hole, leaving a hole in the original covalent bond. Thus the electron traveled to the right and the hole traveled to the left.

It is normal for the acceptor atom to have only three valence electrons. When it accepts the fourth electron, it becomes an *ion* with a negative charge. (Any atom which loses or gains an electron is called an ion). Also, the germanium or silicon atom, which normally has four valence electrons, is left with just three valence electrons. This atom then has a net positive charge equal in magnitude to the negative charge of one electron.

Carefully note the crystal now contains both an acceptor ion (negative) and a hole (positive). The net charge is still zero. But an *electron-hole* pair has been introduced by which the positive hole moves within the crystal.



(A) Acceptor impurity. *(B) Hole movement.* *(C) Donor impurity.*

Fig. 1-3. Ionization effect of acceptor and donor impurities.

Now let us consider what happens when a donor atom is substituted for one of the germanium or silicon atoms (Fig. 1-3C). Since the donor atom has five electrons in its outer orbit, an extra electron is drifting in the crystal; this electron cannot form a covalent bond with one of the electrons of adjacent atoms. The crystal is trying to "donate" this extra electron. Even at normal room temperatures, there is sufficient thermal energy to cause the electron to leave the parent atom and drift through the space between the crystal lattices. When the fifth electron leaves the donor atom, the donor becomes a positive ion.

Remember again that, although there is a drifting electron (carrying a negative charge) in the crystal-lattice structure, the *total* numbers of electrons and protons in the crystal are the same, and the net charge of the crystal is still zero. But the crystal is now ready to "donate" an excess electron.

To summarize: An acceptor ion is negative; a donor ion is positive. We can now temporarily leave the subject of crystal physics and take it up again with junction formation in Chapter 2.

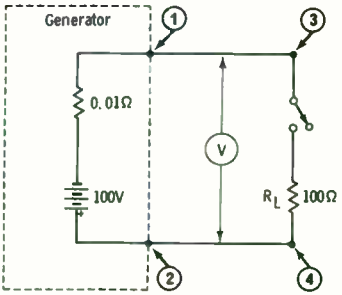
Before going further, it is necessary to get an orientation in "current" itself. This orientation is made necessary because we must understand transistor specification sheets. These will call out, for example, a collector current of "plus milliamperes" or "minus milliamperes." This is partly due

to an unfortunate choice of current direction being "conventional" or being "electronic."

The primary objective here is to obtain a practical visualization of "current" and "electrical charge," to remove the confusion first met by students transferring from electron tubes to solid-state devices.

1-5. POWER SOURCES: WHY "CONSTANT-VOLTAGE" OR "CONSTANT-CURRENT"?

A class-A vacuum-tube amplifier draws no grid current and therefore presents a very high input impedance to the preceding stage. Since this input impedance is normally much greater than the source impedance, it is most convenient to consider the amplifier as a voltage amplifier.



(*A*) *Circuit.*

Condition	Terminals 3-4 Volts	Total Current
Switch Open	100	0
Switch Closed	100 (Very Nearly)	1 Amp (Very Nearly)

(*B*) *Conditions.*

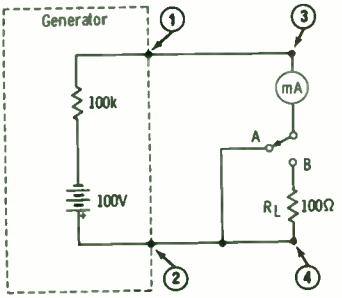
Fig. 1-4. Constant-voltage source.

Now look at Fig. 1-4A. The generator source across terminals 1 and 2 is much lower in impedance than the load (R_L) across terminals 3 and 4. The conditions are tabulated in Fig. 1-4B. With the switch open, 100 volts appears across terminals 3 and 4, and the current is zero. With the switch closed, the voltage across terminals 3 and 4 is still (practically) 100 volts, but the current is almost 1 ampere. So the *voltage* is essentially constant between open-circuit and closed-circuit conditions in Fig. 1-4.

Transistor input circuits (except for field-effect transistors, which we will study later) draw some current, and therefore present a lower input impedance than tube input circuits do. (We still find that circuits can be designed in special applications for relatively high-impedance inputs, but at a sacrifice in other characteristics.) So now let us look at Fig. 1-5A. With the switch in the short-circuit position (position A), the voltage across terminals 3 and 4 is zero, and the current is 1 mA (from Ohm's law). With the switch in position B, the voltage at terminals 3 and 4 is very nearly 100 millivolts, while the current is still (practically) 1 mA. So the *current* is essentially constant between a short-circuit and a load condition.

When the amplifier input impedance is much lower than the source impedance, it is most convenient to consider the amplifier as a *current amplifier* rather than a voltage amplifier.

Please note that in practice the current or voltage is only approximately constant, and depends on the ratio of the internal impedance to the load impedance. Also note that the "reference" in a voltage amplifier is the "open-circuit" voltage, whereas the "reference" in a current amplifier is the "short-circuit" current. We will apply this characteristic later.



(*A*) *Circuit.*

Condition	Terminals 3-4 Volts	Total Current
Switch at "A" (Short Circuit)	0	1 mA
Switch at "B" (Load Connected)	100 mV (Very Nearly)	1 mA (Very Nearly)

(*B*) *Conditions.*

Fig. 1-5. Constant-current source.

1-6. POWER-SOURCE CHARACTERISTICS TO REMEMBER

The basic power source for an amplifier is, of course, the power supply. If it is a chemical (battery) source, we know that chemical action tends to cause an excess of electrons (negative) at one terminal and a deficiency of electrons at the other terminal (making the second terminal positively charged). So we can say that electrons flow from the positive terminal to the negative terminal *within* this source. We can just as accurately say that the chemical process results in one of the terminals having a potential which is positive relative to the other terminal. When we connect an external circuit to this battery, the direction of electron flow through the circuit is from the minus terminal to the plus terminal of the battery. And it makes no difference if we have a rectifier which polarizes and filters ac into a dc voltage; we also have a potential difference between two terminals of this power supply.

A "power source" can also be the output circuit of an amplifier stage. This is the source of signal power for the next stage. With a vacuum tube, we have only one basic way to connect this "power source." The filament or cathode is always the source of electrons, which it emits from its surface because of heat. So call it the "emitter." The emitted electrons are attracted toward the plate of the tube, which is always positive relative to the emitter and therefore collects the bulk of the electrons. So call the

plate the "collector." Now when we connect an external circuit between plate (collector) and cathode (emitter), we know that electron flow is from emitter to collector inside the tube and then back to the emitter through the connected load, where the electrons are made to do useful work. When the grid voltage of a vacuum tube (in class-A service) swings with the applied signal, the plate current changes accordingly, and the plate voltage becomes *more positive* or *less positive*, but is *always* some positive value relative to the cathode.

We will find no such limitation on direction of current in solid-state devices. The collector can be positive or negative relative to the emitter, depending on the type of transistor and on circuit design.

The important thing concerning power sources to keep in mind at this time is that the correct polarity (for the particular application) must always be observed, and the impedance of the source is highly important.

Now we will review some basic Ohm's law, with special considerations that will make following chapters "come alive" in circuit analysis.

1-7. A PRACTICAL CONCEPT OF CURRENT VERSUS ELECTRICAL CHARGE

In Fig. 1-6, a 9-volt battery is connected to a load consisting of three 3-ohm resistors in series. Ammeter A measures the forward current when

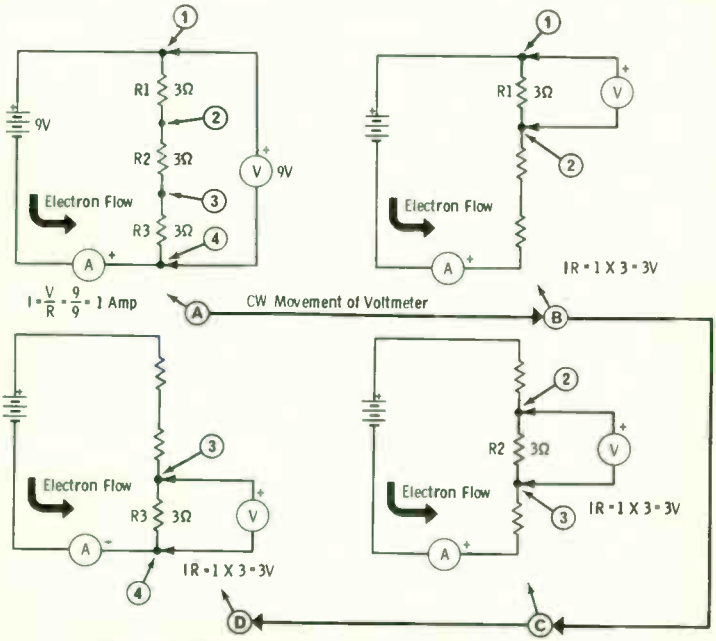


Fig. 1-6. Demonstration of "conventional" current.

connected in series with the circuit with the polarity shown. The voltmeter, connected with the positive lead to terminal 1 and the negative lead to terminal 4, measures the battery voltage of 9 volts. The direction of electron flow is counterclockwise (ccw) around the circuit.

The total current measured by the ammeter is:

$$I = V/R = 9/9 = 1 \text{ ampere}$$

NOTE: When transistors are involved, voltage should be designated by "V" instead of "E." The reason is that the symbol E (or e) is also used to identify the emitter of the transistor.

Now move the negative terminal of the voltmeter to point 2 (diagram B in Fig. 1-6). From Ohm's law, the drop across R1 is 3 volts. Point 1 is positive with respect to point 2 by 3 volts; point 2 is negative with respect to point 1 by 3 volts. In diagram C of Fig. 1-6, we have moved the voltmeter across R2; then in diagram D it is moved across R3. We have simply moved the voltmeter clockwise around the circuit to illustrate the movement of the positive charge.

Similarly, if we started across R3 and moved the voltmeter in the counterclockwise direction, we would illustrate the movement of negative charge, or electron flow. The charge in this case becomes more positive with movement in the ccw direction.

The basic definition of current is the "movement of negatively charged particles of matter called electrons." The direction of electron flow is toward the positive terminal.

From electron theory, a positive charge simply means a *lack of electrons*, or a vacancy, or hole. A hole is not a physical entity, but it moves in a direction opposite to that of electron flow. Remember from basic theory that electrons do *not* "flow" like water through a pipe. Rather, they move toward the positive "attraction" by colliding with adjacent atoms, knocking free electrons away from these atoms to other adjacent atoms, where the process continues. When an electron is released, this action leaves a "hole" (lack of electron) which is immediately filled by a following electron; thus the holes move in a direction opposite to the movement of the electrons. So the electron (negative charge) is moving toward the positive potential, and the positive charge is moving toward the negative potential. We demonstrated this by the simple process of Fig. 1-6. The "positive charge" at point 3 is just 3 volts relative to the negative terminal of the battery (point 4); it is zero at point 4.

To complete the loop of Fig. 1-6, we know that if we connect the positive terminal of the voltmeter to point 4 and the negative terminal to point 1 (you would need a zero-center voltmeter to do this), the voltage reading is again 9 volts, but in the opposite direction. Thus when we "close the loop" on the clockwise movement of the voltmeter to trace the movement of the positive charge, we go toward minus by 9 volts and then go toward plus by 9 volts.

So we have a battery voltage which is the sum of the IR drops across the three resistors, or in terms of the positive charge:

$$+9 - IR1 - IR2 - IR3 = 0$$
$$+9 - 3 - 3 - 3 = 9 - 9 = 0$$

In other words, the algebraic sum of the voltages around any closed loop is zero (Kirchhoff's law).

In terms of the negative charge:

$$-9 + IR1 + IR2 + IR3 = 0$$
$$-9 + 3 + 3 + 3 = -9 + 9 = 0$$

In summary: A positive charge moves toward the negative potential (+ to −). A negative charge moves toward the positive potential (− to +). The *algebraic* sum of voltages around the entire closed loop is zero. We can look at "current" either way; the *work accomplished* is identical.

Then why all this review? It is included because transistors and all solid-state devices operate on basic crystal-structure theory. We find "blocks" of material in which there is a small (minority) electron flow and a large (majority) movement of "holes," which constitutes the main current. These work in conjunction with "blocks" of material which have their main (majority) conduction by electrons, with only small (minority) hole movement. It is not necessary to be able to visualize the most complex crystal-structure action in semiconductors. It is necessary that we be able to visualize the more practical action as will be evident in the progress of these chapters. This visualization is the backbone of practical circuit analysis.

EXERCISES

Try to respond to each question on your own without looking at the answer. If you can't answer a question, review the chapter carefully, and then try again. Exercises at the end of each chapter may, in a few cases, cover an addition to the chapter material, but an addition that is inclusive within the framework of the subject covered. This checks your ability to apply knowledge. For example, later in this group of exercises, you are given questions on basic network analysis of the kind particularly applicable to the coverage in the remainder of the book.

HELPFUL REVIEW: Thevenin's theorem states that any linear network of impedances and generators, if viewed from any two points in the network, can be replaced by an equivalent voltage source (V_{EQ}) and an equivalent impedance (Z_{EQ}) in series. Voltage V_{EQ} is the open-circuit voltage between the two points, and Z_{EQ} is the impedance seen when looking into the network from the two points.

Q1-1. The electric charge on a proton is:
(A) Minus one.
(B) Plus one.
(C) Neutral.

Q1-2. The electric charge on an electron is:
(A) Minus one.
(B) Plus one.
(C) Neutral.

Q1-3. Valence electrons in an atom are those:
(A) In the orbit closest to the nucleus.
(B) In the orbit farthest from the nucleus.

Q1-4. The number of valence electrons in a germanium atom is:
(A) Three.
(B) Four.
(C) Five.

Q1-5. The number of valence electrons in a silicon atom is:
(A) Three.
(B) Four.
(C) Five.

Q1-6. The resistivity of pure germanium or silicon is:
(A) Very high.
(B) Medium.
(C) Very low.

Q1-7. Is the resistivity of pure silicon higher or lower than the resistivity of pure germanium? Why?

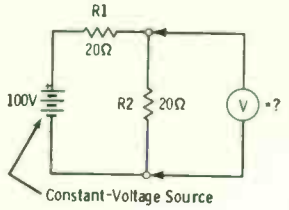
Q1-8. When an impurity is introduced into germanium or silicon, the resistivity is:
(A) Lowered.
(B) Raised.

Q1-9. Relative to the valence band of germanium or silicon, a donor impurity has:
(A) One less valence electron.
(B) One more valence electron.

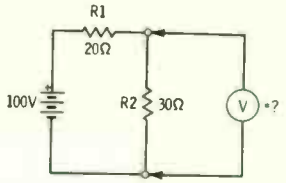
Q1-10. A donor ion is:
(A) Negative.
(B) Positive.
(C) Neutral.

Q1-11. Relative to the valence band of germanium or silicon, an acceptor impurity has:
(A) One less valence electron.
(B) One more valence electron.

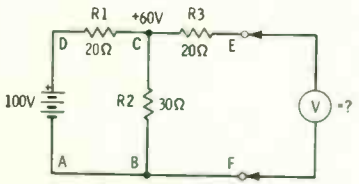
Q1-12. An acceptor ion is:
(A) Negative.
(B) Positive.
(C) Neutral.



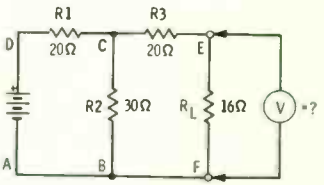
(A) Q1-13.



(B) Q1-14.



(C) Q1-15.



(D) Q1-16.

Fig. 1-7. Circuits for practice exercises.

NOTE: The questions in the next group review basic electronic-circuit analysis desirable to emphasize in this book.

Q1-13. See Fig. 1-7A. What is the voltage across R2?

Q1-14. See Fig. 1-7B. What is the voltage across R2?

NOTE: All following circuits in this circuit-analysis group simply add to the circuit of Fig. 1-7B.

Q1-15. See Fig. 1-7C. What is the voltage between terminals E and F?

Q1-16. See Fig. 1-7D. A load resistor (R_L) has been connected between terminals E and F. What is the voltage between terminals E and F now?

Q1-17. What is the voltage (to be designated as V_L) across R_L in Fig. 1-8 when the switch is in the closed (A) position?

Q1-18. Solve Fig. 1-9 for the current in R_L. (Call this I_L).

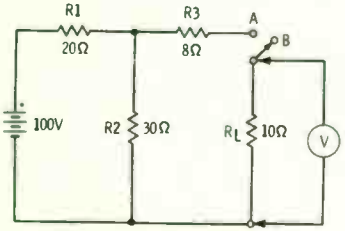


Fig. 1-8. Circuit for Q1-17.

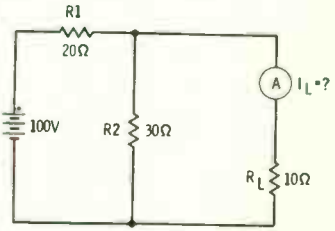


Fig. 1-9. Circuit for Q1-18.

Q1-19. Solve Fig. 1-10 for I_L.

NOTE: The remaining group of questions involves use of Tables A-1 and A-2 in the Appendix.

Q1-20. An oscilloscope amplifier is specified as having a rise time of 35 nanoseconds (35 ns). What is the rise time in microseconds (μs)?

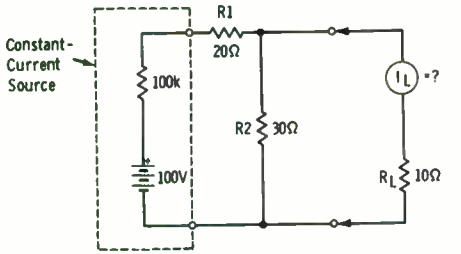


Fig. 1-10. Circuit for Q1-19.

Q1-21. An amplifier is specified as having a bandwidth (between the 3-dB points) of 0.01 gigahertz (0.01 GHz). What is this in megahertz (MHz)?

Q1-22. A capacitor is designated as 470 pF. What is its value in $\mu\mu$F? In μF?

Q1-23. What is the dB equivalent of a power ratio of 0.5?

Q1-24. What is the dB equivalent of a voltage ratio of 0.5?

Q1-25. Find the power ratio for a loss of 57 dB.

CHAPTER 2

Do You Really Know the Diode?

Suppose a basic block of semiconductor material (normally germanium or silicon) has been doped with about 1 part in 10 million of donor impurity so that it has a number of free electrons. This simply means that when a battery is connected across the block (Fig. 2-1A) the donor-impurity electrons in the conduction band migrate, or diffuse, toward the positive-potential junction of the battery. Conduction is similar to conduction in a resistance, except for one very important difference. See Fig. 2-1B. With an increase in temperature, more covalent bonds in the crystal lattice structure break down for a given voltage, elevating more electrons to the conduction band, resulting in greater current. The effect of temperature is much greater on germanium than on silicon.

2-1. SEMICONDUCTOR PHYSICS IN BRIEF

The effect of temperature is the first basic rule of semiconductor physics. Since the semiconductor resistance decreases with an increase in temperature, it has a *negative* temperature coefficient. An increase in temperature of a copper conductor increases the thermal agitation of the atomic structure so as to impede electron flow (increase resistance); hence the resistance of copper has a *positive* temperature coefficient.

A block of semiconductor material might have a resistance of 10 ohms at 0°C. In this case the conductance (inverse of resistance) is:

$$G = \frac{1}{10} = 0.1 \text{ mho} = 100{,}000 \text{ micromhos}$$

(The mho is the unit of conductance—ohm spelled backward.) The same material at 100°C might have a resistance of 2 ohms; the conductance at this temperature is 0.5 mho, or 500,000 micromhos.

An isolated block of n-type material as represented by Fig. 2-1A is electrically neutral. This means that for every free electron in the conduction band a positively ionized donor atom exists in the crystal lattice structure (Fig. 2-1C). Although an n-type block has a number of free electrons, each negative charge is balanced by a fixed positive charge, and the net charge of the crystal is zero (as described in Chapter 1).

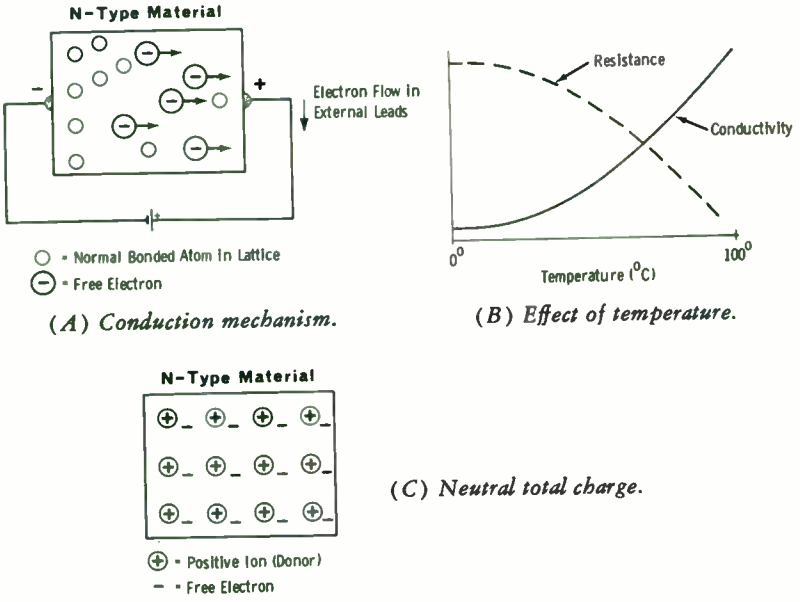
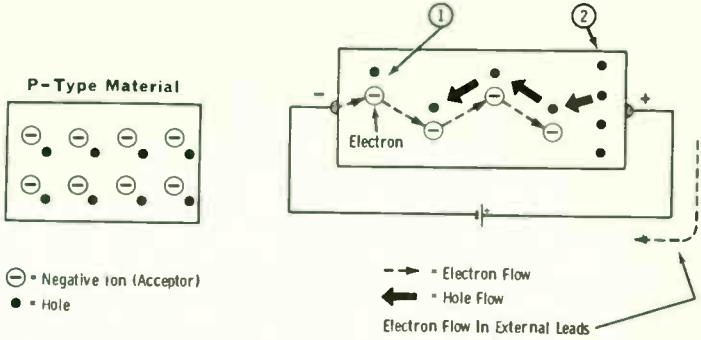


Fig. 2-1. Basic characteristics of n-type material.

Let us carry this idea over into the representation of a p-type material (Fig. 2-2A). In this case, the atom of the doped impurity has one less electron than it needs to establish covalent bonds with neighboring atoms. One covalent bond may have only one electron instead of two, leaving a vacancy, or hole, in that covalent bond. In the process of doping the p-type material, negatively charged acceptor ions are chemically induced, but, as in the n-type material, the net electrical charge is zero. Also as with the n-type material, the p-type material has a negative temperature coefficient of resistance.

Now let us connect a battery to the block of p-type material, as in Fig. 2-2B. The battery circuit is closed through the p-type material, and electrons enter the negative terminal of the block (point 1). The hole at point 1 is filled by an electron. So we see that holes at the negative terminal are being cancelled. We also know that at the positive terminal (point 2) electrons are being drawn away, creating new holes. So as the electrons



(*A*) *Make-up of crystal.* (*B*) *Conduction mechanism.*

Fig. 2-2. Basic characteristics of p-type material.

in adjacent bonds of the crystal structure shift to positions where holes originally existed (from negative to positive), a steady stream of holes (hole current, or positive current) moves from the positive terminal to the negative terminal. This is the *intrinsic current* in the structure. It results in a large *electron flow* in the external battery leads, just as happened for the n-type material.

If this seems confusing at the moment, have patience. It is necessary to gain an insight into the basic physics of semiconductors in order to understand how a transistor amplifies signals. This insight will be of tremendous value to those who progress to more sophisticated studies of solid-state devices. In this book, we are going to cover only what is necessary to understand practical circuits.

For the moment, visualize the following action: The n-type material has a number of excess (free) electrons as depicted by the single free electron of Fig. 1-3C. By the action described in connection with Fig. 1-3C, there will be many more excess electrons than holes in the n-type material. This is true even though the net charge is electrically neutral. The excess electrons, unlike the tightly locked valence electrons, are in the *conduction band* and are able to contribute to current through the crystal.

The p-type material, by the action described in Chapter 1 for Figs. 1-3A and 1-3B, has many more holes than free electrons. Again, this is true even though the net electrical charge is zero.

Therefore, current in n-type material is chiefly by electron carriers. Current in p-type material is chiefly by hole carriers. Another way to say this is:

1. In an n-type material, the *majority carriers* are electrons, and the *minority carriers* are holes.
2. In a p-type material, holes are the *majority carriers*, and electrons are the *minority carriers*.

For the n-type material, the excess electrons are those available for conduction at normal operating temperatures. Valence electrons remain tightly locked in the lattice structure. For the p-type material, valence electrons contribute to the current *only* during the very short lifetime of the electron-hole recombination depicted by Figs. 1-3A and 1-3B. The holes contribute the largest share of current conduction. Holes never leave the crystalline structure; they are simply the carriers which provide conduction through the material so that electrons flow in the external circuit.

2-2. THE PN JUNCTION: A SOLID-STATE DIODE

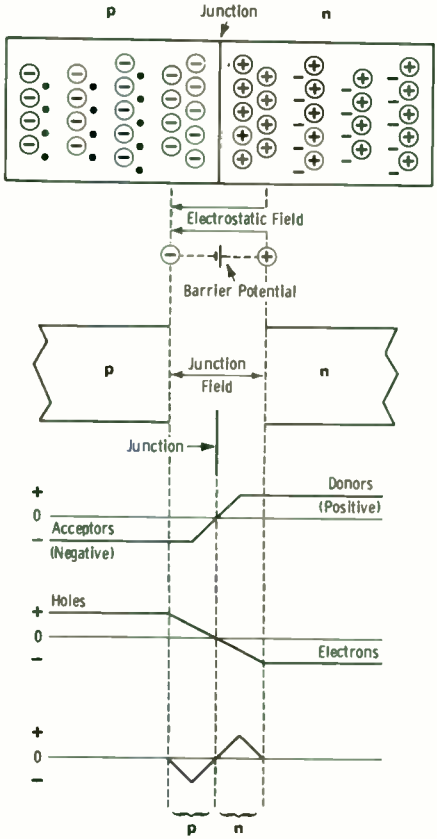
A semiconductor diode is made by taking a single crystal (germanium or silicon) and adding a donor impurity to one region and an acceptor impurity to the other. We then have a single crystal with an n section and a p section. Regardless of the method of manufacture, the junction (where the two sections meet) must itself have the properties of a single crystal.

Now let us look at the pn junction by observing Fig. 2-3A, remembering this is the diode only, without any external voltage applied. When the free electrons in the conduction band of the n material "see" the relatively empty conduction band (holes) of the p-material, they diffuse (drift, move, or spread out) into the p section. These electrons lose their energy and recombine with the holes. (Bear with us a while; you will soon see why the process does not continue beyond this.) Each recombination eliminates a free electron *and* a hole.

When each electron moves from the n section across the junction, it leaves a positive donor ion which is no longer balanced by a negative charge. Also, this same electron, upon recombination with a hole in the p section, causes a negative acceptor ion which is no longer balanced by a positive charge.

Now we begin to see that an electrostatic field exists across the junction between the oppositely charged ions. Negatively charged ions are built up on the p side, and positive ions are built up on the n side. Due to this opposite polarity, a "barrier" is built up which can be represented by a battery connected as shown in Fig. 2-3A. We can also see that this potential difference must be overcome when we forward bias the diode. If we apply only a few millivolts of forward bias, we still do not get current.

But why did the above described recombination stop when it did, before total recombination (neutralization) took place? The diffusion of electrons across the junction continued only until the magnitude of the electrostatic field increased to the point where the electrons no longer had sufficient energy to overcome it. (In the electrostatic field, holes are accelerated *with* the arrows, electrons *against* the arrows.) This action occurred instantly when the junction was formed. Only the carriers in the immediate vicinity of the junction were involved; carriers in the remainder



(A) *Formation of barrier region.*

(B) *Extent of junction field.*

(C) *Charge of impurity ions.*

(D) *Charge of carriers.*

(E) *Net charge near junction.*

Fig. 2-3. Diagrams of pn junction.

of the p and n sections were left largely undisturbed and maintain balanced charges.

Notice that the junction field contains no mobile carriers, only acceptor and donor ions. (Any mobile carriers which would chance to appear within the electrostatic field are accelerated out to the field boundaries.) So we can say that the junction field has a *depletion* of mobile carriers, and it is sometimes termed the *depletion layer*, or *depletion region*. It may also be termed the *space-charge region*, or *junction barrier*.

A question sometimes raised at this point is "You show the junction barrier resulting from an internal charge difference between the p and n sections. If so, why can't I measure a voltage between the two sides of the material with an ultrasensitive voltmeter?" This is a good question, and here is the answer.

The junction field extends beyond the junction as shown by Fig. 2-3B. Note in Fig. 2-3C that the ionized acceptors of the p region have a

negative charge, while the ionized donors of the n region have a positive charge. At the "dead center" junction, the charge is zero.

Fig. 2-3D shows that holes in the p region have a positive charge, and free electrons in the n region have a negative charge. The barrier has driven the holes in the p region and the electrons in the n region away from the junction, so the charges in the p and n regions have moved farther apart. This is the reason for the more gradual slope of the graph in Fig. 2-3D relative to the graph in Fig. 2-3C. The charge at the actual junction is zero, but the rise on either side is more gradual in Fig. 2-3D than in Fig. 2-3C.

In the p region, the net charge on the crystal is equal to the difference between the charge on the acceptor ions and the charges of the holes. In the n region, the net charge is equal to the difference between the charges on the donor ions and the electrons. So the p and n areas beyond the junction field have a net charge of zero. The resultant within the electrostatic field of the junction barrier is zero at the two extremes of the field and at the actual "dead center" junction. So a voltmeter *cannot* read a potential difference between the ends of the diode. The curve of Fig. 2-3E shows the resultant negative charge in the p region and positive charge in the n region, which form the barrier. An external potential would have to be applied with plus to p and minus to n to cause sufficient reduction of barrier width to allow conduction to occur. The required voltage is in the order of at least a few tenths of a volt. Once there is current, *then* a voltmeter can measure the *voltage drop* across the diode in a closed circuit.

2-3. THE PN JUNCTION WITH EXTERNAL VOLTAGE

When a voltage is applied across a pn junction, it "biases" the junction. If the voltage is connected so that it *opposes* the barrier potential, it will *reduce* the intensity and width of the junction field and thereby aid the passage of current through the junction. This is *forward bias*. If the voltage is connected so that it *aids* the barrier potential, it will *increase* the intensity and width of the junction field and thereby oppose the passage of current through the junction. This is *reverse bias*.

Fig. 2-4A shows the familiar diode symbol. Fig. 2-4B illustrates the unbiased pn junction as discussed in connection with Fig. 2-3. Now we apply an external battery with the positive terminal to the p material and the negative terminal to the n material (Fig. 2-4C). The positive voltage repels holes toward the junction. These holes neutralize most of the negatively charged acceptor ions at that edge of the junction field. The negative terminal of the battery repels electrons toward the junction. These electrons neutralize most of the positively charged donor ions at that edge of the junction field. As a result, the barrier field decreases in width and intensity.

Now how does current actually pass through this "forward-biased" junction? Understanding of this process will be of considerable help in

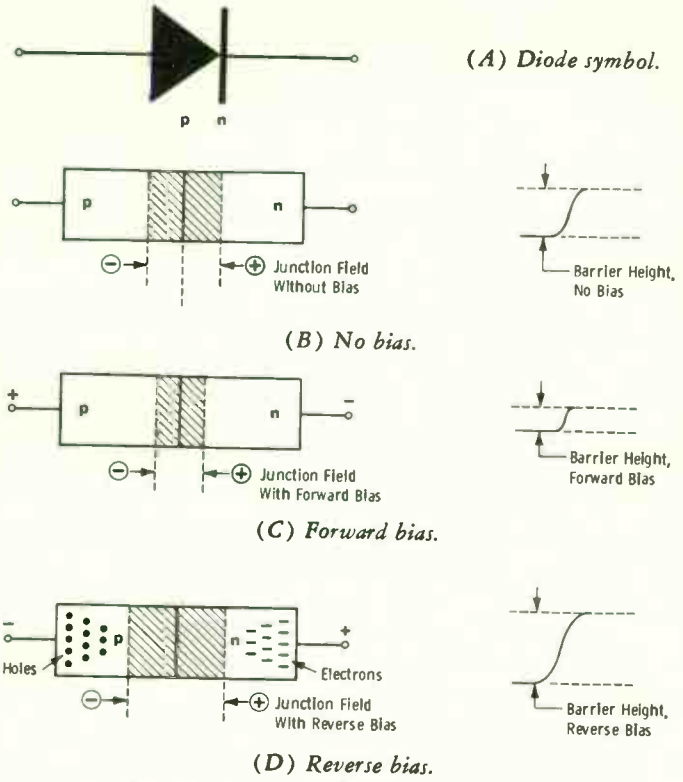


Fig. 2-4. Pn junction with external voltage.

your study of solid-state circuitry. Electrons from the negative terminal of the battery enter the n-type material and move to the edge of the junction field where the slight positive charge exists. Since the other side of the junction field is slightly negative, the electrons lose some of their energy in overcoming this field. But because of the forward bias (external positive potential on the p-type material), the electrons do enter the p-type region, where they are strongly attracted to the positive terminal of the battery, completing the circuit.

Before going further, it is important to realize that p-type material does have some free electrons, and that n-type material does have some holes. But since these are so few in number, they are termed minority carriers. Remember it with the help of Table 2-1. With a forward-biased junction, conduction is by majority carriers.

If the external applied voltage is increased to the point where the barrier potential is completely neutralized, the current will be excessively heavy. Under this condition, the junction can be damaged by the resulting

Table 2-1. Current Carriers

Type of Material	Majority Carriers	Minority Carriers
p	Holes	Electrons
n	Electrons	Holes

heat, so all diodes have a maximum forward current rating. Miniature types are rated in milliamperes. Power diodes are available with ratings of 100 amperes or more.

When we connect the positive terminal of the battery to the n-type material and the negative terminal to the p-type material, as in Fig. 2-4D, we apply a *reverse bias* to the junction. Holes at the edge of the junction field on the p side are attracted away to the negative potential of the battery. The positive terminal of the battery attracts electrons away from the edge of the field on the n side. So the effective width of the junction field is greatly increased. This increase in barrier potential prevents conduction by majority carriers.

But is current through the junction now zero? No! The junction field is in opposition to *majority* carriers only. It is now *forward biased* to *minority* carriers. This current is very low at normal operating voltages and temperatures. But since there *is* a small current, the "reverse resistance" is *not* infinite, but very high. Bear in mind that this resistance (either forward or reverse) decreases with increasing temperature.

In our studies of solid-state devices, we will encounter the term "barrier height." As shown by the curves at the right of Figs. 2-4B, 2-4C, and 2-4D, this is the difference in potential caused by the "barrier width." It simply represents the comparative potential which must be overcome to cause conduction by *majority* carriers.

Of course, for any particular germanium or silicon diode there is a maximum reverse voltage that can be applied before breakdown, or avalanche, occurs. This is the rating known as *peak reverse voltage* (PRV), or *peak inverse voltage* (PIV). It has the same meaning as when applied to the familiar vacuum-tube diode.

Typical diode current-voltage curves are represented by Fig. 2-5. About 0.2 volt of forward bias for germanium, or about 0.6 volt for silicon, is required to cause forward current of any appreciable amount. When the external voltage polarity is reversed, there is a very small reverse current until excessive reverse voltage occurs; at this point, the diode "avalanches." The zener diode uses this characteristic to advantage. We will touch on this subject later, because we will find the zener diode commonly used in modern equipment.

Note that with increasing forward voltage, the curve becomes very steep at about 1 volt. From 1 to 1.5 volts is about the maximum voltage drop that will occur within the normal current ratings of both germanium and

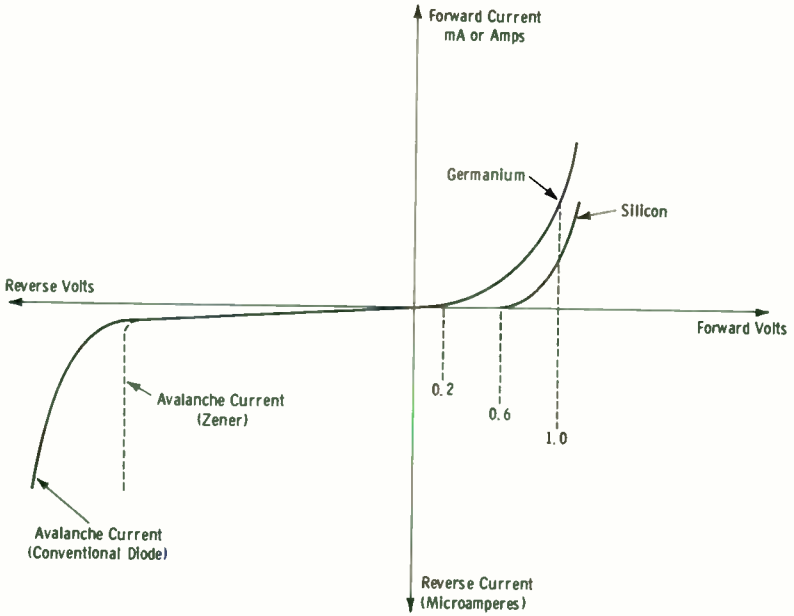


Fig. 2-5. Typical junction-diode current-voltage curves.

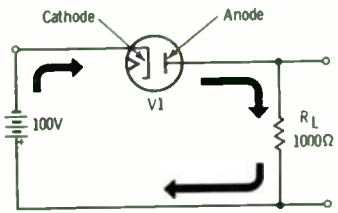
silicon junction diodes. (In this chapter, we are considering "signal diodes" as opposed to "power rectifiers.") These values do not apply to *point-contact* diodes, with which we are rarely concerned in modern solid-state applications. (Exceptions will be noted as they occur.)

2-4. DIODE CIRCUIT ACTION

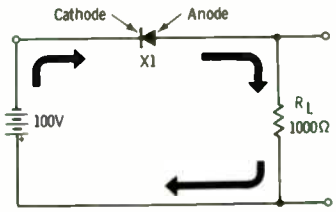
Fig. 2-6A shows the circuit of a forward-biased vacuum-tube diode, and Fig. 2-6B shows the solid-state-diode equivalent. Note that the anode arrow symbol of X1 points in the direction of *positive* current. (This practice is carried over into transistor symbols.) The arrows within the circuit drawings indicate the direction of electron flow.

Figs. 2-6C and 2-6D show each diode replaced with its typical equivalent forward resistance. Follow the current and voltage computations on the drawings. Due to the much lower internal resistance of the crystal as compared to the vacuum tube, greater efficiency results. Voltage values shown on the drawings are with respect to point 1. Note that in each case, the anode is positive relative to the cathode, meeting the condition for forward bias.

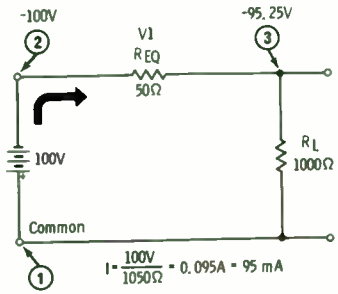
Now study Fig. 2-7, which should clear up one of the aspects most troublesome to newcomers in diode applications. Some diodes are marked on the body with both the symbol and polarity indications as shown. Note



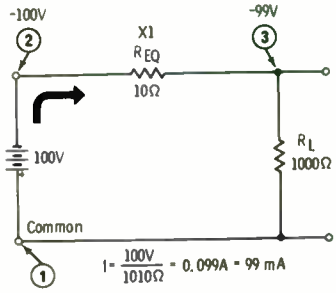
(A) Vacuum-tube circuit.



(B) Solid-state circuit.



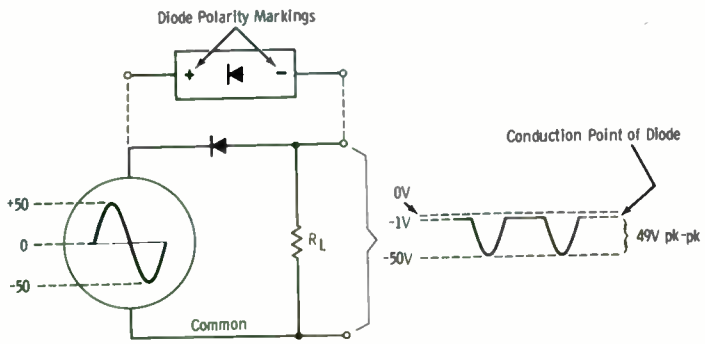
(C) Effect of tube equivalent resistance.



(D) Effect of solid-state-diode resistance.

Fig. 2-6. Diode circuits.

that the polarity given is that which occurs in an active circuit, *not* the condition for forward bias; it is the polarity the diode would have if it were a generator forcing current around the circuit. You know that the anode (arrow) must have an external voltage positive with respect to that at the cathode (bar) for forward conduction. But when the diode is thus forward



Diode polarity markings, when used, indicate signal polarity.

Fig. 2-7. Use of markings on diode.

biased in an active circuit, the signal at the anode will be essentially the same as the signal at the cathode which caused the diode to conduct—in this instance, the negative signal excursion. Of course, if we turn the diode around, the voltage at the top of R_L will be positive.

Some diodes have only the polarity markings without the symbol, and others are color coded to indicate type number (such as 1N34, etc.) and have no designation at all as to which terminal is the cathode and which is the anode. Since there are so many types and styles of diodes with no reliable uniformity of markings, how can we make certain which is the anode lead and which is the cathode lead? Let us take this subject up now.

2-5. HOW TO FIND DIODE POLARITY

The first step in finding polarity is to find out how the red and black leads are connected in the particular ohmmeter to be used. See Fig. 2-8 for a typical circuit, and note that the red lead is actually connected to the *negative* terminal of the 1.5-volt internal battery. If another dc voltmeter is available, simply use it to check the voltage of the VOM red and black leads when the R × 1 range is used. This will tell the polarity. If there is only one meter, take it apart and see in which polarity the leads connect to the battery.

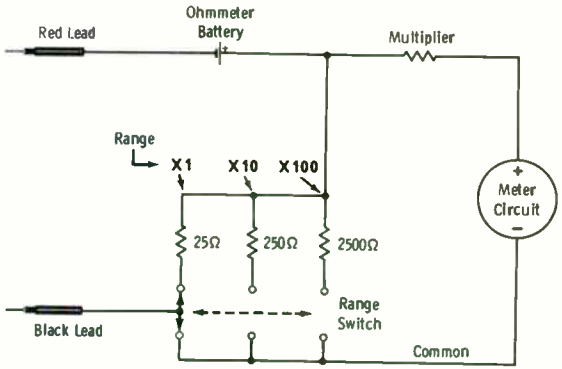


Fig. 2-8. Simplified circuit of typical VOM with switch in ohmmeter position.

Let us take as examples two common meters found in practice: the Weston Analyzer and the Simpson Model 260. Fig. 2-8 is typical of the Weston arrangement when the VOM function switch is placed in the Ohmmeter position: The red lead (marked +) is connected to the *negative* side of the battery, and the black lead (common or −) is positive with respect to the other lead. However, the Simpson Model 260 has a polarity-reversal switch which allows the operator to leave the black lead on common regardless of the polarity of the voltage being measured. When

this meter is operated in the ohmmeter function, we have the following conditions:

With switch in Plus position: red lead (+) is *positive* battery.
With switch in Minus position: red lead is *negative* battery.

When the lead polarity is known, simply connect the red and black leads to the diode and take a reading. Then interchange the leads and take another reading. One polarity will give a low resistance reading; reversing the polarity will give a much higher reading (assuming the diode is not defective). When we find the low-resistance polarity, we will know that the positive battery terminal is connected to the anode, and the negative battery terminal is connected to the cathode. If, for example, the red lead from the meter is negative, the diode terminal to which this lead is connected during the low-resistance reading is the cathode. If we get about the same reading of resistance regardless of how the VOM leads are connected, the diode has broken down and is useless. On the Simpson meter, the polarity switch can be used instead of reversing the lead connections.

Do not expect to get a fixed resistance value when reading diode resistance on the VOM. For example, the "forward-biased" (low-resistance) reading will depend entirely on whether you use the R × 1, R × 10, R × 100, etc., range of the ohmmeter. And herein lies one of the characteristics of solid-state physics. Remember that we are not measuring a fixed resistance such as a resistor. We are actually applying a voltage to a device which has a nonlinear voltage-current characteristic. Current increases or decreases are not necessarily directly proportional to voltage increases or decreases.

At very low voltages, the barrier potential is a hindrance, and several tenths of a volt are required before there is any current. Then, as the voltage increases (forward bias increases), the slope of the current-voltage curve becomes steeper (resistance decreases), and the current increases more rapidly as the voltage increases. In addition to this phenomenon, a close study of the simplified circuit of Fig. 2-8 tells us that when we go from R × 1 to R × 10, we are actually *decreasing* the voltage applied to the diode, and therefore we should measure *greater resistance*. The same effect occurs when we go from the R × 10 to the R × 100 range. (The decrease in applied voltage is the result of increased voltage drop across the larger meter shunt resistors.)

Table 2-2 shows typical readings in ohms (both forward and reverse) for two specific types of small-signal diodes.

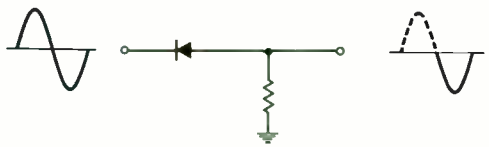
Power-type diodes (used in high-current rectifier power supplies) do not have as great a difference between forward and reverse resistance measurements as do small-signal types. This is normal. There is a considerable variation in forward and reverse resistance measurements, as well as *ratio* of forward and reverse measurements, in all small and miniature diodes. This also is normal.

Table 2-2. Typical Diode Resistance Readings

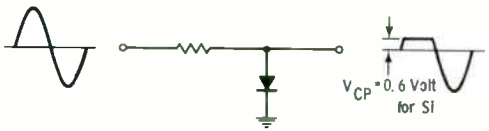
Type 1N34			Type 1N279		
Scale	**Forward R**	**Reverse R**	**Scale**	**Forward R**	**Reverse R**
R × 1	72Ω	Inf	R × 1	16Ω	Inf
R × 10	145Ω	Inf	R × 10	79Ω	Inf
R × 100	500Ω	Inf (almost)	R × 100	450Ω	Inf (almost)
R × 1000	—	700k	R × 1000	—	275k
R × 10,000	—	1.4 meg	R × 10,000	—	470k

2-6. APPLICATIONS FOR SMALL-SIGNAL DIODES

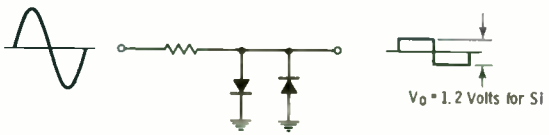
Figs. 2-9A and 2-9B illustrate the conventional signal-diode series and shunt clippers, respectively. In Fig. 2-9B, the forward diode current drawn through the series resistor will result in a clipper potential (V_{CP}) which is about 0.6 volt for a silicon diode. This is especially true for "signal"



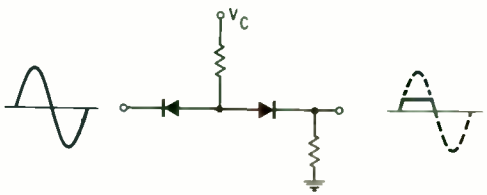
(*A*) *Series.*



(*B*) *Shunt.*



(*C*) *Double shunt.*



(*D*) *Variable level.*

Fig. 2-9. Use of diodes as clippers.

silicon diodes of the *planar epitaxial passivated* (pep) variety. The double shunt-clipper circuit of Fig. 2-9C provides a clipped wave of 1.2 volts peak-to-peak for silicon.

The circuit of Fig. 2-9D illustrates a basic principle of variable clip level. By variation of the dc bias, V_C, the level of diode conduction is adjusted to set the level of clipping. In practice, V_C can be a varying dc voltage from a previous transistor stage, which will "modulate" the applied signal accordingly.

By inspection, we see why the circuit of Fig. 2-10 is called a "corer." (It is also called a "dead space limiter" in analog computers and other electronic control circuitry.) With no dc bias potentials applied, and assuming silicon diodes, X1 will conduct when the applied signal reaches + 0.6 volt. Output will occur through X1 between times a and b, while X2 is cut off. Between times b and c, no conduction can occur. Diode X2 conducts when the input signal reaches − 0.6 volt, and continues to conduct between times c and d. The "core" of the input wave has been removed from the output wave. The spacing of the output wave in Fig. 2-10 is exaggerated for emphasis.

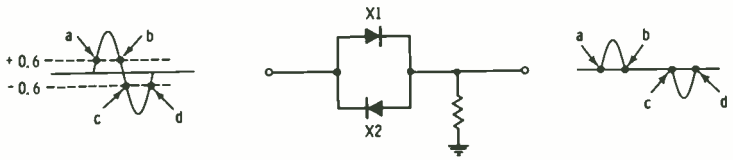


Fig. 2-10. Corer circuit.

It is important to note that the junction voltages as given should not be taken too literally for *all* diodes. Many small-signal diodes, whether germanium or silicon, will show a drop of up to 1 or 1.2 volts if operating near the maximum forward-current rating. Every serious student of solid-state technology should obtain and use a good diode reference book of the latest issue. These books list all characteristics of existing diodes, including forward voltage drop at a given forward current, usually near the maximum current rating of the diode.

The "typical" junction voltage drops for a forward-bias condition are important to remember, however, because they are much more consistent in transistor emitter-base junctions. We will see later that a forward-biased emitter-to-base junction of a transistor just about always has a voltage drop of 0.2 to 0.3 volt for germanium and 0.6 to 0.7 volt for silicon. This voltage is more consistent in a transistor (although influenced to some extent by collector current) because of the accelerating field of the additional collector-base junction. Also, the emitter-base junction is never operating at maximum current rating in small-signal applications.

Applications of small-signal diodes in conjunction with transistors are explained later in this book. Diode *logic circuitry* is also covered later.

2-7. THE ZENER DIODE

The zener diode is designed to be used in the avalanche-current region shown in Fig. 2-5. Fig. 2-11 shows the zener-diode symbol and the basic application as a voltage regulator. Note that the diode is connected so that it operates with the reverse-bias polarity. The zener has two basic specifications, the zener-breakdown voltage and the power rating.

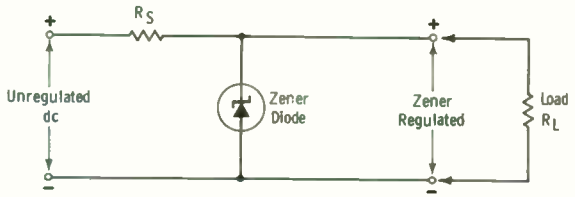


Fig. 2-11. Basic application of zener diode as a voltage regulator.

Returning to Fig. 2-5, note that the reverse-bias current of a diode is very nearly constant until the breakdown voltage is reached. For this reason, it is termed the *reverse saturation current.* ("Saturation" means there is negligible change of reverse current with a change in reverse voltage.) When the zener-breakdown voltage is reached, the reverse voltage is almost perfectly constant for a wide range of current, as evidenced by the practically vertical breakdown-current portion of the curve in Fig. 2-5.

Zener diodes are available with breakdown-voltage ratings from a few volts to over 400 volts. They take the place of gas voltage-regulator tubes in solid-state circuitry, and actually give improved performance over their gas-tube counterparts as voltage regulators.

The power in the zener diode is the product of zener current and volts applied. Therefore the maximum zener-diode current that can be allowed is:

$$\text{Max current} = \frac{\text{Power rating}}{\text{Operating voltage}}$$

In Fig. 2-11, the zener diode is used as a shunt regulating element. Resistor R_S is in series with the parallel combination of the zener and the load; therefore, the total current through this resistor is the total of the zener and load currents. The purpose of R_S is to fix the zener-diode operating point so that regulation will occur over the designed range of load currents and voltage variations, without exceeding the power-dissipation rating of the particular zener used.

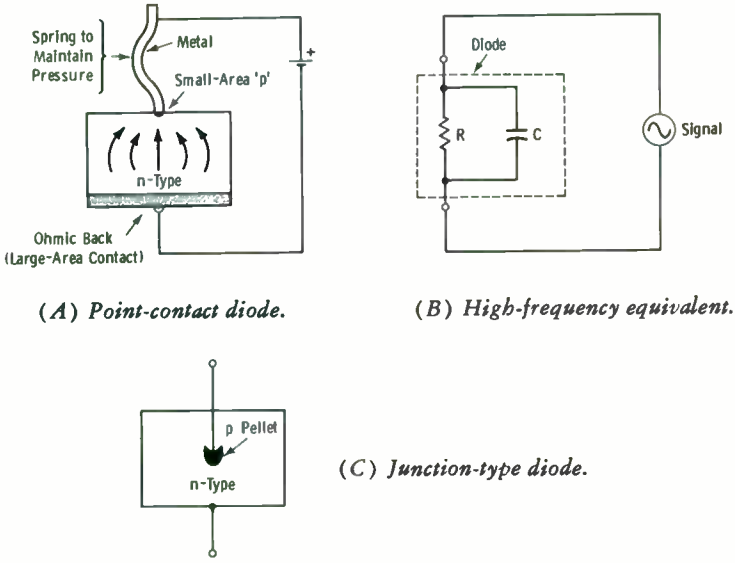
If the input voltage should increase, the current through both the zener and the load will tend to increase. But, as the zener current increases, the

zener resistance decreases, and still more current is passed through the zener junction. The resultant extra current through R_S maintains the voltage across load R_L constant.

Similarly, if the load current increases or decreases, the zener shunt will draw less current or more current, respectively. Thus the diode regulator is capable of maintaining an essentially constant output voltage.

2-8. HIGH-FREQUENCY (MICROWAVE) DIODES

Diodes can be manufactured to function as mixers and detectors at frequencies above one gigahertz (1000 MHz). These diodes are optimized for very low noise and low capacitance. Such characteristics are normally obtained by the point-contact method, or some structure derived from the point-contact principle.



(*A*) *Point-contact diode.* (*B*) *High-frequency equivalent.*

(*C*) *Junction-type diode.*

Fig. 2-12. Diodes for use at high frequencies.

Refer to Fig. 2-12A. The "point contact" with the n-type material is made by a metal "cat whisker." During manufacture, a short surge of current passing through the cat whisker forms a tiny dot, or "island," of p-type material in an impurity region within the n-type block. In use, with voltage applied in the polarity shown, free electrons in the n-type material converge on the point contact. Both conduction and diffusion are involved in the injection of holes from the p-dot area into the n-type region. The junction capacitance is extremely small in this type of diode.

The upper frequency limit of a diode is inversely proportional to the RC product of the series resistance and junction capacitance (Fig. 2-12B). At high frequencies, the capacitive reactance is reduced to near the value of resistance, and the diode shunts out and no longer is able to function as a diode.

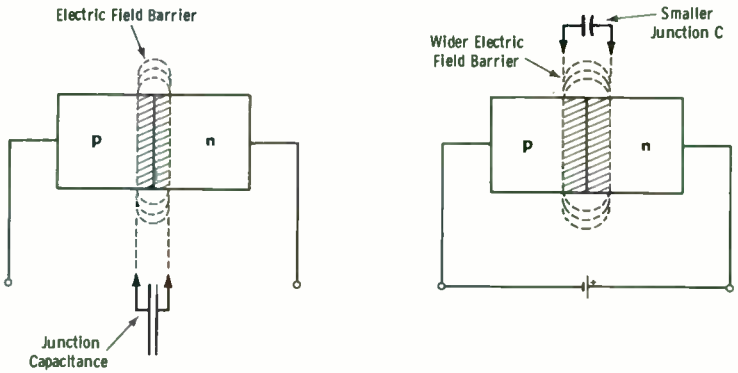
Fig. 2-12C shows a method of obtaining a high-frequency junction diode in which the p region is a tiny hemisphere embedded in an n-type body.

We will examine now how junction capacitance can be put to work rather than being a limitation on performance.

2-9. THE VOLTAGE-VARIABLE-CAPACITANCE DIODE

The width of the barrier in a pn junction is influenced by the voltage across the junction. Since an electrostatic field is thus produced, we have the equivalent of two plates of a capacitor in which the spacing between the plates is governed by the voltage (and current) of the junction.

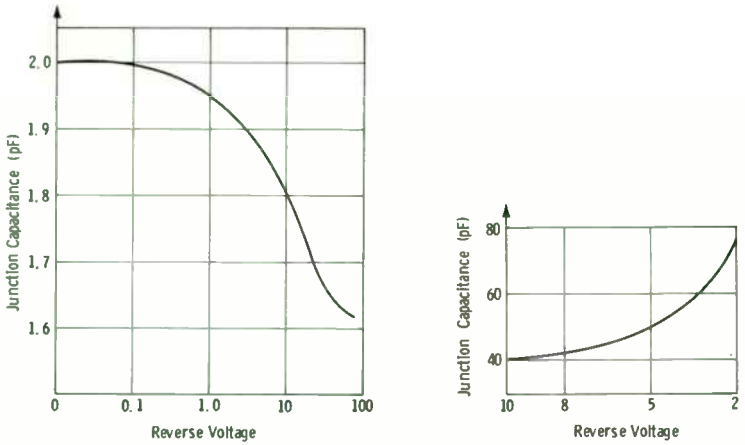
Figs. 2-13A and 2-13B illustrate this effect. Anything that increases the width of the pn junction barrier is equivalent to spreading apart the plates of the capacitor, resulting in less capacitance. As reverse bias is decreased, junction capacitance increases.



(*A*) *Zero bias.* (*B*) *Reverse bias.*

Fig. 2-13. Voltage-variable-capacitance diode.

Fig. 2-14A illustrates the junction-capacitance curve typical of nearly all signal diodes. Note that, in the reverse-voltage region of operation, the capacitance change is quite small over a 100-volt excursion. By comparison, Fig. 2-14B is an example (only) of the curve for one type of *variable-capacitance* diode. There are many different types of variable-capacitance diodes with different sensitivities in pF/volt change. All of these diodes are typically nonlinear in capacitance-to-voltage change, as shown by this graph.



(A) Typical small-signal diode. *(B) Variable-capacitance diode.*

Fig. 2-14. Variation of junction capacitance with voltage.

Some common circuits employ a voltage-variable diode capacitor which may be known as a "variable-capacitance diode," "varicap," or "varactor." This is a diode which is manufactured to maximize certain physical and chemical features affecting junction capacitance. Fig. 2-15 shows three symbols for this type of diode that may be found in practice on schematic diagrams.

Like the zener diode, the variable-capacitance diode is always operated in the reverse-biased condition. Capacitance decreases with increased reverse bias; that is, the capacitance varies inversely with the reverse bias voltage. The capacitance-versus-voltage relationship is nonlinear. The diode normally has a greater change in capacitance for a given change in applied voltage than the effective capacitance change in a conventional reactance-tube circuit.

When the total capacitance used to resonate a tuned circuit is split and used to form a feedback voltage divider, a Colpitts oscillator results. Fig. 2-16A illustrates a transistorized Colpitts oscillator, in which C1 and C2 together set the effective capacitance with which L resonates. Remember that part of this capacitance is "hidden" in junction capacitance of the

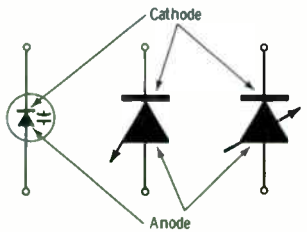
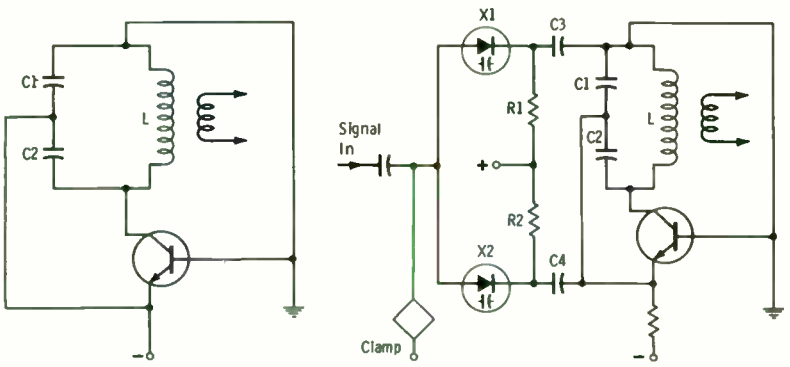


Fig. 2-15. Symbols for voltage-variable capacitance diodes.

transistor. The important point at this time is to understand the effect of a capacitance diode on an LC tuned circuit.

Now look at Fig. 2-16B. This is the same circuit as the one in Fig. 2-16A, but with added components. Variable-capacitance diodes X1 and X2 must remain reverse biased at all times; this bias is supplied through resistors R1 and R2. Capacitors C3 and C4 are large and have negligible reactance to, let us say, a video signal. Now assume that a video signal is applied with sync in the negative polarity. The effective capacitance of X1 and X2 varies with the instantaneous video voltage. Since the diodes are effectively connected to the tank circuit, the resonant frequency is varied in step with the instantaneous video voltage variation. Let us see now in which direction the frequency changes between sync tip and peak white. Since sync is the most negative signal, the reverse bias is increased. Since capacitance varies inversely with the reverse bias, capacitance decreases, *increasing* the output frequency of the oscillator. The same reasoning tells us that as the signal goes toward peak white, the frequency *decreases*. The result is a frequency-modulated (but nonlinear) output.



(A) Colpitts oscillator. *(B) Fm Colpitts oscillator.*

Fig. 2-16. Application for voltage-variable-capacitance diodes.

Please note here that with the same type of transistor and the same polarity of video input signal, X1 and X2 could be reversed in connection of polarity, with a reverse bias now of *negative* rather than *positive* polarity. In this case, the oscillator would be caused to *decrease* in frequency at sync tip and increase in frequency as the signal swings toward peak white. If we take both of the foregoing oscillator circuits and feed the same video signal to both inputs, one oscillator increases in frequency as the other decreases. This is a push-pull type of frequency modulation which tends to cancel the nonlinearity of modulation resulting from the nonlinear voltage-capacitance relationship of voltage-controlled capacitance diodes. When this type of modulation is not used, a nonlinear amplifier of characteristics inverse to those of the modulator restores linearity.

Obviously, this type of application is not limited to the Colpitts oscillator. Nor is it limited to the production of frequency modulation. For example, this type of diode is used in voltage-controlled delay lines (in place of the shunt capacitors) as applied to automatic time correction (atc) in video tape recorders.

2-10. THE CONTROLLED RECTIFIER

The controlled rectifier is the only power-rectifier type of diode we will study in this chapter. The *silicon controlled rectifier* (SCR) has become a very common device in modern solid-state circuitry.

Fig. 2-17 shows a simplified diagram of the construction of an SCR, together with a schematic symbol. The SCR has the following basic characteristics:

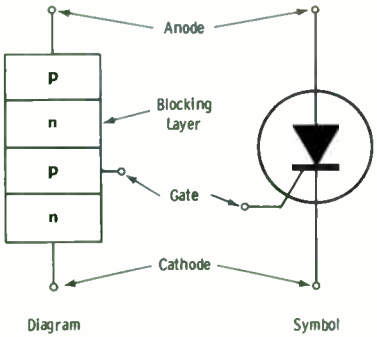
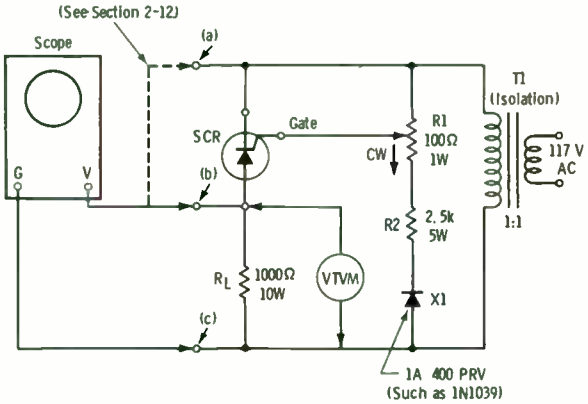
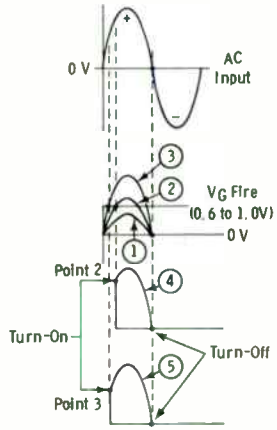


Fig. 2-17. Silicon controlled rectifier.

1. The anode-cathode circuit is normally nonconductive, with extremely high resistance (e.g., 100k) in *both directions.*
2. The gate-to-cathode circuit forms a small diode. Conduction in this diode also influences the "interface" (blocking) layer of n-type material between the anode and gate.
3. If we make the gate lead positive (e.g., 1 volt) relative to the cathode, a small current flows. This current greatly reduces the diode resistance in the direction anode-positive-to-cathode-negative. The resistance in the opposite direction is not affected.
4. The SCR, then, consists of two circuits, the anode-cathode circuit and the gate-cathode circuit, wherein the cathode forms the common reference or terminal.
5. The SCR will pass current *only* when the gate is initially pulsed and the anode is positive relative to the cathode. Once the SCR is conducting, the gate no longer has any control over the current. The SCR will cease conduction only when the anode-cathode voltage drops to a value that is too low to sustain the *holding current.*



(A) Demonstration circuit.



(B) Waveforms.

Fig. 2-18. Operation of silicon controlled rectifier.

A study of the demonstration circuit of Fig. 2-18A should illustrate SCR characteristics. (NOTE: This circuit, with an additional test circuit, is useful in testing SCRs as described in Section 2-12.) Diode X1 produces a half-wave positive pulse across R2 and R1. With gate-voltage potentiometer R1 all the way ccw, the gate voltage (V_G) is zero, and the SCR is nonconducting. The VTVM across R_L will read zero volts.

As R1 is rotated cw toward the junction of R1 and R2, V_G is increased in the positive direction relative to the SCR cathode. The waveform between the arm of R1 and point a is shown by curves 1, 2, and 3 of Fig. 2-18B for three settings of R1. When the amplitude of curve 2 reaches the necessary level, the SCR "fires," and waveform 4 can be observed with the scope between points b and c of the diagram. The VTVM will now

read a voltage across R_L. Conduction ceases when each cycle crosses the ac axis to reverse direction.

Further rotation of R1 in the cw direction raises V_G still more (waveform 3). Note that the SCR is caused to conduct earlier in the cycle, as shown by waveform 5. Therefore the average current delivered to the load is greater.

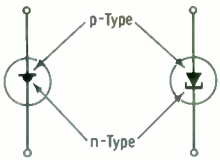
SCR supplies are commonly used in motor speed controls and other devices requiring delivery of a controlled voltage. For example, many modern television-camera chains employ a control module to sense the voltage returned from a long camera cable. Thus voltage can be automatically controlled between rack-mounted power supplies and their loads fed through cables extending from 100 to 3000 feet in length.

2-11. THE TUNNEL DIODE

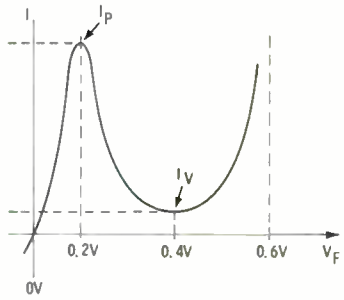
The tunnel diode in its normal form has no rectifying properties, but it can amplify a signal. Since it can amplify, it can oscillate or perform high-speed switching in fast computing systems. Symbols are shown in Fig. 2-19A.

Tunnel-diode junctions are very heavily "doped" with impurities, about 1000 times more heavily than for normal junction diodes. This results in relatively greater conduction abilities, with an extremely thin barrier layer of about a millionth of a centimeter. Junction capacitance is extremely low, and tunnel diodes are used at the upper microwave frequency bands.

Fig. 2-19B illustrates a typical current-voltage characteristic of a tunnel diode. Note that heavy conduction occurs immediately as forward voltage (V_F) is applied. (Compare this to the normal diode curve of Fig. 2-5.) As V_F is further increased, a peak current (I_P) is reached. As V_F is increased again, majority carriers (electrons) in the n-type material can no longer "tunnel" through the thin depletion barrier, so diode current decreases toward a minimum, or valley (I_V). This region is the *negative-*



(*A*) *Schematic symbols.*



(*B*) *Typical characteristic.*

Fig. 2-19. Tunnel diode.

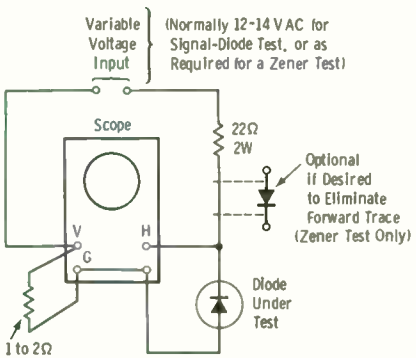
resistance zone (decreasing current with increasing forward bias), and gives the tunnel diode the ability to amplify or oscillate. As V_F is then further increased, the normal transfer curve of a diode prevails, as shown.

A tunnel rectifier (called a *back diode*) is manufactured; in its operation, the reverse current is high and forward current is low. Tunnel rectifiers can provide rectification at much smaller signal voltages than can conventional diodes. High-speed capabilities make them useful in certain computer applications for logic switches or level sensors.

2-12. DIODE TESTING

From previous discussions, we are already familiar with the testing of an ordinary diode with a conventional VOM (high resistance in one direction and low resistance in the other). However, the most reliable check (and one that will clear up many intermittent problems) is made with an oscilloscope. A zener diode can not be checked reliably in any other way. Neither can an SCR unless it reads a low resistance in either direction. The dynamic resistance of a zener diode is only apparent when the breakdown voltage is reached, and the SCR characteristic is still more complex.

The procedure is quite simple for an ordinary diode or a zener diode; see the hookup of Fig. 2-20A. Fig. 2-20B shows the resulting trace for a



(*A*) *Circuit.*

(*B*) *1N34 curve.*

(*C*) *1N279 curve.*

(*D*) *Zener curve.*

Fig. 2-20. Method for testing small-signal and zener diodes.

typical 1N34 diode. Diodes of this type have a natural hysteresis loop as shown, but this loop should remain stable without jitter or erratic "looping" as the variable ac voltage is adjusted around the normal operating voltage. Fig. 2-20C shows the response of a typical 1N279 diode, which gives a "cleaner" trace. In any case, the important thing to observe is any erratic response as the applied ac voltage is varied slowly.

Fig. 2-20D shows the trace we should expect from a zener diode. As we increase the ac voltage from zero upward, the voltage is traced horizontally as shown between points 1 and 2. By adjusting the horizontal-channel scope gain and watching the variable voltage input, we can calibrate the horizontal sweep in volts/cm. When the zener-breakdown voltage is reached (point 2), the voltage trace (horizontal trace) should remain the same length, and the reverse current (downward curve) will increase. *Caution*: Never exceed the wattage of the zener diode being tested; this wattage is the voltage applied to the diode times the diode current. For example, a 1-watt zener with a breakdown voltage of 20 volts should have a *maximum* current of:

$$I_{max} = \frac{\text{Power rating}}{\text{Operating voltage}} = \frac{1}{20} = 50 \text{ mA}$$

It is convenient to connect a milliammeter in series with the diode to avoid exceeding power ratings. By means of the optional series diode connected as in Fig. 2-20A, the forward trace can be eliminated when a zener diode is tested.

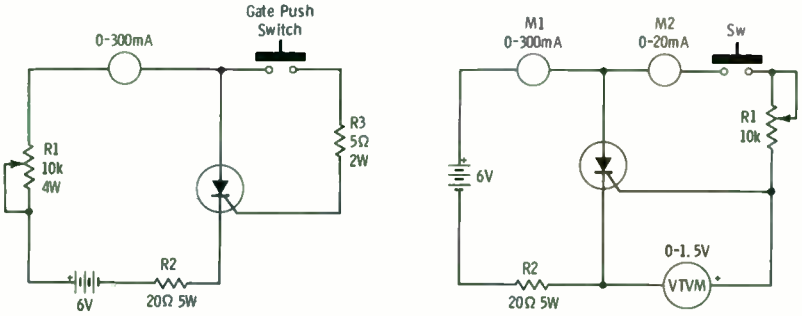
The SCR demonstration circuit of Fig. 2-18A is also a good dynamic testing circuit. The scope should be connected with the ground lead to point c of the diagram. With the scope vertical input connected to point a, the full applied ac waveform can be observed, and the scope amplifier gain and time base can be adjusted to display three to four complete cycles. The lead should then be changed to point b, and the effect of the gate-voltage adjustment can be observed by watching the variation in the angle of conduction. If a dual trace is available, the presentation is more effective.

Now see Fig. 2-21A. Resistor R2 limits the current to $6/20 = 300$ mA. Variable resistor R1 can reduce the forward current to less than 1 mA. With R1 set at zero resistance, momentarily depress the gate switch. This fires the SCR, and we should read about 300 mA of forward current. Note that releasing the gate switch opens the gate circuit, proving that the SCR will continue to conduct so long as the anode is sufficiently positive relative to the cathode.

Now increase the resistance of R1 to reduce the forward current; continue this until the forward current drops abruptly to zero. The current reading just prior to this point is the holding current. Typical SCRs have a holding current between 10 and 15 mA (approximately) at 25°C. At

higher temperatures, the holding current decreases in value. (Note that 25°C is considered normal room temperature; it is equivalent to 77°F.)

The circuit of Fig. 2-21B uses the same parts with the addition of a second milliammeter and a VTVM. Potentiometer R1 has been moved to the gate circuit and is initially set for maximum resistance. Press the gate button and decrease the resistance of R1 until an abrupt rise in forward current is indicated on M1. (The gate button must be held closed). Gate current may then be read on M2, and the gate voltage may be read on the VTVM.



(*A*) *Holding-current test.* (*B*) *Gate-voltage test.*

Fig. 2-21. Method for testing SCR.

Every SCR has its own characteristic of gate-to-cathode voltage and current. Typically, V_G will be about 0.7 volt and gate current about 7 mA. The "normal range" for V_G is from about 0.4 volt to 1.4 volts; for gate current the normal range is about 4 mA to 15 mA.

EXERCISES

Q2-1. Name the two currents involved in the intrinsic (internal) structure of a pn junction.

Q2-2. What is a "hole"?

Q2-3. Of what does current consist in the external circuit of any closed voltage loop?

Q2-4. Does an n-type material contain both electrons and holes?

Q2-5. You connect a battery across a block of n-type material and measure the current. Will you measure the same current if you reverse the battery polarity?

Q2-6. If you do the experiment of Q2-5 at 25°C, and repeat the procedure at 75°C, will you expect the same current with the same voltage?

Q2-7. If you bias a pn junction in such a manner as to increase the depletion region, will the junction field aid or oppose *minority* current?

Q2-8. If you find a diode whose only markings are a + and a −, which marking indicates the cathode end of the diode?

Q2-9. If the zener diode of Fig. 2-11 were connected with the anode to the plus side of the circuit, what would result?

Q2-10. If you remove the load from Fig. 2-11, what happens to the zener current?

Q2-11. If the sine-wave amplitude at the diode of Fig. 2-9B is 0.5 volt peak-to-peak, what would you expect to happen?

Q2-12. If the sine-wave amplitude at the diodes of Fig. 2-10 is 0.5 volt peak-to-peak, what would you expect to happen?

Q2-13. Can you check an SCR with an ohmmeter as you would an ordinary diode?

Q2-14. Give the two conditions necessary for a normal SCR to allow conduction.

Q2-15. Do SCR characteristics change with varying operating temperatures?

CHAPTER 3

Understanding the Transistor

We are now ready to approach the basic action of the transistor from a unique point of view. A word of caution to those who have already trained in solid-state fundamentals: Study and follow this chapter closely! It is slanted to provide the proper comprehension necessary to possess the best analytical tool anyone can have: to do quickly an adequate circuit analysis for troubleshooting or evaluation purposes.

3-1. WHAT THE CIRCUIT MUST DO

First of all, among many other applications, the transistor must do basically the same thing the vacuum tube does: it must be capable of amplifying a signal. So let us take a look at a theoretical network, composed entirely of passive elements, which could do this job based on the following action:

1. An input current is injected into a low-resistance network.
2. The same current that is present in this low-resistance network is transferred to a high-resistance output circuit without reducing the current. We recognize this type of circuit as being a constant-current signal source.

See Fig. 3-1. When the switch is in the A position, we have a 30-volt battery in series with 30 ohms, so there is 1 ampere of current through 30 ohms for a 30-volt drop and 30 watts of power dissipated in R1. Then we throw the switch to position B. Suppose we have invented a physical negative resistance (−R), which is placed in series with R2 and exactly cancels the 3000-ohm resistance of R2. Now we will have exactly the same current in the output resistance (R2) as we have in R1. We do not get a current gain, but we do get power and voltage gain simply because we have transferred the given (fixed) value of current from a low-resistance to a high-resistance load.

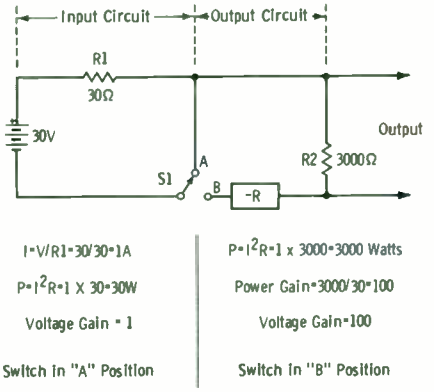
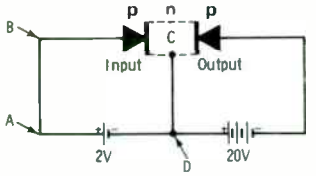


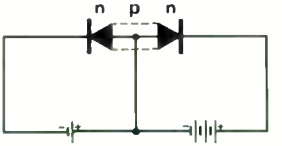
Fig. 3-1. Hypothetical current-transfer network.

3-2. THE SOLID-STATE DIODE AGAIN

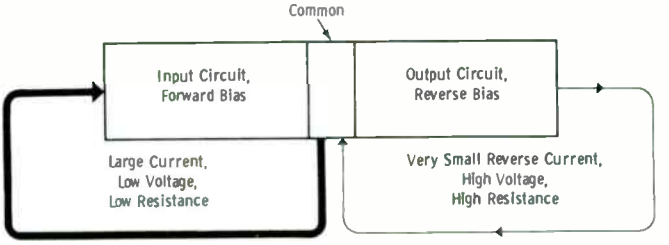
A diode can provide either a low resistance or a high resistance depending upon the polarity of external bias applied. Fig. 3-2A is the representation of two diodes back-to-back, with forward bias on the "input" diode, and reverse bias on the "output" diode. The current shown in Fig. 3-2C results. Current passes easily from A to B to C to D. Let us stay with the direction of "positive current" at this time because of a special significance we will see shortly. Just remember that the direction of *electron* flow is from D to C to B and back to the positive terminal at A. Of course, we



(A) Pnp arrangement.



(B) Npn arrangement.



(C) Current paths.

Fig. 3-2. Diodes connected back-to-back.

can also connect two diodes back-to-back with the polarity shown by Fig. 3-2B. In this case, the battery polarities are reversed to obtain the necessary bias voltages.

Since the output diode is reverse biased, the reverse current is very small (microamperes). Obviously, no "gain" of any kind results. Also, a change in the input voltage or current has no control over the output current or voltage. Even changing the output diode voltage has practically no effect, since the reverse current is essentially constant over a wide range of reverse bias voltage (covered in Chapter 2).

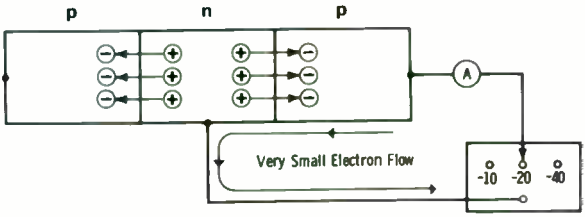
It is obvious that a transistor is not simply two diodes back-to-back with forward and reverse bias applied. But the diode principle is the very action upon which the transistor operates. Let us see how this principle is put to use in practical devices.

3-3. CONDITIONS OF TRANSISTOR OPERATION

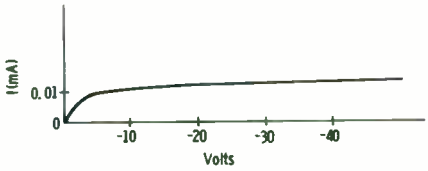
See Fig. 3-3A. Assume the back-to-back diodes are now formed within a single crystal structure by regional doping to make a pnp formation as shown. We attach a tapped battery source to reverse-bias the output side of this structure, and plot the curve illustrating the reverse-bias characteristic (current versus reverse voltage). The curve shown in Fig. 3-3B is typical. The only current is about 0.01 mA (or less) of reverse current between −10 and −40 volts; this is the reverse saturation current. Thus far, we recognize conventional diode action.

Now, keeping the same output-circuit hookup, we forward-bias the input circuit as in Fig. 3-3C. There are three ammeters: one in the input circuit, one in the common circuit, and one in the output circuit. We adjust variable resistance R to obtain 1 mA of input current. When we do this, we get (for example) 0.98 mA of output current (Fig. 3-3D) and only about 0.02 mA of "common" current (Fig. 3-3E). In other words, about 98 percent of the input current is present in the output circuit (*adding* to the reverse current), and only about 2 percent of the input current is present in the common leg. We know that the output circuit is a reverse-biased diode, and therefore presents a high resistance. So we have transferred a given current from the low-impedance input circuit (forward-biased diode) to the high resistance in the output with *very little* loss.

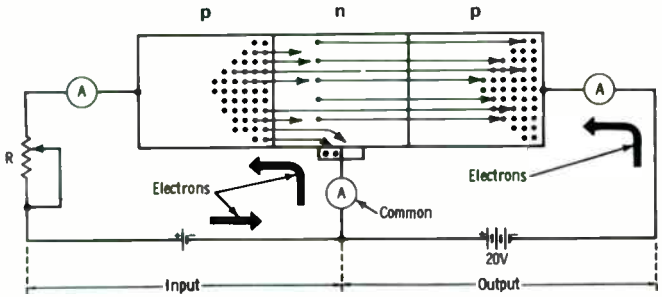
Here is the reason for the action of Fig. 3-3C. The input-common junction is forward biased. The majority carriers (holes) in the p-type region are injected into the n-type material, where they are minority carriers. Now if these holes were not influenced by the output area (again a p-type region), they would simply flow down through the common terminal in the normal junction-diode manner. This would, of course, result in a large electron flow from the common terminal, through the input area, and into the positive battery terminal.



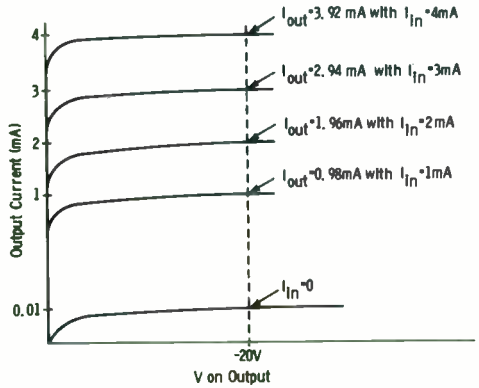
(A) Reverse-biased output junction.



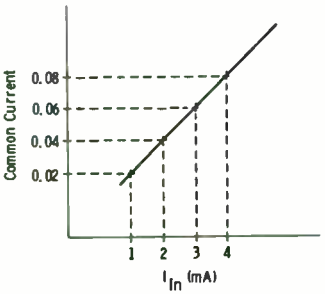
(B) Reverse-current characteristic.



(C) Forward-biased input junction.



(D) Output-current characteristics.



(E) Common current.

Fig. 3-3. Current relationships in a transistor.

But the direction of the output-to-common field is such that most of the holes are accelerated through the common region and injected into the output region. (A few of them do flow into the common battery terminal, and these are lost in contributing to the output current.) The holes that reach the output area move toward the strong attraction of the negative potential at the output terminal. Note that although the majority carriers in this pnp structure are holes, the action simply results in a large flow of electrons in the external circuit.

There are three basic requirements in a practical transistor structure:

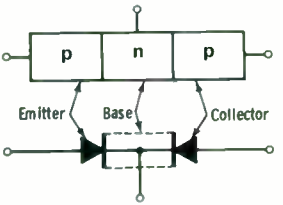
1. The p and n regions must be part of a single crystal structure.
2. The "common" region is not doped as heavily as the other two regions. For example, the p material of the pnp structure is doped more heavily than the n (common) region. This insures that on the right side of the input-common junction of Fig. 3-3C the forward current (holes) will be accelerated more easily to the output area than to the common terminal.
3. Although the common area (n-type in the pnp structure) is not as heavily doped as the other two (p-type) areas, many free electrons are present in the area. Therefore some of the holes are bound to combine with the electrons and diffuse to the common battery terminal. The number of holes remaining to be accelerated by the output field depends on the distance of travel required in the common region. So to obtain a practical efficiency, the common area is made very thin (less than one-thousandth of an inch in many cases) with respect to its cross-sectional area. This helps to assure that most of the minority carriers in the common area are accelerated into the output junction field to become useful current.

An npn structure is also practical. This simply means that the first block of Fig. 3-3C would be n-type material, the common block p-type material, and the output block n-type material. Battery polarities would be reversed, and majority carriers within the crystal structure would be electrons.

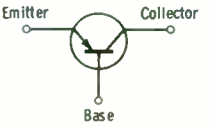
3-4. THE BASIC TRANSISTOR SYMBOL

See Fig. 3-4A for the normal pnp configuration we have been discussing. The lower part of the diagram shows the corresponding symbol if conventional diode representation were used. But from our previous discussion, we know that the "output" arrow is pointing in the direction of flow of electrons, not positive charge. So we know immediately that our description of the diode symbol must be modified as follows: "The diode arrow points in the direction of positive current *when the diode is forward biased.*" As a result, the pnp-transistor symbol is drawn as in Fig. 3-4B,

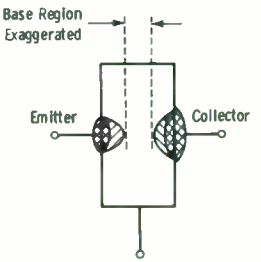
with the arrow on the "output" side deleted. The element with the arrow is designated the *emitter*, the common element is termed the *base*, and the output element is the *collector*. The arrangement of the series of letters pnp or npn is always to designate emitter, base, and collector, in that order. Although the emitter and collector are always the same kind of material (p type or n type), their construction within the crystal is not the same. Efficiency is increased by doping a larger area for the collector than for the emitter (Fig. 3-4C). This is the reason why, although the transistor *can* be used with the emitter and collector leads interchanged to the external circuit, the action is only very limited, and extreme loss of efficiency usually occurs. In later chapters, we will discover there are some transistors that have true bidirectional characteristics and are intended to operate in both directions. In the symbol for these transistors, both the emitter and the collector have arrows.



(*A*) *Simplified structure.*



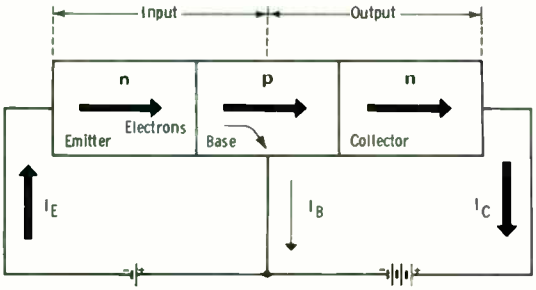
(*B*) *Pnp transistor symbol.*



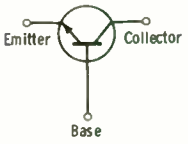
(*C*) *Pictorial diagram.*

Fig. 3-4. Evolution of symbol for pnp transistor.

Fig. 3-5A represents the npn transistor. In this case, free electrons move through the emitter to the emitter-base field. These electrons are injected into the base area (p type), where they become minority carriers. A few are combined with the holes in the vicinity of the common terminal, but most of them are accelerated by the collector-base junction field toward the strong attraction of the positive potential on the collector terminal. This movement of electrons constitutes the "output" or collector current. Fig. 3-5B shows the symbol for the npn transistor. Since the emitter-base junction is a forward-biased junction, the arrow points in the direction of "positive current" (opposite to electron flow) and therefore points away from the base.



(A) Simplified structure.



(B) Npn symbol.

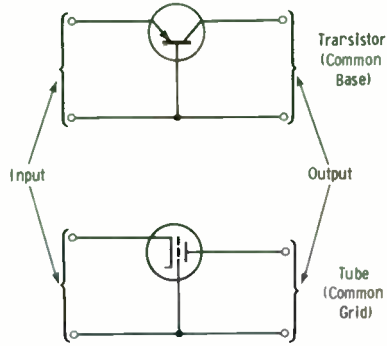
Fig. 3-5. Npn transistor.

In essence, transistor action can be described as *injection* (forward-biased emitter-base junction) of *minority carriers* into the *base region*, *diffusion* of these minority carriers through the base to the region of influence of the *electric field* (reverse-biased collector-base junction), and *acceleration* of the minority carriers across the collector junction for *collection* as output current. The emitter may be considered the source of injection into the base area, comparable to the vacuum-tube cathode, which emits electrons into the space around the grid of the tube. The base then becomes comparable to the vacuum-tube grid, and the collector becomes comparable to the plate.

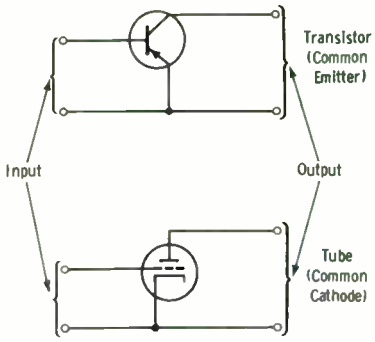
3-5. COMPARISON OF TRANSISTORS AND VACUUM TUBES

Fig. 3-6 illustrates the comparable features of transistors and vacuum tubes. Please note that the transistor input circuit discussed thus far is comparable to that of the vacuum-tube common-grid, or grounded-grid, circuit (Fig. 3-6A). This has been only for convenience in developing transistor circuit theory. In Fig. 3-6B, the input is between base and emitter, with the emitter instead of the base the common element. This is comparable (please note we did not say "identical") to the conventional grounded-cathode tube circuit. In Fig. 3-6C, the input is the same as in Fig. 3-6B, but the output is from the emitter; this circuit is comparable to the tube cathode-follower circuit. Such comparisons are primarily useful in relating signal polarity, because:

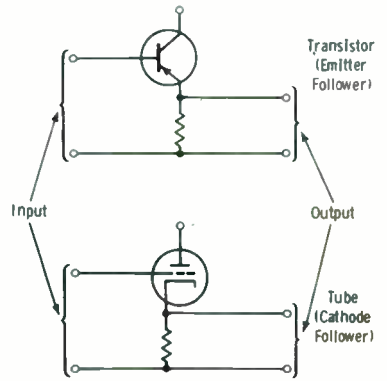
1. In the common-base (common-grid) circuit, the output signal is of the same polarity as the input.
2. In the common-emitter (common-cathode) circuit, the output signal is inverted in polarity from the input signal.
3. In the emitter-follower (cathode-follower) circuit, the output signal is of the same polarity as the input.



(A) Common grid/common base comparison.



(B) Common cathode/common emitter.



(C) Cathode follower/emitter follower.

Fig. 3-6. Comparison of transistors and tubes.

3-6. "CURRENT POLARITY"

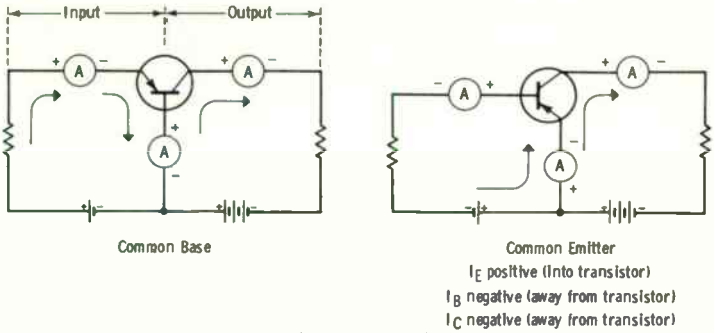
When we begin reading transistor specification sheets and looking at transistor graphs, we will need to know the significance of "current polarity." There are just two ways to feed the input of a transistor:

1. To the emitter.
2. To the base.

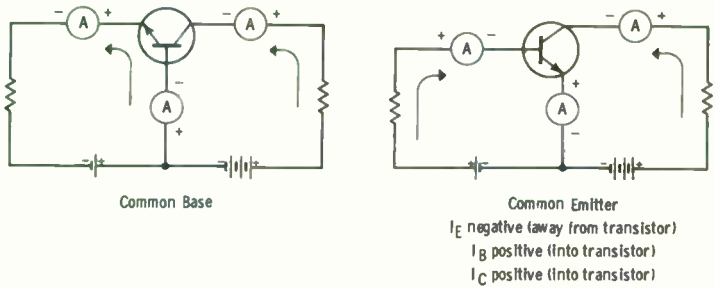
Similarly, there are just two ways of getting the signal out of the transistor:

1. From the collector.
2. From the emitter (in the emitter-follower circuit).

In Fig. 3-7A, observe the pnp transistor connected with both types of inputs. The arrows indicate the direction of "flow" of positive charge, or "conventional current" (opposite in direction to electron flow). It is also "conventional" in network theory to term all conventional currents *into*



(*A*) *Pnp transistor.*



(*B*) *Npn transistor.*

Fig. 3-7. Conventional current in transistors.

the device positive currents, while terming conventional currents *away from* the device negative currents. Note that regardless of the hookup for the pnp transistor, the emitter current would be positive (into the transistor), the base current negative (away from the transistor), and the collector current negative (away from the transistor).

For the npn transistor of Fig. 3-7B, the emitter current is termed negative (away from the transistor), the base current positive (into the transistor), and the collector current positive (into the transistor).

Therefore, we will notice that on some manufacturer specification sheets for specific transistors, we have:

Pnp Types	*Npn Types*
Emitter current (I_E) is positive.	Emitter current (I_E) is negative.
Base current (I_B) is negative.	Base current (I_B) is positive.
Collector current (I_C) is negative.	Collector current (I_C) is positive.

Do not let this type of data presentation be confusing. The important point to keep in mind is that, regardless of the type of charge carriers

involved in internal transistor function, the external current is by electrons, or from the negative terminal of the power supply to the positive terminal. When called upon to connect a milliameter into a transistor circuit (as in Fig. 3-7), we would insert it with the normal polarity determined by the direction of electron flow. This is exactly the same as in any circuit hookup, so we are on familiar ground here. In practice, we normally read emitter current, base current, and collector current in microamperes, milliamperes, or amperes without regard to "polarity" of current. It is simply necessary that this "element of mystery" be removed in reading specification sheets and graphs. Some manufacturer data sheets and graphs ignore this type of "current polarity," but many of them designate the polarity.

3-7. BASIC LAW OF SEMICONDUCTOR PHYSICS

There is a basic physical parameter in solid-state physics from which can be derived a "magic number" that can prove to be a powerful analytical tool to use. We already know that in checking the forward and back resistance of a diode, actual resistance as indicated by the VOM depends on the scale used—in other words, on the voltage applied. The basic law presented in this section brings home the "why" of this characteristic, which, after all, simply indicates the amount of current through the diode.

It is not important to memorize the following formula nor to understand why it exists in the form given. The important point is to see from where a fundamental number, which we will use often in circuit analysis, is derived. This basic law establishes (approximately) the effective resistance of the emitter of a transistor, whether pnp or npn, and regardless of the circuit hookup (which must always be considered separately anyway). We will find out how important this single parameter can be in total circuit analysis as we progress. The parameter is the *small-signal emitter resistance*; it depends on the dc value of emitter current:

$$r_e = \frac{kT}{qmI_E}$$

where,

r_e is the small-signal emitter resistance in ohms,
T is the temperature in degrees Kelvin ($°C + 273$),
k is Boltzmann's constant (1.38×10^{-23} watt-sec/°C),
q is the charge of an electron (1.6×10^{-19} coulomb),
m is a constant (1 for germanium and between 1 and 1.5 for silicon), and
I_E is the dc emitter current.

The above relationship says that the small-signal emitter resistance depends on the dc operating point and the ambient temperature. In the

following manipulations, we will assume room temperature to be 25°C, which makes T about 300°K.

$$r_e = \frac{1.38(10^{-23})300}{1.6(10^{-19})I_E} = \frac{0.0414(10^{-19})}{1.6(10^{-19})I_E} = \frac{0.026}{I_E}$$

Now to keep the powers of ten in line with milliamperes instead of amperes,

$$r_e = \frac{26}{I_E}$$

where I_E is expressed in milliamperes.

This equation says that we can readily approximate the emitter resistance presented to any small signal (as distinguished from signals applied to power and switching devices) by simply dividing the dc value of emitter current (in milliamperes) into 26. Although the value of the constant, m, is slightly higher for silicon, in practice the same value can be used for both germanium and silicon transistors.

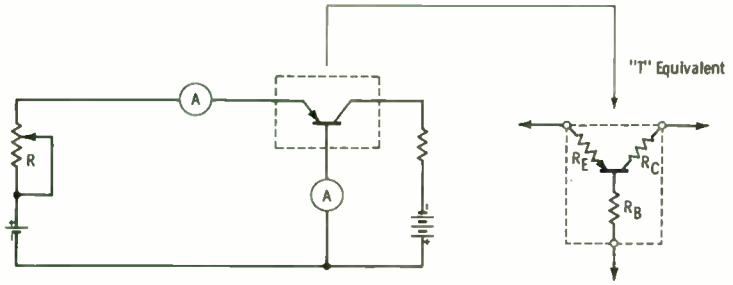
NOTE: When bias conditions are such that the largest ac signal to be amplified is small compared to the dc bias current and voltage, the transistor is said to be operating in the *small-signal mode*. This type of operation includes most conventional amplifiers (audio and video), until we get to large power outputs or to switching devices which obviously must handle signals or pulses greater in amplitude than the bias currents and voltages.

3-8. THE IMPORTANCE OF SMALL-SIGNAL EMITTER RESISTANCE

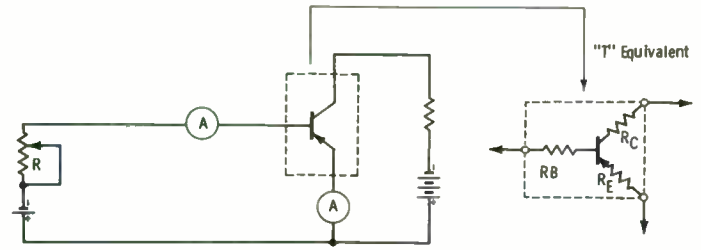
In the graph of Fig. 3-3D, the voltage applied to the output element (collector) has little effect on the output current. The output (collector) current depends almost entirely on the input (bias) current. Also remember from Fig. 3-3E, the graph of common current versus input current (in this case base current versus emitter current), the base current increased by an amount that is small (only 2 percent compared to the amount the emitter current increased.

Now bear this in mind: In the small-signal mode, regardless of how the transistor is connected to the external circuit (common emitter or common base), the base-current change is always *much less* than the emitter-current change. This statement is true because the collector (output) current is always almost the same as the emitter current, while the base current is always only the difference between the emitter current and collector current.

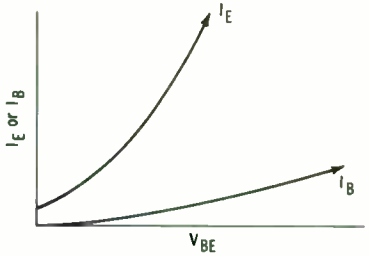
Fig 3-8A shows a common-base hookup; Fig. 3-8B shows a common-emitter hookup. Both transistors are the pnp type. We will be using both pnp and npn types from now on. At this point, the reader should recognize



(A) Common-base circuit.



(B) Common-emitter circuit.



(C) Current-voltage curves.

Fig. 3-8. Basic transistor-impedance relationships.

immediately which type is used, and what the battery polarity should be for normal operation (input junction forward biased, output junction reverse biased).

The diagrams at the right in Figs. 3-8A and 3-8B show the T equivalents of the internal transistor elements. The arrows indicate the points at which the external circuit is connected. In Fig. 3-8A, the input (dc in this case) is to the emitter; in Fig. 3-8B the dc input is to the base. We will assume that the collector is simply operated at a fixed voltage which is negative with the respect to the common element.

Now if we consider *only* the junction formed in the emitter-base region, and we vary the base-to-emitter voltage (V_{BE}) by means of R, we will

have an I-E plot roughly similar to that of Fig. 3-8C. In the common-base circuit (Fig. 3-8A), we already know from the graph of Fig. 3-3D that the collector current will increase almost in direct proportion to the increase of emitter (input) current. A very small percentage of this current passes into the base lead, so a slight increase of base current results.

In the common-emitter circuit (Fig. 3-8B), the input is now to the base. A very small increase in V_{BE} that could cause a change of, say, 1 mA in emitter current would result in, for example, a change of only 0.02 mA in base current. We can say this in another way: A change of only 0.02 mA in the input circuit now results in a change of almost 1 mA in the output circuit. So this type of hookup (common emitter) results in *both* current gain and voltage gain.

NOTE: The capital subscript letters (such as in V_{BE}) indicate dc changes. When we speak of signal changes to be superimposed on the dc bias current, the subscripts will be in small letters, for example, V_{be}.

At this point we can develop two basic parameters of a transistor: *Alpha* is the term used to designate the current gain of a *common-base* (emitter-input) circuit. It is the ratio of output (collector) current to input (emitter) current. In the example of Fig. 3-3, alpha (α) is equal to 0.98; that is, 98 percent of the emitter current is transferred to the collector. There is a current loss, but the circuit is capable of giving large voltage gains.

Beta is the term used to designate the current gain of a *common-emitter* (base-input) circuit. It also is the ratio of output (collector) to input (base) current. Note that in either case the definition is in terms of a ratio of output to input current. The difference is that the "input" in one case is the emitter and in the other case is the base. If we use the same transistor employed in Fig. 3-3 in a common-emitter circuit, beta (β) is approximately $1/0.02 = 50$. A change of 0.02 mA in the input (base) caused a change of approximately 1 mA in the output (collector) circuit.

Now return to Fig. 3-8C; any plot of current and voltage also contains resistance or impedance information ($R = V/I$). The resistance is represented by the *slope* of the curve in an E-I graph, and, therefore, by the reciprocal of the slope of the curve in an I-E graph such as Fig. 3-8C. It is obvious that the slope of the I_E curve is much greater than that of the I_B curve; therefore, the emitter resistance is *much less* than the base resistance (greater current change for a given voltage change). We now have two basic factors by which we can "tie down" the approximate relationship of the two resistances:

1. The *small-signal* emitter resistance is $26/I_E$. For example, if the emitter has a bias current of 1 mA, the small-signal resistance is 26 ohms. Since any signal on the emitter is superimposed on the dc

bias current, we can say that the slope of the I_E curve indicates approximately $26/I_E$ of resistance (in ohms) to a small signal (where I_E is expressed in mA).

2. We also know that the emitter current is approximately β times the base current. To put this in terms of resistance, the resistance corresponding to the I_B curve is approximately β times that corresponding to the I_E curve. (Remember that the symbols α and β represent alpha and beta, respectively).

So from recognizing these relationships, if we know either resistance, we can find the other. And we *do* know one:

$$r_e = \frac{26}{I_E}$$

It is true that the figure 26 is subject to wide variation in practice. That is why transistor parameters as given in specification sheets and graphs are only "design-center" values. It is also why stabilization circuitry is necessary in practical circuits, as covered in future chapters.

Now to apply resistance relationships to transistor circuits: Assume that either one of the circuits of Fig. 3-8 has a small signal superimposed on the input-circuit dc bias. The reciprocal of the slope of the I_E curve is:

$$\frac{\Delta V_{BE}}{\Delta I_E}$$

where the symbol Δ (delta) means a small change in the quantity that follows it.

Note that in the case of the common-base circuit, this is the ratio of change in input voltage to the change in input current:

$$\frac{\Delta V_{in}}{\Delta I_{in}}$$

because the emitter is the input element. This ratio, then, is the input resistance ($R = V/I$). In the case of the common-emitter circuit (input signal to base), the ratio of change in input voltage to change in input current is much higher, indicating a much higher input impedance. But the total input circuit is the forward-biased base-emitter junction. This means that the input signal current is flowing in the input-to-common junction regardless of the input element used. Therefore it makes no difference in using the r_e parameter whether the emitter or base is used as the input element. It is simply necessary for r_e to represent the *resistance seen looking into the emitter*. From this single parameter, r_e, we can closely approximate the input resistance and the voltage amplification of any circuit, as we shall see shortly.

Let us very briefly review comparable vacuum-tube parameters so that we can more readily grasp this convenient analytical tool.

$$g_m = \frac{\Delta I_P}{\Delta V_G}$$

This equation says that the transconductance of a tube is the ratio of a small change in plate current to the change in grid voltage producing it. It also means that this ratio is the change in *output current* divided by the change in *input voltage*.

The reciprocal of conductance is resistance. The reciprocal of transconductance is the *mutual resistance* of the tube:

$$r_m = \frac{\Delta V_G}{\Delta I_P} = \frac{\Delta V_{in}}{\Delta I_{out}} = \frac{1}{g_m}$$

Now assuming a transistor has a high β, the change in input current (ΔI_E) is approximately equal to the change in output current (ΔI_C). So now we can see that the reciprocal of the slope of the I_E curve of Fig. 3-8C closely approximates:

$$\frac{\Delta V_{in}}{\Delta I_{out}}$$

which is the same relationship as the *mutual resistance* of a tube. To sum up thus far:

$$r_e = \frac{26}{I_E} = 1/g_m \text{ of the transistor}$$

From this relationship, we can see immediately that:

$$g_m = \frac{I_E}{26}$$

In this equation, g_m is in mhos when I_E is in milliamperes.

Now study Fig. 3-9. This schematic shows the small-signal equivalent of any transistor. Resistance r_e ($1/g_m$, or $26/I_E$) is the dynamic resistance of the input junction due to carrier action. Resistance R_{EB} represents the dc resistance in the emitter and base leads, as well as the ohmic contact within the pn region. For analysis (ignoring large power-type transistors or switching applications) this ohmic value can be assumed to be between 2 and 6 ohms. The collector resistance (r_c) is very high because of the reverse bias. Note that the "transresistance" is the sum of r_e and R_{EB} and that the total dc ohmic value (R_{EB}) lumps into one resistance in series with r_e in the emitter region of the transistor. To this must be added any external emitter resistance (R_E) which is not bypassed by a capacitor.

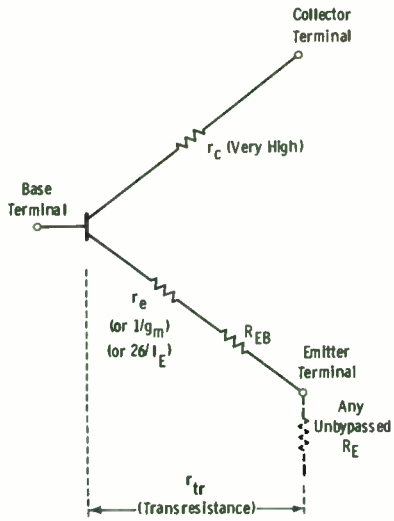


Fig. 3-9. Small-signal equivalent network of transistor.

Resistance R_{EB} may or may not enter into the analysis, depending on the emitter current. For example, at 0.26 mA:

$$\frac{1}{g_m} = \frac{26}{0.26} = 100 \text{ ohms}$$

If we take a median value of 4 ohms for R_{EB}, we see that it is negligible relative to the 100 ohms. However, at 2 mA of I_E:

$$\frac{1}{g_m} = \frac{26}{2} = 13 \text{ ohms}$$

In this case, an R_{EB} of 4 ohms is an appreciable part of r_{tr}.

One more fundamental point: The input resistance for the common-base circuit, since the emitter is the input element, is equal to r_{tr}. However, the input resistance of the common-emitter circuit (input signal to base) is the transresistance times beta. We have already seen that the resistance looking into the base is β times that looking into the emitter. So here is the input-resistance relationship:

Common base: $$r_{in} = r_{tr} = \frac{26}{I_E} + R_{EB} + R_E$$

Common emitter: $$r_{in} = \beta r_{tr} = \beta\left(\frac{26}{I_E} + R_{EB} + R_E\right)$$

Now for voltage amplification (A_v):

$$A_v = \frac{V_{out}}{V_{in}}$$

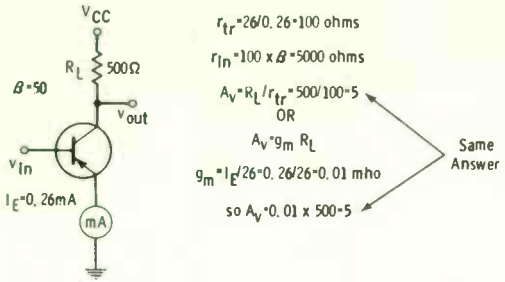


Fig. 3-10. Voltage gain, small emitter current.

or simply the ratio of the output voltage to the input voltage. But we consider r_{tr} to be in the input circuit, so we can put the voltage amplification in terms of the ratio of dynamic impedances presented to the signal:

$$A_v = \frac{R_L}{r_{tr}}$$

For a practical example, take the circuit of Fig. 3-10. The emitter current is 0.26 mA, and the load resistance is 500 ohms. From the specification sheet for the type of transistor employed, we find a beta of 50. Follow the computations in the illustration for r_{in} and A_v. Note that we have gone a step further and calculated the gain using the old "rule of thumb" that the voltage amplification is approximately equal to g_m times R_L. In this case (I_E less than 1 mA), the two answers agree.

Now go to Fig. 3-11, which is the same as Fig. 3-10 except that the emitter current is now 2 mA. Follow the computations on the drawing. Note that at the higher emitter current, the relationship g_m R_L gives a different answer. The A_v in terms of r_{tr} is the most accurate at emitter currents over 1 mA, due to the effect of R_{EB}, which was not contained in the computation for transconductance.

There is a convenient way around this difficulty, as the remaining computations in Fig. 3-11 show. If the transresistance is the sum of r_e and

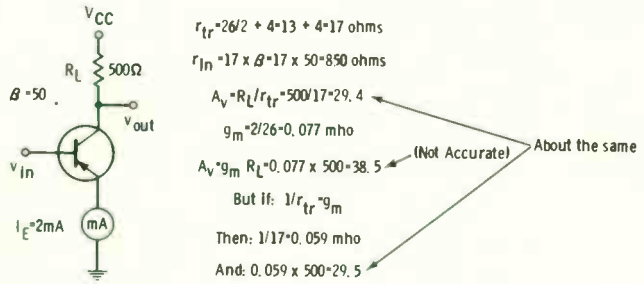


Fig. 3-11. Voltage gain, larger emitter current.

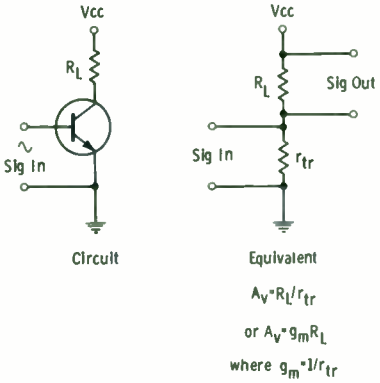


Fig. 3-12. Effective "transconductance" of a transistor.

ohmic resistance R_{EB}, then the reciprocal of r_{tr} is the g_m of the device for simplified analysis procedures. We know from the previous computation that omitting the effect of R_{EB} gave us a value for A_v that is too high. So let:

$$g_m = \frac{1}{r_{tr}} = \frac{1}{\frac{26}{I_E} + R_{EB}}$$

and note that if we *also* include in r_{tr} any external (unbypassed) resistance between the emitter and ground, we can closely estimate the effect on A_v of using the additional emitter resistance. (Such resistance acts as a form of stabilization, just as the cathode resistor acts in vacuum-tube circuits.)

To understand this point, study Fig. 3-12. The input signal, whether applied to the emitter or base, is across the transresistance, r_{tr}. Now add an external emitter resistor as in Fig. 3-13. In this example, the input

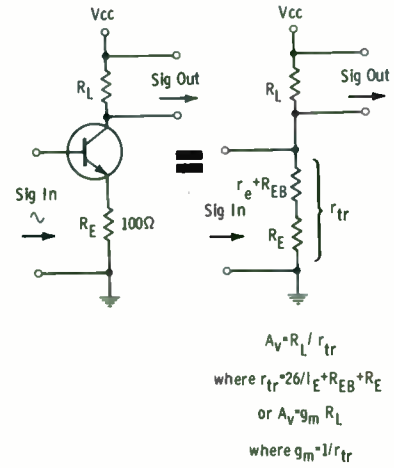


Fig. 3-13. "Transconductance" including emitter resistor.

signal is across the sum of r_e, R_{EB}, and external resistor R_E. The sum total is the transresistance. Let us assume that the circuit of Fig. 3-13 is the same as the circuit in Fig. 3-11 except that the added emitter resistor is 100 ohms. (A different bias voltage would be necessary to obtain the 2-mA emitter current.) We have:

$$R_L = 500 \text{ ohms}$$
$$I_E = 2 \text{ mA}$$
$$\beta = 50$$

Then,

$$r_{tr} = \frac{26}{I_E} + R_{EB} + R_E$$
$$= 13 + 4 + 100 = 117$$

$r_{in} = 117(50) = 5850$ ohms (increased from 850 ohms in Fig. 3-11.)

$$A_v = \frac{R_L}{r_{tr}} = \frac{500}{117} = 4.27 \text{ (Reduced from 29.4 in Fig. 3-11.)}$$

$$g_m = \frac{1}{r_{tr}} = \frac{1}{117} = 0.00855 \text{ mho}$$

So,

$$A_v = g_m R_L = 0.00855(500) = 4.27$$

Some readers may find difficulty in visualizing R_{EB} as being taken (roughly) as 4 ohms, when standard textbooks describe this resistance as a "base spreading resistance" which can be anywhere between a few ohms and several hundred ohms. Let us clarify this point.

First of all, we know that if we look into the emitter, we will see a base-emitter impedance which has a value divided by beta and which appears in series with dynamic resistance r_e. Therefore the emitter current sees an impedance in the emitter-base junction which is the sum of r_e plus R_B/β. The latter term we have called R_{EB}.

So now assume we do have a "base spreading resistance" (R_B) of 200 ohms. Then if beta is 50:

$$R_{EB} = \frac{200}{50} = 4 \text{ ohms}$$

Conversely, if we look into the base of the transistor, we will see a base-emitter impedance which has a value multiplied by beta and which appears in series with r_e. Therefore the base current encounters an impedance in the base-emitter junction which is the product of beta and the sum of r_e plus R_{EB}. Remember, of course, that if an external emitter resistance (R_E) is used, this also becomes part of the product.

NOTE: There are no exercises at the end of this chapter. They have been deferred to the conclusion of Chapter 4 so that the contents of Chapters 3 and 4 can be tied together closely by these exercises.

CHAPTER 4

Basic Transistor Parameters and Stabilization of Parameters

In practical analysis of transistor circuits (as in basic desgin), we need to be able to visualize rapidly the approximate operating parameters:

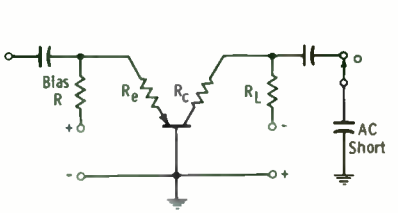
1. Current gain.
2. Voltage gain.
3. Power gain.
4. Power dissipated within the transistor.
5. Input impedance.
6. Output impedance.
7. Signal polarity.

4-1. CURRENT GAIN

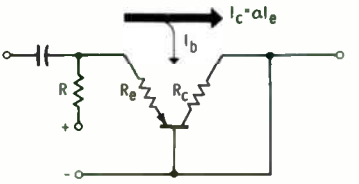
Current gain is simply the ratio of output current to input current (I_{out}/I_{in}). Current gain may be given in data sheets as either dc or ac (signal) specifications. In either case, the value given is with the output circuit short-circuited, and is termed the short-circuit forward current transfer ratio.

Fig. 4-1A shows a common-base (emitter-input) circuit with the internal resistance parameters included. Resistance R_e is relatively small compared to R_c, which is in the order of a megohm or more. A short circuit to signals is simulated by a capacitor across the output. Fig. 4-1B shows the equivalent circuit for the value of alpha (α) when the output is a short circuit.

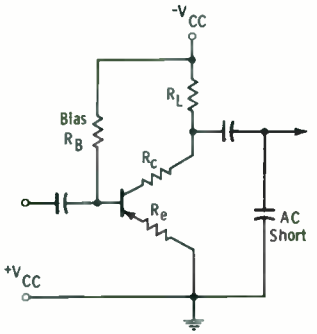
NOTE: Many data sheets represent α by h_{fb}; the subscript f denotes forward current transfer ratio, and the b means "common base."



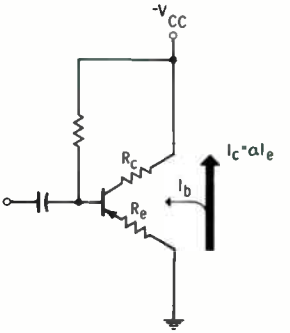
(*A*) *Common-base circuit.*



(*B*) *Equivalent circuit for alpha.*



(*C*) *Common-emitter circuit.*



(*D*) *Equivalent circuit for beta.*

Fig. 4-1. Forward current transfer ratios.

If "current amplification" is represented by the symbol A_i, for the common-base circuit:

$$A_i = \frac{I_c}{I_e} = \frac{\alpha I_e}{I_e} = \alpha$$

Note carefully that the collector current is equal to alpha times the emitter current, and that the current gain is the output current (I_c) divided by the input current (I_e). Therefore, for the common-base circuit, current gain is simply α, as the equation above shows.

Now study Figs. 4-1C and 4-1D for the common-emitter circuit (base input). The current gain is still I_{out}/I_{in}, in this case I_c/I_b. Also, the collector current is still αI_e. But I_b is:

$$I_b = I_e - I_c$$

Since the collector current is α times the emitter current, the collector current can be represented by αI_e. Then the above equation can be rewritten as:

$$I_b = (1 - \alpha) I_e$$

The current gain (designated beta, β, for the common-emitter circuit) is:

$$A_i = I_{out}/I_{in} = I_c/I_b$$

We have said that we can call the collector current αI_e and the base current $(1-\alpha)\ I_e$. Then:

$$\beta = \frac{I_c}{I_b} = \frac{\alpha I_e}{(1-\alpha) I_e} = \frac{\alpha}{1-\alpha}$$

This equation expresses β in terms of α; therefore, if specification sheets give only α, β can be found with this relationship. Also, if we know β, we can find α from the relationship:

$$\alpha = \frac{\beta}{1+\beta}$$

NOTE: Some specification sheets designate β as h_{fe}; the subscript f denotes *f*orward current gain, and the e means "common *e*mitter."

Remember the following symbols:

$\alpha = h_{fb}$ = common-base small-signal short-circuit forward current transfer ratio.

$\beta = h_{fe}$ = common-emitter small-signal short-circuit forward current transfer ratio.

h_{fc} = common-collector small-signal short-circuit forward current transfer ratio.

These "h" symbols are becoming standard. It is important to know they are equivalent to α and β (common base and common emitter, respectively). We will use such terminology interchangeably in this book so that the reader will become accustomed to it. The "h" symbol derives from "hybrid" equivalent circuits, which we will not use in this book.

Observe that in the equivalent circuits of Figs. 4-1B and 4-1D R_L is replaced by a short circuit. Also, R_c is very high in value. Note the similarity to a "constant-current" source. Actually, the value of R_L has very little effect on the current gain, provided that R_L is small relative to R_c. When we attach to this output circuit another transistor the effective value of R_L is lowered by the input impedance of this following stage. Immediately, it is evident that, in most circuits, current gain is affected much less than voltage gain, which does depend on the effective load resistance.

To review what has been covered thus far, current gain (α) of a common-base circuit is always less than 1. The value of α lies between 0.95 and 0.995 in practical transistors. The collector current of a common-emitter circuit is approximately β times the base current, I_b. It is pertinent now to see how a very small difference in α can result in a very large difference in the current gain (β) of a common-emitter circuit. For example, assume $\alpha = 0.98$.

Then:

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = \frac{0.98}{0.02} = 49$$

Now assume $\alpha = 0.99$. Then:

$$\beta = \frac{0.99}{0.01} = 99$$

Finally, assume $\alpha = 0.995$. Then:

$$\beta = \frac{0.995}{0.005} = 199$$

What importance should be attached to the above? It is this: The current gain for the common-base circuit would vary only 0.015 over the above range, but the current gain of the common-emitter circuit would vary over a range of 150. $(199 - 49 = 150.)$

4-2. THE POWER PARAMETERS

Now we will examine the transistor power parameters and review what we already know about the other operating parameters by using a simple, practical example.

Fig. 4-2 shows a common-base amplifier circuit. The dc resistance of the emitter-base junction is negligible compared to the 6k bias resistor (Fig. 4-2B), so the dc emitter bias current is 0.5 mA. Now for a quick analysis, ignore the small base current and assume the same 0.5 mA is present in collector load R_L. The quiescent collector operating point (no-signal dc voltage) is about 5 volts (Fig. 4-2C).

NOTE: It is important to point out here that this type of bias is evidence of class-A amplifier linear operation; the collector voltage at the no-signal operating point is in the vicinity of ½ V_{CC} for linear operation.

The power being dissipated at the collector is the operating collector voltage times the operating current:

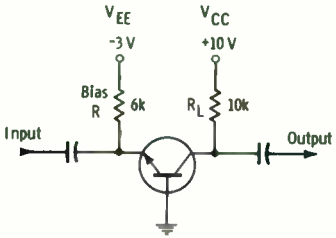
$$P_C = (0.0005)(5) = 2.5 \text{ milliwatts (mW)}$$

The input resistance (Z_{in}) is:

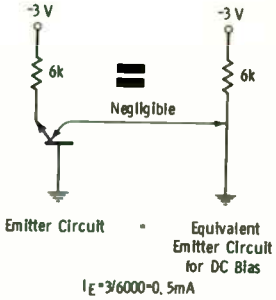
$$Z_{in} = \frac{26}{I_E} + R_{EB} = 52 + 4 = 56 \text{ ohms} = r_{tr}$$

The approximate voltage gain (A_v) for any small signal is the ratio of the output impedance (R_L) to the input impedance (r_{tr}):

$$A_v = \frac{10{,}000}{56} = 178 \text{ (approx)}$$

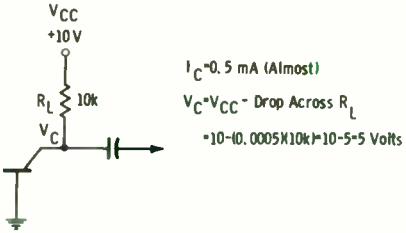


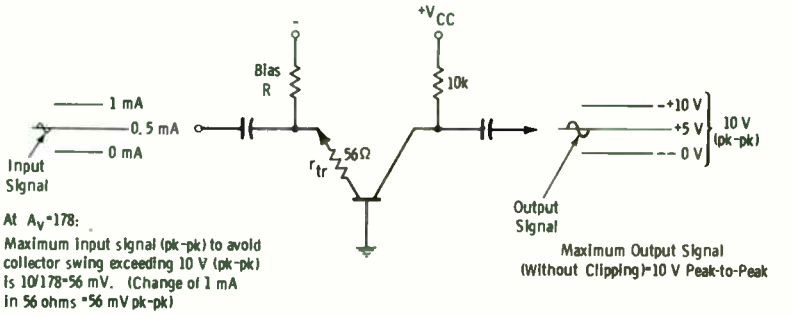
(A) *Amplifier circuit diagram.*



(B) *Bias current for emitter.*

(C) *No-signal collector voltage.*





(D) *Input and output signals.*

Fig. 4-2. Common-base amplifier circuit.

and the power gain (G_p) is the square of the current gain times the impedance ratio. We already know the impedance ratio is 178, and we assumed unity alpha. So in this case:

$$G_p = (1)^2(178) = 178 \text{ (same as voltage gain)}$$

If the transistor actually has an α of 0.98, then:

$$G_p = \alpha^2 \times 178 = (0.98)^2(178) = (0.96)(178) = 171$$

If we wanted to be more exact in voltage-gain analysis (considering alpha as 0.98):

$$A_v = \alpha \times 178 = (0.98)(178) = 174$$

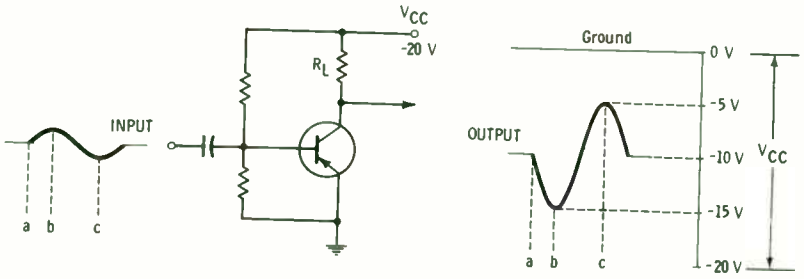
See Fig. 4-2D and let us examine what constitutes "small-signal" or "large-signal" operation. We computed the quiescent (no-signal) collector voltage to be 5 volts. Since the collector supply voltage (V_{CC}) is 10 volts, for linear operation the input signal voltage can be no greater than the amplitude that would cause a change of 5 volts at the collector. The transistor is an npn type, so as the signal current swings positive (counteracting the bias), collector current decreases, causing less voltage drop across R_L; hence the collector signal swings in the positive direction also. If the collector reaches 10 volts and the input signal swings further positive, no change can occur in the collector voltage since it is now at the maximum, V_{CC}. Clipping would occur. A peak-to-peak swing of more than 56 millivolts at the input would cause clipping of the output signal. Actually this would not be a "small-signal" mode of operation. In practice, in the interest of obtaining maximum linearity, the input signal swings the collector signal only about 0.1 or less of the available collector signal range. This is a "small-signal" operating mode. If, in the example of Fig. 4-2D, the input signal approached the level of the operating dc input current (0.5 mA), we would have a "large-signal" mode of operation.

4-3. SIGNAL POLARITY

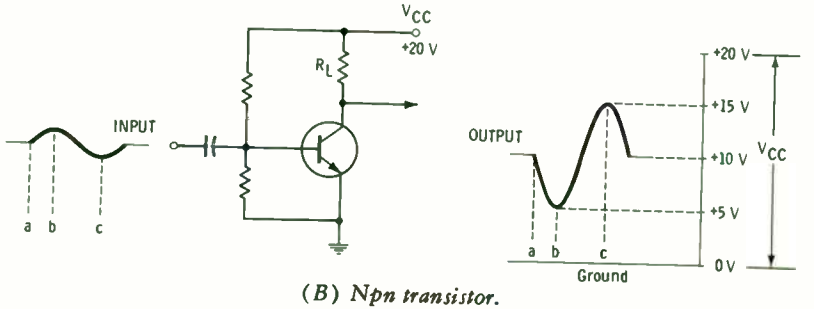
Since we have already encountered the need for examining signal polarity in the preceding example, let us clarify this point now.

We have already observed that the common-base circuit preserves signal polarity; the output signal is of the same polarity as the input signal. Also, in the small-signal mode of operation, signal currents (and voltages) never approach either cutoff or saturation of the transistor.

Now see Fig. 4-3A for the common-emitter (base-input) circuit. Since the circuit contains a pnp transistor, the collector has a negative voltage. Assume that the base current (bias) is such as to cause a quiescent (no-signal) collector voltage of −10 volts. This is point a of the input and output waveforms. As the input signal swings positive between points a and b, forward base-emitter current is decreased, causing less collector current and less voltage drop across R_L. As a result, the collector goes toward the −20-volt supply voltage, and the output waveform swings in inverse polarity to (out of phase with) the input signal. When the input signal swings in the negative direction between points b and c, forward base-emitter current increases, causing increased collector current. This increased collector current causes a greater voltage drop across R_L, and the collector goes toward ground potential. Naturally, if the signal on the n-type base becomes negative enough to saturate the transistor, the entire 20 volts would be dropped across R_L, and the collector would be driven to ground potential.



(A) Pnp transistor.



(B) Npn transistor.

Fig. 4-3. Signal phase relationships in common-emitter amplifier.

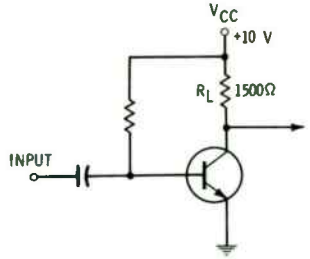
Now we should be able to understand the operation of the npn common-emitter circuit shown in Fig. 4-3B. As the input signal swings positive between points a and b of the waveform, the forward current through the base-emitter junction increases, causing more collector current and greater voltage drop across R_L. Hence the collector voltage drops from +10 volts (the quiescent operating point) to +5 volts (in this example). Thus we see that a signal-polarity inversion occurs in any common-emitter circuit, regardless of the type of transistor used.

It is evident that, since greater base current results in greater emitter current (and vice-versa), the *emitter-follower* circuit preserves signal polarity (no phase inversion). The emitter follower will be treated later.

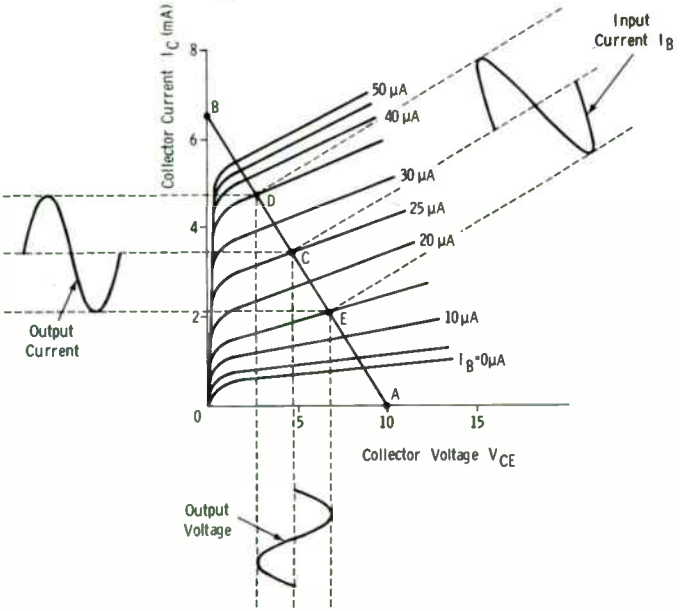
4-4. GRAPHICAL ANALYSIS

Characteristic curves showing collector current as a function of base current for various types of transistors are published by the manufacturers. A keen insight into transistor use can be gained by employing such curves for analysis.

Refer to the circuit of Fig. 4-4A. The collector supply voltage is 10 volts, and the load resistor, R_L, has a value of 1500 ohms. The peak-to-



(A) Common-emitter amplifier.



(B) Load line on characteristics..

Fig. 4-4. Graphical analysis of class-A transistor amplifier.

peak input signal is 20 microamperes (μA). The project is to construct the load line on the static characteristic curves of Fig. 4-4B.

This is done in exactly the same way as for an electron tube:

1. When the collector current is zero, collector voltage V_{CE} equals the collector supply voltage (V_{CC}), which is 10 volts. Point A on the horizontal axis is this zero-current point of the load line.
2. When the transistor is saturated (collector voltage reduced to zero, or ground), the total 10 volts of V_{CC} is dropped across R_L, so I_C is now:

$$I_C = \frac{10}{1500} = 0.0066 \text{ A} = 6.6 \text{ mA},$$

and point B on the vertical axis (6.6mA) is the second point of the load line.

3. When we connect points A and B with a straight line, we have established the load line for an R_L of 1500 ohms and a V_{CC} of 10 volts.
4. Since the input signal is 20 μA peak-to-peak, the deviation will be 10 μA above and below the operating point. As can be observed, the most linear operating point for this signal excursion is where the 25-μA base-current curve intersects the load line, point C on the diagram. Point D is 10 μA above the operating point, and point E is 10 μA below. (This operation actually exceeds the limits for the "small-signal" mode.) Note again that at the quiescent operating point the collector voltage is about ½ V_{CC}.
5. We establish the waveform for the output current by extending a horizontal line through the vertical axis from the operating point (quiescent, or no-signal, point C) and each of the deviation limits, points D and E.
6. We establish the waveform for the output voltage by extending a vertical line through the horizontal axis from operating point C and each of the deviation limits, points D and E. (The vertical line through point C intersects the horizontal axis at the quiescent value of collector voltage.)

Now what are the current gain, voltage gain and power gain of this particular amplifier?

For the current gain:

$$A_i = \frac{\Delta I_C}{\Delta I_B} = \frac{I_{Cmax} - I_{Cmin}}{I_{Bmax} - I_{Bmin}}$$

Substituting known values from the load-line diagram:

$$A_i = \frac{4.7\text{mA} - 2.1\text{mA}}{35\mu\text{A} - 15\mu\text{A}} = \frac{2.6\text{mA}}{20\mu\text{A}} = \frac{2.6\text{mA}}{0.02\text{mA}} = 130$$

So the current gain is 130 times, or $\beta = h_{fe} = 130$ for $R_L = 1500$ ohms.

For the voltage gain:

$$A_v = \frac{\Delta V_{CE}}{\Delta V_{BE}}$$

This equation says that the voltage amplification is the change in collector-to-emitter voltage divided by the change in base-to-emitter voltage (output voltage divided by input voltage). But so far we only know the input current, not the input voltage. The change in input voltage is simply the change in input current times the input impedance.

Since the input signal is to the base, $Z_{in} = h_{fe} \times r_{tr}$. We already know that:

$$r_{tr} = r_e + R_{EB} = \frac{26}{I_E} + R_{EB}$$

We can assume 4 ohms as the median value for R_{EB}, and for rapid (and approximate) calculation, we can take the value of I_E to be the same as the quiescent operating value of I_C (at point C on the load line), or 3.4 mA. Therefore:

$$r_{tr} = \frac{26}{3.4} + 4 = 7.6 + 4 = 11.6 \text{ ohms (round off to 11 ohms)}$$

$$Z_{in} = h_{fe} \times r_{tr} = 130 \times 11 = 1430 \text{ ohms (approx)}$$

Then the input voltage is:

$$V_{in} = I_{in} \times Z_{in} = 20\ \mu A \times 1430 \text{ ohms}$$
$$= 0.00002 \times 1430 = 0.029 \text{ V} = 29 \text{ mV}$$

The voltage gain is:

$$A_v = \frac{6.7 - 2.7}{0.029} = \frac{4}{0.029} = 140 \text{ (approx)}$$

The voltage gain also may be calculated by using g_m:

$$g_m = \frac{1}{r_{tr}} = \frac{1}{11} = 0.09 \text{ mho}$$

$$A_v = g_m R_L = 0.09 \times 1500 = 135 \text{ (close to above answer)}$$

The voltage gain in terms of the resistance ratio is:

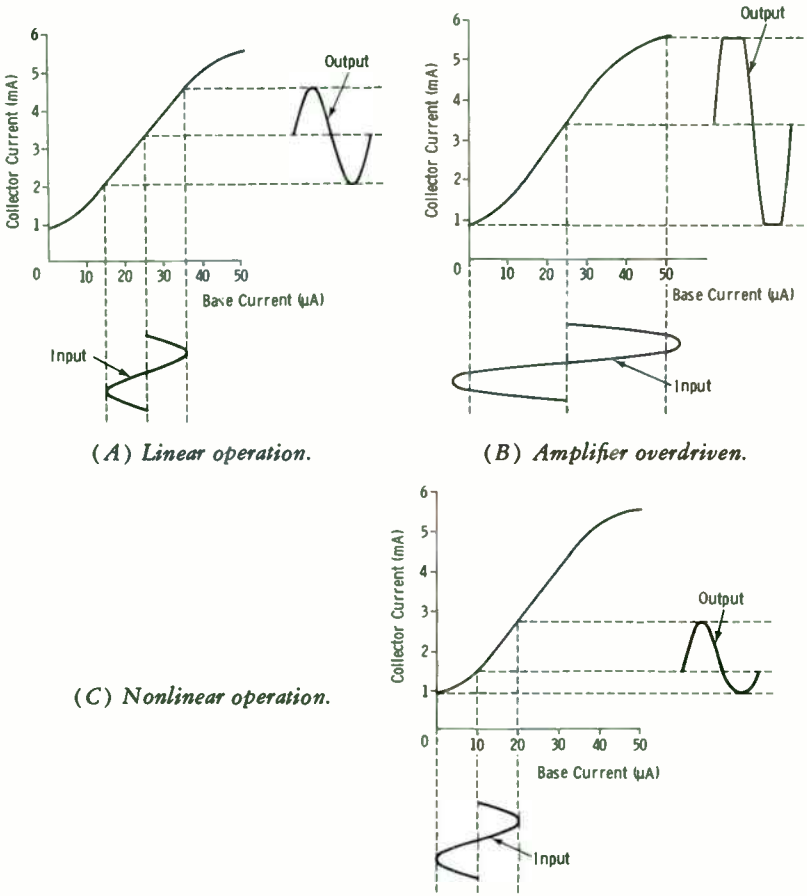
$$A_v = \frac{R_L}{r_{tr}} = \frac{1500}{11} = 136 \text{ (also close to above answer)}$$

The power gain is found by multiplying current gain times voltage gain:

$$G_p = A_v A_i = 140 \times 130 = 18{,}200$$

A published graph of charactertistic curves such as that of Fig. 4-4B can be used to derive a dynamic transfer curve showing collector current as a function of base current. Such curves are also sometimes published by the manufacturer, and are typified by the examples of Fig. 4-5. Fig. 4-5A represents the "normal" linear operation, which in this example

actually exceeds the range we will normally find in practice. (Signal level is usually only about 0.1 or less of the available signal range in well designed linear circuits.) In Fig. 4-5B we see the "clipping" that results from too large a signal input (overdriving), and in Fig. 4-5C we see the result of using the wrong quiescent operating point for a given amplitude of input signal.



(*A*) *Linear operation.*

(*B*) *Amplifier overdriven.*

(*C*) *Nonlinear operation.*

Fig. 4-5. Dynamic transfer characteristics.

Now observe Fig. 4-6. Each transistor has a maximum rated collector power it can safely dissipate without damage. To insure operation below this maximum rating, a *constant-power-dissipation* line can be drawn on any static characteristic curve, as shown in Fig. 4-6. We can then select a collector load resistor such that its load line falls within the area bounded by the horizontal and vertical axes and the constant-power-dissipation line.

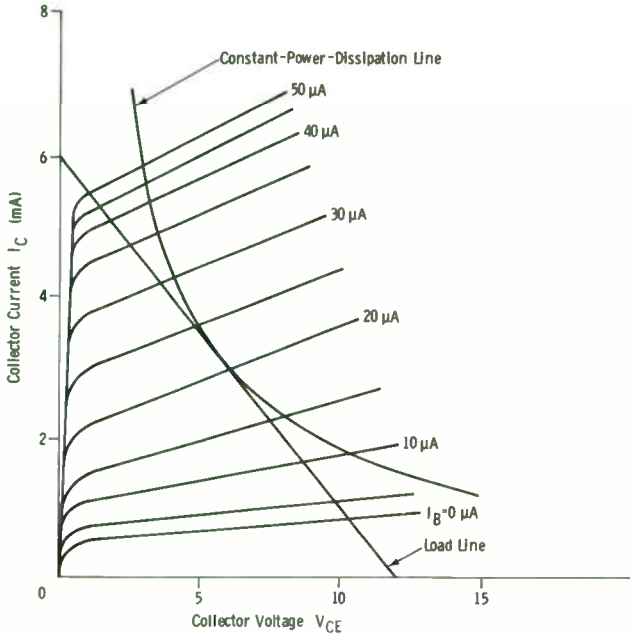


Fig. 4-6. Constant-power-dissipation line on static curves.

The constant-power-dissipation line is actually a plot of a number of points for which the product of collector voltage and collector current is equal to the maximum collector power rating of the particular transistor. The curve is quite simple to plot; all we need is the maximum collector power rating (from specification sheets) and the set of output static characteristic curves (always available from the manufacturer, and usually included in any transistor data book published by the manufacturer).

Assume a rating of 18 mW and a set of curves as shown in Fig. 4-6. We know that power equals volts times amperes:

$$P = IV$$

and by rearranging:

$$I = \frac{P}{V}$$

Now we simply substitute 18 mW (0.018 watt) for P in the formula, and arbitrarily select various values of voltage to obtain corresponding values of current. For example, if we start with 15 volts:

$$I = \frac{0.018}{15} = 0.0012A = 1.2mA$$

We simply continue this procedure until a sufficient number of points are obtained to get the curve. For example:

Volts	*Current*
15	1.2
12	1.5
9	2.0
6	3.0
4	4.5
3	6.0
2	9.0

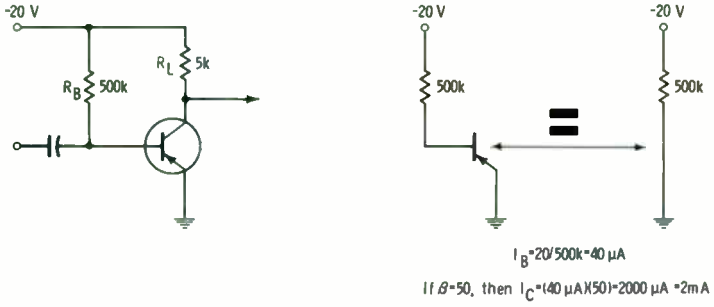
These points, when plotted and connected on the characteristic curves, represent the constant-power-dissipation line. Any load line tangent to this line will insure maximum permissible power gain of the transistor while operation remains within the maximum collector power-dissipation rating. Again note that this operation is not typical of small-signal-mode operation. It is important in the use of power amplifiers. We are trying here to bring the idea of transistor action into focus so that students do not get the impression from the start that small-signal operation and large-signal operation are unrelated. Such is not the case. The difference is simply in *degree* of *use* of the initial rating of a particular transistor.

4-5. WHY STABILIZATION?

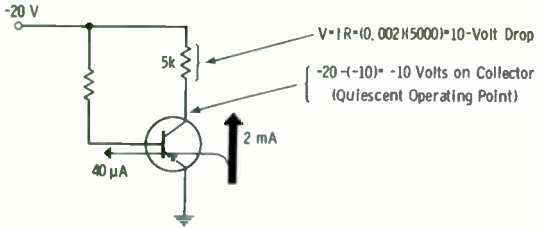
When a transistor is given a rating by the manufacturer, the rating is based on a "design-center" point. For example, the forward current gain of a particular transistor for common-emitter parameters may be listed as 60 for a "nominal" value, but with a minimum of 20 and a maximum of 120. This is the most valid reason for instruction in the use of "rules of thumb" for quick circuit analysis; when we use these rules on the "design-center" specifications, the accuracy of the results will be much better than the manufacturing tolerances themselves. It is also the reason why stabilization circuitry is mandatory.

Take the simple circuit of Fig. 4-7A. Fig. 4-7B shows how we find the base current (bias current) to be 40 μA. Then if an h_{fe} of 50 is specified, the collector current will be 2 mA. So the no-signal operating point is with a collector voltage of -10 volts (Fig. 4-7C). Now go on to Fig. 4-7D. If β happens to be 100 instead of 50 (entirely possible), the transistor would be in saturation without a signal applied. It is fully conducting, with the collector reduced to ground potential.

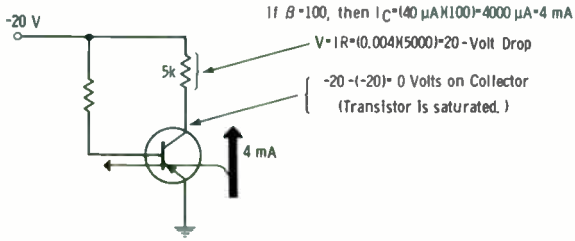
Remember also that the resistance of the pn junction is influenced by temperature. The temperature of the junction depends on operating current and ambient temperature. So the α, β, etc. must be controlled to compensate not only for manufacturing tolerances but for temperature change as well.



(A) Circuit diagram. *(B) Base bias current.*



(C) Collector voltage.



(D) Larger beta value.

Fig. 4-7. Illustration of need for stabilization of transistor parameters.

Here is the most effective way to look at the stabilization problem: Assume we have the transistor mentioned above with a manufacturing tolerance of 20 to 120 in forward current gain. From an ideal standpoint, if we control forward current gain to be always less than 20, then we can replace this transistor with another of the same type without trouble from manufacturing tolerances. If, at the same time, we compensate the negative temperature coefficient (Chapter 2) of the pn junction over the anticipated junction operating temperature range, we have a completely stabilized circuit. This is pretty much what the circuit designers have done in the equipment we must understand and maintain. In most cases

it is not necessary to go all the way to the "ideal" mentioned, but an approach to that point is made.

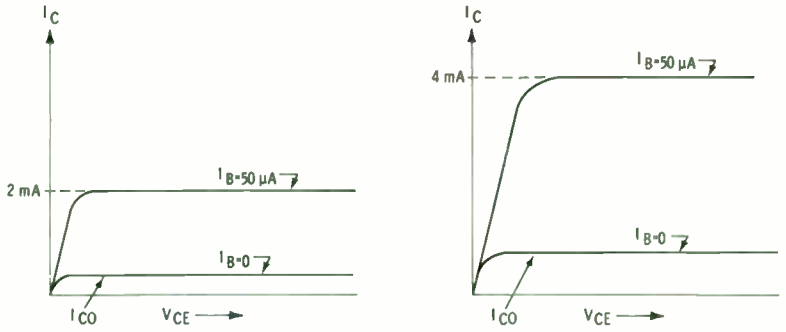
Remember also that a slight difference in α (common-base forward current gain) results in a very large difference in β (common-emitter forward current gain). So we realize the common-base circuit is very stable in comparison to the common-emitter circuit. For this reason, we will concentrate on the stabilization circuitry involved with the common-emitter configuration.

First of all, remember that the reverse-biased collector junction still has a very small current between collector and base. In a good transistor, this current is negligible at room temperature (25°C). But at higher temperatures, the junction resistance decreases, and this "reverse current" increases. Actually, the useful output signal is added to this current, so the actual collector current (I_c) is the total of the quiescent operating current, the signal current, and the reverse current (which is actually in the same direction as the output current). The reverse current between collector and base with the emitter circuit opened is termed "leakage current." For some transistors of the germanium type, the leakage current can double for every 10°C rise in junction temperature.

Leakage current is given the symbol I_{CBO}, which designates collector-base current with emitter open; it may also be abbreviated I_{CO}. Now we are going to add this symbol to the total collector current, which we previously said was equal to alpha times the emitter current:

$$I_C = \alpha I_E + I_{CO}$$

The presence of leakage current is illustrated in Fig. 4-8. Fig. 4-8A represents the condition in which a low value of I_{CO} prevails, and the collector current (I_C) is 2 mA when the base current reaches 50 μA. We could have the same transistor and circuit under high ambient-temperature conditions with a resulting increase in I_{CO}, and I_C could rise to 4 mA (for example) at the same base current of 50 μA (Fig. 4-8B). As the junction



(*A*) *Small leakage.* (*B*) *Higher leakage.*

Fig. 4-8. Effect of leakage current on collector current.

temperature increases, the collector resistance decreases, and the leakage current increases; this action produces further heating with accumulative effect. If the external base lead is opened, the leakage current is amplified by β. With a normal leakage current of (say) 10 μA and with $\beta = 50$, the resulting collector current is $50 \times 10 = 500$ μA. Note carefully the significance of this characteristic: The collector current is beta times the base current (forward current gain in the common-emitter circuit), and this includes any leakage current that is present.

The base current for a given emitter current is:

$$I_B = \frac{I_E}{h_{FE}} - I_{CO}$$

If we study this equation, we can see that an increase in either h_{FE} or I_{CO} means that *less* base current is needed to cause a given amount of emitter current. To state this relationship another way, if I_E tends to change because of variations in h_{FE} and/or I_{CO}, the base current must be changed in order to counteract the change in emitter current.

If the base current (I_B) can be made to depend on I_E and I_{CO}, current gain (hence voltage gain) can be stabilized. Refer to Fig. 4-9. The base current is influenced by the current in R_E. If R_E is large compared to r_{tr}, then gain depends more on circuit constants than on transistor gain characteristics.

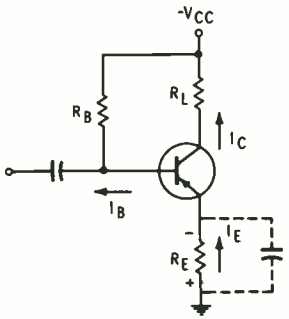
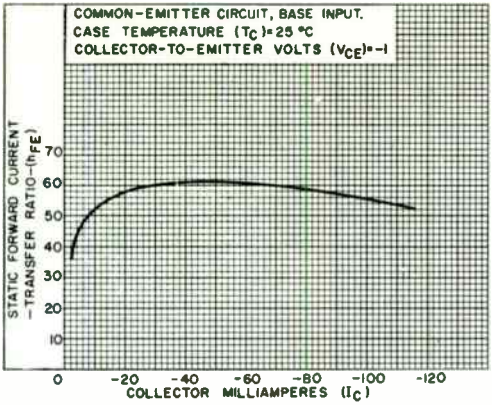


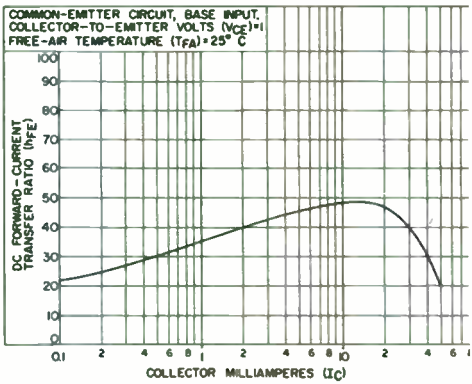
Fig. 4-9. Stabilization with resistor in emitter circuit.

The stabilizing effect of R_E can be explained as follows: Current through R_E causes a voltage drop with the polarity shown in the figure. If the emitter current increases, the voltage drop across R_E increases also, making the emitter more negative. As the emitter becomes more negative, the base-emitter voltage, and therefore the base current, is reduced. The reduction in base current tends to oppose the original increase in collector current. If R_E is bypassed to the signal (as shown by the dash lines), degeneration of the signal does not occur, but the dc operating point is stabilized.

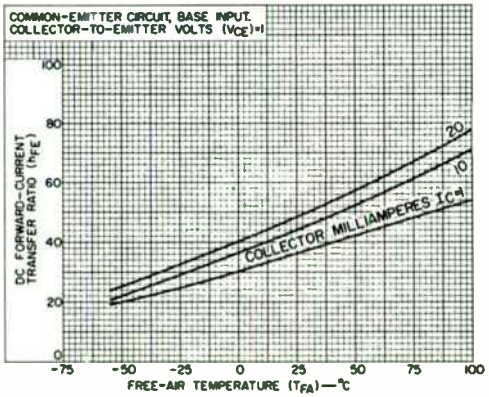
In a common-emitter circuit, beta increases not only from temperature increase, but also as collector current increases. There is a limit to this



(A) Type 2N406 (typical).



(B) Type 2N708 (typical).



(C) Type 2N708, including temperature effects (typical).

Courtesy RCA Corp.

Fig. 4-10. Effects of collector current on beta.

effect, as shown by the graphs of Fig. 4-10. Beta for the 2N406 (Fig. 4-10A) reaches a maximum between 40 and 60 mA of collector current, then gradually falls off. (NOTE: This curve is "typical." Actually, the 2N406 can vary in h_{FE} from 40 to 100 at $I_C = 50$ mA.) Also note that at very small collector currents, much smaller values of beta prevail. The slope of the curve is quite steep in the lower regions of I_C; this is typical of most transistors. To see how these curves vary with different types of transistors, see Fig. 4-10B for the 2N708. Remember, these are all "typical" values, not absolute. Fig. 4-10C extends the data to include both I_C and temperature.

We will go further into the analysis of stabilization (including more complete stabilization of I_{CO}) in the next chapter. This coverage will include the most common forms of negative feedback used in modern circuitry.

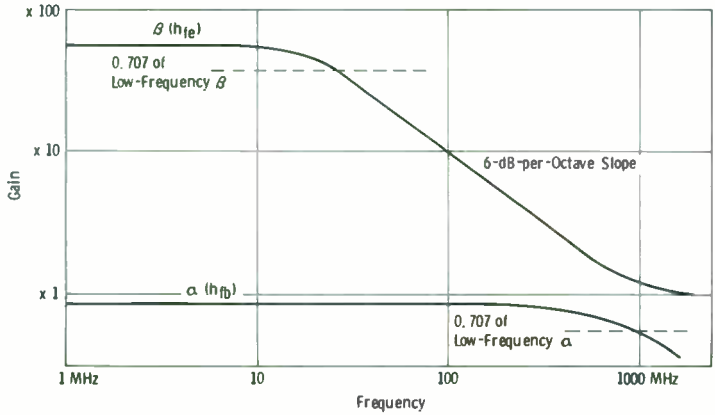


Fig. 4-11. Effects of frequency on alpha and beta for one transistor.

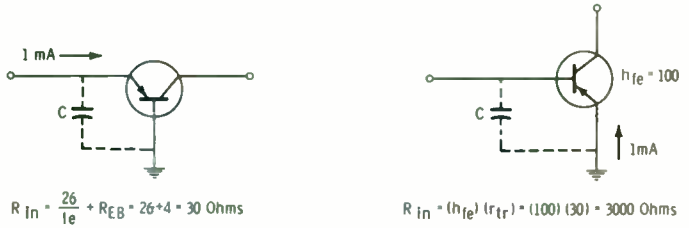
4-6. EFFECT OF FREQUENCY ON ALPHA AND BETA

Alpha (or h_{fb}) and beta (or h_{fe}) are specified at some low frequency (normally 1 kHz) or, in the case of power transistors primarily for power-supply service, in dc values (h_{FB} and h_{FE}). But as the frequency of operation is increased, the forward current gain decreases. This effect is in common with electron-tube circuitry, and occurs for the same reason: input, output, interelement, and circuit capacitance.

The "cutoff frequency" of a transistor is that frequency at which the value of alpha or beta drops to 0.707 (3 dB) of its one-kilohertz value. Fig. 4-11 shows typical curves of alpha and beta (h_{fb} and h_{fe}) as functions of frequency for a high-frequency transistor.

Note that in any such curves the forward current gain of the *common-emitter* circuit (h_{fe}) falls 3 dB from its low-frequency value at a much

lower frequency than h_{fb} does. Why? See Fig. 4-12. Fig. 4-12A shows the common-base circuit with the total input capacitance indicated by dash lines. The input resistance of the common-base circuit is relatively low; in this case ($I_E = 1$ mA), it is 30 ohms. Now study Fig. 4-12B for the same transistor in a common-emitter circuit. The input resistance in this case is 3000 ohms. The same value of capacitance now has a much greater shunting effect; effectively the input capacitance is magnified by the factor h_{fe}. The same kind of problem exists with respect to the plate-load value in a vacuum-tube circuit: The higher R_L is made (for more gain),



(A) Common-base circuit. *(B) Common-emitter circuit.*

Fig. 4-12. Capacitance shunting input resistance.

the greater is the loss of high-frequency response because of output capacitance across the plate load. In the next chapter, we will see how degeneration in a common-emitter circuit can be used to increase the bandwidth by greatly reducing the intrinsic transistor capacitance.

NOTE: The actual multiplication factor is $\beta + 1$, and we will find this value used in other transistor studies. We have dropped the "1" in these chapters, since practical circuit analysis normally does not call for such precise values.

So now we understand why the beta cutoff frequency in Fig. 4-11 is much lower than the alpha cutoff frequency. Here is the basic relationship:

$$f_{hfe} = \frac{f_{hfb}}{h_{fe}}$$

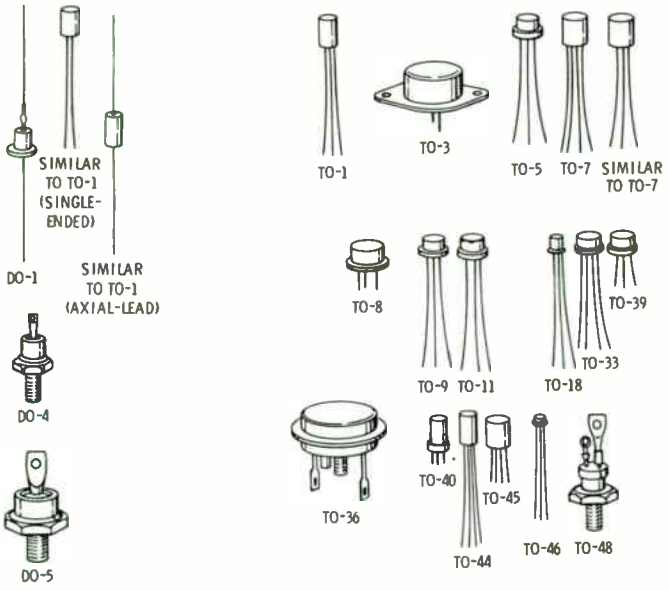
where,

f_{hfe} is the beta cutoff frequency, and
f_{hfb} is the alpha cutoff frequency (normally given in specification sheets).

This formula says that the beta cutoff frequency (point where response is 3-dB down from low-frequency value) is equal to the ratio of the alpha cutoff frequency to the h_{fe} of the transistor. It relates gain to frequency response (in the common-emitter circuit), just as in tube-type amplifiers.

The gain-bandwidth product (f_r) is that frequency at which h_{fe} goes to unity gain. Beyond the β cutoff frequency, β decreases at approximately

6 dB/octave. (If we double the frequency, we have increased the frequency by one octave. If β decreases 6 dB/octave, β is down 6 dB each time the frequency is doubled.) In this frequency range, f_r is the product of a given frequency and the measured h_{fe} at the given frequency. In the example of Fig. 4-11, unity gain (no amplification) occurs at approximately the frequency at which the common-base curve is down 3 dB (alpha cutoff).



(*A*) *Diodes.* (*B*) *Transistors.*

Courtesy RCA Corp.

Fig. 4-13. Examples of packaging of semiconductor devices.

Here is a rule of thumb we can use: The gain-bandwidth product (common-emitter circuit) is approximately equal to one-half alpha cutoff without peaking. It is approximately equal to alpha cutoff with double peaking. This approximation takes care of stray and circuit capacitance in practical amplifiers. Actually, we will find practically no wideband amplifiers (for example, in video service) that employ peaking circuits, since modern transistors designed for this type of service have an extremely high value of gain-bandwith. About the only place we will find compensation circuits (in video applications) is in such units as camera preamplifiers, where pickup-tube coupling circuits require frequency-phase correction. Obviously, amplifiers designed for processing signals (aperture boost, phase correction, etc.) are exceptions. (Some special high-frequency transistors will do better than the one-half alpha rating.)

Let us be sure of the practical application of the gain-bandwidth (GB) relationship. If we have a transistor with an alpha cutoff listed as 500 MHz and we use the rule of thumb just mentioned:

$$GB = 250 \text{ MHz (no peaking)}$$

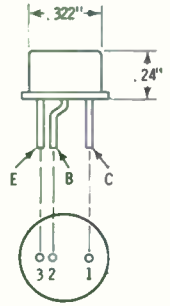
Then the gain for a bandwidth of 10 MHz is:

$$G = \frac{250\text{MHz}}{10\text{MHz}} = 25$$

This result indicates that the maximum gain we can expect for a bandwidth of 10 MHz is 25 times. The bandwidth we would obtain at a gain of 50 is:

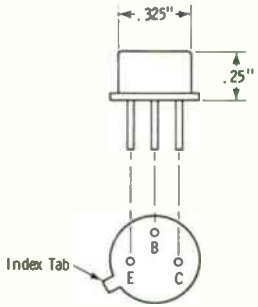
$$B = \frac{250}{50} = 5 \text{ MHz}$$

This result illustrates the familiar rule of thumb that we can halve the gain to double the bandwidth, or double the gain and halve the bandwidth.



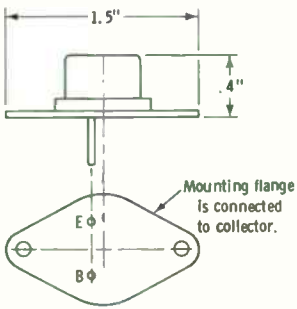
Courtesy RCA Corp.

(*A*) *In-line pattern.*



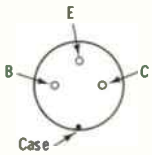
Courtesy RCA Corp.

(*B*) *Triangular pattern.*



Courtesy RCA Corp.

(*C*) *Power-transistor.*



(*D*) *High-frequency.*

Fig. 4-14. Basic transistor-lead arrangements.

4.7. TRANSISTOR PACKAGING

Fig. 4-13 identifies the types of packaging listed on specification sheets for transistors. In Fig. 4-13A are diode (DO) types; in Fig. 4-13B are transistor (TO) types.

Fig. 4-14 shows how to identify the three most common types of lead connections (bottom view). (NOTE: The side view dimensions are an example of a specific transistor only.) Fig. 4-14A shows the "in-line" configuration, Fig. 4-14B shows the "triangle," and Fig. 4-14C shows the power type. On the power type, note that the emitter (E) and base (B) are offset from the center line. Also with this type of transistor, the collector is tied to the case, and the case is insulated from the chassis.

Very important: See Fig. 4-14D, and note that the emitter and base leads are *interchanged* from their positions in Fig. 4-14B. This arrangement is used in a recent type of high-frequency transistor to allow better isolation between output (collector) and input (base). This lead positioning is not due to internal structure, but rather it allows more efficient use of external interterminal shields to reduce feedback caused by external capacitances, particularly as applied to printed circuit boards. This type of transistor normally has four leads, the fourth being connected to the case as shown.

EXERCISES (CHAPTERS THREE AND FOUR)

Q4-1. It has been stated that the common-emitter transistor circuit can be compared to the common-cathode tube circuit. What is the major operating difference?

Q4-2. Why do some manufacturers' specification sheets and graphs show collector and base current as having a negative value? For what type of transistor is this done?

Q4-3. If a transistor can be assumed to have an intrinsic (internal) collector resistance of 1 meghom and it has an h_{fe} of 100, what effect would a collector load (R_L) of 1000 ohms have on h_{fe}?

Q4-4. If a given transistor is listed as having an h_{fb} of 0.95, what is h_{fe}?

Q4-5. Figs. 4-1C and 4-1D show only one dc source instead of two battery sources of opposite polarity. How is this possible?

Q4-6. (A) What is the relationship of collector current to emitter current? (B) Does this relationship depend upon type of circuit hookup (common emitter, common base, or common collector)?

Q4-7. If a transistor has an alpha of 0.99 and an alpha cutoff rating of 100 MHz, and it is being used in a common-emitter circuit, what is the comparative h_{fe} at 100 MHz?

Q4-8. Is the input impedance of Fig. 4-9 greater or less than that of Fig. 4-7?

CHAPTER 5

Basic Linear-Circuit Analysis

This chapter will serve to tie in what has been learned thus far with methods for analyzing a circuit to determine readily what it should and should not do.

We are concerned primarily with two basic functions:

1. Small-signal amplification.
2. Large-signal and power amplification.

These functions are accomplished in three basic circuit configurations:

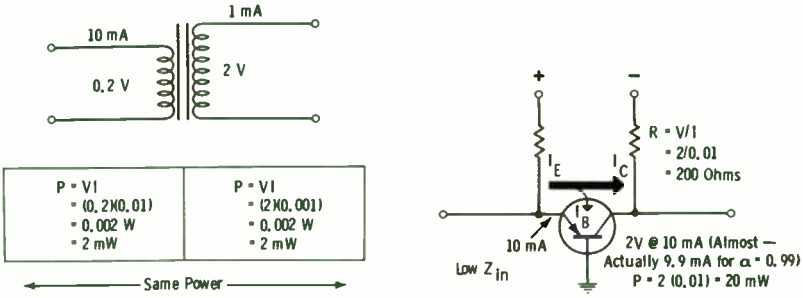
1. Common base (emitter input, collector output).
2. Common emitter (base input, collector output).
3. Common collector (base input, emitter output).

In transistor circuitry, the *common emitter* amplifier is most often used, just as the common-cathode amplifier is the most often used tube circuit. The *common-base* amplifier is used to *match a low-impedance circuit to a high-impedance circuit*. The *common-collector* amplifier is used to match a high-impedance circuit to a low-impedance circuit.

When we consider "matching," we must not think of a transistor in terms of a transformer; there is an essential difference. See Fig. 5-1A and remember from basic theory that a transformer can give voltage gain with reduced current, or current gain with reduced voltage; it *cannot* provide power gain. If we put a 0.2-volt signal at 10 milliamperes (2 milliwatts) into the low-impedance side of the transformer, we can get 2 volts (turns ratio 1:10) at 1 milliampere (2 milliwatts) from the high-impedance side. Conversely, we can put 2 volts at 1 milliampere into the high-impedance side of the transformer and get 0.2 volt at 10 milliamperes from the low-impedance side.

Now see Fig. 5-1B. The transistor can be given a collector load that will provide a 2-volt output for the 10-milliampere input. Since almost all of

the input current appears in the collector load, we can assume almost 10 milliamperes in the collector. The output power is then $2(0.01) = 0.02$ watt $= 20$ milliwatts. So the power input is amplified to about 20 milliwatts in the output. Both voltage *and* power gain have been obtained at a *slight* current loss.



(*A*) *Transformer.* (*B*) *Transistor.*

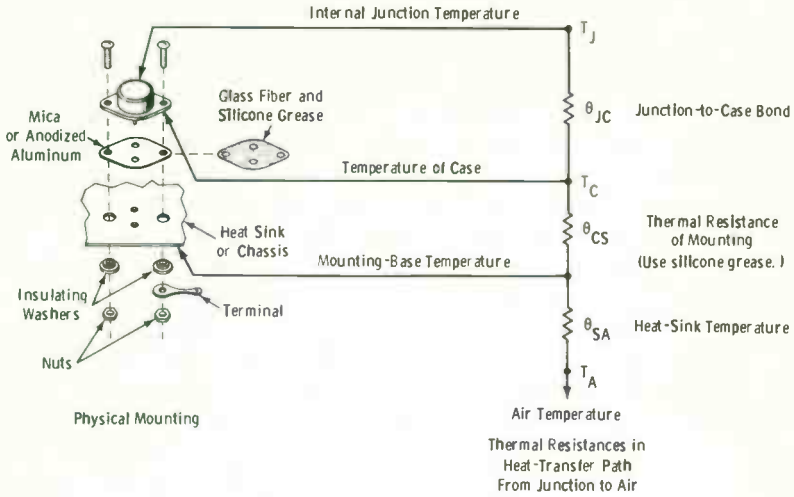
Fig. 5-1. Impedance matching.

We are going to cover the common-collector circuit later in this chapter. For that circuit, we will find we get slightly less than unity *voltage* gain, but that we still get current (and power) gain.

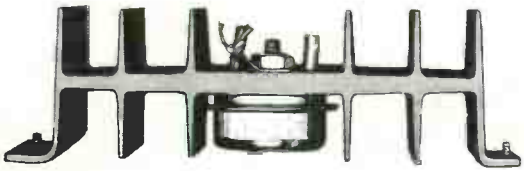
5-1. BIASING AND THERMAL STABILITY

First of all, let us consider the methods used to conduct heat away from the junctions as efficiently as possible. Fig. 5-2A illustrates the several "thermal resistances" in the heat-transfer path from junction to surrounding air. In addition to the ambient air temperature, the internal junction temperature (T_J) will depend on the collector current-voltage product (power dissipation). The junction-to-case bond (θ_{JC}) is not under our control; it is controlled by the manufacturing process. The thermal resistance of the mounting (θ_{CS}) is determined both by the size and type of heat sink used, and by how well we coat the mica or glass-fiber insulating wafer with heat-conducting silicone grease to fill surface irregularities. Fig. 5-2B shows one type of heat sink used for power transistors, and Fig. 5-2C illustrates a "slip-on" fin-type heat radiator used for smaller voltage amplifiers. The heat-sink temperature (θ_{SA}) is determined by exposure to (and temperature of) the ambient air; it is also influenced by the amount of heat radiation from surrounding components.

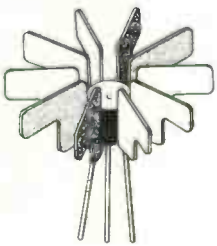
Please note that such precautions are simply a means of operating the transistor at as low a temperature as possible under possible ambient air temperatures that may exceed normal room temperatures. They do *not*



(A) Electrical analog of mounting.



(B) Power-transistor heat sink.



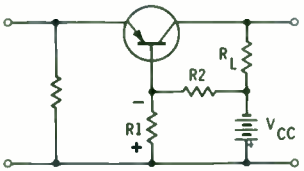
(C) Small-transistor heat sink.

Fig. 5-2. Transistor mounting.

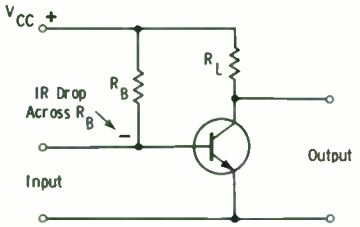
provide means of stabilizing operation under *varying* temperature conditions. Such stabilization is effected by circuit design.

Let us clarify how proper biasing is obtained with only one voltage source, as is the case in most linear amplifiers. Study Fig. 5-3A. Resistors R1 and R2 form a voltage divider to establish emitter-base bias. Remember that electron flow is through R2 and R1 back to the positive (common) terminal. The base is positive relative to the negative battery terminal but is negative relative to ground (or common), so the base is negative relative to the emitter, for proper forward bias. Current division must be such that the base is positive relative to the collector for proper reverse bias (this is a pnp transistor).

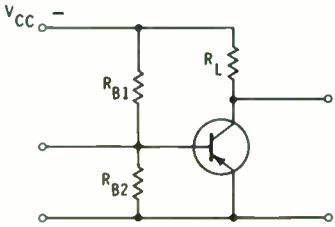
Fig. 5-3B shows how the same principle applies to the common-emitter circuit. Base current drawn through R_B goes toward ground (negative) and supplies the necessary forward bias for the emitter-base junction (npn transistor.) When R_B is used in this fashion to connect the base to the



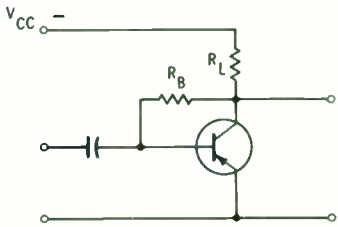
(*A*) *Common-base voltage divider.*



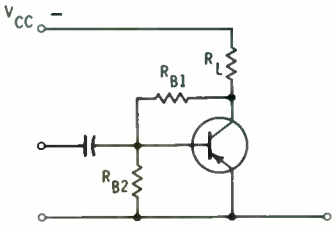
(*B*) *Resistor from supply to base.*



(*C*) *Common-emitter voltage divider.*



(*D*) *Resistor from collector to base.*



(*E*) *Voltage divider from collector.*

Fig. 5-3. Transistor-biasing arrangements.

"high side" of the collector supply, the bias is called "fixed bias" because it is independent of collector current. This is a poor arrangement for good circuit stability.

In Fig. 5-3C, resistor R_{B2} has been added to form a voltage divider for the base-emitter forward bias. Provided the current through R_{B1} and R_{B2} is fairly large, temperature induced changes in the base-emitter junction have reduced effect on the bias, and a little better temperature stability is obtained.

Fig. 5-3D shows R_B connected directly to the collector. This arrangement is termed "self-bias" because the base-emitter bias is now controlled by the collector current. As collector current increases (greater IR drop across R_L), the collector goes toward ground (plus) potential, and the base current is reduced, tending to stabilize the circuit. Therefore, R_B serves as a negative-feedback circuit to the signal, reducing the current gain. In Fig. 5-3E, the voltage-divider arrangement is added to increase the stability further as mentioned in connection with Fig. 5-3C.

The designer establishes the value of R_B by knowing the desired base current (I_B) from characteristic curves such as those in Fig. 4-4. Take for example Fig. 5-3B, and assume the following data:

$$V_{CC} = 6 \text{ volts}$$
$$\text{Desired } I_B = 30 \text{ microamperes}$$

Then by Ohm's law:

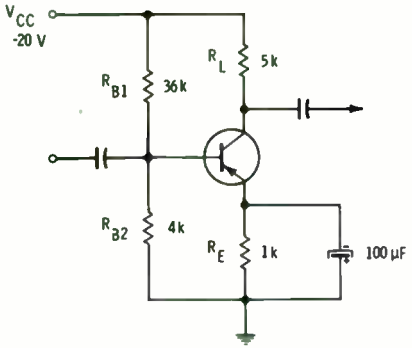
$$R_B = \frac{V_{CC}}{I_B} = \frac{6}{(30)(10^{-6})} = 200{,}000 \text{ ohms}$$

For the self-bias arrangement of Fig. 5-3D, the same procedure applies, except that the collector voltage (V_C) is used in place of the battery voltage (V_{CC}). Assume that a base current of 30 microamperes is desired, and that the quiescent collector voltage is 3 volts. Then:

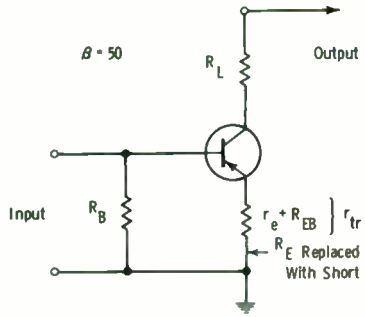
$$R_B = \frac{V_C}{I_B} = \frac{3}{(30)(10^{-6})} = 100{,}000 \text{ ohms}$$

Now let us take a typical circuit such as might be encountered in practice and see how far we can go in analysis. (*Caution*: In practice, we need to consider the preceding and following stages. For the moment, we will be concerned with a single stage only.) See Fig. 5-4A. Step one is to find what bias voltage exists at the base. For a practical analysis, we simply determine the voltage at the junction of R_{B1} and R_{B2} by Ohm's law:

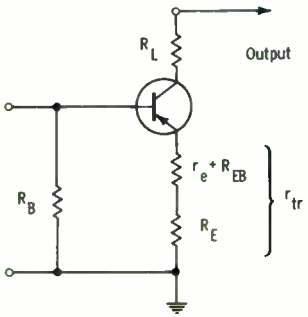
$$I = \frac{V}{R} = \frac{-20}{40{,}000} = -0.5 \text{ mA}$$



(*A*) *Determination of bias.*



(*B*) *Equivalent for signal.*



(*C*) *Equivalent without bypass.*

Fig. 5-4. Common-emitter amplifier circuit.

The ½ milliampere through the 4k resistor produces a voltage drop of:

$$V = IR = (-0.5 \text{ mA})(4000 \text{ ohms}) = -2 \text{ volts} = V_B$$

Note that for this assumption to be made, the base current must be considered negligible with respect to the current through the voltage divider. Said in a different way, the divider current must be relatively large compared to the base current. If this condition did not exist, the base current would upset the computations. Also, regulation (stabilization) would be poor, since the junction resistance depends on temperature, and the bias would therefore change with temperature in the wrong direction for stabilization. This is the reason why the voltage-divider current is always made large compared to the base current.

We have found that −2 volts exists at the base. Remember from basic theory that if we put a voltmeter directly between the base and emitter leads in this active circuit, we will have only about a 0.2-volt drop for a forward-biased germanium pn junction. Therefore, the voltage at the top of R_E (emitter terminal relative to ground) will also be very close to −2 volts (in actuality about −1.5 to −1.8 volts).

For a rapid and practical analysis, assume the emitter to be at −2 volts. Since R_E is 1000 ohms, the current (I_E) to cause this 2-volt drop is:

$$I_E = \frac{V}{R} = \frac{-2}{1000} = -2 \text{ mA}$$

To stay with our rapid analysis, assume α is unity instead of, for example, 0.98, and therefore the collector current (I_C) is also 2 milliamperes. Then the voltage across R_L is:

$$V_{RL} = IR_L = (-2 \text{ mA})(5000) = -10 \text{ volts}$$

With a 10-volt drop across R_L, the voltage at the collector (V_C) is:

$$V_{CC} - V_{RL} = -20 - (-10) = -10 \text{ volts}$$

What is the power dissipation at the collector? The voltage at the emitter is −2 volts and the voltage at the collector is −10 volts, so the collector-to-emitter voltage (V_{CE}) is −8 volts. Since the collector current is −2 mA:

$$P_C = VI = (-8)(-2) = 16 \text{ mW}$$

Now further assume that we have looked up the specifications of this particular transistor and found it to have a dc beta of 50. We can find the base current:

$$I_B = \frac{I_C}{h_{FE}} = \frac{-2 \text{ mA}}{50} = -40 \ \mu\text{A}$$

The base current of 40 microamperes is indeed small compared to the voltage-divider current of 500 microamperes (0.5 milliampere).

We have determined (approximately) the dc operating point of the circuit without using the published curves of I_C vs V_{CE} for specified values of I_B. We can go ahead with the *signal* analysis in the same way without using the published output-characteristic curves.

For signal analysis, redraw the circuit of Fig. 5-4A as in Fig. 5-4B. Resistor R_B is the equivalent of R_{B1} and R_{B2} in parallel; this is the way they appear to the input signal, since R_{B1} is in parallel with R_{B2} through the negligible power-supply impedance to ground. The emitter resistor (R_E) is replaced with a short because the signal is bypassed through the 100-μF capacitor.

In the small-signal mode of operation, with a dc bias current of 40 μA, we can safely assume the signal current superimposed on the dc base current will not exceed 10 μA (pk-pk). This signal would swing the base current between 45 μA and 35 μA. In fact, for many cases of small-signal operation, the signal amplitude is so small relative to the dc bias value that we could not work with published characteristic curves.

Let us go ahead with the analysis assuming an input signal of 10 μA. This input signal is divided between R_B and the transistor input impedance, which is determined by the transresistance (r_{tr}).

$$\text{Input } Z = (r_{tr})(h_{fe}')$$
$$= (26/2 + 4)(50) = (17)(50) = 850 \text{ ohms}$$
$$R_B = \frac{(36k)(4k)}{36k + 4k} = \frac{144k}{40k} = 3.6k$$

We have 3600 ohms (R_B) in parallel with the transistor input impedance of 850 ohms. Now how does the input signal divide? The 3600 ohms is something over four times the transistor input resistance, so R_B will draw something less than one-fourth of the 10-μA signal current. Let us say it draws 20 percent of the current, so about 2 μA is lost in R_B.

The 2-μA current in R_B leaves 8 μA of signal for the transistor. Now very rapidly: A current gain of 50 causes $8 \times 50 = 400$ μA of signal swing in R_L, so the signal-voltage swing is:

$$V_s = IR = (400 \ \mu A)(5000 \text{ ohms}) = 2 \text{ volts}$$

Now with an R_L of 5000 ohms, and since we know that h_{fe} is the *short-circuit* forward current gain, we would expect slightly *less* than 2 volts of signal swing. The rapid circuit analysis is quite valuable provided we keep the value of R_L in mind.

We can also see that the signal input voltage developed is:

$$V_{in} = (8 \ \mu A)(850 \text{ ohms}) = 6.8 \text{ mV}$$

The voltage gain is therefore:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{2}{0.0068} = 300 \text{ (approx)}$$

To double check by another method:

$$g_m = 1/r_{tr} = 1/17 = 0.06 \text{ mho}$$
$$A_v = (g_m)(R_L) = (0.06)(5000) = 300$$

Voltage amplification is also approximately the ratio of R_L to the transresistance:

$$A_v = \frac{5000}{17} = 294 \text{ (very close)}$$

One other point to bear in mind: The total input impedance, including the base-bias supply, is the parallel combination of R_B and the 850-ohm input impedance of the transistor. (The total input impedance, Z_{in}, is the impedance seen by the preceding stage):

$$Z_{in} = \frac{(850)(3600)}{850 + 3600} = 690 \text{ ohms}$$

The circuit of Fig. 5-4A is considered relatively stable. Was anything sacrificed to get this stability? Yes, primarily gain and (where important) input impedance. Why?

Consider deleting R_{B2} from the network. To get 40 μA of base current, R_{B1} would become:

$$R_B = \frac{20 \text{ volts}}{40\ \mu A} = 500{,}000 \text{ ohms}$$

This impedance would have a negligible effect in parallel with the 850-ohm input impedance of the transistor, and would therefore raise both the gain and the input impedance as seen by the preceding stage. (Therefore, there would be more gain in the preceding stage because its effective collector load would not be lowered as much.) But the sacrifice is necessary to obtain the stability required for practical use.

If the bypass capacitor around R_E is not used, we get the added stabilization of negative feedback (with reduced signal gain) from the signal current present in R_E. Redraw the circuit as in Fig. 5-4C.

Now the voltage amplification is:

$$A_v = \frac{R_L}{r_{tr}} = \frac{5000}{1017} = \text{less than } 5$$

The input impedance of the transistor is:

$$Z = (1017)(50) = 50{,}850 \text{ ohms}$$

An unbypassed emitter resistor is often this large in comparison to R_L. The computations above illustrate the sacrifice in gain for the added stability of emitter negative feedback, which also greatly increases the input impedance.

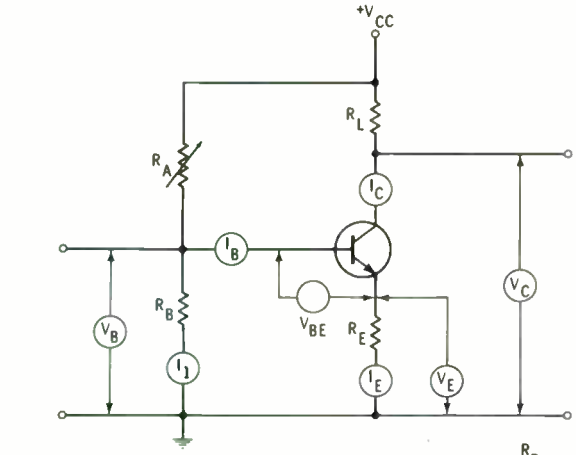
Here is a simple way to handle an *unbypassed* emitter resistor in estimating the effect on gain:

$$A_v = \frac{A}{g_m R_E}$$

where A is the voltage gain with the emitter resistor bypassed. In our example, A was 300. The transconductance (g_m) was 0.06 mho, so the new gain with R_E unbypassed is:

$$A_v = \frac{300}{(0.06)(1000)} = \frac{300}{60} = 5$$

So this is still another trick for rapid circuit analysis. With an unbypassed emitter resistor, we can compute the gain as though the resistor were bypassed, then get the effective gain from the above relationship.



(1) $R_L > 5R_E$
(2) $I_1 > 5I_B$
(3) R_A Adjusted for $V_C \approx 1/2\ V_{CC}$
(4) I_B Dependent Upon (3)
(5) $R_B = V_B/I_1 \approx$ 5 to 10 Times R_E
(6) $R_E = \dfrac{V_E \text{ Desired } (>5V_{BE})}{I_E \text{ Desired (From Signal Mode)}}$

(7) $V_B = V_E + V_{BE}$, or $\dfrac{R_B}{R_A + R_B}\ V_{CC}$
(8) $V_E > 5V_{BE}$
(9) $V_C \approx 1/2\ V_{CC}$
(10) $A_V \approx R_L / R_E$ (With R_E Unbypassed and $I_E > 1$ mA)

Fig. 5-5. Design parameters for common-emitter amplifier.

5-2. UNDERSTANDING EMITTER FEEDBACK

Emitter feedback is, very simply, the result of the unbypassed emitter resistor, R_E. Since the signal induced in useful collector load R_L must pass through R_E, the signal is degenerated. This type of feedback is a form known as "series feedback," and it increases the input impedance. Before we go further, it is important to examine in more detail this most common form of feedback stabilization.

First, let us review what we have learned about the common-emitter amplifier relationships, and put the information down for future reference. See Fig. 5-5, and record what we have covered thus far:

$$V_{BE} = 0.2 \text{ to } 0.3 \text{ V for germanium transistors} \qquad \text{(Eq. 5-1.)}$$

$$V_{BE} = 0.6 \text{ to } 0.7 \text{ V for silicon transistors} \qquad \text{(Eq. 5-2.)}$$

$$I_B = \frac{I_E}{h_{fe}} - I_{CO} \qquad \text{(Eq. 5-3.)}$$

$$I_C = \alpha I_E \qquad \text{(Eq. 5-4.)}$$

$$= I_E - I_B \qquad \text{(Eq. 5-5.)}$$

$$= h_{FE} I_B \qquad \text{(Eq. 5-6.)}$$

$$Z_{in} = h_{FE} r_{tr} \qquad \text{(Eq. 5-7.)}$$

$$Z_{load} = R_L \text{ in parallel with following-stage input Z} \qquad \text{(Eq. 5-8.)}$$

$$A_i = h_{FE} \qquad \text{(Eq. 5-9.)}$$

$$A_v = \frac{R_L}{r_{tr}} \qquad \text{(Eq. 5-10.)}$$

$$= g_m R_L \qquad \text{(Eq. 5-11.)}$$

$$A_p = (A_i)^2 \frac{R_L}{\beta r_{tr}} = A_i A_v = \beta \frac{R_L}{r_{tr}} \qquad \text{(Eq. 5-12.)}$$

Now study the ten points listed on Fig 5-5. They show how the design engineer arrives at stable operating parameters for a linear (class-A) amplifier.

All of the ten points can be understood from studies thus far, with the possible exception of (6). It is stated that the emitter current desired is derived from the intended operating mode. We will expand this point substantially in forthcoming studies. Suffice it to say here that, for example, a low-level stage (such as an audio preamplifier) must be operated at very low emitter (hence base and collector) currents in the interest of low noise level. As the signal level is brought higher and higher in amplitude, more and more dc current must be employed to accommodate the higher peak-to-peak signal swings.

We learned in Section 4-5 that the main problem in stabilization is to control the current gain (β, or h_{FE}) of the common-emitter circuit. The actual value of β differs with different transistors of the same type, and it also varies with temperature changes. Consequently, practical circuit design requires a *controlled beta* (controlled current gain) so that this parameter will remain fixed under varying operating temperatures and with necessary transistor replacements. Thus, if a certain transistor type has a "minimum h_{FE}" of 20, the circuit is designed to limit beta to no more than 20 by means of fixed resistance ratios.

We can now examine a practical single-stage common-emitter linear amplifier and see how such a design is made. See Fig. 5-6. Let us analyze this circuit for practice in determining what we should expect in dc voltage measurements, and to see how it meets the design requirements of Fig. 5-5.

Step 1 is to determine the base voltage, V_B. We can do this by figuring the current in R_B as we have done before, or we can use the second relationship of item (7) in Fig. 5-5. In either case, we get $V_B = +5$ volts.

Then, since the transistor is a silicon (Si) type:

$$V_E = +5 - 0.6 = +4.4 \text{ volts}$$

(Note that this value is greater than 5 times V_{BE}, as called for in Fig. 5-5.)

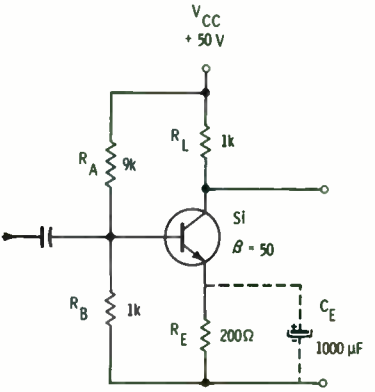


Fig. 5-6. Class-A common-emitter amplifier circuit.

Since the emitter voltage is +4.4 volts, the emitter current (from Ohm's law) must be:

$$I_E = \frac{4.4}{200} = 22 \text{ mA}$$

For rapid analysis, let us assume the same current in the collector as in the emitter:

$$I_C = 22 \text{ mA}$$

Then the dc voltage drop across R_L is:

$$V_{RL} = (0.022)(1000) = 22 \text{ volts}$$

and:

$$V_C = 50 - 22 = +28 \text{ volts}$$

(Note that this value is close to ½ V_{CC}.)

For the given transistor, $h_{FE} = \beta = 50$. Then, from equation 5-3 ignoring I_{CO}):

$$I_B = \frac{0.022}{50} = 0.44 \text{ mA}$$

Note that current I_1 is 5 mA, and therefore meets the requirement of being more than 5 times the base current (I_B).

With R_E bypassed (C_E connected):

$$A_i = h_{FE} = 50 \text{ (from specification sheets)}$$

$$r_{tr} = \frac{26}{22} + 4 = 5 \text{ (approx)}$$

$$A_v = \frac{R_L}{r_{tr}} = 1000/5 = 200$$

$$Z_{in} = (50)(5) = 250 \text{ ohms (Equation 5-7).}$$

Note that since R_E is bypassed for the signal, the signal is not degenerated. Therefore, the full value of beta is in effect, with the exception of the slight shunting action of bias resistors R_A and R_B.

Now we will consider the case in which R_E is not bypassed by C_E. The first big change to note is the effect on input impedance Z_{in} of the transistor alone. When R_E was bypassed, Z_{in} equalled 250 ohms. But when R_E is not bypassed, r_{tr} becomes 205 ohms, or approximately 200 ohms. Then:

$$Z_{in} = (50)(200) = 10{,}000 \text{ ohms}$$

Now it is evident that the value of R_B essentially fixes the value of the new input impedance. Since R_B is only one-tenth of the transistor input impedance, the current gain will be reduced drastically. Let us put this relationship down on record so that we can remember it and use it in practical form.

For practical circuit analysis, the following relationship of currents and resistances is sufficiently accurate:

$$\frac{I_e}{I_{in}} = \frac{R_B}{R_E}$$

This equation says that the emitter current is to the input current as base resistor R_B is to emitter resistor R_E. From this basic relationship we can derive a useful equation for quickly evaluating current gain in a degenerative amplifier. Since collector current (for rapid estimates) can be considered to be the same as emitter current, then substituting I_c (collector current) for I_e (emitter current) in the above basic equation:

$$\frac{I_c}{I_{in}} = \frac{R_B}{R_E}$$

Note that I_c (collector current) to I_{in} (input current) is an expression for current gain (A_i). So:

$$A_i = \frac{R_B}{R_E} \text{ (for an unbypassed } R_E\text{)} \qquad \text{(Eq. 5-13.)}$$

Note also that when an unbypassed R_E is much greater than $r_e + R_{EB}$, voltage amplification (A_v) can be expressed:

$$A_v = \frac{R_L}{R_E} \text{ (for an unbypassed } R_E\text{)} \qquad \text{(Eq. 5-14.)}$$

This equation is valid so long as $r_e + R_{EB}$ is very small in value compared to R_E and can be ignored.

Based on the above equations, the new current gain with R_E unbypassed is:

$$A_i = \frac{R_B}{R_E} = \frac{1000}{200} = 5$$

and the new voltage gain is:

$$A_v = \frac{R_L}{R_E} = \frac{1000}{200} = 5$$

5-3. BASIC NEGATIVE-FEEDBACK CIRCUITS

Although emitter degeneration (series feedback) is almost universally used, other forms of degenerative feedback, which may or may not be used along with emitter degeneration, are often encountered. We will explore briefly the fundamentals of such circuitry here, and then expand on them as we encounter typical circuits in later discussion.

The basic arrangement for collector-base feedback (termed "shunt feedback") is shown in Fig. 5-7. For most practical circuits, the resistance of R_f is small enough that we can use these approximate gain formulas for quick-analysis purposes:

$$A_i = \frac{R_f}{R_L} \qquad \text{(Eq. 5-15.)}$$

$$A_v = \frac{R_f}{Z_{in}} \qquad \text{(Eq. 5-16.)}$$

The quantity Z_{in}, the effective input impedance of the stage, is approximately:

$$Z_{in} = \frac{R_L + R_f}{\beta R_L + R_f} R_{in} \qquad \text{(Eq. 5-17.)}$$

where R_{in} is the input impedance without feedback.

Note that shunt feedback *decreases* the effective Z_{in}, whereas series feedback (such as that provided by an unbypassed emitter resistor) *increases* the effective Z_{in}.

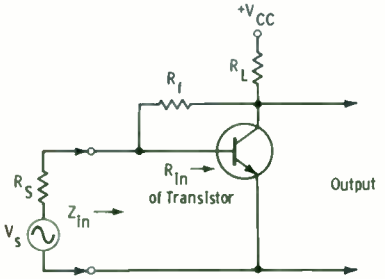


Fig. 5-7. Circuit with shunt feedback.

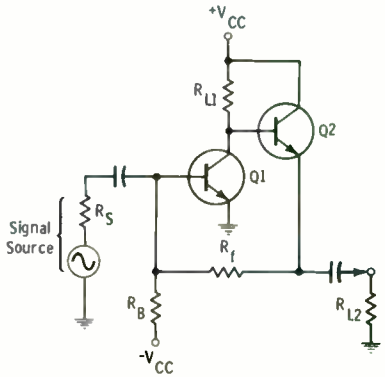


Fig. 5-8. Diagram of a feedback pair.

NOTE: The gain formulas given above are adequate for quick analysis of most circuits because R_f is usually relatively low in value to meet the requirement of "adequate feedback." Somewhat more nearly exact relationships are as follows:

$$A_i = \frac{R_f}{R_f + \beta R_L} \beta$$

$$A_v = \frac{R_f}{R_L + R_f} \beta \frac{R_L}{R_{in}}$$

Fig. 5-8 shows a "feedback pair." This circuit is gaining universal acceptance as a stable, wideband amplifier with inherent ac and dc stability. This type of circuit has low input and output impedance. For quick analysis, its voltage gain can be calculated from the expression:

$$A_v = \frac{R_f}{R_s} \qquad \text{(Eq. 5-18.)}$$

where R_s is the output resistance of the signal source. This formula is sufficiently accurate for use in normal applications of the circuit with low input and output impedances. The voltage gain is almost universally held to a value less than 10.

We will apply these feedback principles to specific circuitry later in this book.

5-4. FEEDBACK GAIN-IMPEDANCE RELATIONSHIPS

Before going into practical circuitry, we should be certain of a "sharp focus" on impedance-to-gain relationships. We will learn why series feedback affects voltage gain much more than current gain, and why shunt feedback affects current gain much more than voltage gain. These facts always bring up the question, "If you cut current gain, how can voltage gain remain the same?" Or: "If current gain is not affected, why does voltage gain decrease?" This section should answer these questions.

See Fig. 5-9A. This circuit is without negative feedback. Assume that:

$A_i = h_{fe} = 50$

Input signal current = 10 μA

Effective Z_{in} = 1000 ohms (resistive)

R_L = 2000 ohms

Then:

Signal current in R_L = (50) (10 μA) = 500 μA.

Signal voltage in Z_{in} = IR = (10 μA) (1000) = 0.01 volt

Signal voltage in R_L = (500 μA) (2000) = 1 volt

$$A_v = \frac{V_{out}}{V_{in}} = \frac{1}{0.01} = 100$$

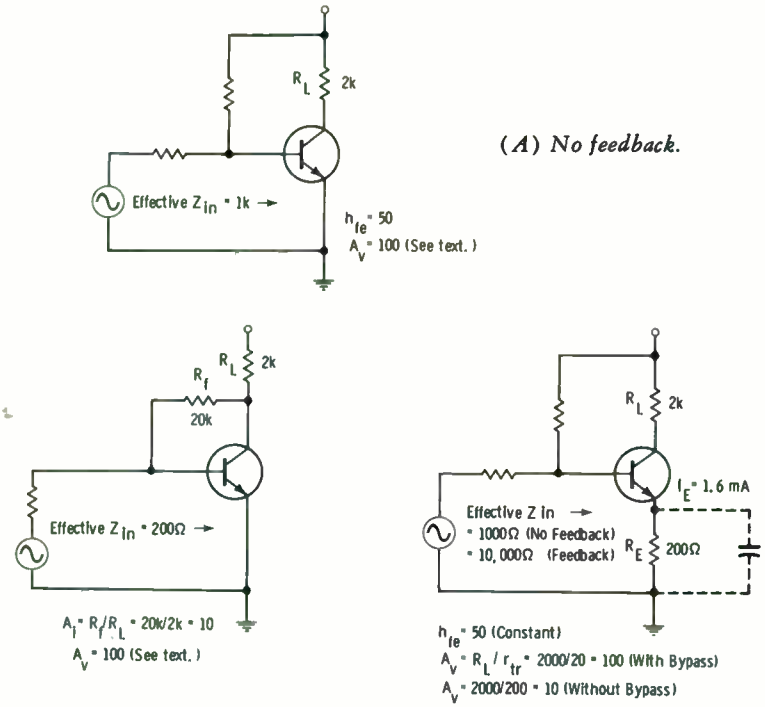


Fig. 5-9. Comparison of shunt and series feedback.

Now see Fig. 5-9B. Shunt feedback is used, and:

A_I is cut to 10 (from 50).

Signal input current is maintained at 10 μA (for reference).

R_{in} is reduced (by shunt feedback) from 1000 ohms to about 200 ohms (from Equation 5-17).

Now:

Signal current in R_L = (10)(10 μA) = 100 μA = 0.1 mA

Signal voltage in R_L = (0.1 mA)(2000Ω) = 0.2 V = 200 mV.

Signal voltage in R_{in} = (10 μA)(200Ω) = 0.002 V = 2 mV

$$A_V = \frac{200\text{ mV}}{2\text{ mV}} = 100 \text{ (the same as for the circuit of Fig. 5-9A)}$$

Note that although the output signal voltage was reduced in amplitude for the same signal input current, the voltage *amplification* remained the same for the circuit of Fig. 5-9B as for that of Fig. 5-9A. The current am-

plification is limited to 10 (which will be below the minimum beta of the transistor used) so that voltage output is stabilized for changes in h_{fe}.

As a matter of interest, the voltage gain calculated from the more complete equation given in the Note above is:

$$A_V = \frac{20k}{2k + 20k}(50)\frac{2k}{1k} = 90$$

The "quick-analysis" value is within about 10 percent of this result.

Fig. 5-9C shows the series-feedback arrangement of the common-emitter circuit. Whether bypassed or not, R_E has no effect on the current-gain parameter of the transistor. But we already know that it drastically affects the voltage gain of the circuit.

Assume that R_E is bypassed and that the signal input is 10 microamperes. Then:

Signal current in R_L = (50) (10 μA) = 500 μA

Signal voltage in R_L = (500 μA) (2000Ω) = 1 volt

$$\text{Signal voltage in } R_{in} = 10\mu A\ (h_{fe}r_{tr}) = 10\ \mu A\ (50)\left(\frac{26}{1.6} + 4\right)$$

$$= 10\ \mu A\ (1000\Omega) = 0.01 \text{ volt}$$

$$A_v = \frac{1}{0.01} = 100$$

Now assume that R_L is not bypassed (series feedback to signal):

$R_{in} = 50\ (20 + 200) = 10{,}000$ ohms (approx)

$V_{in} = (10\ \mu A)\ (10{,}000\Omega) = 0.1$ volt

Signal current in $R_L = 50\ (10\ \mu A) = 500\ \mu A$ (h_{fe} not changed)

Signal voltage in $R_L = (500\ \mu A)\ (2000\Omega) = 1$ volt

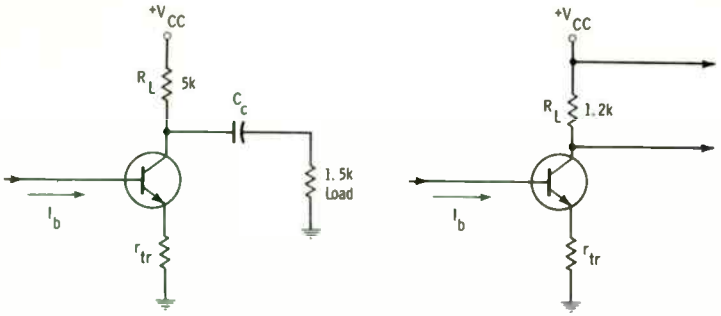
$$A_V = \frac{1}{0.1} = 10 \quad \left(\text{Same as } \frac{R_L}{R_E} = \frac{2000}{200} = 10\right)$$

It has been pointed out that h_{FE} is the dc beta (common emitter) and that h_{fe} is the ac, or signal, beta. This difference can be emphasized by studying Fig. 5-10.

The circuit of Fig. 5-10A is equivalent to a single stage that has a 5k collector load and is feeding a following circuit with a 1.5k input impedance. At low frequencies, the load resistance is effectively 5000 ohms. Assume $h_{FE} = h_{fe} = 50$. The output voltage swing for a base-current swing of (for example) 3 microamperes is:

$$V = (3\ \mu A)\ (50)\ (5000\ \Omega) = 750\ mV$$

As high frequencies (for which the reactance of C_C can be neglected), the effective load becomes 5k in parallel with 1.5 k, or about 1.2k (Fig.



(*A*) *Dc load.* (*B*) *Ac load.*

Fig. 5-10. Circuit equivalents for ac and dc gain.

5-10B). Now the output-voltage swing for a 3-microampere base-current swing is:

$$V = (3\,\mu A)\ (50)\ (1200\,\Omega) = 180\,mV$$

This example simply emphasizes that with h_{fe} equal to h_{FE}, the actual voltage swing is much less for h_{fe} due to the difference in the load the transistor sees.

5-5. PNP AND NPN ON COMMON BATTERY SUPPLY

Many different bias arrangements exist in practical circuits. Study Fig. 5-11, which is a schematic of the first two stages in a television-camera pre-

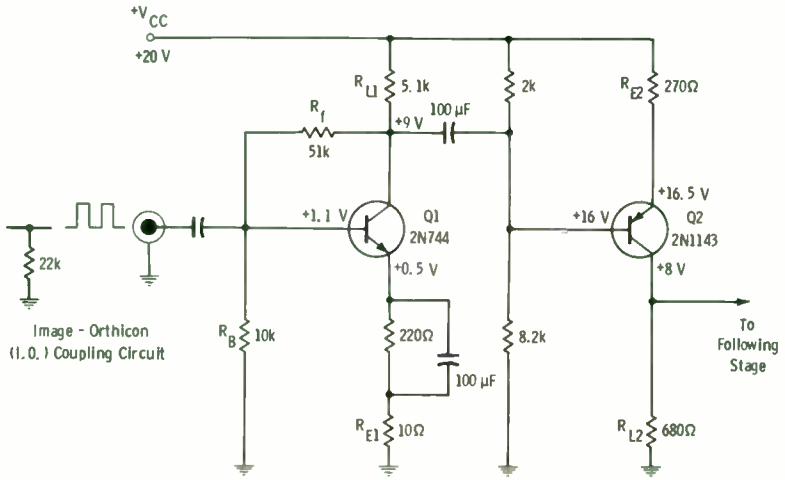


Fig. 5-11. Input stages of a camera preamplifier.

amplifier. Note that the first transistor is an npn type, and the second transistor is a pnp type. There is only one power source, a +20-volt supply. The voltages indicated are those given by the manufacturer as measured to ground with a VTVM. Carefully note that for Q2 the emitter instead of the collector is shown toward the upper part of the diagram; schematics are drawn this way frequently in practice. From the indicated voltages, note how each emitter-base junction is forward biased, and each collector-base junction is reverse biased.

Now let us go through a rapid analysis to review what has been covered thus far in these studies.

Since the voltages are already given, we quickly determine (by Ohm's law) that the emitter current (I_E) of Q1 is:

$$I_E = \frac{0.5}{230} = 2.1 \text{ mA}$$

Remember from our basic studies that it takes about 0.6 volt of forward bias for a silicon junction. (We will find this voltage difference in all relatively *low-current* silicon junctions. The voltage drop will be slightly more in high-current junctions, just as the germanium-junction voltage drop will increase from about 0.2 volt at low currents to 0.3 volt or slightly more at high currents.) Note now that the base of Q1 is 0.6 volt positive relative to the emitter for the necessary forward bias of the junction. This fact tells us at a glance that the 2N744 is a silicon transistor. However, the specification sheets must be used to learn that the 2N744 has a typical h_{FE} of 50 at 2 mA of collector current.

We also know from inspection that the load current (I_L) will be a little more than αI_E because of the voltage divider (R_f-R_B) from collector to ground. The current for this divider must be drawn through the collector load resistor.

Now because the voltages were put on the schematic by the manufacturer, it is not necessary to compute the base current (I_B), but let us do so anyway for a complete understanding:

$$I_C = \frac{20 - 9}{5100} = 2.16 \text{ mA}$$

$$I_B = \frac{I_C}{h_{FE}} = \frac{0.002 \text{ (approx)}}{50} = 40 \,\mu\text{A}$$

All that has been said thus far is that when voltages are designated on the schematic, it is very easy to determine the quiescent operating currents under normal conditions.

Now for small-signal analysis, the 5.1k collector load (R_{L1}) is in parallel with the input impedance of the second stage. The type 2N1143 transistor has a typical h_{fe} of 50. Since the emitter resistor (R_{E2}) of Q2 (270 ohms) is not bypassed, the input impedance of the stage is quite high (we

will determine this later) compared to the parallel combination of the bias-supply divider resistors (2k and 8.2k). So, for a quick analysis, the input impedance (Z_{in}) of the second stage is:

$$Z_{in} = \frac{(8.2k)(2k)}{8.2k + 2k} = \frac{16.4\,k}{10.2k} = 1.6k$$

This 1.6k resistance appears in parallel with the 5.1k collector resistor of Q1, so the effective load seen by Q1 is:

$$Z_{load} = \frac{(5.1k)(1.6k)}{5.1k + 1.6k} = \frac{8.16k}{6.7k} = 1.2k$$

To clarify the analysis, redraw the signal equivalent circuit as in Fig. 5-12. Note that R_B appears in parallel with the input impedance of the transistor, so R_{in} is 10k in parallel with beta times r_{tr}.

$$r_{tr} = \frac{26}{2.1} + 4 + 10 = 26 \text{ ohms (approx)}$$

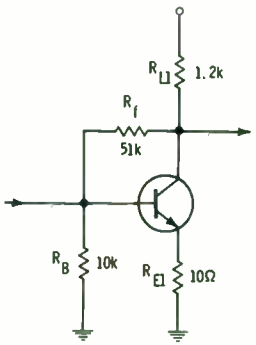


Fig. 5-12. Small-signal equivalent circuit of amplifier stage.

For practical purposes, $R_{in} = 50\ (26) = 1300$ ohms (actually 10,000 ohms in parallel with 1300 ohms). The input impedance of the stage is:

$$Z_{in} = \frac{R_L + R_f}{\beta R_L + R_f} R_{in}$$

$$= \frac{1.2 + 51}{50\ (1.2) + 51} 1300 = 620 \text{ ohms}$$

The voltage gain is:

$$A_v = \frac{51000}{620} = 82$$

If we have a 6-μA signal from the image orthicon tube superimposed on the base bias of 40 μA, this signal current in the 620-ohm input impedance gives an input signal voltage of:

$$V_{in} = I_{in}Z_{in}$$
$$= 6\,\mu A\ (620\,\Omega) = 3.7\ mV$$

With a voltage gain of 82, the output of stage 1 into the input of stage 2 is:

$$V_{out} = 82\ (3.7) = 300\ mV\ (approx)$$

If the reader has followed all these computations closely, he may well ask how we can possibly say, "Let us do a *quick* analysis." How quickly we can make an analysis depends upon how much we practice. We will not need to go through computations in many cases, because we can quickly estimate mentally such items as parallel resistances, effective input and output impedances, etc. The more we practice, the more we "see" circuits automatically in a very rapid manner. We must realize that anything new seems quite difficult at first. Practice, and watch your progress!

If the student desires to progress on to more sophisticated methods of circuit analysis using hybrid parameters, etc., he may find he knows more about transistors, but results in practical circuit analysis will be much slower, more cumbersome, and in the long run no more useful. We say this because of the extremely wide range of tolerances at this time in the actual operating parameters of solid-state devices. This variation is the reason why feedback and stabilization circuitry must be used and understood by maintenance personnel in particular.

Go now to Q2 of Fig. 5-11. Since the emitter is at 16.5 volts, the drop across the 270-ohm emitter resistor is 3.5 volts, so:

$$I_E = \frac{3.5}{270} = 13\ mA$$

The transresistance is:

$$r_{tr} = \frac{26}{13} + 4 + 270 = 276\ ohms$$

The input impedance is:

$$Z_{in} = (h_{FE})\,(276) = (50)\,(276) = 13{,}800\ ohms$$

This result bears out our previous estimate that the transistor input impedance was high compared to the effective resistance of the bias divider.

The voltage gain is:

$$A_v = \frac{R_L}{R_E} = \frac{680}{270} = 2.5$$

So if we have a 0.3-volt signal swing on the base of Q2 from the collector of Q1, we should expect 2.5 times 0.3, or a 0.75-volt signal swing at the collector of Q2. This computation assumes the input impedance of the following stage is fairly high relative to 680 ohms. In this case the assumption is valid because Q3 is a common-collector (emitter-follower) stage—more on this in the next section.

5-6. THE EMITTER FOLLOWER

The emitter follower is used extensively in video circuits, primarily to drive 50-ohm camera lines or 75-ohm distribution lines. It is also very common in other applications in which a low output impedance is desired.

Fig. 5-13 shows the output stage for the preamplifier in Fig. 5-11. The 8 volts on the base is developed across the Q2 collector load. The emitter

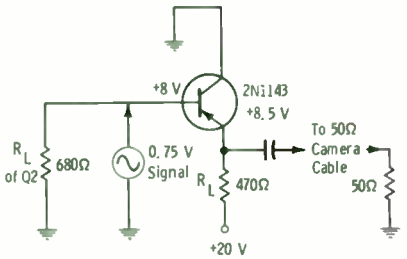


Fig. 5-13. Output stage of camera preamplifier.

measures 8.5 volts, so the voltage drop across R_L is $20 - 8.5 = 11.5$ volts. Therefore:

$$I_E = \frac{11.5}{470} = 24 \text{ mA}$$

The transistor has a typical β of 50; therefore:

$$I_B = \frac{I_E}{h_{FE}} = \frac{0.024}{50} = 480\ \mu A$$

We can see that a current gain (480-μA base current to nearly 24-mA collector current) occurs in the emitter follower just as in the common-emitter amplifier (Fig. 5-14A). But the *voltage* gain is approximately unity. The output signal is of the same amplitude as the input signal, less a very small signal-voltage drop across the base-emitter junction. The voltage gain of this circuit can be explained as follows:

The effective R_L (the load presented to the signal voltage) in this case is the 50-ohm camera-line termination in parallel with 470 ohms, for an effective R_L of 45 ohms. The transresistance (r_{tr}) is:

$$r_{tr} = \frac{26}{I_E} + R_{EB} + R_L$$
$$= 1 \text{ (approx)} + 4 + 45 = 50$$

Then, since g_m is 1/50, or 0.02:

$$A_v = g_m R_L = (0.02)(45) = 0.9$$

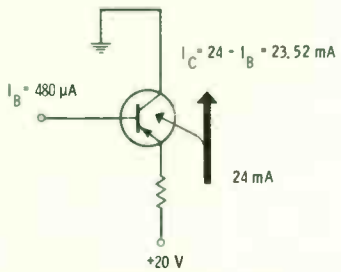
Or, we can say that, since R_L is much greater than $r_e + R_{EB}$:

$$A_v = \frac{R_L}{R_E} \text{ (approx)}$$

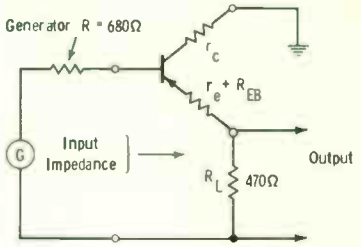
In this case, $R_E = R_L$, so:

$$A_v = \frac{R_L}{R_L} = 1 \text{ (approx)}$$

In practice there are many cases in which we cannot measure any amplitude difference between the signals at the base and emitter of a common-collector stage. For this analysis, we can delete R_{EB} from the g_m computa-



(*A*) *Current relationship.*



(*B*) *Resistances in circuit.*

(*C*) *Use of build-out resistor.*

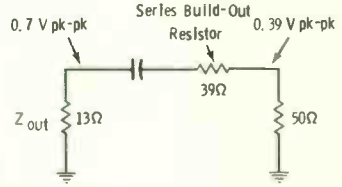


Fig. 5-14. Emitter-follower stage.

tion. The gain may normally be assumed to be unity for quick circuit analysis. Note also that the dc parameters were used in the above analysis, so we are considering only low frequencies (and dc) at the present.

Study Fig. 5-14B, and observe that r_c appears in parallel with the sum of r_e, R_{EB}, and R_L. Since r_c can be assumed to be 1.5 megohms or more, it need not be considered for quick circuit analysis. What is important is to note that the actual input impedance and the output impedance are somewhat interdependent. This is true because the input load is part of the output, and the output load is part of the input. The high intrinsic value of r_c is not serving as isolation between input and output as it did

for the configurations discussed previously. It now forms a parallel resistance only.

Since the emitter follower is used primarily as an impedance transformer, the input and output impedances are most important characteristics to know. While conventional treatments result in highly complex formulas, we can use the following rules of thumb that are fairly accurate in practice:

$$Z_{in} = (\beta + 1)\, R_L \qquad \text{(Eq. 5-19.)}$$

$$Z_{out} = \frac{R_S}{\beta + 1} \qquad \text{(Eq. 5-20.)}$$

The input resistance of the stage in Fig. 5-14 is:

$$Z_{in} = (50 + 1)\ 45 = 2300 \text{ ohms (approx)}$$

This resistance has a reasonably small loading effect on the 680-ohm collector load of Q2.

$$Z_{out} = \frac{680}{50 + 1} = 13 \text{ ohms (approx)}$$

The internal output impedance (sending-end impedance) of an emitter follower can be made quite low, sufficiently low to drive 2-ohm switching buses directly. This low impedance also is the reason why we will usually find a series "build-out" resistor (Fig. 5-14C.) For the receiving end (50 ohms) to "see" a 50-ohm impedance, the 13-ohm output would require a series resistance of 37 ohms. In practice, the standard EIA value of 39 ohms would be used as "build-out" for a 50-ohm load. Note also that this arrangement forms a voltage divider, and a 0.7-volt signal across R_L is dropped to 0.39 volt across the 50 ohms.

In practice, as the effective load impedance increases, the input impedance increases. As the generator impedance increases, the output impedance increases. Providing the generator impedance (previous collector R_L) is not extremely low (so long as it is greater than 10 times R_L, as is usually the case), the formulas given above will prove sufficiently accurate for practical purposes.

Figs. 5-15 through 5-18 illustrate the basic applications of the common-collector configuration. In Fig. 5-15, the output impedance of Q1 is essentially the collector load of 1000 ohms. For class-A operation, we expect a quiescent collector voltage of $\frac{1}{2}V_{CC} = -5$ volts. So assuming germanium transistors with a beta of 50, the common-collector line driver, Q2, has:

$$R_L = \frac{470\ (75)}{470 + 75} = 65 \text{ ohms (Effective load)}$$

$$Z_{out} = \frac{1000}{50 + 1} = 20 \text{ ohms (approx)}$$

$$Z_{in} = (50 + 1)\ 65 = 3300 \text{ ohms (approx)}$$

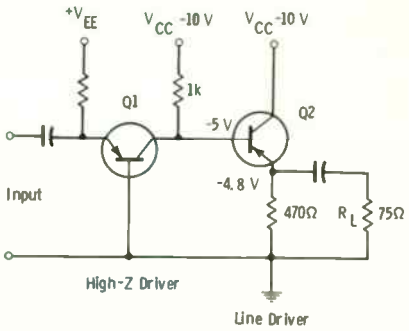


Fig. 5-15. Emitter-follower line driver.

Now study Fig. 5-16A. In this case, the emitter-follower line driver is *driven* by an emitter follower. The lk load is now in the emitter circuit of Q1 rather than the collector circuit. Let us see what happens. (Assume Q1 sees a source resistance of 1000 ohms, and β is 50 for both transistors.)

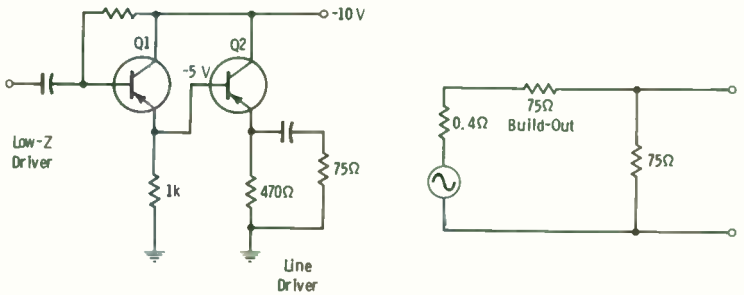
The output impedance of Q1 is:

$$Z_{out} = \frac{1000}{50+1} = 20 \text{ ohms (approx)}$$

Then the output impedance of Q2 is:

$$Z_{out} = \frac{20}{50+1} = 0.4 \text{ ohm (approx)}$$

The equivalent circuit of the output stage is shown in Fig. 5-16B. Note that to feed a 75-ohm load, a build-out resistance of 75 ohms is needed so that the effective internal output impedance becomes 75 ohms. The build-out and load combine to form a 2:1 voltage divider. We must therefore expect to find the signal voltage at the emitter of Q2 to be twice as great as the signal voltage across the 75-ohm load. This condition is normal. For a 1-volt peak-to-peak signal to appear across the 75-ohm load, a 2-volt peak-to-peak signal must be available at the Q2 emitter.



(A) Schematic diagram. *(B) Equivalent of output stage.*

Fig. 5-16. Cascaded emitter followers.

In solid-state circuit applications requiring a very high input impedance, the emitter follower is quite naturally chosen. The Darlington emitter follower shown in Fig. 5-17 consists of two current amplifiers in cascade to provide large current gain and very high input impedance. The input impedance is raised due to the effective product of the betas (h_{fe}) of both transistors. This is to say that, since the base currents have been reduced by the product of the current gains, the input impedance is raised accordingly.

The input impedance of the Darlington current multiplier is limited by the shunting effect of the Q1 collector resistance and capacitance. A technique for reducing this shunting effect is to employ positive shunt feedback, termed "bootstrapping." See Fig. 5-18. The value of R_F is such as to produce at the junction of R1 and R2 a voltage which is in phase with the input voltage. The signal-voltage drop across the bias resistors is thereby reduced, which is equivalent to raising the resistance of the input network. We will find bootstrapping used in other than Darlington circuits for the same reason—to reduce the effective loading of the input biasing networks.

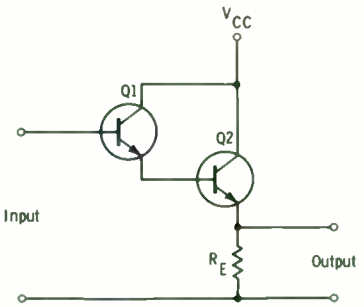


Fig. 5-17. Darlington circuit.

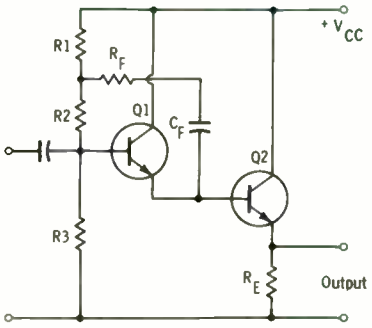


Fig. 5-18. Circuit with bootstrapping.

5-7. BANDWIDTH

Fig. 5-19A shows interelement capacitances of a transistor. Recall that the "width" of the barrier of the pn junction is influenced by the voltage across the junction. Since an electrostatic field is thus generated, we have the equivalent of plates of a capacitor; the spacing between the "plates" is governed by the voltage (and current) of the junction.

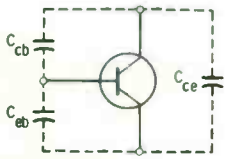
Anything that will increase the width of the pn-junction barrier will be equivalent to spreading apart the plates of the capacitor, resulting in less capacitance. As reverse bias is increased (greater barrier width), the capacitance decreases. As the reverse bias is decreased, junction capacitance increases. For example, decreasing the collector-to-base voltage (V_{CB}) causes C_{cb} to increase. Also, increased emitter current, most of which is injected into the collector through the base-to-collector junction, increases

C_{eb}. The increased pn-junction current in effect reduces the pn-junction width.

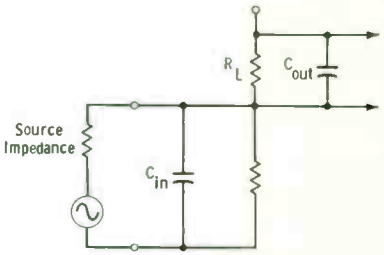
The value of C_{eb} varies from about 1.5 pF in high-frequency transistors to around 50 pF in audio transistors. The collector-emitter capacitance (C_{ce}) is 5 to 10 times greater than C_{eb}, and is also influenced by emitter current and collector voltage. The emitter-base capacitance (C_{eb}), since the pn-junction width is small (forward bias), is higher than C_{ce}, but its effect is less because the input-generator impedance is normally much less than the high internal collector resistance.

Low-frequency transistors give poorer bandwidth than "high-frequency" transistors (low interelement capacitances) can give. A higher R_L will result in less bandwidth due to the effects of output capacitance. Higher currents decrease bandwidth. Capacitance C_{cb} forms a small feedback capacitance which causes oscillation at high (rf) frequencies and must be neutralized. (The latter effect normally is not pertinent to video amplifiers.)

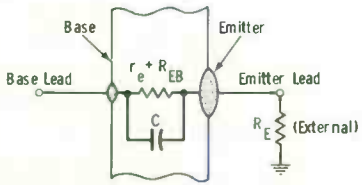
Always bear in mind the high-frequency parameters we have already studied. We know that if a common-emitter circuit results in a half-power frequency of (for example) 1 MHz, a common-base circuit (same transistor) could give a bandwidth beta times as great ($f_{hfe} = f_{hfb}/\beta$). Assuming β is 50, the bandwidth of the circuit would become 50 MHz. But the input impedance is quite low (reducing the gain of the previous stage by radically decreasing its effective R_L), and the current gain is less than one. This is another example of the gain-bandwidth problem.



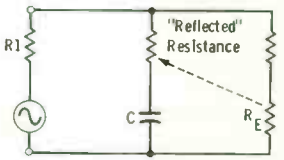
(*A*) *Junction capacitances.*



(*B*) *Low-pass-filter effect.*



(*C*) *Equivalent input circuit.*



(*D*) *Capacitance isolation.*

Fig. 5-19. Transistor capacitance effects.

The basic problem of bandwidth is illustrated in Fig. 5-19B; designers must do what is possible to minimize the effects of the low-pass filters formed by interelement and circuit capacitances. As the source impedance is made higher, the total input capacitance has a greater effect on bandwidth. Also, as R_L is made higher, the effect is the same as if the total output capacitance is increased, and the bandwidth is decreased. Thus R_L (which becomes the source impedance for the following stage) must be a compromise between the gain and bandwidth required.

Another effect of R_L is the "Miller effect": collector-to-base capacitance is multiplied by a factor of 1 + gain. For example, if C_{cb} is 6 pF and the stage gain is 10, an effective C_{cb} of approximately 60 pF appears across the input. So the C_{in} shown in Fig. 5-19B is the sum of C_{eb} and the effective C_{cb}, plus of course component and wiring capacitances.

Now study Fig. 5-19C. This diagram gives a highly simplified equivalent to illustrate intrinsic input capacitance across the base-emitter junction. Note that an unbypassed external emitter resistor (R_E) appears in series with the input capacitance and reduces the effective shunting effect (to higher frequencies) of the capacitance.

An unbypassed emitter resistor (R_E) decreases the effective input capacitance. A "reflection" of R_E appears in series with the shunt capacitance as shown in Fig. 5-19D. Input capacitance can be related to g_m and alpha cutoff frequency (f_{hfb}) as follows:

$$C_{in} = \frac{g_m}{(6.28)(f_{hfb})}$$

Assume a stage without any form of degeneration has a transconductance of 0.035 mho, and that the alpha cutoff (3 dB) is 100 MHz:

$$C_{in} = \frac{0.035}{(6.28)(10^8)} = 56 \text{ pF}$$

Assume an R_E of 100 ohms (unbypassed) is added. Now we have an emitter factor (call it K_e) which is:

$$K_e = \frac{g_m R_E}{1 + (g_m R_E)} = \frac{(0.035)(100)}{1 + (0.035)(100)} = \frac{3.5}{4.5} = 0.8 \text{ (almost)}$$

Since K_e is a degenerative figure, $1 - K_e$ times the former C_{in} is the new input capacitance: $(1 - 0.8)(56) = (0.2)(56) = 11.2$ pF. Bear in mind, however, that although the effective input capacitance has been reduced for greater bandwidth, the gain of the stage has been reduced also.

5-8. MAXIMUM GAIN AND THE NOISE FACTOR

Since voltage amplification for a common-emitter or common-base circuit is:

$$A_v = g_m R_L$$

and since power gain is the square of the current gain times the impedance ratio, one might come to the conclusion that voltage and power gain can be increased without limit by increasing R_L. Such, however, is not the case. The first reason is shown in Fig. 5-20A. The solid lines illustrate A_v as a function of the ratio of R_L to internal collector resistance r_c. The dash lines illustrate current gain (β and α) for the same condition. So that we can visualize R_L in a practical manner, remember that r_c is generally one megohm or more.

After going just this far, we would still conclude that we could use an R_L of about 1 megohm and get a voltage gain of approximately 1000. Because of a second fact, however, we normally can not do this. Large values of R_L result in a second-order mechanism which causes the collector current to depend on the voltage at the reverse-biased collector junction. This mechanism starts to take effect at a voltage gain of 200 to 300, as represented by the "X" on the graph. The net result is that voltage gain no longer increases linearly with an increase in R_L at high values.

Then note the current gain, β. When R_L is equal to r_c, the current gain falls to unity. Of course, alpha is slightly less than 1, and this value also falls off at higher load resistance. Voltage gain is essentially unity in any case for the common-collector circuit.

Fig. 5-20B illustrates the power-gain behavior of a typical transistor. Observe that the common-emitter configuration provides the highest gain. At low values of R_L, the common-collector circuit has greater power gain than the common-base circuit, but for high values of R_L, the opposite is true. It is also evident that power gain optimizes at a different value of R_L for each of the three configurations.

We know the main purpose of any "preamplifier" is to take a very low-level signal and build it up to a higher amplitude. But every component, including solid-state devices, has an inherent "noise factor" which becomes a problem. The lower the signal level at the input, the worse this problem becomes.

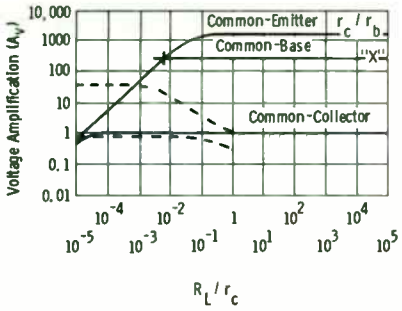
The noise factor (F_o) is the input signal-to-noise power ratio divided by the output signal-to-noise power ratio:

$$F_o = \frac{\text{S/N input}}{\text{S/N output}}$$

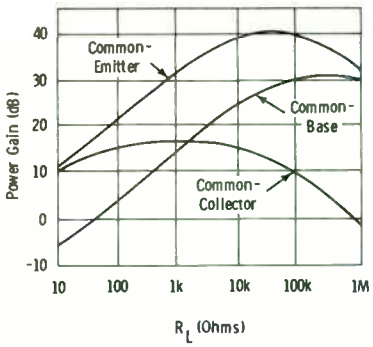
The smaller the value of F_o, the better the noise quality of the amplifier will be.

The noise factor of a given transistor is affected by the operating point (Fig. 5-20C), the signal-source resistance (Fig. 5-20D), and the frequency of the signal (Fig. 5-20E). Ten times the logarithm of the noise-factor ratio gives the noise factor in decibels.

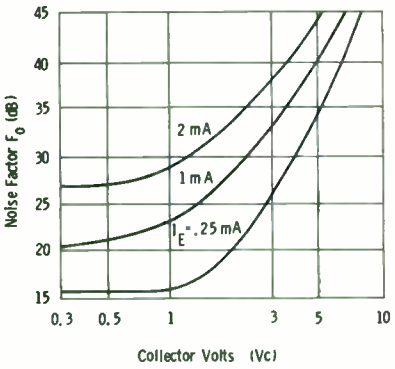
The operating point is established by the zero-signal base or emitter current and the collector voltage. The effects of several values of emitter current and collector voltage on the noise factor of a typical transistor



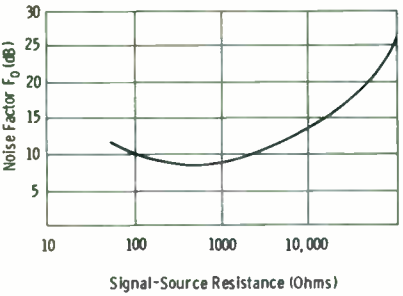
(A) Voltage gain versus load resistance.



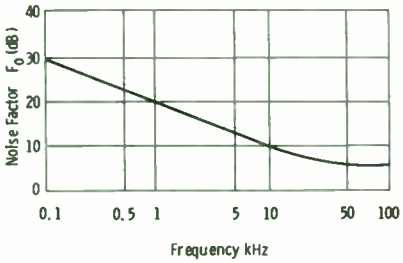
(B) Power gain versus load resistance.



(C) Noise factor versus collector voltage.



(D) Noise factor versus source resistance.



(E) Noise factor versus frequency.

Fig. 5-20. Transistor gain and noise factor.

amplifier are shown by Fig. 5-20C. The curves indicate that, for a given transistor, a low noise factor can be achieved by operating the transistor at an emitter current of less than 1 milliampere and a collector voltage of less than 2 volts.

The resistance of the source feeding the transistor also affects the noise factor of an amplifier. The curve in Fig. 5-20D indicates that the noise factor for a typical transistor can be kept low by using a signal-source resistance in the range of 100 to 3000 ohms.

Fig. 5-20E shows the variation of the noise factor as the frequency is increased. At very low frequencies, the noise factor is high. As the frequency increases, the noise factor improves until about 50 kHz and then starts to increase slowly again. This curve indicates that low-noise dc amplifiers are difficult to design.

Remember also that some transistors especially designed for low-signal-level application have lower noise factors than other types. We can not indiscriminately substitute types of transistors in low-level broadcast applications, for example. With many recent transistors, a noise factor lower than 6 dB can be obtained with careful circuit design.

5-9. AUDIO PREAMPLIFIERS FOR BROADCAST APPLICATIONS

Broadcast applications of solid-state equipment differ from conventional applications primarily in input and output load impedances, and the emphasis placed upon VU and dBm. Therefore, we will stress these items in this instruction so that the reader will be made thoroughly competent in handling maintenance and measurements related to broadcast-station equipment.

The simple installation of Fig. 5-21 will serve for basic discussion. Circuit impedances of 150 ohms are typical up to the line feed of 600 ohms, but all the impedances could be 600 ohms. Conversely, many lines now have 150-ohm impedances, and all circuits in the studio might be 150 ohms. We will get to the significance of impedances after going through the path of microphone signals in Fig. 5-21.

A typical level at the microphone input is −50 dBm. The gain of the preamplifier is 40 dB, so the output into the mixing circuitry is −10 dBm. Typical operating mixer loss is 18 dB, giving −28 dBm at the mixer output. Since the maximum input level to most line amplifiers is around −32 to −35 dBm, a 10-dB pad loads the mixer output to provide a line-amplifier input level of −38 dbm. In this example, the line amplifier is adjusted to provide +18 dBm into the master-gain attenuator. A typical loss setting here is 10 dB, providing +8 dBm to the line-isolation pad. The VU-meter multiplier is set so that a level of +8 VU at this place in the system gives "0" deflection on the meter.

At this point, we must emphasize that the student should have a good working grasp of VU, dB, and dBm relationships.

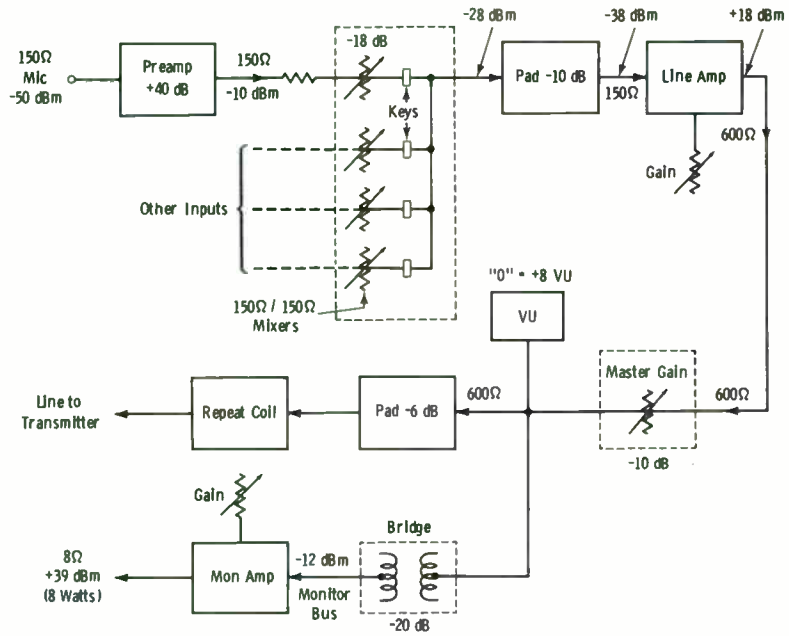


Fig. 5-21. Typical broadcast audio circuit.

DB, DBm, and VU

We will go through a brief review of the highlights with which we are concerned. Refer to Table A-2 in the Appendix. This table lists most of the current, voltage, and power ratios encountered, with their corresponding decibel values. If a dB value is not listed and it is desired to find the corresponding ratio, first subtract one of the given values from the unlisted value (select a value so the remainder will also be listed). Then multiply the ratios given in the chart for each value. To convert a ratio which is not given in the table to a dB value, first factor the ratio so that each factor will be a listed value; then find the dB equivalent for each factor and add them.

Example 1. Find the dB equivalent of a power ratio of 0.631.
Answer: 2-dB loss.

Example 2. Find the current ratio corresponding to a gain of 43 dB.
Answer: 141. First find the current ratio for 40 dB (100); then find the current ratio for 3 dB (1.41). Multiplying, $100 \times 1.41 = 141$.

Example 3. Find the dB value corresponding to a voltage ratio of 150.
Answer: 43.5. First factor 150 into 1.5×100. The dB value for a voltage ratio of 100 is 40; the dB value for a voltage ratio of 1.5 is 3.5 (approxi-

mately). Therefore, the dB value for a voltage ratio of 150 is 40 + 3.5, or 43.5 dB.

Example 4. Find the power ratio for a loss of 57 dB.
Answer: 1.99×10^{-6}. First find the power ratio for 55 dB. This is 3.16×10^{-6}. The power ratio for 2 dB is 0.631. To add dB, power ratios must be multiplied, so: $(0.631)(3.16 \times 10^{-6}) = 1.99 \times 10^{-6}$.

NOTE: In the answer to Example 4, note how much easier it would have been to first find the power ratio for a 50-dB loss (this is 10^{-5}), then the power ratio for a loss of 7 dB (this is 0.199). Then the product, easily found, is 0.199×10^{-5}, which is the same as 1.99×10^{-6}. Practice using the decibel table, and your computations should become quite rapid and accurate.

Fig. A-1 in the Appendix is a graph of dB vs power. For convenience, this graph makes calculations much more rapid, but less accurate, than those made using the table (unless the result happens to fall on marked coordinates).

NOTE: The reference level normally used in broadcasting is the one for which 0 dB is equal to 1 milliwatt (1 mW), or 0.001 watt. Also shown on this graph are other reference levels (no longer used in broadcasting, but sometimes used in other services) of 6 mW and 12.5 mW.

Example 1. If the reference level is 0 dB = 1 mW, what power is represented by a level of +40 dB.
Answer: Use the "A" scale vertically and horizontally to find 10 watts.

Example 2. What power is represented by a level of −40 dB?
Answer: Use the "B" scales and find 0.0000001 watt, or 0.0001 mW, or 10^{-4} mW.

Very important: Note that power levels expressed in dB are independent of impedance values. Also, dB can be expressed as an absolute value *only* if the reference level is specified.

Fig. A-2 in the Appendix is a graph of voltage versus dBm (for levels above −30 dBm). First of all, review these facts: (1) The term dBm says that zero (reference) level is 1 mW. This reference *power level* is independent of the impedance value. (2) When decibels are related to *voltage* or *current*, the value of impedance must be taken into account, since the voltage across or the current through an impedance depends on the impedance value as well as the power level.

Fig. A-2 shows the rms voltage across a matched load for dBm values above −30 dBm. Fig. A-3 shows the same relationship for dBm values below −30 dBm. Note from Fig. A-2 that the voltage across 150 ohms at 0 dBm (1 mW) is just one-half that across 600 ohms at the same 0 dBm. Note from Table A-2 that a voltage ratio of 2 to 1 is equivalent to

6 dB. This tells us there is a 6-dB difference in *voltage* level between 0 dBm in 600 and 150 ohms.

The VU meter is calibrated across a 600-ohm load. In the "calibrate" position (when provided), the meter will read 0 VU when measuring a sine wave that produces a power of 1 mW in 600 ohms. But the meter is essentially reading voltages across the 600-ohm impedance. If we connect a standard VU meter across 150 ohms and feed in a sine-wave signal that develops 1 mW, *a 6-dB correction factor must be applied.* The maximum sensitivity of the VU meter in the normal operating mode is +4 dBm in 600 ohms. Thus if the meter deflects to zero when connected across 150 ohms, the actual level is +4 dBm plus the 6-dBm correction factor, or +10 dBm.

Remember this: A volume unit (VU) implies a complex waveform such as occurs in normal programming. Never use VUs to indicate the level of the sine-wave signal—the latter should always be referred to in terms of dBm. Even if a VU meter is used to read the level of a steady-state sine-wave signal (which is quite permissible), the reading should be referred to as so many dBm, after the multiplier sensitivity and line impedance have been taken into account.

Preamplifier Input Stage

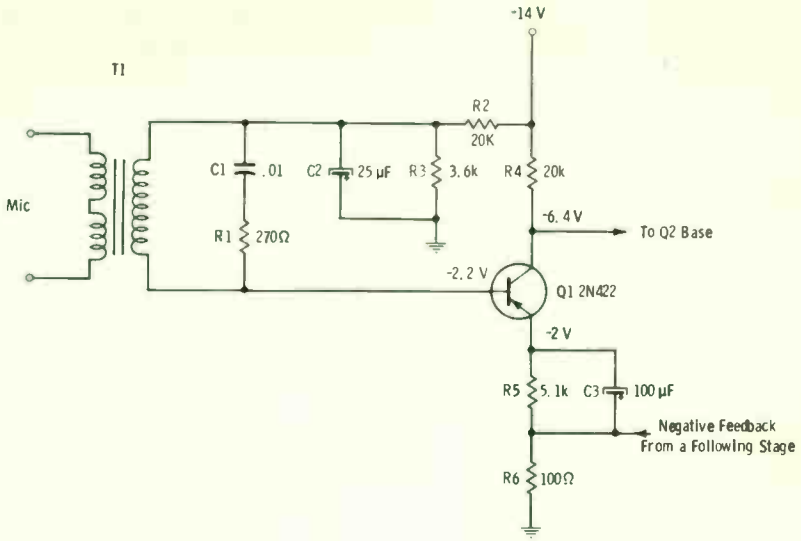
A typical microphone input circuit for broadcast application is shown in Fig. 5-22A. Broadcast microphones are always of low impedance, so the first requirement (low source resistance) for a low noise factor is met.

Secondly, the microphone normally has fairly long cables, so a transformer input is used to minimize hum and other extraneous pickup. If it were not for this fact, a very simple grounded-base (emitter-input) circuit could be used because of its low input impedance.

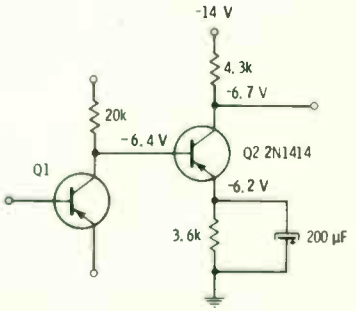
The primary of T1 is balanced to eliminate hum and noise pickup. The secondary is operated unloaded, which is conventional for low-impedance microphones. Note that the base of Q1 is series-fed from the secondary of T1; this is the type of feed almost universally used in solid-state broadcast applications. This technique minimizes any tendency toward load change with signal variation, and results in maximum input gain (maximum transducer gain) from T1. The network R1-C1 across T1 is used to roll off frequencies above the audio passband; therefore, it is sometimes stated that the network provides high-frequency stabilization of the circuit.

Since V_{CE} and the emitter current must be kept very low for a low noise factor, we invariably find high values of R_L (R4) and R_E (R5-R6) in the first stage of a preamplifier.

Now we will go through the dc analysis (operating point) for this stage. Voltage divider R2-R3 provides about −2.2 volts to the base of Q1. Since the 2N422 is a germanium transistor, the emitter voltage will be about −2 volts. So the emitter current is $2/5.2k = 0.38$ mA (approx).



(A) Input stage.



(B) Second stage.

Fig. 5-22. Microphone preamplifier circuits.

Assuming the collector current is the same as the emitter current, we have $-[14-(0.38)(20)]=-6.4$ volts at the collector, so $V_{CE}=-6.4-(-2)=-4.4$ volts.

If you ignore negative feedback and the input impedance of the following stage, what voltage gain would you expect?

$$r_{tr}=\frac{26}{0.38}+100=168$$

and

$$A_v=\frac{R_L}{r_{tr}}=\frac{20000}{168}=120 \text{ (approx)}$$

Fig. 5-22B shows a typical second stage into which the circuit of Fig. 5-22A might be coupled. Since the emitter current of this second stage is 6.2/3.6k = 1.7 mA:

$$r_{tr} = \frac{26}{1.7} + 4 = 19 \text{ (approx)}$$

and

$$Z_{in} = (h_{fe})(r_{tr}) = (40)(19) = 750 \text{ ohms (approx)}$$

Now the effective R_L of the first stage is 20k in parallel with 750 ohms, or about 720 ohms. Therefore the actual A_v of the first stage (still ignoring any negative feedback) is:

$$A_v = \frac{R_L}{r_{tr}} = \frac{720}{168} = 3.7$$

In practice, negative feedback (which is usually applied by an arrangement similar to that in Fig. 5-22A) can bring the voltage gain down to unity or less (depending on the type of feedback).

This analysis has been made to emphasize a point: The first stage of a preamplifier is usually operating at a very low gain, sometimes an actual voltage loss, in the interest of maximum fidelity and low inherent noise.

Fig. 5-23 shows a typical preamplifier input stage for a magnetic phonograph pickup or tape head. This circuit was chosen purposely to

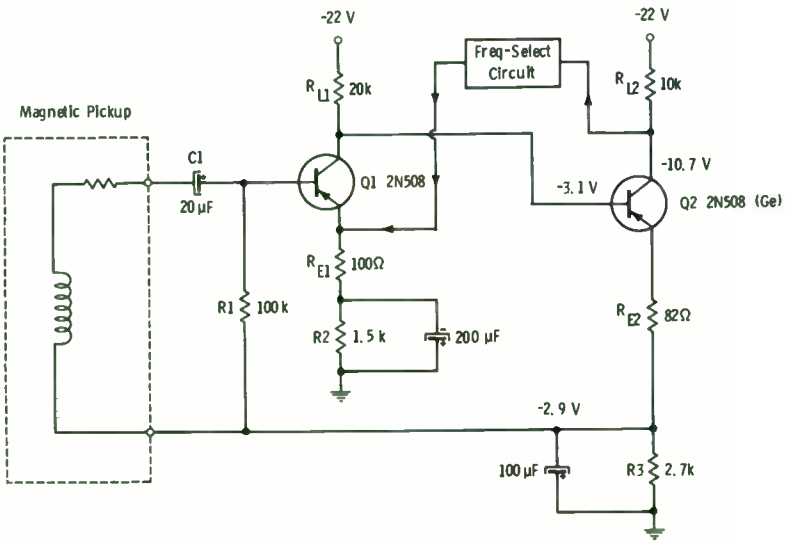


Fig. 5-23. Preamplifier for pickup.

explain how one would go about analysis of the dc operating point. Note that the base of Q1 is biased from a current that is directly proportional to the emitter current of Q2. This connection stabilizes voltage and current bias points for changes in operating temperature and transistor h_{FE}.

This circuit would be difficult to analyze for dc voltage operating point except for the basic rule of thumb that class-A amplifiers have a collector voltage somewhere near one-half the collector supply voltage. (This rule applies to the second and following stages of a preamplifier, *never* to the first stage.) If we start with the assumption of −11 volts at the Q2 collector, we can see how close we would come to the actual voltage readings shown. This problem is included in the exercises at the end of this chapter.

Note also the similarity of this circuit to those of Fig. 5-22A and Fig. 5-22B combined. The second stage has a relatively low input impedance.

Response-curve equalization is almost invariably found in the negative-feedback circuit, as in Fig. 5-23. Fig. 5-24 shows a typical feedback net-

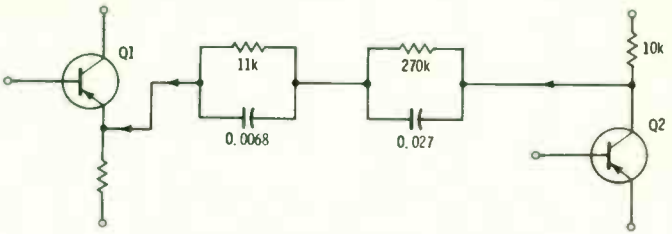


Fig. 5-24. RIAA/NAB feedback network.

work for RIAA/NAB playback characteristics. Note that the capacitors across the resistors provide more feedback at high frequencies than at lower frequencies. Since this is a degenerative circuit, high-frequency response is reduced to provide the proper playback response. This method eliminates the need to load a magnetic cartridge with the proper resistance for high-frequency compensation. Just as in the case of a microphone, a magnetic phonograph pickup is best operated into a relatively high-impedance circuit with proper equalization following the input.

Preamplifier Output Stage

The output stage of a broadcast preamplifier normally feeds a 150-ohm or 600-ohm fader. Fig. 5-25A shows a typical emitter-follower output circuit. To review the analysis of this stage, assume a 600-ohm fader, a 720-ohm source resistance, and a β of 50. Then:

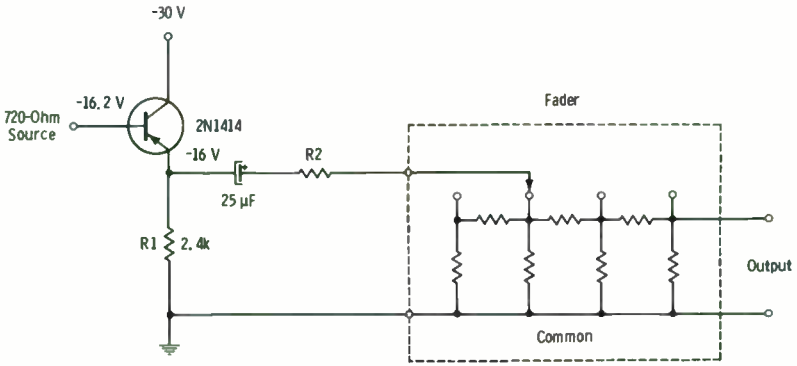
$$Z_{out} = \frac{720}{50+1} = 14 \text{ ohms (approx)}$$

and:

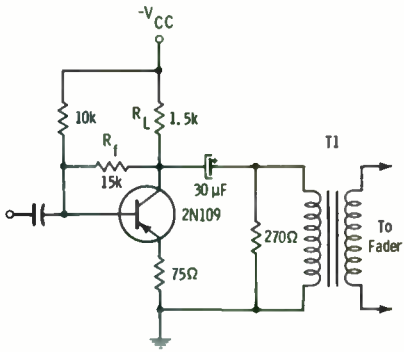
$$R2 = 600 - 14 = 586 \text{ ohms (nearest EIA value} = 560 \text{ ohms)}$$

From previous training, the student should be able to follow the above analysis easily.

Fig. 5-25B shows the typical output stage when a transformer is used. The negative feedback provided by R_f reduces the output impedance as well as the input impedance. The output-transformer primary is always loaded with a fixed resistor to insure a fixed load on the collector circuit.



(A) Emitter follower.



(B) Use of transformer.

Fig. 5-25. Attenuator coupling.

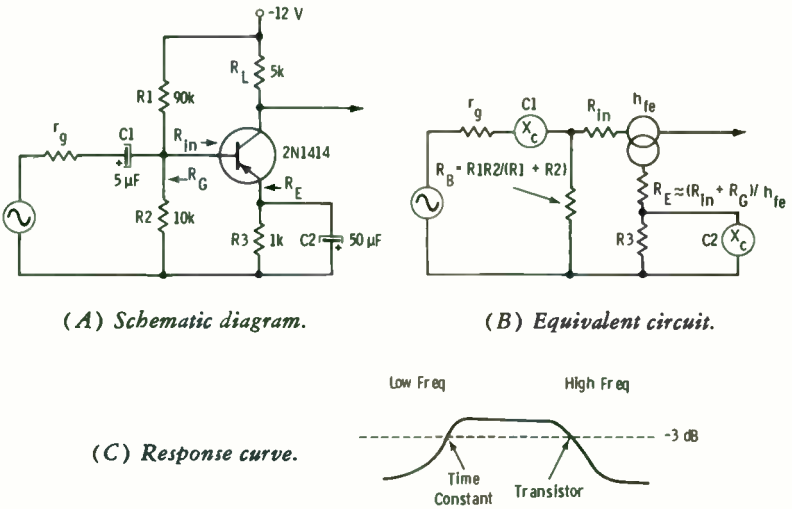
Interstage Time Constants

See Fig. 5-26A. The reference frequency (0 dB) is normally taken as 1000 Hz. Low-frequency response relative to this reference will be reduced 3 dB when the reactance of C1 is equal to the generator resistance (r_g) plus the input resistance (R_{in}) of the transistor (the bias network of R1 and R2 is assumed to be high in resistance relative to R_{in}).

We need a good visualization of the time constants in a transistor circuit. Two new factors, R_G and R_E, are shown in Fig. 5-26A to give this comprehension. Resistance R_G is seen looking back into the network from the base of the transistor, and R_E is seen looking into the emitter. Therefore, R_G consists of the parallel combination of R1, R2, and r_g. So $R_G = R_B$ in parallel with r_g, where R_B is R1 and R2 in parallel. Resistance R_E is related to h_{fe} as shown in Fig. 5-26B.

Reduction of the low-frequency response also results at frequencies for which the reactance of emitter bypass capacitor C2 is no longer negligible. The low-frequency response will be down 3 dB at a frequency where the reactance of C2 equals the resistance of R3 and R_E in parallel.

The rule to keep in mind is that low-frequency response depends primarily on circuit design. High-frequency response is much more dependent on the type of transistor. (See Fig. 5-26C.)



(A) Schematic diagram. *(B) Equivalent circuit.*

(C) Response curve.

Fig. 5-26. Frequency response of a transistor stage.

In broadcasting and high-fidelity commercial applications, we are concerned with a low-frequency response good down to 30 Hz. How does the circuit of Fig. 5-26A meet this requirement? If we analyze this circuit, we find a collector current of about 1 mA. Reference sheets for the 2N1414 indicate h_{fe} is about 40 at this operating current. Then:

$$r_{tr} = \frac{26}{I} + 4 = 26 + 4 = 30 \text{ ohms}$$

$$R_{in} = (h_{fe})(r_{tr}) = (40)(30) = 1200 \text{ ohms}$$

Assume r_g (which might be the collector impedance of a preceding stage) is 1000 ohms. Then:

$$r_g + R_{in} = 2200 \text{ ohms}$$

The capacitive reactance (X_C) of C1 (5μF) is slightly over 1000 ohms at 30 Hz. So the response will *not* be down 3 dB at 30 Hz, since X_C is less than $r_g + R_{in}$. The value of 5μF for C1 is adequate.

Now how about the effect of C2 (50 μF)?

$$R_B = \frac{R1R2}{R1 + R2} = \frac{90k(10k)}{90k + 10k} = 9k$$

$$R_G = \frac{R_B r_g}{R_B + r_g} = \frac{9k(1k)}{9k + 1k} = 900 \text{ ohms}$$

$$R_E = \frac{1200 + 900}{40} = \frac{2100}{40} = 52 \text{ ohms (approx)}$$

Then, R3 in parallel with R_E is:

$$\frac{R3R_E}{R3 + R_E} = \frac{1000(52)}{1000 + 52} = 50 \text{ ohms (approx)}$$

The reactance of C2 (50 μF) at 30 Hz is about 100 ohms. So we can see that the response at 30 Hz will be down *more* than 3 dB because X_C is greater than the resistance of R3 and R_E in parallel. We need about 200 μF for C2 to assure good response at 30 Hz.

NOTE: To find capacitive reactance, we can use the relationship $X_C = 1/2\pi fC$, or we can use the reactance nomographs found in most electronics reference books.

Notice that since h_{fe} appears in the denominator of the expression for R_E, an increase in h_{fe} will decrease R_E. This reduced resistance decreases the time constant and causes loss of lows for a given value of bypass capacitance.

From the foregoing, we see the importance of checking emitter bypass capacitors when loss of frequency response occurs. In older circuitry, dried-up or otherwise defective bypass capacitors of large value can be troublesome. Obviously, the coupling capacitor (C1) is also subject to suspicion when loss of lows occurs.

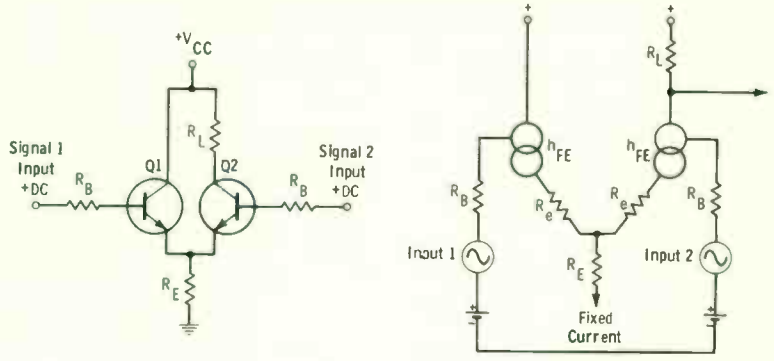
5-10. THE DIFFERENTIAL AMPLIFIER AND INTEGRATED CIRCUITS

Fig. 5-27 shows a basic differential amplifier circuit. The term "differential" in the amplifier name is not related to differential calculus or a differentiating network. The circuit is, quite simply, a difference amplifier.

The circuit is used in many applications, including audio amplifiers. Let us see why.

One of the main contributors to the low-frequency noise problem is drift, which results in dc "noise." For the lowest possible noise level, the base-emitter voltage (V_{BE}) and h_{FE} would ideally remain absolutely constant. Thus anything we can do to approach this ideal condition will result in improved performance.

Fig. 5-27A is a schematic of a typical differential amplifier, and Fig. 5-27B is the circuit equivalent to show functional analysis. Transistors Q1



(A) Schematic. *(B) Equivalent circuit.*

Fig. 5-27. Differential amplifier.

and Q2 draw a very small current, so R_E can have a very high value. This means a constant-current source. A transistor might provide this source, as we will see shortly.

Now assume a positive-going signal is applied to the base of Q1 only (the base of Q2 remains at a fixed dc potential). The low-resistance emitter output of Q1 is coupled directly to the low emitter input resistance of Q2. The positive-going signal applied to the emitter of Q2 decreases conduction, causing the collector to go positive (no phase inversion).

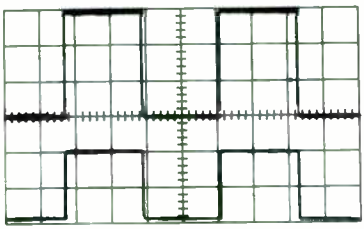
Now assume we make the dc potential applied to the Q2 base more positive. Then Q2 will draw more collector current. This would cancel the effect of the positive-going signal applied to the Q1 base. Here we see that if we applied the same signal to the base of both Q1 and Q2, there would be no change in collector voltage (assuming the V_{BE} and h_{FE} of the transistors were exactly matched).

Any difference in the voltage required at the base of Q2 to maintain a balanced condition is termed the *offset voltage*. For example, the Q2 base might require a dc voltage plus or minus 0.5 volt different from that applied to the Q1 base. The operation of the circuit is such that the Q2 collector responds only to the difference between the two base signal inputs.

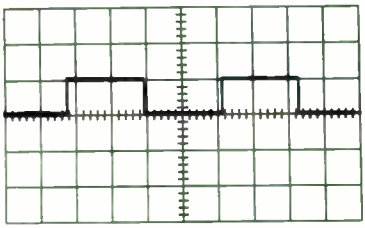
Fig. 5-28 serves to illustrate the basic function of a differential amplifier. It remains now to explain why this type of circuit is becoming so popular in the audio field, as well as in many other applications.

First of all, if the current in one side of the differential amplifier increases, the current in the other decreases by a like amount. Thus drift, or low-frequency "noise," is drastically reduced.

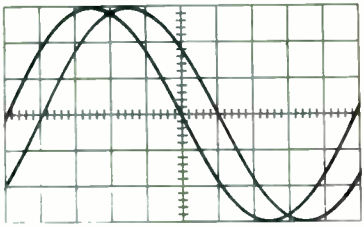
Since a differential amplifier amplifies the difference between two applied signals, an in-phase feedback signal can be applied to one side of the amplifier for negative feedback. There are many other applications, such as agc or other forms of limiting audio amplifiers, in which this property of the differential amplifier may be used to advantage.



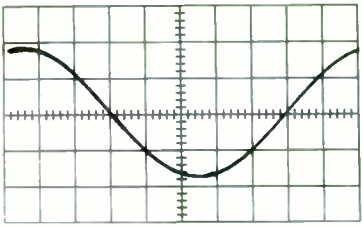
(A) Square waves of unequal amplitude.



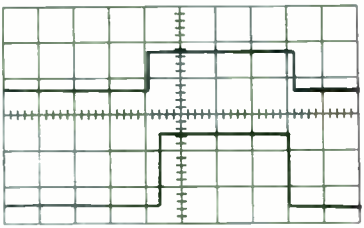
(B) Resultant output for input waveforms in A.



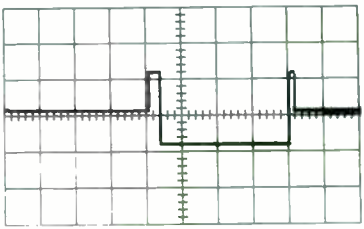
(C) Equal sine waves out of phase.



(D) Resultant output for C inputs.



(E) Square waves, unequal height and width.



(F) Resultant output for input waveforms in E.

Courtesy Tektronix, Inc.

Fig. 5-28. Waveforms for a differential amplifier.

Base-emitter voltages tend to cancel each other in the differential amplifier. But any *difference* of base-emitter voltages cannot be distinguished from the signal. So it is important not only that V_{BE} of the two transistors be matched, but also that each transistor be at the same temperature, since both V_{BE} and h_{FE} are temperature-dependent.

The first method of maintaining a matched pair of transistors at the same temperature was by mounting the transistor pellets on isolated islands of a header in a multiple-lead TO-5 package. This method has been largely replaced by the *integrated circuit* (often called an IC), in which transistors, resistors, diodes, etc., are contained in one structure, which might also be contained in a TO-5 package. The IC is becoming quite common in new audio gear.

See Fig. 5-29. A *monolithic integrated circuit* is contained in one structure (silicon chip). This construction is different from other forms of in-

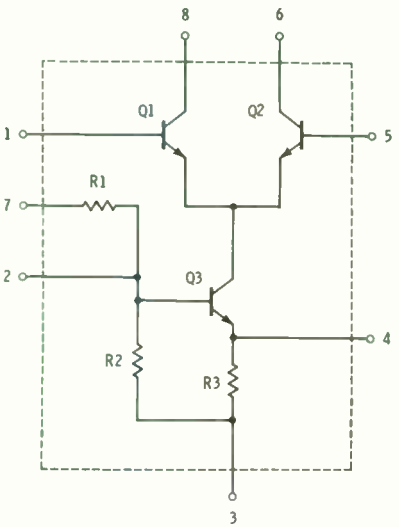


Fig. 5-29. Diagram of an integrated circuit (Type CA 3028).

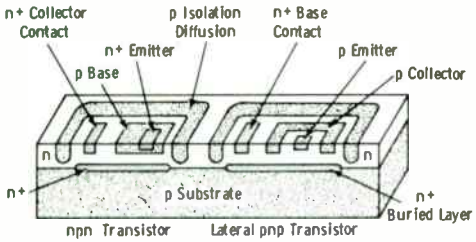
Courtesy RCA Corp.

tegrated circuits that are made up of discrete components on a common substrate (thick-film, thin-film, hybrids, etc.). The circuit is contained in a TO-5 package with 8 pins. The particular circuit in Fig. 5-29 is an RCA CA 3028 IC.

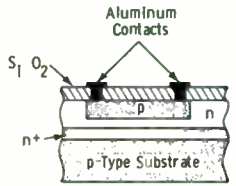
In the circuit of Fig. 5-29, the collector current of Q3 is at very high impedance and is the constant-current source for Q1 and Q2. Note that Q3 is able to be controlled by connection of an external circuit.

See Fig. 5-30A. The GE PA-237 is an all-diffused (monolithic) IC power amplifier that can deliver 2 watts continuous power to a load. (This IC is contained in a flat package rather than a TO-5 package.) The silicon

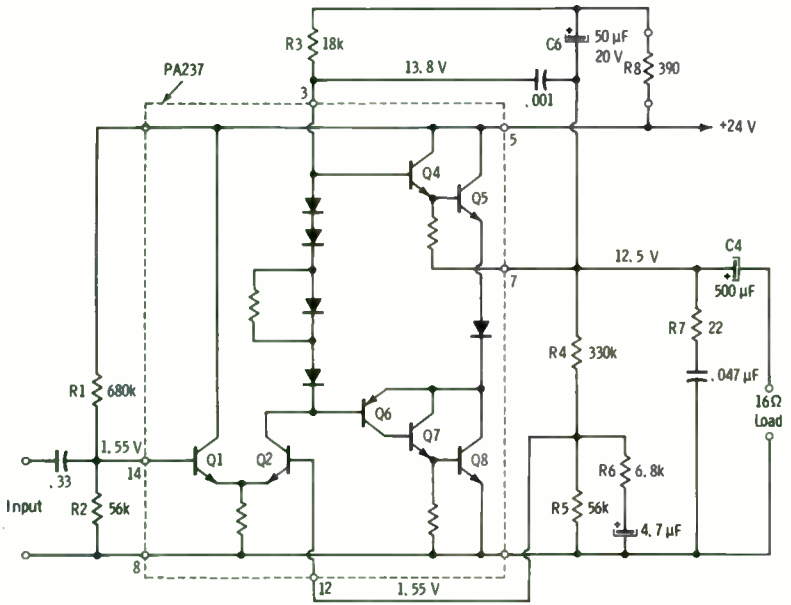
chip consists of a p-type substrate into which the circuit elements are diffused. Interconnections between elements are made with an aluminum metalization pattern on the top surface of the IC chip. Electrical isolation between circuit elements is achieved with a reverse-biased pn junction which completely surrounds each element or group of elements. The p-type region of the isolating junction is common with the p substrate of the IC as shown. The structure on the left in Fig. 5-30A is an npn silicon transistor in which the emitter current passes down across the base region and is collected at the n+ region directly below. Since all the connections



(A) Monolithic transistors in single silicon chip.



(B) Monolithic p-type diffused resistor.



(C) IC used to drive load returned to ground.

Courtesy General Electric Co.

Fig. 5-30. Integrated-circuit power amplifier.

are made on the top surface with the metalization pattern, the collector current passes laterally through the low-impedance n+ buried layer until it reaches a point of shortest path in the vertical direction to the collector contact area.

The n+ buried region not only reduces the saturation resistance of the IC transistor but also minimizes vertical pnp action to the substrate. The p substrate must always be connected to the most negative potential so the isolating junctions will be reverse biased.

The lateral pnp transistor shown at the right of the diagram gets its name from the lateral path of transistor current from emitter to collector. The h_{FE} is low because of the wider base region which is determined by the physical space between the collector and emitter areas of this transistor configuration.

Most monolithic resistors are formed during the p-type (transistor base) diffusion cycle and have resistance values that depend on their physical length and width. Large resistor values become expensive because of the large silicon area required. The cross section of a monolithic resistor is shown in Fig. 5-30B.

When diodes are required in a monolithic circuit, the usual practice is to use a collector-base-shorted transistor connection because it has a low dynamic resistance, reduces current to the substrate, and reduces stored charge in the collector region.

In Fig. 5-30C, the monolithic circuit of the GE PA-237 is shown inside the dash line. The remaining circuitry is external to the chip. If we look at the overall circuit, we see a quasi-complementary push-pull output circuit connection comprising Q4, Q5, Q6, Q7, and Q8. Two transistors are required for the composite driver transistor since the h_{FE} of Q6 (lateral pnp transistor) is low (between 1 and 10 at 1-mA collector current). This arrangement of push-pull composite transistors provides high current amplification so that Q2 can operate at low currents (approximately 0.5 mA). As a result, R3 can be made relatively large (18k) to enhance the voltage amplification. Transistors Q1 and Q2 form a differential amplifier in which Q1 operates as an emitter follower and drives Q2 as a quasi-common-base stage. The Q2 stage does operate in a common-base mode when R6 is zero (i.e., feedback removed from base of Q2). This circuit has no phase inversion of the signal from input to output except within the composite transistor. The feedback signal applied to the base of Q2 is in phase with the input as required with this connection of the differential amplifier.

The differential amplifier has voltage-source base bias and provides good bias stability against variations in h_{FE} for Q1 and Q2, and against temperature variations. It is important that the dc bias voltage at lead 7 be stable if maximum power output at low distortion is to be maintained. The differential amplifier with dc feedback to the base of Q2 provides this stability.

The diode string between the bases of Q4 and Q6 provides the necessary dc bias voltage for the quasi-complimentary push-pull output to minimize distortion at low signal levels.

It is obvious that we do not "service" an IC. It is important for us to know what the intended signal input level is, and what the level at the output should be. If the voltage inputs to the various pins are correct but there is a malfunction within the IC, the entire chip is replaced. Components external to the IC can, of course, be replaced.

The type of circuitry exemplified by this chip will be expanded within the context of studies to follow.

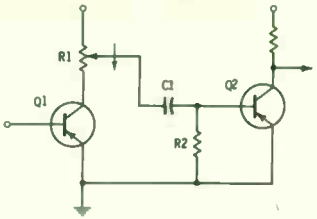
5-11. MANUAL AND AUTOMATIC GAIN CONTROL

We have three characteristics to consider in manual gain controls for solid-state audio amplifiers. (1) Gain: The gain control (and its associated circuit) should permit gain variation from zero to maximum. (2) Noise: A minimum amount of noise (ideally zero) should be introduced when the gain control is operated. A basic rule here is that this requirement can be achieved by avoiding direct current through the gain control, but there are exceptions as will be seen. (3) Frequency Response: All frequencies in the intended passband should be attenuated equally for all positions of the variable arm on the control. This requirement of course does not consider the "bass-boost" arrangement for low gain settings on certain types of gain controls.

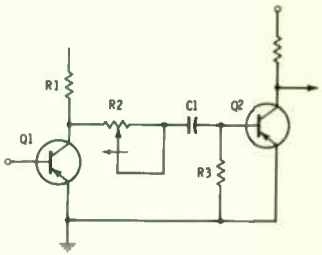
See Fig. 5-31A. This arrangement is not desirable from the noise standpoint. The dc collector current of Q1 will produce noise as the control is varied. NOTE: In all the drawings, the small arrow indicates the direction of clockwise (cw) control rotation (increase of gain).

The circuit of Fig. 5-31B eliminates the problem of direct current through the control, but fails to meet the other two basic requirements for a gain adjustment. Unless R2 is made infinite in value (in the extreme ccw position), the gain cannot be reduced to zero. When the variable arm is in the extreme cw position (zero resistance), C1 alone is used and will attenuate the lower frequencies more than the highs unless the input time constant can be made very long. As the arm is moved toward the ccw position (increasing resistance), the total coupling impedance becomes more R than C. the relative attenuation of the high frequencies compared to the lower frequencies becomes greater (the coupling elements form a low-pass filter with the input capacitance.)

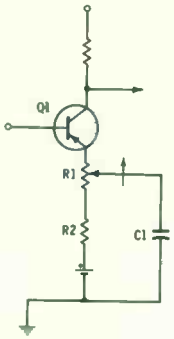
Fig. 5-31C shows an emitter-degenerative type of gain control. As the arm is rotated cw, more of the effective emitter resistance is bypassed, increasing the gain. As the arm is rotated ccw, more degeneration takes place and the gain is reduced. The signal cannot be reduced to zero unless R1 is made very large, say 20k to 50k in value. Then a relatively high-voltage battery is required. Dc emitter current causes excessive noise as the



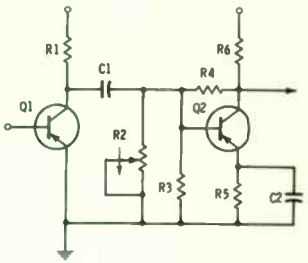
(*A*) *Collector resistor.*



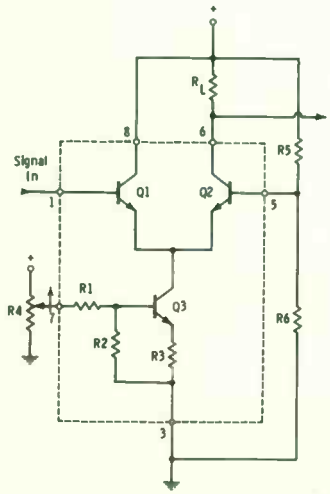
(*B*) *RC network.*



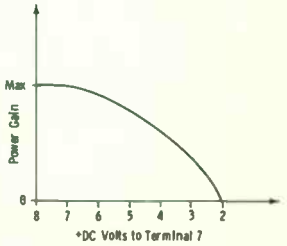
(*C*) *Variable feedback.*



(*D*) *Variable voltage divider.*



(*E*) *Emitter-current control.*



(*F*) *Gain variation.*

Fig. 5-31. Gain controls.

gain control is varied. Thus the noise requirement is not met. Since the gain should vary from zero to maximum, the emitter time-constant variation becomes a frequency-response problem. As more emitter resistance is bypassed by C1 (increasing the gain), the low-frequency response can be boosted. This is because C1 becomes more effective in low-frequency bypassing as the resistance it shunts becomes greater. This results in less degeneration of the lows, increasing their amplitude at the output.

This type of gain control can be quite effective in certain limited applications in which the requirement is not so severe as to demand gain control from zero to maximum. It is often used in some types of video and wideband amplifiers for limited control.

Fig. 5-31D shows a practical method of manual gain control that meets all three basic requirements. Resistor R4 and the parallel combination R2 and R3 form a voltage divider to supply the base of Q2. Note that the basic requirement of no dc through the gain control is violated. But the path for this current is through the relatively large feedback resistor, R4, and the parallel combination of R2 and R3. Thus the change in dc through the control is very small compared to the amplification of the signal. The noise generated by operation of the gain control is not significant.

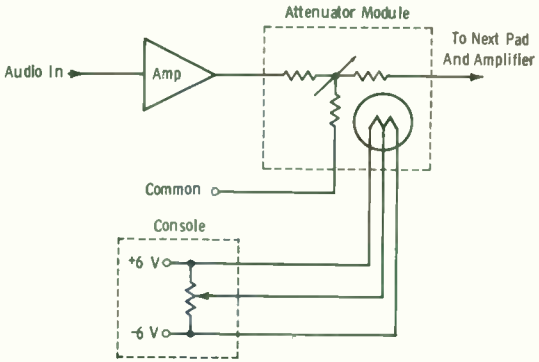
In Fig. 5-31E, the area enclosed by dash lines is the integrated circuit of Fig. 5-29. The gain control (R4), the base-bias resistors (R5 and R6) for Q2, and collector load R_L are external components. Gain control is achieved by varying the positive dc voltage applied to the input (pin 7) of Q3, which serves as a constant-current source for the emitters of Q1 and Q2. As this voltage is increased in the positive direction, the emitter current of Q1 and Q2 increases, increasing the gain. As the voltage is lowered, the total emitter current of Q1 and Q2 is decreased. Variation of gain is typified by the curve of Fig. 5-31F, which shows the result when the Q1-Q2 emitter current is varied between 1 mA and 0.1 mA by controlling the constant-current source. The gain variation results from changes in both beta and impedance. (Remember that beta is dependent on current; also, if the impedance is matched at 1 mA, a mismatch occurs at higher or lower emitter currents.)

NOTE: All of the circuits of Fig. 5-31 apply to internal controls of audio amplifiers. Broadcast consoles employ attenuators as typified by Fig. 5-21. These control the signal levels between either fixed-gain or variable-gain amplifiers.

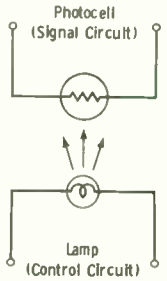
It now remains to become familiar with the latest type of manual console gain controls; when these controls are used, audio itself is not brought into the control console except for VU-meter or monitoring purposes. In Fig. 5-32A, the light-controlled attenuator and light source are in one module which is placed in the audio circuitry. The control pot is in the audio control console, which may be at some distance from the audio racks. Note in

this case that the slider arm rotates between plus and minus voltages so that the constant impedance of the attenuator is maintained just as in physical manual faders.

Fig. 5-32B illustrates the basic principle of these controls. The cells are normally of the cadmium-sulfide type, and the intensity of the light or lights (located adjacent to the cell) changes the cell resistance, thereby affecting the gain of the audio path in which the cell is placed. This



(*A*) *Typical application.*



(*B*) *Principle of attenuator.*

2 & 4 Control Circuit (Light Source)
1 & 3 Signal Circuit (Photoresistor)

1 & 2 Control Circuit (Light Source)
3 & 4 Signal Circuit (Photoresistor)

1 & 2 Control Circuit (Light Source)
3 Shield (Ground)
4 & 5 Signal Circuit (P. E. C.)

(*C*) *Terminal arrangements.*

Fig. 5-32. Light-controlled attenuators.

provides a noise-free control over a wide dynamic range without transients or contact chatter. Resistance *decreases* as lamp intensity *increases*. A current-limiting resistor may be found in series with the lamp, or a transistor constant-current source may be used. The control current is then linear with voltage over a stated range. Fig. 5-32C shows typical terminal arrangements.

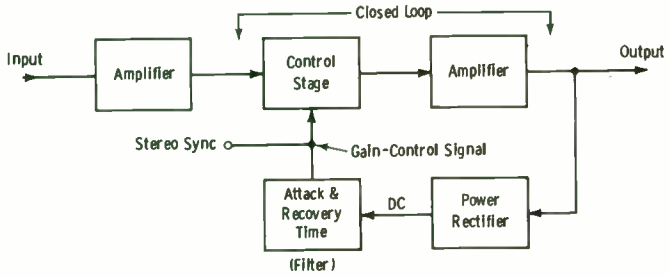
The cell resistance at maximum light intensity may vary between about 50 and 150 ohms. The "dark" resistance may be as high as 100 megohms or more depending upon type. A reaction time of 5 to 20 milliseconds is typical.

A defective unit will ordinarily be detected as an open circuit between the control-circuit (lamp) terminals. Normal resistance at the lamp terminals as checked with an ohmmeter is around 100 to 200 ohms, depending on the voltage rating of the lamp.

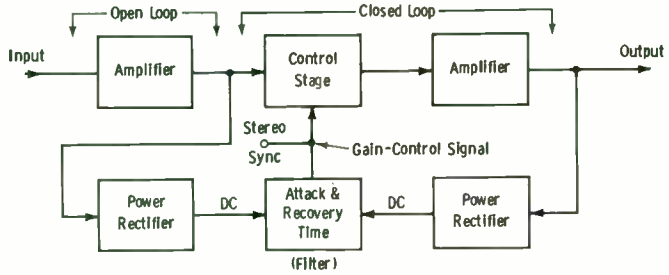
Dual attenuators with tracking capability of 1.5 dB between attenuators have been designed for stereo applications.

Fig. 5-33A shows a block diagram of the fundamental audio amplitude limiter. Fig. 5-33B shows a block diagram of the fundamental agc system. Let us talk about the differences between these circuits now.

Limiter (or compressor) amplifiers normally employ only the closed-loop arrangement of Fig. 5-33A. This loop is degenerative, acting to reduce



(A) Limiter amplifier.



(B) Agc amplifier.

Fig. 5-33. Audio level-control devices.

the gain as the input signal rises above a given level. For instance, an input signal increase of 10 dB might result in an increase at the output of only 1 dB. The gain reduction (in this example 9 dB) is the amount the signal has been limited or compressed.

In addition to gain reduction on high signals, the agc amplifier (Fig. 5-33B) allows a gain expansion over a limited range of lower-level signals. This combination of expansion and limiting, using both the open-loop and closed-loop control, maintains high uniform average levels without over-modulation and (ideally) without raising noise level during dead sound intervals.

When agc is used in stereo applications, an additional factor is involved. It is important to maintain the original amplitude difference between channels so that maximum separation effect is obtained. Using a separate agc amplifier in each channel results in equal left and right volume, and

some of the stereo positioning is lost. This problem is solved by tying the agc amplifiers together so that both have the same dc gain-control signal. This maintains relative gains, and amplitude difference is preserved.

The most common types of gain-controlling devices are those that have variable amplification, those that exhibit a variable impedance, or those that exhibit both methods combined. For example, amplification can be made quite dependent upon base bias; this bias can be supplied by the dc gain-control signal.

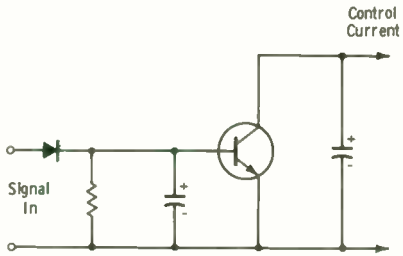
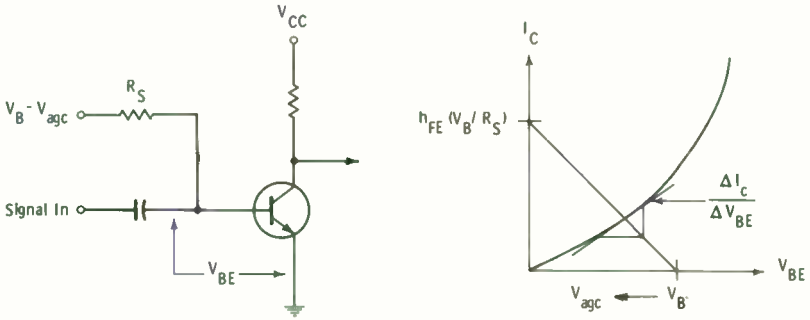


Fig. 5-34. Power rectifier circuit diagram.

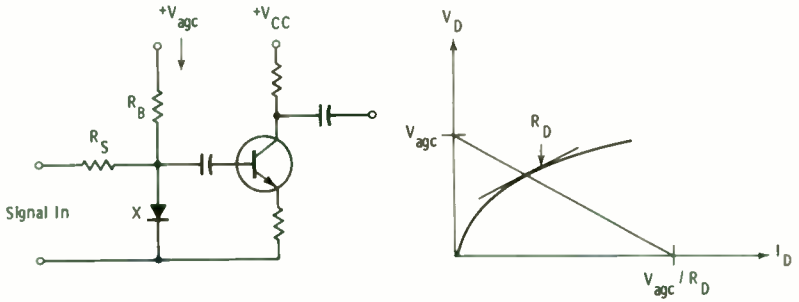
See Fig. 5-34; the "power rectifier" in the blocks of Fig. 5-33 is typified by this circuit. It is a filtered dc amplifier driven from the signal-rectifier diode. In some cases, only the base-emitter junction is used as the rectifier at the expense of the power gain.

Fig. 5-35A shows an example of amplification dependent on base bias. The transistor, biased in the active region, has its base voltage modified by the agc voltage from the power rectifier. Note from Fig. 35B that the *slope* of the curve (ratio of change in collector current to change in base-emitter voltage) is affected. As the signal increases, a larger negative agc voltage is applied to drive the transistor toward cutoff. The maximum gain reduction available in this type circuit is about 15 dB if serious non-linear distortion is to be avoided.



(A) Circuit diagram. *(B) Variation of gain.*

Fig. 5-35. Base-bias control of gain.



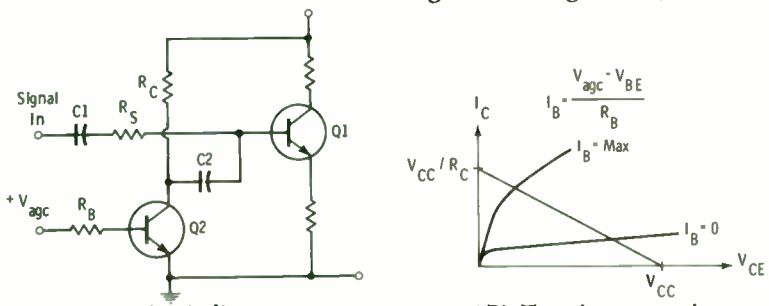
(*A*) *Circuit diagram.* (*B*) *Diode resistance.*

Fig. 5-36. Variable-impedance gain control.

In Fig. 5-36 is an example of variable impedance in parallel with the signal path. When current through a diode increases, the diode resistance decreases, and vice versa. Input current divides between the amplifier input and the diode resistance, R_D. When the signal is increased, the agc voltage increases and R_D decreases, lowering the overall stage gain. With this type of circuit, the signal source must have a high resistance (R_S), and the amplifier input impedance must be high also.

Fig. 5-37 shows a two-terminal shunt arrangement. Look at it this way: If a large agc voltage is developed (large signal), Q2 will have maximum base current and will saturate. Capacitor C2 is then returned to ground and provides a short circuit to the signal. As less agc is developed, Q2 assumes a higher shunt impedance (because its base current is decreased), and the gain is increased. Most of the agc action occurs in the region near Q2 saturation, where the slope of the output characteristic is changing most rapidly.

Video gain-control circuitry is essentially the same as for audio. When the gain control is a "local" function (located on the particular unit), we find a circuit similar to one of those in Fig. 5-38. In Fig. 5-38A, the control

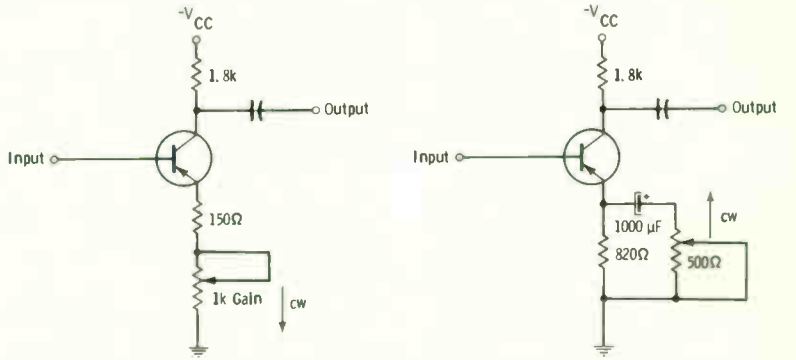


(*A*) *Circuit diagram.* (*B*) *Transistor operation.*

Fig. 5-37. Variable impedance with transistor.

provides variable emitter degeneration to adjust the gain. Note that the control also varies the dc operating point; for this reason, such types of controls have been largely replaced by the circuit of Fig. 5-38B. In this case, only the signal receives a variable amount of degeneration; the dc operating point remains fixed.

In vacuum-tube video amplifiers where the gain is controlled from a remote panel, a variable dc bias control is normally provided to adjust the operating point of a "remote-gain-control" tube in the unit. Such an arrangement is not satisfactory for transistor circuits. The very small increments of dc bias required would be subject to noise and transients in remote cabling and power supplies. For this reason, we will often encounter the light-controlled gain adjustment shown in Fig. 5-39. This is the same circuit as Fig. 5-38B, except that the gain potentiometer is replaced with a photoelectric cell (P.E.C.) or photodiode. The two parallel lamps used for illumination of the photocell have their current controlled from the remote location; this current normally varies from about 70 to 140 mA and is provided by the current source, Q2. For a 20-volt circuit, the lamps are usually 28-volt types, such as the type 1829 or similar bulbs. Thus their life is quite long and reliable.



(A) Variable emitter resistance. *(B) Variable emitter feedback.*

Fig. 5-38. Local gain controls for video.

For video service the P.E.C. will, in general, have a resistance which varies from about 70 ohms to 30,000 ohms, depending on the currents in the lamps that illuminate the cell. The lamp current is adjusted from the remote control position. We will often find this type of control employed in both audio and video applications when the remote-control feature is provided.

In all of the circuits shown by Figs. 5-38 and 5-39, the voltage amplification is approximately equal to the collector load resistance divided by the effective (unbypassed) emitter resistance.

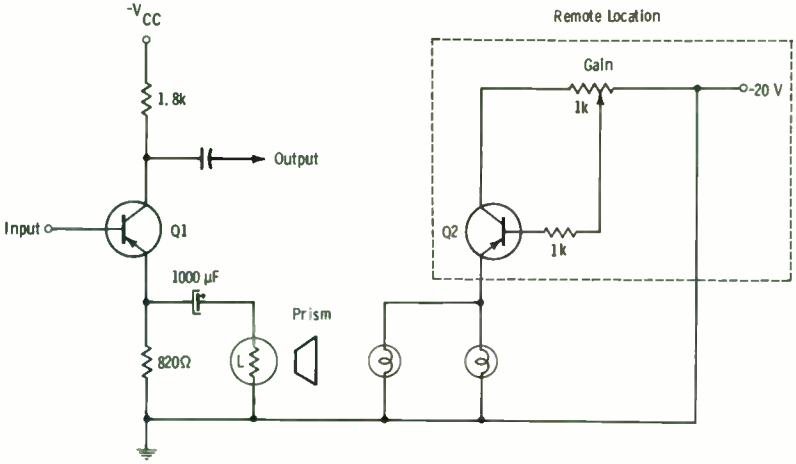


Fig. 5-39. Remote gain control for video.

NOTE: Figs. A-4 through A-7 in the Appendix illustrate all basic operating parameters for the three transistor circuit configurations. Review this information constantly until it is committed to memory.

EXERCISES

Q5-1. Assume you have the circuit of Fig. 5-1B. What value of build-out resistor would you expect to find in series with the emitter to provide a 75-ohm termination?

Q5-2. What effect does an increase in junction temperature have on the quiescent operating point of a transistor?

Q5-3. Explain the difference between fixed bias and self-bias.

Q5-4. Why is reverse saturation current a greater problem in the common-emitter configuration than in the common-base configuration?

Q5-5. If you find a transistor which is specified as having an alpha cutoff of 1000 MHz and a typical beta of 50, what is the beta cutoff frequency?

Q5-6. What value of build-out resistor would be used with the circuit of Fig. 5-13 to match a 75-ohm distribution termination?

Q5-7. What would be the signal amplitude at the 75-ohm termination with the added build-out resistor of Q5-6? (Assume a 0.7-volt signal at the emitter.)

Q5-8. What happens to the output impedance of a common-collector stage if the source impedance should decrease?

Q5-9. In the circuit of Fig. 5-26, assume the same component values but a transistor h_{FE} of 20 and a generator impedance of 150 ohms. Will the value of C1 be adequate for 30-Hz response?

Q5-10. In the circuit of Fig. 5-26, assume the same component values and a transistor with an h_{FE} of 40, but a generator impedance of 150 ohms. What would you expect the 30-Hz response to be now?

Q5-11. In the circuit of Fig. 5-26, if h_{FE} is 80, what will be its effect on the response at 30 Hz?

Q5-12. In the circuit of Fig. 5-26, if the resistance of R3 is doubled, how will this affect (A) low-frequency response and (B) voltage amplification?

Q5-13. In the circuit of Fig. 5-30C, what is the purpose of R7 and the series 0.047-μF capacitor?

Q5-14. In the circuit of Fig. 5-30C, what is the purpose of the C6-R3 network?

Q5-15. What is the purpose of the 0.001-μF capacitor across the network mentioned in Q5-14?

Q5-16. How do you check an IC amplifier such as the one in Fig. 5-30C?

Q5-17. Name the three basic requirements for a manual gain control.

Q5-18. What is the primary advantage of the circuit of Fig. 5-38B over the circuit of Fig. 5-31C?

Q5-19. If an agc power rectifier is connected to pin 7 (Fig. 5-31E) in place of the potentiometer arm, what should be the polarity of the agc voltage with increasing signal?

Q5-20. Could a light-controlled resistor be used in conjunction with agc control circuits?

Q5-21. Name the two basic types of agc circuitry.

Q5-22. Are the agc circuits adaptable to manual gain control?

Q5-23. You have 0 dBm in 600 ohms. Without the aid of charts or graphs, how would you determine the rms signal voltage? What is the voltage?

Q5-24. You have 0 dBm in 150 ohms. What is the rms signal voltage?

Q5-25. Prove that the answers to Q5-23 and Q5-24 result in the same power level.

Q5-26. In Fig. 5-21, if you feed -50 dBm into the preamplifier from a signal generator, what rms signal voltage would you expect to read at the preamplifier output?

Q5-27. In the problem of Q5-26, suppose you were measuring the signal voltage with an oscilloscope. What peak-to-peak voltage would you expect?

Q5-28. Why will you normally find large-value collector and emitter resistors in the first stage of a transistor preamplifier?

Q5-29. Give the corresponding change in signal-to-noise ratio for an amplifier with a noise factor of: (A) 2 dB. (B) 5 dB. (C) 10 dB. (D) 20 dB.

Q5-30. When the input-stage voltage gain is reduced to unity or less by negative signal-voltage feedback, how can the stage be considered an amplifier?

Q5-31. When a frequency-compensation network is used in a preamplifier, in what circuit is it normally found?

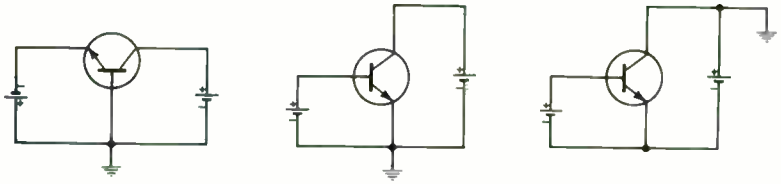
Q5-32. In the audio passband from 30 to 20,000 Hz, does transistor noise factor increase or decrease as the frequency is lowered?

Q5-33. Refer to Fig. 5-23. Ignoring voltages given on the schematic, find your own expected voltages, including those at the Q1 emitter and base (dc operating parameters).

Q5-34. See Fig. 5-40. Fill in all the quantities called for.

Q5-35. What circuit configuration is most sensitive to I_{CO}? Why?

Q5-36. What factor other than a deteriorating transistor is most likely to increase leakage current?



(A) (B) (C)

	(A) CB	(B) CE	(C) CC
h_{FB}			
h_{FE}			
h_{FC}			
I_B (In Terms of I_E)			
I_C (In Terms of I_E)			
Voltage Gain?			
Current Gain?			
Power Gain?			
Phase Inversion?			
Comparative Input Z			
Comparative Output Z			

Fig. 5-40. Diagrams and table for Q5-34.

Fig. 5-41. Diagram for Q5-40.

Q5-37. Does a diode junction increase or decrease in resistance as temperature increases?

Q5-38. What determines "barrier width"?

Q5-39. What determines "barrier capacitance"?

Q5-40. See Fig. 5-41. Point 2 will have what polarity relative to point 1? Point 2 will have what polarity relative to point 3?

Q5-41. In Fig. 5-42, what is the voltage from base to ground?

Q5-42. In Fig. 5-42, what is the emitter current?

Q5-43. In Fig. 5-42, assuming $\alpha = 0.98$, what is the collector current?

Q5-44. In Fig. 5-42, what values of V_B, V_E, and V_C would you expect to read on an external voltmeter?

Q5-45. In Fig. 5-42, what is V_{CE}?

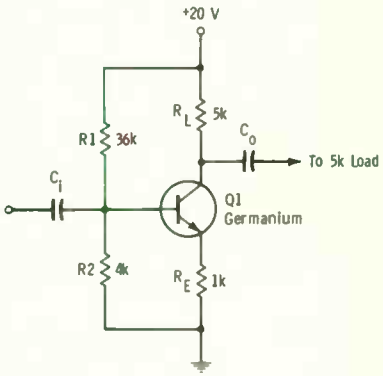


Fig. 5-42. Diagram for Q5-41 through Q5-53 and Q5-56 through Q5-59.

Q5-46. In Fig. 5-42, what is the collector power dissipation?

Q5-47. If α of Q1 in Fig. 5-42 is 0.98, what is β?

Q5-48. What is I_B in Fig. 5-42?

Q5-49. What is the input impedance of the transistor in Fig. 5-42?

Q5-50. What is the load impedance in Fig. 5-42?

Q5-51. What is the voltage amplification of the circuit in Fig. 5-42?

Q5-52. What is your short-cut visualization of voltage-amplification value for Fig. 5-42?

Q5-53. Now see Fig. 5-43. The same transistor is used as in Fig. 5-42. What are the emitter current, collector current, input impedance of the transistor, and load impedance?

Q5-54. What dc V_E and V_C would you expect to measure in Fig. 5-43?

Q5-55. What A_V should you expect in Fig. 5-43?

Q5-56. How will the bandwidth of the circuit in Fig. 5-43 compare to that of the circuit in Fig. 5-42?

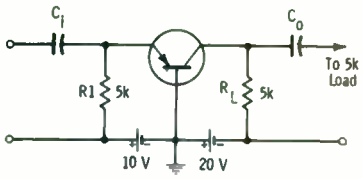


Fig. 5-43. Diagram for Q5-53 through Q5-58 and Q5-61.

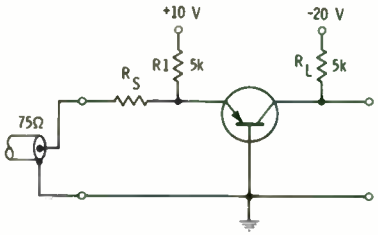


Fig. 5-44. Diagram for Q5-61 and Q5-62.

Q5-57. What is the main disadvantage of the circuit of Fig. 5-43 compared to that of Fig. 5-42?

Q5-58. You have seen that the circuit of Fig. 5-43 has much greater voltage gain than the circuit of Fig. 5-42. Now what are the respective power gains?

Q5-59. In the circuit of Fig. 5-42, if a large bypass capacitor is placed across R_E, what are the new values for voltage gain, transistor input impedance, and power gain?

Q5-60. Does type of transistor affect frequency response?

Q5-61. See Fig. 5-44; this is the same circuit as Fig. 5-43, and the same transistor is being used. The only addition is the series resistor, R_S. If this input is to terminate a 75-ohm line feed, what is the value of R_S?

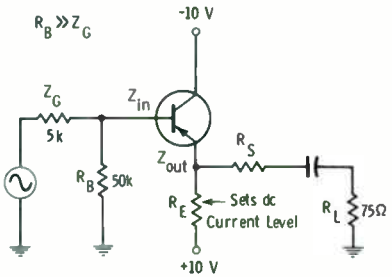


Fig. 5-45. Diagram for Q5-63 through Q5-65.

Q5-62. What is the actual voltage gain in the circuit of Fig. 5-44?

Q5-63. See Fig. 5-45. For the circuit shown, what should be the value of R_S if the emitter follower is to "see" a matched impedance?

Q5-64. What peak-to-peak current would be required in R_L to get a 1-volt peak-to-peak signal?

Q5-65. What value of R_E should be provided to supply a 20-mA peak-to-peak signal current without clipping?

Q5-66. If it is desirable to provide an output impedance of just a fraction of an ohm, what method would be used?

CHAPTER 6

Advanced Linear and Power Amplifiers

Before proceeding, we should be certain of a good visualization of ac (signal) grounds.

6-1. AC GROUNDS

Review these basic facts: When no external emitter resistance is used (or the emitter resistor is bypassed),

$$A_v = \frac{R_L}{r_{tr}} \text{ (approx)} \qquad \text{(Eq. 5-10)}$$

When an external (unbypassed) emitter resistance (R_E) is used, and when its resistance is much greater than $r_e + R_{EB}$:

$$A_v = \frac{R_L}{R_E} \text{ (approx)} \qquad \text{(Eq. 5-14)}$$

Remember this: Resistor R_E constitutes an impedence through which the signal current passes to ac ground. An ac ground point is any point at which the signal power level is reduced to zero. We will define three types of ac ground points (refer to Fig. 6-1): (1) Actual ac ground. This is any chassis point or dc ground point. Also, insofar as the signal is concerned, the hot side of the power supply is an actual ac ground. (2) Apparent ac ground. This term is applied to any point in the circuit which provides a low impedance to the signal between that point and actual ac ground. (3) Virtual ac ground. This term means any point in a circuit at which there are two signals equal in frequency and amplitude, but exactly opposite in phase.

Bear in mind the relationship of ac ground to the signal. In circuit A of Fig. 6-1, with capacitor C assumed to have negligible reactance at the lowest frequency involved, R_E affects only the dc parameters; the ac

ground is directly at the emitter, so the signal sees only $r_e + R_{EB}$. If the capacitor is not used, the signal sees $r_e + R_{EB} + R_E$. This is to emphasize that the value of r_{tr} is quite different for the two conditions. Remember that for convenience in our use of transresistance we include R_E in all computations.

In the circuit of Fig. 6-2A, at first glance one might think that the rather large value of R5 would result in a large value of R_E and drastically affect signal amplification. But this assumption is not true, and here is the importance of being able to recognize and handle ac grounds. So we will go through the analysis of this type of circuit and show how to break it down step by step.

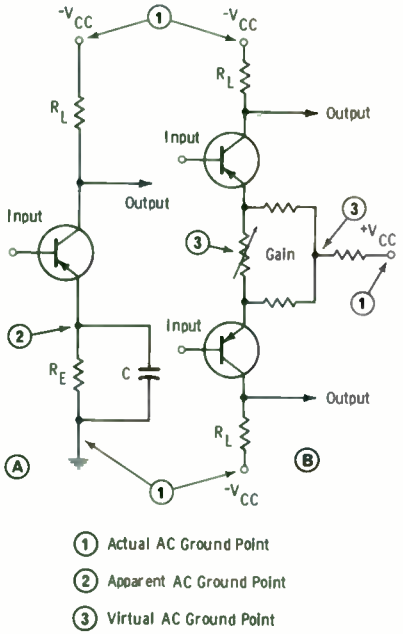
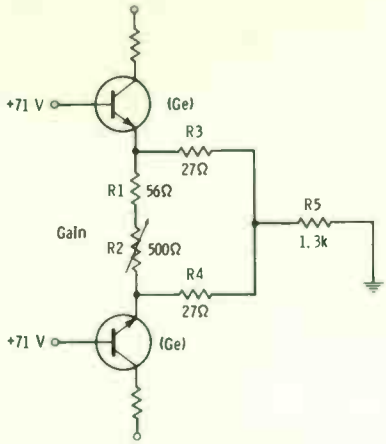
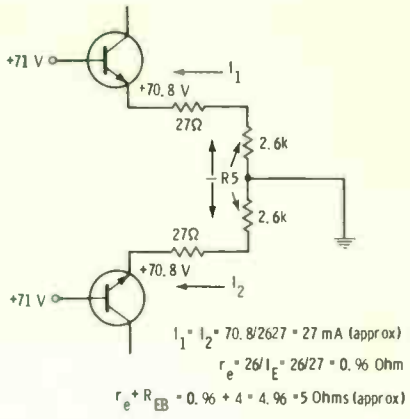


Fig. 6-1. Types of ac grounds.

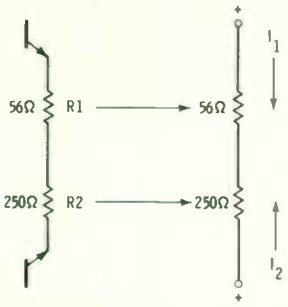
First of all, these are germanium transistors with +71 volts from a preceding dc amplifier appearing at each base. We know immediately that the emitter of each npn transistor will be 0.2 volt (approximately) negative with respect to the base, or 70.8 volts positive with respect to ground (Fig. 6-2B). In Fig. 6-2B, R5 is redrawn to account for the fact that both emitter currents (shown in terms of electron flow) pass through this resistor. The effect is essentially the same as if R5 were made up of two resistors, each twice the original value. We find the emitter currents to be 27 mA; therefore the dynamic emitter resistance (r_e) is 0.96 ohm. Adding the constant of 4 ohms, we get $r_e + R_{EB} = 5$ ohms (approx).



(A) *Circuit diagram.*

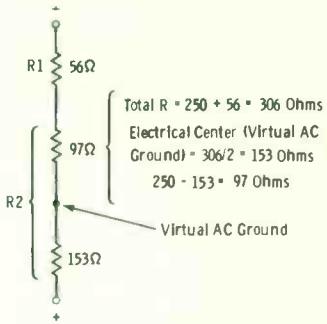


(B) *Emitter currents.*

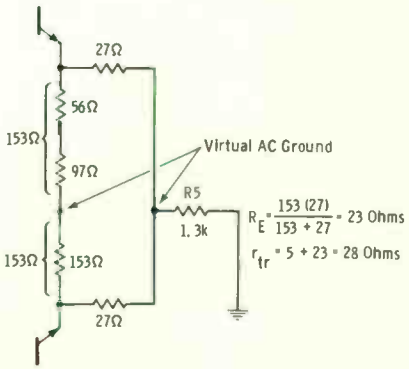


(C) *Gain-control branch.*

(D) *Control-branch currents.*



(E) *Electrical-center computation.*



(F) *Virtual ac grounds.*

Fig. 6-2. Analysis of circuit with virtual ac grounds.

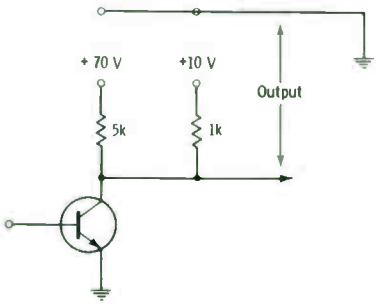
Now assume the GAIN control (R2) is set in the middle of its range, or 250 ohms (Fig. 6-2C). This will be the "nominal" gain setting. Electron flow now is as indicated in Fig. 6-2D, so find the "electrical center," or virtual ac ground. Following the indicated computation, we arrive at the equivalent circuit of Fig. 6-2E. The virtual ac ground occurs in R2 where the two legs become equal in value, as indicated. Since the signal currents are equal and opposite in phase in R5 (push-pull stage), another virtual ac ground occurs at the "top" of this resistor, as indicated in Fig. 6-2F. So far as the signal is concerned, the effective R_E for each transistor is 153 ohms in parallel with 27 ohms, or 23 ohms.

So now get the value for r_{tr}. This is $5 + 23 = 28$ ohms. If we know the collector loads, we can now compute A_v, etc., when the GAIN control is set at midrange.

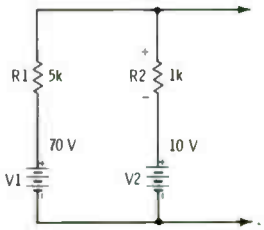
6-2. PRACTICAL APPLICATION OF THEVENIN'S THEOREM

Before proceeding, review the exercises at the conclusion of Chapter 1 relating to the application of Thevenin's theorem.

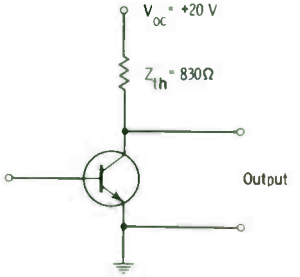
We will often encounter circuits, such as the one in Fig. 6-3A, in which several voltages of different values are applied to components connected to one point in the circuit. For convenience, let us restate Thevenin's



(*A*) *Circuit diagram.*



(*B*) *Equivalent collector network.*



(*C*) *Effective circuit.*

Fig. 6-3. Application of Thevenin's theorem.

theorem as follows: Any linear network of impedances and generators, if viewed from any two points in the network, can be replaced by an equivalent voltage source (V_{oc}) and an equivalent impedance (Z_{th}) in series.

Transfer the circuit of Fig. 6-3A to its equivalent in Fig. 6-3B. First of all, we know there will be current in R2 because of the difference in voltage (60 volts) between V1 and V2:

$$I = \frac{V}{R} = \frac{60}{R1 + R2} = \frac{60}{6k} = 10\,mA$$

The voltage drop across R2 from this circulating current is:

$$V = IR = (0.01)(1000) = 10 \text{ volts}$$

(This voltage drop has the polarity shown because V1 is larger than V2.)

Then:

$$V_{R2} + V2 = 10 + 10 = 20 \text{ volts} = V_{oc}$$

or,

$$V_{oc} = I(R2) + V2$$

or,

$$V_{oc} = \frac{(V1 - V2)R2}{R1 + R2} + V2$$

$$= \frac{(70 - 10)1000}{6000} + 10$$

$$= \frac{60k}{6k} + 10 = 10 + 10 = 20 \text{ volts}$$

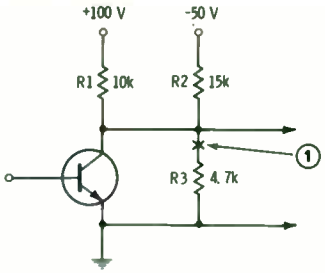
We have simply developed Thevenin's theorem numerically as applied to the circuit of Fig. 6-3A. We have found the equivalent voltage (V_{oc}) looking back into the network from the output terminals.

In this example, finding the equivalent impedance (Z_{th}) is quite simple, since the "batteries" are replaced with short circuits. The impedance looking back into the network is simply 5000 ohms in parallel with 1000 ohms, or about 830 ohms. The effective circuit is shown in Fig. 6-3C.

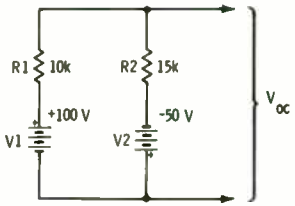
Fig. 6-4A shows another type of circuit we will encounter. Remember that we work from a basic two points in the network, and then add one element at a time until all are included in the equivalent (and simplified) network.

Our first step is to open the circuit at point 1, eliminating R3. Then we have the circuit of Fig. 6-4B, and:

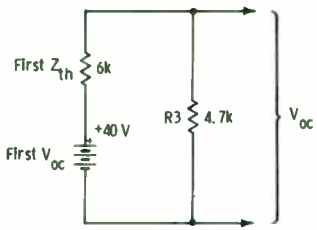
$$V_{oc} = \frac{(V1 - V2)R2}{R1 + R2} + V2$$



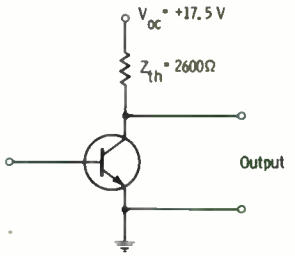
(*A*) *Circuit diagram.*



(*B*) *Equivalent collector network.*



(*C*) *Equivalent including R3.*



(*D*) *Effective circuit.*

Fig. 6-4. Additional example using Thevenin's theorem.

$$= \frac{[100 - (-50)]15k}{15k + 10k} - 50$$

$$= \frac{(150)(15k)}{25k} - 50 = 90 - 50 = 40 \text{ volts}$$

The equivalent impedance is:

$$Z_{th} = \frac{(R1)(R2)}{R1 + R2} = \frac{(15k)(10k)}{25k} = \frac{150k}{25k} = 6000 \text{ ohms}$$

So up to point 1, we have a V_{oc} of 40 volts and a Z_{th} of 6k. Now draw the first equivalent circuit as in Fig. 6-4C and add R3. There is now no V2, so:

$$\text{Total } V_{oc} = \frac{(\text{First } V_{oc})(4.7k)}{\text{First } Z_{th} + 4.7k} = \frac{(40)(4.7k)}{6k + 4.7k} = 17.5 \text{ volts}$$

$$\text{Total } Z_{th} = \frac{(6k)(4.7k)}{6k + 4.7k} = 2.6k, \text{ or } 2600 \text{ ohms.}$$

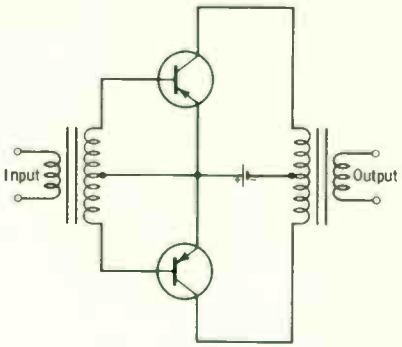
The final equivalent circuit is shown in Fig. 6-4D.

6-3. CLASS-B AUDIO OPERATION

Class-B push-pull power amplifiers are used mainly in equipment requiring high power output and high power efficiency.

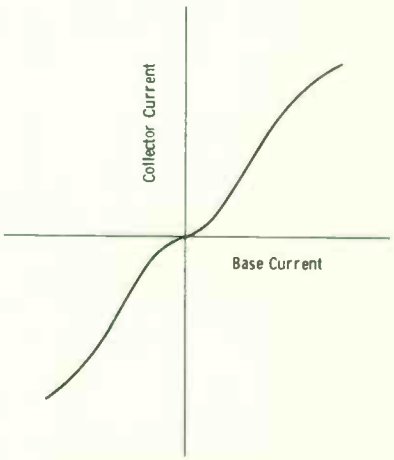
Fig. 6-5A shows a simplified circuit of a class-B amplifier. The emitter-base junctions are zero biased. In this circuit each transistor conducts on alternate half cycles of the input signal. The output-signal half cycles are combined in the secondary of the output transformer. Maximum efficiency is obtained even during idling periods (no input signal), because neither transistor conducts during these periods.

An indication of the output current waveform for a given signal current input can be obtained by considering the dynamic transfer characteristic for the amplifier. It is assumed that the two transistors have



(*A*) *Schematic diagram.*

(*B*) *Single transfer characteristic.*

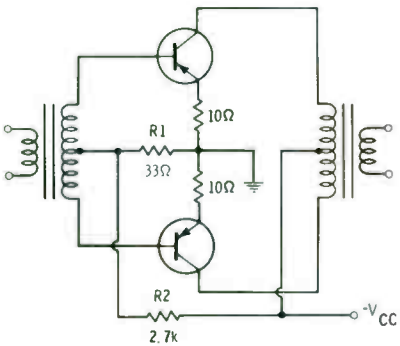


(*C*) *Combined transfer characteristics.*

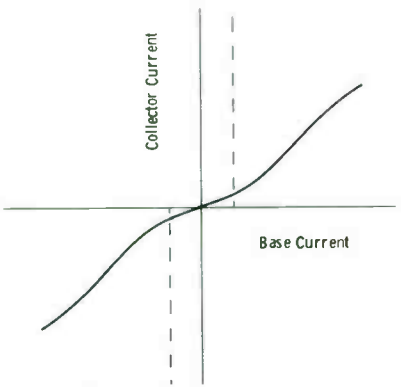
Fig. 6-5. Basic class-B amplifier.

identical dynamic transfer characteristics. The characteristic for one of the transistors is shown in Fig. 6-5B. The variation in output (collector) current is plotted against input (base) current under load conditions. Since two transistors are used, the overall dynamic transfer characteristic for the push-pull amplifier is obtained by placing two of the curves back-to-back. The two curves are shown back-to-back *and combined* in Fig. 6-5C. Note that the zero lines of the two curves are lined up vertically to reflect the zero bias current. Note that severe distortion occurs at the crossover point, that is, at the point where the signal passes through zero. This crossover distortion becomes more severe with low signal input currents. Crossover distortion can be eliminated by using a small forward bias on both transistors of the push-pull amplifier.

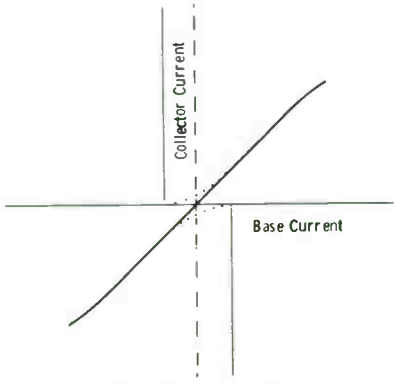
A class-B push-pull amplifier with a small forward bias applied to the base-emitter junctions is shown in Fig. 6-6A. A voltage divider is formed by resistors R2 and R1; the voltage developed across R1 supplies the base-emitter bias for both transistors.



(*A*) *Schematic diagram.*



(*B*) *Uncombined transfer curves.*



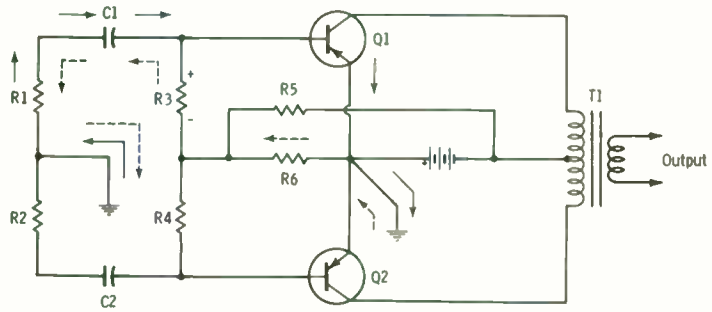
(*C*) *Combined transfer curve.*

Fig. 6-6. Use of forward bias in class-B amplifier.

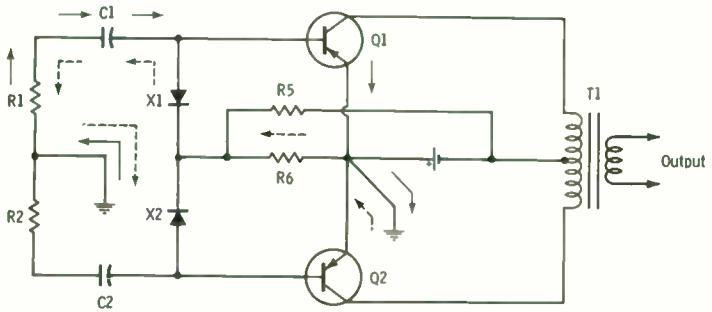
A study of the dynamic-transfer characteristic curve of the amplifier demonstrates the elimination of crossover distortion. In Fig. 6-6B, the dynamic transfer characteristic curves of the two transistors are placed back-to-back (but not combined) for zero-base-current bias conditions. The dash lines indicate the zero-signal point for each curve when forward bias is applied to the transistors. To obtain the overall characteristic (Fig. 6-6C), the two graphs are shifted until the dash lines meet; then the individual curves (dotted lines) are combined to form the solid curve.

We can not satisfactorily use resistance-capacitance coupling to the input of a class-B push-pull amplifier without special considerations. Here is why.

In the class-B push-pull amplifier, one transistor conducts during one half cycle of the input signal; the other transistor remains nonconducting during this time, except for the small forward bias applied to minimize crossover distortion. Refer to Fig. 6-7A. Assume that the input signal causes transistor Q1 to conduct. Electrons (solid-line arrows) leave the right-hand plate of coupling capacitor C1, enter the base-emitter junction of transistor Q1, flow to the emitter ground connection, go through ground



(A) Input resistors.



(B) Input diodes.

Fig. 6-7. Class-B amplifier with RC input coupling.

to the junction of resistors R1 and R2, and pass through resistor R1 to the left-hand plate of C1. (Resistor R1 represents the output resistance of the previous amplifier.) Capacitor C1 charges rapidly through this low-resistance path. However C1 cannot *discharge* through the emitter-base junction of Q1; for practical purposes, the junction represents an open circuit to electron flow *from emitter to base*. Electrons on the left-hand plate of capacitor C1 must flow through resistor R1, through ground to the emitter connection of Q1, and through resistors R6 and R3 to the right-hand plate of C1. (The discharge path is shown by the dash-line arrows.) Capacitor C1 discharges slowly because it must discharge through R3; normally the resistance of R3 is made large to avoid shunting of signal current around the Q1 base-emitter junction. The discharge current through R3 develops a reverse-bias voltage with the polarity indicated. The reverse bias can cause *class-C* operation with resultant severe distortion of the signal. (The discharge current through resistor R6 does not result in a reverse bias because the battery current in the opposite direction through this resistor maintains a forward bias.)

The advantages of RC coupling (economy and better frequency response) can be retained by replacing resistor R3 with a diode, as shown in Fig. 6-7B. Diode X1 is reverse biased and acts as a high-value resistance when the input signal has the polarity that causes the emitter-base junction of Q1 to conduct. This high resistance prevents the shunting of signal current around the emitter base junction. The charge path (solid-line arrows) for capacitor C1 is the same as that for the circuit shown in Fig. 6-7A. In the discharge path (dash arrows), resistor R3 is now replaced by diode X1, which is forward biased and has negligible resistance during the discharge period. Capacitor C1 discharges rapidly, therefore, and reverse bias of the emitter-base junction is avoided.

NOTE: The secondary windings of any class-B driver transformer (input to class-B stage) should be bifilar wound to obtain tight coupling and thereby minimize leakage inductance. Otherwise, "ringing" may occur in the crossover region as a result of the "kickback" energy stored in leakage inductance.

Now let's go into some power computations. By definition:

$$A_p = \frac{P_{out}}{P_{in}} = \frac{I_o^2 R_L}{I_{in}^2 R_{in}} \qquad \text{(Eq. 6-1.)}$$

Now since, for a small load resistance, the ratio I_o/I_{in} is the same as beta (common-emitter circuit), the power gain (which can be expressed in terms of the square of the current gain times the ratio of output to input resistance) can be expressed:

$$A_p = \beta^2 \frac{R_{c\text{-}c}}{R_{b\text{-}b}} \qquad \text{(Eq. 6-2.)}$$

where,

$R_{c\text{-}c}$ is the collector-to-collector load resistance, and
$R_{b\text{-}b}$ is the base-to-base input resistance.

With this information, observe again Fig. 6-6A. Assume that the power-supply voltage is −12 volts, the impedance of the output-transformer primary is 300 ohms, center tapped, and the impedance of the input-transformer secondary is 2000 ohms, center tapped. Assume a nominal beta of 50.

Then from Equation 6-2:

$$A_p = (50)^2 \frac{300}{2000} = 2500(0.15) = 375$$

What is the actual power output? The rule of thumb here is:

$$P_o = \frac{2\,V_{CE}^2}{R_{c\text{-}c}} \qquad \text{(Eq. 6-3.)}$$

In this equation, V_{CE} is the collector-to-emitter voltage at *no signal*. Remember that in a class-B stage, this voltage is very close to the power-supply potential (close to current cutoff); it may be taken as about 85 percent of V_{CC}. Thus, in this example, assume $V_{CE} = -10$ volts. Then:

$$P_o = \frac{2(-10)^2}{300} = \frac{200}{300} = 666\text{ mW}$$

But remember that the power in the secondary depends on transformer efficiency, which we normally assume to be about 75 percent. So the actual power delivered by the secondary is (0.75) (666 mW) = 500 mW (approx).

Since the power gain is 375 and the power output (collector-to-collector) is 666 mW, then the required input power is:

$$P_{in} = \frac{P_{out}}{A_p} = \frac{666\text{ mW}}{375} = 1.8\text{ mW (approx) base-to-base}$$

Then remember that we must also assume 75 percent efficiency of the driver transformer, so the driver power must be:

$$P_{driver} = \frac{P\text{ into input}}{0.75} = \frac{1.8\text{ mW}}{0.75} = 2.4\text{ mW}$$

The best performance check of any amplifier (audio or video) is to determine how faithfully it reproduces a square wave. When a transformer is used, it must be physically large for good low-frequency response, and it must be of high-quality design and construction throughout. Therefore, a great deal of effort has been expended in developing "transformerless"

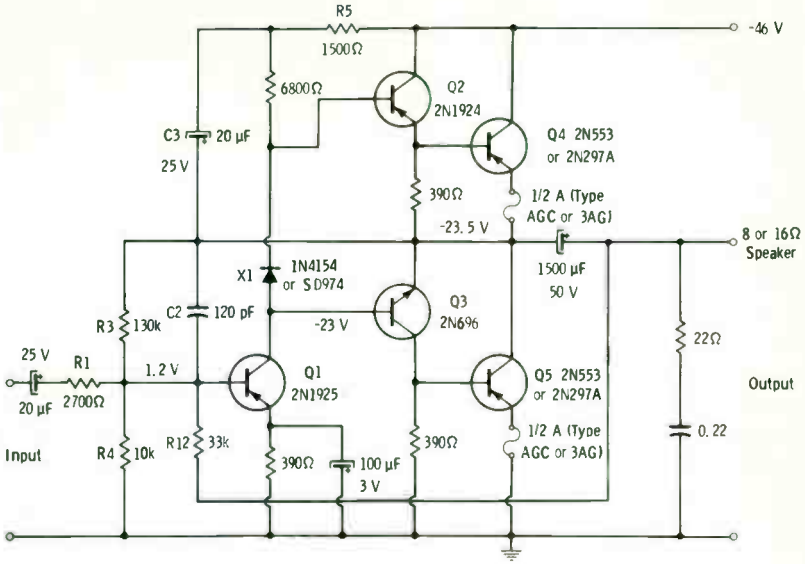
push-pull circuitry. In tube circuits, a number of tubes must be used in parallel to obtain the necessary current to develop power in low-impedance devices such as the voice coils of loudspeakers. Power transistors, however, lend themselves ideally to this application since they are inherently low-voltage, high-current devices. Fig. 6-8A shows an amplifier of the "single-ended push-pull" output class. Let's see how it works. (The information relative to Fig. 6-8 was furnished by the General Electric Company, Semiconductor Products Department, and is used with permission.)

Note that the bases of Q2 and Q3 are driven in phase. Transistor Q2 is used in an emitter follower stage (no phase inversion), whereas Q3 is in a common-emitter stage (phase inversion). When a negative signal is applied to the base of Q4, this transistor draws current, which must pass through the speaker because the simultaneous positive signal at the base of Q5 holds Q5 near cutoff. When the signal polarity reverses, Q4 is cut off and Q5 conducts. Thus we have a "single-ended push-pull" output stage. As the diagram shows, its input is strictly direct-coupled, resulting in excellent low-frequency response.

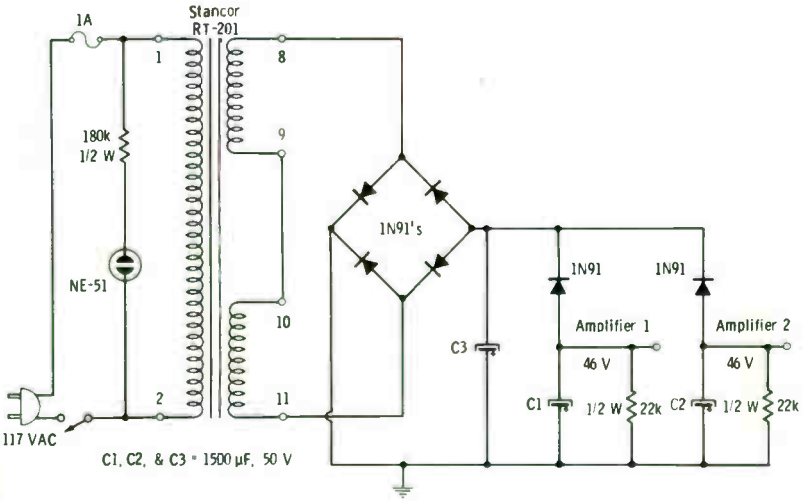
The circuit also has the advantage of dc feedback for temperature stabilization of all stages. This feedback system stabilizes the voltage division across power-output transistors Q4 and Q5. Transistors Q2 and Q3 also operate class-B in the Darlington connection to increase the current gain. Using an npn transistor for Q3 gives the required phase inversion for driving Q5 and also makes possible the advantage of push-pull emitter-follower operation from the output of Q1 to the load. Emitter-follower operation makes possible lower inherent distortion and low output impedance.

Transistors Q4 and Q5 have a small forward bias of 10 to 20 mA to minimize crossover distortion and to operate the output transistors in a more favorable beta range. This bias is set by the voltage drop across the 390-ohm resistors that shunt the inputs to Q4 and Q5. Transistors Q2 and Q3 are biased at about 1 mA (to minimize crossover distortion) with the voltage drop across the silicon diode (X1). Junction diodes have a temperature characteristic similar to that of the emitter-base junction of a transistor. Therefore, this diode also gives compensation for temperature variation of the emitter-base resistance of Q2, Q3, and Q4. These resistances decrease with increasing temperature; thus the decrease in forward voltage drop of approximately 2 millivolts/degree centigrade of the diode provides some temperature compensation.

Transistor Q1 is a class-A driver with an emitter current of about 3 mA. Negative feedback to the base of Q1 lowers the input impedance of this stage. A source impedance higher than the input impedance is needed so that the feedback current will pass into the amplifier rather than into the source; resistor R1 limits the minimum value of source impedance. The value of R3 permits about one-half the supply voltage to appear across transistor Q5.



(A) Amplifier schematic.



(B) Power-supply schematic.

Courtesy General Electric Company, Semiconductor Products Department

Fig. 6-8. "Single-ended push-pull" amplifier.

About 11 dB of positive feedback is applied across R5 by way of C3. This bootstrapping action helps to compensate for the unsymmetrical output circuit and permits the positive peak signal swing to approach the amplitude of the negative peak. This positive feedback is offset by about the same magnitude of negative feedback through R3 to the base of Q1. The net amount of negative feedback is approximately 14 dB resulting from the connection of R12 from the output to the input. In addition, there is the local feedback inherent in the emitter-follower stages. The value for feedback capacitor C2 was chosen for optimum square-wave response (short rise time and minimum overshoot).

A ½-ampere fuse is used in the emitter of each output transistor for protection and to provide local feedback. (The type of fuse used has a dc resistance of about 1 ohm.) This local feedback increases the bias stability of the circuit and also improves the declining frequency response of Q4 and Q5 at the upper end of the audio spectrum. Because of reduced transistor efficiency above 10 kHz, care should be used when checking the amplifier for maximum continuous sine-wave output at these frequencies. If continuous power is applied for more than a short time, the resultant heating may raise the transistor current enough to blow the ½-ampere fuses. Actual performance of the amplifier does not suffer, since the power level in music and speech declines as the frequency increases beyond about 1 to 2 kHz.

The speaker system is shunted by a 22-ohm resistor in series with a 0.22-μF capacitor. This network is used to compensate for the continued rise of the amplifier load impedance and its accompanying phase shift beyond the audio spectrum.

The overall result of using direct coupling and ample degeneration is an amplifier with low distortion, good bandwidth, and output impedance of about 1 ohm for good speaker damping. The performance specifications for the amplifier of Fig. 6-8A include: power response at 1 watt, flat from 30 Hz to 15 kHz and down 3 dB at 50 kHz; total harmonic and IM distortion at 1 watt both less than 1 percent. At 7 watts the IM distortion is less than 2-½ percent, and the total harmonic distortion is less than 1 percent measured at 50 Hz, 1 kHz, and 10 kHz. Performance is about the same for both 8- and 16-ohm loads.

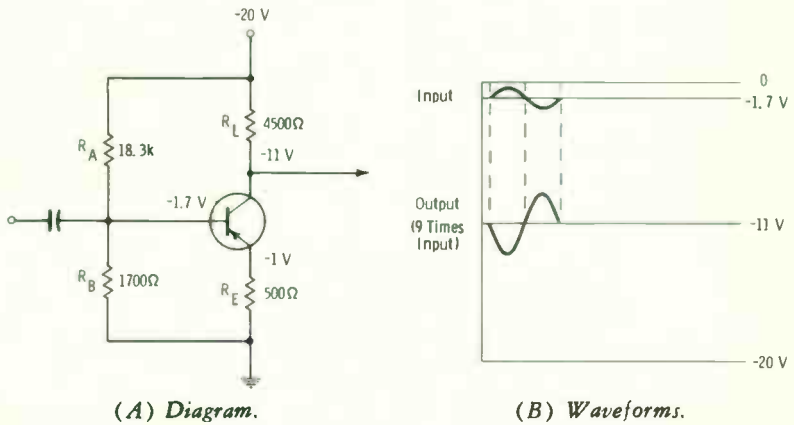
This amplifier is capable of about 8 watts of continuous output power with 1-volt-rms input, or 10 watts of music power into 8 or 16 ohms when used with the power supply of Fig. 6-8B. This power supply has diode decoupling, which provides excellent separation (80 dB) between the two stereo amplifier channels. (Power supplies will be covered in greater detail in Chapter 16.)

Power transistors Q4 and Q5 should each be mounted on an adequate heat radiator, such as is used for the output in an automobile radio, or mounted on a $3'' \times 3'' \times \frac{3}{32}''$ aluminum plate that is insulated from the chassis.

6-4. LARGE-SIGNAL AMPLIFIERS, FEEDBACK PAIRS, AND BOOTSTRAPPING

Let us examine two basic ways of handling large signal waveforms. The same function will occur, but with two distinct and specific interpretations in circuit analysis.

See Fig. 6-9A. The current in R_A and R_B is 20 V/20k = 1 mA. The drop across R_B is (1 mA) (1700 ohms) = 1.7 volts, so the base voltage is −1.7 volts. Assume the transistor is a silicon type; the emitter voltage will be about −1 volt. Then the emitter current is about 1/500 = 2 mA. If 2 mA in the collector is assumed, the voltage drop across R_L is (2 mA) (4500) = 9 volts, so the collector voltage is −11 volts.



(*A*) *Diagram.* (*B*) *Waveforms.*

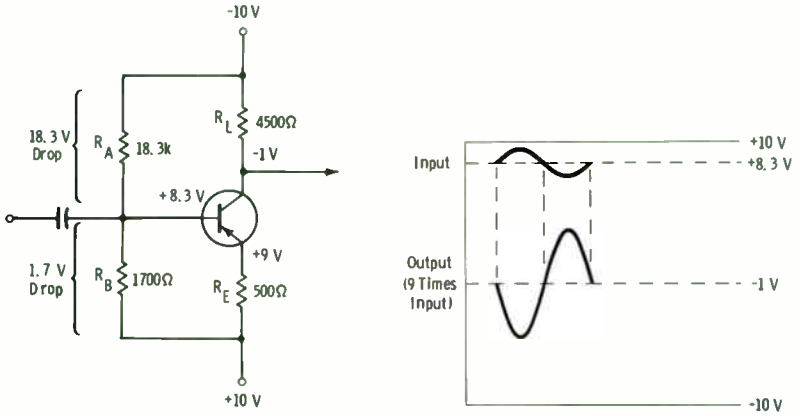
Fig. 6-9. Common-emitter amplifier with single voltage source.

Fig. 6-9B shows the input signal superimposed on the −1.7-volt base bias, and the output signal superimposed on the −11-volt collector voltage. Thus with a −20-volt supply, the output signal can swing very close to plus and minus 10 volts from the quiescent point, for a peak-to-peak swing of just under 20 volts. (The voltage gain of the stage is approximately $R_L/R_E = 4500/500 = 9$. Therefore the output in Fig. 6-9B is 9 times the input.)

Fig. 6-10 shows how the same large signal swing can be accommodated with the use of two ten-volt supplies. For comparison, component values the same as those in Fig. 6-9 are used. Resistors R_A and R_B now see a difference of voltage equal to 20 volts, so the current through them is:

$$I = 20/20k = 1\ mA$$

The voltage drop across R_B is (1 mA) (1700 ohms) = 1.7 volts. So V_B is 10 − 1.7 = +8.3 volts. The remaining 18.3 volts is dropped across R_A.



(A) Diagram. *(B) Waveforms.*

Fig. 6-10. Common-emitter amplifier with dual voltage sources.

Since the transistor is silicon, the emitter will be at about +9 volts. Note that this is just a 1-volt drop from the emitter supply of +10 volts. So the emitter current is:

$$I_E = \frac{1}{500} = 2 \text{ mA}$$

With 2 mA in the collector assumed, the drop across R_L is (2 mA) (4500) = 9 volts, so V_C is −1 volt.

Note that the collector is at −10 volts relative to the emitter, which is the "center" operating point ($\frac{1}{2}V_{CC}$) for a linear amplifier. But also note the extreme difference in dc voltages to ground between Fig. 6-9 and Fig. 6-10. The waveforms in Fig. 6-10B show how the same peak-to-

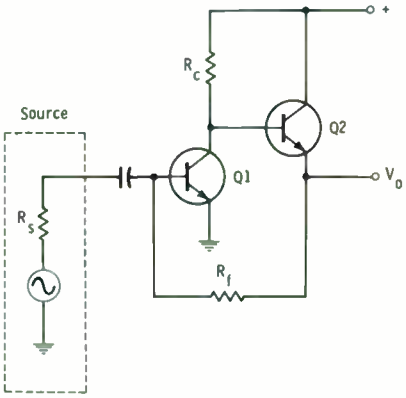


Fig. 6-11. Diagram of current feedback pair.

peak capability exists for this circuit as for the circuit of Fig. 6-9, with the different dc axis of measurment. (Again, $A_v = R_L/R_E = 9$.)

Due to transistor and circuit capacitance effects, the lower we make input and output impedances, the higher the frequency response can be made, but at the expense of gain. When low impedances are obtained by feedback, we have the additional factor of signal inverse feedback to improve frequency response and signal linearity. The basic circuit of Fig. 6-11 shows feedback resistor R_f connected in a circuit known as a "feedback pair."

The feedback pair is very common (for one example) in modern color cameras, particularly as a line driver for a 50- or 75-ohm line. Fig. 6-12 shows a typical circuit. The following relationships may be used in the analysis of this circuit:

$$Z_{in} = \frac{R_f}{A_v + 1} \qquad \text{(Eq. 6-4)}$$

$$A_v = \frac{R_f}{R_S} \qquad \text{(Eq. 6-5)}$$

$$R_f = A_v R_S \qquad \text{(Eq. 6-6)}$$

For the analysis, assume the transistors are silicon. Since this is so, and the emitter of Q1 is grounded, we know that the Q1 base can be assumed to be at about +0.7 volt relative to ground. The difference between the −10-volt supply and the +0.7 volt junction is 10.7 volts, so the current in R1 is 10.7/6200 = 1.73 mA.

This same 1.73 mA is present in the emitter return of Q2, so it is present in the 2500-ohm feedback resistor, R_f. Consequently, there is a voltage of (1.73)(2500) = 4.3 volts across R_f, with the end toward Q2 more positive. Adding the starting point of 0.7 volt, we expect a Q2 emitter voltage of +0.7 +4.3 = +5 volts.

Since the Q2 emitter voltage is +5 volts, we should measure about +5.7 volts at the Q2 base. The same voltage appears at the Q1 collector. The voltage drop across R_c is 10 − 5.7 = 4.3 volts, and the Q1 collector current is 4.3/860 = 5 mA. So now we know that the Q1 collector current is about 5 mA, and the Q2 current is about 1.73 mA.

If the sending (source) impedance is 500 ohms, the expected voltage amplification (by Equation 6-5) is about 2500/500 = 5. The output signal current is superimposed on the 1.73 mA quiescent current, so 2 × 1.73 = 3.46 mA peak-to-peak signal swing is the maximum available without clipping. If R_L is 500 ohms, this current swing results in a signal voltage of 3.46 × 500 = 1.73 volts peak-to-peak. If R_L is 50 ohms, the peak-to-peak signal swing is 3.46 × 50 = 0.173 volt.

Fig. 6-13 shows the same circuit with modifications that drastically affect its operation. The Q1 collector load has been split into two equal resistors that total the original 860 ohms. This arrangement provides a tap

for the bootstrap capacitor, which adds positive feedback to overcome the signal loss resulting from negative feedback through R_f. Since we now obviously have a greater signal current swing because of the bootstrapping, an additional current must be supplied to the Q2 emitter. This is done through R2, a 250-ohm resistor. The difference between the −10-volt supply voltage and the +5 volts at the Q2 emitter is +15 volts. Therefore an additional $15/250 = 60$ mA is added to the already existing 1.73 mA in Q2 for a total of about 62 mA of quiescent operating current. The output signal current can now swing ±62 mA for a peak-to-peak swing of approximately 120 mA without clipping. This current swing develops a signal of 6 volts peak-to-peak across a 50-ohm load, or an output capability over 30 times greater than in the circuit of Fig. 6-12. Please note that there is no difference in quiescent voltage readings to ground at the transistor junctions in the two circuits.

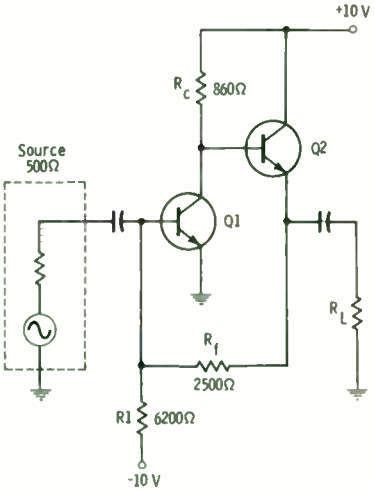


Fig. 6-12. Diagram of typical feedback pair.

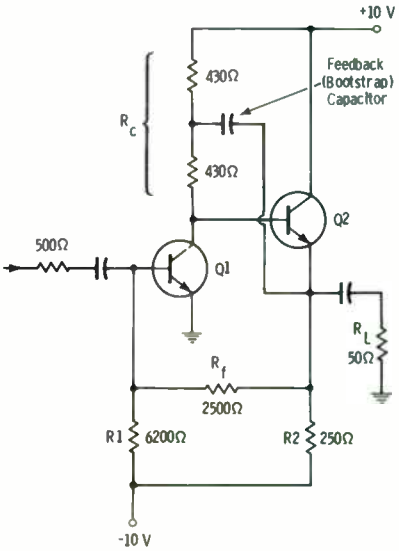


Fig. 6-13. Baatstrapped feedback pair.

There are two fundamental tests in troubleshooting these circuits; both can be done quickly with the oscilloscope. One example will suffice: Assume we are "scoping" the Q2 emitter. First, we know the dc operating point will be around +5 volts. Calibrate the scope for a 1 volt/cm sensitivity, and position the trace at the bottom graticule line (with the probe touching ground and the scope set on dc input). Then apply the probe to the Q2 emitter and check to see that the trace moves upward 5 cm. In the case of the circuit in Fig. 6-12, the signal superimposed on the scope trace

will be very small, so to check the peak-to-peak signal swing go to ac operation and increase the scope gain. We now have the complete functional story of conditions at the emitter terminal. In the case of the circuit in Fig. 6-13, we would likely observe the signal swing at the same time we check the dc level; this swing should have the +5-volt level as its axis.

EXERCISES

Q6-1. In Fig. 6-14,
(A) What is the quiescent I_C?
(B) What is Z_{in}?
(C) What is the approximate load impedance?
(D) What is the approximate voltage gain?

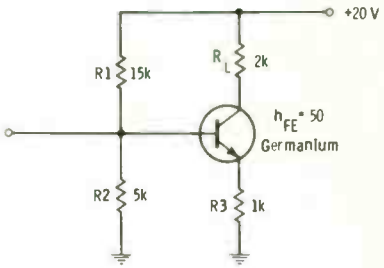


Fig. 6-14. Circuit for questions Q6-1 and Q6-2.

Q6-2. Compute the answer to Q6-1D in terms of g_m.

Q6-3. Make your dc analysis of the circuit in Fig. 6-15. What voltage would you expect to read at the bases of Q1 and Q2, the collectors of Q1 and Q2, and the emitter of Q1? Assume silicon transistors.

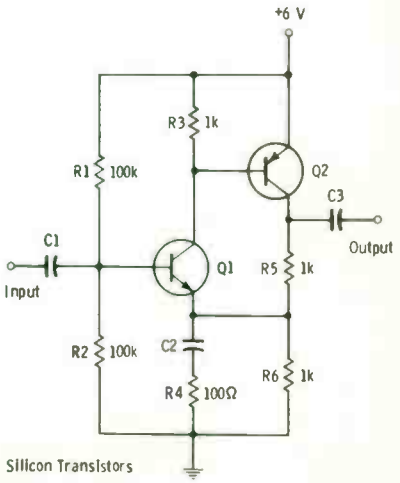


Fig. 6-15. Circuit for question Q6-3.

Q6-4. Suppose you have the circuit of Fig. 6-12, except that R1 is 10k and R_f is 3k. What dc voltages would you expect to measure at the base and collector of Q1, and the base and emitter of Q2 (measuring with respect to ground)? The transistors are silicon.

Q6-5. With the circuit mentioned above in question Q6-4, what would be the maximum peak-to-peak signal voltage developed in a 75-ohm load?

CHAPTER 7

Practice Problems in Solid-State Amplifier Circuitry

This chapter offers practice problems in solid-state amplifier circuit analysis and basic design. It covers the types of circuitry most frequently encountered in practice. (NOTE: Chapter 11 will cover practice problems in pulse circuitry.)

If the student prefers, he can follow these problems strictly "on paper." But it will be of advantage to actually construct the circuits on convenient "pegboard" bases with spring-type solderless connectors. Following is the basic list of materials for both this chapter and Chapter 11:

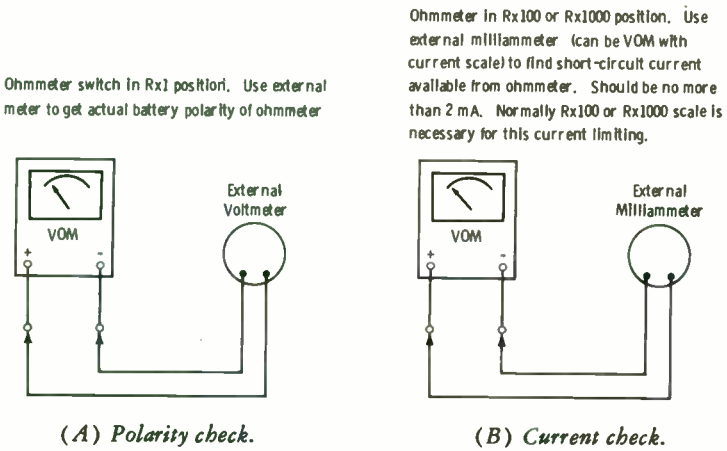
Vectorbord (or equivalent) prepunched terminal board with 0.093" holes
Vector T32A (or equivalent) spring-type push-in terminals
Transistor, type 2N404A (as typical switch); used in Chapter 11
Transistor, type 2N406 (as typical audio-frequency amplifier)
Transistor, type 2N1143 (as typical video amplifier)
Transistor, type 2N2219 (two)
Assortment of 1/2-watt resistors and low-voltage capacitors
RCA VS-301 battery (3-6-9 volt) or equivalent
RCA VS-036 battery (1.5-volt D cell) or equivalent
Battery holders for D cells, one single-cell and two two-cell-series

By actually doing these practice problems, the student will gain familiarity and experience in practical design and circuit analysis. His study should be quite effective if he can use his station or shop equipment (VOM, oscilloscope, etc.) and can benefit by "classroom" practice (and discussion) of the problems involved.

7-1. TRANSISTOR IDENTIFICATION AND BASIC TESTING

Solutions and comments for each of the following practice problems are given in Section 7-3. Before proceeding, review Section 2-5 on the ohmmeter technique, and Section 4-7 on transistor lead identification.

See Fig. 7-1A. This illustration shows the first step to be taken before going ahead. Fig. 7-1B represents the second step in knowing the VOM as applied to transistor testing. Never use the R×1 scale of the ohmmeter in checking junctions, because it can deliver a considerable amount of power which can damage small junctions. In most cases, we can use the R×10 scale without worry, but even then some of the smaller and more delicate junctions can be damaged. So do this (as shown by Fig. 7-1B):



(*A*) *Polarity check.* (*B*) *Current check.*

Fig. 7-1. Preporation for ohmmeter tests of transistors.

Place an external ammeter across the VOM leads, and find a scale which limits the maximum short-circuit current to 2 mA. This will normally be the R×100 scale, or in some cases the R×1000 scale. We can safely use the 2-mA-limited source without worry about damage to the tiniest transistor. The R×1 scale can be used for the larger power transistors, but even here the R×10 scale is best.

NOTE: In all tests involving the ohmmeter, remember that the indicated polarity is battery polarity on the test leads. This does not necessarily mean that the red lead is positive and the black lead is negative! Know your VOM.

Obviously, it is possible to say, "Resistance should be 'high' with one polarity and 'low' with the opposite polarity." But it is also convenient to tell whether the transistor is pnp or npn without looking at specification sheets.

Problem 1: Testing Transistor Forward Resistance

A simple technique for checking forward resistance is shown in Fig. 7-2. The transistor is pnp, so to read forward resistance, Step 1 is to connect the ohmmeter with the plus lead to the emitter and the minus lead to the base. Read the forward resistance. A high reading indicates an open; a zero reading indicates a short. A normal transistor resistance reading in the forward direction will vary somewhat with the ohmmeter range required (voltage applied), but in general it should measure below 500 ohms. Step 2 is to read the forward resistance between base and collector, as shown. The same conditions apply. For an npn transistor, reverse the ohmmeter leads.

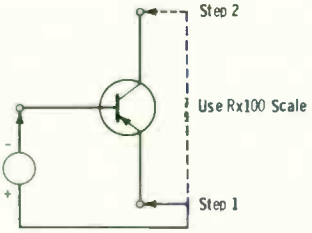


Fig. 7-2. Measurement of forward resistance.

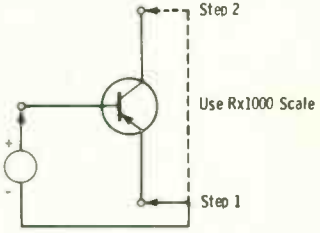


Fig. 7-3. Measurement of reverse resistance.

Problem 2: Testing Reverse Resistance as an Indication of Leakage

Step 1 (Fig. 7-3) is to reverse-bias the emitter-base junction with the ohmmeter. To reverse-bias the pnp transistor, the base should be positive relative to the emitter. Read the resistance using the R×1000 scale. Low- and medium-power transistors should measure over 200k or so; if they do not, more accurate checks should be made as shown later. Step 2 is to measure the reverse resistance of the base-collector junction. The same conditions prevail. For an npn transistor, reverse the ohmmeter leads.

Note that the tests of problems 1 and 2 can be carried out by simply reversing the meter polarity during Step 1 and also during Step 2. This reversal could be very conveniently done by throwing the polarity-reversal switch on a meter so equipped, or by reversing the leads of the ohmmeter. The reading should be lower in the forward direction than in the reverse direction. For power transistors, the reverse resistance can be rather low—in the order of 1000 ohms or so in some cases.

Problem 3: More Accurate Leakage Test

Leakage current (I_{CBO}, or I_{CO}) is the dc collector current present when a specified reverse-bias voltage is applied from collector to base (emitter open). Make the hookup shown in Fig. 7-4 for Step 1. Low- and medium-power transistors should show less than 15 μA at normal room tempera-

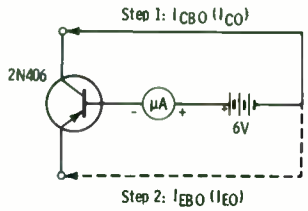


Fig. 7-4. More accurate leakage test for transistors.

R_C	I_{CO}
R_C=0	
R_C=10k	
R_C=100k	

(A)

I_{CO}	I_{CEO}	h_{FE}

From Fig. 7-5A, Value for R_C=0

(B)

Fig. 7-5. Tabulation of measurement results.

ture of 25°C (about 77°F). In germanium transistors, the leakage current can double for each 10°C temperature rise.

Take the reading for I_{CO} and record it in the table of Fig. 7-5A for $R_c = 0$ (no resistance in collector circuit.) Now hold your fingers tightly around the transistor for at least two minutes. Has the leakage current decreased or increased?

Now do Step 2 (Fig. 7-4) to measure I_{EBO}, or I_{EO}. This is the dc current present when a specified reverse-bias voltage is applied from emitter to base (collector open). The same conditions apply as for I_{CO}.

NOTE: The leakage current for a power transistor can range up to 100 μA, or slightly more, at room temperature.

Now refer to Fig. 7-6, Step 1. What effect does the insertion of a 10k resistor have on I_{CO}? Record the reading in Fig. 7-5A. What effect does the insertion of a 100k resistor (Fig. 7-6, Step 2) have on I_{CO}? Record the reading in Fig. 7-5A.

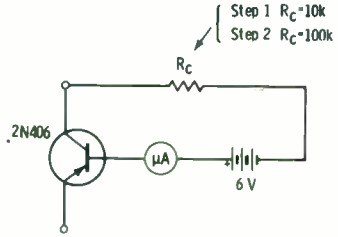


Fig 7-6. Test for effect of collector resistor on leakage current.

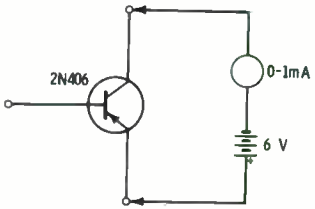
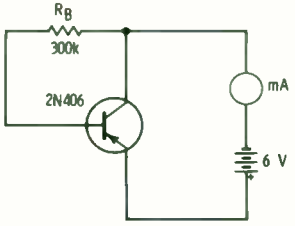


Fig. 7-7. Measurement of I_{CEO} in a transistor.

Make the hookup of Fig. 7-7 for measurement of I_{CEO}. This is the dc current present when a specified voltage is applied from collector to emitter (base open) with such polarity that the collector-base junction is reverse-biased. For a pnp transistor, the collector is negative relative to the base.



I_C	
DC Beta (h_{FE})	

(A) Circuit diagram. *(B) Table for results.*

Fig. 7-8. Determination of dc beta.

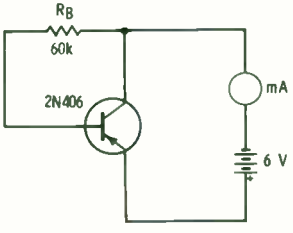
Note that here we are using a milliammeter rather than a microammeter; a meter with a 1-mA full-scale capability should indicate the maximum we will measure for low- and medium-power transistors (up to 1 watt). We are proving here a point brought out earlier: I_{CO} is amplified by the dc beta of the transistor. That is, the leakage current between base and collector is amplified by β so that the leakage current between emitter and collector is β times I_{CO}. Record the reading of I_{CEO} in Fig. 7-5B. How do we know what the approximate dc beta (h_{FE}) of this transistor is?

It will be quite educational, while reading this current, to repeat the finger test: Hold your fingers tightly around the transistor, and watch the meter.

Problem 4: Determination of Beta

Make the hookup of Fig. 7-8A by adding a 300k resistor (R_B) to introduce a small base current. Record the collector-current reading in the table of Fig. 7-8B. Now what is the dc beta?

Next substitute a 60k base-supply resistor (Fig. 7-9A), and fill in the table of Fig. 7-9B. Wait for the circuit to stabilize. (Why?) Our previous measurements of beta were taken in terms of leakage-current



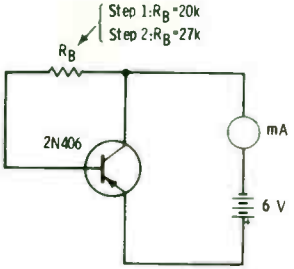
I_C With R_B=300k	
I_C With R_B=60k	
DC Beta (h_{FE})	
AC Beta (h_{fe})	

From Fig. 7-8B

This Will be Wrong. (Why?)

(A) Circuit diagram. *(B) Table for results.*

Fig. 7-9. Inaccurate determination of ac beta.



(*A*) *Circuit diagram.*

I_C With R_B = 20k	
h_{FE} (Step 1)	
h_{fe} (Step 2)	

(*B*) *Table for results.*

Fig. 7-10. Determination of ac beta.

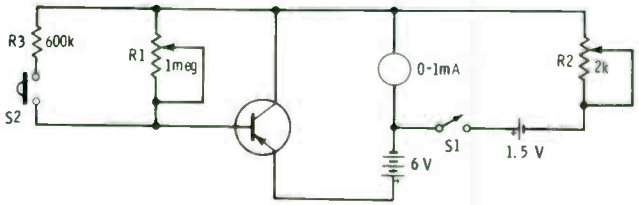
limitations. Do the dc and ac beta values increase or decrease with higher average I_C? Why will the computation of ac beta (h_{fe}) be wrong in this example?

Now go to Fig. 7-10A, Step 1. Make $R_B = 20k$ and measure I_C (record this value in Fig. 7-10B). Compute h_{FE} for this step. For Step 2, make $R_B = 27k$ and then compute h_{fe} (ac beta). Why is this value accurate, whereas the computation in Fig. 7-9B was wrong? With $R_B = 20k$, repeat the finger test by holding the transistor tightly with your fingers. What happens this time?

Fig. 7-11 shows a "direct-reading" beta checker to double-check the h_{FE} measurements for low- and medium-power transistors (up to 1 watt). Explain how this circuit provides a direct reading of beta. What else should be specified when we give a reading for h_{FE} or h_{fe}?

7-2. RULE-OF-THUMB DESIGN AND CIRCUIT ANALYSIS

This section will introduce rule-of-thumb design procedures for basic small-signal linear amplifiers. This type of design work also can simplify



1. S1 & S2 open. Adjust R1 for 1-mA reading on meter.
2. Close S1. Adjust R2 to balance meter to zero.
3. Close S2 (adds 10-μA base current through R3).
4. Read beta directly on meter.

For npn, reverse all polarities

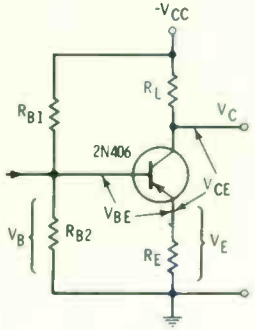
Fig. 7-11. Diagram of direct-reading beta checker.

understanding and analysis of circuits for general interpretation and troubleshooting. Solutions and discussions are contained in Section 7-4.

The student will be shown how to approach proper biasing of transistors with the simple expedient of Ohm's law. He will work out circuit component values by using ratios of circuit currents (or voltages) to "standards" of the transistor itself, as required for good circuit stability.

Problem 1: Amplifier with Series Feedback

Study the circuit and the data given in Fig. 7-12. The information all should be evident from previous studies, except that it has not been required to apply such knowledge to designing a circuit.



Constants: V_{BE}=0.2 V (Germanium)

V_{BE}=0.7 V (Silicon)

Design Parameters:

1. Specify I_E from signal mode.
2. $I_B = I_E/h_{FE} - I_{CO}$ ← Can be ignored for room temperature.
3. Make $V_{CE} = 1/2 (V_{CC} - V_E)$
4. $V_B = V_E + V_{BE}$
5. Make current in R_{B2} at least 5 times base current (I_B).
6. Make V_E at least 5 times V_{BE}.

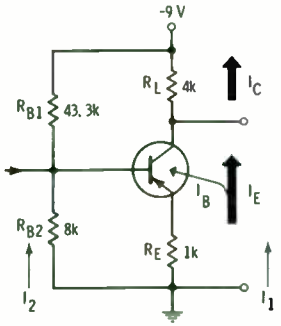
Fig. 7-12. Design parameters for amplifier with series feedback.

Start with just two given parameters: (A) $V_{CC} = -9$ volts, and (B) $I_E = 1$ mA. (This current is typical for the small-signal mode as used for very low-level [input] stages with the 2N406. When the transistor is used as a driver for a high-level stage, the emitter current can range up to 40 mA or more.) Now follow these steps:

1. $I_B = I_E/h_{FE} = 0.001/35 = 30\mu A$ (approx). (The dc beta of 35 is as listed in "typical" specification sheets for the 2N406 at 1-mA collector current.)
2. Since the 2N406 is germanium, $V_{BE} = -0.2$ V (pnp).
3. Now, since $I_E R_E$ (a measure of voltage at the emitter) should be at least 5 times V_{BE}, then $I_E R_E = (5)(-0.2) = -1$ volt. This says the emitter voltage (V_E) should be -1 volt to ground.
4. So V_B (base voltage to ground) should be -1.2 volts (base negative with respect to emitter for pnp).
5. Also, V_{CE} should be $\frac{1}{2}(9-1) = 4$ volts. Therefore, the 1-mA collector current should drop 4 volts across R_L, so:
6. $R_L = V/I = 4/0.001 = 4000$ ohms. So we have a -1-volt V_E and a V_{CE} of another -4 volts, or -5 volts from collector to ground (V_C).

7. $R_E = 1/0.001 = 1000$ ohms.
8. The current in R_{B2} should be five times I_B, or $(5)(30\ \mu A) = 150\ \mu A$. So:
9. $R_{B2} = 1.2/0.00015 = 8000$ ohms.
10. R_{B1} must drop the -9-volt V_{CC} to the -1.2 volt V_B. The drop required is $9 - 1.2 = 7.8$ volts. This resistor handles the voltage-divider current and I_B, or 30 μA plus 150 $\mu A = 180\ \mu A$. So: $R_{B1} = 7.8/0.00018 = 43.3$k.

We now have the circuit of Fig. 7-13. This is the "design-center" circuit just put together on the basis of "minimum" stability-factor requirements. It should be quite stable over normal operating temperatures.



Derived Relationships:

$V_B = I_E R_E + V_{BE}$

$R_{B2} = V_B / I_2$, and $I_2 =$ 5 times I_B (min)

$R_{B1} = (V_{CC} - V_B)/(I_2 + I_B)$

$R_E = \frac{V_E \text{ Desired (5 Times } V_{BE} \text{ Min)}}{I_E \text{ Desired (From Signal Mode)}}$

$R_L = (V_{CC} - V_{CE})/I_E - R_E$

Fig. 7-13. Design formulas for amplifier with series feedback.

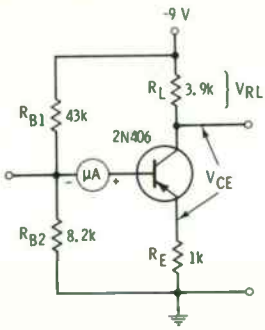
Note in the data accompanying Fig. 7-13 how we can derive the required relationships (formulas) for this design procedure. Base voltage V_B must be the total of emitter voltage $I_E R_E$ and the necessary forward bias, V_{BE}. The value of R_{B2} must be the required base voltage divided by the current through R_{B2}, and this current must be a minimum of five times the base current for good stability. The rest of the derivations should be self-evident. Why is the voltage gain of this circuit practically independent of variations in transistor beta?

Make the hookup in Fig. 7-14A with resistors which have EIA values as close as possible to the designed values of Fig. 7-13. Fill in the table of Fig. 7-14B. What tolerance would be expected in the meter reading?

How could we drastically increase the voltage amplification in this circuit? What signal-amplitude limitations do we need to consider if we do this?

Problem 2: Amplifier With Shunt Feedback

Now suppose the circuit of Fig. 7-14 is modified as shown in Fig. 7-15. What should be the value of R_f? What happens to the input impedance and to the voltage gain?



(A) *Diagram with parts values.*

V_{RL}	
I_C	
I_B	
h_{FE}	
V_{CE}	
P_C	
A_V	

(B) *Table for operating parameters.*

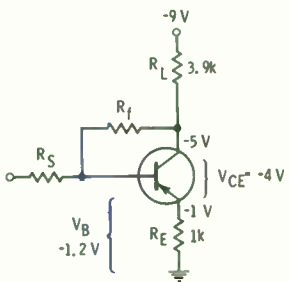
Fig. 7-14. Result of rule-of-thumb design of amplifier with series feedback.

Problem 3: Amplifier With Dual Power Sources

The circuit of Fig. 7-16A is one found quite often in modern solid-state circuitry. Note that the emitter and collector are now supplied from separate power sources. Let us go through a rule-of-thumb design procedure for this circuit, with the following assumptions: V_{CC} is plus and minus 9 volts, the quiescent operating current is to be 1 mA, and the transistor is a germanium type with a minimum β of 20.

First of all, V_{CE} should be about one-half the total supply voltage. In this case, the total V_{CC} is 18 volts, so V_{CE} should be 9 volts. We know the $I_E R_E$ product should be at least 5 times the V_{BE} of 0.2 volt (germanium transistor); therefore $I_E R_E$ is 1 volt and V_E is +8 volts. Then the collector voltage is $8 - 9 = -1$ volt. The base voltage is $8 - 0.2 = +7.8$ volts.

We want to drop 1 volt across R_E as indicated, so $R_E = 1/0.001 = 1000$ ohms. Since R_L should drop 8 volts with a current of 1 mA, $R_L = 8/1$ mA $= 8000$ ohms. The maximum value of I_B is $I_C/\beta_{min} = 0.001/20 = 0.05$ mA, or 50 μA.



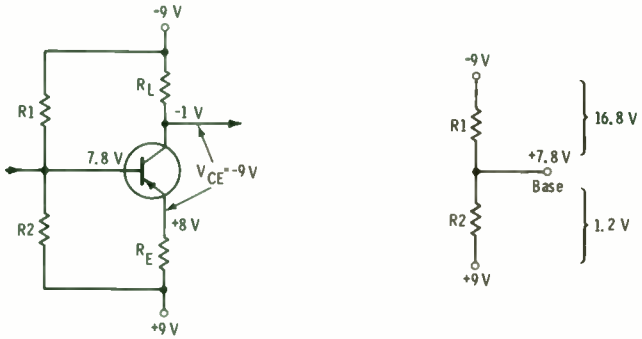
I_E=1 mA

$I_B = I_E/h_{FE} = 0.001/35 = 30$ μA

R_L =3900 Ohms

R_f =?

Fig. 7-15. Circuit with shunt feedback.



(*A*) *Schematic.* (*B*) *Bias network.*

Fig. 7-16. Amplifier with two dc voltage sources.

Now here is where our rule-of-thumb procedure differs slightly from previous design. Base-bias resistors R1 and R2 should carry at least 10 times the maximum quiescent base current. In this case, the current would be (10)(50 μA) = 500 μA, or 0.5 mA. So, R2 = 1.2 V/0.5 mA = 2400 ohms. Where does the 1.2 volt come from? We know that the emitter must be positive relative to the base, so the base supply must provide 0.2 volt more than the 1-volt emitter drop. See Fig. 7-16B. The resistance of R1 (again see Fig. 7-16B) is 16.8 V/0.5 mA = 33.6k.

The circuit values are now:

$R_L = 8k$
$R_E = 1k$
$R1 = 33.6k$
$R2 = 2.4k$
$I_B = 50\ \mu A$
$I_C = I_E$ (approx) = 1 mA
$A_v = R_L/R_E$ (approx) = 8000/1000 = 8

Assume the input signal swing is 5 μA (pk-pk). What is the input signal in millivolts, and on what dc level is this signal superimposed? What is the peak-to-peak output voltage, and what is the dc axis of this output signal? What, if any, is the advantage of this circuit over that of Fig. 7-13?

Problem 4: Feedback Pair

The feedback pair of Fig. 7-17 is assuming universal acceptance as a stable, wideband amplifier because of its inherent dc and ac stability. In analyzing this circuit, we must consider the sending and receiving impedances in determining the operating parameters. Since silicon transistors

have become most popularly used here, we have indicated this transistor type for this circuit. From the parameters listed in the figure, follow through the design procedure:

Step 1. Since the transistors are silicon, we know immediately (since the Q1 emitter is grounded) that $V_{B1} = +0.7$ volt (npn transistor).

Step 2. We need a voltage gain of 5. Since $A_v = R_f/R_s$, then $R_f = (A_v)(R_s) = (5)(500) = 2500$ ohms.

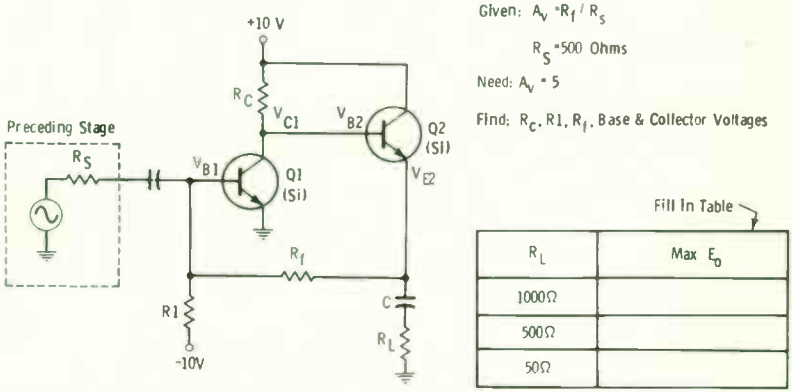


Fig. 7-17. Design of feedback pair.

Step 3. Follow rule-of-thumb procedure, and fix the Q2 emitter so that V_{CE} for Q2 is +5 volts (one-half V_{CC} as center of operating range).

Step 4. The "bottom" end of R_f is at +0.7 volt, and the emitter end must be at +5 volts. Find the required current: $I = V/R = 4.3/2500 = 1.72$ mA. (The difference between 0.7 volt and 5 volts is 4.3 volts.)

Step 5. Find the value of R1. This same 1.72 mA must flow through R1, and it must result in +0.7 volt at the junction of R1 and R_f (base of Q1), or a drop of 10.7 volts across R1. So: $R1 = 10.7/1.72 = 6200$ ohms.

Step 6. Find the Q1 collector voltage. This is the same as the Q2 base voltage, which must be +0.7 relative to the Q2 emitter, or +5.7 volts.

Step 7. Find the Q1 collector current. This will be the hardest quantity to visualize. Here is the rule-of-thumb approach: The Q2 emitter current is 1.72 mA. This means that if the transistor pair were operated in the large-signal mode, the maximum signal current passed to R_L would be plus and minus 1.72 mA. Small-signal-mode design is the same in the interest of maximum transfer linearity.

Now we realize that the product of the Q1 base current and the current gain of the pair must support the current in the Q2 emitter, or $(2)(1.72) = 3.44$ mA peak-to-peak. As a rule of thumb, we can assume the Q1 collector current will be three times the quiescent Q2 emitter

current, or: $(3)(1.72) = 5.16$ mA. (Say 5 mA for simplicity in rule-of-thumb design.)

In practice, we can see that the current gain is not dependent upon the beta of Q1 or Q2. As current gain increases, the feedback current to the base of Q1 subtracts from the input current, and the voltage gain reduces.

Step 8. Find the value of R_c. The 5 mA must drop the +10 volts of the supply to the +5.7 volts at the Q2 base, or: $10 - 5.7 = 4.3$ volts. Then $R_c = V/I = 4.3/0.005 = 860$ ohms.

Now fill in the table of Fig. 7-17.

7-3. SOLUTIONS AND COMMENTS, PRACTICE PROBLEMS ON TRANSISTOR IDENTIFICATION AND TESTING

Fig. 7-1 should be self-explanatory. The important point, since newer high-frequency types of transistors have interchanged base and emitter leads, is to have a transistor reference guide. The user will find a column designated "Physical Outline," "Terminal Arrangement," or "Drawing Number" which will show the terminal arrangement.

Problems 1 and 2: Testing Forward and Reverse Resistance

The tests relating to Figs. 7-2 and 7-3 should be self-explanatory. We can also answer the question, "Pnp or npn?" When we know the ohmmeter battery polarity, the transistor is npn if the low resistance reading occurs with plus on base and minus on emitter; the reverse is true for pnp types. (Again, when in doubt, use reference data to identify the base and emitter leads.) Obviously, in any case we should get a low resistance with one polarity and a high resistance with reversed polarity if the transistor is good. Measurement from emitter to collector should show "high" resistance with any polarity.

Problem 3: More Accurate Leakage Test

A typical value of I_{CO} for the type 2N406 at room temperature is 6 μA. Holding your fingers around the transistor will prove how leakage current increases with temperature. The amount of increase (as well as the original leakage current) will depend on how high the room temperature is at the time; in a "cold" room, the increases will be more than in a "hot" room. In a room at 70°F, a typical increase from body heat is around 4μA, bringing I_{CO} up to 10 μA. Leakage current in many transistors doubles for every rise in temperature of ten degrees centigrade. We will get approximately the same reading for I_{EO} as for I_{CO}.

In the test of Fig. 7-6, there should be no change. Even a 100k resistance is small compared to the internal collector-junction resistance. This result provides a practical illustration of the "constant-current" principle of the collector junction.

For Fig. 7-7, a typical value of I_{CEO} for the 2N406 is 0.2 mA, or 200 μA. Since this current is beta times I_{CO}, the dc β (h_{FE}) is:

$$h_{FE} = \frac{I_{CEO}}{I_{CO}} = \frac{200}{6} = 33+$$

This result means that the very small leakage current in the base is amplified slightly more than 33 times by the dc beta of the transistor. With the base open (zero voltage), the emitter-base junction in this hookup is forward biased, and the collector-base junction is reversed biased. Conditions are such that the transistor should amplify, and it does —in this case, it amplifies the small collector-base leakage current.

Remember that beta is the short-circuit current amplification; the "short circuit" in this case is the very low internal impedance of the milliammeter and battery.

Problem 4: Determination of Beta

In the circuit of Fig. 7-8, with a small amount of base current (I_B) introduced, a typical collector current (I_C) for the 2N406 is 0.8 mA, or 800 μA. Now what is the base current? It is quite simply:

$$I = \frac{V}{R_B} = \frac{6}{300k} = 20\mu A$$

So: $h_{FE} = 800/20 = 40$

In Fig. 7-9, we have increased I_B by lowering the value of bias-supply resistor R_B. You must wait for the circuit to stabilize because heating of the junction will rise due to the larger power dissipation. A typical I_C for a 2N406 in this circuit is 5.6 mA, or 5600 μA. $I_B = 6/60k = 100$ μA. So:

$$h_{FE} = \frac{5600}{100} = 56$$

It is readily observed that beta in a common-emitter circuit increases as collector current increases. (Review Section 4-5.)

Now what about ac beta (h_{fe})? We know that:

$$h_{fe} = \frac{\Delta I_c}{\Delta I_b}$$

That is, ac beta is the ratio of a change in collector current to the change in base current producing it.

What we have done in going from Fig. 7-8A to Fig. 7-9A is to increase I_B by 5 times (a change from 20 μA to 100 μA of base current). So, using the only figures we have to compute h_{fe}, we get:

$$h_{fe} = \frac{5600 - 800}{100 - 20} = \frac{4800}{80} = 60$$

This result indicates that the ac beta is greater than the highest dc beta. Why is the computation in error?

First of all we know that h_{fe} will be less than h_{FE}. The above measurement is meaningless because it has not simulated actual operating conditions. The signal swing on the base (for linear amplification) cannot be five times the quiescent base-current value! The signal-current swing will normally be less than ⅓ the quiescent base current, in most cases $\frac{1}{10}$ or less. So now go to Fig. 7-10.

For Step 1 of Fig. 7-10A, $I_B = 6/20k = 300\ \mu A$. A typical I_C for $I_B = 300\ \mu A$ is 20 mA, or 20,000 μA. So this $h_{FE} = 20{,}000/300 = 66$, proving again that beta has increased with higher I_C.

For Step 2, $R_B = 27k$, $I_B = 6/27k = 222\ \mu A$, less than a ⅓ reduction in I_B. A typical I_C (for the 2N406) is now 16 mA, or 16,000 μA. So the ac beta is:

$$h_{fe} = \frac{20{,}000 - 16{,}000}{300 - 222} = \frac{4000}{78} = 51$$

This is a realistic computation for h_{fe}, since it more nearly simulates actual operating conditions. In commercial ac-beta checkers, I_B is normally *reduced* by a factor of less than ⅓, usually by $\frac{1}{10}$ or less, to obtain the measurement.

Now what about the finger (heat) test? With a transistor running near the maximum power-dissipation rating, your fingers actually provide a "heat sink," and I_C falls off! Here we begin to see the relativity factor of solid-state design.

Incidentally, the maximum power-dissipation rating for a 2N406 is 150 mW at 25°C. What is the power dissipation with the 20k base-bias resistor above? The power is quite simply the collector voltage times the collector current, or $6 \times 0.02 = 120$ mW. This is a factor we must always consider in any experimental or design work we do. Always stay below the maximum power dissipation rating.

In Fig. 7-11, with both switches open, adjustment of R1 provides the base current necessary to result in 1 mA of collector current. Closure of S1 makes possible adjustment of R2 so that the resulting opposing current can zero the meter for reference. Thus an introduction of more base current will deflect the meter upward from this reference. In this example, more base current is supplied through R3 (600k) by pushing S2. The 600k resistor will supply an additional 10 μA of base current ($6/600k = 10\ \mu A$).

If, for example, the beta of the transistor is 60, the 10μA base current would result in $60 \times 10 = 600\ \mu A$, or 0.6 mA, of collector current. So a $0 - 100$ scale used in place of the $0 - 1$ mA scale would be direct-reading for beta measurement. The 0.6-mA reading becomes a direct reading of 60.

For an h_{FE} reading to be meaningful, we must specify the collector voltage and the collector current. (The product specifies power dissipation, hence heating effect.) For h_{fe} we must specify the operating parameters as in the discussion for Fig. 7-10. In actual operating conditions considering the signal to be used, the signal frequency must be specified. Always remember the effect of temperature. Junction currents rise and beta increases with an increase in temperature.

7-4. SOLUTIONS AND COMMENTS, RULE-OF-THUMB DESIGN AND ANALYSIS

The solutions and comments in this section are for the problems given in Section 7-2 on rule-of-thumb design and analysis.

Problem 1: Amplifier with Series Feedback

The discussion relative to Fig. 7-12 should be self-explanatory. The constants and design parameters were all explained in previous study; we are now applying what we have learned to simplified design of a circuit.

The voltage gain of the circuit in Fig. 7-13 is practically independent of transistor beta because of the base "swamping" resistor, R_{B2} and the self-biasing action of R_E. If beta increases, the increased current through R_E biases the base-emitter junction inversely to reduce gain. Effects of changes in base-emitter junction currents, such as those caused by heat, are minimized by the swamping effect of the current through the base voltage-divider resistors. The higher the ratio of voltage-divider current to base current, the better the regulation is. (When the base voltage is held constant, the voltage feedback of R_E has maximum stabilizing effect.)

"Typical" readings for the table in Fig. 7-14B are:

$V_{RL} = 4.5$ volts

$I_C = 4.5/3900 = 1.15$ mA

$I_B = 27\ \mu A$

$h_{FE} = I_C/I_B = 1.15/0.027 = 42$ (approx)

$V_{CE} = 3.4$ volts

$P_C = (V_{CE})(I_C) = (3.4)(1.15) = 3.9$ mW

$A_v = R_L/R_E = 3900/1000 = 3.9$

The readings will be affected by: voltmeter impedance and accuracy, condition of battery (should be fresh), tolerance of resistors, tolerance of transistor. Note how the table values above differ from any original calculated values.

The voltage amplification could be increased by using an adequate bypass capacitor around R_E. In this case $A_v = 3900/30 = 130$ (approx). We

could make the voltage gain anything up to this value by bypassing a portion of R_E as in Fig. 7-18. In this example, R_E is split so that one-half is bypassed, giving an approximate A_v of $3900/500 = 7.8$.

What is the maximum peak-to-peak signal swing we could tolerate with R_E bypassed in this circuit? Assume $V_{CE} = 4.5$ volts nominal. Then the maximum peak-to-peak output signal would be almost $2 \times 4.5 = 9$ volts, and the input signal would be $9/130 = 70$ mV (approx) peak-to-peak. The ac input impedance of the stage is $Z_{in} = (h_{fe})(r_{tr}) = (35)(30) = 1050$ ohms (approx—call it 1000 ohms). (In this calculation of Z_{in},

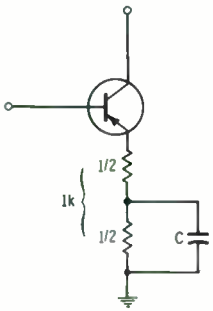


Fig. 7-18. Partial bypassing of emitter resistance to set gain.

h_{fe} is assumed equal to h_{FE}, and the resistance of R_{B1}-R_{B2} is assumed large enough to ignore.) The input signal current is then $70/1000 = 70\ \mu A$. But with a quiescent base current of 30 μA, we can tolerate an input signal swing of only 60 μA without clipping. And this would far exceed the "small-signal" mode of operation. For maximum signal-transfer linearity, we must operate over a very small portion of the transfer curve, as is normally the case for the small-signal mode. If R_E were bypassed in the circuit under investigation, the input signal swing would normally be about one-tenth of the maximum available range.

Problem 2: Amplifier With Shunt Feedback

In Fig. 7-15 we recognize the inverse feedback circuit through R_f. We have the same circuit as in Fig. 7-14 in the following respect:

$I_E = 1$ mA
$I_B = I_E/h_{FE} = 0.001/35 = 30\ \mu A$
$R_L = 3900$ ohms (provides almost 4-volt drop)

The value of R_f must be such as to provide the 30-μA base current from the quiescent operating value of collector voltage V_c. The dc voltage across R_f is 3.8 volts, so $R_f = 3.8/30\ \mu A = 120$k (approx).

The voltage gain is:

$$A_v = \frac{R_f}{Z_{in}}$$

The input impedance is:

$$Z_{in} = \frac{R_L + R_f}{\beta R_L + R_f} R_{in}$$

Problem 3: Amplifier With Dual Power Sources

The discussion concerning Fig. 7-16 should be self-explanatory. Note that the relationship for maximum base current takes into account the fact that maximum I_B occurs when beta is at a minimum. Thus R2 is figured on the basis of allowing for a minimum-beta transistor.

The axis of the input signal voltage will be the +7.8-volt base voltage. The input impedance (Z_{in}) of the stage is R1 and R2 in parallel across the input impedance of the transistor, or:

$$Z_{in} = R1 \,||\, R2 \,||\, h_{fe} R_E = 2.24k \,||\, 20k = 2000 \text{ ohms (approx)}$$

where the symbol || means "in parallel with." Then:

$$V_{in} = (5\,\mu A)(2000) = 10 \text{ mV, or } 0.01 \text{ volt (peak-to-peak)}$$
$$V_{out} = (A_v)(V_{in}) = (8)(0.01) = 0.08 \text{ volt, or } 80 \text{ mV (peak-to-peak)}$$

The output signal has its ac axis on the −1 volt collector voltage. The advantage of this circuit is its much longer transfer curve, which allows maximum linearity over a wide range of transistor beta.

Problem 4: Feedback Pair

The circuit in Fig. 7-17 serves to emphasize the relationship of source impedance and feedback resistance. The table in Fig. 7-17 points up the maximum peak-to-peak voltage available in the load when the quiescent output current is 1.72 mA. The signal swing cannot exceed plus and minus 1.72 mA, or 3.44 mA peak-to-peak, without clipping.

Voltage swing with $R_L = 1000$ ohms: $(0.00344)(1000) = 3.44$ V
Voltage swing with $R_L = 500$ ohms: $(0.00344)(500) = 1.72$ V
Voltage swing with $R_L = 50$ ohms: $(0.00344)(50) = 0.172$ V

CHAPTER 8

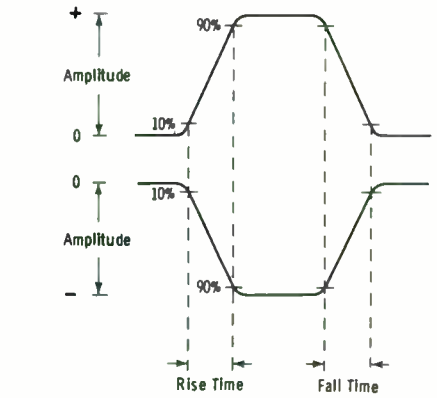
Switching Fundamentals

In this chapter, we will leave the linear transistor applications studied thus far and delve into on-off circuitry. Simple on-off circuitry in solid-state devices is not as "simple" as it might first seem. Switching and pulse applications, however, are fascinating as well as challenging. We will use all we have learned thus far plus some added knowledge. Emphasis will be given those characteristics we need to know to recognize what a circuit is supposed to do, so that we can rapidly analyze it and arrive at sensible procedures for testing and servicing.

8-1. BASIC REVIEW OF PULSE THEORY

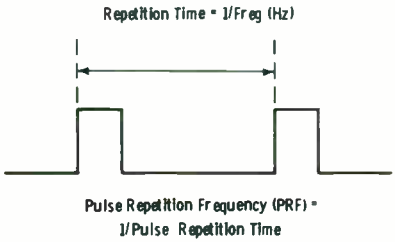
First, let us take a quick review of pertinent pulse theory. See Fig. 8-1 for pulse nomenclature. An important point to bear in mind is that rise time (t_r) is measured between the 10% and 90% pulse amplitudes, whether the pulse is positive-going (Fig. 8-1A) or negative-going (Fig. 8-1B). The same is true of the fall time (t_f), sometimes termed "decay time." The pulse duration is between the 90% amplitudes of the rise and fall. Also remember this: The "zero" level shown in Figs. 8-1A and 8-1B is simply a reference. For the pulse in Fig. 8-1A, the amplitude is increasing in the positive direction. But the base of the pulse (reference) might be at −10 volts and the peak (maximum amplitude) might be at zero volts. The peak is simply positive relative to the base. Similarly, the pulse base (reference) in Fig. 8-1B might be at +10 volts, and the peak (least positive amplitude) might be at zero volts. The peak is simply negative relative to the base.

Fig. 8-1C presents a review of pulse repetition time, sometimes termed "pulse period." It is normally taken as the time interval between the leading edges of successive pulses. It could be the time from 50% amplitude of the leading edge of one pulse to 50% amplitude of the leading edge of the next pulse; or it could be from 10% amplitude of the trailing edge of one pulse to 10% amplitude of the trailing edge of the next



(*A*) *Positive-going pulse.*

(*B*) *Negative-going pulse.*



(*C*) *Repetition time and frequency.*

Fig. 8-1. Basic pulse nomenclature.

pulse. This is to say that the pulse period includes the rise time, the pulse duration, the fall time, and the interval between pulses. The pulse repetition time is equal to the reciprocal of the pulse frequency, sometimes termed "pulse repetition rate (PRR)," or "pulse repetition frequency (PRF)." Conversely, the pulse repetition *rate* is the reciprocal of the pulse repetition *time*.

For example, the frequency (PRR) of horizontal sync pulses is 15,750 Hz. So the pulse repetition time is $1/15{,}750 = 63.5$ microseconds. This is the time interval between corresponding parts of successive pulses. Conversely, $1/(63.5 \times 10^{-6}) = 15{,}750$ Hz. In this connection, bear in mind that we have a chain of pulses at a certain PRR which may be "keyed on" at a much lower rate. Equalizing pulses are 31.5-kHz pulses keyed on at the rate of 60 Hz.

The time constant of a resistance-capacitance combination is the product RC. In Curve 1 of Fig. 8-2, the voltage rise across C for a short time constant is shown. (NOTE: A short time constant means the RC product

is small relative to a pulse period.) Curve 2 depicts the charge on C for a longer time constant, and Curve 3 is for a still longer time constant. The shorter the RC product is (relative to the pulse period), the greater will be the amplitude of the instantaneous voltage (v) after a given charging time (ΔT). The longer the time constant is relative to the pulse period, the less will be the amplitude of the instantaneous voltage developed in a given time, but the slope of the voltage curve will be more gradual and practically linear. Thus the longer the time constant is for a given pulse frequency, the more linear will be the voltage developed across the capacitor, and the more faithfully reproduced will be the pulse across the resistance.

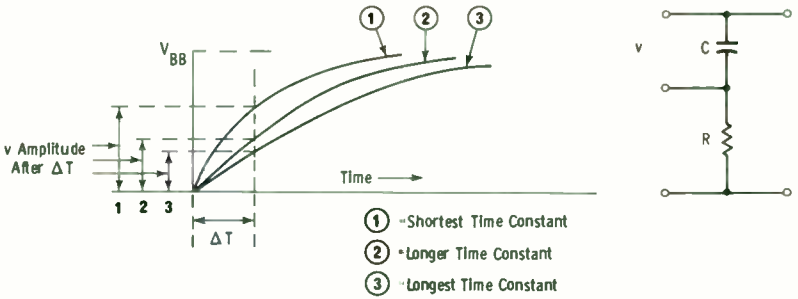
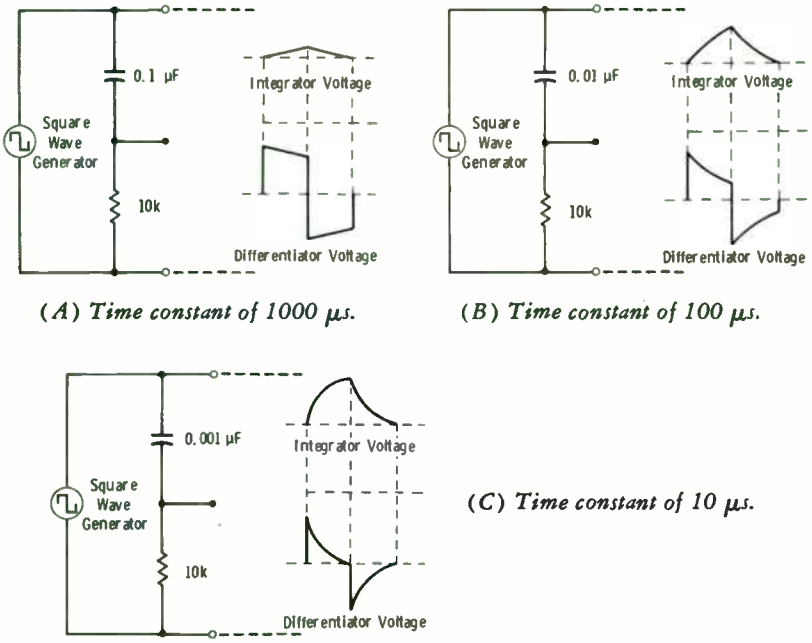


Fig. 8-2. Time constant of RC circuit.

These facts are reviewed in Fig. 8-3. A 10k resistor is used with three different values of capacitance to result in time constants of 1000, 100, and 10 microseconds, respectively. (The most convenient way to get time constant in microseconds is to multiply R in megohms times C in pF.) Now assume we have a symmetrical square wave with a pulse period of 100 μs. When this signal is applied to the circuit of Fig. 8-3A, in which the RC product is ten times the pulse period, the capacitor voltage (integrator voltage) is low but linear, and the resistor voltage output (differentiator voltage) has very little "tilt." The tilt is actually exaggerated in the drawing to emphasize that there will be a slight tilt even at this time constant, since (theoretically) a capacitor never becomes fully charged or discharged. When the RC product is about equal to the pulse period (Fig. 8-3B), the integrator voltage is higher (and nonlinear), and the differentiator voltage exhibits considerable tilt. When the RC product is only one-tenth of the pulses period (Fig. 8-3C), we have the more familiar waveform found in practice in pulse-differentiating circuits. Remember that the polarity of the integrator (capacitor) voltage remains the same, but due to the charge-discharge of C, the current through the resistor reverses, and the differentiator voltage is driven alternately in the positive and negative direction.

Pulses are composed of a dc voltage plus a large number of ac voltages with harmonically related frequencies. The dc component of a pulse series is equal to the average voltage of the pulses. For example, in the series of positive input pulses in Fig. 8-4A, each pulse has an amplitude of +5 volts for a 10-microsecond duration, and zero for a 10-microsecond duration. This variation describes a symmetrical square wave. Assuming



(A) Time constant of 1000 μs.

(B) Time constant of 100 μs.

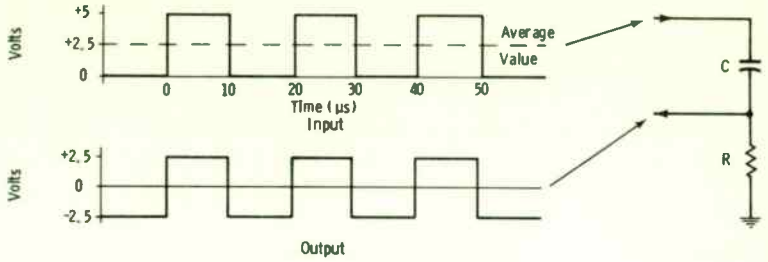
(C) Time constant of 10 μs.

Fig. 8-3. Effect of time constant on waveform.

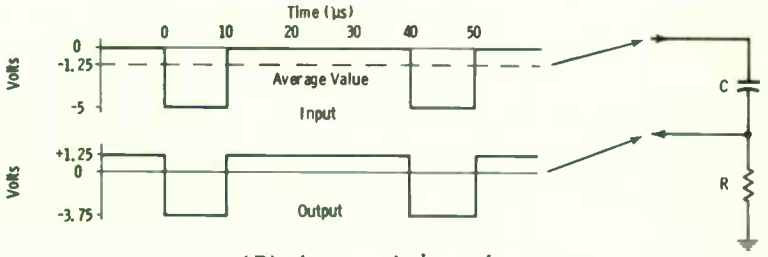
this waveform is transferred through a capacitive coupling circuit with an RC product sufficiently long to prevent distortion, the pulse series will arrange itself so that the ac axis corresponds to the average dc value (output waveform in Fig. 8-4A).

In the series of negative input pulses of Fig. 8-4B, the input waveform has an amplitude of −5 volts for 10 microseconds, and then the voltage is zero for 30 microseconds. This variation describes a nonsymmetrical (asymmetrical) pulse series. At the output of the coupling network, the ac axis (zero axis) of the waveform corresponds to the average dc value of the input, so the base of the pulse is at +1.25 volts, and the pulse tip is at −3.75 volts.

Power normally is measured as an average value over a relatively long period of time. But in nonsymmetrical pulse chains, average power de-



(A) Symmetrical waveform.



(B) Asymmetrical waveform.

Fig. 8-4. Transfer of pulses through RC network.

livered over one cycle of operation can be quite low compared to the peak power available during the pulse time. Here is the basic relationship:

$$\frac{\text{Average Power}}{\text{Peak Power}} = \frac{\text{Pulse Width}}{\text{Pulse Repetition Time}}$$

That is, the average power is to the peak power as the pulse width is to the pulse repetition time. Either one of the above ratios is an expression of the fraction of the total time that energy is supplied. This time relationship is termed the duty cycle:

$$\text{Duty Cycle} = \frac{\text{Average Power}}{\text{Peak Power}}$$

and:

$$\text{Duty Cycle} = \frac{\text{Pulse Width}}{\text{Pulse Repetition Time}}$$

Since a "resting time" occurs between pulses that are narrow in comparison to the repetition time, the average power for such pulse trains can be quite low even though the peak power might be quite high. The horizontal sync pulse with a width of 4.8 microseconds and a repetition time of 63.5 microseconds has a duty cycle of $4.8/63.5 = 0.075 = 7.5\%$. Suppose we arbitrarily assign a peak power level of 1000 watts. Then for

4.8 microseconds, 1000 watts of power is dissipated. For the remaining 58.7 microseconds (63.5 − 4.8 = 58.7), zero power is available. Now from the basic relationship:

$$\text{Average Power} = (\text{Peak Power})\,(\text{Duty Cycle})$$

Then:

$$\text{Average Power} = (1000)\,(0.075) = 75 \text{ watts}$$

Putting this result into terms of a transistor handling horizontal sync pulses, if the peak pulse power is 1000 milliwatts, the average power handled by the transistor is 75 milliwatts. (NOTE: This value can be dependent on the polarity of the input pulse for a given type of transistor. See Q8-4 through Q8-7 in the Exercises at the end of this chapter.)

8-2. BASIC TRANSISTOR SWITCH

A pulse generator or amplifier, multivibrator, clamp, counter, gate, etc., in general operates as a switch, or nearly so. A diode or a transistor can be made to operate as a very efficient analog of a mechanical switching device. Either can be made to have a high-resistance (open) or a low-resistance (closed) state. A diode can be switched only by altering its bias. The state of a transistor can be controlled easily from the base lead; a relatively small base current can control a relatively large collector current. So by analogy, a diode is to a mechanical switch what a transistor is to a relay.

In a switching mode, the transistor is operated, by a pulse or a dc level, either fully on or fully off (saturation or cutoff). See Fig. 8-5. For the load line selected (which is typical for switch service), a considerable portion of the line is in an area where the power dissipation is excessive (Chapter 4). But point A (cutoff) and point B (fully on) are within the safe operating limits. The only time the transistor will operate in the "active" region between A and B is during the transient time taken for the device to be turned "on" or "off" from its previous state. At moderate switching rates, the average power dissipation of the transistor can be quite low even at high peak powers. Of course, the higher the switching rate (or the greater the duty cycle), the more the transient excursion into the high-power region becomes a factor.

Point A has a very low current and a relatively high voltage. These values imply a high-resistance, or "open," condition. In a properly designed circuit, this current is simply I_{CO}. In a silicon transistor, the leakage current can be as small as a few nanoamperes. In a germanium transistor (which has an inherently higher leakage current), it is typically 2 to 5 microamperes or more.

Point B has a relatively high current and a low voltage. These values imply a low-resistance, or "closed," condition. The symbol V_S designates

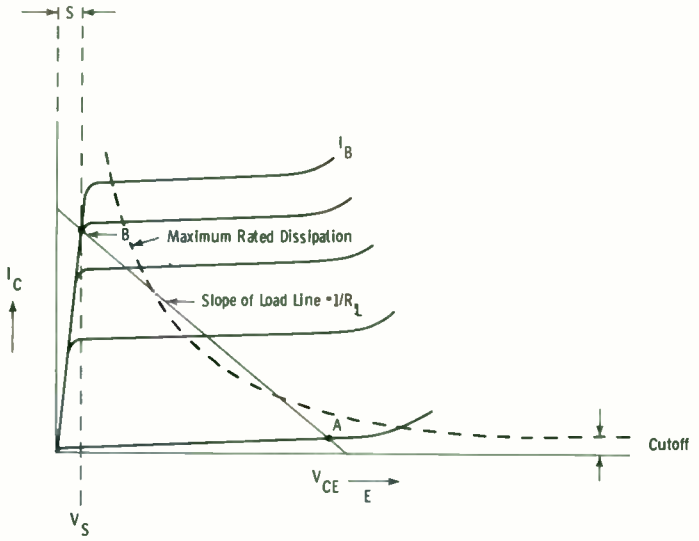


Fig. 8-5. Collector characteristics.

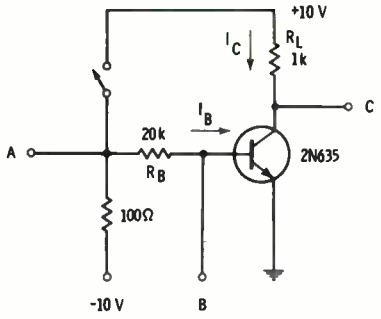
the voltage from collector to emitter in the saturated condition. Note that a sufficient amount of base current must be supplied to cause saturation.

The basic switching problem is one of transient response. See Fig. 8-6A. The mechanical switch in the circuit can represent any switch-type configuration. At time T1 (Fig. 8-6B), the switch is open. We have a −10 volt source connected to the base of an npn transistor, so the base-emitter junction is reverse biased at −10 volts, less a very slight voltage drop from leakage currents. Thus the transistor is cut off, and, since there is no I_C, the collector voltage is +10 volts (less the small drop due to leakage currents). So we would measure a total voltage of +20 volts from collector to base.

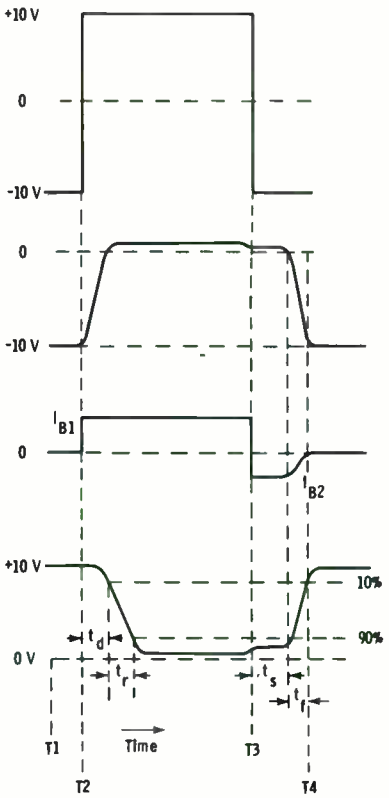
This condition (switch open) means that any capacitance between collector and base must be charged to 20 volts, and any capacitance between base and emitter must be charged to 10 volts. At time T2 (instant of switch closure), the base voltage cannot change instantaneously because of the charged base capacitance. Since this is true, we have placed 20 volts across 20k, so:

$$I_B = \frac{20}{20{,}000} = 1 \text{ mA}$$

Until V_{BE} (voltage across the base-emitter capacitance) decreases sufficiently, the transistor cannot turn on. As soon as V_{BE} has reached +0.2 volt (for germanium) or +0.6 volt (for silicon), collector current will begin. At this time, V_{BE} becomes clamped and will no longer rise. This



(A) Diagram.



① Waveform at A Caused by Switch Action

② Waveform at B. Forward bias on base occurs during saturation.

③ Base - Current Waveform. (I_{B2} is reverse current due to base bias during saturation.)

④ Collector - Voltage Waveform Showing Definitions of Response Times

(B) Waveforms.

Fig. 8-6. Transistor switching circuit.

is the standard base-emitter voltage drop in the forward-biased condition. When the transistor is saturated, I_C is $10/1000 = 10$ mA. The collector *voltage* will be very close to ground potential (very small voltage drop across the transistor).

The time after closing of the switch required to reach the threshold of transistor turn-on (the 10-percent amplitude point of the waveform) is the delay time (t_d) shown in waveform 4 of Fig. 8-6B. The time from the 10-percent point to the 90-percent point is the rise time (t_r). The remainder of the pulse to time T3 is the pulse duration.

When V_{BE} reaches the forward-bias level, the value of I_B remains essentially constant at $10/20{,}000 = 0.5$ mA (I_{B1} of waveform 3).

Note that during the time between T2 and T3 the base voltage (waveform 2) is slightly positive (this is an npn transistor), and the collector voltage (waveform 4) is also only slightly positive. In saturation, the collector voltage actually falls below the base voltage, so the base-collector junction now becomes *forward biased*, and the collector begins emitting. Keep the following relationships in mind:

1. When the transistor is cut off, both the base-emitter and base-collector junctions are reverse biased. The voltages under this condition cause the junction capacitance to assume a charge which must be overcome to turn the transistor on. This is the reason for delay time t_d.
2. When the transistor is saturated, both the base-emitter and base-collector junctions are *forward* biased. This condition results in a stored charge of carriers in the base region. Current is controlled by the carrier distribution in the base; this means that collector current cannot decrease until the stored base charge is removed. It is the reason for "storage time" t_s shown in waveform 4.

At time T3, the switch is opened again. The voltage at A drops immediately to -10 volts. But the base voltage (waveform 2, Fig. 8-6B) cannot go negative immediately due to the stored carriers in the base. The negative voltage across the base resistor draws the positive carriers out of the base, resulting in current I_{B2} (waveform 3, Fig. 8-6B). As soon as the stored carriers are released, the transistor begins to turn off. Remember here the effect of junction voltages and currents on junction capacitance (Chapter 2). The higher the forward current (I_{B1}), the greater the stored charge will be. The higher the reverse current (I_{B2}), the faster the stored charge is drained away.

The main result of operating a transistor switch in a saturated condition is pulse widening.

8-3. CONTROLLED CURRENT GAIN

Observe the circuit of Fig. 8-6, and note a very important point. Resistance R_L is 1000 ohms, and the base resistor (R_B) is 20,000 ohms. If the transistor is in saturation, the collector saturation current is:

$$I_{CS} = \frac{V_{CC}}{R_L} = \frac{10}{1000} = 10\text{ mA}$$

The base current is:

$$I_B = \frac{V_{BB}}{R_B} = \frac{10}{20{,}000} = 0.5\text{ mA}$$

and the dc current gain is:

$$A_i = \frac{I_C}{I_B} = \frac{10}{0.5} = 20$$

What is so important about this? Simply that current gain is the ratio of R_B to R_L:

$$A_i = \frac{R_B}{R_L}$$

In the example just used, A_i is 20,000/1000 = 20. Note that the transistor in the example is a type 2N635. Specification sheets reveal that the type 2N635 has a minimum h_{FE} of 25 at 25°C. So in this case current gain is limited by circuit design and is independent of transistor beta. Although this specific type of transistor can have a beta of 25 to 100, a replacement installed in this circuit would not affect operating parameters.

Now suppose R_L in Fig. 8-6 is reduced to 100 ohms. What would happen? (Assume same base resistor and supply voltages.)

We still have the same operating base current of 0.5 mA. If we take the minimum beta of 25, the collector current is:

$$I_C = (h_{FE})(I_B) = (25)(0.5\text{ mA}) = 12.5\text{ mA}$$

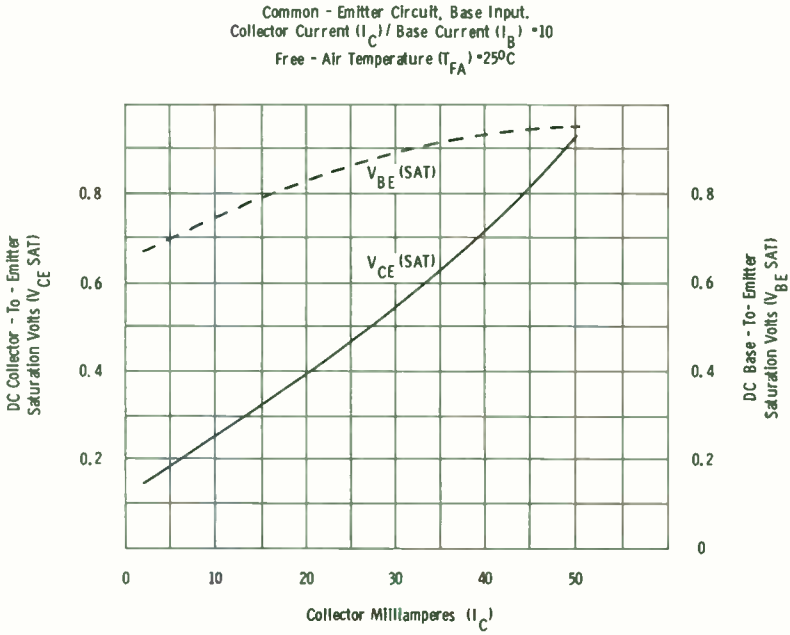
The voltage drop across R_L of 100 ohms is (0.0125)(100) = 1.25 volts. So the collector voltage is 10 − 1.25 = 8.75 volts. The transistor is nowhere near saturation.

Even at the maximum beta of 100, the collector current is 50 mA, and the voltage drop across R_L is then 5 volts. Again, the transistor is nowhere near saturation. If R_L is too low (relative to R_B), the transistor will not saturate, and the current gain is entirely dependent upon h_{FE}. This is "normal" (linear) operation with the input junction forward biased and the output junction reverse biased.

For the transistor to be saturated, the collector voltage must fall below the base voltage (base-collector junction forward biased). The voltage at the collector is then the "saturation voltage," V_s, indicated in Fig. 8-5. It will generally be a volt or less, normally around 0.1 to 0.2 volt, depending on current and type of transistor.

Obviously, if the transistor is cut off, either from design or because of faulty junctions, we will measure the entire supply voltage for V_{CE}. Remember that V_{CE} will be *less* than V_{BE} if the transistor is saturated,

as the curves of Fig. 8-7 show. Note that the collector current influences both voltage measurements, and that the temperature is specified as 25°C. *Carefully note* that when a transistor is in saturation, we can get a higher value of V_{BE} than that required to cause conduction (0.6 to 0.7 volt for silicon), and that this voltage increases with increases in I_c.



Courtesy RCA Corp.

Fig. 8-7. Typical saturation-voltage characteristics for type 2N708.

For V_{BE}, if the transistor is conducting, we will measure the "standard" voltage drop depending upon whether the transistor is germanium or silicon. (Voltage V_{BE} is also somewhat dependent on total emitter current and temperature.) But how about a circuit which incorporates a reverse-biased base-emitter junction? Naturally this V_{BE} can be any value up to the maximum rating for the particular transistor type. For the 2N406, for example, this rating is 2.5 volts (emitter negative relative to base); the rating includes *both* the dc and peak ac signal value. This is another important reason to have manufacturer's data on any particular transistor with which we are experimenting.

8-4. MODIFICATIONS TO PREVENT PULSE WIDENING

When a transistor is to act simply as a switch, cutoff (maximum resistance) and saturation (minimum resistance) are desirable and neces-

sary states. In many applications of this nature, pulse duration is not an important factor. Conversely, in higher-speed switch service and in certain pulse generators and amplifiers, turn-on and turn-off times are very important.

If just sufficient base current to saturate the transistor is employed, the stored charge will be minimized. By overdriving the base to cut it off, widening of the pulse is minimized. These methods would require precise control of pulse input amplitude, and therefore very critical circuit and component tolerances would have to be maintained over a wide temperature range. This is an impractical requirement, and so designers must devise other approaches to the problem.

See Fig. 8-8 for basic means of preventing saturation. (There are others which we will point out in later chapters.) Fig. 8-8A illustrates the simplest technique used. The diode back-bias voltage (V_D) is such as to prevent the collector voltage from falling below the base voltage. Unless the base-collector junction can become forward biased, the transistor cannot saturate.

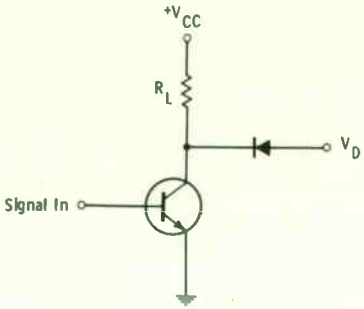
In Fig. 8-8B, the base current is controlled so that the collector current is held below the saturation level (collector voltage always held slightly above base voltage). As the collector voltage falls below the voltage at the junction of R1 and R2, the diode becomes forward biased and diverts part of the current from R1 toward the collector. This action prevents further increase in the base current and hence in the collector current. Since the current in R2 is the base current (I_B), and since $I_C = (h_{FE})(I_B)$, then V_{CE} is approximately $I_C R2/h_{FE}$.

In Fig. 8-8C, we find the added base-bias network (R3 and voltage $-V_B$) used in many circuits to make V_{CE} independent of I_C and h_{FE}. Values for R3 and V_B are chosen to give a suitable minimum V_{CE}.

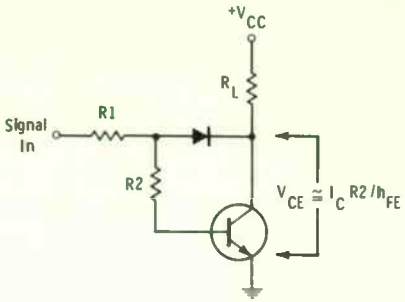
In Fig. 8-8D, R2 is replaced with a silicon diode. Remember that a silicon junction has a forward voltage drop of 0.6 to 0.7 volt over a wide range of junction current. So V_{CE} will be held at approximately 0.6 to 0.7 volt.

Fig. 8-8E shows a very simple and effective collector-current clamp suitable for use with a silicon transistor. Since the germanium junction has a forward voltage drop of only 0.2 to 0.3 volt, the 0.6-volt forward bias on the collector-base junction (necessary for saturation) cannot be reached with the germanium diode connected between the collector and base as shown.

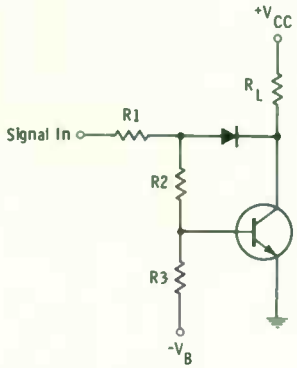
A basic means of avoiding turn-off storage time delay is represented by Fig. 8-8F. With zero picofarads (0 pF) the maximum storage time will take place. With the proper voltage source and capacitance, the capacitive charge neutralizes the stored charge. It is a means of actually "overdriving" the turn-off current into the base to get sharper pulse edges. Diodes are sometimes used in place of the RC network to accomplish a similar result.



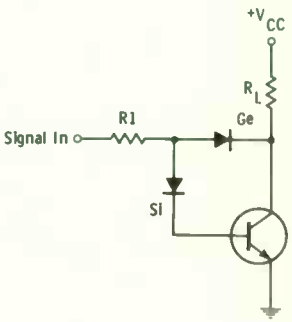
(A) *Collector diode clamp.*



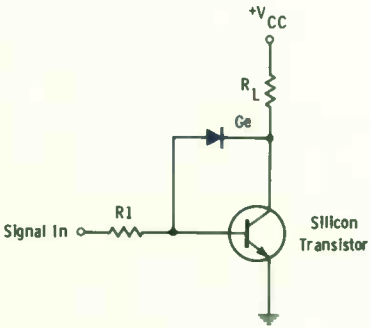
(B) *Controlled base current.*



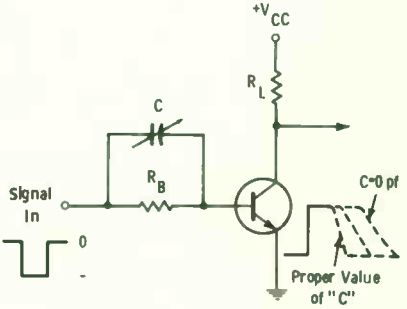
(C) *Added bias supply.*



(D) *Collector current clamp.*



(E) *Simpler clamp circuit.*



(F) *Speed-up capacitor.*

Fig. 8-8. Basic methods for preventing pulse widening.

EXERCISES

Q8-1. If a symmetrical square wave has a frequency of 50 kHz, what are the pulse period and the duty cycle?

Q8-2. What can you say about the duty cycle of any symmetrical square wave regardless of pulse width or pulse repetition time?

Q8-3. If a waveform has a pulse period of 40 μs and a pulse width of 10 μs, what are the pulse frequency and the duty cycle?

Q8-4. Assuming waveform A of Fig. 8-9 is of sufficient amplitude to drive transistors B and C from cutoff to saturation, what are (1) the duty cycle at the collector of B, and (2) the duty cycle at the collector of C?

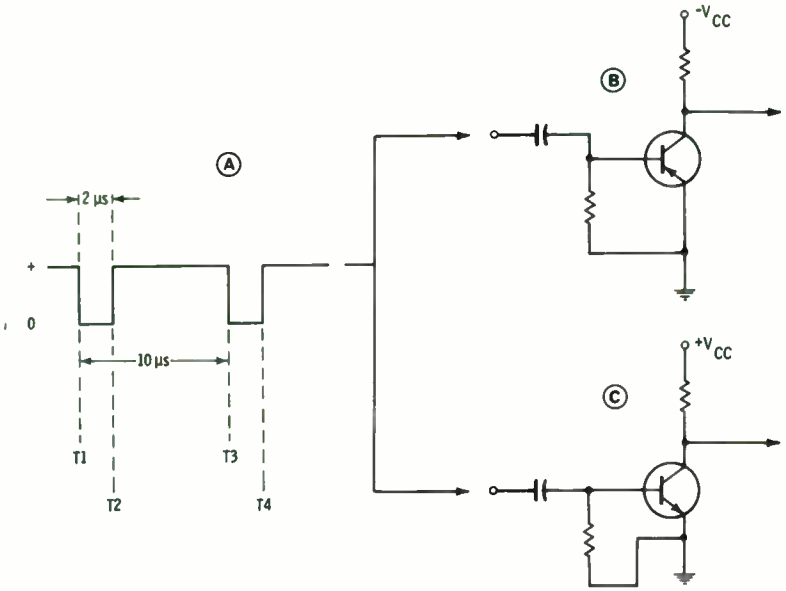


Fig. 8-9. Pnp and npn duty cycles (Q8-4).

Q8-5. If the peak power of the 2μs pulse in Fig. 8-9 is 100 mW, what is the average power?

Q8-6. What is the average power at the collector of transistor C (Fig. 8-9)?

Q8-7. If the polarity of the input pulse of Fig. 8-9 is reversed, what can you say about the duty cycle at B and C?

Q8-8. See Fig. 8-10. What pulse amplitude is necessary at the input of this simple circuit to saturate the transistor? Will such a simple circuit work satisfactorily as a pulse amplifier?

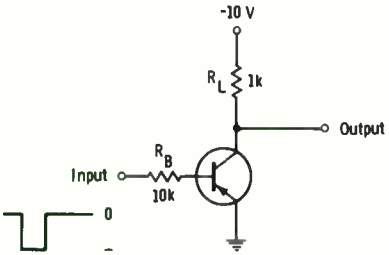


Fig. 8-10. Pulse-amplitude problem (Q8-8).

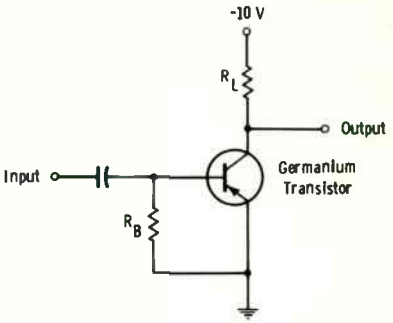


Fig. 8-11. Simple pulse circuit (Q8-10).

Q8-9. If R_L of Fig. 8-10 is left at 1k and R_B is reduced to 5k, what is the necessary amplitude of the input pulse to saturate the transistor?

Q8-10. Is the simple pulse circuit of Fig. 8-11 effective? What is the main drawback?

CHAPTER 9

Switching and Pulse Applications

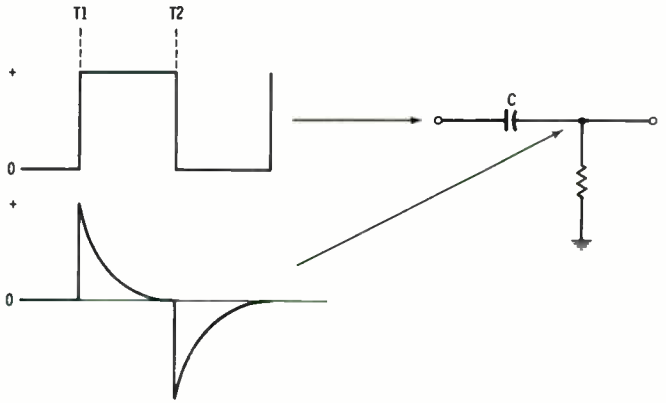
This chapter will introduce practical transistor pulse-circuit analysis. We will learn how to tell what a circuit is intended to do, and what to expect in the way of input and output waveforms if the circuit is to function as intended.

9-1. "BOXCAR" PULSE GENERATOR

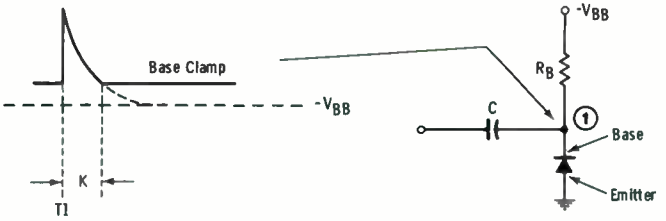
Chapter 8 introduced cutoff-saturation transistor characteristics. We learned that pulse-widening results from switching a transistor between cutoff and saturation. We will now consider a saturated transistor circuit which narrows a pulse, and is capable of adjusting the output pulse width.

The first step is to analyze the content of Fig. 9-1. Fig. 9-1A can be used to review the conventional action of a short-time-constant RC circuit on a square-wave input. Prior to time T1, there is no charge on the capacitor, and no current in the resistor. At T1, a positive-going voltage is applied in the form of a square wave. The capacitor begins to charge, but there is no voltage across the capacitor until it is charged. Therefore, at T1 the entire voltage must appear as a voltage drop across the resistor. As the capacitor becomes charged, the voltage appearing across it is subtracted from the applied voltage, and the voltage across the resistor is decreased. Since the time constant (RC product) is short relative to the input pulse duration, the capacitor charges quite rapidly, and the voltage across the resistor quickly falls to zero (T2). At this time, the negative-going pulse reverses the previous action, and the conventional differentiated waveform with twice the peak-to-peak value of the applied pulse results.

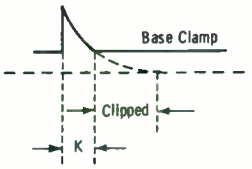
Now go to Fig. 9-1B. Here is a diode which simulates the base-emitter junction of a pnp transistor. It is forward-biased by the current from V_{BB} through R_B. The time constant, CR_B, is assumed the same as in A above.



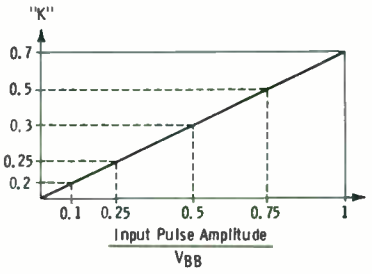
(A) Differentiating network.



(B) Equivalent of junction.



(C) Smaller pulse amplitude.



(D) Graph of "K factor."

Fig. 9-1. Action of a forward-biased base-emitter junction.

Prior to time T1, point 1 is held near ground potential by the forward-biased diode junction. At time T1, application of the positive pulse reverse-biases (opens) the diode junction, and the capacitor starts to charge toward negative potential V_{BB} through R_B. The action continues only to the point at which the diode again becomes forward biased and the potential falls to the small forward voltage drop across the junction. Note that any further negative-going excursions of the waveform are clamped out by the forward-biased junction.

So now we have a very important "K" factor which determines the width of the pulse at the transistor base. This K factor depends not only on the RC product (which determines the "shape" of the charge-discharge curve), but also on the amplitude of the input pulse. Observe Fig. 9-1C, where the input pulse is smaller in amplitude than in Fig. 9-1B. Now the base clamp occurs earlier, and the K factor becomes smaller in value. The width of the pulse at the base of the waveform is less than in Fig. 9-1B.

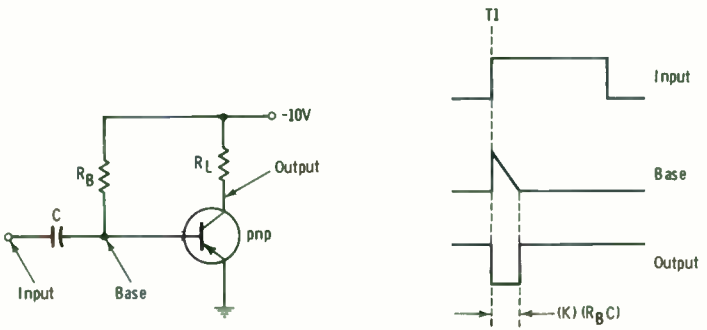
A very approximate relationship of the K factor to input pulse amplitude is shown in the graph of Fig. 9-1D. If the input pulse is equal to or greater than V_{BB}, a K factor of 0.7 results. If the ratio of the input pulse to V_{BB} is unity (one), the base pulse width will be:

$$\text{Width} = (K)(RC) = 0.7(RC) \qquad \text{(approx)}$$

This relationship is only approximate, but it is useful.

Apply this principle to the circuit of Fig. 9-2A. In the absence of an input pulse, the transistor is held in saturation because the base is returned to −10 volts and the emitter is tied directly to ground. In this state, the collector voltage is very near ground potential.

At time T1 (Fig. 9-2B), a positive input pulse is applied, reverse-biasing the base-emitter junction and cutting off the transistor (assuming the pulse supplies sufficient cutoff current.) This action sends the collector voltage to −10 volts. The capacitor starts to charge through the

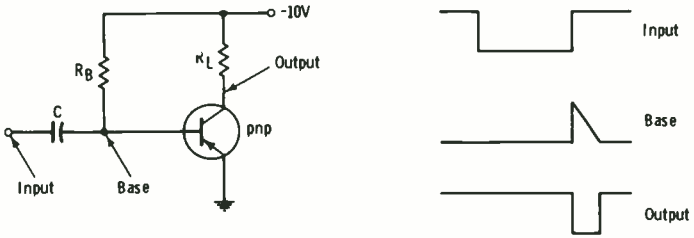


(*A*) *Diagram.* (*B*) *Waveforms.*

Fig. 9-2. Inverting circuit for narrowing positive pulses.

base resistor toward −10 volts, but the base voltage is clamped at the point where the input junction again becomes forward biased. The transistor is again saturated, and the collector voltage is again near zero. The width of the output pulse is approximately the K factor times the product CR_B.

A circuit in which a transistor is operated in saturation until a pulse comes along to send it toward cutoff is termed a "boxcar" circuit, just as is its equivalent in vacuum-tube circuitry. It is popular and important, and we should become well acquainted with with what to expect in this type of circuit.

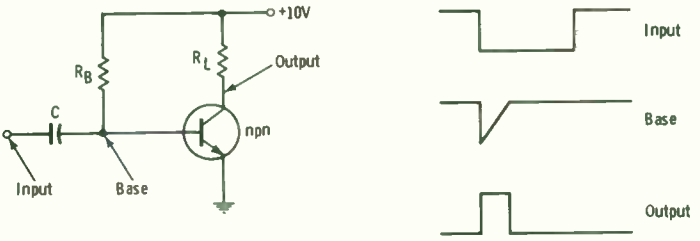


(*A*) *Diagram.* (*B*) *Waveforms.*

Fig. 9-3. Noninverting circuit for narrowing positive pulses.

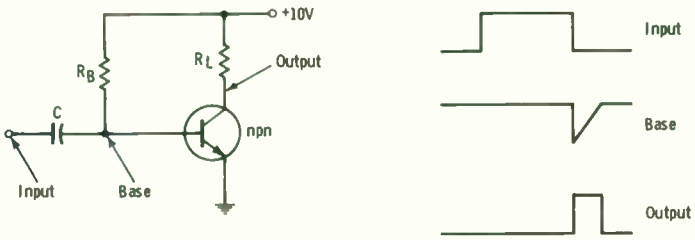
Now go to Fig. 9-3. Here we have the same pnp transistor and circuit as in Fig. 9-2. But the input pulse is a *negative*-going pulse. At the base of the transistor, the pulse transferred by the coupling capacitor would normally consist of a negative-going excursion followed by a positive-going excursion. However, the low forward impedance of the junction provides a clamping action which prevents negative-going excursions. Since the transistor is already saturated, negative excursions have no effect. At the end of the input pulse, the positive-going excursion drives the transistor toward cutoff, and C begins to charge through R_B toward −10 volts. Note that the output pulse occurs at the *trailing edge* of the input pulse. The width of the output pulse is $(K)(R_BC)$. Obviously, if R_B is made variable, the pulse width can be adjusted as desired.

Using the foregoing principles, the reader should be able to analyze the circuitry of Figs. 9-4 and 9-5. When we know the type of transistor (pnp or npn) and the polarity of the input pulse, we know whether the circuit is intended as an undelayed pulse generator or a delayed pulse generator. Also bear in mind that the initial pulse narrowing is done by the differentiator circuit (R_B-C), and that the resulting output pulse width depends upon this RC product as well as the K factor. The K factor is determined by the ratio of the input pulse amplitude to the base supply voltage. To drive the transistor completely to cutoff, the pulse must



(A) Diagram. *(B) Waveforms.*

Fig. 9-4. Inverting circuit for narrowing negative pulses.



(A) Diagram. *(B) Waveforms.*

Fig. 9-5. Noninverting circuit for delaying positive pulses.

have sufficient current to overcome the forward bias current. Some analysis practice is included in the exercises at the end of this chapter.

9-2. LOW-IMPEDANCE PULSE DRIVERS

In pulse work as in video distribution, it is sometimes necessary to provide a low-impedance sending-end termination. This application is not limited to pulse distribution lines. For example, if a pulse is to be supplied to several circuits, or to a grouping of diodes in which the capacitance buildup can be considerable, problems in pulse distortion can accumulate.

The first thought in low-impedance transistor output circuits is quite naturally the emitter follower. Fig. 9-6A shows the basic problem in a pnp emitter follower for pulse work. Capacitance C represents the depletion-layer capacitance between the emitter and base, as well as the capacitance of the load. A negative input pulse at the base of Q1 causes conduction, and C is charged through the relatively low resistance of the forward-biased junction with the polarity shown. Removal of the negative drive from the base means that the emitter is held negative with respect to the base, causing cutoff. The capacitance must now discharge through R. We can see that if R is higher in value than the very low

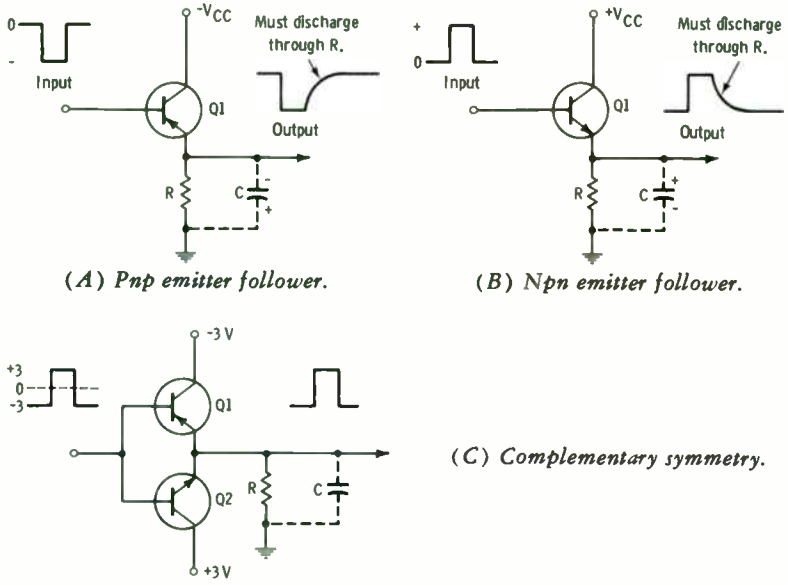


Fig. 9-6. Effects of capacitance on pulse amplifiers.

charging resistance, the fall time of the output pulse will be longer than the rise time. Following the same line of reasoning, note that the same problem exists for the npn circuit of Fig. 9-6B.

Obviously the fall time of the output waveform can be reduced by providing a low-impedance discharge path for C similar to the charge path. This is just what is provided by the complementary emitter-follower circuit of Fig. 9-6C. A positive input at the base drives Q2 into conduction, charging C to a voltage almost equal to the input voltage. When the input goes negative, Q1 conducts and discharges C through the relatively low-resistance base-emitter diode of Q1. With matched transistors, rise and fall times are identical, and the output pulse is symmetrical.

When Q1 of Fig. 9-6C is conducting, Q2 is cut off, and vice versa. So we have a push-pull stage without the need of a transformer or phase splitter. This is one transistor circuit impossible to duplicate with vacuum tubes. Although the circuit is push-pull, it provides a single-in, single-out connection. The output voltage swing will have approximately the same amplitude as the input voltage swing.

9-3. SYNC SEPARATORS

A sync separator is simply one application of a clipper circuit. Sometimes we will find these circuits termed "sync clippers." This term is also applied to sync-in, sync-out circuits for purposes of shaping or level

control. Sync separation in the sense we are considering here means a level (amplitude) function: separating the sync portion from a composite signal and eliminating the video portion.

Consider the circuit of Fig. 9-7, and analyze it in this way: The input signal (composite) swings from −10 to −22 volts. This is a peak-to-peak swing of 12 volts. We know the video-to-sync ratio at the studio is 70 to 30, or 30 percent sync, so the most negative portion of the signal is 30 percent of 12, or 3.6 volts sync.

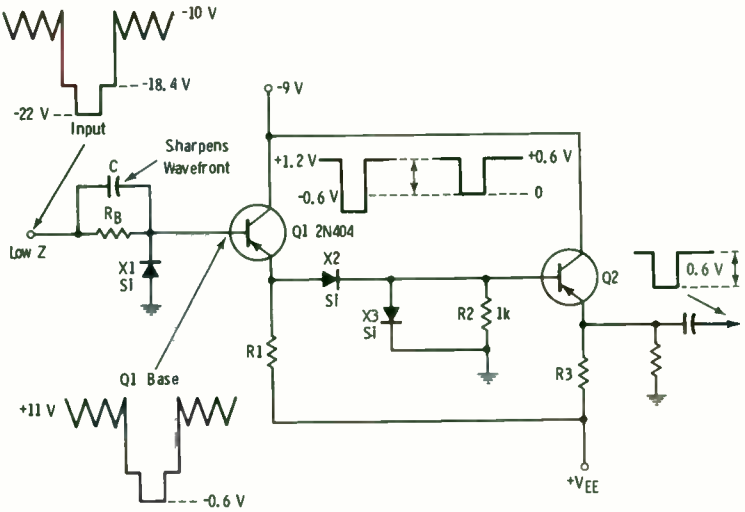


Fig. 9-7. Sync-separator circuit.

Through the action of diode X1, the sync tips appearing at the Q1 base are clamped at −0.6 volt, as the waveform on the diagram shows. Now what is the potential at the Q1 emitter? It can be no more positive than is allowed by the forward voltage drops of X2 and X3, regardless of the positive dc potential of the emitter supply. Since the resistance of R2 (the dc return for the diodes and the Q2 base) is high relative to the forward resistance of X3, X2 and X3 are effectively in series. So the Q1 emitter cannot go more positive than +1.2 volts (0.6-volt forward drop to ground through each diode in series).

Now we have the two reference points for the signal swing at the Q1 emitter. Since the 2N404 transistor (Q1) will conduct as long as its base is at least 0.2 volt negative relative to the emitter (germanium transistor), and assuming essentially unity gain for the emitter follower, the sync tip occurs at −0.6 volt at the Q1 emitter (same amplitude as at base in conduction state). When the input signal rises to about +1 volt at the Q1 base, the transistor begins to cut off. At cutoff, the emitter po-

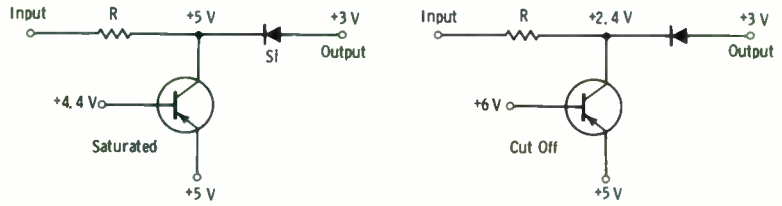
tential becomes +1.2 volts. Therefore Q1 passes only the part of the waveform from tip of sync (−0.6 volt) up to about +1 volt. The remaining sync region and all of the video region are clipped off. If we find any video at the Q1 emitter, the most likely trouble is *low amplitude* of the input signal.

Diode X3 clamps the signal at the Q2 base to +0.6 volt. Therefore, Q2 passes only that portion of sync from the baseline down to zero volts, clipping the tip of sync. The combined action of Q1 and Q2 is to take a slice out of the center of the sync region and to pass this on to the next stage.

All sync separators work on this principle; the stage is made sensitive only to the sync region of the composite video signal. Usually more than one stage is used in the process to obtain sharp leading and trailing edges, and to eliminate any "noise" in the sync region. Sync can also be separated (or eliminated) by gating circuits, which we will study next.

9-4. GATES

A gate is just what its name implies—it can be open or closed to a given signal. Because of the ability of a gate circuit to evaluate input conditions and then provide a predetermined output, these circuits are often referred to as *logic* circuits. In this chapter, we will consider only the simplest approach to "gating." Chapter 14 covers the logic circuits and terminology so necessary in following the new instruction books on latest solid-state systems.



(*A*) *Circuit open.* (*B*) *Circuit closed.*

Fig. 9-8. Transistor-diode gate.

Fig. 9-8 represents a common type of transistor-diode gating circuit for video switching systems. With the bias voltages as shown in Fig. 9-8A, the transistor is saturated, and the +5 volts at the emitter appears at the collector (switch closed). Thus the diode is reverse-biased, and the input is isolated from the output. With the transistor biased as in Fig. 9-8B, the transistor is cut off (switch open). The diode is forward biased, the shunt transistor switch is open, and the input signal appears at the output. In practice, the transistor is normally one section of a bistable multivi-

brator (Chapter 10) which will be on or off depending upon application of a control pulse supplied by the switcher control.

In the common-base circuit of Fig. 9-9, note that the emitter is returned to a positive potential and the base is grounded. *This is the first step in analysis of any pulse or switch circuit: Determine whether the dc (quiescent) condition causes conduction or nonconduction.* In this example, the dc bias conditions are such as to forward-bias the input; therefore, the transistor is conducting in the absence of a signal.

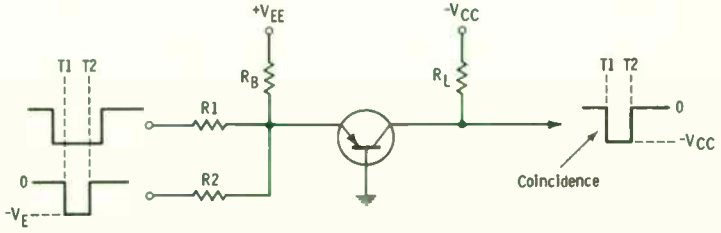


Fig. 9-9. Common-base AND (coincidence) gate.

When we see a circuit of this type with multiple inputs, we will know it is designed so that the signals applied through isolation resistors R1 and R2 *must be coincident* to cause an output. Either pulse alone is not sufficient to cut off the transistor. We know of course that the pulses must be negative (at the emitter) to cut off the pnp transistor, positive pulses being clamped by the low-impedance emitter-base junction. This gate is termed a coincidence gate, or (in logic) an AND gate. An npn transistor could be used with reverse dc and pulse polarities.

The circuit of Fig. 9-10 is identical to that of Fig. 9-9, except that no forward (or reverse) bias is applied to the input junction. Since a transistor must have its input junction slightly forward-biased to conduct, we know this transistor is normally off. Now, whereas the circuit of Fig. 9-9 must have combined pulse currents sufficient to overcome the forward bias currents for turnoff, the pulse amplitudes in Fig. 9-10 need be only great enough to supply a forward bias to the input junction. When we see a circuit of this type with multiple inputs, we will know it is an OR

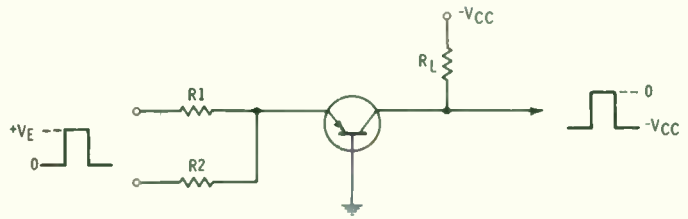


Fig. 9-10. Common-base OR gate.

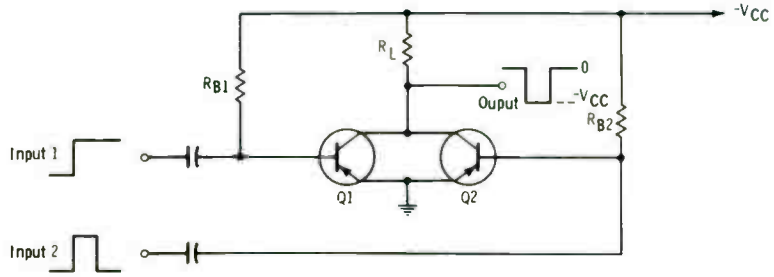


Fig. 9-11. Circuit for AND (coincidence) gate.

gate; that is, either input will result in an output. Naturally, the input must be a positive pulse for a pnp transistor.

Fig. 9-11 shows a very popular parallel coincidence gate. Note that both transistors are "boxcars" in saturation from the bias arrangement. With pnp transistors, positive pulses must be applied to the bases for cutoff. If these pulses occur only on one input, the opposite transistor is still in saturation and the output voltage is near zero. When coincidence occurs, both transistors cut off, and the output goes to the full $-V_{CC}$. Since the common-emitter arrangement is used here, the output is inverted from the input. (CAUTION: Phase inversion *would not* occur if the coincidence gate is used as a delay generator. Review Fig. 9-3.)

As an example of circuit application, Input 2 could be a continuous chain of vertical sync pulses, and Input 1 a 6-line gating pulse. Thus the output would contain 6 vertical sync pulses "gated on" by the 6H interval at a rate of 60 Hz.

In Fig. 9-12, both the base resistors and the emitters are returned to ground. In the absence of a signal, Q1 and Q2 are at cutoff, and the collector voltage is the full $-V_{CC}$. A negative pulse (pnp transistor) at either input will result in conduction of the associated transistor. Assuming saturation, the collector rises to essentially ground (zero) potential.

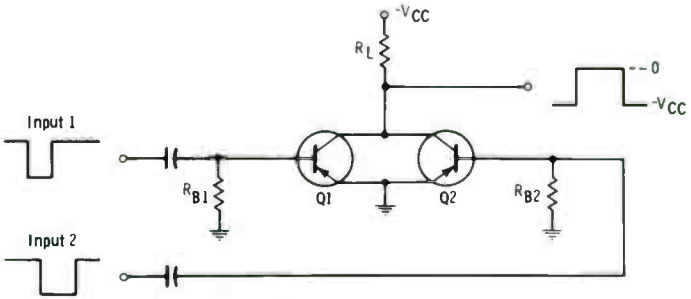


Fig. 9-12. Circuit for OR gate.

The output pulse will have a constant amplitude (the saturation collector voltage) whether one or both inputs are active. The width of the output pulse is dependent upon the widths and phasing of the input pulses.

Fig. 9-13 illustrates the shunt (inhibition) gate. Note that Q1 is reverse biased at the base. With this quiescent operating condition (shunt switch open), any signal applied is developed across R_L. When the base receives a negative control pulse of sufficient amplitude to overcome the reverse bias, Q1 is driven into conduction. Since the shunt switch is now a closed circuit, the signal is shorted to ground, and no output exists

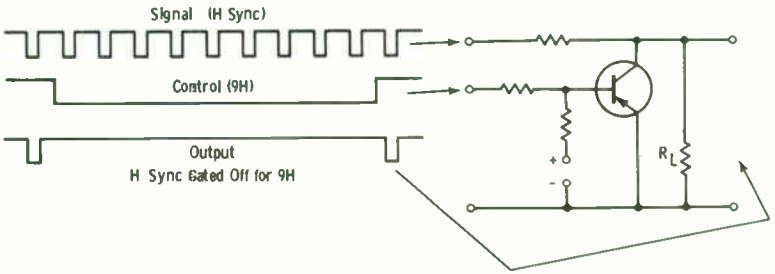


Fig. 9-13. Operation of an inhibition gate.

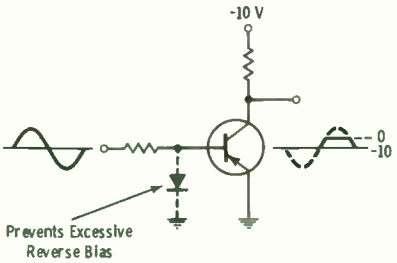


Fig. 9-14. Circuit diagram of transistor clipper.

across R_L. The example given is the "keying out" which occurs for horizontal sync pulses during the 9-line vertical-sync interval.

Fig. 9-14 shows a basic transistor clipper. We will often find a diode (shown by dash lines) connected from base to ground to prevent the base-emitter junction from receiving excessive reverse bias from the input signal swing. If we lose a transistor in this type of circuit, we should always check the diode to be sure it has not opened.

9-5. CLAMPERS

Clampers are switch-operated devices which are timed to refer either sync-tip or back-porch level to a reference voltage (either ground or a regulated voltage displaced from ground).

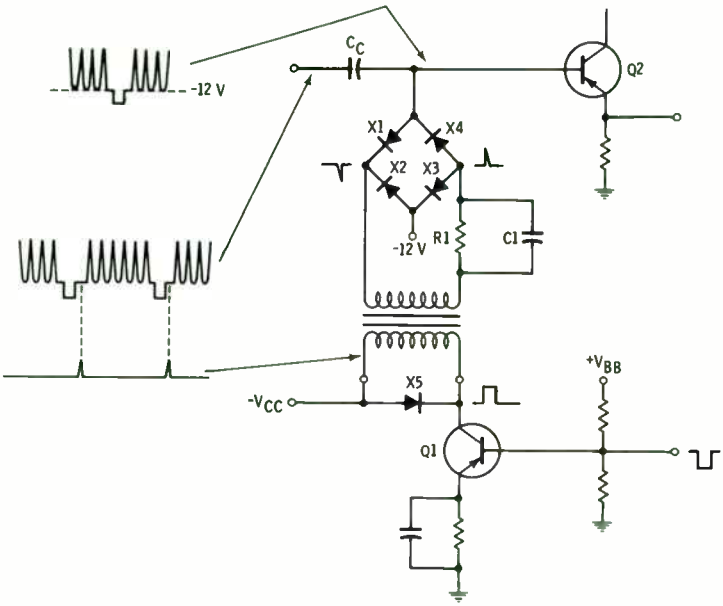


Fig. 9-15. Clamping circuit with pulse transformer.

Fig. 9-15 illustrates the pulse-transformer type of clamping circuit. The base of clamp driver Q1 receives a sharp negative pulse to drive it from cutoff to saturation. The sudden pulse of collector current through the primary of the transformer "rings" this circuit due to the inductive "kickback." But after the first positive excursion, diode X5 shorts out the primary when the collector attempts to swing negative. Note that this polarity would be reversed if an npn transistor is used. Note also the polarity of the resulting pulses on the secondary, and how this results in forward-biasing of the quad diode circuit. This forward-biasing closes the "switch," and −12 volts is applied to the base of Q2. Coupling capacitor C_c is always small, since it must be charged or discharged quickly (during the approximately 1.5-μs duration of clamping) to the reference −12 volts. The R1C1 time constant must be long compared to a line interval so that the charge on C1 will hold the switch open (nonconducting) between pulses during the active line (video) interval. As a rule of thumb, the pulse amplitudes at each end of the quad are at least 3 times the video signal (peak-to-peak) at the clamped base. This relationship will be true for any type of driven clamping circuit.

Now let us go through the circuit of Fig. 9-16 to prove that we can rapidly analyze a chain of pulse circuitry by applying the fundamentals we have learned. We will see that we can determine what to expect in waveforms if the circuit is functioning as intended.

Since this is a "back-porch" clamper, we know that clamping pulses must occur after the trailing edge of horizontal sync. If we correlate the circuit of Q1 with Fig. 9-5, we know how the delay is obtained.

NOTE: Since it is conventional to show grounded circuits at the bottom of a schematic, we will almost always see the "inverted" type of drawing when the emitter rather than collector is connected to the voltage supply.

Note that Q1 is actually a form of boxcar (saturated), since the emitter is returned directly to −20 volts and the base is grounded through its resistor. The delayed negative base pulse drives Q1 toward cutoff, but the Q1 collector is directly coupled to the Q2 base. The positive-going pulse excursion at this point is "caught" by the −12 volt base-emitter clamp of Q2, and can go no further positive.

We know that prior to the pulse Q1 is saturated and its collector is at −20 volts (switch closed). At this same time, since the Q2 emitter is at −12 volts and its base is at −20 volts, Q2 is cut off. The positive pulse at the Q2 base drives it on, and since there are no limiting diodes and no emitter resistance for self-bias, Q2 will saturate. So we would expect at the Q2 collector a pulse extending from 0 volts (cutoff) to −12 volts (saturation). The unbypassed emitter resistance of phase-splitter Q3 tells us that the input impedance of Q3 will be quite high (very low base current), so we would expect about the same pulse amplitude directly at the Q3 base.

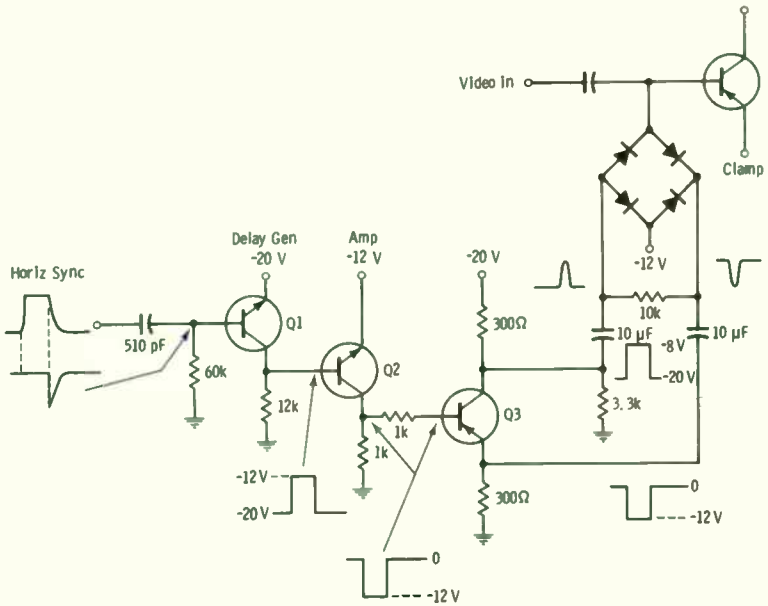


Fig. 9-16. Circuit of back-porch clamper.

Now analyze Q3, first the interval between pulses, then the pulse interval. Between pulses, the Q3 base is at essentially zero voltage, so the transistor is cut off. During the pulse interval, since the Q3 emitter and collector loads are identical, we will expect essentially unity gain. Therefore, we would expect the Q3 emitter pulse to extend from 0 (cutoff) to −12 volts (unity gain).

The emitter current at the −12 volt peak is:

$$I_e = \frac{V}{R_e} = \frac{12}{300} = 40\text{ mA}$$

For a quick analysis, assume the same collector current as emitter current; the collector signal-voltage swing from the pulse is:

$$V_c = (0.04)(300) = 12\text{ volts}$$

Then we would expect the collector pulse to swing up 12 volts from −20 volts (cutoff), or to −8 volts.

In practice, we realize that the collector current is slightly less than the emitter current ($I_c = \alpha I_e$), and for this reason, we will normally find the collector load resistor of a clamp driver slightly higher in value than the emitter resistance. For a 300-ohm emitter resistance, the collector load would usually be around 330 ohms. Thus the slightly smaller collector-current swing develops a voltage swing equal to that at the emitter.

The above analysis should serve to emphasize an important servicing technique: Always use the dc-amplifier position during scope checks. This mode tells us considerably more about circuit function than the ac-coupled position. For large-signal operation, this method is very convenient.

EXERCISES

Q9-1. See Fig. 9-2. The amplitude of the input pulse is over 10 volts, C is 1370 pF, and R_B is 5000 ohms. What output pulse width would you expect, approximately?

Q9-2. See Fig. 9-3. The input pulse amplitude is 5 volts, C is 1000 pF, and R_B consists of two resistors, a fixed 2.2k and a variable 5k. What approximate minimum and maximum pulse widths would you expect for the output pulse?

Q9-3. In any of the "boxcar" diagrams, if R_L is 1000 ohms and R_B is 100k, is the circuit a boxcar?

Q9-4. Where will you most likely find the complementary-symmetry emitter follower used?

Q9-5. In Fig. 9-7, if the composite video level falls in amplitude such that the sync region at the Q1 base is only about −0.6 to +0.6 volt, what will occur?

Q9-6. In the circuit of Fig. 9-11, is it necessary to have positive input pulses to turn the transistors off?

CHAPTER 10

Multivibrators

The multivibrator is a switching-type (nonsinusoidal) oscillator with which the reader should already be familiar. However, we should review briefly the definitions of three basic types.

The monostable multivibrator has only one stable condition; this is the quiescent operating condition. When the circuit is triggered by an external pulse, the operating point is shifted to an opposite condition (cutoff or conducting). The circuit remains in this condition for a time depending upon the time constant of an RC network, and then the operating point shifts back to the original stable mode. The circuit remains in this mode until another trigger is applied; hence it is often termed a "one-shot," "single-shot," or "single-swing" multivibrator (or MV for short). This operation is also referred to as *flip-flip* action; a trigger is required to *flip* the state of the circuit, which automatically *flips* back to the original stable state.

A bistable multivibrator has two stable states, one of which is the quiescent operating condition. When a trigger pulse arrives, the operating point moves from this stable condition to the other stable state, which is also held by the quiescent operating point. The circuit remains in this second state until another trigger pulse is applied; the circuit then returns to the original stable condition. This operation is referred to as *flip-flop* action; two trigger pulses are required, one to *flip* the state of the circuit and the second to *flop* the circuit back to the original state. Since one output pulse results from two triggers, this multivibrator is also termed a binary (divide-by-two) circuit.

An astable multivibrator is cross-coupled so that there is continuous regeneration; hence it is a "free-running" circuit, a continuous relaxation-type oscillator. It does not require a trigger to operate, but it can be *synchronized* to an external signal by application of a trigger derived from that signal.

10-1. THE MONOSTABLE MULTIVIBRATOR

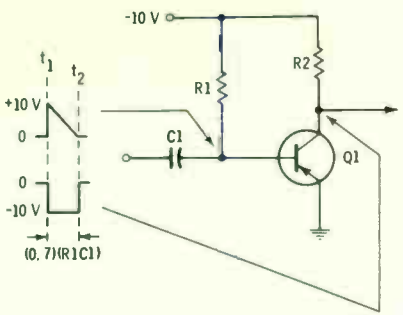
Fig. 10-1A shows the familiar boxcar circuit. Prior to t_1, Q1 is in saturation, and its collector is at zero potential. At t_1, Q1 is cut off, and the collector goes to −10 volts for the interval between t_1 and t_2. In Fig. 10-1B, we have a transistor held off by the reverse bias applied to its base. Therefore, the collector is at −10 volts until the arrival of a negative pulse of sufficient amplitude to overcome the reverse bias at the base terminal and turn the transistor on.

Now put parts A and B together to form the circuit of Fig. 10-1C. In the quiescent operating condition, Q1 is saturated. Since in this mode of operation the Q1 collector is at 0 volts, Q2 is cut off. At t_1, the collector of Q1 goes toward −10 volts. As soon as the Q1 collector voltage becomes large enough to cancel the reverse bias of Q2 (always less than the collector supply voltage of Q1), Q2 is turned on. A positive-going voltage now appears at the Q2 collector, so the leading edge of the trigger is fed back to the Q1 base; the action is reinforced, Q1 is driven completely to cutoff, and Q2 is driven into saturation. The circuit will remain in this condition until C1 is discharged through R1. Since the regenerative action resulted in an input pulse amplitude which must equal the supply voltage we will expect the pulse duration to be 0.7 times the product R1C1. (Review Chapter 9 if this is not clear.) When C1 becomes discharged, Q1 again enters saturation, and the resulting collector-voltage change cuts off Q2. The circuit is returned to the original stable mode and remains there until another trigger arrives.

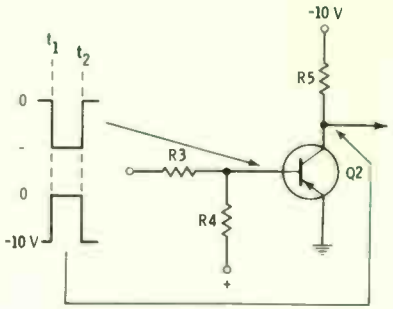
Note that in this circuit a trigger amplitude that is greater than the very small base-emitter forward voltage drop of Q1 is all that is required. (Bear in mind, however, that greater trigger *current* is required to turn off a *saturated* transistor than an *unsaturated* one.) When Q1 is driven toward cutoff, the resulting *regenerative action* results in an input pulse equal in amplitude to the supply voltage. So the trigger from the preceding stage can be well under the amplitude required to match the supply voltage, but the resulting pulse at the Q1 base will be very nearly equal to the supply voltage. Resistor R6 is used to provide isolation for the input trigger to prevent loading of the input by the Q2 circuit.

Now study Fig. 10-1D. The circuit is reversed, but the action is similar. The point to bear in mind is that if one side of a multivibrator is designed to be on by applied quiescent operating voltages, and the other side of the circuit either has zero bias or a reverse bias to hold it off, the circuit is a monostable multivibrator. It will not operate at all in the absence of trigger pulses. Also note that the trigger amplitude for the circuit of Fig. 10-1D must be sufficient to overcome the reverse bias present on the Q2 base.

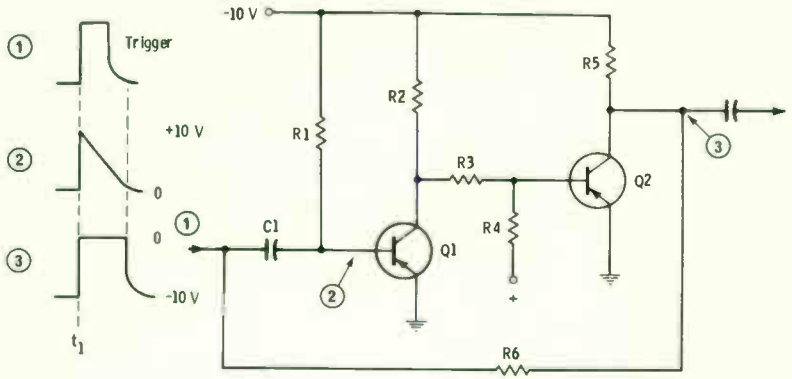
See Fig. 10-2. Fig. 10-2A shows the circuit of Fig. 10-1C redrawn, and Fig. 10-2B shows the same circuit except for npn transistors. In Fig. 10-2C,



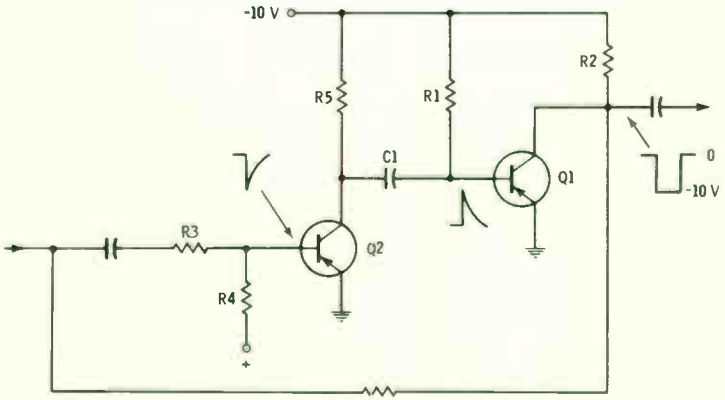
(A) *"Boxcar" circuit.*



(B) *Amplifier circuit.*

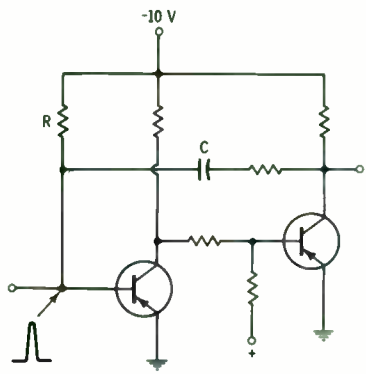


(C) *Monostable multivibrator.*

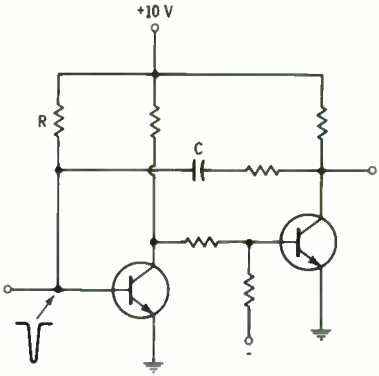


(D) *Alternate arrangement.*

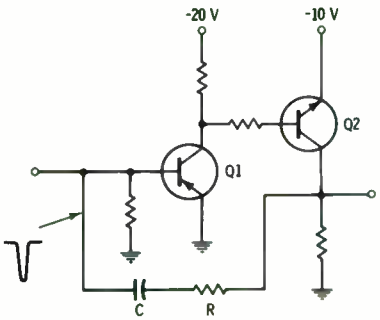
Fig. 10-1. Fundamentals of the monostable multivibrator.



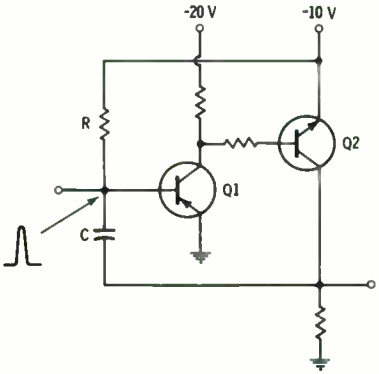
(*A*) *Pnp transistors.*



(*B*) *Npn transistors.*



(*C*) *Stable state: cutoff.*



(*D*) *Stable state: saturation.*

Fig. 10-2. Monostable multivibrators.

note the complementary-symmetry arrangement. Let us analyze this circuit before going on.

Here is the way to reason it out: First, what is the quiescent operating condition? Note carefully that two negative supplies are used, a −10 volt supply and a −20-volt supply. The base of Q1 is returned to ground (through a resistor), and there is nothing to turn this transistor on. The base of Q2 is connected to the Q1 collector, and the Q2 emitter is returned to −10 volts. For npn transistor Q2, the base must be positive relative to the emitter for conduction. Since Q1 is off, the Q2 base is at −20 volts, so this transistor also is off. The application of a negative trigger to the base of Q1 turns Q1 on. The resulting collector current will cause a voltage drop across the collector load, and the base of Q2 will go in the positive (ground) direction. When the base of Q2 reaches a voltage slightly positive relative to the −10 volt emitter potential, Q2 will turn on. The action is regenerative, causing *both* transistors to *saturate*. The circuit will

remain in this mode until C is charged through R, at which time both transistors return to the original stable mode—both transistors off.

The circuit of Fig. 10-2D is the same as that of Fig. 10-2C, except the Q1 base is now returned to the −10-volt supply. Again analyze the quiescent operating condition. Since Q1 is saturated, its collector (and the Q2 base) is essentially at ground potential. This makes the Q2 base more positive than its emitter, so Q2 is also in saturation. With the application of a positive trigger at the base of Q1, this transistor will be driven toward cutoff, and the collector voltage (Q2 base) will go more negative. The resulting positive-going swing at the Q2 collector is fed back to the Q1 base, and the regenerative action completely cuts off Q1, also cutting off Q2. The circuit will remain in this mode until C discharges through R, again causing Q1 (and hence Q2) to saturate. This is the original stable mode of operation. Both transistors remain in saturation until the arrival of another trigger pulse.

10-2. THE BISTABLE (BINARY) MULTIVIBRATOR

Figs. 10-3A and 10-3B show two identical circuits, not interconnected. From the base voltage-divider arrangement, it is obvious that each circuit would be conducting. (The base voltage is a little less than ½ of the −25-volt supply voltage, in a forward-bias polarity.) Analyze the two extremes of operation as follows.

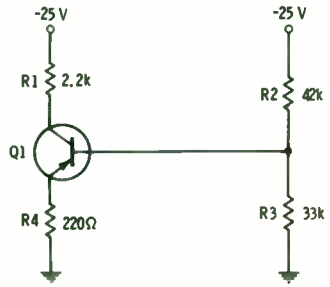
Saturation: Since the emitter resistance is $\frac{1}{10}$ of the collector resistance, the voltage at the emitter would be about −2.5 volts. Since there is negligible voltage drop across the transistor in saturation, the voltage at the collector is also approximately −2.5 volts.

Cutoff: Suppose the transistor were driven to cutoff by some means. Then the collector voltage would be identical to the supply voltage (−25 volts), since there would be no collector current to drop the voltage.

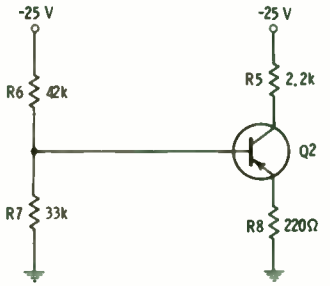
Now suppose we are able to switch the top end of R2 between the −25 volts and −2.5 volts. Further suppose we can make the emitter voltage of Q1 a constant −2.5 volts. With this condition, since the base of Q1 will be something under ½ of −2.5 volts (actually about −1 volt), the base is positive relative to the emitter, and the transistor cannot conduct.

Fig. 10-3C shows the individual circuits of Figs. 10-3A and 10-3B cross-coupled. The emitters of Q1 and Q2 are now returned to ground through a common resistor, R4. The "top" ends of R2 and R6 are each connected to the collector of the opposite transistor.

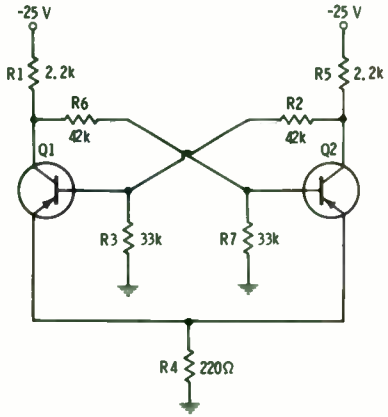
For analysis, since both circuits are identical, we must arbitrarily assume one transistor or the other in conduction. Let's assume Q1 is in saturation. Then its emitter and collector are at −2.5 volts, and the top of R6 is also at −2.5 volts. Note that since the emitters are now common, both emitters will be at −2.5 volts; consequently, Q2 is at cutoff, from our



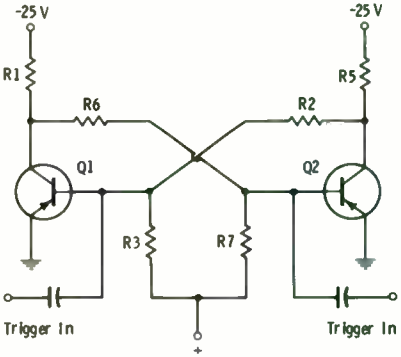
(A) Left half-circuit.



(B) Right half-circuit.



(C) Complete multivibrator.



(D) Use of base supply.

Fig. 10-3. Fundamentals of bistable multivibrator.

previous analysis. Since Q2 is cut off, its collector is at −25 volts, the top of R2 is also at −25 volts, and therefore Q1 is truly in saturation. The circuit is "flipped"; in the absence of any change, one transistor is saturated and the other is cut off.

Suppose now that base triggering is used. We know that a trigger applied to either base will start a chain reaction; since pnp transistors are being used, the trigger must be positive to the base of the on transistor, or negative to the base of the off transistor. Assume, for example, that a positive-going trigger is applied to the on transistor, Q1. Transistor Q1 will be driven toward cutoff, its collector will swing negative (less voltage drop across R1), and the base of Q2 will become more negative because of the cross coupling through R6. So Q2 starts to conduct; the drop through R5 swings the Q1 base positive (toward ground from −25 volts), further cutting off Q1. The regenerative action continues (even though the trigger pulse is very short in duration) until Q1 is completely cut off and Q2 is saturated. The circuit is "flopped"; the reverse

conditions from the previous mode now exist. In the absence of any change, the circuit will remain in this mode.

When the bases are returned to ground, a common emitter resistor must be used to make the emitter of the off transistor slightly negative. Thus the more positive base can keep the transistor cut off. The emitter resistor can be deleted when the bases are returned to a slight reverse bias, as shown by Fig. 10-3D. When we find this circuit, it works the same as that of Fig. 10-3C, except that the off transistor is held off by the external reverse bias.

In the common-emitter circuit of Fig. 10-3C, we may find emitter triggering used. When emitter triggering is not used, we will usually find emitter resistor R4 bypassed with a capacitor to avoid degeneration of the signal voltage.

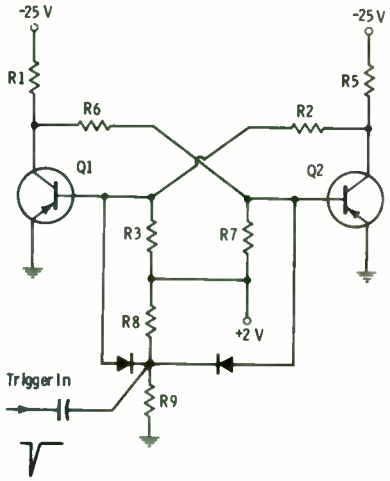
Further note that we used the example of a positive trigger pulse to the base of Q1 to turn the transistor off. To turn it back on again, a pulse of the opposite polarity would need to be applied to the *Q1 base*, or a pulse of the *same polarity* would need to be applied to the *Q2 base*. But suppose an emitter trigger is used. Assume Q1 is saturated (Q2 off), and the trigger is negative-going.

Since the base of Q2 is already positive relative to the emitter, a negative pulse at the emitter will only momentarily increase the reverse bias, and hence will not affect the operation of Q2. But Q1 is conducting because its base is negative relative to its emitter. When the negative trigger pulse arrives at the common emitter, Q1 is driven toward cutoff by the reduced forward bias, and regeneration takes care of the rest of the action. Transistor Q1 becomes cut off, and Q2 becomes saturated; the multivibrator has changed state.

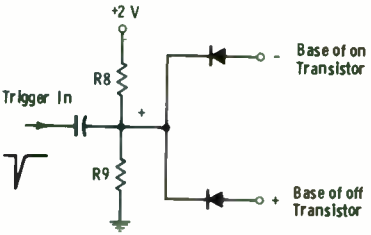
Now another negative pulse arrives. Since Q1 is already cut off, it is not affected. But Q2 is driven toward cutoff, and again regeneration causes the circuit to flop back to the original state. So a chain of negative pulses (or, as should be evident, a chain of positive pulses) is all that is required. No "steering" of pulses with regard to polarity is required in emitter triggering. The negative emitter pulse has no affect on the off transistor but affects the on transistor. If the pulses are positive, they will not affect the transistor which is already on, but will affect the off transistor. Remember also that this entire description concerned pnp transistors. For npn transistors, all polarities are reversed. Be sure to visualize the action for npn bistable multivibrators. Practice is included in the exercises at the end of this chapter.

Observe again Fig. 10-3D. A trigger at the base of Q1 changes the state of the multivibrator. To change the state again, a trigger of the opposite polarity at the Q1 base would be required, or a trigger of the same polarity at the Q2 base. But we will normally be concerned with a given polarity of trigger pulses for a bistable multivibrator, so let us see how this is done.

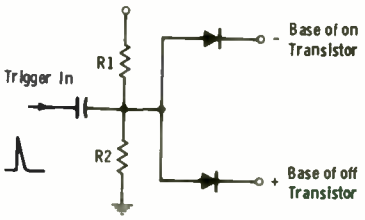
See Fig. 10-4A. This bistable multivibrator is identical to the circuit of Fig. 10-3D except for the method of triggering. Negative pulses from one input source are applied to the bases of both transistors. Since this is base triggering for pnp transistors, a negative pulse will drive the off transistor on. See Fig. 10-4B for analysis. Resistors R8 and R9 form a voltage divider from the +2-volt reverse-bias supply so that the cathodes of the diodes are at a slight positive (reverse) potential. The base of whichever transistor is on will be negative, so the corresponding diode is reverse biased, and this circuit remains open (no effect.) The base of the off transistor is held positive by the reverse-bias supply, so its diode is turned "on" by the negative pulse. Hence, the off transistor receives the negative pulse, which turns it on. Regeneration completes the action; the circuit flips and reverses polarity of the output voltage. The next negative pulse flops the circuit back to the original state. The diodes are termed "steering diodes" for obvious reasons.



(A) Multivibrator with steering diodes.



(B) Steering diodes for negative pulses.



(C) Steering diodes for positive pulses.

Fig. 10-4. Pulse-steering fundamentals.

For analysis of positive-pulse steering, see Fig. 10-4C, and use it in conjunction with Fig. 10-5. At the moment, we are confining the analysis of Fig. 10-5 to triggering only (diodes X5 and X6). This arrangement is always termed "collector triggering," but remember that the collector pulse is actually cross-coupled to the opposite transistor base. This cross-coupling is what does the job of changing the state of the multivibrator.

Since the trigger pulse is positive and the transistors are pnp, the trigger will drive the on transistor off. The steering is evident from Fig. 10-4C when we bear in mind that the base of the on transistor is tied to the collector of the off transistor (Fig. 10-5).

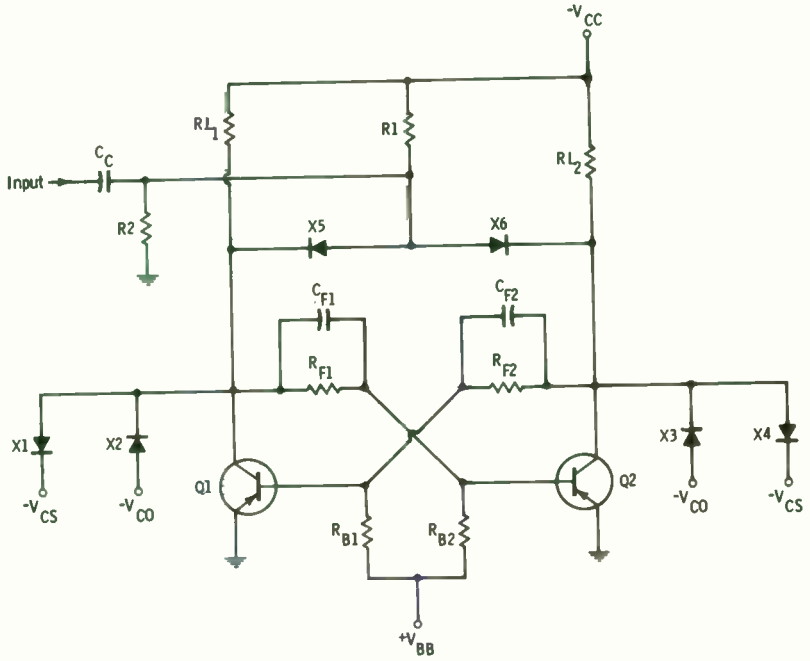


Fig. 10-5. Nonsaturating bistable multivibrator.

The circuit of Fig. 10-5 is a nonsaturating bistable multivibrator. When we see the additional diode arrangement shown, we will know the MV is held out of both saturation and cutoff by means of biased diodes. This decreases the storage time and increases the pulse-repetition-rate capability.

Diodes X1 and X4 with bias source V_{CS} are used for saturation clamping. Diodes X2 and X3 with bias source V_{CO} are used for cutoff clamping. The circuit is so designed that without clamping it would both saturate and cut off. Clamping the upper and lower limits of the output permits more reliable substitution of transistors when necessary. The analysis is as follows:

Saturation clamping: Collector diodes X1 and X4 have their cathodes returned to a slight negative voltage, for example −2 volts. When the respective transistor is not in saturation, the anode of the diode is considerably more negative than the cathode, and the diode is effectively an open circuit. When the transistor is driven toward saturation, the voltage at the collector attempts to reach ground potential (more positive than the base) and forward-bias the base-collector junction (the required condition for saturation). But as soon as the collector reaches a voltage slightly less negative than the diode cathode potential, the diode becomes forward biased, and the collector is held at the V_{CS} supply voltage. Thus the transistor cannot saturate.

Cutoff clamping: Diodes X2 and X3 have their anodes returned to a reverse bias which is somewhat less than the collector supply voltage. When the transistor nears cutoff, the diode is forward biased, and the collector is held at $-V_{CO}$. This action prevents the transistor from being cut off.

NOTE: Clamping diodes hold the operation in the more linear portion of the output characteristic curve. Thus the average power dissipation is increased, and to avoid transistor damage the designer must choose a loadline such that operation of the circuit falls within the maximum permissible power dissipation curve.

Fig. 10-6 illustrates what a binary circuit does. Note that binary 1 has one output pulse for every two input pulses. Then binary 2 again has one output pulse for every two pulses from binary 1. So the output of binary 2 is at one-fourth of the original frequency. Stated another way:

$$\text{Total Division} = 2^n$$

where,

n is the number of binary scalers (bistable multivibrators).

We will see in Chapter 14 how a series of binaries can be made to count an *odd* number, such as the 525 count required in sync generators.

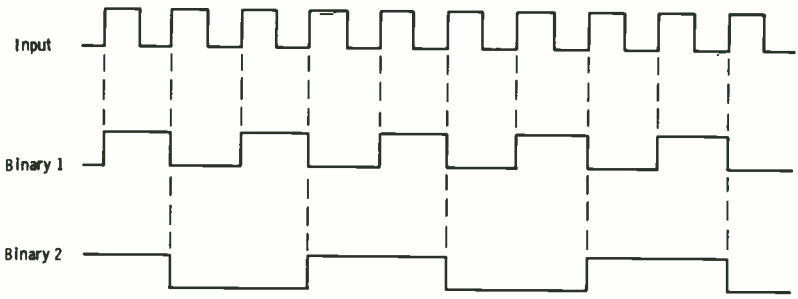


Fig. 10-6. Waveforms of binary circuits.

Although they have been omitted from most of the illustrations of multivibrators in this chapter, we will normally find small capacitors across the coupling resistors between transistors. These capacitors sharpen the wavefront for more rapid switching.

10-3. THE ASTABLE MULTIVIBRATOR

The astable multivibrator has no stable state; it changes state in a continuous (free-runing) manner because of its own cross-coupling. It also can be "synchronized" with an external signal. If its built-in time constant is made much longer than the time period of the synchronizing frequency, the circuit will synchronize to a subharmonic of that frequency, just as its electron-tube counterpart does.

Most transistor astable multivibrator circuits are counterparts of circuits using electron tubes. For example, the emitter-coupled transistor multivibrator is analogous to the cathode-coupled electron-tube multivibrator, and the collector-coupled transistor multivibrator (Fig. 10-7) is analogous to the plate-coupled electron-tube multivibrator. Since most multivibrator circuits function similarly, only the collector-coupled transistor multivibrator will be discussed here. The circuit description and Figs. 10-7 and 10-8 are taken from Department of the Army Technical Manual TM 11-690.

The basic collector-coupled transistor multivibrator of Fig. 10-7 is a two-stage resistance-capacitance coupled common-emitter amplifier with the output of the first stage coupled to the input of the second stage and the output of the second stage coupled to the input of the first stage. Since the signal in the collector circuit of a common-emitter amplifier is reversed in phase with respect to the input of that stage, a portion of the output of each stage is fed to the other stage in phase with the signal on the base. This regenerative feedback with amplification is required for oscillation. Bias and stabilization are established identically for both transistors.

Because of the variation in tolerance of the components, one transistor will conduct before the other or will conduct more heavily than the other. Assuming transistor Q1 is conducting more heavily than transistor Q2, more current (I_{b1} in Fig. 10-8) will be present in the base circuit of transistor Q1 than in the base circuit of Q2. Collector current I_{c1} in transistor Q1 increases rapidly, causing collector voltage V_{c1} (the voltage at the junction of R_{C1} and R_{F1}) to decrease (become more positive). This increasing positive voltage is applied through capacitor C_{F1} to the base of transistor Q2.

As base voltage V_{b2} of transistor Q2 becomes more positive, the forward bias decreases, resulting in a rapid decrease in base current I_{b2} and collector current I_{c2} in transistor Q2. Collector voltage V_{c2} (the voltage at the junction of R_{C2} and R_{F2}) becomes more negative. This negatively

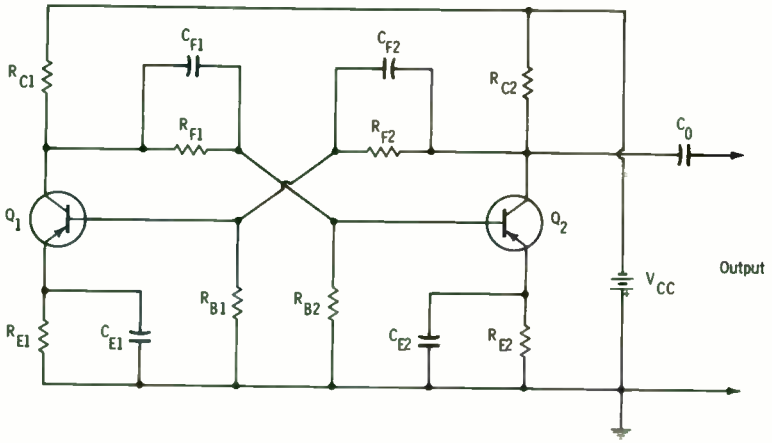


Fig. 10-7. Circuit of astable multivibrator.

increasing voltage is fed back through capacitor C_{F2} to the base of transistor Q1, increasing the forward bias.

The process just described continues until a point is reached where base voltage V_{b2} of transistor Q2 is made so positive with respect to the emitter that transistor Q2 is cut off (reverse bias is applied) and transistor Q1 is saturated (total dc voltage V_{cc} appears across resistor R_{C1}). That is, the current through transistor Q1 increases steadily as the current through transistor Q2 decreases steadily until transistor Q2 is cut off. Point A in Fig. 10-8 represents this action. The entire action happens so quickly that capacitor C_{F1} does not have a chance to discharge, and the increased positive voltage at the collector of transistor Q1 appears entirely across resistor R_{B2}.

During the period from A to B (Fig. 10-8), collector current I_{c1} and collector voltage V_{c1} remain constant, and capacitor C_{F1} discharges through

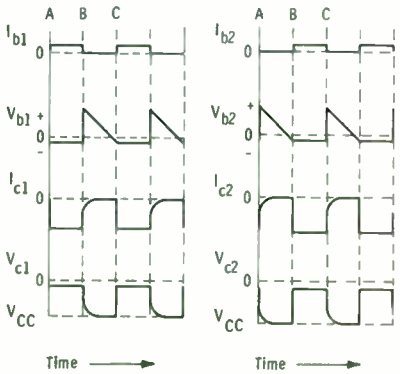


Fig. 10-8. Waveforms of astable multivibrator.

resistor R_{F1}. As C_{F2} discharges, more of the previously increased positive voltage at the collector of Q1 appears across C_{F1} and less across R_{B2}. Consequently, the reverse bias on the base of Q2 decreases. This action continues until the time at point B is reached and forward bias is re-established across the base-emitter junction of Q2.

Transistor Q2 conducts. As collector current I_{c2} in Q2 increases, collector voltage V_{c2} becomes less negative, or more positive. This voltage, coupled through capacitor C_{F2} to the base of transistor Q1, drives the Q1 base more positive and causes a decrease in current through Q1. The resulting increased negative voltage at the collector of Q1 is coupled through capacitor C_{F1} and appears across resistor R_{B2}. The collector current of Q2 therefore increases. This process continues rapidly until Q1 is cut off. Transistor Q1 remains cut off (and transistor Q2 conducts) until capacitor C_{F2} discharges through resistor R_{F2} enough to decrease the reverse bias on the base of Q1 (time C, Fig. 10-8). The entire cycle is then repeated.

The oscillating frequency of the multivibrator is usually determined by the values of resistance and capacitance in the circuit. In the collector-coupled multivibrator of Fig. 10-7, collector loads are provided by resistors R_{C1} and R_{C2}. Base bias for transistor Q1 is established through voltage-divider resistors R_{B1} and R_{F2}. Base bias for transistor Q2 is established through voltage-divider resistors R_{F1} and R_{B2}. Stabilization is obtained with emitter swamping resistor R_{E1} for transistor Q1, and resistor R_{E2} for transistor Q2. Emitter capacitors C_{E1} and C_{E2} are ac bypass capacitors.

The output signal is coupled through capacitor C_o to the load. The output waveform, which is essentially square, may be obtained from either collector (but with opposite polarities). To obtain a sawtooth output, a capacitor is usually connected from collector to ground for development of the output voltage.

If the time constants for both transistors are the same, a "symmetrical" square wave results. If the time constants differ, an "asymmetrical" wave is obtained.

NOTE: The multivibrator may be modified to produce a sinusoidal output wave. This is accomplished through the connection of a parallel-tuned circuit between the base electrodes of the transistors. The square-wave output can also be fed to a filter circuit for the purpose of obtaining a sine wave.

EXERCISES

Q10-1. Refer to Fig. 10-1D. The value of C1 is 680 pF, and R1 is 22k. What is the approximate pulse duration at the output?

Q10-2. In any multivibrator circuit using transistors, is it possible for both transistors to be off or on simultaneously and still function properly?

Q10-3. See Fig. 10-2A. The value of C is 1400 pF, and R is 20k. What is the maximum trigger rate you would expect?

Q10-4. For the same conditions as in Q10-3, what trigger repetition rate would produce essentially a square-wave output?

Q10-5. What is the purpose of the common emitter resistor (R4) in Fig. 10-3C?

Q10-6. Assume the circuit of Fig. 10-3C is to be designed for npn transistors, with supply polarities opposite to those shown. What effect would negative trigger pulses to the common emitter have?

Q10-7. What is the purpose of R8 and R9 in Fig. 10-4A?

Q10-8. You have a series of three binary stages with a 240-Hz input. What is the output frequency?

CHAPTER 11

Practice Problems in Pulse Circuitry

The best way to learn about pulse circuits is to build some and experiment with them. This chapter provides a series of practice problems that will help in gaining experience with these circuits.

11-1. EXPERIMENTS

Parts required for building the circuits of this chapter were included in the parts list given at the beginning of Chapter 7.

Saturation Experiment

Make the hookup of Fig. 11-1A using a 2N404A. Then follow the procedure outlined in the following eleven steps.

Step 1—Adjust R1 to its maximum value of 100k. Measure the voltage drop across R_L by using the voltmeter in position 1. This is V_{RL}. Record this value in the table of Fig. 11-1B.

Step 2—What is the collector current (I_C)? Record this in the table.

Step 3—Measure V_{BE} by using position 2. Record this.

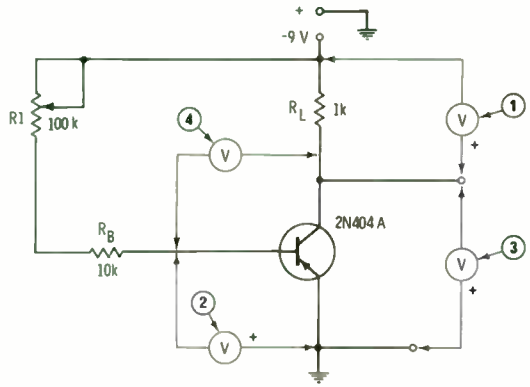
Step 4—Measure V_{CE} (position 3). Record this.

Step 5—Measure V_{CB} (position 4). Record this.

Step 6—Calculate and record h_{FE} for this condition.

NOTE: The measurements with R1 = 100k should reveal typical "class-A" linear operation. Assuming this is true, can you calculate theoretically what the above readings should be? How closely do your theoretical calculations compare with your actual voltmeter readings?

Step 7—Leave the voltmeter in position 4. Decrease the value of R1 until V_{CB} just drops to 0 volts. In what condition have you placed the transistor?



(A) Diagram of circuit.

Condition	V_{RL}	I_C	h_{FE}	V_{BE}	V_{CE}	V_{CB}
R1 = 100k						
R1 adjusted for V_{CB} = 0 volts R1=						0
R1 adjusted for V_{CB} = +0.1 volt						+0.1
R1 shorted (R_B = 10k)						

(B) Table for results.

Fig. 11-1. Transistor saturation experiment.

Step 8—Without disturbing its setting, disconnect R1 and measure its resistance with the ohmmeter. Record this value just below the tabulated condition "R1 adjusted for $V_{CB} = 0$ volts."

Step 9—Reconnect R1, take the required measurements, and fill in the remainder of this line of the table.

Step 10—With the voltmeter in position 4, decrease R1 still further until V_{CB} becomes +0.1 volt (collector positive relative to base). Take the required readings and fill in the next line of the table.

Step 11—Rotate R1 to zero resistance. Fill in the bottom line of the table. What kind of curve have you traced in these 11 steps?

Now let's go back over these steps immediately for a check.

Step 1—A typical reading for V_{RL} is 4.4 volts. If you had assumed class-A operation, you would have expected 4.5 volts (one-half of V_{CC}).

Step 2—Calculate I_C by Ohm's law: $I_C = V_{RL}/1k = 4.4/1000 = 4.4$ mA. If you were following through on a theoretical analysis, your collector current would have been $4.5/1k = 4.5$ mA.

Step 3—This is a germanium transistor, with a typical reading (on the one used for this experiment) of 0.18 volt. For theoretical analysis, you would assume 0.2 volt (base negative relative to emitter).

Step 4 —The reading here was 4.4 volts with a 20,000-ohms/volt meter. Remember that you are measuring relatively low voltages across a very high impedance. In theoretical analysis (which is really more accurate than actual measurement) you would have assumed 4.5 volts. Obviously the total V_{CC} is 9 volts, so with 4.5 volts across R_L, you would have $9 - 4.5 = 4.5$ volts for V_{CE}.

Step 5—Typical reading here with a 20,000-ohms/volt meter is -3.2 volts. Again, remember you are measuring across the very high resistance of a reverse-biased junction. How would you calculate what the voltage difference should be? You know the collector-to-emitter voltage is 4.5 volts (theoretical value). Also, the base-emitter voltage drop is about 0.2 volt. So the collector-to-base voltage should be $4.5 - 0.2 = 4.3$ volts, approximately.

Step 6—First calculate the base current: $I_B = V/R = 9/110k = 0.08$ mA (approx). Then $h_{FE} = I_C/I_B = 4.5/0.08 = 56$ (approx).

Step 7—You have placed your transistor "on the verge" of saturation. Remember that when the transistor is truly in saturation, the collector-to-base junction as well as the base-emitter junction is forward biased. What you have done here is to increase I_B to the point of saturation of collector current.

Step 8—A typical reading here is 36k for R1.

Step 9—Typical values are:

$V_{RL} = 8.8$ V

$I_C = 8.8$ mA (calculated)

$h_{FE} = 44$ (calculated)

$V_{BE} = 0.2$ V (slightly increased at higher base current)

$V_{CE} = 0.2$ V (same as V_{BE})

Step 10—The transistor is now in saturation. Typical readings:

$V_{RL} = 8.85$ V

$I_C = 8.85$ mA

$V_{BE} = 0.2$ V

$V_{CE} = 0.15$ V (Note that this is less than V_{BE}, another feature of "saturation.")

Step 11—The transistor is now in "hard saturation." Typical readings:

$V_{RL} = 9$ V

$I_C = 9$ mA

$V_{BE} = 0.2$ V

$V_{CE} = 0.05$ V (practically zero).

Naturally, h_{FE} is fixed at $R_B/R_L = 10k/1k = 10$; or $I_C/I_B = 9/0.9 = 10$.

The kind of curve you have traced is similar to that of Fig. 4-4B, from point C to point B on the load line, that is, from midpoint operation (class-A) to the saturation level.

In Step 7, you found the limit of base current beyond which any further increase will not increase the collector current significantly. This is the "verge of saturation," and any input signal existing at this point would already start to be "compressed." In Step 8, you found the total base resistance to be 36k + 10k = 46k. So the base current is:

$$I_B = \frac{9}{46k} = 0.2 \text{ mA (almost)}$$

You can check this value by measuring the voltage drop across the 10k resistor (R_B), where you will find about 2 volts.

Overdriven-Amplifier Experiment

You can check the foregoing results quite readily by applying a sine wave as in Fig. 11-2A. Use 1000 Hz, and adjust the input signal to 4 volts peak-to-peak. As the signal increases from zero to plus 2 volts, the output should clip. As the signal swings from zero to minus 2 volts, the output should again clip. Verify this by observing the output signal on an oscilloscope (waveform 1). You use a sine wave instead of a square wave so that you can see the transfer characteristic at any instantaneous amplitude.

Next, increase the input signal to 10 volts peak-to-peak, and you will see the effect of "hard saturation" (waveform 2). The sine wave is converted to a square wave, and the fast off-on operation of the transistor can be seen. The 10k resistance of R_B isolates the sending-end impedance from the extreme change of transistor input resistance, between the "off" and "on" states, and it provides a current-limiting resistance for the base-emitter junction.

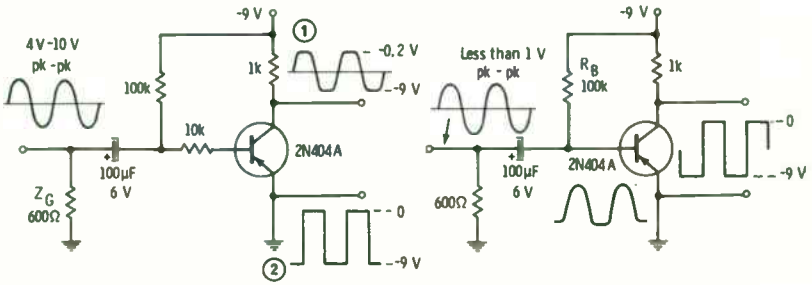
In Fig. 11-2B, the 10k resistor is deleted, and I_B is supplied by the 100k resistor. Note how extremely low the input signal can go to obtain a very good square wave at the output. Biased in this manner, the transistor saturates as soon as the base-emitter junction current increases slightly. As soon as the current swings slightly lower than the quiescent value, the transistor cuts off. Remember that for linear operation, this circuit would see signals in the millivolt range, not the volt range. You are now looking at "large-signal" applications.

With the hookup of Fig. 11-2C, in the absence of any signal the transistor is cut off. Now follow these steps:

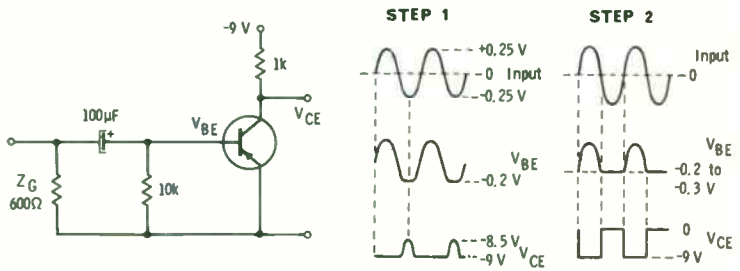
Step 1—Apply a 0.5-volt (peak-to-peak) sine-wave signal from the generator. Note that V_{BE} on the scope begins to show a slight clipping

at about −0.2 volt on the negative-going peak. (Do you recognize the base clamp?) Then observe the output signal (V_{CE}) and note that the transistor barely begins to conduct at this point.

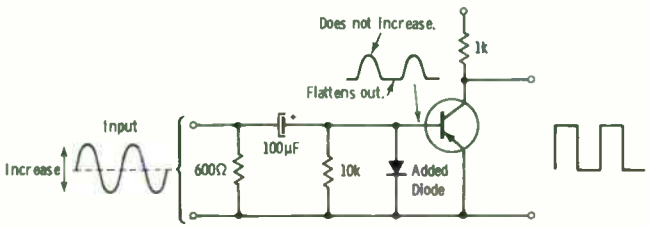
Step 2—Gradually increase the input signal while observing the output on the scope. Increase the generator gain until the transistor is operated as a switch by the sine wave (square-wave output). Now observe V_{BE} on the scope, and note that the negative excursion of the sine wave is still clamped at about −0.2 to −0.3 volt (dc position of scope). The "valley," however, has now broadened to cut off the entire negative excursion below the clamp point.



(A) Resistor in base lead. *(B) No base-lead resistor.*



(C) Cutoff with no signal.



(D) Reverse voltage limited.

Fig. 11-2. Transistor circuits with sine-wave input.

These observations should strengthen your viewpoint that it is the base-emitter junction *current* that must cause the collector saturation current of 9 mA. Voltage V_{BE} cannot increase in the forward-bias direction beyond the base clamping point. (See Chapter 9.)

But also remember this: Every transistor has a maximum V_{BE} rating. In the case of the 2N404A, this rating is 25 volts. For a 2N404, the maximum V_{BE} is 12 volts. For a switching circuit, you can install a diode as in Fig. 11-2D to prevent the positive swing from exceeding 0.6 to 0.7 volt for silicon or 0.2 to 0.3 volt for germanium. When you observe V_{BE} on the scope, note that as the input level is increased, the positive peaks of V_{BE} do not increase, but the negative excursion continues to flatten out from the base clamp (indicating increased base-emitter current). This action also prevents excessive charging of the transistor input capacitance in the reverse direction, decreasing turn-on time and storage time.

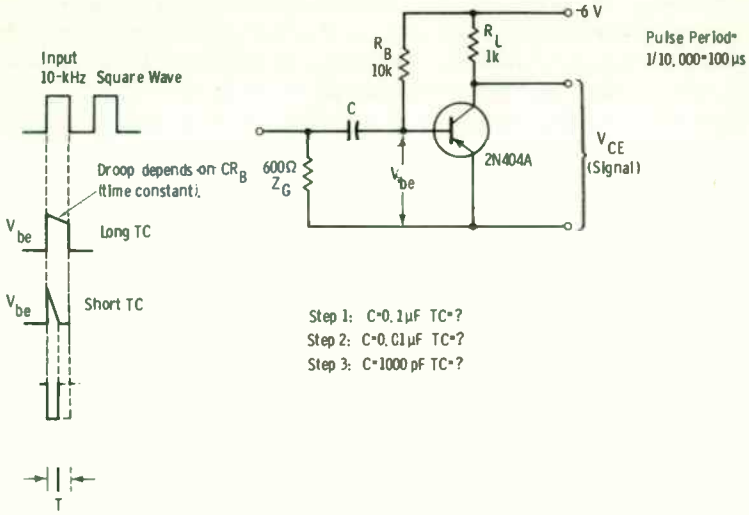
Time-Constant Experiment

Construct the circuit of Fig. 11-3A, and note that you will use a C of 0.1 μF in Step 1, 0.01 μF in Step 2, and 0.001 μF in Step 3. Feed a 10-kHz square wave to the input, using a signal amplitude equal to the supply voltage as the "high" setting. Fill in the time-constant (TC) values where indicated. (Note: It is most convenient to put R in megohms and C in pF to get the time constant in microseconds.)

Step 1—The 0.1-μF capacitance provides a long time constant. Why? Because the pulse period of the 10-kHz square wave is 100 microseconds. Since the TC in this step is 10 times this value (1000 μs), the V_{be} observed on the scope has very little droop. The V_{ce} output pulse is almost a faithful transfer of the input signal. While observing this output, decrease the input amplitude, and note that the output pulse has the same width and essentially the same amplitude over a reasonable range of input signal levels.

Step 2—The time constant now equals the input pulse period. With the input amplitude still "low," note that the negative-going output pulse is narrower than the input pulse and is asymmetrical. Now raise the amplitude of the input square wave and note that the output becomes essentially a square wave again. (If the action here is a mystery to you, carefully review Chapter 9.) In this step, with TC equal to the pulse period, insufficient "differentiation" takes place on the "high amplitude" input to narrow the output pulse.

Step 3—TC is now one-tenth of the input pulse. With the signal input still at "high" amplitude (equal to dc supply voltage), the negative peaks are narrow. What width should they be? (See if you can figure this before going ahead). If you figured correctly, you got $T = (0.7)(RC) = (0.7)(10) = 7$ μs.



(A) Circuit.

(B) Waveforms.

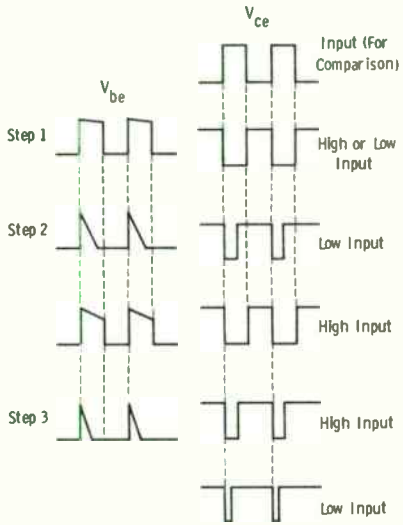


Fig. 11-3. Transistor pulse amplifier.

Remember the "tolerance" factor. (Tolerance is a beautiful word in explaining discrepancies!) Not only is the "K" factor approximate, but so also are the actual values of capacitance and resistance. If you are using a suitable oscilloscope, measure the actual width of the pulse. The main advantage of knowing these facts is in being able to design or analyze a circuit quickly (and, alas, approximately) so that you know *just about* what to expect without relying on waveform charts or guesses.

Now while observing the output waveform, reduce the input signal amplitude and note how the negative pulse narrows still further. You should be able to explain why. (If not, review Fig. 9-1C.)

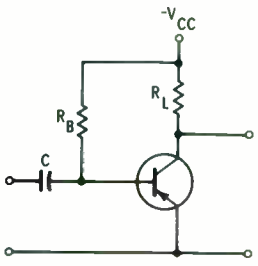
Of course, you should know why it is only the negative-going output pulse that is narrowed. (Another way of saying this is that the positive-going output pulse is broadened.) When the input pulse goes positive by just a few tenths of a volt, the transistor is driven from saturation to cutoff. At this instant, the output goes from (essentially) zero to −6 volts (a negative swing, hence phase inversion of signal). The capacitor starts to charge through R_B, but, due to the short time constant, it clamps at the point where the input junction again reaches forward bias before the input pulse ceases. The negative-going input pulse has no effect (pnp transistor), since the transistor is already in saturation.

11-2. PRACTICE PROBLEMS IN CIRCUIT ANALYSIS AND DESIGN

In the following paragraphs, we will go through some typical problems in pulse circuitry without actual construction. In these exercises, try to solve the problem on your own before going ahead to read the solution, which follows immediately after each problem.

Design of Boxcar Circuit

Fig. 11-4 should help you review the boxcar circuit, with the viewpoint of design. You select R_L by dividing the supply voltage by the desired saturation collector current. The value of R_B must be less than the



$R_L = V_{CC} / I_{sat}$

I_{sat} = Desired saturation collector current.

R_B = Less than minimum h_{fe} time R_L.
(For most applications, arbitrarily make $h_{fe} = 10$. Then make $R_B = 10R_L$.)

$T = 0.7R_BC$ (approximately), and therefore:

$C = T/0.7R_B$

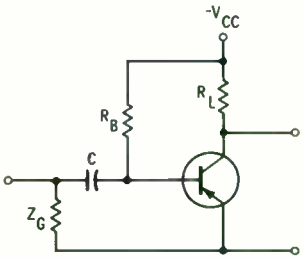
Fig. 11-4. Design of "boxcar" circuit.

minimum beta rating of the transistor times the R_L selected. For all practical purposes, you can make the value of h_{fe} an arbitrary 10, so $R_B = 10R_L$. The minimum beta of a transistor is usually around 20, so the figure of 10 is safe. You already know that T (duration of the output pulse) will be approximately $0.7CR_B$. Therefore $C = T/0.7R_B$, approximately.

Now, for practice in designing a boxcar circuit refer to Fig. 11-5 and go through the following steps.

Step 1—For the given data, specify the values of R_L, R_B, and C.

Step 2—Note that the only change made is in the desired saturation current. Specify the new values of R_L, R_B and C.



Step 1	V_{CC} = -6 V Output Pulse Width = 5 μs Collector Current = 6 mA (sat) R_L = ? R_B = ? C = ?
Step 2	V_{CC} = -6 V Output Width = 5 μs Collector Current = 3 mA (sat) R_L = ? R_B = ? C = ?

Fig. 11-5. Practice problem in "boxcar" design.

If you have designed correctly, you have the following results:

Step 1. $R_L = 1000$ ohms
$R_B = 10{,}000$ ohms
C = 714 pF (Closest standard value is 680 pF.)

Step 2. $R_L = 2000$ ohms
$R_B = 20{,}000$ ohms
C = 357 pF (Use 330 pF.)

NOTE: Always go to the next smaller value of capacitance that provides a standard value.

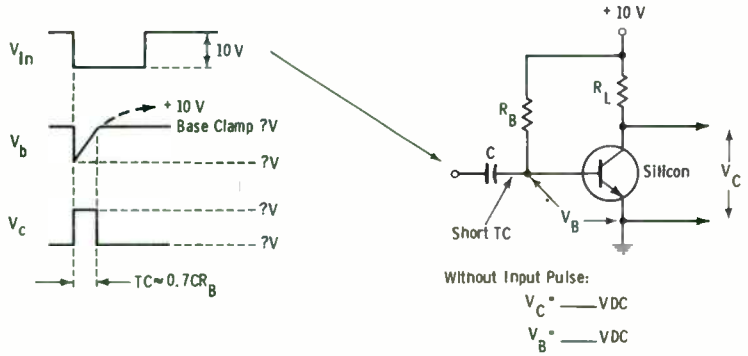
Question: How would you "trim" the time constant to get an exact specified pulse width? Answer: By using a variable resistance for R_B.

Problem 1 (Fig. 11-6)

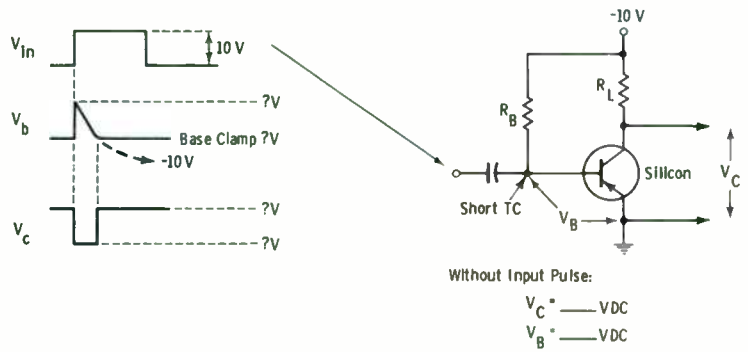
Problem, Fig. 11-6A—Note that this circuit has an npn silicon transistor and a short input time constant. First, fill in the values of dc collector and base voltages you would expect with no input signal, or with the input signal removed. Then, assuming V_{in} as indicated, fill in the values of the V_b and V_c signal voltages as they should check out on a scope operated in the dc position.

Solution, Fig. 11-6A—Since this is a "boxcar" circuit (ratio of R_B to R_L no greater than 20:1), you know the transistor is saturated without an input signal. Therefore, the dc collector voltage is about +0.1 volt, and the dc base voltage is about +0.7 volt. (In class-A operation, a silicon junction has a base-emitter voltage of about +0.6 volt, but in saturation, the higher base current produces a drop of about +0.7 volt.)

When the transistor is in saturation, capacitor C is essentially uncharged, since the transistor base is at +0.7 volt. So the "base clamp" voltage is



(A) Npn transistor.

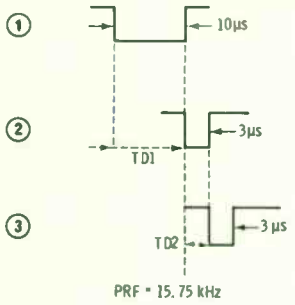


(B) Pnp transistor.

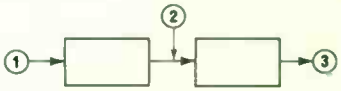
Fig. 11-6. "Boxcar" pulse circuits.

+0.7 volt. Since V_{in} is 10 volts peak-to-peak, the negative excursion cuts the transistor off, and the peak negative value of the V_b pulse is $-10 - (+0.7) = -9.3$ volts.

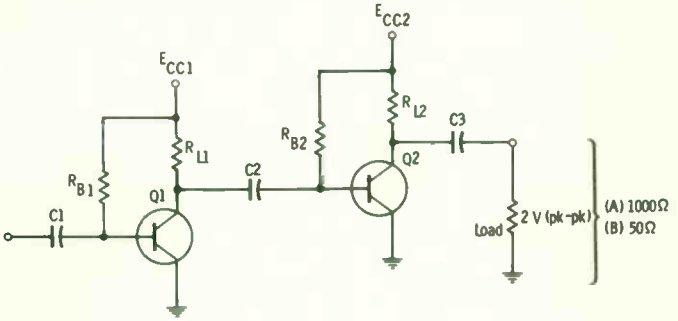
Before the negative signal arrived, V_c was at approximately +0.1 volt, so this is the value of the base line of the V_c output pulse. Since the negative excursion cuts the transistor off, V_c goes positive (no drop across R_L with no collector current), so the entire +10 volts of the supply appears at the peak of the output pulse.



(*A*) *Waveform requirements.*



(*B*) *Block diagram.*



(*C*) *Schematic diagram.*

Fig. 11-7. Circuit for pulse narrowing and delay.

Problem, Fig. 11-6B—This circuit has a pnp silicon transistor and a short input time constant. First, fill in the values of the dc collector and base voltages you would expect with no input signal. Then, assuming V_{in} as indicated, fill in the values of the V_b and V_c signal voltages as they should appear on a scope operated in the dc position.

Solution, Fig. 11-6B—With no input signal, the transistor is in saturation. Voltage V_C should be about -0.1 volt and V_B about -0.7 volt dc. Therefore the base line of the V_b waveform (base clamp point) is -0.7 volt. The positive pulse will peak at $+10 - 0.7 = 9.3$ volts.

The base line of the output pulse (V_c) is the saturation level of -0.1 volt. At cutoff (peak negative excursion), the full supply voltage of -10 volts prevails.

Note that, in every case, the actual peak-to-peak output pulse is the full supply voltage minus the small saturation voltage at the transistor collector.

Problem 2 (Fig. 11-7)

Problem—You have an input pulse (waveform 1 in Fig. 11-7A) from which you want to form a pulse at the trailing edge as in waveform 2. Then you want to take the second pulse and form another pulse (waveform 3) which occurs at the trailing edge of waveform 2 and has the same 3-μs pulse width.

The basic circuit arrangement will take the form of Fig. 11-7B. In this block diagram, the input pulse is applied at point 1, the first output pulse at point 2, and the second output pulse at point 3.

Next, draw the basic cascaded boxcar circuits as in Fig. 11-7C. Assuming E_{CC} is 10 volts of the required polarity, select the type of transistor (pnp or npn) required, and the values of resistors and capacitors required. Do this for two separate output load values, 1000 ohms and 50 ohms. The load must receive 2 volts (peak-to-peak) of signal in both cases.

Solution—If you are having a problem here, review Chapters 8 and 9. First of all, you should know that to delay a negative pulse, the transistor must be a pnp type, so draw in the emitter arrows accordingly, and mark the power supply "-10 volts." Now start backward, with the output load-current requirement to produce 2 volts of signal. With Q2 in saturation, the voltage across C3 is essentially zero, and this voltage cannot change instantaneously when Q2 cuts off. Therefore, immediately after cutoff of Q2, the entire 10-volt supply voltage must be divided between R_{L2} and the load. We want 2 volts across the load, so we want the charging current to be:

$$I = \frac{2}{1k} = 2\,mA$$

The current of 2 mA through R_{L2} must drop the remaining 8 volts, so:

$$R_{L2} = \frac{8}{2} = 4k, \text{or } 4000 \text{ ohms}$$

(It should be noted that C3 must provide a long time constant to prevent excessive droop in the output pulse.)

Now note from the pulse requirements that the output pulse (waveform 3) must have the same width as the pulse at the base of Q2. Therefore, you must use a long time constant for C2-R_{B2}, and when you think of a "long time constant," you mean one which is about 10 times the input pulse period. Since the PRF is 15.75 kHz, this period is 63.5 μs, and you need about a 600-μs time constant for C2-R_{B2}.

It is a good rule of thumb to make R_B about 10 times the collector load resistor, so you would give R_{B2} a value of about 40k. Now, since the time constant is in microseconds, put R in megohms to get C in pF:

$$C = \frac{TC}{R}$$

$$C2 = \frac{600}{0.04} = 15{,}000 \text{ pF, or } 0.015 \ \mu\text{F}$$

Now you have C2 = 0.015 μF, R_{B2} = 40k, and R_{L2} = 4k. The output pulse has the same width as the output pulse of the first stage, and it gives a 2-volt (peak-to-peak) signal in 1000 ohms.

The base current of the output stage (Q2) is one-tenth of the collector current. The collector current with Q2 saturated is 10/4k = 2.5 mA. Thus I_B = 0.25 mA, and the preceding stage (Q1) should supply at least twice this base current for good cutoff from saturation. This requirement will pose no problem at all, so you can go to the good standard value of 1k for R_{L1}. Then R_{B1} can be 10k, and you are ready to find the value of C1.

The product $C1R_{B1}$ must have a value such that (0.7)(RC) = 3 μs. Then:

$$C1 = \frac{3}{(0.7)(10k)} = \frac{3}{0.007} = 430 \text{ pF (approx)}$$

Now you have completed the design for a 1000-ohm load. How do the results change if the load is 50 ohms?

First, the load current becomes 2 volts/50 ohms = 40 mA. So now R_{L2} = 8 volts/40 mA = 200 ohms! You can see this affects the design considerably! Then R_{B2} must be fixed at no more than 20 times this value (to allow for minimum beta, unless you go to a very-high-beta transistor), so let R_{B2} = 4k. Then to maintain a long time constant, C2 must be:

$$C2 = \frac{600}{0.004} = 150{,}000 \text{ pF, or } 0.15 \ \mu\text{F}$$

The base current is one-twentieth of the collector current, or 2 mA. Will the 1k R_{L1} need to be changed? No, because the available peak-to-peak current swing is 10 mA, which is adequate. So the first stage need not be changed in this example. If you had used a higher value for R_{L1} (so that you would supply just sufficient current at the output-stage base

for cutoff at the original 0.25-mA base-current value), you would, of course, need to redesign the input stage.

It should be noted that a boxcar circuit does not normally feed a low-impedance circuit such as a 50-ohm line. Where this operation is required, the boxcar usually feeds the relatively high input impedance of an emitter follower which, in turn, feeds the low-impedance load.

Problem 3 (Fig. 11-8)

Problem—The boxcar circuit is normally a pulse-narrowing circuit. In Fig. 11-8 is a 20-microsecond trigger pulse which will be widened. What type of multivibrator is this? Can you draw the expected pulse outputs, and give the expected pulse widths?

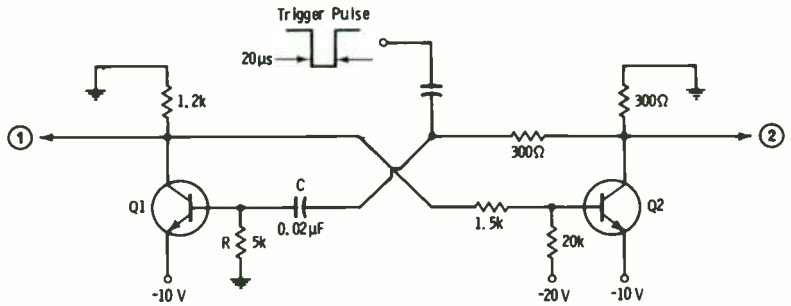


Fig. 11-8. Pulse-widening circuit.

Solution—You should recognize immediately that Q1 is in a boxcar circuit; it is saturated by the forward bias applied to the emitter (with base returned to ground through a resistor), and the ratio of base resistance to collector resistance is less than 5:1. Transistor Q2, as you should observe, is biased off, because the base of this npn transistor is more negative than the emitter. Therefore the circuit is a monostable multivibrator.

Prior to a trigger, capacitor C is charged to −1 volt because of the saturation of Q1. The negative trigger drives Q1 into cutoff and begins the timed cycle (unstable state). Transistor Q2 is driven to saturation by the positive-going pulse at the Q1 collector. The duration of this state is the time required by C to discharge toward ground through resistor R. As soon as the potential at the Q1 base is slightly positive relative to −10 volts, Q1 again saturates and cuts Q2 off. (Since the action is regenerative, the amplitude of the trigger pulse need be only sufficient to drive Q1 to cutoff.)

The duration of the unstable state is approximately $(0.7)(RC) = (0.7)(0.005)(20{,}000) = 70\ \mu s$.

The waveform at point 1 has a level prior to trigger of −10 volts. When Q1 cuts off (at time of trigger), the pulse rises toward ground

potential. Thus the waveform is a pulse with a base line at −10 volts and a peak at zero (ground) potential; it is a positive-going pulse with a duration of 70 microseconds. Waveform 2 is a pulse with its base line at 0 volts and its peak at −10 volts (negative-going pulse). It has the same duration as waveform 1.

Problem 4 (Fig. 11-9)

Problem—What type of multivibrator is shown in Fig. 11-9? Give times for a, b, and c on the waveform. What is the PRF?

Solution—You should recognize that this arrangement is simply two cross-coupled boxcar circuits forming an astable multivibrator. Since the time constants are equal, a symmetrical pulse output (square wave) will result. A transistor will be on or off for a time equal to (0.7)(C1R2) or (0.7)(C2R3). The duration in microseconds of each *pulse* is: (0.7)(10,000)(0.001) = (0.7)(10) = 7 μs (a or b on the waveform of Fig. 11-9). The duration of one complete cycle (leading edge of positive pulse to leading edge of next positive pulse) is (2)(7) = 14 μs (c of the waveform in Fig. 11-9).

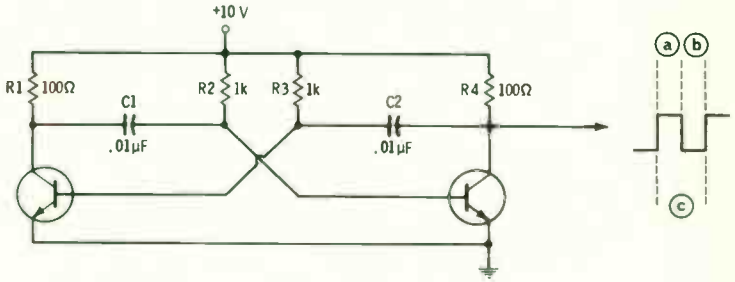


Fig. 11-9. Transistor multivibrator circuit.

The pulse repetition frequency is:

$$\text{PRF} = \frac{1}{\text{repetition time}} = \frac{1}{14\ \mu\text{s}} = 71.4\ \text{kHz}$$

The peak-to-peak voltage swing at the output (assuming a high-impedance load) is about 10 volts. The collector-current swing is 10/100 = 0.1A, or 100 mA.

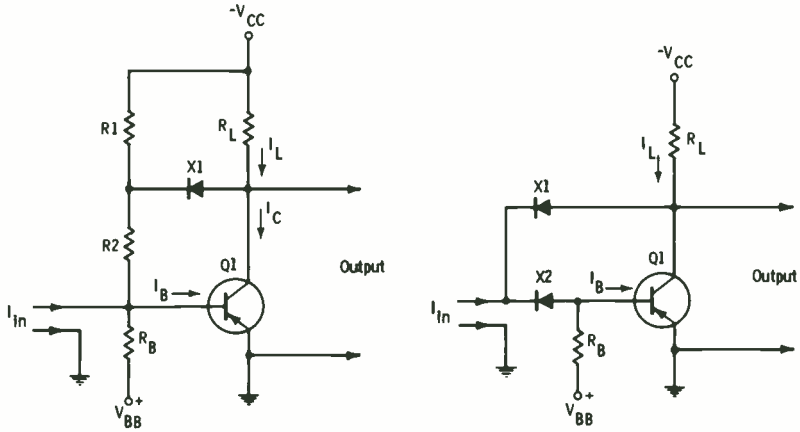
Problem 5 (Fig. 11-10)

Problem—Figs. 11-10A and 11-10B show pulse-amplifier circuits. What type are they, and how do the diodes function? What is the purpose of this type of pulse amplifier?

Solution—Fig. 11-10A shows an efficient type of pulse amplifier in which deep saturation and the resulting pulse widening and delay are

prevented. From your previous work, you should be able to analyze this circuit as follows:

In the cutoff condition of the transistor, diode X1 and the emitter-base junction of Q1 are reverse-biased by the voltage-divider network consisting of resistors R1, R2, and R_B. When supply voltages V_{CC} and V_{BB} are equal, the sum of the resistances of R1 and R2 is made slightly greater than the resistance of R_B. This provides the required initial reverse bias for the emitter-base junction. Resistor R1 is very much larger than resistor R2, the ratio of the two resistors being determined by the desired clamping voltage when the transistor is conducting.



(*A*) *One diode.* (*B*) *Two diodes.*

Fig. 11-10. Pulse-amplifier circuits.

Assume that an applied signal (I_{in}) drives the transistor to saturation. The potential at the junction of resistors R1 and R2 is negative and effectively fixed near the very low saturation voltage of the transistor used. The collector potential falls from its high negative value (V_{CC}) toward the value of the potential at the junction of resistors R1 and R2. During this period, diode X1 is nonconducting, and base current I_B is equal to the input current, I_{in}. Load current I_L is equal to collector current I_C and is the amplified driving current. When the collector potential falls just below the potential at the junction of resistors R1 and R2, diode X1 conducts. As input current I_{in} increases further, base current I_B remains essentially constant, and the excess current is shunted through resistor R2 and diode X1.

Dissipation of supply power in resistors R1 and R2 of Fig. 11-10A can be avoided by using double-diode clamping. In Fig. 11-10B diode X1 functions as a clamping diode. Forward-biased diode X2 is substituted for resistor R2 of Fig. 11-10A.

The emitter-base junction of Q1 is reverse biased by voltage V_{BB} through resistor R_B. Collector reverse bias is provided by battery V_{CC} through load resistor R_L. Diode X2 remains forward-biased throughout the functioning of the circuit. (A negative signal must be applied to the base to drive the transistor into conduction.) Generally, a germanium diode, with a low forward voltage drop, is used as the clamping diode (X1), and a silicon diode, with a slightly higher forward voltage drop, is used as the biasing diode (X2). For example, in a typical application, diode X1 provides a forward voltage drop of 1 volt, and diode X2 provides a forward voltage drop of 1.2 volts. This essentially maintains a reverse bias of 0.2 volt between collector and base of Q1 after clamping action takes place.

Circuit functioning is similar to that of the single-diode clamping circuit. All of input current I_{in} is applied to the base while diode X1 remains reverse-biased. This condition exists until load current I_L drops the collector potential just below the potential at the junction of diodes X1 and X2. (The base potential is more positive than the potential at this point by the value of the voltage drop across X2.) Diode X1 becomes forward biased and shunts the excess input current to the collector. The smaller voltage drop across X1 maintains the reverse collector-base bias at the difference between the forward voltage drops across diodes X1 and X2.

This circuit produces little output-pulse widening, and the maximum pulse repetition rate of the switching circuit is thereby increased.

CHAPTER 12

Special Applications and Special Transistors

In this chapter, we will cover some new circuits and special applications of circuits already studied.

12-1. THE SCHMITT TRIGGER

The Schmitt trigger is an emitter-coupled regenerative bistable circuit whose state depends on the *amplitude* of the input voltage. This circuit has no cross coupling from the output transistor back to the input transistor; the common emitter resistor is the only regenerative element used. The Schmitt trigger is widely used for pulse shaping (squaring sinusoidal or nonrectangular inputs), dc level detecting, and signal-level shifting, and sometimes as a counter circuit.

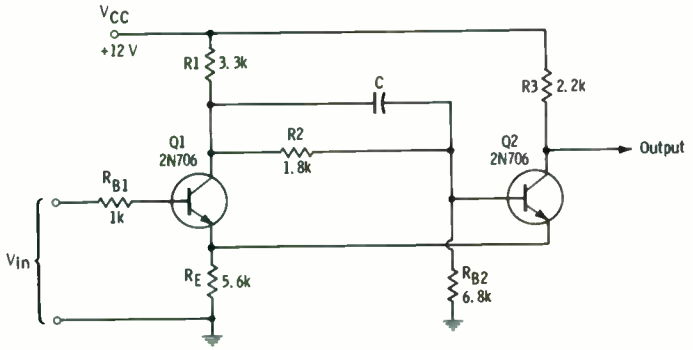
Fig. 12-1A shows an example of a Schmitt trigger. At this point in our studies, we should readily see that if V_{in} is zero, Q1 is off and Q2 is on. Resistors R1, R2, and R_{B2} form a voltage divider which results in a voltage of about +6.8 volts. This result can be estimated very quickly because the sum of R1, R2, and R_{B2} is very close to 12,000 ohms, so the total current is 1 mA. This 1 mA through the 6.8k resistor (R_{B2}) produces +6.8 volts at the Q2 base.

The 2N706 transistor is a silicon type, so its emitter will be about 0.6 volt less positive than its base, or at about 6.2 volts. This is V_E when Q2 is conducting and Q1 is off.

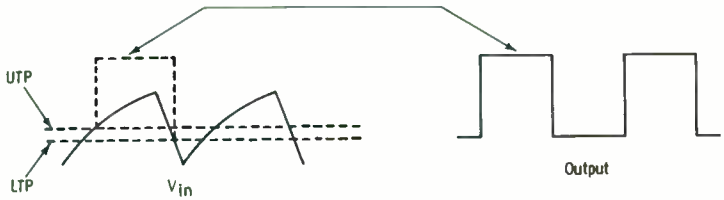
Since the emitter voltage is +6.2 volts, we know that if V_{in} is less than +6.8 volts the circuit will remain as it is. But when the input voltage rises to about +6.8 volts, Q1 begins to conduct, the collector voltage of Q1 (and hence the Q2 base voltage) is lowered, and V_E increases momentarily until Q2 comes out of saturation. The reduced base current of Q2 results in lowered Q2 emitter current; thus V_E is lowered, and the current through R_{E1} increases. The action is regenerative until Q1 is on and Q2 is off. The emitter voltage is now *less* than it was initially (this will be

explained in a moment); therefore the *trip point* is also lowered. The two trip points are termed upper trip point (UTP) and lower trip point (LTP) (Fig. 12-1B).

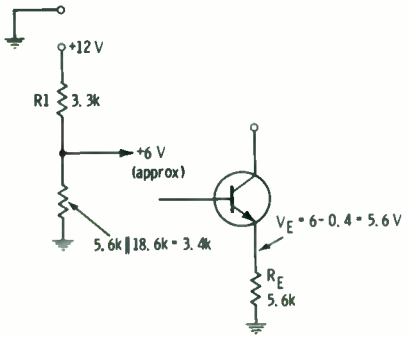
This difference in trip points results in a good *snap* action, producing sharp square-wave transitions from any sinusoidal or other nonrectangular waveform. When V_{in} falls to the LTP, operation reverses, and the circuit returns to its initial state.



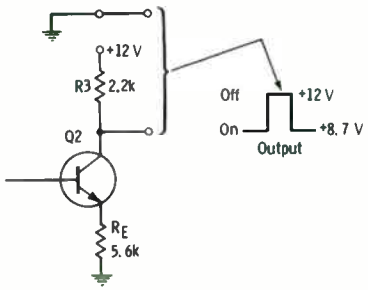
(A) Typical circuit.



(B) Typical waveforms.



(C) Equivalent bias circuit.



(D) Equivalent output circuit.

Fig. 12-1. Fundamentals of the Schmitt trigger.

We have seen how the UTP value is computed (+6.8 volts in this example). Now what is the LTP? For the circuit under discussion, Q1 must now be driven toward cutoff. Since Q2 is at cutoff, we know that V_E now depends on the Q1 current.

The analysis continues with Fig. 12-1C. The total current through R1 is now the Q1 current plus the current through voltage divider R2-R_{B2}. The 5.6k resistor is effectively in parallel with 8.6k ($R2 + R_{B2}$); the equivalent is about 3.4k. For a quick analysis, since R1 is 3.3k the voltage at the Q1 collector will be about half of V_{CC}, or +6 volts. There will be about a 0.4-volt drop from collector to emitter (slightly less than the base-emitter drop), so $V_E = 6 - 0.4 = 5.6$ volts (approx).

Since Q1 must be brought out of saturation, its base voltage must be made less than 5.6 volts plus the 0.6 volt required for conduction, or 6.2 volts. To recapitulate:

V_E with Q2 conducting = +6.2 volts (approx).

V_E with Q1 conducting = +5.6 volts (approx).

UTP = +6.8 volts (Q1 always conducts if input exceeds +6.8 volts.)

LTP = 6.2 volts (Q2 always conducts if input is less positive than +6.2 volts).

Then:

$$UTP = V_{E2} + V_{BE1}$$
$$LTP = V_{E1} + V_{BE1}$$

where,

V_{E2} = V_E with Q2 on,
V_{E1} = V_E with Q1 on, and
V_{BE1} = base-emitter voltage of Q1.

We can readily check a Schmitt trigger circuit by disconnecting the input and applying a known (and variable) dc voltage to the Q1 base.

What would we expect for the output at the Q2 collector? See Fig. 12-1D. Since the unbypassed R_E is larger than collector load R3 (large amount of degeneration), we will not get the full V_{CC} swing between the cutoff and saturated states. When Q2 is off, there is no current in R3, so we would expect to find the top of output waveform at about +12 volts. When Q2 is turned "fully on" by the regenerative action previously described, the Q2 collector current is:

$$\frac{V}{R} = \frac{12}{(2.2k + 5.6k)} = 1.5 \text{ mA (approx)}$$

This 1.5 mA through R3 results in a voltage drop of (0.0015)(2200) = 3.3 volts.
Then 12 − 3.3 = 8.7 volts at the output when Q2 is in the on state.

Therefore we would expect an excursion from about +8.7 volts to +12 volts, resulting in a peak-to-peak waveform of about 3.3 volts. In practice, due to circuit losses, we will normally find this peak-to-peak value slightly less than V_{CC} minus the on voltage drop across R3.

12-2. SPECIAL WAVEFORM GENERATORS

Fig. 12-2 shows a conventional sawtooth generator. Prior to t_1 (prior to an applied pulse), C is charging toward −20 volts through R. At t_1, the transistor is driven into saturation; the resulting very low impedance to ground (closed switch) discharges C. The incremental slope of the sawtooth depends on time constant RC; for a linear sawtooth, the time constant must be long compared to the trigger-pulse period. (The charge of a capacitor follows an exponential curve.) A positive-going sawtooth would be obtained if an npn transistor were used with a positive trigger input and a positive supply voltage.

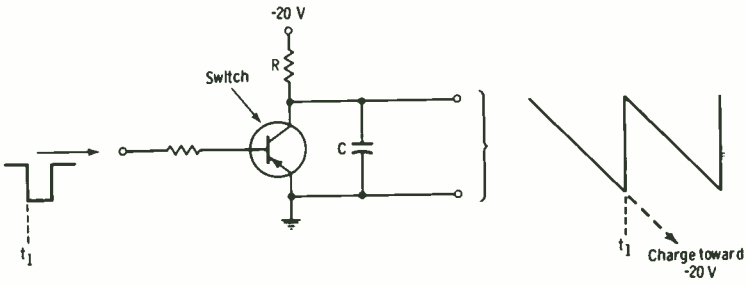


Fig. 12-2. Transistor sawtooth generator.

As we will see later, a trapezoidal (truncated sawtooth) waveform is sometimes required. Fig. 12-3 shows a circuit for generating such a waveform. Because of the positive voltage at the emitter of Q1, this transistor is normally saturated. Thus the switch is closed, the Q1 collector is at +70 volts, and C2 is charged to this potential. The capacitance of C2 is only 6800 pF, so this capacitor charges quickly. The positive-going edge of the applied signal cuts Q1 off. At this instant, the Q1 collector voltage attempts to go to ground potential, but C2 holds its charge until it is drained off through R1. The rate of discharge is fixed by the R1-C2 time constant. We have here a quick-charge, slow-discharge circuit.

Changes in the voltage of C2 are coupled through C3 to Q2 and Q3. With Q1 saturated (C2 charged to +70 volts), the common bases of Q2 and Q3 are essentially at ground potential through forward-biased diode X1. When C2 discharges toward ground (swings negative), this change in voltage is transferred to the common bases, reverse-biasing diode X1. When this base potential attempts to exceed −20 volts, the

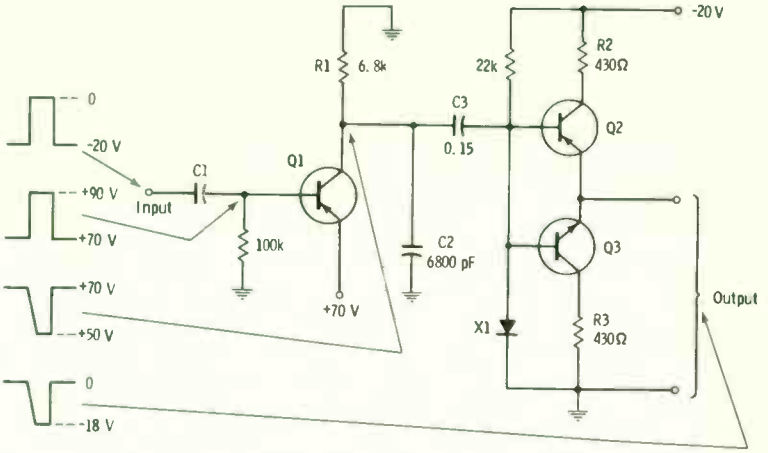


Fig. 12-3. Trapezoidal-waveform circuit.

collector-base junction of Q2 becomes forward biased and clamps at −20 volts, so for the remainder of the pulse, no voltage change occurs, as shown by the waveforms in Fig. 12-3. This is a "truncated sawtooth," or trapezoidal waveform.

When Q1 again saturates (end of input pulse), the bases of Q2 and Q3 attempt to go positive because of the voltage change coupled through C3. Diode X1 now conducts and clamps at ground potential. Thus the output trapezoid swings between ground (zero potential) and some negative value. For the circuit shown, what value of output waveform should we expect? When X1 is conducting, the emitters of Q2 and Q3 will be at essentially ground (zero) potential. Note the complementary-symmetry arrangement of Q2 and Q3. When Q1 is cut off, the Q2 base goes negative, causing Q2 to draw current. The resulting negative potential at the Q2 emitter (X1 is now an open switch) brings Q3 into conduction at the same time. Since we have a 20-volt signal swing at the common base, and the output circuit is an emitter follower, the output signal will be very close to this peak-to-peak value, except for about a 1-volt drop across each transistor. So we would expect an output signal swing from 0 to −18 volts (approximately).

When extreme accuracy in pulse width is required, and where jitter-free leading edges must be obtained (as in T-Pulse generators), we will often find a type of "ringing oscillator" used. See Fig. 12-4. The transistor is used as a switch to either suddenly supply or quickly interrupt current to a resonant circuit. In the example shown, Q1 is normally conducting because R_B is returned to $-V_{CC}$. With Q1 saturated, practically a short circuit exists across LC and the diode output circuit, and no voltage is present. When a positive gate pulse is applied to the base, Q1 is quickly

cut off; C begins to charge toward $-V_{CC}$, and resonant circuit LC is "shocked" into oscillation. Since the initial voltage swing is negative, a negative pulse occurs. When the inductive field collapses and the induced voltage tends to go positive (oscillation), this positive swing is damped out by X1 and R1. The rate of the energy exchange between L and C is determined by the resonant frequency (and circuit Q) of the combination; thus we can see that the *width* of the output pulse is determined by this resonant frequency.

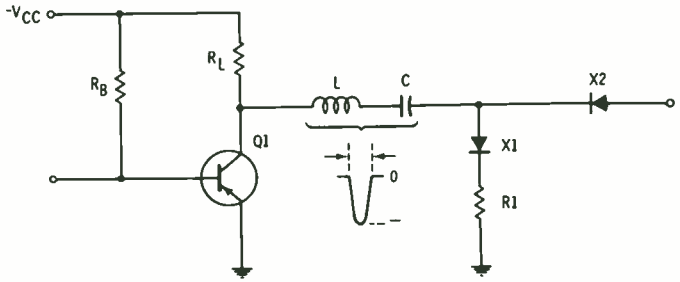


Fig. 12-4. "Ringing oscillotor" circuit.

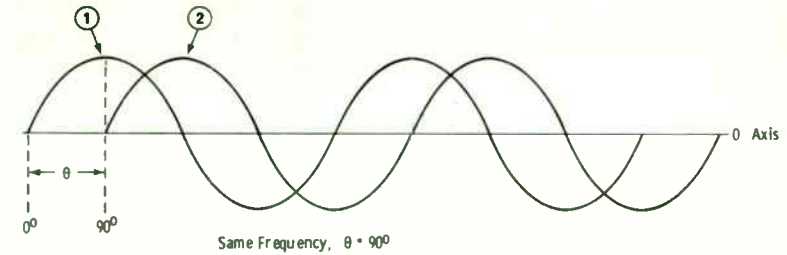
There are many variations of the circuit described above, but they all work on the same principle. Sometimes we find a parallel resonant circuit used in either the emitter or collector lead. Since the transistor acts purely as a switch, operation is not affected by changes in its characteristics. The circuit provides a stable pulse which is considerably more jitter-free than that obtainable from (for example) the usual monostable multivibrator.

Another type of circuit requiring a damping diode is the pulse-transformer configuration of Fig. 9-15. The in and out impedance of a pulse transformer is normally around 100 ohms, and pulse amplitude and width depend on the specifications of the particular pulse transformer used.

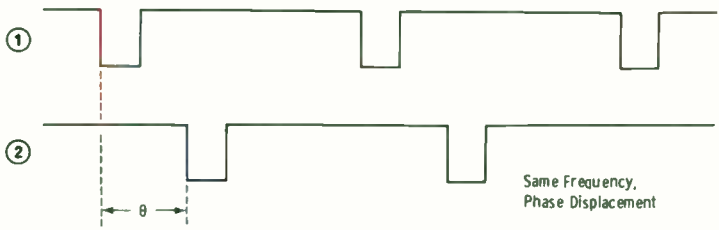
12-3. ERROR DETECTION, AFC, APC

Automatic frequency control (AFC) and automatic phase control (APC) are both forms of *error detection* with an associated *corrective function.* The "error" must be related to some known standard.

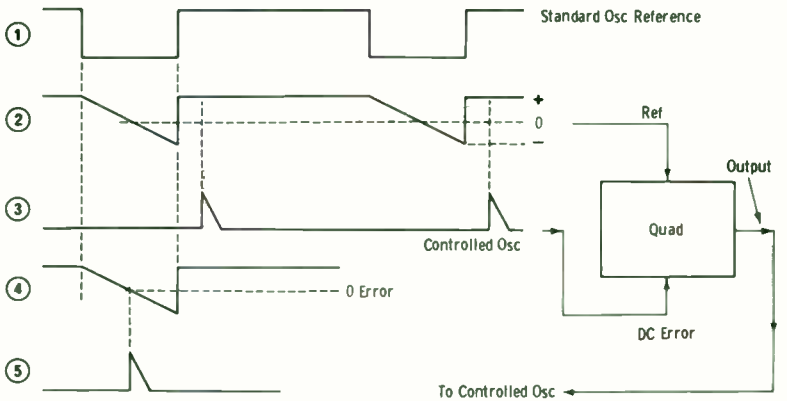
Fig. 12-5A shows two sine waves of identical frequency but with a 90° phase difference. If we take waveform 1 as the reference, waveform 2 *lags* waveform 1 by 90°. If we take waveform 2 as the reference, waveform 1 *leads* waveform 2 by 90°. Either sine wave could be the reference or "standard," and the other controlled in frequency and phase. The proper



(A) Phase relation of sine waves.



(B) Phase relation of pulses.



(C) Error detection and correction.

Fig. 12-5. Fundamentals of error detection.

phase relationship might be the 90° shown, zero, or some other phase difference.

Next, look at Fig. 12-5B. We have two pulses of identical frequency (same pulse period), but with a phase displacement. Now go on to Fig. 12-5C. In waveform 1 we have the "reference" or "standard" pulse period. This might be from the local sync generator, a color-subcarrier pulse (or countdown thereof), etc. We form a sawtooth from this stan-

dard pulse as in waveform 2. Waveform 3 is a pulse from an oscillator to be controlled. It may or may not have the correct frequency at this time; we know from the drawing that it definitely is not in phase with the reference.

We feed waveforms 2 and 3 into an error detector such as a diode "quad" (to be described shortly). The quad conducts for the duration of the pulse in waveform 3, and at the moment we can see the resultant dc output will be a positive voltage. (The quad is sampling at a time when waveform 2 is maximum positive). If this "error voltage" is fed back to the controlled oscillator, it should serve to change the oscillation *frequency* in the proper direction until the sampling occurs near the center of the reference sawtooth (essentially zero error voltage). This condition is shown by waveforms 4 and 5. Thus the controlled oscillator is locked in frequency *and* phase. The proper system phasing is obtained by the position of the reference pulse; this could be at the leading edge of sync, trailing edge of sync, a certain position within vertical sync, etc. This entire process is termed "sampling pulse technique."

In Fig. 12-6 we see how to measure "loop gain," and the difference between a sawtooth and trapezoid derived from the same reference pulse period. In the example given, we have two nonvariables; the pulse duration is 10 microseconds, and the amplitude is 10 volts. The trapezoid slope (hence loop gain) is twice as great as for the sawtooth. If the level change is completed in 5 μs, the slope is 0.5 μs/volt; that is, it takes just one-half microsecond to change one volt, or five microseconds to change 10 volts. The slope of the sawtooth is more gradual (lower loop gain). This waveform requires 10 microseconds to change 10 volts; thus the sensitivity is 1 μs/volt. We will find some systems use first the lower loop gain (sawtooth) to establish frequency control, then the trapezoid to exert a tighter phase control after the frequency has been stabilized. In any case, the sampling pulse (derived from the controlled oscillator) will tend to hold the oscillator frequency (and phase) at the point where sampling occurs at zero error voltage (center of slope).

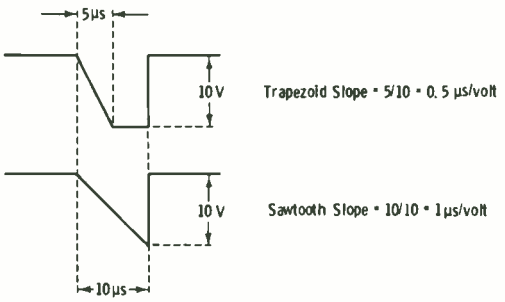


Fig. 12-6. Sawtooth and trapezoid of same duration.

The function of the sampling diode quad is shown by Fig. 12-7. At the instant of the sampling pulses (waveform B), the diode bridge is driven into conduction, connecting the trapezoid waveform (A) to "memory capacitor" C_M. This capacitor will charge (or discharge) to the dc potential existing at the time of the "sample." Capacitor C1 charges during pulse time, and the time constant of R1 and C1 holds the quad nonconducting during the interval between sampling pulses. Capacitor C_M has no discharge path except through the relatively high impedance of Q1 and the diode bridge. Therefore it "remembers" the condition existing at the time of the previous pulse, and its charge will change only if the next pulse samples at a different dc level than existed for the preceding pulse. By dc coupling through Q1 back to the controlled oscillator (from which the sampling pulses are derived), the frequency-phase relationship is maintained.

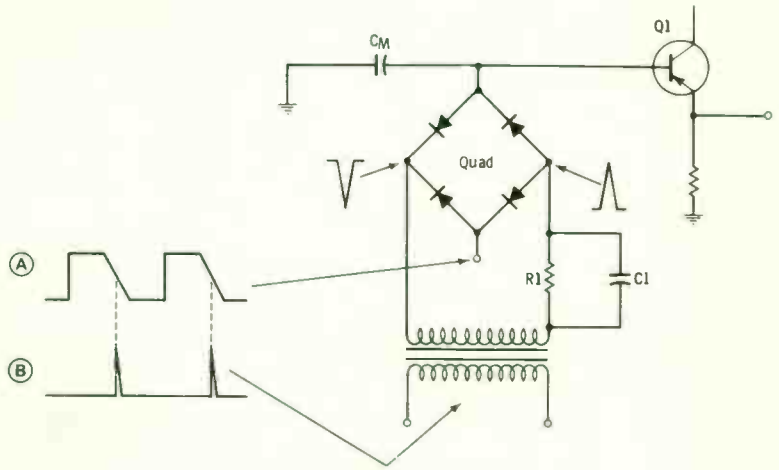


Fig. 12-7. Circuit of phase detector.

12-4. SIGNAL PROCESSING

Signal processing is employed for such operations as separation of luminance and chrominance signals for separate processing, phase correction (as in camera preamps), and gamma correction.

The separation of luminance and chroma information as used in stabilizing amplifiers and other composite color equipment is illustrated by Figs. 12-8 and 12-9. In the processing of Fig. 12-8, L1-C1-C2 is a parallel circuit tuned to 3.58 MHz. Thus the output across R_{E1} is low-frequency video and sync only, which is fed to the luminance signal-processing channel. The Q1 emitter is coupled to the Q2 base through a

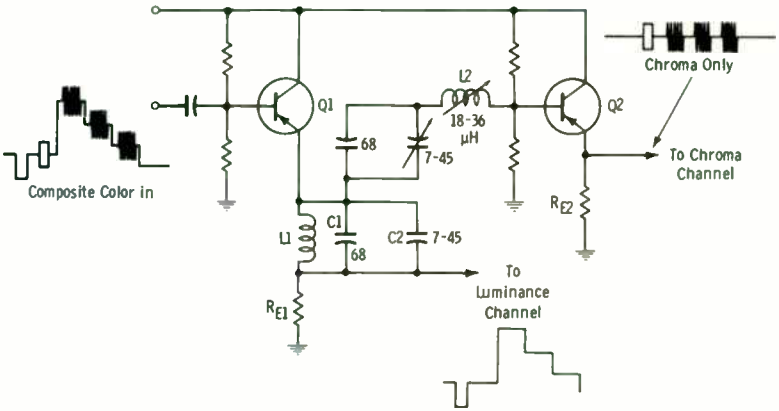


Fig. 12-8. Circuit for separating chrominance and luminance.

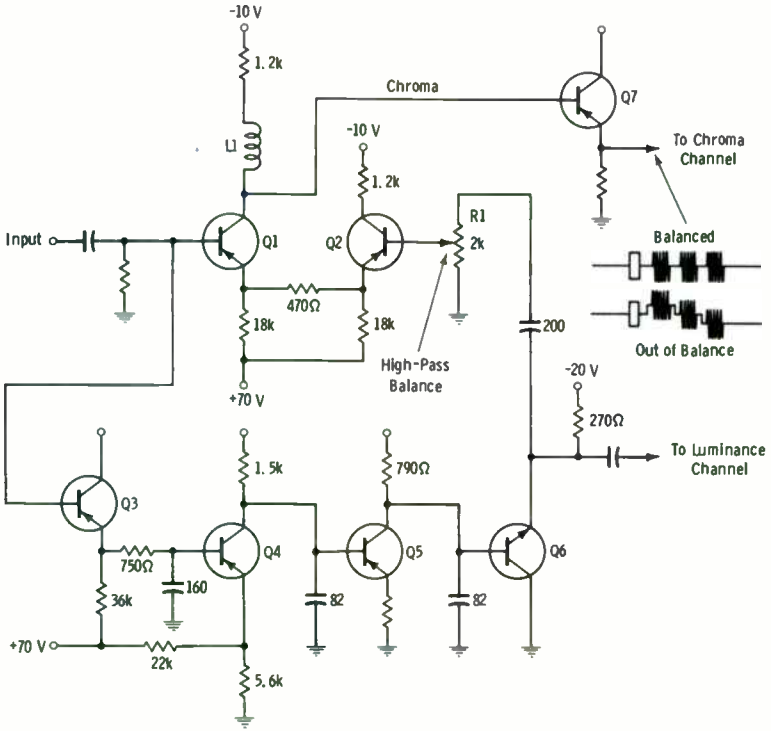
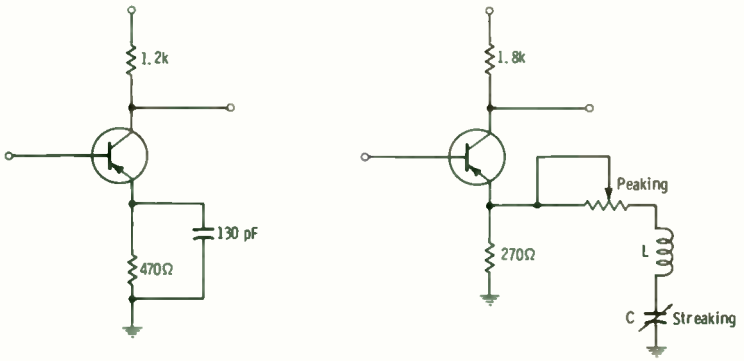


Fig. 12-9. Feedback used for chrominance-luminance separation.

circuit series-resonant to 3.58 MHz. Thus the output across R_{E2} consists only of chrominance information.

The circuit of Fig. 12-9 is a more sophisticated approach which we will encounter in varying degrees in modern composite color signal units. Transistors Q1 and Q2 are connected in a differential amplifier circuit (Chapter 5). Transistor Q3 isolates (at high impedance) the low-pass circuitry of Q4, Q5, and current-gain driver Q6. The filtering is accomplished by the shunt capacitors from the bases to ground. Note that the signal phase shift through the low-pass stages is 360 degrees, so the signal at the Q2 base is back in phase with the composite signal at the Q1 base. Thus at low (luminance) frequencies, an amplitude change at the Q1 base is followed by a proportional amplitude change caused by Q2 at the Q1 emitter. Therefore, the Q1 collector signal is the *difference* signal; the luminance information has been cancelled, and only the chroma is passed. Potentiometer R1 is a high-pass balance control which is adjusted to provide the same amplitude of luminance signal at the Q2 base that appears at the Q1 base. If these amplitudes differ, the chroma-signal axis is shifted up or down in step with the luminance amplitude difference. Peaking coil L1 compensates for high-frequency losses.

In camera preamplifiers, a certain amount of processing is necessary because of the round shape and finite size of the pickup-tube scanning spot (aperture). High-frequency boosting to compensate for this effect is termed "aperture correction." In Fig. 12-10A, the emitter resistor forms



(*A*) *Method of emitter peaking.* (*B*) *Peaking and phase correction.*

Fig. 12-10. Methods of aperture correction.

an inverse feedback path that is incompletely bypassed by the small value of capacitance. Signals at higher frequencies are bypassed while signals at lower frequencies must pass through the inverse feedback path.

Since the "aperture effect" is equivalent to loss of high frequencies without phase error, and since "aperture correction" *does introduce phase*

error, some means must be provided to recorrect the signal phase. The phase angle should increase linearly with frequency, maintaining the same time delay for all frequencies in the passband. Departure from this characteristic results in phase distortion most noticeable as trailing white edges following black edges (negative-polarity streaking) or "white after white" (positive-polarity streaking).

One type of phase distortion can be compensated by an equal and opposite phase correction. Therefore, we will find the capacitor of Fig. 12-10A made variable in some circuits and termed a "streaking control." Since a lagging phase shift is corrected by an equal leading phase shift, and vice-versa, we will sometimes encounter the circuit of Fig. 12-10B. The LC circuit is resonant near the top of the intended passband. The variable resistance (peaking control) determines the magnitude of the resonant peak introduced. The variable capacitor (streaking control) adjusts the resonant frequency to that necessary to introduce the required lead or lag in phase.

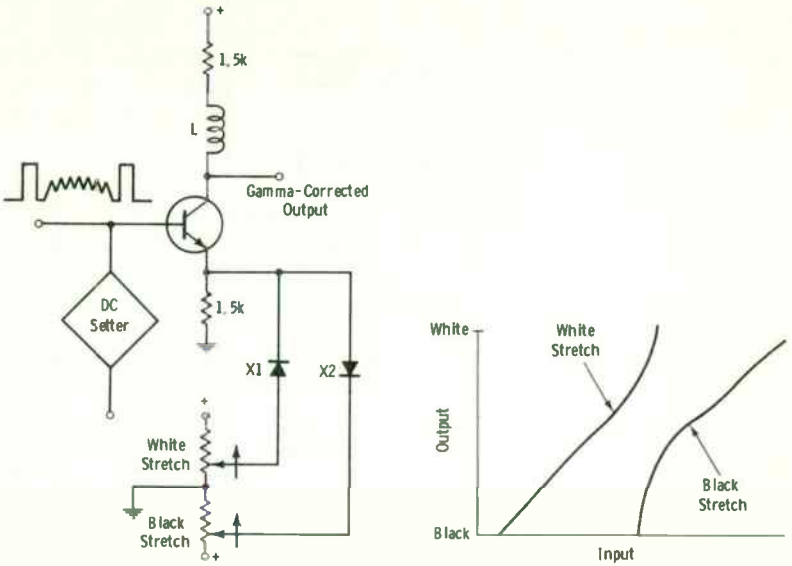
In either image-orthicon or vidicon camera chains, we will find nonlinear amplifiers used as "gamma-correction" circuits. The image orthicon in particular exhibits white compression when operated several stops beyond the "knee" of the transfer characteristic curve. A "white stretch" control may be employed to correct this operation. In addition, the kinescope exhibits a nonlinear voltage-to-brightness curve which essentially compresses blacks, particularly for "low-key" scenes. Also, the average film requires a certain amount of "black stretch" to "fit" the television-system transfer curve, whether monochrome or color.

Fig. 12-11A shows the basic idea of gamma-control circuitry. As in any stage where blanking or sync is inserted, or where a nonlinear function is introduced, black level must be ascertained and held to a reference point. So the input of such a stage will be clamped, or dc set, or clipped at a given dc level, so that the nonlinear operation is referred to a desired level as a starting point. The coil in the collector circuit is a shunt peaking coil to compensate for high-frequency losses in the emitter circuit.

When the white stretch control is rotated clockwise (direction of arrow), a point is reached at which X1 becomes forward biased. Since white is of negative polarity at the emitter, this voltage fixes the point of "bend" in the white region. When X1 conducts, the emitter resistance is partially bypassed, reducing degeneration and increasing gain. See the white-stretch curve in Fig. 12-11B.

Similarly, as the black stretch control is rotated clockwise, back bias on X2 is reduced, and it conducts. Note that black is of positive polarity at the emitter, so the gain increases in the black region, stretching blacks. The corresponding curve for black stretch is shown also in Fig. 12-11B.

We will find a considerable variation in design of gamma circuitry, but all work on these principles.



(*A*) *Circuit diagram.* (*B*) *Output vs input.*

Fig. 12-11. Gamma-correction amplifier.

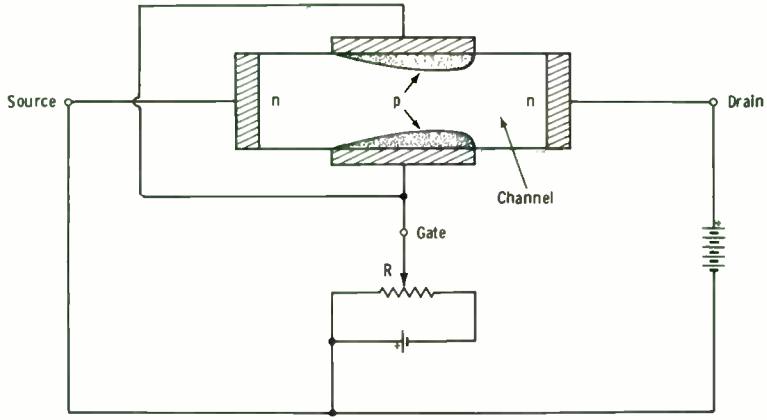
12-5. THE FIELD EFFECT TRANSISTOR (FET)

The field effect transistor (FET) is relatively new in equipment in the field, but it will gain substantially in practical applications in a short time. As with any practical device, it has advantages and disadvantages when compared to the conventional transistor studied thus far.

For the conventional transistor, we know there are two major differences in operation compared to the vacuum tube; the input circuit must be forward biased (the tube is actually reverse biased), and the output circuit must be reverse biased. So essentially we have a current-operated device (transistor) compared to a voltage-operated device (tube). This is simply the most convenient way to contrast the two devices.

Now see Fig. 12-12A. In this "junction type" of FET, a pn junction is employed for the gate (control) electrode. The sole function of this gate is to provide a control element analogous to the grid of a vacuum tube. The FET also has a source (analogous to the cathode) and a drain (analogous to the plate). Note that the gate receives a voltage which is the reverse bias necessary to control majority-carrier current in the "channel."

When the gate voltage is increased, the fields set up by the junction barriers cause a reduction in the number of majority carriers flowing through the channel from source to drain (see Fig. 12-13). As the gate voltage is reduced, drain current increases. The area in which the drain



(A) Simplified diagram.

(B) Schematic symbols.

Fig. 12-12. Fundamentals of junction FET.

voltage has a relatively small effect on drain current (between points A and B in Fig. 12-13) is termed the "pinch-off region" of operation. As the drain-to-source voltage is increased, or the gate voltage goes to zero bias or a slight forward bias, the drain current can increase excessively, and the FET can be damaged by the resultant heating of the junction (part C of the curve in Fig. 12-13).

Just as with the vacuum tube, the input impedance of the FET in the common-source configuration is very high due to the reverse bias on the gate. The FET is advantageous to use where very high input impedances are required in a single stage of amplification. The device is extremely delicate in handling and servicing, but this disadvantage is rapidly being overcome.

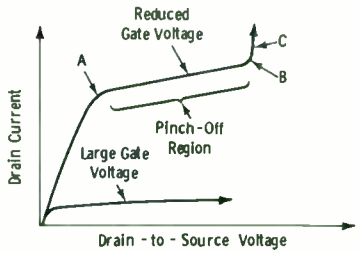
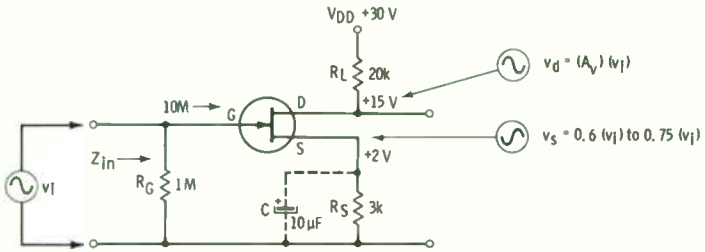


Fig. 12-13. Typical FET drain-current characteristic.

Figs. 12-14A and 12-14B present a circuit drawn for an n-channel and a p-channel FET. The gate input impedance is normally around 10 megohms, and a fixed resistor (R_G) is used so that the input signal voltage (v_i) is developed across a known load for all frequencies concerned.

Typically, the signal at the source (v_s) will be between 0.6 and 0.75 of v_i when R_S is not bypassed. Resistor R_S supplies the proper bias to the gate and (for class-A operation) fixes the drain voltage at about ½ of V_{DD}. The drain signal output (v_d) is inverted.



(A) N-channel.

(B) P-channel.

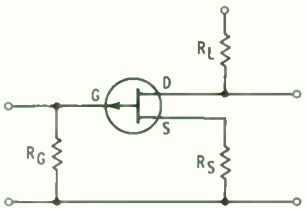


Fig. 12-14. Amplifier circuits using FETs.

Just as $\beta = 50$ is a good "average" for the conventional transistor, so the transconductance (g_m) for the proper operating point of the average FET can be assumed to be $g_m = 500$ micromhos, and $A_v = g_m R_L$ (approx) without feedback.

NOTE: In an FET, g_m varies with drain current just as the beta of a conventional transistor varies with collector current. Therefore it is subject to wide variation, and data sheets must be consulted to determine g_m at a specified drain current.

The voltage amplification with source feedback (C not connected) is:

$$A_v = \frac{g_m R_L}{1 + g_m R_s} \text{ (approx)}$$

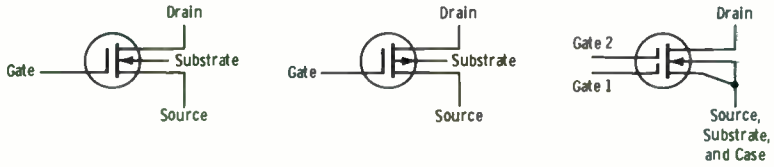
For the circuit of Fig. 12-14A, assume that $g_m = 500$. Then the gain without feedback is:

$$A_v = (0.0005)(20{,}000) = 10 \text{ (approx)}$$

With C not used (source feedback):

$$A_v = \frac{0.0005\ (20{,}000)}{1 + 0.0005\ (3000)} = 4 \text{ (approx)}$$

Fig. 12-15 shows symbols for three types of metal-oxide-semiconductor FET (MOSFET). These transistors are treated further in applicable portions of following chapters.



(A) N-channel MOSFET symbol. *(B) P-channel MOSFET symbol.* *(C) Dual-insulated-gate MOSFET.*

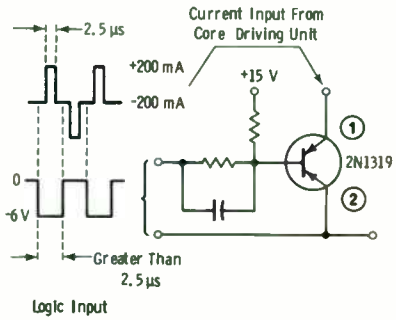
Fig. 12-15. Schematic symbols for MOSFETs.

FET characteristics may be summarized as follows:

1. High impedances permit use of vacuum-tube biasing techniques.
2. Very good thermal stability.

(A) Npn schematic symbol.

(B) Pnp schematic symbol.



(C) Typical switch application.

Fig. 12-16. Bidirectional transistor.

3. Extremely low feedback capacitance.
4. Low noise figure (NF = 3.5 dB, typical).

12-6. THE BIDIRECTIONAL TRANSISTOR

In the "bidirectional" transistor (Fig. 12-16), the emitter and collector can be used interchangeably, permitting either to be used as the input or output electrode without loss of efficiency. The switching of current from one direction to the other is achieved without appreciable difference in current gain.

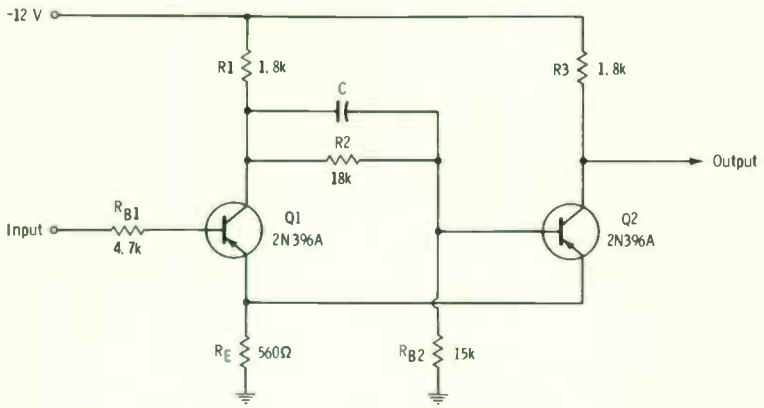


Fig. 12-17. Circuit for Q12-1.

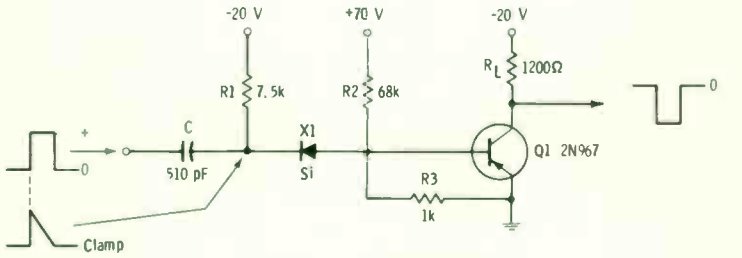


Fig. 12-18. Circuit for Q12-2.

Fig. 12-16A shows the symbol for an npn bidirectional transistor, such as the 2N1169 or 2N1170; Fig. 12-16B represents a pnp type, such as the 2N1319. The circuit of Fig. 12-16C is a typical application in which the duration and phase of the current input relative to the logic-voltage input determines whether electrode 1 becomes the "emitter" or the "collector."

EXERCISES

Q12-1. Analyze the circuit of Fig. 12-17. What are the UTP, the LTP, the voltage levels of the output pulse, and the peak-to-peak value of the output pulse?

Q12-2. Analyze the circuit in Fig. 12-18. This exercise will test your general circuit-analysis capability.

Q12-3. In Fig. 12-4, if L and C are resonant at 4 MHz, what approximate pulse width would you expect at the output?

Q12-4. How many "memory circuits" have you studied thus far in this book?

CHAPTER 13

Oscillators and Radio-Frequency Amplifiers

For radio-frequency operation of transistors, we will start with the oscillator. We have studied the multivibrator type in Chapter 10. This chapter will be concerned with sine-wave oscillators. (Much of the material in the first nine sections of this chapter has been taken, with minor changes, from Department of the Army Technical Manual TM11-690, *Basic Theory and Application of Transistors.*)

13-1. OSCILLATING FREQUENCY AND DC POWER

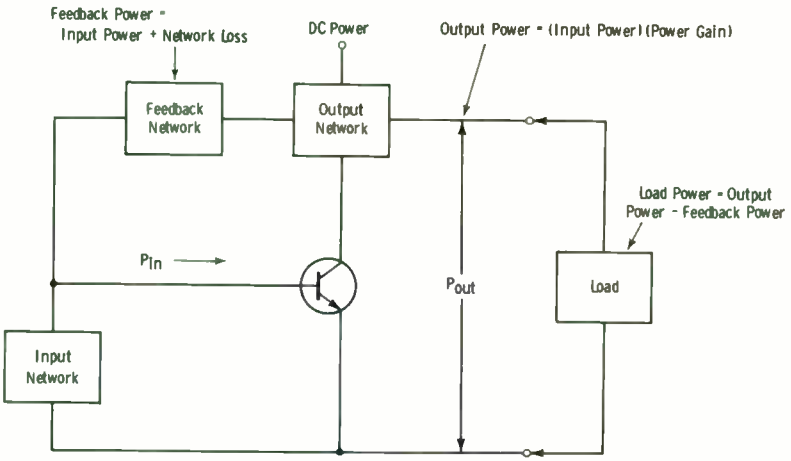
To generate ac power with a transistor amplifier (Fig. 13-1), a portion of the output power must be returned to the input in phase with the starting power (regenerative, or positive, feedback). The power delivered to the load will be the output power less the feedback power.

Besides the requirement for regenerative feedback, frequency-determining elements and the necessary dc bias voltages must be included in the transistor oscillator circuit. The frequency-determining circuit elements may consist of an inductance-capacitance (LC) network, a crystal, or a resistance-capacitance (RC) network.

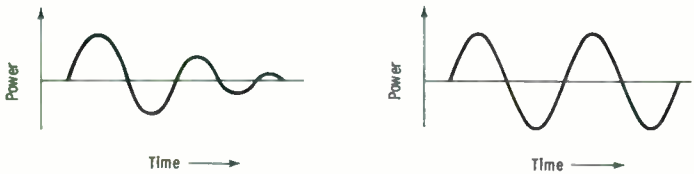
Bias-voltage requirements for the transistor oscillator are similar to those for the transistor amplifier. Stabilization of the operating point also is an important factor for consideration in the transistor oscillator circuit, since stability of the operating point affects the output amplitude, waveform, and frequency stability.

13-2. IMPEDANCE DIFFERENCES BETWEEN TUBES AND TRANSISTORS

The input and output impedances of an electron-tube circuit are high; the feedback signal suffers little loss from mismatch in the feedback



(A) Functional diagram.



(B) Insufficient feedback. *(C) Sufficient feedback.*

Fig. 13-1. Basic oscillator principles.

network. In the transistor common-base configuration, the input impedance is low; the output impedance is high. Coupling the feedback signal from the output to the input requires a feedback network to match unequal impedances; sometimes the loss due to mismatch may be compensated for by providing more feedback energy. Other transistor configurations involve similar problems.

13-3. SELECTION OF CIRCUIT CONFIGURATION

The choice of transistor circuit configuration for an oscillator is determined by oscillator requirements and the advantages (if any) of a particular transistor amplifier configuration.

The common-base configuration has the lowest input impedance and the highest output impedance. Compensation for the loss in the feedback circuit must be made unless matching is achieved. Current gain is less than one, and voltage and power gains are greater than one. There is no phase reversal between input and output.

The common-emitter configuration has "moderate" input and output impedances, reducing the requirement for matching with a feedback circuit. This configuration resembles the grounded-cathode electron-tube circuit in that a phase reversal occurs between the input and output circuits. Current, voltage, and power gains are all greater than one. The highest power gains are obtained with this configuration, making it generally desirable for use in transistor oscillator circuits.

The common-collector configuration has a high input impedance and a moderate to low output impedance. The requirement for matching the input and output impedances with the feedback circuit also exists with this configuration. Voltage gain is less than one, and the current and power gains are greater than one. There is no phase reversal between input and output.

13-4. FREQUENCY LIMITATIONS

The data sheet of a transistor includes the cutoff frequency of the transistor in its high-frequency characteristics. This frequency is given with relation to the current gain of the transistor when used in either the common-base (alpha) or the common-emitter (beta) configuration. The cutoff frequency is defined as the point at which the current gain drops 3 dB, or to 0.707 times its low-frequency (normally 1000 Hz) value.

Oscillators can operate above the cutoff frequency and could operate up to but not including the f_{max} of the transistor. The maximum frequency of the transistor is defined as the frequency at which the power gain of the transistor amplifier becomes unity. That is, an input signal of a specific level would appear in the output of the transistor amplifier at the same level (no loss or gain). Since power gain is required to overcome losses in the feedback circuit, note that operation of the transistor oscillator at f_{max} is not possible. An operating frequency somewhat below f_{max} is therefore chosen so that sufficient power gain for feedback and output can be obtained.

13-5. INITIAL AND SUSTAINED OSCILLATION

Oscillation is initially caused in a transistor circuit by a process similar to that in a vacuum-tube oscillator circuit. The circuit may be externally excited (triggered) or self-excited. In the self-excited circuit, at the moment dc power is applied, the energy level does not instantly reach maximum but, instead, gradually approaches it. Oscillations build up to a point limited by the normal operation of the amplifier, the feedback energy, and the nonlinear condition of the circuit.

In Fig. 13-1A, the output power is equal to the power gain of the amplifier multiplied by the input power. When the amplifier power gain is less than one, a damped oscillation is obtained (Fig. 13-1B); that is,

the oscillations become smaller with time until they reach zero amplitude. For example, if the power gain of the transistor amplifier is 0.9 and the starting signal is 1 mW, the output power after the first cycle is 0.9 mW. If all of this power is fed back to the input and amplified, the output power on the second cycle becomes 0.81 mW. The action continues in this way until oscillation ceases. This process is similar to the oscillation in a charged parallel-tuned circuit, where the resistance present damps the oscillation. Thus, to sustain oscillation the power gain of an amplifier must be equal to or greater than one (Fig. 13-1C).

In a practical transistor oscillator circuit, the output power is divided. A portion is supplied to the load, and the remainder goes to the feedback network. Power losses occur in the feedback network; the required feedback power is equal to the input power needed plus these losses. For example, if the power gain of a transistor amplifier is 20 dB and the input power level is 1 dBm, the output power is 21 dBm. If the loss in the feedback network is 10 dB, the feedback power must be 11 dBm to sustain oscillation. In other words, the feedback power minus the loss in the feedback network is equal to the input power, 1 mW. Thus all values remain constant, and oscillation is sustained as in Fig. 13-1C.

13-6. FREQUENCY STABILITY

Let us consider at this point frequency instability caused by transistor characteristics rather than by external circuit elements. The dc operating point is usually chosen so that the operation of the transistor circuit is over the linear portion of the transistor characteristic (class-A operation). When the operation of the circuit falls into a nonlinear portion of the transistor characteristic because of variations in bias voltages, the transistor parameters vary. Since these parameters are basic to the transistor, and therefore affect the frequency of oscillation, frequency variation will occur with changes in bias voltages. A constant supply voltage is thus a prime requirement for frequency stability.

The collector-to-emitter capacitance of the transistor has more effect than the other parameters on frequency stability. This reactive element (sometimes referred to as the barrier capacitance) varies with changes in collector or emitter voltage and with temperature. In high-frequency oscillators, in which the collector-to-emitter capacitance becomes an important factor, the effect of changes in the capacitance may be minimized by inserting a relatively large swamping capacitor across the collector and emitter terminals. The total of the interelement and swamping capacitances in parallel results in a circuit which is less sensitive to variations in voltage. The added capacitor may be part of a tuned circuit.

The use of a common bias source for both the collector and the emitter maintains a relatively constant ratio of the two voltages. In effect, a change in one voltage is somewhat counteracted by the change in the

other, since an increased collector voltage causes an increase in the oscillating frequency and an increased emitter voltage causes a decrease in the oscillating frequency. However, complete compensation is not obtained since the effects on the circuit parameters of each bias voltage differ.

Changes in operating point with changes in temperature are encountered in the transistor oscillator. Since the transistor oscillator is an amplifier with additional circuitry, the means of temperature stablization are the same for both oscillators and amplifiers.

13-7. THE PHASE-SHIFT OSCILLATOR

A sine-wave output may be obtained from an oscillator in which an RC network is used instead of an LC network (Fig. 13-2). The RC network determines the frequency of oscillation and provides regenerative feedback between output and input. Since, in the common-emitter configuration, the signal between base and collector is reversed in phase, an additional 180° phase shift must be given the signal returned from output to input for positive feedback. This shift is accomplished by an RC network consisting of three sections, each contributing a 60° phase shift at the frequency of oscillation.

The current in a circuit consisting of resistance and capacitance in series is determined by the applied voltage divided by the combined impedance of the components (Ohm's law). Since the impedance of an RC circuit is capacitive, the current leads the applied voltage by a phase angle determined by the numerical relationship of resistance and capacitance. The voltage drop across the resistor, determined by the current through the resistor, therefore *leads* the applied voltage by the same phase angle.

If the capacitance is fixed, a variation in the resistance value will cause a variation in the phase angle. When the resistance becomes equal to zero, a maximum phase angle of 90° will exist between the applied voltage and current. This condition, however, is of no value since no voltage is developed across a zero resistance, and the applied voltage appears entirely across the capacitor. With a minimum of resistance in the section, the phase angle will be slightly less than 90°. Thus, at least three RC sections are required to provide the required 180° phase shift necessary for positive feedback. The value of resistance is generally chosen so that each section will provide a 60° phase shift.

In Fig. 13-2, resistors R_B, R3, and R_C provide base and collector bias for the oscillator. Capacitor C_E bypasses ac around emitter swamping resistor R_E. Capacitors C1, C2, and C3 and resistors R1, R2, and R_B constitute the feedback and phase-shifting network.

Oscillations are started by any random noise or transistor noise when power is applied. A change in the base current results in a larger change in collector current, 180° out of phase with the base-current change. The

signal returned to the base is inverted by the phase shifter, making the signal fed back regenerative.

The output waveform is very nearly sinusoidal; the output frequency is fixed. That is, with fixed resistance and capacitance in the phase-shifting network, the 180° phase shift occurs at only one frequency. At other frequencies, the capacitive reactance increases or decreases, causing a variation in phase relationship, and the feedback is not in phase, preventing sustained oscillations. The phase-shift oscillator is normally made variable over particular ranges by providing ganged variable capacitors or resistors in the phase shifter.

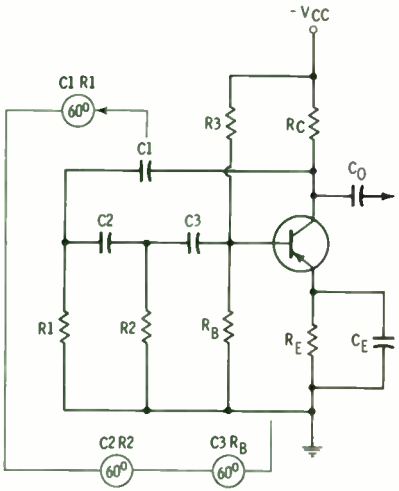


Fig. 13-2. Phase-shift oscillator.

A high-gain transistor must be used with the three-section phase-shifting network because the losses in the network are high. Increasing the number of phase-shifting sections causes a *reduction in the loss* of the overall network. This is so because additional sections reduce the phase shift necessary for each section, and the *loss* for each section is *lowered* as the *phase shift is reduced.* It is therefore not uncommon to encounter a phase-shift oscillator which employs more than three sections in the phase-shifting network.

With this review of oscillator fundamentals, we realize that in the event of a malfunctioning circuit, the transistor is most likely at fault. An increase in leakage current, a lowered h_{fe}, or any parameter that might affect f_{max} can prevent sustained oscillation.

13-8. THE HARTLEY OSCILLATOR

Fig. 13-3 shows a typical Hartley oscillator circuit and the representative dc-voltage distribution of a properly operating circuit.

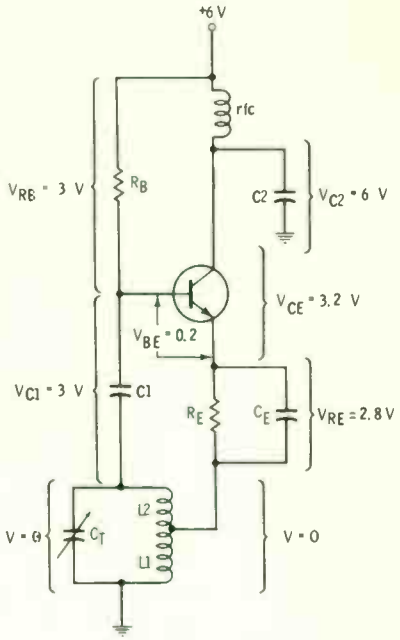


Fig. 13-3. Voltages in typical Hartley oscillator.

The radio-frequency choke (rfc) and capacitor C2 are to decouple the power supply. For convenience, we have assumed that L1, L2, and rfc are so low in resistance that zero voltage drop occurs at dc; in practice, a very small dc drop does occur.

Capacitor C2 should charge to the full supply voltage. Note that V_{CE} and V_{RE} should have a sum equal to the supply voltage. Also, the sum of V_{RB} and V_{C1} should equal the supply voltage. Carefully note that we should be able to judge the proper value of V_{C1}. Since C1 is across stabilizing network R_EC_E and the base-emitter junction, V_{C1} must equal the sum of V_{BE} and V_{RE} (3 volts in this example). Voltage drop V_{BE} is of the proper polarity to cause conduction (class-A operation).

Bear in mind that in a transistor circuit, bias depends on the amount of *current* through the base-emitter junction. This value is determined by the supply voltage and the resistance in the bias-current path. Base-circuit electron flow is from ground (negative terminal of the 6-volt supply) through L1, R_E, the emitter-base junction, and R_B back to the positive terminal of the supply.

Knowing the value of the voltage drops across R_B and R_E gives the bias voltage. Base-emitter voltage V_{BE} equals the supply voltage (V_{CC}) minus the sum of the other voltage drops:

$$V_{BE} = V_{CC} - (V_{RE} + V_{RB})$$

NOTE: Review Fig. 2-16 and related text for a transistorized Colpitts oscillator circuit and the use of variable-capacitance diodes for frequency modulation.

13-9. PRACTICAL USE OF JUNCTION CAPACITANCE IN FM OSCILLATORS

We have studied how junction capacitances are dependent on junction voltages and currents. Fig. 13-4 shows how this effect is put to use in a transistorized frequency modulator. Transistor Q1 provides the oscillator signal. Capacitor C1 and winding 1-3 of transformer T1 form the

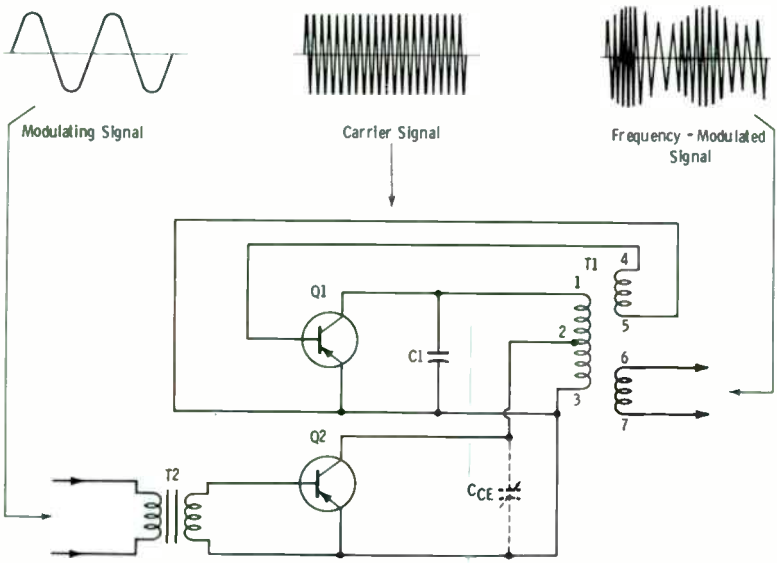


Fig. 13-4. Frequency-modulated oscillator.

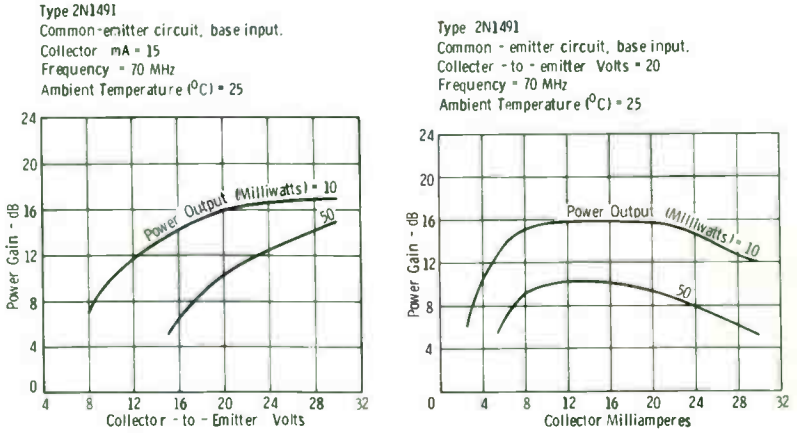
oscillator tank circuit; winding 4-5 of transformer T1 provides the required feedback; and winding 6-7 couples the oscillator signal to the following stage. The modulating signal, coupled through T2, varies the emitter-base current and collector voltage of reactance modulator Q2. As the collector voltage increases, output capacitance C_{CE} decreases, and as the collector voltage decreases, C_{CE} increases. When output capacitance C_{CE} decreases, the resonant frequency of the oscillator tank circuit increases. When output capacitance C_{CE} increases, the resonant frequency of the oscillator tank circuit decreases. The resonant frequency of the oscillator tank circuit is therefore increasing and decreasing at the modulating rate. Thus, the frequency of the signal generated by the oscillator

is increasing and decreasing at the modulating rate, and the output of the oscillator is a frequency-modulated signal. The slight amount of amplitude modulation is easily removed by frequency multipliers and limiters.

When afc is employed, the dc error signal may be applied to the base, emitter, or collector of the reactance transistor. Just bear in mind here that the polarity of the error voltage required for a given correction will depend upon whether the reactance transistor is pnp or npn. Always remember that the amplitude of the error dc is dependent on how far the controlled oscillator is off frequency, and the *polarity* of the error dc is dependent on whether the controlled oscillator is higher or lower in frequency than the reference signal.

13-10. RADIO-FREQUENCY AMPLIFIERS

Radio-frequency amplifiers generally use high-frequency silicon transistors in either the common-emitter or common-base configuration. Remember from previous studies that, for a given transistor, the common-base configuration is capable of operation at much higher frequencies than is the common-emitter connection.



(*A*) *As function of collector voltage.* (*B*) *As function of collector current.*

Courtesy RCA Corp.

Fig. 13-5. Power gain of type 2N1491 transistor.

Figs. 13-5A and 13-5B show the power gain of a typical 2N1491 transistor as a function of collector voltage and current. The operating frequency is specified as 70 MHz with power outputs of 10 and 50 mW. These curves show that the 2N1491 will operate satisfactorily at low power levels (outputs up to 10 milliwatts) with a minimum collector voltage of from 10 to 15 volts and a minimum collector current of from

3 to 5 milliamperes. As the power output is increased to 50 milliwatts, however, both the collector voltage and the collector current must be increased to provide reasonable gain. For example, a minimum collector voltage of about 19.5 volts would be required to provide a minimum power gain of 10 dB at an output level of 50 milliwatts. Because maximum power gain is obtained at a collector current of approximately 12 milliamperes, a suitable operating point would be a collector voltage of 20 volts and a collector current of 12 milliamperes.

Either the 2N1492 or the 2N1493 may be used to provide greater power output than can be obtained from the 2N1491. All of these types provide higher power gain as the collector voltage is increased. However, care must be exercised in the selection of collector voltage and current in order that the maximum ratings for the type used will not be exceeded and the dissipation in the transistor will be kept within ratings.

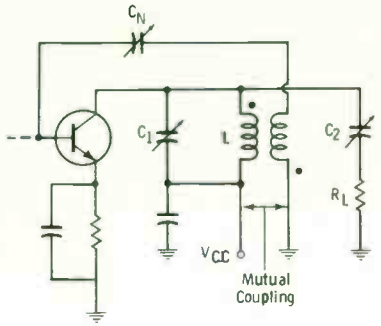
Fig. 13-6 shows typical biasing and neutralization circuits commonly used with L and pi output matching circuits. Circuits for the pi matching network (Figs. 13-6C and 13-6D) are slightly more complex than those for the L network (Figs. 13-6A and 13-6B). However, when harmonic radiation must be carefully suppressed, the pi network is used.

13-11. FETs IN OSCILLATOR CIRCUITS

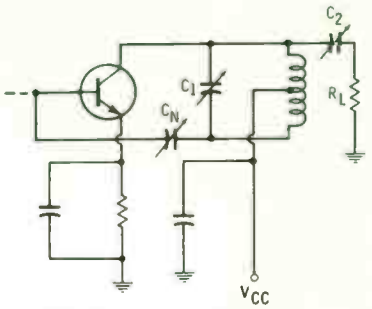
Figs. 13-7 through 13-14 are from *Insulated-Gate Field-Effect Transistors in Oscillator Circuits*, by G. D. Hanchette, and are used here courtesy of RCA Corp. Insulated-gate field-effect transistors can be made to oscillate in almost any of the well-known vacuum-tube oscillator circuits. Some slight modification of the vacuum-tube form of the circuit may be required, but the distinct advantages offered by the field-effect transistor compensate for this requirement. The two major advantages to the use of field-effect transistors are:

1. Faster and better thermal stability: A field-effect transistor, due to its extremely small mass, reaches thermal equilibrium in a matter of seconds and in most cases is completely stable after 20 seconds. A vacuum tube, on the other hand, might take as long as 10 to 15 minutes to reach thermal equilibrium, mainly because of heater requirements and the relatively large size of the elements.
2. Less heat dissipation: The low operating potential as well as the modest current requirements of the field-effect transistor result in an extremely low device dissipation; consequently, very little heat is transferred to the adjacent oscillator components even though they may be in close proximity. The negligible heat transfer produces a much more stable oscillator over-all.

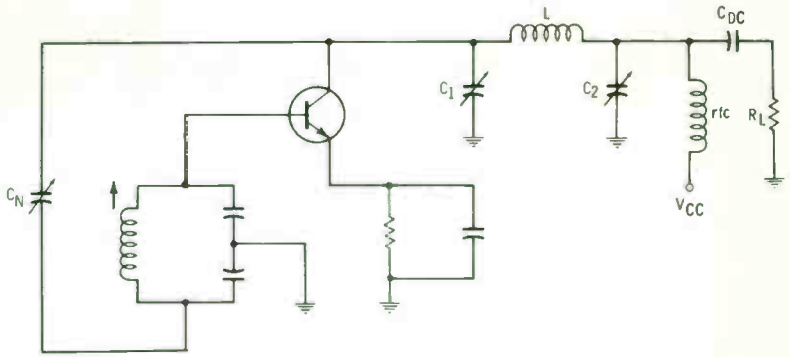
Fig. 13-7 shows two arrangements of the Hartley oscillator circuit. The circuit in Fig. 13-7A utilizes a bypassed source resistor to provide proper



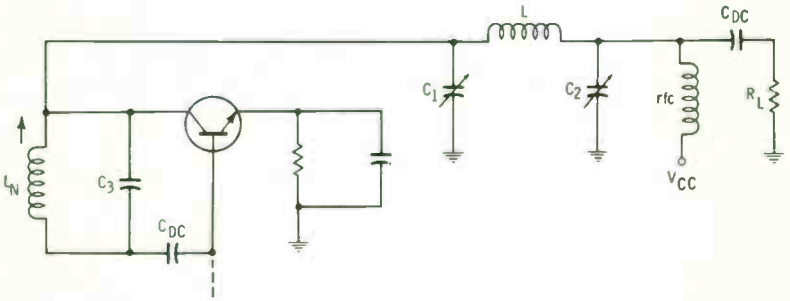
(*A*) *L output, separate coil.*



(*B*) *L output, tapped coil.*



(*C*) *Pi output, neutralizing capacitor.*

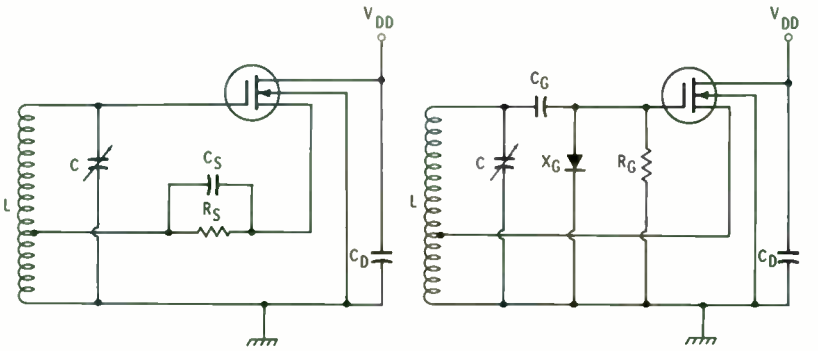


(*D*) *Pi output, neutralizing coil.*

Courtesy RCA Corp.

Fig. 13-6. Neutralizing and biasing methods.

operating conditions; the circuit in Fig. 13-7B utilizes a gate-leak resistor and biasing diode. The amount of feedback in either circuit is dependent on the position of the tap on the coil. Too little feedback results in a feedback signal voltage at the gate insufficient to sustain oscillation; too much feedback causes the impedance between source and drain to become so low that the circuit becomes unstable. Output from these circuits can be obtained through inductive coupling to the coil or through capacitive coupling to the gate.



(*A*) *Source bias.* (*B*) *Gate-leak bias.*

Courtesy RCA Corp.

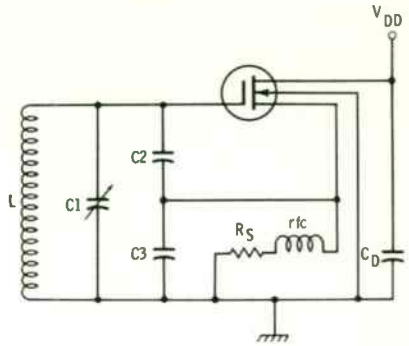
Fig. 13-7. Hartley oscillator circuits.

Fig. 13-8 shows the field-effect transistor in use in two forms of the Colpitts oscillator circuit. These circuits are more commonly used in vhf and uhf equipment than the Hartley circuits because of the mechanical difficulty involved in making tapped coils for use at these frequencies. Feedback is controlled in the Colpitts oscillator by the ratio of the capacitance of C2 to the capacitance of C3.

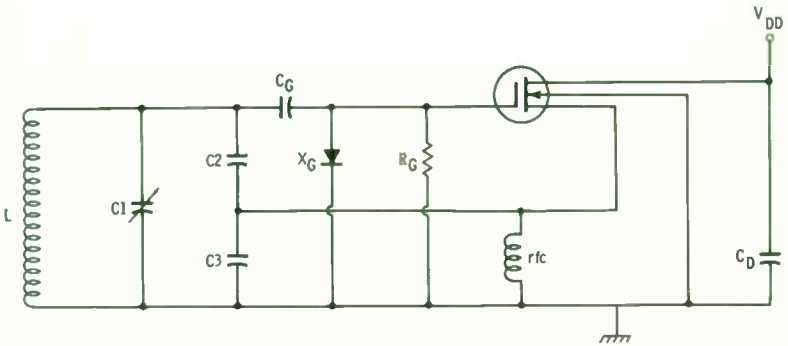
Fig. 13-9 shows gate-tickler-feedback oscillator circuits, and Fig. 13-10 shows drain-tickler-feedback oscillator circuits. These circuits have no particular advantages over the Hartley and Colpitts circuits, except that in some designs it might be cheaper to provide a tickler winding than a tapped coil or capacitive divider.

The field-effect transistor also operates well in crystal oscillator circuits such as the Pierce-type oscillator shown in Fig. 13-11. This oscillator is extremely popular because of its simplicity and minimum number of components. At frequencies below 2 megahertz, a capacitive voltage divider may be required across the crystal. The connection between the voltage-divider capacitors must be grounded so that the voltage developed across the capacitors is 180° phase reversed.

Frequently it is desirable to operate crystals in communications equipment at their harmonic or overtone frequencies; Fig. 13-12 shows two



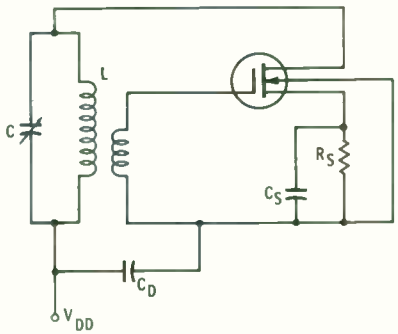
(A) Source bias.



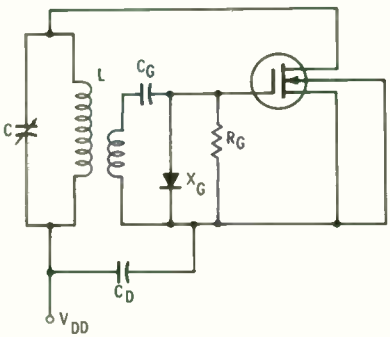
(B) Gate-leak bias.

Courtesy RCA Corp.

Fig. 13-8. Colpitts oscillator circuits.



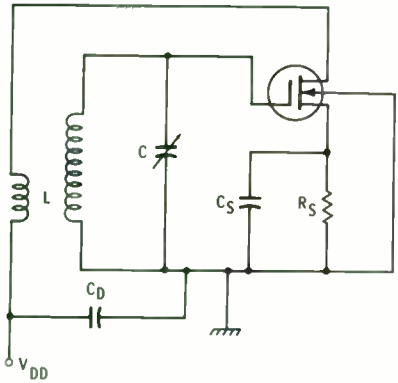
(A) Source bias.



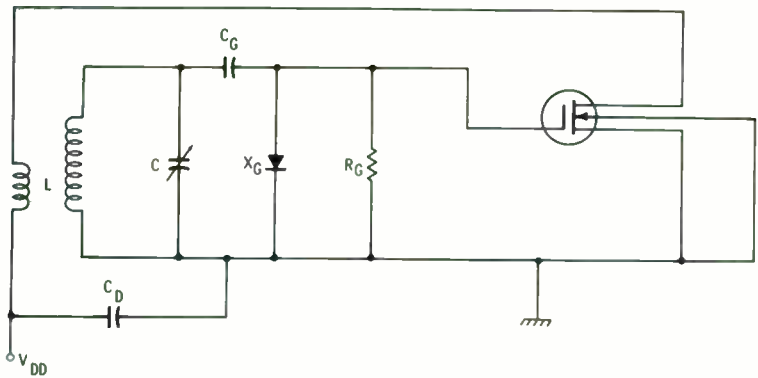
(B) Gate-leak bias.

Courtesy RCA Corp.

Fig. 13-9. Oscillator circuits with gate-tickler feedback.



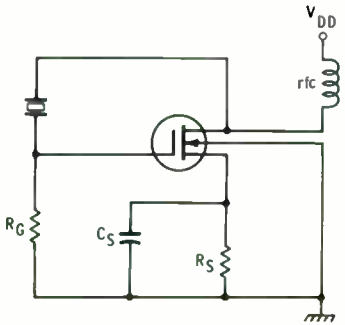
(A) Source bias.



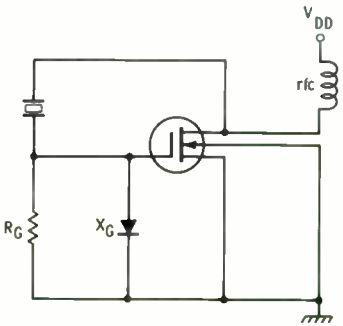
(B) Gate-leak bias.

Courtesy RCA Corp.

Fig. 13-10. Oscillator circuits with drain-tickler feedback.



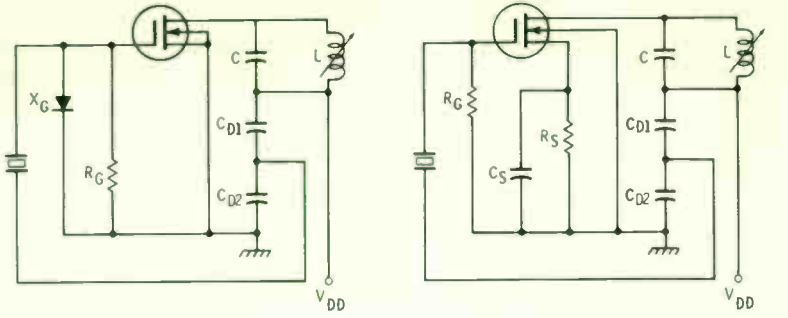
(A) Source bias.



(B) Gate-leak bias.

Courtesy RCA Corp.

Fig. 13-11. Pierce-type crystal-controlled oscillators.

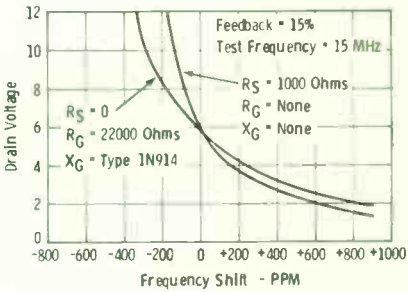


(A) Gate-leak bias. *(B) Source bias.*

Courtesy RCA Corp.

Fig. 13-12. Crystal oscillators for operation at harmonic frequencies.

circuits designed for this purpose. Additional feedback is obtained for the overtone crystal by the use of a capacitive divider as the tank bypass. Most third-overtone crystals operate satisfactorily without this additional feedback, but for the fifth and seventh harmonics, the extra feedback is required. The tanks in Figs. 13-12A and 13-12B are not fully bypassed and produce a voltage that aids oscillation. In both circuits, the crystal is connected to the junction of capacitors C_{D1} and C_{D2}; the ratio of these capacitors should be approximately 1:3.



Courtesy RCA Corp.

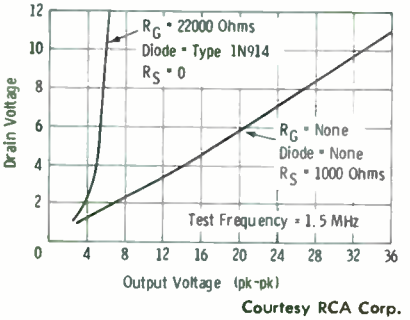
Fig. 13-13. Comparison of frequency stability for source and gate-leak biasing.

Many factors must be considered in the design of stable field-effect-transistor oscillators. For example, the frequency-determining components must be temperature stable, and the mechanical arrangement and construction of the oscillator must be such that no physical movement of the individual components is possible.

In each of the circuits of Figs. 13-7 through 13-12, two biasing arrangements are shown. One biasing arrangement makes use of a bypassed source resistor, and the other makes use of a gate resistor with a biasing diode. Experiments have been conducted to illustrate the effect on circuit performance of these biasing methods, and of changes in circuit param-

eters. The Hartley circuit was selected because of its popularity with most design engineers. Results of the experiments have been described as follows.

Five-percent feedback was attempted but proved insufficient to sustain oscillation. In both biasing methods, it appears that the best feedback level is somewhere near 15 percent. For comparison purposes, the 15-percent feedback stability curves for both biasing methods are plotted in Fig. 13-13. Note that under normal operation the source-resistor biasing method has a slight advantage over the method using a gate resistor and



Courtesy RCA Corp.

Fig. 13-14. Comparison of output-voltage stability for source and gate-leak biasing.

biasing diode. However, if output-voltage regulation is of any importance, the method using a gate resistor and biasing diode is far superior. Fig. 13-14 shows this result clearly.

EXERCISES

Q13-1. What is the ac "input power" to an oscillator?

Q13-2. What is the first and fundamental requirement for frequency stability of an oscillator circuit?

Q13-3. What parameter of the transistor has the greatest effect on frequency stability?

Q13-4. What effect does an increase of collector voltage have on the frequency of oscillation?

Q13-5. What effect does an increase of emitter voltage have on the frequency of oscillation?

Q13-6. If more than three RC feedback sections are used in a phase-shift oscillator, will feedback attenuation increase or decrease?

Q13-7. In the circuit of Fig. 13-3, if C2 should open, would the circuit cease to oscillate?

Q13-8. What is the meaning of the dots on L in the circuit of Fig. 13-6A?

Q13-9. What is the maximum frequency capability of a grounded-base oscillator compared to a grounded-emitter oscillator?

Q13-10. Why is neutralization necessary in a high-frequency rf amplifier?

CHAPTER 14

Logic Math Fundamentals

We have studied thus far basic circuit operation and theory with the purpose of developing techniques of analysis—knowing what a circuit is supposed to do, knowing what to expect in input and output waveforms, and determining the influence on the circuit of an immediately preceding or following stage. We are now entering a phase of application in which individual circuitry is only incidental to the operation of a system.

A considerable portion of "new breed" television and radio equipment involves the application of *logic systems*. We will need to break away (for awhile) from individual circuit concepts to *interconnection*, *organization*, and *system* (the net result desired) concepts.

Before exploring this type of concept, it is necessary to be introduced to *binary notation* and *boolean algebra*. This introduction will be very brief; only the "number notation" and its application in logic systems will be considered.

14-1. INTRODUCTION TO BINARIES

The *radix* for the conventional decimal number system is 10. For example, 2924 is $2000 + 900 + 20 + 4$, or $2 \times 10^3 + 9 \times 10^2 + 2 \times 10^1 + 4 \times 10^0$. (Note: $10^0 = 1$) As an example of fractions in the decimal system, 0.204 is $2 \times 10^{-1} + 0 \times 10^{-2} + 4 \times 10^{-3}$.

In the binary system, the radix is 2. All numbers are constructed on the basis of powers of 2. For example, 1001 is $1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$ (Note: $2^0 = 1$)

The first notation (1×2^3) is simply the 1 of the first digit of the number (1001) times 2 raised to the power which represents the number of digits remaining in the original number (3). Now to find the decimal equivalent:

$$1 \times 2^3 = 8$$
$$0 \times 2^2 = 0$$

$0 \times 2^1 = 0$

$1 \times 2^0 = 1$

Adding: $8 + 0 + 0 + 1 = 9$, decimal equivalent of binary 1001.

Binary Addition

From the above, construct the binary table as follows: Write down four zeros:

0000 (Make this equal to zero.)
0001 (Add 1.)
0001 (This equals 1 in the decimal system.)

Now we are going to add another 1 to get a decimal value of 2.

0001
0001

When 1 is directly under 1 in the binary system, the sum is zero, and 1 is carried to the next column to the left. If there is already a 1 in that column, the sum is again zero and the 1 carries to the left again, etc. So:

0001
0001
0010 (This equals 2 in the decimal system).

Now add another 1:

0010
0001
0011 (This is 3 in the decimal system, 1 + 1 + 1.)

Add another 1:

0011
0001
0100 (This is 4 in the decimal system, 1 + 1 + 1 + 1.)

The binary equivalents of the decimal numbers 0 to 10 are given in Table 14-1.

The radix in the binary system is 2 for both whole numbers and fractions. For example, binary 0.010 is $0 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} = 0 + (\frac{1}{2})^2 + 0 = 0 + \frac{1}{4} + 0 = 0.250$. Some binary fractions and their decimal equivalents are given in Table 14-2.

We have already noted that the digits on the left of the binary point are coefficients of increasing *positive* powers of 2, with 2^0 adjacent to

Table 14-1. Binary-Decimal Equivalents (Whole Numbers)

Binary	Decimal
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10

the binary point. So the digits on the right of the point are coefficients of increasing *negative* powers of 2, with 2^{-1} adjacent to the point.

For another example, the decimal equivalent of binary 100101.01 is found as follows:

Binary		Decimal
1×2^5	=	32
$+0 \times 2^4$	=	0
$+0 \times 2^3$	=	0
$+1 \times 2^2$	=	4
$+0 \times 2^1$	=	0
$+1 \times 2^0$	=	1
$+0 \times 2^{-1}$	=	0
$+1 \times 2^{-2}$	=	0.25
100101.01	=	37.25

The binary method requires only two digits, 0 and 1. All numbers can be expressed by combinations of zeros and ones. We can see the necessity of working with "powers of two," and Table 14-3 is very convenient.

Table 14-2. Binary-Decimal Equivalents (Fractions)

Binary	Decimal
0.000	0
0.001	0.125
0.010	0.250
0.011	0.375
0.100	0.500
0.101	0.625
0.110	0.750
0.111	0.875

With a math system employing only 0 and 1, an open circuit can signify 0, and a closed circuit can signify 1. So an open switch or relay, a blocked tube or transistor, an extinguished lamp, etc., may say 0. If the operation is reversed, the device says 1. In table 14-1, we have four places. How far can we go with four-place binary numbers in the decimal system? Let us see.

Starting with 1010 (binary 10), successively add binary 1 (0001) and obtain 1011 (or 11), 1100 (12), 1101 (13), 1110 (14) and 1111 (15). Now if we add 0001 again, we get 10000 (binary 16). So we have five places. This tells us that four "gates" (on-off devices) will handle up to the equivalent of 15 in the decimal system. So we need just four elements to display from zero to 15 events.

Table 14-3. Positive Powers of Two

Power of 2	Decimal Equiv.
2^0	1
2^1	2
2^2	4
2^3	8
2^4	16
2^5	32
2^6	64
2^7	128
2^8	256
2^9	512
2^{10}	1024
2^{11}	2048
2^{12}	4096

Complements in Binaries

We are now in a position to study the addition of positive and negative numbers in binary form. For example, consider the addition of 0101 and −0010. Note that in decimal form, this is 5 − 2. Binary technique here is: Change the sign of the negative number, *complement* this number, and add the result to the positive number.

To complement a binary number, we simply change all zeros to ones, change all ones to zeros, and *then add one.* Thus, to complement 0010:

$$\begin{array}{r} 1101 \\ +1 \\ \hline 1110 \end{array}$$

Then add the 1110 to 0101:

$$\begin{array}{r} 0101 \\ +1110 \\ \hline 10011 \end{array}$$

Now we *discard* the overflow digit in the answer and *replace it with either a plus or minus sign.* (NOTE: The overflow digit is the digit in the answer one place to the left of the leftmost digit in the two numbers added. In our example, the leftmost 1 in 10011 is the overflow digit.) *If the digit is a 1*, the sign is *plus.* If the overflow digit is a *zero*, the sign is *minus.* Thus the answer in our example is +0011. This is the binary notation for decimal 3, which satisfies the condition $5 - 2 = 3$.

When a negative number is added to a smaller positive number, the overflow digit is always zero, and the answer is always negative. When the result is negative, the number must be *recomplemented* to obtain the correct solution. For example: Add −1000 (decimal −8) to 0011 (decimal 3). First find the complement of 1000:

$$\begin{array}{r} 0111 \\ +1 \\ \hline 1000 \end{array}$$

Now add this to 0011:

$$\begin{array}{r} 1000 \\ +0011 \\ \hline 01011 \end{array}$$

Since the overflow digit is 0, we discard it and substitute a negative sign, giving −1011. Now to recomplement:

$$\begin{array}{r} 0100 \\ +1 \\ \hline 0101 \end{array}$$

So the answer is −0101. This is decimal number −5, which results from adding −8 to +3 in the decimal system.

Binary Subtraction

This is exactly the same as addition of positive and negative binary numbers. For example, subtract 0100 (decimal 4) from 1010 (decimal 10). First find the complement of 0100:

$$\begin{array}{r} 1011 \\ +1 \\ \hline 1100 \end{array}$$

Then add:

$$\begin{array}{r} 1010 \\ +1100 \\ \hline 10110 = +0110 \text{ (answer)} \end{array}$$

Note that 0110 is decimal 6, which is the result of subtracting decimal 4 from decimal 10.

Binary Multiplication, Digital Methods

Digital computers multiply by over-and-over addition, and divide by over-and-over subtraction. A 5-MHz flip-flop will perform five million such operations per second.

For over-and-over addition, we make use of two registers, the *accumulator* and the *multiplier*. The accumulator starts with all zeros, and the multiplier keeps account of the number of additions performed. To illustrate, let us start with conventional numbers and assume we want to multiply 462×232:

	Accumulator	Multiplier
1.	000000	232
2.	000462	
3.	000462	231
4.	000462	
5.	000924	230
6.	004620	
7.	005544	220
8.	004620	
9.	010164	210
10.	004620	
11.	014784	200
12.	046200	
13.	060984	100
14.	046200	
15.	107184 (Answer)	000

The above table shows the results of the following operations: In Step 1, we recorded zeros in the accumulator column, and the multiplier (232) in the right column. In Step 2, the multiplicand is recorded. Step 3 is the first addition, $000 + 462 = 462$. Since we have now made one addition, the multiplier is reduced by one, to give 231. In Step 4, we record the multiplicand again. In Step 5, $462 + 462 = 924$. The multiplier register is again reduced by one to give 230. The first-order digit of the multiplier is now zero, so in the next step, move the multiplicand one place to the left. (Now the multiplicand will be added *ten* times in each step.) In Step 7, add Steps 5 and 6 to get 5544, and reduce the multiplier by *ten*, to give 220. In Step 8, the multiplicand of Step 6 is repeated. In

Step 9, the sum of 5544 and 4620 is 10164. Put it down and again reduce the multiplier by ten to get 210. In Step 10, repeat the multiplicand as in Step 8. In Step 11, the total of Steps 9 and 10 is 14784. The multiplier is now 200. Now the second-order digit is zero, so in the next step you again move the multiplicand one place to the left. (Now the multiplicand will be added *100* times in each step.) In Step 13, record the new sum in the accumulator column, and reduce the multiplier by 100 to get 100. In Step 14, repeat the same multiplicand. In Step 15, the total is 107184; this is the answer, since the multiplier has been reduced to zero.

Now multiply binary 1011 × binary 11010:

	Accumulator	Multiplier	Operations
1.	000000000	11010	Move multiplicand one place left.
2.	000010110		Add.
3.	000010110	11000	Move multiplicand two places left.
4.	001011000		Add.
5.	001101110	10000	Move multiplicand one place left.
6.	010110000		Add.
7.	100011110	00000	This is the answer.

14-2. BASIC BOOLEAN ALGEBRA

Boolean algebra is old (about 1850), but its application is new. It has become an important link in understanding electronic computer and logic systems.

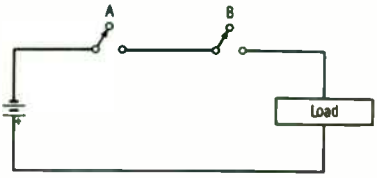
Fig. 14-1. Basic logic states.

This algebra is concerned with elements having only two possible stable states and no unstable states. It becomes very useful in representing switching circuits. A switch can be in only one of two possible stable states, "closed" or "open" (Fig. 14-1). The symbol "0" can represent an open switch and a "1" can represent a closed switch. From the outset remember this: The 0 and 1 *do not represent numbers;* they are shorthand for representing the presence or absence of a conducting path.

0 = open circuit, or nonconducting path.

1 = closed circuit, or conducting path.

In Fig. 14-2A, we have a simple circuit of two switches in series. Obviously, both switches must be closed to complete the circuit. If either switch A or B is open, the state is 0. If both are closed, the state is 1. If we



(*A*) *Basic function.*

Truth Table (AND)

Condition	A	B	f (A, B) = AB
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	1

(*B*) *Truth table.*

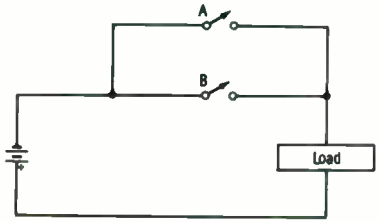
(*C*) *Diagram symbol.*

Fig. 14-2. Fundamentals of an AND circuit.

draw up a "truth table" for this circuit as shown in Fig. 14-2B, we list all the possible states of the switches under A and B, and derive the function of A and B in the last column. Condition 1 is with A and B open (0 state), so function f(A,B) is also 0. Conditions 2 and 3 have only one switch closed (state 1) at a time, so the function of A and B is still 0. Condition 4 is with both A and B in the closed (1) state, and therefore f(A,B) = 1. We should recognize this as an AND (coincidence) circuit. Both A and B must be in the 1 state for a current to exist in the load. The symbol AB is read "A *and* B." It *does not* mean the product A × B as in conventional algebra.

Shown in Fig. 14-2C is the diagram symbol for the AND circuit. When we see this symbol without further identification, we must recognize it as an AND circuit. When a regular block is used, it will be labelled "AND."

We should now readily see the significance of Fig. 14-3, except for one thing. The expression A + B is read "A OR B," *not* "A plus B." This is

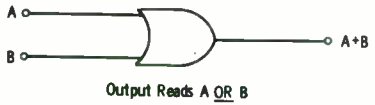


(*A*) *Basic function.*

Truth Table (OR)

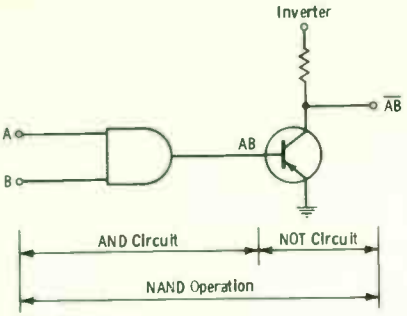
Condition	A	B	f (A, B) = A+B
1	0	0	0
2	1	0	1
3	0	1	1
4	1	1	1

(*B*) *Truth table.*



(*C*) *Diagram symbol.*

Fig. 14-3. Fundamentals of an OR circuit.



(A) Diagram.

Truth Table (NAND)

A	B	AB	f(A, B) = $\overline{AB}$
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

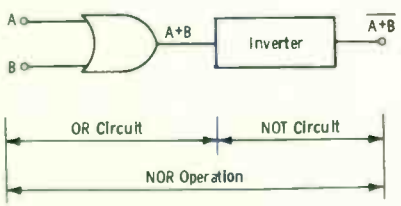
(B) Truth table.

Fig. 14-4. Fundamentals of a NAND circuit.

an OR circuit. The truth table of Fig. 14-3B can be seen to be true if we think of the logic involved. The expression A + B means A OR B, which is function f(A,B). So if A or B takes the value of 1 (switch closed), then f(A,B) must equal 1. Compare this to the logic of the AND circuit (Fig. 14-2).

Now if 0 is an open circuit and 1 is a closed circuit, what happens when a signal resulting from a given state goes through a phase reversal? Just what we would expect! See Fig. 14-4A. We have an AND circuit feeding the base of a transistor. The AND-circuit output is A AND B, so if both inputs are 1's, the base is in a 1 state (condition 4 of the truth table, Fig. 14-2B). This signal is inverted at the collector, so the output is now a 0 state, or NOT AB (signified by a line over AB, or $\overline{AB}$). The entire circuit is now termed a NAND circuit. This simply means we have an inverted AND, or NOT AND, operation, which is to say an AND circuit with phase reversal.

Note that the first three columns of the NAND truth table (Fig. 14-4B) are a copy of the AND truth table in Fig. 14-2B. But the inverted output changes all 0's to 1's, and the 1 to a 0. Note that the whole quantity AB,



(A) Diagram.

Truth Table (NOR)

A	B	A+B	f(A, B) = $\overline{A+B}$
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

(B) Truth table.

Fig. 14-5. Fundamentals of a NOR circuit.

not the separate variables of individual switch states, is complemented (reversed).

Fig. 14-5 shows the same kind of logic applied to an OR circuit. When the phase is reversed, the state becomes NOT A OR B (designated $\overline{A+B}$). Compare the resulting truth table (Fig. 14-5B) with the one in Fig. 14-4B.

For Figs. 14-6 through 14-11, a positive signal is defined as 1. Here is the way to look at these circuits:

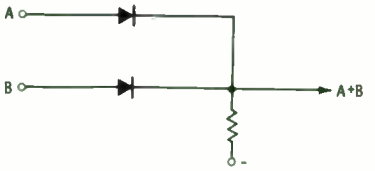


Fig. 14-6. Diode-logic OR circuit.

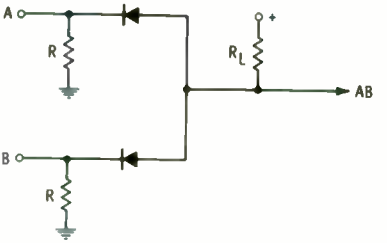


Fig. 14-7. Diode-logic AND circuit.

Fig. 14-6 shows a *diode logic* (DL) circuit. If a positive pulse is applied to either input A or B, A OR B will appear at the output.

Fig. 14-7 is also a diode logic circuit, but in this case the diodes are forward biased through their respective resistors. If a positive pulse is applied to only one of the inputs, the other diode is still conducting, providing a low-impedance bypass to any signal change. So the voltage at the output remains low. If positive pulses are applied to *both* inputs simultaneously, the diodes are open switches, and the output rises to the R_L supply voltage. This is an AND (coincidence) circuit.

A *direct-coupled-transistor* logic (DCTL) circuit is shown in Fig. 14-8. A positive pulse applied to only one of the inputs still leaves the other transistor without forward bias. Therefore, the switch is still open, and no change occurs at the output. A positive pulse must be applied to *both*

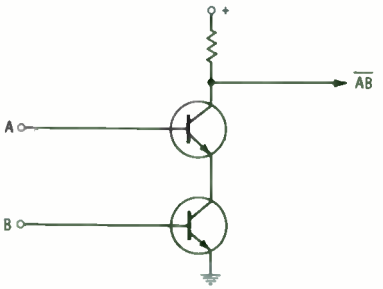


Fig. 14-8. Direct-coupled-transistor-logic NAND circuit.

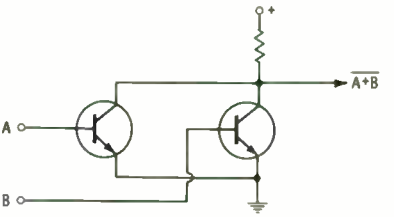


Fig. 14-9. Direct-coupled-transistor-logic NOR circuit.

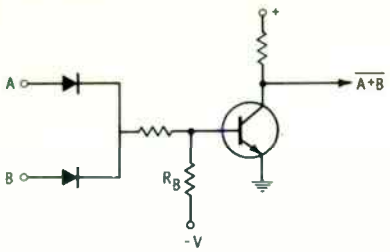


Fig. 14-10. Diode-transistor-logic NOR circuit.

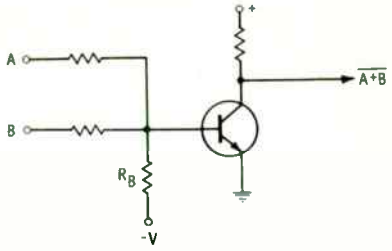


Fig. 14-11. Resistor-transistor-logic NOR circuit.

inputs simultaneously to close the switch. Since phase inversion occurs, the circuit is a NOT AND, or NAND, circuit.

Another DCTL circuit is shown in Fig. 14-9, but in this case a positive pulse appearing at either input will appear inverted at the output. So this is a NOT OR (NOR) circuit.

The diagram in Fig. 14-10 represents a *diode-transistor logic* (DTL) circuit. Here we recognize an OR circuit followed by a NOT circuit (NOR operation).

The *resistor-transistor* logic (RTL) circuit in Fig. 14-11 is the same as the circuit of Fig. 14-10 except that resistors are used instead of diodes. When capacitors are used around the resistors (to enhance switching speed), the circuit is termed resistor-capacitor-transistor logic (RCTL).

Instruction manuals for modern solid-state equipment bristles with the above terminology. Regardless of how complex the circuits may look at first glance, they work on these principles.

NOTE: Exercises are deferred to the end of Chapter 15 so that logic math and logic circuitry can be covered at the same time.

CHAPTER 15

Basic Logic Circuitry and Applications

We are going to have to get well acquainted with the term "logic," and know how to read "schematics" of logic systems. It makes no difference in what field we are engaged, electronic equipment is absorbing an ever increasing amount of "logic."

With such gear, servicing as we have known it will not exist. Some present applications, and a great number of upcoming broadcast and commercial applications, use "chips" (a single chip can replace a fantastic number of transistors) on printed-circuit or etched-wiring boards. Does this mean our transistor studies are all in vain, except as a transition from vacuum tubes through transistors to chips? Certainly not. Our study and experience with transistors will make the new field of microminiaturization a "natural." And please rule out any thought that new systems will do away with the maintenance job! The only way this can happen is for us to fail to keep up with the times; and *this* is nothing new in the technical field.

15-1. LOGIC-SCHEMATIC NOTATION

"Schematics" of many logic systems are quite simply block or flow diagrams with certain symbology that tells what is expected of the circuit. We can't service a single "stage" of a microminiature block; we must know how to check for the trouble and then replace a single plug-in "block" on a board, or an entire card of blocks in a multiple-card module.

In Fig. 15-1A we have the familiar series of pulses making up a square wave. Now simply add an L (for low, or negative-going pulses) and an H (for high, or positive-going pulses).

Fig. 15-1B lists the nomenclature applied in logic systems. Column 1 repeats what we have just done; we have a "high-level" or a "low-level" point. Column 2 repeats what we learned in Chapter 14. Column 3 says

Column	1	2	3	4	5	
	Hi	1	+	0	True	etc.
	Lo	0	0	-	False	

(*A*) *Pulses.* (*B*) *Nomenclature.*

Fig. 15-1. Pulse nomenclature for logic systems.

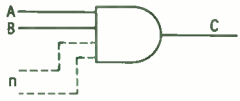
the "high" level can be a plus voltage and the "low" level can be ground, or zero volts. Column 4 reminds us that the high level can be zero volts (common or ground) and the low level can be a minus voltage. In either case, the "high" level is positive relative to the low level. Column 5 says that "1" can be "true" and "0" can be "false." This can be reversed, depending upon application. Further columns would be limited only by our imagination; they could be "John" or "Mary," "go" or "no-go," etc.

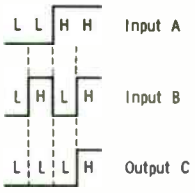
Fig. 15-2A shows the symbol for an AND (coincidence) gate. (Remember that any number of inputs could exist, not just two.) The input waveforms and corresponding output waveforms are shown in Fig. 15-2B. Please note a significant fact here: When both the A and B inputs are low (0), the output at C is also low, or zero. But the *same* output condition exists when inputs A and B have pulses of *opposite polarity* applied. The significance of this fact is that the *coincidence* of two *positive* pulses at the inputs is the "reference" operation; it is the *only* operation which results in a change of output waveform.

Fig. 15-2C is the corresponding truth table. This table is much more convenient than drawing out waveforms for A, B, and C. Again, it tells us that the reference operation (the only condition causing a change in output level) is for two coincident positive pulses (or High, or 1, etc.) to be present at the inputs.

Question: Look at Fig. 9-9. This is an AND gate (coincidence gate without inversion). Does it fit the function of the circuit we are now covering?

Answer: In the circuit of Fig. 9-9, the biasing is such as to result in a saturated transistor in the absence of pulses. This requires coincident





Input		Output
A	B	C
L	L	L
L	H	L
H	L	L
H	H	H

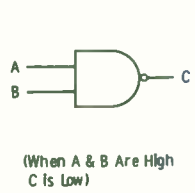
(*A*) *Symbol.* (*B*) *Waveforms.* (*C*) *Truth table.*

Fig. 15-2. Coincidence (AND) gate.

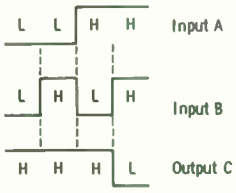
negative pulses at the inputs to change the output level. Therefore the circuit differs from that of Fig. 15-2. How could we make the two circuits behave in the same way? We could use an npn transistor in Fig. 9-9 and reverse the dc polarities.

Question: Look at Fig. 14-7. Does this circuit fit the function of the circuit we are now covering?

Answer: Yes.



(*A*) *Symbol.*



(*B*) *Waveforms.*

Input		Output
A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

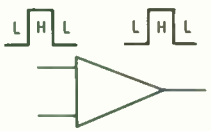
(*C*) *Truth table.*

Fig. 15-3. NAND gate.

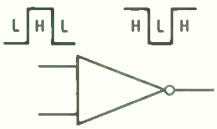
Fig. 15-3A shows the symbol for a NAND gate (NOT AND, or AND gate with inversion). Note the small circle at the output end of the symbol; this circle indicates signal inversion. From the waveforms of Fig. 15-3B, observe that coincident high-level pulses must occur at the input to change the output to the low level. Note that column C of the truth table of Fig. 15-3C is just opposite to that of Fig. 15-2C.

Question: Observe Fig. 9-11. Does this NAND circuit fit the function of the circuit we are now covering?

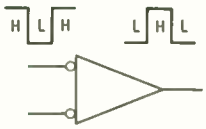
Answer: Coincident positive input pulses are required to result in a changed level (negative-going) at the output. This behavior fits the circuit we are now covering.



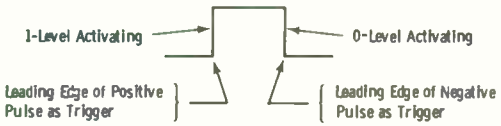
(*A*) *Noninverting stage.*



(*B*) *High-level activated.*



(*C*) *Low-level activated.*

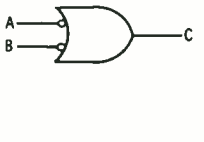


(*D*) *Triggering waveform.*

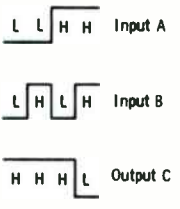
Fig. 15-4. Inversion in logic stages.

In Fig. 15-4A, we have the "triangle" representation of any stage that is noninverting. (NOTE: In logic circuitry, this symbol is normally replaced by the block symbol of an AND or OR circuit.) In Fig. 15-4B, we have the circle at the output, designating that the low-level output is the reference. This symbol represents a "high-level-activated" device, because the high level is required to change the output to a low level. In Fig. 15-4C, the circles are at the inputs. Now we have a "low-level-activated" device; low-level inputs are required for a high-level output.

Fig. 15-4D illustrates that a 1 (high-level) activation is the leading edge of a positive pulse. This is the same as the trailing edge of a negative pulse. Also, a zero (low-level) activation is the leading edge of a negative pulse. This is the same as the trailing edge of a positive pulse. These relationships should help to keep the comprehension of "levels" in proper perspective.



(*A*) *Symbol.*



(*B*) *Waveforms.*

Input		Output
A	B	C
L	L	H
L	H	H
H	L	H
H	H	L

(*C*) *Truth table.*

Fig. 15-5. OR gate with phase inversion.

In Fig. 15-5A we have the most common symbol for the OR gate with phase inversion added; therefore a NOR gate is indicated. The circles on the inputs designate a low-level-activated device; if either input A or B is *low*, the output will be *high*. Fig. 15-5B shows the waveforms, and Fig. 15-5C is the more convenient truth table for this circuit function.

Question: Does the circuit of Fig. 14-5 fit this function?

Answer: Note carefully that function A + B (read "A or B") is the ***noninverted*** OR function, and indicates that if either input is high, the output is high. Then the ***inverted*** function $\overline{(A+B)}$, which is read "not A or B," is low (or zero) at the output only when either input is high (or 1). Therefore this condition is opposite to that of Fig. 15-5, and would be a high-level-activated NOR circuit.

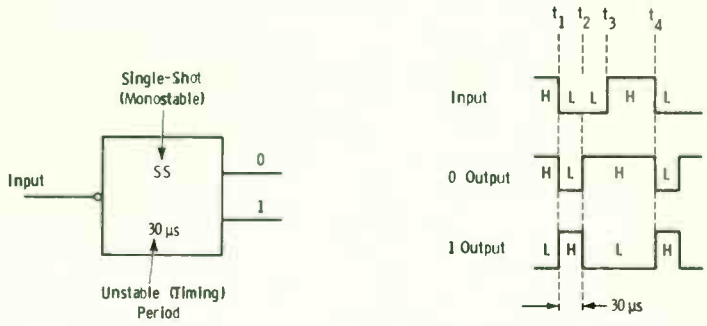
Question: Does the circuit of Fig. 9-12 fit the condition we are now covering?

Answer: We should recognize this circuit as actually being a NOR gate, since phase inversion occurs. Note that when either input is low (negative), the output is high (ground or zero). When both inputs are high, the output is low, in this case negative potential V_{CC}. Therefore, this circuit does fit the condition of Fig. 15-5.

Question: How could we change the circuit of Fig. 9-12 to fit the function called for in Fig. 14-5?

Answer: We could use npn transistors, and reverse the dc and pulse polarities.

Fig. 15-6A shows a block with the labels "SS," "30 μs," "0," and "1." The SS means single-shot (monostable) multivibrator, the 30 μs indicates the unstable (timing) period, and the two outputs (one from each side of the MV) are designated as the 0 output and the 1 output. Some schematics say "OS" (for one-shot MV), which is the same as "SS" (single-shot). In addition, note that the input line is terminated in a circle. This circle indicates to us that when the input is at low level, we have the "reference" polarity of output signals.



(*A*) *Symbol.* (*B*) *Waveforms.*

Fig. 15-6. Monostable multivibrator.

Now study the waveforms of Fig. 15-6B. Prior to time t_1, the input is high, the 0 output is high, and the 1 output is low. (Multivibrators were covered in Chapter 10). At time t_1, the input swings low. This action triggers the single-shot MV into its unstable state (which in this example has a duration of 30μs); thus the 0 side transfers from high to low, and the 1 side transfers from low to high. This condition prevails for the built-in timing period of 30 μs, and then at t_2 the outputs reverse polarity again. Now remember that the single-shot must wait for another "low" (negative-going) trigger before it can operate again. Thus from t_2 to t_4 the outputs remain unchanged. At t_4, the timing period starts again (negative, or low, input pulse).

Note carefully that only during the timing period, which was initiated by the negative-going transistion, is the "1" output really 1, and the"0" output really zero (or low). This is the "reference" pulse mentioned before.

Question: Look at Fig. 10-1C. Tell which side of this multivibrator is the 0 and which is the 1 output to meet the conditions of Fig. 15-6.

Answer: We ought to see immediately why this circuit cannot meet the condition of Fig. 15-6. This is quite simply because, in Fig. 15-6, the unstable (timing) period must be initiated by a *low* (negative-going) pulse. Since the input side of Fig. 10-1C is a pnp boxcar, it is cut off only by a positive pulse.

Question: Look at Fig. 10-1D. Tell which side of this multivibrator is the 0 (low) and which is the 1 (high) output (Fig. 15-6).

Answer: When the input goes negative, Q2 is saturated, and its collector changes from −10 volts to ground; therefore this is the 1 output. The Q1 collector changes from ground to −10 volts; therefore this is the 0 (low) output.

15-2. SET AND RESET IN LOGIC CIRCUITS

Being what it is, a logic circuit must "recognize" certain conditions as well as "remember" a preceding condition. Study Fig. 15-7. We should

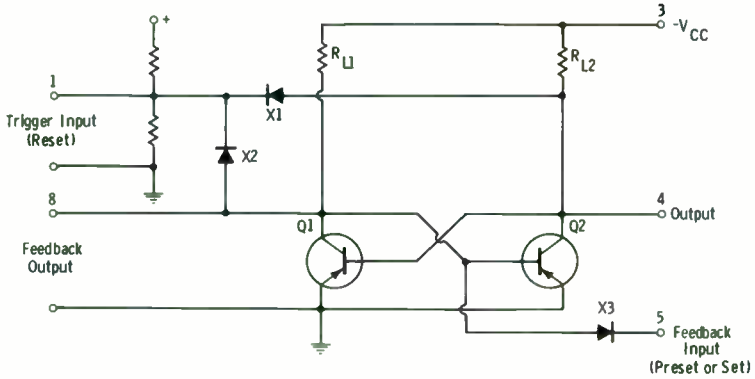


Fig. 15-7. Binary with preset or set input.

immediately recognize X1-X2 as the negative-pulse steering for binary Q1-Q2. A negative trigger-pulse input at point 1 will turn on whichever transistor is off; it has no effect on the transistor already on, since that base is already negative. The arrival of the next negative trigger will again reverse (reset) the state of the binary. All of this is review. The *new* element introduced here is that the above action will occur *only* if there is no conflicting information from X3; that is, if X3 is an open switch. Thus if X3 has been opened, the binary has been *preset* or *set* to operate as an ordinary binary (divide-by-two) multivibrator. The output at point 4 will be zero voltage when Q2 is saturated, and $-V_{CC}$ when Q2 is open.

In Fig. 15-8A we have three of the binaries of Fig. 15-7 interconnected to form a chain. Normally (without the feedback loop) we would have

2^3, or 8-to-1, division. But now let us see how the action is modified by feedback from the third binary to the first one.

See the waveforms of Fig. 15-8B. The output (point 4) of binary 3 is in a 0 state at the extreme left of the drawing. Therefore, Q2 of that binary is cut off (open switch) so that the output voltage is $-V_{CC}$. Also, Q1 of that binary is saturated, so point 8 is at ground. Since point 8 is connected back to X3 (point 5) of the first binary, this X3 is open (no forward bias), and binary 1 is counting.

After four input pulses to the first binary, Q1 of the third binary is changed from saturation to cutoff, and point 8 goes negative. This voltage is fed back (through a slight delay so as not to disturb the triggering of the second binary) to point 5 of binary 1. Now X3 of the first stage is forward biased and immediately brings the Q2 base to a negative value. So Q2, which was driven to cutoff at the trailing edge of the pulse shown as number 4 in the input waveform, is immediately set back to a 1 state. The resulting pulse serves as the *first* of the next group of four pulses applied to binary 2. The result is that after only seven pulses from the input triggering signal, the last counter again triggers, setting the first binary to repeat the cycle. This is most evident in the waveform at point 4 of binary 1; note the "set" occuring at the trailing edge of input pulses 4 and 11 (seven-pulse interval). Thus this group of three binary scalers produces a count of 7 to 1 rather than the normal 8 to 1 obtained when no feedback loop is employed.

When binary scalers are used as counters in sync generators, the method just described is the fundamental principle upon which they operate. The action of a chain of binary counters of any given number of units, with a feedback loop from the last unit to any preceding one in the chain, has the following relationship:

$$\text{Total division} = 2^n - 2^p$$

where,

n is the total number of binary scalers, and

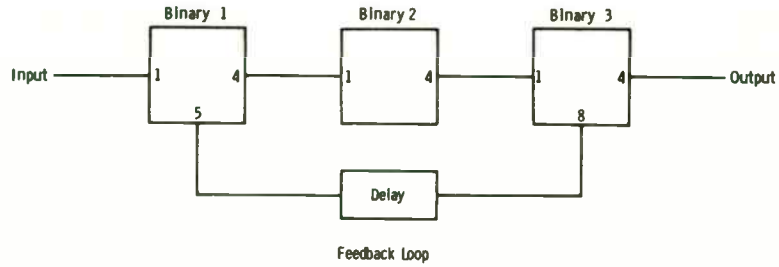
p is one less than the order number of the scaler to which feedback from the output scaler is applied.

If the feedback pulse is applied to the first scaler, $p = 0$; if it is applied to the input of the second scaler, $p = 1$; if it is applied to the third scaler, $p = 2$; etc. Thus for Fig. 15-8, $2^n - 2^p = 2^3 - 2^0 = 8 - 1 = 7$. If this is not clear, review Table 14-3 and the related text in Chapter 14.

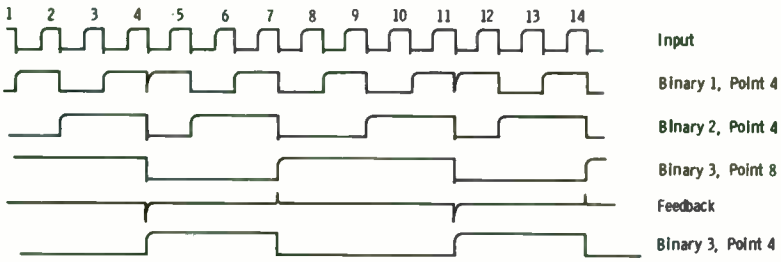
NOTE: The three binaries of Fig. 15-8 represent the 7-to-1 counter section of a 15-7-5 counting system for a sync generator.

15-3. HOW TO LOOK AT LOGIC SYSTEMS

Logic systems are comprised of a number of individual circuits whose states are generally in the 0 or 1 condition; these individual "blocks" are



(A) Diagram.



(B) Waveforms.

Fig. 15-8. Divide-by-seven counting chain.

interconnected in such a way as to perform a specified function. We must know this function to be able to analyze the system.

Let us take a common application in modern TV systems to show what we mean. See Fig. 15-9. When color equipment is to be integrated with monochrome systems, the horizontal drive and blanking must be delayed to all monochrome cameras, and sync must be delayed to the switcher (or sync insertion point). This delay is necessary because the signal is delayed approximately 1.2 microseconds in color equipment. The monochrome camera horizontal drive and blanking must be delayed a corresponding amount, and sync must be delayed to provide the same

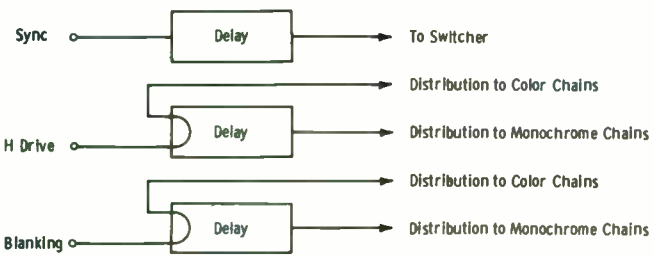
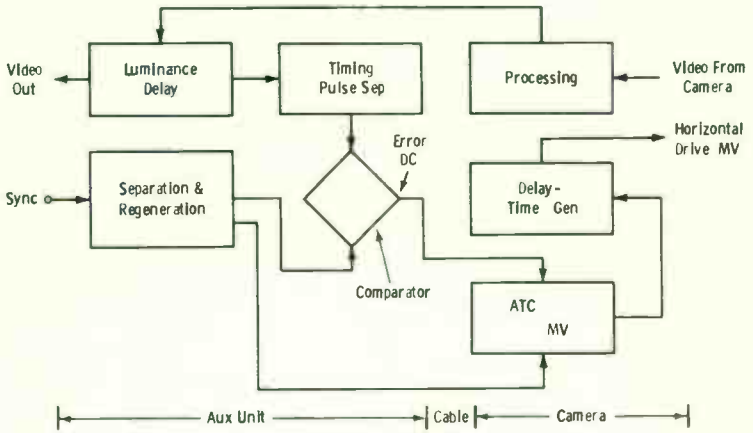


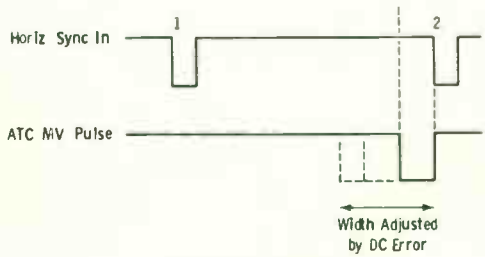
Fig. 15-9. Integration of color and monochrome equipment (old system).

front-porch width regardless of whether the source is monochrome or color.

Actually, the same problem exists in monochrome-only practice when studios are widely separated, with some cameras close to the sync source and others far away (governed by the length of the cables used from the control units to the cameras). There is about 1.5 microseconds of delay per 1000 feet of coaxial cable, so it is necessary to use delayed pulses for "near" cameras to match the "far-camera" delays.



(A) Diagram.



(B) ATC pulse.

Fig. 15-10. Integration of color and monochrome equipment (new system).

The new breed of TV broadcast equipment is bypassing this problem by regenerating its own drives and blanking, sensing the delay occurring, and then advancing drives to compensate exactly for this delay.

See Fig. 15-10A for the basic idea of how each camera chain in "new" systems automatically adjusts camera timing for proper phasing at the final switching point. We are illustrating here only the timing of horizontal sync (as separated from incoming composite sync from the sync gen-

erator), which is then used to regenerate blanking and horizontal drive to the camera. The basic idea is to sense the delay through the individual camera system (including luminance delay in color chains), compare it to incoming sync, and derive an error voltage (dc) to control camera drives and blanking to exactly compensate for this delay.

Horizontal sync is separated and regenerated to obtain a constant level regardless of the incoming level. One regenerated output goes to an automatic time correction (ATC) multivibrator; the width of the multivibrator output pulse depends on a dc control voltage from the comparator (Fig. 15-10B). The comparator derives a dc voltage dependent on the phase difference between the regenerated sync and a timing pulse carried through the system as shown in the block diagram. Because the leading edge of the ATC pulse is used to derive horizontal drive and blanking, the camera signals are advanced relative to incoming sync timing. The amount of advance depends on the corresponding cable length between the Auxiliary and Camera units, and the amount of delay in the processing of video. This is to say that the pulse in the camera corresponding to a given video line is initiated by the sync pulse corresponding to the preceding line.

Naturally this is only one limited example of a particular "logic" function. But it is the type of information we need to know about *any* system which is interconnected to compute, recognize, or remember an intended result. Always get this visualization first; in case of trouble calling for tracking down a malfunction, we must then test in entire blocks which are associated with an individual function of the system as a whole.

As a simple example, take the case of the binary-scaler counting system used to derive a nominal 60 Hz from the 31.5-kHz master oscillator. Due to the presence of feedback required for proper operation, pulses occurring during abnormal operation are meaningless. There is only *one* logical approach to tracing down the offending circuit; this is by complete "block" testing first. For example, assume we have the 15-7-5 binary chain discussed earlier. We have random or unusable 60-Hz output from the counter chain. Here is the way we test:

1. First scope the 31.5-kHz pulse output from the master oscillator. If these pulses are of normal amplitude and frequency, as quickly judged from the calibrated scope time base, adjust the scope time base to get *exactly* 15 cycles in the full 10 centimeters of the scope graticule.
2. Now go to the output of the 15-to-1 counter. There should be *exactly one* cycle in the 10 centimeters of the scope graticule. If the signal is correct here, adjust the scope time base to get *exactly* seven cycles in 10 centimeters. (NOTE: The feedback trigger may have to be removed, in which case the count is greater than 15 to 1.)
3. Next, scope the 7-to-1 counter. There should be *exactly one* cycle

in 10 centimeters at this output. If there is, adjust the scope time base for exactly five cycles in 10 centimeters.

4. Now scope the 5-to-1 counter. There should be exactly one cycle in 10 centimeters at the output.

If we discover trouble in the 15-to-1 counter, we still do not know which of the four binaries is faulty. But we *have* isolated the trouble to these four "blocks"; we know the 31.5-kHz master oscillator is working. (This is obvious in the first place if the divide-by-two stage for horizontal timing is working.) Scoping of the four individual transistors making up the 15-to-1 counter is sometimes useless, depending on the nature of the trouble. It is now necessary to go to voltage checks and transistor or component tests. If the trouble is in the 7-to-1 or 5-to-1 counter, we have just three binary stages involved.

NOTE: In some cases a *succeeding* counter can be malfunctioning so badly that waveforms at the output of a counter chain look erratic. When in doubt, disconnect the interconnecting diode or capacitor, and note if the output is affected. Trouble can, of course, also be caused by a defect in the coupling diode or capacitor itself.

15-4. LOGIC APPLICATIONS IN AUTOMATIC CONTROL

The need is pressing for a good visualization of solid-state logic circuitry as used in broadcasting. Therefore, let us apply what we already know to specific applications in am/fm automation circuitry.

Refer to Fig. 15-11. Output H will apply high voltage to the final stage of a transmitter if:

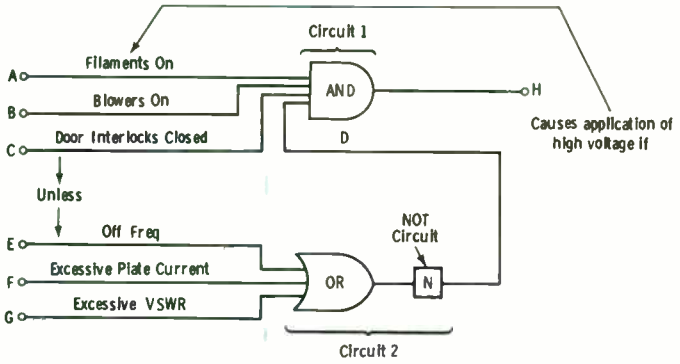
Filaments are on,
Blowers are on,
Door interlocks are closed,

but not if:

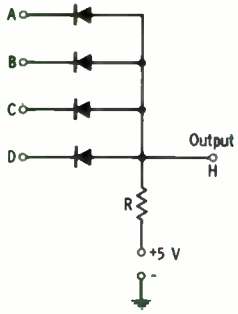
Exciter is out of frequency limits,
Final-stage plate currents are excessive when power is applied,
VSWR is excessive when power is applied.

These conditions mean that output H will be logic 1 when all the inputs (A, B, C, and D) to the AND circuit are logic 1. Inputs A, B, and C are logic 1 if the corresponding conditions are satisfied. The NOT output (which provides input D) will be 1 if inputs E, F, and G are all at logic 0. If any one of these inputs becomes logic 1, the OR output is logic 1. Since this output is complemented (inverted) by the NOT circuit, output D becomes a 0, and high voltage is not applied because output H of the AND gate will be at logic 0.

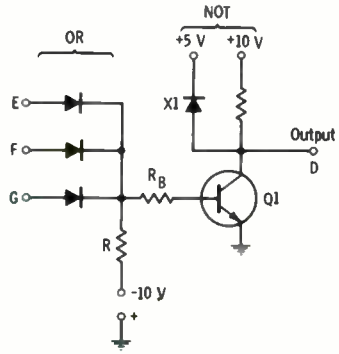
We ought to be able to understand the action of Circuit 1 and Circuit 2 from previous studies, but let us very briefly review how they work.



(A) System diagram.



(B) Circuit 1.



(C) Circuit 2.

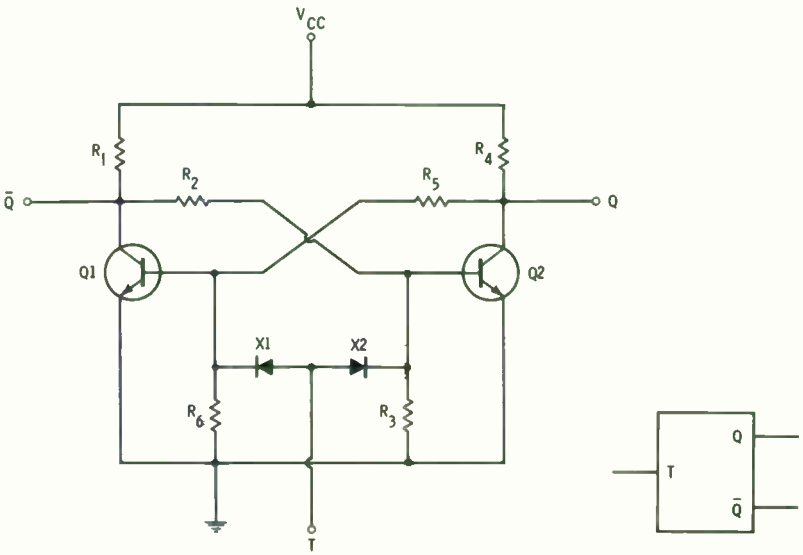
Fig. 15-11. Logic circuits for transmitter high voltage.

In Circuit 1 (AND gate—Fig. 15-11B), if all inputs are at logic 1, the resulting positive potential at the diode cathodes holds the diodes at cutoff, and there is no current through resistor R. Therefore the potential at H is at plus 5 volts, or logic 1. If any one of the inputs goes to logic 0, the associated diode cathode is essentially returned to ground, and the diode conducts. Therefore the voltage at H drops to ground potential (minus the small forward voltage drop across the diode), and the output voltage becomes essentially 0 (logic 0). So we can see that *all* the inputs must be at logic 1 to have logic 1 at the output.

In circuit 2, we need to consider the OR gate and NOT gate separately. If *any* of the inputs to the OR gate is at logic 1, the diode will conduct, and the voltage at the junction of R and R_B will be essentially the positive voltage applied to the diode. This back-biases the other diodes, and the OR-gate output goes to logic 1. If all inputs are at logic 0 (ground), the voltage at the R-R_B junction goes to zero minus the small forward voltage drop across the diodes.

Now consider the NOT circuit. When the base of Q1 goes positive (indicating a logic 1 from the OR circuit, which in turn indicates a faulty-condition input), the transistor is saturated and output D goes to essentially ground potential. So the AND circuit will not apply high voltage to the transmitter, since input D is at logic 0. When the Q1 base is returned to ground (all inputs to the OR circuit are at logic 0), the transistor is cut off, and output D goes to plus 5 volts, or logic 1.

There is just one thing we might not see immediately; what is the purpose of X1 in the collector circuit of Q1? This diode simply prevents the logic-1 output from exceeding 5 volts. When Q1 is not conducting, X1 becomes forward biased and clamps the logic-1 output to plus 5 volts. When Q1 is saturated, X1 is reversed biased and effectively out of the circuit. This technique is used when it is desirable to match all input levels to the AND gate.



(A) Schematic. *(B) Symbol.*

Fig. 15-12. One form of JK flip-flop.

Shown in Fig. 15-12A is the basic schematic of a circuit known as a *JK flip-flop*, or *toggle*, which is becoming quite popularly used. Fig. 15-12B is the symbol for the JK.

The JK has a single trigger input (T), and two outputs (Q and $\bar{Q}$) which are complements of each other, as shown. For each trigger pulse the state is reversed; the logic-1 output goes to logic 0, and the logic-0 output goes to logic 1. The input trigger is required for the change of mode.

As a brief review, assume Q2 is saturated (logic 0). A positive trigger at T will not affect Q2, since it is already saturated. But X1 will conduct and turn on Q1. Thus the state of the bistable is reversed and will remain so until the next positive trigger at T.

Most logic circuitry today is made up in integrated circuits (ICs). Therefore, it is normally necessary to know how to check inputs and outputs with a scope to isolate troubles in logic circuitry where the entire chip would need replacing. So let us go through the timing diagram of Fig. 15-13 to show how it is done.

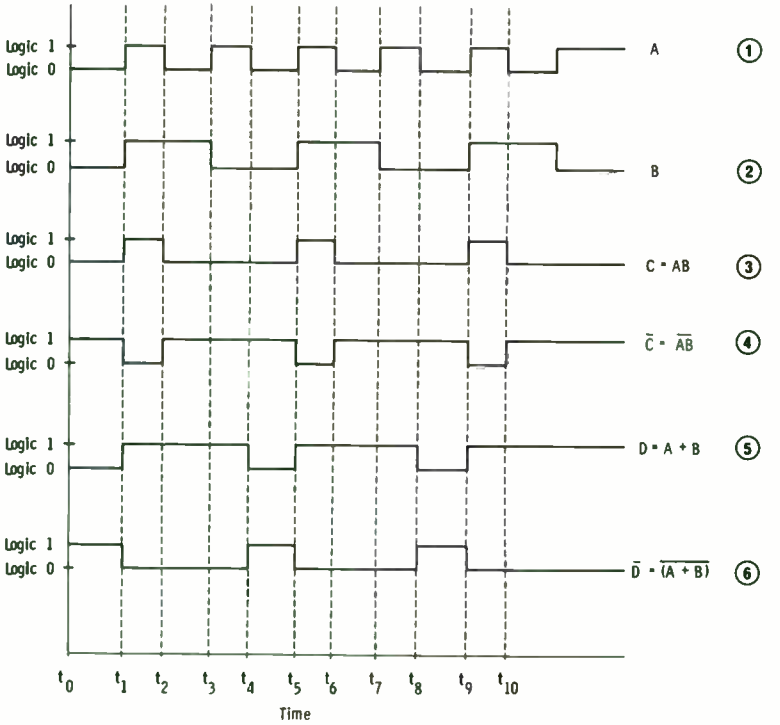


Fig. 15-13. Timing diagram.

IMPORTANT NOTE: Pulses are rarely as perfectly shaped as indicated on such drawings as Fig. 15-13. We will usually find some rounding in practice, and this may be normal. It is always desirable to scope such circuitry when it is working perfectly to ascertain the normal shape of pulses in any particular equipment.

In the timing diagram chosen, Variable A (Row 1) is a stream of data comprised of alternate 1's and 0's. Variable B (Row 2) is composed of alternate *groups* of *two* 1's and *two* 0's.

The remaining rows indicate the following:
Row 3: A and B combined in an AND gate. (C = AB reads "C equals A *and* B.")
Row 4: The complement of row 3 (NOT or NAND circuit).
Row 5: A and B combined in an OR gate. (D = A + B reads "D equals A *or* B.")
Row 6: The complement of row 5 (NOT or NOR circuit).

So here we have every combination fundamental to logic circuitry. If we understand the symbols for bistables and gate circuitry, we should know what to expect at the output of each chip for a given input or inputs. For example, we can quickly check inputs A and B to the AND gate. We must then determine the normal output as shown by Row 3. For a NAND circuit, we should have the inverted function of Row 4.

Again as a matter of review, bear in mind that the bistable is a natural divide-by-two circuit. If the first pulse results in logic 1, a second pulse is required to result in logic 0. So to complete one output pulse, two input pulses are required. For example, if Variable A (Row 1 in Fig. 15-13) is the input to a bistable, Variable B (Row 2) would be the output. This is to say that the frequency of B is half that of A.

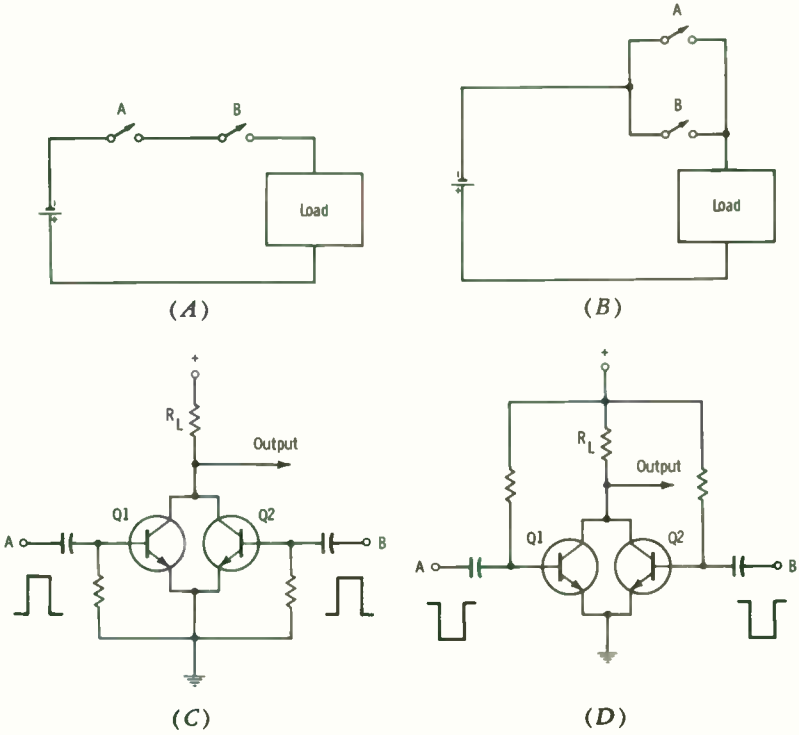
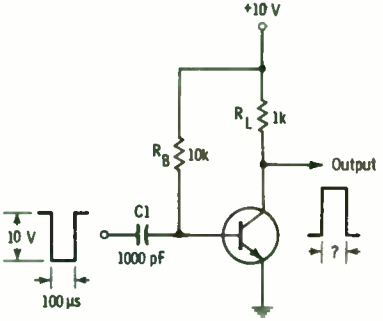
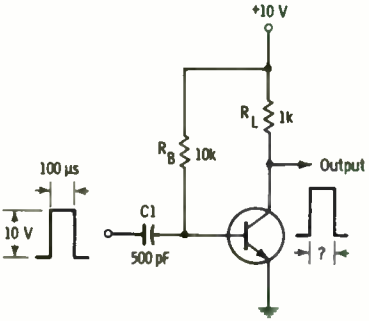


Fig. 15-14. Circuits for Q15-1, Q15-2, and Q15-3.



(A) *For Q15-4.*

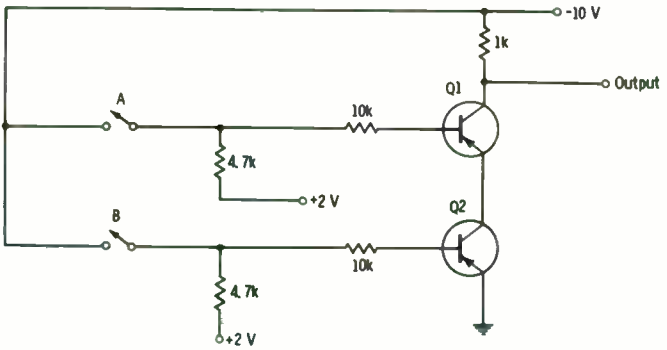


(B) *For Q15-5.*

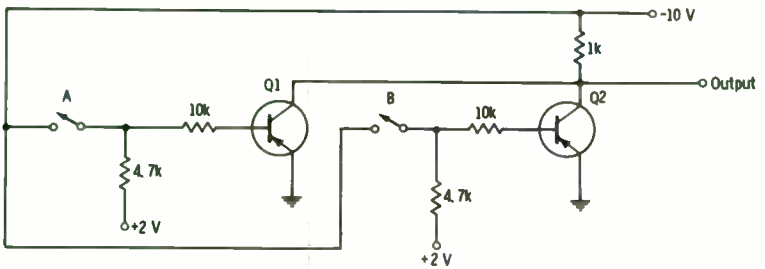
Fig. 15-15. Pulse circuits for exercises.

EXERCISES

Q15-1. What type of circuit does the series switch arrangement of Fig. 15-14A represent? What type does the parallel switch arrangement of Fig. 15-14B represent?



(A) *For Q15-6 and Q15-8.*



(B) *For Q15-7 and Q15-8.*

Fig. 15-16. Logic circuits for exercises.

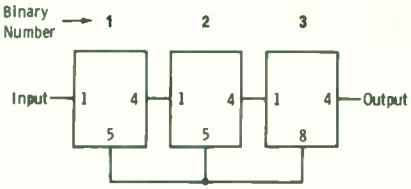


Fig. 15-17. Circuit for Q15-10.

Q15-2. See Fig. 15-14C. Does this circuit correspond to Fig. 15-14A or 15-14B?

Q15-3. See Fig. 15-14D. Does this circuit correspond to Fig. 15-14A or 15-14B?

Q15-4. See Fig. 15-15A. What is the approximate width of the output pulse? Does the leading edge of this output pulse occur at the same time as the leading edge of the input pulse?

Q15-5. See Fig. 15-15B. What is the width of the output pulse? Does the the leading edge of this output pulse occur coincident with the leading edge of the input pulse?

Q15-6. See Fig. 15-16A. What would you call this circuit for:
(A) Switches normally open?
(B) Switches normally closed?

Q15-7. See Fig. 15-16B. What would you call this circuit for:
(A) Switches normally open?
(B) Switches normally closed?

Q15-8. If the transistors of Fig. 15-16 where npn types instead of pnp, would the circuit functions change? (Assume the dc polarities were reversed.)

Q15-9. If you have a chain of three binaries with a pulse repetition rate of 240 pps at the input, what is the pulse repetition rate at the output? (Assume no feedback circuits are involved.)

Q15-10. What is the total division of the chain of three binaries in Fig. 15-17?

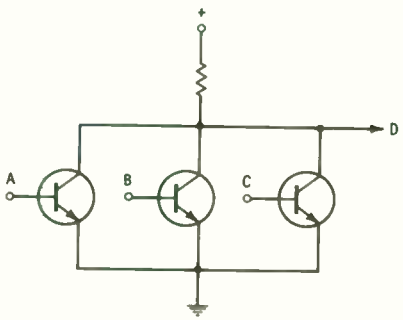


Fig. 15-18. Circuit for Q15-15.

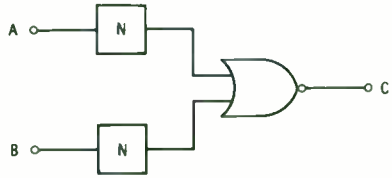


Fig. 15-19. Circuit for Q15-16.

Q15-11. Write the algebraic equation for output H of Fig. 15-11A in the form V = ?

Q15-12. Prepare the truth table for Circuit 1 (AND) of Fig. 15-11A.

Q15-13. Prepare the truth table for the OR portion of Circuit 2, Fig. 15-11A.

Q15-14. Prepare the truth table for the NOT portion of Fig. 15-11A.

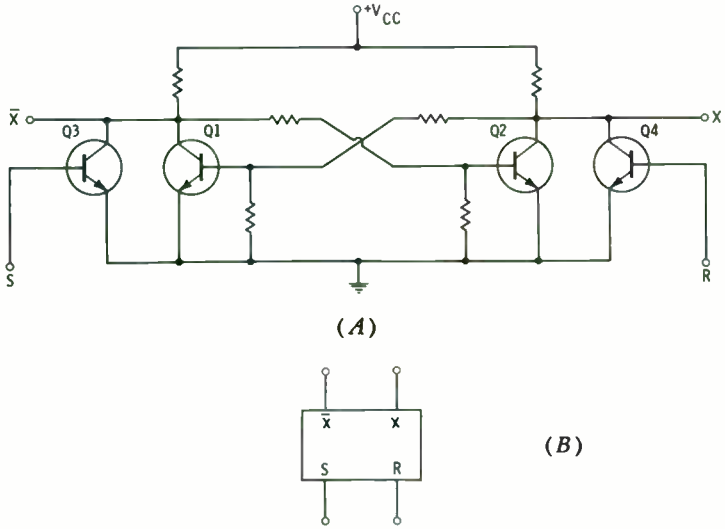


Fig. 15-20. Illustrations for Q15-17.

Q15-15. What does the simple circuit of Fig. 15-18 represent? Draw it as a symbol.

Q15-16. Prepare the truth table for Fig. 15-19.

Q15-17. See Figs. 15-20A and 15-20B. What do these illustrations represent?

Q15-18. Does a series of cascaded binaries always count to 2^n, where n is the number of binary circuits?

CHAPTER 16

Power Supplies

Most solid-state power supplies incorporate the zener diode (Chapter 2) for the purpose of providing a reference voltage to other controlling devices. It is pertinent, therefore, to be sure we understand the zener before proceding.

The zener diode is usually thought of in connection with regulated dc circuitry. It is just as useful in certain ac applications, and this fact provides some practice in using zener characteristics. For example, precision sine-wave oscillators of the vacuum-tube type employ regulated dc voltages for tube elements, and some form of filament-voltage regulation, either ac or dc. Before the zener diode was developed, elaborate rectifier-regulator circuits, saturable-core reactors, or ballast tubes were required for filament-voltage control.

16-1. AC APPLICATION OF ZENER DIODES

First, consider the known variables of a 6.3 volt, 300-mA filament. If the line voltage varies over a range of 100 to 130 volts (115 volts nominal), the corresponding filament-voltage variation would be approximately 5.4 to 7.1 volts. Assuming a linear current variation with voltage, the current range would be about 260 to 340 mA. The average variable-frequency oscillator, if calibrated at 115 line volts, will not maintain tolerable calibration at either extreme of line voltage unless the filaments are regulated.

The best tolerance we can get in a reasonably priced zener diode is 5 percent. If we were to employ a 6.3-volt zener, a tolerance at the high limit would run the filaments at 6.6 to 6.7 volts, needlessly reducing tube life. The matter of importance is the regulation, not absolute voltage. A 5.6-volt, 5-percent zener diode will work nicely for this application.

Since we must consider the regulating-diode current required, a 12.6-volt transformer should be used as in Fig. 16-1. Exact calculations for the circuit of Fig. 6-1 are difficult because the action of the zener diodes

makes the waveforms far from sine waves. We can, however, arrive at an approximate answer by using the following simplified method:

Step 1. For proper regulation, the zener current must be made at least 10 percent of the *minimum* load current. If we assume the minimum filament current is about 250 mA = 0.25 A, then 10 percent of this value is 25 mA = 0.025 A. Therefore, we must design the circuit so that, at minimum line voltage, the zener will draw 25 mA.

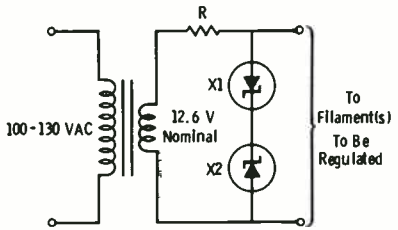


Fig. 16-1. Basic regulated filament supply.

Step 2. Find the minimum current through resistor R. This will be the zener current plus the filament current, or 0.025 + 0.25 = 0.275 A.

Step 3. Find the peak current through R. Let p = 0.6 and I_R = resistor current found in Step 2. Then the peak resistor current is:

$$\frac{I_R}{p} = \frac{0.275}{0.6} = 0.46\,A$$

Step 4. Find the minimum voltage on the 12.6-volt bus. This will be:

$$\frac{115}{12.6} = \frac{100}{x}$$

$$115x = 1260$$

$$x = 10.9 \text{ volts}$$

The above computation is used simply to determine the minimum secondary voltage (line voltage of 100 volts) if the secondary voltage is 12.6 volts at a line voltage of 115 volts. It says that 115 is to 12.6 as 100 is to the unknown voltage. Cross-multiplying, we get the result, 10.9 volts.

Step 5. Find the proper value for R. We have the following known values: The minimum secondary voltage will be 10.9 volts (this is rms, so the peak minimum voltage is 1.4 times this value); the peak resistor current is 0.46 ampere; and the zener diode we decided on was a 5.6-volt unit. So the value for R is:

$$R = \frac{V_{min}\,(1.4) - V_z}{I_{R\ peak}}$$

Substituting the known values in this formula:

$$R = \frac{10.9\,(1.4) - 5.6}{0.46}$$

$$= \frac{9.7}{0.46} = 21 \text{ ohms (20 ohms is close enough.)}$$

Step 6. Before deciding the wattage ratings for the zener diode and the resistor, we must first determine the zener current based upon the maximum (rms) zener current that occurs at maximum line voltage. Following the method of Step 4 and substituting the maximum line voltage (130 volts), we determine the corresponding secondary voltage to be 14.2 volts. Then the maximum zener current is:

$$\text{Max } I_z = \frac{V_{max}\,(1.4) - V_z}{R}(p)$$

Substituting the known values:

$$\text{Max } I_z = \frac{14.2\,(1.4) - 5.6}{20}(0.6)$$

$$= \frac{14.3}{20}(0.6) = 0.43 \text{ A}$$

Step 7. To find the power dissipated in the zener diode:

$$P_z = \frac{(V_z)\,(I_{z\,max})}{2}$$

(Since two diodes are used, each dissipates half the total power, hence the division by two.)

$$P_z = \frac{(5.6)\,(0.43)}{2} = \frac{2.4}{2} = 1.2 \text{ watts}$$

The next larger size is a 3.5-watt zener diode.

Step 8. To determine the wattage rating of R:

$$P_R = R\,(I_{z\,max} + I_{L\,min})^2$$

where,

$I_{L\,min}$ is the minimum load current.

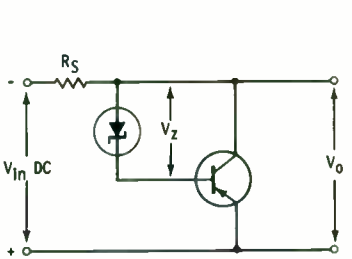
Remember that as the load current varies, the zener current also varies. Substituting:

$$P_R = 20(0.43 + 0.25)^2 = 20(0.68)^2 = 20(0.46) = 9 \text{ watts}$$

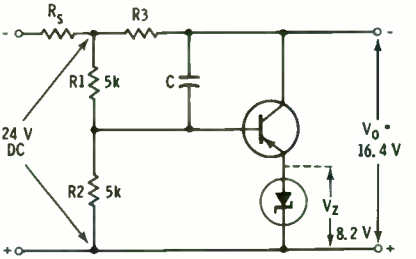
So R should be a 20-ohm, 20-watt resistor. (We double the actual dissipation value to allow adequate cooling of the resistor.)

16-2. FUNDAMENTALS OF REGULATED DC SUPPLIES

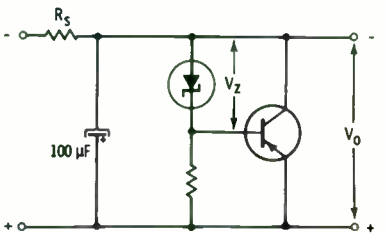
When a zener diode is used to control the operating bias of a transistor, voltage-control capability is considerably increased. See Fig. 16-2A. In this shunt regulator circuit, only the very small transistor base current passes through the zener. The regulation factor is improved by the current gain (beta) of the transistor. Thus if the transistor is controlled at a current gain of 10, a 1-watt zener can control a 10-watt load.



(*A*) *Basic shunt regulator circuit.*



(*B*) *Zener in emitter circuit.*



(*C*) *Zener in base circuit.*

Fig. 16-2. Fundamentals of shunt regulators.

See Fig. 16-2B. In this circuit, V_o depends on R1, R2, and the zener voltage:

$$V_o = \frac{R1 + R2}{R2} V_z$$

Thus when R1 equals R2 as in the schematic, we have $V_o = 2V_z$, or 16.4 volts in the example shown.

In the circuit of Fig. 16-2C, note that the collector-emitter voltage is effectively regulated by the zener diode. If this zener is a 10-volt regulator and the transistor is silicon, $V_o = 10 + 0.6 = 10.6$ volts, approximately.

A basic series regulator is shown in Fig. 16-3. The transistor (or a number in parallel, depending upon required power dissipation) absorbs voltage variations in series with the load. Since V_{in} is applied through R_s and a zener diode to the transistor base, a reference bias voltage is

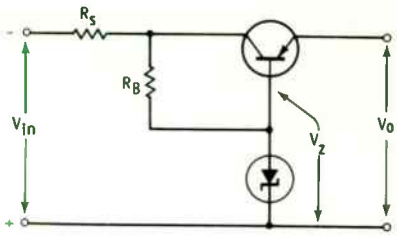
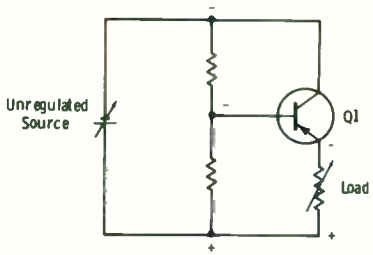


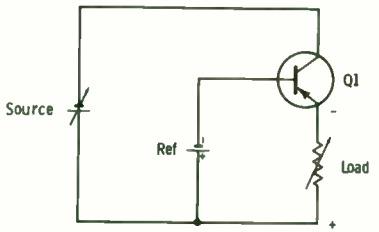
Fig. 16-3. Basic series regulator circuit.

established relative to the positive terminal. The transistor then functions as an emitter follower. Thus the emitter voltage is held within 0.2 to 0.7 volt (germanium or silicon) of the base reference voltage established by the zener diode.

The circuit shown in Fig. 16-4A will be recognized as a common version of the basic emitter-follower (or common-collector) circuit. The power-supply load (symbolized by a variable resistance) is placed in series with a transistor whose impedance is automatically controlled in such a way that it tends to compensate for the impedance changes (or current changes) in the load, thus maintaining an essentially constant voltage across the load. The voltage drop across the emitter-base junction of a transistor is negligible in comparison with the supply voltage (at least over reasonable operating ranges), so the emitter tends to remain near the potential



(A) Stabilized against variations in the load only.



(B) Stabilized against load and source variations.

(C) Amplified correction for further stabilization.

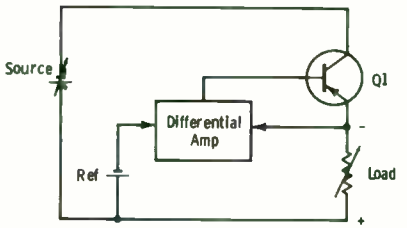


Fig. 16-4. Stobilization of load voltage.

established by the voltage divider in the base circuit. Since the base current is only a small fraction of the emitter (or load) current, the base voltage is not significantly altered by changes in load current, provided the resistors in the voltage divider are not too large. An alternative approach to the explanation of the regulating action is to show that the output impedance of an emitter follower is inherently low, and it approaches the impedance of an emitter-base junction alone as the base impedance decreases to zero. The output impedance never decreases to zero, however, so the regulation never becomes perfect with this simple circuit.

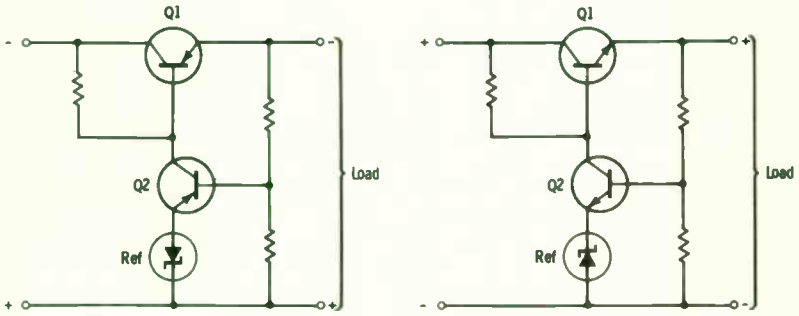
A regulating transistor of the pnp type is more conveniently placed in series with the *negative* side of the load, rather than the *positive* side, as would be the case with most vacuum-tube regulators. The transistor itself, or the required number placed in parallel, must be capable of handling the maximum load current. In practical transistor power supplies, it is necessary to mount the large series regulators on radiators or other types of heat sinks to keep the temperatures of the transistor junctions within safe limits.

While the simple circuit in Fig. 16-4A is reasonably effective in stabilizing the output voltage against load variations, it does not remove variations due to voltage changes in the unregulated source. This is because the voltage at the base of the transistor is changed in proportion to the unregulated voltage. The circuit in Fig. 16-4B overcomes this problem through the use of a separate, stabilized reference voltage source at the base. Although a battery symbol is shown, the reference-voltage source in a practical circuit could be a zener diode as in Fig. 16-3. Reference diodes are preferable to gaseous voltage-regulator tubes for transistorized power supplies, because they operate at lower voltages (usually on the order of 5 to 6 volts on up to 100 volts or more) and because they are generally superior to their tube counterparts with respect to stability and inherent regulation.

The degree of regulation attainable with the circuit in Fig. 16-4B is determined by the emitter-base impedance of the transistor itself, which might be on the order of a few ohms. Even better stabilization (or lower output impedance) can be provided by the use of additional gain in the control circuit to supplement the gain of the regulating transistor itself. Such an approach is illustrated in simplified form in Fig. 16-4C. The voltage across the load may be compared with a stabilized reference voltage in a differential amplifier, which can be designed with enough gain to make the voltage variation at the load as small as required.

A differential amplifier takes a sample of the output voltage, compares it with a reference voltage, and produces a signal that is proportional to the difference. See Fig. 16-5A for a negative supply (common plus) and Fig. 16-5B for a positive supply (common minus). Note the required types of transistors in each application for the necessary bias conditions.

First analyze Fig. 16-5A. Note that Q1 is in the same part of the circuit as in Fig. 16-4. A sample of the output voltage is applied to the Q2 base. If the output voltage tries to increase, the Q2 base goes more negative and increases the Q2 collector current. The emitter is held at the zener-diode reference voltage even though there is more current in the circuit. Thus the "difference voltage" is amplified by Q2. If the output voltage tends to drop (less negative, or more positive), the Q2 collector current decreases. The change in Q2 collector current and the change in input current to series control element Q1 are out of phase. This means that as the output voltage begins to rise, the amplified difference voltage *decreases* the current into the series control element, correcting the output voltage.



(A) Negative supply. *(B) Positive supply.*

Fig. 16-5. Differential amplification in regulators.

The circuit of Fig. 16-5B operates in the same way except that the series regulator is an npn type, since it is in the positive supply lead.

All transistor regulated power supplies operate on these general principles. The number of transistors (and diodes) depends upon how many different voltages (and voltage polarities) are provided. In high-voltage supplies, series regulators may be compounded with several in series (to withstand the difference in voltage between unregulated and regulated sections) and others in parallel (to provide sufficient current without exceeding individual transistor power ratings).

The most important addition with which we should be familiar is the manner in which transistor power supplies are protected against short circuits. Ordinary fuse-type protection is generally not fast enough to protect transistors, so we will nearly always encounter special circuitry included to provide this protection.

See Fig. 16-6. The added protection circuitry is enclosed in dash lines. The value of R_B is chosen so that during normal regulator operation Q3 is saturated. This places negligible resistance in series with the negative return. Potentiometer R_E is adjusted so that it produces sufficient voltage

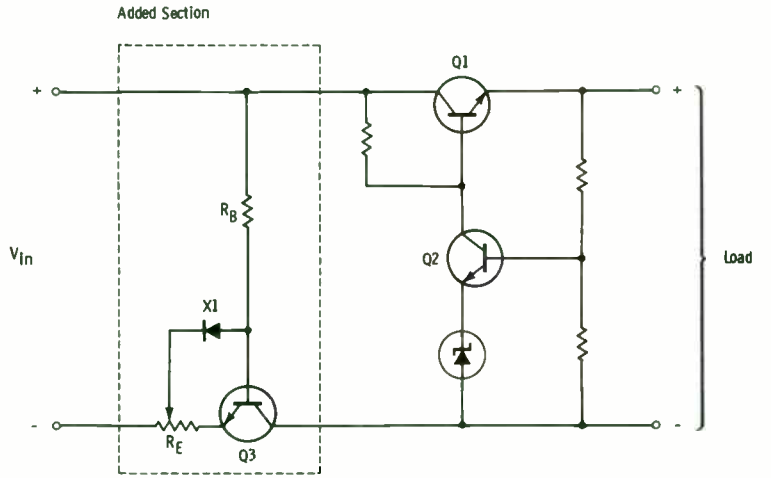


Fig. 16-6. Regulator with added protection circuit.

drop to cause X1 to conduct if the load should develop a short or a specific value of overload (low resistance, excessive current). Conduction of X1 reduces the bias on Q3 so that it appears as an increasing series resistance in the regulator circuit.

EXERCISES

Q16-1. What is the required ratio of minimum zener current (I_z) to load current for good regulation?

Q16-2. What is the actual power dissipation of a 10-volt zener diode with a regulating current through it of 100 mA?

Q16-3. What is the maximum permissible current for a 10-volt zener diode of 0.5-watt power rating?

Q16-4. In the circuit of Fig. 16-3, if the collector voltage is 24 volts and $V_o = 12$ volts at 100 mA, what is the transistor power dissipation?

Q16-5. In Fig. 16-6, if X1 should open, will normal operation of the power supply be affected?

CHAPTER 17

Basic Testing and Servicing Techniques

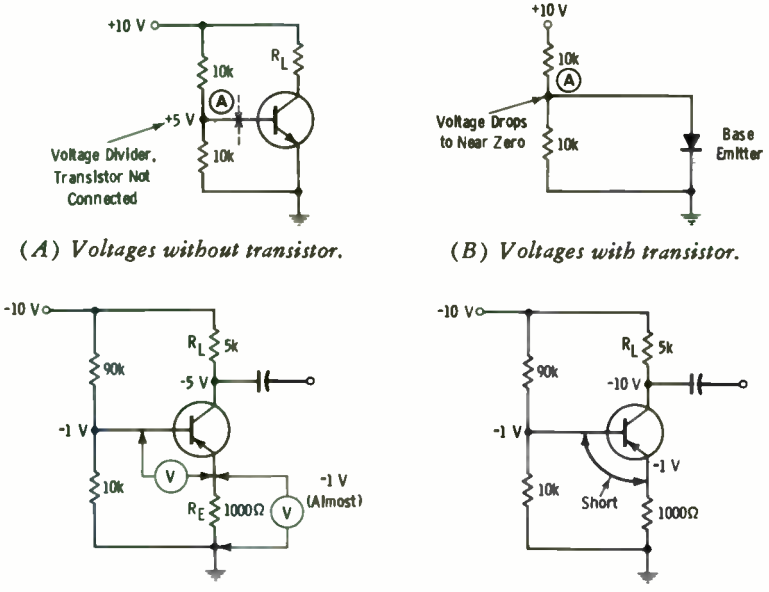
With a good grasp of the fundamentals covered in previous chapters, we can go a long way in testing and servicing solid-state circuitry. Specific testing and servicing techniques have been covered in some instances in previous chapters, as follows: diodes and rectifiers, including SCRs and zeners, Chapter 2; transistor testing techniques, Chapter 7; the Schmitt trigger, Chapter 12; and logic systems, Chapter 15.

17-1. BASIC IN-CIRCUIT TESTING

Figs. 17-1A and 17-1B show a basic principle of the transistor. The two equal base-bias resistors form a voltage divider, so we would expect 5 volts relative to ground at point A *if the transistor is not connected.* But the emitter goes directly to ground, so only about 0.2 volt (for germanium) or 0.6 volt (for silicon) will exist at the base when the transistor is connected into the circuit. So the voltage at the base will be near ground potential, unless an external emitter resistor is used. If the emitter-base junction is good, we will measure the standard 0.2 to 0.6-volt drop across the junction. The junction can be either open or shorted. If it is shorted, the voltage is zero. If it is open, we will measure about +5 volts from base to ground (in this particular circuit).

Here is a good place to emphasize an important point. In transistor circuits, we are almost always involved in reading *very low* voltages. These voltages are often across high values of resistance. Therefore, we should use a high-impedance voltmeter for transistor-circuit tests. Use either a 20,000-ohms/volt meter or (preferably) a VTVM.

Study now Fig. 17-1C. Using Ohm's law on the base bias-supply circuit, we expect −1 volt at the base. We know the emitter will be within 0.2



(A) Voltages without transistor. *(B) Voltages with transistor.*

(C) Voltages in a CE stage. *(D) Use of short for test.*

Fig. 17-1. Fundamentals of in-circuit testing.

to 0.6 volt of the base; for quick computation we assume the current through R_E causes a 1-volt drop:

$$I_E = \frac{V}{R_E} = \frac{1}{1000} = 1\text{ mA}$$

Again for quick computation, we assume the same current in the collector as in the emitter:

$$IR_L = (0.001)(5000) = 5\text{ volts}$$

So a 5-volt drop from −10 volts leaves −5 volts at the collector. For linear amplifier operation, the collector will always be somewhere in the vicinity of one-half the supply voltage, usually within a few volts.

When we have isolated the faulty stage by scope tracing (which is the most reliable method for any video or audio application), voltage checks should be made. We find many circuit schematics and instruction books for equipment that give no indication of any kind as to normal voltages to expect. So practice the analytical procedure outlined in previous chapters until voltage charts are not needed.

After the first voltmeter checks to ground for any obviously missing voltages, measure the voltage difference between base and emitter. Unlike the vacuum tube, the transistor must have a forward bias to conduct at

all. In the npn transistor, the base must measure 0.2 to 0.6 volt positive relative to the emitter. For the pnp transistor, the base must measure 0.2 to 0.6 volt negative relative to the emitter. In the circuit of Fig. 17-1C with −1 volt base to ground, the emitter-to-ground voltage will be approximately −0.8 to −0.4 volt.

This discussion leads quite logically to the very informative test of Fig. 17-1D. If we short the base and emitter leads together with a jumper, the transistor should cut off. With no collector current, we should measure the full supply voltage at the collector. With excessive leakage current, the transistor will not cut off, and the point of operation has slipped upward on the load line to cause compression of whites or blacks (video) or amplitude clipping (audio). Note that the only voltage that changes significantly with this test is the collector voltage.

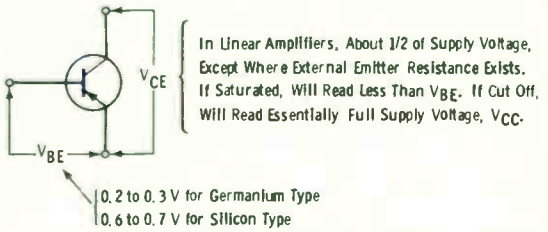


Fig. 17-2. In-circuit voltage tests.

In-circuit voltage checks of a transistor are summarized in Fig. 17-2. For the collector, we know that good design practice (linear amplification) generally results in a collector-to-common voltage of about one-half the supply voltage. Of course if the emitter is grounded, the same is true for the collector-to-emitter voltage. If an external emitter resistor is used, a voltage difference results. For example, if the emitter is plus 0.5 volt and the collector is plus 8 volts (to common), then V_{CE} will be $8 - 0.5 = 7.5$ volts.

Obviously, if the transistor is cut off—either from design or because of faulty junctions—we will measure the entire supply voltage for V_{CE}. If the transistor is saturated, remember that V_{CE} will be *less* than V_{BE}. (This phenomenon was covered in Section 8-2.)

Voltage V_{BE} determines the junction current when the transistor is forward biased. The higher this forward bias, the greater the emitter (hence collector) current will be. The voltage difference from base to emitter will be very close to 0.2 or 0.3 volt for germanium, or 0.6 to 0.7 volt for silicon. When the base-emitter junction is *reverse biased*, V_{BE} must never exceed the maximum V_{BE} rating for the particular transistor.

Now look at Fig. 17-3; this is an actual circuit in a commercial video amplifier. The student should be able to tell at a glance the approximate voltage gain of Q1. If we ignore Q2, the voltage gain of the first stage

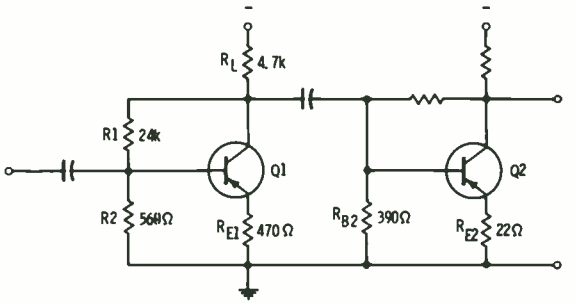


Fig. 17-3. Practical video circuit.

would be approximately $4700/470 = 10$. But the value of R_{B2} tells us the effective R_L of Q1 is less than 390 ohms. Since the value of R_{E1} is 470 ohms, we know quickly that Q1 will have a voltage gain of *less* than unity (390/470 = less than 1).

The actual input impedance of Q2 (load on Q1 collector) is (assuming nominal beta of 50): $Z_{in} = (50)(22) = 1100$ ohms. Then 390 ohms in parallel with 1100 ohms is 290 ohms (approximately). So now:

$$A_v = \frac{\text{Effective } R_L}{R_{E1}} = \frac{290}{470} = 0.6 \text{ (approx)}$$

So if we have a 1-volt peak-to-peak signal at the Q1 base, we have about the same signal at the Q1 emitter. At the collector, we would expect $(0.6)(1) = 0.6$ volt peak to peak.

17-2. TRANSISTOR REPLACEMENT

When it is necessary to replace a transistor, we must observe special rules. When unsoldering a transistor lead (most transistors are soldered into the circuit), we *must* use a heat sink on the lead itself, between the transistor case and the point where heat is applied. This heat sink can be thin-nose pliers held on the lead with one hand while the other hand is used to apply the iron. (This is good practice even though we know the transistor is defunct. Never get out of the habit!) We *must* use the same procedure in installing the new transistor. More convenient is a special transistor heat sink (which can be purchased from parts suppliers) that clamps onto the lead to free both hands for working. Or we can use an ordinary alligator clamp on the lead while soldering. If this is done, fill the clip wire receptacle with solder to increase its heat-dissipating capability. Use a 25- to 40-watt soldering iron, preferably dc; ac can damage some tiny transistors.

For in-circuit scope signal tracing, we should be able to correlate previous material on circuit analysis, and estimate quite closely how much gain should result in any circuit. If gain is obviously low, voltage checks

are next in order. If these seem reasonable and it appears all is normal in biasing, the transistor is probably faulty.

17-3. TRANSISTOR SUBSTITUTION

Quite a few transistor substitution publications are available on the market. These are quite worthwhile, but additional information other than a listing of direct substitutions is often more useful. A listing of specifications for given transistor types is the most informative type of reference.

The important things to know about any transistor, both for practice in circuit analysis and for practical application, are the *maximum* ratings of the following:

P_c = Collector power dissipation. It is necessary to know whether this is rated for ambient air (T_a) or actual case temperature (T_c), which normally means a heat sink is required.
I_c = Maximum collector current.
V_{CE} = Maximum collector-to-emitter voltage.
V_{CB} = Maximum collector-to-base voltage.
V_{EB} = Maximum emitter-to-base voltage.

In addition it is important to know the following ratings, which are always "average" or "design center," and subject to some variation in practice:

h_{fe} or h_{FE} = Common-emitter short-circuit forward current transfer ratio. You should also know at what I_c this rating was determined.
f_{hfb} = Alpha cutoff frequency or f_{hfe} = Beta cutoff frequency, or gain-bandwidth product.

Also important, of course, is the designation as to whether the transistor is an npn or a pnp type, and whether the structure is germanium or silicon. The type of mounting is also useful information, and this is usually listed.

As to "substitution," it is, of course, ideal to replace a transistor with one of the same type as that removed. In practice, because of the many, many types of transistors involved in even a small broadcast station, we may inadvertantly "run out of" a particular type. If this happens, the author has found the following to work in an emergency in every case tried thus far:

We can use a 2N404 (pnp) or a 2N585 (npn) for emergency replacement of any low-frequency germanium transistor. For any high-frequency germanium transistor (as in video amplifiers), use the 2N1306 (npn) or 2N1307 (pnp). If you should happen to use the above types in your installation, keep a few extra units on hand for this purpose. *The important thing is to double check the P_c and maximum I_c ratings.* For this purpose, Table 17-1 is included for the types mentioned. Note that the

Table 17-1. Transistor Maximum Ratings

Type	Number	I_c (Amps)	V_{CE}	V_{CB}	V_{EB}	P_C (Watts), T_a	Use
pnp	2N404	0.1	−24	−25	12	0.12	Low Frequency
npn	2N585	0.2	15	25	20	0.12	Low Frequency
npn	2N1306	0.3	15	25	25	0.15	High Frequency
pnp	2N1307	0.3	−15	−30	25	0.15	High Frequency
pnp	2N1143	0.1	−25	−35	30	0.75	High Frequency

2N1143 (pnp) also is included because of its extreme popularity in modern video circuitry. You obviously cannot substitute a pnp transistor for an npn transistor, or vice-versa.

For silicon transistors (general-purpose, low- or high-frequency applications), the 2N2905 (pnp) or 2N2219 (npn) often may be used for emergency replacement.

Just as is the case with vacuum tubes, the best way to determine whether a transistor should be replaced is to replace it. But, unlike tubes, transistors are often soldered into the circuit. Sometimes the disturbance caused by removing a transistor will temporarily "heal" an intermittent capacitor connected to the same point. It is certainly desirable to have some kind of indication to confirm that a transistor is bad even though it checks satisfactorily with the VOM (Chapter 7).

There are many "transistor checkers" on the market, but all have many limitations, unless we purchase rather expensive equipment. In addition, larger power transistors can exhibit troubles only under dynamic operating conditions. (This is also true of smaller transistors, but to a lesser degree.) So if we could devise a means of looking at the dynamic operating characteristic at or near the maximum rating of the transistor, we would have a very useful device.

You can prove to yourself the usefulness of such a tester by constructing the simple circuit of Fig. 17-4A breadboard fashion. A pnp test is shown; for an npn transistor, the polarities of the rectifier and the base battery would be reversed. With the 6.3-volt transformer winding, the collector "sweep" is from zero to about −9 volts peak. The collector *current* is sampled by the resistor in the collector lead and a signal fed to the vertical amplifier of the scope. The collector sweep *voltage* applied to the horizontal input of the scope deflects the trace horizontally; the sweep can, of course, be calibrated in peak volts per centimeter.

As you increase the base current, traces similar to Fig. 17-4B should result. Of course, you will get only one trace at a time. If you use the dc input of the vertical scope amplifier, the starting point of the transfer curve will remain at one spot for convenience. If you get a clean transfer curve at operating currents somewhat under the maximum ratings (for safety, since circuitry normally prevents operation at the top ratings),

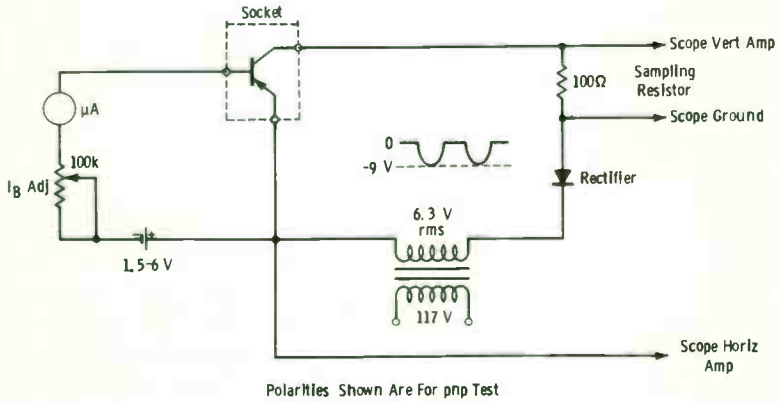
you can be reasonably sure the transistor is good. Fig. 17-4C shows what to expect for traces from faulty transistors.

Such a test will reveal 99 percent of transistors that can cause trouble. High-frequency response is not revealed by this test, but when the problem is only one of a rolloff in frequency response, the first thing to do is change the transistor. If frequency response returns to normal, there is no purpose in saving the transistor for further tests.

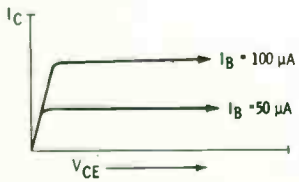
17-4. THE "WORKSHOP" CURVE TRACER

Even if you do not intend to construct the curve tracer described in this section, be sure to study this material, since the techniques described will broaden your familiarity with the practical application of transistors.

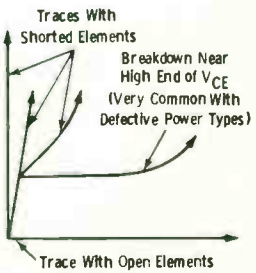
The simple circuit of Fig. 17-4A can be expanded almost without limit to result in greater flexibility and broader applications. The basic additions to be desired are pnp-npn polarity switches, adjustable ranges of



(A) Circuit diagram.



(B) Normal traces.



(C) Abnormal traces.

Fig. 17-4. Simple transistor checker.

collector sweep and base currents to cover all transistors from the tiny ones to power types drawing up to 10 amperes of collector current, and a means of quickly selecting values of sampling resistors so that the vertical deflection can be calibrated in milliamperes or amperes per centimeter.

Construction of such a circuit (Fig. 17-5) will serve two basic purposes: (1.) a fundamental education in correlation of collector current with voltage and base bias current, and (2.) as good a transistor tester as you can have unless you invest many times the cost of this device. (Naturally, its cost will depend on the number of parts you may already have on hand—see parts list on page 332.)

Details of the current-range selector for the particular meter used (basic 200 μA movement) are shown in Fig. 17-6. Naturally, if you use a different meter with different internal resistance, you will need to use the relationship:

$$R_s = \frac{R_m}{n-1}$$

where,

R_s is the required shunt resistance,
R_m is the resistance of the meter movement, and
n is the multiplication factor.

For example, assume the meter has an internal resistance of 1000 ohms. The first shunt takes the 200-μA meter range to 2mA, so n is 10 times:

$$R_s = \frac{1000}{10-1} = \frac{1000}{9} = 111 \text{ ohms for the 2-mA range}$$

All of the 1-percent resistors in the meter current-range selector and the sensitivity (sampling-resistor) circuits are made by the Dalohm Corporation, but you can use any available make provided you observe the required wattage shown for the sensitivity section. All the resistors in the current-range selector are of one-half-watt rating.

Note that the SENSITIVITY switch enables you to select the proper sensitivity of scope deflection in milliamperes per volt. For example, see Fig. 17-7. If the switch is set on 10 mA/volt (100-ohm resistor) and the scope trace at the upper extreme of the collector voltage (5.6 volts in this example) measures 1 volt vertically, we know the collector current is 10 mA at the particular base bias current indicated by the I_B meter.

The transformer for the collector sweep should provide about three voltages as shown; the exact values are not critical since you should feed this transformer from a variable autotransformer to obtain any desired peak swing of the collector-to-emitter voltage. Please note that the 4-volt tap is marked "5.6" at the switch selector position; this is peak value for 4 volts rms. So the peak values available in this instance are 5.6, 22.4 and 34 volts when the primary voltage is 117 volts. The transformer should

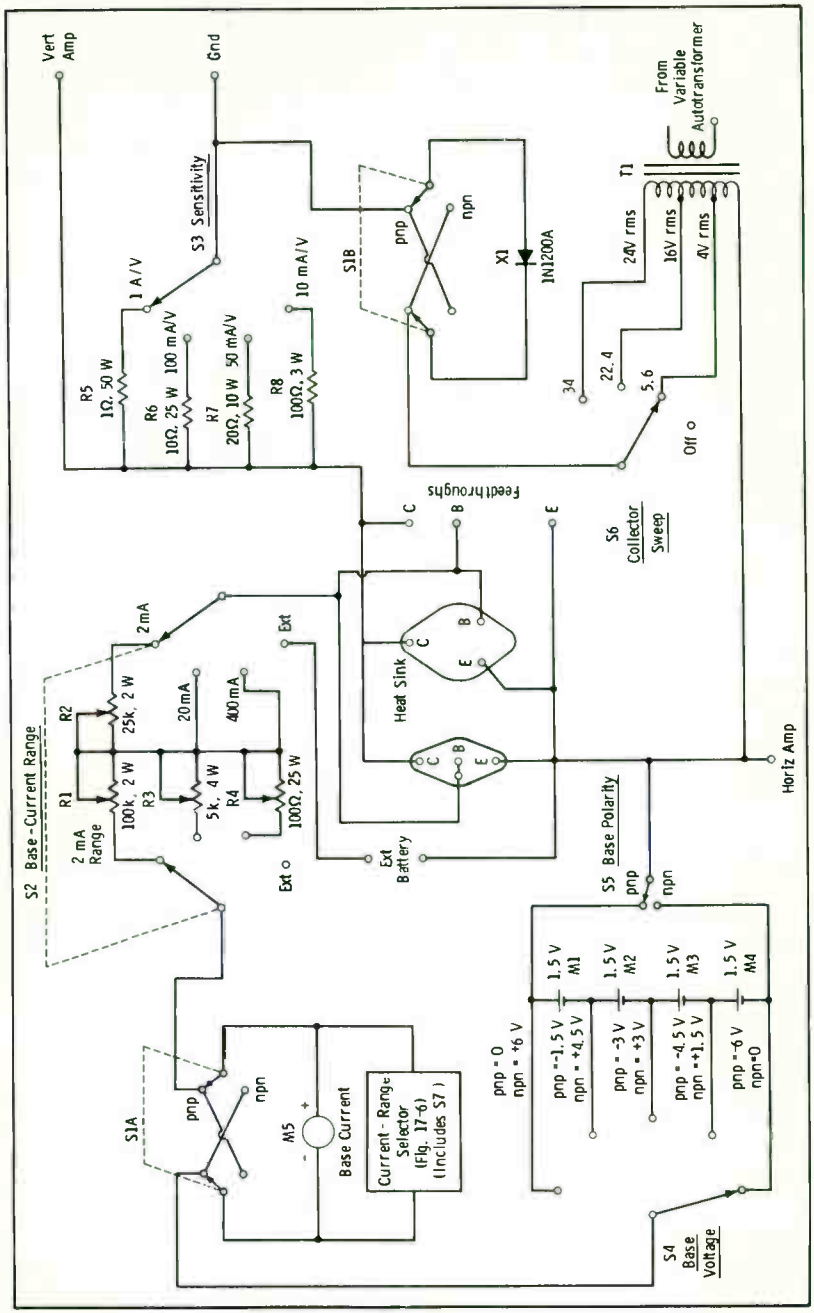


Fig. 17-5. Circuit of transistor-curve tracer.

Electrical Parts List for Transistor Curve Tracer

Switches

S1	4PDT, 12-Terminal (J-B-T MS 25068-23)
S2	4-Position, 2-Gang (Grayhill 24002-4)
S3, S6	4-Position (Grayhill 19001-4)
S4, S7	5-Position (Grayhill 24001-5)
S5	SPDT (Arrow-Hart & Hegeman 21350-EH)

Resistors

R1	100k, 2W (Ohmite cu-1041)
R2	25k, 2W (Ohmite cu-2631)
R3	5k, 4W (IRC WP-5000)
R4	100 ohm, 25W (Ohmite H-0151)
R5	1 ohm, 50W, 1% (Dalohm Type RH-50)
R6	10 ohm, 25W, 1% (Dalohm Type RS-25)
R7	20 ohm, 10W, 1% (Dalohm Type RS-10)
R8	100 ohm, 3W, 1% (Dalohm Type RS-2)
R9	110 ohm, ½W, 1%
R10, R13	1 ohm, ½W, 1%
R11	10 ohm, ½W, 1%
R12	0.1 ohm, ½W, 1%
R14	0.5 ohm, ½W, 1%

Miscellaneous

T1	Thordarson-Meissner 23V42
X1	1N1200A
M1, M2, M3, M4	RCA VS 1335
M5	Simpson No. 29 Panel Meter (4½"), 0-200μA DC

Mechanical parts: Transistor sockets, battery holder, binding posts, feed-throughs, chassis, miscellaneous parts and hardware.

NOTE: Use parts specified, or their equivalents.

be capable of supplying 10 amperes at the maximum-voltage tap for testing power-type transistors.

Just two transistor sockets are shown: one "combination" type for the "triangle" and the "in-line" transistors, and a power socket on a heat

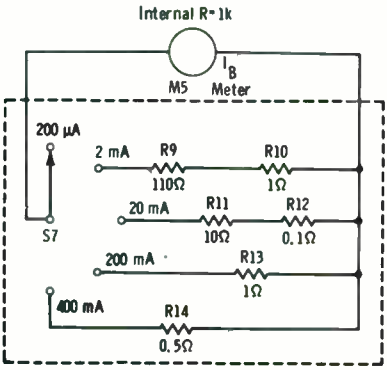


Fig. 17-6. Diagram of current-range selector.

sink. Also included are feedthroughs for jumpering to any type of transistor, as well as to provide a convenient place to hook up a VTVM.

To provide extreme flexibility in base voltage-current adjustments, the tapped-battery arrangement is used, as well as a separate battery-polarity switch to allow reverse-biasing if desired. Since up to 0.4 ampere is supplied by the base bias batteries, manganese alkaline batteries (RCA type VS 1335 or equivalent) are required.

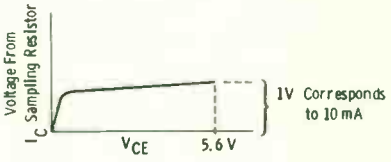


Fig. 17-7. Sensitivity of curve tracer.

Also handy are the extra binding posts for the "External" position of the I_B RANGE switch, which allows you to use an external meter and adjustable voltage source for transistors that require extra heavy base current.

Now let us go through a typical application of the curve tracer. Characteristic curves for three representative types of transistors are given in Figs. 17-8, 17-9, and 17-10 simply as a guide for this discussion; they are not needed in using the curve tracer, as we will see later.

Take first the type 2N404, which is the work horse in low-frequency transistor circuits, as the type 12AT7 is in vacuum-tube applications. There are just three things we need to know for a test: maximum collector power (P_c), maximum collector current (I_c), and whether the transistor is pnp or npn. We can find these readily in any manufacturer's specification listings. For the 2N404 (pnp) we find maximum ratings as follows:

$$P_c = 120 \text{ mW}$$
$$I_c = 100 \text{ mA}$$

It is desirable to test the transistor near the maximum ratings; a 4/5 rule provides the necessary safety factor, so:

$$4/5 \text{ of } P_c = 4/5 \text{ of } 120 \text{ mW} = 96 \text{ mW}$$
$$4/5 \text{ of } I_c = 4/5 \text{ of } 100 \text{ mA} = 80 \text{ mA}$$
$$\text{Maximum } V_{CE} \text{ for } 80 \text{ mA} = \frac{P}{I} = \frac{0.096}{0.080} = 1.2 \text{ volts}$$

So we will want a collector-emitter voltage of no more than 1.2 volts. We will want to adjust the base current to get 80 mA of collector current. Essentially, that's all there is to it. If we get a "clean" curve with no breakaway, the 2N404 is very likely in excellent shape.

Here is the way you assure a V_{CE} of 1.2 volts. Set the COLLECTOR SWEEP switch to the 5.6-volt position. Have a VTVM attached to the collector and emitter feedthrough terminals. Since the collector current will be about 80 mA, set the SENSITIVITY switch to the 50 mA/V position. As you bring up the base current, adjust the autotransformer to obtain 1.2 volts (on the peak-to-peak scale) on the VTVM when you reach a collector current of 80 mA. Since the sensitivity is 50 mA/V, 80 mA is reached when the scope shows $80/50 = 1.6$ volts of vertical deflection at the end of the horizontal trace. You would, of course, first calibrate the scope for 1.6 volts in some convenient number of centimeters on the graticule.

If we have the curves available as in Fig. 17-8, we can go much further in comparison just for the sake of a thorough analysis. We can reduce V_{CE} to 0.7 volt peak as shown on the curves, and compare the traces at given values of I_B to see if they fall within the minimum and maximum tolerances. We can also, of course, determine the dc beta, since:

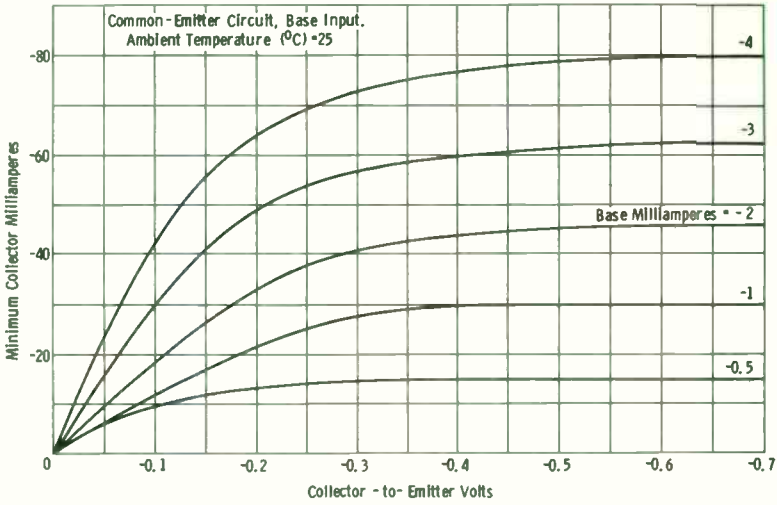
$$h_{FE} = \frac{I_C}{I_B}$$

It may not be clear why the peak-to-peak scale of the VTVM should be read to get the peak V_{CE} indication. Remember that a half-wave rectifier is being used, and, since a half-cycle of the waveform is missing, 1.2 volts is actually the peak-to-peak amplitude of the waveform.

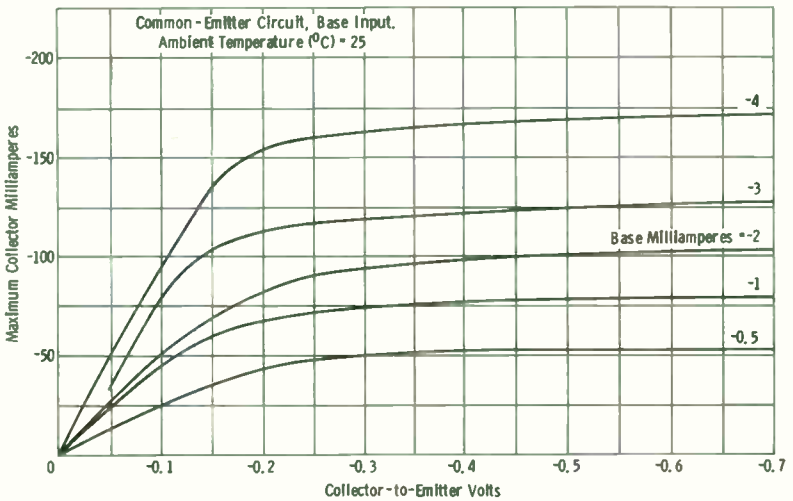
Caution: If you have been thinking this discussion through, you have already been alerted to what could happen if you were simply tracing the curves of Fig. 17-8 without remembering P_c. Suppose you have a transistor that produces the "maximum" trace. At 0.7 volt for V_{CE}, if you use 4 mA of base current, you can get a collector current of about 170 mA. You have exceeded the recommended safety factor, and P_c is at the maximum of 120 mW. If you leave the test on too long without sufficient derating for heat, or without forced cooling, you can damage a good transistor. *It is good practice to install "clip-on" heat sinks on all small transistors while testing them.* For power transistors, always use the large heat sink provided. Your parts supplier can recommend the types of heat sinks available to him.

Remember that the most important part of this test is the shape of the trace revealed at a safety margin normally provided in the circuits in which the transistor is used.

Now let us see how we would handle a smaller transistor such as a 2N384. (From Fig. 17-9, you can see that you would want around −16 volts for V_{CE}, so set the COLLECTOR SWEEP on the 22.5-volt tap and adjust the variable autotransformer for −16 volts (peak-to-peak scale) on the VTVM. Adjust I_B to the proper value and set the SENSITIVITY switch to the 10 mA/V range. (We are expecting I_C somewhere around 2 to 3 mA.) At 2 mA we have 2/10, or 0.2 volt, of vertical deflection.



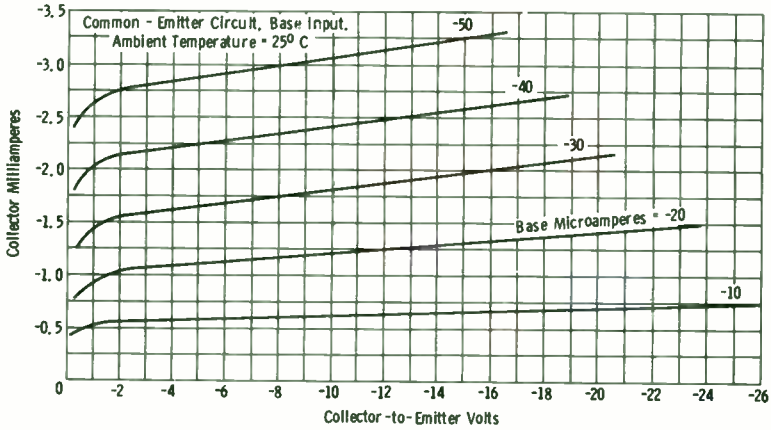
(A) Minimum collector characteristics.



(B) Maximum collector characteristics.

Courtesy RCA Corp.

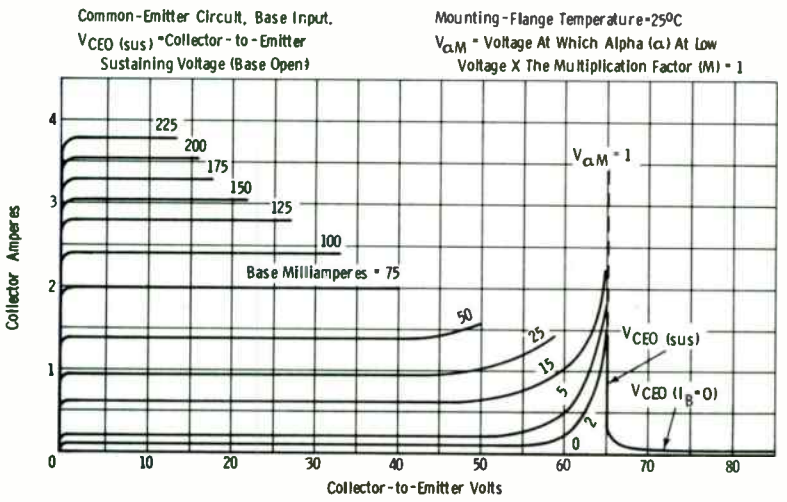
Fig. 17-8. Characteristic curves for type 2N404.



Courtesy RCA Corp.

Fig. 17-9. Characteristic curves for type 2N384.

The above two examples have covered transistor types with a low V_{CE} at medium I_c (2N404), and a medium V_{CE} at low I_c (2N384). Now for an example of a power-type transistor (such as the 2N1487), see Fig. 17-10. This is an npn transistor. You will find this type of transistor has a high-V_{CE}, high-I_c characteristic. Note that on such a curve, as I_c increases, the V_{CE} must be decreased to limit P_c; consequently, the maximum I_B curves (high I_c) are considerably shortened horizontally.



Courtesy RCA Corp.

Fig. 17-10. Characteristic curves for type 2N1487.

Let us emphasize that you do not need the transfer curves at all. Take the popular type 2N1022A power transistor with the following ratings:

$$\text{Max } P_c \text{ (at case temperature of 25°C)} = 150 \text{ watts}$$
$$\text{Max } I_c = 7 \text{ amperes}$$

Then:

$$4/5 \text{ of } P_c = 4/5 \text{ of } 150 \text{ watts} = 120 \text{ watts}$$

and:

$$4/5 \text{ of } I_c = 4/5 \text{ of } 7 \text{ amperes} = 5 \text{ amperes (approx)}$$

Max V_{CE} for 5 amperes of I_c is:

$$P/I = 120/5 = 24 \text{ volts}$$

The test procedure would be as follows:

1. Set COLLECTOR SWEEP on the 34-volt tap.
2. Adjust variable autotransformer to obtain V_{CE} of about 24 volts on VTVM (peak-to-peak scale).
3. Adjust I_B to obtain I_C of 5 amperes. (SENSITIVITY control on 1A/V position.) This step results in 5 volts of vertical deflection on the scope at the end of the sweep. There is your curve at the proper safety margin for the test.

NOTE: In operating the I_B controls, always start with the smallest battery-voltage tap (1.5 volt), with the battery switch in the proper position (pnp or npn.) If you can not obtain sufficient base current to get the desired I_C, go to the next higher tap. You will observe that the 2-mA position of the I_B range switch inserts an extra variable potentiometer ("2 mA range" in Fig. 17-5) because of the wide range of base currents required (from about 20 μA to 2 mA).

To test a zener diode, place S1 in the pnp position. Place the zener diode with the anode lead at the collector terminal of the tester and the cathode lead at the emitter terminal (reverse bias). Refer to Fig. 17-11.

As you increase the sweep voltage, the horizontal sweep on the scope CRT increases. When the zener breakdown voltage is reached, the trace

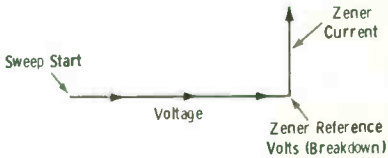
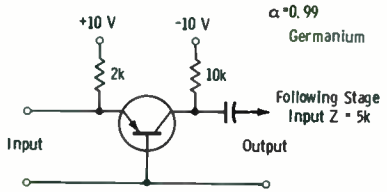


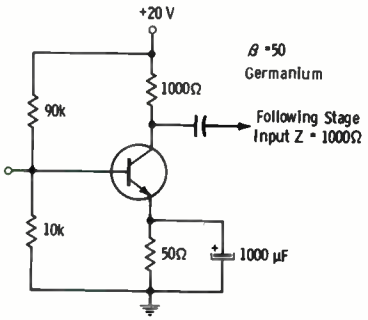
Fig. 17-11. Curve traced for a zener diode.

will sweep upward in this arrangement. For example, if you are testing a 20-volt zener, when the VTVM measures 20 volts (peak-to-peak scale), the upward trace should start. There is no "forward current" in this test, since the diode is being swept from zero to the required "reverse voltage." This provides a "clean" test for zener action.

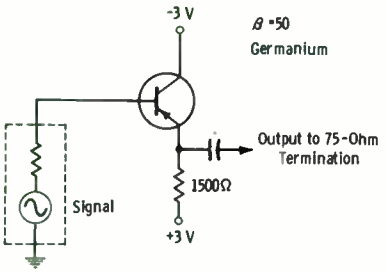
CAUTION: Never leave a transistor on in this test any longer than necessary to obtain the curve. Remember your test ratings are based on maximum ratings at "room temperature." When current is present, junctions are heated, resistances decreased, and currents increased. If you observe I_C starting to increase with no change in adjustment of I_B, *be alert*: you are nearing "thermal runaway." This is particularly likely to happen with large power transistors tested near maximum I_C.



(A) Circuit for Q17-2.



(B) Circuit for Q17-3 and Q17-5.



(C) Circuit for Q17-4.

Fig. 17-12. Circuits for exercises.

EXERCISES

Q17-1. If a transistor is being operated class A, what would be the minimum value of bias used with a 100 mV (peak-to-peak) input signal?

Q17-2. See Fig. 17-12A. What are the input impedance, load impedance, current gain, and voltage gain?

Q17-3. See Fig. 17-12B. What are the input imepdance, load impedance, current gain, and voltage gain?

Q17-4. See Fig. 17-12C. What is the emitter current (dc), and what is the internal output impedance?

Q17-5. What would be the voltage gain of the circuit in Fig. 17-12B without the emitter bypass?

Q17-6. When the input current is zero, is the current in the collector circuit due to minority or majority carriers?

Q17-7. Why is the reverse collector current with zero base current called "saturation current?"

Q17-8. If you have a V_{CC} of 20 volts, an R_L of 1000 ohms, and a V_{CE} of 10 volts, what is P_C?

Q17-9. If you have a V_{CC} of 20 volts, an R_L of 1k, and a V_{CE} of 20 volts, what does this indicate?

Q17-10. If you have a V_{CC} of 20 volts, an R_L of 1k, and a V_{CE} near zero, what does this indicate?

APPENDIX A

Useful Information

Table A-1. Prefix Symbols

Prefix	Symbol	Multiplier	Notes
tera	T	10^{12}	one trillion
giga	G	10^{9}	one billion (1000 mega)
mega	M	10^{6}	one million
kilo	k	10^{3}	one thousand
hecto	H	10^{2}	one hundred
deka	D	10	ten
deci	d	10^{-1}	one tenth
centi	c	10^{-2}	one hundredth
milli	m	10^{-3}	one thousandth
micro	μ	10^{-6}	one millionth
nano	n	10^{-9}	millimicro (one thousandth of one millionth)
pico	p	10^{-12}	micromicro (one millionth of one millionth)
atto	a	10^{-18}	millionth of micromicro

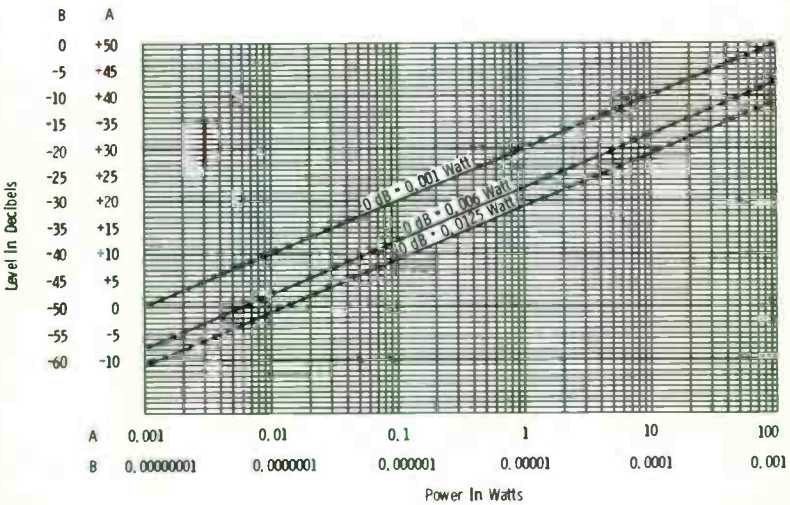


Fig. A-1. Power levels in watts and decibels.

Table A-2. Decibel Table

dB	Current and Voltage Ratio		Power Ratio		B	Current and Voltage Ratio		Power Ratio	
	Gain	Loss	Gain	Loss		Gain	Loss	Gain	Loss
0.1	1.01	0.989	1.02	0.977	8.0	2.51	0.398	6.31	0.158
0.2	1.02	0.977	1.05	0.955	8.5	2.66	0.376	7.08	0.141
0.3	1.03	0.966	1.07	0.933	9.0	2.82	0.355	7.94	0.126
0.4	1.05	0.955	1.10	0.912	9.5	2.98	0.335	8.91	0.112
0.5	1.06	0.944	1.12	0.891	10.0	3.16	0.316	10.00	0.100
0.6	1.07	0.933	1.15	0.871	11.0	3.55	0.282	12.6	0.079
0.7	1.08	0.923	1.17	0.851	12.0	3.98	0.251	15.8	0.063
0.8	1.10	0.912	1.20	0.832	13.0	4.47	0.224	19.9	0.050
0.9	1.11	0.902	1.23	0.813	14.0	5.01	0.199	25.1	0.040
1.0	1.12	0.891	1.26	0.794	15.0	5.62	0.178	31.6	0.032
1.1	1.13	0.881	1.29	0.776	16.0	6.31	0.158	39.8	0.025
1.2	1.15	0.871	1.32	0.759	17.0	7.08	0.141	50.1	0.020
1.3	1.16	0.861	1.35	0.741	18.0	7.94	0.126	63.1	0.016
1.4	1.17	0.851	1.38	0.724	19.0	8.91	0.112	79.4	0.013
1.5	1.19	0.841	1.41	0.708	20.0	10.00	0.100	100.0	0.010
1.6	1.20	0.832	1.44	0.692	25.0	17.7	0.056	3.16×10^{2}	3.16×10^{-3}
1.7	1.22	0.822	1.48	0.676	30.0	31.6	0.032	10^{3}	10^{-3}
1.8	1.23	0.813	1.51	0.661	35.0	56.0	0.018	3.16×10^{3}	3.16×10^{-4}
1.9	1.24	0.803	1.55	0.646	40.0	100.0	0.010	10^{4}	10^{-4}
2.0	1.26	0.794	1.58	0.631	45.0	177.0	0.006	3.16×10^{4}	3.16×10^{-5}
2.2	1.29	0.776	1.66	0.603	50.0	316	0.003	10^{5}	10^{-5}
2.4	1.32	0.759	1.74	0.575	55.0	560	0.002	3.16×10^{5}	3.16×10^{-6}
2.6	1.35	0.741	1.82	0.550	60.0	1,000	0.001	10^{6}	10^{-6}
2.8	1.38	0.724	1.90	0.525	65.0	1,770	0.0006	3.16×10^{6}	3.16×10^{-7}
3.0	1.41	0.708	1.99	0.501	70.0	3,160	0.0003	10^{7}	10^{-7}
3.2	1.44	0.692	2.09	0.479	75.0	5,600	0.0002	3.16×10^{7}	3.16×10^{-8}
3.4	1.48	0.676	2.19	0.457	80.0	10,000	0.0001	10^{8}	10^{-8}
3.6	1.51	0.661	2.29	0.436	85.0	17,700	0.00006	3.16×10^{8}	3.16×10^{-9}
3.8	1.55	0.646	2.40	0.417	90.0	31,600	0.00003	10^{9}	10^{-9}
4.0	1.58	0.631	2.51	0.398	95.0	56,000	0.00002	3.16×10^{9}	3.16×10^{-10}
4.2	1.62	0.617	2.63	0.380	100.0	100,000	0.00001	10^{10}	10^{-10}
4.4	1.66	0.603	2.75	0.363	105.0	177,000	0.000006	3.16×10^{10}	3.16×10^{-11}
4.6	1.70	0.589	2.88	0.347	110.0	316,000	0.000003	10^{11}	10^{-11}
4.8	1.74	0.575	3.02	0.331	115.0	560,000	0.000002	3.16×10^{11}	3.16×10^{-12}
5.0	1.78	0.562	3.16	0.316	120.0	1,000,000	0.000001	10^{12}	10^{-12}
5.5	1.88	0.531	3.55	0.282	130.0	3.16×10^{6}	3.16×10^{-7}	10^{13}	10^{-13}
6.0	1.99	0.501	3.98	0.251	140.0	10^{7}	10^{-7}	10^{14}	10^{-14}
6.5	2.11	0.473	4.47	0.224	150.0	3.16×10^{7}	3.16×10^{-8}	10^{15}	10^{-15}
7.0	2.24	0.447	5.01	0.199	160.0	10^{8}	10^{-8}	10^{16}	10^{-16}
7.5	2.37	0.422	5.62	0.178	170.0	3.16×10^{8}	3.16×10^{-9}	10^{17}	10^{-17}

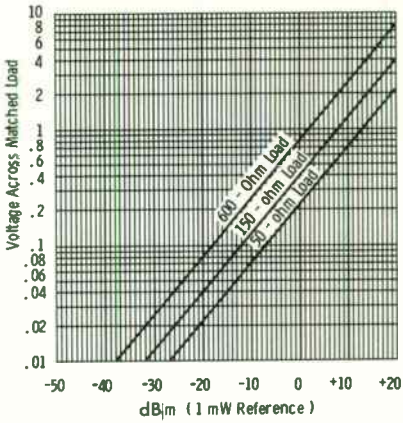


Fig. A-2. Voltages for levels above −30 dBm.

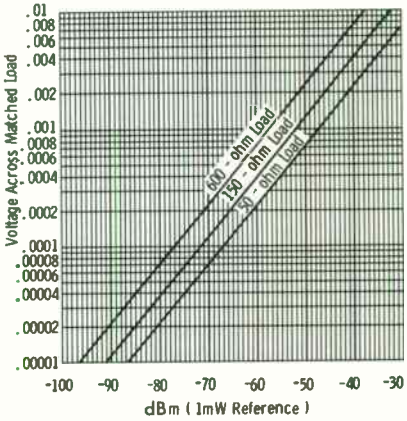


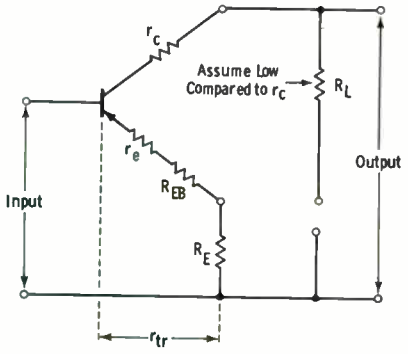
Fig. A-3. Voltages for levels below −30 dBm.

Table A-3. Symbols Used in This Book: Definitions

α	Alpha. Common-base short-circuit current gain.
A_i	Current gain.
A_p	Power gain.
A_v	Voltage gain.
β	Beta. Common-emitter short-circuit current gain.
f_{hfb}	Alpha cutoff frequency (common base).
f_{hfe}	Beta cutoff frequency (common emitter).
f_{max}	Maximum frequency of oscillation.
C_{ce}	Collector-emitter capacitance.
C_{eb}	Collector-base capacitance.
C_{in}	Input capacitance.
Ge	Germanium.
g_m	Transconductance.
h_{FE}	dc short-circuit current gain.
h_{fe}	ac (signal) short-circuit current gain.
I_B	dc base current.
I_b	ac (signal) base current.
I_C	dc collector current.
I_c	ac (signal) collector current.
I_{CO}	Collector leakage current (cutoff current).
I_E	dc emitter current.
I_e	ac (signal) emitter current.
r_e	Small-signal emitter resistance.
R_E	Emitter resistor.
R_{EB}	Emitter-base junction resistance (assume 4 ohms average).
R_f	Feedback resistance.
R_G	Generator resistance.
R_{in}	Input resistance.
R_L	Load resistance.
R_S	Source resistance.
r_{tr}	Transresistance.
Si	Silicon.
V_B	Base voltage (dc).
V_{BB}	Base supply voltage.
V_{BE}	Base-to-emitter voltage (dc).
V_C	Collector voltage (dc).
V_{CC}	Collector supply voltage.
V_{CE}	Collector-to-emitter voltage (dc).
V_E	Emitter voltage (dc).
V_{EE}	Emitter supply voltage.
Z_g	Generator impedance.
Z_{in}	Input impedance.
Z_o	Output impedance.
Z_s	Source impedance.

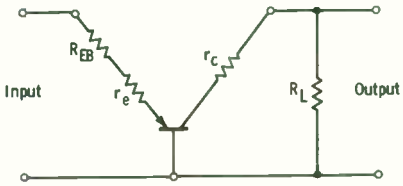
Base Current	$I_B = I_E - I_C = \frac{I_C}{h_{FE}}$ or $\frac{I_E}{h_{FE}} - I_{CO}$
Collector Current	$I_C = I_E - I_B = \alpha I_E = h_{FE} I_B$
Collector Power	$P_C = V_{CE} I_C$
Emitter Current	$I_E = I_B + I_C$ (Total Current)
Small-Signal Emitter Resistance	$r_e = \frac{26}{I_E}$ where, I_E is emitter current in mA.
Transresistance	$r_{tr} = r_e + R_{EB} + R_E$ where, r_e is the small-signal emitter resistance in ohms, R_{EB} is assumed to be 4 ohms, and R_E is the unbypassed external emitter resistance.
Transconductance	$g_m = \frac{1}{r_{tr}} = \frac{I_E}{26}$ where, I_E is emitter current in mA.
Bandwidth	$f_{hfe} = \frac{f_{hfb}}{h_{fe}}$, or $f_{hfb} = h_{fe} f_{hfe}$ where, f_{hfe} is the beta cutoff frequency (3-dB point), f_{hfb} is the alpha cutoff frequency (3-dB point), h_{fe} is $\beta = \frac{\alpha}{1 - \alpha}$
Upper Frequency Limit	$f_u = \frac{g_m}{6.28 C_t}$ where, f_u is upper frequency limit (unity gain) in MHz, g_m is transconductance in micromhos, and C_t is total capacitance in pF.
Input Capacitance	$C_{in} = \frac{g_m}{6.28 f_{hfb}}$

Fig. A-4. Basic parameters common to all configurations.



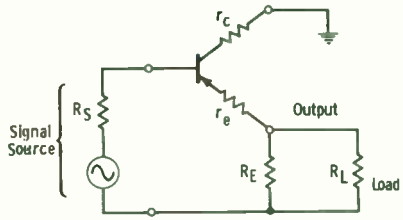
Input Impedance	$Z_{in} = h_{fe} r_{tr}$
Load Impedance	$Z_L = R_L$ in parallel with input impedance of next stage.
Current Gain	$A_I = \frac{\Delta I_C}{\Delta I_B} = h_{fe}$ where, $h_{fe} = \beta = \frac{I_c}{I_b} = \frac{\alpha}{1-\alpha}$
Voltage Gain	$A_v = \frac{\Delta V_C}{\Delta V_B} = \frac{Z_L}{r_{tr}} = g_m Z_L$
Power Gain	$A_p = \frac{V_{out} I_{out}}{V_{in} I_{in}} = \beta \frac{Z_L}{r_{tr}}$
Typical Values (Single Stage)	Z_{in} 500-1500 ohms Z_L 1k-50k A_v 100-1000 A_I 25-100 A_p 25-70 dB

Fig. A-5. Parameters of common-emitter circuit .



Input Impedance	$Z_{in} = r_{tr}$
Load Impedance	$Z_L = R_L$ in parallel with input impedance of following stage.
Current Gain	$A_i = \alpha = \frac{\beta}{1+\beta}$ (In practice, α is 0.95 to 0.995, or approximately 1.)
Voltage Gain	$A_v \approx \frac{Z_L}{r_{tr}} = g_m Z_L$
Typical Values (Single Stage)	Z_{in} 5-150 ohms Z_L 100k-500k A_v 100-1500 A_i Less than 1 (slightly) A_p 20-30 dB
(The common-base circuit is used primarily to match a low impedance to a high impedance.)	

Fig. A-6. Parameters of common-base circuit.



Input Impedance	$Z_{in} = (\beta + 1)Z_L$ where, Z_L is R_L in parallel with R_E.
Output Impedance	$Z_{out} = \frac{R_s}{\beta + 1}$ where, R_s is the output impedance of the signal source.
Current Amplification	$A_i \approx \beta$
Voltage Amplification	A_v = Less than unity
Typical Values (Single Stage)	Z_{in} 1k-500k Z_{out} 2-1000 ohms A_v Less than 1 A_i 25-100 A_p 10-35 dB
(The common-collector circuit is used primarily to match a high impedance to a low impedance.)	

Fig. A-7. Parameters of common-collector circuit.

APPENDIX **B**

Answers to Exercises

CHAPTER 1

A1-1. (B) Plus one.

A1-2. (A) Minus one.

A1-3. (B) In the orbit farthest from the nucleus.

A1-4. (B) Four.

A1-5. (B) Four.

A1-6. (B) Medium.

A1-7. Higher. The valence electrons are closer to the nucleus than is the case for germanium.

A1-8. (A) Lowered.

A1-9. (B) One more valence electron.

A1-10. (B) Positive.

A1-11. (A) One less valence electron.

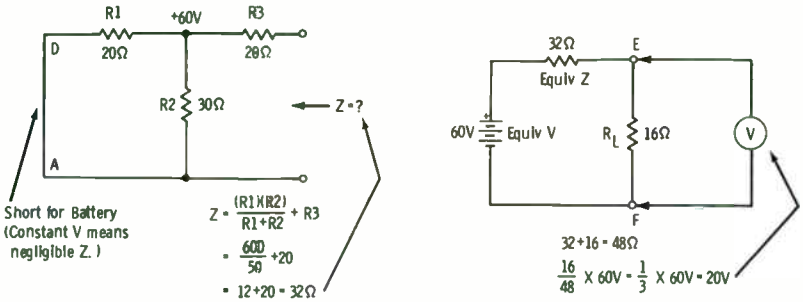
A1-12. (A) Negative.

A1-13. The answer is 50 volts. This should be evident to you immediately upon inspection. You know that the total drop across R1 and R2 is 100 volts, and since the resistances are of equal value, ½ of 100 volts is dropped across each resistor.

A1-14. The answer is 60 volts. Again the drop across R1 plus the drop across R2 is equal to 100 volts. R1 + R2 = 50 ohms. Since R2 is $^{30}/_{50}$ of 50 ohms, the voltage across R2 is ⅗ of 100 volts, or 60 volts.

A1-15. The voltage measured between terminals E and F is the same as that across R2 (60 volts), since there is no current through R3 (assuming a high-impedance voltmeter).

A1-16. This question tests your ability in basic circuit analysis. Note that a constant-voltage source (the battery) has been specified. (In practice, the internal resistance of a good dry cell is less than 0.01 ohm, which can be ignored.) It is now most convenient to find the impedance looking back into the network from the output, with the load (R_L) disconnected (Fig. B-1A). Since the battery



(A) Load disconnected. *(B) Equivalent circuit.*

Fig. B-1. Solution for Q1-16.

is a constant-voltage (low-impedance) source, it is replaced with a short circuit from terminal A to terminal D. Now by inspection you can see this places R1 and R2 in parallel, with R3 in series. You see by the solution in Fig. B-1A that the equivalent impedance is 32 ohms.

Now see Fig. B-1B. From A1-15 you know that the equivalent voltage between terminals E and F with R_L disconnected is 60 volts, and you have found the equivalent impedance to be 32 ohms. From the solution in Fig. B-1B, you can see that the voltage across R_L is 20 volts.

The above procedure is a practical application of Thevenin's theorem. It is simply Ohm's law applied to network analysis.

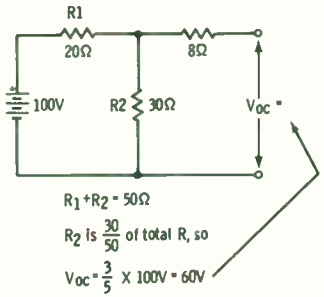
A1-17. In all of our practical analysis of solid-state circuits, we will not use any more complicated approaches than this simplified analysis procedure, so be sure you can master it. You should be able to follow the solution to this exercise in parts A, B, and C of Fig. B-2, Fig. B-2A shows how to find the open circuit voltage, V_{OC} (switch of Fig. 1-8 in B position). In Fig. B-2B, the constant-voltage source (negligible impedance) has been replaced with a short to permit finding the equivalent impedance looking back into the network from the load side. In Fig. B-2C, the equivalent circuit has been drawn so that V_L can be found conveniently.

But now let us simplify the handling of such analysis still further. You know that for any closed loop the voltage drops are directly proportional to resistance (or impedance) for a given source voltage. So the load voltage at the the network output can be put into terms of the equivalent voltage and equivalent impedance as follows:

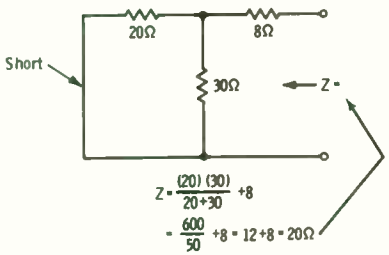
$$V_L = V_{EQ} \frac{R_L}{Z_{EQ} + R_L} = \frac{V_{EQ} R_L}{Z_{EQ} + R_L}$$

where,

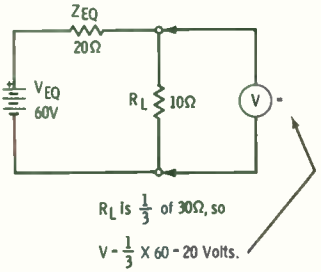
V_{EQ} is the equivalent voltage, and
Z_{EQ} is the equivalent (open-circuit) impedance.



(A) *Open-circuit voltage.*



(B) *Equivalent impedance.*



(C) *Equivalent circuit.*

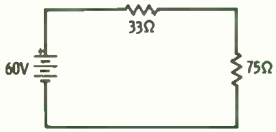
Fig. B-2. Solution for Q1-17.

So in Fig. B-2C, substituting the known values in the above equation gives:

$$V_L = \frac{60 \times 10}{30} = 20 \text{ volts}$$

You can see that this method simplifies the final computation when the resistances do not have an obviously easy ratio to calculate the voltage ratio. (As an example, suppose the equivalent Z is 33 ohms, and R_L is 75 ohms, as in Fig. B-3.)

A1-18. Now you should use Ohm's law for current analysis rather than voltage analysis. Disconnect R_L to get the short-circuit current, I_{SC}, as in Fig. B-4A. Resistor R2 is shorted out by the ammeter, so R1 is in series with the source; thus I_{SC} is 5 amperes. Then find the equivalent impedance looking back into the network, as in Fig. B-4B. Since the battery has negligible resistance, it is replaced with a short, so R1 and R2 are in parallel. Thus Z_{EQ} is



(A) *Equivalent circuit.*

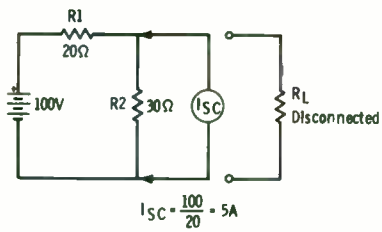
$$V_L = \frac{V_{EQ}\, R_L}{Z_{EQ}+R_L}$$

$$V_L = \frac{(60)(75)}{33+75} = \frac{4500}{108}$$

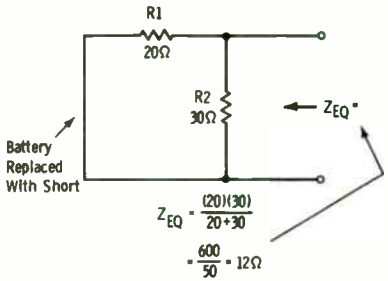
$$= 41.66 \text{ Volts}$$

(B) *Computation.*

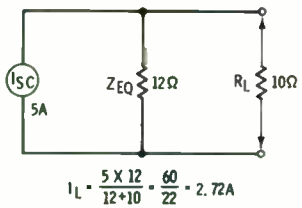
Fig. B-3. Simplified circuit solution.



(*A*) *Short-circuit current.*



(*B*) *Equivalent impedance.*



(*C*) *Equivalent circuit.*

Fig. B-4. Solution for Q1-18.

12 ohms. Now, since the short-circuit current has been derived, you can use Norton's theorem, which states that any linear network of sources and impedances, if viewed from any two points in the network, can be replaced by an equivalent impedance in *shunt* with an equivalent constant-current source. The current from the equivalent source is the current that would pass through a short between the two points, and the equivalent impedance is the impedance seen when looking into the network from the two points. Observe Fig. B-4C; simply connect R_L to the equivalent circuit. You can see that if R_L were 12 ohms, the current would be equally divided, with 2.5 amperes in each branch. However, R_L is slightly less than Z_{EQ} and will draw a little more of the total current. The formula for making use of Norton's theorem is in the same form you found for Thevenin's theorem, except the product (numerator) contains Z_{EQ} instead of R_L:

$$I_L = I_{SC} \frac{Z_{EQ}}{Z_{EQ} + R_L} = \frac{I_{SC} Z_{EQ}}{Z_{EQ} + R_L}$$

In Fig. B-4, the current is found to be 2.72 amperes.

A1-19. Now you are working with a "constant-current source." In Fig. B-5A, I_{SC} is found to be 1 mA. In Fig. B-5B, the constant-current source is replaced with its equivalent impedance (100,000 ohms); the impedance looking back into the network from the load side is

found to be 30 ohms. Then in Fig. B-5C, I_L is found to be 0.75 milliampere.

You will note from the above that the small value of R1 (in ratio to the internal impedance) is ignored, since it affects the result hardly at all. This also tells you that when you have such a low-impedance network across a high-impedance source, the impedance looking back from the output may be taken as the value of the shunt arm, R2 in this case.

A1-20. 35 ns = 0.035 μs.

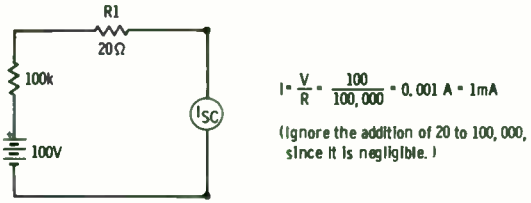
A1-21. 0.01 GHz = 10 MHz.

A1-22. 470 $\mu\mu$F; 0.00047 μF.

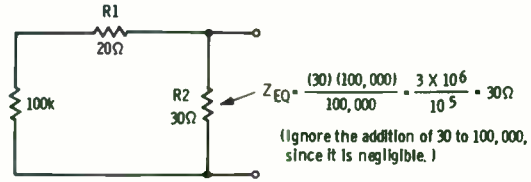
A1-23. Essentially −3 dB.

A1-24. Essentially −6 dB.

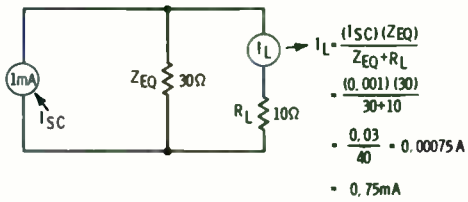
A1-25. 0.199×10^{-5}. First find the power ratio for a 50-dB loss. This is 10^{-5}. The power ratio for a 7-dB loss is 0.199, and the product (to add dB, power ratios must be multiplied) is 0.199×10^{-5}.



(A) Short-circuit current.



(B) Equivalent impedance.



(C) Equivalent circuit.

Fig. B-5. Solution for Q1-19.

CHAPTER 2

A2-1. The two currents are electron current and hole current.

A2-2. A hole is a vacancy in the valence-band structure of a semiconductor material. It must be considered a mobile carrier, since it is caused to drift through the structure by the forces applied.

A2-3. Electrons.

A2-4. Yes. Electrons (the majority carriers) far outnumber the holes, which are the minority carriers. In a p-type material, the holes (majority carriers) far outnumber the electrons, which become the minority carriers.

A2-5. Yes. Neither n-type nor p-type material alone has rectifying properties.

A2-6. No. At the higher temperature, many more carriers are made available, and the resistance to current decreases, causing increased current for a given applied voltage.

A2-7. The direction of the junction field is such that it always aids minority current. The polarity and magnitude of the bias voltage merely determine the degree of aid.

A2-8. The + end normally indicates the cathode.

A2-9. There would be practically no output voltage. See Fig. 2-5. The result would be the same as for an ordinary diode, resulting in an output of about 1 volt.

A2-10. The zener current would increase because the load current would no longer be present to contribute to the voltage drop across R_S. This is voltage regulation; as the load current increases, the zener current decreases, and vice versa, to hold the zener voltage constant.

A2-11. The diode will not conduct on the positive peak, and the sine wave will be passed as a sine wave (no clipping).

A2-12. Assuming silicon diodes, neither would conduct. The circuit would behave as an open switch, and no signal would appear across the load resistor.

A2-13. No. It will measure very high resistance in both directions.

A2-14. Gate voltage sufficiently positive with respect to the cathode, and anode voltage sufficiently positive with respect to the cathode.

A2-15. Yes, just as for any solid-state device.

CHAPTERS 3 AND 4

A4-1. Since the input circuit of a conventional transistor must be forward biased, the input impedance is lower than that of a tube circuit in the common-cathode mode of operation (grid input).

A4-2. Because they assume "positive charge" to be moving *away* from the pnp transistor in the base and collector leads.

A4-3. Since an R_L of 1000 ohms is only $\frac{1}{1000}$ of the intrinsic r_c, you can assume h_{fe} (short-circuit forward current gain) to be the same with the load as with a short circut. Where much higher values of R_L are used, construction of the load line on the output characteristic curves is more accurate.

A4-4. $$h_{fe} = \frac{h_{fb}}{1 - h_{fb}} = \frac{0.95}{0.05} = 19$$

A4-5. All that is necessary is that the base of a pnp transistor be negative relative to the emitter, and that the collector be negative relative to the base and emitter. The emitter of Fig. 4-1C is approximately at ground potential and therefore positive relative to base and collector. Bias resistor R_B and collector load R_L must be so chosen for the currents involved that the base voltage is sufficient to provide a forward-biased emitter-base junction, while the collector is more negative than the base. This subject will be covered further in the next Chapter.

A4-6. (A) $I_C = \alpha I_E$
(B) No.

A4-7. Alpha cutoff is the 3-dB (0.707-current) point. So let us compare h_{fe} at low frequencies to the resulting h_{fe} at the "cutoff" point. At low frequency:

$$h_{fe} = \frac{0.99}{1 - 0.99} = 99$$

But at the alpha cutoff frequency, α is down to 0.7 of its former value:

$$0.99 \times 0.7 = 0.69$$

so:

$$h_{fe} = \frac{0.69}{1 - 0.69} = \frac{0.69}{0.31} = 2 \text{ (approx)}$$

Thus h_{fe} is approximately 2 at 100 MHz, compared to 99 at low frequency.

A4-8. Greater by beta times R_E (approximately).

CHAPTER 5

A5-1. The input impedance is:

$$Z_{in} = \frac{26}{I_e} + R_{EB} = \frac{26}{10} + 4 = 2.6 + 4 = 6.6 \text{ ohms}$$

So, the required build-out resistance is:

$$75 - 6.6 = 68.4 \text{ ohms}$$

In practice, a 68-ohm resistor would be used.

A5-2. The operating point shifts upward on the load line (greater I_c).

A5-3. Fixed bias is a voltage applied to an element directly from the power source. Self-bias is obtained from a point in the circuit so that the bias is dependent on the current being drawn; thus, compensation is made for current changes to stabilize the operating point.

A5-4. Leakage current (I_{co}) is amplified by beta in the common-emitter circuit.

A5-5. $f_{hfe} = f_{hfb}/h_{fe} = 1000/50 = 20$ MHz.

A5-6. $75 - 13 = 62$-ohm build-out required.

A5-7. The signal amplitude would be about 0.38 volt across the 75-ohm receiving termination.

A5-8. The output impedance would decrease.

A5-9. No. The reactance of C1 at 30 Hz (about 1000 ohms) will be greater than $r_g + R_{in}$ (about 750 ohms).

A5-10. The sum of r_g and R_{in} is now about 1350 ohms, so the input response will be within 3 dB at 30 Hz. But C2 would be entirely inadequate.

A5-11. The low-frequency response would be poorer than with an h_{FE} of 40.

A5-12. (A) Low-frequency response would be improved. (B) Voltage gain would not be affected, since R3 is bypassed. But since V_{CE} is reduced, the maximum amplitude before clipping would be reduced.

A5-13. This RC network in parallel with the load limits the increase of inductive load impedance which would result in phase shift at increasing frequencies. You will find a similar network in most discrete amplifiers feeding a speaker; it is not peculiar to IC circuitry.

A5-14. If you check signal polarity, you will find this network provides positive signal feedback; therefore it is a "bootstrap" circuit.

A5-15. Because of the excellent high-frequency capability of monolithic transistors, more precautions are required to prevent high-frequency oscillation than is the case with discrete amplifiers. The 0.001-μF capacitor stabilizes high-frequency operation by decreasing the effective bootstrapping of R3 at extremely high frequencies.

A5-16. By checking for proper input signal and then checking the output for proper amplitude. All input voltages should be checked for proper values. For example, a low voltage at pin 3 would result from excessive drop across R3 and would indicate a shorted or leaky element. The entire chip is replaced if trouble exists.

A5-17. (1) Gain variation from zero to maximum. (2) Minimum noise

level. (3) No effect on frequency response over the gain-control range.

A5-18. No dc in the gain control.

A5-19. Agc voltage should go less positive with increasing signal amplitude.

A5-20. Very satisfactorily (if the reaction time of 5 to 20 milliseconds can be tolerated).

A5-21. Variable-amplification and variable-impedance.

A5-22. Yes, by use of a variable pot together with a dc supply of the proper polarity.

A5-23. $V = \sqrt{WR} = \sqrt{(0.001)(600)} = \sqrt{0.6} = 0.774$ volt

A5-24. $V = \sqrt{(0.001)(150)} = \sqrt{0.150} = 0.387$ volt

A5-25. Watts $= E^2/R$
For 600 ohms:

$$W = (0.774)^2/600 = 0.6/600 = 1 \text{ mW}$$

For 150 ohms:

$$W = (0.387)^2/150 = 0.15/150 = 1 \text{ mW}$$

A5-26. The output is −10 dBm in 150 ohms. From Fig. A-2 in Appendix A, you would estimate about 0.125 volt (125 mV). Working it longhand, from the decibel table (Table A-2, Appendix A) −10 dB is a 0.1 power ratio, so the 1 mW reference is reduced to 0.1 mW.
Then:

$$V = \sqrt{(0.0001)(150)} = \sqrt{0.015} = 0.123 \text{ volt}$$

A5-27. Peak-to-peak signal voltage is 2.8 times rms voltage, so:

$$(2.8)(0.123) = 0.344 \text{ volts}$$

A5-28. To operate the stage at a very low collector current and voltage in the interest of obtaining a low noise factor.

A5-29. From Table A-2 in Appendix A, the corresponding power ratios are:
(A) 1.58
(B) 3.16
(C) 10.0
(D) 100.0

A5-30. No voltage gain does not necessarily mean no power gain when the input and output impedances are not equal. For example, in the circuit of Fig. 5-22, assume a signal of 2mV at the base of Q1, and 2 mV at the collector (unity gain). Further assume that h_{fe} of Q1 is 40 at the operating point; then $Z_{in} = (h_{fe})(r_{tr}) = (40)(168) = 6720$ ohms. This impedance is reduced by the shunt path of the T1 secondary in series with R2 and R3 in parallel; the actual impedance into Q1 becomes about 5000 ohms. (The

secondary of T1 presents a rather high-impedance path for the audio frequencies concerned.) So 2 mV of signal in 5000 ohms is:

$$W = E^2/R = (0.002)^2/5000$$
$$= 0.8 \times 10^{-9}\ W \text{ (approx) at the input}$$

You have already determined that the collector load is about 720 ohms, so the 2 mV of signal in the collector is:

$$W = (0.002)^2/720$$
$$= 5.5 \times 10^{-9}\ W \text{ (approx) at the collector}$$

This is a power gain of $5.5/0.8 = 6.9$ times (about 8.4 dB).

A5-31. In the negative-feedback circuit.

A5-32. The noise factor increases as the frequency is lowered.

A5-33. Since this is a class-A amplifier, assume the Q2 collector voltage is one-half the collector supply voltage, −11 volts. Then for Q2:

$$I_C = \frac{11\ V}{10k} = 1.1\ mA$$
$$I_E = 1.1\ mA \text{ (approx)}$$
$$V_E = (-1.1\ mA)(2700\ ohms) = -3.0\ V$$
$$V_B = -3.0v + (-0.2\ V)$$
$$= -3.2v \text{ (2N508 is germanium)}$$

Now, for Q1:

$$V_C = -3.2v$$
$$\text{Drop across } R_{L1} = -22\ V - (-3.2\ V) = 18.8\ V$$
$$I_C = 18.8/20k = 0.94\ mA$$
$$I_E = 0.94\ mA \text{ (approx)}$$
$$V_E = (-94\ mA)(1600\ ohms) = -1.5\ V$$
$$V_B = -1.5 + (-0.2) = -1.7\ V$$

A5-34.

	(A) CB	(B) CE	(C) CC
h_{FB}	I_C/I_E		
h_{FE}		β, or I_C/I_B	
h_{FC}			I_E/I_B
I_B	$(1-\alpha)I_E$	$(1-\alpha)I_E$	$(1-\alpha)I_E$
I_C	αI_E, or $I_E - I_B$	$I_E - I_B$	$I_E - I_B$
Voltage Gain?	Yes	Yes	No

A5-34.—(Continued)

	(A) CB	(B) CE	(C) CC
Current Gain?	No (less than unity)	Yes	Yes
Power Gain?	Yes	Yes (highest)	Yes
Phase Inversion?	No	Yes	No
Comparative Input Z	Lowest	Intermediate	Highest
Comparative Output Z	Highest	Intermediate	Lowest

A5-35. The CE circuit, because the collector current contains a component $(h_{FE})(I_{CO})$.

A5-36. Temperature increase.

A5-37. Resistance decreases (negative temperature coefficient).

A5-38. Bias voltages and currents.

A5-39. Bias voltages and currents.

A5-40. Point 2 will be negative relative to point 1. Point 2 will be positive relative to point 3.

A5-41. Total current through R1-R2 is $20/40k = 0.5$ mA (base current assumed negligible). The 0.5 mA through R2 produces (0.5 mA) (4000 ohms) = 2 volts base to ground.

A5-42. Since Q1 is germanium, the emitter voltage to ground is about +1.8 volts. So the emitter current is $1.8/1000 = 0.0018$ amp = 1.8 mA.

A5-43. The collector current is (0.98) (1.8 mA) = 1.76 mA.

A5-44. $V_B = +2$ V; $V_E = +1.8$ V; $V_C = +11.2$ V.

A5-45. Since V_E is 1.8 V and V_C is 11.2 V, then $V_{CE} = 11.2 - 1.8 = 9.4$ V.

A5-46. $P_C = (9.4\text{ V})(1.76\text{ mA}) = 16.5$ milliwatts.

A5-47. $\beta = \alpha/(1-\alpha) = 0.98/0.02 = 49$ (For quick analysis, the value of β can be assumed to be 50.)

A5-48. $I_B = I_C/\beta = 1.76$ mA$/50 = 35$ μA (approx)

A5-49. Input $Z = (r_{tr})(h_{FE}) = (26/1.8 + 4 + 1000)(50)$
$= 1018\ (50) = 50{,}900$ ohms

A5-50. Load Z = 5k in parallel with 5k = 2.5k (approx)

A5-51. $A_v = R_L/r_{tr} = 2500/1018 = 2.5$ (approx)

A5-52. With a large R_E you know that A_v is essentially R_L/R_E, or $2500/1000 = 2.5$ times

A5-53. $I_E = 10/5000 = 2$ mA. $I_C = (0.98)(2\text{ mA}) = 1.96$ mA (Can be assumed to be 2 mA—same as emitter current—for rapid analysis.) Input $Z = r_{tr} = 26/2 + 4 = 17$ ohms. Load Z = 5k in parallel with 5k = 2.5k

A5-54. V_E should be about +0.2 to +0.3 V. V_C should be about −10 V.

A5-55. $A_v = \dfrac{\text{Load Z}}{\text{Input Z}} = 2500/17 = 147 \text{ (approx)}$

A5-56. There will be very little actual difference because the degenerative emitter resistance in Fig. 5-42 greatly reduces the input capacitance. But note the extreme difference in gain to get approximately the same bandwidth.

A5-57. The extremely low input impedance. To get an input impedance equivalent to that of Fig. 5-42, a large series resistor would be necessary in the signal path to the emitter, greatly reducing A_v.

A5-58. For Fig. 5-42:

$$A_p = \beta \frac{R_L}{r_{tr}} = 50\ (2.5) = 125$$

For Fig. 5-43:

$$A_p = \alpha^2 \frac{R_L}{r_{tr}} = (0.98)^2\ (147)$$
$$= (0.96)\,(147) = 141$$

A5-59. The new $r_{tr} = 26/1.8 + 4 = 18$ ohms (approx)
Then $A_v = 2500/18 = 139$
Input $Z = (18)\,(50) = 900$ ohms

$$Ap = (50)\left(\frac{2500}{18}\right) = 6950$$

Although a higher impedance than in Fig. 5-43 has been obtained at approximately the same voltage gain, the bandwidth is less.

A5-60. Yes, very much. High-frequency types are manufactured which offer much improvement in bandwidth over lower-frequency types.

A5-61. Input Z of transistor is 17 ohms (see A5-53). So, $R_s = 75 - 17 = 58$ ohms. The 75-ohm line is "transformed" to an impedance of 5000 ohms in parallel with the following load. Both voltage and power gain are provided in this transformation.

A5-62. The input signal now appearing at the emitter is $17/75 = 0.23$ (approx) of the signal at the end of the 75-ohm line. So the actual voltage gain is now $(0.23)\,(147) = 34$ (approx). Compare this result to A5-55.

A5-63. $Z_{out} = 5000/(50 + 1) = 100$ ohms (approx) looking back into the emitter itself. Then $R_s = 100 - 75 = 25$ ohms.

A5-64. $1/75 = 13.3$ mA (approx) peak to peak.

A5-65. The total supply voltage is 20 volts (collector and emitter work between minus 10 and plus 10 volts respectively). So $R_E = V/I = 20/0.02 = 1000$ ohms. A signal swing more than 20 mA pk-pk will then cause clipping.

A5-66. Use of a stage with low output impedance (such as another emitter follower) to drive an emitter follower.

CHAPTER 6

A6-1. (A) $V_B = 5$ volts (from R1-R2 voltage divider)
So $V_E = 5 - 0.2 = 4.8$ volts
Then $I_E = 4.8/1000 = 4.8$ mA

$$\text{If } h_{FE} = \beta = 50,\ \alpha = \frac{\beta}{1+\beta} = \frac{50}{1+50} = 0.98$$

Then $I_C = (0.98)(4.8) = 4.7$ mA

(B) $Z_{in} = \beta r_{tr} = (50)(1000) = 50\text{k}$ (approx) for transistor
But the actual Z_{in} of the stage is determined by R1 in parallel with R2 (much lower than the 50k of the transistor). So:

$$Z_{in} = \frac{(15\text{k})(5\text{k})}{5\text{k} + 15\text{k}} = 3.75\text{k} \text{ (approx)}$$

(C) $Z_L = R_L$ in parallel with Z_{in} of the following stage.
(D) The ratio of R_L to R2, or about 2 times (if Z_{in} of the following stage is high).

A6-2. With R3 bypassed, r_{tr} would be:

$$r_{tr} = \frac{26}{4.8} + 4 = 10 \text{ ohms (approx)}$$

Then:

$$g_m = \frac{1}{r_{tr}} = 0.1 \text{ mho}$$

The voltage gain with R3 bypassed would be:

$$A = \frac{R_L}{r_{tr}} = \frac{2000}{10} = 200$$

The voltage gain with R2 not bypassed is:

$$A_v = \frac{A}{g_m R_E} = \frac{200}{0.1(1000)} = 2$$

A6-3. The R1-R2 voltage divider gives a voltage of 3 volts at the Q1 base. See Fig. B-6; this is the dc equivalent circuit. Note that the feedback shown in this diagram is dc feedback only; C2 and R4 provide a bypass around R6 to frequencies in the passband. Coupling capacitors C1 and C3 prevent the dc operating point from being influenced by source and load characteristics.

Since the voltage at the base of Q1 is 3 volts, V_E of Q1 is $+3 - 0.6 = 2.4$ volts. The current through R6 to produce this 2.4 volts is $2.4/1000 = 2.4$ mA.

At Q2 there will be a 0.6-volt difference between emitter and base, so V_B of Q2 $= 6 - 0.6 = 5.4$ volts. This is also the voltage at the collector of Q1. The current through R3 to drop 0.6 volt is $0.6/1000 = 0.6$ mA, and almost all of this current goes to the Q1 collector. The emitter current of Q1 will also be about 0.6 mA.

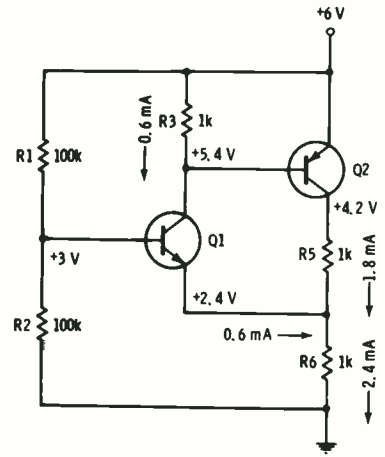


Fig. B-6. Dc equivalent of Fig. 6-15.

The current through R6 is 2.4 mA. Since 0.6 mA of this current comes from the emitter of Q1, $2.4 - 0.6 = 1.8$ mA must come through R5. The voltage drop across R5 is then $(1.8)(1) = 1.8$ volts. The voltage at the collector of Q2 is the sum of the voltage drops across R5 and R6, or $2.4 + 1.8 = 4.2$ volts.

A6-4. Q1 base voltage $= +0.7$ volt (approx)
Q2 emitter current $= 10.7/10{,}000 = 1$ mA (approx)
Voltage across $R_f = (0.001)(3000) = 3$ volts (approx)
Q2 emitter voltage $0.7 + 3 = +3.7$ volts (approx)
Therefore, Q2 base and Q1 collector voltage $= 3.7 + 0.7 = +4.4$ volts (approx)

A6-5. The maximum current swing is ± 1 mA in 75 ohms, so the maximum peak-to-peak voltage is $(0.002)(75) = 0.15$ volt.

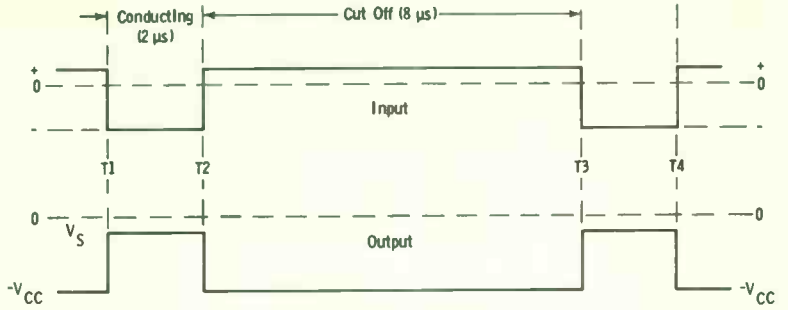
CHAPTER 8

A8-1. The pulse period is 20 μs, and the duty cycle is 0.5, or 50 percent.

A8-2. The duty cycle is 50 percent.

A8-3. The pulse frequency is 25 kHz, and the duty cycle is 0.25, or 25 percent.

A8-4. (1.) Transistor B is a pnp type. The transistor will be cut off when the waveform on the base side of the coupling capacitor goes in the positive direction, and the transistor will saturate when the waveform goes in the negative direction (Fig. B-7). Therefore collector current will be drawn from T1 to T2, or 20 percent of each cycle. The duty cycle is 20 percent.
(2.) Collector current will be drawn from T2 to T3, or 80 percent of each cycle, by npn transistor B (Fig. B-8). The duty cycle is 80 percent.



Collector current is drawn for 2/10=0.2 =20% of each cycle. Duty cycle is 20%.

Fig. B-7. Waveforms for pnp transistor (A8-4).

A8-5. Average power = (peak power)(duty cycle) = (100 mW)(0.2) = 20 mW.

A8-6. 80 mW.

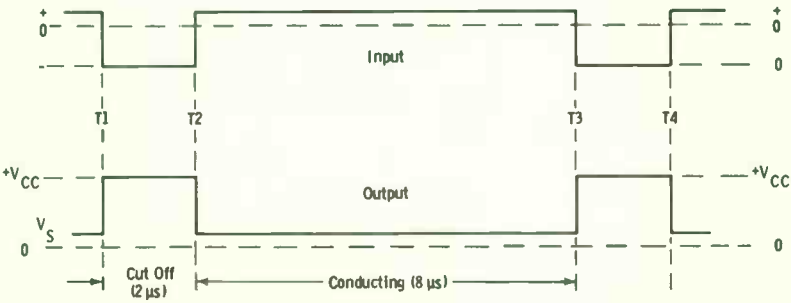
A8-7. Duty cycles are interchanged.

A8-8. You know that if the transistor is saturated, I_C must be $V_{CC}/R_L = 10/1000 = 10$ mA. Since the current gain is approximately $R_B/R_L = 10k/1k = 10$, the required base current is 1/10 of $I_C = 1$ mA. To give 1 mA of I_B, the input pulse must have an amplitude $V = IR = (0.001)(10{,}000) = 10$ volts. This is the same amplitude as the dc collector supply voltage.

Just these three elements work very well as a pulse amplifier. But for minimum storage time (minimum pulse widening), the transistor must be kept from saturation.

A8-9. Now the circuit current gain is $5k/1k = 5$. The base current must be 1/5 of the collector current, or 2 mA, so the required pulse amplitude is (0.002)(5000) = 10 volts (same as supply voltage).

A8-10. It can work very well under controlled temperature conditions. A



Collector current is drawn for 8/10 =0.8 =80% of each cycle. Duty cycle is 80%.

Fig. B-8. Waveforms for npn transistor (A8-4).

germanium transistor takes only about 0.2 volt (negative for a pnp transistor) at the base to turn it on. This voltage can be provided by leakage currents at high junction temperatures. If R_B is made low in value, leakage current is drained away and cannot be amplified. Silicon transistors, with their higher required forward bias (0.6 to 0.7 volt) for turn-on, are more suitable for this simple circuit. The same goes for the circuit of Fig. 8-10. You will realize also that the problem of leakage current is overcome by applying a small amount of reverse bias voltage to the base-emitter junction.

CHAPTER 9

A9-1. Width = (K) (RC) = (0.7) (0.005) (1370) = 4.8 μs (approx).

A9-2. Minimum width = (0.3) (0.0022) (1000) = 0.66 μs (approx).

Maximum width = (0.3) (0.0072) (1000) = 2.2 μs approx).

A9-3. No; it is probably intended as a linear amplifier. Remember this: For the transistor to be in saturation without depending upon h_{FE}, the ratio of R_B to R_L must be *less* than the *minimum* h_{FE} rating of the particular transistor. You will recognize a saturated circuit if the ratio of R_B to R_L is about 20 or less. This is *not* to say that the circuit as mentioned in the question could not saturate. It has no stabilization circuitry, and if h_{FE} is more than 100, or at higher temperatures (more leakage current), it can saturate.

A9-4. As a low impedance source driving a capacitive load. This load may be a number of paralleled circuits (where the total capacitance can accumulate to a significant value), or it may consist of diode "quads" (bridges), which can exhibit considerable capacitance.

A9-5. Obviously some video (an amount depending upon video "setup" level) will be present along the baseline of the pulse at the Q1 emitter. This video will not be removed by the Q2 stage since this stage clips only the sync-tip region.

A9-6. The answer depends on circuit conditions. If the values of the coupling capacitors and base resistors are such as to form a differentiating circuit, you have the condition of Fig. 9-3, and negative input pulses give positive pulses at the bases. The base pulses must still be coincident, however.

CHAPTER 10

A10-1. You would expect a pulse duration of approximately:

(0.7) (R1C1) = (0.7) (0.022) (680) = 10.5 μs.

A10-2. Yes. See Figs. 10-2C and 10-2D. This condition is normal only in complementary-symmetry circuits. If it should occur in other circuits, "lockout" results, and the multivibrator is inoperative.

A10-3. The pulse duration is about 20 μs. Now for a trigger pulse to produce reliable triggering, all capacitance must be charged (or discharged) before the arrival of a trigger pulse. Each pulse must find the circuit in the same state as it was for the previous pulse. If charging (or discharging) is still occurring, the result is equivalent to *reducing* the trigger-pulse amplitude. So trigger pulses must be farther apart than the output pulse *duration.* An interval of 20 μs corresponds to a frequency of $1/20(10^{-6}) = 50$kHz. You would expect a trigger frequency *under* this rate.

A10-4. 25 kHz.

A10-5. Resistor R4 makes the emitter potential slightly negative so that the base of the off transistor is more positive than the emitter and will hold the transistor off reliably until it is triggered.

A10-6. The emitter resistor would now establish a slight positive voltage. Thus the base of the off transistor is more negative than the emitter and the transistor can not conduct. When the emitters go negative from the trigger, the on transistor is not affected, but the off transistor is turned on. Regeneration completes the flopping action.

A10-7. These resistors form a voltage divider to supply a small reverse bias to the steering diodes. The trigger voltage is developed across resistor R9.

A10-8. Total division $= 2^3 = 8$. Then:

$$\frac{240}{8} = 30 \text{ Hz at the output}$$

CHAPTER 12

A12-1. The Q2 base voltage formed by voltage divider R1-R2-R_{B2} is -5 volts. The type 2N396A is germanium, so with Q2 on, V_E is about -4.8 volts. So the UTP is -5 volts (Q1 will conduct if the input is more negative than -5 volts). With Q1 on, for a quick computation you can say that Q1 takes most of the current since the parallel path of $R2 + R_{B2}$ is high in resistance compared to R_E. So the Q1 current is approximately $-12/2360 = -5$ mA. Therefore V_E is $(-0.005)(560) = -2.8$ volts. So the LTP is -3 volts (approx). Then Q2 will conduct if the input is less negative (more positive) than -3 volts. The output pulse will vary between about -3 and -12 volts (see Fig. B-9), for a peak-to-peak value of about 9 volts.

A12-2. For analysis, always start by determining the quiescent operating conditions. First, ignore the diode and examine Q1. The voltage at the base would be:

$$\frac{1}{1+68}\,70 = +1 \text{ volt (approx)}$$

So the transistor would be cut off without the diode in the circuit. Now ignore the transistor and examine the diode. As a first

approximation, ignore R2 also. Then the diode current would be $-20/8.5 = 2.4$ mA (approx). The voltage drop across R1 would be $-2.4(7.5) = -18$ volts, so the cathode of X1 would be at -2 volts and the anode at -1.4 volts (silicon diode). Thus with the diode in the circuit, Q1 conducts.

With Q1 conducting, its base (and the anode of X1) would be held at about -0.2 volt. (The 2N967 is germanium). With a 0.6-volt drop across X1, you know that the clamped point of the waveform at the junction of R1 and X1 is -0.8 volt (approx).

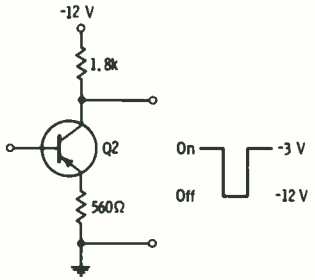


Fig. B-9. Solution for Q12-1.

On
- On Current = -12/2360 = -5 mA
- Drop Across 1.8k = (-0.005) (1800) = -9V
- Collector Volts = -12 -(-9) = -3 V

Off
- Off Current = 0
- Collector Volts = - 12 V

When the positive-going input pulse is applied, at some positive potential X1 will open. Since voltage divider R2-R3 places $+1$ volt on the anode (with Q1 nonconducting), as the input pulse reaches this $+1$ volt plus the 0.6 volt required for conduction ($+1.6$ volts), the diode opens. The Q1 base then goes to the $+1$ volt, and the transistor cuts off. The base can go no further positive, so X1 prevents base-emitter breakdown of Q1 from excessive reverse potential of the input pulse. The leading edge of the input pulse opens the diode as soon as it reaches $+1.6$ volts, and the duration of Q1 cutoff is determined by the C-R1 time constant.

Now what is the peak-to-peak amplitude of the output pulse? When Q1 is conducting, it is obviously in saturation, since the ratio of R1 to R_L is only about 6. You also know that when X1 opens, Q1 is cut off. So *if* you ignore any succeeding stage being fed by Q1, the pulse amplitude across R_L is from zero (saturation) to -20 volts (cutoff). But there is only one nonvariable here! If the transistor feeds the base of another transistor, it may be clamped at some point below the -20 volts. So the only nonvariable is that when Q1 is saturated, the collector will be at essentially zero volts. This results from the fact that the emitter is returned directly to ground (no emitter resistor), and there is negligible voltage drop across the saturated transistor.

A12-3. $T = 1/f = 1/4(10^6) = 0.250$ μs. But this is the period of a *complete cycle* at 4 MHz. In the circuit of Fig. 12-4, the positive alternation is damped out, so you have a pulse width of 0.125 μs (see Fig. B-10).

A12-4. In addition to the "memory capacitor," flip-flops and Schmitt triggers, since their state depends upon a previous condition, are memory circuits.

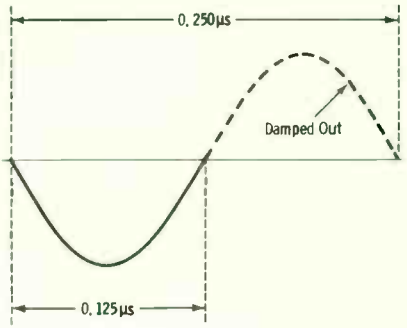


Fig. B-10. Solution for Q12-3.

CHAPTER 13

A13-1. The feedback power less the feedback-network attenuation.

A13-2. An unvarying dc supply.

A13-3. Collector-to-emitter capacitance (C_{CE}).

A13-4. An increase of collector voltage decreases C_{CE}, so the resonant frequency increases.

A13-5. Increased emitter voltage increases the barrier capacitance, so the resonant frequency decreases.

A13-6. Feedback attenuation will *decrease* as more sections are added.

A13-7. No. But opening C2 would permit collector-voltage variation to have a much greater effect on oscillation-frequency stability.

A13-8. The dots indicate the "in-phase" ends of the coils. Thus the placement of the dots at opposite ends indicates the secondary winding is 180° out of phase with the primary. Therefore the phase reversal in the common-emitter circuit is cancelled so that the action is regenerative.

A13-9. Beta times as great.

A13-10. To neutralize the effect of collector-base capacitance.

CHAPTER 15

A15-1. The circuit of Fig. 15-14A represents an AND circuit. Both switches must be closed to supply the load. The circuit of Fig. 15-14B represents an OR circuit. Closing either switch energizes the load.

A15-2. You should see that both Q1 and Q2 are cut off in the absence of an input signal (no forward bias supplied). So the output is at the plus supply potential. But application of a positive pulse at *either* input will cause that transistor to conduct. The output goes toward ground. So the circuit is a NOR circuit, and does not strictly correspond to either Fig. 15-14A or Fig. 15-14B.

A15-3. The circuit corresponds to Fig. 15-14A. Both Q1 and Q2 are saturated in the absence of input signals. So the output is essentially at ground potential. Application of just one negative input will drive that transistor off, but the opposite transistor is still shorting the output to ground. So *both* inputs must go negative simultaneously to drive *both* transistors to cutoff. The output then goes to the full negative potential of the supply voltage. This is an AND circuit.

A15-4. The time constant of $C1R_B$ is 10 μs, so you have a short time constant compared to the input pulse. The output pulse width is approximately $(0.7)(10) = 7$ μs. The leading edge will occur coincident with the leading edge of the input pulse (no delay, phase inversion).

A15-5. The output pulse width is approximately $(0.7)(5) = 3.5$ μs. The leading edge of the output will occur at the *trailing* edge of the input pulse (pulse delay, no phase inversion).

A15-6. (A) If the switches are normally open, closing either switch alone will not close the circuit, since the opposite series transistor is still nonconducting. Therefore this is an AND gate with phase inversion, so the proper name is a NAND gate.
(B) If the switches are normally closed, both transistors are in saturation. The output is essentially at ground potential (minus the slight voltage drop across Q1 and Q2). Now opening either switch will open the circuit, and the output goes negative (full −10 volts). So this is an OR gate with phase inversion; the proper name is a NOR gate.

A15-7. (A) If the switches are normally open, closing either switch will change the gate from a 0 to a 1 state. So this is an OR circuit with phase inversion (NOR gate).
(B) If the switches are normally closed, opening either switch alone still leaves the opposite parallel transistor conducting in saturation. It is necessary to open *both* switches to change the state. Therefore this is an AND gate with phase inversion (NAND gate).

A15-8. The NAND and NOR designations would not be changed.

A15-9. Total division is $2^n = 2^3 = 8$, so the output is $240/8 = 30$ pps.

A15-10. Total division $= 2^n - 2^{p1} - 2^{p2}$

$= 2^3 - 2^0 - 2^1$

$= 8 - 1 - 2$

$= 5$

A15-11. $H = ABC\ (\overline{E + F + G})$ This reads: "H equals A and B and C and not E and not F and not G." The parentheses group the OR inputs, and the bar over this group NOTs the group.

A15-12.

AND

A	B	C	D	H
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Note that the truth table starts with binary number zero (0000) and increases by adding 1 each time until the number 15 (1111) is reached. This assures that no combination is omitted.

A15-13.

OR

E	F	G	OUT TO Q1 BASE
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

A15-14.

NOT

INPUT	OUTPUT
1	0
0	1

A15-15. You should recognize this is a NOR gate (OR gate with phase inversion). The symbol is shown by Fig. B-11. The circle at D indicates output at logic zero when input is logic one.

Fig. B-11. Symbol portion of A15-15.

A15-16. This is a NOR circuit preceded by NOTs, so the truth table is:

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Note that when you have inverted inputs to a NOR gate, the combination becomes an AND gate.

A15-17. In Fig. 15-20A is the schematic of a reset-set (RS) flip-flop. Fig. 15-20B is the symbol for this flip-flop. With a positive pulse applied to the set (S) input, Q3 saturates, shorting the Q1 collector to ground. Then the Q2 base is returned to ground, and Q2 is cut off. The Q2 output is X, or logic 1, while the Q1 output is $\overline{X}$, or logic 0. A positive pulse at the reset (R) input reverses the mode of operation. Note the difference between the RS and the JK flip-flop.

A15-18. No. A reset pulse can be made to coincide with the binary equivalent of an odd number, restarting the count to obtain division by an odd integer.

CHAPTER 16

A16-1. I_z should be at least 10 percent of the load current.

A16-2. Power $= (V_z)(I_z) = (10)(100) = 1000$ mW $= 1$ watt.

A16-3. $I_{z\,max} = \dfrac{\text{Power Rating}}{\text{Operating Voltage}} = \dfrac{0.5}{10} = 0.05\text{A} = 50$ mA.

A16-4. The power dissipated is the voltage drop across the transistor times the current drawn through it (load current plus base current). So:

$$P_d = (12)(0.1) \text{ approx} = 1.2 \text{ watts (approx)}$$

The assumed 10-mA base current is considered negligible.

A16-5. Normal operation would not be affected, but protection against a shorted load would not exist. (Review text if this is not clear).

CHAPTER 17

A17-1. Notice that this question designates a signal voltage, not current. The minimum forward bias would necessarily be 50 mV to prevent the signal from reverse-biasing the input junction, resulting in signal clipping. Also notice that this question is a loaded one. The 50-mV minimum value of bias is simply that which would *prevent distortion*. You would expect considerably more bias than this for a 100 mV input signal, particularly in the small-signal mode of operation.

A17-2.

$I_E = 10/2k = 5$ mA, so
$Z_{in} = (26/5 + 4) = (5.2 + 4) = 9.2$ ohms
$Z_L = 3.3k$ (approx). This is 10k in parallel with 5k.
$A_i = \alpha = 0.99$
$A_v = 3300/9.2 = 360$ (approx)

A17-3.

$Z_{in} = 330$ ohms (approx)
$Z_L = 500$ ohms
$A_i = \beta = 50$
$A_v = 76$ (approx)

A17-4. $I_E = 4$ mA
Internal Output $Z = 8$ ohms (approx)

A17-5. $A_v = 10$ (approx)

A17-6. Minority.

A17-7. Because it has about the same amplitude regardless of V_{CE}. It is more dependent upon temperature than upon V_{CE}.

A17-8. 100 mW

A17-9. The transistor is cut off (no drop across R_L).

A17-10. The transistor is saturated (fully "turned on").

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