Proceedings of the Fifth Annual *WIRELESS* Symposium

FEBRUARY 10-13, 1997
SANTA CLARA CONVENTION CENTER, SANTA CLARA, CA

Sponsored by
Microwaves & RF and
Wireless Systems Design magazines

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Special thanks are due to all WIRELESS authors and presenters, for their extra time and effort in assembling presentations for the Fifth Annual WIRELESS Symposium and Exhibition. While attending their talks, or reading their papers or abstracts in this digest, bear in mind the personal sacrifices that they made to assemble data and complete their presentations in time for this conference. In a field where time to market is everything, these men and women have taken time out of their busy schedules to contribute to the success of the WIRELESS Symposium.

Gratitude is also due to all WIRELESS Program Chairpeople. Their support, guidance, and help have improved the technical quality of the WIRELESS Symposium year after year. Their willingness to guide each session with experience and wisdom helps makes the WIRELESS Symposium and Exhibition a unique experience for attendees and exhibitors alike.

Our thanks are also offered to all of you who have taken time from your work schedules to attend the Fifth Annual WIRELESS Symposium and Exhibition. Your continued support and appreciation for this conference make the year-long efforts worthwhile.

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RFID/AUTOMOTIVE

RFID/Automotive Applications

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Security Applications of RFID

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Some background

The first security application of RFID was the IFF, or Identify Friend or Foe transponders which allowed allied forces to determine if incoming airplanes were friendly or enemy aircraft.

By the 1970's, government agencies experimented with methods of identifying objects and personnel in nuclear facilities. Los Alamos Scientific Labs (LASL), was apparently one center of this activity. In the late 70's, this technology was transferred to the private sector with Amtech and Identronix Research independently developing commercial applications in the 900 MHz spectrum.

By 1980, these companies had taken different paths with Amtech sticking with the original "modulated backscatter" technique and Identronix pursuing a "modulated harmonic" technique as a less efficient method but one having far less nulling problems. Both companies pursued transportation uses of RFID but Identronix (IDX, Inc.) also pursued use of RFID to identify stock animals and for industrial uses (1).

These early efforts resulted in systems which by the mid 80s had ten to one hundred foot range at speeds up to 120 MPH and data lengths up to 8K bytes. Versions had been developed with Read Only, Re-programmable, and full Read - Write capability.

Kinds of Security Applications for RFID

The basic areas where RFID is used for security include:

- Access Control
- Automatic Toll Collection
- Emergency Response
- Home Incarceration
- Keyless Entry
- Patient Monitoring / Security
- Theft Protection
- Personnel Monitoring
- Pet Identification

Access Control

Access control can include parking structures and lots, buildings, and secured or monitored areas. Ease of use of such a system may determine its effectiveness since, in general, people are also part of the formula. Their perspective on how much of a "nuisance" the system presents may determine its acceptability and thus affect its performance.

The best system is a totally "hands off" system which requires no action by the user. If the card access to a parking lot requires leaning out the window of the vehicle in the middle of winter in North Dakota, it is not as "acceptable" as one which merely requires placing the card inside the car window then just driving through the barrier at a normal speed. In fact, many such systems provide a tag which can be "permanently" attached behind the rear view mirror or in the bottom, driver's side of the front window

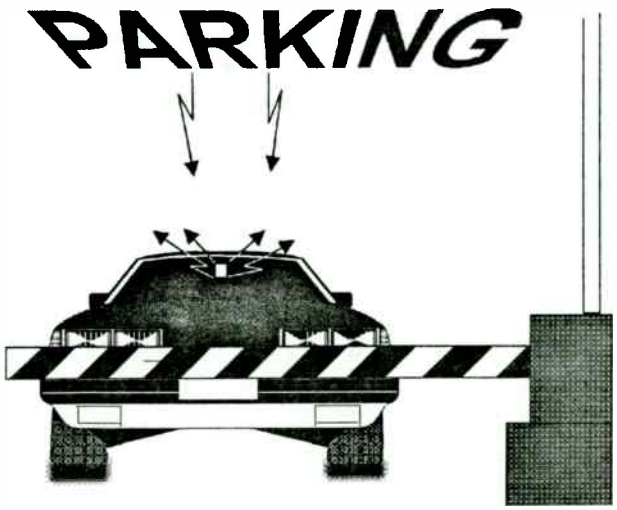


Illustration 1. Gate Access

In one sense, the highway RFID systems are also a kind of security system though the main emphasis is on automatic toll collection rather than access control. Only those vehicles having the appropriate "tag", after all, can bypass the usually slow manual toll booths and zip through special automatic toll collection lanes which allow passage at 45 to 60 MPH without even slowing down.

An interesting problem for multi-lane use of RFID tags for this purpose is how to distinguish tags located in adjacent lanes. UHF signals can be made directional, but they can't be made to have no nulls or reflections. This might cause reading a tag in an adjacent lane. If full coverage of Lane 2 is required, some coverage, however spotty, is likely to occur in Lanes 1 and 3.

Keep in mind that a vehicle passing a read site at 60 MPH is traveling 88 feet per second so that a 100 millisecond transaction would require perfect reception over an 8.8 foot window. Any UHF signal covering this long a window is quite likely to cover up to three times this far in directions of enhanced reflections if set up to read through expected nulled signal levels. Spread Spectrum and/or spatial or polarization diversity may improve this, but lane to lane "leakage" is still quite likely.

Of course, transaction times may be much less than 100 milliseconds at UHF, but antenna to vehicle distance will still need to be long enough to completely cover the lane being covered so that the problem would exist regardless of the transaction time requirement. UHF rf has no "brick wall".

Illustration 2. Multiple Lane Automatic Toll Collection

Amtech has a patent on one method to overcome this problem. They bury a VLF loop in the roadway in each lane. This loop transmits a unique lane identification code continuously. This code is picked up by the vehicle as it passes over the loop and is added to the tag information so that the lane number becomes part of the data transmitted during a normal UHF transaction. Thus a UHF antenna on an adjacent lane may interrogate the wrong tag, but the identification code won't match the lane so that such responses will be ignored (2).

Since the VLF loop can be driven with fairly high power, reception by the tag is much more likely than reception of a VLF tag's much weaker return signal if used in the usual transponder fashion. Furthermore, the data rate required to pass a short lane ID number is much lower than that required for the usual toll collection transaction so that reception is assured even at high passing speeds. The VLF transaction will not require an impracticably large loop antenna in order to provide a large enough window to pass the lane code.

Representative vehicle access control systems are offered by Amtech, TIRIS, Indala/Motorola, and ISD LTD (Australia).

The general technique of pairing VLF with UHF has been used elsewhere to work around other limitations each frequency band presents by itself.

While VLF has excellent capability to limit radiation and pickup to a very controllable area, it lacks the distance capability often required for many applications. It also is prone to noise interference and has limited data rate capability due to its low carrier frequency.

UHF, on the other hand, can operate over hundreds of feet in some cases with very high data rates, but it is also much more difficult to control in terms of trying to establish coverage up to but no further than some arbitrary "brick wall" due to reflections, multipath nulling, and the far field 20 Log (Distance) nature of VHF and UHF propagation loss.

Chart 1: VHF versus UHF Characteristics

SPECTRUM CHARACTERISTICS

Band	VLF	HF	VHF	UHF	uWAVE
Data Rate	Low	Med	Med	High	Very High
Noise	High	Med	Low	Lower	Negligible
"Skip" Interference	None	High	Tropo	None	None
Absorption	Low	Low	Med	Med	High
Reflection	None	Low	Med	Higher	High
License Required	No	Y/N	Y/N	Y/N	No

Amtech has systems operating up to 2450 MHz for highway, rail, and containerized cargo use. They provide both bumper and window mounted versions of their tags for vehicle use. For containerized cargo, Amtech produces a dual mode tag offering the better performance of 915 MHz operation in those countries which allow it but also providing the more universal 2450 MHz frequency for countries where 915 MHz is not available. They have passive (batteryless) versions which achieve interrogation ranges up to 18 feet and battery powered tags usable to 300 feet. These longer ranges are at Automatic Vehicle Monitoring (AVM) levels, however, not the much lower Part 15 levels (3).

Texas Instruments also provides a variety of VLF through UHF tags under the general heading of Texas Instruments RF Identification Systems or TIRIS(TM). Toll collection versions of these can also be window or bumper mounted, depending on the application (4).

Indala, another of the early VLF RFID companies, has become part of Motorola and offers systems useful for access control as well as industrial control applications (5).

These systems fall under the general heading of ITS, or Intelligent Transportation Systems which utilize a variety of technologies to provide intermodal operation of vehicle transportation whether by car, truck, rail, or ship (6).

Integrated Silicon Design, Limited (ISD, LTD) of Australia provides a variety of RFID products including both vehicle and personnel access control as well as anti-theft "tags" for cars. Car theft is a big problem in South Africa, for example, where vehicles are stolen then taken across the border into neighboring countries for re-sale. Some of the techniques used for these applications were explored in a paper delivered at the Wireless Symposium in March of 1966 for those who wish to find out more (7).

Ticket Collection

Ski operators have begun to use VLF RFID to provide lift "tickets" which provide hourly, weekly, or seasonal access depending on the balance stored in the tag. Theme park operators and transit systems have also used RFID as one means of access to rides. RFID, unlike bar codes and magnetic stripe cards, is much harder to "clone" and provides "contactless" access.

While magnetic stripe cards and various contact versions of smart cards can also be used for these applications, contactless rf based systems can provide more convenience to someone wearing ski gloves at an access gate and reader site where ice may form or snow be blowing around.

Generally these systems are either VLF or HF and have a read range under one foot.

An interesting, recent use of RFID for security purposes was in "multimedia" badges used during the Summer Olympics. These provided picture, bar code, magnetic stripe, and RF identification to validate identity for athletes, coaches, officials, journalists and dignitaries. Another RFID "tag" was used with long distance runners to track them as they passed various check points. While the final tally of race times did not use this information exclusively, use of the RFID tag helped communicate the progress of individual runners throughout the event.

The City of Atlanta also used RFID tags from Amtech to monitor check points along the route of the Metropolitan Atlanta Rapid Transit Authority (MARTA) to trigger on board announcements of upcoming stations through their automatic train announcement system (ATAS). This concept was first experimented with by the Toronto Transit Commission (TTC) on subways in 1983 using equipment developed by IDX, Inc. and was also experimented with several years later on Boston's Metropolitan Transit System. Atlanta, however, implemented their ATAS system on all 240 rail cars to provide announcements in several languages in order to meet the needs of foreign visitors to the Olympic games (8).

Emergency Response Systems (ERS)

We've all seen the "I've fallen and I can't get up" commercials. While we sometimes joke about it, help alert or emergency response systems (ERS) are becoming important to a growing number of Americans as "baby boomers" approach an age when they or their parent's continuing independence may depend on just such a system.

ERS is used both in the home environment such as we see in the commercials, as well as in assisted living facilities and retirement communities. In the larger systems, often a means of determining the location of the alarm is provided in addition to the identification of the individual requiring assistance.

The technologies involved include everything from simple, garage door opener style pendant transmitters to more sophisticated spread-spectrum systems such as the Code Alert ERS frequency hopping system. Interface to the public phone system, a paging system, or local area network is commonly part of such systems.

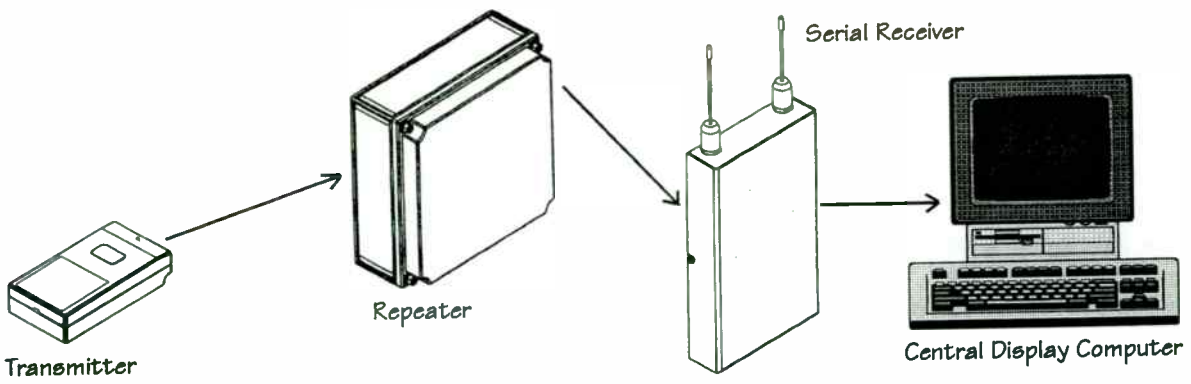


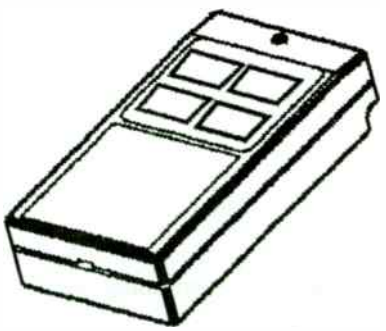
Illustration 3. Code Alert QRS (Quick Response) System:

Campus security is another common use for ERS. Schools, hospitals, and business campuses are not always as safe as we'd like them to be so that ERS provides an extra measure of security and confidence to employees or students, especially during hours when security is more difficult to guarantee. Generally the system reports not only the number of the alarm device which has been triggered, but also indicates which receiver has received the signal. Determining location is a key element in this kind of system in addition to identifying the person seeking assistance.

An ERS system may also include wireless fire or call box alarms to supplement the personal pendant alarm carried by individuals.

Institutional uses of ERS includes mental facilities, prisons, military bases, or large businesses where guards making the rounds need to report in at call boxes and during emergency situations. The transmitters in these applications usually provide more than one coded signal so that a guard can use one button for checking on or off his shift, another for indicating arrival at a check point, another for non-priority assistance calls and, of course, a general alarm button.

Often this kind of transmitter is worn on a belt clip and has both a pull pin and "person down" feature. A pull pin is set up to automatically causes an alarm if someone pulls the transmitter away from the guard thus triggering the alarm. The "person down" feature uses a tilt switch to indicate that a guard has been knocked to the ground.



Pendant style Transmitter

Help Alert
Man Down Transmitter

Illustration 4. ERS System Equipment

Some companies supplying equipment in the ERS area include Code Alert (RFT), Innovonics, Visonic, and Linear. One major distributor of such equipment is ADI of Syosset, New York (9).

Home Incarceration

About 20 years ago, my chief engineer at the time was involved in a consulting job for a group in California who were developing a method of "tagging" prisoners. The concept was to attach a secure RF "tag" to a prisoner so that they could serve their sentences for minor offenses at home rather than burdening the already overcrowded prison system. Since that time, more and more states and local governments have sought to use this approach to reduce the economic burden on the taxpayer of adding even more prison space to already expensive corrections systems. Home incarceration for non violent offenders is one way to do this while still providing effective deterrents to crime.

Today these systems haven't changed much in concept, but the materials used for the attachment band are much tougher to cut, the interface to the outside world may include a GPS receiver as well as the standard phone connection, and, using the GPS location capabilities, the prisoner may also be allowed to travel to a limited number of destinations such as a place of employment or community service, government offices, parole offices, and so forth. His movements can be tracked all along the way using technologies which weren't readily available in the 1970s.

Some companies involved in home incarceration equipment production include BI and Pro Tech Monitoring (10).

Keyless Entry

Time was that the only way to get into your car was to turn a key in a lock. That's a simple enough operation, but it becomes more difficult when loaded down with bags of groceries or when ice has frozen the lock shut. And, as every repo man knows, it's not that hard to find the right key to open almost any car if you know what you're doing.

Not too many years back high end car makers provided a new option.. keyless entry. The first attempt was to use a keypad, but this proved less than practical in the automotive environment. Aside from requiring someone to remember a combination, environmental factors like ice, snow, dust, and dirt are not conducive to keeping keypads functional when mounted on the outside of vehicles.

Since then, RF "keyless" entry (RKE) based on technology similar to garage door openers have become a standard option for even mid priced cars, vans, and trucks.

Early units typically used 8 bit codes, but it was found that the enterprising thief could merely transmit all 256 possible code combinations in about 30 seconds to open your car door.

Attempts to get around this included delaying the time between allowable retries to 10 or 15 seconds which stretches the time required for entry to minutes instead of seconds. This, however, may make the system less convenient for the legitimate user whenever he doesn't gain entry upon the first try. It doesn't really provide much of a deterrent to a thief, anyway, since he can still keep trying for an extended period of time since he can do so from the relative safety of a location up to 100 feet away from your car.

Raising the number of code bits to 40 bits eliminates the potential for transmitting all possible codes (it would take about 6000 years!), but anything being transmitted 50-100 feet to your car can also be intercepted by someone using a special receiver, stored, then transmitted back after you leave the area.

Many methods have been developed to prevent such "cloning". One is to use a repeating sequence of codes programmed by the user (or automatically by the system). Rolling codes do not use the same code twice in a row to open the car. This helps prevent cloning except by a persistent thief willing to follow you around for several opening and closing cycles.

More secure techniques include reprogramming the key's code each time . Essentially, each time the key is used

it is given a new code either through direct contact or through a VLF pickup coil. The code is changed each time the owner places the key is in the ignition. Thus the next code which can be used to open the door is both placed into the key and remembered by the vehicle's receive decoder. Only that number will open the lock.

An example of this kind of system is the TI Marcstar rolling or hopping code system which "hops" randomly to a new 40-bit code with each use. The system can make more than 1-trillion different code combinations which will not be repeated during the entire lifetime of the vehicle. Provision has also been made to track up to 4 different validated users so that mom, dad, junior, and sis can all use the vehicle with their own unique code transactions but still not repeat any code combination! **(11)**

Other companies offering this kind of chip include EXEL and MICROCHIP **(12)**.

Wanderers

As the population ages, and life expectancies increase, dementia, Alzheimer's Disease and other problems of the very old are becoming much more common at the same time that we are trying to cut back on the cost of long term healthcare by reducing nursing home and group home staffing. Just one or two residents who tend to become disoriented and wander off can create major problems for such facilities. If the facility is located near a major road, in rough terrain, near a lake or swamp, or in an area of bitter cold winters, wandering residents could face serious consequences or even death, not to mention that the health care providers would face severe liability in such a situation.

For quite a few years, companies like Code Alert have provided Low Frequency radio frequency transmitters or transponders to prevent monitored individuals from getting out of a facility without setting off a warning alarm. VLF is usually used to provide a signal which is harder to block than VHF or UHF signals and because VLF doesn't have the nulling and reflection range enhancement problems of the higher frequencies.

If you are picking up a VLF signal, it is very likely that it is less than 10 feet and probably less than 5 feet from the antenna picking it up. At the same time, there is little likelihood that there will be a signal "hot spot" located 15 or 20 feet in front of the door or exit. With VHF or higher frequencies, localization and control of undesired "hot spots" is much more difficult even when using diversity techniques.

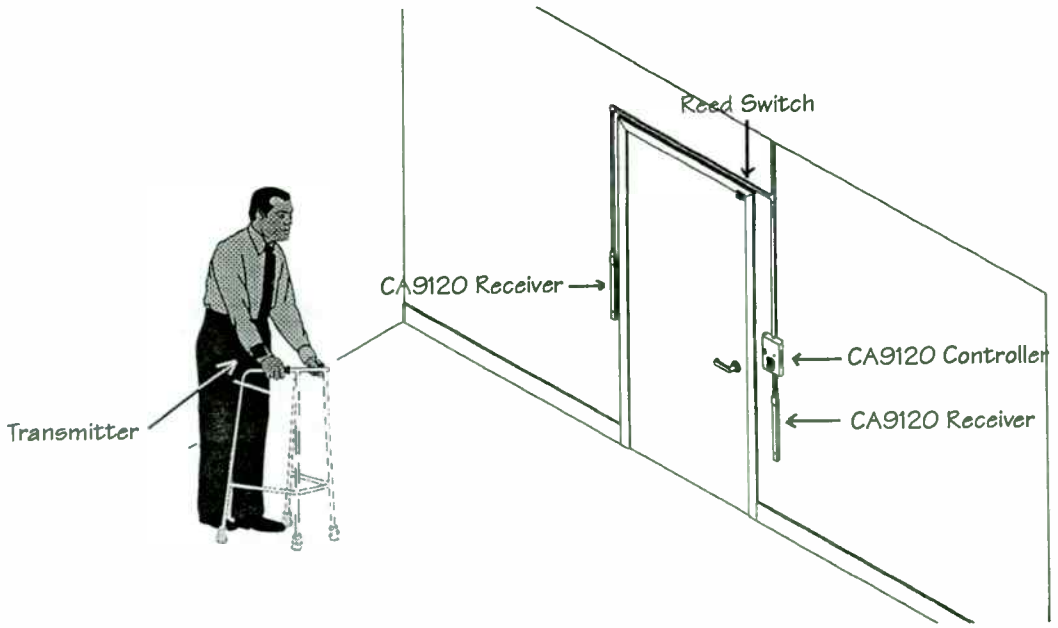


Illustration 5. Code Alert CA9120 System

Restricting and controlling pickup is important for one other reason. Residents inside of a facility should be allowed to have complete freedom of movement. It is only when they go through an open exit door or are close to an exit door which is already open that an alarm should sound. At all other times, alarms should not occur. In particular, nuisance alarms should not occur when the resident is 15 or 20 feet away from a door when someone else opens it to go through! We do not want to create a "boy who cried 'wolf' " atmosphere by having too many false alarms.

Illustration 6. Out of Ranger

Many wanderer monitoring systems actually cause a closed door to magnetically lock whenever the monitored resident gets close to it. This prevents them from opening the door. If a monitored individual is 10 feet away from the door, however, we would certainly not want the door to lock down for staff, visitors, or other residents who might want to use it.

There are, of course, NFPA fire safety regulations concerning use of magnetic locks which require that steady pressure applied to the door for more than about 15 seconds will automatically release it. Fortunately, most wanderers will give up long before that amount of time making the system effective in preventing instead of just alarming on wandering incidents.

Some wanderer monitoring systems also provide a UHF "supervision" signal which is used as a check to regularly report the continuing presence of the individual within range of the monitor receiver(s). It also reports status of the transmitter such as "low battery" and may indicate that the band holding the transmitter to the individual has been cut or removed.

Use of the UHF signal allows longer range tracking to help find an individual if they should manage to get out of the facility undetected or wander far enough away to become "lost" before staff can respond to an alarm. VHF or UHF has the range required to provide several hundred feet (some as much as a half mile) when ground based equipment is used but can provide up to a couple of miles using an aircraft.

Various out-of-range schemes have also been developed to monitor a moderate sized zone to allow an Alzheimer's patient freedom of a front or back yard or within a preset distance in a park during an outing yet alarm if the monitor signal is lost if the individual wanders outside the coverage area. Tracking equipment can then be used to locate the wanderer using directional antennas and full receiver sensitivity.

Infant and Child Security Systems

An unfortunate fact of life in the 1990s is that a number of newborn infants have been abducted from hospitals over the past ten years. While not yet a common occurrence, many hospitals have taken proactive steps to ensure that it doesn't happen in their facility.

At one hospital I visited last year, over 80 nurses were used to fill 8-12 full and part time positions per shift in the maternity ward. This facility had as many as 25 babies on any given day and the typical hospital stay was less than 20 hours, let alone the 48 hours recently debated in Congress! May I suggest that keeping track of infants under these circumstances can be difficult?

There have been a number of methods applied to keep track of infants electronically. Some systems transmit a UHF signal which is totally supervised. If the signal is not picked up for a predetermined period of some number of seconds, it is presumed to be "missing" and an alarm will sound.

If the band of any infant transmitter is cut or removed, the transmitted signal comes on immediately at full strength and changes its transmitted code to indicate a "cut band alert". If the unit's battery becomes weak, a data flag is set in the normal data transmission to indicate that the battery is near the end of its life.

While this kind of system is "fail safe", that is, any fault will cause an alarm, it also can be subject to a great deal of "false" alarming.

As discussed earlier, no "brick wall" exists where inside the ward the signal is always heard but outside the ward the signal is lost completely. Determining that an infant is about to be taken out an exit will also be difficult to determine until after the fact.

Even within the desired coverage area there will be nulls and signal blockage, which inside of buildings can be 20 to 40 dB deep.. very hard to overcome using Part 15 power levels, especially while trying to establish reliable coverage only up to a theoretical "brick wall".

At RF Technologies we opted to take a different approach which integrates what we feel to be the best characteristics of both VLF and UHF systems. Our Infant and Child Security System (ICSS) uses a standard VLF wander monitoring transmitter to cover exit alarm functions but provides a wide area UHF transmission if the attachment band is cut or removed.

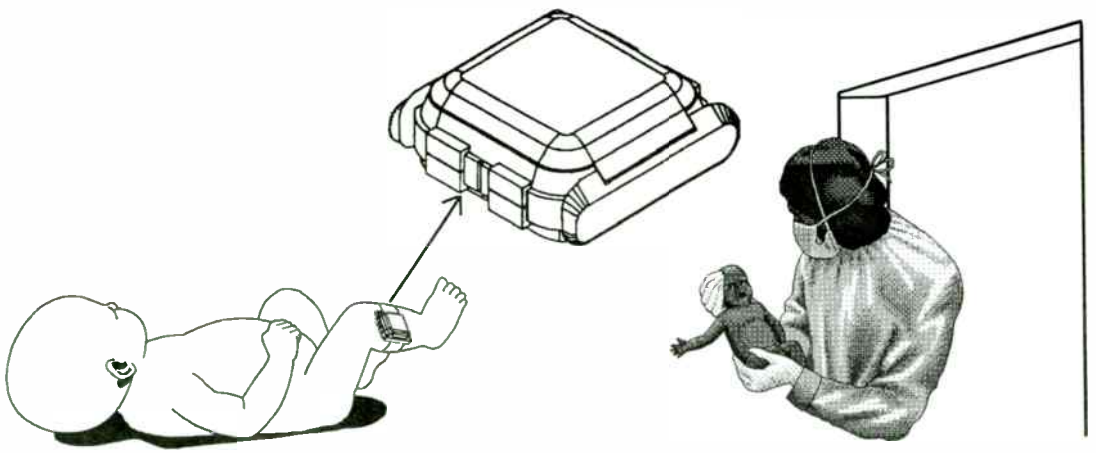


Illustration 7. Code Alert ICSS Diagram

The UHF signal is received by a multiple diversity arrangement of many receivers so that an abductor cutting the band while trying the block the signal will have a difficult time doing so. The receivers form sort of a reverse cellular system with many intentionally overlapping "cells" to provide the ultimate in diversity reception.

There is, of course, no perfect security system, but ICSS provides one more level of protection to aid in the multiple level security approach demanded by today's world. An ICSS installation should never take the place of staff vigilance, but it can provide a valuable addition to efforts to improve security.

Theft Protection

We've all see the theft prevention systems in our local malls and retail stores. A variety of techniques have been used to detect items leaving a store without benefit of purchase. Some of these systems use magnetism. Others use a printed coil and paper capacitor which resonates when passing through the alarm portal thus setting off the alarm. If the item has been purchased, however, sufficient voltage is applied to the "capacitor" to blow it apart which makes the tuned circuit non resonant.

Still other systems look for the harmonic or "backscatter modulation" generated or enhanced by a passive "tag" when it passes between the system's antennas.

All of these systems are, in effect, "one bit" systems. The signal, harmonic, resonance, magnetic flux change, or whatever detection scheme being used is either present or absent.

Simple systems of this kind are only about 90-95% effective in detecting theft but the tags are also very inexpensive. Given the relative low cost and the reusability of many of these tags, these system are quite adequate to reduce losses to the retailer. These systems also have a deterrent effect on all but the most persistent shoplifters.

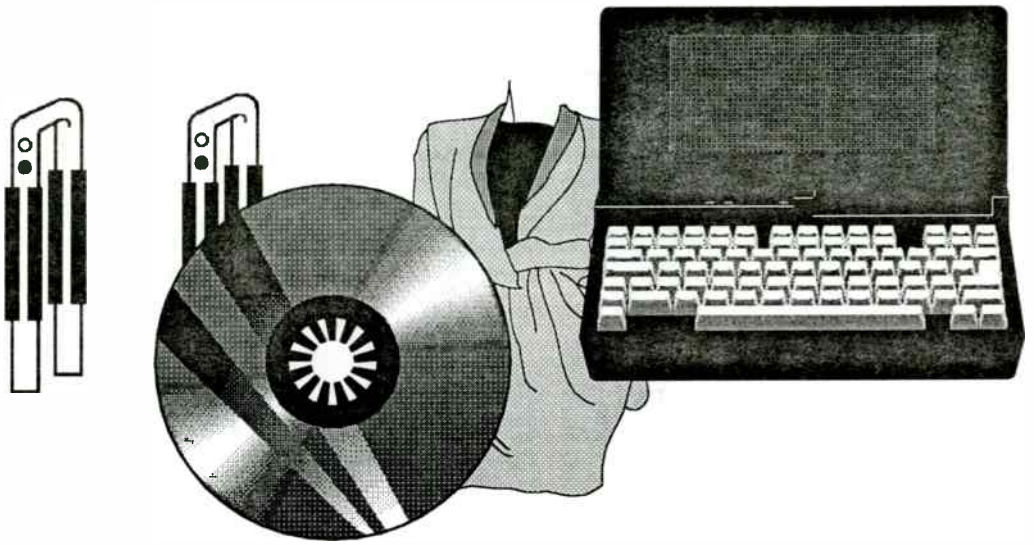


Illustration 8. Store Theft

Another area of growing concern is the theft of high tech equipment from businesses. A common target is the laptop computer. Some businesses are using RFID tags to not only indicate whenever a laptop passes out of the plant, but which specific laptop. In combination with security check points, cameras, and other techniques, RFID used in this way can provide a level of protection and detection not provided by simpler, "one bit" systems.

Personnel Monitoring

Personnel monitoring involves tracking individuals coming into or leaving a workplace. This may be done for accounting reasons or to provide monitoring of personnel entering secured or hazardous areas.

Typically this is done using a magnetic card reader but some companies are changing to various forms of RFID. For one thing, RFID cards are more difficult to counterfeit than magnetic cards, but a more important consideration is that many RFID cards can be read at a distance of several feet and do not require contact with the reader. Even if two people use one card to get in a door, both can be identified using RFID (assuming both have cards, of course.) This might become critical in a nuclear power plant after an emergency incident to make sure that everyone actually inside the critical area has been evacuated

Some companies have even provided systems which replace the need for a receptionist in businesses which really don't have enough walk in business to warrant hiring one. Anyone who enters the lobby who is not wearing the appropriate "tag" will trigger a normal infrared or other kind of detector so that their presence can be indicated to staff inside the plant.

Company employees, on the other hand, merely need to pass through the outer door, have their "tag" read, then proceed through the inner door. This is particularly useful when employees are carrying equipment or packages making use of a magnetic card reader, keypad, or other traditional entry device inconvenient.

An example of receptionless building access is the 13.57 MHz system offered by ISD of Australia. It uses HF RFID technology using a name tag sized transponder which responds up to 1 meter (3 feet) from the reader. This provides hands free access to the building or secured area.

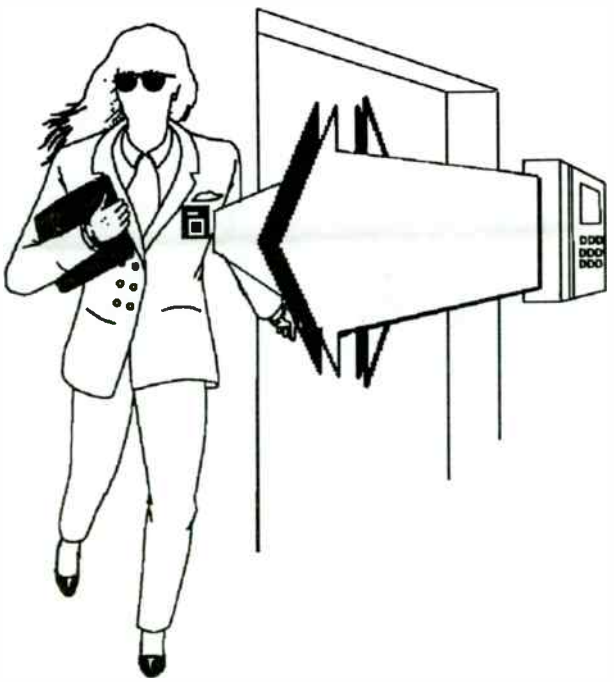


Illustration 9. ISD Building Access System

Pet Identification

Another potentially large use for RFID security tags is to identify pets. In most cases the animal has a sub-dermal implant made of a VLF transponder. While the reading distance of the transponder is only a few inches, most animals like cats and dogs are easily identified since getting close to them is not generally an issue.

One unique application of RFID was to use the "tag" to allow only one's own pet to open a pet door by allowing the door to open only when the pet's tag was present.

AIM, the Automatic Identification Manufacturers (13), has established an RFID specification for small animals. Some manufacturers in small animal I.D. include AVID, Destron, and Info Pet (14).

Summary:

RFID has been applied to widely varying kinds of security applications from simple to complex. Each application has its own special requirements and no "universal" solution exists. Both VLF and UHF techniques have been applied to these applications as well as VLF/UHF, RF/Infrared, and other combinations of complementary technologies.

Notes:

(1) RFID: Spectrum, Applications, and Techniques, J. Eagleson, Proceedings of 4th Annual Wireless Symposium, Santa Clara, February 1996, pp. 310-327)

(2) Patent #5,351,052, Transponder Systems for Automatic Identification Purposes, L. D'Hont, A. Tip, and H. Meier, Texas Instruments, Dallas, TX

(3) Amtech, 17304 Preston Road, Dallas, TX, 1-800-923-4824 (www.asctmd.com)

(4) Texas Instruments, xxx, Dallas ? TX (www.ti.com/mc/docs/tiris/docs/index.htm)

(5) Motorola/Indala, 3041 Orchard Parkway, San Jose, CA 95131 408/369-4625 (www.mot.com)

(6) "Intelligent Transportation Hits the Road", Electronic Design, Oct 14, 1996, pp. 91-102)

(7) Michael Loukine, "Integral Backscattering Transponders for Low Cost RFID Applications", Proceedings of Wireless Symposium, Santa Clara, February 1996 pp. 328-336)

(8) ADC Goes for the Gold", Paul Quinn, ID Systems, August 1996, pp. 32-38)

(9) RF Technologies (Code Alert), 3125 N 125th Street, Brookfield, WI 53005, 1-800-669-9946 (www.execpc.com/~rftech)

Visonic, Linear, and Innovonics equipment is listed in the ADI catalog, 180 Michael Drive, Syosset, NY, 11791, 1-800-441-4130 (www.adilink.com)

(10) BI, Inc., Boulder, CO Fax 303/530-5349, Voice 1-800-241-2911, Pro Tech Monitoring, 1211 N Westshore Blvd., Tampa, FL 813/286-1038 (http://www.ptm.com)

(11) www.ti.com TRC1300 and TRC1315, TRF1400

(12) Exel, Inc., 2150 Commerce Dr., San Jose, CA 95161, 408/432-0500 (www.exel.com)

Microchip, 2355 West Chandler Blvd., Chandler, AZ, 602/786-7200 (www.microchip.com)

(13) AIM USA, 634 Alpha Drive, Pittsburg, PA, 412/963-8588 (www.

(14)Avid, 3179 HammerAve., Norco, CA 91760 1-800-339-2843 Destron, Electronic ID, Inc., 131 East ExchangeAve., Suite 116, Ft. Worth, TX, 1-800-842-8725, (www.dfw.net/~tqg/electonicid)

InfoPet, 415 W. Traveler's Trail, Burnsville, Mn 55337, 1-800-463-6738

Some Internet Web sites about RFID:

http://www.execpc.com/~rftech

http://rapidttp.com/rfid/

http://www.microcomcorp.com/rfid.html

http://www.com.au/intag/index.html

http://ilab.com/prosp43.htm

http://www.hotsites.net/allflexusa/earvsimp.html

http://www.psmfc.org/pittag/animlid.htm

http://www.id-tech.com/freebie.htm

http://www.eleceng.adelaide.edu.au/Personal/dhall/isd.htm

http://www.datalogic.com/index.htm

http://www.datachip.com/overview.html

http://info.pix.za:80/0/business/rfid/supertag.html

http://balogh-group.com/

http://www.flexnet.com/GTL/sirit.htm

http://www.ptm.com

http://www.versanet.com/infonet/index.html

http://www.futureone.com/microchip/pressrel/keeprin.

http://village.ios.com/~mkolb/avi.html

http://dot.ca.gov/hq/traffops/elecsys/title21

http://www.aiag.org

Wireless Vehicle Identification with Early Detection: An Alternative to Traditional Toll-Collection Methods

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ABSTRACT. Wireless Vehicle Identification (WVI) offers an alternative to traditional toll-collection options. An early warning system (EWS) identifies and preprocesses all approaching vehicles, allowing them to pass through a toll lane without stopping. As vehicles approach a toll plaza, all vehicle-based transponder units wake up, execute a listen–transmit anticollision algorithm, and communicate their identification number to the EWS. Each patron's eligibility status is determined and communicated back to the appropriate transponder, allowing sufficient time for drivers to make any necessary lane changes. As vehicles pass an in-lane reader, the appropriate toll is charged to the driver's account.

1. Introduction

The $480 billion global telecommunications market is estimated to grow to $1.2 trillion over the next 4 years, with 70–80% of that growth coming from the enhanced services segment, largely composed of wireless services [8]. Highway toll-collection systems are just one of the enhanced services areas actively being explored for the uses of wireless communications.

Traditional toll-collection systems are dependent on humans and thus are subject to human error. Further, existing systems require each vehicle to come to a complete stop to pay the toll. These mandatory stops often result in a significant bottleneck at toll plazas. The processes of making change and issuing receipts only worsen the problem.

Several states have recognized the potential benefits of applied wireless technology and implemented automated toll-collection systems on major roadways. Several of these systems are based on designs that allow only a single opportunity to detect and charge the driver; this usually occurs as the vehicle passes by an in-lane detector. Other systems have maximum speeds as low as 10 mph, and minimum speeds as low as 0 mph (*i.e.*, a complete stop). The authors personally experienced multiple vehicle detection failures with one of the existing systems, while obeying posted speed limits. Such systems may be failing to collect thousands of dollars per year in tolls.

The next generation of wireless identification systems will most likely use early detection methods to provide ample time for vehicle identification and toll assessment.

2. System Overview

The Wireless Vehicle Identification (WVI) system was developed to provide a highly accurate, secure, and automated alternative to traditional toll-collection options. The system was designed to detect and charge vehicles that pass through plaza toll lanes at speeds of up to 100 mph.

WVI includes an Early Warning System (EWS) that determines each patron's eligibility status as the vehicle approaches within 1000 ft of a toll plaza. The status is relayed to the patron so that any necessary lane changes may be made before passing through the toll lane.

The WVI system charges an appropriate toll based on the vehicle class. A monthly statement detailing all account activity is mailed to WVI patrons.

Net throughput depends on peak data rate and latencies attributed to medium access control (MAC) scheme, retransmission due to data packet collisions, and other data packet efficiencies. Moreover, net throughput and peak rates are meaningless unless the physical layer is reliable and robust to noise [1].

3. System Components

The WVI system comprises the EWS, vehicle-based transponders, and one in-lane reader for each lane of traffic.

The EWS is made up of a 9-dB directional gain, corner reflector, extended range 900–960-MHz dipole antenna, with a 25-dB front-to-back ratio to reduce interference, and a land-based computer with custom software and hardware.

The transponder, located in the vehicle, is a battery-operated RF transceiver, with audio and visual status indicators and additional circuitry.

The in-lane reader consists of a short-range, 900–926-MHz dipole antenna, an AC-powered Superhethrodyne FM receiver, an FM 915 MHz transmitter, and additional circuitry.

4. System Operation

The early warning system antenna sends an ENQuiry command to all transponders in the area. As vehicles enter zone 1, which is normally 1000 ft before the toll plaza, but can be any reasonable distance of similar magnitude (Fig. 1), each transponder in the zone wakes up and processes the test signal. If the EWS antenna is determined to be the source of the signal, then both the EWS antenna and the transponder communicate by way of a custom-designed listen–transmit algorithm (LTA) [9].

After performing a check of the account information, the land-based computer (part of EWS) determines whether each patron is eligible to continue through to the express lane(s). The appropriate status is communicated back to each transponder, allowing sufficient time for patrons to make any necessary lane changes. The vehicle identification numbers (VID) and account status are simultaneously sent to all in-lane readers; thus the system knows the identity of, and is ready to process, all approaching vehicles. As vehicles pass a reader, the appropriate toll is charged to the patron's account.

5. System Design

5.1. Transponder. The vehicle-based transponder is a small, battery-operated unit that is composed of a 915-MHz transceiver, a digital microprocessor with nonvolatile RAM, and a power-management circuit.

5.1.1. Sleep Mode. To conserve battery power, the unit operates in a sleep mode and remains there until energy is detected in the 906-926 MHz range. Upon sensing the energy, the unit will wake up and execute a self-test to verify that the receiver, transmitter, and memory are operational. If the input data contain a valid EWS trigger signal the unit will establish communication with the toll plaza EWS antenna and the unit will emit three beeps to inform the patron that it is awake and functional. If the transponder fails its self-test, the patron is warned not to use the automated toll lane because of an error condition.

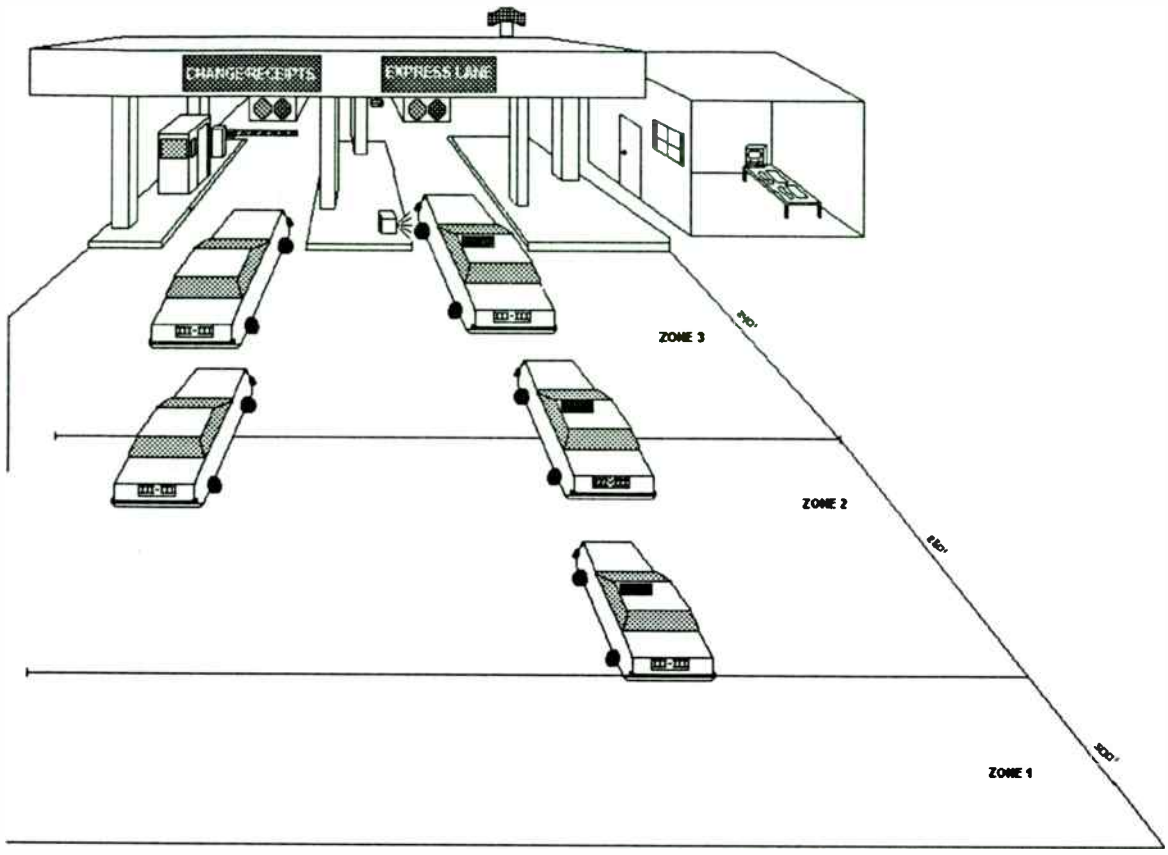

Fig. 1. Schematic diagram of toll plaza with one traditional lane and one express lane. Note that the express lane does not require a barrier. The computer is shown in a room to the right, but may be virtually anywhere. (This diagram is not to scale)

5.1.2. Receiver. A dual conversion, wideband FM (WBFM) receiver is implemented having frequency agility when controlled by a dual PLL synthesizer. A custom-built printed circuit board (PCB) that uses "off-the-shelf" communication surface-mount components. It comprises a PCB trace antenna, two RF filters, a low-noise amplifier (LNA), a two-stage mixer, and a local oscillator (LO) as shown in Fig. 2.

The received signal is captured by the antenna and fed through a RF ceramic bandpass preselector filter centered at 915 MHz. The signal is amplified by a low-noise amplifier (MC13144 LNA) [2] and passed through a second RF ceramic filter. The signal is fed into a single IC (MC13142) [3] that consists of a second LNA, a down-converter, and a voltage-controlled oscillator (VCO). A 1.1 GHz dual PLL synthesizer (MC145220) [4] controls the receiver first LO.

The output of the front-end section, described above, is sent to an 49.83 MHz IF filter (not shown in Fig. 2) and an IF subsystem (MC13158) [5] that consists of a second down-converter, IF and limiting amplifiers, wideband FM quadrature detector, and data slicer. Greater than 50dB second image rejection is provided by the receiver back-end section. Frequency tripling the 13.043 MHz reference crystal oscillator provides the IF subsystem LO (receiver second LO); this eliminates the need for a second crystal source. The dual synthesizer is used to control both the first converter VCO and the transmitter oscillator/exciter (see section 5.1.3). The dual synthesizer is fully programmable via three digital

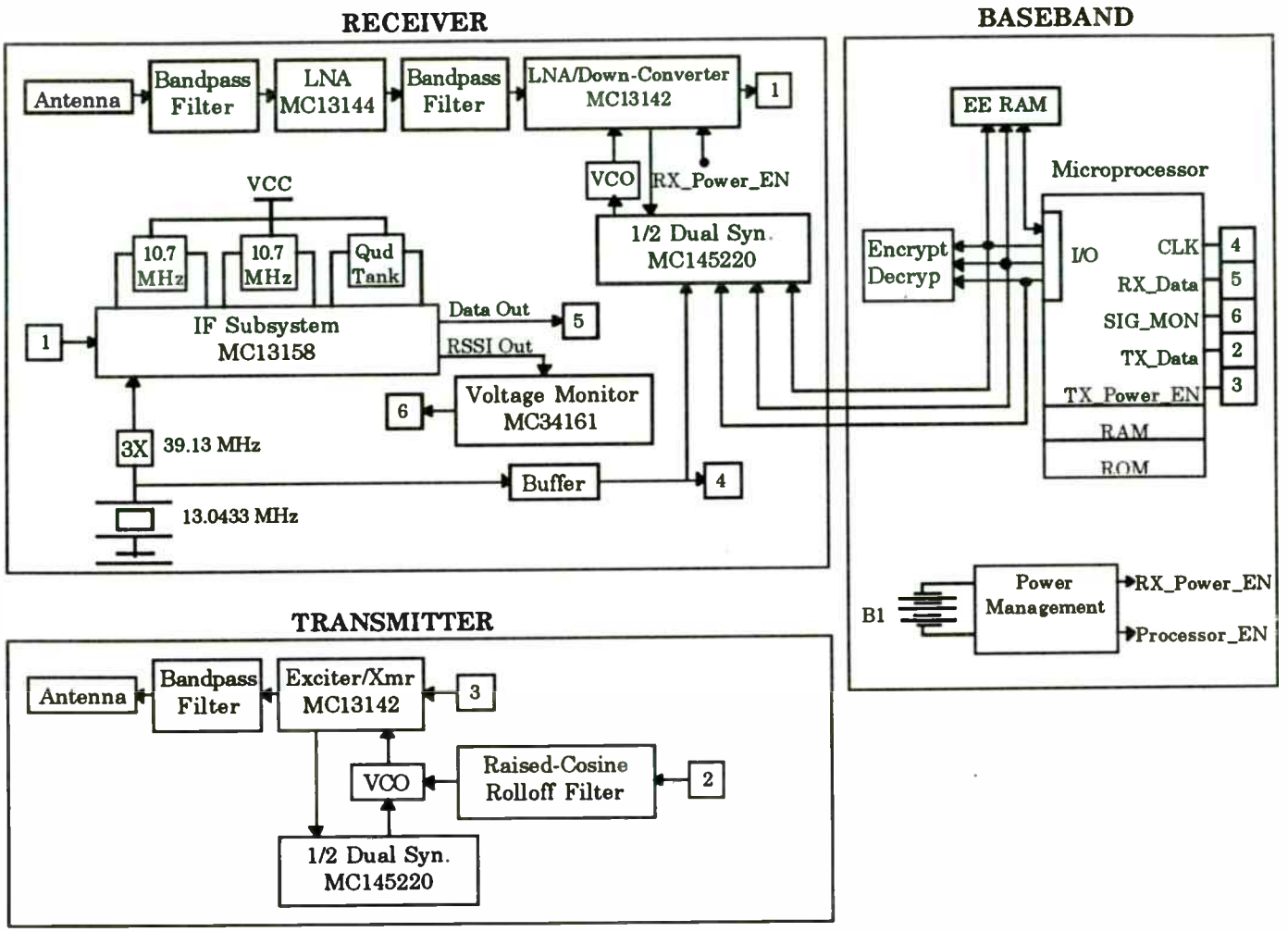

Fig. 2. Component block diagram of the three elements of the transponder unit

outputs from the microprocessor. A data slicer (not shown) converts the analog output into a TTL waveform ready to be fed into the encoder/decoder software module. This design is used to achieve –90 dBm at 110 kbps with a very low error rate. Higher data rates of 300kbps are achievable but cost is significantly higher.

5.1.3. Transmitter. The transmitter converts the vehicle identification number into an FM signal. To limit transmission bandwidth, a baseband data stream signal is routed from the microprocessor through a raised cosine-rolloff premodulation filter. The output of the filter is then fed into a VCO/exciter (MC13142) [4] where is modulated unto the 915 MHz carrier. The wideband FM signal is filtered by a 915 MHz RF ceramic bandpass filter and radiated by the PCB trace antenna.

The radiated power and harmonic content of the signal meet the criteria specified by the FCC in the Code of Federal Regulations (CFR), Title 47, Part 15 [6]. This system is designed for half duplex operation; both the transmitter and receiver are at 915 MHz and have their own trace antennas. Both transmitter and receiver are shut off independently.

5.1.4. Baseband. The baseband unit consists of an RISC processor with external nonvolatile RAM and rolling code encryptor/decryptor (XL107) [7]. The baseband is designed as a state machine for throughput and cost effectiveness. The baseband microprocessor performs the Manchester encoding and decoding and the serial communication with the EWS computer. The processor communicates with the EWS computer by using two additional digital I/O pins to transmit

and receive data. Nonvolatile RAM stores the rolling password and vehicle identification number.

5.2. Early Warning System.

5.2.1. Receiver and Transmitter. The EWS receiver and transmitter circuits are similar to those shown in Fig. 2 . The main difference is that the EWS uses a directional gain, corner reflector, 900 MHz dipole antenna instead of a PCB trace antenna

5.2.3. Baseband. The baseband unit consists of an 8 bit microprocessor, memory buffer, and a high speed serial port capable of transmitting up to 300kbs. The microprocessor communicates data from the computer to the transponders and from the transponders to the computer.

5.2.3. Operation. EWS initiates communication with all transponders within 1000 ft of the toll plaza by sending the ENQuiry wake-up signal. The wake-up signal is a 915 MHz signal with a modulated 128-bit code, which includes timing frames, synchronized pulses, encrypted data, and a noncryptic checksum that is emitted from the EWS antenna every 15.6 ms. The test signal is received and processed by the transponder to verify that the first 16 bits form a frame and synchronized pattern and that the checksum byte is correct. Upon successful recognition, each transponder and the EWS execute a custom anticollision listen–talk algorithm. The LTA allows only one transponder at time to successfully communicate its VID to EWS, after which time it waits for an eligibility response.

Four possible communication scenarios exist after successful transponder recognition of EWS test signal:

1. A. Transponder able to respond via LTA (successful VID transmission to EWS)
   B. Eligibility status relayed
   C. Unit dormant

2. A. Transponder able to respond via LTA (successful VID transmission to EWS)
   B. No eligibility status relayed within 0.5 s.
   C. Transmission failure
   D. Re-execute LTA

3. A. Transponder not able to respond via LTA (EWS accepted transmission from another transponder or general communication failure)
   B. Re-execute LTA

4. A. Eligibility status not received within 3.5 seconds.
   B. Error condition signaled at transponder

5.3. In-Lane Reader. The receiver, transmitter, and baseband of the in-lane reader (ILR) are similar to those of the EWS. The ILR uses a short-range, directional, 45 degree antenna. The baseband unit utilizes an 8 bit microprocessor that is linked with the computer via a serial data connection and a circular memory buffer to store vehicle information.

The ILR receives vehicle identification data (VID and eligibility status) from the computer and stores it in its circular memory buffer. As cars pass through the express toll lane, the ILR reader is triggered by a light-beam interruption or by a weight detecting treadle.

The short range antenna independently reads the transponder's VID number, by sending an ENQuiry command, and compares it against the stored vehicle information. If the VID was deemed eligible by the EWS, a "charge" event is recorded in the local memory along with a date/time stamp. If the VID was not eligible to use the express lane, the ILR signals the violation enforcement system (see section 7) and records a "violation" event in the local memory along with a date/time stamp.

The circular memory buffer is continuously read by the main computer to charge the appropriate toll fees to patron accounts. The circular memory buffer is managed memory. The data residing in memory are always made contiguous, and data is deleted and added under strict rules.

6. Supporting Data

The EWS was designed based on the following assumptions: 100 mph maximum vehicle speeds, vehicle detection begins 1000 ft before the toll plaza, two-lane highway (each way) with one traditional toll lane and one express lane, 300 kbs data transfer rates.

In a 5 second period the WVI system is able to accurately process 25 vehicles within 1000 feet of the toll plaza while passing through the toll plaza at up to100 mph (147.67 ft/sec).

(100 mi/hr) x (5280 ft/m) x (hr/3600 s)
= 146.67 ft/s (1)

The EWS sends out 30 ENQuiry commands per second. Each vehicle (transponder) has 7.8 ms in which to respond after "waking-up" from ENQuiry command.

In the worst case scenario with no collisions, the LTA requires 1.6 ms to execute (from initial ENQuiry command to the time EWS receives VID).

(vehicle/7.8ms) x (1.6ms/ENQuiry) =
4 vehicles/ENQuiry command (2)

(4 vehicles/ENQuiry) x (30 ENQuiry/s) =
120 vehicles/s (3)

The WVI system has the ability to process 600 vehicles in 5 seconds.

(5 s)(120 vehicles/s) = 600 vehicles (4)

This allows for an average of 24 failed communication attempts per vehicle to establish an eligibility status within 5 seconds for 25 vehicles at the worst-case communication rates.

In 5 seconds the vehicle has traveled 733.3 ft and complete communication has occurred within this distance, and the toll lane computers are ready to receive the fast-paced vehicle. There is no required stopping or slowing of vehicles.

The toll lane computer contains the approaching vehicle data in its memory. This allows for microsecond access while the vehicle travels through the lane and the account is charged. The necessary response time of the computer is 81.8 ms, which allows the computer 10 retries within the 12 ft ILR zone.

(12 ft read zone) / (147.67 ft/s) = 0.0818 s (5)

With one express lane and one EWS, the expected throughput is 18000 vehicles/hr, which would all but eliminate toll plaza bottlenecks due to toll collection.

(25 cars /5 s) x (3600 s/hr) = 18,000 vehicles/hr (6)

The other important advantage of the early warning feature is the feedback of account status to the patron. The patron can change lanes early, without danger of collision.

7. Violation Enforcement System

Each express lane will be equipped with a violation enforcement system (VES) comprising an in-lane camera and a VES computer linked to the land-based main computer. In this way, violators will be identified and penalized accordingly. This offers the opportunity to recoup financial losses presently unrecoverable in most instances.

8. Future Work and Applications

The transponder of the future may also have multichannel capability in case of noise or heavy traffic at the selected frequency. This technology has myriad applications:

1. Controlled parking facilities. Here, the system automatically detects the vehicle, authorizes or does not authorize the vehicle to proceed, and keeps a log of the entries and exits. This is well suited to schools, hospitals, courthouses, federal buildings, etc.
2. Current smart-card facilities can also benefit: WVI adds the security advantage of not having to lower the window or come to a complete stop. Again, a log of entries and exits may be kept.
3. This system can be used to check vehicles in and out of a secured facility. For example, mail trucks can be logged in and out. This way, missing, late, or stolen vehicles can be detected and tracked automatically.
4. Rental car agencies could also benefit. WVI could be used to keep an up-to-date inventory.
5. Land-based as well as water-based traffic could utilize this technology. The water-based applications mirror those on land (marina security, etc.).
6. Finally, this technology can be applied to home security. It can be used to disarm the home security system, automatically alerting the user of a break in or emergency and thereby avoiding surprise attacks. In this way the vehicle can be used as a safety shield.

9. Conclusions

In this paper, a state of the art vehicle identification system has been described. By utilizing the technology of today, this system can be used to modernize current toll-collection systems, maximizing potential and minimizing current problems.

10. Acknowledgments

Our thanks to Douglas and Amy Lichorwic for their technical assistance in preparing this manuscript and to Christina Medina for preparing portions of the figures.

11. References

[1] A. Kamerman, "Evaluate Wireless LAN PHY options to best Match Your Application," *Wireless Design and Devlopment, Magazine of Wireless Technology*, Vol 4, No10, October 1996, pp. 21-25.

[2] MC13144D, Motorola Semiconductor Technical Data, Motorola, Inc., Tempe, AZ, 1996.

[3] MC13142D, Motorola Semiconductor Technical Data, Motorola, Inc., Tempe, AZ, 1996.

[4] MC145220DT, Motorola Communications Device Data, Motorola, Inc., Phoenix, AZ, October, 1996.

[5] MC13158, Motorola Semiconductor Technical Data, Motorola, Inc., Tempe, AZ 1996.

[6] Code of Federal Regulations, Title 47, U.S. Washington, DC, 1994, Parts 15, 95.

[7] XL107, "1996 Data Book," Excel Microelectronics, Inc., 1996.

[8] D. Parker and W. Wiseman, "Bridging the Future: Enhanced Communications Services for Mobile Business Systems," *Commercial Wireless Systems*, October, 1996, pp 59.

[9] Carlos A. Medina, Patent Application, "Vehicle Detection and Identification System," filed September 7. 1995.

High Accuracy Radar Angle Sensor With Passive Nonlinear Transponder

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This article considers theoretical and practical aspects of a high accuracy, as well as a reliable radar angle sensors, which was designed for the industrial mining applications.

In spite of the fact that mining is one of the most profitable resource exploration industry, the level of automation is still much less commonly used compare with manufacturing industry. This problem is an object of many R&D projects. One of the typical task here is to design sensors of angle displacement that obtain high accuracy (fraction of a meter) when the operational distance can reach 100 m and more under the strong environmental conditions: dusty, dirty, humidity and so on. Most attractive for such applications are radar equipment. One of the serious restriction on the radar implementation is the target noise as the geometrical size of targets. In mining industry typically (trucks, draglines, flat wagon and so on) this size much bigger then requirement accuracy. In order to solve this problem, a radar transponders are recommend to place on these targets.

In the paper will be introduced some results in the design and field test of radar sensor for dragline's bucket (the bucket size is about 4x4x8 m) azimuth angle measurement. The requirement linear accuracy is about 0.5 m (standard deviation) at the distance 100 m from the target. In general this technique can also be extended to other applications.

This sensor has a two channels receiver and spatially separated antennas. The phases of the signals are compared by the detector and after analog to digital conversion processed in the computer. The phase different will curry information regarding to the time delay of the signal propagation between target and the receivers centre axis. It can be recalculated for the bucket displacement relative to the axis. On the dragline bucket a transponder is used and it is merely functioning as a nonlinear frequency doubler. This transponder contain 6 dBi gain patch cross polarized transmitter and receiver antennas , input and output filters and zero bias diode. The operational frequencies are ISM 902 MHz-928 MHz for the transmitter and relevant second harmonic for the receiver. This type of transponder will work effectively with input power between -10 dBm to -15 dBm, that satisfy requirement distance with 1 W average power transmitter.

This system architecture is tolerance to the target noise, and provide a fraction of meter linear accuracy at the distance 100 m. Some results of the field test for the working prototype, problems and future directions of the work will be described in the paper.

Advanced RF Solutions for Automotive RKE Systems

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Abstract

This paper will address the advantages of Radio Frequency [RF] over Infra-Red in Remote Keyless Entry [RKE] systems. It will also address the various regulatory requirements worldwide and how they affect RF designs / solutions. A description of several RF solutions, including application highlights, will be presented as well.

RF vs. IR

The trend away from Infra-red (IR) systems, which dominated RKE in the 1980s, towards RF systems continues with a pace. The advantages of the low price and simplicity which IR systems can offer is no longer enough to satisfy the demands of OEM automotive manufacturers and their aftermarket Car Alarm / RKE counterparts.

RF systems offer the following advantages:

- ...do not require line-of-sight operation
- ...not blocked by fog, snow, dirt or fluorescent lighting
- ...multi-mode operation (trunk, remote start alarm, immobiliser, etc.)
- ...increased security and complexity of encryption software
- ...extended range of operation

Regional Specification Issues

The local regulatory authorities in each country issue specifications which set the RF performance of RKE systems that are intended for use in these countries. Although there is great similarity in these specifications, there are some particular regional differences that need to be fully understood in order to service these markets. For example, some countries have specific frequency allocations for periodic telemetry type communications only, and continuous transmission must be performed at a separate frequency. Discussions on these points will be included in the paper.

Solutions Using Integrated RF Receivers and Transmitters

The paper will also address the various design options / trade-offs and will provide valuable application solutions / suggestions.

Embedded Antennas – Promises, Pitfalls, and Precautions

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Abstract––Wireless applications often require the antenna to be embedded into a metallic assembly that is not necessarily ideal for good antenna performance. With careful design, multi-step prototyping, and accurate measurements, one can tailor the antenna to the application and achieve the desired performance. The procedure for embedded antenna development, some examples, and pitfalls to avoid are presented.

1.0 INTRODUCTION

The dream of any antenna designer is to have plenty of space to fit an appropriate antenna into an application, with a completely unobstructed view from the antenna to the outside world. Unfortunately this ideal often is not the case. In many wireless applications the antenna must be hidden from view for aesthetic reasons, or located directly on the printed circuit board (PCB) for cost and manufacturability considerations. As a result the antenna may be smaller than optimum, a different shape than the "classical" antenna design, and surrounded by materials and circuit components that greatly influence its performance. Implementation of such "embedded" antennas require custom design with great attention to detail, along with accurate performance verification measurements. While there are no hard and fast rules for embedded antenna design, this article describes some general guidelines, techniques, precautions, and design examples for embedded antenna applications.

2.0 OVERVIEW OF EMBEDDED ANTENNAS

2.1 Definitions

Before describing some typical types of antennas for embedded applications, a brief review of antenna related definitions is in order. Following are terms that are important for an antenna designer to understand:

- Antenna: a device that transfers electromagnetic energy between a transmission line and free space. An antenna couples RF energy into or out of the electro-

magnetic field in the vicinity of the antenna, and thus is affected by nearby objects that absorb or reflect RF energy.

- Radiation pattern: a plot of the amplitude versus angle of a transmitted or received signal relative to that of a reference antenna, for a fixed frequency and polarization. Antenna patterns are usually plotted in dB relative to an isotropic source (dBi) or a dipole (dBd), where 0 dBd is equal to 2.2 dBi. Since most antennas are reciprocal devices, the pattern for receiving is the same as that for transmitting. Fig. 1 shows an example.

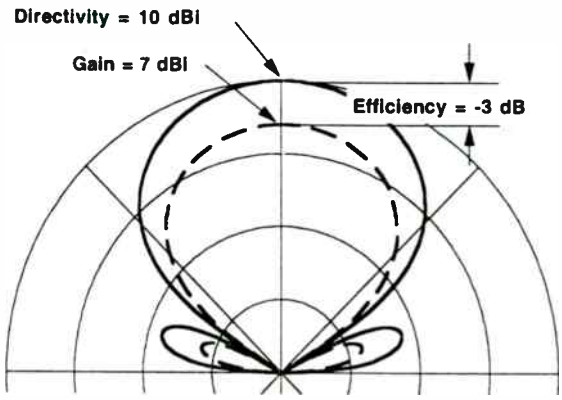


Fig. 1 Antenna Radiation Patterns Illustrating the Definition of Efficiency

- Directivity: the ratio of the radiation intensity (watts/unit solid angle) to the average radiated power, in the direction where the radiation intensity is maximum. Directivity is a measure of the ability of the antenna to concentrate power in one direction. Directivity may be expressed as a ratio or in decibels. The peak of the antenna directivity pattern in Fig. 1 is the directivity.
- Gain: same as directivity except total input power is used instead of average radiated power. Gain is directivity with ohmic losses and reflection losses in the antenna included. The peak of the antenna gain pattern in Fig. 1 is the gain.
- Efficiency: the difference between gain and directivity, representing the absorptive and reflective losses in the antenna. For example, an antenna with a gain of 7 dBi and a directivity of 10 dBi has an efficiency of -3 dB, or 50%, as illustrated in Fig. 1.
- Half-power beamwidth (HPBW): the angular width between the points on an antenna pattern that are 3 dB down from the peak, representing a power ratio of one-half. The half-power beamwidth is illustrated in Fig. 2.

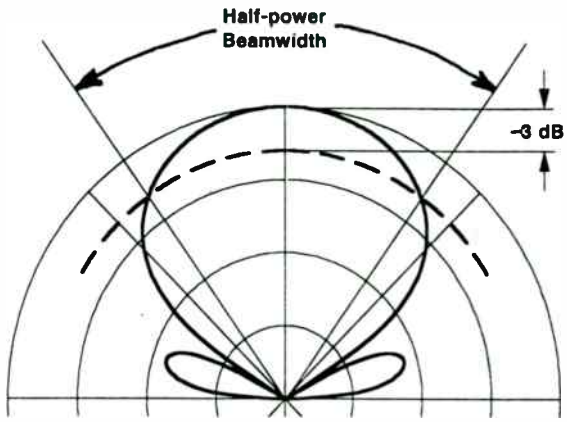


Fig. 2 Definition of Half-power Beamwidth

- Polarization: orientation of the electric field of an antenna or electromagnetic wave. Antennas must have matched polarizations for maximum power transfer.
- Voltage standing wave ratio (VSWR): ratio of peaks to nulls of the standing wave produced by reflection from a discontinuity in a transmission line. VSWR is a measure of the power reflected back into the output circuit for a transmit antenna, or back into space for a receive antenna.
- Bandwidth: frequency range over which a chosen parameter, such as VSWR, meets specification.

2.2 What makes an antenna radiate?

Also important for embedded antenna design is an understanding of the principle of antenna radiation. When an antenna is embedded into an assembly, there may be no clear cut definition of where the RF circuitry ends and the antenna begins. Care must be taken to assure that the antenna and not the

circuitry is the prime source of radiation or reception.

An antenna will radiate (or receive) electromagnetic energy when it provides either a separation of charge or a current loop, as illustrated in Fig. 3, and its impedance is matched to the circuit. Parts of the circuitry or assembly to which the antenna is attached may radiate or receive unwanted energy if they also form separations of charge or current loops.

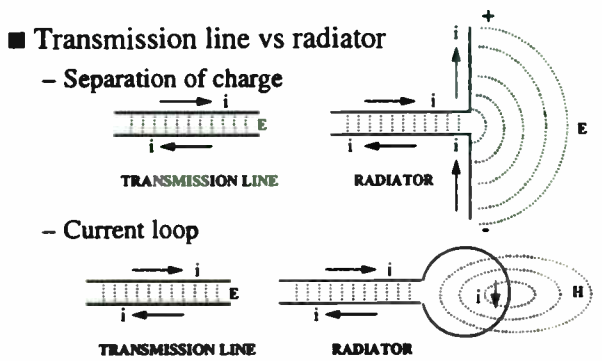


Fig. 3 Principle of Antenna Radiation

2.3 Typical antenna types for embedded applications

Embedded antennas for wireless applications usually must be small and operate at a single frequency or over a narrow frequency range. Typical small narrowband antennas types are monopoles, dipoles, loops, and patches, as illustrated in Fig. 4. The inverted-L, inverted-F, and planar inverted-F antennas are simply reduced height versions of the quarter-wave monopole. Monopole and dipole type antennas radiate because they provide a separation of charge, while the loop antenna forms a current loop. The patch antenna forms a separation of charge across the slot between the radiating element and the ground plane. Implementation of an embedded inverted-L antenna in an electric utility meter is shown in Fig. 5.

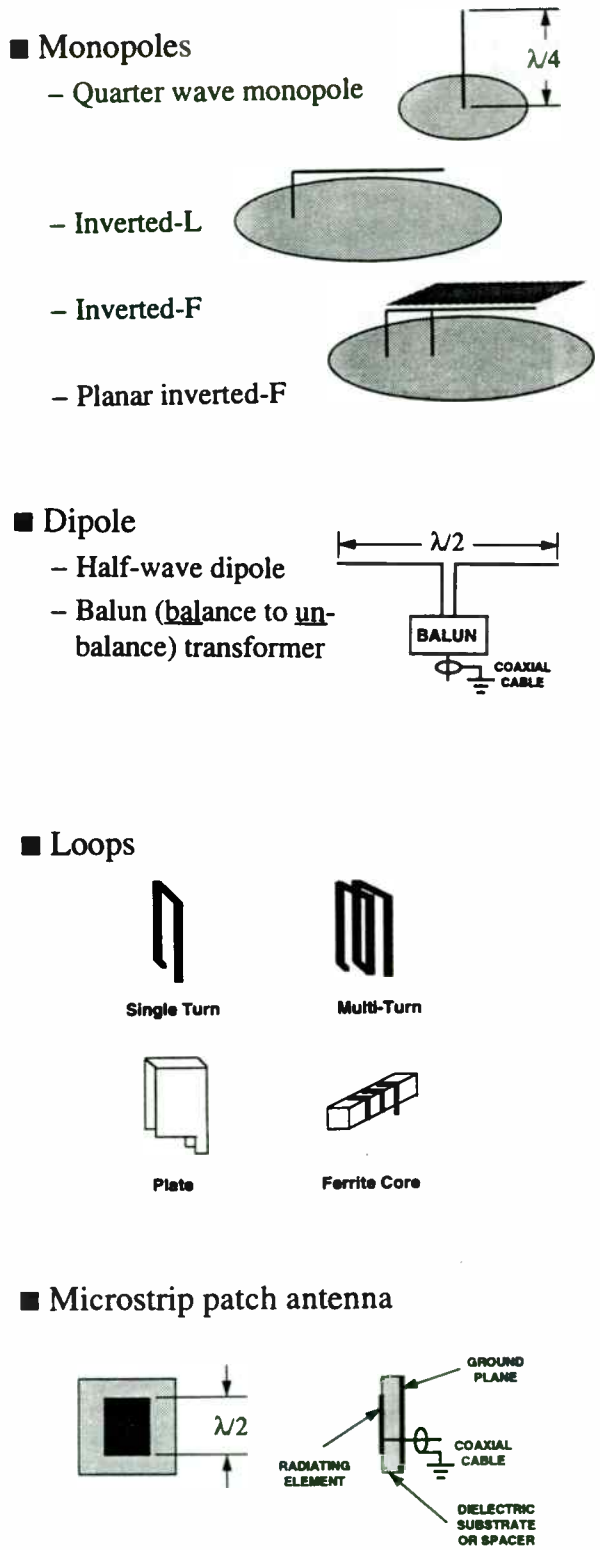


Fig. 4 Typical Antenna Types for Embedded Applications

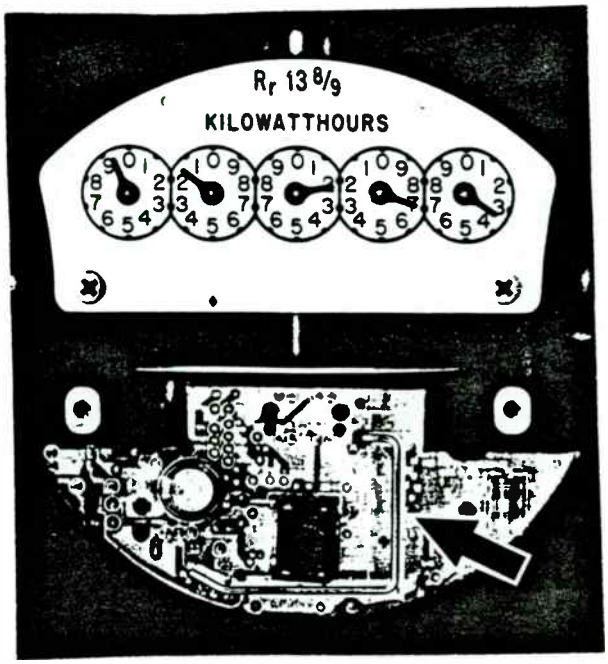


Fig. 5 Inverted-L Antenna (Arrow) Embedded in an Electric Utility Meter

2.4 Requirements for embedded antennas

All antennas have basic requirements that dictate antenna type, size, and shape, while embedded antennas may also have stringent physical constraints. The designer must assure that the antenna impedance is matched to the circuitry for maximum power transfer, usually stated as a VSWR specification. The frequency bandwidth may be expressed as a percentage about the center frequency, and must include a margin for variations in manufacturing. The peak gain and HPBW must provide sufficient link margin and angular coverage, while the polarization must be such that maximum energy is transferred to or from the antenna at the other end of the link. And the limits on size, location within the assembly, and manufacturing cost must be met.

As an example of typical requirements for an embedded antenna application, an endpoint device for a wireless LAN microcell may require an antenna matched to 50 ohms with under 2:1 VSWR, over a frequency bandwidth of 3%, with good efficiency such that gain is optimized over a broad coverage angle (i.e., low directivity since the direction to the base station is unknown), with predominantly vertical polarization. The antenna must be small, soldered directly on the PCB to reduce cost, and is surrounded by metal structures that may reflect, resonate, or absorb at the LAN frequency.

3.0 ANTENNA DESIGN PROCEDURE

Antenna design follows a basic procedure that involves theory and simulation, prototyping, and measurement, as described in the following sections.

3.1 Design process

While some antenna designers rely heavily on theory and others lean more toward empirical modeling, they all tend to follow the same basic steps:

- Determine requirements.
- Trade off candidate antenna types.
- Search literature and text books for design information.
- Perform numerical modeling.
- Build and test breadboards.
- Perform design iterations (as needed).
- Build and test prototypes.
- Specify design details for alpha, beta, and production builds.
- Pray a lot.

The last step results more often from desperation than from reverence!

3.2 Theory and simulation

A wealth of information on antennas exists in the literature, some highly theoretical, some very practical. Some of the more useful sources for embedded antenna design are listed in the references. Numerical analyses can be performed and antenna patterns computed using computer simulation programs such as NEC (Numerical Electromagnetics Code) and

MININEC; however, all antenna analysis programs require experience to determine their limitations, and verification of results by measurement is highly recommended.

3.3 Prototyping

Because of the limited predictability of antenna performance, particularly when the antenna is surrounded by absorbing and reflecting structures, the value of good prototyping cannot be overemphasized. Early prototyping of the antenna in the conceptual stage will prove feasibility of the design and verify performance predictions. Since the materials, circuit boards, and structures surrounding the antenna often do not exist early in the development, the designer must make the best effort to simulate them for early measurements, and then repeat prototype antenna measurements when the real materials, circuit boards, and structures become available. Rechecks of the antenna performance for the alpha, beta, and production pilot versions of the product are important to verify that changes to board layout or other structures have not adversely impacted antenna performance.

3.4 Measurement

Prototyping of new antenna designs and verification of final performance require accurate measurement of antenna patterns and gain, and of VSWR. Embedded antennas are usually electrically small, which makes accurate measurements more difficult because test cables tend to radiate or receive RF energy with nearly as much gain as the antenna under test. Ferrite beads can be used on test cables to suppress stray radiation. Typically gain measurement accuracy of 1-2 dB and pattern dynamic range of 20-40 dB are required to verify link margins and pattern coverage, while VSWR (or return loss) must be measured with enough accuracy to verify that the antenna is properly tuned. All measurements should be performed with the antenna residing in the assembly with surroundings intact, to simulate any effects that may detune the antenna or change its gain or pattern shape.

While accurate network analyzers for measuring VSWR are readily available, good range facilities for gain and pattern measurements are expensive and require careful design. Construction and instrumentation of an anechoic chamber suitable for most wireless applications costs about $100K-200K. Anechoic chambers or outdoor ranges can sometimes be rented. Open-air test sites designed for FCC-required radiated emissions measurements are not suitable for antenna development because the ground plane over which the measurements are performed does not simulate free-space.

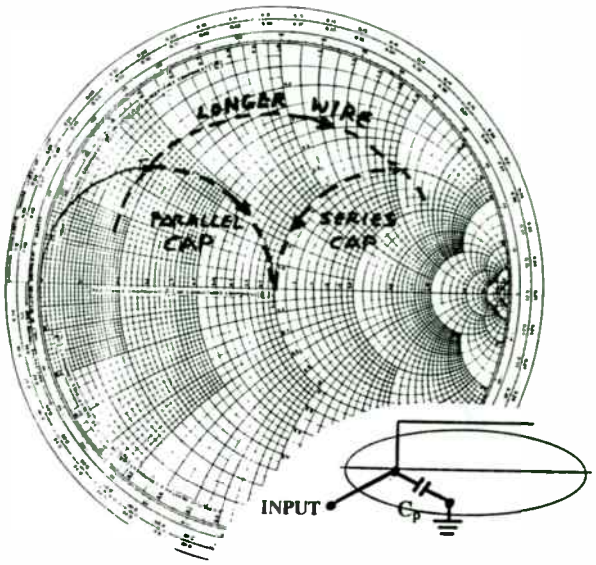
4.0 EMBEDDED ANTENNA EXAMPLES

Several design examples will serve to illustrate design practices and effects of embedding antennas.

4.1 Inverted-L wire monopole

The inverted-L wire monopole antenna is compact and inexpensive to manufacture, and can be soldered directly to a PCB. Proximity of the wire to the ground plane lowers its impedance to about 10 ohms, versus 37 ohms for a quarter-wave monopole over a ground plane. The antenna can be easily matched with a series or parallel capacitor, as shown in Fig. 6, where the length of the wire is adjusted to move the impedance or admittance to the unit circle on the Smith chart.

Computed gain and patterns for two polarizations using MININEC shown in Fig. 7 illustrate why the inverted-L antenna is desirable for applications where a mix of vertical and horizontal polarizations across a wide beam is desired Since the antenna is driven against a ground plane, mounting the inverted-L antenna on an actual PCB may cause the gain to drop several dB, depending on PCB material and shape, component density, and height of the antenna off the PCB. Patterns of an inverted-L antenna on a small PCB are shown in Fig. 8. When the height of the element is reduced and the PCB is buried in the metallic assemble of an electric utility meter, the gain is reduced and patterns are distorted further as shown in Fig. 9.



- Wire length adjusted to move to unit admittance or impedance circle
- Parallel or series capacitor added to move to center (perfect match)

Fig. 6 Use of a Smith Plot to Match the Inverted-L Antenna

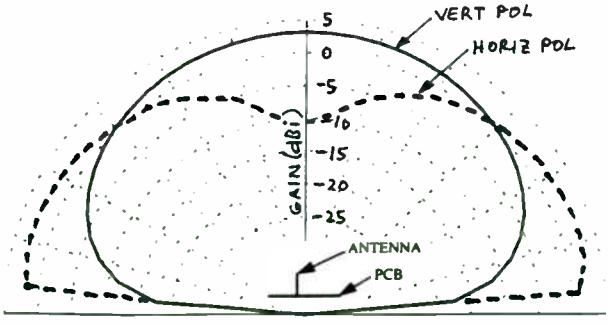


Fig. 7 Calculated Patterns of the Inverted-L Antenna

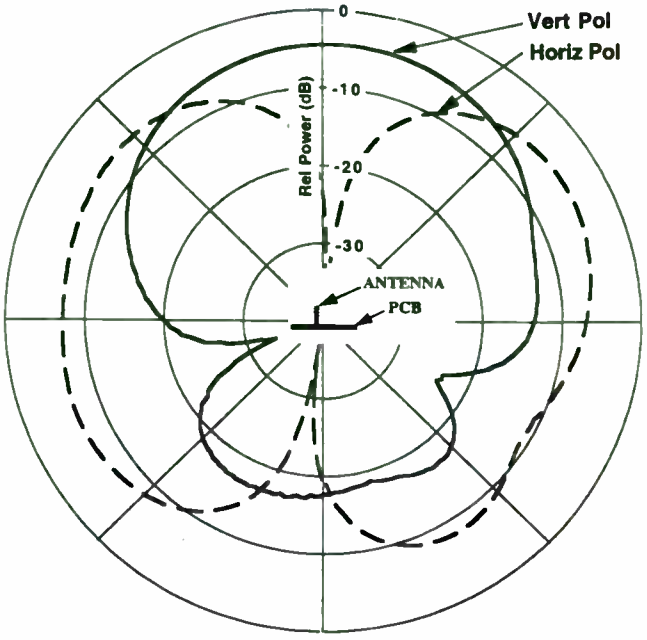


Fig. 8 Measured Patterns of an Inverted-L Antenna on a Small PCB

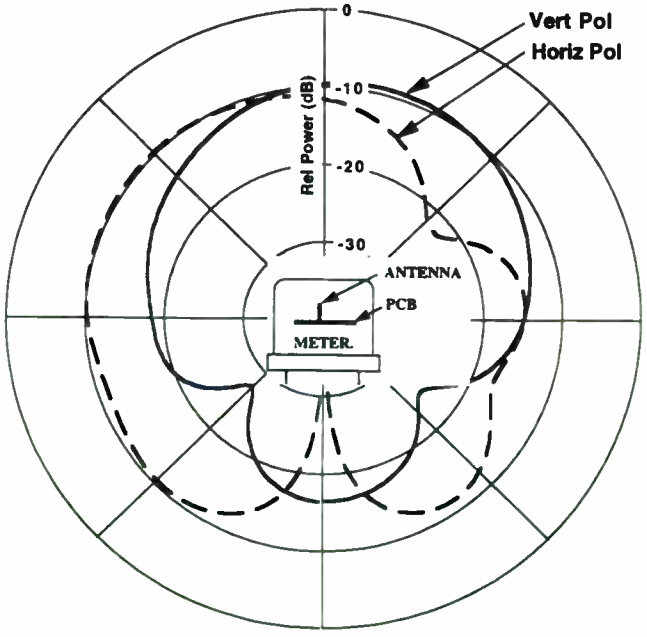


Fig. 9 Measured Patterns of an Inverted-L Antenna Embedded in an Electric Meter

4.2 Loop antenna

The loop antenna is small, rugged, and inexpensive to manufacture. Because it couples to the magnetic field rather than the electric field, a loop is generally less sensitive to surroundings and therefore more efficient than monopole type antennas. However, a small loop has a very low impedance, generally 1-2 ohms, which causes losses in the conductor and matching network to affect its gain more than for a monopole. Gain of the loop is proportional to its included area; thus the area should be made as large as possible. Matching should be done with capacitors rather than inductors, since inductors have lower Q (more loss) and will reduce the gain. A single series capacitor will match a loop of limited size, while two capacitors placed as shown in Fig. 10 will allow the loop to be larger for more gain.

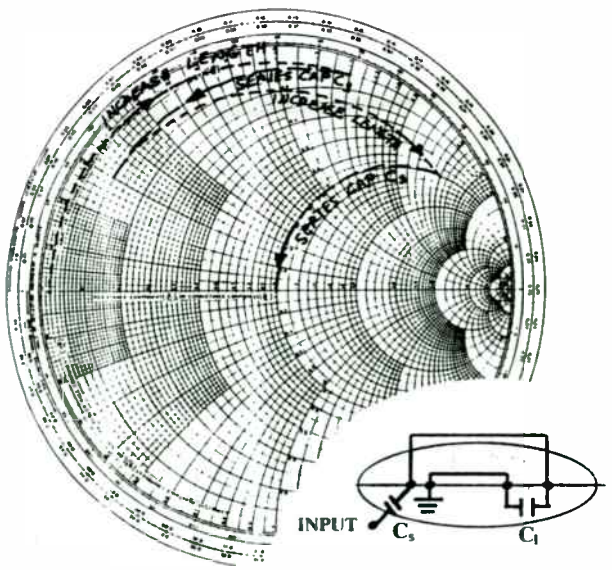


Fig. 10 Use of a Smith Plot to Match the Loop Antenna

A loop on a small PCB produces the measured patterns shown in Fig. 11, which shows nulls perpendicular to the loop and predominant polarization in the plane of the loop. When the same loop and PCB are embedded into an electric utility meter, a broad pattern is produced in front of the meter due to the meter base acting as a ground plane as seen in Fig. 12, and the gain is several dB higher than that obtained from the loop and PCB alone.

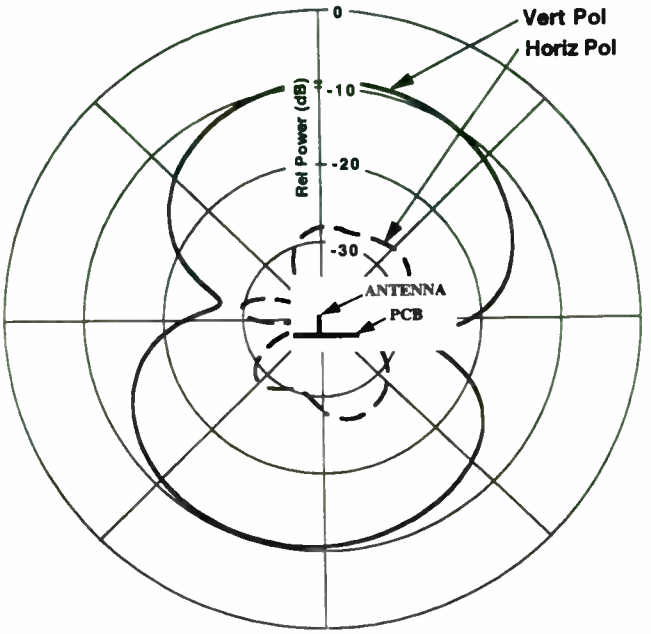


Fig. 11 Measured Patterns of a Loop Antenna on a Small PCB

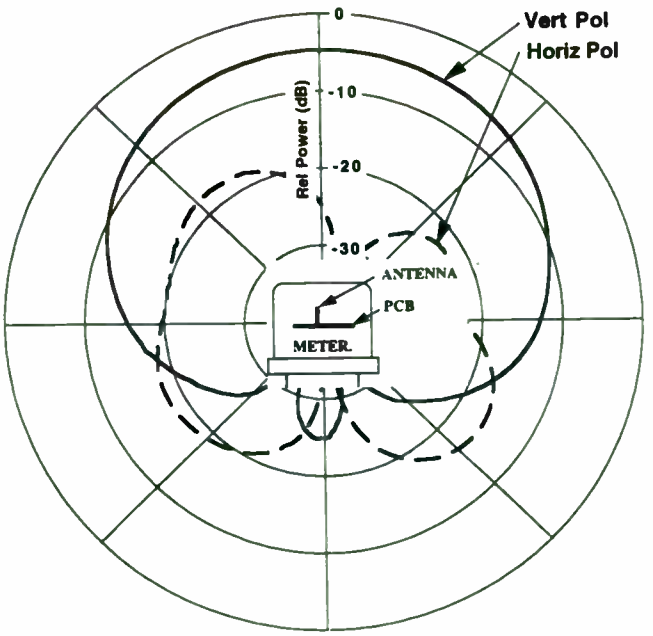


Fig. 12 Measured Patterns of a Loop Antenna Embedded in an Electric Meter

4.3 Printed dipole antenna

Sometimes the PCB is buried in an assembly such that an antenna mounted directly on the PCB cannot provide adequate pattern coverage. In this case a dipole printed on a flexible substrate with a coaxial cable attachment is a good solution, albeit more expensive to manufacture than a PCB-mounted antenna. The dipole can be placed in a part of the assembly that has minimal effect on its performance, and it can be oriented for the desired polarization. The printed circuit dipole shown in Fig. 13 is photoetched on 3 mil mylar and uses surface mount components to form a lattice balun to appropriately advance and delay the currents for balanced excitation from the coaxial cable. Measured free-space patterns shown in Fig. 14 are typical of a dipole antenna. Fig. 15 shows the patterns of this antenna when placed along the edge of an electric utility meter face. While the pattern is skewed off center due to the asymmetry of its location in the meter, the gain is high because the antenna is away from the structure and does not rely on the PCB to provide a ground plane.

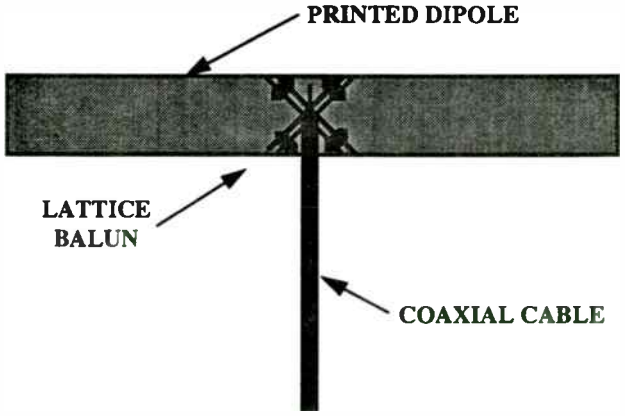


Fig. 13 Printed Dipole Antenna

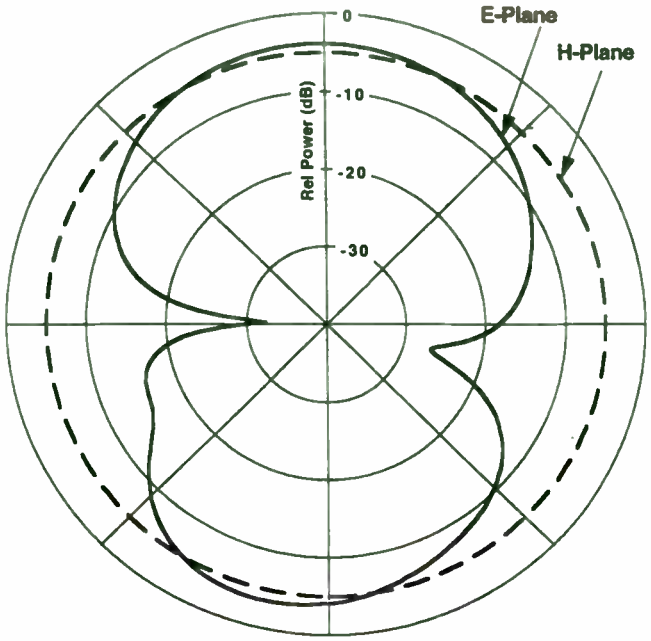


Fig. 14 Measured Patterns of a Printed Dipole Antenna in Free-Space

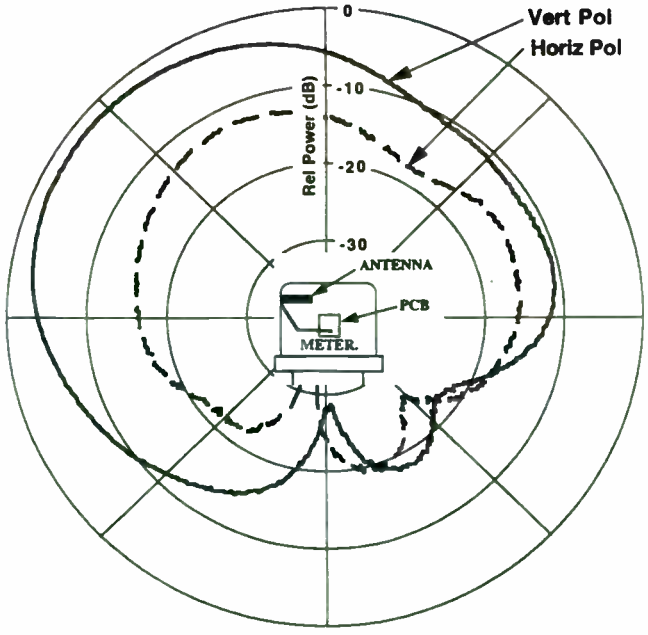


Fig. 15 Measured Patterns of a Printed Dipole Antenna on an Electric Meter

5.0 CONCLUSIONS

The foregoing discussion and examples should serve to illustrate some basic principles that must be observed for successful design and implementation of embedded antennas:

- **Design to fit the application.** An "off-the shelf" antenna will not work in most embedded antenna applications. A custom design, taking into account all the requirements and trade-offs, is the key to success.
- **Pay attention to details.** When the antenna is such an integral part of the whole assembly, small details or changes can have major effects on antenna performance.
- **Prototype, prototype, and prototype again.** Never underestimate the value of prototyping and measuring performance at each step along the way.
- **Design for manufacturability.** The design of a high performance antenna is wasted if its performance cannot be maintained though the manufacturing process, or if the cost to manufacture it is prohibitive. Early and frequent interface with manufacturing is essential to provide a finished product that meets requirements for manufacturability.

REFERENCES

- K. Fujimoto and J. R. James, Ed., *Mobile Antenna Systems Handbook*, Artech House, 1994.
- K. Fujimoto, A. Henderson, K. Hirasawa and J. R. James, *Small Antennas*, Research Studies Press Ltd., 1988.
- Richard C. Johnson and Henry Jasik, Ed., *Antenna Engineering Handbook*, McGraw-Hill, 1984.
- John D. Kraus, *Antennas*, McGraw-Hill, 1950.
- *IEEE Transactions on Antennas and Propagation.*

WIRELESS COMPONENT SOLUTIONS

Wireless Component Solutions

Session Chairperson: Paul Khanna,
Hewlett-Packard Co., Communications Components Division (Santa Clara, CA)

Antenna Technologies for New Millimeterwave Communication Systems

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Introduction:

The explosive growth of new point-to-point, point-to-multipoint, and satellite communication systems in the millimeterwave spectrum has created a demand for new and innovative antenna systems. Each system has its own set of special requirements. Some require sharply focused pencil beam antennas while others require shaped sector coverage. Cost and size are factors for all types. As the number of antennas on roof tops increases, so does the need for aesthetic solutions.

This paper outlines the antenna design considerations, and describes recent developments in millimeterwave antennas. It also provides an overview of the various antenna architectures and technologies used for new applications. The key characteristics of each antenna are compared, to highlight the relative advantages. Among the new products discussed are flat antennas for point-to-point radio systems and high gain sectorized antennas for LMDS, LMCS, and MVDS point-to-multipoint systems. Also, multiple beam antennas are considered for point-to-multipoint applications.

Millimeterwave Systems Overview:

The recent need for both higher data rate communications as well as the ability to handle an increased traffic load has resulted in a push to higher frequency use, such as millimeterwaves (loosely defined as the frequency range from 18 GHz to 100 GHz). With increased frequency of operation comes the increased bandwidth required for high data rate communications. Millimeterwave systems can support bandwidths in excess of 500MHz while cellular systems typically employ approximately 25MHz. Assuming this bandwidth, data rates comparable to fiber optical transmission are possible.

Millimeterwave propagation attenuation is greater than it is for signals in the cellular region due to higher path loss. This results in a reduction of interfering signal strength. Unfortunately, atmospheric absorption, rain, snow and fog cause significant desired signal attenuation at these frequencies, and prevents link ranges from exceeding about 10 km (i.e., at 36GHz the attenuation in medium rain is approximately 6dB/Km.). The systems must be designed for statistical worst case rain conditions that very dramatically with latitude. The transmission through building walls and trees is reduced by approximately the ratio of the frequencies (e.g., 36GHz / 0.9GHz). Therefore, unlike 900MHz cellular systems, millimeterwave reception depends on line-of-sight propagation. This allows polarization diversity to effectively double the system bandwidth. These and a variety of other system tradeoffs dictate the antennas electrical requirements.

New systems must be ubiquitous, reliable, cheap and easy to install and operate. It is possible that in the not so distant future, system installation costs will be less for millimeterwave systems than for comparable cellular systems. Millimeter wave antennas are smaller, lighter, and require simpler mounting bracketry. The resultant savings in installation cost will approach a significant percentage of the overall installed system cost.

Design Considerations for millimeterwave Antenna Systems:

An antenna is a transition between electromagnetic waves in space and voltages or currents in a transmission line. When transmitting, the antenna converts electrical signals into radio waves; a receiving antenna reverses the process and transforms radio waves back into electrical signals. Most antennas are *passive*; structures that launch or collect radio waves without the benefit of *active* circuitry. The ability of the antenna to concentrate its radiated power is called

directivity. Antenna gain is the directivity reduced by the antenna's inherent inefficiency such as feed attenuation and miss-match loss. We refer to the angular width of the main beam measured between the 3 dB points as the half power beamwidth. Beamwidth and directivity vary inversely with each other; a high-directivity antenna has a narrow beamwidth and vice versa. Directivity is proportional to the physical area of an antenna expressed in square wavelengths. This infers a frequency scaling nature to antenna design. For example, if an antenna with a given directivity is 4m in diameter at 0.9GHz, a 36GHz frequency scaled version of the antenna would have the same beamwidth and directivity characteristics but would be only 10cm. Alternatively stated, the same size antenna provides narrower beamwidths and higher directivity as frequency increases. Therefore, millimeterwave antennas are smaller than their lower frequency counterparts, for equivalent performance. Subsequently they require higher tolerance production techniques.

The dissipative loss associated with millimeterwave feed geometries makes it more difficult to achieve high efficiencies. At lower frequencies dielectric losses generally dominate the transmission line loss. A conductor's surface resistivity increases as the square root of frequency. Therefore feed networks that have significant transmission line content must employ low loss line geometries such as waveguide or suspended stripline. Free space is of course the lowest loss transmission line and antennas, such as parabolic reflectors and space fed arrays generally have higher efficiencies than printed circuit arrays. **Table 1** lists common high gain geometries and notes the amount of dissipative loss.

Because the feed structure is a key part of antenna design, a variety of schemes have been developed. *Parallel, series*, and *resonant* are the three common array feeding schemes. A parallel feed is essentially an *N*-way power divider, *N* being the number of elements. In contrast, a series feed consists of a single transmission line. The array elements couple the appropriate amplitude and phase from the transmission line. An antenna with a series feed is refereed to as a traveling wave antenna. It typically has a matched load at the end of the transmission line to absorb the remaining power. The resonant feed is similar to the series feed except that it is short-circuited at the end of the transmission line. Hence, rather than *a traveling wave*, a *standing wave* resides in the transmission line. . Of the three feed types, traveling wave arrays normally have the lowest losses. *Resonant arrays* are typically narrow band solutions. Parallel feeds offer the most pattern control.

Applications and Systems:

Point-to-point links; The traditional use of millimeterwave frequencies is for high data rate point to point links. The fastest growing point-to-point application is in cellular networks, handling traffic between radio base stations and host switching centers, and between radio base stations. The main attraction of this type of radio transmission system is the speed with which the base station infrastructure can be installed. It eliminates the need for the civil engineering work and cable laying associated with land-lines. Each system handles between two and sixteen E-1/T-1 channels over a distance of 3 to 15km depending on frequency and antenna size. Radio frequencies of 23, 26 and 38 GHz are standard.

The traditional antenna solution for point-to-point applications is the reflector antenna. Parabolic "dishes" are the design of choice. These consist of a parabolic reflector illuminated directly by a feed antenna, or indirectly through a subreflector. Feed antennas are usually horns or open ended waveguide. The directly illuminated version is referred to as a "prime focus fed" antenna. Indirectly illuminated versions are usually based on classical "folded" optical telescopes -- "Cassegrain" and "Gregorian" antennas for example. If a planar, subreflector is placed very close to the small feed horn, the subreflector is referred to as a splash plate.

Table 1. Antenna Architecture as a Function of Dissipative Loss

Low Loss	Medium Loss	High Loss
Horn / Reflector	Waveguide Array	Microstrip Array
Space Fed Array / Lens	Radial Slot Line Array	Stripline Array

Interference is a growing, pervasive threat to the wireless industry, particularly in dense urban regions. As wireless penetration increases, more dense urban cell sites are needed, causing increased interference. To reduce the effects of in-band interference the regulatory boards such as the FCC dictate that antenna sidelobes (spurious radiation in directions other than the desired main beam) must be suppressed below a certain level. In order to meet this requirement two approaches prevail. The traditional approach involves using an absorbing shroud around the perimeter of the reflector to absorb the stray radiation that results in sidelobes. However modern design tools and software now make possible a second alternative that employs a broad beam feed and a reflector with a very small focal length to diameter ratio. **Figure 1** shows the two structures. With proper design, both approaches yield comparable sidelobe levels. However, the second approach results in a significant reduction in antenna depth and therefore windloading, lower cost through the elimination of the shroud and expensive absorber, and improved aesthetics. This is important when considering the increased resistance to highly visible antennas arising in the US and other countries. The radiation pattern of a shroudless antenna and the various regulatory specifications are shown in **Figure 2.**

Although modern shroudless reflector antennas are much smaller, there is a strong desire for even thinner "flat" antennas. Low profile array antennas have been proposed as an alternative to parabolic reflectors. To truly be competitive the array must have a comparable cost, electrical and mechanical performance, and reliability. Therefore, the production materials must be environmentally robust, consistent, repeatable, and low cost. To achieve a gain of 44dBi (assuming 100% efficiency), an array generally needs on the order of 25,000 radiating apertures or "elements".

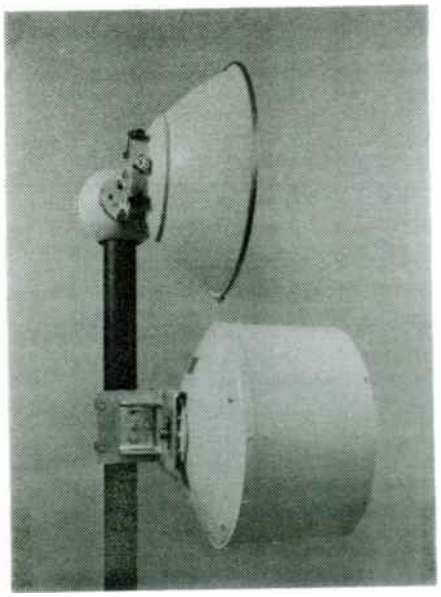


Figure 1. Reflector Antenna Geometries

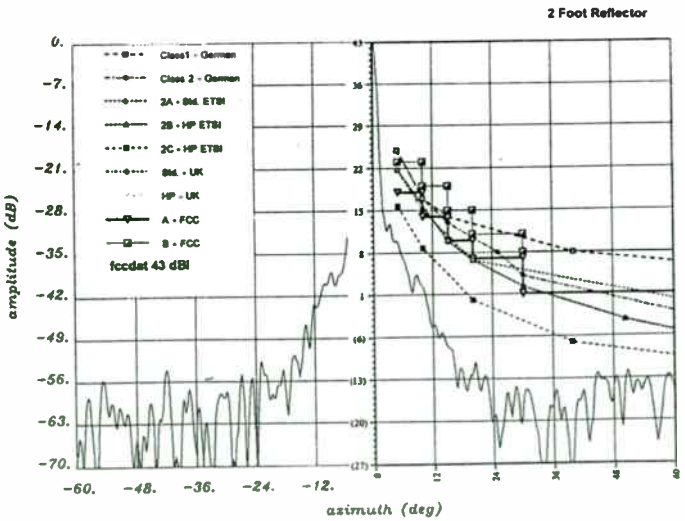


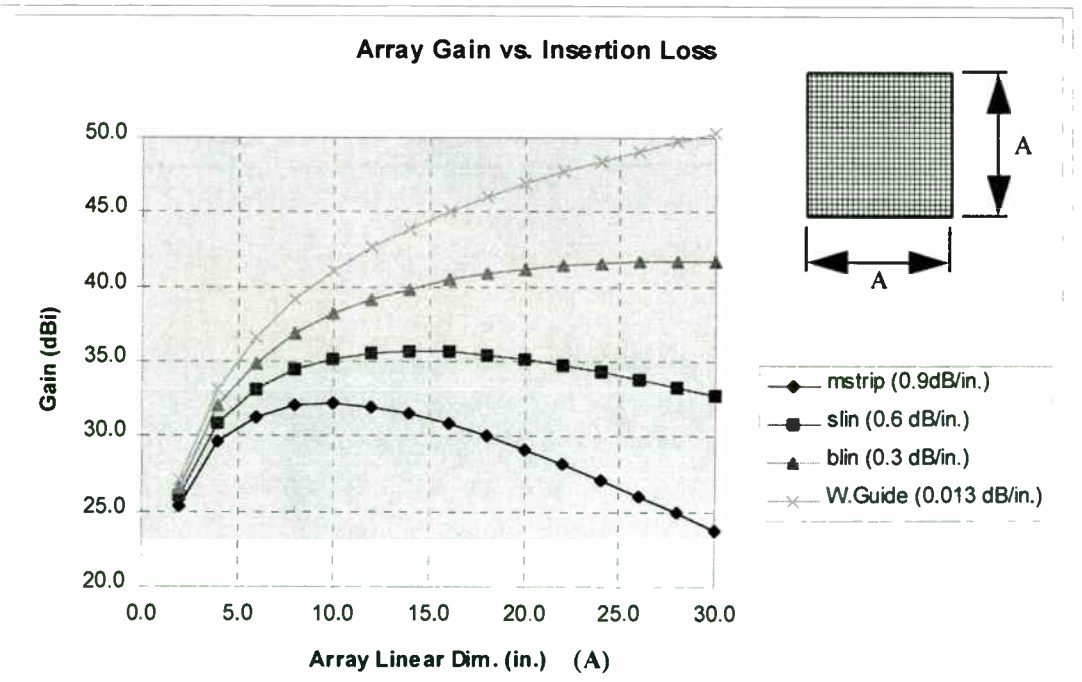
Figure 2. Radiation Pattern and Sidelobe Envelopes

This clearly would require a sophisticated feed network to divided the power between the elements with the proper amplitude and phase. As mentioned earlier, such arrays suffer from significant attenuation due to feeder losses. This means that as the number of elements and therefore the size of the array grows, the attenuation increases. **Figure 3** shows antenna gain as a function of array size. What can be concluded from this figure is that printed circuit arrays are not practical for gains greater than 30 (microstrip) or 35 (stripline) dBi.

In order to achieve the high efficiencies required for back-haul applications, low loss waveguide type feeds must be employed. Additionally, in order to satisfy the stringent sidelobe levels imposed by the regulatory commissions, the amplitude and phase accuracies at each element are extremely difficult to achieve, and maintain in high volume production. As an example, for a 38 dBi array to meet the FCC standard "A" sidelobe levels, the allowable amplitude or phase errors are approximately ± 0.8dB (RMS gaussian errors assuming no phase error) or ± 7° (RMS gaussian errors assuming no amplitude error) respectively. If both errors are present, the amount of errors allowable is a *few tenths* of dB in amplitude and a *few* degrees.

Printed circuit arrays typical for lower frequency products are inappropriate at millimeterwaves, due to inherent variabilities of the substrate materials used. This statement is true for even the most expensive materials available. As an example, **Table 2** summarizes typical substrate errors for common materials, and the resultant amplitude and phase errors. Printed circuit array errors are too large for these applications. Therefore, arrays are not presently a cost effective alternative to high gain reflectors at millimeter wave frequencies.

Present low profile printed arrays are not yet adequate for traditional point-to-point applications. They are best suited for smaller, lower performance applications such as short haul Ethernet links in business parks or within buildings. Examples of 12 and 38 GHz microstrip arrays are shown in **Figure 4**.



(mstrip = microstrip, slin = stripline, blin = air supported barline, w.guide = waveguide)

Figure 3. Array Gain vs. Insertion Loss

Point to Multi-point links; This is an area of growing interest. Local Multi-point Distribution Systems (LMDS) provide interactive broadband video, voice, and data services helping to meet the public demand for multichannel video programming and two-way voice and data services. Assuming the proposed FCC rulemaking is adopted, they will use the radio frequency spectrum between 27.5 and 28.35 GHz and two smaller bands in the 28 to 31 GHz band. They will send and receive two-way broadband signals in cells of 3 to 6 miles in diameter. On the surface, they work like the narrow band operations of cellular telephone systems. However, the video, voice and data broadband LMDS signals are two-way capable. The hub antenna requirement for LMDS systems is similar in scope to that of cellular base stations. The user end, however, is quite different.

Table 2. Typical Array Errors

Type of Error	Physical Error	Microstrip Series-fed Phase Error, 5% Bandwidth (degrees)	Microstrip Series-fed Amplitude Error, 5% Bandwidth (dB)	Aperture Coupled Phase Error, 10% Bandwidth (degrees)	Aperture Coupled Amplitude Error, 10% Bandwidth (dB)
Excitation Amplitude	+/- 0.2 dB		.2		.2
Excitation Phase	+/- 5 deg.	5		5	
Subs. Diel. Constant	+/- 0.04	8	.1	8	.1
Subs. Thickness	+/- 0.001 in.	12	.25	12	.25
Etching Tolerance	+/- 0.001 in.	12	.25	12	.25
Manuf. Variation	+/- 0.001 in.	12	.25	12	.25
Element match (dB)	-15 to -30 loss	6	.05	6	.05
Element Positioning	0.001 in.	12	.25	12	.25
Frequency Dispersion	0.2 dB, 5 deg.	5	.2	10	.4
Diffract./Space wave	-20 dB	6	.1	6	.1
RSS Errors (1)		**27.6**	**0.6**	**28.9**	**0.7**

(1) - Root Sum Squared

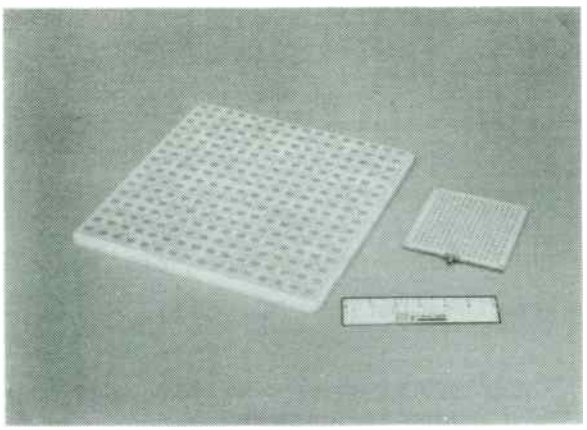


Figure 4 - Low profile array antennas

One would like to broadcast power into a cell such that all the recipients in the cell receive comparable power levels, and all recipients outside the cell receive as little power as possible. The best solution is an antenna with elevation beam shaping capabilities and very low azimuthal sidelobes. Due to the frequency scaling nature of antennas, the technology used for conventional cellular base stations is not feasible at 28GHz, because of to the associated difficulties relating to achieving tight tolerances at low cost. At the moment there are few LMDS base station antennas on the market. **Figure 5** shows a traveling wave array technology that is currently in use today. This antenna produces a 25dB gain fan beam suitable for 45 degree sector coverage. The antenna has a 2 degree elevation pattern and null filling to illuminate users near the base station. Similar designs are available for other sector coverage.

The LMDS customer requires antennas similar to that of the point to point links described earlier. The most notable difference is the cost and reliability. Our telephone service providers are willing to pay a premium for system reliability. Hence the point to point antennas described earlier must withstand extreme environmental conditions without a significant statistical chance of failure. In general, the average consumer is not willing to pay this premium. Therefore, lower cost alternatives are required. This normally means less sophisticated, low cost dish antennas and mounts, similar to the direct satellite TV dishes. These provide somewhat degraded electrical performance, relative to the traditional point-to-point reflectors.

Another particularly interesting antenna for point to multi-point hubs is the spherical lens. The lens has radiation characteristics comparable to a reflector antenna with the same diameter. However, this shared aperture structure can generate many beams. The number of beams is limited only by the physical space behind the lens. It is an ideal hub structure for congested regions with limited "roof-rights". **Figure 6** shows a spherical lens with feeds that provide both 38GHz and 28GHz.

Satellite Links; Most current low earth orbit (LEO) satellites lack sufficient space on the system *bus* to deploy large antennas, but instead utilize simple monopole antennas, often called "whips." The reduction in antenna gain of these whips as compared to the reflector antennas carried by a typical geostationary earth orbit (GEO) satellite is compensated for by the reduction in path loss resulting from shrinking the radio path length from perhaps 40,000 km for a GEO satellite to perhaps less than 2,000 km for a LEO satellite.

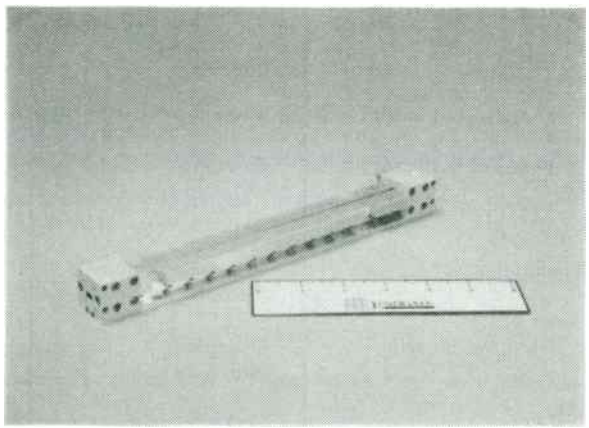


Figure 5 - LMDS Antenna

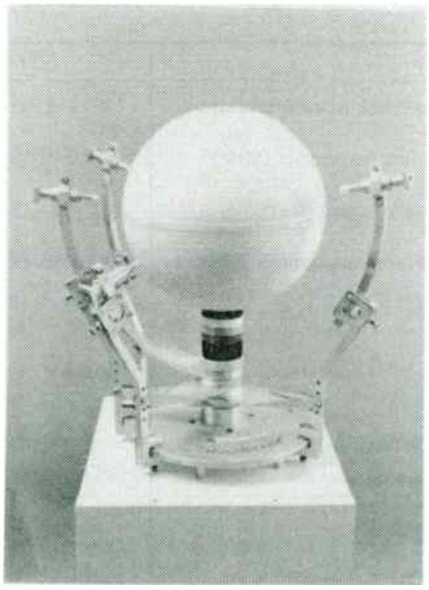


Figure 6 - Multiple Beam Spherical Lens Antenna

Ground antennas for LEO systems have tended to be Yagis or helices. Reflector antennas would be impractically large at the lower frequencies used in present day systems. However, there is no inherent difference in the requirements for LEO and GEO system ground antennas. Horn-fed reflector antennas constitute a mature technology which is particularly suited to those applications where an earth station or a satellite communicates with space or ground terminals in relatively fixed locations where there is room to install a dish. Thus most *large* GEO satellites carry front-fed offset parabolic antennas. Spot beams are generated by exciting appropriate collections of feed horns. Two reflectors may be nested one behind the other to provide beams with different shapes on, for example, vertical and horizontal polarization. The front reflector reflects horizontally polarized signals while being nearly transparent to the orthogonal vertically polarized signals. The rear reflector reflects the vertically polarized waves that passed through the front reflector.

Table 3 summarizes the information required by the ground-station antenna designer for some of the major upcoming communication satellite systems that have a significant millimeterwave content. With the advent of LEO systems like Motorola's IRIDIUM, that require sophisticated beams, LEO satellites may soon be carrying phased arrays and reflector antennas. The uses of millimeterwave frequencies allow these structures to be small and therefore more easily deployed on satellites.

The Teledesic system has by far the most millimeterwave content. Using a constellation of several hundred low-Earth-orbit satellites, a global, broadband "Internet-in-the-sky," Teledesic will enable affordable access to fiber-like telecommunications capability anywhere in the world. Approximately 840 satellites in 21 planes in a sun-synchronous, inclined circular low earth orbits provide the services. Rather than targeting voice and supporting low bit-rate data as Odyssey and Iridium do, Teledesic focuses on providing wireless broadband services with a fiber-like quality, focusing on data and supporting voice. The user terminal antennas have a diameter ranging from 8 cm to 1.8 meters, and an average output power ranging from 0.01 W to 4.7 W. The antenna diameter is determined by maximum output power, maximum channel rate, climatic region and availability requirements.

These proposed Ka-band LEO systems will offer the antenna designer a challenge to develop a large quantity of low cost millimeterwave "user" antennas. More sophisticated (possibly scanning) antennas will be required for the gateways.

Table 3. Planned Satellite Systems Utilizing Significant Millimeterwave Content

	Odyssey	Iridium	Teledesic
Mobile down-link frequencies (MHz)	2483.5 -2500.0 (S-band)	1616.0 -1626.5 (L-band)	Ka-band
Mobile up-link frequencies (MHz)	1610.0 -1626.5 (L-band)	1616.0 -1626.5 (L-band)	Ka-band
Feeder up-link frequencies (GHz)	29.1 - 29.4 (Ka-band)	27.5 -30.0 (Ka-band)	Ka-band
Feeder down-link frequencies (GHz)	19.3 - 19.6 (Ka-band)	18.8 -20.2 (Ka-band)	Ka-band
Inter-satellite Link (ISL) freq's (GHz)	N/A	22.55 -23.550	60
Beams per satellite	61	48	64 beams (supercells) 576 cells
Satellite antenna	Steerable, moving cells using directed coverage	Fixed, moving cells	Steerable earth-fixed cells
Orbit class	MEO	LEO	LEO
Altitude (km)	10354	780	695-705
Number of Satellites	12 + 3 spare	66 +6 spare	840 + up to 84 spare
Mobile terminal min. El. angle (deg.)	20	8.2	40

Future Trends:

The rapid development of cellular and PCS networks, video on demand, videoconferencing, and interactive television are creating unprecedented demands for new millimeterwave systems and innovative antenna solutions. As build out continues, the need for smaller, less obtrusive antennas will become increasingly important. This is driven both from a societal desire for aesthetics, as well as the need to deploy and install the greatest number of antennas in a fixed number of locations. Therefore, the antenna designer will be encouraged to develop smaller, lighter and simpler antenna solutions. Concealment will be an increasingly important design consideration, as will cost reduction as the competition drives the cost-per-installation downwards. The new "Campus-LAN" opportunities offer the designer the opportunity to deploy inexpensive microstrip antenna arrays in large volume, while the backhaul requirements mandate the use of more sophisticated, highly efficient arrays. The greatest challenge lies in the innovation of new flat plate antenna concepts that lend themselves to high volume, low cost production.

Another opportunity relates to the ability of service providers to adapt their system as they add new subscribers, without the need for an installer to climb the tower. One example is an adaptive multiple beam antenna which provides growth potential via switchable feeds. Unused beams are activated to accommodate new users. Further into the future the arrays might be fully adaptive. They would optimize the link through beam steering and pattern nulling. It becomes obvious that the associated active millimeter wave component costs must be reduced dramatically, to be feasible in these scenarios. Active integrated arrays offer the highest degree of antenna flexibility, but are not yet feasible due to their economics.

LOW-SIDELOBE ARRAYS FED BY A UNIFORM DISTRIBUTION FEEDING NETWORK

by

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ABSTRACT Low sidelobe arrays typically use feeding networks with appropriate amplitude and phase distributions which in some cases can be lossy and narrow-band as a result of their complexity. In the new approach presented in this paper, a simple uniform distribution is feeding the array elements which are not uniformly positioned in the traditional uniform grid.
The location of the array elements is such that the sidelobes of the array factor are "pushed" in the end-fire direction. There, the element pattern is low enough in amplitude to effectively suppress the array-factor sidelobes to the required level. The combination between the simple uniform distribution feeding network and the spatial distribution of the array elements results in a simple design of a low-sidelobe array.

1. INTRODUCTION

The methods for the design of low sidelobe array are well established and are essentially based on complex feeding network feeding radiating elements positioned on a uniform grid. The realization of these feeding networks can be quite complex, and the results could be a 'crowded circuit' that generates the undesired mutual coupling between the feeding network and the radiating elements.
In this paper, we propose a simple design of low-sidelobes arrays using a "reversed logic". The feeding network is of the simple binary type leading to a uniform distribution; the radiating elements though, are positioned on a non-uniform grid. The idea is to break the array-factor sidelobes close to the main-beam, and "push" them towards the end-fire where the attenuation due to the radiating element pattern will reduce the array sidelobes to the required level. As it will be shown, this is a wide band effect. The efficiency of such an array is very close to that of a classical array with the amplitude distribution producing the same sidelobe level.

2. DESIGN

The array described below is a linear (H-plane) array of 32 patches (Figure 1). As mentioned above, the design involves the redistribution of the array elements so that the high sidelobes of the array-factor rise towards the end-fire direction. The main consideration (except for the radiation pattern) was to obtain a relatively small antenna, in order to keep

the aperture efficiency comparable to the one obtained using the a traditional tapered feeding network. For example, if a 20 dB side-lobe array with a raised cosine distribution has a gain factor of 0.833 [1], the non-uniform array should have a similar gain factor.
The array was designed to work at 2.45 GHz and was required to have a sidelobe level better than 18 dB. Initially, the synthesis method for non-planar arrays described in [2] was used. There, the displacement of elements from the uniform grid was relatively small and could be treated as a slight perturbation. The results obtained were not satisfactory, since to obtain a sidelobe level of about 20 dB, the size of the deviations from the uniform grid were such that they could not be considered just perturbations. A number of optimization routines (typically used in pattern synthesis) were used, however they did not give satisfactory results. The reason for this, probably resides in the difference between the character of the unknowns (coefficients in the array factor summation versus array element locations); the error function in the latter case is of an oscillatory kind which makes it very difficult to converge. Finally, the design was based on a Geometrical Optics cancellation of the first couple of sidelobes and was subsequently refined using a polynomial expansion for the location of the array elements:

$$x_j = x_{j-1} + d_o \sum_{i=1}^{Q} i \times \left(\frac{j}{N}\right)^{i \times m}$$
$$0 \le j \le N-1 \qquad (1)$$

where

x_j - the location of the j-th element.
d_o - the initial distance between the first and the second element ($0.7\lambda_o$).
m= 6.8.
Q=3.

Figure 1 - The layout of the array.

A parameter study was performed and the values shown for m and Q where found to give the best results. The change in the distance between consecutive elements (in cm) for the array described, is shown in Figure 2.

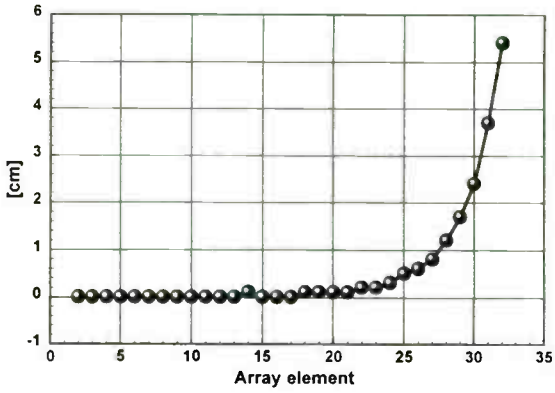

Figure 2 - The change in the spacing between consecutive elements, compared with the spacing between the first and the second element.

The radiation patterns of the array are shown in Figure 3.

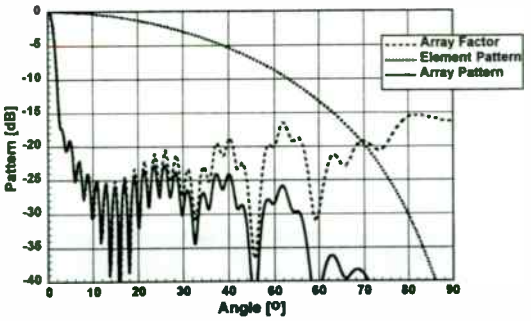

Figure 3 - The radiation patterns of the array factor, the radiating element and the array itself.

The performances of such an array were checked over a relatively wide range of frequencies. The results are shown in Figure 4.

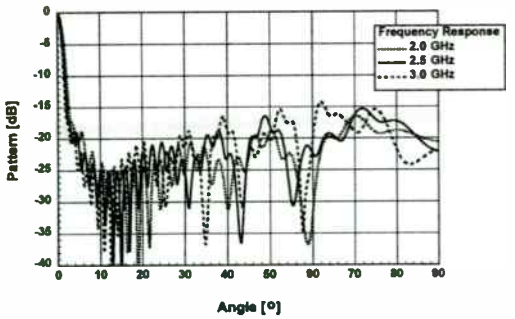

Figure 4 - The Array Factor performance over 50% bandwidth.

Considering the change in the radiating element pattern over this frequency range (assumed to be the pattern of a cosine distribution), the array patterns are shown in Figure 5.
As shown in Figures 4 and 5, the effect obtained is relatively broadband.

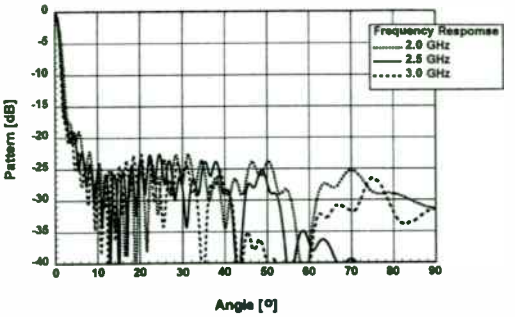

Figure 5 - The Array performance over 75% bandwidth.

3. CONCLUSION

It was found that the lower the sidelobe requirement is, the lower the resulting aperture efficiency is (compared with traditional tapered arrays). Thus, this method of design is best applicable for arrays where the highest sidelobes are in the 18-22 dB range. If the requirement is for sidelobes lower than 18-20 dB, then, the designer is facing the trade-off between the feeding network complexity (using the classical uniform grid) and aperture efficiency (using the approach proposed here).

REFERENCE

[1] H. Jasik, Antenna Engineering Handbook, McGraw-Hill, 1961, p.2-26.
[2] N. Herscovici, "A Simple Cosec2-Microstrip Array: The Shovel-Microstrip Array", *IEEE Antennas and Propagation Magazine*, Vol. 35, No. 4, August 1993, pp.42-44.

1900 MHz LNA Design with High Linearity and Low Noise Figure

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Today's wireless applications for cellular and PCS require Low Noise Amplifiers (LNAs) with a combination of high IP3@ input and low noise figure. To accomplish these demands, well-thought choices should be made. The choices are naturally on the device level, but especially on the level of the surrounding circuitry.

With the advanced 'double poly' bipolar RF process, developed by Philips Semiconductors, it is possible to create devices that do not only have an excellent noise figure at high frequencies, but also have enough power handling capability for good IP3 performance. Such a device is the BFG425W, a XB425 crystal in SOT343 package.

More important in LNA design with high linearity are the impedances which the matching circuits present to the device. One can not only match for optimum noise performance, but also use the matching circuits for other purposes which can significantly improve intermodulation performance. For example:
- Base decoupling at low frequencies
- Harmonic termination

During the presentation, design techniques for optimized matching circuits will be shown. This will result in a low cost, robust design of the Low Noise Amplifier. A circuit is available and measured data will be compared to simulation results.

Aging and Anomalous Time Stability Behaviors of Quartz Crystal Frequency Sources

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The aging of quartz crystal frequency sources has traditionally established the life, maintainability, and capability of communications systems. This aspect continues to be encountered by the designers of advanced wireless systems. This paper will provide a detailed overview of the time-dependent frequency stability of quartz and what limitations a designer should be aware of when specifying quartz controlled frequency sources. These limitations are particularly relevant when considering the use of a disciplined quartz system as a substitute for rubidium or other atomic based frequency standards.

Aspects to be covered are aging drift, retrace, frequency and phase popping, hysteresis and noise (frequency jitter). Specific detail will be provided about unpredictable and non-repeating events. A technique will be revealed which allows the separation of the contribution of the quartz resonator from the sustaining circuitry to permit advanced diagnostics of the frequency control system. Finally, a review of the physical mechanisms will be discussed to provide a boundary to the limitations of quartz technology as it currently exists and what can be anticipated from precision quartz manufacturers in the future.

Ceramic Filter Design

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Introduction

RF wireless communications has become a tremendous growth field. RF devices are appearing in applications from telephones to computers to wireless identification tags. In the vast majority of these applications radio transceivers are used of which RF filters are primary components. Ceramic filter technology offers a cost effective solution to many of today's new RF transceiver applications.

Papers have been written that discuss the design of ceramic filters[1,2]. The purpose of this paper is to augment the previous publications by embarking on a brief review of ceramic filter operation and then focussing on recent developments in intercell coupling, 3D modelling of ceramic filters, and surfact mount application.

Ceramic Filter Operation

The vast majority of filters produced by Motorola CPD are distributed element combline filters. Their design is based on the quarter wave resonator. But before there can be discussion of the design of ceramic filters, a discussion of the resonant properties of ceramic must ensue.

Figure 1 is a cross sectional view of a ceramic resonator. The resonant frequency of this structure can be approximately determined the following formula:

(1) $$Fo = c/(4he_r^{1/2})$$

where:

Fo = Resonant frequency
c = Speed of light in vacuum
h = Height of the resonator
e_r = Relative dielectric constant

The reason that this is an approximate formula is that there is some fringing capacitance at the open circuit end of the resonator that lowers the resonant frequency slightly.

It was discovered that these resonant elements could be placed in proximity of each other in a monolithic structure in such a manner that intercell coupling could be created and that the spacing of the resonant elements could be calculated for filters of desired bandwidth. Chebyshev responses of a monotonic nature could be created by assuring that all electric field fringing components were minimized, however, it was also discovered that the intercell fringing capacitances could be manipulated synergistically with intercell magnetic field coupling to place transmission zeros at finite frequencies. By using a quasi-elliptic response, higher values of attenuation close to the passband could

be achieved than the traditional monotonic response.

The first monolithic ceramic bandpass filters that manipulated coupling zeros used an edge coupled pattern that was printed on the open-circuit side of the filter. This technique became very popular and is still in use today on duplex filters. However, this technique utilizes processes that, unless highly automated, are labor intensive and it soon became apparent that a less laborious coupling technique was needed. This led to using 3D coupling structures.

Recent Coupling Developments

It was found that, by creating geometries on the open-circuit and short-circuit end of the resonators, the intercell coupling zeros could be manipulated in a similar manner to the printed patterns. The advantage of the new technique is that the forming of the geometries could be combined with the forming of the monolithic resonators. While the design of the structures became more complicated, 3D coupling structures significantly reduced the processing costs of the filter.

As time progressed and cost pressures continued to ensue it became apparent that a new technique was needed to further reduce the manufacturing costs of ceramic monolithic bandpass filters. A new coupling technique was needed that reduced performance sensitivity to process variation and reduced the number of process steps required to manufacture the filter. A third technique has been developed that accomplishes many of the objectives. It is centered around the concept that, instead of manipulating the geometry of the resonator to adjust intercell coupling, it could be more cost effective to manipulate the ground plane in proximity of the resonator to achieve the desired result. This ground plane coupling technique reduces design sensitivity because the manipulation of coupling occurs in areas that are removed from the maximum electric and magnetic fields. By holding similar process tolerances that would be held for the former techniques, the net variation is reduced or, if net variation is not critical, less costly processes could be used to create the product.

Another interesting concept evolved with the implementation of ground plane coupling structures. The top print and 3D coupling geometries are very useful for manipulating adjacent cell coupling zeros. As such, for an N pole filter, N-1 adjacent cell coupling zeros could be easily obtained. These structures do not easily lend themselves to non-adjacent resonator coupling. It was found that non-adjacent resonator coupling could be easily achieved by altering the ground plane. This means that the number of coupling zeros that can be theoretically manipulated increases from N-1 to N!/2(N-2)!. With the introduction of additional coupling zeros stopband performance is again enhanced.

3D Modelling of Monolithic Ceramic Bandpass Filters

One of the challenges facing the design engineer in the design of monolithic ceramic bandpass filters is to find a design simulation tool that accurately predicts the performance and geometry of the final product. Such a tool, if established, would dramatically reduce design cycle time and iterative tooling costs. It would also prove valuable in estimating feasibility of new coupling and resonator concepts.

Motorola CPD uses a combination of modelling tools in the design of this class of filters. Initial proof of concept is performed using Touchstone. Figure 2 is a Touchstone model of a typical filter. Parasitic effects can be qualitatively modelled using Touchstone, however, it is difficult to draw quantitative conclusions on parasitic effects. Optimal self

and mutual impedances can be quantitatively gathered as well as approximate resonator length. At that point it is best to switch to Ansoft Eminence.

The first module that is helpful is the 2D parameter extractor. This module is used to obtain the cross sectional geometries of the resonators that are consistent with the self and mutual impedances established by Touchstone. The geometries are obtained through an iterative analysis of the impedance matrix which is transformed from the capacitance matrix using these formulas:

(2) Zo_i = Self Impedance of the ith Resonator = $e_r^{1/2}/(c\sum_{j=1}^{N} C_{ij})$

(3) Z_{ik} = Mutual Impedance between Resonators i and k = $e_r^{1/2}/(c|C_{ik}|)$

where;

C_{ij} = Capacitance between Resonator i and j
c = Speed of Light in Meters per Second
C_{ik} = Capacitance between Resonators i and k

Linpar can also be used to ahieve the same results.

Once the cross sectional geometries are established they can be swept into a three dimensional structure and analyzed using the Eminence 3D structure simulator. Figure 3 is a model of a 3 pole ceramic filter that has been modelled using Eminence. Input and output ports of a coaxial nature have been used. The primary advantage in using Eminence is that, if care is taken during modelling, parasitic couplings can be realized to a reasonably accurate level. The secondary advantage is that the coupling structures can be precisely determined and tooling can be designed explicitly from model parameters. The latter concept significantly reduces development cycle time.

Surface Mount Application of Ceramic Filters

Monolithic Ceramic Filters are coated with a fired silver thick film metallization. This metallization is subject to interactions with the Tin component of molten solder alloys commonly selected for component attachment to printed circuit boards. This interaction is exacerbated by excessive heat. As such some time should be spent discussing the surface mounting of these filters.

Monolithic Ceramic Filters are usually applied using solder paste. To minimize tin ingress into the silver metallization it is recommended that a silver bearing alloy be used. Two common silver bearing alloys are 62Sn/36Pb/2Ag and 62Sn/36Pb/1.4Ag. Non-silver bearing solder alloys have been used successfully, however, knowledge of this application is limited.

The process physics behind the application of the silver metallization to the ceramic body is such that the metallization near the edges of the filter is not as thick as the metallization in the center of the metallized surfaces. As such, it is recommended that solder masks be designed to in such a manner to prevent solder from contacting the edges of the filter. An offset of .030" is desirable and .010" is an absolute minimum.

Another issue that arises in the surface mount process is that, as the solder reaches reflow temperature, the filter will float on the liquid solder and move, causing solder shorts or poor attach. This effect can be significantly reduced by creating a grid

resist pattern in the areas where large quantities of solder is being applied. The resist grid breaks the surface cohesive forces and reduces filter slip.

Furnace Reflow

The optimum solder reflow technique for ceramic filters is furnace reflow. Reflow ovens provide greater thermal uniformity when reflowing metallized components, however, care needs to be exercised when creating and adjusting oven reflow profiles so that the component is not subjected to temperatures that would accelerate tin ingress. This is particularly challenging when the large thermal mass of these filters is considered. Perhaps the best technique for administering this process is to attach a thermocouple inside the filter resonator hole and run a temperature profile of the filter as it is reflowed. The temperature of the filter body, as measured in the resonator hole, must not exceed 205 degrees centigrade and should not dwell above 180 degrees centigrade for more than 60 seconds.

Manual Reflow

If manual reflow is necessary, it is recommended that a heat gun or hot plate be used. It is helpful that the filter be preheated to 180 degrees centigrade before final reflow. Pretinning the filter with a soldering iron is not recommended due to possible damage generated by a concentrated heat source.

Humidity/DC Bias

It was discovered that the application of a DC potential to the input and output terminations of the filter in the presence of humidity activates a migration of the silver ions from the ground areas to the termination, dropping the DC resistance from several megohms to several hundred ohms within a month of exposure. As such, when applying ceramic filters, it is recommended that blocking capacitors be used to eliminate this potential.

WANs AND WLANs

WANs and WLANs

Session Chairperson: Aljis Juodikis,
Juodikis and Associates (San Jose, CA)

New Standards and Radio Chipset Solutions Enable Untethered Information Systems:

PRISM™ 2.4 GHz "Antenna-to-Bits" 802.11 DSSS Radio Chipset Solution.

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Abstract

The markets for mobile application-specific devices and general purpose laptop personal computers promise great fortune for those providers who drive Wireless Lan cost and performance. Unfortunately the lack of Wireless Lan industry standards has slowed the development of integrated chipset solutions. However, a complete "antenna-to-bits" 802.11 draft DSSS compliant chipset is available today to address many commercial applications.

The chipset utilizes a single conversion architecture minimizing external components, providing a high level of integration for 2.4GHz RF, IF and baseband functions. This paper presents a brief overview of WLAN markets and Standards, the chipset architecture, and design considerations for chipset partition. The performance and cost advantages of the chipset features will also be discussed including: low voltage operation, programmable data rates, BPSK and QPSK modulation, antenna diversity, programmable PN code, and PCMCIA compatibility.

I. Introduction

Our desire for better and faster information seems to be growing at an astonishing rate in the last 10-12 years. With mobile electronic information tools and communication devices now ubiquitous in most modern societies, our expectations for untethered information systems (UIS) is becoming the norm. Although the masses of the world do not even have access to a telephone, millions of people in North America, Asia, and Europe could not conceive of life without cordless phones, cellular telecommunication, or laptop computing devices.

Wireless data systems, only a half dozen years in existence, are quickly developing to satisfy this UIS appetite in every day life applications. Business week recently reported a SmartCart, developed by Klever Marketing, Inc., Salt Lake City, UT., will put product advertisements, price, and location information in the hands of grocery shopping customers. With a touch of a button, the shopping cart display unit provides the store's point of sale computer network information, including price scanning, to the customer's cart in any part of the store. Product specials and advertisements are displayed as shoppers stroll throughout the store. Most major rental car companies now process your express reservations and checkout in an instant with application specific wireless data terminals in courtesy buses and parking lots. These devices display and process customer order and billing information from the terminal's main computers via wireless local area network (WLAN) connection. Many major department and discount stores now perform all inventory verification with application specific wireless data terminals tied into the store's WLAN.

II. Wireless Data Markets

While these wireless data 'vertical market' applications have been instrumental in transforming work processes in many cases, each application is highly specialized with significant costs, relatively low levels of component integration, and rely on proprietary, non-interoperable technolo-

gies. The UIS appetite is far from satisfied without addressing 'horizontal market' demands. UIS is slowly spreading to the offices, universities, hospitals, warehouses, small offices, and home offices. Enterprise wide wireless data networks will untether office workers, institutional professionals, and university students in the same way mobile computing and communication did a dozen years ago for field service and sales people. Warehouse operators are already outfitting forklift trucks with laptop computers equipped with bar scanning devices. Inventory control and location tracking information is immediately transmitted via WLAN to the warehouse information systems for processing, archive, and future dispatch instructions to forklift drivers. Students and professors will access databases, email, and other network services from any classroom or laboratory. Doctors and nurses will update and retrieve patient information at a patient's bedside. Engineers will be able to access drawings and bill of material information on the manufacturing floor or conference room. Mobility will take on a whole new meaning as office workers share information and files with interoperable wireless LAN adapter cards inserted in the PCMCIA interface slot of their personal digital assistant (PDA). Email and faxes will be sent and received anywhere on campus.

According to Data Quest, the PC based Wireless LAN market compounded average growth rate is 113% to calendar year 1999. This phenomenal growth rate will push the world wide shipments of Wireless LAN products to $2 billion by 2002. Great fortune can be predicted to those providers who drive Wireless LAN cost and performance. "The needs for mobility are significantly increasing and the cost of the technology is falling due to integration", according to Jon Edney of InTalk, Inc. "As these factors of demand and cost meet, there will be a rapid growth in the market." InTalk plans to use Harris Semiconductor's PRISM™ chipset for a range of mixed media wireless office appliances and portable devices incorporating data, voice, and video capability.

III. Standards Enable the Markets

One of the key elements enabling the horizontal market is WLAN interoperability standards. Standards usually drive lower prices through high volume standard chipsets rather than expensive, proprietary IC technologies. Standards should mean you can use a compliant product from any vendor and it will be interoperable with any other vendor. Standards tend to drive volume sales, encouraging IC vendors to strive for high levels of radio integration and lower costs. IC vendors must chase volume applications to liquidate the high capital costs of IC manufacturing, and to further reduce the cost/price per unit. This in turn brings down the cost of systems enough to enable a larger number of end users. We are very familiar with the cost/price curves of virtually all electronic devices over 3-5 years.

IV. IEEE 802.11 Standard

The IEEE 802.11 Global Standard for Wireless Data has been in committee development for several years. The 802.11 committee continues to refine the Media Access Control (MAC) and Physical (PHY) layers of the network. However, the IEEE 802.11 standard has been finalized to the extent necessary for IC vendors to build PHY and MAC chipsets, resulting in working draft compliant evaluation radios available for WLAN system integrators today.

IEEE 802.11 Standards provides the following key rules and guidelines for Wireless Data Systems:

A. Media Access Control (MAC)

Much like wired Ethernet, IEEE 802.11 utilizes a shared media protocol known as carrier sense, multiple access, collision avoidance (CSMA/CA). The chance of wireless nodes colliding is minimized by first sending a short ready to send (RTS) message which tells other nodes the message duration and intended destination. This allows other nodes to hold their transmission for the duration of the active RTS signal. The receiving station then must issue a clear to send (CTS). This lets the transmitting node know that the medium is clear and the receiving station is ready to listen. After the data frame is received the receiver must then issue an acknowledgment (ACK) to verify the data frame

was received without error. If an ACK is not received, an attempt to transmit the data frame is repeated by the transmitter.

B. Physical Layer (PHY)

The physical layer specifications include two RF spread spectrum technologies and one Infrared technology. Spread spectrum radio technology reduces the average power spectral density by spreading radio energy over a much wider bandwidth than necessary for the desired data rate. This reduces transmitted power to keep users from interfering with others in the band. Both RF technologies use 83 MHz of the 2.4 GHz industrial, scientific and medical (ISM) unlicensed band. Operation of RF spread spectrum devices in this 2.4000 - 2.4835 GHz band is governed by FCC specification 15.247 part 15.

i. Frequency Hopping (FH)

The frequency hopping (FH) physical layer uses a transmitter and receiver predefined pseudorandom hopping pattern which must hop across 75, 1MHz frequency slots at least once every 400ms. Three sets of 22 hopping patterns are defined in the 802.11 standard. Each frequency slot must be utilized at least once every 30 seconds. Frequency hopping systems typically use Gaussian Frequency Shift Keying (GFSK) modulation. The 802.11 standard specifies that an entire data frame must be sent before it hops to another frequency. This reduces the level of interference immunity compared to the frequency diversity employed by some FH systems that spread individual data packets over the entire spectrum. Data rates for FH are typically 1Mb/second.

ii. Direct Sequence (DS)

The direct spread (DS) physical layer requires that each data bit is spread over a 22MHz slice of the ISM band by mixing (XOR) each data bit with a high rate pseudorandom "chipping code" before being PSK modulated onto the RF carrier. For interoperability, the only spreading code allowed by IEEE 802.11 is an 11 chip Barker sequence. The Barker Code is unique because no section of it matches any other part of the chip sequence unless the entire 11 chips are completely aligned. This eases the job of the DSP correlator in the despreading function of the DS receiver. Since each individual bit is transmitted and received as an 11 chip sequence spread over a 22MHz band, a narrow band noise spike in one area of the band will most likely not prohibit the pattern from being decoded by the receiver. The length of the chip sequence is directly related to the processing gain. A chip rate of 11, increases the transmission rate by a factor of 11. The more the signal is spread, the greater the processing gain, and the lower the interference from other radios. The DS physical layer partitions the 83MHz band into 11 channels with 5MHz spacing between center frequencies. Direct Spread systems utilize BPSK modulation for 1 Mbit/Second data rates, and QPSK for 2 Mbit/Second data rates.

C. Wireless Data Network Configurations

Wireless data network configurations include "ad-hoc" or peer to peer (node to node connection), and infrastructure where wireless nodes communicate with a wired LAN through access points installed throughout an enterprise or building.

D. Data Framing

Data framing specifications breaks data into blocks or packets, bundling each block with control and address information. IEEE 802.11 guidelines show a 30 byte sequence for control, addressing, data frame length, and signaling information. After this information, the actual data follows ranging to a maximum of 2048 bytes. A 4 byte CRC error detection code ends the data frame sequence. IEEE 802.11 recommended data packet size is 400 bytes for FH radios and 1500 or 2048 bytes for DS radios. Implementing this recommendation means that FH systems will add significantly to the overhead required when transmitting long data packets.

E. Data Security

Data security includes authentication for making sure a node joining the network is authorized to do so, and privacy data encryption to prohibit unauthorized listening on the network. The encryption scheme specified can be characterized as moderately secure to assure there is no violation of US export licensing restrictions in the world wide standard.

F. Power Management

Provisions in 802.11 for power management allow inactive nodes to "sleep" and only "wake up" periodically to receive a beacon indicating the nodes for which data is waiting to be transferred.

G. Roaming

Roaming rules allow a node to "roam" between network access points. When a node experiences a weak signal from its current access point, it will look for a stronger signal from another one. If a new link is established all data then is transmitted through the new access point. IEEE 802.11 does not specify how a node chooses a unique access point. It leaves this up to system designers to come up with their own decision algorithm.

V. PRISM™ Chipset - A Complete "Antenna-to-Bits" Radio Solution

A spread spectrum integrated circuit (IC) IEEE 802.11 chip set can be a key enabler to the growth of wireless data systems. A PCMCIA Type II compatible chipset will provide UIS designers a significant advantage in board space, design time to market, and development costs. An effective chipset solution must offer flexibility for implementation of IEEE 802.11 standards as well as the ability to provide cost effective solutions in alternative application specific wireless data systems.

Harris Semiconductor's PRISM™ chipset for 2.4 GHz 802.11 compliant radios, and other RF modems employing Direct Sequence Spread Spectrum (DSSS) RF technology, offers a highly integrated cost effective solution for wireless data system designers. Shown in Fig. 1, PRISM™ is the first RF through baseband DSSS chipset solution targeted specifically to the nearly complete IEEE 802.11 WLAN Standard. An integrated chipset radio solution offers a designer a simplified product design, speeding time to market and reducing system costs. The single power supply (2.7v-5.5v) chipset designed together to provide all RF, IF and Baseband functions, virtually eliminates all passive tuning elements and signal interface "glue" common in many of today's radio

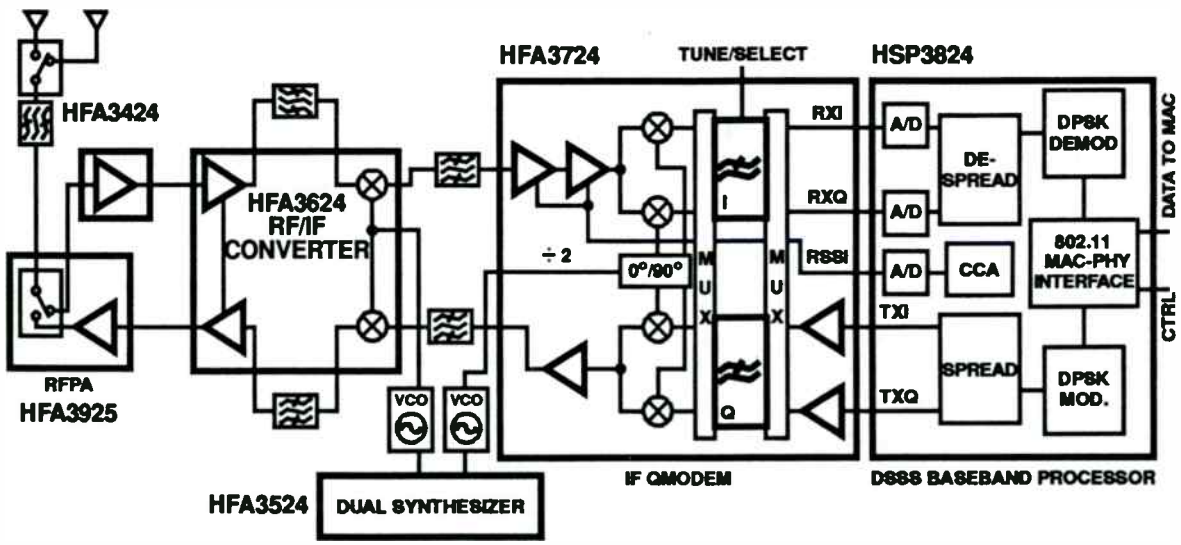

FIG. 1 PRISM™ Radio Architecture

designs. This is a real manufacturing cost advantage when considering component costs, testability, and first pass manufacturing yields.

The PRISM™ chipset can achieve data rates up to 4 Mbit/second, yet also implements the IEEE 802.11 proposed 2 Mbit/second DS Physical Layer (DS-PHY) standard with ease. The radio architecture reflects a single heterodyne IF down conversion from 2.4GHz to an intermediate IF frequency (10MHz - 400MHz). IF is then converted into In phase (I) and Quadrature (Q) baseband components. The signal is then despread into its original spectrum and demodulated packetized bit stream in the DSP Baseband Processor function.The DSP Baseband Processor provides antenna diversity implementation decision logic, and each IC in the chipset offers power management control.

VI. Radio Features

The chipset architecture and objective specifications were driven largely by a desired list of radio features. Several of the more important features and/or categories of features include: Size, Cost, and Power; IEEE 802.11 Compliance; Performance; and Flexibility.

A. Size, Cost and Power

Because many systems will be used with notebook computers and/or handheld computers, size, power consumption, and cost are all key drivers. A single conversion architecture was chosen with all three factors in mind. More than one conversion would require additional local oscillators, IF filters, and additional amplifier stages.

Certain system and chip level design objectives were chosen to minimize the cost of the external filters needed to realize the complete radio. For instance, the signal path off chip is designed to be single-ended to take advantage of readily available, inexpensive filters. Other examples include allowing for enough front-end gain in the chipset to accommodate moderate IF filter losses, and designing for a high IF frequency, up to 400 MHz, to ease the front-end image filtering requirements.

The selection of PCMCIA type II compliant low cost plastic packaging for each of the chips was another key design consideration for both size and cost.

Finally, power consumption was addressed through establishing a supply current budget for the radio and each of the chips, designing for low voltage operation, down to 2.7V, and by including on chip power down control logic for each of the circuits.

B. IEEE 802.11 Compliance

Compliance to the IEEE 802.11 standard brings with it the benefit of interoperability. In addition, there are no licenses required for operation in the 2.4GHz ISM frequency band (2.4 - 2.483GHz), and no service provider fees required for air time. Although the IEEE 802.11 specification is complex, a few of the key physical layer requirements and how these influenced the system design objectives merit consideration.

On the receive side, the required sensitivity is -80dBm for a frame error rate (FER) of $8 \cdot 10^{-2}$, using differential quadrature (DQPSK) modulation. With a bit to noise energy ratio (E_b/N_0) of approximately 16dB to meet the required FER, a front-end noise figure of 18dB is needed. In our implementation however, the goal for receiver sensitivity was -90dBm (to allow for greater range with a given transmit power), requiring a front-end noise figure of 8dB. Since there is approximately 3.5dB of loss before the active receive components, the receive noise figure requirement at the low noise amplifier is actually 4.5dB.

On the transmit side, the desired output power is +16.5dBm. Since there is approximately 3.5dB of loss after the power amplifier, the amplifier must operate at +20dBm. After allowing for 3 to 4dB of back-off from its 1dB compression point, the required amplifier compression point is +23 to +24dBm. Also, the transmit spectral mask requires the first sidelobe of the PSK signal to be suppressed at least 30dB with respect to the main-lobe. An unfil-

tered PSK signal would have the first sidelobe only 13dB below the main-lobe. This requirement drives the choice of the baseband transmit low pass filter, and sets the amount of back-off from compression allowable in the transmit chain.

C. Performance

In addition to the radio features discussed thus far, certain performance parameters such as range, throughput, and interference immunity were also considered important. A consideration of these factors led to the selection of the direct sequence (DS) architecture as shown in Fig. 1.

The receiver employs limiting IF processing, and analog demodulation to baseband. Digital signal processing (DSP) is used to despread and demodulate the signal. Limiting IF amplifiers may be used with DS systems, and are especially suited for systems with short PN codes. With the 11 bit code specified by 802.11, the processing gain is modest, resulting in slightly positive signal to noise ratios at the limiter input while operating. As a consequence, limiting IF systems actually perform slightly better than automatic gain (AGC) IF systems in most environments. The use of limiting IF amplifiers lowers system cost and complexity, as AGC IF systems are difficult to implement in a WLAN environment where fast acquisition (less than 20 usec) of packets is required.

The transition between analog signal processing and digital signal processing was carefully chosen to exploit the advantages of DSP, while avoiding the high supply current penalty commonly associated with IF based DSP. Using low-cost DSP techniques at baseband maximizes overall system performance. For example, the second LO, used to provide quadrature demodulation in the receive path, is not part of a carrier recovery loop. Instead, a proprietary PSK demodulator achieves performance levels close to those of a complex coherent system, without the burden of an external feedback loop. The required simple fixed frequency LO is easily implemented.

Other DSP techniques that improve system performance include the despreading and demodulation scheme, which is optimized to exploit the impact of the limiting IF amplifiers. This results in improved receiver sensitivity at a given bit-error rate (BER). Further, a DSP based leveling circuit is used to provide control of the received baseband signals, maximizing the dynamic range of the A/D converters.

The transmit processing follows a similar single conversion flow. Starting at baseband, quadrature digital PSK modulated signals are generated, and then spread. The baseband signals are then low pass filtered to meet the transmit spectral mask specified in 802.11. After this filtering, the remaining transmit components must be operated in a linear fashion to avoid spectral regrowth. Quadrature IF modulation is used to convert the baseband signals to the IF frequency. A further up conversion then shifts the carrier up to the desired channel in the 2.4GHz ISM band. To develop the required output power, an integrated RF power amplifier is used. As previously discussed, this power amplifier must be operated in a linear manner, with a fixed back-off from its 1dB compression point to avoid spectral regrowth.

D. Flexibility

Realizing that one size may not fit all, additional features were incorporated in the chipset design to allow for a certain degree of flexibility in the system implementation. In fact, the degree of flexibility available is enough to enable a wide range of 802.11 compliant and non 802.11 compliant systems in the unlicensed 2.4GHz ISM band. The low power spectral density nature of DS lends itself nicely to the design of systems that are not necessarily disruptive to other narrowband or broadband communications on the same frequency.

Examples of chipset features that allow for flexible system design include the choice of two different modulation types, programmable data rates, programmable PN code length, and dual antenna diversity.

Two modulation types, differential quadrature phase shift keying (DQPSK), and differential binary phase shift keying (DBPSK), both types compliant with the 802.11 DS physical layer specifications, are supported by the baseband processor. With a maximum symbol rate as specified by 802.11 of 1Msps, the resulting data rate is 2Mbps with DQPSK, and 1Mbps with DBPSK.

The bit rate for QPSK is twice that of BPSK, but it takes 3dB more power per bit to get the same signal to noise ratio. Another way of saying this is that for a fixed transmit output power, the separation between transmitter and receiver (range) can be somewhere between 20 to 40% greater (depending on the environment) using the lower rate BPSK modulation. Of course if the added range is not needed, one can take advantage of the higher rate possible with QPSK.

Programmable data rates from 256Kbps to 4Mbps can also accommodated, though it should be noted that the 802.11 specification currently supports only the 1Mbps and 2Mbps rates. Lower data rate systems offer the advantage of increased channel capacity and extended range (or the same range with lower output power). Higher data rate systems offer the obvious advantage of speed.

The PN code length can also be programmed, to lengths of 11, 13, 15, or 16 bits, although it should be noted that for interoperability, the only code supported by 802.11 is an 11-bit Barker code. The PN code psuedorandomly chops the phase of the data into brief time intervals, called chips. These chips are several times shorter than the duration of a data bit (e.g. an 11-bit PN code results in 11 chips per data symbol). The effect is that the energy of the data is spread across a much higher bandwidth appearing very much like low level broadband noise. To despread the signal, the receiver uses an identical PN code to the one used in the transmitter.

The characteristics of the spreading code are critical because the network code set must exhibit low cross-correlation characteristics among its individual codes. For non-802.11 applications a higher bit length spreading code could be used for improved processing gain. Processing gain means that a DS receiver can recover a signal even when the interfering signal has a higher power than the spread waveform.

The chipset design also supports the use of single or dual antennas. Dual antennas can be used to combat the effects of delay spread (multipath). Delay spread is a general problem in mobile applications and in environments where there are many reflective surfaces, such as factory floors and some office environments. With PRISM™, dual antennas may be utilized at both ends of the link or only at one. In small form factor applications such as PCMCIA type II WLAN cards, systems could use a single antenna on the PC card and antenna diversity on the access point or base station.

In designs that take advantage of antenna diversity, a low loss diversity switch follows the antennas, Antenna selection is completely automated by the baseband processor and takes place during the preamble of each packet.

VII. Process Technologies

The chipset partitioning was heavily influenced by the available process technologies. In this case, there were a wide range of available technologies including a GaAs MESFET process, a high speed silicon bipolar process, two separate mixed signal BiCMOS processes, and a digital CMOS process. Similar frequency processing was grouped together so that the process most appropriate for a given frequency could be optimally chosen. Also since the system operates in a half-duplex mode, transmit and receive functions could be placed on the same die, with little concern for isolation.

A GaAs MESFET process, appropriate for small level integration, was used for the integrated Power Amplifier and T/R switch. The same process, with its low noise figure devices, is also used for an optional LNA which precedes the RF/IF Converter.

A high speed silicon bipolar process (UHF1X), with an NPN fmax of 13GHz, and a PNP fmax of 7GHz was used for the RF/IF Converter and for the IF QMODEM. This complementary process is built using dielectrically isolated, bonded wafer techniques. By controlling the features of the substrate, the high frequency losses commonly associated with silicon are minimized.

A high speed BiCMOS process, suited to medium and large scale integration, with fast bipolar and dense CMOS logic, was used for the dual synthesizer.

A digital CMOS process, with high density 0.6 micron triple level metal technology, was chosen for the integration of the DSP intensive DSSS Baseband Processor.

VIII. Description of Major Blocks

A. RF/IF Converter (HFA3624)

The integrated RF/IF Converter incorporates on-chip spiral inductors and MOS capacitors to provide 50 ohm internal matching on all high frequency ports, as well as higher impedances for the IF ports, thus supporting simple connection to IF filters. No IF baluns are required. One LO input is needed, with internal connections between the transmit and receive mixers. The IF passband extends well beyond 400MHz.

In the receive path, a two-stage LNA establishes the receiver noise figure. An optional external image rejection filter can enhance overall system sensitivity. The single-balanced receive mixer is optimized for high conversion gain, low noise figure, and high third-order intercept. The IF output is a differential structure that supports IF impedance-matching networks. Optionally, the IF output can be used in a single-ended fashion.

In the transmit path, the RF/IF Converter uses a double-balanced up-conversion mixer to minimize the amount of LO leakage in the transmit output. The chip allows use of an external sideband selection filter, with characteristics similar to those in the receive image-reject filter. An on-chip two-stage exciter amplifier eases RF power amplifier gain requirements.

The RF/IF Converter is partitioned separately from the IF sections to allow for high isolation in the receive IF filter. The off-chip image filters associated with the RF/IF converter require only modest isolation for proper operation.

B. IF Filtering

Both the receive and transmit IF paths use filtering. A highly selective SAW filter provides receiver selectivity. At the recommended 280MHz IF, and an 11Mcps chipping rate, the filter bandwidth should be approximately 17MHz. Insertion loss should be less than 15dB, and differential group delay should be less than 100ns.

C. Dual Synthesizer (HFA3524)

In both transmit and receive a dual-frequency synthesizer provides the LO signal for both the RF/IF Converter and the phase splitter in the IF QMODEM. By maintaining identical IF frequencies in both transmit and receive paths there is no frequency switching and therefore no settling time requirements. This enhances transmit/receive turnaround time, a key issue in carrier sense multiple access (CSMA) data applications.

D. RF Power Amplifier (HFA3925)

The linear RF power amplifier provides matched 50 ohm characteristic impedances and provides a +23dBm 1dB compression point. To limit spectral regrowth, the amplifier operates 3dB below the 1dB compression point. Assuming 3.5dB insertion loss for the antenna diversity scheme, +16.5dBm of transmit power is available at the antenna.

The RF power amplifier together with the T/R switch is partitioned as a separate IC due to thermal issues, as well as the large signal nature of the circuit.

E. IF QMODEM (HFA3724)

In the IF QMODEM, a two-stage limiting amplifier in the receive path provides sufficient gain and bandwidth to exhibit a -84dBm -3dB limiting sensitivity at frequencies up to 400MHz. The limited output is typically 200mV, and is compensated over temperature. An internal RSSI (Received Signal Strength Indicator) provides linear temperature-compensated performance. The RSSI signal is routed to the internal 6-bit RSSI A/D converter on the baseband processor, where it is used for Clear Channel Assessment (CCA).

Following limiting, the IF signal is routed to a quadrature demodulator featuring an internal, quadrature LO network that achieves accurate phase performance. The quadrature network utilizes a divide-by-two approach to achieve broadband operation. Feedback circuits maintain phase accuracy over a wide range of LO input levels and duty cycles. The demodulator input compression point exceeds 1Vpp, making it suitable for use with the limiter output, or with any external AGC, should system designers wish to bypass the on-board limiters. The I/Q baseband signals exhibit ±0. 6 degree phase balance and ±0.2 dB amplitude balance. On the transmit side, the quadrature modulator utilizes the same quadrature LO network and provides an accurate IF output from 10 to 400MHz. As a result of the excellent phase and amplitude balance, sideband suppression in a single sideband (SSB) operating mode is typically 33dB.

The IF QMODEM also provides programmable baseband I and Q low pass filtering. Dual fifth-order Butterworth filters are internally multiplexed between the transmit and receive channels. These filters offer four digitally-selectable cutoffs: 2.2, 4.4, 8.8, and 17.6 MHz. These cutoffs correspond to DS chip rates of 2.75, 5.5, 11, and 22Mcps. In addition, the filters may be tuned up to 20% above or below the fixed cutoffs by changing an external resistor. The filter response was selected to meet the transmit spectral mask requirements. Specifically, the first side-lobe attenuation of the transmitted spread DBPSK or DQPSK signal is typically -35dBc relative to the main-lobe. In receive mode, the demodulated, filtered I and Q signals are routed to the baseband processor. In transmit mode, the digital I and Q signals from the baseband processor feed to the IF QMODEM. To avoid spectral regrowth, once the transmit single-bit inputs are filtered by the fifth-order Butterworth filters, the rest of the transmit chain must operate linearly. In other words, all further transmit elements must be operated backed-off from their 1dB compression points. Despite this characteristic of BPSK and QPSK modulation, the improved receiver performance over simpler non-coherent modulations such as GFSK results in an overall system performance advantage, especially at high data rates.

F. DSSS Baseband Processor (HSP3824)

In the DSSS Baseband Processor, the analog I and Q signal outputs from the lowpass filters are digitized by 3-bit A/D converters at 22Msps, twice the chip rate.The quantized I and Q baseband paths are correlated against a reference PN code, using separate matched filter correlators. The reference PN code is programmable from 11 to 16 chips. The correlators despread information of interest back to its original data rate while spreading interfering signals and noise. After the despreading, the I and Q signals are converted to polar form, and the phase information is subsequently processed by the DPSK demodulator, which supports both DBPSK and DQPSK. A digital phase locked carrier tracking loop allows coherent DPSK data processing. In the transmit mode, the baseband processor functions as a DPSK modulator, including a data scrambler, and a BPSK spread modulator. Serial data and control ports allow for flexible interfacing with most major controllers.

The baseband processor is partitioned as a separate IC due to the large digital content of this function.

IX. Summary

Utilizing the PRISM™ chipset in UIS designs speeds system level design time to market, reduces development costs up to 80%, and significantly

reduces manufacturing costs. UIS markets promises great fortune for those providers who drive WLAN costs and performance by implementing an effective radio chipset strategy to their early to market wireless data system design.

References

[1] M. Chian et. al., "IC Implementation Challenges of a 2.4 GHz Wireless LAN Chipset", Harris Semiconductor Technical Journal, vol 2 number 1, July-September 1996, pp. 5-19.

[2] J. Fakatselis, and A. Petrick, "System Considerations in Spread Spectrum Designs", Wireless Design and Development, July 6, 1995.

[3] A. Kamerman, "Spread Spectrum Techniques Drive WLAN Performance", Microwaves and RF, September 1996.

[4] L Goldberg, "Wireless LANs: Mobile Computing's Second Wave", Electronic Design, June 26, 1995.

[5] C. Castillo, "Wireless LAN Industry Leaders Establish Consortium", WLANA Press Release, San Jose, CA, March 25, 1996.

[6] C. Andren, "A Brief Tutorial on Spread Spectrum and Packet Radio", Harris Semiconductor Tech Brief, No. TB337.1, May 1996.

[7] K Sullivan, "Wireless Networks Spread Their Wings", PC Week, October 9, 1996.

[8] A. Petrick, J. Fakatselis, and C. Andren, "Integrated RF and DSP Solution Simplifies DSSS Architecture for the emerging IEEE802.11 WLAN Standard", DSP & Multimedia Technology, May/June 1996.

[9] I. Wickelgren, "Local-area Networks Go Wireless"', IEEE Spectrum, September 1996.

[10] W. Kilgore, A. Petrick, and D. Schultz, "Four-Chip Set Supports High-Speed DSSS PCMCIA Applications", RF Design, October 1995.

[11] B. Razavi, "Challenges in Portable RF Transceiver Design", Circuits and Devices, September 1996.

GaAs MMICs for 5.2GHz HIPERLAN

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Abstract

HIPERLAN (HIgh PErformance Radio Local Area Networks) is an emerging European standard for wireless local area networks with an in air data rate of 23.5 Mbits/sec. This paper details the design manufacture and measured performance of two application specific GaAs MMICs which form the majority of the 5.2 GHz RF front end. One MMIC is a power amplifier with level control and the other is an up/down-converter with on chip VCO. These are the first GaAs MMICs designed specifically for the HIPERLAN standard.

I Introduction

The European Telecommunication Institute, ETSI is looking towards the future of wireless data communication and is working on a standard for High Performance Radio Local Area Networks (HIPERLAN) [1]. The first HIPERLAN standard (Type 1) due to be published in late 1996 defines a system which will support data rates up to 23.5Mbit/s. Type 1 HIPERLAN uses a distributed medium access control protocol which can do away with base stations and access points. It does not however allow medium use per terminal to be scheduled since medium access is negotiated at each transmission event. This is a problem for wireless ATM. Realising this ETSI decided to develop a second standard aimed at wireless ATM access - HIPERLAN Type 2. This will be released for comment in 1997. The frequency allocations for HIPERLAN are 5.15 to 5.25GHz and 17.1 to 17.2GHz. An extension of the lower band from 5.25 to 5.3GHz will be released by individual countries based on national demand. These bands are specific to HIPERLAN in the European Union and therefore provide a more benign operating environment from the point of view of interference. Unlike the ISM bands where spread spectrum techniques are essential to make the systems interference resistant. Up to three power levels are specified: 10dBm, 20 dBm and 30 dBm. The modulation scheme chosen is GMSK which allows the use of efficient non linear power amplifiers. Since a major application of HIPERLAN will be for battery operated portable equipment DC power consumption is an important consideration. Other power saving features have also been defined in the specification.

The operating frequencies for HIPERLAN currently preclude the use of Silicon ASICs in the RF front end. The market areas that HIPERLAN is targeting (such as PCMCIA cards for personal computers) will also require very high levels of integration in order to meet the size constraints. Packaging of components at 5.2 GHz presents a problem since the low cost plastic packages used at 2.4 GHz become unusable at 5.2 GHz due to parasitic lead inductance's and the loading effect of the plastics. Multi Chip Module (MCM) technology can however provide a solution [2].

II GaAs Chip Set

Fig. 1 shows a block diagram of the RF to IF section of a HIPERLAN radio designed around a custom GaAs MMIC chip set. Two MMICs are used. An up/down converter chip that contains; IF amplifiers, T/R switching, VCO with on chip varactor and resonator, bi-directional mixer and Tx pre amplifier. The second chip is a 21 dBm power amplifier with power level control. The T/R switch and the diversity switch are realised using standard GMMT switch MMICs.

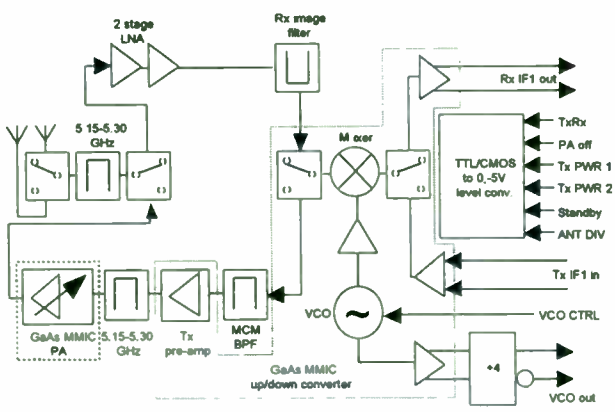

Fig. 1. HIPERLAN Front End Block Diagram

The MMICs are integrated into a multilayer MCM D substrate that provides a medium to realise lumped element and distributed microwave components for the filters and matching elements for the discrete HEMT LNA. MCM D technology allows the integration of the RF front end with CMOS control devices and a Silicon prescaler made using a 15 GHz Ft bipolar process. These can be solder bumped and flip chipped onto the substrate to form a very compact low cost assembly with good microwave performance. The MCM is assembled into a 17mm square Ball Grid Array package which can then be surface mounted with other portions of the radio on a conventional PCB. Fig 2 shows the MCMD assembly containing the GaAs MMIC chip set and the MCM LNA. Also shown next to the MCM tile is a ceramic microstrip filter linking the transceiver to the Power Amplifier.

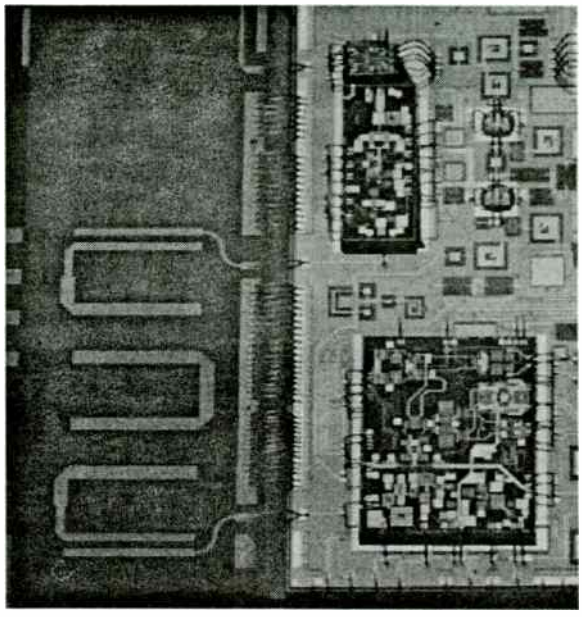

Fig. 2. MCM D Assembly

The two stage LNA utilises discrete HEMT die and MCM passive components to achieve a gain of 22 dB with a noise figure of 2 dB. This is used to buffer the noise figure of the down-converter.

The key performance requirements of the two GaAs MMICs are given below.

Power Amplifier:

Frequency	**5.15 to 5.3 GHz**
Gain	**>16 dB**
Return Losses	**>10 dB**
1 dB CP	**>21 dBm**
Psat	**23±2 dBm**
Current	**<150 mA**

Transceiver:

LO	**5.80 to 6.05 GHz**	**1 - 4 V**
RF	**5.15 to 5.30 GHz**	
Rx Gain	**>-7 dB**	
Rx Noise Figure	**<22 dB**	
Rx Input IP3	**>10 dBm**	
Rx Current	**<50 mA**	
Tx Power Out	**>9 dBm**	**300 mV IF in**
Tx spurious	**<-63 dBc**	**4.88 - 5.55 GHz**
Tx current	**<200 mA**	

Both MMICs were fabricated using the standard GMMT F20 process, which utilises 0.5 µm gate length, depletion mode MESFETs. The simple 9 mask process is ideally suited to volume manufacture of MMICs.

III Power Amplifier

Fig. 3 shows a photograph of the two stage power amplifier MMIC.

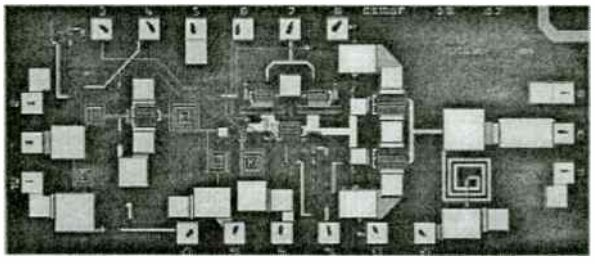

Fig. 3. Power Amplifier MMIC Photograph

The output stage is realised by two devices in parallel. A low gain / output power mode is available when an interstage attenuator is switched in. At the same time one of the two output stage FETs is pinched-off resulting in an output power reduction of around 10 dB with a 38% DC power consumption saving. The measured gain of the power amplifier is over 20 dB and both input and output return losses are greater than 17 dB. The small signal S-parameters of the power amplifier are plotted in Fig 4 and the power transfer characteristics of a sample of 24 amplifiers is shown in Fig 5.

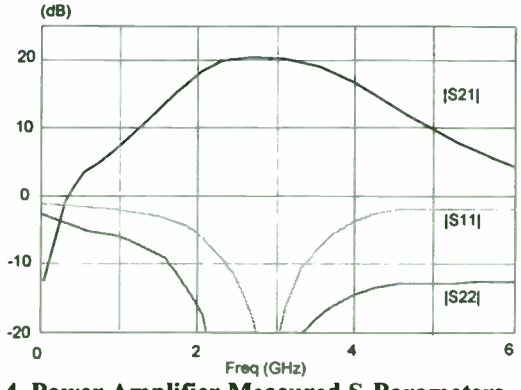

Fig. 4. Power Amplifier Measured S-Parameters

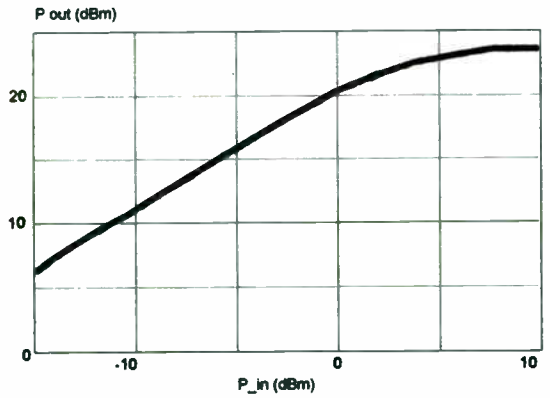

Fig. 5. Power Amplifier Power Transfer Characteristics

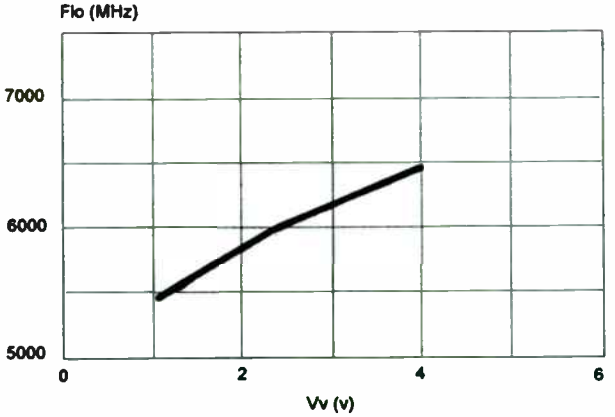

Fig. 6. VCO Tuning Characteristics

IV Transceiver

As shown in Fig. 1, the transceiver MMIC comprises a VCO, buffer amplifier, mixer, RF balun, RF and IF Tx/Rx switches, Rx and Tx IF amplifiers and a Tx RF pre-amplifier. To minimise component count, the VCO, buffer, mixer and balun are used in both transmit and receive modes. Following the MCM LNA and filter, the receive input signal is selected by the Tx/Rx switch and fed through the 180° splitter to the mixer. An IF amplifier provides the down-converted signal with gain and match to the high impedance external IF filter. In transmit operation, an IF amplifier provides a high input impedance and gain prior to up-conversion using the same LO and mixer. The mixer RF output is converted to single-ended by the RF balun. The signal is then routed off chip for USB removal before returning to the pre-amplifier contained within the same chip. The individual sub-circuits are described below.

VCO / Buffer / Mixer

The on-chip Clapp-type VCO is fully self-contained and includes the resonator and tuning varactor. This push-pull device essentially comprises two separate oscillators connected and biased through virtual earths where a corresponding single-ended oscillator would have demanded RF grounding. The varactor tuning voltage is also applied at a virtual earth. The push-pull arrangement minimises on-chip RF decoupling requirements as well as providing the differential input to the double-balanced mixer. Over the required 200 MHz bandwidth, the linearity of the VCO is better than 1.3:1. and the phase noise was measured at -133 dBc/Hz at 10 MHz offset. The VCO consumes approximately 25 mA. The tuning Characreristics of the oscillator are shown in Fig 6.

The buffer amplifier is required to provide a differential sample of the on-chip LO signal to allow external phase locking. It is also required to isolate the VCO from the loading and possible pulling effects of the phase locked loop (PLL). The buffer amplifier Consists of a long-tailed pair of small FETs, biased by a current source. No input matching is used in order to present a high input impedance to the VCO. Reactive matching is used at the output to provide a good match and thereby power gain. The current drawn by the buffer amplifier is ~7 mA.

The double-balanced mixer is formed by a quad ring of FETs. With differential signals at RF, LO and IF ports, each port is a virtual earth of the other two. The gates are driven by the differential output of the VCO. A 200 Ω resistor across the LO input reduces the LO voltage available to the gates but reduces the pulling effect of Tx/Rx switching at the RF and IF ports.

Diplexer / IF Amplifiers

The IF side of the mixer is connected to the Tx/Rx switches by means of a diplexer filter. This assures a resistive termination at LO, RF, image, 2LO, 2RF etc., minimising VCO pulling and controlling intermodulation.

The IF amplifiers are essentially low-pass in design, i.e. unmatched, since it is not practical to provide reactive matching on-chip at 700 MHz. The low frequency cut-off is determined by the coupling and active load bias capacitors. The Rx IF amplifier is a single stage with approximately 7 dB gain when conjugately matched (~600 Ω) to the external IF filter and consumes 13 mA.

The Tx IFA is similar in design but has two stages with an inter-stage variable attenuator included to control the IF power into the mixer to ensure linearity. Differentially measured s-parameters of the Tx IF

amplifiers are shown in Fig 7. Allowing for the difference between the sub-circuit measurement system impedance and the amplifier input impedance, show the IFA provides 18 dB gain. 13 dB of gain control is available by means of the voltage-variable attenuator. The Tx IF amplifier draws 63 mA and has a 1 dB compression point of just under 10 dBm.

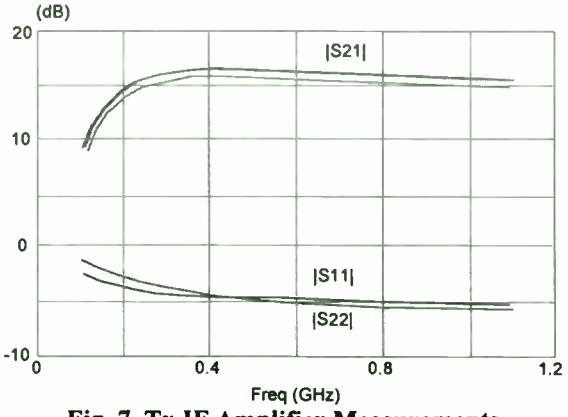

Fig. 7. Tx IF Amplifier Measurements

RF Balun / Tx Pre-Amplifier

A 180° splitter/ combiner is formed by combination of a lumped element Wilkinson splitter/ combiner and high and low pass filter sections. This is used in Rx and Tx modes to generate a differential signal for down-conversion and a single-ended up-converted signal respectively. The RF pre-amplifier is used to boost the level of the up-converted mixer output. The amplifier is realised as a three stage reactively matched circuit. The measured S-Parameters of the pre -amplifier sub circuit are shown in Fig 8. Gain is ~27 dB at 5.2 GHz and nearly 10 dB down at the lowest frequency of the (unwanted) USB. Return losses are better than 13 dB over the required RF range. The pre-amplifier has a 1 dB compression point of 19 dBm and a saturated output power of 20.5 dBm while drawing less than 90 mA.

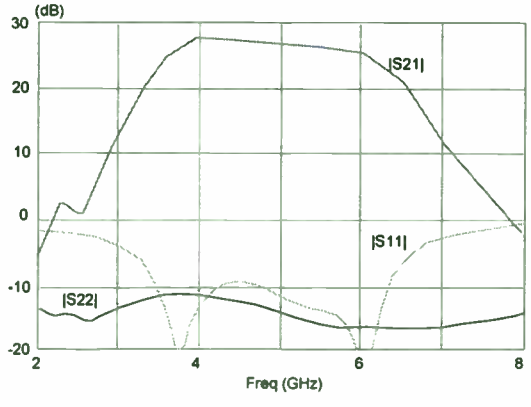

Fig. 8. Tx RF Pre-Amplifier Measurements

The sub-circuits are interconnected into a single MMIC, Fig. 9. On chip bias networks are included. These allow the Tx, Rx and common circuits to be independently enabled by means of single-ended 0/ -5 V controls at about 0.4 mA each when on. In the standby mode with all control inputs at -5 V, the total current drawn by the MMIC from the fixed +5 and -5 V supplies is < 1 mA and <0.2 mA respectively.

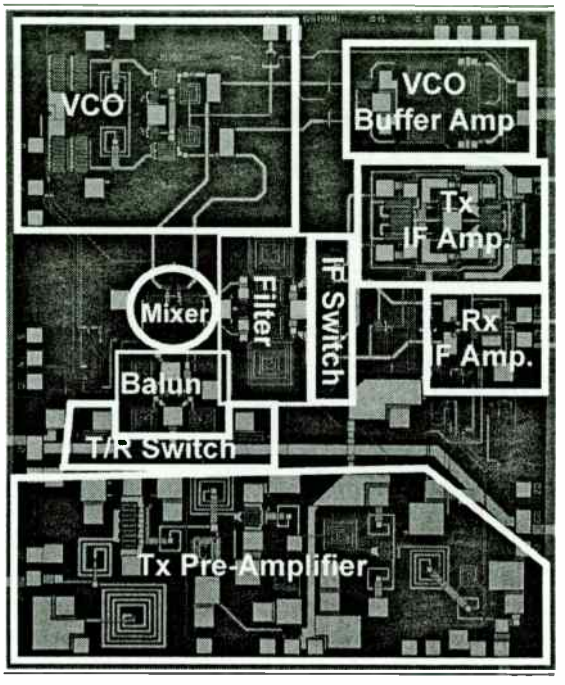

Fig. 9. Transceiver MMIC Photograph

The down-converter is designed to have conversion loss. Fig. 10 shows the conversion loss of a random sample of down-converters measured directly on wafer. The measured conversion loss is 8 dB, this improves to 6 dB when the IF outputs are conjugately matched, as will happen in practice.

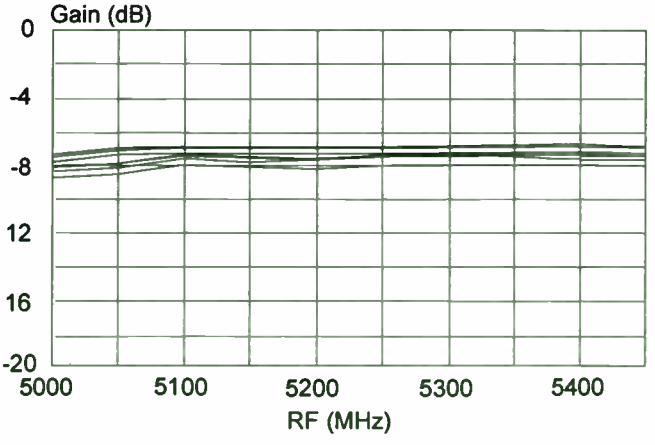

Fig. 10. Transceiver Rx Conversion Loss

In transmit mode, the up-converter has an output power of over 10 dBm for an input of -13 dBm (Fig. 11). When integrated into the MCM, this output is filtered and is then used to drive the PA MMIC. After filtering there will still be sufficient power to drive the PA into saturation, providing +23 dBm of output power.

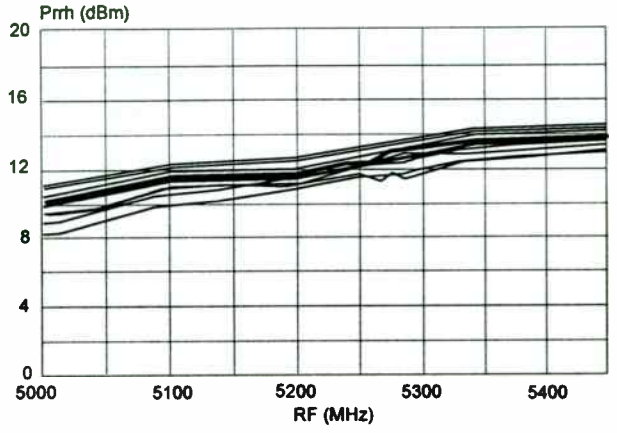

Fig. 11. Transceiver Tx Output Power

Fig. 12 shows a typical output spectrum of the transceiver, without any additional filtering. All spurious signals are at least 20 dB below the wanted signal, with the LO at -28 dBc. This is a reflection of the excellent balance of the VCO and mixer. In band spurious signals are at -70 dBc which is due to both a good choice of IF frequency (resulting in only very high order spurs. falling in-band) and the IF amplifier operating sufficiently linearly so as not to generate large harmonic tones.

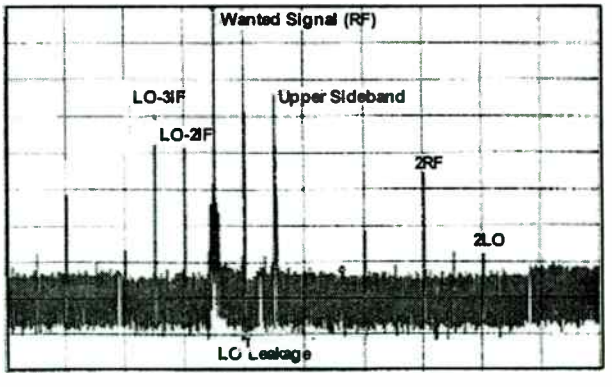

Fig. 12. Transceiver Output, 0 to 15 GHz

A consequence of the incorporation of the MMICs into MCMs is that full on-wafer RF measurement of the MMICs is necessary to select known good die. With the up/down-converter MMIC, a set of custom mixed RF and DC probes are used for this purpose. Differential probes are used to interface to the IF input and output. These are matched to a differential impedance of 200Ω. To reduce the number of separate measurements to be made, the up-converter output is connected to the pre-amplifier input by means of a track through the saw lane on the wafer. This track is severed at die separation, but allows the whole transmit chain to be checked with a single measurement at the wafer stage.

V Conclusions

A power amplifier and highly integrated transceiver MMICs have been manufactured in a single design cycle. The functionality of the sub-circuits is very close to the target requirements with the result that the integrated transceiver operates to specification. On-wafer measurement of circuit RF functionality allows selection of known good die for incorporation into a Multi-Chip Module.

VI Acknowledgements

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The HIPERLAN development was carried out under subcontract to GEC Plessey Semiconductors as part of the HIPERION project which has received funding from the European Commission (EC ESPRIT project No. 9166).

VII References

[1] J Kruys, " Wireless ATM - tales of a marriage" Proceedings of "Microwaves and RF 96", pp 24-31,

[2] C Faulkner et al, " MCM Based Radio Solutions for Wireless LAN" Proceedings of "Microwaves and RF 96", pp 33-38,

Proposed IEEE802.11 Direct Sequence Spread Spectrum Physical Layer Characteristics

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ABSTRACT

This paper gives a broad overview of the proposed RF waveforms to be utilized for Wireless LAN's as defined in the proposed IEEE802.11 standard. It provides a brief background of the ISM band and of Spread Spectrum waveforms. Details of the RF specifications for Direct Sequence Spread Spectrum is then described. It addresses implementation specifications as well as international regulatory rules. The standard is based on a CSMA/CA protocol and defines two RF waveforms for the transmissions of the packets. The two waveforms are Frequency Hop (FH) and Direct Sequence (DS) Spread Spectrum signals. The allocated band is the unlicensed 2.4 GHz ISM band. Spread Spectrum techniques appear to have desirable performance properties as well as being within the regulatory transmission restrictions for various countries.

I. INTRODUCTION

The IEEE802.11 committee has been chartered to define a standard for wireless LAN's. At the time of this paper the standard has not been completed. It is being finalized and is undergoing the steps of the IEEE approval cycle. Any reference to the standard is based on the latest available draft of the IEEE802.11 working group (Draft 5.1).
The two RF waveforms defined by IEEE802.11 are Frequency Hop (FH) and Direct Sequence (DS) Spread Spectrum signals. This paper will overview both and will concentrate on the RF requirements of the DS waveform. Harris Semiconductor has proved feasibility of the DS requirements by designing PRISM™, which is a DS radio chip set.

Spread Spectrum techniques "spread" the signal energy over a wide frequency range. The two spread spectrum waveforms chosen for the standard are :

A. Frequency Hop (FH).

FH is constantly switching its instantaneous transmit frequency in time at a minimum rate of 1 hop/sec. The FH system follows a pseudorandom sequence of frequencies. This pseudorandom sequence is known to the receiver and synchronizes to it for successful demodulation. FH systems average the total energy in time throughout the overall frequency band.

B. Direct Sequence (DS).

DS is spreading the narrowband energy by switching the phase of each actual bit with a "spreading code" running at a rate that is at least 10 times faster than the data rate. The spreading code is once again a pseudorandom sequence and the receiver needs to synchronize to it for successful demodulation. The channels of operation have been selected to meet requirements of the various international regulatory bodies.

II. BACKGROUND

Spread spectrum technology has been around for many decades. It was initially developed for government defense communications systems. Today this technology is being used in modern radio design for unlicensed commercial application, and has been positioned as an alternative to frequency bands requiring licenses. The knowledge gained over the years using this technology for government use, has led to the spawning of a number of start-up companies pioneering proprietary spread spectrum radio transceivers for the marketplace. The demand for this technology did not expand commercially until the late 1980's. In 1983 when the U.S. Federal Communication Commission (FCC) made changes to the spectrum allocation and opened three frequency bands, 902-928 MHz, 2400-2483.5 MHz, and 5728-5750 MHz. These frequencies were defined as the Industrial Scientific and Medical (ISM) band and reserved for unlicensed users with

transmit power restriction set by the provision of Rule 15.247. Much of the commercial equipment manufactured today is made to operate in the 900 MHz band.

In recent years, the 900 MHz ISM band has been troubled with user overcrowding and interfering congestion. Much of the overcrowding was attributed to inadequate spectrum allocation, and the lack of standards and interoperability. It is apparent that the 900 MHz band was the 1st generation or trial band for this technology. Unfortunately this band suffers from spectral efficiency because of the number of users which coexist. In the last few years, the overcrowded 900 MHz band has challenged the equipment and semiconductor manufacturers of this technology to start a 2nd generation of products, by migrating to the 2.4 GHz band. The 2.4 GHz band offers more spectrum bandwidth, permits higher data rates with substantial reduction in implementation size and power. Most importantly, this band will promote standards and protocols which will be the roadmap of global representation. Much of the credit in this effort is given to the work of the IEEE802.11 WLAN standards committee having as a goal to set the basis for interoperability between the various vendors and well defined communication protocols. IEEE802.11 introduces Spread Spectrum as the form of RF WLAN communications.

III. SPREAD SPECTRUM COMMUNICATIONS OVERVIEW.

Spread spectrum communication systems utilize a transmission frequency bandwidth that is much wider than the actual data bandwidth (BW). Spread spectrum is attractive to military users for the following fundamental reasons.

- It can provide Low Probability of Interception (LPI).
- It has Anti Jamming (AJ) properties.
- It can allow for simultaneous multiple signal access.

In addition, it has inherent properties of secure communications, making it difficult for adversaries to recover the signal intelligence even if they are capable of detecting the presence of such signals. Spread spectrum techniques to find their way into commercial applications. The benefits that commercial users are deriving are parallel to those that motivated the military users. If we attempt to define a parallel set of benefits that Spread spectrum systems offer to the commercial environment , they are:

A. Low transmit power density function per Hertz.

This helps the spectral contamination issue making it easier to comply with regulatory requirements. In addition, the interference generated from each operating channel to others is reduced.

B. Interference rejection capability.

This provides a performance advantage over classical narrowband transmissions due to the fact that spread spectrum systems are more immune to interference sources.

C. Simultaneous multiple system transmissions over the same frequency bandwidth.

This allows for code division multiplexing schemes that allow for simultaneous transmission of more than one signals.

Communication security or less expensive privacy protection aspects are also important to commercial networks. The primary spread spectrum waveforms are Frequency Hoping (FH) and Direct Sequence (DS) spread spectrum. Both of these techniques capitalize on the utilization of a wide frequency bandwidth for their communications in order to extract the stated benefits.

IV. WORLDWIDE REGULATORY BODIES AND DOCUMENT SUMMARY.

The various countries have adapted their own set of regulatory rules for the ISM band around which the IEEE802.11 is developed. The working group, as part of the standard development process, has considered the variations of the regulations per geographical area. The documents listed on Table 1 below have been used as reference for the current regulatory requirements for various geographic areas at the time that the standard was developed. This set of documents are provided for information only. The table is a sample of some geographies and it should be understood that the references are subject to change or revision at any time.

TABLE 1. REFERENCE TO REGULATORY AUTHORITIES/DOCUMENTS

EUROPE
Approval Standards: European Telecommunications Standards Institute
Documents: ETS 300-328, ETS 300-339
Approval Authority: National Type Approval Authorities

FRANCE
Approval Standards: La Reglementation en France por les Equipements fonctionnant dans la bande de frequences 2.4 GHz "RLAN-Radio Local Area Network"
Documents: SP/DGPT/ATAS/23, ETS 300-328, ETS 300-339
Approval Authority: Direction Generale des Postes et Telecommunications

JAPAN
Approval Standards: Research and Development Center for Radio Communications (RCR)
Documents: RCR STD-33A
Approval Authority: Ministry of Telecommunications (MKK)

NORTH AMERICA
Approval Standards: Industry Canada (IC), Canada
Documents: GL36
Federal Communications Commission (FCC), USA
Documents: CFR47, Part 15, Sections 15.205, 15.209, 15.247.
Approval Authority: Industry Canada (Canada), FCC (USA)

SPAIN
Approval Standards: Supplemento Del Numero 164 Del Boletin Oficial Del Estado (Published 10 July 91, Revised 25 June 93)
Documents: ETS 300-328, ETS 300-339
Approval Authority: Cuadro Nacional De Atribucion De Frecuesias

V. RF FREQUENCY RANGES AND BANDWIDTH.

Even though most geographic areas allow operation at the 2.4 GHz band, the exact frequencies and bandwidth allocation vary per each area. Table 2 below illustrates an example of the allocated frequency bands for selected geographies:

TABLE 2. FREQUENCY ALLOCATION TABLE

FREQUENCY RANGES	GEOGRAPHICAL AREA
2.400-2.4835 GHz	North America
2.400-2.4835 GHz	Europe
2.471-2.497 GHz	Japan
2.445-2.475 GHz	Spain
2.4465-2.4835 GHz	France

The total bandwidth allocated is of significant importance because it defines the number of channels that can be utilized at each geographical area. The same IEEE802.11 standard can be more versatile in areas that there is additional overall bandwidth allocated. The advantage is due to the greater number of channels that can be potentially deployed.

VI. DS RF POWER REQUIREMENTS.

In addition to the frequency and bandwidth allocation one key parameter that is regulated by the various authorities is the allowable transmit output power. The transmit output power is directly related with the range of coverage that a particular radio can achieve. Even though the more the power the larger the range, there are power (DC) consumption and cost implications that the industry would have to trade even if regulators were to allow liberal power transmission levels. Table 3 below illustrates a sample of allowable power output levels for selected geographies.

TABLE 3. Tx POWER REQUIREMENTS.

MAXIMUM ALLOWABLE POWER	GEOGRAPHICAL AREA
1000 mw	USA
100 mw (EIRP)	EUROPE
10 mw/Mhz	JAPAN

VII. PROCESSING GAIN.

One other key parameter that is regulated is processing gain. Processing gain is what distinguishes spread spectrum waveforms from their narrowband counterparts. Processing gain provides spread spectrum waveforms with properties that result, among other things, additional immunity to interference and low power spectral density. In the case of the DS waveform processing gain is defined as the ratio of the spread BW over the data BW expressed in dB. The FCC defines processing gain for a DS system to be a minimum of 10 dB. Even though the greater the processing gain the better its outcome benefits, there is a BW trade off and design complexity that needs consideration. High processing gain systems occupy more total BW together with a proportional increase in implementation complexity. The result of the trade off for the IEEE802.11 is to comply with the minimum requirement of 10 dB.

VIII. HEADER AND SYNCHRONIZATION.

IEEE802.11 defines a synchronization pattern of 128 bits, followed by a header field of 64 bits for all DS packets. The 128 synchronization bits are all logic 1's and they are required, by the receiver, for initial acquisition of a packet. The synchronization field is followed with 64 bits of Physical Layer (PHY) header information. The header fields contain information such as address ID, data rate, packet size and a CRC error detection field. The synchronization and header fields are always transmitted at a rate of 1 Mbps independent of the rate of the actual data packet that follows.

IX. DS PHY SCRAMBLER AND DESCRAMBLER.

IEEE802.11 draft 5.1, requires data scrambling of all DS transmissions. Scrambling helps to avoid any CW transmission that can cause the waveform to be nonconformant to regulations. The entire packet including synchronization and PHY header bits are always scrambled. The polynomial $G(z) = z^{-7} + z^{-4} + 1$ is used to scramble. The implementation is a feedthrough configuration that is self synchronizing requiring no prior knowledge of the transmit initialization.

X. SPREADING SEQUENCE.

The spread properties of the DS waveform are attributed to the use of a pseudonoise (PN) random code that is used to modulate each of the transmitted bits. The code selected by IEEE802.11 belongs to a

class of codes known as Barker codes. The Barker codes have desirable autocorrelation properties that can contribute to the design of effective receivers. The following 11 chip Barker sequence is used as the PN code sequence:

+1, -1,+1,+1, -1,+1, +1, +1, -1, -1, -1

The left most chip is being output first in time. The symbol duration is exactly 11 chips long.

XI. MODULATION AND RATES.

Two modulation formats and data rates are specified for the DS PHY.A Basic Access Rate and an Enhanced Access Rate. The Basic Access Rate is based on 1 Mbps DBPSK modulation. The Enhanced Access Rate is based on 2 Mbps DQPSK.

XII. SPURIOUS EMISSIONS.

The DS PHY conforms with in-band and out-of-band spurious emissions as set by regulatory bodies. For the USA, refer to FCC 15.247, 15.205, and 15.209. For Europe, refer to ETS 300-328.

XIII. RF TURNAROUND TIMES

The transmit (TX) to receive (RX) turnaround time is less than 10 μs including the power down ramp. The TX to RX turnaround time is measured at the air interface from the trailing edge of the last transmitted bit to the valid detection of an incoming signal. The to TX turnaround time is less than or equal to 5 μs. This includes the transmit power up ramp described. This is primarily the delay from the network processor to the radio. The transmit power on ramp for 10% to 90% of maximum power is no greater than 2 μs. The transmit power down ramp for 90% to 10% maximum power is no greater than 2 μs.

XIV. POWER LEVEL CONTROL.

Power control is required for transmitted power greater than 100 mW. A maximum of 4 power levels may be provided. At a minimum, a radio capable of transmission greater than 100 mW shall be capable of switching power back to 100 mW or less.

XV. TX POWER SPECTRAL MASK.

The transmit spectral mask is designed to meet the requirements of the various regulatory bodies. The transmitted spectral products shall be less than -30 dBr (dB relative to the SINx/x peak) for f_c -22 MHz $< f < f_c$ -11 MHz and f_c +11 MHz $< f < f_c$ + 22 MHz and -50 dBr for $f < f_c$ -22 MHz and $f > f_c$ + 22 MHz where f_c is the channel center frequency. The measurements are made using 100 KHz resolution bandwidth and a 30 KHz video bandwidth.

XVI. RF CARRIER SUPPRESSION.

To comply with regulations, the RF carrier suppression measured at the channel center frequency must be at least 15 dB below the peak SIN(x)/x power spectrum. The RF carrier suppression is measured while transmitting a repetitive 01 data sequence with the scrambler disabled and by using DQPSK modulation. A 100 kHz resolution bandwidth must be used to perform this measurement.

XVII. RECEIVER SENSITIVITY.

For an input level of -80 dBm measured at the antenna connector, the Frame Error Rate (FER) must be less than $8x10^{-2}$ for a packet length of 1024 bytes. FER is specified for 2 Mbps DQPSK modulation. For an input level of -4 dBm measured at the antenna connector, the Frame Error Rate (FER) must be less than $8x10^{-2}$ for a packet length of 1024 bytes. Again, FER is specified for 2 Mbps DQPSK modulation.

XVIII. ADJACENT CHANNEL REJECTION.

The adjacent channel rejection must be equal to or better than 35 dB with an FER of $8x10^{-2}$ using 2 Mbps DQPSK modulation for a packet length of 1024 bytes.

XIX. CLEAR CHANNEL ASSESSMENT.

The DS PHY provides the capability to perform Clear Channel Assessment (CCA) according to at least one of the following three methods:

- Energy above threshold.

  CCA shall report a busy medium upon detecting any energy above a predefined the ED threshold.

- Carrier sense only.

  CCA shall report a busy medium only upon the detection of a DS signal. This implies detection of a valid spread sequence. This signal may be above or below the ED threshold.

- Carrier sense with energy above threshold.

CCA shall report a busy medium upon the detection of a DS signal with energy above the predefined ED threshold.

XX. REFERENCES

[1] J. Fakatselis, and A. Petrick, "System Considerations in Spread Spectrum Designs", Wireless Design and Development, July 6, 1995.

[2] IEEE P802.11, Draft Standard for Wireless LAN "Medium Access Control (MAC) and Physical Layer (PHY) Specification" unapproved draft P802.11 D5.1, November 22, 1996.

A NEW AUTOMATED COLLECTING SYSTEM OF DATA FOR SURVEYS

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Abstract - **This paper shows a new wireless system developed in order to automate surveys. The system is primarily intended for population surveys but it can be used with another system for surveys. The main features of the system are its inherent simplicity, and low cost. The paper is focused specially on the low cost wireless devices developed to work in this new system.**

I. INTRODUCTION

Surveys that use a great amount of data are expensive and slow. Some surveys, specially surveys of population designed to predict new public transport services into towns or to measure movements of population in some areas, are specially suited to be automated using wireless systems.

These surveys are very expensive and slow too. Avoiding the problem of the post processing of the collected data, in a general way most surveys need a lot of samples to improve its accuracy. This data must be taken by trained agents. Apart from this, some problems appear derived from false answers, etc.

An automatic system to collect this data is very helpful to improve the efficiency of these surveys and to reduce cost.

The system proposed in this paper uses very small, reliable, and cheap transmitters that must be carried by the population to be analyzed. Apart from the transmitters a set of receivers located in strategic points are also necessary.

A unit of the transmitter must be give to any of the persons that are going to be "used" as sample for the survey. To incentive hisor her collaboration and to recover the transmitter (alive) at the end of the work a small reward must be give to the collaborators. For example a Council must give free bonus for public transport and so on. Obviously the cost of the transmitter must be as low as possible because the risk associated to it. The receiver must very reliable and capable to work in "hostile" environments.

In the next paragraphs we will discuss about the more interesting electronic aspects for the designer.

II. Oscillator of the transmitter unit

One of the most important parts of the whole system is the transmitter. Its main requirements are the following:
-Small size
-Low power consumption
-Low cost
-Reliable operation

One effective way to satisfy the previous points is to use the smallest amount of parts as possible. This lead to very simple topologies. Nevertheless, simple topologies usually exhibit poor electric performance. To avoid it the designer can work over:
-The specifications of the whole system, making them less strict.
-Optimizing the electronic design, searching for easy solutions to improve the final performance.

To solve this problem we have design and tested two topologies:
-Transmitters based on a low power crystal oscillator.
-Transmitter based on an S.A.W. oscillator.

a) Transmitter based on a low power crystal oscillator. The advantages and the design methods of the low power crystal oscillators have been described by several authors [1,2,3]. The main advantage of this kind of oscillators is low size, low power consumption and very high stability. This stability depends on the Q of the quartz crystal, so the cost of the oscillator depends on the stability desired [4,5].

Table I. Comparison of pushing and pulling figures

	Crystal Oscillator	S.A.W. Oscillator
Pushing	± 1 ppm / V.	±17 ppm /V.
Pulling (12 db R.L.)	± 0.5 ppm	7.8 ppm

The maximum frequency that can be reach with a crystal oscillator is lower than the frequency of the band used by the whole system.

The scheme of the figure 1 shows a transmitter based on a quartz crystal. The output frequency is an overtone of the fundamental frequency of the crystal. Several topologies have been studied [2] to perform this function and the selected are showed in the figure 1.

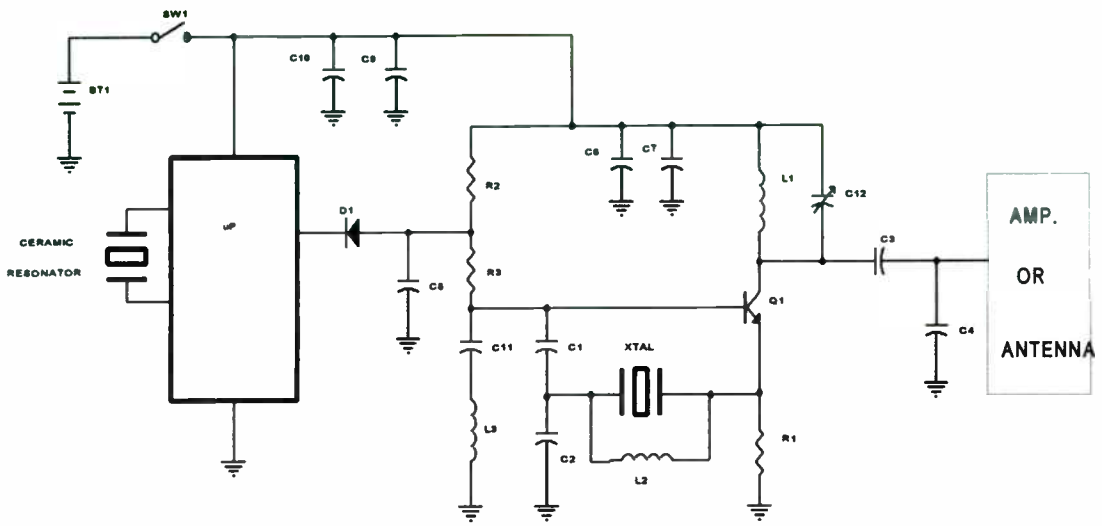

Fig 1. Transmitter based on crystal oscillator

b) Transmitter based on S.A.W. oscillator. The main advantage of this topology is its inherent simplicity. It doesn't need special adjustment if is properly designed. The amount of parts used by this topology is minimum, so the reliability is also high.

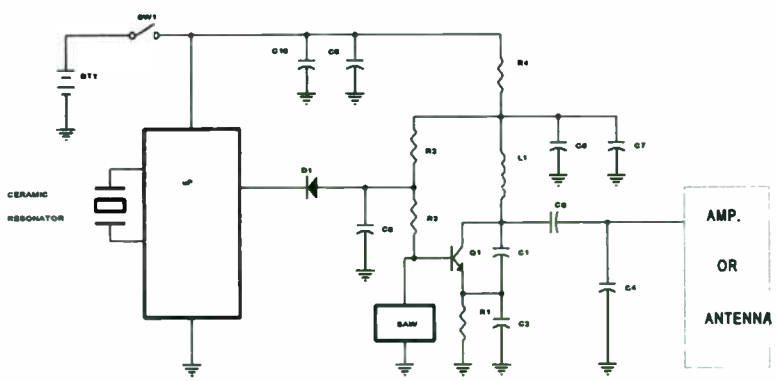

Fig 2. Transmitter based on S.A.W. oscillator

The main disadvantage of this topology is the low stability of its output frequency. This cannot be accepted by all the systems. So its validity depends on the specifications of the system. Furthermore this topology doesn't need a frequency multiplier. Therefore, if the bandwidth assigned to the system is not narrow it would be the preferred.

Another disadvantage is the cost of the parts, specially the S.A.W. device that usually is higher tan the cost

of an equivalent quartz crystal to get similar performance.

III. POWER AMPLIFIER OF THE TRANSMITTER

The output power of the transmitter is low (10 dBm aprox). Nevertheless, it is a good practice to locate one or more amplifier stages after the oscillator to improve the stability, specially, when a S.A.W. oscillator is employed. These stages not only increase the output level but also are useful to get isolament of the amplifier from the load variations.

The most power consumed by the transmitter is done by this stage. So it is very important to get the highest efficiency possible. High efficiency operation modes are not very easy to perform in such a limited environment

Due to the low levels at the output of the oscillator and the limits imposed by simplicity of the transmitter, high efficiency modes are not suitable for this amplifier. Even mode "C" or "CD" modes of amplification are not a good choice.

Because the "output impedance" of the power transistor is high, using a C-L-C (Pi network) for matching it is possible to approximate an "E" amplification mode (it is not a true E mode), nevertheless the limits imposed by the low excitation level that precludes this mode.

The power amplifier is biased similar like a class "AB amplifier." The matching network and bias have been optimized to maximize the efficiency of the amplifier using simulation and tests.

Bipolar technology has been selected because its low cost and good performance for the working voltage.

The efficiency obtained is 50% aprox. for a 50-Ohm load. This is a good value for the efficiency because the working voltage is only 3 volt. To improve the efficiency with low voltages we also have work over the dynamic load line of the amplifier. The impedances showed to the harmonics are purely reactive.

Nevertheless we have considered that it is not very useful to get improvements on the efficiency working to exhibit exotic values of the load impedance at the harmonics because this impedance is varying continuously. The results in efficiency working in such a way over the load at the harmonic frequencies would be worse than the obtained value if the load impedance changes.

Here we also considered it is better to get a stable point of work sacrificing electrical features.

IV ANTENNA OF THE TRANSMITTER

The transmitter is enclosed into a small plastic box. A small multiturn antenna is used. The main benefit of this antenna is its small size. The main problem is its bad efficiency (-6 dB). Several designs have been tested. The P.C.B loop antenna used in [1] has not been selected due to its size. We have used a multiturn antenna made of silver coated wire. With this antenna, at the frequency of operation it is possible to get good performance in spite of the electric and radiation losses.

The core of the antenna is the air. Therefore, the input impedance of the antenna is low. To minimize the matching losses the components of the matching network have been selected of high Q.

Fig 3. Photograph of the transmitter

V. TOPOLOGY OF THE RECEIVER

The "boundary specifications" of the receiver are not as strong as the transmitter. A small amount of receivers is needed compared to the amount of transmitters. By other hand thee receivers are located in fixed places and there are not restrictions in size.

The most important features of this receiver are similar to the features of any receiver for mobile communications located into a city:

-Good Sensitivity
-High Dynamic range
-Good cochannel interfererence rejection . . .
-High reliability.
-Low power consumption

Several architectures were studied during the first designing stages. A Direct Conversion receiver was proposed due to its important advantages and the experience of the group of researchers on the matter. This receiver must use a powerful A.G.C. system [6] to work in some electromagnetic "pollutioned" environments.

Nevertheless, the size is not a problem in this design, neither the power consumption (with some limits). A proper designed superheterodyne receiver usually offers better electrical behavior than a Direct Conversion system. This is the reason because the superheterodyne topology was selected (The D.C. system has not been rejected yet).

The power consumption is not the most important problem of a receiver supplied by an A.C. line. Nevertheless, this receiver will be located in very offensive environments. Not only electromagnetic interferences but also thermal limits must be taken into account.

So it is very important to perform a low power consumption to minimize the derated power and the temperature into the enclosures of the receiver set.

The dynamic range with A.G.C. and without it, of the proper designed superheterodyne topology is better. The previous are more true if there is not limit for power

consumption.

In the next paragraphs the most important different stages of the receiver will be discussed:

a) Low noise amplifier: The first amplifier determines more than any stage the noise figure of the receiver. A Bipolar Low Noise transistor has been selected for this stage. The Ic bias current is 20 mA and the Vce is 6 volts. This ensures a high IP3 (30dBm) and a noise figure of only (2.5) dB. It is more than enough for an urban location.

The location of the receiver is important to select a receiver with maximum dynamic range instead of minimum noise figure.

The receiver will be located in a place where the impedance of the antenna is not varying continuously. This let us to select a transistor with minimum noise figure being sure that this noise figure will be reached [1].

b) Mixer: A passive, "high injection level," diode ring mixer was selected. This mixer ensures high dynamic range and reliability. Nevertheless a previous system analysis and simulation were performed to determine exactly the specifications of the mixer in order to keep "specifications balance" along the receiving chain.

C) Intermediate frequency: The intermediate frequency is divided into to stages at 21.4 MHz and 455 KHz respectively. To keep the high dynamic range desired in the receiver MOS transistor was used in the amplifiers of this stage.

The filters are both ceramic an crystal based. In this way the selectivity is better than 60 dB for the adjacent channel. The rest of the amplifier chain is inside a commercial Integrated Circuit that includes: I.F. stages, active mixer, F.M. detector, L.F. filter and a data slicer.

After this stage a buffer stage with a very simple data filter is located to help the digital decoding operation. The decoding operation is performed by a software running into a special microprocessor. This µP is only entrusted to do this function.

VI. TECHNOLOGY

Low cost is one of the most important goals in the design of the transmitters. A lot of transmitters will be constructed and probably, many of them will be damaged or lost.

So the technology used with the transmitter must be as cheap as possible but satisfying the previous requirements.

The P.C.B uses dual coated G10 material (0.7mm thick). This ensures good performance and minimum cost. The number or parts have been reduced as possible and they are intended for surface mounting (0805 size).

A low cost PVC enclosure has been used to protect the circuit. This is a "transparent" material for the R.F. Therefore the antenna can radiate without problems. The R.F. shielding has been reduced to one cooper side of the PCB. The whole receiver has got a small chain to be used as a turnkey.

The receiver is more sophisticated than the transmitter. G10 also has been used for the PCB of the receiver. Surface mounted components are employed. The main difference is in the enclosures hardware. Like the subsystems are essentially "cool" all of they are enclosed in tin enclosures. This is enough for shielding and not very expensive. The receiver is mounted on a waterproof anodized aluminum box. This box is,covered of plastic, is capable of working in adverse climatological conditions.

It only has two waterproof hidden connectors: one is for the antenna and the other one is a multipin connector for the supply and data communications.

This set (receiver) has been tested to work between -20° C and +60 ° C and it has not exhibited problems.

Fig 4. Photograph of the receiver

VII. CONCLUSIONS

The most important electrical features of the transmitter (S.A.W. version) and the receiver are shown in the next tables,table I and table II respectively.

Table II. Main features of the transmitter.

- Vcc = 3 V.
- P_{out} = 10 dBm.
- Stability = +- 180 ppm from -20° to 60°
- Size =1000 mm^2.
- range> 2 months.
- Spurs and Harmonics < -60 dBc.
- Rate: 256 bits/s

Table III. Electrical features of the receiver.

- Vcc = 9 V.
- Sensitivity < -123 dBm.
- Stability = +- 28 ppm to -20° to 60°
- Size = 12500 mm^2.
- Adjacent channel rejection < -70 dBc.
- frequency: 330 Mhz.
- Rate: 256 bits/sec.
- Intermediate frequency: 21.4 Mhz / 455 KHz.

The use of a small amount of components and

widely used technologies reduce the cost of the transmitter to be reliable and competitive with traditional systems.

Low power superheterodyne technologies allow high reliability in hostile electromagnetic and climatological locations.

The receiver and a transmitter intended to perform automatic data collection for surveys showed. Apart from the electric shave fulfilled the cost specifications of the project.

Automatic data collection based on wireless systems have not been widely used (even evaluated and studied) yet. This new wireless application will be probably massively developed in the future because its inherent advantages over the traditional systems. The use of wireless technology joined to the use of data networks have important potential of growing in the future. The validity of the idea and its industrial potential has been extensively proved in this work.

REFERENCES

[1] F.J. Ortega Gonzalez, J.L. Jimenez Martin, "Optimum direct conversion receivers", Proceeding of the 4th Wireless Symposium, Sta Clara, CA. Pp 55-60

[2] R. Matthys, "Cristal Oscillator Circuits". Wiley Interscience, 1983.

[3] Donald Belcher. "Designing a High stability VHF Oscillator". RF Design, January/February 1983.

[4] Randall W. Rhea "Oscillator Design and Computer simulation". Noble Publishing, 1995.

[5] R. Matthys "A High Performance VHF Crystal Oscillator Circuit". RF Design. March 1987

[6] F.J. Ortega González, J.L. Jimenez Martin, "A Direct Conversion receiver using a novel ultra low power A.G.C." Proceedings of the 1997 VTC (to be published)

A Constant Envelope Modulation Technique for WLAN DS-SS Applications

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Abstract: A newly developed constant envelope modulation technique is proposed for wireless LAN direct sequence spread spectrum (WLAN DS-SS) applications to improve system power efficiency. By introducing I/Q cross-correlation to an offset QPSK system and employing modified baseband filtering techniques, the proposed modulation architecture provides a constant envelope modulated signal and improves power efficiency by 4 - 7 dB as compared to the current WLAN DS-SS standard QPSK. Bit error rate (BER) and error floor characteristic of this system are evaluated in non-linear amplified (NLA) Rayleigh fading channels corrupted by co-channel interference (CCI) and delay spreading. System capacity and throughput are analyzed based on the evaluation results. Hardware implementation and measured results are also briefly discussed. It is demonstrated that by selecting different system parameters, this system can be optimized for a wide range of PCS and mobile communication applications.

1. Introduction

Due to the wireless nature of the network and the limited power of the mobile unites, both power efficiency and spectrum efficiency are very desirable for wireless LAN applications. Unfortunately, power efficiency and spectrum efficiency are mutually incompatible in most extant systems. For example, constant envelope modulation schemes usually have higher power efficiency because they are capable of using class-C power amplifiers without introducing spectrum regeneration. However, most constant envelope systems don't have the desired spectrum efficiency [4]. For the IEEE 802.11 wireless LAN DS-SS applications, since no appropriate constant envelope modulation system can meet the FCC output spectrum mask which guarantees the efficiency of spectrum utilization, a non-constant envelope linear modulation method, QPSK, had to be used, therefore the system suffers a low power efficiency.

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In this paper, a novel constant envelope modulation technique is proposed and investigated for the WLAN DS-SS applications. This technique introduces a modified double jump filter (DJ) to an I/Q cross-correlated offset QPSK structure, by controlling the DJ filter parameters and the I/Q cross-correlation factor, it provides a constant envelope modulated signal as well as meets the FCC spectrum mask. As compared to the conventional QPSK, the power efficiency can be improved by 4 - 7 dB. BER performance of this system is evaluated in a CCI limited Rayleigh fading channel, and a time delay spreading channel. System capacity and throughput are also analyzed. It is demonstrated that with different system parameters, this new modulation architecture can be optimized for a wide range of PCS and mobile communications applications.

This paper is organized as follows. After the introduction, the proposed system architecture including both modulator and demodulator is described in detail in section 2. System performance such as spectral efficiency, power efficiency, BER, and system capacity/throughput are presented in section 3. Hardware implementation and measured results are discussed in Section 4. And Section 5 is a summary of this paper.

2. The Proposed System Architecture

The block diagram of the proposed system is presented in Figure 1. This modulation architecture is developed based on an I/Q cross-correlated offset QPSK (XPSK)[1] structure which was invented and patented by Kato and Feher[2]. The I/Q baseband signals are first applied to the inter-symbol interference and jitter free (IJF)[3] low pass filters which have the impulse response expressed as:

$$h(t) = \begin{cases} \frac{1}{2}\left[1 + \cos\left(\pi t / T_S\right)\right] & |t| \le T_S \\ o & otherwise \end{cases}$$

Then a controlled amount of cross-correlation between the I and Q channel signals is introduced. The basic

schedule to introduce the cross correlation can be described as follows: (i) when the I channel signal is zero, the shifted Q channel signal is the maximum amplitude of 1 (normalized), (ii) when the I channel signal is non-zero, the maximum magnitude of the shifted Q channel signal is reduced from 1 to A, (iii) when the Q channel signal is zero, the I channel signal is 1, (iv) when the Q channel signal is non-zero, the I channel signal is reduced from 1 to A. Figure 2 presents an example of the base band signals, where the solid line represents the output of the I/Q cross-correlator, and the dot line is the input I/Q signal. The four different signal transition functions are defined as:

$$f_1 = 1 - k\cos^2\left(\pi/T_s\right) \quad f_2 = 1 - k\sin^2\left(\pi/T_s\right)$$
$$f_3 = -1 + k\cos^2\left(\pi/T_s\right) \quad f_4 = -1 + k\sin^2\left(\pi/T_s\right)$$

where $k = 1 - A$. Table 1 illustrates the eight possible transition patterns, and Figure 3 presents the signal space diagrams at the output of the cross-correlator with $A = 0.707$, and 0.5 as compared to the input signal space diagram ($A = 1$). It can be observed from Figure 3 that by controlling the amount of cross correlation, the envelope fluctuation can be reduced from 3 dB to approximately 0 dB (quasi constant envelope), thus improving its performance in NLA systems [1]. Unfortunately, the spectrum efficiency was not be improved by this technique[1], it has practically the same spectrum efficiency as conventional FQPSK and GMSK[4].

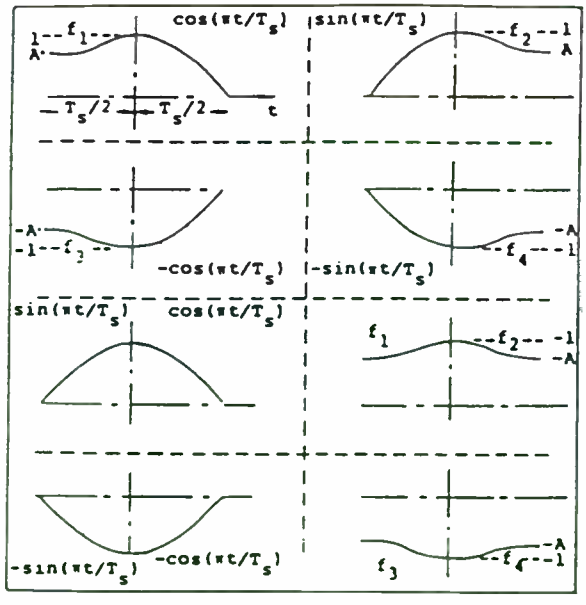


Table 1. Eight possible transition functions

In order to achieve higher spectral efficiency while keeping the constant envelope nature, a modified double jump filter was introduced to the I/Q cross-correlated off-set QPSK structure, which forms a new category of constant envelope modem/radio techniques, double jump filtered QPSK (DJ-FQPSK). Based on the study and computer aided optimization, a square root DJ filter with a very small jump rate factor has been found to be the optimal filter for this application. The frequency response of the square root DJ filter can be expressed as

$$H(f) = \begin{cases} 1 & 0 \le f \le ((1-\alpha)f_n) \\ \sqrt{(1-\gamma) - \dfrac{(1-2\gamma)(f+\alpha f_n - f_n)}{2\alpha f_n}} & (1-\alpha)f_n \le f \le (1+\alpha)f_n \\ 0 & (1+\alpha)f \le f \end{cases}$$

where f_n is the Nyquist frequency, α is roll-off factor, and γ is the jump rate factor. By optimizing the DJ filter parameters, α, γ, and I/Q cross correlation factor A, the DJ-FQPSK can improve spectrum efficiency and system capacity significantly for different PCS and cellular mobile communications [4].

After passing through the DJ filters, I, Q channel baseband signals go to the quadrature modulator. The output of the hard limiter is the DJ-FQPSK modulated signal. As a constant envelope modulated signal, this system is capable of operating with class C power amplifiers without any output back-off (OBO). This is in contrast with the conventional non-constant envelope QPSK modulation which typically requires 1 - 3 dB OBO to avoid spectral spreading caused by non-linear amplification [7], plus 3 - 4 dB margin against gain fluctuation of the power amplifier due to environmental variations. Thus the proposed DJ filtered FQPSK is 4 - 7 dB more power efficient than the QPSK structure used in the wireless LAN DS-SS standards.

DJ-FQPSK signal can be demodulated by a conventional OQPSK demodulator. Therefore this technique could be easily adopted by the QPSK modulated systems such as WLAN DS-SS. This is another advantage of this scheme over other similar constant envelope modulation methods such as TFM, which requires a more complex signal processing approach[1]. Based on our investigation, Buttworth BPF or LPF with $BT_b = 0.55$ provides the best BER performance for the demodulator as shown in Figure 4.

3. Performance Evaluation

A. Spectral Efficiency

Spectral efficiency η_f (b/s/Hz) of a digital modulation scheme is defined as $\eta_f = 1/(WT_b)$, where W is channel spacing and T_b is the one bit duration. In a multi-channel system, normalized channel spacing, WT_b, is usually determined by the maximum acceptable adjacent channel interference (ACI) level. For different applications, there are different definitions for the normalized bandwidth WT_b. For example, in wireless LAN systems, -20 dB and -30 dB power spectrum density (PSD) points are defined as the channel spacing[10]. In the US EIA IS-54 and European DECT standards, the integrated signal power in a specific bandwidth is used to determine the channel spacing[5,6]. And in the public Land Mobile Radio (PLMR) systems, -40 dB PSD point is the critical point to decide the channel spacing.

For the IEEE 802.11 wireless LAN direct sequence spread spectrum (DS-SS) applications, the FCC rules can be interpreted as shown in Figure 5 [10]. It is required that the system has to achieve at least 1 b/s/Hz and 0.5b/s/Hz at -30 dB and -50 dB PSD points, respectively. Since extant constant envelope modulation schemes including GMSK, and the conventional I/Q cross-correlated QPSK can not meet these requirements as we can see in Figure 6 and Table 2, linear DQPSK has been adopted as one of the standards [10], which makes the system suffer about 4 - 7 dB power efficiency loss as compared to a constant envelope system. With the proposed constant envelope DJ-FQPSK system, however, by selecting $A = 0.5$, $\gamma = 0.01$, and $\alpha = 0.5$ these requirements can be met comfortably as shown in Figure 6 and Table 2.

	Spectrum Efficiency(b/s/Hz)				C/I	Capacity
	PSD			ACI	Rayleigh @ 10^{-2}	η_T (b/s/Hz/m²) @ -26dB ACI
	-30dB	-40dB	-50dB	-26dB		
GMSK BT = 0.5	0.58 (100%)	0.46 (100%)	0.40 (100%)	0.86 (100%)	14dB	0.12 (100%)
XPSK A = 0.707	0.87 (150%)	0.67 (146%)	0.41 (102%)	1.18 (137%)	14dB	0.17 (142%)
DJ-FQPSK A = 0.5, α = 0.5	1.17 (200%)		0.55 (137%)	1.42 (165%)	14dB	0.21 (172%)
DJ-FQPSK A = 0.5, α = 1		0.92 (200%)				

Table 2. Summary of DJ-FQPSK performance

As compared to other constant envelope modulation techniques, the proposed DJ-FQPSK system has significant spectrum efficiency advantage. By selecting different system parameters, It can be optimized for different applications such as IEEE 802.11 wireless LAN frequency hopping (FH) spread spectrum systems, public land mobile radio (PLMR) systems, and the DECT related applications. Table 2 presents a summary of the spectrum efficiency of DJ-FQPSK as compared with other techniques, which shows 20 - 100% spectrum efficiency improvements can be achieved depending on different specifications.

B. BER Performance

For most digital modulation schemes, BER performance will be degraded while reducing the signal bandwidth or increasing the spectrum efficiency. However, this proposed DJ-FQPSK doesn't suffer BER degradation for higher spectrum efficiency. In his section the BER performance of DJ-FQPSK is evaluated in a NLA CCI limited Rayleigh fading channel. Error floor characteristics is evaluated in a delay spreading Rayleigh fading channel. System parameters, A, α, and γ, are selected as the same as that to obtain the best spectral efficiency for different applications. Coherent detection is assumed for demodulation. Receiver BPF is a 4th order Buttworth filter with $BT_b=0.55$. Figure 4 presents a block diagram of the demodulator.

Figure 7 presents the BER performance of DJ-FQPSK with different system parameters in a CCI limited environment as compared to coherent QPSK and GMSK. It is shown that with $A = 0.5$, $\alpha = 0.5$, and $\gamma = 0.01$ as specified for the WLAN DS-SS applications, DJ-FQPSK has about the same BER performance with QPSK and GMSK.

The error floor characteristics of DJ-FQPSK in a time delay spread Rayleigh fading environment is also evaluated. Two-way equal gain channel model is used in the evaluation. Results as shown in Figure 8 indicate that DJ-FQPSK has about the same performance as linear QPSK in a delay spread Rayleigh fading environment.

C. System Power Efficiency and Throughput

Power efficiency of a system is determined by two major factors, the output power amplifier efficiency and BER performance. In order to use the most efficient class-C power amplifier without spectrum

regeneration, a constant envelope modulated signal is required. For linear modulation schemes such as QPSK, about 1 - 3 dB output back-off (OBO) is necessary to avoid spectral spreading caused by non-linear amplification[3], and 3 - 4 dB margin is required against gain fluctuation of the power amplifier due to environmental variations. Therefore the proposed constant envelope DJ-FQPSK system is 4 - 7 dB more power efficient than the conventional QPSK as employed by the WLAN DS-SS systems.

More importantly, this 4-7dB power efficiency improvement does not sacrifice the BER performance as shown in the previous section. In wireless LAN applications, system capacity or throughput is determined by spectral efficiency, and BER performance. This better BER performance not only represents higher power efficiency (longer battery life time), since less power needs to be transmitted to achieve the same quality of link connection, but also leads to a shorter data file transfer time/message delay and increased system throughput which are the most important issues in wireless LAN applications.

In a cellular/micro-cellular PCS system, capacity is determined by spectral efficiency, BER (power efficiency), and frequency reuse ability. This means that applications of our power and spectrally efficient DJ-FQPSK in PCS and other cellular mobile systems could lead to a higher system capacity. The capacity of DJ-FQPSK based on IS-54 definition is presented in Table 2.

4. Hardware Experiments

The proposed DJ-FQPSK architecture can be implemented with many methods[9]. One of them is the Xilinx Field Programmable Gate Array (FPGA) implementation [9]. A look-up table was developed to implement the I/Q cross-correlator for reduced memory. The proposed DJ filter can be approximated with a 7th order Kaiser window FIR. Detailed design and implementation of this scheme can be found in [9]. Figure 9 presents the measured space diagram and output PSD of the Xilinx FPGA implemented DJ-FQPSK with $A = 0.5$, $\alpha = 0.5$, and $\gamma = 0.01$.

5. Summary

A spectrally efficient constant envelope DJ-FQPSK modulation system is proposed and investigated for the WLAN DS-SS applications. Performance of this system including spectral efficiency, power efficiency, BER, and system capacity/throughput is evaluated in a NLA AWGN/Rayleigh fading environment. Results show that the proposed DJ-FQPSK meets the spectrum efficiency requirements and improves system power efficiency by 4~7dB as compared to the standard QPSK system. With no BER degradation, this system therefore also improves the system capacity and throughput significantly. It is also demonstrated that the proposed DJ-FQPSK system can be optimized for a wide range of wireless applications to improve spectrum efficiency and system capacity.

References

[1] S. Kato, K. Feher, "XPSK: A New Cross-Correlated Phase-Shift-Keying Modulation Technique," *IEEE Trans. on Commun.*, May 1983.

[2] S. Kato and K. Feher: "Correlated signal processor," US patent No.4,567,602, issued January 28, 1986. Canada No. 1211517, issued Sept. 16, 1986.

[3] K. Feher, "Filters," U.S. Patent No. 4339724, issued July 13, 1982; Canada No. 1130871, August 31, 1982.

[4] Y. Guo and K. Feher, "A New FQPSK Modem/Radio Architecture for PCS and Mobile communications," *IEEE Journal on Selected Areas in Communications*, Feb. 1995, pp.345 - 353.

[5] Engineering Dept., EIA, Cellular System: Dual-Mode Subscriber Equipment— Network Equipment Compatibility Specification, Dec. 1989.

[6] DECT Specifications, Physical Layer, CI SPEC Part 1, Rev.06.0.

[7] K. Hirade, "Mobile Radio Communications", Chapter10 in *Advanced Digital Commun.: Systems and Signal Processing Techniques*, by K. Feher, Englewood Cliffs: Prentice-Hall Inc., 1987.

[8] W. C. Y. Lee, "*Mobile Cellular Telecommun Systems*," McGraw Hill, 1989.

[9] R. Atienza, "*Simulation and Implementation of Baseband Modulation Techniques*," MS Thesis, University of California, Davis, 1994.

[10] Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications, Draft Standard IEEE 802.11.

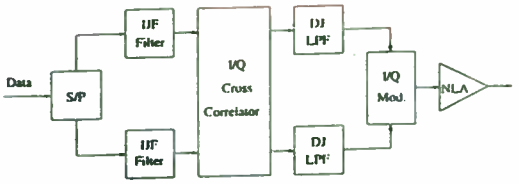


Figure 1. Block diagram of DJ-FQPSK system

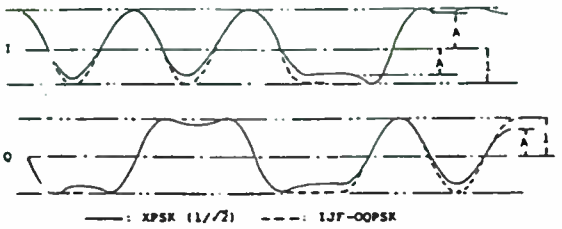


Figure 2. Baseband I/Q signal waveforms of the cross-correlated XPSK

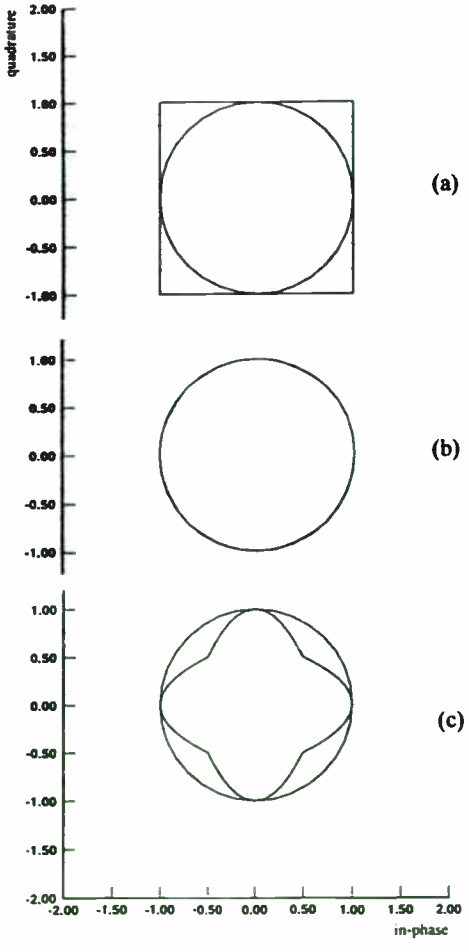


Figure 3. Space diagrams (a) A=1, (b) A=.707, (c) A=0.5.

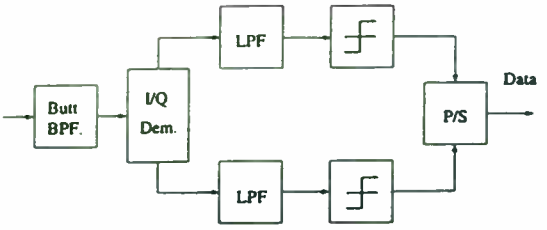


Figure 4. Block diagram of the DJ-FQPSK demodulator

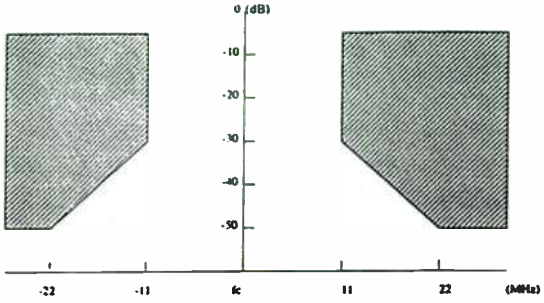


Figure 5. FCC spectrum mask for the WLAN DS-SS (chip rate = 11Mchip/s)

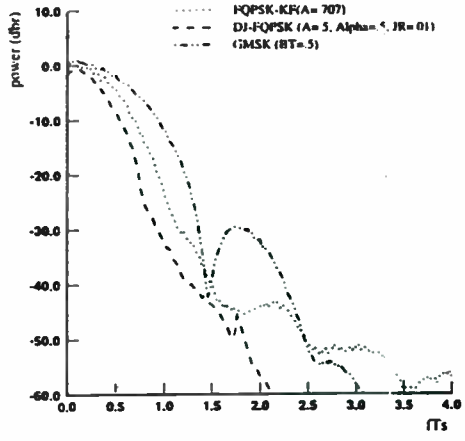


Figure 6. PSD of DJ-FQPSK, GMSK, and FQPSK

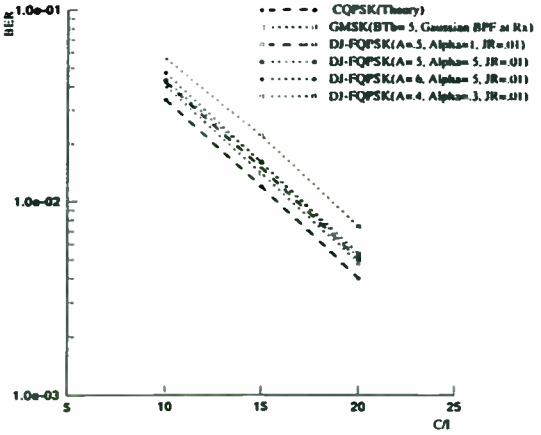


Figure 7. BER of DJ-FQPSK in Rayleigh/CCI

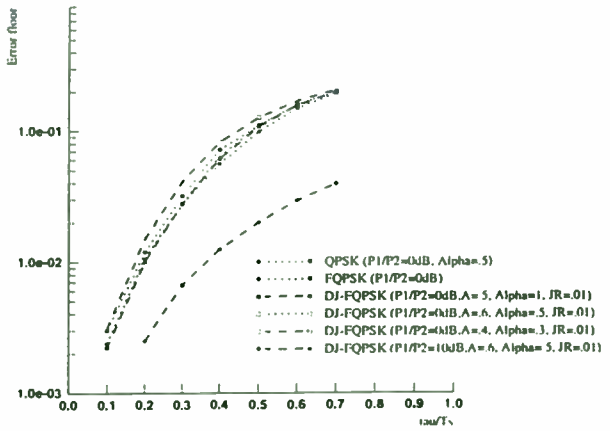
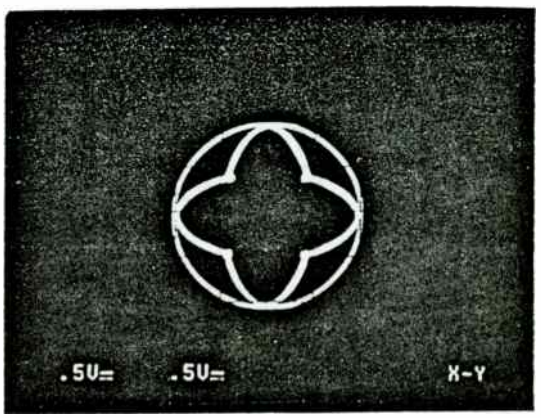
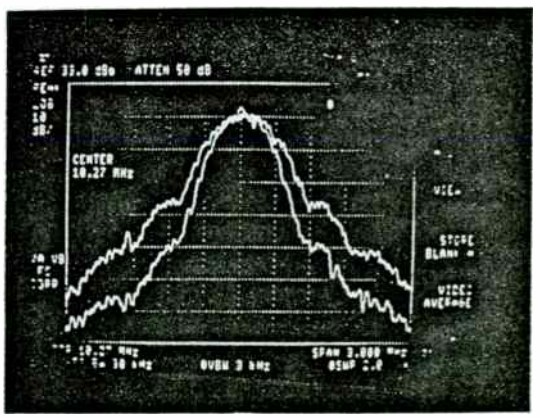


Figure 8. Error floor of DJ-FQPSK in Rayleigh/delay spreading channel



(a)



(b)

Figure 9. Measured results of DJ-FQPSK (a) Space diagram (A=.5, α = .5), (b) PSD (upper FQPSK A=.707, lower: DJ-FQPSK A=.5, α = .5)

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He is an Assistant Professor of Electrical Engineering at the University of Missouri-Columbia/Kansas City. Before joined the University, he had been with Philips Semiconductors, Wireless Communications Product Group, Sunnyvale, CA for three years. His research interests include power and spectrum efficient modem/radio architecture, spread spectrum techniques, and channel equalization for wireless communications.

Wireless LANs

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Designing a High Speed Direct Sequence Spread Spectrum Radio

This session shares some of Lucent Technologies wide experience (10+ years) in developing high speed Direct Sequence Spread Spectrum radios. It will elaborate on the differences between Direct Sequence (DS) and Frequency Hopping (FH) modulation techniques. How to achieve a high quality radio design while meeting the customer requirements in cost, coverage, performance, capacity, power & regulations will be discussed. The session will cover future technology and development directions with respect to wireless LANs & chip development for the different layers (MAC, PHY, and Radio), with emphasis on the IEEE 802.11 standard currently under development.

I. INTRODUCTION

From day one, designing data communication products has always been a fight for higher data rates and throughput, in cabled systems as well as in wireless systems.
The Narrow band radios used in various applications by nature have their limitations with respect to throughput. The small bandwidth available for Narrow band radios do not allow for high throughput. Regulations however do allow for higher output power on Narrow band radios which results in relative large coverage area. Therefore the Narrow band applications only cover a niche market where low throughput and high range are acceptable parameters and where standard system compatibility is no issue. Therefore this option will not be discussed in any more detail in this document. The considerations in this paper on designing a radio will be totally focused on Spread Spectrum radios, which because of higher available bandwidth allows for higher data throughput. Spread Spectrum Radios will also allow for unlicensed use of the Band.

The Direct Sequence Spread Spectrum (DSSS) Radios, transmit a signal over multiple frequencies simultaneously, which allows it to allocate the complete Waveband, and makes it highly resistant to interference. A receiver, by match filtering, will retrieve the original data.
The Frequency Hopping Spread Spectrum (FHSS) Radios, modulate a signal into a number of different packets, that are transmitted one by one, over multiple frequencies. Most frequency hoppers on the market today are so-called "slow frequency hoppers". Slow Frequency Hoppers transmit the data in relatively low number of large datapackets. When a hop fails the packets must be sent again over another hop.

The pro's and con's of the different systems will be highlighted in the section design trade off's. First the standards and regulations, and the requirements for wireless LANs will be discussed in more detail.

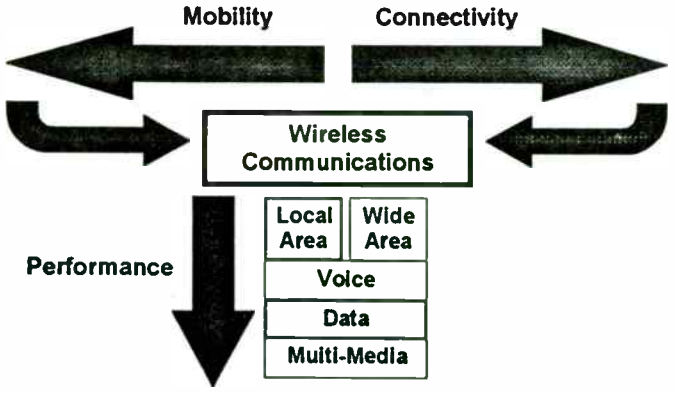
II. NEED FOR WIRELESS LAN COMMUNICATIONS

Workers in jobs ranging from retail organizations to shipping companies to medical environment to the office executive, set the requirement for Mobility and Connectivity at the same time. The Solution here is Wireless communications.

Data Communication requirements for the mobile worker can be identified in both, Local Area and Wide Area Applications. Wireless Communication products for voice became widely accepted over the past few years.

Future systems will move towards a full integration of the different wireless applications into Multi-Media Systems.

Enterprises worldwide are finding that wireless data-communication schemes can be leveraged to Increase work force efficiency,



improve customer service, and simplify the installation and connection of nformation systems. Specifically, wireless LANs are easy to deploy and can serve in applications ranging from retail to manufacturing. No industry-wide standards exists however, and the different implementations of spread spectrum technology used by different vendors results in substantially different performance. Examine the spread spectrum implementation closely before choosing a wireless LAN technology.

Wireless LANs are a close cousin of the ubiquitous Ethernet LAN. The wireless alternative simply uses RF data transmission techniques in place of the wire used in Ethernet environments. In either case, the LAN allows users to seamlessly access disk drives, printers, and other peripherals on other connected systems. In fact, wired and wireless nodes are regularly combined on the same network with no logical distinction from a users' perspective.

The expanding wireless LAN market has overcome several obstacles to reach its current stage of growth. Wireless LANs offer the throughput necessary to serve in environments ranging from point-of-sale applications to office networks. Price hasn't reached the level of wired Ethernet LANs, but the cost has dropped to around $700 for wireless LAN interface cards. Many companies find the price very affordable relative to the cost of installation of wired LANs, and relative to the increased productivity and revenue realized through the use of wireless technology in compelling applications.

III. STANDARDS AND REGULATIONS

The lack of industry standards remains the most significant obstacle to ubiquitous deployment of wireless LANs. Today, products from different vendors won't necessarily interoperate the same way Ethernet cards from different vendors can be seamlessly connected. What standard will there be for the PHY and MAC Layers?

The IEEE is addressing the need for a standard via its 802.11 working group and draft standard for the 2.4 GHz ISM Band, which is available worldwide as unlicensed spectrum. Completion of the standard is six months away. A number of LAN vendor companies did put in significant efforts to create this standard. Lucent Technologies, one of the main proposers of the protocol, did contribute with their experience on WaveLAN products to make the proposal and develop the current specification. The modulation is the same as in the current WaveLAN product which was chosen for its efficient coding. The MAC Protocol is based on a Proposal developed in cooperation between Lucent Technologies, Symbol Technologies and Xircom. A wide market acceptance for this standard is expected, in fact the market already shows a strong pull for IEEE products.

The IEEE 802.11 standard actually defines two different types of RF-based wireless LANs -- Direct Sequence Spread Spectrum (DSSS) and Frequency Hopping Spread Spectrum (FHSS). Despite sharing the name spread spectrum, DSSS and FHSS technologies have little in common.

FHSS is by far the simpler of the two. As the name implies, the systems hop from narrow band to narrow band within a wide band. Specifically, FHSS radios send one or more data packets at one carrier frequency, hop to another frequency and send one or more data packets and continue this hop-transmit sequence. The time the FHSS radios dwell on each frequency depends on a combination of individual implementation, governmental regulations, and adherence to the IEEE 802.11 draft standard. The hopping pattern or sequence appears random but is actually a periodic sequence tracked by sender and receiver. FHSS systems can be susceptible to noise during any one hop but typically can achieve

error-free transmissions during other hops around the wide band.

DSSS increases modulation rate. DSSS systems spread transmissions across a relatively wide band by artificially increasing the used bandwidth. A DSSS transmitter converts an incoming data stream into a symbol stream where each symbol represents a group of 1, 2, or more bits. Using a phase-varying modulation technique such as quadrature phase shift keying (QPSK), the DSSS transmitter modulates or multiplies each symbol with a pseudorandom sequence which is called a "chip" sequence. The multiplication operation in a DSSS transmitter artificially increases the used bandwidth based on the length of the chip sequence.

IEEE defines the use of an 11-chip sequence which is actually a sequence of 11 -1 and +1 values. The spread signal can undergo as many as 11 phase changes per symbol period where a nonspreaded QPSK signal would undergo a maximum of one phase change per symbol period. The receiver correlates the received signal with the 11 chip sequence to obtain the originally sent data. Thanks to the redundancy in the transmitted information, the receiver can better identify the data even if the received signal was compromised by noise or interference.

What standards will there be to define the Protocol on the Backbone?

IAPP. The IEEE 802.11 Standard does only standardize the MAC and the PHY layers and does not give any directions for the higher layers. This implies that for the cable backbone there is no standard for handover of messages from access point to access point in case of roaming in a multi cell environment. Therefore the IEEE 802.11 standard on its own still does not guarantee compatibility between access points in multi vendor environments. For this reason Lucent Technologies, Aironet corporation and Digital Ocean came up with the Inter Access Point Protocol (IAPP), which allows for multi-Vendor interoperability. The IAPP enables wireless LAN system vendors to build systems providing real Interoperability. IAPP was finalized based on the inputs from interested parties, the majority of the IEEE members. The goal is to add this to the 802.11 standard in the future.

What Regulations to comply to?

Worldwide a number regulatory bodies are setting rules with respect to output power and spurious emissions. for Radio products to be used in their countries. Also the IEEE standard sets additional rules for spectrum and spurs. These rules translated to specific Radio requirements increases the complexity of radio design for Wireless LANs. A short summary of the radio regulations;

US, The FCC. Specifies a maximum output power of 30 dBm (1 Watt) at the products' connector. Effective Isotropic Radiated power 36 dBm (4 watt). The available frequency band 2400 MHz to 2483.5 MHz is directly limited by the so called Restricted bands at 2390 MHz and 2483.5 MHz, where absolute radiated levels have to be lower then -41 dBm.

Europe, The ETS. Standard specifies a maximum output 20 dBm EIRP (100 mW Effective Isotopic Radiated Power). Building a worldwide applicable product, reduces the design impact of the ETS spurious emission requirements significantly because the FCC forbidden band are more stringent.

Japan, MKK. Specifies the output power limit as 10 dBm per MHz (10 mWatt / MHz), in practice this is 18.5 dBm output power at the connector. The available frequency band in Japan is only from 2471 MHz through 2497 MHz (26 MHz), which limits the throughput significantly relative to other countries. For spurious emissions also the MKK requirements are covered by the equal or more stringent requirements of the FCC and the IEEE.

IEEE, specifies that all spurs outside 22 MHz from centerfrequency should be lower than 50 dB relative to the center frequency. The so called "Transmit Spectrum Mask". This translates to absolute levels of spurs outside the 44 MHz band of -53 dBm!

IV. THE MAJOR REQUIREMENTS FOR A WIRELESS LAN PRODUCT

A. General

For most users of a Wireless Local Area network product, it is of little importance what type of modulation or spread spectrum technology is available, or how it operates. The key requirements for wireless networking are:

- Ability to use it anywhere with Reliable Data Transfer
- High Speed Data Transfer
- Large coverage area (minimize cost, calculated in number of access points per meter)
- Compatibility with Other LAN products.
- Efficient Power consumption to save battery capacity on portable computing devices.

B. Form factor

With the need for mobility it is clear that for Wireless LANs there is a continuous focus on miniaturization. The most common form factor is the PC Card type of products. Integration in other devices like handheld and scanners, can result in even more stringent form factor requirements. Therefore designing today's wireless LAN product automatically implies chip level integration in different parts of the radio.

C. Power consumption

Power consumption, often confused with peak current consumption, is an important aspect in mobility. The battery life, depending on the application will be affected by the use of wireless connections. Wireless LAN products have different modes of operating. Transmit mode (TX), in which the Transmitter has to generate the required output power to be able to reach the other station. Receive mode (RX), where the receiver has to receive the package and needs to retrieve the original data. Sleep mode, which is the actual power save mode where as much as possible is switched off in order to save battery life time.

Most of the Mobile Platforms today can handle peak current consumption's for PC Card products of 300 mA, which sets the maximum requirement for wireless LAN designs in TX and RX mode. Of course anything below this value will help, but this is not where the real saving is. The total average power consumption is mostly defined by the consumption in sleep mode if a good power management scheme is used to control the products' hardware. This power management scheme will keep the product in sleep mode for 95%(or higher) of its time. Additional functionality in the Access point will be required for Buffering messages when the mobile unit is in sleep in order to achieve this kind of Power savings.

D. Speed

Users will usually look for the highest speed products or equivalents to wired products with 10 Mbps Ethernet being one of the standards compared to. With the IEEE 802.11 standard (2 Mbps for DSSS and 1 Mbps for FHSS), which now soon will become the standard for Wireless LANs, it is clear that whoever starts designing a radio today, has to look at alternative speeds. This is generating a hard design requirement for radios to be compatible with the IEEE 802.11 standard and allow for higher speeds.

E. Security

For radio communication often the perception exists that it is by definition less secure than a wired system. The IEEE 802.11 standard however is providing a security mechanism that is called "Wired Equivalent Privacy". This is a security mechanism which ensures the wireless link to be as secure as a wired link. This security mechanism is based on the RC4 algorithm and gives a Wireless LAN product the required security for the majority of applications.

V. DESIGN TRADE-OFF'S

A. DS vs. FH

In specifying both spread spectrum alternatives, members of the 802.11 working committee felt that DSSS would offer advantages in applications requiring reliability, robustness to noise, and peak data rate, while FHSS would offer advantages in applications that demand low cost. A closer look at DSSS and FHSS implementations reveals actual cost

and performance differences and highlight the issue of aggregate throughput supported in a wireless cell.

Modulation differences. The differences in performance, capacity, and price depends both on the choice of DSSS or FHSS and on the type of modulation scheme used. The choice of modulation scheme, however, isn't entirely arbitrary. The reliability and high data rates of the DSSS scheme is best realized using a phase-varying modulation such as (QPSK), or differential phase shift keying (DQPSK). The FHSS concept doesn't presume any specific modulation scheme but the IEEE 802.11 draft prescribes the use of Gaussian frequency shift keying (GFSK). Moreover, most existing FHSS implementations use some form of frequency shift keying (FSK).

The theoretical cost difference between DSSS and FHSS can be attributed to both the modulation and spread spectrum schemes. Compared to DSSS, the simpler FHSS scheme requires fewer DSP MIPS in the receiver to recover the spread signal. Therefore, an FHSS system could potentially use a lower cost DSP.

From the modulation perspective, the IEEE 802.11 committee selected GFSK for use in FHSS systems because it simplifies the design of the RF transmitter. The frequency component of an FSK signal conveys the content. The amplitude of the signal is unimportant. Such a modulation scheme is referred to as a constant envelope scheme. A low-cost, nonlinear power amplifier can be used to transmit the constant envelope signal without regard for clipping of the signal peaks.

QPSK, conversely, relies on accurate transmission of amplitude ripples to maintain the spectral purity of the transmitted signal. To avoid clipping of the signal peaks, designers of

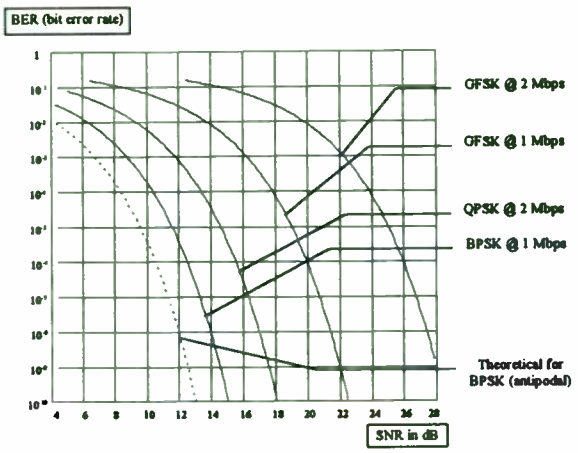


Figure 1

QPSK radios must use linear power amplifiers. Without question, nonlinear amplifiers cost less

than linear amplifiers. Moreover, many developers of wireless LAN products may lack the capability to design and manufacture linear amplifiers. On the other hand, companies with mixed-signal IC design expertise can minimize the cost difference.

Ultimately, the cost of a linear amplifier is easily justified relative to performance. QPSK-based DSSS, in fact, provides a significant theoretical advantage over FSK-based FHSS in terms of peak data rate and robustness to noise. Figures 1, 2 and 3 graphically depict this advantage. The first figure graphs the bit error rate (BER) advantage afforded by DSSS relative to FHSS, as a function of the SNR. This directly results in an improved probability of a reliable link at a certain sensitivity and/or range, as depicted in in figures 2 and 3.

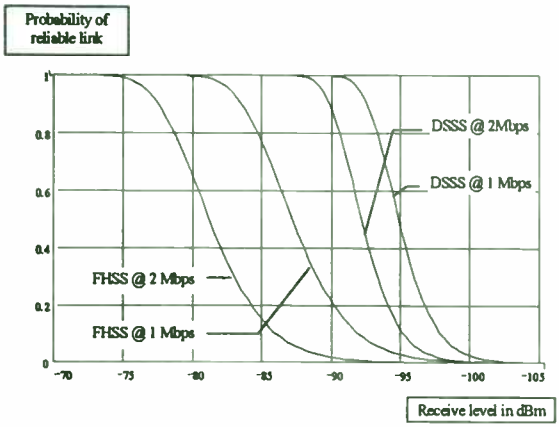


Figure 2

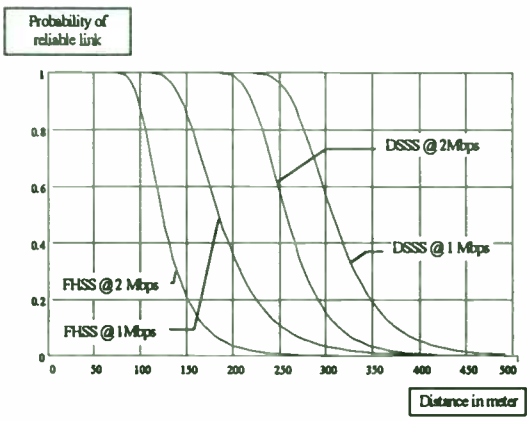


Figure 3

Peak data rates and aggregate throughput. As Figure 1 shows, the BER of GFSK-based FHSS at 2 Mbps makes transmission at that rate unreliable. The IEEE 802.11 draft actually describes FHSS LANs operating at a standard speed of 1 Mbps, with optional 2 Mbps speeds possible in optimal-quality conditions. Meanwhile, 2-Mbps QPSK-based DSSS systems offer significantly better BER than FHSS systems operating at a peak rate of 1 Mbps. The IEEE 802.11 draft describes standard DSSS links at 2 Mbps using QPSK with fallback to 1-Mbps binary phase shift keying (BPSK) in noisy conditions.

Perhaps even more important than peak data rate, however, is aggregate throughput. The former is key to how fast a single file can be transferred but the latter determines how many users can effectively connect to a wireless LAN via a single access point (AP). As you might expect based on peak data rates, a DSSS AP offers substantially more aggregate throughput than can a FHSS AP. The advantage in most applications, in fact, is far beyond the 2:1 peak data rate difference.

To maximize aggregate throughput, you need to minimize latencies related to medium access, to minimize errors that result in the rebroadcast of packets, and to optimize packet efficiencies. Ultimately, the IEEE 802.11 standard will prescribe that both DSSS and FHSS systems use similar medium access schemes. FHSS systems, however, suffer latencies on each frequency hop. FHSS systems also suffer from more frequent rebroadcast of packets because the systems are fundamentally more susceptible to noise.

Moreover the IEEE 802.11 recommended packet size is only 400 bytes for FHSS, while it is 1500 or 2400 bytes for DSSS. This means that FHSS systems will have to break up almost all long data packets into fragments. A transmission preamble and a MAC header are needed for each fragment as well as a separate acknowledgment frame per transmission. These packet issues significantly add to the overhead of FHSS systems transmitting long packets. The fact that DSSS uses the airwaves more efficiently can result in a 4 to 10x difference in realized performance.

Capacity and channels. The higher data rate and lower latency offered by DSSS translates directly into the ability to serve more users from a single AP. WaveLAN, in fact, has been successfully deployed in point-of-sale applications with

more than 120 nodes connected to a single AP.

While the capacity comparison between DSSS and FHSS systems is straightforward when a single access point is concerned, multiple access points complicate the matter significantly. In fact, multiple APs can be collocated in the same area to boost aggregate throughput in either type of system. A close look will reveal just how much capacity can be reasonably realized through multiple access points.

Consider systems that meet US or European governmental regulations for operating in the 2.4-GHz-band designated for industrial scientific and medical (ISM) applications. The regulatory agencies have set aside an 83.5-MHz band for unlicensed use by spread-spectrum-based devices. A DSSS system such as WaveLAN requires an 11-MHz channel to transmit a 2 Mbps signal. Lucent Technologies actually reserves a 22-MHz band for each channel to minimize the risk of crosstalk between channels. The WaveLAN design breaks the available 83.5 MHz of bandwidth into eight separate channels. Adjacent channels overlap and access points using adjacent channels would not typically be located in the same or adjacent cells.

The WaveLAN frequency allocation does result in three channels that are separated by more than 22 MHz. APs using these three channels can be collocated thus tripling the available aggregate bandwidth. The remainder of the channels can complete the layout of a cell structure that minimizes interference between cells.

Each FHSS AP, meanwhile, uses almost the full 83.5-MHz band for hopping. To collocate FHSS APs, you must acknowledge that the APs will occasionally collide on a hop. Different hopping patterns minimize the collision risk to a degree, and can result in a near linear increase in total shareable throughput with a low number of collocated APs.

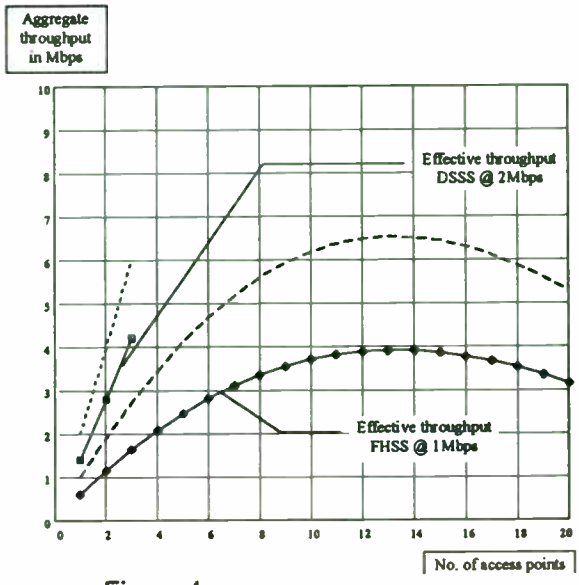


Figure 4
(Applicable for FCC and ETS countries)

Some FHSS proponents have even claimed the ability to collocate 10 or more access points and claimed a 10x or greater linear ramp in aggregate throughput. To date, such capabilities haven't been proven in real-world demonstrations.

Practical FHSS limitations.
Theoretical calculations, in fact, show substantially different results between DSSS and FHSS (See figure 4). The calculations reveal degradation that occurs as more access points are collocated thereby increasing the number of collisions. Such collisions require regular retransmission by both APs.

Such calculations show that when using 1-Mbps FHSS access points, aggregate bandwidth (taking latencies and packet overhead into account) never exceeds 4 Mbps regardless of how many APs are used. Moreover, more than 10 APs are required to reach 3.7 Mbps in aggregate throughput. DSSS systems can offer more than 4 Mbps of aggregate throughput with only 3 APs.

Minimizing reuse distance. Not only does a detailed examination reveal that DSSS systems scale significantly better than FHSS systems, but the former can also be packed more closely together. The QPSK-based DSSS system is more robust relative to cochannel interference than is GFSK-based FHSS systems. This advantage means that the same channel in DSSS systems can be used in nearby cells with only occasional interference. The IEEE 802.11 draft spec recognizes this fact in how it defines a difference in signal capture with respect to power level. The spec has set the DSSS defer level for valid transmissions 15 dB above the FHSS defer level. This defer threshold advantage allows two DSSS cells using the same channel to be packed four to eight times as dense as two FHSS cells that use the same hop sequence. This same behavior accounts for a lower susceptibility to interference in general.

B. Conformity to Standards IEEE and IAPP

Is it an option at all to not to design according to a Standard? No, this year, for wireless LANs, is the year of standardization. There is a strong move, driven by customer requirements, towards systems conform to an open standard. It is clear that given the level of support in the IEEE by major LAN providers, the 802.11 will be the open standard for wireless LANs once its there. Further, the only known way to provide real Inter vendor inter-operability, is to adhere to the IAPP standard. For any vendor starting a Wireless LAN design today, this is probably setting the most important set of parameters for his design.

C. What chips to use

Given the form factor requirements and functionality it is a must to achieve a high level of integration in the design. The question is, does one use integrated components available on the market, or is ASIC development required to be able to meet al requirements. A thorough investigation at the start of a Wireless LAN development will need to be performed to summarize the available alternatives. New development programs within Lucent Technologies showed that all the large building blocks available in the market have their own disadvantages which limits the designs' ability to meet the requirements. For example; available MAC controllers usually have on board processors to be able to adopt the latest IEEE changes (where it is still questionable if it can handle the final standard), the consequence of this is a high current consumption device.
Also there are no devices available supporting high speed radio designs beyond IEEE, which also still guarantee IEEE compatibility.
Although several man-years of development are involved, Lucent Technologies decided to start their own chip set development in order to design a Wireless LAN product with a good price / performance / functionality balance.

VI. DESIGNING THE RADIO

A. Radio Development

The radio development is mainly focused high integration to fit into the PC Card size and a highly linear design for the transmit and receive path. This means that the components in use, e.g. transistor, are used a number of dB's below its 1 dB compression point. Blocking of unwanted signals is done with help of numerous filters (very steep S(urface) A(ucoustic) W(ave) filter). The 3.3 V requirement for platforms only supporting this, is a challenge for the Power stage design. It is difficult to achieve a Linear Amplifier at low voltage generating the required output power. Integration of RF parts, such as Filters and VCO's, requires some very specific expertise in RF chip technology and RF radio design. Therefore in most cases Companies have to bundle their strengths like Lucent Technologies does with Partner alliances to achieve the right form fit and function at low cost. PCB design for this kind of applications is an art,

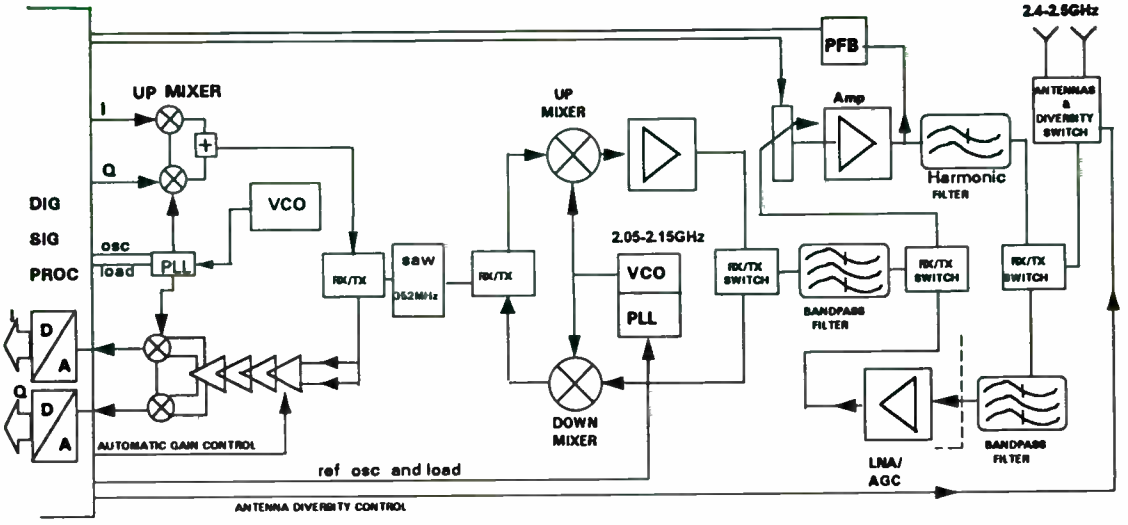


Figure 5.

with the required density and RF characteristics the PCB becomes a high tech RF component. Striplines and embedded filters complicate the PCB design even more, only very few parallels to conventional digital PCB design still exist.

B. Radio block diagram

The Radio blockdiagram (Figure 5) shows a design for a DSSS Radio in the 2.4 GHz band.

The block diagram shows I and Q modulation and demodulation, into the Digital Signal Processor. In the Transmit path the signal is via a mixer transformed an intermediate frequency (352 MHz), after filtering the signal is transformed to the 2.4 GHz band. A Linear power amplifier generates the required output power to the transmit antenna. In the Receive path the signal is coming in via one of the antenna's (antenna diversity) and fed into the Low Noise Amplifier (LNA). The LNA is one of the most important pieces of the radio design since the sensitivity of this block can be directly translated into range. Further down the receive path the signal will be fed into the automatic gain control block to adjust the receive level on the inputs of the DSP.

C. MAC and DSP chip development

Both the MAC and the PHY functionality require large scale integration because of their complexity. For the MAC functionality there are some chips available in the market today, these devices however do have some disadvantages with respect to current consumption, required support chips and size (form factor). Therefore Lucent Technologies for example decided to do its own MAC development for their next generation Product. The DSP chip is a very critical component in the Radio design, it carries the spreading and the modulation functionality. For LAN vendors to prepare for higher speeds, beyond IEEE 802.11, significant investments are required in DSP development. The only alternative for LAN Vendors is to use of the shelf available chips which has its limitations with respect to migration to higher speeds.

D. Antenna Development

Integrated antenna's are preferred in this type of application, this way the end user does not have to worry about antenna connections and placement. Also the cost of the total unit can be kept as low as possible with internal antennas. Two antenna's are used which are placed to have optimum

sensitivity in both a horizontal and vertical polarization. One of the two antennas is selected during the training based on signal quality. If thus one antenna is in a fade, the other antenna will be selected automatically. The performance improvement is approximately 10 dB by using this so called Antenna diversity. This considerably increases the coverage area of the system. External antenna's are only used when the application of the internal antenna through its use is hindered by obstacles that prevent radiation.

VII. CONCLUSIONS AND FUTURE DIRECTIONS

A. Technology DSSS vs. FHSS

A look to the future suggests that DSSS will be the best technical choice for wireless LANs operating at two to five times current 2 Mbps speed as available today. FHSS proponents have hinted that they can double data rates through new modulation schemes, however it is likely that more expensive linear amplifiers will be required, which are already included in DSSS.

Our research indicates that DSSS has the potential to make a jump to 10-Mbps data rates. In such a case, three collocated access points could afford an aggregate throughput of 30 Mbps. Lucent Technologies has extensive experience in modulation algorithms and radio designs that will enable a move to 10 Mbps.

Today, FHSS offers a small advantage in implementation cost. Even this advantage will shrink as companies such as Lucent Technologies combine their DSP and mixed-signal expertise to develop single-chip DSSS interfaces. Meanwhile, virtually all applications benefit from the faster and more robust DSSS scheme. Although this does not mean to say that there will be no future for Frequency Hoppers as a lower speed (utility) LAN if costs and prices can be reduced to a level where is a significant reduction below that of Direct Sequence.

C. Flexible Wireless systems

Flexibility will be key in future systems, where different applications require different system specifications with respect to Range and Speed. For example a retail environment requires relative low speed and high coverage, where as in an office environment usually higher system throughputs are required. Since data throughput and range, by nature are each others enemy in Radio design, future systems will have to adapt to the customer needs on these parameters. This way the customer can design its wireless system according to local throughput requirements in the system. By simply increasing the density of access points which are automatically switching speeds (1 and 2 Mbps IEEE and higher speeds 10 Mbps-30 Mbps), performance tuning based on customer needs can be achieved. Today's systems only allow for duplicating the number of access points, which in case of FHSS is only adding marginal steps, and for both systems FHSS and DSSS is an expensive solution for a high speed system.

CELLULAR/CORDLESS DESIGN, I

Cellular/Cordless Design, I

Session Chairperson: Thomas Brinkoetter,
Tektronix, Inc. (Beaverton, OR)

COMMUNICATING VOICE, DATA, VIDEO VIA GSM NETWORKS.

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ABSTRACT

The need to communicate via voice, data, and video, anytime and anywhere has resulted in new technologies rapidly unfolding and being successfully implemented in the Americas.

Rapid advances in personal telecommunications such as the advent of PCS1900, Wireless Local Loop, and CT2, have allowed consumers to increasingly avail themselves to new voice services.

The advent of low cost dual mode (Analog / Digital) and tri-mode (Analog / IS-136 / GSM) cellular phones and reductions in service costs have resulted in a growing number of users benefiting from the advantages offered by cellular telephony. This enables the users to use the same phone at home, in the car or at the office for voice and data services.

Being able to access the internet via a hand held cellular phone is a feature that is increasingly being coveted by the mobile business person.

Wireless video technology offers real time, cost effective, near broadcast quality services being offered over Wireless Local Loop and Fixed Wireless Access networks. A standard National Television System Committee (NTSC) video format occupies a bandwidth of 4.5 MHz which means that in a FM system the bandwidth will vary from 14 to 27 MHz.

In the ISM bands, 24MHz, 81MHz and 123MHz are the usable spectrum found in the 900MHz, 2400MHz and 5700MHz bands, respectively.

Propagation of direct broadcast services via satellite, fixed wireless services in developing and remote regions, and the installation of GSM platforms to support GSM based PCS1900 in N. America are rapidly unfolding the information age for voice, video and data.

The deployment of Hybrid Fiber Coax by telephone and cable operating companies after deregulation of cable and telephone industries has spawned new interactive services.

This paper discusses voice, data and video services over a GSM network. Diagram below shows how different services will allow for the remotest and urban areas to be connected.

Figure 1. PCS SERVICES

1. PRIMARY GSM

In primary GSM the mobile station transmits in the 890 - 915 Mhz (uplink) band; and the base station in the 935 - 960 Mhz (downlink).

The basic rate is 13 kb/s, using residual excited linear predictive coder (RELP) with a long term predictor (LTP). Speech is processed in 20 msec frames. Each speech frame consists of 260 bits, a 3 bit cyclic redundancy check (CRC) is added to 182 most significant bits, 4 tail bits making a total of 189 bits. Through a half rate channel encoder 378 bits are produced. The remaining 78 least significant coded speech bits are then added making a total of 456 bits.

Information is conveyed in a 8 time slot frame of duration 4.615 ms. The transmitted bit rate is 270.83 kb/s (approx. 156.25 bits in 0.577 ms). A 26 multi-frame structure is used for the traffic channel combinations and a 51 multi-frame structure is used for signaling combinations. The total length of a 26 frame structure is 120 ms, i.e. (26 x 4.615 ms).

We have 125 carriers with widths of 200 kHz each for a total of 125 x 8 (1000 channels). As indicated above a duplex spacing of 45 Mhz is used.

2. CHANNEL DATA RATE

In primary GSM there are five different data channels. For the purpose of this paper the highest data rate channel is discussed. TCH/F9.6 is the one with the highest data rate.

A user bit stream is divided into four blocks of 60 bits each, for a total of 240 bits. Four zero bits are added to the 240 bits to reset the decoder. A convolution coding scheme of r = 1/2, K = 5 is applied to the 244 bits which results in 488 coded bits.

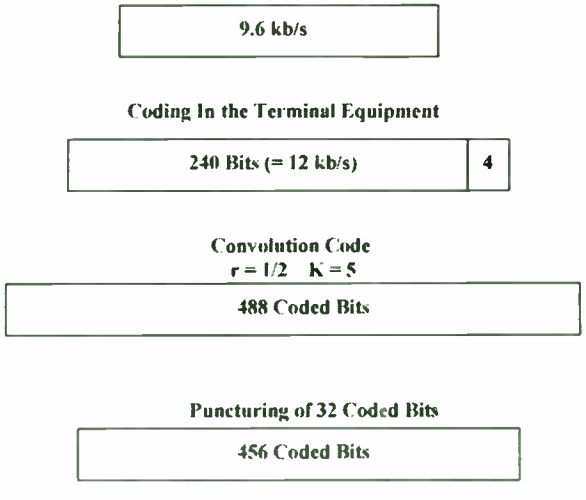
The 488 bits are punctured to fit the 456 bits per block scheme as used in coded speech data. These 32 bits (488 - 456) are not transmitted.

The blocks are spread over 22 bursts with its Slow Associated Control Channel (SACCH) and idle frame. A complex mapping scheme is performed on 456 bits so as to fit the 22 bursts. The scheme breaks up the 456 bit block into 16 parts of 24 bits, and 2 parts of 18 bits, 2 parts of 12 bits, and 2 parts of 6 bits each. A time slot or burst consists of information from either 5 or 6 consecutive data blocks, that is 4 parts of 24 bits (4 x 24 = 96 bits) and either 1 part of 18 bits (1 x 18 bits = 18) for a total of 114 bits (96 + 18) or 1 part of 12 bits (1 x 12 = 12) and 1 part of 6 bits (1 x 6 = 6); for a total of 144 bits (96 + 12 + 6).

The first and twenty-second bursts contain 6 bits each (2 x 6 = 12). The second and twenty-first burst contain 12 bits each (2 x 12 = 24). The third and twentieth burst carry 18 bits each (2 x 28 = 36). Now 6 bits are used up and 16 bursts remain of the 22 bursts we started with. 24 bits in each of the fourth through nineteenth bursts (16 x 24 = 384). All 456 bits are thus accomodated in the 22 traffic channel frames. The structure repeats itself at every fourth burst so that the bits are distributed over 22 time slots diagonally. Each burst carries 5 or 6 different data contirbutions, depending on which frame in the traffic channel multiframe is refered to.

Even though the transmission data rate is 9.6 kb/s, the actual rate is brought upto 12 kbps though coding in the customer equipment. See Figure 2 below.

Figure 2. CODING SCHEME FOR 9.6kb/s DATA TRANSMISSION



3. MULTIMEDIA COMMUNICATIONS TERMINAL

H.324 standard is an international standard for a videophone terminal operating over the public switched telephone network. In 1995 the ITU began work on the H.324 series of recommendations for application to mobile networks, called H.324M.

Table 1. ITU NETWORK & TERMINAL STANDARDS

	PSTN	MOBILE
Overall	H.324	H.324M
Video	H.261/ H.263	H.261/ H.263
Mux	H.223	H.223 (A)
Ctrl./Sig.	H.245	H.245
Audio	G.723.1	G.723.1 (C)
Comm. Inter.	V.34 Modem	Mobile Radio

All H.324 terminals offering video communications support H.263 and H.261 video codecs. The five standardized image formats are 16 CIF, 4 CIF, CIF, QCIF and SQCIF.

Due to incompatibility betweeen the TV broadcast standards, specific picture structures, CIF (Common Intermediate Format) and QCIF had to be employed.

The QCIF format employs half the CIF spatial resolution in both horizontal and vertical directions, full CIF is optional. For videophone applications QCIF is used where head and shoulder pictures are required. Conversely, the full CIF format is used for teleconferencing.

The H.263 coding algorithm is an extension of H.261. H.263 describes a DPCM/ DCT video coding method. Both standards use techniques such as DCT, motion compensation, variable length coding, and scalar quantization and both use the well known macroblock structure. The maximum data rate for H.261 isthat associated with the V.34 modem i.e. 28.8 Kp/s.

Table 2. CIF & QCIF PARAMETERS

PARAMETER	CIF	QCIF
Coded Pictures Per Second	29.97	(or Integral submultiple)
Coded Luminance Pixels Per Line	352	176
Coded Luminance Pixels Per Picture	288	144
Coded Color Pixels Per Line	176	88
Coded Color Lines Per Picture	144	72

If conventional 8 bit PCM encoding was applied to a standard TV signal, a bit rate of 90 Mb/s would be required for transmission. Compression technology is used to reduce this bit rate to the primary rates (1.544 Mb/s, 2.048 Mp/s), fractional primary rates (384 Kb/s) and basic (64 Kp/s and multiples) for economical transmission. The compression function is performed by a video codec and H.261 is the ITU recommendation.

Table 3, gives the basic resolutions and transfer rates for video telephony, video conferencing and Digital TV.

Table 3. INFORMATION VOLUME & TRANSMISSION RATES

	VIDEO TELE.	VIDEO CONF.	DIGITAL TV
Spat. Res.	176X144	352X288	720X480 (NTSC) 720x576 (PAL)
Temp. Res.	30 f/s	30 f/s	30 f/s
Color Repr.	.....Luminance (Y)..... .....Chrominance (Cr, Cb).....		
Bit Rate Req.	64kp/s x n	64kp/s x n	30-45Mb/s or 140 Mb/s

The G.723.1 speech coder can be used for a wide range of audio signals but is optimized to code speech. The system's two mandatory bit rates are 5.3 Kp/s and 6.3 Kp/s. The coder provides a quality essentially equivalent to that of a POTS call. For clear speech or with background speech, the 6.3 Kb/s mode provides speech quality equivalent to the 32 Kb/s G.726 coder. The 5.3 Kp/s mode performs better than the IS-54 digital cellular standard.

4. GSM / HSCSD

GSM standard is evolving to incorporate High Speed Circuit Switched Data (HSCSD), which will boost user capacity upto 64 kb/s and higher.

GSM uses TDMA technology which divides each 200 kHz carrier into eight time slots. To provide a single voice channel one time slot is used, also one time slot isused to provide a single 9.6 kb/s data circuit. The TCH/F9.6 channel was explained above. However, all eight time slots will be used to prvoide one 64 kb/s circuit. This will require a new radio link protocol.

HSCSD has an inbuilt bandwidth on demand capability, hence the service will provide whatever speed they require upto 64 kb/s.

Fast setup times and high link quality will be achieved when such a 64 kb/s wireless terminal is interconnected to the ISDN network, giving the user complete end-to-end digital connectivity.

HSCSD will spwan several new applications for mobile communications, video conferencing, medical tele-imaging and scaning. Connecting to the internet and downloading text with high graphic content will be made easy and as quick as terrestrial services.

5. ODEUM OFFERINGS

Odeum Microsystems Inc. offers QPSK and QAM demodulators for DVB broadcasts suitable for Receiver implementations in either headends or customer terminals. Furthermore, MPEG audio and video decoders available from Odeum are suitable for video decoding in PDAs, multimedia terminals or in file servers for World Wide Web services.

CONCLUSION

Communicating video over GSM networks is becoming an increasing reality. HSCSD will allow each carrier in GSM to carry video and audio upto 64 kb/s. H.324M will ensure compatibility betweeen mobile terminals worldwide to allow for video telephony and video conferencing.

REFERENCES

[1] GSM Technical Specifications, ETSI, Sophia Antipolis.

[2] CEPT TS 46-20 Recommendation and CCITT Q.920/921 Recommendations.

[3] ITU, Recommendation H.320: Narrowband Visual Telephone Systems and Terminal Equipment.

[4] ITU, Recommendation H.261: Video Codec for Audiovisual Services at P x 64 kb/s.

[5] ITU, Recommendation H.324: Terminal for Low Bit Rate Multimedia Communication.

[6] ITU, Recommendation for H.263: Video Coding For Low Bit Rate Communication.

[7] ITU, Recommendation H.324M: Terminal for Mobile Multimedia Communication.

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An Simple and Efficient Method of Adding a Voice Recording and Playback System into a Digital Cellular Phone.

Abstract

Cellular and mobile telephony has experienced tremendous growth in the last decade. Various digital cellular schemes such as GSM, IS-54, IS-95, IS-136 and others have emerged in the last few years to address the capacity crunch in heavily congested areas. GSM has found itself as a very well accepted standard in Europe, Asia and the Middle East while in the US there are many competing technologies. Explosive growth in the digital cellular market has provided an opportunity and a challenge to cellular phone manufacturers at the same time. Their customers are demanding smaller size, lower cost, longer talk times, data modem interface and other attractive features such as a built-in voice recording. This article features a simple and efficient solution to implement a voice memo recording system by adding a specialized voice recorder chip to a digital cellular phone and compares its benefits to an all digital approach.

I. Introduction

Cellular phone manufacturers are constantly under pressure to release new models of phones with more user features and compact designs. This puts tremendous pressure on the development teams to re-engineer the phone architecture, software, hardware, and layout. Time to market with a new product is also very important for manufacturers to remain competitive.

An emerging trend in cellular phone handsets is the addition of 'voice' features. These voice features include: 1) the ability to record 'on-the-fly' conversations, to eliminate the need for writing down notes from a conversation and enable hands free driving safety, 2) voice memos, to record voice reminders to oneself, and 3) integrated telephone answering machines, to screen or capture otherwise missed calls and store those messages right in the handset. The basic function which enables these new features to is the ability to reliably record and playback voice. To meet the requirements of cellular handset performance, the solution must be low power, to conserve battery life, a small form factor, to enable a compact design, low cost to keep the retail pricing down, and reproduce high quality sound, to meet the expectations of consumers. Additional factors in design is development time and costs, since time to market and design investment are important considerations for any new products design.

Designers have several approaches available to them, especially in digital cellular handsets, where intuitively much of the required hardware to store voice digitally seems to be resident in the handset design. The design approaches described here compares available solutions to implement these voice functions using a GSM handset application as a digital cellular example.

This examination concludes a specialized, 3V, single voice record and playback chip is superior in power consumption, design cycle time, board space and cross platform flexibility compared to storing the digital voice data stream into digital memory

II. Overview of the GSM System

The GSM (originally Groupe Speciale Mobile -- now known as Global System for Mobile Communications) is a Time Division Multiple Access (TDMA) system for mobile communication of voice and data information. There are 124 channels in the system with 200 KHz bandwidth for the transmit and receive bands. There are eight time slots in each frame and the frame duration is 4.615 msec. Each time slot is assigned to a single mobile subscriber. The data rate on the channel is 270.83 Kb/s. The full rate speech coder has a rate of 13 Kb/s for the speech data. The speech coder operates on a 13-bit speech data sample with a sampling rate of 8 ksps. The sample data is reduced to coefficients on a 20 ms window. Each window is 20 ms wide. Therefore 160 samples in each window which are converted to the coefficients of 260 bits for each window.

The RF section typically consists of the front-end RF switch, low noise amplifier (LNA), filters, down-converter, frequency synthesizers, I/Q demodulator, I/Q modulator, power amplifier, power control circuitry and a VCTCXO. The received signal is in the 935-960 MHz band with a 200 KHz channel bandwidth and spacing. The transmit signal is in the 890-915 MHz band and 200 KHz channel bandwidth and spacing. The LNA amplifies the signal, the down converter brings the amplified signal to an intermediate frequency and the I/Q demodulators resolve the signal into a baseband I and Q data stream. The I/Q modulator accepts the baseband signal and upconverts it to the RF. The power control circuitry does the power ramp up control and the VCTCXO provides a voltage controlled temperature compensated crystal reference frequency to the synthesizers.

The baseband sub-section consists of a high performance DSP, a mixed mode ASIC with A/D, D/A converters, and analog interface to microphone and speaker. The DSP performs the channel equalization, decryption, de-interleaving, channel decoding, speech decoding, speech encoding, channel encoding, interleaving and encryption of data. The voice band and base band signal quantization and reconstruction is typically performed by the mixed mode ASIC. The system microcontroller implements the GSM protocol stack layers 2 and 3, the code to run the DSP engines, memory management, man-machine interface to keyboard, display and battery power management.

III. Digital Voice Recording in a GSM Phone

To digitally store voice messages in a GSM phone, voice data from the GSM baseband section needs to be accessed, routed and stored into available digital memory. With the full-rate speech codec running at 13Kbs, 1 Mbit of memory stores 79 seconds of voice data.

Since the data stream between the channel codec and the voice codec is usually in a serial format and most of the high density memories have parallel data inputs and outputs, additional serial to parallel and parallel to serial converters are required to store this data into memory.

A typical block diagram of the GSM phone utilizing digital memory to record and playback voice information is shown in Figure 1.

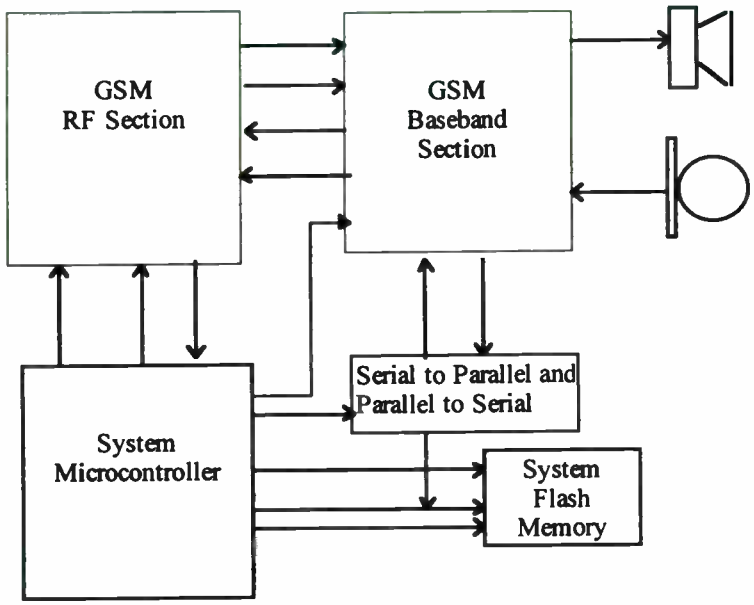

Figure 1

In a typical GSM phone implementation, approximately 750 Kbytes to 900 Kbytes (6 to 7 Mbit) of Flash memory would be required for the protocol stack, layer 1, layer 2 and layer 3, human interface, etc. Utilizing one 8Mb (1Mb x 8) Flash memory to store this program code means there remains excess Flash memory which could theoretically store approximately 80 to 160 seconds of voice data. However, due the block/sector erase structure of Flash memories entire blocks/sectors need to be free to allow storage and deletion of voice messages without affecting stored system program code. In addition, bus access timing and memory read, write or erase cycles need careful consideration to avoid bus conflicts between the microcontroller accessing the memory for GSM protocol and the voice message read, write or erase.

GSM speech frames operate on a 20 ms window and some Flash memories have programming times as high as 10 ms. DSP engines can take as much as 8 to 9 ms or more for the channel encoding/decoding and speech encoding/decoding process. This could be potentially problematic for 'on-the-fly' recording. Well thought out software architecture and implementation is needed to avoid these problems.

Additional and/or alternative message storage can be accomplished by utilizing separate Flash memory which would avoid some of the bus contention concerns. However, in either case software needs to be developed for the message and memory management of stored voice messages.

4Mb Flash memories are usually available in either block write/erase mode or sectored write/erase mode. In the memories with block write/erase mode there are usually 3-4 main blocks of 128K x 8 which are available for storage. If no special memory management techniques are implemented, this would imply that only 3-4 messages could be stored in the entire chip, one message in each block. Each message would have to be less than 80 seconds in length. If any message exceeds 80 seconds in length, then fewer than 3 messages would be stored on the chip. Sectored write/erase memories have sector size of 64Kbytes which can be individually erased or written, and thus would provide up to 8 messages of 40 seconds each.

To optimize the storage of messages shorter than 40 seconds (or the equivalent duration of the available block or sector), additional software management is needed for the 'housekeeping' of the message pointer. When a message which only occupies a portion of a block or sector needs to be erased, the microcontroller could re-write the remaining of stored messages in an unused block and then erase the entire block. This 'garbage' collection method does compact the storage space and improve message flexibility, but also requires one blank block/sector to be available at all times. It also increases the software complexity and the power consumption because of the additional power consumed by the microcontroller to process the memory management and the additional power required to erase and rewrite within the memory. If a separate digital memory chip is utilized for voice, then appropriate chip selects and read/write signals would also be required. The software development required for the digital storage of voice data represents the largest component of development time and cost in this implementation.

Design layout will have to consider the board space needed for the serial to parallel and a parallel to serial interfaces and a separate memory, if used, for this design. Devices such as a 74HC7597 and a 74HC4094 to interface the serial port on the DSP side and the parallel bus of the Flash memory. These devices come in 16 pin SOPs and the Flash memory in a 48 pin TSOP. Figure 2 shows the block diagram of the digital voice storage using a separate Flash memory. There are some serial input/output memories also available for voice message storage which eliminates the need for the serial to parallel and parallel to serial converters. Serial input/output memories such as serial Flash or SRAM still mean additional packages over the system memory requirement are needed, plus the software support for addressing and accessing the memories, memory management.

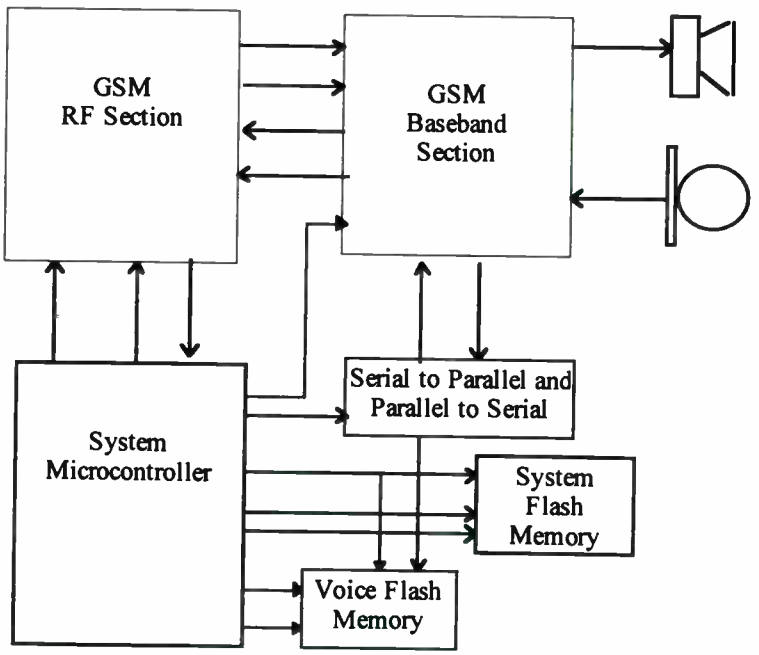

Figure 2

Serial Flash and SRAM memories software development would involve a few extra steps in interfacing with the DSP. Typically the format used by the voice codec and DSP to communicate is different that the format used by the serial memories to read and write from a controller. After the serial data between the DSP and the voice codec is intercepted, it is necessary to reformat it to write into the serial memory. A similar situation will arise in reading from the serial memory and sending the data to the voice codec for playback of recorded messages. Additional glue logic may be necessary to accomplish this data transfer between the microcontroller, DSP and voice codec. The standard controls such as chip enable, chip select and serial clock signals would also be required for interfacing with the serial memories.

SRAM also requires battery back up to retain stored voice data which increases power consumption. A separate lithium battery is needed to preserve stored messages when phone batteries have been discharged or are being replaced. This amounts to extra cost, weight, size and complexity in implementation. Figure 3 shows the SRAM implementation.

Intelligent memory and message management can be implemented in the software to maximize the memory storage when messages are erased out of sequence. It would read and re-write messages to occupy a contiguous block of memory when a message has been erased. This would optimize the memory storage but would result in additional power consumption due to the read and write operations on the Flash memory or serial SRAMs.

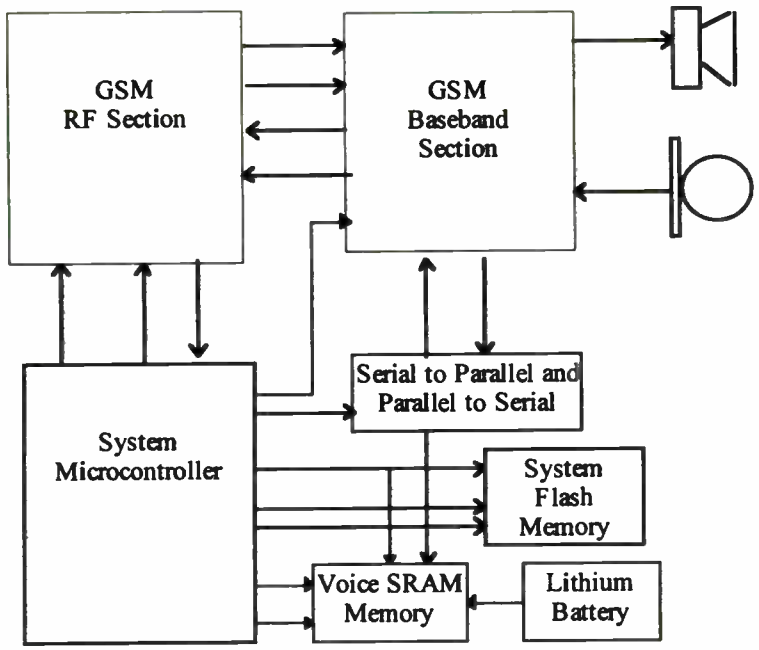

Figure 3

In either case (serial or parallel memories) board space considerations are needed to make to room for the added memory and interface Ics.

Power consumption of this type of solution is considered next. The Flash memory required in this digital voice data storage system consumes about 90 mA in the record or playback mode and about 130 µA in standby mode. The DSP also contributes to the current consumption while it is executing the code for the speech codec as does the codec itself. Typical speech encoder and decoder function requires about 5 MIPS loading on the DSP. When in the playback mode the DSP loading is about 1.5 MIPS and when in the record mode about 3.5 MIPS loading of the DSP is typical. Given these loadings, the DSP consumes approximately 75 mA while active and 6 mA in standby mode. The codec consumes about 18 mA while active in the recording or playback mode. Thus the total current consumption for the digital implementation will be typically 183 mA in active mode and less than 10 mA in standby mode. Figures 4 and 5 show the systems power consumption during 'on-the-fly' message recording, message playback and standby modes for the system utilizing resident system Flash memory and dedicated Flash memory for voice storage, respectively.

Device	**Record**	**Playback**	**Standby**
DSP Engine / Core	75 mA	65 mA	6 mA
System Flash Memory	80 mA	80 mA	130 µA
Micro-controller	30 - 45 mA	30 - 45 mA	2 mA
Serial to Parallel	3-6 mA	-	-
Parallel to Serial	-	3-6 mA	-
Codec, D/A, A/D	18 mA	18 mA	30 µA
Total	**~ 224 mA**	**~ 214 mA**	**~ 8 mA**

Figure 4

Device	**Record**	**Playback**	**Standby**
DSP Engine / Core	75 mA	65 mA	6 mA
System Flash Memory	80 mA	80 mA	130 µA
Voice Flash Memory	90 mA	80 mA	130 µA
Micro-controller	30 - 45 mA	30 - 45 mA	2 mA
Serial to Parallel	3-6 mA	-	-
Parallel to Serial	-	3-6 mA	-
Codec, D/A, A/D	18 mA	18 mA	30 µA
Total	**~ 314 mA**	**~ 294 mA**	**~ 8 mA**

Figure 5

Voice Storage Utilizing a Specialized Voice Record and Playback Chip

Voice storage and retrieval can also be achieved by utilizing a voice recording and playback chip specifically designed for cellular phone integration. The block diagram of this type of solution in GSM cellular handset is shown in Figure 6.

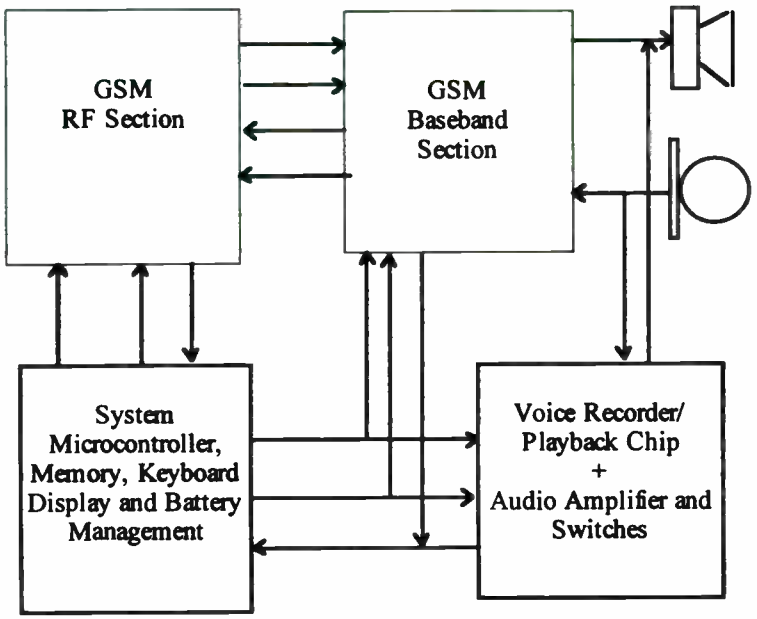

Figure 6

This 3V chip stores analog voice and audio signals directly into on-chip nonvolatile memory. The product is available in a series of durations ranging from one to four minutes. The overall device duration is determined by the sampling rate selected. The highest sound quality is achieved by sampling the audio inputs at an 8KHz rate. Other available sampling rates include 6.4KHz, 5.3KHz and 4.0KHz. Because of its analog input and outputs, this device interfaces directly to the speaker and microphone signals, which avoids involving the DSP software for speech encoding and decoding or adding code to the protocol stack, layer 1, layer 2 and layer 3 of the GSM protocol. The voice recording and user interface is controlled via a 3-pin serial peripheral interface (SPI), which connects directly to the system micro-controllers standard 8-bit general purpose I/O (GPIO) port. This interface also provides the control for message management. This device is available in 28-pin TSOP packaging.

Besides the voice recorder two other ICs are utilized: switches are used as an analog multiplexer to select the audio input and output paths, and an audio amplifier with fixed gain drives the speaker. A 74HC4053 can be used as the analog mutiplexer switch, which comes in a single 16-pin SOIC package and a TDA7050T can provide the amplification and is available in a 8-pin SOIC . The GPIOs on the systems microcontroller control the switches for source selection between the audio input/output of the voice storage chip and the GSM baseband section and the speaker and microphone.

In layout, optimal device performance requires power supply decoupling capacitors and a good ground plane around the device to enhance the noise performance and audio reproduction. All the peripheral components should be placed as close as possible to the chip and lead lengths and trace lengths should be minimized. If possible, the RF and IF sections of the GSM radio section should be isolated from the baseband section of the phone to avoid noise, spurious injection or pickup from the proximity of resonating components.

Due to the serial architecture of this devices nonvolatile memory array and its ability to be addressed, read, written and erased by row, software development for message management and control of this voice record and playback chip is straight forward. Figures 7 shows the basic flowchart for recording 'on-the-fly' conversations.

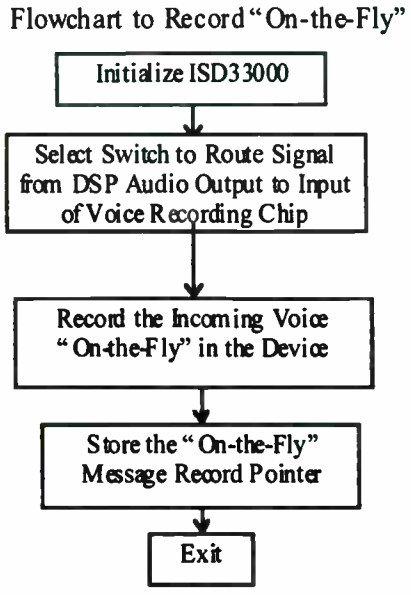

Figure 7

The power consumption of this solution is minimized because of the 3V supply and low current consumption characteristics of this specialized voice record/playback chip. This translates into longer battery life. Figure 8 displays the total power consumption for recording, playback and standby. For instance, in standby mode this device contributes is less than 10 µA. When in active mode, it adds less than 45 mA to the systems power consumption. Because this audio chip plays directly to the speaker and does not require the baseband or codec functions, or microcontroller processing past the initial control, the systems power consumption during playback is minimized.

Device	Record	Playback	Standby
DSP Engine / Core	75 mA	6 mA	6 mA
System Flash Memory	80 mA	130 µA	130 µA
Voice Rec/Play Device	40 mA	30 mA	10 µA
Micro-controller	30 - 45 mA	2 mA	2 mA
Switches/Amp	8 mA	20 mA	8 mA
Codec, D/A, A/D	18 mA	30 µA	30 µA
Total	**~266mA**	**~58 mA**	**~16 mA**

Figure 8

IV. Comparison Between the Digital Storage and the Specialized Audio Chip Storage for Recording and Playback Voice

From the above analysis of the two methods of implementation for a voice recording and playback system in a GSM cellular phone, the specialized recording / playback chip demonstrates several advantages. The first and foremost is the development time required. The primary component of the development time for the digital approach is in the software development. In the case of the specialized voice recording device the software development is simplified because of its ease of control and row accessible memory array. Figure 9 estimates the total development time of each approach by development task. By this estimate total development time using the specific voice record / playback device is 2-3 weeks as opposed to the digital approach which requires 2-3 months.

Development Tasks	Voice Recording / Playback Device	Digital Storage Flash / SRAM
Hardware Design	3 days	
Printed Circuit Board Layout	1 day	
Software Development	10 days	
Storage Memory Management	2 days	
Message Management	4 days	
Total Est. Development time	**3 - 4 Weeks**	**2 -3 Months**

Figure 9

Power consumption utilizing the voice record and playback chip is also substantially less than the digital implementation especially during message playback. Figure 10 compares the two methods power consumption in each mode. Considering longer battery life and smaller, lighter phones are critical features for cellular handsets, the benefits of the lower power consumption of the dedicated voice recording/playback device are significant.

Mode	Voice Recording / Playback Device	Digital Storage Flash / SRAM
Record	266 mA	316 mA
Playback	101 mA	294 mA
Standby	16 mA	8 mA

Figure 10

V. Conclusion

New cost effective features will continue to be added in cellular phones to increase the utility and value to the end-user and to help differentiate cellular phones between manufacturers. A voice recording and playback system based on a specialized 3V, audio record / playback chip was discussed and compared to alternative digital voice storage systems. The comparison shows that the specialized audio chip requires less development time and system power and provides high quality voice reproduction. The shorter development time enables an accelerated time to market of new 'voice' features, such as call recording, voice memos and integrated telephone answering machines. Also the single-chip form factor and superior power performance insures the final cellular design will remain compact and provide long battery life.

Most digital cellular handset designs are similar in architecture regardless of their protocol standards (IS-54, IS-136, CDMA, etc...). Because this audio chip is integrated along the analog audio path and not in the digital baseband section, this design not only provides superior solution to the storage and retrieval of digital voice data but also provides a flexible cross-platform solution for all digital or analog cellular phones standards.

Tradeoff Between Insertion Loss and Performance of SAW Filters for Portable Phones

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Abstract

As wireless receiver designs continue to evolve, the required insertion loss of the IF filtering components continue to be reduced. This reduction is due to the dynamic range and noise figure requirements of the ASICs that are becoming more common in receiver designs. In addition, the lower losses in the IF chain reduce the DC power requirements of the portable phone.

For a given filter requirement, as the insertion loss of the filter is reduced, various parameters of the SAW filter are affected. Among these are VSWR, rejection, passband ripple, and rms phase error. Most of these parameters are dependent on the matching network. The overall performance of the filter in production will therefore depend on the manufacturing tolerances that the phone manufacturer can achieve.

Presented are three different PCS filter designs at 210.38 MHz, each optimized for a different nominal insertion loss. Comparisons of the filters' performances and sensitivities to matching element variations will be presented. Also presented will be various IF filters designed specifically for high volume production.

Introduction

The communication market is booming. One particularly strong market segment is wireless communications, driven by a technical advances in electronics. One form of wireless, the cellular phone, is a consumer product requiring high technology components in high volume, with high quality and a low price.

The Surface Acoustic Wave filters are used for both RF and IF filtering inside mobile phones. These filters are key components because they have a direct impact on the channel filtering which translates to communication quality. Recent advances in SAW filter design has led to the ability to build low insertion loss filters.

The drawback of the lower insertion loss is the higher matching element sensitivity and increased sensitivity to the manufacturing variations of the SAW filter. These effects, if not thoroughly considered in the system design, can result in low product yields.

This paper will explain the properties of the SPUDT (Single Phase UniDirectional Transducter), used in the majority of low loss SAW filters now on the market. Then a transmission line model for the SPUDT based SAW filter will be used to derive relationships between insertion loss, mismatch loss, and VSWR. Next, the effects of matching element variations and SAW filter capacitance variations on the passband ripple and insertion loss will be presented.

Three IF PCS-CDMA filters designed for different nominal insertion losses are presented and performances are compared with the results of the model. The lowest loss filter is shown to be too sensitive to matching and manufacturing variations to be a practical filter. Matching element sensitivities will be shown for the optimum filter, along with filter guaranteed performances in manufacturing. Finally, conclusions will be presented.

I. The SPUDT structure

The Single Phase Unidirectional Transducer (SPUDT) is one of the most interesting techniques for reducing the insertion loss : it only requires a single level fabrication, uses simple tuning and can achieve very low amplitude and phase / group delay ripple by canceling the triple transit. It can take on many structures. A general theory has been presented by J.M. Hodé [1] with a global approach of the relations

between the transmission and the reflection the transducer must have to achieve maximum directivity.

A transmission line model of a filter made with two SPUDTs has been introduced by P. Dufilié [1]. This model (Fig. 2) is accurate enough to describe the behavior of the filter near the center frequency.

A DART (Distributed Acoustic Reflection Transducer) is an important type of SPUDT structure. The term DART can be used to represent all structures which use sets of metal strips for the transduction without acoustic reflection and sets of strips for only acoustic reflection. The general relation of the phase between transduction and reflection for the SPUDT is a localized relation in the DART.

The figure below (Fig. 1) illustrates the local directivity of a DART. Acoustic waves are emitted in both directions from the transduction center, the backward wave (to the left) is reflected at the reflection center. At a specific distance between transduction and reflection centers the reflected wave is in phase with the forward wave (to the right) making this cell directional in the forward direction.

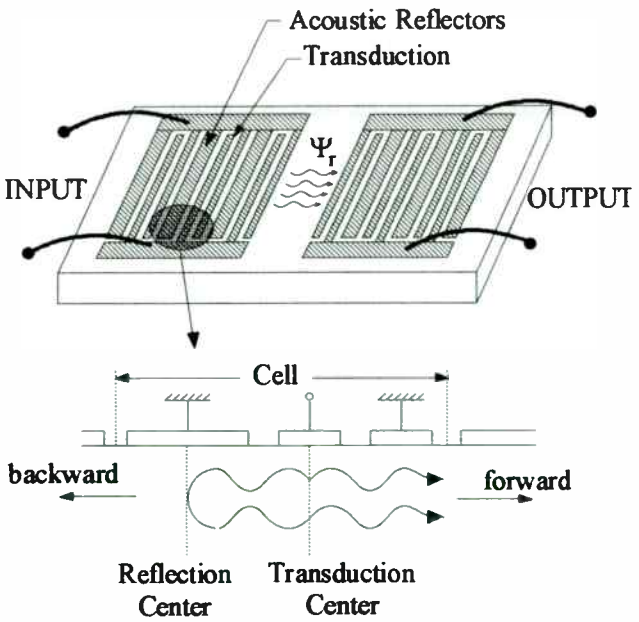

Fig. 1 - SPUDT filter

For low triple transit, the total reflection at the forward acoustic port must equal zero, which means that the short-circuit reflection must exactly cancel the electrical regeneration. This can be achieved by an optimal tuning.

The load conductivity can be written :

from [2] : $G_L = \frac{k^2+1}{k^2-1}G$ where k=1 for the conventional bidirectional transducer and k=∞ for the ideal unidirectional transducer.

The tranducer directivity is the normalized difference of power radiated in the two directions. The directivity can be seen as the acoustic short-circuit reflection.

$$d = \frac{k^2-1}{k^2+1} \qquad (1)$$

from [1] : $G_L = \frac{G}{d}$ where d is the directivity of the transducer. Both results are identical.

The presence of acoustic reflection internal to the transducer makes the design of SPUDT based filters more complex than the design of conventional bidirectional filters ([3]). A simultaneous reflection and transduction nonlinear algorithm was developed in order to optimize all the filter parameters ([4],[5]). This optimization procedure converges to transducer designs with resonant cavities inside, increasing the impulse responses of the SPUDTs and resulting in a better filtering efficiency for the transducer. Comparing different SPUDTs with the same characteristics, these Resonant SPUDTs ([6]) have a smaller size, resulting in a smaller package and smaller price.

II. Insertion Loss

From the transmission line model presented by P. Dufilie [1], it is possible to deduce the insertion loss of the filter. Assuming that a SPUDT is a non-dissipative system (i.e. neglecting ohmic losses, propagation and diffraction losses) its losses are only related to electrical mismatch and acoustic directivity.

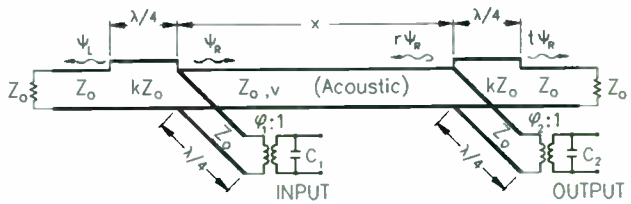

Fig. 2 - Transmission line model for practical low loss filter

The transmission at the electrical port is : $t_e = \sqrt{1-|r_e|^2}$ where $|r_e|$ is the electrical reflection coefficient of the tuned transducer. At the center frequency,

assuming the static capacitance of the transducer is perfectly compensated by the inductor (that means $LC\omega_0^2 = 1$) :

$$|r_e| = \left|\frac{G - G_0}{G + G_0}\right| = \frac{1}{k^2} \qquad (2)$$

so $$t_e = \sqrt{1 - \frac{1}{k^4}} \qquad (3)$$

The practical SPUDT is not perfectly unidirectional. The electrical power is converted into a forward wave and a backward wave which is lost. The transmitted power to forward direction can be written :

$$t_d^2 = \frac{k^2}{1 + k^2} \qquad (4)$$

For the ideal unidirectional transducer, $k=\infty$, all the power is transmitted, $t_d=1$ and for the conventional bidirectional transducer, $k=1$, only half the power is transmitted.

For port 1 the transmission is

$$t = t_e \cdot t_d = \sqrt{1 - \frac{1}{k^2}} \qquad (5)$$

Both transducer don't necessarily have the same directivity. The total transmission of the filter is

$$|S_{12}| = \sqrt{1 - \frac{1}{k_1^2}}\sqrt{1 - \frac{1}{k_2^2}} \qquad (6)$$

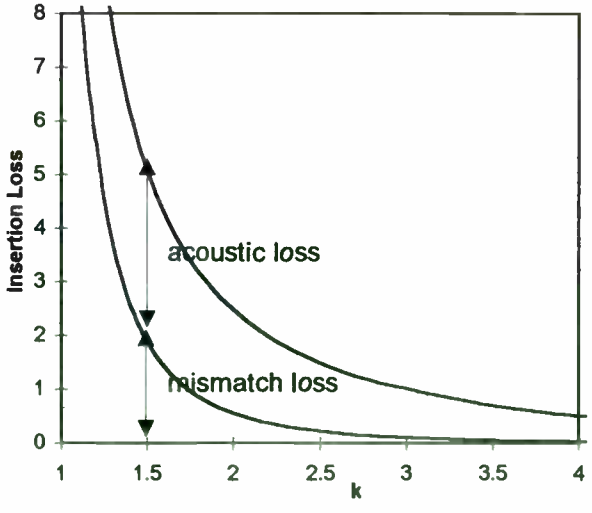

Fig. 3 - Total insertion loss of the filter.

As the directivity and parameter k increase, both types of loss are decreasing : acoustic and mismatch loss. The directivity is directly related to the acoustic reflection coefficient of the tranducer. It's value is then a function of the substate, the metal thickness and relative bandwidth of the filter.

III. Insertion Loss outcome

The TMX PCS-CDMA filter FBF033 will be used to illustrate this outcome. This filter is the object of a more detailed presentation in the last chapter. In this section, simulation results on the insertion loss will be presented.

Four insertion loss mechanisms can identified :

A. electrical mismatch and directivity loss

A detailed filter simulation gives a center frequency insertion loss of 5.35 dB. The ratio of the input filter conductivity to the source conductivity (and output to load) is approximatly $\frac{G}{G_0} = 0.4$. This corresponds to a parameter k=1.53. On the plot of the insertion loss versus k (Fig. 3), we determine an insertion loss of 5 dB. It can be noted that the filter under this condition is not perfectly impedance matched. All the resistive losses, inductor losses and capacitives parasitics are taken into account in the design of the filter so that the filter is optimaly matched on the specified source and load. In this simulation, all the resistive parasitics have been removed, so the filter is no longer perfectly matched. This can explain the discrepency in the results.

B. Internal resistive loss

In this simulation, electrode, bus bar and wirebounding resistance and inductance as well as package and PC board capacitance have been added. The center frequency insertion loss increases by 0.6 dB.

C. Diffraction loss

Diffraction analysis has been added to this simulation. The loss due to the diffraction is 1 dB.

D. Resistive loss in the inductor

If we take into account the resistive parasitic of the matching inductor, it adds 1.8 dB to the center frequency insertion loss.

The total simulated center frequency insertion loss is then 8.24 dB and the measured insertion loss is between 8.21 and 8.3 dB on 5 filters.

IV. VSWR

The VSWR can easily be deduced from the electrical reflection coefficient given in equation 2.

$$VSWR = \frac{k^2+1}{k^2-1} : 1 \qquad (7)$$

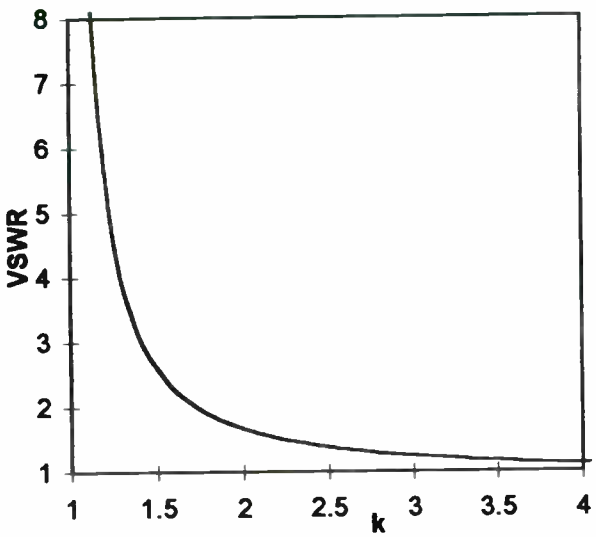

Fig. 4 - VSWR of one transducer

Decreasing the nominal insertion loss has also the benefit of reducing the impedance mismatch between the input (output) and source (load), resulting in a good VSWR.

V. Insertion Loss sensitivity to a mismatch

In this chapter, we will see the effect of variation of the matching inductance.

If we assume that the transducer conductance is constant over the bandwidth, then the electrical reflection coefficient can be written :

$$r_e = \frac{(G-G_L)+j\left(C\omega-\frac{1}{L\omega}\right)}{(G+G_L)+j\left(C\omega-\frac{1}{L\omega}\right)} \qquad (8)$$

The transmission is then :

$$t_e = \frac{2\sqrt{\frac{G}{G_L}}}{\sqrt{\left(\frac{G}{G_L}+1\right)^2+Q_L^2\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)^2}} \qquad (9)$$

where

$$LC\omega_0^2 = 1 \qquad (10)$$

$$Q_L = \frac{C\omega_0}{G_L} = \frac{R_L}{L\omega_0} \qquad (11)$$

ω_0 is not the center frequency of the filter (ω_c). They correspond only when the filter is perfectly matched.

Q_L is the Q of the matching network.

In the bandwidth it is very accurate to assume that $\Delta\omega = \omega - \omega_0 << \omega_0$. We can write :

$$t_e = \frac{2\sqrt{\frac{G}{G_L}}}{\frac{G}{G_L}+1}\left(1-\frac{2Q_L^2}{\left(\frac{G}{G_L}+1\right)^2}\left(\frac{\Delta\omega}{\omega_0}\right)^2\right) \qquad (12)$$

Then, the insertion loss in dB is the sum of two terms. The first one does not vary with the mismatch, we have seen this term in the preceding chapter. The second term can be written :

$$t_{dB} = \frac{40}{\ln(10)}\frac{Q_L^2}{\left(\frac{G}{G_L}+1\right)^2}\left(\frac{\Delta\omega}{\omega_0}\right)^2 \qquad (13)$$

This term simply adds a parabola shape to the insertion loss. When the inductor value varies, the center frequency of this parabola moves :

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad (14)$$

This small inductance variation is called δ.

$$L = L_N(1+\delta) \qquad (15)$$

where L_N is the nominal inductance value which gives the perfect matching.

so $$\omega_0 = \omega_C\left(1-\frac{\delta}{2}\right) \qquad (16)$$

where ω_C is the center frequency of the filter.

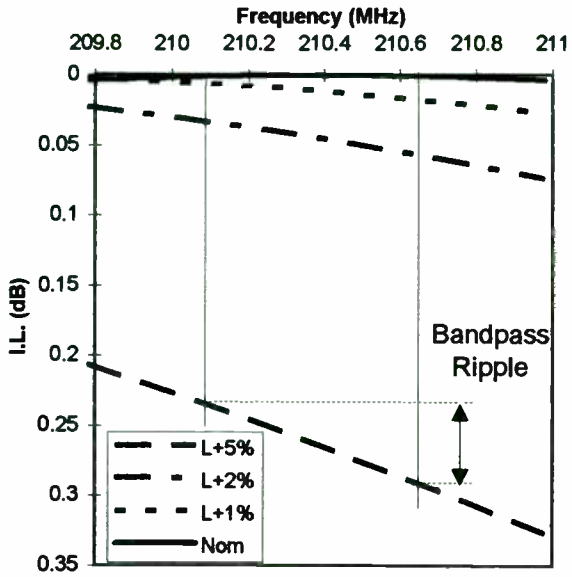

Fig. 5 - Insertion induced by an inductance variation

Parameters used for the plot :

- $Q_L = 10$
- $\frac{G}{G_L} = 0.4$

A variation of the inductance has two main effects :

- increase of the center frequency insertion loss
- generation of a tilt in the passband. This tilt is the main reason for the increase of the passband ripple.

As it can be seen on the figure, if the inductors have the same sign variation from the nominal, the bandwidth tilt will be maximum. If the variations are of opposite sign, the tilts are canceling but it still remains an increase of the insertion loss. This will be seen in the last chaper on a practical exemple.

Q_L is the main parameter of these two effects. We will see in the following chapter that Q_L is increasing when the nominal insertion loss is decreasing. The filter becomes more sensitive to a mismatch. For this reason the maximum insertion is a much a more accurate specification than the nominal insertion loss.

VI. Static capacitance

In a first approximation, we can assume that the static capacitance of the transducer is proportional to the capacitance of a single electrode in an array of grounded electrodes.

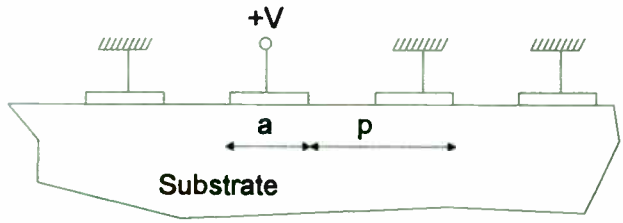

Fig. 6 : Illustration of the strucutre used for the static capacitance calculation.

The result of the simulation with different linewidths for a constant period is plotted below

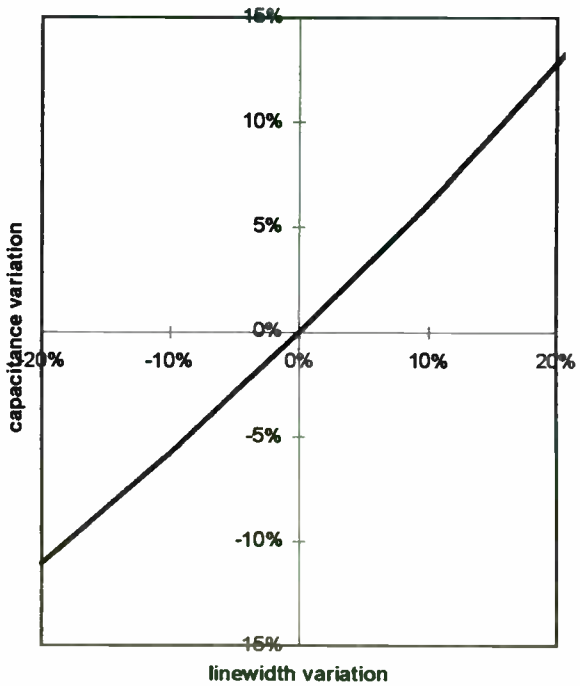

Fig. 7 - capacitance variation with the linewidth.

An error on the linewidth generates a variation of the static capacitance of the filter. This variation of the capacitance operates like a variation of the matching inductor generating ripple and insertion loss discrepancy.

The linewidth error does not depend on the linewidth. That means the error is expressed in µm and not in %. So when the center frequency of the filter is inscreasing (the linewidth is decreasing), the capacitance variation becomes larger.

VII. The matching Q

The matching Q is the ratio of the load impedance to the load susceptance. This value is related the material, the relative bandwidth and the nominal insertion loss.

On the figure below is plotted the matching Q versus insertion loss for the three PCS-CDMA filters. All three have the same center frequency, bandwidth and are manufactured on the same material but are designed to have a different nominal insertion loss.

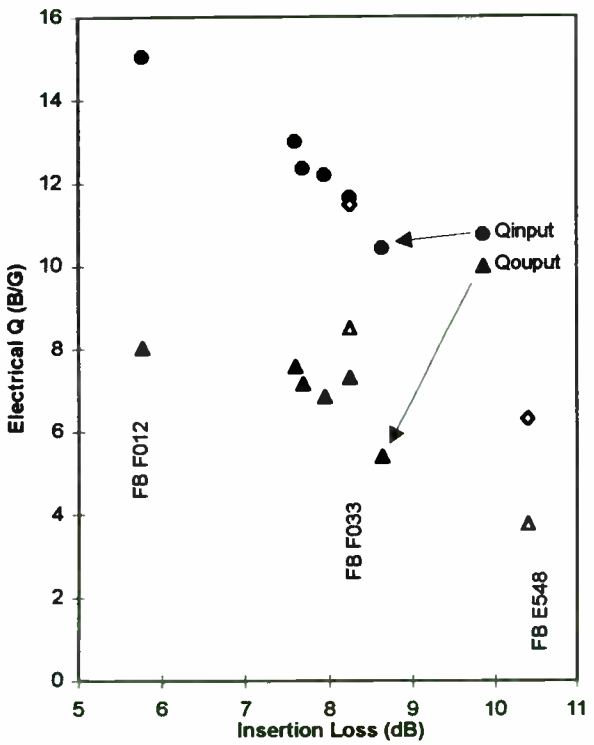

Fig. 8 : Evolution of the electrical Q of the matching for different TMX PCS-CDMA filters. The black points are simulations and the white one are mesurements.

This series of filter has different source and load impedance and different Q. As the sensitivity evolves with Q^2 the higher value will be the most important part of the performance variation.

The lowest loss filter : FB F012 will be 4 times more sensitive to the inductor and the linewidth variation than the FB E548. It is in fact too sensitive to be a practical filter today.

The filter we will present next is an optimum tradeoff between insertion loss and sensitivity to inductor variation and manufacturing tolerances.

VIII. PCS-CDMA IF filter : TMX FBF033

The interests of using the SPUDT structure for the PCS and CDMA architecture are : the very small phase and amplitude ripples, the low losses, but above all, no triple transit echo in the time domain response.

For this filter, the typical performances at room temperature are the following :

Center frequency	210.38 MHz
Insertion Loss at F0	8.25 dB
Passband at 5 dB	1.48 MHz
Rejection at 31 dB	2.30 MHz
Amplitude Ripple within $f_0 \pm 0.3$ MHz	0.3 dB
Phase variations within $f_0 \pm 1.26$ MHz	1.3 °RMS

The filter can either be driven balanced or single ended or a combination of both. It is mounted in a 13.3 x 6.5 mm^2 ceramic SMT package.

The filter is tuned with two parallel inductors (Fig. 9). The values of the inductors depend on the structure of the PC board and its associated stray capacitance. They also depend on the way the filter is driven. The filter requires ±2% inductors with a high Q (Q>55) to guaranteee good insertion loss and amplitude ripple.

All the performances of the TMX IF filters are guaranteed within the total temperature range and within the inductor tolerances specified for the filter.

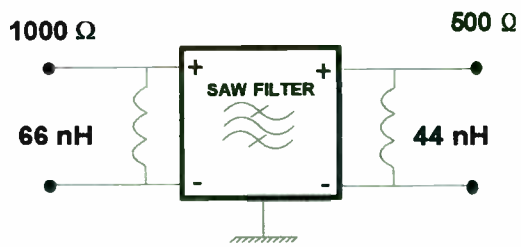

Fig. 9 - Schematic of the tuning.

A typical S21 and phase response of this filter are shown on the Fig. 10. The corresponding time domain response is shown on Fig. 11.

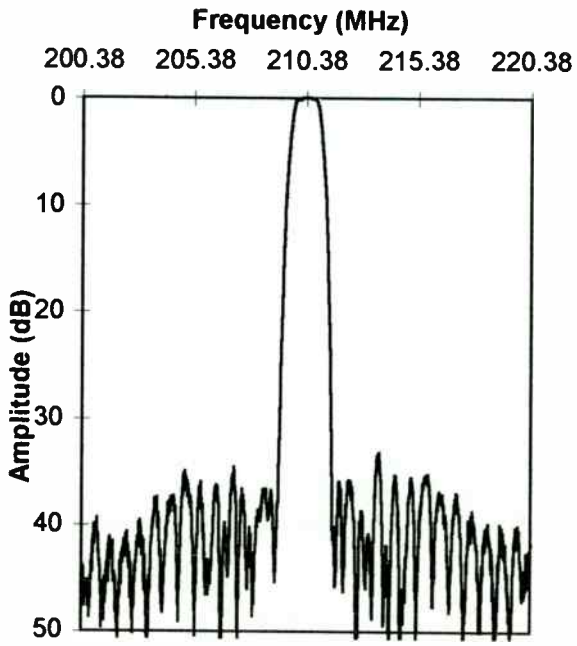

Fig. 10 - Typical response

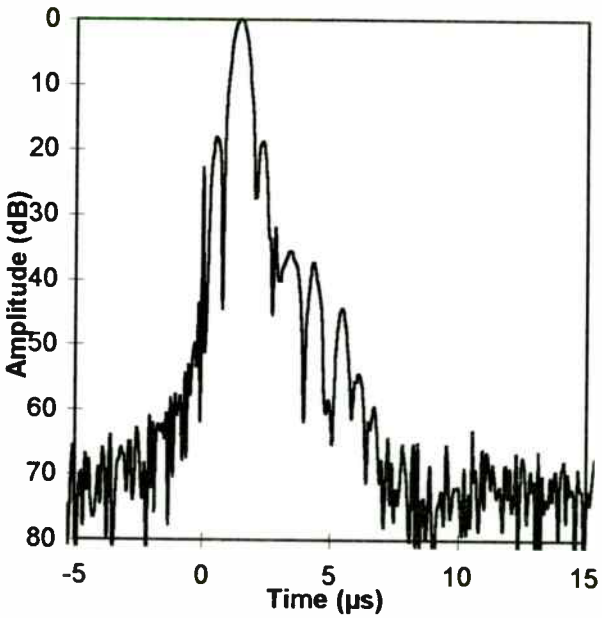

Fig. 11 - Typical time domain response

The variation of the ripple due to the inductors is shown on the Fig. 12. For variations which are a little more than ±2%, the ripple remains very good. We must add the static capacitance variation due to the linewidth variation to obtain the maximum ripple in the passband.

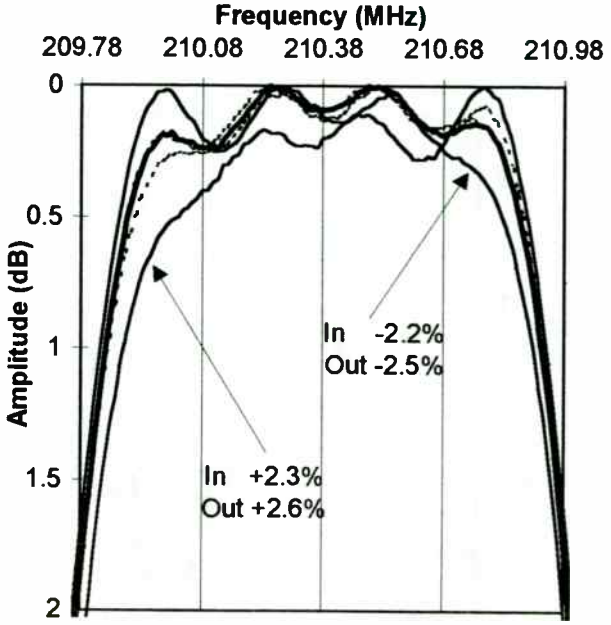

Fig. 12 - S21 referenced to minimum insertion loss of the same filter with different values of inductors.

The variation of the insertion loss is shown on the next figure (Fig. 12).

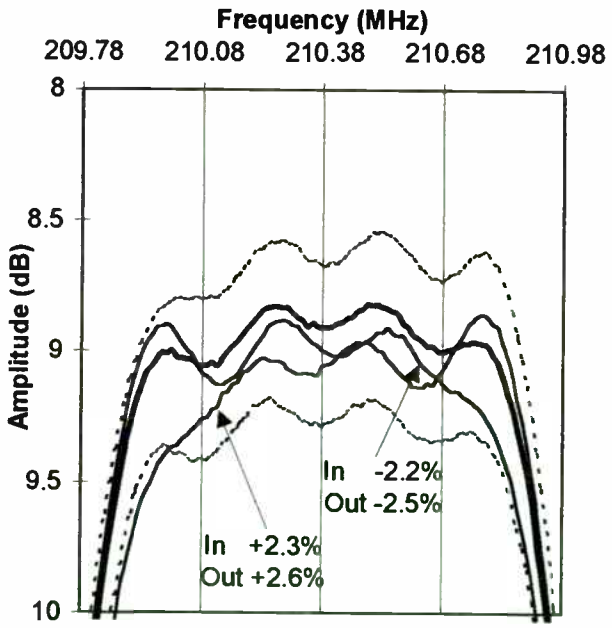

Fig. 13 - S21 of the same filter with different values of inductors.

On the next figure, the phase of the filter has been plotted in the same condition of inductor variation.

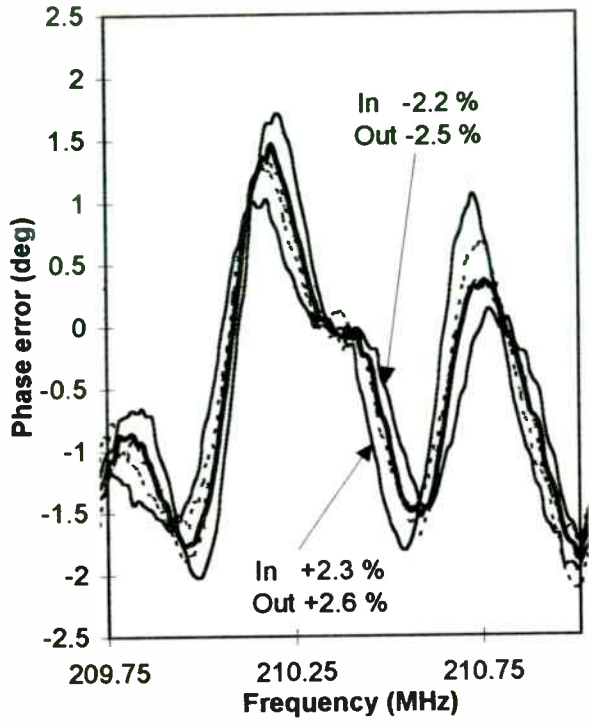

Fig. 14 - Phase of the same filter with different values of inductors.

The table below summerize the RMS phase error for different inductor values. As it can be seen on the figure, the maximum error is for inductor variations of the same sign for both input and ouput. These values remain very good.

Inductor values	RMS Phase Error
nominal	0.891
In -2.2 % Out -2.5 %	0.928
In -2.2 % Out +2.6 %	0.887
In +2.3 % Out -2.5 %	0.896
In +2.3 % Out +2.6 %	0.938

Table 1 : Variation of the RMS phase error versus the inductors values.

IX. Conclusion

We first explained the properties of the SPUDT structureand the benefits for the IF filters for PCS and CDMA handset. A simple explanation of the filters sensitivity to matching inductors and linewidth variation has been presented based on the SPUDT transmission line model. It has also been shown that the sensitivity increases when the insertion loss are decreases. The design of a SAW filter is then a tradeoff between insertion loss and performance. We also presented data on an optimized IF SAW filter for PCS-CDMA applications at 210.38 MHz.

References

[1] J.M. Hodé, J. Desbois, P. Dufilie, M. Solal, P. Ventura, "SPUDT-Based Filters : Design and Optimization", *IEEE Ultrasonics Symposium Proceedings,* 1995, pp. 39-50.

[2] P. Dufilie, E. Psaïla, L. Chommeloux, F. Roux, "Low Loss SAW Filters for Mobile Communication", *Wireless Symposium Proceedings,* 1996, pp. 47-54.

[3] C. S. Hartmann, B.P. Abbott, "Overview of Design Challenges for Single Phase Unidirectional Saw Filters", *IEEE Ultrasonics Symposium Proceedings,* 1989, pp. 79-89.

[4] P. Ventura, M. Solal, P. Dufilié, J. Desbois, M. Doisy, J.M. Hodé, "Synthesis of SPUDT filters with simultaneous reflection and transduction optimization", *IEEE Ultrasonics Symposium Proceedings,* 1992, pp. 71-75.

[5] P. Ventura, M. Solal, P. Dufilié, S. Chamaly, "A Global Optimization Procedure for SPUDT filters", *IEEE Ultrasonics Symposium Proceedings,* 1993, pp. 5-8.

[6] P. Ventura, M. Solal, P. Dufilié, J.M. Hodé, F. Roux, "A New Concept in SPUDT Design : the RSPUDT (Resonnant SPUDT)", *IEEE Ultrasonics Symposium Proceedings,* 1994, pp. 1-6.

FIRST: DoD's Range Radio Data Link Standard. Synergy with Commercial Wireless Applications*

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SUMMARY

To develop a modern, cost-efficient Department of Defense (DoD) common data link standard for a Family of Interoperable Range System Transceivers (FIRST) which could serve Test and Evaluation (T&E) Training, within the US Navy, Air Force and Army, a new standard development task has been undertaken. Study of commercially available wireless standards and equipment led to the conclusion that a strong synergism between commercial and military resources could lead to enhanced performance, increased capacity and range, reduced latency and system cost for DoD's ranges of the FIRST standardized radio program. DoD's studies [1,2] indicate that more than $250 million savings will be achieved by the FIRST standard in the military field. Use of "dual mode" military and commercial technology/synergism could lead to the first universal bit rate, global joint commercial/military standard.

It is the intent of DoD's Common Data Link Technical Working Group (TWG) to develop FIRST, a comprehensive wireless/radio standard that will not only serve the needs of the military range community, but also those of many similar applications required in the military and in emerging commercial wireless digital and personal communication systems. Current DoD systems, such as RAJPO DLS-1, NGTCS, JTCTS, MAIS, RDMS upgrade, operate in the data range of 10kb/s to 2Mb/s and chip/bit rates to 30Mchip/sec. Based on current trends we foresee, within the next 15 years, potential requirements for increased data rates from the low 8kb/s range to 2Mb/s and even in the 30Mb/s (30Mchip/s) range. Some of these systems operate with relatively low power (in the m-Watt to 1Watt range), while others require almost 100Watt of transmitted RF power. Most of these systems deploy modulation techniques which are suitable for Non Linearly Amplified (NLA) i.e., saturated RF power amplification in the 100MHz to multiple GHz range.

The TWG of FIRST, in consultations with industrial organizations, has been developing a re-configurable, programmable, multi-RF-band-based strategy for a variety of bit rate, chip rate and RF band multiple-purpose applications. By means of a "mix-and-match" approach, readily available and most efficient technology components from world leading wireless digital communications standards such as GSM, DECT, CDMA and TDMA and from emerging not-yet-standardized applications and products have been considered. To meet stringent RF spectral/power efficiency (of more than 1.2 b/s/Hz-for 99% in band power), small-size, reduced-cost and robust BER performance (maximal range with lowest BER=Pe) requirements the FIRST-TWG-proposed FQPSK or compatible/interoperable enhanced efficiency OQPSK-GMSK quadrature modem/radio architectures. These interoperable systems are suitable for NLA operation. Among the robust BER performance modem/radio NLA technologies FQPSK offers the highest combined power and spectral efficiency and meets the specifications of the FIRST standard. In this paper the most important performance criteria/specifications of the Physical Layer (PHY) modem/radio are highlighted.

* Material in this publication is based on FIRST Program Office, DoD Common Data Link Technical Working Group (TWG) briefings/reports and on other reports and publications of the authors, listed in the references.

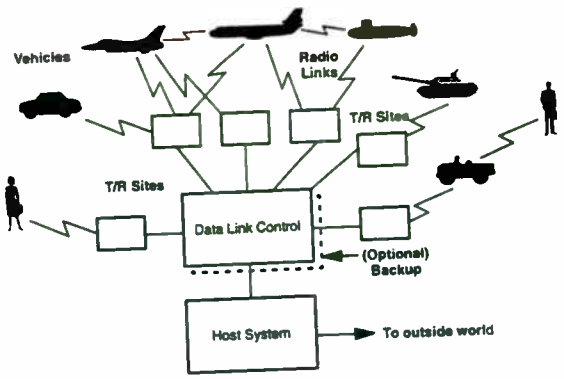

Fig.1 Architecture of a typical FIRST (Family of Interoperable Radio System Transceivers) Installation - DoD Radio Common Data Link

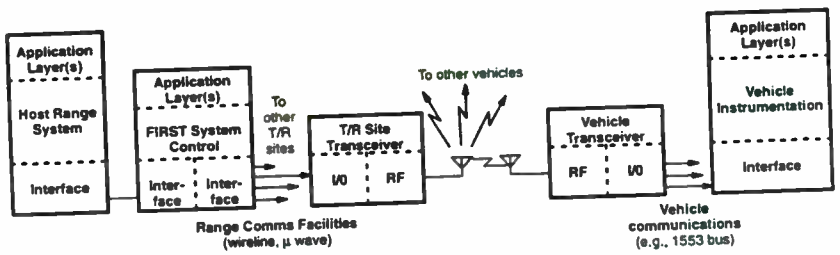

Fig.2 Signal Path Illustration-connection of host system at central facility to the instrumentation aboard a vehicle (without relaying)

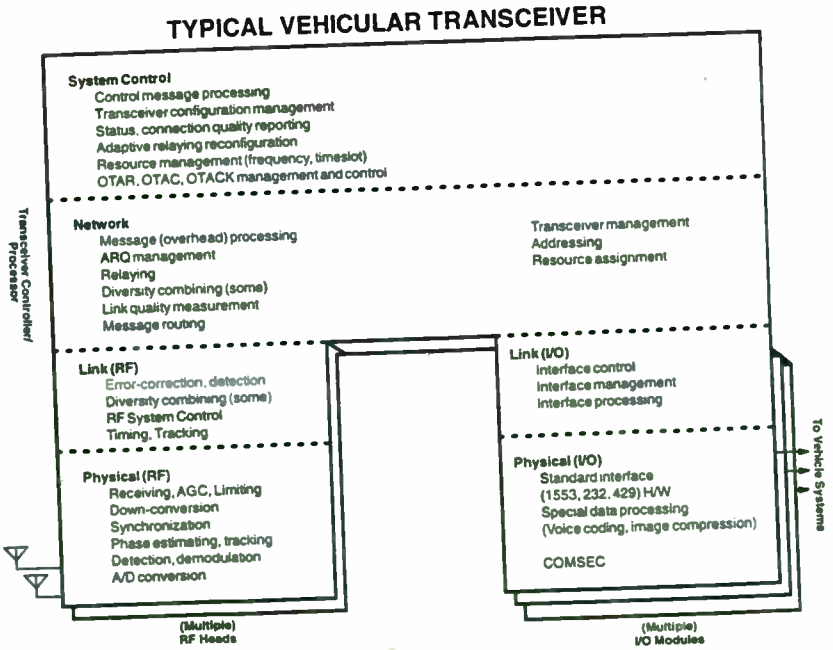

Fig.3 Functions performed by a typical FIRST Vehicle Transceiver , the one on the right in Fig.2

1. INTRODUCTION

RF data links are used at over 50 military test and training ranges to relay position and status data from vehicle instrumentation to ground control and recording facilities and to exercise control over vehicles and other assets such as targets. Links in use today were for the most part developed on an "ad hoc" basis as incidental parts of larger applications and are largely incompatible with one another. They operate in many different spectral regions, with different modulation, coding and signaling formats. Until recently use of so many different "point solutions" was acceptable since range operations and functions were traditionally autonomous, involving minimal coordination. Plans to integrate future test and training activities more fully (and the successful use of open system standards in the commercial community) have led to the realization that this situation should be changed. An effort is now underway, funded by the Department of Defense (DoD) Central Test and Evaluation Investment Program, to develop a general-purpose data link that can be tailored to serve in a wide variety of common test and training applications. Known as project FIRST (Family of Interoperable Radio or Range System Transceivers), that effort is focusing on the development of a common air interface standard.

The standard will cover a variety of transceiver types, from those carried by individual troops to report their position and status to those used in high-performance aircraft, with appropriate differences in transmission rate and RF output power. It will promote the concept of tailorability through software (and modular hardware) changes so that transceivers can be adapted to provide the performance demanded by the particular application. For example the transceiver developed for use on high-performance aircraft will be programmable to provide maximum net capacity (throughput) in some applications (e.g., observation and recording of air combat training exercises) or minimum latency and high link reliability in others (e.g., drone control). Where throughput limitations permit, it will be possible to accommodate multiple applications and transceiver types simultaneously on the same net. A variety of vehicular interfaces will be provided for connection to different types of vehicle data collection systems and to accommodate different types of information (e.g., packetized telemetry, speech, imagery).

Development of the standard is a collaborative effort involving all military services and the entire military test and training range community. All major current development programs that involve range data links are also involved. Although it has just recently begun, the activity will adopt the approach used by the commercial wireless communications community in the development of recent wireless system standards. This is a major change from the way range data link business has been done in the past, and an example of how the military hopes to benefit in the future from adopting commercial technologies and methodologies. In return we hope to develop a comprehensive standard that will not only serve the needs of the military range community but also those of may similar efforts in the commercial community. In Fig. 1 to Fig. 3 the architecture of a typical FIRST standardized installation, signal path and performed functions are depicted. The predicted cost savings of the DoD in the more-than-$250 million range are documented in [1,2] and other FIRST program office reports. In this publication we present some of the most essential highlights of the technology selection process and specifications of the PHY (Physical Layer) of the FIRST draft standard. This includes modulation/radio transceiver architectures and performance requirement highlights [1-21].

2. MODULATION/RADIO TRANSCEIVER TECHNICAL CONSIDERATIONS/HIGHLIGHTS

We surveyed a large class of commercially available digital radio/microwave modulation technologies and found that compatible and interoperable modulated NLA radio architectures of FQPSK, enhanced efficiency GMSK and OQPSK [10-21] could meet the transmit RF spectrum and power efficiency and wide bit range rate variation requirements of FIRST. To meet the simultaneous NLA transmit RF power efficiency and robust BER = $f(E_b/N_o)$ requirement, for a variety of mobile applications, which may be Rayleigh-faded (Rician-faded in case of some satellite applications) and operated over NLA radio in an interference-controlled environment, we concluded that quadrature FQPSK and enhanced performance GMSK and OQPSK coherent quadrature demodulation structures have a considerably better performance than their non-coherent counterparts. For normalized NLA radio spectral efficiencies in terms of b/s/Hz, for minimum 1.2b/s/Hz RF spectral efficiency requirement the link margin advantage of quadrature modems is in the 7dB to15dB range. For large delay spread (frequency selective fading) environments, quadrature radio demodulators have been equipped with efficient adaptive equalizers, while effective delay spread countermeasures of non-coherent systems are not commercially available.

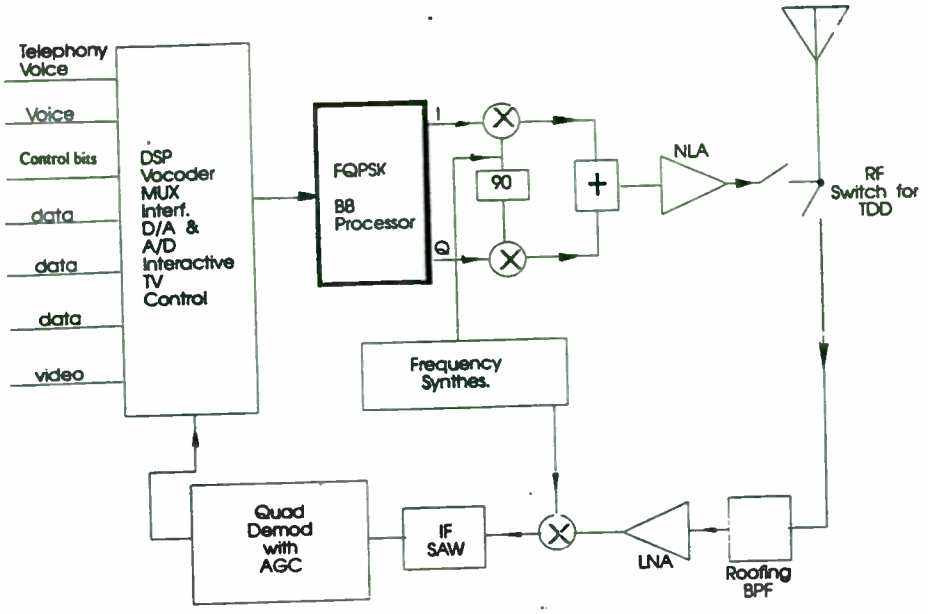

Fig.4 Transceiver Block Diagram of a typical FIRST Quadrature Modem/Radio suitable for Nonlinearly Amplified(NLA) RF power and spectrally efficient mode and robust BER operation. . The illustrated FQPSK[references 3;4; 10-16 and 21]] architecture enables backward and forward compatible interoperable operation with current DoD quadrature modulated OQPSK and MSK systems, with major commercially standardized GMSK based systems as well as future new system developments.

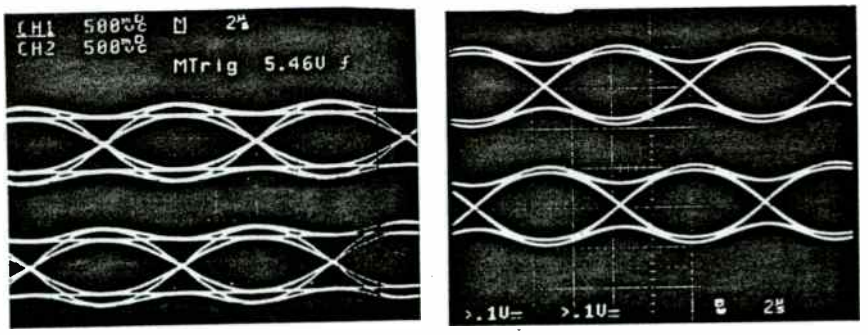

Fig 5. Widely open demodulated EYE diagram measurement results of commercially available FQPSK and GMSK [10-19] products . These photographs are an indication of the robust BER performance of these systems

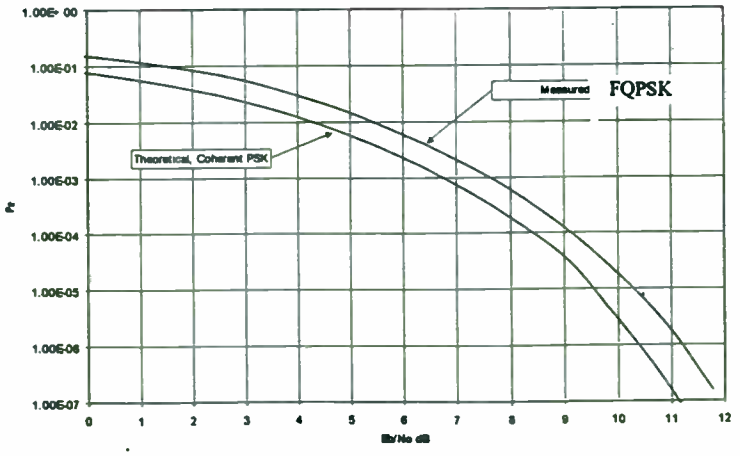

Fig 6. BER = f (Eb/No) results of an FQPSK modem/radio system, operated at 34Mb/s equivalent 17Mchip/sec rate , measured at the FIRST program office ,US Navy, Point Mugu, CA. Practically the same results were measured at the University of California, Davis (UC Davis) and at Lockheed Martin, Salt Lake City. The "EB200KF: FQPSK-GMSK Universal Modem/Radio " Lockheed Martin manufactured product, manufactured under license of Feher et al. patents-Ref.[10], property of IOTA, Inc.-IOCOMM [16 and 18] , illustrates the very robust performance of nonlinearly amplified FQPSK, to be within 1dB of ideal coherent linearly amplified QPSK

	Systems/ Standards	Order of Magnitude of Estimated Number of Subscribers by Year 2000 in Millions (M)	RF Bands (approximate)	RF Bandwidth (-10 to -30dB)	Bit Rate [kb/s]	Spectral Efficiency in [b/s/Hz] for -20dBr	Uncoded BER=10^{-5} E_b/N_o [dB] Required in Stationary AWGN	Modulation
1	CT-2	20M+	930MHz	100kHz	72kb/s	0.7b/s/Hz		GFSK
2	CDPD	1M+	896MHz	30kHz	19.2kb/s	0.7b/s/Hz	18-22dB	GMSK (BT_b=0.5) approx GFSK
3	LMR (non-standard)	2M++	150MHz to 900MHz	5kHz to 50kHz	9.6-64kb/s	1.5b/s/Hz	10-13dB	FQPSK or other
4	GSM	80M++	900MHz	200kHz	270.833 kb/s	1.3b/s/Hz -10dBr	10-13dB	GMSK BT_b=0.3
5	PCS-1900	25M+	1.9GHz	200kHz	270.833 kb/s	1.2b/s/Hz -10dBr	10-13dB	GMSK BT_b=0.3
6	DCS-1800	30M++	1.8GHz	200kHz	270.833 kb/s	1.3b/s/Hz -10dBr	10-13dB	GMSK BT_b=0.3
7	RAM-Mobitex	2M+	935MHz	12.5kHz	8kb/s	0.65b/s/Hz	?	GMSK BTb=0.3
8	IEEE 802.11-FH	1M	2.4GHz and 5.7GHz	1MHz	1Mb/s	1b/s/Hz (-20dBr)	22-28dB	GFSK BT_b=0.5
9	DECT	50M++	1.85GHz	1.728 MHz	1,152 Mb/s	0.6b/s/Hz	20-25dB	GFSK BT_b=0.5
10	HIPERLAN	3M+?	5.7GHz	10MHz to 50MHz	10-30 Mb/s	0.7b/s/Hz 1.3b/s/Hz	10-13dB 10-13dB	GMSK FQPSK
11	Non-standard WLL; FLL; WLAN; SATCOM	30M++	2.4GHz 5.7GHz 24GHz other RF	1MHz to 100MHz ++	300kb/s-10Mb/s ++	1.0b/s/Hz 1.3b/s/Hz 1.5b.s.Hz	20-25dB 10-13dB 10-15dB	GFSK GMSK FQPSK OQPSK SQAM QPSK-C
12	Wireless - Cable	10M+	2.2GHz + other	5MHz+	10Mb/s	1.3b/s/Hz	10-15dB	FQPSK or equivalent?

Table 1 Commercial major US and International standardized

FDMA, TDMA and TDMA -FH-SS (CDMA) and non-standardized systems use GMSK, GFSK and equivalent enhanced efficiency compatible OQPSK,FQPSK QPSK-C, SQAM and other modems. For RF-power efficiency Nonlinearly Amplified (NLA) low cost/reduced size/reduced battery power is desired. All entries are approximate, estimated values.

Table 2 DoD Common Range Data Link Parameters[1-9]

Parameter	Data Link System							
	CMTC-IS	DLS	JRTC-IS	JTCTS	MAIS	NGTCS	NTC-IS	PRIME
Frequency Range (MHz)	30-88	1350-1390+	225-250	1710-1850	512-806	1350-1390	824-894	350-450
Multiple Access	FDMA/TDMA	FDMA/TDMA	FDMA/TDMA	TDMA	FDMA/TDMA	FDMA/TDMA	FDMA/Async. TDMA	FDMA/Polling/ TDMA
# of RF Channels	42 (5KHz)	6 (3MHzx2)	42 (25KHz)	2 (22.5MHz)	6 (150KHz)	~10 (1.2 MHz)	27-78 (30KHz)	8 (25KHz)
Slots/Sec/RF Ch	Variable	330	Variable	P=280T+10R, S=30B+60A+10H	<250	330	~10 (Variable)	Variable (30 typ.)
# of Users	2000/4000	>3000	2000/4000	138	1830	48	2000	300
User Assignment Technique	Fixed, Reassignable	Fixed, Reassignable	Fixed, Reassignable	Fixed, Reassignable	Fixed, Reassignable	Fixed Reassignable	Random	Polling/ Assignable
Message Size (Bits)	Variable (40-2040)	736	Variable (40-2040)	Variable (496-26,880)	Variable 40-2000	1024	Variable 40-2040 (typ. 500)	Variable (typ. 800)
Throughput (kbps)	<8	242	<8	138.9 + Relay	62	337	2	<8
Modulation	Non-Coherent FM	MSK	Non-Coherent FM	OQPSK	Non-Coherent FM	Square-Root Raised Cosine QPSK	Non-Coherent FM	Non-Coherent FM
Peak Info Transfer Rate (kbps)	9.6	628	9.6	351/703/1406	6.25	846	10	9.6
Error Correction Technique	None	Conv/Viterbi	None	R-S (78,62) + R-S (100,84)	None	R-S + Viterbi	BCH/Repeat	None
Error Detection	Checksum	CRC-24	Checksum	FEC	CRC-16	CRC-24	CRC-16	Checksum
COMSEC	None	REM/CEC	None	AMODSM	REM/CEC	REM/CEC	None	None
Range per Hop (nmi)	20	150	10	150	20	200 (G-A) 100 (A-A)	18	3
Relaying	No	Any User, Automatically	No	Dedicated by Platform or Any User (Automatically)	No	Any User Automatically	Automatic If required	No
Timing	GPS or Internal	GPS or Internal	GPS or Internal	GPS or Internal	GPS or internal	GPS	GPS or Internal	GPS

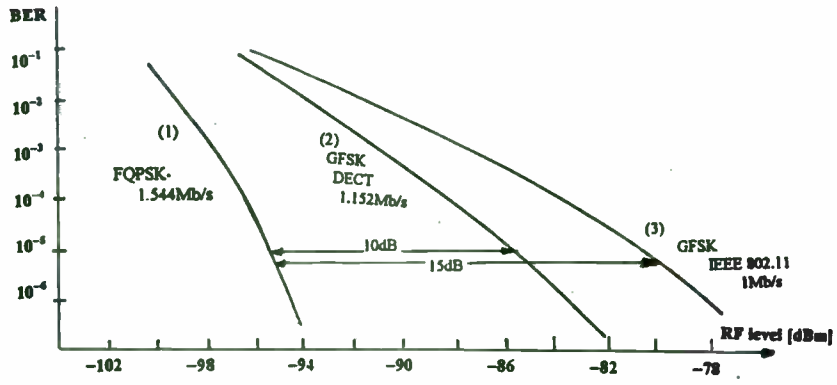

Fig 7 Performance comparison of standardized DECT, IEEE 802.11 and of nonlinearly amplified FQPSK systems. Illustrative measured data and approximate standardized system specifications of BER as a function of received RF level in [dBm] are shown. Curve (1) is a Lockheed Martin measurement result of a 2.40-2.48GHz RF link operated at 1.544Mb/s with FQPSK and a chipping rate of 16.984Mchips/second. Measured at Lockheed Martin, Salt Lake City, UT on 10/15/96 with EB200KF 70MHz IF modem and Celeritek's IF-RF link operated at full saturation, C-class RF amplifier (+25.5dBm at TDD switch output). Curve (2) is an illustrative DECT standardized BER specification for GFSK with BT_b=0.5 operated at a 1.152Mb/s data rate in the 1.88-1.99GHz RF band. Curve (3) is a typical IEEE 802.11 performance measured at 1Mb/s rate with standardized GFSK with BT_b=0.5 in the 2.40-2.48GHz band. Curves (2) and (3) are based on: "Cost effective evaluation of digital communication ICs," an article by Marc Brendan Judson of the Philips Semiconductor-Communications Product Division, in "RF Design," October 1996.

The significant 10dB to 16dB fade margin advantages of the FQPSK and GMSK systems are evident from the measured data on the Lockheed Martin EB200KF 2.4GHz system. For a received carrier power of -95dBm, the BER of this system is 10,000 times lower than that of the DECT and IEEE 802.11 systems

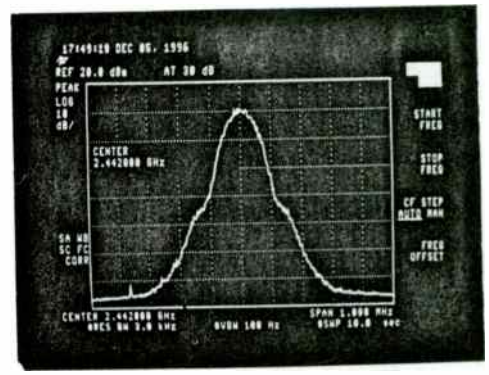

Fig.8 2.4GHz power spectrum of an FQPSK[10;11] product in full saturation NLA RF output power of +27.5dBm at 192kb/s rate. In Fig. 8, 9, 10, 15 different coefficients have been programmed -for a variety of specific radio requirements and applications.

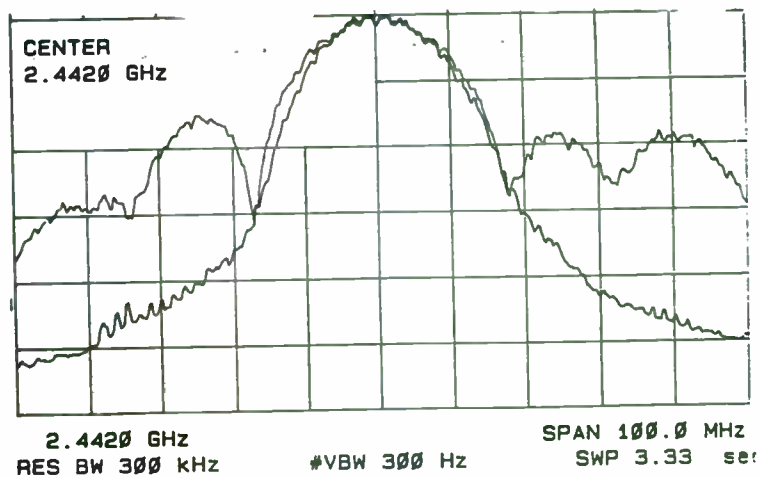

Fig. 9 Measured PSD of Direct Sequence Spread Spectrum/CDMA of the NLA FQPSK-based IOCOMM-IOTA system [18] at 17Mc/s
lower trace and with conventional OQPSK (upper trace)

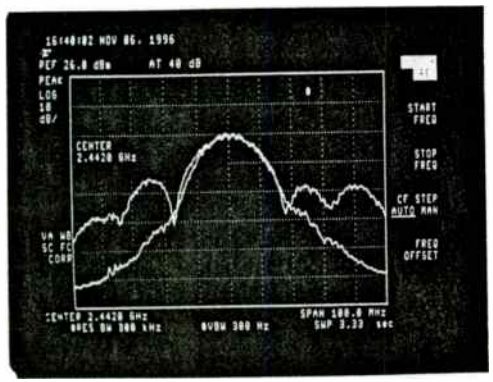

Fig. 10 FQPSK (lower trace) and OQPSK NLA spectra at 34Mb/s over CELERITEK RF-2.4GHz system. Modem "EB200KF" manufactured by Lockheed Martin under license of Feher et al. patents listed in reference [10].

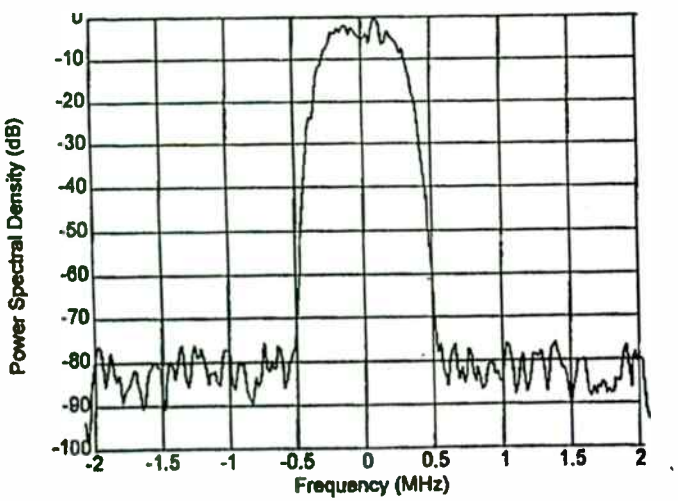

Fig.11 An illustrative spectrum of LIN(Linearly RF amplified class AB) QPSK and LIN amplified FQPSK system operated at a bit rate of approx . 850kb/s This spectrum is typical for some currently specified DoD systems. For a robust BER of about 5*10(exp-6) at Eb/No=10.5dB conventional QPSK,OQPSK and FQPSK are suitable for such a highly spectral efficient requirements. Constant envelope robust BER performance systems such as GMSK, and CPM do not meet these efficiency requirements.

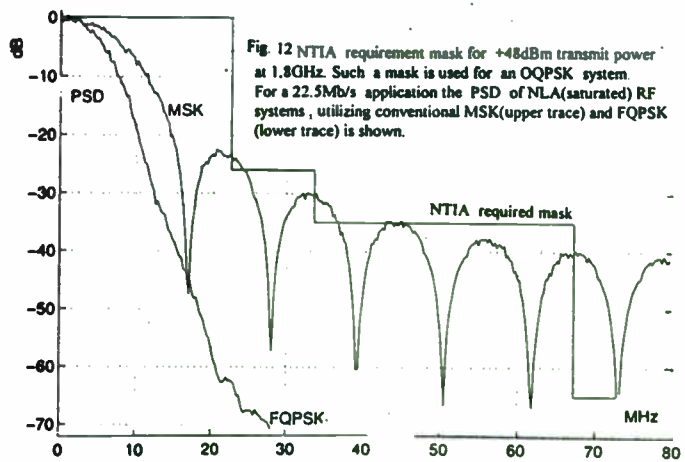

Fig. 12 NTIA requirement mask for +48dBm transmit power at 1.8GHz. Such a mask is used for an OQPSK system. For a 22.5Mb/s application the PSD of NLA(saturated) RF systems , utilizing conventional MSK(upper trace) and FQPSK (lower trace) is shown.

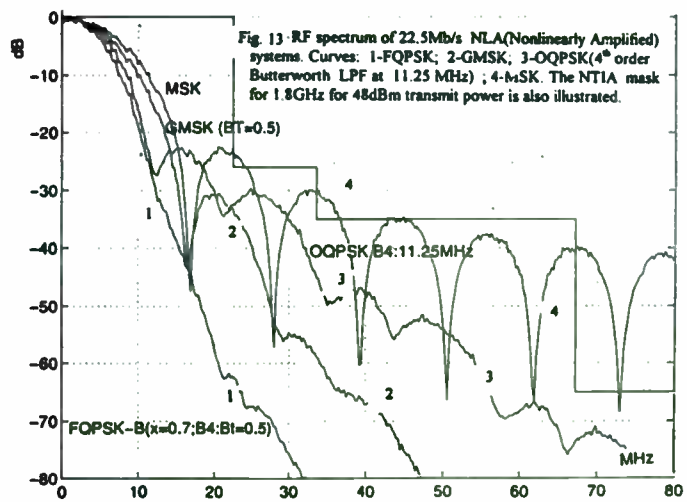

Fig. 13 RF spectrum of 22.5Mb/s NLA(Nonlinearly Amplified) systems. Curves: 1-FQPSK; 2-GMSK; 3-OQPSK(4th order Butterworth LPF at 11.25 MHz) ; 4-MSK. The NTIA mask for 1.8GHz for 48dBm transmit power is also illustrated.

In the commercial arena the major standardized 270kb/s+ rate GSM (more than 60 million GMSK quadrature modulated subscribers), 20Mb/s+ rate flexible bit rate HIPERLAN, the 1Mchip/s+ CDMA and numerous other higher-speed wireless and SATCOM products operated up to 120Mb/s+ rates, use quadrature modulator/coherent demodulator FQPSK, GMSK and OQPSK interoperable and compatible structures. Among the surveyed robust BER performance modem/ NLA radio techniques, FQPSK offers the highest power and spectral efficiency [1-21].

3. COMPATIBLE ARCHITECTURES/INTEROPERABILITY OF MILITARY AND COMMERCIAL SYSTEMS

From Table 1 note that GMSK modulation is used in major commercial standards in the US and internationally by many millions of users. From Table 2 note that higher speed systems (more than 50kb/s) use quadrature modulated OQPSK, QPSK and MSK systems. To leverage commercial products and developments with military applications and to develop a new standard, we selected techniques used by both communities. The new FIRST standard has initial applications in the military range, Test and Evaluation (T&E) and training fields. It also has the potential to be applicable in the commercial arena.

Dual mode military and commercial joint developments and implementations will lead to significant performance improvement, increased power and spectral efficiency by using compatible modulation/radio - Physical Layer (PHY) interfaces. These systems include:

"FQPSK" = "OQPSK" = "GMSK" = "MSK"

The above "equal" ("=") signs between FQPSK, OQPSK, GMSK and MSK indicate that these systems (appropriately designed and specified) have interoperable and compatible architectures [10-16]. Note that "FQPSK" is an abbreviation for Feher's QPSK [10-12]. Enhanced performance quadrature modulated GMSK and OQPSK systems have also been implemented [10-21]. The well-known MSK systems have the advantage of NLA radio applications, however are not sufficiently spectrally efficient for new, emerging applications. Interoperability of DoD's FIRST, potential other new emerging military or telemetry applications and commercial, universal global wireless systems and networks [1-21] is attained by the above "architectural and interoperable/compatible" aforementioned relationship.

In Fig. 1-3 architectures, signal pass and functions performed by a typical FIRST vehicle transceiver are illustrated. In Fig. 4 a typical transceiver block diagram of a Nonlinearly Amplified (NLA) modem/RF system is illustrated. In Fig. 5-6 the wide-open demodulated eye diagrams and the measured BER performance of a 34Mb/s system are depicted. Note that the FQPSK system in an NLA as well as LIN mode is within 1dB of ideal LIN (Linearly Amplified) coherent PSK theory. In Fig. 7 a performance comparison between standardized IEEE 802.11, DECT and FQPSK systems illustrates 7dB to 15dB advantage of the measured 2.4GHz FQPSK-RF link operated at 1.544Mb/s. Fig. 8-15 illustrate the spectral efficiencies attainable by programmable modulation formats.

Due to space limitation in this Conference Proceedings we limit our briefing to figures and tables. These highlight DoD's FIRST-TWG-standardized specifications and preliminary conclusions as of December 1996. In Table 3 requirements of the FIRST standard Physical Layer (PHY) technologies and specifications [Draft.1.0; Rev 1; Dec. 9, 1996] are highlighted. The list of references provided in Section 4 is particularly useful for details not contained in this paper.

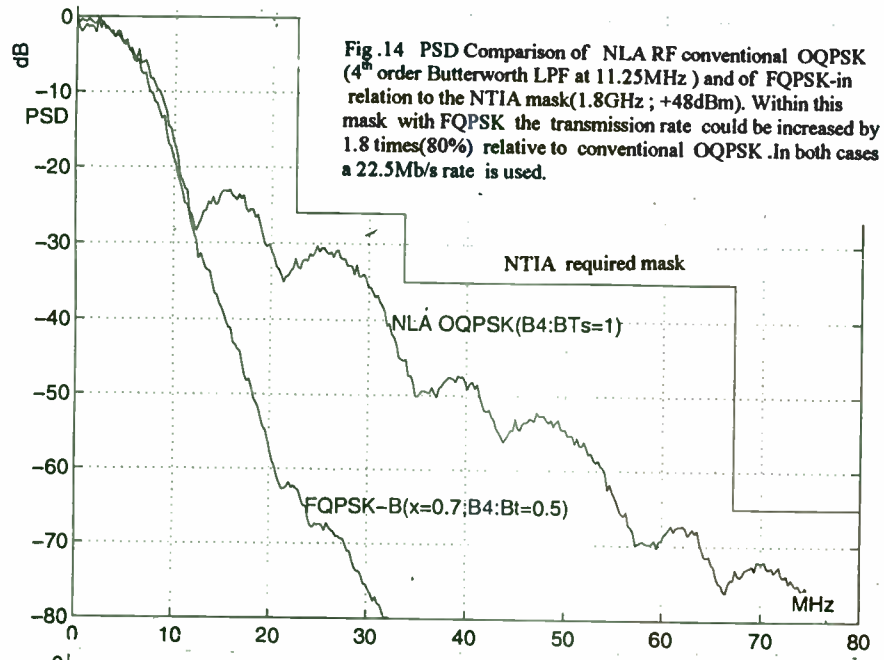

Fig .14 PSD Comparison of NLA RF conventional OQPSK (4^{th} order Butterworth LPF at 11.25MHz) and of FQPSK-in relation to the NTIA mask(1.8GHz ; +48dBm). Within this mask with FQPSK the transmission rate could be increased by 1.8 times(80%) relative to conventional OQPSK .In both cases a 22.5Mb/s rate is used.

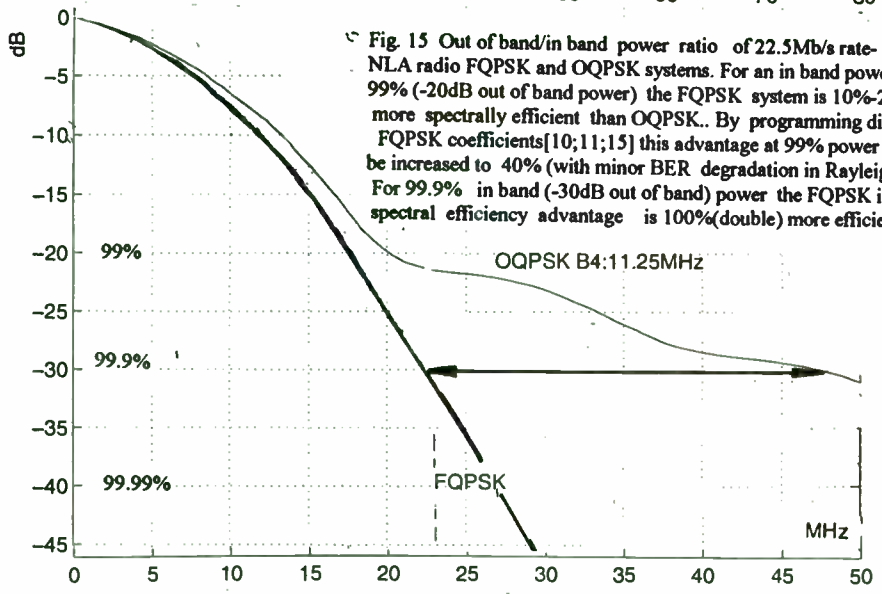

Fig. 15 Out of band/in band power ratio of 22.5Mb/s rate-NLA radio FQPSK and OQPSK systems. For an in band power of 99% (-20dB out of band power) the FQPSK system is 10%-25% more spectrally efficient than OQPSK.. By programming different FQPSK coefficients[10;11;15] this advantage at 99% power could be increased to 40% (with minor BER degradation in Rayleigh fades) For 99.9% in band (-30dB out of band) power the FQPSK integrated spectral efficiency advantage is 100%(double) more efficient .

Table 3 Specifications/requirements of DoD's common RF data link standard FIRST. Pbysical Layer(PHY). Modulation/RF.
Data rates and performance highlights
FIRST Technical Working Group (TWG) Specification
Draft 1.0, Rev. 1, Dec. 9, 1996. Partial list from specifications.

1.	Bit rate range	10kb/s to 45Mb/s (22.5 Mchip/sec)	
2	Data rate increments	N * 8kb/s (low rates) N * 64kb/s (medium rates) N * 256kb/s (high data rates) N = 1,2,3,4, . . .	
3	Modulation	FQPSK or compatible enhanced efficiency GMSK or OQPSK	
4	RF amplification and transceiver	Modulation/demodulation must be suitable for NLA (NonLinearly Amplified (saturated) RF power efficient Transceivers as well as for Linearly Amplified (LIN) increased spectral efficiency RF applications	
5	Integrated power spectral efficiency [b/s/Hz] requirements	For NLA (saturated; C-class) and for LIN operated transceivers the spectral efficiency will meet at least the following objectives:	
		NLA transceivers [b/s/Hz]	**LIN transceivers [b/s/Hz]**
	99% occupied in-band power (-20dB integrated out of band)	1.2b/s/Hz	1.8b/s/Hz
	99.9% in-band power (-30dB integrated out of band)	0.9b/s/Hz	1.6b/s/Hz
	99.99% in-band power (-40dB integrated out of band)	0.7b/s/Hz	1.5b/s/Hz
6	Power Spectral Density (PSD) [b/s/Hz] minimal efficiency requirements relative to maximal in-band PSD		
		NLA transceivers	**LIN transceivers**
	-20dB	1.0 b/s/Hz	1.70 b/s/Hz
	-30dB	0.9 b/s/Hz	1.60 b/s/Hz
	-40dB	0.45 b/s/Hz	1.55 b/s/Hz
	-60dB	0.25 b/s/Hz	1.50 b/s/Hz
7	Probability of Error Performance(BER): BER = f(E_b/N_o) requirement (raw - uncoded) for both LIN and NLA systems specified in AWGN stationary environment		
		E_b/N_o[dB]	**BER better than**
		7dB	10^{-2}
		9dB	10^{-3}
		11dB	10^{-4}
		13dB*	10^{-6}
		15dB*	10^{-8}

* for systems above 300kb/s

References

1. A. Cameron, T. Cirineo, K. Eggertsen: "The Family of Interoperable Range System Transceivers - (FIRST)," *Proceedings of the International Telemetering Conference,* October 29-30, 1996, San Diego, CA. (pp. 577-584)
2. FIRST Joint Program Office: "Family of Interoperable Range System Transceivers (FIRST)," *Acquisition Report: Requirements vs. Capabilities Section,* July 1996 (Draft version), Naval Air Warfare Center, Weapons Division, Point Mugu, CA 93042-5001.
3. FIRST Program Office: "Commercially Available Wireless Standards and Equipment - Synergy with DoD's FIRST," *DoD Common Data Link Technical Working Group (TWG),* FIRST.techr.1.doc, Nov. 9, 1996.
4. FIRST Program Office, T. Cirineo: "Test Report, EB200KF Lockheed Martin FQPSK System," *DoD Common Data Link Technical Working Group,* U.S. Navy, Point Mugu, CA 93042, Nov. 27, 1996.
5. FIRST Program Office, S. Douglas: "Memos Regarding JTCTS for FIRST," *from NWAD,* Nov. and Dec. 1996.
6. FIRST Program Office, "FIRST Common Data Link Standard - Physical Layer (PHY) and Multiple Access Method (MAC) Specifications," *DoD Common Data Link Technical Working Group,* U.S. Navy, Point Mugu, CA 93042, Draft 1.0, Rev. 0, Dec. 4, 1996.
7. E.L. Law: "Binary PCM/FM: Tradeoffs between spectral occupancy and bit error probability," *Proceedings of the International Telemetry Conference,* 1994.
8. E.L. Law: "Performance of PCM/FM During Frequency Selective Fading," *Proceedings of the International Telemetry Conference,* 1995.
9. Range Commanders Council, Telemetry Group: "Telemetry Standards," *IRIG Standard 106-96,* May 1996, Published by Secretariat.
10. Feher et al. U.S. Patents: 4,567,602; 4,339,724; 4,644,565; 5,491,457 and Canadian Patents: 1,211,517; 1,130,871; 1,265,851; *licensed exclusively by Digcom, Inc.*; 44685 Country Club Drive; El Macero, CA 95618; USA; Tel. 916-753-0738; Fax 916-753-1788.
11. Digcom, Inc.: "Technology Transfer, Licensing & Consulting - InfP.1; 7/96" *Digcom file: InfP.1; 7/96,* July 1996. An approximately 100-page information packet which includes Feher et al. patents and technology transfer information. Available upon written request from Digcom, Inc.; 44685 Country Club Drive; El Macero, CA 95618; USA; Tel. 916-753-0738; Fax 916-753-1788.
12. K. Feher: "*Wireless Digital Communications: Modulation and Spread Spectrum.* Prentice Hall, 1995.
13. K. Feher: "Filtering inventions enhance modulated RF products," *Microwaves & RF,* April 1995
14. M. Yu et al.: "$\pi/4$-FQPSK: An efficiency improved, standardized $\pi/4$-DQPSK-compatible modulation/nonlinearly amplified RF wireless solution," *IEEE Trans. on Broadcasting,* June 1996
15. Y. Guo, et al.: "A new FQPSK modem/radio architecture for PCS and mobile satellite communications," *IEEE Journal on Selected Areas in Communications*, Feb. 1995.
16. K. Feher, M. Yu, D. Lee, W.C.Y. Lee, D. Bayendor: "Innovative Modulation Approaches Enhance CDMA and GSM Performance," *Wireless System Design,* October 1996
17. B. Krishan, D. Shih, B. Singh, H. Martinez, K. Feher; NovaLink, Inc.: "Data modem/RF technology for new wireless PLMR and CDPD applications," *The Proceedings of the 4th Annual Wireless Symposium*, Santa Clara, CA, February 12-16, 1996.
18. T. Defries and D. Bayendor, IOTA, Inc. "DS-SS high-capacity (1.544Mb/s to 10Mb/s) FQPSK power-efficient modem/radio," IOCOMM® of IOTA, Tel. 520-771-9397; Fax 520-541-9324, *The Proceedings of the 4th Annual Wireless Symposium, CA,* Feb. 12-16, 1996.
19. EIP Microwave Communicator: "Product Announcement," *IEEE MTT,* June 18-21, 1996; Ivan Andres; EIP Microwave, Inc.; 1589 Centre Pointe Drive, Milpitas, CA 95035.
20. Lockheed Martin manufactured "EB200KF FQPSK-GMSK Universal Modem/Radio" under license of Feher patents. Contact: L.K. Erickson, Lockheed Martin, Tel. 801-594-2044; Fax 801-594-2195 or Digcom, Inc. (See Ref. [11] above.)
21. FIRST Joint Program Office: " Spectrally and Power Efficient Integrated Modem/Radio Alternatives for FIRST, based on cost efficient commercially available universal data rate FQPSK-GMSK and OQPSK technologies," *Report No: FIRST.techr.2.doc,* TWG meeting, Dallas, Dec. 1996, Naval Air Warfare Center, Weapons Division, Point Mugu, CA 93042-5001.

Analysis of Wide-Area Wireless Data Communication Services

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Most of the existing applications were originally designed for wired networks. Unreliable RF environments and limited available bandwidth are the major differences between wired and wireless networks. The wireless networks with higher layer protocols optimized for wireless environments have better performance, but it is costly to port the existing wire-line applications to these new higher layer protocols. Both circuit-switched and packet-switched approaches have been used for wireless data communications. However, the packet-switching approach makes more efficient use of the wireless medium. Several protocol suites are introduced for wireless networks, which are mostly closed networks.

Ericsson's MOBITEX is a mobile data technology which uses a cellular architecture with multichannel frequency reuse, store and forward capability, and an air interface known as ROSI (RadiO SIgnaling). It uses a proprietary network-layer protocol (MPAK) and transport protocol (MTP/1) that are optimized for radio environments. Motorola's ARDIS is based on single-frequency reuse, where a single frequency is shared among all cell sites in an area. As a result, the system has limited capacity. MDC-4800 by Mobile Data International (MDI) and Motorola's RD-LAP protocols are used in ARDIS networks.

CDPD was originally introduced by IBM for packet switching communication as an overlay of the existing analog cellular voice network. The CDPD standards were later defined by a consortium of several phone companies as an open architecture. CDPD standards introduce a physical and link layer for the air interface and support the IP and OSI protocols for network and transport layers. The existing applications can be easily ported to CDPD environments. CDPD also supports the AT command set, which facilitates communication over wireless links.

Two-way messaging services using narrowband PCS is another new trend in the wireless data communication market. Destineer (Mtel's nationwide wireless network) consists of two nationwide networks for inbound and outbound traffic. Metricom's Ricochet is a high-speed microcellular data network which uses frequency-hopping spread spectrum technology. Following the recent FCC auctions for narrowband and broadband PCS, several companies are aggressively deploying personal communication networks.

One of the problems with the existing wireless data networks is their low speed. The market asks for multimedia support in wireless data networks, and the technology is mature enough and ready to offer that. Microcellular architectures introduce better frequency reuse, which can offer higher speed for wireless communication. Performance measurements such as blocking probability and call/packet dropping are some of the important factors in this regard. Microcell-only systems and microcells with macrocell overlay are two cellular approaches to networking. These solutions try to provide higher speed, better quality, and more reliable communication. Satellite systems are another player in the data communication market that can cooperate with cellular networks.

Interoperability is an important issue in wireless data networks. CDPD standards address the interoperability with other network standards, such as TCP/IP and ISO. RAM is connected to TCP/IP, X.25, and SNA 3270 through the Mobigate gateway, which converts MOBITEX protocols to other protocols. The Portable Computer and Communications Association (PCCA) has introduced a wireless extension to the AT command set. The CDPD system specification includes that extended AT interface. Some products, such as Metricom's Ricochet modem, Ericsson's AT Mobidem, and Pinpoint's modem, support the AT command set. Standard extensions to the Winstock interface is another another activity in higher layers of the protocol stack. Oracle in Motion (OIM) has a client/server architecture that uses the native packet protocols and runs on RAM Mobile Data's MOBITEX and other wireless networks.

Using DECT for Wireless Multimedia Communication

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Abstract

DECT (Digital European Cordless Telecommunications) was originally introduced as a standard for digital in-house telephony applications. However, as a digital transmission system, DECT offers far more possibilities than simple telephony services. Depending on the application, wireless multimedia communications will place different requirements on a transmission system in terms of data rate, delay, error rate, etc. This paper will introduce the parts of the DECT protocol that are necessary to serve these requirements. Some protocol implementations have been realized, and the achieved results are presented here.

TEST AND MEASUREMENT SOLUTIONS

Test and Measurement Solutions

Session Chairperson: Ben Zarlingo,
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Using Adaptive Equalization in Modulation Analysis and Troubleshooting

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Many digital wireless systems use adaptive equalization to improve transmission range, reliability, and carrying capacity. The equalization accomplishes this by dynamically creating and applying a compensating filter, removing linear errors from modulated signals. These errors include group delay distortion, frequency response errors (tilt, ripple), and reflections or multipath distortion.

Analysis and troubleshooting of such systems can be made more efficient by using this same technique in measurement tools. Indeed, some impaired signals can only be measured *after* equalization.

This paper describes adaptive equalization and its benefits in modulation analysis and troubleshooting.

The purpose of test equipment in wireless design and manufacture is twofold: to understand and predict the performance of a system and to find and quantify problems so that they can be fixed (or ignored, if appropriate). To do this, test equipment is often called upon to mimic all or portions of the functions of a transmitter or receiver.

To test complete transmitters or to test components such as modulators and power amplifiers it is desirable to have some sort of ideal or perfect receiver. Test equipment has historically been called upon to perform this function, and it has been a constant effort to keep such equipment up-to-date with the components and systems it is designed to test.

Nowhere is this more true than in the field of digital communications. Several factors conspire to hamper the development of the ideal measuring receiver or demodulator. They include the fast pace of design and innovations, the complexity of systems and measurements, and the highly variable nature of the specifics of these systems.

Adaptive equalization is a good example. Though the technique is used in many digital radio receivers, it is only now starting to appear in the test equipment normally used to design and test these receivers. Since receivers which use adaptive equalization already exist commercially, it is obviously possible to design and manufacture them without test equipment so equipped. But it is considerably more difficult.

Fig. 1 illustrates one form of the difficulty. Does this measurement represent an acceptable 16QAM signal or an unacceptable one?

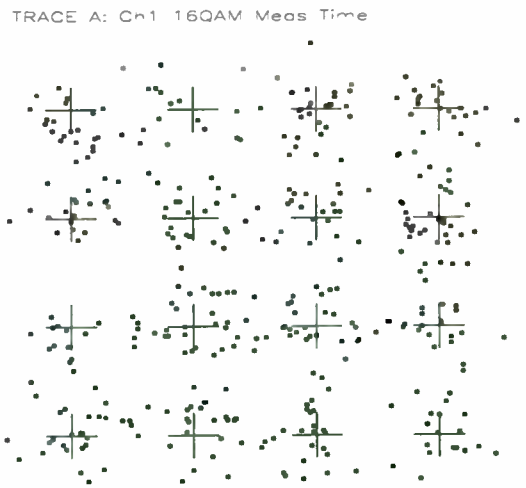

Fig. 1. 16QAM signal without equalization--15% EVM

The same question can be asked about the measurement in Fig. 2.

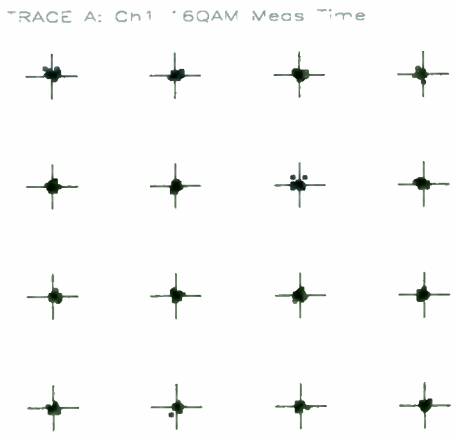

Fig. 2. 16QAM signal with equalization--1.5% EVM

Of course, these two measurements are of the same signal. The difference is the presence of an equalization filter in the measuring receiver, which reduces the error in the signal by an order of magnitude. Whether the signal quality is deemed acceptable or not is a decision that can now be made with full knowledge of how a real receiver (with adaptive equalization) would respond. In a less-extreme situation this kind of knowledge may allow an otherwise good modulator or transmitter to be used instead of thrown away.

Adaptive Equalization Primer

Since this paper covers the use of adaptive equalization rather than the theory, only a brief summary of adaptive equalization itself will be provided.

Equalization is the process of applying a filter to a signal to remove or compensate for the effects of linear distortion. This filter can be defined in the frequency domain by frequency response parameters such as gain and phase or group delay. Alternatively it can be defined in the time domain by its impulse response.

Adaptive equalization dynamically creates and applies such a compensating filter, modifying it to more completely compensate for distortion or to track changing signal characteristics.

Equalization is effective at compensating for linear distortion mechanisms including:

- Frequency response errors such as ripple or tilt
- Non-flat group delay or nonlinear phase
- Multipath or delay spread

However equalization in not effective on nonlinear distortion mechanisms such as:

- Noise
- Spectral regrowth or adjacent ch. interference
- Intermodulation
- Spurious
- Harmonic distortion

This lack of effectiveness on nonlinear distortion mechanisms in an unfortunate fact from the standpoint of receiver performance. However if the equalizer capability can be made switchable in the measuring receiver (test equipment), the result is an effective way to distinguish linear from nonlinear distortion. This has considerable implications in the testing of modulators, transmitters and transmission paths. These implications will be covered later in this paper.

Equalizer Types

Equalizers can be sorted into two main types: *Feed-forward* and *decision feedback*. A diagram of the feed-forward equalizer is shown in Fig. 3.

Fig. 3. Feed-forward equalizer topology

In this equalizer the input signal is passed through the equalization filter and then through any other filtering required by the system. Following detection or demodulation the signal is measured. The result of this measurement can then be used to refine the equalization filter.

The decision feedback equalizer topology is shown below in fig. 4.

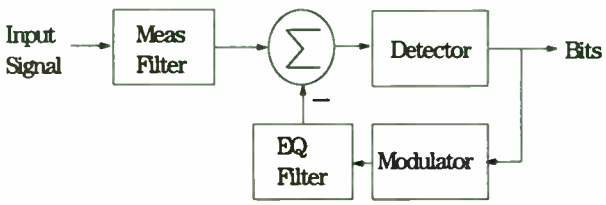

Fig. 4. Decision feedback equalizer topology

In this equalizer the demodulation result (recovered bits) is used as the input to a modulator circuit. The output of this modulator (an ideal, noise-free signal) is then filtered and subtracted from the input signal. This allows equalization to be performed without the equalization process itself adding noise to the signal.

Equalizer Algorithms and Training

All adaptive equalizers require some mechanism for adaptively changing filter parameters or "training" the equalizer. Equalizer training can be sorted into two main types: *Decision-directed* and those that use *training sequences*. Decision-directed training is illustrated in Fig. 5. The LMS (least mean square) algorithm is described in [1].

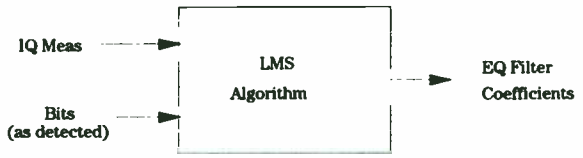

Fig. 5. Decision-directed equalizer training

Decision-directed equalizer training requires no prior knowledge of the transmitted data. This can be an advantage in test equipment where the necessity to provide such a sequence (and its exact position in a transmission, etc.) is avoided. However the training action (filter convergence) is slower and less certain when there are bit errors and is then often too slow to follow rapidly-changing channel characteristics.

For these reasons, an alternate method of training which uses a training sequence is more common in practical radios. It is shown in Fig. 6.

Fig. 6. Equalizer training using a training sequence

The use of a training sequence implies prior knowledge of a portion of the transmitted data. The training sequence carries no information and therefore reduces the payload of the system. However the sequence allows the equalizer to converge in the presence of many bit errors and can allow the equalizer to converge fast enough to follow rapid changes in the channel.

Adaptive Eq. in Test and Troubleshooting

Adaptive equalization in a flexible test instrument provides a variety of benefits. They include:

- Evaluating a signal in the same way that a receiver (equipped with adaptive equalization) would.
- Ability to separate linear from nonlinear distortion mechanisms so that design and troubleshooting effort can be concentrated on the important ones.
- Ability to measure small nonlinear distortions in the presence of large linear distortion that would normally obscure them.
- Ability to measure impaired signals. Accurate measurement of some impaired signals may require equalization to obtain a symbol lock and successful demodulation.
- Ability to derive important parameters of the linear distortion such as the frequency response of the channel or the timing of delay spread.

To demonstrate these benefits we will make use of measurements and displays from the HP 89441A Vector Signal Analyzer, the first general-purpose signal analyzer to offer an adaptive equalization capability.

Comparable Measurements

In systems where the receivers include equalization, many linear errors can be compensated for, and do not cause loss of information. Therefore measurements made in the lab or on the production line to evaluate the actual performance of a system should also include equalization.

If equalization is not performed it may be very difficult to predict the actual performance of a system. In addition, good transmitters or modulators may be rejected and much time or money may be spent in optimizing a design or adjusting a modulator or amplifier to minimize a source of distortion which has no real consequence.

In such measurements the equalizer in the test equipment must perform the same general function as the receiver equalizer, but an exact match of equalizer topologies or training techniques is not required.

Linear vs. Nonlinear Distortion

The ability to isolate problems and error sources is vital to successful system integration and troubleshooting. As mentioned previously, equalization is able to reduce the effect of linear error mechanisms only. By switching the equalization on and off in the precision receiver, the magnitude of both distortion types can be measured.

Of course the nature (linear or nonlinear) of a distortion source is a clue to its origin and to potential remedies. Fig. 7 below shows the constellation of an 8PSK signal without adaptive

equalization applied. Measured EVM is approximately 8%.

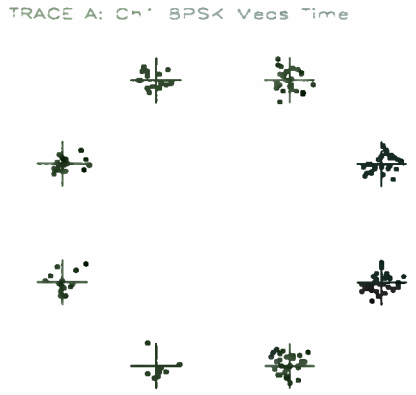

Fig. 7. 8PSK measured constellation without equalization

With an adaptive equalizer in the receiver the EVM is reduced to 5% as shown in Fig. 8 below.

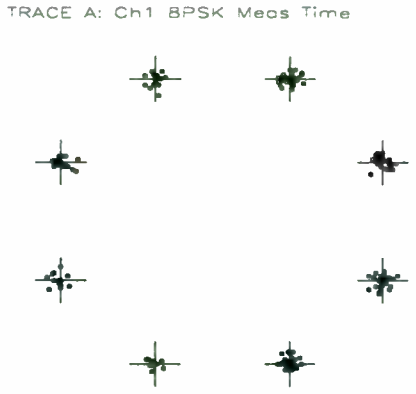

Fig. 8. 8PSK measured constellation with equalization

Other measurements (in addition to EVM) can now be made on the equalized signal to determine the nature of the nonlinear distortion. A flat EVM spectrum for example, would indicate a noise problem. An EVM spectrum raised at a band edge would indicate adjacent channel interference.

Measurements such as these could also be used to establish and manage a system error budget with separate categories for linear and nonlinear mechanisms, along with the usual categories for different system blocks.

Uncovering Smaller Distortions

In systems where receivers are equipped with equalizers it may be important to find and eliminate nonlinear distortion sources, even when their error contribution is much smaller than that of linear distortion sources.

Equalized error measurements are an obvious answer to this need. Consider the QPSK constellation in Fig. 9.

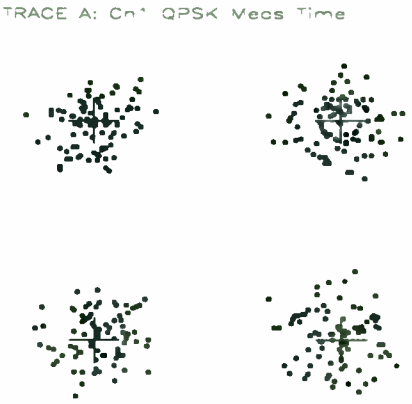

Fig. 9. QPSK measured constellation without equalization

This signal has both linear distortion and a small spurious signal which is in-band. That is not evident, however, from either the constellation display in Fig. 9 or the error vector spectrum measurement in Fig. 10 below.

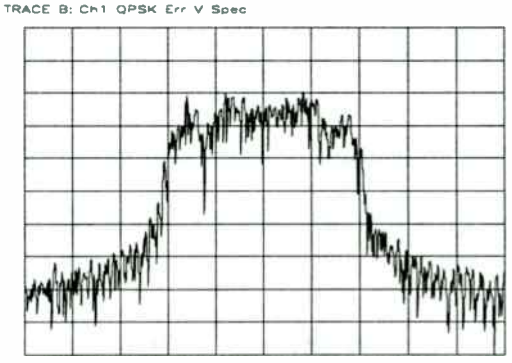

Fig. 10. QPSK meas. EVM spectrum without equalization

Adding an equalizer to the precision receiver removes the linear distortion and significantly changes both the measured constellation and EVM spectrum.

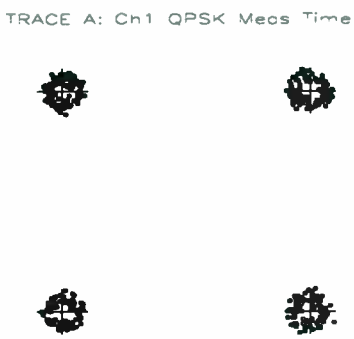

Fig. 11. QPSK measured constellation with equalization

The constellation in Fig. 11 clearly shows the effects of spurious interference. This is confirmed in Fig. 12 below.

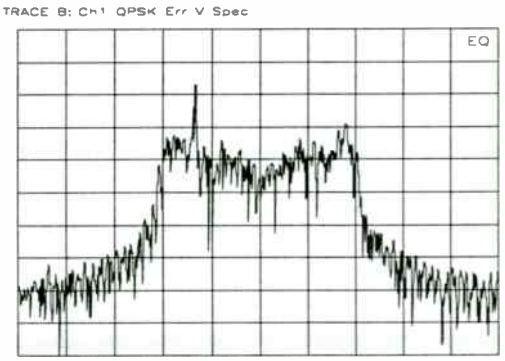

Fig. 12. QPSK measured EVM spectrum with equalization

The broadband error energy in the measurement has been considerably reduced, revealing a spurious signal in the channel. Its frequency can now be accurately measured, providing a clue as to its source.

Measuring Impaired Signals

In real-world situations some signals are impaired by large amounts of linear distortion. This is particularly true of over-the-air transmissions where multipath or delay spread is a problem. Without equalization in the receiver, these impairments may be too severe to allow symbol clock recovery and successful demodulation. An example is shown in Fig. 13.

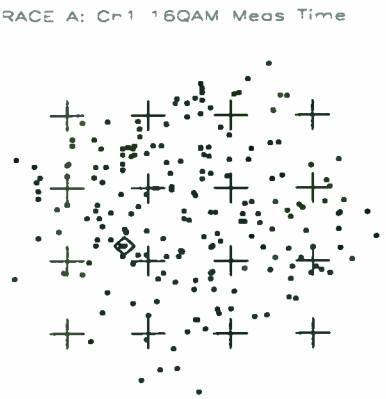

Fig. 13. 16QAM signal before equalization

It may be suspected from the dots in the constellation that this is some sort of QAM signal with a square constellation. However the receiver is unable to regenerate a symbol clock and no quantitative information can be gained from this measurement.

Adding a decision-directed (no training sequence) adaptive equalizer to the circuit quickly improves the measurement. Fig. 14 below shows the early results while the equalizer is being trained.

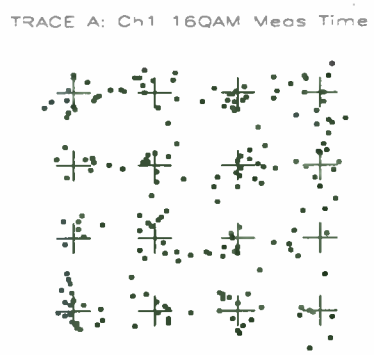

Fig. 14. 16QAM signal after 8 measurement updates

The symbol clock in the receiver is clearly now in a locked condition. Symbol errors are still present but demodulation is now successful.

Once symbol lock is achieved the equalizer trains (converges) much faster. Fig. 15 shows the measurement result after just 4 more measurement updates.

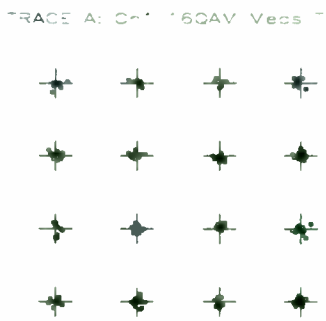

Fig. 15. 16QAM signal after 12 measurement updates

Measured EVM has been now been reduced to just 3% on a signal which could not be demodulated at all before equalization. The ability of this general-purpose adaptive equalizer to successfully train itself without a training sequence and without initial symbol lock is obviously important for severely-impaired signals.

Deriving Distortion Parameters

Once trained, the receiver's adaptive equalizer filter is itself an important source of information. In the HP 89441A, its complex filter coefficients can be viewed in the form of the impulse response of the equalizer filter. They can also be represented (in inverse form) as the imputed frequency response of the channel.

Figure 16 below is an example of an equalizer filter impulse response.

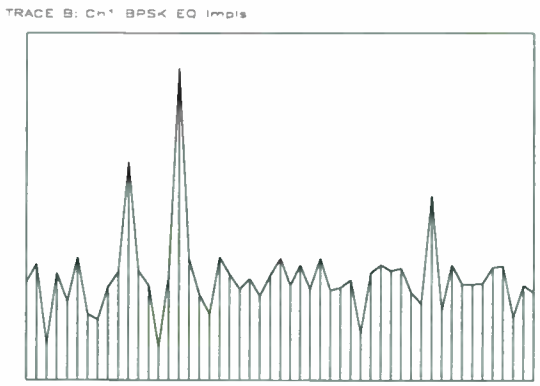

Fig. 16. Equalizer filter impulse response

The filter tap magnitudes are shown on the Y-axis in log magnitude format while the X-axis is linear in time or in symbols. In this case the symbol times are shown by the vertical bars.

A display such as this can be useful in determining the relative magnitude and timing of multipath or delay spread. The largest response represents the strongest signal received and the smaller responses represent weaker alternate paths. Note that one of the weaker signals has a negative delay relative to the strongest signal. This would indicate a situation where the direct (shortest) path has more attenuation than one of the alternates.

To understand linear distortion in a transmitter it is more useful to look at frequency response parameters such as gain and phase or group delay. The frequency response of a channel can be derived from the impulse response of the equalizing filter as shown in Fig. 17. This is a filtered version of a signal from an NADC (IS-54) transmitter.

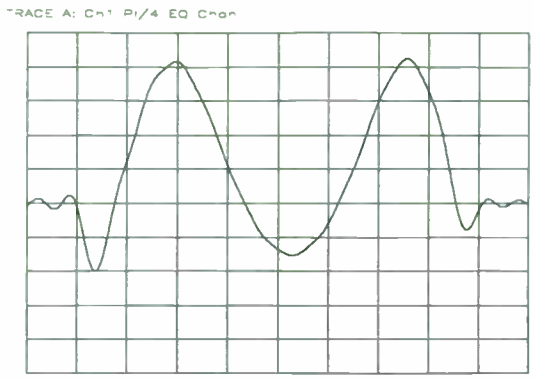

Fig. 17 Channel frequency response, log magnitude

This measurement of the channel frequency response is in log magnitude format and peak-peak ripple is approximately 2.8 dB.

Since the filter coefficients are complex, the derived channel frequency response can also be expressed as phase or group delay.

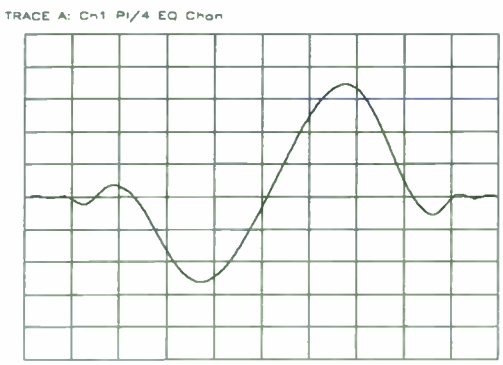

Fig. 18 Channel frequency response, phase

Fig. 18 above is the phase of the channel frequency response. Peak-peak phase variation across this filtered channel is 30 degrees.

Fig. 19 below shows the group delay or phase linearity of the channel. This filtered channel deviates from ideal (constant) delay by approximately 20 microseconds.

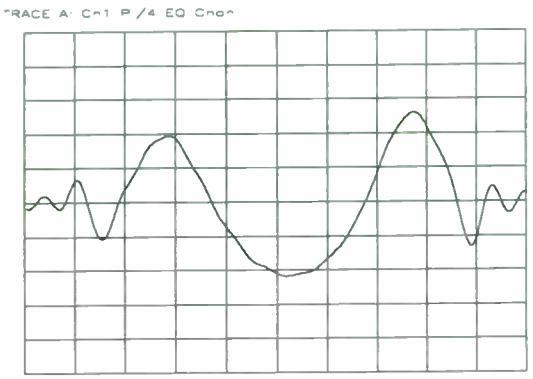

Fig. 19 Channel frequency response, group delay

The information generated by, and derived from adaptive equalization is not a universal substitute for traditional network analysis. However it is an accurate tool for troubleshooting and system verification. It has the important added advantage of using the (NADC in this case) signal itself as a network stimulus. Therefore it can be used as a single-ended, in-service measure of transmitter characteristics and/or channel impairments.

Restrictions and Limitations

As demonstrated here, adaptive equalization implemented in a general-purpose, precision receiver has several important uses. However any generalized implementation will also have some limitations relative to implementations which are application-specific.

This adaptive equalizer does not operate in *real time*. It is a block-mode implementation and does not continuously follow the input signal. Some portions of the input signal are usually not measured because the analyzer does not acquire new data while it is processing previous data.

Since it is not real time and is deprived of the information in a training sequence, this equalization adapts more slowly and is therefore restricted to "stationary" signals. For example this rules out its use for in-service measurements in moving vehicles. Fortunately a time capture mode with extensive overlap processing is available in the HP 89441A and this can be used in some cases to make signals appear to be stationary.

This general-purpose equalizer is not usually as robust as those designed for a specific application. Their parameters can be carefully selected to optimize convergence and stability and they often benefit from training sequences.

For similar reasons, the results produced by this generalized receiver will not exactly match those from an application-specific receiver. Differences in equalization and training techniques and in operating parameters will yield some differences in demodulation results.

Finally, this equalization algorithm cannot be guaranteed to be stable under all conditions. Equalizer training is similar to the operation of a control system, and under some conditions the training algorithms will diverge or fail to converge.

Despite these limitations, this general-purpose implementation of adaptive equalization has significant benefits for both the design and manufacturing of wireless systems. This is true whether or not the systems to be measured use adaptive equalization themselves.

References

[1] "Block Implementation of Adaptive Digital Filters," IEEE Transactions on Circuits and Systems, June 1981, Vol. CAS-28, No. 6.

Phase Noise Measurement Techniques for the Automated Testing Environment

Al Street and Joe DiBona
RDL, inc.

Introduction

This paper reviews two basic methods for measuring phase noise on a frequency source: the Phase Locked Loop method and the Delay-line Frequency Discriminator method. After a basic description of each method, the critical considerations will be discussed and comparisons of the two methods will be summarized. Finally, automated measurements will be examined.

Phase Locked Loop method

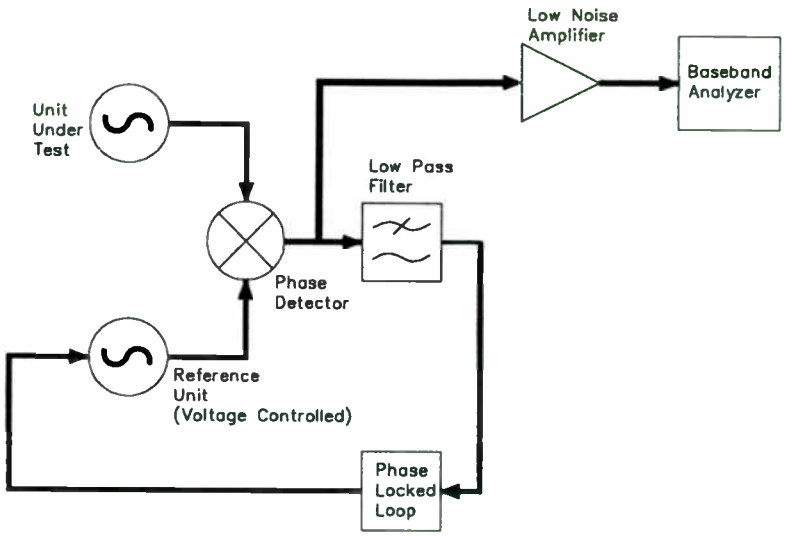

Figure 1. Phase locked loop measurement diagram (simplified)

The basic block diagram of this technique is shown in figure 1. Two sources are phase locked together and their outputs are presented to a double-balanced mixer acting as a phase detector. With the signals at identical frequencies and in phase quadrature, the output of the phase detector is a fluctuating voltage which is proportional to the instantaneous phase difference between the two signals. This fluctuating output voltage represents the combined phase noise sidebands of the two input signals. Within the loop bandwidth of the PLL, the phase noise spectrum of the source under voltage control is suppressed by the loop tracking response.

Critical Calibration / Setup requirements

The phase noise of the reference source as well as that of the unit under test (UUT) contribute to the output noise from the phase detector. If the noise of the reference source is equal to that of the UUT, the measurement results will be 3 dB higher than the noise of the UUT. To

ensure that this noise "bump" due to the reference source is less than 0.5 dB, the noise of the reference must be at least 10 dB below that of the UUT.

If the reference source and the UUT are not well isolated from each other, there will be a tendency for the two sources to "injection lock" which will cause measurement errors because of the uncertainty of the loop characteristics. Combinations of isolators, pads, and amplifiers are often used on each source output to defeat injection locking. It may also be necessary to power the two sources from separate supplies.

Within the bandwidth of the phase locked loop the noise is suppressed; therefore the loop must be characterized carefully so the suppression can be corrected for in the measurement results. An alternative is to narrow the loop and only consider the noise far outside of the loop bandwidth, which may not be practical.

Power levels within the measurement setup must also be considered relative to noise floor. For example, with a thermal noise floor of -174 dBm/Hz and an RF power of 0 dBm, noise sidebands at -160 dBc/Hz will be bumped by about 0.2 dB.

Calibration at any one offset frequency can be obtained by phase-modulating one of the two sources, noting the sideband level on an RF analyzer, and equating that level with the resultant baseband signal produced at that offset.

Delay-Line Discriminator Method

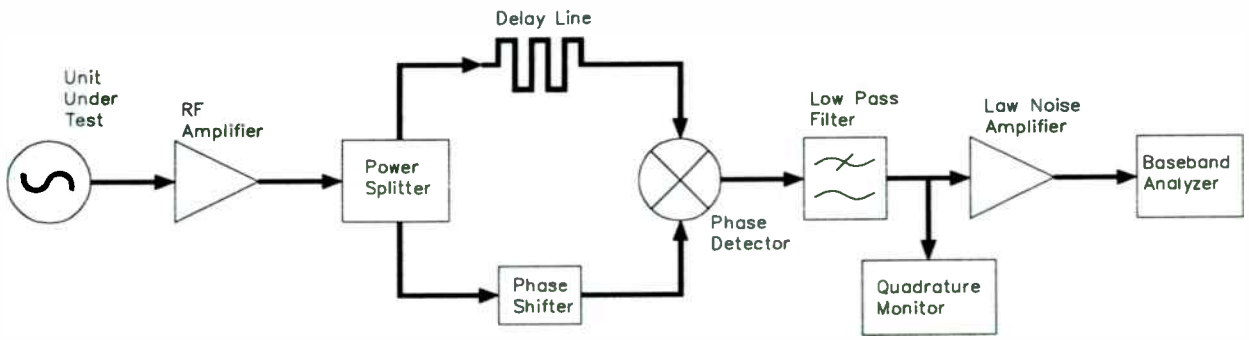

Figure 2. Delay-line Discriminator measurement

The basic block diagram of the Delay-Line Discriminator is shown in Figure 2. In this method the output of the test source is split into two signals. One of the two resulting signals is delayed and it and the undelayed signal are presented to a phase detector (as before, a double-balanced mixer). The fixed time delay causes a phase shift in the delayed signal which is proportional to the frequency. When compared to the undelayed signal from the other path, frequency fluctuations on the original signal are converted to phase fluctuations. These phase fluctuations are converted by the phase detector into amplitude (voltage) fluctuations. As in the

phase locked loop method, the phase detector output is proportional to the input phase differences of two signals in phase quadrature at the input. The transfer response is

$$\Delta V(f_m) = \Delta f(f_m) \cdot \left[K_\phi \cdot 2 \cdot \pi \cdot \tau_d \cdot \frac{\sin(\pi \cdot f_m \cdot \tau_d)}{(\pi \cdot f_m \cdot \tau_d)} \right]$$

For offset frequencies that are less than $[(2 \cdot \tau_d)^{-1}]$, the above relationship is a linear function of f_m, the offset frequency. At higher offset frequencies, the response is nonlinear, so that correction of measured data is required. At the offset frequencies equal to multiples of $[(\tau_d)^{-1}]$, the response has a "null," making accurate measurements impractical. Therefore, the delay line length is chosen to provide maximum gain in the frequency offset range of interest while maintaining linear response over the frequency range.

Critical Calibration / setup requirements

Since the output is proportional to both the phase detector constant and the delay, we would like to make both large for maximum sensitivity. However, the presence of the (sin x) / x component introduces peaks and nulls into the response which complicates matters. For offsets less than $1/(2\pi\tau)$ this effect can be neglected. At greater than this offset a correction for the response must be made. Also, there are nulls in the response at even multiples of $n/(2\tau)$ where the system sensitivity degrades and can not be corrected for. Here the only option is to reduce the amount of delay to push the null out beyond the frequency of interest.

The noise floor vs signal level considerations that were described for the phase locked loop method also apply to the delay-line discriminator measurement method. This is also a consideration in selection of the amount of delay. For instance, 100 feet of .085 semi-rigid cable (150 nsecs delay) has about 2.5 dB loss at 50 MHz but about 12 dB loss at 1 GHz. Care must be taken when choosing the amount of delay to cover requirements for sensitivity as well as not overdriving components at lower frequencies or falling into the thermal noise floor at higher frequencies.

For maximum sensitivity, the two signals incident on the phase detector must be in quadrature. This is nominally at 0 Volts output of the mixer. However, if AM noise is an issue, a more sensitive measure of quadrature is the phase at which the AM output of the mixer is at a minimum. Unfortunately, this is rarely at 0 Volts and will also change with RF frequency .

As with the phase locked loop method, calibration at any offset frequency can be accomplished by phase-modulating the source, noting the sideband level on an RF analyzer, and equating that level with the resultant baseband signal produced at that offset.

Comparison of the two methods

I. Phase locked loop method

Advantages:	Disadvantages:
Lower noise floor	Need second (reference) source at each frequency to be tested.
Good AM rejection	Reference source noise must be at least 10 dB below the noise of the unit under test to avoid significant distortion of the measurement.
	One source must be voltage-tunable.
	Tendency for injection-locking.
	The phase locked loop parameters must be characterized for each measurement to insure accuracy.
	Poor tolerance of frequency drift of source

II. Delay-Line Discriminator Method

Advantages:	Disadvantages:
Simpler setup.	Relatively poor noise floor at low offset frequencies
Does not require reference source.	Poor AM rejection
Good noise floor at high offset frequencies.	
Easier calibration.	
No possibility of injection locking.	
Wide RF frequency coverage.	
Less sensitive to source frequency drift.	

Automated measurements

PLL method

Automated measurement systems based on the phase locked loop method are commercially available. While these systems strive to make utilization of this method more convenient for the user, the advantages and disadvantages previously described still apply for the most part.

Delay-Line Discriminator Method

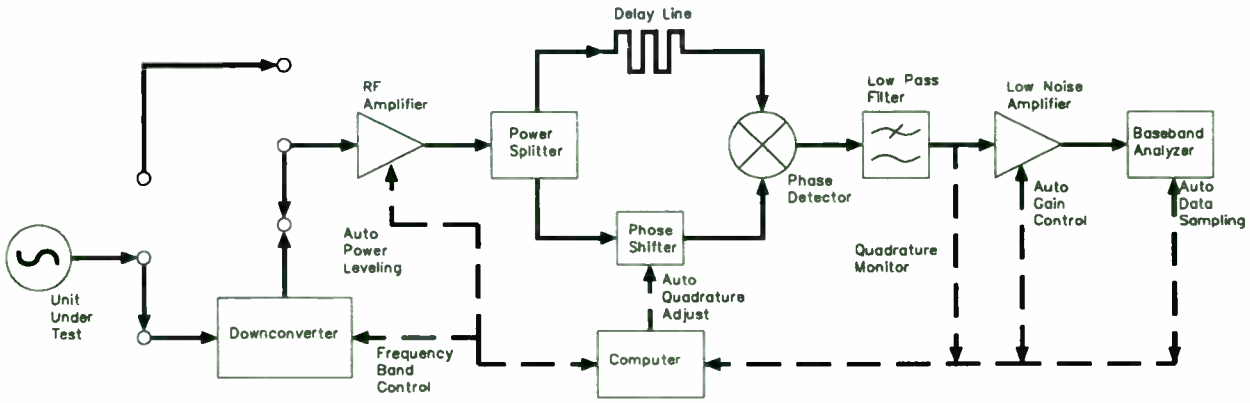

Figure 3. Automated noise measurement using RDL NTS-1000A Phase Noise Analyzer and DCR-14000 downconverter

An automated implementation of the delay-line discriminator is shown in figure 3. In this approach, the concerns described previously (and others) have been addressed. Automatic power leveling circuits ensure that power levels are correct for the RF frequency of interest. Quadrature is established automatically and monitored during the measurement to prevent degradation of measurement accuracy. Calibration occurs automatically at each measurement using a precisely calibrated, wideband modulator. Baseband gains and filters are selected as appropriate for the offset range under consideration. Data sampling, averaging and post processing are all handled under software control.

With this instrument, power leveling, calibration, quadrature, baseband gain and data sampling are all handled automatically. Measurements can be made over a wide range of RF input frequencies and power levels without reconfiguring the setup. Pass/fail limits can be programmed for use in a high-speed production environment. The complete measurement process takes as little as one second depending on menu configurations.

Considerations for Extending the Frequency Range of the Measurement

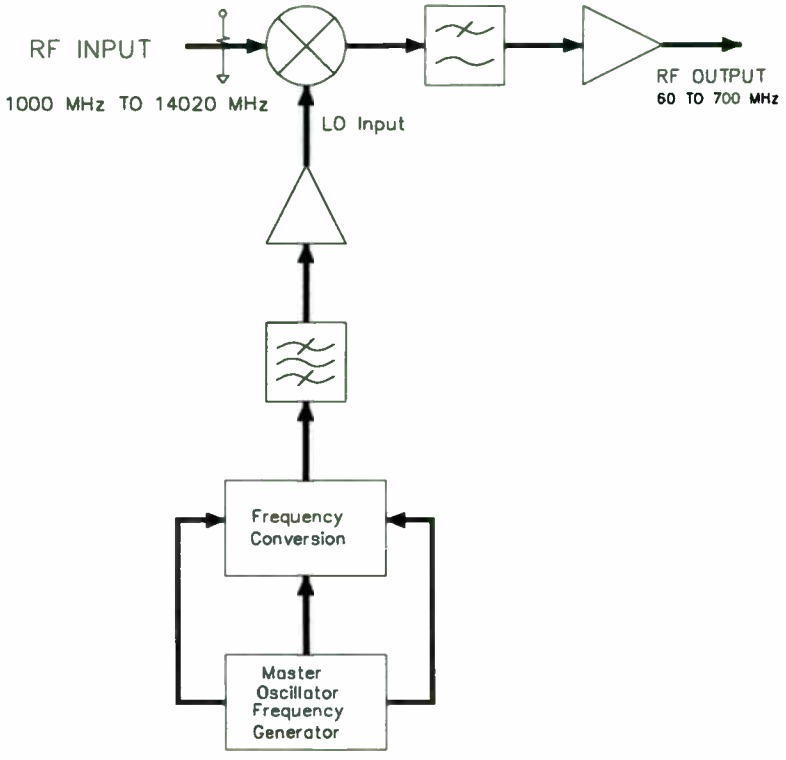

Figure 4. Downconverter

A method commonly used to extend the frequency range of a delay line discriminator noise measurement is downconversion.

Figure 4 shows the basic functionality of a typical down-conversion scheme. There are several considerations involved in designing this scheme. The goal is an intermod-free downconverter which causes no degradation in the noise floor of the frequency discriminator.

The noise floor is simply a function of the source which generates the LOs. When a signal is passed through the mixer the resulting noise is the sum of the two sources.

For example, the source employed by the DCR-14000 starts to affect the NTS-1000A discriminator floor immediately depending on the offset frequency being measured. At offsets less than 1.0 kHz from the carrier the downconverter causes less than 1 dB of degradation to the noise floor with inputs up to 14020 MHz (see figure 5).

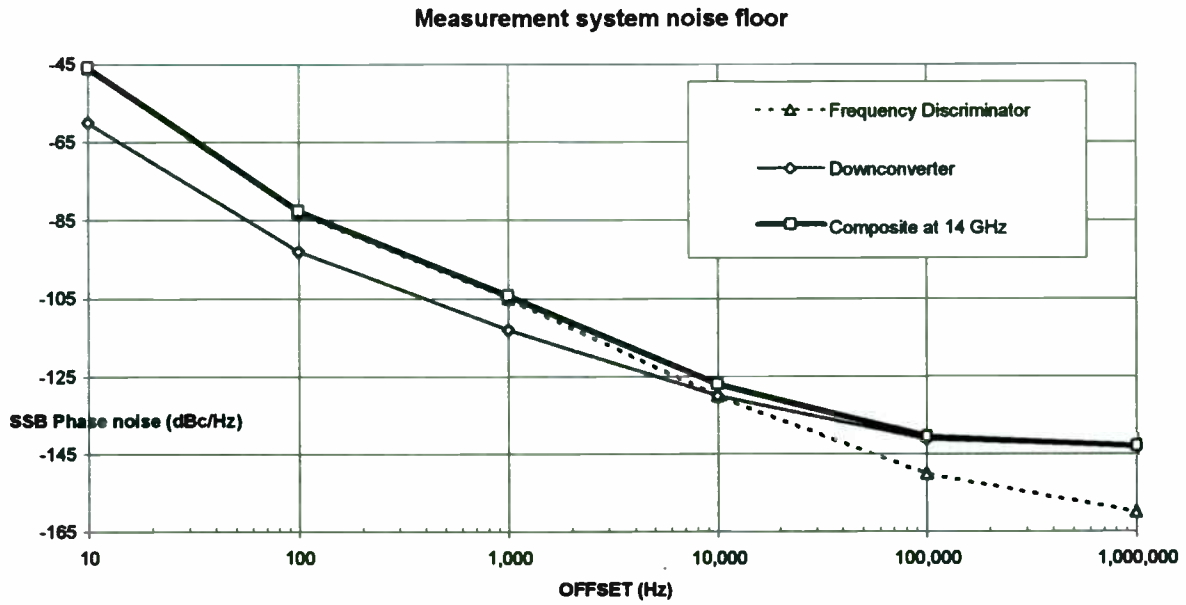

Figure 5. Measurement System Noise Floor

The intermods are caused by different multiples of the LO mixing with different multiples of the RF. This causes mixer products to land in the measurement bandwidth. Quite often this causes a hole in the measurement abilities of the downconverter and delay line discriminator combination.

Conclusion

Many issues must be carefully considered when making phase noise measurements of today's sources. But with careful design and thoughtful implementation, a Phase Noise Analyzer measurement system such as RDL's NTS-1000A coupled with a DCR-14000 frequency downconverter can provide reliable, accurate measurements in less than 30 seconds for full-band measurements or as little as less than one second for streamlined measurements.

Low Cost Phase Noise Measurement

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Introduction

Phase noise levels in receiver local oscillators limit the signal to noise ratio and adjacent channel rejection. For an FM system 50 dB of signal to noise is desirable. Noise power is integrated from noise density over the range of offset frequencies that pass through the IF. A 3 KHz IF bandwidth requires about -85 dBc/Hz phase noise at a 300 Hz offset. With test margin about -95 dBc/Hz is needed in the test system.

Adjacent channel rejection is noise density integrated over the IF bandwidth, at a one channel offset from the carrier. 90 dB of rejection requires an oscillator with -125 dBc/Hz phase noise and a test system capable of -135 dBc/Hz. Channel spacing can be 10 KHz.

Currently available spectrum analyzers do not have sufficient measurement range. To fill the need a few phase noise test systems are available in the $30,000 and up price range. They implement the phase detector method which will be described.

A low cost implementation is offered to make the measurements more widely available.

Phase Detector Method

The phase detector method allows a spectrum analyzer to make a phase noise measurement without viewing it's internal phase noise. The block diagram is shown in Figure 1.

Two signal sources are used with one being phase locked to the other. The phase locked loop shown is initially in an open loop state. One signal is frequency offset from the other. The difference frequency level is measured. Then the loop is connected. During phase lock the mixer IF port is at 0v DC with superimposed noise. RF and LO port signals will be separated in phase by 90° (See Figure 2). Noise output is viewed after it passes through the LNA. Phase noise at a particular offset is the level difference between the beat and noise output with correction factors.

Correction Factors

The reference beat note is usually measured with the LNA bypassed, to avoid overload. LNA gain must be subtracted from the noise level measured with it in circuit.

Mixing the signals down to DC folds one sideband's noise into the other. Sideband noise is in phase resulting in voltage addition. 6 dB is subtracted from the measured noise to account for folding.

If two equal phase noise sources are used, 3 dB is subtracted from noise measured. This accounts for power addition. If one source is much lower than the other, no correction is made.

Analog Spectrum Analyzers without noise markers need correction for the effective noise bandwidth of their resolution bandwidth filters, noise response of peak detectors and Log amplifiers. These should be in the manual. Being able to manually add in the correction factors makes many old Spectrum Analyzers suitable. They need to tune the range of offset frequencies of interest and have a resolution bandwidth 10-20% of the lowest noise offset. The HP 141T has been seen selling for $900.

If both signal generators are of equal phase noise and noise markers are used then:

$$P_{SSB} = P_N - P_B - G_{LNA} - 9dB$$

Note that P_{SSB} is single sideband noise relative to carrier, P_N is the noise level measured, P_B is power level of the beat and G_{LNA} is LNA gain.

If the reference generator has 10 dB lower noise than VCO under test then:

$$P_{SSB} = P_N - P_B - G_{LNA} - 6dB$$

A low noise generator is a convenience, to avoid having to optimize two VCO's or PLL's at the same time.

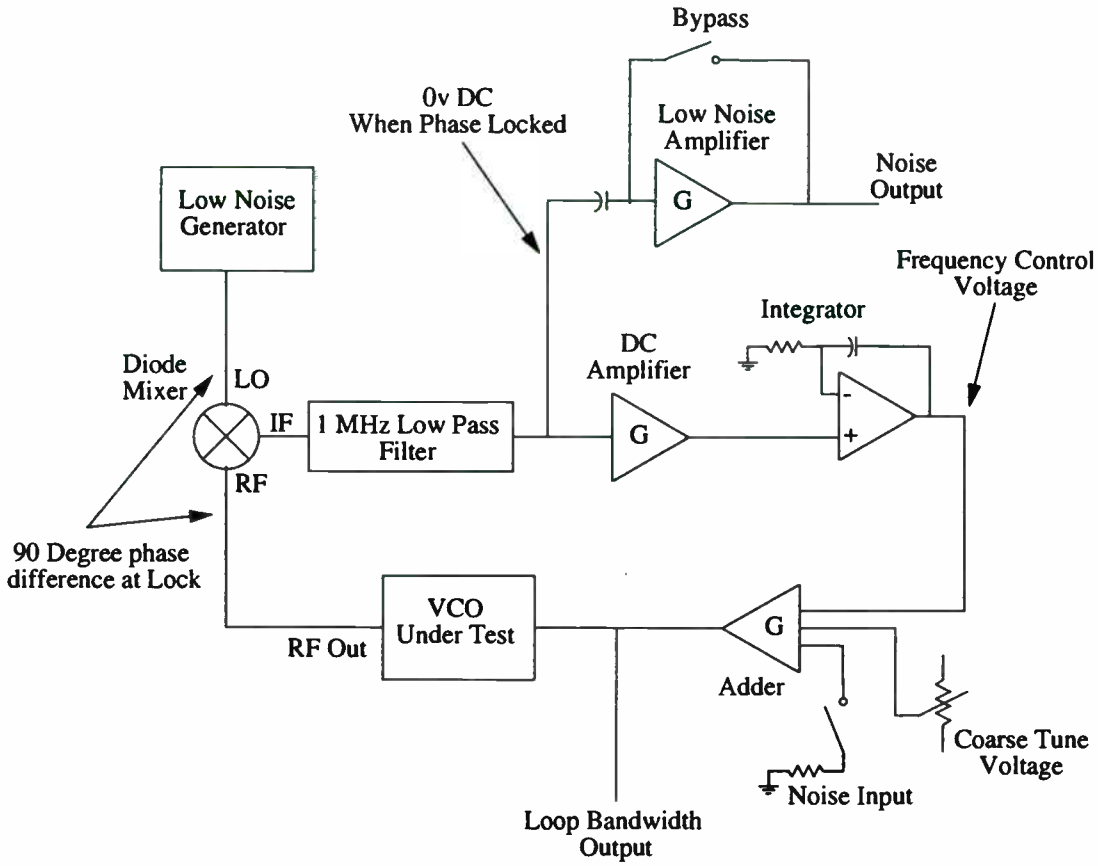

Figure 1. Phase Detector Noise Measurement

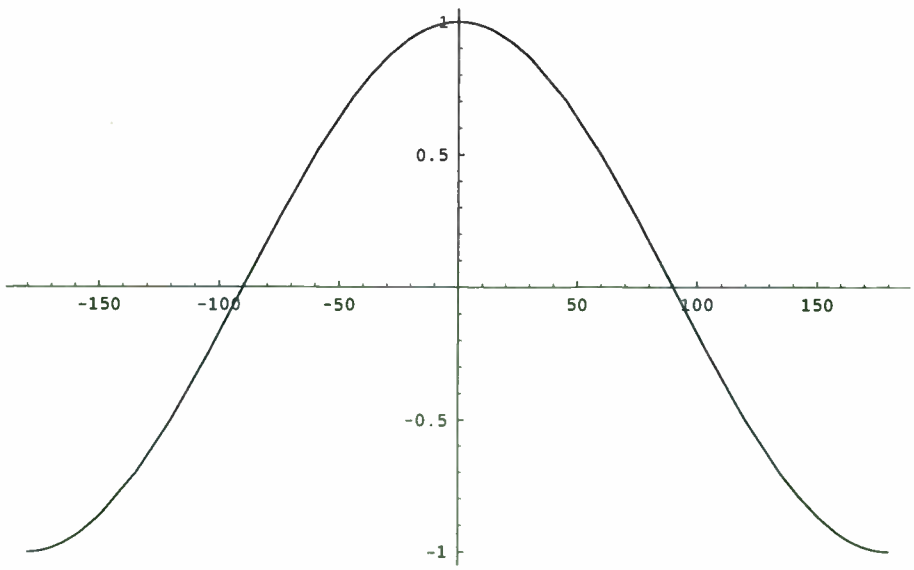

Figure 2. Mixer output Voltage vs. Phase Difference of Inputs

Beat Measurement

Accurate noise measurement by comparison to a beat power level depends on a beat's zero crossing slope reflecting the RMS value of a Sine wave. Zero crossing slope is the conversion factor between Radians of phase jitter and volts of noise output. Mixer output beat harmonics should be kept below -30 dB.

With highly distorted beat products, accurate measurements can be made by measuring zero crossing slope and knowing the sense of the loop. Loop sense is needed when the two zero crossing slopes are different (+/- 90°).

If the reference source is 10 dB or more below noise from the device under test, phase noise is:

$$P_{SSB} = 20\,\mathrm{Log}\left[\frac{V_N}{K_P\sqrt{B}}\right] - G_{LNA} - 6\mathrm{dB}$$

After phase lock, V_N is the RMS noise voltage at the desired offset, measured in the noise bandwidth B, with a mixer of phase slope K_P. Units of K_P are volts of output per radian of phase difference. Noise markers are corrected for a 1 Hz bandwidth (B=1).

Using two identical sources phase noise is:

$$P_{SSB} = 20\,\mathrm{Log}\left[\frac{V_N}{K_P\sqrt{B}}\right] - G_{LNA} - 9\mathrm{dB}$$

Small Angle Criteria

The V_N/K_P ratio is the RMS phase deviation of the carrier that occurs at the offset frequency rate. RMS phase deviation squared is the phase noise. The straight line approximation of K_P relies on the identity $\mathrm{Sin}\theta \cong \theta$ valid for small angles. Operating within +/-10 degrees of the zero crossing will keep error below 0.13 dB (1.5%) which is not significant. K_P is computed from a Oscilloscope trace.

Loop Bandwidth and Damping

Noise is suppressed within the loop bandwidth as shown in Figure 4. Without showing the intermediate steps and choosing the integrator time constant RC=1, the loop bandwidth is:

$$f = K_P G_L K_V$$

f is in Hertz, G_L is the loop gain in volts/volt and K_V is VCO sensitivity in Hz/volt.

Again with RC=1, the damping is:

$$\zeta = \sqrt{\frac{\pi K_P K_V G_L}{2}}$$

From the loop bandwidth and damping formulas, $\zeta = \sqrt{\frac{\pi f}{2}}$. and $\zeta \propto \sqrt{f}$. Damping is greater than one for all loop bandwidths 0.64 Hz and greater. System response to noise can be quickly viewed by injecting thermal noise at the adder as shown in Figure 1.

Dynamic Range

System dynamic range is the level difference between the beat and mixer, LNA noise floor with corrections. A +13 dBm LO and +7 dBm RF results in about +1 dBm at the IF beat. With thermal noise at -174 dBm/Hz and a perfect LNA the noise floor could be -181 dBc/Hz. Low noise op amps currently available would limit that to -173 dBc/Hz at 10 Hz and -179 dBc/Hz at 1 KHz.

Phase noise can be amplified sufficiently to overcome the internal noise of any spectrum analyzer. LNA compression level was set at +20 dBm. It is limited below the typical Spectrum Analyzer 1 watt protection level.

Line related sidebands (60 Hz) are present in any measurement. The spectrum analyzer used (HP 8563) requires suppression by greater than the LNA gain added plus 6 dB or 9 dB. It has a 0 to -100 dBm/Hz level range with 10 dB of input attenuation for 10 Hz to 600 Hz offsets. To see the ultimate system noise floor at 10 Hz, sidebands must be <-90 dB.

MC144048 EVK
Phase Noise Measurement System

A simple phase noise test system has been designed which implements the phase lock technique. It operates from 10 MHz to 2 GHz and measures noise in the 10 Hz to 1 MHz offset range. It has achieved -140 dbc/Hz at 10 Hz and -166 dBc/Hz at 10 KHz. Alternate units on the market offer a specified amplitude accuracy of +/- 2 dB, noise floor of -140 dBc/Hz at 10 Hz and -170 dBc/Hz at 10 KHz at prices of $27K to $40K.

The system was in it's prototype stage at the time of writing. It offers a series of loop gain settings, which vary loop bandwidth and an Oscilloscope output to monitor phase lock. Noise can be injected and loop bandwidth monitored. There are RF amplifiers and antenuators to adjust mixer RF and LO levels.

All voltage tuned oscillators and signal generators that tune with -1 to +10 volts can be phase locked. The board is due for release in the second quarter of 1997 at a price under $1,000.

Results

Table 1 shows a MC145191 EVK phase locked to a HP 8665B signal generator. The two approaches diverge up to 2 dB.

Offset Frequency	Phase Lock Method (dBc/Hz)	Direct Measurement (dBc/Hz)
100 Hz	-71.7	-69.5
1 KHz	-73.6	-73.4
10 KHz	-95.1	-93.4

Table 1. MC145191 EVK noise at 738 MHz

Table 2 was computed from two phase locked Motorola Saber 14.4 MHz TCXO's. Available from the Component Products Division, they are analog compensated (lack the spurs of digitally compensated TCXO's), small, hermetic, low cost and drain 2.5 mA from a 5v supply when the RF load is 1K//15pF. Specified stability is +/- 2 PPM over -30 to +85 C. Over -15 to +55 C they are typically +/- 0.3 PPM.

Offset Frequency	Phase Lock Method (dBc/Hz)
10 Hz	-91.0
100 Hz	-112.7
1 KHz	-138.3
10 KHz	-148.3

Table 2. Saber TCXO 14.4 MHz noise

Figure 3 shows display appearance when measuring the MC145191 EVK. The board was frequency controlled by voltage tuning it's TCXO (a Saber). For direct phase noise readout. the marker level can be offset.

Figure 4 is two Saber 14.4 MHz TCXO's phase locked. Thermal noise is injected at the adder input and viewed at the adder output. The frequency where the loop suppresses the noise -3 dB is 8 Hz. As loop gain increases loop bandwidth also increases.

Figure 5 shows a 10 Hz offset noise measurement on the TCXO's.

Figure 6 is an open loop beat product display. It shows the 2nd and 3rd harmonics are suppressed enough to calibrate with beat power rather than zero crossing slope.

The traditional Log frequency plot can be achieved with GPIB control of the spectrum analyzer to change the spans and compose the plot. Alternatively a computer plug in Analog to digital conversion board can avoid the spectrum analyzer entirely.

For those of us who already own a spectrum analyzer, the preferred solution is a firmware upgrade to sweep log frequency from 0 Hz, with selectable resolution bandwidths, multiple noise markers and level offset from the reference beat.

References

[1] Product Note 11729B-1, Phase Noise Characterization of Microwave Oscillators- Phase Detector Method, Hewlett Packard, March 1984.

[2] Jeff Hinderer, Crystal oscillator noise measurement notes, Wenzel Associates, 1992.

[3] Harold T. McAleer, A New Look at the Phased Locked Oscillator, IRE Proceedings, June 1959.

[4] Application Note 93-0002, PN-9000 Automated Phase Noise Measurement System, Comstron 1993.

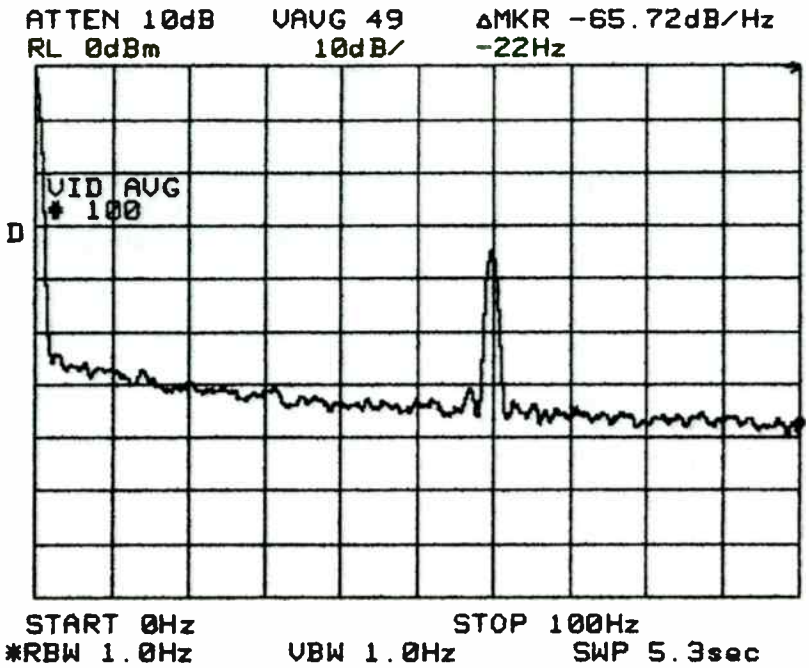

Figure 3. MC145191EVK Noise at 100 Hz offset, phase locked to HP 8665B. Phase Noise is -71.72 dBc/Hz, LNA not used.

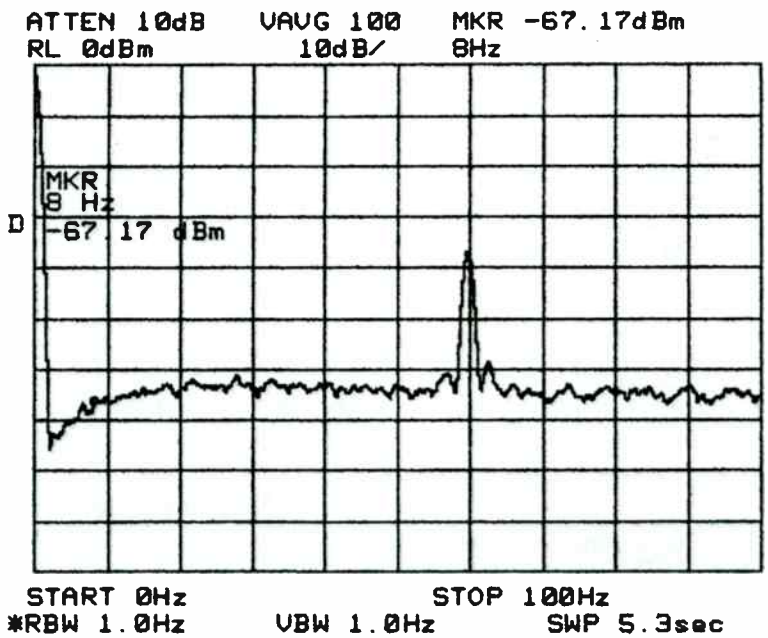

Figure 4. Motorola Saber 14.4 MHz TCXO Phase Locked with injected noise and viewing Loop Bandwidth (= 8Hz)

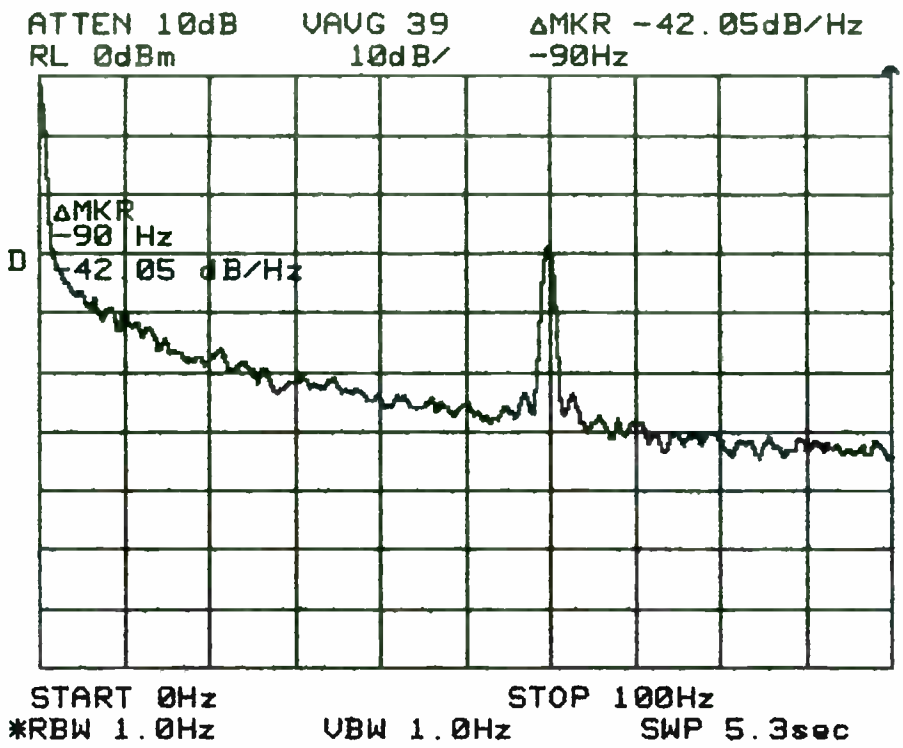

Figure 5. Two Saber TCXO's 14.4 MHz phase locked. Noise is referenced to a 100 Hz beat and passes through a 40 dB LNA. At 10 Hz offset noise is -91.0 dBc/Hz.

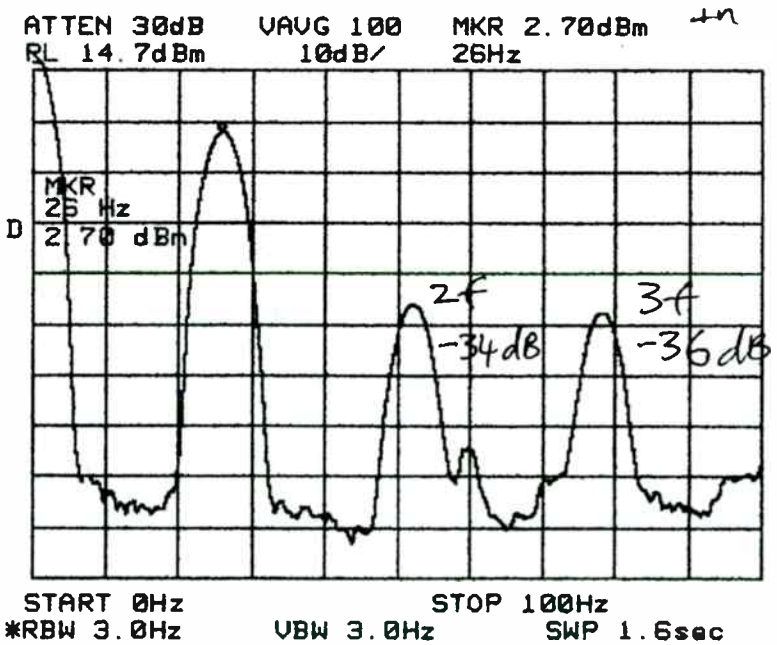

Figure 6. Two Saber TCXO's beat note at 26 Hz (+2.7 dBm) with LNA Bypassed. The LO level was +13 dBm and RF level +7 dBm. Second harmonic is -34 dB and 3rd is -36 dB.

Testing Low Power Spread Spectrum Radios for Compliance

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INTRODUCTION

In recent years an increasing number of frequency bands have been made available for use in unlicensed or consumer applications. This paper will discuss the tests called out by FCC's certification requirements for spread spectrum radios under Part 15, as well as those called out in prETS 300 328, the spread spectrum radio type approval test standard being adopted by the European Union (EU).

There are two basic types of spread spectrum modulation. Frequency hopping (FH) systems, as the name implies, vary the channel center frequency in a pseudorandom fashion. The dwell time at each hopping channel can also be varied in a pseudorandom manner.

Direct sequence (DS) systems, also known as CDMA or Code Division Multiple Access systems, use a multibit spreading sequence to spread the information bits over a wide frequency range.

The FCC allows both direct sequence and frequency hopping systems, as well as hybrids of the two systems, to operate under section 15.247 of Part 15 of the Rules.

Part 15 spread spectrum systems may operate in the following bands, at up to 1 watt power output:

902 - 928 MH
2400 - 2483.5 MH
5725 - 5850 MHz

TEST PROCEDURES

Transmitter RF Power Output Measurements (DS and FH)

Test Equipment Requirements

RF power meter
Spectrum analyzer
Receive antenna

For devices which have a coaxial antenna connector, power measurements are made by connecting a short length of the appropriate type cable between the device under test (DUT) and the power meter or the spectrum analyzer. Peak reading RF power meters have wide enough bandwidth to capture the emission bandwidth of the DUT; spectrum analyzers should be set to greater than the 6 dB bandwidth of the emission.

For channelized direct sequence spread spectrum systems, power measurements are required for a channel near the low end of the band, near the middle of the band, and near the high end of the band, in keeping with requirements listed in paragraph 15.31(m) of the Rules. For hopping frequency systems, the hop function must be disabled and measurements shall be made at a low, middle, and high frequency hopping channel.

If the system employs some type of pulsed or packeted output where the transmitter is turned on and off, this function should be disabled as well, or the peak reading meter will record artificially low levels.

If the DUT employs a permanently attached antenna, radiated tests may be used to show compliance with RF output power requirements (and other conducted measurements as well). The transmitter peak power can be calculated using the following equation:

$$E = \frac{\sqrt{30PG}}{d}$$

Where:

E = the maximum measured field strength in V/m using the widest available RBW

G = the numeric gain of the transmitting antenna over an isotropic radiator
d = the distance in meters from which field strength was measured
P = the power being solved:

$$P = \frac{(Ed)2}{30G}$$

Care must be taken to maximize received field strength, and RBW must be set to at least the 6 dB bandwidth of the emission, otherwise transmitter power calculations will be artificially low.

Occupied Bandwidth Measurements (DS and FH)

Test Equipment Requirements

Spectrum analyzer
Receive antenna

Section 15.247 calls out a 6 dB minimum bandwidth requirement for DS systems, and a 20 dB maximum bandwidth for FH systems. Testing is straight forward and easily done using spectrum analyzer DISPLAY LINE, PEAK SEARCH, and DELTA MARKER functions. Care should be taken in the choice of spectrum analyzer resolution bandwidth (RBW) since too large a bandwidth may include adjacent ambients and noise, especially when using the radiated measurement method for devices having fixed transmit antennas. Modulation should be on during this test, frequency hop functions off.

Hopping Channels, Separation, and Duration of Channel Occupancy (FH)

Test Equipment Requirements

Spectrum analyzer
Receive antenna

For either the radiated or the direct connect method of measurement, the spectrum analyzer START and STOP frequencies are set to the frequency endpoints of the band. The MAX HOLD function is activated after the transmitter starts its normal hop transmissions. The spectrum analyzer SWEEP TIME is chosen to be as fast as possible without causing measurements to go out of calibration. The transmitter is allowed to run for at least 2 minutes, and the resulting peaks on the stored spectrum analyzer trace can be counted for comparison with required minimums.

Minimum channel separation can also be determined from the stored trace. It may be necessary to break the spectrum into several sections and to make multiple spectrum analyzer graphs in order to be able to resolve the channels and the separation between them.

Hopping channel occupancy time can be measured using the ZERO SPAN function of the spectrum analyzer. The CENTER frequency is set to one of the hopping channels, the SWEEP TIME is set to 20 seconds or 30 seconds as appropriate. This will produce a time v. amplitude record, and using the DELTA MARKER function, total channel on time can be measured and compared to the 0.4 second maximum requirement.

Power Density (DS)

The spectrum analyzer CENTER is set to the frequency for which peak power is maximum. SPAN is set to 300 kHz around the peak. RBW and video bandwidth (VBW) are set to 3 kHz. Sweep time is set to 100 seconds (= 300 sec/3 kHz). The resultant sweep trace is a record of maximum peak power in any 3 kHz bandwidth, averaged over 1 second, which can be compared against the 8 dBm limit.

Note that this is different from what is implied by the wording of the rule paragraph, which seems to indicate power is measured with an average weighting meter. The wording is incorrect; FCC Laboratory personnel have confirmed this on numerous occasions. Hopefully the next published edition of the Rules (October 1996) will have an editorial change to clarify the meaning of this paragraph.

Processing Gain (DS)

Test Equipment

Signal generator
Power meter or Spectrum analyzer Communications analyzer (BER meter)

Processing gain for a DS system can be determined using the CW jamming margin method. The test consists of stepping the signal generator through the passband of the system in 50 kHz steps. The generator level required to produce the recommended bit error rate (BER) is recorded at each step. This is the "jammer" level. The DUT transmitter output level is measured at the same point. The Jammer to Signal (J/S) ratio is then calculated. After discarding the worst (lowest) 20% of the J/S data points, the lowest remaining J/S ratio is used to calculate the Processing Gain using the equation

$$Gp = (S/N)o + Mj + Lsys$$

where:

(S/N)o = the required signal to noise ration at the receiver output for a given received signal quality, i.e., for the chosen BER,

Mj = J/S ratio

Lsys = system losses, such as those due to non-optimal filtering, lack of equalization, LO phase noise, "corner cutting in digital processing", etc. Total losses in a system, including TX and RX, should be assumed no more than 2 dB.

Out of Band Emissions (DS and FH)

Test Equipment

Spectrum Analyzer
Antennas
Pre-amplifiers
High pass filters or band stop filters to attenuate transmitter fundamental
Low-loss microwave coax

Emissions in Restricted Bands

This one test accounts for almost all of the compliance failures experienced by spread spectrum radios. The restricted bands are listed in paragraph 15.205 of FCC's Rules, and must be met by all intentional radiators (i.e., transmitters) operating under Part 15. The test is a radiated emissions test, and for emissions above 960 MHz the radiated field strength limit is 54 dBuV/m at a 3 meter measurement distance. Harmonics of all three spread spectrum operating bands will fall in restricted bands, and there doesn't seem to be a practical way to select operating frequencies that will completely avoid them.

Because measurement system losses are high at microwave frequencies, pre-amplifiers are usually required to overcome the high receive antenna factors, cable losses, and spectrum analyzer noise floors. High pass filters are required at preamplifier inputs to prevent overload from the transmitter's fundamental frequency output.

Part 15 requires that measurements be performed up to the 10th harmonic of the fundamental or to 40 GHz, whichever is lower, and since suitable microwave preamplifiers may not be available, FCC allows measurements to be made at distances closer than 3 m. The results so obtained are compared to 3 m limits by using inverse linear extrapolation.

Harmonic microwave emissions from low power transmitters are usually highly directional in nature. The microwave horns used for receiving these emissions have very narrow receive lobes. This combination of factors means that it is easy to miss the search antenna azimuth and height at which the maximum field strength occurs. It is imperative that radiated emissions tests be performed slowly and carefully, and preferably at a measurement distance less than 3 meters .

The hopping function of FH systems and any transmitter duty cycle function must be disabled during this test. Radiated levels must be reported for both peak and average analyzer detector settings.

Spectrum analyzer RBW is 1 MHz for emissions above 1 GHz. For peak detector readings, VBW is greater or equal to 1 MHz. For average detector readings, RBW is also 1 MHz , but the VBW is reduced from 1 MHz to 10 Hz after the maximum peak reading is determined (by rotating the device, and raising and lowering the search antenna in both vertical and horizontal polarity). Duty cycle correction, if any, is then added to the resultant maximized emission for final calculation of average field strength.

Section 15.35(c) requires that duty cycle corrections be calculated by comparing TX on time to total pulse train duration, or if the transmitter is on for more than 0.1 seconds, TX on time is compared to 100 msec. For FH systems to take advantage of a duty cycle correction, it is usually necessary to show that maximum dwell time at any channel is less than 100 msec.

Emissions Not in Restricted Bands

For systems with coaxial antenna connectors, the transmitter output is directly coupled to the input of the spectrum analyzer, through suitable internal or external attenuators to prevent overloading the analyzer. RBW is set to 100 kHz, a display line is set to 20 dB below the peak transmitter output level, and frequency sweeps are made to the 10th harmonic of the fundamental frequency. All emissions must be below the display line, otherwise, radiated emissions tests are required to show that all emissions are below the levels specified in section 15.209(a) of the Rules. Radiated emissions measurements will also be required for devices with permanently attached antennas.

Table 1 FCC Part 15 Spread Spectrum Test Requirements Matrix

TEST	Rule Para.	FH 902 MHz 2.4/5.8GHz	DS 902 MHz 2.4/5.8GHz	REMARKS
Output power	15.247b	1 watt 1 watt	1 watt 1 watt	reduce power by X dB if TX ant gain =X + 6 dBi
DS 6 dB bandwidth	15.247a(2)	- n/a -	500 kHz 500 kHz	minimum BW
FH 20 dB bandwidth	15.247a(1)	500 kHz 1 MHz	- n/a -	maximum BW
Hop channel separation	15.247a(1)	greater 25 kHz or 20 dB BW	- n/a -	minimum separations
Hopping channels	15.247a(1)	50 minimum 75 minimum	- n/a -	
Ch.Time of Occupancy	15.247a(1)	0.4s in 20s 0.4s in 30s	- n/a -	
Power Density	15.247d	- n/a -	8 dBm in any 3 kHz BW	
Processing gain	15.247e	- n/a -	minimum 10 dB	FH/DS hybrids: 17 dB
Out of band emissions, in restricted bands	15.205	fe>960 MHz: 54 dBuV/m fe<960 MHz: see 15.209(a)	fe>960 MHz: 54 dBuV/m fe<960 MHz: see 15.209(a)	radiated measurements taken at 3m distance
Out of band emissions, not in restricted bands	15.247c	20 dBc, 100 kHz BW to 10fo or 40 GHz	20 dBc, 100 kHz BW to 10fo or 40 GHz	or to 15.209a levels, whichever is less atten.
AC line conducted	15.207	.450 - 30 MHz: 250 uV	.450 - 30 MHz: 250 uV	for devices obtaining power from AC or AC adapter
Receiver radiated emissions	15.109	see 15.109 n/a	see 15.109 n/a	required after 6/23/99
Receiver antenna conducted emissions	15.211	2.0 nW n/a	2.0 nW n/a	required after 6/23/99

TESTING 2.45 GHZ SPREAD SPECTRUM FOR EUROPEAN COMPLIANCE

The fifteen nations in the European Union (EU) are working towards removing trade barriers that exist among the member nations; a significant portion of this effort has been towards harmonizing compliance requirements in such areas as medical devices, safety, and EMC. For example, if manufacturer's product has been tested and shown to comply with the EMC Directive's requirements, the product may be imported into any of the EU countries because the national requirements for each of the member states have incorporated the same requirements, those found in 89/336/EEC, the EMC Directive.

Harmonization of the telecom regulations in Europe is also being pursued, much of the work being performed

by the European Telecommunications Standards Institute (ETSI), based in France. Low-power transmitter type approvals are still issued on a country by country basis, but some national authorities are reciprocally recognizing type examination of products performed in accordance with some of the ETSI standards. One of these standards is prETS 300 328 (June 1994), a draft standard for determining the

technical characteristics and test conditions for 2.4 GHz band spread spectrum radio products.

prETS 300 328 requirements differ from FCC Part 15 requirements in significant ways, although in many cases data and procedures used to qualify products for FCC can be used to demonstrate conformance with European requirements, summarized in Table 2 below:

Table 2 ETS 300 328 v FCC Part 15 Test Requirements

Test Parameter	**FCC Part 15**	**prETS 300 328**
Frequency range	902-928/2400-2483.5/5725-5850 MHz	2400-2500 MHz
Maximum output power	1 watt (with 6 dBi ant. = 4 watts e.i.r.p.)	100 mW e.i.r.p.
FHSS hopping channels, min	75	20
FH SS channel 20 dB bandwidth	1 MHz	- not specified -
Hopping channel separation	greater than 25 kHz or 20 dB BW	20 dB BW
Dwell time	0.4s in 30 s	0.4s in 32 s *
Peak Power Density, FHSS	n/a	100 mW/100 kHz
Peak Power Density, DSSS	8 dBm/3 kHz (6.3 mW/3 kHz)	10 mW/1 MHz
Processing Gain	10 dB min, DSSS	- not specified -
Out of Band Emissions	- 20 dBc non-restricted bands Restricted bands: 30-88 MHz 40 dBuV/m @ 3m 88-216 MHz 43.5 dBuV/m @ 3m 216-960 MHz 46 dBuV/m @ 3m Above 960 MHz 54 dbuV/m @ 3m	30-1000 MHz -36 dBm (250 nW) 41-68 MHz -54 dBm 87.5 -118 MHz -54 dBm 162-230 MHz -54 dBm 470-862 MHz -54 dBm 890-960 MHz -56/-36 dBm** 1.8-1.9 GHz -56/-30 dBm** 5.15-5.3 GHz -56/-30 dBm** 1-12.75 GHz -30 dBm
Receiver Spurious Emissions	no requirement for fo> 960 MHz	30-1000 MHz -57 dBm 1 - 12.75 GHz -47 dBm

* Standard states, "each channel of the hopping sequence shall be occupied least once during the period not exceeding four times the product of the dwell time per hop and the number of channels". For maximum dwell time and minimum channel numbers, 4 x .4 x 20 = 32

** Less stringent limit for narrowband signals

The preferred method of testing for power, power density, frequency range, and occupied band width is by conducted rather than radiated measurements. For devices with permanently attached antennas, the standard requires two samples be submitted for testing, one with the antenna attached, the other with a test cable and coaxial connector wired to where the antenna would normally be attached. Radiated spurious and out of band case radiated emissions from transmitters and receivers are defined as power levels determined by signal substitution methods, whereas FCC specifies field strength limits.

Other significant differences between prETS 300 328 and Part 15 methodologies are the ETSI standard requires measurements to be made at extremes of temperature and supply voltage, and for radios mounted on cards or removabie I/O boards, tests on three

different hosts are required to be made. FCC measurements are done at 20 °C and at nominal supply voltage, and testing with one representative host will almost always be adequate to qualify a radio built on an I/O board or card.

In addition to radio type approval issues, radio devices, like almost every other kind of electronic device, are subject to the requirements of the EMC Directive in each of the EU countries. Immunity as well as emissions are addressed by the Directive. ETSI has developed a standard for generic electromagnetic compatibility for radio equipment, prETS 300 339, which is based on generic emissions standard EN 50081-1, generic immunity standard EN50082-1, and other immunity standards where appropriate.

GENERAL COMMENTS and SUGGESTIONS

Spend the money. High quality cables, connectors, antennas and preamplifiers used at microwave frequencies are expensive but necessary to overcome inherent system losses encountered when measuring low level signals.

Go slowly. Microwave emissions are very directional, the receive antenna lobes are narrow, and emission levels are often quite near the noise floors of the measuring equipment. It is easy to miss a significant emission if testing is performed too quickly.

Read all the rules. Spread spectrum devices are subject to all the other requirements listed in Part 15, unless specifically excluded. Information concerning such subjects as measurement instrumentation settings, radiated emissions measurement distances, measurement frequency ranges, etc., may not be listed in section 15.247, nor are they necessarily cross-referenced.

Shop around. When looking for a contract test laboratory, be sure the facility has available the high quality cables, amplifiers, high pass filters, and other specialized equipment required. There are many EMC laboratories on file with FCC, but most are limited in equipment and expertise to measurements below 1 or 2 GHz.

Be prepared. If your company or contract test lab has submitted spread spectrum applications to FCC in the past, there is about a one in five chance the next application will be targeted for pre-grant sample testing. For first-time submitters, the chance increases to near certainty.

References

(1) Code of Federal Regulations, Title 47, Parts 0 - 19 (October 1995)

(2) prETS 300 328, "Radio Equipment and Systems (RES); Wideband data transmission systems, Technical characteristics and test conditions for data transmission equipment operating in the 2.4 GHz ISM band and using spread spectrum modulation techniques", European Telecommunications Standards Institute, 1994

(3) Guidance on Measurements for Direct Sequence Spread Spectrum Systems, FCC Authorization and Evaluation Division, Columbia, MD

(4) Dixon, Robert C. Spread Spectrum Systems, Second Edition, John Wiley & Sons, 1984

While the wireless industry is experiencing phenomenal growth, several wireless technologies are competing for global acceptance into the cellular and PCS marketplace. CDMA is one emerging technology that promises major advantages over competing systems. To ensure properly designed systems, CDMA wireless communications equipment must be designed to meet performance requirements of recently introduced test specifications.

CDMA test specifications require emulation of radio frequency propagation, carrier-to-noise, and carrier-to-interference conditions. Test systems that implement these specifications most provide accurate emulation and additional functions such as system control and configuration, RF power measurements, and level control. In the past, a complete CDMA test system emulating the wireless channel has required an extensive rack of many instruments. Aside from the obvious cost implications, such multiple instrument solutions also present control and calibration challenges.

This paper provides an overview of the CDMA testing standards. A description of the various test requirements and the necessary test equipment for evaluating the performance of CDMA receivers will be provided. In addition, an integrated system solution for evaluating CDMA base and mobile station equipment will be presented.

CDMA TEST SPECIFICATIONS

With the expansion of the CDMA wireless market, there are several different testing standards emerging for cellular and PCS base and mobile equipment. Within these standards are definitions, methods of measurement, and minimum performance requirements. In addition to these standards, there are also documents that define interoperability testing. Table 1 lists the applicable CDMA testing documents.

Document Number	Document Title
TIA/EIA IS-98A	Recommended Minimum Performance Standards for Dual-Mode Wideband Spread Spectrum Cellular Mobile Stations
TIA/EIA IS-97A	Recommended Minimum Performance Standards for Base Stations Supporting Dual-Mode Wideband Spread Spectrum Cellular Mobile Stations
ANSI J-STD-018	Recommended Minimum Performance Requirements for 1.8 to 2.0 GHz Code Division Multiple Access (CDMA) Personal Stations
ANSI J-STD-019	Recommended Minimum Performance Requirements for Base Stations Supporting 1.8 to 2.0 GHz Code Division Multiple Access (CDMA) Personal Stations
CDG REF 22A	Stage 2 Cellular Interoperability Tests
CDG REF 22B	Stage 2 PCS Interoperability Tests

Table 1. CDMA Testing Documents

These test specifications can be grouped into three categories:

- Mobile Station Test Standards
- Base Station Test Standards
- Interoperability Test Standards

The IS-98A and J-STD-018 are both standards for evaluating mobile station performance. Similarly, IS-97A and J-STD-019 are standards for evaluating base station performance. The CDG REF22A and REF22B specifications define interoperability testing between CDMA infrastructure and mobile equipment. The major difference between each pair of documents is that one is defined for cellular while the other is defined for PCS.

TEST EQUIPMENT REQUIREMENTS

All the CDMA testing standards defined above require evaluation of the receiver performance under realistic, controllable RF channel conditions. The RF channel models defined in these specifications require emulation of RF propagation, carrier-to-noise, and carrier-to-interference characteristics. The standards also define the methodology and the setups required for each test.

Although each standard is unique, a generic list of test equipment can be derived from the specifications. The list of required equipment for evaluating the performance of CDMA communications equipment is as follows:

- Base or Mobile Station Emulator
- Fading Emulators
- Additive White Gaussian Noise (AWGN) Generators
- Signal Generators
- Power Meters
- Calibrated Attenuators
- Cabling, Splitters, and Combiners

With the exception of the base or mobile station emulator, it is important to note that the standards require multiple quantities of the equipment listed above.

TESTING ISSUES

Wireless system engineers face several challenges when testing and evaluating CDMA products. Two of the foremost problems presented are:

- Designing an accurate and repeatable test bench.
- Ensuring their product meets performance requirements stated in industry standards.

Today's complex digital transmission technologies, such as CDMA, attempt to squeeze every drop of performance and capacity out of the wireless network. In these scenarios, a fraction of a dB margin on the signal to noise performance ratio can make or break communication performance. Because of this small margin for error, laboratory performance testing must be accurate and repeatable.

To gain a better understanding of some of the other issues associated with testing, lets examine one of the test setups from standards. Figure 1 depicts a test setup specified in IS-97A and J-STD-019 for evaluating CDMA base station performance. In this particular test, the performance of the demodulation of the reverse traffic channel in a multi-path environment is determined by the frame error rate (FER) at specified values for E_b/N_0.

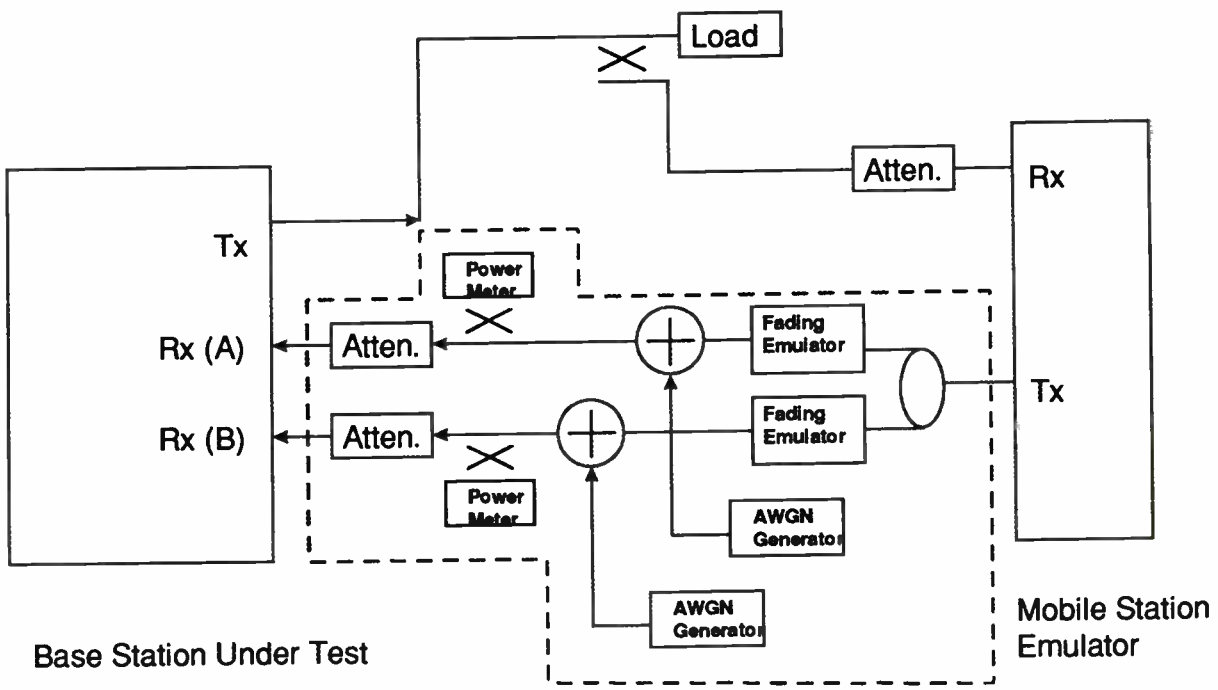


Figure 1. CDMA Base Station Test Setup

The output from the mobile station emulator is split before being transmitted through the fading emulators and are summed with AWGN. The signals are then coupled through calibrated attenuators and then connected to the diversity ports on the base station receiver.

For each base station test, the configuration of impairments in the area outlined in Figure 1 will vary. Depending on the specifics of the tests, the channel model will change requiring different test equipment. This same statement also holds true for mobile station testing.

INTEGRATED SYSTEM SOLUTION

In the past, a complete CDMA test system required racks of equipment to emulate the RF propagation, carrier-to-noise, and carrier-to-interference characteristics. To simplify the testing process, TAS has engineered an integrated system for evaluating CDMA base and mobile station equipment.

The TAS CDMA-LAB™ test system combines all the elements required by the cellular and PCS test specifications into one integrated system, shown in Figure 2. CDMA-LAB works with a base station or mobile station equipment or emulators to provide a complete, end-to-end test solution.

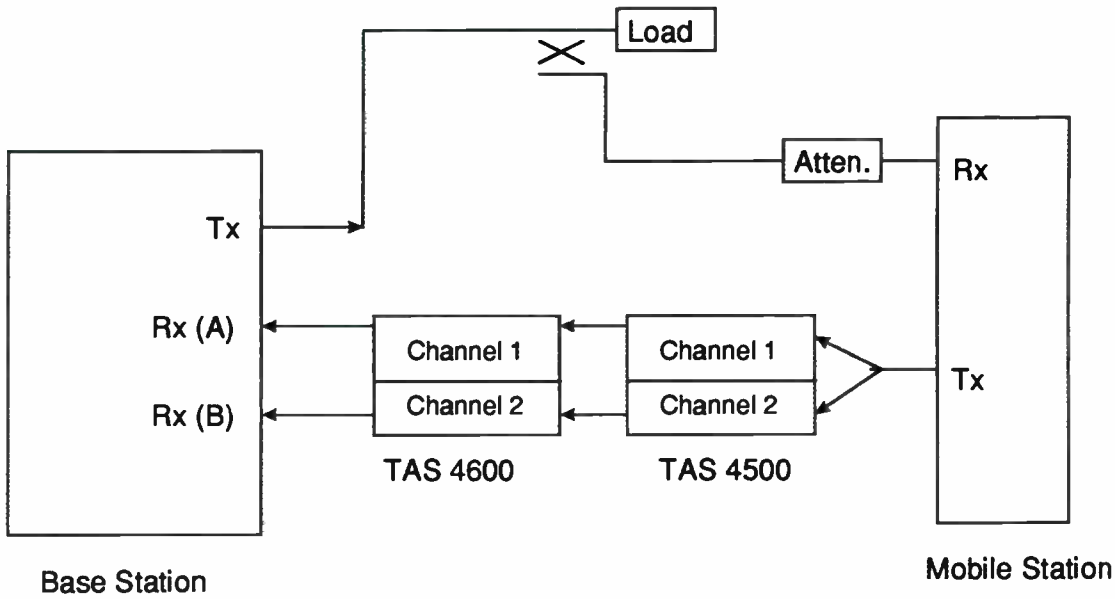


Figure 2. TAS CDMA-LAB

CDMA-LAB is the most powerful, integrated solution for CDMA base and mobile testing. In addition to implementing all the channel conditions required by the standards, it drastically reduces the number of instruments and interconnections required for comprehensive testing. CDMA-LAB consists of a single TAS 4600 and a single TAS 4500 controlled via Windows test application software.

The TAS 4500 FLEX4™ RF Channel Emulator is a precision instrument that emulates the characteristics of RF communication channels. FLEX4 provides accurate and repeatable emulation of all RF channel characteristics, including:

- Multi-Path Fading
- Log-Normal (terrain-induced) fading
- Delay Spread
- Path Loss

The TAS 4500 comes equipped with up to two independent RF channels that supports up to twelve paths in a single enclosure. A block diagram of single channel is shown in Figure 3. The system features built-in local oscillators used for the signal translation. For each path, independent control of delay, modulation, path loss, and terrain fading is provided.

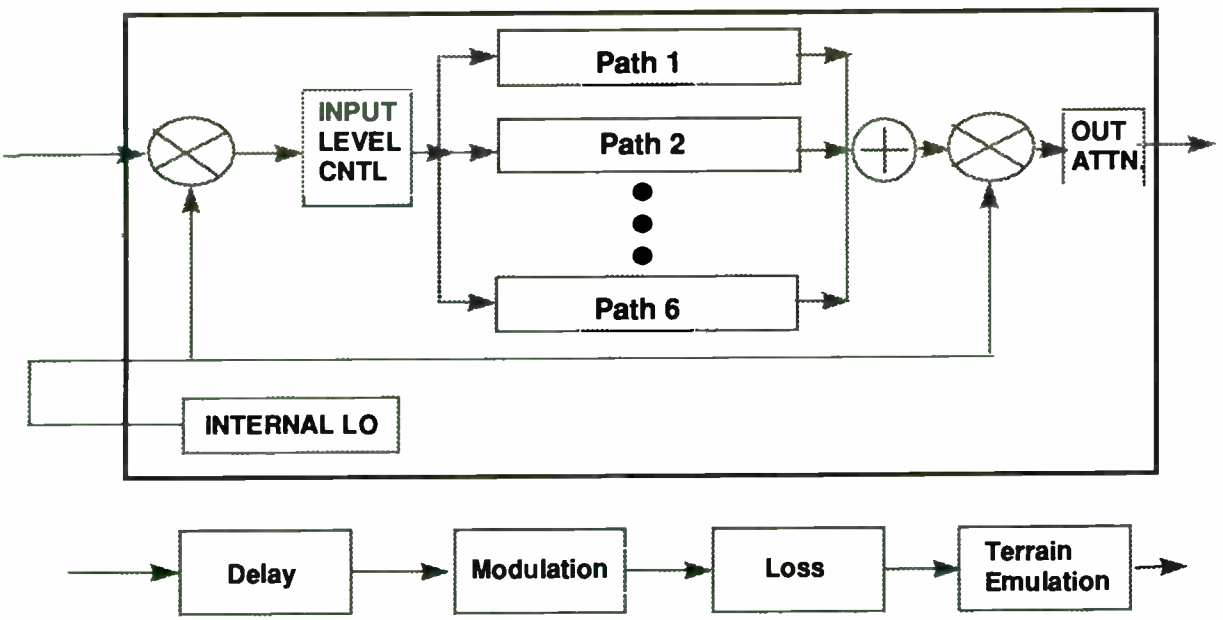


Figure 3. TAS 4500 Functional Diagram (1 Channel)

The next instrument in the TAS CDMA-LAB system is the TAS 4600 Noise and Interference Emulator. The TAS 4600 emulates the co-channel and adjacent channel interference present in wideband communications systems. The 4600 is a complete solution for precision noise, carrier-to-noise, and carrier-to-interference tests.

The 4600 provides two independent wide bandwidth RF channels, each with independent additive interference, in a single instrument. Each channel provides the capability to impair the user's carrier signal over a wide range of carrier-to-noise (C/N), carrier-to-interferer (C/I), or energy-per-bit-to-noise-density (E_b/N_0) ratios. A block diagram of the system architecture is shown in Figure 4.

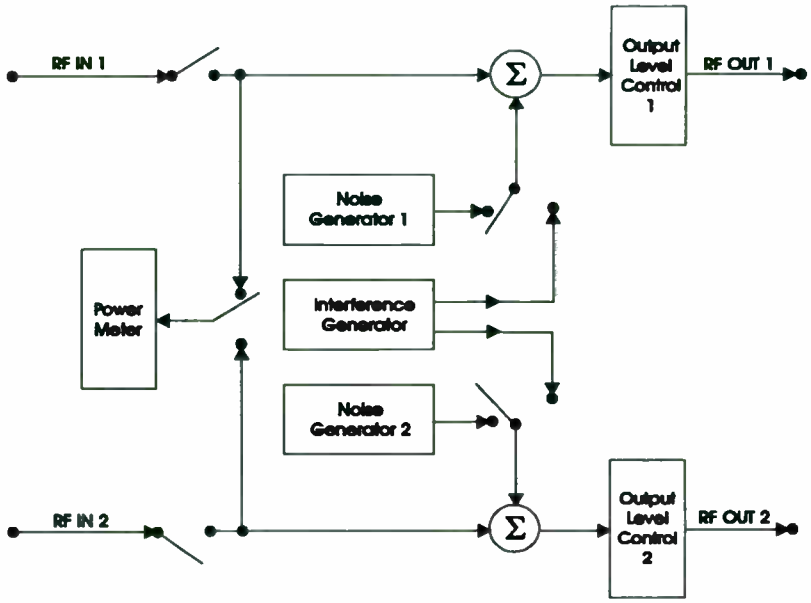


Figure 4. TAS 4600 Block Diagram

Inside the TAS 4600, the user carrier signal is combined with a programmable level of noise or interference. The 4600 utilizes an instrumentation-grade power meter for setting exact carrier to noise ratios. After the carrier signal is summed with noise or interference, the composite impaired signal is scaled to meet the user's desired output level.

Testing in the presence of Additive White Gaussian Noise (AWGN) and CW interference is often performed at low carrier receive signal power, typically at levels well below -70 dBm. The 4600 eliminates the need for racks of programmable attenuators by allowing the user to directly program the level of impaired carrier signal down to -130 dBm with 0.1 dB resolution.

TASKIT® for Windows software, shown in Figure 5, provides powerful, easy-to-use access to all TAS 4500 and TAS 4600 features. In addition, simple front panel controls provide a quick alternative to Windows PC control. The system includes industry standard test conditions to get you up and running immediately. GPIB and RS-232 remote control interfaces are standard and each instruments offers an easy-to-use, high level command set.

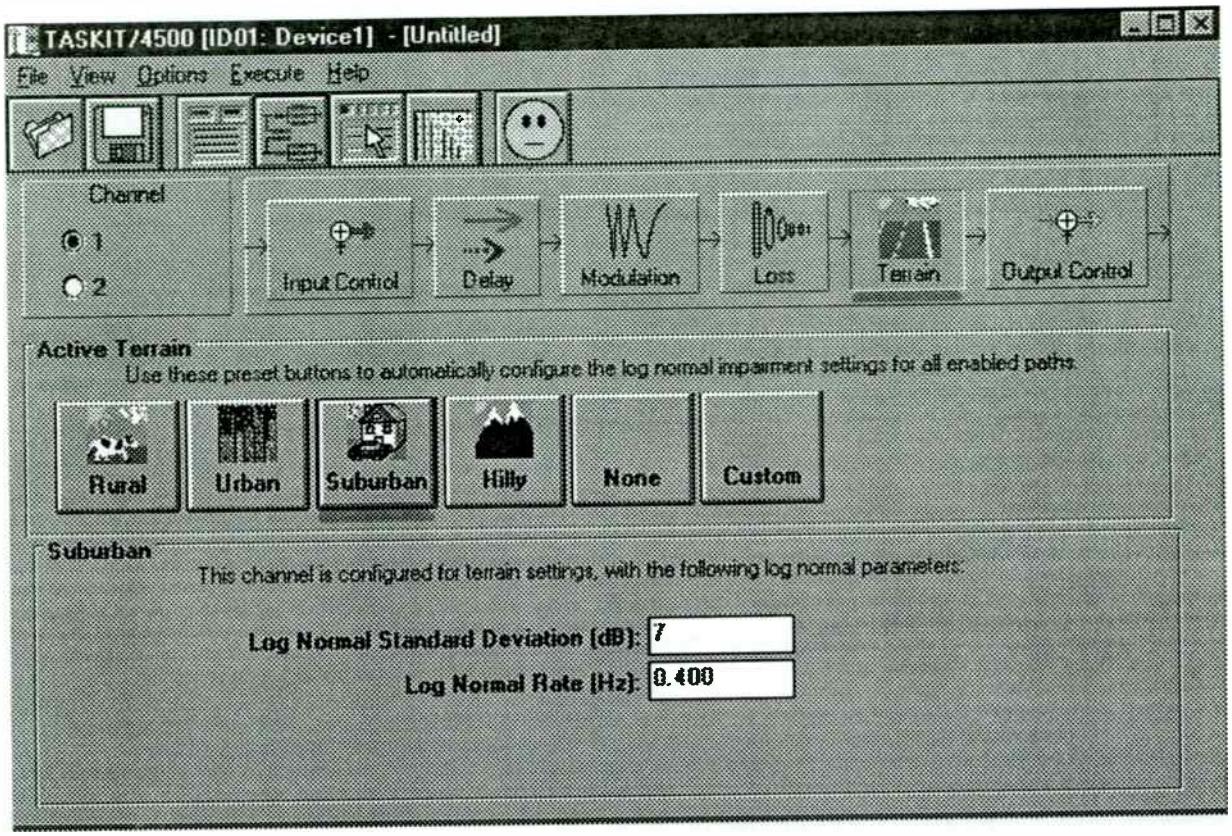


Figure 5. TASKIT Control Software

The modular architecture of the TAS 4500 and TAS 4600 ensures cost-effective testing as a customer's requirements evolve. Each of these instruments can be ordered in a variety of configurations to meet specific application requirements.

SUMMARY

There are several standards that define test procedures for CDMA wireless communications products. With standards defined for cellular and PCS bands, test systems must be designed to meet these requirements in both frequency bands. Fortunately, CDMA-LAB from TAS addresses these need.

Wireless system engineers face several challenges when designing or evaluating CDMA wireless communications products. Designing an accurate and repeatable test bench had been one problem. With the test system presented in this paper, engineers can ensure their product meets performance requirements stated in industry standards and not worry about their test setup.

In addition to testing CDMA base and mobile station equipment, the test systems described in this paper can be applied to testing a wide variety of wireless data communication equipment.

Characterization of Peak Factor Effects and Intermodulation Distortion (IMD) in Multi-carrier Communications Systems

Thomas D. Marra
RDL, Inc.

Abstract

Systems transmitting or receiving more than two carriers are subject to unpredictable variations in peak factor and IMD performance as a result of uncontrolled carrier phases. This problem is compounded in systems using fiber-optic transmission networks due to the hard clipping that occurs in laser diodes during peak power events. Phase-controlled multi-carrier signal generators provide the means to evaluate system components under controlled conditions, using a precisely controllable peak power factor. Applications for cellular, PCS, CDMA, and CATV testing will be discussed.

Introduction

A multi-tone signal is defined as a combined waveform consisting of two or more carriers. Mathematically, a multi-tone signal can be represented as:

$$v(t) = \sum_{i=1}^{N} \cos[\omega_i * t + \theta_i]$$

where N is the number of sinusoidal signals combined to form v(t), ω_i are the frequencies of the individual sinusoids, and θ_i are the corresponding phases. The relationship of the individual phases, θ_i, determines the characteristic of v(t) for a given set of equally spaced frequencies ω_i. For example, if N=4 and all four phases, θ_1, θ_2, θ_3, and θ_4 are equal to zero then four equally frequency spaced sinusoids forming v(t) would be as shown in Figure 1.

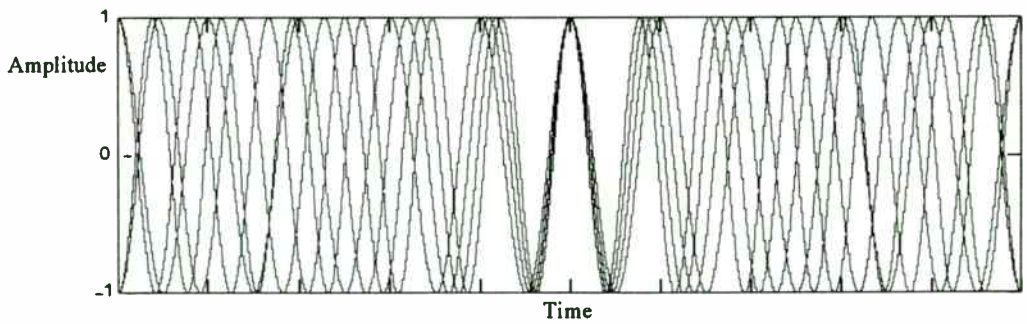


Figure 1. Four sinusoidal signals, zero phase.

The case of zero phase carriers is also called the phase aligned case. The combined waveform, v(t), for the phase aligned carriers is shown in Figure 2. As can be seen, with zero phases the sinusoids constructively add creating "peaks" in the combined waveform at the points where the individual sinusoids are simultaneously equal to 1. Note, the frequency spacing of the multiple tones in the above example is 10% of the sinusoid center frequency. This was done to observe more clearly the peaking effect for phase aligned carriers. For typical wireless systems, the frequency spacing would be much smaller (on the order of 0.01% or less).

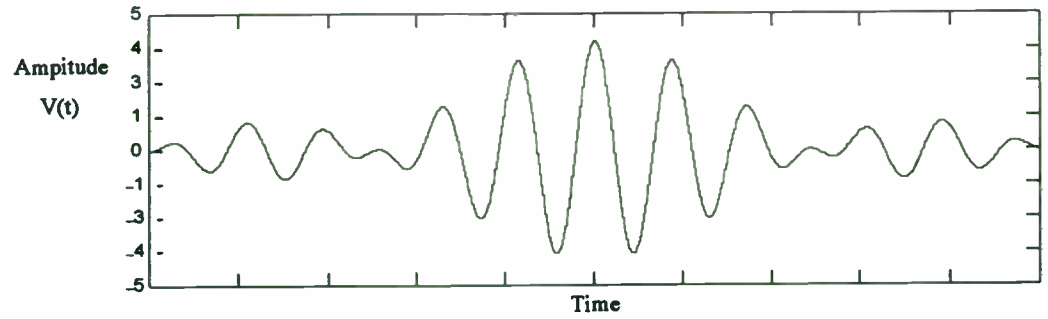


Figure 2. Combined waveform of four sinusoids, zero phase.

If the phases of the four sinusoids are random, then the four individual sinusoids may have the relationship shown in Figure 3.

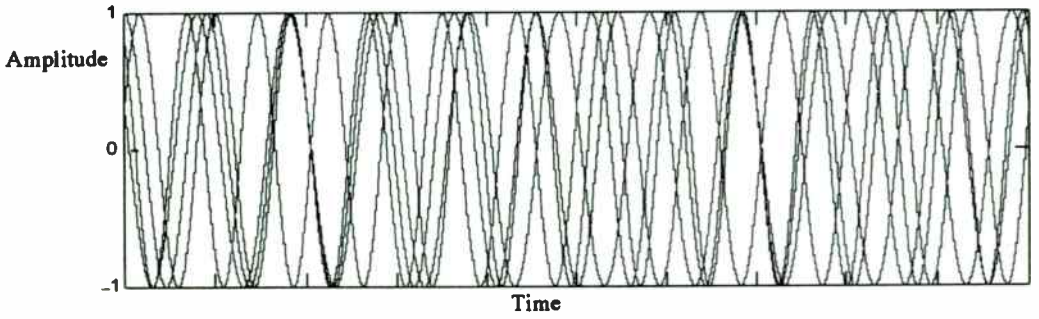


Figure 3. Four sinusoidal signals, random phase.

The corresponding combined waveform is shown in Figure 4.

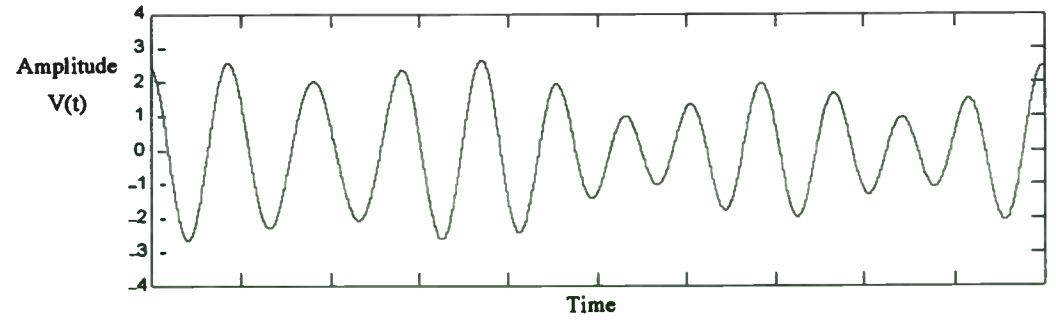


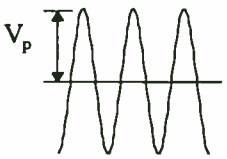
Figure 4. Combined waveform of four sinusoids, random phase.

Hence, the combined waveform has an amplitude that is more evenly distributed versus time and does not exhibit the peaking seen for the zero phase case. It is also worth noting that both of the above two cases would appear identical on a spectrum analyzer and would have the same average power.

Peak-to-Average Power Ratio

In order to characterize multi-tone waveforms, the concept of peak-to-average power ratio will be introduced. The true rms average power or envelope power of a single sinusoidal carrier is

$$P_{env} = \frac{\left[\frac{V_p}{\sqrt{2}}\right]^2}{R}$$



where V_p is the voltage amplitude of the sinusoidal signal and R is the resistance of the load that the sinusoid is driving. The power level P_{env} is the average power dissipation of the sinusoid and is equal to the power dissipation of a constant DC voltage of $V_{rms} = V_p/\sqrt{2}$ which is the rms voltage of the sinusoid.

For a multi-tone waveform, the envelope power fluctuates as a function time. This is seen in Figures 2 and 4 above. The average envelope power is the sum of the envelope powers of the individual carriers. For N carriers of equal amplitude, the average envelope power is

$$average\ envelope\ power = P_{avg-env} = N * P_{env}$$

where P_{env} is the envelope power of each carrier. Therefore, both of the multi-tone cases described above, zero phase and random phase, have the same average envelope power.

The peak envelope power is the maximum value of the envelope power of the multi-tone waveform. The peak-to-average power ratio is simply the ratio of the peak envelope power to the average envelope power. The peak-to-average power ratio is also called the peak factor. Hence, the peak factor indicates the amount of peaking that occurs in the power envelope of the multi-tone signal. In general, the peak factor of a multi-tone signal is

$$peak\ \ factor = 10\log\left[\frac{P_{peak-env}}{P_{avg-env}}\right] dB$$

where $P_{peak\text{-}env}$ is the peak envelope power and $P_{avg\text{-}env}$ is the average envelope power.

The peak envelope power, and therefore the peak factor, will be directly affected by the phase relationship of the sinusoids forming the waveform. The worst case peak factor for a given number N of carriers occurs in the phase aligned case since the peak envelope power is at its maximum value. Any other arrangement of carrier phases will result in a peak factor that is less than the phase aligned case.

For a given number N of carriers, the peak factor will vary depending upon the phases of the N carriers. If the phases have a uniform random distribution, the resulting peak factor will have a random distribution also. Figure 5 shows a histogram of peak factor distributions of an 8 tone signal with randomly distributed carrier phases. The carrier phases are uniformly distributed from 0 to 360 degrees and 10,000 trials computed. The results of this analysis indicate that the peak factor will be distributed between 2 and 9 dB with 58% of the occurrences between 4.5 and 6 dB. A peak factor of 9 dB corresponds to the phase aligned case and was observed once in the 10,000 trials.

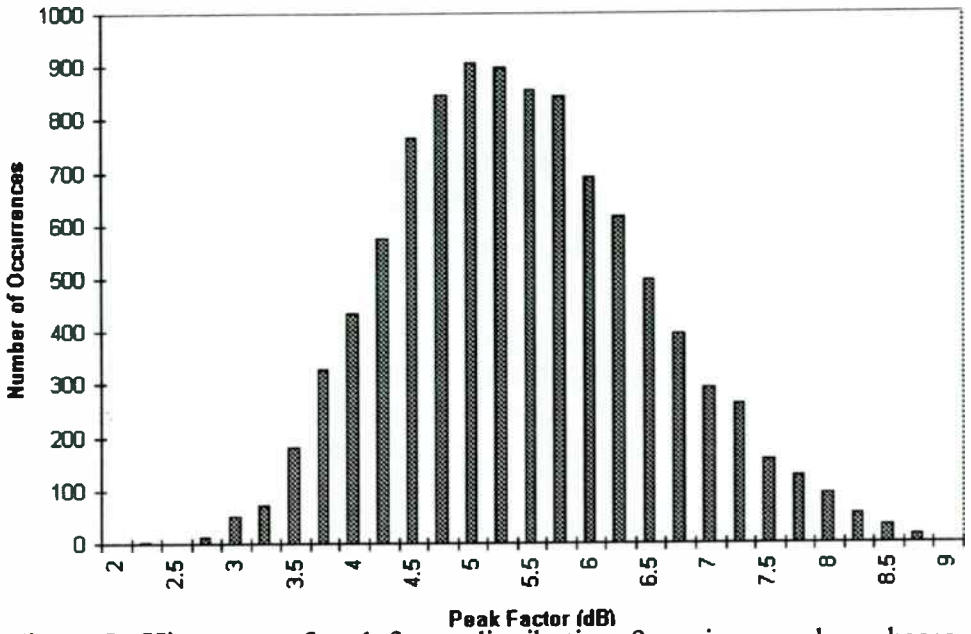


Figure 5. Histogram of peak factor distribution, 8 carriers, random phases.

In the zero phase case, the voltage peak of the waveform is at the maximum value attainable for N tones since the voltage peak for the individual N tones are in alignment. The peak envelope power for the phase aligned case is given by

$$peak\ envelope\ power\ (phase\ aligned) = P_{peak-env(pa)} = \frac{\left[\frac{N * V_p}{\sqrt{2}}\right]^2}{R}$$

The peak factor of a phase aligned multi-carrier waveform is therefore

$$peak\ factor_{(pa)} = \frac{P_{peak-env(pa)}}{P_{avg-env}} = \frac{\frac{\left[\frac{N * V_p}{\sqrt{2}}\right]^2}{R}}{N * P_{env}} = \frac{\frac{\left[\frac{N * V_p}{\sqrt{2}}\right]^2}{R}}{\frac{\left[\frac{V_p}{\sqrt{2}}\right]^2}{R}} = N$$

where N is the number of phase aligned sinusoids combined to form the multi-tone waveform. In decibels, the peak factor of a phase aligned multi-carrier waveform is

$$\text{peak factor}_{(pa)} = 10\log(N)\ \text{dB}$$

A plot of peak factor versus N, the number of phase aligned carriers, is shown in Figure 6. From this figure it can be seen that for 8 phase aligned carriers the peak factor is 9 dB and for 100 phase aligned carriers the peak factor is 20 dB.

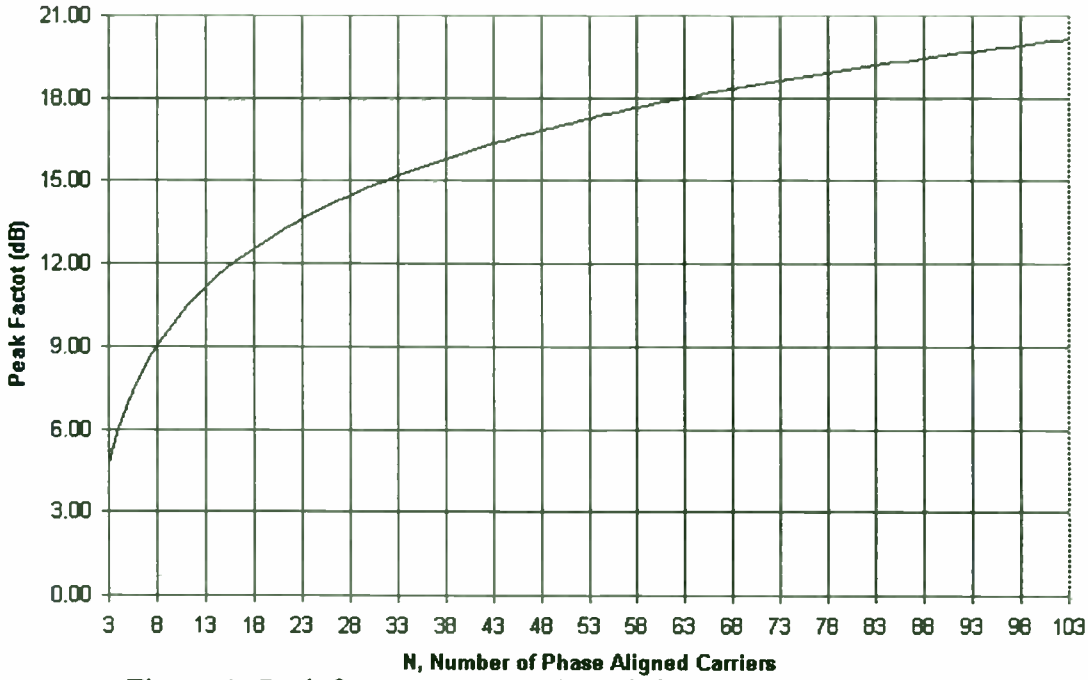


Figure 6. Peak factor versus number of phase aligned carriers.

The Effects of Peak Factor on System Performance

Peaking in the power envelope of a multi-tone signal can has various effects upon system performance. For example, RF amplifiers are subject to intermodulation distortion (IMD) products when operating in saturation. This occurs when multiple carriers mix within the amplifier due to the nonlinear operation of the amplifier in saturation. IMD products are interference to adjacent channels in a multi-channel system and therefore degrade system performance. A multi-tone signal with an average power that results in linear operation of an amplifier may or may not produce IMD products on the amplifier output depending upon the peak factor of the signal. The higher the peak factor, the larger the peak power is above the average power. The peak power peaks may drive the amplifier into its nonlinear operation and corresponding produce IMD products. The relative phase alignment of the tones forming the multi-tone signal will determine the peak factor and the amplitude of the power peaks. The worst case IMD products will be generated when a phase aligned multi-tone signal is used for the measurement. This effect of IMD products is present in both cellular and CATV amplifiers due to the multi-tone signals amplified by these amplifiers.

In a Hybrid Fiber-Coax (HFC) system using both analog and digital transmission techniques, the effects of high peak factors can be worse than in an analog only system. In an HFC system, peaking in the envelope power may cause clipping to occur in the laser operation. This clipping may cause BER thresholds to be exceeded resulting in a momentary loss of the transmission channel. The other primary difference between analog and HFC systems is that analog systems exhibit soft (2nd, 3rd order) nonlinearities whereas clipping in HFC systems produces higher order nonlinearities. This can result in even more variation in IMD products in response to uncontrolled carrier phases.

Multi-tone Signal Generator Testing

Phase-controlled multi-tone signal generators provide the means to evaluate system components using a precisely controllable peak factor. A signal generator capable of phase aligning of multiple carriers can be used to test at the worst case condition for a multi-tone signal, i.e., with maximum peak factor. In addition, with control over the carrier phases any peak factor can be selected up to the maximum peak factor. This provides additional flexibility for testing at peak factors below the maximum peak factor. Controllable carrier phases also provide a means for performing repeatable multi-tone testing. Multi-tone signal generators with no carrier phase control will have a random peak factor as shown in Figure 5. Measurements and testing performed with a multi-tone signal generator without peak factor control will produce dubious test data at best. Figure 7 shows a block diagram of the RDL IMD Simulator which is a phased-controlled multi-tone signal generator.

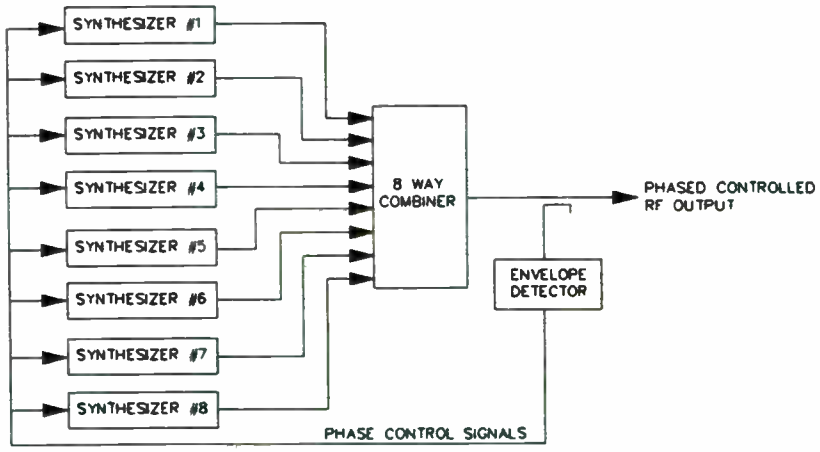
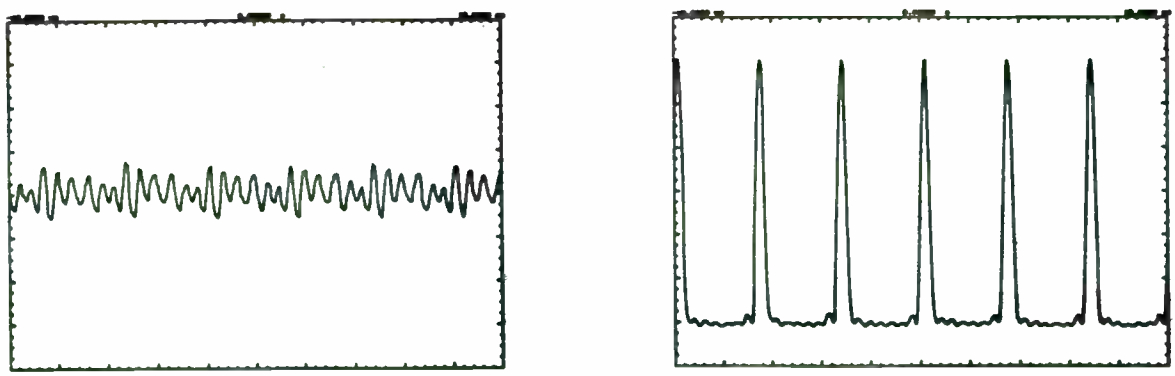


Figure 7. Block diagram of RDL IMD Simulator signal generator

Figure 8 shows actual detected power envelopes of eight combined carriers generated with an RDL IMD Simulator. The first power envelope has eight carriers with random phases and the second has the carriers phase aligned. The peaking of the power envelope is clearly seen in the second case of phase aligned carriers.



Random Phases Aligned Phases

Figure 8. Actual detected power envelopes

In summary, a phase controlled multi-tone signal generator provides the best accuracy, repeatability, and flexibility when testing multi-carrier communications systems.

New Techniques for Analyzing Wireless Signals with Digital Oscilloscopes

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I Abstract

Modern Digital Oscilloscopes are capable of capturing long complex waveforms, displaying them with a variety of viewing tools and then making sophisticated measurements. This allows the wireless designer to examine data streams using familiar tools such as eye diagrams and XY displays but also to perform much more accurate diagnostics and analysis of circuit performance.

II Improvements in Eye Diagram Measurements

Eye diagrams are one of the most common tools used by wireless design engineers to qualitatively examine signal fidelity. Traditionally, the engineer looks for a large open area in the center of the eye as the sign of good clean signal. Impingement of signals into the central area from the left/right side are indications of phase noise (timing jitter), while reduction of eye size from the top/bottom is caused by amplitude instabilities. The advent of new display and calculating capabilities in digital oscilloscopes now make it possible to view and measure eye diagrams more exactly. Worst case parameter statistics make it possible to know the exact eye size, and histograms allow the engineer to characterize both timing and amplitude jitter much more accurately. This allows the engineer to more accurately evaluate the effect of changes intended to improve signal fidelity. Also, instead of looking at just a random overlay of multiple signals that form the "eye" it is possible to recall the individual occurrences (for example, those which violate the central area of the eye) for closer examination.

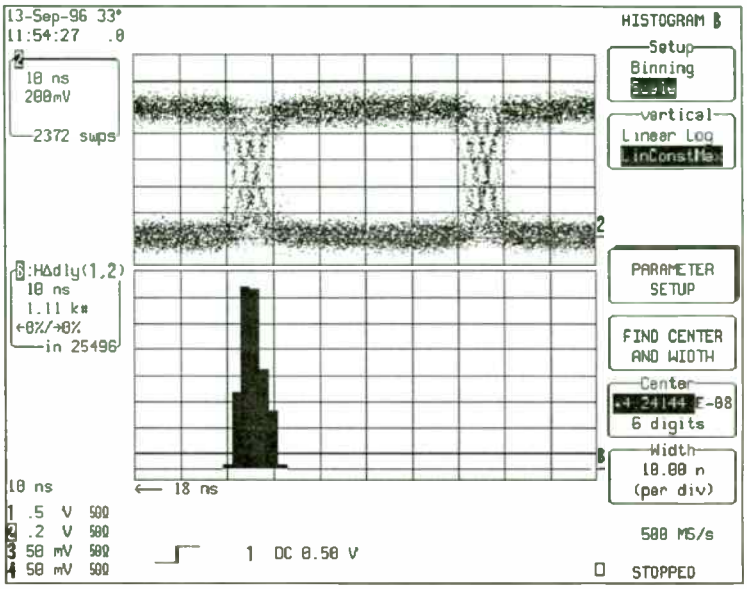

Figure 1 - Eye diagram with histogram of phase jitter

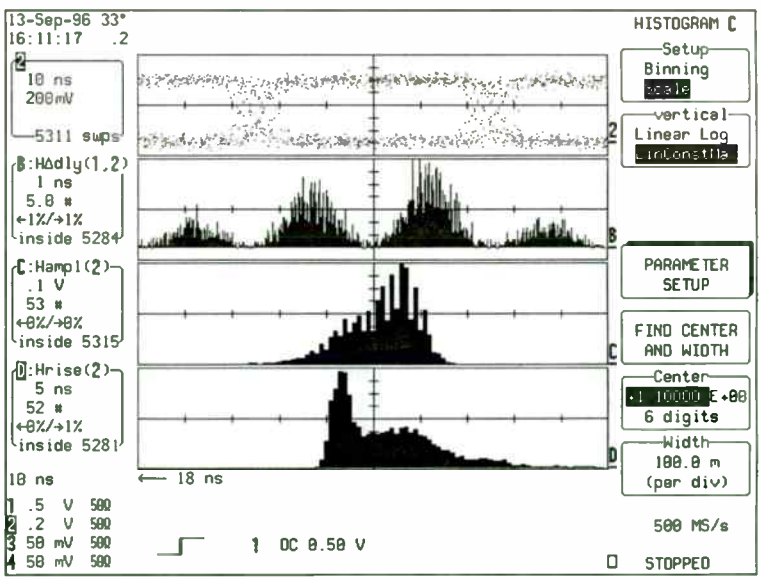

Figure 2 - Eye diagram with histograms of phase jitter, amplitude fluctuation and risetime variations. The histogram of phase jitter in the second trace is an expansion of the same data portrayed in the lower trace of figure 1

Figure 1 shows an eye diagram captured on a digital oscilloscope displayed in traditional format. Note there are four distinct bands on the falling edge due to severe phase jitter. The histogram below the eye shows a statistical distribution of the arrival times of the signal edges. In figure 2, this histogram has been expanded for easier viewing, and additional histograms have been added to display an analysis of pulse widths and risetimes. This type of augmentation to the traditional eye diagram allows the engineer to make much more accurate analysis of circuit performance and to see much finer details of signal characteristics. In the simplest case, the maximum and minimum values of the histogram will show if the worst case performance of the product under test meets specifications.

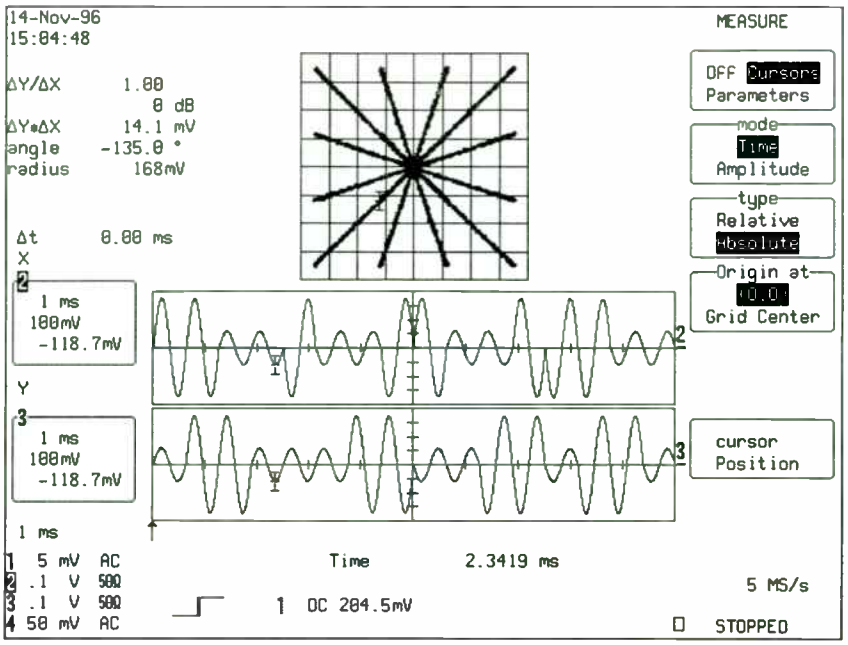

Figure 3 - Trace 2 shows the in-phase (I) component and trace 3 the quadrature (Q) component of a 16 QAM signal. The state transitions are shown in the X-Y diagram. Note that cursors mark a typical peak in the I and Q signals and simultaneously measure the phase and amplitude (radius) of the resultant vector sum.

III Measuring Peak and Average Power

Another interesting development driven from the new display and calculation abilities of digital scopes affects engineers who want to measure the peak and average power in complex signals. A 16 QAM signal, for example, can be analyzed by viewing an XY-display of I and Q simultaneously with I vs time and Q vs time. These complex signals may result in data dependent, high peak to average power ratios requiring amplifiers and related components with large dynamic ranges. Digital oscilloscopes can help designers of such systems evaluate the dynamic range requirements by providing a fast, easy method to measure instantaneous power on very long data records. Measurement parameters can read the average and peak power levels directly from the instantaneous power waveform. The following example illustrates the techniques that can be used to measure instantaneous power.

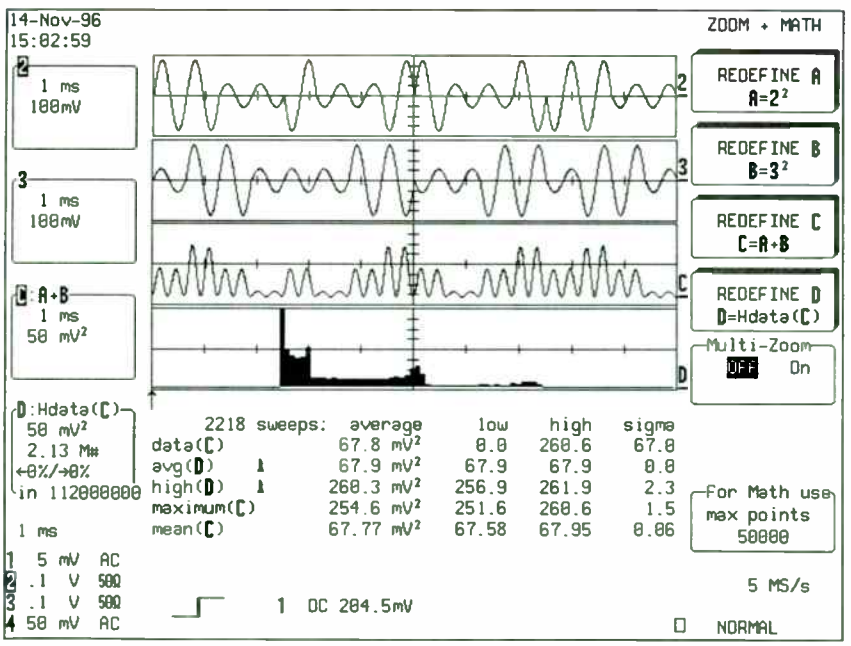

Figure 4 - Top Trace -I signal, Second Trace -Q signal, Third Trace - I^2+Q^2 (sum of the squares), Bottom Trace - Histogram of Values for I^2+Q^2

The in-phase (I) and quadrature (Q) components of a 16-state quadrature amplitude modulated (16 QAM) signal are shown in traces 2 and 3 , respectively, in figure 3. The 16 states shown utilize 3 distinct average power levels corresponding to the 3 possible combinations of the I and Q voltage levels of 0.707and 0.236 V_{P-P}. The power levels are:

$$P_A = 0.126\ V^2 \quad (1)$$
$$P_B = 0.069\ V^2 \quad (2)$$
$$P_C = 0.056\ V^2 \quad (3)$$

Note that since we will be taking power ratios the power is expressed as a squared voltage,V^2, to simply the measurements. If required the square of the voltage can be divided by the impedance using the rescale function.

The expected average power in the waveform based on the 16 states included can be calculated as:

$$(4P_A + 8P_B + 4P_C)/16 = 0.069\ V^2 \quad (4)$$

The peak power, corresponding to P_A is 0.249 V^2.

We have now derived the expected average and peak power for a known waveform from purely theoretical considerations:

Average Power = 0.069 V^2 (5)

Peak Power = 0.249 V^2 (6)

Figure 4 shows the steps used to measure the instantaneous power waveform and derive the peak and average power levels. The instantaneous power of the output signal is calculated by taking the sum of the squares of the I and Q waveforms. This is displayed in trace C. The data in trace C is histogrammed and shown in trace D. This trace shows three overlapping distributions. The average and peak values were determined in two ways. The average value of the histogram data and the mean value of trace C were both measured using the appropriate parameters. Likewise, the peak power was determined using Maximum of C and Highest value in the histogram (HIGH[D]). Maximum of C, an average of over 2200 maxima, was used in order to evaluate the range of maximum values encountered and determine the effect of noise peaks on the peak power measurement. Based on the measured values the ratio of peak to average power is:

$$P_{PEAK}/P_{AVG} = 0.2546/0.067$$
$$= 3.8$$
or 10 log (3.8) = 5.79 dB

Based on the expected values which were derived previously:

$$P_{PEAK}/P_{AVG} = 0.249/0.069$$
$$= 3.61 \quad (7)$$
or 10 log (3.61) = 5.57 dB (8)

This is a difference of about 0.2 dB or about 5% of the expected value.

Note that this error margin includes the errors due to two sources, the arbitrary waveform generator which produced the waveforms and the oscilloscope. Since both units have similar DC accuracy specifications we can assume that the error is equally distributed between them.

It is important to note that certain features assumed in this discussion are key to implementing the measurements. They include the ability to do chained mathematical calculations on long waveforms, extract key waveform parameters automatically, display histograms and calculate parameters concerning the statistical distribution of the histograms.

IV Measuring Amplitude, Phase and Power in Vector Modulated Signals

Vector modulation is used to generate complex signals which encode multiple data bits per symbol. As an example, consider the vector diagram of the I (in phase) and Q (quadrature) components of a CDMA signal shown in figure 5. The vector diagram shows the four possible data states per character and the transition paths between them. X-Y Cursors provide readouts of the I and Q amplitudes and the vector phase angle and magnitude simultaneously. This feature allows spurious states in the vector diagram to be linked to the source waveforms.

By using a symbol clock to externally sample the oscilloscope a constellation diagram is generated. Figure 6 shows a constellation diagram for a 16 QAM signal. Relative amplitude cursors are used to measure the width and height dispersion of the logic states. By using the polar readouts and the absolute time cursor the phase and/or amplitude differences of the signal can be measured. Math functions allow users to perform more extensive analysis. In figure 7 the instantaneous power and bandwidth of a 5 MHz carrier, modulated by a CDMA signal, is shown.

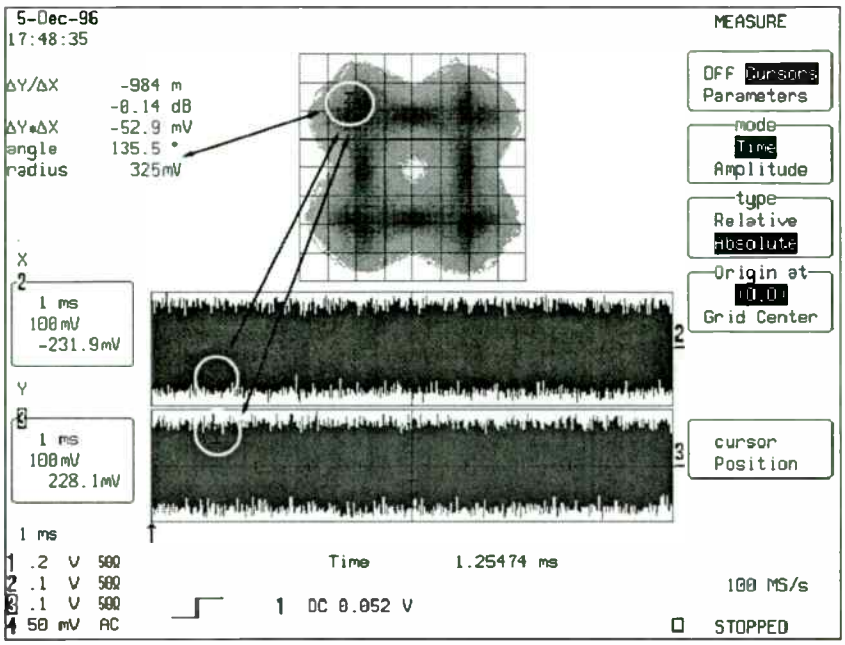

Figure 5 - Vector Diagram using X-Y display includes both Cartesian and Polar readout of cursor position. Vector magnitude (325 mV) and Phase (135.5 °) are read in the X-Y cursor field. This is the vector sum of I (-232mV) and Q (228mV).

CDMA signal from Anritsu model MC3670B courtesy of Qualcomm Corp.

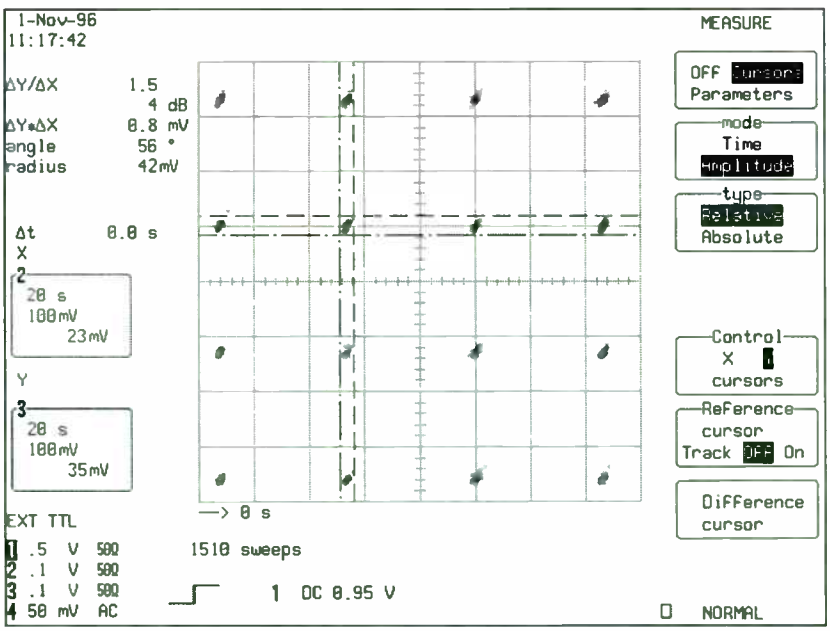

Figure 6 - A constellation display of a 16 QAM signal. The line cursors measure time and amplitude jitter.

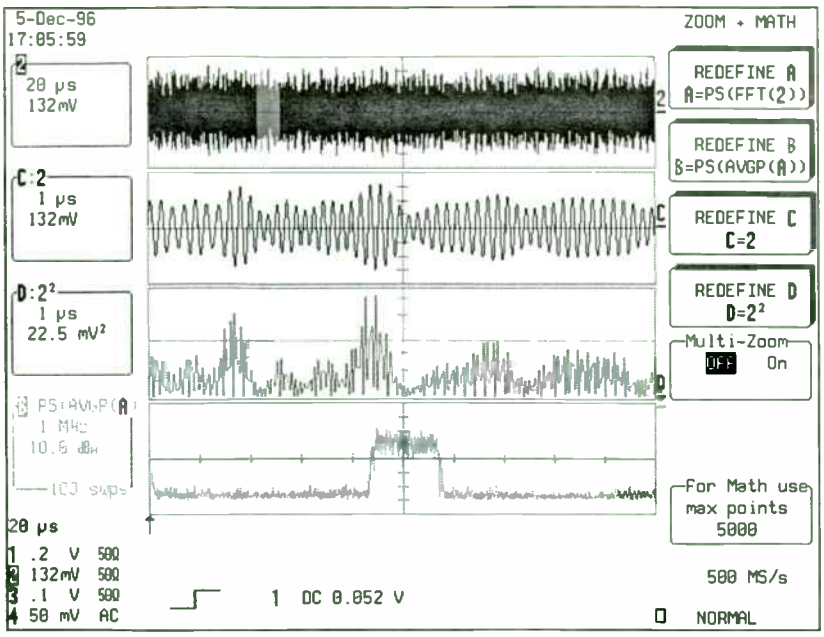

Figure 7-Top trace: Modulated waveform. Second trace: expanded view of the modulated carrier. Third trace is the squared voltage (power) waveform. Bottom trace: Frequency spectrum (FFT) showing signal bandwidth. CDMA signal from Anritsu model MC3670B courtesy Qualcomm Corp.

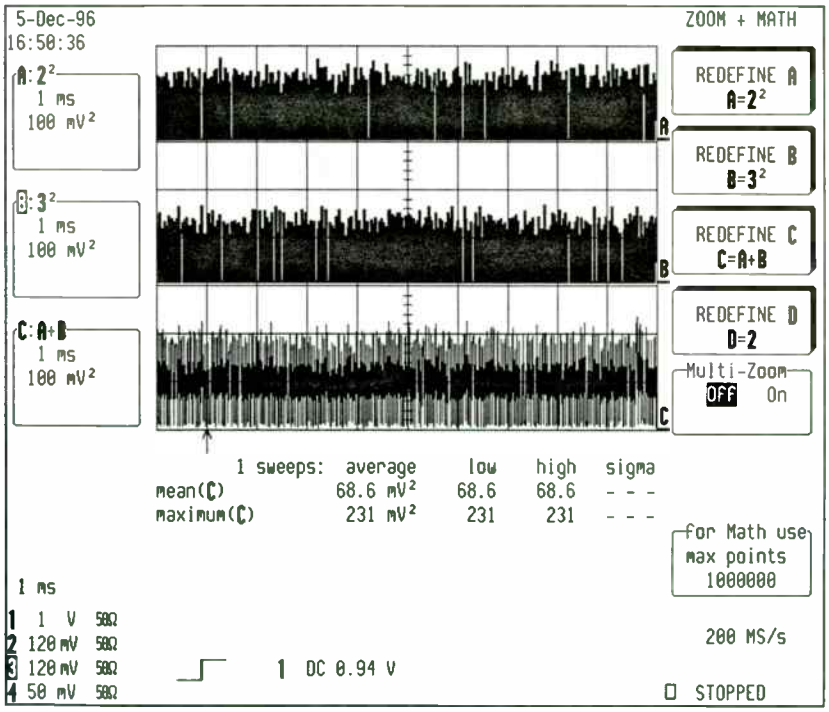

Figure 8 - Using cascaded math operations to calculate instantaneous power from the I and Q components of a CDMA signal. The top two traces are I^2 and Q^2, the lower trace is the sum of the squares. The two parameters at the bottom of the screen give the mean (average) and peak (maximum) power. CDMA signal from Anritsu model MC3670B courtesy Qualcomm Corp.

The instantaneous power is calculated by squaring the voltage waveform. If required this can be normalized to impedance level by using the rescale function to divide the waveform by a constant value. The signal bandwidth is determined by taking the FFT of the signal, here displayed in power spectrum format. Any of these analyses can be expanded horizontally or vertically using zoom functions. This permits detail such as the carrier waveform to be observed.

Note that it is important to be able to chain math functions. It often requires a series of calculations in order to extract the desired parameter. In figure 8 the instantaneous power of the CDMA waveform is calculated by squaring and summing the I and Q components. Note that all math operations in this case use up to 1,000,000 data points. Processing speed becomes essential in calculations involving such long records.

Automatic parameter extraction, such as determining the peak (maximum) and average (mean) from the instantaneous power waveform, simplifies analysis. Instead of having to transfer long long records to an external computer the oscilloscope analyzes the data and provides only the desired values.

PERSONAL-COMMUNICATIONS-SERVICES (PCS) APPLICATIONS

Personal-Communications-Services (PCS) Applications

Session Chairperson: Roland Soohoo,
Fujitsu Microelectronics (San Jose, CA)

A Silicon Bipolar/Bi-CMOS 'Gate Array' for High Volume and Low Cost Wireless Applications

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Abstract

As Wireless systems become increasingly popular in the marketplace, the need for price reduction and higher levels of integration are paramount. This paper describes an innovative, fast-turnaround Silicon "gate array" technology known as Versi-TILE that provides an extremely high level of RF and support circuitry integration (including PLLs) at up to 3 Ghz operating frequency on a single chip.

Because of its RF operating frequency range this technology can be applied to such diverse applications as GPS, cellular handsets and infrastructure, cordless telephone, WLL, ISM-Band hardware and other high-volume wireless equipment and systems.

Overview

The Wireless industry has matured substantially over the past few years in terms of both technology and the market. The use of discrete devices and designs continues to be popular. However, end users are increasingly demanding smaller and lighter electronics with more functionality. The use of ICs with one or two RF functions is becoming commonplace to meet this need. More recently chipsets have appeared that are targeted toward specific applications.

Versi-TILE is a unique semi-custom technology that bridges the gap between discrete and chipset approaches. It provides a smaller, lighter solution as compared with discrete appraoaches due to its high level of integration. It also lowers manufacturing costs since the number of assembly steps are reduced and the parts count is less. In addition, since Versi-TILE is a "gate array" type of technology, it offers lower risk and quicker turnaround time than full custom approaches. This high level of integration and flexibility enable the RF designer to specify exactly what he/she wants for a particular application.

1. The Technology

Versi-TILE is a RF LSI technology that utilizes a "frame" which is an uncommitted array of transistors, capacitors and resistors deposited on silicon. The devices can be

interconnected by a two level metal system to create a variety of RF and IF functions derived from predefined macros and user requirements. Both Bipolar and Bi-CMOS processes may be utilized depending on what functions need to be realized. A typical frame is shown in Figure 1.

There are different areas on the chip that are designated for particular functions including prescaler, PLL, charge pump and analog. One of the key features of Versi-TILE is the ability for a customer to implement an entire PLL except for the loop filter from an extensive library of production device macros and combine it with RF functions on the same chip. A full PLL is implemented using a Bi-CMOS process. The CMOS devices utilize .8 um design rules.

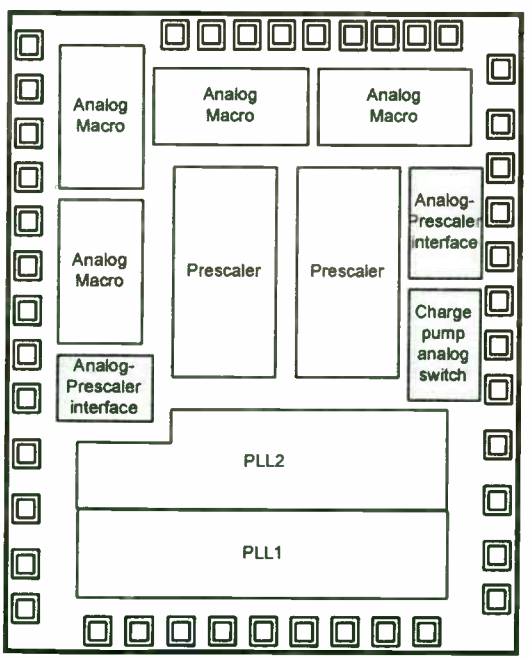

Figure 1 - A Typical Versi-TILE Frame

A more detailed view of a typical analog macro is shown in Figure 2. Each analog cell consists of a collection of resistors, transistors and capacitors that can be interconnected to realize RF and IF functions. The Bipolar devices utilize a state-of-the-art self-aligned .6 um process and has a finished emitter width of .2 um with an ft of approximately 28 Ghz.

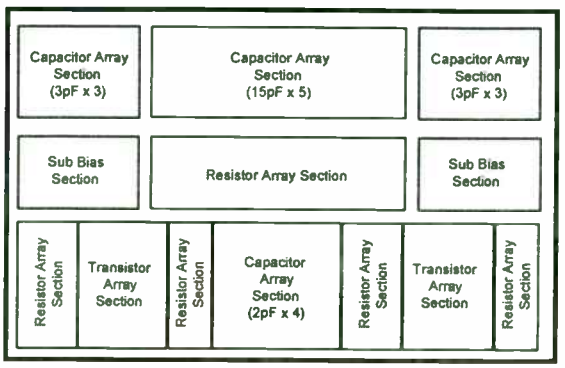

Figure 2 - Detailed View of Analog Cell

Many of the popular RF analog components such as mixers, LNAs, RF/ IF/AGC amplifiers, VCO's,modulators / demodulators (including I/Q), Limiters, Discriminators, Detectors (SSI/RSSI) have predefined, fully characterized macros that can be fine tuned based on customer need. Since the frame contains uncommitted elements customization is easily accomplished.

2. Functional Block Descriptions

A wide variety of functions have been implemented using Versi-TILE. The descriptions below describe only basic characteristics of macros that have already been developed.

A. The Oscillator

The on-board oscillator cell is based on a Colpits design as shown in Figure 3. A

buffer is included to shield the source from load pulling effects and to increase the output power. An off chip resonant circuit is used to set the output frequency of the oscillator since the Q and resultant phase noise are better than on chip solutions.

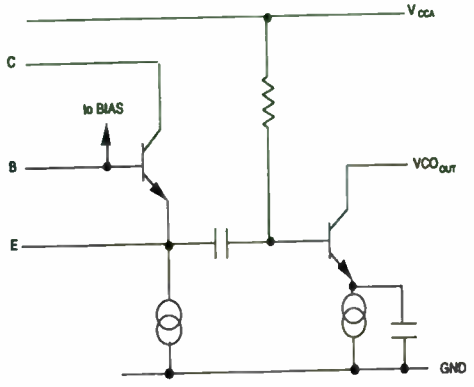

Figure 3 - Colpits Oscillator Cell

B. Mixer Cell

A Gilbert-cell topology is typically used for realizing the mixer function as shown in Figure 4. Pairs of differential amps are interconnected to create an active double balanced mixer. The mixer is followed by a IF amp which provides a single ended output. Typical conversion gains can range between 6 and 12 dB with about 9 to 12 dB Noise Figure.

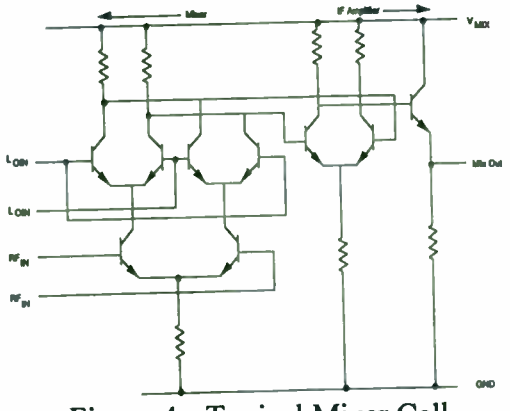

Figure 4 - Typical Mixer Cell

C. Amplifiers

A variety of amplifiers have been implemented using Versi-TILE including LNAs, Gain Blocks, VGAs, AGCs, and Limiting Amps at both IF and RF Frequencies. Typical Noise Figures at 900 Mhz is below 2 dB with 14 dB of gain. A variety of compression points are available since different device sizes are available in the frame.

E. PLLs, Prescalers and Charge Pumps

Depending on which Versi-TILE frame is utilized as many as 3 complete PLLs (RF or IF) can be implemented on one chip along with RF functions. The complete PLLs include a prescaler, swallow counter, programable counter, phase comparator and optimized charge pump. The user only needs to provide a external loop filter for operation. Figure 5 shows the block diagram of the integrated PLL. Fujitsu has a wide array of standard PLL cells to choose from that can be optimized for lock up time, low power consumption, etc. A mask programable IF PLL is also offered which eliminates the need for command and clock lines for single frequency operation.

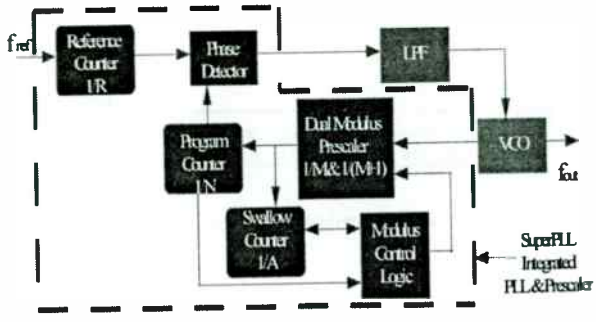

Figure 5 - "Super PLL" Block Diagram

F. Other Functions

Optimized macros have also been developed for I/Q modulators, SSIs, RSSIs and phase shifters. The key point is that a very wide range of IF and RF functions can be realized with Versi-TILE.

G. Packaging and Pinouts

A wide range of packaging options are available depending on how many functions are implemented on the Versi-TILE chip. Packages range from 8-pin SSOPs to 64 -pin SQFPs. Each RF and IF function can have its own set of pinouts. In this way the risk is minimized by giving the designer the most control over each separate function. During the evaluation phase the designer can test each function separately to fully qualify his design. During the manufacturing phase a series of interconnects along with interstage matching (if needed) on the printed circuit board can be implemented between pins.

The first-pass success rate is extremely high with this process because many of the macros that are implemented have been proven over a several-year period. Because of the high level of integration that Versi-TILE provides, a significant amount of board space can be saved. This integated approach also drives the cost of manufacturing down since a very repeatable package profile is attained which results in reduced assembly issues during pick and place and assembly operations.

3. Turnaround Time

Another unique feature of the Versi-TILE process is the ability to deliver engineering samples within 10-12 weeks after freezing a mutually agreed upon specification. After customer qualification, manufacturing quantities can be available within 10-12 weeks. Figure 6 shows the typical development cycle from initial discussions to manufacturing.

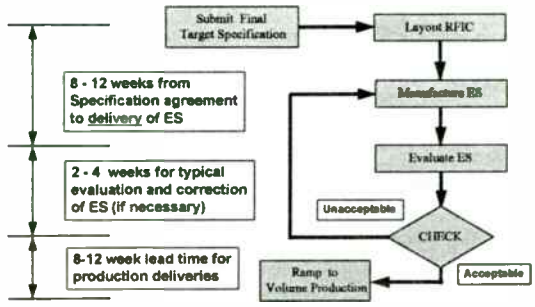

Figure 6 - Versi-TILE Development Process

This timeline can be compared to the full custom approach where a typical development can take as much as 12-18 months with no guarantee of first pass success.

4. The Integrated Approach - An Actual Implementation

Many designs have been spun with the Versi-TILE process. An example of the level of integration that can be achieved is shown in Figure 7. This chip serves as an RF front end for a cellular digital phone application. Three PLLs (TX LO, RX LO and offset mixer LO), 2 RX mixers, IF LIM/RSSI CKTS, TX I/Q MOD, offset mixer and AGC amplifiers

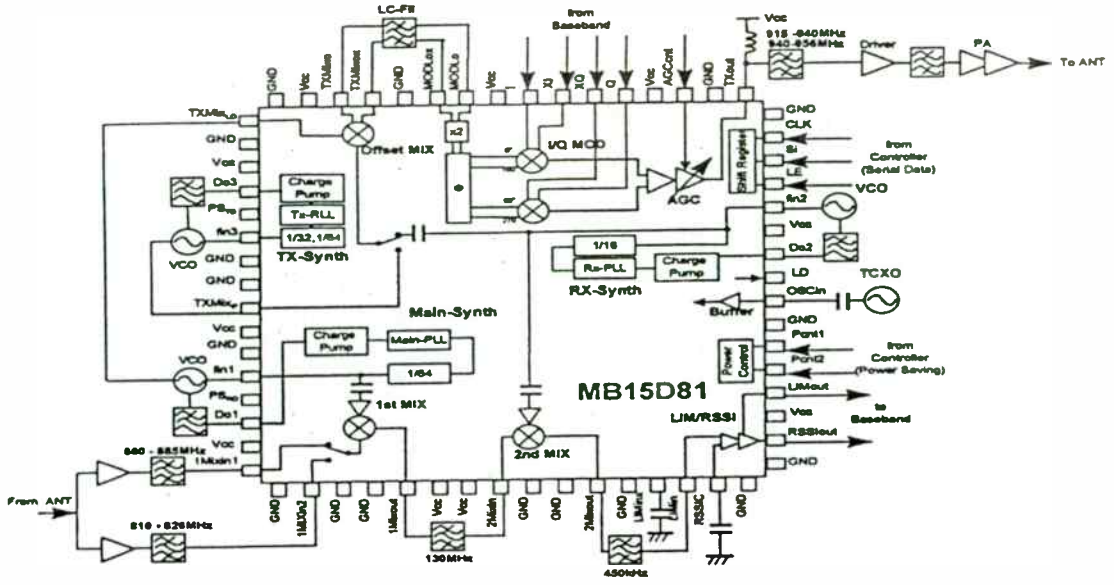

Figure 7 - An actual Versi-TILE implementation

are contained on one piece of silicon. This level of functionality is realized in a 10x10x1.5 mm package. Varying levels of integration is available depending on the designer's needs.

Some of the key specifications of the chip include:

TX chain:

I/Q modulator/AGC amp:

Operating Frequency:914-958 Mhz (RF)
Vector Error: 3.0%
Phase Error: 1.5 degrees
Carrier Leakage: -30 dBc Max.
SSB Max. Output Power: +4 dBm typ.

Offset mixer:

Operating Frequency: 914-958 (RF), LO (two bands) 680-755 Mhz and 1044-1086 Mhz
Conversion gain: -4 dBm typ.
1 dB compression point: -15 dBm typ.
LO input level: -10 dBm typ.

RX chain:

1st mixer:

Conversion gain: 17 dB
NF = 7 dB
1 dB compression point: -3 dBm

2nd mixer:

Operating Frequency: 130 Mhz (RF), 450 Khz (IF)
Conversion gain: 22 dB
NF = 10 dB
1 dB compression point: +2 dBm

LIM/RSSI:

Operating Frequency: 450 Khz
Limiting amp gain: 80 dB
RSSI output sens.: 30 mV/dB
RSSI dynamic range: 70 dB

Conclusion

Versi-TILE, a unique RF LSI 'Gate Array' technology has been described. It utilizes standard "frames" that consists of uncommitted cells of transistors, capacitors and resistors. These devices are interconnected by two layers of metalization based upon the RF designers' circuitry and system needs. Because it is a semi-custom process, it offers the RF designer a major amount of flexibility to implement what they need for their application.

The process offers very quick turnaround time and a extremely high first-pass success rate. Versi-TILE drives the level of integration up thus eliminating excess size and weight compared to discrete approaches. Manufacturability and repeatability is also improved using this approach.

Acknowledgements

The authors would like to thank John Quinn for his encouragement and his helpful suggestions that improved this paper. We would also like to thank Rachel Wilson for her assistance in preparing the final draft.

Internetworking and Interoperability Between Similar and Dissimilar PCS Systems

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Personal Communications Services (PCS) is an integrated voice and data solution that provides communications at any place, any time, and through any access device. To realize such a service, internetworking and interoperability (I&I) between different PCS systems is an important factor. Standard bodies such as the Telecommunications Industry Association (TIA's) TR-46 and the American Telecommunications Standards Institute's (ATSI's) T1P1 are working on I&I issues. However, much more effort should address such issues if having a nationwide service in the U.S. is the goal. At present, six different air interfaces are defined and are planned for implementation in North America. These standards are dealing with two different Mobile Application Parts (MAPs). Several issues should be addressed by telecommunication carriers and device manufacturers in order to achieve interoperability. Roaming between similar and dissimilar networks, privacy, and authentication are some of the major areas of concern.

Three different approaches are introduced for PCS security. Shared Secret Data (SSD), Token-based Secret Key, and public key systems are the three most commonly-used mechanisms. An IS-41-based authentication system using SSD is planned for use in most PCS systems in North America. In this system, a secret key is stored in the network and device, and SSD is generated from this key. The token-based secret key system is used in GSM and is based on DCS1900 authentication. It uses a secret key with authentication triplets. Each device has an International Mobile Station Identification (IMSI). When a subscriber registers in the system, the system assigns a Temporary Mobile Station Identification (TMSI). The TMSI is changed when the subscriber roams from one service area to another, The Personal Access Communications System (PACS) air interface uses a public key system. In this system, a transmitter encrypts the data by its private key and the receiver's public key. When a mobile system roams from its Home Location Register (HLR) to a Visitor Location Register (VLR), the interoperability of the security mechanism comes into play. The TIA has defined a solution for I&I between IS-41 and DCS1900 MAP which addresses privacy and authentication. It is a dual-mode HLR solution for I&I functionality (HLR-IIF).

When the mobile end system roams, intersystem handoffs can become a complicated issue. When current and next stations have a dissimilar air interface, the handoff is a challenge. When the handoff is mobile-triggered, then the mobile should be able to compare signal strength and error rate based on two different air interfaces. The situation is more or less the same when the handoff is initiated by base stations.

In addition to the roaming issue, intersystem startup is another important factor. When a multimode mobile end system is turned on, it should figure out which system it is operating and appropriately set its mode of operation.

There are numerous other areas that need careful attention. Level of service, maintenance, and equal access are some of these topics. This paper discusses all of the aforementioned issues in detail.

PCS MINI-CELL BASE STATION GROUNDING

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Abstract

Second generation cellular digital wireless Personal Communications Services (PCS) has recently begun deployment, and is expected to generate annual revenues of $10 billion by the year 2000. Considerable amounts of sensitive electronic equipment is currently being installed in PCS mini-cell base station sites around the world. In order to protect this investment and stay on-line, proper grounding and bonding practices are essential. This article describes the advantages and disadvantages of current grounding practices, with a focus on identifying the limitations associated with the use of traditional driven rod subsystems. The installation of one heavy-duty electrolytic earth electrode is proposed as a cost-effective protection system with maximum long-term safety, stability and reliability. The general principles of this advanced digital wireless telephone system grounding are discussed, including recommendations concerning appropriate grounding and bonding.

Introduction

At a PCS site, an earth grounding system is necessary for the following reasons: 1) To maintain good contact with the earth so that all noncurrent-carrying metal parts on site are maintained at ground or near zero potential; 2) To provide paths into the earth for high currents caused by lightning or surges to be dissipated into the earth as quickly and safely as possible; 3) To provide paths into the earth for low currents caused by RFI or static which can be accumulated in or on the system enclosures.[1]

A grounding system should provide a stable, low impedance path to earth without problems or recurring costs. The system should be maintenance free, with a life expectancy which exceeds the expected life of the cell site. Each element of the system should have sufficient conductivity, resist fusing and mechanical deterioration, and be mechanically rugged and highly reliable. [2]

Traditional Earth Electrode Subsystems

Traditionally, the preferred method of providing an earth ground for communications sites is to bury a ring ground encircling the tower and/or the site and supplement this ring with ground rods installed every 15 feet. Various types of mechanical connectors are used to bond all components. Although this method can provide a satisfactory grounding system at the time of installation, it has several limitations.

Installing a ring ground around the site requires extensive trenching, which may be difficult and sometimes is not feasible due to geological barriers such as rock. A ground ring is typically buried 1-3 feet below grade and is subject to seasonal changes in temperature and soil moisture content. These seasonal changes greatly affect the stability of the grounding system, and the characteristics often change as the years go by.

The integrity of driven rods is influenced by the installation process. Ground rods are pounded or driven into the earth to the desired depth, typically 8'. In rocky or hardpan soil, or if the soil is underlaid with a layer of rock, rods cannot be installed in this manner. The ground rods will either bend or refuse further pounding. On occasion, they have been known to return and protrude from the surface after being deflected by underground obstacles.

Ground rods can be damaged at installation and degrade over time. The copper coating scratches or chips off during installation, and the steel underneath galvanically reacts and quickly corrodes. It is common to find these types of rods completely disintegrated upon excavation, however, this situation oftentimes is unnoticed due to the relative disinterest in grounding system evaluations.

In analyzing resistance to remote earth, the first few inches around the rod are the most important [3]. When pounding a driven ground rod into the earth, it is often difficult to obtain satisfactory contact between the rod and soil because of the nonhomogeneous characteristic of most soil.

While mechanical clamps may be effective when first installed, they tend to loosen over time. To maintain a continuous, low resistance grounding path, they must be checked and tightened periodically. Shielding loses its effectiveness across these bonds. Even though the DC resistance may be low, mechanical clamps provide a physically nonhomogeneous bond. The interface is not continuous at RF frequencies and results in a bowing or wavy effect between the connected members [4]. Mechanical clamps are prone to corrosion, especially when used in outdoor or underground applications. Oxygen and moisture which penetrates minute gaps in mechanical connections can rapidly corrode the bond.

The traditional type of grounding system must be maintained annually by inspection and testing of system integrity including checking the effectiveness of all connectors and visual inspection for corrosion.

Recommended PCS Mini-Cell Base Station Grounding

A site survey should be conducted before installing the grounding system. The survey should determine soil resistivity and other geological characteristics of the site, as well as environmental and climatological characteristics [5]. Actual soil resistivity measurements at the site offer the only practical means of determining the conductivity of the soil. This procedure is necessary to design a grounding system which will meet an acceptable resistance to earth.

An alternative to driven rods is an electrolytic ground rod system. This electrode is a hard-drawn copper pipe filled with a mixture of non-hazardous earth salts (see fig.1). The function of an electrolytic system is similar to the traditional chemical treatment of grounds, without the increased labor or loss of effectiveness over time, and without any detrimental effects to the environment. An L-shaped rod provides the same protection as a vertical rod without having to auger a hole into the earth.

Soil resistivity measurements taken during the site survey are used to model the conductivity of the soil in the vicinity. I.E.E.E. formulae as well as various software packages are used to determine the length of the XIT rod required to meet a specified resistance to earth specification. In general, 5 ohms is a proper target resistance for a PCS Mini-Cell Base Station grounding system.

Installation and proper bonding of one heavy-duty electrolytic earth electrode in conjunction with proper lightning protection and surge suppression equipment will provide a cost-effective protection system with maximum long-term safety, stability and reliability. Installation typically requires a small area. The resulting system provides a low-impedance path to ground for surge and fault conditions. The system is very stable and has a life expectancy of approximately 50 years.

The holes should be backfilled with high-solids encapsulated bentonite clay. Bentonite is a very dense clay that will adhere to any surface, creating very effective contact with the electrodes. High-solids bentonite hydrates and will not dry out over time. It is non-corrosive and allows natural mineral salts to ionize, making bentonite a highly conductive material with a PH of 8 to 10. Bentonite has a resistivity of 2.5 ohm-m and, when properly used as a backfill material, actually increases the rod's electrical effectiveness [6].

Exothermic welds or irreversible high-compression type fittings provide the most durable, permanent connection available. Both types of connectors are inherently free from galvanic corrosion. Both types of connectors have been approved by the National Electric Code [7] and IEEE Std. 80 [8].

Note that all components used in the recommended grounding system are solid copper. Copper conductors are highly conductive and, because of their cathodic nature, resist underground corrosion. If all components are adequately sized and free from damage, the use of copper assures integrity of the below grade grounding system for many years [9].

Two basic types of PCS Mini-Cell Base Stations exist. The monopole and the rooftop site. At the monopole sites, the electrolytic rod should be installed at the base of the tower. The electrolytic rod is bonded directly to a Master Ground Bus. Exothermic welds or irreversible high-compression fittings should be used to bond these components.

At a rooftop site, the electrolytic rod is installed at ground level. This rod may be installed either indoors or outdoors. A #4/0 copper conductor bonds the ground rod to the Master Ground Bus, located on the rooftop. This conductor should be run inside conduit for protection of both personnel and the conductor itself.

At both the monopole and rooftop sites, a copper Master Ground Bus (MGB) should be installed at a convenient location. The following items should be bonded to the MGB: cable ground kits, the monopole, the plenum/BTS, all non-current carrying metal objects such as fences and masts, and the power and telephone utility service entrances. The MGB should be bonded directly out to the electrolytic rod using #4/0 AWG copper conductor. (See fig.2)

It is very important to keep all current carrying devices at the same voltage potential. Bonding must be provided to assure electrical continuity and capacity to safely conduct any fault current likely to be imposed. Bond all components using exothermic welds or irreversible high-compression two hole lug connections to ensure a permanent, quality connection.

Lightning Protection

For land sites, the monopole itself acts as an air terminal. If there are antennas near the top of the tower, a lightning air terminal should be installed to protect the antennas as specified by NFPA 780. Approved cable ground kits should be properly installed on all cable sheaths at the top and the bottom of the monopole. A cable ground bar should be installed near the top of the tower. All cable ground kits should be bonded to bus bars at both the top and the bottom of the monopole. The ground bar at the top of the monopole is bonded to the MGB.

For rooftop sites, air terminals, lightning conductors and masts are used to provide zones of protection from lightning. The lightning protection system is kept separate from the radio system, except where it is referenced to the MGB. The MGB is bonded directly to the XIT grounding system.

Transient Voltage Surge Suppression

When a transient is allowed to enter communications and electronic circuitry, the result can be unreliable operation or complete destruction of electronic circuitry. Such damage can be prevented by proper protective devices [10]. Power protection products absorb incoming transients, protecting all equipment from damage and downtime. AC lines and Telco lines should be protected by surge suppressors. A properly specified and installed transient voltage surge suppressor which utilizes high speed semiconductor devices (such as silicon avalanche diodes) as well as a back-up secondary stage will provide the best protection.

Verification Testing

If soil resistivity and designs are performed correctly, the resulting grounding system will meet or exceed requirements. However, measurements of the ground resistance should be taken to verify the adequacy of the new grounding system. These measurements should be taken immediately after the grounding system has been installed. There are two types of tests to determine the resistance to earth of a grounding system. The three point fall-of-potential test is used when the grounding system under test is isolated. If the grounding system is not isolated, such as when the utility services have already been installed, a clamp-on meter may be used.

Cost Comparison

Installation of the PCS Mini-Cell Base Station Grounding System requires minimal trenching, thereby greatly reducing the labor involved with installation. The 50 year life expectancy of the system in conjunction with high quality permanent bonding eliminates the need for annual maintenance. The initial cost of electrolytic rods is offset by the fact that the lower resistance per rod allows fewer rods and buried copper conductor to do the same job. In general, when directly comparing the two systems including materials and labor, the PCS Mini-Cell Base Station Grounding System saves money, time, and lasts longer.

Conclusion

Consideration should always be given to installation or changes of a grounding system. A field survey to examine suitability and safety should be

performed by consultants or trained personnel. Installation should be performed only by qualified construction personnel experienced in the area of grounding.

The recommendations covered in this paper are made in the interests of safety, quality assurance, proper procedure, and operation reliability in compliance with the intentions of the National Electric Code. Installation of the PCS Mini-Cell Base Station Grounding System will result in the following benefits and improvements to the communication cell site:

1) The low-resistance grounding system provides protection from lightning and transient voltage surges. This safeguards the cell site to more likely remain on the air during unexpected voltage surges.

2) Keeping all non-current carrying metal objects at the same voltage potential reduces interference from radio and electromagnetic waves.

3) All recommendations are made with the interest of providing a long-term, maintenance free grounding system with no recurring costs or problems.

4) A field survey with soil resistivity testing, followed with experienced engineering design, removes the element of chance and guesswork in providing a grounding system which will be safe, long-lasting, and will meet a specified resistance to earth.

5) Upgrade to a level of top quality standards. Installation of the PCS Mini-Cell Base Station Grounding System will provide the highest quality grounding system in terms of: safety, effectiveness, longevity, investment protection and cellular customer satisfaction.

References

[1] "*Electrical Grounding*", Ronald P. O'Riley, Delmar Publishers Inc., 1988, p. 55

[2] *IEEE Guide for Safety In AC Substation Grounding*, ASNI/IEEE Standard 80-1986, p.63

[3] *Recommended Practice for Grounding of Industrial and Commercial Power Systems*, ASNI/IEEE Standard 142-1982, p.121

[4] "*Grounding and Bonding*", Gilbert Sharick, abc of the Telephone, Vol. 13, 1981, p. 75

[5] "*Grounding and Bonding*", Gilbert Sharick, abc of the Telephone, Vol. 13, 1981, p. 7

[6] "Bentonite Rods Assure Ground Rod Installation In Problem Soils", Warren R. Jones, *I.E.E.E. Transactions on Power Apparatus and Systems*, Vol. PAS-99, No. 4 July/Aug 1980 pp. 1343-1345

[7] *National Electric Code*, NFPA No. 70 1993 article 250-113

[8] *IEEE Guide for Safety in AC Substation Grounding*, ANSI/IEEE Standard 80-1986, pp. 68-69

[9] *IEEE Guide for Safety In AC Substation Grounding*, ASNI/IEEE Standard 80-1986, p.63

[10] *Power System Grounding and Transients: An Introduction*, A.P. Sakis Meliopoulos, Marcel Dekker, Inc., 1988 pp. 339-340

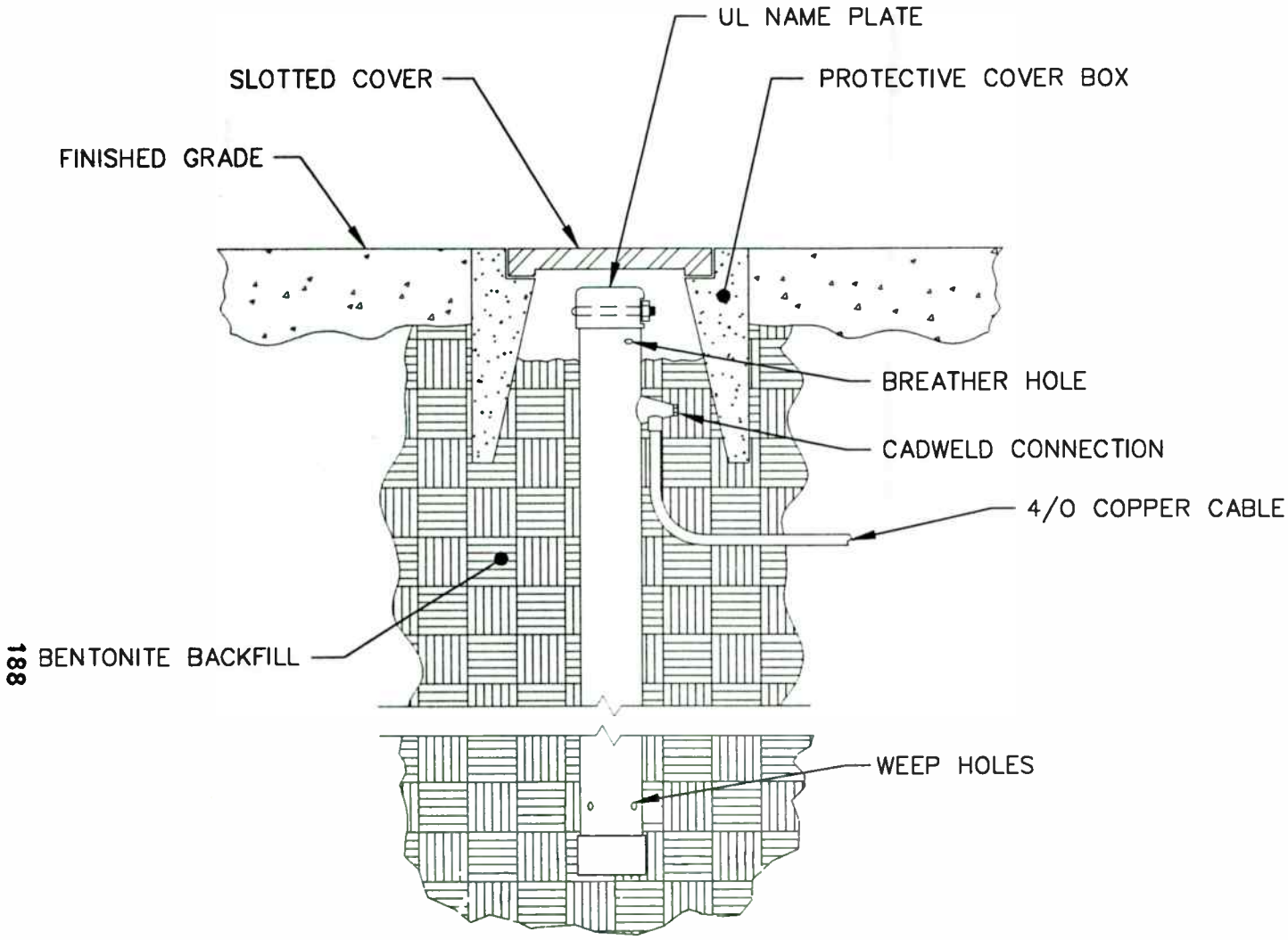
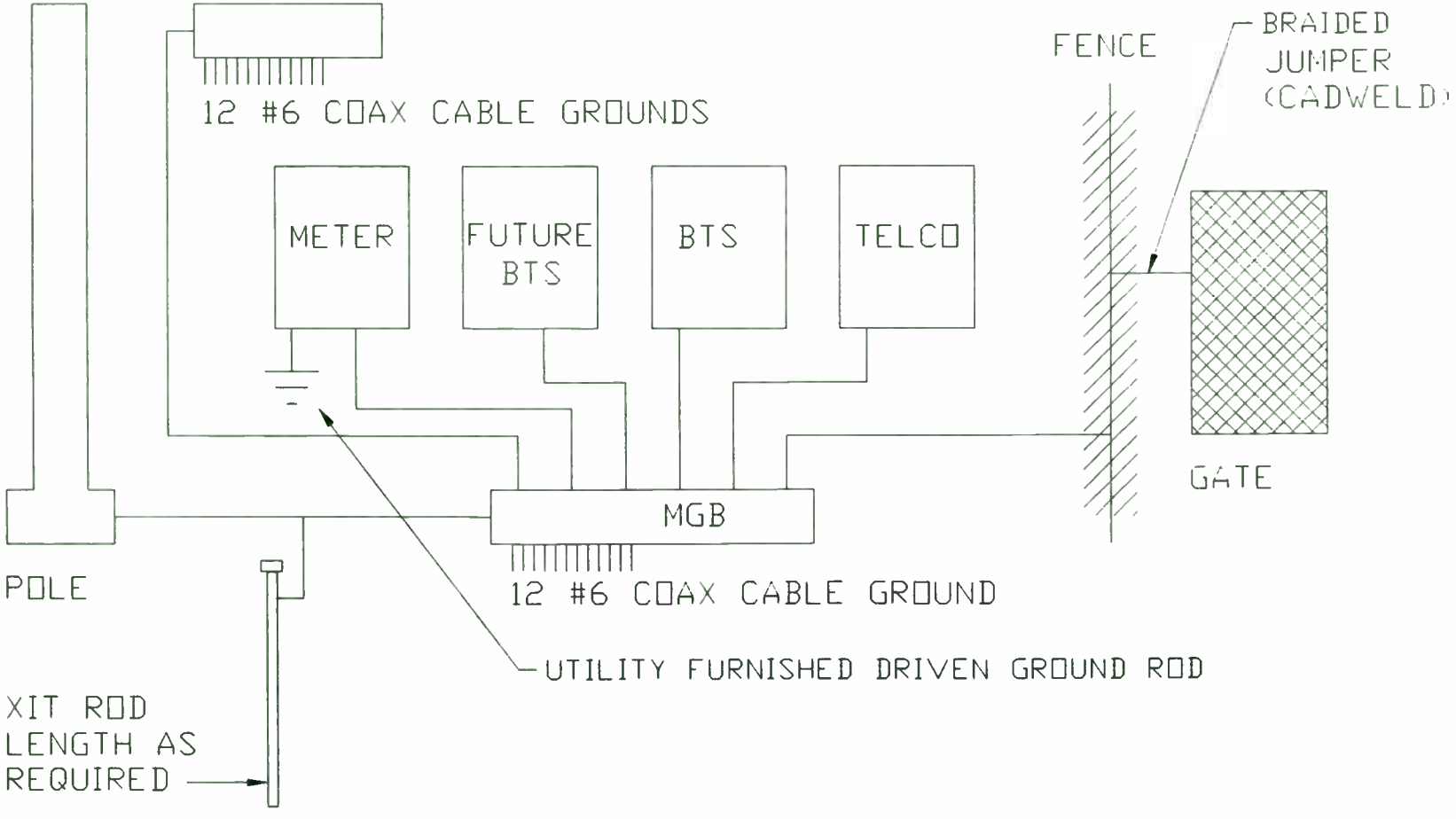


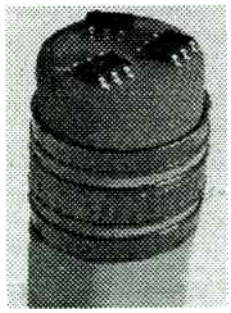
fig.1 XIT GROUNDING SYSTEM

Lyncole XIT Grounding
3547 Voyager St., Suite #104
Torrance, California 90503
(800) 962-2610

FIGURE 2. TYPICAL MONOPOLE GROUNDING SYSTEM



Miniature 3V GaAs LNA, VGA and PA for Low Cost .5-4 Ghz Wireless Applications.



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ABSTRACT

Hewlett-Packard provides quality RF and Microwave components with three goals in mind: Price, Performance, and Size. In the last two years, 5 new GaAs RFICs (amplifiers and mixers) have been released in the SC70 (SOT-363) six lead, miniature plastic package. For 1997, three more 3V RFICs are being developed for this SC70 family. These include a LNA (Low Noise amplifier), and VGA (Variable Gain Amplifier) and PA (Power Amplifier). This paper focuses on the design and utilization of these new RFICs.

INTRODUCTION

HP manufactures 5 different GaAs RFIC building blocks in the SOT-363 (SC-70) package. 3 to 5 additional blocks will be added over the next 18 months. The SOT-363 is over 80% smaller than the standard SO-8 package. Price and performance are competitive (see Table 1). All of the SC-70 building blocks are available on tape and reel.

Part Number	Desc.	Freq Range GHz	V	Cur mA	NF dB	Gn dB	I P3 dBm
IAM-91563	Down conv.	0.8-6.0	3	9	8.5	9	2.5
MGA-81563	Driver amp	0.1-6.0	3	42	2.7	12	27
MGA-82563	Driver amp	0.1-6.0	3	84	2.2	13	31
MGA-86563	LNA	1.5-6.0	5	14	1.6	22	15
MGA-87563	LNA	0.5-4.0	3	4.5	1.6	14	8
MGA-8XX63	*LNA 1997*	*0.5-6.0*	*3*	*13*	*1.6*	*19*	*13*
MGA-8XX63	*PA 1997*	*0.5-6.0*	*3*	*130*	*5.5*	*22*	*28*

Table 1. RFIC gain blocks available in miniature SOT-363 (SC70) package at Hewlett-Packard.

Each SC70 building block provides one function. Most blocks are internally matched to 50 Ω. A few (LNAs and mixers) require an external one or two element impedance match for optimum performance in a narrow frequency band. This technique of usage is appropriate since all commercial systems operate on a select frequency. The cost of incorporating the match into the integrated circuit would push the price up, and degrade the general multi-frequency usage and performance.

The miniature SC70 RFIC building blocks are designed to be the "glue" that holds the RF front end together. A typical wireless system RF section is shown in Figure 1. While the system shown could be entirely built using discrete components (FETs, transistors, diodes) this would lead to a fairly complex, hard to change design. Building blocks allow quick, compact designs that are flexible enough to be changed. This flexibility also allows future system revisions to be done quickly and modifications made easily. For example, if a designer is told he needs a better system noise figure (increase dynamic range), he can substitute an MGA-87563 for a INA-12063 in the LNA and instantly reduce the system noise figure 1 dB.

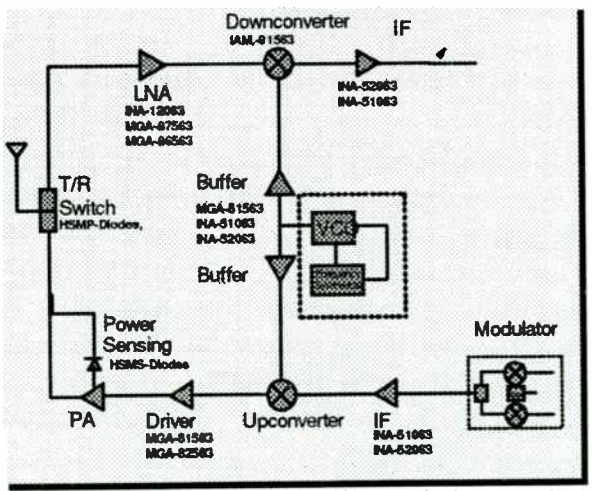

Figure 1 Typical RF design for a wireless system with target SC70 RFIC labeled

DEVICE AND FABRICATION

The devices used in this monolithic design were pseudomorphic high electron mobility transistor (PHEMT) structures built using molecular beam epotaxy (MBE) material growth techniques. The gates were defined using electron-beam

lithography. The results were lengths from 0.12 to 0.17 microns. A mushroom shaped gate was formed in order to reduce gate parasitic resistance by increasing the gate's cross sectional area.

Typical noise figures of 0.25 dB with an associated gain of 15 dB are measured at 4.0 GHz on the 200u Process Control Monitor (PCM) devices. The typical DC characteristics of these devices are an Idss of 25 mA (0.13A/mm) with a pinch off voltage of -.50V at 10% Idss and a transconductance of 66 mS at 50% Idss (330 S/mm). Typical sheet Rho for bulk GaAs material is 330 Ohms/sq with and resistive etch allowance to 350 Ohms/sq. The MIM capacitors are typically 400 pF/mm. Silicon nitride dielectric is deposited for capacitors and passivation.

Low Noise Amplifier

The LNA is designed to complement our present SC70 based LNAs, the MGA-86563 and MGA-87563. The MMIC is packaged in the standard surface mount, low cost SC-70 (SOT-363) package. Pin outs, biasing, and usage are compatible with other GaAs and Silicon building block type products. Primary use includes: 900 MHz (Cellular), 1500 MHz (GPS), 1800 MHz (DECT, PCN), 2400 MHz (ISM), 4000 MHz (Satellite/TVRO), C-Band (Aviation transponders), and full band (Instrumentation and military).

MMICs, such as this SC-70 MGA, simplify the design process of producing a stable, minimum noise LNA. The obvious advantage is that bias and voltage regulation is incorporated monolithically, thus eliminating complicated bias circuits. MMICs are normally unconditionally stable, removing stability fears for system design. Last, MMICs commonly incorporate feedback and internal matching techniques. This can eliminate or significantly reduce the complexity of external impedance matching circuits

The LNA is a two stage design that works on a single, 3V DC supply applied to the output port. The LNA will provide 18 dB gain and less than 1.7 dB noise figure. Bandwidth is 0.5 to 6.0 GHz. The output is matched to 50 Ω while the input is partially matched (3:1 VSWR) and allowing the user to finalize the noise match with a simple series inductor. A unique feature of this LNA is that the user can adjust the output power (+3dBm to +13 dBm) by adding an external resistor. Changing power (and linearity) does not effect noise figure or gain and can be done actively in a system to increase system sensitivity and dynamic range.

The LNA is two stage design as Figure 2 shows. It consists of two FET gain stages, a partial input match of feedback on the 1st stage, and a heavy feedback network on the 2nd stage. The gain stages consist of a FET; biased at 30% of Idss with the gates DC grounded. A capacitor and resistor network provide feedback on each gain stage to improve match, provide stability, and flatten gain. A shunt resistor on the 2nd stage provides the DC ground. Both stages use current sources to elevate source voltage and partially pinch-off the FETs. Separate source grounding capacitors are used as well as separate ground bonds to improve high frequency stability. The die size is approximately 0.44 mm (17.3 mils) by 0.44 mm (17.3 mils).

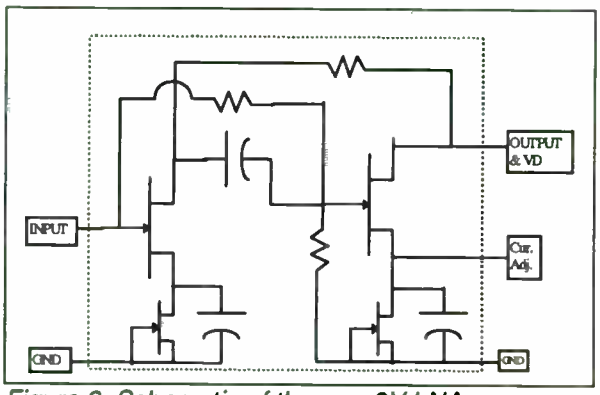

Figure 2. Schematic of the new 3V LNA

In an application the input match must be designed to present Gopt (as defined by the device noise parameters in the data sheet) at or near the frequency of interest in order to obtain the minimum noise form the amplifier. The match is easily achieved through use of a series inductor, implemented using the entire etched trace on the circuit board or a surface mount lumped inductor. at the input. The output match of the LNA is sufficiently close to 50 Ω that no additional output matching was needed to the MMIC.

For DC bias, a simple DC blocking capacitor and RF blocking inductor choke combination can be used. Values of the choke and capacitor are chosen for least amount of interference at the frequency of usage. Selection of the external bias resistor is most unique to this amplifier. In most applications the pin is simply left open, allowing the LNA to self regulate it bias to a typical 13 mA and +3dBm of output power at one dB

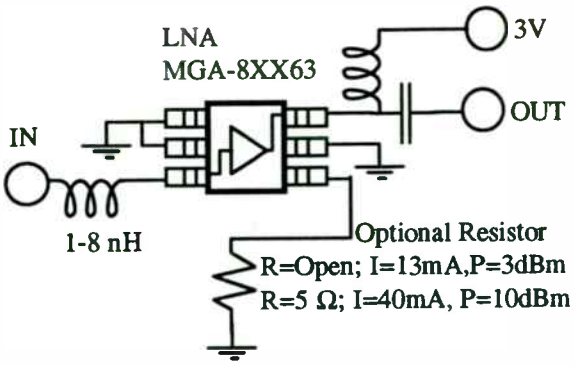

Figure 3. Typical application of the 3V LNA

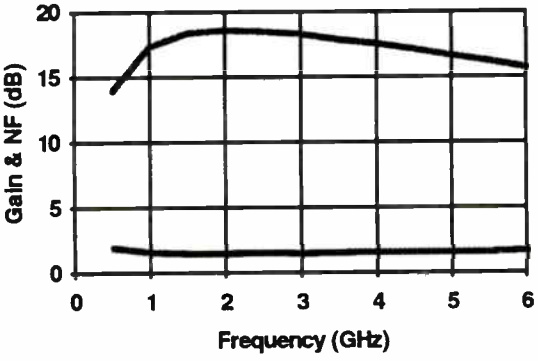

Figure 4. Typical Gain and NF of the new 3V LNA

compression. However, the user has the capability of increasing the current, hence increasing the output power, by applying different value resistors to this pin. Maximum power and current is achieved with a 5 Ω resistor resulting in a 40mA current and a +10 dBm output power. A typical application schematic of the LNA in use is shown in Figure 3.

POWER AMPLIFIER

The new PA is an extension of our popular MGA-81563 and MGA-82563 medium power amplifiers. This amplifier will provide greater than 20 dB gain and 20 dBm output power over the 0.8 to 6.0 GHz range. Input and output are internally matched to 50 Ω for small signal and linear application. Maximum power (saturated) is achieved with a simple output power match. The amplifier operates on 3.0V applied to two package pins. For saturated (transmit) applications the amplifier can be operated at 3dB compression and typically produce 200 mW (23 dBm) of power. Power added efficiency is in excess of 45%.

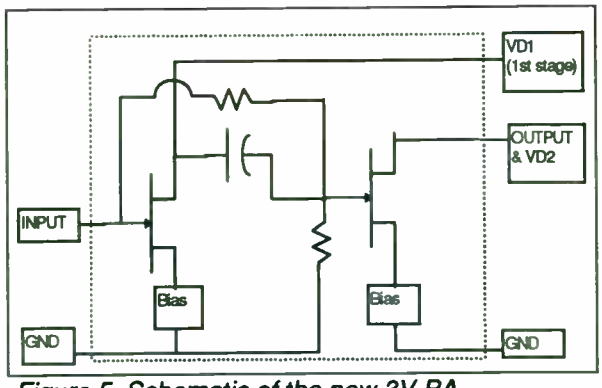

Figure 5. Schematic of the new 3V PA

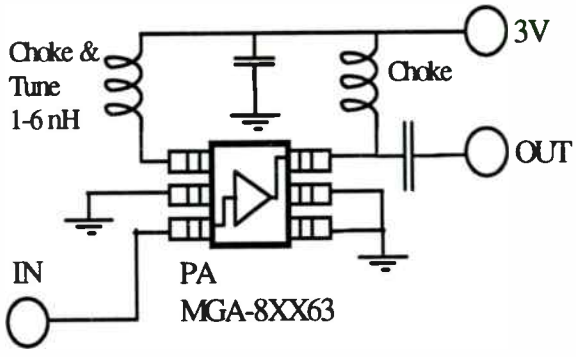

Figure 6. Typical application of the 3V PA

The 20/20 PA is classic two stage design as Figure 5 shows. It consists of two FET gain stages, full feedback on the 1st stage (for match), and open drain on the 2nd stage for maximum power. The 1st gain stage consists of a FET biased at a large percentage of Idss with the gate DC grounded. A capacitor and resistor network provide feedback on the 1st stage to improve match, provide stability, and flatten gain. The 2nd stage is a FET also biased at a large percentageof Idss. A shunt resistor on the 2nd stage provides the DC ground and lossy interstage match. A separate DC supply is used for each stage to improve stability and allow the interstage to be "tuned" for max gain and power. Separate source grounding pads and ground bonds are used to improve high frequency stability. The die size is approximately 0.44 mm (17.3 mils) by 0.36 mm (14.2 mils).

In an application, the PA is simple to use. The DC supply must be applied to two pins. These pins must be RF isolated to prevent unwanted feedback from leaking between stages. The output choke and DC blocking capacitor must be large enough and of enough quality as to prevent any interference in the application frequency. The

inductor/choke to the input stage must be chosen as to set the input match. Typical values for this inductor are in the 1 to 6 nH range, depending on the application frequency. For example, a 2.2nH inductor is used for 2.4 Ghz ISM band power amplifier. A small amount of shunt capacitance (0.5 to 2 pF) can be used on the output to improve Power-added-efficiency for high power applications. A typical application circuit is shown in Figure 6. Typical performance data is shown in Figures 7 and 8.

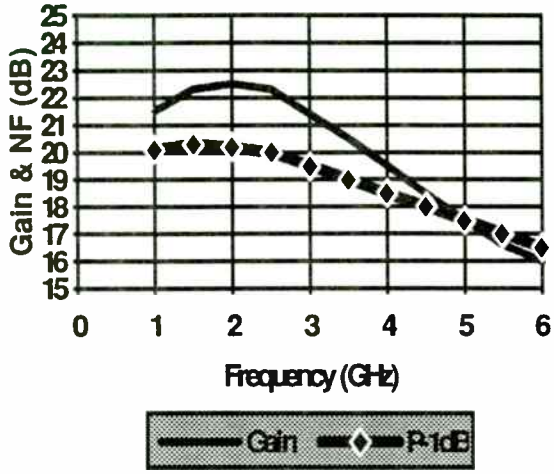

Figure 7. Typical Gain and Power of the 3V PA

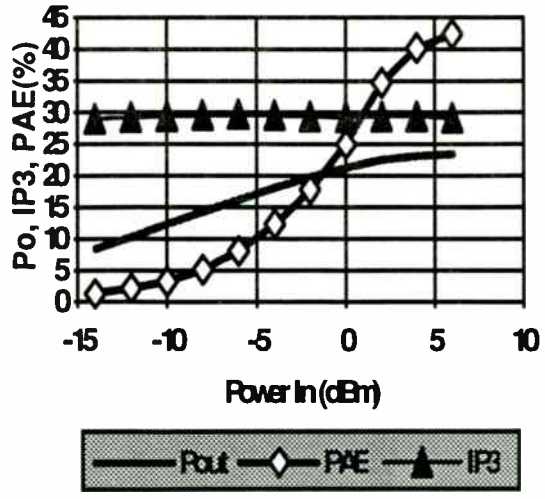

Figure 8. Typical Power, IP3, PAE of the 3V PA at 2.4 Ghz and 3.0 Volt supply.

VARIABLE GAIN AMPLIFIER

The VGA development is a departure from the rest of the SC70 GaAs family. The 3V DC is supplied through the RF output pin. Input and Output are partially matched to 50 Ω (3:1 VSWR), but are easily matched with a single inductor. Bandwidth is 0.5 to 4.0 Ghz. Gain can be varied over 20 dB with the simple application of a POSITIVE voltage (no current) to one of the SC70 pins. A +2.0V or greater voltage will achieve maximum gain state (+10 dB). A +1.0V or less will achieve maximum attenuation (-12 dB). Control voltage between +1.0V and +2.0V will select any gain state between these limits. This VGA is unique in the fact that no matter what gain state is chosen, DC current, linearity, and I/O match remains constant and stable.

The topology for the VGA was selected for it's integrated compactness as well as it's performance. A schematic is shown in Figure 9. The first stage consists of a heavily feedback common source FET with an integrated source bypass capacitor and bias setting current source. The second stage consists of two FETs in series configured with zero drain-to-source voltage so that they are essentially voltage controlled resistors. DC blocking capacitors and a voltage divider is employed to allow the drain/source voltage to be set to 2V from a 3V supply. This allows the control voltage for maximum attenuation be set at 1V (-1V gate-to-source), well beyond the -0.5V PHEMT FET pinch-off voltage. The last stage is again a heavily feedback common source FET utilizing an external source capacitor and integrated current source.

Realization of the VGA is shown in Figure 10. The die measured only 0.45mm by 0.45 mm. The VGA can be placed in even our smallest IC package (SC-70 or SOT-363 package). Figure 11 shows measured data of the VGA demonstrating the gain control over control voltage.

Figure 12 shows the input IP3 (3rd order intercept point) and gain/attenuation verses control voltage. One of the only disappointing aspect of this MMIC is that the IP3 takes a noticeable reduction in performance just as the attenuating FETs reach full pinch-off. It is postulated that this highly linearity unstable state is caused by the FET in reaching at or near pinch-off. For this reason, this VGA will likely never be released in this form.

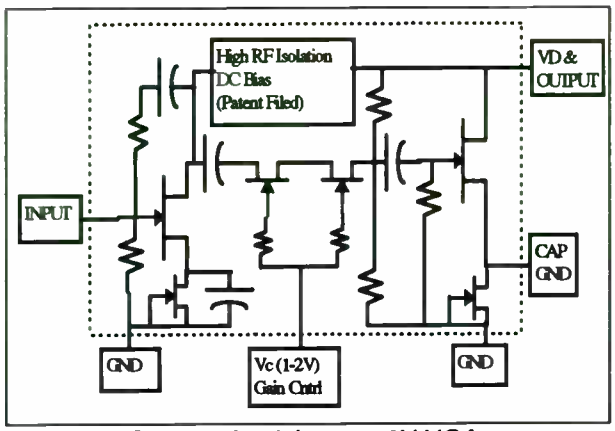

Figure 9. Schematic of the new 3V VGA

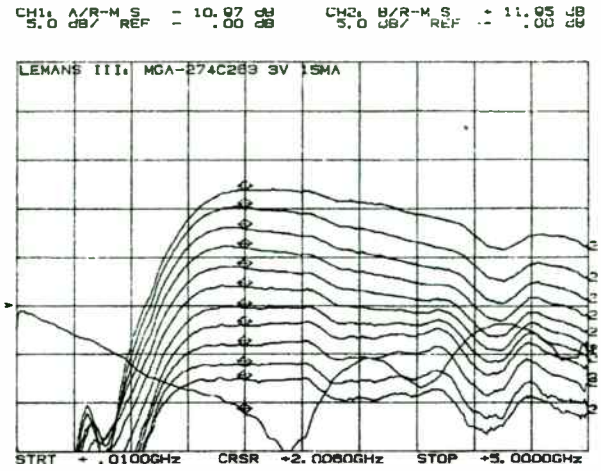

Figure 11. VGA typical package gain/attenuation.

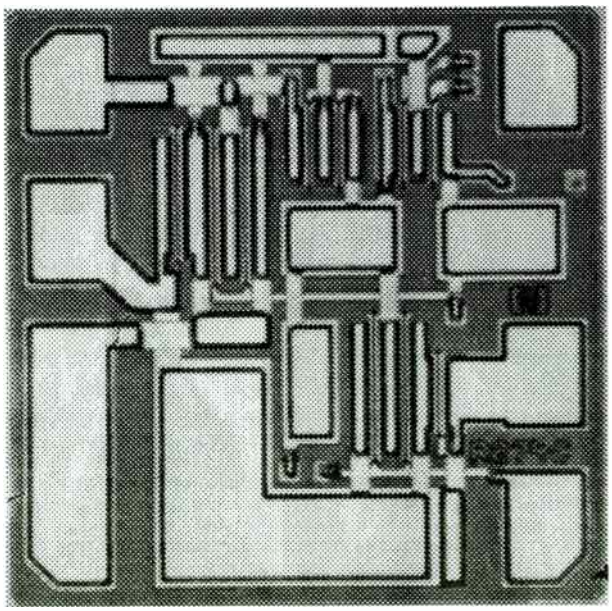

Figure 10. Photograph of VGA as fabricated.

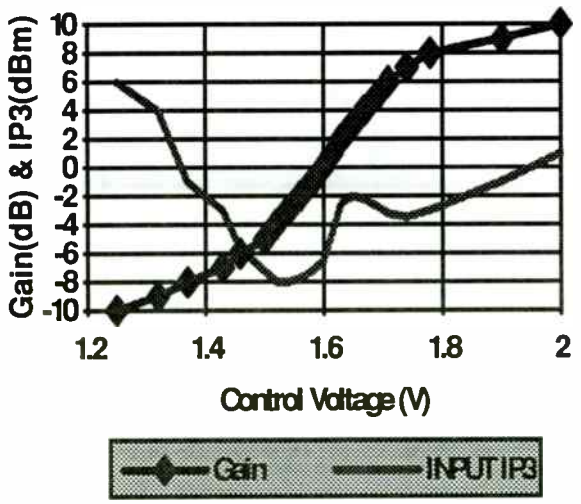

Figure 12. Input IP3 and Gain vs Control Voltage for the PHEMT MMIC VGA.

CONCLUSION

This paper has presented three GaAs PHEMT MMICs designed for usage in the SC-70 package. The LNA and PA are fully functional and will be offered to sale for commercial application in early 1997. The VGA will not be released for sale in it's present form.

All these products are designed for low cost and high volume. They complement existing HP product lines and enable system designs to design smaller, lower cost, high performance wireless systems. Special thanks is extended to: Mike Frank, Kevin Negus, John Coward, Tuan Lam, Ruben Reyes, Julie Kessler, Tson-Ming Kao, Chris Pease, Chris Siu, and Gary Carr for their diligent work and contributions to these products.

REFERENCES

1. K. Joshin, N. Hidaka, K. Hikosaka, "A High-Gain HEMT Monolithic Downconverter for X-Band Direct Broadcast Satellite Applications", *1993 IEE GaAs IC Symposium*, pp 229-232.
2. H. Morkner, N. Nguyen, A, Ward, B. Myers, G. Carr, "Design and Utilization of Wireless Monolithic Low Noise Amplifiers fot 3 Volt, Low Current Applications", *1995 RF Expo West*, Jan 1995.
3. H. Morkner, N. Nguyen, G. Carr, "Monolithic Gain Blocks in Mini-Packages for DC to 4000 MHz Wireless Hand-Held Communication", *1995 Wireless Symposium,* Feb 1995.
4. M. Williams, F. Bonn, C. Gong, T. Quach, "GaAs RF ICs Target 2.4-GHz Frequency Band", *Microwaves and RF*, July 1994, pp 111-118.
5. Stephen A. Maas, "Microwave Mixers", Artech House, INC., Dedham, MA, 1986
6. H. Morkner, M. Frank, D. Millicker, "A High Performance 1.5 dB Low Noise PHEMT MMIC Amplifier for low cost 1.5 - 8 GHz Commercial Applications", *1993 Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp 13 - 16.
7. H. Morkner, M. Frank, R. Kishimura, "A Novel MMIC PHEMT Low Noise Amplifier for GPS Applications", *1992 Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp 13-16.
8. P.M. Smith, P.C. Chao, K. Duh, L.F. Lester, B.R.Lee, and J.M. Ballingall, "Advances in HEMT Technology and Applications", *1987 IEEE MTT-S International Symposium*, p. 749.
9. M. Frank, "The Current Source as a Microwave Biasing Element", US Patent # 4,912,430.
10. M. Frank, "The 2 to 6 GHz Block GaAs MMIC Amplifier", *Microwave Journal*, Aug. 1990, pp 83-92.

A Family of 3-V Frequency Converters for 0.8-4-GHz Wireless Applications

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As the size of portable handsets continues to shrink, the use of smaller battery packs becomes more pervasive. Coupled with this trend is the need for low voltage operation, which has pushed semiconductor manufacturers to provide devices that can operate on voltages of 3 V or lower. This paper will present a family of frequency converters for wireless applications that can operate down to 2.7 V. This family, containing both upconverters and downconverters, uses some unique circuit topologies which will be discussed here. One member of this family is a double-balanced downconverter utilizing on-chip baluns to achieve a conversion gain of 5 dB and an input IP3 of 0 dBm at 1.9 GHz. Another member of this family is a single-sideband upconverter that can generate a carrier at (LO1+LO2) or (LO1-LO2); the selection is made via a CMOS input. Thus, the part is ideally suited for emerging dual-mode phones that can operate at both 900 MHz and 1.9 GHz. All parts in this family have a power-down feature that takes the supply current to below 10 μA. The ICs are manufactured using Hewlett-Packard's bipolar ISOSAT process, and are housed in MSOP-10 (Microwave Small Outline Package) plastic packages.

A Programmable Direct Sequence Spread Spectrum Pager Evaluation Board.

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Abstract—

In this paper, we present an evaluation environment built around the DIRAC, a Direct-sequence Integrated Receiver with ARM^{TM} Core. The system allows for direct sequence spread spectrum communication using 4 parallel channels with different codes of maximum length 1024. With a clock frequency of 30 MHz, the maximum chip rate is 1.8 Mchips/s per channel.

A minimal functional system consists of the spread spectrum receiver ASIC, a program ROM, a data RAM and an analog to digital converter. In addition to these minimal requirements, the evaluation board presented here contains an ISA-interface, an RS-232 interface, a general purpose parallel port and multiple logic analyzer pods for soft- and hardware debugging.

The large programmability of the functional blocks and the programmable core make the system very flexible and compatible with a vast variety of receiver-only systems.

I. Introduction

The market of consumer electronic products is driven by the demand for devices which are small, cheap and consume little power, especially if they need to be portable. This can only be achieved by high integration, often in combination with the implementation of formerly analog functionality in a digital way.

Although in the past, this did not apply to the satellite market because it was not oriented towards mass consumer production, this situation is changing rapidly, as satellite based pager and telephone systems are emerging.

In this context, the DIRAC ASIC [3] [4] was developed. The DIRAC integrates an ARM6 32-bit RISC μprocessor core together with customized DSP hardware, an SRAM for the spreading codes and a serial port. The DSP hardware consists of a band-limiting Squared Root Raised Cosine (SRRC) filter, an Intermediate Frequency (IF) down converter and a number of de-spreading correlators.

The features of the ASIC are ideal for mobile communication terminals. The core offers the benefits of a standard programmable component, such as a short design time and programmability, as well as development tools, like a C-compiler, an assembler and a debugger. The customized hardware gives the chip the extra performance, which would be very hard to get from standard components at low cost and power.

For easy evaluation of the DIRAC ASIC, a full size ISA compliant PC board has been developed which contains all necessary hardware to implement a pager application. In combination with application specific software, the DIRAC evaluation board performs all down-conversion, demodulation, de-spreading, frame extraction and user interface tasks which are necessary to convert an analog IF input signal to user data and transmit them over the serial port.

In addition, the evaluation board facilitates debugging by the provision of logic analyzer pods, allowing for convenient instruction disassembly.

The ISA-interface allows to operate the user interface, to download programs during the development phase and to evaluate the receiver performance by real-time evaluation of critical parameters of the embedded software.

A general purpose parallel port is provided for controlling external devices, e.g. for programming the frequency of an external RF down converter.

In section II, the industrial applications delivering the specifications for the system are explained. Next, the functionality of the DIRAC ASIC is discussed in section III. Then, the board hardware is outlined in section IV and the problem of receiver synchronization is explained in section V. In section VI conclusions are drawn.

II. Applications

A. The IRIS satellite application

The driving application for the design of the DIRAC was IRIS, a system for Intercontinental Retrieval of Information via Satellite [1] put forward by the European Space Agency (ESA). The service aims at world-wide non-real time delivery of messages to and from users equipped with small, low cost terminals operating in the VHF or UHF band, using one or more small Low Earth Orbit (LEO) satellites (figure 1). The system uses direct sequence spread spectrum in the down link as well as in the up link.

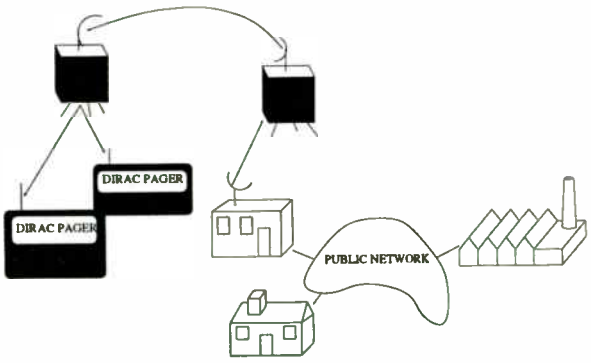

Fig. 1. *DIRAC paging in the IRIS system.*

It is possible to subscribe to the system on a cheap paging only basis, or take full advantage of the alpha-numeric bi-directional communication capability. For the latter purpose, a specific transceiver ASIC, called ASTRA, has been developed [5].

B. The MSBN satellite application

The Mobile Satellite Business Network (MSBN) [1] [2] is a program undertaken by the European Space Agency (ESA), to promote mobile satellite communications in Europe. It uses a multi-star network topology that is typically used for mobile fleet management. Each star consists out of a central point, the Fixed Earth Station (FES), from where a dispatcher can get in contact with his fleet of Mobile Earth Stations (MES). Furthermore, there is a Network Management Station (NMS) which synchronizes the different transmissions allowing a modulation technique called BLQS-CDMA (Band Limited Quasi Synchronous Code Division Multiple Access). All users are synchronized using a reference carrier that is permanently transmitted by the network management system. This technique increases the capacity of the network from 50 users to 124 users in each 1MHz satellite transponder band. It also removes the need for fast acquisition as the synchronization can be maintained even if the particular user is not receiving any messages.

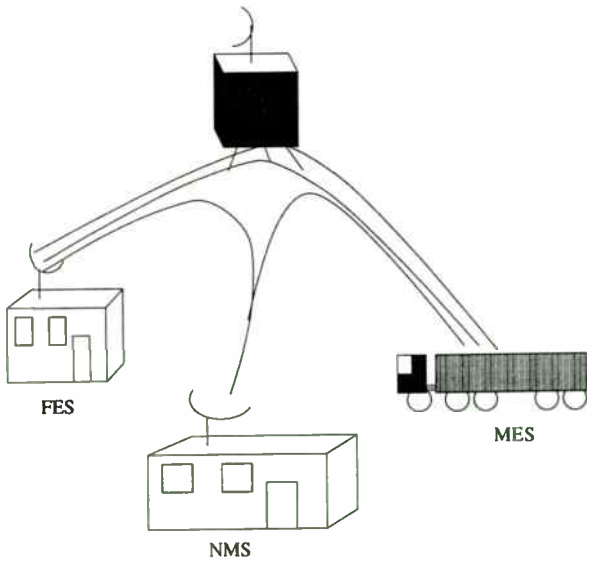

Fig. 2. *DIRAC paging in the MSBN system.*

The code length is 255. The symbol rate is 3400 symb/s with a 20 ms framing, permitting a throughput of 6400 bits/s (QPSK). As in the previous application, the service addresses cheap receive only terminals as well as complete transceivers.

C. Earth-based receiver-only applications

Although the complexity and associated high cost exclude the DIRAC from being used in simple alpha-numeric pagers, the ASIC is well suited for reception of complex data streams, especially in highly ether polluted environments. This is the case for remote video surveillance in large plants with lots of industrial equipment like oil-refinery installations in the harbor area. Another application area is the reception of data from numerous sensors (e.g. gas-flow, water-pressure, air-humidity) as parameters for process control.

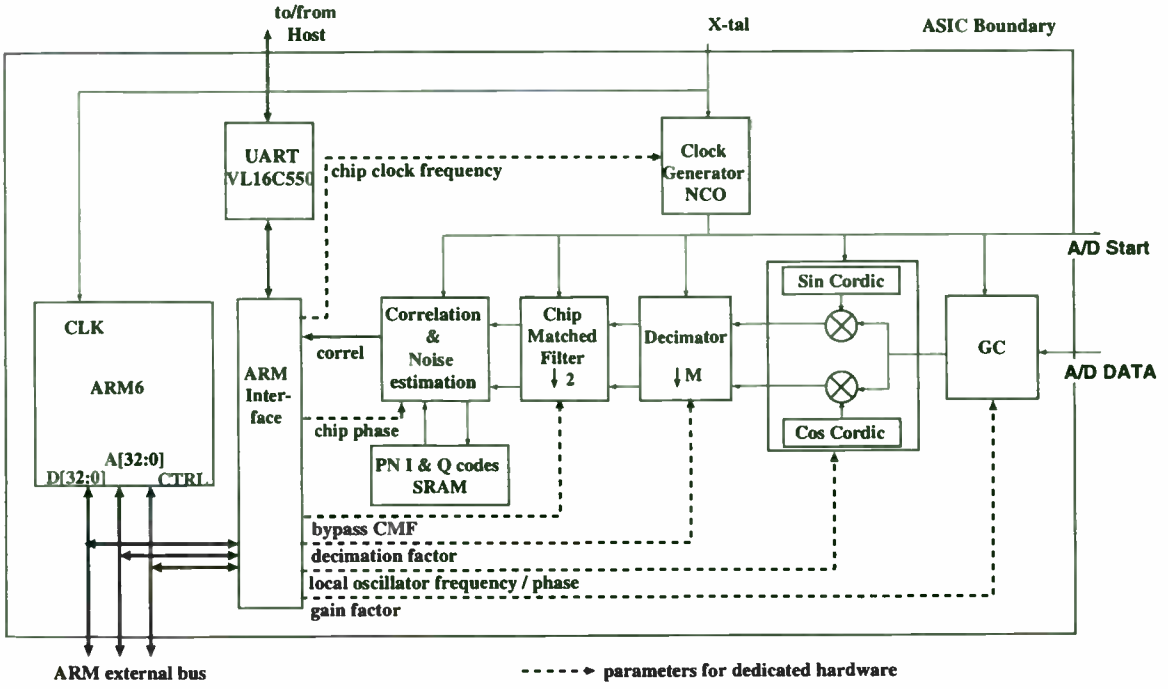

Fig. 3. *Architecture of the DIRAC.*

III. Receiver Functionality

Fig. 3 shows the block diagram of the DIRAC. It consists of the ARM6 core, the VL16C550 UART, the ARM interface and a number of dedicated interconnected DSP blocks, which will be described next.

A. Input signal sampling and leveling

The DIRAC requires an input signal with an intermediate frequency between 0 and 10 MHz. This signal is sampled with 8-bits resolution at a frequency of $8Mf_{chip}$, with M the oversampling factor and f_{chip} the chip frequency. The sample frequency and the on-chip clock are derived from an external crystal by the Clock Generator NCO, according to the chip clock frequency parameter specified by the ARM core.

Next, in the first stage of the receiver, the level of the signal is adapted in the gain control block (GC), in such a way that the full 8-bit dynamic range at the input of the down-converter is used, hence reducing the down-converters numerical noise. The gain factor is a parameter which can be set by the ARM core, allowing to implement an automatic gain control (AGC) mechanism.

B. Down-conversion and decimation

In the down-converter the signal is quadrature down-converted to baseband with an I and a Q local carrier extracted from a CORDIC, with programmable frequency. Because of the digital implementation, the frequency is very accurate and there is no settling time. This allows the down converter to eliminate Doppler shifts or frequency offsets originating from the radio link. The frequency and the phase of the local oscillator are parameters which can be controlled in real time by the software running on the ARM.

The resulting complex signal is down-sampled by the variable decimator to a rate of 8 complex samples per chip. The decimator allows to choose the spreading rates and the intermediate frequency of the incoming signal independently. Suppose the input signal is at an intermediate frequency f_{if}. In order to satisfy Nyquist's criterion, this signal has to be sampled at a rate above $2f_{if}$. Because the sample rate is given by $8Mf_{chip}$, the decimation factor M allows to achieve high f_{if} even at low f_{chip}.

C. Filtering and de-spreading

The decimated samples are fed into the Chip Matched Filter (CMF), which is a Square Rooted Raised Cosine (SRRC) filter with a roll-off of 0.4. It has a SNR of 40 dB and a spurious response suppression of 50 dBc. The 34-tap CMF realizes a down-sampling with a factor 2, down to 4 times the chip frequency. The quality of this filter allows the usage of simpler analog filters in the RF front-end.

The CMF samples are consumed in a dual de-spreader structure, de-spreading a pilot (reference) channel and a traffic (information) channel. This allows the use of synchronous CDMA. The correlations calculated, for both the I and the Q branch are with the pilot I-code, the pilot Q-code, the traffic I-code, the traffic Q-code, an early correlation with the pilot I-code and finally a late correlation with the pilot I-code. The signal strength estimator (SSE) calculates the sum of the absolute values of both the I and the Q branch. This yields a total of 12 real correlation and 2 SSE values. The local de-spreading codes are stored in an on-chip RAM and can have a length between 1 and 1024, which results in a maximum processing gain of 30.1dB. The RAM stores 4 codes, two for the pilot's I and Q branches and two for the traffic's. These codes can be swapped at runtime. The 4 codes can be correlated with the data-stream at a rate of 1.8Mc/s, resulting in a maximum chip rate of 4*1.8Mc/s.

D. Interface Architecture

The ARM communicates with the DSP accelerators via its interface. The latter can store 12 correlations and 2 SSE values, all 16 bit wide, and 14 parameters of different length controlling the DSP hardware, e.g. carrier frequency and phase, decimating factor, GC value.

This allows ARM I/O without wait-states, leaving a maximum of cycles for the users algorithms.

IV. Evaluation board hardware

Fig. 4 shows the block diagram and physical layout of the PC evaluation board.

A. PCB components

In the upper left corner of the board a DB9 connector and DC-DC conversion hardware are provided which allow connecting the on chip UART to external devices using a standard RS-232 serial interface. Further down, a coaxial input feeds the spread spectrum IF signal to the analog to digital converter (ADC), which is connected to the DIRAC via a dedicated 8 bit bus.

At the left center, a Field Programmable Gate Array (FPGA) can be found, which implements a 16 bit ISA interface. It also handles ISA interrupts and provides DMA support. The FPGA can be programmed from an EPROM at boot-time, or from a host via a serial interface. The programming mode is controlled by the switch on the lower left corner. In addition, tri-state buffers make the physical interconnection with the ISA-bus, as a safety barrier against faulty programming. Below, a pair of 8-bit FIFOs with a depth of 1024, acting as a single 16-bit wide device, has been provided for outgoing data. This allows zero wait states for the DIRAC when writing to the interface. It also makes it possible to write all the correlation values for real-time display and debugging purposes to the ISA-bus without having to wait.

Below the FIFOs, a fast 133 MHz Electrical Erasable Programmable Logic Device (EEPLD) takes care of the address decoding for the memory mapped components, as well as the ARM interrupt priority decoding and the signal level control during the booting sequence. The in system programmability capability offers a very fast and convenient way to implement changes to the behavior of the EEPLD.

At the bottom to the right of the center, the DIRAC is located, clocked by a 30 MHz reference clock. To assure a stable address during a complete clock cycle, the address bus is latched. A 32 bit wide data bus is used for communication with 128k words 1 wait state static RAM (20 ns) and with 128k words of EPROM (70 ns) containing the debugger software and the user program. Both memories are composed out of 8-bit wide components. The user program is copied to RAM at boot time, but the debugger is accessed directly from EPROM.

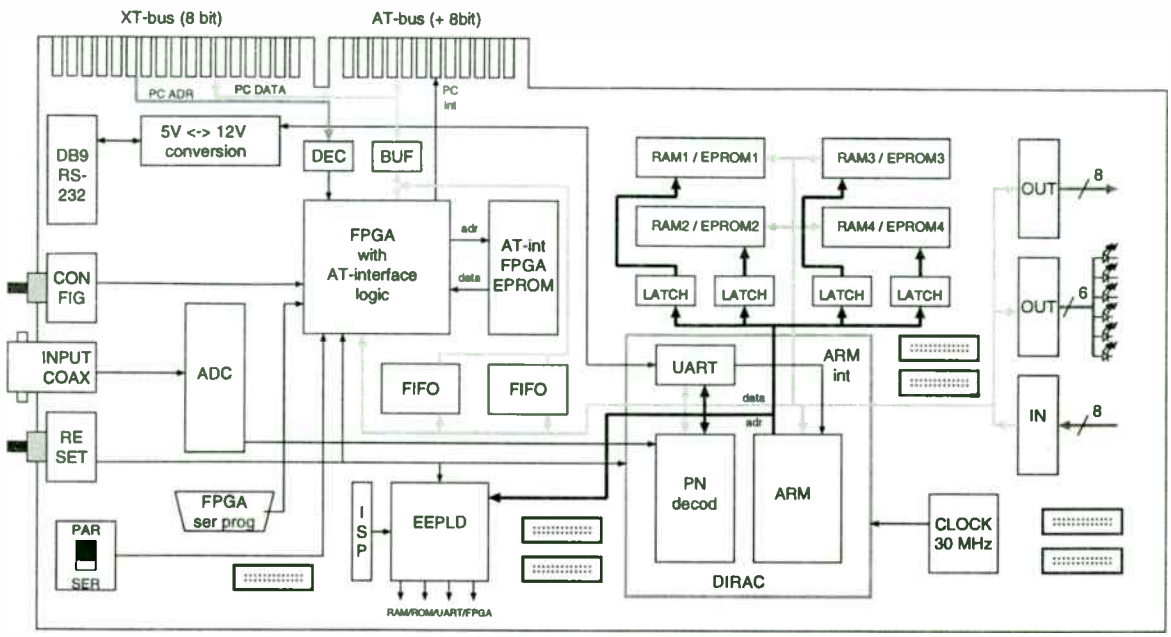

Fig. 4. *Evaluation board diagram*

At the right, a separate 8 bit parallel input and output bus for communication with external devices, as well as 6 programmable LEDs for visual feedback have been provided. The address decoding to access the ports is performed by the FPGA.

Finally, seven 20-pin logic analyzer PODS allow for easy access to the processor's control lines, data & address bus, the sampled ADC data output and a number of signals to monitor the operation on the ISA-bus.

B. The ISA interface

The internal structure of the ISA-interface is shown in Fig. 5. It consists of two sets of three 8-bit registers. The first register if for status feedback, the second for data storage and the third for controlling the internal behavior. For readability, the drawing has been simplified by removing the internal logic for updating the flags of the status registers as well as for generating interrupts.

The interface access is controlled by a 2 bit wide address bus, a pair of read and write lines and a chip select signal indicating when the data on the former lines is valid.

Viewed from the ARM-bus, the ISA-interface consists of a separate PC-data register for input and an ARM-data register for output, which are mapped to the same address. Writing to the ARM-data register will set the data output available (DOAV) bit in the PC-status register. When the interrupt to the PC is not masked, it will also generate an interrupt request (IRQ#). To check what caused the interrupt, the PC has to evaluate the contents of the PC-status register. The DOAV bit will be cleared when the PC reads the ARM-data register and will cause the data output acknowledge bit to be set in the ARM-status register (DOACK), informing the ARM that the data has been read. The DOACK bit is cleared again on the occasion of a subsequent write to the ARM-data register.

A similar mechanism is used for writing from the PC-side.

This type of 1 line deep memory interface is well suited for polled or interrupt driven user interface interaction. For debugging purposes of large chunks of data, without sacrificing the performance of the program running on the ARM, data can be written to the 1024x16-bit FIFO. To allow zero wait state interaction, the FIFO address is decoded by the EEPLD and not by the FPGA. From the ISA-interface, reading is performed through the FPGA. Depending on the needs, an interrupt can be generated on not-empty, half-full or full conditions or a polling

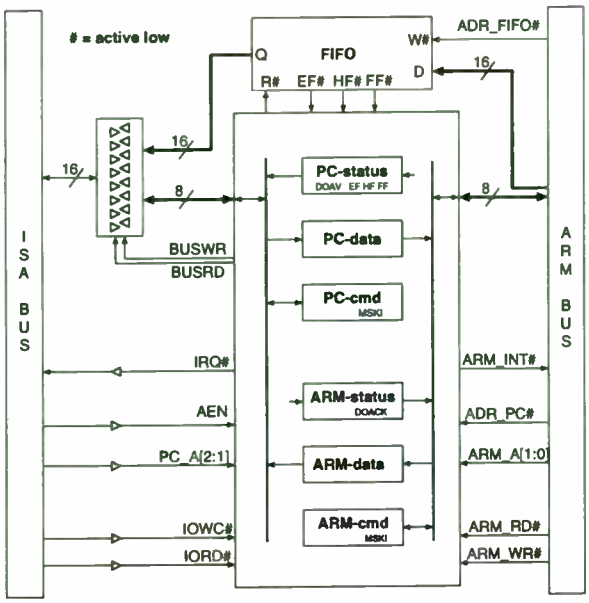

Fig. 5. *ISA interface internal structure*

mechanism can be used to check the contents of the PC-status register.

The cmd register is read/write, which allows to check the settings which influence the internal behavior. The status register is read-only as the contents are completely dependent on the operations that occurred on the interface.

V. Receiver synchronization

A. Definition

Synchronization is a 3 step sequential process of acquisition, tracking and framing. Through *acquisition* a course synchronization of the local carrier and de-spreading code is obtained. Directly following the acquisition, *tracking* locks or fine tunes the local carrier and code to obtain almost perfect synchronization. Next, *framing* locates the data packet starting point which makes it possible to start interpreting the incoming data.

The synchronization is performed in software and is one of the major tasks of the ARM, next to the user-interface implementation.

The working principle is explained in the state diagram of Fig. 6.

In the *unlocked* state, the received code is totally uncorrelated with the locally generated code. After acquisition, both codes are aligned or *locked*. In this new state, the tracking and

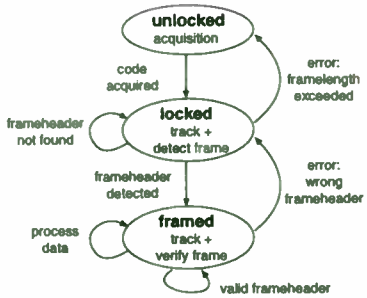

Fig. 6. *Synchronization process state diagram*

framing routines are executed on interrupt driven basis at every de-spread symbol, trying to detect the start of the frame. The moment the frame header is detected, the system moves on to the *framed* state. However, if the header was not found within 1 frame length, the system returns to the unlocked state. In the framed state, the data bits are passed on to the users application for interpretation. Tracking and framing are executed at every de-spread symbol. If the verification of the frame header at the expected position is successful, the system persists in this state. If not, it backtracks one level to the locked state.

In the next two sections, the acquisition and tracking procedures are explained in detail.

B. Acquisition

First, synchronization of the local and the received carrier is obtained by means of an FFT on the correlated data. Because of the low bit rate (typically 4800 bits/s), the frequency window is small (2.4 kHz). If this is not sufficient, multiple FFTs at subsequent local carrier frequencies must be performed.

Second, the code is acquired by means of a a *sliding correlator*. In this mechanism, the correlation peak is located for the programmed parameter set by shifting the pn code with steps of 1/2 chip over the received signal, storing the position of the maximal correlation value. At the end of this operation the pn-code is shifted to the location of the peak and the *locked* state is assumed.

The minimal acquisition time is determined by the pn-code length, the precision and the number of correlators. In this case three correlations are performed simultaneously with 1/2 step resolution (Early, Middle, Late), leading to an average acquisition time of 2 * (pn-code length) / 3 chips.

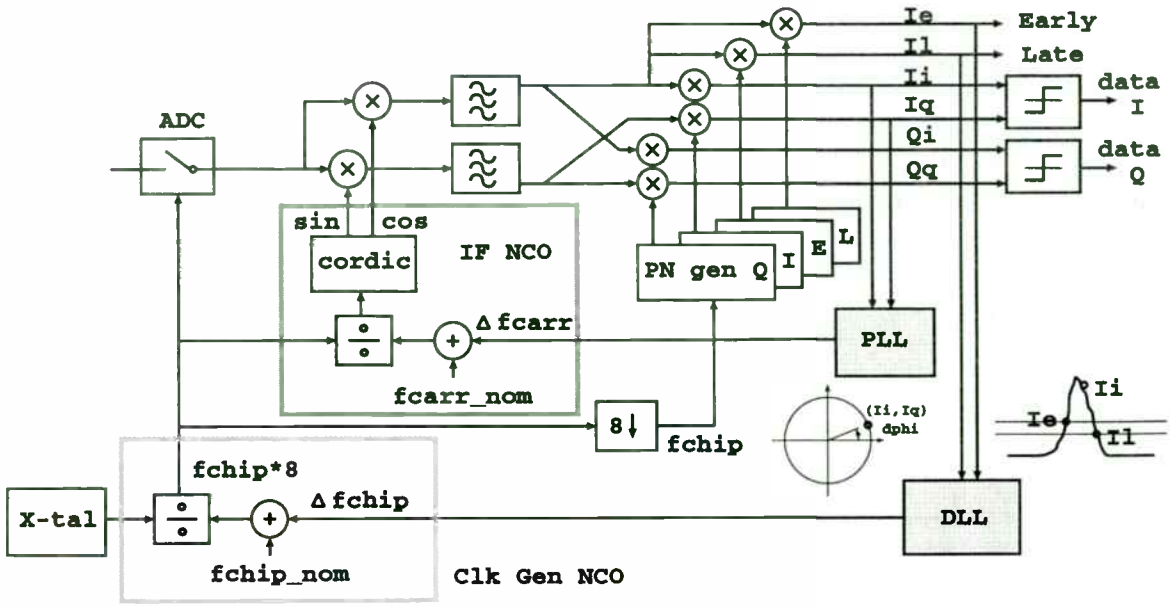

Fig. 7. *Tracking block diagram*

C. Tracking

For tracking, the IF carrier frequency and the chip frequency must be fine tuned. How this is achieved is schematically shown in Fig. 7. At the left side, the incoming signal is sampled by the ADC. The sampling frequency is generated by the clock generator Numerical Controlled Oscillator (NCO) in the lower left corner. The IF carrier frequency is generated by the IF NCO, which takes its reference clock from the the first NCO. The correlators run at fchip which is directly related to the sampling clock by a factor 1/8. Six correlators are shown: A complex correlator for I, one for Q and an Early (-1/2 chip) and Late (+1/2 chip) correlation with I. The correlation values are used to control the respective NCOs by means of a feedback control loop implemented in software.

The outer loop uses 3 correlation values shifted over 1/2 chip to control the chip frequency. The difference in the early (Ie) and late (Il) correlation values is used as input to a DLL, which increments or decrements the sampling frequency. It can be seen intuitively that shifting the sampling instance will shift the middle correlation value (Ii) exactly to the top of the correlation peak.

The inner loop adjusts the IF carrier frequency to avoid any resulting modulation in the down converted signal. As modulation shows up in the correlation plot as a rotation of the I-Q vector constellation over time, the phase difference between two subsequent correlations of I gives an indication of the carrier offset. The relative angle between the current and the former correlation of I can thus be used as an input to a PLL which adjusts the down conversion frequency accordingly to obtain zero phase shift. The absolute position of the I and Q vector must be corrected by an additional software rotation to the origin.

VI. Conclusions

A direct sequence spread spectrum evaluation board has been developed which accepts an analog low IF signal and demodulates it into a digital data stream. Due to the high programmability and the extensive debugging facilities, the system allows for real time performance evaluation of different modulation schemes, pseudo noise codes and code lengths, as well as various acquisition and tracking schemes. The ISA-interface assures PC-compatibility and provides high speed and convenient access for programming and debugging.

VII. Acknowledgments

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The authors wish to acknowledge the contributions from Bart Vanhoof at IMEC, from the engineers at SAIT Devlonics for their expert knowledge in the design of satellite systems and the WDN division of ESTEC, Noordwijk for the support and funding of the DIRAC ASIC as part of the SCADES-II project. Marc Engels is a Senior Research Assistant of the NFWO.

REFERENCES

[1] C. Van Himbeeck, "The use of CDMA in European Mobile Satellite Communication Systems", *ISSSTA '94, Proceedings IEEE Third International Symposium on Spread Spectrum Techniques and Applications*, Oulu, Finland, p. 381-385 vol. 2, July 4-6, 1994.

[2] L. Philips, I. Bolsens and H. De Man "A Programmable CDMA IF Transceiver ASIC for Wireless Communications" *CICC '95, Proceedings IEEE Custom Integrated Circuit Conference*, Santa Clara, CA, USA, p. 307-310, May , 1995.

[3] B. Gyselickx, M. Engels, I. Bolsens "Design of an ARM Core Based Direct Sequence Spread Spectrum Receiver" *Proceedings of the EMSYS96-OMI 6th annual conference*, September 1996.

[4] B. Gyselickx, M. Engels, I. Bolsens "A flexible Direct Sequence Integrated Receiver with ARM core" *9th Annual IEEE International ASIC Conference*, Sept. 23-27, Hyatt Regency Rochester, USA, pp. 93-96, 1996.

[5] R. De Wulf, M. Wouters, V. Derudder, M. Engels, I. Bolsens "A programmable CDMA IF system fro satellite communications" *Int. Conference on Signal Processing Applications and Technology, ICSPAT 96*, October 7-10, Boston, USA, p. 1545-1549, 1996.

TITLE: "USING SILICON FOR HIGH POWER PCS"

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I. ABSTRACT

The recent availability of the PCS (Personal Communications Service) in the 1.8 to 2.0 GHz frequency band has created a demand for high power linear solid state amplifier devices operating in this frequency range. The requirement is for Base station amplifiers which provide power in the order of 100 Watts with low Spectral Regrowth for GSM, TDMA and CDMA service. Available solid state power amplifier devices, GaAs MESFET, Silicon BiPolar transistor and the MOSFET are described and compared.

II. INTRODUCTION

The paper will describe the solid state device technology available for use by high power linear base station amplifier designers. The available devices include the GaAs FET amplifier and the Silicon MOSFET amplifier.

The application of solid state devices in the design of linear power amplifiers in the 1900 MHZ PCS band is discussed. Applications include base station linear amplifiers for the GSM (Global System for Mobile Communications), NADC (North American Digital Cellular), TDMA (Time Division Multiple Access), and CDMA (Code Division Multiple Access) systems.
Devices available to the designer include:

GaAs FET (MESFET) amplifier

Silicon BiPolar transistors

Silicon MOSFET transistors

This presentation provides a detailed look at some of the most recent high power BiPolar transistors and their capability to perform in line with the demands of the PCS system. The BiPolar transistors discussed are a high power Class A driver with 12 Watts at P1dB and a Class AB transistor with 60 Watts at P1dB. A basic module using the 12 Watt part to drive the 60 Watt transistor is evaluated.

III. GaAs FET (MESFET) Devices

3.1 GaAs FET -- advantages Since the introduction of the power GaAs FET on 1973, it has excelled as a RF power amplifier when compared to all other technologies. It exhibits the highest gain, highest power added efficiency and highest power output available at microwave frequencies. The basic physical properties which Gallium Arsenide possess allow it to have very high majority carrier mobility, therefore high gain-bandwidth products are realizable. These basic properties will allow the GaAs FET to remain the leader of the solid state microwave power amplifier devices. The nearest silicon class of competitors include the Silicon BiPolar transistor and the Silicon MOSFET.

The GaAs FET amplifier also has very low distortion characteristics. This is true since the device is typically biased in the Class A mode of operation; i.e., 360 degree drain conduction angle. Class A operation allows for a non switching, low cross over distortion mode of operation. Only when the amplifier is operated near the 1 dB compression point, is the device in the partial cutoff mode. This is termed the Class AB mode, when the conduction angle is less than 360 degrees and is typically more than 270 degrees.

Power GaAs FET Linearity is usually listed on the data sheet as a curve of Output Power vs Input Power. The curve for the Fujitsu Model FLL300IL-1 is shown below:

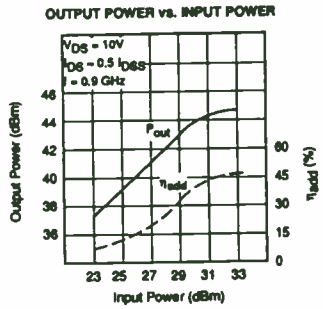


Fig 1. Output Power vs Input Power for FLL300IL

The physical properties of the gallium arsenide material allow amplifiers to be designed using a low power supply voltage, typically 8 to 10 Volts. Fully Integrated small signal receiver units can be designed to operate using a supply as low as 2 to 3 Volts with exceptional noise figure and very attractive gain per stage. Most all Microwave receivers use the GaAs FET - MMIC - technology at this time, including the popular 900 MHZ cellular radios.

3.2 GaAs FET --Disadvantages

The very feature, low supply Voltage, which make the GaAs FET desirable as a lower power, low noise figure amplifier reduces the performance as a high power amplifier. The fact that it must be operated at a low power supply Voltage demand very high currents and therefore very high current density in the package and outputs circuits. At a given power level the output impedance of the drain becomes very low thus limiting the bandwidth. Required matching stages become more sophisticated.

The amplifier is generally limited to Class A mode of operation because of the low gate-drain junction breakdown voltage, typically less than 5 Volts. When the amplifier is driven with power levels that approach the 1 dB saturation level and therefore approaching the class AB mode, the gate junction will start to conduct and gate currents will flow. This current can damage a high frequency MESFET because of the very fine lithography used in the fabrication. The current density in the metal feeds can be excessive.

The GaAs FET amplifier chip configuration allows lower power density. The GaAs FET utilizes a lateral geometry. This lateral geometry does not allow the high-power density that an equivalent BiPolar device can utilize. The power dissipation is located on the surface of the chip and GaAs is a poorer thermal conductor, thereby requiring a very thin chip. The thickness, for better thermal conduction, is typically about 25 microns, the thinner material is more difficult to handle through the assembly process as the chip gets larger, thereby forcing the designer to work with lower power per chip, more chips in the package for a given power level. The GaAs process technology incorporates sub-micron dimensions and air insulated metal bridges. This forces very tight photolithographic processing and wafers which are susceptible to surface damage in subsequent processes.

The GaAs FET amplifier requires tender loving care in order to maintain full performance and not have it 'self destruct'. The circuit designer must incorporate a tight control of the gate bias as part of the overall design.

The GaAs FET amplifier cannot <u>really</u> be operated in a low conduction angle, high efficiency mode of operation.

High Price. For a variety of reasons, the GaAs FET amplifier device commands a substantially higher price than the Silicon BiPolar transistor. One reason has been the price and availability of the basic Gallium Arsenide wafers. This material is more difficult to produce in the high purity state required for fabrication of the devices compared to the relatively common Silicon wafers. The processing of the GaAs wafers is more complex and likely more expensive, the assembly of the final transistor requires elaborate handling and therefore more expensive. These items add to the overall cost of the finished device.

IV. SILICON BiPolar Transistors

4.1 SILICON BiPolar Advantages

The 2.0 GHz Silicon BiPolar device is now competitive with GaAs FET devices! Power Gain is nearly equal and Supply Voltage is Higher - providing products with much higher power levels. Power Gain is still lower than the GaAs FET but has improved in the past year - yielding 9 to 10 dB available at 60 Watts class AB. P1dB exceeds 60 Watts Class AB at 2.0 GHz using a 25 Volt power supply . 12 Watts of Class A power is available from the 1920A12 yielding better than 10 dB power gain. Power efficiency is also very near to the GaAs FET device.

The Silicon BiPolar transistor CAN be operated in a cutoff mode. (The GaAs FET amplifier can require tender loving care when driven into the Class AB mode of operation.) This allows Class AB, Class B, and Class C operation. Class AB operation allows higher power output than Class A mode with the same size semiconductor chip . Class C mode of operation is available for use with some GSM application resulting in very high power where the requirement for low distortion is less demanding.

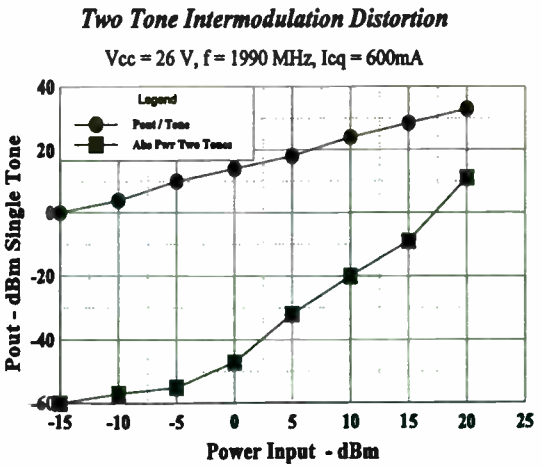


Fig 2. 1920A05 Two tone IP3 Curve

Allowable BiPolar transistor power density is higher than the GaAs FET design. Due to the fact that BiPolar current flow is vertical through the bulk material, BiPolar transistors can produce very high power density, resulting in reduced package size for the same power device. Silicon chip sizes are larger, therefore fewer chips are required in a high power transistor. The GaAs FET is a lateral design, the device is formed along the surface of the material.

The Silicon BiPolar transistor generates lower phase noise than the GaAs FET. This fact makes the BiPolar valuable for use as a power oscillator. As early as 1986 a BiPolar power oscillator transistor had been produced with a fundamental oscillation (f_{max}) frequency of 26 GHz. It was useful because of the very low spectral noise power near the carrier frequency.

High junction breakdowns allow higher power supply voltages. Power supply voltage equal to 28 Volts is typical, and 35 Volts is practical. Higher output impedances is the result, allowing wider bandwidth. Reduced collector current results in a less bulky power supply requirement at similar RF power levels.

Silicon as a material has been in production for nearly 50 years and is well understood. The performance and reliability capability of Silicon is well documented and a number of suppliers are on the market with product. The availability and cost weigh in favor of Silicon as the base material.

Advances in fabrication techniques resulting in submicron lithography, are allowing higher gain and efficiency BiPolar devices to be produced. At the same time new Class A BiPolar devices are being introduced that make use of these advances.

4.2 SILICON BiPolar - Disadvantages

Small Signal Gain - The silicon BiPolar is inherently a lower gain structure - it will always have a Small Signal gain which is less than the GaAs MESFET device.

Limited Dynamic Range - The Silicon BiPolar will have a dynamic range which is of the order of 8 dB when operated Class AB - does not have this restriction when operated Class A.

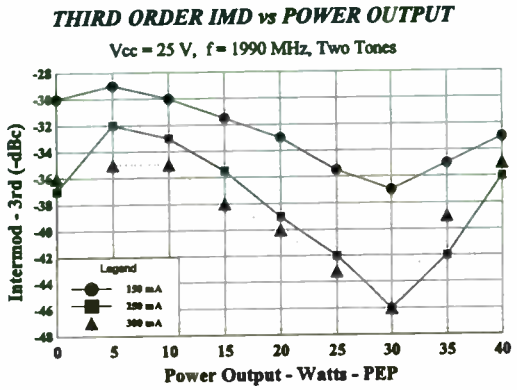


Fig 3. 1920AB35 Intermodulation Distortion

Higher Voltage of Operation - The Silicon BiPolar is of limited use under 5 Volts - however designs can be made to operate at Voltages as high as 35 Volts.

V. SILICON MOSFET Transistors

5.1 Traditional D-MOS

Silicon MOSFET devices started in the VHF bands in the early 1980's and are being used in applications up to 500 MHz. In addition, they been used recently for some RF power amplifiers in service for the Cellular 900 MHz band using transistors with Power Output of 30 Watts, when the high Volume BiPolar will provide 150 Watts. They offer high gain, good power efficiency, and are priced competitive to the BiPolar transistors.

They share the advantage of the higher Supply Voltage of Silicon BiPolar - however as an enhancement mode device, the chip is larger than the BiPolar for the same power level and the bandwidth is limited by the interelectrode capacitance - Crss. Each vendor has selected a design approach which best fits their processing and therefore there is no 'Industry Standard' design which is widely used and therefore little 'second sourcing' available at this time.

At this time it appears unlikely that there will be DMOS devices for use at 2 GHz.

5.2 Lateral D-MOS

This is a relative new comer to the RF Device world. The concept is to build the active transistor on the top surface and use Via Connections through the silicon to have the backside of the silicon become the Source. This will allow for a Common Source package which eliminates the BeO - insulating ceramic - of the traditional package. This should improve the performance of the transistor and reduce the cost of the package. There has been considerable development on this product technology for the past 8 to 10 years - initiated in Japan. Recently some of the Power Transistor suppliers are offering LD-MOS transistors for use in the 1.8 - 2.0 GHz band.

A very recent paper, [6] given at IEDM, International Electron Devices Meeting - San Francisco, (Dec. '96) gave details of the state of the art in LDMOS devices.

The gain could be somewhat higher, the distortion could be in the ballpark compared to a silicon BiPolar device. Additional operating data is required in order to determine how suitable this product will be for PCS applications.

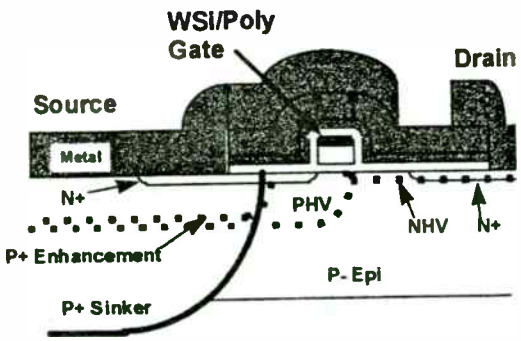


Fig 4. LDMOS Cross Section for 1 gate finger

VI. PCS Linear Device Performance - BiPolar

6.1 - 12 Watt Class A Amplifier

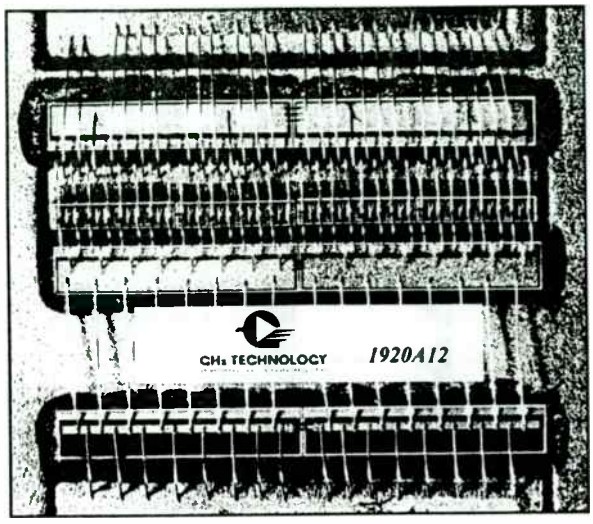


Fig 5. 1920A12-- BiPolar Class AB Transistor

The 12 Watt Class A transistor consists of 32 active Cell pairs - each capable of approximately one half watt output. In addition, the transistor includes a two step input match and a collector resonant output match. The transistor will operate over the entire 200 MHz bandwidth.

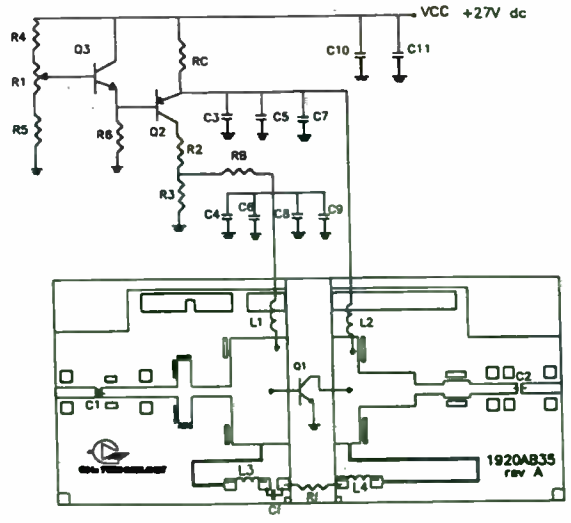


Fig 6. 1920A12 Class A test circuit schematic

Linearity tests have been conducted with the transistor in a single stage test fixture. The results have been compared - both using the Noise Com CDMA Simulator and the HP Channel Power tests. The results confirm that the performance of the Class A BiPolar is very close to the GaAs MESFET.

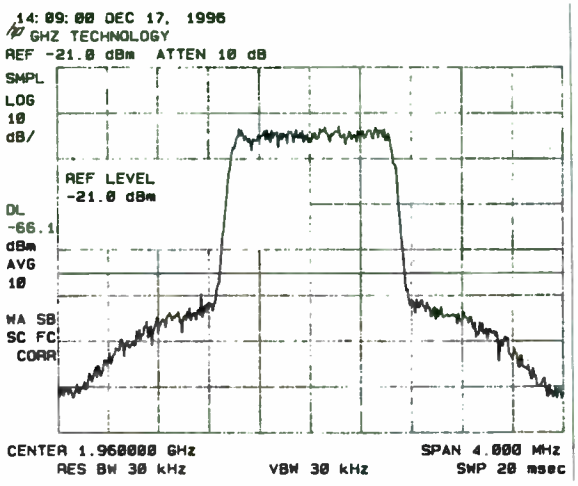


Fig 7. Spectral Regrowth of 1920A12 at 2.5 Watt Power Average - using Noise Com CDMA Simulator.

6.2 35 Watt Class AB stage - 1920AB35

High power Class AB transistors are used in the final stages of the linear amplifier. A broadband part for the application at the 35 Watt level is the 1920AB35. The broadband circuit for this device.

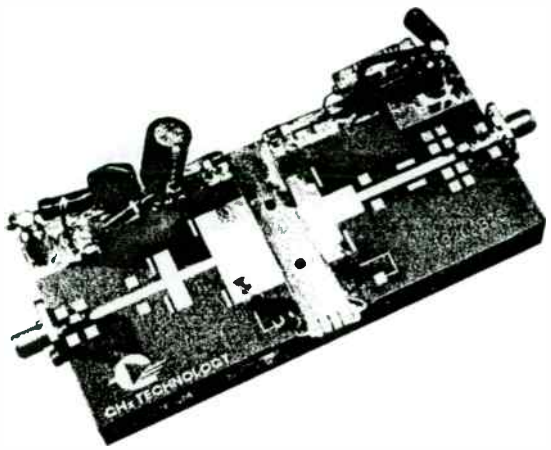


Fig8. Test Circuit for 1920AB35

Tests under the CDMA modulation scheme have yielded quite good performance as shown by the following figure. The drive source was very clean and the noise power is measured in the 30 kHz channels shown.

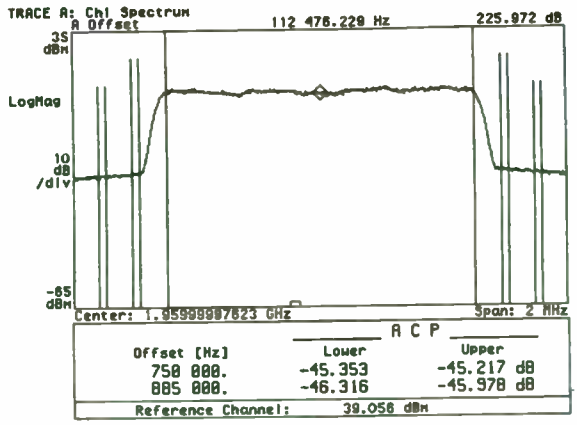
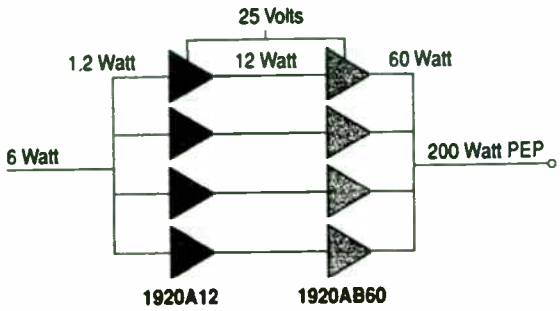


Fig 9. CDMA Adjacent Channel Power for 1920AB35 driven by SA1056 Amp, power level is 8 Watts average.

The CDMA Adjacent Channel Power is shown to be-45.2 dBc when 750 kHz from the center of the 1.23 MHz channel.

6.3 The 60 Watt 25 Volt Power Module

A high power amplifier may consist of several transistors combined in the final stage. One approach is to build a module consisting of a Class A driver and high power Class AB final stage. This module is combined in an array of four for a high power sub assembly.



The example shown consists of a combined set of four (4) modules.

Fig 10. Example High Power Amplifier

Measurements have been made on a single module for Adjacent Channel Power. This module consisted of a single 12 Watt Class A transistor stage driving a single 60 Watt Class AB

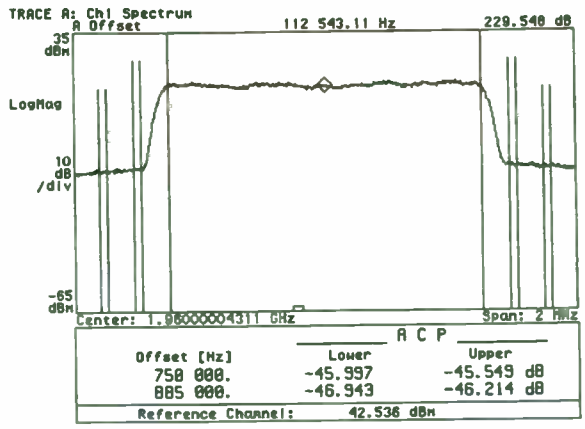


Fig 11. Adjacent Channel Power for a 2 stage amplifier - 1920A12 driving 1920AB60, driven by SA1056. Power Level at 18 Watts Average.

VII. LDMOS Transistor capability

The latest information presented at the IEDM shows the Intermodulation distortion provide for a 30 Watt LDMOS transistor. The data shows that it has a response similar to that of the BiPolar transistor.

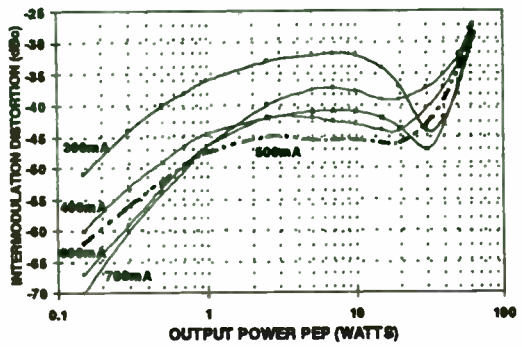


Fig. 12 - LDMOS - 2 Tone Intermodulation Distortion versus Output Power.

VIII. SUMMARY

Silicon Power Transistors - both BiPolar and LDMOS have improved the ability to handle linear amplification requirements over the past few years and through design and process techniques, have greatly reduced the 'GAP' with the historic GaAs MESFET devices to where they are now a viable candidate.

System designers now have a Silicon Solution to the challenge for developing Linear High Power amplifiers for use in CDMA and other PCS applications.

REFERENCES

[1] TIA/EIA/IS-95A "Mobile Station--Base Station Compatibility Standard for Dual-Mode Wideband Spread Spectrum Cellular System," Global Engineering Documents.

[2] TIA/EIA/IS-97A "Recommended Minimum Performance Standards for Base Stations Supporting Dual-Mode Wideband Spread Spectrum Cellular Mobile Stations," Global Engineering Documents.

[3] D. Whipple, "The CDMA Standard" Applied Microwave and Wireless, Vol. 8 No. 2, pp.58-66, Spring 1995

[4] R. Oltman, CDMA Noise Measurements". Applied Microwave and Wireless, Vol. 8 No.1, pp. 40-48, Winter 1996

[5] Franco N. Sechi, "Linearized Class-B Transistor Amplifiers" IEEE Journal of Solid-State Circuits, April 1976, p 264

[6] A. Wood, C. Dragon and W. Burger, "High Performance Silicon LDMOS Technology for 2 GHz RF Power Amplifier Applications." Paper presented at International Electron Devices Meeting.

ACKNOWLEDGMENT

The authors are pleased to acknowledge the support of Noise Com Inc. by providing a CDMA Simulator Source for the initial tests and the valuable assistance of E. James Crescenzi Jr., Principal Scientist, Microwave Products Division, Watkins Johnson Co., Palo Alto. His loan of lab equipment including the HP89441A Vector Analyzer and other digital communication test sets was extremely helpful. The high power digital test source included the WJ SA1056 CDMA Power Amplifier being introduced by the firm.

MODULATION TECHNIQUES

Modulation Techniques

Session Chairperson: Harold Walker,
Pegasus Data Systems (Middlesex, NJ)

VPSK MODULATION ON FM SUBCARRIERS

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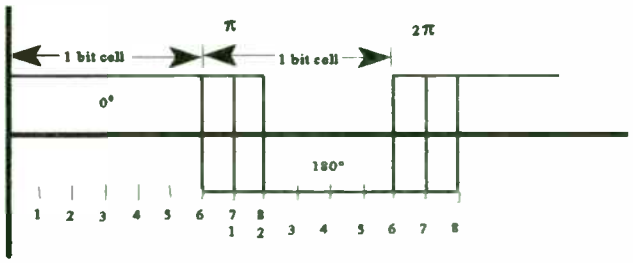
ABSTRACT:

Data can be transmitted over FM subcarriers at 196 Kb/s by using a patented (6) "Biphase" code at baseband. The bandwidth required is 20 KHz, extending from 78 to 98 KHz in the detected FM baseband. The method operates error free with a 15 dB S/N ratio in the filtered off subcarrier band. Special extremely linear filters are required throughout - at RF, IF and baseband- to prevent main carrier bleed through. The encoding method, which compresses data to 10 bits/sec/Hz, is described as well as the ultra-linear filters and the linear detector circuit.

Biphase data encoding is well known in the industry, but under appreciated. Manchester encoding, which is used with ETHERNET is one example. Miller or MFM encoding used in disk recording is another. The "Slip Codes" are a patented variation of MFM.



The slip code used in the FM-SCA system to be described is the 6,7,8 code. Fig. 1 shows the "eye" pattern for 6,7,8 slip coding. The rules are:

1)If there is no change from the previous bit, the polarity or phase is changed after one normal bit width.(6/6 bit width.)

2) If there is a change from the previous bit, from a 1 to a 0, or 0 to 1, the bit width is stretched 1/6 and the transition occurs after 7/6 bit width.

3) After 4 changes, if there is a 101 data pattern in the pipeline, the bit width is stretched by 2/6 and the transition occurs after 8/6 bit width.

This latter change resets all internal counters in the encoder and decoder chips and starts the patterns anew. Due to the stretching, the data comes in slower than it goes out of the decoder, so there will soon be a slipped or missed bit. This bit is always a 0, so the decoder inserts this missing bit and sets the present bit to a one. The name "slip code" comes from this slipped or added bit.

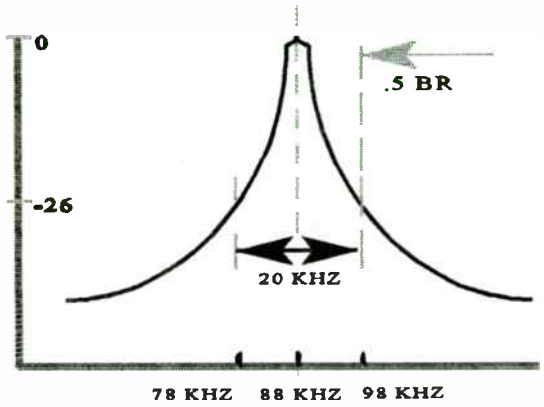
The bandwidth efficiency and modulation error angle of this encoding method are given by the formulas:

$$Q = \frac{2.2\ [2\ (m\ +\ 1)\ ]}{\pi}\ \text{Bits/sec/Hz}$$

$$\beta = \frac{\pi}{2\ (m\ +\ 1)}\ \text{Radians}$$

This is a phase angle modulation method, with a phase change of approximately pi/6 radians, or 30 degrees per zero crossing change. The error angle β is given in the lower equation.

The spectrum of this biphase code centers around .45 Bit Rate. (It extends from .5 BR to .4 BR at the -26dB points). The space at baseband below .4 BR is not used by this coding method and therefor is available to pass the main channel information of an FM signal. Only minimal filtering is required at the transmitter to keep any low level energy from the subcarrier out of the main channels. The spectrum is shown in Fig. 2.



The FCC requires that subcarriers be 20 dB or more below the main carrier so the receiver will require that all main carrier energy be suppressed by about 40 dB. This is accomplished with a FIR filter at Baseband which has a very flat differential group delay.

RF and IF filters must be extremely phase linear so that there is a minimum of distortion due to the FM excursions which would distort the baseband signal. As mentioned, the modulation angle for 6,7,8 coding is 30 degrees and the error angle is 15 degrees. The distortion from the main channel must obviously be kept below this amount.

Fortunately there is a phase noise reduction factor "R" that will be discussed later which helps in this regard.

It can be shown that two LC circuits operated in parallel and stagger tuned so that the -3B response points of the two overlap, will have a flat group delay response between the two outer -3dB points. Ordinary cascaded LC filters do not exhibit a flat group delay, so they cannot be used. The filter must have a BESSEL response. The RF and IF filters are shown in Fig. 3.

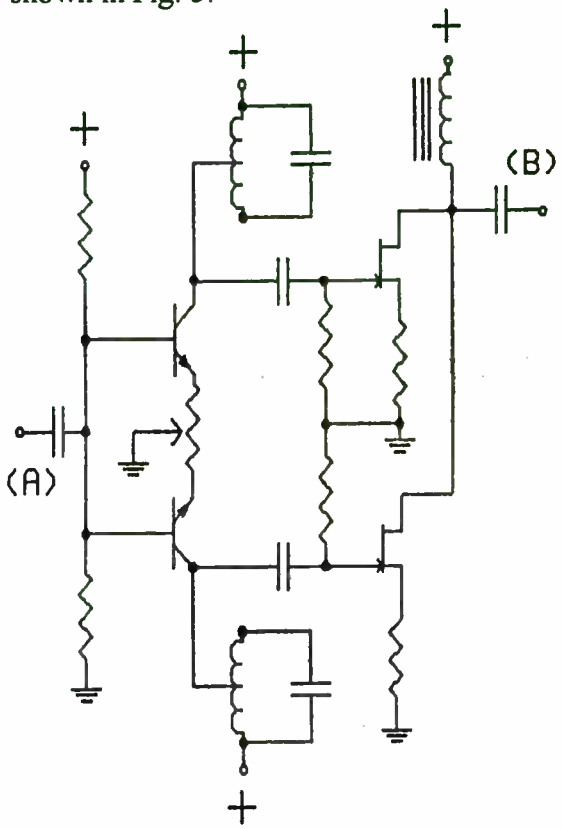
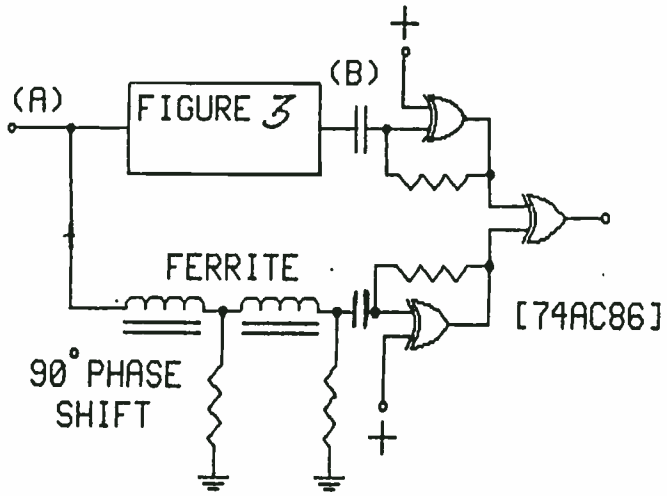


Fig. 3. Bessel Response Filter.

A little known, or at least little noticed, characteristic of a ferrite bead is that once the permeability knee is passed the permeability decreases with frequency, hence the reactance is nearly constant.

Figure 4 shows a detector circuit in which this principle is used. The LR network provides a constant phase shift with frequency to provide a reference signal to a phase detector. The upper portion of the circuit in Figure 4 is the same as that for the IF amplifier, Fig. 3, where there is a very linear phase change with frequency. This is matched with a constant

phase from the ferrites in a phase detector to provide an FM detector which is free of the usual S curve distortion.



The baseband signal from an FM receiver is analogous to that of a servo mechanism or PLL circuit with a given AM noise ratio and a narrow band PLL loop filter. The bandwidth needed to pass a wide deviation FM signal is much greater than the audio equivalent. A substantial noise reduction and phase angle improvement can be realized by using a PLL as part of the FM detector. In this case a FIR filter replaces the loop filter by providing a very narrow response band at the upper limit of the total bandpass. This situation has been analyzed by Best (3) who derives the equation:

ϕ noise Improvement
= (Pin/Pout)(Nyquist BW/noise BW)C/N

Pin/Pout is obviously the Nyquist bandwidth ratio before and after filtering. In this case 100 KHz/20KHz. It is a noise power improvement. But note the second part which is the Nyquist BW/Filter BW, the same as Pi/Po, but this is a totally independent number, the phase noise improvement, as opposed to the noise power improvement. If the bandpass filter reduced the main channel AM interference by 40 dB, resulting in a 20 dB S/N at the subcarrier level, then the second part would also decrease the phase noise. It can be measured directly by using two CW signal generators in the bandpass of the filter. In this case it should have been the same as the power ratio (5/1), but actually turns out to measure about 4.5 to 1, or almost exactly the value 1/beta from the equation above.

Best's equation can be restated as:

ϕ Noise Improvement= QR C/N

Where R = Nyquist BW/Noise BW

The post detection SNR can be determined from the formula:

SNR= β^2 QR Eb/n

Where Q above is the power ratio and R has the same value (Both equal 5).Beta = .22.

SNR = (.05)25Eb/n = 1.25 Eb/n = 1.25 C/N

Those familiar with modulation methods will recognize that this figure is 50% better than that obtained using BPSK modulation, which has no bandwidth compression in bits/sec/Hz, and much better than that which could be obtained using FM, QPSK, MPSK or QAM.

In case one is inclined to gloss over the R factor with a Ho-Hum, they should take another look.

A normal FM/FM subcarrier at 67 or 92 KHz has a modulation index less than 1. Under the best of conditions, the maximum data rate obtainable is about 20-22 KHz. The subcarrier is an NRZ Line Coded signal, with its carrier at the center. The R factor =1. The Nyquist BW and noise bandwidth are the same, hence there is no R factor improvement.

Using VPSK modulation at baseband, there is no carrier. Zero Hz of the 100KHz total FM baseband replaces it. The data modulation is a group of high frequencies with the same status as the L+R baseband, but at a lower modulation injection level. The ideal filter noise bandwidth for the data modulation is 20 KHz.

100/20 = 5 = R. This is a 7 dB improvement over an FM/FM subcarrier, while increasing the data rate by 10/1. This gain makes up for the loss due to bandwidth compression.

The signal to noise ratio required for a bit error rate of one in one million using an FM/FM subcarrier is slightly more than 13 dB. The S/N ratio for baseband VPSK at the same BER is around 8 dB.

In comparison, VPSK has a 5 dB S/N ratio advantage over an FM/FM subcarrier, which would be significant even if there were no huge data rate advantage.

To obtain an equivalent error rate using QAM in the manner used for V.34 telephone modems, a CNR of over 40 dB would be required, while the 6,7,8 code needs only 8-9 dB (10-6 BER). The QAM method cannot be limited and the phase errors, if over 1 or 2 degrees, could be disastrous. Also note that QAM centers around its own carrier, although suppressed, and the R effect does not apply, losing another 7 dB.

The "slip code" receiver requires a baseband filter that has a flat group delay.(BESSEL response). Such filters are possible using LC high and low pass filters and traps, but the digital FIR filter is preferred. The noise BW of the filter should be as narrow as possible, since the S/N degrades with the square of the excess filter BW. However, a filter which is optimally narrow requires too many taps, so a compromise must be made by accepting a filter somewhat wider than ideal.

Another factor also enters the design problem. The filter must respond to a very narrow phase change, which dictates that it must be an "over sampled" FIR bandpass filter. The filter is over sampled at a 60X rate, ie. at 12 MHZ. This is beyond the capability of most DSPs, so an FPGA chip is used. This adds somewhat to the complexity. Or, one could say it is not a $2.00 filter. The added cost is acceptable however in a commercial device such as an FM-SCA receiver.

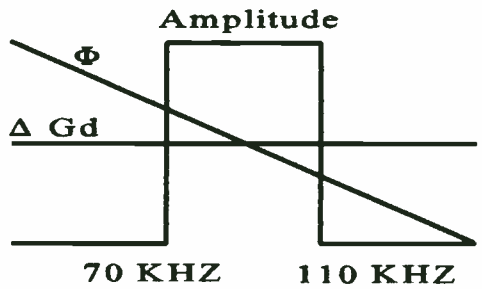
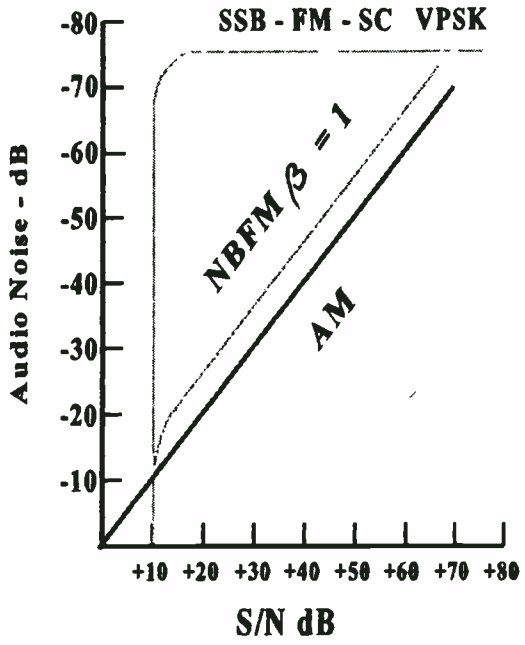


Fig. 5 shows the characteristics of the FIR bandpass filter. Amplitude, Phase and Group delay are plotted.

Fig. 6 shows a comparison of VPSK modulation vs AM and FM with beta=1. Note that the output audio S/N is far superior to FM/FM or AM subcarriers for the same input signal to noise.

Data at 196 Kb/s is adequate to transmit three 64 Kb/s "B" channels, or nearly 20 CELP voice channels. It can also carry the ISDN standards -2B1Q and 2B+D - with space left over. Videoconferencing of high quality is available at this data rate, or video transmissions of a commercial nature for stores and other purposes can be accommodated. It can also transmit stereo digital audio with a 12 KHz analog response.



While this is not quite as good as the main channel 15 KHz, it is still of higher quality than most people can hear.

The most likely uses for high data rate subcarriers are for commercial point to multi point users such as stock quote services, background music, storecasting with video, and high speed data transmission to a number of addressable users.

Pegasus Data Systems is providing this SCA equipment for Berwick Communications, a new FM station network which is expected to install the equipment at the earliest opportunity. A similar modulation method recently patented (VMSK) can be used over microwave links, cellular services and satellites. In satellite service, two full digital stereo programs (15 KHz audio) for FM station rebroadcast can be transmitted in the standard 60KHz SCPC channel to service the network. Each program requires a 256 Kb/s data rate. Two programs = 512 Kb/s. At 10/1 bits/sec/Hz, the bandwidth required is 52 KHz. There is 80 Kb/s space left over for an AM audio channel of high quality.

It is hoped, naturally, that other broadcasters will also adopt the slip code method described here, so that it becomes the High Speed Data Standard for FM broadcasting.

References:

1) B. Stryzak and H.R. Walker," Improve Data Transmission Using Single Sideband FM With Suppressed Carrier". Microwaves and RF Magazine, Wireless Design Supplement, Nov. 1994.

2) H.R. Walker, "VPSK Modulation Transmits Digital Audio at 15 Bits/Sec./Hz". Microwaves and RF Magazine, Wireless Design Supplement, Dec. 1996.

3) R.E. Best, *"Phase Locked Loops"*, Mc Graw Hill, NYC. 1984. (Analyzes the PLL as an FM detector.)

4) H.R. Walker, "The Advantages of VPSK Modulation" IEEE Wescon, San Franscisco, Nov. 1995.

5) H.R. Walker, "High Data Rate Power Line Modem", Wireless Symposium 1997. Santa Clara, Cal. (Baseband application of VMSK).

6) H.R. Walker, "High Speed Data Communications System Using Phase Shift Key Coding" U.S. Pats. 4,742,532 and 5,185,765. (Basic VPSK Patents.)

7) H.R. Walker, "Linear Phase IF Filters and Detectors", Proceedings, Wireless Technology 95, Stamford Conn. Sept.1995.

Using Quadrature Modulators to produce Frequency Modulation.

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The invention and perfection of the small, monolithic quadrature modulator has been a great boon to the design of portable wireless systems. These quadrature modulators are noted for their small size, low cost, ease of integration, and excellent performance. Virtually any modulation format can be produced using these modulators - AM, PM, FM, or any combination thereof. These performance characteristics, coupled with a wide variety of low-cost modulator offerings from a large number of vendors, have made the quadrature modulator RFIC universal in wireless design.

It is well known that constant envelope, frequency modulated signals such as FSK or GMSK can be produced by the quadrature modulator. These signals are created in much the same fashion as PSK type modulations, but with the added constraint that the envelope of the signal always be constant. The advantages of using the quadrature modulator to produce these signals include FM response down to zero hertz, exact setting of the modulation index, and the ability to complete decouple the modulation circuitry from that of the synthesizer circuitry.

In this paper, the basics of FSK generation using quadrature modulators are discussed. The various error components produced by the modulator are examined and the sources of those errors explained. A detailed analysis is then made of the effects of those errors on the demodulated output of an FSK modulated system. System-level simulations and measured data from a production status GMSK link are included to support the results of the analysis.

I. FSK generation using quadrature modulation

The basic technique for producing a frequency varying waveform with a quadrature modulator can be derived by expanding the standard expression for an FM waveform into a form that lends itself to quadrature implementation. Equation 1 shows the basic mathematical representation for an FM modulated carrier. The signal has a constant amplitude A, a center frequency equal to ω_c radians/second, and a modulated phase component $\Phi_m(t)$.

$$V_{fm}=A\cos(\omega_c t+\phi_m(t)) \qquad \text{Eq. 1}$$

Equation 2 shows the relationship between this term and the original modulating signal m(t) (in this case, an input bit stream).

$$\phi_m(t)=K_v\int_0^{\tau} m(t)dt \qquad \text{Eq. 2}$$

Equation 1 can be expanded into a more complex but equivalent form (equation 3) that hints at a possible quadrature implementation.

$$V_{fm}(t)=Cos(\omega_c t)Cos(\phi_m(t)) \quad \text{Eq. 3}$$
$$-Sin(\omega_c t)Sin(\phi_m(t))$$

$$V_{fm}(t)=Cos(\omega_c t)Cos[K_v\int_0^\tau m(t)dt] \quad \text{Eq.4}$$
$$-Sin(\omega_c t)Sin[K_v\int_0^\tau m(t)dt]$$

Final expansion of this expression into equation 4 shows the complete mathematical representation of the FSK waveform implemented in quadrature fashion. Note that the cos $\Phi_m(t)$ and sin $\Phi_m(t)$ components have been expanded into forms that link them back to their original, modulating data source - m(t). References 4 and 5 provide complete details concerning the basic FM equations and quadrature implementations.

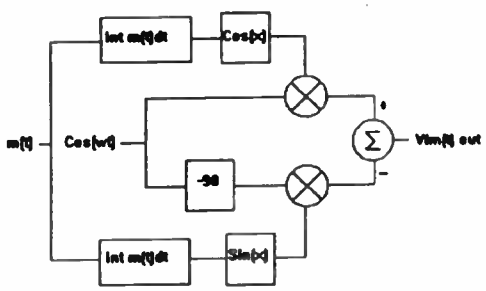

Figure 1

Compare equation 3 to the FSK quadrature modulator block diagram shown in figure 1. An input local oscillator (LO) waveform is split into in-phase and quadrature components. Each of the LO signals are then fed into multipliers (usually Gilbert cell mixers) and multiplied by I and Q modulation waveforms. These two products are then summed to form the modulated output signal. Note that the FSK modulator directly implements the expression found in equation 3.

Those with analog radio experience will recognize the circuit in figure 1 as a single-sideband modulator. This is no coincidence. In fact, possibly the best intuitive model of the FSK quadrature modulator circuit is as a single-sideband modulator with frequency agility. The process is straightforward. A data "1" into the modulator driver creates the required I and Q waveforms necessary to produce the sideband above the (suppressed) carrier. A data "0" conversely produces the lower sideband. The single-sideband circuit, normally thought of as an amplitude modulator, essentially produces an FSK waveform. In actual practice, the upper and lower sideband frequencies aren't allowed to pop back and forth instantaneously. Rather, the transitions are tightly controlled to produce precise phase transitions between the "mark" and "space" frequencies. In fact, much of the research effort directed towards FSK has centered on finding the optimum modulation waveforms necessary to make these phase transitions smoother and more spectrally efficient (i.e. GMSK, TFM, etc.).

II. Error Sources in Quadrature Modulators

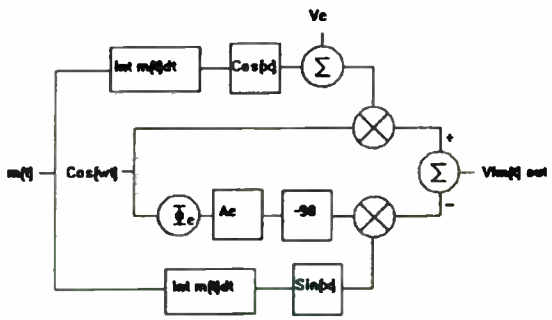

Figure 2

The theoretical implementation of an FSK quadrature modulator is shown in figure 1. The output of this theoretical modulator is a flawlessly produced FSK waveform, free from any sort of undesired spurs or distortions. As is the case with most electronic components and systems however, the devil is in the details.

Figure 2 shows the complete block diagram of a "real" FSK quadrature modulator set up to produce a single sideband signal. This more detailed block diagram exhibits the shortcomings that occur in a commercially available quadrature modulator. Note that in Figure 2, additional offset voltages, phase and gain errors have been added to the basic construction shown previously. These terms, representing physical shortcomings intrinsic to the modulator, have been added to accurately model its performance. Those errors manifest themselves in the production of two spurious signals at the modulator output: a carrier leakthrough component and an opposite sideband leakthrough component. If the relative levels of these error components are high enough, then the overall output can be degraded to the point where modulator induced bit errors will occur.

Carrier leakage (usually referred to as LO leakage) occurs as the result of small dc offset voltages in the I and Q Gilbert cell mixers. Slight mismatches between the BJTs in the input differential pairs will result in less than perfect carrier suppression. Opposite sideband leakage results from two error mechanisms within the modulator -gain imbalance and/or phase offset from true quadrature between the in-phase and quadrature signal paths inside the modulator. Gain imbalances in the modulator occur as a result of mismatches between the I and Q Gilbert cell mixers and the summation circuits that follow. Phase errors (from true quadrature) occur in the phase splitting circuit that drives the two multipliers. DC offset voltages, gain and phase imbalance in the I and Q paths of the modulator can all be compensated by adjusting the modulation signals going into the device[1,2,3]. However, these compensation techniques will generally work best at one temperature and one frequency.

III. Calculation of Carrier and Opposite Sideband Suppression

Equation 5 is the mathematical representation of the "real" modulator circuit shown in figure 2. Note that the effects of modulator dc errors, amplitude imbalance and phase offsets have all been included. After some algebraic manipulation, three like terms are produced and are shown in Eq 6. These terms are the (desired in this case) upper sideband - USB, the undesired lower sideband - LSB, and the carrier leakthrough component - LO.

$$V_{fm}(t)=Cos(\omega_c t)Cos(\omega_m t+V_e) - A_e Sin(\omega_c t+\phi_e)Sin(\omega_m t) \quad \text{Eq. 5}$$

$$V_{USB}(t)=1/2Cos(\omega_c+\omega_m)t + (A_e/2)Cos((\omega_c+\omega_m)t+\phi_e) \quad \text{Eq. 6a}$$

$$V_{LSB}(t)=1/2Cos(\omega_c-\omega_m)t - (A_e/2)Cos((\omega_c-\omega_m)t+\phi_e) \quad \text{Eq. 6b}$$

$$V_{LO}(t)=V_e Cos\omega_c t \quad \text{Eq. 6c}$$

Equation 6c shows that the LO leakage term is linearly dependent on the amount of dc offset present in either the I or Q multipliers. The carrier suppression ratio for this model of a quadrature modulator is equal to 20*log (1/Ve). Note that the voltage, Ve, does not actually exist in a physical sense in a given modulator, rather it serves as a mathematical term that models all of the actual dc offsets that may exist within the device. The evaluation of sideband suppression is more complicated. Two terms influence the ratio of desired to undesired sideband ratio - A_e and Φ_e. One way to observe the relationship between these error terms and their resulting suppression levels is to set one of the error terms to zero and observe the change in suppression as the other error term is varied.

Figures 3 and 4 show two such graphs. In figure 3, the phase error is set to zero and the amplitude imbalance between the two channels is varied to produce various levels of sideband

suppression. In figure 4, amplitude imbalance is set to zero and phase offset is varied to produce the carrier suppression. It is clear that opposite sideband suppression is fairly sensitive to phase and amplitude mismatch in the modulator.

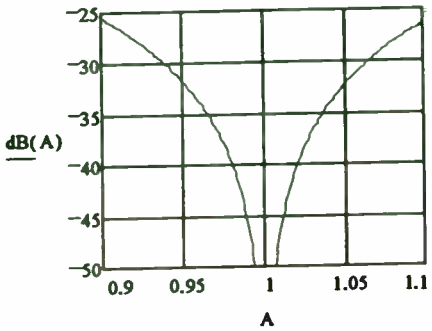

Figure 3

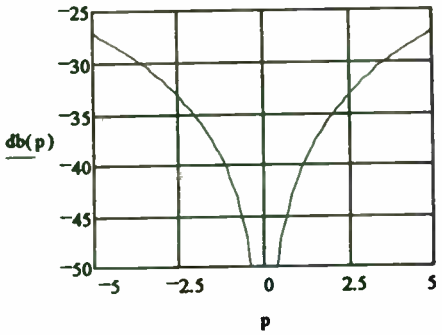

Figure 4

IV. Visualization of Carrier/Sideband Leakthrough with I/Q Plots

Excessive levels of carrier and opposite sideband leakage can have adverse effects on the quality of the total transmitted FSK signal. However, the way in which these spurious products show up in an FM discriminator's output is not immediately obvious. The key to understanding the discriminator's response to the flawed FSK signal is to first determine how the leakage terms present in the transmitted FSK signal affect the overall phase of the signal.

The baseband I/Q plot provides an illustrative way to visualize the instantaneous phase of an FSK signal. An I/Q plot is essentially a baseband representation of a modulated signal. The phase rotation due to the signal's carrier component has been removed from the plot, leaving only the amplitude and phase changes resulting from the modulating inputs.

The I/Q plot for the flawed FSK signal described by equation 6 can be constructed by setting ω_c equal to zero (baseband conversion) and by plotting the phase and amplitude of the resultant waveform. The USB term produces a clockwise rotating vector with an amplitude of $(A+1)/2$ and an angular velocity of $2\pi*F_{dev}$. The opposite sideband (LSB) produces a counterclockwise rotating vector with an amplitude of $(A-1)/2$ and an angular velocity of $2\pi*F_{dev}$. The leaked carrier component (LO) offsets the point at which the vectors rotate about the origin. The superposition of the USB, LSB vectors and the carrier offset produces a composite vector that traces out an I/Q plot like that shown in figure 5. This composite exhibits a non-constant angular velocity as it spins about the origin. The average velocity, corresponding to frequency offset, is equal to $2\pi*F_{dev}$ radians/second. The instantaneous velocity (or frequency) deviates above and below this average as the vector traces out its eccentric path.

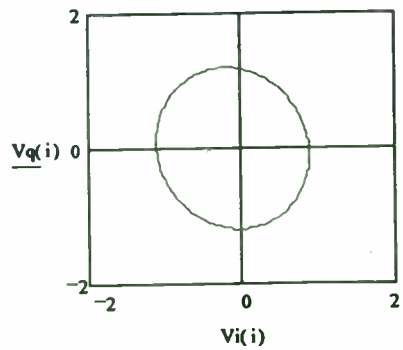

Figure 5

V. Effects of Carrier and Sideband Suppression on FM Demodulated Output

An FM discriminator produces an output that is proportional to the time derivative of the phase of its input. As a result, an FM demodulator reveals errors related to the derivative of the phase of the incoming signal. As long as the phase of the incoming signal advances at a constant rate, the output remains constant. Any variations in this phase advance, however, cause "wobble" in the demodulated output. As indicated in the previous paragraph, the carrier and opposite sideband leakthrough components produced in a "real" modulator will produce such phase variations.

Two Mathcad plots will help in relating carrier and sideband suppression ratios to demodulated distortion levels.

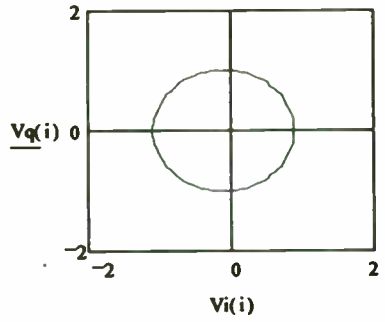

Figure 6a

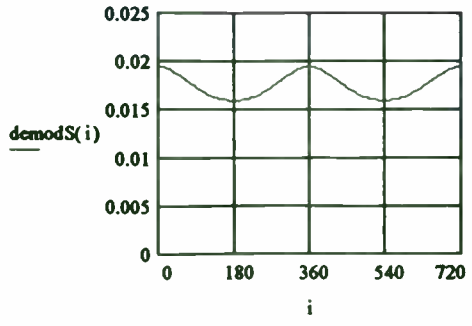

Figure 6b

The first plots illustrate the effects of carrier leakthrough on demodulated output. Figure 6a shows the Mathcad I/Q plot of an imperfect FSK carrier with a carrier feedthrough component 20dB below the upper sideband. Note that the circle is slightly offset to the left from true center. Figure 6b shows the discriminated output of this signal. The ripple component of the demodulated waveform has a frequency component equal to the peak frequency deviation of the input signal (F_{dev}). This reason for this phenomena is that as the vector sweeps around the smaller amplitude portion of the circle (as measured from the origin), it traverses more angular displacement in a given time period than it does when the vector is sweeping out across the greatest amplitude portion. In other words, the angular velocity (frequency) is the greatest whenever the vector is tracing out that section of the curve that is closest to the origin.

Figures 7a and 7b show the situation that occurs when only opposite sideband leakage (due to amplitude imbalance in the modulator) is present. Note that the I/Q circle is elongated in the Q direction. As the signal vector traverses this outline, the angular velocity is at its greatest when it crosses the horizontal axis (I axis) and its lowest when it crosses the vertical (Q). Since the vector passes through two maximums and two minimums on its path around the circle, this condition produces a demodulated output that has a 2x ripple component - twice that of F_{dev}. Note that the same type of ripple component would have been observed at the demodulator output had the phase offset in the modulator been in error.

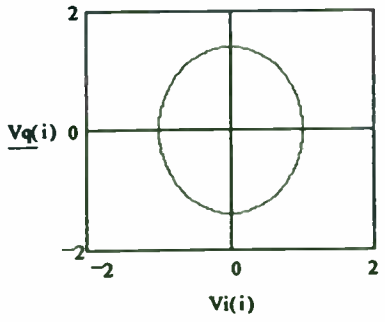

Figure 7a

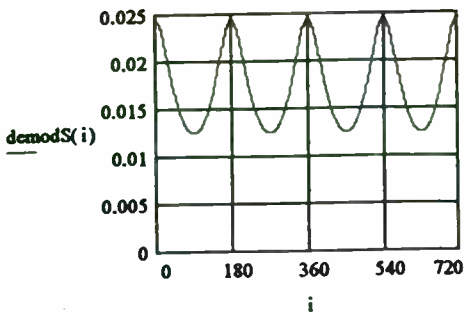

Figure 7b

VI. Demodulator Output Ripple versus Carrier and Sideband Suppression Levels.

The I/Q plot provides a simple method to visualize the effects of carrier and sideband leakage on demodulated output. Unfortunately, the plot is useful only for the limited case of the modulator transmitting all "1s" or "0s" (constant rotation of the vector in one direction). The response of the demodulator to a quadrature modulator sending real data is more complex since the signal vector is spinning clockwise and counterclockwise at different rates of velocity. Visualizing the effects of spurious products on modulated data requires the use of computer simulation.

TESS, a communications systems simulator from TESOFT, was used to model an imperfect quadrature modulator source feeding an FM discriminator. The model had provisions for dc offset, gain imbalance, and phase offset. These error parameters were varied until the predetermined level of carrier and sideband feedthrough were produced. The flawed FSK generator was then modulated with a data stream. The signal was fed into a standard discriminator and the received output "eye" recorded.

Two simulations were run to investigate the results of spurious feedthrough on demodulated output. For the first simulation, carrier leakthrough was set to 30 dBc and sideband suppression was set to 40 dBc. These values were chosen to mimic the single sideband performance of a commercially available quadrature modulator. Figure 8 shows the demodulated result of this signal when data is fed into the generator. Note the low frequency ripple component superimposed over the received data waveform. Figure 8 shows that system BER performance will probably be impacted by less than 1 dB.

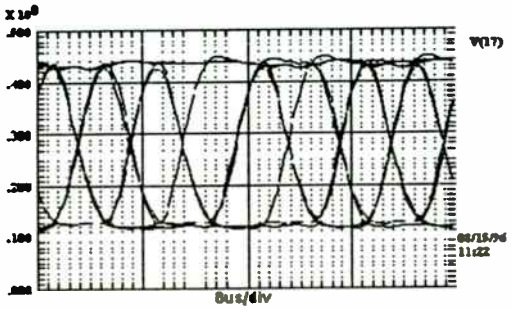

Figure 8

Figure 9 shows the demodulated output of a more severe case where carrier and sideband levels have been set to 20 dBc. Suprisingly, an output eye is still observable.

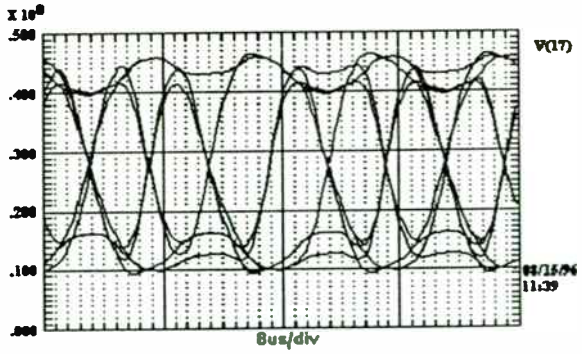

Figure 9

VII. Measured Results

Measurements of carrier and sideband leakthrough versus demodulated output

were taken from the WIT2400 frequency hopping transceiver. It was during the development stage of the WIT2400 that this phenomena was first noticed. The simulations shown in this paper were initially created in an effort to understand the effects of leakthrough on demodulated output. In addition, we wanted to learn the maximum level of feedthrough we could tolerate without affecting the BER of the system. Because the modulation and demodulation circuitry used in the WIT2400 is industry standard, the results shown here should be of general use to other designers.

Figure 10a shows a typical situation for the WIT2400. The modulator is set to produce an lower sideband signal. Carrier suppression is roughly 27 dBc and opposite sideband suppression is approximately 32 dBc. The other visible spurs are related to intermodulation products within the modulator as well as harmonic products produced by the I and Q D/A converters. The demodulated output is shown in figure 10b. Note the presence of the low frequency ripple in the output eye. The peak frequency deviation for the WIT2400 modulator is 62.5 KHz. The over-the-air bit rate is 250 Kbps. The ripple component present in the demodulated eye is a combination of the 62.5 KHz component generated by the carrier leakthrough and the 125 KHz component generated by the opposite sideband leak through.

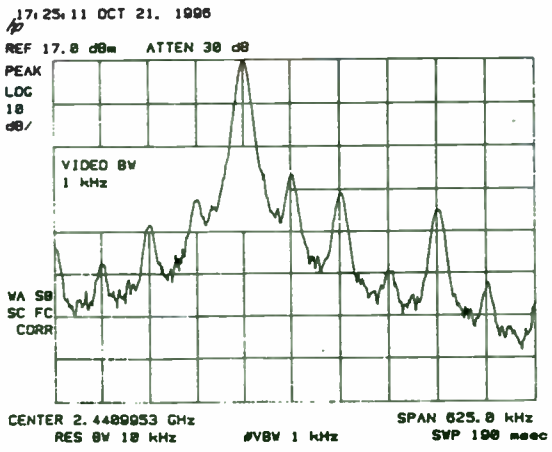

Figure 10a

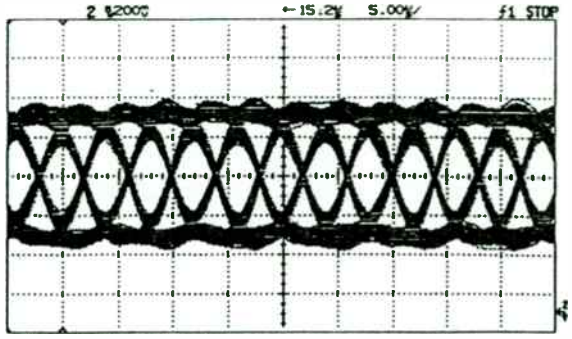

Figure 10b

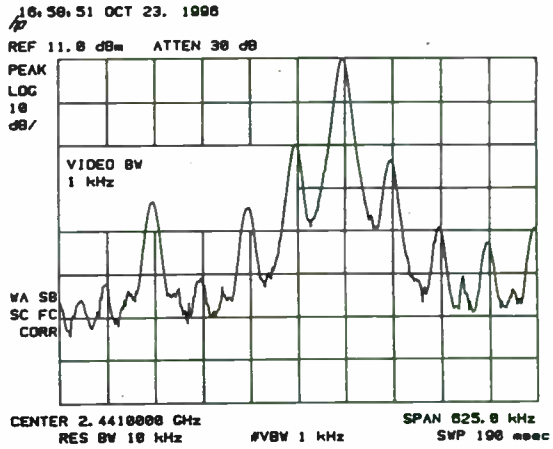

Figure 11a

Figure 11a shows the single sideband output spectrum of another quadrature modulator. The bias levels for this device were intentionally misadjusted to produce a 20dBc carrier leakage term. Two different data patterns were then fed into this modulator; a string of all "1"s and a pseudorandom data stream. Figure 11b shows the demodulated results of both of these cases. Since, in this case, carrier leakthrough is much higher than opposite sideband leakthrough, the demodulated results of these spurious signals are easier to see. The uppermost trace in figure 11b shows the demodulated result of the string of all "1"s being fed into the modulator. Note the

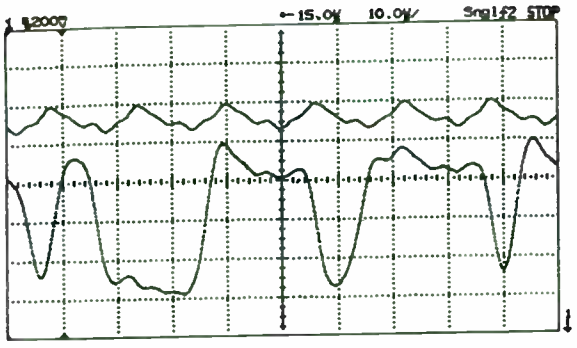

Figure 11b

strong 62.5 KHz component present in the output due to the severe carrier leakthrough. The lower trace in figure 11b shows a demodulated bit stream coming from the same modulator. Note the 62.5 KHz ripple seen in the all "1"s modulated case is present in this output as well - most noticeably when the data stream consists of consecutive "1"s. The demodulated output in the lower trace of figure 11b, as ugly as it is, will still probably impact the overall system BER by less than a dB or two. Through system level tests with the WIT2400, we have empirically found that a transmitted eye with this much distortion will degrade our overall received sensitivity only a couple of dB.

VIII. Summary

A simple model of the Quadrature modulator as a frequency modulator has been introduced. The error terms associated with this modulator have been defined and explained. The effects of these errors on the demodulated eye of an FSK modulated link have been described and simulated. These results have also been qualitatively confirmed by measurements on a GMSK modulated transceiver. Generally speaking, the carrier suppression and opposite sideband suppression guaranteed by most of the commercially available quadrature modulators is more than adequate for most commercial grade FSK applications.

References

[1] Ravi Datta and Stewart N. Crozier, "Direct Modulation at L Band Using a Quadrature Modulator with Feedback," International Mobile Satellite Conference, IMSC 1995.

[2] M. Faulkner, T. Mattsson, W. Yates, "Automatic Adjustment of Quadrature Modulators," Electronic Letters, January 1991, Volume 27, Number 3.

[3] Derek Hilborn, Shawn Stapleton, James Cavers, "An Adaptive Direct Conversion Transmitter," IEEE Transactions on Vehicular Technology, May 1994, Volume 43, Number 2.

[4] Paul H. Young, "Electronic Communications Techniques, 3rd Edition," Merrill Publishing 1994, pp. 325-326.

[5] Kamilo Feher, "Wireless Digital Communications," Prentice Hall, 1995, pp. 168-169.

AN IN-LOOP MODULATION SYNTHESIZER FOR CONSTANT ENVELOPE DIGITAL COMMUNICATION SYSTEMS

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ABSTRACT

A novel architecture for digital communication systems employing constant envelope modulation schemes is presented. The described technique allows the injection of constant envelope modulation inside a phase locked loop (PLL). The PLL voltage controlled oscillator (VCO) generates a highly accurate, low noise modulated signal at RF frequencies. The result is a highly accurate, low noise signal presented to the power amplifier requiring minimum filtering prior to the antenna.

A 0.5μm BiCMOS chip with low power consumption integrating the three key building blocks of the modulation synthesizer architecture is described. The solution draws less than 26mA from a 2.7V supply, while meeting the GSM specifications for modulation spectrum and RMS phase error. Measurements of the IC in a typical system application, achieve a modulation RMS phase error of less than 1°.

I. INTRODUCTION

Worldwide standards for mobile communication systems require spectrally efficient digital modulation schemes. Low cost, low power, highly integrated solutions are required to meet the low cost and long talk time requirements of the end user.

Presently, several different digital modulation schemes are employed world wide for cellular systems. Each modulation type has advantages and disadvantages. A large category of the used modulation schemes like GMSK (GSM, DCS1800, PCS1900), GFSK (DECT), etc., all have constant envelope. The constant envelope modulation technique is not as spectrally efficient as QPSK and π/4-QPSK, but it is well known that a constant output amplitude allows a more efficient class C implementation of the transmit power amplifier (PA). Class C amplification will result in significantly lower power consumption (longer talk time) for the system. However, only in the power amplifier have the properties of constant envelope been exploited so far. Presently, most constant envelope modulation systems utilize a traditional transmitter architecture as shown in Fig. 1. As portrayed in the figure, the modulation is generated at IF using a quadrature mixer. The resulting signal is then up-converted to RF frequencies. After the up-conversion the output is filtered to reject undesired noise, where after an additional gain stage is used to amplify the signal before it enters the PA. The output power of the quadrature mixer must be low enough to ensure sufficient linearity of the modulator and up-conversion mixer. In this paper a novel architecture is presented that overcomes many of the above problems by exercising the benefits of constant envelope modulation.

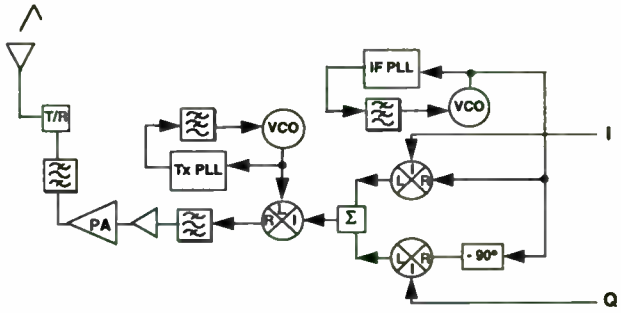

Fig. 1. Typical transmitter architecture

II. MODULATION SYNTHESIZER ARCHITECTURE

As the name infers, constant envelope modulation has the property that the output signal will maintain a constant amplitude after it is imposed on a carrier. All types of FM signals fall in this category, including frequency shift keying (FSK). The GSM standard uses a special form of frequency shift keying that is called

gaussian minimum shift keying (GMSK), which is also constant envelope. It is this constant envelope property that is used in the new architecture shown in Fig. 2. Rather than up-converting the modulated signal, the waveform is generated directly by the voltage controlled oscillator (VCO). The VCO varies the output frequency based on an input voltage, and it is inherently amplitude limited for its given output frequency range. VCO's can be designed to have an output power upwards of +10dBm, with harmonics existing only at multiples of the fundamental frequency. By directly modulating the VCO, a modulated RF signal with constant envelope can be generated.

Typically, the VCO is locked to a given center frequency by use of a phase locked loop; an approach already being used in many communication systems. One disadvantage of modulating the VCO in a closed loop PLL is the suppression low frequency components due to the high pass filtering of the VCO feedback signal [1]. Similarly, when modulating the PLL reference input, the high frequency signals are attenuated by the loop filter. Where frequency drift during transmission is allowed, this distortion may be overcome by open loop modulation [2]. This is a viable approach for DECT, which has an allowable drift of 13kHz/msec, but other systems like GSM have much tighter requirements, thus open loop modulation is not acceptable.

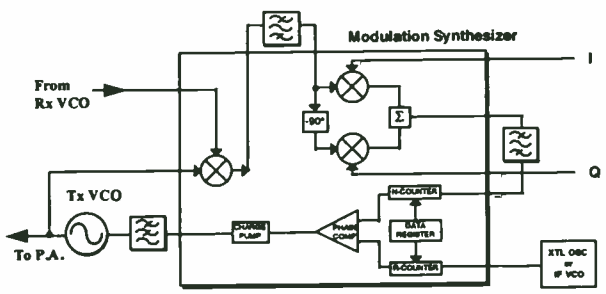

Fig. 2. Modulation Synthesizer Architecture

The modulation synthesizer architecture proposed here generates a highly accurate, low noise modulated signal at RF frequencies. Rather than modulating the VCO directly, a quadrature mixer is inserted in the feedback path (N-counter input) of a PLL (see Fig. 2). The phase detector and charge pump of the of the PLL operate at a much higher rate than the frequency deviation of the modulation. Therefore, the fast PLL can track the slow varying feedback signal generated by the quadrature mixer. If the loop tracks the modulation perfectly, when the modulation signal forces an increase in the frequency/phase, the loop will compensate for it by increasing the VCO output frequency accordingly.

A higher phase detector frequency leads to improvement in PLL phase noise. Ideally, the noise inside the loop will be proportional to the divide ratio by the following formula:

$$\mathcal{L}(f) \propto 20 \log (N) \quad (1)$$

where $\mathcal{L}(f)$ is the single sideband phase noise and N is the integer value programmed in the PLL's N-counter. However, by operating the PLL's phase detector/charge pump at a high frequency, the transmitters output frequency selectivity is significantly reduced. Traditionally, if the channel spacing of the system is 200kHz, then the phase detector frequency has to be equal to or a fraction of 200kHz:

$$f_{out} = N * fcomp \quad (2)$$

where f_{out} is the VCO output frequency, and *fcomp* is the comparison frequency. Thus, if N is increased by 1, *fout* will increase by *fcomp*, so when *fcomp* is much greater than the channel spacing the frequency selectivity is reduced.

The situation is remedied by introducing a down conversion mixer prior to the phase shifter input of the quadrature mixer. This mixer will downconvert the output of the VCO to a predetermined fixed frequency that is an integer multiple of the phase detector comparison frequency. If the mixer LO is changed, the loop will compensate by changing the VCO output frequency accordingly. Thus the LO can be used to perform the required channel selection, and the phase noise contribution of the Tx PLL is reduced even more because of the lower N divider value. By careful frequency planning, the receive PLL's VCO can be used to generate the required LO for the modulation synthesizer.

The wide band noise generated by this architecture is now gated by the noise floor of the VCO, and not the quadrature modulator. Since the constant envelope modulation is generated at RF frequencies by the VCO, it can drive the power amplifier directly through a simple low-pass filter, that removes the VCO harmonics. This will decrease the amount of filtering necessary before and after the PA, and therefore reduce current consumption of the transmitter.

III. System Implementation

To implement the proposed architecture in a cost and power efficient manner, a chip containing the three key components of the modulation synthesizer was developed. The chip is implemented in a high performance 0.5μm BiCMOS process. The IC contains a quadrature modulator, an RF mixer, and a high frequency PLL. The PLL includes a phase detector/charge pump that runs at frequencies above 40MHz, and high frequency inputs (max 650MHz) at both the N-counter and the reference counter. The Tx VCO and loop filter are external to the chip. The down conversion mixer operates with RF and LO input levels down to -15dBm at frequencies of up to 2GHz, and supplies a differential IF output at frequencies of up to more than 350MHz. The quadrature modulator phase shifter accepts inputs of 50-350MHz, and both the LO feedthrough and undesired sideband are suppressed by more than 30dB. The chip is programmable through a serial μ-wire port, and allows selective power down of the three blocks as well as programmable correction for the wide frequency range variation of the phase shifter.

An example of a GSM transceiver using the modulation synthesizer concept is shown in Fig. 3. As seen in Fig. 3, several filters have been added among the three building blocks. These filters are simple discrete LC filters that help to reduce undesired frequency components. To increase the isolation of the Rx LO to the Tx output, two attenuators are added at the respective inputs to the mixer.

In GSM, three of the key transmitter specifications are: the modulation accuracy, adjacent channel power, and noise in the receive band. The modulation accuracy must have a RMS phase error of less than 5 degrees [3]. The adjacent channel power must be less than 60 dB down relative to the carrier (dBc) at offsets ≥400kHz in a 30kHz measurement bandwidth [3]. The transmitter noise measured in the receive band (25 MHz offset) must be less than -162dBc/Hz.

The system requirements specify a SNR at 400kHz away from the carrier frequency. This SNR requirement cannot be fulfilled by rolling off close in phase noise before 400kHz, as it would affect the modulation RMS phase error. The loop filter bandwidth needs to be much wider than the frequency deviation of the GMSK signal (67.7kHz) in order to avoid introducing phase distortions. Thus, the noise 'inside the loop' must be low enough to exceed this requirements. The wideband noise at offsets greater than 20 MHz, will track the phase noise of the VCO. Thus, the noise from the transmitter output measured in the receive band will be dominated by the Q-factor of the VCO tank circuitry, rather than the noise floor of the quadrature modulator.

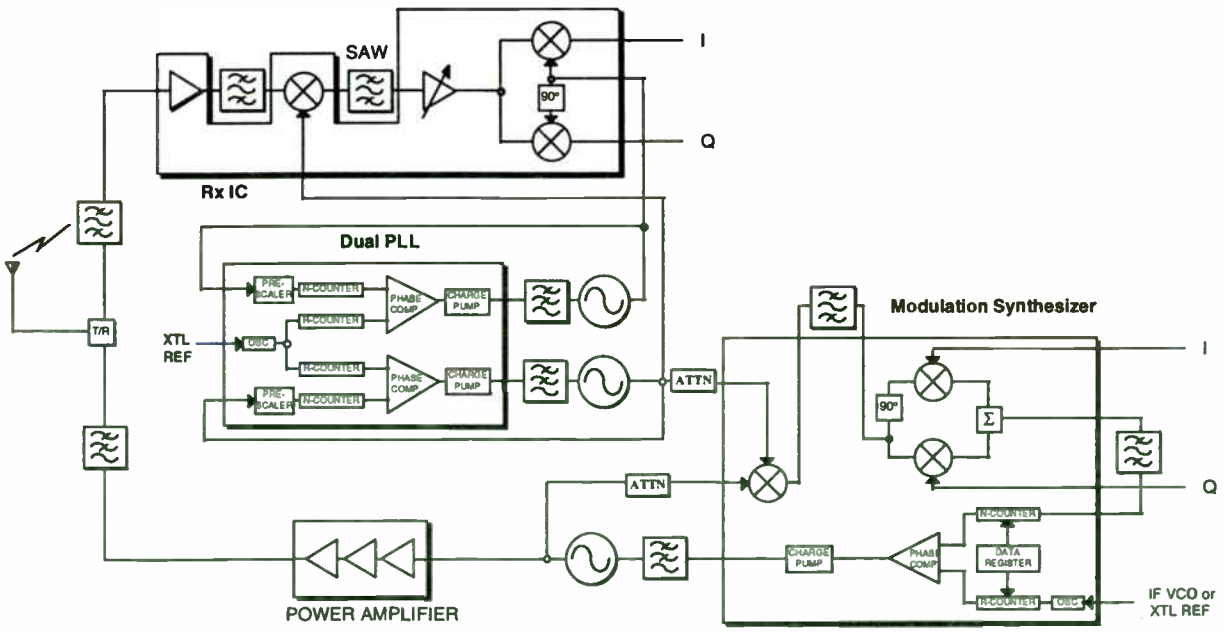

Fig. 3. Proposed GSM Transceiver Architecture

IV. Results

A prototype GSM transmitter system based on Fig. 2 was built and characterized. An IF frequency of 234MHz was chosen, and the comparison frequency was set at 39MHz. The initial results appear very promising. Fig. 4-6 show some of the obtained results.

Performing the modulation accuracy measurement using a HP 89441 Vector Network Analyzer yields a RMS phase error of 0.739° as shown in Fig. 4. The corresponding error vector magnitude (EVM) is 1.2%, both well within the GSM specifications.

As can be seen, the SNR inside the loop is approximately -64dBc (Fig. 5) using the GSM type approval measurement conditions (30kHz RBW, 30kHz VBW, 100ms sweep time), which is 4dB better than the GSM specification. This is obtained using a loop filter bandwidth of approximately 1MHz (Fig 6.). The SNR can be further improved by increasing the phase detector frequency, and/or decreasing the noise contribution of other components in the loop. All measurements were performed using a 2.7V power supply, and an ALPS URE8X-934 VCO. The power consumption of the chip when all blocks are functional is approximately 26mA.

V. Conclusion

A new architecture to implement the transmit section in a constant envelope modulation system is presented. The system utilized the properties of constant envelope modulation to overcome many of the drawbacks present architectures exhibit. The VCO is modulated directly by inserting the quadrature modulation in conjunction with a down conversion mixer inside the phase locked loop feedback.

A 0.5µm BiCMOS chip integrating the three key components is presented along with measurement results showing an in-loop SNR of 64dBc, and a RMS phase error of less than 1° is achieved. The chip uses 26mA from a 2.7V supply.

Acknowledgments

The authors would like to thank Jeff Huard, David Bien, and Dr. Benny Madsen, whose contributions were instrumental in developing the modulation synthesizer integrated transmitter solution.

References

[1] Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*, Prentice-Hall, 1983

[2] Madsen, B. and Fague D, "Radios for the Future: Designing for DECT", *RF Design*, April 1993.

[3] Redl, S.M., Weber, M.K., and Oliphant, M.W., *An Introduction to GSM*, Artech House, Inc, 1995.

[4] *Operating and Evaluating Quadrature Modulators for Personal Communication Systems*, National Semiconductor Application Note, AN-899, October 1996

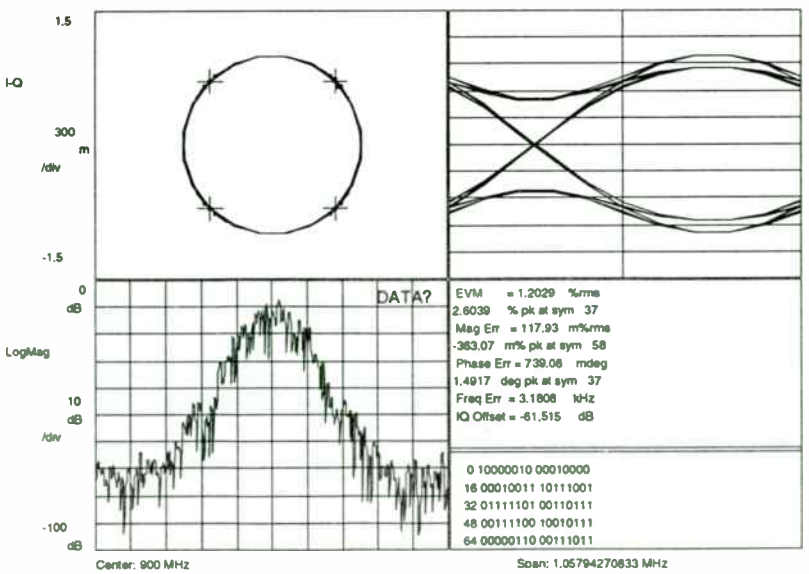

Fig. 4. Measured GMSK RMS Phase Error

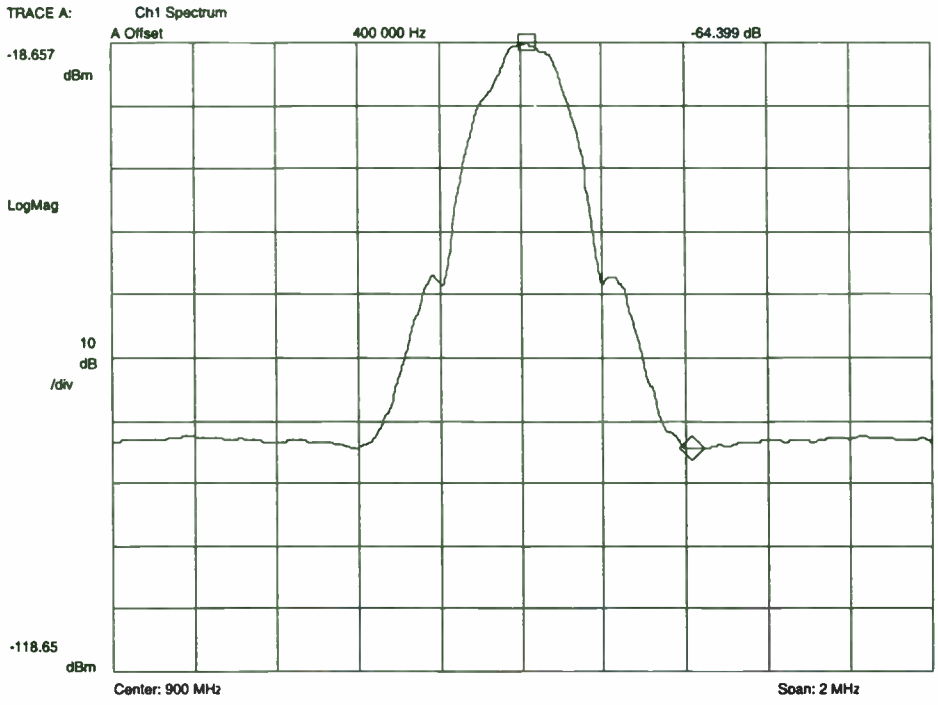

Fig. 5. Measured GMSK Modulation Spectrum

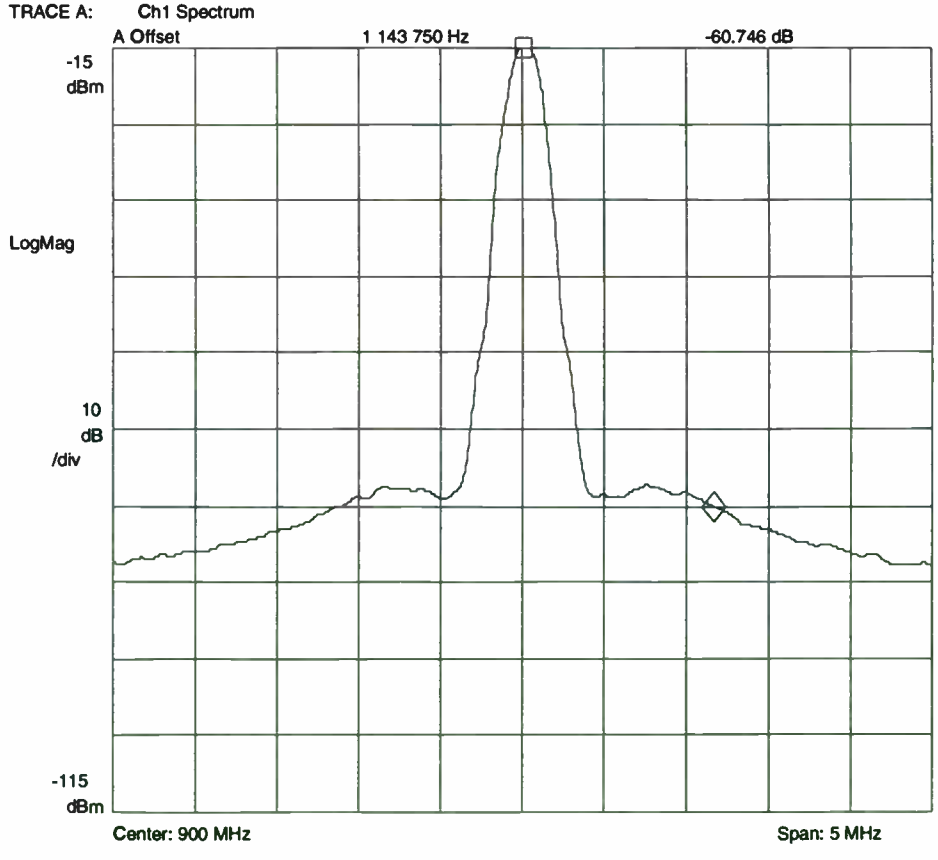

Fig. 6. Measured Modulation Synthesizer Loop Bandwidth

HIGH DATA RATE POWER LINE MODEM USES BIPHASE MODULATION

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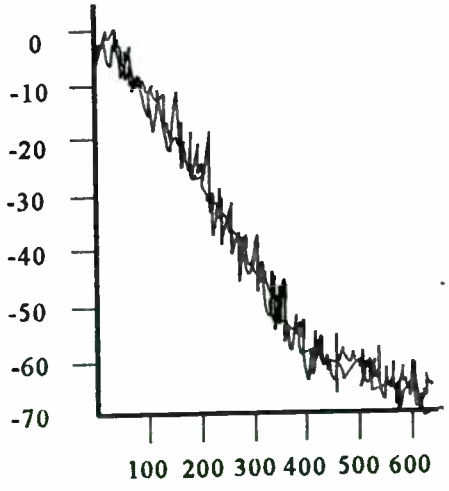
Middlesex, N.J.

ABSTRACT:

The wiring within a building which is used for lighting etc. can be used as a transmission medium for data at rates of 1700 Kb/s or higher. This paper outlines some tests made using "Biphase" modulation with two different codes over the power lines in an industrial building complex. A new modulation method called VMSK (Very Minimum Shift Keying) is described that permits data rates 15 times or more above those presently in use on power lines, while still complying with FCC Part 15.

The power line within a building, where the wires are in pairs to each user outlet, resembles a transmission line with an impedance varying from very few ohms to about 100 ohms. As is to be expected, this is a complex impedance which changes as additional loads are added or subtracted from the line. The line terminates in a transformer which may be off premises, or within the building. The transformer is usually a three phase device that will not pass high frequencies, yet permits a surprising amount of coupling between phases, since at some point wires with all phases are usually in the same conduit.

Figure 1 shows a representation of the power line and its loads. Some of the loads are inductive, some capacitive and some resistive. The ordinary lamp bulb is a resistive load up to very high frequencies. Fluorescent lamps are both resistive and inductive, as are most other loads. Some devices on the line will also be noise sources, competing with the desired signal. Switching supplies can be notorious noise sources which may require power line filters on the individual device. A high intensity Halogen desk lamp with a switching supply can generate enough noise to make the power lines nearly useless. Fortunately, this noise decreases with frequency.



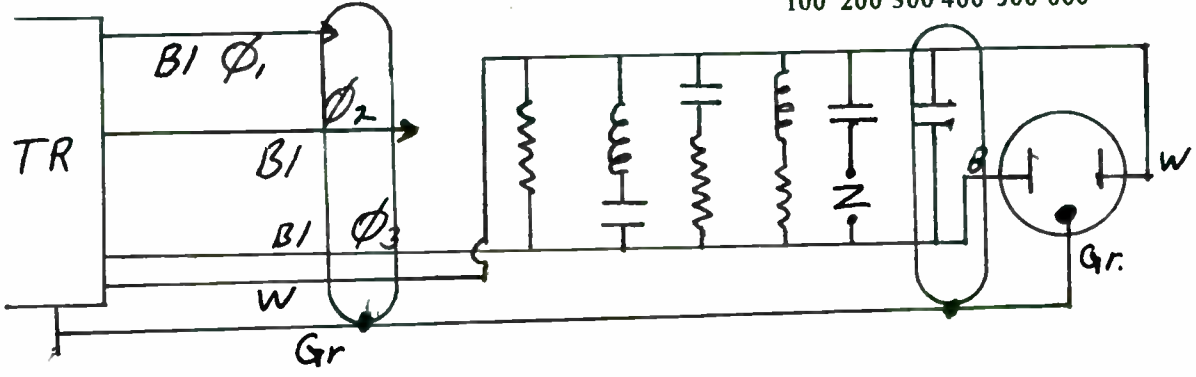


Figure 2 shows the spectral noise measured on the test lines. Note that this noise is a maximum at relatively low frequencies, and almost disappears at the lower edge of the broadcast band. This dictates that the modulation or coding method chosen must operate as high as possible in the spectrum and must have a lower spectral edge above the high noise region.

There are several factors which influence the choice of modulation method and operating frequency. The FCC Regulations, Part 15, apply, and these can be very restrictive. They permit a very high power level in the broadcast band - in a 10 Khz bandwidth, but are very restrictive if the bandwidth exceeds 10 Khz. Only in the region below 490 Khz is the use of fairly high power levels and broadband signals permitted.

The permitted power level for an intentional radiator over power lines is governed by the leakage from the lines to the outside world, except for Part 15.207c1, which permits as much power as needed if the signal can be received on normal AM radio. In a building where nearly all of the lines are shielded, as in conduit, there is little or no outside radiation and higher power input levels can be used. Refer to FCC Rules, Part 15.

The maximum permitted leakage is given by the formula:

Field Strength in Microvolts/Meter at 300 meters must be less than 2400/F (Khz).

Or: F.S in Microvolts/Meter at 30 meters must be less than 24,000/F(Khz) microvolts.

Anyone who has worked at these frequencies knows that these levels are difficult to reach, since transmission lines in a shield just do not leak that much. Also, measurement is difficult, even at 30 meters, since the normal atmospheric background noise is often in excess of this value.

There is an additional requirement that the conducted signal must not exceed 1 millivolt, except as noted in 15.207c1, where higher levels are permitted in the broadcast band.

There is no fixed set of rules that can apply, since every installation will have varying noise levels, losses and leakages. For this reason, power line modems are subject to simple "Verification" according to FCC rules.

Power line modems can be made using either a modulated carrier or a baseband signal. The baseband signal concept (similar to ETHERNET) greatly increases the data rates available.

Using a carrier as an example, one could choose a frequency of 400 Khz, which is in a relatively clear region, and modulate it with FM. The data rate would be limited to about 50 Kb/s. In this case the signal is comparable to an FM-SCA subcarrier. The circuitry is relatively simple and inexpensive. AM could be used at this frequency as well, but the use of FM with a limiter to obtain a constant output level makes FM a desirable choice. It goes without saying that suitable filters must be used, which complicates the situation. The filters must have the flattest group delay possible, which suggests BESSEL filters, which may be of the high pass type.

The signal to noise ratio should be 20 dB or better after filtering to obtain a good error rate. The use of a limiter is recommended, even though ordinary FM is not being used, to obtain a fixed output level for the decision making circuit.

There is a way to obtain much higher data

rates than those possible with an FM or any other carrier method. That is to use one of the "Biphase" codes at baseband.

Biphase codes are in common use, but often are poorly appreciated. ETHERNET wired LANs use Manchester encoding, which is a biphase code. Disk recorders in the personal computer use Miller (1) encoding, which is a biphase code that is twice as bandwidth efficient as Manchester coding. The various Slip Codes, or Walker codes (2) are the most bandwidth efficient of the known biphase codes. A newer coding method known as "Aperture Coding", or VMSK when used with an RF modulator (International Pats. Pending) is 2/3 as bandwidth efficient as the slip codes, but has other advantages.

For example, Manchester codes offer no bandwidth compression at baseband. Miller coding offers a 2/1 reduction in bandwidth, the various Walker codes as much as 15 bits/sec/Hz and VMSK about the same. All of these codes are "time, phase or frequency modulation" codes and can be limited. Any amplitude variation is undesirable.

All biphase codes concentrate the spectrum in a region as far away from zero Hz as possible, which is an advantage when using a power line modem, since the noise is greatest as the frequency approaches 0 Hz.

Manchester and Miller codes were rejected because they require too much bandwidth. The Walker 4,5,6 code was tried along with the newer aperture coded VMSK, which is similar to Manchester code transmitting all ones, but the center crossing varies in time/position for a 1 or 0 as shown by the arrows in Fig. 3.

For these tests, a 4,5,6 slip code and the 6,7(13) aperture code were used. The aperture codes were later found to offer far more advantages as will be noted. The data rate chosen was 950 Kb/s for the slip codes, since this concentrates the spectrum below 490 Khz. Walker slip codes are preferred for operation below 490KHz, since they offer the highest data rates in the narrowest BW. - 4,5,6 Walker coding has a spectrum from .36BR to .5BR. That is from 346 Khz to 475 Khz at a 950 Kb/s data rate.

4,5,6 slip code has a lower bandwidth edge of about 346 Khz, so it is a good choice if there is excessive noise in the 200 Khz region. The error angle for the 4,5,6 code is 22.5 degrees. (Equivalent to 8PSK). Higher slip codes can be used, but at the risk of too much phase distortion in the transmission path. The aperture code spectrum will be discussed later.

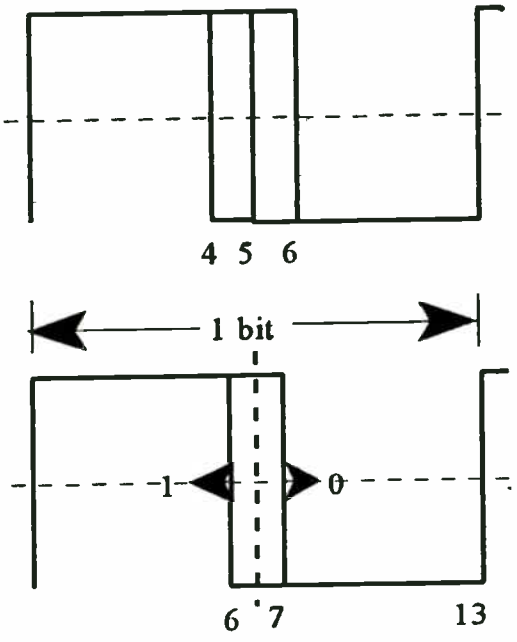


Figure 3. The Codes Used.

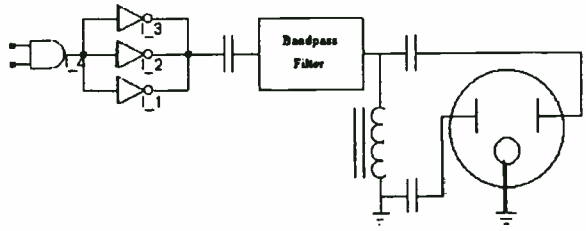
Filtering for the slip codes and the aperture codes is a problem since only BESSEL filters can be used.

An interesting feature of all biphase codes is the R factor. As the error angle decreases due to the bandwdth compression, (or increased bandwidth efficiency in bits/sec/Hz) one would expect a much higher error rate for a given noise level. This is not true, since the noise beats against the signal and the beat frequency lies outside the filter BW. The data is sampled at a rate higher than the noise beat frequency, so only a portion of the noise appears in each sample. This is the R factor, or **phase noise reduction factor**. It also applies to FM signal analysis where the final signal bandwidth is less than the RF bandwidth. For example 75 Khz deviation for 15 Khz audio has an R factor of 5. It is well known where phase locked loops are used to extend the FM knee. See Best (3) pp 49 or 57 (depending on edition.)

R = Nyquist BW/Filter BW

This factor, plus the decreased noise BW, almost completely cancels any loss in signal power due to biphase modulation at high bandwidth compression rates. In theory, the higher slip codes are 2X better than ordinary BPSK modulation and do not lose anything as the bandwidth is compressed. VPSK modulation, which uses a 10,11,12 slip code, compresses the RF bandwidth by 15.3/1- that is the bandwidth efficiency is 15.3 bits/sec/Hz, which is not achievable by any known method other than VMSK. The measured C/N value for 10-6 BER is about 13-14 dB. If this were possible using QAM, the C/N would be 55dB for the same BER. The R factor gives biphase modulation a distinct advantage over the NRZ Line Codes such as QAM, QPSK or MPSK.

The disadvantage of the higher bandwidth compression codes is that they require FIR filters to obtain the necessary flat group delay response and FIR filters can be very expensive at high data rates. High and low pass LC filters were used in these tests as a low cost compromise.



For these tests, both codes were used to drive the 74HCT04 used as a line driver as shown in Fig. 4. The nominal output current drive matches an impedance of 16 ohms so that it can drive the usual power line outlet at a +20 dBm level. Higher powers are obtainable by using power transistors. The LC filter at the output serves primarily to keep 60 Hz power away from the modem source (74HCT04). The AND gate serves to turn the power off during receive. The system is operated in a TDMA mode with carrier sensing (CSMA) to tell the users unit when to send.

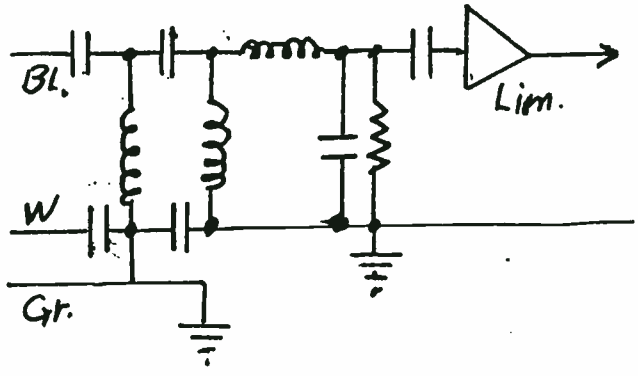


Figure 5 shows the receiver circuit, which has a high pass filter with a roll off knee around 150 Khz. This filter can affect the phase response so it must be carefully chosen and tuned. The filter output is amplified, limited and sent to the decision making circuit, or decoder chip.

Unfortunately, encoder and decoder chips for these codes (aperture and Slip) are not available in the marketplace at this time for those wishing to experiment.

The measured S/N on the experimental network using a 4,5,6 code was 35/40 dB. This was more than adequate to provide error free operation - except when a very noisy high intensity Halogen desk lamp was turned on. As mentioned above, each installation is a separate case.

Figure 6 shows the spectrum of a 4,5,6 slip code and the spectrum of the new VMSK code. Note that the slip code is 26 dB down at the nominal band edges, while the VMSK code is slightly more than 30 dB down below a very narrow center. This center is actually a single frequency, with no visual FM or AM sidebands. All of the modulation is phase modulation which does not change the frequency. It appears from this spectrum to be a form of phase spread spectrum with a fixed carrier in the middle.

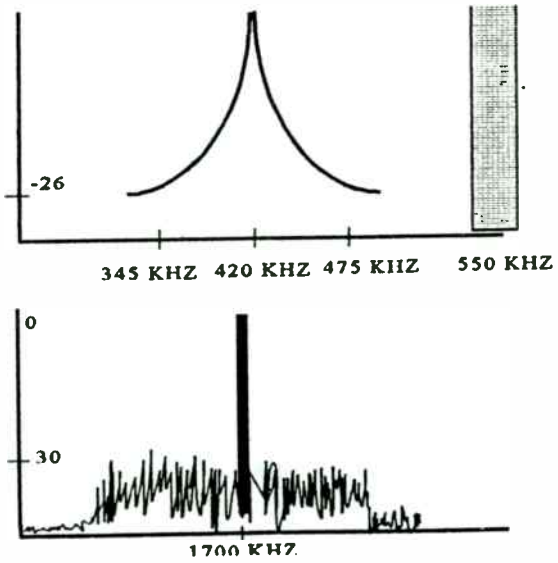
Appearances however are deceiving. The actual spectrum carrying the information is about the same as that for a slip code. The background levels observed come from the Fourier amplitude variation levels and not from the frequency or phase change. The frequency is constant, but a fairly wide bandpass filter is needed to decode the digital data.

The amazing thing is that this carrier can be modulated with a low level AM signal without interfering with the high speed data. This AM signal can be detected with a normal AM radio, so that it can be used for paging, annnouncing, security circuits etc. while the high speed data transmission is going on in the background simultaneously. Of course - only one transmitter at a time (TDMA).

The center frequency for the AM signal is the same as the data rate, so data at 550 to 1705 Kb/s can be transmitted over the circuit while complying with FCC 15.207c1. If the other codes were used, the signal power would be limited to a lower level. An experimental modem has been built carrying continous T1 (1.544 Mb/s) data and soft background music receivable on the AM receiver.

Software for a power line LAN is the same as for a STARNET or 10 Base T LAN. Several sources provide such software. Later versions of Windows, Windows for Work Groups and Windows NT, or the equivalent Apple program may be used directly. There is a Novell interface available. For those wishing to write their own, the book "Introduction to a LAN" may be of help, though it is now out of date with regard to current operating systems. The programs are written in C++ so they are transportable. The EIA-600 standard may also be used for guidance in consumer applications.

When using VMSK, (Aperture coding at RF), software written for IEEE802 use is applicable. Only the transmission method differs.



The aperture coded method described here can also be used at RF. Although it might appear that the two codes described are operating RF frequencies, they are actually baseband frequencies that can be used to modulate an RF carrier, which should be 40-60 times the data rate minimum. Thus a 1.5 Mb/s baseband signal should modulate a 60 MHz carrier. This can in turn be up converted to the desired RF transmission frequency.

VPSK (Variable Phase Shift Keying) coding is applicable to FM-SCA modulation and terrestrial microwave links. The aperture codes are used as VMSK or Very Miminum Shift Keying starters. This code can be used on satellites and other RF links as well. It is self clocking and simpler to implement that VPSK. VMSK is similar to GMSK or FSK, but the frequencies are much closer together. GMSK seeks to keep a quadrature relationship. VMSK cares only about a difference in zero crossing time for a signal consisting of the aperture coded sideband mixed with a restored carrier.

VPSK is a three frequency or three tone code. VMSK is a two frequency or two tone method. Transmission is by SINGLE SIDEBAND FM with suppressed carrier as described in the references.

It is unusual to have a SSB transmission method for data with suppressed carrier. VPSK and VMSK can restore the carrier from the data if the carrier is a mathematical multiple of the data rate. The zero crossings shown in Fig. 3 are used to create pulses that cause a ringing coil to ring at a multiple of the data rate. This ringing frequency is matched in a PLL with a frequency divided down from the carrier and used to obtain an AFC voltage. It can be shown using a dual trace scope that the transmit and receive frequencies are exactly matched.

VMSK has an advantage in that it can be used in this AFC mode (coherent) or non coherent. This is an advantage when used with satellites since there are frequency offsets that make coherent carrier restoration impossible, or very difficult.

References:

1) Miller, A. and Miller, W. U.S. Pats. 3,108,261 and 3,646,534.(MFM Pats.).

2) H.R. Walker, "High Speed Data Communications System Using Phase Shift Key Coding" U.S. Pats. 4,742,532 and 5,185,765. (Basic VPSK and "slip code" Patents.)

3) B. Stryzak and H.R. Walker," Improve Data Transmission Using Single Sideband FM With Suppressed Carrier". Microwaves and RF Magazine, Wireless Design Supplement, Nov. 1994.

4) H.R. Walker, "VPSK Modulation Transmits Digital Audio at 15 Bits/Sec./Hz". Microwaves and RF Magazine, Wireless Design Supplement, Dec. 1996.

5) R.E. Best, *"Phase Locked Loops"*, Mc Graw Hill, NYC. 1984. (Analyzes the PLL as an FM detector and the R factor).

6) H.R. Walker, "The Advantages of VPSK Modulation" IEEE Wescon, San Franscisco, Nov. 1995.

7) Craig Chaiken, " Blueprint of a LAN", M&T Publishing Inc. Redwood City, Cal., 1989.

8) EIA -600, CE Bus standard. CSMA Networking Protocol, provides physical and data link protocol functionality.

A WIDEBAND, HIGH Q, TWO FILTER NETWORK

Vasil Uzunoglu Marvin H. White

ABSTRACT

Classical networks have only one filter. If noise rejection is improved the network's data handling capacity reduces and the acquisition time increases. There is only one filter and one bandwidth. The product of noise rejection and data bandwidth remains always constant. On the other hand, in a Synchronous Oscillator the product of noise rejection and data bandwidth is optimized, by providing two internal independent filters. This paper deals with this and other functional properties, which identify and separate the classical networks from the Synchronous Oscillators. The Synchronous oscillator is an optimum network in all its functional properties. Classical networks are not optimum nor they can be made optimum.

INTRODUCTION

The design with classical networks is a constant struggle to compromise between noise, bandwidth and acquisition time. All these functions are interrelated, with noise rejection on one side and data bandwidth with acquisition time, on the other side. Moreover, the individual functions are also limited in performance. For example, in a second order PLL [1] a two pole loop filter, doesn't provide adequate filtering, while acquisition time remains slow and the data bandwidth is at the mercy of the noise rejection bandwidth, because the noise rejection filter and the data filter are the same units. There are no separated filters. The designer doesn't have much design flexibility. In a classical filter

NOISE REJECTION X BANDWIDTH=CONSTANT (1)

This implies that if we want to improve the noise rejection, the bandwidth of the filter, will shrink and the acquisition time will falter.

The Synchronous Oscillator(SO) [2-6] has solved this complex problem. by maximizing and/or optimizing expression (1). That is

NOISE REJECTION X BANDWIDTH=IS OPTIMIZED (2)

The SO does this by providing internally, two filters, namely a noise rejection filter and a data filter, which are, for all pratical purposes, independent of each other. The regeneration gain is a key factor in all operations. For example, if the regeneration gain is increased, the noise rejection improves, the bandwidth widens and the acquisition time is reduced. The SO operates similar to a spectrum analyzer. where the noise rejection filter corresponds to the resolution bandwidth of the spectrum analyzer. The SO looks at any time to the instantaneous input frequency or instantaneous data, and its immediate surrounding frequencies, through a high "Q" network and scans the entire incoming data. Fig.1 shows the movement of a noise rejection filter within the data filter. The noise rejection bandwidth can be as low as few hundred Hz wide while it can scan several MHz data. SO is the only network that can perform such a task. The noise rejection of a SO, can be made very high, the bandwidth very wide and the acquisition time very fast. On the other hand, in classical networks, such as a second order PLL, the acquisition time, the noise rejection and the data bandwidth are highly interdependent and they can not be optimized individualy nor as a product. of two functions. That is, a poor quality "Q", struggles to compromise with an insufficient data bandwidth and poor acquisition time, for a given design. In a SO, the acquisition time and the data bandwidth act as first order loops, ideal performances for any network, while the noise rejection filter remains few hundred Hz.

In classical networks, while the struggle between noise rejection, acquisition time and insufficient bandwidth goes on, their energy efficiency appears to hinder further their operational features. The classical networks are less efficient in their handling of energy.

Maxwell has pointed out "Dissipationless Network is a Distortionless Network." This

fact judges the performance of a network by its dissipation level. A distorted sinusoidal waveform is less efficient than a non-distorted one. Our choice of an LC sinusoidal oscillator, for a SO, has multiple reasons. One of the reasons is the energy efficiency. Sinusoidal waveforms have the highest energy efficiency and require the least energy, to be generated.

Although, both the classical networks and the SO use the same circuit elements, the SO performs all its functions while oscillating, with high regeneration gain while classical networks operate under high stability, and avoid oscillations.

Also, the SO has very high input signal and high input S/N sensitivities. Both sensitivities are directly proportional to the regeneration gain, so is the noise rejection. As a matter of fact, the regeneration gain and the input signal sensitivities of a SO are inversely proportional to the input signal level. This implies that the regeneration gain and the input signal sensitivities go to infinity as the input signal level tends to zero. The detectebility of the smallest possible signal is limited by the thermal noise of circuit elements. Fortunately, the effects of thermal and other noises are minimal on a SO, because of the very high "Q".

The SO is a universal multifunctional network which can synchronize, track, amplify, filter, detect, sample, modulate and divide, including rational integer numbers, such as 3/4, 5/8, etc. in a single process.

In order for the SO to perform optimally two operational requirements must be satisfied.The regeneration gain must be high and the input stimulus must not exceed -5dBm, for the SO circuit shown in Fig.2. The input stimulus is kept low, to prevent disturbance on oscillations.

Classical networks obey Bode's Integral Theorem, Paley Wiener's Realizability Criteria and Lyapunov's Stability Criteria. The SO does't obey Bode's Integral Theorem, while it complies with the realizability criteria, concerning the gain response. Lyapunov's Stability criteria does not apply for SO.

F.Kaiser [7] identified the functional properties of the SO, long before the SO existed. He quoted:"Only non-linear systems, in thermal equilibrium, not disturbed by a low level stimulus, can be optimal." This definition fits exactly the performance of a SO.

GAIN-PHASE CURVES OF A SO

Fig.3 shows the gain-phase curves of a SO. It has a wide and flat data bandwidth, with abrupt transition corners. At the bottom, the fast decaying gain of the data filter curves flatten out and don't touch the ground.

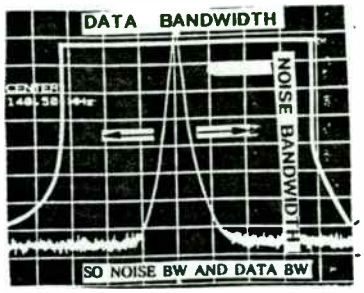


Fig.1
NOISE BW WITHIN DATA BANDWIDTH

According to Paley-Wiener Criteria, such a curve is realizable(see section on Paley Wiener Criteria). From practical considerations such a response is not realizable with classical networks, but it is realizable with a SO. The abrupt transition corner are unique for the termination of a regeneration.

According to Bode's Integral Theorem the phase curve for a gain response, shown in Fig.3, can not be linear. It should follow the sudden variations of the gain response(see section on Bode's Integral Theorem). The phase of a SO is linear and remain always 180°. SO does not obey Bode's Integral Theorem.

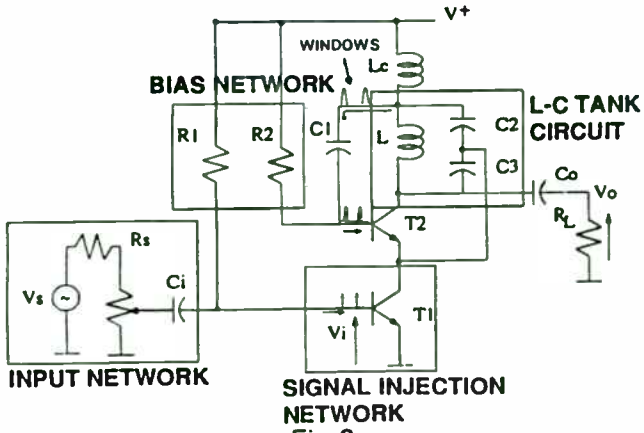


Fig.2
SO CIRCUIT DIAGRAM

SO CIRCUIT DIAGRAM

Fig.4 shows the formation of a flat and wide tracking range with abrupt transition corners. The regeneration gain and the amplitude of oscillation curves are inverse functions of each other, the product of which becomes constant, as shown in Figs 3 and 4. As long as the regeneration gain and the input stimulus energy are sufficient to compensate, for the losses in the tank circuit, the bandwidth widens. If the internal regeneration gain and the input stimulus energy are not sufficient, the regeneration, for the input signal, terminates and the data filter collapses.

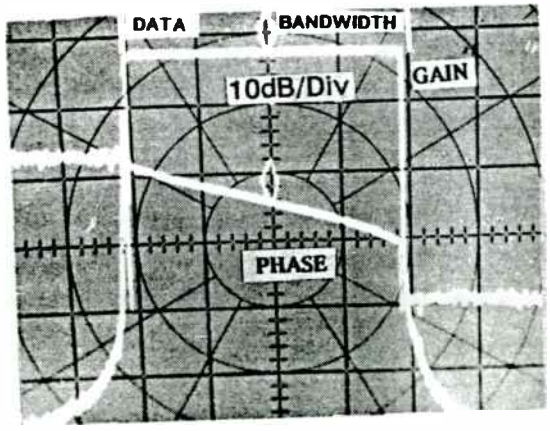


Fig.3
GAIN-PHASE CURVES OF A SO

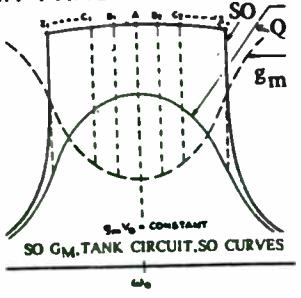


Fig.4
FORMATION OF SO RESPONSE

COMMENTS ON TWO FILTERS

The two filter technique is the only means to detect weak wideband signals, imbedded in high noise. This is assumed to be the technique by whlch dolphins, bats and sharks communicate and perform signal processing. The two filter technique in connection with the high input signal and high input S/N sentivities and high noise rejection have done away with the limited and often poor performances of bulky classical networks.

In this technique the SO looks in increments, through a very high "Q" noise rejection filter to the data and scans it. The detection, and scaning a data with 1MHz bandwidth and -20dB signal-to-noise ratio, at any frequency, is a standard procedure for a SO.

THE SAMPLING PROCESS

Fig.5 shows the sampling process in the block diagram of an SO. It can be seen also in the circuit diagram in Fig.2.

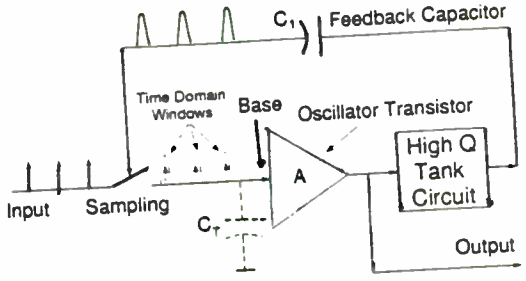


Fig.5
SAMPLING PROCESS IN A SO

The sinusoidal oscillator of Fig.2 operates in class "C" mode. This implies that the positive feedback is not continuous but occurs in bursts, between the tank circuit and the input of the oscillator. We will call these bursts as time domain window. Each time domain window performs sampling. When the window approaches the base of the oscillator circuit, it acts as a sampling network, during which time the input signal enters the window and together they become part of the regeneration process, within the oscillator. The power level of the input signal level should not exceed -5dBm. As the input is very small compared to the amplitude of oscillations, it is subject to higher regeneration gain. This is due to the self-regulation properties of the SO, which says

REGENERATION GAIN X AMPLIT.OF OSCILLATIONS (3)

is constant. This implies that the low level

signals within the SO, are subject to higher regeneration gain, until they reach the amplitude of oscillations. At this point the regenerated input signal replaces the original oscillations.

NOISE REJECTION

The SO has two internal filters. The first filter is the narrow band noise rejection filter, established by the tank circuit "Q", under regeneration and the other one the wideband data filter established by the sampling process.

We can determine the total noise rejection experimentally, by applying, a signal imbedded in noise, directly to a spectrum analyzer. as shown in Fig.6a. We apply the same signal to the spectrum analyzer through a SO. In order for the spectrum analyzer not to interfere with the noise rejection performance of the SO, the resolution bandwidth of the SO is set at 3MHz. The improvement of the S/N ratio indicates the noise rejection properties of the SO. Fig.6b shows over 40dB S/N .improvement. We can approximate the S/N improvement by

$$S/N=40dB=10\log[3MHz/\text{Noise BW}] \quad (4)$$

Solution yields for 140MHz oscillator an effective "Q

$$Q_e = 2.9\times10^6 \quad (5)$$

The "Q_e" expressed by (5) is a result of both filters, the noise rejection filter and the data filter. In the sampling of periodic signals, imbedded in high noise, the improvement in the S/N ratio due to sampling is given by (6). One of the means to realize a sampling filter is by use of tapped delay lines or transversal filters. Correlation gain is realized for a signal imbedded in noise [3] since the periodic signal in the sampling process add directly, whereas the noise adds only rms-wise. One has

$$S/N = 10\log\frac{(A+A+A.....)^2}{\sqrt{(A^2+A^2+A^2...)^2}} \quad (6)$$

which results in the expression (7)

$$S/N = 10\log N \quad (7)$$

where N is the number of samples. This implies that in sampling 1000 times the improvement can be as high as 30dB.

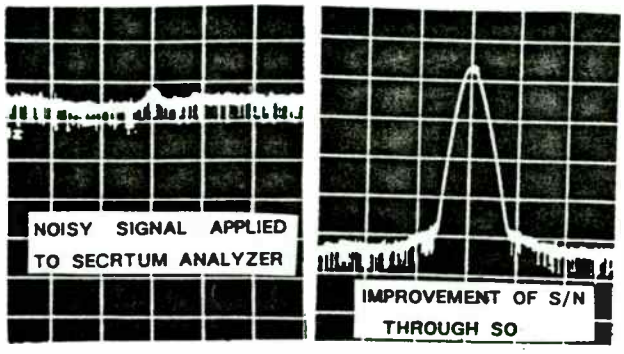


Fig.6a Fig.6b

SO NOISE REJECTION

INPUT SIGNAL SENSITIVITY

The presence of two filters, the noise rejection filter, with very high noise rejection and independent of the data filter and the high input signal and high input signal-to-noise ratio sensitivities are important findings in the area of circuits and networks. They open a new era in the design, performance and applications as well as new concept in the operation of optimun systems, including biological life. The SO will have profound effect beyond the field of electronic engineering.

The input signal sensitivity is a direct function of the regeneration gain, which controls many functions in the SO [3] including the presence of two filters, the high noise rejection, the wideband data filter and the high input signal and S/N sensitivities.

The input signal sensitivity is given by [3]:

$$S = KE_m^{-2/3} \quad (8)$$

where K is a constant and E_m is the input signal. According to exppression (8), the input signal sensitivity tends to infinity when its magnitude decreases. The limiting factor, in the detection of the lowest possible signal, comes from the thermal noise, of circuit elements. Even this has little effect on SO, because of high "Q".

Expression (3) is the heart of all operations. An oscillator exists because of expression (3). Continuous positive feedback would eventually destroy the oscillator. Whenever amplitude increases the regeneration gain automatically reduces to protect the oscillator.

Also, expression (9) provides self-regulation between the input signal and the regeneration gain:

INPUT SIGNAL X REGENERATION GAIN=Constant (9)

This implies that the regeneration gain tends to infinity as the input signal goes to zero. This expression will become clearer by presenting the amplitude curves of the oscillator along with gain curves. The output of a SO is independent of the input signal level and it is constant. Figure 7 shows the amplitude of the oscillations, while Fig.8 shows three gain curves of a SO, where the gain is inversely proportional to the input signal level. In classical networks constant amplitude implies saturation, but not in a SO. The gain variations are due to self-regulation, to keep expression (9) constant. There is no saturation in a SO, the waveforms remain always sinusoidal.

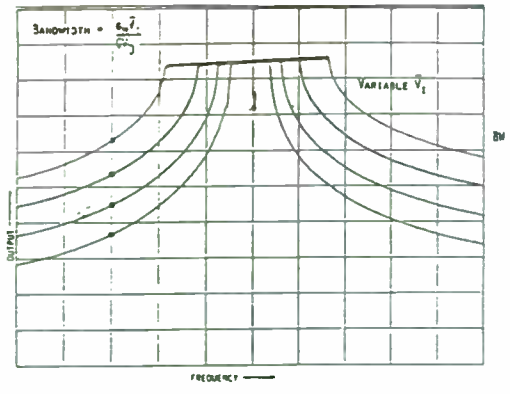


Fig.7
AMPLITUDE CURVES OF A SO

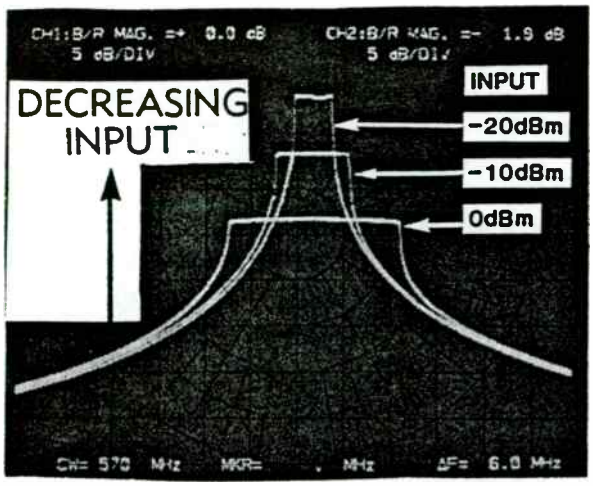


Fig.8
GAIN VS INPUT SIGNAL

DERIVATION OF EXPRESSION (3)

This simple expression is powerful, because it provides a functional property that is unique and only available in a SO, while signal processing is taking place.

The collector current of a transistor is approximated by

$$I_C = I_S[e^{qVs/nKT} - 1] = I_S[e^{\alpha Vs}] \qquad (10)$$

where I_S is the leakage current and V_S is the saturation voltage accross the base-emitter junction. This voltege has nothing to do with the sel-regulation. For a given transistor I_S and V_S are constant. The term q/nKT is 0.026 at 300°K and "n" ranges between 2 and 4 for silicon. Dividing both sides by V_{EB}, the voltage accross the base-emitter junction, we have

$$\frac{I_C}{V_{EB}} = \frac{I_S\{e^{\alpha Vs}\}}{V_{EB}} \qquad (11)$$

where I_C/V_{EB} is the transconductance, under regeneration, for an oscillator and $I_S[e^{\alpha Vs}]$ is constant. We write expression (11) as

$$G_M = K/A \qquad (12)$$

where K is constant and A is the amplitude of oscillations. In expression (12) we replaced V_{EB} with "A", since they are in phase. Any difference in amplitude is contained in K.

NOISE REJECTION ENHANCEMENT

The input signal sensitivity and input signal-to-noise sensitivity are very high, namely -100dBm and -38dB for the SO circuit shown in Fig.2. Due to circuit and P.C. board shortcommings, such as feedback and feedthrough through the PC. boad, the SO can not utilize all the advantages of its functional properties. A circuit which improves the noise rejection, is shown in Fig.9. A second tuned circuit, a Π-network, is inserted at the input. The signal-to-noise sensitivity of this circuit is 8 to 9dB better than that of Fig.2.

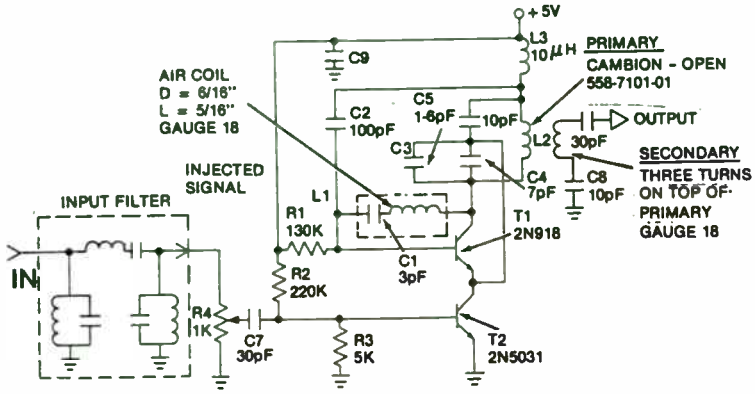


Fig.9
SO WITH NOISE REJECTION ENHANCEMENT

The skirt selectivity of the passive Π-network is increased from 24dB/3.6MHz to 24dB/10KHz, due to regeneration process. Transistor T_2 is partially under regeneration. T_1 is the oscillator transistor.

SO AS A FIRST ORDER LOOP

In three areas of operation the SO acts as a first order loop network. These are the tracking range, the acquisition time and the phase. These are ideal operational features for any network. They represent qualitativey their behavior and are given in expressions (13) through (15).

$$\text{TRACKING RANGE} = (G_M \times V_1)/(C \times V_o) = K \qquad (13)$$

$$\text{ACQUISITION TIME} = \frac{1}{K\left[1-(\Delta\omega/K)^{1/2}\right]^2} \qquad (14)$$

$$\text{PHASE} = \sin^{-1}\left[\Delta\omega/K\right] \qquad (15)$$

where G_M = TRANSCONDUCTANCE OF T_1 UNDER REGENERATION.
V_1 = INPUT SIGNAL LEVEL TO THE SO
V_o = AMPLITUDE OF OSCILLATIONS
IN EXPRESSION (14), C IS GIVEN BY

$$C = C_3[C_1 + C_3/C_2]$$

The SO acquires within 1 or two cycles, around the center frequency and phase is always +90°→0°→_90°=180°.

COHERENT PHASE-LOCKED SO

Coherent Phase-Locked Synchronous Oscillator(CPSO)[8-10] is formed using a SO with two external loops. It provides coherency(zero phase error) to the SO throughout the tracking range. A block diagram of a CPSO is shown in Fig.10. The feedforward loop carries the input signal frequency to the phase-detector, while the feedback loop carries the synchronized output frequency through a divider and a 90° phase shifter to the same phase detector. The phase detector detects the difference of phase, or the phase error, and through an integrating amplifier delivers it to the base of the oscillator, to make the resonant frequency of the SO to be equal to the input frequency. There is only one voltage which makes this adjustment. This is why the oscillator is calibrated to achieve this adjustment. The CPSO retains all the properties of the SO, while providing the coherency. In digital systems the phase error can deteriorate the BER by as much as 2dB to 3dB, for a frequency shift of ±50KHz at 140MHz.

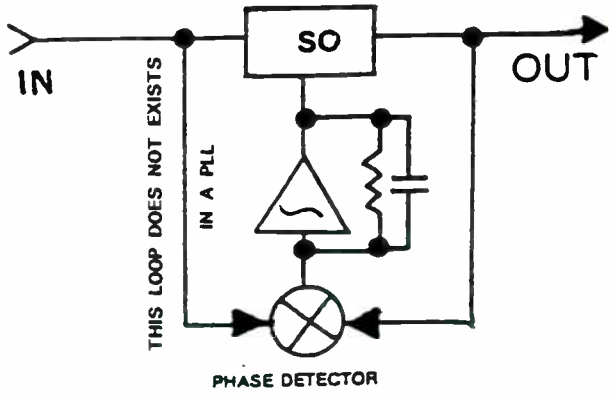


Fig.10
BLOCK DIAGRAM OF A CPSO

BODE's INTEGRAL THEOREM

The SO is not a clssical network. In a classical network an oscillator is regarded as an unstable network that can not perform linear signal processing. The SO performs linear signal processing while in oscillation. As a matter of fact, optimum performance can be achieved only by SO.

Bode's Integral Theorem [11] derives the phase of a linear network from its amplitude and vice versa. The expression below performs this translation between the phase and the amplitude behavior.

$$\phi = -\frac{1}{\pi}\int \frac{dA}{du} \log \coth \left|\frac{u}{2}\right| du \qquad (16)$$

where $u = \log\frac{\omega}{\omega_c}$

and A = Attenuation in nepers

If we set $\frac{dA}{du} = k$ = slope, we obtain

$$\phi = \frac{-k}{\pi} \int \log \coth \left|\frac{u}{2}\right| du \qquad (17)$$

The solution of $\phi = \frac{-k\pi}{2}$ (18)

k = 1 corresponds to one pole network, with 6 dB/Oct. fall-off and phase becomes $\frac{-\pi}{2}$. Likewise, for a two pole network k=2 and the phase is $-\pi$. In a SO the phase is independent of the amplitude behavior and it is determined by the tank circuit. For a two pole tank circuit the phase is $-\pi$, no matter what the amplitude behavior is. The amplitude characteristic of a SO is ideal or near ideal, according to classical network theories. and ideal gain curves can not have linear phase The phase of a SO is linear and it is always $-\pi/2 \rightarrow 0 \rightarrow +\pi/2$. Ideal amplitude curves can not be realized, according to classical theories.

PALEY-WIENER CRITERIA

Paley-Wiener Realizability criteria sets the rules for the realizabilty of classical networks. The necessary and sufficient condition for the gain function to be realizable, the following must be true.

$$\int \frac{\log [A(j\omega)]}{1 + \omega^2} d\omega \quad < \infty \qquad (19)$$

In the above expression

$\log [A(j\omega)] = \omega^2$

so that the integral

$$\int \frac{\omega^2}{1 + \omega^2} d\omega \qquad (20)$$

is not finite.

Fig.3 shows the gain and phase curves of a SO. Note the steepness of the skirt selectivities and the phase remains always 180°. Figures 11a and 11b . show the gain functions which are not realizable, while Fig.12 shows the gain function which is realizable. theoretically. A network to be realizable must follow two rules: the gain function can not fall-off faster than exponential order and it can have infinite rejection for discrete set of frequencies, but it can not have infinite rejection over a band of frequencies. The gain functions of Figures 11a and 11b can not be realized, because it has infinite rejection on either side of band, while the network of Fig.12 is theoretically realizable The gain function does not reach zero level. This is true, at least theoretically. Network of Fig.12 can not be realized with classical networks, but it can be realized with a SO.

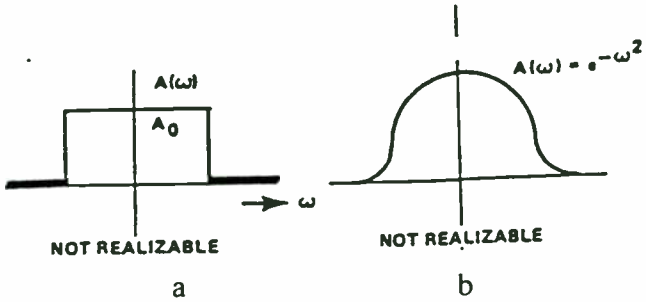


Fig.11
NOT REALIZABLE GAIN FUNCTIONS

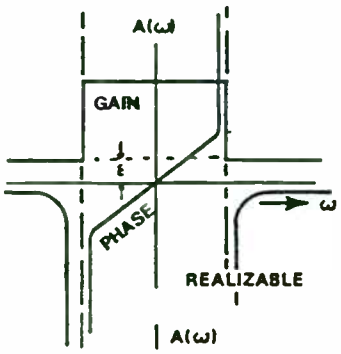


Fig.12
REALIZABLE GAIN FUNCTION

AUDIO FILTERING & MODULATION

Transversal equalizers were used for filtering audio signals, music and in reduction of noise in medical instruments [12].Transversal equalizers were used also for reducing the BER in satellite modems [13]. The transversal equalizer, shown in Fig.13 was never commercialized in quantities, because of its cost and bulkiness. Here, the output of the transversal equalizer and the noise are subtracted from each other to recover the signal. The noise transducer is connected to the source of the noise, which may be one of the walls of the room. On the other hand digital transversal equalizers were used in telephone lines. With the introduction of the Synchronous Oscillator and the Coherent Phase-Locked Synchronous Oscillators transversal equalizers have lost their importance and their demand is limited.

A low power, audio filtering and modulation network, is shown in Fig.14. It is one transistor SO with β>150. This gain is enough for the SO to generate the proper regeneration gain to provide the necessary, narrow-band, noise rejection filter.

The filtering and the modulation are performed in two simultaneous steps First, when the audio and the associated window enter the oscillator, the base-emitter junction capacitor converts the audio variations into frequency variationss. Low amplitude frequency variations become part of the regeneration process and they are amplified until they reach the amplitude of oscillations. At that stage the original oscillations are replaced with the regenerated input signal and start tracking the input frequency variations. Fig.15a, Fig.15b and Fig.15c show FM, AM and chaotic operations of the SO. For FM operation the input audio should not exceed -10dBm, while for AM operation the input should range between -5 and 0dBm. In the AM operation, shown in Fig.15b, appearently, the input signal was not high enough to provide higher index of modulation.

A noisy low frequency sine wave was applied directly to an oscilloscope, as shown in Fig.16a. The same noisy sine wave was applied to the oscilloscope through a SO The improvement of the S/N is approximately 15dB, as shown in Fig.16b Higher regeneration gain for higher noise rejection is possible

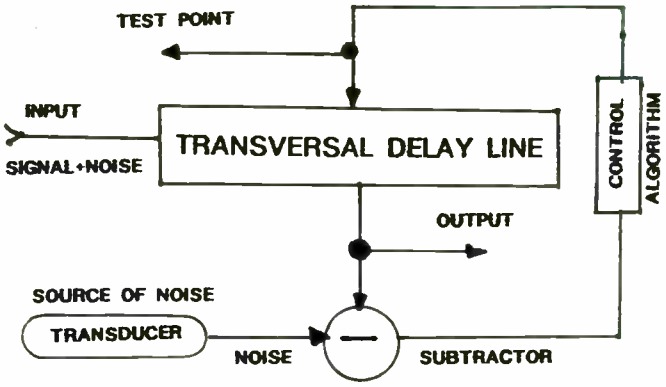


Fig.13
TRANSVERSAL EQUALIZER

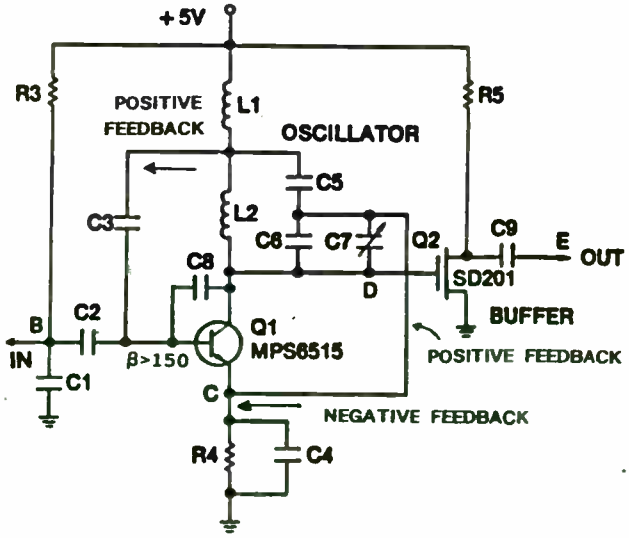


Fig.14
AUDIO FILTERING SO

by increasing the β of thransistor or the passive "Q" of the tank circuit or the supply voltage. These modulators are small, low power transmitters. The audio can be demodulated by a discriminator at the output of the modulator or simply by using the modulator as a transmitter and picking up the audio by a FM receiver.

Such modulators or transmitters were built on a chip, using ring oscillators.

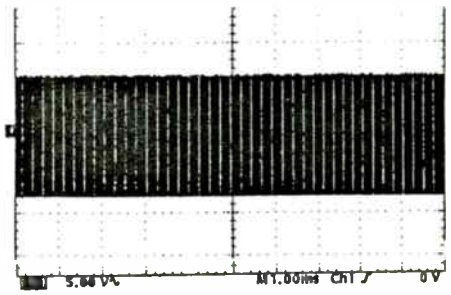


Fig.15a
FM MODULATOR OUTPUT

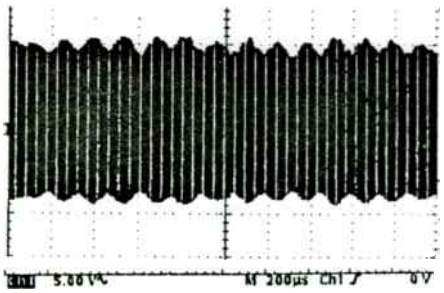


Fig.15b
AM MODULATOR OUTPUT

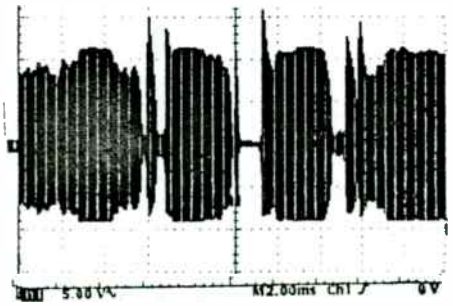


Fig.15c
CHAOTIC OPERATION

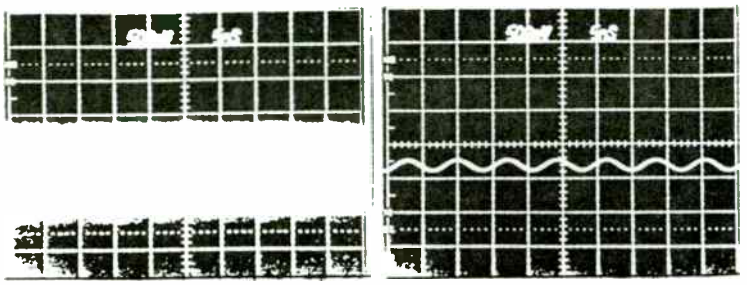


Fig.16
AUDIO NOISE ELIMINATION

REFERENCES

1. Lindsey C.William, "SYNCHRONIZATION SYSTEMS in Communications and Control", Prentice Hall, Inc., Prelude.
2. Vasil Uzunoglu and Marvin H.White, "An Optimum Network for Spread Spectrum and Digital HDTV", Proc.of the Fourth Annual Wireless Symposium, pp.270–277.
3. Vasil Uzunoglu, Marvin H.White "Synchronous Oscillator and Coherent Phase–Locked Synchronous Oscillator: New Techniques in Synchronization and Tracking", IEEE Trans. on Circuits and Systems, Vol..36, No.7, 1989, pp.997–1024.
4. Vasil Uzunoglu, Marvin H.White, "Synchronous Oscillator as a Synchronization and Tracking Network", IEEE Journal Solid State Circuits, pp.1224–1226, Dec.1985.
5. Vasil Uzunoglu, Patents # 4,335,404, # 4,274,067, # 4,356,456.
6. Andre Kestelot, "A Direct Sequence Spread Spectrum UHF Direct Link", QST, May 1989.
7. F.Kaiser, Uslenghi, Academic Press, "Non–linear Electromagnetic Waves", Chapter 1.
8. Vasil Uzunoglu, "Coherent Phase–Locked Synchronous Oscillator", Electronic Letters, 25th September, 86, Vo.22, pp.1060–1061.
9. Zhigang Ma, Marvin H.White, "A High Performance Coherent Phase–Locked SYnchronous Oscillator", 35th Midwest Symposium on Circuits and Systems, August 9–12, 92.
10. Vasil Uzunoglu, Marvin H.White "Coherent Phase–Locked :Synchronous Oscillator–Graphical Design", IEEE Trans. on Circuits

and Systems, Vol. 40, Jan. 1993.
11. H.W.Bode, "Network Analysis and Feedback Amplifier Design", Van Nostrand Comp.Inc., Princeton, New Jersey 1945.
12. B.Widrow, John M.McCool, Charles S.Williams, Robert H.Hearn, James R.Zeidler, Eugene Dong Jr., Robert C. Goodlin, John R.Glover and John Kaunitz, "Adaptive Noise Cancelling: Principles and Applications", Proc. of the IEEE, 63, (12), pp.1692–1716, 1975.
13. Vasil Uzunoglu, "SIXTY Mbit/s TRANSVERSAL EQUALIZER", International Journal of Satellite Communications, Vol.5, pp.13–21, 1987.

A Self Calibrating Quadrature Generator with Wide Frequency Range

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Abstract- A quadrature local oscillator generator that produces 0° and 90° amplitude matched signals over a wide frequency range was fabricated using a high performance bipolar technology. This circuit employs a unique phase shifting circuit combined with an improved high frequency phase detector to produce quadrature outputs. RC based circuits, which have typically been used to generate high frequency quadrature signals, can operate only over a narrow frequency range. Other quadrature generation methods such as frequency dividers use a reference LO frequency at least twice that of the desired quadrature signal and require a duty cycle adjustment circuit which has bandwidth limitations. The circuit described in this paper operates over a frequency range of 400MHz through 700MHz with low amplitude and phase imbalance.

An accurate phase shifter is necessary for communication receivers using an image reject mixer or I/Q downconverter[1][2][3]. The utilization of an image reject mixer eases the requirements of the image filter. Similarly, an I/Q demodulator relies on zero-IF filtering for most of its selectivity, therefore reducing the need for mechanical filters. This circuit utilizes a delay locked loop (DLL) to produce quadrature outputs. The DLL is fully integrated including the loop filter and utilizes a differential architecture. Integration allows the circuit to be self calibrating. The DLL produces quadrature signals which are insensitive to changes in temperature, process, frequency or amplitude.

Fig. 1 depicts the delay locked loop as implemented in the quadrature generator. A Local Oscillator (LO) signal is applied to a single-ended to differential buffer. The output of this buffer drives both the phase shifted and non-shifted paths. The phase shifted path includes a current controlled phase shifter which is followed by a limiting amplifier. The phase shifter delays the incident signal by an amount controlled by a phase detector. The non-phase shifted path includes another limiter matched to the first one. These limiting amplifiers remove gain imbalance introduced by the phase shifter. The outputs of the limiting amplifiers are applied to the phase detector which is based upon an analog multiplier. The phase detector output is filtered and applied to the phase shifter resulting in an output signal phase locked to the reference with a 90° phase offset. The limiting amplifiers also drive matched output buffers which have been designed for 50Ω matched interfaces.

Stacked architectures are commonly utilized in phase detectors to reduce current consumption. A disadvantage of these circuits is the unequal propagation delays between the inputs. The net effect is a non-zero output when the input signals are at the desired phase shifts. This result is detrimental at high frequencies where the inherent propagation delay becomes a significant fraction of the signal time period. The low pass filtered output of an ideal analog multiplier used as a phase detector has a low pass filtered transfer function defined by (1) for inputs $A\cos(\omega t+\alpha)$ and $B\cos(\omega t+\beta)$. This phase detector will have zero DC output when $\alpha-\beta=90°$.

$$z = \frac{AB}{2}\cos(\alpha-\beta) \qquad (1)$$

A similar phase detector which includes propagation delays differing by Δ, has a low pass filtered transfer function defined by (2). This phase detector will have zero DC output when $\alpha-\beta=\Delta+90°$.

$$z = \frac{AB}{2}\cos(\alpha-\beta-\Delta) \qquad (2)$$

Fig. 2 depicts a cross-coupling method which uses two phase detectors to reduce the effect of unequal propagation delays. The low pass filtered transfer function of this arrangement is defined by (3). The simulated phase error introduced by the phase detector is improved from 10° to under 0.1°.

$$z = AB\cos(\alpha-\beta)\cos(\Delta) \qquad (3)$$

The delay circuit uses two cascaded emitter followers each biased by variable current sources to drive capacitors and provide the appropriate delay. The simplified circuit schematic of a phase shifter is shown in Fig. 3.The phase delay of a single delay stage is defined by (4).

$$\angle\frac{V_o}{V_i} = \operatorname{atan}\left[-\frac{2\pi f C V_T}{I}\right] \qquad (4)$$

It can be seen by (4) that if only one emitter follower stage was used, a bias current of zero would be required to achieve the 90° phase shift. This constraint necessitated the use of at least one additional phase shifter.

The quadrature generator was evaluated in an SO-8 package mounted on an FR4 PC board using microstrip lines for all high frequency connections.

Fig. 4 shows the measured phase and amplitude error versus frequency for the quadrature

generator. Phase error is defined as the deviation from the expected 90° separation and amplitude error is defined as the difference in the output powers. Less than 1° of phase error was achieved over the frequency range of 435MHz to 660MHz.

Phase noise contribution of the quadrature generator is minimal. Fig. 5 shows the phase noise of the quadrature generator's input source and the phase noise of each of the quadrature generator's outputs. This result shows that the DLL does not degrade the phase noise of either signal.

Greater than 40dB of isolation was measured between the input signal and the outputs as well as between the two quadrature outputs. The actual phase separation of the quadrature outputs will be the vector sum of the intended signal plus the coupled signals. For instance, the coupling of a 90° phase shifted signal with a 0° phase shifted signal, 40dB lower in amplitude, results in a vector of 89.4° and negligible amplitude change. Lower phase error can be expected when the quadrature generator drives mixers located on the same die rather than driving low impedance external loads.

The quadrature generator operates with a 3V power supply and draws 8mA of current. Current drain is increased by another 4mA to accommodate the low impedance buffers which are used only for evaluation purposes to drive test equipment (50Ω loads).

Fig. 6 shows the plot of the test IC that was fabricated with Motorola's MOSAIC V™ high performance silicon bipolar process to validate the design concepts described by this paper.

References:

[1] Jan Crois and Michael Steyaert, "A Fully Integrated 900MHz CMOS Double Quadrature Downconverter," ISSCC Digest of Technical Papers, pp. 136-137, Feb. 1995.

[2] Asad A. Abidi, "Direct-Conversion Radio Transceivers for Digital Communications," IEEE Journal of Solid-State Circuits, Vol. 30, No. 12, pp. 1399-1410, Dec. 1995.

[3] Shoji Otaka, et. al., "A Low Local Input 1.9GHz Si-Bipolar Quadrature Modulator with No Adjustment," IEEE Journal of Solid-State Circuits, Vol. 31, No. 1, Jan. 1996.

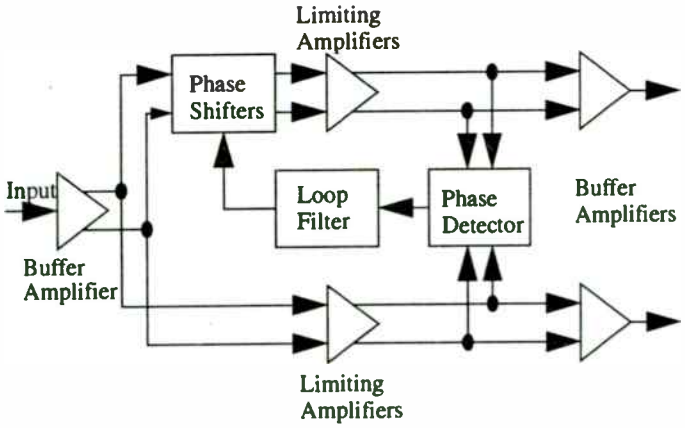

Fig. 1. Quadrature Generator with Delay Locked Loop

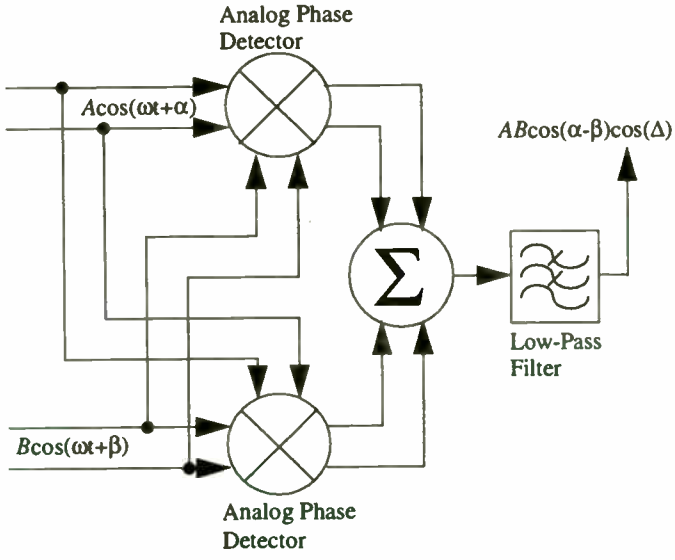

Fig. 2. Phase Detector block diagram

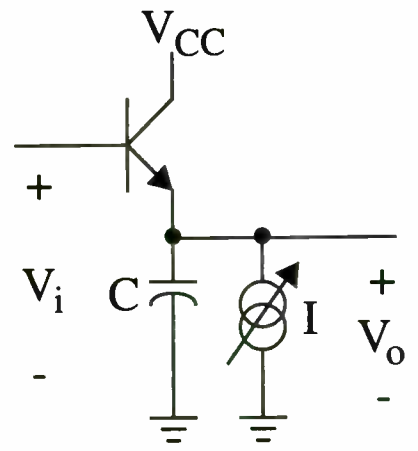

Fig. 3. Phase shifter schematic

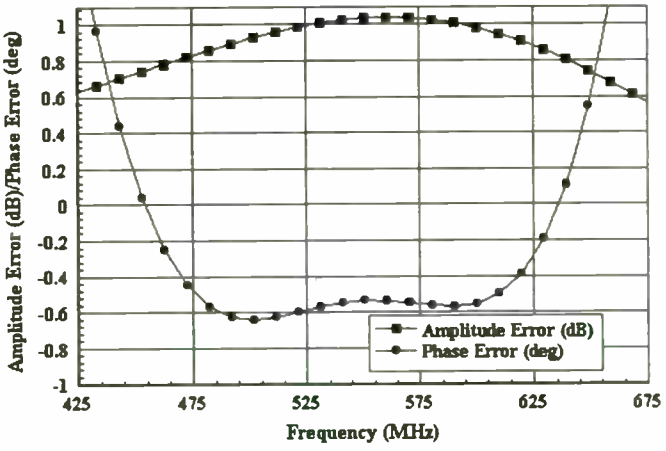

Fig. 4. Amplitude and phase error versus frequency

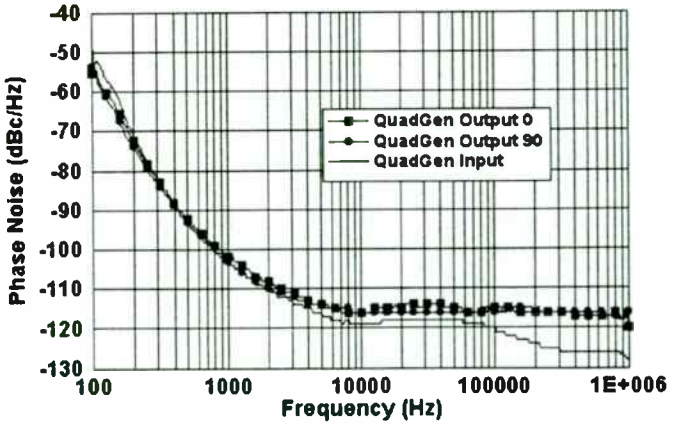

Fig. 5. Phase noise of quadrature input and each output

DIGITAL COMMUNICATIONS SYSTEMS

Digital Communications Systems

Session Chairperson: Eric Schmidt,
California Eastern Laboratories (Santa Clara, CA)

Design, Simulation and Analysis of CDMA Communication Systems

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This paper focuses on some of the special techniques that are useful for the simulation of CDMA systems and spread-spectrum systems, in general. Topics covered include efficient simulation architectures for fast Bit Error Rate (BER) simulations, combined Monte-Carlo and analytical evaluation, fast algorithms for synchronization, and evaluation of error-control coding performance.

I. Introduction

Spread-spectrum techniques have been employed in military communication and radar systems for about 50 years. The primary purposes in communications have been to combat the effects of jamming and to effect covertness. In radar systems, the primary purpose has been to provide accurate ranging (delay measurement). Numerous books and papers have been written on spread-spectrum techniques used for these purposes over the years.

Spread-spectrum techniques are also useful in commercial applications, although the motivation to apply such techniques to these applications has developed only fairly recently. The most important use of spread-spectrum techniques in the commercial world is in multi-user communications. Spreading the signal of multiple users with a unique spreading waveform assigned to that user can allow simultaneous access to a shared communication channel. This technique is called Code-Division Multiple-Access (CDMA) and forms the basis of the IS-95-A standard. Many papers have been published on CDMA techniques over the years, but the first textbook devoted to CDMA appeared but recently [1].

CDMA systems can provide superior multiple-access capabilities, in addition to a number of other desirable attributes for wireless cellular service. These attributes include optimum subscriber station power management, universal frequency reuse, soft handoff, and enablement of the use of optimum receiver structures for time-varying multipath fading channels. We assume that the reader has some familiarity with CDMA principles. We provide a basic description of the architecture of the IS-95-A forward (base station to subscriber) and reverse (subscriber to base station) links in the next section.

In this paper, we discuss some important issues for the system-level modelling and simulation of CDMA systems. The wide bandwidth generally associated with spread-spectrum systems normally requires large sampling rates within digital transceivers that are now commonly used to implement such systems. Simulation on digital computers has now become a popular evaluation technique for performance assessment of communication systems. In this technique, all components of an end-to-end communications link must be represented with adequate fidelity, including channels and analog components. System-level simulations of links normally employ a sampled-data representation of analog signals, incurring lengthy run times due to high sampling rates and the associated large volumes of data processing.

This paper discusses certain techniques for implementing efficient simulations of CDMA systems. We begin by discussing the various levels of modelling abstraction and system evaluation that are involved in a communication system's life cycle. We next discuss efficient architectures for the simulation of wideband systems. This primarily involves techniques for moving and synchronizing large amounts of data between the various subsystem and component models participating in the simulation. We also discuss channel models of varying levels of complexity within the specific context of mobile cellular radio. We then demonstrate how these models can be used in both coded and uncoded system performance evaluations.

Throughout the remainder of this paper, we illustrate basic CDMA concepts with example simulations of the IS-95-A CDMA standard [2-3].

II. Efficient Behavioral-Level Simulation of CDMA Systems

The modeling and simulation process is often applied at different stages in the life cycle of engineering systems. At the conceptualization stage, simulation is typically used to explore "what if" scenarios involving tradeoffs of major design choices. In design of wireless systems, the designer may need to select from various modulation schemes and/or error-control coding types to enable efficient transmission over a given channel. If a communication standard has already been specified, the designer might be tasked with developing an appropriate transceiver architecture for implementing the standard. Both of these scenarios involve characterizing the system

at the *behavioral* level. At this level, we are interested in assessing the idealized behavior of the algorithms involved in the overall system design. This level of modelling abstraction is often called *system-level* modelling. To avoid confusion in what follows, we will refer to this level of modelling as behavioral-level modelling. End-to-end performance measures such as Bit Error Rate (BER) are used to characterize system performance at this level. The next stage in the design cycle is the characterization of the non-ideal behavior of the various components and subsystems that will be used to physically implement the design. This type of assessment can be performed by the various modelling and simulation packages available for simulation of circuits and devices. Programs like SPICE provide accurate modelling facilities for ordinary electronic circuits. There are also many simulation tools for RF and microwave circuits. These circuit and hardware-oriented programs generally model electronic systems at a much greater level of detail than that required at the behavioral level. In behavioral-level modelling, the differential equations describing the system under study are often approximated with finite-differences. Circuit-level modelling usually involves a direct iterative solution of a set of coupled differential equations within an arbitrary accuracy. There is thus a trade-off between accuracy and computational complexity that arises between the various modelling techniques that are in common use. Ideally, a mixture of abstraction levels could be combined into a single modelling environment. This would afford the user the ability to model critical portions of the system at the circuit level, with the remainder of the system model composed of system-level elements. To date, an effective multi-level environment has not emerged. In what follows, we will focus on techniques for efficient behavioral-level modelling and performance analysis. We will see that there are trade-offs between speed and accuracy even within the behavioral level.

A major goal of behavioral-level simulation and analysis is the characterization of the long-term statistical performance of the system under study. In many cases of interest to the system designer, the events that are to be characterized occur only rarely. Bit errors are an obvious example of rare events that need to be characterized in communication system performance evaluation. In cases where rare events need to be observed, it is necessary to generate correspondingly large amounts of data. To ensure statistical significance of empirical results, it is prudent to observe 10-100 of the events that are to be statistically characterized. In the case of independent bit errors, for example, this requires the generation of a number of bits 10-100 times the inverse of the bit error rate. Thus the tabulation of a bit error rate of 0.0001 requires one hundred thousand to one million symbols to be processed. If an entire system were to be modelled at the circuit level, realistic statistical simulations would not be possible on today's computers.

We will next describe the basic architecture of the IS-95-A system, which we use as an example to illustrate the special modelling requirements of CDMA systems.

III. IS-95-A CDMA Basics

The digital IS-95-A standard employs Direct-Sequence (DS) spectrum spreading by multiplying the user's narrowband waveform by a wideband signal. This wideband signal is generated by spreading "codes" consisting of sequences of 64 "chips," associated with each symbol interval. The entire sequence of chips is used to modulate the carrier during each symbol period, resulting in a widened or "spread" spectrum. The underlying information sequence is mapped into the chip sequence in different ways in the forward vis-à-vis the reverse channel. In both cases, the characteristics of the spread-spectrum signal provide some important advantages.

A block diagram of the base station to subscriber link is shown in Fig. 1. This link is called the Forward CDMA Channel. This link operates coherently, enabled by the transmission of a pilot signal. In this paper, we will discuss only the forward traffic channel. We will not discuss the sync and paging channels here. The implementation of these channels is straightforward. Within the diagrams in this document, we employ a small circle around the operator within summation or multiplication icons to indicate that the operation is performed over a binary field of {0,1}.

The Forward link is capable of accepting information bits at the rate of 0.8 Kbps, 2.0 Kbps, 4.0 Kbps and 8.6 Kbps. Channel symbols are transmitted in frames, with each frame containing a number of information bits and a convolutional encoder tail sequence to drive the convolutional encoder into a known state at the end of each frame. Additionally, the frame incorporates a frame quality indicator sequence for the two highest data rates. The frame quality indicator sequence is nothing but a set of parity check digits that detect errors in the frame. It is also used to establish the incoming data rate at the subscriber station.

After the possible addition of the check digits and the addition of the tail bits, each frame is convolutionally

encoded with a rate = 1/2 constraint length 9 convolutional encoder with tap connections = {753, 561} (Octal).

Depending on the data rate, the encoder output sequence is repetition-encoded by a factor of 1 (no encoding), 2, 4 or 8. This brings the final baseband symbol rate up to a constant 19.2 Kbps.

A block interleaver of special design is employed to interleave and permute the order of the baseband symbols before transmission.

After interleaving, the baseband sequence is scrambled by a "long code generator," the decimated output of which is modulo-2 added to the baseband symbol stream. The long code output is also used to randomize the placement of a power control bit within the baseband symbol stream.

The power control bit is generated at an average rate of 800 bps in response to changing received SNR conditions at the Base station. The power control bit commands the subscriber equipment to either raise or lower its power output to achieve adequate but not wasteful received power levels. This is a key element in both the superior capacity and power efficiency attributes of CDMA cellular systems.

After multiplexing, the baseband symbol stream is spread by multiplication with a Walsh sequence of length 64, thus creating a baseband "chip" sequence at a rate of 1.2288 Mcps. There are 64 orthogonal Walsh sequences of length 64, certain of which are assigned to different users of the channel. All users' transmissions occur synchronously from the base station, so these transmissions are also synchronized at any individual subscriber's receiver. The use of a set of orthogonal sequences thus allows perfect rejection of other-user interference associated with any given transmission path.

The baseband sequence is finally BPSK-modulated on both the inphase (I) and quadrature (Q) channels. The same baseband sequence is duplicated on both channels, then spread with different pilot sequences on the I and Q channels. This technique allows independent despreading and amplitude measurement of both channels. This, in turn, allows the embedded pilot sequence to be employed for channel sounding purposes to determine the amplitudes and phases of various multipath components received at the subscriber station.

After spreading by the pilot sequences, the chip sequences are passed through identical baseband filters to produce the baseband I/Q modulating signals. The filters are specified in the IS-95-A standard on the basis of a spectral mask and allowed mean-square deviation from a discrete-time impulse response. The impulse response is specified at 4 samples per chip with length 48, the same rate and length as the baseband filters in the Library. Fig. 1 indicates that each channel is applied to an individual

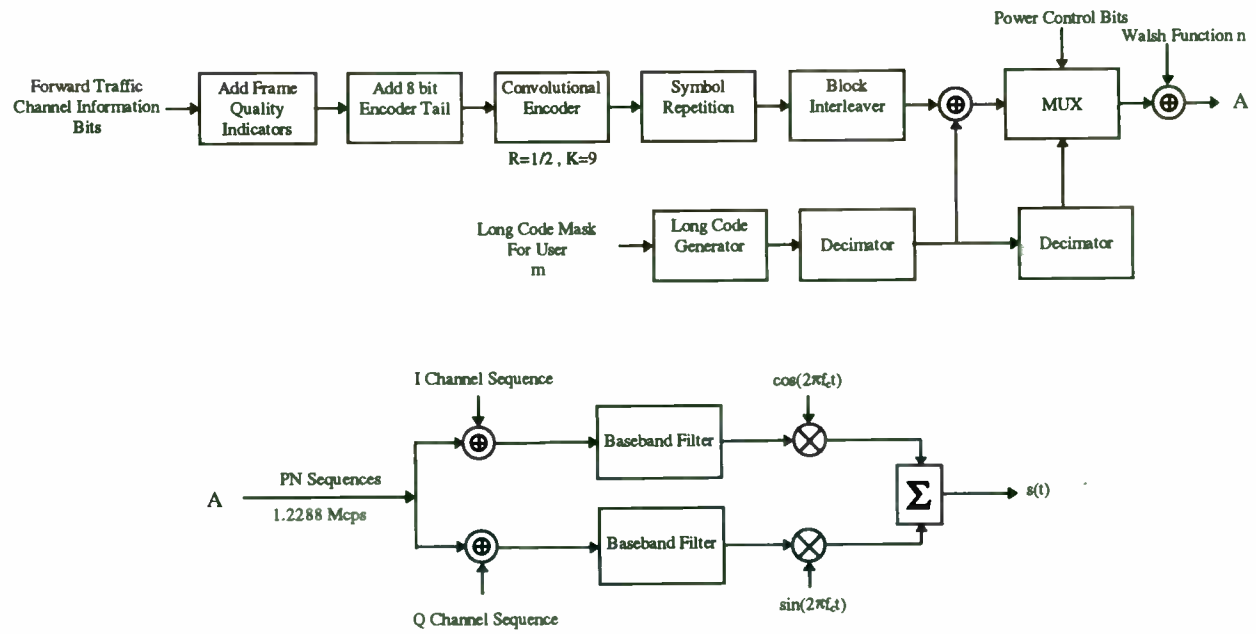

Fig. 1. Forward CDMA Channels.

modulator. In this case, the various signals, s(t), would be added together to form a composite multi-user signal. In practice, the signals might be combined algebraically at baseband before being input to the modulator.

At the receiving end, the IS-95-A specification is silent on the specific architecture of the subscriber receiver. It does, however, refer to the IS-97 "Recommended Minimum Receiver Performance Standards for Base Stations Supporting Wideband Spread Spectrum Cellular Mobile Stations," which supplies general minimum operational performance specifications. The generic receiver architecture commonly used in IS-95-A systems is known as a "Rake" receiver. This is a multipath reception technique that attempts to perform what might be deemed an obvious procedure for combining multiple received signals. The Rake technique attempts to time-align the various delayed paths and add them up again. The paths must be weighted in an optimum fashion, which depends heavily on the long-term fading statistics of the various received paths. If the Rake receiver additionally attempts to extract and exploit information concerning the phase of the received paths, the Rake receiver is deemed coherent. Due to the presence of a pilot sequence in the forward IS-95-A transmitted signal, subscriber receivers usually employ a coherent technique. A description of Rake receivers can be found in [4].

In the context of cellular mobile radio, Rake receivers have two functions. The first is to periodically perform measurements on the time-varying channel to determine the multipath structure (delays, amplitudes and possibly phases) and track its changes over time. This is often called channel "sounding." Since the multipath structure of mobile radio channels is usually changing more rapidly than "quasi-static" multipath channels (like HF and TROPO, for example), this aspect of the receiver's operation becomes critical. For a given multipath structure, the Rake receiver must then act by combining a selected number of received paths in some optimum or approximately optimum fashion. The number of paths to be combined is often fixed as part of the receiver specification, so the receiver usually attempts the recombining of

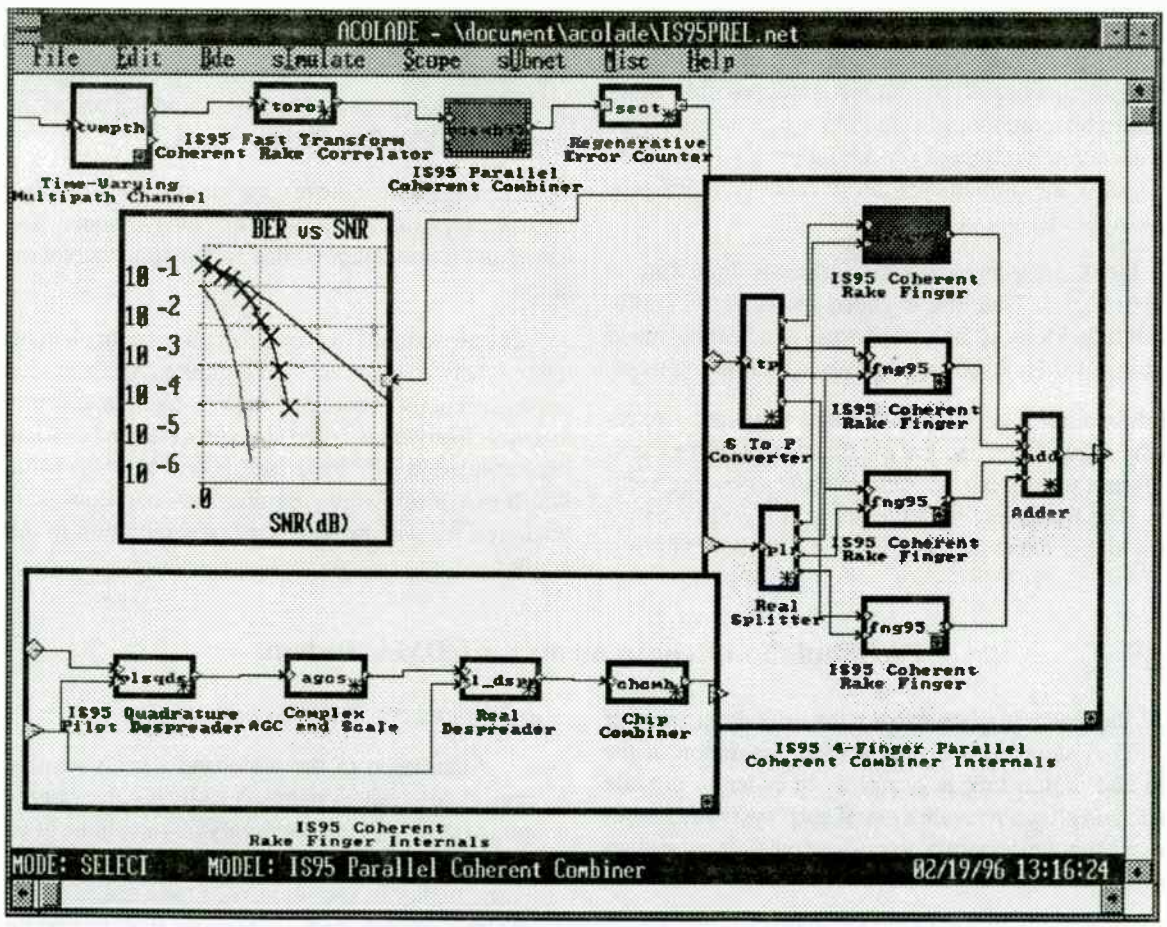

Fig. 2. Parallel Rake Finger Combiner.

the N strongest received paths. N typically ranges from 3 to 6 in most Rake receivers.

The Rake receiver may be implemented with a variety of structures, each with its own set of advantages and disadvantages. Classically, Rake receivers have been implemented with a number of discrete receiving elements, called "fingers" of the Rake. This is most appropriate for implementation with monolithic components, used to actually implement the several fingers. A model of this approach is shown in Fig. 2, where a parallel Rake finger combiner is illustrated, along with the internal details of one of its fingers. On the other hand, modern DSP technology has made it possible to perform more and more baseband functions within programmable chips or ASIC's. In this case, individual paths may be processed serially. With this type of implementation, certain DSP techniques make it possible to perform some of the receiver functions very efficiently. These and other techniques may be mixed and matched in any given receiver design.

The IS-95-A subscriber-to-base station link employs a noncoherent transmission technique. Generally, the subscriber equipment is power-limited, hence transmission of a separate pilot sequence to enable coherent operation is not attractive. The determination of multipath structure and subsequent path combining is still possible, however, with a bit more sophisticated signal processing. Since the base station equipment can be larger (and generally more costly), the implementation of more complex processing is usually not problematic.

A block diagram of the subscriber-to-base link is shown in Fig. 3. This link is called the Reverse Traffic Channel link. Many of the components will be recognized from the forward link, but some are used in different ways.

Information rates and the channel signaling rate remain the same, but some intermediate rates differ based on different processing, modulation and encoding techniques. The frame quality indicator is still employed for the two higher data rates, as well as the encoder tail bits.

In this case, a rate = 1/3, constraint length 9 convolutional code is employed, which provides a greater output symbol rate than the forward channel encoder.

The code symbols are again repeated for all data rates except the highest and input to the same type of block interleaver.

In the reverse link, the Walsh codes are employed at this point to provide a noncoherent orthogonal sequence modulation technique. The Walsh modulator accepts the six bits needed to create an index for the set of 64 64-ary orthogonal sequences which may be transmitted. This produces a Walsh chip rate of 307.2 kcps.

A "data burst randomizer" is employed to delete all but one copy of each code symbol from the symbol stream that is eventually transmitted. The randomizer operates by dividing each frame into 16 groups of 6 64-ary modulation symbols and determining which of the 16 groups is to be transmitted. The transmitter is to be gated off during periods of no transmission. The long code generator spreads the randomizer output with four PN chips per Walsh chip, giving a final output chip rate of 1.2288 Mcps. The baseband modulating sampled-data waveforms are created in the same fashion as in the forward channel, with the exception of a one-half chip delay imposed on the quadrature channel. Thus, the modulation on the reverse channel is offset QPSK.

The receiver for the reverse channel is still usually of the Rake type, although the processing is somewhat different and more complex, due to the noncoherent modulation.

The demodulation process involves noncoherent correlation between the received complex Walsh-modulated sequence and 64 candidate Walsh sequences to determine that most likely transmitted. This process can be efficiently implemented in DSP hardware, however, in the form of a Walsh transform, which requires only additions and subtractions. We will provide further elaboration in the examples.

IV. Simulation Requirements for CDMA Systems

As the reader may glean from the brief description of the IS-95-A standard provided above, simulation of the end-to-end digital link is complex. In order to provide realistic and effective evaluation of such systems, a modelling and simulation tool must possess the following characteristics:

a) Fast and efficient data processing

Simulation of the wideband signals involved in spread-spectrum systems typically involves large sampling rates. A correspondingly large volume of data is required to be passed between the various model blocks participating in a simulation. Statistical performance analysis of such systems requires that data be moved and processed efficiently.

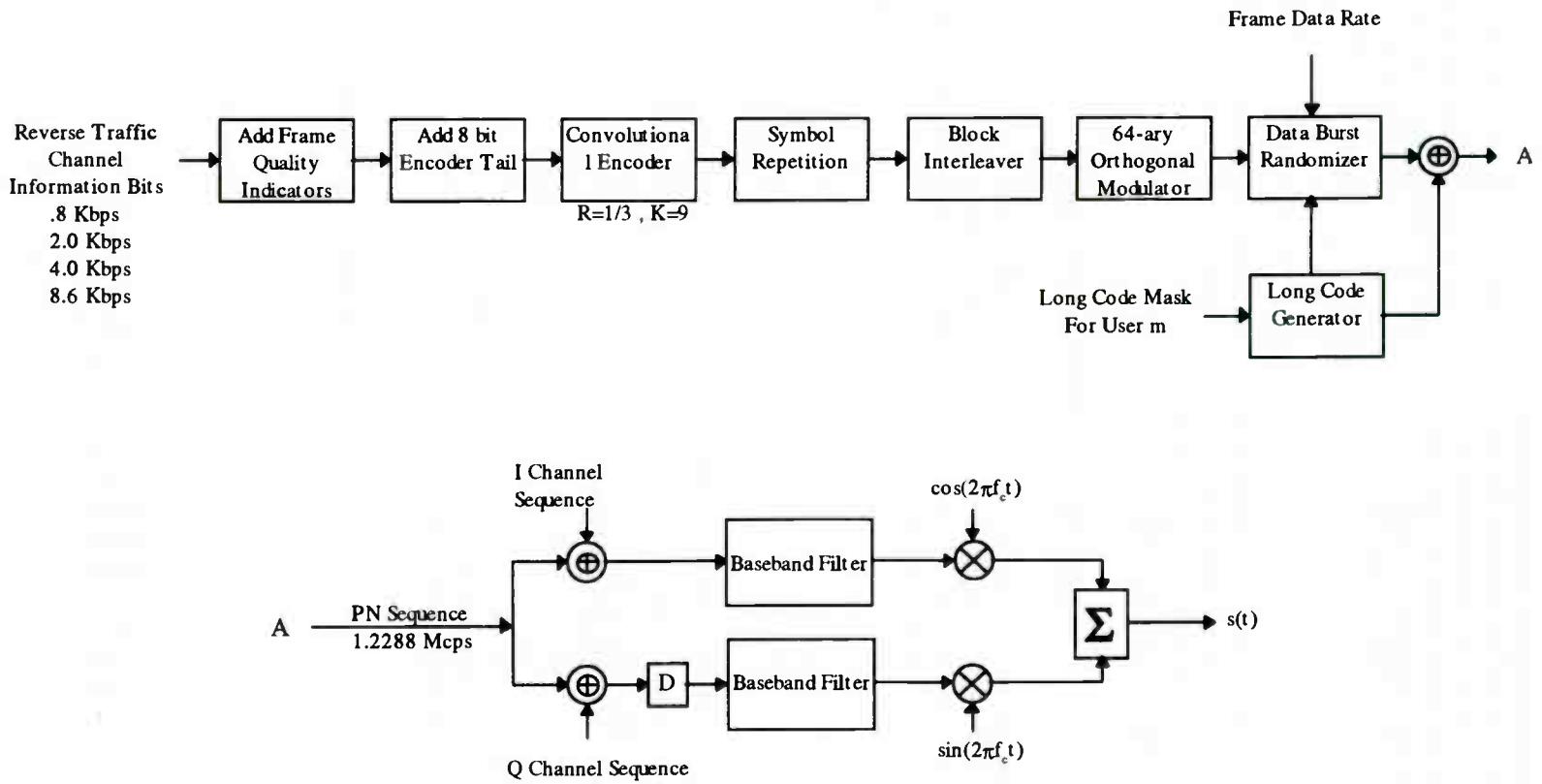

Fig. 3. Reverse CDMA Channel.

b) Graceful support of multirate processing

Typical modern CDMA systems employ spread-spectrum techniques in conjunction with sophisticated coding, interleaving and other signal processing techniques. Data production and consumption rates may vary widely among the various model blocks associated with a given design. Any effective simulation of such designs must efficiently accommodate these multiple rates.

c) Different levels of modelling abstraction

Even within a system-level tool, it is desirable to provide a hierarchy of levels of modelling abstraction. The user should be provided with just enough detail for appropriate modelling of the system function under study. A user designing a transmitter might not require extremely detailed models of the channel, for example.

d) Analysis models as an adjunct to simulation

In many cases, the use of analytical models for BER and other measures of performance can be used in conjunction with simulation results. Semi-analytic methods, combining some simulation with some analysis, can often be used to allow Monte-Carlo simulations to be performed in much shorter times.

The next section describes methods for implementation of the requirements described.

V. Techniques for Efficient Simulation

This section describes some techniques for implementing the types of efficient simulation required at the behavioral level for CDMA systems. The first section discusses procedures for efficient data processing and manipulation. We then move on to discuss techniques for modelling with different levels of abstraction within different portions of the system under study. Finally, we discuss the use of analytical methods as an adjunct to simulation.

1) An efficient data processing methodology

Within the complex systems involved in today's wireless field, many different types of subsystems exist in the end-to-end communication link. Some subsystems will always be analog, although more and more digital technology is being applied in current system designs. These various subsystems and their simulation models have widely differing data processing requirements. In the digital portions of the system, clock rates may differ by orders of magnitude between different chips, boards or components. Additionally, different portions of the system may need to process data in different size chunks, or blocks. Many modern DSP algorithms are based on block transforms such as FFT's and Walsh transforms. Models for these algorithms need to be mixed with models for such architectures as digital and analog feedback loops. These latter models are normally implemented with "sample-by-sample" processing. A dilemma arises when attempting to mix models with such varying data transfer requirements within standard simulation tools. Normally, the user has to do a significant amount of additional work in synchronizing the movement of data between the various model blocks participating in such complex simulations. Unless this data synchronization is performed in an efficient fashion, simulation run times can become excessive, rendering Monte-Carlo techniques almost useless. Any useful

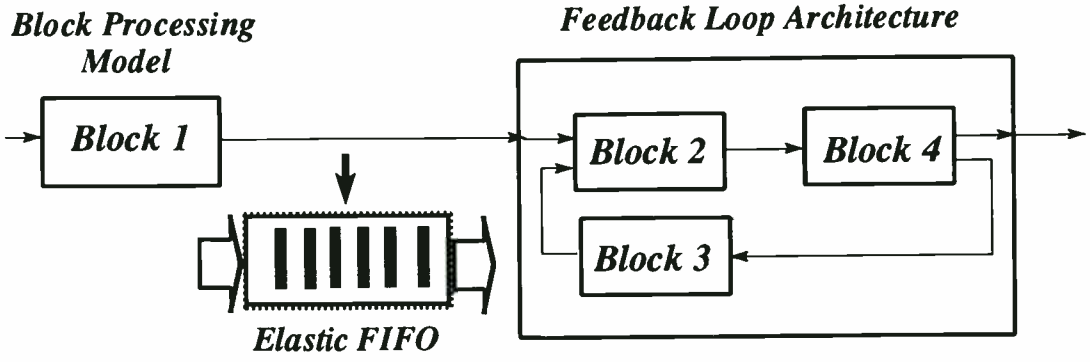

Fig. 4. Elastic FIFOs used to manage asynchronous data transfer.

simulation environment for the systems under consideration must employ efficient techniques for data movement and synchronization between model blocks.

One technique that can be used effectively for the support and synchronization of various types and rates of data transfer is elastic buffering. With this technique, elastic buffers are placed between the model blocks within a simulation to act as "storage tanks" for data that may be generated and consumed at differing local rates. This technique is illustrated in Fig. 4.

The diagram illustrates the case where a block processing model is connected to a feedback loop which is assumed to process data a sample at a time. The elastic buffer shown here is a First In First Out (FIFO) buffer that is responsible for holding a block of data that is produced by the block processing model and feeding it a sample at a time to the following feedback architecture. Obviously, the simulation executive program must have the logic built in to refrain from calling the block processing model again until the elastic buffer is empty.

2) Variable levels of model abstraction

System designers generally need to model different parts of a system at different levels of detail at different stages in the development process. In the concept definition stage of a communication system design, the designer would be interested in exploring modulation, coding and other system-level trade-offs to establish a single or small set of viable communication techniques. Since many possible combinations of basic algorithms will be studied, it's desirable to have efficient models that allow a large number of test cases to be evaluated. Generally, modelling at this stage in the development cycle can be rather abstract, since the designer is primarily interested in establishing performance trends and narrowing the set of possible design choices. This normally involves eliminating those choices that provide clearly inadequate performance. Thus the models employed within this scenario often need to provide only rough order of magnitude accuracy.

In addition to ideal demodulator performance, a receiver designer would need to explore the perfor-

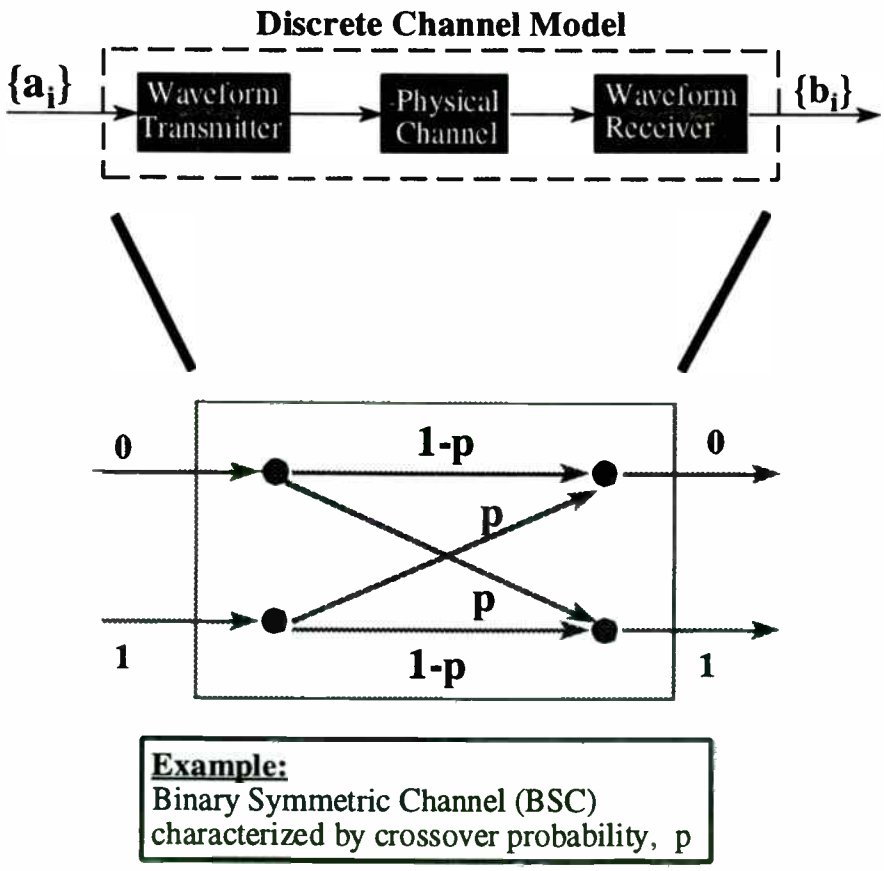

Fig. 5. Example of an Abstract Channel Model.

mance of various ancillary functions. These might include phase tracking, bit synchronization, equalization, or in the case of CDMA systems, various RAKE reception algorithms. An ideal modelling and simulation environment would provide alternative models at different levels of abstraction for the modelling of different portions of a systems at different stages in the design process.

A concrete example of the above consideration is the various levels of abstraction that might be provided for modelling the communication channel. *Abstract* channel models are often employed for efficient evaluation of coded system performance. An abstract channel model treats the transmitter/channel/receiver cascade as a discrete "superchannel" that receives M-ary input symbols and produces Q-ary output symbols with a given distribution, based on given "channel transition probabilities." This model is depicted in Fig. 5, for the case M = Q = 2.

This particular model assumes that independent symbols arrive at the decoder input with a given distribution. The distribution, in turn, may be evaluated through empirical studies made on the transmitter/channel/receiver cascade. In the IS-95-A application, for example, the Q-ary output might correspond to the quantized levels appearing at the input to the Viterbi decoder. In this case, the actual *physical* channel model would correspond to the type of fading multipath conditions encountered within the mobile cellular environment. A description of these types of channel models can be found in [5]. It is also possible and very useful to provide models intermediate between these two extremes. We illustrate this concept with a simulation example.

Fig. 6 illustrates a simulation of the IS-95-A noncoherent reverse link.

This simulation addresses only the demodulator performance in the presence of various types of fading. A Walsh modulator is employed on the transmit-

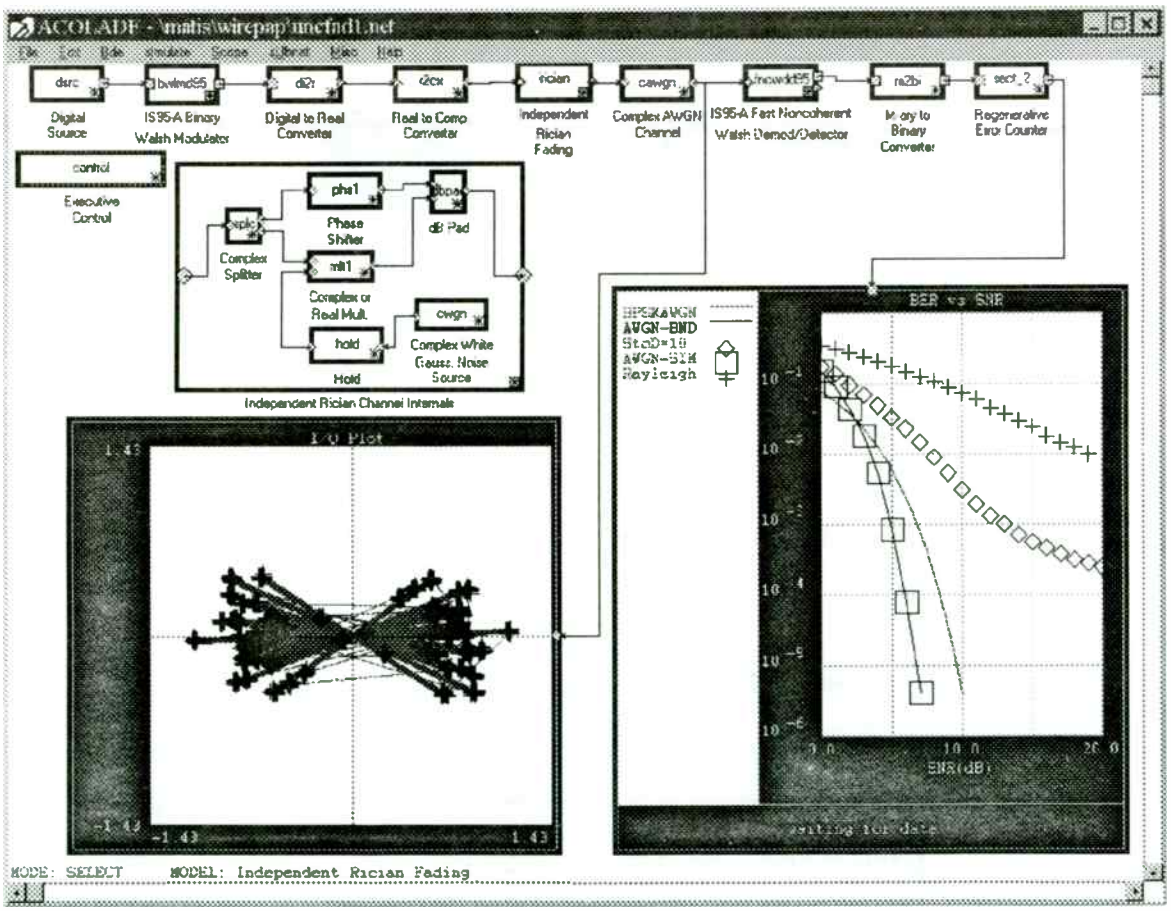

Fig. 6. Example of an Abstract Channel Model.

ting side, with a Walsh transform-based demodulator being employed at the receiving side. A single Rician path is assumed, with adjustable ratio of specular to diffuse energy. The internals of the **Independent Rician Fading** hierarchical model are shown on the bottom left of the canvas. It is an abstract channel model designed to simulate the effects of slow Rician fading in the limit as the fading bandwidth becomes a vanishingly small fraction of the symbol rate. This is the limiting case of "flat" fading, but is reasonably-well approximated when the fading bandwidth is on the order of $1/10^{th}$ the symbol rate. A **Complex Splitter** model splits the Subnet input into diffuse and specular components. This particular model generates a complex Gaussian variate with the **Complex Additive White Gaussian Noise** model and holds (replicates) it for a period of time before inputting it to a **Complex Multiplier**. A **Hold** model is employed for this purpose. A complex Gaussian variate with independent I and Q components results in Rayleigh-distributed magnitude and uniformly distributed phase. The resulting magnitude scaled and phase-shifted signal is applied to a **dB Pad** model where it is scaled and added to a scaled specular component. The specular component possesses a fixed, but user-specifiable phase. The scaling applied in the dB Pad model achieves a given user-specified specular-to-diffuse (S/D) energy ratio. The result of this process is that the signal undergoes Rician fading that is constant during intervals, but independent from interval to interval. This is extremely useful in the simulation of coded systems employing interleaving. If the "hold" period is chosen to be one symbol (or the number of symbols grouped together into an interleaving "cell"), the effects of an arbitrarily large interleaver can be simulated without actually having to use one. In simulating coded systems, this is an appropriate model for channels with a slow fading rate compared to the channel symbol time, but fast with respect to the total interleaving delay. We employ this model in this simulation, since the use of Walsh modulation can be viewed as a form of coding, in which Walsh "chips" play the role of encoded symbols. The overall simulation model in Fig. 6 assumes that the channel is constant over 64 chips, but independent from one 6-bit Walsh symbol to the next. This would correspond to the situation where an interleaving cell contains a number of Walsh symbols. After processing with the Independent Rician fading model, the signal is corrupted with AWGN with another complex AWGN model.

The Bit Error Rate (BER) as a function of bit energy-to-noise power ratio (Eb/N0), in decibels, is shown in the bit error rate plot on the right of the figure. The smooth curve corresponds to antipodal signalling in AWGN. The dashed curve corresponds to the theoretical BER performance for non-coherent reception of 64-ary orthogonal signals in AWGN. The open squares are the simulation results. In all cases, at least 100 bit errors were tabulated for each SNR value by setting the "Minimum Errors Requested" parameter in the error counter to that value. This provides extremely high statistical significance levels to our results. It will be noted that the empirical results fall exactly on the theoretical results for 64-ary modulation. Another interesting note is the fact that the 64-ary orthogonal modulation provides significant coding "gain" over the BPSK case, even with noncoherent detection. This is due to the fact that orthogonal sequence modulation can be properly considered a form of error-control coding. Using more than one transmission per bit allows the introduction of controlled redundancy into the transmitted chip stream. Alternatively viewed, this allows transmitted chip sequences (codewords) to be differentiated in a number of positions from one another, allowing the probability of *sequence* error to be greatly reduced. The BER curve for the coded orthogonal modulation shows the normal threshold behavior associated with coded systems in general. At low SNR, the performance is worse than uncoded, but exceeds it at higher SNR values. For further reference to the theory of data transmission by orthogonal functions, see [5]. The other curves on the figure show results for S/D ratios of 10.0 dB and -100.0 dB. The latter case represents essentially Rayleigh fading conditions. A plot of the noise-corrupted modulated phase trajectory over 2048 chips is shown in the bottom left of the figure. This plot was generated with S/D = 10 dB and Es/N0 = 20.0 dB. Note the dispersion about the signal antipodal mean values due to the skew and amplitude fading of the Rayleigh component.

VI. Conclusion

In this paper we have attempted to describe certain techniques for effective evaluation of CDMA systems and spread-spectrum systems in general. We hope that this discussion will be of value to those readers involved in the system development process or in the development of simulation tools and techniques.

References

[1] Viterbi, A. J., "CDMA-Principles of Spread-Spectrum Communication"; Addison-Wesley 1995.

[2] "Mobile-Station Compatibility Standard for Dual-Mode Wideband Spread Spectrum Cellular System" TIA/EIA/IS-95-A, May 1995.

[3] ACOLADE IS-95-A/CDMA Library Overview. ICUCOM Corporation, Troy, NY, 1996.

[4] Price, R. and Green, P. E., Jr. "A Communication Technique for Multipath Channels" Proc. IRE **46**, (1958) 555-570.

[5] ACOLADE IS-95-A/CDMA Library Manual. ICUCOM Corporation, Troy, NY, 1996.

Design and Simulation of a 100MHz $F_s/4$ QPSK Digital Communication System

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Abstract - **With the increasing advancement in Digital Signal Processing (DSP) hardware, it has become advantageous to implement DSP algorithms in order to process normally analog signals digitally. Using DSP techniques eliminates errors due to thermal drift, increases overall processing speed, and reduces circuit complexity. The challenge to the DSP designer is to develop fast and accurate algorithms.**

Traditionally Quadrature Phase Shift Keying (QPSK) modulation and demodulation are accomplished by using a combination of DACs, ADCs and analog mixers on both the in-phase and quadrature-phase channels. This paper will demonstrate the design and simulation of a 100 mega symbol per second DSP hardware QPSK communication system utilizing a technique that eliminates the complexity associated with generating trigonometric functions. Specifically, by setting the carrier's center frequency equal to ¼ the sampling rate (F_S), the QPSK hardware implementation is significantly simplified, and the benefits of using DSP chips can be realized.

I. DESIGN

The article will take the reader through the design process and simulation of a $F_s/4$ DSP QPSK system using SystemView®, a windows based simulation tool available from Elanix, Inc.

Traditional analog designs for QPSK systems (Figure 1) rely on analog circuitry to modulate a sinusoid with data.

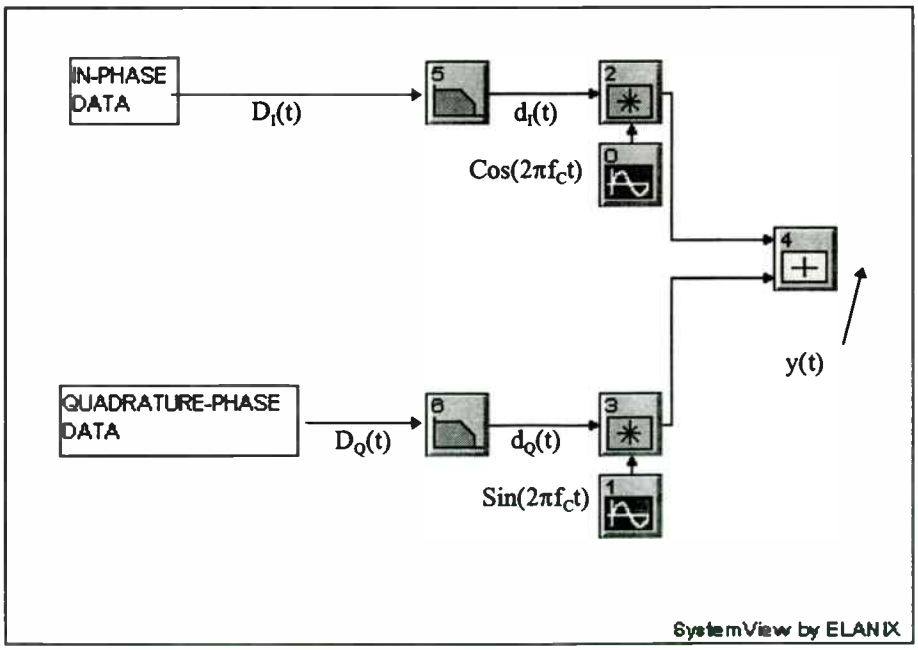

Figure 1. Analog QPSK modulator

By inspection of the QPSK transmitter in Figure 1 the output signal is

$$y(t) = d_I(t)\cos(2\pi f_c t) + d_Q(t)\sin(2\pi f_c t). \qquad [1]$$

If the components in Figure 1 were now replaced with their digital equivalents then [1] would take on the form

$$y(nT) = d_I(nT)\cos(\Omega_c nT) + d_Q(nT)\sin(\Omega_c nT) \qquad [2]$$

where $1/T = F_S$ is the sampling rate, and $\Omega_c = 2\pi f_c$, the center frequency. The values $d_I(nT)$ and $d_Q(nT)$ are the results of convolving the in-phase ($D_I(nT)$) and quadrature ($D_Q(nT)$) data with the impulse response of the pulse shaping digital FIR filters. Digitally modulating signals with sinusoids as in equation [2] becomes difficult.

However, if f_c is set to ¼ F_S (i.e. $\Omega_c T = \pi/2$) then equation [2] can be rewritten as

$$y(nT) = d_I(nT)\cos(n\pi/2) + d_Q(nT)\sin(n\pi/2). \qquad [3]$$

The output y(nT) will be $d_I(0)$, $d_Q(T)$, $-d_I(2T)$, $-d_Q(3T)$, $d_I(4T)$, $d_Q(5T)$,... since $\cos(\Omega_c nT) = 1,0,-1,0$ and $\sin(\Omega_c nT) = 0,1,0,-1$. The $F_s/4$ technique reduces the carrier modulation effort to multiplying the data by "1" and "-1". Hence, the speed and precision in which the data is modulated is increased. There is no need for high speed digital multipliers and adders to implement the modulation.

Now lets take a closer look at the terms d_I and d_Q. The general expression for d_I is given by the convolution relation,

$$d_I(n) = \sum_{m=0}^{N} h(m) D_I(n-m) \qquad [4]$$

where h(m) are the coefficients of the pulse shaping filter. Now write out equation [4] in detail to obtain;

$d_I(0) = h(0)D_I(0)$
$d_I(1) = h(0)\,D_I(1) + h(1)\,D_I(0)$
$d_I(2) = h(0)\,D_I(2) + h(1)\,D_I(1) + h(2)\,D_I(0)$
$d_I(3) = h(0)\,D_I(3) + h(1)\,D_I(2) + h(2)\,D_I(1) + h(3)\,D_I(0)$
$d_I(4) = h(0)\,D_I(4) + h(1)\,D_I(3) + h(2)\,D_I(2) + h(3)\,D_I(1)$
$d_I(5) = h(0)\,D_I(5) + h(1)\,D_I(4) + h(2)\,D_I(3) + h(3)\,D_I(2)$

Table 1

For illustration purposes N was set to equal three in equation [4]. The proper way to drive the pulse shaping filters is with impulses at the symbol data rate. For example, if the symbol rate is also Fs/4, then the input data samples into the filter are of the form; $S_I(0),0,0,0$, $S_I(1),0,0,0$, $S_I(2),0,0,0$, $S_I(3)$ etc., where $S_I(0) = D_I(0)$, $S_I(1) = D_I(4)$, $S_I(2) = D_I(8)$, etc. Thus the filter output of Table 1 can be rewritten as;

$d_I(0) = S_I(0)h(0)$
$d_I(1) = S_I(0)h(1)$
$d_I(2) = S_I(0)h(2)$
$d_I(3) = S_I(0)h(3)$
$d_I(4) = S_I(1)h(0) + S_I(0)h(4)$
$d_I(5) = S_I(1)h(1) + S_I(0)h(5)$
etc.

Table 2

Since $\cos(n\pi/2)$ is zero for odd values of n, only the even terms of the above expression need to be computed. And, hence, only the even terms of h(n) are retained. In the same manner, the equivalent expression for the quadrature signal only involves the odd coefficients of h(n). As a result, the single pulse shaping filter can be split into two filters one with even coefficients and one with odd coefficients, each running at half of the original rate. In addition, the process of multiplying the data points by alternating "1" and "-1", as previously discussed, can be eliminated by negating every other filter coefficient. Thus, a further reduction in computational complexity is realized.

The DSP $F_s/4$ QPSK transmitter implementation that was simulated is shown in Figure 2. The data rate on the in-phase and quadrature channels is 100MHz, and the computational rate is then 400 MHz. The basic building blocks are referred to as tokens in SytemView®.

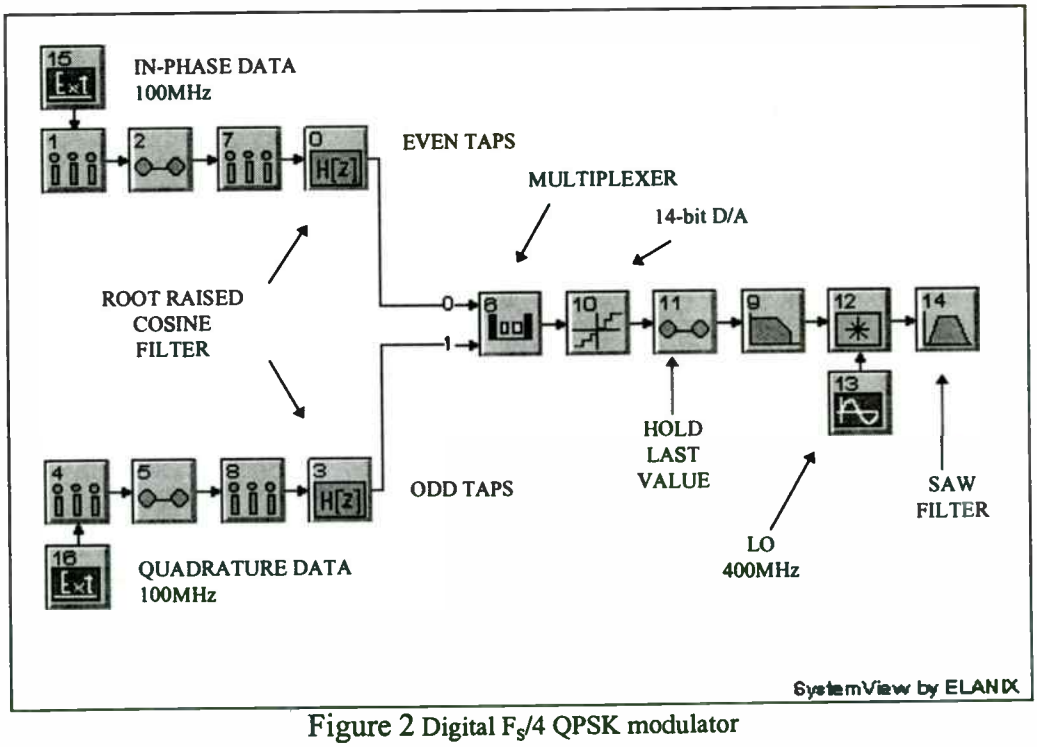

Figure 2 Digital $F_s/4$ QPSK modulator

The first step in constructing the transmitted signal is achieved by sampling the input signal at 100MHz (token 1 and token 4) such that there is one bit per symbol. The output of the 100MHz sampler is then fed into a Hold Last Value token and then sampled at 200MHz. Figure 3 depicts the in-phase 100MHz sampled data overlaid with

the resulting output of the 200MHz sampler. The series of impulses representing the original data is then processed by a root raised cosine filter. The root raised cosine filters (token 0 and token 3) both have a roll off factor of 0.3. This pulse shaping filter was chosen because of its intersymbol interference (ISI) properties.

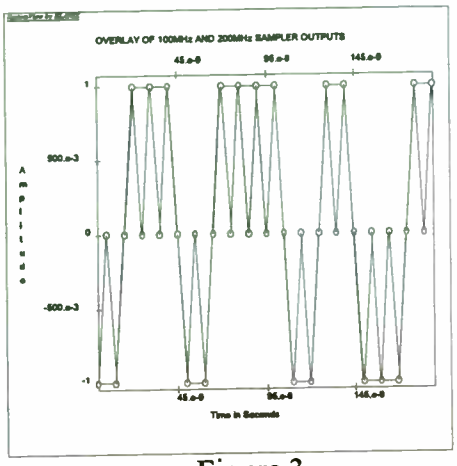

Figure 3
Overlay of 100MHz and 200MHz sampler outputs

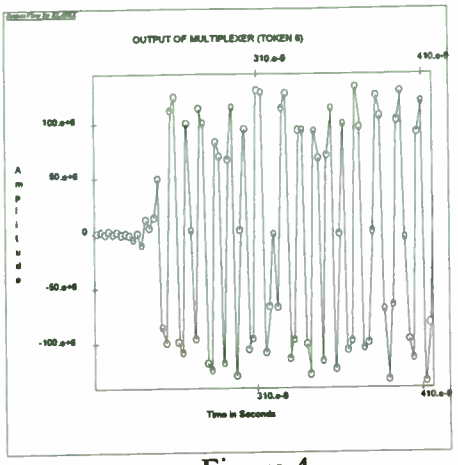

Figure 4
Output of multiplexer (token 6)

The outputs of the root raised cosine filters on the in-phase channel and quadrature channel are multiplexed together by token 6. The resulting waveform is a digital representation of y(nT) defined in equation [2]. The output of token 6 is shown in Figure 4, where spacing between samples is 2.5ns. The output signal's power spectrum is shown in Figure 5 and its center frequency is 100MHz..

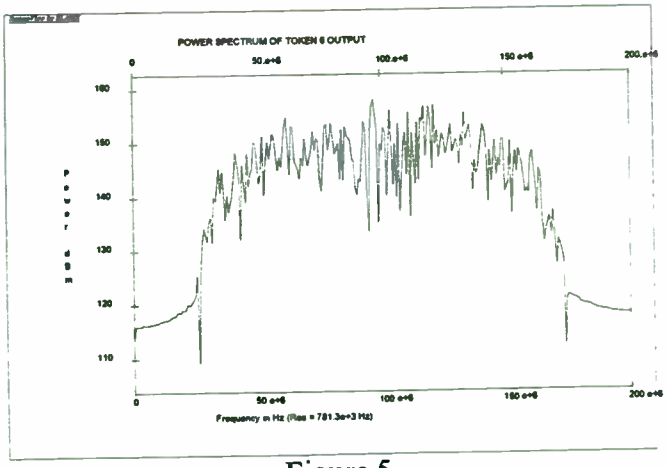

Figure 5
Power spectrum of Token 6 output

After the signal has been digitized it is then converted it to an analog signal using a 14 bit quantizer (token 10) in conjunction with a sample and hold (token 11). The output of token 11 is then passed through a 200MHz low pass filter (token 9). Finally, the signal is mixed with a 400MHz local oscillator and passed through a Surface Acoustic Wave (SAW) band pass filter with cut off frequencies at 400MHz and 600MHz.

The receiver portion of this QPSK system is shown in Figure 6. The first step in processing the received signal is to directly sample the incoming signal at 400MHz, effectively spectrally shifting the transmitted center frequency from 500MHz to 100MHz. The signal is then demultiplexed into odd and even samples. Demultiplexing the signal is achieved by decimating the 400MHz signal by 2 to extract even samples. Odd samples are extracted by delaying the signal by one sample and then decimating it by 2.

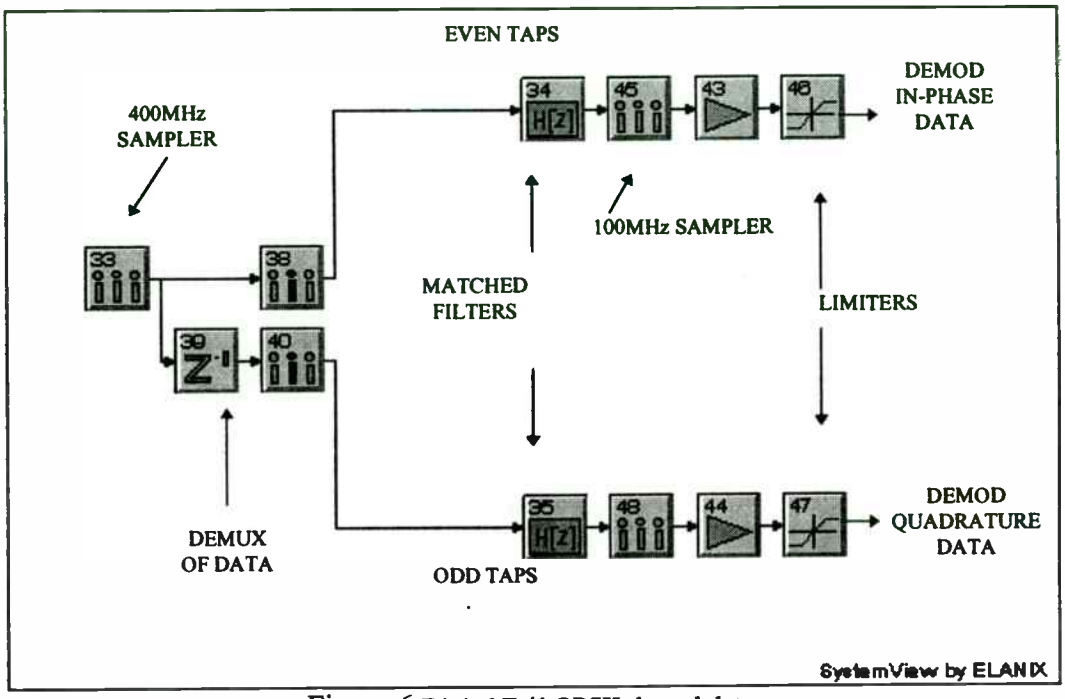

Figure 6 Digital $F_S/4$ QPSK demodulator

The output of the samplers (tokens 38 and 40), the in-phase and quadrature channels, are then processed by matched root raised cosine filters. Again even coefficients are used to process in-phase data samples and odd coefficients are used to process quadrature samples. The outputs of the matched filters are then sampled at 100MHz.

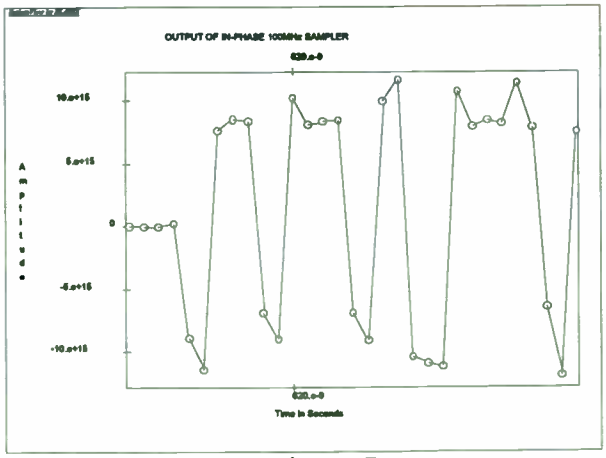

Figure 7
Output of in-phase 100MHz sampler

Figure 7 is the output of the in-phase channel's matched filter after it had been sampled (token 45) at 100MHz. Note that each sample is separated by 10ns. The output of the limiter (token 59) is shown in Figure 8. Figure 9 shows the original in-phase data.

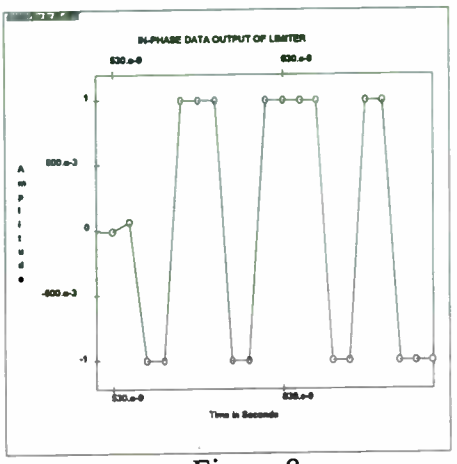

Figure 8
In-phase data output of limiter

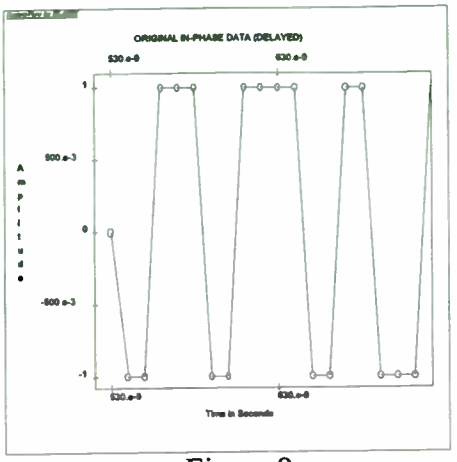

Figure 9
Original in-phase data (delayed)

II. CONCLUSION

The digital implementation of a 100 mega symbol per second QPSK modulator and demodulator using a $F_s/4$ process has been designed and simulated using SytemView® by ELANIX. SytemView® is a PC-based design and simulation environment used for advanced Communications and DSP development worldwide. Information and demonstration software is available from ELANIX, Inc. at (818) 597-1414, www.elanix.com.

Analysis of the mathematics involved in this process lead to the realization that a significant portion of the signal processing can be implemented by using a DSP chip. Hence, the reliance on the anticipated accuracy of analog components has been virtually eliminated. Furthermore, the needed hardware to build a modulator and demodulator has been minimized by using this method.

III. REFERENCE

[1] Samueli, Henry and Wong, Bennett, "A VLSI Architecture for a High-Speed All-Digital Quadrature Modulator and Demodulator for Digital Radio Applications," IEEE Journal on Selected Areas in Communications, Vol 8. No 8. October 1990.

System Simulation Improves CDMA Product Design

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Abstract

Code Division Multiple Access (CDMA) is increasingly challenging other modulation techniques for dominance in the personal communications services (PCS) and other mobile communications systems. First generation mobile stations that are compatible with the IS-95 standard and use the Qualcomm chip set are currently in production. Improving the current performance while meeting cost and time-to-market goals is a daunting task that will occupy wireless engineers well into the next century. Engineers will best be able to meet this challenge through the use of system simulation. Accurate system simulation allows for more advanced design at the analog circuit level, RF subsystem level, and DSP baseband level. This paper focuses on applying standard simulation models and RF models to CDMA system design.

I. Introduction

Detailed simulation studies, which can improve the performance of CDMA transceivers, can be achieved without sacrificing time to market goals. Instead of spending valuable engineering resources creating models in C code or mathematical software packages, designers can turn to existing wireless simulation tools such as the E4604A OmniSys communications simulator from HP EEsof (Westlake Village, CA). For example, in OmniSys there are several communication models that are useful for modeling CDMA receivers and transmitters that are based on the IS-95 standard. The CDMA system simulation models include a programmable Walsh code generator, a full rate interleaver, a convolutional encoder, a Viterbi decoder model, forward- and reverse-link modulators, RF transceiver models, delay-locked loop tracking circuitry, IS-95-compliant propagation models, error vector magnitude (EVM) measurements, and waveform quality measurements. Simulations using these models will be shown herein. As an example, the modulated forward spectrum will be propagated through a Rayleigh faded channel and sent through an extended Rake receiver, where bit error rate (BER) performance can be verified.

II. Top-level simulation

The system simulations shown in this paper are based on the IS-95 CDMA specification and can be depicted at the top level as shown in Figure 1. The functionality of the baseband section is to perform DSP convolutional encoding, interleaving, Walsh code spreading, and in-phase and quadrature short code spreading. Next, the mixer and oscillator perform an analog up-conversion and the amplifier block

represents the high-frequency components such as the power amplifier, transmit/receive switch, and power control functions. After power amplification, the transmitted spectrum travels through the RF propagation environment and is then down-converted and demodulated by the receiver. The I and Q baseband waveforms are then de-spread using the locally generated PN code and the locally generated Walsh code. Acquisition circuitry generates the correct timing. The resulting data is then de-interleaved, and finally decoded using the Viterbi decoder model (Figure 2).

One of the key advantages of this type of system simulation is the ability to accurately model the finite numeric effects of the digital signal processing (DSP) components, the transient and steady-state effects of the analog components, and the VSWR and frequency-domain distortion of the RF components. To accurately model all these effects with custom in-house simulation tools is, to say the least, challenging. This challenge is further complicated by the requirement that the system must be simulated in a radio frequency environment with delay, Doppler, and attenuation at the transmitted frequency.

III. System modeling details

In this section, the details of the sub-blocks that make up the standardized system are described.

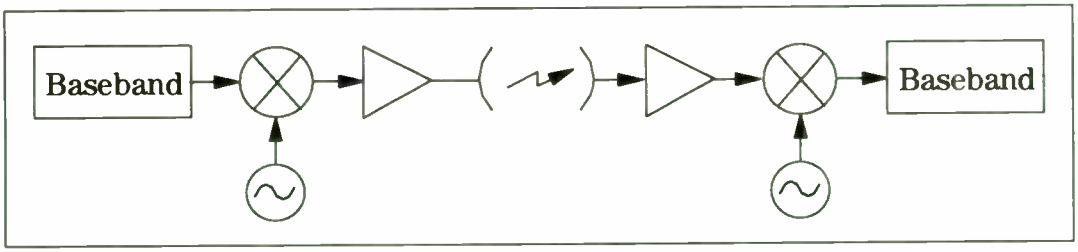

Figure 1. CDMA system block diagram.

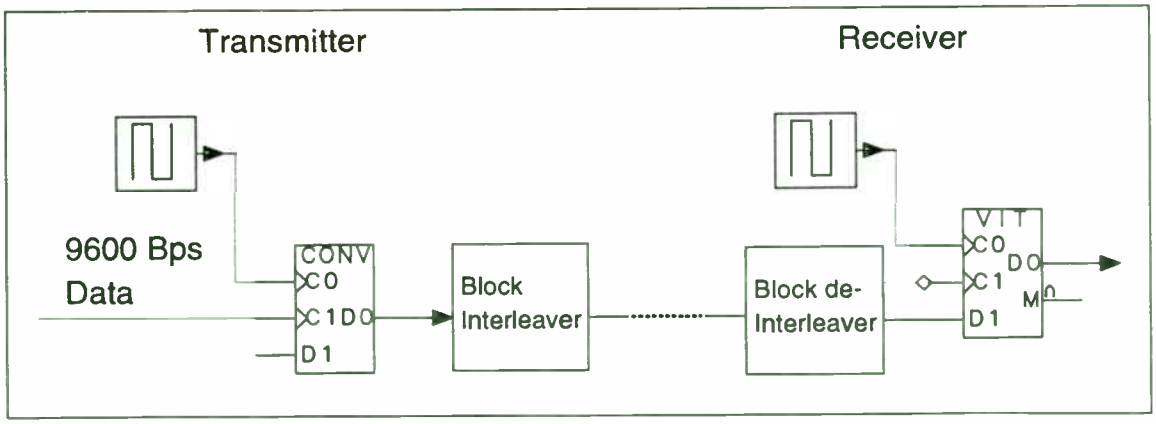

Figure 2. Coding and Decoding.

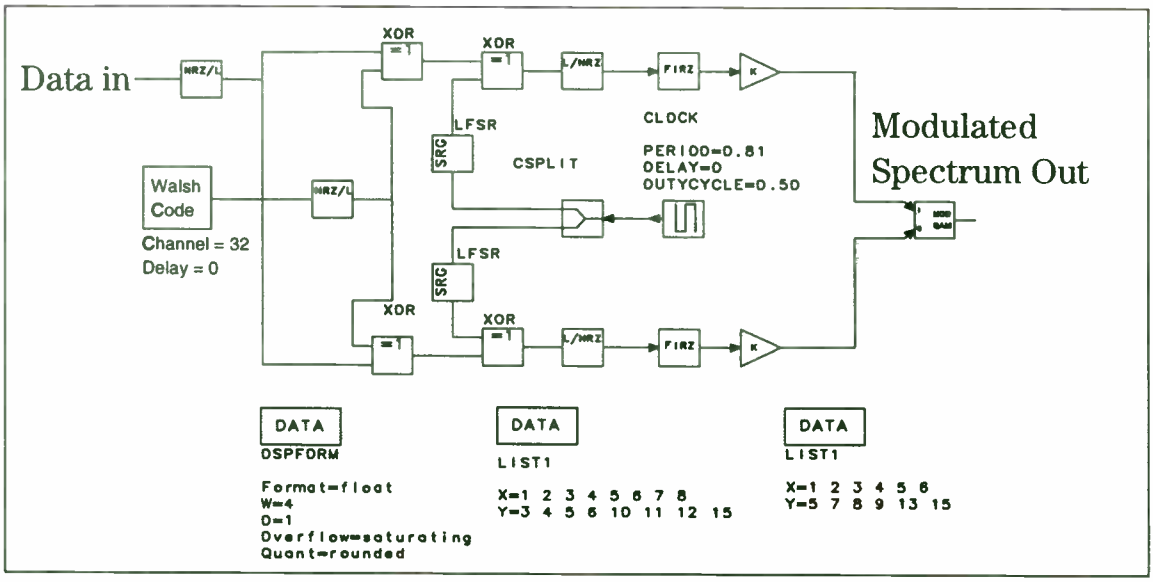

Figure 3. CDMA modulator block diagram.

The next block is the I/Q modulator and is shown in Figure 3.

The data enters from the left and is first spread by the Walsh code, which is currently set to channel 32 (synch channel). The Walsh coded signal is then spread by the I and Q short PN codes which are set by the linear feedback shift registers (LFSR). After this baseband signal is filtered using the IS-95 specified finite impulse response (FIR) tap coefficients, it is modulated to 83 MHz using the QPSK modulator. If the reverse channel modulator were being used, a delay equal to 1/2 the chipping rate would be inserted in the Q channel, thereby creating OQPSK. Notice that the designer has complete control over the finite numeric effects of each of the digital blocks in the modulator. These effects include format (fixed or floating point), overflow (saturation, etc.), and quantization (rounded or truncated) of the numeric signals. Refer to Figure 4 for the constellation diagram of the QPSK and OQPSK signals for the forward and reverse channels.

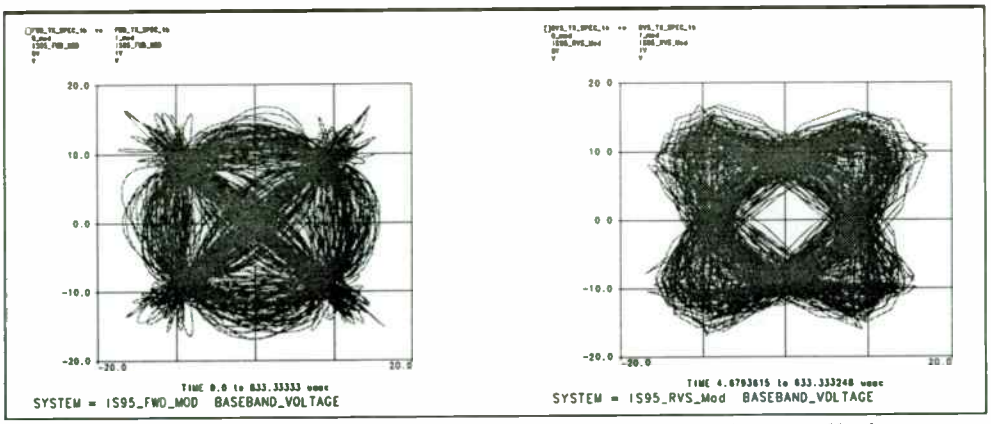

Figure 4. Forward and reverse channel constellations.

The inter-symbol interference (ISI) or, more precisely, inter-chip interference (ICI) present on these signals arises solely from the FIR filters, but will be further distorted after the analog RF transmitter section.

Using the many analog high-frequency system models available in OmniSys, an engineer can quickly construct a schematic representing the proposed design. A typical RF receiver model is shown in Figure 5, and includes amplifiers, a mixer, an oscillator, and RF and IF filters, as well as a microstrip transmission line model. The usefulness of this model comes from its being able to accurately include high-frequency effects such as input and output VSWR, phase noise, amplifier and mixer nonlinearities, and group delay. For example, designers can study the effects of an amplifier's AM-AM and AM-PM distortion on the CDMA spectrum. In fact, the nonlinear model used in the simulation can be derived from either laboratory measurement or an RF circuit simulation. The approach used to model amplifiers in OmniSys works well for Class A and Class AB amplifiers and allows for accurate predictions of critical parameters, such as adjacent power channel ratio (ACPR) or EVM. A simulation that includes the performance of RF components allows designers the flexibility to tune or vary the parameters of any component in the design. Also of interest is the simulator's ability to automatically optimize performance of critical system-level performance measures such as BER. The effects of system architecture changes can also be readily evaluated.

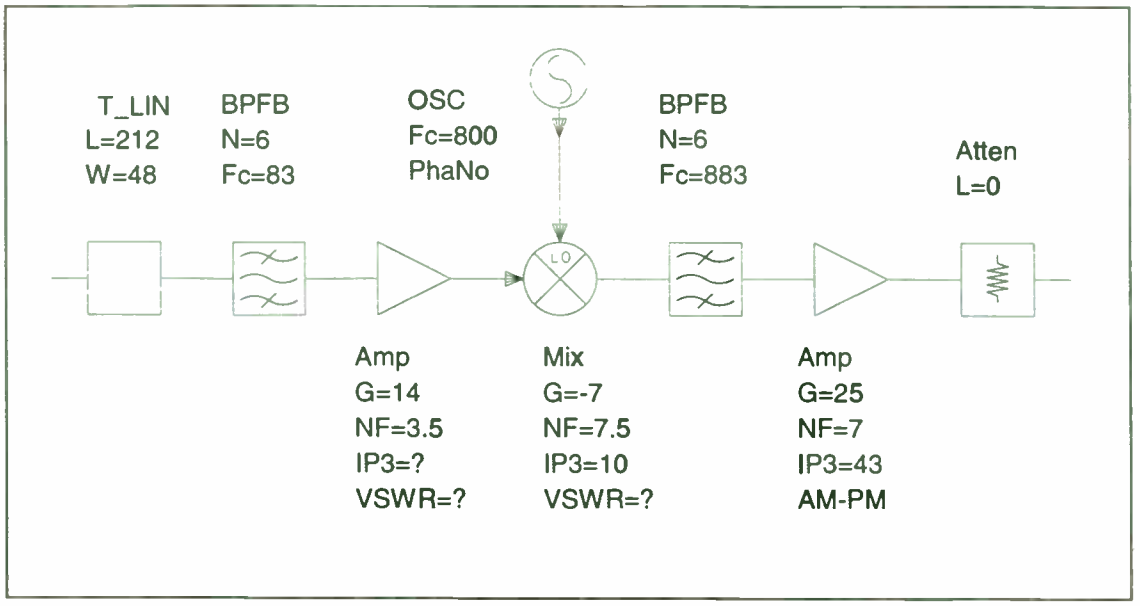

Figure 5. Analog/RF transmitter section.

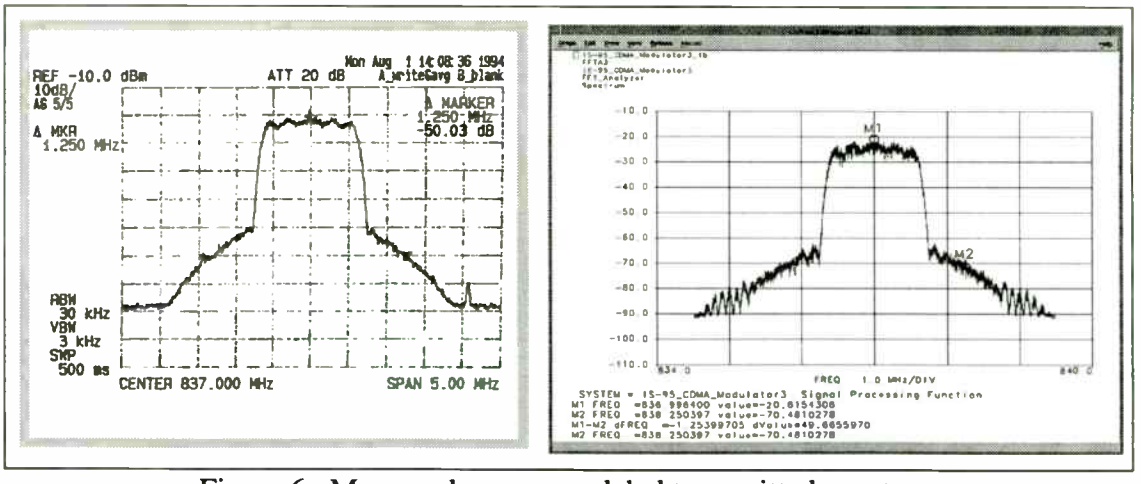

Figure 6. Measured versus modeled transmitted spectrums.

Figure 6 shows plots of transmitted spectrum predicted by OmniSys and actual hardware measured by a CDMA vendor. As can be seen from the plots of each spectrum, the adjacent channel power is down -35 dB in the measured spectrum, which correlates closely with the -35.5 dB down of the simulated system. The EVM of the transmitted signal can be measured as can pilot channel waveform quality (ρ). For example, the forward link constellation, (shown on the left side of Figure 4) has a measured EVM of % 16.5 rms. The relationship between EVM and ρ can be shown to be:

$$\mathbf{EVM} \sim \sqrt{\frac{1}{\rho} - 1} \qquad (1)$$

This relationship is approximate, but is useful in evaluating the relative effects

of the various RF components comprising the transmitter. A Rho (ρ) measurement will be available in OmniSys in early 1997.

The next stage in the system simulation is to send the spectrum in Figure 6 through a propagation channel model. This model accepts information on location, elevation, vehicle speed and direction. These elements are based on statistical models that simulate multipath effects by incorporating multi-tap delay networks and Rayleigh and Rician probability distribution functions. For this case, ignoring Doppler effects, the delay profile can be represented by:

$$P(\tau) = \sum_{n=1}^{3} \sigma_n^2 \delta(\tau - \tau_n) \qquad (2)$$

and the transmission path loss for a typical urban environment is based on Hata's model, which is shown in Equation 3.

For this simulation, the channel model is set for a 3-path Rayleigh fade per the IS-97 specification. Figure 7 shows the noisy, distorted signal at the input of the receiver.

On reception, the distorted spectrum is down-converted to a suitable IF using a receiver that has been modeled in a manner similar to how the transmitter was modeled. The IF is then demodulated using a QPSK demodulator. The de-spreading occurs when the local PN sequence is in phase with the received PN sequence. The acquisition of the proper PN code phase is achieved using either a matched filter correlator (parallel acquisition) or a sliding block correlator (serial acquisition). After acquisition, a code tracking circuit is used to maintain the proper code phase. In this simulation, we will include a 3-channel Rake receiver to overcome the effects of the 3-path Rayleigh faded signal. The principle behind a Rake receiver is the coherent summation of all the multipath's paths.

$$L_{TU} = 69.55 + 26.16 \log_{10} fc - 13.82 \log_{10} H_{bs} + (44.9 - 6.55 \log_{10} H_{bs}) \log_{10} R \qquad (3)$$

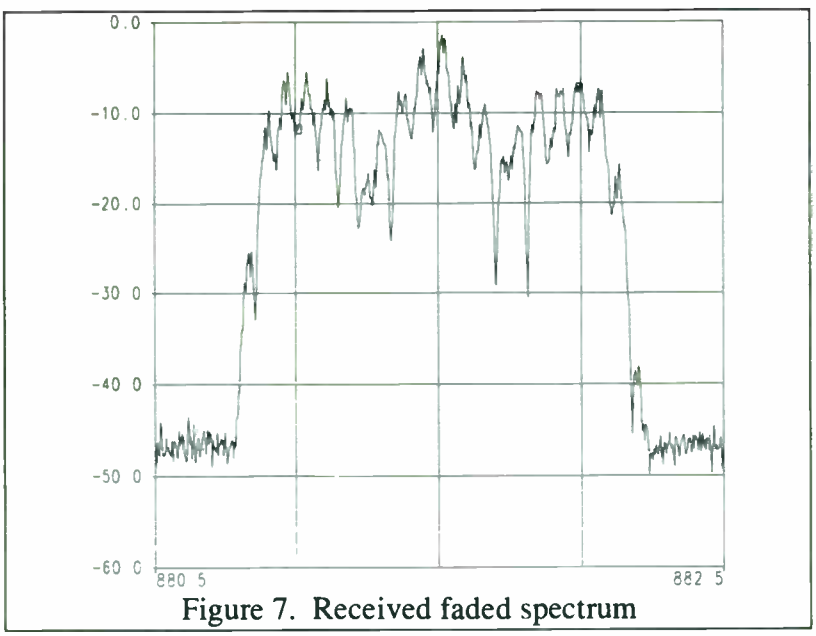

Figure 7. Received faded spectrum

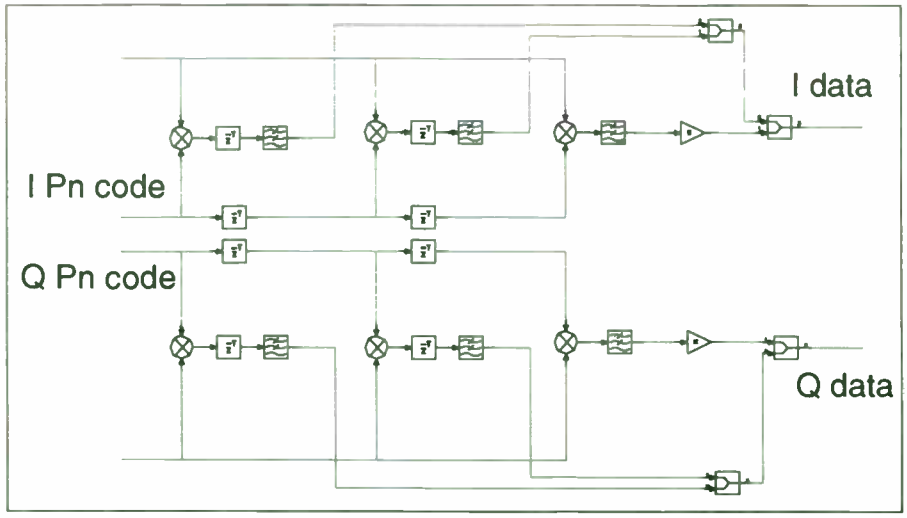

Figure 8. 3-arm Rake receiver.

At the receiver, the signal is a composite of several versions of the transmitted signal, each of which has a different delay and amplitude. The Rake receiver uses a tapped delay line to create delayed versions of the PN sequence corresponding to the different delays experienced by the transmitted signal . These delayed versions are multiplied with the composite spread spectrum signal, then filtered (averaged) and added together coherently in time as shown in Figure 8.

Figure 8 shows a 3-arm Rake which can be used to recover the signal after fading from the IS-97-compliant 3-path fading model. In this simplified example, the inputs to the Rake system are the I and Q baseband signals from the demodulator and the local I and Q PN sequences. Since there are three paths in the propagation model (excess delays of 2us and 14 us) three versions of the PN code with three different delays are used to de-spread to the received composite signal. The results are shown in Figure 9.

As can be seen in Figure 9, after an initial delay while the delay locked loop locks up to track the PN codes, the data is correctly recovered. At this point, the benchmark system simulation is operating correctly per specification and is now ready for the various design groups to use for detailed analog, DSP, and high-frequency RF designs.

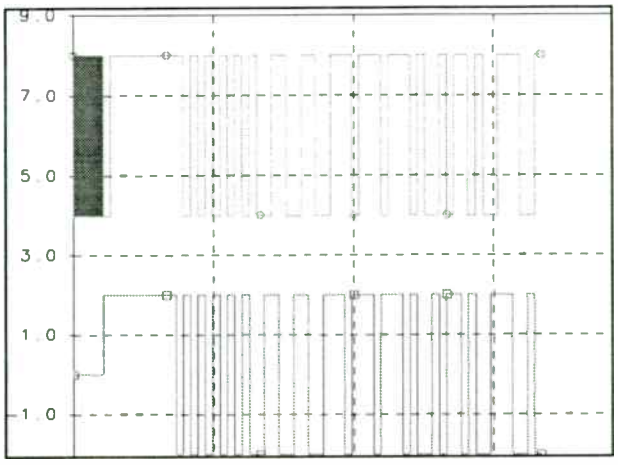

Figure 9. Rake receiver transmitted and recovered data.

IV. Optimization example

Another useful feature of the simulator is the ability to apply optimization techniques toward communication problems. For example, we noted that the transmit filter generates ICI. We also expect the filters and amplifiers present in the RF section to increase the ICI. At the receiver, a baseband filter that is complementary to the transmit filter is typically employed. If a matched filter (optimizes SNR) is used, the inter-chip interference is not removed completely. An alternate approach is to design an FIR filter that, when cascaded with the transmit filter, removes or at least minimizes the ICI. The design of this filter can be facilitated using the performance optimizer in OmniSys. Figure 10 shows a cascade of the IS-95 48 tap FIR filter and a 44 tap FIR receive filter. The optimization goal is to force the impulse response of the cascade to be zero at multiples of the chip duration (Tc), thereby ensuring zero ICI.

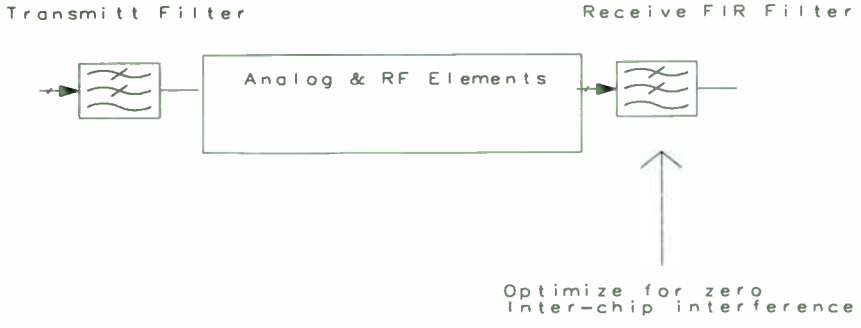

Figure 10. Cascade of transmit pulse shaping filter and receive filter.

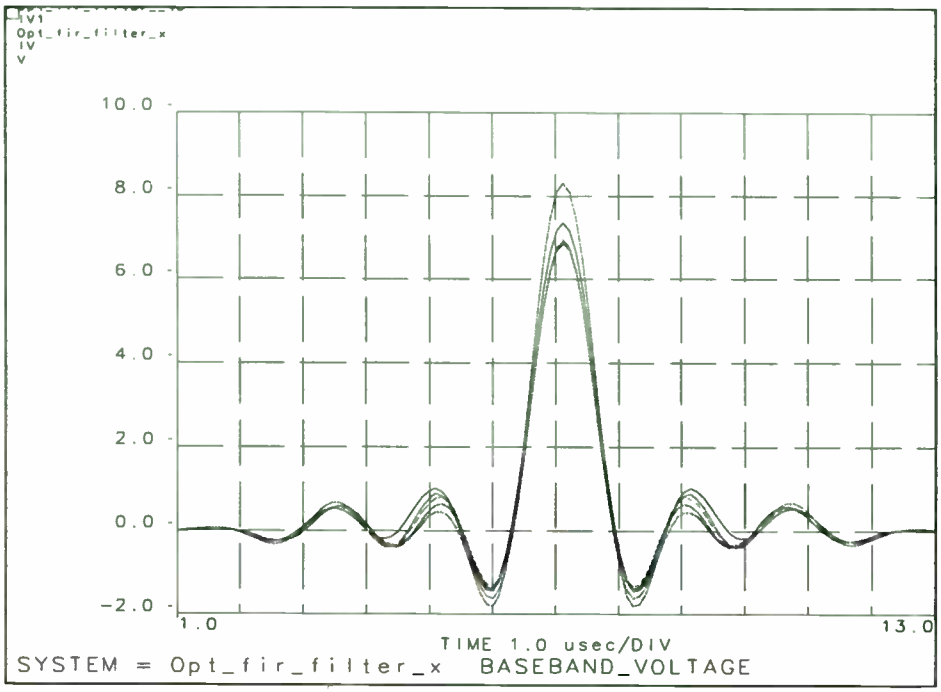

Figure 11. Optimized impulse response of transmit and receive filter cascade.

Figure 11 shows the results. As an initial guess for the receive filter, we can use the center 44 tap coefficients of the transmit filter. The optimizer searches through the design space for a set of tap coefficients that meet the zero crossing criterion for the cascade. This approach is very similar to the approach used in adaptive equalizers (i.e., zero forcing the received waveform at adjacent sampling instances). In general, removing ICI in this manner slightly decreases the SNR, which in turn increases the BER. However, if the ICI generated by the RF filters increase ICI, then trading off SNR for a reduction in ICI may actually improve the BER. This can quickly be verified using the simulator. In a similar manner, the filter optimization can also partially compensate for the effects of the SAW subscriber filter found in the receiver.

Conclusion

A CDMA system simulation was assembled using the HP E4604A OmniSys Design Suite. This CDMA system simulation included a programmable Walsh code generator, a forward- and reverse-link modulator, an RF transceiver, a delay locked loop, and a matched filter. This system was made more realistic by the addition of a propagation model, a mobile antenna, the base station antenna, and quantization effects in the DSP functions. After RF reception, the system utilized a delay-locked loop and a 3-tap Rake receiver to demodulate the transmitted data. The benefit of using

such a system is to allow designers to focus on their analog, DSP, or RF detailed designs and verify these designs in the targeted IS-95 system before prototyping begins.

I/Q Modulators for Interference Cancellation in Wireless Communication

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Abstract

Dual axis I/Q devices are an integral part of many communication systems. Modern designs increasingly demand that these products provide a higher precision, a wider dynamic range and greater RF bandwidth. This paper describes a technique using the basic I/Q modulator for extending the control of the I and Q axis signal components over a dynamic range of more than 60 dB, with minimum amplitude and phase error. Analysis and measured data are presented.

Introduction

The modulator is a key component in complex, high performance communication systems. The accuracy of the transmitted signal is a direct function of the amplitude and phase distortion of the modulator. Many modern modulation schemes in wireless communication involve the dual axis I/Q modulation process, (e.g. QAM type modulation). In receiver applications, I/Q modulators are used to cancel coherent and non-coherent interference. Examples of this are found in linear equalizers, pulse shaping networks, echo cancellation schemes, and antenna reflection nulling in monostatic systems. In these and similar application, broad RF bandwidth and wide dynamic range are required.

In the following sections, a basic I/Q modulator will be described and its limitation characterized by a simple error model. This model will provide a tool to explain a method of extending the dynamic range of the I and Q axis. An error analysis and measured data are presented.

Basic I/Q Modulator

The basic element of a dual axis I/Q modulator, shown in Fig. 1, is a pair of variable attenuating devices, combined in a quadrature arrangement and independently controlled by separate I and Q commands. By defining the character of the output vector Z in the Cartesian notation, $Z=M(I)+jM(Q)$, it is evident that the output of each attenuator, M(I) and M(Q), must be monotonic along the axis of modulation. Ideally the output should be without any amplitude and phase distortion. In Fig. 1, these attenuators are designated as an in phase path and a quadrature path bi-phase modulators, respectively.

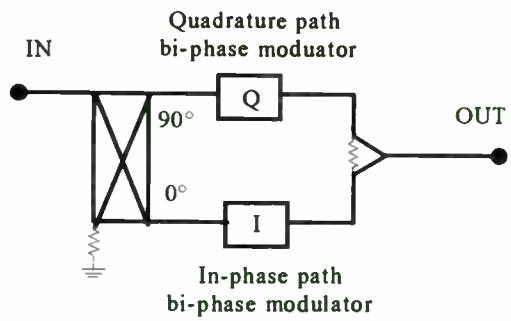

Figure 1: Basic I/Q Modulator

As shown in Fig. 2, the bi-phase modulator is a double balanced arrangement of a pair of attenuators connected by means of input and output quadrature couplers.

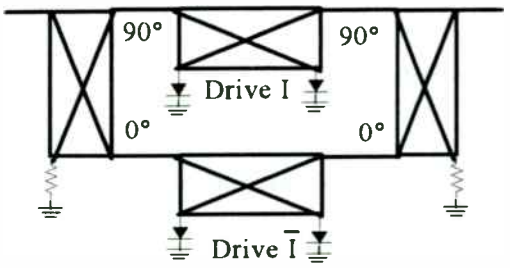

Figure 2: Bi-phase Modulator

Each attenuator, also referred to in the literature as a 90° single balanced modulator (SBM), consists of a 3dB quadrature coupler and a pair of PIN diodes terminating the two mutually isolated ports. For the purposes of the subsequent analysis it is sufficient to characterize the response of each SBM to be proportional to $\Gamma+\delta$ and $\bar{\Gamma}+\delta$, where Γ and $\bar{\Gamma}$ are the reflection coefficients of the diodes biased by complimentary drives, I and $\bar{I}$, respectively. The complex coefficient δ is related to the inherent directivity of the 3dB coupler.

A voltage or current biased PIN diode is a preferred device used to control the attenuation of RF signals since it offers relatively fast response time, high dynamic range and low attenuation sensitivity to the incident RF power. However, at the microwave frequencies, the basic limitation in dynamic range of the SBM due to reactance associated with the diodes and other circuit parasitic elements. The consequence ot the parasitics is an attenuation range limited to 20 dB typically and as low as 15 dB over any significantly broad RF bandwidth.

The arrangement of the pair of SBMs in Fig. 2 is routinely called a double balanced modulator or DBM. The combined response of both SBMs, balanced 180° between the input and output quadrature couplers, can be shown, to a first order, to be proportional to

$$M(I) \propto \tfrac{1}{2}(\Gamma-\bar{\Gamma}) + \epsilon(\Gamma+\bar{\Gamma}) + \epsilon\delta.$$

The coefficient ϵ represents the phase and amplitude imbalance of the quadrature couplers. Typically, in the microwave frequency range, $|\epsilon|$ and $|\delta|$ are ≤ 0.2, (or -14dB), over broader RF bandwidth. A detailed quantitative analysis and bias requirements of DBM are treated in [1] and [2]. On a qualitative level, it is sufficient to observe that, if a condition $\Gamma \approx -\bar{\Gamma}$ is maintained over the bias range I and $\bar{I}$, the maximum attenuation of the DBM approaches

$$M(I)_{min} = 2\epsilon\Gamma_o + \epsilon\delta,$$

where Γ_o is the minimum value, or $\Gamma_o \equiv \Gamma_{min} = \bar{\Gamma}_{min}$. In practical circuits, over the RF band of interests, $|\Gamma_o|$ varies between 0.1 and 0.2 (-14dB and -20dB respectively).

Dynamic Range Limitation of the Basic I/Q Modulator

The dynamic range of the I/Q modulator is limited by the attenuation range and phase distortion of the DBM. The above qualitative analysis suggests that the expected attenuation range of a broadband DBM, as shown in Fig. 2, is about 28 to 40 dB. As a tool for subsequent analysis, it is useful to construct a simplified error model. Let us redefine the normalized vector response of the basic DBM, i.e. M(I), according to Eqn. (1).

$$M(I) = m(I) + \mu \qquad (1)$$

The term m(I) is defined to have the properties of an ideal DBM: (i) m(I) is identical to a straight line through the origin of an I/Q plane, (ii) has the bi-phase relationship $m(I)=-m(\bar{I})$, (iii) has an infinite attenuation range ($m_{min}=0$) and, (iv) its magnitude is proportional to the control I. All the phase and

amplitude errors are accumulated in the complex term μ. It is implied by Eqn. (1) that μ is independent of the drive control, I. In practice, the magnitude of μ depends somewhat on the drive. Nevertheless, relative to magnitude of m(I) dependence on I, it is negligible. In terms of the frequency, the error term μ is highly dependent.

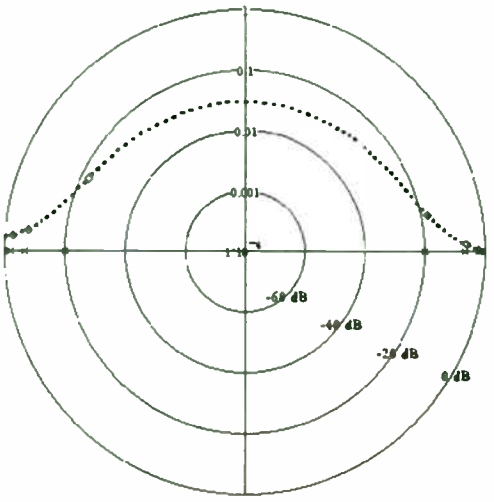

Figure 3: Typical Response of a Double Balanced Modulator

A typical response of a DBM is shown in the polar chart in Fig. 3. To increase the resolution of the phase and amplitude distortion near origin, the magnitude is plotted in dB. The outer circle, 0dB, corresponds to the minimum insertion loss of the device. Additional circles are spaced at -20dB intervals, with the -80dB point situated at the origin. Observe that the modulator curve M(I) spans from its minimum IL point at 0dB and 0°, through the maximum attenuation point at -32 dB at about 90° and continues to the point of minimum IL at about 170°. Using a lenient criteria, the useful control range of this response is limited to about -20 dB. At that magnitude, the bi-phase error approaches 45°. This phase error corresponds to the error term μ in Eqn. (1), and is frequency sensitive.

I/Q Modulator with an Extended Dynamic Range

In many common applications, a 20dB dynamic range I/Q modulator is adequate. Increasingly, however, broadband, higher dynamic range I/Q modulators are required for applications such as unwanted signal cancellation and linear equalization. The attenuation range increase is obtained by the I/Q modulator arrangement in Fig. 4, in which each path uses three DBM modulators.

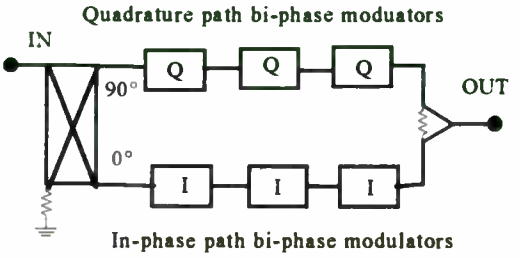

Figure 4: Extended Range I/Q Modulator

By cascading odd number of modulators, the overall attenuation range will be increased accordingly (note that an odd number is always required in order to preserve bi-phase property). Applying Eqn. (1) and given that each modulator has the normalized vector response M(I), the response of the cascade arrangement, labeled as $M_{sym}(I)$, is

$$\begin{aligned} M_{sym}(I) &\equiv M^3(I) \\ &= [\, m(I) + \mu \,]^3 \\ &= m^3(I) + \mu_{sym} \end{aligned} \qquad (2)$$

A few remarks are needed to substantiate Eqn. (2). (i) The effect of the VSWR mismatch has been ignored here, justified because the double balanced arrangement in Fig. 2 is inherently well matched. Any RF energy not transmitted through each modulator is practically absorbed by either the

diodes or 50Ω resistors terminating the outer quadrature couplers. As long as the diodes are correctly biased, their parasitics are equal and the couplers will have a good quadrature response. (ii) The subscript "sym" used in the equation implies that all three modulators are biased identically, i.e. symmetrically. (iii) The equation has been reformulated similarly to Eqn. (1), i.e. in terms of the ideal term $m^3(I)$ and the complex error μ_{sym} due to the phase and amplitude deviation from the straight line.

When Eqn. (2) is evaluated using the single section DBM response shown in Fig. 3, the result yields a response shown in Fig. 5 as a dashed curve. As expected, the attenuation range of the type in Fig. 4 has increased considerably. At the -60 dB attenuation level, the bi-phase error approaches 60°, still an unacceptably large value.

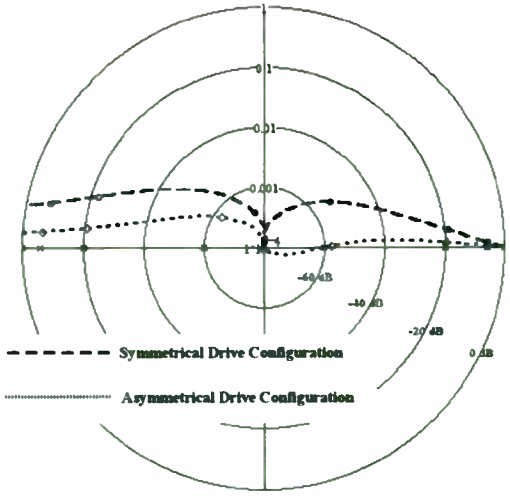

Figure 5: Phase Error of Extended Range I/Q Modulator

Asymmetric Drive Configuration with Reduced Bi-phase Error

The analysis of the three-section configuration assumed that all sections have an identical drive. Consider an alternative setup of the drives I and $\bar{I}$, such that the bias is inverted between successive stages. Therefore, the first and third stages are driven by bias $\bar{I}$ and the middle stage by I. The response of such asymmetrically biased configuration, $M_{asym}(I)$, can be obtained by appropriately altering the Eqn. (2), namely

$$\begin{aligned} M_{asym}(I) &\equiv M(\bar{I}) \cdot M(I) \cdot M(\bar{I}) \\ &= [-m(I) + \mu]^2 \cdot [m(I) + \mu] \\ &= m^3(I) + \mu_{asym} \end{aligned} \qquad (3)$$

Of interest is the comparison of the error terms μ_{sym} and μ_{asym} in the two alternate drive configurations. A simple algebraic manipulation of Eqns. (2) and (3) yields two expressions which are functions of μ, the error term for the single section. The result is shown in Eqn. (4).

$$\begin{aligned} \mu_{sym} &= 3\mu \cdot m^2(I) + \ldots \\ \mu_{asym} &= -\mu \cdot m^2(I) + \ldots \end{aligned} \qquad (4)$$

Only the largest term is of concern. Evidently, from Eqn. (4), the magnitude of the error is smaller for the asymmetric biased configuration. The response of $M_{asym}(I)$, the dotted curve in Fig. 5, can be compared to the $M_{sym}(I)$ response, the dashed curve. As predicted by Eqn. (4), the bi-phase error of the asymmetrical configuration is approximately 20° at the -60 dB circle -- a threefold reduction compared with the symmetrical case.

The essence of the above analysis has been to compare alternative bias configuration and provide a method of further improving the dynamic range of the I/Q modulator. However, this improvement does not come without cost. As the Eqn. (3) implies, the three modulators must have identical responses. Indeed a more rigorous analysis would indicate that even a small variation between the

individual modulators actually degrades the performance of the I/Q modulator.

Finally, the performance of the I/Q modulator is demonstrated with measured data for a typical GMC Model 7328 unit, presented in Fig. 6. The chart is in a polar format with same dB scale as in previous charts. The three curves are shown as responses to an I commands at 8, 12 and 16 GHz. At any given attenuation, the I commands are the same over the frequency. The Q command has been set at the origin, i.e. to a maximum attenuation. The plot graphically illustrates how closely the I/Q modulator matches the ideal axis over 60 dB attenuation range, independent of frequency.

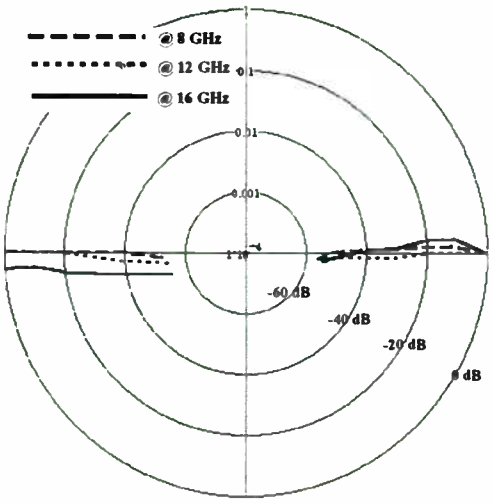

Figure 6: Model 7328 Measured Data

Conclusion

General Microwave has been actively pursuing the development of amplitude and phase control products over the past 20 years. Several models of broadband wide dynamic range I/Q modulators successfully employing the above scheme have been produced. In production, maintaining a proper level of reproducibility is of paramount importance. The key component in this scheme, necessary to maintain the required repeatability and RF bandwidth in the microwave frequency range, is the quadrature coupler. The I/Q modulators employ a proprietary quadrature hybrid originally designed by S. Hopfer [3]. This coupler, a very reproducible planar structure suitable for microwave integrated circuits, has coupling properties independent of etching tolerances. The excellent quadrature phase property maintained over an extremely wide frequency range is the consequence of the distributed nature of this coupling structure. Using these techniques General Microwave has developed a high dynamic range I/Q modulator in the 2.0 to 24.0 GHz frequency range which has become a useful tool resolving system integration problems and advancing state-of-the-art modulation techniques.

References:

1. Z. Adler and B. Smilowitz "Octave-Band High-Precision Balanced Modulator," *IEEE MTT-S International Microwave Symposium Digest, 1984.*

2. Z. Adler and P.Maritato, "Broadband Phase Invariant Attenuator", *IEEE MTT-S International Microwave Symposium Digest, 1988.*

3. S. Hopfer, "A Hybrid Coupler for Microstrip Configuration," *IEEE MTT-S International Microwave Symposium Digest, 1979.*

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LMDS -- A Wireless Solution to Last Mile Access

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Abstract

The wireless revolution of the 1990s is being extended beyond the realm of voice and data with a new technology called Local Multi-point Distribution Service(LMDS) having the capability of providing interactive wireless multimedia services. An LMDS system is essentially a fixed wireless broadband transport network that delivers 1.3 GHz of signal capacity in the **28-31 GHz** band. In a fully digital implementation, LMDS has the capacity to cost-effectively transport high speed data, advanced telephony and interactive video on the same RF channel to many users simultaneously.

Many telecommunication companies are looking at LMDS as a quick-to-market solution to last mile broadband access. The FCC is currently in the process of setting up an auction date(expected in October1996) and there is a great deal of interest being expressed by carriers as this will be the largest chunk of spectrum ever sold.

This paper will describe the basic system architecture for an LMDS system, system capabilties and constraints, implementation issues, current state of research and development and comparison to competing broadband alternatives. It will try to provide a realistic systems approach to broadband wireless communication for business and residential environments. It will discuss the various systems proposed for a seamless wireless ATM network of the future and show how a broadband wireless network can be the backbone of existing cellular and upcoming PCS systems.

1.8 - 2.7GHz Complete Full Duplex Radio Front End Chipset

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Abstract

A complete full duplex, high performance antenna to baseband chipset in the 1.8 to 2.7GHz range is now possible addressing many commercial applications for voice and data. The Chipset utilizes a single conversion architecture which minimizes external components and provides a compact, high level of integration while performing all RF, IF, and analog baseband filtering functions. The highly linear transmit and receive chains feature wide automatic gain control range, low spurious distortion, and excellent balance acceptable for many modulation applications. This paper presents and quantify the features, cost reduction advantages and overall flexibility of the chipset.

Overview

Digital wireless communication systems are combining voice and data services. These systems require highly integrated design solutions to meet cost and size objectives as well as achieve high performance. Applications like wireless local loops, Personal Communications Services (PCS), and ISM band transceivers are emerging worldwide. Harris Semiconductor has developed a complete full duplex antenna to baseband chipset which covers the 1.8 - 2.7GHz frequency range. Besides a broad frequency coverage, other features of this chipset make it versatile enough to address many of these emerging applications.

Combining voice and data services in a wireless communication system requires taking into account different critical requirements of each. Voice communication is more sensitive to real-time latency issues forcing many practical networking applications to provide full duplex operation. While in data communication bit errors are the concern, making robust data transmission even in difficult environments the requirement. With the high cost of frequency spectrum, all systems are concerned about maximizing user capacity and a key component is spectral efficiency. Many wireless digital systems today approach nearly one bit per Hertz spectral efficiency at reasonable cost, power, and performance. To enable this capability, the radio front end or RF/analog processing plays a critical role in determining overall performance. Some of the important radio parameters largely determined by the radio front end from RF to analog baseband are: RF frequency range, Rx noise figure, Rx input intercept point, Tx output power and spectral mask, Tx spurious emissions, gain or power control range, adjacent channel interference, quadrature balance, and in-band signal to noise and distortion.

The Harris Prism™ Full Duplex chipset provides a nearly complete radio front end solution, see Fig. 1. This chipset utilizes a single conversion architecture, quadrature modulation/demodulation, programmable analog baseband filtering, and wide AGC range for highly linear processing. All IC's operate from 2.7 - 5.5V single power supplies, across -40 - +85 degree centigrade temperature range, and have a power enable function for power saving modes of operation. A chipset design solution has many advantages including optimal parti-

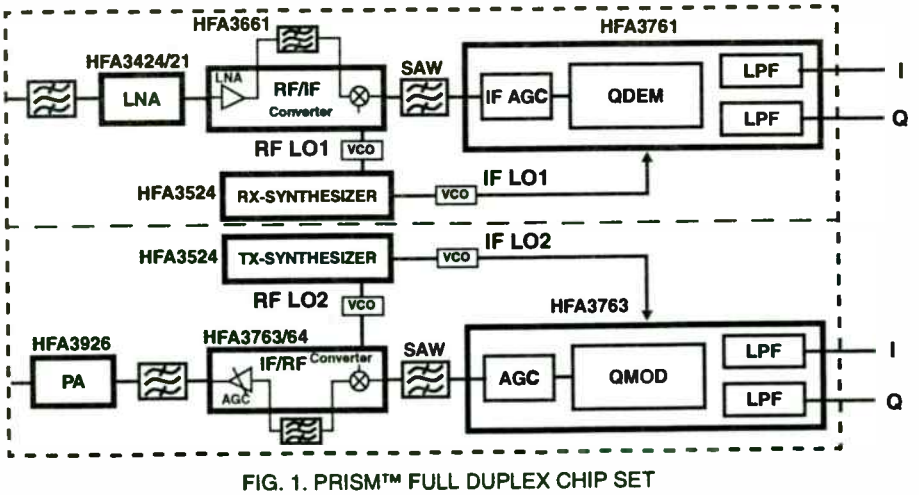

FIG. 1. PRISM™ FULL DUPLEX CHIP SET

tioning of functions by technology to give highest performance, and minimizing external components which include matching networks, interface circuits, and control or bias circuits being integrated. Other advantages a chipset gives are quicker time to market, proven technology that minimizes risks, zero or minimal manufacturing adjustments, lower costs, and consistent power supply and temperature. It would be illustrative in understanding the features of this chipset to site a specific type of system and see how it's characteristics can be met.

CDMA (Code Division Multiple Access) is the choice technology of several wireless standards as well as proprietary wireless systems. In this technology, each user signal consists of a unique pseudorandom binary sequence that modulates the carrier, spreading the spectrum of the waveform. This same spread frequency spectrum is shared by a large number of user's where each can be identified by their unique binary sequence. To minimize interference between users, it is vital that all signals in a specific bandwidth be at nearly the same power level and time aligned when their signals arrive at their common base station. The power control necessity means that all transmit signal chains must have a wide dynamic power control range. The chipset has typically 75db of analog power control range with additional step control range if needed. The Tx power control range is divided up with 45db at IF and 30db at RF frequencies to improve overall signal to noise. The IF and RF AGC controls can be either ganged together or operated independently. Signal to noise ratio (S/N) is degraded as power is lowered and can limit capacity in a given channel. The chipset achieves 30db of S/N even at 60db of power control attenuation applied.

CDMA systems typically require tight Tx spectral masks and low in-band distortions including carrier suppression and quadrature imbalances. These specifications translate into requiring transmit chain components with high IP3 or P1db (See section on individual component performance). Any analog baseband filtering must have low total harmonic distortion - typically 3% for this chipset, gain imbalance is typically 0.2db with phase imbalances <2 degrees for the total filter and modulator sections, and carrier suppression is 40dbc. Some systems do not require any extensive transmit baseband analog filtering in which case a 5th order Butterworth filter can be used for reconstruction or bypassed.

The receiver problem created by CDMA waveforms is complicated by the large number of user's sharing and transmitting on the same channel. The receiver must be capable of operating with large peak to average swings (e.g. 10db) created by receiving all these simultaneous users. This requires a highly linear Rx chain with enough overhead to handle these swings - high IP3 or P1db (See section on individual component performance). This waveform can be viewed as creating a "QAM like" signal space. For this reason, linear processing must be utilized and distortions minimized. Similar levels of demodulator and filter imbalances - 0.2db and 2 degrees, carrier suppression - 40dbc, and total harmonic distortion <3% are achieved by the chipset as on the Tx side. Wide dynamic AGC range is required to insure linear processing for near or far signals. The chipset achieves >75db of IF analog AGC while also providing an additional step LNA bypass control which enables an input IP3 of +1dbm.

RECEIVER SECTION

To illustrate the performance of this chipset a typical level diagram analysis of the receiver is shown in Fig. 2. Assumed input power levels of -110dbm, -40dbm, and -20dbm with their corresponding AGC control applied

Input Power vs AGC Ctrl		IL=3.5	G=13dB NF=1.9 OIP3=15	Bypass G=16 NF=3.8 OIP3=15 Byp IL=20 Byp NF=30 Byp OIP3= -1	IL=3.5	G=19 NF=12 OIP3=13	IL=16	IL=10	G=65 AGC=1.2V NF=11 OIP3= -4 G=0 AGC=2.1V NF=40 OIP3= -4 G=11 AGC=1.9V NF=28 OIP3= -4 63mVpp
-110dBm Vagc=1.2V	GAIN	-3.5dB	9.5dB	25.5dB	22.0dB	41dB	25.0dB	15.0dB	80dB
	NF	3.5dB	5.4dB	5.59dB	5.6dB	5.71dB	5.71dB	5.74dB	6.15dB
	InpIP3	-84	-28.1dBm	-28.1dBm	-28.1dBm	-10.61dBm	-10.61dBm	5.5dBm	∞ dBm
-40dBm Vagc=2.1V	GAIN	-3.5dB	9.5dB	25.5dB	22.0dB	41.0dB	25.0dB	15.0dB	15.0dB
	NF	3.50dB	5.40dB	5.59dB	5.60dB	5.71dB	5.71dB	5.74dB	25.05dB
	InpIP3	-28.6	-28.1dBm	-28.1dBm	-28.1dBm	-10.6dBm	-10.6dBm	5.5dBm	∞ dBm
-20dBm Vagc=1.9V Bypass Mode	GAIN	-3.5dB	9.5dB	-10.5dB	-14.0dB	5.0dB	-11.0dB	-21.0dB	-10.0dB
	NF	3.50dB	5.40dB	20.63dB	21.12dB	27.01dB	27.12dB	27.98dB	49.03dB
	InpIP3	0.95	2.58dBm	2.58dBm	2.58dBm	4.04dBm	4.04dBm	5.5dBm	∞ dBm

Previous AGC stage is specified in power gain with 50 to 500Ω input to output impedances . The demodulator and filters can be viewed as voltage gain blocks where noise figures are not of a concern. The table is built assuming a constant output of -30dBm @ 500Ω before the demodulator.

FIG. 2. CUMULATIVE RECEIVER LEVEL DIAGRAM vs AGC CONTROL

are provided. The -110dbm can be considered a minimum input sensitivity level and where near maximum gain is applied. The -40dbm level corresponds to where all IF analog AGC control is applied. The -20dbm level combines LNA bypass mode with IF analog AGC control to give the maximum input receiver level. The RF to Baseband Quadrature front end block exhibits in the 2.4 to 2.5GHz range an overall gain of 80dB with a noise figure of 6.15db when in full AGC gain setting of 1.2V as shown. Next, for maximum IF AGC control signal of 2.1V, this front end exhibits a gain of 15dB, a noise figure of 25db, and an input third order intercept point of -28dbm. Finally, using a bypass feature added to the second LNA/Mixer device, which makes the handling of strong signals manageable by external switching control, the overall gain is reduced to -10db with an improved Input IP3 of +1dbm. In resume, this highly linear RF/IF front end with a AGC dynamic range of 90db and -110dbm of sensitivity can successfully be applied in a variety of high performance radio applications.

Individual Receiver block descriptions

First LNA

This low noise amplifier, manufactured in a low noise Ion-Implanted, GaAs MESFET process is responsible for setting most of the receiver noise figure baseline. Fig. 3 depicts its typical block diagram. With a noise figure of 1.9dB and a careful choice of a low loss preselector or duplexer filter, the overall noise figure of the receiver can be set. Using the cascaded noise figure relationship and a filter loss of 3.5dB with typical gain of 13dB for the LNA, the baseline noise figure is calculated to be of 5.4dB. The next stages noise figures will add a small amount to this baseline.

Two devices are available which cover the 1.8 to 2.3GHz and the 2.3 to 2.7GHz ranges as shown in fig. 1. They are essentially of the same design but have been "tuned" to these different ranges. These devices are single supply amplifiers that draw a typical 5mA for a 5V supply operation and are parametrically tested and guaranteed for operation down to 2.7V. They feature on chip coupling capacitors that are optimized to work with the device parasitics and bond wires for good input and output return losses across the range of interest. No external RF tuning elements are necessary.

Another feature of these devices is the user access to the main source bias leg of the FET. The overall transistor biasing is set by a trimmed on chip AC decoupled resistor of approximately 200 ohms to ground. Gain, noise figure and intercept point can be improved with the expense of a higher supply current when an external resistor of around 30 to 35 ohms is added at this pin to ground. The designer can also make use of this pin to vary by small amounts the gain of the device upon application of external bias voltages at the pin to sink or source current from the FET as desired while being careful to keep the device in linear operation. Gain variations of +/- 6dB are possible by this method. Adding to the main features of these LNA's, it is worth mentioning the excellent input intercept point of 1dBm. 4.5dBm input IP3 is possible with preselector filters with 3.5dB of loss.

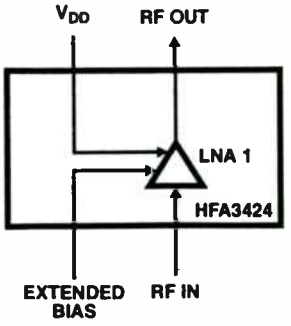

FIG. 3. LOW NOISE AMPLIFIER

Second LNA and RF/IF Down Converter

This device is manufactured in a Silicon Bipolar Bonded Wafer Dielectric Isolation process featuring ft's is excess of 12GHz. Its monolithic construction incorporates an LNA, down conversion mixer, IF driver amplifier, and biasing in a small 20 lead SSOP package. Please refer to block diagram in fig. 4. One device covers the entire frequency range as referred in this paper abstract. The IF operation ranges from 10 to in excess of 400MHz and the device uses a single supply ranging from 2.7 to 5.5V. Current consumption is moderate and on the order of 35 mA.

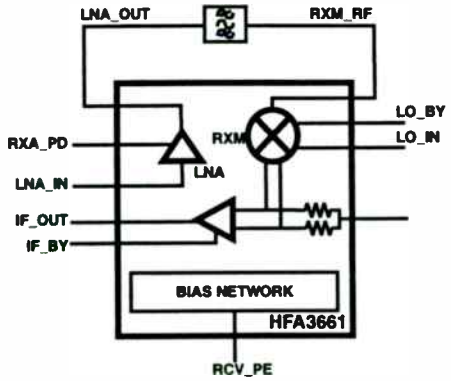

FIG. 4. LNA and RF/IF CONVERTER

The device uses a differential architecture for good isolation as well as rejection of common mode signals and better use of voltage overheads. To lower radio manufacturing costs, the device includes all internal matching networks with the exception of the IF output port which needs one external inductor. Low cost, small outline chip capacitors are used to AC couple all ports. The local oscillator drive level is -8dBm with a wide tolerance allowed enabling the use of lower cost, low power oscillators.

The device can be used as a moderate performance radio front end without an extra LNA due to the its own LNA noise figure ranging from 3.0 to 4.0dB across the 1.8 to 2.7GHz range. A LNA bypass mode set by digital control has been added to the device to permit the use of step AGC schemes allowing improved radio spurious free input dynamic range. When this step feature is used with the LNA mentioned in the previous section, an increase in SFDR of about 29dB can be managed and controlled as depicted in fig. 2. It is important to mention that a compromise of noise figure and third order intermodulation products have to be analyzed carefully when dealing with cascaded LNA's. Very often the use of intermediate pads can be considered for improvement of dynamic ranges with attention to the added noise figure they incur. The use of a bypass mode, when managed carefully, can largely improve the performance without resource to interstage attenuation.

The LNA included in this design has a gain ranging from 21 to 14dB across the frequency range with a constant 15dbm of output third order intercept. The gain variation, and its corresponding input IP3 variation needs to be included in the design for a specific band of operation. The LNA in a bypass mode shows a typical attenuation of 20dB. Following the LNA, the design requires the use of an image filter which is responsible for removing the image noise generated by the combination of two LNA's in cascade. The next stage, the down converter mixer, features a conversion gain of 19dB with an output intercept point of 13dBm across the frequency range. This large conversion gain eliminates the need for any additional IF gain stage. Note that at this point, the input intercept point is relatively low compared to the output intercept of the previous stage and the mixer is always a very critical component for generation of spurious and intermodulation products. Cascaded budget or level diagram analysis for a specific radio specification and bypass/padding decision are critical for optimization of SFDR at this stage. The down converter mixer has a noise figure of 12dB.

AGC IF Amplifier, I/Q Down Converter and Selectable Low Pass Filter

This multichip module is housed in a 80 pin Thin Quad Flat Pack package which includes two stages of independent AGC amplifiers, an I/Q quadrature down-converter and a set of selectable 5th order Butterworth Low Pass Filters. Adding to the cost advantages of this device is the highly integrated design with a minimum of external components and broadband operation. All devices included in this module use differential architecture for reasons explained in the last section. The chips are processed using a combination of a high performance Bonded Wafer DI bipolar and BiCMOS technologies and operate with a single supply in the range of 2.7 to 5.5V.

Referring to the block diagram of fig. 5, the independent AGC amplifiers and the I/Q down converters have frequency responses in excess of 400MHz which enable

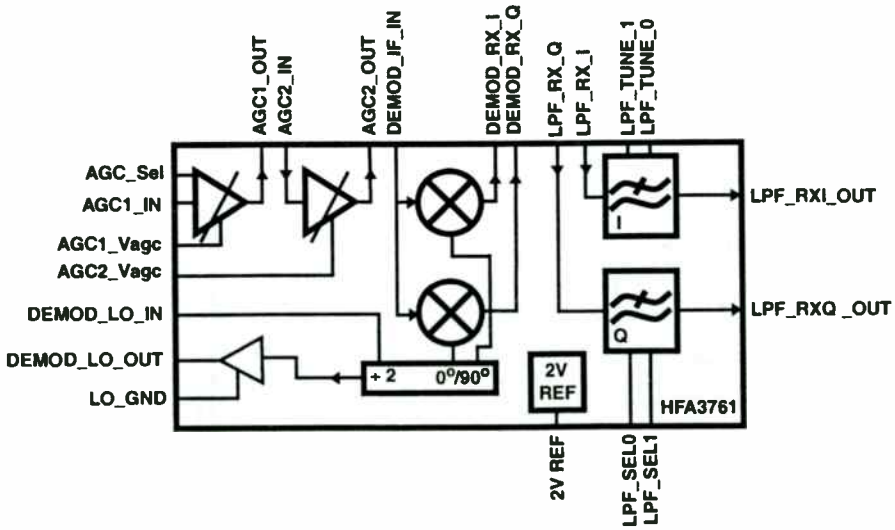

FIG. 5. AGC IF AMPLIFIER , I/Q DEMODULATOR

the use of higher IF's bringing the advantages of better image rejection, single conversion architecture and lower cost. The two cascaded AGC stages offer excellent stability and a overall voltage gain of 82dB for an output termination of 500 ohms. The first stage is set for single ended input while its output and the input of the next stage are fully differential. Featuring an input impedance of 50 ohms single ended, these devices are responsible for 75dB of AGC control range.

50 ohms or properly matched single ended SAW filters can easily interface with the AGC input. The SAW or IF filter set the channel bandwidth of the system. Their quasi brick wall characteristics with very steep bandstop attenuation is responsible for the channel separation of the radio front end and is very important to limit the noise bandwidth presented to very high gain chains such as AGC amplifiers. The insertion loss is accounted for in the overall cascaded gain of the system and plays an important role when these losses are relatively high for the overall radio gain specification. The two AGC amplifiers are independent from each other and the designer can access the differential output of the first stage and the differential input of the second stage for further interstage filtering if so desired. It is recommended the use of an interstate filter due to the broad 400MHz frequency response of both AGC amplifiers relative to the narrow SAW IF bandwidth response presented before the first AGC stage. This interstage filter limits the noise generated by the first AGC amplifier and improves the overall signal to noise ratio and sensitivity.

The AGC control pins are ganged together for full range or can be driven separately for convenience. The typical noise figure for each of the stages is of 10dB with an output compression point of -13dbm referred to 500 ohms (158.3mVrms). The output compression of the device is independent of the AGC. The signal output settling time for a full AGC range change within 1dB is 1.5uS and is mostly dependent on external AC input and interstage coupling components. The insertion phase change for a full AGC variation is of 300ps. Being a broadband device, its group delay and group delay variation with AGC are negligible.

Following the AGC chain, the next stage comprises the broadband I/Q baseband demodulator and Local Oscillator quadrature driver. A divide by two architecture and a duty cycle compensator form a broad band quadrature reference for the I and Q doubly balanced mixers. LO input frequencies in excess of 800MHz with input levels as low as -20dBm can be used by this divide by two input. Baseband amplitude and phase balance of 2° and 0.5dB are typical and 100% tested. The down conversion mixer has a voltage gain of 2.5V/V driving a 4Kohms differential load and exhibits a 1Kohms differential input impedance. This high impedance enables the differential AC coupling between the last AGC stage with an external termination of 1Kohm yielding a 500 ohms load for the AGC amplifier. The baseband rolloff frequency is of 30MHz enabling a multitude of data rates and spread spectrum chip rates. The demodulator compression output is of 1.25Vpp at a 4Kohms load. Care must be taken when driving the next filter stage to prevent overdrive.

The last stage in the overall receiver front end chain is the bank of Selectable Low Pass antialiasing filters. These filters are programmable in 4 selected bandwidths of 2.2, 4.4, 8.8 and 17.6MHz. These filters are "gm-C" filters which exhibit excellent phase and amplitude balance characteristics and can also enable fine tuning within +/-20% of the setting by an external resistor. These filters have only 3% of total harmonic distortion and are balanced within 2° and 0.5dB between the I and Q channels which reduces the cost of passive filtering and manufacturing tolerances. They exhibit 0db of gain, have a differential to single end architecture and have a typical linear output voltage swing of 550mVpp. This compression must be taken into account when performing the AGC function at the IF level (the previous stages, the demodulator and the AGC amplifiers can swing 1.11Vpp inputs without distortion to this filter bank). Another useful feature of the filter bank is the provision of a very accurate and thermally controlled voltage reference of 2V that can be used for A/D references or external application circuits.

TRANSMITTER SECTION

To illustrate the performance of the transmitter, a typical level diagram analysis is shown in Fig. 6. Assumed output power levels of +20dbm, and -40dbm with their corresponding AGC control applied are provided. The +20dbm can be considered the maximum output power case, and the -40dbm level corresponds to 60db of applied power control range. The RF and IF AGC controls are ganged in these examples, better S/N is possible with separate controls. The Baseband to RF Quadrature section block exhibits a linear output power of 20dBm with a 30dBc of main lobe to side lobe spectrum regrowth in the 2.4 to 2.5GHz range and overall gain of 28dB when in full AGC gain setting. For -40dbm output power, this transmitter exhibits a gain of -32dB with 29dB of signal to noise ratio @ a 2MHz bandwidth. This highly linear Baseband to RF section with an AGC dynamic range of 60db can successfully be applied in a variety of high performance radio applications where transmit power control is essential.

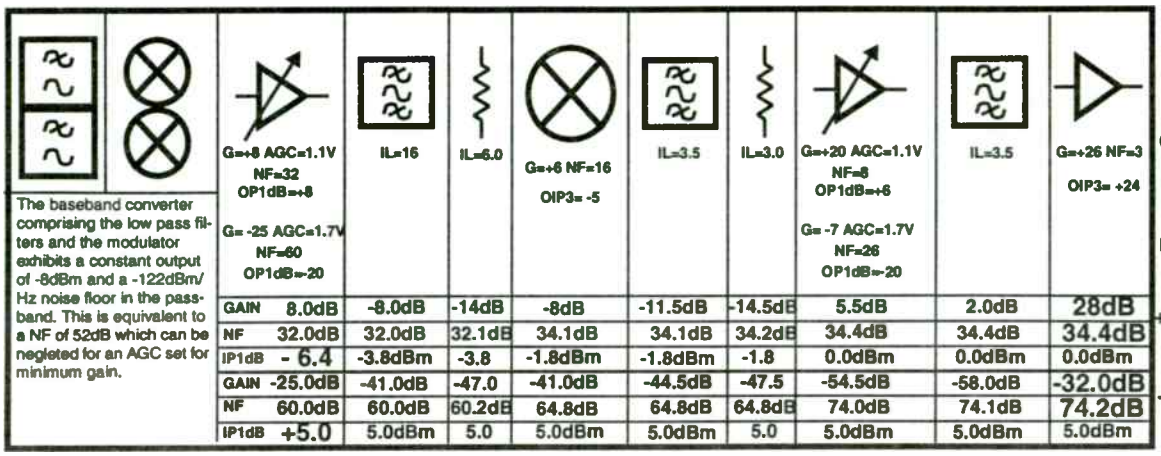

FIG. 6. CUMULATIVE TRANSMIT LEVEL DIAGRAM vs AGC CONTROL

Individual Transmitter block descriptions

Selectable Low Pass Shaping Filters, I/Q Modulator and IF AGC Amplifier

This is another multichip module housed in a 80 pin Thin Quad Flat Pack package which includes a set of selectable 5th order Butterworth Low Pass Filters, an I/Q quadrature upconverter and a output stage responsible for gain/attenuation control. The device is also a highly integrated design with minimum external components and broadband operation in excess of 400MHz. The devices are processed using the high performance Bonded Wafer DI technology, operate with single supply in the range of 2.7 to 5.5V, and use a differential architecture throughout. Please refer to the block diagram depicted in Fig. 7. The transmit section starts with a bank of selectable 5th order Butterworth filters which are identical to those presented in the I/Q demodulator section. The main feature of this input filter is the capability of selecting either TTL digital baseband signals or analog single ended pre-shaped signals like from a D/A converter. The analog input accepts signals of typically 550mVpp. These filters are responsible for pre-shaping the baseband signals according to a selected filter bandwidth as described in the previous section.

The group delay variation follows closely a 5th order Butterworth theoretical response which is known to be not exactly flat but introduces negligible system implementation losses for certain types of digital modulation. Fine tuning the selectable cutoff frequency enables the designer to adjust the filter response to compensate for any extra spectrum regrowth along the transmit chain. When properly AC coupled inputs are used, the LO

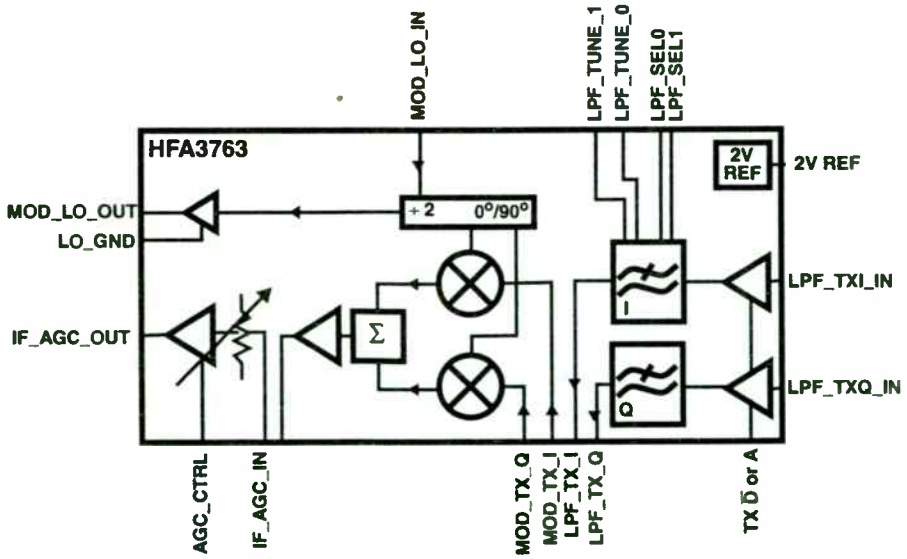

FIG. 7. I/Q MODULATOR and POWER CONTROL

leakage at the I/Q modulator is of the order of 40dBc.

Following the Baseband filtering bank, the shaped signals reach the input of the I/Q baseband quadrature up converter mixers. The architecture is very similar to the one used for down conversion with an LO of twice the frequency of operation and broadband response in excess of 400MHz. Phase and amplitude balance are of 2° and 0.5dB respectively which can be checked by its SSB characteristics or simply DC evaluated. The two I and Q outputs from the doubly balanced mixers are summed together and output to a single ended open collector port. This modulator stage outputs a -8dBm SSB signal into 250 ohms when two 90° apart baseband signals at 500mVpp each are applied to the I and Q inputs. Its output noise floor within the baseband filter passband is of -122dBm/Hz.

Following this stage, a 250 ohms input impedance amplifier/attenuator is available for power gain control and exhibits a gain control range in excess of 40dB. This amplifier has a power gain of 8dB and an attenuation range in excess of 40dB when referred to 250 ohms input and output. To complete this upconversion stage it is common to add a sharp cut off SAW filter device in order to reduce the excess out of band noise floor that could be amplified by the next stages causing potential adjacent channel interference and also help shape the spectrum further for reduction of the side lobes resulting from the I/Q modulation process.

RF Up Converter, AGC and Preamplifier

This device is manufactured in a Silicon Bipolar Bonded Wafer Dielectric Isolation process featuring ft's is excess of 12GHz. Its monolithic construction incorporates an Up Conversion mixer, a gain controlled preamplifier and biasing in a small 20 lead SSOP package. Please refer to block diagram in figure 8. Two devices are offered to cover the full 1.8 to 2.7GHZ range as pointed out in figure 1 and operate from a 2.7 to 5V supply. It features an doubly balanced mixer design for the up converter mixer with a conversion gain of 6dB, requiring a low power LO signal of -8dBm with wide tolerance. The device exhibits an LO leakage of approximately absolute -25dBm. The output compression point of the mixer is -5dBm. For the purpose of signal to noise calculations, its noise figure is 16dB. All ports are on-chip matched to 50 ohms and only coupling and decoupling capacitors are needed. At this stage in the chain it is usual to add a bandpass filter to the mixer output in order to; provide the first postselection of transmitting channels, reduce the out of band noise and mixing spurs, and the LO leakage before being fed to the preamplifier. This filter is not critical in terms of number of poles.

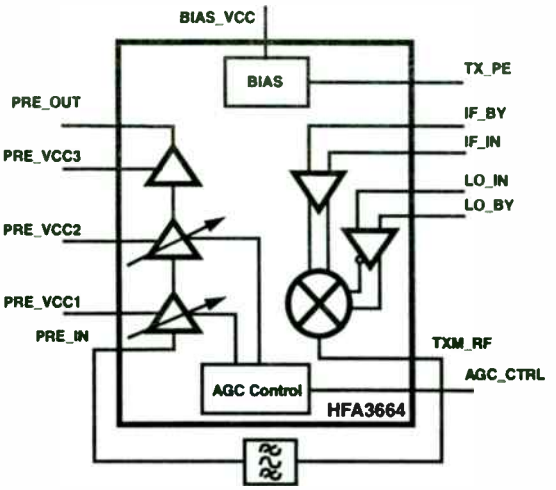

FIG. 8. IF/RF CONVERTER and AGC CONTROL

Two pole filters with a bandwidth of the channel bank of interest can suffice.

The next stage in the chain is the RF gain control preamplifier. It features a maximum gain for full AGC control of 22dB with an output compression point of +8dBm. Typical AGC range is 30dB. This gain control, combined with the 45dB of range of the previous stage (I/Q Modulator/Attenuator) yields a typical 75dB power control range for applications where transmit power control are necessary (CDMA for example). The relatively high output P1dB allows linear drive capability to satisfy many power amplifier applications. In applications requiring high performance it is a good idea to place a second filter after this preamplifier to further attenuate the LO leakage and also remove any spurious responses from the preamplifier. This filter is often placed before the power amplifier to make use of the full dynamic range and compression limitations of the power amplifier.

Power Amplifier

This GaAs power amplifier is a highly integrated solution housed in a 28 pin SSOP package. The block diagram is depicted in fig. 9. It is capable of linear operation up to 21dBm with a 24dBm compression point. It features three independent internally cascaded common source stages with individual gate and drain biasing. Its input and output are matched to 50 ohms within the 1.8 to 2.7Ghz range. With a typical linear gain of 32 to 24dB across the frequency range, this device is suitable for use with all other preceding stages for a complete radio solution. Operating with VDD's of 2.7 to 5.5V this device requires negative biasing of gates. The individual gate control topology and the use of a negative biasing scheme, brings flexibility for lower power operation and

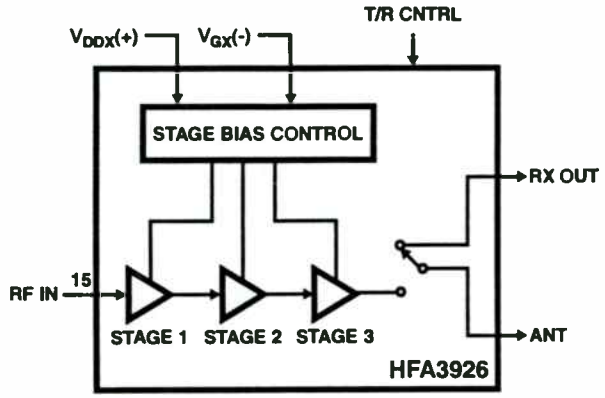

FIG. 9.RF POWER AMPLIFIER

enable optimization of each stage for either saturated, linear or a combination of both operations. Applications requiring high power linear class A operation may require fine tuning of DC bias and classical low cost FET biasing schemes are required for the last stage only. The use of a low cost and low loss harmonic filter following the power amplifier is the only requirement in case an antenna filter or duplexer is not used.

Dual Synthesizers

This paper presents a complete independent transmit/ receive duplex solution for a single conversion architecture, meaning the use of only one IF chain. This architecture requires the use of four local oscillators; two for the RF and the two for the IF quadrature demodulator and modulator mixers. For a full duplex operation sharing the same pc board, the designer always has the choice of using only one RF VCO frequency using high and low injection with a couple of VCO's for the IF mixers. This condition is not always advantageous for specific designs where careful choice of two different IF frequencies and channel frequency plans may not yield lower cost due to customizing of SAW filters, antenna duplexers and flexibility of frequency allocation. In this case, the designers choice is to use a pair of dual synthesizers and 4 VCO's.

Referring to Fig. 10, the chipset includes monolithic integrated dual synthesizers fabricated in a BiCMOS process where the RF LO can be as high as 2.5GHz and the IF LO can be as high as 600MHz. Using the classical dual modulus architecture, the device can operate from 2.7 to 5.5V and has very low power consumption and excellent phase noise capability. Its phase lock loop uses a current output charge pump technique that includes the removal of comparator dead zones and permits the use of simple PLL passive filtering for generation of very stable and low noise control voltages for VCO's. Counter, prescaler and various modes of operation are accomplished by a serial three wire data interface.

Conclusion

The Harris Prism™ Full Duplex Radio chipset allows antenna to baseband processing across the 1.8 to 2.7GHz range. All front end radio functions including RF, IF, and analog baseband filtering are performed.

The receiver analysis demonstrated how 90db of highly linear dynamic range can be achieved, with a

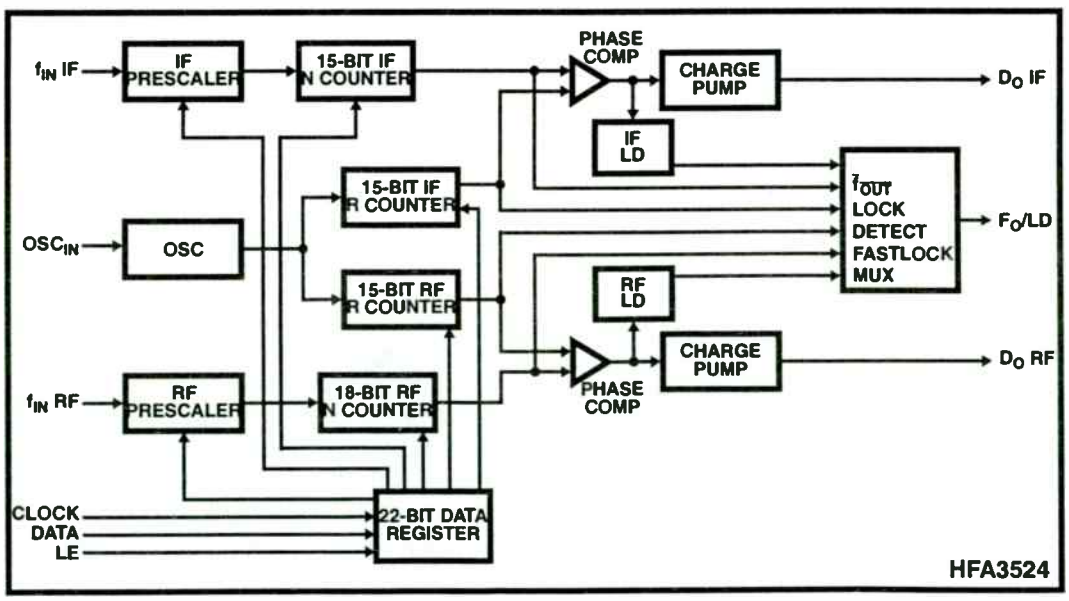

FIG. 10. DUAL SYNTHESIZER BLOCK DIAGRAM

maximum gain NF=6db and minimum gain input IP3=+1dbm. The transmitter analysis showed a +20dbm maximum output power with 30dbc main to first side lobe attenuation, and 30db of S/N even at 60db of power control attenuation. Excellent quadrature balance, 0.2db gain balance and 2 degrees phase balance, carrier suppression - 40dbc, and total harmonic distortion <3% were achieved. High IP3 and P1db specifications throughout the transmit and receive chains combine with wide AGC range >75db to provide highly linear processing.

The chipset works from 2.7 - 5.5V supplies, across -40 to +85 degree centigrade temperatures, and has power management functions. ■

Bibliography

1. "Communications Receivers Principles and Design" Ulrich L. Rohde, T.T.N. Bucher, McGraw Hill, 1988
2. "Single-Sideband System & Circuits" William E. Sabin, Edgar O. Schoenike, McGraw Hill, 1987
3. "Principles of Digital Communication and Coding" Andrew J. Viterbi, Jim K. Omura, McGraw Hill, 1979
4. "Digital Communication" Edward A. Lee, David G. Messerschmitt, Kluwer Academic Publishers, 1988
5. "Spread Spectrum Systems" Robert C. Dixon, John Wiley & Sons, 1984
6. Harris Semiconductor Preliminary Data Sheets:
   HFA3424 File # 4131
   HFA3661 File # 4240
   HFA3761 File # 4236
   HFA3524 File # 4062
   HFA3925 File # 4132
   HFA3663 File # 4241
   HFA3664 File # 4242
   HFA3763 File # 4237
   HFA3721 File "Advanced"
   HFA3926 File "Advanced"

MATERIALS AND PACKAGING TECHNOLOGIES

Materials and Packaging Technologies

Session Chairperson: David Light,
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Wireless Board Level Electronic Packaging - an Overview

Abstract - High frequency applications in the high volume Wireless industry impose unique requirements upon electronic packaging. This in turn necessitates the use of unique materials and processing capabilities. This paper will present an overview of typical functional requirements in high frequency printed wiring boards and will discuss what that means in terms of board designs, materials, and constructions. Certain future trends which may further differentiate high frequency board level electronic packaging will also be examined. The frequency range where design issues become 'different', what those issues are, and the materials and constructions available or being developed to resolve them will also be discussed.

The overview is intended to leave the audience with an awareness of the special needs that must be met for successful commercialization of wireless board level electronic packaging.

Dale Reed
Business Development
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High Power RF Transistors in Wireless Base Station Equipment: Assembly Packaging Needs

Jim Clemans
Lucent Technologies
Network Wireless Systems

Telecommunications equipment manufacturers are addressing the challenge of assembling high power RF transistor packages simultaneously onto a heat sink and an RF circuit board. This presentation will review the trends in designers' and manufacturers' needs, which are driven by customer requirements. The newest aspect of this board-level packaging design problem is the need for solutions that are suitable for cost-effective, high-volume manufacturing. Manufacturing cost and quality improvements must be addressed in the context of other engineering constraints. There are functional design needs for impedance matching and ever-increasing transistor heat dissipation requirements. The need for outdoor deployment of equipment increases environmental stresses so that functional performance and reliability requirements are more difficult to meet. The emphasis on smaller equipment profiles, which is concomitant with outdoor siting, also constrains the packaging design.

We will also discuss the possible improvement of the transistor package itself. The high thickness of gold on the transistor leads "as-fabricated" creates a reliability issue in a normal soldering environment. Transistor manufacturers could improve the ease of assembling their product for reliable use by manufacturing the transistor with a substantially reduced gold plating thickness on the leads.

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MULTILAYERABLE, LOW LOSS MATERIALS FOR HIGH FREQUENCY STRIPLINE CIRCUITS IN A HOMOGENEOUS MEDIUM

Authors: Chet Guiles, Rob Fuller, Paul Kyle

There is a large and growing selection of substrate materials available to the high frequency PWB designer. This can be both a benefit and a source of confusion. Despite the large selection of available materials, the production of low cost, microwave printed wiring boards with stripline or dual offset stripline circuitry in a homogeneous dielectric environment has been an elusive goal for the design community.

The availability of a 'B-staged' prepreg offers significant advantages in design and simulation, processing, uniformity of electrical performance and cost when compared to low loss substrates requiring bonding sheets which do not match the physical or electrical properties of the base laminate material. Fusion bonding of low loss thermoplastics such as PTFE laminates will provide a homogeneous environment, but requires high temperature lamination processing (350°C) and necessitates unique surface activation prior to metallization of the PTFE.

This paper will describe a low loss thermoset material system developed by Arlon which enables a fully homogeneous, low loss multilayer package with the following key properties:

- Er (Dielectric Constant) = 3.2 to 3.4 at 1 GHz
- Loss Tangent = 0.0025-0.003 at 1 GHz
- Low Dispersion (Er Stable from 1 MHz to 10 GHz)
- CTEr (Thermal Coefficient of Er) = 0 between -20 and +140°C
- Prepreg Bonding Sheets Available
- Processing Similar to Conventional Laminates (Polyimide, FR-4)

The paper will address the key design-related properties of this new material (designated Arlon 25N) for microwave and high speed digital applications, and will review basic processing information for construction of high frequency printed wiring boards.

Thermo-Mechanical Integrity of Area Array Interconnections on Microwave Laminates

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Abstract

Low-cost, low-loss laminate circuit substrates with thermoplastic or thermoset polymeric materials are finding increasing use in microwave applications, as commercial market segments such as wireless communications grow. Examples of these microwave materials include low-loss thermoset materials (GE's Getek and Rogers Corporation's 4003), woven-glass reinforced PTFE materials (Taconic Plastics' 602 and TLC 32, Arlon's AR320), and ceramic-loaded PTFE materials (Rogers' 3003 and Arlon's CLTE). A number of different issues must be considered when selecting a microwave laminate material for high frequency applications, including electrical characteristics (loss tangent, dielectric constant, dispersion factor), thermo-mechanical properties and their impact on package integrity, ease of fabrication, compatibility with multilayer constructions, etc. The goal of the present study is to assess the thermo-mechanical integrity of the assembly interfaces of a package constructed from these materials. Specifically, the reliability of area array solder interconnections (Ball Grid Array or Flip Chip Attach) to packages constructed from common microwave laminate materials will be assessed. Since alumina-based ceramic packages are a common high-frequency alternative to the above package materials, the thermo-mechanical behavior of these microwave laminates will be compared to alumina substrates. In this study, the thermo-mechanical behavior of the various laminates is used to build finite element models of a representative multilayer circuit board (with one signal layer and one power layer). A representative DCA package with an area array interconnection between the package and the laminate is also modeled using finite elements. Comparisons are made between the materials on the basis of the relative thermo-mechanical deformation of the packages on different laminates and on the basis of the relative integrity of solder joints attached to the different laminates.

PLATED THROUGH HOLE INTEGRITY IN FLUOROPOLYMER LAMINATE-BASED PRINTED WIRING BOARDS

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ABSTRACT

The use of fluoropolymer-based dielectric materials is rapidly increasing in commercial printed wiring boards (PWB's). This has been driven largely by growth in RF/microwave-frequency applications for the wireless communications market, where the favorable electrical properties of these materials at high frequency provide significant performance advantages. Concurrently, there has been a trend toward integration of increased functionality into the printed wiring board. Multiple RF/microwave functions, as well as power distribution, digital signal processing, and control circuitry, are frequently being embedded into a single, multilayer board. With this trend, board layer count and thickness are also increasing.

Many of the fluoropolymer-based laminate materials available have a relatively high coefficient of thermal expansion out-of-plane (in the z-axis). For this reason, reliability of the plated through holes (PTHs) used to interconnect the various conductor planes of a multilayer board can be at risk. To address this concern, and provide guidance for designers in specifying materials, board thickness, layer count, drilled hole diameter, pad size, plated copper thickness, and copper mechanical properties, activity is underway at IBM Microelectronics to develop predictive models for the field life of plated through holes. These models will incorporate the key design elements and material properties of the PWB. They are also intended to provide guidance in specifying appropriate stress testing procedures and conditions, performed on a sampling basis, to ensure consistent plated-through-hole integrity. A critical part of this activity is to experimentally measure the integrity of plated through holes in microwave laminate materials of various designs and through varied stress test conditions, and to integrate the results into the models being developed. This paper will review the mechanical aspects of plated through hole integrity, and will describe the work in progress to develop predictive tools for PTH integrity in microwave printed wiring boards. Preliminary experimental results will be reviewed and discussed.

INTRODUCTION

Fluoropolymer-based laminate materials can provide significant advantages for high-frequency electronic packaging applications. Low dissipation factor (typically 0.001 to 0.002) minimizes signal attenuation at high operating frequencies. Dissipation factor and dielectric constant are relatively stable across a broad frequency band and temperature range. Low moisture absorbtion, high temperature stability, resistance to electromigration shorting mechanisms, and low modulus for reduced internal and interfacial stresses also provide advantages for many applications.
Despite these advantages, many fluoropolymer-based laminate materials have an out-of-plane (Z-axis) coefficient of thermal expansion (CTE) which is significantly higher than standard laminate materials. This is of particular concern for woven and non-woven glass-reinforced polytetrafluoroethylene (PTFE) (most reinforced fluoropolymer laminate materials are PTFE-based), where the z-axis CTE can range to over 250 ppm/C. Ceramic particle-filled fluoropolymers have much lower Z-axis CTE values, in the range of 24 to 40 ppm/C. The woven-glass reinforced PTFE materials provide enhanced rigidity and easier handling during processing and assembly than the ceramic or microfiber filled materials. Price is often lower as well. However, the reliability of PTHs through surface finishing (Hot Air Solder Levelling or solder fusing), component assembly processing, product storage and shipping, and thermal cycling during field life can be at risk for some designs. Many high frequency PWB applications, particularly in the wireless communications industry, specify long product field lifetimes (often 10-20 years), increasing the overall stress the PTH must withstand in the field.

While a significant amount of work has been performed to understand the reliability of plated through holes in standard laminate material constructions (FR4), little effort has been focussed on microwave-compatible laminates. Work that has been done has been primarily empirical. We are not aware of quantitative, predictive tools available to assess PTH reliability in PTFE-based laminate constructions. In order to provide guidelines for design engineers with regard to laminate material selection, board layer count and thickness, drilled hole diameter, plated copper thickness, pad size, copper mechanical properties and stress test conditions, IBM is developing analytical models to predict the field life of PTHs. These models incorporate Z-axis CTE and compressive modulus of the laminate material, the board thickness, PTH diameter, pad size, copper thickness, and copper ductility and tensile strength. Initial models have been constructed for high density, digital fluoropolymer PWB designs for high performance computer packaging, utilizing thin (2 mil) ceramic-filled PTFE, fine diameter (4 mil) plated through holes, and thin copper plating (0.4 mils). These models were shown to be consistent with experimental stress testing data for this product set. The current activity is focussed on designs and materials more typical of RF/microwave-frequency PWBs for wireless communications applications (including woven-glass PTFE, thick cross-sections (20 mils+), larger diameter PTHs (10-125 mils), and thicker copper plating (1 mil+)). Test boards have been fabricated to provide an experimental database for correlation with the models being developed.

BACKGROUND

Failures in the plated-through-holes of printed wiring boards are primarily due to tensile deformation caused by mismatch of out-of-plane thermal displacements between the laminate dielectric materials and the plated copper in the PTH 'barrel'(1). These failures can lead to continuous or intermittent open circuits in the PWB assembly, requiring replacement or repair (e.g. circuit re-routing with coaxial wire). Significant costs can be incurred as a result of these failures, particularly when field or warranty service is required, or when a PWB assembled with expensive components must be scrapped.

The thermal displacement mismatch between copper and the typical laminate dielectric material is due to mismatch in the out-of-plane coefficient of thermal expansion (CTE) between the materials. Copper expands at a fairly constant rate of 17 parts per million per degree Celsius (ppm/C) over the practical temperature range for PWB fabrication, assembly, and field usage. Typical laminate materials such as FR4 epoxy-glass expand at approximately 50-75 ppm/C out of plane below the glass transition temperature (Tg) of the epoxy (usually 125 to 140C), and 400 ppm/C above Tg. The compressive modulus (compliancy) of FR4 decreases significantly from its room temperature value above its Tg (2). Fluoropolymer-based laminate materials generally exhibit a constant CTE value from room temperature to the melt transition temperature (327C for polytetrafluoro-ethylene). The value of the CTE is dependent on the type of reinforcement (woven glass, chopped glass, ceramic particle). Since most electronic equipment operates below the Tg of FR4 materials, out of plane expansion and contraction during field life is relatively modest. Recent trends toward increased functional integration and higher circuit density in PWB's has led to smaller diameter PTHs and thicker boards, however, and in some cases long-term wearout failures of 'good' (defect-free) PTHs can occur. More frequently, failures in PTHs occur due to non-uniform plating thickness or discontinuities in the plating distribution; these defects act to concentrate stress and are frequently the locus of crack initiation (3).

Strain levels during component assembly are typically significantly higher than in field life. Solder reflow temperatures are well above the Tg of FR4. Significant tensile stress is imposed on the PTH due to this large temperature swing and the very high z-axis CTE of FR4 above its Tg. The PTH effectively acts as a rivet in the PWB. Expansion of the laminate leads to thermomechanical deformation (strain) of the PTH barrel, and bending of the surface pads (becoming concave). Barker et al (2) found stress due to z-axis laminate expansion to be highest at the midplane of the PTH, with relatively high values at the corners of the surface pads and the innerplanes. The high stress of the PTH-surface pad junction is associated with bending of the pad with respect to the PTH barrel, with the corner acting as a hinge. The amount of stress on the PTH barrel and corners is related in part to the diameter of the surface pad; a larger pad for a given PTH diameter would be expected to resist depression into the laminate material in response to tensile stress to a greater extent than a smaller pad; the result would be a greater allocation of strain to the PTH copper relative to dielectric compression than with a smaller pad size.

Strain in the plastic range is cumulative. Therefore, copper fatigue which occurs due to the substantial thermal cycle (or cycles in the case of multiple reflows) during component assembly can predispose the PTH to early failure in the field. However, even strain in the elastic range can lead to metallurgical changes in the copper PTH, which can shorten PTH life in the field. Barker et al (2) found that component assembly processes can actually have two opposing effects on PTH life. The first, as described above, is strain in the PTH in response to tensile stress due to CTE mismatch between the dielectric material and copper. The latter is compressive residual stress in the PTH barrel due to contraction of the dielectric material at a faster rate than the copper during cooldown. This can act to mitigate the effect of subsequent tensile stress due to thermal cycling to some extent.

The failure sites for PTHs subjected to cyclic thermomechanical strain are either circumferential barrel cracks, interfacial cracks occurring at the barrel junction to innerplanes, or cracks at the 'corner' of the PTH where it enters the surface pads (4). Barrel fractures initiated at these sites during during component assembly may be arrested before complete fracture occurs, and it may require subsequent thermal cycles to propagate these cracks to complete separation. These 'latent' defects can be difficult to detect and therefore can be present in product shipped to the field, where temperature cycling during field life may complete the fracture (2). PTH copper which has fatigued significantly due to assembly thermal stress without cracking can also predispose the PTH to early failure, but is nearly impossible to detect. Analytical models which can predict excessive fatigue are therefore of significant value.

Fatigue, as applied to the behavior of metals, is a detectable change in the mechanical properties of the metal in response to a cyclically variable stress of sufficient magnitude. Fatigue failure in metals can be defined as the premature fracture of metals under repeatedly applied low stress (5). Fatigue failure can occur in copper PTHs due to thermal displacement upon thermal cycling, and is a consequence of the localized slip deformation which occurs within the individual crystals of copper as dislocations move through them and pile up at the grain boundaries. This slip deformation results in plastic deformation (strain) of the PTH. Accumulation of plastic strain can occur through repeated low level thermomechanical stress, eventually leading to crack initiation and propagation through the copper barrel (5). For this reason, the failure process is strongly dependent on the magnitude of the gross cyclic plastic deformation of the metal, which in turn is determined by the dielectric material properties (z-axis CTE, compressive modulus), the range of the thermal cycle, the product design, and the metallurgy of the copper PTH.

Fluoropolymer-based dielectric materials, as mentioned, provide specific electrical properties which may be required for many high speed and/or high frequency packaging applications. These materials are available reinforced with chopped glass, woven glass, and particulate ceramic. The former two materials typically have very high coefficients of thermal expansion out of plane (z-axis), in the range of 150-250 ppm/C, due to the high thermal expansion of neat PTFE relative to epoxy. The ceramic-filled materials have a significantly lower CTE, in the range

of 24-40 ppm/C, as they are highly loaded with low-expansion, particulate silica. Table 1 shows typical z-axis CTE values for the different varieties of PTFE-based laminate materials as well as FR4 epoxy.

REINFORCEMENT TYPE	DIELECTRIC CONSTANT AT 10 GHz	DISSIPATION FACTOR AT 10 GHz	Z-AXIS CTE (ppm/C) (0-100C)	COMPRESSIVE MODULUS (kpsi)
WOVEN GLASS	2.20	0.0009	252-280	237
WOVEN GLASS	3.00	0.0029	71	372
CHOPPED GLASS	2.20	0.0009	237	136
CHOPPED GLASS	2.33	0.0012	173	120
CERAMIC PARTICLE	2.94	0.0012	24	100
FR4 EPOXY (WOVEN GLASS)	4-4.5	0.02-0.03	50-70 (below Tg) 400 (above Tg)	800-1500

Table 1. Comparison of key electrical and mechanical properties of PTFE-based microwave laminate materials and FR4 (at room temperature unless otherwise noted).

It is interesting to note that while glass-reinforced, PTFE-based laminates have significantly higher z-axis CTE values than FR4-based laminates below the Tg of FR4, above its Tg FR4 exceeds the CTE of these microwave laminates.
Table 1 also lists the compressive modulus of these different materials. The stress and strain in a solid are related directly by the modulus of the material; a high modulus material is more resistant to deformation (strain) under load (stress) than a low modulus material. The dielectric material's modulus is also a critical parameter in determining the amount of strain that occurs in a PTH through thermal cycling due to the CTE mismatch between the laminate and copper. In the hypothetical case of an incompressible polymer, all of the displacement due to laminate thermal expansion would be accomodated by strain of the copper barrel. In actual situations, the compressive modulus of the dielectric material determines in part how much of the displacement is apportioned between strain in the copper PTH and compression of the dielectric material. The modulus of glass-reinforced epoxy materials is significantly higher than that of PTFE-based materials (even above Tg), so the higher z-axis CTE for the fluoropolymers is partially mitigated by the greater compliancy of these materials. Note that from the perspective of PTH copper strain due to thermal cycling, the ceramic-loaded PTFE materials provide the best combination of

low z-axis CTE and low modulus. Likewise, the low dielectric constant, woven-glass reinforced PTFE materials have very high z-axis CTE and an intermediate modulus, leading to the greatest PTH strain during thermal cycling. Above its Tg, FR4 has the highest z-axis CTE and compressive modulus of the materials shown in table 1. As a result, cycles to failure is expected to be significantly lower than for ceramic-filled PTFE. This has been demonstrated by Arthur and Kozij (13). It can also be seen from table 1 that as the dielectric constant and dissipation factor decrease for a given class of microwave material, the z-axis CTE increases. This is because these electrical properties are proportional to the ratio of glass filler to PTFE in the laminate.

Previous work has identified several consistent trends regarding the effects of product design and materials on PTH reliability:

PTH reliability (number of thermal cycles to failure) increases with:
- a-increasing copper ductility and tensile strength
- b-increasing minimum plating thickness
- c-increasing PTH diameter
- d-decreasing plating non-uniformity
- e-decreasing pad diameter
- f-decreasing temperature excursion
- g-decreasing effective CTE of the dielectric material
- h-decreasing compressive modulus of the dielectric material
- i-decreasing thickness of the dielectric material (length of barrel)

(4), (7), and (8).
Items e,f,g,h, and i reduce PTH strain by reducing load (tensile stress) on the barrel. Items b,c, and d reduce PTH strain by increasing the resistance of the PTH to deformation under tensile load. Item a relates to the ability of a copper deposit to accomodate a given strain without fatigue or failure.

FINITE ELEMENT ANALYSIS

Numerous studies have been published which utilized numerical or finite element analysis to investigate the reliability of plated through holes (1-3, 7, 9-12). The authors are aware of no published models relating to PTH integrity in fluoropolymer-based printed wiring boards. For this reason, work has been initiated to develop predictive models for PTH integrity in microwave PWBs fabricated from PTFE-based or other low loss laminate materials. Finite element methods are being used to solve the models in this study. A unit cell consisting of the PTH and the surrounding dielectric material is being modelled as an axi-symmetric structure. Uniform heating and cooling rates are being assumed. Commercially available finite element code is being used to solve the models. Initial models are being constructed for simple, two-sided PWBs with no innerplanes. Future effort will be directed toward more complex structures with multiple innerplanes. Model predictions will be correlated with experimental results to determine accuracy of the models, which will be refined based on the experimental results. Details of the models, their predictions, and the results of correlation with experimental results will be reported in a future publication. This paper will focus on the experimental results for a single dielectric material and thickness.

EXPERIMENTAL

Initial experiments have been performed with a single material type and thickness. 20 mil (508 um) thick Arlon DiClad 880 (R), a woven-glass reinforced, PTFE-based microwave material, were fabricated into test panels using a standard 18 x 24" panel format. Each panel contains two identical test vehicle images ('half-panels'). Each half-panel contains coupons consisting of 10, 30, and 125 mil diameter PTHs. PTHs of a given diameter are stitched together in groups to form electrically testable wiring nets. Table 2 shows the distribution of PTHs in nets and coupons.

PTH Diameter (inches)	No. Holes Per Net	No. Nets Per Coupon	No. Coupons Per Half-Panel	Pad Dia. (inches)	PTH Pitch (inches)
0.010	46	6	5	0.030	0.050
0.030	30	3	3	0.090	0.150
0.125 (large land)	26	3	2	0.375	0.450
0.125 (small land)	10	6	2	0.138	0.200

Table 2. Distribution of PTHs in nets, coupons, and test vehicles broken out by diameter. Pad diameter and PTH center-to-center spacing is also shown.

Surface pads (lands) for the different sized PTHs were scaled according to the diameter of the PTH, such that the ratio of hole diameter to land diameter was constant for the three landed PTH sizes. In addition, coupons were included with 125 mil diameter PTHs of nearly 'landless' design (surface pad diameter approximately equal to PTH diameter) (table 2). This was done to allow investigation of the effect of pad size on PTH reliability.

Figure 1 shows the approximate layout of test coupons on the half-panel sized test vehicles.

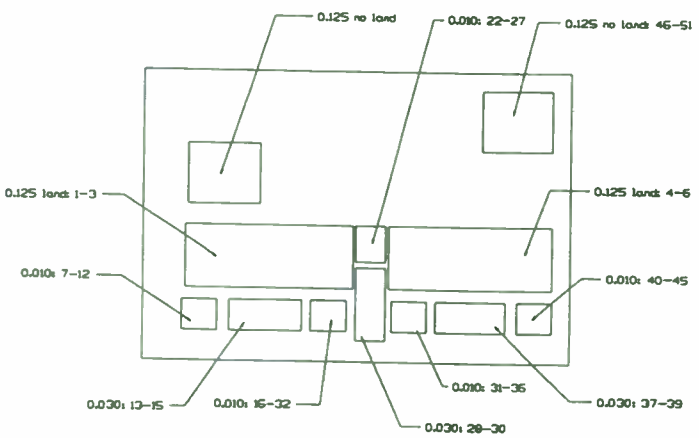

Figure 1. Non-scaled drawing of approximate layout of test coupons on 12 x 18 inch 'half-panel'.

Each coupon is designed to accomodate a connector to enable automated 4 pole monitoring of the electrical resistance of these stitched PTH nets. Measurements were performed at room temperature. Deviation of resistance by more than 10 milliohms from initial values was considered a failure

Two lots of panels were fabricated, to allow investigation of two different nominal plated copper thicknesses in the PTHs (1.0 and 1.7 mils). All nets were tested after fabrication. Additionally, angled X-ray images were taken to identify complete or partial defects in the PTH copper plating. Nets with high resistance values at time zero, and/or anomalies visible in X-ray imaging, were not used for the reliability data base. Data will be analyzed from some of these nets, however, to gain a better understanding of the sensitivity of PTH reliability to pre-existing defects.

After testing, all parts were subjected to a typical component assembly reflow cycle, in a conveyorized IR oven (216 C peak temperature), to simulate the pre-stressing typical PWBs would endure prior to field usage. Nets were again electrically tested following simulated assembly. Figure 2 shows the thermal profile for the precondition cycle used to simulate component assembly processing.

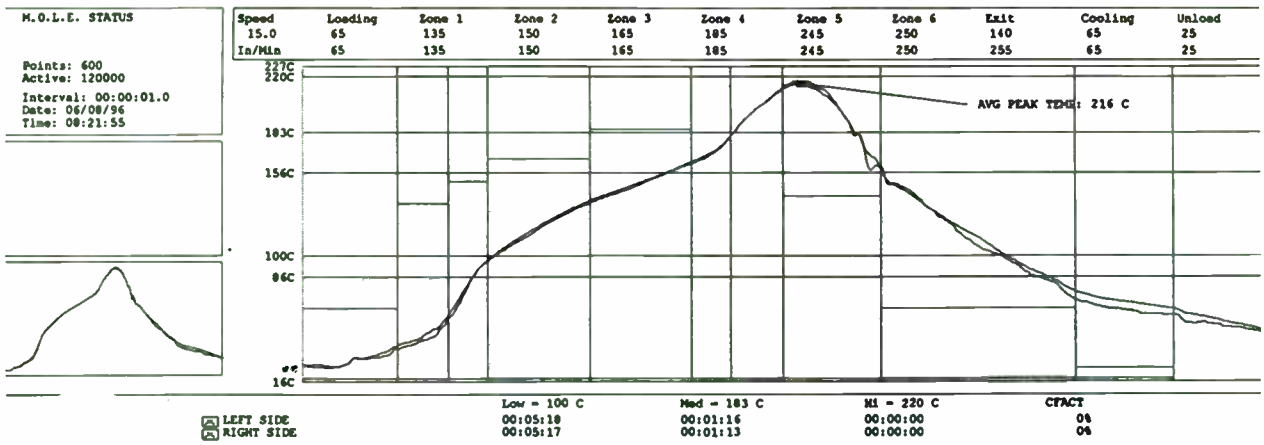

Figure 2. Thermal profile for the precondition cycle used to simulate component assembly processing for a typical eutectic solder.

Test vehicles were then placed in accelerated thermal cycle (ATC) test chambers. Test parts were divided into several different cells for exposure to varying degrees of thermal stress (25 to 75C, 25 to 170C, -55 to 125C). The allocation of coupons in the different test cells is shown in table 3. Table 3 also shows the planned number of cycles for each test cell. Thermal cycling will be continued beyond this number of cycles if necessary to generate sufficient fails to provide a statistically significant data base. Depending on the total number of cycles run, electrical resistance readings will be taken at 100, 200, 400, 700, 1000, 1400, 1800, 2200, 2600 and 3000 cycles.

Cell #	Thermal Cycle (C)	Number of Coupons 0.010"	0.030"	0.125" (large pad)	0.125" (small pad)
1 (1 mil plating)	25 to 75 3000 cycles	7	15	10	0
2 (1.7 mil plating)	25 to 75 3000 cycles	7	15	10	0
3 (1 mil plating)	25 to 170 1000 cycles	7	15	10	0
4 (1.7 mil plating)	25 to 170 1000 cycles	7	15	10	0
5 (1 mil plating)	-55 to 125 1000 cycles	7	15	10	4
6 (1.7 mil plating)	-55 to 125 1000 cycles	7	15	10	4

Table 3. Experimental layout showing different cells for plated copper thickness, PTH diameter (and pad size), and ATC temperature range. 10 mil PTH coupons contain 276 holes each; 30 mil coupons contain 90 holes. Large pad 125 mil coupons contain 78 holes, and small pad 125 mil coupons contain 60 holes each.

Table 4 shows the details of the ATC temperature profiles.

ATC Cell	Cycles/hour (approx.)	Dwell	Ramp Rate
25 to 75C (50C delta)	3	5 min.	10C/min
25 to 170C (145C delta)	1	5 min.	6C/min
-55 to 125C (180C delta)	1	5 min.	7C/min

Table 4. Cycles per hour, temperature ramp rates, and dwell times for ATC testing.

In addition to the standard ATC stress testing, additional samples were assigned to Current-Induced Thermal Cycling (CITC). CITC provides a significantly faster thermal cycling capability, reducing the time required for reliability evaluations. Additionally, equipment costs and complexity are significantly reduced for CITC versus standard ATC chambers. However, CITC is limited in the sample size which can be tested. Care must be taken in defining the cycle to achieve an appropriate level of thermal stress which can be correlated to field conditions or other stress test methodologies (ATC). CITC testing was performed at two conditions, 25 to 75C and 25 to 170C. Temperature ramp rate was 1C/min, and dwell time at the temperature extremes was 15 sec. 30 mil diameter PTHs with 1 mil copper plating thickness were tested. 12 nets have been tested, with 30 PTHs per net.

RESULTS AND DISCUSSION

The data from some of the test cells was plotted using a two-parameter weibull fit. In these graphs, the cumulative percentage of nets which have failed (increase in resistance greater than 10 milliohms) is plotted versus the number of ATC cycles run. Most nets showed complete open circuits when they failed.
Figure 3 shows the data from the 30 mil PTH, 1.0 mil plating thickness, and -55 to 125C ATC cell plotted on a weibull graph (since the data is grouped, i.e. read out at three intervals, only three data points are shown, although they represent 45 actual test failures in this cell). A best fit straight line is also plotted. Two parameters have been calculated from this data. The shape parameter indicates whether failure rate is decreasing (shape < 1), stable (shape = 1) or increasing (shape > 1). A shape < 1 is generally attributed to a large early failure rate due to the presence of defects. A shape equal to 1 would be indicative of the true intrinsic failure rate. A shape parameter > 1 would be attributed to increasing failure rate due to wear-out (fatigue failure) of the PTHs. The cell plotted in figure 3 has a shape parameter of 5.08, indicating failure rate is increasing due to wear-out of the PTHs. This is the expected response to the high stress loading in this cell (-55 to 125C) and a low incidence of pre-existing defects in the PTHs. The scale parameter indicates the number of cycles of a given temperature range at which 63% of the population is expected to fail (analogous to the N50 for a population). For the cell plotted in figure 3, 63% of the PTHs would be expected to fail by 721 ATC cycles based on this scale parameter. Other test cells (10 and 30 mil PTH) are shown in figures 4-6 (through 1000 cycles). (No fails occurred for 125 mil PTHs through 1000 cycles). Corresponding shape and scale parameters are shown on each graph. In all cases shown, the shape parameter indicates wear-out of the PTHs has occurred due to copper fatigue. Figure 10 shows a cell where there are early life fails and/or the population is non-homogeneous. Note the shape parameter for this experimental cell is less than 1. Experimental cells exhibiting this behavior will be cross-sectioned and failures will be analyzed to determine if they can be attributed to pre-existing defects in the PTHs or copper metallurgy, or whether the failure mode is non-uniform across the samples (i.e. multiple failure modes). Non-uniform failures will be censored from the data so that only uniform, wearout driven failure data is fed into the finite element models.

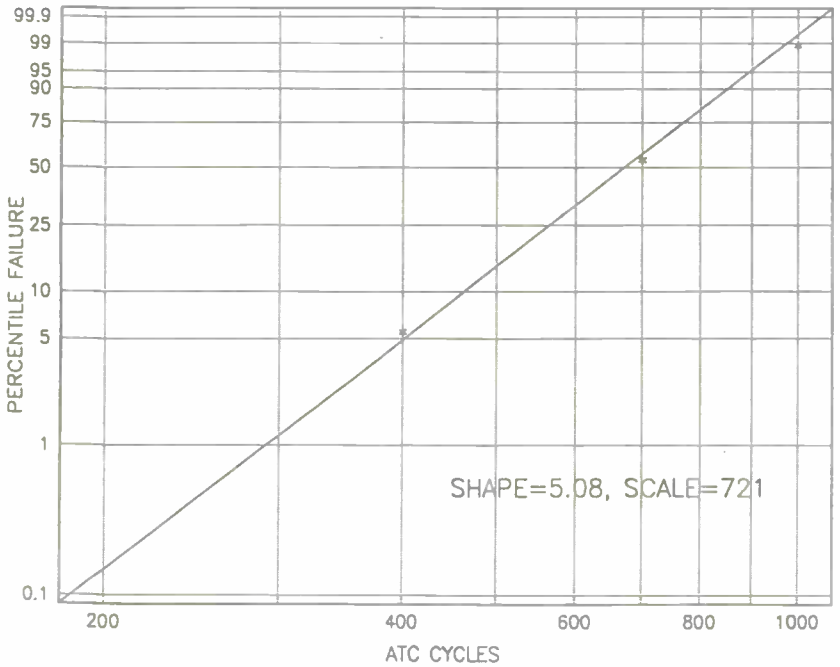

Figure 3: Weibull plot of 30 mil PTH, 1.0 mil plate, -55/125 ATC.

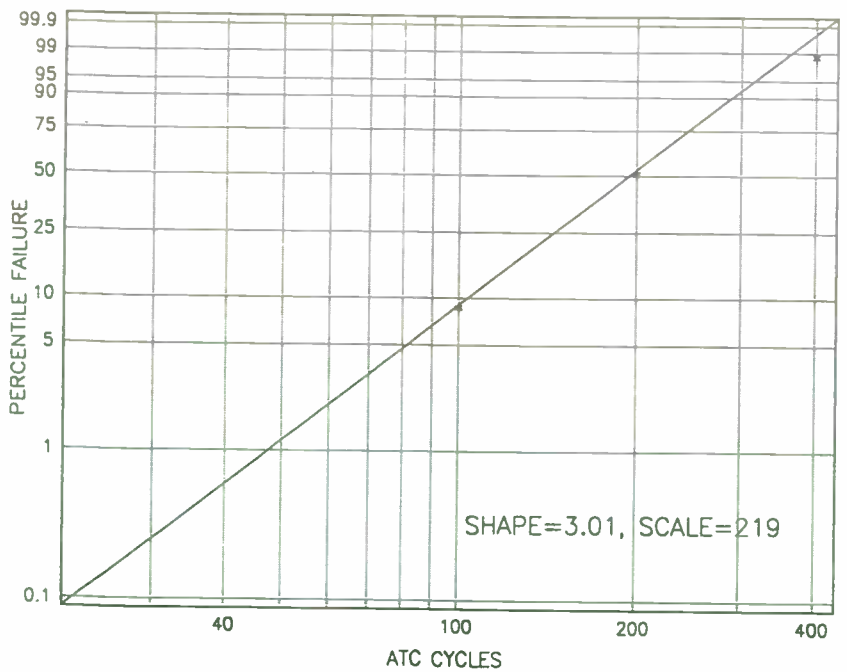

Figure 4: Weibull plot of 10 mil PTH, 1.0 mil plate, -55/125 ATC.

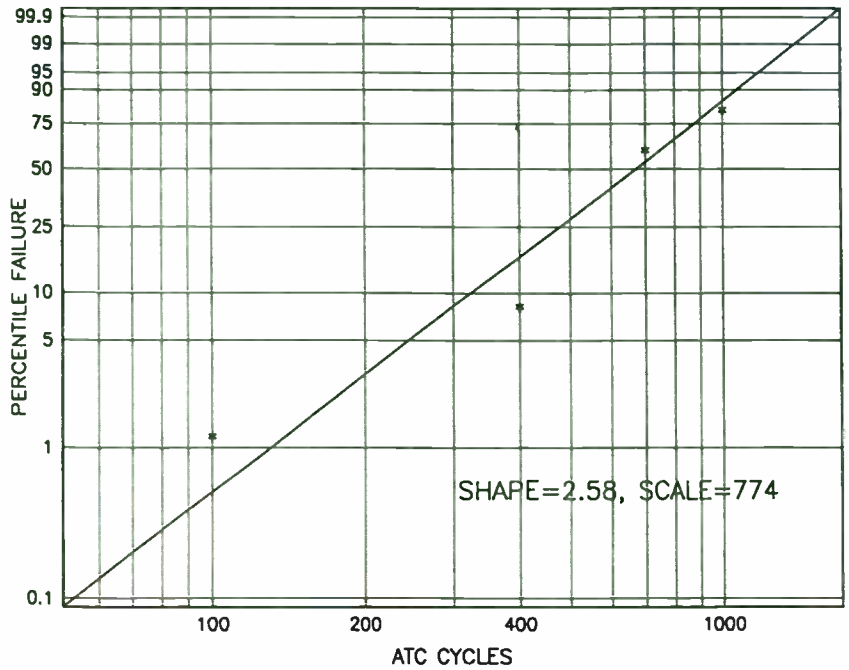

Figure 5: Weibull plot of 10 mil PTH, 1.7 mil plate, -55/125 ATC.

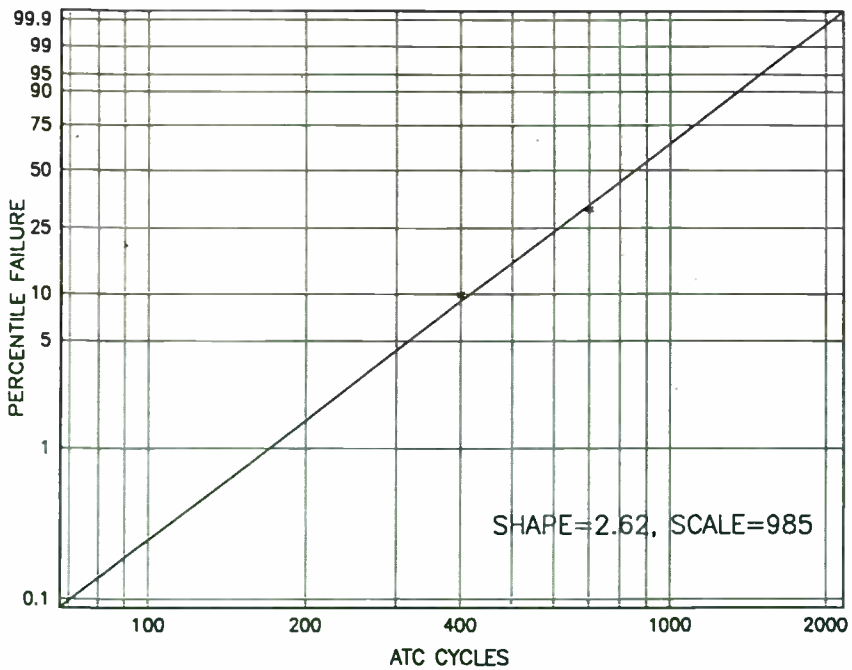

Figure 6: Weibull plot of 30 mil PTH, 1.0 mil plate, 25/170 ATC.

Figure 7 shows an example of the data that is used to 'calibrate' the models. In this plot, the 10 and 30 mil PTH data are displayed together for the -55 to 125C ATC cells (1 mil copper thickness). As shown in table 5 below, the shape and scale parameters for the 10 mil diameter PTHs are 3.01 and 219 respectively; the shape and scale parameters for the 30 mil PTHs are 5.08 and 721. Shape parameters of 3.01 and 5.08 are fairly similar, and as seen in figure 7, the slope of the two lines are nearly the same. This lends support to the assumption that the failure modes between these two populations are similar. This assumption will be verified by cross sectioning the failure sites once the samples are taken off of test. Given that the 10 and 30 mil diameter PTH populations are exhibiting the same failure modes, one can determine the relative fatigue life for a 10 mil PTH vs a 30 mil PTH for this PWB design and material set. This is calculated by taking the ratio of the scale parameters for the two populations:

$$\text{Scale}_{30} / \text{Scale}_{10} = 721/219 = 3.29$$

This indicates that the 30 mil PTH has approximately a 3 times longer lifetime through thermal cycling from -55 to 125C than a 10 mil PTH in this product.

Similarly, figure 8 shows a comparison between 1.0 mil plating and 1.7 mil plating for 10 mil diameter PTH's tested in -55 to 125C ATC. The fatigue life improvement is

$$\text{Scale}_{1.7} / \text{Scale}_{1.0} = 774/219 = 3.53$$

due to increasing plated copper thickness from 1.0 to 1.7 mils in these 10 mil PTHs. These data points will be used to calibrate and verify the finite element models which are being developed.

Cell Description	Shape	Scale
10 mil PTH, 1.0 mil plate, -55/125 ATC	3.01	219
30 mil PTH, 1.0 mil plate, -55/125 ATC	5.08	721
10 mil PTH, 1.7 mil plate, -55/125 ATC	2.58	774
30 mil PTH, 1.0 mil plate, 25/170 ATC	2.62	985

Table 5. Shape and scale parameters from weibull analyses of several experimental cells.

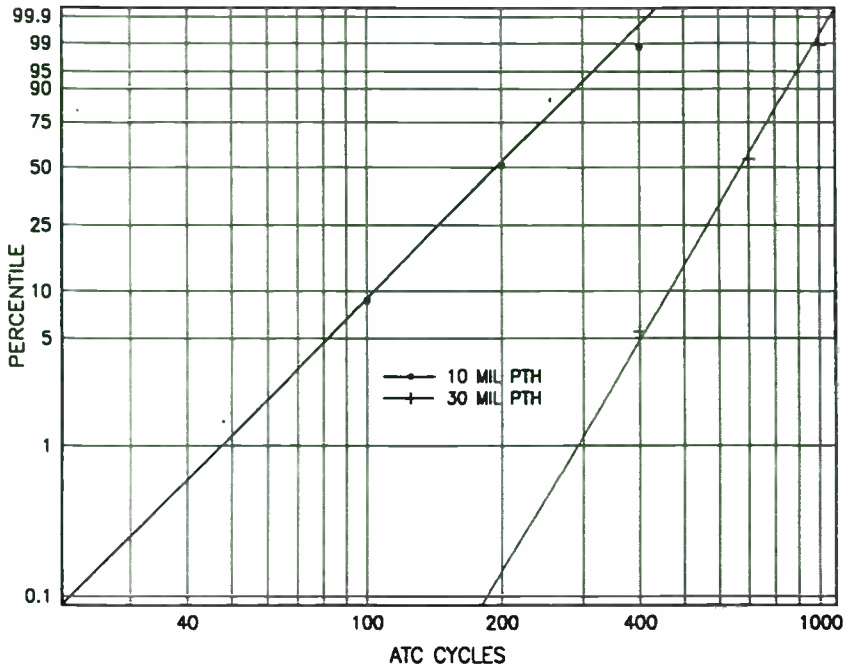

Figure 7: Weibull plot of 10 vs 30 mil PTH, 1.0 mil plate, -55/125 ATC

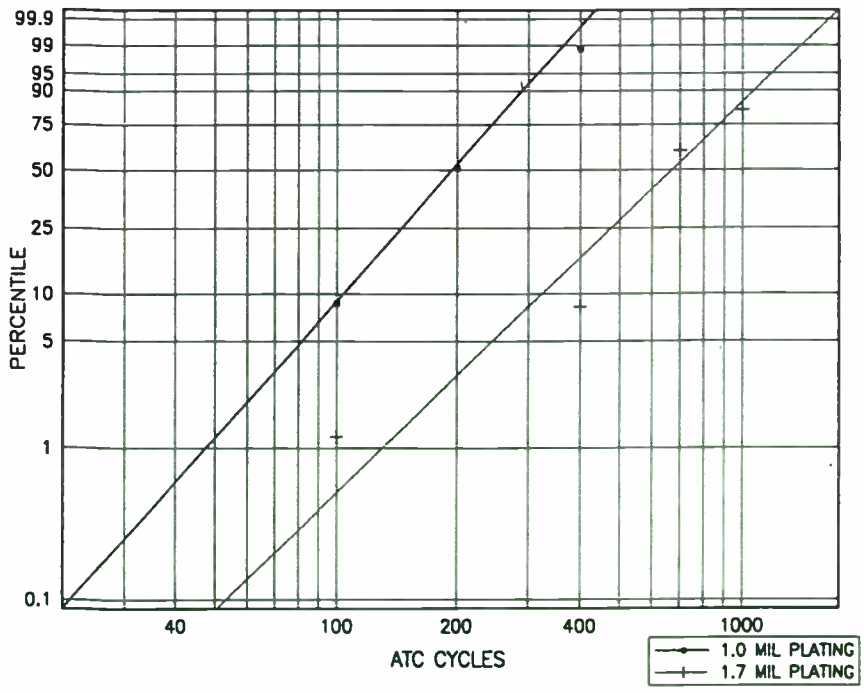

Figure 8: Weibull plot of 1.0 vs 1.7 mil plate, 10 mil PTH, -55/125 ATC

Once calibration of the models is complete, the design, process, and stress data will be used to predict field performance for the PTHs. Typically, a simple Coffin-Manson acceleration formula is used to project from one stress condition to another or from a stress condition to field conditions. The formula commonly used for copper PTHs is:

$$(\Delta T_1 / \Delta T_2)^2 = \text{Acceleration Factor}$$

In this equation, the strain term within the parentheses is assumed to be linear. Figure 9 shows a weibull plot of the -55 to 125C ATC data for 30 mil PTHs with 1 mil thick copper plating (solid line). From this data, the Coffin-Manson equation has been used to project the expected fail data for the 25 to 170C ATC cell for 30 mil PTHs with 1 mil copper. Results of this projection are shown as the dashed line in figure 9. The dotted line in figure 9 is a plot of the experimental data for the 25 to 170C ATC testing performed on the 30 mil PTHs with 1 mil copper. It can be seen that the experimental data for the 25 to 170C cell and the data projected by the Coffin-Manson equation do not correlate well. There are several possible reasons for this. First, the failure modes may not be the same for the two different temperature ranges. Second, a significant portion of the coupons in the 25 to 170C test cell have not been tested to failure yet, and the data may be premature; as the testing progresses further, the actual data may converge with the projected data. Finally, it may be that the strain term in the Coffin-Manson equation is not linear for this product and stress range, and may have to be modified. If this proves to be the case, the three stress conditions (25 to 75, 25 to 170 and -55 to 125C) will be used to define a non-linear strain term.

In addition to the ATC testing, CITC testing is being performed in parallel for the 25 to 75C and 25 to 170C conditions. The advantage of using CITC is that the parts can be run to failure more quickly, particularly for the low stress cell (25 to 75C). The testing is incomplete at this time, and for this reason the results will be deferred to a future publication. Preliminary data suggests that for the test vehicle design used here, acceleration due to CITC testing is significantly greater than for ATC testing for a given temperature range and number of cycles.

It can be seen from the data presented above that the trends observed with respect to the impact of PTH diameter and copper thickness on the cycles to failure for PTHs in high z-CTE microwave laminates are consistent with data published for standard (FR4 epoxy-glass) materials; increased diameter and thicker copper plating improve the reliability of the PTH. As the modelling and correlation with experimental data is completed, it is hoped that accurate, verified tools will be available with which to predict the reliability of plated through holes through end of line processing and field life.

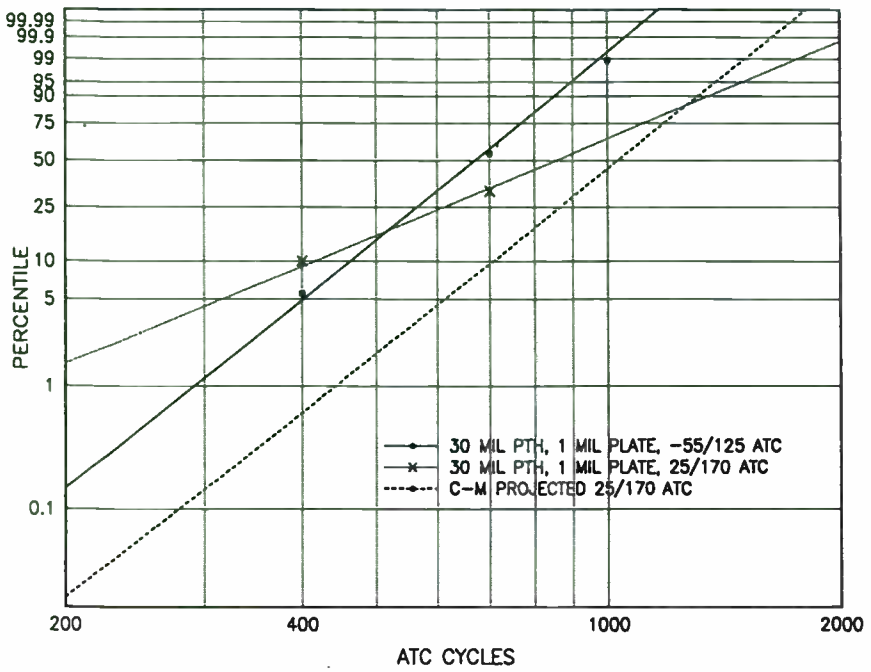

Figure 9: Weibull plot of projected vs actual failure rates for 30 mil PTH, 1.0 mil plate, 25/170 ATC.

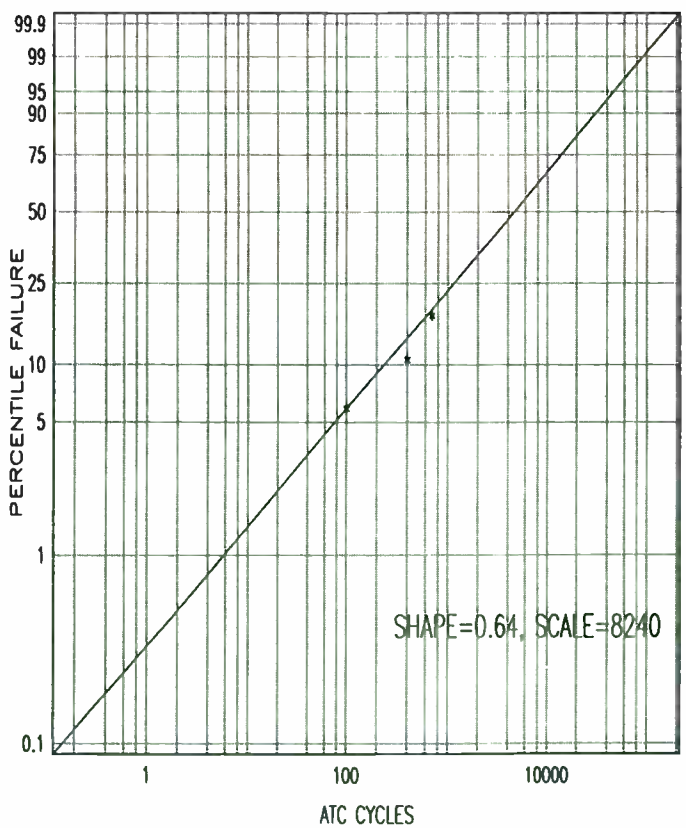

Figure 10. Weibull plot of 10 mil PTH, 1.7 mil copper plate, 25 to 170C ATC.

FUTURE WORK

The work reported here is the first phase of a broader activity. The overall effort aims to develop verified, predictive models for PTH reliability in PWBs fabricated with microwave materials spanning the typical range of mechanical properties observed in high frequency, commercial designs (z-axis CTE, compressive modulus, reinforcement-type, polymer material, and thickness). The current work utilized one dielectric material (20 mil Arlon DiClad 880, woven glass-reinforced PTFE). Activity is underway to experimentally measure the PTH fatigue behavior in PWBs fabricated from the other general categories of commercial microwave materials (ceramic-filled PTFE, low loss thermosets) as a function of PWB thickness. The plan is summarized in Table 6.

Material Type	PWB Thickness	PTH Diameters	Copper Thickness	ATC
Arlon Diclad 880	20,60,120 mils	10,30,125 mils	1.0,1.7 mils	25 to 75C 25 to 170C -55 to 125C
Rogers RO3003(R)	20,60,120 mils	10,30,125 mils	1.0 mils	-55 to 125C
Rogers RO4003(R)	20,60,120 mils	10,30,125 mils	1.0 mils	-55 to 125C

Table 6. Summary of additional experimental cells which will be run to support development of a generic set of predictive models for PTH reliability in microwave PWB designs.

SUMMARY

Work is underway to develop predictive models for PTH integrity in printed wiring boards fabricated with commercial microwave laminate materials. Initial test results demonstrate improved PTH integrity resulting from increased PTH diameter and increased plated copper thickness. Failures are observed for low aspect ratio (2:1, 1:1.5) plated through holes following a relatively small number of ATC cycles. This can be explained by the high z-axis CTE of the laminate materials used for this study, which is typical of many high frequency materials.

ACKNOWLEDGEMENTS

The authors wish to acknowledge their colleagues who supported this activity, including Andy Seman, Stan Albrechta and the Advanced Circuit Center in IBM where panels were fabricated; Chris Boyko for assistance with plating; Sam Sariti for x-ray support; Jim Ohara and John Kresge for test vehicle design; Joe Zdimal for test vehicle preconditioning; Giana Phelan for help in designing the study and organizing the early activities; and Randy Hoffman for assisting with stress test and sample preparation. Donald Farquhar and Thomas Light participated in helpful discussions on the fatigue behavior of metals. Thanks also go to Bob Daigle and Rob McCard at Rogers Corp. for material samples.

REFERENCES

1 K. Ramakrishna, W.T. Chen, G.H. Thiel, J.E. Steinwall, and T.M. Niu "Plated Through Holes in Thick Printed Wiring Boards: Interaction Between Design, Materials, and Assembly Processes", Proceedings of the Winter Meeting of the ASME, Chicago, IL, Nov. 6-11, 1994.

2. D. Barker, M. Pecht, A. Dasgupta and S. Naqvi, "Transient Thermal Stress Analysis of a Plated Through Hole Subjected to Wave Soldering" Journal of Electronic Packaging, Vol. 113, June, 1991, p. 149-155.

3. K. Ramakrishna, G. Subbarayan, and B. Sammakia, "Effect of Non-Uniformities and Defects on PTH Strain During Assembly and Accelerated Thermal Cycling", Proc. of the First ASME/JSME Joint Packaging Conference, Milpitas, CA, April 9-12, 1992, pp. 891-909

4. K. Kurosawa, Y. Takeda, K. Takagi, and H. Kawamata, "An Investigation of the Reliability Behavior of PTHs in Multilayer Printed Wiring Boards", Proceedings of the IPC Fall Meeting, Dallas, TX, Sept. 1991

5. R.E. Smallman, Modern Physical Metallurgy, Butterworth & Co., 1962 Sec. 2.5.5, Sec. 9.3

6. L.F. Coffin, Jr. and J.F. Tavernelli, "The Cyclic Straining and Fatigue of Metals", Transactions of the Metallurgical Society of AIME, Volume 215, Oct. 1959, P. 794-807.

7. R. Iannuzzelli, "Predicting Plated-Through-Hole Reliability in High Temperature Manufacturing Processes", IEEE 0569-5503/91/0000-0410, 1991.

8. D. Dinella, "The Reliability of Small Diameter Plated Through Holes (PTH) in Printed Wiring Boards", Proceedings of 2nd International SAMPE Electronics Conference, June 14-16, 1988.

9. B. Ozmat, H. Walker, and M. Elkins, "A Nonlinear Thermal Stress Analysis of the Plated Through Holes Of Printed Wiring Boards", Proceedings of the International Electronics Packaging Technical Conference, Marlborough, MA, 1990, P. 359-381.

10. T. Wu, Y. Guo, and W. Chen, "Thermal-Mechanical Strain Characterization for Printed Wiring Boards", IBM J. Res. Develop. Vol. 37, No. 5, Sept. 1993

11. L.C. Lee, V.S. Darekar, C.K. Lim, "Micromechanics of Multilayer Printed Circuit Boards", IBM J. Res. Develop., Vol. 28, No 6, November, 1984.

12. K. Ramakrishna, B. Sammakia, "Analysis of Strains in Plated Through Holes During Current Induced Thermal Cycling of a Printed Wiring Board", Proc. of ASME Intl. Mech. Eng. Congress, Nov. 12-17, 1995.

13. D. Arthur and E. Kozij, "PTH Reliability of High Peformance PWB Material", Proc. of the Intl. Electronics Packaging Soc. Conf., 1988, pp. 74-86.

Overview of Wireless and Microwave Packaging at Georgia Tech's Packaging Research Center

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With the emergence of wireless applications as perhaps the most financially significant market in recent years , wireless technology has become a global core competency. The demand for increasingly higher rates of data transmission, from voice to video and data, will drive technology to exploiting higher frequencies, where bandwith for channel capacity is easier to find. The emerging applications of personal communication networks, wireless local area networks, satellite communications and automotive electronics provide the impetus for the wireless electronics thrust. Successful insertion of wireless technology requires effective integration of digital, analog and RF/microwave technologies compatible with the demands of the commercial market place. A second technical driver will be the desire of the consumer for smaller size and lighter weight in portable and handheld products, which, in turn, will accelerate improvements in integration density and dc/rf conversion efficiency. At the same time, as the wireless component technology area broadens its focus from high performance to include low cost manufacturing techniques, it is clear that an equally important driving force behind advances in this field will be sustainable volume.

Within the Wireless Electronics thrust of the PRC, we believe needs for improvements in wireless components come in a few categories: those of the evolutionary type, where gradual improvements will happen as a result of engineering, those of the revolutionary type, where paradigm shifts in approaching the problem are necessary, and regulatory type, where the rules must be changed to allow an alternative approach to the problem. In collaboration with industrial partners and PRC thruts we are focused upon both revolutionary and evolutionary improvements for present and future applications between 1 and 100 GHz. Ongoing research projects include the investigation of RF/microwave packaging , interconnects and low cost active packaging approaches for high performance, highly integrated, low-cost wireless systems. In addition, with our industrial partners we are establishing a strategic focus for the wireless electronics packaging and the PRC single level integrated module (SLIM) concept.

Examples of Recent Results

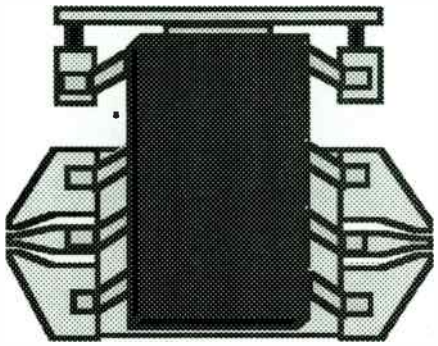

Fig. 1 Application of surface mount SSOP packages to greater than 10 GHz.

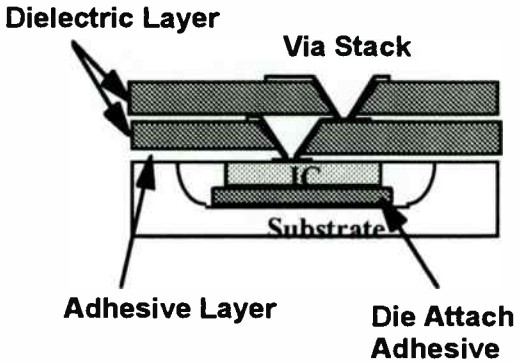

Fig. 2: Investigation of multi-layer, microwave interconnect layers.

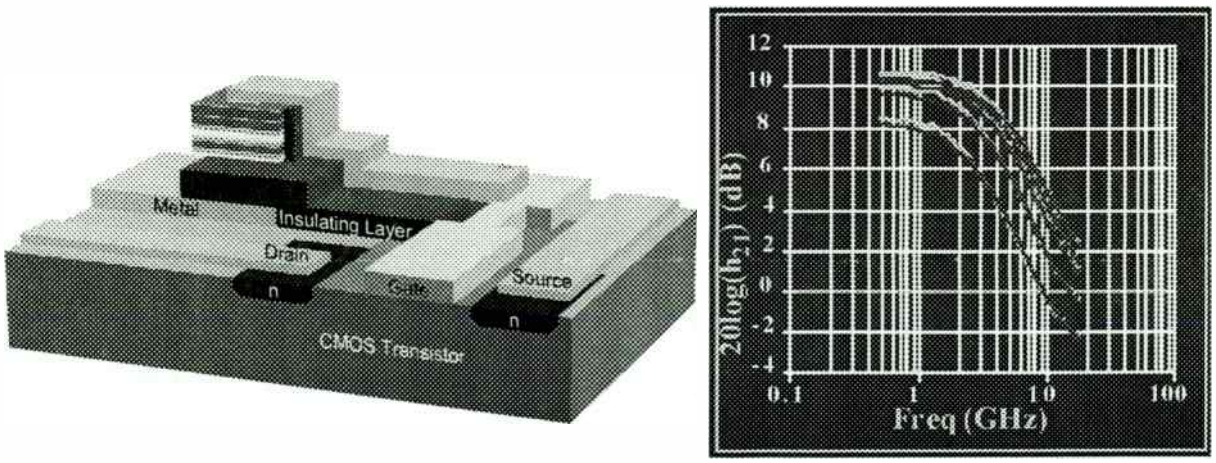

Fig. 3: Example of Active Packaging Concept for Direct Integration of Wireless ICs.

SATELLITE COMMUNICATIONS

Satellite Communications

Session Chairperson: Tim A. Williams,
Wireless Access (Santa Clara, CA)

Digital Maps and Satellite Imagery: Database Mapping Solutions for Cellular Network Design

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Accurate digital mapping information (clutter/morphology, elevation data, building height data, image maps) is fundamental to cellular systems planning. Traditionally, regions without a strong national mapping agency (virtually all economically developing countries, including China and most of southeast Asia) have little to offer in the way of accurate maps. Domestically, maps from the U.S. Geological Survey are an excellent source of elevation data for large scale areas, but poor in terms of timeliness and detail. (The average U.S.G.S. map is 25 years old.) Satellite imagery, aerial photography, and updated digital maps offer better solutions for mapping cells. Maps are the basis for a range of network activities from RF planning to marketing, including developing more predictable coverage maps with digital imagery and identifying interferences with morphology databases to optimize frequency allocation.

With higher quality maps, the engineering processes used to plan, design, survey, build, and install cellular networks become more efficient and accurate. This ultimately leads to site optimization, savings for operators, and improved service to customers. To be competitive, operators should be aware of the variety of commercial and government mapping databases available and their attributes.

This presentation (25 minutes) will include:

- An overview of mapping for cellular system planning to design
- Availability and accuracy of the numerous mapping sources (satellite imagery, aerial photography, existing maps)
- Digital mapping for RF engineering, including building height databases and ground-cover databases

Digital Maps and Satellite Imagery

Database Mapping Solutions for Cellular Network Design

SPOT Image Corporation

Agenda

- Overview of mapping for cellular system planning design
- Availability and accuracy of the numerous mapping sources
- Digital mapping for RF engineering

Cellular System Design Mapping

- Three steps of design
  - Initial build out
  - Optimization
  - Expansion
- Every step in wireless system design requires a map

RF Engineering Digital Mapping

- Digital Elevation Models
- Land Use, Clutter and Morphology
- Linear Networks
- Building Height Databases
- Orthoimage

Mapping Sources Availability and Accuracy

- Paper maps
- Satellite imagery
- Aerial photography

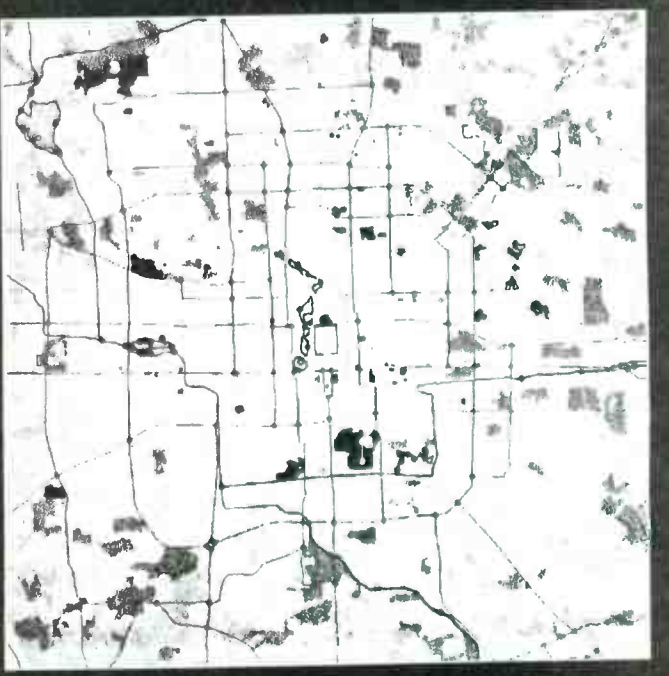
SPOT Image Corporation

Conclusion

- Accurate and up to date maps critical for succesful RF design
- Use of Satellite and aerial photography offer alternate solution to paper maps
- Propogation affected by elevation and morphology
- Accurate modeling avoids overbuilding a system

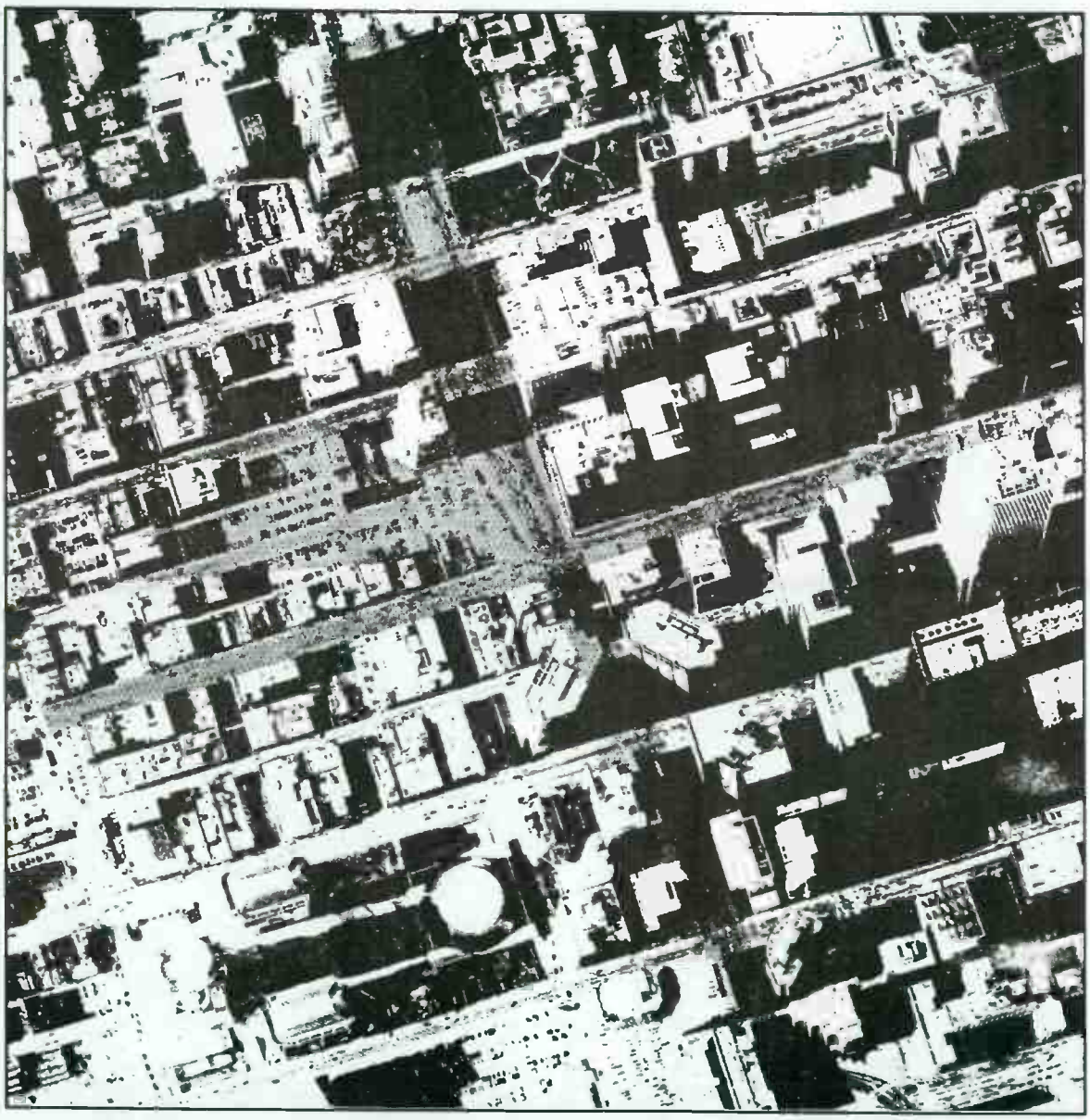
Telecommunications

- Market analysis
- Site selection
- Wave propagation analysis
- Network design and engineering
- Network maintenance and expansion



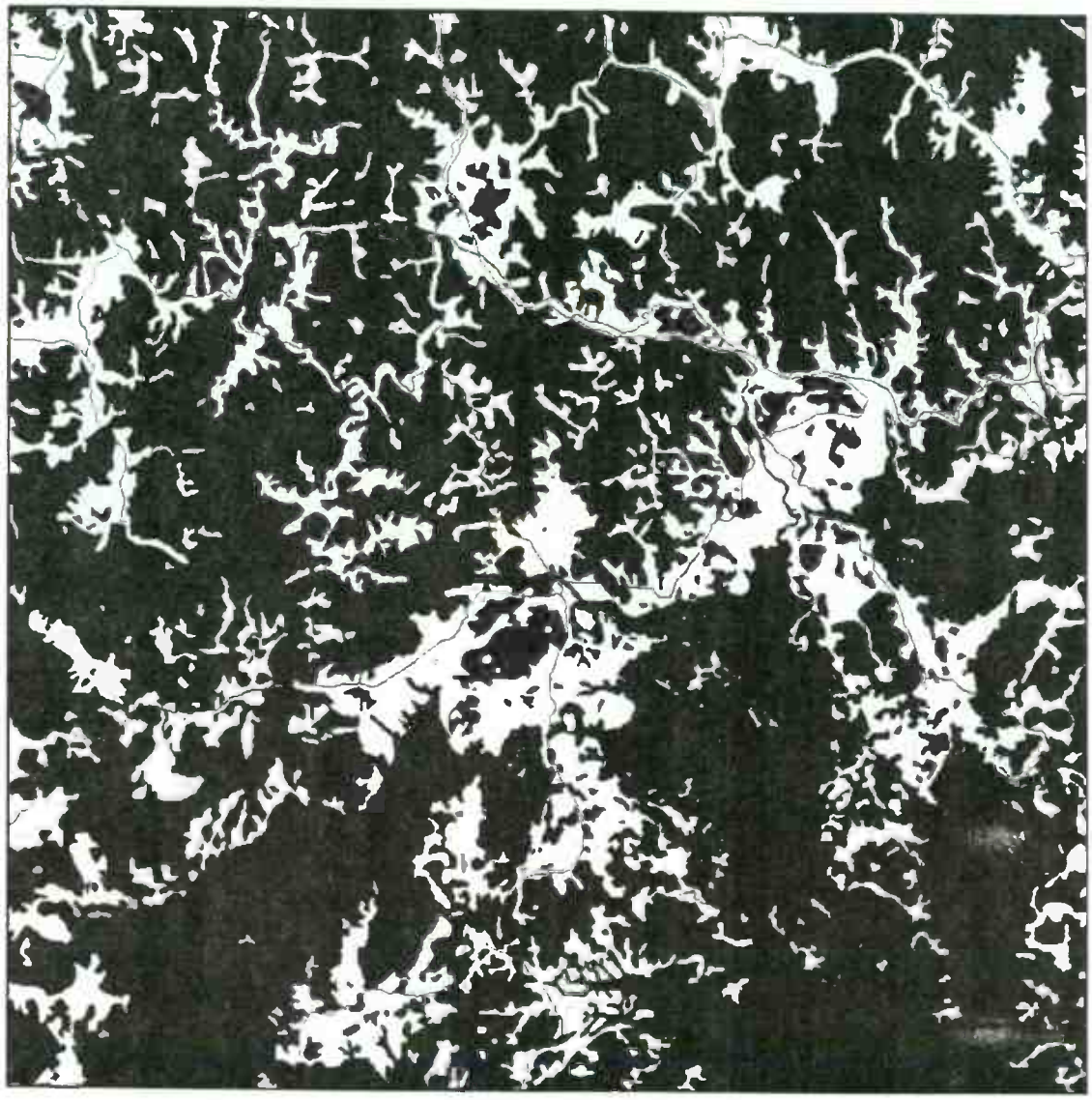
Beijing, China Clutter/Morphology

Ortho-Image Line of Site
Toronto, Canada



A 400-meter line of site for a base station antenna positioned 10 meters above ground is represented in green. With the ortho-image in the background, obstacles to the line of site and interference areas within the cell served by the base station can be identified.

5-Class Linear Network
(with clutter database in background)
Southern Coast, South Korea



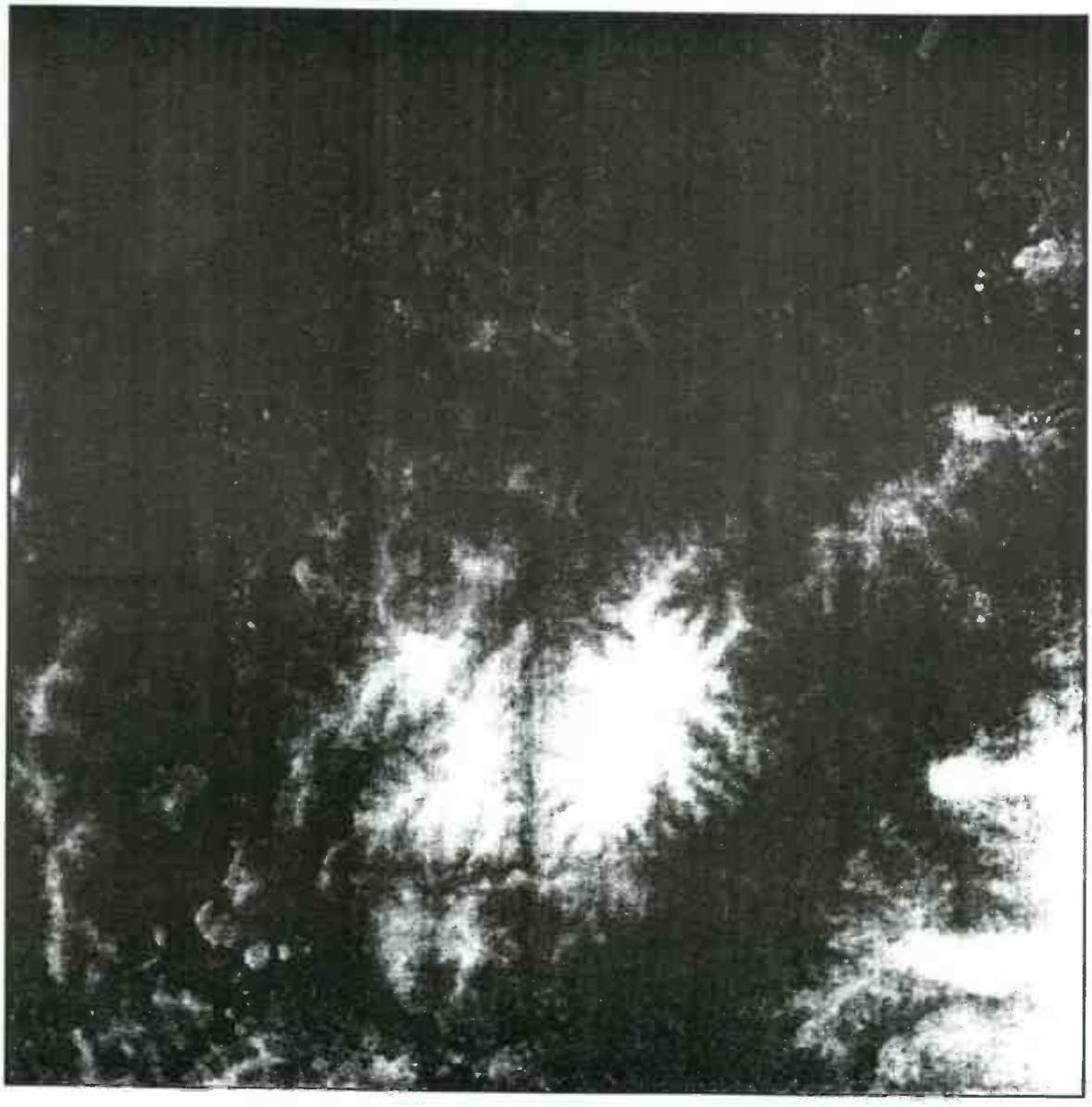
Color Legend

- Highways
- Railroads*
- Roads*
- Rivers and Lakes*
- Coastlines

This vector database represents the transportation infrastructure and natural linear features of an 80km x 80km coastal area near Pusan (South Korea). The most current and accurate maps are used to derive the linear network.

*These features do not exist in this sample area.

SPOT / ISTAR DTM
Seoul, South Korea



This digital terrain model (DTM) of Seoul and the mountains to the south correspond to the SPOT ortho-image. The DTM, created from SPOT stereo imagery, is comprised of elevation data representing Seoul's topography and has a spatial resolution of 20 meters.

12-Class Clutter
Seoul, South Korea

Color Legend

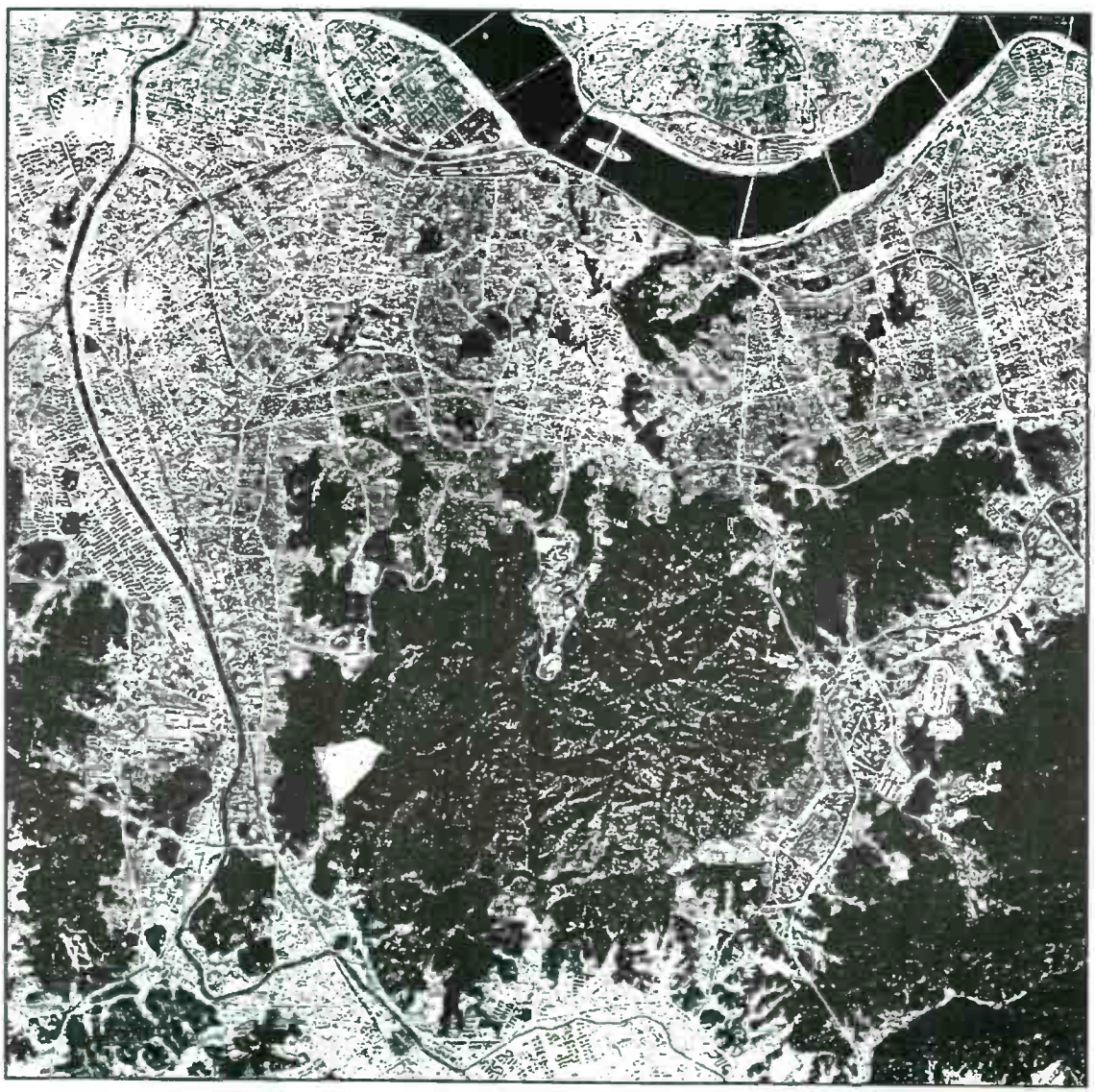
Open	Urban-Open	Urban with 60m+ Buildings	Residential
Forest	Urban-Dense	Urban-Medium Dense	Industrial
Inland Water	Urban-Parks	Villages	Sea/Ocean

In this clutter database, the natural and built-up features of Seoul have been classified into 12 classes, each of which has a distinct impact on wave propagation.

5-Class Linear Network

(with SPOT ortho-image in background)

Seoul, South Korea



Highways Railroads Rivers and Lakes Roads Coastlines*

The transportation infrastructure and natural linear features of Seoul are represented in a vector database that can be easily displayed with or without the SPOT ortho-image as a backdrop (as shown here). The most current and accurate imagery and maps are used to derive the linear network.

*This feature does not exist in this sample area.

Distributed Microprocessor Control of MPEG2 Satellite Receiver

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Abstract

In spite of the delays in availability of digital video and other broadband DTH services, new and high capacity satellite networks are currently under deployment. This paper presents set-top box developed for 54MHz wide Ku band satellite delivery systems with coherent QPSK modulation / demodulation with total bit rate of 90Mbit/s and aggregate data rate of 54 Mbit/s which is able to provide 8 high quality video-audio programs per transponder.

Our satellite receiver is based on C-Cube CL9110 MPEG2 transport demultiplexer & CL9100 MPEG2 video decoder. Total control of set-top box is done by Motorola MC68306 32bit CISC microcontroller as a host processor, while QPSK front end *Network Interface Module (NIM)* is controlled by 8-bit microcontroller, (Philips 80C51FB), *Conditional Access Module (CAM)* is under control of local 8bit microcontroller (SGS ST90).Then actual transport parsing and video decoding is done by 32bit RISC cores & audio decoding is performed by DSP. For *Call Back Channel* for *Pay-Per-View* applications we u se 2400bit/s telephone modem build around Intel 80C96 RISC like 16 bit core. Finally, for infra-red control of the set-top box we use 8bit ROM based microcontroller (Motorola 6805C4). Host microcontroller takes care about synchronization to all *distributed local processors* and executes dedicated algorithms for PCR processing, A/V synchronization, closed caption data extraction and insertion into color decoder (Brooktree Bt9104) and extraction of program specific services like asynchronous data from separate PES stream.

This paper outlines main hardware functional building blocks and basic software applications for process synchronization in multitasking environment.

Key Words

QPSK demodulation, smart card based conditional access, extraction of closed caption data from user data field of picture layer, extraction of async data from PES stream, A/V synchronization, PCR processing.

Wireless '97
Fifth Wireless International Symposium

Slide #1

Distributed Microprocessor Control of MPEG2 Satellite Receiver

WIRELESS '97

Tee-Comm Electronics, Inc.

Microwaves & RF

Slide #2

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Direct Broadcast Satellite Systems

as new and fast growing telecomunication industry combine advanced compression, modulation and error correction techniques to enable low cost but reliable operation under difficult environmental and noisy channel conditions and, what's even more important in the consumer applications, brings new types of educational and entertainment services as:

- Few hundred channels.
- Video-on-demand.
- Interactive television.
- High-rate data service.
- Digital ad insertion.
- Video telephony.
- Satellite news gathering.
- Impulse pay-per-view.
- Electronic TV guide and animation's.
- Possibility for gambling-on-demand.

Unlike many technological advances that fail to catch on with the public or attract or deliver these new services lead toward convergence of Interactive Computing, Newspapers, Television and High-Speed Networks. All of this multimedia services has been predicted (ref1. - ref3). It was a matter of video-audio compression / decompression theory and VLSI integrated circuits technology in last 10 years which enables practical development and deployment of home entertainment products in the reasonably low cost (below $500). Another reason for digital set top box revolution is effective satellite transponder usage.

If we compare DBS and older analog satellite services, when signal conditions are good with high SNR, DBS system outperforms any analog TVRO with laser disc picture quality and CD equivalent audio. But, when signal conditions are poor, primarily due to rain, lower SNR compromise error correction capability & error concealment capability of MPEG2 algorithms and system typically exhibits macroblock based video artifacts or loss of audio. This phenomenon is equivalent to 'snow' on picture of analog systems, but it is more severe.

In spite of the early deployment of DSS closed system established Hughes with Direct TV and USSB as two program distributors, newer DVB *Digital Video Broadcasting* networks like EchoStar or more recent ***AlphaStar*** digital video TV services are based on open, non-proprietary standards, first established in Europe. This standard specifies and defines performance requirements among vendors of DVB compatible transmit and receive equipment

In this paper major functional building blocks of MPEG2 digital set top box are described. In first section, short overview of MPEG2 transport stream is given. Second section describes main layers in the satellite communication system: presentation, transport and physical. Third part gives very detail study of superheterodyne QPSK receiver with some notes regarding newer direct conversion technology for *NIM (Network Interface Module)* design. Fourth and last part of this paper shows organization of channel memory of satellite receiver, typical MPEG2 PSI and DVB SI table parsing and process of channel change in the environment of three CISC, three dedicated RISC and one dedicated DSP processor used in set-top.

Part 1: MPEG2 Streams

After video, audio & data compression and encoding has been done output of encoder is in a form of pure elementary stream form. ISO/IEC 13818-1 standard specifies 3 basic layers:

- Compression layer with *Elementary Streams*
- System layer with *Packetized Elementary Streams*
- Multiplex-wide layer with *Transport or Program Streams.*

MPEG Elementary Streams are supported by decoding and presentation time stamps (DTS & PTS). They are included in a PES header and are retrieved by related audio / video decoders. Usually, PES packets are much larger than transport packets and they may form PES streams. In that case they contain ESCR - Elementary Stream Clock Reference and Elementary Stream Rate fields. PES header also may contains a number of flags opening up a broad range of optional fields. Always PES packets made up of Elementary Streams form a program channel with a common (same) timebase and are intended to be used in a form of Program Streams intended for multimedia applications on CD-ROM and Transport Streams for environments with significant errors. Transport Stream System Layer is divided into Transport Packet Layer for so called multiplex wide operations and individual Elementary Streams (PES packet layer for stream specific operations). Second layer is Transport Stream Compression Layer for audio and video decoders.

Transport packets with 188 bytes in length begin with 32 bit prefix. Prefix contains one synch byte (47H), 13 bit long packet ID (PID) and optional adaptation field which may carries sample of 27MHz encoder clock (Program Clock Reference or PCR) and a group of flags indicating private data or MPEG2 Program Specific Information tables MPEG2 defines four PSI tables:

- *Program Association Table (PAT).*
- *Program Map Table (PMT).*
- *Network Information Table (NIT).*
- *Conditional Access Table (CAT).*

Part 2: Multi Layer Approach

Typical satellite uplink system provides:

- ***Presentation Network Layer.***
- ***Transport Network Layer.***
- ***Physical Network Layer.***

Coordination of three layers on the set-top site provides ***Multilayer Control Software.***

Presentation Network Layer for video decoding is fully compliant with MPEG2 Main Level @ Main Profile. Supported video rates are from 1 to 12 Mbit/s with automatic 3:2 pull - down detection for 24Hz film video. Encoder can generate or skip B frames and may have various length of Group Of Pictures (GOP). It also supports a few resolution levels. Audio encoder supports ISO / IEC 13818-3 MPEG2 standard for Layers 1,2 audio compression from 32 - 384 Kbit/s bit rates. In a transport stream we could have up to 6 audio streams per each video stream (multilingual channels). Audio / Video synchronization is done by means of MPEG2 time-stamp mechanism or by streams alignment.

Block diagram of our satellite receiver at Fig. 3 shows a few separate building block:

- *Motorola 68306 32 - bit CISC microcontroller* with 16 bit data bus and 16 MBytes address space. For device drivers we use 4Mbit OTP (one time programmable) memory organized as 256K x 16 (Atmel 27C4096). This memory stores fixed part of application software. Receiver's channel memory, conditional access system software and GUI interface is stored in 4Mbit flash memory organized as 256K x 16 (INTEL, AMD or SGS Thomson memory).
- *9600 bit/s full duplex, multidrop serial link to QPSK receiver* for issuing control messages for frequency, symbol rate and Viterbi rate setup. Internal uart A of 68306 MCU is used and it can operate as remote diagnostic serial port.
- *9600 bit/s full duplex serial link to front panel controller* organized around Motorola 68HC05C4 8 bit MCU. This module is used as scanning and decoding IRED remote and front panel key controller. Also it refreshes 4 digits LED display.

Slide #3

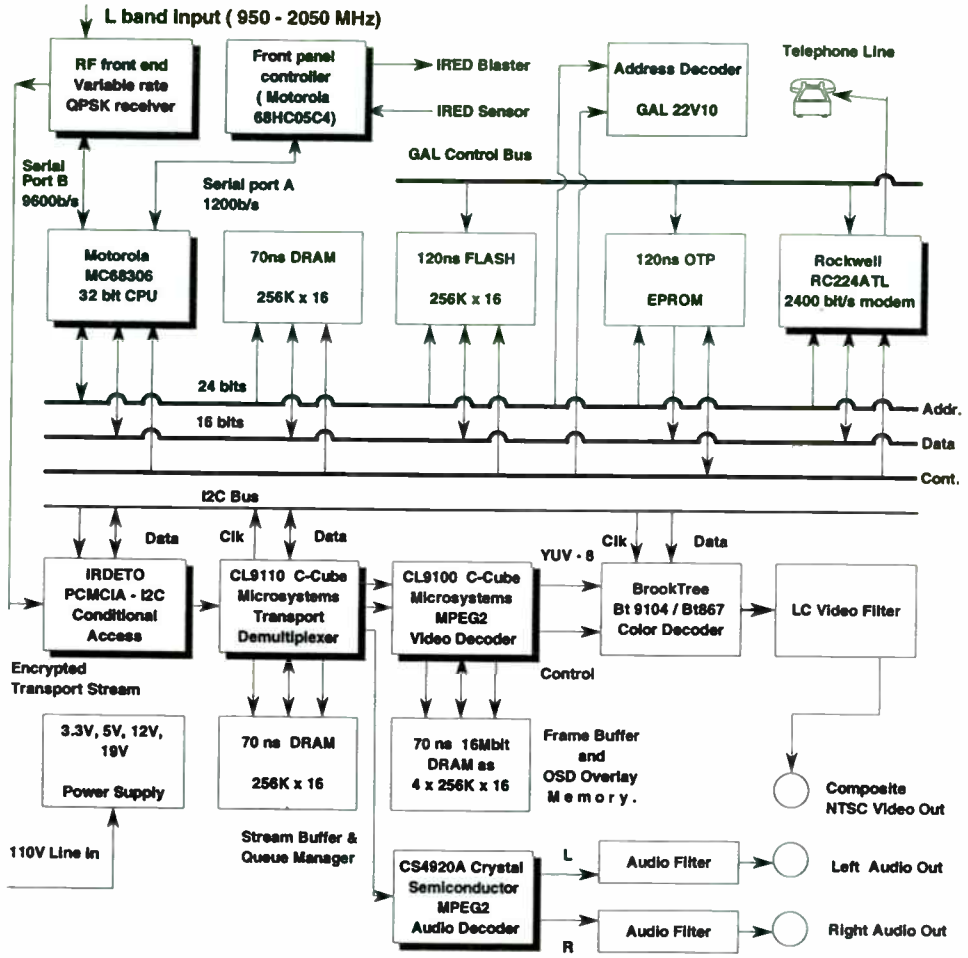

Fig.3 Block diagram of MPEG2 satellite receiver

- MPEG2 subsystem consists of C-Cube's CL9110 transport demultiplexer, CL9100 video decoder, Crystal Semiconductor CS4920A audio decoder and Brooktree Bt867 color decoder (video encoder).

- *I²C serial link* integrated in CL9110 is used for initialization of Bt9104 color decoder and for audio decoder microcode downloading.

- *Rockwell ATL224 2400 bps telephone modem* is used as upstream link to remote subscriber management center for PPV applications.

- *Conditional access system* is based on IRDETO EURO-I descrambler chip. Modified ACCESS BUS ™ control channel is used for message exchange between host CPU and ST-9 MCU embedded in CAM (conditional access module).

As the block diagram shows, another types of front-end descramblers like Philips SAA7206 or Sony CXD 1954 can be used in a similar way, where CAM is placed between QPSK or QAM NIM receiver and transport demultiplexer.

Acquisition of ECM and EMM messages has to be done by transport demultiplexer and host CPU. Another possible location for descrambler device is at descrambler port of CL9110 and DVCOM or VLSI device could be used. Decryption of control messages in a CAM is done by ISO-7816 smart card. Also, working key for descrambler is retrieved from smart card at approximately every 10 seconds. IPPV - Impulse Pay Per View records are stored in a smart card and once per month are retrieved from the card for the billing purpose. By using RSA or DES encryption / decryption, smart card based access system usually offers:

* Peer Entity Authentication
* Data Origin Authentication
* Access Control and Audit
* Confidentiality
* Integrity and Non Repudiation
* Access Key Management
* Screen Blackout Control
* IPPV Management
* Region Blackout
* Parental Control and Home Shopping
* Macrovision Control
* Pre-View and Event Recording

- *Analog active LC video and RC audio filters* to RCA back panel connectors for external audio / video home theater system.

Closed captioning and teletext is supported by means of VBI information data extracted from the input NTSC / PAL signal at the encoder and transported in a User Data Field of Video Picture Layer (2 bytes per frame). At the set-top box side this information is extracted from CL9100 video decoder chip on interrupt base per frame. It is *inserted locally* in IRD (integrated receiver decoder) by using YUV - PAL/NTSC video encoder IC which supports closed captioning at line 21.

On-Screen-Displays (OSD) for multilingual bitmapped graphics, graphical overlays or program provider logos are supported with graphical overlay feature of CL9100 video decoder chip. Also, this is the base of our TV-Guide.

Transport Network Layer is ISO 13818-1 MPEG2 System Layer. System multiplex can use *Statistical Multiplexing or Joint Bit Rate Control* to achieve constant overall bit rate in a group of video encoders and variable output bit rate at each individual video encoder within defined range. This feature is based on human eye characteristic that different complexity of video source could have variable bit rate (low in case of static pictures - opera or drama as example, and higher in case of dynamic pictures - sport events or action movies) and still achieve very good visual or image quality. This changes in the video bit rate could be done dynamically per frame and increase compression efficiency up to 20%, or in a very simple form dynamically per program by using DVB EIT-Event Information Table which contains category descriptor for each TV program.

Physical Network Layer applies QPSK satellite modulator and demodulator for very low bit error rate (less than 10^{-10}) over satellite link. This requires appropriate receive antenna size and error protection technique at the transmit side. Accepted satellite modulation system is QPSK with coherent demodulation due to power efficiency & robustness regarding transponder nonlinearity's. Satellite modems have variable Nyquist roll - off filtering, selectable between 20, 27, 35 and 40%.

Digital QPSK modulation is based on phase modulation of the carrier [see ref. 4, 5, 7] according to the data state. It is the most efficient modulation technique in terms of required minimum energy for a given bit error rate. Normalized S/N ratio is a quantity called Eb/No, where Eb is energy per bit and No is the spectral density of the noise. Energy per bit power times time i.e. carrier power C times period T. So we have that Eb/ No = C T / No equals C / T No. Because T is bit period (interval) then 1/T equals R or bit rate. So, one end ups with Eb / No as C / NoR = C / N because No R is noise power in a bit rate bandwidth. Phase modulation of the carrier exists as:

- *BPSK or Biphase Modulation* where we take each information bit and modulate the carrier into two phase states.
- *QPSK or Quadraphase Modulation* where every two data bits or dibits modulate the carrier into four states.

Before modulation we use concatenated error protection coding based on convolutional inner code (Viterbi) and [204, 188] Reed - Solomon outer code with framing and convolutional interleaving. This code will relate Reed Solomon (RS) code words directly to MPEG2 Transport Packets, so in case of uncorrectable but detected errors only one 188 bytes Transport Packet will be affected but flagged. Before RS encoding data is randomized according to IESS-309 standard for the low satellite interference and possible timing recovery. Viterbi code rates are 1/2, 2/3, 3/4 5/6 and 7/8.

Slide #4

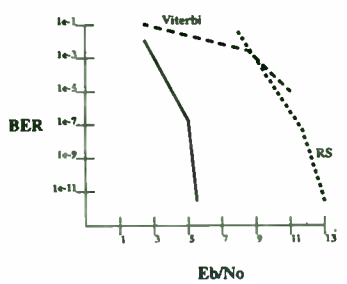

Fig. 4 Efficiency of concatenated error protection

Part 3: QPSK NIM design

Slide #5

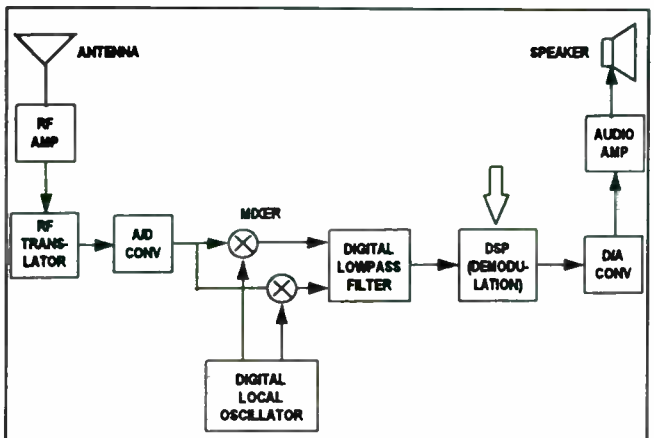

Fig. 5 Typical structure of digital receiver

Digital receiver, whose general structure is shown on Fig.5 can significantly reduce the DSP or dedicated ASIC requirements for systems which need to process signals within a certain frequency range of wideband signal. In the case of QPSK modulated signals transmitted over Ku / Xa band, first downconversion from 11/12 Ghz to L band (950 to 2050 MHz) occurs in LNB stage of satellite antenna. Due to routed cable distance between the antenna & the receiver of 50 or more feet RF stage and this first downconversion has three advantages:

- To provide significant critical gain in the RF stage for the -100 to -90dBm received signal with very low noise operating over the range of Eb/No values between 5 and 15.
- Translate signal to L band, where inexpensive circuits can tune and demodulate individual signals .
- To reach the set-top box with far less loss than in the 12GHz band through various RG-x coax cables (loss could be up to 30dB).

From L band signal can be downconverted to 0 (principle of direct conversion) or two low IF stage of 70MHz typically where all of subsequent mixing, filtering and demodulation are performed using DSP elements or ASICs. More often, tuning to the range of interest and extracting a narrow band signal from wide band signal could be done by DDS (direct frequency synthesizer) or NCO (numerically controlled oscillator). This is a viable alternative to analog based PLL technology due to:

- Higher output frequency resolution achieved by programming the amount of phase advance per sample (usually, 32 bit phase accumulator offers a tuning resolution far below 1Hz)
- In phase - continuous transition to the new frequency
- Very low output switching time limited by DDS processing delay (below 200ns), where the PLLs require more than 1ms due to feedback loop settling time and VCO response time.
- Wide tuning range over the full Nyquist range, where the PLLs are stable only within certain frequency range.
- Low phase noise better than that of its reference clock, where multiply phase noise of their frequency reference.

Typical disadvantage is still not high enough frequency range due to low sampling clock of up to 70MHz for signals up to 35MHz which may not be enough in the case of 54MHz wide transponders.

To zoom around narrowband signal, tunable mixer with decimated linear phase FIR low pass filter is used. By setting the decimation factor (usually in the range from 1 - 5000), output sample rate and bandwidth are controlled. This design is insensitive to aging, component tolerance, temperature variations or calibration. If all other subsequent processing at a lower sampling rate is done in DSP, this concept is known as ***software radio.***

But, it is worth to say that superheterodyne receivers are less sensitive to off channel signals near the receiver passband, & are also less sensitive to subharmonic signals. They also offer consistent performance across very large bandwidths. In most cases satellite antenna provides good selectivity and directivity and additional selectivity is achieved with preselection filters. Preamp in the antenna also improve signal sensitivity. If IF frequencies are in the range from 400 - 700MHz than less expensive SAW filters can be used. Typical structure of superhet receiver is shown on Figure 6. In many receivers two downconversion stages are used (known as ***double conversion***). Since all received frequencies are converted to the same IF frequency, demodulation is performed consistently at all frequencies, offering consistent performance over wide range of input frequencies.

Slide #6

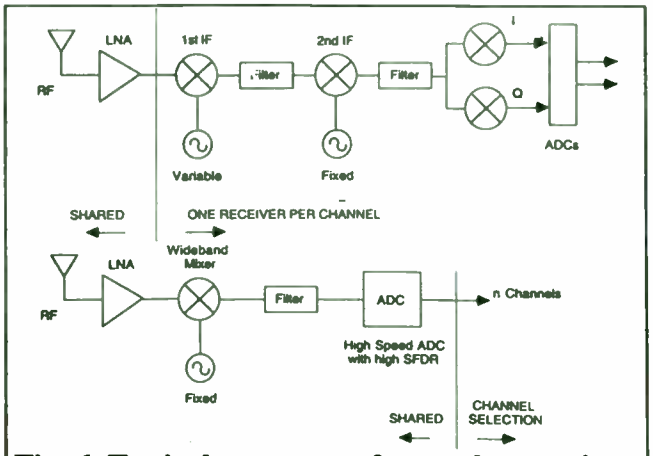

Fig. 6 Typical structure of superhet receiver

Highly-selective passive bandpass filter and sufficiently high IF frequency puts image channel in the stopband of the RF preselection filter. This filter also must have a wide dynamic range to be able to handle strong signals without distortion while being sensitive to weak signals just above the intrinsic noise level in the passband. For I/Q mixer, an error in quadrature of less than 1° is desired. Typical requirement is 0.5° phase error and 0.5dB amplitude error. Phase noise levels should be below -90 dBc/Hz at 100KHz offset from the carrier.

The system block diagram of QPSK receiver is shown at Figure 7. The downconverted Ku band input signal by the satellite dish LNB fits L band from 950 to 2050 MHz. L band local oscillator in the tuner synthesizes frequency band from 1.44 to 2.54 GHz by using crystal reference and PLL with the programmable divider (divide by N) in the feedback Due to the large tuning range (greater than twice the intermediate frequency of 480.5 MHz a tunable

Slide #7

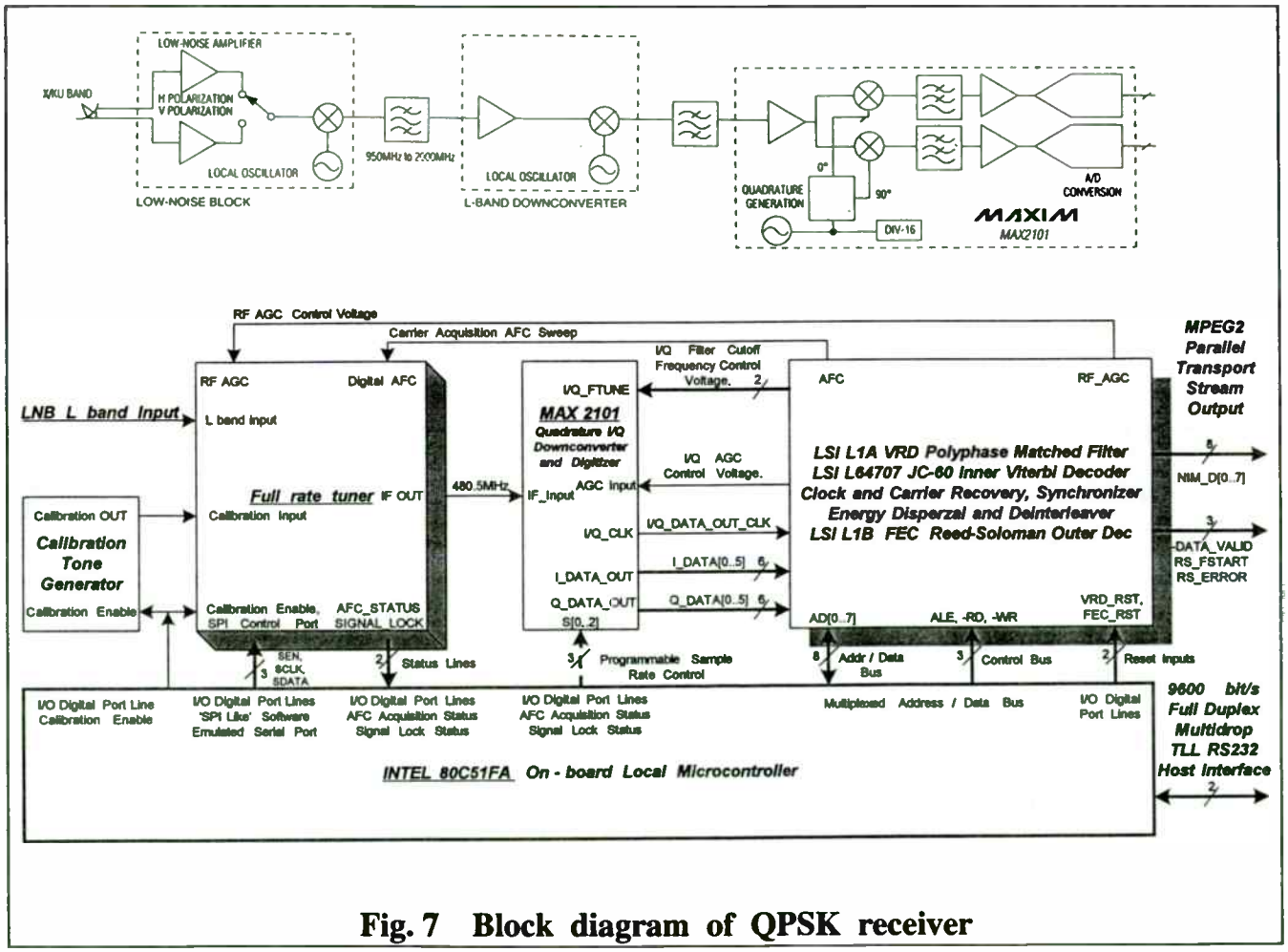

Fig. 7 Block diagram of QPSK receiver

image reject filter is used.

Filtering of 54 MHz satellite transponder signal is done with a surface acoustics wave filter (SAW). As a passband filter it has very narrow transition band and it also reject adjacent channel interference and limits the noise power. This filter has adequate bandwidth to pass the signal with the highest data rate.

Downconversion of 480.5 MHz IF signal in quadrature to baseband is done by fixed LO. Dual 60 Msym/s analog to digital A/D converters sample the quadrature baseband signals. Sample rate is controlled by 3 digital outputs from on board local microcontroller (INTEL 80C51FA).

Extrapolation and interpolation to 90 MHz signal is done in ASIC. Also antialiasing low pass filters for I and Q baseband signals have externally variable bandwidth from 10 - 30 MHz and are under CPU control. The digital downconverter performs decimation to twice the baud rate, removes the residual frequency offset & performs the root-raised cosine filtering. The coefficient set of polyphase root-raised cosine filters are downloadable, so PMF filters could have 20, 27, 35 and 40 % roll-off.

The symbol synchronizer closes quadrature data transition tracking loop. The demodulated I and Q data streams are passed to the deinterleaver before being decoded by the inner Viterbi decoder. Next step is Reed - Solomon outer decoding. Byte wide data with clock and RS error signaling are passed to C-CUBE CL9110 MPEG2 transport layer demultiplexer. Measured BER performance are shown at Fig. 8.

MAX2101 6-bit quadrature digitizer is used. It combines quadrature demodulation with A/D conversion on a single bipolar silicon die and solves the most complex interface when achieving ***RF-to-bits*** function (interface between quadrature demodulator and ADC). This portion of the signal path can introduce phase and amplitude errors that compromise back - end error correction. MAX2101 also includes an IF gain block (from 400 - 700 MHz) with at least 40dB of dynamic range, a VCO and prescaler necessary to generate an accurate LO frequency, fully integrated baseband anti-aliasing 5^{th} order Butterworth lowpass filters for I and Q channels with externally variable bandwidth from 10 to 30 MHz. Filters are realized using a gyrator

Slide #8

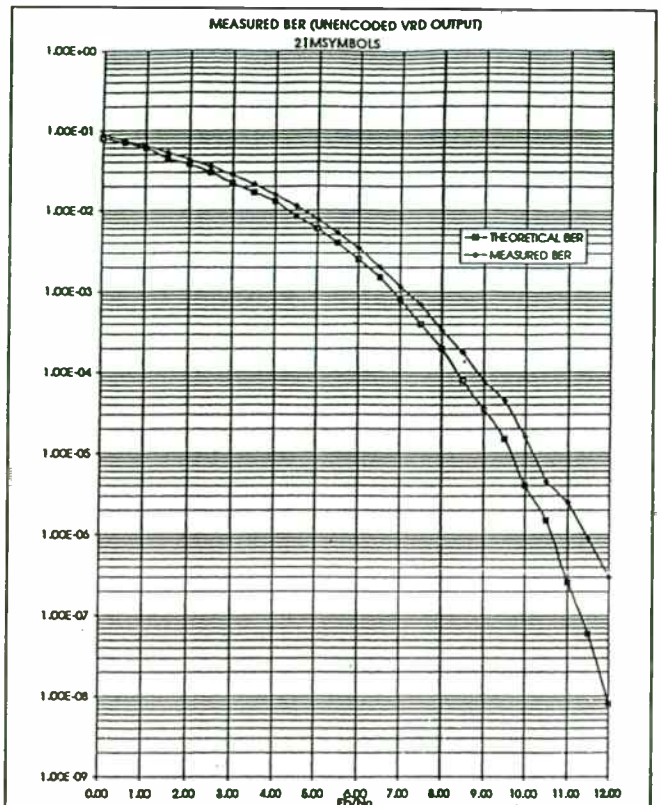

Fig 8. Implementation loss at 21 Msym/s

topology with temperature compensation circuits to achieve constant filter response over ambient temperature.

These filters are however one of the two common sources of offset (depending on a cut-off frequency) of the baseband signals applied to the ADC. Another source is possible LO coupling into the IF input where coupled LO mixed down to a DC value, which depends on the AGC setting. In any case, offset in the signal path can seriously affect and decrease useful dynamic range and offset variations between I and Q channels degrades overall receiver performance. A feedback controlled, offset-correction network based on differential base-band signal sampling and integration over large period of time (which depends on a minimum frequency of the baseband signal) extracts the offset signal. This technique eliminates all offset parts, independent of AGC setting, filter cut-off frequency or ambient temperature.

LO frequency is generated by a VCO controlled by a PLL. VCO is differential negative resistance amplifier with very high rejection of spurious signals and minimal second harmonic distortion.

Typical LO phase noise floor is -140 dBc/Hz and LO phase noise at 10KHz from carrier is -88dBc/Hz.. I/Q amplitude balance is 0.3dB and phase balance is1.5°.Low pass stopband attenuation at twice the carrier frequency is 28dB.

On board 80C51FA microcontroller provides control of I &Q channel baseband amplifier and I & Q channel filter cutoff frequency, and sets up three programmable sample rate control inputs. MAX2101 has AGC control input of the I/Q down-converter driven by subsequent automatic gain controller in the demodulator to provide proper amplitude at the input of the ADC and 40dB wide signal dynamic range. Demodulator provides:

- I/Q signals quadrature demodulation.
- AGC control for wide dynamic range.
- Carrier recovery.
- Clock recovery.
- Decoding and clock & data rate exchange.

Clock recovery circuit has digital phase detector , AFC and sigma-delta DAC with analog loop filter and provides the clock for MAX2101 ADC

Carrier feedback VCO on the demodulator provides a sweep function to find and control a exact frequency of the I/Q downconverter. This carrier synchronizer has phase error detector based upon Costas Loop, loop filter, phase lock detector, frequency sweep generator (synthesizer) and frequency lock detector and operates in two modes:

- ***Acquisition mode***, where sweep function of AFC executes until inner, clock acquisition, is achieved. Usually, this function compensates large frequency uncertainties (as +/-5MHhz of cheap LNBs). Sweep rate and range (sweep limits) are under control of local processor.

- ***Tracking mode*** takes its input from the timing error detector after achieved signal acquisition.

Viterbi timing and phase inputs are altered until the alignment detection. After that R-S circuit looks for sync byte of 0x47 (start of 204 bytes MPEG2 data packet with redundant code). Upon successful match deinterleaver, R-S decoder and the descrambler (V.35, IESS-308, IESS-309) are aligned and MPEG2 transport packets are clocked out from deinterleaver FIFO, through parallel bus, at maximum data rate of 7.5 Mbytes.

Although invented in the 1950's to simplify generation, transmission and reception of single sideband (SSB) signals, *direct conversion* receivers are not often used. Main advantage of direct conversion receiver are nonexistent images and simple IF filtering. However, quadrature errors in mixer stage and phase and amplitude errors between two IF paths may generate spurious beat components in baseband signal. IF errors vary with modulation frequency, where quadrature errors are constant within one channel, but they are channel dependent. Imperfect IF AGC tracking is additional source of errors.

Due to spectral efficiency, the transmitted signal in digital communications is SSB. Carrier is usually suppressed. It usually requires sharp RF filter with narrow transition band to suppers one sideband on the modulated carrier and pass the other. The unwanted sideband and LO leakage are always present spectral components. Distortion due to strong signals in the downconversion mixer will drop the sensitivity of the direct-conversion receiver DC offset in the baseband section, after mixing, may appear as larger than thermal or flicker noise in the downcoverted signal. The SNR is lower than in the high IF superhet receiver where only thermal noise exists. A small frequency error between the transmitter & receiver LO's will cause asymmetric downconversion around DC. To solve this problem, a very stable frequency reference or AFC is used. In spite of strict requirements for very linear mixer and rigorous DC or static offset elimination circuits, direct conversion receiver, shown at Fig. 9, offers less complex and inexpensive design.

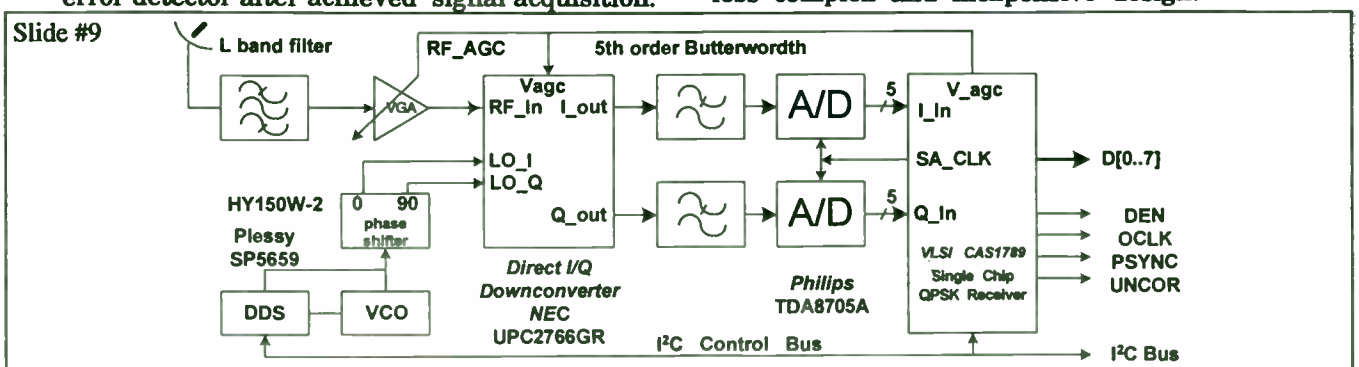

Fig. 9 Single chip, direct conversion QPSK receiver

Part 4: Distributed control

As we can see from Fig. 3 there are nine different types of CISC / RISC / DSP processors cooperating in asynchronous CPU system.

- ***Motorola MC68HC05C4*** eight bit local CPU executes its embedded program from 2Kbytes internal OTP EPROM. This CPU performs decoding of front panel keys and pulse train coming from infrared or UHF remote controller. Another task is to refresh 4 digits LED display. It is connected to host CPU by full duplex, CMOS 9600 bit/s asynchronous interface.

- ***Intel 80C51FA*** eight bit local CPU executes its embedded program from 16Kbytes internal OTP EPROM. This CPU performs all tuning and monitoring functions of QPSK receivers. It emulates SPI, low speed, serial communication to full rate tuner looking for signal acquisition and tracking status and signal lock. It also monitors complete baseband demodulation process of I/Q signals and estimates RSSI (received signal strength indicator) and SNR for the purpose of satellite antenna alignment by using 8-bit parallel bus. It supports variable message length, receive-acknowledge 9600 bit/s, full-duplex, multidrop, CMOS interface to host CPU.

- ***Thomson ST90*** eight bit local CPU used in the conditional access module (CAM) executes its embedded program from external 64KBytes EPROM. CAM provides access for particular network based applications, access particular types of program content for viewing and access system information for reading or modifying. In addition to this basic services its 'non-repudiation like' function which can prove origin and reception of the message supports pay-per-view, home shopping and true parental lockout PIN based applications. IRDETO's CAM module is suitable for encrypted MPEG2 transport packet payloads and non-encrypted MPEG2 packet headers and adaptation fields. CA_descriptor of the PMT is used for on-line identification of the scrambling algorithm. The broadcast encrypted content is decrypted using control word (CW). Cws are retrieved from ECM messages (entitlement control) which contain at least one (or multiple in the case of local area based blackout control) encrypted code words for actual program decryption. ST90 in CAM typically performs retrieval and syntax analyze of delivered ECMs. User public key is sent to smart card and working code word is delivered from the smart card. To prevent intercept of a control words (which are loaded into external descrambler) where is a concept of odd / even CWs, it is desirably to change CWs at very high frequency (every few seconds). Other ST90 tasks are retrieval of group keys and special ECM payload for flexible key management, loading of encrypted CWs to smart card, loading of clear Cws to descrambler, updating of preview program timers, application of RSA to user defined and supplied message encryption, PIN and password verification for program access and home shopping, etc.Typical key distribution chain is shown at Fig. 10. ST90 is connected to the host CPU via I^2C bus.

- ***Philips 80C852*** secure microcontroller used in the smart card supports code word delivery and RSA based encryption or decryption of user supplied messages. It is connected to local microcontroller by ISO 7816-3, 9600 bit/s half duplex asynchronous interface.

Slide # 10

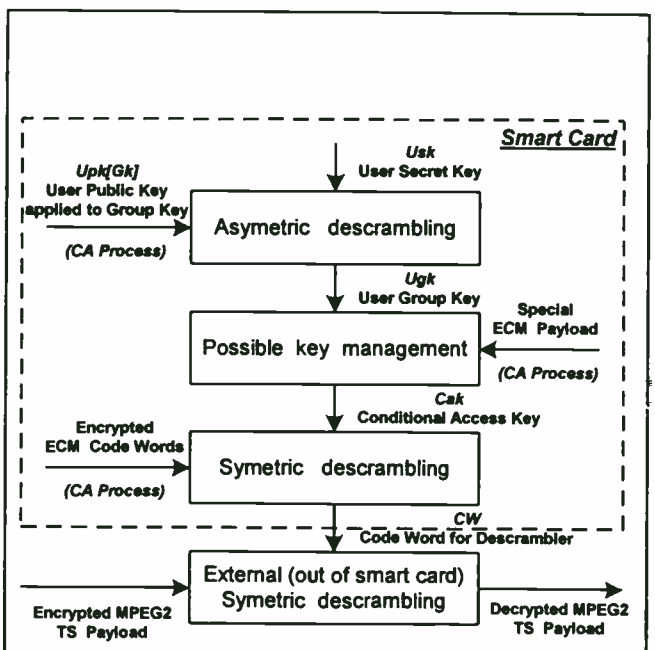

Fig. 10 Typical key distribution process

- ***Intel 80C96*** 16-bit 'RISC like' microcontroller used in Rockwell RC224ATL V22.bis telephone modem supports all modem functions for the purpose of actual pay-per-view billing. Host CPU sees this local CPU as '16C450 like' UART with 8 bit parallel bus interface (memory mapped peripheral).

- ***C-Cube CL9110*** is RISC CPU based transport demultiplexer interfaced to the host via parallel 16 bit data bus. RISC engine requires download of 1KByte microcode from the host CPU and performs next functions:

  1. PES and PSI MPEG-2 transport parsing.
  2. Stream demultiplexing and filtering.
  3. Control of external stream descrambler.
  4. PCR, video and audio PTS extraction.
  5. Video & audio channel data buffering.
  6. Extended channel rate buffering.
  7. Video decoder interface (to CL9100).
  8. Audio decoder interface (to CS4920A.
  9. HSO or High Speed Output interface for outputting transport packets based on PID matches in real time.
  10. I^2C interface for sending data and control messages to audio and color decoder.
  11. Program Clock Reference or PCR recovery by using PCR samples embedded in an MPEG2 transport packet.

- ***C-Cube CL9100*** RISC based MPEG2 video decoder provides interface to 16 Mbit DRAM used as video buffer and OSD overlay. Interface to host CPU is via 8 bit wide parallel host bus through CL9110 memory manager. Main tasks are:

  1. MPEG2 Main Level @ Main Profile decoding
  2. MPEG2 Main Level @ Simple Profile with dual prime mode.
  3. ISO/IEC 11172 & ISO/IEC 13818 compatible error detection and concealment.
  4. User-data field extraction (applied for closed captioning)
  5. Audio / Video synchronization using PTS embedded in an FIFO buffer or in an user-data field of picture header.
  6. Internal 90KHz System Time Clock (STC)
  7. Decodes MPEG1 & MPEG2 bitstreams up to CCIR 601 resolution of 720x480 @ 30Hz for NTSC or 720 x 576 @ 25Hz for PAL.
  8. Pan-and-scan for 16:9 video source.
  9. Supports conversion of 24Hz film rate.
  10. Supports MPEG2 high - level command interface (Reset, Play, Pause, Freeze, New Channel, Scan, Fast Forward, Single Step, Slow Motion and Block Write commands for simple operation).

- Horizontal resampling and vertical resampling

As a RISC based video decoder CL9100 requires a downloading of approximately 47 KBytes microcode for executing inputting, decoding and displaying processes. Inputting process transfers data from on-chip FIFO to the bitstream buffer in the DRAM MPEG2 decoding process includes VLC decoding, dequantization, inverse DCT, motion compensation error concealment and picture storing in the frame buffers. Displaying process sends data to the video interface in YUV format towards color decoder.

- ***Crystal Semiconductor CS4920A*** audio dec. is DSP based audio subsystem with integrated CD quality stereo Digital-to-Analog Converter, programmable PLL clock multiplier, an audio serial input port, SPI or I^2C serial control port and an AES-EBU - S/PDIF compatible digital audio transmitter. Interface to host CPU is via I^2C control port.

The CS4920 DSP core requires downloading of approximately 18KBytes microcode for MPEG layers 1 & 2 algorithms. The DSP engine has a 24-bit fixed point data path 4K words of program RAM and 2K words of data RAM. The execution unit has a 48-bit accumulator only. On-chip ALU typically reads instructions from program memory, operands from data memory and returns results back to data memory. For 44.1 KHz sample rate DSP engine has up to 16.9 MIPS. A/V sync could be achieved by:

1. Retrieving audio PTS from CS4920A to the host, comparing with internal STC and forcing video decoder to skip or repeat a video frame.

2. Video slaved to audio requires initialization of STC counters in audio and video decoders with a first PCR value from transport stream. At every frame (every second VSYNC interrupt) host has to read CS4920A internal PCR counter and write this value to video decoder PTS FIFO buffer. At the same time CS4920A will self - synchronize by using MPEG1 Packet Stream or MPEG2 PES.

Slide #11

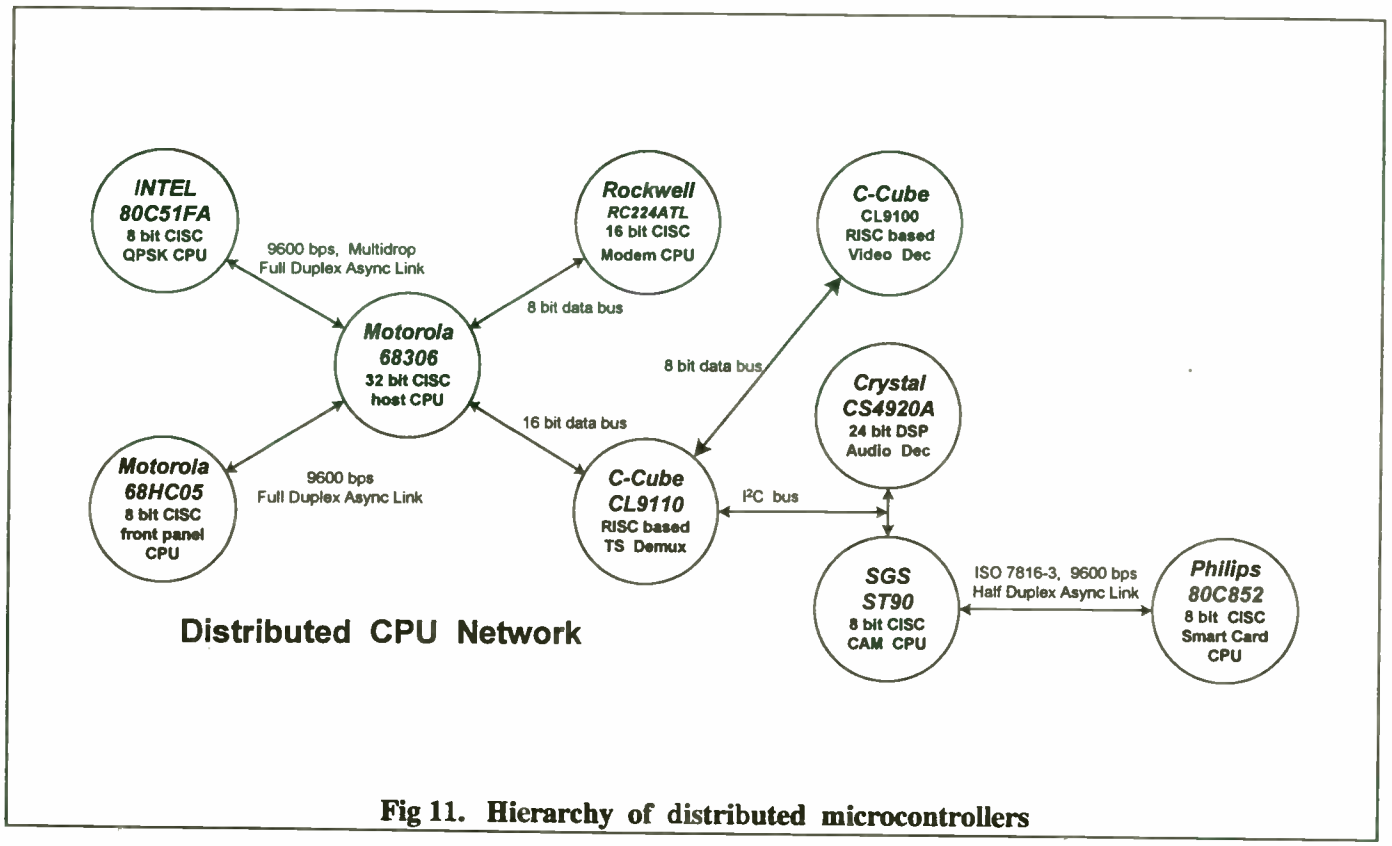

Fig 11. Hierarchy of distributed microcontrollers

As it is shown at Fig. 11, perhaps the most complex software layer is executing on host 68306 CPU, which has a role of main, synchronizing CPU among distributed processors. It executes complete channel change process, performs A/V process, OSD (screen - display) and volume control. After channel change, this processor monitors main conditions in satellite link by polling QPSK receiver at every one second and gathering information about current state of QPSK receiver (acquisition or tracking), received signal strength indicator (RSSI) or SNR values and number of corrected and uncorrected RS errors (from FEC decoder). If some of these, NIM related parameters are out of acceptable range, host CPU stops current program (decoding of audio and video) to prevent appearance of macroblock errors on decoded video display or possible loss of audio and keeps inquiring QPSK receiver. When satellite link is again established, host CPU executes channel change process to recover normal decoding of audio and video streams. During normal decoding conditions host CPU monitors proper operation of transport demultiplexer. Video decoding monitor is based on 5 seconds sliding window function which polls video decoder against number of repeated or skipped frames and number of decoded bytes. If any of these parameters is out of range, a portions of channel change (which includes flashing of video and audio buffers and executing New_Channel () MPEG2 command to resume decoding) is executed to correct decoding process.

Host CPU also performs interrupt driven A/V synchronization process (based on acquisition of video PTS values from CL9110 transport demux to initialize STC counters in video and audio decoders to the same timebase.

Other, table parsing related processes, are relevant to process TDT (Time and Date) Table for acquisition of date and time, important to event scheduling function of Electronic Program Guide, and version number check of NIT (Network Information) Table. If NIT process shows new version number, different to previously acquired and stored into flash memory version number, host CPU flags the end user with short OSD message at channel change, that new 'Channel Data' are available. At user request, 68306 starts off - line acquisition of all NITs at every transponder and builds channel memory of the satellite receiver.

Fig. 12 EPROM based boot loader

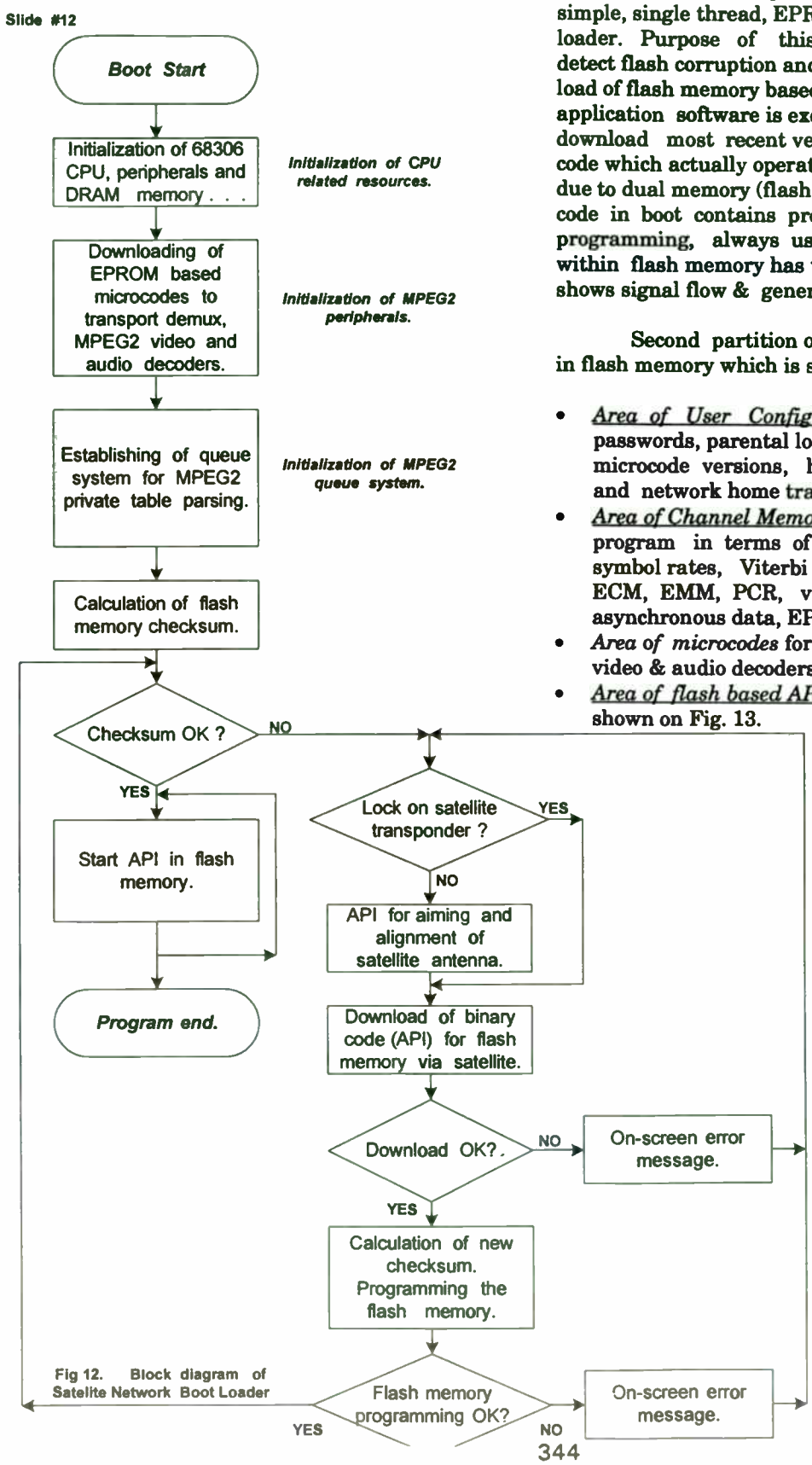

Fig 12. Block diagram of Satelite Network Boot Loader

In our satellite receiver, API software is segmented into two partitions. First partition is simple, single thread, EPROM or ROM based boot loader. Purpose of this software segment is to detect flash corruption and to force automatic download of flash memory based API software. Also, this application software is executed on user request to download most recent version of flash based API code which actually operates set-top receiver. Also, due to dual memory (flash & EPROM) architecture code in boot contains program for flash memory programming, always used when any of sectors within flash memory has to be changed. Figure 12. shows signal flow & general operation of boot code.

Second partition of API software is stored in flash memory which is segmented into four areas:

- *Area of User Configurable Parameters* (for passwords, parental lock options, software and microcode versions, hardware configurations and network home transponder parameters.
- *Area of Channel Memory* as description of every program in terms of transponder frequency, symbol rates, Viterbi rate and used PIDs for ECM, EMM, PCR, video, audio, low speed asynchronous data, EPG and other private data.
- *Area of microcodes* for transport demultiplexer, video & audio decoders for run-time application.
- *Area of flash based API code* whose structure is shown on Fig. 13.

Slide #13

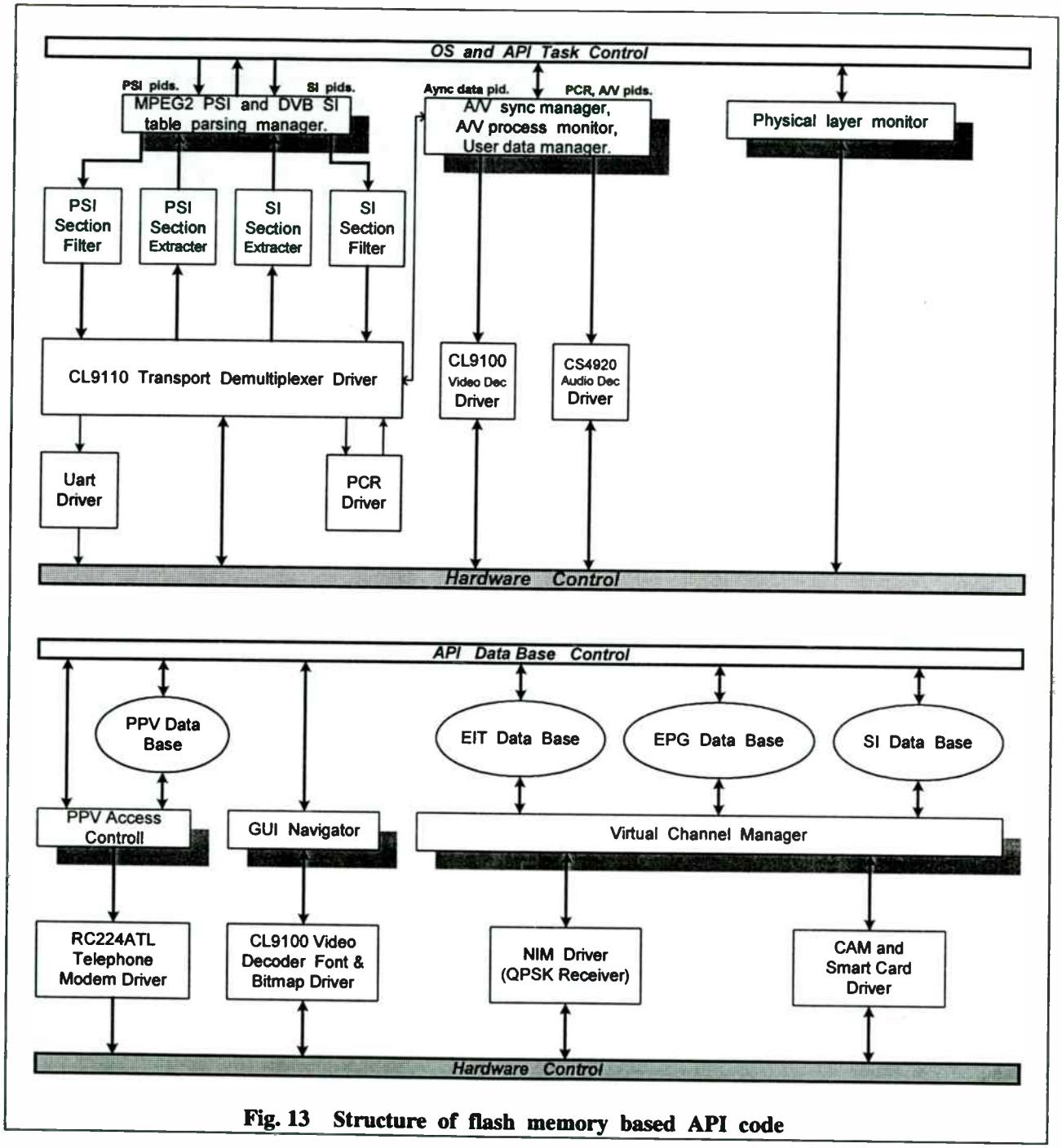

Fig. 13 Structure of flash memory based API code

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References:

Bernard Sklar
Digital Communications
Fundamentals and Applications, Prentice Hall '94

A Three IC Chipset for 2-Way Paging

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ABSTRACT

A highly integrated chipset for 2-way paging systems based a new double direct downconversion scheme for the ReFLEX™ series of 2-way paging protocols has been developed. The chipset consists of 3 ICs including a 900 MHz band bipolar front end transceiver IC, a mixed signal CMOS transceiver IC and a Digital Signal Processing CMOS IC. All channel select filtering has been integrated into the chipset and the architecture requires only a single crystal for generating all frequencies including local oscillators and digital clocks. The integrated AFC scheme extracts the incoming carrier and adjusts the oscillator frequency to within an accuracy of 0.5ppm. Also, the initial crystal oscillator frequency is tuned electronically at manufacturing through the use of the DACs eliminating assembly line hand tuning. The chipset is electronically switchable to either ReFLEX50 or ReFLEX25 modulation formats. An electronically tunable Butterworth pre-modulation filter is also integrated.

I. INTRODUCTION

Recently, nationwide 2-way paging networks based on the ReFLEX™ [1,2] family of protocols have become available to the public. These networks and the corresponding subscriber devices, allow the user to respond to incoming messages with custom replies or initiate custom messages directly from the pager. The responses can take the form of simple acknowledgment, canned response, multiple choice, or full custom using the subscriber unit's virtual keyboard. The pager can receive and send messages directly to other pagers, through its internet e-mail address, through a computer and modem, or through a live operator over the phone. Because of the acknowledgment feature and it's corresponding notification of the location of the pager to the network, network service providers are able to re-use wide area frequencies rather than having to inefficiently broadcast messages in all possible pager locations as in one-way paging. Because of this cost effective use of the spectrum, 2-way paging is expected to replace one-way paging for all wide area applications if the cost of subscriber units is kept to a small premium over 1-way units and the size of the units is comparable. Also, it is important that the subscriber units are capable of at least a months operation on a single AA battery. In order to accomplish these goals, a low power chipset which achieves a higher degree of integration than that available today is required within the subscriber units.

Current one-way and two-way paging architectures are dominated by traditional double downcoversion as shown in Fig. 1. This type of architecture achieves channel selection filtering through external crystal and ceramic filters which add size and expense to the implementation. Also, a sharp image reject filter is needed on the front end because of the low IF frequencies required for use of the crystal filter. Another disadvantage is that multiple crystals are

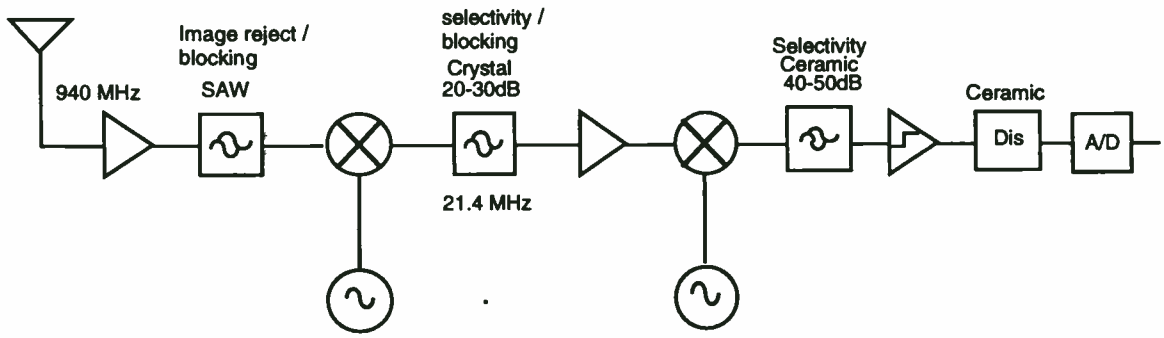
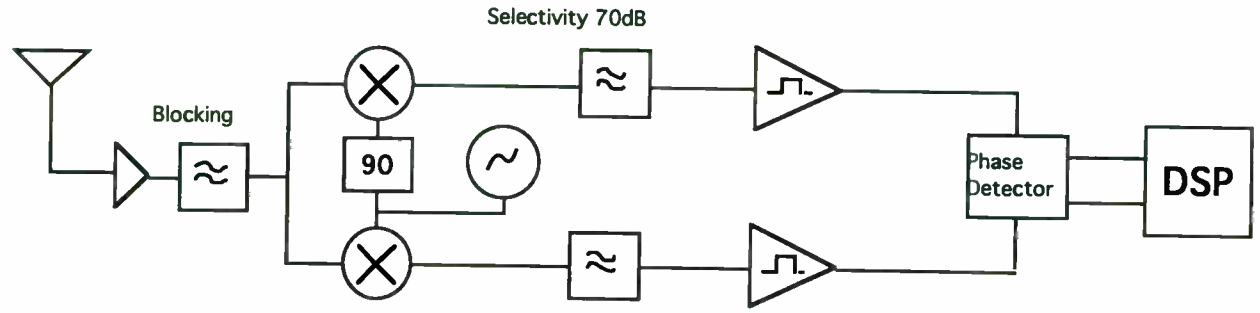
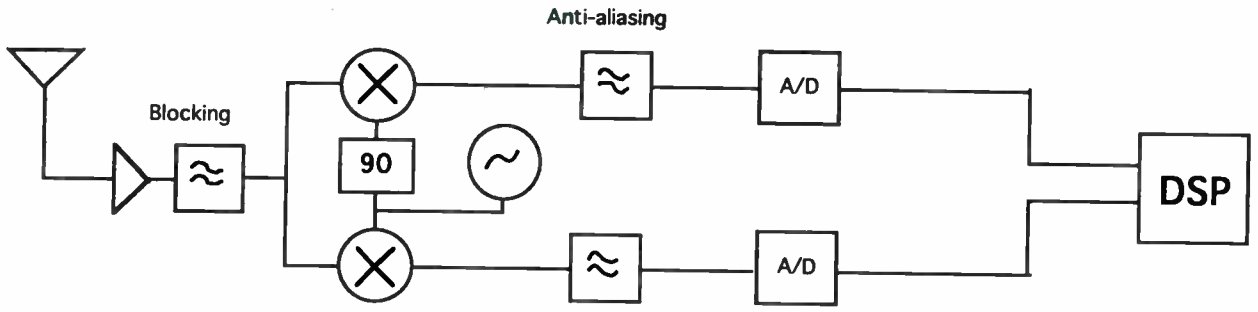


Figure 1. Traditional double downconversion paging architecture

ReFLEX™ is a trademark of Motorola Inc.



(a)



(b)

Figure 2. Traditional direct conversion architecture (a) with analog processing and (b) with digital processing

generally used to perform the downconversions adding additional size and expense. Double downcoversion does not lend itself very well to integration because the high center frequencies of the channel selection filters make integration of a low power, high dynamic range filter extremely difficult.

Figure 2 shows traditional direct conversion receiver architectures. Although this architecture relieves the need for external channel selectivity and image reject filters and thus lowers the cost and size over double downconversion, it is plagued by several other problems. First of all, since the RF and LO are at the same frequency, it is nearly impossible to keep a reasonable level of LO power from leaking out the antenna port. Even though this level may be low enough to meet government regulations, it is often high enough to interfere with nearby pagers which are operating under the same architecture. Any small difference between the LO frequency of the two interfering pagers will cause a beat frequency which will convert in band reducing the receiver sensitivity. Also, there is a propensity for the LO signal to be reflected back into the mixer and combine out of phase with the original LO. This phenomena combined with asymmetries in the I and Q mixer will cause a DC offset to occur at the output of the mixer. Removal of the DC offset can either be accomplished by the use of a high pass filter in Fig. 2a or using a digital scheme if the outputs from the I/Q mixer are converted to digital signals through the use of an A/D converter as in Fig. 2b. In the first approach, the high pass filter will cause loss of signal energy at the center ofthe band. This loss was tolerable in previous paging protocols which had wide FSK deviations and low symbol rates (+-4500 Hz deviations and 1200 or 2400 S/s symbol rates for POCSAG) but is intolerable in new paging protocols(800 and 2400 Hz FSK deviations with 3200 S/s symbol rate for ReFLEX™). In the case of digital extraction of the DC offset, the high dynamic range and high sampling rate of the A/D converter coupled with the digital signal processing required to extract and demodulate the signal necessitates power consumptions much too high for belt worn pagers operating from a single AA battery.

An architecture will be described here which combines the low cost and small size benefits of direct conversion with the performance advantages of double downconversion while achieving power consumption consistent with the paging paradigm.

II. SYSTEM ARCHITECTURE

The RF downconversion for the new architecture is shown in Fig. 3. It can be seen that in this architecture, the LO and RF are at different frequencies which eliminates the direct conversion interference. Leakage is significantly reduced because the LO is blocked by the image reject/blocking filter which is ineffective in filtering the in-band LO signal in a direct conversion receiver. Since the image is located well away from the RF at 3/5 RF, the blocking filter acts as an image reject filter and therefore no additional image filtering over that required for the direct conversion case is required. Power consumption is similar to the direct conversion case because one RF mixer is eliminated while a high frequency divider and IF I/Q mixer are added. The Cost is also nearly identical since both architectures are easily integrated and the additional Si area is insignificant.

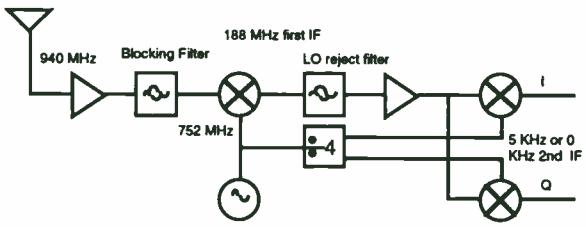


Fig. 3 Downconversion architecture of the RF front end

The DC offset is eliminated in one of two ways. In ReFLEX50 as shown in Fig. 4, there are four subchannels located within a 50 KHz narrowband PCS channel spaced at -15 KHz, -5 KHz, +5 KHz, and +15 KHz from the center of the channel. Each of these subchannels has 4 level FSK modulation with an approximate bandwidth of 8 kHz. The signal is downconverted to a zero IF so that subchannels FsA and FsD are overlapping and subchannels FsB and FsC are overlapping. There is then an unused portion of the channel between 0 and 1 KHz where no signal

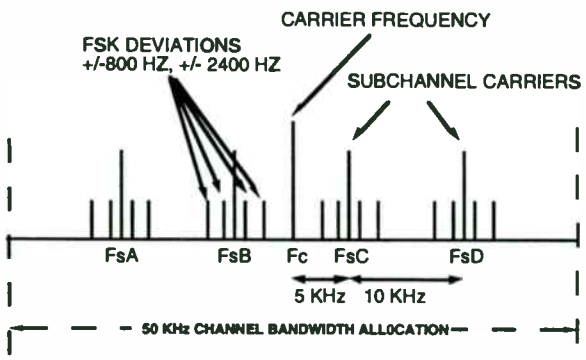


Fig. 4. ReFLEX50 channel modulation format

is present. Because of this, the I and Q outputs can simply be high pass filtered with no degradation to the signal. The resulting I and Q outputs contain 4 independent subchannels to be demodulated.

The situation is slightly different for ReFLEX™25 as shown in Fig. 5. In this case, the 4FSK signal energy is concentrated at the center of a 25 KHz narrowband PCS channel. In order to demodulate this signal and remove the DC offset, the LO frequency is adjusted to downconvert the signal to a 5 KHz second IF frequency. The DC offset can than again be removed by a simple high pass filter with a cutoff well below 1 KHz. The downconversion to a non-zero IF causes the formation of an image frequency at -5 KHz from the channel center. This frequency, however, falls in the channel dead space where there is no significant signal energy present and is rejected by the inherent image rejection of the I and Q mixers to a level of approximately 30 dBc.

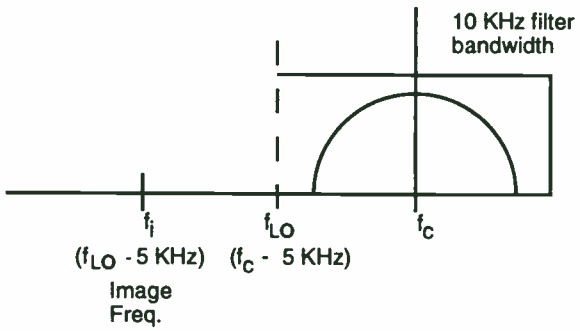


Fig. 5 Downconversion of a ReFLEX™25 signal

A block diagram of the system is shown in Fig. 6. The three ICs are the WR6010 bipolar RF transceiver IC, the WM6040 mixed signal demodulation IC, and the WB6050 digital signal processing IC. The additional ICs which are required to complete the system are a synthesizer, power amplifier, and microcontroller. All system frequencies are derived from a single oscillator located on the WM6040. This oscillator is electronically tuned at manufacturing from a crystal with a room temperature tolerance of 15ppm and temperature tolerance of 7.5ppm. An automatic frequency control algorithm which derives an accurate frequency from the received signal, tunes the oscillator to within 0.5ppm during operation. The only external filters in the architecture are the front end blocking filter, and an LO reject filter which requires only a single LC resonator. All of the channel select filtering is accomplished in the WM6040. Adjustable gain control is accomplished within the WM6040 and via

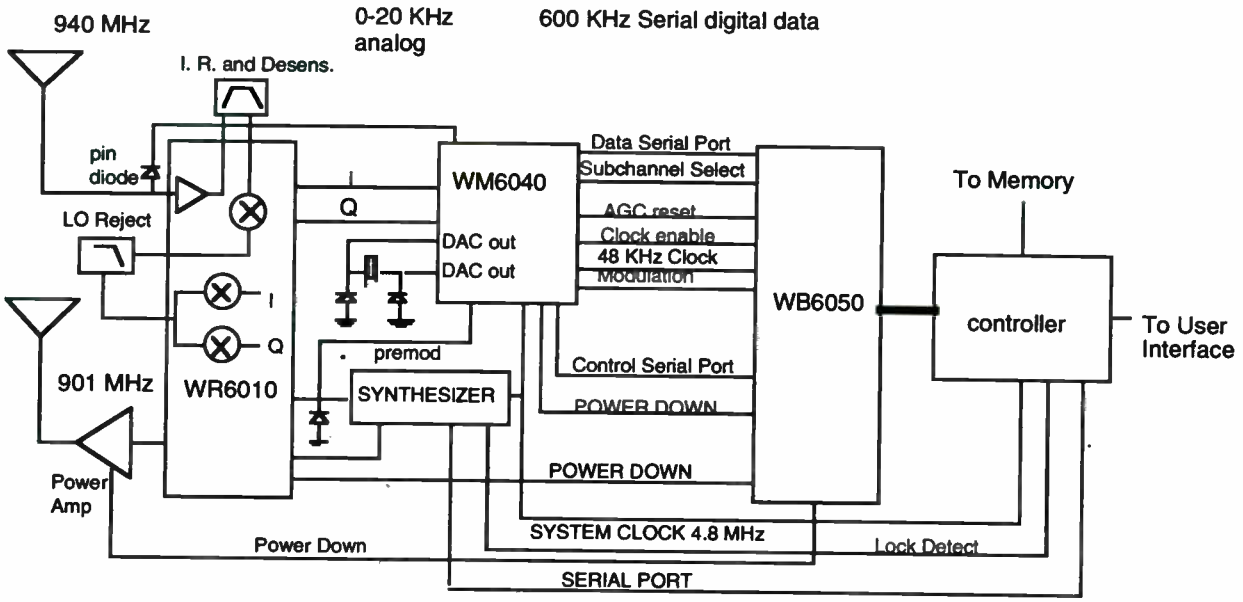


Fig. 6. Block diagram of the new system architecture.

a pin diode attenuator on the front end. The attenuator boosts the dynamic range by 15 - 30 dB depending on the attenuator configuration (shunt diode only or series shunt). An electronic switch adjusts the channel select filter bandwidths and selects the single channel ReFLEX™25 or multiple subchannel ReFLEX™50 format.

Transmit modulation is accomplished through DACs located on the WM6040. The deviation values are extracted at the time of manufacturing. DAC outputs are provided to drive both the RF VCO and the reference oscillator. By using a combination of modulation on both VCOs, there is no high or low frequency cutoff for the modulation rate.

Since the power consumption is dominated by power down current and receive mode current, the emphasis on low power design is in these two modes. Very little time is spent in transmit operation and during this time, the power consumption is dominated by the power amplifier. Therefore, power optimization on the transmit path is of much less importance.

III. WR6010

A block diagram of the Si bipolar WR6010 RF front end IC is shown in Fig. 7. The IC has been designed with the primary goal of minimizing power consumption. Three power down pins are included in order to separately control the receiver, transmit driver amplifier, and transmit VCO. The two power pins on the transmit side allow optimization of the power cycling to minimize frequency splatter due to frequency pulling on the VCO from the driver amp and power amp. The LNA input and output as well as the mixer input are single ended whereas the output of the first RF mixer and I/Q mixer are differential. The single ended structure of the LNA and mixer input simplifies the external matching required and reduces the power consumption. Matching for the LNA can be accomplished with a simple two element matching network at the input and output. The current consumption for the LNA is 1mA and the mixer current is 600µA.

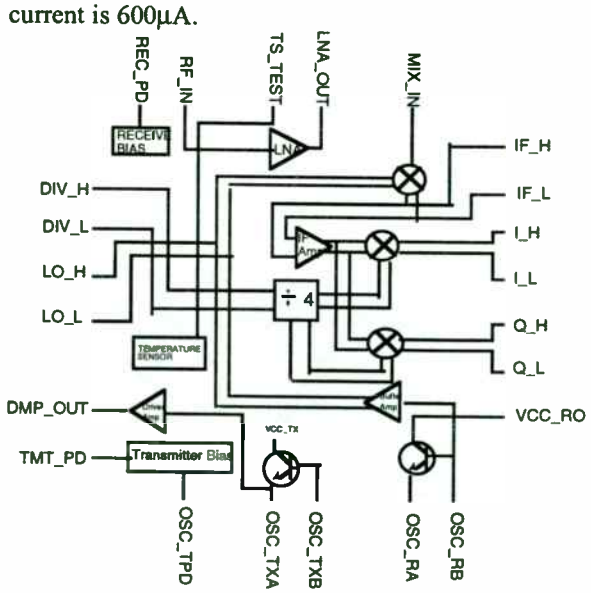


Fig. 7 WR6010 Block Diagram

Both receive and transmit VCO transistors are included on the IC. The use of different VCOs for receive and transmit allows them to be optimized for phase noise at their respective frequencies. Also, the transmit VCO can be run at higher current to match the more stringent phase noise specification on the transmit side. The transistor currents for the VCOs are controllable with external resistors. The receive VCO has a high impedance base tap to a buffer amplifier which amplifiers the signal to an output voltage amplitude of 150mV. An external LC resonator is used at this output to minimize current consumption in the buffer amplifier. This output is input to the divide by four which provides near perfect broadband quadrature LO signals for the I and Q mixer. Typical matching is within 0.5 degree. All of the receiver functions combined exclduding the VCO consume around 3.5 mA. The receiver VCO can typically be run in the 1.0-1.5mA range with acceptable performance.

The transmit VCO has a low impedance emitter tap to the driver amplifier. The driver amplifier has been designed to drive a 1 Watt power amplifier. In saturation, the output power is 3 to 6 dBm depending on the value of a fixed external resistor. Table 1 shows some typical measured parameters for the device. The voltage operation range is for the IC is 2.7-3.6V.

Table 1. Measured parameters from WR6010

Parameter	*Conditions*	*Typ. Value*	*Units*
LNA			
Gain	940Mhz, 3.0V	19	dB
NF	940Mhz, 3.0V	1.9	dB
P1dB	940Mhz, 3.0V	-30	dBm
I	3.0V	0.9	mA
RF mixer			
G	940Mhz, 3.0V	20	dBV
NF	940Mhz, 3.0V	10.5	dB
I/Q mixer			
Gain	188Mhz, 3.0V	16.5	dBV
I/Q Match			
Amp.	3.0V	0.35	%
Phase	3.0V	0.5	deg
Temp. Sens.			
Gain	-20C to +70C	2.1	mV/C
Linearity	-20C to +70C	0.4	%
Total Receive I	excludes VCO, 3.0V	3.5	mA
Power Down I	3.0V	1	µA
Driv. amp Psat	pin = -3 dBm, 3.0V	3-6	dBm

IV. WM6040

The WM6040 mixed signal CMOS IC block diagram is shown in Fig. 8. The outputs from the WR6010 are passed to the WM6040 where they are high pass filtered to remove the DC offset. The input low noise amplifier is designed to receive signals down to a level of 9 µV. The interspersed adjustable gain and filter sections yield a dynamic range of about 90 dB for the WM6040 and as much as 120 dB for the entire system including the front end attenuator. The bandwidth switchable front end continuous time filters provide a rejection of at least 65 dB to adjacent channel signals located at 25 KHz away for ReFLEX™25 and 50 KHz away for ReFLEX™50. These filters are electronically self-tuned to the correct bandwidth from the crystal oscillator reference frequency and therefore the bandwidth does not vary with process, temperature, or voltage.

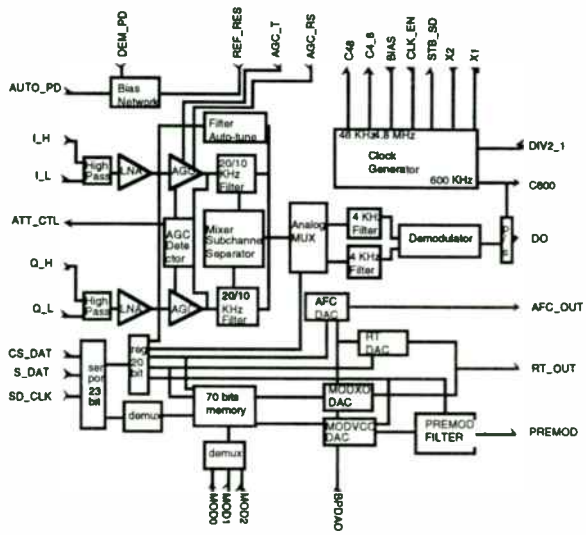


Fig. 8 WM6040 mixed signal CMOS IC

The attenuator driver circuit turns on when the input voltage exceeds 125mV forming a close loop system with the input PIN diode attenuator until the attenuator reaches its maximum value of 15-30 dB. After passing through the input gain and filtering section, the 4 subchannels in ReFLEX™50 are simultaneously downconverted to 0 IF in a third downconversion step. One of these channels is then selected by the analog multiplexer for further processing. In the ReFLEX™25 case, the signal is also downconverted to 0 IF and the multiplexer is locked into one position.

Following subchannel selection, the signal is further filtered to remove any adjacent subchannel signal and improve channel selectivity with 4.5 KHz

bandwidth switch capacitor filters. Switch capacitor filters are used because of the reduced dynamic range requirements in this portion of the signal path. The filtered signal passes through the demodulator which converts the 4 level FSK analog signal to a digital signal and extracts zero crossing information. That information is output at a rate of 600Khz to the serial port for transfer to the digital signal processing IC.

The IC also contains 4 DACs for oscillator control and transmit modulation generation. The RTDAC performs a room temperature adjust on the crystal oscillator to tune out initial crystal inaccuracies. The extracted value for the DAC is stored in non-volatile memory. The AFCDAC is calibrated during manufacturing with a series of measurements on the crystal oscillator. The measurement values are also stored in non-volatile memory. This DAC is used to control the crystal oscillator frequency to within 0.5ppm during operation. The MODXO DAC is used to impart modulation on the reference oscillator and the MODVCO DAC imparts modulation on the VCO. If the loop filter has a bandwidth less than the premod filter, there is no need to filter the MODXO output through the premod filter. Therefore, only the MODVCO DAC output is routed through the Premod filter. The values for the modulation deviations are extracted at manufacturing and stored in non-volatile memory. The values are loaded through the serial port. The second order Butterworth premod filter is a switch capacitor design and can be programmed through the serial port to a bandwidth of 3200 or 4800 Hz as required by the protocol.

The crystal oscillator is a low power design which consumes about 55 µA when operated at 9.6 Mhz or 40 µA when operated at 4.8 Mhz. There is a switchable output clock buffer provided on chip which will drive the microprocessor clock input at this frequency. This output driver is turned off during power down. A 48 KHz clock output driver is always powered on and is used by the WB6050 for all signal processing. The digital dividers necessary for this clock and the DACs are always operational resulting in a measured total power down current consumption around 110 µA. The voltage operation range is 2.7 to 3.6 V. Table 2 lists key measured performance data and specifications.

V. WB6050

A diagram of the WB6050 digital signal processing IC is shown in Fig. 9. The IC has been designed to perform all signal processing at clock rates of 60 KHz or less in order to minimize power consumption. The zero crossing information from the

Table 2. WM6040 measured data and specifications

Parameter	*Conditions*	*Typ. Value*	*Units*
Filter bandwidth			
ReFLEX25	3.0V, f=3dB	19	KHz
ReFLEX50	3.0V, f=3dB	9	KHz
Filter rejection			
ReFLEX25	Δf = 25 KHz	68	dB
ReFLEX50	Δf = 50 KHz	71	dB
Input frequency		0-20	KHz
FSK Deviations		200-6400	Hz
Symbol Rate		0-6400	Hz
Current			
Receiver on	3.0V	4.0	mA
Pow. down	9.8 Mhz ref.,	110	µA
Dynamic range	BER = 1/30	90	dB
Premod filter cutoff		3200, 4800	Hz
DAC ranges			
RT DAC			V
AFC DAC			V
MODXO DAC			V
MODVCO DAC			V
Xtal Oscillator freq.		4.8, 9.6	MHz

WM6040 is sent directly to the input of the WB6050 and passed through a post detection filter which counts and smoothes out the zero crossing indicators. The output from this block is a numerical representation of the frequency deviation. The timing recovery block extracts the data clock from the post detection filter output. The carrier frequency offset is

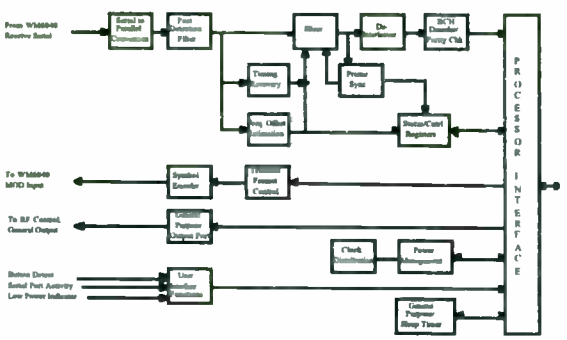


Fig. 9 Block diagram of the WB6050

also extracted from this output for use in the AFC algorithm to adjust the reference clock located on the WM6040. The slicer determines the raw bits.

With the raw bit output available, the pattern is compared with known patterns allowed by the ReFLEX™25 and ReFLEX™50 protocols to determine the location of the frame in the frame synchronization block. The signal is interleaved as specified by the protocol in order to smooth out the effects of fading on the signal. The 32 X 32 bit de-interleaver buffer performs the appropriate de-interleaving. The BCH decoder inputs 32 bit words of BCH encoded data from the de-interleaver buffer and outputs a 21 bit decoded data word. The BCH encoding allows for correction of up to 2 bit errors in each 21 bit data word.

The communication to the processor is through a bi-directional 8-bit parallel port. The microcontroller is normally asleep in order to minimize the power consumption. The microcontroller is awakened by the WB6050 in response to a programmed sleep value in the sleep timer (set by the microcontroller itself) or in response to an interrupt from the user interface module. The user interface module detects activity on user buttons, an external serial port, and a low voltage indicator.

The transmit symbol encoder can accommodate data rates of 800, 1600, 6400, and 9600 bps. The encoder allows for 5 deviations (4FSK + carrier) and controls the ramp sequence specified by the protocol. This data is output to the WM6040 modulation control pins

VI. SYSTEM PERFORMANCE

The system performance was verified with a system containing the WR6010, WM6040, and FPGA version of the WB6050. Table 3 shows sample results of BER testing. System raw BER (bypassing the de-interleaver and BCH decoder) was measured. The criterion for sensitivity was 1/30 bit error rate. Performance was measured over voltage ranges from 2.7 to 3.6V, temperature ranges from -20 to +70C and symbol rates of 1.6 and 3.2 Ks/S. In all cases, the sensitivity was within 2 dB of the numbers listed in Table 3. Selectivity was measured for ReFLEX™50 on the subchannel closest to the interferer at channel center to channel center difference of 50 KHz (the actual difference between the wanted channel and interferer was therefore 35 KHz). Selectivity was defined as the point at which the sensitivity degrades by 3 dB. The selectivity tone is defined as in [2].

Table 3. Measured 3 IC system parameters

Parameter	*Conditions*	*Typ. Value*	*Units*
Sensitivity			
ReFLEX™50	3.0V, 3.2Ks/S, 25C		
FSA		-124	dBm
FSB		-124.5	dBm
FSC		-125.5	dBm
FSD		-124.5	dBm
ReFLEX™25		-124	dBm
Selectivity			
ReFLEX™50	3.0V, 3.2Ks/S	67	dB
ReFLEX™25	3.0V, 3.2Ks/S	69.5	dB

VII. CONCLUSION

A low power three IC chipset for the ReFLEX™25 and ReFLEX™50 two way paging protocols has been developed. The chipset eliminates all external channel select filters and runs from a single crystal oscillator. All crystal oscillator tuning is accomplished electronically through hardware incorporated on the chipset. The only external ICs required to form a fully functional two way paging transceiver are an external synthesizer, power amplifier, and microprocessor. This chipset enables wireless IC portable device vendors to build extremely low cost, low power, and small size 2-way pagers and paging modules for use with narrowband PCS in a variety of applications including belt top pagers, PDAs, utility monitoring, vending machines, vehicle location, and PCMCIA card pagers.

References

[1] Motorola Inc., *ReFLEX™50 Protocol Specification Document*, Doc. RFL50-021194, Ver. 4.3a, Aug. 30, 1996.

[2] Motorola Inc., *ReFLEX™25 Protocol Specification Document*, Doc. RFL25LX-033195, Ver. 2.4, March 15, 1996.

[3] International Electrotechnical Commission, *Methods of measurement for radio equipment used in the mobile services, Part 6: Selective-calling and data equipment,* IEC 489-6,1987, p.13.

Automatic Satellite Identification for Consumer Analog Satellite Receivers

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Abstract

Nowadays market of analog satellite set-top boxes contains an increased number of various types of DTH home entertainment and professional satellite receivers, but only with a limited possibilities in C/Ku band *satellite antenna navigation.* Usually, installer has to find a few satellites (at least three) in pseudo-automatic mode by using infrared or UHF remote controller of satellite receiver to move the antenna and observe pattern on selected channel. This requires that particular video program is on. Later on, some of currently available receivers are able to calculate positions of other satellites by using longitude coordinates stored in EPROM or FLASH memories and known number of pulses from dish actuator between east and west limits of antenna. Even than, accuracy of calculated satellite positions is not very high, which is important in the case of Ku band antennas. Our ***Star * Trak 800,*** consumer satellite receiver, is able to automatically recognize some of about 44 North American C/Ku band satellites by adjusting audio circuits to 7.02 / 7.11 MHz on which some satellites carry Morse code. Later on, we digitize analog audio signal and execute *slide window real time sequence recognition* to recognize particular satellite. By using this method, our receiver is able to move the antenna from east to west limit, to find and to record maximums of signal strength on both polarities and on reverse dish motion to stop on peaked positions (where the satellites are), to listen the Morse code and to identify the satellite. In the group of 44 satellite, receiver is able to recognize 6 to 12 satellite, while the positions of others are calculated. The whole process usually takes about 20 min.

This paper outlines main hardware functional building blocks and basic software applications for signal processing and ***Automatic Satellite Identification (ASI™)*** by Morse code.

Key Words

Morse code signal processing, automatic gain control, A/D conversion, audio subcarriers, EPROM & SRAM memories, satellite and channel memories of receiver, EPROM look-up tables, CISC microcontroller.

Wireless '97
Fifth Wireless International Symposium

Slide #1

Automatic Satellite Identification for Consumer Analog Satellite Receivers

WIRELESS '97

Tee-Comm Electronics, Inc.

Microwaves & RF

Slide #2

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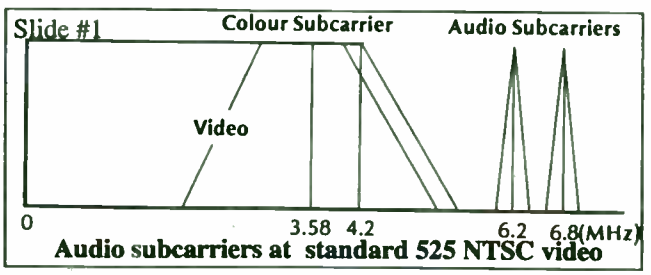
Abstract

Nowadays analog satellite receivers for DTH consumer home entertainment and professional applications have only a limited possibilities in C/ Ku band *self satellite antenna navigation*. Usually, installer has to find a few satellites (at least three) operating receiver in the pseudo-automatic mode by using its infrared or UHF remote controller to move the antenna and watch current video on the selected program. This implies that used transponder and selected channel is on. Later on, some of currently available receivers are able to calculate positions of other satellites by using longitude coordinates stored in internal EPROM or FLASH memories and known number of pulses from antenna actuator between east and west limits. Even than, accuracy of calculated satellite positions is not very high, which is important in the case of Ku band.

Audio signals are relayed within transponder bandwidth. The received satellite TV signal is takes frequencies from 0-10MHz, where video occupies 4.6MHz (NTSC) other remaining space can be used for audio channels (sound that matches the video signal) or for special purposes (for example Morse code), as it is shown on Fig.1.



Audio subcarriers at standard 525 NTSC video

Introduction

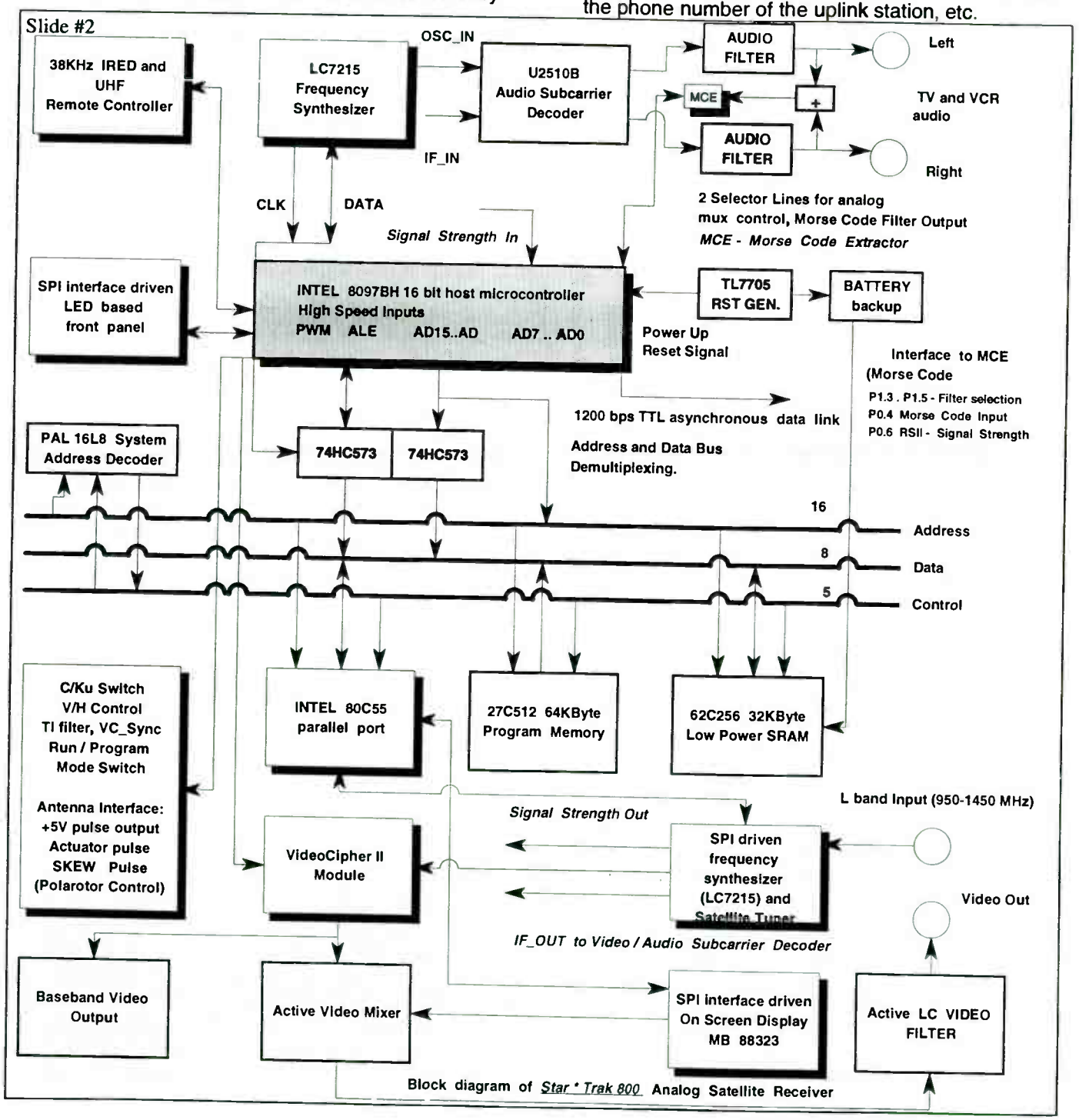
Tee-Comm's ***Star * Trak 800***, fully integrated satellite receiver - decoder (IRD) for consumer DTH application is able to automatically recognize some of about 44 North American C/Ku band satellites by adjusting audio circuits to 7.02 / 7.11 MHz on which some satellites carry Morse code. After digitizing analog audio signal and executing *slide window real time sequence recognition*, host processor of set-top identifies particular satellite. By using this method, our receiver is able to move the antenna from east to west limit, to find and to record maximums of signal strength on both polarities and on reverse motion to stop on peaked positions (where the satellites are) and to identify some of the existing satellites.

This paper outlines main digital hardware functional building blocks and basic software layers, structures and applications for signal processing and ***Automatic Satellite Identification (ASI ™)*** by Morse Code.

First section of the paper gives a simplified block diagram of satellite receiver with very special emphasize on analog audio preprocessing circuit known as *Morse code Extractor (MCE)* for rectifying audio signal. Second part presents main software layers and structures for ASI application. Third part gives a list of existing satellites and one method for position estimation of non-identified satellites based on positions of known, already recognized satellites at ASI process. Finally, last section presents ASI algorithm via few flow diagrams.

Part 1: Structure of the receiver

On April 13, 1990, the FCC issued a ruling which required all video uplink stations to transmit an identification signal. All broadband satellite video earth stations are under obligation to transmit a sub-carrier with ***Automatic Transmitter Identification System (ATIS)*** in a form of audio subcarrier. Primary purpose and application of ATIS signal is to resolve interference problems and to find proper positions of satellites at orbital slots. FCC ruled that before March 1, 1991, uplink earth stations were required to start broadcasting ATIS. In many instances this signal is a ***Morse Code (CW)*** identifier which contains the origin of programming, known call sign (letter E with the string of at least 4 numbers, special identity code, the phone number of the uplink station, etc.



Block diagram of *Star * Trak 800* Analog Satellite Receiver

Slide #3

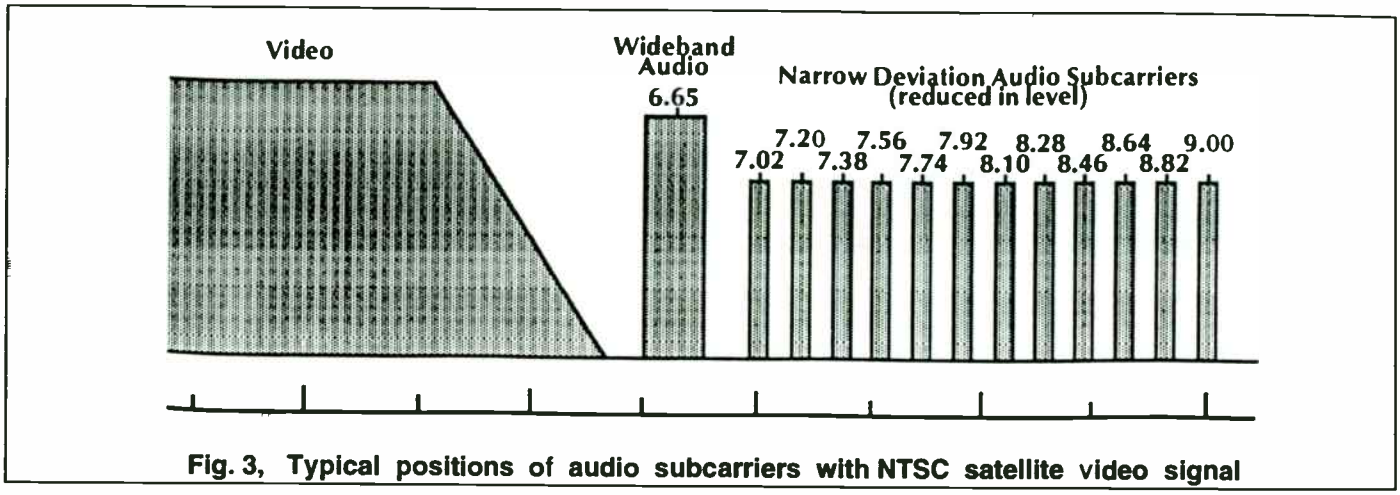


Fig. 3, Typical positions of audio subcarriers with NTSC satellite video signal

The ATIS message is usually carried on a 7.11MHz audio subcarrier, in the case of B_MAC and Video Cypher II encryption systems, ATIS carrier is on 8.3MHz. Typical message speed is 25 words per minute.

In a standard 525 NTSC satellite TV signal, video occupies ranges from zero to 4.2MHz with the color subcarrier falling at 3.58MHz. The remaining bandwidth from 5 to 8.5MHz, with 75 microseconds pre-emphasis for noise reduction, is used for audio carriers. Some of them may not be necessarily related with the actual video signal.. These non-video related audio subcarriers have a more narrow bandwidth and lower power levels than standard 6.2 / 6.8 MHz subcarriers. Stereo sound is often modulated onto 5.58 and 5.76 MHz subcarriers. Audio content can be transmitted totally separate from the video signal in a systems known as single channel per carrier - SCPC *(FM satellite radio).* Figure 3. shows relation between wideband audio and narrow multi-audio subcarriers.

Block diagram of *Star*Trak ST-800* satellite receiver is shown at Fig. 2.There are three separated software emulated 'SPI like' buses in a system. One is used for control of LC7215 frequency synthesizer for to generate a programmable frequency to U2510 audio subcarrier decoder. Another is used for similar application at satellite tuner. Third is used to control SIPO (serial-in parallel-out) registers for front panel LED display and PISO (parallel-in serial-out) register for scanning of the front panel's keys. Host micro-controller is 16-bit INTEL 8097BH used in 8-bit bus interface mode. Run time application code is stored in 64KBytes EPROM. From total 64KBytes address space of host CPU, about 56 KBytes are assigned for application program, 2 KBytes are used for system RAM, 2 KBytes are allocated for I/O page and 4 KBytes for 32 KBytes low power SRAM with battery backup and paging control from system PAL 16L8 which also performs address decoding. This SRAM contains 600 channels receiver memory and table description of satellites. In system, parallel I/O ports extension is done via INTEL 80C55 parallel bus I/O device.

Decoding of incoming IRED and UHF remote pulse train is done by host CPU. Receiver's SRAM memory-to-memory transfer is available via 19.2 Kbit/s RS-232 asynchronous serial port.

Figure 4. shows a structure of audio pre-processing circuit known as *Morse Code Extractor - MCE*. This circuit depends on implemented software algorithm for processing of pulse train which forms a CW message. In our case, 'preprocessed' analog signal in a form of pulse train is converted to a digital domain via 10 bit internal analog-to-digital converter, already available and integrated to host CPU. One can use input capture method for measurements of dot and dash intervals via internal CPU timer. This method would need a Schmidth trigger for pulse edge forming at the output of proposed circuit.

First section shows a 4^{th} order bandpass filter composed of two biquads. Input to a filter circuit is from main audio baseband output, after audio processing being done from 7.11MHz carrier. Filters are realized as active RC network, where central frequency is under CPU control via 4052 multiplexer. At the end, hard limiter is used for pulse extraction.

Slide #4

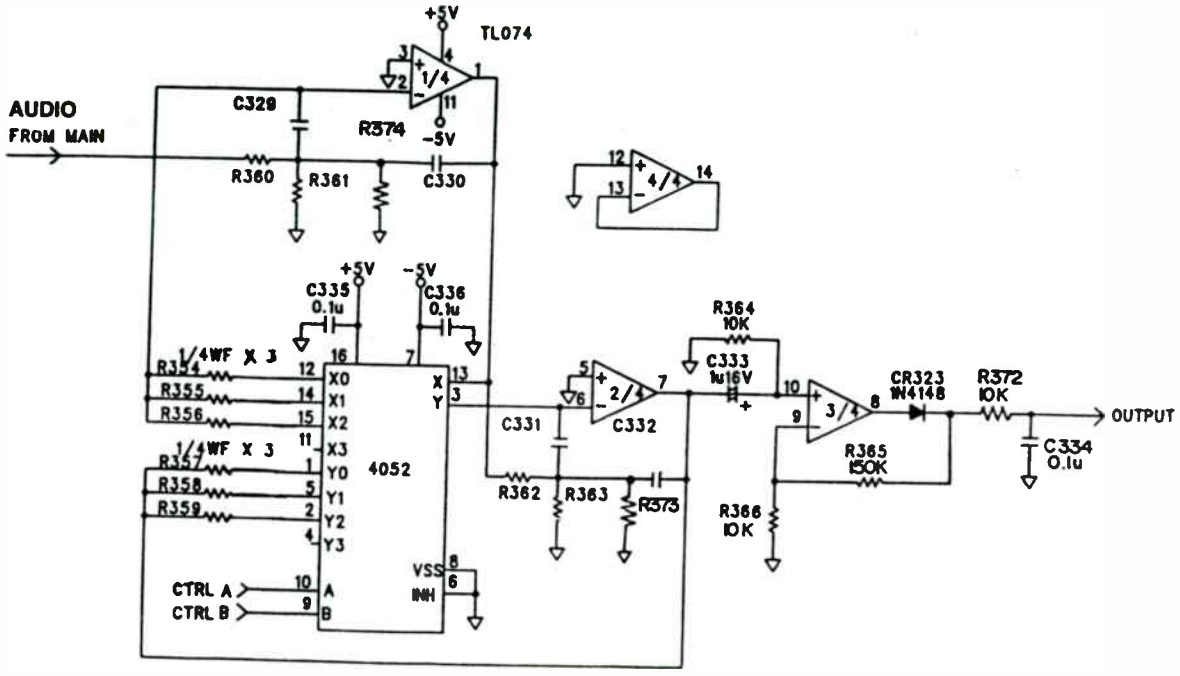


Fig. 4 Circuit for extraction of Morse Code pulse train from audio signal

Part 2: Main software layers

Regarding ASI process, system software has recording process of signal strength from satellite antenna, Morse Code recognition step and complex in-loop ASI process.

Slide #5

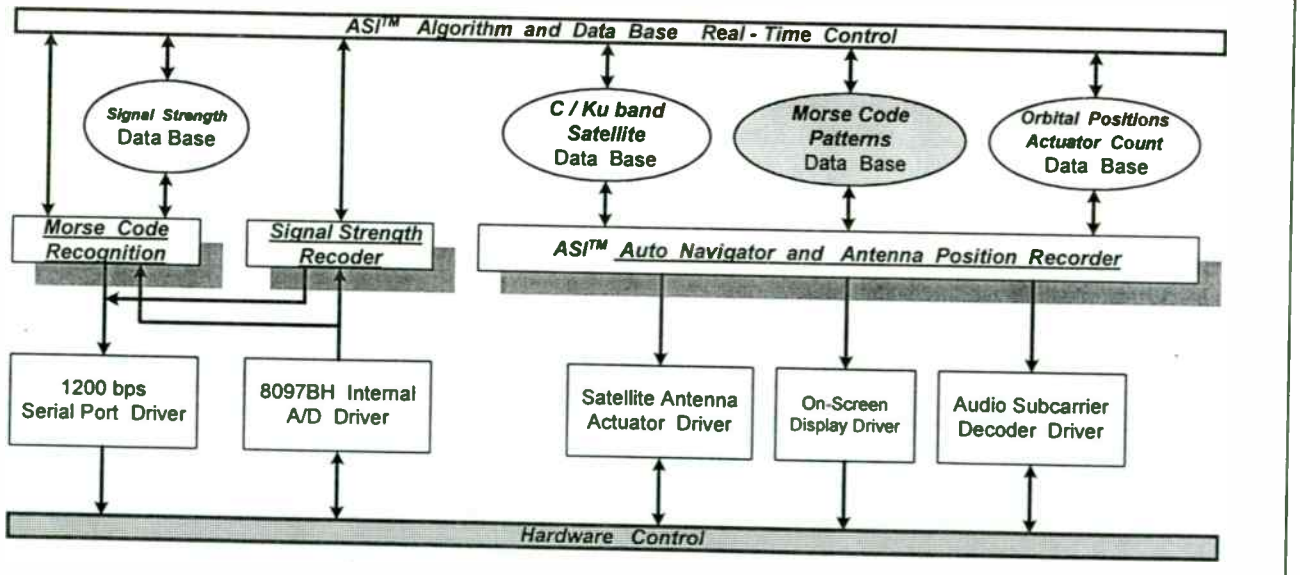


Fig. 5 Main software processing steps in Automatic Satellite Identification system.

Slide #6

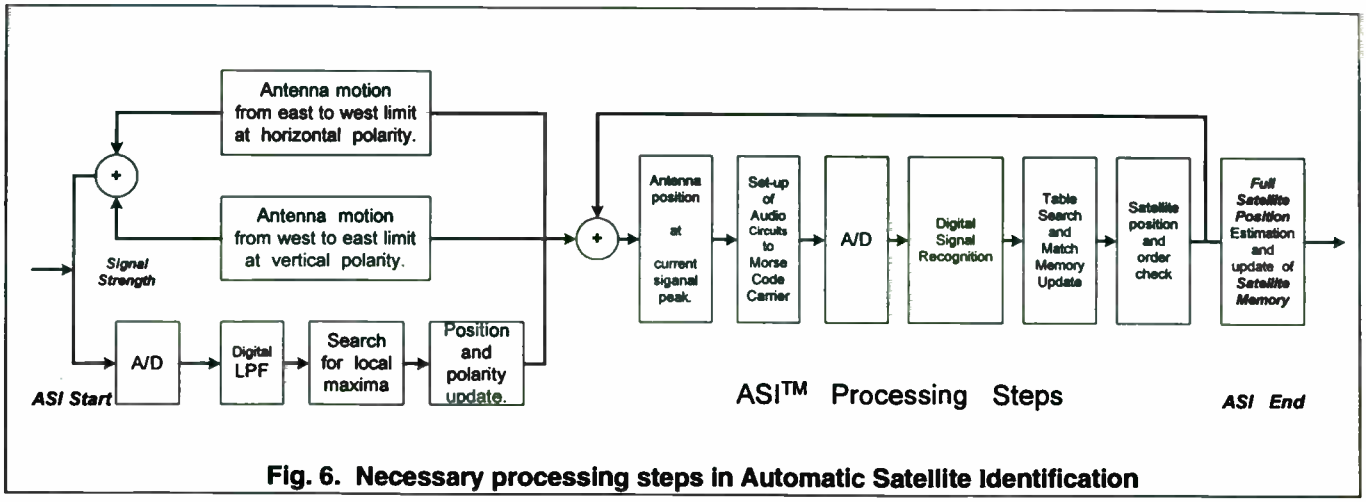


Fig. 6. Necessary processing steps in Automatic Satellite Identification

As we can see from Fig. 5., at the higher software layers, a few data base structures exist in a EPROM or SRAM memories. ***C/Ku band satellite data base*** is stored in EPROM in a form of array of 52 records (total number of satellites) containing:

- Satellite number.
- Satellite name [8 characters].
- Satellite abbreviation (for on-screen display).
- Number of channels.
- Pointer to table of used video / audio frequencies.
- C/Ku band and H/V polarity flag
- Skew value.
- Longitude of satellite.

Database of Morse Code patterns has a form of EPROM based array of 23 records containing:

- Satellite number.
- Channel Number.
- CW characteristic pattern of 4 bytes.

First two items are used to tune to a satellite, last one is used at CW recognition.

Data base of satellite orbital positions has a structure array of 52 records showing:

- Satellite number.
- Optimum skew value.
- Flags for unknown / identified, clear / calculated.
- Satellite position from the east limit as number of counts from reed-relay of antenna actuator.

This data base is stored in SRAM with battery backup and it is updated during automatic or manual satellite identification process.

Data base of recorded signal strength values has a form of maximum size array of records with:

- Signal strength value.
- Antenna position.
- East / west flag.
- Horizontal or vertical (H/V) polarity flag.
- Tuned skew value (angular position of polarotor).

This structure is stored in SRAM with battery backup and it is updated only during ASI process.

As Fig.5 shows, bottom. lower software layers forms a set of driver routines f or 1200 serial link to host PC (as a remote data logger), A/D conversion of analog signal strength and CW 'pulse train' signals and support for tuning to a satellite and to a channel with on-screen display (OSD).

Fig. 6 shows main processing steps necessary before actual satellite identification and at ASI process. Successful ASI should be possible only if there is a way to position antenna very close to the orbital slot which perhaps has satellite & CW. As a position indicator, an analog signal strength available in most satellite tuners is used. Its value increases if antenna is closer to a satellite and if angular position of polarotor is optimum (good skew value). As a position locator, a double motion of satellite antenna is used with on-line A/D & filtering.

Slide #7

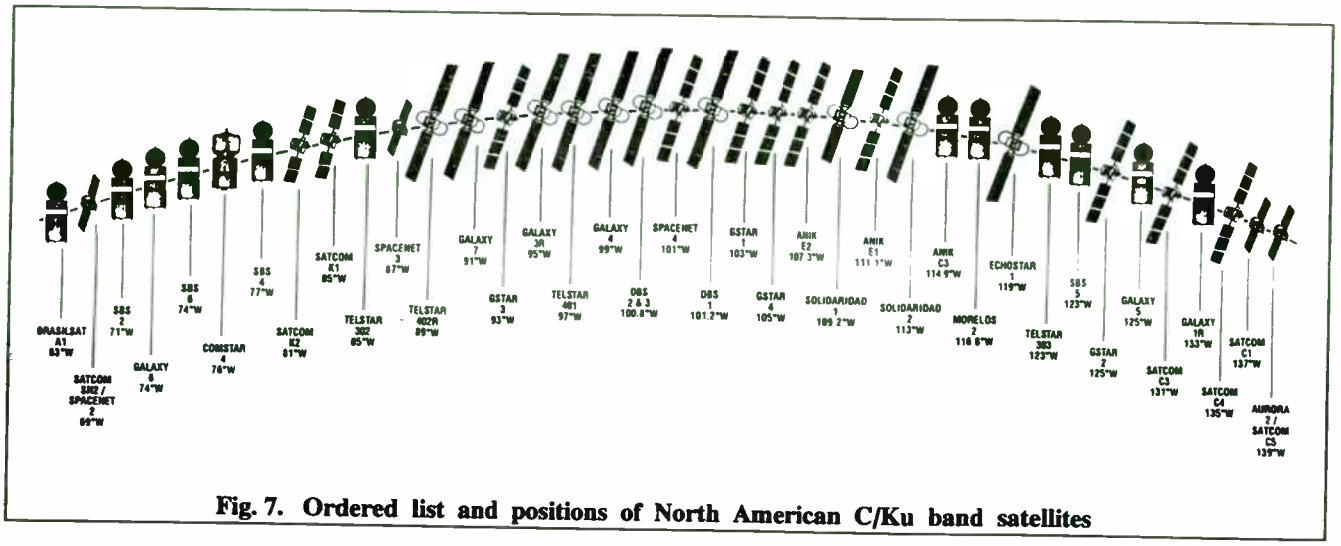


Fig. 7. Ordered list and positions of North American C/Ku band satellites

Part 3: Orbital estimation

Fig. 7. shows a list of available C/Ku band satellites over North America, ordered from east toward west.

Prior to ASI process, all satellites are non-identified in terms of position, where orbital position is internally presented as longitude number. Prior to ASI process, data base of orbital positions of all satellites is initialized to 5000 (which is default east limit value). Also, the position of west limit is known. When host CPU turns on dish actuator, the pulses which are generated by switch or reed-relay logic from actuator are incrementing internal number from east limit value (from 5000) toward west limit value (for example 6600).

In a given example, position sensor from 6' satellite antenna actuator generates about 1600 counts for one full motion. So, one can write that:

TC = WEST_LIMIT - EAST_LIMIT; (1)
where TC is total number of counts.

Satellites identified at ASI process have non 5000 value of their orbital count position and flag as identified satellite. Others are unknown, their orbital position count is 5000, ***but all*** satellite longitude values are known from Fig. 7. and saved in a data base of C/Ku band satellites. Now, if host CPU has positions of at least three satellites, it can calculate positions of all others.

if A and B are known satellites and X is the satellite which has to be identified than, by using simple linear approximation we have:

case than X is between A and B:
EAST_LIMIT < A < X < B < WEST_LIMIT

Count_Diff = Count_B - Count_A; (2)
Longitude_Diff = Longitude_B - Longitude_A; (3)
CPL = Count_Diff / Longitude_Diff ; (4)
than:
Count_X = Count_A +
(Longitude_X - Longitude_A) * CPL; (5)

where CPL is term known as count per longitude.

case than X is eastern from A and B:
EAST_LIMIT < X < A < B < WEST_LIMIT

Count_X = Count_A -
(Longitude_A - Longitude_X) * CPL; (6)

case than X is western from A and B:
EAST_LIMIT < A < B < X < WEST_LIMIT

Count_X = Count_B +
(Longitude_X - Longitude_B) * CPL; (7)

In all, above mentioned relations, to minimize the error due to linear approximation, host CPU has to use two closest identified satellites as reference for position estimation.

Slide #8

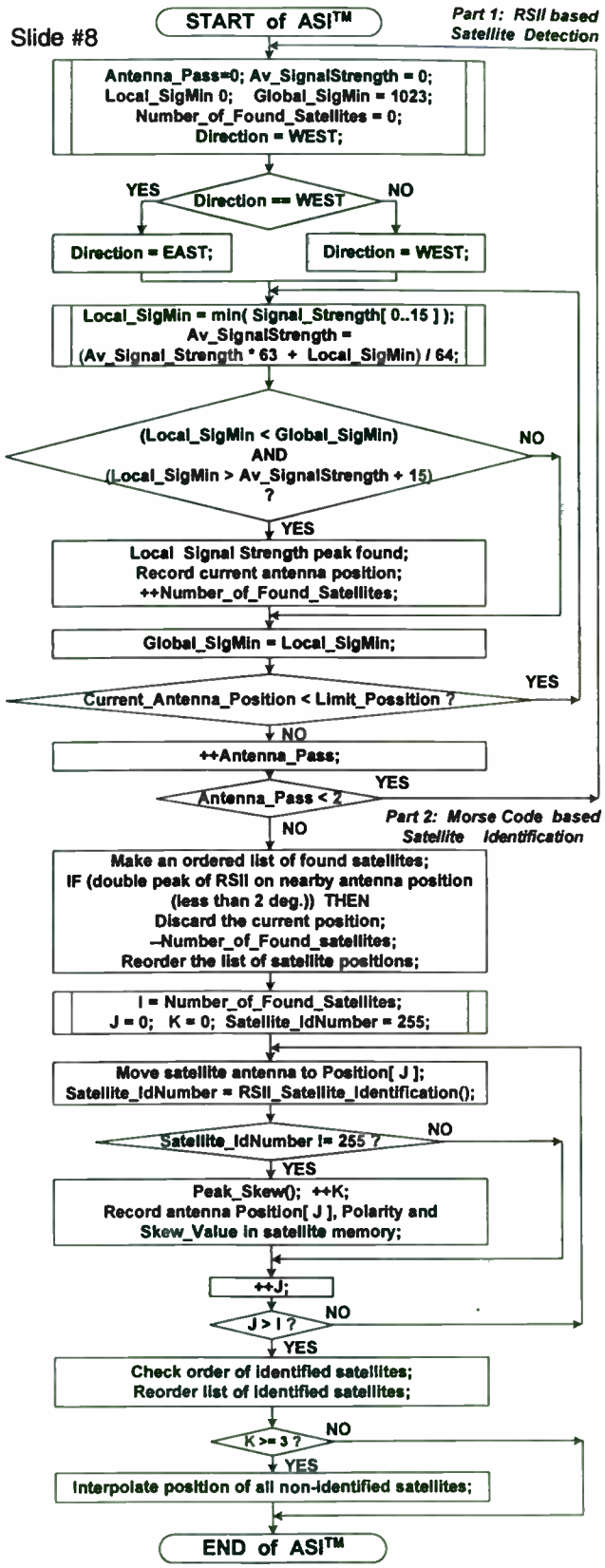
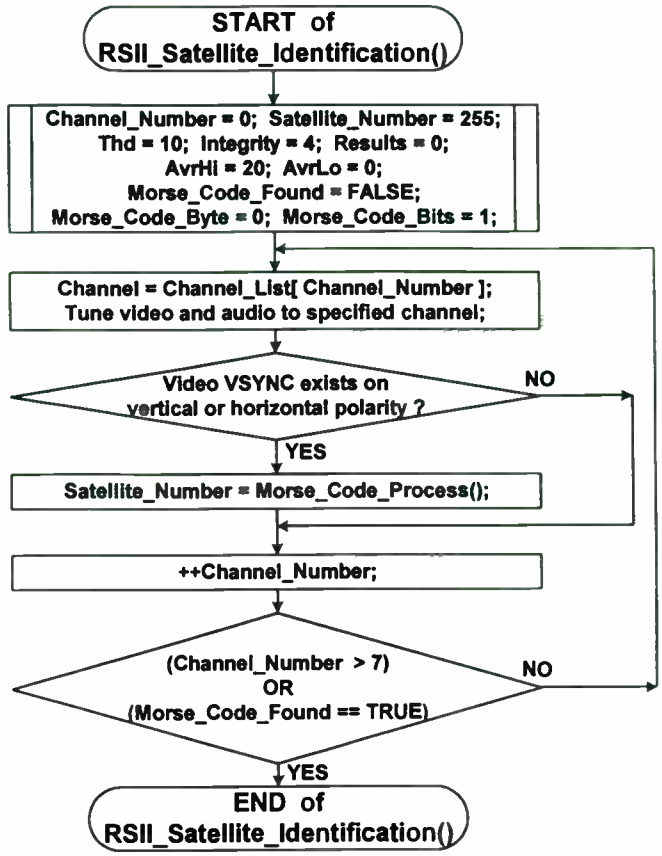


Fig. 8. Block diagram of ASI algorithm

Slide #9



Block diagram of Satellite Identification by Morse Code

Fig. #9 Structure of ASI channel tuning

Part 4: ASI algorithm

Fig. 8. shows principal structure of signal processing steps prior to and during satellite identification. As it is shown, satellite positions are identified according to local analog signal maximum strength, available as output from satellite tuner. To eliminate noise contribution, samples of signal strength are digitally lowpass filtered by software moving average filter with order of 64. After filtering, run time search is implemented and positions of local maximums are recorded in signal strength data base.

Search for local maximum is performed on double antenna motion, in both polarities. As the Fig. 9 shows, attempt to identified the satellite on local maximum is performed only if on tuned channel there is a good video (stable vertical synch pulse detected by host CPU), sequentially on up to seven channels.

Slide #10

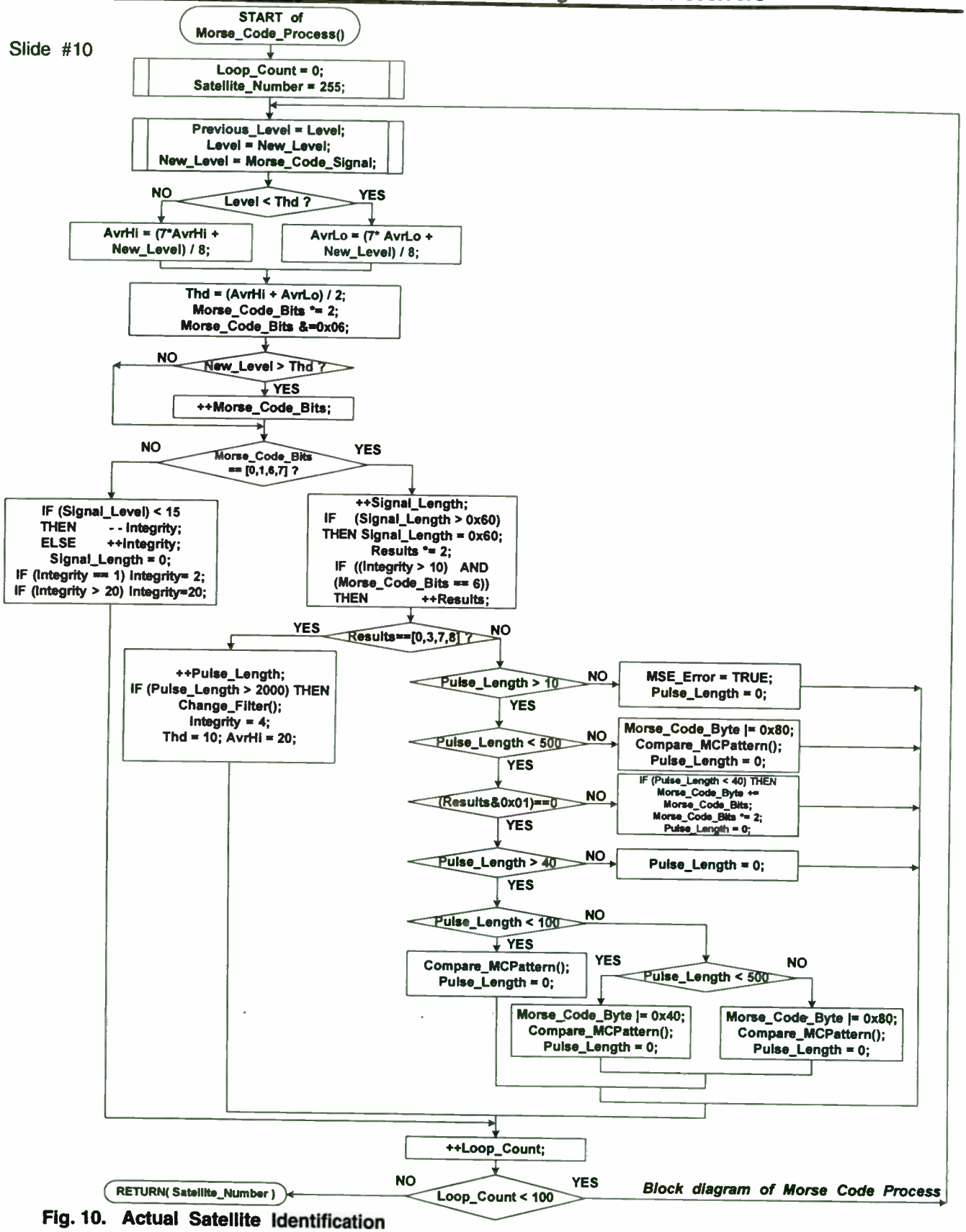
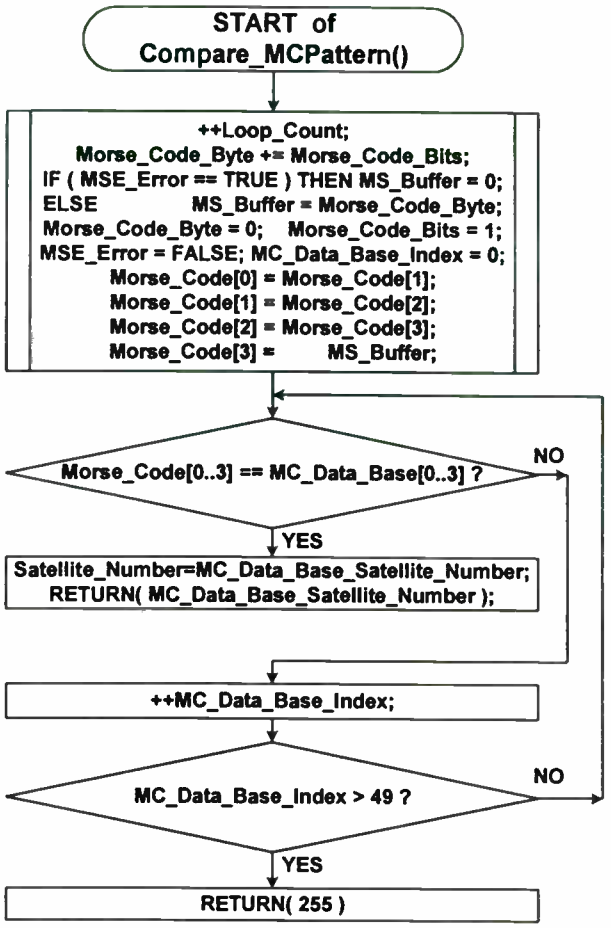


Fig. 10. Actual Satellite Identification

Slide #11



Structure of pattern search through Morse Code Data Base

Fig. 11. Actual comparison of CW patterns

Fig. 11 shows actual comparison of 4 bytes CW pattern acquired in real-time, during recognition process. If real-time pattern matches one of 42 pre-stored patterns, satellite is identified according to satellite number recorded in CW data base.

After completion of ASI process, if there is more than four identified satellites, host CPU will estimate orbital positions of all other satellites, using closest two satellites as a references for linear approximation.

As we can see from Fig. 10. recognition algorithm is based on loop counting and transition detection. Algorithm is under 'heavy' control of specific parameters (almost 'fuzzy'). Some of them, like Thd, AvrLo,AvrHii are 'software filter' parameters which controls availability and occurrences of CWs. Recognition algorithm is based on number of passes through specific states of pulse recognition (low and high levels plus edge detection). This is used for bit - by - bit extraction. Also, algorithm has loop count which is important in the case of usability to identify any of available pattern. In that instance, algorithm terminates identification and moves antenna to the next position.

Conclusion

At this paper, one algorithm for automatic satellite identification is described. Algorithm is based on regulatory ATIS message transmitted as Morse Code (CW) sequence on 7.11MHz audio sub-carrier. This has been implemented in one of our standard analog satellite receivers. Algorithm is described in terms of typical signal processing steps necessary for automatic pattern recognition.

Acknowledgments

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References

1. Frank Baylin, Brent Gale:
Ku - Band Satellite TV
Baylin Publications, 1991.

2. Mark Long:
The 1993 / 1994 World Satellite Annual
Mark Long Enterprises, Inc., 1993.

3. Westsat's Satellite:
Vol 15, No. 6 Nov/Dec 1995
Westsat Communications, 19 February, 1996.

Positioning/Navigation Applications Over MOBITEX Networks

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Abstract - Since the introduction of the Global Positioning System (GPS) by the U.S. government in the late 80's, many different applications have been developed to utilize GPS for position determination and navigation purposes. These applications include military electronic warfare, marine navigation systems, aircraft landing systems, vehicle navigation systems, and personal location systems. The position information derived from the GPS receiver in a remote/mobile system can either be used by the remote user or be relayed to a host system in a back office for further processing and manipulation.

The MOBITEX® network, a terrestrial two-way wireless data network that has been deployed in many countries worldwide, can be extremely useful for relaying such positioning information from the remote system to the host system. Use of MOBITEX networks for positioning and navigation can be beneficial in a variety of applications, such as monitoring of mobile systems, dispatching systems, mobile information services, route management, and vehicle control/security systems. In the area of personal applications, users can use MOBITEX networks to efficiently transport positioning information to public safety authorities or medical service providers in case of emergency, as well as to incorporate the information in messages for wireless e-mail or two-way interactive paging systems.

The broad features of the MOBITEX system and design criteria for a combined GPS/MOBITEX device are presented.

I. INTRODUCTION

With the advent of cellular phones and satellite communications systems, the ability to communicate with remote personnel or equipment has become indispensable in many businesses and industries. In many situations, it is important to know the exact location of the remote system. This positioning information can either be used by the remote system itself or be relayed to a host system in the back office. Important decisions can then be made based on the position of the remote system.

Despite the fact that many land-based positioning and navigation systems have been proposed and developed utilizing GPS, an effective system must include a near-real-time, reliable, and efficient wireless wide area data network. In this paper, the system infrastructure chosen to provide such an efficient communications pipe is MOBITEX.

II. THE MOBITEX SYSTEM

The MOBITEX system was designed by Ericsson Mobile Data Design AB in Sweden in the mid 80's as an integrated voice and data system. The evolution of the system has made MOBITEX a robust and efficient two-way wireless data communications system. The MOBITEX system has been deployed in 17 countries worldwide, with the U.S. network being the largest. RAM Mobile Data operates the MOBITEX network in the U.S. within its licensed SMR (Specialized Mobile Radio) frequency band (i.e., 900 MHz).

MOBITEX is a digital wireless data system using the GMSK (Gaussian Minimum Shift Keying) modulation technique. The data rate over the radio link is 8000 bps (bits per second), which makes it an ideal system for

transporting positioning information and short messages. The channel access algorithm utilizes a TDMA-like reservation slotted Aloha technique, which makes data transmission very efficient. Additionally, the system incorporates several different error detection and correction techniques, as well as an effective message block retransmission (ARQ) algorithm. Like new digital cellular systems, MOBITEX has an efficient power control algorithm, which allows the mobile device to control its output power via both closed-loop and open-loop mechanisms. MOBITEX also employs an advanced battery saving protocol, which helps conserve the mobile device's battery life. Unlike cellular systems, roaming is transparent to MOBITEX users, and no additional roaming charges are incurred. Cell hand-off is primarily determined by the mobile device based on the received signal strength from the current and neighboring base stations.

The architecture of the MOBITEX system is hierarchical, as shown in Fig. 1; that is, messages are transferred to the destination at the lowest possible level. MOBITEX base stations and switches can operate autonomously if up-node connections are broken. Host systems can be connected to the MOBITEX network at the local switch (i.e., MOX) level via FEPs (Front End Processors). The host connection can be either shared or dedicated, at speeds of up to 56 Kbps.

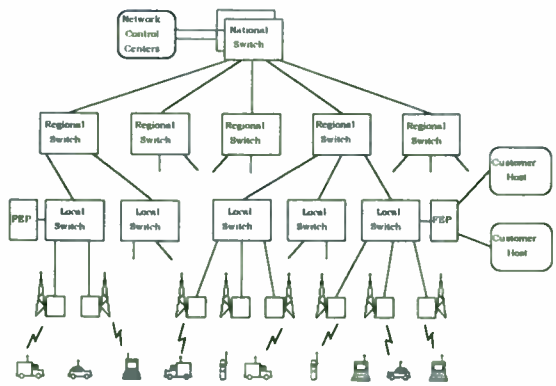

Fig. 1. MOBITEX System Architecture

In addition to its robust and efficient design, the MOBITEX system also employs many other features that can be very useful for the land-based positioning and navigation system. The user configurable "Store-&-Forward" feature allows messages to be stored in the network mailbox if the destination is not reachable, and those messages will be forwarded to the destination when it becomes available. Although the messaging protocol of MOBITEX is designed to be NAK-based (i.e., negative acknowledgment), the host system can request a positive acknowledgment to be sent back when the message has been delivered to the mobile device. This feature is extremely useful for the host system to confirm the receipt of the message by the remote system.

III. MOBITEX Strategic Network Initiative

In an effort to address ubiquitous coverage, RAM Mobile Data has developed a Strategic Network Initiative (SNI). The SNI allows different types of networks, i.e., satellite, circuit-switched cellular, PSTN and paging, to be connected to the MOBITEX network and to provide additional coverage.

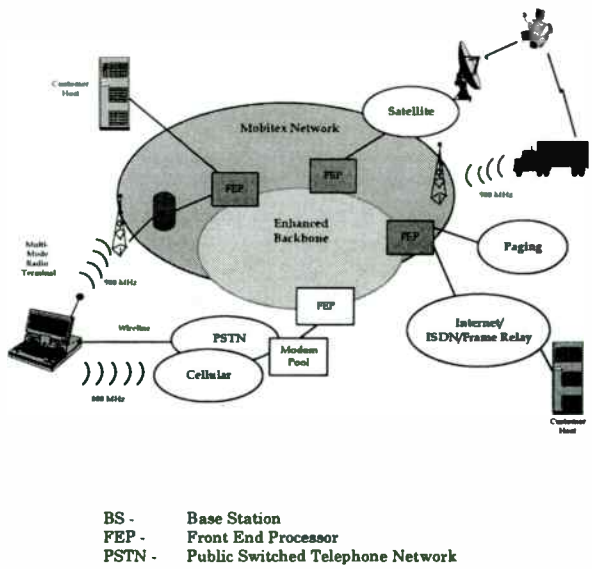

Fig. 2. MOBITEX Strategic Network

As shown in Fig. 2, the SNI employs MOBITEX as a primary service and other networks as secondary services if MOBITEX coverage is not available. In order to eliminate the need for a complex application design, a single application resides on the host

system, which only interfaces with the MOBITEX network. A single application is also used in the remote system, and switching between different networks can be handled by an underlying API (Application Program Interface) and is transparent to the user.

The MOBITEX Strategic Network is particularly useful for a land-based positioning and navigation system that encompasses a very wide area. Such a system may require a ubiquitous coverage for communications between the host system and remote system.

IV. Land-based Positioning/Navigation Applications

Typical land-based positioning/navigation applications can be categorized into the following types:

- Mobile Monitoring
- Dispatching and Route Management
- Mobile Information Services
- Vehicle Control and Security
- Personal Positioning and Navigation

Monitoring of mobile systems is the basic function of the land-based positioning/ navigation system. The primary purpose of mobile monitoring is to allow the host system to collect vehicle-related information and positioning information, so that the information can be used for future planning. Interactive communications between the remote system and host system are typically precluded in the mobile monitoring application.

Dispatching and route management have become indispensable functions of many transportation and field service businesses. Based on the positioning information received from the remote system, the dispatching center can efficiently manage service routes and schedule pick-up and delivery times. Interactive communications between the host and remote systems are generally allowed. The remote system can send short "canned" messages or free form messages.

Mobile information services are intended for the horizontal market, such that travel-related information can be provided to the remote system from an independent service provider. The services may also allow the user of the remote system to send and receive electronic mail.

Vehicle control and security has been a popular subject in the transportation industry. Typical applications include remotely unlocking vehicle doors or disabling the engine if the vehicle has been tampered with. Use of the positioning information can help public safety authorities locate stolen vehicles.

Use of GPS receivers has been seen in many personal applications, such as those used by hikers, campers, etc. The positioning information is being used by individuals to determine their locations. By using a wide area wireless communications system, such as MOBITEX, the positioning information, along with distress signals, can be sent to public safety authorities or medical service providers in case of emergency.

V. HYPOTHETICAL CASE STUDY

The following hypothetical example has been created to cover different aspects of the land-based positioning and navigation system, which uses MOBITEX as primary means to transport data between the host and remote systems in near real time.

A long-haul trucking company operates a fleet of trucks to transport refrigerated goods across the continent. The truck tractor has a refrigeration trailer, which includes a controller for controlling temperature of the refrigeration unit. In order for the company to monitor engine performance, a J1708-based diagnostics module is installed in the vehicle. A special mobile device has been developed for the system, which consists of a GPS receiver and a MOBITEX core unit and which resides in the tractor. The MOBITEX core unit interfaces with the GPS receiver, refrigeration control module ("refeer"), engine diagnostics module, a keyboard/ display unit ("KDU") in the cab, and various sensors. The individual interface functions and system components are shown in Fig. 3.

The MOBITEX core unit incorporates the SNI technology by combining the MOBITEX and SATCOM (i.e., satellite communication via a geo-stationary satellite) functions in one box. This configuration is cost effective by allowing the remote system to operate on the MOBITEX network in urban and suburban areas, and on the SATCOM network in rural areas, where MOBITEX generally lacks extensive coverage. Additionally, use of the MOBITEX network as a primary service is less expensive because of its pricing structure, in which charges are incurred for actual packet transfers across the network and, as mentioned above, customers do not incur any additional charges for roaming from coast to coast.

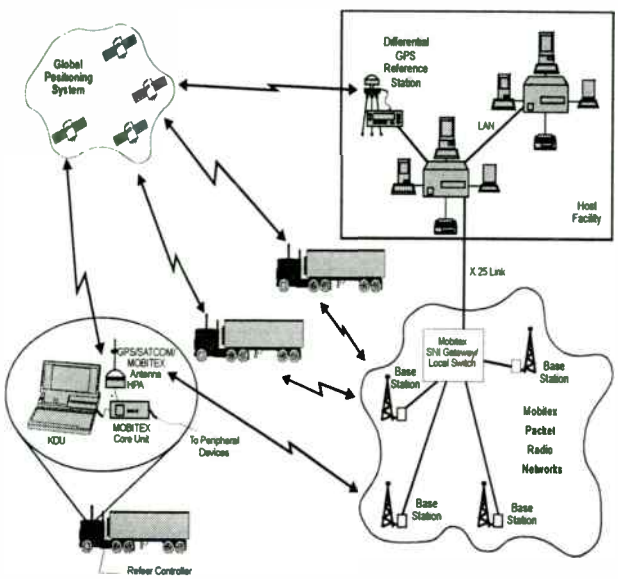

Fig. 3. Hypothetical System Design

MOBITEX-GPS Interface

The GPS receiver is configured to periodically (e.g., every two minutes) send updated positioning information to the MOBITEX core unit. The interface module maintains a history of the positioning data, and will trigger the MOBITEX core unit to transmit the positioning data periodically or along with other transmissions.

The interface conforms to the NMEA (National Marine Electronics Association) standards over an EIA-422 physical connection.

MOBITEX-Refeer Interface

The MOBITEX core unit communicates with the refeer unit under two situations. When the refeer temperature reading is out of range (i.e., above certain threshold), an alert message will be generated and be sent to the dispatching center. The dispatcher can also initiate specific commands to control the refeer (e.g., to collect temperature readings or set a new reference temperature).

This interface extends between the tractor and trailer of the truck. Due to the noisy environment in the truck, a custom protocol is developed for the interface to minimize the interference. The physical link of the interface conforms to the EIA-232 standard.

MOBITEX-J1708 Interface

The J1708 bus based engine performance monitoring module communicates with the MOBITEX core unit by periodically sending the vehicle-related information, such as odometer reading, gas level, average driving speed, engine temperature, engine idling time, etc. The information is collected by the MOBITEX core unit, and will be relayed back to the dispatching center at a fixed interval. Additionally, an alarm message may be generated under conditions such as engine overheat. This alarm message will be sent to the dispatching center immediately.

This interface conforms to the EIA-485 standard.

MOBITEX-KDU Interface

The KDU allows the driver to receive and view text messages sent by the dispatcher, and to compose messages (pre-programmed canned messages or free form messages) for transmitting to the dispatcher. The driver can also use the KDU to monitor and control the refeer and engine diagnostics modules. The positioning information derived by the GPS receiver can be read using the KDU. Additionally, the KDU allows the driver to monitor and change certain network operating

parameters, such as signal level, channel information, and main and backup battery status. The KDU has LED's indicating the network coverage status (for MOBITEX and SATCOM), and the LED blinks when transmission is occurring.

The interface employs a custom asynchronous protocol over an EIA-232 physical link.

MOBITEX-Sensor Interface

The MOBITEX core unit has an interface module for interfacing with various sensors in the truck, such as a vehicle alarm system, tire pressure sensor, cable disconnect, etc. These sensor signals will trigger an immediate alert message transmission to the dispatching center. The interface module can be simple on/off switches, but should incorporate a de-bouncing mechanism to prevent false signals due to static or EMI.

Antenna System

In addition to a variety of interfaces to the peripheral modules, the remote system employs an integrated antenna system. The bottom part is a flat HPA (high power amplifier), which is used by the SATCOM transmitter to provide 10 to 20 Watts output power levels. The nominal output power for Mobitex transmission is 4 Watts, which is generated by an internal power amplifier in the MOBITEX core unit. A flat panel GPS antenna is on the top of the HPA. Above the GPS antenna is a SATCOM cone-shape panel antenna, whereas a vertical whip-type antenna is used for MOBITEX. The GPS and SATCOM antennas can be further integrated provided the same frequency range is used. In order to minimize interference, only one type of transmission is allowed at any given time. When transmission is occurring, the GPS receiver must be turned off to prevent possible damage on the receiver front end.

The antenna system can be mounted on the top of the tractor, or be hidden inside a nose cone. The antenna cable length must be carefully characterized and designed, so the RFI/EMI due to noisy trucking environment can be minimized.

The Dispatching Center

The trucking company's dispatching center consists of a mid-range host computer (i.e., an IBM AS-400) and PCs connected to a company LAN. The host computer has an X.25 connection to a MOBITEX POP (Point of Presence) over a dedicated DDS (Digital Data Service) leased line. The MOBITEX POP consists of a Strategic Network gateway and a MOBITEX local switch. The host connection can carry TCP/IP packets over X.25 if so desired.

The application on the host computer is MOBITEX literate; that is, it understands the messaging protocol (i.e., MPAKs) used in the MOBITEX system. The host computer is also used as a server to distribute the data to client PCs via the company LAN. Each PC is running a mapping software, and the routes of selected trucks are represented by icons on the map. Clicking a truck icon will show the status of the vehicle, including its engine performance, message transactions, and emergency conditions.

To assist in more accurate positioning determination, a differential GPS (DGPS) reference station can be used at or near the host facility. The DGPS data is fed into the host computer and is combined with the GPS information received from the remote truck. As a result, the new position of the truck can have an accuracy of less than a meter.

The operator at the dispatching center can send text messages for new pick-ups, route changes, or personal messages. Time-sensitive messages can be sent to the remote system with a request for positive acknowledgment. When the MOBITEX network delivers the packets to the remote system, a confirmation (i.e., positive acknowledgment) will be received by the dispatcher. Positive acknowledgment can help the dispatcher make a quick decision for an alternate plan if the intended recipient is not available. Other types of messages (i.e., personal messages) can be sent with the mailbox function enabled. Under such circumstances, the message will be stored in the MOBITEX mailbox if the intended recipient is not reachable (e.g., the remote

system is out of MOBITEX network coverage). A similar store-and-forward function can also be provided by the SATCOM infrastructure or by the SNI gateway.

A large company that has redundant hosts at different locations can utilize the MOBITEX host group feature. This feature allows different host platforms to use the same logical MOBITEX address, so messages will be routed to the nearest host platform. In addition to providing a local or shortest path for host access, this feature also improves reliability of host connectivity and achieves load balancing and redundancy.

An alert message (i.e., refeer temperature out of range or engine overheat) will trigger an alarm system in the dispatching center. The dispatching center operator can take whatever action is appropriate.

Switching Between MOBITEX and SATCOM

The remote system communicates with the host system primarily over the MOBITEX network. The MOBITEX core unit of the remote system can detect if the system is out of MOBITEX network coverage, and will automatically enable the SATCOM function. While the remote system is operating on a SATCOM channel, the MOBITEX receiver continues to scan available MOBITEX signals. When a valid MOBITEX channel is found, the remote system reverts to MOBITEX operation.

The entire switching process is transparent to the user and to the mobile application. The communication processor of the MOBITEX core unit handles message routing appropriately.

Outbound messages (i.e., from the host to the remote) can be routed to a proper communication facility by the Strategic Network gateway. The gateway keeps coverage status of the remote system. If the remote system is not in MOBITEX coverage, outbound messages will automatically be routed to the SATCOM facility. In order to make the gateway function efficiently, customer profile information is maintained in the gateway. This configuration helps the host system only deal with one network using a single application, which significantly reduces the complexity and cost of an application design.

VI. CONCLUSION

Using the MOBITEX system, along with the Strategic Network, to transport data between a host system and a remote system in a land-based positioning/navigation application will provide reliable, efficient, and cost effective ways of conducting business. Unnecessary stops of the truck can be minimized, if not eliminated, thereby saving costs of fuel and time. Return on investment for this system can be readily and quickly realized. Because of the continuous evolution of the MOBITEX system, the user's investment in the system will be protected.

References

[1] T. Yang, "Use of MOBITEX Wireless Wide Area Networks as a Solution to Land-Based Positioning and Navigation," *Proceedings of the Position, Location and Navigation Symposium*, 1994.

CAD of LNA based on an new transistor characterization method for satellite communications

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ABSTRACT

A new simplified procedure for the determination of noise parameters of active devices at microwave frequencies is here employed for investigating the performance of a low-noise amplifier based on a set of HEMTs (NE20283A, by NEC) for satellite communications. The results of the comparison with the performance computed with the standard method are also reported.

I. INTRODUCTION

An accurate computer-aided design of low-noise amplifiers for VSAT system based on HEMT's, requires a very detailed representation of the scattering parameters [S] and transistor noise {N}.
The measurement of two-port scattering parameters vs. frequency and bias is easily handled by use of modern automatic network analyzer (ANA) operating up to the millimeter wave range (50 GHz).
On the contrary, the experimental determination of the noise parameters (F_{min}, Γ_{opt}, r_n) is based on a complex time-consuming procedure which still requires a great deal of operator expertise, despite the fact that automated noise figure measurement systems are now commercially available.
To the aim of simplifying the device characterization procedure, a new method that allows the determination of the noise parameters starting from a computer analysis of a noisy circuit model previously extracted from measured scattering parameters plus one single noise figure measurement in input match condition (i.e. 50 Ω) has been derived [1].
In this paper we present the performance of a low-noise amplifier for satellite communications based on a set of HEMTs (NE20283A, by NEC), characterized according with new method. The results of the comparison with the standard method are also reported.

II. TRANSISTOR CHARACTERIZATION: SIMPLIFIED PROCEDURE

As far as the standard transistor's characterization is concerned, the noise parameters (F_{min}, Γ_{opt}, and r_n) are derived by computating the equation mentioned under for different values of transistor's noise figures (more than four, for redundance)

$$F(\Gamma_S) = F_{min} + 4\, r_n \frac{|\Gamma_S - \Gamma_O|^2}{|1+\Gamma_O|^2(1-|\Gamma_S|^2)}$$

measured at different input termination conditions Γ_s. The $F(\Gamma_S)$ values are calculated by employing the noise figure measuring set-up reported in Fig.1 (working up to 40 GHz for chip and packaged transistors).
Starting from the knowledge of the noise parameters {N}, the scattering parameters [S] can be computed ([2] and references therein).
The automated version of the standard procedure is rapid and very accurate when compared with conventional ones, but a very skilled operator is required.
So, recently a new simplified version has been set-up useful for industrial applications.
With reference to the simplified procedure, as a first step the transistor scattering parameters are measured by an ANA and the F_{50} noise figure value is measured by the measuring set-up reported in Fig.2. In particular the noise figure F_{50} of the transistor in input matched condition has been chosen, as it can be correctly measured by using a commercial noise figure meter (NFM).
A circuit model is then extracted by fitting the performance of the typical device. The model

extraction is accomplished by fixing the basic circuit topology that includes the package parasitics and by applying a decomposition approach for the separate optimization of the circuit variables.
Next, the noise performance are associated to the equivalent circuit by using a noise temperature model that allows to emulate noise parameters upon assignment of equivalent noise temperatures T_g and T_d to the resistive elements R_{gs} and R_{ds}. It has been argumented that T_g approaches the device ambient temperature, while the T_d value is calculated by fitting the F_{50} noise figure values vs. frequency. Starting from the noise model, the noise parameters can be computed by a circuit analysis carried out by using a commercial software package.

III. EXPERIMENTAL RESULTS

A set of 4 packaged pseudomorphic HEMTs'samples (NE20283A, by NEC) has been characterized over the 6-18 GHz range, according to the simplified procedure. The noise model network is reported in Fig.3 together with the table of the element values.
As a second experimental step, the characterization of the transistors starting from noise figure measurements, according to the standard version, has been performed and the noisy model extracted. On the basis of the measured {N}, the F_{50} noise figure values have been computed.
The effectiveness of the simplified procedure is exhibited by the plots reported in Fig.4.
Starting from the noisy models a careful investigation on the optimum performance values (noise figure, operating power gain, input VSWR) of the HEMTs set has been carried out.
A two-stages front-end LNA over the VSAT frequency range has been designed by imposing as goals optimum trade-off values in order to obtain high performance and to avoid unfriendly procedures of trial and error during the process of loads selection [3].
Optimum noise figure, operating power gain, input VSWR and unconditional stability has been the key parameters which defined the LNA input matching network and its design. The circuit configuration has been analysed using the Smith chart and the LIBRA_CAD package.

The HEMTs minimum noise figure (F_o) starting from the two models as a function of frequency is reported in Fig.5
Some interesting remarks can be made:
- over the 8-18 GHz frequency range the values relative to the minimum noise figure obtained from the simplified procedure (F_o-mod) coincide or lie above the values relative to the minimum noise figure derived from the standard procedure (F_o-meas).
It occurred that, designing the LNA by imposing the F_o-mod values as goals for a minimum noise figure, the simulated noise and gain have a value corresponding to an optimum trade-off and it is characterized by a more stable behaviour of the power gain against variations of the device noise figure.
- over the 6-8 GHz frequency range the curves'position is reversed, but it corresponds to a devices' unstability.

IV. CONCLUSIONS

A new simplified procedure for the determination of noise parameters of active devices at microwave frequencies has been employed for investigating the performance of a low-noise amplifier based on a set of HEMTs (NE20283A, by NEC) for satellite communications. The result of the comparison with the performance computed with the standard method has been reported.

REFERENCES

[1] A. Caddemi, A. Di Paola, M. Sannino "Comparison between two measuring methods for complete characterization of low-noise HEMTs at microwaves", *Proc.of 26th European Microwave Conference*, Praga, 9-12 Sept.1996.
[2] G. Martines, M. Sannino, "The determination of the noise, gain and scattering parameters of microwave transistors (HEMTs) using only an automatic noise figure test-set", *IEEE Trans. Microwave Theory Tech.*, July 1994.
[3] G. Capponi, B. Di Maio, P. Livreri, "HEMTs for low-noise microwave: CAD-oriented performance evaluation", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-43, pp. 1226-1229, June 1995.

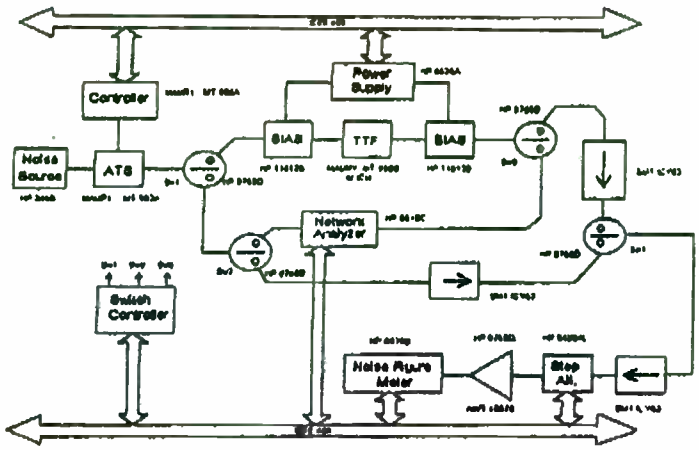

Fig.1 - Block diagram of the computer controlled noise figure measuring system for the simultaneous determination of noise, gain and scattering parameter sets in the version up to 40 Ghz.

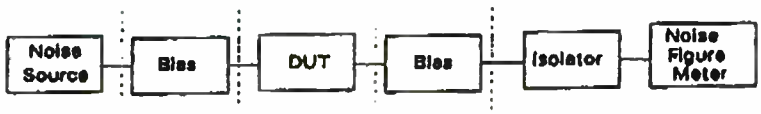

Fig.2 - Block diagram of the measuring set-up for measurement of noise figure in input matched condition (50 ohm).

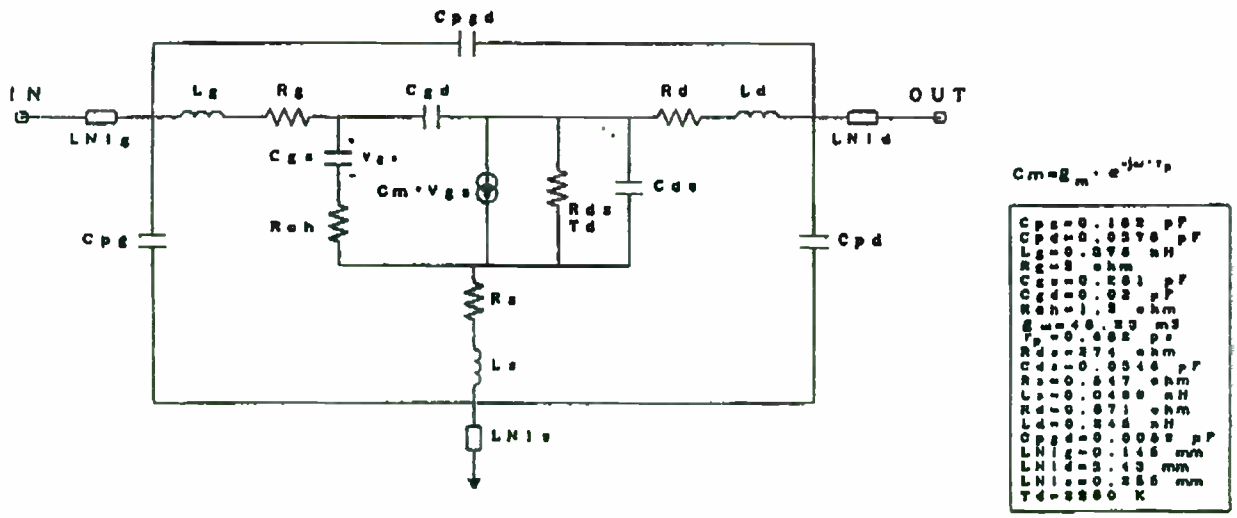

Fig.3- The *typical* circuit model of the packaged pseudomorphic HEMT NE20283A (by NEC) together with the table of the relevant element values.

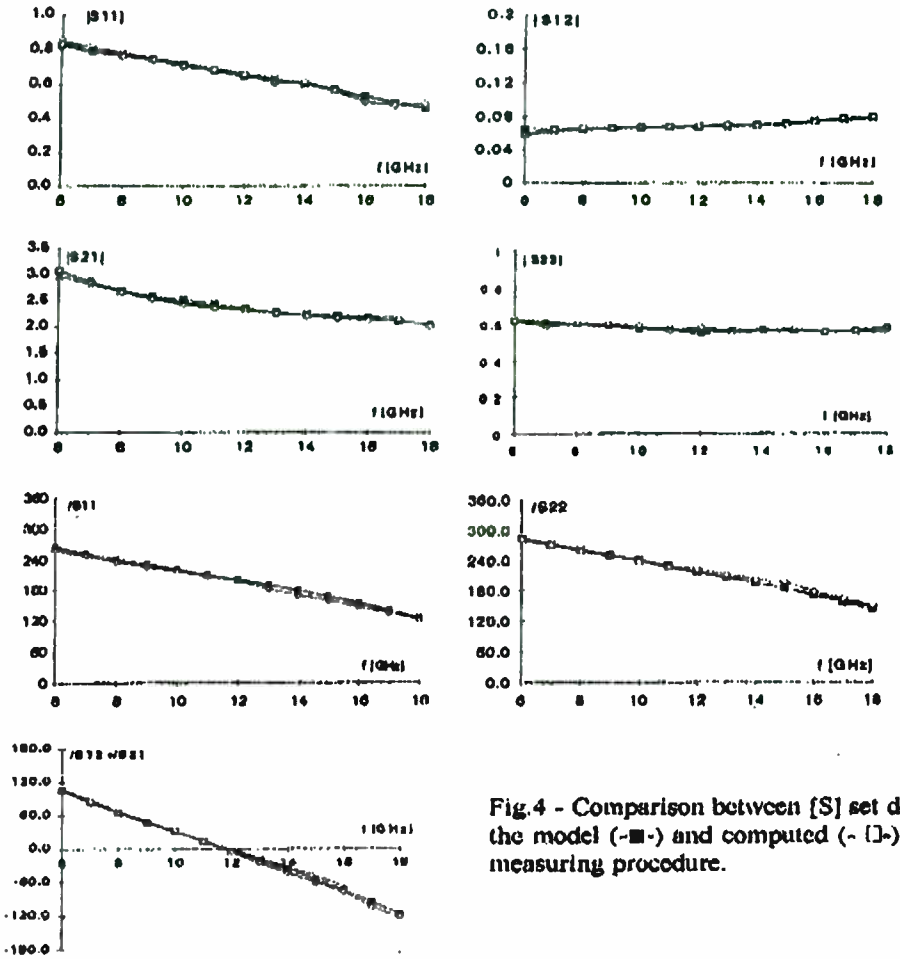

Fig.4 - Comparison between [S] set derived by the model (-■-) and computed (- □-) by noise measuring procedure.

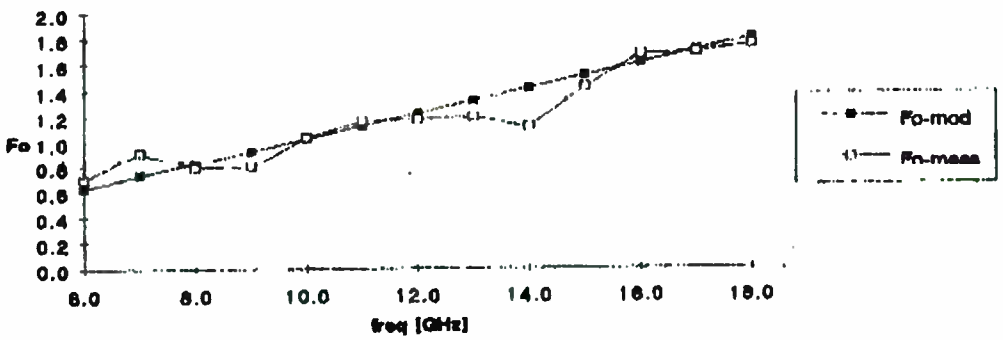

Fig.5 - HEMT's minimum noise figure.

A CONFIGURABLE RF SUBSYSTEM FOR ADAPTATIVE SIGNAL PROCESSING

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ABSTRACT

Signal processing in navigation, telecommunication and telemetry systems needs to be adaptative because of the dynamic environment. Furthermore, one encounters different data format in the above mentionned domains.
In order to choose algorithms based on signal conditions a reconfigurable hardware sub-system was designed : Chiptelos. It is a software configurable hardware subsystem.

1. INTRODUCTION

In transmission related fields, one encounters modulation, demodulation, bit-synchronization, error correction and data extraction. Under a dynamic environment, it is needed to choose a signal processing algorithm adapted to the application environment. This condition requires a great flexibility at the hardware level. The recent development in FPGAs has offered the possibility to lay foundations for such a high bandwidth reconfigurable subsystem.

2. OBJECTIVES

Chiptelos has been developed to meet the following requirements :

- Reconfigurable technology environment with application oriented symetrical architecture
- Asic emulation facility
- Adaptative GPS receiver
- Realtime kernel
- Highspeed interface
- Single slot PCI interface

3. SYSTEM ARCHITECTURE

Chiptelos is made of the 3 main following functional blocks which can be individually selected according to the needs of specific applications :

- A reconfigurable hardware block
- A scalable floating-point DSP block
- A reconfigurable memory block

and an interactive user interface.

3.1 Reconfigurable hardware block

This block is mainly based on two 4000E-series FPGAs from Xilinx. Chiptelos reconfigurable structure has been designed to accomodate :

- Polyface filters
- Spectrum forming filters
- Correlators
- Automatic gain control and baseline correction
- Frame and bit synchronizers

Polyface filters have been used for decimentation purposes in order to lessen the intermediate frequency analog filter constraints. Due to its configurable nature, the filter structure can be chosen to adapt the quantized signal rate.
The configurable nature of the spectrum forming filters allows us to study the various possible structures on the development stage .
The correlators are the heart of the signal processing applications on GPS and other CDMA applications.

3.2 A scalable floating-point DSP block

The DSP block is based on SHARC 21062 from Analog Devices. It is mainly used for distributed signal processing. The processors can be configured in a pipeline mode. The FFT processing is performed in conjunction with the configurable hardware block.
A user added configurable block can be plugged onto the application slot of Chiptelos and linked to the above two blocks.

3.3 Interface

This interface has been made for windows environment on PC. Its nature allows to design and test systems interactively.

4. APPLICATION EXAMPLE

The current application library aims at developing a system in order to receive navigational and time information from two different sources : Navstar and Inmarsat-3. Both have different signal processing requirements due to their symbol rate and Inmarsat-3 has a forward error correction facility. It is geostationnery and will provide information about its position, time information and the tropospheric delay correction. In GPS based systems, two degradation factors dominate :

1. Selective Availability (SA)
2. Ionospheric distortion

On a system using two different frequencies (for example L1 and L2 frequencies for GPS), and starting from both frequencies, it is possible to calculate the ionosphere delay which is a function of the frequency. With Inmarsat-3 these informations are already available.

These information will be used to obtain a better navigational solution on Navstar satellites. It is performed in the following manner :
The processing is shared between the configurable hardware DSP block and the scalable processor block. All the correlators for this design have been implemented on the configurable hardware block. The results of the correlation are then used to detect the availability of the satellites using coarse and fine FFT processing. The code, carrier tracking and error correction are implemented in software. Eventhough there is a possibility to implement the error correction facility and the telemetry information on the configuration block, it has been done in software which facilitates the detection and correction of multipath errors. In order to track GPS satellites, Chiptelos will first lock onto Inmarsat-3 and get all the available information. Then, during the second phase of the processing, it will lock onto Navstar satellites.
To switch from Inmarsat-3 to Navstar, or vice versa, Chiptelos changes both hardware and software libraries in realtime.

Other applications currently under consideration include the development of a satellite ranging system based on Chiptelos architecture where the configurable architecture has been designed to test first the transmission channels and then to perform the ranging applications.

Chiptelos can also be configured to meet numerous other applications in transmission, multiplexing and demultiplexing, base stations (DGPS or GSM) ASIC emulation, functional simulation, data acquisition and processing with high speed storage (80 Mbytes/s) interface for digital recorders, workstation or to a PCI based peripheral.

5. CONCLUSION

As the FPGA functional capabilities keep on increasing, the reconfigurable computing provides an alternative to the classical way of designing applications.
Front end development is achieved today by simulation. The Chiptelos reconfigurable architecture has been designed to valid simulation interactively. It is a modular system. Hardware modules are tuned according to the application requirements which make it a highly adaptable subsystem for PCI environment on PC. The architecture allows signal processing resources to be switched in a real time mode.

ACKNOWLEDGEMENTS

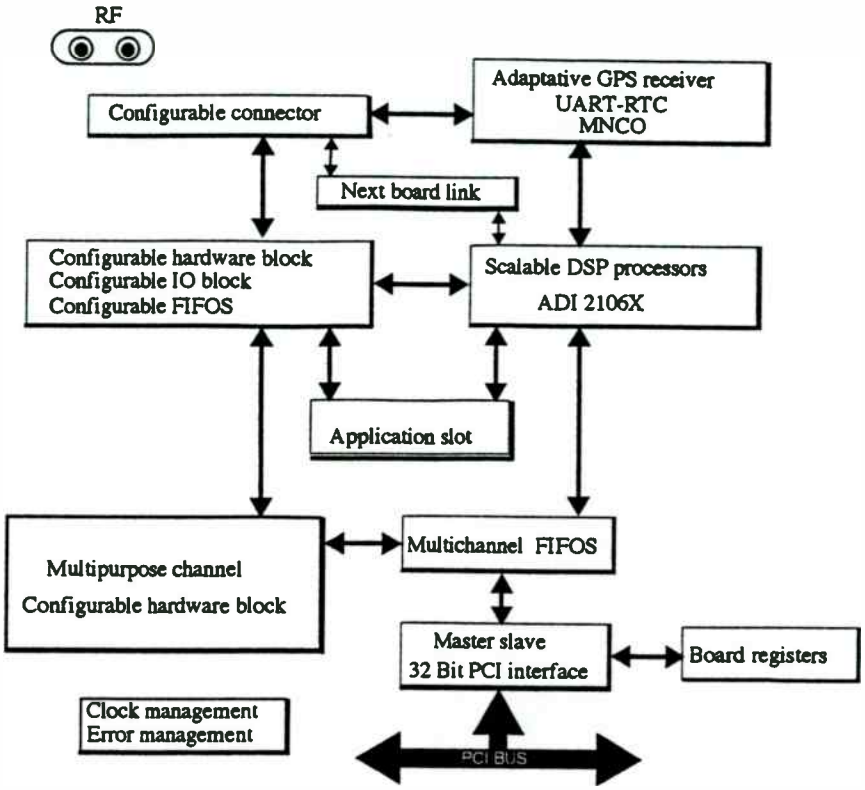
This project has been supported in part by ANVAR and DRIRE.

REFERENCES

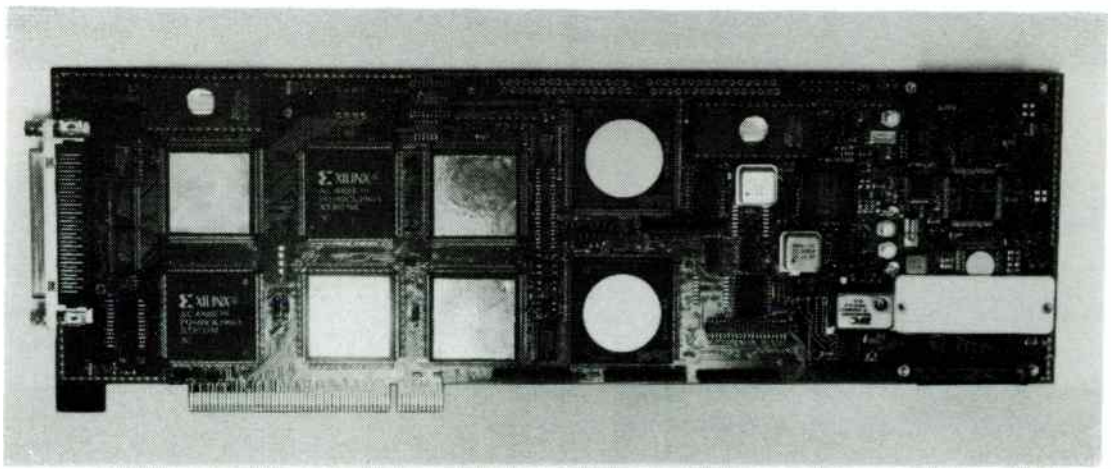
- R.A. Valenzuela and A.G. Constantinides, "Digital signal processing schemes for efficient interpolation and decimation" IEE Proceedings, Vol.130, Pt.G.No.6, December 83
- Gin-Kou Ma and Fred J.Taylor, "Multiplier policies for digital signal processing" IEEE ASSP Magazine, January 1990

- Stanley A.White, "Applications of distributed arithmetic to digital signal processing : tutorial review" IEEE ASSP Magazine, July 1989
- A.M.Michelson and A.H.Levesque, "Error-control techniques for digital communication", Wiley-Interscience
- John J. Shynk, " Frequency-Domain and multirate adaptive filtering" IEEE SP Magazine, January 92
- Proceedings of the "Third international workshop on Digital Signal Processing Techniques applied to Space Communications", 23-25 September 1992, ESTEC, The Netherlands
- Kamilo Feher, "Wireless digital communications" Prentice-Hall
- Xilinx, Inc., "The programmable gate array data book" San Jose, CA, 1994
- Analog Devices, "ADSP-2106x SHARC user's manual" (3/95)
- I-Cube, "The FPID^{TM} family data sheet", September 1994 (Rev. 3.0)
- Lattice Semiconductor Corp, "Lattice semiconductor Data Book 1996"
- Jim Nagle and George Kinal, "An Inmarsat Geostationary Overlay to GPS and GLONASS" Inmarsat August 1994

CHIPTELOS BLOCK DIAGRAM



Chiptelos prototype



INTEGRATED-CIRCUIT SOLUTIONS

Integrated-Circuit Solutions

Session Chairperson: Mark McDonald,
Linear Technology (Milpitas, CA)

Techniques for Optimizing UHF Front-End Integrated Circuits

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Abstract

This paper discusses S-parameter and related calculations, as well as a method for noise figure calculations, for UHF front-end integrated circuits using the SA621 and SA611 as examples. These devices are high performance low-power communications systems, optimized over the 800-1000MHz range. The SA621 combines a low noise amplifier (LNA), mixer and voltage controlled oscillator (VCO), while the SA611 is a simplified version containing only the LNA and mixer. This paper, however, will focus primarily on matching of the LNA input and output to achieve stability and optimal gain via S-parameters and related calculations. Also discussed is a procedure developed by Philips for obtaining noise figure design data without the use of an automated data-acquisition setup.

Introduction

The high frequency communication industry is growing so rapidly that the design phase of product development is becoming shorter and shorter. Time-to-market is one of the critical factors in the success or failure of a product. Given that, long periods of experimentation are no longer feasible. Designers need quick and reliable ways to evaluate integrated circuit parts and decide which parts are best suited for their products.

One way which trial-and-error experimentation can be reduced is by judiciously using S-parameters. In order to optimize a design, accurate S-parameters may need to be taken when not available from published data sheets. Through use of these measurements, stability can be determined and optimal gain achieved. Another significant way which design uncertainties can be reduced is by an experimental noise figure procedure capable of producing accurate results when automated data-acquisition equipment is unavailable. This paper presents and discusses S-parameters techniques emphasizing analysis readily doable on a hand-held scientific calculator. This is particularly useful for obtaining often-wanted first order design approximations.

SA621/SA611 LNA and S-parameters

To familiarize the reader of the examples to follow, a short description of SA621/SA611 is described. The LNA performance of the SA621 and SA611 are virtually identical. They have an average gain of 15dB with an achievable noise figure of approximately 1.7dB, and an input IP3 of -7dBm over the Advanced Mobile Phones System (AMPS) receive frequency range (869-894MHz). The LNA also performs well in the Industrial, Scientific and Medical (ISM) band (902-928 MHz.).

The LNA S-parameters play a critical role in obtaining optimum gain and noise figure by design. Understanding how they are obtained and what to do with them can greatly decrease the experimental work necessary to make the LNA function properly. Knowing exactly where data sheet S-parameters are measured is the first step in applying them. The SA621/SA611 data sheet records typical measurements taken at *the pins of the IC.* They were obtained using a calibration board designed specifically for this purpose (figure 1). Thus, any matching networks will refer to an actual pin connection on the IC. Measurements were made using a Hewlett Packard network analyzer (HP8753D) to automatically log data over a swept range from 100 to 1200 MHz. This instrument measures reflection coefficients at the ends of its calibrated coaxial connection points. These points are connected to the IC pins through SMA connectors and short PCB microstrip transmission lines. Time delays associated with these connectors and lines at input and output (figure 2a) were rotated out using the "Port Extensions" function located in the "Calibration" menu. Open and short termination results were observed with no chip on the board. If the microstrip transmission line and its associated connector (input or output) have negligible effect on each measurement over this frequency range, then the pad is open circuited and the rotated display should ideally be a single point on the outermost circle of the Smith Chart at $R = \infty$ (figure 2b). When the pad is shorted a similar point would be observed at $R = 0$. Following this port extension calibration, a chip was then soldered onto the calibration board and actual S-parameter data automatically gathered. Note that these parameters cannot be obtained from the functional demonstration (demo) board because it has external matching networks and transmission lines.

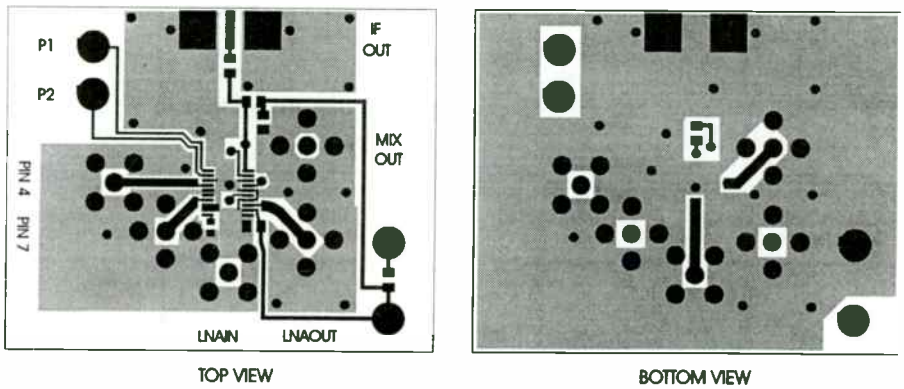

Figure 1. Calibration board layout.

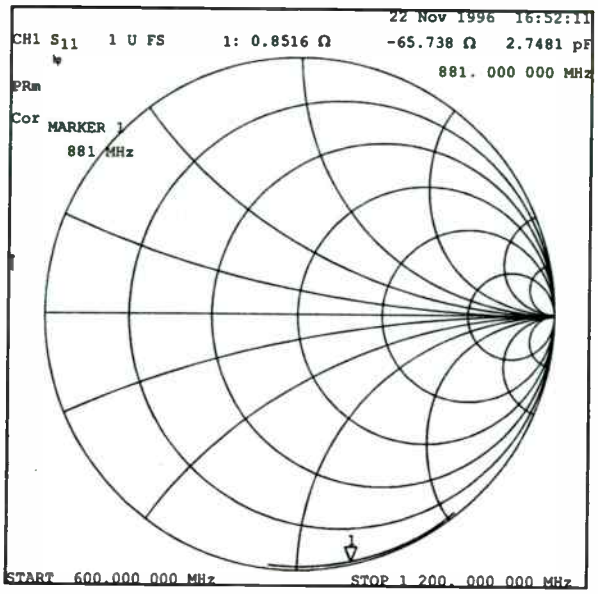

Figure 2a. HP output before rotation.

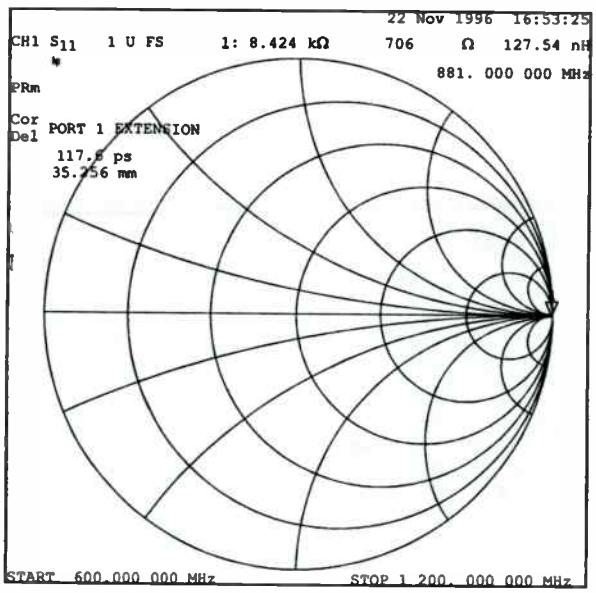

Figure 2b. HP output after rotation.

Measured LNA input and output S-parameters (S_{11} and S_{22}) are shown below (figures 3a and 3b). A full set of S-parameter data is found in the SA621 and SA611 data sheet.

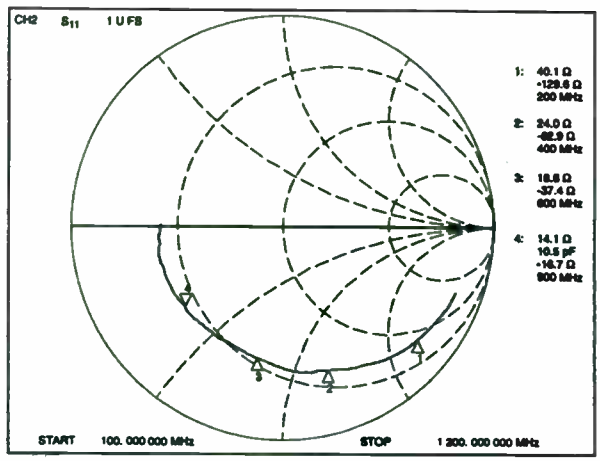

Figure 3a. S_{11} (input) data.

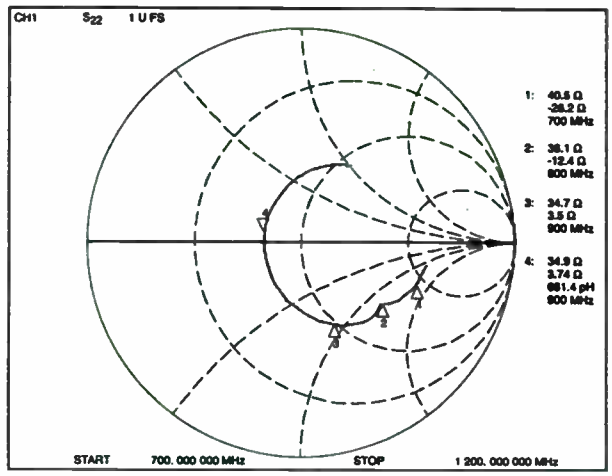

Figure 3b. S_{22} data.

Data sheet S-parameters only inform us of the LNA's performance when the source and load terminations are 50 Ohms. Since the input and output impedances of this device are not 50 Ohms, some return loss will be associated with the mismatch to 50 Ohms at each port. These losses can be eliminated simply by conjugately matching each of them to 50 Ohms. The standard first-order equation describing the resulting maximum unilateral gain (G_{umax}) is given by (1.1a) below (many good references exist treating the theory and practice of S-parameters; for our purposes, the best are [1] and [2]).

$$G_{u\max} = \frac{1}{1-|S_{11}|^2}\,|S_{21}|^2\,\frac{1}{1-|S_{22}|^2},\ (S_{12}=0) \qquad (1.1a)$$

This equation assumes the LNA is unconditionally stable when conjugately matched. The first and last terms describe the result of conjugately matching both the input and output ports respectively, thereby gaining back the losses due to mismatches present when S_{11} and S_{22} were determined at whatever impedance they were measured at, 50 Ohms with the network analyzer in this case. It should be clear that if both LNA ports miraculously exhibited 50 Ohm impedances, S_{11} and S_{22} would be 0 (no reflections!) and these terms would reduce to unity leaving only $|S_{21}|^2$, the unilateral transducer gain (remember, since scattering parameters are voltage ratios, they must be squared to obtain power). This term is an invariant

property of the LNA itself that depends externally only on frequency but not source and load terminations. Finally, this is a *practical* equation since it assumes that the reverse transmission gain is zero ($S_{12} = 0$), making the device *unilateral.* Specifically, it does not account for the fact that when the load termination changes S_{11} also changes slightly and vice-versa.

The complete expressions for the non-unilateral or *bilateral* maximum gain G_{max} when $S_{12} \neq 0$ are:

$$G_{max} = \left|\frac{S_{21}}{S_{12}}\right| \left(K + \sqrt{K^2 - 1}\right) \text{ when } B < 0 \tag{1.1b}$$

$$G_{max} = \left|\frac{S_{21}}{S_{12}}\right| \left(K + \sqrt{K^2 - 1}\right) \text{ when } B < 0, \tag{1.1c}$$

where the parameter $B = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$, and K and Δ are from (1.2) and (1.3) following. G_{umax} is much easier to calculate, and usually it is close enough to the actual value G_{max} to warrant using it as a good approximation for design purposes.

Stability

As noted above, (1.1a,b,c) can only be used if the amplifier in question is stable when conjugately matched. Some amplifiers will oscillate with certain source and load terminations; these devices are *conditionally stable.* Otherwise, they are *unconditionally stable* since no passive source and load terminations exist that will cause oscillation. Stability is easily determined from measured S-parameters. This involves finding a stability factor K (scalar number) and Δ (a complex number), where

$$K = \frac{1+|S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{21}|} = \frac{1+|\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{21}|} \tag{1.2}$$

and

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{1.3}$$

If $K > 1$, the device will be *at least* stable when simultaneously conjugately matched to 50 Ohms, and G_{umax} or G_{max} can then be found. If $K > 1$ *and* $|\Delta < 1|$, then the device is also unconditionally stable with any termination. Note that K only tells us whether the device is stable when conjugately matched to the same characteristic impedance used to obtain the measured S-parameters, usually 50 Ohms. The SA621/611 LNA is unconditionally stable at all frequencies between 100 and 1200 MHz.

Conditionally stable devices require further analysis to determine regions on the Smith Chart where they are stable. This is done by determining classic *source* and *load* stability circles. Not only must their location and radii be determined, but whether regions inside or outside them constitute stability terminations. This treatment is beyond the scope of this paper and will not be discussed here. Those interested in an excellent and readable treatment should refer to [2] as a good example.

Example -1

Example showing the LNA to be unconditionally stable at 870 MHz:

Substitute S-parameters from Table 1 below into stability equations (1.2) and (1.3).

$\|S_{11}\|$	$\angle°$	$\|S_{12}\|$	$\angle°$	$\|S_{21}\|$	$\angle°$	$\|S_{22}\|$	$\angle°$
0.596	-135.8	0.027	111.9	4.81	26.9	0.179	-175.1

Table 1. S-parameter data at 870 MHz.

Find $|\Delta|$ first, then stability factor K:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$$

$$|\Delta| = |0.596 \cdot 0.179\angle(-135.8 - 175.1) - 0.027 \cdot 4.81\angle(111.9 + 26.9)| = 0.168$$

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{21}|}$$

$$K = \frac{1 + 0.168^2 - 0.596^2 - 0.179^2}{2 \cdot 0.027 \cdot 4.81} = 2.25$$

Since $K > 1$ and $|\Delta < 1|$, the LNA is unconditionally stable at 870 MHz.

Thus, the maximum unilateral gain can be found from (1.1a),

$$G_{u\max} = \frac{1}{1 - |S_{11}|^2} |S_{21}|^2 \frac{1}{1 - |S_{22}|^2} = (1.551)(4.81)^2(1.033) = 37.1 = 15.69 \text{ dB}$$

and the bilateral gain from (1.1b,c), found by computer,

$$G_{\max} = 15.77 \text{ dB}.$$

These two results differ by less than 0.08 dB and show the value of the simpler unilateral form. Note also that gain measured by the network analyzer would be just $10\log\left(|S_{21}|^2\right) = 13.6$ dB. Thus, we conclude that without any matching (50 Ohm source and load terminations) we can expect a gain of 13.6 dB, while the most obtainable under any matching conditions is about 15.8 dB.

Gain and Noise Circles

Input gain and noise circles plotted on the Smith Chart greatly facilitate the design of input matching networks by graphically showing a designer the tradeoff between any particular gain and some wanted noise figure. We will first discuss input gain circles and then noise circles after that. Because of the calibration board, accurate S-parameter data is referred to the physical pins of the IC. From these measured S-parameters, LNA gain can be calculated for *any* matching network attached to either the input or output pins.

Consider the case when the input matching network has a source reflection coefficient Γ_S (scattering parameter looking *into* the *output* of the network connected to the LNA input pin) equal to the conjugate of the input reflection coefficient S_{11} (scattering parameter seen looking *into* the LNA input IC pin) (figure 4).

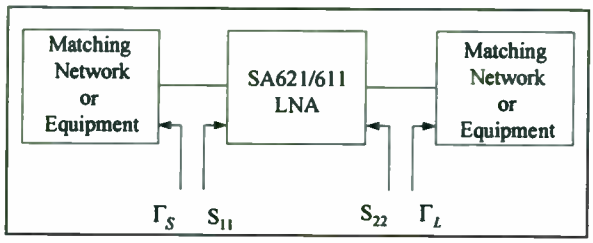

Figure 4. Amplifier setup.

Thus,

$$\Gamma_S = S_{11}^{*}, \quad \text{unilateral device } (S_{12} = 0). \tag{1.4a}$$

$$\Gamma_S = \left(S_{11} + \frac{S_{12}S_{21}\Gamma_S}{1-\Gamma_L S_{22}} \right)^{*}, \quad \text{bilateral device } (S_{12} \neq 0). \tag{1.4b}$$

This condition will plot Γ_S as a single point on the Smith Chart that can be used to design a suitable matching network to whatever source is driving the network's input, typically 50 Ohms. Note that (1.4a) is quite simple and often differs little from (1.4b), especially for quick estimations. Comparison of (1.4a) and (1.4b) clearly shows the effect the load has on the LNA input when $S_{12} \neq 0$.

If a similar procedure is used to match the output, we have the unique situation described by any (1.1) equations, where the LNA exhibits its maximum possible gain, $G_{u\max}$ If we stipulate that the output always remain conjugately matched, but introduce a deliberate input mismatch, the gain G will obviously be less than the maximum possible. For any particular $G < G_{\max}$, many different Γ_S exist that will result in this same gain. It can be shown that the locus of these various Γ_S all lie on a single circle on the Smith Chart [1] [2]. Therefore, choosing any point on this circle defines a particular matching network all of which yield the same return loss or mismatch and thus the same gain G. In the time domain, this simply means the amplitude ratio of the forward and reverse traveling waves remains unchanged, but the phase between them will be different for each point on the circle.

Calculating input gain circles can be accomplished using either simplified unilateral equations or the more complicated bilateral forms. The former are useful for practical designs and can easily be done by any good engineering calculator. Hewlett Packard's classic *HP Application Note 154* [1], for example, covers these unilateral forms quite nicely. Reference [2] contains a well-developed complete treatment for an actual bilateral device like the SA621/SA611, and are most suitable when done by a computer or calculator program.

Since the device will no longer be conjugately matched, (1.5) expresses the unilateral gain form of (1.1a) rewritten for *any* source or load terminations:

$$G_u = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}\,|S_{12}|^2\,\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \qquad \text{where } G_u \text{ is always} \le G_{u\max}. \qquad (1.5)$$

As stated earlier, the output will remain conjugately matched; only the input mismatch will be varied through Γ_S. For this special case, (1.5) becomes:

$$G_{su} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}\,|S_{12}|^2\,\frac{1}{|1-S_{22}|^2} \qquad (1.6)$$

Since any arbitrary value of G_{su} is between 0 and G_{umax}, solutions for Γ_S lie on a circle. We can choose any Γ_S and calculate its gain (G_{su}). So if we choose Γ_S along a 15.2dB circle, we would have a G_{su} of 15.2dB. Equations (1.7 - 1.9) from [1] determine where a gain circle can be found on the Smith Chart.

$$d_{ui} = \frac{g_{ui}|S_{11}|}{1-|S_{11}|^2(1-g_{ui})} \angle\, S_{11}^{*}, \quad \text{gain circle center} \qquad (1.7)$$

$$R_{ui} = \frac{\sqrt{1-g_{ui}}\,(1-|S_{11}|^2)}{1-|S_{11}|^2(1-g_{ui})}, \quad \text{gain circle radius} \qquad (1.8)$$

where g_{ui} is a parameter expressing the gain circle's wanted gain G_{ui} normalized to $G_{u\max}$.

$$g_{ui} = G_{ui}(1-|S_{11}|^2) = \frac{G_{ui}}{G_{u\max}} \qquad (1.9)$$

Note that d_{ui} is the distance from the center of the Smith Chart to the center of the gain circle along the conjugate S_{11} vector (S_{11}^{*}) and R_{ui} is the radius of the circle at that point.

Example 2:

Calculate and plot on the Smith Chart an input gain circle 0.5dB below the maximum gain for the SA621/SA611 at 870 MHz using the simplified unilateral assumption and compare it to the general bilateral case.

Begin by finding g_{ui}:

$$g_{ui} = G_i(1-|S_{11}|^2) = \frac{G_i}{G_{u\max}}$$

Choose $G_i = G_{u\max} - 0.5$ dB = 15.7 dB - .5 dB = 15.2 dB.

Linearize the gain and find g_{ui}:

$$g_{ui} = 10^{\frac{15.2-15.7}{10}} = 0.891$$

Find the center, C_{ui}:

$$C_{ui} = \frac{g_i |S_{11}|}{1-|S_{11}|^2\left(1-g_{ui}\right)} \angle S_{11}^{*}$$

$$C_{ui} = \frac{(0.891)(0.596)}{1-(0.596)^2(1-0.891)} \angle -(-135.8)^{\circ} = \frac{0.530}{0.9614} \angle 135.8^{\circ} = 0.55 \angle 135.8^{\circ}$$

Find the radius, R_{ui}:

$$R_{ui} = \frac{\sqrt{1-g_{ui}}\left(1-|S_{11}|^2\right)}{1-|S_{11}|^2\left(1-g_{ui}\right)} = \frac{\sqrt{1-0.891}\left(1-(0.596)^2\right)}{0.9614} = 0.22$$

Thus, the center will be located at $0.55 \angle 135.8^{\circ}$ with radius of 0.22.

Compare this result with a computer derived bilateral center and radius for the same G_{max} - 0.5 dB gain circle [2]:

Gain Circle for G_{max} - 0.5 dB = 15.3 dB

$d_{Ci} = 0.56 \angle 133.4^{\circ}$

$R_{Ci} = 0.22$

The radii are equal with the centers differing only slightly and the gains by 0.1 dB. Now that all the information is found, a designer can draw these gain circles on the Smith Chart for visual comparison. Figure 5 shows these two gain circles plotted on the Smith Chart.

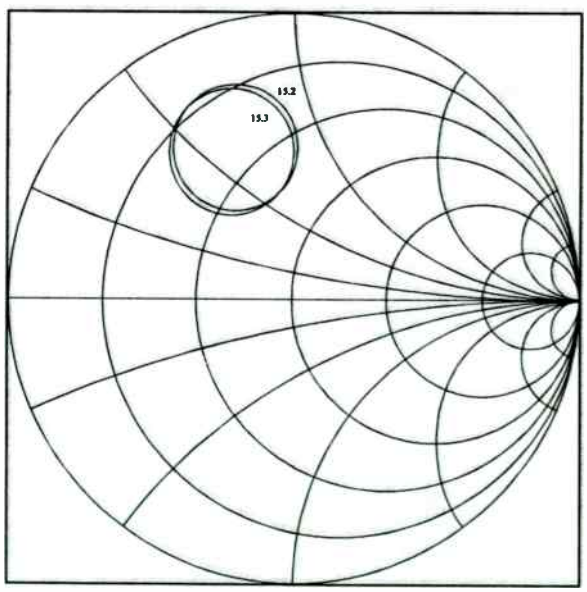

Figure 5. Plot of example-1: unilateral and bilateral gain circle.

Noise Figure Circles

Noise factor NF is defined as the ratio of the signal-to-noise ratio at the input to the signal-to-noise ratio at the output,

$$NF = \frac{S_i/N_i}{S_o/N_o}$$

It is always greater than 1 for practical devices. Noise figure F is simply NF expressed in dB, $F = 10\log(NF)$. Note that a perfect device having no internal noise generation has noise factor of 1 which yields a noise figure of 0 dB.

The LNA noise figure depends on the source impedance connected to its input port and frequency of operation. Further, the minimum noise figure, F_{min}, increases monotonically with frequency. Like most devices, F_{min} does not occur when the source is 50 Ohms. Thus, if a designer conjugately matches the input to realize maximum gain, observed noise figure F will be greater than F_{min}. How much greater? Similar to gain circles, noise circles can also be determined and plotted as an indispensable design aid to answering this question. Each circle describes a locus of source reflection coefficients Γ_S all having a constant $F > F_{min}$. Essentially, this is the same thing we did for gain circles except here the parameter is noise figure rather than gain.

Remember that gain circles are found by calculation employing the four basic S-parameters known at a particular frequency. Noise figure circles are based on three additional parameters: F_{min} at Γ_{min} and R_n. If these are not known and a designer does not have automated testing equipment, accurately determining them can be an exacting and time-consuming chore. An experimental method for obtaining them is presented in *Hewlett Packard Application Note 154* [1]. This method requires two basic measurements: One to determine what input reflection coefficient $\Gamma_s = \Gamma_{min}$ is required for best noise figure F_{min} and one additional point used to find the equivalent noise resistance R_n, described below in (1.10). The value and limitations of this method when applied to the LNA will be discussed later. After obtaining these quantities, any wanted noise circle may be found and plotted on the Smith Chart.

The following equation [1][2] expresses the fundamental relation between any noise figure F and the minimum noise figure F_{min} (at Γ_{min}) as a function of Γ_S.

$$F = F_{min} + 4r_n \frac{|\Gamma_s - \Gamma_{min}|^2}{|1 + \Gamma_{min}|^2 (1 - |\Gamma_{min}|^2)} \tag{1.10}$$

where

$$r_n = \frac{R_n}{Z_o} \tag{1.11}$$

F	noise figure ≥ F_{min}
Γ_S	source reflection coefficient at F
F_{min}	minimum noise figure possible for the device
Γ_{min}	source reflection coefficient at minimum noise figure
R_n	equivalent noise resistance in Ohms
Z_o	characteristic impedance of system, usually 50 Ohms
r_n	normalized equivalent noise resistance

Note that R_n is a parameter having dimensions of Ohms. It is *not* the actual Thevenin source resistance required for minimum noise figure; that can be found from Γ_{min}. Rather, it is a scalar factor gauging the

dependence of F on Γ_S. This should be evident by inspection of (1.10). Also, Smith Charts usually have the center normalized to be 1 Ohm, so only normalized quantities can be plotted. Thus, the normalized equivalent noise resistance r_n must be found.

Once r_n is found, it is used with Γ_{min} and F_{min} to determine a family of circles representing different noise figures found by applying (1.13) and (1.14) for each one as follows.

$$C_{Fi} = \frac{\Gamma_{min}}{1+N_i} \qquad \text{noise circle center} \qquad (1.12)$$

$$R_{Fi} = \frac{1}{1+N_i}\sqrt{N_i^2 + N_i\left(1-|\Gamma_{min}|^2\right)} \qquad \text{noise circle radius} \qquad (1.13)$$

where

$$N_i = \frac{F_i - F_{min}}{4r_n}\left[1+\Gamma_{min}\right], \qquad F_i > F_{min} \qquad (1.14)$$

C_{Fi} determines where the noise circle is located, and is found by measuring $|C_{Fi}|$ from the center of the Smith Chart along the vector $\angle C_{Fi}$. R_{Fi} is the radius of the circle then constructed at that point. Note that S_{12} does not appear in these equations (1.10 to 1.14), so these apply to both unilateral and bilateral devices.

The necessary parameters were determined using the following setup:

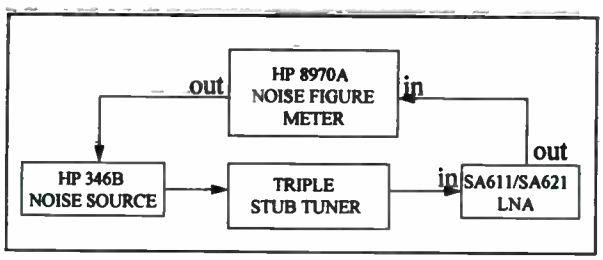

Figure 6a. Noise Circle Setup for measuring noise figure.

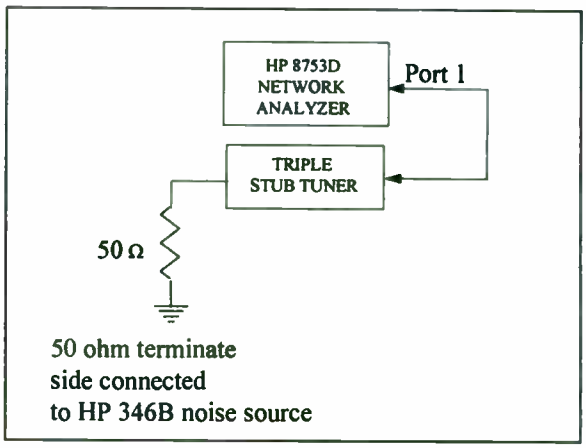

Figure 6b. Noise circle setup to determine location.

The setup consists of two major pieces of equipment, a noise figure meter and a network analyzer and follows the general method discussed in *Hewlett Packard Application Note 154* [1]. The following is for those familiar with test procedures when measuring source reflection coefficients, Γ_S. The point to remember, here, is we are finding reflection coefficients looking *into* the *output* of the network that was connected to the *input* of the LNA. When we measure Γ looking into the LNA we label it S_{11}. When we measure Γ looking into the output of a network attached to the LNA's input, we label it Γ_S.

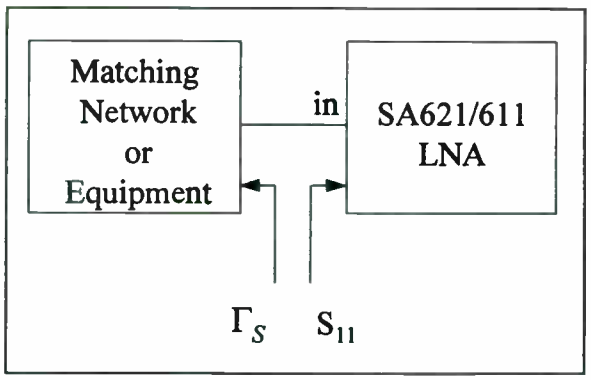

Figure 7. Input matching network showing source reflection coefficient Γ_S and input reflection coefficient S_{11}.

1. Using the noise figure meter (Figure 6a), find the minimum noise figure F_{min} of the device by carefully tuning the triple-stub tuner. Most noise figure meters express to 3 significant digits (e.g. 1.73 dB), so some physical interpolation of the stub elements may be necessary to set the triple-stub to a good estimate of where the minimum actually occurs. The reflection coefficient looking into the stub will be equal to Γ_{min}.

2. To measure Γ_{min}, connect a 50 Ohm termination to the triple-stub tuner on the *same* side where the noise source was connected (Figure 6b). Measure the reflection coefficient Γ of the tuner on a network analyzer. This will be the same as $\Gamma_S = \Gamma_{min}$. Note that on the HP8753D network analyzer Γ is displayed when the format is "Polar". If the format is "Smith", then the display will give impedance Z even though the reflection coefficient plane is actually being displayed. The formulas require reflection coefficients not impedances. However, one can easily convert Z to Γ by using the familiar relation:

$$\Gamma = \frac{Z_s - Z_L}{Z_s + Z_L} \tag{1.15}$$

where, Z_S and Z_L are the source and load impedance, respectively. Because the HP network analyzer normalizes to 50 ohms, the equation becomes:

$$\Gamma = \frac{Z_s - 1}{Z_s + 1} \tag{1.16}$$

3. This procedure can be repeated for measurements of different noise figures, not just F_{min}.

4. Please keep in mind that *any* added lengths and attenuations need to be *accurately* accounted for. Depending on hardware, this can be tedious and complicated. For a simple example, if a barrel is attached to the triple-stub tuner (that was not used when the stub was connected to the LNA) to obtain Γ_S , it will exhibit some time delay causing rotation on the Smith Chart as well as attenuation. Particular attention must be given to attenuations not accounted for when the noise figure apparatus was calibrated. Thus, attenuations of *all additional* RF hardware needs to be accounted for: including the stub-tuner, barrels etc. Since errors of 0.05 dB will typically observable changes in the diameter of plotted noise circles. There is no substitute for experience when dealing with these quantities.

Example-3

Using the described noise circle setup, determine and plot the 2.0 dB noise circle on the Smith Chart for the SA621/SA611 at 881 MHz.

This is accomplished by using the triple-stub tuner to find all the necessary variables mentioned above. Following the HP procedure as a guide, we first find F_{min} and Γ_{min} using the noise figure meter and triple-stub tuner. Finding r_n requires another determination of any F and its associated Γ_S. Eqn. (1.10) is then solved for r_n, the named quantities substituted and r_n found. The HP procedure uses an especially simple and mathematically convenient way for finding this by letting $\Gamma_S = 0$; this occurs when the source termination is 50 Ω, or just the noise figure reading *without* the triple-stub tuner. This makes sense, but unfortunately does not work well with the SA621/SA611 LNA. It turns out the two noise figures are quite close, F_{min} and F at 50Ω, and each of these is expressed to only three significant figures; after linearizing their decibel forms, the resulting numerical error can be quite large. Further, the uncertainty in finding Γ_{min} with the stub tuner contributes to a larger overall uncertainty. Using this method, R_n has been observed to vary between 3 and 20 Ω, an unacceptably large variance. Philips has developed a better method to experimentally determine and verify these parameters.

The two re-written forms of (1.10), general and special cases respectively, solved for r_n, are given as:

$$r_n = \frac{\left(F - F_{min}\right)\left(|1 + \Gamma_{min}|^2 \left(1 - |\Gamma_s|^2\right)\right)}{4\left(|\Gamma_s - \Gamma_{min}|^2\right)} \tag{1.17a}$$

$$r_n = \frac{\left(F - F_{\min}\right)\left(|1+\Gamma_{\min}|^2\right)}{4\left(|\Gamma_{\min}|^2\right)}, \qquad \text{when } \Gamma_s = 0 \tag{1.17b}$$

Eqn. (1.17b) is used with the HP procedure, while (1.17a) the Philips procedure. Additional measurements are taken at random noise figures, ideally scattered around the Smith Chart, each yielding an associated R_n found by applying (1.12a) and multiplying by Z_o. Simple mean and variance or sample standard deviation are then calculated for the ensemble of R_n. The mean is taken to be the best estimate of R_n. Further, inspection of the R_n series can usually pin-point experimental errors when especially bad points turn up.

Assuming rotations and attentions have been properly accounted for (see point 4 above), the weak point in this procedure is the estimate of $\Gamma_{\min}$ since it is based on only one measurement subject to considerable error. This fact can only be appreciated by actually doing the laboratory measurement and getting a feel for the latitude one has in setting the triple-stub tuner at minimum noise figure. A further refinement is then possible using the measurement series of ordered pairs F and Γ_s for each R_n. A gradient search algorithm can be developed that finds a better estimate of $\Gamma_{\min}$ based on minimizing the ratio of the mean to variance of the ensemble R_n for each candidate $\Gamma_{\min}$. Clearly, this is not suitable for hand calculator computations, but is easily done by a computer. First order approximations suitable for experimental design may be composed of several (at least 3) measurements for F and Γ_s to ascertain "whether we are in the ballpark" in the value settled upon for R_n. This is easily done on a hand calculator or with computer assistance using such common programs as Matlab.

Let's continue with this example using the Philips' method. A particular session in the screen room yielded the following actual set of experimental measurements using the calibration board for the LNA at 881 MHz:

n	F(dB)	Gamma	
Sample	Noise Figure	Magnitude	Angle
1	1.60	0.170	126.1
2	4.53	0.737	15.0
3	3.15	0.551	-96.8
4	2.04	0.320	-131.1
5	2.45	0.428	-105.6
6	3.89	0.684	-102.2
7	3.38	0.706	-165.0
8	1.73	0.058	-91.0

Table 2. Noise figure measurements for nine samples.

Sample calculation using (1.17a) for $F = 2.03$ dB at $\Gamma_s = 0.32\angle -131.1^\circ$,

$$r_4 = \frac{\left(\log^{-1}\left(2.03/10\right) - \log^{-1}\left(1.60/10\right)\right)\left(|1\angle 0^\circ + 0.170\angle 126.1^\circ|^2\,(1-|0.32|^2)\right)}{4\left(|0.32\angle -131.1^\circ - 0.170\angle 126.1^\circ|^2\right)} = \frac{(0.150)(0.791)(0.898)}{4(0.131)}$$

$$r_4 = 0.203\ \Omega$$

$$R_4 = r_4 Z_o = (0.203)(50) = 10.2\ \Omega$$

Using a computer, better estimates of Γ_{min} and R_n were found to be:

$$\hat{\Gamma}_{min} = 0.174\angle 131.6^{\circ}, \text{ so } \hat{R}_n = 9.0\ \Omega$$

To find the 2.0 dB noise figure circle we apply eqns.(1.12-1.14) using the non-optimized values for Γ_{min} and R_n for comparison purposes.

Find parameter N_i:

$$N_i = \frac{F_i - F_{min}}{4r_n}\left[1+\Gamma_{min}\right]$$

$$N_i = \frac{\log^{-1}\left(2.0/10\right) - \log^{-1}\left(1.60/10\right)}{4\left(10.2/50\right)}\left|1\angle 0^{\circ} + 0.170\angle 126.1^{\circ}\right|^2 = \frac{(0.140)(0.791)}{0.816} = 0.135$$

Find where the noise circle is centered, C_{Fi}:

$$C_{Fi} = \frac{\Gamma_{min}}{1+N_i} = \frac{0.170\angle 126.1^{\circ}}{1.135} = 0.150\angle 126.1^{\circ}$$

Find the noise circle's radius, R_{Fi}:

$$R_{Fi} = \frac{1}{1+N_i}\sqrt{N_i^2 + N_i\left(1-|\Gamma_{min}|^2\right)} = 0.881\sqrt{0.149} = 0.340$$

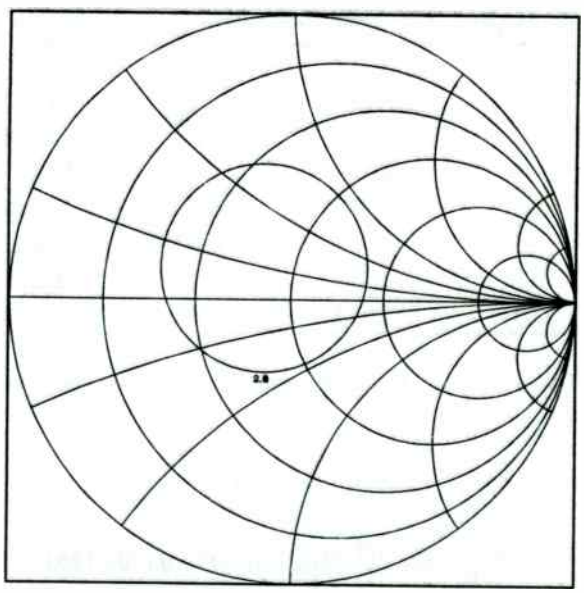

Figure 8. 2.0 dB noise circle at 881MHz.

Piecing everything together

When gain circles, noise figure circles, and stability are all determined the designer is ready to design a match to realize an optimal noise figure and gain. Figure 9 shows the combined gain and noise circles on a single Smith Chart computed for 881 MHz. The noise circles were found from the data set in example 3 above with Γ_{min} and R_n optimized by a gradient search algorithm with the experimental data from Table 2. Compare especially the 2.0 dB noise circle with that found using the non-optimized Γ_{min} and R_n from example 3 shown in figure 8. The optimized location for this circle is $\hat{C}_{Fi} = 0.151\angle 131.6^{\circ}$ with a radius $\hat{R}_{Fi} = 0.361$.

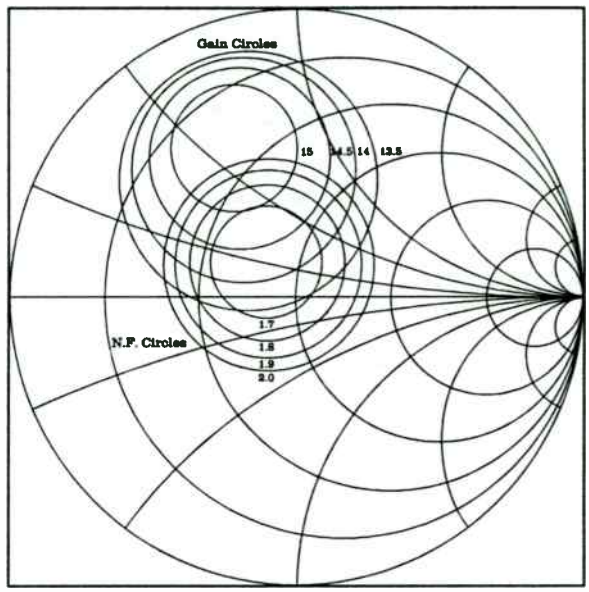

Figure 9. Noise and Gain Circles at 881 MHz.

Since the LNA is unconditionally stable at 881 MHz , there are no matching conditions that will cause it to oscillate. Therefore, interpreting the data in figure 9 is easy: any input reflection coefficient Γ_s can be located as a point on the Smith Chart. The gain and noise circles tell us immediately what the expected gain and noise performance will be at this point, and we can proceed to design a suitable input matching network to realize this particular Γ_s.

Say a designer wants a noise figure of 1.8dB and a gain of 15dB when the source driving the LNA input is 50 Ω. On the Smith Chart, this noise figure and gain point are at approximately $Z_s = 31 + j20\ \Omega$. Since the LNA "sees" Γ_s, we begin from the center of the Chart, corresponding to the source of impedance of 50 Ω and move using suitable series or shunt elements to the Γ_s point. Thus, we choose components to match to the ending point (connected to the input of the LNA). Usually, more than one solution exists. In this case shunt C and series L are used. (figure 10).

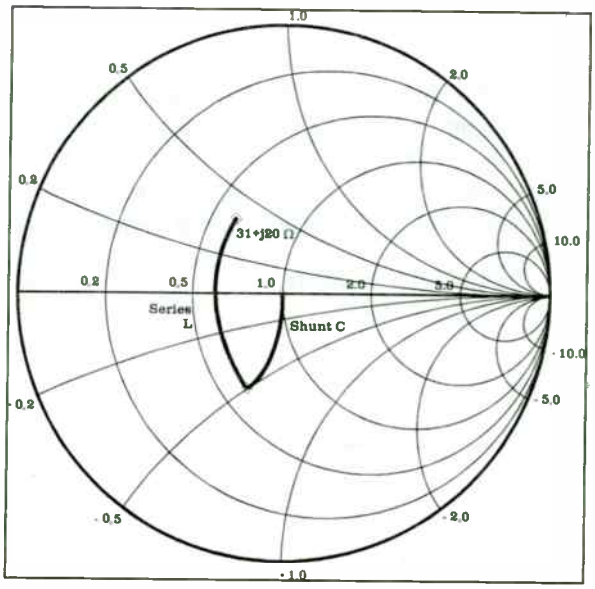

Figure 10. Smith chart display of matching.

The circuit to match the input of the LNA is seen in Figure 11.

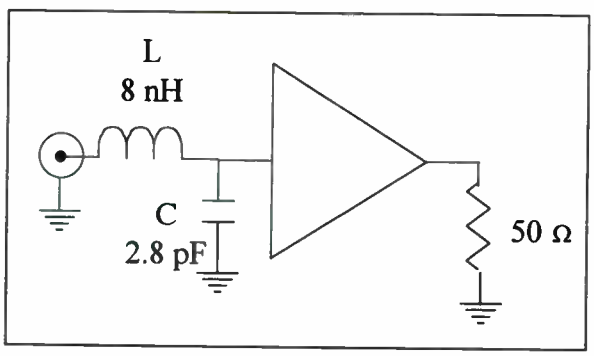

Figure 11. LNA input matching.

Application Demonstration Board (Demo Board)

By conjugately matching the output port to 50 Ohms, a designer can easily improve the gain since test equipment is usually terminated at 50 ohms and also most image rejection filters have 50 ohms terminations.

On the application board however, no output matching was used because the standing wave ratio without it is no more than 2, so 0.5dB at most will be lost. However, a designer could improve the output match by 0.4dB by using the low pass circuit below (figure 12), which also has the advantage of reducing high frequency noise. One is not constrained to use only this circuit, but may choose to use a high pass circuit which uses one less external component if parts count is more important than noise filtering.

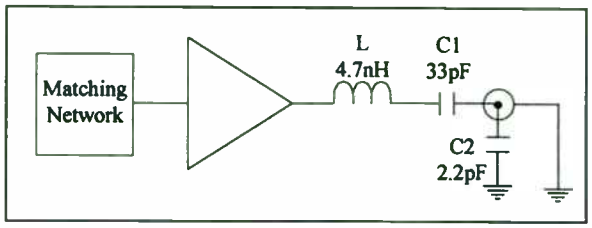

Figure 12 LNA output circuit

The input matching circuit (figure 13) is basically a simple shunt L match. The network may seem theoretically trivial but its realization is not. For example, placement of a size 0805 SMD inductor is critical because the necessary interconnecting transmission lines and the spatial size of the inductor itself will rotate the theoretical point to another position on the Smith chart. Therefore, the actual impedance being matched will vary depending on where the designer places the 6.8nH inductor with respect to the LNA input pin. This is always a consequence of using lumped parameter solutions at microwave frequencies rather than transmission line segments; the advantage is reduced board space at the expense of greater difficulty in getting the match to work properly. These devices should be as small as possible consistent with wanted efficiency or element Q. Inductors are typically size 0805 or larger while capacitors are 0603 or larger.

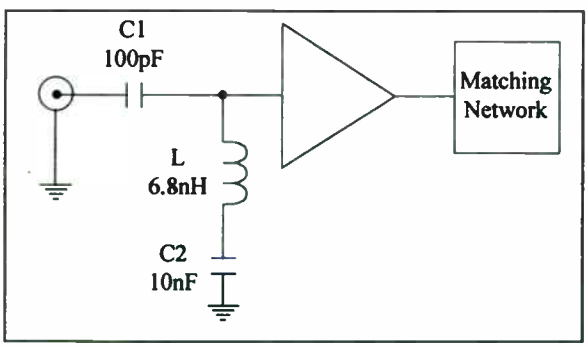

Figure 13. LNA Input Match

Note that the input matching network also includes a 100pF capacitor for DC blocking as well as a 10nF capacitor. The 10nF capacitor plays two roles in this circuit. First, DC-wise, the capacitor prevents shorting the DC bias potential present on the input pin through the 6.8nH inductor. Second, the 10nF capacitor introduces destructive phase correlation between the third order intermodulation products present at the input and output thus improving the overall LNA IP3 performance. As this capacitor is increased, IP3 improves at the expense of LNA power-up turn-on time (turning on the LNA after powering it down). Table 3 shows the compromise between turn-on switching time and input IP3.

RF Input Level = -30dBm			
Capacitance	IP3in	Gain	Switching Time
10nF	-7.5	15	84uS
22nF	-6.3	14.8	220uS
47nF	-5	15	490uS
100nF	-5	15	720uS

Table 3. LNA input IP3 vs switching time.

Layout

With any UHF RF application, layout is critically important to circuit performance. For matching and RF signal routing, board traces must be viewed and treated as transmission lines or antenna segments. As transmission lines, they affect nodal impedances (impedance at any point on the segment or at its ends) and cause rotations on the Smith Chart. The most common model treats them using classic microstrip theory where they are implemented as traces over a single ground plane. Without a ground plane, a microstrip becomes a trace or wire behaving as an antenna segment susceptible to unwanted coupling and radiation. Thus, designer's must account for length and width of traces as well as their proximity and relation to associated ground planes. Generally, narrow traces should be avoided because of their high characteristic impedance, greater phase delay and radiation losses. The demo board has microstrip lines connected to both ports of the LNA with associated ground planes on opposite sides of the board. Their lengths were kept as short and as wide as practical. Since truly 50 Ohm lines are impractical, being over 100 mils wide on 62 mil thick FR4/5 PCB, the demo board uses traces having characteristic impedances between approximately 75 and 90 Ohms. This makes introducing lumped matching elements simple, because they have predictable electrical length (phase delay) and low radiation thereby improving isolation and minimizing unwanted coupling. Discrete capacitors or inductors should generally be mounted over a ground plane for best isolation. Radiation, especially from inductors, may also need to be taken into account. A FET probe on a spectrum analyzer can be useful in determining whether such elements need shielding or re-location. Elements carrying comparatively high RF currents, in oscillator tank circuits for example, will nearly always require shielding for good isolation and spurious radiation attenuation.

Good port-to-port isolation is necessary to minimize unwanted output-to-input feedback that might result in parasitic oscillations or poor stability. Poor isolation also increases the affect of output termination on the actual input impedance of the device and vice-versa, modifying the actual S_{11} and S_{22} seen at input and outputs respectively with particular port terminations. Essentially, this modifies S_{12}. This can make realizing a particular gain and noise figure by design difficult or impossible.

Board layout will always degrade isolation. For example, on the SA621/SA611 demo board, the LNA input is pin 15 and the output pin 13. Since these pins are so close together, special attention must be given to obtaining good isolation between them. This is best accomplished by having the input and output ports on opposite sides of the board to take advantage of ground plane isolation. This layout achieved more than 25dB of isolation. Since the LNA's internal isolation is about 17 dB, this layout minimally degraded S_{12}.

Another aspect to the layout is proper RF ground returns to the LNA, pins 14 and 16 are the essential ground returns. Input RF currents should return to pin 14 while output RF currents should return to pin 16. One must keep the ground lengths associated with these port's external components as short as physically possible. Failure to do this can result in poor isolation, instability, and parasitic oscillations.

Conclusion

This paper has presented a review of RF amplifier matching network design from a practical standpoint using S-parameters. For simplicity, unconditionally stable devices were considered, although the methods could easily be extended to conditionally stable devices as well. The Philips SA621/SA611 integrated UHF front-end chip was presented as a typical device. Stability, input gain circles and noise circles were defined with examples for each. We note that output gain circles are also obtainable using techniques similar to those employed to finding input gain circles, but this topic was not treated, since they are usually not required. However, the utility of input gain circles is obvious owing to their immediate value in graphical comparison to noise circles, as both types vary with changes in the input reflection coefficient Γ_S. Also, since useful noise performance data is often lacking in published device data sheets, an experimental method was presented that makes obtaining them for design purposes reasonably quick and accurate. Interested designers can easily construct calibration boards for rapid in-house evaluation of candidate devices when data sheet S-parameters or noise data are deemed insufficient for a particular application.

Layout and construction issues were also discussed from the standpoint of exploiting hybrid designs using a mix of transmission line segments and classic low-frequency lumped parameter elements in the form of surface mount inductors, resistors and capacitors. This technique can save considerable PC real-estate but suffers from requiring much time to realize a suitable design. Understanding S-parameters, the Smith Chart, and layout issues can greatly decrease development or evaluation time without expensive simulation packages.

REFERENCES

[1] Hewlett Packard, "Application Note 154. S-Parameter Design", April 1972; revised May 1973.

[2] Ha Tri T. "Solid-state microwave amplifier design", John Wiley & Sons, Inc. 1981, ISBN 0-471-08971-0.

[3] Fish, Peter J., "Electronic Noise and Low Noise Design", Mc. Graw Hill, 1994, ISBN 0-07-021004-7.

A HIGHLY INTEGRATED DECT RADIO TRANSCEIVER

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Abstract

A complete radio transceiver solution for the Digital Enhanced Cordless Telecommunications (DECT) standard demonstrating a high level of integration along with reduced component count and board size has been constructed. A single conversion receiver and a direct conversion transmitter has been fabricated on a single integrated circuit (IC). The architecture and functionality of the system blocks are described in detail. In addition, the performance of the transceiver is evaluated including sensitivity, and bit error rate (BER).

This paper concentrates on details of the various circuit blocks in a complete DECT transceiver solution. The second section of this paper will describe the enabling BiCMOS transceiver IC. Section three will present the performance of the transceiver as used in the DECT system, notably -92 dBm sensitivity at BER< 0.001. Conclusions will be drawn about the impact on size, cost, and performance of mobile terminals.

I. Introduction

The roadmap in new digital communications system development is leading towards smaller size, lighter weight, and lower price, without sacrificing performance. For products to survive in the highly competitive commercial world of cordless telephones, it is necessary for new generations to be high performance, pocket sized and cost sensitive. This presents an ever increasing challenge for semiconductor manufacturers since the biggest cost savings is attained by integrating more and more subsystems onto one piece of silicon. This trend is especially true for consumer telecommunications products where semiconductor suppliers are working to put complete radio transceivers on a single integrated circuit (IC).

In previous generation DECT radio solutions, many separate IC's were fabricated for the various radio components. A new IC combines both receive and transmit functions onto a single piece of silicon. A single chip transceiver has been developed for the Digital Enhanced Cordless Telecommunications (DECT) standard incorporating all of the RF subsystems except for the filters, front stage LNA, VCO and GaAs power amplifier. This device combines the functions of more than 8 components (mixer, IF Amp, IF limiting amplifier, quadrature demodulator, RSSI, 1 GHz phase locked-loop, regulators, frequency doubler, etc.). The chip is fabricated in a 0.5 µm BiCMOS process, allowing integration of both high performance analog circuits as well as digital functions on the same piece of silicon.

The total DECT radio solution consists of three integrated circuits (IC) and various discrete components (Fig. 1). The three ICs which comprise the DECT radio are the BiCMOS RF transceiver chip, a GaAs power amplifier and a CMOS baseband controller (the baseband controller IC is not shown in Fig. 1).

Along with the GaAs power amplifier and baseband IC, the highly integrated transceiver chip provides a 3 chip DECT radio exceeding type approval specifications. The resulting transceiver solution enables highly compact radio designs which contribute to smaller, lighter personal communications equipment. The reduction in complexity and component count translates directly into faster time to market and higher reliability for consumer products.

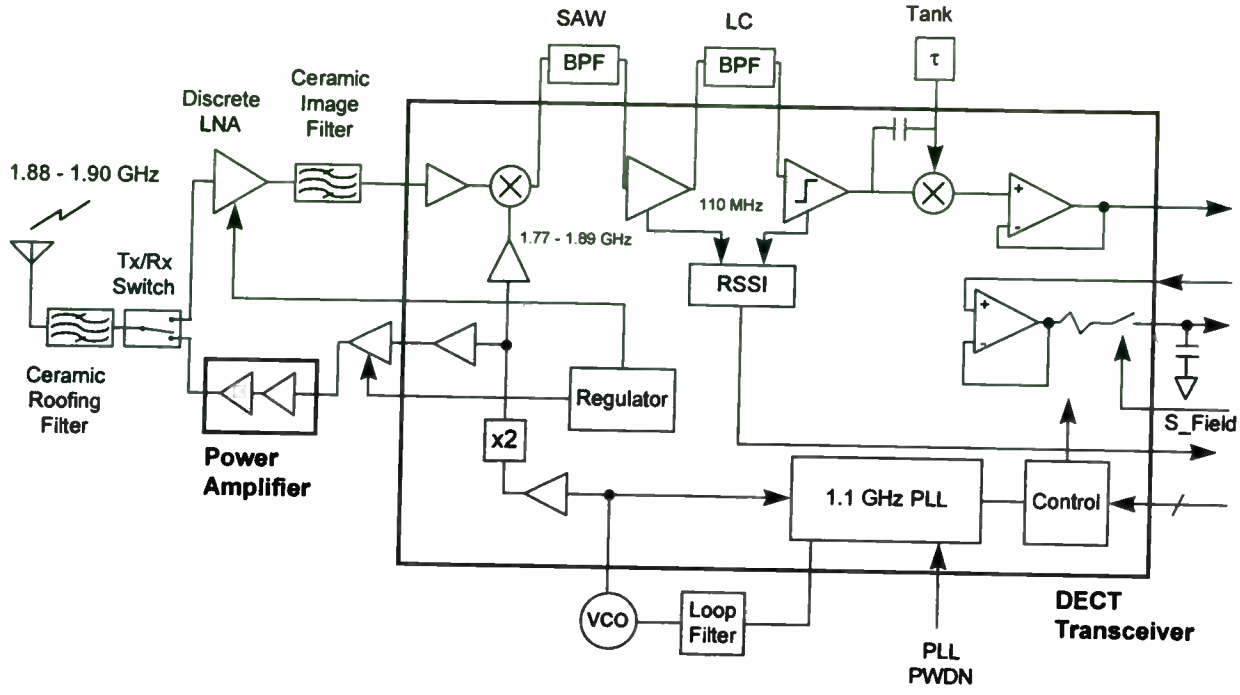

Fig. 1 - DECT transceiver block diagram

II. RF Transceiver Chip

The transceiver chip consolidates receiver, transmitter and phase locked loop (PLL) subsystems. All blocks are internally regulated for 3.0V to 5.5V operation. The chip also includes two regulated voltage outputs and three programmable CMOS outputs. Power control and register information is input via a three wire MICROWIRE™ programming interface.

The PLL /VCO runs at one half of the DECT frequency (880 - 950 MHz) and uses an on board frequency doubler to synthesize the correct DECT frequencies. The use of a frequency doubler alleviates the effects of EMI radiation on the VCO from the power amp. The frequency doubler also decreases the effects of load pulling on the VCO by increasing the isolation between the power amplifier and the VCO.

The receiver subsystem consists of a down converting mixer, an IF amplifier, limiting amplifier and quadrature demodulator. The modulated RF signal is first passed through a roofing filter to attenuate signals outside of 1880 - 1900 MHz, the DECT frequency spectrum. An inexpensive discrete LNA is then used to provide the first gain stage of about 14 dB with a noise figure of about 2 dB. Another ceramic filter is used to attenuate the image of the signal. The RF signal then comes on chip and is down converted to 110.562 MHz and passed through an off chip SAW filter to suppress the adjacent channel signals. Cascaded RF gain before the SAW filter is approximately 28 dB with a cascaded NF less than 6 dB. The signal comes back on chip through the IF amplifier (~25 dB gain) and then off chip through a discrete filter to remove wideband noise (~8-10 dB insertion loss). The signal is passed through a 60 dB gain limiting amplifier and then converted to baseband using a quadrature demodulator. The total gain in the IF section is approximately 80 dB. An off chip LC tank circuit is required to generate the 90° phase shifted signal. The output of the quadrature demodulator goes off chip for low pass filtering, then back on chip for DC recovery using a sample and hold circuit.

The transmitter subsystem consists of a 1.1 GHz phase-locked loop, a frequency doubler and a transmit output buffer. Transmission is accomplished by direct, open loop modulation of the 1 GHz VCO. In the time slot prior to transmission, the PLL is phase locked to one half the DECT transmit frequency and then powered down to open the loop during the desired transmit slot. Very low drift (<3 kHz/ms typical) of the open-loop VCO is accomplished by maintaining low leakage from the charge pump, varactor and loop components. This exceeds the DECT frequency drift specification of 13

kHz/ms. Performance of the open loop modulator has been documented [2]. The modulated signal then comes on chip for frequency doubling accomplished through the use of a full wave rectifier. The doubled frequency is then selectively amplified before going off chip into a tuned amplifier stage for further amplification and filtering. The signal is then at an appropriate input power level (~0 dBm) for the GaAs power amplifier to operate efficiently.

III. Performance of the Radio Transceiver

For DECT radios, the primary receiver specification is the receiver sensitivity. Receiver sensitivity for voice communications is the signal level where the Bit Error Rate (BER) is 10^{-3}. Table 1 summarizes the results for the receiver in the additive white Gaussian noise (AWGN) environment and for the adjacent channel interferer (ACI) and co-channel interferer (CCI) measurements. For the ACI and CCI measurements the desired signal level was always set to -73 dBm and the interfering signal level was adjusted consistent with DECT type approval measurements.

Table 1
Summary of Measured Results for AWGN and ACI/CCI

Parameter for BER= 10^{-3}	Measured	DECT Spec
Desired Signal Power Level	-93 dBm	-86 dBm
Co-channel interferer power level	-80 dBm	-83 dBm
1st Adjacent channel power level	-56 dBm	-58 dBm
2nd Adjacent channel power level	-34 dBm	-38 dBm

Other receiver metrics include receive signal strength indicator (RSSI) and the quadrature demodulator output eye diagram. The RSSI performance was measured by varying the signal level at the input to the antenna and recording the observed voltage level on the RSSI output pin. An averaged result is shown in Fig. 2.

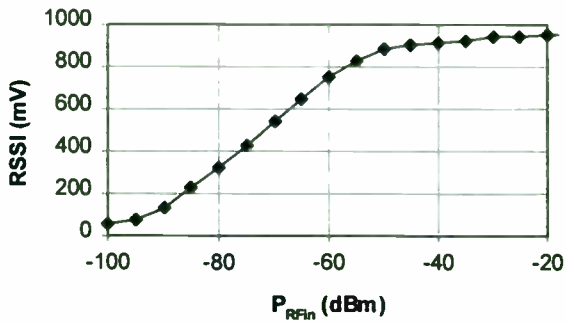

Fig. 2 - RSSI vs RF Input Power at the Antenna

The quadrature demodulator output eye diagram for 3X quadrature demodulator gain mode is shown in Fig. 3. The data pattern used was a pseudorandom bit sequence. The input signal power level was -73 dBm.

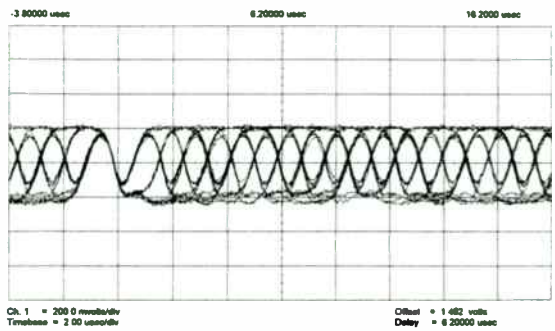

Fig. 3 - Quadrature Demodulator Output Eye Diagram for 3X Gain Mode

Transmitter performance is primarily dependent on the frequency drift during open loop and the harmonic content of the output signal. These parameters dictate the transmit frequency accuracy and spurious noise performance. Fig. 4 shows the open loop frequency drift to be about 2.5 kHz/ms which far exceeds the DECT requirement of 13 kHz/ms.

Fig. 5 shows the output spectrum of the frequency doubler during transmit for an input signal of -10 dBm at 890 MHz. The output signal level at the desired doubled frequency is about -4 dBm while the undesired fundamental and 3rd harmonic are suppressed by 32 dB and 28 dB respectively.

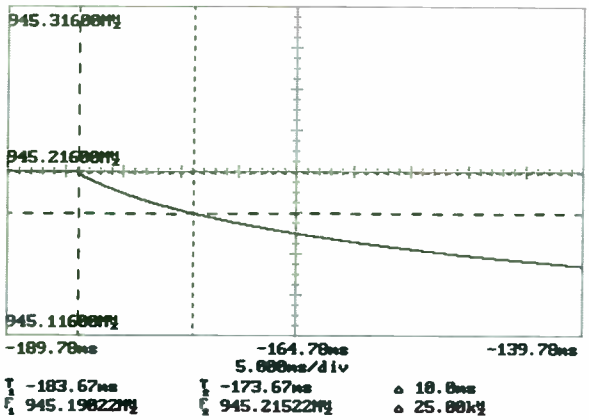

Fig. 4 - Open Loop Frequency Drift

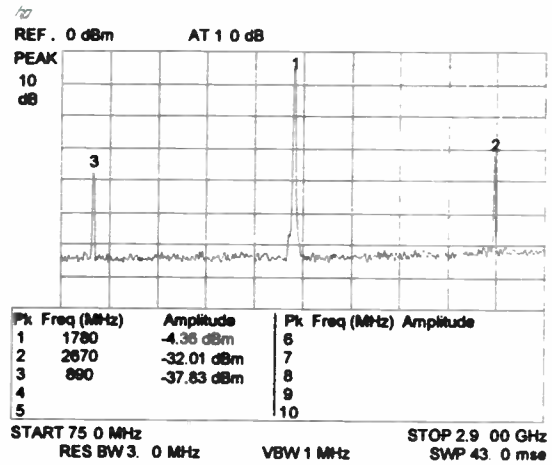

Fig. 5 - Frequncy Doubler Output Spectrum

IV. Conclusion

The architecture and performance of a highly integrated radio solution for the DECT market has been presented. An RF transceiver IC forming the backbone of a three chip DECT radio was described in detail. Measured data has been presented showing this chip to be an excellent solution for a DECT radio with sensitivity of -93 dBm for BER of 10^{-3}. Because of the device's high level of integration, the DECT radio will have fewer components thus enabling a solution that is smaller and costs less than previous solutions.

Acknowledgments

The authors would like to thank Bill Burdette, Chris Schell, David Bien, and Tom Anderson, whose contributions were instrumental in developing the single chip transceiver solution.

References

[1] B. Madsen and D. Fague, 1993. "Radios for the future: designing for DECT", *RF Design*, April, 1993.

[2] D.E. Fague, A. Dao, and C. Karmel, "Techniques for Open Loop Modulation of a Wideband VCO for DECT", *Proceedings of the RF Expo 1994*, San Jose, CA (USA), March, 1994.

[3] ETSI, Final Draft - prETS 300 175-2, Specification for DECT, Part 2: Physical Layer, Cedex, France, May, 1992.

Investigation on VLSIs' Susceptibility to Conducted RF Interference

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Abstract

The usual susceptibility measurements performed to check VLSI's hardness to conducted interferences do not seem to be useful looking for the VLSI's subcircuit culprit of the output ports upset. Susceptibility measurements carried out directly on the chip are mandatory.
Aimed to these questions we developed an innovative susceptibility test bench. The method, based on the single PIN injection, allows to carry out "on chip" susceptibility measurements, in order to investigate on the VLSI's devices behaviour. Many measurements have been performed on a VLSI CMOS (.7 μm) input pads for interference carrier frequency in the range 20 MHz - 1 GHz and available power level up to 15dBm.

Introduction

The recent explosion in the portable electronics market combined with increasingly hostile electromagnetic (EM) enviroment have intensified the need to include electromagnetic susceptibility design and test methods in applicable low-power IC's. In the presence of electromagnetic incident field (produced for examples by the cellular phone transmitting antenna), cables connected to the electronic systems and PCBs' traces behave as receiving antennas capturing disturbances. The induced RF currents reach the input ports of active devices and often produce system malfunctioning. In this paper we refer to conducted interference because we firmly believe that the EM interference and the traces routed on the chip are lightly coupled and the susceptibility effects negligible. Interferences conducted into IC's pins could induce failures of two different kind.

- Static Failures: for a fixed input pattern and RF interference signal injected into a gate's input (single PIN injection), static failures occur when the output pattern is not related with the input one. Some of the output voltages are not into the high state or low state noise margin. For high level interference signal (RF voltage pick higher than commutation threshold) the outputs follow the disturbance.
- Dinamic Failures: conducted RF interference superimposed on the input signal (i.e digital signal) of a digital gate , gives an output signal extra propagation delay [3].

For CMOS ICs the dinamic failures occur before static ones and could be the cause of misfunctioning in VLSI general purpose machines: the logic gates settling time, hold time but also the sampling time masks could not be respected. In this way, the errors due to conducted interference, observed at the IC's output ports come from the fault (or combined faults) of one or more IC's subcircuits. In order to carry out susceptibility measurements directly on the chip a new test bench has been developed. The effects of the interference signal superimposed on the digital one are observed on the chip by an Electron Beam Testing probe system.

Measurements Test Bench

The DUT has been mounted into the Electron Beam Testing probe system: the test fixture (where the DUT has mounted on) is the upper surface of EBT's vacuum chamber (see fig.1). A DC current holds the tungsten filament temperature at 2400 C. The electron delivered from the hot filament by thermionic effect are accelerated by 1kV voltage and focalized using the optical column shown in fig.2. Energy of secondary electrons delivered from the die surface depends on the local surface potential. The electromagnetic fields producted close to magnetic lens collect the secondary electrons. Scintillator (not indicated in fig.2) converts the secondary electrons energy in photons and the photomoltiplicator (PMT) acts as amplifier. On the basis of PMT output the DUT layout image is shown on the workstation monitor linked to the EBT [1]. For instance, a supply trace (+5 V) appears darker then a ground one, while the image of a trace excited by square wave appears on the screen like a black and white dotted bend (see fig.3 test point (A) and (Z)). The EBT gives voltage contrast image and allows to show, by software probe station scope tool, the time domain behaviour of the surface potential in each point of the die.
Performing susceptibility tests on the input port of

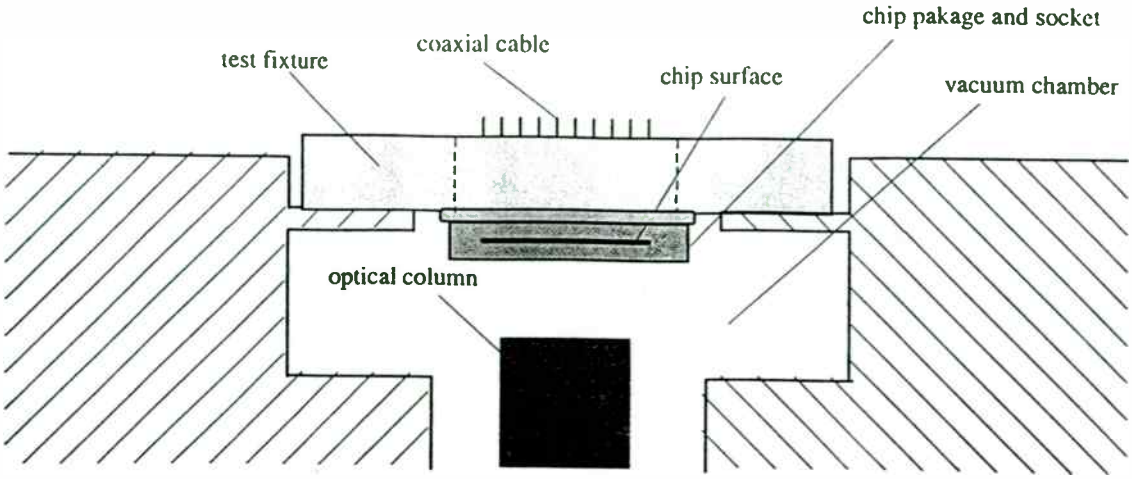

Fig. 1: EBT vacuum chamber cross section.

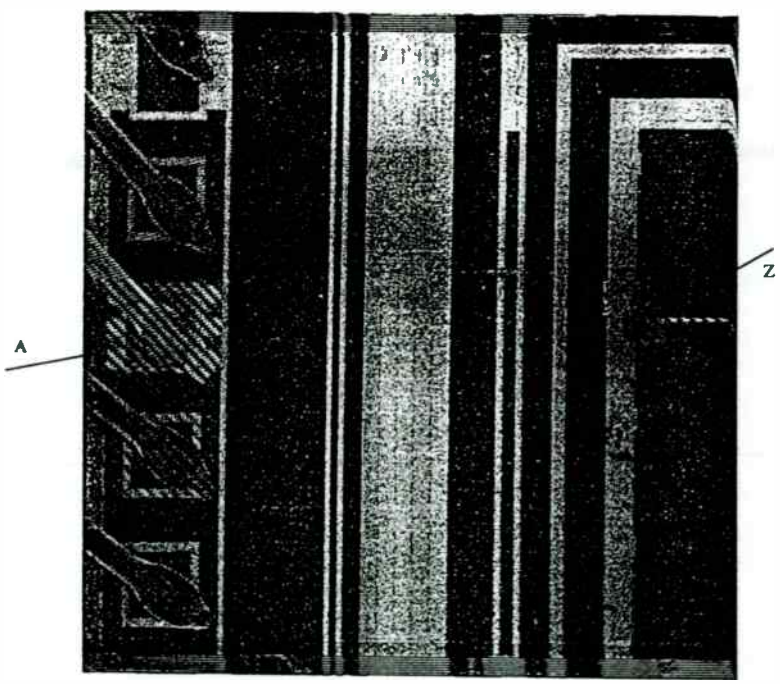

Fig. 3: Image of the die obtained by The Electron Beam Testing probe system.

VLSI (CMOS, .7μm), the input pad extra propagation delay evaluation requires digital and interference signals syncronization. In this way the input square wave is locked with respect to the RF signal. More-

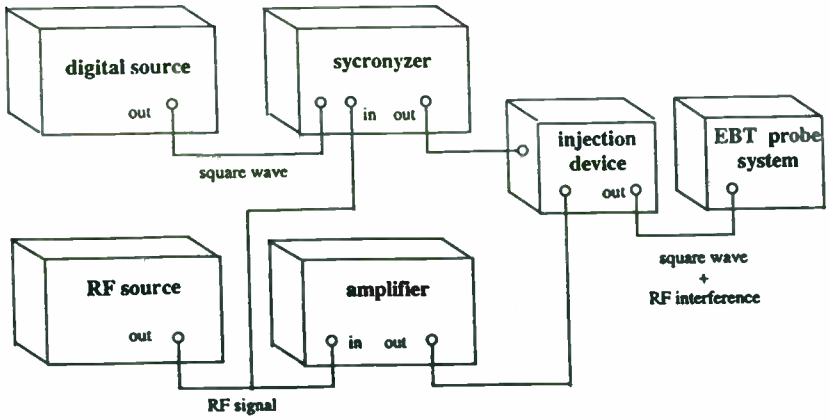

Fig. 4: Susceptibility test bench.

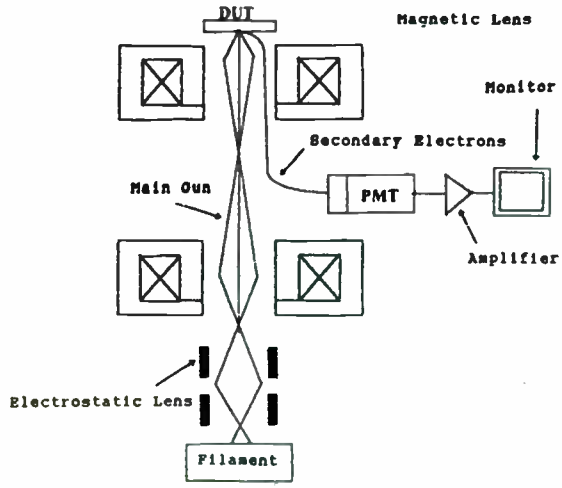

Fig. 2: EBT optical Column.

over, the syncronyzer allows the variation of the time delay between the input port signals (interference and square wave)[3]. Syncronyzer allow the control of the time delay between the input signals (named Ph) allowing the input pad extra propagation delay ($\Delta\tau$) evaluation [3].

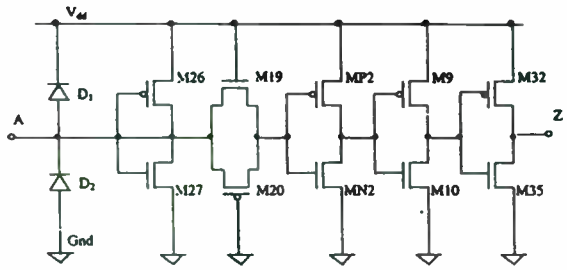

Fig. 7: DUT: CMOS input pad (0.7μm). (A) and (Z) are the test points.

CMOS Input Port Susceptibility

By the test bench shown in fig.4, susceptibility measurements on VLSI's CMOS (0.7μm) input pad (fig.7) have been performed (point (A) and (Z)). The input port extra propagation delay $\Delta\tau$ vs. the input time delay Ph has been measured for interference carrier frequency in the range 20 MHz - 1 GHz and available power level up to 15dBm (Figg.8, 9, 10). The results obtained at low interference carrier frequency are close to the experimental ones shown in [3] [4].

When the period of RF signal is lower then digital wave edge duration, the pad extra propagation delay measured on the output port of the input pad is negligible (compared with edge duration), and the output signal shows the behaviour depicted in figg.5,6.

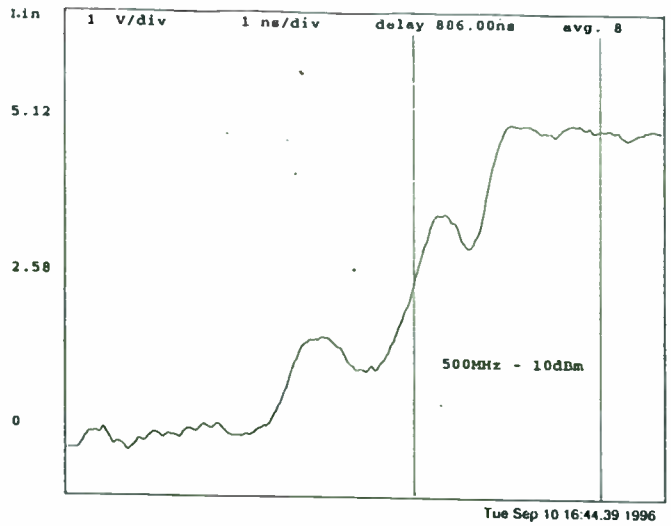

Fig. 5: Voltage measurement by EBT probe system on the output (point (Z)) in the presence of (500MHz, 10dBm) interference signal superimposed on the input square wave.

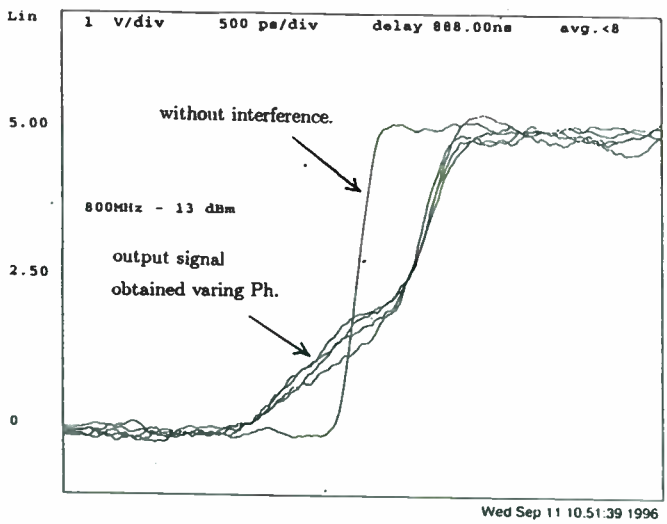

Fig. 6: Voltage measure by EBT probe system on the output (point (Z)) in the presence of (800MHz, 13dBm) interference signal superimposed on the input square wave. By this figure is possible to compare the output signal behaviour with and without interference output signal obtained varing Ph.

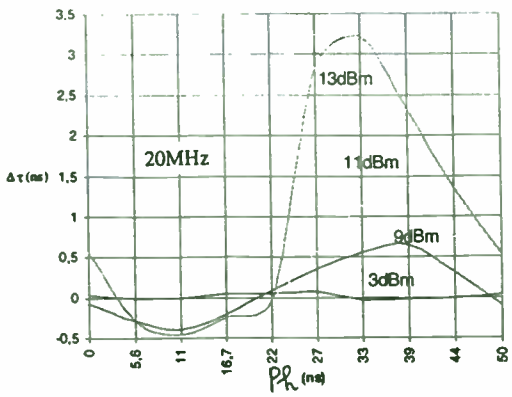

Fig. 8: Extra propagation delay $\Delta\tau$ vs. input time delay Ph.

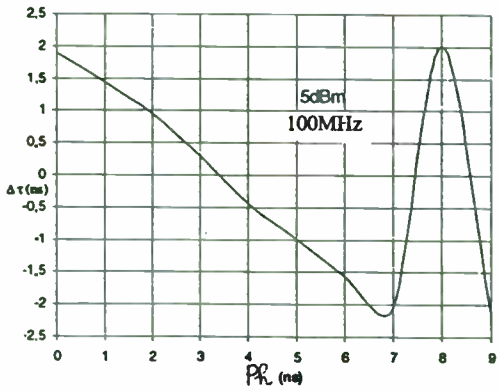

Fig. 9: Extra propagation delay $\Delta\tau$ vs. input time delay Ph.

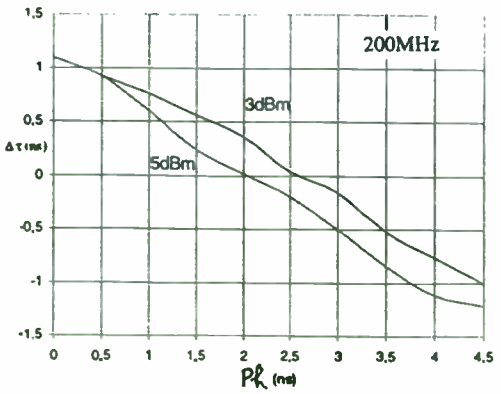

Fig. 10: Extra propagation delay $\Delta\tau$ vs. input time delay Ph.

Conclusions

The experimental test bench developed to perform susceptibility measurements directly on the chip can be the right tool in on chip susceptibility investigation.

Measurements performed by the test bench previously described are shown that the RF interference applied on the input ports of a digital IC is confined on the border of the IC: ESD protections and input pads are involved by interfernces. In the case of interference period lower than input square wave rise (fall) time, an extra propagation delay has been measured. Increasing in interference frequency the extra propagation delay decreses and the input pad shows abnormal behaviour as indicated in fig.6.

The method described in this paper can be useful in the evaluation of analog IC susceptibility.

References

[1] Schlumberger co., EBT IDS-3000 User Manual, Schlumberger, 1990.

[2] Electromagnetic compatibility measurement procedures for ICs - integrated circuit radiated emissions measurement procedures 150 kHz to 1 GHz, TEM cell", SAE surface vehicle recommanded practice J1752/3, Society of Automotive Engineers, Warrendale, PA, 1995.

[3] J.J Laurin, *EMI Induced Failure in Digital Systems*, Ph.D. dissertation, University of Toronto, Toronto, ON, Canada 1991.

[4] J.J. Laurin, S.G. Zaky, K.G. Balmain *Prediction of Delay Induced by In-Band RFI in CMOS Inverters*, IEEE Trans. on Electromagnetic Compatibility May 1995, vol. EMC 37, No.2, pp 167-174.

Use of Image Rejection Mixing in Low Cost RF Design

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Due to availability of low cost filtering and inexpensive CMOS signal processing, 10.7 Mhz. is an ideal interface Intermediate Frequency for digital wireless systems. Problems arise however when using such a design in systems used in bands whose width exceeds 10 Mhz. and trying to filter image and Local Oscillator frequencies. While dual conversion radio designs solve the problem, they are expensive and consume too much power. Double balanced single sideband mixer chips solve the problem elegantly and inexpensively with good design reproduction.

I. Background

From toys to interactive television, digital radio is penetrating every niche in consumer electronics [1]. Consumer markets function similar to computer markets, where "magic" price points remain steady while consumers expect greater quality and functionality from year to year for a given price of a product [2]. This phenomenon forces

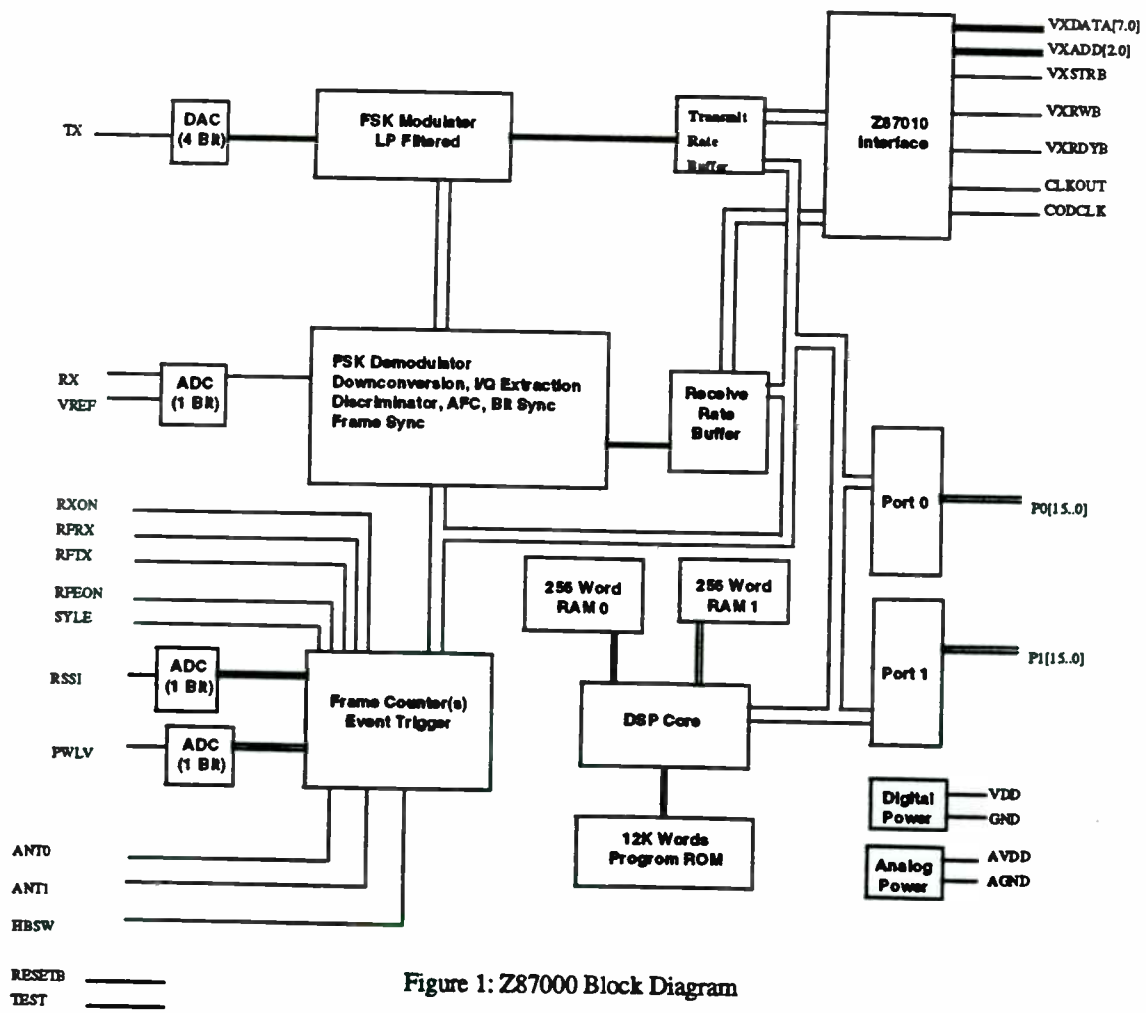


Figure 1: Z87000 Block Diagram

digital radio designers and manufacturers to act very aggressively to minimize system costs and this primary design objective begins from initial systems design. Current digital radio systems typically divide digital processing and RF between devices built with differing technology, with analog/digital conversion at the limen. This architecture is due to the cost/performance tradeoffs in material technology, AD/DA cost and filtering. This paper's focus is on silicon, since more expensive technologies such as gallium arsenide are out of reach of consumer systems.

II. Design Trade-Offs

Comparative technology cost drives system designers to seek ways to maximize the digital processing in the system. Usually implemented in CMOS, the technology is the lowest cost available to the engineer per unit area. CMOS technology is available to implement more and more of a system function as cost drops with the square of any reduction in feature size. Feature size reductions also raise the gain-bandwidth product of any analog circuits made with the material, opening the door to inexpensive mixed mode devices where system AD cost is absorbed into

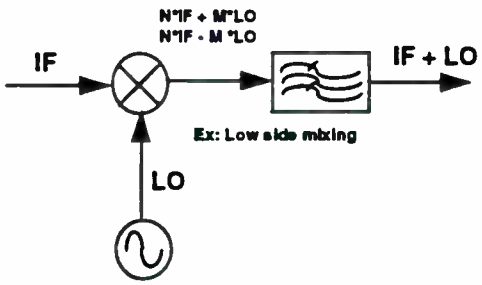


Figure 2: RF Mixing

the baseband controller.

A typical example of a device taking full advantage of the capabilities of CMOS to optimize cost in a digital radio system is the Zilog Z87000 [3]. This device integrates an instruction set processor optimized for DSP with hardwired digital radio and the system's AD and DA converters. All microcontrol, modulation and demodulation are performed on the Z87000 and the Z87000 communicates at 10.7 MHz (Fig 1). This configuration is ideal for low cost digital radio due to scale of integration, cost of implementing technology and integration of mixed mode processing. The Z87000 implements its digital RF using a frequency plan which greatly simplifies demodulation. The selection of 10.7 MHz. as an interface frequency also renders filter cost almost negligible.

III. RF Challenges

A band of operation for which the Z87000 is currently targeted is the 900 MHz. Industrial, Scientific and Measurement (ISM) band. This band extends from 902 MHz. to 928 MHz. and permits unlicensed transmission with up to 1 Watt radiated power if the transmitter utilizes spread spectrum transmission techniques [4]. The Z87000 complies by frequency hopping at a rate of 250 hops per second. Even taking advantage of the Z87000's high frequency data interfaces at 10.7 MHz., additional frequency conversion is necessary in a Z87000 system running in the 900 MHz. ISM band. This frequency conversion is accomplished (Fig. 2) by use of an RF oscillator (LO) mixed with the 10.7 MHz. port of the Z87000 used as an Intermediate Frequency (IF).

As shown in Fig. 2, the output of the mixer includes undesired harmonic

products in addition to the desired frequency. Frequencies generated by the mixer are

$$N*LO +/- M*IF \quad (1)$$

where as the coefficients rise power drops as in a harmonic series. The desired frequency is selected after the mixing process by a filter commonly referred to as an image filter. The image referred to is the sign inverted sum of the fundamental LO and IF appearing in Fig. 3 symmetric to the desired frequency on the opposite side of the LO. Effective filtering of the image depends on making the image far from the desired frequency with respect to the LO and the bandwidth of the image filter.

This last consideration has until recently dictated use of dual conversion radio transceivers for ISM band systems using the inexpensive 10.7 MHz. IF. Adding a higher frequency first IF as shown in Fig. 3 moves the image further from the desired mixer output, but at the expense of additional component cost including a mixing stage, oscillator and filters to prepare the new, higher LO. The image is thus moved further out into the final filter skirts where it can be effectively attenuated, but at the cost of money, size and power consumption.

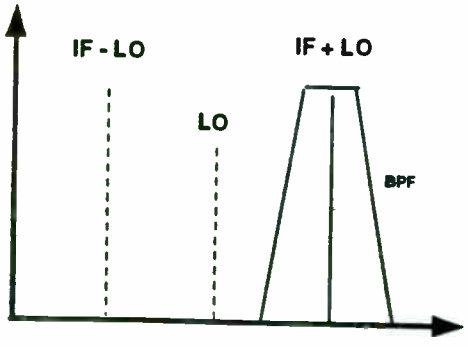
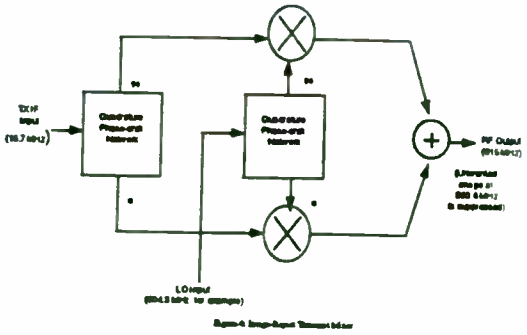


Figure 3:
Low Side Mixerand Bandpass Filter



IV. Single Conversion Solution

For ease of manufacturing, it is desirable to integrate this RF function. Utilization of a digital signal processor such as the Zilog Z87000 can minimize the functionality necessary in the radio transceiver and render it amenable to single-chip integration. Image-reject

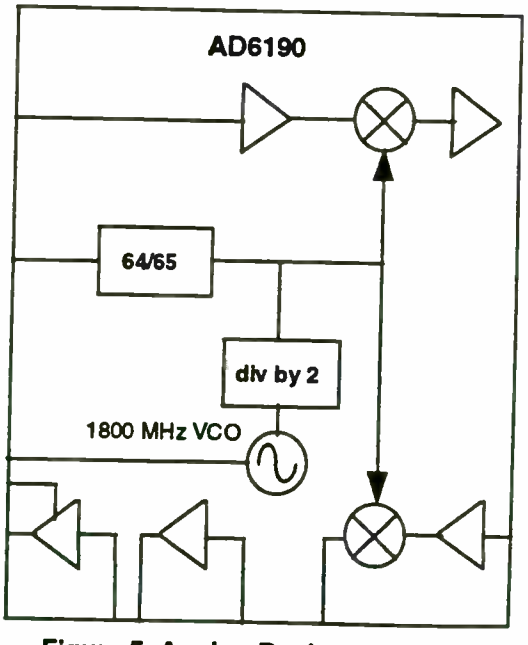


Figure 5: Analog Devices AD6190

mixing can be achieved by using a pair of mixers in conjunction with quadrature phase-shift networks in the LO and IF signal paths, as shown in Figure 4. With careful design, is it possible to implement fully-integrated process-tolerant phase-shift networks which provide excellent image-rejection characteristics over the band of interest in both the transmit and

receive mixers. The mixers themselves can be standard Gilbert-cell types, readily implemented in silicon processes for use at 900 MHz.

Image-reject mixing, is sometimes referred to as "single-sideband mixing", since the technique is often used for single-sideband generation. Rigorous mathematical treatment of the technique can be found in various texts on communications systems [5]. Bipolar ICs with this type of RF mixing capability are seen increasingly today. One such device is the Analog Devices 6190. The AD6190 is show in Fig. 5.

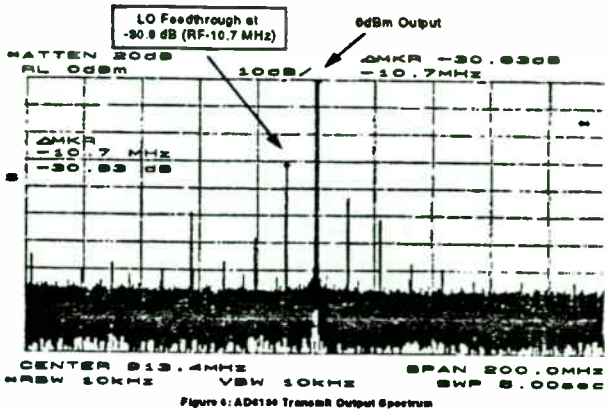


Figure 6: AD6190 Transmit Output Spectrum

optimal non-linear digital radio design by providing a hard limited output to the baseband processor. An example radio transceiver utilizing the AD6190 is shown in Fig. 7.

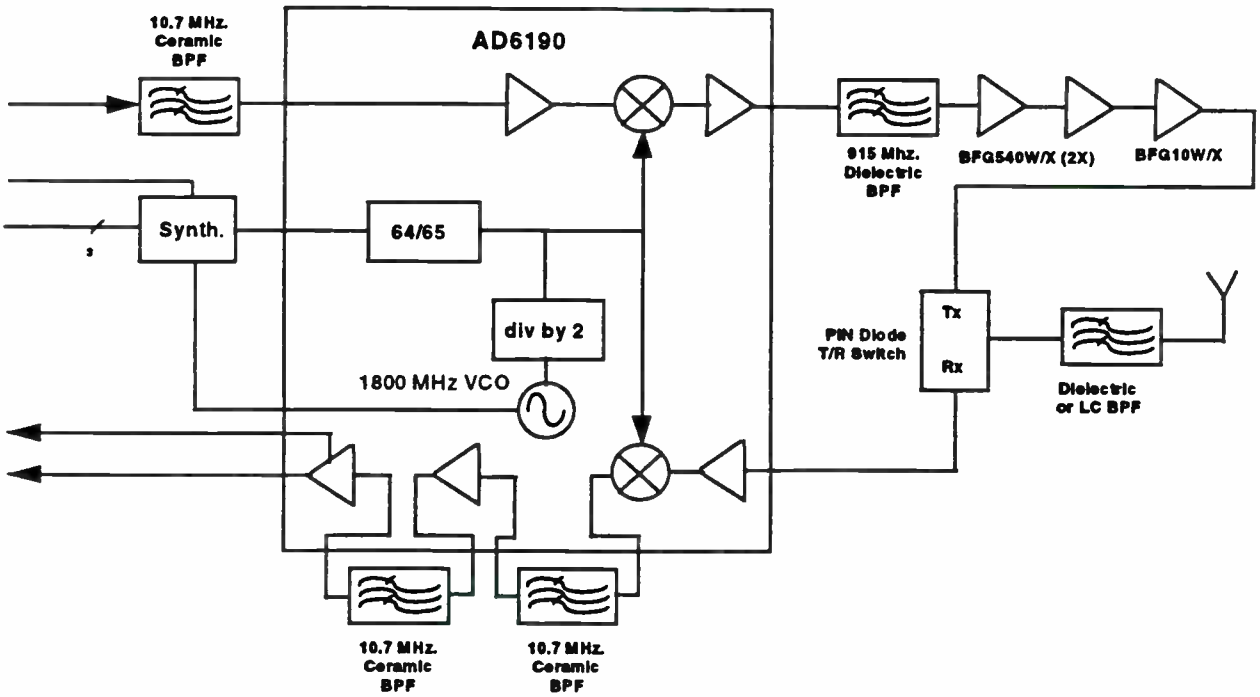


Figure 7: Single Conversion Radio

This device is specified to deliver more than 35 dB image and LO rejection operating in the 900 MHz. ISM band with an IF input of 10.7 MHz. Actual performance can greatly exceed the specification (Fig. 6). The AD6190 minimizes design risk with its double frequency integrally voltage regulated VCO for LO generation and enables

V. System Integration

Operated together, the Zilog Z87000 and the Analog Devices AD6190 form an optimal digital radio system. All possible signal processing is performed on the CMOS mixed mode device. That signal processing at frequencies beyond the capabilities of production CMOS are

implemented in a conventional silicon bipolar process. The result is a digital radio system that when built by combining these two devices, is inexpensive, performs well, and is small, low-cost, and amenable to consistent high-volume manufacture. Power output, left in discretes is the product manufacturer's choice.

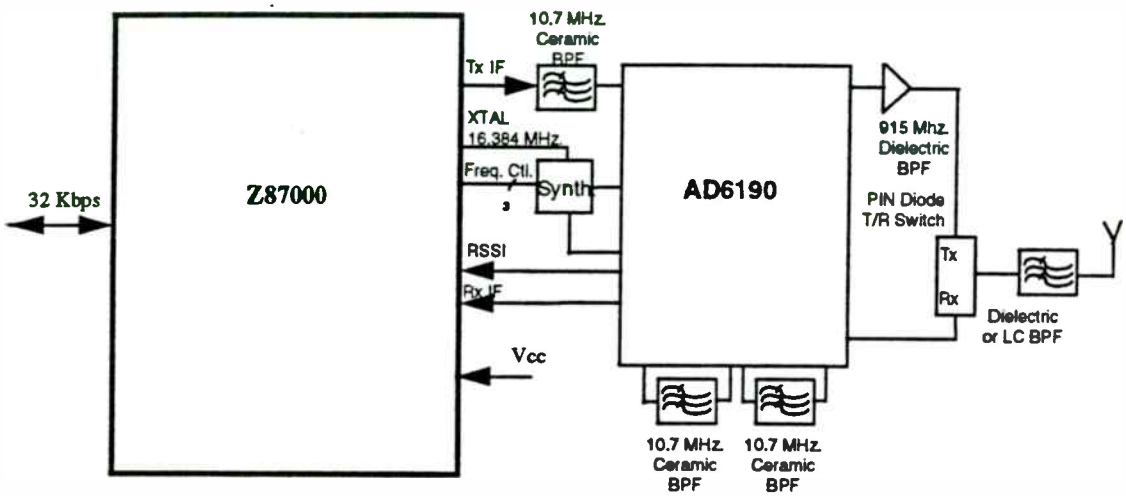


Figure 8: Digital Radio Design

An example of this digital radio design appears in Fig. 8 and features a 250 mWatt EIRP transmitter, adaptive frequency hopping, adaptive output power, telephone quality voice transmission and high performance. This system is capable of a range exceeding 2 kilometers with a bit error rate less than 1E10-4 and sustaining an MOS score of 3.9 [6]. Example applications for this digital radio include digital cordless telephones, spread spectrum cordless telephones, networked radio communicators, interactive TV back channel, wireless PBX, wireless local loop, wireless modem and industrial controls. The use of the single conversion transceiver chip enables the most cost effective full duplex radio design possible.

References:

[1] Consumer Electronics Manufacturers Association, "US Consumer Electronics Sales and Forecasts 1991-1996"

[2] *IBID.* [1]

[3] Zilog Incorporated, *Wireless Databook*, Zilog Incorporated, 210 East Hacienda Avenue, Campbell, California 95008.

[4] Code of Federal Regulations, Title 47, Part 15, Sections 247, "Operation within the bands 902-928 MHz, 2400-2483.5 MHz, and 5725-5850 MHz"; and 249, "Operation within the bands 902-928 MHz, 2400-2483.5 MHz, 5725-5875 MHz, and 24.0-24.25 GHz".

[5] Lathi, B.P., "Communications Systems", J.W. Wiley, 1968, Chapter 3.4 - Single Sideband Transmission, p. 180-184

[6] Zilog internal communication.

SILICON BIPOLAR RFICs FOR 900MHz CORDLESS PHONE APPLICATIONS

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Abstract- **Motorola's MOSAIC™ V RF silicon bipolar process is well suited for a variety of low power, cost sensitive wireless applications including cordless telephones. The use of a high frequency silicon process technology and novel circuit techniques has resulted in the production of high performance RF building blocks. Success with higher levels of integration is facilitated by detailed characterization of RF standard cells. MOSAIC V standard cells fill the need for complete RF system configuration at frequencies up to 2.4GHz with a minimum number of external components. Higher levels of integration allow for decreased cost, lower power consumption and improved performance. Example system configurations for 900MHz analog and digital cordless telephone applications are presented.**

I. INTRODUCTION

Today's portable communications products require high performance, low power, off-the-shelf ICs to meet aggressive new product introduction schedules. The competitive consumer market, where most of these new products are targeted, demands incremental improvements in performance coupled with cost reductions. Recent offerings from Motorola provide attractive solutions to these market issues.

Low noise amplifiers, up and down frequency converters, VCOs, synthesizers, exciters and IF processing blocks are all realized with Motorola's MOSAIC V RF silicon bipolar process. These functions comprise a set of well characterized RF integrated circuits which achieve the design goals for noise figure, linearity and power consumption. Design cycle times for increased levels of integration are reduced through the use of these cell libraries.

II. SILICON PROCESSING

High performance receiver front end circuits were fabricated using Motorola's MOSAIC V process (Fig. 1). Process characteristics include a 0.3µm effective emitter width, 14GHz f_τ, 0.1Ω-cm p+ substrate, poly silicon emitter and trench isolation.

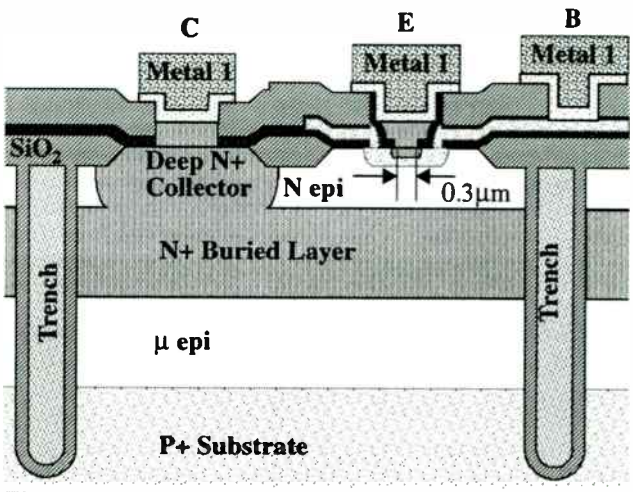

Fig. 1. MOSAIC V NPN transistor cross section

A. *Signal Isolation*

Signal isolation is a critical parameter in RF integrated circuit design. Isolation on the packaged die is greatly aided by the use of a low resistance substrate contact. Isolation measurements between two MOSAIC V epi contacts spaced 12µm apart and separated by a top side substrate contact (Fig. 2) were made. The results of this measurement are shown in Fig. 3. The data shows that this process is capable of achieving 94dB of isolation at 1GHz. The actual isolation achieved in practice will be limited by the package in which the die is placed.

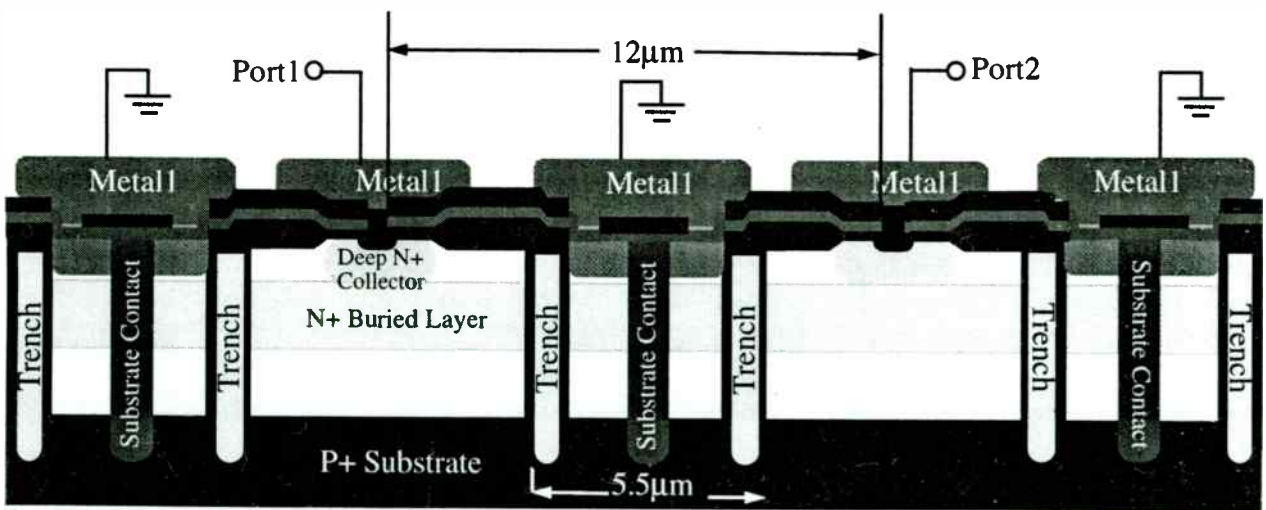

Fig. 2. Isolation Test Structure

MOSAIC is a trademark of Motorola, Inc.

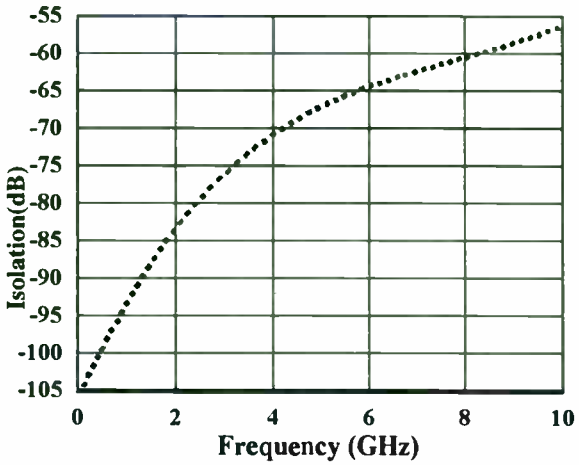

Fig. 3. Epi contact isolation versus frequency

III. PACKAGING

Motorola continues its commitment to wireless integrated circuits by introducing a new plastic 20-pin thin quad flat package (TQFP) customized for RF applications. This plastic package features a 4mm x 4mm body and 0.65mm pin pitch. The leadframe (Fig. 4) is customized for RF signal isolation which is further improved by the connection of two leads directly to the leadframe flag. The quad arrangement eases external component configuration allowing easy access to ground pins.

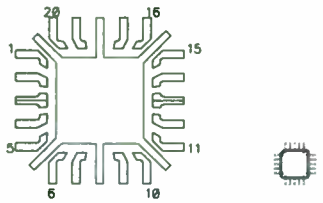

Fig. 4. TQFP20 Leadframe (5X magnification) and package (1X magnification)

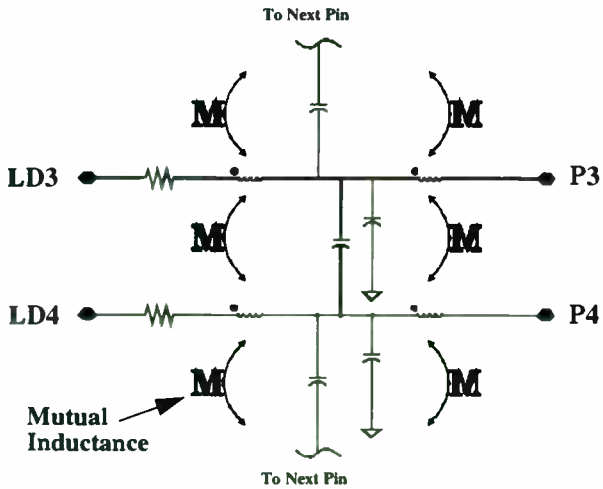

Fig. 5. Partial lumped element model of TQFP20

A. Characterization and Modeling

The RF suitability of a package can not be appropriately determined in the design and simulation of a circuit without the aid of an accurate package model. Electromagnetic simulation of a package in addition to RF package characterization based on measured S-parameters yields a reliable model (Fig. 5). Additionally, the effects of substrate coupling are minimized with the top side substrate contact and the low resistivity substrate in the MOSAIC V process.

IV. CELL LIBRARY

An established library of analog and RF circuits exists in Motorola's MOSAIC V cell library. Each cell features independent current regulation with temperature and power supply compensation. The liberal use of substrate contact shielding facilitated by the low resistance substrate contact and low resistivity substrate greatly aid signal isolation.

Some of the characterized cells which are important pieces for integration include the following:

A. High Linearity Mixer

This cell[1] is a low power consumption high compression linear mixer with single-ended 50Ω input and differential output. Designed for up or down conversion, this cell can be used from DC-2.4GHz and features double-balanced operation with linearity adjustment. The IP^3_i, gain and supply current for the mixer are plotted against adjustment current in Fig. 6.

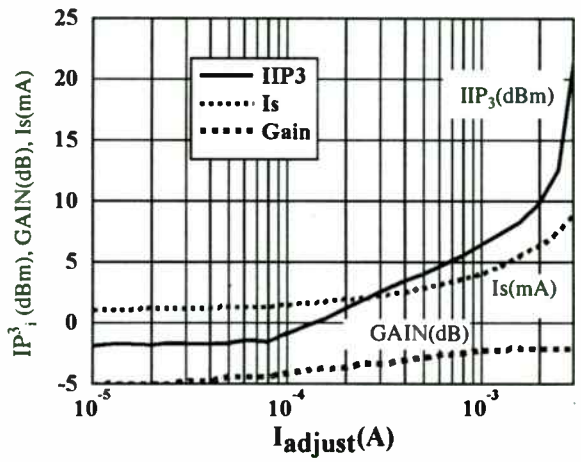

Fig. 6. IP^3_i versus linearity adjustment current

B. Prescaler

This dual modulus prescaler is programmable for ÷32/33, ÷64/65 or ÷128/129 and optimized for 1,2GHz operation

C. Quadrature Generator

In order to implement an image rejection mixer, a local oscillator which provides both 0° and 90° signals is required. This quadrature generator accepts a local oscillator signal and generates a 90° phase shifted version equal in amplitude to the original signal. This architecture is self calibrating and insensitive to supply, process and temperature variations. This cell is currently designed to operate from 400MHz through 700MHz with low amplitude and phase imbalance. This cell can also be used in a quadrature modulator. The measured amplitude and phase error of the quadrature generator are plotted versus input frequency in Fig. 7.

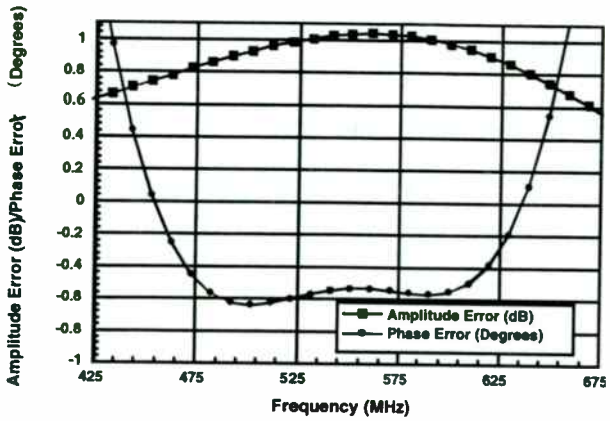

Fig. 7. Measured Amplitude and Phase Error versus Frequency

D. *Low Noise Amplifier*

This cascode amplifier features four digitally programmable bias states. An off state, a low power mode, a low noise figure mode and a high linearity mode are available. This amplifier can be used as an LNA in the receive path or an exciter in the transmit path. Consuming only 4mA of current and requiring only three external matching elements, the LNA exhibits 16dB of gain and 1.4dB of noise figure. The measured and modeled S-parameters for this configuration are plotted in Fig. 8 and Fig. 9.

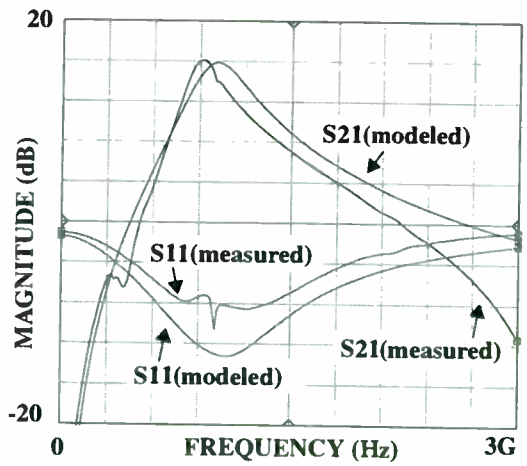

Fig. 8. Measured/Modeled S21 and S11 vs. Frequency

E. *Coilless Demodulator*

This is a unique frequency demodulator design which eliminates the conventional tunable quadrature coil. It also is self tuning and allows for the programming of output amplitude, center frequency and bandwidth. Fig. 10 shows the measured signal, noise and distortion power (relative to maximum output) versus input power for the IF processing block. The IF processing block includes an IF amplifier, limiter and coilless demodulator

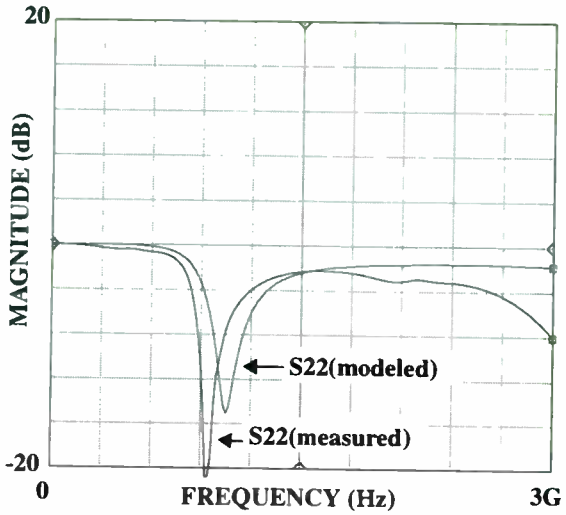

Fig. 9. Measured/Modeled S22 vs. Frequency

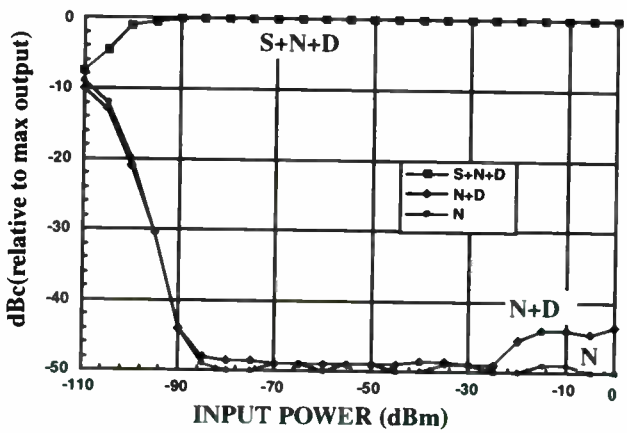

Fig. 10. Measured Signal, Noise and Distortion

V. BUILDING BLOCKS

Motorola's new family of MOSAIC V RF building blocks provide quick turn solutions for RF system design.

A. *MC13143*

Fig. 11 depicts the block diagram and pin out for a class AB linear mixer. The class AB nature of the circuit allows for a low quiescent current while a high power input will cause an increase of the bias. The concept of a class AB mixer has been implemented in the past as a single-balanced architecture but not as a double-balanced architecture. The linearity of single-balanced architectures typically requires increased power consumption. The double balanced architecture provides an improvement in LO to IF and RF to IF isolation when implemented in a down conversion mixer. This circuit has wide bandwidth at all three ports and can thus be operated as either an upconversion or a downconversion mixer.

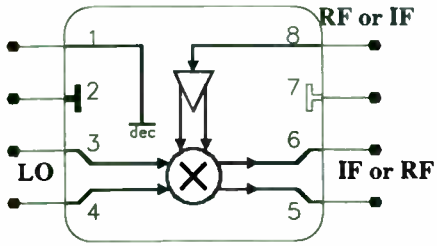

Fig. 11. Block diagram of class AB up/down mixer

The double-balanced class AB mixer has a +3dBm input 1dB compression point, 50Ω single-ended input, and an input third order intermodulation intercept (IP^3_i) which can be externally programed as high as +21dBm. Nominal single sideband mixer noise figure (NF_{SSB}) of less than 12dB and conversion gain of -3dB are achieved at a supply voltage of 2V while consuming under 1mA of supply current. The linearity adjustment feature of this circuit is an important facet because the linearity can be programmed. Certain situations favor reduced power consumption over linearity whereas others sacrifice power drain for linearity improvements. This circuit can accommodate each of these cases. For detailed performance curves see [2].

B. MC13144

The MC13144 (Fig. 12) is a cascoded LNA usable through 2GHz, operable at power supplies as low as 1.8Vdc, featuring a 2-bit digitally programmable bias. Three optimum states (minimum NF, minimum current and maximum IP^3_i) and an off state are selectable. Targeted applications include CDMA where multiple modes for LNA gain and linearity are required.

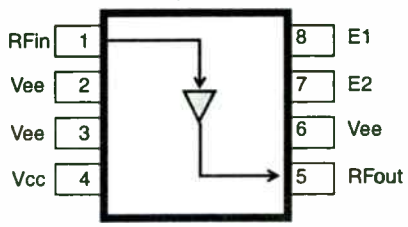

Fig. 12. MC13144 SOIC8 package

C. MC13141

The MC13141 is intended to be used as a first amplifier and down converter for RF applications. It features wide band operation, low noise, high gain, and high linearity. The circuit consists of a low noise amplifier (LNA), a local oscillator amplifier (LOamp), a mixer, an IF amplifier (IFamp) and a DC control section with enable function. This circuit is available in the SOIC8 (Fig. 13), SOIC14 and TQFP20 packages.

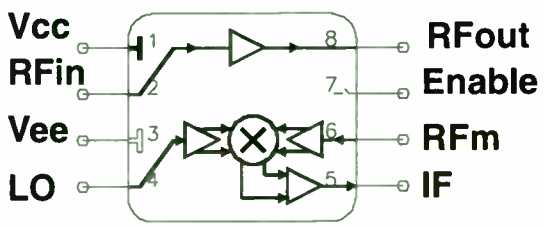

Fig. 13. MC13141 SOIC8 package

D. MC13142

The MC13142 adds a voltage controlled oscillator and oscillator buffer to the MC13141 circuit. The mixer and oscillator can be enabled independently. This circuit is available in the SOIC16 and TQFP20 (Fig. 14) packages.

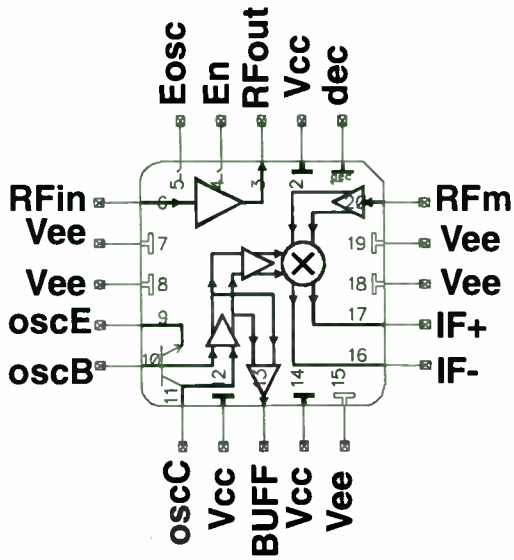

Fig. 14. MC13142 TQFP20 package

E. Performance Overview

The measured performance data for the RF building block circuits is summarized in TABLE 1. Linearity adjustment of the mixer is available in each circuit except the SOIC8 version of the MC13141. The availability of the linearity adjustment allows a user to program the circuit for the desired linearity with a minimal change in the gain. Very high linearity (IP^3_i of +21dBm) is achieved with the MC13143 at an efficient power dissipation (8.8mA at 3V). These results prove the versatility and high performance nature of the new class AB mixer.

TABLE 1. Measured Performance Data

	Gp(dB)	NF(dB)	IP^3_i
MC13141			
LNA	17	1.8	-5
MIXER	7	16	-5➡+15
MC13142			
LNA	17	1.8	-5
MIXER	-3	11.5	-3➡+21
MC13143			
MIXER	-3	11.8	-3 ➡+21
MC13144			
LNA	➡16➡	1.4	-5➡

VI. INTEGRATION

The following higher integration products are either in design or being evaluated:

A. *MC13160*

The MC13160 (Fig. 15) is an integrated UHF low power receiver which includes a mixer, oscillator, buffered oscillator output, IF amplifier, limiter, RSSI output, and coilless demodulator.

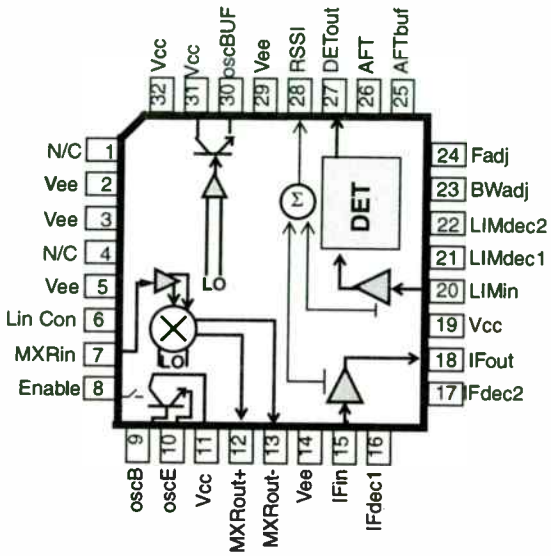

Fig. 15. MC13160 TQFP32 package

B. *MC13161*

The MC13161 (Fig. 16) adds an LNA to the MC13160.

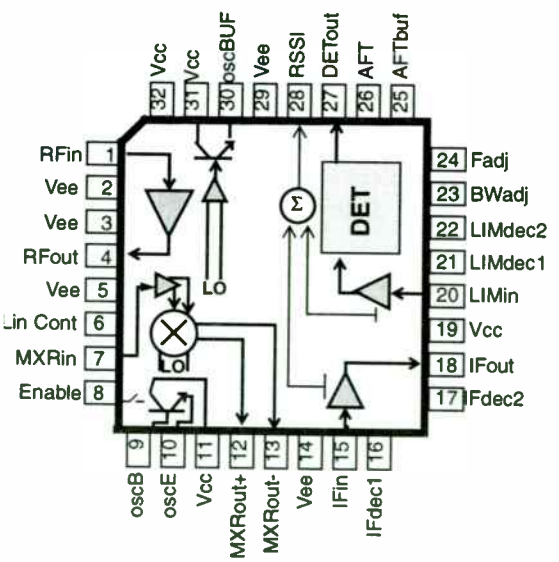

Fig. 16. MC13161 TQFP32 package

C. *MC13145*

The MC13145 (Fig. 17) is a dual conversion integrated RF receiver targeted at 900MHz, 1.8GHz and 2.4GHz cordless telephone applications. It features a low noise amplifier, two mixers with linearity control, voltage controlled oscillator, second LO amplifier, dual modulus Prescaler, split IF Amplifier and limiter, RSSI output, coilless demodulator and power down control.

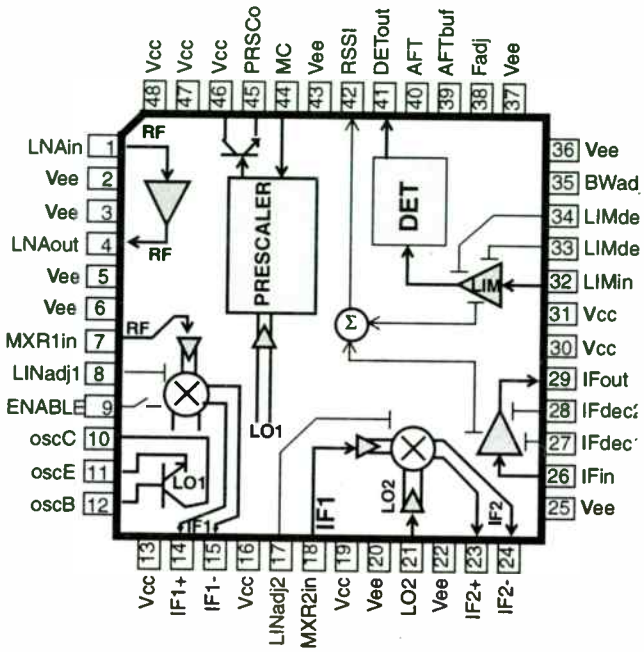

Fig. 17. MC13145 TQFP48 package

D. *MC13146*

The MC13146 (Fig. 18) is an integrated RF transmitter targeted at 900MHz, 1.8GHz and 2.4GHz cordles telephone applications. It features a 50Ω linear mixer with linearity control, voltage controlled oscillator, dual modulus prescaler, and exciter.

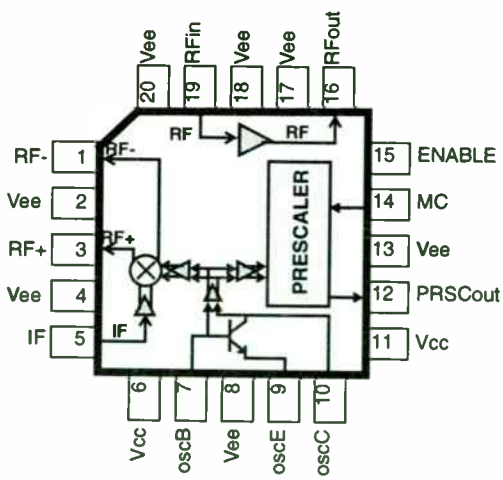

Fig. 18. MC13146 TQFP20 package

VII. EXAMPLE CHIP SETS

A. 900MHz Analog FDD Cordless Telephone

An example of the implementation of a 900 MHz analog frequency division duplex (FDD) transceiver is shown in Fig. 19. This chip set utilizes Motorola's existing ICs to provide a high performance cost effective solution.

B. 900MHz Digital FDD Cordless Telephone

An example of the implementation of a 900 MHz CVSD digital (Continuously Variable Slope Delta) FDD transceiver is shown in Fig. 19. The use of CVSD offers significant cost savings over ADPCM because of its simplicity. This chip set utilizes higher integration to further reduce cost and increase performance with the MC13145, MC13146 and MC33410. For further discussion see [3].

REFERENCES

[1] W. E. Main and J. C. Durec, "A Linear Class AB Single-Ended to Differential Transconverter Suitable for RF Circuits," *Proceedings of the 1996 MTT-S International Microwave Symposium, pp 1071-1074.*

[2] J. C. Durec, W. E. Main and D. Lovelace, "Motorola's Mosaic V Silicon RF Building Blocks Fill Gaps in High Performance Low Power Wireless Chip Sets" *Proceedings of the 1996 Wireless Symposium, pp. 218-223.*

[3] Y. Legrand, "Wireless Systems Improvements through Innovation and Integration" *Proceedings of the 1996 Wireless Symposium, pp. 248-253.*

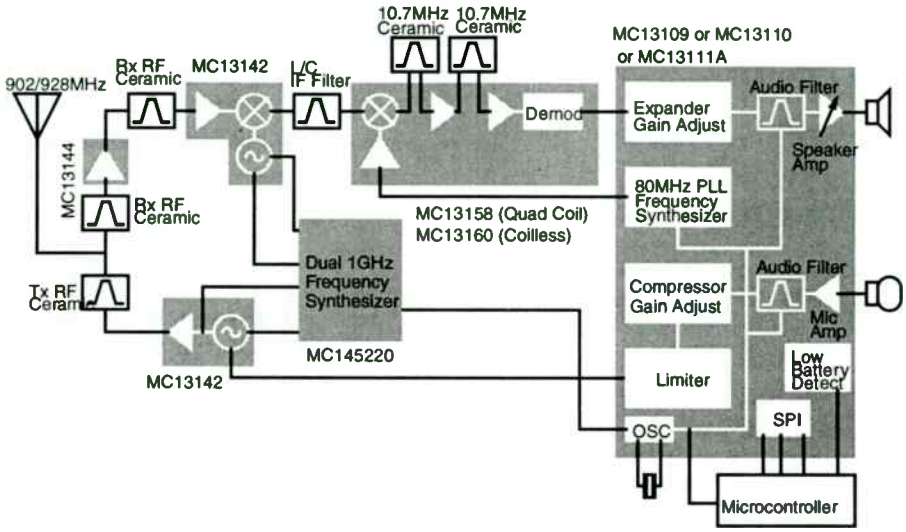

Fig. 19. 900MHz Analog FDD Cordless Telephone

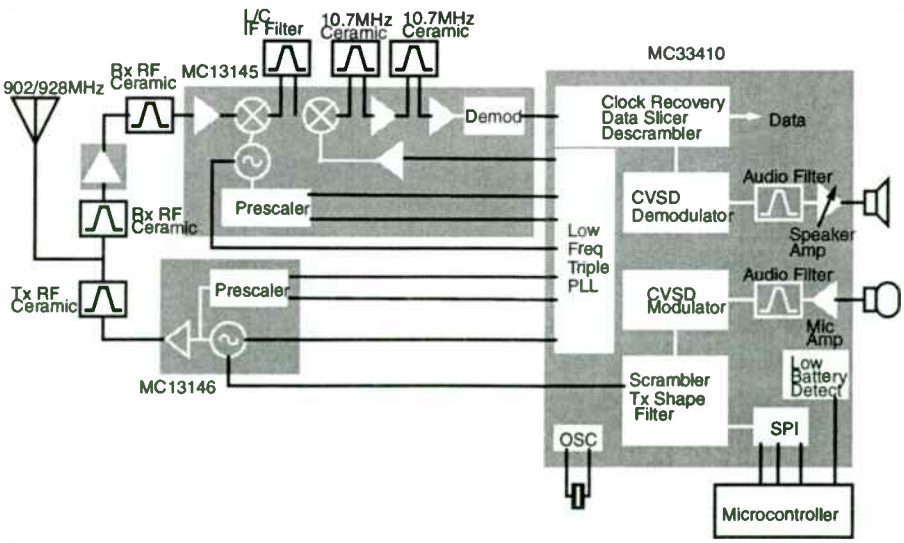

Fig. 20. 900MHz Digital FDD Cordless Telephone

AN INTEGRATED 900MHz SILICON BIPOLAR CASCODE LNA WITH 1.4dB NOISE FIGURE

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Abstract- **A low noise amplifier (LNA) circuit is presented which is suitable for portable wireless applications including cordless telephone. The LNA utilizes Motorola's MOSAIC™ V RF silicon bipolar process. The LNA features a 2-bit control interface which programs the circuit to one of four bias conditions including an off state. The circuit requires only three external matching components to provide 1.4dB of noise figure (NF) and 16.5dB of gain at 900MHz while consuming only 4mA with a 3V supply. The circuit is operable from 6.5V down through 1.8V. A high degree of on chip bias regulation is maintained in each bias state**

I. INTRODUCTION

Communication receiver systems depend heavily on the use of an LNA to set the system noise figure. High demands are put on this block including low noise figure, high gain, low power dissipation and high linearity. More importantly, the device must be cost effective. The combination of low cost plastic packaging, high performance silicon processing and novel circuit techniques has resulted in the development of the MC13144 LNA.

II. SILICON PROCESSING

The MOSAIC V process [1] features a high performance RF NPN which is a very good starting point for integrated RF circuitry.The layout for the RF NPN is shown in Fig. 1. This device features 9 emitters, 11 base contacts and a side collector contact. The wafer probed RF NPN performance characteristics at 1GHz are presented in TABLE 1.

TABLE 1. RF NPN PERFORMANCE (1V, 3mA)

characteristic	value at 1GHz
NFmin (dB)	0.6
G@NFmin (dB)	16.6
Γopt	19Ω ∠21°

Packaged performance will degrade due to the parasitic inductance and capacitance associated with the package as well as the parasitic capacitance of the ESD devices. Additionally, the impedance of the substrate connection plays an important part in determining the isolation characteristics of the amplifier. In order to maximize isolation, low impedance substrate contacts are placed throughout the die.

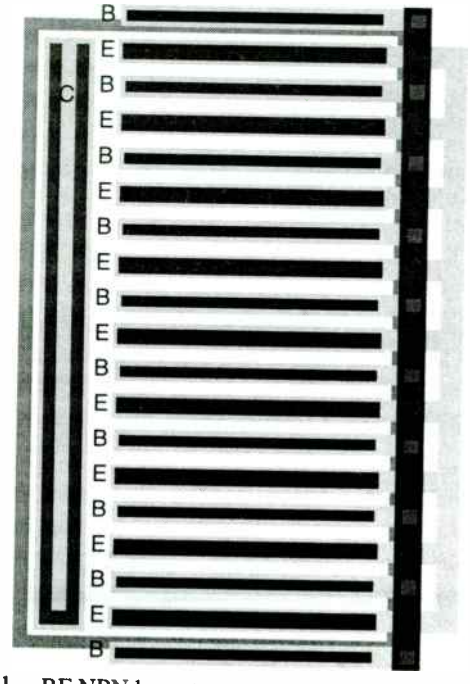

Fig. 1. RF NPN layout

III. PACKAGING

The LNA is packaged in an inexpensive plastic SOIC-8 package (Fig. 2). The package features 1.27mm lead pitch and 4mm x 5mm plastic cavity dimensions. Fig. 3 shows the die placed in the leadframe of the package. The eight lead configuration has ample I/O's to accommodate the RF interfaces, supply pins and control bits.

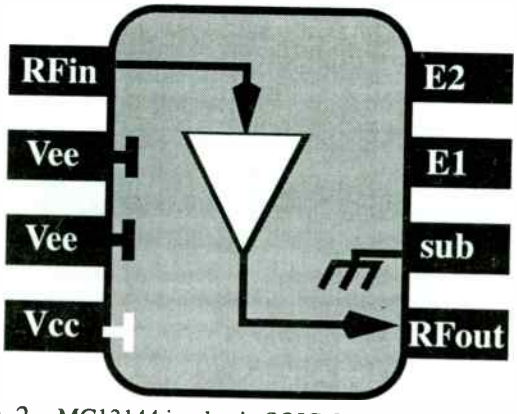

Fig. 2. MC13144 in plastic SOIC-8 package

MOSAIC is a trademark of Motorola, Inc.

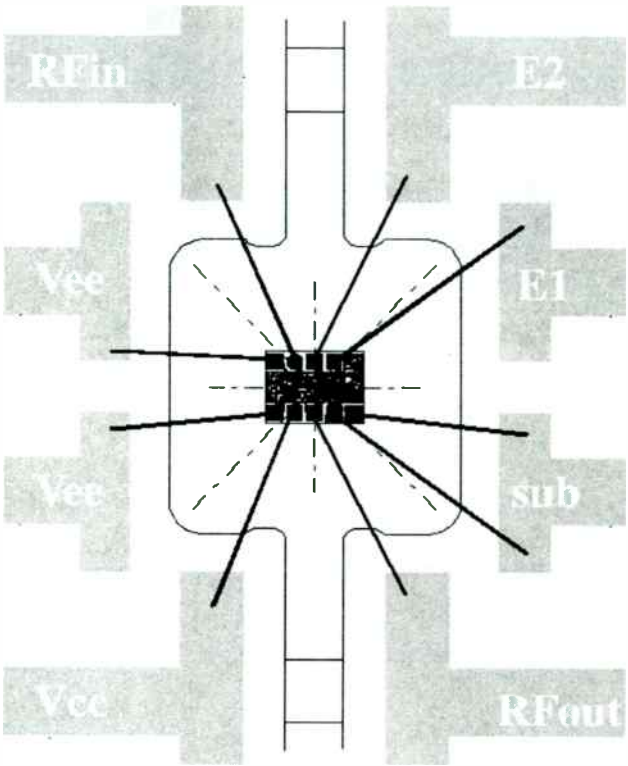

Fig. 3. Leadframe and die

IV. DESIGN GOALS

The LNA was originally designed for use in 900MHz cordless phone applications but is suitable for many other portable wireless applications. The important design goals included:

Low Noise Figure
Low Power Dissipation
Simple External Match
Digitally Programmable Bias
Good Supply Rejection

The programmable nature of the device can accommodate sleep mode, high power and high linearity mode, low power mode and low noise mode. The circuit is designed for fast mode selection and turn on/off.

V. CIRCUIT DESCRIPTION

Extensive use of analog techniques are utilized to control the DC operation of the device. There are only two active RF devices in the circuit but the total transistor count is greater than fifty.

A. DC BIAS METHODOLGY

Often it is required to establish a regulated current and mirror the current up to a higher value. In the circuit depicted in Fig. 4, a current regulator is used as a comparator with a built in reference voltage. The regulated output current is defined in (1). This current regulator is very efficient in that it requires very little overhead biasing current (~1%) to establish the output current. Additionally, the Vreg bias point is very low impedance and can support a significant amount of additional current source outputs.

Define: I_3 = regulated output current
Vt = thermal voltage=kT/q
A, B, C, D = respective transistor areas

Choose: I_1 = $I_3/1000$
I_2 = $I_3/100$

$$I_3 = \left(\frac{Vt}{R}\ln\frac{BC}{AD}\right) - I1 \qquad (1)$$

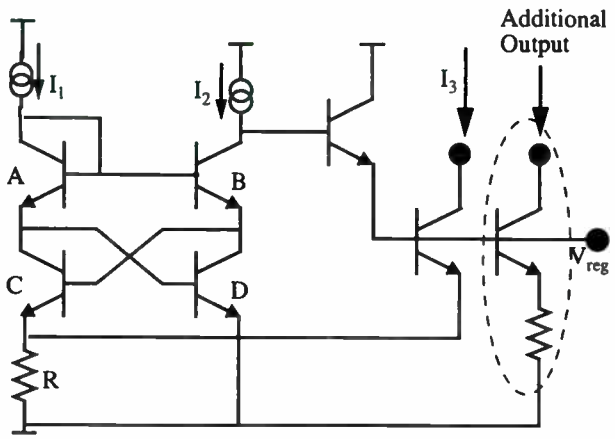

Fig. 4. Efficient current regulator

Occasionally it is desired to switch bias conditions in an accurate manner. The circuit shown in Fig. 5 provides a method for generating three values of output current each selected by one of three unregulaed input currents (I_A, I_B, I_C). The output current (I_D), defined by (2), is selected by asserting the appropriate control current. An extension of this methodology is utilized in the digitally programmable bias current of the amplifier.

$$I_D = \begin{cases} \frac{Vt}{R_{10}}\ln\left(\frac{A_1A_4}{A_2A_3}\right) & I_A \gg I_B, I_C \\ \frac{Vt}{R_{10}}\ln\left(\frac{A_6A_4}{A_7A_3}\right) & I_B \gg I_A, I_C \\ \frac{Vt}{R_{10}}\ln\left(\frac{A_8A_4}{A_9A_3}\right) & I_C \gg I_A, I_B \\ 0 & I_A = I_B = I_C = 0 \end{cases} \qquad (2)$$

The bias methodologies utilized in this design are very insensitive to supply variations. In most cases, early voltage cancellation is utilized to further increase the regulation.

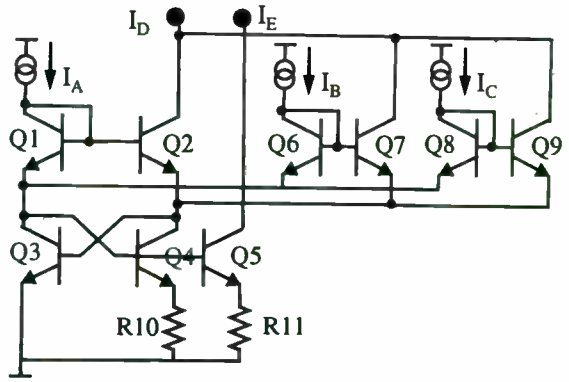

Fig. 5. Digitally programmable current regulator

B. Circuit Operation

Fig. 6 depicts a functional diagram of the operation of the control circuitry and active RF devices. Logic inputs (E1, E2) are asserted to program the device to one of four bias states as described in TABLE 2. Control logic determines the appropriate voltage reference to apply to the positive comparator input of the DC bias circuitry. A current source establishes a 2*Vbe reference voltage applied to the base of the RF cascode transistor. The base voltage of the common emitter transistor is sensed and compared against the reference voltage determined by the control logic. The comparator forces these two voltages to be equal thus establishing the appropriate bias current. An internal load consisting of a resistor in series with a capacitor is attached to the collector output of the cascode device to ensure stability in the plastic package.

TABLE 2. Bias programmability

E1 \ E2	0	1
0	0mA	2mA
1	4mA	8mA

The cascoding of a common emitter amplifier improves stability and available gain. A drawback to this is an increase in the minimum allowable supply voltage as well as peculiar effects at high input powers. Under very large RF input signals, the DC base current of the common emitter and cascode transistors can become very significant. At some point, the base current of the cascode transistor will overcome the available current of the DC current source establishing the 2*Vbe reference. If this happens, the 2*Vbe reference will collapse, causing the common emitter transistor to saturate and reduce the available output current. A sensing circuit prevents this from happening. The DC base current of the common emitter transistor is monitored and fed forward to the 2*Vbe reference to guarantee that there is always sufficient DC base current available for the cascode transistor under all power levels.

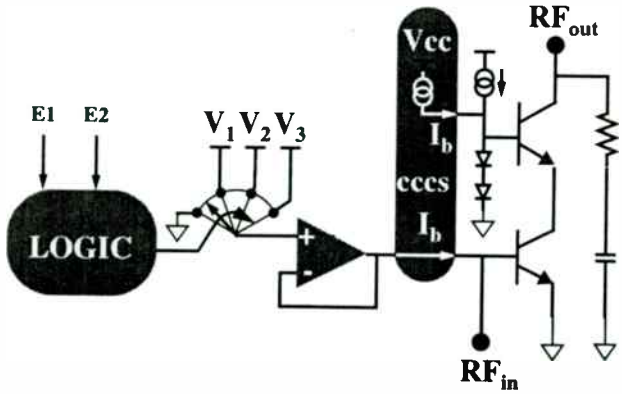

Fig. 6. FUNCTIONAL DIAGRAM

C. LAYOUT

Special care has been taken in the IC layout of the device to maximize signal isolation. Extensive use of substrate contacts and guard rings aid isolation. As shown in Fig. 7, the die size is very small. Double bonding for the substrate pads allows for the net bond wire inductance to be reduced in half.

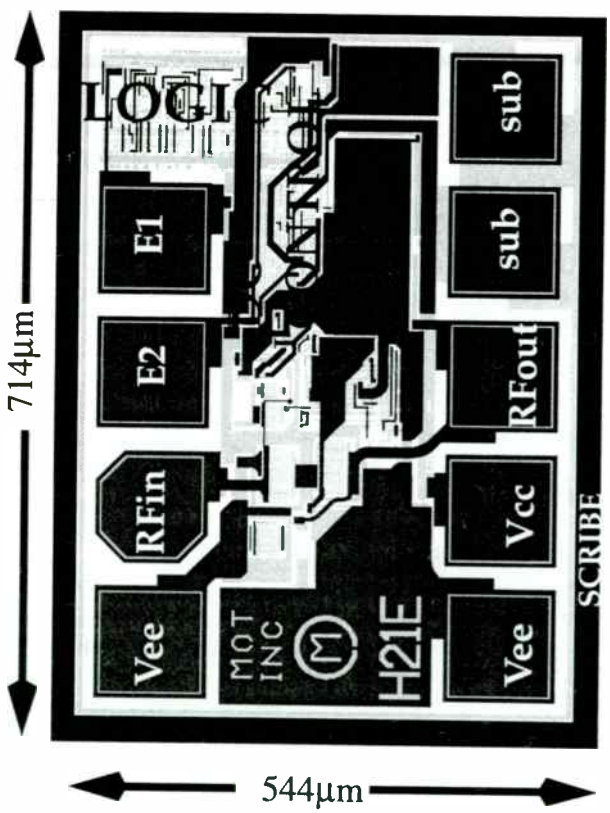

Fig. 7. Die Layout

VI. APPLICATION CIRCUIT

The LNA requires only three external matching components for optimum performance. A series inductor is used at the input. A shunt inductor followed by a series capacitor is used at the output. The circuit was tested using a 14 mil thick FR4 printed circuit board with bottom side ground plane, via holes and top side 1/2 ounce copper (Fig. 8). SMA connectors are attached to each port. The logic inputs E1 and E2 accept DC levels to program the bias state. The resistors in series with the logic inputs is for ease of testing and are not required in the final application circuit. The RF I/O traces are 50Ω transmission lines. The schematic for the application test board is depicted in Fig. 9

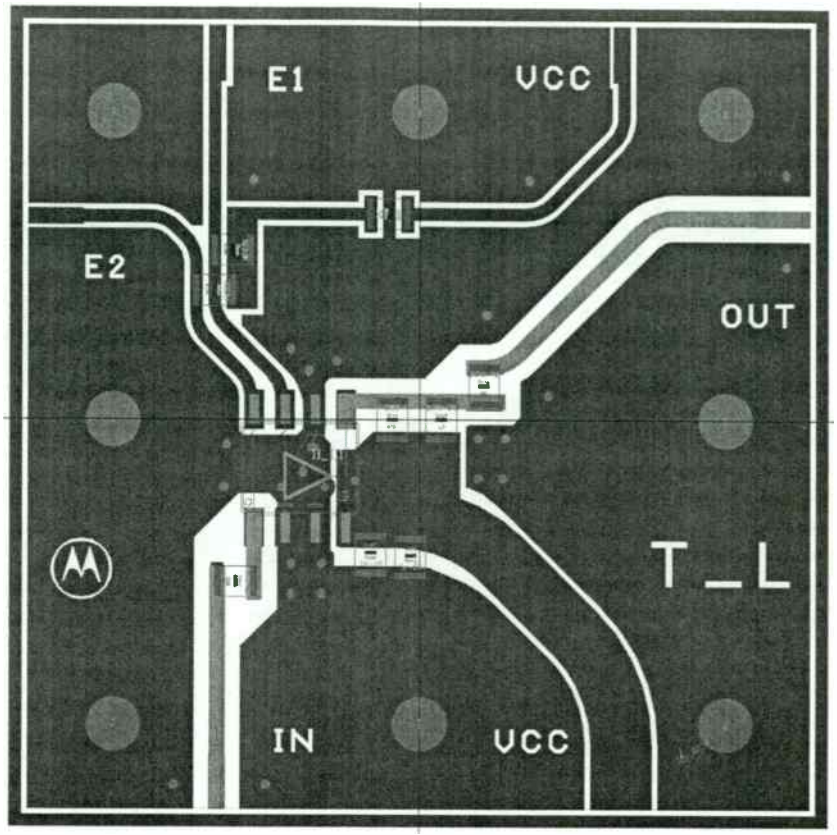

Fig. 8. PCB layout

VII. OPTIONAL EXTERNAL BIASING

The internal biasing can be overridden through the use of external biasing if desired. If E1 and E2 are set to Vee and a DC path from the input of the amplifier to Vcc is provided, such as through a resistor, the amplifier will bias appropriately. A cascode amplifier with no internal biasing typically requires an external bias circuit to establish the quiescent current in addition to a bias voltage for the cascode bias. In the MC13144, the internal circuitry will sense an external bias and still provide the 2*Vbe reference voltage for the cascode bias. Thus, an external cascode reference voltage is not necessary.

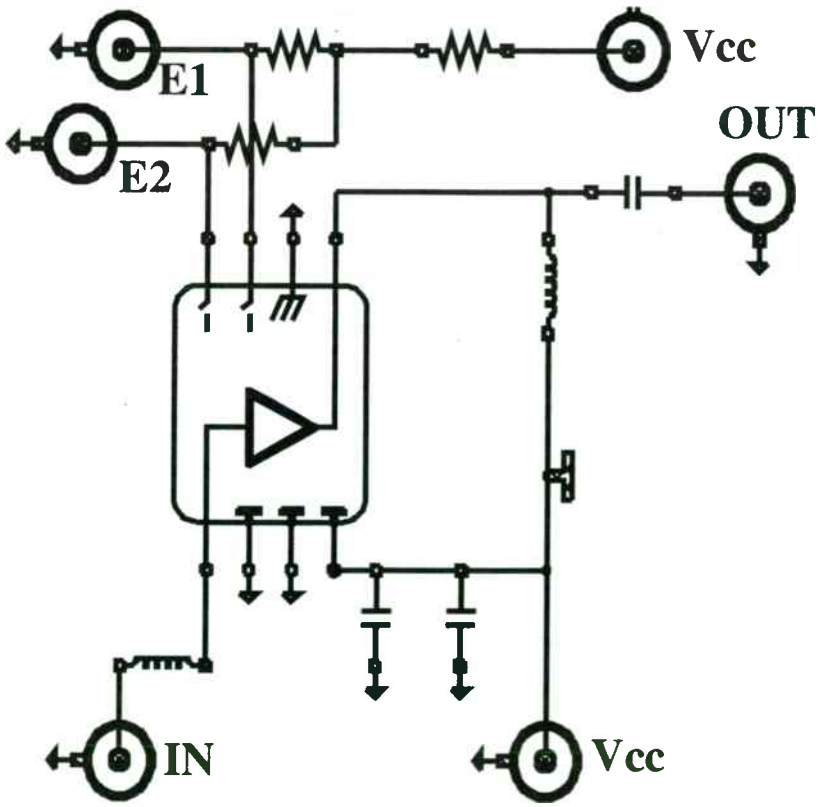

Fig. 9. PCB schematic

VIII. MC13144 PERFORMANCE DATA

The MC13144 packaged in the SOIC-8 plastic package has been characterized yielding the following data. The PC board depicted in Fig. 9 was used unmodified for each test. The test conditions for the following data plots include:

Vs = 3V
RF frequency=900MHz
RF amplitude=-30dBm
E1=0V
E2=3V
Ibias=4mA

Fig. 10 shows the measured noise figure and gain versus frequency for the 4mA bias condition. The external components are tuned for 915MHz operation. The gain at 915MHz is 16.5dB with a noise figure of 1.4dB.

The measured S-parameters for the device are shown in Fig. 11. The output is tuned for maximum gain and the input is tuned for minimum noise figure. The S-parameters change slightly when other active states are asserted. S21 changes +2,-4 dB and S11 changes by -4, +2 dB for the other two states. S22 and S12 are constant as the active states are changed.

Fig. 12 shows the bias regulation of the device where supply current is plotted versus supply voltage for each of the three active states.

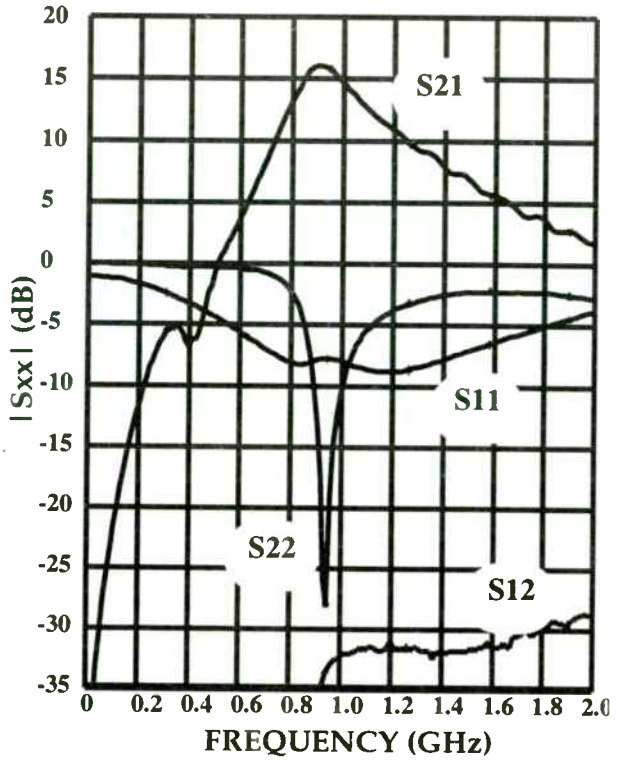

Fig. 11. MEASURED S-PARAMETERS

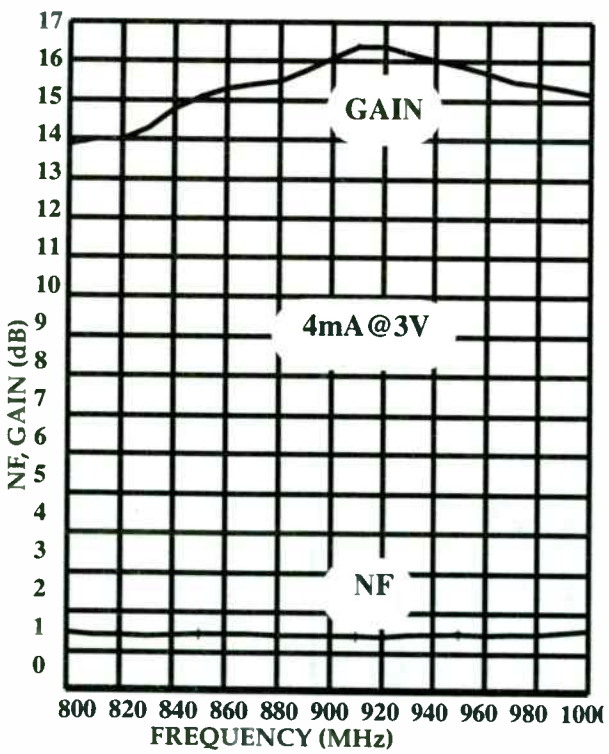

Fig. 10. MEASURED NF vs. FREQUENCY

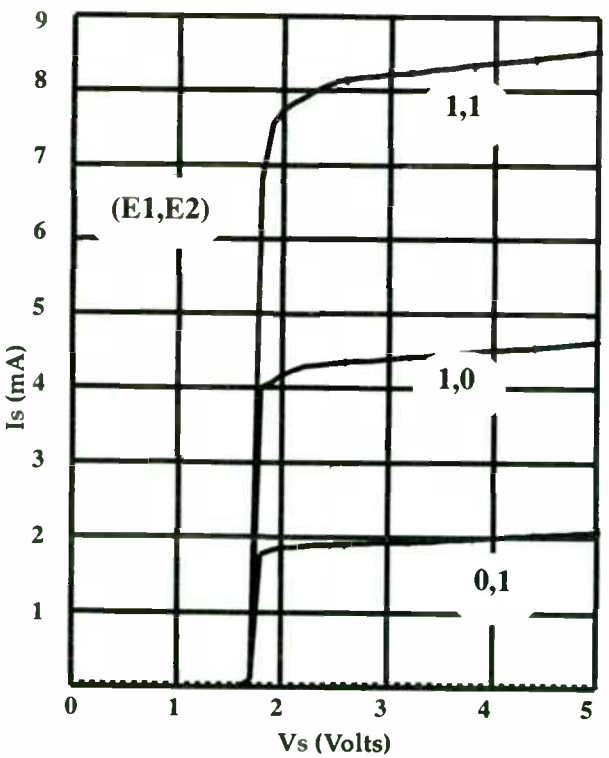

Fig. 12. CURRENT DRAIN vs. SUPPLY VOLTAGE

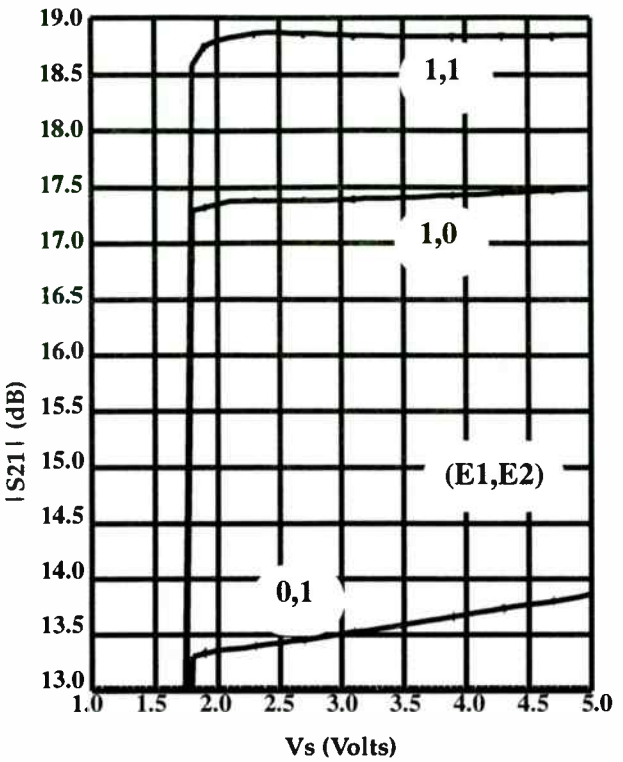

Fig. 13. GAIN vs. SUPPLY VOLTAGE

Fig. 13 shows the sensitivity of the gain to supply voltage variations. Accurate regulation is maintained down through 1.8V. Bias regulation reduces or removes the need for external supply voltage regulation.

IX. PERFORMANCE OVERVIEW

In review, the MC13144 is an integrated 900MHz silicon bipolar cascode LNA with 1.4dB noise figure. A simple external match involving 2 inductors and one capacitor provide for gain as high as 18.8dB (@8mA). The device bias is digitally programmable (0mA, 2mA, 4mA, 8mA) and is functional with only 3.6mW power dissipation (2mA @ 1.8V). The circuit is operable from 6.5V down through 1.8V. A high degree of bias regulation is maintained in each bias state.

X. CHIP SETS

The MC13144 adds to Motorola's growing RF building block library. For examples on how this device as well as other building block parts interface to each other in a system application see [1] and [2].

REFERENCES

[1] J. C. Durec and D. Lovelace, "Silicon Bipolar RFICs for 900Mhz Cordless Phone Applications", Proceedings of the 1997 Wireless Symposium, Feb. 1997.

[2] J. C. Durec, W. E. Main and D. Lovelace, "Motorola's Mosaic V Silicon RF Building Blocks Fill Gaps in High Performance Low Power Wireless Chip Sets" Proceedings of the 1996 Wireless Symposium, pp. 218-223.

[3] Y. Legrand, "Wireless Systems Improvements through Innovation and Integration" Proceedings of the 1996 Wireless Symposium, pp. 248-253.

[4] R. G. Meyer and W. D. Mack, "A 1-GHz BiCMOS RF Front-End IC," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 350-355, Mar. 1994.

SPREAD-SPECTRUM TECHNIQUES

Spread-Spectrum Techniques

Session Chairperson: Graham Barnes,
Glenayre Western Multiplex (Sunnyvale, CA)

SPREAD SPECTRUM APPLICATIONS

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The use of spread spectrum technology for voice and data links has been widely accepted throughout the wireless industry, particularly in the unlicensed ISM bands. The gap between performance expectations and available hardware is closing as new applications are successfully implemented and as actual performance is better understood. This presentation investigates the main applications of spread spectrum radios and the areas of concern to users in their performance. Radio architectures which address the performance areas of noise and interference immunity, together with multipath fading resistance, are presented. Software-defined radios using DSP and wideband A/D and D/A conversion techniques that promise new levels of user programmability are also described. Newer user applications ranging from industrial data to near-live video and PCS connections are examined, as well as the new Part 15 FCC regulations that have been proposed to increase the successful use of these systems, particularly for professional installations.

Processing Gain in Spread Spectrum Signals.

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ABSTRACT

This paper addresses the processing gain (PG) characteristics of Spread Spectrum Systems. PG provides some unique properties to the Spread Spectrum waveforms that can primarily improve performance in the area of interference tolerance. The paper describes the benefits of processing gain and the reasons that the PG properties have been attractive for both military and commercial applications. It describes the signal processing required to implement such systems for Direct Sequence (DS), Frequency hop, and Hybrid Spread Spectrum Systems. The paper gives examples of applications that use the PG properties in communications systems. An overview of the maturity and the state of the art of presently available Spread Spectrum technology is also highlighted.

I. INTRODUCTION.

Processing Gain (PG) is a term used to describe one of the unique properties of Spread Spectrum Waveforms. PG helps to measure the performance advantage of spread spectrum against narrowband waveforms. Spread spectrum waveforms are modulated twice. Once by using traditional modulation techniques such as PSK, FSK, etc. and then, for a second time with the wideband modulation of choice, i.e. Frequency Hopping (FH), Direct Sequence (DS) or Hybrid (FHDS). The wideband modulation tends to spread the signal energy over a wide range of frequencies. The wideband modulation is what provides the basis for the PG in spread spectrum systems.

Spread Spectrum is being used because of a number of attractive properties. Spread spectrum techniques had originally appealed to military systems applications. These attractive properties are partially attributed to the PG. They are used to improve:

- Anti-jamming performance.
- Low probability of intercept, and
- Multiple Access communications.

Commercial applications have adapted spread spectrum technology and they can extract parallel benefits. These are:

- Interference immunity.
- Low transmit power density.
- Multiple simultaneous transmissions.

II. PROCESSING GAIN FOR FH SYSTEMS.

A Frequency Hop (FH) system obtains its wideband modulation characteristics by switching its narrowband signal over a wide range of frequencies in time. Figure 1 illustrates an example of a transmission for a FH system. This is a 3- dimensional figure with the horizontal axis being Time the y-axis being frequency and the z-axis being amplitude. As it is shown during FH the narrowband signal is " hopping " from frequency-to-frequency over time. The narrowband signal is typically modulated using FSK modulation technique variations.

For a Frequency Hop system the PG is defined as the ratio between the instantaneous BW of each hop (narrowband signal) and the overall BW of the transmission channel in dB. The FH system avoids narrowband interference by continuously hopping to a new instantaneous frequency. The FH receiver is impacted by the interferer only when the signal happens to hop at the same frequency with the interferer.

This is best illustrated in Figure 1. The interference area of coverage is overlayed on the 3- dimensional diagram that shows the FH transmission example. As shown on Figure 1, there are only three hop frequencies that have been impacted by the presence of the interference. The rest of the frequencies are interference free and the communications take place uninterrupted. It is obvious from the example that the more instantaneous

frequencies are used and the wider the overall frequency BW is, the greater interference immunity is realized. This is because the signal spends less overall time on frequencies affected by interference. One observation is that FH waveforms can potentially avoid all together the frequencies covered by interference and use the remainder. Conceptually is a valid possibility but regulatory bodies require mandatory usage of all frequencies in a random fashion. This is to maintain a reduced average power density over all the frequencies used in the band.

III. PROCESSING GAIN FOR DS SYSTEMS.

For a DS system, random binary data with a bit rate of r_b bits per sec (bps) is multiplied (Exclusive Or'd) by a pseudorandom binary waveform, which is at much higher rate and it provides the frequency spreading operation. This pseudorandom (PN) binary source outputs symbols called chips at a constant chip rate r_c chips per sec (cps). This is a random noise like signal and hence the name PN signal. The chip rate is always higher than the bit rate, and the ratio of the chip rate to the bit rate in dB is defined as the processing gain. The PG can be viewed as signal to jammer (interference) ratio at the receiver after the despreading operation (removal of PN).

The larger the overall BW used, the higher the PG assuming a constant data rate. A higher PG implies greater immunity against interference. DS signals can actually operate at negative signal to noise ratios given that they possess enough processing gain.

The typical primary modulation for a DS signal is of the PSK variation. If for example the narrowband PSK requires an Eb/No of 12 dB to achieve a certain bit error rate performance, then a DS modulated PSK signal with a PG of 20 dB requires an Eb/No of -8 dB (12dB-20dB). One trade-off that must be carefully worked out is that of total BW vs. PG. The greater the BW the more total interference can potentially be interfering with the DS waveform.

Figure 2 illustrates the concept of processing gain for DS waveforms as seen at the receiver end. The unspread signal is the narrowband PSK signal before applying the wideband modulation. The spread signal is with the addition of the wideband modulation utilizing the PN code. It is apparent that the spread signal is wider in frequency BW but with lower power spectral density per Hz. The spread signal is actually shown to be close to the noise floor. PG for a DS system can be visualized as the jamming margin that exists as the difference between the unspread and spread waveforms.

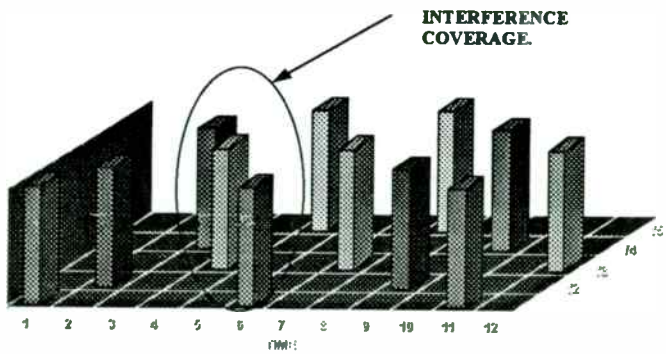


Figure 1. FH Waveform in the Presence of Interference.

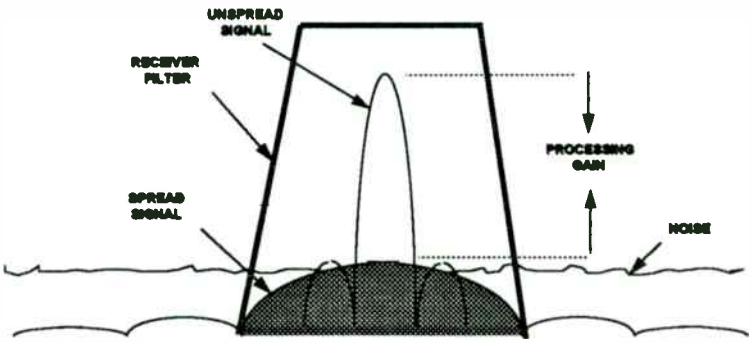


Figure 2. DS Processing Gain concept at the receiver.

The primary benefit of processing gain is its contribution towards interference resistance. The PN code spreads the transmitted signal in bandwidth and it makes it less susceptible to narrowband interference within the spread BW. The receiver of a DS system can be viewed as unspreading the intended signal and at the same time spreading the interfering waveform. This operation is best illustrated on Figure 3.

Figure 3 depicts the power spectral density functions of the signals at the receiver input, the despread signal, the bandpass filter power transfer function, and the band pass filter output. Figure 3 graphically describes the effect of the processing gain on a jammer. The interference (jammer) is narrow, and has a highly peaked psd, while the psd of the DS is wide and low. The despreading operation spreads the jammer power psd and lowers its peak, and the BPF output shows the effect on the signal to jammer ratio.

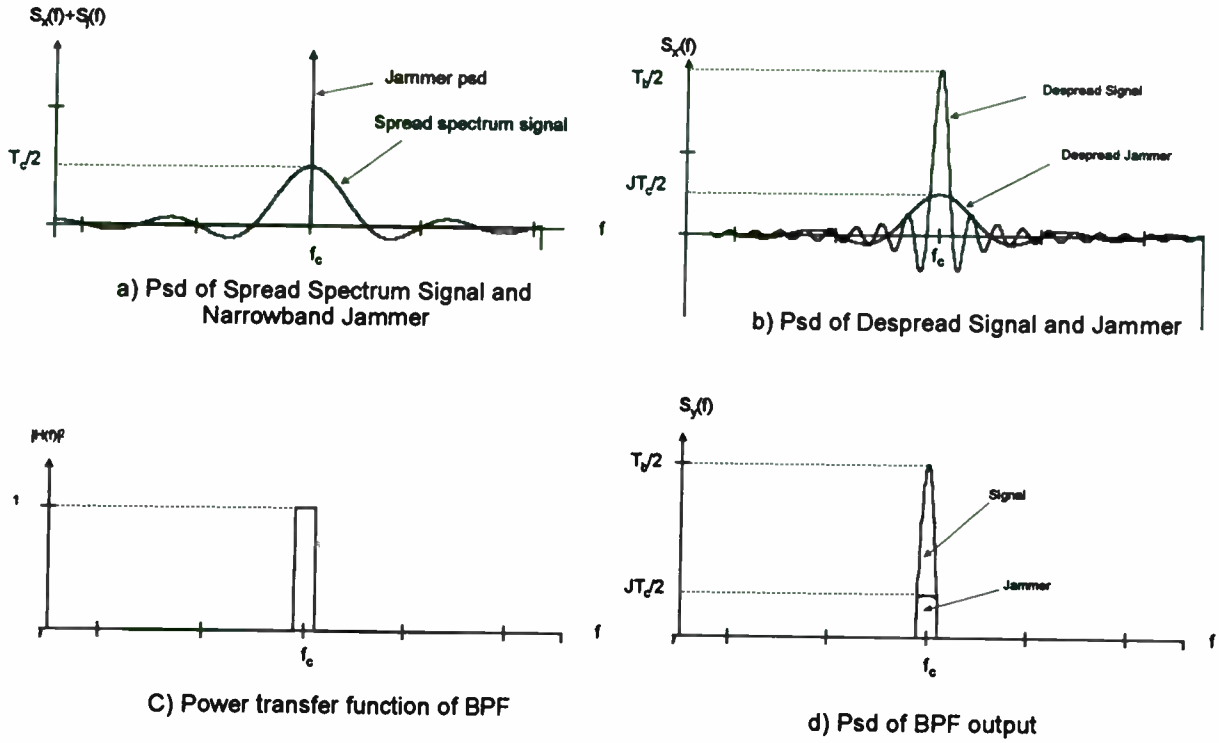
If for example, BPSK modulation is used and an Eb/No of lets say 14 dB is required to achieve a certain BER performance when this waveform is spread with a processing gain of 10 dB, then the receiver can still achieve its required performance with the signal having a 4dB power advantage over the interference. This is derived from the 14dB required minus the 10 dB of PG.

The higher the processing gain of the DSSS waveform the more the resistance to interference of the DS signal.

The classical definition of processing gain is the10 Log[r_c /r_b] in dB. By this definition a system that has a data rate of 10MBPS and a chip rate (rate of PN code) of 11MCPS will have a PG of 10.41 dB. PG

IV. USING THE PRISM™

Harris Semiconductor has developed a state of the art DS radio chip set, the PRISM™ which implements the concept of PG. Using the PRISM™ chip set each data bit is x-ored with an 11 to 16 bit sequence. The processing gain is approximated as the 10Log[11-16] dB where 11-16 is the length of the PN code. If a code with a length of 16 bits is to be used then the processing gain is equivalent to 10 Log[16] dB or 12.04 dB. To this end these PN signals must possess certain mathematical properties to be useful as part of a DS system. Primarily the PN



a) Psd of Spread Spectrum Signal and Narrowband Jammer

b) Psd of Despread Signal and Jammer

C) Power transfer function of BPF

d) Psd of BPF output

Fig. 3 Processing Gain Effect on Narrow Band Jamming

codes that are useful must have very good autocorrelation and crosscorrelation properties as well as maintaining some randomness properties.

The DS receiver is utilizing a reference PN sequence which is a replica to the transmitted sequence. When it detects correlation between the reference and the incoming sequences, it declares initial acquisition and establishes initial symbol timing. Any partial correlations can result in false acquisitions and degradation to the receiver performance. This is why the PN code must have good correlation properties. Some of the PN code classes with such properties are described next.

Codes that have appropriate properties for DS receiver design include the Barker codes, Willard codes and m-sequences with 7 and 15 chips per period which are all implementable using the HSP3824, baseband processor of the PRISM™.

V. PG FOR HYBRID SYSTEMS.

Hybrid signals are a combination of FH and DS signals. The narrowband signal is spread in frequency as in DS and is also being hoped as in FH. For Hybrid systems, since they are a combination of FH and DS, the processing gain is the combination of the FH and DS PG's combined as one parameter. FHDS systems appear to be attractive in theory but implementation is quite challenging making them restrictive for practical applications.

VI. REFERENCES.

[1] J. Fakatselis, and M. Belkerdid, "Processing Gain for Direct Sequence Spread Spectrum Communication Systems and PRISM™ , Harris Semiconductor application note, No. AN9633, August 1996.

[2] Harris Semiconductor "1996 Wireless Communications Seminar Handbook", Melbourne FL., March 1996.

Long-Range High-Reliability Telemetry in Unlicensed Frequency Bands

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1 Abstract

With the highly respected digital high speed spread spectrum techniques emerging, the traditional and well optimized narrow band telemetry systems seem to loose some importance. However, by combining old-fashioned but well proven narrow band radio transmission with modern DSP-technology and intelligent networking algorithms, efficient and robust telemetry networks can be created.

First the paper will describe differences between narrow band and wide band solutions when operated in a non exclusive frequency band, which is the typical situation in Europe. The concept of an air interface will be described, which can operate both in unlicensed and licensed frequency bands, depending on the requirements for system availability and cost. Digital Signal Processing can improve the performance of such an air interface significantly compared to the classical telemetry receiver structures. The potential of such a narrow band telemetry system when combined with modern DSP-technology, advanced network and MAC protocols will be explained.

Finally, the advantages and limitations of such wide range telemetry applications will be derived considering practical applications.

2 Introduction

Narrow band data transmission systems have reached a high level of maturity [IIS94]. Due to the tight specifications arising from a variety of potential applications, especially professional telecommand and telemetry systems have become highly sophisticated and predominantly analogue PCB designs.

But a comparison between consumer PCS systems, like GSM, and state-of-the-art narrow band industrial data transmission systems clearly shows a tremendous gap in performance and price. Technologically, the GSM system is probably 10 years ahead of the vast majority of data transmission systems in unlicensed bands. In sharp contrast to modern PCS, digital components only play a minor role in system control and maybe some „data shaping".

When the digital high speed spread spectrum techniques appeared on the civilian market, VLSI components for digital signal processing became available for data-transmission in unlicensed frequency bands. The traditional and well optimized analog narrow band telemetry systems seemed to loose some importance.

In the meantime, the rapid growth in PCS has prompted a number of chip manufacturers to offer low power DSPs with considerable computational power at reasonable unit prices and relatively low power consumption.

Therefore, recently a DSP supported transceiver has been developed at the Fraunhofer Institut für Integrierte Schaltungen to bring new technology into a market with mature products and relatively slow innovation speed.

By combining old-fashioned but well proven narrow band radio transmission with modern DSP-technology and intelligent networking algorithms, new, more efficient and robust telemetry networks can be created.

3 Spread Spectrum vs. Narrow Band

Different from the situation in the US, in Europe no exclusive frequency band for spread spectrum systems is available. Although significant bandwidth exists at 2,4 GHz, the permitted output power (10mW ERP) is not enough, to achieve reasonable range under realistic indoor conditions.

At 434 MHz, however, only 1.7 MHz bandwidth is available. Basically, this may be enough for a spread spectrum system. But there are a number of drawbacks compared to a high performance narrow band transceiver:

- Commercial direct sequence systems use about 20dB processing gain. The bandwidth of the transmitted data is increased by a factor of roughly one hundred. If two transmitters operate simultaneously, the near-far-problem will prevent any data transmission, if the unwanted signal appears only 10dB higher at the receiver than the wanted signal. A narrow band system, however, can easily tolerate 60dB and more difference between the wanted and the unwanted channel.

- In a densely occupied frequency band like the 434MHz ISM band, a narrow band data transmission system is much more likely to find an unoccupied channel than a wide band spread spectrum system. Provided, the transmission protocol supports frequency changes, such systems guarantees very efficient use of the available spectrum, whenever no administration of the operating transmitters is possible. This is certainly the case on an ISM band, different from the situation that occurs in cellular communication systems.
- Frequency hopping transceivers can be rather robust against interferers. They, however, prevent or make at least very difficult any communication between „friendly" narrow band systems.

4 Analogue RF Front-end with Digital Signal Processing

Various architectures for digital receivers and transmitters have been proposed. Basically, the main difference between them is the way, channel selection is performed and where the ADCs are located in the transceiver signal chain.

The most general approach, which means sampling at a high IF with a wide bandwidth and doing most of the channel selection in the digital domain is certainly not suitable for a low power receiver. The ADC and DAC must have a SFDR of 60 dB or more and a high sampling rate in the range of several ten megahertz. This which means high power consumption.

For the DSP transceiver described in this article, a different approach was chosen. Fig. 1 shows a general block diagram of the design.

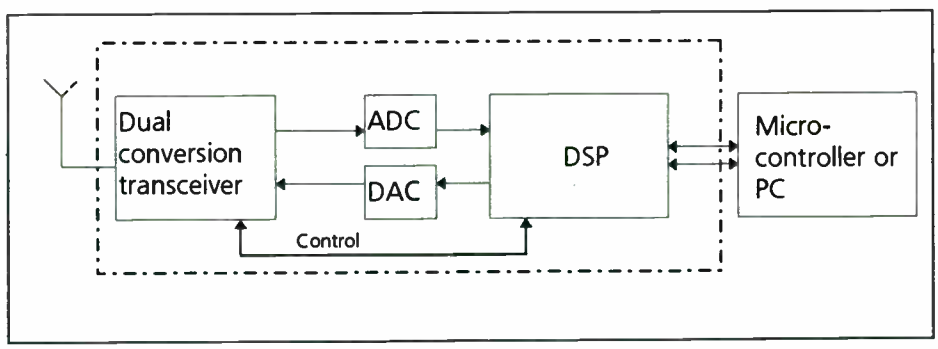

Fig. 1: General block diagram of the DSP transceiver

The system consists of a narrow band high performance front end with a second IF of 455kHz. Analogue filters are used to perform the complete channel selection with more than 60dB selectivity and a bandwidth of 30kHz. This helps keeping the power consumption low.

Using a low IF and a rather narrow bandwidth makes it easy, to use standard industrial ADCs and DACs for IF sampling. These components are cheap, power consumption is about 50mW and a second source is available.

The DSP performs all functions of a digital receiver: the down conversion of the digitized IF signal, demodulation, matched filtering, decision, symbol timing recovery and carrier phase estimation, as far a coherent detection is considered. In addition to this, the DSP can do at least some channel decoding and error correction.

When data is to be transmitted, the DSP carries out channel coding, filtering and upconversion to the IF frequency.

Furthermore, the DSP controls all necessary parameters within the analogue front end, like

- PLL-Synthesizer settings
- RX/TX
- output power
- gain
- bandwidth
- center frequency
- temperature compensation of the reference oscillator

In addition to this, the DSP has access to various test points via ADCs to carry out a self check of the front-end.

Basically, the DSP together with the RF front end forms the physical layer in the ISO/OSI model.

The MAC and DLC is done either by an external micro controller or a PC. These can communicate with the DSP and thus the whole receiver via the host port.

This port is used for all data exchange between the transceiver system and the external controller:

- receive data
- transmit data
- control signals to the transceiver (e.g. desired frequency channel)
- system information from the transceiver (e.g. RSSI)
- firmware download

5 Advantages

Compared to the standard quasi-analog industrial data transmission systems, a DSP-supported transceiver opens up a wide range of new possibilities. Solutions presently established on the market for digital data transmission - except some spread spectrum systems - are predominantly incoherent receivers with discriminators.

Now at least some of the benefits of digital transmission theory can be applied in unlicensed bands for non standardized data transmission systems.

Different to PCS, dedicated digital signal processing hardware performing e.g. de-interleaving or a viterby detection is not available. Every desired function has to be implemented into the DSP program code.

The availability of several ten Mips of computational power - mainly interesting in the receiver - for example makes it possible to

- increase the range of low speed one-way telemetry links drastically by employing coherent detection and convolutional coding
- use powerful algorithms for detection and synchronization in packet oriented wireless networks
- equalize a fading channel
- bandwidth efficient modulation schemes like QPSK or GMSK, which are state-of-the art but difficult to demodulate with purely analog systems, now can be applied in unlicensed frequency bands.

6 Practical realization

6.1 RF front end

The front end is built on one multilayer PCB. To keep costs low, only FR4 material has been used. Exclusively SMT components were selected for this design which makes assembly easier and cheaper. The dimensions of the RF front end PCB are 120x80x15mm. Power consumption is about 70mA for reception and 250mA for transmit.

This transceiver has been originally developed for GMSK transmission which has the advantage of constant carrier power. Nevertheless, the linearity of transmitter and receiver is good enough to test and use also PAM modulation like QPSK.

6.1.1 Receiver

The receiver is a dual conversion architecture. It has been primarily designed to operate in the European ISM band 433.050 to 434.790 MHz. Helix filters serve as preselector. The system concept, however, allows easy adaptation to broader tuning ranges to cover other bands in the 400 MHz range as well.

As first LO a low phase noise VCO together with a single loop PLL are used.

The first IF is 82.2 MHz, which is a standard IF in IS54 systems. High quality SAW filters are available. The second IF is 455kHz, which is a standard center frequency of high quality ceramic filters.

IF amplification is done by a high performance integrated IF system, which contains limiting amplifiers. In case limiting of the received signal is not desired, DSP controlled attenuator pads with a range of 0...60dB are switched into the signal chain. If further attenuation is necessary, the gain of the input stage can be reduced by approximately 20dB.

6.1.2 Transmitter

The transmitter uses the same dual-conversion architecture as the receiver. IF-filters, mixers and, as far as necessary, amplifiers are bi-directional.

This is not really common in ISM data transmission and certainly more expensive than direct modulation of the VCO, but a prerogative for IF sampling. Besides this, it has two big advantages from the RF engineer's point of view:

- A single synthesizer can be used for receive and transmit. Its tuning range is not affected by the choice of the first IF.
- The receive to transmit time can be very short because the frequency of the first LO synthesizer needs not to be changed.
- The PLL bandwidth can be set arbitrarily to achieve lowest microphonics and phase noise. If the VCO is modulated directly, the PLL bandwidth has to be lower than the lowest modulation frequency.

The LO spurious in the output signal are kept down by appropriate filtering in the IF and RF sections. The second LO signal has to be suppressed by more than 80dB to meet the requirements of the European ETS 300.220 or the German FTZ 17 TR 2014.

In order to adapt the transmit power to different national regulations, it can be set by the DSP between 10 and 500mW. Optimized output filters ensure compliance with the different national regulations.

6.2 DSP section

This transceiver is also intended to serve as a platform for experiments with different modulation and coding schemes in the 434 MHz ISM band.

Therefore the DSP section was designed more flexible and with more memory than probably necessary in an application. It can, however, be easily scaled down to the actual demand.

For this design, the Analog Devices AD2781 DSP was chosen. It offers about 33 MIPS. The power consumption is 500mW.

The system has 128k FlashROM for software and data and 32k RAM.

To generate and measure analog control voltages of the RF front-end, precision serial ADCs and DACs are located on the DSP board.

One serial port of the DSP is used for IF generation and sampling. The interface between analog RF section and the DSP is of paramount importance for the performance of the transceiver. Its design is mainly a trade-off between low power consumption and performance of the transceivers. In this design, undersampling the IF frequency helps saving power.

The IF frequencies of the RF front end suggest a symbol rate of the transmission of 32,5ksymbols per second. A resolution of 8 bit is easy to achieve with standard industrial converters. The converters used in this system have offer a SFDR of 46dB.

7 System Considerations

Looking at only a single broadcasting station, a highly robust and reliable wireless link implemented by a powerful receiver is the key for successful data transmission. But in practice, wireless communication will only be efficient if the available spectrum is shared among all potential transmitters in the same area and frequency band. This is true particularly for communication in unlicensed and licensed band designated to several applications.

7.1 Medium Access Control

To allow the coexistence of several broadcasting stations, some kind of medium access control (MAC) has to be used to avoid such simultaneous transmissions which most likely result in the loss of all the colliding messages. Even more, because higher levels of the communication protocol will usually try to retransmit messages not acknowledged by the destination, the capabilities of the MAC protocol will determine the average bandwidth requirements and the saturation point of the network. If an inefficient MAC strategy is used – e.g. by implementing an „aloha" protocol which has no MAC at all – the average traffic offered to the network must be limited to a very small fraction (less than about 30%) of the available bandwidth to avoid saturation resulting in a dramatically decreasing throughput.

To design an efficient MAC protocol, the basic structure of the wireless network and the communication structure of the application has to be considered first. In Fig. 1, two basic topologies are shown.

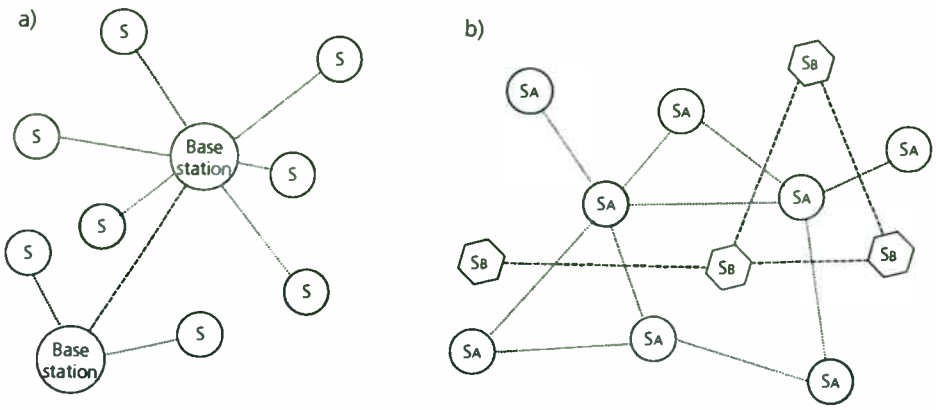

Fig. 2: Basic Topologies

In Fig. 2a, all stations in one coverage area are grouped around a single base station. Thus, the communication of all the „slaves" (ordinary stations) in the network might be easily coordinated by the single „master" (base station). For example, this might be done by cyclic polling of the slaves. Or, the base station might provide global synchronization for all slaves which is the basic requirement for MAC strategies based on time division (TDMA). The overhead of such an approach is very small, thus allowing a very efficient usage of the available bandwidth. The main drawback is the fact, that administration and planing of the network is mandatory and that a dedicated base station is required. Usually, such topologies are only possible in licensed bands designated to a single application using a fixed protocol, e.g. telecommunication networks running the GSM or DECT protocol.

Fig. 2b shows a structure that is more typical for wireless control networks and wireless extensions to fieldbuses or local area networks using licensed or unlicensed bands. Their main characteristics are:

- free topology with only partial connectivity
- no administration or planing
- systems from different vendors with non-compatible air interfaces (e.g. different modulation schemes or speed)
- large number of nodes

Due to the absence of central control and coordination, only distributed algorithms for MAC can be used. Typical MAC algorithms for such systems are based on CSMA (carrier sense, multiple access), where every station has to monitor the channel and will only be allowed to transmit if the channel is sensed to be not in use by others.

The criteria for this decision might either be a „received signal strength" (RSS) measurement or the decoded information itself. Using RSS, a station will defer its transmission if the strength of the incoming signal is higher than a certain threshold. This has the advantage that even the transmission of other stations that cannot be decoded (non-compatible air interface, weak signal) will be

preserved. On the other hand, high levels of background noise might block (potentially successful) transmissions for an undetermined long time. Interpreting the information in the received signal itself might provide better throughput, but will ignore all transmission from systems that cannot be decoded correctly. Thus, a combination of both criteria, with a low sensitivity of the RSSI measurement, should be used to allow a „friendly" behavior with respect to compatible and non-compatible systems.

On a half duplex link, the time required for switching from receive to transmit mode (R2T time) is the critical parameter for the efficiency of CSMA. This is due to the fact that other stations will sense the channel as „not in use" during this R2T time and might simultaneously start transmitting. The longer the R2T time, the higher the probability that a collision between two or more stations will occur. Thus, for an efficient implementation, an air interface with short R2T time is preferable but not always feasible.

The decision to transmit or not is based on the local view of the broadcasting station – which might not match the situation on the receivers side, because a third station near the receiving but far from the broadcasting station is active („hidden node" problem). If the broadcasting station starts its transmission under such circumstances, the message might not reach its destination. Because the impact on the efficiency of the network depends on the length of the lost message, it is advisable to used short messages in a RTS-CTS sequence (request to send, clear to send) to check the presence of the designated receiver first, before transmitting larger amounts of data. The RTS-CTS sequence might also be used for the reservation of the channel if the time required for the following data transmission is encoded into the RTS and CTS packet. Any station receiving either a RTS or CTS packet might defer its own transmissions until the channel is not in use.

The main disadvantage of CSMA on a wireless link arises from the fact that a broadcasting station usually cannot detect collisions while transmitting. Thus it is not possible to stop the transmission as soon as a collision occurs and typically all messages colliding will be lost, wasting the capacity of the channel for the duration of the longest message. Because the probability of a collision immediately after the end of a packet is extremely high – all stations that sensed the channel busy are waiting for the end of the transmission and will start broadcasting immediately afterwards – additional collision avoidance (CA) should be used: To do this, a certain period of time following after the end of a transmission is divided into a fixed (or variable, depending on offered traffic) number of equal „arbitration slots". Each slot has to be long enough (longer than R2T time) to allow the detection of a transmission that started at the beginning of the slot until the beginning of the next one. To avoid potential collisions, each deferred station selects one of the slots on an arbitrary basis and will start broadcasting only if the selected arbitration slot is reached and no other transmission is sensed in the meantime. Because the number of arbitration slots is usually much higher than the average number of stations willing to transmit, the probability that two (or more) stations chose the same arbitration slot is very low, thus minimizing collisions. Using arbitration slots, even an additional priority mechanism might be implemented to provide some

kind of determinism in the no deterministic CSMA MAC protocol. To do so, a certain number of (the first) arbitration slots will be reserved for priority messages. The lower the slot number used, the higher the priority of the message.

7.2 Implementation

Most of the concepts for MAC based on CSMA described above can be found in IEEE publication P802.11 „Wireless LAN Medium Access Control and Physical Specification" [IEEE94]. Since this standard primarily deals with wireless local area networks, including station mobility between different coverage areas (BSS) and integration with wired LANs, most of the additional elements of this standard are not required in a much simpler wireless control network. Thus, the IEEE 802.11 standard and its objects served as a basic guideline for the structure of our implementation, but only a subset of its scope was actually implemented. This includes:

- transmission of unacknowledged and acknowledge messages in an ad-hoc network
- MAC based on CSMA with additional collision avoidance (CA): The number of arbitration slots used for CA is self-adaptive; non priority and up to 16 priority messages are supported.
- RTS-CTS handshake (optional, dependent on message length) for channel reservation and for the avoidance of the „hidden node" problem.
- fragmentation of large message into sub-messages. This may be used to tune data throughput depending on the quality of the wireless link.
- most of the parameters of the protocol are adjustable to adapt to the characteristics of the channel and the demands of the application.

The protocol was implemented in 'C' using an 8 bit microprocessor (78K0 series from NEC, [NEC95]) running at 5 MHz with 8K of external RAM (used for buffering incoming and outgoing messages). One of the serial channels of the processor serves as communication interface to the host processor. This serial interface is similar to the widespread SPI interface, supporting a (configurable) data rate from 19,5 kbps up to 1,25 Mbps.

7.3 Performance Measurements

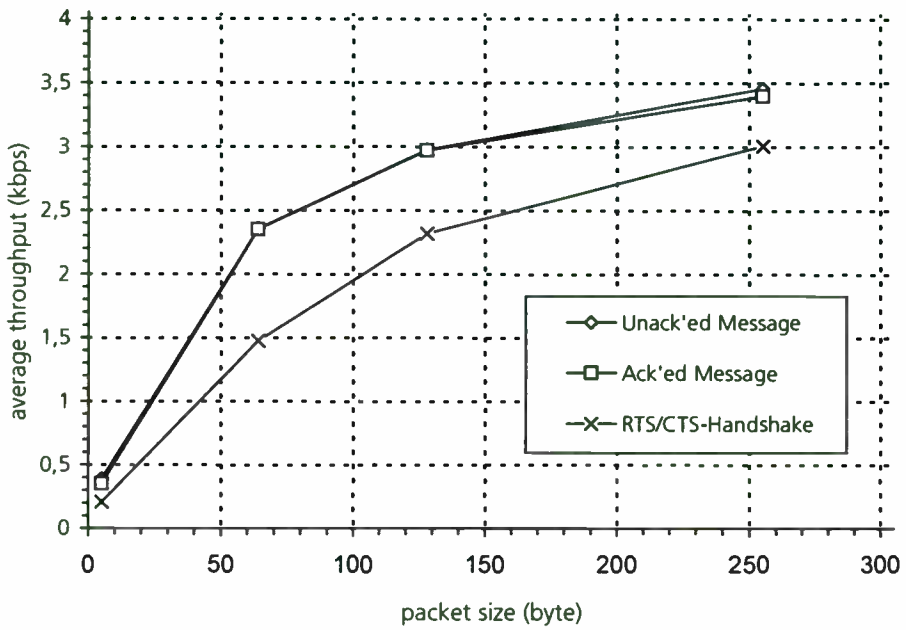

Fig. 3: Performance for different message types

Fig. 3 shows some basic performance measurements for this implementation using different message types and packet sizes. The RF transceiver used for the experiment provided a raw data rate of 10 kbps while the serial interface was configured to 19,5 kbps. The average throughput given in the figure is derived from the measured delay from the beginning of the communication with the transceiver (over the serial host interface) and the end of message reception in the target host; thus this time already includes twice the serial communication between host and transceiver, the processing of the message inside the transceiver and the transmission over the wireless link.

8 References

[IIS94] THILO LENHARD, ALBERT HEUBERGER, RAINER PERTHOLD, LUDWIG WALLRAPP, MAX HECKL: Flexible UHF Data-Transmission System Has Broad Tuning Range. In: *Microwaves & RF Product Extra*, March/April 1994

[IEEE94] IEEE COMPUTER SOCIETY: *P802.11 Wireless LAN Medium Access Control (MAC) and Physical Specification*. New York, 1994 (Unapproved Draft 20b3)

[NEC95] NEC CORPORATION: *User's Manual, μPD78054 Subseries 8-Bit Single-Chip Microcontroller*. Japan, 1995 (Document No. IEU-1356B)

Direct Sequence versus Frequency Hopping Spread Spectrum Modulation for IEEE 802.11 Applications at 2.4 GHz

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Abstract

Two types of spread spectrum have been approved for use by the FCC in the unlicensed ISM band because no one knows for sure which is best. The 802.11 WLAN committee did not settle this argument and chose to allow the user to decide. This paper analyzes an approach to determining the performance tradeoffs so that a network engineer can make a decision. The approach is based on determining the maximum data flow per acre or the maximum number of networks per acre. The analyses done to date show that up to 13 collocated FH networks can be placed before network throughput peaks. Only 3 or 4 DS networks following the 802.11 standards can be collocated before the spectrum is filled. Does this mean that FH is the right choice? Let's examine further. The next group of 13 FH nets must be placed a long distance away before their interference with the first group is minimized. DS nets, on the other hand can be placed much closer to other DS nets on the same channel due the interference resistant nature of the DS waveform. From this reasoning, the maximum number of nets per acre or per square mile can be determined and a more intelligent choice made. Which is more important, a tight group of nets in your facility or a broad coverage area. Is the possibility that a neighboring facilities' network might interfere a concern? What else can be done for maximizing network throughput and minimizing latency. Which type spread spectrum is best for time bounded traffic? These questions are examined and some conclusions proposed.

1. Introduction

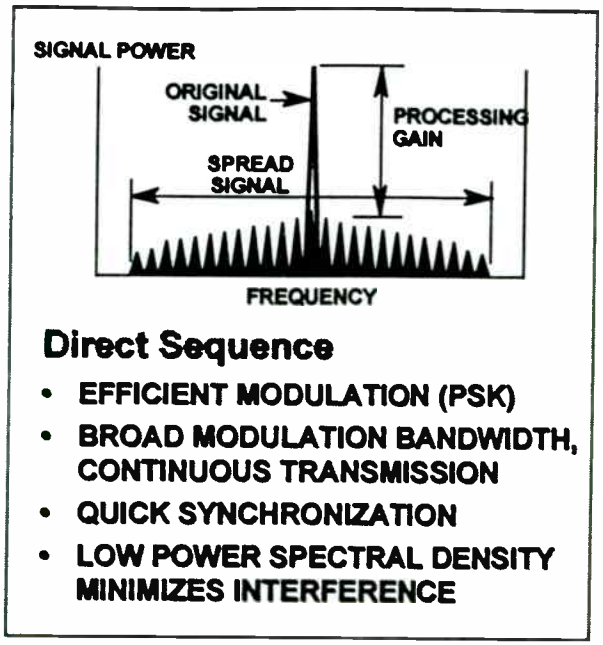
When it comes to the relative merits of (DS) versus frequency hop (FH) spread spectrum modulation schemes, the answer is: *it depends*. Choices depend on the particular implementation scenario. Hopefully, this article will dispel some of the confusion and allow engineers to pick the best choice for their particular job. Some observations are general, others relate to specific FCC part 15.247 requirements for the 2.4-GHz ISM band or to the portions of the draft IEEE 802.11 spec for interoperability in that band.

2. Spectral Density Reduction

Both DS and FH reduce the average power spectral density of a signal. The way they do it is fundamentally different and has serious consequences for other users. The objectives are to reduce both transmitted power and power spectral density to keep from interfering with other users in the band. The FCC has rules for both and you need to conform to these rules to stay legal and to avoid annoying other radio users.

DS spreads its energy by rapidly phase-chopping the signal so that it is continuous only for very brief time intervals. These intervals are called chips and are at least 10 times shorter than the data bits they chop. Thus, instead of all the transmitted energy being concentrated in the data bandwidth, it is spread out over the spreading bandwidth. The total power is the same, but the spectral density is lower. Of course, more channels are interfered with than before, but at a lower level. If the spread signal comes in under the noise level of most other users, it will not be noticed.

A DS spectrum exhibits discrete spectral lines that are related to the length of the sequence used for the spreading. In 802.11, the spreading uses an 11-bit barker sequence, so you would expect 11 lines (peak to null). Each line is further smeared by data scrambling, which spreads each spectral line and therefore fills in between the lines to make the spectrum more nearly continuous. The overall spectrum profile is $\frac{\sin X}{X}$, which is humped up in the middle. Thus the interference is greatest at the channel center and it rolls off at the edges. Fig. 1 shows both DS and FH modulations.



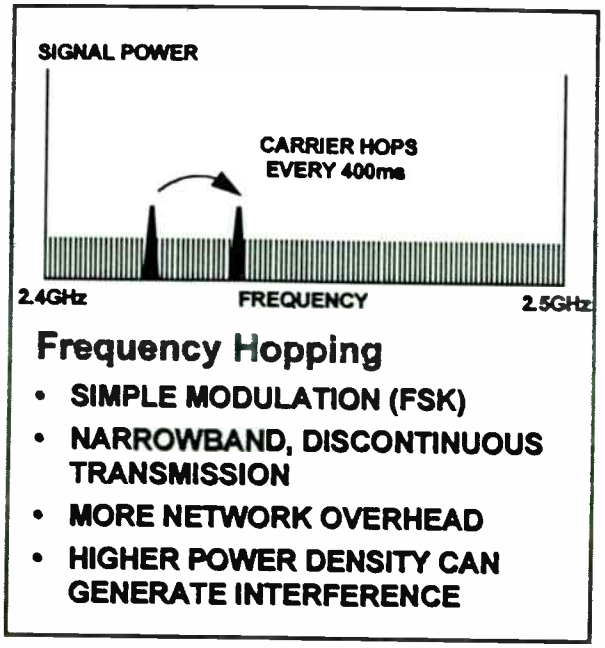


Fig. 1, DS and FH Modulation

Traditional FH signals lower their average power spectral density by hopping over many channels. During any one hop, however, an FH signal appears to be a narrowband signal. With slow hopping, the interference reductions are slight. A narrowband radio being interfered with will experience a pop or burst of noise when the hopper hits its channel. The main reason that 802.11 (and GSM) use hopping is not to minimize interference, but to share the pain of bad channels and to allow multiple uncoordinated nets to share the same spectrum.

If there are a lot of asynchronous FH radios using different hop sets in a given band, the overall effect is to spread out the energy over the whole band.

The spectrum of the FH signal modulated to conform to 802.11 concentrates the signal energy close to the channel center which is an inefficient use of the bandwidth. Additionally, FSK, is less power efficient than PSK, as will be shown, so more transmit power is needed. This power efficiency is further compromised with a low deviation ratio in order to conform to the FCC rules on occupied bandwidth. These rules state that the 20 dB bandwidth be less than 1 MHz. With the low deviation ratios required to conform to this specification for 802.11 FH WLANs combined with the inefficiency of GFSK modulation, the transmit power required to achieve a given range is substantially greater than for DS. Since the best overall interference reduction technique is to radiate less power, this gives an edge to DS.

3. Interference Susceptibility

So far, we've looked at the interference caused by spread-spectrum modulation schemes. The other side of the interference coin is that spread spectrum reduces the effects of other signals on the desired signal. The way FH and DS accomplish this is different, however. In DS receivers, the de-spreading operation multiplies the incoming signal by a local replica of the spreading waveform. This correlates with the desired signal to collapse it to the data bandwidth, while spreading all other signals. After the de-spread signal is filtered to the data bandwidth, most of the noise is outside this new narrower bandwidth and is discarded. Although, this helps with all types of narrowband and uncorrelated interference, it has no advantage for wideband interference such as the microwave oven, since spread noise is still noise and the percentage that falls within the data bandwidth is unchanged. One drawback of DS is that the bandwidth over which the interference is damaging is wider than for a non-spread system. This requires that the channels be spaced wider and well away from high-power signals such as broadcast stations.

The FH signal is agile and does not spend much time on any one frequency. When it hits a frequency that has too much interference, the desired signal is lost. In a packet switched WLAN network,

this results in a re-transmission, hopefully on a clearer channel. In a fast enough FH system, the portion of signal lost may be recovered by spreading the data energy out in time through forward error coding, but only if the FEC spans more than one hop in time. For the very low hop rates suggested for 802.11 WLANs, forward error coding is not practical.

The ability of any signal to tolerate interference is also related to the minimum system Eb/N0[1]. A lower Eb/N0 means that the system can tolerate a dirtier signal. Therefore, the power efficiency of the modulation should be as high as possible. The standard is BPSK, which is recognized as efficient and robust. DS signals usually use BPSK, since there is no jamming resistance advantage to QPSK, but 802.11 specifies QPSK at 2 MBps to maintain the FCC-mandated 10-dB minimum processing gain. It doesn't make any difference, however, since the required Eb/N0 doesn't change.

If the 802.11 DS system operates at 13.4 dB Eb/N0 as discussed below, it can tolerate interference up to a level -3 dB relative to the desired signal. (This also means that there is no code division multiple access (CDMA) capability, since the processing gain and required Eb/N0 do not allow another signal of the same power to occupy the same channel.)

For the purposes of this discussion, FH is narrowband GFSK, since it doesn't hop during a packet. There is no processing gain during a packet and the signal is less power efficient. IEEE 802.11 allows 24 dB Eb/N0 for 1 MBps (and 29 dB for 2 MBps). The theoretical performance is only 5 dB better than this , so the 1-MBps FH system can only tolerate in-band interference up to -19 dB relative to the signal carrier. Compared to DS, this is 16 dB less tolerant. However, FH is more tolerant of interference that occurs outside its 1-MHz signal bandwidth, since the receiver filters will reject it.

To summarize, broadband noise affects both FH and DS similarly, so the system with the better Eb/N0 (i.e. DS) will be more immune. Narrowband interference will have a more severe impact on an FH signal than on a DS signal if it is on the same channel but a less severe impact if it is on a different channel

4. Near/Far Ratio

Near/far effects are often put forth as a limitation for DS. However, they also affect FH and narrowband signals. The term near/far refers to the effects on a receiver from a transmitter operating on its frequency that is nearer to it than the transmitter you want to receive from. DS signals can operate with much better near/far ratios than FH signals since they have processing gain. On the other hand, since they operate over a wider bandwidth, they have to deal with more extraneous signals. On a given channel, distant FH signals are blocked by nearer signals, but, theoretically, as long as they can hop to another channel and re-transmit they can get around the problem.

5. Multipath

DS suppresses multipath by decorrelating the delayed signal. When multipath signals are delayed by more than one chip relative to the direct-path signal, the direct signal has a processing gain advantage. When the multipath signal arrives within a one-chip delay, this creates fading. That is, the direct signal can be either enhanced or suppressed. Therefore, for DS to achieve significant multipath rejection, its bandwidth must be wider than the coherence delay of the environment. For 802.11 the chip rate is 11 MCps, so the coherence interval is 1/11 M, or about 91 ns. This will provide good multipath protection in large warehouses, but less in office buildings.

For FH, multipath signals always arrive within the signal's coherence interval and cause fading. The coherence interval, in this case, is the symbol duration. This causes some paths to be unusable, and that's why this waveform is hopped.

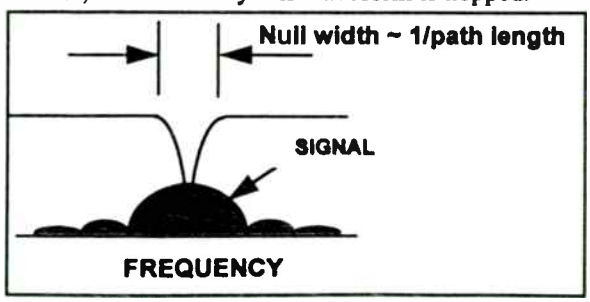


Fig. 2, Channel Response

[1] Energy/bit. Eb/N0 = C(dB) - N(dB) + NBW - 10log(R), where
C(dB) = signal power
N(dB) = noise power
NBW = the channel's Noise Bandwidth, expressed in dB(10log(f))
R = data rate in bits per second.

One way to look at the multipath effects is to look at the spectral nulling that occurs in the channel response.
broadband and can take out a significant part of the DS spectrum. For longer paths, the spectral null is narrower in bandwidth and can take out less of the DS energy. For FH, the spectral null takes out most of the signal energy since the signal is narrowband and falls well within the null bandwidth. Again, DS is effected less but over a wider range of frequencies than FH.

When the direct path and indirect path signals are short, the spectral null that occurs is losses). The Harris Prism™ demodulator (HFA3824), for example, has 2.8 dB implementation loss, for a net 13.4-dB Eb/N0.

The 802.11 FH narrowband GFSK signal, which is power inefficient within the given constraints, requires 19 dB Eb/N0 when used with the greatest modulation index that will fit in the allocated bandwidth. Based on FCC rules, the

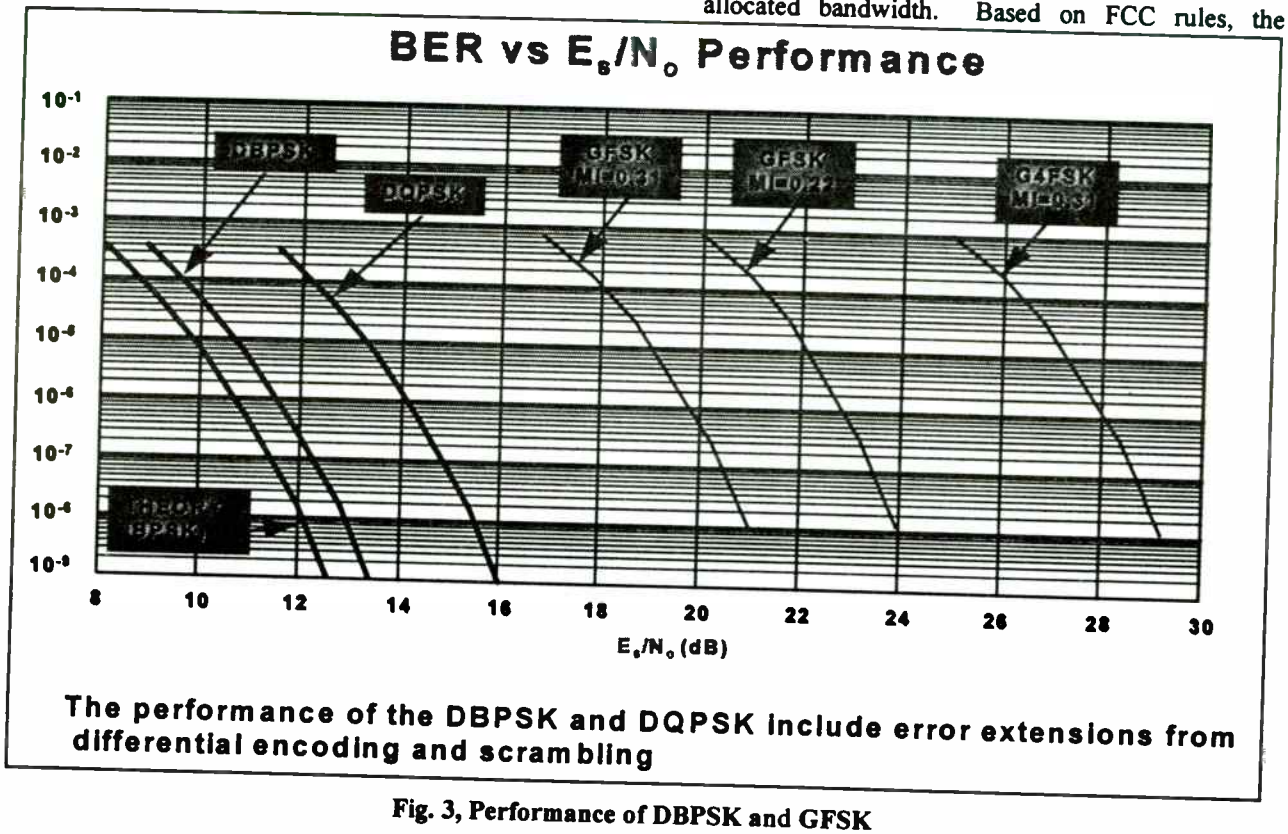


Fig. 3, Performance of DBPSK and GFSK

6. Comparison of DPSK and GFSK modulations

BPSK and QPSK are modulation schemes that are well known to give close to the best power efficiency available along with reasonable bandwidth efficiency. The bandwidth efficiency is discarded with DS spreading in order to lower the power spectral density. There are additional losses with differential encoding and scrambling that cause a loss in performance due to error extension. This means that for every error that occurs, the differential decoding extends that to 2 errors and descrambling further extends that to 6 errors. Thus, you can expect the theoretical 9.6 dB Eb/N0 performance for 10^{-5} BER to be degraded to 10.6 dB (plus implementation

bandwidth allowed the FH signal is 1 MHz at -20 dB. This is too narrow for efficient transmission at 1 MBps, and is even more inefficient for the 4-FSK used for 2 MBps, because the allowed deviation ratios are minuscule. This does, however, keep the overall spectrum occupancy low and allows more channels in a given band. In a 4-FSK demodulator that uses conventional limiter/discriminator techniques without coding, the expected power efficiency performance will be much worse than QPSK.

The curves in Fig. 3 show the Es/N0 performance of DBPSK, DQPSK, GFSK, and G4FSK. Two modulation indices for GFSK are shown. They represent the minimum modulation index and the nominal index. A systems designer

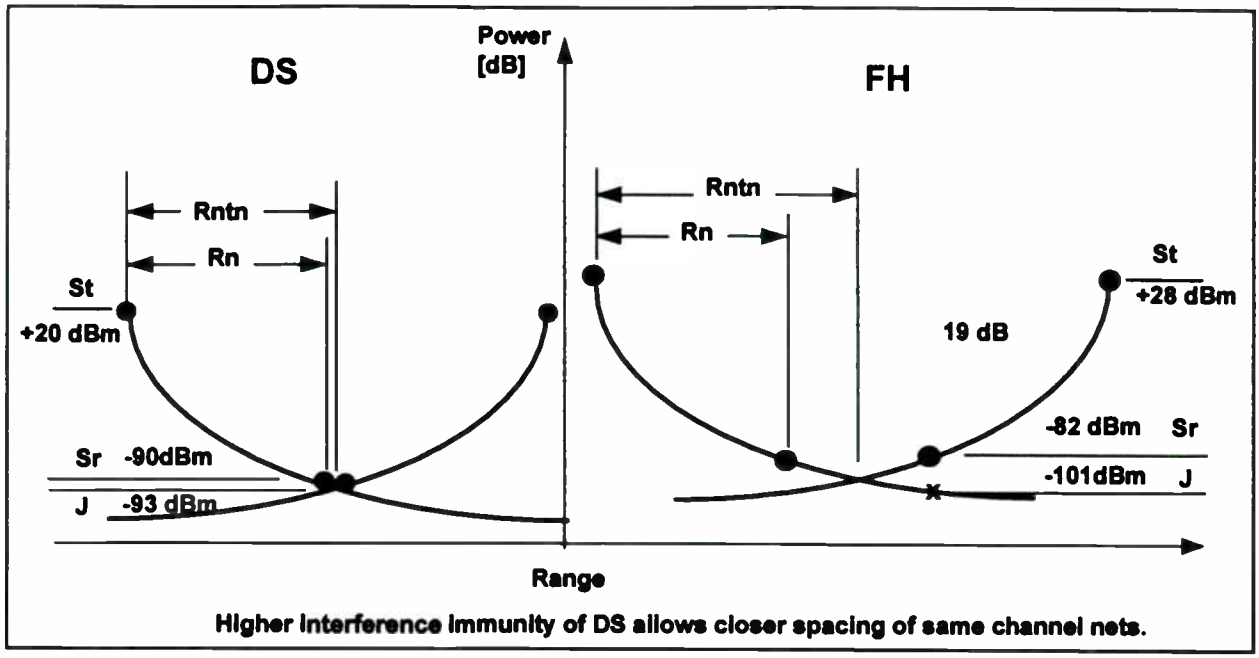


Fig. 4 Ranges of DS and FH

would use the largest modulation index that will still allow the unit to pass the FCC bandwidth requirement.

7. Ability to expand to higher data rates

The DS signal can achieve higher data rates by increasing the modulation complexity or increasing the clock rates. Each increase in the data rate will, however, require a corresponding increase in the transmit power or a cut in range. FH has few options for data rate increases. 8-FSK, with an extremely small deviation, is not feasible (Eb/N0 $\simeq$ 36 dB). FH would need a wider bandwidth allocation to achieve any higher data rate, but the wider bandwidth would cut the number of channels to hop in. This would in turn cause more collisions unless the number of collocated nets was reduced. This is a non linear problem, so the number of nets that could be collocated would reduce to about 3 if the number of hopping channels were reduced to 20.

8. Transmit power

DS, being more power-efficient should require less transmit power. This is tempered, however by the need to minimize the transmitter cost by avoiding post-modulation filtering. This means you cannot fully utilize the saturated power of the power amplifier. To keep the spectrum shape, the DS designer must cut back the power from the amplifier by 3 to 6 dB. Since the basic DS waveform is more power efficient than FH, this makes DS more efficient in PA utilization usage than FH at 1 MBps. At 2 MBps, the extremely low efficiency of the 802.11 FH system requires a significant boost in transmit power, giving a clear edge to DS. The FH signal is very constant in amplitude and can fully utilize the saturated power amplifier output, but its lower modulation power efficiency more than outweighs this advantage.

Under IEEE 802.11, the DS signal is spread over 22 MHz, lowering its spectral density. This allows it to use higher transmit power without interfering with other users of the band. The drawback is that it can interfere with more users over the wider bandwidth. If power spectral density is the constraining issue, DS clearly has the edge over FH.

9. Multiple Signal Operation

As noted in section 3, an 802.11-conforming DS network cannot employ CDMA because the processing gain and required Eb/N0 do not allow another signal of the same power to occupy the same channel. Thus, only 3 (4 with agressive filtering) networks can operate collocated. These can operate on separate channels (for example 1,6 and 11) at the

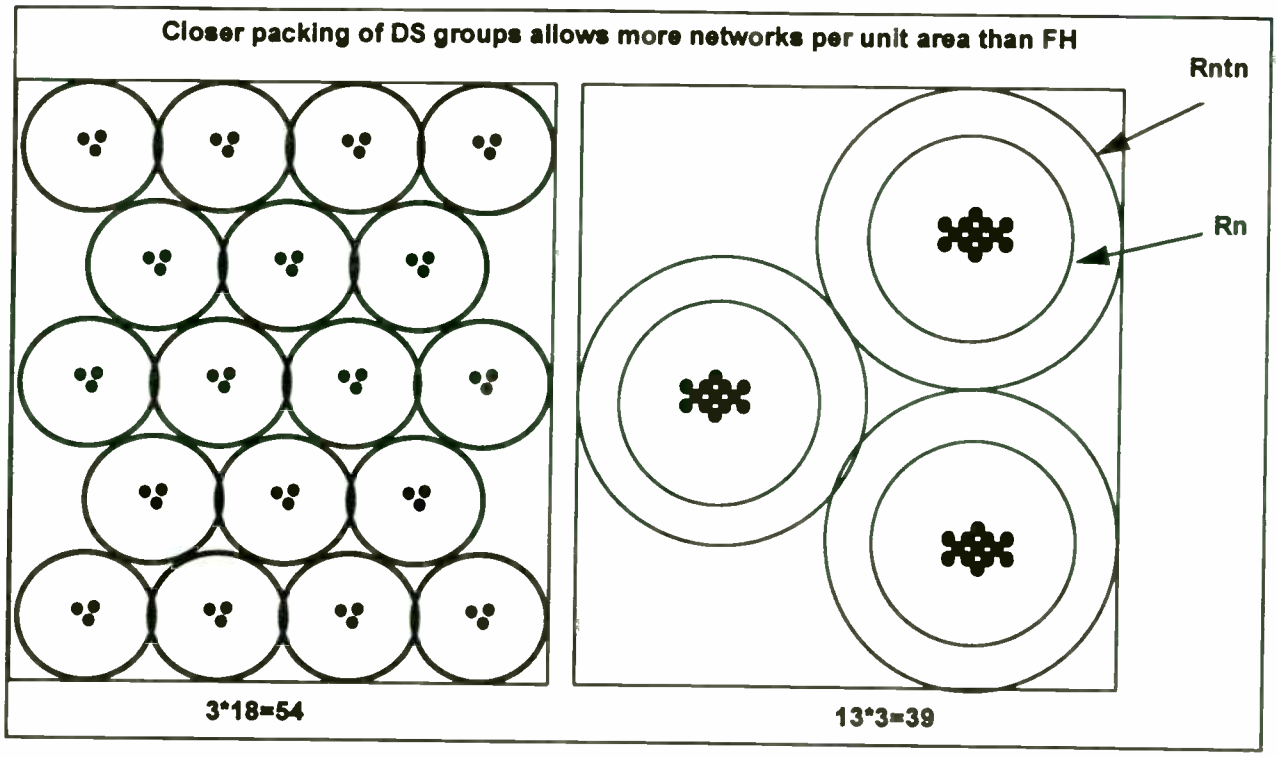


Fig. 5. Packing of Networks

same site, that is, in the same room . FH, on the other hand, allows multiple signals to be collocated as long as they are non-coordinated. Up to 15 FH nets can be collocated before the interference is too great. (This is based on the probability of collisions where two of the nets choose the same one of 79 channels at the same time.) When the probability of collisions gets too high, network throughput suffers. A recent paper by Lucent Technologies[1] showed that effective throughput peaks at about 13 nets. The aggregate throughput of these 13 collocated FH nets is less than the aggregate throughput of the 3 collocated DS nets because they are interfering with each other and only operate at 1 MBps.

DS nets on the same channel can be placed much closer together, since the signaling is more robust, *allowing more total networks and therefore more capacity in a given area.* Section 3 showed that an FH system for 802.11 needs 7.6 dB more transmit power to achieve the same range and has an 18 dB disadvantage in interference rejection. *Thus the FH nets have to be placed 25.6 dB further apart. So, when combined with the FH advantage of 5:1 (7 dB) in channels collocated, this translates to 18.6 dB fewer nets in a given area. How this dB number relates to the number of nets is dependent on the propagation conditions.*

In a real world application, for example, an FH system can support a higher density of nets (access points) in a single room—up to 13, while DS allows only three to four. However, the next group of nets in an FH system has to be much further away (the signal has to be 19 dB down!) or both groups suffer loss of throughput. DS groups of 3 can be much closer together, allowing more total nets and more total throughput per hectare.

Now, a sensible designer wouldn't necessarily place the nets in such an arrangement, but the fact remains, if two nets are using the same channel or hop set, they must be placed much farther apart in FH than in DS because the zone of interference is much larger.

Fig. 5 shows how the nets can be packed and defines the net range and . the net to net spacing diagramatically. For DS, the network range is dictated by 110 dB of path loss which is the ratio of the +20 dBm transmitted signal to the -90 dBm level of the minimum receive signal. Various studies of indoor range losses put the average propagation loss at range cubed. It is well known that the loss exponent is a function of range, but this would complicate the message here. The range to the next net (net to net spacing) is dictated by the maximum

interference signal, which has been stated to be -3.2 dB relative to the desired signal in DS. Thus, the net to net spacing is slightly larger than the net range.

For FH, the required transmit power to reach the same range is 8 dB higher, since the receiver is that much less sensitive. The net to net spacing is also larger since the interfering signal must be reduced to -19 dB relative to the desired signal. This is due to the combined effects of the higher Eb/N0 and not having processing gain. In dB terms, the FH net to net spacing is 25.6 dB greater than DS.

10. Synchronization and timing.

DS is self-synchronizing, since it employs a very short code that can be searched with a time-invariant matched filter. Thus, a DS radio, while roaming, can rapidly change to another channel and join another net, assuming that it knows the frequency to tune to. If not, it must scan all frequencies and stay on each until a signal is transmitted on that channel. The FH system search procedure allows the mobile station to sit on any one frequency and wait for a signal or beacon. If this is a bad frequency for this net, it may have to move to another and sit and wait. This is because the FH system has many channels to search and it is not feasible to perform the search in parallel. If the station scans for energy, it may or may not improve its chances since any one channel might not have energy while it is looking. Once a station hears a beacon, it gets the network timing and the hop set or next hop frequency. Under FCC rules , FH has been denied a calling channel and a global timing reference, severely constraining its ability to achieve rapid roaming synchronization. Thus, roaming with FH will require a longer time to achieve net switching.

In time bounded services, latency must be minimized. Various studies have shown that 30 ms is the most that can be tolerated with voice traffic. In an FH net, if the channel is jammed, the next available retransmission time on a clear channel may be 400 ms away. In addition, the rules state that if a packet can't be completed within the current hop, it should be held until the next hop. No such timing constraints exist for DS, but if it is jammed, it is jammed until the jammer goes away.

11. Implementation issue.

There is no clear-cut inherent advantage in hardware cost between the two modulation schemes. FH requires a fast tuning frequency synthesizer, DS does not. DS requires higher logic speeds and more complex processing, but this is not the strong cost driver it once was.

12. Capacity issues

The network protocols for DS and FH are slightly different to accommodate the peculiarities of each physical layer. In particular the interframe spacing and Slot Times are different, and recommended packet sizes are smaller for FH (400 bytes vs 1000). The net effect is a slight edge for DS in overall throughput. Since the FH nets will most likely operate at 1 MBps and the DS nets at 2 MBps, there will be a power savings with DS from the shorter duration of the packets and the lower overhead.

13. Summary

When it comes to the relative merits of (DS) versus frequency hop (FH) spread spectrum modulation schemes, the answer is: *it depends*. The choices depend on the particular implementation scenario.

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[i] A. Kamerman, "Spread Spectrum Techniques Drive WLAN Performance.", *Microwaves & RF* September, 1996, ppz. 109-114

An Impartial Comparison of DSSS and FHSS Under Narrowband Interference for ISM Band Operation*

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Abstract: **Direct sequence spread spectrum (DSSS) and frequency hopping spread spectrum (FHSS) have different physical mechanisms for rejecting narrowband interference. Because of these physical differences, their performance under varying levels of narrowband interference is not identical. This paper presents the physical mechanisms by which each spread spectrum method rejects narrowband interferers, as this is an important case for successful operation in the ISM bands. Comparisons between the two methods are drawn highlighting the conditions under which they perform identically, and also when one method performs better than the other. The proper choice of direct sequence or frequency hopping as a spread spectrum technique is shown to depend on the actual environment that the system will be deployed into.**

I. Introduction

Spread spectrum communications has enjoyed a surge of interest since the Federal Communications Commission (FCC) allowed its type-approved and unlicensed use under Part-15 Regulations in the late 1980s [1]. This FCC allocation is as a shared and lower tier occupant in the Industrial, Scientific, and Medical (ISM) bands around 915, 2442, and 5750 MHz. An important aspect of this allocation is the word *shared*. There are other users, and therefore other signals, present in these ISM bands. Successful spread spectrum products must tolerate their presence. Indeed, the FCC has set this situation up intentionally in order to foster the commercial development of spread spectrum technology.

By definition, a spread spectrum system uses a process other than the information signal to expand, or spread, the bandwidth of the signal [2, 3, 4]. There are two fundamental techniques for spectrum spreading: direct sequence and frequency hopping. These both achieve the desired spectrum spreading, but that is about all they have in common.

Direct sequence spectrum spreading combines the information signal with a spreading signal having much wider bandwidth. The net modulation signal effectively has the wide bandwidth of the spreading signal. This wide modulation is then applied to a fixed frequency carrier signal for transmission. The spreading code *directly* spreads the information, ahead and independent of the RF modulator. The principle of direct sequence spread spectrum generation, and despreading in the receiver, is shown in Fig.1.

Frequency hopping takes the exact opposite approach. Rather than spreading the modulation about a fixed carrier, the information is left unchanged and modulates a varying carrier frequency. The principle of frequency hopping spread spectrum generation is shown in Fig.2.

* This paper is extracted from and based on E. McCune's doctoral thesis at the University of California, Davis, ECE Department and is fully copyrighted material property of E. McCune. The Authors reserve the right to publish E. McCune's thesis elsewhere [8]

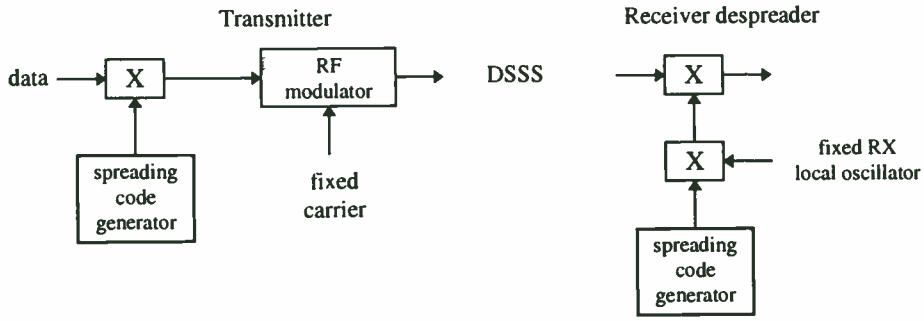


Figure 1. Principle of Direct Sequence Spread Spectrum

In frequency hopping the spreading signal is used to change the frequency of the carrier provided by the carrier generator. The data directly modulates this hopping carrier. In essence, the frequency hopping approach is just a particular collection of conventional narrowband signals.

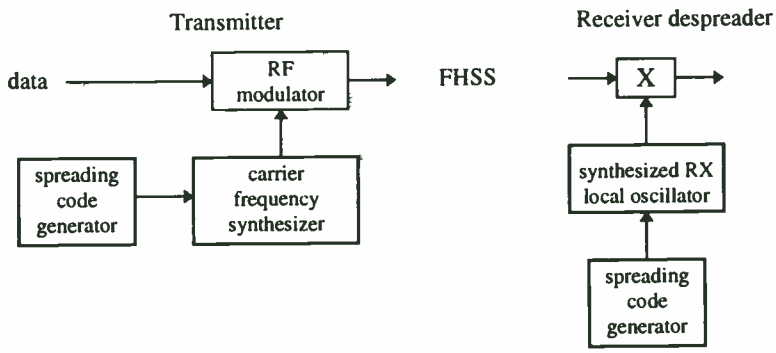


Figure 2. Principle of Frequency Hopping Spread Spectrum

This paper describes the performance of these two spread spectrum techniques in the presence of narrowband interference. Since the methods of generating the spread spectrum signals differ significantly, their methods of suppressing narrowband interference are shown to also differ. Measurements of DSSS and FHSS operation in the 915 MHz ISM band are presented under likely implementation parameters. Interference to the intended communication is determined to occur only when the following three criteria are ALL met:

1- An interfering signal exists at the demodulation frequency, AND
2- This interfering signal exists at the time demodulation is attempted, AND
3- The interference is strong enough to corrupt the demodulation

Issues of circuitry and implementation technology are left to other texts.

II. Physics of DS Interference Rejection

A key to the interference rejection of DSSS is the cyclic cancellation of the spreading code under consecutive digital multiplications, implemented by the exclusive-OR gate. These are fancy words that mean that a second spreading operation with the same code cancels the spreading on an input DSSS signal. The spreading process itself is independent of the data, so by cancelling the spreading the data is left intact. Fig. 3 demonstrates this process. In a real DSSS system, only the first two stages are actually used. The first stage is in the transmitter, and the second is in the receiver.

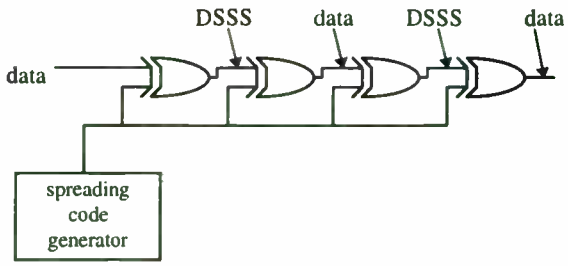


Fig. 3. Cyclic cancellation of Direct Sequence spreading codes

An interfering signal appears in the channel between the transmitter and receiver. In the receiver, the multiplier with the spreading code is the second multpily the DSSS signal encounters, but it is the first multiply with the spreading code that the interference 'sees'. The data is recovered as it follows the second stage. The interference behaves as if it was at the transmitter: it becomes a direct sequence spread spectrum signal. Thus, the interference becomes spread as the data is despread. One possible interpretation of this process is that the spreading process 'breaks' the data signal into many little pieces. The despreading process, using the same code, 'knows' where these pieces are and collects them back together. In this reassembly process, any other signal does not fit and so is broken up into pieces of its own.

Filtering the now narrowband data signal rejects much of the power in the spread interference signal. Only a portion of the interfering signal power remains in the bandwidth of the data signal, and this portion appears as a noise floor in the passband. As long as there remains sufficient signal to noise ratio in the receiver to successfully demodulate the despread data signal, the DSSS system completely rejects the narrowband interferer. This continues as long as the above qualifier is met: sufficient despread signal to noise ratio at the detector.

The despreading process is linear, so that any increases in interference power correspond to equivalent increases in the despread noise floor. It is clear that at some point the noise could be sufficiently raised such that the detector begins to make mistakes. As long as the filtered spread interferer behaves like noise, which actually is a fair to good approximation, then conventional noise performance theory can be applied to the detector's performance. This leads to the well published concept of the Jamming Margin [2, 3, 4]. As long as the interferer power is within the jamming margin, then the direct sequence processing will completely reject it. At higher interference powers the despread noise floor due to the interferer(s) exceeds the detectors ability to make error free decisions. The DSSS system quickly folds as the interference exceeds the jamming margin.

To evaluate a particular case, take a DSSS system using BPSK modulation and spreading with a 127 bit maximal length sequence. For more realism, assume further that the packet or frame being sent is 1000 bits (125 bytes) long and protected by a CRC (cyclic redundancy code) parity field. If any errors are encountered in reception of the frame/packet, then the CRC should detect it and cause it to be discarded. What is desired is the frame/packet throughput rate in the presence of a narrowband interferer near to the DSSS carrier frequency. As Fig. 4 shows, the throughput remains constant and total up to the jamming margin. As the noise floor of the despread desired signal is raised by the spread interferer, more errors are made until the packet/frame error rate nears unity. At this point the throughput, defined as the ratio of the system bit rate out to the system input bit rate, is essentially zero.

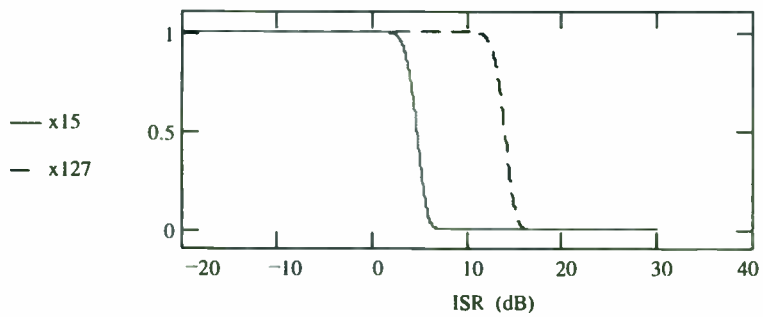


Figure 4. DSSS normalized packet/frame throughput vs. interference to signal ratio

III. Physics of FH Interference Rejection

If the operation of direct sequence is viewed as interference suppression, then frequency hopping can be viewed as performing interference avoidance [4]. The frequency hopping receiver has bandwidth matched to the data modulation, and follows the transmitter as it jumps around the band. If one of those jumps encounters a narrowband interferer, then the communication on that channel can be jammed if all three interference conditions described earlier are met. On the next jump the narrowband interferer will be moved away from (avoided). This allows the receiver's selectivity filters to reject the narrowband interferer. The amount of interference rejection is therefore limited by the performance of the receiver selectivity filters.

Channels can, in principle, be overlapped, adjacent, or spaced. For operation in the ISM bands overlapped channels are not allowed. The total spread if the FH signal must be at least the channel size times the number of hops. This sets the avoidance range of the FH system, in that the FH signal has that much room to move away from a narrowband interferer within that range.

Examine now what happens when the interferer is in the current channel. During a hop, the FH system operates as a conventional narrowband single channel signal. The modulation chosen, along with the demodulation method used, will set the interference to signal ratio (ISR) that the radio can tolerate. Unfortunately detailed information on ISR performance is not well documented in the reference literature for general modulations. For purposes of discussion, assume that for binary frequency shift keyed (BFSK) modulation that is demodulated with a limiter-discriminator the tolerable ISR is -10dB. Thus, if the interference is 10dB below the desired signal power or higher, the interference 'wins' and communication on that channel ceases. Communication on the remaining N-1 channels still continues.

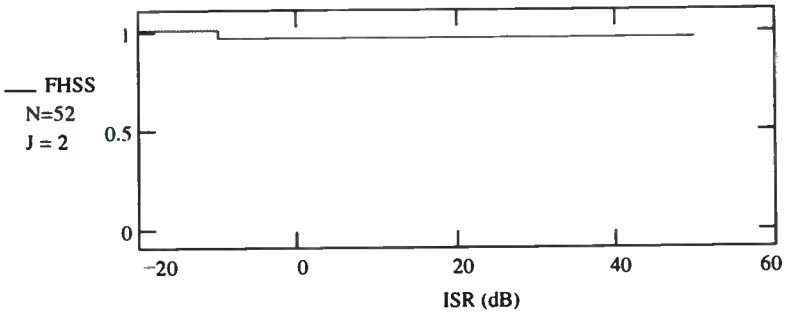


Figure 5. FHSS normalized packet/frame throughput vs. interference to signal ratio

The net throughput of the FHSS system is shown in Fig. 5. Interference in one channel has no effect as long as it is below the ISR limit of the demodulator, -10dB in this case. Above this limit, the interference controls the demodulator on that channel and the desired communication is lost. On the remaining channels the interference is not present, and communication proceeds normally. The throughput falls to (N-J)/N, where J is the number of jammed channels out of the N available.

IV. Evaluated System Definitions

To put quantitative numbers on these cases, the following system definitions have been made:

DSSS evaluation

There are two system configurations used for the direct sequence spread spectrum evaluation. Both systems use binary phase shift keying (BPSK) for their modulation. The first is near the minimum accepted by the FCC for Part 15.247 applications, and uses 15 chips per input bit. This design has a maximum process gain of 10log(15) = 11.8 dB. For an input bit rate of 50 kbps, this results in a mainlobe bandwidth of 1.5 MHz.

The second DSSS system evaluated changes only the spreading. Instead of using 15 chips per input bit, this system uses 127. The maximum process gain is now 10log(127) = 21 dB. Since the input data rate is not changed, the bandwidth of the main lobe is increased to 12 MHz. Fig. 6 shows an overlay of these two DSSS signals, where both signals have the same output power.

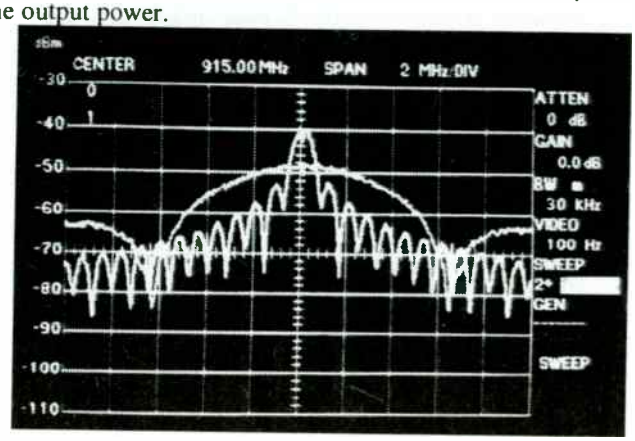


Fig 6. Direct sequence spreading comparisons: x15 and x127.

Notice that the occupied bandwidth of either DSSS signal of Fig. 6 is not absolute. Much of the signal energy is in the main lobe of the spectrum, but there is energy also in many sidelobes. Measurements of the total DSSS bandwidth at -20 dBc, -40 dBc, and -60 dBc, all give very different values. This feature of DSSS signals is defined as 'soft-bounded spreading.' This characteristic becomes important in some of the later measurements.

FHSS evaluation:

Only one system configuration is used for the frequency hopping evaluation. As in the direct sequence evaluation, the bit rate is set to 50 kbps. Channel spacing is set at 76 kHz, which is a convenient value for the frequency synthesizer used in the test. This sets the channel bandwidth efficiency to 50/76 = 0.66 bits/sec/Hz. This value is compatible with binary frequency shift keying, the conventional modulation type for FHSS systems. Using 52 channels for the hopper, which is just over the minimum of 50 required by the FCC for operation in the 902 MHz ISM band under part15.247, this provides a total spreading bandwidth of 3.9 MHz. This spread is placed between 912 and 916 Mhz, as shown in Fig. 7.

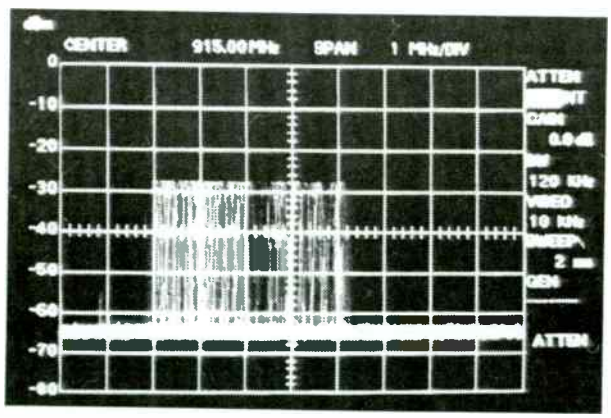
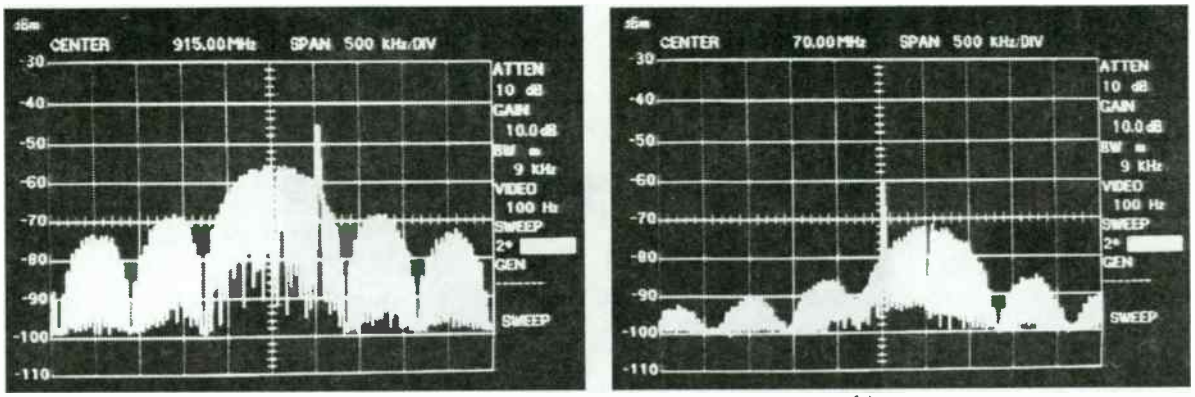


Fig. 7. Frequency Hopping spreading process, as used in the evaluations

Unlike the DSSS systems, the spread bandwidth of the FHSS signal in Fig. 7 is well bounded. Measurements of the total FHSS bandwidth at -20 dBc, -40 dBc, and -60 dBc, all give essentially the same value. This behavior is defined as 'hard-bounded spreading.'

V. DS Narrowband Interference Rejection Performance

The basic operation of the interference rejection mechinism is illustrated in Fig. 8. The first photograph shows the channel, with the x15 DSSS signal at 915 MHz and an interfering CW tone at 915.5 MHz. From the earlier discussion, after the receiver's despreading operation the DSSS signal should return to its original, unspread form. At the same time, the interference should become spread. This is indeed what happens, as shown in the second photograph. The original DSSS signal is now a single spike at the 70 MHz intermediate frequency (IF). Centered 500 kHz above the desired signal, at the converted frequency of the interference, is the spread interference.

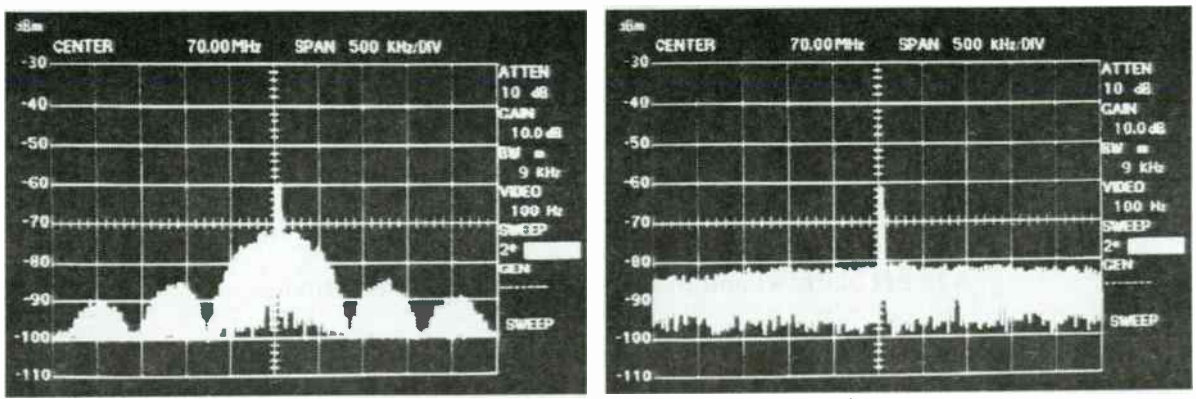


a) b)

Fig. 8. Direct sequence interference transformations: a) x15 DSSS signal with CW interferer at 915.5 Mhz; b) despread IF signal showing compressed DSSS signal and spread interference

To actually achieve rejection of the interference, the desired signal is now passed through a bandpass filter. Since most of the interference energy is now outside the filter designed to pass only the despread signal, this energy is blocked from continuing into the receiver. As long as there is a significant amount of spreading, then there will be an equally significant amount of interference power rejection from the receiver. This is clearly shown in Fig. 9, where signals after despreading in the receiver are presented. For these measurements the equal power interference was moved to be right on the carrier frequency. This is the condition used in the mathematical models predicting process gain and jamming margin.

The first photograph (Fig. 9a) shows the behavior of the x15 DSSS system. There is approximately 12 dB from the top of the despread signal to the peak of the spread interferer. It is no accident that this distance essentially matches the process gain for this configuration. The second photograph (Fig. 9b) shows the same measurement except that now the wider spread factor of x127 is used. The distance to the peak of the spread interference is now 20 dB. Wider spreading improves the rejection of interference, as expected.

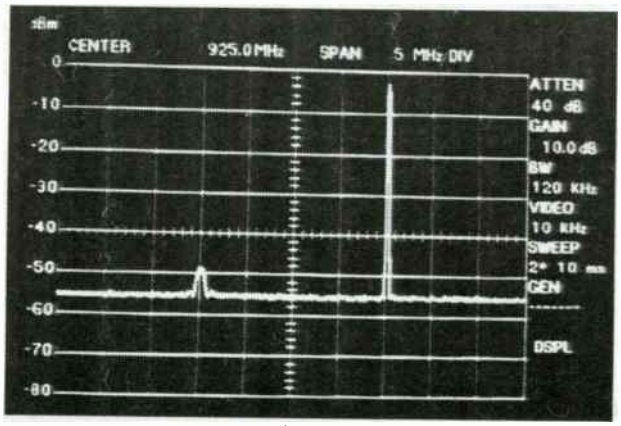


a) b)

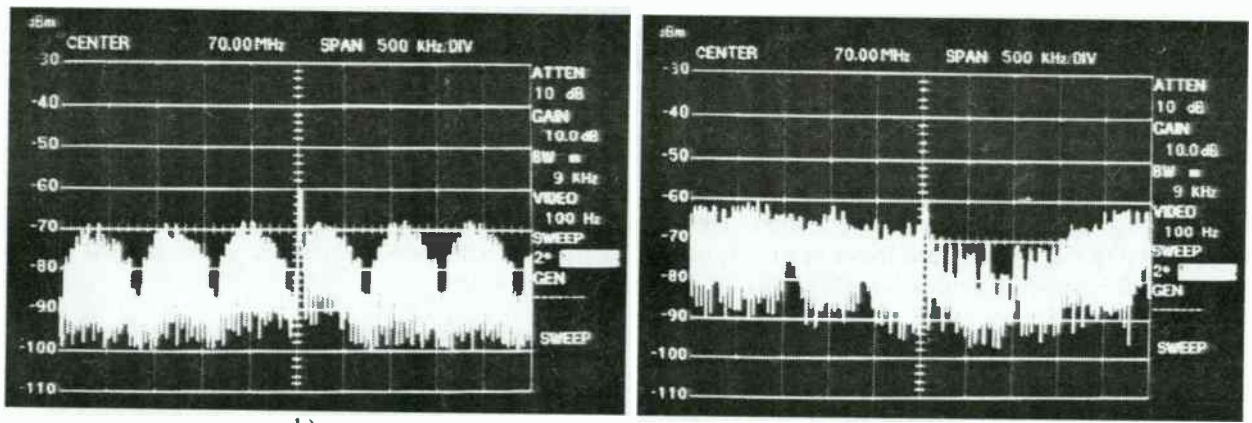
Fig. 9. Direct sequence process gain effects at the receiver, with equal power CW interferers on the carrier frerquency: a) x15 DSSS; b) x127 DSSS

The 902 MHz ISM band has large pager transmitter signals just above it, around 935 MHz. It is important to check the behavior of the DSSS systems in the presence of such large, out of band signals. These measurements are shown in Fig. 10. Fig. 10a is the test setup, showing the DSSS signal at 915 MHz, which for this photograph is the x15 version, and the interferer at 935 MHz with an amplitude that is 40 dB greater than the DSSS signal.

Fig. 10b shows the receiver after despreading this channel signal arrangement. Notice that there is spreading energy from the interferer present in the signal passband. The receiver filters will still reject the interference power, but now there is much more interference power to reject. In the photograph of Fig. 10c the DSSS system behavior is more striking. There is actually more interference from the out of band interferer with the wider (x127) spreading in use! The very feature that improved the in-band interference rejection is exacerbating the out of band interference rejection. This is a direct result of the 'soft bounded spreading' discussed above. Since the spreading factor is nearly eight times wider, the rolloff of the spreading sidebands is eight times slower.



a)



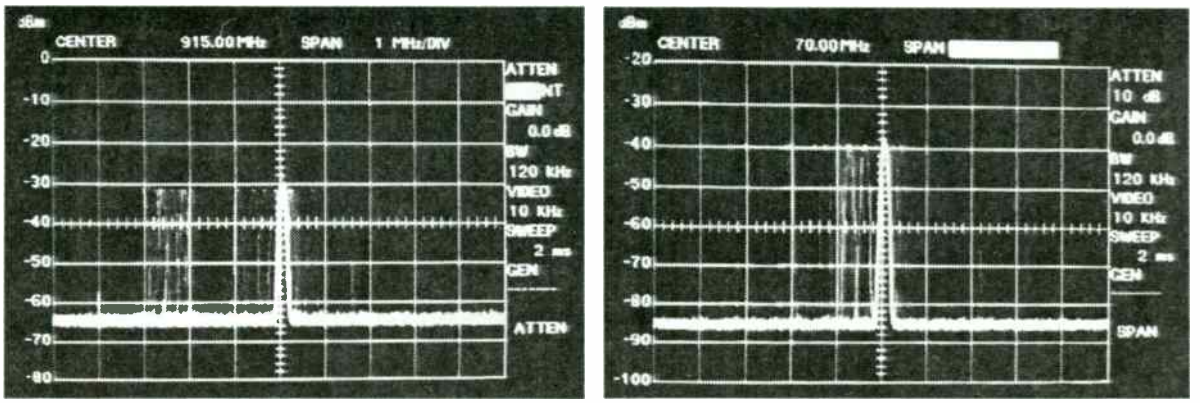
b) c)

Fig. 10. Direct sequence out of band interferer performance measurements: a) interferer at +20 MHz and +40 dB from the DSSS signal; b) x15 DSSS after receiver despreading; c) x127 DSSS after receiver despreading.

VI. FH Narrowband Interference Rejection Performance

Like direct sequence spread spectrum, frequency hopping achieves its interference tolerance by spreading the interfering signal over a wide frequency range at the same time as it collects and despreads the desired signal. However, the physical process is quite different. Fig. 11 illustrates the FH process. In Fig. 11a the FH signal covering 912-916 MHz is shown with an equal power interferer at 915 MHz. Compare this with Fig. 8a, where the same conditions are applied to a DSSS signal. Two major differences are noted: 1) the FH system applies all of its

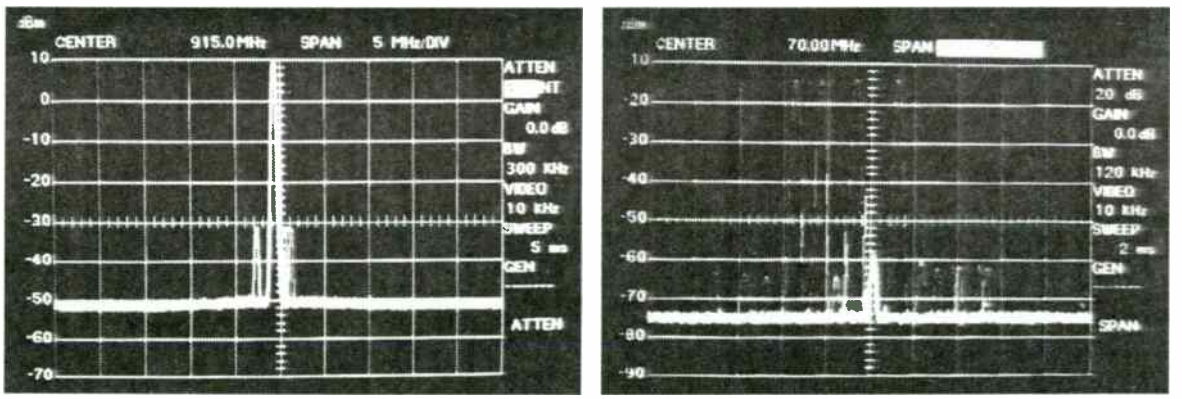
output power at whatever frequency it is operating at during a hop, unlike the DS system which uses all frequencies simultaneously, and 2) the soft-bounded nature of the DS spread compared to the hard-bounded nature of the FH spread.



a) b)

Fig. 11. Frequency hopping interference transformations:
a) FHSS signal with equal power CW interferer at 915 MHz;
b) despread IF signal showing compressed FHSS signal and spread interference

Fig. 11b shows the signals in the FH receiver following the despread operation. The desired FH signal is now compressed into a single tone at the 70 MHz IF, and the interference is spread. Like the DS system, the use of a narrowband bandpass filter to select the despread FH signal will cause the rejection of most of the interference power. Unlike the DS system, when the interfering signal overlays the desired signal it is not a noise signal, but a real jamming signal. For that particular hop communication is likely to be impossible. This characteristic is expanded on in Fig. 12. The interfering power is increased by 40 dB. Fig. 12a shows the channel with the large interferer. In Fig. 12b the signals following the FH despreader are shown. The interferer is now spread. Notice that if the narrowband bandpass filter has sufficient selectivity, this large interferer will be rejected when it is shifted outside the filter. Communication is jammed completely when the frequencies align.

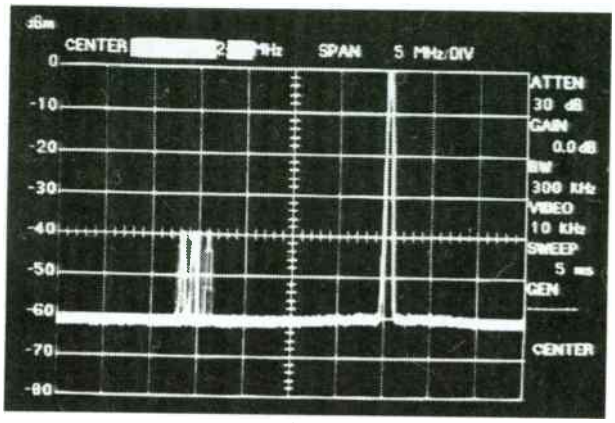


a) b)

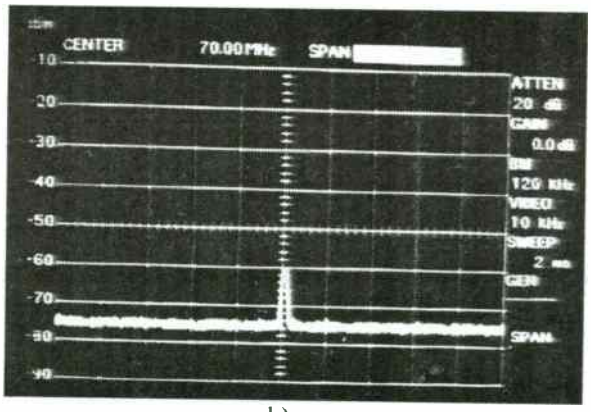
Fig. 12. Frequency hopper large in-band interferer performance: a) +40dB CW interferer at 914 Mhz; b) despread IF signal showing compressed FHSS signal and spread interference

Evaluation of the FHSS system performance in the presence of a large out of band interferer is the last comparison measurement. The results are presented in Fig. 13. The first photograph shows the channel configuration, which is using the same conditions as those used in the DSSS evaluation: the large out of band interferer is 20 MHz above the spread signal, with +40 dB more signal power. The despread signal is shown in Fig. 13b. This shows only the despread FHSS signal, with no effect from the interferer. The wider band measurement of Fig. 13c shows the entire story. The spread interferer is present, but all of its energy is removed in frequency by 20

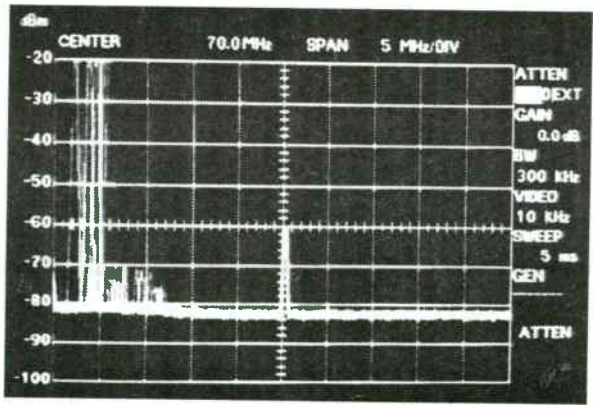
MHz. Filter selectivity can be used to completely reject this interference. This is a direct consequence of the hard-bounded nature of the frequency hopped spreading process.



a)



b)



c)

Fig. 13. Frequency hopping out of band interference performance: a) interferer at +20 MHz and +40 dB from the FHSS signal; b) FHSS after receiver despreading; c) wider band measurement of the FHSS following despreading.

VII. Comparison Discussion

These measurements show that the differing physical processes used in direct sequence and frequency hopping do perform differently in the presence of narrowband interference. In fact, these two spread spectrum approaches can be considered duals, in a way. If the interferer is within the spreading band, then the DSSS system can tolerate and completely reject it while the FHSS system can be completely jammed on that channel. For a large out of band interferer, the opposite is true. The DSSS process is sensitive to such interferers, where the FHSS system is not.

For the DSSS system, this sensitivity to large out of band interferers is a direct consequence of the switched mixer method of generating BPSK. Remember that this modulation method is used twice, once in the transmitter, and once in the receiver for the despreader (Fig. 1). The problem is in the receiver despreader, where the spreading of the interference takes place. There are two ways to address this problem. First is to use a roofing bandpass filter to eliminate out of band signals. This works, but since it is not inherently required by the FHSS system (Fig. 13) then this puts a DSSS system at a complexity disadvantage. The other method is to examine the real source of the problem, the receiver despreader, and to address that directly.

Using a different type of modulation, where the signal envlope is constrained (ideally to a constant) while generating the BPSK has been shown to significantly reduce the distant sidelobes [5,6,7]. This modulation method is called FBPSK. An example of a closely related signal, FQPSK, is shown in Fig. 14. This measurement was made through a completely saturated amplifier, so it accurately depicts the performance of this signal when used to drive the LO port of the despreading mixer. Note that the sidelobes are essentially gone, which is a tremendous improvement over the signal of Fig. 6. The DSSS signal of Fig. 14 exhibits far less of a soft-bounded spread than the ones in Fig. 6. With less signal energy at a far distance from the carrier, there is far less sensitivity to out of band interferers. Use of this kind of spreading modulation eliminates this disadvantage from DSSS systems compared to the FHSS performance.

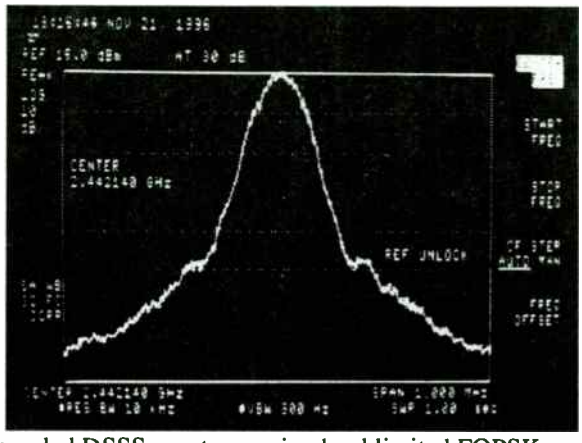


Fig. 14. Bounded DSSS spectrum using hard limited FQPSK modulation [9]

The remaining points of comparison relate to Figures 4 and 5. Considering the system Frame Error Probability (FEP) in the presence of a narrowband interferer, Fig. 4 shows that the direct sequence system initially completely rejects its presence. For signals lower than the jamming margin, the DSSS system throughput is unity, which means that every packet sent can be accurately received. When the jamming margin is reached, within 5 dB of additional interference power the throughput of the DSSS system has gone to zero. The noise from the spread interferer in the receiver is now large enough to completely dominate the detector. As the interference level continues to grow, so does the noise following the despreader, and the throughput remains at zero.

The frequency hopper shows a degradation in performance at a significantly lower level of interfering signal power. Once the interference is large enough to disturb the detector on that channel, communication through that channel is lost. Any packets sent on that channel must be resent on a different channel. A major difference here is that once that channel is lost due to the narrowband interference, then it remains lost. This remains true irrespective of the level of the interfering signal power, to first order. At very large interference levels other effects such as ultimate filter rejection levels and front end compression come into effect, but that is beyond the scope of this paper. Fig. 15 presents an overlay of the DSSS and FHSS performances.

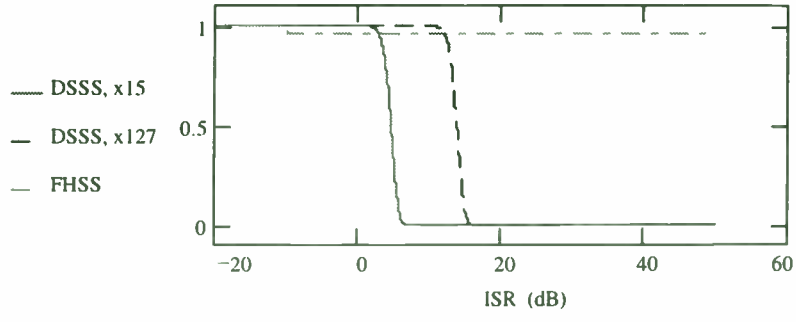


Fig 15. Comparison of DSSS and FHSS throughput vs. Interference to signal ratio (ISR)

VIII. Conclusion

The proper choice of direct sequence or frequency hopping as a spread spectrum technique depends on the actual environment that the system will be deployed into. If there are narrowband interferers of moderate level, then a DSSS system may be designable that will completely reject them. Should there be any large interfering signals, then FHSS is more likely to continue operating, even though the interference is not completely rejected.

References

[1] FCC, Code of Federal Regulations CFR 47, Part 15, section .247

[2] R. C. Dixon, *Spread spectrum Systems with Commercial Applications*, 3ed, John Wiley & Sons, New York, 1994

[3] M. K. Simon, J. K. Omura, R. A. Scholtz, B. K. Levitt, *Spread Spectrum Communications Handbook*, McGraw-Hill, New York, 1994

[4] H. Taub, D. L. Schilling, *Principles of Communication Systems*, 2ed, McGraw-Hill, New York, 1986

[5] K. Feher, *Wireless Digital Communications*, Prentice Hall, New Jersey, 1995

[6] H. Mehdi, "FBPSK and FQPSK, Power and Spectrally Efficient Modulations for Wireless Communications," Ph.D. Dissertation, University of California, Davis, Dec. 1995

[7] K. Feher, H. Mehdi, "Modulation/Microwave Integrated Digital Wireless Developments," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 43, No. 7, July 1995, pp. 1715-32

[8] E. McCune, "Constant Envelope Modulations with Extremely Low Sidelobe Energy," Ph.D. Dissertation topic, University of California, Davis, Davis, CA 95616, Dec. 1997

[9] K. Feher, et. al., US Patents 4,339,724, 4,567,602, 4,644,565, and 5,491,457

Short PN Sequences for

Direct Sequence Spread Spectrum Radios

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Abstract

Traditional military spread spectrum systems use Direct Sequence Spread Spectrum (DSSS) for its jam resistance and low probability of intercept. Additionally, the transmission security afforded by long PN sequences in the waveform is important as is the ability to do code division multiple access (CDMA). DSSS systems as proposed for the unlicensed ISM band use a form of DS that has few of these attributes. The sequences used are so short that special attention must be placed on what are the best sequences to use. The Barker sequences are often chosen, but do they have the right characteristics? A Barker word has good autocorrelation sidelobes when preceded and succeeded by all zeros. Does it have good correlation sidelobes when preceded and succeeded by more Barker words with QPSK modulation? That is, the adjoining sequences can have any of four phases relative to it and this may cause some sequences that initially look good to not be. This paper examines 11, 13, 15, and 16 bit sequences for these properties and makes sequence recommendations.

1. Introduction

The Prism™ baseband processor (HFA3824) is a direct sequence spread spectrum modem that is set up to handle spreading ratios of 11, 13, 15, and 16 chips per bit. These give processing gains of 10.4 to 12 dB theoretically. This paper discusses the properties of suitable chipping sequences.

The IEEE 802.11 committee developing the standards for wireless LANs in the 2.4 GHz band has chosen the 11 bit Barker sequence for their DS spreading function. This sequence is well known in the industry as having 'optimal' autocorrelation properties. It produces a single peak and uniformly low sidelobes when correlated against time shifted versions of itself. These can be created by multipath echoes. Thus, it has very good rejection of multipath. The committee could have chosen the 13 bit Barker word for a little more processing gain, but didn't want to use any more bandwidth than necessary. Other users with non 802.11 schemes in mind will want to explore the options.

The autocorrelation properties of Barker words are often measured with all zero data to either side of the sequence being correlated for. The DS spreading of 802.11 places identical words to either side with 0, 90 or 180 degree relative phase rotations. Thus the correlation properties being sought are those of good autocorrelation with adjoining words of the same sequence at phase rotations of $k*90^{\circ}$ (k=0 to 3). The multipath performance of the receiver is also optimized by having a single sharp peak in the correlation with low sidelobes.

The Barker words are only defined to 13 bits, but maximal length sequences exist for all lengths of 2^n-1. This paper defines at least one 15 bit sequence which should have good properties. When checked in the real application, the maximal length sequence was found lacking and another sequence showed better performance.

2. Correlation Properties

The photographs that follow show some trial sequences and their correlation properties in the Prism™ evaluation circuits. The HFA3824

has a test port to monitor the correlator magnitude output in real time. This allows observation of the sidelobe structure of the code being used to analyze its suitability. The first code described below is the IEEE 802.11 defined code, an 11 bit Barker word. It can be defined by the HEX codeword 05B8 to the registers of the HFA3824. The 5 leading digits of this 16 bit word are ignored when the chip is programmed for 11 chips per bit operation. This makes the actual sequence:

101 1011 1000

Fig. 1 shows the correlator output of the chip with asynchronous transmit and receive chip clocks and random QPSK data. This clock offset causes the chip tracking to jitter by 0.25 chip as the optimum tracking point slides by. It is evidenced by the fuzzy nature of the correlation peak as the tracking loop continually readjusts the asynchronous sampling clock to sample close to the peak.

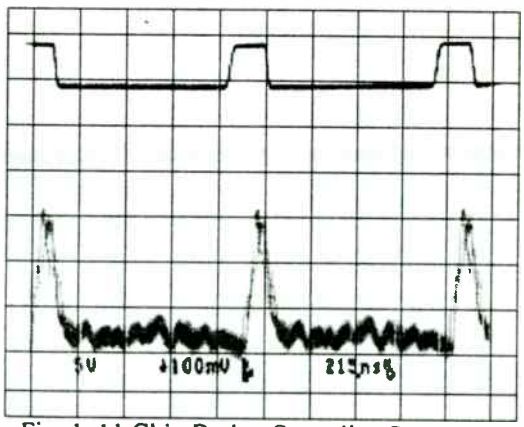

Fig. 1, 11 Chip Barker Spreading Sequence

In Fig. 1, the upper trace is the receive bit clock for reference. The oscilloscope is triggered on the bit clock. The correlation is referenced to a graticle line just above the notations. The Barker words have uniformly low autocorrelation sidelobes as shown by the uniform and low values of the correlations except at the peak. The maximum sidelobe is theoretically 1/11th of the value of the peak. This photo shows that this is true even with adjacent symbols QPSK modulated. Any cyclic shift of the Barker word is a also good sequence as is a reversed Barker word.

The 13 bit Barker sequence for 13 chip per bit spreading is considered next. The 13 bit Barker sequence is coded into the HFA3824 registers as 1F 35 in hex notation. Again, the leading digits are ignored to truncate the 16 bit number to 13 bits. The resulting bit sequence is:

1 1111 0011 0101

The 13 bit Barker word has low correlation sidelobes and is a good sequence for spreading even though it has a large unbalance of 1s and 0s (9 to 4).

Fig. 2 shows the correlation of the 13 bit sequence. It has good sidelobe properties even with the adjacent symbols QPSK modulated. The bit clock to which the oscilloscope is triggered is at the top. The baseline reference for the correlation is the graticle line just above the notations.

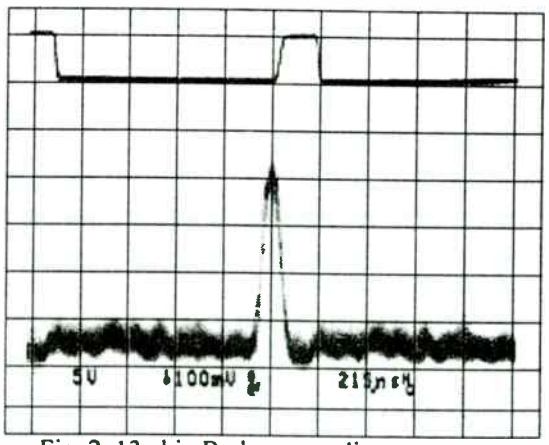

Fig. 2, 13 chip Barker spreading sequence

The maximal length sequence for 15 bits created with the generator polynomial: $x^4 + x + 1$ was considered. In hex notation it is 789A or in bits:

111 1000 1001 1010

This sequence did not have properties as good as the 13 bit Barker word as expected. It had some large sidelobes, as shown in Fig. 3. These sidelobes can cause a reduction in the performance of the radio. The performance of the demodulator is related to the ability to distinguish the peak from the rest in the presence of noise. If a large sidelobe exists, there is more likelihood that noise can raise its value higher than the real peak which will make a symbol error occur.

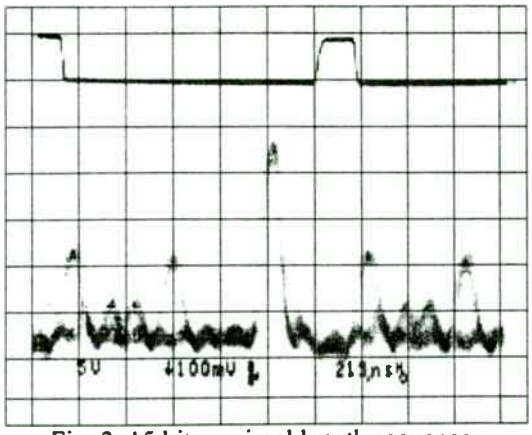

Fig. 3, 15 bit maximal length sequence

To make a good 15 bit sequence, the 13 bit Barker word with two leading 0s was tried and gave better results. Using the sequence 1F35 again, the sequence is now better balanced in 1s and 0s and also has better sidelobe properties than the maximal length sequence in this application. The sequence is:

001 1111 0011 0101

Remember that PN sequence sidelobes are not usually measured with adjacent symbols QPSK modulated like was done here. Fig. 4 shows sidelobes are low and uniform, which is the desired result

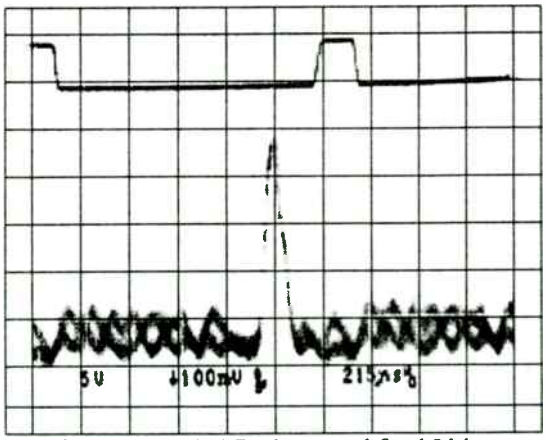

Fig. 4, Extended Barker word for 15 bit

The next set is one of several 16 bit sequences examined. The unique word used in the 802.11 specification as a start frame delimiter was tried with the results shown in Fig. 5. This 16 bit sequence is coded into the HFA3824 registers as F134 in hex notation. It has poorer correlation properties than the extended 13 bit Barker word that follows.

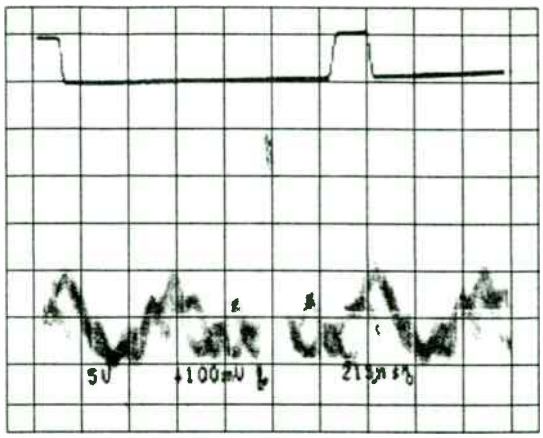

Fig. 5, 16 bit synchronization sequence

The 16 bit code made from the 13 bit Barker word (1F35) with 3 leading 0s is shown in Fig. 6.. It has a nearly balanced number of 1s and 0s and shows good correlation sidelobes. This code has uniform sidelobes with a well defined peak. The sequence is:

0001 1111 0011 0101

The properties of this code are better for 16 chip applications than any other that was tried.

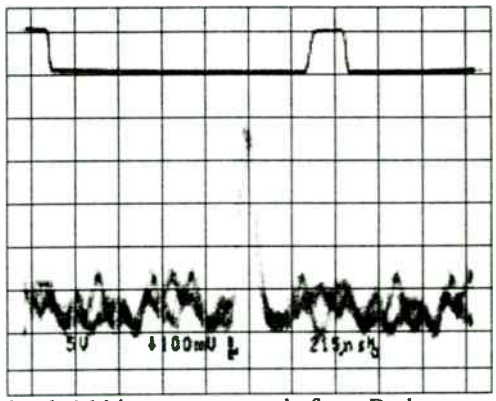

Fig. 6, 16 bit sequence made from Barker word

Shorter sequences can be programmed into the HFA3824 than 11 chips per bit using a subterfuge. Using a spreading sequence of half 1s and half 0s (00FF) makes a minimal (2 chips per symbol) spreading ratio to operate nearly unspread. This is equivalent to biphase-level data modulation in BPSK modes. The mid bit phase change provides essential tracking information to the bit timing loop. The design of the Prism™ baseband processor does not support

wholly unspread (spread sequence = FFFF or 1 chip per symbol) operation. While it will acquire and track in an unspread mode, it makes errors at high SNR (due to low tracking loop gain) which is unacceptable. Using specialized sequences such as these, at a nominal spread ratio of 16 chips per symbol, a system designer can get effective spread ratios of 8, 4, and 2 chips per symbol.

3. Processing Gain

The FCC rules for the 2.4 GHz ISM band call for a DS spread spectrum waveform with at least 10 dB processing gain. The suggested test for processing gain is for interference rejection and this allows a slightly different definition of processing gain than is sometimes used.

Many textbooks call processing gain the ratio of spread rate to bit rate. The FCC rules use spread bandwidth to modulation bandwidth which can be different. This FCC rule is based on reducing the power spectral density and providing interference immunity. For example, a modulation with BPSK spreading and QPSK data modulation is the 802.11 DS standard which calls for 11 MCps spreading and 1 MSps QPSK data modulation. An incoming signal is filtered to 22 MHz, despread, and then filtered to 2 MHz bandwidth. Thus, an 11 to 1 bandwidth reduction is effected and this provides 10.4 dB of interference rejection. Interfering CW signals are spread to 22 MHz null to null and 91% of their energy is thus outside the final bandwidth. This meets the processing gain test even though the spread rate to data rate ratio is only 5.5. Indeed, 2048 QUAM could be used for the data modulation and 91% of the jammer energy would still be rejected even with a spread rate to bit rate ratio of unity. Of course, the J/S ratio would be worse by the increase in Eb/N0 required.

The spread spectrum defined by the 802.11 standard (11 chips per symbol) will not allow much, if any, CDMA capability. The reason is that processing gain is on the order of the required Eb/N0 that the modem needs to get good bit error rates. Thus, the signal to noise ratio in the spread bandwidth is near unity in BPSK mode and positive 3 dB in QPSK. This does not allow any CDMA in QPSK and only one other equal range channel in BPSK. However, it allows DS networks to be operated at least 10 dB closer together than unspread networks all other things being equal.

4. Summary

In summary, the best spreading codes to use for the Prism™ wireless chip set have been found and are 05B8 for 11 chips per bit and 1F35 for 13, 15, and 16 chips per bit. These are the 11 and 13 bit Barker words with added zeros for the longer sequences. Cyclic shifts of these sequences and reversed sequences are also good. Cross correlations between these have not been tested thoroughly, but the radios will not lock up on reversed sequences or different lengths. Cross correlations between cyclic shifted versions will be high.

HIGH-POWER DESIGN

High-Power Design

Session Chairperson: John Salvey,
Fujitsu Microelectronics (San Jose, CA)

Characterization and Modeling of High Power RF Semiconductor Devices Under Constant and Pulsed Excitations

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Abstract - To investigate the contribution of thermal effects on device model parameters, high power bipolar junction transistors (BJTs) and lateral diffusion metal oxide field effect transistors (LDMOS) were fully characterized under constant and pulsed DC and RF conditions. All of the principal pulse parameters, pulse width, sampling location and duty cycle were investigated to ensure an isothermal extraction environment. Finally, comparisons are made between model parameters extracted under constant DC and RF versus model parameters extracted under pulsed DC and RF conditions.

I. Introduction

To properly account for self-heating effects, semiconductor nonlinear models need to dynamically account for model parameter temperature variations. Several authors [1,2] have already reported ways to implement dynamic self-heating effects into harmonic balance simulators with bipolar junction transistors and field effect transistors nonlinear models. During the model extraction procedure, the model parameters thermal and electrical dependencies need to be de-coupled, allowing extraction of isothermal model parameters and their temperature dependencies, making the model thermally consistent. One way [1] to determine the isothermal model parameters is by way of measuring the devices under pulsed DC and RF conditions. Another way. [2] is by performing all measurements under non-isothermal conditions, i.e., constant DC and RF excitations, and then thermally de-embed the data to arrive to an isothermal set of measurements.

II. Pulsed Modeling System

The high voltage BJT and LDMOS devices were characterized under constant DC, pulsed DC, constant S-parameters and pulsed S-parameters with the use of the HP 85122A E20 pulsed modeling system. The pulsed modeling system consists of the integration of a DC and a RF subsystem.

The DC subsystem allows the bias to be pulsed during RF measurements, and allows voltage and current measurements under pulsed conditions. Four HP 6629A power supplies, providing a maximum pulse and quiescent voltage range of ± 100 V, provide drive to two HP 85210A K48 pulsers. The pulsers allow voltages to be supplied with a 200 nsec. minimum pulse width and a maximum duty cycle of 4 % at the pulsed maximum current of 10 A. The pulsers also allow the user to set a quiescent bias point, then pulse to bias voltages either higher or lower than the quiescent voltage. Two dual channel HP 8110A pulse generators synchronize the pulses, set the desired pulse width and period and provide a trigger for the DC and RF sampling location. The pulsed DC measurements are accomplished using four HP 3458A digital multimeters which can be triggered to measure voltages and currents over any 2 nsec. aperture on the waveform. To measure current, there is current viewing resistor circuitry with attenuators and gain stages, built into each pulser. For constant DC measurements under 1 mA, an HP 4142 modular DC source measure unit is used, due to the 50 to 100 μA noise floor for pulsed current measurements. The pulsers include a clean low leakage path to the HP 4142 for standard constant DC measurements.

The RF subsystem consists of an HP 8510C vector network analyzer, an HP 8115A test set, an HP 85110A test set and two synthesized sources, one for the LO internal test set downconverters and the other to provide the RF stimulus to the device under test. The HP 85110A is a custom made test set that can operate in constant and pulsed modes from 500 MHz to 20 GHz, while the HP 8515A test set only operates in constant or CW mode from 45 MHz to 26.5 GHz. Bias networks are used to

couple the RF and bias to the DUT, allowing pulsed bias DC operation and pulsed RF operation from 400 MHz to 26.5 GHz. An HP 3488A switch unit allows the user to switch between test sets without any additional connections. Both the DC and the RF subsystems are under complete computer control of the IC-CAP Modeling Software.

III. Extraction Environment

For this investigation two different high voltage silicon devices were used. The first device is a sub micron BJT operating at 28 V. The device has 1915 μm^2 emitter area. The second device is an LDMOS operating at 28 V with a gate periphery of 5.04 mm. Both devices were mounted in engineering packages and all measurements we made with the use of an Inter-Continental Microwave fixture.

The first step in the investigation was to determine the minimum pulse width, sampling location and duty cycle that will guarantee an isothermal environment. Fig. 1 shows constant and pulsed DC collector current of the BJTdevice vs. collector to emitter voltage for 1.5 µsec, 5 µsec and 50 µsec pulse widths for base to emitter voltages of 0.9 V and 1.0 V. Fig. 2 shows constant and pulsed DC drain current of the LDMOS device vs. drain to source voltage for 1.5 µsec, 5 µsec, 20 µsec and 100 µsec pulse widths and gate to source voltages of 6.0 V and 10.0 V. In both cases, very little changes were noticed below pulse widths of 1.5 µsec. For both fig.1 and fig. 2 the pulse repetition period was changed for each pulse width to mantain a constant duty cycle of 0.1 %.

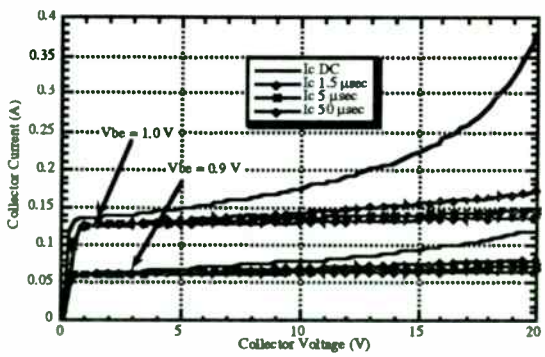

Fig. 1 Constant and pulsed DC collector current vs. collector to emitter voltage for 1.5 µsec, 5 µsec and 50 µsec pulse widths and base to emitter voltages of 0.9 V and 1.0 V of the sub-micron BJT device.

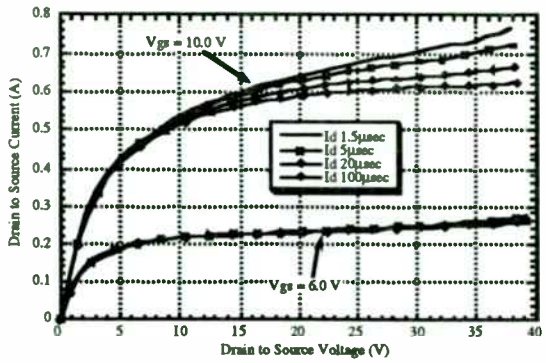

Fig. 2 Constant and pulsed DC drain current vs. drain to source voltage for 1.5 µsec, 5 µsec, 20 µsec and 100 µsec pulse widths and gate to source voltages of 6.0 V and 10.0 V of the high voltage LDMOS device.

As expected, fig. 1 clearly shows how the thermal run-away varies with the applied bias pulse width. Fig.2 shows the differences in the slope of the Ids-Vds curves under different pulse conditions. Finally, the applied duty cycled was reduced until no changes were detectable in the collector and drain current values.

During the pulsed DC and RF extractions, the gate and base bias pulses were within the drain and collector bias pulses (in depletion mode FETs the drain pulse will always be

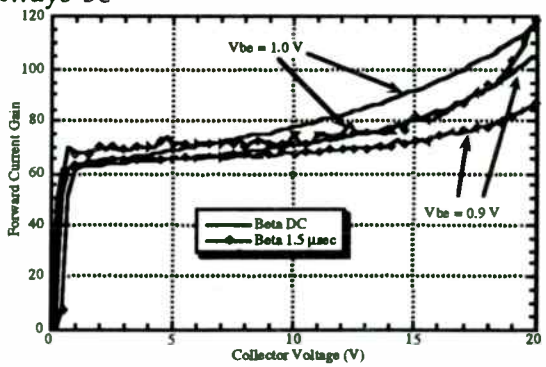

Fig. 3 Constant and pulsed DC forward current gain β_f vs. collector voltage for base to emitter voltage of 0.9 V and 1.0 V.

within the gate pulse), which will always follow the path of low current in the IV plane. The gate and drain pulse widths were 1.8 µsec and 2.0 µsec respectively, with the gate pulse delayed by 100 nsec. The RF pulse was delayed by 200 nsec. and its pulse width was 1.6 µsec. Both the pulsed DC and RF sampling location

was at 1.5 μsec into the drain pulse. The duty cycle used during measurements was .1 %.

IV. Results

For the BJT device, two basics measurements were performed. The first was a DC measurement of the forward current gain and the second was a measurement of the unit gain frequency Ft. To calculate the value of Ft, S-parameters were measured at the desired bias, between .5 GHz and 8 GHz, and then converted to H-parameters, where the value of Ft was interpolated between the adjacent frequency points in which the magnitude of H21 became less than unity.

Fig. 3 shows constant and pulsed DC forward current gain β_f vs. collector voltage for base to emitter voltage of 0.9 V and 1.0 V, for the BJT device. As expected, the constant DC values of the forward current gain are consistently higher than the pulsed DC measurement values, due to the effect of thermal run-away during the constant DC measurements.

Fig. 4 shows constant and pulsed DC/RF Ft vs. base to emitter voltage for a collector to emitter voltage of 10.0 V for the BJT device, while fig. 5 shows Ft vs. the collector current. The peak Ft value calculated from the pulsed S-parameters measurements is about .2 GHz higher than the one calculated from constant S-parameters. But the biggest difference is not in the peak value of Ft, but its high current roll-off behavior, where the pulsed measurement shows that the value of Ft does not compress nearly the same as in the constant S-parameter measurement.

For the LDMOS device three distinct measurements were performed. First, the drain to source current was measured as a function of both the drain to source voltage and the gate to source voltage. From the measured values of drain current, both the output conductance Gds and transconductance Gm were calculated. The second set of measurements performed determined the Ft under constant and pulsed DC/RF excitations. The method used was identical to the one described for the BJT device. Finally, the three main nonlinearities of the LDMOS, the transconductance Gm, the output conductance Gds and the gate to source capacitance Cgs were extracted with the use of 1 GHz S-parameter measurements.

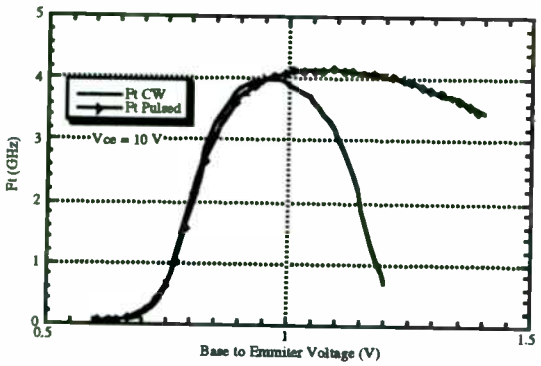

Fig. 4 Constant and pulsed DC/RF Ft vs. base to emitter voltage for a collector to emitter voltage of 10.0 V.

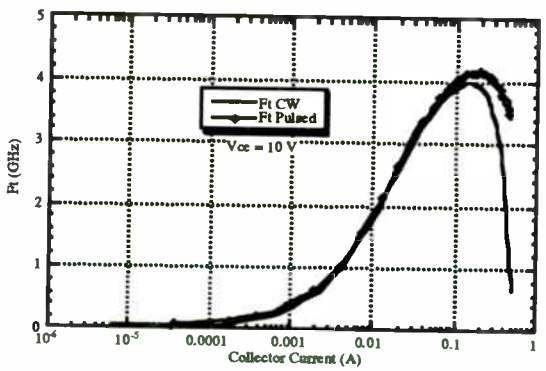

Fig. 5 Constant and pulsed DC/RF Ft vs. collector current for a collector to emitter voltage of 10.0 V.

Fig. 6 shows constant and pulsed DC drain current for the LDMOS device vs. drain to source voltage for gate to source voltages from 4.0 V to 10.0 V, while fig. 7 shows constant and pulsed DC drain current vs. gate to source voltage for drain to source voltages of 5.0 V to 20.0 V. Both figures show significant differences between constant and pulsed DC measurements.

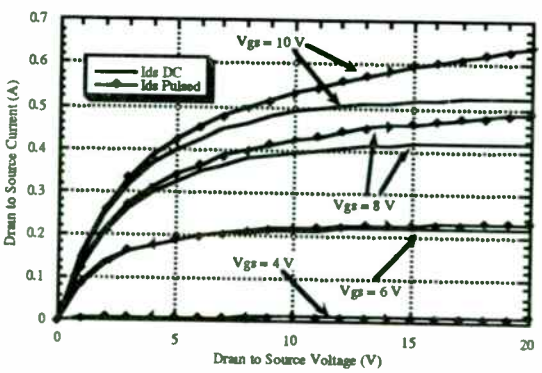

Fig. 6 Constant and pulsed DC drain current vs. drain to source voltage for gate to source voltages from 4.0 V to 10.0 V.

Based on these measurements, it's not surprising that significant differences should also appear in constant vs. pulsed DC values of Gds and Gm. A clear comparison of the constant and pulsed DC output conductance Gds vs. drain to source voltage for gate to source voltages varying from 4.0 V to 10.0 V is shown in fig. 8. Fig. 9 shows constant and pulsed DC transconductance Gm vs. gate to source voltage for drain to source voltages of 5.0 V and 20.0 V. Notice how the constant and pulsed DC values of Ids, Gds and Gm diverge from each other as the power dissipation (i.e., the product of Vds and Ids) increases, showing the clear effect of self heating in the device.

As in the case of the BJT, the Ft values extracted from pulsed measurements does not show the same high current roll-off behavior as constant DC/RF measurements. As mentioned earlier the Ft values were extracted under constant and pulsed DC/RF S-parameter measurements. Fig. 10 shows constant and pulsed DC/RF Ft vs. gate to source voltage for a drain to source voltage of 26.0 V. Fig. 11 shows the same values of Ft but this time vs. drain to source current. Contrary to the BJT, the LDMOS device does show a significant difference in the peak value of Ft, more than 1 GHz between constant and pulsed DC/RF extraction.

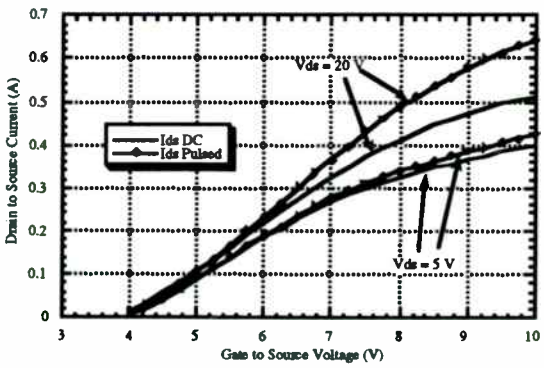

Fig. 7 Constant and pulsed DC drain current vs. gate to source voltage for drain to source voltages of 5.0 V and 20.0 V.

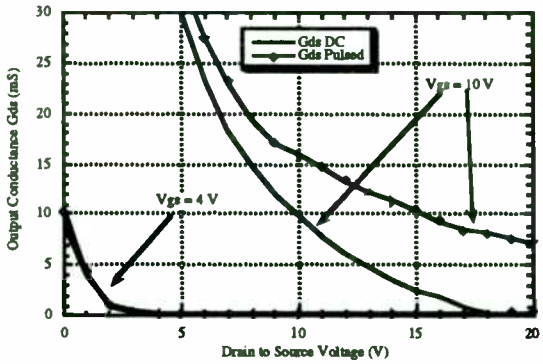

Fig. 8 Constant and pulsed DC output conductance Gds vs. drain to source voltage for gate to source voltages of 4.0 V and 10.0 V.

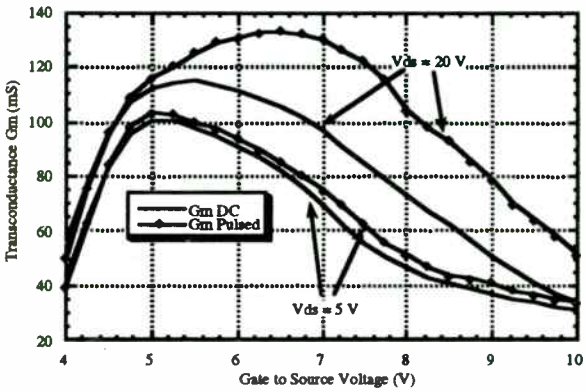

Fig. 9 Constant and pulsed DC transconductance Gm vs. gate to source voltage for drain to source voltages of 5.0 V and 20.0 V.

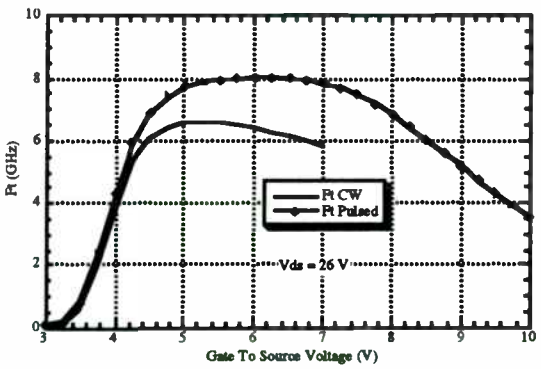

Fig. 10 Constant and pulsed DC/RF Ft vs. gate to source voltage for a drain to source voltage of 26.0 V.

S-parameter measurements were performed under both constant pulsed DC/RF conditions at 1 GHz to determine how the small signal LDMOS model parameters compared between isothermal and non-isothermal measurement conditions. Prior calculation of the intrinsic model parameters, namely , Gds,

Gm, Cgs, Cds and Cgd, package parasitcs, bond wire inductances and parasitic resistances Rg, Rd and Rs were de-embedded from the measured S-parameters. Fig. 12 shows constant and pulsed DC/RF transconductance Gm vs. drain to source voltage for gate to source voltages of 4.0 V and 6.0 V. Fig. 13 shows Gm but this time vs. gate to source voltage for drain to source voltages of 10.0 V and 30.0 V. Both of these results are consistent with the Gm extractions performed under pulsed and constant DC conditions. The output conductance Gds show trends similar to those seen in the measurement of Gm. Fig. 14 shows constant and pulsed DC/RF output conductance Gds vs. drain to source voltage for gate to source voltages of 4.0 V and 6.0 V. Fig. 15 shows Gds vs. gate to source voltage for drain to source voltages of 10.0 V and 30.0 V. Once again, the results are consistent with previous pulsed vs. constant DC extractions.

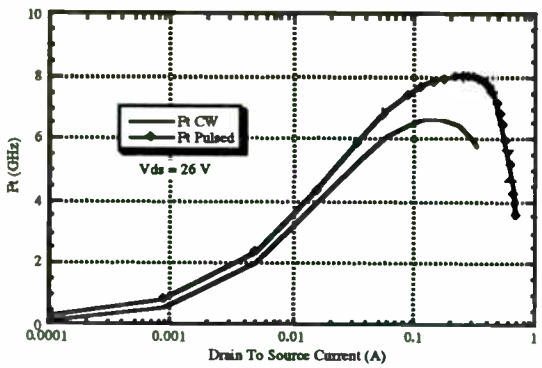

Fig. 11 Constant and pulsed DC/RF Ft vs. drain to source current for a drain to source voltage of 26.0 V.

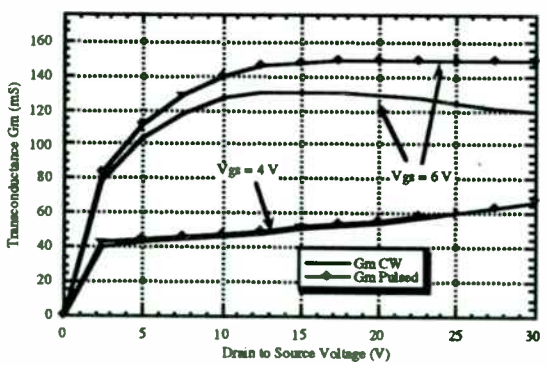

Fig. 12 Constant and pulsed DC/RF transconductance Gm vs. drain to source voltage for gate to source voltages of 4.0 V and 6.0 V.

Finally, fig. 16 shows constant and pulsed DC/RF gate to source capacitance Cgs vs. drain to source voltage for gate to source voltages of 4.0 V and 6.0 V., while fig. 17 shows its dependency vs. gate to source voltage for drain to source voltages of 10.0 V and 30.0 V. Contrary to the drain to source conductance and the transconductance, the thermal dependency of Cgs is very weak. Differences between the extracted values under constant and pulsed excitations are only about 1 to 2 %. Although not shown, both Cds and Cdg showed no significant thermal dependencies. Both of these results, for the 5.04 mm LDMOS device and the 1915 μm^2 BJT device, are consistent with what one would expect the model parameter behavior to be influenced as the device's channel and junction temperature.

V. Conclusions

The contribution of thermal effects on device model parameter have been quantified by means of extracting key nonlinear model parameters for both the high voltage LDMOS and the sub micron BJT under constant and pulsed DC and RF conditions. Results clearly indicate the need for a thermally consistent electro-thermal MOSFET and BJT models that can account for self-heating effects.

VI. References

[1] M. Dunn & B. Schaefer, Link Measurements to Nonlinear Bipolar Device Modeling, Microwaves & RF, Feb. 96.

[2] J. Meyer, D. Root & K. Poulton, Dynamic Thermal Modeling of Active Devices in Circuits, MTT Thermal Workshop, June 93.

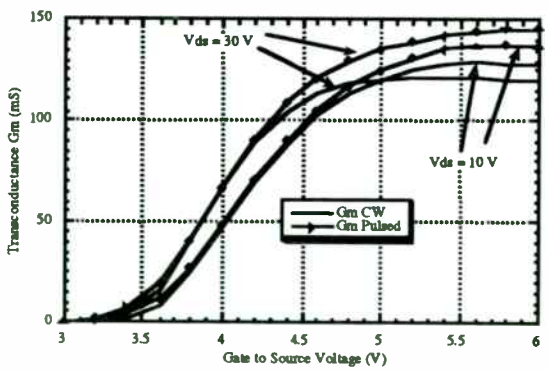

Fig. 13 Constant and pulsed DC/RF transconductance Gm vs. gate to source voltage for drain to source voltages of 10.0 V and 30.0 V.

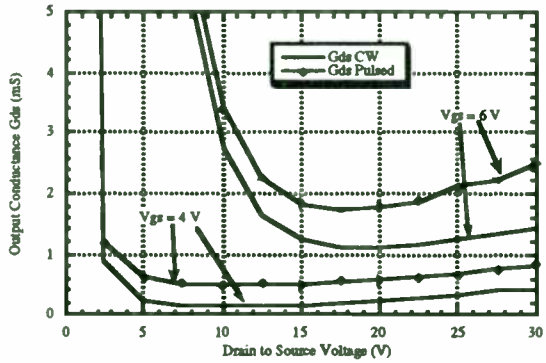

Fig. 14 Constant and pulsed DC/RF output conductance Gds vs. drain to source voltage for gate to source voltages of 4.0 V and 6.0 V.

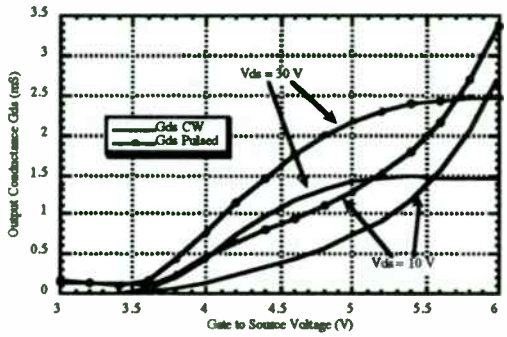

Fig. 15 Constant and pulsed DC/RF output conductance Gds vs. gate to source voltage for drain to source voltages of 10.0 V and 30.0 V.

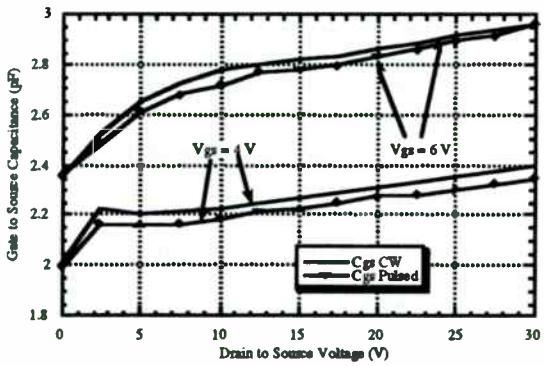

Fig. 16 Constant and pulsed DC/RF gate to source capacitance Cgs vs. drain to source voltage for gate to source voltages of 4.0 V and 6.0 V.

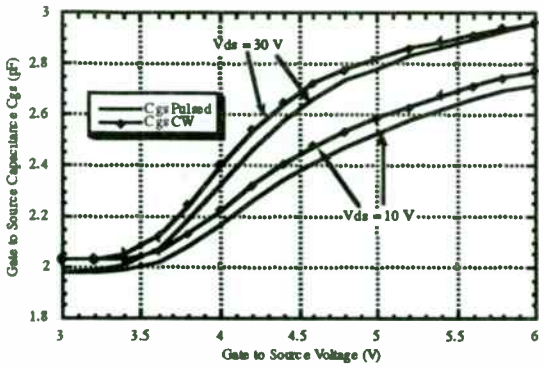

Fig. 17 Constant and pulsed DC/RF gate to source capacitance Cgs vs. gate to source voltage for drain to source voltages of 10.0 V and 30.0 V.

THERMAL DESIGN OF PLASTIC PACKAGED GaAs RFIC POWER AMPLIFIERS

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ABSTRACT

The trend in the wireless market of producing higher power amplifiers in smaller packages continues to challenge engineers to balance cost and reliability when designing and manufacturing high power devices. ITT GTC has developed a unique thermal modeling and measurement process for its RFIC products, to accurately determine device temperatures for a wide variety of applications. The validation of modeled results is a key engineering challenge, which we have met using a combination of analytical and finite element models and by empirical measurements using liquid crystal techniques. Using this multifaceted approach, we have been able to integrate thermal design as an iterative part of the design and development process.

This presentation will focus on a three dimensional thermal analysis of a GaAs power amplifier in a plastic SOP-16 package, mounted on a printed circuit board (PCB). Finite element techniques are used to analyze this complex structure including the chip, die attach, leadframe and plastic molding compound, the surface mount solder, and the PCB for varying boundary conditions, representative of wireless communications applications. The analytical Unit Thermal Profile Method is used to refine the initial chip level analysis by considering individual heat sources and the die attach layer. To validate the modeled results, liquid crystal microthermography was performed on open cavity plastic packaged devices. The results of this approach allow us to accurately predict maximum device temperatures and ensure reliability for a variety of today's wireless applications.

INTRODUCTION

Why does the thermal design of a power device need to be considered as an integral part of the design process? There are several answers to this question, the first of which involves device reliability. For devices which dissipate power in excess of 100mW, a significant temperature rise can occur in small surface mount packages. This fact becomes increasingly important as plastic packaging trends towards smaller sized packages while dissipating higher powers, which can have a great impact on the reliability of a device. Areas of concern include the impact on mean time to failure and the integrity of the plastic package itself.

A second reason why thermal design needs be considered is cost. In today's competitive wireless communications market it is essential to design the system correctly the first time at the lowest possible cost. There is no time to design, fabricate, and assemble a device only to find out that it fails due to excessive temperature.

With these ideas in mind, the goal of this paper is to discuss how to design a high power IC which concurrently meets the thermal design and cost requirements. To achieve typical wireless application power dissipations of 1-5 Watts, an accurate modeling process is required. The following section will discuss the primary approaches to thermal modeling and how they can be used as part of a robust design process.

THERMAL MODELING APPROACHES

Figure 1 summarizes several options for incorporating thermal modeling into the overall design process. Four techniques are presented. The first thermal modeling approach involves rough calculations. This includes "back of the envelope" calculations of device and leadframe thermal resistance, and temperature rises for a power device. This method has roughly a 20% to 30% accuracy. It can be used in the early phase of a design to estimate if the concept is thermally feasible without expending a great deal of time and effort.

The next step in Figure 1 involves physics-based analytical thermal models. This involves such things as chip level models which take into account individual heat sources and temperature dependent material properties. Examples of these include The H. Cooke Model [9] and The Unit Thermal Profile Method [5]. These provide more accurate calculations of maximum device temperature with accuracy of roughly 10% to 20%. This step could be used after the concept phase and before the preliminary design review to

provide more detail while still keeping time and effort spent to a minimum.

Method	A	B	C	D	E
	Rough Estimate	Analytical Models	FEA Models	FEA & Analytical Combination	Physical Measurements
Approximate Accuracy	30%	20%	5%	2%	1%
Average Completion Times	1-2 Days	2-3 Days	2-3 Weeks	1-2 Months	1-2 Months
Strengths	Short Time for Completion	Multiple Heat Sources Individual Heat Sources	Multiple Heat Sources Exact Geometry and Boundary Conditions	High Accuracy Complex Layouts B&C Strengths Combined	Highly Accurate Repeatable Actual Operational Data
Weaknesses	Low Accuracy	Simulated Boundary Conditions	Involved Distributed Area Heat-source Approximation	Long Completion Time	Long Setup Time Not Possible on Some Devices

Figure 1: Table of Modeling Options, Accuracy, Strengths and Weaknesses

The third step for incorporating thermal modeling into the design process is finite element modeling. Finite element involves creating a highly accurate geometric representation of a power device, assigning boundary conditions to the device and running it using power dissipations typical of the intended application. The accuracy from this technique is approximately 5%. This approach could be used as part of a detailed design review when specific operating conditions need to be thermally evaluated. Finite element modeling represents a significant investment of time and would probably not be used until a design had a high probability of moving to production.

The next step involves merging the best aspects of the analytical and finite element models to improve the overall model accuracy to roughly 2%. This could be done as part of a performance and yield review where highly accurate thermal performance data is required to verify that the parts meets customer thermal specifications based on actual device data such as voltage, current, and ambient temperature. Again, since this represents an even greater level of effort it is done when a part was ready for production.

Figure 2 summarizes the areas of a generic design process flow where each type of modeling listed above could be used.

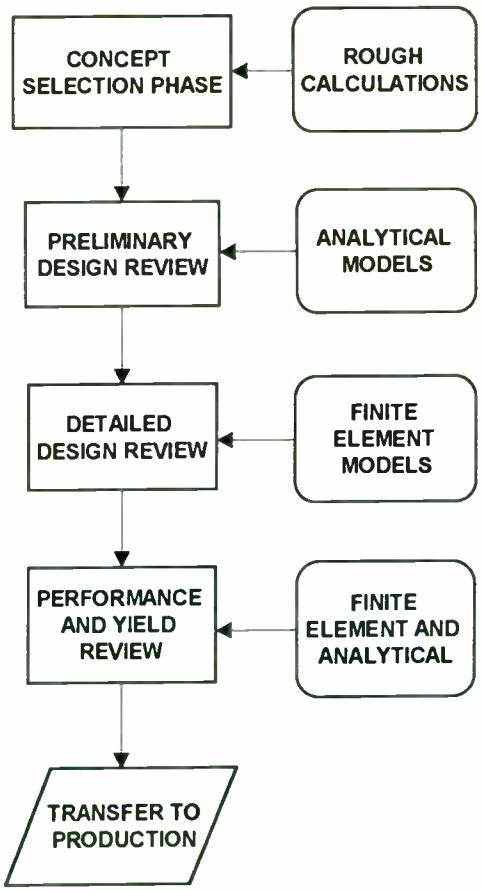

Figure 2: Generic Design Process Flow with Sample Modeling Approaches Added

Thermal analyses enable designers not only to predict thermal performance but also to cultivate new heat transport enhancement ideas using "what if" scenarios.

THE FINITE ELEMENT MODEL

The finite element model (FEM) represents a very powerful tool for thermal design and modeling. Some of the advantages FEM has over other modeling approaches are: First, complex geometries of a device can be modeled exactly. Second, compound materials, such as a copper leadframe surrounded by plastic molding compound, can be modeled using finite element techniques. Also FEM can include temperature dependent material properties. This iterative temperature dependent capability is critical to achieving an accurate model of a GaAs power amplifier, since GaAs thermal conductivity varies with temperature. Figure 3 below illustrates GaAs thermal conductivity as a function of temperature. The effect of ignoring the change in GaAs thermal conductivity from 25°C to 150°C would lead to a large error in the modeled results.

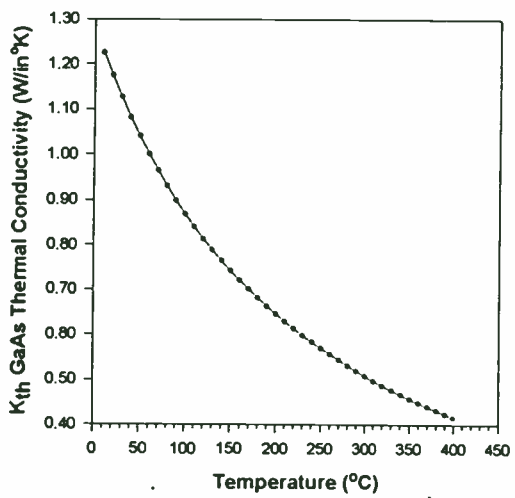

Figure 3: GaAs Thermal Conductivity vs. Temp.

Third, the finite element model can simulate real world boundary conditions such as conduction of heat through a leadframe or convection of heat from a printed circuit board into the air.

An example of using finite element techniques to accurately model temperature profiles of an ITT GTC GaAs RFIC power amplifier in an SOP-16 package follows. In this example the device chip has two field effect transistors (FETs). Other components on the chip are neglected because they generate very little heat. For a valid comparison between the modeling results and the empirical data, the FE model is constructed using the same boundary conditions as the experimental setup.

A total dissipated power of 0.65 Watts is used in this example. FET A has one 300μm by 1μm gate finger dissipating 0.105 Watts of power and FET B has sixteen 150μm by 1μm gate fingers with a finger pitch of 15μm dissipating 0.545 Watts. Due to the large difference in size between the FET fingers and the PCB (3.8cm by 4.2cm), it is impractical for finite element (FE) method to model all individual FET fingers with the appropriate element dimension aspect ratio and a manageable number of elements. Thus, in the FE analysis, FET A is modeled as 3 nodes with concentrated power of 0.035 Watts each spaced at 100μm from one another and FET B is approximated by one uniform heat source that covers the same area and position on the die as FET B does.

Further refinement of the chip model to cover individual fingers of FET B will be presented in the next section. A standard FE software package is used for the FE analysis [1]. The complete FE model includes the chip, the package, the solder joints and the PCB. A total of 25,616 elements and 30,736 nodes are used for the complete structure. The 3-layer PCB consists of top and bottom copper layers each measuring 35μm in thickness and a 500μm FR-4 layer sandwiched in between.

Figure 4 lists the material properties for the SOP-16 package. A free air convection coefficient of 10 by 10^{-4} W/cm^2-°C is used on all surfaces of the structure with an ambient temperature of 27°C.

Layer No.	Material	Thickness mm	Thermal Conductivity W/cm-°C
1	Molding	450	7.0 by 10^{-3}
2	GaAs	125	0.45 @27°C
3	Copper Leadframe	200	3.6
4	Molding	650	7.0×10^{-3}

Figure 4: SOP-16 Package Material properties

Figure 5 shows the plastic SOP-16 package of the complete model with the calculated temperature distribution. The die-

attach layer is not shown in Figure 4. The die-attach layer (25μm) is very thin comparing to the whole structure. Very large element aspect ratio and a large number of elements must be used to model such thin layer in a large structure. Thus it is impractical to model it using FE technique. While most die-attach adhesives have poor thermal conductivity, the ITT GTC SOP-16 packages use high thermal conductivity adhesive epoxy that has approximately 87% of thermal conductivity of copper, to improve the overall device thermal heat transfer. Thus the die-attach layer is considered as a portion of the leadframe to simplify the FE model. However, the die-attach will be treated as a separate layer in the chip model to be presented in the next section.

Figure 6 displays the FEM leadframe mesh with calculated temperature contours. Figure 7 shows an enlarged view of the leadframe near FET B. The leadframe geometry is modeled in detail to obtain information on how the shape of leadframe affects the heat conduction efficiency. In this area FE method stands above all numerical and analytical methods. Several geometries can be modeled and thermally evaluated. This allows an engineer to iterate design parameters with high confidence to obtain the best thermal design without having to physically fabricate, and test the device. Figure 8 shows the GaAs chip mesh with the temperature distribution. Figure 9 depicts an enlarged view of the die at FET B. The peak temperature of 109.5^{o}C occurs at about the center of FET B. Temperature dependence of GaAs thermal conductivity has been included in the FE model. This result will be compared to other modeling and measurement techniques in the final section.

Due to the comparatively low thermal resistance of the ITT GTC SOP-16 fused leadframe, only 0.16% of the total heat escapes through the surfaces of molding compound by still air convection. The remaining heat conducts through the leadframe, solder, PCB copper and then convects to the air. Little heat is carried to those leads that are not connected to the die-pad of the copper leadframe. The temperature of the die bottom is approximately 74.5^{o}C. This temperature is later used as a worst case isothermal bottom temperature for the chip model. Based on the fact that only a small fraction of the heat escapes through the molding compound, an approximation of an adiabatic top surface and isothermal bottom surface can be used for the analytical chip model which allows an important approximation as will be discussed in the next section.

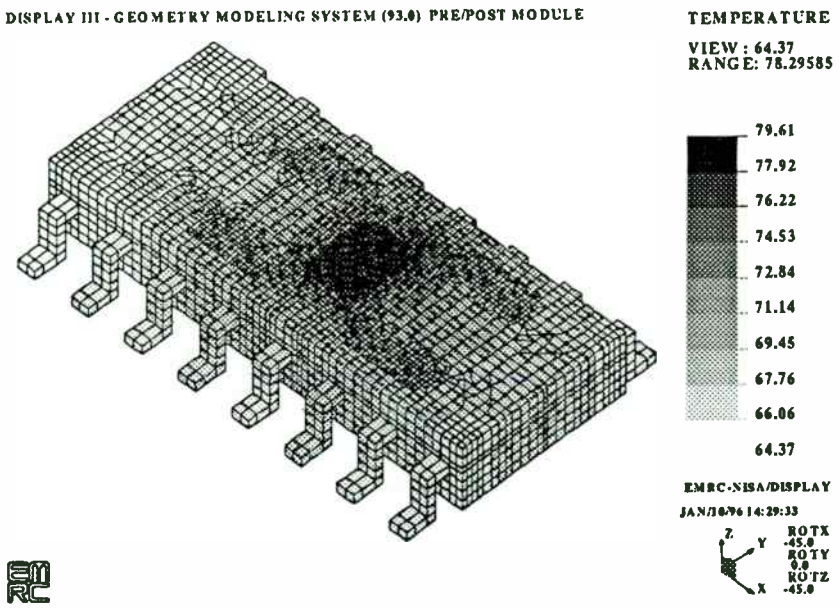

Figure 5: Finite Element Model showing ITT GTC SOP-16 Package

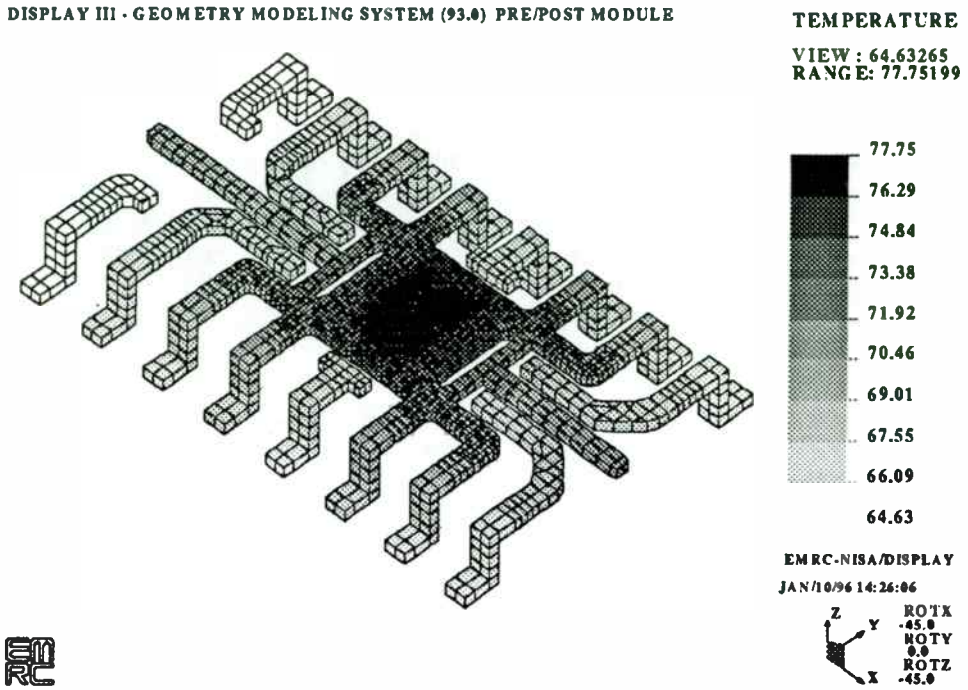

Figure 6: Meshed leadframe with calculated temperature information.

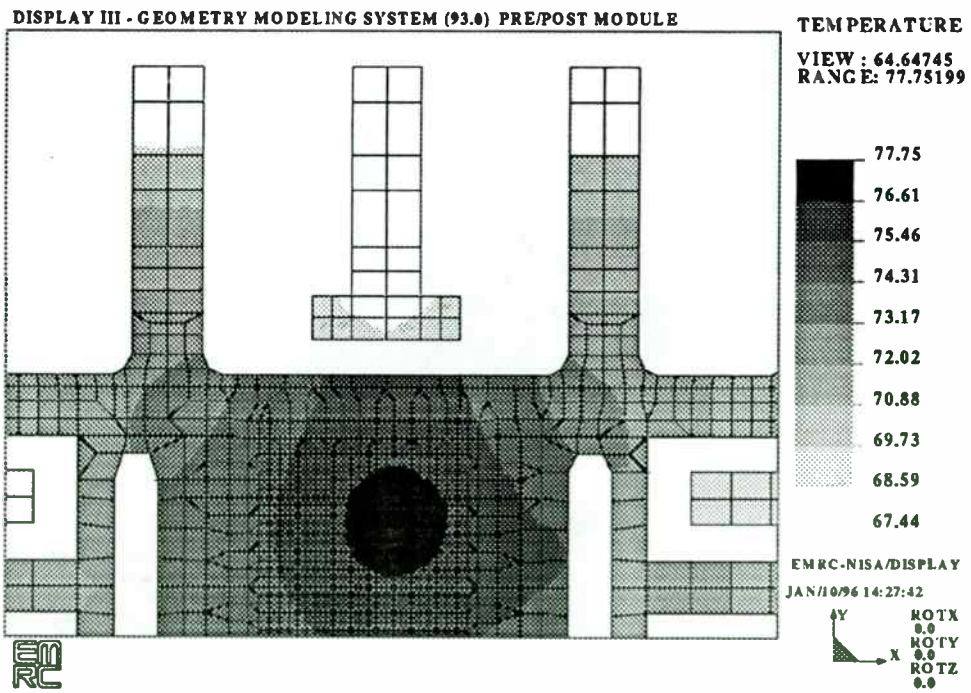

Figure 7 Detailed view of the leadframe near FET B.

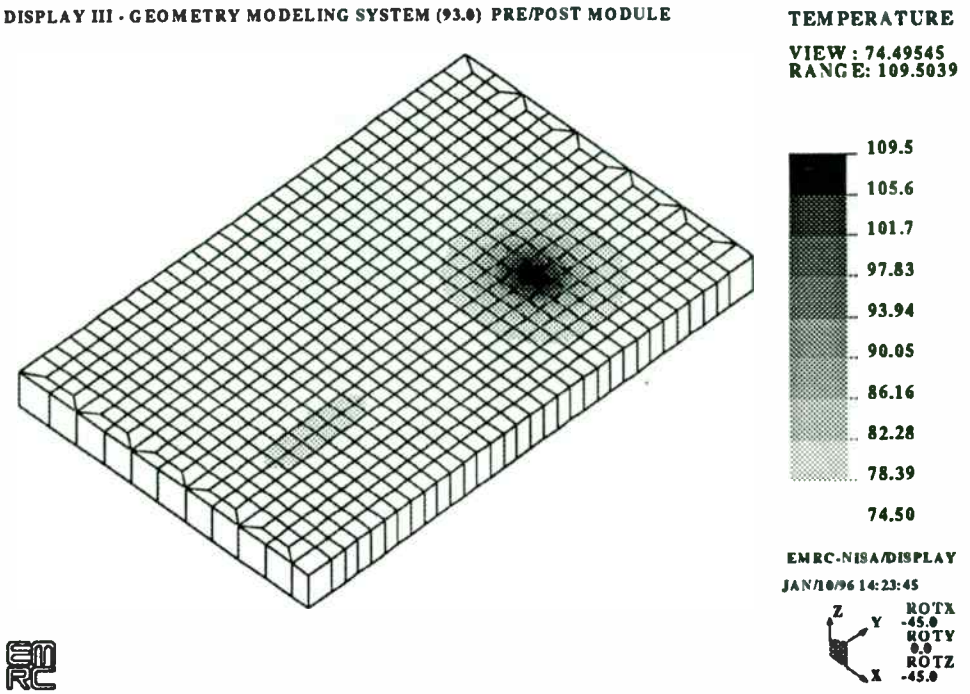

Figure 8: GaAs chip with two heat sources representing two FETs.

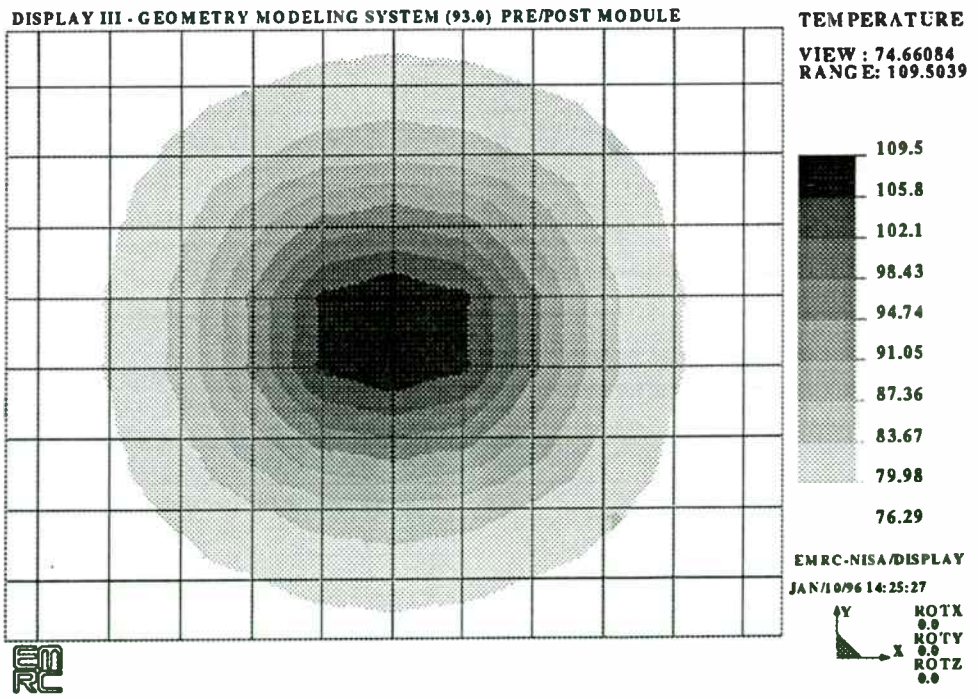

Figure 9: Detailed view of FET B.

ANALYTICAL CHIP LEVEL MODEL

In the finite element model above, each FET is approximated by a uniform heat source or nodal heat source to keep the number of elements manageable. In reality, FET B is constructed of 16 fingers each forming a highly elongated heat source. To take all individual fingers into account, and to allow analysis of chips having a large number of transistors, we turn to the unit thermal profile approach for chip level modeling [2]. The GaAs chip is modeled as a two-layer structure with properties listed in Figure 10. In the FEM, the die-attach layer is not separately modeled due to the limitations discussed above. In the analytical chip model, these limitations do not apply. Therefore, the unit thermal profile method can include the thin die-attach layer in our chip model. From the results of FEM analyses, it is known that only 0.16% of heat escapes through the molding compound surfaces. Thus, the heat that dissipates from the chip into the upper molding compound would be even less. Accordingly, the boundary condition approximations of an adiabatic GaAs top surface and finite lateral boundaries with an isothermal bottom surface below the die-attach, are valid. Since the chip is attached to high thermal conductive copper leadframe, an isothermal bottom surface is also a good approximation.

Layer No.	Material	Thickness μm	Thermal conductivity W/cm-°C
1	GaAs	125	0.45 @27°C
2	Die-Attach	25	3.143

Figure 10: Analytical Model Material Properties.

The chip level analytical model consists of a circular unit source of 1 μm^2 in area with an arbitrary power dissipation of 1 mW. Using PAMICE software [3] written based on analytical temperature solutions of structures with a circular heat source [4], the unit thermal profile produced by the unit source is calculated at the isothermal base temperature of 74.5°C as shown in Fig. 5. The FET finger sources on the chip are next automatically decomposed into a large number of unit sources by UNITHERM [5], a program written based on unit thermal profile approach [2]. The powers and locations of the unit sources are determined by the dissipated powers and layout of the FET fingers on the chip. The overall temperature profile on the chip is then the summation of the profiles produced by all unit sources weighted by the power and distance factors referenced by the unit thermal profile plus the image sources. Image sources are included when a heat source is close to the adiabatic lateral boundaries of the chip. To take into account the temperature dependence of GaAs thermal conductivity, Kirchhoff transformation is applied [6], [7]. Figure 11 displays the resulting temperature profile calculated by UNITHERM after taking care of the GaAs thermal conductivity temperature dependency. The total power used is 0.65 Watts. The isothermal die-bottom temperature used is 74.5°C from the FEM results.

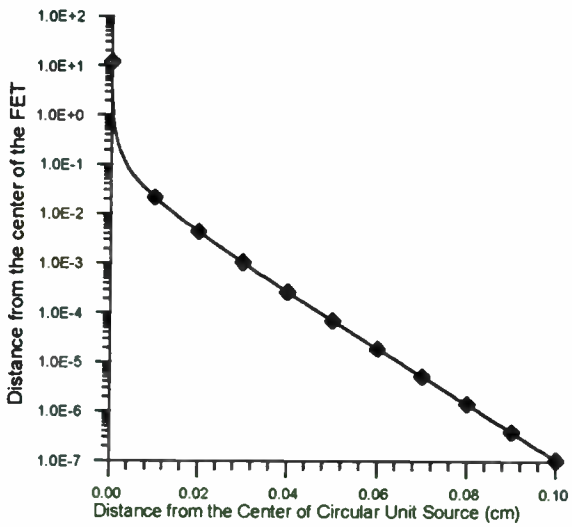

Figure 11: Unit thermal profile as a function distance from the circular source having 1mW power with 1mm^2 area at the isothermal base temperature of 74.5°C from the FE results.

Figure 12 illustrates the analytical chip level temperature profile. The results indicate a temperature rise at the junction of the larger FET of 37.1°C. When this is added to the base temperature of the die (74.5°C), the resulting maximum FET temperature calculated by the analytical chip level model is 111.6°C. This result will be referenced for comparison in the next section.

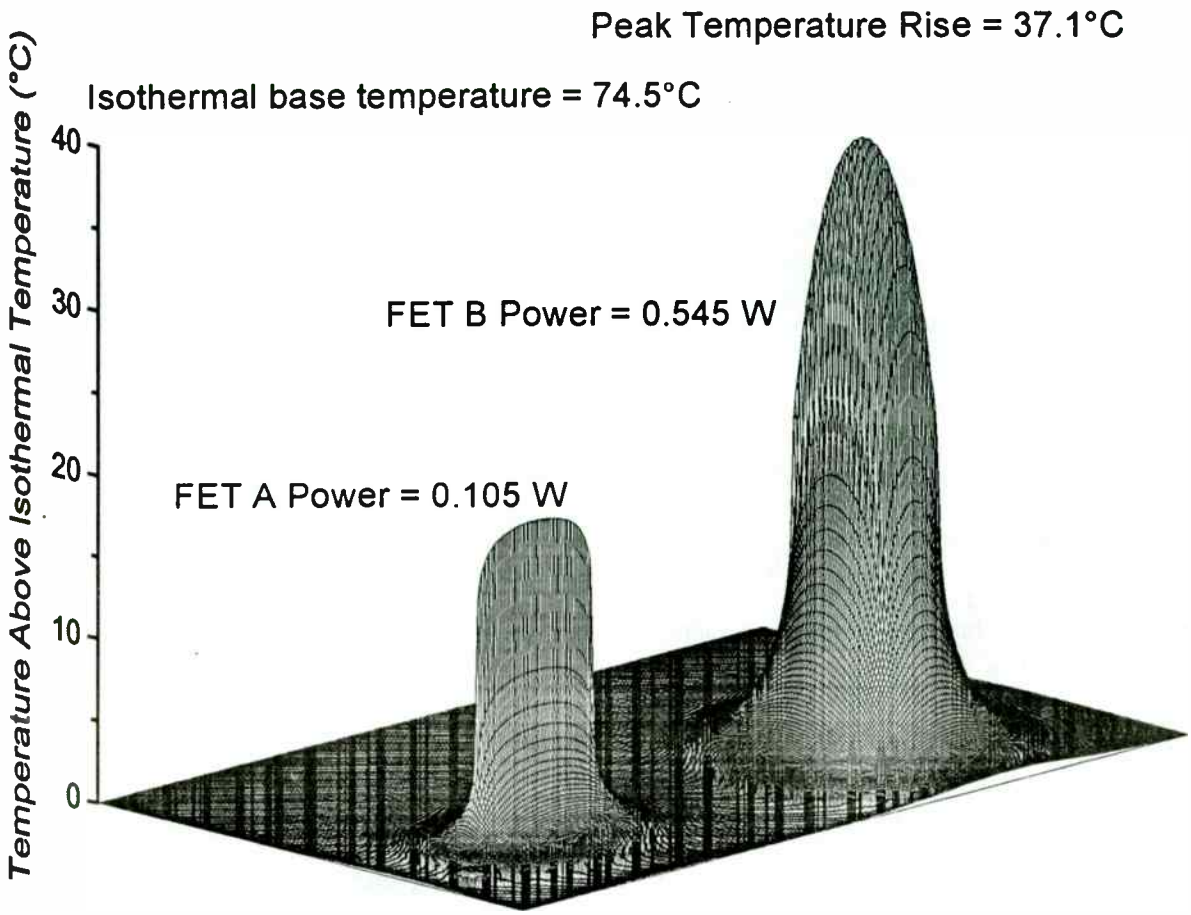

Figure 12: Analytical Thermal Model Temperature for the GaAs Chip

COMPARISON OF MODELING APPROACHES

Upon comparing the results from the FE and Analytical modeling approaches above, the peak temperature from the chip model is found to be 2.1°C higher than the FE model. (111.6°C for the analytical model, 109.3 for the FEM) This is due to the chip model accounting for individual FET finger heat sources instead one large uniform source as in the FE model. Thus the heat fluxes on the FET fingers are concentrated within each finger rather than distributed over the entire FET area. Figure 13 illustrates the contrast between the analytical model and finite element model results for FET B. Notice the sharp temperature rise from the analytical model which corresponds to the center of a FET gate finger heat source. Figure 15 will summarize these values for comparison to empirical data at the end of the next section.

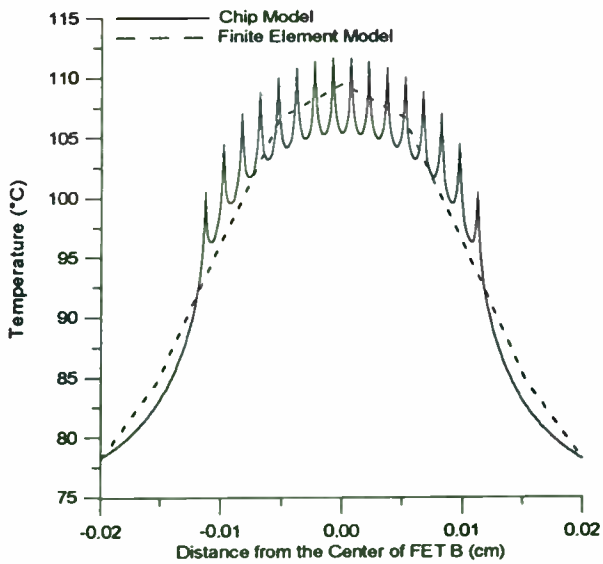

Figure 13: Temperature profile comparison between FE and chip models across FET B fingers.

VALIDATION OF MODELED RESULTS

Validation of the modeled results is critical and must be done before using the results to commit to a design. Invalid assumptions regarding boundary conditions and material properties can lead to large errors in the peak temperatures. For this reason initial models need to be validated by using empirical measurements. For example, the first FE model should be of a device which can also be empirically measured. This allows a direct comparison between modeled and empirically measured results. Using the empirical results, one can adjust model variables such as the still air convection transfer coefficient until the modeled results correlate to the empirical data. That coefficient can then be used as a boundary condition in a future model with a high degree of confidence in its accuracy.

To verify the calculated chip temperatures from both modeling approaches, empirical thermal measurements were made using liquid crystal microthermography [8]. The packaged parts were de-processed to expose the GaAs chip surface. The FEM analysis results presented earlier showed that only 0.16% of heat escapes from the chip into the upper molding compound. Thus, the removal of the compound on top of the chip should have little effect the accuracy of the measured results. After de-processing, the chip surface was coated with a nematic liquid crystal that has a phase transition temperature ~110°C. When the crystal is viewed through a polarizing microscope, it is possible to distinguish the transition with a spatial resolution of about 2 μm.

To determine the thermal resistance of the unit under test, a thermocouple was attached to the arbitrarily chosen thermal reference plane where the leads of the package are soldered. Then the device bias is slowly increased until phase transition is observed at the hottest point on the FET. The power being dissipated in the device at the transition is recorded. This power is determined for a series of different reference temperatures controlled by a hot plate and measured by a thermocouple. The results in reference temperature are plotted against the dissipated power to find the thermal resistance. The intercept of the fitted curve represents the transition temperature of the crystal while the slope is proportional to the thermal resistance.

Measurements were made on the same GaAs device previously modeled using the liquid crystal method described above. In the measurement, only FET B was used and thus the power measured was consumed by FET B alone. A linear regression was performed on the data to obtain the crystal transition temperature and the thermal resistance. The results for this measurement were a crystal transition temperature of 110.8°C and a thermal resistance of 77.4°C/W. Figure 14 displays the measured data.

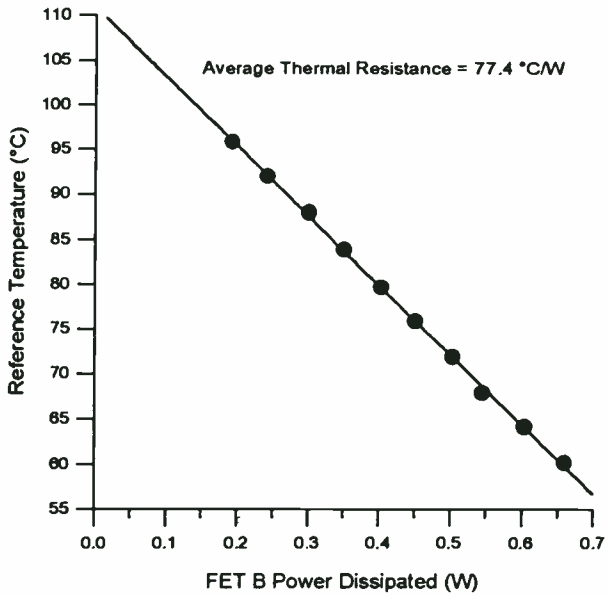

Figure 14: Reference temperature at liquid crystal phase transition versus power dissipated.

The FE model yields a peak temperature of 109.5°C at the center of FET B and a thermal resistance of 76.0°C/W. Similarly, the chip model obtains a peak temperature of 111.6°C. Using a previously measured thermal resistance value for the leadframe and the chip model results, the chip model junction to leadframe thermal resistance is 79.8°C/W. The empirical data obtained from the liquid crystal measurement, as displayed in Fig. 8, yields a thermal resistance of 77.4°C/W, quite close to the calculated values. Figure 15 summarizes the temperature and thermal resistance data above.

Model Description	Peak FET Temperature	Thermal Resistance Junction to Leadframe
Analytical Chip Model	111.6°C	80 °C/W
Finite Element Model	109.4 °C	76 °C/W
Physical Measurement	112.2 °C	77 °C/W

Figure 15: Summary of Validation Results

CONCLUSION

As the wireless communications industry trends towards using smaller IC's that dissipate higher powers, the importance of thermal modeling as part of the design process will continue to grow. Several modeling approaches have been presented as examples of how to accomplish this task. The modeled results were then validated by a close correlation to empirical measurements. This validation allows the thermal models to be used as accurate tools for predicting future device behavior during the design phase, as well as in different application environments.

REFERENCES

[1] NISA II Finite Element Heat Transfer version 93.0, Engineering Mechanics Research Corp., Troy, Michigan.

[2] Chin C. Lee and Arthur L. Palisoc, "Real-Time Thermal Design of Integrated Circuit Devices," *IEEE Trans. Components, Hybrids, and Manufacturing Tech.*, 11, pp. 485-492, Dec. 1988.

[3] Chin C. Lee and David H. Chien, "PAMICE - A Program for the Potential Analysis of Multilayer Infinite Plate Structures with Circular Embedded Sources," Software, version 1.0, 1994.

[4] David H. Chien, Chen Y. Wang and Chin C. Lee, "Temperature Solution of Five-Layer Structures with a Circular Embedded Source and Its Applications," *IEEE Trans. CHMT*, 15, pp. 707-714, Oct. 1992.

[5] David H. Chien and Chin C. Lee, "UNITHERM - Unit Thermal Profiler," Software, version 1.1, 1995.

[6] Arthur L. Palisoc and Chin C. Lee, "Thermal properties of the multi-layer Infinite Plate Structure," *J. Applied Physics*, 64(1), pp. 410-415, July 1988.

[7] H.S. Carslaw and J.C. Jaeger, *Conduction of Heat in Solids*, 2nd Ed., p. 11, Clarendon, Oxford, 1959.

[8] Gidi Fleuren, "Liquid Crystal Micro-thermography - State of the Art," *IEEE Semiconductor Thermal and Temperature Measurement Symp.*, Dec. 1986.

[9] H. Cooke, "Precise Technique Finds FET Thermal Resistance," *Microwaves & RF*, Aug. 1986.

Predicting Nonlinearities in a MRF20060 Applications Circuit Using AM-AM and AM-PM Characteristics

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Abstract

This paper describes a method for predicting nonlinear behavior of a MRF20060 RF power amplifier. Using single tone gain and phase characteristics of the power amplifier the nonlinear amplification can be simulated for various modulated signals. The intermodulation distortion (IMD) of multi-tone or spectral regrowth of digitally modulated signals can then be predicted. In this article a two tone signal and a Code Division Multiple Access (CDMA) modulated signal will be examined.

I. Introduction

The emergence of digital modulation schemes has set stringent linearity requirements for RF power amplifiers used in wireless communication systems. Characterizing linearity is of prime importance when designing a power amplifier.

In this paper, the technique of predicting intermodulation distortion of multi-tone and spectral regrowth of CDMA signals by using single-tone gain compression (AM-AM) and amplitude-phase distortion (AM-PM) characteristics is presented. Our primary interest is to predict nonlinearities of a Motorola MRF20060 class-AB application circuit. The MRF20060 is a 60 W submicron bipolar RF power transistor used in base station applications. The application circuit is capable of over 9 dB gain, better than 33% efficiency and less than -30 dBc IMD for a 60 W output PEP two tone signal across the band of 1.93 to 1.99 GHz.

II. Theory of Operation

A common way to measure nonlinearites is by examining the IMD of a two-tone signal. Intermodulation distortion products are generated by nonlinear amplifiers when two or more frequencies are amplified. For the two-tone case, the odd order products (such as the third $2f_1$-f_2 or $2f_2$-f_1, the fifth $3f_1$-$2f_2$ or $3f_2$-$2f_1$, and the seventh order $4f_1$-$3f_2$ or $4f_2$-$3f_1$) occur near the frequency of operation and are difficult to filter out. Spectral regrowth is a specific case of IMD and occurs when nonlinear amplifiers are used to amplify digitally modulated signals.

A modulated RF signal can be represented by its equivalent lowpass representation if the signal is narrowband and its envelope is slowly varying when compared to the carrier frequency. Let x(t) be the input signal,

$$x(t) = |x(t)| e^{j\Theta(t)} \qquad (1)$$

where $|x(t)|$ represents the magnitude and $\theta(t)$ the phase of x(t). The gain compression G(•) and phase distortion P(•) characteristics of a

nonlinear device, as a function of the magnitude of the input signal |x(t)|, can be used to characterize nonlinear behavior for different modulation schemes. The distorted output signal y(t) can be found as Eq. 2.

$$y(t) = |x(t)|\,[G(|x(t)|)]\,e^{j[\theta(t) + P(|x(t)|)]} \qquad (2)$$

III. Application Circuit

Using the device impedance, a microstrip matching network was constructed from RO4003™ board as shown in Fig. 1. The circuit board and device were mounted on a 2" by 3" heatsink. A temperature compensating transistor was used for the base supply. Simple quarter wave lines were used for the bias supplies.

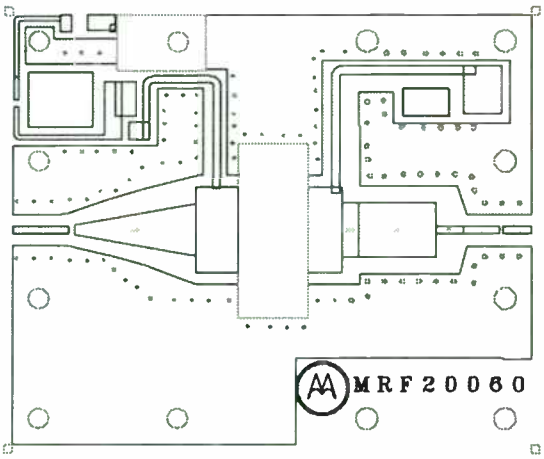

Fig. 1 Circuit board layout

IV. Making the Measurements

A HP 8753D vector network analyzer was used to measure the single tone gain characteristics of the amplifier. The setup is shown in Fig. 2. The procedure for setting up the network analyzer is described in the appendix. The power meter was used to monitor the output power. Fig. 3 and 4 show the gain compression and phase distortion characteristics of the device.

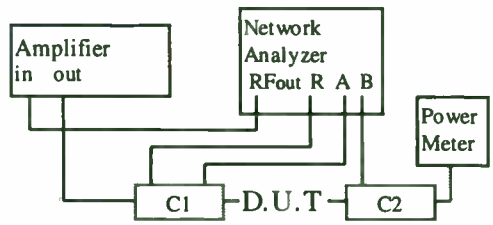

Fig. 2 Setup for power sweep characterization

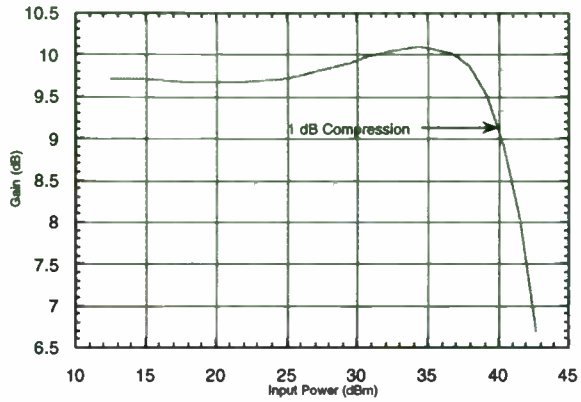

Fig. 3 Gain Characteristics of MRF20060 vs. Input Power

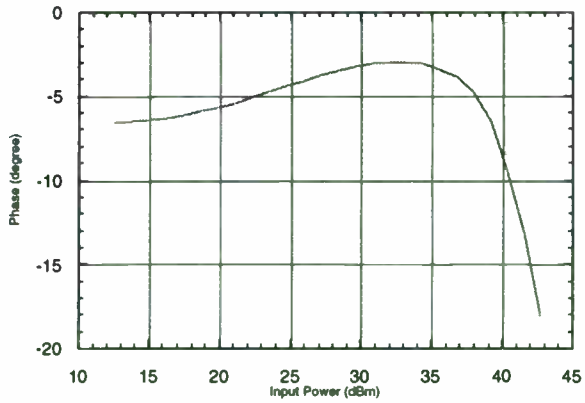

Fig. 4 Phase characteristics of MRF20060 vs. Input Power

V. Simulating Nonlinearities

MatLab™ was used to simulate the nonlinear behavior using the AM-AM and AM-PM

characteristics of the circuit. The single tone gain characteristics as a function of input voltage were spline-fitted. Two signals were examined. First, as a proof of concept, a two-tone signal was examined. This is simply two equal amplitude cosine signals, with a small frequency spacing, added together. Second, a forward link QPSK CDMA signal was used. A random number generator was used to generate the I and Q data. The data was then oversampled four times. The signal was then multiplied with the FIR filter in the frequency domain.

After generating the signals, they were then sampled in the time domain. The sampled signal was multiplied by the complex gain measurement. The distorted output signal was then transformed to the frequency domain and the IMD or spectral regrowth was measured. The process was repeated for a range of input power levels.

V. Discussion of Results

First, the intermodulation distortion of a two-tone signal was investigated. The third, fifth and seventh order IM products on both the right and the left side of the signals were measured.

Fig. 5 shows the measured and predicted IM products of a 5 kHz spaced two-tone signal. Data was collected from 1 to 70W PEP output power. Most measured IM products match closely to the prediction. The -30 dBc point was reached at 60W output power.

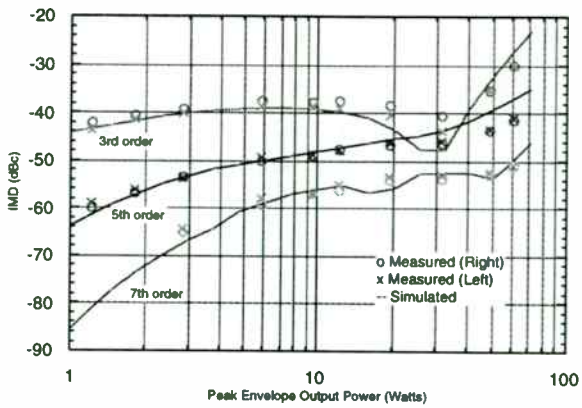

Fig. 5 IM products of a two-tone signal, 5 kHz apart

Different tone spacings were used and IMD measurements were taken. It was observed that as the two tone frequencies grew farther apart from each other, the measured IM products deviate more from the predicted values. Fig. 6, 7 and 8 shows the measured (R for Right, L for Left) and predicted (dotted lines) third, fifth and seventh order IM products of 10 kHz and 100kHz apart two-tone input signals.

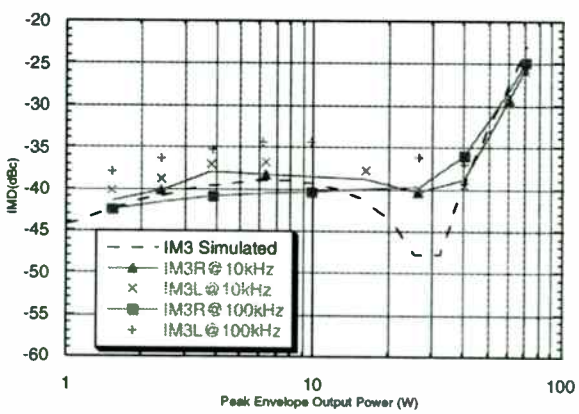

Fig. 6 Third order IM products

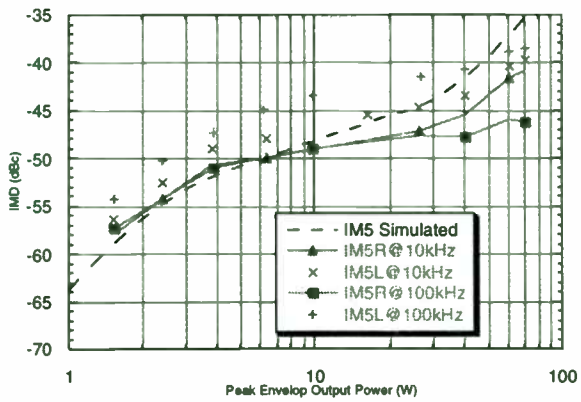

Fig. 7 Fifth order IM products

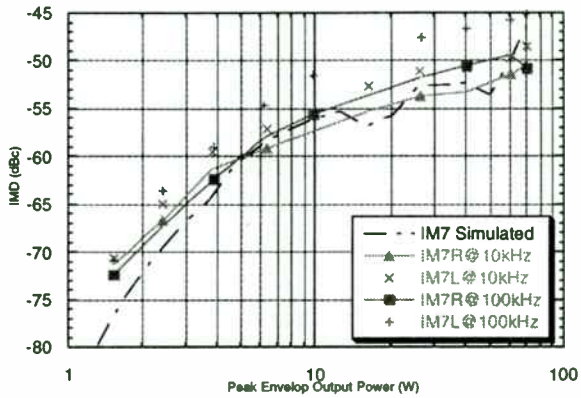

Fig. 8 Seventh order IM products

It was also observed that the IM products on the left side of the two-tone signal generally deviate more from predictions than the ones on the right. Table 1 shows the average deviations ($\frac{1}{N}\sum_{\text{power level}}^{N}$ | simulated – measured |) at different delta frequencies. The table also displays an increasing trend of deviation as the delta frequency increases.

Table 1 Average IMD deviations

Δf (kHz)	IM3R (dBc)	IM3L (dBc)	IM5R (dBc)	IM5L (dBc)	IM7R (dBc)	IM7L (dBc)
5	2.66	1.58	1.14	1.50	1.80	1.48
10	1.91	2.24	2.35	2.69	2.62	3.78
100	2.08	3.76	2.13	4.65	3.82	5.51

One way to eliminate this IMD deviation over tone spacing is to place a small resistance in the base feed of the circuit.

Finally, a simulated CDMA signal at 10W output power level was compared to the measured data. Figure 9 shows the simulated and measured results. As in the two tone case the right side is closer to the simulated results.

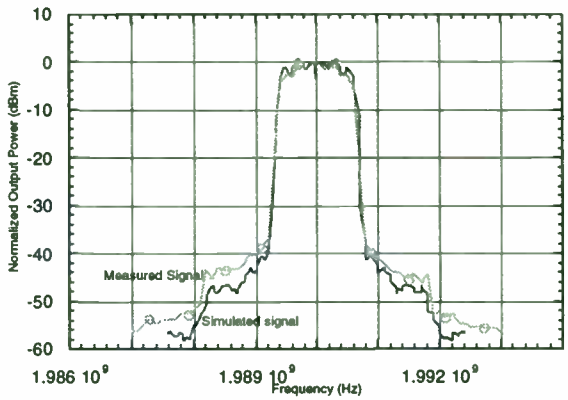

Fig. 9 Measured and simulated spectral regrowth of a CDMA signal

VI. Conclusion

The concept of using single tone AM-AM and AM-PM characteristics to predict nonlinearities for a MRF20060 application circuit has been explained. Multi-tone and CDMA signals were examined. MatLab was employed to predict the IM products using the gain and phase characteristics of the amplifier. The graphs of the measured and simulated IM products suggest the method is highly accurate. On the other hand, the limitation of the prediction method is also observed. This method works with complex digital modulation schemes as shown in the simulated and measured CDMA data.

Acknowledgment

The authors would like to thank John Sevic of Qualcomm and Jaime Pla of Motorola for assistance with generation of the CDMA signal in MatLab™.

Reference

[1] S. Chen, W. Panton & R. Gilmore, "Effects of Nonlinear Distortion on CDMA Communication Systems", IEEE MTT-S Digest, WE3D-5, 1996, p. 775-778.

[2] T. Takagi, S. Ogura, Y. Ikeda & N. Suematsu, "Intermodulation and Noise Power Ratio Analysis of Multiple-Carrier Amplifiers Using Discrete Fourier Transform", IEICE Trans Electron, Vol. E77-C, No. 6, June 1994, p. 935-941.

[3] J. S. Kenney, A. Leke, "Simulation of Spectral Regrowth, Adjacent Channel Power, and Error Vector Magnitude in Digital Cellular and PCS Power Amplifiers", Microwave Journal, Vol. 39, No. 10, October 1995.

[4] A. Oppenheim & R. Schafer, *Digital Signal Processing*, Prentice Hall, New Jersey, 1975.

[5] A. Leon-Garcia, *Probability and Random Processes for Electrical Engineering*, Addison-Wesley Publishing Company, Inc., 1994.

[6] Theo van de Roer, Microwave Electronic Devices, Chapman & Hall, London U.K, 1994.

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Appendix

Before taking the gain and phase measurements, the network analyzer needed to be calibrated with the power meter. The application circuit was disconnected from the setup for calibration. First, a power sweep calibration was done. The amplifier was not used in this procedure and Coupler 1 was hooked up directly to the RFout port of the network analyzer. Port R and A were connected to Coupler 1 as in Fig. 2. A power meter was connected to the D.U.T. side of Coupler 1. Under **Sweep type** in **Menu**, power sweep was selected. The highest possible dynamic range was used. For our case, CW frequency was set to 1.99 GHz. **Number of Points** in **Menu** and **Power Sweep Cal** were selected to be the same. Under **Power Sweep Cal**, a **Take One Sweep** calibration was performed.

The two channels on the network analyzer were calibrated to measure the gain/phase and output power. Channel 2 was set up to measure output power by selecting under **Measure**, port-B. Knowing the attenuation of Coupler 2, output powers were found. These measurements were compared with the absolute power read from the power meter. Input powers were recovered by subtracting the corresponding gain from the output power levels. To calibrate Channel 1 for gain and phase measurements, a S21 response-thru calibration was performed.

A New 3 Volt, Single Bias, High Efficiency Power Amplifier Product Family

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Abstract

ITT GTC has developed a new line of GaAs single bias 3 Volt RF IC power amplifiers (PAs) that utilize the TSSOP-16 surface mount plastic package. With the market pressures on today's wireless communications products for low cost, small size and long battery life, OEMs are forced to constantly push the limits of PA technology in both performance and packaging.

In addition to requiring higher efficiency PAs at lower supply voltages, the amplifiers must also operate from a single positive supply voltage. This constraint alone eliminates the need for a negative voltage generator in the traditional "negative gate biased" amplifier. Ultimately, this will eliminate the excess cost and space in the final PCB design and layout phases of any wireless product development.

With ITT GTC's new single supply 3V PAs, various output power capabilities, ranging from 500mW to 1.2W can be achieved with power added efficiencies of better than 55%. The first applications targeted by these new products will cover the 890-940 MHz frequency band, including ISM and narrowband PCS, and the 1880-1900 MHz frequency band for DECT.

This paper provides an overview of the GaAs manufacturing process behind this RF IC PA product development and will discuss the key performance parameters of the resulting new products.

A 60 Watt Amplifier Using 48 Volt LDMOS Device Technology

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Abstract:
RF performance of an amplifier using a 4 cell 48 volt Silicon LDMOS (Lateral Diffusion MOSFET) device is described. The amplifier demonstrates greater than 15 Watts PEP (Peak Envelope Power) output power at an intermodulation distortion level of -30 dBc. In order to demonstrate power scaling capability, (4) 4 cell devices were cascaded in parallel. The amplifier resulting from this experiment demonstrated 15 dB of gain, 35 % drain efficiency, approximately 60 Watts PEP output power at an intermodulation distortion level of -30 dBc and greater than 28 Watts PEP output power at an intermodulation distortion level of -40 dBc.

I. Introduction

There are several advantages that 48 volt LDMOS device technology presents over its lower voltage counterparts. One of the principal benefits is that the power density of a given device is substantially increased for an equivalent die size from a lower voltage LDMOS device technology. The higher operating voltage also means that the device output impedance will be increased, which simplifies the design of the output matching network, as well as potentially increasing the bandwidth of operation. The total gate periphery of the device is 20 mm. There were three devices of interest, the topology of which was identical for all three devices. The difference between the three devices were several key process variables which were controlled during the fabrication of the devices.

II. Summary of Results

A summary of the DC parameters for a group of typical 4 cell 48 volt LDMOS devices is shown in Table 1. The controlled process variables appear to have the greatest impact on the value of Vds(on) .

BV_{DSS} (Volts)	$V_{DS(ON)}$ (Volts)	$V_{GS(th)}$ (Volts)	G_m (mS)
106	.450	3.46	340
114	.450	2.98	325
116	.500	3.17	315
120	.500	3.02	325
116	.550	3.37	325
115	.549	3.06	335

Table 1. Typical DC Parameters of 4 Cell 48 Volt LDMOS Devices

In order to determine the impact of the process variables on the RF power performance of the 48 volt LDMOS device, two tone measurements were performed. The device was tuned for peak power performance at the -30 dBc IMD point. The results of this measurement is shown in Fig. 1.

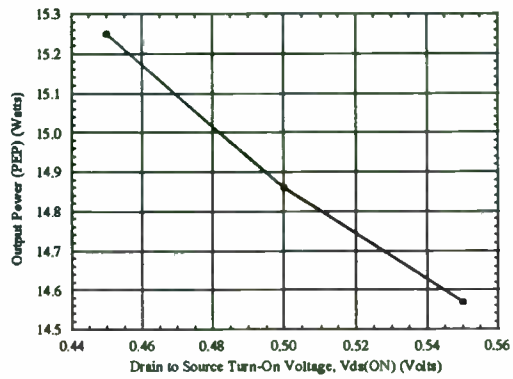

Fig. 1. Output Power (PEP) Performance versus Drain to Source Turn On Voltage

From the graph, it can be seen that the output power increases as the value of Vds(on) decreases, which is consistent with classical device theory. The output power shown is the peak envelope power (PEP), which denotes a two tone input power mode of operation. The tone spacing between the two tones for the measurements shown is 100 kHz. The frequency of operation is fo = 900 MHz and the quiescent bias conditions for the measurements shown were Vdd = 48 V and Idq = 75 mA.

Two tone ruggedness measurements were performed on the 4 cell 48 volt LDMOS devices, terminating the devices in an 8:1 VSWR load mismatch. The initial ruggedness measurement was made at the input power level that coincided with the operating point of the circuit, in this case at an input power of Pin = 150 mW. To obtain a complete set of ruggedness measurements, the input power was increased in 1 dB steps from this nominal operating point. At the completion of each incremental input power level, the device's DC parameters were re-measured. The device degradation point was determined to be the point at which the device's Vds(ON) increased by 5 %. The results showed that the device does not exhibit any significant performance degradation with an input power level up to 5 dB over the input power level that coincides with the nominal operating point.

Finite element thermal analysis was then performed on the 4 cell device, to obtain a better quantitative idea of what the overall thermal resistance of the package containing the device would be under normal operating conditions. The thermal analysis was performed using a package as shown in Fig. 2. The thermal analysis performed assumed a dissipated power of 14.1 Watts, based upon an average output power of 7.5 Watts, a power gain of 17.0 dB, a drain efficiency of 35 % and a package case temperature of 100 °C. The results obtained from this thermal analysis gave a device thermal resistance of 6.03 °C/W.

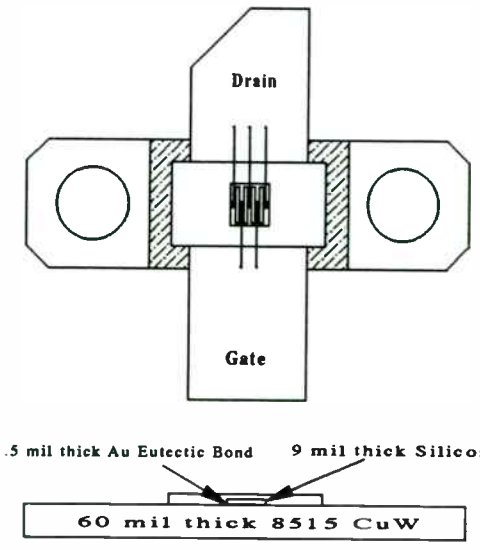

Fig. 2. 48 V LDMOS Device Mounted in Package, Showing Critical Dimensions

In order to achieve 60 Watts output power performance, (4) 4 cell 48 volt LDMOS die were mounted in parallel. To suppress potential odd mode oscillations, the gate to gate and drain to drain bond pads of each of the die were connected in a cascaded configuration, to assure that an equivalent voltage potential would exist across each device. Fig. 3 shows the drain efficiency, power gain and intermodulation distortion performance of the assembled circuit. The results obtained show approximately 60 Watts PEP at an intermodulation level of -30 dBc and greater than 28 Watts PEP at an intermodulation level of -40 dBc. For the measurements shown the frequency of operation is fo = 900 MHz and the quiescent bias conditions for the measurements shown were Vdd = 48 V and Idq = 250 mA.

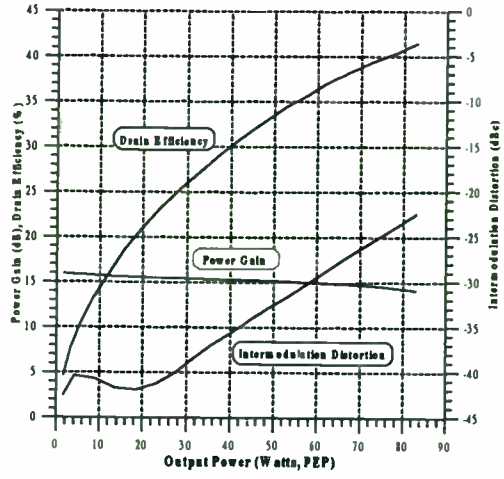

Fig. 3. RF Performance of (4) 4 Cell 48 Volt LDMOS Devices

Thermal analysis was then performed on the 16 cell 48 volt LDMOS device, to obtain a better quantitative idea of what the overall thermal resistance of the device would be under normal operating conditions. Thermal analysis was performed using a package with dimensions that were identical to that of the 4 cell device thermal analysis. The thermal analysis performed assumed a dissipated power of 56.5 Watts, based upon an average output power of 30 Watts, a power gain of 15.5 dB a drain efficiency of 35 % and a package case temperature of 100 °C. The results obtained from this thermal analysis gave a package thermal resistance of 1.85 °C/W .

The combination of the power dissipated by the device under normal operating conditions, coupled with its value of thermal resistance, may be high enough to result in a degradation in the RF performance of the device. One possible solution to reduce the thermal resistance of the package would be to reduce the

thickness of the device substrate. Another possible solution would be to reduce the thickness of the package flange substrate.

III. Conclusion

The feasibility of 48 volt LDMOS device technology was proven through the 4 cell device performance. To demonstrate power scaling capability, (4) 4 cell die were mounted in parallel in the engineering package and the RF performance was evaluated. The results obtained show excellent scaling in the output power performance, relative to the output power performance of the 4 cell device, with approximately 60 Watts PEP output power at an intermodulation level of -30 dBc and greater than 28 Watts PEP output power at an intermodulation level of -40 dBc. Thermal analysis was performed on this package to obtain a better quantitative feel for the device's thermal resistance. The results indicate that additional improvement in the thermal performance will be necessary in order to use this as a production device. Several solutions were proposed to reduce the device's junction temperature. Both of the solutions presented have the net effect of reducing the overall thermal resistance.

S-Band 30 Watt Power GaAs MESFET For MMDS Application

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*California Eastern Laboratories
**NEC Corporation

ABSTRACT

A new microwave high power GaAs FET for the MMDS (Multi-point, Multi-Channel Distribution Systems) wireless cable TV market has been developed. The NES2527B-30 is a 30 watt GaAs FET device with partial internal matching designed specifically for the 2.5 - 2.7 GHz band. In this band, the device exhibits the following broad band performance: 32 W typical P_{-1dB}, 12 dB typical gain, -48 dBc typical IM3 at 33 dBm each tone (39 dBm PEP), and 40 % typical power-added efficiency. The transistor is biased at 40 % Idss; i.e. Vds = 10 V and Idq = 6.0 A.

I. INTRODUCTION

This paper describes the design process of the NES2527B-30, a 30 watts S-band class A power GaAs MESFET device. It presents the design methodology and the practical modeling techniques utilized in this design. The performance of nine devices from two wafers is presented and a comparison is made between measured and simulated results.

II. BACKGROUND

Design Goals

The goal was to design a linear GaAs power FET that would deliver 30 watt of output power at one dB Gain Compression (P_{-1dB}) across the 2.1 - 2.7 GHz band, with an associated gain (G_{-1dB}) of over 10.5 dB, and low distortion. The device needed to be biased in class A or class AB (30% to 40% Idss) to meet the linearity requirements. The instantaneous band width of the FET needed to be at least 200 MHz within the above specified band. Finally, existing processes and manufacturing capabilities had to be used, and, because the target market for this device is commercial broadcast, the cost had to be minimized.

Design Challenges

In designing a power transistor, the main challenge is always to transform, with minimum loss, the very low impedances at the plane of the chip to larger and closer to 50 Ω impedances at the lead of the device. The existing NEC S-band power GaAs FET chips delivered about 18 watts of P_{-1dB}. So, to design a 30 watt S-band device, two of these chips had to be utilized. This further complicated the design because power splitting/combining issues had to be considered.

Another challenge is the lack of 2-port models for such large chips that could accurately predict large signal performance. The main parameters needed for the design are the FET chip's input and output large signal impedances, its gain, and its P_{-1dB} across the frequency band of interest.

III. DESIGN CONSIDERATIONS

Before starting the design of this device, some measurements were performed to generate simple practical models of the FET chip and the other components used in the design.

FET Chip Model

One port input and output models of the FET chip were created similar to those presented in [1] and [2]. An elementary FET chip section (a cell with 5.28 mm gate periphery which represents 1/8th of the full chip) was mounted on a carrier and its input and output terminals were matched to 50 Ω source and load impedances at 2.7 GHz by bonding its gate and drain pads to single section transmission line quarter-wave transformers. Quarter-wave length transformers of various impedances were available for this use, and based on the particular ones used the input and output large signal impedances of the elementary FET at 2.7 GHz were de-imbedded.

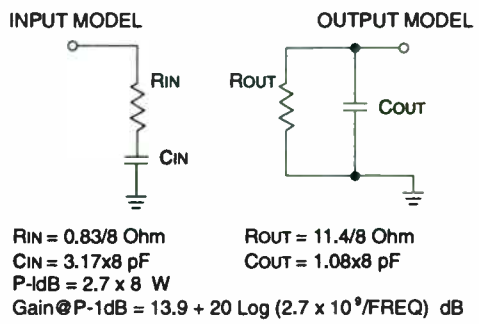
These de-imbedded impedances were:
Zin = 0.83 - j18.6 (Ω)
Zout = 10.9 - j2.0 (Ω)

From these impedances, two element large signal impedance models for the input and output were created: a series RC model for the input and a shunt RC model for the output. See figure 1. This type of simplified model can be used for broad band design with satisfactory results.

Additionally the output power (P_{-1dB}), the gain (G_{-1dB}), and the power-added efficiency (P.A.E.) at one dB gain compression of this elementary cell at 2.7 GHz were noted to be 2.7 watts, 13.9 dB, and 47.8% respectively.

To get a model of the full FET chip which consisted of 8 cells, the input and output impedances, as well as the P_{-1dB}, were scaled and then the P_{-1dB} was assumed to be constant and the gain was assumed to follow a -6.0 dB per octave slope with frequency. With these measurements and assumptions, a practical model of the FET chip was obtained that could be used in the simulation of the design and the estimation of the performance for this device. This model is shown in figure 1.

Figure 1. Large Signal Simple Chip Model.



Component Models

Next, models were created for the internal matching components such as the transmission line substrate/combiner, the chip capacitors, and the bond wires. For the substrate/combiner, an EM simulation software was used to calculate the 3-port S-parameters. The EM simulation software can give S-parameters for odd shaped transmission line circuits that are otherwise unavailable from circuit element libraries of traditional transmission line simulators. For the capacitors, a resonance technique was used to measure the Q at 2.7 GHz. Having an accurate value for the losses at the operating frequencies is crucial in estimating the gain and the gain slope of the device. Finally, a simple series RL model was used for the bond wires.

Pre-Matched Versus Fully Matched Device

Because this device was targeted for operation in the 2.1 - 2.7 GHz frequency band, due to size and cost constraints it was not possible to internally match its input and output impedances to 50 Ω at the device leads. Instead, the FET chip's input and output ports were prematched internally to impedances at the device's leads that could then be easily transformed to 50 Ω by the use of different external matching circuits for different applications in the 2.1 - 2.7 GHz frequency band. Such a philosophy led to a wide band and robust design.

Package

Traditionally, GaAs FET packages use metal side-walls for eliminating resonance structures near the device's operating frequencies. Also, such packages usually have 50 Ω feed-throughs for the leads. A package with metalized ceramic side-walls and low impedance feed-throughs was used for this device. The metalized ceramic side-walls are less costly than their metal counterparts but still achieve the desired cutoff and shielding characteristics at these frequencies. The low impedance feed-through reduces the impedance transformation Q for pre-matched devices thus improving the performance and band width of the device. For the feed-throughs, models based on their physical structures were created to be used in the design and simulation of the device.

IV. DEVICE DESIGN

The design of the device was carried out in the HP MDS environment. The device consisted of two FET chips, each with a gate periphery of 42 mm, and input and output internal matching circuits (IMN) that partially transformed the FET chip's input and output port impedances to impedances that could then be easily transformed to 50 ohms with external matching circuits. Because the FET chip model was based on one-port models, the input and output sides of the device were designed separately.

Input Design

The input IMN was designed in the 2.1 - 2.7 GHz band such that it would compensate for the -6 dB per octave gain slope that is inherent in the FET chip, thus achieving a flat gain capability for the device. The input IMN consisted of a two section low pass LC type structure and the low impedance feed-through. Bond wires were used for the inductors and high dielectric custom chip capacitors were used for the capacitors. To simulate the gain available from the FET chip, the 13.9 dB G_{1dB} at 2.7 GHz obtained from the one-cell measurements was used and a -6.0 dB gain slope per octave was assumed. The values of the capacitors and inductors were then optimized within size and manufacturability constraints to obtain an input loss profile that would result in a flat gain capability.

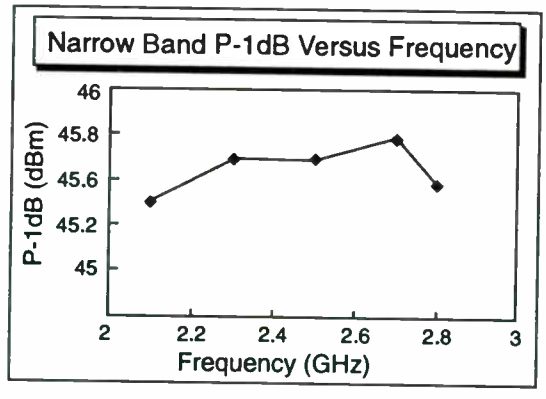
Output Design

The output IMN was designed in the 2.1 - 2.7 GHz band such that it would minimize the losses of the output match, present the optimal load impedance for power, and achieve the widest band width possible. The output IMN also consisted of a two section low pass LC type structure and the low impedance feed-through. For the first section, bond wires and high dielectric custom chip capacitors were used. For the second section, an alumina substrate with transmission line and open stub patterns was used. This substrate also performed the function of combining the two chips. The S-parameters of this 3-port substrate were calculated by using the Momentum EM simulation software and then checked to ensure good phase and amplitude balance. The value of the inductor and capacitor, and the pattern of the alumina substrate were optimized to minimize loss and optimize band width.

V. ASSEMBLY AND EXPERIMENTATION

The designed components and the package were procured and several devices were then assembled according to the design. Because of the complexity of the design and the difficulty in predicting the actual inductance of bond wires once the device is assembled, some experimentation with the internal matching network, especially the bond wires, was necessary. In deciding how to modify or tune the assembled devices, the following methodology was used. First, each device was mounted in a break-apart amplifier circuit where the input and output external circuit impedances could be measured with a Network Analyzer. The external input and output circuits were then tuned for optimum narrow band performance at 2.1, 2.3, 2.5, 2.7, and 2.8 GHz respectively, and then the optimum large signal load and source impedances for each of these frequencies were measured. These impedances were then compared to the impedance values predicted by the models and simulation results and the IMN modified to get optimum load and source impedances closer to the modeled values. This process was carried out iteratively until the measurement results agreed with the modeled results. All these measurements were carried out in a high power automated test system presented in [3]. Figure 2 shows the optimum narrow band RF performance results.

Figure 2. Narrow Band Optimum P_{-1dB} & G_{-1dB}.



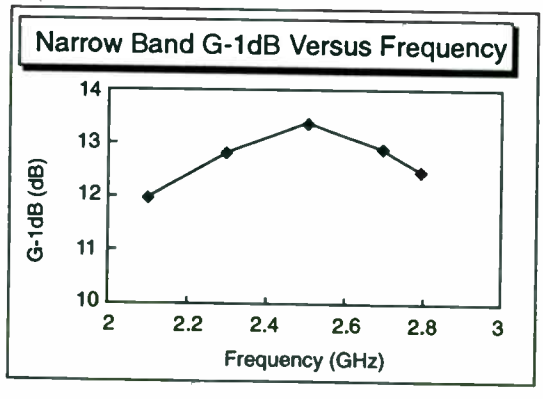


Figure 3. Input & Output Impedances & Losses.

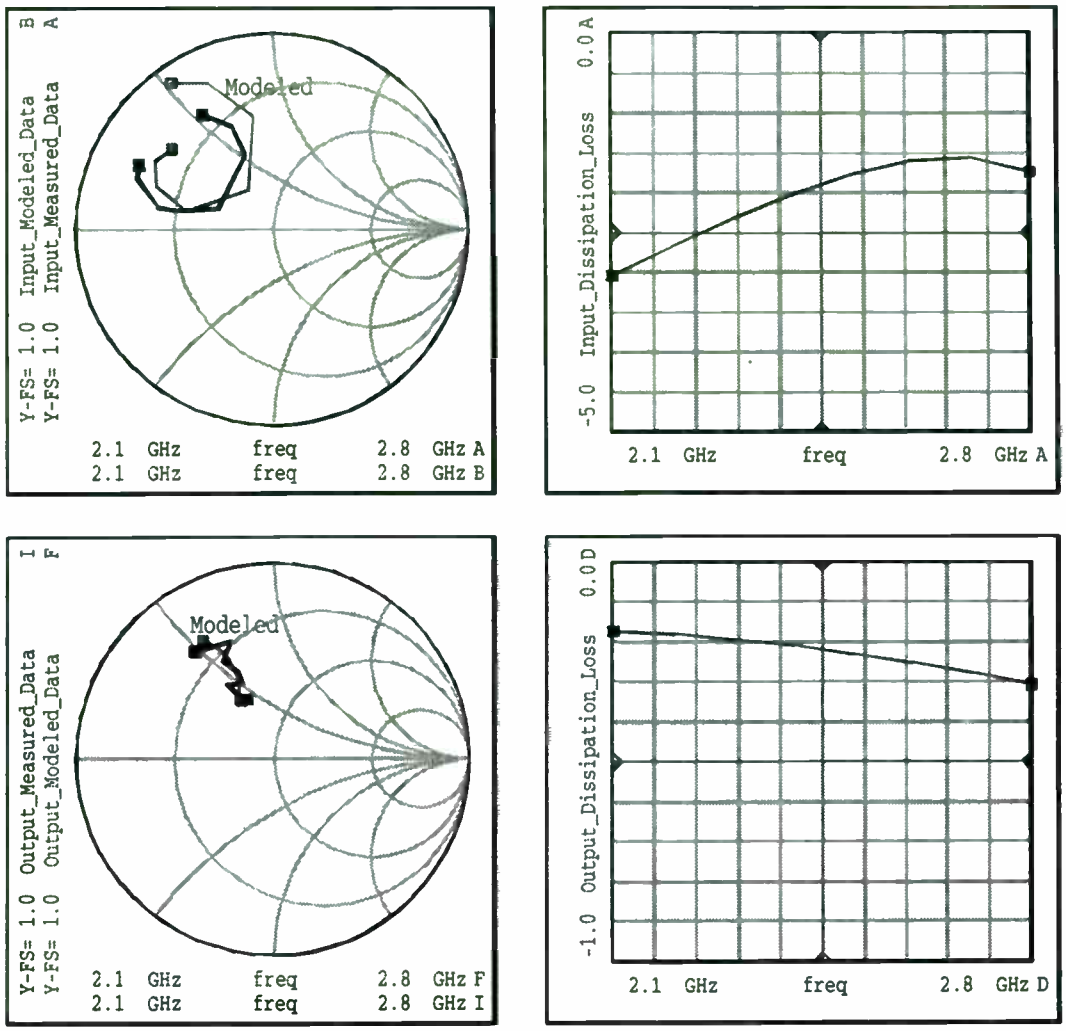


Figure 4. RF Test Fixture (2.4 - 2.8 GHz).

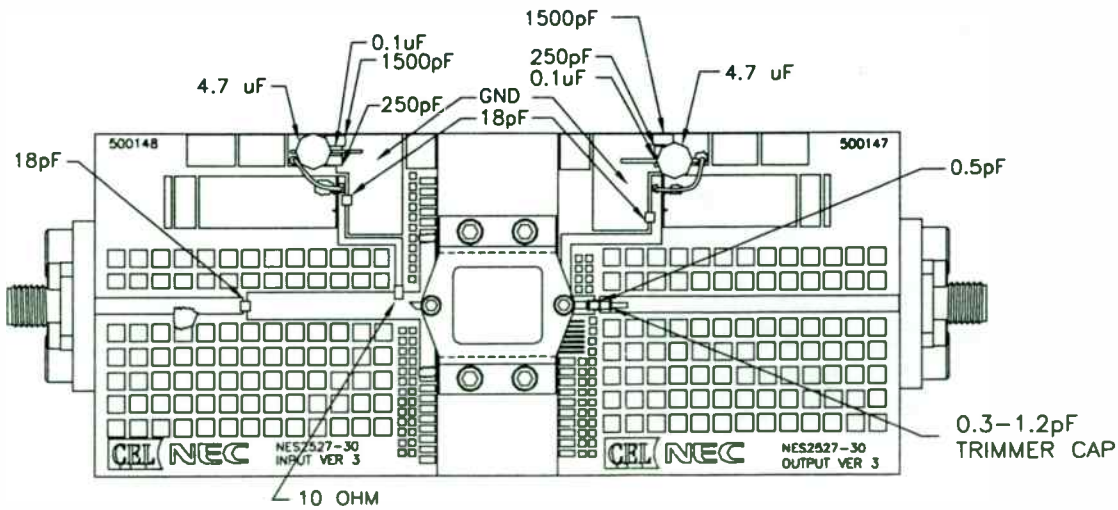


Figure 3 shows the input and output large signal impedance and dissipation loss modeled results for the device. Figure 3 also shows the measured optimum input and output large signal impedances. As can be seen, for the output side the agreement between modeled and measured optimum large signal impedances is very good. For the input side, the agreement between modeled and measured optimum large signal impedances is satisfactory.

VI. MEASUREMENT RESULTS

Once good agreement between the measured and modeled impedances was achieved and the performance of the device satisfied the design goals, the experimentation with the IMN and assembly was concluded and the device design was complete. The next step was to design a broad band amplifier. Since the 2.5 - 2.7 GHz band is the most commonly used and is at the high frequency end of this device's capability, a broad band amplifier was built based on the optimum large signal input and output impedance values. This amplifier covered 2.4 - 2.8 GHz. Figure 4 shows a drawing of this amplifier.

Figure 5.

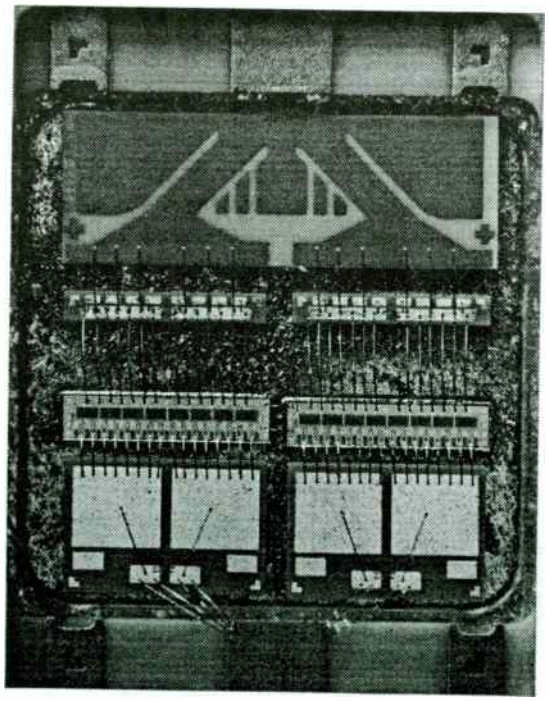


Figure 5 shows a picture of the device. Nine such devices from 2 different wafers were assembled and RF tested in this amplifier circuit. There was no any additional tuning performed on either the devices or the amplifier. The broad band test results are shown in figure 6. The results show 45 dBm typical P_{-1dB}, 12 dB typical G_{-1dB}, -48 dBc typical IM3 at 33 dBm each tone (39 dBm PEP), and 40 % typical P.A.E. The transistor was biased at 40 % Idss; i.e. Vds = 10 V and Idq = 6.0 A.

Thermal Characteristics

The device channel-to-case thermal impedance (R_{th}) is 1.3 K/W typical and 1.5 K/W maximum measured at I_{DS} = 6.0 A, V_{DS} = 10 V, and T_{flange} = 25 °C. At T_{flange} = 62 °C, the maximum R_{th} is 1.66 K/W.

At 1 dB Gain Compression operating condition, the dissipated power (P_{DISS}) is given by the following formula:

$$P_{DISS} = P_{-1dB}(1 - 1/G_{-1dB})(1/\eta_{add} - 1) \qquad (1)$$

With: P_{-1dB} = 31.6 W typical
G_{-1dB} = 15.9 typical
η_{add} = 0.40 typical
these give:
P_{DISS} = 44.4 W typical

For this case, the maximum channel-to-flange temperature rise at 1 dB Gain Compression then is:

$\Delta T = 1.66 \times 44.4 = 73.7$ °C

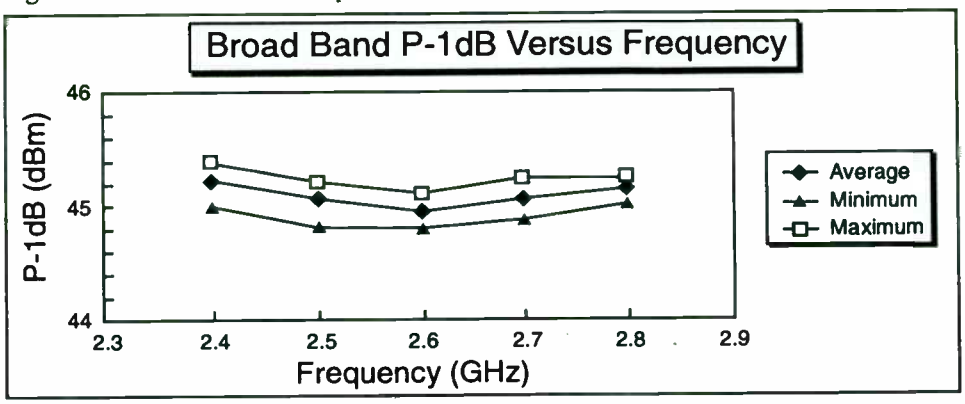
For a flange temperature of 88 °C and at 1 dB Gain Compression the MTTF of the device is expected to be more than 10^6 hrs.

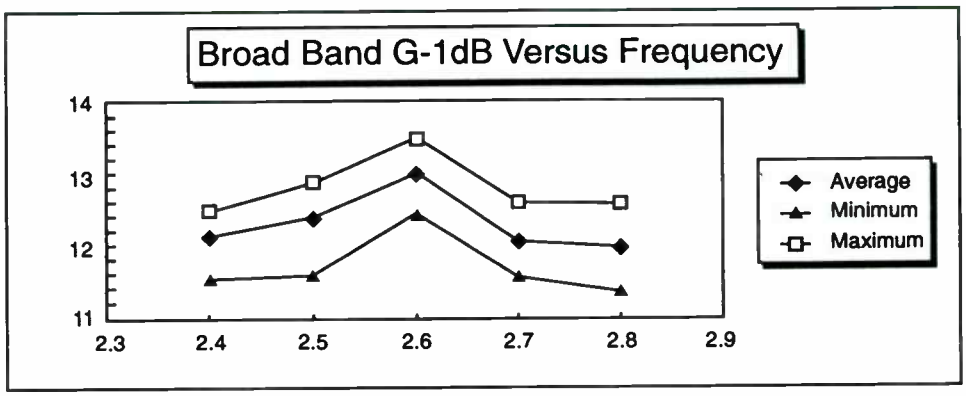
The worst case scenario occurs when the device is biased and the RF power is turned off or is at a very low level. In this case:

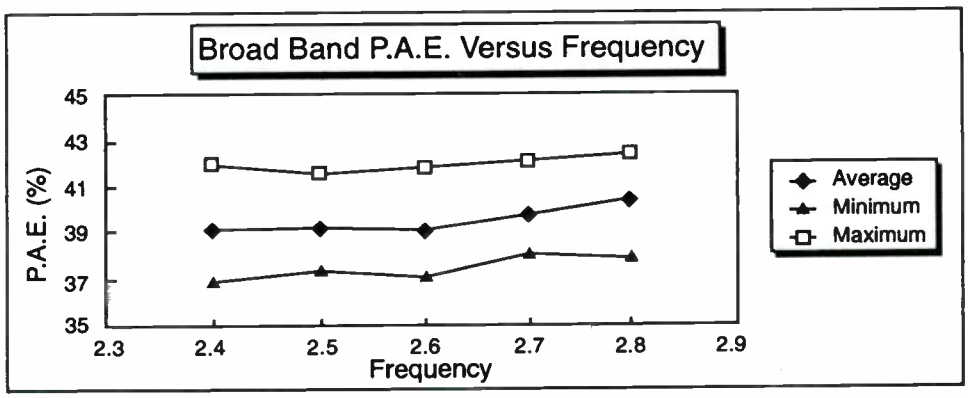
$P_{DISS} = I_{DQ} \times V_{DS} = 6.0 \times 10.0 = 60$ W
$\Delta T = 1.66 \times 60 = 99.6$ °C maximum

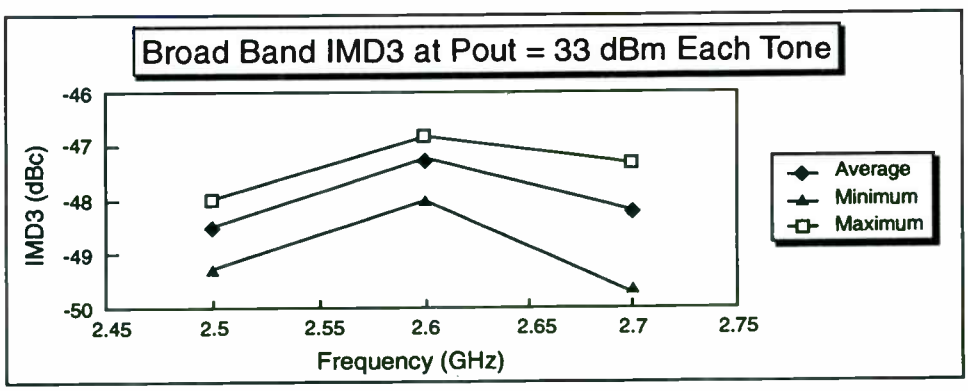
Under such operating conditions at a flange temperature of 62 °C, the MTTF of the device is expected to be more than 10^6 hrs.

Figure 6. RF Performance Graphs.









VI. CONCLUSION

A 30 watt S-band partially matched linear GaAs FET device has been designed for the MMDS transmitter amplifier application. Practical modeling techniques were utilized in the design and simulation of this device. Experimental techniques were used to adjust assembly parameters such that close agreement was obtained between the modeled and actual optimum large signal impedance values. Nine devices with FET chips from two different wafers were assembled and tested. The results showed that this device delivers state-of-the-art performance in terms of P-1dB, gain, linearity, and band width.

VII. ACKNOWLEDGMENTS

The authors are grateful to H. Hirayama for initial development support at NEC, to M. Hart for testing these devices, and to D. Newman for assembling these complex parts.

VIII. REFERENCES

[1] M. Avasarala, D.S. Day, B. Kraemer, and R. Basset, "High Power GaAs FETs And Drop-In Amplifiers For C & X-Band", Microwave Journal, February 1989.

[2] R. Basset, B. Kraemer, and D. Day, "10-Watt, MBE GaAs FET Power Amplifier", Applied Microwave, Summer 1992.

[3] R. Basset, D. Raicu, G. Sarkissian, and D. Phelps, "Automated Test Equipment For High Power Solid State Device Development And Characterization", 47th ARFTG Conference Digest, Spring 1996.

1/2-Watts, η> 40% PHEMT MMIC Power Amplifier for VSAT, Satcom and Wireless Communications

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Abstract

A high-efficiency 14 GHz GaAs PHEMT MMIC power amplifier has been developed for emerging market in VSAT, Satcom, and other wireless communications. Operation of the MMIC requires a +7V DC supply and a negative DC supply. The MMIC achieves a linear power gain of more than 20 dB, and a typical RF output power of 27.5 dBm with an overall power added efficiency of greater than 40%.

I. Introduction

The emerging applications of VSAT, Satcom, and other wireless communication applications at 14 GHz requires a 1/2 watts power amplifier with a power added efficiency of greater than 40%. This paper discusses the design approach and presents the measured results of a GaAs PHEMT MMIC power amplifier operating at 14 GHz with a high-efficiency.

II. Design Approach

To obtain maximum output power and high power efficiency, the Litton power PHEMT technology is chosen. The averaged maximum transconductance (Gm_{max}) of the PHEMT is 450mS/mm and the maximum saturation drain current ($Idss_{max}$) is 550mA/mm. A 720 um device can deliver 1/2 Watt output power with a power added efficiency of 70% for class AB operation. In order to obtain an output power level of 27.5 dBm and optimum bias condition to achieve the required output power level at its best power added efficiency, a load pull device characterization has carefully been performed to obtain output load impedance. A load pull device characterization is done with of a tuner terminated at the output of the device, and tuner stubs are adjusted to obtain maximum output power. For a 720um device, the optimum power load resistance is about 6 ohm.

The functional schematic diagram is shown in Figure 1. The MMIC itself uses 0.25 um gate length technology and has 2 stages of amplification. The driver

stage and the output stage employ devices with gate widths of 240um and 720um respectively. The input impedance matches the input device to 50 ohm. The interstage impedance network matches the input of the second device to the output of the first device. The output impedance matches the output device to the optimum power load. The MMIC layout, shown in Figure 2, is 2.1mm x 0.9mm in size. It requires a Vdd of +7 V and a negative gate bias. A 240um first stage device was selected to provide the gain as well as the linearity to drive the output stage of a 720um device. This two stage MMIC power amplifier can provide a linear power gain of 17.5 dB, an output power @ 1 dB gain compression of greater than 27 dBm with power added efficiency of greater than 40 % and most importantly, this amplifier is unconditional stability. This MMIC chip requires a 7 volts of Vdd and an operating current of 200mA.

III. Measured Performance

The temperature dependence of P_{3dB} is as shown in Figure 3. It is found to be much better than our prediction. The plot of output power vs. input power is shown in Figure 4. The gain expansion is observed to be bias dependent. With a good combination of biasing currents in the first and second stages, we have been able to minimize the gain expansion commonly observed in a PHEMT MMICs. The tight distribution of gain from two wafers is shown in Figure 5. This demonstrates the insensitivity of the designed circuits to the process variation. The unexpected low value of the output power shown in the figure is attributed to the low value of I_{max} singular to these wafers. For a high I_{max} wafer, output power as high as 28dBm can be expected. This MMIC is tested to be unconditionally stable.

IV. Conclusion

We have demonstrated an MMIC design using Litton's power PHEMT technology to achieve a tightly distributed linear power gain and a temperature insensitive P_{3dB}. This MMIC is tested to be unconditionally stable. A typical RF output power of 27.5 dBm with power added efficiency of greater than 40% has been realized. With a higher I_{max} wafer, an output power of 28 dBm is expected.

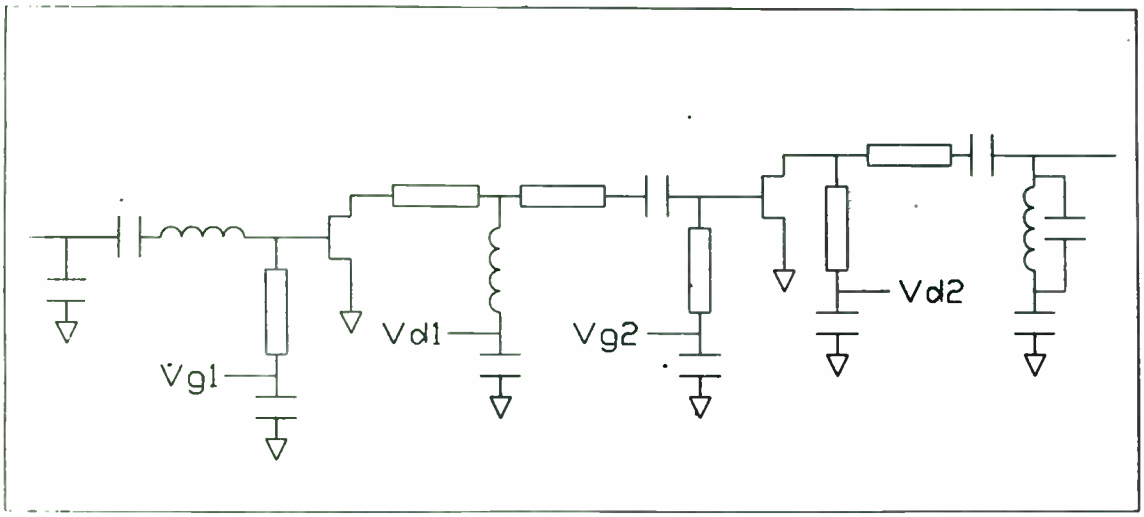

FIGURE 1. POWER AMPLIFIER SCHEMATIC

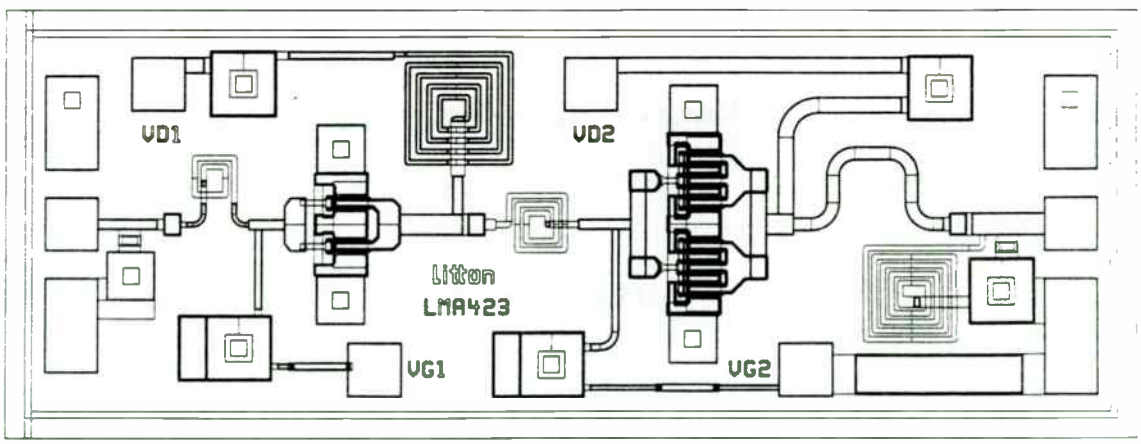

FIGURE 2. POWER AMPLIFIER LAYOUT

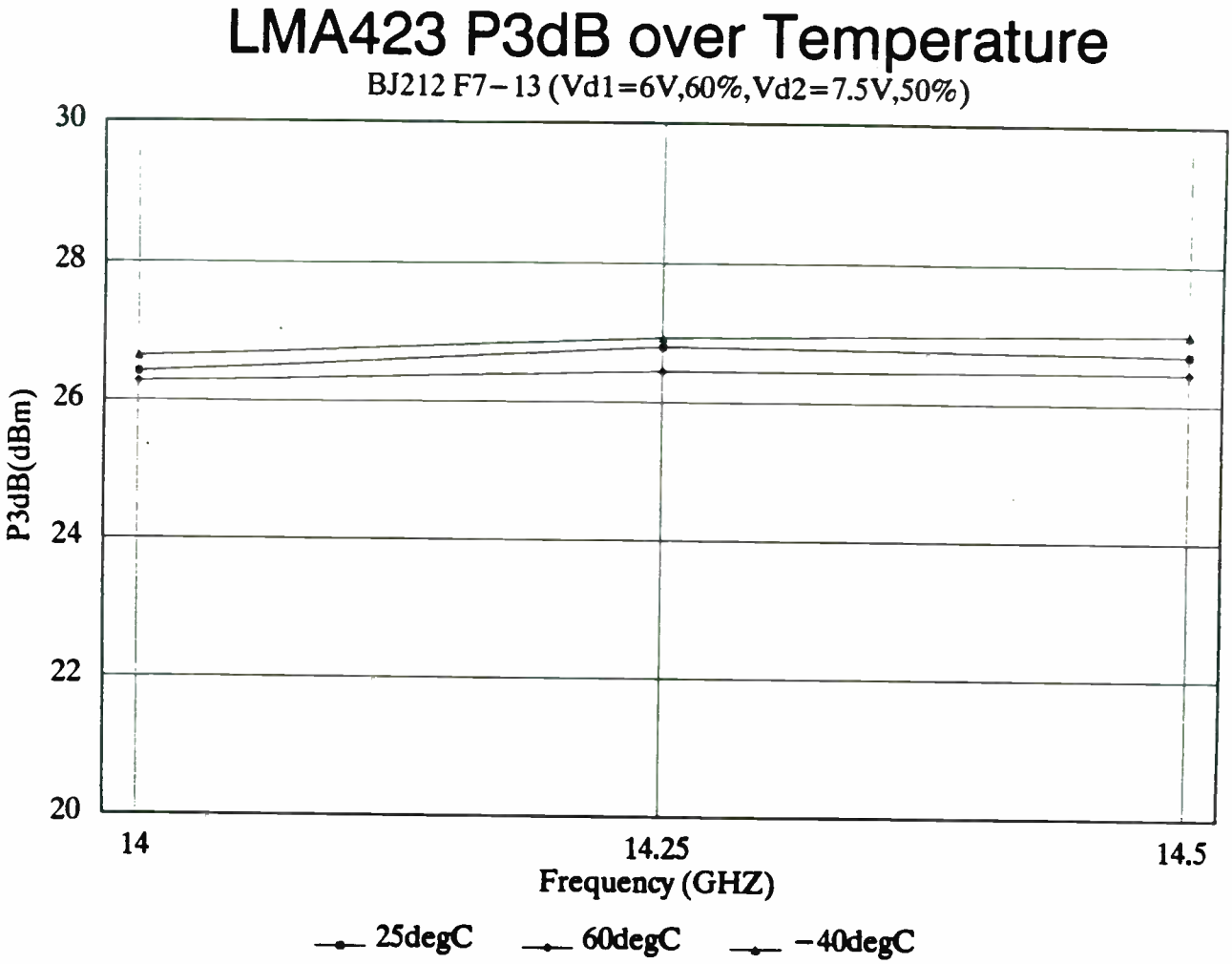

FIGURE 3. TEMPERATURE DEPENDENCE OF P_{3DB}

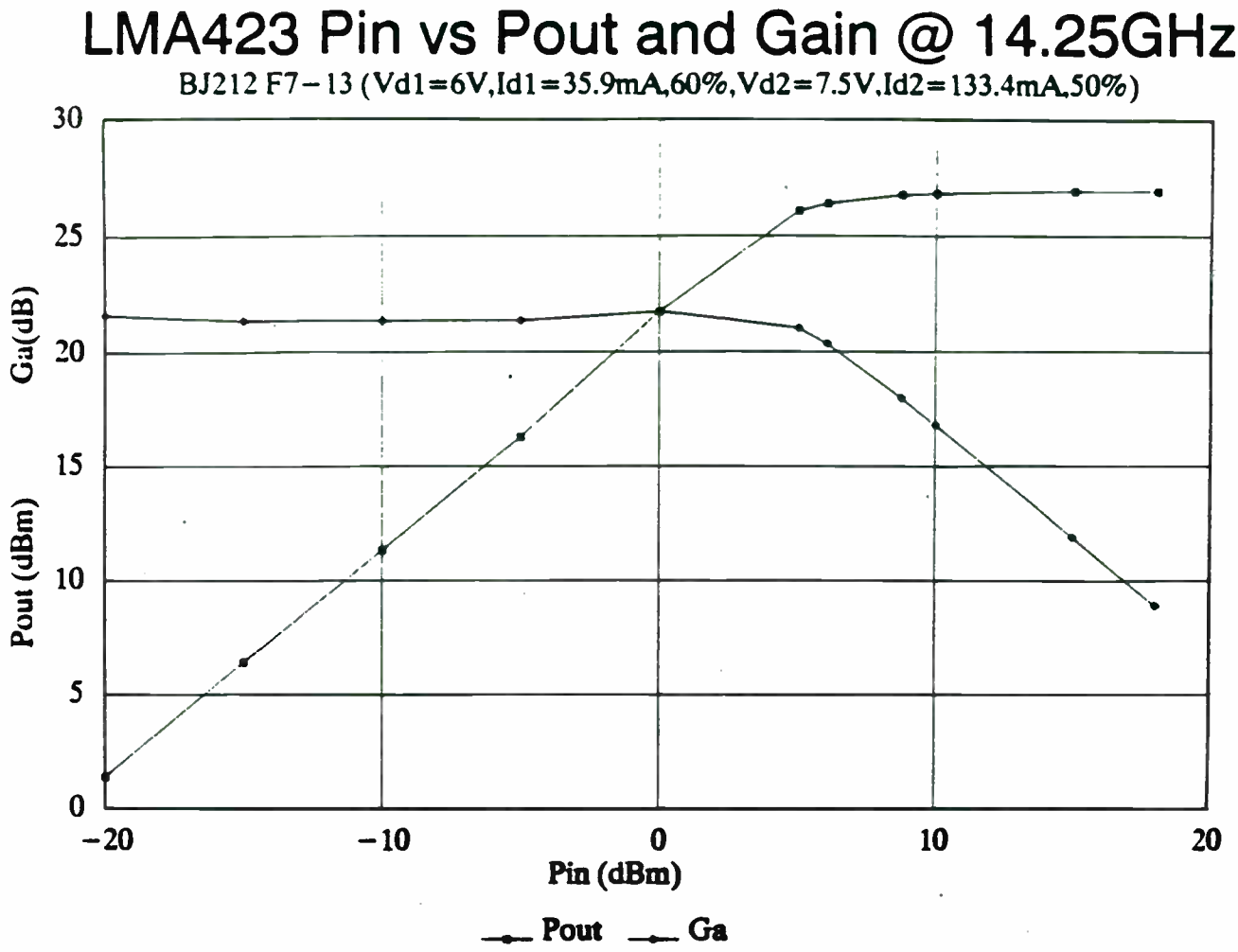

FIGURE 4. OUTPUT POWER VS. INPUT POWER

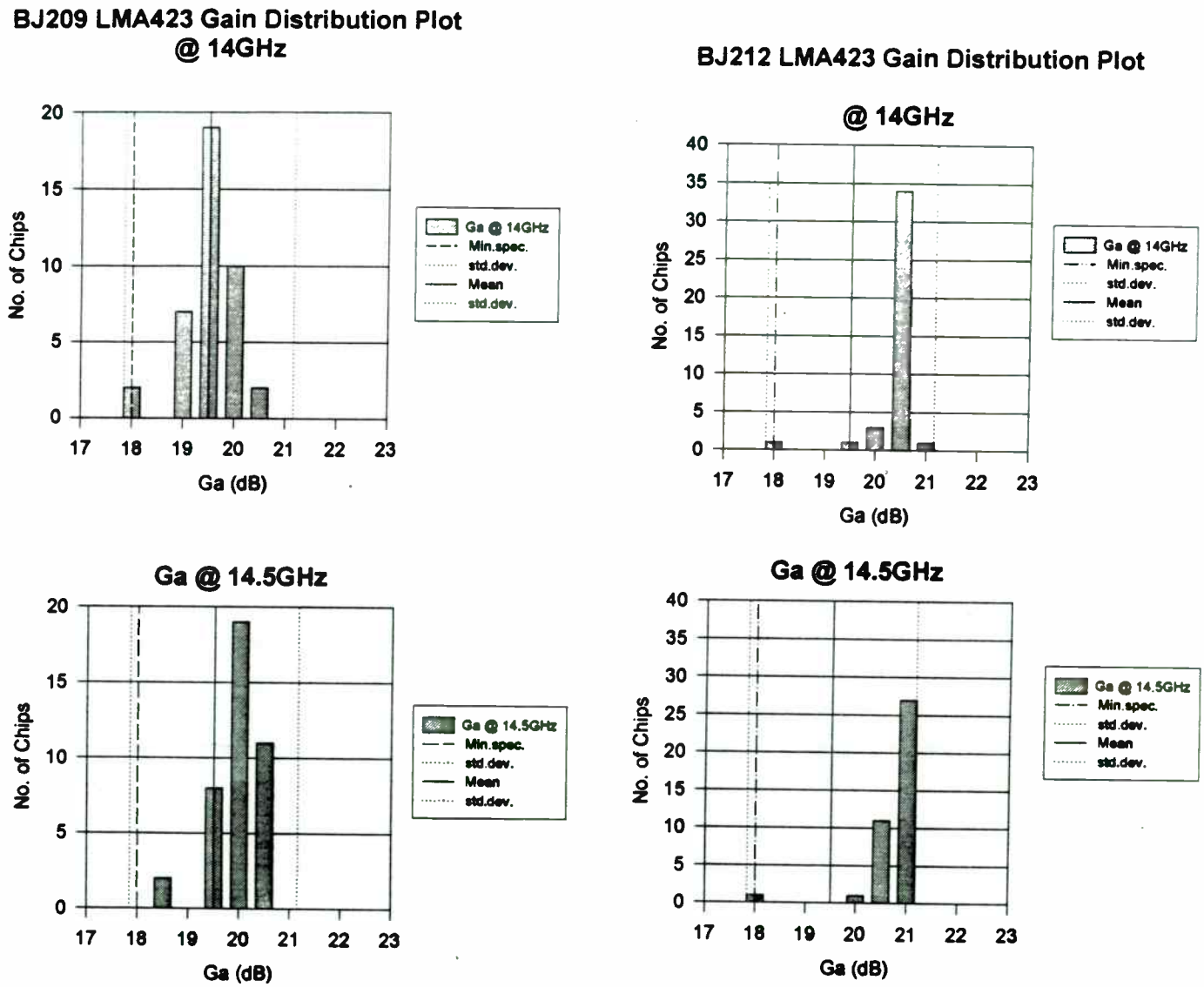

FIGURE 5. GAIN DISTRIBUTION OF THE POWER AMPLIFIER FROM TWO WAFERS

CELLULAR/CORDLESS DESIGN, II

Cellular/Cordless Design, II

Session Chairperson: Gaylene Phetteplace,
Motorola Semiconductor Products Sector (Tempe, AZ)

Off-the-Shelf 900 MHz Cordless Telephone System: System Overview and Baseband Design

By

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Introduction

As the 46/49 MHz cordless telephone technology has matured, there has been increased interest in a cordless phone with better performance over a longer distance in the consumer price range. This market is being addressed by the next generation of cordless phone technology in the 902 - 928 MHz frequency band. The application described here concentrates on an inexpensive, off-the-shelf solution. The modular approach both minimizes the design cycle and provides the flexibility to move to the 2.4 GHz as that technology becomes practical. The following paper will provide a brief, overall system description for a 900 MHz Analog FM Cordless Telephone using a Motorola chipset, and will include information on the design methodology used. We will then focus on the baseband section, discussing the use of the Motorola MC13110 Combo Chip to simplify the system design for a full featured secure telephone. Specific receiver, transmitter, and PLL design issues and performance will be discussed in separate papers.

System Description

This design features a 900 MHz transmitter and dual conversion receiver and complete baseband signal processing. RF transmit and receive frequencies, and first and second IF frequencies were all selected based on filter availability. The channel spacing chosen for this application is 320 kHz which allows for 10 channels within the given filter bandwidth and with an even division of the 10.24 MHz reference frequency. Narrower spacing may be used to increase the number of channels without using wider filters, however the wider channel spacing provides the fastest lock time and moves the reference spurs out on the PLL, in addition to better signal to noise ratio and receiver quieting with strong input levels. These features help provide a better quality telephone to the end customer and make use of the wider bandwidth allowed by the FCC in the 902 - 928 MHz band.

This chipset makes use of Motorola's MOSAIC™ 5, MOSAIC 1.5 and 75% BiCMOS process capabilities to achieve the maximum performance versus cost tradeoff. The receiver

consists of an MC13144 Low Noise Amplifier (LNA) with 17 dB of gain and a 1.4 dB noise figure at 900 MHz, the MC13142 LNA/Downconverter which is capable of another 14 dB of gain, and the MC13158 Downconverter and Limiting IF/Demodulator. For the transmitter, the MC13142 has been reconfigured to provide the 900 MHz oscillator which is directly modulated using a varactor. The mixer is then unbalanced by pulling one input to ground through a 1.8 kΩ resistor and it is used as an on chip power amplifier. Both the MC13144 and MC13142 are fabricated on Motorola's low noise MOSAIC 5 RF process, while the baseband IC is designed in BiCMOS to allow integration of the switched capacitor filters in the audio path and the digital control functions. The first LO frequency is high side injection to move it away from the US cellular frequency band, and is controlled by Motorola's MC145220 Dual 1.1 GHz Phase Locked Loop (PLL). The MC13110 performs the baseband signal processing for both the transmit and receive as well as providing the LO for the MC13158 and the MC145220 reference frequency.

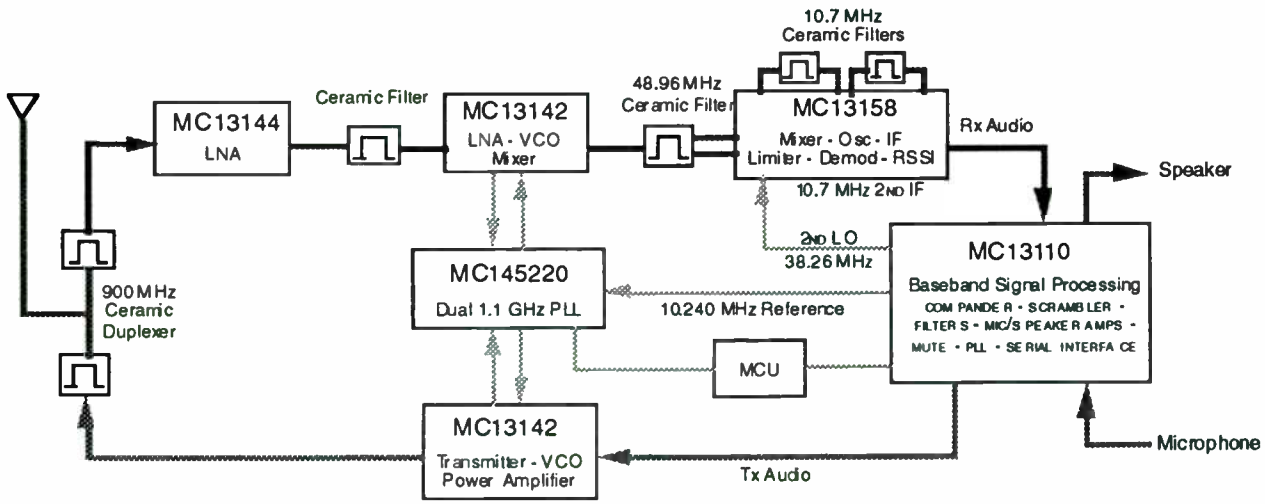

Figure 1. Simplified System Block Diagram

System performance of course depends largely on the passive components and filters used, however with the design described here we have achieved a sensitivity of -114 dBm (12 dB SINAD), < 1.5% distortion, and better than -70 dBm of image rejection with ±75 kHz deviation. This magnitude of performance requires careful matching, good layout and decoupling, and the use of high Q passive components (specified for 900 MHz design) in the RF section. Recommendations on external components and layout suggestions are included in each of the data sheets.

Key Specifications:

- f_{RF}
  - f_C (high band) = 926.24 MHz
  - f_C (low band) = 903.84 MHz
- Channel Spacing = 320 kHz
- IF1 = 48.96 MHz
- IF2 = 10.7 MHz
- f_{LO2} = 38.26 MHz
- BW_{RF} = 3.2 MHz
- f_{dev} = ± 100 kHz
- f_{ref} = 10.240 MHz

Channel Frequencies

Channel	Handset	Base
1	902.40	924.80
2	902.72	925.12
3	903.04	925.44
4	903.36	925.76
5	903.68	926.08
6	904.00	926.40
7	904.32	926.72
8	904.64	927.04
9	904.96	927.36
10	905.28	927.68

Figure 2. Key System Specifications

Design Methodology

This application circuit began as a compilation of various existing subcircuit boards into a full duplex, system level design. Careful attention has been paid to the layout and application circuit for each board, which provides a stable platform both to evaluate the individual blocks and to integrate each into a larger system. These boards are available for many of Motorola's RF integrated circuits and may be obtained through your local Motorola Sales Office.

The initial breadboard was used to demonstrate the capability of this chipset in a 900 MHz radio application, and to provide an opportunity to evaluate the performance of the individual devices and circuit blocks as well as to measure system specifications. Using this modular approach enables the user to quickly produce a 'tweakable' board. Each block can be debugged and modified independently which significantly simplifies the design. For test purposes, each RF block was initially matched on the input and output to 50 Ω. Note that although this board can be used to measure system parameters such as SINAD and THD, it is obviously not optimized for power consumption or space considerations. The second generation breadboard compressed the layout onto a single board and the match between RF blocks was optimized. The microcontroller interface for both breadboards was through a separate board which was programmed to operate the MC13110 and MC145220 in a demonstration/evaluation mode, as opposed to operating the system as a "real" telephone. The software is written for a Motorola 68HC05C8 microcontroller and is completely flexible. A menu system enables the user to easily tab through the most commonly used functions and all of the

registers for both ICs can also be programmed directly.

Baseband Circuit Design

The baseband processing is performed by the Motorola MC13110 Universal Cordless Telephone Subsystem IC with Scrambler. It interfaces with a microcontroller via a serial interface which provides digital control of key functions during system design, test and end use. This enables the overall system to be customized by the manufacturer during the design phase and can be used to tune the receiver electronically during production. The end user will have the ability to turn the scrambler on and off, mute the audio, and adjust the volume. MC13110 baseband processing functions include companding, scrambler, switched capacitor audio filtering, transmit path limiting, and variable transmit and receive path gain adjust. In addition, the on-board PLL provides a stable local oscillator for the MC13158 receiver second LO. A buffer circuit is used to drive the MC145220 reference from the MC13110 crystal oscillator. *This design requires only one crystal for the entire duplex, dual conversion system.*

The MC13110 was designed for use in 46/49 MHz narrowband FM cordless telephones. To achieve the bandwidths desired for the 900 MHz system, the FM receiver portion of the MC13110 was replaced with the MC13158 wideband FM IF. Although there is some duplication of function, the MC13110 still greatly simplifies the baseband design by integrating all of the necessary functions including the filtering into a single IC. Also, the first LO of the MC13110 is buffered out through the first mixer to be used as the second LO in the MC13158.

To disable the unused RF portion of the MC13110 without powering down the first mixer and LO, the input to the second mixer is tied to Vcc and the limiter input is tied to the adjacent decoupling pin. This is to prevent noise from the unused limiter from getting into the rest of the circuit. The RF Vcc line must still enabled so that the first mixer can be used to buffer out the LO frequency to the MC13158.

Scrambler

The MC13110 contains a frequency inversion scrambler which can be enabled/disabled through the serial interface. Included in the scrambler block are switched capacitor filters before and after a double balanced mixer. In the software written for this demo, the scrambler default is off to facilitate SINAD measurements. With the scrambler on, a 1 kHz test tone will be received as a 3 kHz signal which will be read as a harmonic distortion product in a typical test system. The scrambler modulation clock frequency is derived from the 10.24 MHz reference frequency. This block also includes the receive gain adjust and mute functions which are also micro controlled. Receive gain level is normally determined during the design phase and is not configurable by the user.

Switched Capacitor Filters

The internal digital filters in the MC13110 provide the equivalent of 6 poles of filtering with a corner frequency

of 3.5 kHz. To ensure a stable reference voltage for the filters, the Vag pin should be decoupled with 0.1µF. Inadequate decoupling may result in low frequency noise on the audio output.

Compander

Included in the compressor block are the automatic level control (ALC), transmit mute, limiter and gain adjust functions. The ALC provides a soft limit to the output signal without adding distortion, while the limiter circuit clips the peaks of rapidly changing signals. ALC, mute, limiter, and gain adjust functions are all programmable. The attack and decay measurements for the compressor and expandor as recommended by EIA/CCITT are given in the MC13110 data sheet.

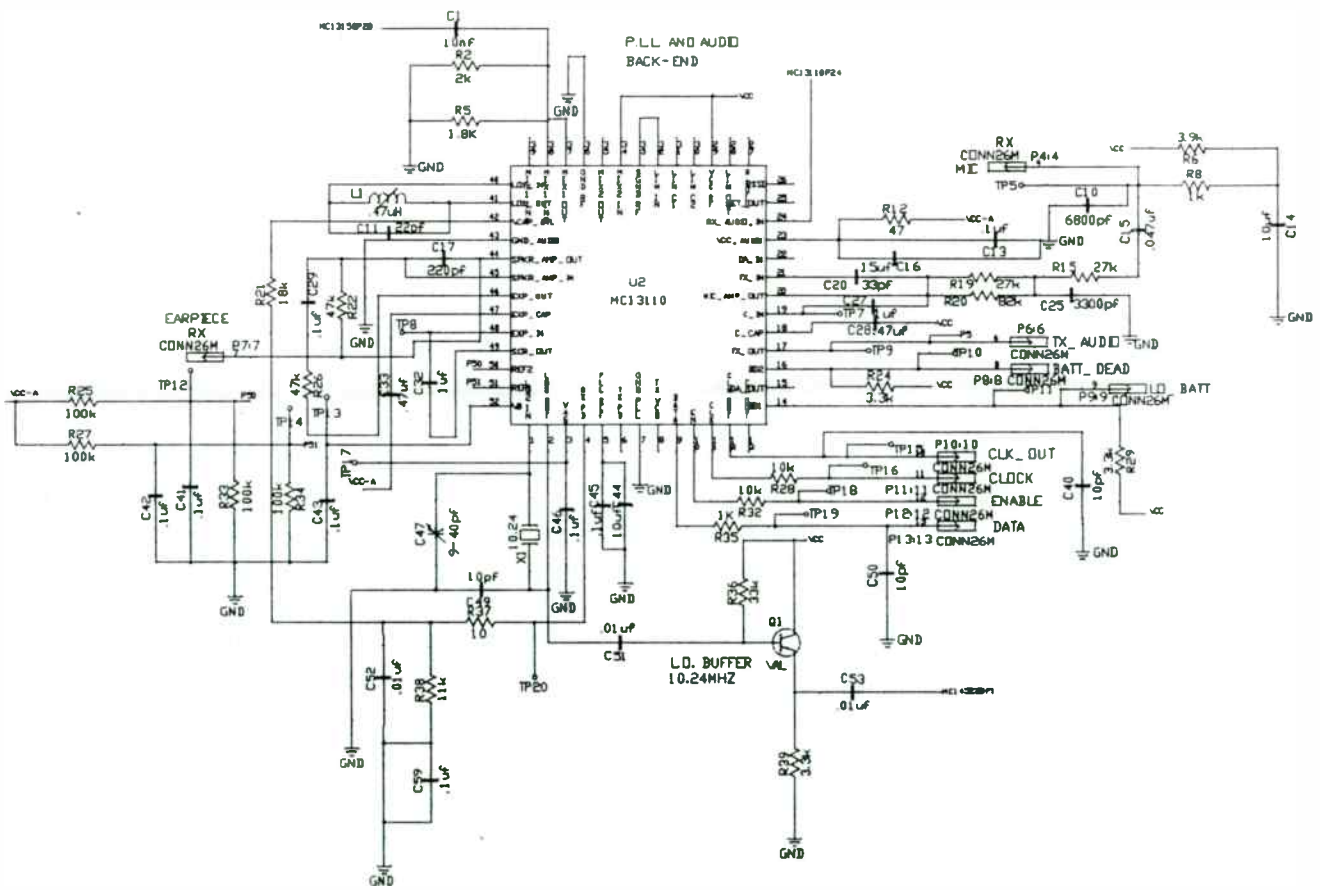

Figure 3. Baseband Application Ciruit

Mic Amp/Speaker Amp/ Volume Control

The mic amp and speaker amp use inverting, rail-to-rail operational amplifiers to make the best use of low voltage applications. The noninverting inputs are tied internally to the Vb reference which requires external decoupling. The receive volume can be programmed in 2 dB steps from -14 dB to +16dB.

Transmit/Receive PLL and 1st LO

The transmit PLL is not used in this applicatio. The TxPD pin should be allowed to float, but the TxVCO pin may be ac coupled to ground. The receive PLL is used to provide a stable LO for the MC13158 receiver without adding another crystal. The frequency reference for both PLLs is 10.24 MHz which is generated from a crystal controlled CMOS oscillator. Since this single oscillator is used not only as the reference for the 38.23 MHz LO, but also for the 900 MHz Dual PLL, it is extremely important that this reference is on frequency. A 2 kHz error at 10.24 MHz translates to a 200 kHz error on the receiver first LO and transmit frequencies. The reference frequency is adjustable by tuning C47. C47 and C49 must be increased if a crystal specified for a higher load capacitance is used.

Since there is no buffered LO out on the MC13110, we have configured the first mixer as an amplifier by imbalancing the inputs. The mixer output is then used to drive the MC13158 LO input. For additional LO level, the current in the mixer can be increased by adding a 2 kΩ resistor from the output to ground. The optimum LO level for the MC13158 is approximately -7 dBm. Too high or too low LO signal level will affect the receiver sensitivity.

Data Amp/RSSI and Carrier Detect

Both the MC13110 and the MC13158 are equipped with data slicers. The wider band MC13158 is capable of handling higher data rates if desired.

To use the carrier detect function in the MC13110, the RSSI must be brought in from the MC13158 RSSI output since the MC13110 receiver is disabled.

Additional Functions

The MC13110 also has two levels of battery monitoring with separate trip points and outputs, and programmable power .saving modes. However the IC must be in active or receive mode for the carrier detect to be functional.

Conclusion

This 900 MHz application is designed to be easily implemented and cost effective, yet includes all of the attributes of a high-end full-featured telephone.

Acknowledgements

MOSAIC™ is a trademark of Motorola Inc. The authors wish to thank the following people for their assistance on this project.

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Carey Johnson
Dennis Welty
Klaas Wortel

Off-the-Shelf 900 MHz Cordless Telephone System: MC13142 Transmitter Design

By

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INTRODUCTION

A key element of the cordless radio system is a low cost easily manufactured wide-band FM /FSK transmitter to complement the dual conversion receiver described in the preceding papers. Our choices were to use multiple discrete transistors, create a new TX I.C., or to reuse one of the existing receiver devices. The last option was selected as the most expedient and cost effective. The MC13142 down converter includes the basic elements needed plus it is easily repartitioned to reverse its basic functions. The LNA was used as the P.A.: the mixer as the driver/ isolation amplifier and the VCO with an added varactor diode became the modulated R.F. source. All objectives for performance as an I.S.M. band, Part 15 compliant transmitter were met.

TRANSMITTER REQUIREMENTS

The transmission system selected for this 900 MHz cordless telephone is simple wide-band Analog FM with a peak deviation of 75 kHz. Low distortion, less than 1% maximum THD was specified along with a >50dB "full quieting," i.e. strong signal to noise ratio. Power output was targeted to be a maximum of +3 dBm. This power generally gives adequate margin to overcome the transmitter duplexer filter loss and the losses of somewhat imperfect antennas. The actual power of this type of transmitter is expressed in a radiated field strength at a given distance. (50,000 µV/meter at 3 meters). If there is net positive antenna gain the transmitter power output must be reduced but the overall system will improve due to the increase in net receiver performance. Of course there will be a decrease in D.C. power which will extend the battery life.

The transmitter must also have an R.F. output for the P.L.L. tuning subsystem (MC145220). This must be accomplished while still providing for the audio modulation. Since the antenna, especially on the handset, is likely to have a widely changing S.W.R. the transmitter must be very stable into a less than

5 dB return loss load and have high internal isolation , 30 dB or more, to prevent the VCO from being pulled out-of-lock. Finally and most importantly, the transmitter must have very low residual noise in the receiver input passband to prevent "desense" in this simple full duplex (FDD) system. At twenty MHz from the transmit frequency the net noise floor including the transmitter filter/duplexer rejection must be greater than -125 dBc .

The MC13142 I.C.

The MC13142 is one of the latest core building block RFICs developed by the W.T.V. Operation at Motorola Semiconductors in Tempe Arizona. Originally targeted as a general purpose RF front end for a wide array of low cost commercial radio applications from 100 MHz to beyond 1 GHz, it has found a strong market in the emerging 900 MHz home cordless telephone market. The MC13142 is processed in the RF bipolar MOSAIC™ 5 process which produces IC NPN transistors that are similar in performance to the industry leader MRF941 type. The part is available in both a standard 16 pin SOIC and the 20 pin QFP package. When we designed the MC13142 flexibility was a key factor in both the circuit and layout. In particular keeping the LNA and VCO partitioned for external filtering and interconnection was done at the expense of some additional pins. Unlike many conventional RFICs the 13142 has all the DC bias and circuit convention of a standard Analog IC. Thus current drain and performance are essentially independent of supply voltage over more than a 2 to 1 range. On the other hand the oscillator is simple and discrete like allowing for conventional Colpitts or Clapp configurations as appropriate. A PLL buffer driver and complementary mixer outputs allow for up to three outputs. Data taken on the VCO phase-noise indicates a noise floor rivaling the best discrete transistors.

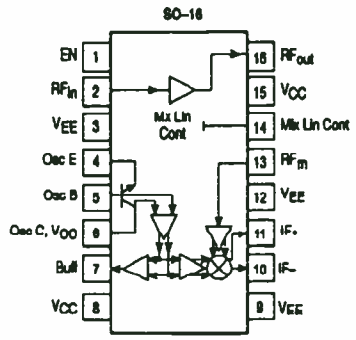

Figure 1. MC13142

AND FINALLY -- THE DESIGN

The LNA of the MC13142 was characterized for "large signal" operation. The amplifier, at 3 volts, had a 1 dB compression of -3 dB and hit hard limiting at +6 dBm. At +3 dBm output, our target power out, the gain was 12 dB. Minor changes in the output match were required as compared to the conventional small signal amplifier. A shunt 18 nH from Vcc to the output was followed by a series 27 nH inductor. This produced the optimum load line for the hard driven amplifier. The second harmonic was - 25 dBc.

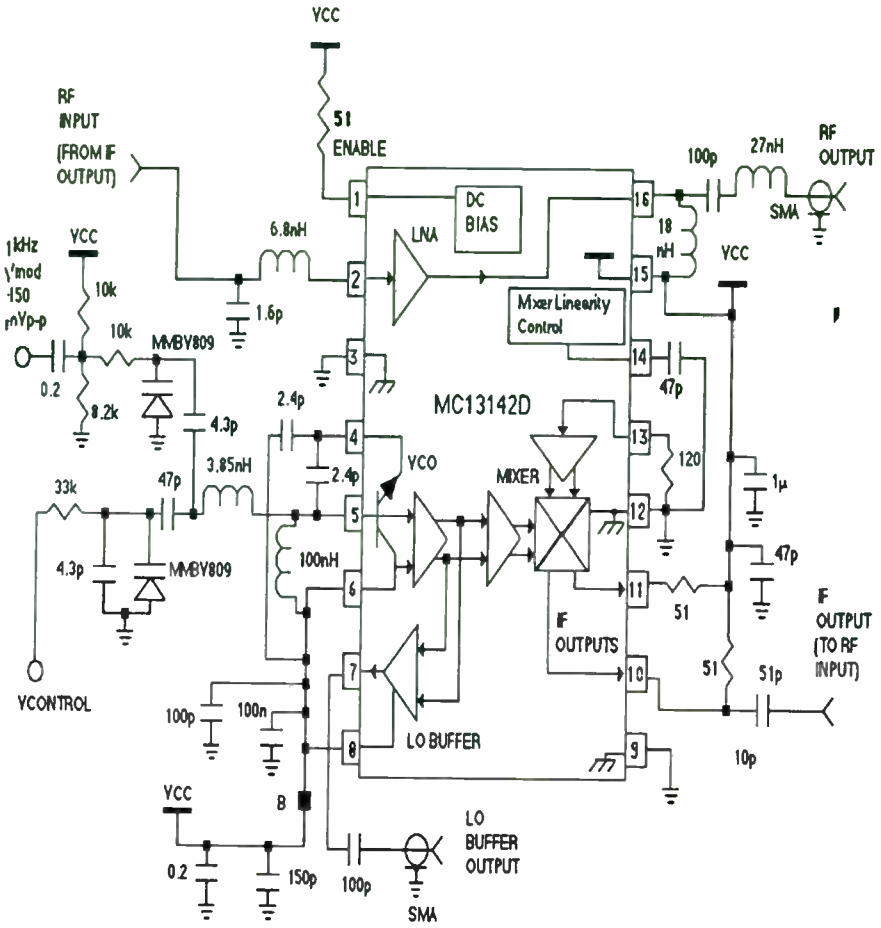

Figure 2. MC13142 Transmitter Application Circuit

To use the mixer as a VCO buffer amplifier, the normal RF in pin 13 was biased to DC ground using a 120 ohm resistor. This locks the mixer in an "on" amplifier mode. The I.F. output pins, 10 and 11 when matched, delivered more than - 3 dBm into 50 ohms. Since we needed only -10 dBm drive for the PA all matching could be eliminated. Simply terminating each output with a 51 ohm resistor and then coupling the pin 10 output to pin 2 the PA input with a blocking capacitor gave us a nominal TX output of +3 dBm.

The VCO required some special attention. For the basic tuning function a Clapp circuit configuration was selected. The tank circuit consists of a High Q 3.85 nH fixed inductor which resonates with the parallel combination of a 4.3 pF chip capacitor and the varactor tuning diode a MMBV809. The nominal bias point for this diode is 1 to 1.5 volts. This gives the transmitter a typical tuning range of +/- 75 MHz with a +/- 1/2 dB power output variation.

FM or FSK modulation is applied by using a second MMBV809 tuning diode loosely coupled to the primary tuning circuit through a 4.3 pF fixed capacitor. This diode is fixed biased to 1.5 volts and audio or data is applied through a large coupling capacitor. 150 mV p-p generates peak deviation of 75 to 80 kHz. Appropriate pre-emphasis is developed in the MC13110 audio baseband I.C.

Transmitter wideband noise is often a limiting factor in full duplex radio systems. Multiple filters and shielding are often required to prevent this noise from "desensing" the receiver. In this design the low noise VCO and amplifier running in the near linear mode reduce this noise to the point where little or no shielding is necessary and only one filter, the duplexer filter is required on the transmitter output. To prevent incidental wideband FM of the transmitter from the PLL clocks and other digital artifacts, the Vcc line to the transmitter must include low frequency (<10 MHz) decoupling. In this design a combination of a lossy ferrite bead and multiple parallel bypass capacitors cleaned up the DC supply from the co-located 900 MHz and second I.F. local oscillator PLL circuits. The Mixer Linearity pin 14 must also be bypassed to RF ground to prevent stray noise pick-up. Additional care MUST be used in routing of the VCO control and modulation input lines. The VCO control has a sensitivity of typically 10 MHz per volt . Any noise pickup here will result in an unwanted wideband noise floor increase and potential receiver sensitivity degradation. For testing purposes the transmitter has a simple enable control input to pin 1 which is normally connected to Vcc via a 51 ohm resistor.

Passive component selection at 900 MHz is quite different than what is used in the VHF bands. For the most part we recommend chip rather than leaded capacitors and resistors due to their parasitic inductance. Chip capacitors with high "Q" in the range of 100 or better are recommended for the VCO section. The inductors are quite critical for efficiency, stability and VCO noise. Coilcraft 0805HS are suggested for the matching and VCO resonator coils.

CONCLUSION

The MC13142 Down Converter turned out to be a relatively easy to convert into a simple easy to build low power 900 MHz FM transmitter. It is ideal, along with the MC145220 PLL, as a transmitter subsystem for 900 MHz cordless telephones that require low noise floors and a minimal external component count. It met the original target specs for power, modulation and spurious output. Other similar applications such as home TV links, simple RF tags, or wireless remote controls can be built effectively without the need for a huge investment in complex RF design and test facilities.

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"Off-the-Shelf" 900 MHz Cordless Telephone System: Wideband FM Receiver Design

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Abstract

The design, construction and evaluation of a wideband FM receiver in a low power full duplex cordless phone is discussed. It is implemented with "off the shelf" RF and baseband IF subsystem ICs and passive components on low cost FR4 printed circuit board. The receiver subsystem operates to 2.7 Vdc with the 1st and 2nd local oscillators controlled by PLL synthesizers referenced to a single low cost crystal clock. The receiver is isolated from the transmitter via a simple low cost duplex filter comprised of low cost ceramic filters and microstrip transmission lines.

Design criteria such as system noise figure, VCO phase noise and gain constant, loop filter bandwidth, IF filter bandwidth and quadrature detector tuning , and gain partitioning are discussed. SINAD performance, IIP3, receiver adjacent channel rejection, 1st and 2nd image rejection, reverse isolation and level of unintentional radiators are measured and compared to design goals.

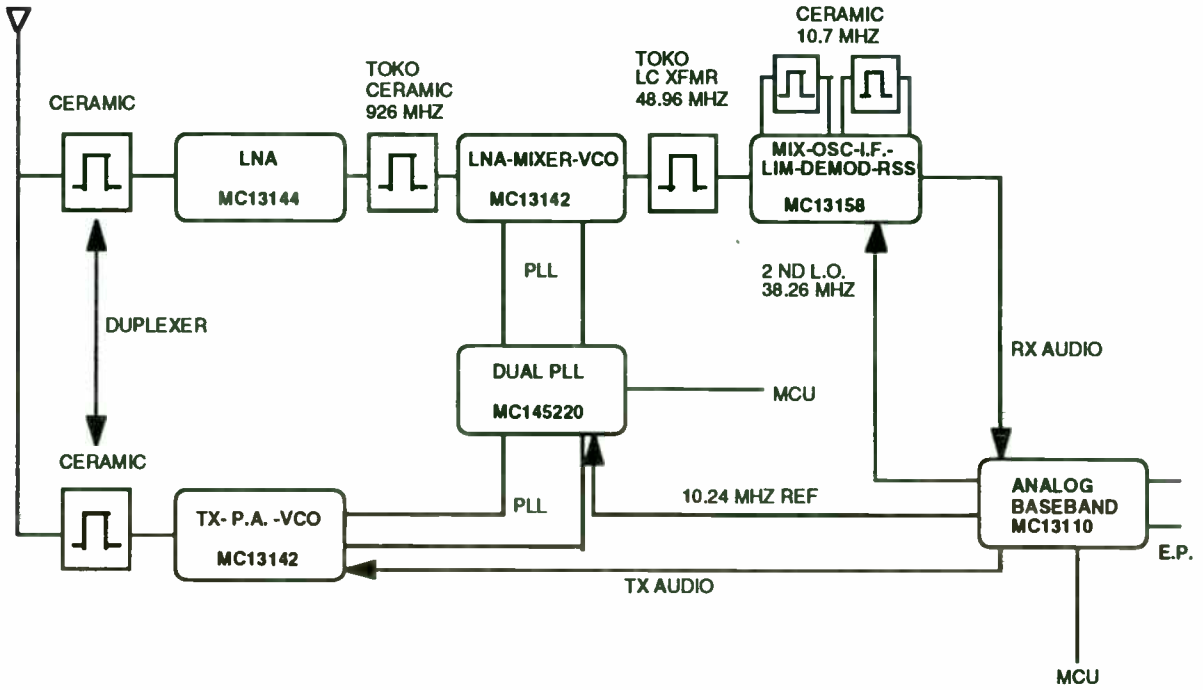
Basic layout criteria are discussed and examples are shown. A full duplex 900 MHz cordless phone demo is presented. Additional papers featuring the dual PLL synthesizer circuit design and programming, transmitter design concepts, baseband audio and system design are presented to complete the application and system design concepts of a unique 900 MHz cordless phone.

1. Introduction

This paper describes an analog wideband FM receiver designed for 902-928 MHz ISM Band Part 15 cordless phone applications [1]. The receiver is a full duplex dual conversion superheterodyne receiver incorporating a low cost silicon monolithic IC chip set which is comprised of 1) a low noise figure LNA IC, MC13144 [2], 2) an integrated LNA, Mixer and VCO RF front-end IC, MC13142 [3], 3) a single conversion, split IF and quadrature detector back-end WBFM IC, MC13158 [4], a baseband audio processor, MC13110 [5] and a Dual PLL Synthesizer MC145220 [6]. Design techniques to optimize the receiver sensitivity and noise performance are analyzed and developed. Tradeoffs in signal handling and power management are discussed. Surface mount components, small size PCB layout and few external components allow fabrication of a receiver suitable for portable applications. Performance is verified in a 900 MHz demonstration transceiver pair that represents a full duplex cordless phone handset and base station.

Figure 1 shows the simplified block diagram of the "Off-the-Shelf" 900 MHz Cordless Phone System. The receiver topology is specifically selected to implement a 10 channel 902 - 928 MHz cordless phone but it may also be utilized in similar wireless communications applications such as PC to PC and PC peripheral wireless data links, WLAN and security systems.

Figure 1 - "Off-the-Shelf" 900 MHz Cordless Phone System Block Diagram



2. Description of Chip Set

2.1 Front-end Receiver ICs

The MC13144 is intended to be used as the first low noise amplifier (LNA). It features a programmable, low noise, high gain RF amplifier having excellent linearity while maintaining low current consumption.
Figure 2 shows the pin connections in the 8 pin SOIC package. Features include:

* Low Noise Figure at 1.4 dB
* High Gain Associated with NF of 17 dB
* Low Power Operation at 3 V & 4.2 mA
* Programmable Bias with 2 Bit Logic Control

The MC13142D is used as the second LNA, voltage controlled oscillator and down converter. The circuit consists of a low noise amplifier (LNA), a voltage controlled oscillator (VCO), a buffered oscillator output, a doubly balanced mixer, a wideband IF amplifier and a dc control section. The wideband IF amp allows this IC to also be used as an exciter amplifier in the transmitter.

Figure 3 shows the MC13142 pin connections in the16 pin SOIC package. A pin is provided for linearity adjustment of the mixer; the input intercept point may be increased up to +20 dBm. Other features include:

* Low Power Operation : 13 mA at V_{CC}= 2.7 - 6.5 Vdc
* High Mixer Linearity: Input IP3 = + 3.0 dBm
* Single - Ended 50 Ω Mixer Input
* Double Balanced Mixer Operation
* Open Collector Mixer Output
* Single Transistor Oscillator with Collector, Base and Emitter Pinned Out
* Buffered Oscillator Outputs
* Mixer and Oscillator Can Be Enabled Independently

Figure 2 - MC13144D Pin Connections

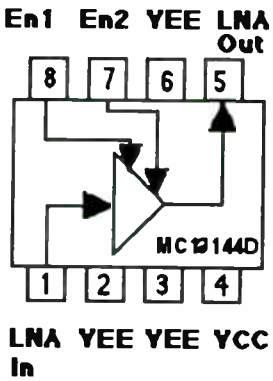
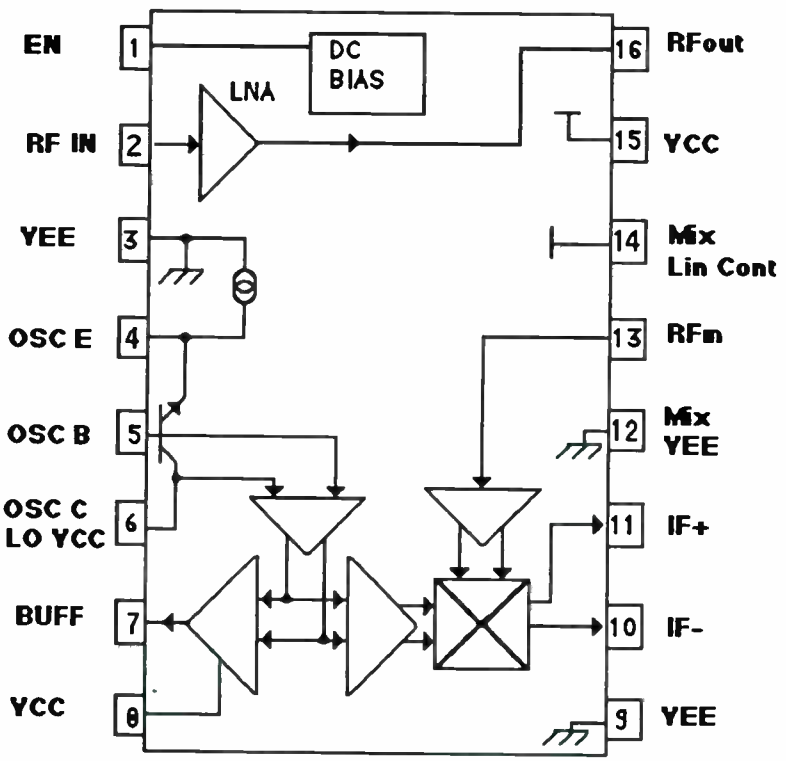


Figure 3 - MC13142D Pin Connections



2.2 Back-end Receiver IC

The MC13158 is designed for use as the back-end in analog wideband FM systems such as 900 MHz cordless phones and data links with data rates up to 1 Mbps. The MC13158 is a low power, single conversion, wideband FM receiver incorporating a split IF. It is comprised of a doubly balanced mixer, common collector transistor oscillator, received signal strength indicator (RSSI), RSSI buffer, IF amplifier, limiting IF, and quadrature detector and a device enable function (Refer to Figure 4, Simplified Block Diagram and Pin Connections).

The following are key features of this unique IC:

* Linear Wideband Quadrature Detector
* Split IF to Accommodate Low Cost IF Filters
* Low Current at 6.5 mAdc at 2.3 to 6.5 Vdc
* 70 dB RSSI Dynamic Range
* 12 dB SINAD Sensitivity = -100 dBm
* Available in 32 Pin TQFP Package

The MC13158 data sheet contains details on the IC description and applications. The MC145220 Dual PLL Synthesizer is used to control the first VCO in the receiver and the transmitter VCO. The MC13110 is used as the Baseband Audio Processor, Second Local Oscillator and Reference Oscillator.

Figure 4 - MC13158FTB Block Diagram and Pin Connections

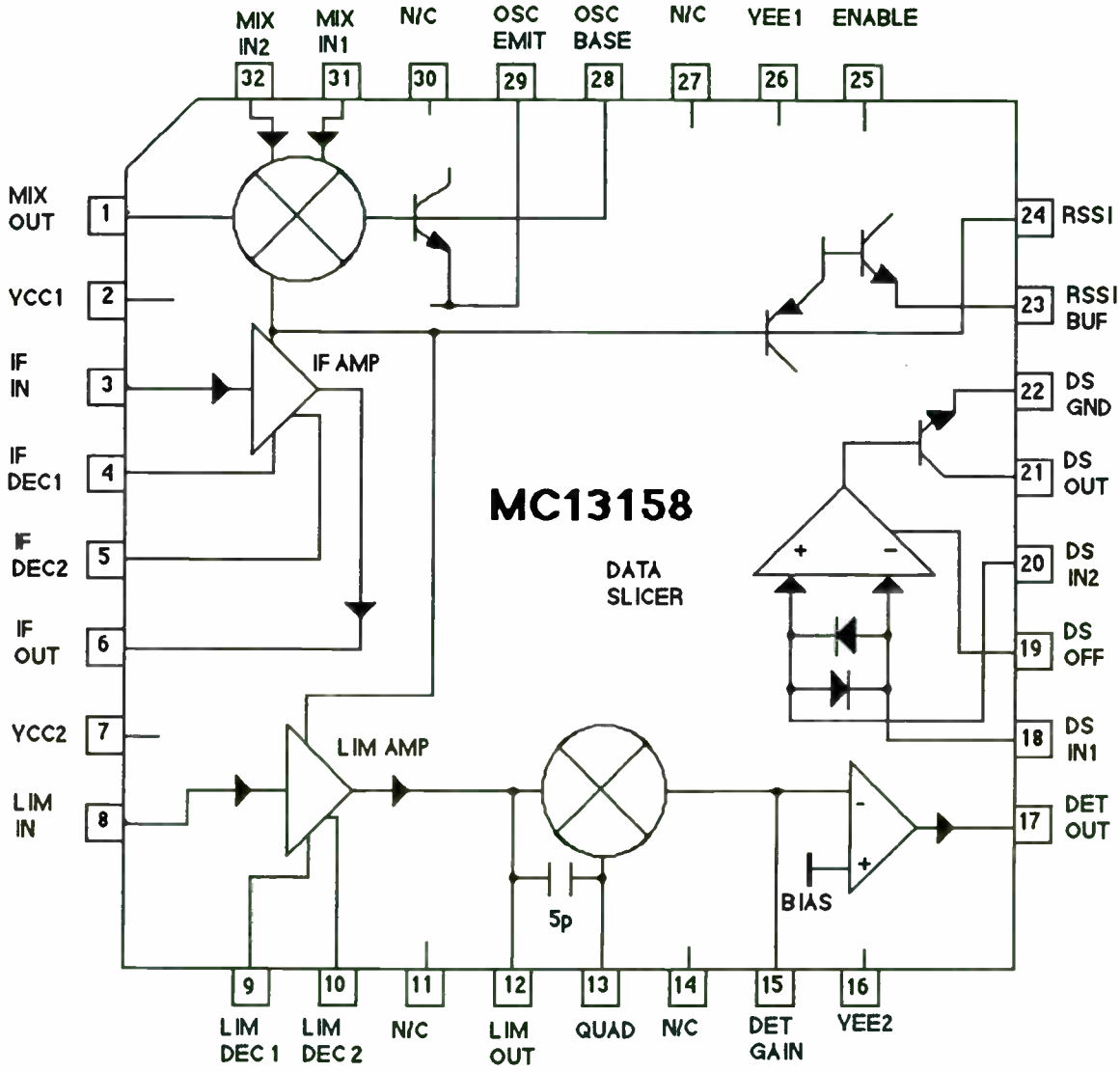
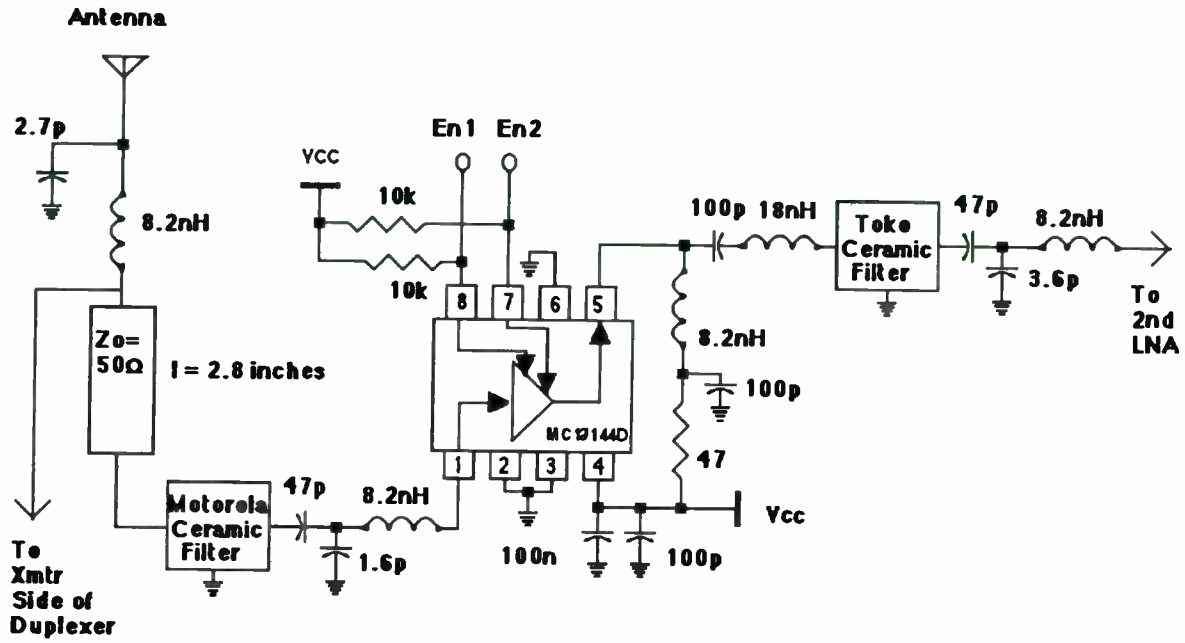
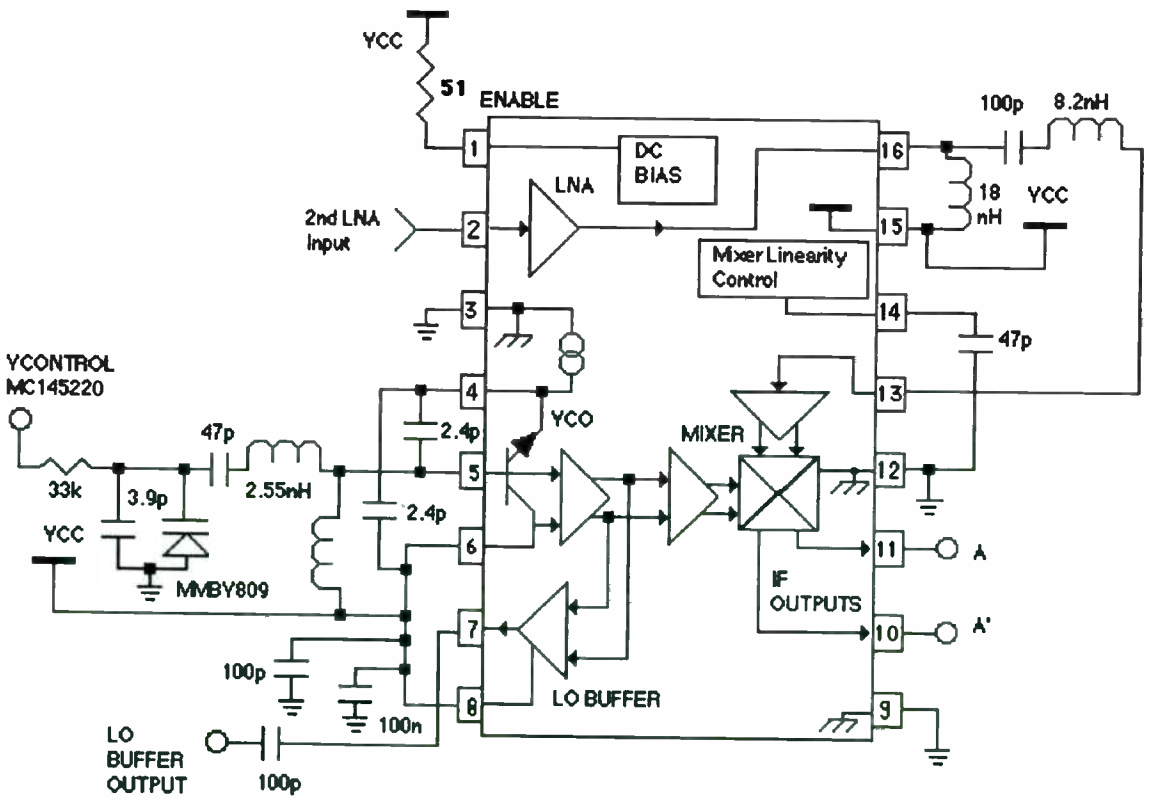


Figure 5 - 902 - 928 MHz Receiver System Front-end Section





3. Receiver System Design

3.1 Receiver Front-end

Figure 5 , Circuit Schematic of the receiver front-end shows the implementation of a low noise, high gain LNA (MC13144D) before the MC13142 to improve sensitivity. A detailed noise analysis supports this conclusion.

The front-end receiver circuit is comprised of the receiver side of the duplexer, the 1st LNA and the 2nd LNA, 1st mixer and VCO. The LNA matching networks are optimized for noise figure, gain and input VSWR. Small signal scattering parameters are found in the IC data sheet.

3.1.1. Antenna and Duplexer

The duplexer provides the necessary isolation of the transmitter from the receiver in the full duplex operation of a cordless phone. The duplexer's job is to appreciably attenuate the transmitter signal in the passband of the receiver so that the transmitter does not desense the receiver. Ideally, the antenna impedance should be 50 ohms at its interface to the duplexer. However, since it is generally not 50 ohms; a concerted effort must be made to match to the duplexer. The antenna design is critical to the optimal performance of the system.

3.1.2. Image Filter

RF ceramic filters are used before and after the 1st LNA to provide image rejection. A variety of filters - SAW, ceramic and dielectric are offered by many manufacturers such as Toko, Motorola, and Murata. The ceramic filters are the most appealing solution when weighing performance and cost. Both Toko (Part # 4DFA-926A-11 at 926.5 MHz & Part # 4DFA-904A-10 at 904.5 Mhz [7]) and Motorola (Part # KFF6140A at 904.5 MHz & Part # KFF6141A at 926.5 MHz [8]) make ceramic filters for 902-928 MHz Part 15 applications. The above filters have 3 dB bandwidths of 2 to 3 MHz, typical insertion loss of 3.5 dB and image frequency notches at 22 MHz from the center frequency. Filters having lower insertion loss (<2 dB), and an image frequency notch further out are under development; these provide the optimal solution design for a dual conversion receiver in which the 1st IF is in the 70 to 75 MHz range.

3.1.3. 1st LNA

The MC13144 LNA noise figure is typically 1.5 dB in a conjugately matched configuration. Matching the LNA input to the output of the receiver side duplex filter requires a simple series L, shunt C network; the 47 pF capacitor is used as a dc blocking component to enhance reliability of the filter by removing the bias. The ouput matching network optimizes the gain and provides a stable interface to the 2nd RF ceramic filter.
A unique feature is the ability to select a proper bias condition based on the dynamic needs of the system. In the cordless receiver, the bias on the cascode amplifier is set for the optimal noise figure performance at 4.2 mA (see IC data sheet) [2].

3.1.4. 2nd LNA/1st Mixer

The 2nd LNA matching is similar to the 1st LNA. Input matching uses the same topology but slightly different values; the output is matched to the mixer which has an input impedance of 50 ohms.

A unique double balanced class AB mixer employs a linearity control function in which the mixer can be biased for an input third order intercept point (IIP3) of up to +20 dBm. This not particularly needed in a cordless telephone application so the control pin is simply bypassed to ground with a 47 pF.

The mixer IF outputs are open collector and must be externally biased. The optimal external load impedance is 2 to 4 kohm. The mixer narrowband gain is about 5 dB. The mixer IF output frequency response is about 2.4 GHz.

3.1.5. Front-end Receiver Performance

1) Overall gain of the 1st and 2nd LNA (filter loss included) is typically 26 dB.

2) Noise Figure typically 2.5 dB at 3 Vdc.

3) Reverse Isolation of the 1st LO at the antenna port < -60 dBm (FCC required).

4) Unintentional radiation from the antenna or off the board < -60 dBm.

3.1.6. 1st Local Oscillator

The 1st Local Oscillator is PLL controlled with a MC145220 dual PPL synthesizer. The MC13142 has an on-board transistor with the emitter base and collector pinned out . Figure 6 shows the VCO circuit which uses a common collector configuration. The following equation is used to calculate the center frequency of the varactor controlled oscillator at a nominal 2 volt control voltage:

$$f_{osc} = 0.159 \{L' [(C1C2/(C1+C2)) + C_p]\}^{-1/2}$$

where

C_p is the parasitic capacitance of the IC and PCB layout; C_p is typically 4 pF.

$L' = L - (1/\omega^2) (C_V+C_B)/ C_V C_B$

The sensitivity may be adjusted by changing CB; if CB >> Cv, then Cv dominates and the VCO sensitivity is maximized; thus,

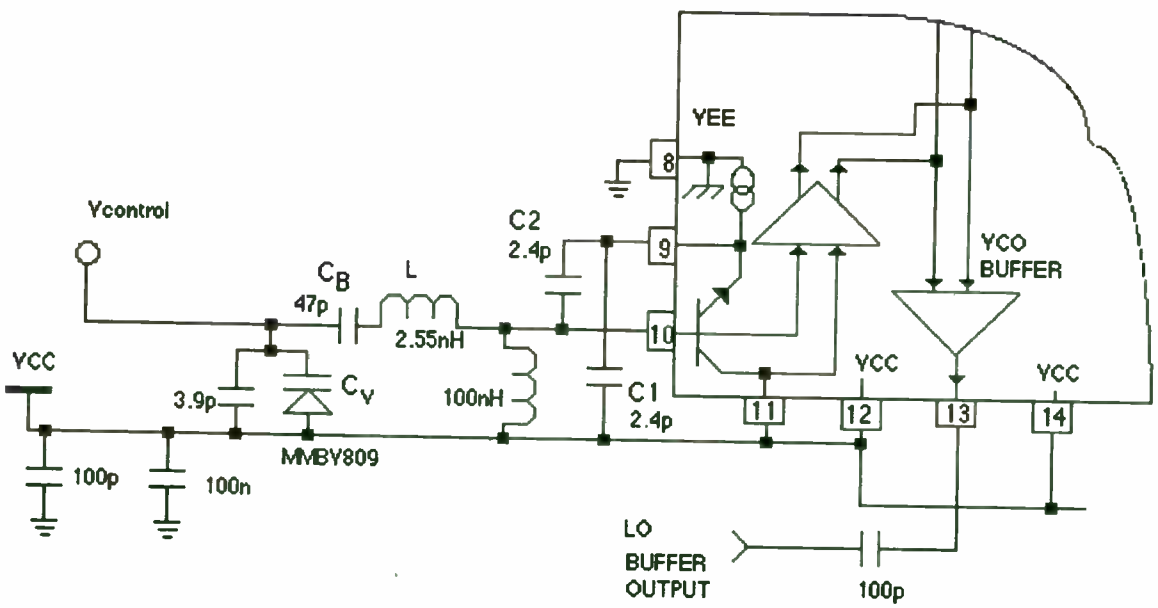
$$L' \sim L - 1/\omega^2 C_V$$

If CB ~ Cv, then the effect of Cv is minimized and the VCO sensitivity is minimized.

The parasitic capacitance , Cp, is minimized by keeping the interconnects short and maintaining small component mounting pads. Components should be chosen that are high Q having minimum parasitics. The Q of the inductor is important to maintain phase noise performance and power developed in the VCO. Also, the varactor should have sufficient Q at the VCO frequency; the MMBV809 offers high Q (150) with 6pF at 2 volts.

Thus, the nominal center frequency of the VCO with 2 volt varactor controlled voltage is calculated to be 970 MHz; the required LO center frequency is 975 MHz.

Figure 6 - 1st Local Oscillator "VCO" Circuit



3.2. Back-end Receiver Circuit

The back-end function of the receiver makes use of the MC13158, Wideband FM IF Subsystem (see Figure 7 - Back-end Receiver Circuit).

3.2.1. IF Interface Matching

IF interface matching between the MC13142 and the MC13158 differential mixer input is implemented with an "off-the-shelf" 49.8 MHz LC bandpass transformer that is housed in a 7 mm shielded can (Toko Part # 600 GCS-8519N [7]). To optimize the bandpass response, the transformer has a ferrite slug to allow for adjustment of the inductance. 48.96 MHz is chosen as the 1st IF where the LC transformer is tuned. System 2nd image rejection of better than 50 dB is achieved using this high Q bandpass transformer.

On one side, the transformer is tapped at 2 turns (pins 2 &3) and has a capacitor across the 8 turn winding (pins 1 & 3). Between pins 1 & 3, a parallel LC circuit is formed which is resonant at 49.8 MHz center frequency; pin 3 is connected to VCC via an RC filter/decoupling network. The IF outputs are connected across the 2 turn winding (pins 1 & 2).

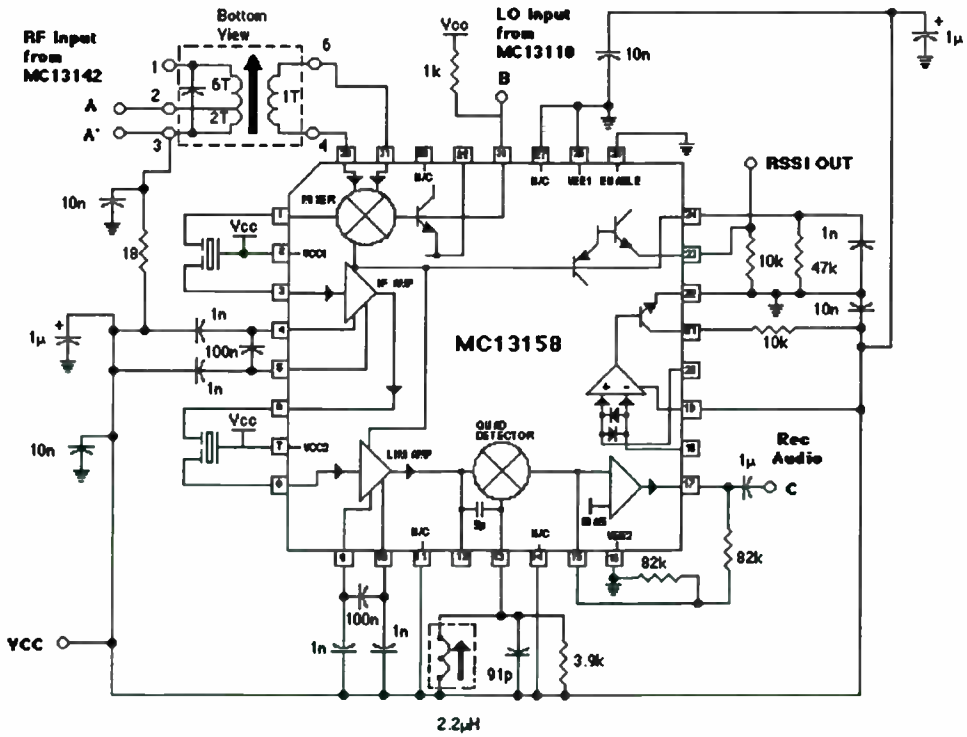
The IF signal is transformed to other side of the transformer which has a 1 turn winding at pins 4 & 6 ; they are connected to the differential mixer inputs of the MC13158. This 1st IF filter provides at least 50 dB of 2nd image rejection in the wide band FM receiver with a 10.7 MHz limiting IF.

An IF preamp provides additional gain with low noise figure and is used to lower the secondary noise figure contribution of the back-end portion of the receiver system; this, however, makes very little difference to overall noise performance but it does reduce the signal handling capability of the receiver. A receiver noise analysis is presented later which shows the results with and without the preamp (see Table 1).

3.2.2. 2nd Local Oscillator

The 2nd local oscillator is at 38.26 MHz; it is derived from the low frequency PLL and the master PLL reference oscillator in the MC13110.

Figure 7 - Back-end Receiver Circuit



3.3. System Noise Analysis

The system noise analysis uses a public domain software application published by HP called AppCAD. A summary of the system noise figure, overall gain, input 3rd order intercept point (IIP3), IMD and SINAD is presented in Table 1.

3.3.1. Front-end Noise Analysis

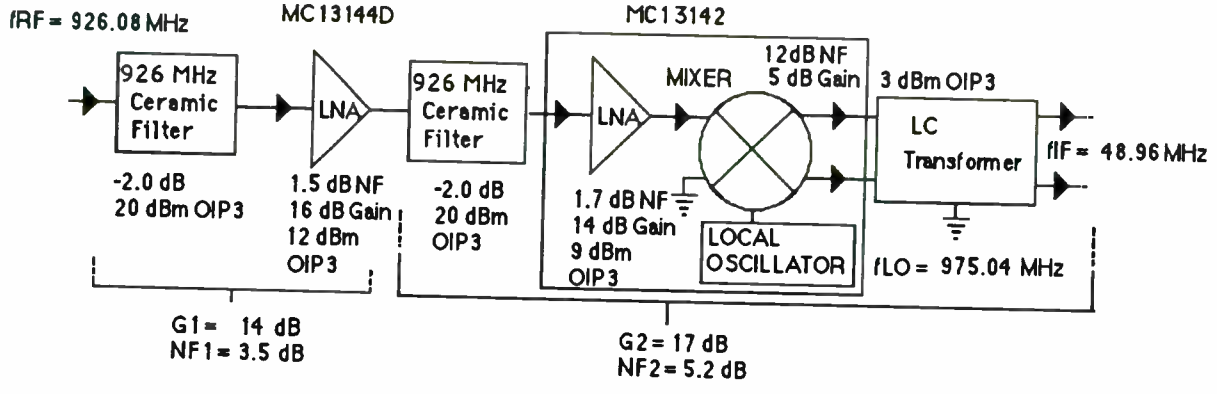
Noise analysis of the front-end and back-end IC circuits is done separately, based on the performance characterization of the ICs. Figure 8 shows the model used for the MC13144, low noise amplifier (LNA) and the MC13142D. Using both the MC13144D and the MC13142 is preferable for the following reasons:

1) Provides better overall system noise figure and SINAD performance due to added gain and lower noise figure.

2) Improves reverse isolation of the LO at the antenna port.

The additional MC13144D LNA circuit preceeding the MC13142FTB improves the reverse isolation by the contribution of the LNA 's excellent S12 reverse transmission coefficient and the RF bandpass filters that are before and after the LNA. While the RF LNA provides excellent improvement in noise performance, it reduces the IIP3. The first RF ceramic duplexer filter contributes to 1.5 to 3.8 dB insertion loss; this adds directly to the system noise figure, but the filter is necessary to improve 1st image frequency rejection and rejection of the transmitter through its duplexer action. These benefits far outweigh the loss in IIP3 performance.

Figure 8 - Noise Analysis Diagram of MC13144 & MC13142 Front-end



3.3.2. Back-end Noise Analysis

Figure 9 shows the noise model of the MC13158 at 49 MHz using the 1st IF LC filter specified in the application. The limiting IF filters are selected for 180 kHz bandwidth. Carson's Rule [10] predicts that the occupied bandwidth (OBW) is two times the maximum peak deviation, ΔF (ΔF = 75 kHz). Thus,

$$OBW = 2\,\Delta F = 150kHz.$$

Therefore, a filter having 180 kHz bandwidth allows for variations in the filter center frequency and bandwidth.

Performance is shown with and without a preamp in Table 1 (Circuits 2 &3). With an IF preamp, IIP3 worsens while sensitivity is improved.

Figure 9 - Noise Analysis Diagram of MC13158 Back-end

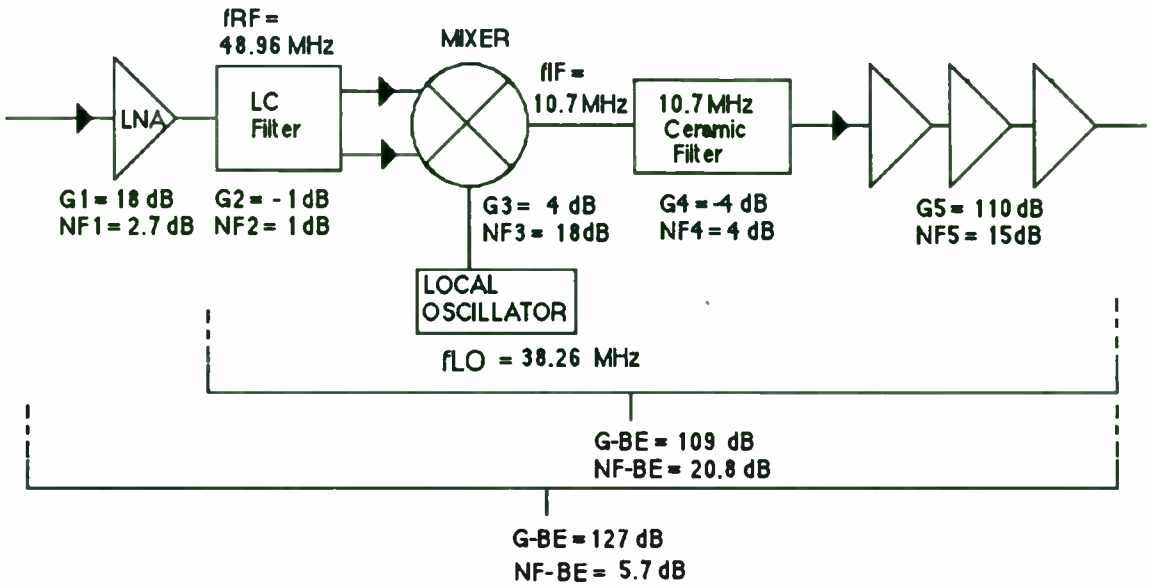


Table 1 - Noise Analysis Front-end and Back-end Circuits

VCC = 3 Vdc; Input Power = -30 dBm; fdev = ± 75 kHz; 10.7 MHz IF Ceramic Filters w/180 kHz 3 dB Bandpass.

Circuit Reference Number	Circuit Configuration Description	Cascaded Gain (dB)	Cascaded NF (dB)	Input IP3 (dBm)	Minimum Detectable Signal (dBm)	Output IP3 IM3 O/P Level (dBm)
1 (Figure10)	MC13144D + MC13142D	31	3.67	-28.3	-115.8	2.7 -2.3
2 (Figure11)	MC13158 w Preamp	127	5.72	-17.6	-113.8	109.4 72.1
3 (Figure11)	MC13158 w/o Preamp	109	20.8	0.5	-98.8	109.5 18.
4 (Figure10 & Figure 11)	Circuits1 & 3: MC13144D+ MC13142D + MC13158	140	3.84	-29.1	-115.6	111. 108.2
5 (Figure 10 & Figure 11)	Circuits 1 & 2: MC13144D+ MC13142D+ MC13158 w/preamp	158	3.68	-29.1	-115.8	128.9 126.2

3.3.3. Cascaded Receiver System Noise Analysis

The front-end and back-end circuits in Table 1 are cascaded together showing the overall gain and noise figure, receiver sensitivity, intermodulation and intercept point performance. The receiver system comprised of the MC13144D, MC13142 and MC13158 with no external IF preamp (Table 1- circuit reference number 4) is chosen because it offers the best overall performance. The cascaded noise figure and sensitivity are optimized while maintaining reasonable third order intercept point and intermod performance. The worst peformances for IIP3 and intermod are when preamp is used with back-end IC.

4. Performance Criteria

The receiver outlined in Figure 5 has the following measured performance in the complete system:

> System Noise Figure is typically 3.8 dB
> 12 dB SINAD performance is typically -114dBm.
> Input Third Order Intercept Point of -29 dBm
> 1st Image Rejection > 70 dB
> 2nd Image Rejection > 50 dB
> Adjacent channel rejection Is > 60 dB
> RSSI Dynamic Range of Typically 70 dB

5. Other Design Considerations

5.1. Component Selection

Component selection is a critical issue in RF circuit design. Components used in these radio and wireless systems must be well characterized and must be consistent from lot to lot. The Q and tolerance of the components used in fixed tuned circuits should be tightly specified. Of the several manufacturers of RF SAW and dielectric bandpass filters for cordless phone applications, the specifications for maximum insertion loss are somewhat relaxed and varied. If the RF preselector filter has wide and uncertain specification limits, this will adversely affect the receiver system performance since the preselector filter insertion loss adds directly to system noise figure. These filters are optimized for 50 ohm load and source terminations; it is important that the interface matching is implemented correctly and that it can be repeated in a production manufacturing environment .

5.2. PCB Layout

In RF circuit design, controlled impedance lines are used to reduce lump component count and to reduce manufacturing cost. Microstrip techniques are successfully used in 900 Mhz duplexer/preselector filter design. The ICs specified in this receiver are surface mount components; a compact layout using these ICs and other surface mount passive components is realized. The demonstration receiver PCB is an example of good RF layout and grounding practices; other good examples are represented in the evaluation PCB discussed in each IC data sheet. Chapter 8 of the Analog IC data book discusses the criteria for for good RF layout [9].

5.3. FCC Regulation and Approval

The receiver system discussed in this paper is not considered a final product nor is it pre-approved by the FCC. It is the responsibility of the manufacturer to obtain the acceptance and the licenses required by the Code of Federal Regulation (CFR Title 47) to manufacture and market a radio frequency product. The main purpose of this paper is to help the radio designer in his quest for design techniques, application solutions, and suitable semiconductor and passive components that achieve the performance criteria of the wireless communication system.

6. References

[1] Code of Federal Regulations, Title 47, U.S. Government Printing Office, Washington, 1994, Part 15 & 95.

[2] MC13144/D, Motorola Semiconductor Technical Data, Motorola, Inc., Tempe, AZ, 1996.

[3] MC13142 /D, Motorola Semiconductor Technical Data, Motorola, Inc. ,Tempe, AZ, 1995.

[4] MC13158/D, Motorola Semiconductor Technical Data, Motorola, Inc., Tempe, AZ, 1994.

[5] MC33110/D, Motorola Semiconductor Technical Data, Motorola, Inc., Tempe, AZ, 1993.

[6] MC145220/D, Motorola Semiconductor Technical Data, Motorola, Inc., Tempe, AZ, 1994.

[7] Ceramic Bandpass Filters Data, Motorola Components Division, Motorola, Inc., Albuquerque, NM, 1994.

[8] 600GCS-8519N Coil Specification, Toko, Inc., Tokyo, Japan, 1993.

[9] Analog and Interface Data Book, DL 128/D, Rev. 6, Motorola, Inc., Tempe, AZ, 1996.

[10] Couch II, Leon W., Digital and Analog Communications Systems, 4th ed., Macmillian Publishing Co., New York, 1993, p 384.

Off-the-Shelf 900 MHz Cordless Telephone System: Dual PLL Design

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The MC145220 dual PLL supports two 900 MHz loops simultaneously using a common reference which feeds two independent reference counters. The only additions needed to build two frequency sources for an analog cordless phone are low-pass filters and a pair of MC13142 ICs with on-chip VCOs. The PLL allows one or both loops to be placed in standby to extend battery life.

Packages available are the EIAJ 20-pin surface-mount package with 50-mil lead pitch and the TSSOP (thin shrunk small-outline package) with 0.65 mm pitch.

Main Features

The PLL frequency synthesizer shown in Figure 1 contains two on-board programmable counters covering a range of 40 to 1100 MHz. (Evaluation of operation down to 22 MHz was being conducted at the time this paper was written.) Input sensitivity is -16 dBm from 700 to 1100 MHz over a temperature range of -40 to 85° C [1].

A minimum operating voltage of 2.7 V, an operating current of 6 mA nominal per loop, and two standby modes make this PLL attractive for cordless phone applications. Two phase/frequency detectors are included for each loop; one has a current source/sink output and the second has a double-ended output.

Wide Channel Spacing

The loop counters allow lower loop counter divide ratios than most other 1 GHz PLLs. This is because the counters have independent prescalers with divide ratios of 32/33 and 64/65. The 32/33 setting allows a minimum divide ratio of 992. Thus, the wide channel spacing of 320 kHz is possible for the cordless phone application at 900 MHz because the minimum divide ratio required is 900 MHz / 320 kHz or about 2,812.

A PLL with a 64/65 prescaler is precluded from this application because its minimum divide ratio (with continous band coverage) is 4,032.

Operating Current

Supply current is determined by three modes which are controllable via a serial port. Both loops on standby is a current drain of a few microamps. With the reference running and one loop operating, the current is about 6.5 mA. With both loops and the reference operating, the supply current is nominally 12 mA.

Phase Detectors

The device has two types of phase detectors (actually, phase/frequency detectors).

One detector has a single-ended output which is a current source/sink/float. This detector is used in the cordless phone application. The "current-source" detector output's working voltage range is to within a half volt of either supply rail and it is usually used with an external passive low-pass filter.

The other detector has a double-ended output which is tied to an external combiner and loop filter. This circuit usually includes an op amp.

Additional Attributes

The reference counters may independently programmed which allows different step sizes for each loop. With the cordless phone, both were programmed with the same value to achieve the same channel spacing for both loops.

The synchronous serial port is SPI compatible and may be operated up to 2 megabits per second. A single steering bit allows random access of the five registers due to the patented register logic. An 8-bit transfer accesses the C registers which select which detector is used, the polarity of the phase/frequency detectors, engages the standby modes, and controls the gain of the current-source phase detectors. A 16-bit transfer accesses the R register which determines the reference counter divide ratio and oscillator/reference circuit mode. The R register is double-buffered to allow new divide ratios to be presented to the reference and loop dividers simultaneously. A 24-bit transfer accesses the A registers which determine the loop (or VCO frequency) divide value. This is also refered to as the loop multiplying factor.

A lock detect signal is available for each loop.

The IC includes the capability of monitoring the outputs of the counters. An auxiliary reference divider may be engaged to divide the reference by 16, 8, 4, 2, or 1. The output of the divider is fed to the REFout pin.

Loop Filter Design

The referenced application note [2] is used to calculate the loop filter component values. A five element loop filter is used per Figure 2 and is similar to the filter used in the PLL evaluation kit [3].

First, the variables which determine the first section of the loop filter are calculated.

The phase detector gain equation is

$Kp = Ip/2\pi.$ (1)

The output current is 1 mA out of the phase detector. Therefore,

$Kp = 1mA/2\pi = 0.000159$ amps/rad. (2)

The VCO in the application (on the MC13142) has a sensitivity of 6.53×10^7 radians/volt.

Per the note [2], $a = Kp \times Kv = 10{,}400$. (3)

Using Tables 1 and 2, the middle of the transmit frequency bands to be tuned is

$f = fmax + fmin / 2$ (4)

$= 902.4 + 927.68 / 2 = 915$ MHz.

Note that for ease of design, the maximum frequency from the base unit and the minimum frequency from the handset are used. (The middle portion of this "band" is actually not tuned.) Thus, the nominal loop multiplying factor is the middle frequency / channel spacing which is

$n = 915$ MHz / 320 kHz = 2860. (5)

Lock time t is picked to be 5 ms.

For the cordless phone, lock is when the loop has settled to within 1 kHz of the

final frequency. For the collective transmit bands shown in Tables 1 and 2, the range of the VCO is approximately 26 MHz.

Therefore, from the app note [2]

$b = \ln (1\ kHz / 26\ MHz) = -10.2.$ (6)

Finally, the calculations for the first section of the loop filter are

$r = - (2nb / at) =$ approx 1 kΩ. (7)

$c = at^2 / n (b^2 + \pi^2) =$ about 0.82 µF. (8)

Second, the saturation capacitor is selected by using 5 to 25% of c or 0.82 µF. This gives a range of 0.04 to 0.2 µF. A 0.15 uF capacitor was used.

Finally, the second filter section is determined by calculating the -3 dB frequency of the closed loop (of the first filter section). This is 870 Hz. The second filter section should be set to

10 x 870 or 8.7 kHz. (9)

Choosing R to be 12 kΩ,

$C = 1 / 2\pi fR =$ approx 1500 pF. (10)

Calculations for the receive loops yield similar results. Thus, the same loop filter was used for all loops.

Programming

The Configuration Registers (C Registers) are initially programmed to activate both loops. Per Figure 3, the standby bits must be low. Maximum phase detector gain is selected by setting the current bits (I2 and I1) to high levels. The current source/sink phase detectors are selected by clearing the PDA/B bits low. The Port bit is a don't care because Output A is not used in the cordless phone. Finally, the phase detector polarity bits are cleared low to be compatible with the MC13142 VCO design (which increases its frequency when the input control voltage increases). Summarizing, two 1-byte packets need to be sent to the IC with hexadecimal values of $30 and $B0.

The Reference Register (R Register) is programmed to place the IC in "reference mode" to accept an input from an external 10.24 MHz reference oscillator. The reference output (REFout) is programmed to be shut off. Finally, the reference counter is programmed to divide the 10.24 MHz down to 320 kHz which is the channel spacing for the cordless phone. Therefore, a divide ratio of 10.24 MHz / 320 kHz or 32 is needed. 32 is converted to $20. Summarizing, one 2-byte packet of $4020 is sent. Refer to Figure 4.

The two A Registers are used to determine the frequencies tuned. See Figure 5. The values are calculated by first determining the multiplication factor needed for a particular frequency. For example, from Table 1, 902.40 MHz is tuned by multiplying the 320 kHz reference counter output by 2,820. The formula $N \times P + A$ (11) from the MC145220 data sheet [1] is used. P is the prescaler lower value which is 32 for the cordless phone. 2,820 is divided by 32 then rounded down to the nearing whole number; this is 88 or $58. Formula 11 is then used to calculate A to be 4. Refering to Figure 5, the hex value for the register is then $805804. Summarizing, a 3-byte packet of $805804 is sent to program the PLL' multiplying factor. The next higher channel is tuned by incrementing the A Register value by one. Thus, $805805 tunes 902.72 MHz. Tables 1 and 2 show the programming for all 20 channel pairs used in the cordless phone.

Obtain More Information

For additional information on this product, call the Motorola automated fax service at 602-244-6609. Request data sheet number MC145220 and the evaluation kit technical summary MC145220EVKTS.

PLL samples and evaluation kits are shippable from stock and may be ordered through an authorized Motorola Semiconductor distributor or a Motorola Semiconductor sales office. The MC145220DT is the TSSOP and the MC145220F is the EIAJ package. The kit part number is MC145220EVK.

Additional papers are included in this publication which describe the other devices in the Motorola 900 MHz cordless phone chip set.

References

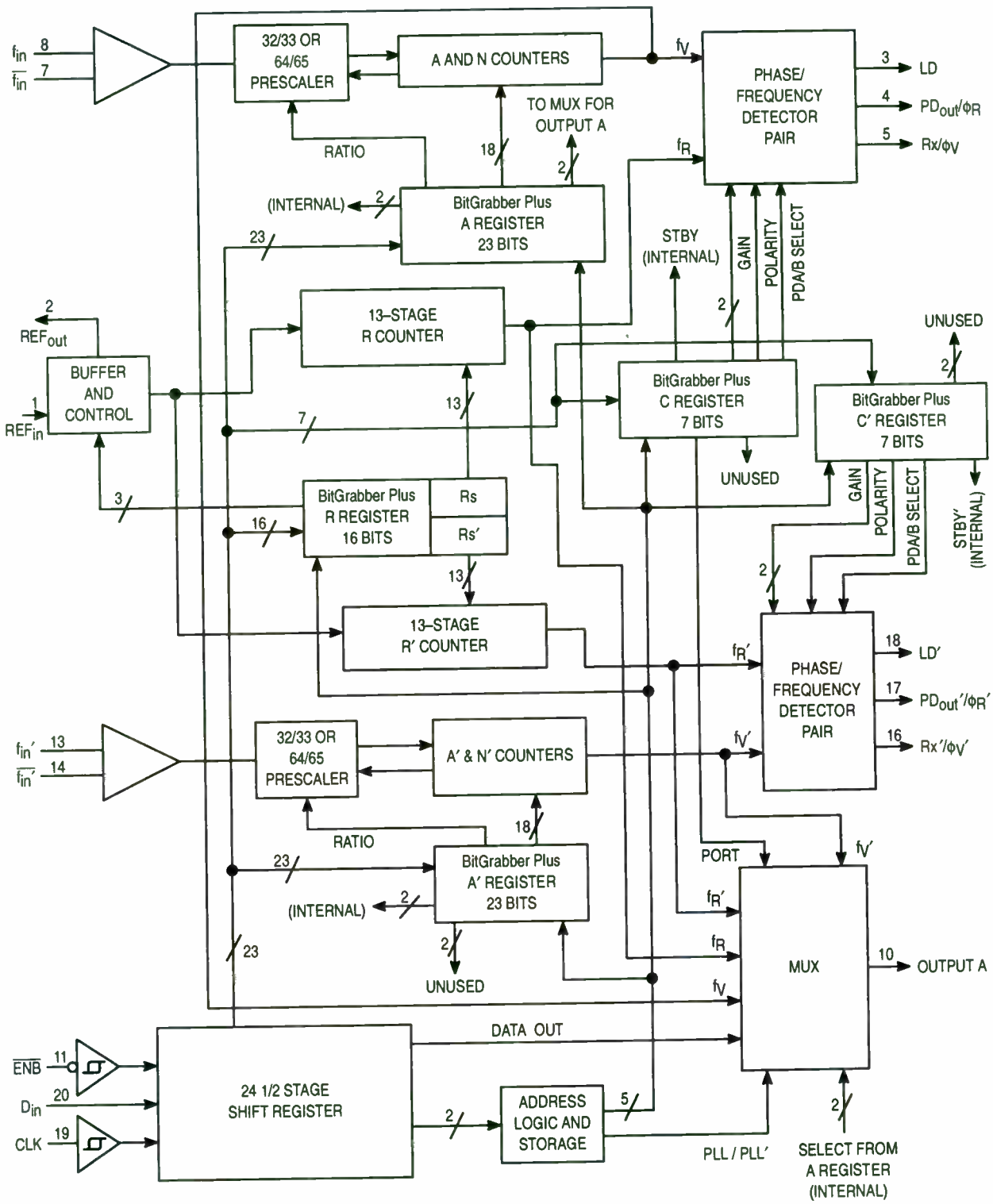
[1] MC145220 Data Sheet, rev. 3, Motorola, 1995
[2] AN1253 Application Note, Motorola, 1995
[3] MC145220EVKTS Evaluation Kit Technical Summary

Table 1. Handset Channels

Channel No.	PLL		PLL′	
	Receive L.O. Frequency, MHz	Program Data for A Register, Hexadecimal	Transmit Frequency, MHz	Program Data for A′ Register, Hexadecimal
1	973.76	005F03	902.40	805804
2	974.08	005F04	902.72	805805
3	974.40	005F05	903.04	805806
4	974.72	005F06	903.36	805807
5	975.04	005F07	903.68	805808
6	975.36	005F08	904.00	805809
7	975.68	005F09	904.32	80580A
8	976.00	005F0A	904.64	80580B
9	976.32	005F0B	904.96	80580C
10	976.64	005F0C	905.28	80580D

Table 2. Base Unit Channels

Channel No.	PLL		PLL′	
	Receive L.O. Frequency, MHz	Program Data for A Register, Hexadecimal	Transmit Frequency, MHz	Program Data for A′ Register, Hexadecimal
1	951.36	005C1D	924.80	805A0A
2	951.68	005C1E	925.12	805A0B
3	952.00	005C1F	925.44	805A0C
4	952.32	005D00	925.76	805A0D
5	952.64	005D01	926.08	805A0E
6	952.96	005D02	926.40	805A0F
7	953.28	005D03	926.72	805A10
8	953.60	005D04	927.04	805A11
9	953.92	005D05	927.36	805A12
10	954.24	005D06	927.68	805A13



PIN 9 = V+ (Positive Power to the main PLL, Reference Circuit, and a portion of the Serial Port)
PIN 6 = GND (Ground to the main PLL, Reference Circuit, and a portion of the Serial Port)
PIN 12 = V+′ (Positive Power to PLL′ and a portion of the Serial Port)
PIN 15 = GND′ (Ground to PLL′ and a portion of the Serial Port)

Figure 1. MC145220 Block Diagram

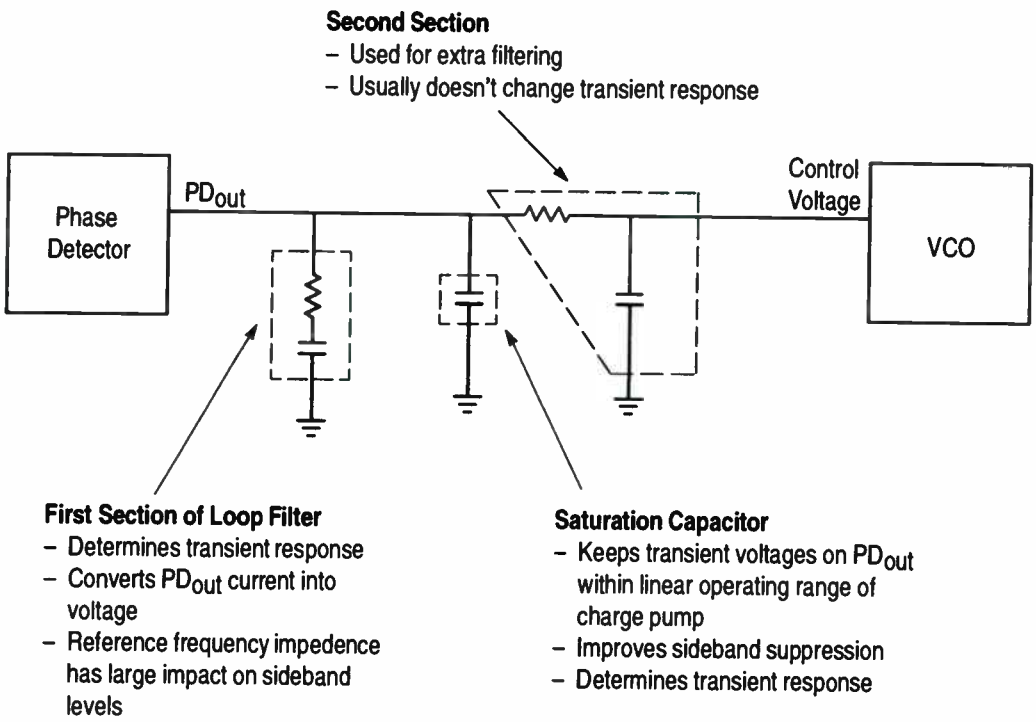
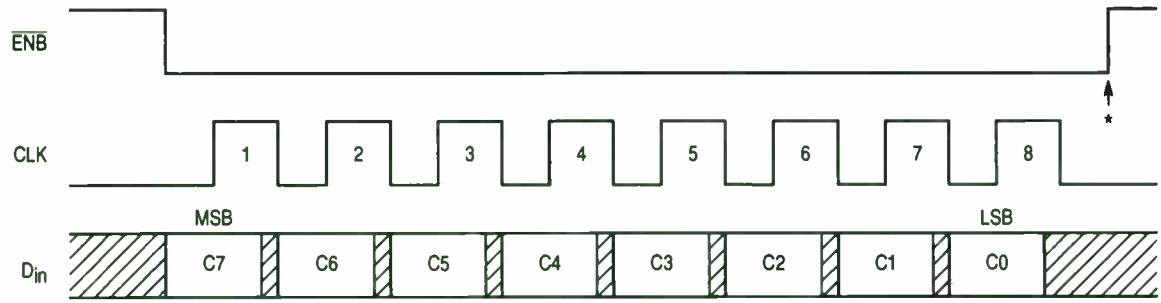


Figure 2. Standard Loop Filter



* At this point, the new byte is transferred to the C or C′ register and stored. No other registers are affected.

C7 – Steer: Used to direct the data to either the C or C′ register. A lqw level directs data to the C register; a high level is for the C′ register.

C6 – Standby: When set high, places both the main PLL and PLL′ (when C6 is set in the C register) or PLL′ only (when C6 is set in the C′ register) in the standby mode for reduced power consumption.

C5, C4 – I2, I1: Independently controls the PD_{out} or PD_{out}' source/sink current. With both bits high, the maximum current is available.

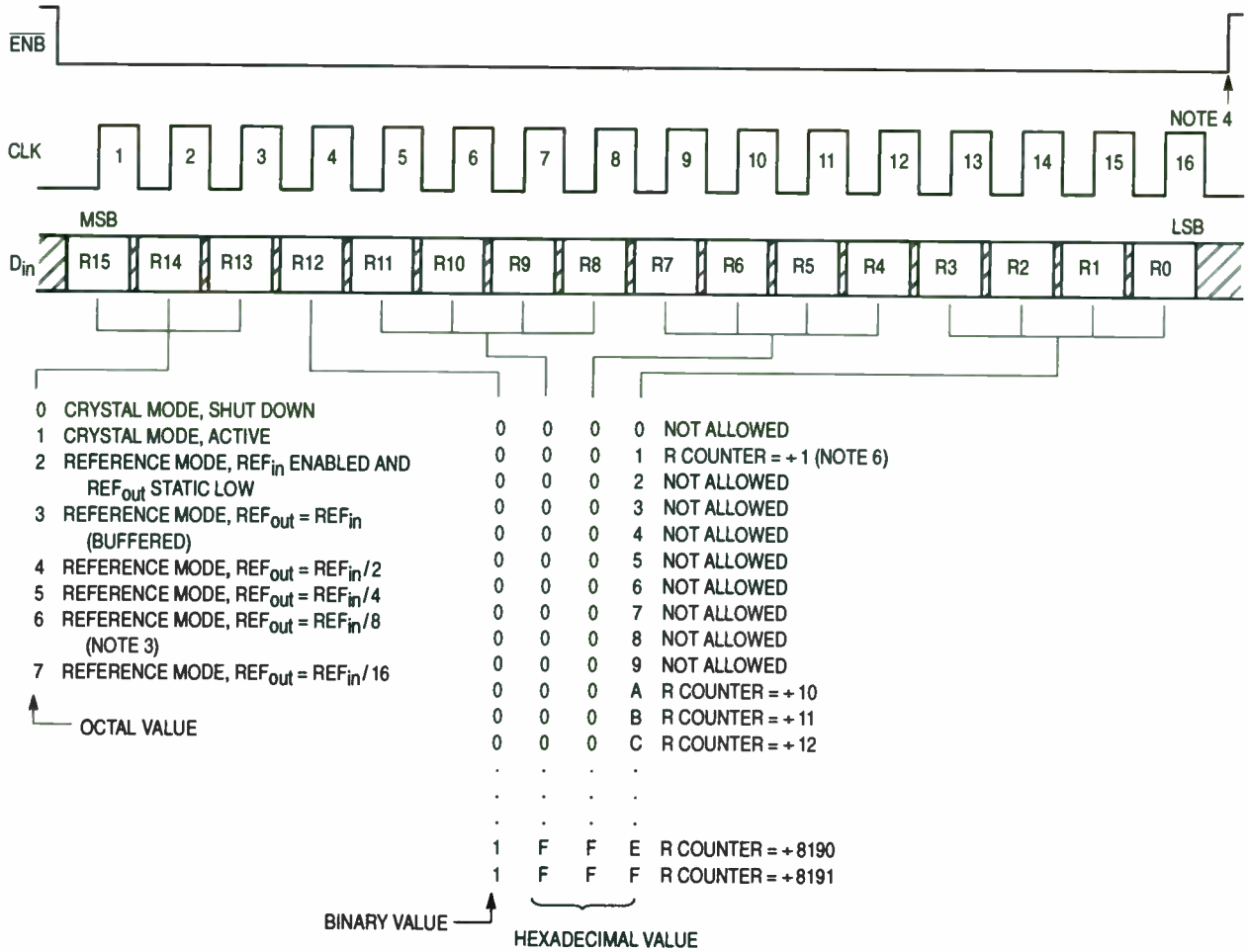
C3 – Spare: Unused

C2 – PDA/B: Independently selects which phase/frequency detector is to be used. When set high, the double–ended detector is selected with outputs ϕ_R and ϕ_V or ϕ_R' and ϕ_V'. When reset low, the current source/sink detector is selected with outputs PD_{out} or PD_{out}'.

C1 – Port: When the Output A pin is selected as "Port" via bits A22 and A21, C1 of the C register determines the state of Output A. When C1 is set high, Output A is forced to the high–impedance state; C1 low forces Output A low.

C0 – POL: Selects the output polarity of the associated phase/frequency detectors.

Figure 3. C and C′ Register Accesses and Format (8 Clock Cycles are Used)



NOTES:

1. Bits R15 – R13 control the configurable "Buffer and Control" block (see Block Diagram).
2. Bits R12 – R0 control the "13–stage R counter" blocks (see Block Diagram).
3. A power–on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "Buffer and Control" block in the Block Diagram. Bits R0 – R12 are loaded into the first buffer in the double–buffered section of the R register. Therefore, the R or R′ counter divide ratio is not altered yet and retains the previous ratio loaded. The C, C′, A, and A′ registers are not affected.
5. Bits R0 – R12 are transferred to the second buffer of the R register (Rs in the Block Diagram) on a subsequent 24–bit write to the A register. The bits are transferred to Rs′ on a subsequent 24–bit write to the A′ register. The respective R counter begins dividing by the new ratio after completing the rest of its present count cycle.
6. Allows direct access to reference input of phase/frequency detectors.

Figure 4. R Register Access and Format (16 Clock Cycles are Used)

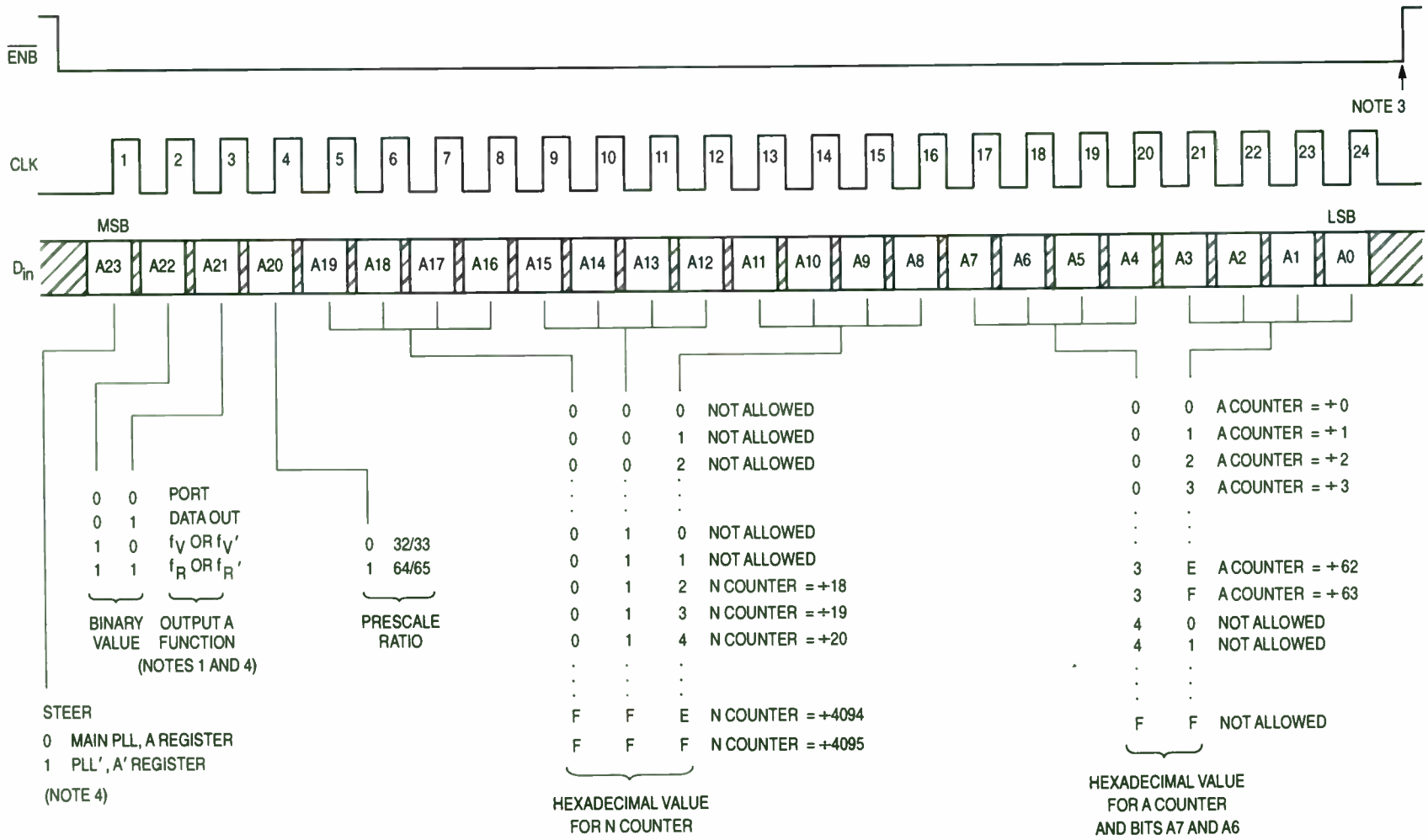


Figure 5. A and A′ Register Accesses and Format (24 Clock Cycles are Used)

NOTES:

1. A power-on initialize circuit forces the Output A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x P + A where N is the value programmed for the N counter, P is 32 if bit A20 is low or 64 if A20 is high, and A is the value programmed for the A counter.
3. At this point, the three new bytes are transferred to the A register if bit A23 is a "0" or A′ register if A23 is a "1". In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's relative second buffer, Rs or Rs′. Thus, the R, N, and A (or R′, N′, and A′) counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C or C′ registers are not affected.
4. A "0" for the Steering bit allows selection of f_R, f_V, Data Out, or Port by bits A21 and A22. A "1" for the Steering bit allows selection of $f_{R'}$, $f_{V'}$, Data Out, or Port.

Surface-Mount Wireless IC Power Dividers, Directional Couplers, and Hybrid Junctions

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Technical Subject (keywords): Power Dividers, Directional Couplers, Quadrature Hybrids, Wireless, Plastic Packaged MMIC.

Content of Presentation: A departure from traditional technology for power dividers, couplers, and quadrature hybrids is presented. In the past, ferrite core technology has been the preferred technology to implement these functions at RF and lower microwave frequencies. Alpha has utilized its MMIC fabrication technology to realize these components in small standard IC packages (SOIC-8, MSOP-8, and SOT-6). These devices are not only lower in cost and smaller in size than their ferrite or stripline predecessors, but are also more repeatable and reliable.

Value to Audience: These products are not only new to Alpha, but are also new to the industry. Many engineers are either unaware they exist or may have questions about how they are made and how they perform.

1/f Noise Characteristics Influencing Phase Noise

ABSTRACT

In applications such as VCO's where 1/f noise is the major contributor to phase noise in a given circuit, the device with the best 1/f noise will yield the best phase noise. To better understand how 1/f noise changes with bias and from device to device, the 1/f noise of two different bipolar devices was measured and compared. Nonlinear models were developed and the predicted and measured 1/f noise spectrums were compared. In addition, how manufacturers quantify 1/f for simulation purposes is evaluated to provide the designer with better insight into what the 1/f coefficient and exponent mean, and how the values effect the 1/f noise simulations.

INTRODUCTION

The phase noise of an oscillator, quantified by its short term frequency stability, determines the system's ability to separate adjacent channels. With the significant increase in portable, wireless traffic and digital transmission, better frequency stability is required. Phase noise is an important consideration. Choosing the appropriate topology for a low phase noise source is important, as is the choice of resonator and coupling network [1]. Many articles exist on how to design an oscillator for low phase noise by selecting the appropriate topology, resonator and coupling network. One example is provided in reference [2]. Once the oscillator topology, resonator and coupling structures are selected, the active device is selected.

PHASE NOISE

To evaluate the effects of 1/f noise on the overall phase noise of the oscillator, the expression for sideband noise due to noise upconversion is evaluated in terms of the small signal equivalent circuit parameters documented by J.S. Yuan [3]:

$$SBN = 20\log\{(d\varnothing / dI_c)\,[dI_c f_o / (2.828\, Q_L f_m)]\} \quad (1)$$

Where f_o is the oscillator frequency, Q_L is the oscillator loaded quality factor, f_m is the offset frequency, and dI_c is the collector current variation due to noise sources. These noise sources are quantified in the following equation:

$$dI_c = [(4kTB/r_e)^{1/2} + (4kTBr_{bb}g_m^2)^{1/2}] + [(K_F I_b^{A_F} B)/F_c]^{1/2} + [2qI_cB]^{1/2} \quad (2)$$

In equation (2), the first term represents thermal noise, the second term represents flicker noise, and the third term represents the shot noise. k is Boltzmann's constant, T is the temperature in degrees Kelvin, B is the bandwidth in Hertz, r_e is the intrinsic emitter resistance, r_{bb} is the base spreading resistance, gm is the transconductance, K_F and A_F are flicker noise variables, I_b is the flicker noise base current, F_c is the flicker noise corner frequency, q is the electron charge, and I_c is the DC collector current.

From equation (2), the intrinsic *device characteristics* that effect the sideband noise performance are: (a) base and emitter resistances, (b) transconductance, and (c) 1/f noise characteristics. These device characteristics are a function of the *operating conditions*: temperature, frequency bandwidth, and DC bias. In addition, 1/f and r_{bb} are related in that devices with higher r_{bb} have higher 1/f noise.

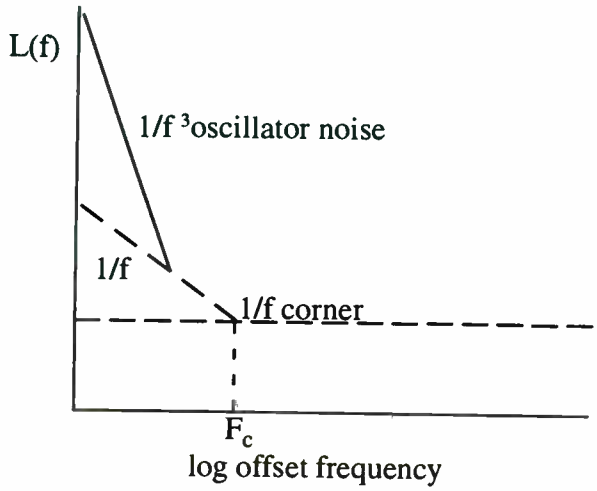


Figure 1. Flicker noise upconverted to oscillator phase noise.

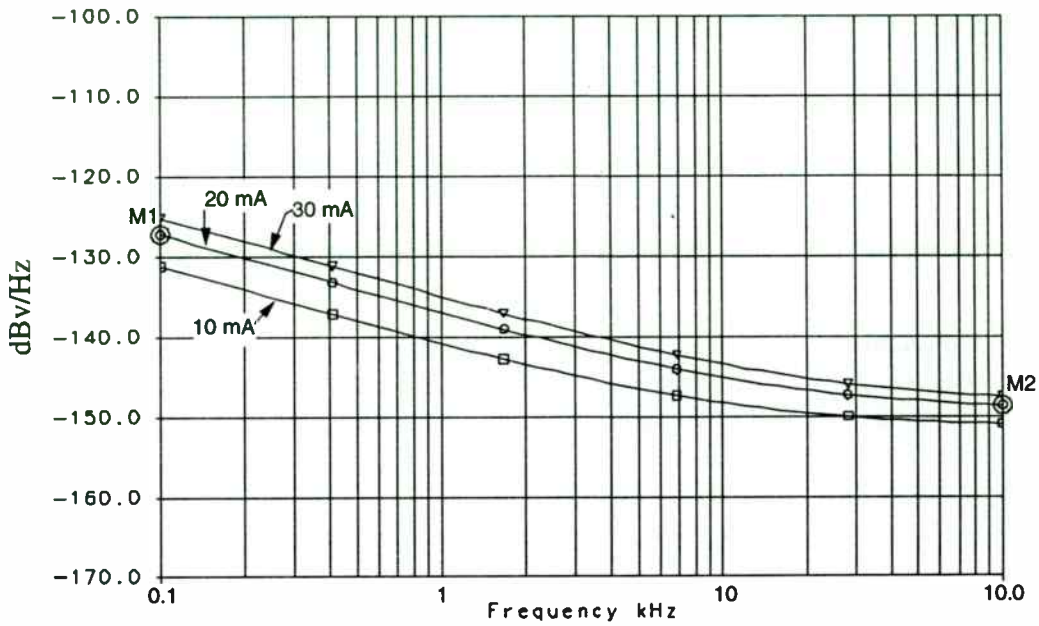
DEVICE ANALYSIS

The following analysis examines two NEC devices in the miniature surface mount "19" package. Key device specifications are shown in Table 1. These two devices were chosen because they are used in a wide variety of oscillator designs. ICmax for the 688 and 685 are 100mA and 30mA respectively. Vcemax for both parts is 6 volts. The NE68519 has a higher gain-bandwidth product, f_T, than the NE68819, 8.7GHz and 6.1GHz, respectively. The intrinsic base and emitter resistances are lower for the NE68819.

	NE68519	NE68819
V_{CE} MAX (volts)	6	6
I_C MAX (mA)	30	100
P_T MAX (mW)	125	125
f_T (GHz) MEASURED (3V, 5mA, 2GHz)	8.7	6.1
r_{bb} (OHMS)	10	6.14
r_e (OHMS)	1.3	0.4
NF (dB), TYPICAL	1.5 (3V, 3mA, 2GHz)	1.7 (1V, 3mA, 2GHz)
$\|S_{21}\|^2$ (dB), MEASURED (3V, 5mA, 2GHz)	9.4	7.0

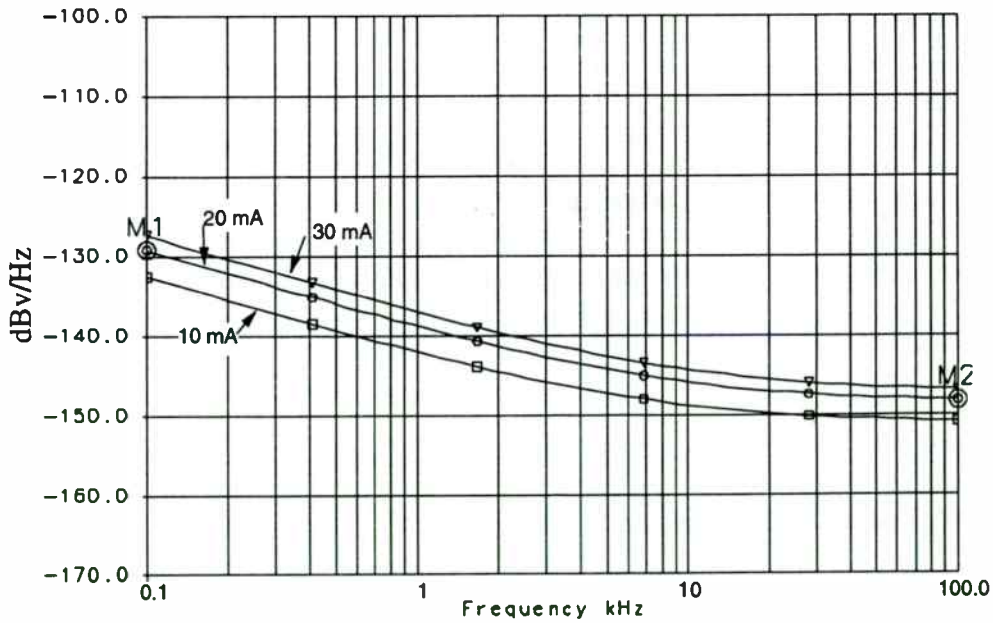
TABLE 1. Device Specifications

The 1/f characteristics were measured in accordance with reference [4]. As can be observed from equation (2), the 1/f noise is a function of the collector bias current of the device. This is well known and documented [4]. The calculated and measured 1/f corner frequencies were within 5% of each other. The 1/f simulations for the NE68519 and NE68819 biased at Vce = 3Volts and Ic = 10mA, 20mA and 30 mA are shown in Figure 2A and 2B. Figure 3A and 3B show the linear relationship between Fc and Ic.



M1 Frequency=0.1 value=-127.2
M2 Frequency=100 value=-148.6

Figure 2A. $1/_f$ noise vs. IC for the NE68500.



M1 Frequency=0.1 value=-129.2
M2 Frequency=100 value=-148.2

Figure 2B. $1/_f$ noise vs. IC for the NE68800.

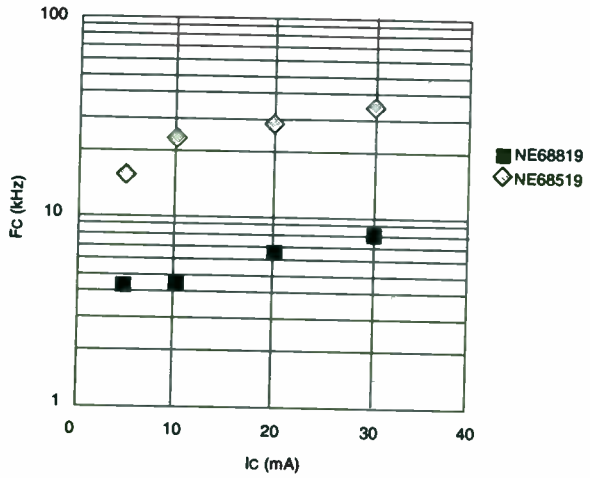


Figure 3A. Measured FC vs. IC @ VCE = 1V.

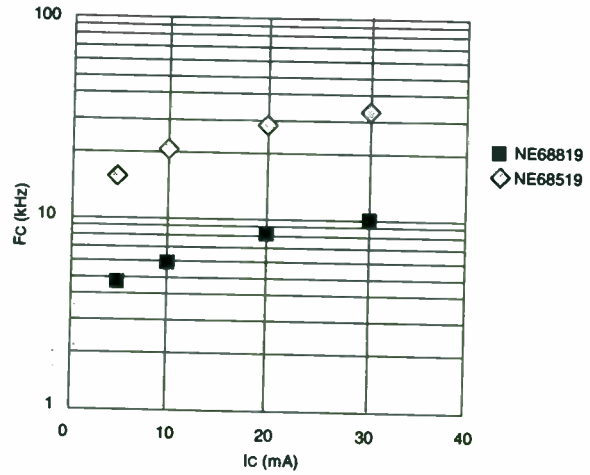


Figure 3B. Measured FC vs. IC @ VCE = 3V.

1/f noise was measured at two different Vce biases to determine the effects on 1/f noise. The 1/f corner frequency increases slightly as Vce increases as shown in Table 2. For the NE68519, an increase of Vce from 1 to 3 volts results in a 4kHz maximum increase in corner frequency from 23kHz to 27kHz, an increase of 21%. For the NE68819, the same Vce increase results in a 2kHz maximum increase in corner frequency from 8kHz to 10kHz, an increase of 25%. The 1/f profile of these two devices shows that the 68819 is far superior where close in phase noise is important.

	FC(KHZ)				%CHANGE W/VCE	
	VCE = 1 VOLT		VCE = 3 VOLTS			
IC (MA)	NE68519	NE68819	NE68519	NE68819	NE68519	NE68819
5	10	4.3	11	4.6	9% (1kHz)	7% (0.3kHz)
10	15	4.5	19	5.8	21% (4kHz)	29% (1.3kHz)
20	20	6.7	22	8	9% (2kHz)	19% (1.3kHz)
30	23	8	27	10	15% (4kHz)	25% (2kHz)

TABLE 2. Fc vs. Ic at 2 different Vce values.

Next we will examine how the 1/f noise measurements are converted to the A_F and K_F parameters for nonlinear simulation [5] using the flicker noise equation:

$$\text{Flicker Noise} = (K_F I_b^{A_F} B)/F_c \qquad (3)$$

As shown in reference [4], two 1/f measurements are made at 2 different base currents, resulting in Fc1 at Ib1 and Fc2 at Ib2. We then have two equations and two unknowns and can solve for A_F and K_F in terms of Fc1, Ib1, Fc2, and Ib2 as follows:

$$A_F = (\log Fc1 - \log Fc2 + Z) / Z \qquad (4)$$

$$Z = \log Ib1 - \log Ib2 \qquad (5)$$

$$K_F = 10^{(\log Fc1 + \log Ib1 - 18.49 - A_F \log Ib1)} \qquad (6)$$

These are the A_F and K_F values provided in the nonlinear model to simulate 1/f noise, and the devices phase noise performance with respect to 1/f noise. It is important that the A_F and K_F values used are extracted from discrete 1/f measurements, and not averaged. The A_F and K_F values used for these simulations are A_F=1.568 and K_F=6.8e-13 for the NE68519 and A_F=1.26 and KF=2.6e-14 for the NE68819. The effect of using A_F or K_F other than the extracted values are shown in Figures 4A and 4B. Although not shown in the graphs, if the default values of A_F =1 and K_F=0 are used, equation (3) results in a device with no 1/f noise and the device noise simulation will contain only thermal noise and shot noise which are frequency independent.

Figures 5A and 5B contain the nonlinear schematic and test bench using HP/EESOF's Libra simulator. The nonlinear model parameters for the NE685 and NE688 are included in Figures 5C and 5D.

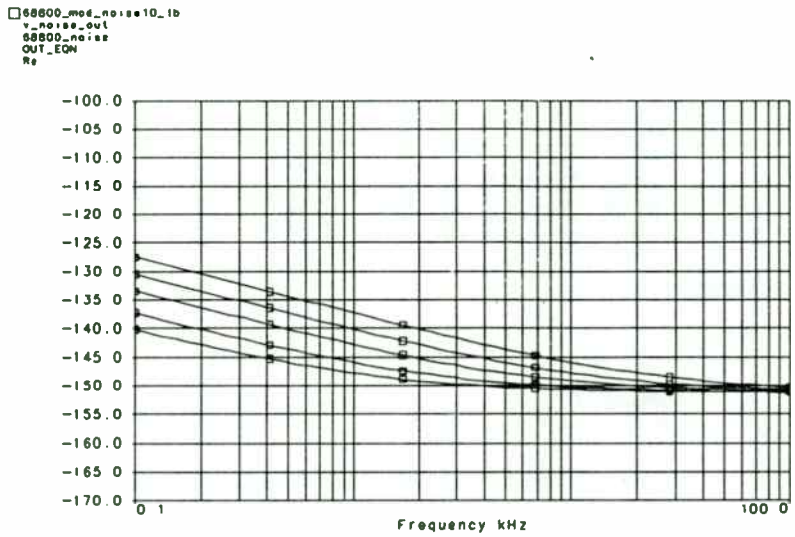


Figure 4A. K_F variation.

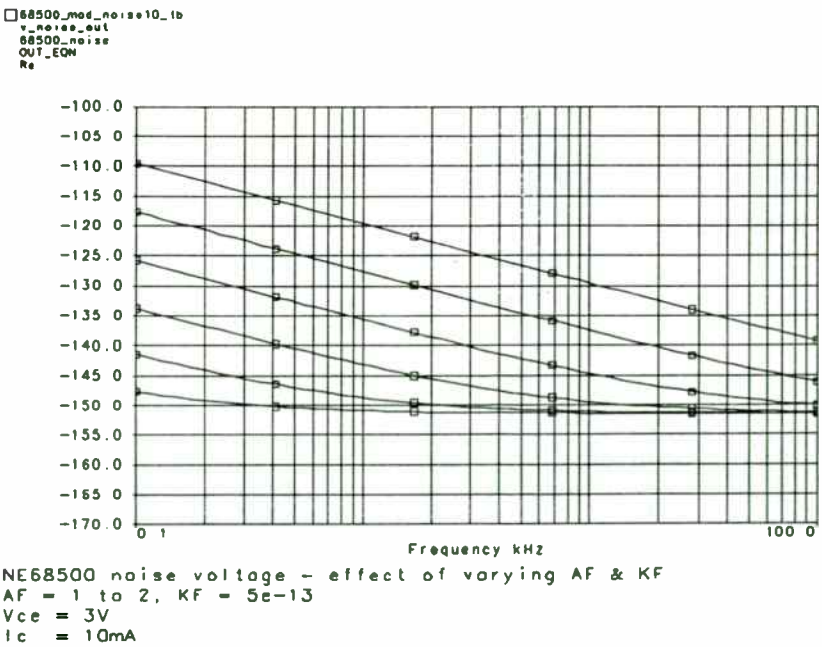


Figure 4B. A_F variations.

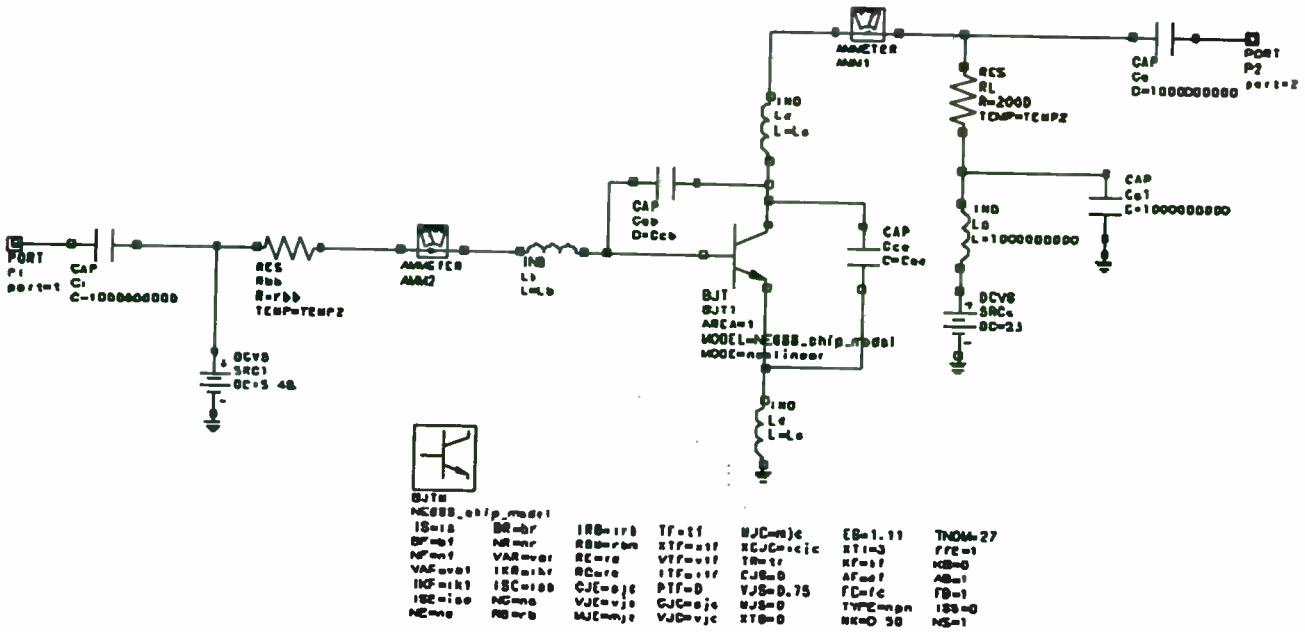


Figure 5A. Simulator schematic.

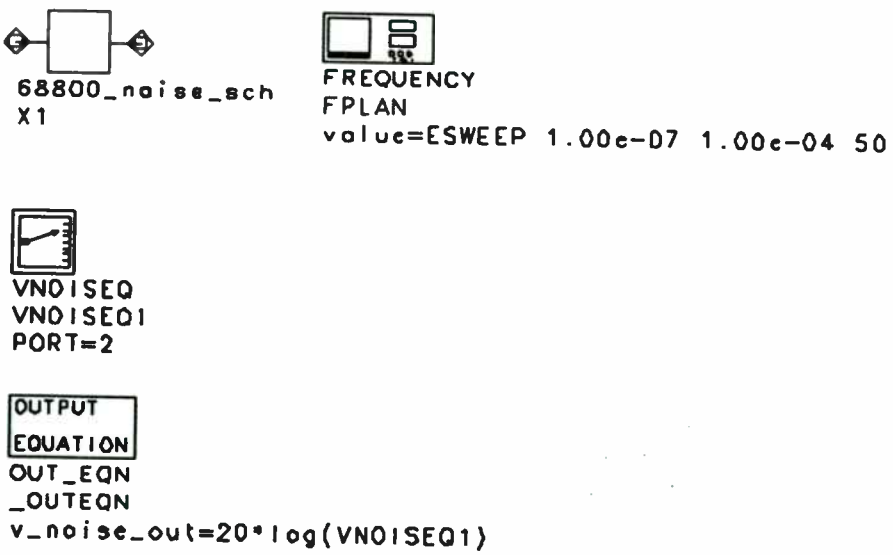


Figure 5B. Simulation test bench.

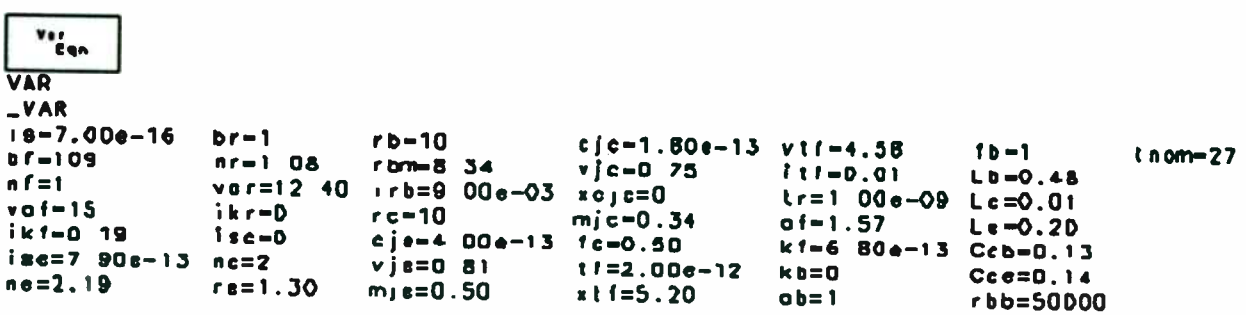


Figure 5C. NE68519 nonlinear model.

```
VAR
_VAR
is=3.80e-16   br=12.25      irb=1.00e-03  tf=1.10e-11   mjc=0.45     Cce=0.27
bf=133.70     nr=1.10       rbm=3.50      xtf=0.30      xcjc=0.55    Lb=0.72
nf=1.00       var=3.50      re=0.40       vtf=0.65      tr=3.20e-11  Lc=0.51
vaf=28        ikr=0.06      rc=4.20       itf=0.61      fc=0.75      Le=0.19
ikf=0.60      ise=3.50e-15  cje=7.96e-13  ptf=30        kf=2.60e-14  rbb=50000
ise=3.80e-15  nc=1.62       vje=0.71      cjc=5.49e-13  af=1.28
ne=1.49       rb=8.14       mje=0.38      vjc=0.65      Ccb=0.24
```

Figure 5D. NE68819 nonlinear model.

CONCLUSIONS

As the active device biased is increased, the 1/f noise corner frequency increases proportionally. The extraction technique used in reference [4] for determining A_F and K_F parameters values has been applied to two NEC devices with excellent correlation to measured data. 1/f noise profiles can be accurately simulated, providing the correct coefficients are obtained from the manufacturer. If oscillator simulations are performed with the flicker noise coefficient, K_F, and flicker noise exponent, A_F, at their default values of 0 and 1 respectively, the simulated low frequency noise spectrum will be flat with no frequency dependent noise components.

ACKNOWLEDGEMENTS

Robin Croston , Gery Peterson, Olivier Razafindramena, and Anna Duran at California Eastern Laboratories, and Andy Howard at HP/EESOF for supporting the tedious 1/f measurements and simulation effort.

REFERENCES

[1] Roger Muat, "Choosing devices for quiet oscillators," Microwave & RF, August 1984, pp. 166-170.

[2] Grant Moulton, "Dig for the roots of oscillator noise," Microwave & RF, pp. 65-69, April 1986.

[3] J.S. Yuan, "Modeling the Bipolar Oscillator Phase Noise," Solid State Electronics, Vol. 37, No. 10, 1994, pp. 1765-1767.

[4] Julio Costa et al, "Extracting 1/f Noise Coefficients for BJT's," IEEE Transactions on Electron Devices, Vol. 41, No. 11, pp. 1992-1999, Nov. 1994.

[5] "Simulating Noise in Nonlinear Circuits Using the HP Microwave and RF Design Systems," HP Product note 85150-4, c 1993.

High Performance Base Station SAW Filters and the Effects of Mechanical Stress

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ABSTRACT

Base stations for CDMA and PCS systems require adjacent channel rejections of 80 dB and more. This requirement can only be practically met with a cascade of two SAW filters. The required passband-to-stopband transition width of the filter can be as small as 100 kHz for the receiver channel filters (1 to 50 dB for the cascade) and 60 kHz (1.5 to 26 dB) for the transmitter filters, resulting in filter substrate lengths as large as 70 mm. The small transition width also makes the filter sensitive to mechanical stresses which occur during filter manufacture and mounting on a PC board. The mechanical stresses cause a degradation in the close-in rejection of the SAW filter. The SAW filter manufacturer can minimize the stresses occurring during the manufacturing process, however the metallic package has an effect on the stress sensitivity of the filter.

This paper will show the effects of mechanical stress on the performance of different base station filters. Also shown will be a variety of Base Station filters currently in production for which the mechanical stress effects have been minimized.

I. INTRODUCTION

It has been known for many years [1], [2] that a mechanical strain on the substrate of a SAW filter results in a change in the surface wave velocity and a change in the dimensions. These properties have been used for SAW oscillator pressure sensors as far back as 1975 [3], however mechanical strain can be a source of degradation in the performance of most SAW devices.

In a SAW filter there are two major sources of strain. The first is introduced during the mounting of the SAW substrate into the package. The SAW industry has minimized this source by using pliable epoxies to mount the substrate to the package. The second major source comes from stresses on the SAW filter package when it is mounted on the customer's PC board. The package plays a major role in the level of strain resulting from these stresses.

In this paper we will first present the relationship between mechanical strain on the substrate and SAW velocity. Next, the effect on the group delay of a SAW filter will be shown, followed by a discussion of the effects of package stress and experimental results. Finally, the performances of a variety of base station filters will be presented for which steps were taken to reduce the filters' stress sensitivity.

II. MECHANICAL STRAIN AND SAW VELOCITY [4]

Strains on the SAW substrate consist of three normal and three shear components. In this discussion only the normal strains will be considered. The variables (following [1]) ε_1 and ε_2 represent the normal strains parallel and perpendicular to the direction of the SAW propagation axis x (see fig. 1). The variable ε_3 represents the strain normal to the surface.

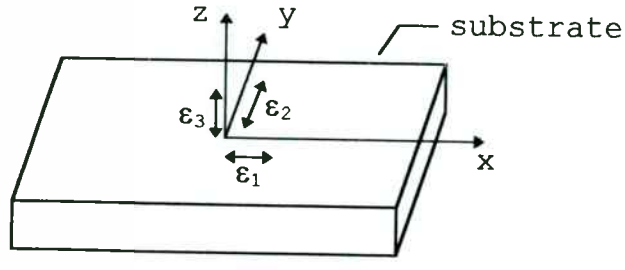

Fig. 1 - Normal strains on the substrate

A substrate without strain is represented in fig. 2a with particles located on the propagation axis. The same substrate under uniform extension along the propagation axis is represented in fig. 2b. The particles have moved a distance u along the propagation axis. This displacement is related to the uniform strain by the following equation.

$$u = \varepsilon_1 x_0 \quad \Rightarrow \quad x(\varepsilon_1) = (1+\varepsilon_1)\, x_0 \tag{1}$$

The first order dependence of the SAW propagation velocity V on the strains ε_n can be written as

$$V = V_0(1+\gamma_n \varepsilon_n) \tag{2}$$

where V_0 is the unstrained velocity and γ_n is the strain coefficient for strain ε_n with implicit summation over n.

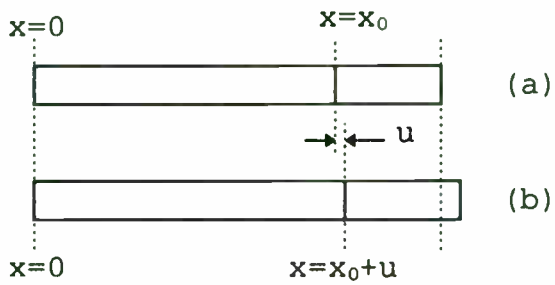

Fig. 2 - Particle displacement in (a) equilibrium, (b) with extension

The effects of substrate deformation and the velocity change together modify the acoustical delay between the particles (0 and x_0). If the assumption is made that only the ε_1 component of strain is non zero, then the group delay τ between the particles can be computed in terms of the uniform strain ε_1 .

$$\tau(\varepsilon_1) = \frac{x(\varepsilon_1)}{V(\varepsilon_1)} = \tau_0 \frac{1+\varepsilon_1}{1+\gamma_1\varepsilon_1} \qquad \text{with } \tau_0 = \frac{x_0}{V(\varepsilon_1)} \tag{3}$$

where τ_0 is the delay for the uncompressed substrate. For the case of an ST cut quartz substrate, that used for most of the base station filters currently in manufacture, the magnitude of the coefficient γ_1 is small (<.01, from [1]), thus the deformation is more important than the change in velocity.

III. SAW FILTER SENSITIVITY

A conventional SAW filter consists of two bi-directional transducers, each having a pair of interdigitated metal electrodes deposited on the surface of a piezoelectric substrate as shown in fig. 3.

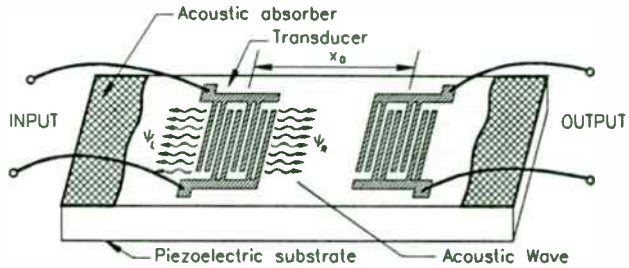

Fig. 3 - Conventional SAW filter

The distance between the centers of the transducers is x_0. The filter delay is given by equation 3 when the substrate undergoes a uniform strain along the acoustic propagation direction.

There is a corresponding change in the center frequency of the filter due to the uniform strain. This relationship is given by equation 4.

$$\Delta f/f = -\Delta\tau/\tau \tag{4}$$

For the case of a non-uniform strain the effects on the two transducers are not the same, normally resulting in a degradation of the close-in sidelobes.

IV. STRAIN DUE TO PACKAGE STRESS

A cut-away view of a SAW filter mounted in a platform package is shown in fig. 4. The cut is parallel to the propagation axis. The substrate is attached to the platform of the package with a pliable epoxy.

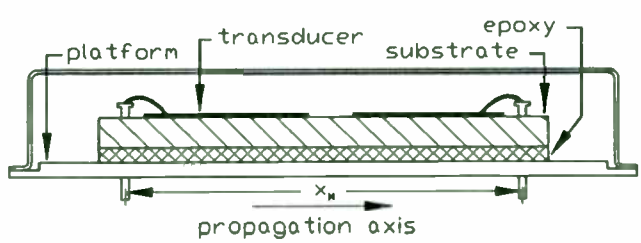

Fig. 4 - SAW filter in a platform package

The strain ε_1 occurs when the platform of the package is bent as shown in fig. 5. This can happen when the PC board that the filter is mounted on becomes warped or if an object is under the package during the soldering process. This type of bending will, at a minimum, lower the center frequency of the filter.

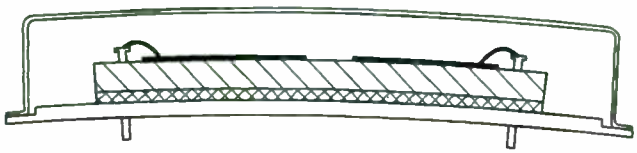

Fig. 5 - SAW filter undergoing a bending stress

Base station filters like those for CDMA systems are typically 73mm in length and have center frequencies ranging from 70 MHz to 170 MHz. A mismatch between the package and PC board coefficients of thermal expansion can introduce temperature dependent strain. This mismatch can also cause failure of the solder connections between the package and PC board. For the filter shown in fig. 4 the filter is mechanically fixed to the PC board over a distance x_M, the distance between the outer package pins. By choosing a smaller x_M, the total surface deformation will be reduced. The same holds true for a ceramic surface mount packaged SAW filter.

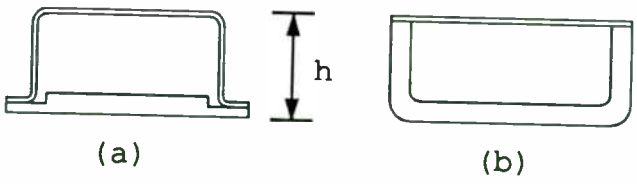

Fig. 6 - Cross section of a sealed (a) platform package, (b) unibody package

The rigidity of the package determines the filter's stress sensitivity, however this goal is in conflict with the goals of the customer, eg small size, height and cost. A cross section of two styles of metallic package are shown in fig. 6. The unibody package (fig. 6b) has a much thicker sidewall than the platform package (fig. 6a), and for the same package height h it less susceptible to the bending represented in fig. 5.

V. PACKAGE STRESS EXPERIMENTS

Experiments were performed on a some base station filters The tests consisted of placing one or two wires under the package, applying a force on the package and measuring S21 of the matched filter.

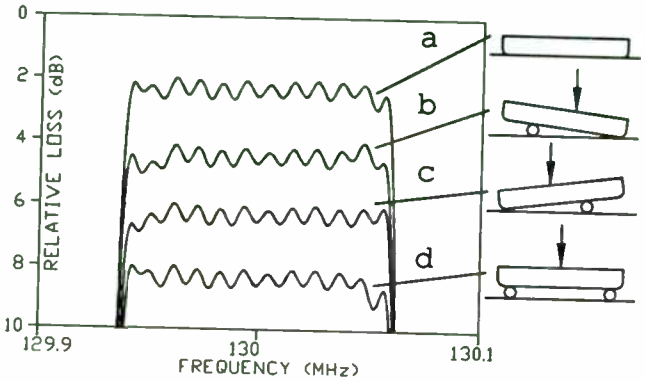

Fig. 7 - Amplitude characteristic of a base station filter under various mechanical loading conditions

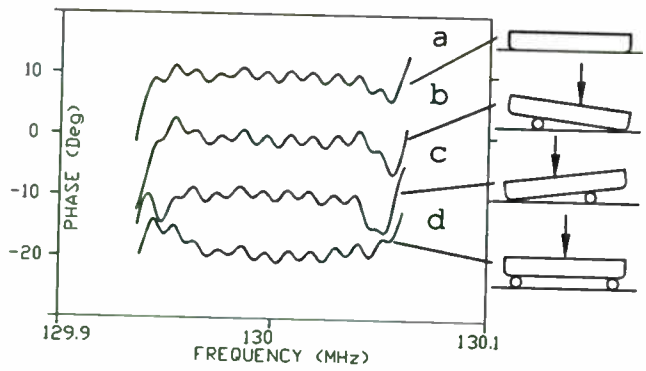

Fig. 8 - Phase characteristic of a base station filter under various mechanical loading conditions

The filter tested is at 130 MHz and is used in the transmitter chain of a CDMA base station. The amplitude and phase of S21 are shown in figs. 7 and 8 for four mechanical loading conditions. There are noticeable changes in the amplitude and phase characteristics for the asymmetric mechanical loading conditions (b and c) when compared with the unloaded condition (a). The amplitude remains nearly unchanged for the symmetrical loading (d), however the phase has a quadratic component.

The effects of mechanical stress on filter rejection sidelobes is shown in fig. 9. The top line of each plot corresponds to the 25 dB attenuation of the filter. Even though the sidelobes are only 30 dB down, the effects of mechanical package stress can clearly be seen.

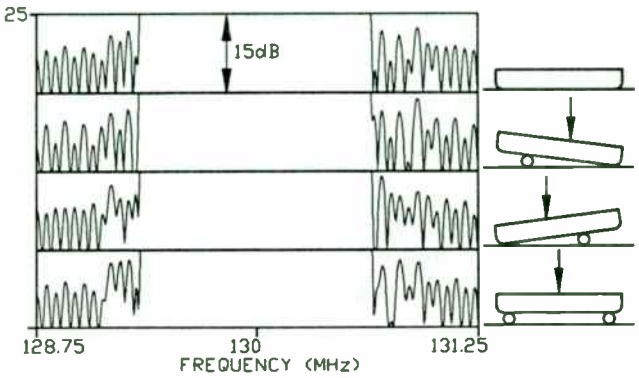

Fig. 9 - Rejection sidelobes for a base station filter under various mechanical loading conditions

VI. 160 MHz PCS TRANSMIT FILTER

Presented in this section are typical measurements on a 160 MHz transmitter filter. This filter is supplied in a 20.1 mm X 6.5 mm surface mount package. Typical performances for this filter are:

Insertion loss	21.7 dB
0.5 dB bandwidth	1.33 MHz
6 dB bandwidth	1.73 MHz
30 dB bandwidth	2.17 MHz
phase (1.2MHz)	< 3°peak-peak

This filter is used in the transmitter chain of a PCS base station. The performances easily exceed the rejection requirements of 15 dB at $f_0 \pm 1.25$MHz and 30 dB ultimate rejection. The resistors in the matching network of fig. 10a are used to obtain better than 1.5:1 VSWR.

Fig. 10a - Matching network

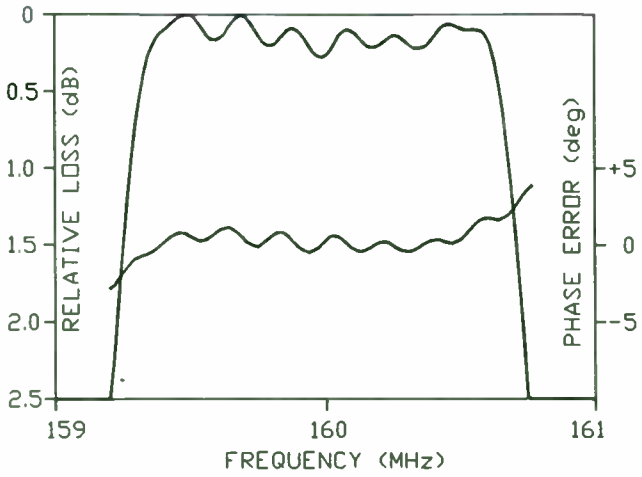

Fig. 10b - Amplitude and phase of typical 160 MHz filter

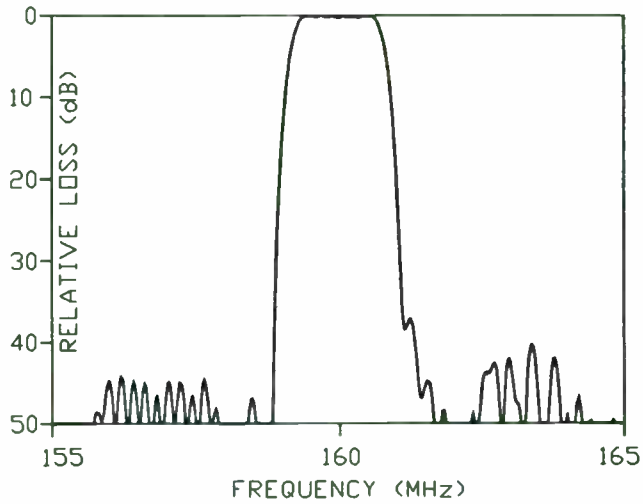

Fig. 10c - Amplitude of typical 160 MHz filter

VII. 70 MHz CDMA RECEIVER FILTER

Presented in this section are typical measurements on a 70 MHz CDMA receiver filter. This filter is supplied in a 73 mm X 19.7 mm unibody package. Typical performances for this filter are:

Insertion loss	21.0 dB
1.5 dB bandwidth	1.30 MHz
35 dB bandwidth	1.46 MHz
50 dB bandwidth	1.62 MHz
phase (1.23MHz)	< 4°peak-peak

Fig. 11a - Matching network

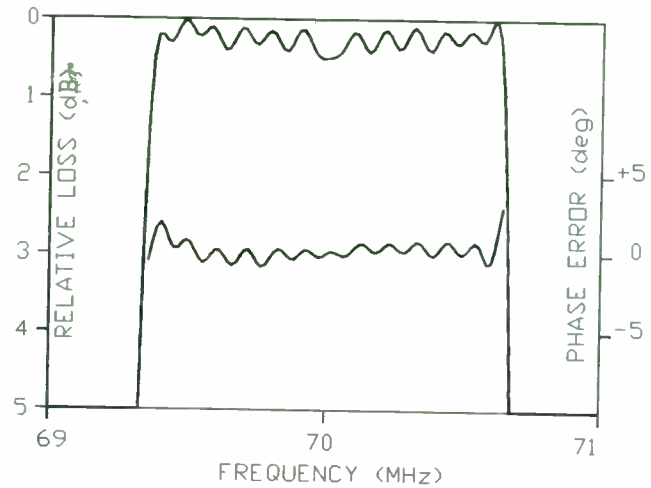

Fig. 11b - Amplitude and phase of typical 70 MHz filter

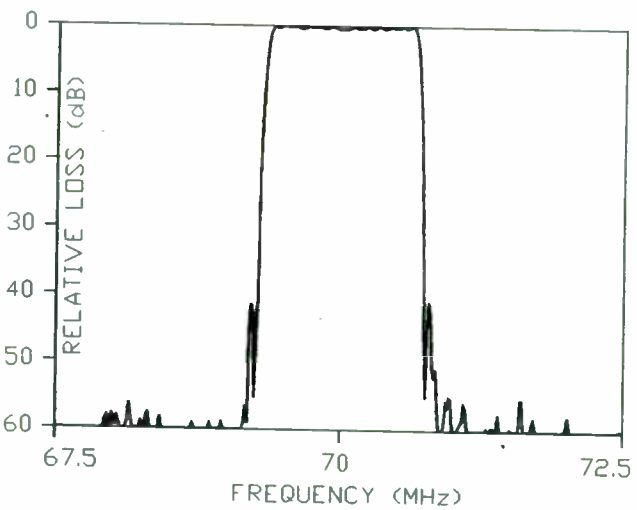

Fig. 11c - Amplitude of typical 70 MHz filter

Package stress experiments similar to those in section V were made on this filter. The changes in the rejection sidelobe levels observed were less than 1 dB for all of the package stress conditions. Passband amplitude variations were 0.2 dB and phase variations were 2°. Even with these variations the filter remained within the specifications.

VIII. CONCLUSIONS

The concept of strain on the substrate of a SAW filter has been presented. The relationship between strain and SAW wave velocity, filter delay, and filter center frequency have been discussed. The effect of package stress on the SAW substrate and the key role that packaging plays has been discussed.

A demonstration of the effects of package stresses on a 130 MHz transmitter filter has been shown for various mechanical loading conditions. Typical measurements on high performance PCS and CDMA base station filters have also been presented.

References

[1] M. Lewis, "The Surface Acoustic Wave Oscillator - A Natural and Timely Development of the Quartz Crystal Oscillator", *28th Annual Symposium on Frequency Control*, 1994, pp 304-314

[2] D.E. Cullen and T.M. Reader, "Measurement of SAW Velocity versus Strain for YX and ST Quartz", *1975 IEEE Ultrasonics Symposium Proceedings*, pp 519-522

[3] T.M. Reader, D.E. Cullen, and M. Gilden, "SAW Oscillator Pressure Sensors", *1975 IEEE Ultrasonics Symposium Proceedings*, pp 264-268

[4] B.A. Auld, *Acoustic Field and Waves in Solids*, Vol 1, Ch 1, John Wiley & Sons, New York, 1973