Proceedings of the Second Annual *WIRELESS* Symposium

FEBRUARY 15-18, 1994
SANTA CLARA CONVENTION CENTER, SANTA CLARA, CA

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ACKNOWLEDGMENTS

Doing something a second time does not necessarily make the task any easier. But in organizing the Second Annual WIRELESS Symposium, the final results certainly made for a more rewarding experience, especially with the help of the Program Chairpeople who gave so willingly of their time before and during the conference.

Special thanks is also in order for each and every WIRELESS author and presenter. In these demanding days of competitive business, time is precious, yet each of these authors made the extra effort to prepare presentations and travel—sometimes great distances—to the Santa Clara Convention Center. Their efforts will continue to fuel the growth of the many emerging wireless markets.

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Analog and Mixed-Signal ICs for Wireless Communications

Session Chairperson: Mark McDonald,
Wireless Communications, National Semiconductor (Santa Clara, CA)

PR/DP - N93/178B

Second Annual WIRELESS SYMPOSIUM
Santa Clara Convention Center (California) - February 15-18, 1994

A 3 V RF FRONT-END GaAs MMIC FOR DCS 1800 CELLULAR COMMUNICATIONS

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Abstract

An integrated class II RF front-end including a 500 mW power amplifier has been designed and fabricated for the Digital Cellular Communication System operating at 1800 MHz (DCS 1800) using the standard Philips Microwave Limeil (PML) enhancement and depletion modes ER07AD process. The IC operates at 3 V supply voltage and includes RF functions of both the Rx (Receive) and Tx (Transmit) chains. This paper describes the design and experimental performance of the circuit, which constitutes, to the authors' best knowledge, the first monolithic 3 V RF front-end for DCS 1800 cellular communications.

Introduction

RF Integrated Circuits for cellular communications will constitute a considerable market for the semiconductor industry in the 1995-2000 period, where GaAs technology will play an important role. Indeed, it is now widely considered that GaAs MESFET technology is particularly well suited for the implementation of the Tx power stages, where high efficiency amplification is required, and several Power Amplifiers (PA) have already been reported at L-band. This holds particularly true since the volume and weight reduction of the mobile terminals leads the battery supply voltages to decrease steadily to 3 V. Arguments for a monolithic implementation of a complete Rx-Tx front-end are manifold :

- a power stage uses transistors with high periphery even at medium output power (0.5 to 2 W) and therefore occupies a relatively large area of semiconductor, typically 2 to 3 mm^2 for a 0.5 W three-stage power amplifier at L-band [1]. The integration of low power RF functions (Low Noise Amplifier, Local Oscillator and even Rx and/or Tx mixers) can therefore be implemented at a marginal cost in terms of semiconductor area, thus resulting in a cheap one-package solution for an integrated RF front-end
- In almost all cellular communication standards, Rx and Tx channels use 2 separate frequency bands and are alternatively switched. They never operate simultaneously, which excludes cross-coupling interference problems.
- GaAs enhancement mode MESFET technology leads to excellent power consumption performance allowing the use of low cost plastic packaging required for these consumer products.

General architecture

The block diagram of the designed RF front-end is shown in **Figure 1**. In addition to the Power Amplifier, the Tx stage includes an up converter (MTx) mixing the Local Oscillator frequency LO and the Intermediate Frequency IF_Tx, which is set to 400 MHz. The LO frequency is generated by a Voltage Controlled Oscillator (VCO); it is tuned by an external resonator into a frequency plan ranging from 2110 MHz to 2185 MHz. An external filter is inserted between the MTX output RF_Tx and the PA input PA_IN in order to remove the signals generated in the image bandwith from 2510 MHz to 2585 MHz.

The Rx stage consists of a Low Noise Amplifier (LNA) and an Image Reject Mixer (IRM). The RF input RF_Rx has a bandwidth from 1805 MHz to 1880 MHz, while the IF output IF_RX is set to 300 MHz, thus resulting in a LO frequency in the range of 2105-2180 MHz. Therefore, as the same VCO is used for both Tx and Rx modes, LO frequencies between 2105 MHz and 2185 MHz have to be available.

Moreover, a 128/129 dual-modulus prescaler is implemented on chip in order to generate from the LO frequency an output signal of around 17 MHz, which is compatible with standard synthesizers.

The supply voltages of the Rx and Tx chains are alternatively switched off by depleted FETs controlled by an external signal.

Circuit fabrication

The DCS 1800 RF front-end has been fabricated using PML's 0.7 μm MESFET ER07AD process. This process uses 3" LEC wafers, gate recessing, Si^+ implantation, boron isolation, standard photolithography, dry etching and enhanced lift-off techniques. It is especially suited for low power L-band to C-band mixed analog/digital applications. Enhancement mode transistors (E-FET) and depletion mode transistors (D-FET) are available in this process, which both have a typical F_T of 17 GHz. The E-FET threshold voltage is V_t = 0.175 V and the drain current is 50 mA/mm at Vgs = 0.7 V. The D-FET, which is mostly dedicated to power applications, has a threshold voltage of -2.0 V and an associated drain current of 200 mA/mm at Vgs = 0 V. A photograph of the IC is shown in **Figure 2** , the chip size is 2.5 mm x 2.5 mm.

Power Amplifier

The PA design is designed to reach an output power of over 27 dBm and a Power-Added Efficiency (PAE) higher than 30 % in the DCS band (1710 MHz-1785 MHz) under a 3.3 V supply voltage. The input power at PA_IN is set to 0 dBm.

The design of the three-stage PA is based on the high power-added efficiency of the D-FET in saturated class-AB and makes use of harmonic enhancement for the interstage matching circuits (**Figure 3**). The sizes of the D-FETs are fixed to insure power output capability as well as saturation. Feedback circuits are positioned between the drain and the gate of the depleted transistor in order to insure low frequency stability. The last output matching network is chosen to be implemented externally because of the 9 mm gate width output transistor in order to lower losses. Furthermore, the power gain of the PA can be adjusted by applying gate voltages between -2 V and -1 V on the nodes VG1, VG2 and VG3 for a total gate current less than 0.5 mA.

The PA performance has been measured at 1.8 GHz under 3.3 V and the results are presented in **Figure 4**. For 0 dBm input power, the measured output power is around 27 dBm and the PAE is higher than 34 %.

Tx stage

A Colpitts type VCO, which is well suited for low supply voltages, is used. The positive feedback is achieved via a capacitive bridge between gate and source of the E-FET. Two varactor diodes are integrated on the IC and the LO frequency is determined by the external resonator and the control voltage CTRL_VCO. Measurements on a similar VCO shows a phase noise of -100 dBc at 100 kHz frequency offset (**Figure 5**). The signal delivered by the VCO is fed into the up converter MTx via 2 differential amplifier stages.

The MTx stage is a double-balanced Gilbert cell with a differential IF stage designed with D-FETs because of the large amplitude (0 dBm) of the input signals IF_Tx. The RF output signals are taken on the drains of the mixing transistors and are then combined into a low input impedance push-pull stage. The loads of the Gilbert cell are LC parallel networks tuned at the required RF_Tx frequency band OL-IF_Tx (1710 MHz-1785 MHz). Thus, the amplitude of the signals in the image band OL+IF_Tx (2510 MHz-2585 MHz) is reduced before being filtered externally.

The simulated DC power consumption of the complete Tx stage is around 210 mW.

Rx stage

The LNA consists of 2 cascaded E-FETs biased via a resistive bridge which achieves the best trade-off between gain and noise figure. A feedback loop is added for the stabilization of the operating points. The input matching of this cell is achieved via an external inductance. The LNA integrates an Automatic Gain Control, thus providing a conversion gain from -6 dB to 17 dB from the whole Rx chain by applying an input voltage between 0 and 3 V at the pin AGC_RF.

The IRM removes by phase cancellation the undesired signal and noise generated at the RF frequency OL+ IF_Rx. It consists of 2 double-balanced Gilbert mixers with a RF differential stage with one grounded input. The first Gilbert cell mixes the LNA output with the VCO complementary outputs, the second one with the LO complementary signals phase shifted by 90°. After mixing, the four phases of the IF signals are available. Two of them with a phase difference of 90° are combined with the two others via a differential stage so that the adjacent RF image band is rejected.

The IRM requires therefore the quadrature phase shifting of the LO signals. Each phase shifter is a RC network and integrates a phase adjustment pin for optimum phase balance. Amplifier stages are added to the phase shifters so that the phase shifted signals have the same amplitude as the non phase shifted ones.

The measured performance of the Rx chain indicates a DSB noise figure less than 7 dB, a typical 1 dB compression point of -30 dBm with respect to the input at 1.8 GHz and an input third order intercept point higher than -22 dBm. **Figure 6** shows that an image rejection higher than 25 dB is obtained for a conversion gain of 16.3 dB at 1.8 GHz. The measured power consumption of the Rx stage is less than 135 mW under 3 V supply voltage.

128/129 dual-modulus prescaler

The proper division range 128/129 is obtained by 3 cascaded dividers and a pulse swallowing technique, as indicated in the **Figure 7**. A control logic driven by the input pin CTRL_PR ensures correct toggling of the divider by 5/6. The design goal is to reduce significantly the power consumption of the prescaler. The use of dynamic logic is therefore required [2]. A dynamic flip-flop is easily implemented using 2 transmitting gates and 2 Direct Coupled FET Logic (DCFL) inverters as shown in **Figure 8.** The divider by 5/6 (operating at the highest frequency) and the divider by 4 use dynamic flip-flops. The dynamic logic is limited by a minimum operating frequency of around 500 MHz given by the discharge time of the flip-flop noninverting stage. This limitation is alleviated by adding a memory cell in parallel to the dynamic flip-flop leading to semidynamic flip-flop (**Figure 9**). The divider by 6 has been designed with such flip-flops.

Moreover, as the DCFL gates requires only a 1.5 V supply voltage, a middle node VDB = 1.5 V is generated on chip via a resistive bridge. The divider by 5/6 is implemented between VDB and 3 V, and the 2 other dividers between the Ground and VDB in order to reduce the prescaler power consumption.

The division of frequencies from 1.9 GHz to 2.3 GHz under 3.0 V with a power consumption of around 15 mW is obtained.

Conclusion

A fully monolithic 3 V class II DCS 1800 RF front-end integrating a 500 mW power amplifier, a Rx low noise amplifier and image rejection mixer, a Tx up converter mixer as well as a voltage controlled oscillator and a PLL dual modulus prescaler is demonstrated. Performance compatible with its integration in a DCS 1800 terminal is obtained, thus demonstrating the validity of the monolithic approach. A low cost, SMD packaged, simplified version will be introduced on the market by the end of 1994.

Extensive experimental data will be presented at the conference.

Acknowledgements

This project has been designed for Matra Communication and supported by the DRI (Direction des Relations Industrielles, France Telecom). The authors would like to thank François-René Humbert, Pierre-Jean Séverin and André Jolivet at Matra Communication for their fruitful

cooperation. They are grateful to Marc Grillaud and Marcel Pertus for their effort in the layout, assembly and testing of the circuit.

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[2]M.Rocchi et al., "GaAs Digital Dynamic IC's for Applications up to 10GHz", *IEEE Journal of Solid-State Circuits*, vol. SC-18, no. 7, pp. 355-356, March 1986.

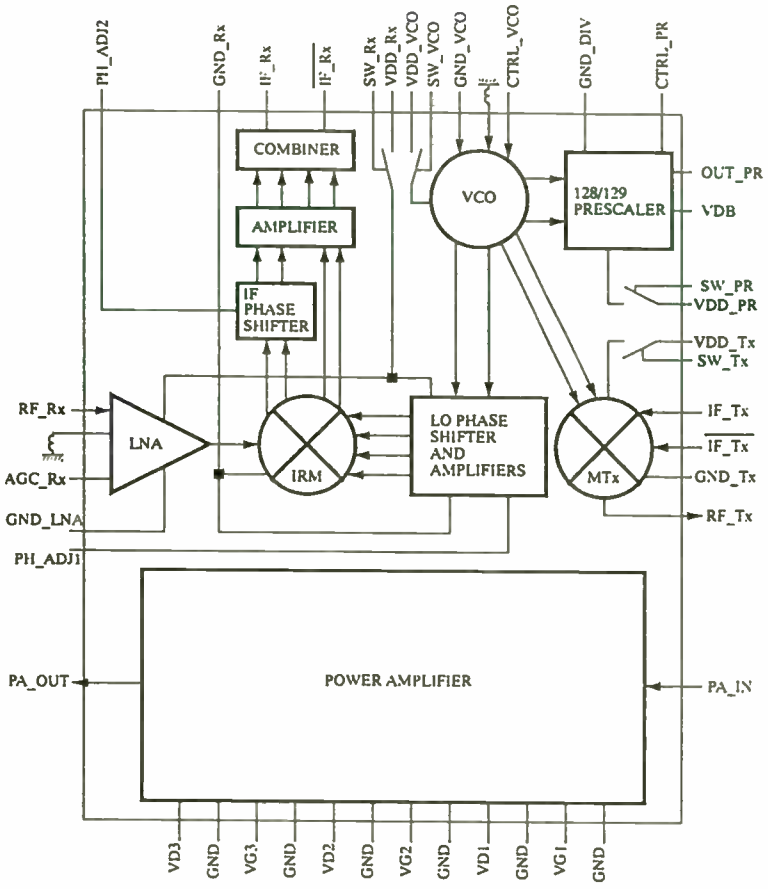

Figure 1 : Block diagram of the 3 V DCS 1800 RF front-end IC

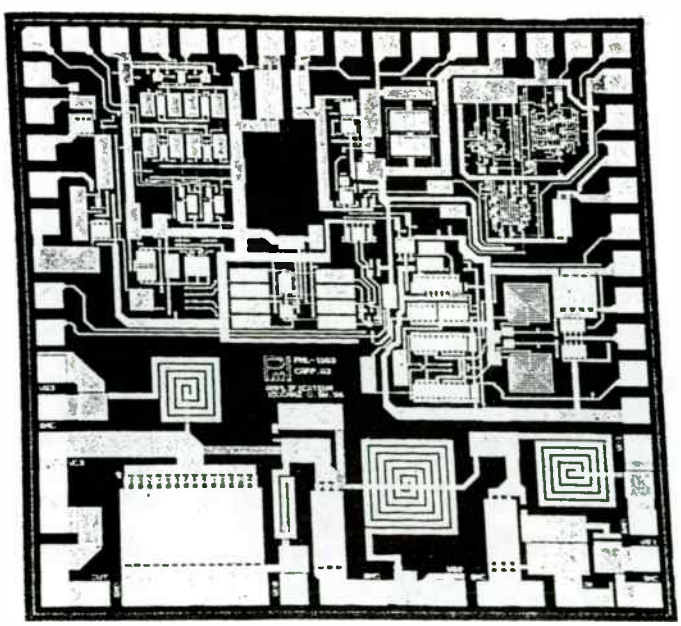

Figure 2 : Photograph of the 3 V DCS 1800 RF front-end IC

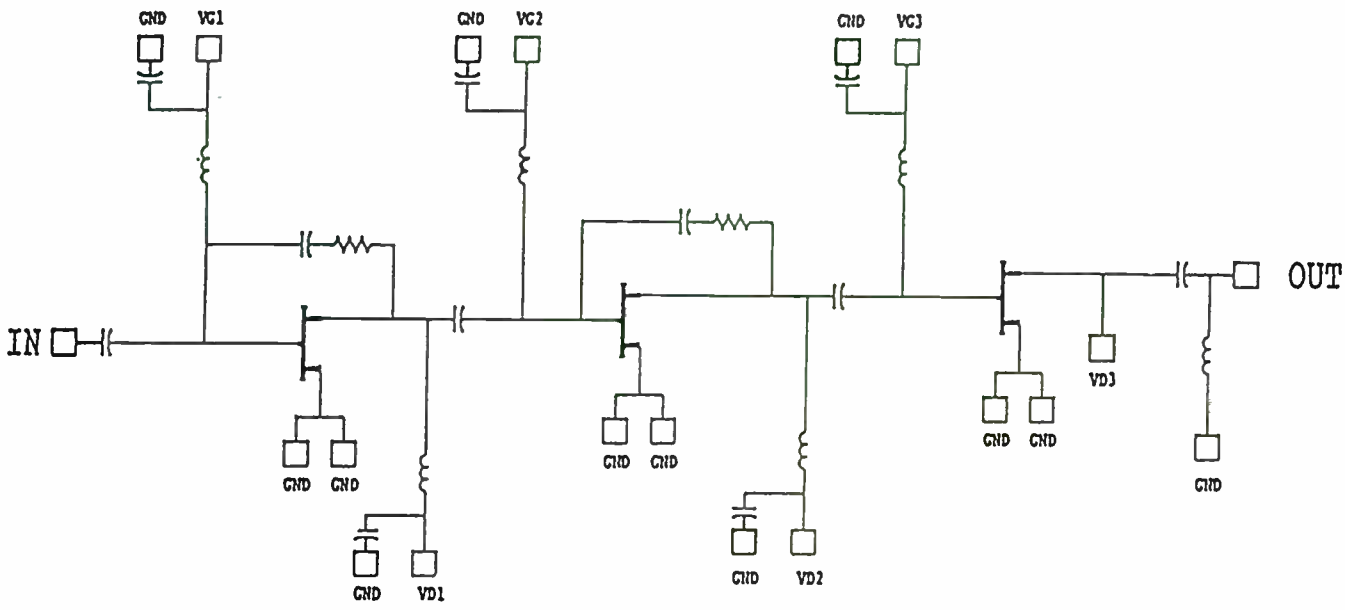

Figure 3 : Block diagram of three stage power amplifier

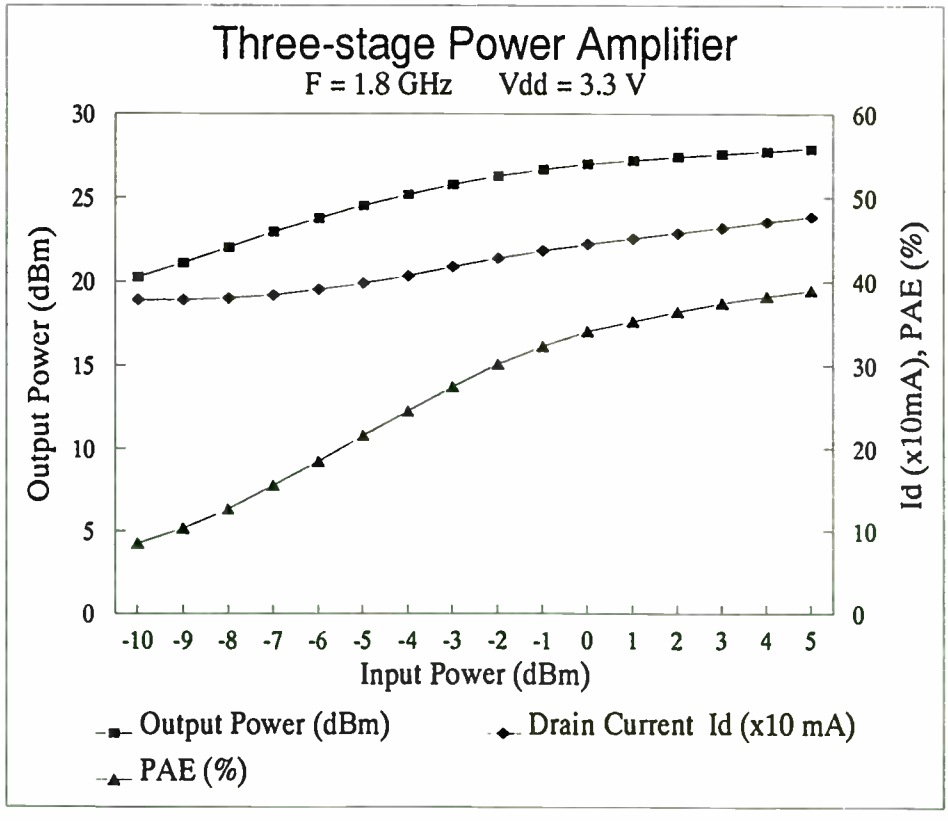

Figure 4 : Output power, PAE and drain current curves versus input power

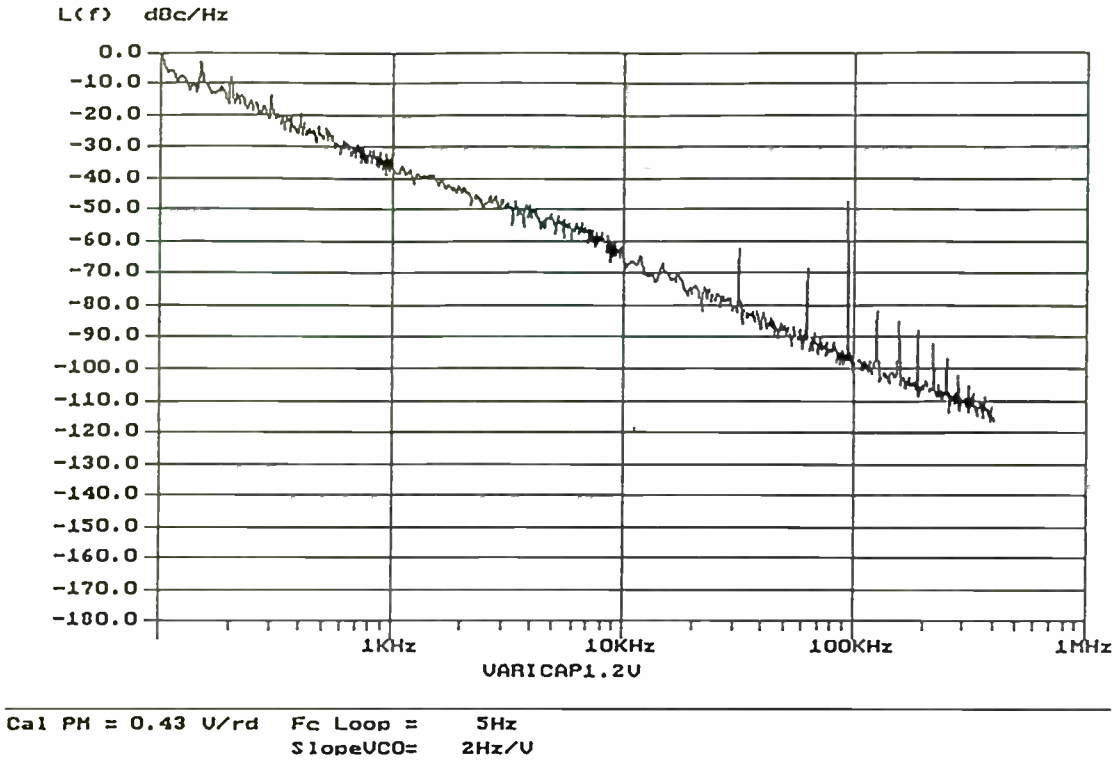

Figure 5 : Phase noise of the Voltage Controlled Oscillator

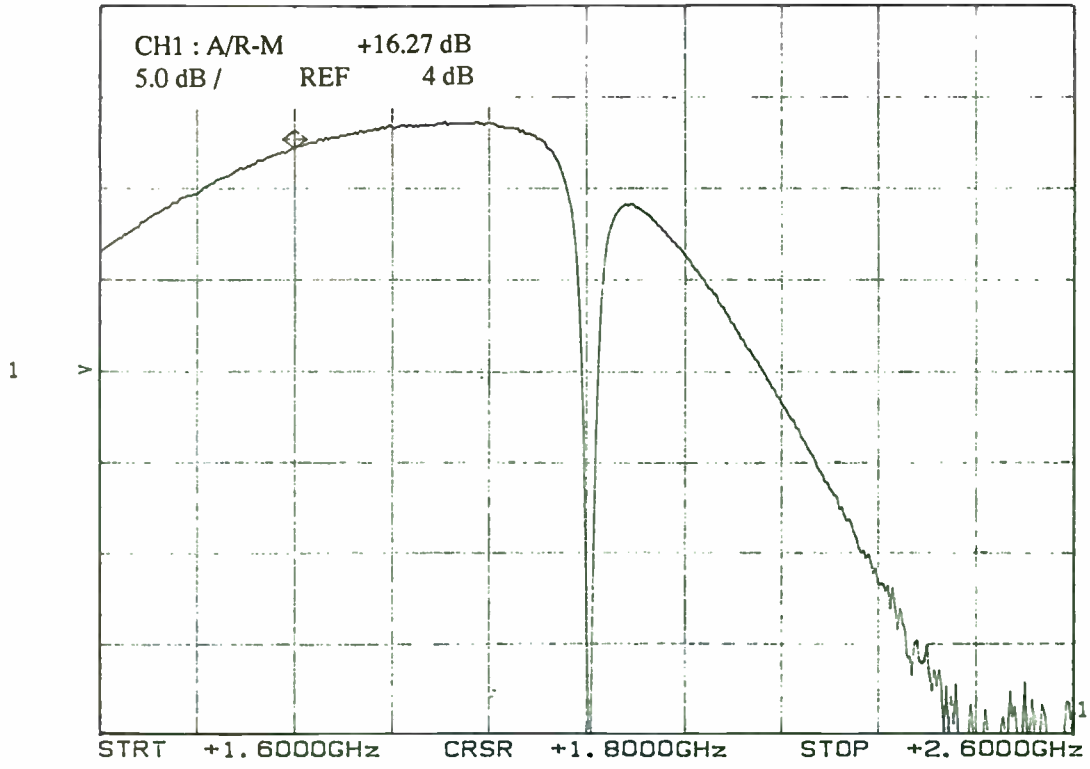

Figure 6 : Conversion gain vs RF frequency for a fixed LO of 2100 MHz

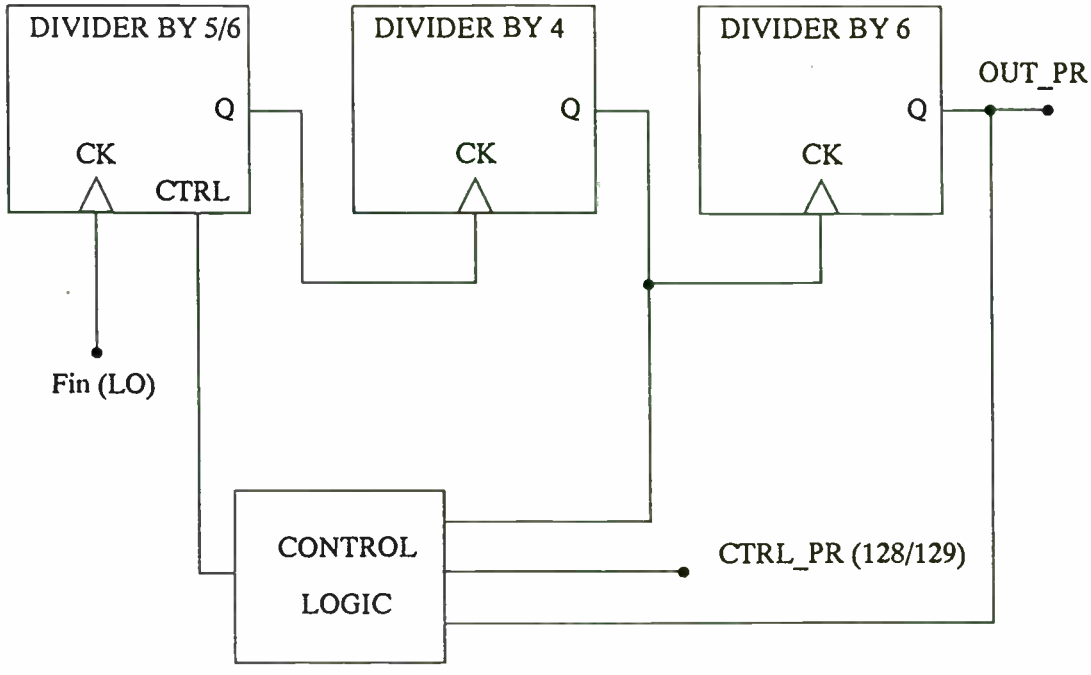

Figure 7 : Block diagram of the 128/129 dual-modulus prescaler

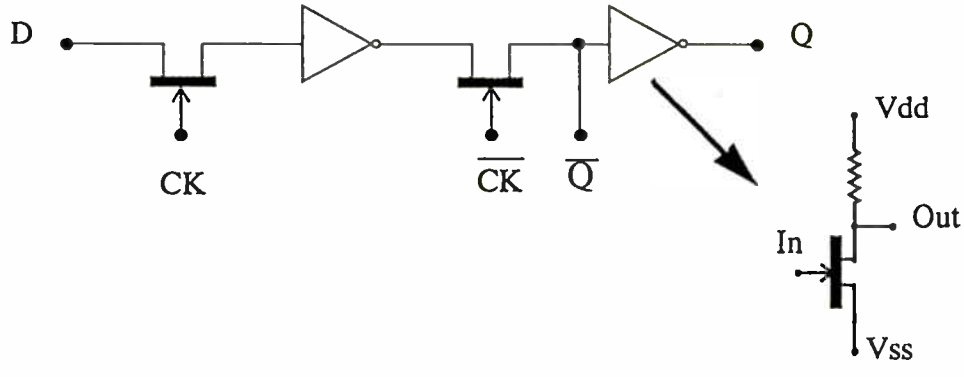

Figure 8 : Block diagram of the dynamic flip-flop

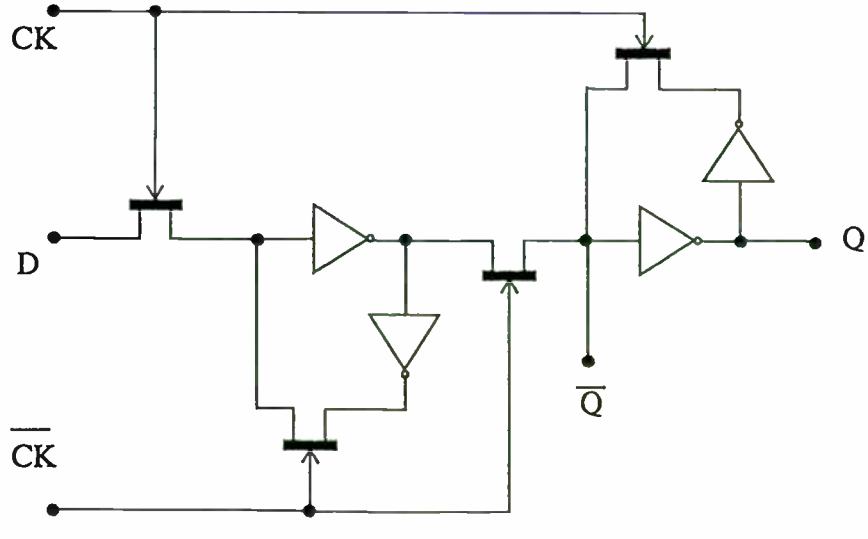

Figure 9 : Block diagram of the semidynamic flip-flop

Push-Pull Receiver Input Amplifier Stages -- The Solution to Intermod Problems

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Today's battery operated handhelds require an optimal sensitivity, an excellent large signal behaviour and an extremely low dc power consumption. But as normally the large signal behaviour is directly combined to dc current, there exists a system boundary that could not be passed up to now.
The new circuit offered here allows an increase in IP3 of 17dB at 8mA dc current with almost no decrease in gain, noise behaviour or reverse isolation. IM2 behaviour is improved as well as higher order intermodulation (see table below).
These results are achieved with a push pull complementary grounded base arrangement. A NPN bipolar transistor and a pnp bipolar transistor operate as parallel amplifiers for high frequency signals. If the supply current through both devices is equal, the intermod distortions compensate each other to a certain extent and therefore a nearly ideal linear amplifier is built. The same current through both devices is achieved by simply switching both transistors in series. One can connect either the emitters or the collectors of both transistors. Both circuits are equivalent in their electrical behaviour, so that practical aspects like operating point stabilization or signal handling may decide what is preferred. For a correct function, the parallel ac operation must be maintained down to the lowest difference frequency of two possible input signals.
The transistors need not be matched, just taking similary types is sufficient. The resulting noise figure is about the mean value of the noise figure of the npn- and pnp-device.
Taking over these results to FET-devices suffers from the fact that matching becomes necessary, as FET devices do not follow the Shockley's equation.
It is planned to extend these results from amplifier devices to mixer devices. First results are quite promising.

device	MOSFET	BJT	Push Pull BJT
circuit	grounded source	grounded base	grounded base
source imp.	500 Ω	50 Ω	50 Ω
F/db	0.8	1.0	1.2
Gain/dB	20	10	10
IP2/dBm	26	46	51
IP3/dBm	0	10	27(=0.5W)
IP5/dBm	-9.5	9	18

Table 1: Comparing different devices as receiver input stages at 100MHz and 8mA biasing current (measurement values)

A low-voltage IC front-end for cellular radio

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Today's portable cellular users are demanding smaller, lighter phones with loner talk time. In response, cellular phone manufacturers are forced to use highly integrated and low-voltage ICs in their designs. The Philips SA601 front-end IC fulfills these needs by incorporating a high-performance LNA and mixer in a single 3-V device. The SA601 can be combined with the Philips SA606 (low-voltage FM/IF) and SA5752/SA5753 (low-voltage audio processor chipset) to form a complete 3-V receiver section which meets AMPS specifications.

This presentation will discuss the importance of a high-performance integrated front-end to meet the strict requirements for cellular radio. Additionally, SA601 performance graphs will be shown along with performance graphs for the entire cellular receiver.

A Monolithic Quadrature Demodulator and Digitizer for PSK and QAM Applications

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Abstract

The signal conditioning and processing required in modern QPSK and QAM modems is performed by imbedded low cost, high performance digital signal processors. Sample rates exceeding 60 MHz (I/Q), representing input bandwidths up to 45 MHz, can now be supported in consumer grade products. The pre–processing task required of a DSP based modem is the transformation (or transduction) of the modulated input signal from an input IF carrier to a pair of quadrature baseband analog to digital (A/D) converted data streams. While conceptually simple to implement, this conversion represents a formidable challenge at the 60 MHz sample rate. This transformation, requiring a quadrature spectral translation, anti–aliasing filtering, sampling, quantization, and binary coding has been implemented by a versatile, highly integrated, mixed mode integrated circuit which we introduce and discuss here.

Introduction

Digital signal processing (DSP) techniques are being applied to the implementation of various stages of radio receivers (and in particular, modems) for a number of reasons. These include improved cost–performance considerations, reduced costs of manufacturing, alignment and testing, reduced inventory requirements in support of a product line, low cost for product enhancements, and ease of incorporating growth features.

Modems can be implemented incorporating various degrees of imbedded DSP. The interface between the analog and digital portions of the modem is the analog to digital converter (ADC). The location of this interface is related to the required performance parameters of the converter. The most important parameters are signal bandwidth and signal to noise ratio which define, respectively, the necessary sample rate and effective number of bits required for the conversion. Additional considerations are stability of the sampling clock, aperture uncertainty, quadrature channel matching, and the cutoff frequency of the quantizer networks. Subject to satisfying these considerations it is desirable to locate the analog to digital interface as early in the processing chain as possible.

Conventional quadrature receiver architectures designed to leverage the advantages of DSP have relied on separate functional blocks for the IF gain, quadrature demodulation, baseband filtering, I and Q sampling, clock generation, and local oscillator subsystems, resulting in considerable complexity and cost. This traditional implementation is particularly unsuited to a volume production environment due to the difficulty of achieving repeatable amplitude and phase matching of I and Q channels without post–assembly adjustments.

We discuss here a highly integrated component that provides IF to baseband quadrature demodulation, anti–aliasing filtering, and A/D conversion on a single monolithic die. The high level of integration, combined with superior specifications, provides a reliable cost effective solution for the most demanding of vector modulated digital receiver applications.

Architecture

Functional Description

The component can be functionally divided into two block diagrams, illustrated in figures 1 and 2. The analog signal conditioning, consisting of IF processing, quadrature demodulation, baseband lowpass filtering, and buffering functions are shown in figure 1. The ADCs and supporting circuitry are illustrated in Figure 2.

IF Quadrature Demodulator

We now present details of the quadrature demodulator block of the component which is shown in figure 1. This block integrates the IF processing functions which includes a controlled input impedance amplifier, a variable gain amplifier, and matched mixers to produce the I and Q baseband signals. The block also includes an integrated VCO, a divide–by–16 frequency prescaler, and an active phase shift network which forms the quadrature LO signals. The final portion of this block contains a pair of integrated active low pass filters and baseband amplifiers to supply the drive levels required by the ensuing ADCs.

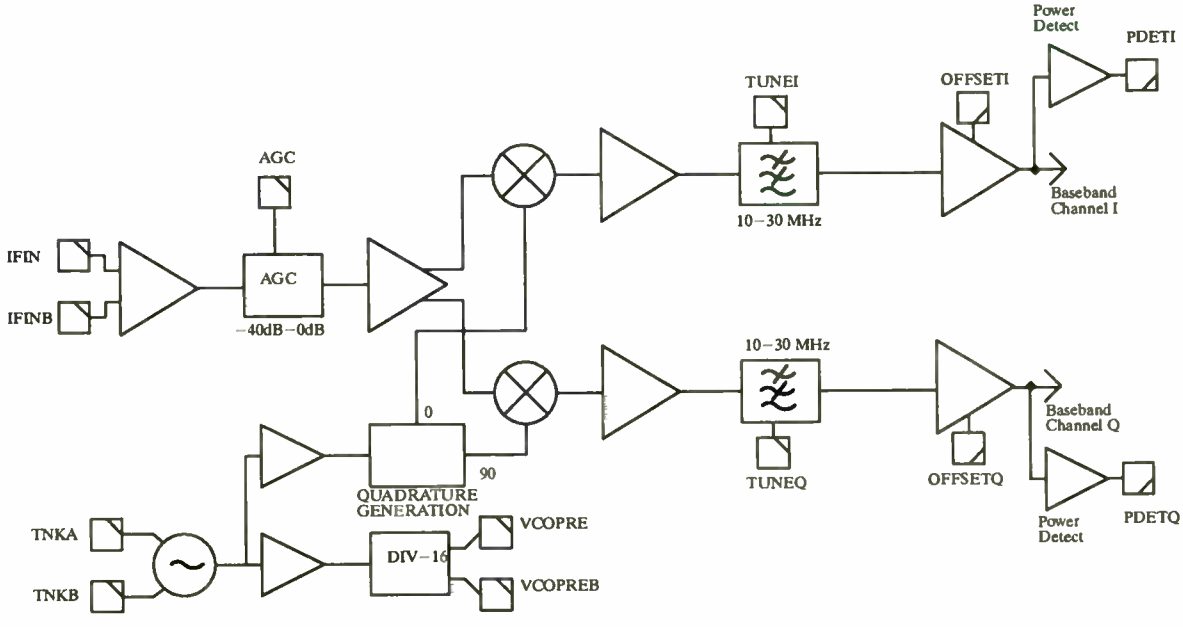

Figure 1: IF Quadrature Demodulation Network

The IF input amplifier is a wide bandwidth 50 ohm input impedance amplifier with sufficient insertion gain and linearity to provide an IIP3 of +5 dBm for an expected input power of –10 dBm. Differential inputs are provided, but single–ended drive is accepted with proper termination of the unused input. A variable gain cell follows the input amp. This cell uses a modified double balanced mixer topology to provide an attenuation range in excess of 40 dB. An amplifier follows the variable gain cell to provide additional gain and drive to the mixers. Linearity is enhanced by a current feedback topology and by buffering the degeneration resistors. A classic double balanced mixer cell is the core of a baseband power detection function, provided for each of the two channels. A differential to single ended converter drives the on board gyrator filters.

The negative resistance amplifier of a resonant tuned oscillator is provided on chip. A differential topology is utilized to provide maximum interference rejection. The oscillator is buffered, and drives a quadrature generation network as well as a divide–by–16 prescaler.

A variation of a phase lock loop topology is utilized in the quadrature generation circuitry to provide the stringent phase error specifications called for in this design. This architecture uses a variable delay element, a

phase detector, and an integrator in a feedback loop to lock the I and Q LO signals at 90 degrees phase difference.

A fully integrated 5th order Butterworth low pass filter is realized using a gyrator topology. The cutoff frequency is adjustable from 10 MHz to 30 MHz. The filters for each channel are independently adjustable.

The baseband amplifier, one each for the two channels, provides 29 dB of gain to drive the A to D converter. The amplifier exhibits a 3 dB bandwidth in excess of 120 MHz, providing a maximally flat response from DC to 20 MHz. Each amplifier has an offset adjustment to compensate for any offsets introduced by the filters.

A/D Converter

The dual ADCs and supporting circuitry are shown in figure 2. This block integrates two matching 6 bit flash ADCs, the clock generation network, and all the bias and reference generation circuitry.

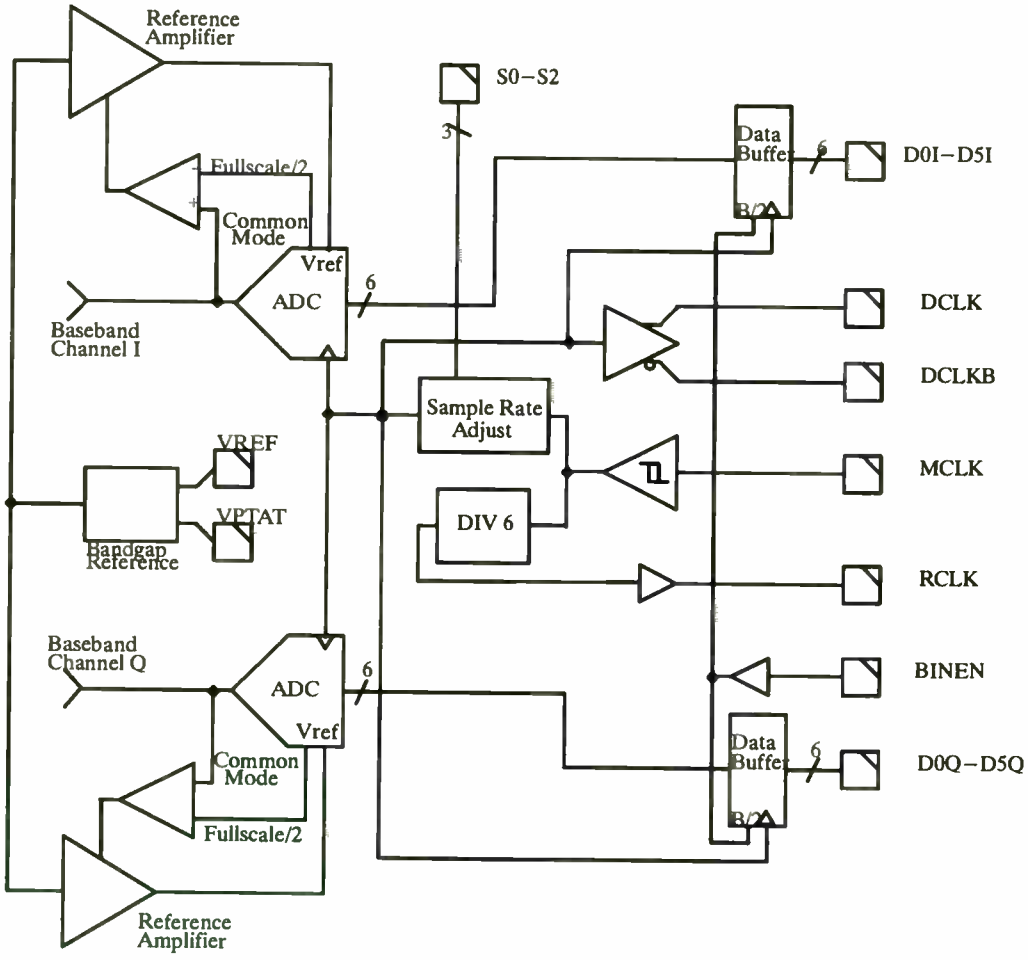

Figure 2: Dual ADCs and Supporting Circuitry

Each ADC provides 6 bits of resolution, and is implemented using a full flash topology. All signal paths in the converter are balanced to minimize common mode interference and eliminate ladder droop. The converter uses a Thermometer to Grey to Binary decoding sequence to minimize the errors due to out of sequence codes when digitizing a high speed signal. The decoding sequence is coupled with appropriate delay elements to drive metastable related errors to a statistically acceptable level. The data is latched, and is available to the user in either a 2s complement or offset binary format.

The resistive ladder, which provides the threshold voltages for the ADC comparators, is driven by an on chip reference amplifier. A ladder and reference amplifier is provided for each channel. The reference amplifiers' drive levels, derived from a bandgap voltage, define the full scale input voltage of the ADCs. The common mode levels of each reference amplifier are designed to mimic the common mode voltage of the corresponding baseband amplifier. Feedback is incorporated to insure proper common mode match between reference and signal.

The clock generation network accepts a sinusoidal input from the user, buffers and translates the signal, and drives the programmable sample rate prescaler as well as a reference clock prescaler. The programmable sample rate divider determines the actual sample rate for the ADC and the data clock out, as well as the latched output data.

Most reference and bias levels are generated from master bandgap reference cell. This cell provides supply independent biasing, and both temperature independent and PTAT bias are available. Slave reference cells provide the reference and bias signals for the various functions.

The design includes an independent single supply operational amplifier for use as determined by the user. The op amp runs on a single +10 volt supply and provides greater than 85 dB of open loop gain, 10 MHz gain bandwidth product, and less then 1 uVpp integrated noise voltage. This op amp is useful in AGC loops or for conditioning the filter cutoff frequency adjustment.

The Interface

The interface between the RF front end and the ADC consists of differential baseband signals and all reference signals necessary for the circuitry. The baseband amplifier must only drive a high impedance load, as the signal remains on chip. The power requirement of the baseband amplifier is thus considerably less than that required to drive a signal off chip into a controlled impedance environment. The monolithic solution also provides simplified bias requirements, as all gain dependant functions will track over variations in process. This eliminates the need for the user to compensate for changes in gain from part to part, and from channel to channel.

Banner Specifications

The design boasts many characteristics that have never before been achieved in monolithic form. The level of integration will simplify the job of the receiver designer by eliminating several of the traditional interfaces required by discrete designs. The high level of integration will decrease the total parts count of a design, increasing the reliability of a receiver system.

Each channel ADC provides 6 bits of resolution at a sample rate of 60 MSPS. The dynamic resolution of the converter degrades by only 0.5 effective bits for input frequencies near nyquist. The dynamic accuracy of the converter is possible due to proprietary design of the comparators and the process technology specifications. Metastable errors that might contribute to Bit Error Rate (BER) have been statistically eliminated by appropriate placement of signal regeneration. In addition, the Thermometer to Grey to Binary conversion insures that any problems in the conversion will result in at most a 1 LSB error at the output.

The quadrature generation network utilizes the PLL topology mentioned above to achieve unprecedented phase and amplitude accuracy in a monolithic quadrature demodulator.

The variable gain amplifier discussed above exhibits a range of attenuation from –3dB to an excess of –43dB, thus delivering an input dynamic range in excess of 40dB.

The filters are realized utilizing a gyrator topology and implement a fifth order Butterworth response. The cutoff frequency of the filters can be adjusted between 10MHz and 30MHz via an analog input. The variable

cutoff characteristic is useful in multi–sample rate situations, where the baseband signal has a predetermined bandwidth. The integrated filters provide superior channel to channel matching, in addition to simplifying the overall system design.

Isolation Issues

A design with this level of complexity will provide many opportunities for unwanted coupling between various functions of the chip. The majority of these isolation issues involve the digital outputs and the associated harmonic energy coupling into the circuitry in question, either through the substrate or via the package parasitic capacitance and mutual inductance. Several design techniques were utilized to minimize the effect of coupled signals, including the use of differential topologies for all analog and digital signals. Differential I/O was used wherever possible to increase isolation through the package and on the board. The digital outputs have been designed with controlled rise and fall times into well defined loads to limit the harmonic energy. The integrated filters, where the signal path is single–ended, utilize grounded capacitors to take advantage of a parasitic PN junction, thus increasing the substrate isolation. The prescaler divide ratio was chosen such as to guarantee the prescaler frequency does not fall in the baseband. Finally, separate supplies are brought out of the package to insure sufficient cell to cell supply rejection.

Results

Chip Statistics

The die measures 156 x 129 mils^2, and a die photograph is shown in figure 3. The design integrates 500 cell instances and utilizes 10,000 transistors and 10,000 passive elements. The component dissipates 1.3 watts at room temperature, and is packaged in a 100 pin MQFP.

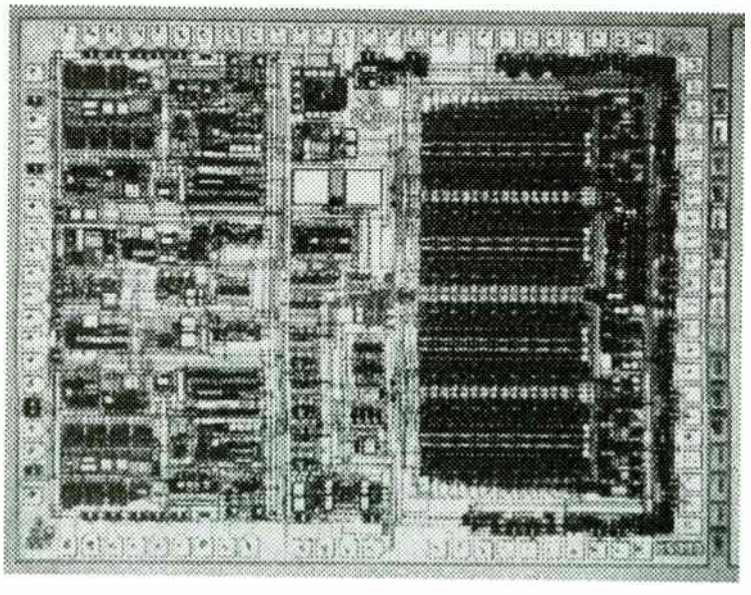

Figure 3: Quadrature Digitizer Chip Photograph

The design is fabricated on a trench isolated, double poly–silicon, bipolar technology. The NPN transistors exhibit a nominal f_T of 14 GHz, and may be scaled to a minimum area of 8 x 12 μm^2. At this minimum size the junction capacitors have the following values: Cjc = 15.5fF, Cje = 9.3fF, and Cjs = 11.3fF. The technology also offers lateral PNPs, schottky diodes, 200 ohm/sq poly–silicon resistors, 50 ohm/sq thin film trimmable Nichrome resistors, and MOS capacitors.

Four layers of interconnect are available, including three layers of gold and 1 ohm/sq poly–silicon. The poly–silicon and bottom two layers of gold metal may be patterned at a 4 μm pitch. The third gold layer may be drawn at a 16 μm pitch. This top gold layer is very useful for power bussing, as it is twice the thickness of the other two layers of metallization.

Measurements

Evaluation was performed on the die to determine part functionality. All major blocks of the chip were functional. The range of IF Gain vs. AGC input, shown in figure 4, enables the component to deliver greater than 40 dB of dynamic range.

The result of the quadrature demodulation process is shown in figure 5, which shows both I and Q baseband signals that are the result of a 684MHz VCO frequency and a 664 MHz IF frequency. The test environment necessitated the averaging of the baseband signals, but this will only serve to ease the measurement of any systematic quadrature phase or amplitude error. The measurements in figure 5 result in a phase error of less than 0.3 degrees and an amplitude error less than 0.1 dB.

The ADC linearity is presented in figures 6 and 7. The maximum integral linearity error and differential linearity error are both less than 0.2 LSB. The measured gain match is less than 0.05 dB.

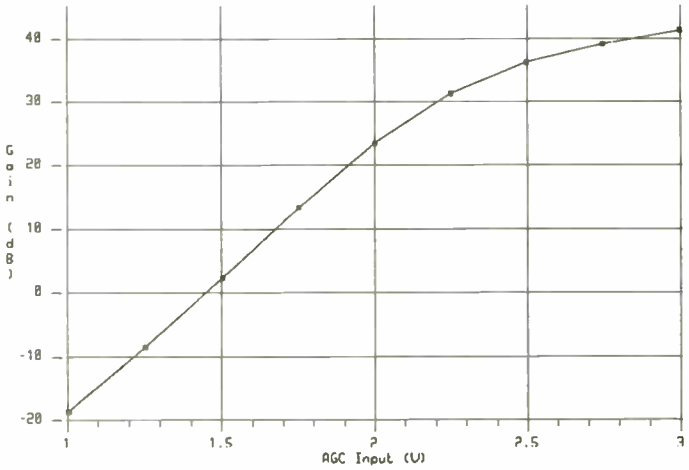

Figure 4: IF Gain Vs. AGC Control Voltage

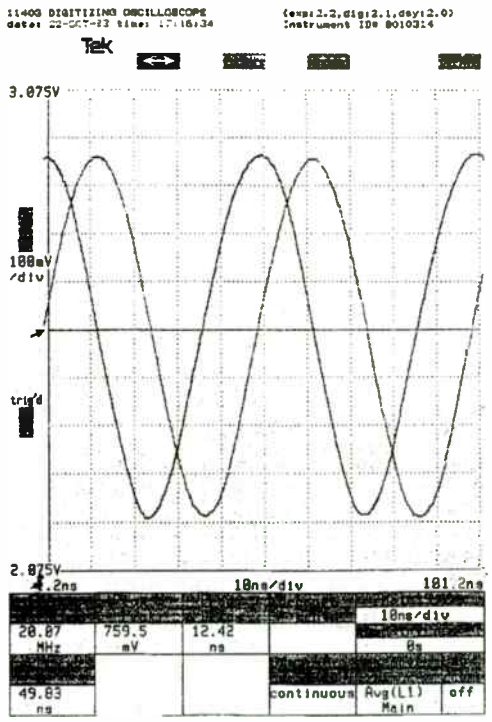

Figure 5: I and Q Baseband Signals

Conclusions

The emergence of DSP techniques that drive digital communication and data compression technology is enabling consumer and industrial applications not economically feasible just a few years ago. These markets will put cost pressure on traditional receiver implementations, thus encouraging integration of functionality. New technologies will require greater performance requirements on these functions, again requiring increased integration of traditional discrete designs. A component is described that performs the IF to baseband quadrature demodulation, anti–aliasing filtering, and digitization in a format compatible with evolving digital

demodulation and video compression standards. This design delivers exceptional dynamic range, linearity, dynamic accuracy, and is targeted for emerging QPSK and QAM applications.

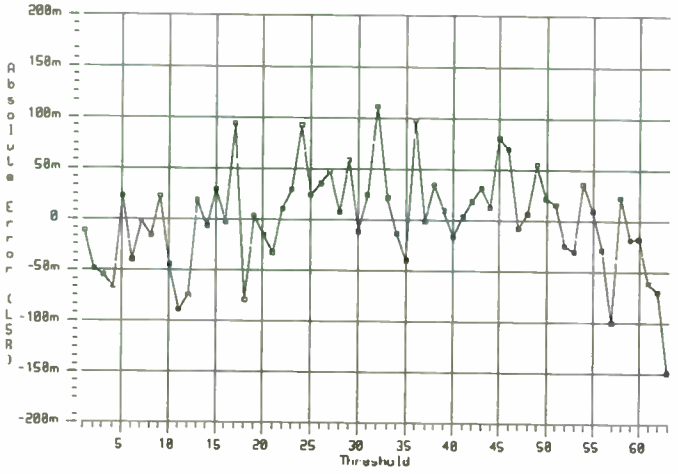

Figure 6: ADC Integral Linearity vs. Threshold

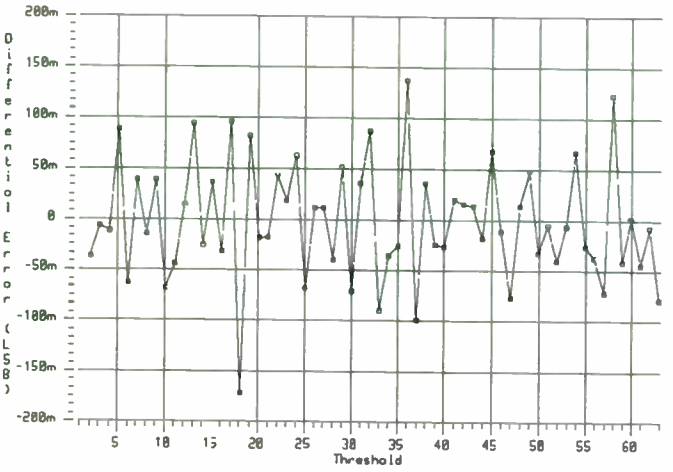

Figure 7: ADC Differential Linearity vs. Threshold

Acknowledgements

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Fractional-N Frequency Synthesizers for Next Generation Cellular and Wireless Applications

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Abstract

The phase detector comparison frequency of the described 1 GHz fractional-N PLL frequency synthesizer can be either 5 or 8 time higher than the channel bandwidth. This implies that the close-in phase noise of the carriers can be up to 14dB (20log5) and 18dB (20log8) lower than the ones generated by the traditional synthesizers. At the same time, since the reference spurs are at least 5 times further away than the next channel, wider loop filters are allowed to use, which yields a faster switching time. By simple software programming, the device can switch between two loop filter configurations, where loop responses can be designed differently in switching or steady state. Combined with low-noise and fast lock-time performance, this fractional-N synthesizer is a true winner for the next generation cellular and wireless handsets.

A 1-V CMOS FSK receiver for wireless applications

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This paper will report on an extremely low voltage (1 V) CMOS process for battery-operated wireless circuits and systems. Results will be shown for a low-current FSK receiver chip that is suitable for a variety of applications.

Microphone-to-Antenna Solutions

Session Chairperson: Robert Clarke,
Analog Devices, Inc. (Wilmington, MA)

The Applications of Advanced CMOS/CCD Technology in Spread-Spectrum Receivers

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Introduction

Recent advances in charge-coupled device (CCD) signal-processing technology, together with its merging with mainstream silicon CMOS technology, make it an attractive candidate for many functions in wireless receivers. Integrating a high-speed, low-voltage CCD with a mixed-signal CMOS process allows discrete-time analog signal processing sample rates and bandwidths to far exceed those possible with switched-capacitor filter (SCF) technology. Indeed, sample rates are increasing rapidly as the technology is scaled. We believe that as scaling progresses below 1 μm sample rates and bandwidths will equal or exceed those practical with surface acoustic wave (SAW) and acoustic charge transport (ACT) technologies. Even at these high speeds the CCD will retain its advantage of low power and precise, programmable clock control of delay.

This availability of high-speed, low-power discrete-time analog technology allows many receiver functions to be implemented more efficiently than with either pure analog or pure digital signal processing (preceded by an A/D converter). Furthermore, with the merging of advanced CCD technology with CMOS (ultimately BiCMOS) technology many receiver functions can be implemented on the same chip, each in the most appropriate technology. In this manner the highest performance/cost ratio can be achieved at the system level.

Requirements of Spread-Spectrum Communications Receivers

Spread-spectrum communications technology has long been used by the military and NASA because of the well-known advantages in the areas of security, fade resistance due to reduced multipath sensitivity, immunity to interference, and ability to accommodate more users in a given bandwidth. However, the high cost of spread-spectrum technology has inhibited its use in the commercial sector until recently. This situation is rapidly changing as a result of advances in IC technology. With the recent approval of Qualcomm's code-division multiple-access (CDMA) format as the interim standard for cellular telecommunications in North America this trend to spread-spectrum communications should accelerate. In addition, the Global Positioning Satellite system (GPS) employs spread-spectrum technology. The civilian applications of this extremely precise navigation system are growing rapidly as the cost of GPS receivers decreases. For

example, personal navigators coupled with digital mapping technology promise to revolutionize automobile driving once the cost of the technology reaches consumer levels.

In spread-spectrum systems the signal bandwidth is spread over a much wider bandwidth either by frequency hopping (FH) of the carrier or pseudonoise (PN) modulation of the signal. Communication systems have been built that use both of these spreading techniques simultaneously. Common to both types of systems is the use of error correction techniques to mitigate the effect of an occasional missed or corrupted transmission.

In the FH case the instantaneous carrier bandwidth is identical to the signal bandwidth. Accommodation of multiple users is achieved by assigning different carrier hopping patterns to the different users. For the PN case, the signal bits are modulated by a much higher frequency code (in communications jargon the bits in the PN code are called "chips," and the PN bit rate is referred to as the "chipping" rate). Hence, the instantaneous bandwidth is much wider than the signal bandwidth. A desirable result of this wider instantaneous bandwidth is that the instantaneous spectral power density is lower than in the FH case. Consequently, a transmitter causes less interference, and without error-correction coding more users can simultaneously occupy the same bandwidth. Furthermore, the direct-sequence transmitter will drop below the thermal noise floor of the receivers at a shorter range, thereby allowing greater spatial reuse options. Accommodation of multiple users is effected by assigning different PN codes to individual users. In both FH and PN cases security is added by randomizing and frequently changing the hopping patterns or PN codes, respectively.

In both types of spread-spectrum systems the receiver must collapse the spread signal and recover the original information. To perform this function in the FH scenario a hopping local oscillator (LO) is required for "dehopping" the carrier. For a fast hopper a very fast-settling frequency synthesizer is required to generate the hopping LO. For the PN case a programmable matched filter is needed to strip off the PN modulation from the signal. However, this matched filter must sample at the PN chip rate (or higher), which can be many times the bit rate of the original signal. Furthermore, when the PN code is changed rapidly the matched filter must be able to update its reference code quickly, with minimum dead time in the signal path.

In scenarios where signal acquisition time is unimportant simple serial correlators suffice for the PN case. Here, the synchronized receiver adds up appropriately-weighted samples of the modulated signal and determines whether the original signal chip was a 1 or 0. Because the acquisition time tends be very long for serial correlators [proportional to (number of chips)^{2}x(chip duration)] this approach is appropriate only for systems whose messages are long compared to the acquisition time.

In an increasing number of cases, however, rapid and frequent acquisition is required. Mobile communications and navigation systems often experience dropouts due to fading caused by buildings, bridges, tunnels, etc. Furthermore, modern digital communications systems are increasingly using packet-switching techniques to transmit data. Virtually all data transfer is packetized in new systems today. For example, the telephone system is converting to asynchronous transfer mode (ATM) technology, a form of packet switching. Such packets tend to be short (~100s of bits), and adding a synchronization sequence to each packet incurs a stiff overhead penalty that decreases

effective throughput. Consequently, parallel matched filters are often required to significantly reduce acquisition times. Such filters are able to look at a pipelined sequence of samples simultaneously and rapidly determine the point in time when the received sequence matches the stored reference. To perform this matched-filtering operation requires a massive amount of high-speed signal processing, with simultaneous delays, and multiply-adds of a large number of signal samples required. Up until recently, it has been difficult to implement programmable high-speed matched filters of the required length with acceptable throughput, power dissipation, and component count.

The sample rate required in the matched filter can be surprisingly high. Take the case of a voice signal represented by a 16-kb/s stream. If each bit in that stream is modulated by a PN code of length 256 then the resulting stream has a bit rate of 4.1 MHz. This information must be sampled at a minimum of 4.1 Ms/s (and often at twice that rate).

The situation for Ethernet is even more dramatic: if the 10-Mb/s data stream is modulated by a 12-bit PN sequence the resulting stream must be sampled at a minimum of 120 Ms/s. The FCC mandates that a spreading factor of at least 10 be used in wireless spread-spectrum communication systems, and the limit on transmitted power in the allocated slots is 1 W. The C-band (5.400-5.525 GHz) bandwidth allocation is 125 MHz, the S-band (2.400-2.4835 GHz) allocation is 83.5 MHz, and the L-band (902-928 MHz) allocation is 26 MHz. For highest data rates the maximum bandwidth allocation should be used, and to do so will require very high-speed matched filters.

At the other end of the transmitted power budget are spread-spectrum systems intended for low-power inter- and intra-building and personal communication systems. Here, the extremely low limit on transmitted power (~1 mW), coupled with the multipath environment common in buildings, severely degrades the signal-to-noise (S/N) ratio. The instantaneous power limit is too low for FH systems to be used effectively. To mitigate the effects of low power and multipath, PN systems with long codes are desirable because the noise and interference typically are uncorrelated to the PN code used to modulate the signal. Therefore, the S/N power ratio improves by the number of PN chips per bit. For example, a PN code of length 256 increases the S/N by 24 dB.

Because increasing the spreading bandwidth improves all of the desirable features of a spread-spectrum communications system there is inexorable pressure to build faster, wider-bandwidth systems. This trend, however, conflicts with the requirements of wireless systems: low power and low cost. Hence the need to implement each function as efficiently as possible.

Finally, modern digital communications systems tend to have "bursty" data. Packet radio is a good example of such a system. If the duty cycle of the data is low enough it would be desirable to absorb and store the burst but process the signal during dead time at a bandwidth or data rate lower than that of the incoming signal. At a 50% duty cycle there is no advantage (readout rate must equal input rate). However, as the duty cycle decreases below 50% the readout rate can be significantly reduced. At a duty cycle of 1/3 the readout rate can be half the input rate. At a 10% duty cycle the readout rate can be $1/9^{th}$ of the input rate. The advantage to this scheme, known as FISO (fast-in, slow-out) is that many of the downstream signal processing components can be slower, lower power, lower cost, and potentially lower noise. To realize the full benefits of FISO, however, requires that the high-speed input sampling and storage circuitry be very area

and power efficient. This generally is not the case when flash A/Ds and high-speed digital memory are used for this function.

A summary of the requirements of wireless spread-spectrum communications receivers is given below.

Summary of spread-spectrum receiver requirements

- Fast, programmable, parallel matched filters
  -For wideband PN systems requiring rapid acquisition

- Fast-settling frequency synthesizers for building fast-hopping local oscillators
  -For fast-hopping FH systems

- Long, programmable matched filters for narrowband signals
  -For low-bandwidth, low-power systems requiring long PN codes

- High-speed, low-power FISO circuitry to absorb data bursts
  -Allows processing of signals at lower speed, power, noise, and cost in low-duty-cycle systems

- Low-power, low-cost components for consumer wireless applications

As will be discussed below, advanced CMOS/CCD technology can be of great benefit in meeting many of these requirements.

Characteristics of Advanced CMOS/CCD Technology

Signals can be represented in the voltage, current, or charge domains. Historically, the use of the voltage domain has dominated, with the current domain sometimes employed in applications where its advantage in speed outweighs its typically higher power dissipation (e.g., RF, ECL). As geometries and power supply voltages are reduced, however, these two domains become more difficult to use. In the case of voltage-domain circuits, headroom, noise margins, and speed are negatively impacted by shrinking geometries and supplies, and higher parasitic capacitance. In the current domain, performance is degraded by reduced headroom and more resistive devices and interconnects. Because a current inevitably flows between supplies the number of signal-processing operations (each requiring at least a diode drop) that can be performed before this current must be "reflected" off a supply is severely diminished as headroom drops. Indeed, even the reflection requires a minimum of a diode drop, and is itself a source of signal degradation and power dissipation.

More recently, charge-domain signal-processing techniques have begun to make inroads. Charge is *the* fundamental electrical quantity (voltage and current are manifestations of charge), and the processing of signals in the charge domain appears to have significant advantages in many applications. As IC technologies are scaled below

about 2 μm they become much more capacitive. Charge-domain signal processing takes advantage of this inevitable trend: higher capacitance per unit area allows higher charge densities. In switched-capacitor filter (SCF) technology, for example, the easy availability of capacitors and good switches have made it possible to replace "current through a resistor" with "charge on a capacitor" as a way to process signals. Such capability allows precision and programmability to be achieved with the control clock, rather than a fixed precision resistor. Furthermore, a savings in power is frequently realized. However, SCFs require voltage-domain feedback in order to move charge from one capacitor to another. This has resulted in frequency limitations that have restricted the use of SCFs to applications requiring sample rates below approximately 1 MHz (depending upon the required accuracy).

CCD signal processing does not require feedback to transfer charge. Its characteristics more closely resemble those of current-domain signal processing, but with the strong advantage of a self-restoring operating point after each transfer. Although many of the advantages of CCD-based signal processing have long been recognized, the high voltages, multiple clock phases, and high capacitance of early CCDs made it difficult to realize the advantages. However, these drawbacks are historical, not fundamental; many stem from the attempt to use CCD imager processes for signal-processing applications. The requirements for imaging and signal processing are so different that IC processes tailored for the former are unsuitable for signal processing.

CCD signal-processing technology has made major strides over the past decade. The advances have been so rapid that most public domain references are out of date. Noteworthy among these advances are the reduction of operating voltages to 5 V and the perfection of uniphase clocking [1]. The lower voltage and use of a single clock have been accomplished without a reduction in maximum CCD charge transfer rate. Indeed, 5-V CCDs fabricated in the late 1980s with older 4-um NMOS/CCD technology had reached test-equipment-limited speeds of 370 MHz [2]. Both device-level simulations and experience indicate that CCD charge transfer rates far exceed the ability of the on-chip peripheral circuitry to keep pace.

These recent advances have made CCD signal-processing technology compatible with 5-V CMOS technology. Simulations of more advanced CCD structures indicate that operation down to at least 3 V should be possible. It should be emphasized that CCD structures and processes designed for signal processing are much simpler than those for imaging applications, where optical and anti-blooming characteristics are critical. The simpler CCD structures are much more compatible with standard MOS technology. Furthermore, it appears that the compatibility with CMOS and BiCMOS technology improves as geometries are scaled down.

CCDs transfer packets of charge under clock control. The packets reside in potential wells created by MOS capacitors (see figure 1). Because of leakage currents the charge packets cannot be stored indefinitely; hence, CCDs are dynamic devices. In modern CCD technology this leakage current ("dark current") is very low, and storage times of 100s of μs at room temperature is possible. Storage times decrease with increasing temperature.

The charge-coupling effect occurs when adjacent MOS capacitors are close enough to cause their underlying potential wells to merge. By the application of appropriate voltages to the MOS capacitor gates the charge packets can be moved with a transfer efficiency exceeding 0.99999 in modern devices. Such high transfer efficiencies imply that in the transfer of a typical charge packet at most a few electrons are lost. The details of charge storage and transfer are covered thoroughly in several references on the subject [3,4] and will not be repeated here. Instead, the implications of these characteristics will be discussed.

The charge packets stored in the CCD potential wells can be analog in nature, with a wide dynamic range. Transfer of these signal samples under clock control can be effected very rapidly with virtually no distortion or addition of noise. No switch is required to move charge, as in the SCF case, thereby avoiding kTC noise. With the smaller geometries, lower voltages, and uniphase operation of advanced CCDs the transfer of a typical charge packet requires approximately 250 fJ of energy (supplied by the clock driver). Even at 100-MHz transfer rates the power dissipation per packet is only about 25 μW. At this speed the simultaneous transfer of 1,000 charge packets consumes roughly 25 mW.

With the high transfer efficiency of advanced CCDs a charge packet can be transferred hundreds of times without significant degradation. With fast clock edges complete charge transfer can be achieved in less than 1 ns. Furthermore, techniques are available to nondestructively sense the charge packets, at each storage site if desired. Depending upon details of the CCD design and sample rate, dynamic ranges between 8 and 12 bits are typical, and linearities between 6 and 10 bits are easily achieved. Improved linearities are possible with the use of differential techniques, matching circuits, etc.

The high dynamic range possible in CCDs even at high clock rates opens up the possibility of implementing multi-level logic functions that can be very efficient in power and area compared with binary logic [5,6]. With such capability it may be possible to achieve any required digital signal processing on a CMOS/CCD chip without resorting to drastic scaling of device dimensions, with a concomitant reduction in operating voltage. More generally, we can view the high information density possible in advanced CCD technology as allowing a full spectrum of quantization levels, from binary to multi-level to analog.

Summary of the characteristics of advanced CMOS/CCD technology

- Simple 5-V uniphase operation
  - -Compatible with CMOS process technology
- Very fast transfer of charge packets with:
  - -Very high transfer efficiency
  - -Very low power dissipation
- Wide dynamic range and low noise permit:
  - -Discrete-time analog circuits
  - -Multi-level digital logic
- Parallel processing of hundreds of signal samples
- Dynamic operation:
  - -Charge packets have finite storage times

Characteristics of Digital CMOS Technology

Today, binary logic implemented in digital CMOS technology is ubiquitous. Among the key reasons are low cost and power dissipation, both of which are of vital importance to wireless communications in consumer applications. However, these two characteristics must be re-examined as the technology is scaled and average gate toggle rates increase.

The forces behind the scaling of CMOS technology include the need for increased speed and density, and lower power dissipation and cost per function. Down to geometries of about 0.8 μm scaling has delivered on its promise. Below these dimensions many issues come into play that slow or even reverse the gains previously achieved.

Both speed and density are negatively impacted when the operating voltage must be reduced from 5 V to 3 V to reliably accommodate MOSFET gate lengths shorter than about 0.8 μm. Logic gate switching speed is slowed because the effective MOSFET gate drive voltage is reduced, thereby decreasing transconductance. Increased parasitic capacitance also contributes to slower switching.

Except in memory applications the drop in supply voltage has a surprising impact on functional density. With reduced headroom the number of devices stacked vertically to form a logic gate must be reduced. For example, a 4-input NAND gate may no longer be practical, and functions must be implemented with multiple 2-input gates, inverters, etc. Consequently, the number of transistors, the propagation delay, and the power dissipation per function can actually *increase*.

Power dissipation in fully-complementary CMOS logic circuits is proportional to CV^2f, where f is the gate toggle rate. Decreasing V, however, does not always yield the expected power dissipation reduction, especially if geometries are scaled. The reasons are twofold: first, junction capacitances increase as the supplies are lowered, and second,

parasitic capacitance increases as geometries are scaled. Adding to the problem is the fact that interconnect lengths have not scaled as rapidly as widths, and the increasing number of layers of interconnect create a third dimension for parasitic capacitance.

The equation for power dissipation given above is responsible for an increasingly troublesome fact: although CMOS logic has the lowest static power dissipation of any IC logic technology, it also has the highest dynamic power dissipation by far. When the average toggle rate of CMOS logic gate reaches into the range of roughly 50-100 MHz even emitter-coupled logic (ECL) may have lower power dissipation. The explanation for this is that at a certain point the high static power dissipation of ECL is offset by the much higher dynamic power dissipation of CMOS (ECL has very low dynamic power dissipation). Hence, in many high-throughput applications CMOS technology may not be the lowest power option. Partitioning of a system into low- and high-throughput blocks, each implemented in the optimum logic technology, may be necessary to minimize total system power dissipation.

The digital revolution of the past 15 years has occurred because, among other factors, the cost of a transistor has decreased as scaling proceeded. This resulted in higher functional density at lower cost per function. This trend, however, appears to be bottoming out somewhere in the range of 0.5-0.8-μm geometries , and cost per transistor will *increase* below these dimensions [7]. While there are many reasons, the two key factors are increasing processing complexity and the escalating cost of the fabrication equipment and facilities required to achieve the extraordinarily low defect densities necessary for adequate yield in non-redundant (mainly non-memory) circuits. The cost per function will increase even faster than that of a transistor because, as discussed above, the number of transistors per function will increase as supplies are reduced. As a result of the increasing functional cost of scaling below a certain point, greater emphasis will be placed on alternative techniques to achieve the required throughput and power dissipation. One of these alternatives is multi-level logic, as discussed above. Others include greater use of mixed-signal and analog technology, as well as more clever design techniques.

A final point on digital CMOS technology in signal-processing applications has to do with the nature of the logic gate current spike during switching. Pure CMOS logic gates conduct current between supplies only during switching. In advanced CMOS technology this spike is of high amplitude and very sharp. Unlike memories and general purpose functions (e.g., microprocessors), high-throughput dedicated signal-processing functions tend to be heavily paralleled and/or pipelined. Logic gates switch frequently and nearly synchronously. A systolic array is an extreme example of this architecture: each gate switches at half the clock rate (on average) and simultaneously with all other gates. Consequently, the current spikes of many gates are closely aligned, and the overall spike can easily reach many amps in amplitude. Because of resistance in the power busses the internal supply voltage tends to collapse during the current spike. At best, switching will be slowed by the lower effective internal supplies; at worst, data can be lost. The sensitivity to this "current starving" of internal logic is exacerbated when the supply voltage is lowered. While adding on-chip decoupling capacitance is helpful, this approach decreases functional density and increases die area.

This disadvantage to CMOS logic is one of the reasons that ECL is often preferred in such applications. ECL is current-steering logic, and the supply current is relatively constant regardless of switching.

Hence, the use of advanced digital CMOS technology in spread-spectrum systems must be done carefully. Applications should be selected that take advantages of the strengths of CMOS while avoiding its weaknesses.

Summary of the characteristics of advanced digital CMOS technology

- Extremely low static power dissipation
- Extremely high dynamic power dissipation
- Sharp current spikes during logic transitions
  -May collapse internal supply voltage in heavily pipelined architectures
- Increasing transistor count per function as supply voltage drops below 5 V
- Increasing transistor and functional cost as geometries drop below 0.8-0.5 μm

RF & IF Applications of Mixed-Signal CMOS/CCD Technology

CCD Prescalers

The frequency-hopping version of a spread-spectrum receiver requires a hopping LO in order to dehop the received signal. One way to generate this hopping LO is with a frequency synthesizer based upon a phase-locked loop (PLL). Such a synthesizer requires a programmable frequency prescaler in the phase-locked loop to divide down the synthesizer output. This function is typically performed by a flip-flop based frequency divider, with very high f_T transistors. These transistors are biased for high-frequency operation and consume a fair amount of power.

An alternative approach to solve this problem based upon CCD technology has recently been presented and demonstrated [8]. The basic concept is shown in figure 2, where a uniphase silicon CCD is assumed (the authors of [8] used a two-phase GaAs CCD to achieve operation up to 18 GHz). Operation of the prescaler is as follows. The high-frequency input (amplified until of sufficient strength to serve as the CCD transfer clock) is applied to the CCD clock electrodes, which operate perfectly well with a sinusoidal clock. Under control of this clock charge packets are extracted from the source and transferred to a selectable output stage (only one output is shown here for clarity). The potential at this output stage is fed back to an input control gate that is capable of passing or blocking the charge extracted from the source diffusion. This feedback point is also the output of the circuit.

Key to the operation of the divider is that when charge packets already in the CCD channel reach the output they are able to inhibit the injection of new charge packets. Assume for starting conditions that all storage wells under the DC phase of the four-stage

CCD of figure 2 are full. Then injection of new charge packets will be blocked for four cycles of the input waveform. Once the four packets have been cleared out then new charge packets will be injected for four more cycles, after which the first "new" packet reaches the output. The cycle then repeats. Hence, the four stage prescaler shown divides down the input frequency by a factor of eight.

The key features of the CCD-based prescaler are simplicity, small area, and low power dissipation compared with flip-flop based implementations. All of these features are advantageous in wireless communications. With 2-μm silicon CMOS/CCD technology the prescaler should be capable of operation from ~1 kHz to ~100 MHz. Scaling to a 1-μm process should extend the upper end beyond 200 MHz.

Programmable Bandpass Filters

Receivers require bandpass filters (BPF) in several locations. One is at the output of the mixer, where it is necessary to reject the undesired sum or difference frequency. When a fixed LO is used the BPF can likewise be fixed, and such filters are typically implemented with passive components. For such applications it is difficult for an active filter to compete with the cost of SAW- or LC-based filters. However, where programmable filters are of benefit transversal filters based upon CMOS/CCD technology may be attractive. With programmability the receiver not only can change center frequency and bandwidth, but also tailor the skirt slopes and even introduce notches to reject interference. Such devices may ultimately reduce inventory costs by having fewer, programmable components able to cover a range of applications that would require many fixed, passive filters. Furthermore, the trend towards programmable receivers able to accommodate a wide range of frequencies, waveforms, and modulation schemes may tilt the balance in favor of programmable BPFs.

A typical transversal filter is shown in figure 3. Here, the delayed signal samples are weighted and summed to achieve the desired result. Tap weight accuracy and resolution, as well as the length of the CCD and oversampling factor, are all parameters that can be used by the filter designer to achieve the required transfer function. In general, tap weight resolution and accuracy can be reduced by increasing the length of the delay line and number of taps. Ternary weights (+1, 0, -1) are easily implemented. Taps of greater resolution are possible but require greater work. In adaptive-equalization applications tap accuracy can usually be relaxed because feedback will adjust the tap weights to the correct values as long as the required *resolution* is available [Note: this ability to exploit the distinction between accuracy and resolution in analog circuits is *unavailable* in digital circuits]. Fully-differential filters can be designed with two CCD channels. The sample rates possible with a CCD transversal filter are similar to those for the prescaler discussed above: about 100 MHz for 2-μm technology and at least 200 MHz for 1-μm technology

Although programmable transversal filters can be implemented with DSP technology (preceded by an A/D), such an approach consumes much more power and area than in the CCD case. Furthermore, the upper frequency limit will be much lower for the DSP case because of the speed bottleneck created by the multiply-add operations. While the DSP approach is theoretically capable of greater accuracy than the CCD approach, in practice the accuracy limit is set by the A/D and truncation error. At typical IF

frequencies (~70 MHz) it is difficult for A/Ds to achieve even seven effective bits of accuracy. This speed-accuracy tradeoff is the key reason that high-accuracy real-time digital filtering is currently limited to about 1 MHz.

IF Subsampling

Mixers are typically used where conversion of the signal to baseband is necessary. Although these are mature components they still have several deficiencies. The minimum insertion loss is several dB, and the higher-performance units tend to consume a fair amount of power. An alternative technique for dropping the signal to baseband is to sample the IF at a subharmonic that is at least twice the *signal* bandwidth. Although this technique requires a very short aperture uncertainty, the insertion loss can be very low. Furthermore, in the case of a FH system it may be possible to avoid generating a hopping LO by simply adjusting the sample rate.

While the sampling can be done with a track-and-hold or A/D, using a CCD to sample has several advantages because the samples can be stored. The presence of many delayed signal samples enables several signal-processing operations to be accomplished. Among these are transversal filtering (discussed above), matched filtering (to be described later), the direct generation of I&Q baseband components, and buffering of data bursts, both of which will be described below.

I&Q Generation

Generation of in-phase (I) and quadrature (Q) components of the baseband signal is normally accomplished by using two mixers with LOs that are in quadrature. This technique has the drawbacks described above. Another way of accomplishing this function is with a transversal filter. By following the IF sampler with a Hilbert transform implemented in the tap weights it is possible to directly generate I&Q components and thereby avoid the complexity, power dissipation, insertion loss, and I&Q imbalance inherent with mixers [9] (see figure 4). Merging of the direct IF sampler with the Hilbert transform should result in a very compact, low-power signal-processing block. In bursty data situations there could be another benefit to this approach, as discussed next.

Fast-In, Slow-Out (FISO) Data Buffers

As described in the earlier section on spread-spectrum receiver requirements, many modern digital communications systems send bursts of data. When the duty cycle of the data bursts is less than 50% it becomes possible to read out and process the information at a rate lower than the sample rate. At a duty cycle of 1/3 the readout rate can be half the input rate. At a 10% duty cycle the readout rate can be $1/9^{th}$ of the input rate. This FISO approach has the advantage of allowing downstream circuits to be slower, lower noise, and lower power.

One approach to sampling and buffering high speed bursts is to use a very fast A/D followed by ECL logic. Unfortunately, this very expensive in terms of power dissipation, component count, and cost. Often the costs outweigh the benefits. With advanced CCD technology, however, the tradeoffs are far more attractive. In the first place, it is far easier to make a high-speed analog sampler than an entire A/D. Secondly, with a CCD these analog samples can be stored and transferred at high speed and low power. Changing the

readout rate is effected by simply changing the CCD transfer clock rate. If A/D conversion must ultimately be done in the system it can be done at the lower readout rate, thereby reducing the cost and power dissipation of that operation.

Once the signal samples are in the charge domain many of the operations described above can be performed in the same device. For example, it may be possible to perform direct IF subsampling, FISO, I&Q generation, transversal filtering, and matched filtering, all in the same device.

With today's CCD technology bursts of up to ~256 samples can be absorbed in a single linear CCD shift register at very high speeds. For longer bursts a serial-parallel-serial (SPS) structure is more appropriate. As shown in figure 5, the SPS structure consists of two serial CCDs of length n connected by n parallel CCDs of length m. Operation is as follows: When the high-speed serial input register is full the charge packets are transferred in parallel to the first stages of the parallel CCDs. This process is repeated until the central array is filled, at which point n x m samples are stored. Then readout through the lower output serial register is effected by making a parallel-to-serial transfer from the central array to the output register. Note that the central array clock rate during read-in is $1/n^{th}$ that of the high-speed input clock, and that the output clock rate is independent of the input rate.

SPS CCDs have been built in older 4-μm NMOS/CCD technology that have input sample rates of hundreds of MHz and store tens of thousands of analog samples [10]. The use of more advanced technology should allow significant improvements to these figures. Similarly, more advanced processes should mitigate one undesirable characteristic of these devices: the serial-to-parallel transfer normally takes longer than one high-speed clock cycle. Hence, for complete signal coverage it is presently necessary to ping pong between two SPS devices (which can be on the same chip). With scaling and other improvements this dead time should be reduced and possibly eliminated.

The SPS architecture introduces another feature of CCD technology: the ability to perform two-dimensional operations. While barely explored here, this capability opens up another degree of freedom that may be very powerful.

As an example of the potential benefits of the FISO approach, consider a system where the data bursts are at 100 MHz, while the duty cycle of the bursts is $1/11^{th}$. The readout rate could be as low as 10 MHz (20 MHz is double sampling). At the high burst rate flash converters and ECL logic and memory would likely be required. At the lower readout rate non-flash converters and lower-power CMOS logic and memory could probably be used. In addition, noise and component costs would be reduced.

Summary of RF & IF applications of mixed-signal CMOS/CCD technology

- Programmable frequency prescalers
  -Small, simple, fast, low power
- Programmable filters
- Direct IF subsampling
- I & Q generation
- FISO data buffering

Baseband Applications of Mixed-Signal CMOS/CCD Technology

Regardless of the method by which the signal reaches baseband there are a number of operations that are normally required to be performed there. In this discussion it will be assumed that none of the required processing has been done at IF, and that the signal has been dropped to baseband by conventional methods (mixers and LOs).

FISO Memories for Data Buffering

As at IF, the ability to soak up a high-speed data burst and later feed it out slowly to slower downstream circuitry is of great value if the required circuitry is compact and low power. The requirements and benefits at baseband are similar to those at IF, previously described, and the discussion will not be repeated here. One distinction of the baseband FISO circuitry is that the aperture uncertainty can be greater because the signal is not being sampled on a carrier.

Programmable Matched Filters

As discussed in the earlier section on PN spread-spectrum systems, programmable matched filters (PMFs) are required when acquisition time must be short relative to the message length. PMFs are a special case of transversal filters (see figure 3) in which the reference is identical to the (original) signal. In a PN-type system the PMF reference is identical to the PN code used to modulate the original data stream at the transmitter. This implies that the PMF reference code is binary (or ternary), a great advantage. Since the bits in the original data stream modulate the polarity of the transmitted code, the output of a PMF is a positive or negative correlation spike when the received signal is aligned with the fixed reference. Consequently, is possible to determine whether the transmitted bit is a one or zero, as well as when the match occurred. When the signal is double sampled (required in many situations to avoid straddling loss) significant circuitry savings can be realized by having one tap per two samples. In this situation, every other sample is sensed and weighted on one clock cycle. On the following clock cycle the samples have moved one stage, and now the second set of interleaved samples is aligned with the taps. With this arrangement the PMF output is a double correlation spike. The amplitudes of the two

correlation spikes are equal only for the case of optimal sampling timing. This fact is frequently used to adjust the timing with a feedback loop. This class of PMF is frequently referred to as "double-sampling PMFs."

It can be shown that a matched filter provides the optimum correlation amplitude possible with the received signal. Furthermore, it provides rejection for unwanted signals. Although the PMF output would ideally be zero between correlation spikes, in practice this is impossible because of properties of the PN code itself, imperfect rejection of unwanted signals, and imperfections in the PMF. These factors result in non-zero "sidelobes" being generated between correlation spikes. As for the PMF, the peak-to-sidelobe ratio relative to the theoretical ideal is an important figure of merit.

As with the PTF, a massive amount of signal processing is typically required to implement a PMF. At each clock tick each sample of the received signal must be appropriately weighted by the corresponding reference code bit, and the resulting products added. One clock cycle later the signal has moved down one stage, and the process is repeated. Typical resolutions required in the signal path are 6-8 bits, with ternary weighting sufficing for the reference code if the original modulation was digital. PMF sample rates can range from low MHz to >50 MHz with present technology, with even higher speeds required to handle some proposed systems such as wireless Ethernet.

CMOS/CCD technology is well suited to handle the sampling and delay of the signal with required dynamic range and speed. The upper speed limit is set by the CMOS weighting circuitry, which in 2-μm CMOS technology is about 50-100 MHz. Far higher speed can be expected as the technology is scaled down. Summing of the weighted signals is done in the analog current or charge domains and does not typically impose a speed limitation (speed is often limited by the output drivers).

Figure 6 shows the output of an experimental matched filter based upon older 4-μm NMOS/CCD technology [11]. The device (known as the 4ABC) is a four-channel (two pairs of I&Q channels), 128-sample, 64-tap, double-sampling PMF with an analog signal path and ternary reference weights. The PN code used is a cyclic maximal-length sequence ("m sequence"). This class of codes has the unique property that the sidelobes between correlation spikes is ideally flat. Hence, these codes are useful for testing PMFs, and in figure 6 the peak-to-sidelobe ratio is about 40 dB. More careful testing revealed that the limiting factor in the sidelobes was not the PMF but rather the inability to generate the m sequence with sufficient accuracy (a 1% variation in the code amplitude will produce sidelobes 40 dB down from the correlation peak).

A more advanced CCD PMF (known as the 2ATC) based upon 2-μm CMOS/CCD technology is currently in testing. This chip was developed at MIT Lincoln Laboratory under NASA sponsorship. The device is a dual-channel (I&Q), 512-sample, 256-tap double-sampling PMF with analog signal samples and ternary weights. Preliminary results indicate full operation up to 50 MHz, with further testing required to fully characterize the device.

For PMFs based upon digital technology the multiply-additions are the most difficult operations. Where pipeline delay can be tolerated the multipliers can be made serial and the addition of the many products is typically done with an adder tree. Because of their high transistor count digital PMFs require a large silicon area. In addition,

because the average gate toggle rate is high the power dissipation is likewise high for a given functionality.

Table 1 compares the 4ABC and 2ATC CCD-based PMFs with a commercially-available digital correlator (the TMC2023) of similar architecture but shorter length, much lower signal resolution, and only one channel. Using the 2ATC as the reference for functionality it is seen that although the digital PMF uses much more advanced 1-μm CMOS technology, it would take 64 chips to equal the functionality of one 2ATC, which is based upon 2-μm CMOS/CCD technology. In addition, the TMC2023 approach would require two 8-bit A/Ds, a large adder tree, and substantial glue logic, and would be significantly slower. The power dissipation for the fully-digital approach is about 30 times higher than that for the CMOS/CCD PMF. Basically, a board-level solution is required for the digital PMF to compete with a one-chip CMOS/CCD PMF.

More advanced digital PMFs have recently been introduced that use sub-μm CMOS technology and improved architectures. However, reduction of CMOS/CCD geometries by a similar *factor* would maintain the performance and functionality advantages demonstrated here, without resorting to the smallest-geometry process available. This comparison of the functional density and performance of PMFs based upon digital and mixed-signal CCD technologies is an excellent example of the advantage that discrete-time analog signal processing can have in many applications. Consequently, a given level of performance can be achieved with a less aggressive and expensive IC process.

Programmable Discrete-Time Analog Transversal Filters

As with the IF BPFs discussed earlier, the advantages of programmable filters at baseband may offset their added cost compared with passive, fixed filters. The issues are similar to those already covered for the IF case, and will not be repeated here. One point to emphasize, however, is that the baseband PTF may actually be a section of an IF subsampling chip. In a FISO situation the PTF may be turned into a baseband filter by simply reducing the CCD clock rate between signal bursts.

Analog-to-Digital Converters (A/Ds)

A/Ds based upon CCD technology appear to offer advantages over conventional conversion techniques in many situations, particularly when the signal is in the charge domain. Not surprisingly, these advantages are in the areas of speed, power dissipation, and chip area. Details about this new application cannot yet be discussed because of the proprietary issues surrounding work in this category. Suffice it to say that representing the signal in the charge domain, together with operations possible with a CCD, opens up new architectures and algorithms for both analog-to-digital and digital-to-analog conversion.

Multi-Level Digital Logic

The wide dynamic range of advanced CCD technology allows not only analog but also digital signal processing to be implemented. While CCD binary digital logic is possible, it does not have sufficient advantages over conventional digital technology in most applications to justify it use. Where CCD digital logic begins to pull ahead is where

the high information density of the CCD is put to use to create multi-level logic, often called multiple-valued logic (MVL), where "multiple" implies more than two levels [5,6].

While MVL has been demonstrated in the voltage, current, and charge domains, the charge domain appears at this point to have the edge in power dissipation and density. MVL test circuits in all domains have demonstrated impressive improvements in either speed, power dissipation, or density compared with conventional binary logic. Often the logic functions available in the different MVL technologies are different from those in well-established binary logic technologies. The optimum algorithm for a particular function may be radically different in an MVL technology than in a binary technology. What is holding up the adoption of MVL is the lack of design methodologies, CAD tools, and testing techniques, all of which are well established for binary logic. However, once the cost of transistors and functions begins to rise as a result of scaling (discussed earlier in the section on digital CMOS), then more emphasis will be placed on developing the tools and techniques required to take advantage of MVL.

Note that with the CCD A/D capability just discussed, the possibility exists for processing signals in the discrete-time analog domain, converting to MVL via a CCD A/D with MVL outputs, and continuing the processing in the digital domain, all on the same chip.

Performance Projections for CMOS/CCD Technology

Since the performance of the CCD itself is limited by that of the surrounding "conventional" circuitry, overall chip performance and density will benefit from the scaling of device dimensions. Device simulations of advanced silicon CCD structures indicate that charge can be transferred at GHz rates, even at 3 V. This potential speed is far beyond that projected even for scaled peripheral circuits. Table 2 shows performance projections for complex CMOS/CCD signal-processing devices, such as PTFs, PMFs, and converters. The speed projections are based entirely upon the speed limitations of the on-chip voltage- and current-domain circuits. Even higher performance may be possible as we learn to implement certain functions in the typically-faster charge domain, or develop new algorithms that avoid the speed bottlenecks of conventional circuitry.

Summary and Conclusions

Advanced silicon CMOS/CCD signal-processing technology can address many of the demanding requirements of wireless spread-spectrum communications technology. Potentially significant improvements may be realized in speed, density, and power dissipation. Recent advances in CCD design and processing allow simple 5-V uniphase operation, as well as compatibility with CMOS technology. The high speed of advanced CCD processes and structures allows RF and IF functions to be addressed, in addition to those at baseband. The high information density of a CCD enables signal processing in the discrete-time analog and multi-level digital logic domains. When such capability is combined with a CMOS (ultimately BiCMOS) process, each required function can be

performed with the most efficient algorithm in the optimum domain. With this approach, the overall system performance/cost ratio is maximized.

The high speed and information density of CCD-based charge-domain signal processing allows it to perform many functions far more efficiently than with a binary digital approach, even when compared with a much more advanced digital CMOS process. The advantages often translate into more than an order of magnitude improvement in key parameters such as power dissipation and die area. Alternatively, the same performance could be achieved with far more relaxed geometries.

With a new tool set of basic operations available in a CMOS/CCD process, new algorithms for implementing required functions are possible. Far higher performance is expected as the process is scaled. On the other hand, scaling of digital CMOS technology below approximately 0.8-0.5 μm is expected to raise the cost per function, and may even degrade performance as the supply voltage drops. Hence, the relative performance and cost advantages of a CMOS/CCD technology will likely grow.

Acknowledgments

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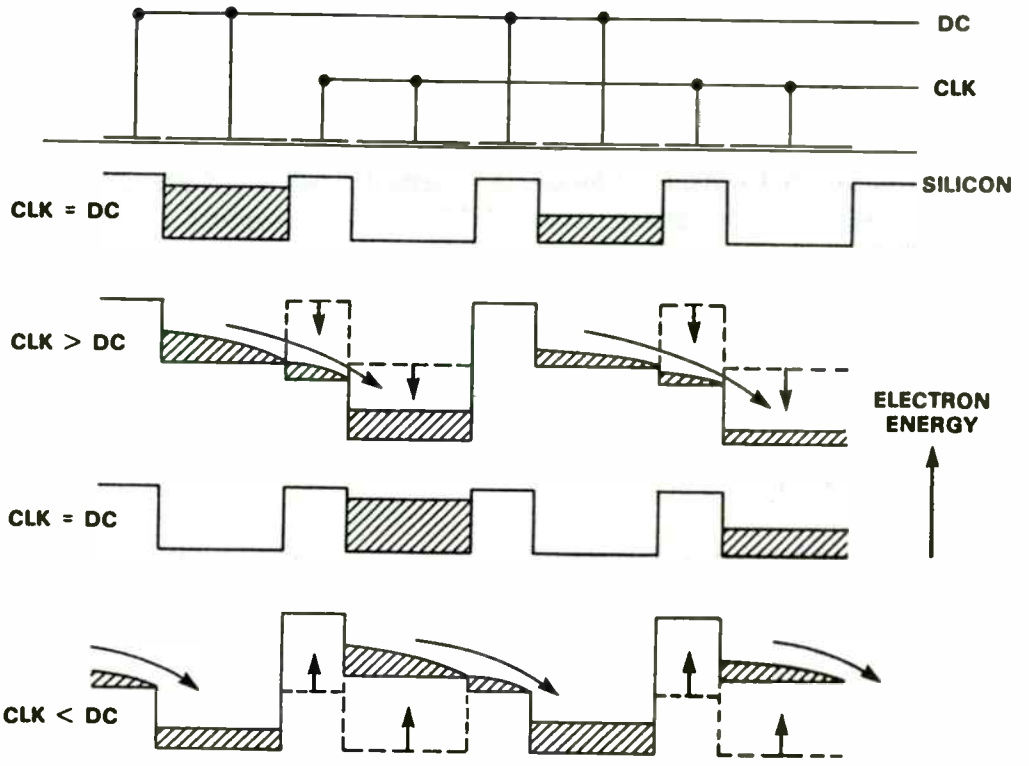

Figure 1. Uniphase operation of a CCD shift register. Charge packets are stored under MOS capacitors, and built-in potential wells and barriers contain charge and force it to move unidirectionally.

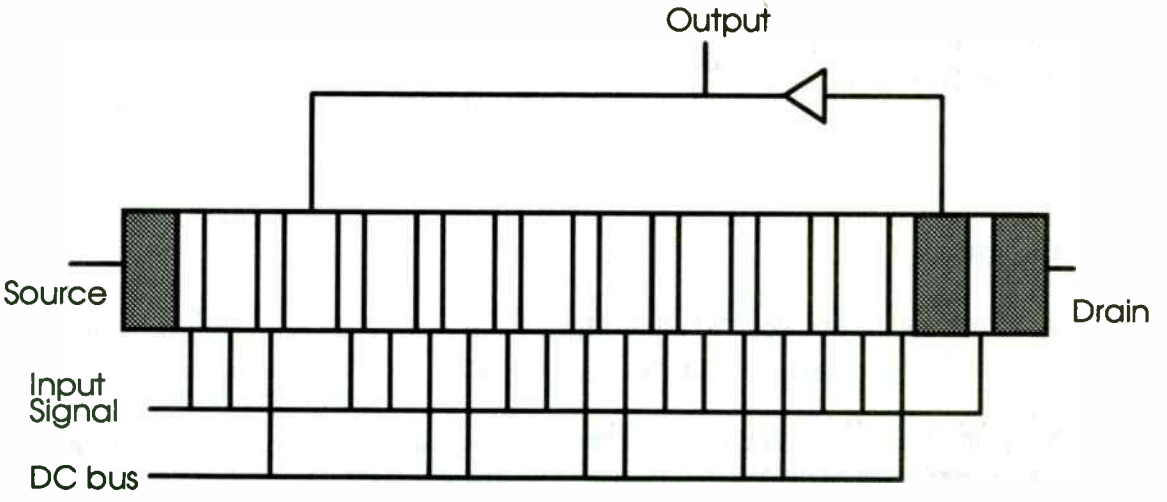

Figure 2. Simplified diagram of uniphase CCD divide-by-eight prescaler. Shaded areas are diffusions. Progammability can be effected by making the tap and/or feedback points selectable.

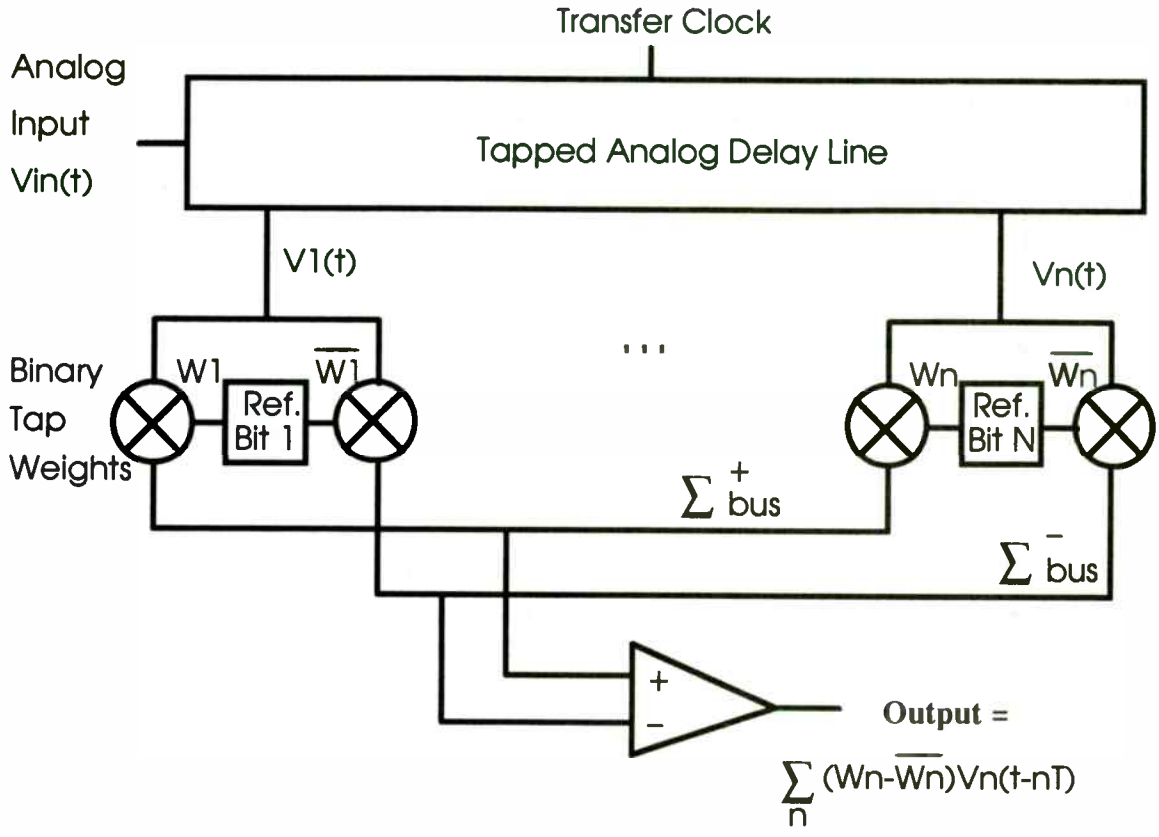

Figure 3. Generic analog-binary transversal filter. Delayed signal samples are nondestructively sensed. Resulting signals are routed to either a positive or negative sum bus, with routing determined by the corresponding reference bit. A differential amplifier takes the difference between the summed signals on the two busses and yields the desired result.

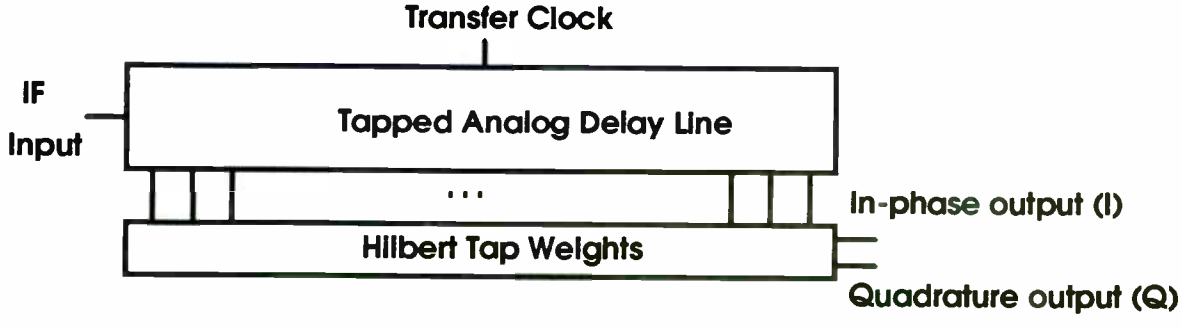

Figure 4. I&Q generation by subsampling at IF and Hilbert weighting of delayed samples.

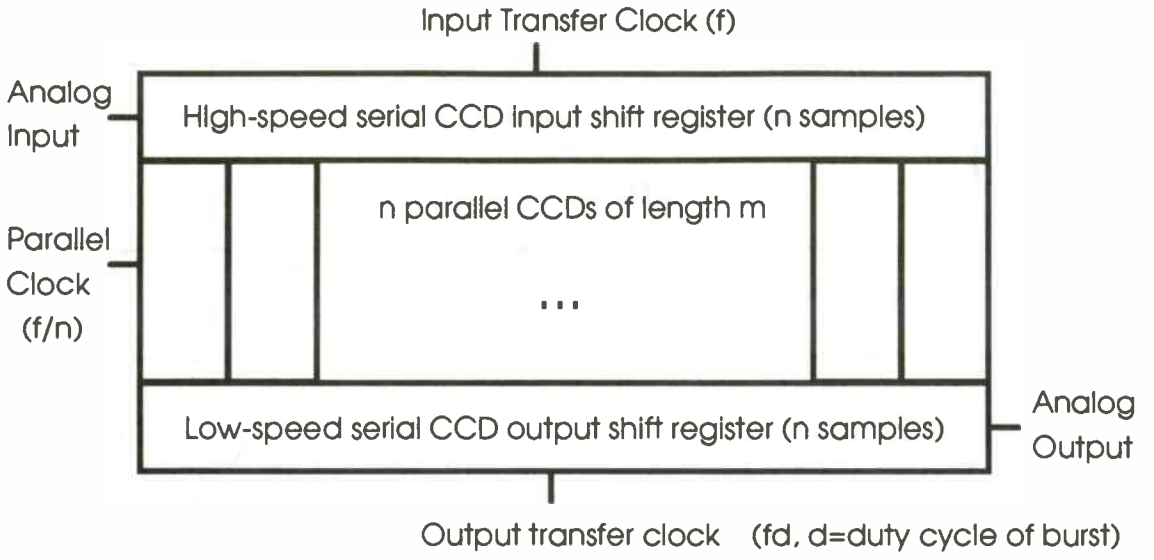

Figure 5. Serial-Parallel-Serial (SPS) CCD architecture for storing a large number of analog samples. The central array of parallel CCDs can store n x m samples. For low-duty-cycle data bursts the output rate can be much lower than the input rate.

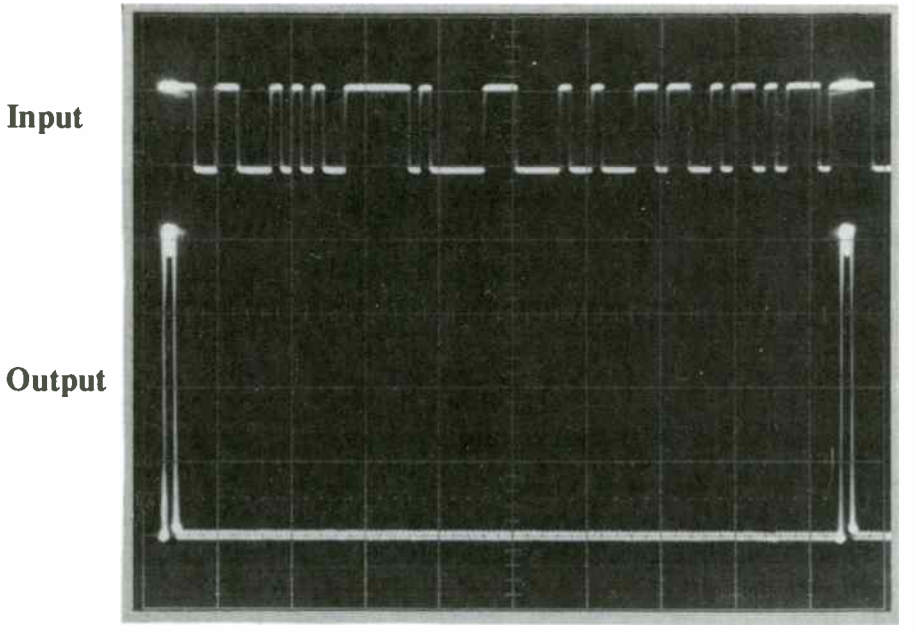

Figure 6. Performance of the 4ABC NMOS/CCD matched filter. Chip is a four-channel, 128-sample, 64-tap device. Reference code is a 63-bit m sequence. Input (top trace) is cyclic version of same code. Output (lower trace, one channel shown) is a correlation spike once every code cycle, and occurs when signal and reference codes are aligned. Sample rate is 10 MHz. Note the very flat sidelobes. (Oscillogram provided by MIT Lincoln Laboratory).

Table 1
Comparison of CCD and Digital Correlators

Device name	4ABC-2	2ATC-2	TMC2023
Technology	4-µm NMOS/CCD	2-µm CMOS/CCD	1.0-µm CMOS
Architecture			
Taps	64	256	64
Signal resolution (bits)	8	8	1
Reference weights	0, +/-1	0, +/-1	0, +/-1
Channels	4	2	1
Max correlation rate (Ms/s)	40	50	30
Max program rate (MHz)	50	100	?
Power Dissipation (W)	1	1	0.4
Die size (mm^2)	25.8	81	?
Number of chips to equal functionality of 2ATC-2	2	1	64*

* In addition to 8-bit A/Ds, a large adder tree, and glue logic

Table 2
CCD Technology Migration and Performance Projections*

Technology	2-µm CMOS/CCD	1.2-µm CMOS/CCD	0.6-µm BiCMOS/CCD
Max Sample Rate (Ms/s)	75	150	300

* Performance if for a complex signal-processing device, the speed of which is limited by on-chip peripheral circuitry. Simpler devices may be able to take greater advantage of the much higher speed of the CCD.

Signal Processing Requirements for Direct IF Sampling Receivers

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Advances in semiconductor processes have resulted in low cost Digital Signal Processing (DSP) and analog signal processing technology. These, in turn, have created alternative architectures for a variety of communication applications. Direct IF Sampling (DIFS) is one example of how the power of low cost DSP can be harnessed to serve the needs of the wide range of digital communication systems in development today. Moving the analog-to-digital converter (ADC) closer to the antenna, once a dream, is becoming a reality in many systems. DIFS can reduce cost and space while increasing the reliability, flexibility, and capabilities of modern communication systems. This paper will examine the signal processing requirements for digital receivers, especially as they relate to the selection and use of ADCs. Dynamic range, Bit Error Rate (BER), and bandwidth are among the topics to be discussed as they relate to digital demodulation, filtering, tuning, and equalization in a single channel receiver. This discussion will then be expanded to analyze the requirements for multi-channel digital receivers.

SINGLE CHANNEL RECEIVERS

The single channel receiver refers to a system that processes only one carrier signal at a time. A cellular handset or cable decoder box falls into this category. These receivers may tune a wide range of signal inputs but will process only one modulated carrier at any particular time. This paper will analyze the impact of sytem level requirements such as BER, data rate, and bandwidth on the selection of ADCs.

Bit Error Rate (BER)

One of the primary concerns in the design of digital communication systems is the Bit Error Rate (BER) requirement. BER requirements help to determine the dynamic range necessary in the communications channel. The channel Signal-to-Noise Ratio (SNR) traditionally dictates the resolution of the Analog to Digital Converter (ADC) to be used. Unfortunately, ADCs also contribute to the BER in ways that are *not* predicted by a simple noise analysis of the system.

Figure 1. graphically shows the expected BER of a digital radio system for various modulation formats and a given channel Carrier-to-Noise Ratio (CNR). The bandwidth is equal to the double-sided bandwidth required for an arbitrary symbol rate. These results correctly predict the BER resulting from noise acting on an ideal decision circuit (i.e. ADC). Higher order modulation schemes require greater dynamic range in order to accurately discriminate small phase and amplitude differences between symbols.

The CNR requirement derived from this analysis refers to the average signal power and must be converted to peak amplitude to insure that the selected ADC is not overdriven. The peak-to-average ratio (PAVGR) depends on a number of factors, including filter characterics and modulation scheme. The PAVGR can range from as low as 3 dB up to 15 dB. As an example, assume that a receiver is to be designed to directly sample a 10 MHz IF frequency with a single ADC, and perform digital demodulation on a 64-QAM signal. The BER requirement is 10^{-7} and the PAVGR is assumed to be 10 dB.

Refering to figure 1, the required CNR to support this BER is 27 dB . Adding another 10 dB (for PAVGR) yields a peak SNR at the ADC of 37 dB. In a real system, additional implementation margin is required to support non-linearities in the system and additional digital signal processing such as adjacent channel filtering, equalization, and AGC. This could add another 10 dB, resulting in a minimum of 47 dB SNR as the dynamic range requirement in the ADC. In this case, a theoretically perfect 8-bit ADC would provide the necessary dynamic range of 50 dB ($6n + 1.8$ dB).

Selecting ADCs

ADCs are not ideal however, and are specified with a SNR that varies as a function of the number of bits, analog input frequency, and signal level. Figure 2. shows the SNR vs. analog input frequency for several ADCs. It is important to note that the SNR (including distortion) or Effective Number of Bits (ENOB) degrades as the analog input frequency increases. The low frequency performance is generally dominated by static linearity problems such as differential or integral non-linearity. As the input frequency increases, the degradations are due more to AC affects. Jitter, slew rate limitations, non-linear capacitances, and differential delays on the chip are among the culprits that reduce the performance.

Beware of the bandwidth specification! Like the gain-bandwidth product specification in amplifers, the ADC bandwidth can be used only as a figure of merit in comparing ADCs. The bandwidth alone does not characterize the fidelity of the signal being digitized. An 8-bit ADC with 150 MHz bandwidth may digitize a 100 MHz signal but the effective resolution could be degraded to the point where a wider bandwidth 6-bit ADC would actually give a better representation of the signal.

The SNR of the ADC adds to the total system noise and in practice is usually over-specified to insure that the degradation due to the ADC is not significant. In our example, we assume a narrow band signal centered at 10 MHz as the ADC input. Referring to figure 2, we see that the AD9040A 10-bit ADC appears to be a good choice. Later we will see that these are not always sufficient criteria for selecting the ADC. The BER, sample rate, cost, and other factors must also be considered.

Other considerations include the aperture uncertainty of the ADC (particularly in direct IF sampling applications), output coding, and input signal levels. Another popular implementation is to include a high quality track-and-hold device (such as Analog Devices AD9100 or AD9101) in front of the ADC.

BER in ADCs

Random white noise, regardless of the source, creates a finite probability of errors (deviations from the expected ouput). The selection criteria described above take this noise into account in predicting the BER of the system. Unfortunately, ADCs also contribute to error rate in ways that *cannot* be predicted by noise analysis alone. Before describing these error code sources it is important to define what constitutes an ADC error.

Noise generated prior to or inside the ADC can be analyzed in the traditional manner. Therefore, an ADC error code is defined as *any deviation from the expected output which is not attributable to the equivalent input noise of the ADC*. Figure 3 shows an exaggerated output for a pure sinewave applied to the ADC. Note that the SNR of the ADC creates some uncertainty in the output. These anomalies are *not* considered error codes, but are simply the result of quantization and white noise. The large errors are more significant and are not expected. These errors are random and so infrequent that an SNR test of the ADC will rarely catch them. Because they are unpredictable and difficult to test, many ADC manufacturers have started characterizing these errors in various BER tests.

In most ADCs, the analog input is simultaneously compared to a set of reference levels by a string of comparators (this parallel or "flash" architecture is commonly used in stand alone converters or imbedded as part of a subranging ADC architecture) as shown in Figure 4. The comparators sense the appropriate signal level and load the decode data bus with a thermometer code. This digital word is then processed into binary code by the decode logic and passed to the output stage.

Three types of performance failure commonly dictate the BER of a flash ADC. The first is comparator metastability. A metastable comparator will cause an incorrect digital word to be loaded on the decode data bus. The second type of error occurs when two comparators turn on simultaneously attempting to load the data bus with different digital words. The rate of occurrence of this type of bus contention error is affected by the offset of multiple input paths, skews in input signals, high analog input slew rates, and noise.

The third source of BER is simply lost data due to poor timing. As data is passed from one cell to another, poor timing between clock commands and data switching can cause erroneous data transfer. This type of error is affected by internal propagation delays and clock rate.

Unfortunately, the most common source of unpredicted BER problems with ADCs result from improper system design. ADC manufacturers' recommendations should be followed to avoid digital noise coupling into the analog input or voltage references from either the power supplies or digital outputs. This is generally accomplished through careful routing of signal paths, good grounding practices, and proper power supply bypassing.

MULTI-CHANNEL RECEIVERS

A multi-channel receiver refers to any system which simultaneously processes more than one received carrier at the same time. A cellular base station falls into this category. Figure 5 shows a Traditional Digital Basestation Architecture comprised of a channelized heterodyne transceiver and shows components historically used in the design of a classic quadrature demodulator and modulator.

The All-Digital Basestation Architecture shown in Figure 6 is a radical departure from previous designs. The entire band of interest (multiple channels) is digitized simultaneously with a single ADC. All tuning and demodulation is then done in dedicated DSP hardware running at the sample rate of the ADC. Digital decimation filters then extract the narrowband information and present the data at a reduced sample rate to general purpose DSP for additional signal processing. In this architecture, analog signal processing requirements in the front end are more demanding (bandwidth, dynamic range, etc.), but there are many advantages. Individual tuners, demodulators, filters, and ADC pairs for each channel are replaced with low cost and programmable digital signal processing components.

Figure 7 depicts the frequency spectrum of the analog input presented to the ADC in this environment. The spectral lines represent narrow-band signal inputs from a variety of signal sources at different received power levels. Signal "C" could represent a transmitter located relatively far away from the signal sources "A" and "B". However, the receiver must recover all signals with equal clarity. This requires that distortion from the front end RF and IF signal processing components, including the ADC, does not exceed the minimum acceptable level required to demodulate the weakest signal of interest. Clearly, the third order intermodulation distortion products generated by "A" and "B" (2 x B - A) will distort signal "C" if the nonlinearities in the front end are severe.

In many systems the power level of the individual transmitters is under the control of the base station. This capability helps to reduce the total dynamic range required in the receiver. However, the highest signal could be a strong out-of-band interference source. Signal "D" in Figure 7 shows a large signal that may be attenuated by the filter, but is still powerful enough to introduce distortion.

ADC Noise Limitations

The dynamic range limitations of the ADC are limited by converter nonlinearities rather than noise. Random and quantization noise are spread evenly over the information bandwidth with a spectral density that is roughly constant. After the digital tuner, decimation filters will improve the SNR of the narrowband signal. This processing gain is proportional to the ratio of the sample rate of the ADC to the bandwidth of the digital filter (SNR improvement = 10log(Fs/2Fbw).

ADC Linearity Limitations

Spurious signals generated by the front end receiver or ADC cannot be reduced by oversampling. The Third order intercept point for a linear device (with some nonlinearity) is a good way to predict 3rd order spurious signals as a function on input signal level. However, for an ADC this is an invalid concept except with signals near fullscale. As the input signal is reduced, the performance burden switches from the input T/H to the encoder. This creates a nonlinear function, in contrast to the third order intercept behavior which predicts an improvement in dynamic range as the signal is dropped.

For signals below this level, the Spurious Free Dynamic Range (SFDR) is a more accurate predictor of dynamic range. The SFDR curve is generated by measuring the ratio of the signal (either tone in the two tone measurement) to the worst spurious signal observed (usually the 2nd harmonic or 3rd order IMD) as the analog input signal level is swept. The SFDR for a 12-bit 20 MSPS ADC (Analog Devices AD9022) is shown in Figure 8 for a two tone input. The straight line with a slope of one is constructed at the point where the worst SFDR point touches the line. This line, extrapolated to fullscale, gives the SFDR of the ADC. This value can be used to predict dynamic range by simply subtracting the input signal level from the SFDR. For instance, on the two-tone SFDR plot, a signal 20 dB below full scale will always have a dynamic range of at least 67 dB (87dB - 20 dB).

Dithering is one technique of improving the SFDR of an ADC at the expense of SNR. When noise is added to the input signal, nonlinearities are "smeared" across the transfer function of the ADC. In the frequency domain, the average energy of spurious signals is reduced while the SNR is degraded. The additive noise reduces the total dynamic range available, since the peak signal which can be applied without clipping in the ADC is now reduced. A refinement is often referred to as subtractive dithering. In this technique, the input noise source is generated by a DAC and the same value is then subtracted from the digital output. This method subtracts out the added noise, resulting in the same SNR as an undithered ADC. However, peak dynamic range is still reduced by the amount of noise added.

CONCLUSION

ADC requirements for direct IF sampling are driven by system demodulation requirements including the BER, data rate, and IF frequency. The ADC must have sufficient resolution (ENOB, SNR) at the maximum input frequency of interest . The sample rate, number of bits, and bandwidth specifications are not sufficient criteria for selecting the ADC in most applications. The converter is also an additional source of error codes. The BER of the converter should be considered independently from the noise analysis of the system.

In a multi-channel receiver, the dynamic range requirements are driven by the single channel requirements in the presence of multiple signals which must also be considered. In this environment, the SFDR of the converter is frequently the limitation on performance.

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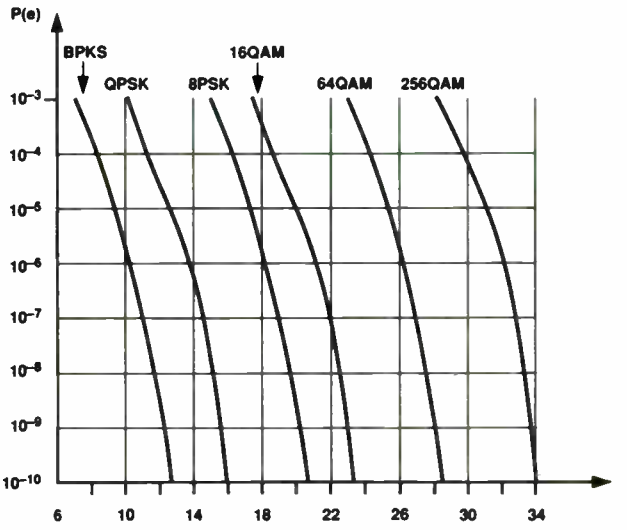

Figure 1. BER Performance vs. CNR

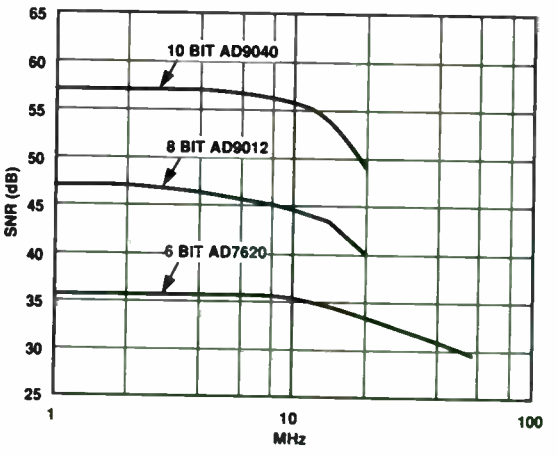

Figure 2. SNR vs. Analog Input Frequency for ADCs

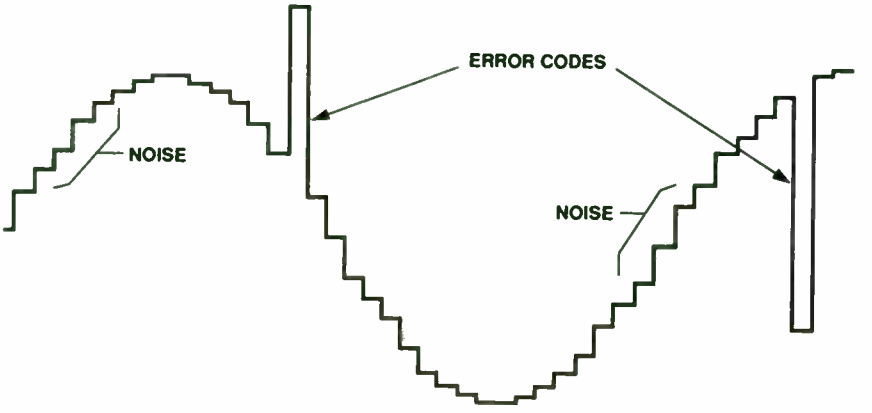

Figure 3. ADC Output Errors for a pure sine wave

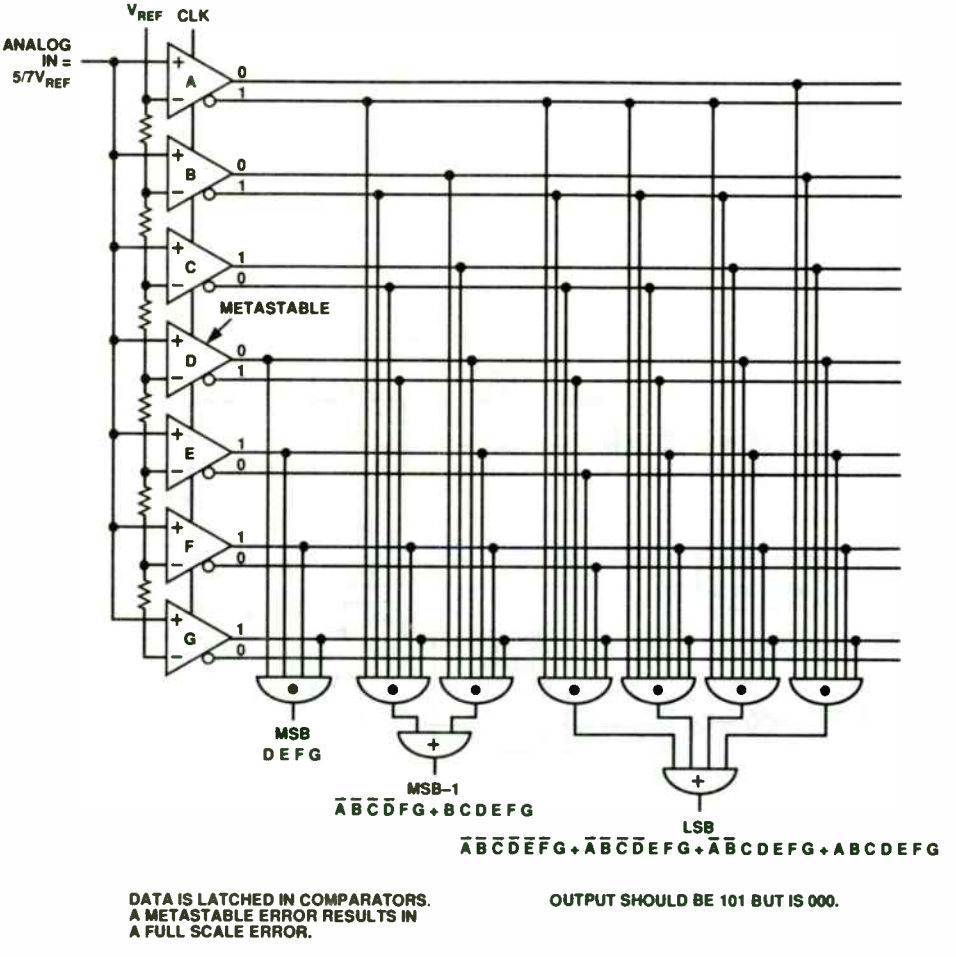

Figure 4. Analog/Digital Converter Comparator Stage

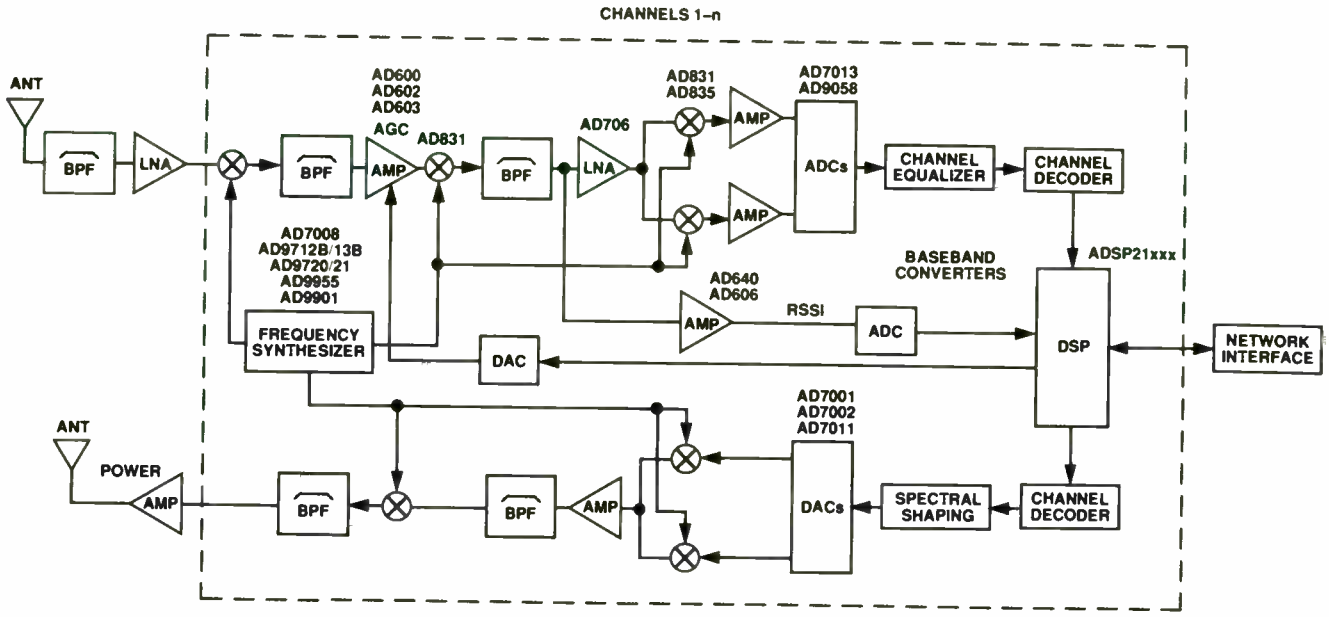

Figure 5. Traditional Digital Basestation Architecture

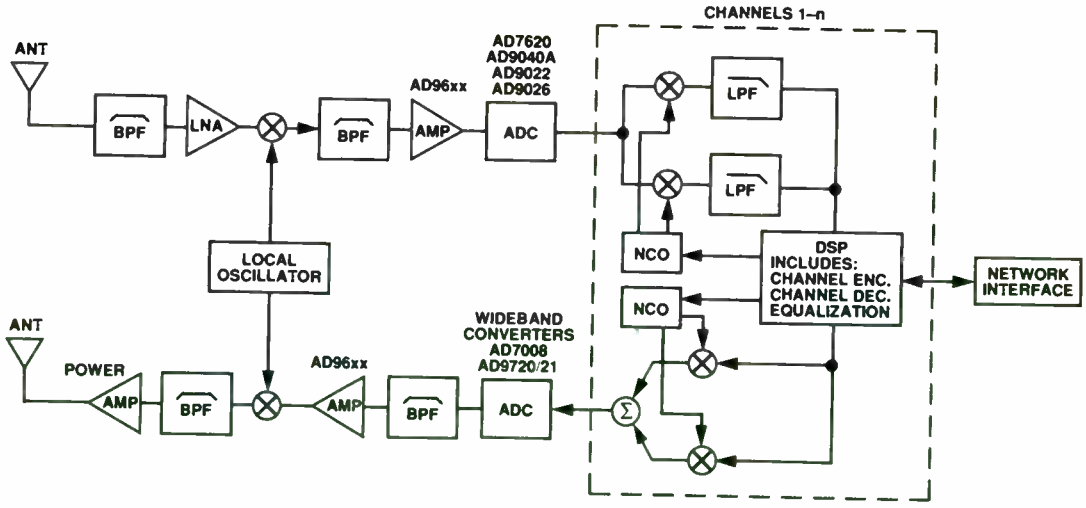

Figure 6. All-digital basestation architecture

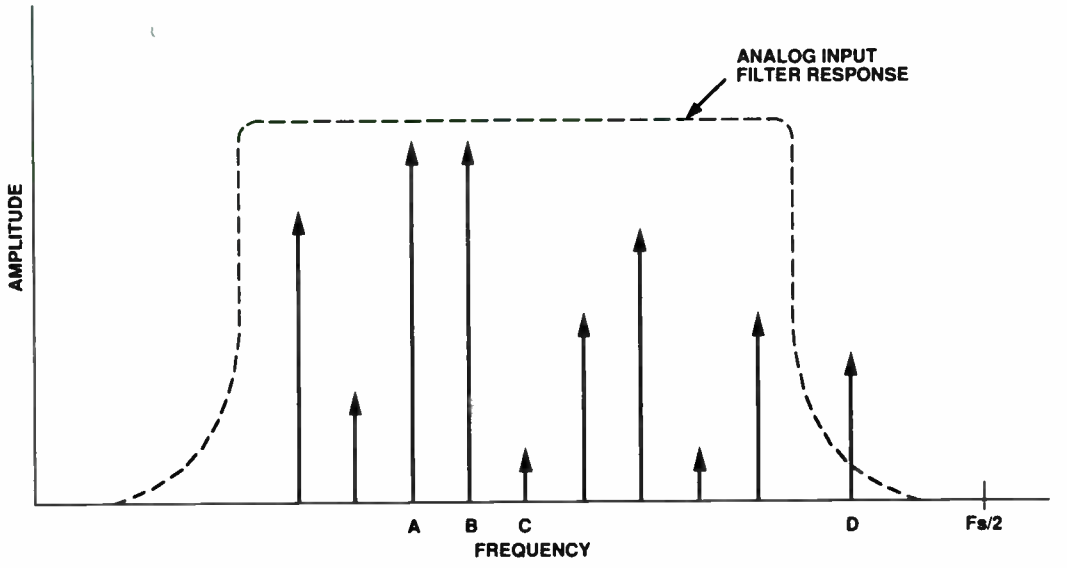

Figure 7. ADC Analog Input Spectrum

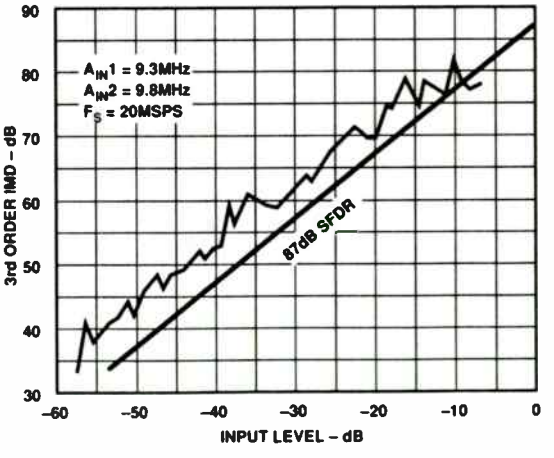

Figure 8. Two Tone SFDR for the AD9002

Baseband Superintegration Roadmap for Digital Cellular Handsets

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This paper discusses the challenges faced in reducing the number of Ics used in the baseband protion of digital cellular handsets. It presents a roadmap from 1992 through 1996, showing the reduction in IC count from five devices to a single-chip solution. Functions included in the signal path are DSP, microcontroller, voice codec, baseband converter, and gate array.

Challenges faced and tradeoffs examined include:

--migration from one micron to 0.35 micron CMOS
--reduction in power dissipation
--forward compatibility with half-rate codecs
--the path from 5 V to 3 V (and to 1 V?)
--importance of packaging technology (TAB, flip-chip)
--algorithm shrinks
--additional software functionality (hands-off operation, etc)
--cost improvements
--time-to-market tradeoffs

For a semiconductor company, the challenge is to develop and exploit total systems expertise, since the largest rewards will go to those companies that learn to leverage such system know-how.

Advanced RF ICs for VHF and UHF Communications

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Introduction

Developing ICs for the cellular RF-to-baseband environment,means meeting a customer's requirements. In the mobile-phone market, these are Price, Power, Package, and Performance.

Price leads, as always, because consumers and carriers want the phones to be as cheap as possible. Power translates into Talk Time, which is one of the few things resembling a technical specification that cellular-phone users care about. That means that we as semiconductor vendors must look for ways to design systems and chips that are as power efficient as possible; what's more, we must power down any function not being used.

Package translates into a phone's weight and size. Battery weight brings us back to minimizing power, but it also means making the phone as small as possible, or at least as small as a customer feels comfortable holding in his or her hand. So we're really talking about the volume occupied by the phone, and, by extension, the volume occupied by the chip set.

Performance is last because type acceptance is the great equalizer. Maybe a sophisticated customer will walk into his dealer and say, "Give me a phone that works on Route 128 in Waltham," (or wherever your local "Intermod Alley" is located) but that customer will be the exception rather than the rule.

These end-customer requirements drive our IC and process development. The trick is to take these customer inputs, step back, and figure out how to provide the most effective solution from a system-level perspective.

Process and Partitioning

When planning a chip set, one of the problems is partitioning the functions to keep the cost down, the design simple to reproduce, and the power consumption low. Although direct-to-

baseband conversion (also known as homodyne and 0 IF), single conversion, and dual conversion architectures are the subject of much debate as to which is the best architecture, we will use a dual conversion architecture as the vehicle for this discussion.

Figure 1 shows a simple dual-conversion transceiver. The baseband portion of the design is straight forward: all the functions are digital or baseband analog and can be fabricated on CMOS processes. The RF portion of the design, however, is not so straightforward. The T/R switch, LNA, RF mixer, prescaler, and power amplifier are "obviously" GaAs, but what about the IF subsystem and the synthesizer?

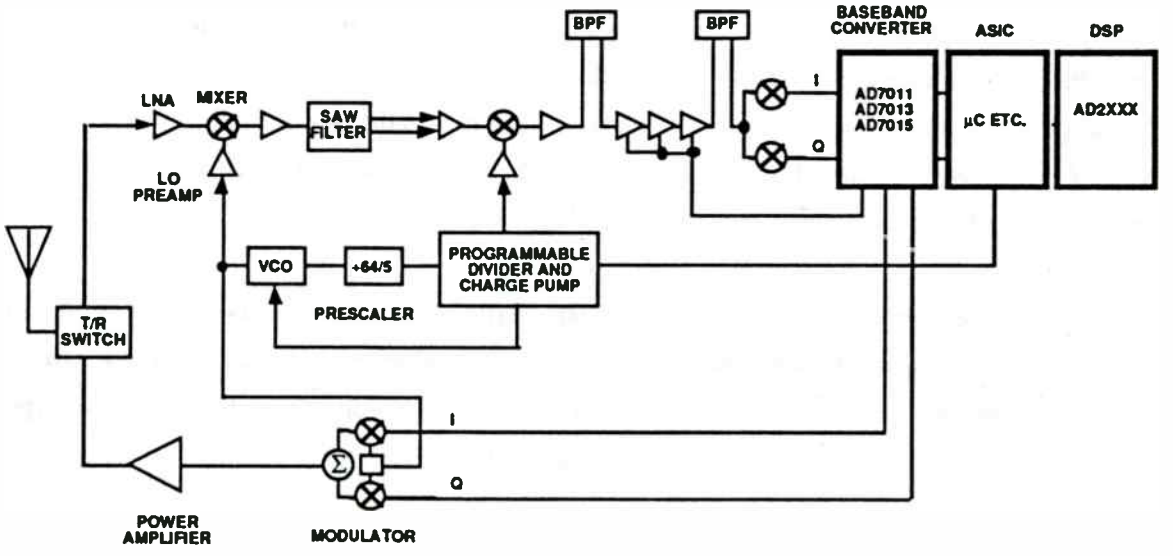

Figure 1. A Dual Conversion GSM Transceiver

One approach is use GaAs for all of the RF functions, silicon for the IF, and CMOS for the programmable divider and charge pump portion of the synthesizer (Figure 2). This approach does allow some optimization; GaAs provides low noise and high speed for the RF functions and prescaler and a 3 GHz complimentary bipolar process such as Analog Device's XFCB can be used for the IF subsystem IC. The complimentary bipolar process allows the IC designer to save substantial power at high signal levels by using Class AB amplifiers to drive the IF filters rather than Class A amplifiers. It also reduces chip area by allowing dc-coupled stages internally and simplifies design for low-voltage (2.7V) operation.

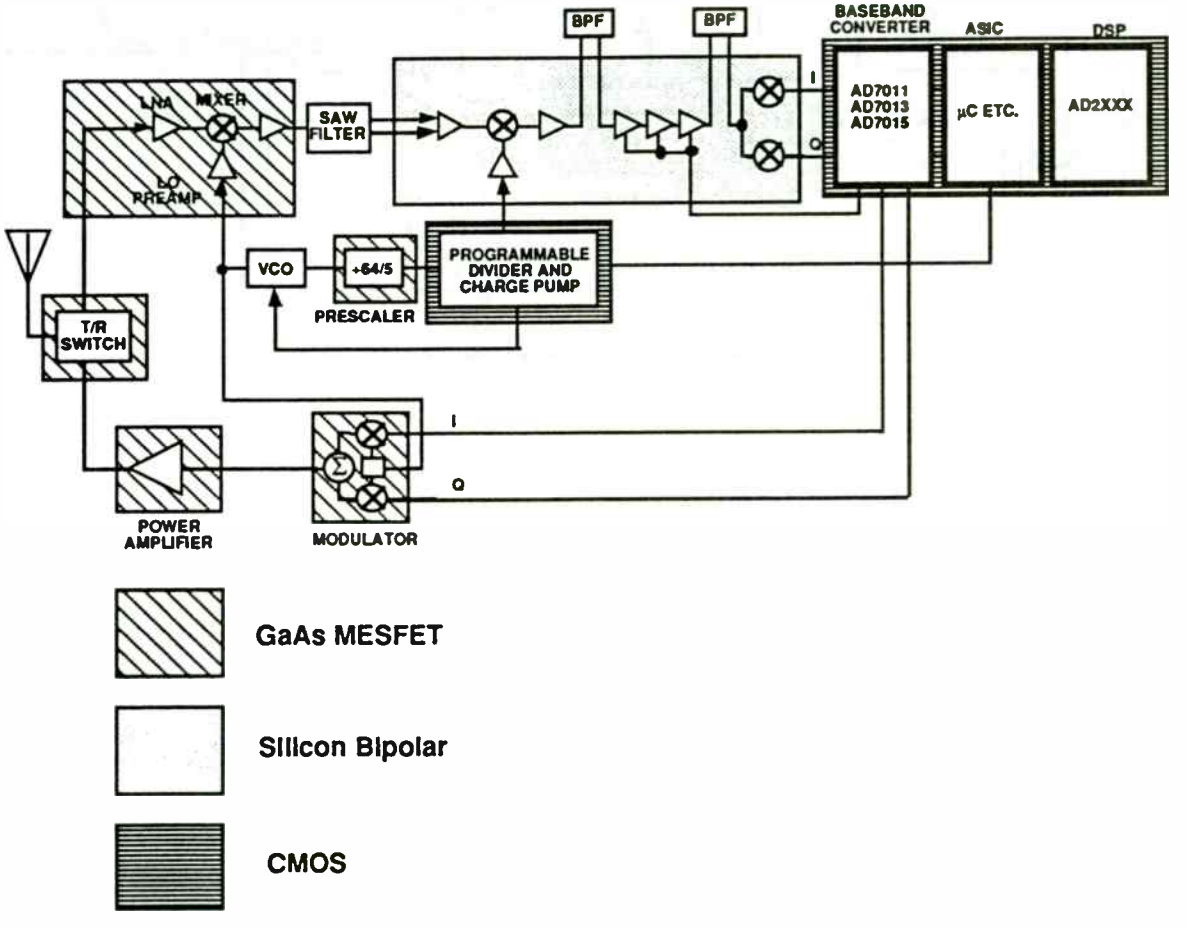

Figure 2. The Same Dual Conversion GSM Transceiver Showing Partitioning Into ICs using GaAs, a moderate-speed Silicon Process, and CMOS

What about all-NPN and BiCMOS processes? Figure 3 shows an approach in which functions are combined using high-speed bipolar and BiCMOS processes, each with NPN transistors having an $f_t \geq 20$ GHz. Integrating the charge pump and prescaler is a tradeoff between the reduced components count due to integration and the added cost of the BiCMOS process for a single function.

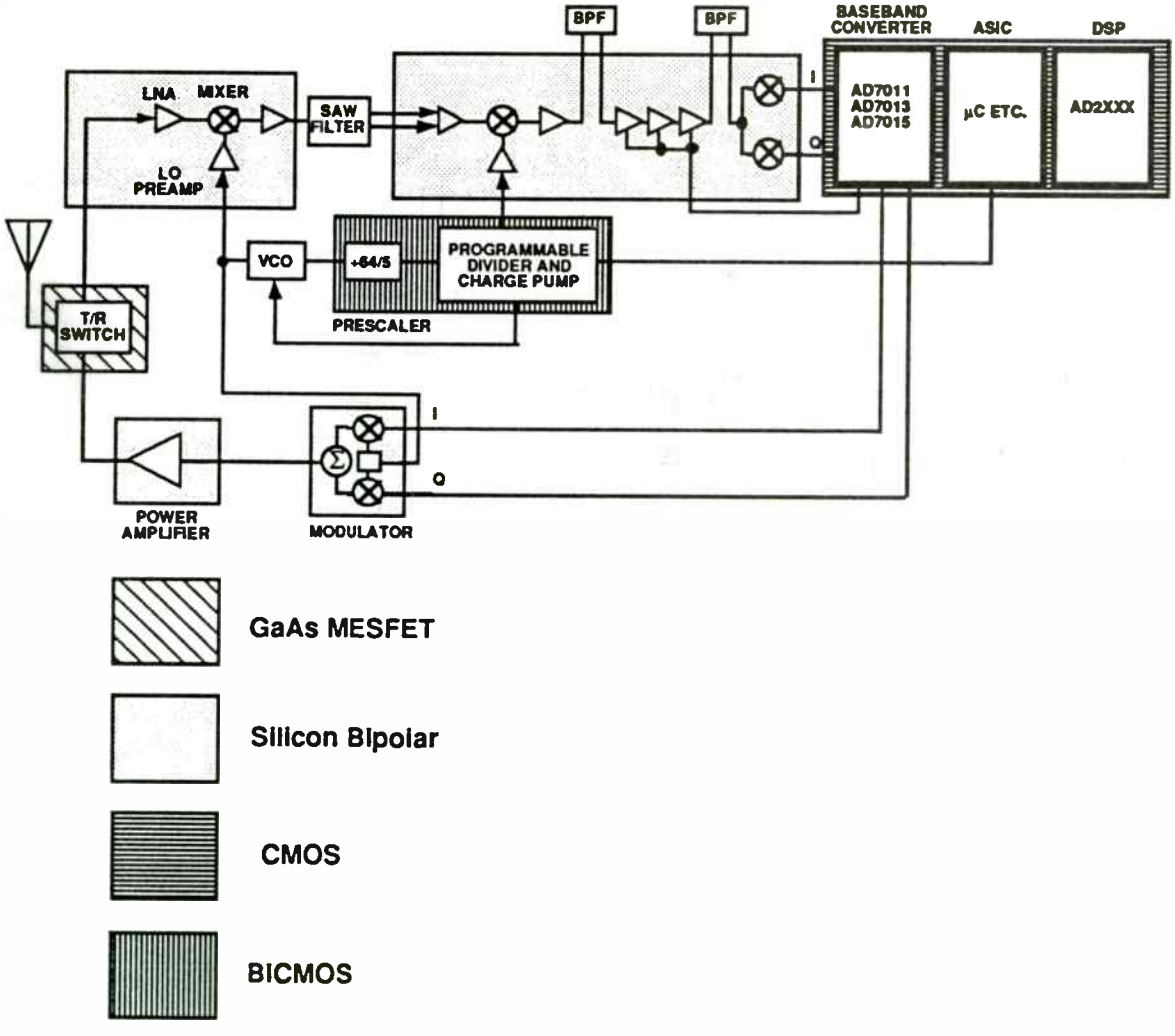

Figure 3. The Same Dual Conversion GSM Transceiver Showing Partitioning Into ICs using GaAs, a high-speed ($f_t \geq 20$ GHz) Silicon Process, a high-speed BiCMOS Process, and CMOS

This tradeoff can be avoided by careful partitioning (Figure 4) : placing all moderate and low-speed digital functions and some analog functions (the PLL and charge pump) in a CMOS process and the RF/IF functions and the high-speed prescaler in a high speed silicon bipolar process. The T/R switch remains GaAs. Th power amplifier can be in the same bipolar process, but due to heat dissipation will remain in a separate package.

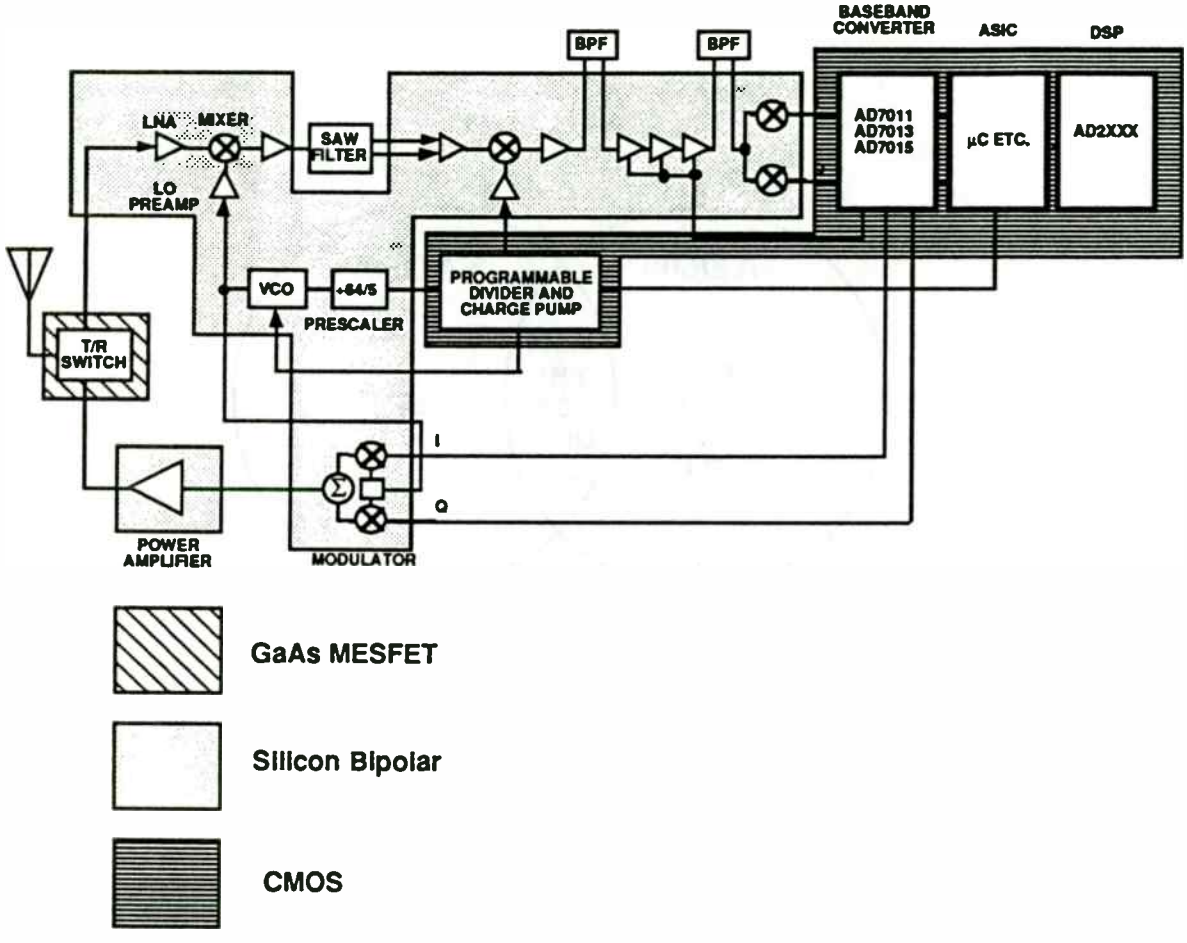

Figure 4. The Same Dual Conversion GSM Transceiver Showing Partitioning Into ICs using GaAs, a high-speed (f_t≥20 GHz) BiCMOS Process, and CMOS

In order to meet these requirements, we've developed small, low-power, IF ICs for two demodulation schemes, the AD607 and the AD608. Both are used in such applications as PHP, PCN, DECT, CT2, and GSM (**Figure 5**) where the modulation mode is some form of phase-shift keying (PSK). Either the AD607 and AD608 can be used in the signal chain with the appropriate demodulator.

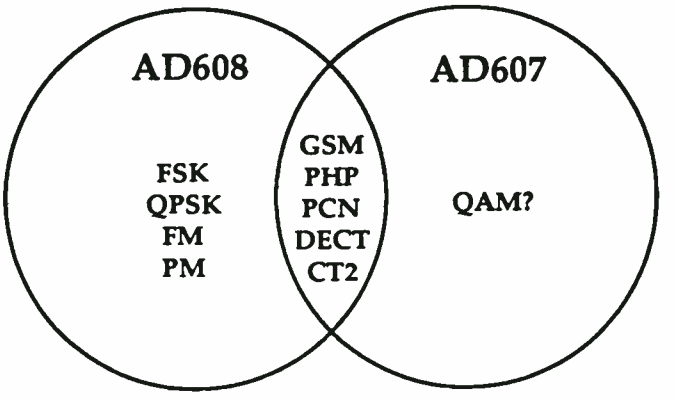

Figure 5. Applications solution space showing mapping of AD607 and AD608 into important standards and modulation modes

The choice of part depends on the customer's architecture. The standard architecture in GSM and PHP uses a rectangular representation of the signal, that is, S(t) = I(t) + Q(t), and requires a linear IF (**Figure 6**) such as that proposed in the AD607. In this architecture, a baseband converter consisting of two signal inputs; each low-pass filters and digitizes the I(t) and Q(t) outputs of the IF IC's quadrature demodulator. An equalizer (in DSP) then determines the correct MGC voltage (or digital signal) to change the IF IC's gain to "center" the signal in the dynamic range of the baseband converter. The equalizer calculates the RSSI value as part of this process.

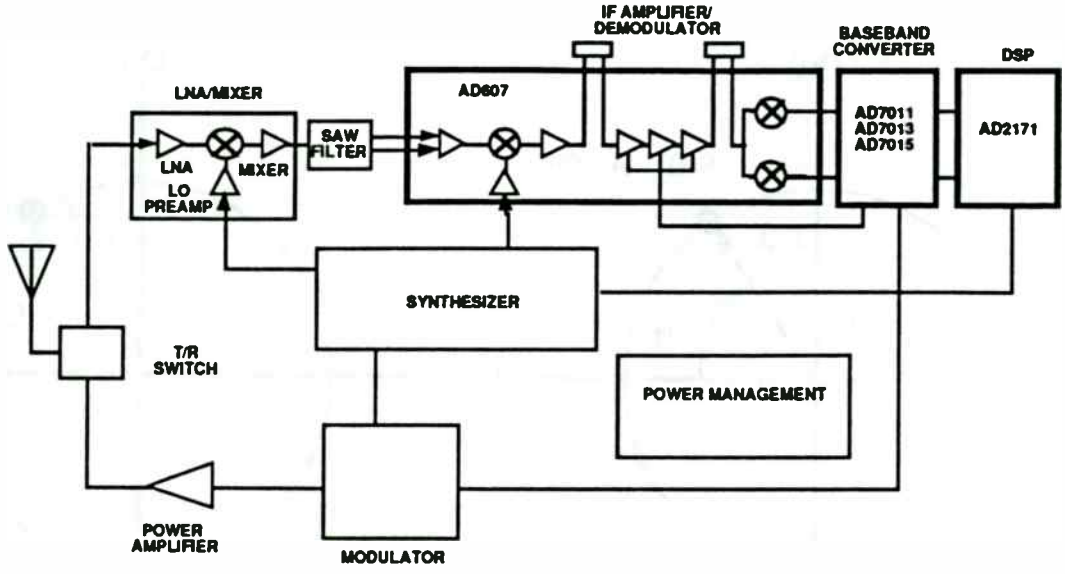

Figure 6. DMR Receiver using Quadrature (I and Q) Demodulator

The other architecture (Figure 7) uses a polar representation of the signal, that is, $S(t) = Ae^{j\phi(t)}$. In this architecture, a digital "baseband converter" uses a digital demodulator (a counter, for example) that measures the phase of the AD606's hard-limited output to provide the signal $\phi(t)$ and uses an ADC that digitizes the RSSI output of the AD606 to measure the amplitude A(t).

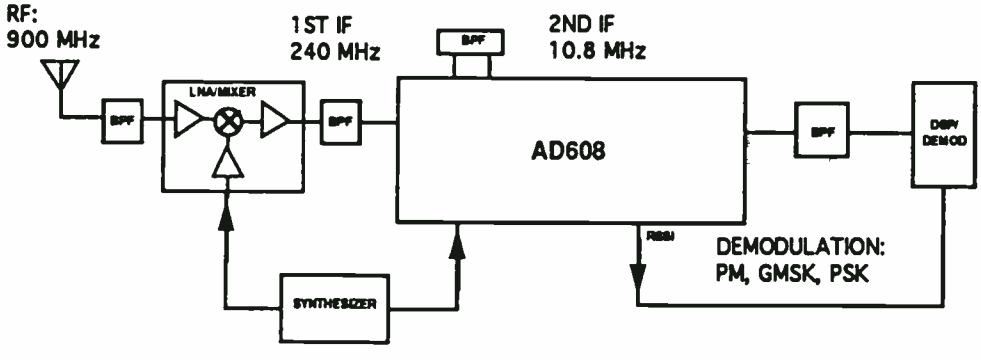

Figure 7. DMR Receiver using Phase Demodulator

Figure 8 shows the polar and rectangular representations for comparison. Both vectors point to the same point on the unit circle. The conversion between the coordinate systems is $S(t) = I(t) + Q(t) = Ae^{j\phi(t)}$ where $A(t) = \{ I(t)^2 + Q(t)^2 \}^{1/2}$ and $\phi(t) = \arctan\{ Q(t)/I(t) \}$.

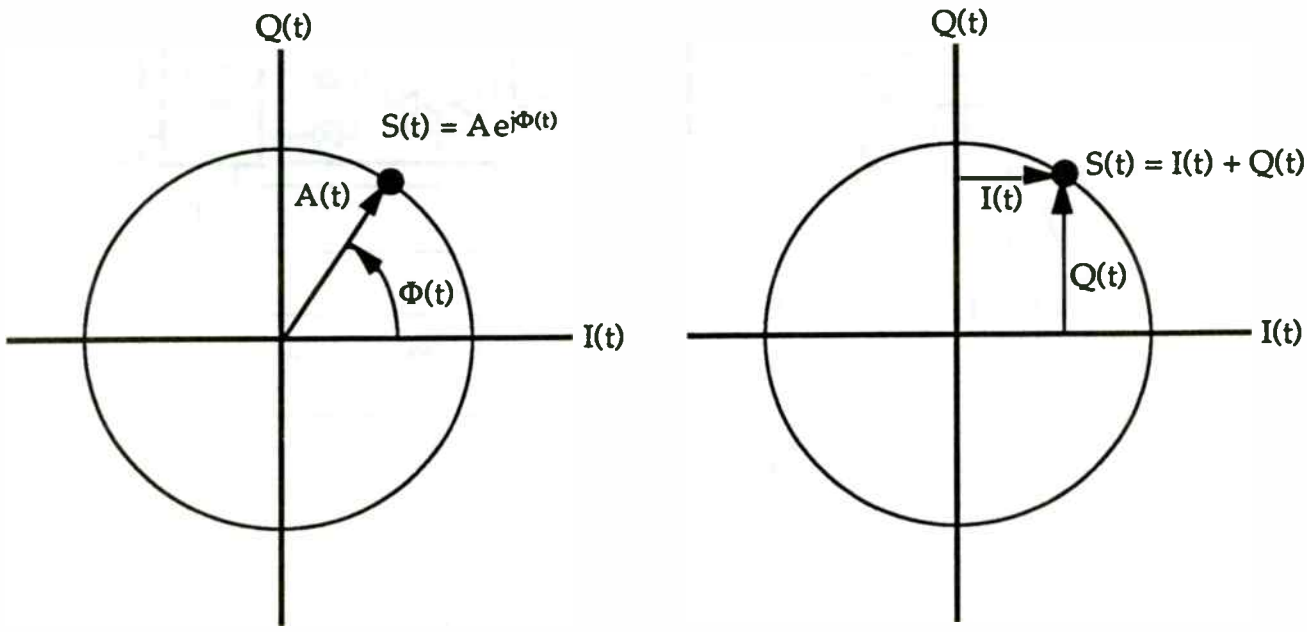

Figure 8. Polar (left) and rectangular (right) representations of phase-modulated signal

Choice of IFs

From a system perspective, both are designed for a dual conversion system, using a first IF of approximately 240 MHz and a second IF of 10.7 MHz (6.5 MHz may also be used). Why these IFs? The exact intermediate frequencies are the user's choice, but SAW filters for frequencies above 200 MHz are smaller, have lower insertion loss, and cost less than those in the <100 MHz frequency range. As for the second IF, 10.7 MHz filters (used in FM broadcast receivers in the US) are low cost and widely available. (Filters for 6.5 MHz, a TV audio IF, are available in Europe.)

The AD608

Now let's narrow our focus and use the AD608 IF subsystem IC (Figure 9) as a case study. In order to keep both the price and package size down, we minimized the pin count and fit the part in a low-cost, industry standard 16-pin narrow-body SOIC. This package had several advantages: from a cost point of view, it was cheaper than the 20-pin SSOP currently in vogue. From the customer's point of view, it was within 10% of the same size. From the perspective of our manufacturing and assembly engineering people, we already had a handler and trackwork in house and we had a suitable lead-frame for the die size. From a performance point of view, the lead spacings are wider than those of the 20-pin SSOP, leading to a reduction in the capacitance between leads and less likelihood of oscillation.

Process Simplifies Design, Reduces Power

The process is a 3-GHz dielectrically-isolated process called XFCB, for "Extra Fast Complementary Bipolar". In this and other IF amplifier designs, dielectric isolation has advantages over junction isolation: transistors can now be treated as three-terminal devices because the parasitic capacitances are minimized and the junction capacitances (e.g., C_μ in the hybrid-π model) are smaller than those of a junction-isolated process with a similar f_t. The result is that the high frequency performance is much better than one might expect due to the f_t alone. The fast PNP transistor simplifies level shifting circuits and reduces the power needed in amplifier output stages. Driving 330Ω filters, for example, was simplified because complementary structures could be used.

The AD608

The AD608 provides both a low-power, low-distortion, low-noise mixer and a complete, monolithic logarithmic/limiting amplifier using a 'successive-detection' technique. It provides both a high-speed RSSI (receiver signal strength indicator) output and a hard-limited output. The RSSI output provides a loadable output voltage of +0.1 V to +2 V. The AD608 operates from a single 2.7V to 6V supply at a typical power level of 20 mW at 3V.

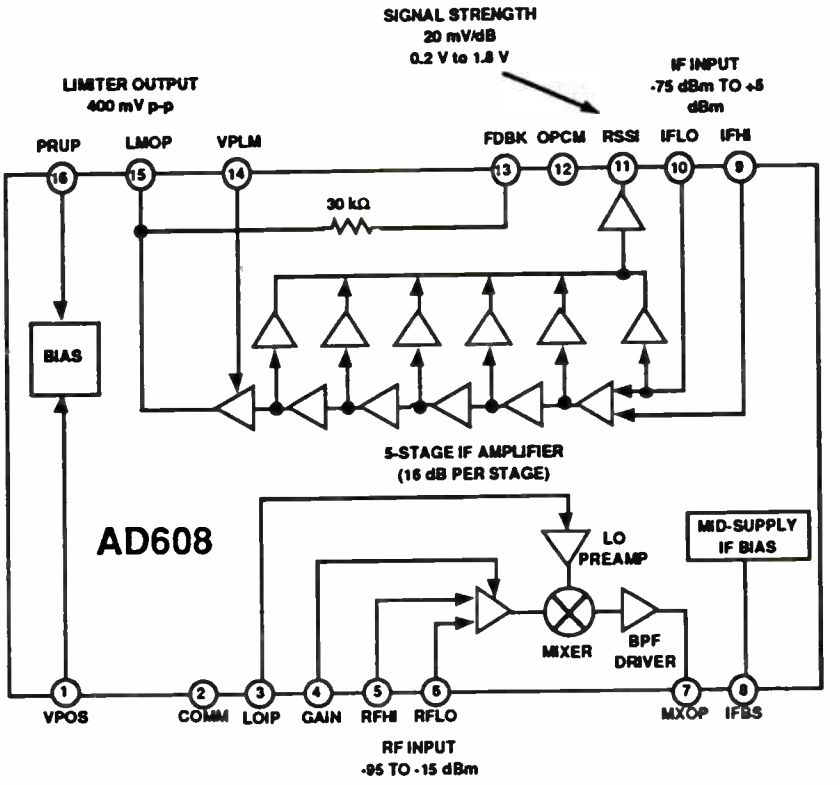

Figure 9. AD608 Functional Block Diagram

The AD608's RF and LO bandwidths both exceed 240 MHz. In a typical IF application, the AD608 will accept the differential output of a 240-MHz SAW filter, amplify it via a 26-dB-gain, low-noise amplifier, and down convert it to a nominal 10.7 MHz IF. (The AD608's log/limiting section handles any IF from LF to as high as 50 MHz.)

The mixer is a doubly-balanced "Gilbert-Cell" type and operates linearly for RF inputs spanning -95 dBm to -15 dBm. It has a nominal 0 dBm third-order intercept. An on-board LO preamplifier requires only -16 dBm of LO drive. The mixer's output drives a reverse-terminated, industry-standard 10.7 MHz 330Ω filter and can drive filter impedances as low as 220Ω.

The nominal logarithmic scaling is such that the output is +0.2 V for a sinusoidal input of -75 dBm and +1.8 V at an input of +5 dBm; over this range the logarithmic conformance is typically ±0.4 dB. The logarithmic slope is proportional to the supply voltage.

The AD608 can operate above and below these input levels, with reduced linearity, to provide as much as 90 dB of conversion range. An feedback loop circuit automatically nulls the input offset of the first stage down to the sub-microvolt level.

The AD608's limiter output provides a hard-limited signal output at 400 mV p-p. The voltage gain of the limiting amplifier to this output is more than 100 dB. Transition times are 7 ns and the phase is stable to within ±3° at 10.7 MHz for signals from -75 dBm to +5 dBm.

It is enabled by a CMOS logic-level voltage input, with a response time of 150 ns. When disabled, the standby power is reduced to 3 µW within 5 µs.

Under the hood

Internally, the AD608 contains some departures from standard designs. For example, the mixer contains special linearizing circuitry to extend its linear operating range: The 1-dB compression point is -15 dBm and the third-order intercept is 0 dBm, both 10 to 15 dB higher than those of other IF ICs, yet the total power consumption is less than 30 mW using a 3V supply.

The circuit for driving the filter is also different. Most designs use a voltage output that drives a termination resistor in series with the filter. The AD608's mixer uses an output in the form of a current that drives a termination resistor in parallel with the filter. This difference, plus the fact that the filter's AC ground is biased at 1/2 the supply voltage, reduces the overall power consumption at high signal levels.

The AD608's logarithmic amplifier section is a third-generation design, the first two generations being the AD640, a five-stage log amp, and the AD606, a 9-stage log amp (**Figure 10**). The logarithmic amplifier section is a five-stage successive-detection, each stage contributing 16 dB to the overall logarithmic response. **Figure 11** sows the accuracy of the RSSI response.

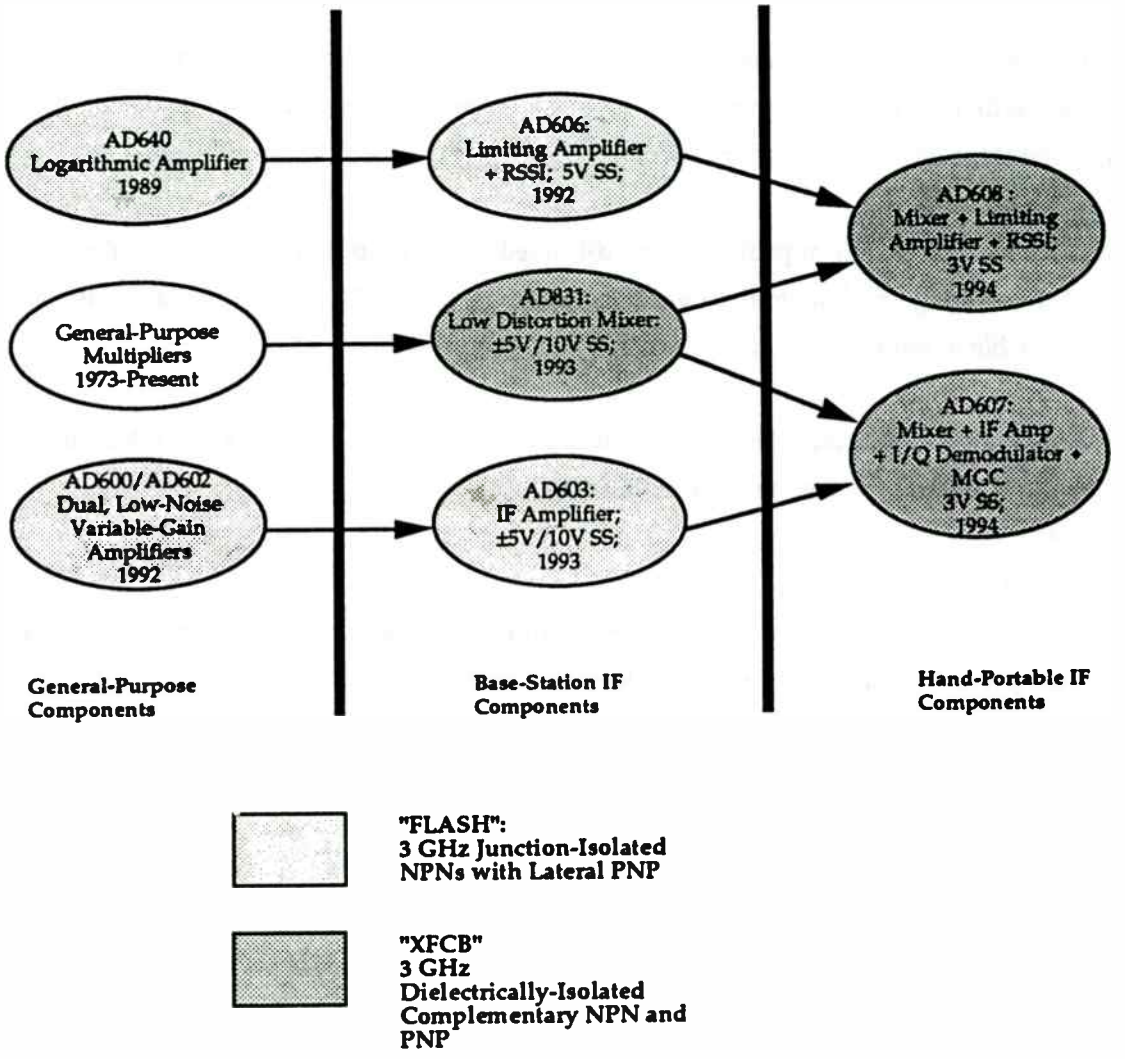

Figure 10. Three Generations of Log Amp Designs

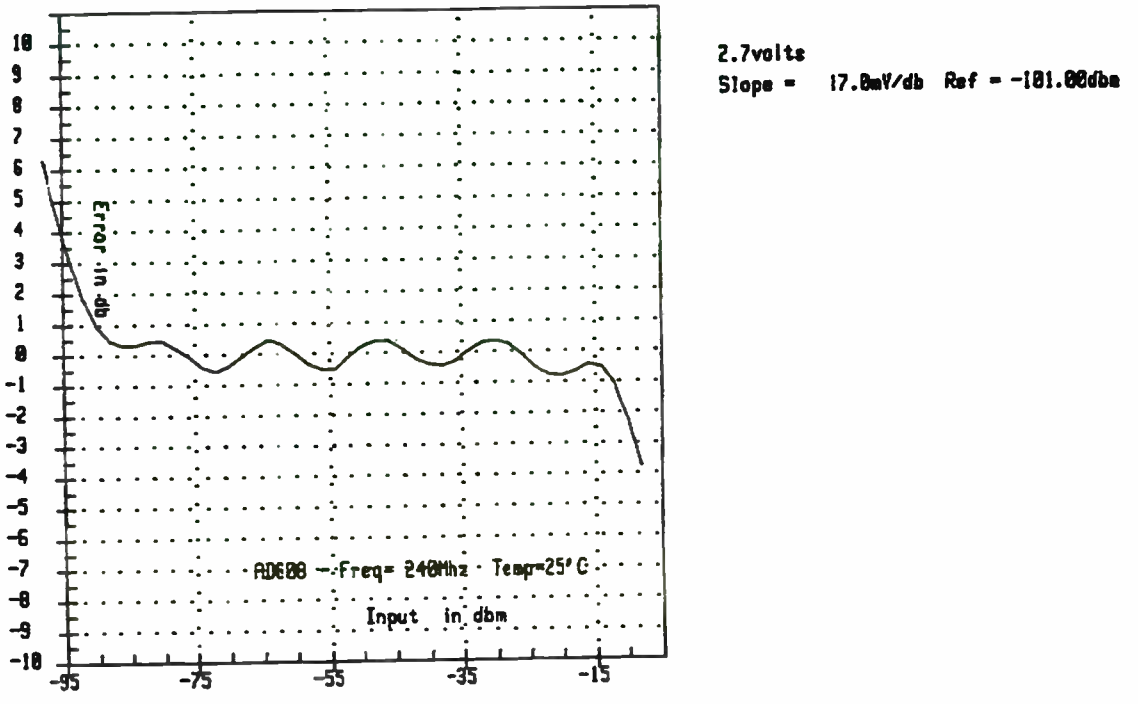

Figure 11. AD608 RSSI Accuracy

In Use

The limiter response of the AD608 (±3° over an 80-dB input range) gives it immunity to deep fades such as those caused by a car driving under a bridge or a user passing behind a barrier. Its fast RSSI response time allows the phone to instantly respond to incoming data — there is neither an RSSI voltage for a DSP to compute nor an AGC loop to settle.

Direct Digital Synthesis/Direct Digital Modulation

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This paper will discuss the emergence of an exciting new level of integration and functionality: direct digital synthesis (DDS). While the principal of DDS has been known for many years, it has only been with the availability of low-cost implementations (such as the AD7008) that it is now being considered as a viable technique for commercial applications. This paper will focus on two areas:

--local oscillator synthesis using DDS:

The demands placed on oscillator designers to provide faster switching local oscillators (LO) with greater frequency-hopping capability, to be used with the developing digital communication standards, require new techniques to provide effective solutions. Currently, the LO area is where DDS has been given most attention, working in combination with traditional techniques, to provide new solution architectures with a distinct set of advantages and limitations.

--direct digital modulation using DDS:

With the on-going development of new digital communication standards, the ability to implement different modulation schemes with DSP software and DDS may prove to be very attractive. Here, we will discuss how some of the more common digital modulation techniques, such as Gaussian Minimum Shift Keying (GMSK) and $\pi/4$ Differential Quadrature Phase Shift Keying can be implemented using DDS.

The combination of DDS and Direct Digital Modulation leads to radically different system architectures, with various tradeoffs. This may prove more appropriate for certain design challenges which require design flexibility and improved performance at a lower cost.

Integrated-Circuit Solutions

Session Chairperson: John Brewer,
Tektronix, Inc., Microelectronics Div. (Beaverton, OR)

ARCHITECTING RF SUBSYSTEMS USING INTEGRATED R.F. CIRCUITS FOR WIRELESS COMMUNICATIONS PRODUCTS

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Over the past 10 years there has been an explosive growth of personal wireless products ranging from pagers to cordless and cellular telephones. Until recently, the RF sections found in these products incorporated very low levels of integration — most consisted of discrete components. However, with the advent of digital cordless and cellular telephony, it became difficult to realize the size, power and cost objectives using discrete components. The need to produce these products in high volume at competitive prices adds to the technological pressure to incorporate much higher levels of integration, including the RF section. As a result of this growing demand, many semiconductor manufacturers are developing integrated solutions for the RF section of personal wireless communication products. This paper explores the factors that impact the greater integration of solid state RF components for personal wireless communications products.

The past decade witnessed the explosive growth in the use of personal wireless telephone products. For example, more than 13 million cellular telephones are now in use in the United States alone. Moreover, more than 60% of all new telephones sold here today are cordless models. Clearly, telephone users want portability. Equipment manufacturers are trying to meet the demand with ever smaller, lighter and less power hungry cordless and cellular products.

To meet the growing demand of more customers, new digital communications standards have been developed to make more efficient use of radio frequency spectrum. These standards increase the user capacity by three times or more by the combination of time division multiplex-

ing (TDM) and digital speech compression. Though there are different systems in use or under development in various parts of the world, all permit at least three users to "simultaneously" share a wireless communications channel.

The use of TDM and speech compression impact the design process because they are far more complex than the older analog technologies. As a result, far more signal processing is required throughout the wireless product's function blocks. Because of this, the new generation of digital wireless products are designed around digital signal processors (DSP).

Concurrent with the need for increased processing power, the market is demanding smaller and lighter products that provide more talk and standby time. Although digital communications provide for more user traffic by increasing channel capacity, the increased signal processing components consume more power to the detriment of increased talk and standby time. Thus, manufacturers are faced with the need to produce far more complex products while at the same time reducing power consumption and holding or even reducing the selling price.

Achieving these seemingly mutually exclusive goals requires higher levels of circuit integration than previously used, not only in the baseband circuits, but also in the RF section. Early attempts at integrating RF circuits were limited to what might be described as small scale integration. Typical examples of the functions performed by these devices include mixers and intermediate frequency amplifiers. More recently, semiconductor manufacturers began grouping functions onto a single die to achieve what might be described as medium scale integration. A typical example of these newer devices is an integrated quadrature modulator. And further levels of integration are needed to fully realize cost, size and power objectives.

To achieve significant improvement, devices must be optimized from a system perspective. Optimizing at the device level brings with it only limited improvement at the system level. What this means is that individual devices may not provide the very best performance when considered separately, but the overall system performance is enhanced. For example, in designing an integrated quadrature modulator, a relatively high output power (typically 0 dBm) must be generated from minimum supply current. To an IC designer, this can be best achieved by driving the output differentially. However, optimizing the

modulator's circuit design leaves the system designer with the problem of driving a single-ended filter with a differential signal from the modulator. Since this usually involves the use of a balun implemented with discrete components, the benefits of integration would be compromised by the dependence on the external components at the system level.

Designing The Optimum RF ICs

It should be understood that "optimum" is defined by each customer. Thus, optimizing is achieved by meeting the customer specified tradeoffs of integration, price, size and power consumption. Different system designers may prioritize these factors differently, depending on their specific development objectives. We will describe the often conflicting implications of balancing these objectives and how they are influenced by the system standard.

System Standards: There are many wireless communications standards now in use or proposed throughout the world. For digital cellular, four standards have been accepted for use: two for the USA (IS-54, based on TDMA, and IS-95, based on CDMA), one for Europe (GSM) and one for Japan (PDC). For digital cordless applications, Europe (DECT) and Japan (PHP) have each adopted a standard but the USA has yet to do so. Although the requirements set forth in the various standards affect all portions of a wireless communications product, their effect on the RF section is very significant.

These standards, for example, set the frequency range, channel bandwidth, output power level, receiver sensitivity, minimum signal-to-noise ratio and other operating parameters. Table 1 lists these and other parameters for the various systems. Some of these have a direct impact on the levels of integration achievable, and are discussed below.

System	Channel	Access/Duplex	TxRF	RxRF	TxPower	Frame ÷ slots
IS54/55	30KHz	a)FDMA/FDD b)TDMA/TDD	824 – 849 MHz	869 – 894 MHz	0.6 W (Class IV)	a) N.A. b)40 ms ÷ 6
Japan PDC	25 KHz	TDMA/TDD	810 – 826 MHz	940 – 956 MHz	0.8 W, 0.3 W (Class III, IV)	40 ms ÷ 6
GSM	200 KHz	TDMA/TDD	890 – 915 MHz	935 – 960 MHz	2W, 0.8 W (Class IV, V)	4.6 ms ÷ 8
DECT	1.7 MHz	TDMA/TDD	1.88 – 1.9 GHz	1.88 – 1.9 GHz	0.25W	10 ms ÷ 24
Japan PHP	300 KHz	TDMA/TDD	1.88 – 1.9 GHz	1.88 – 1.9 GHz	0.01 W	5 ms ÷ 8

Table 1: Standard-specified Parameters for Various Systems

Transmit Power: To compensate for filter losses between the power amplifier and the antenna, the power amplifier output level must usually exceed the specified radiated power by up to 50%. To protect the receiver against overload from the transmitter power amplifier, a duplex filter is required. These devices, however, are fabricated using different technology than either the receiver's low noise amplifier (LNA) or the transmitter's power amplifier (PA). LNAs and PAs are usually implemented using gallium arsenide (GaAs) technology because of the intrinsic characteristics of GaAs for lower noise (for the LNA) and higher efficiency (for the PA). This means that a single integrated circuit cannot be used to implement the duplex filter, LNA and PA.

In lower power systems, such as digital cordless telephones where the radiated power levels are several hundred milliwatts, a duplex filter is not required. Instead, a simple switch can be used to toggle between receive and transmit modes. In these systems, the switch can also be implemented in GaAs technology, making a fully integrated front-end (switch, LNA and PA) realizable.

Channel Bandwidth: Wide channel bandwidths (GSM, DECT and PHP) imply S.A.W. IF filters, suggesting the IC will interface to a medium impedance. However, IC output nodes driving these are likely to be the collectors/drains of active RF mixers which have high source impedances. As a result, the matching networks will be somewhat more sensitive to matching component tolerances than if the source impedance is low. This may make achieving the passband characteristics of the S.A.W. more difficult without premium matching components. A lower source impedance may be easier to match but is likely to be more wasteful of supply current needed to bias the output.

TDMA Timing: Biasing of inputs and outputs is an important consideration in TDMA systems in which power can be saved by turning off the radio during idle time slots. In the IS54/55 and PDC systems, there is an idle period of up to 13.3 milliseconds between active slots for either transmit or receive. However, large external coupling capacitors may be needed if the operating frequency, or the source or load impedance, is low, or a matching network design specifies it. Four milliseconds or more may be required to charge large coupling capacitors. As a result, supply current may be wasted by having to power up prematurely to allow a high-impedance IC bias circuit to charge the external capacitors. So, it is beneficial to plan

for low time constants, relative to the time slot length, for external reactance interfaces to the I/O of an RF IC.

Transmit-Receive Frequency Offset: Reduction of the RF VCOs into one unit integrated with other subcircuits is often desirable. The VCO frequency rate of change is a consideration that can be inferred from Table 1. In both IS54/55 and GSM, the transmit/receive offset is 45 MHz in the TDMA mode. In IS54, the VCO must change 45 MHZ in about 2.2 milliseconds (20.5 MHz/msec) while in GSM the change must occur in 1.1 milliseconds (41 MHz/msec). Settling time specifications overlay the gross frequency transition requirements and together these implicate feasibility of IC design, and the IC-to-board interface as well.

Power Consumption Objectives: As previously mentioned, portability is a key objective for wireless communications products. Many factors affect the power consumption of the electronics, including the electrical requirements imposed by the standards, battery voltage and semiconductor technology used to implement the electronics.

One fundamental characteristic of the semiconductor process will be mentioned here along with some of its consequences. The operating bandwidth of transistors made in a process are especially the result of its fT, bias currents and voltages, and parasitic capacitances. The opportunity to integrate often involves high frequency functions formerly relegated to discrete components (LNA, active RF mixers, IF amplifiers and active phase shifters). For these to be feasible, the transistors must have adequate bandwidth at acceptable levels of supply current. Restated, the opportunity to minimize supply current of integrated radio functions at a given operating frequency depends inversely on the bandwidth of the semiconductor process. The challange facing the designer is extending battery life to provide more operating time while minimizing size, weight and cost.

In the RF subsystem, the power amplifier is the primary consumer of power when the unit is in the talk mode. Although optimizing the power amplifier can significantly impact overall power consumption, power savings also can be achieved elsewhere in the RF section. Consider, for example, the receiver's overall gain. It may be realized at RF frequencies, but that strategy would consume significantly more power than putting most of the receiver's gain at a lower intermediate frequency. A design analysis may show that even more savings can

be achieved by adding another mixer and down converting again to an even lower intermediate frequency.

Representations of a single- and dual-conversion receiver are shown in Figures 1a and 1b. As can be seen, the single-conversion architecture consumes 3 milliamps more in the IF stages than the dual-conversion design because it employs more circuitry at higher frequencies. The RF, first IF and baseband frequencies are comparable in both designs. Note, however, that the dual-conversion design requires more external components. The tradeoff between increased power consumption and increased external component count will be viewed differently by each customer.

External Components: The whole point of turning to higher levels of integration is to minimize the number of components and their associated costs. However, some functions have not yet been incorporated into integrated solutions. This is especially true in RF circuits due to the extensive use of inductors and capacitors. While smaller values of inductance and capacitance may be indispensable when fabricated on a monolithic semiconductor, their use in some functions is limited by sensitivity to bias voltage, Q or current density. So, for many high frequency applications, external inductors or capacitors are required. The problem is compounded by the die area needed to implement larger capacitor and inductor values because more chip area means higher chip cost.

Figure 1a & 1b: Comparison of Tradeoffs in Integration of Two Radio Receiver Architectures

(All Amplifiers, Mixers, and Baseband Filter Assumed Candidates for Integration)

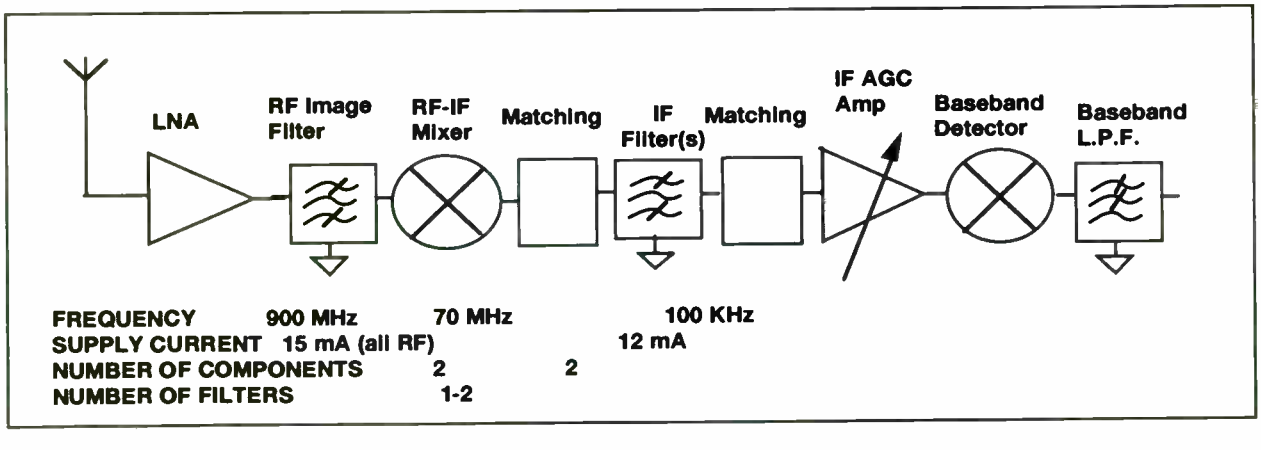


Figure 1a: Single IF Heterodyne Receiver Architecture

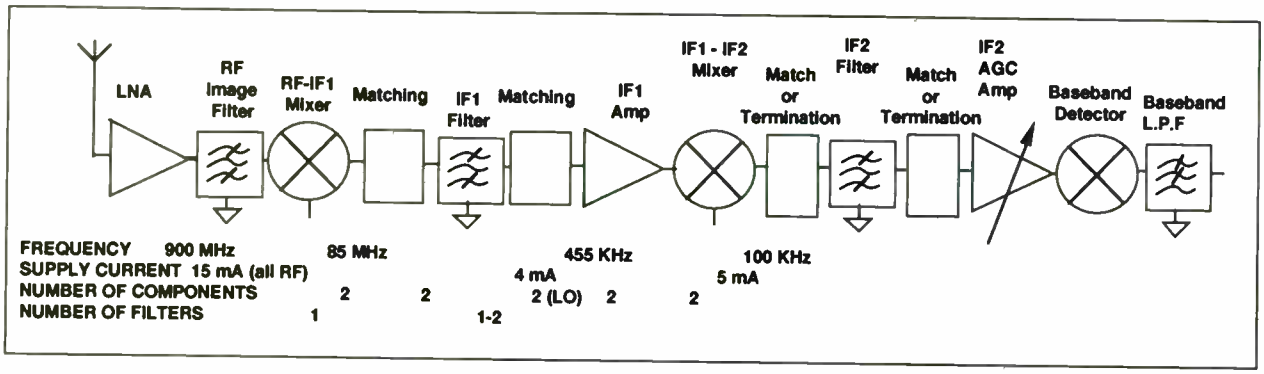


Figure 1b: Dual IF Heterodyne Receiver Architecture

Also, when considering RF architectures, external components required as part of the architecture must be seriously considered. It is of no use to realize an advanced IC architecture that places unrealizable demands in terms of performance, size and cost on external components. Consider again the example of the single- and dual-conversion receivers. The implications of external IF filters are shown in Figures 2a through 2c.

Figure 2a-2c: Relationship of Receiver Complexity to Achievement of Required Channel Selectivity

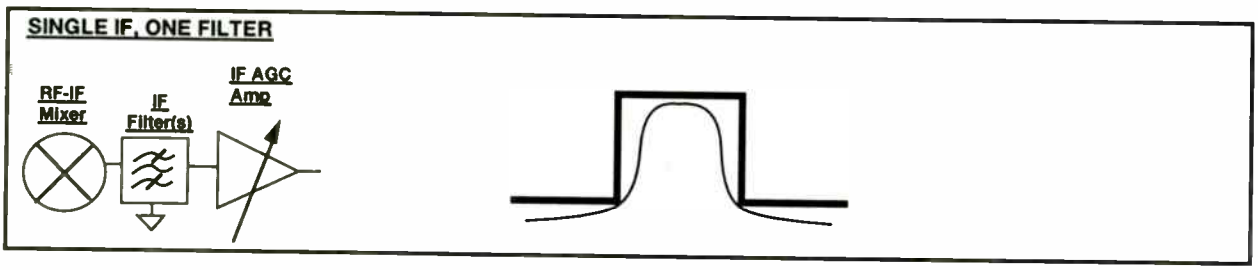


Figure 2a: Single IF Architecture — One IF Filter

Figure 2a illustrates an ideal single IF heterodyne receiver architecture, which requires a minimum of filters and filter matching components. However, a filter with adequate selectivity for the system requirements may not be available, or may be expensive. At the same time, the IF frequency must be high enough to avoid demodulating two channels in the same band. Since the IF frequency will be higher, more supply current will be required to provide the full IF gain.

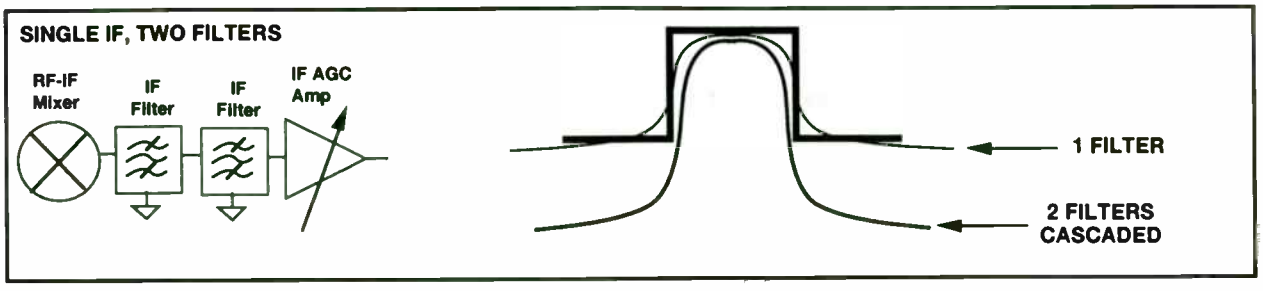


Figure 2b: Single IF Architecture — Two IF Filters

Figure 2b illustrates an architecture similar to that shown in Figure 2a but with one filter replaced by two. The two duplicate filters are more likely to be readily available but if they are S.A.W. filters they may consume a large amount of board area. And, as in Figure 2a, the IF must be higher and, as a result, the supply current needed for full IF gain will also be higher.

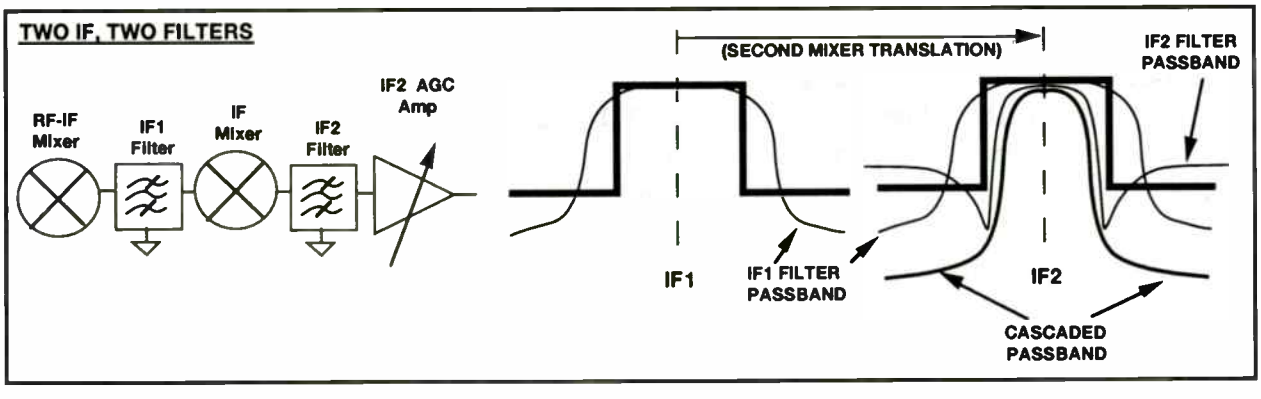


Figure 2c: Dual IF Architecture — Two IF Filters

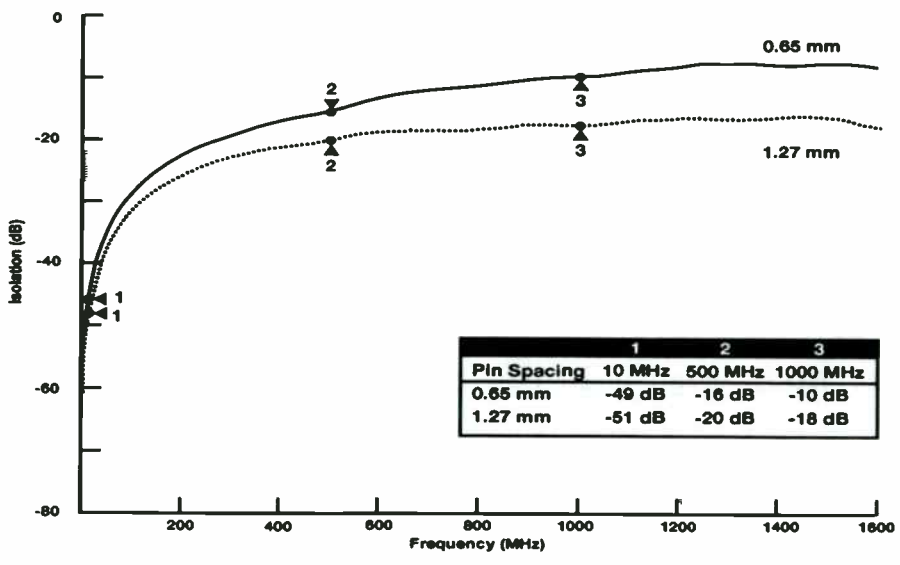
Figure 2c illustrates a double-conversion architecture using readily available first and second IF filters, which together provide the required selectivity. The first IF filter requires matching components but the second IF filter, which operates at a lower frequency, can be terminated with resistors because power transfer is not critical. Also, high gain can be provided with minimum supply current.

Size Objectives: Users of wireless communications want unobtrusive products that can be slipped into a pocket or other convenient location when not in use. Therefore, the physical size of the elec-

tronic components are continually forced to be smaller and smaller. This is often achieved through higher integration and advanced packaging. Of course, the cost objectives are also being reduced, which limits packaging options.

The need for low cost dictates plastic packaging, but the need to operate at up to 2 GHz raises interesting challenges. Challenges also arise from the need for small, low-profile packages with high lead counts which results from higher levels of integration. Limiting package size, however, means decreasing the space between leads, which increases inter-pin capacitance and inductive coupling. At a few hundred megahertz, this capacitance has little effect on performance but in the gigahertz range it can create significant problems. Also, as the packages grow in pin count and size, bond wire inductance from the die to the package leadframe can significantly degrade performance.

The effect of reduced pin-to-pin spacing is decreased isolation. While very good isolation can be achieved on an integrated circuit die, bringing signals out onto I/O pins degrades isolation. Reduced pin spacing, necessary for smaller packages or higher pin counts, also degrades isolation. The simplest example of the impact on isolation is an input and output at the same frequency. If the integrated circuit provides more gain than the package provides isolation, the subcircuit will be unstable. Figure 3 plots adjacent pin isolation for a 28-pin gullwing SOIC package with 1.27 millimeter spacing and a similar package with 0.65 millimeter spacing. As can be seen, isolation decreases as pin spacing decreases. It can also be seen that isolation decreases as frequency increases.



Pin Spacing	1 10 MHz	2 500 MHz	3 1000 MHz
0.65 mm	-49 dB	-16 dB	-10 dB
1.27 mm	-51 dB	-20 dB	-18 dB

Figure 3: Adjacent Pin Isolation vs. Frequency

Another example in which isolation is critical is the situation where two pins — an output and an input — are coupled through a highly selective external filter. Successful monolithic integration of the subcircuits at both ends of the filter depends on isolation for filter stopband frequencies being comparable to the filter rejection.

Beyond simply degrading circuit performance, increased pin-to-pin capacitance increases the potential for crosstalk. Often a designer must separate what would have been adjacent pins with a third pin connected to a signal ground to shield the two pins from each other. Thus, shrinking the distance between pins can become counterproductive if it results in the need for additional 'shielding' pins to eliminate the potential for pin-to-pin crosstalk.

Reduced pin spacing results in decreased isolation because reactance between the pins increases but this increased reactance can be compensated with external matching networks. Thus, even when the problem of decreased pin-to-pin isolation is solved at the package level by interleaving signal ground pins, coupling between external components may degrade isolation. In some cases, circuit design can actively manage I/O impedances so that external compensation networks can be minimized.

The examples given represent only some of the important factors that affect a wireless communications product's size, weight, efficiency and cost. We have treated some of the effects of system standards, power, size and external components on RF integration as separate factors when this could not be further from the truth! Decisions in devising the optimum RF architecture actually involve reaching the most acceptable compromise amongst all the conflicting requirements. Trading off costs, the number of external components, power and level of integration is the IC and systems designer's challenge. Regardless of what factors are taken into consideration during the design process, it is important to approach the design from a systems point of view. Often the optimum solution requires the attention of both the systems designer and semiconductor manufacturers. The key to the whole process, however, is a clear understanding before the project begins of just what constitutes an optimum design in the mind of the customer.

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Performance Analysis of DS-CDMA with Slotted ALOHA random Access for Packet PCNs

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DS-CDMA packet radio with slotted ALOHA (DS-CDMA-S-ALOHA) has the promise of combining the properties of statistical multiplexing from DS-CDMA and random access from slotted ALOHA to achieve higher spectrum utilization for diverse services. While DS-CDMA-S-ALOHA introduces receiver capture capability, it also introduces random interference which will cause random errors. Thus, the performance of DS-CDMA-S-ALOHA protocol will depend not only on the receiver capture but also on the retransmission caused by random errors.

In this paper, a discrete Markov chain based mathematical model is derived. The model captures both the random access and the random errors associated with DS-CDMA-S-ALOHA. The model also captures the effect of adding error control bits to packets. In the paper, in addition to DS-CDMA-S-ALOHA, an idealized protocol — DS-CDMA-S-ALOHA with collision detection (DS-CDMA-S-ALOHA-CD) is also introduced to provide a upper bound for the performance of the system. The derived mathematical model is then used to evaluate the performance of both schemes in addition to the trade-off of adding error control bits in packets.

A Monolithic 915 MHz Direct Sequence Spread Spectrum Transmitter

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The allocation of the Spread Spectrum bands has spawned a wide range of applications which demand high performance designs with economical implementations. This article describes one such design which is a 915 MHz Spread Spectrum transmitter implemented with a minimum number of parts and a low manufacturing cost. An overview of the system design will be presented, however the bulk of the discussion will concern the transmitter ASIC which is a monolithic implementation including the 915 MHz oscillator, a divide–by–eight prescaler, a pseudorandom code input buffer, an up–converting mixer, an AGC amplifier, and an output driver.

SYSTEM OVERVIEW

This design is part of a fault detection system that broadcasts a signal to a remote location, identifying the fault condition. The transmitted signal has to be successfully received at distances up to two miles. The sensitivity of the receiver requires the transmitted signal output be +20 dBm. The total transmitter design fits on a circuit board which is less than 1.5 square inches. As shown in Figure 1, there are two ASICs in the design, the bipolar ASIC described above and a CMOS ASIC. The CMOS ASIC includes a pseudo–random code generator, a crystal controlled oscillator, a phase detector, and an integrating amp. In addition to the two ASICs, the transmitter board contains a prescaler, a regulator, and various passive components.

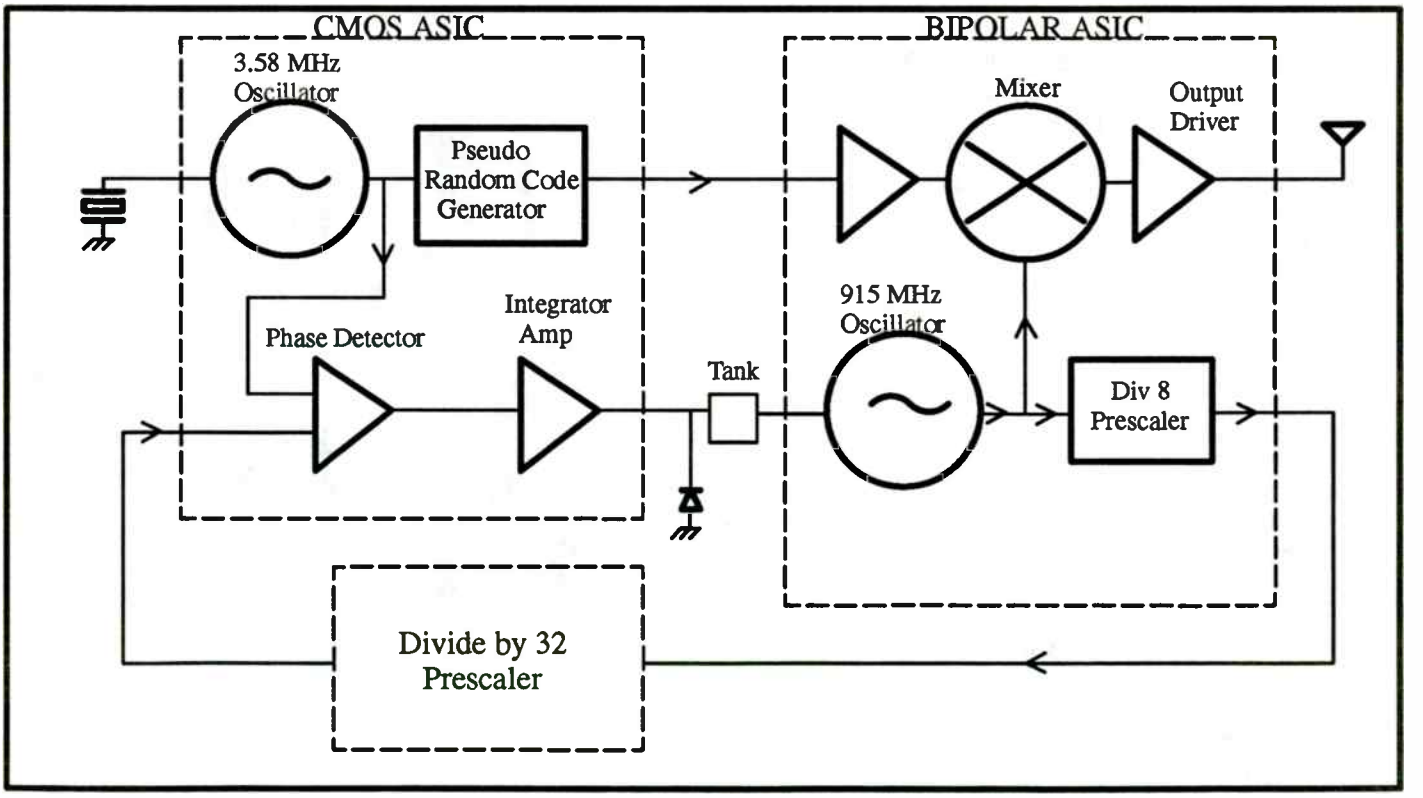

Figure 1. System Overview

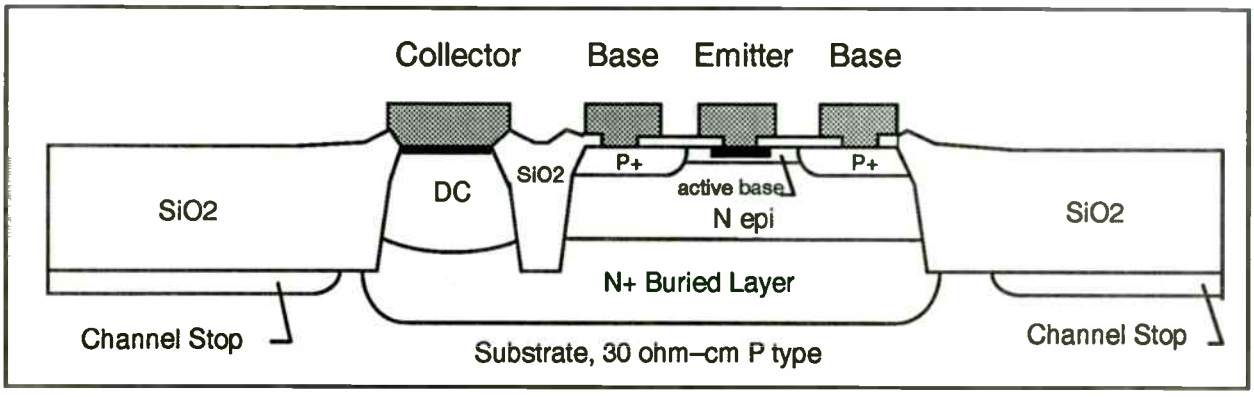

Figure 2. NPN transistor cross section

The crystal controlled oscillator on the CMOS ASIC provides the clock for the pseudo–random code (PN code) generator. The PN code is a 255 bit sequence which is encoded with information using Direct Sequence techniques. In this case there is one bit of information per complete sequence where logic 1 is the normal 255 bit sequence and 0 is the inversion of the sequence. The code is output from the CMOS ASIC to the Bipolar RF ASIC.

The 915 MHz oscillator on the bipolar ASIC is phase locked to the crystal controlled oscillator on the CMOS ASIC. The prescaler function is partitioned between the Bipolar ASIC and the external prescaler. The Prescaler output is compared to the crystal oscillator output by the phase/frequency detector (PFD) whose output remains linear over a range of $\pm 2\pi$ radians. The PFD output drives a high gain charge pump integrator. The filter network for the integrator is performed with discrete devices external to the CMOS ASIC. The voltage output from the integrator is fed back to a varactor diode which is part of the tank circuit in the 915 MHz oscillator.

In the bipolar ASIC the PN code is converted from CMOS logic levels to a differential signal with appropriate levels for the mixer. The 915 MHz oscillator output and the PN code are mixed, resulting in a several MHz flat band signal which is centered at 915 MHz. This signal is passed through a two stage output driver before the antenna. The antenna is a 37 ohm quarter wave monopole.

BIPOLAR TRANSMITTER ASIC

The Bipolar ASIC was fabricated on the Tektronix SHPi oxide isolated process [1] using two layers of metal interconnect and offering npn transistors with an F_T in excess of 9 GHz. A transistor cross section is shown in Figure 2. The design was executed on a QuickChip 6–40 which is a standard array of devices located in fixed positions on the die. The layout was accomplished by interconnecting devices using the two layers of metal. By choosing this standard array we were able to reduce fab time to 4 weeks, reduce the number of masks purchased to four, and significantly reduce the layout time. The QuickChip array provides vertical npn transistors, lateral pnp transistors, JFET transistors, Schottky diodes, MOS and junction capacitors, two types of implant resistors, and optional nichrome resistors. (Figure 3.)

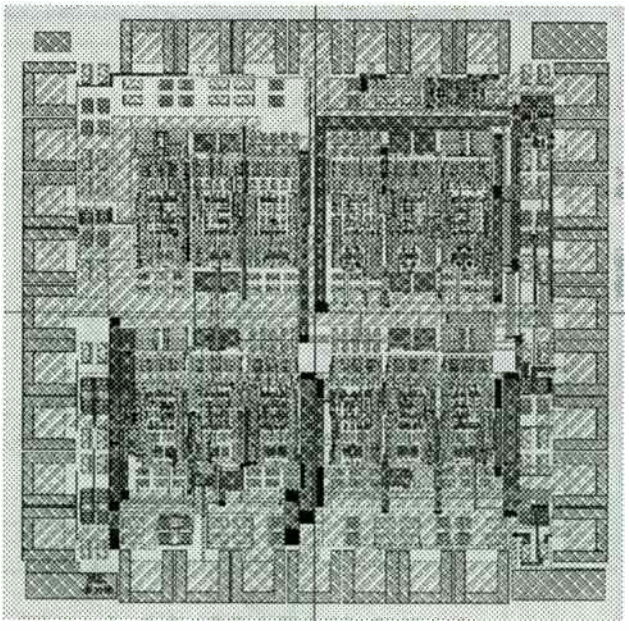

Figure 3. Bipolar Transmitter ASIC layout

An expanded block diagram of the Transmitter ASIC is shown in Figure 4.

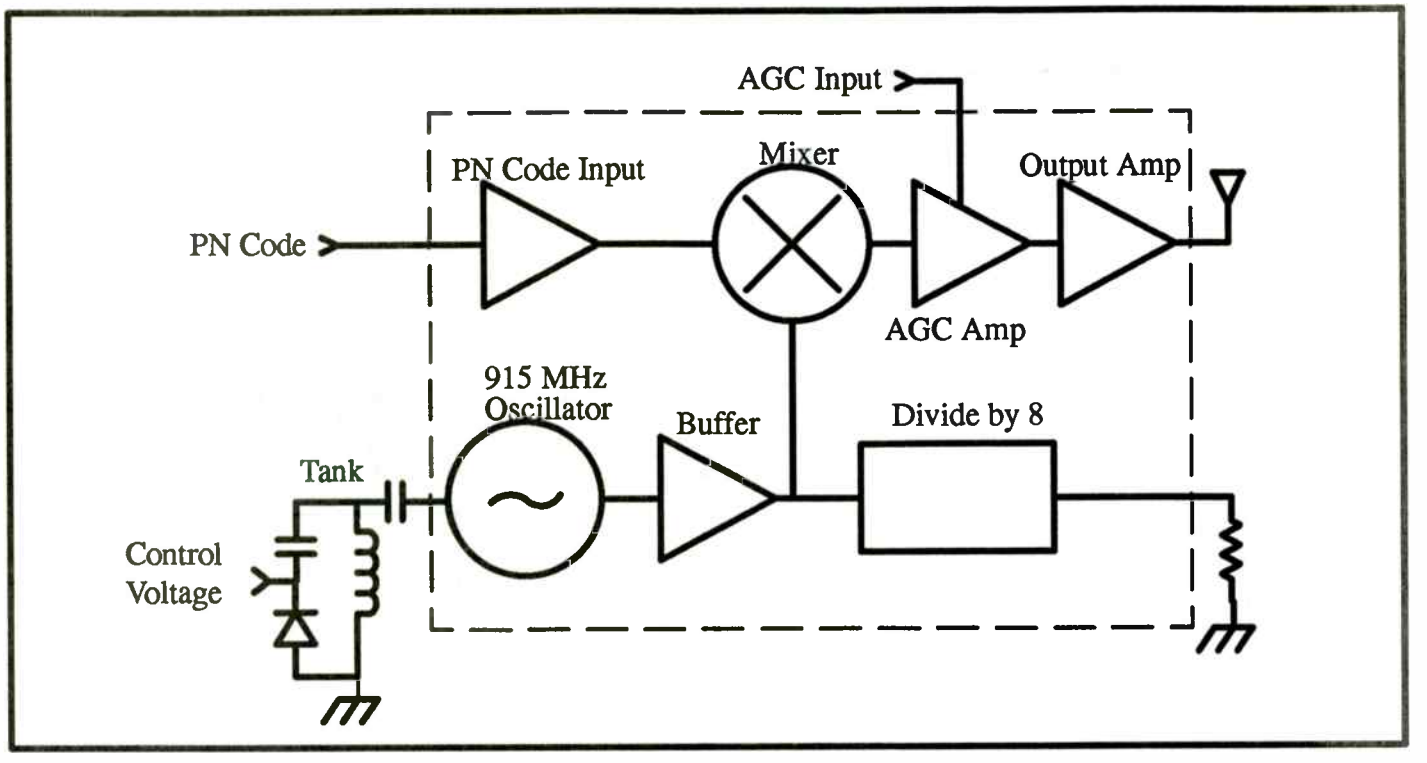

Figure 4. Transmitter ASIC

915 MHz OSCILLATOR

The negative impedance oscillator used in this circuit is single ended and resembles the Colpitts architecture. (See Figure 5.) The principal components include transistor Q7, capacitors C1 and C2, and the external tank circuit. In the tank circuit a varactor diode was used as a means of adjusting the frequency of oscillation. A parallel tank circuit was used to desensitize the oscillation frequency to bond wire inductance. In a negative impedance oscillator the real portion of impedance looking in from the tank is negative at the frequency of oscillation (and for some surrounding bandwidth). It is this negative impedance that allows the circuit to oscillate. The reflection coefficient looking into a negative impedance is more than one, which implies a continually growing oscillation at the resonant frequency of the tank. The factor limiting the amplitude of oscillation varies in different oscillator architectures. However a convenient way to view amplitude limits can be presented with a series resonant tank. In a series resonnant tank there will be a parasitic resistance in the L and the C tank elements and the trace connecting the elements and the oscillator on the IC. The relationship between this resistance and the inductance and capacitance of the tank can form the main contribution to determining the Q of the circuit where;

$$Q = \frac{1}{R} * \sqrt{\frac{L}{C}}$$

During a cycle of oscillation the sinusodal voltage variation changes the input impedance of the oscillator from the initial impedance at the DC bias point. This is due to large signal effects on the bias point of the transistor base. When the magnitude of the negative resistance of the oscillator equals the parasitic resistance then the oscillation amplitude will grow no further.[2][3]

The oscillation at the tank is transferred to the emitter of Q7 where it is converted to a current. This current is mirrored from Q8 to Q9. Q10 is a cascode stage used to increase the bandwidth. The mirrored current is converted to a voltage across R9. This signal is buffered by Q1 and fed into the single–ended–to–differential stage (Q2, Q3). R10 biases the undriven side of the differential stage (Q3). C3 provides an AC ground at this input. The signal is amplified across the differential pair, Q2 and Q3. One draw back to differential conversion using this technique is that the DC voltage dropped across R10 forms an offset on the Q3 side of the amplifier. To minimize the offset R10 must not be too large.

The initial amplitude of the oscillation at the tank is determined by large signal phenomena. Because it is difficult to predict the exact amplitude of the oscillation at the tank, the oscillator was designed to limit at the Q2–Q3 amplifier for all temperature and process conditions. Thus the limiting conditions of this amplifier, which are predictable, control the output amplitude of the oscillator stage. Limiting at this stage does introduce harmonics, however these are reduced by the bandwidth limit of later stages and by the matching network used at the output.

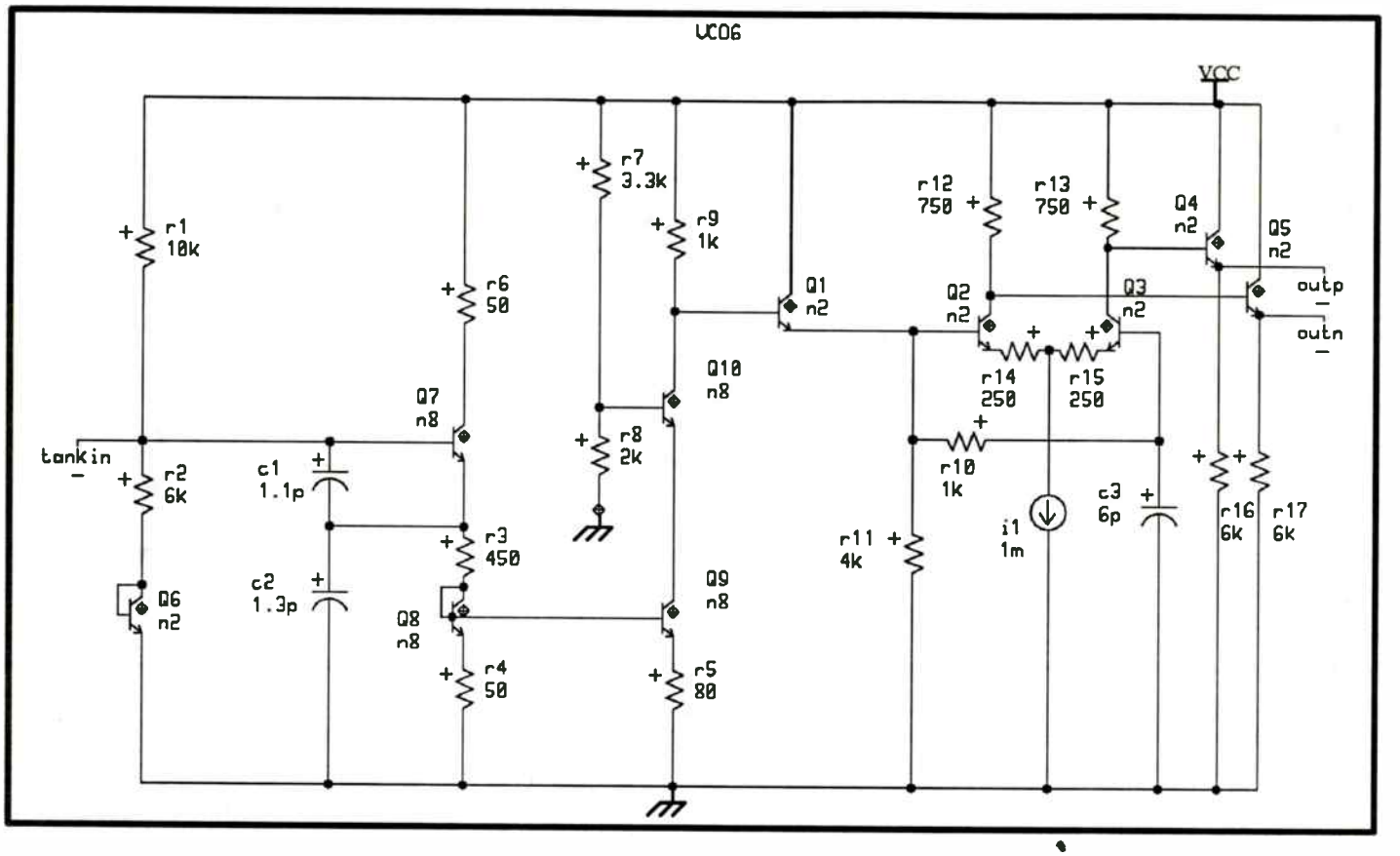

Figure 5. Simplified schematic of the VCO

THE PRESCALER

Although it would be desirable to put the complete prescaler on chip, this was not possible since this design was done on a standard array with limited numbers of devices. It is useful to have some of the prescaler on chip for two reasons. First it is an excellent buffer between the oscillator and the off chip prescaler and second, a 115 MHz signal coming off chip is handled much more easily than a 915 MHz signal.

The prescaler is a traditional ECL sequential divider using three flip–flops. Since the architecture is standard it will not be discussed further here.

PN CODE INPUT

The PN Code input is designed to accept a CMOS input signal. In this particular application the code rate is about 3 megabits per second (MBPS).

THE MIXER

The mixer as shown in Figure 6 is based on the Gilbert mixer design. Normally in a mixer the lower port (Q5 and Q6) is the RF port and the LO input is the upper port (Q2, Q3, Q7, and Q8). The amplifier formed with the lower differential pair is linearized with the addition of the emitter degeneration resistors R4 and R11. By so doing IP3 is increased and harmonics are decreased. Q5 and Q6 are large devices to lower noise on the RF port. However in a mixer which is part of a Spread Spectrum transmitter these rationales may not hold. As shown in Figure 6, the LO from the VCO is placed at the lower port and the PN code is placed at the upper port. This connection scheme is the opposite of that used in most applications. In a Spread Spectrum system the LO is phase modulated by the PN code, in particular the phase shift during a PN code transition is 180 degrees. The quicker this phase shift occurs the better defined is the information. The upper port accomplishes this task. The lower port accepts the high frequency 915 MHz LO. Because the lower port was used for the LO the bandwidth of the mixer remains relatively flat to 1 GHz. Two factors act to increase the bandwidth in the LO path through the mixer. First the transistors in the upper port, which are switching at a relatively slow rate (≈1.5 MHz), act as a cascode for the the transistors at the lower port. Second, by keeping the degeneration resistors (R4 and R11) at the lower port the gain is reduced to about 1.5 which also increases the bandwidth. The goal in this design was to keep the bandwidth flat past the frequency of transmission. As shown in Figure 7, simulation indicates this goal was achieved in the mixer.

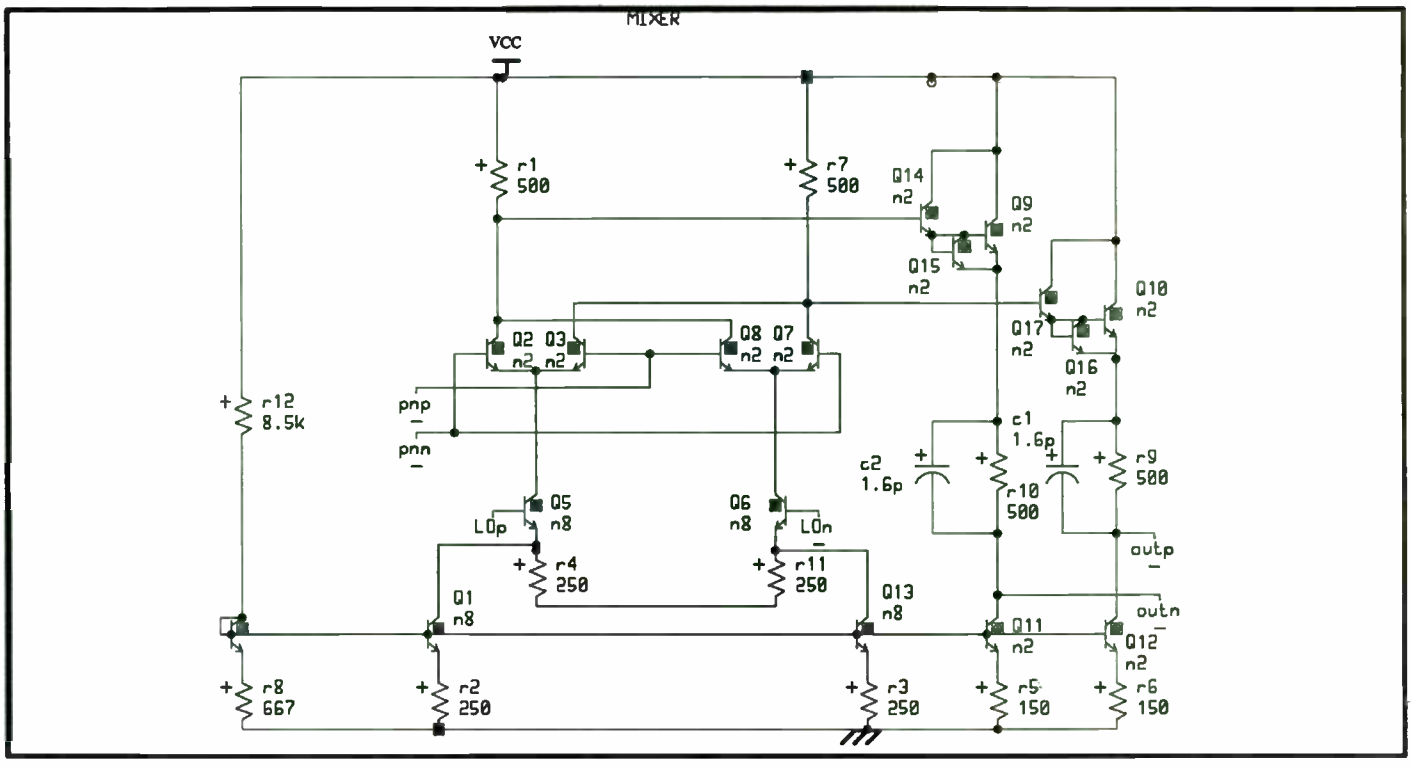

Figure 6. Simplified mixer schematic

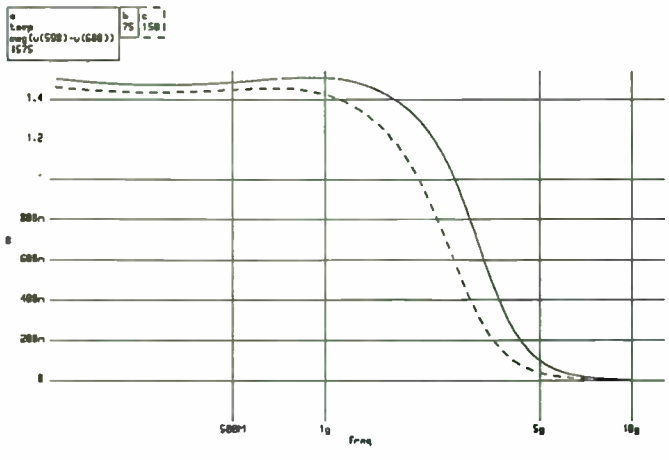

Figure 7. Mixer gain over bandwidth and temperature (simulated)

AGC AMPLIFIER

The peak to peak voltage coming out of the mixer is about 1 volt. The AGC amplifier increases this signal to about 1.8 volts. Since the circuit operates with a 5.2 volt supply and signal levels become relatively large, it is important to assure that for all signal conditions no transistors saturate. The mixer output is level shifted through two diode drops and an additional 1 volt through R9 and R10 before being passed on to the AGC amplifier. This allows the AGC enough headroom to swing a 1.8V signal. Amplification in the AGC stage is provided by the differential pair Q1 and Q2 (see Figure 8). Gain is adjusted by varying the bias current in Q1 and Q2. This is accomplished by circuitry consisting of Q7, Q3, Q4, Q12, Q13 and associated resistors. As the applied AGC voltage at the base of Q7 is reduced from the nominal 5.2 volts, the current supplied to Q1 and Q2 is reduced which decreases the gain. The AGC gain adjustment does not have to be linear for this system but it does requires 20dB of range which is achieved. (Figure 9). The purpose of the AGC is to cut back the transmitted power when the system battery power starts to fall. Since there is no requirement for a linear relationship between the AGC voltage and output power, the system described above is satisfactory.

The circuitry comprised of PLAT1, PLAT2, and Q16–Q20 keep the output common mode voltage level constant over the normal AGC voltage range. This compensation circuitry prevents the Output Amplifier stage from saturating. As the AGC voltage is reduced the common mode voltage level at R10 and R11 rise due to the reduced current supplied to Q1 and Q2. Also as the AGC voltage drops, the compensation circuitry increases the common mode voltage drop across R20 and R21 to keep the AGC amplifier output common mode voltage level constant.

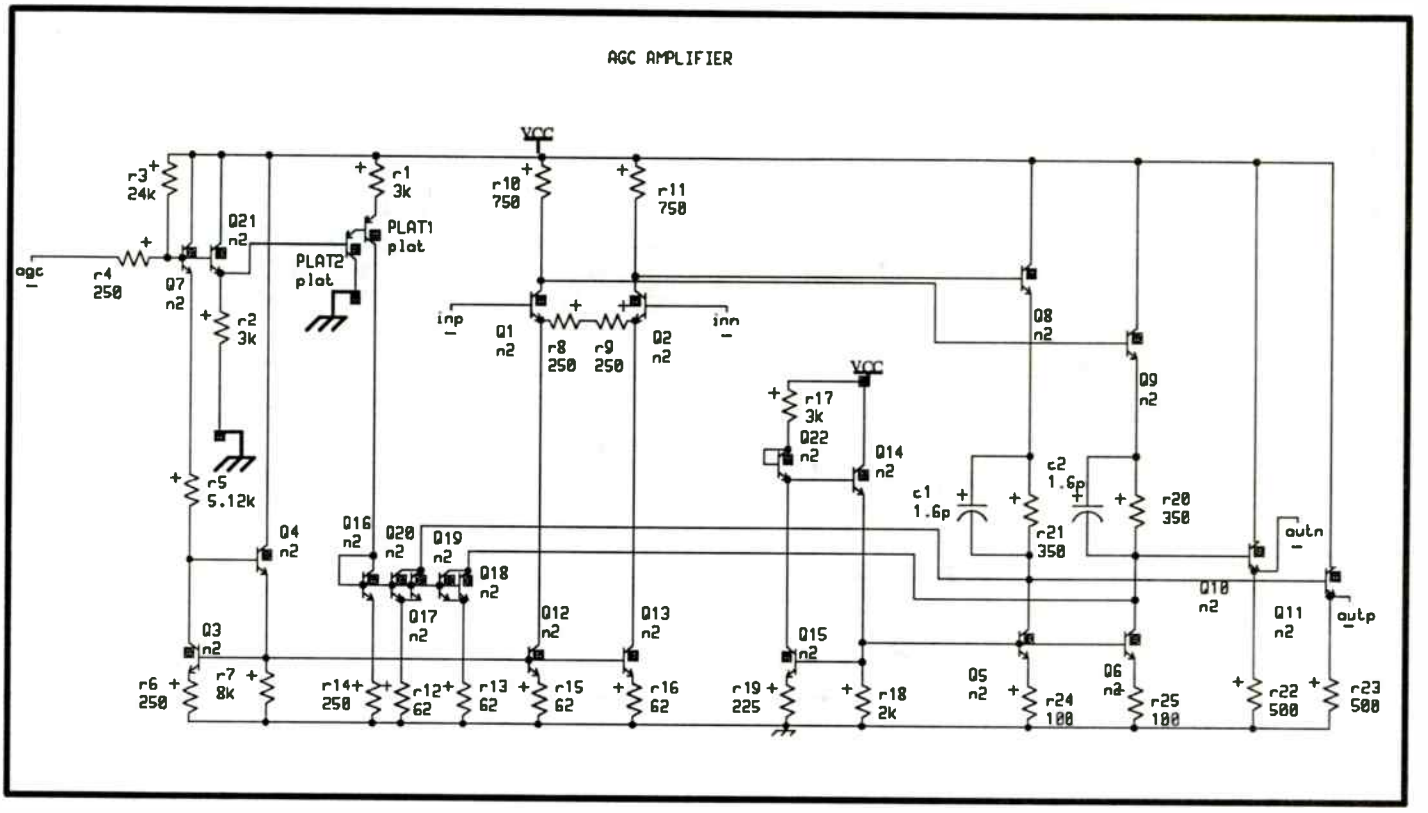

Figure 8. Simplified schematic of AGC amplifier

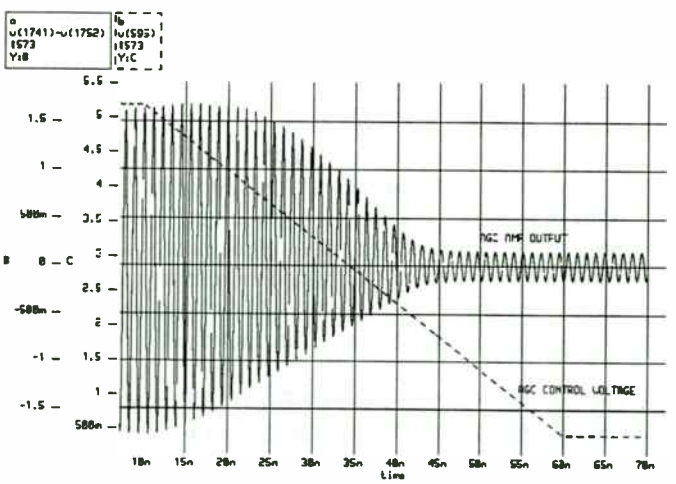

Figure 9. AGC effect on the transmitter output

OUTPUT DRIVER

The output driver initially performs a differential to single ended conversion with the amplifier composed of Q3 and Q18 (in Figure 10). The output of this stage is AC coupled through C11 to two emitter follower stages (Q7, Q12, Q24). These drive into the final common emitter stage consisting of Q21–23 and Q25. The output driver transfers power to a 37 ohm antenna through a matching network.

RESULTS

The initial results on the bipolar ASIC have been measured in isolation from the rest of the system to separate the performance of the ASIC from the total system. As shown in the plot of Figure 11, the measured output power was 18dBm which is 2 dB below our system goal of 20dBm. Since the tests were run in isolation from the rest of the system, the oscillator was not phase locked and thus the frequency is not exactly 915 MHz. Figure 12 shows a narrow band plot of the output signal as viewed on a spectrum analyzer. The resolution bandwidth of the measurement was 1 kHz. Extrapolating from this the phase noise measured 100kHz from the fundamental is 97.2 dB down for a 1 Hz bandwidth. Also specified was the match between the transmitter output power with the PN code in either state (logic 1 or 0). This output power with PN code in logic state 1 and in logic state 0 matched to within 0.5dBm. This result achieved the required level. All results were measured with a Tektronix 2756P spectrum analyzer.

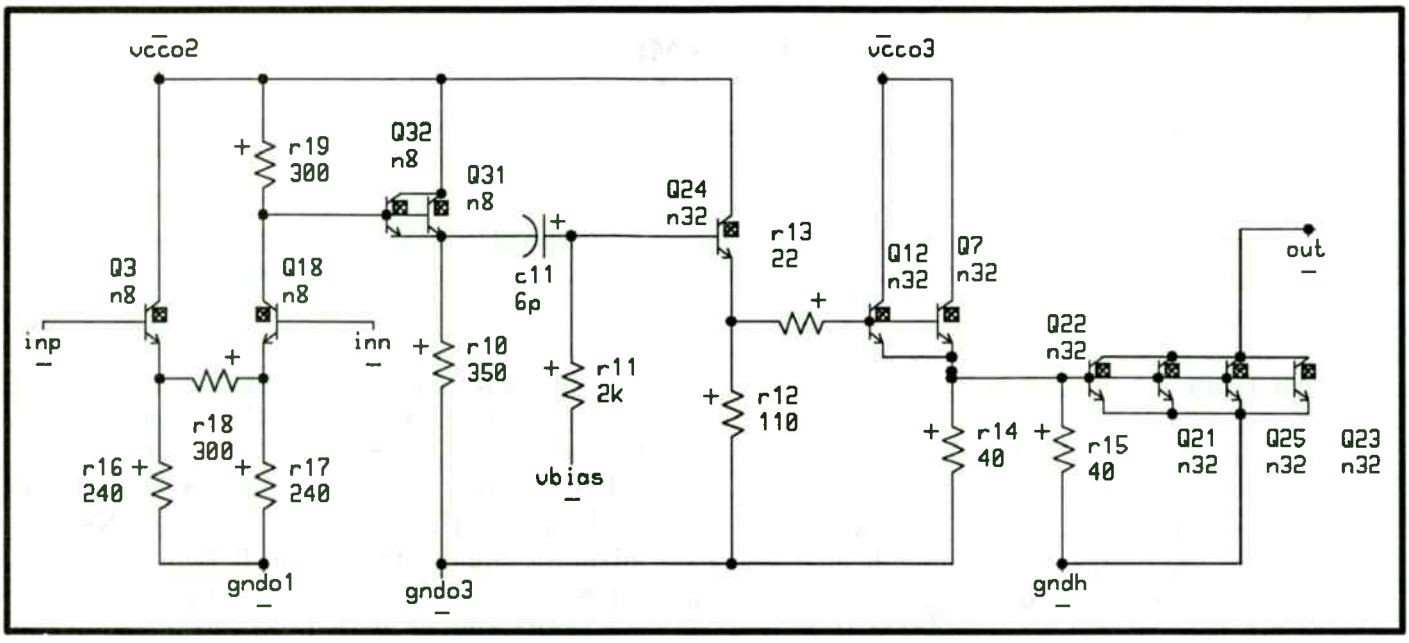

Figure 10. Simplified schematic of output driver

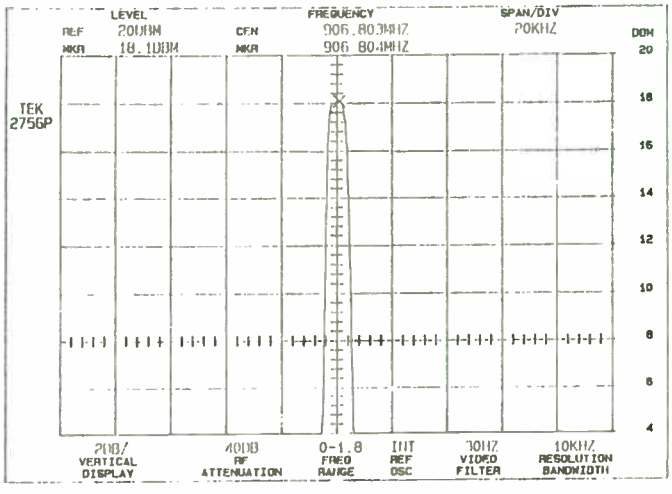

Figure 11. Transmitter output power

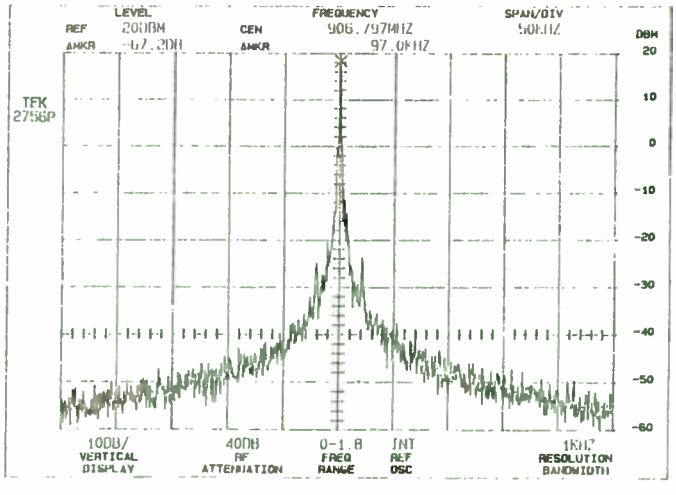

Figure 12. Phase noise at the output of the transmitter.

DISCUSSION

This design has successfully integrated five RF functions on a monolithic integrated circuit design. By so doing we have been able to make possible from a size and cost standpoint a system that would not have been possible with a discrete or multiple IC approach. With the rapidly growing use of the 915 MHz band this type of design will enable the implementation of many systems that would not otherwise be viable.

The RF ASIC met all of the system goals with the exception of transmitter output power. As discussed in the earlier section the measured output power was 2dB below the required 20dBm level. High frequency probing of the part has shown less than expected gain at 915 MHz in interior stages due to less than anticipated bandwidth in these stages. This problem is being addressed in a redesign of the part.

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An E/D Mode S-Band MMIC Frequency Converter

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Abstract - An I-Q frequency down converter using enhancement/depletion (E/D) mode FET has been realized at S-Band. Low conversion loss with low LO power was achieved by using passive DFET mixer. Low DC power consumption on amplifiers was obtained by using EFET and self biasing circuitry. The whole receiver was integrated in a 2x1 mm^2 MMIC chip biased at a single 5V power supply.

Introduction

I-Q frequency converters have been used in many commercial wireless communication applications such as spread spectrum, cellular radio, and data communications.[1,2] As more and more components are integrated into a MMIC chip, power consumption becomes one of the prime concerns. Enhancement mode MMIC technology which has demonstrated for low power consumption capabilities,[3,4] appears to be a solution to minimize the power consumption.

This paper describes an I-Q frequency down converter circuit utilizing enhancement/depletion (E/D) mode MESFET MMIC technology for 2.4 GHz wireless Local Area Network (LAN) applications. The converter includes a LNA, two mixers, a quadrature hybrid, two band stop filters, and LO drivers. It consumes about 17 mA of DC current, with 10 mA as a goal in the near future. The chip is processed at Raytheon's MMC foundry using newly developed commercial E/D process. Design topology and test results are presented.

Circuit Design

The frequency converter circuit is a generic image reject down converter circuit. It down converts the S-band (2.4 GHz) signal to DC-100 MHz. Figure 1 shows block diagram of the circuit. It includes a two stage low noise amplifier (LNA), a passive 90° hybrid splitter, two single stage LO drivers (LOD), two passive FET

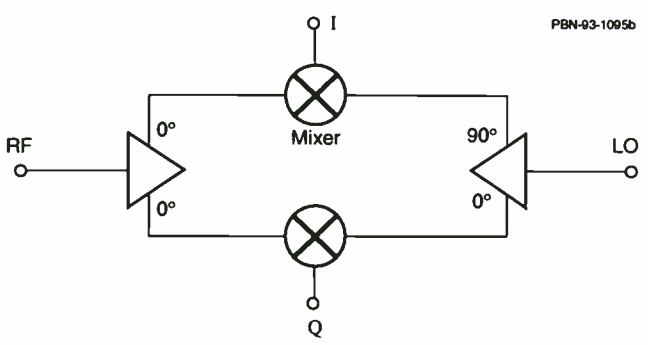

Figure 1. Block diagram of an Image Reject mixer.

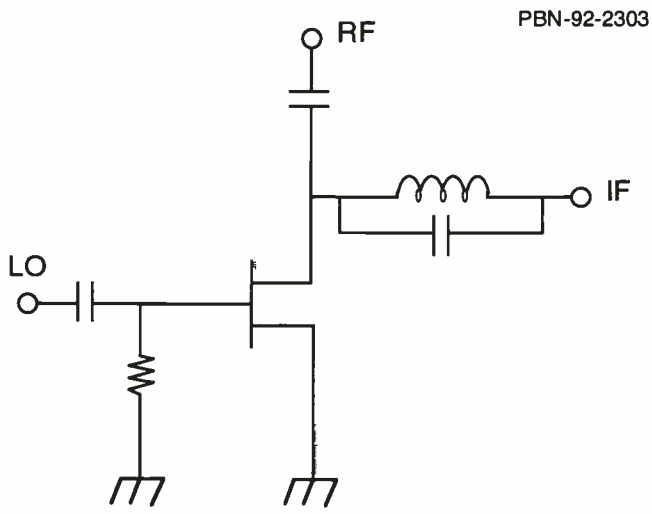

Figure 2. Circuit of the passive FET mixer.

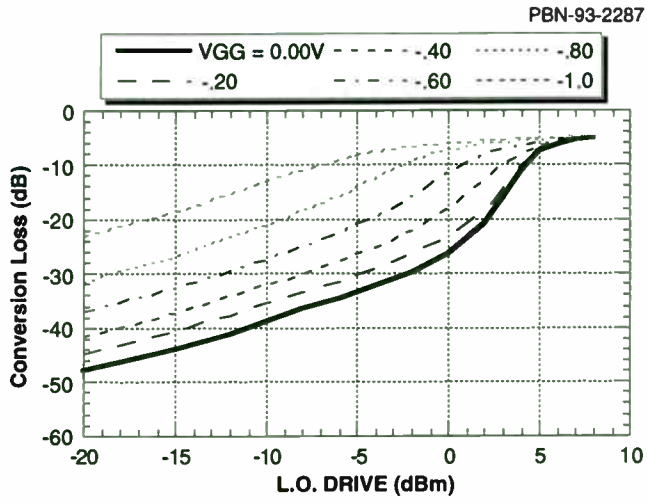

Figure 3. Conversion loss vs. LO drive at different gate bias for a typical 400 μm MESFET.

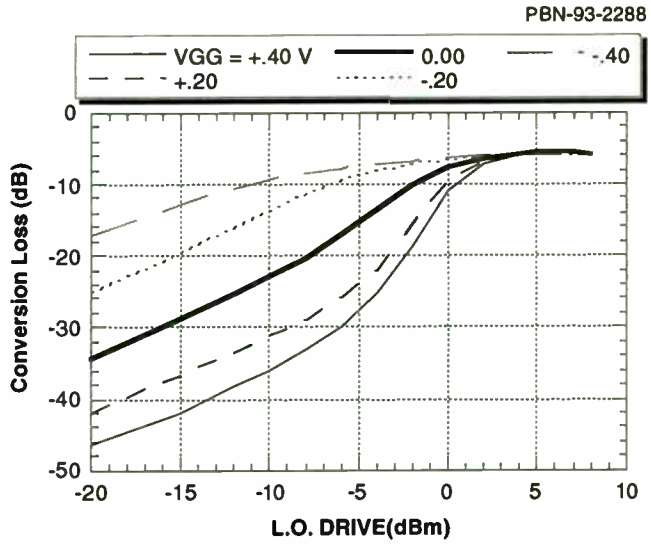

Figure 4. IF output power vs. LO drive at different gate bias for a typical 500 μm DFET.

mixers, and two RF band stop filters.

The mixers are passive DFET mixers. Figure 2 shows a circuit of the mixer. The RF and IF signals share the drain of the device and are separated by a band-stop filter. The LO power feeds the gate of the device. Due to the lower pinch-off voltage, (~-0.7 V), compared to the typical MESFET devices, (~-1.5 V), it allows the conversion at a lower LO power. At 0 dBm of available LO power, the conversion loss is about 8 dB for the mixer alone. Figures 3 and 4 show conversion loss versus LO power at different gate biasing for a MESFET and a DFET, respectively. It can be seen that at 0 dBm LO drive, the conversion loss is about -26 dB for a typical 400 μm MESFET mixer and about -8 dB for a typical DFET mixer, when V_{GG} = 0 V.

The LNA includes two stages. The two second stage amplifiers also serve as a splitter to improve the isolation between two RF signals. It was designed for 20 dB gain and 3 dB noise figure. Figure 5 shows circuit of the LNA.

The LO drivers, in addition to amplifying the LO signal, also provide isolation between the mixer LO input ports and impedance matching between the quadrature hybrid and the mixers. The quadrature hybrid is a four (4) element LC circuit. It provides sufficient amplitude balance and phase quadrature over the LO frequency bandwidth (200 MHz at 2.4 GHz) for image rejection requirement. Figure 6 shows circuit schematic of the quadrature and two LO drivers. EFET's were used in both LNA and LOD to minimize the power consumption.

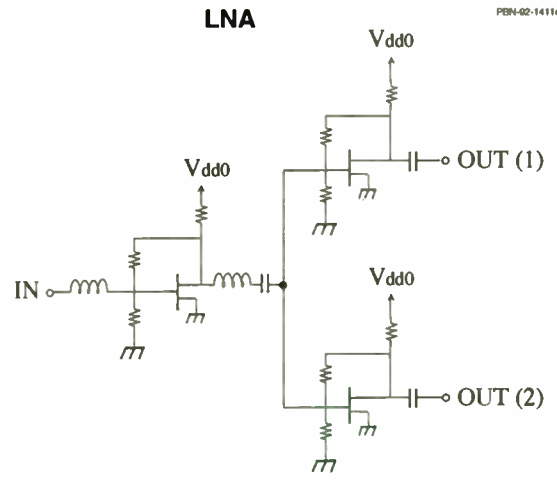

Figure 5. LNA circuit.

Circuit Fabrication

Circuits were fabricated using Raytheon's 0.5 μm gate E/D technology. The EFET and DFET channel implants are formed by selective ion implantation of Si and Be. The source and drain ohmic contacts are formed on N^+ regions of the FET, which has a sheet resistance of

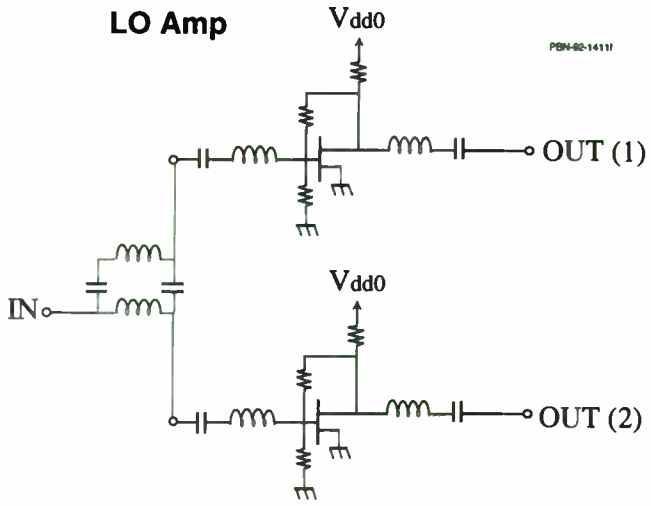

Figure 6. LOA circuit.

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	EFET	DFET
IDS - (mA/mm) (V_{ds} = 2.0 V, V_{gs} = 0.5 V)	60	250
Transconductance - mS/mm (V_{ds} = 2.0 V, V_{gs} = 0.5 V)	250	225
V_p - (V)	0.1	-0.7
BV_{dg} - (V)	> 7	> 7

Table 1. FET characteristics of E/D Devices.

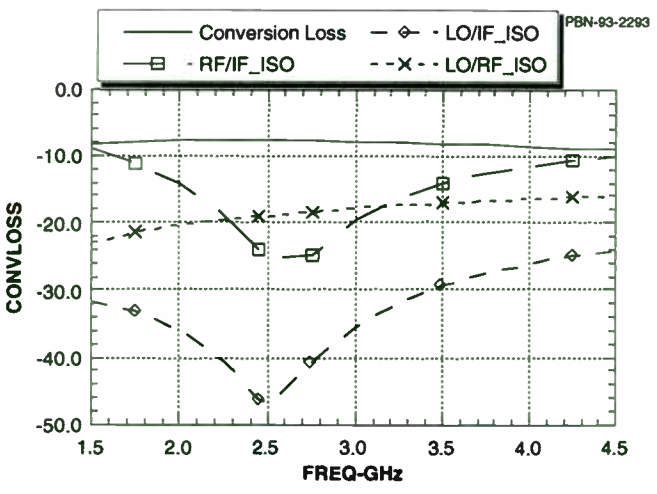

Figure 7. Simulated conversion loss, R/I, L/I and L/R isolation of a single–ended mixer.

200 Ω/square. The gate material is Ti/Pt/Au. The FET characteristics are given in Table 1. The process also features GaAs implanted resistors with a sheet resistance of 850 Ω/square, low temperature coefficient (<200 ppm/C) 6 Ω/square TaN resistors, 300 pF/mm^2 MIM capacitors with 2000 Å SiN dielectric, air bridges, and low loss inductors and transmission lines using Ti/Au with a sheet resistance of 10 mΩ/square.

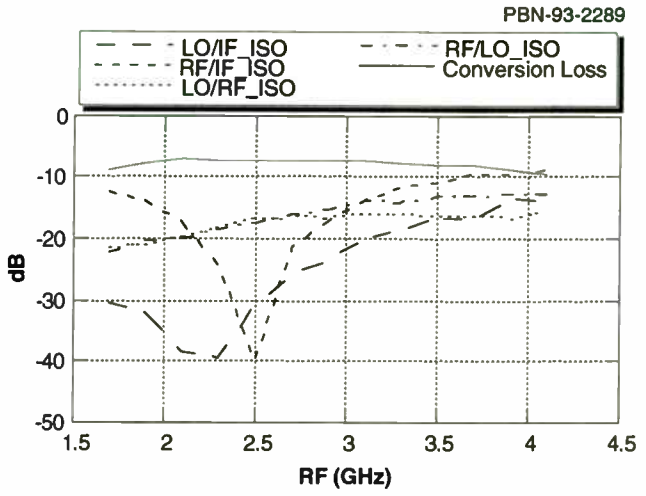

Figure 8. Measured conversion loss, R/I, L/I, L/R and R/L isolation of a single–ended mixer.

Test Results

Wafers of the E/D devices were thinned down to 15 mil. Both the complete receiver chips and component test patterns were evaluated using both on-wafer probing and discrete chip test in test jigs. Figures 7 and 8 show simulated and measured conversion loss, isolation between LO to RF, LO to IF and RF to IF, of the mixer alone versus the RF frequency.

A photo of the down converter circuit is shown in Figure 9. Test results are listed in Table 2. It shows that the conversion gain of the receiver is larger than the required 15 dB voltage gain to a 1 kΩ load. The I and Q amplitude difference was 0.4 dB and the phase difference was 84°. With an ideal 90° combiner, this corresponds to better than 25 dB of image rejection. The isolation from LO to RF port is better than 50 dB. Noise figure and conversion gain to a 50 Ω load are given in Figure 10, which shows the noise figure is about 4.5 dB in the frequency range, 2.4 +/- .1 GHz.

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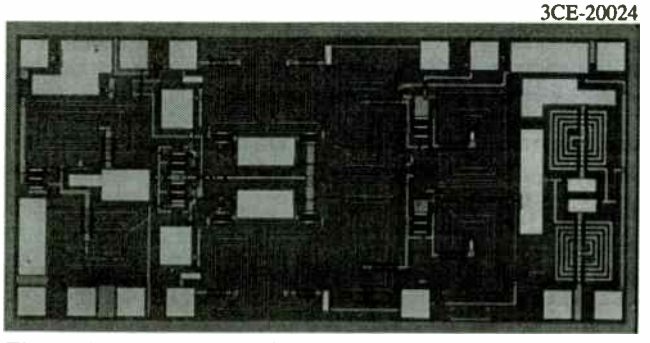

Figure 9. Photo of an S–band down converter.

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RF Frequency	2.35 GHz
LO Frequency	2.45 GHz
RF Power	-20 dBm
LO.Power	0 dBm
Bias Voltage	5 V
DC Current	17.1 mA
Conversion Voltage Gain to 1 KΩ Load	>15 dB
RF to IF Isolation	-27.4 dB
Lo to RF Isolation	-51.8 dB
I/Q Phase Deviation	84°
I/Q amplitude Deviation	0.5 dB
IP3 Relative to Output	+5 dBm

Table 2. Summary of RF test results.

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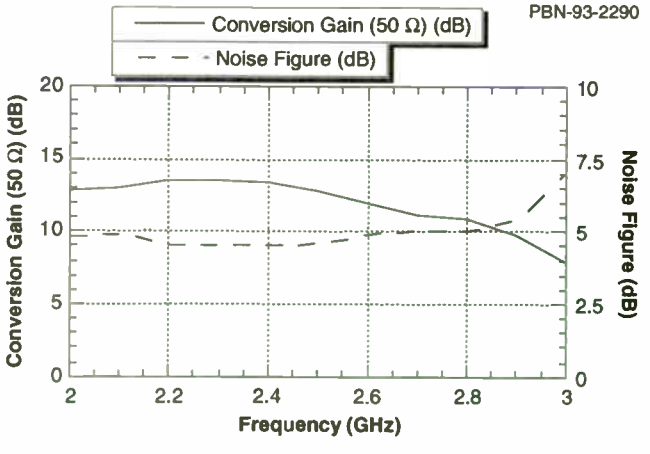

Figure 10. Conversion gain and noise figure of the I–Q down converter.

Summary

This paper describes a 2.4 GHz MMIC I-Q frequency converter using E/D MMIC technology. The design topology and test results have been described. This chip has been integrated into a transceiver chip which is currently in the initial phase of mass production.

Acknowledgment

The authors would like to thank W. Struble and S. Nash for device characterization, B. Engel for chip assembly, and H. Renaud for circuit layout. They would also like to thank the management support from Raytheon's Research Division and Advanced Device Center in Andover.

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RFIC Components for Cordless Phones

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Introduction

The commercial market for RF Integrated Circuits (RFICs) is expanding rapidly. Many commercial applications are appearing which need small, efficient components which provide higher levels of integration. Some examples include Point-of-Sale (POS) Terminals, cordless and cellular telephones, wireless meter reading equipment, wireless security systems, and many others. This increased integration level provides very low component counts on the PC board, and reduces the burden placed on the system manufacturer, ultimately allowing much lower system cost. This progression is analogous to that seen with digital circuits and microprocessors, whereby increasing levels of technology was placed upon the IC, and taken off the circuit board.

One application which requires high-volume, low-cost RFICs is the digital cordless telephone. Several 900 MHz phones have appeared on the market recently, requiring a low-cost RF section. Some of these RF sections are all discrete, others use a number of individual ICs, while still others use highly integrated ICs. Also, some of the entries utilize channel frequency hopping, others use direct-sequence spread-spectrum (DS-SS), and others use a combination of DS-SS and frequency hopping. A highly integrated RF chipset for a 915 MHz

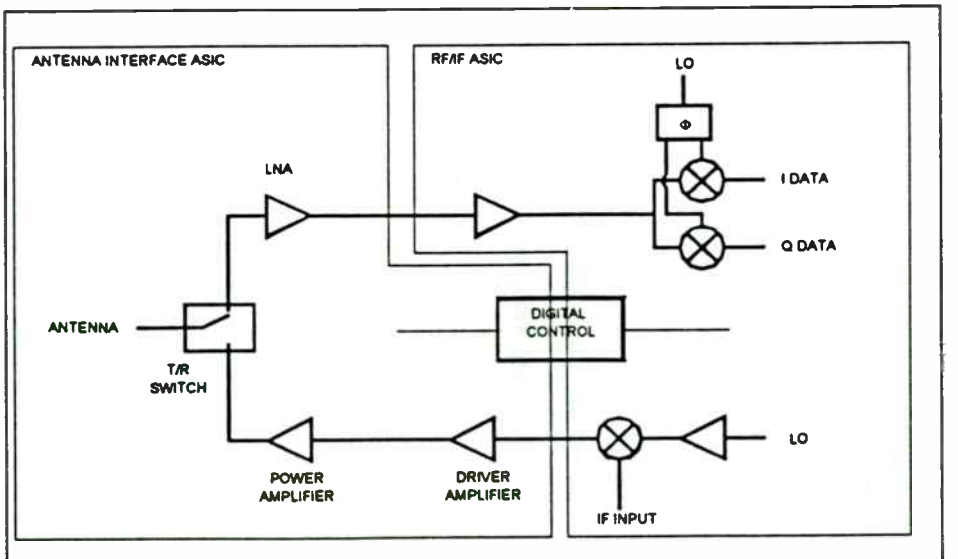

Figure 1.
RF Section for Cordless Phone.

spread-spectrum cordless phone has been developed and will be described.

RF Chipset Requirements

The RF section such as that shown in Fig. 1 performs the following functions:

- Modulates the baseband spread-spectrum encoded data signals directly onto an RF carrier at 915 MHz,
- Amplifies the modulated signal with a power amplifier to 100 mW for transmission,
- Provides for switching between transmit and receive paths, using a T/R switch with digital control,
- Receives the incoming signal and amplifies with a low-noise amplifier,
- Demodulates the signal directly to baseband In-phase and Quadrature-phase components.

The chipset consists of two chips: an Antenna Interface ASIC and a RF/IF ASIC, as shown in Fig. 2 and 3. RF Micro Devices, Inc. utilized **Optimum Technology Matching™**, choosing high-performance GaAs MESFET technology for the Antenna Interface ASIC, and low-cost Silicon bipolar technology for the RF/IF ASIC. This partitioning of technologies allows the optimum price/performance trade-off.

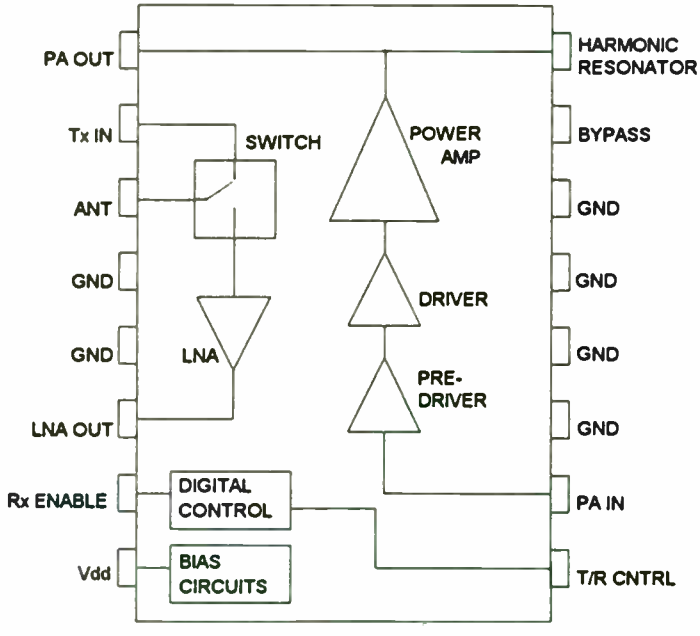

Figure 2.
Antenna Interface ASIC.

Antenna Interface ASIC

The Antenna Interface ASIC is a GaAs MESFET circuit, including a T/R switch, high-gain power amplifier, and a low-noise amplifier. The chip, supplied in a plastic SOIC-16 package, operates from a single 5V power supply. The overall specifications for the circuit require gain of 23 dB in transmit mode with 100 mW transmitted power, and 23 dB gain with less than 3 dB noise figure in receive mode. The T/R switch is controlled by digital translators, so a standard CMOS or TTL level input can be applied to control transmit or receive. Power down features are incorporated on all circuits and are tied to the T/R control.

The power amplifier is a self-biased, 3-stage GaAs MESFET design, with a total gate width on the final stage of 1.2mm. The final stage is biased slightly Class-AB, and consists of depletion-mode FETs with pinch-off voltage of ~-0.9V. Total current consumption in transmit mode is ~60 mA. Enhancement-mode FETs are used for part of the driver amplifiers as well as in the power down circuitry. The EFETs allow the amplifier to be shut off completely when not in use, using only the positive voltages available from the translators. The entire amplifier operates from a

single 5V supply, with no need for an external negative voltage.

The LNA is a 12 dB gain block with ~2 dB noise figure. The input and output are matched to 50Ω; the output interfaces directly to the RF IN port on the RF/IF ASIC.

RF/IF ASIC

The RF/IF ASIC is a Silicon bipolar circuit, and includes a bi-phase modulator for transmit, and a quadrature demodulator for receive. The LO input power is -10 dBm, which is amplified by the LO buffers to 0 dBm, and is distributed to both the up- and down-converter. Direct bi-phase modulation and direct quadrature demodulation is used, so a single external synthesizer is all that is required for the transceiver function. The 90° phase shifter for the quadrature demodulator is included on-chip to simplify the interface requirements.

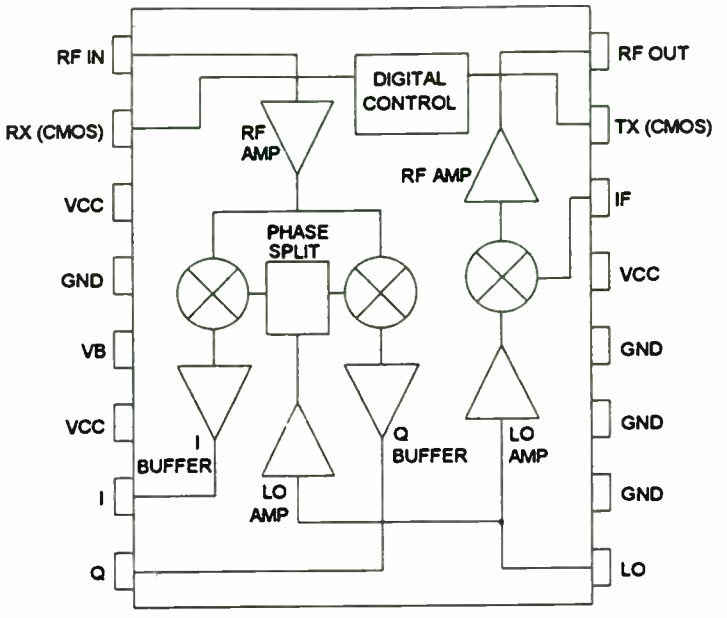

Figure 3.
RF/IF ASIC.

The bi-phase modulator accepts inputs from 0 to >3 MHz with up to $0.5V_{p\text{-}p}$. Carrier suppression is >25 dBc for the maximum input level. Maximum output from the chip is -10 to -15 dBm. This provides an easily achievable level from the bipolar process, placing the majority of the gain and power output onto the GaAs circuit, where gain/stage and power are much higher.

The quadrature demodulator operates directly at 915 MHz. Input signals can range from 900-930 MHz, and the I/Q output bandwidth is 0 to 3 MHz minimum. Amplitude and phase balance specs are <1 dB and ±5°, respectively. I/Q output level can be as high as $1.4V_{p\text{-}p}$ at 1dB gain compression.

This chip also operates from a single 5V power supply and is supplied in an SOIC-16 package.

Summary

A highly integrated 2 chip set has been designed for cordless phones operating in the 915 MHz ISM-band using direct-sequence spread-spectrum modulation. This chipset allows the phone to be produced with much lower manufacturing costs and greater reliability than do the discrete components.

Acknowledgments

The authors wish to thank Powell Seymour for layout and operations support and Jill Howard for test support.

A 100 mW UHF Spread-Spectrum Transmitter IC

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ABSTRACT

A low-cost direct quadrature modulator IC capable of greater than 100 mW output power from a single 5V power supply has been developed for digital wireless communication applications in the 800 to 1000 MHz frequency range. The RF2423 integrates a fully-monolithic high-accuracy direct quadrature modulator with a variable-gain power amplifier on a compact GaAs chip. A standard SO-16 plastic packaging approach is used. Our overall design approach emphasizes low cost, high performance, single-supply operation, ease of use, and compact circuit board layout with no critical-value external circuitry.

INTRODUCTION

A myriad of new digital wireless communication systems are being designed today, including next-generation cordless telephones, wireless utility meter-reading equipment, and point-of-sale data links, which take advantage of recent FCC rules changes allowing unlicensed use of 902-928 MHz and other "ISM" bands at up to 1 watt transmitter output. However, many applications can achieve required link distance and interference rejection with 100 mW output power, reducing battery requirements and lowering system cost.

Quadrature modulation techniques provide an adaptable means of amplitude, phase, and frequency modulation for new digital wireless communication systems.[1,2] Advances in fabrication technology make possible low-cost highly-integrated RFIC solutions to cost and size minimization necessary for commercial and consumer applications.[3] Direct modulation transmitter topologies minimize transmitter size and cost by eliminating up-conversion after modulation. A low-power UHF oscillator and this new IC are the only RF components required for an extremely compact 100 mW spread-spectrum transmitter.

CIRCUIT DESCRIPTION

Our design approach emphasizes low cost, high performance, single-supply operation, ease of use, minimum external parts count, and compact circuit board layout with no critical-value external circuitry. A compact chip layout, use of a mature high-yield enhancement/depletion-mode GaAs MESFET fabrication process, and plastic SOIC packaging contribute to minimum production cost for commercial and consumer application. Principal design challenges included achieving 100 mW output and standby mode with single-supply operation, and sufficient isolation between modulator and power amplifier without increasing packaging cost.

A circuit block diagram is shown in Figure 1. The design methodology utilizes schematic circuit entry, linear and non-linear simulation using both foundry-supplied and proprietary device models, and manual layout with foundry-specific design rules checking (DRC). Proprietary software links schematic entry and simulation, and checks layout versus schematic (LVS) to ensure functioning circuits after one pass through fabrication.

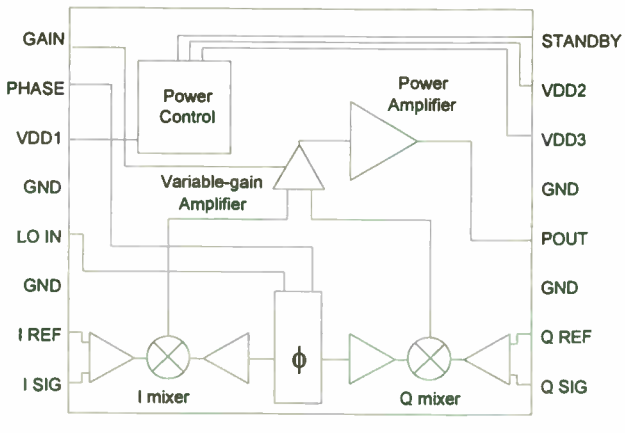

Figure 1. RF2423 100 mW UHF direct-modulation spread-spectrum transmitter IC block diagram.

A pair of doubly-balanced active mixers forms the core of the quadrature modulator function. The single-ended carrier input is divided and passed through an on-chip phase-splitting network. Resulting signals are amplitude-limited to drive the mixer switching circuits in quadrature. Relative phase in the two paths may be trimmed by an external voltage around 1.4 volts, or left unconnected as a default condition.

The carrier input is not internally matched to 50 ohms to retain flexibility in the interface between source oscillator and this IC.

I and Q modulation inputs are differential, although single-ended inputs are accommodated as well. Mixer outputs are summed and are passed through two variable-gain amplifier stages for output level control. Output impedance-matching circuitry and power supply feed are integrated with the fixed-gain output stage to minimize the number of external components required.

An enhancement-mode FET is utilized in the output amplifier to simplify class AB bias and to make possible switching the output amplifier into a low-current standby state. Positive gate bias voltage is generated by the current mirror circuit shown in Figure 2. This approach eliminates the need to internally or externally generate a negative gate bias voltage and reduces the effect of FET threshold variation on bias current. CMOS logic levels control the standby switch, which turns off the output FET through the current mirror. On-chip EFET switches in series with the power supply leads control current to the remainder of the circuit.

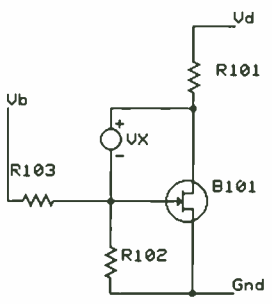

Figure 2. Positive gate bias voltage for the enhancement-mode output FET is determined by a current mirror.

The variable gain function is based on differential-pair amplifier stages with sources coupled through MESFET variable resistors. An approximation to a logarithmic control characteristic is obtained by using two different FET sizes in parallel for the variable resistance in each of the two amplifier stages and by scaling and offsetting the gate voltages to the four variable-resistance FETs.

MEASURED PERFORMANCE

Data presented in this section represents initial measurements of plastic packaged ICs from the first fabrication run, such as shown in the Figure 3 photograph. Modulation inputs were driven unbalanced (single-ended). Amplifier frequency response, gain control range, and maximum output power closely match design simulations. However, the data indicates low amplifier gain, partially the result of a bias point modeling error in the output amplifier. Higher than predicted modulation amplitude was required to produce 100 mW output, leading to slightly higher than expected distortion in the modulator.

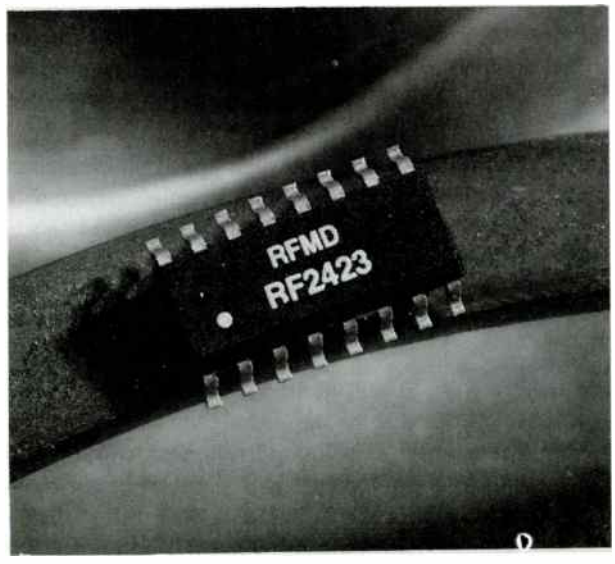

Figure 3. Photograph of packaged transmitter IC.

Even so, excellent phase modulation performance was obtained this first pass through fabrication. Minor changes to the circuit to increase gain have been identified, which should increase modulator accuracy by lowering modulation amplitude requirements.

Figure 4 is a plot of the measured output power vs. gain control voltage between 800 and 1000 MHz. Reference line (3 divisions from bottom of plot) is 0 dBm. Vertical scale is 5 dB per division. Carrier input level is 0 dBm. At 900 MHz the output level is varied between 21 dBm and -6 dBm with a control voltage between 0 and +5 V for this unit. The mean level control range at 900 MHz was measured to be 25.5 dB.

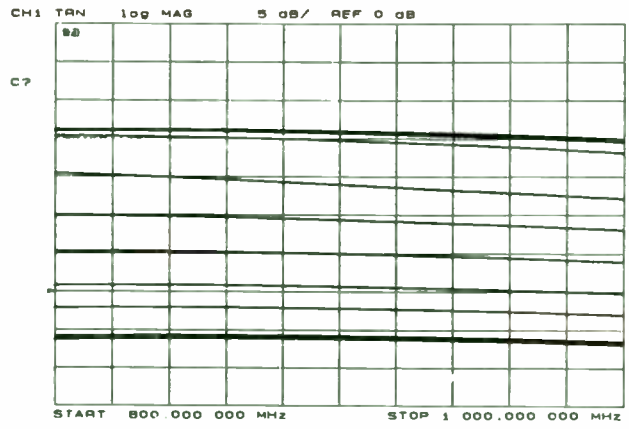

Figure 4. Measured output power vs. gain control voltage over the 800 to 1000 MHz frequency range. Reference line (3 divisions from bottom) is 0 dBm. Vertical scale is 5 dB per division.

Figure 5 shows the measured 900 MHz vector output for sine modulation inputs at 20 dBm output power, showing minimal deviation from theoretical circular output.

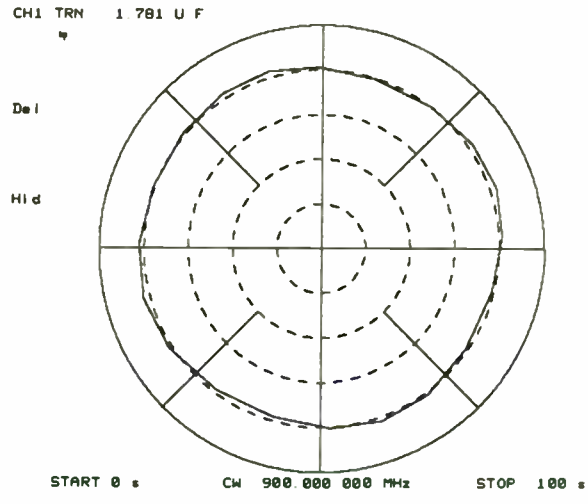

Figure 5. Measured 100 mW vector output with sine I and Q modulation.

Table 1 summarizes the mean modulator error terms at 800, 900, and 1000 MHz obtained from SSB spectrum measurements. Modulation amplitude, DC offsets, and phase are adjusted to null carrier and image. Carrier phase quadrature is centered at approximately 900 MHz, and is +2.5, -2.4 degrees between 800 and 1000 MHz. Q modulation channel gain is approximately 1 percent lower than the I channel in these measurements. I and Q channel DC offsets are between 32 and 112 mV.

Freq. MHz	I_{offset} mV	Q_{offset} mV	Phase Error	Q Mag. Error
800	78	61	+2.5 °	-1.1 %
900	100	44	+0.1 °	-0.9 %
1000	112	32	-2.4 °	-1.4 %

Table 1. Mean modulator errors in initial SSB measurements.

Another indication of modulator accuracy is the level of SSB carrier and image suppression with no modulation input or phase adjustments, summarized at 800, 900, and 1000 MHz in Table 2. Mean unadjusted carrier suppression is 29 to 30 dB. Mean unadjusted image suppression is 34 to 40 dB.

Freq. MHz	SSB Carrier Suppression, dB	SSB Image Suppression, dB
800	30	34
900	29	40
1000	29	34

Table 2. Unadjusted mean SSB carrier and image suppression in initial measurements.

The carrier input port is not internally matched to 50 ohms to retain flexibility in the interface between source oscillator and this IC. Typical carrier input port impedance is 150 -j150 ohms at 900 MHz, measured at the SO-16 package lead. This impedance is easily transformed to 50 ohms with parasitic circuit board shunt capacitance and a series inductor. Figure 6 shows the measured carrier input port impedance between 800 and 1000 MHz, using an external 22 nH series inductor for impedance matching.

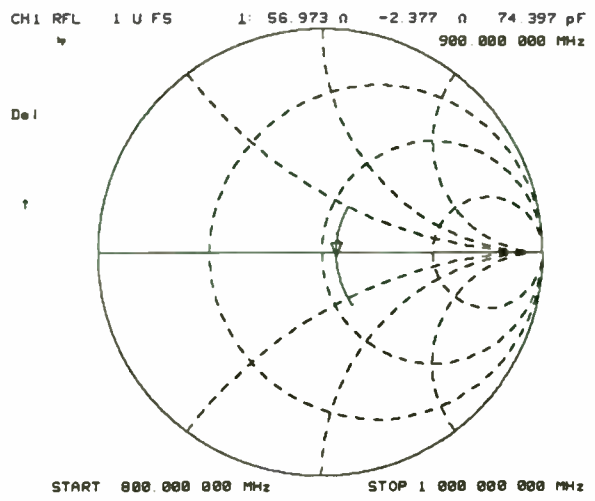

Figure 6. Measured carrier input port impedance using a 22 nH external series chip inductor to match impedance to 50 ohms.

Measured output power vs. carrier input level at 800, 900, and 1000 MHz is plotted in Figure 7, showing the carrier input limiting characteristic. Nominal carrier input level requirement is 0 dBm for resistive input termination (as plotted). An inductive input match approach (as in Figure 6) reduces input power requirement to -5 dBm.

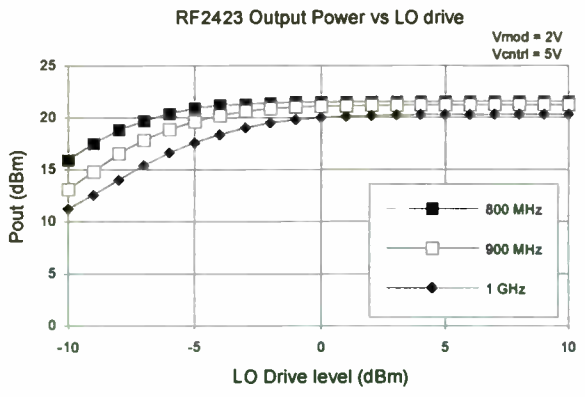

Figure 7. Measured output power vs. carrier input level at 800, 900, and 1000 MHz. External resistive carrier input termination is used. Inductive input matching circuit reduces input power requirement by 5 dB.

Mean idle DC current drain was 67 mA from the single 5V supply. Mean DC current drain at 100 mW output power at 900 MHz was 127 mA. Mean standby-mode current drain was 7 mA.

CONCLUSION

A low-cost 100 mW UHF direct quadrature modulator IC has been developed for digital wireless communication transmitters in the 800 to 1000 MHz frequency range. Completely monolithic carrier phase splitter, carrier limiting amplifiers, a pair of active doubly-balanced mixers, variable-gain amplifier, and power amplifier are integrated on a compact GaAs MESFET IC. The plastic SO-16 packaging approach is chosen for high-volume commercial and consumer applications. This IC and a low-power UHF oscillator are the only RF components required for an extremely compact 100 mW spread-spectrum transmitter.

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Testing for Improved Wireless Design

Session Chairperson: Ben Zarlingo,
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Improving Wireless Design and System Integration with Real-World Testing

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Abstract: Designing tomorrow's wireless systems is a complex task undertaken in an environment of fierce competition. System integration is a special challenge in new applications where the connections between component performance, modulation technique, signal path variations and overall system performance are not well understood.

This paper demonstrates how the use of real-world test signals and advanced signal analysis can improve component or system testing and speed system integration. Examples are provided at baseband, IF and RF through the use of vector signal analysis and flexible multi-format digital demodulation.

Testing is a vital part of any communications system design and systems using digital modulation techniques are no exception. However the most widely used tools, tests and analysis techniques do a much better job with the traditional analog part of the test problem than with the new digital functions. The difference between the old and the new can be expressed in several different ways--The presence of burst or pulsed signals, the use of I-Q modulation, the need to measure phase. In many systems all of these differences apply.

Traditional *precision* tools such as spectrum analyzers, power meters and counters are not sensitive to signal phase and most are not designed for time-varying signals. Thus it may be difficult to measure the signal content, total power or even the exact frequency of burst and/or complex modulated signals. Digital oscilloscopes can capture signals completely but even with extensive signal processing they do not have the measurement precision and resolution to fill the gap. Nonetheless it is vital for designers to know what effect each component has on overall modulation quality and system performance.

System Integration

In the system integration phase of design it is important to be able to track signal integrity *throughout the block diagram* since this is the best way to identify malfunctioning blocks or to track down problems at the interface between blocks. Unfortunately this can be very difficult due to the changes the signals undergo as they pass through the system. They are filtered, their frequency is changed, and they are often split into components such as I and Q. In many systems they are also multiplexed in frequency and/or time.

The ability to track a signal through the block diagram has other benefits for the design engineer. There is no need for the entire system to be up and running before individual blocks can be realistically tested. This avoids the sometimes-primitive design technique of dismantling the system, making a change, putting the system back together again to evaluate the change, etc.

Design Optimization

In the design optimization phase the system is working and the goal is to optimize one or (inevitably) more factors. System design is often managed from an error budget point-of-view and here, better testing can bring a variety of benefits:

- Designs are completed sooner--Powerful, definitive tests allow designers to meet the error budget faster. Shorter time-to-market is always better
- Design costs are lower--A shorter design process is inherently less expensive, and
- Product costs are lower--Unambiguous, detailed testing shows engineers where they must spend for better performance and where they can economize.
- System performance is improved--Better testing means a more optimal design and the best possible performance from a given system, whether

performance is measured as error rate, spectral efficiency, battery life, etc.

- Manufacturability is enhanced--Clearer insight into the factors that affect each performance parameter reduce expected yields and speed system checkout and adjustment.
- Frequency utilization is more efficient--Optimally designed systems make the most of valuable RF spectrum. Smaller system errors improve noise margin and may allow for more spectrum-efficient (and demanding) modulation types to be used.

Real-World Testing

The most efficient and productive testing is that which relates directly to the functionality and performance of a system. Traditional measures such as harmonic and intermodulation distortion, spurious and phase noise were appropriate for CW methods of transmitting analog data but fall short in representing the true performance of modern digital systems. End-to-end testing such as BERT (Bit Error Rate) is both realistic and useful, yet offers only limited insight since it reveals the *existence* of problems but not their location.

What follows are examples of real-world tests that take advantage of advanced displays and signal processing to more clearly identify the performance of individual blocks in operating digital communications systems. Measurements and displays shown are from HP 89410A/89440A Vector Signal Analyzers.

Example: Adjacent-Channel Power

An essential consideration in almost every radio application is the potential for interference between transmitters. This interference is generally the result of amplifier distortion in the transmitter, and that is where testing and optimization efforts are directed. Though spurious and harmonic distortion products can produce interference at widely different frequencies, the most common problem is adjacent channel interference. In analog radios intermodulation distortion (IMD) is usually suspected as the cause of this interference since 3rd and 5th order IMD will produce distortion products very close to the carrier frequency.

It is logical to extend this reasoning to the design of amplifiers for systems transmitting digital data as well. The implication would be to test such amplifiers using closely-spaced CW signals as a stimulus and IMD as the primary measure of quality. Designers would then modify amplifier design and operating parameters to minimize IMD, *assuming that minimum IMD would result in minimum adjacent channel interference.*

The assumptions inherent in this measurement and design approach may not be valid, however. A much more realistic test alternative is to use a digitally modulated signal as the stimulus and to measure the actual adjacent channel power (ACP) that results from it. Though this approach requires more advanced measurement techniques it is much more likely to predict the actual performance of an operational system and should result in more optimal design trade-offs.

Both the stimulus and analysis capability can be provided by a vector signal analyzer with an RF arbitrary waveform source. The source supplies a signal similar to the one to be used in actual system operation. The resulting amplifier output is then directly analyzed for adjacent channel power using an integrated band power measurement feature.

First the power in the occupied channel is integrated over the actual channel bandwidth and used as a relative power reference. Such a measurement is shown in figure 1 below.

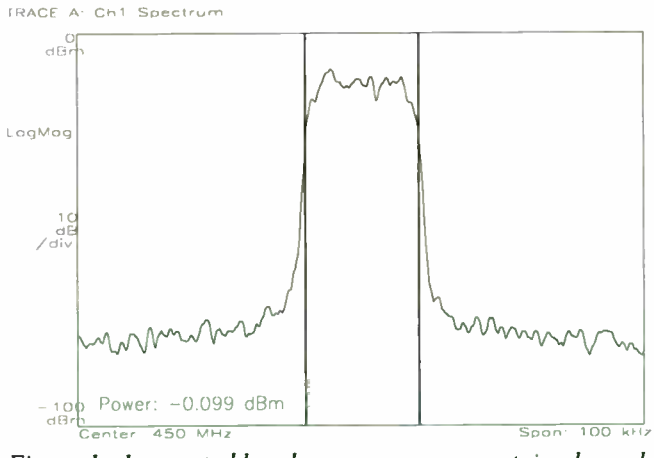

Figure 1: Integrated band power measurement, in-channel power measured as -0.01 dBm

The band power markers are then positioned over the adjacent channel and its power is integrated as well. The difference between this reading and the reference figure is a direct measure of ACP. This measurement is illustrated in figure 2.

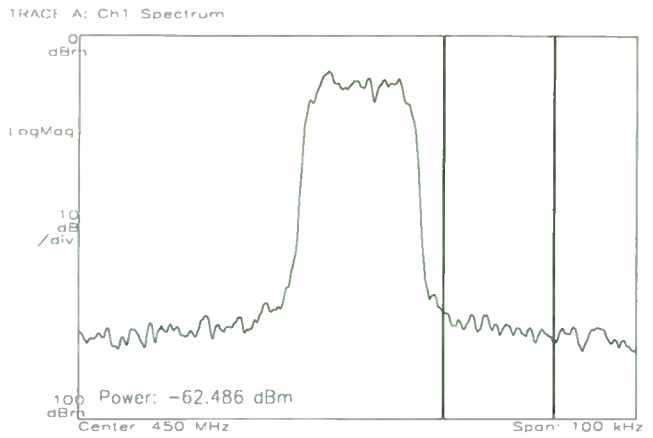

Figure 2: Integrated band power measurement, adjacent channel power measured as --62.5 dBm

The benefit of the real-world nature of this test goes far beyond the theoretical. *In some systems ACP and IMD indeed do not correlate in the expected manner.* Strategies for minimizing IMD such as increasing amplifier current and selecting amplifiers for minimum IMD may provide no benefit in actual radios and could actually create problems in the following areas:

- Poorer amplifier yield--Selecting for minimum IMD could result in the discarding of amplifiers with acceptable ACP.
- Higher manufacturing costs--Wrongly discarding useful amplifiers and tuning others for a parameter that does not actually improve performance increases the resources spent on each amplifier.
- Increased power drain/shorter battery life--Changing the operating conditions of an amplifier could result in shorter operating time for portable equipment with no benefit in operational performance and perhaps a heat-related reliability penalty..
- Larger size/weight for portable products--Another penalty of higher-power operating conditions is the need for larger batteries and power supply circuits.
- Longer design cycle--Achieving the same level of real-world performance and reliability in a system takes longer when the wrong parameters are optimized.

Example: Error-Vector-Magnitude

The basic measure of digital radio performance is Bit-Error-Rate (BER). However in most design situations this is a catastrophic indicator and not a continuous measure of modulation quality. Specifically, a bad BER can indicate that a problems exists but provides no insight into the nature of the problem. Conversely a good BER may mask developing problems and give no indication of problems until failure is imminent.

Other measures of modulation quality have been developed which are more narrow indicators of overall radio performance but which offer much more diagnostic insight. Magnitude and phase error (sometimes referred to as global phase error) are good examples. One of the best indicators is a composite of magnitude and phase error--Error Vector Magnitude (EVM). EVM is shown graphically in figure 3 below.

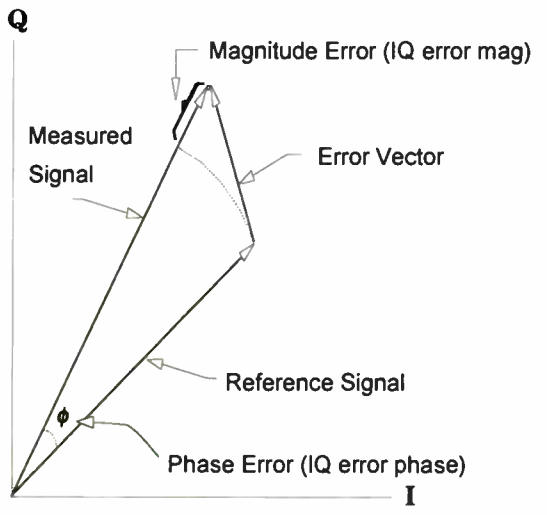

Figure 3: Error Vector Magnitude is the vector difference between the measured I-Q signal and an "ideal" reference signal.

EVM refers to the vector (I-Q or magnitude-phase) difference between the actual and ideal symbol locations at the decision point or the symbol clock. From the diagram it can be seen that magnitude and phase errors are component parts of EVM. Since amplitude errors can cause data errors even in constant-amplitude modulation techniques it is beneficial to look at EVM in most cases. Thus EVM will be the focus of demonstrations in this paper, though amplitude and phase (or I-Q) error measurements may be performed in a similar fashion with the same equipment and are also described.

EVM is a very flexible measure of system or block performance. It can be applied globally, to an entire modulator system or to an entire burst. Alternatively ,

it can be used to evaluate individual blocks or to examine a single troublesome symbol isolated from a long sequence. Most importantly, it relates *directly* to the proper functioning of a component or system and it can be evaluated both visually (for a general appraisal of functionality) and numerically (for a precise measure of modulation quality.

The principal drawback of measuring EVM is its complexity. Not complexity of use, but complexity of execution. EVM is essentially a *residual* measurement and, as such, it requires the generation of an ideal signal for comparison. The measurement/computation process is shown in Figure 4 below.

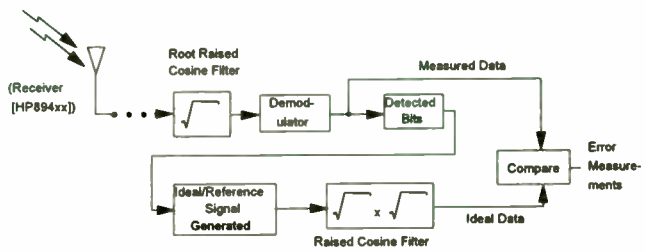

Figure 4: Calculation Error Vector Magnitude and/or its component parts requires the generation of an ideal reference signal. Generation of this signal may also involve filtering to match specific system requirements.

Generation of an EVM measurement is a two-path process. The modulated signal is downconverted if necessary and then demodulated using a carrier lock algorithm. The recovered modulation is processed to recover a symbol clock and is often passed through a channel filter. Channel filters are used to limit signal bandwidth and to improve receiver sensitivity and may be implemented in the transmitter, receiver or both. The most common filters are Gaussian and raised-cosine (Nyquist) or root-raised-cosine.

Production of the reference signal starts with decoding the bit sequence represented by the signal under test. This bit sequence is used along with the specified modulation parameters of the system (channel filter bandwidth and type, symbol rate) to digitally create an "ideal" signal trajectory corresponding to the symbol sequence from the actual measured trajectory. The vector difference (residual) between the real and ideal trajectories is the system error, also called I-Q error. An example of these two trajectories (overlaid) is shown in Figure 5. The modulation format of the signal is 16 QAM and the symbol rate is 3.84 MHz.

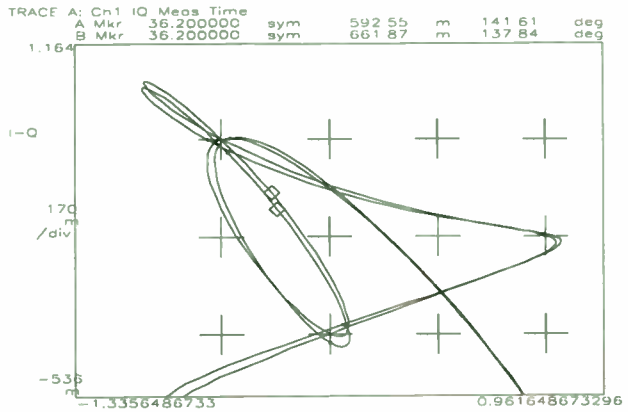

Figure 5: Measured and ideal (reference) I-Q signal trajectories overlaid. This is an expanded portion of a 16QAM vector (polar) measurement. The trajectory is measured at a resolution of 10 points per symbol. For clarity, only 10 symbols of a 100 symbol measurement are shown.

The generation of I-Q error is thus a complex process requiring precision measurements and extensive signal processing. Fortunately the uses of this parameter are simple and intuitive and quite powerful, and the complex signal processing can be performed by advanced analysis equipment. Since all the complexities and details of the modulation technique are taken care of automatically the designer can focus on the residual errors alone--errors that directly represent the non-ideal behavior of the signal or system. Analysis tools such as vector signal analyzers are now available with appropriate algorithms and high speed signal processing that can perform these measurements fast enough for real-time evaluation and adjustment.

An example EVM measurement is shown below in two different views as Figure 6. A group of 100 symbols has been demodulated and EVM has been measured as described above.

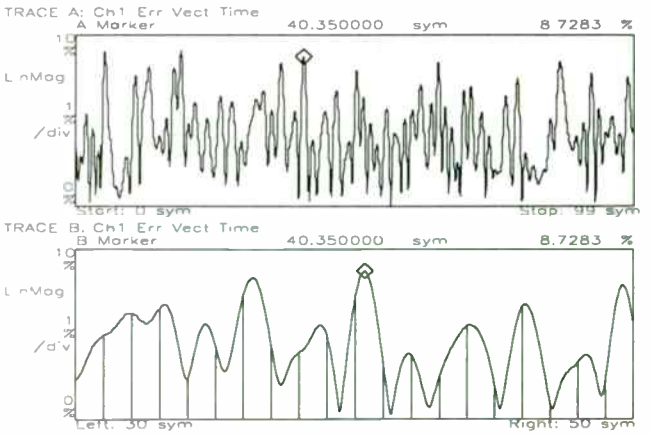

Figure 6: Error Vector Magnitude measurement of 100 symbols (top trace). In the lower trace the scale has been expanded around the point of maximum error and vertical lines are used to signify the symbol times. Only 20 symbols of the measurement are shown in the lower trace. Note that maximum EVM does not occur at a symbol time.

In Figure 6 above EVM is plotted vs. time, where time is expressed in symbols. At the symbol rate of 3.84 MHz and with 10 measured points/symbol, EVM is calculated every 26 ns. In the upper trace the EVM of the entire group of 100 symbols is shown. This is a useful macroscopic display of error behavior over an entire burst, and this analyzer can measure bursts of over 4000 symbols in length. In this longer view error trends can be spotted, and the overall EVM behavior can be assessed. Built-in peak search routines can be used to easily find the maximum error in a burst.

The lower trace provides a much closer view of the same information. A section of the upper trace representing only 20 symbols is expanded to show error magnitude around the peak error found in this burst. This allows error behavior to be examined symbol-by-symbol, showing the transition between each state.

Time domain measurements of error such as this can be made to show even more detail. The measurements above were made with a resolution of 10 point/symbol. With sufficient sample rate, memory etc. these measurements can be made with many more points/symbol--up to 20 in the case of the analyzer used here. In addition to more frequent sampling, the analyzer must generate more frequent "ideal" signal states to compare to the trajectory of the actual signal. Thus the signal trajectory between symbol states (decision points) can be closely examined as well, and compared to an ideal. Such a measurement is shown in Figure 7 below.

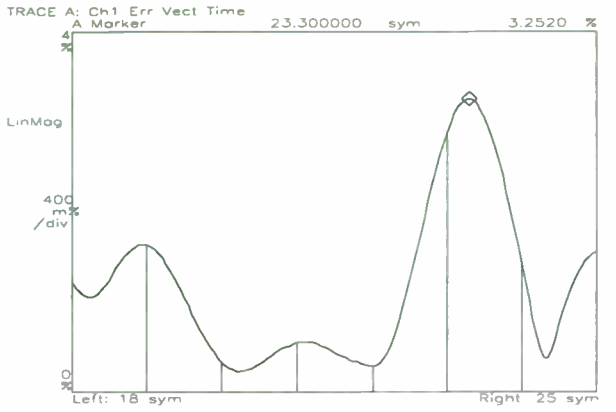

Figure 7: Error Vector Magnitude measurement of 8 symbols with a resolution of 20 points per symbol. The signal is NADC, π/4DQPSK, with a symbol rate of 24.3 kHz and an alpha of 0.35

As it is with many other measurement situations, additional processing of this time-domain information provides much more flexible and powerful analysis. The simplest example is the use of peak search and RMS routines. Identifying the peak EVM and the symbol or transition associated with it can reveal modulator errors. An RMS value of EVM provides an overall measure of modulation quality or level of interference.

Perhaps the most powerful use of EVM comes from frequency domain analysis of the error signal. Since the modulation has been effectively removed, small amounts of noise, interference and nonlinearities can be isolated, measured and their causes tracked down. This process is demonstrated in the following figures.

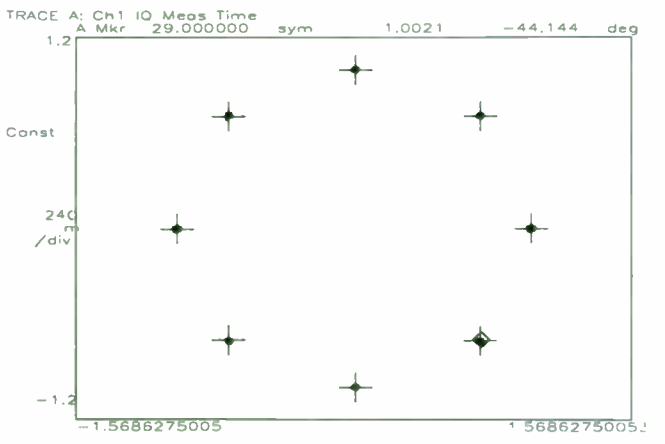

Figure 8: Constellation diagram of an NADC signal with a spurious in-channel signal added. The signal is measured

only at its decision points, and the ideal I-Q values for the signal trajectory at the decision points are shown as crosses.

In the constellation diagram above some errors are evident in the dot groups which are not exactly on the crosses. The I-Q errors are shown in magnitude and phase form in Figure 9 below.

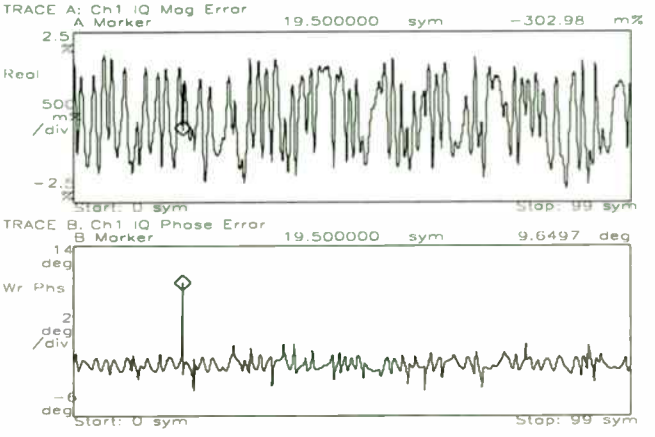

Figure 9: Magnitude and phase error of an NADC signal with spurious distortion. The large phase error occurs during the transition from symbol 19 to symbol 20 when the signal trajectory passes near the origin and the effect of the interference is on signal phase is much greater.

In this format errors such as amplitude droop, group delay and phase jitter can be more clearly isolated. As with EVM above, peak values can be examined and linked with particular symbols (states) or symbol times (the beginning of a burst, for example).

Where interfering signals are suspected, the error signal can be transformed to the frequency domain for identification as in Figure 10.

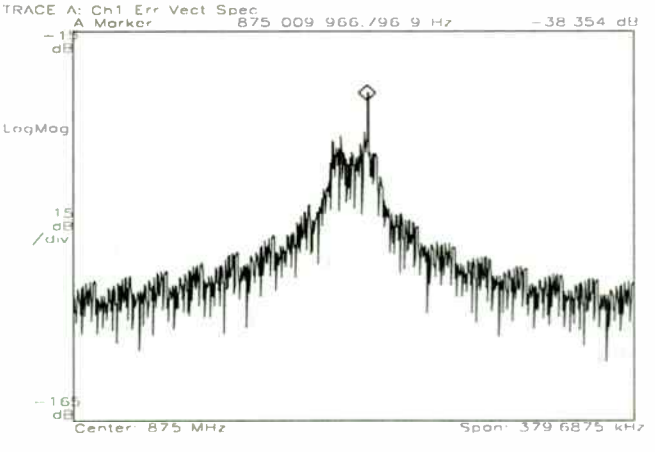

Figure 10: Error vector spectrum measurement of an NADC signal with spurious distortion.

The discrete signal shown in the measurement above can be seen in no other way, since its power is approximately 40 dB below the power of the modulated signal itself. In any direct spectrum measurement the interference signal would be swamped by the main signal. This is true, even though the interference could contribute to errors in the system or degrade the error margin. While the interference in the example above is a discrete signal, noise-like interference could be handled in the same way, and would be even harder to detect or measure by any other means.

This is an important benefit of residual measurements where the main signal is removed. Such measurements provide a high resolution indicator of the various elements of system performance. This is especially valuable in design optimization efforts where systems are already working and designers need to differentiate between small changes in performance.

Other Measurements

The architecture and signal processing of vector signal analyzers provides for many other examples of real-world testing. Some, beyond the scope of this paper include:

- Phase perturbation measurements such as phase jitter, time jitter, phase deviation, peak and RMS phase deviation. The analyzer's combination of direct phase demodulation, auto carrier compensation and band power markers provide time-domain measurements of phase deviation corresponding to actual system behavior.
- Carrier frequency measurements of phase and frequency modulated signals. A linear regression of demodulated phase slope yields a fast, accurate measurement of carrier frequency for singly-modulated signals.
- Instantaneous power measurements. Digital demodulation without normalization provides a polar (vector) measurement which can be scaled in dBm. Signal power can be measured at every point in the trajectory, and changes to parameters such as filter alpha can be evaluated for their effect on required amplifier power.

Measuring Carrier Frequency of Wireless Communication Systems in the Presence of π/4 DQPSK Modulation

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Introduction

Modern modulation methods, such as π/4 DQPSK and MSK, impose deliberate phase and frequency changes on a carrier in order to transmit data. This affects the timing of the zero crossings of the signal. Depending on the modulating data, the number of zero crossings in a given time is often quite different from what would be seen on an unmodulated carrier. This presents a challenge when trying to measure or monitor the carrier frequency in the presence of modulation. This may be especially true for wireless systems early in the design phase when dedicated test equipment does not yet exist. Frequency counters, for example, measure average frequency by counting cycles in a given time (or time for N cycles). They will produce answers which fluctuate randomly—and often significantly—around the true carrier frequency if modulation is present.

This paper describes a method of accurately measuring carrier frequency in the presence of digital modulation. The example used to illustrate the technique is π/4 DQPSK modulation which is found in the NADC and JDC cellular radio systems. The technique is by no means limited to these systems and can be adapted to cover other modulation techniques based on similar frequency or phase modulation.

The measurement requires a Time Interval or Modulation Domain Analyzer to gather zero crossing time stamps. This is the raw data needed by an algorithm which produces a very accurate estimation of carrier frequency in the presence of modulation. At the present time, this algorithm is implemented as a Windows application on a PC.

The technique involves decoding the data imposed on the carrier. Dynamic characteristics of the signal, such as Phase and Frequency Deviation versus time, are computed. The program can also compute the Fourier transform of both Phase and Frequency Deviation and display plots of phase and frequency spectra.

Applications

There are a number of applications for this technique. It is clearly useful in the design of modern cellular radio systems. It should be useful to efforts aimed at identifying and classifying radio transmissions. In general, it can contribute to any situation where it is necessary to measure carrier frequency in the presence of phase modulation or where it is desirable to recover digital information encoded in phase.

Basics of Time Interval Analyzers

A brief introduction to Modulation Domain and Time Interval Analyzers is presented to ensure the reader has a basic understanding of how these instruments work.

A Time Interval or Modulation Domain Analyzer time-stamps and records certain zero-crossings of a signal. The signal is "sampled" in the sense that every Mth edge (rising or falling or both) is time stamped against the instrument's clock to a high degree of precision—typically less than 100 ps. Figure 1 illustrates how the TIA captures the timing information from a simple sinewave.

In this simple example of estimating frequency, the TIA samples (time stamps) every 8th positive zero crossing of a sinewave to a precision of 50 ps. Table 1 excerpts typical results using a total of 1024 time stamps. In this case, 8 edges of the signal occur about every 100 ns so the signal is on the order of 80 MHz.

A much more accurate estimate of the signal frequency can be obtained by using a least squares fit over the Event-Time columns illustrated in Table 1. The slope of the fit is a very good estimate of the frequency averaged over the 1024 samples taken. In fact, if the signal is a stable unmodulated clock and the error is entirely due to the round-off error in each measurement of 50 ps, the regression method can estimate the frequency to better than .05 ppm (4 Hz) in the relatively short measurement of time of 102 μs.

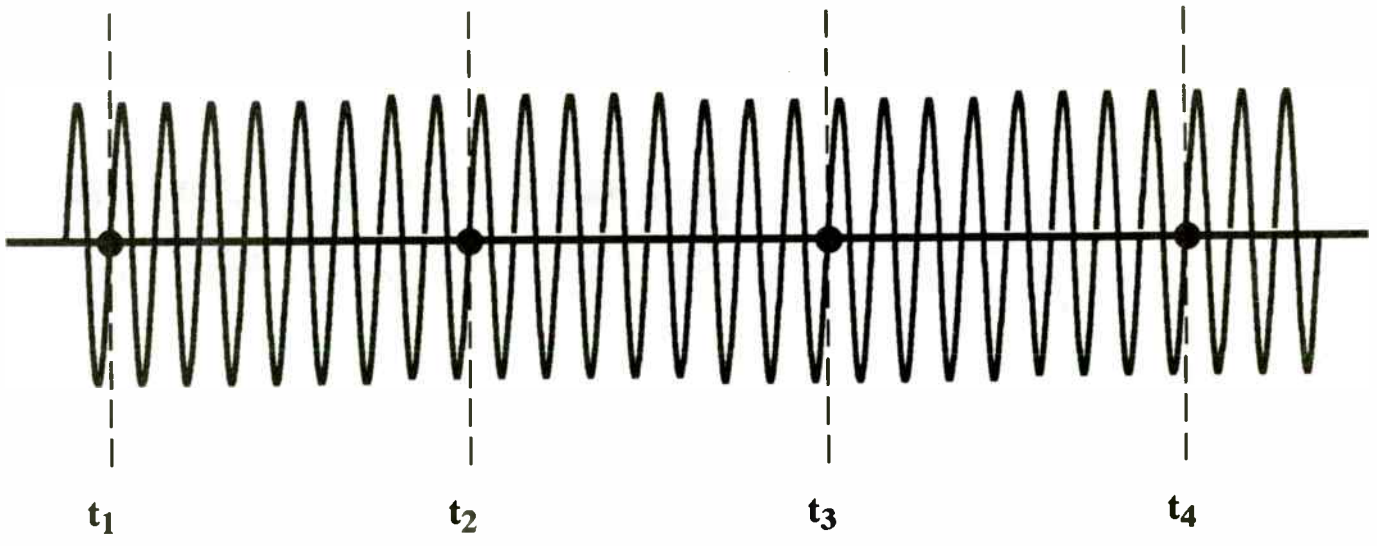

Figure 1. *Simple illustration of how a Time Interval Analyzer works. Black dots indicate time stamps. In this case, an sample is defined as every eighth rising edge. Each sample is assigned a precise time stamp.*

Sample #	Time (ns)	Event #
1	00.30	0
2	100.25	8
3	200.35	16
4	300.25	24
5	400.30	32
6	500.40	40
7	600.35	48
8	700.40	56
9	800.45	64
----------	----------	----------
1024	102345.60	8184

Table 1. *Data structure from a TIA.*

Every 8th cycle (in this example) is sampled to a precision of 50 ps against the internal timebase clock of the TIA. Since 8 cycles takes about 100 ns, the signal frequency is about 80 MHz. A linear regression of Events and Time over all 1024 samples gives a very precise frequency estimate for this simple signal—in this case 79.973248 MHz.

Phase Deviation

Once the carrier frequency has been estimated, the phase deviation of the measured signal from the computed carrier can be calculated by simply subtracting the actual phase from the estimated phase. The regression produces a straight line fit $\mathbf{e}_{fit}$ vs t, as:

$$\mathbf{e}_{fit}(i) = \mathbf{e}_0 + f_0 \cdot t_i$$

where t_i is the time-stamp column. The constants f_0 and $\mathbf{e}_0$ come from the regression curve fit.

The slope is f_0 (79.973248 MHz in this example) and the "y-intercept"is $\mathbf{e}_0$. Phase deviation at t_i is the difference between the Event $\mathbf{e}_i$, and the curve fit $\mathbf{e}_{fit}(i)$, i.e.

$$\text{Phase Deviation at } t_i = \mathbf{e}_i - \mathbf{e}_{fit}(i)$$

Figure 2 shows a plot of the Phase Deviation of a π/4 DQPSK signal computed using a linear regression frequency estimate. The effect of a least squares fit is to remove a "best" straight line from the data so no net slope is visible in the result. The frequency estimate of 1.499998964 GHz, however, is not particularly good, being low by 1.036 kHz. The actual frequency is 1.5 GHz. See f_0 at lower left of Figure 2.

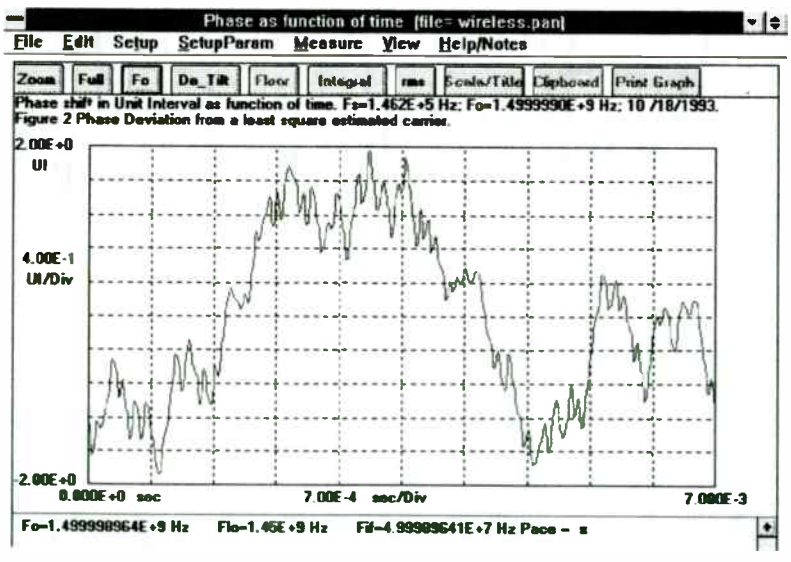

Figure 2. *Phase Deviation of a π/4 DQPSK signal using a Least Squares fit. The phase deviation averages to zero, but the carrier estimate is over 1 kHz off from the true value (1.5 GHz). This is a consequence of the modulation affecting the total cycles per second during the measurement time.*

Frequency Deviation

Dynamic frequency information can also be computed from the event-time data. The simplest method of computing frequency vs time is to divide adjacent event differences by the corresponding time differences, i.e.

$$Freq(t_i) = \frac{e_{i+1} - e_i}{t_{i+1} - t_i}$$

(Maximum bandwidth)

This computation has the highest bandwidth but it is usually very noisy due to the small time intervals involved in the differentiation process. A trade-off of bandwidth for less noise is to use data points further apart such as

$$Freq(t_i) = \frac{e_{i+j} - e_{i-j}}{t_{i+j} - t_{i-j}}$$

(Less bandwidth)

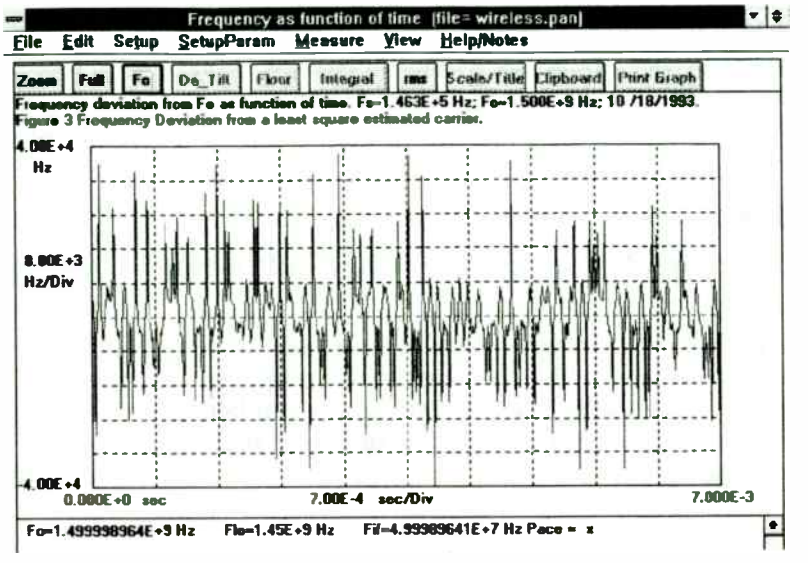

Fig 3. *Frequency Deviation from Least Square Frequency Estimate. The spikes occur at the intersymbol times when phase switches rapidly.*

where j is chosen to trade bandwidth for less noise. The estimate can also be averaged over several j's.

Many people prefer to see the Frequency Deviation rather than absolute frequency. This is done by simply subtracting a fixed constant, usually the estimated carrier frequency, from the frequency at t_i, *i.e.*:

Freq Deviation at t_i =

Freq(t_i) - Estimated Carrier Freq

Figure 3 shows Frequency Deviation vs Time computed from the same raw TIA data which generated the Phase Deviation in Figure 2. In this plot, the frequency is averaged over j=1 and j=2 to obtain a smoother curve at the expense of a slight reduction in bandwidth. Notice the spiking of the frequency at various intervals. The spikes correspond to the intersymbol times when phase switching is most rapid. The spiking rate is at the symbol rate of 24.3 kHz.

For $\pi/4$ DQPSK modulation, a phase change occurs between symbols depending on the two-bit data word modulating it. For example, a 00 data word will generate a + 45° phase change and a 01 word a + 135° phase change. Since the data sequence is random there is no guarantee that, within the measurement period, the phase changes will sum algebraically to zero and therefore leave the total number of carrier cycles in that time frame unchanged.

For example, if there are a lot more 10 and 11 symbols than 00 and 01 symbols the total number of cycles will be less than for the un-modulated carrier. This will fool most electronic counters which keep track of the number of cycles in a given time or reciprocal counters which keep track of the time for a given number of cycles. Either type will report a frequency lower than the real value.

Time Interval Analyzer data processed using linear regression for carrier estimation, generally, does not fare much better. Exactly what would be reported is harder to predict as it depends not only on the total sum of the phase changes but also on the order in which they come in the sequence. Suffice to say that the accuracy is generally not adequate. Fig 2 is an example. TIA data is used to estimate the frequency using linear regression alone. The result is in error by 1.036 kHz.

Estimating Carrier Frequency Specifically for π/4 DQPSK Modulation

The TIA, which simply captures the raw data, is not to blame for the poor frequency estimate. The fault lies with the least squares algorithm because it fails to take into account the precise effect of the modulation.

Linear regression does, however, do a good job of providing a useable first estimate of the carrier frequency. Using this initial estimate and adding a frequency correction which takes into account the effect of the π/4 DQPSK (or other) modulation, it is possible to dramatically improve the precision of measuring carrier frequency in the presence of modulation.

The technique requires knowledge of the modulating data code. This is derived from the phase deviation data.

Starting with the Frequency vs Time data (Figure 3) and knowing the symbol rate the inter-symbol switching times of the signal are established. The symbol "nodes" lie halfway between them. From the least squares Phase Deviation plot (Figure 2), the measured phase change from one symbol node to the next can be found by subtraction. This phase change is rounded to the nearest of 4 discrete values: +45°, -45°, +135°, and -135°. These are the only possible values permitted by π/4 DQPSK modulation.

The computation goes on, one symbol at a time, until all symbols are processed. Next, the discrete phase changes are sequentially added algebraically to generate a "discrete phase deviation" function vs time. Comparison between the discrete phase deviation plot and the least squares phase deviation plot provides the information necessary to correct the frequency estimate. Once the frequency is corrected, a new phase deviation plot is drawn. This is shown in Figure 4.

The corrected frequency is now 1.50000000121 GHz, which is only 1.2 Hz from the true value. (See F_0 lower left of Fig. 4). Note the pronounced tilt of the deviation shown in Figure 4. The tilt is the result of the particular data modulating the carrier and it will vary radically from record to record. It is easy to see why the least squares method is fooled trying to remove this tilt using an incorrect frequency. As a result, Fig 2 shows very little tilt, but the frequency is in error.

The discrete phase shifts collected, of course, yield the modulating code directly according to the table:

1/8 U.I. = 45° → 00
3/8 U.I. = 135° → 01
-1/8 U.I. = - 45° → 10
-3/8 U.I. = - 135° → 11

The recovered code is shown in Figure 4 at the bottom of the illustration. It is displayed in Hex.

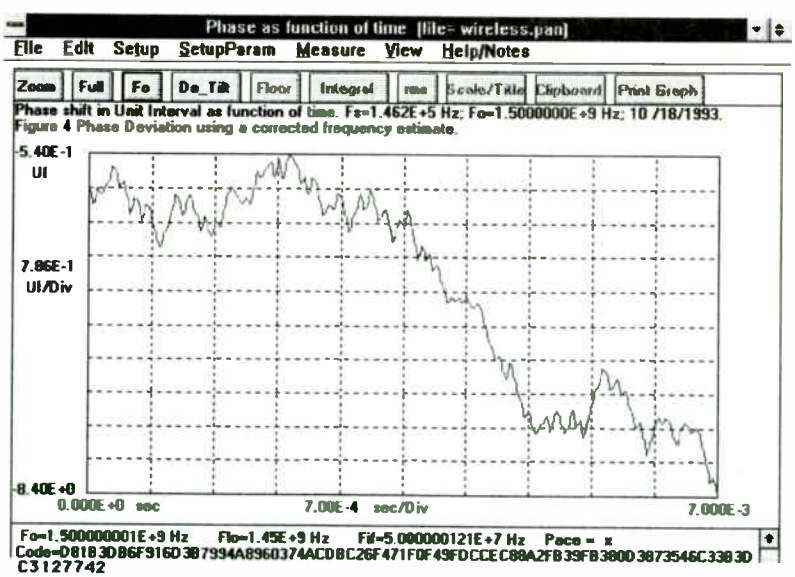

Fig 4. *Phase Deviation using a corrected frequency estimate. The tilt is inherent for this particular modulating data code. A least square fit will try to remove the tilt using a wrong frequency.*

Instrumentation

The measurement system which acquired the data and plots used in this paper is shown in Figure 5. The following explains the role of each item of equipment.

Signal source: The π/4 DQPSK signal is generated by an HP 11846B π/4 DQPSK I/Q Generator. The bit clock of 48.6 kHz comes from an HP 8904A Multifunction Synthesizer. A home-brewed pseudo random data generator provides data to the HP 11846B. The I and Q signals are inputs to the HP 8780A Vector Generator which modulates them to a selected carrier. A carrier of 1.5 GHz is selected in the experiments. The output of this equipment simulates the transmitted signal

Analyzer: The π/4 DQPSK signal is captured by an HP 53310A Modulation Domain Analyzer (TIA) equipped with Option 031. The option allows, among other features, measurement in the GHz region because it provides built-in down-conversion. The HP 53310A is under HP-IB control by a PC. The algorithm described here is implemented in a Phase Analysis program running under Windows 3.1.

System: The 10 MHz time bases of the HP 53310A, HP 8780A, and HP 8904A are locked together so that the accuracy of the frequency estimate can be effectively compared to the frequency (1.5 GHZ) set by the Vector Generator. A local oscillator frequency of 1.45 GHz is chosen for the HP 53310A. This yields an IF frequency of 50 MHz.

Measurement Results

Even though the carrier is at 1.5 GHz and the IF is 50 MHz for the measurements illustrated here, the sampling rate of the signal is only 150 kHz, about 6 times the symbol rate. For a sample size of 1024 this will cover a 7 millisecond window or 170 symbols. The low sampling rate can be a major advantage because it allows maximum use of memory compared to digitizing the entire signal at high speed. The algorithm works well even at 100 kHz sampling, or about 4 times the symbol rate.

The RMS timing error of the HP 53310A is typically 80 ps. This produces a frequency resolution floor of about .1 Hz for an IF of 50 MHz. Usually this is not the limiting factor. The actual phases of the simulated signal depart from the expected values significantly more than the instrument's resolution. This is seen if Figure 6 which shows the Constellation plot of the I and Q signals for NADC using a root Nyquist filter with a shape factor of $\alpha = 0.35$. The nodes are not very distinct as the simulated transmitted signal is measured without a matching filter. The results should be even better if such filters are used.

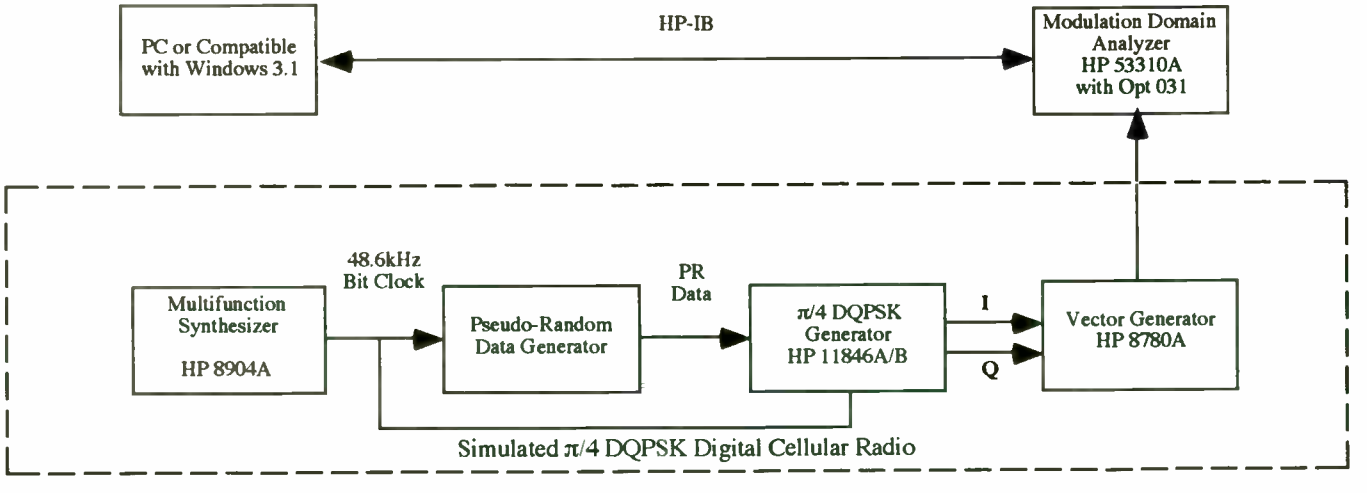

Figure 5. *The TIA (HP 53310A with Option 031) gathers data from the radio which is analyzed by Phase Analysis Software.*

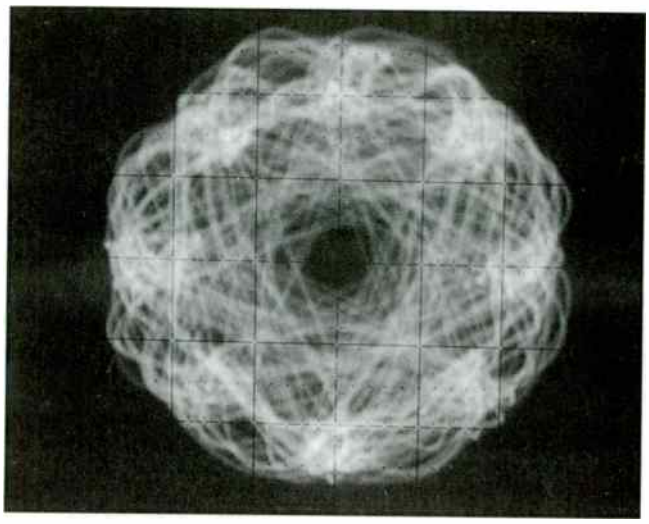

Figure 6. *A Constellation plot of the I and Q signals from the HP 11846B measured using an oscilloscope.*

Phase and Frequency Deviation—Spectral Information

The program can compute the FFT of either the Phase Deviation or Frequency Deviation data. Figure 7 shows the Phase Deviation Spectrum. Figure 8 shows the Frequency Deviation Spectrum.

Symbol Rate Measurement

For the measurements illustrated in this paper, a known symbol rate (24.3 kHz) was manually entered for the calculation. This is not a requirement because the symbol rate can be determined from the TIA data. The "spiking" of frequency in the Frequency Deviation data due to inter-symbol switching is both positive and negative, and no discernible "bright line" appears at the symbol rate in the Frequency Deviation Spectrum shown in Figure 8. However, the transform of the absolute value of the Frequency Deviation shows a clear "bright line" at 24.3 kHz. This is illustrated in Figure 9. The symbol rate can be directly determined from the modulated signal. Once the symbol rate is known, the frequency correction described above can be made.

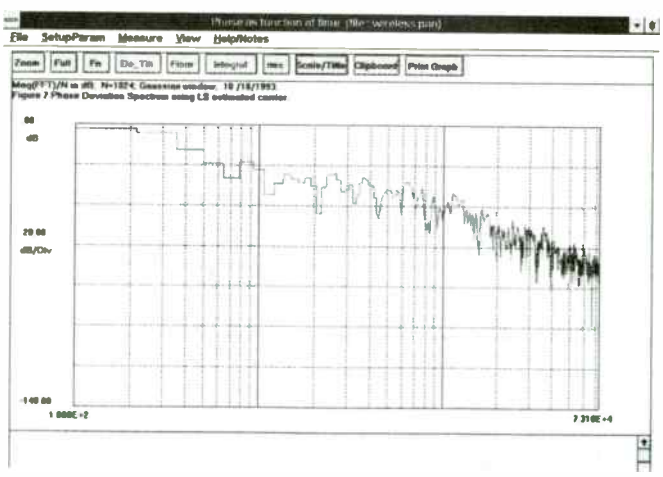

Figure 7. *PhaseDeviation Spectrum*

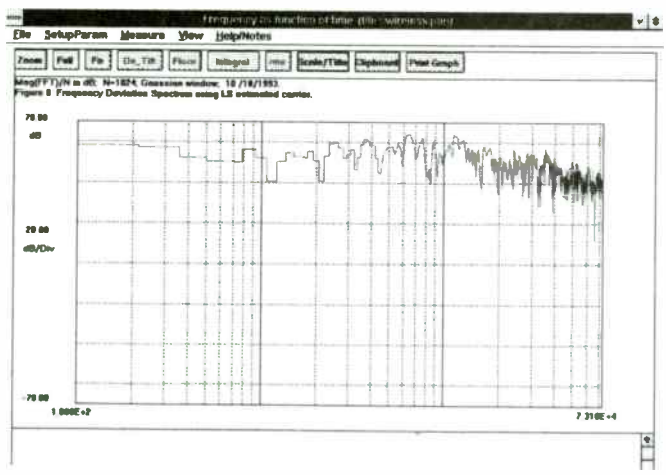

Figure 8. *Frequency Deviation Spectrum No discerable "bright line" can be seen at the symbol rate of 24.3 kHz.*

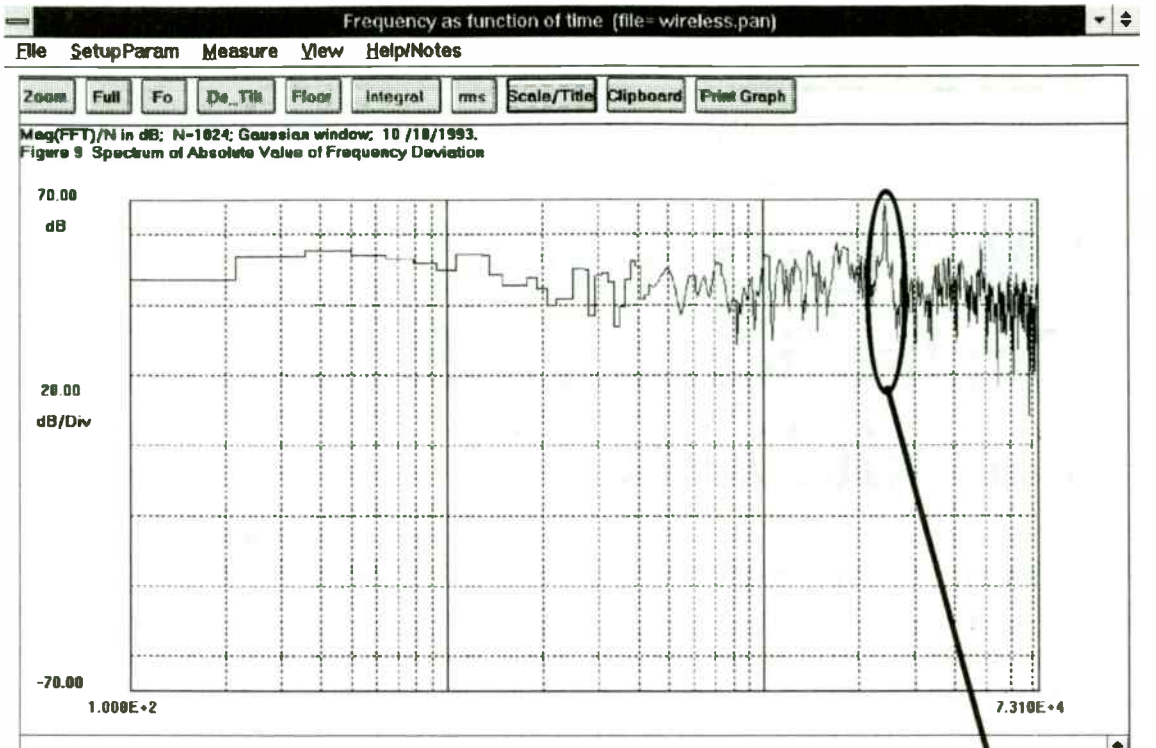

Figure 9. *Spectrum of Absolute Value of Frequency Deviation. A "bright line" is seen at the symbol rate of 24.3 kHz.*

Note "Bright Line" at 24.3 kHz. This is the Symbol Rate.

Summary

Using a TIA sampling at 150 kHz for about 7 ms, the carrier frequency of a $\pi/4$ DQPSK modulated signal can be accurately determined to a few parts in 10^9. The same raw data can generate plots of Phase Deviation, Frequency Deviation, Phase Deviation Spectrum and Frequency Deviation Spectrum. The symbol rate can also be determined from the same data if the application demands it. Modifications to the algorithm can be made to allow similar measurements on other phase modulated signals.

Acknowledgments:

The authors wish to thank Luiz Peregrino for incorporating the algorithm into his Phase Analysis program, giving us the benefit of many necessary computational facilities. Bob Perdriau encouraged us to write the article, edited it and labored to put it into a form which could be published.

References:

D.C. Chu, "Phase Digitizing Sharpens Timing Measurements", *IEEE Spectrum*, July 1988, pp 28-32.

Barry Dropping, "Testing Methods Improve Digital RF Communications", *Microwaves & RF*, July 1992.

SMD Component Evaluation for RF Circuit Design

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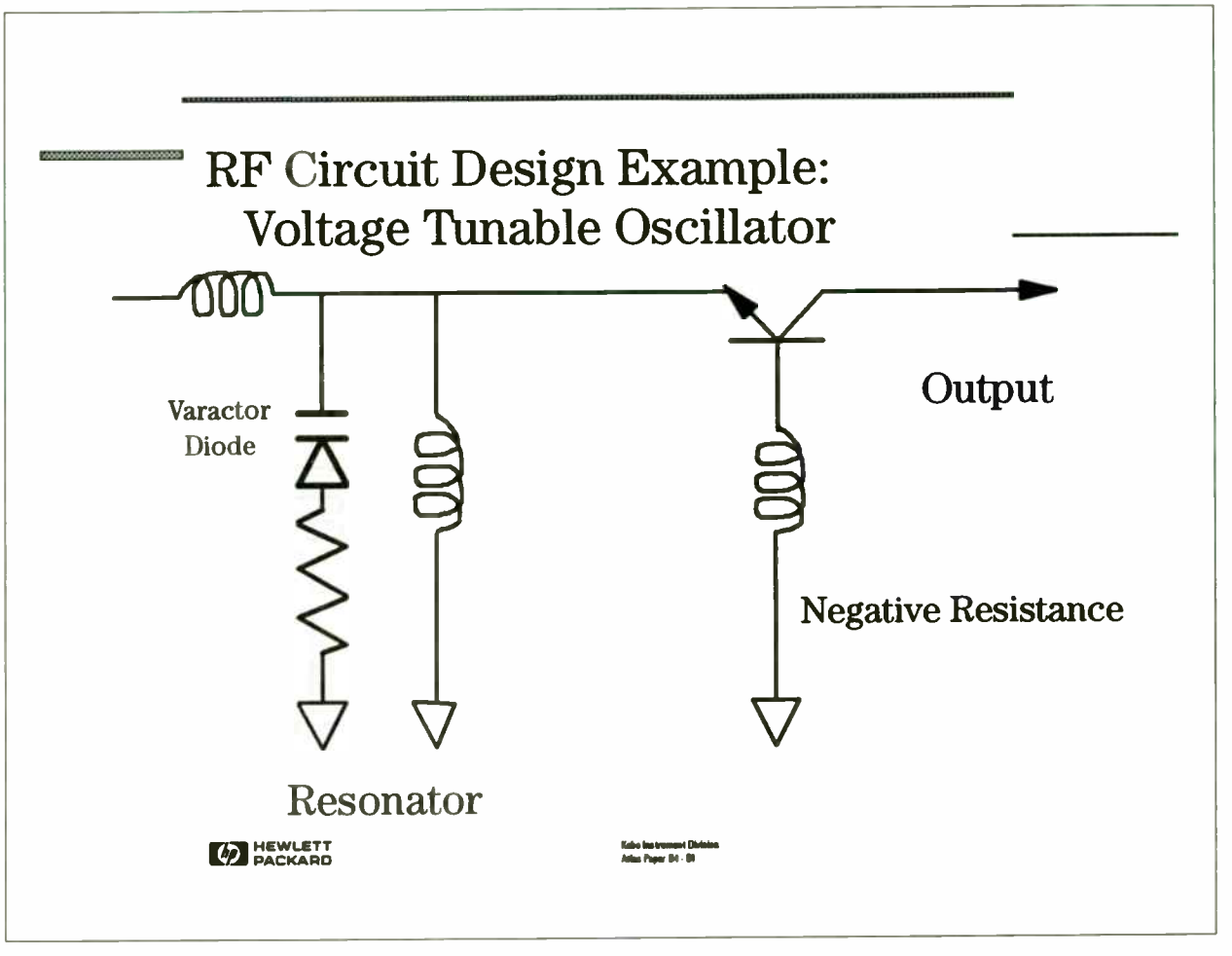
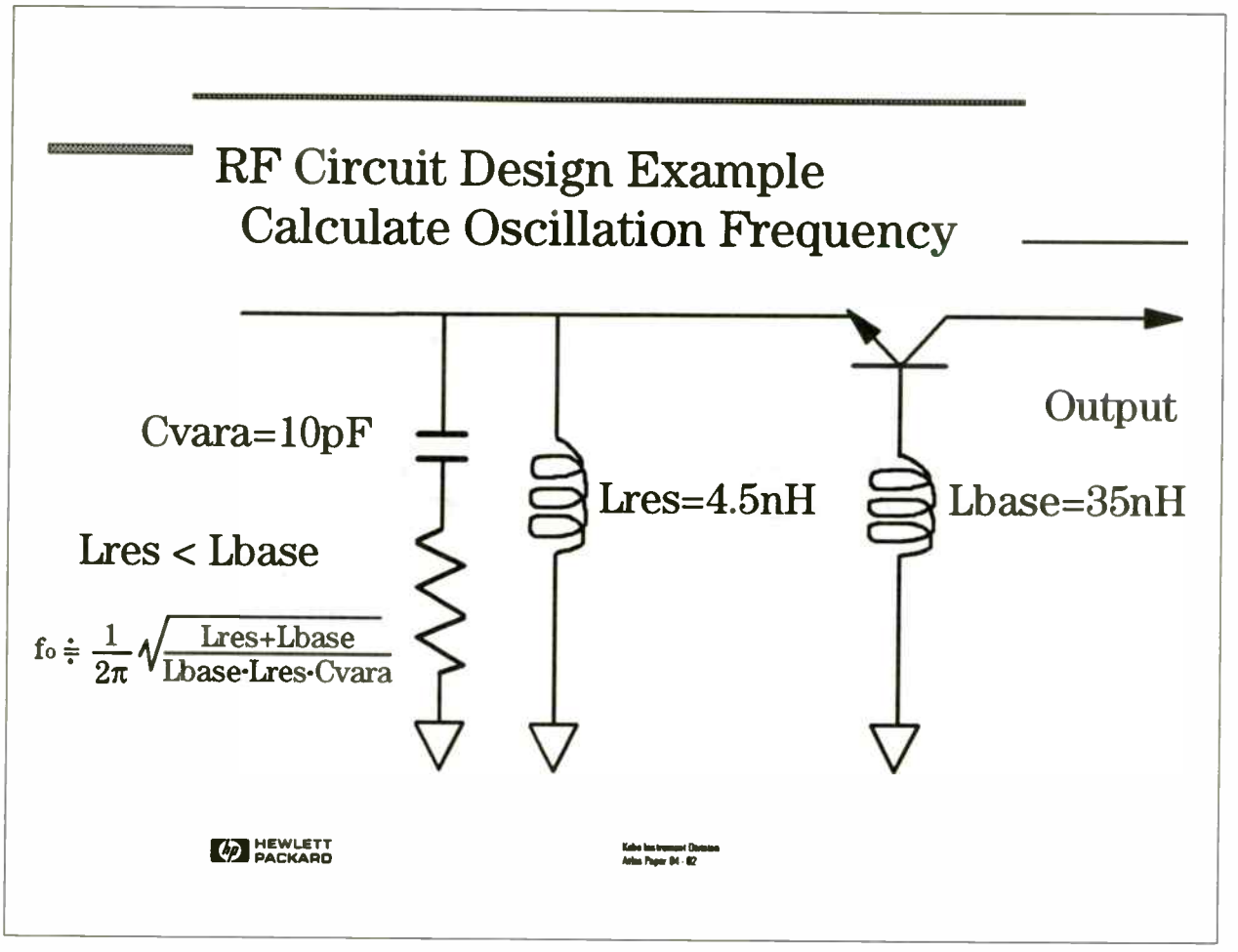
Introducing a New RF I-V Technique

HEWLETT PACKARD

- This paper will explain why impedance measurements for RF components are important for RF circuit design. A newly announced RF I-V technique for measuring impedance is covered in this paper. This technique can measure impedance over a wide measurement range, which is important for RF circuit design.



- This is a typical RF Voltage Tunable Oscillator circuit that is designed to oscillate around 800MHz with a 100MHz bandwidth. We will use this circuit as our example to show the importance of measuring the impedance of RF components.



- If Lres is smaller than Lbase, the center frequency of oscillation can be obtained using the equation in this slide. The capacitance value of the varactor is around 10pF when -5 Volts is applied to the input. This is determinec from the specification of the varactor diode, which is characterised at 10 MHz by the manufacturer. The values of 4.5 nH for Lres and 35nH for Lbase can be calculated by solving this equation.

RF Circuit Design Example: Voltage Tunable Oscillator

The circuit doesn't work as designed!

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- Our first measurement of this circuit shows that it doesn't oscillate at 800MHz until the control voltage reaches -8 Volts, instead of -5 volts. This is a typical problem when a designer uses the "cut and try" method of design.

RF Circuit Design Example: Voltage Tunable Oscillator

Problems:

- Impedance values are dependent upon the operating frequency.
- Component manufacturers specify components only under certain test conditions.

Solution:

- Measure the impedance of the component at operating conditions.

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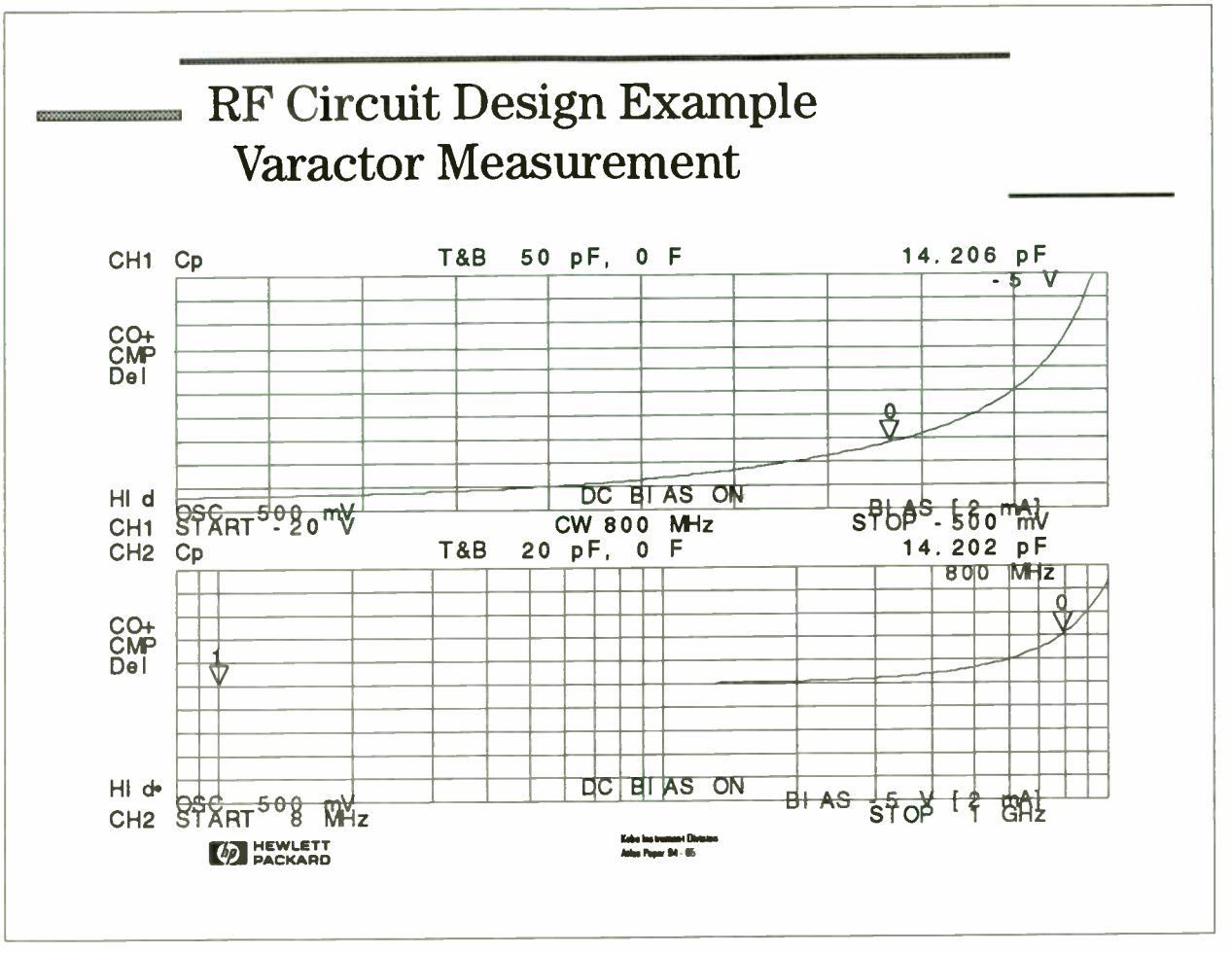
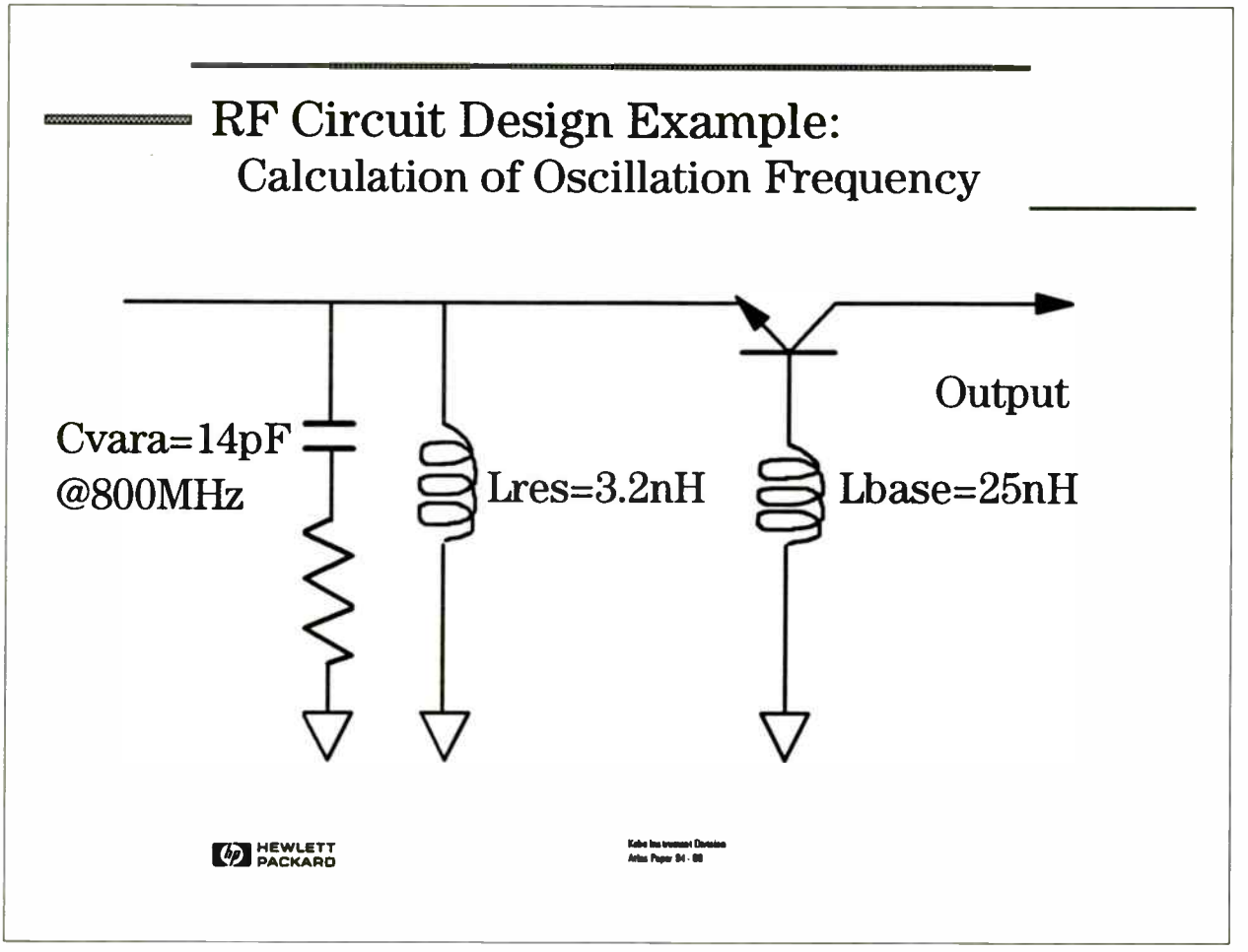
- The reason why our circuit didn't oscillate properly was the capacitance value of the varactor diode. The capacitance value that we assumed in this case is from a specification sheet from the manufacturer. However, we need to measure capacitance value at 800 MHz for proper design.



- The newly announced HP 4291A 1.8GHz Impedance/Material Analyzer can measure this capacitance value at 800MHz very easily. One channel is sweeping frequency with a fixed dc bias while the second channel is sweeping the dc bias with a fixed frequency. The marker of the second channel shows 14pF.



- Using the actual capacitance value of this varactor diode at 800 MHz, values of 3.2nH for Lres and 25nH for Lbase are obtained from the equation. Now, the circuit works as we wanted.

Why haven't RF Components been measured under the operating conditions?

- No Clean Solutions
  - Autobalancing Bridge Technique
    - ★ Limited to 40MHz
  - I-V Technique
    - ★ Limited to 100MHz
  - Network Analyzer (Reflection Coeficient)
    - ★ Accuracy spec'ed around 50 +j0 ohms.

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Kelso Instrument Division
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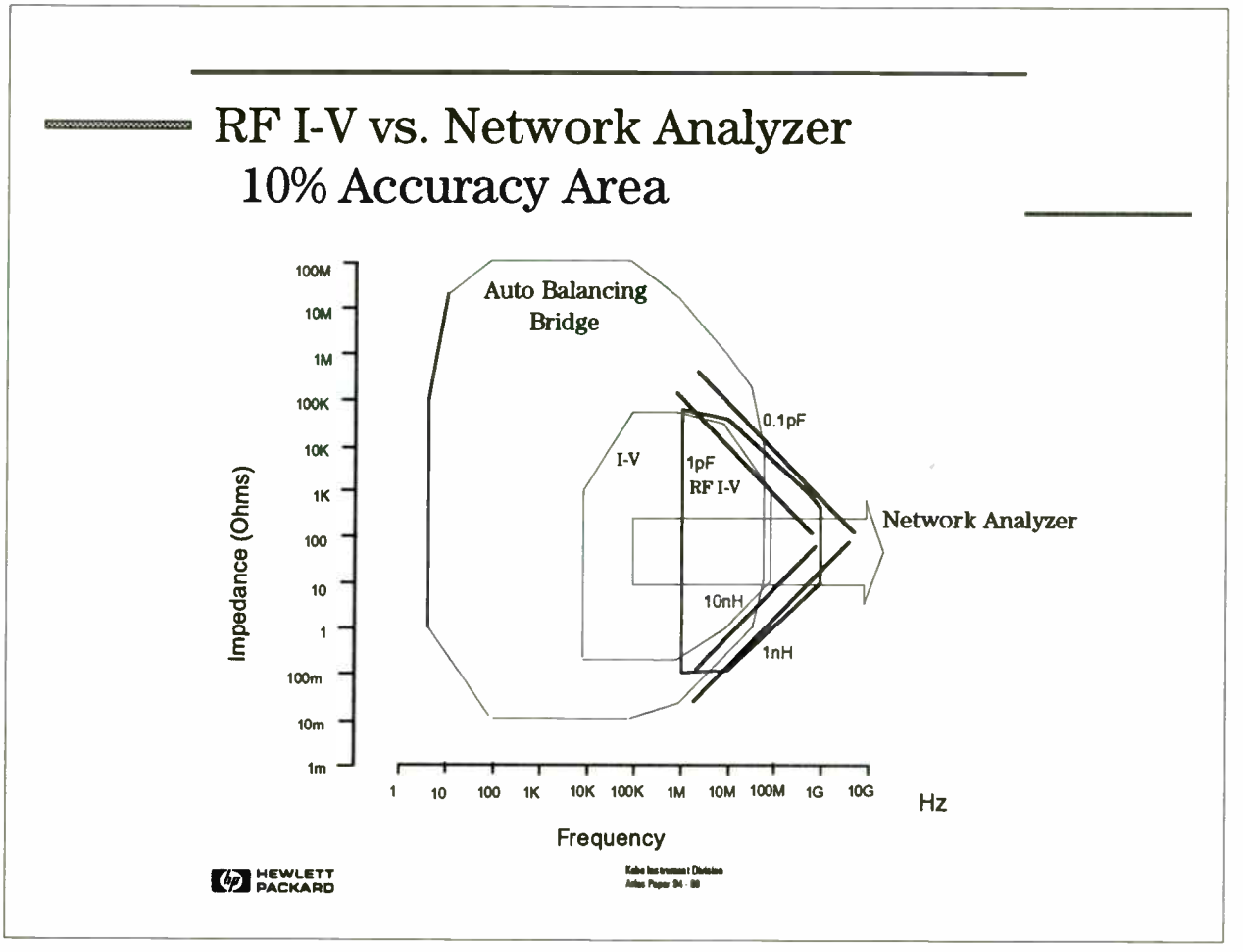
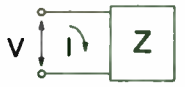
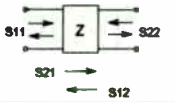
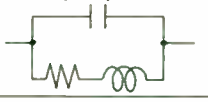
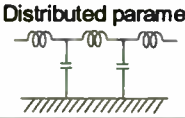
- Before the HP 4291A, there wasn't a good impedance analyzer that could measure impedance of RF components under operating conditions. The Autobalancing Bridge technique and I-V technique can give a resonably wide impedance measurement range, but they have frequency limitations. Network Analyzers can measure high frequencies, but the impedance measurement range is limited to around 50 + j0 ohms.



- This chart shows you the 10% accuracy area o the RF I-V technique and the Network Analyzer technique. Recent RF measurements require 0.1 to 1pF capacitance measurement and 1 to 10nH inductance measurement because RF components are getting smaller. (This is because smaller RF components have small "parasitic" and designed capacitance and inductance.) Until now there was no way to measure these values accurately.

RF I-V vs. Network Analyzer

	HP 4291A	Network Analyzer
Advantatges	* Direct Z parameter Read-out * High Impedance measurement Accuracy * Wide measurement impedance range (Voltage & current absolute value measurements) * High Q accuracy - ALC function - Material Measurement - Temperature Chara.	* Frequency > 1.8 GHz (Signal wave pcwer ratio measurements) * Two port measurement
	* 1 Port Measurements 	* 2 Port Measurements 
Measurement Technique	RF IV Method $Z = \frac{V}{I}$	Network Analysis Method Reflection Co-efficient $Z = Z\left(\frac{1+\Gamma}{1+\Gamma}\right)$
Circuit Theory	Lumped parameter 	Distributed parameter 

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- The traditional way to measure impedance values at RF is with a Network Analyzer (Reflection Coefficient). Basically,the network analyzer measures S11 and converts this to impedance. However, measurement error associated with this calculation will increase when the measurement value is away from 50 ohms. This is because of the poor resolution of the reflection measurement away from 50 ohms.

What Made These Measurements Possible?

A *NEW* RF I-V Technique

- Expanded frequency range
  - Use a wide frequency balun
- Expanded impedance range
  - Amplify measurement signal in the test station

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- Before now, engineers had to rely on impedance values that were measured at low frequency. The newly invented RF I-V technique makes measurement of RF component values at their operating condition possible. There are two major innovations that made the RF I-V technique possible. First, the frequency range is expanded to 1.8GHz by using a wide frequency balun. Also, the measurement range is expanded by using an amplifier and attenuator in the test station of the 4291A.

Other RF Components requiring Impedance Measurement

- Capacitors
- Inductors
- PIN Diodes
- IC Package
- PC Boards
- .....

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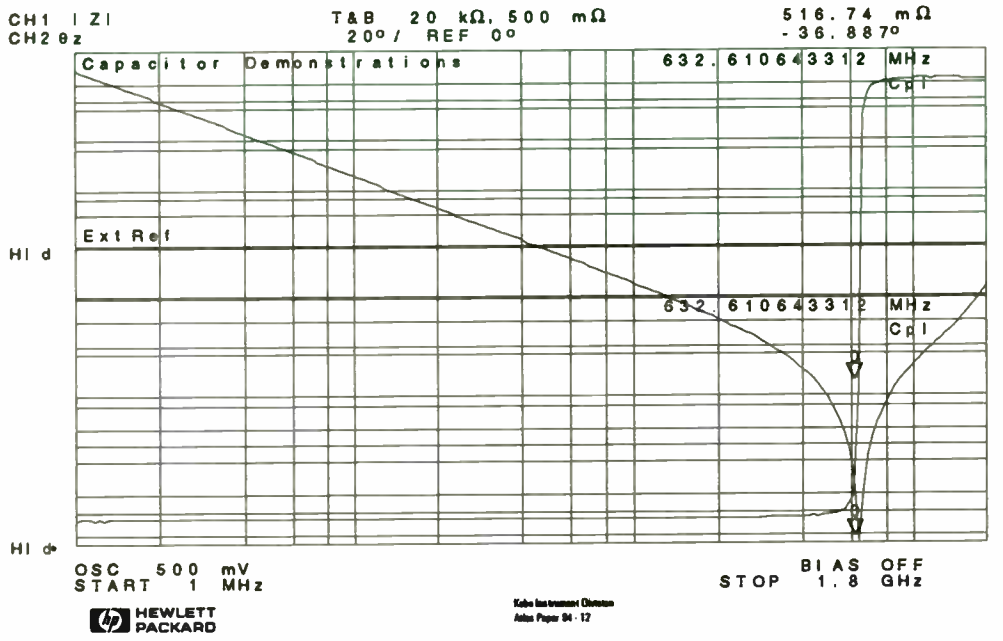
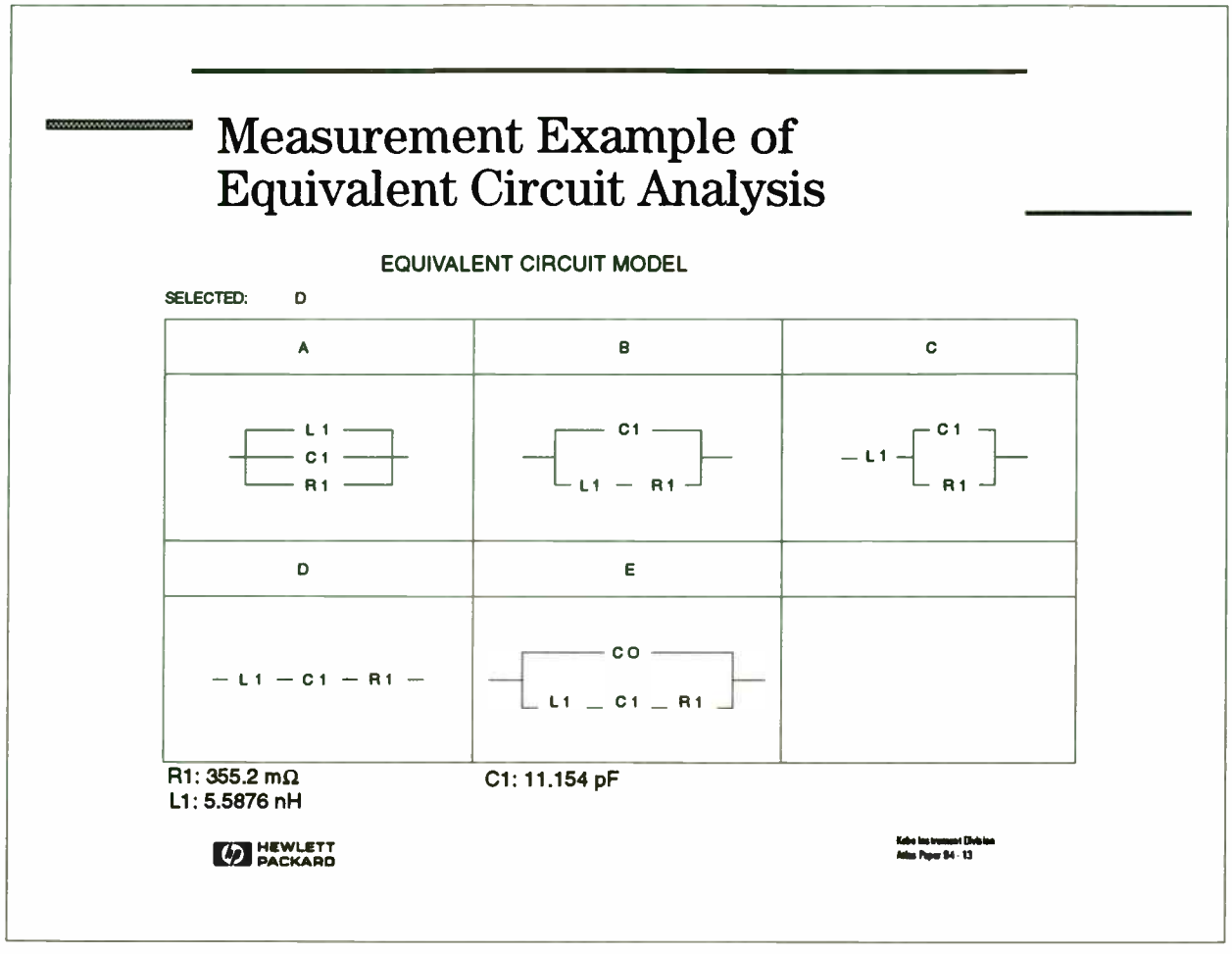
- Not only Varactor Diodes require RF impedance measurements. Capacitors, inductors, PIN Diodes, IC Packages, PC Boards, and other components in RF circuits also need these measurements. The following slides show you some of these examples.

Measurement Example of a Capacitor

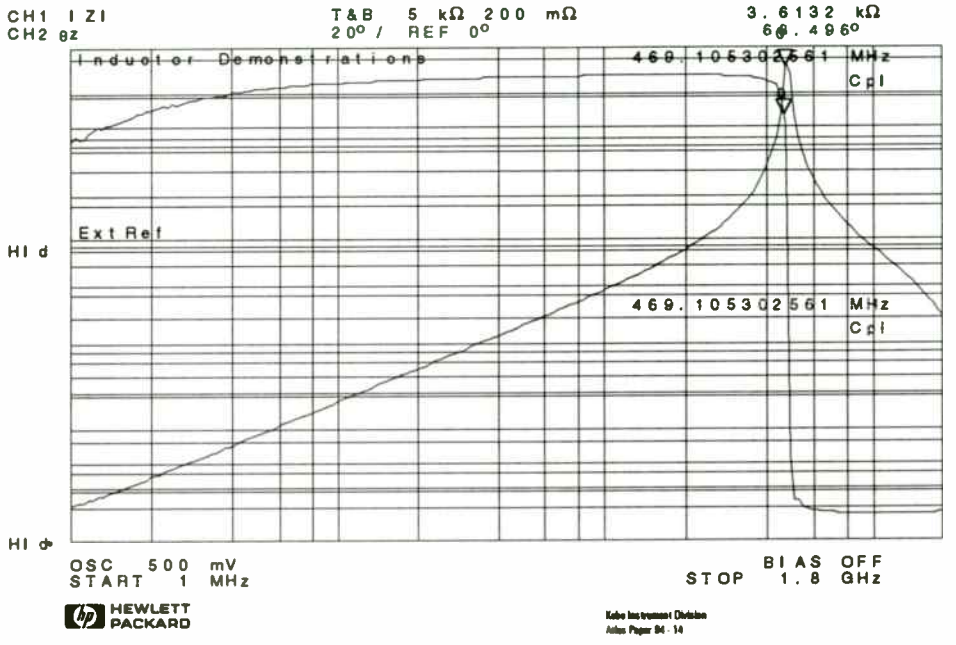


- This slide shows you the frequency characteristics of impedance and phase when a ceramic capacitor is measured. A resonance can be observed around 630 MHz and therefore this capacitor can not be used in a circuit that operates near or above 630 MHz. The RF I-V technique gives a clear peak value even though the series resistance at resonance is only 516 mohms.



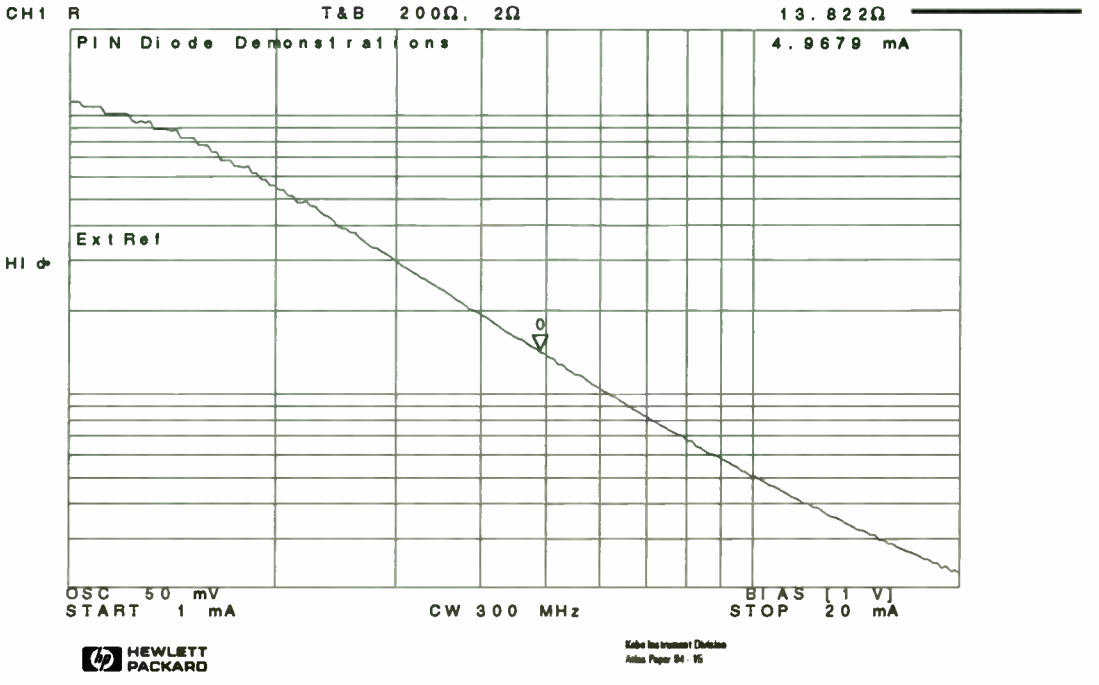
- The Equivalent Circuit Analysis function is useful for wide frequency circuit design. By measuring three values (C1, L1 and R1), a designer can calculate impedance at any frequency. For example, if you measure C and DF (or Q) using an LCR Meter, these values are only accurate at one frequency point and thus will act differently at any other frequency.
- Inductors, Resistors and Resonators can also be analyzed using this Equivalent Circuit Analysis function.

Measurement Example of Inductors



- An inductor measurement almost looks like the opposite of a capacitor measurement. As with the inductor, a resonant impedance value and frequency are observed very easily.

PIN Diode Measurement



- Another example is a PIN Diode measurement. The Equivalent Series Resistance is measured at 300 MHz by sweeping a DC Bias current from 1 mA to 20 mA. This is another important measurement in the RF area. (For example, PIN Diodes are used as switches and attenuators in many RF circuits.)

Multipath Fading Emulation for Wireless Communications

By: Bent Hessen-Schmidt

Wireless communication systems such as GSM, DCS1800, CDMA, IS-54, DECT, and CT-2 mobile telephones are required to be tested while subjected to multipath fading, see Reference [1]. Truly most line-of-sight communication systems can benefit from multipath fading tests.

- First, the power budget for multipath fading is relatively large compared to the allowances for noise figure, carrier to noise ratio, and antenna gain, see Table 1.

- Second, multipath fading causes the amplitude of the received signal to vary, thus increasing the bit error rate, disturbing and, in the worst case, interrupting the communication.

This multipath fading is experienced by the user. The performance during multipath fading is therefore often associated with:

The Quality of the mobile telephone.

Now with the introduction of new instruments the emulation of and testing during multipath fading has become easy.

Table 1. Typical Effect Budget for a Mobile Radio Link

Transmitted power (2 W)	(Px)	+43 dBm
Path Loss	(L)	-143 dB
Nominal Received Carrier Power	(C)	-100 dBm
Data Rate (64 kbit/s)		48 dB/Hz
Nominal Received Bit Energy	(Eb)	-148 dBm/Hz
Bit Energy to Noise Density @ 10-9 BER	(Eb/No)	4 dB
Fading margin	(M)	17 dB
Noise Floor + Noise Figure (5 dB)	(kT+NF)	-169 dBm/Hz

Bent Hessen-Schmidt can be reached at Noise Com (201) 261 8797
Noise Com, Inc. (American Stock Exchange Symbol: NOI)
manufacturers test equipment for wireless & telecommunications
The present line of products include instrumentation for: injection of noise and interference, co-channel and adjacent-channel testing, precision carrier to noise ratio (Eb/No) settings, noise figure measurements, and multipath fading.

The Multipath Fading RF Channel.

Multipath fading occurs when two or more replicas of a radio signal arrive at the receiver with different time delays. The multipath faded RF channel can therefore be emulated as a sum of N rays, whit each arriving at the receiver via a different path thus having different attenuation and delay.

A typical scenario can be the wireless communication link to a mobile telephone. The mobile phone moves through an environment consisting of buildings, trees, the ground, clouds, etc. The transmitter is omni-directional, and therefore some of the transmitted energy is imposed on each of the objects in the environment. It is then reflected from those objects and received by the mobile phone. These reflected signals add as vectors at the receiver causing the amplitude and phase of the received signal to vary, and in the worst case approach zero, disturbing and interrupting the communication. The communication channel can therefore be emulated by multiple paths, normally up to 12 paths, each having an associated doppler, delay, attenuation, and Ricean or Rayleigh (Classical) scattering.

Each related path will have a signal strength most likely less than the power of the direct path. The reflected signals are also delayed relative to the direct since the path lenghts are longer. That is, if a direct path exists. Some of the weaker reflected signals may actually arrive earlier than the strongest reflected signal when a direct path does not exist, see Table 2. Also, in a special case of line-off-sight communication, the refractive index of the air may make the non-direct-wave travel faster and arrive first even though it travelled the longer distance [3].

If the receiver is moving, the paths will exhibit a doppler shift due to the speed of the receiver, but the amount of doppler depends on the angle of the reflecting object relative to the direct path, see Equation 1.

$$fd = \frac{v \cos(a)}{c} fc \qquad (1)$$

where v is the speed of the vehicle, fc is the center frequency of the radio transmitter, c is the speed of light, and a is the angle of arrival as defined in Figure 1.

If the mobile phone is moving directly away from the transmitter, then the doppler of the direct path will reduce the frequency directly in proportion to the speed. If a reflector happens to be in front of the receiver, then the doppler for that path will have equal magnitude but opposite sign of the direct path. Objects to the side of the receiver will cause a doppler shift between these two extremes. For a scenario with homogeneously distributed reflectors the angle of arrival is distributed over 360° resulting in a spectrum

that spreads the signal energy over a band which is the transmitted frequency (F_c) plus and minus the doppler shift (F_d). The spectral power distribution is not flat, but has peaking at the doppler offset since the doppler offset changes slowly at angles of arrival equal to or near 0° and 180° because of the cos(a) term in equation 1. The summation from reflectors at or near 0° and 180° will therefore contain more power, see Figure 2.

Scintillation in the air and objects with irregular surfaces scatters the reflected signal causing a random phase shift. The scattering can be visualized as consisting of many smaller reflections each having a random amplitude and random phase. The phase is usually evenly distributed from 0 to 360°. Each of the reflected signals can be split into two orthogonal vectors $X_i\cos(u) + Y_i\sin(u)$, where X_i and Y_i are stochastic variables, which depend on the additional path length and the reflection coefficients of the obstructions. If none of the stochastic variables are dominating then the stochastic variables, X_r and Y_r, resulting from the addition of the many small reflections will have a Gaussian distribution function. This is a result of the central-limit-theorem. Thus the time-varying amplitude resulting from the scattering can be emulated by adding two orthogonal vectors, each with Gaussian distribution functions.

$$|A| = \sqrt{X_r^2 + Y_r^2}$$

The result is a Rayleigh distribution of the signal amplitude. The vector addition also shows that each path with Rayleigh distributed scattering automatically will have a random phase that is evenly distributed from 0 to 360°. However the paths may still be correlated due to their relationship to each other in the scenario.

The Rayleigh scattered path may be combined with another path which has a strong but unscattered signal. The unscattered signal which could be a direct signal or a reflection from a large often man-made object such as a building may also have a doppler shift. This is for example the case in the emulation of a Rural Area (RAxx) for GSM and DCS1800 mobile telephone systems, Reference [1]. The sum of the unscattered and the Rayleigh distributed signals results in a Ricean distribution. Most multipath fading emulators such as Noise Com's MP-2400, display their own hardware configuration, see Figure 3, and are capable of generating combinations of Rayleigh (Classical) and Rician paths.

The sum of N paths may be expressed mathematically, which has been done excellently by Goldman in Reference [2]. The N-paths multipath faded channel can be described by the transfer function of equation 2.

$$H(jw) = \sum_{n=0}^{N} a_n \exp(-j(w-w_o)t_n) \qquad (2)$$

Each of the variables, a, b, a_n, and t_n, in above model are stochastic variables with statistical distributions as described in Reference [2]. It is important that these stochastical variables take values at random and without repeating in time. Traditionally multipath fadings of channels carrying analog signals have been emulated by use of the Simple-3-path model (also called Rummler's model) in Reference [3] and the 2-path model.

$$H(jw) = 1 - b \exp(-j(w-w_o)t) \qquad \text{2-path} \qquad (3)$$

$$H(jw) = a [1 - b \exp(-j(w-w_o)t)] \qquad \text{Simple-3-path} \qquad (4)$$

However fading of an analog signal does not impair the communication in the same way as the fading of a digital signal. The analog signal to noise ratio degrades proportional to the fading whereas the bit error rate of the digital system will increase proportionally until it reaches a threshold beyond which it looses synchronization of the error correcting algorithms, the clock and the data. Modern digital wireless communication systems uses forward error correction coding, diversity antenna systems, adaptive power control etc. to reduce the impact of multipath fading. Digital mobile radios have also moved into urban areas in cellular systems. Testing while submitted to 12 paths fading is generally recommended for wireless systems, f.ex. GSM, DCS1800 etc., Reference [1]. As a rule of thumb each path which has an average power within 30 dB of the power of the strongest path may impact the communication. Noise Com's MP-2400 Multipath Fading Emulator is therefore designed to contain up to 12 path which may be grouped into two times six paths for testing of adjacent/co-channel interference or diversity systems, see Figure 4.

The correlation between paths is achieved in the Noise Com's MP-2400 Multipath Fading Emulator by summing a portion of the modulation signal from one path with a portion from another. The amount of correlation may be set in percent relative to any other path.

It is important that the above fading distribution functions are implemented correctly and performed identically whether the instrument is used for tests domestically or overseas. Noise Com's MP-2400 therefore downconverts the signal to an intermediate frequency where it is A/D converted before it is split into the 12 paths. Each path is therefore assured to be fed exactly the same digital copy of the signal.

The above described Doppler spreading which may be of Rayleigh or Ricean nature, is obtained by digital processing of the A/D converted signal. The digital operations result in an exact number, limited only by the number of bits of the digital circuitry. These multiplications and modulations are performed in parallel for each paths to maintain real time performance.

The required differential path delay, attenuation, and correlation are programmable for each path, see Figure 5. Each path includes a MAC (multiply/ accumulator) which performs the function of the doppler spreading by mixing the I/Q signal samples with two filtered Gaussian signal sources. Each source is shaped using a digital FIR filter with a bandwidth equal to the doppler rate. The result is then delayed and attenuated digitally before being converted to an analog signal using a D/A converter. The 12 paths are summed at the instrument output, emulating the summation which occurs at the receiver antenna.

The composite signal is upconverted to a microwave frequency using dual conversion, and then downconverted to the received frequency in order to maintain an output free of spurious, image signals, and without local oscillator leakage. The output power can be set between -10 and -100 dBm to match the level expected at the receiver input.

The capability to handle signals of various power levels is very important. Mobile telephones transmit between 5 mW and 3 W average power whereas their peak power can reach 20 W. An AGC control is therefore incorporated in the MP-2400 to maintain the maximum signal-to-noise ratio into the A/D converter. The AGC can be switched On and Off as desired. Noise Com's MP-2400 accepts inputs directly from a transmitter at up to +43 dBm (20 W) and returns it to the receiver with fading at power levels down to -100 dBm. This capability of handling a large dynamic range signal is important because many modern wireless telephone systems use adaptive power control (f.ex. CDMA). The automatic calculation of the output power level of the fading emulator, from -10 to -100 dBm, eliminates the need of external metering and computations.

The MP-2400 emulates a wireless communication channel with up to 12 paths between a base station and a mobile station. It contains an embedded 486DX-33 microprocessor with PC compatible interfaces including an IEEE 488.2 interface to provide an easily transportable selfcontained instrument. The built-in AT style keyboard, mouse and flat panel color LCD display make the MP-2400 an extremely powerful tool as a stand alone instrument or as a controller for an entire test station.

MP-2400 is also available with two independent channels of 6 paths each. These two channels are used to emulate multipath fading for the tests of diversity systems or to independently fade an interferer and a desired signal. The interferer may be an adjacent or co-channel signal as required for the test of GSM and DCS1800 mobile telephones. Figure 4 shows a block diagram of a diversity and interference test with two MP-2400s emulating 4 channels with 6 paths each. Multipath fading can be emulated in both static and dynamic modes on the MP-2400:

- In STATIC MODE the user sets the desired parmeters for each path. Standard test conditions for GSM, DCS, NADC (CDMA), etc. are factory stored and can be recalled from memory. Up to eight sets of conditions can be linked into a single file and run uninterrupted.

- In DYNAMIC (GRAPHIC) MODE the user enters the initial and final parameters for a dynamic scenario. For example, a mobile receiver starts at rest, then accelerates to 96 km/h (60 Mph) over a 5 minute period. The user inputs the scenario including the reflecting objects on a graphic display, see Figure 1. Software calculates intermediate states for doppler, delay and attenuation.

The path settings are displayed on the VGA monitor in a tabular form. The instrument status and graphic representation of certain scenarios, the doppler spectrum, and the hardware configuration may also be displayed. Other available features are a help key for setting up path characteristics for desired scenarios and Recall/Save of setups. The user has the option to select the best matching shape of the doppler spreading from a library if the antenna pattern is different from the standard omnidirectional model.

Conclusion.

Effective multipath testing of modern communication systems, besides being a requirement, can also help making these systems more efficient. Today, it is possible to make modern communication systems which tolerate severe multipath fadings. These new wireless systems employing sophisticated modulation, diversity antennas, adaptive equalization, forward error correction coding, phase locked synchronization, and adaptive transmitter power control techniques, may soon all be tested using multipath fading emulators.

References:

[1] ETSI/TC GSM 05.05 - "Radio Transmission and Reception" version 3.12.0, European Telecommunication Standards Institute, February 1992.

[2] "Mathematical Analysis of the Three-ray Dispersive Fading Channel Model", Haim Goldman, IEE Proceedings-I, Vol. 138, No. 2, April 1991, pp. 87-94 .

[3] "A New Selective Fading Model: Application to Propagation Data", W.D. Rummler, Bell Systems Technical Journal, Vol. 58, No. 5, May - June 1979, pp. 1037-1071.

NOISE/COM's MP-2400

Frequency	800 to 2500 MHz or 10 to 6000 MHz
# of Paths per Instrument	Up to 12
# of Channels per Instrument	Up to 2
User Interface	Built-in 486DX-33
Keyboard	Incl. Trackball
Display	Built-in Color LCD (VGA)
Remote Interface	IEEE-488.2
Operating System Software	Microsoft Windows[R]
# of Stored User Files	Unlimited
Signal Processing	All Digital
Frequency Conversion	Triple Conversion System
Channel and Common Delay	Up to 204.8 us
Delay Accuracy	+/- 5 ns
Signal Input Power	-10 to +43 dBm
Peak Detecting AGC	30 dB Range with ON/OFF
Output Power Computation	Yes from -10 to -100 dBm
Spurious Signals, All Types	Better than -60 dBc
Size	455mm D x 364mm W x 197mm H

Microsoft Windows[R] is a registered trademark by Microsoft

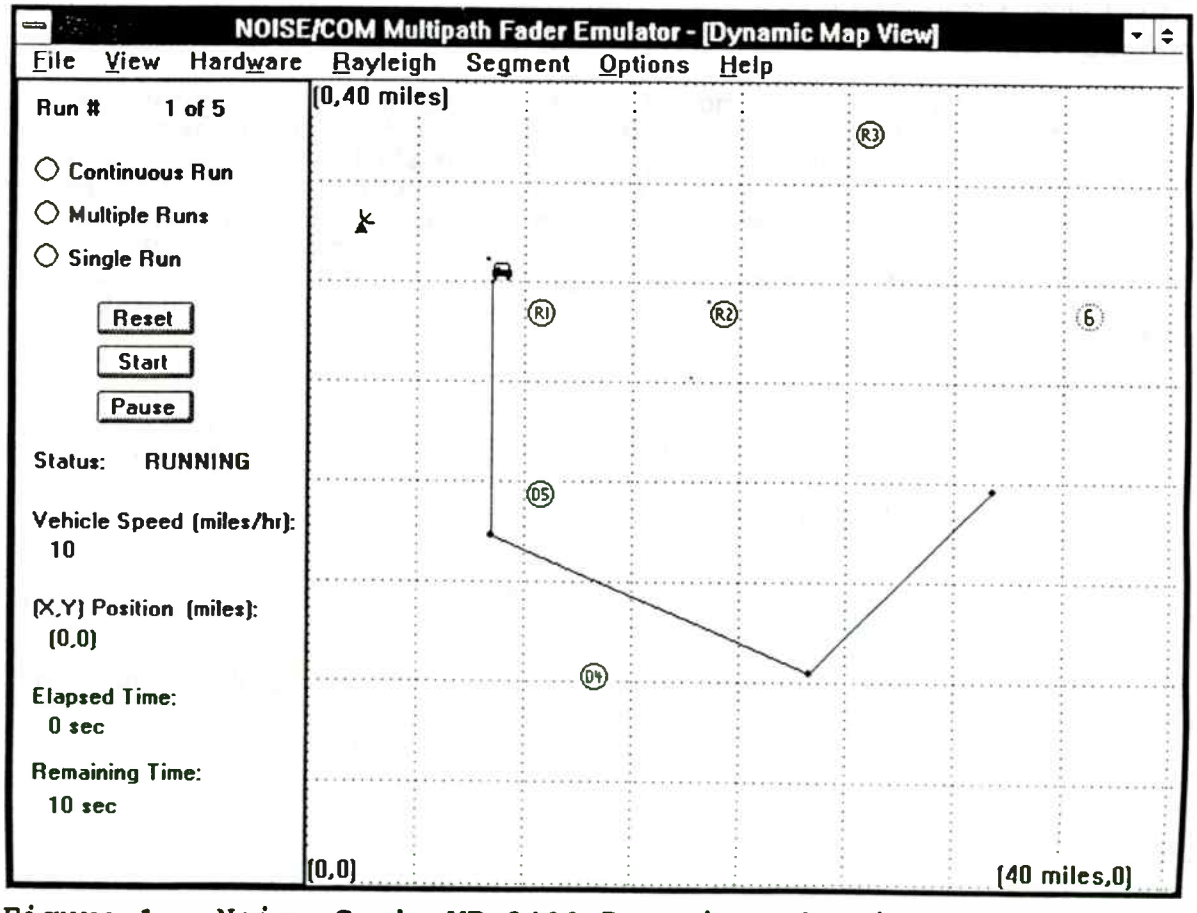


Figure 1. Noise Com's MP-2400 Dynamic Mode Display with Angle of Arrival in a Multipath Fading Scenario inserted.

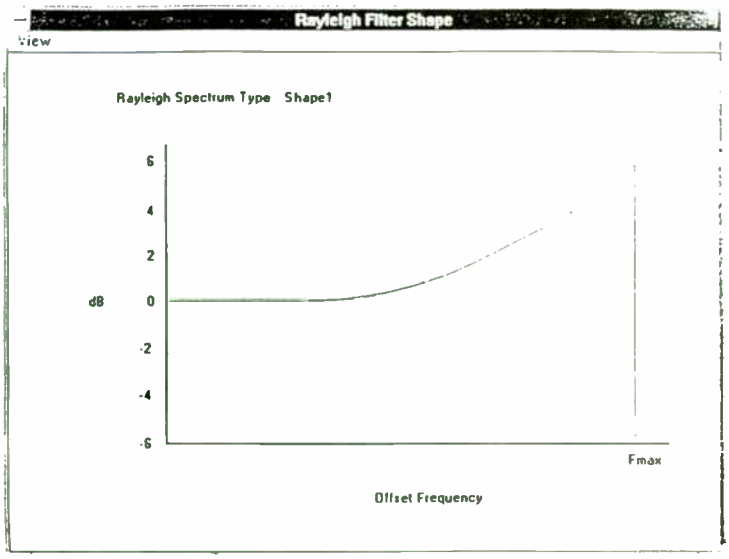


Figure 2.
MP-2400 Display of Doppler Spectrum for Omni-directional Antennas.

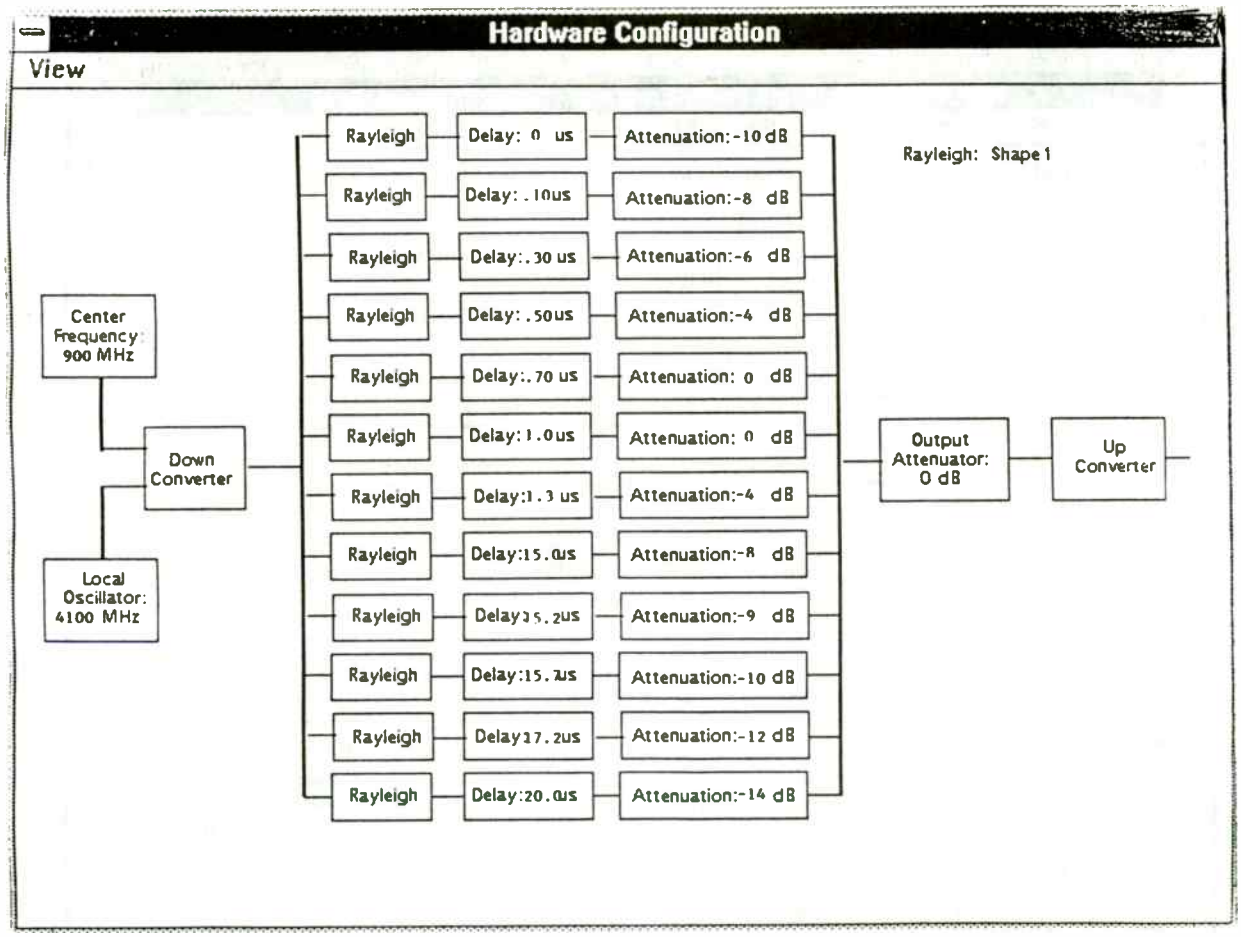


Figure 3. MP-2400 Display of Hardware Configuration.

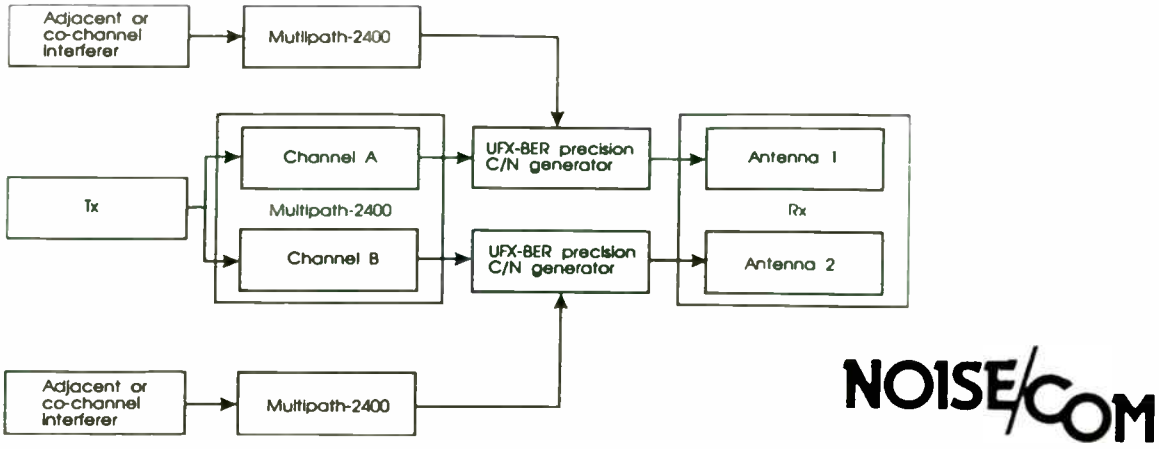


Figure 4. Diversity and Interference Test Using 2 MP-2400s Configured for 2 Channels with 6 Paths each.

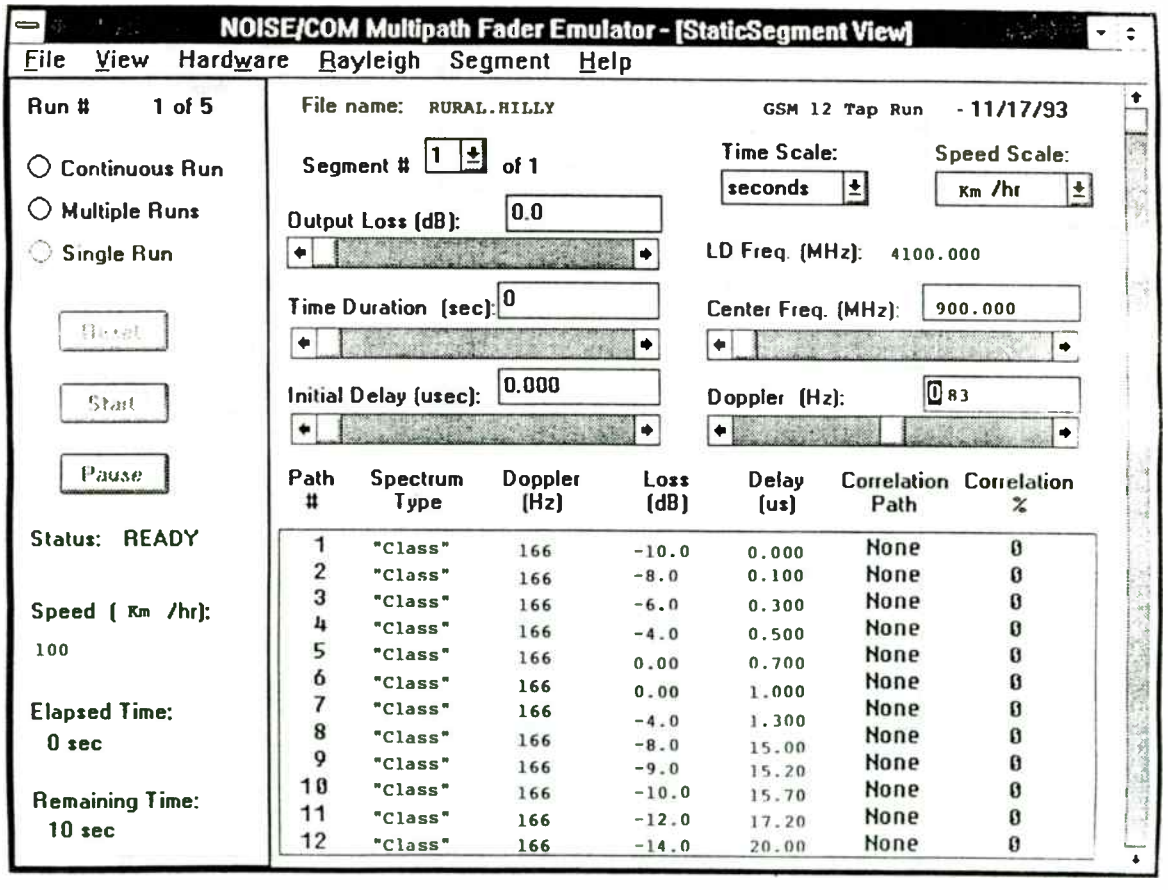


Figure 5. MP-2400 Multipath Fading Emulator, Display for Entry of Fading Path Parameters in Static Mode.

Evaluating Iridium Amplifiers with a New Noise Power Ratio Technique

R. McMorrow, Raytheon, S. Yates, Hewlett Packard

Abstract

A new approach to noise power ratio testing uses a digitally controlled stimulus to generate the signal instead of a noise source and filtering. This gives greater flexibility in the measurement setup and configuration. Repeatable results are easily obtained as the NPR signal's peak to average ratio and time domain waveform are clearly defined.

Introduction

Amplifier linearity and efficiency are both important in the characterization of Iridium amplifiers. These amplifiers need to operate under adverse conditions while obtaining maximum output power with low distortion. Noise power ratio(NPR) measurements are a good way to evaluate the amplifier performance when the real life signal includes multiple channels of information. NPR is a distortion measurement used to help determine the amplifier's maximum spurious free dynamic range. Another distortion measurement commonly used to determine amplifier linearity is the two tone test. For this application, two tone testing does not provide the randomly changing amplitude verses time waveform or the peak to average ratio needed to fully stress the DUT.

NPR testing requires a complex stimulus and a measurement receiver. The stimulus may be some combination of a broadband noise source, low pass filters, band pass filters, band reject filters, amplifiers, and upconverters. These components are combined to generate a band of noise with a notch missing at the frequency of interest. In the classical approach, the measurement receiver includes downconverters, attenuators, filters, and an average power meter at selective frequencies. The NPR measurement is made by taking the difference between the power levels at the notch frequency with and without the notch filter.

The technique used to evaluate the Iridium amplifiers is different from the classical NPR method. Instead of using a multitude of components to create the NPR signal, an arbitrary waveform synthesizer is used. This signal is developed mathematically, downloaded into memory, and clocked through a high speed digital to analog converter (DAC). This technique generates a repeatable, periodic noise signal that has a flat power spectrum with a random phase distribution. When the NPR signal is digitally generated, the noise and notch bandwidth, plus the flatness across the signal are easily controlled. The test

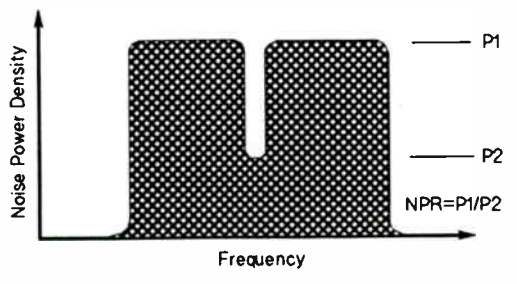


Figure 1. NPR Signal in the Frequency domain.

receiver used to make Iridium NPR measurements is a spectrum analyzer instead of an average power meter and a downconverter. The spectrum analyzer has much more flexibility in being able to measure at different frequencies. When making the NPR test with these two pieces of test equipment, the notched noise is measured and compared to the noise outside of the notch with the difference being the NPR. Figure 1 shows the NPR signal in the frequency domain. Amplifier measurements will show the validity of this new measurement technique.

Classical NPR Technique

The NPR test was first used by AT&T to measure distortion in telephone or voice telephony systems. This test methodology is better than traditional distortion tests as band limited white noise more closely approximates a fully loaded multichannel communications signal. The NPR signal can be modeled as a carrier with complex wideband AM and PM modulation. Since complex wide band AM and PM modulated signals have a larger peak to average time variation, the amplifier performance with the NPR signal will be different than with single or two tone stimuli. The DUT distortion can be determined by filling all but one of the system channels with noise and observing the level of noise in this unoccupied channel after the DUT. Third and fifth order intermodulation products generated by the DUT can be most easily observed in this unoccupied channel. The NPR is calculated as the power ratio of these distortion products to that of an equal, adjacent, channel which is filled with noise. Figure 2 illustrates this test signal as observed on a spectrum analyzer.

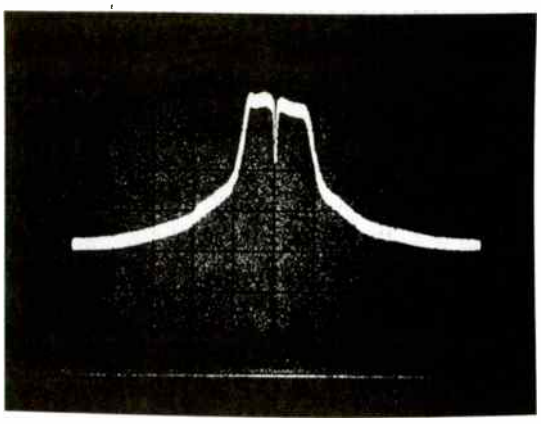


Figure 2. Classic NPR signal in the frequency domain.

The most common method for performing this measurement is identical to that originally used by AT&T. White noise is injected into a band-pass filter limiting the noise to the DUT bandwidth, followed by a notch filter creating the unoccupied channel. This signal feeds directly into the DUT. NPR is determined by using more filters and a power meter to measure the signal. By increasing the input noise level while monitoring the NPR, the onset of system saturation can be determined.

There are some common variations to this technique which add more flexibility to the measurement. The noise signal is generated at baseband or some intermediate frequency, then mixed with a variable local oscillator producing a range of frequencies. Now the band limited noise signal can be shifted in frequency to suit the needs of a particular DUT. Additional notch filters at different frequencies can be switched in to determine the NPR at different points in the system band. Another variation that adds flexibility is the use of a spectrum analyzer. A spectrum analyzer can be utilized without the cost of using

additional mixers to downconvert the notch frequency to a power meter. Also, automatic gain control(AGC) can be used to hold the total power in the noise bandwidth constant with and without the notch filter inserted. This way, both distorted power and transmitted power can be measured at the same frequency saving the cost of some filters.

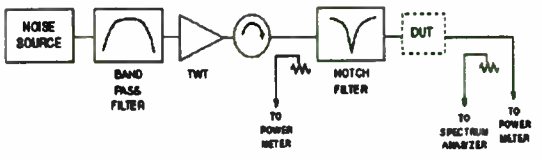


Figure 3. Classic NPR Block Diagram.

Figure 3 shows a measurement setup used to make an NPR measurement using this technique. A variable attenuator can be inserted before the DUT to sweep the input power while the NPR is measured using a spectrum analyzer. Figure 4 graphs NPR vs. input power and Figure 5 graphs Output power vs. Input power for a simple class AB amplifier at 1600 MHz.

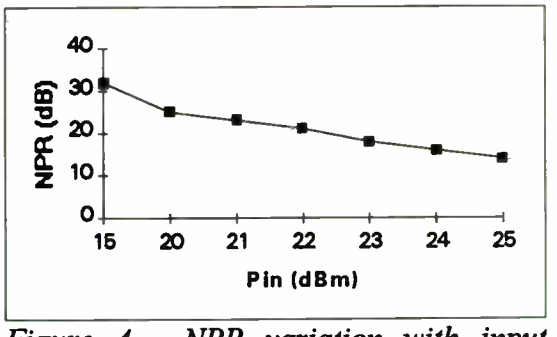


Figure 4. NPR variation with input power.

Digital NPR Technique

In the classic technique, the NPR signal is developed with noise generators, filters and frequency converters. To test the Iridium amplifiers, an arbitrary waveform synthesizer generates the NPR signal. The arbitrary waveform generator uses digital memories, a DAC, and upconversion to create the signal. Generating the noise signal digitally has many benefits when compared to the classical technique. These benefits include signal parameter flexibility and repeatability. The signals noise bandwidth and notch bandwidth are easily modified when digitally implemented instead of using discrete filters. Also, the flatness across the noise bandwidth in the frequency domain can be controlled to correct for any frequency response in the test system. The digital NPR signal is very repeatable as the

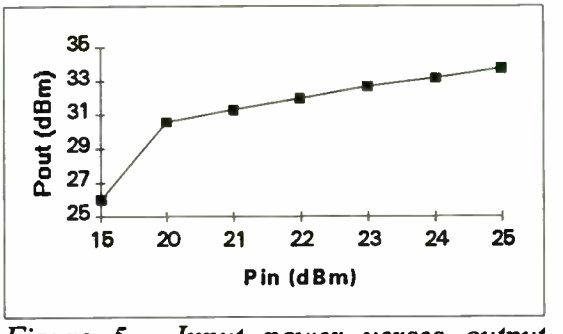


Figure 5. Input power verses output power.

magnitude and the phase are controlled by programming as opposed to being generated with a noise diode. However, there are some physical differences in this new NPR signal as compared to the classical signal. These differences are due to the digital and repetitive nature of the waveform generation. When testing the Iridium amplifiers, the digitally generated NPR signal allows for flexible setups and provides repeatable results.

The arbitrary waveform generator used to create the NPR signal is the HP 8791 Model 11. This arbitrary generator uses multiple memories driving a DAC through

a Sine computer as shown in Figure 6. The NPR signal is modeled as a carrier with AM and PM modulation, thus the AM, PM and FREQ memories are used to create the signal. These memories will allow for the entry of the magnitude, phase and carrier frequency of the NPR signal and will get clocked into the DAC at a 134 MHz rate. The analog output of the DAC is upconverted to 1.62 GHz with the agile upconverter and has a 40 MHz instantaneous bandwidth. This signal is now ready to test the Iridium amplifiers without the need for analog filters. Signal parameters can be varied by changing the values in the AM and PM memory which can have noise bandwidths from 100 KHz to 40 MHz and notch bandwidths from 4 KHz to 40 MHz.

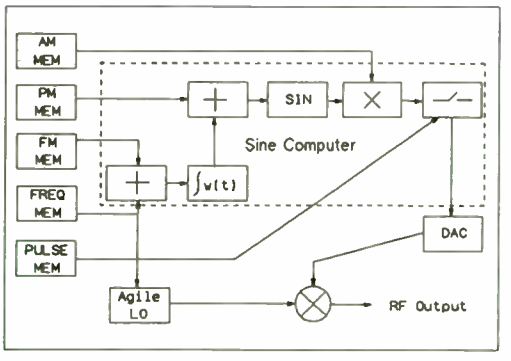


Figure 6. HP 8791 Block diagram.

The NPR signal used to test Iridium amplifiers is mathematically developed and downloaded into the memories driving the DAC. Since the waveform represents noise, an algorithm is used that allows the arbitrary waveform generator to simulate random noise. When deriving random noise, there are three characteristics that need to be satisfied. First, the power spectrum needs to be flat with frequency. Second, the ordinates (voltage vs. time) need to have a Gaussian distribution; and third, a zero auto correlation for all non zero time shifts. The first and second noise characteristics can easily be satisfied by creating the noise signal in the frequency domain. This is accomplished by creating a signal with constant amplitude verses frequency and random phase verses frequency over the bandwidth desired. The phase is uniformly distributed between -180 degrees and 180 degrees. Since the DAC needs to have the data in an amplitude verses time format, an inverse fourier transform is performed on this frequency domain noise signal. Then the time waveform is converted to a polar format and the magnitude and phase data is placed into the AM and PM memories. The AM and PM memories are combined in a Sine computer to create the amplitude verses time data. When generating the signal digitally, the output is periodic and the auto correlation is low for all time shifts except for multiples of the waveform period. The output noise signal is repetitive due to the finite memories driving the DAC. When the sequencer finishes clocking out the last memory location, in order to continuously output a signal, it returns the first memory location and clocks through the memory again. Playing the memory through the DAC multiple times creates a periodic nature to the waveform. This periodic nature in the time domain waveform causes the auto correlation function to be one for integral multiples of the sequence length. A periodic waveform in time will cause a sampled or discrete waveform in frequency. When using the HP 8791 Model 11 as the waveform generator, the memory length used to create the NPR signal is 64k bits. With a clock frequency of 134 MHz, the noise signal will repeat every 488 usec and will show up as discrete tones 2.048 KHz apart in the

frequency domain. For the Iridium amplifier, the non zero auto correlation function does not cause any significant measurement uncertainty as the frequency spacing of the tones is much smaller than the notch and noise bandwidths used in the testing.

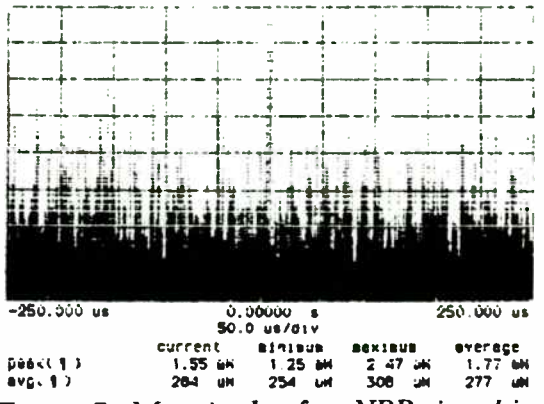


Figure 7. Magnitude of an NPR signal in the time domain.

The NPR signal is created in the frequency domain with closely spaced tones whose amplitude and phase are specified. In the time domain, the NPR signal has a largely varying signal amplitude with time as shown in Figure 7. The peak value is several dB larger than the average value. It is this peak to average ratio that stresses the amplifier and makes NPR a better test for communication systems as compared to two tone testing. The peak to average ratio is determined by the phase distribution of the tones. When the NPR signal is digitally derived, the peak to average ratio can be controlled, since the magnitude and phase of each tone is controlled. This makes the technique repeatable when compared to a noise source where the peak to average ratio is random.

The test setup for the Iridium amplifiers is shown in Figure 8. In this setup, the arbitrary waveform generator is creating an NPR signal with a 3 dB noise bandwidth of 10.5 MHz and a 3 dB notch bandwidth of 0.2 MHz. This signal drives a linear amplifier to produce the proper output power. The test receiver is a spectrum analyzer. The spectrum analyzer measures the signal level in the notch, the signal level outside of the notch; and the ratio of these two measurements is the NPR. Figure 9 shows the measurement as seen on a spectrum analyzer. The NPR measurement is made at several input power levels to determine when system saturation occurs and the relative linearity of the DUT.

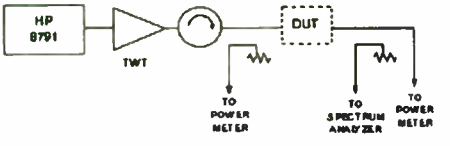


Figure 8. Digital NPR Block Diagram.

NPR Measurement Receiver

The NPR measurement receiver for the Iridium amplifier under test is a spectrum analyzer. A spectrum analyzer is a frequency selective, peak responding

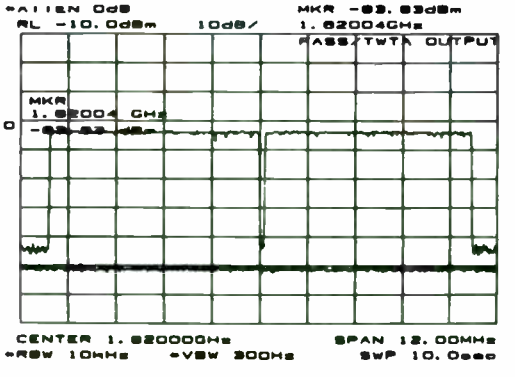


Figure 9. Digital NPR signal as shown on a spectrum analyzer.

voltmeter calibrated to display the RMS value for a sine wave. This swept tuned super heterodyne receiver has many advantages over the traditional technique employing fixed tuned receivers. Since the spectrum analyzer is swept tuned, the entire NPR waveform can be displayed at one time. The notch depth can be observed directly and measured. Only one signal is needed to measure NPR, unlike the traditional technique that may require two noise waveforms, one with and one without a notch. The NPR measurement is made with the spectrum analyzer by making a measurement inside the notch and a measurement outside of the notch and taking the ratio.

When measuring the NPR signal with a spectrum analyzer there are several considerations that need to be addressed for accurate results. First, it is desirable to have the input signal's NPR at least 10 dB lower than the amplifier under test NPR. This insures the test signals effect is negligible when measuring the DUT's NPR. Any nonlinear device before the DUT (preamplifiers, frequency converters, etc.) will introduce distortion and cause the input signals NPR to rise. A second consideration requires keeping the spectrum analyzer out of compression and within its linear measurement range. Even though each tone has a limited amplitude, the total average power in the NPR signal is the sum of all the tones and can easily compress the spectrum analyzer input. The NPR signal will also compress the spectrum analyzer with the large instantaneous time domain peaks. The compression can be checked by varying the spectrum analyzer's input attenuator while verifying that the displayed signal level does not change. If it changes, then the spectrum analyzer's input section is in compression and the input attenuator needs to be increased for accurate results. A third consideration has to do with the way that the spectrum analyzer measures noise. Since the spectrum analyzer is calibrated to measure sinusoids, correction factors are needed when measuring noise. This is true only when measuring the absolute power levels of a noise signal. Since the NPR signal is a ratio of two noise measurements, no correction factor is needed.

The spectrum analyzer set up is also crucial for accurate and repeatable results. In order to make these measurements, the proper resolution bandwidth (RBW) and video bandwidth (VBW) need to be chosen. When the NPR signal is digitally generated, the signal is made up of individual tones and the RBW needs to be at least 2 times the NPR signal tone spacing. This will ensure the spectrum analyzer will not resolve the individual tones and the signal will appear noise like.

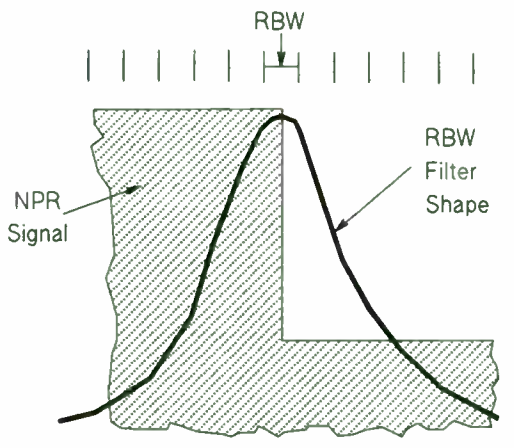


Figure 10. RBW affects on the NPR notch edge.

While in the traditional method, the RBW should be much less than the notch bandwidth for accurate depth measurements. The VBW needs to be

chosen to be at least 1/100 of the RBW to obtain the average for this noise signal. The power measurements both inside and outside of the notch need to be average power measurements. In the digital technique, the average power is obtained for the notch bandwidth by integrating the total power across a notch bandwidth and dividing by the bandwidth. While in the classic technique, proper VBW selection is only required to get the average power. When tabulating the average power, it is necessary to make sure that the RBW filter response is not affecting the results. The RBW filter response makes the inside of the notch appear narrower than actual. This error shows up as an elevated average power in the notch. For accurate results, the power measurements must be taken at least 5 RBWs away from the notch edge for minimal effect from the RBW filter response. The same bandwidth used to measure in the notch is used to measure outside of the notch. The average power measurement outside of the notch also needs to be at least 5 RBW bandwidths away from the notch edge. If power measurements are made close to the notch edge, reduced average power levels may be obtained. Figure 10 illustrates how the RBW filter response affects the measurements. The spectrum analyzer setup for RBW, VBW, input attenuator, and measurement placement of the NPR signal is crucial for accurate and repeatable measurements.

Comparison

Figure 11 shows the NPR vs. Input power results on the class AB amplifier for both measurement techniques. Since the classical NPR measurements were performed with a 3 dB noise bandwidth of 50 MHz and the digital NPR

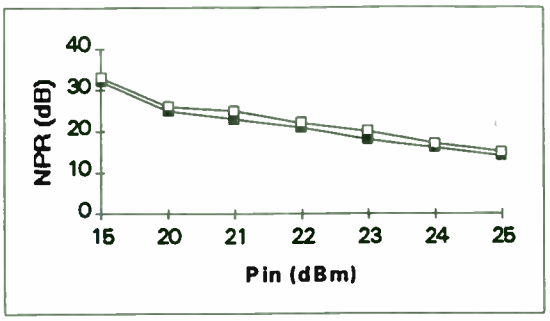


Figure 11. NPR comparison for both the Classic and Digital techniques.

measurements with a 3 dB noise bandwidth of 10.5 MHz, some variation can be expected. However, there is excellent correlation between the two curves. The only significant error is a 1 dB offset between the digital and classical techniques. This is attributable to round off error in the measurement. The software used in the digital measurement system returns a real number for the NPR which is rounded to an integer. For the classical measurement, the NPR was manually observed as the difference in levels on the spectrum analyzer. The possible errors involved with this made it desirable to always round down to the worst case NPR. This difference in the measurement techniques along with the change in total noise bandwidth easily explains the small difference in the results.

Since this new method for NPR testing produces equivalent results, a more detailed comparison of the advantages and disadvantages should be examined. Flexibility has already been mentioned as an advantage of the digital technique. In addition to making the notch size, position, and signal bandwidth variable, frequency shaping across the band is possible. This can be used to compensate for the effect of any frequency sensitive components in the test setup. This is in

direct contrast to the analog technique where a filter's ripple or slope will be propagated when generating the signal. In the analog method, the noise bandwidth minimum size can be a limitation. This is limited by the notch filter design as the analog filter bandwidth can only be so small, and the noise bandwidth must always be much greater than the notch bandwidth. The practical lower limit at L band was about 10 MHz for the total noise bandwidth. On the other hand, the digital technique has a much smaller lower limit but has a maximum noise bandwidth limitation of 40 MHz. In comparing measurement speed, averaging can be done faster with the digital technique as the waveform period is known compared to the traditional technique where the period is infinite. The digital NPR technique offers more flexibility, faster results and gives equivalent results to the classical technique.

Conclusion

Noise power ratio measurements with a digitally controlled stimulus give accurate and comparable results to the classical technique. With a digitally controlled stimulus, the NPR waveform is repeatable as the magnitude and phase of the signal is digitally developed. It is also easy to change the signal characteristics by changing the data stored in the memories of the arbitrary waveform synthesizer. These attributes makes this technique easier and more repeatable than the classic technique.

Acknowledgments

The authors thank Dave Upton from Raytheon, and Dave Koberstein from Hewlett Packard, for their insightful discussions on this topic.

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2. Hewlett-Packard Product Note 8791-3, Theory of Operation for the HP 8791 Models 7/10/11/21 Frequency Agile Signal Simulator. 1992.

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4. The White Noise Book, Multichannel Communication Systems and White Noise Testing. M. J. Tant. Marconi Instruments Limited. July 1974.

Trends, formats, and testing of digital cellular

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This paper will address current trends in digital cellular and personal communications services (PCS),, help in the understanding of many of the digital cellular formats in existence today, and explore high-speed, high-accuracy test methods. The status of TDMA, CDMA, digital cellular, and PCS around the world will be discussed. An overview of the parameters of NADC, CDMA, GSM, PDC, PHP, etc., will be presented. Finally, high-speed, high-accuracy, multiformat testing will be described.

Cellular Design

Session Chairperson: David L. Sprague,
InMark—Independent Marketing Corporation (Walnut Creek, CA)

Concepts of CDMA

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Abstract:

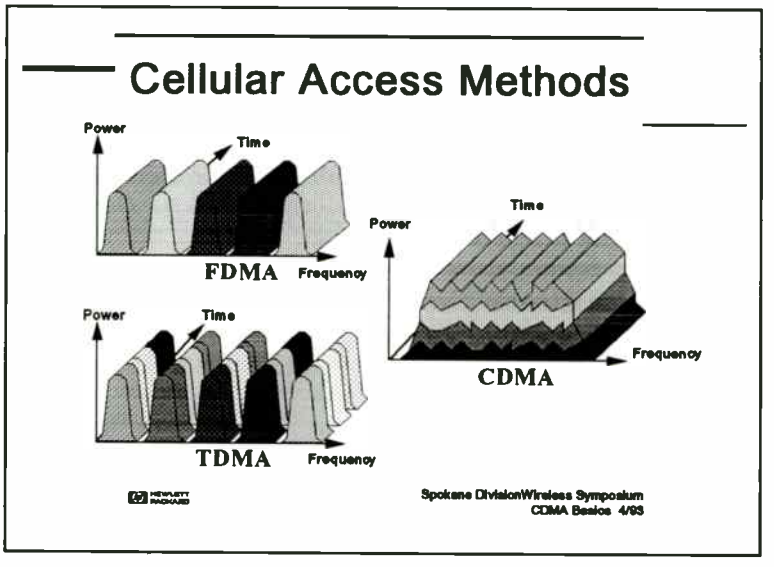
This presentation gives an overview of the proposed CDMA cellular system defined by the TIA 45.5 sub-committee. This system is largely based on the CDMA system developed by Qualcomm. The intent of this paper is to provide insight into the technology of CDMA and to describe some of the operating features of the proposed TIA CDMA system.

Author Biography:

KEN THOMPSON is a Product Marketing Engineer at Spokane Division of Hewlett-Packard. He received his BSEE in 1983 from Brigham Young University and joined Hewlett-Packard in the same year. Ken has helped develop several software products including the HP 11836A 0.3 GSMK modulation measurements software and HP 11847A $\pi/4$ DQPSK modulation measurement software. He has recently been involved in the introduction of the HP 8922 family of GSM one-box measurement products and the HP 8921D TDMA dual-mode cell site test system.

Objectives: This presentation gives an overview of the proposed CDMA cellular system defined by the TIA 45.5 sub-committee. This system is largely based on the CDMA system developed by Qualcomm. The intent of this paper is to provide insight into the technology of CDMA and to describe some of the operating features of the proposed TIA CDMA system.

Slide #1



The Problem of Access: The personal communication industry is faced with the problem of an ever increasing number of users sharing the same limited frequency bands. To expand the user base, the industry must find methods to increase capacity without degrading the quality of service.

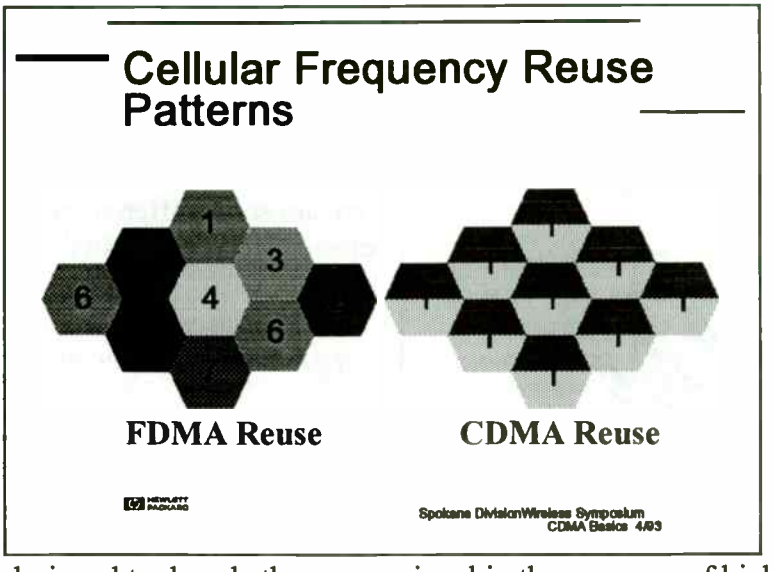
The current analog cellular system uses a complex system of channelization with 30 kHz channels, commonly called FDMA (Frequency Division Multiple Access). To maximize capacity, FDMA cellular uses directive antennas (cell sectoring) and complex frequency reuse planning.

To further increase system capacity, a digital access method is being implemented called TDMA (Time Division Multiple Access). This system uses the same frequency channelization and reuse as FDMA analog and adds a time sharing element. Each channel is shared in time by three users to effectively triple system capacity.

CDMA stands for Code Division Multiple Access and uses correlative codes to distinguish one user from another. Frequency divisions are still used, but in a much larger bandwidth (1.25 MHz). In CDMA, a single user's channel consists of a specific frequency combined with a unique code. CDMA also uses sectored cells to increase capacity. One of the major differences in access is that any CDMA frequency can be used in all sectors of all cells.

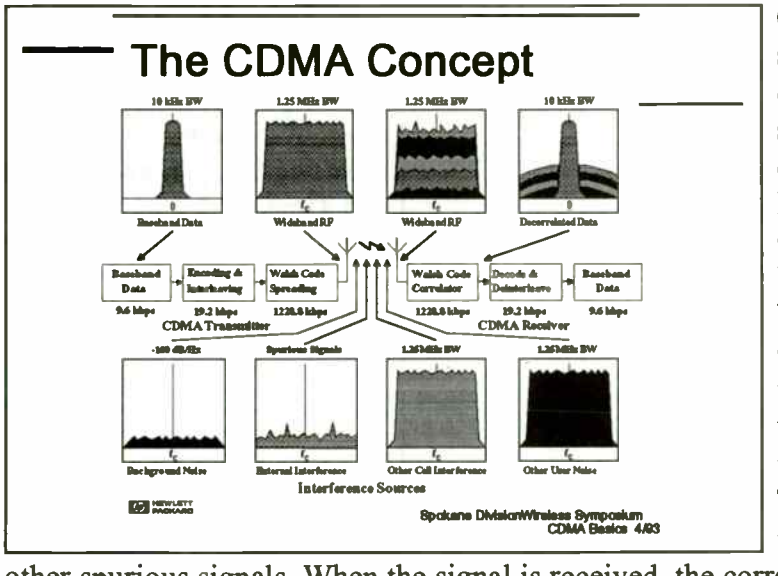
The correlative codes allow each user to operate in the presence of substantial interference. An analogy to this is a crowded cocktail party. Many people are talking at the same time, but you are able to understand one person at a time. This is because your brain can sort out the voice characteristics and differentiate them from the other talkers. As the party grows larger, each person has to talk louder, and the size of the talk zone grows smaller. This would be more dramatic if each conversation were in a different language. CDMA is similar, but the recognition is based on the code. The interference is the sum of all other users on the same CDMA frequency, both from within and without the home cell and from delayed versions of these signals. It also includes the usual thermal noise and atmospheric disturbances. Delayed signals caused by multipath are separately received and combined in CDMA. This will be discussed in greater detail later in this presentation.

Slide #2



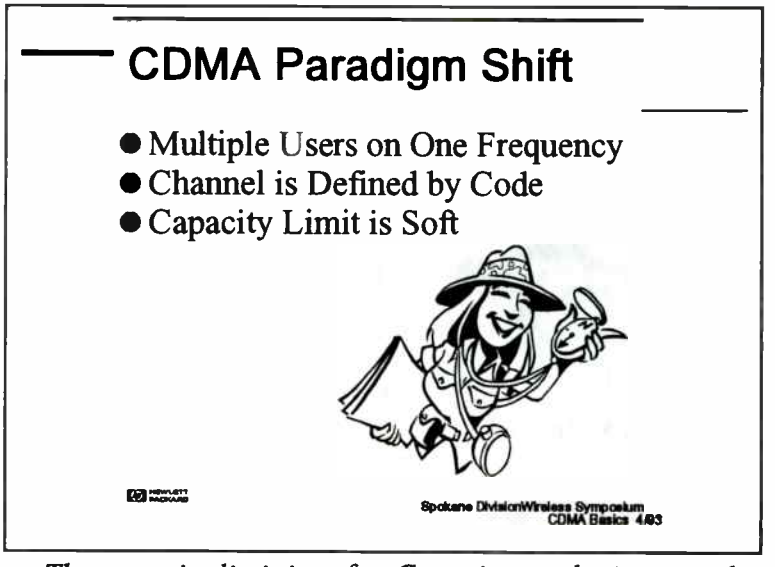
One of the major capacity gains with CDMA is because of its frequency reuse patterns. The normal reuse pattern for analog and TDMA systems employs only one seventh of the available frequencies in any given cell. This could really be called frequency non-reuse. With CDMA, the same frequencies are used in all cells. If using sectored cells, the same frequencies can be used in all sectors of all cells. This is possible because CDMA is designed to decode the proper signal in the presence of high interference.

Slide #3



CDMA starts with a narrowband signal, shown here at the full data rate of 9600 bps. This is spread with the use of specialized codes to a bandwidth of 1.23 MHz. When transmitted, a CDMA signal experiences high levels of interference, dominated by the coded signals of other CDMA users. This takes two forms, interference from other users in the same cell and interference from adjacent cells. The total interference also includes background noise and other spurious signals. When the signal is received, the correlator recovers the desired signal and rejects the interference. The is possible because the interference sources are uncorrelated to the desired signal.

Slide #4

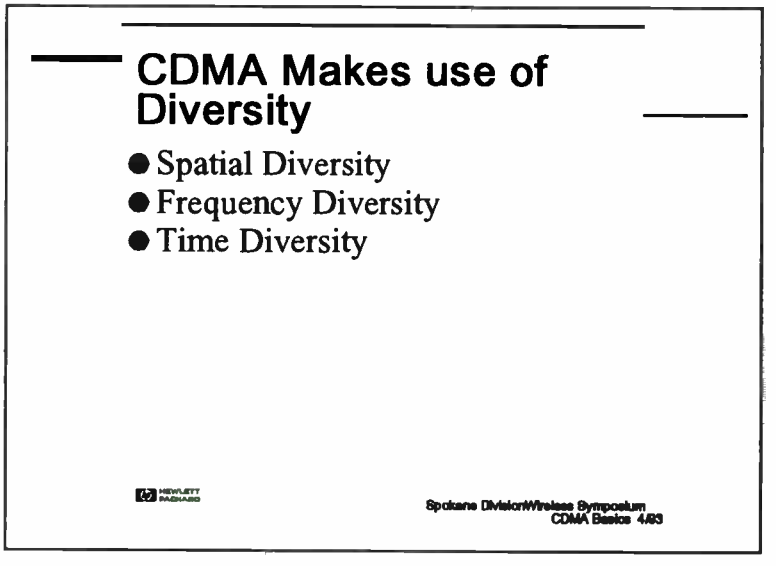


For most people familiar with FM communication systems, a paradigm shift is needed to properly discuss CDMA.

Here are some differences between CDMA and analog FM:

- *Multiple users are on one frequency simultaneously*
- *A Channel is defined by the correlative code in addition to the frequency*
- *The capacity limit is soft. Capacity can be increased with some degradation of the error rate or voice quality.*

Slide #5



Another aspect of CDMA is diversity. CDMA uses three types of diversity: Spatial diversity, Frequency diversity, and Time diversity.

Slide #6

CDMA Spatial Diversity

- Multiple Antennas at Base Station
- Multiple Base Stations for Soft Handoff

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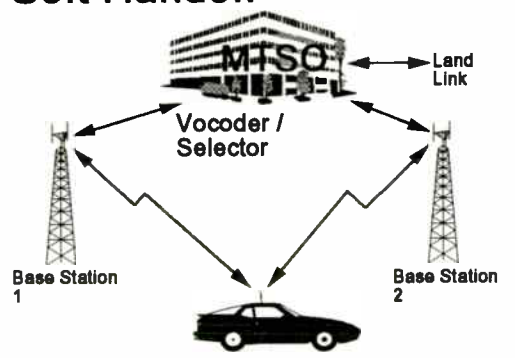
Spatial diversity takes two forms:

- *Two antennas: The base station uses two receive antennas for greater immunity to fading. This is the classical version of spatial diversity.*
- *Multiple base stations simultaneously talk to the mobile during soft handoff.*

Slide #7

Spatial Diversity During Soft Handoff



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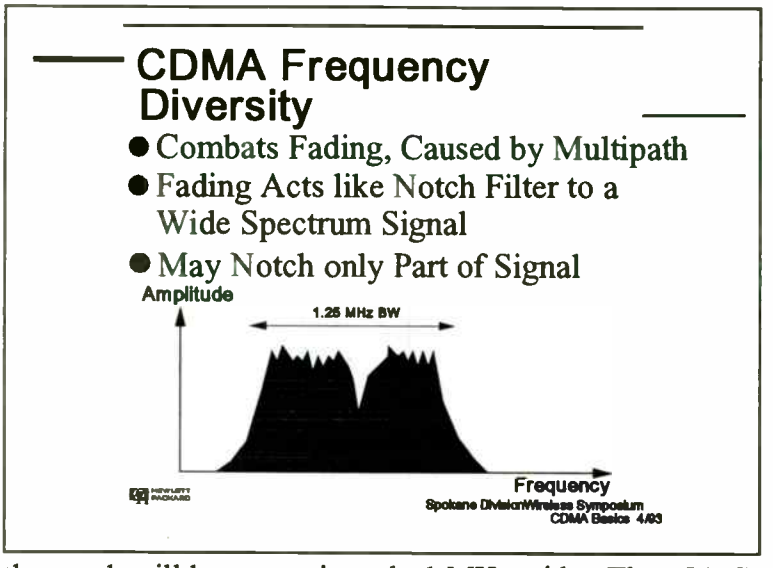
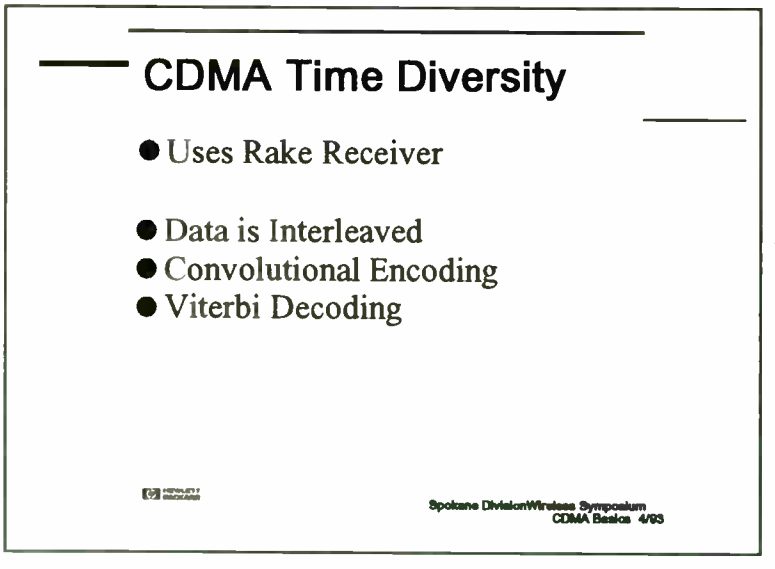
During Soft Hand-off, contact is made with two base stations simultaneously. The signals from the base to mobile are treated as multipath signals and are coherently combined at the mobile unit. At the base stations, the signals are transmitted via the network to the Mobile Telephone Switching Office (MTSO), where a quality decision is made on a frame-by-frame basis, every 20 msec.

Slide #8



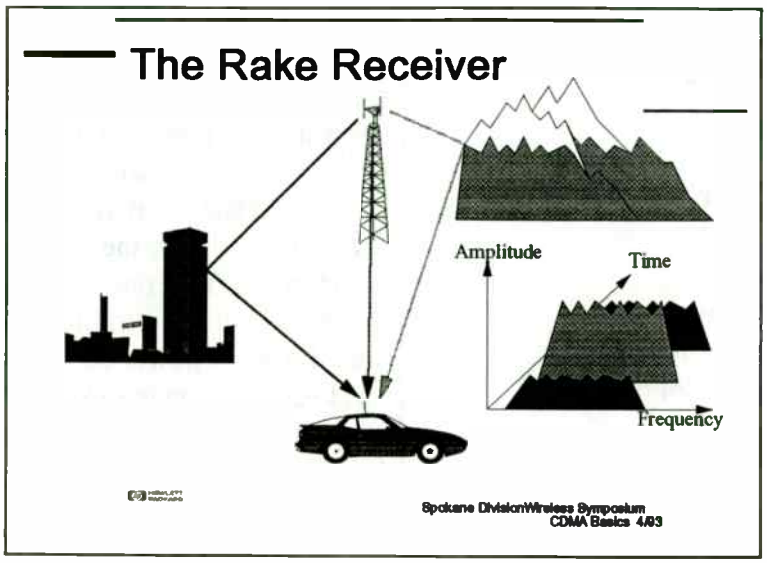
Frequency diversity is inherent in spread spectrum systems. A fade of the signal is less likely than with narrow band systems. Fading is caused by multipath and is a function of the time delays in the alternate paths. In the frequency domain, a fade appears as a notch filter that moves across a band. As the user moves, the frequency of the notch changes. The width of the notch is on the order of one over the difference in arrival time of two signals. For a 1 μsec delay, the notch will be approximately 1 MHz wide. The TIA CDMA system uses a 1.25 MHz bandwidth, so only those multipaths of time less than 1 μsec actually cause the signal to experience a deep fade. In many environments, the multipath signals will arrive at the receiver after a much longer delay. This means that only a narrow portion of the signal is lost. In the display shown, the fade is 200 to 300 kHz wide. This results in a power loss to a CDMA signal, but could result in a the complete loss of an analog or TDMA signal.

Slide #9



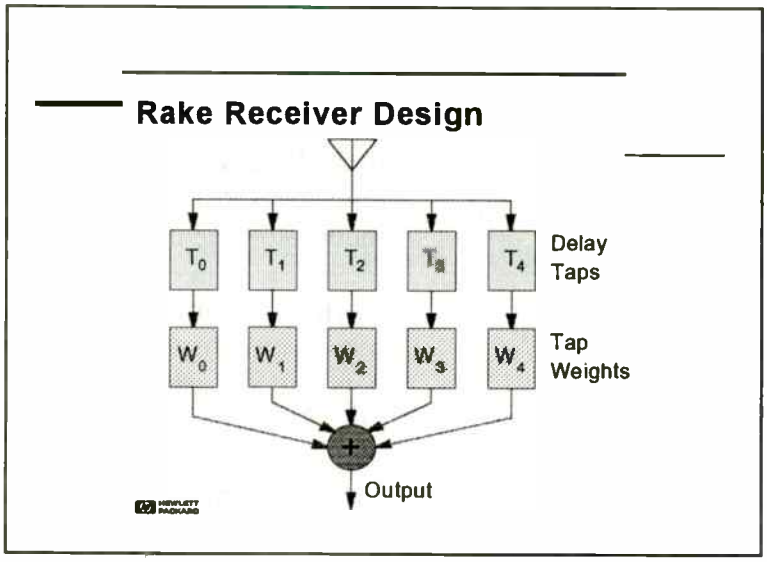
Time diversity is a technique common to most digital transmission systems. Signals are spread in time by use of interleaving. Forward error correction is applied, along with maximal likelihood detection. The particular scheme used for CDMA is convolutional encoding in the transmitter with Viterbi decoding using soft decision points in the receiver.

Slide #10



CDMA takes advantage of the multipath by using multiple receivers and assigning them to the strongest signals. The mobile receiver uses three receiving elements, and the base station uses four. This multiple correlator system is called a rake receiver. In addition to the separate correlators, searchers are also used to look for alternate multipaths and for neighboring base station signals.

Slide #11



This slide shows a conceptual block diagram of how a rake receiver works. The RF signal from the antenna is fed to a system of taps with each tap having a different delay (T_0, T_1, T_2, T_3, T_4). Any signal that matches the delay in a tap is passed on to a weighting function that scales the signal to correct for amplitude errors. After scaling, each tap is summed together to create a stronger version that more closely matches the original RF signal.

Slide #12

CDMA Reverse Link Power Control

- All Mobiles are Received at Base Station at Equal Power
- Two Types of Control
  - Open Loop Power Control
  - Closed Loop Power Control

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Power Control: One of the fundamental enabling technologies of CDMA is power control. The power of all mobile units is controlled so as to arrive at the base station at an equal level. In this way, the interference from one unit to another is held to a minimum. Two forms of power control are used for the reverse link: open loop power control, and closed loop power control.

Slide #13

Open Loop Power Control

- Assumes Loss is Similar on Forward and Reverse Paths.
- Receive Power+Transmit Power = -73
  - All powers in dBm
- Example:
  - For a Received Power of -85 dBm

    Transmit Power = (-73) - (-85)

    Transmit Power = +12 dBm

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Open loop power control is based on the similarity of the loss in the forward path to the loss in the reverse path (forward refers to the base-to-mobile link, while reverse refers to the mobile-to-base link).

Open loop control sets the sum of transmit power and receive power to a constant, nominally -73, if both powers are in dBm. A reduction in signal level at the receive antenna will result in an increase in signal power from the transmitter. For example, assume the received power from the base station is -85 dBm. This is composite signal from the base station. The open loop transmit power setting would be +12 dBm.

Slide #14

Closed Loop Power Control

- Directed by Base Station
- Updated Every 1.25 msec
- 1 dB Step Size
- Corrects Open Loop Power Estimate

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Closed loop power control is used to allow the power from the mobile unit to deviate from the nominal as set by open loop control. This is done with a form of delta modulator. The base station monitors the power received from each mobile station and commands the mobile to either raise power or lower power by a fixed step of 1 dB. This process is repeated 800 times per second, or every 1.25 msec.

Because the power of the mobile is controlled to be no more than is needed to maintain the link at the base station, much less power is typically transmitted from the mobiles than is the case with analog. The analog radio needs to transmit enough power to maintain a link even in the presence of a fade. Most of the time it is transmitting with excess power. The CDMA radio is controlled in real time and is kept at low power. This has the benefit of longer battery life and smaller, lower cost amplifier design. If recent health concerns over cellular phone radiation are founded, CDMA will be preferred.

Slide #15

CDMA Variable Rate Speech Coder

- 20 Millisecond Blocks of Speech
- Full Data Rate of 9600 bps
- Lowest Rate (1/8) of 1200 bps
- Mobile Transmits in Bursts of 1.25 msec
- Base Repeats Bits and Lowers Power
- System Capacity Increases by 1/Voice Activity Factor

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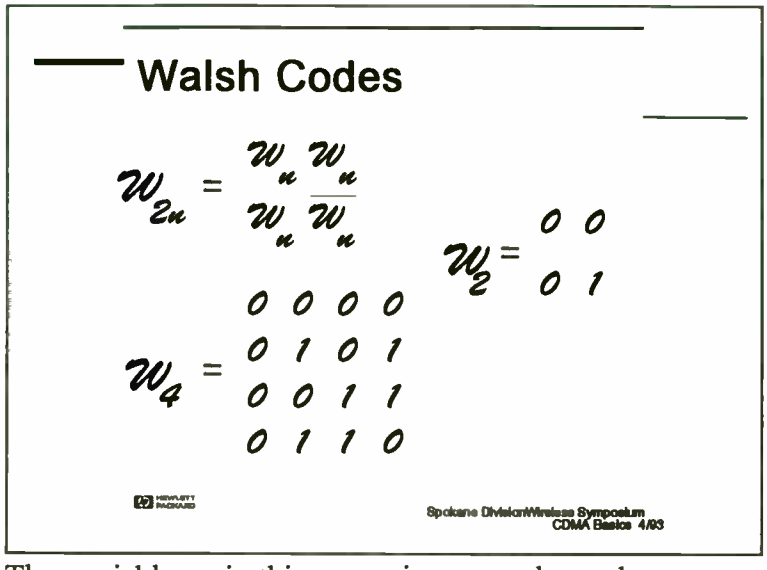
CDMA takes advantage of quiet times during speech to raise capacity. A variable rate vocoder is used; the channel is at 9600 bps when the user is talking. When the user pauses, or is listening, the data rate drops to only 1200 bps. 2400 and 4800 bps are also used, though not as often as the other two. The data rate is based on speech activity and a decision as to the appropriate rate is made every 20 msec. Normal telephone speech has approximately a 40% activity factor.

The mobile station lowers its data rate by turning off its transmitter when the vocoder is operating at less than 9600 bps. At 1200 bps, the duty cycle is only 1/8 that of the full data rate. The choice of time for this duty cycling is stochastic, so the power is lowered at all times when averaged over many users. Lowering the transmit power at the mobile reduces the level of interference for all other users.

The base station uses a slightly different scheme. It repeats the same bit patterns as many times as needed to get back to the full rate of 9600 bps. The transmit power for that channel is adjusted to reflect this repetition which allows the interference to be minimized. Repeating the bits at lower power is more effective on the forward link than it could be on the reverse link due to the use of a coherent phase reference called the pilot signal.

Slide #16



An important feature of the forward link is the use of Walsh codes. These have the characteristic of being orthogonal to each other and to the logical NOT of each other. Two codes are defined to be orthogonal if they have an exact zero cross product when summed over the full period of the codes. Walsh codes are generated by the expansion shown below:

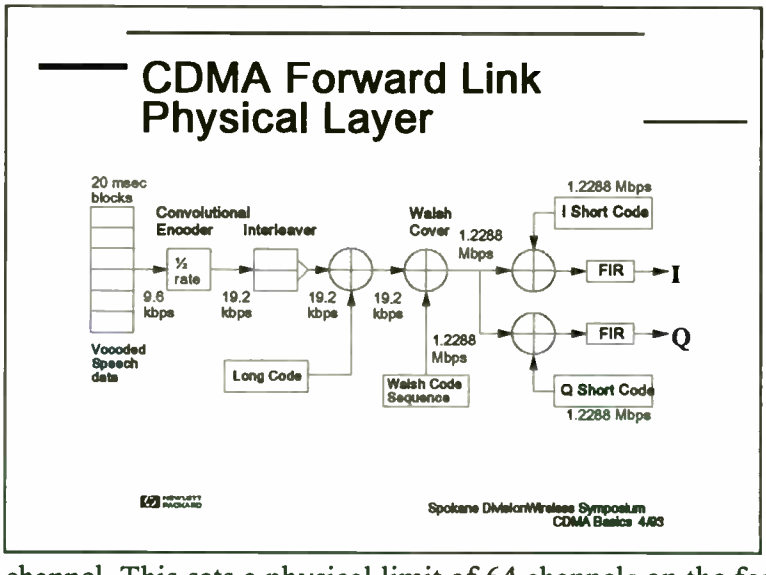
$$W_{2n} = \begin{matrix} W_n & W_n \\ W_n & \overline{W_n} \end{matrix}$$

The variable, n, in this expansion must always be a power of two. This is seeded with the one by one matrix:

$$W_1 = 0$$

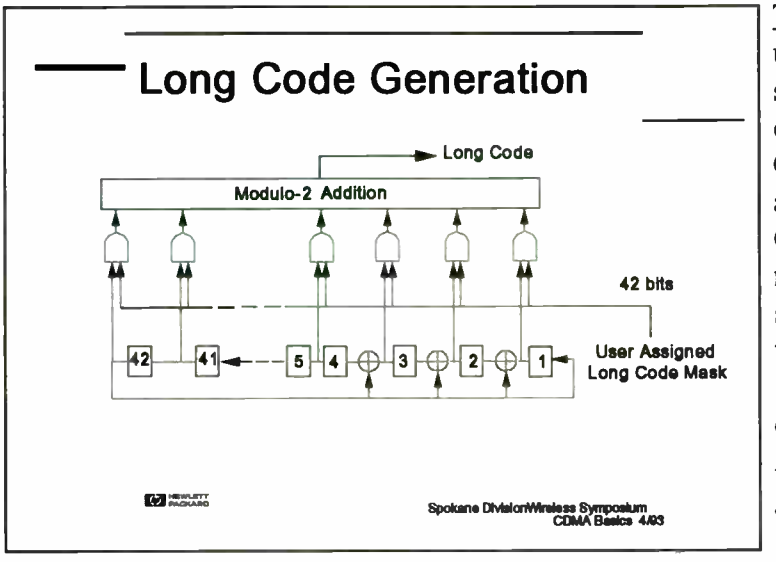
The TIA CDMA system uses a 64 by 64 Walsh matrix (each Walsh code is 64 bits long).

Slide #17



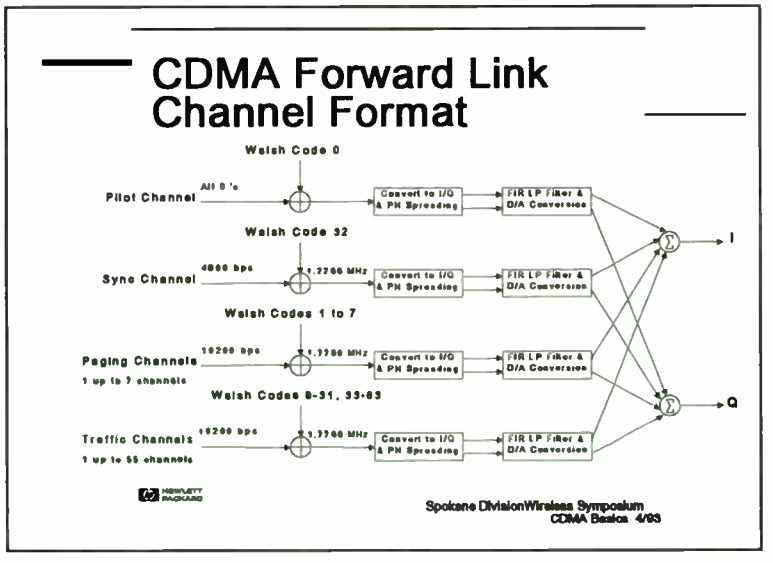
Voice data at 9600 bps (full rate) is first passed through a convolutional encoder, which doubles the data rate. It is then interleaved, a process that has no effect on the rate, but does introduce time delays in the final reconstruction of the signal. A long code is XOR'ed with the data, which is a voice privacy function and not needed for channelization. CDMA then applies a 64 bit Walsh code which is uniquely assigned to a base to mobile link to form one channel. This sets a physical limit of 64 channels on the forward link. If the coded voice data is a zero, the Walsh sequence is output; if the data is a one, the logical not of the Walsh code is sent. The Walsh coding yields a data rate increase of 64 times. The data is then split into I and Q channels, and spread with short codes. The final signals are passed through a low pass filter, and eventually sent to an I/Q modulator.

Slide #18



The Long Code is generated using a 42 bit linear feedback shift register. This is the master clock and is synchronized in all CDMA radios. To synchronize all of the base stations in the CDMA system, GPS satellite receivers are used. CDMA system time is the same as GPS time which started on March 6, 1980. The long code generator is driven by the system time clock. A specific mask is applied to generate a unique long code.

Slide #19



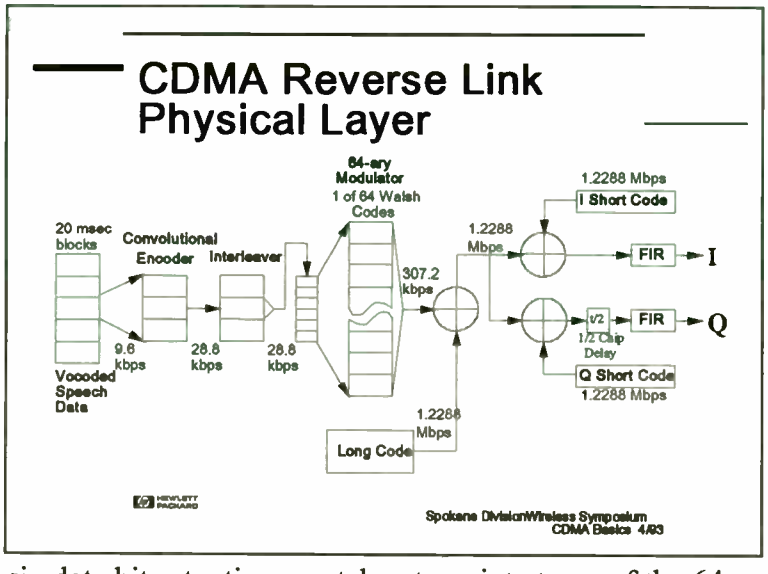
The Base Station transmitter signal is the composite of many channels (with a minimum of four). The Pilot channel is unmodulated; it consists of only the final spreading sequence (short sequences). The Pilot Channel is used by all mobiles linked to a cell as a coherent phase reference. The other three channels are the Sync channel, the Paging channel, and the Traffic Channel which use the same data flow, but different data are sent on these channels.

The Sync channel transmits time of day information. This allows the mobile and the base to align clocks which form the basis of the codes that are needed by both to make a link.

The Paging channel is the digital control channel for the forward link. Its complement is the access channel which is the reverse link control channel. One base station can have multiple paging channels and access channels if needed.

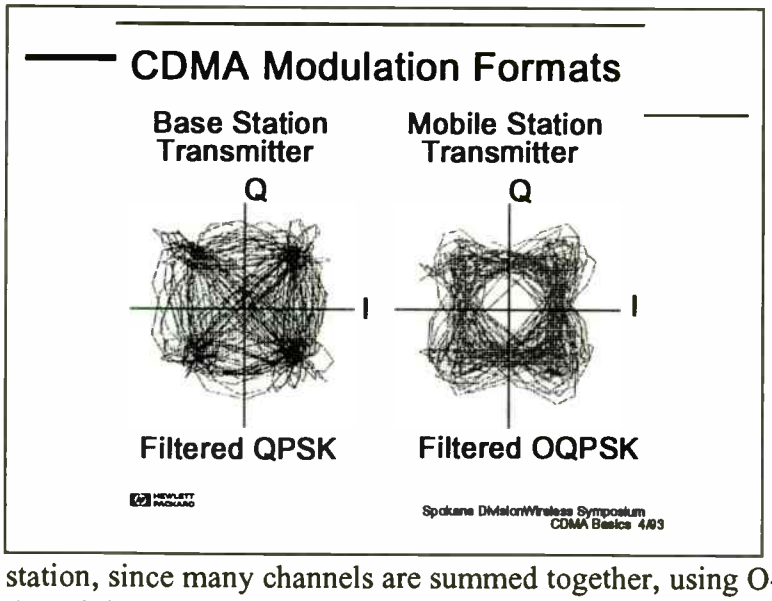
The Traffic channel is equivalent to the analog voice channel. This is where the actual conversations take place.

Slide #20



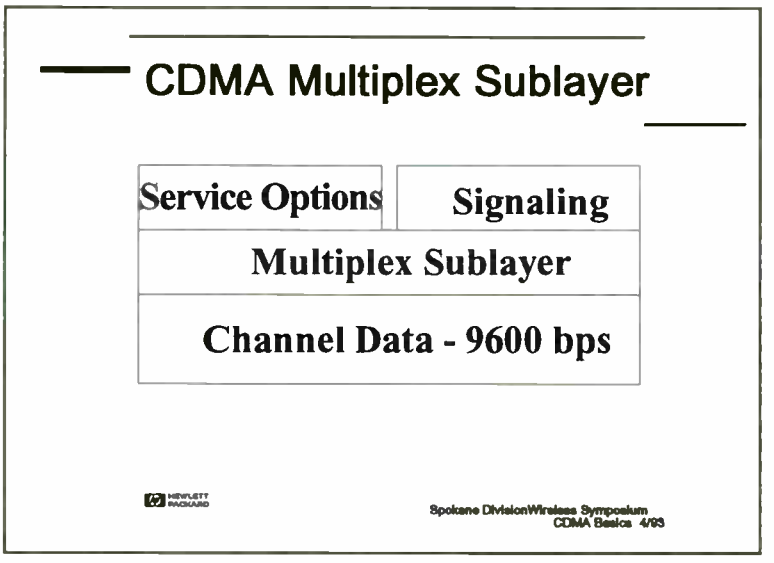
The CDMA reverse link uses a different coding scheme to transmit data. Unlike the forward link, the reverse link cannot support a pilot channel for synchronous demodulation (since each mobile station would need its own pilot channel). Due to this limitation, the reverse link has less capacity than the forward link. To aid reverse link performance, the 9600 bps voice data uses a one-third rate convolutional coded for more powerful error correction. Then six data bits at a time are taken to point at one of the 64 available Walsh codes. The data which is at 307.2 kbps is then XOR'ed with the long code to reach the full 1.2288 Mbps data rate. This unique long code is the channelization for the reverse link.

Slide #21



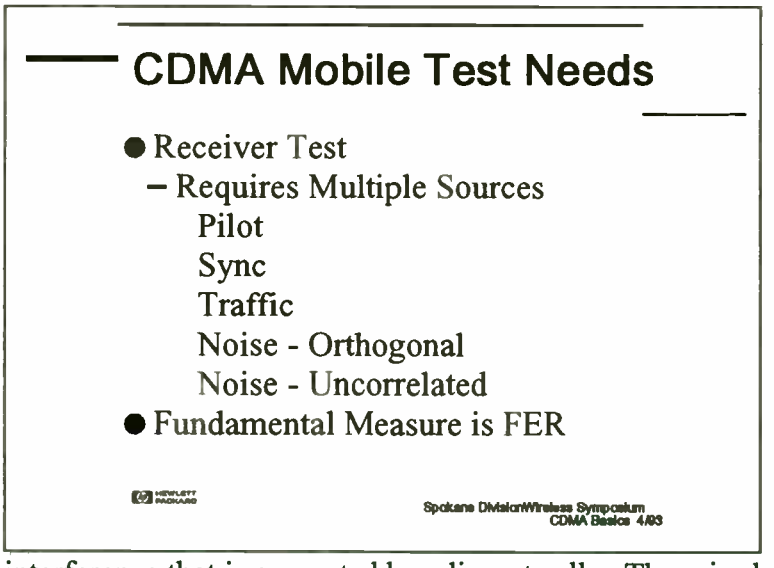
The modulation is Filtered QPSK in the base station, and Filtered Offset QPSK in the mobile station. Note that the I/Q diagram for the base station signal is for only a single channel (such as the pilot channel). In normal operation, many channels are summed together and transmitted on top of each other by the base station. O-QPSK is used in the mobile stations because it avoids the origin and makes the design of the output amplifier easier. For the base station, since many channels are summed together, using O-QPSK would not always avoid the origin. This is due to random nature of adding many signals together.

Slide #22



Signaling is well structured in CDMA. The full data rate of 9600 bps can be shared between data for the user and signaling data. The channel is effectively a modem that can be used for a variety of services. Current standards exist for service option 1, the vocoder. Service options 2 and 3 are under discussion at the standards committee. These proposed options are for a test mode of data loopback, and data services.

Slide #23



Test Aspects of CDMA: The test aspects can be broken into two major categories: transmitter test and receiver test.

Receiver Test: The receiver is made to work in the presence of high interference. For this reason, it is necessary to generate interference as part of the test equipment. An extra CDMA channel is added to the equipment and has its timing offset from the test channel. This is equivalent to the interference that is generated by adjacent cells. There is also an interference generator that is time aligned to the test channel but on a different Walsh code. This is orthogonal noise and is equivalent to the interference that would come from within the users active cell. Turning off the interference generators allows the sensitivity to be measured. This is more a measure of the noise figure of the receiver. CDMA radios operate with significant levels of bit errors; the raw channel bits have no inherent information and are not available outside IC's. The fundamental performance measure is the Frame Error Rate rather than Bit Error Rate.

Slide #24

CDMA Mobile Test Needs

- Transmitter Tests
  - Modulation Accuracy
    - Correlated Power
    - Frequency
  - Power Control
    - Open Loop
    - Closed Loop
- Fundamental Measure is Waveform Quality

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Transmitter Tests: The CDMA transmitter is measured for modulation accuracy which is defined as the cross correlation between the actual transmitted power and the ideal. This is important because any uncorrelated power from the transmitter is interference to all users of that frequency. The measurement must first be corrected for frequency error. The mobile must track the frequency of the base within 200 Hz. The modulation accuracy measurement also measures frequency. Power control needs to be checked; both closed loop and open loop. Open loop is checked by setting the power at the antenna port to a calibrated level and measuring the level of the transmitter. Varying the level of the test source should also vary the mobile station's output power. Closed loop power control is measured by setting the power control bits to specified sequences and verifying the power response of the mobile unit. It is necessary to establish a link to make this measurement.

Slide #25

CDMA Conclusions

- New Access Method
  - Code Based
- Designed for Use in Interfering Environment
- Uses Multipath to Advantage
- Has High Capacity
  - 10 to 20 Times Analog

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Conclusions: CDMA provides an advanced technology for Cellular applications. It provides high quality service to a large number of users. It is a system that has been extensively tested and it will be deployed later this year in pre-commercial applications. Commercial service is scheduled to begin in 1994.

Sequence Generation and Detection for Variable Rate CDMA Networks

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Abstract

By employing multiple spreading sequences generated by a multiple-register configuration, it is possible to increase the data rate in spread spectrum signals with relatively little loss in processing gain. Each sequence constitutes a symbol representing several bits of information. An additional bit of information can be sent during a symbol interval by taking polarity into account. A sequence is transmitted during a symbol interval to convey the information corresponding to that symbol. An efficient and effective method for generating sequences from a family of suitable spreading sequences and detecting which sequence was transmitted can be implemented using a two-register configuration, either real-time or block correlation methods, thresholding, and a decision logic that, when combined with coding, virtually eliminates the possibility of errors. Each sequence employed has relatively short period, facilitating synchronization and enabling either synchronous or asynchronous operation. Even using small-period sequences, the code space is quite large, so that a large number of users can be accommodated. The technique also provides an extra degree of freedom in power control.

1. Introduction

The coming revolution in wireless communications has been given a considerable impetus by FCC Rule 15.247, which allows license-free operation of spread spectrum radios (subject to certain power restrictions) within the Industrial, Scientific, and Medical (ISM) bands: 902-928 MHz, 2400-2483.5 MHz, and 5725-5850 MHz. Indeed, several manufacturers have developed spread spectrum radios that operate in these bands (for example, Cylink, Omnipoint, Western Digital, Proxim, WinData). In addition, spread spectrum communications and code division multiple access (CDMA) multiplexing have advantages in a number of application areas.

As is the case with any communications scheme, there are tradeoffs associated with use of spread spectrum and CDMA. For use in unlicensed portions of the RF spectrum, the principal advantage is low power spectral density - the power is distributed in frequency, so that a spread spectrum signal appears as broadband noise to other users in the band, raising their noise floors only slightly. In general, the main advantage of spread spectrum is robustness. Since there is so much redundancy in the signal, interference and other channel impairments, such as multipath, can be tolerated to a far greater extent than in other forms of communications.

There are a number of disadvantages to spread spectrum and CDMA, however, including the following. Synchronization and tracking can be difficult because the signal-to-noise-plus-interference ratio is often quite low. The "near-far problem," "shadowed" users, and similar problems make network power control an important and potentially difficult problem, much more so than in frequency-division multiple access (FDMA) and time-division multiple access (TDMA) systems. And, to achieve a given level of "processing gain" within a given bandwidth, the data rate must be limited to well below the rate that could otherwise be achieved were not such processing gain required. Communications over power lines [1] provides a good example.

Several authors ([2]-[8]) have pointed out that increases in data rate for a given bandwidth can be achieved by use of multiple spreading sequences. By utilizing multiple periodic sequences, it is possible to increase the information rate with much less loss in processing gain and concomitant increase in bit error rate than would result if the bandwidth of the information signal were increased directly. A more detailed explanation is given in section 2. In subsequent sections, convenient methods for generating and detecting sequences in a multiple sequence spread spectrum system are described. These techniques have a number of advantages over conventional systems and other multiple-sequence techniques that have been proposed. A number of these are listed in Section 3 and discussed further in later sections. Section 4 contains a description of two-register multiple sequence generation techniques. In Section 5, techniques for detection and decoding are given. Section 6 contains an explanation of the use of Hadamard Transforms for block correlation of the received signal with the possibly transmitted sequences. Section 7 provides a method for carrier tracking, which is especially important for mobile applications in which significant Doppler shifts are

possible. Section 7 contains a discussion on increasing the data rate by transmitting multiple sequences simultaneously. Section 9 provides an example that shows how MPEG/T1 rates can be supported using a 20 MHz chip rate. A summary is given in section 10.

2. The fundamental reason for using multiple sequences to increase data rate.

A conventional direct sequence spread spectrum signal can be viewed as the result of mixing a narrowband information-bearing signal $i(t)$ with an informationless wideband (and constant envelope) "spreading" signal $c(t)$, as depicted in Figure 1. If B_i, B_c denotes the bandwidths of $i(t)$, $c(t)$, respectively, and if $B_i << B_c$, then the bandwidth of the "spread" signal $i(t)c(t)$ is also approximately B_c. The "processing gain" available to the receiver is $G = B_c/B_i$, which can be realized (with some implementation losses, of course) by synchronizing the incoming signal to a locally generated version $c_0(t)$ of $c(t)$, mixing the received signal and $c_0(t)$, thus removing $c(t)$ from the signal and "collapsing" the signal to the "information bandwidth" B_i, within which the despread signal should have sufficient signal-to-noise ratio (SNR) to enable recovery of the information.

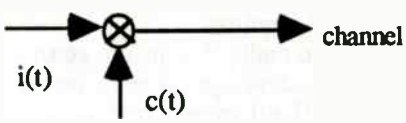

Figure 1. Simplified version of conventional direct sequence spread spectrum signal generation.

In voice channel or microwave communications, when faced with limited bandwidth availability and a need to transmit data faster, modem manufacturers commonly resort to increases in complexity, going from binary phase shift keying (BPSK), for example, to various quadrature-amplitude modulated (QAM) techniques. Unfortunately, in so doing, the transmitted symbols get "closer together" in phase and amplitude, thus increasing the probability of symbol error (unless, of course, power is increased) and requiring the introduction of complex equalizers to reduce channel distortion.

In a multiple sequence spread spectrum system, fixed lengths of each sequence are regarded as symbols that convey multiple bits of information, like the symbols consisting of phase-amplitude states in a QAM system. If, however, the sequences are (nearly) "orthogonal" over the length of a symbol (their cross correlations are 0 or very nearly 0 compared to the sequence length), then they are the same distance apart regardless of their number. It is this fact that explains why using multiple sequences to increase data rate provides an improvement in performance over that obtained if the data rate is increased by simply increasing the bandwidth B_i of the information signal $i(t)$, thereby directly decreasing the processing gain, G.

This can be seen using the following simple argument. Regard each of M orthogonal sequences as consisting of N "chips," each chip having a value of $+1$ or -1. The received signal consists one of the sequences plus additive white Gaussian noise (AWGN). Each noise sample has mean 0 and variance $\sigma^2/2$, where $\sigma^2 = 1/SNR$ (the factor $1/2$ is based on the assumption that two independent noise samples per chip have been averaged). The received signal is correlated with each of the M possibly transmitted sequences to obtain M correlation outputs. Ignoring the possibility of a sign inversion, the correlation output corresponding to the actually transmitted sequence can be represented as $N + x$, where $x \varepsilon N(0,N\sigma^2/2)$ (i. e., x is normally distributed with mean 0 and variance $N\sigma^2/2$). Since the sequences are assumed to be orthogonal, any other correlation output y is $N(0,N\sigma^2/2)$. The probability that the correlation output corresponding to the actually transmitted sequence exceeds a correlation output corresponding to another sequence is equal to the probability that $N + x > y$, which is the probability that a $N(0,1)$ random variable is less than $\sqrt{(N \times SNR)}$, or $1 - Q(\sqrt{(N \times SNR)})$, where

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} e^{-t^2/2} dt.$$

If Maximum Likelihood detection is used, so that the detected symbol is the one with the largest corresponding correlation value, then the probability that the correct symbol is detected is $(1-Q(\sqrt{(N \times SNR)}))^{M-1}$, and the probability of error is $0.5(1-(1-Q(\sqrt{(N \times SNR)}))^{M-1})$ (the factor 0.5 is included because if a symbol is decoded incorrectly, then, statistically, one-half of the decoded bits are correct and one-half are incorrect). The probability of error is plotted as a function of SNR in Figure 1 for the case that $M = 512$ sequences of length $N = 512$ are used. Using 512 sequences, 9 bits of information per period can be transmitted. Also shown in Figure 2 are the probabilities of error for (1) a conventional spread spectrum system with a processing gain of 512 (27 dB), and (2) a conventional system in which a factor-of-9 increase in data rate is achieved by decreasing the processing gain from 512 (27 dB) to $512/9$ (17.5 dB). The figure shows that there is some loss in processing gain in using multiple sequences, but much less than would result by directly increasing the data rate.

The performance improvement shown in Figure 2 can also be interpreted in terms of capacity. If a bit error rate (BER) of 10^{-3} (before decoding) is required for a particular

application, then the SNR can be as low about *-14* dB. This equates to about 20 simultaneous users sharing the channel, assuming that each user's signal arrives at the receiver with the same power. Each user is assumed to be transmitting 9 bits per period, with *512* chips per period. Hence, the aggegrate data rate is given by $20 \times 9/512 = .35$, or a system capacity (ignoring error control) of more than a third-of-a-bit per Hertz. Of course, for a less stringent BER requirement, the capacity is greater.

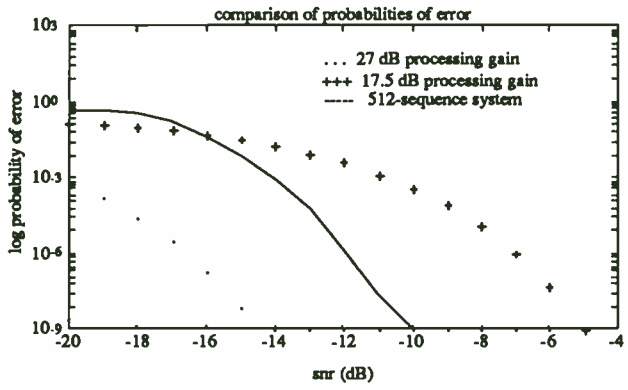

Figure 2. The use of multiple orthogonal sequences provides an improvement over systems that achieve the same information rate in the same spread bandwidth by decreasing processing gain.

In the following sections, methods for implementing multiple sequence spread spectrum systems are discussed. These include alternative methods of making symbol decisions that can reduce the probability of error (at an increase in the number of erasures) and that can also provide a mechanism for assisting in power control.

3. Advantages of two-register multiple sequence generation.

If multiple sequences are to be employed in a spread spectrum communications system, it is important that the sequences not be merely time offsets of one another. In that case, false synchronization could occur, and symbols could be interpreted incorrectly. Authors who have dealt with the practical aspects of implementing such a system have recognized this (see [6], for example). An easy way to guarantee the independence of the spreading sequences at all offsets of one another is to add modulo-*2* a pseudo-random sequence to whichever information-bearing sequence is to be transmitted. This is the approach taken below, in a way that provides a large measure of flexibility in choosing data rates and processing gains.

Most authors ([2], [3], [4], [6], for example) who have suggested the use of multiple orthogonal sequences have assumed perfect orthogonality of the sequences and then conducted performance analyses (as in section 2). They have not provided implementation details. The best-known existing system which employs multiple sequences is that of Qualcomm [8]. It conveys six bits of information every *64* bits in the form of one of the rows of a 64×64 Hadamard matrix, which are added to a pseudorandom sequence of very long period to form the spreading sequence. That is, a type-1 Reed-Muller code [9, pp. 31-32] is applied. At the receiver, the long sequence is "stripped," the resulting data is formed into a 64-long vector, and a Hadamard Transform is computed. The transform coefficient with the largest magnitude is assumed to correspond to the actually transmitted sequence (the Maximum Likelihood decision rule). The Hadamard Transform is very computationally efficient, since the only operations required are $N \times \log_2(N) = 64 \times 6 = 384$ adds/subtracts. While the rows of a Hadamard matrix are perfectly orthogonal, they are not easily generated one at a time. Thus, if rows of a Hadamard matrix are used as symbols, it is likely that the entire matrix is stored and a given row is clocked-out when needed. Kuroyanagi and Guo [11] have proposed using rows of a Hadamard matrix combined with short maximal-length linear recursive sequences ("M-sequences") of approximately the same length. The Qualcomm technique and the Kuroyanagi/Guo method provide orthogonal spreading codes, but they offer very little flexibility in data rates and limited amounts of processing gain. They are not applicable in a system in which a wide range of rates and gains are required.

The approach to multiple sequence generation described below retains the advantages of using perfectly orthogonal but perhaps difficult-to-generate codes, and it also provides added flexibility. It has the following properties:

(a) A large family of almost-orthogonal sequences can be generated with compact circuitry.

(b) Using sequences of large period imposes very little additional memory requirements over using sequences of small period, since different sequences are specified by assigning feedback taps and initial fills to relatively short registers.

(c) Because the sequences are relatively short, rapid acquisition of synchronization is possible, enabling either synchronous or asynchronous modes of operation.

(d) A two-register configuration eliminates any reasonable likelihood of false synchronization and ensures rapid detection of loss of synchronization.

(e) Switching between sequences is easily accomplished.

(f) There is no need to have a correlation circuit for each candidate input sequence. A Fourier or Hadamard transform technique (as in the Qualcomm and Kuroyanagi/Guo approaches) or a hard-wired approach can be used to compute all correlations simultaneously .

(g) Error correction coding is easily incorporated. Because "blocks" of bits correspond to each sequence, the

system is especially well suited to implementation using Reed-Solomon codes.

(h) A threshold detection method in conjunction with coding can virtually eliminate the possibility of errors, in favor of erasures. One correlation magnitude per possible transmitted sequence is computed and the largest is compared to the next-largest. If their ratio exceeds a specified threshold, a decision is made. The threshold is chosen so that the probability of an "erasure" is much greater than that of an error, so that errors do not occur in isolation but in conjunction with erasures. The coding scheme either corrects the errors and fills in the erasures or else declares a non-correctable error/erasure pattern.

This scheme can also aid in power control, since, for example, a sequence of marginal detections can indicate that a user should be allocated more power or should increase sequence length (by adjusting feedback taps and fills).

(h) "On-demand" data rate is available to a given user in the network by dynamic allocation of variable numbers of sequences to different users and also by allocation of different power levels, enabling users with greater power allocations to transmit multiple sequences simultaneously. If CDMA is combined with TDMA or FDMA, the user may also be allocated a variable number of time or frequency slots.

(i) The transmitter and receiver can be "asymmetric" in that the number of sequences available to one node in a network can be different from the number available to another. This can be important in applications where it may be desired to maximize the rate of the data transmitted from a remote station, for example, while the rate (and hence power) requirements of that station for receiving control, set-up, "housekeeping," and other such information may be quite modest.

(j) An extra degree of freedom in power control is provided. For example, a "near-far condition" manifests itself in the receiver as a sequence of erasures, as does a loss of synchronization or a loss of signal (a "fade"). If an "erasure condition" is combined with a measurement of received signal strength, then the actual presence of a competing signal can be declared. In this case, the receiver could signal the transmitter to switch frequencies, increase power, increase processing gain by increasing sequence length (thereby decreasing data rate), or take other measures to restore the link. Sequences with large period (and hence large processing gain) can be used at start-up to facilitate initial power allocations.

(k) The technique is compatible with other spread spectrum systems employing linear feedback shift registers for spreading sequence generation.

(l) Despite the use of sequences with short period, the code space is quite large, so that system capacity is not limited because an insufficient number of codes is available.

(m) In mobile applications where significant Doppler shifts can occur, an auxiliary, "informationless" code sequence can be transmitted, thus facilitating carrier tracking and synchronization.

4. Sequence generation.

Figure 3 is a block diagram of a multiple-sequence generator and a symbol- (sequence-) selection unit. Fundamental to the implementation is the use of two registers for sequence generation. In the configuration shown, there are thirteen possible output sequences, one less than the total number of stages in the shift registers (Note that the number of stages can be greater than the degrees of the generating polynomials of the sequences). Each output sequence is obtained from the modulo-*2* sum of different stages of the registers. While the feedback taps are shown as hard-wired, they should be regarded as programmable, so that a large number of shift register sequences can be generated.

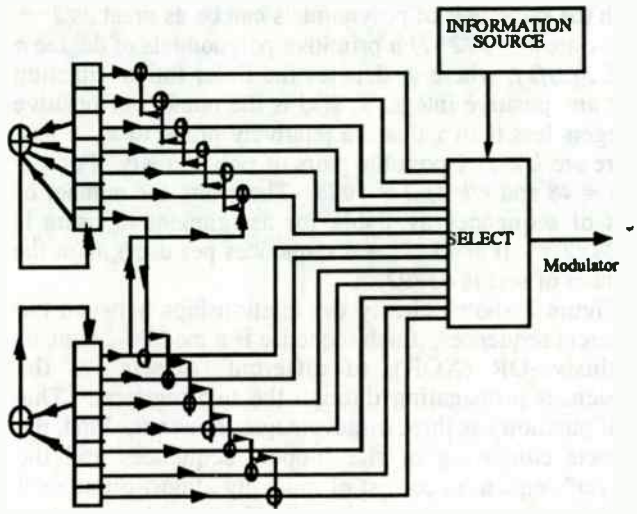

Figure 3. Example of multiple sequence generation. In the configuration shown, M = 7 is the number of stages in each register. n=5 is the degree of each of the polynomials in the "Gold preferred pair", $1+x^2+x^5$ and $1+x+x^2+x^4+x^5$.

Each sequence generated by the apparatus in Figure 3 has the same period. A new output sequence is selected for transmission once per symbol interval. Taking the number of "chips" per symbol to be equal to the period of the sequences ensures best-possible cross correlation properties over the entire of the family of sequences, but, in general, the symbol period can be any specified number of chips.

The feedback taps in the registers shown in Figure 3 correspond to a "Gold preferred pair" [11] of "primitive" polynomials of degree *5*, and sequences generated by a product of such polynomials is commonly called a "Gold Code" (a primitive polynomial over *GF(2)*, the field of two elements, is an irreducible polynomial that generates a maximal-length linear recursive sequence, or "M-sequence"). Kasami Codes [12] or Reciprocal Codes [13]

are other good candidate sequences. These sequences provide guaranteed maxima of cross correlation coefficients when the correlations are computed over a period of the sequences, and they are widely recognized as suitable for use in CDMA networks where, for example, each user is given a Gold Code to use as a spreading sequence. However, in networks with a large number of users, the average cross correlation value is more important than the maximum, and sequences generated by a product of arbitrarily chosen primitive polynomials of the same degree usually provide satisfactory performance. This means that the code space is quite large, so that a large number of users can be accommodated with spreading sequences - much larger than the channel could actually support.

As an example, if each composite polynomial f_1, f_2 is primitive of degree n, then there are 2^n+1 possible sequences that can be generated by the product f_1f_2. If each user is assigned 2^m sequences, the number of users with the same pair of polynomials can be as great as 2^{n-m}. There are $k = \phi(2^n-1)/n$ primitive polynomials of degree n in $GF(2)[x]$, where ϕ denotes the Euler totient function (for any positive integer x, $\phi(x)$ is the number of positive integers less than x that are relatively prime to x). Thus, there are $k(k-1)/2$ possible pairs of polynomials. For $n = 9$, $k = 48$ and $k(k-1)/2 = 1028$. Therefore, the number of sets of sequences available for assignment to users is $1028 \times 2^{9-m}$. If $m=3$ ($2^3 = 8$ sequences per user), then the number of sets is 65792.

Figure 3 shows clearly the relationships between the different sequences. Each sequence is a modulo-2 sum, or exclusive-OR (XOR), of different "offsets" of the sequences propagating through the two registers. This configuration has three disadvantages, however. First, the subsets consisting of the "upper" sequences and the "lower" sequences consist of mutually almost-orthogonal sequences when correlated at 0-offset, but correlations between subsets are correlations of different sequences within a Gold-code family and therefore have the 3-level autocorrelation properties typical of Gold Codes. Implemented as shown, a decision scheme that is more complex than the simple Maximum Likelihood technique is necessary to achieve best performance (see the next section). This disadvantage is eliminated in quadrature implementations such as that shown in Figure 4. There, two sequences are transmitted in quadrature, one sequence being taken from the "upper" subset and one from the "lower" subset. Because the non-orthogonal sequences are transmitted on orthogonal carriers, they do not interfere with one another.

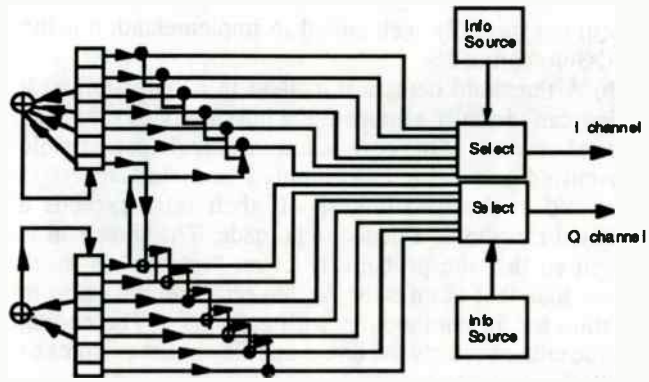

Figure 4. Sequences can be transmitted simultaneously, in quadrature, thereby increasing the data rate and eliminating the problem of non-orthogonality between the "upper" and "lower" sequences.

Of course, sending two sequences simultaneously requires twice as much power, an increase of 3 dB. This can be avoided by adjusting the taps of the shift registers in Figure 4 to utilize polynomials of degree 6 rather than 5. Then, the period of the sequences is 63 rather than 31, giving an additional processing gain of 3 dB. There are 4 sequences per arm, so 2 information bits per 63-chip period are transmitted per arm, or 4 information bits per 63-chip period. In the configuration in Figure 4, 3 information bits every 31 chips were conveyed. Thus, there has been a decrease of approximately 33 percent in data rate in exchange for isolation of the sequences without increasing power, and also in exchange for an increase in receiver complexity. The percentage decrease in data rate that results from using this technique diminishes as the number of sequences and hence the number of bits per period increases. For example, if a user is assigned 16 sequences, the data rate changes from 4 bits every 31 chips to 6 bits every 63 chips, a decrease of about 25 percent.

The second disadvantage of the configuration in Figures 3 and 4 is that the number of sequences that can be generated is limited by the size of the shift registers. Thus, in the example shown, probably no more than 8 sequences would be used. The third disadvantage is that such an architecture requires as many XORs and register stages as there are sequences. These limitations can be overcome by "switching-in" appropriate register fills at the beginning of each symbol interval, as shown in Figure 5. These initial fills correspond (via table lookup) to the bits represented by each sequence. Because arbitrary fills can be switched into the register, the number of sequences available to a user is limited only to 2^n, where n is the degree of the generating polynomial of the upper register. Consequently, 2^n fills and therefore a maximum of 2^n sequences are available and could be assigned to a single user.

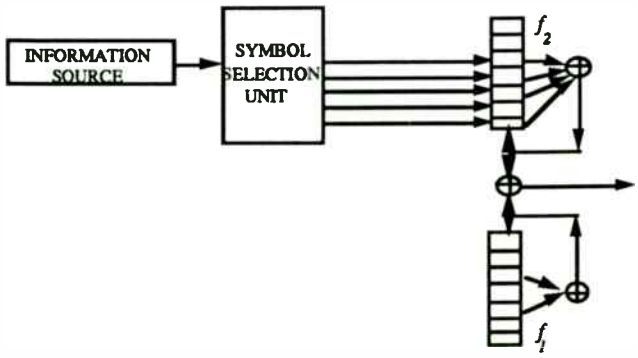

Figure 5. A more hardware-efficient method of generating multiple sequences. Fills corresponding to the information to be transmitted are "switched-in" at the beginning of each symbol interval. As many as 2^n sequences can be generated for a given tap setting, where n is the degree of the primitive polynomial f_2 that "drives" the upper register.

Assigning sequences to a user is no more difficult than specifying a pair of polynomials, the number 2^m of sequences allocated to that user, and an "initial fill" (the lower register can be assumed to contain the "impulse fill," *00...01*). The initial fills corresponding the 2^m sequences are the specified fill and the 2^m-1 fills that appear in the register as it is stepped 2^m-1 times, starting with the specified fill.

Suppose that $n = 10$ and that all *1024* sequences of period *1023* are assigned to a single user, each sequence corresponding to a distinct initial fill of ten bits. This user can then transmit eleven bits of information per symbol (*1023* chips), ten bits corresponding to the sequence selected for transmission and an eleventh (differential) bit of information conveyed by the "polarity," or sign, of the sequence: if the eleventh bit is unchanged from the last symbol, the sequence is transmitted "upright" (as is); if it changes from *0* to *1* or from *1* to *0*, the sequence is "inverted" modulo-*2* (Stark and Woerner [4] employed the "polarity bit" in a trellis coding scheme, rather than using it for data). In general, the data rate, f_d (ignoring coding and including the polarity bit), the chip rate, f_c, the sequence length, $2^n - 1$, and the number of sequences, n_s (assumed to be 2^m for some integer $m \leq n$), employed by a user are related by the equation $f_d = f_c(m+1)/(2^n-1)$.

A user's data rate can be increased/decreased by a factor of *2* and processing gain decreased/increased commensurately by *3* dB by decreasing/increasing n by *1*. This can be done dynamically, in response to detection performance. Also, by increasing m to $m+1$, an additional bit per period of information can be transmitted, at the cost of reducing the number of sequences available to other users by 2^m. Data rate can also be varied by sending multiple sequences simultaneously (see section 7). Thus, by varying a user's parameters, variable rates and variable processing gains can be accommodated within a single CDMA network - hence the term "variable rate" in the title of this paper.

It is worth noting that the sequence generated by the lower register in Figure 5 is arbitrary. While Figures 3 and 4 show sequences that correspond to a Gold preferred pair, it is not necessary that there be any relationship between the sequences propagating in the upper and lower registers. Indeed, in synchronous communications, only the sequence in the upper register need be periodic. The main purposes of the sequence in the lower register are to enable acquisition and maintenance of synchronism and detection of false synchrony and to enlarge the address space.

5. Sequence detection.

Case 1. Relatively few sequences per user.

In Figure 3, each output sequence $\{c_k\}$ is of one of two types: (i) $c_k = a_{k-u} \oplus b_k$ or (ii) $c_k = a_k \oplus b_{k-v}$ ("$\oplus$" denotes addition *mod 2*) for some integers u, $v (mod\ 2^n-1)$, where $\{a_k\}$ denotes the sequence emanating from the bottom stage of the upper register and $\{b_k\}$ denotes the sequence emanating from the top stage of the lower register. In the receiver, detection of the transmitted sequence is tantamount to determination of the correct type, (i) or (ii), and the correct offset, u or v.

The first step is to correlate the incoming signal with each possibly transmitted sequence. To obtain useful results from the correlations, the signal must be at baseband, so carrier recovery and tracking is critical in this or other multiple-sequence systems (this is discussed further in section 7). Figure 6 shows a block diagram of a "traditional" receiver structure that performs this function. One matched filter per possible transmitted signal is implemented. The received signal is filtered by each and the outputs evaluated. Such an architecture is unnecessarily complex for detecting the sequences proposed here.

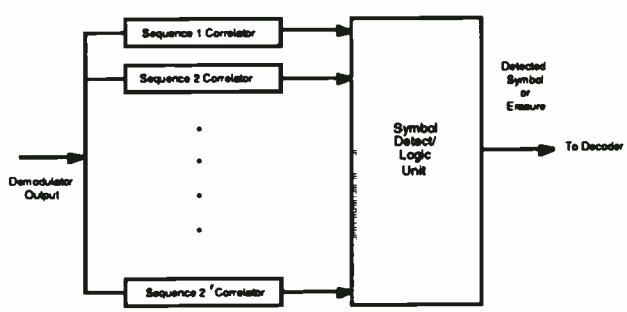

Figure 6. A receiver consisting of a bank of matched filters, one for each possible received sequence. This architecture is unnecessarily complex, even when the number of sequences is relatively small.

Figure 7 depicts an alternative the method for performing the required correlations of the received signal (at baseband and chip-synchronized) with each of eight sequences, which illustrates that if the number of sequences per user is less than the number of stages in the shift registers that generate the component sequences, then the same circuitry can be utilized in both the transmitter and receiver. Note that after the last chip in a symbol has been received, the correlation values are available for analysis and symbol decision.

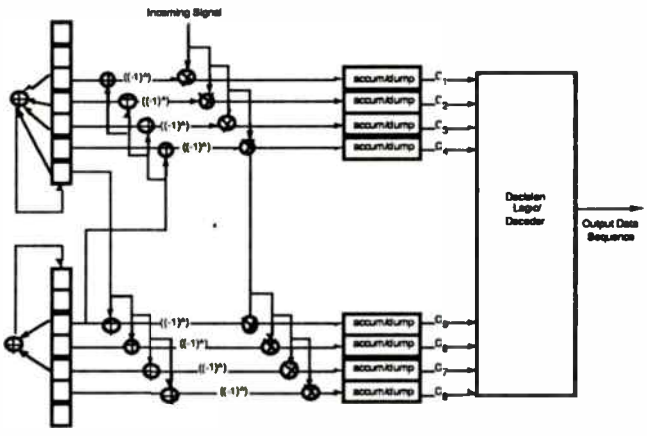

Figure 7. The multiply-accumulates required for each matched filter are performed in parallel as the baseband, chip-synchronized signal is received, using the same circuitry that was used to generate the sequences.

In previous analyses of multiple-sequence spread spectrum schemes where the sequences are perfectly orthogonal ([2],[3]), the detection logic has been maximum likelihood detection, where a sequence is determined to have been transmitted if the correlation of that sequence with the incoming signal has the largest magnitude. Within each of the classes (i), (ii) above, the sequences cross-correlate as different offsets of an M-sequence, and therefore the cross-correlation magnitudes are almost *0*. That is, within each class, the sequences are orthogonal. However, the cross-correlation of a sequences in class (i) and a sequence in class(ii) need not be *0*. For example, in the case that the component sequences are generated by a preferred pair of Gold Code polynomials of degree *n*, the correlation magnitude is, with probability *0.5*, approximately $2^{[n+2]/2}$, where "[.]" denotes the "greatest integer function." Consequently, performance can be improved by determining the most likely class and the most likely sequence within that class, if the largest correlation magnitude among all sequences is not sufficiently greater than the second-largest correlation magnitude. Figure 8 is a block diagram of a decision logic for implementing this concept. The threshold is selected so that the probability of error is considerably less than the probability of erasure, and it depends on the values of the cross-correlations of the upper and lower sequences in Figure 7.

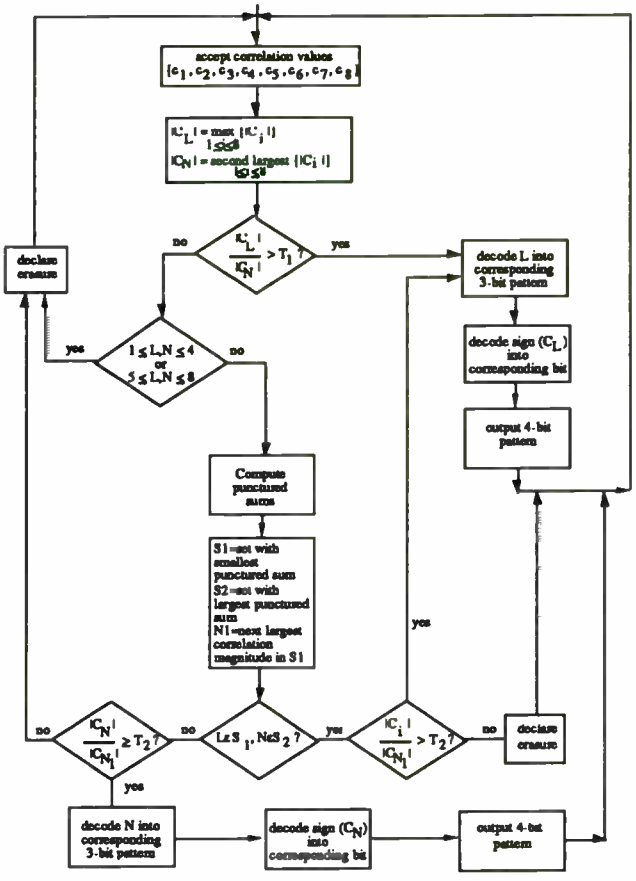

Figure 8. Decision logic for the detection scheme shown in Figure 7. If the largest correlation magnitude is not sufficiently greater than the next-largest, a decision between "upper" and "lower" subsets is made. Then a sequence within the winning subset is selected, or an erasure is declared.

Case 2. Many sequences per user.

In Figure 5, an output sequence $\{c_k\}$ is of the form $c_k = a_{k-u} \oplus b_k$ for some integer u *(mod* 2^n*-1)*. Detection of the transmitted sequence is equivalent to determination of the correct offset u. The offset can be determined by first "stripping" $\{b_k\}$ from the baseband, chip-synchronized received signal, accumulating the result over a period of the remaining sequence $\{a_k\}$, and "block correlating" the stored period with $\{a_k\}$ using fast transform techniques.

Figure 9 contains a diagram that illustrates the sequence generation, transmission, and block correlation process. The block correlator can be implemented in one of several ways. If an efficient DFT algorithm on $N = 2^n-1$ points is available, then the cyclic correlation between the received sequence (with $\{b_k\}$ stripped) and the stored sequence requires an application of the N-point DFT algorithm, followed by N complex multiplies by the precomputed and stored N-point transform of the sequence

$\{(-1)^{a_k}\}$, followed by application of the associated N-point inverse DFT algorithm. Unfortunately, to achieve good efficiency, custom DFT algorithms must be designed for each value of N (a methodology for developing such algorithms is given in [14]).

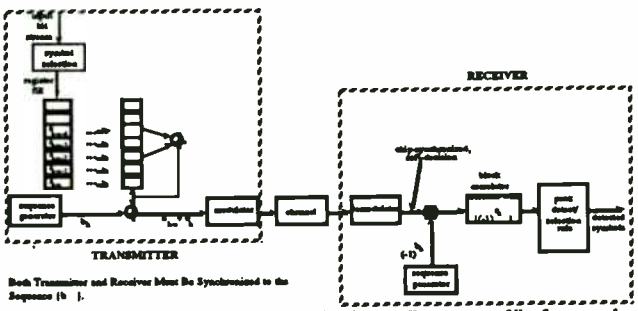

Figure 9. The sequence $\{b_k\}$ is "stripped" from the baseband, chip-synchronized signal, and the result is correlated with all possibly transmitted sequences with a block correlator implemented using fast transform techniques.

An alternative is to compute acyclic correlations using fast Fourier transforms (FFTs) of length 2^{n+1}. $(2^n - 1)$-point sequences can be correlated by padding with 0's to form two 2^{n+1}-point sequences, multiplying the transform coefficients point-by-point, and computing the inverse transform. Of course, the transform of $\{(-1)^{a_k}\}$ (padded with 0's) can be pre-computed. Optimized power-of-2 FFT algorithms are available for every commercial DSP chip, so use of FFTs many be an attractive option for the block correlator.

Hadamard transforms can also be used, as in the Qualcomm scheme, and this approach represents the most attractive alternative for implementing a block correlator for M-sequences. The inputs and outputs of the Hadamard transform must be permuted in a manner dependent on the primitive generating polynomial of $\{a_k\}$ (explained in the next section), but these permutations can be implemented using table lookups. Thus, it is not necessary to use difficult-to-generate rows of a Hadamard matrix as spreading sequences to make use of efficient Hadamard transforms for detection. Easily generated and more flexible M-sequences can be used just as well.

The advantage of using Hadamard transforms to compute the correlations can be easily seen from operations count. As indicated above, the desired correlations can be computed using a real FFT of length 2^{n+1}, 2^{n+1} complex multiplies, and a complex inverse FFT of length 2^{n+1}. The number of real operations for these computations is approximately $18(n+1)\times 2^n$. If the correlations are performed using a single 2^n-point Hadamard transform, which requires only $n \times 2^n$ real additions/subtractions, then the computational savings is a factor of about 18.

Hadamard Transforms are efficiently computed using Yates' Algorithm [15, 16], which is well-suited to implementation in an ASIC to achieve high-speed operation. The ASIC would compute the Hadamard Transform and also perform some additional functions, including the reorderings indicated in the next section.

As an example of the order of computation required, if the period is 1023 and the chip rate is 10.23 MHz, then 10000 1024-point Hadamard Transforms per second must be computed and their outputs processed. The computational requirements are slightly less that 100 Mflops. Also, the decoding process is parallelizable, since different symbols can be processed by different processors. Thus, multiple processors could be employed, with the received symbols (sequence segments) allocated cyclically to the available processors. Consequently, computational requirements are well within the capabilities of current technology.

The largest squared output of the block correlator corresponding to a valid offset corresponds to the most likely sequence. To ensure that the data received is of good quality, an "erasure" could be declared unless the largest squared correlation magnitude exceeds the second largest by a pre-selected threshold, TH. An error occurs when the squared magnitude of the correlation of the input signal and an incorrect sequence exceeds the squared magnitude of the correlation of the signal with the sequence actually transmitted by a factor of at least TH. An erasure occurs when the ratio of the largest squared correlation magnitude to the next-largest squared correlation magnitude is less than TH.

The value chosen for TH depends principally on the required bit error rate, data rate, and complexity of coding/decoding acceptable. Detected symbols and erasures are interpreted by the error correcting code logic employed to correct the erased or incorrect symbols, or to declare a "block erasure" when too many erasures have occurred. Reed-Solomon codes are especially well suited to this purpose,

A Reed-Solomon code of minimum distance d can correct a pattern of r erasures and e errors provided that $r + 2e < d$. If d or more erasures occur, the decoder will not attempt correction and will declare that an uncorrectable word has been received. Thus, for example, if TH is chosen so that the probability of an error is much less than $1/8$-th that of an erasure, then a received word that contains no more than $4d/5$ erasures is unlikely to contain more than $d/10$ errors. If the decoder does not attempt to decode blocks with more than $4d/5$ erasures, then the probability is very small that a block will be incorrectly decoded. In practice, TH must be chosen to provide an acceptable balance between r and e.

If the largest squared correlation magnitude corresponds to the actually transmitted sequence, then the ratio of the largest squared correlation magnitude to the next largest is the ratio of a non-central chi-square random variable and an order statistic, the maximum of a collection of $2^m - 1$ chisquared random variables, where 2^m is the number of possible sequences. The probability density function of the ratio of these random variables is complicated but

calculable, and thus the probability of a correct decision as a function of sequence length, signal-to-noise ratio, and TH is can be obtained in a straightforward manner.

As an example, the probability that the largest of 511 samples from a χ_1^2 distribution exceeds the next-largest by a factor of 2 is about 10^{-2}. Thus, if $TH = 2$, then during a fade, for every decision (and consequent probable error) 100 erasures are expected. In general, if it is desired that $pr(\text{(largest } \chi_1^2)/(\text{next-largest } \chi_1^2 > TH) < \varepsilon$, then it can be shown that TH can be chosen by the formula $TH = 1 + (1/a_N) \ln (1/\varepsilon)$, where $a_N = -1.5 + \ln (4+N)$, N being the number of χ_1^2 samples.

6. Hadamard Transform Correlators.

Just as in the Qualcomm CDMA scheme, the Hadamard transform can be used to correlate the incoming signal with each of the possible spreading sequences $\{a_{k-u} \oplus b_k\}$, after the sequence $\{b_k\}$ has been stripped from the signal by multiplying each incoming baseband, chip-synchronized signal sample by $(-1)^{b_k}$. Unlike the Qualcomm method, the incoming data must be permuted prior to applying the Hadamard transform, and then the Hadamard transform coefficients must be permuted again to obtain the correlation values at successive offsets. An explanation is given below.

All operations in the following (except for sums of subscripted indices) take place over $GF(2)$, the field of two elements. The cyclic correlations $\{c_0, c_1, \cdots, c_{2^n-2}\}$ at successive offsets between a (2^n-1)-long sequence $\{y_0, y_1, \cdots, y_{2^n-2}\}$ of real or complex numbers and a binary sequence $\{u_0, u_1, \cdots, u_{2^n-2}\}$ of the same length are defined by the equations

$$c_k = \sum_{i=0}^{2^n-1} y_i (-1)^{u_{i+k}}, \quad 0 \le k \le 2^n-2.$$

The Hadamard transform of a 2^n-long sequence $\{z_0, z_1, \cdots, z_{2^n-1}\}$ is defined to be the set of transform coefficients $\{Z_s\}$, defined by

$$Z_s = \frac{1}{2^n} \sum_{k=0}^{2^n-1} (-1)^{\bar{k}\cdot\bar{s}} z_k,$$

where $\bar{k} \cdot \bar{s}$ denotes the dot product of the vectors $\bar{k}$ and $\bar{s}$ consisting of the n-long binary representation of the integers k and s, respectively (that is, if $k = \sum_{i=0}^{n-1} k_i 2^i$, then $\bar{k} = (k_0, k_1, \cdots k_{n-1})$). The convolution coefficients $\{c_k\}$ may be obtained as a permutation of the coefficients of a Hadamard transform applied to a padded and reordered version of the sequence $\{y_k\}$. To show this, it is necessary to discuss some concepts from the theory of finite fields.

Suppose that $f(x)$ is a polynomial of degree n in $GF(2)[x]$ (the set of polynomials in the variable x with coefficients in $GF(2)$, the field of two elements, 0 and 1), given by

$$f(x) = x^n \oplus \sum_{i=1}^{n} f_i x^{n-i}$$

(Here, Σ denotes a sum in $GF(2)[x]$). A linear recursive sequence satisfying f is a sequence $\{u_k\}$ such that $u_k = f_1 u_{k-1} \oplus \cdots \oplus f_n u_{k-n}$, and f is said to "generate" $\{u_k\}$. As mentioned previously, if $\{u_k\}$ is an M-sequence, then f is said to be "primitive." The "companion matrix" of f is defined to be

$$A = \begin{bmatrix} f_1 & f_2 & \cdots & f_{n-1} & f_n \\ 1 & 0 & \cdots & 0 & 0 \\ 0 & 1 & \cdots & 0 & 0 \\ \cdot & \cdot & \cdots & \cdot & \cdot \\ \cdot & \cdot & \cdots & \cdot & \cdot \\ \cdot & \cdot & \cdots & \cdot & \cdot \\ 0 & 0 & \cdots & 1 & 0 \end{bmatrix}.$$

If $\{u_k\}$ is a linear recursive sequence over $GF(2)$ satisfying $f(x)$, let $\underline{u}_k$ denote the column vector

$$\underline{u}_k = \begin{bmatrix} u_{k+n-1} \\ \cdot \\ \cdot \\ \cdot \\ u_{k+1} \\ u_k \end{bmatrix}.$$

Then, $A_f \underline{u}_k = \underline{u}_{k+1}$. That is, multiplication of a fill $\underline{u}_k$ by A_f shifts a register "driven by f" to produce the next fill, $\underline{u}_{k+1}$. Thus, $\underline{u}_k = A_f^k \underline{u}_0$. If f is primitive of degree n, then a sequence of 2^n-1 successive fills of a register driven by f consists of a permutation of all of the non-zero binary n-tuples.

Let

$$\underline{e} = \begin{bmatrix} 0 \\ 0 \\ \cdot \\ \cdot \\ \cdot \\ 1 \end{bmatrix},$$

and suppose $\underline{e}^T$ denotes the transpose of $\underline{e}$. Let $\underline{e}_k = (A_f^T)^k \underline{e} = (e_{ki})$. Then, $\underline{u}_k = e^T u_k = \underline{e}^T A_f^k \underline{u}_0 = e_k^T \underline{u}_0$.

Now suppose that f is primitive and define $\{z_0, z_1, z_2, \cdots, z_{2^n-1}\}$ by $z_0 = 0$ and $z_{\underline{e}_i} = y_i$, $0 \le i \le 2^n-2$ (here, $\underline{e}_i$ is

allocated *32* sequences. Then by transmitting a single sequence plus parity, six bits of information are conveyed. Suppose that the allocation is increased to *48* sequences and that these are partitioned into three sets of sixteen. If three sequences, one sequence from each set plus parity, are transmitted simultaneously, then five bits of information are conveyed by each sequence during a symbol interval. That is, by increasing the sequence allocation, tripling the power, and transmitting three sequences in a single symbol interval, the data rate is increased by a factor of *5/2*, with no loss in performance. The cost is a factor of 3 (5 dB) in increased power and increased transmitter and receiver complexities.

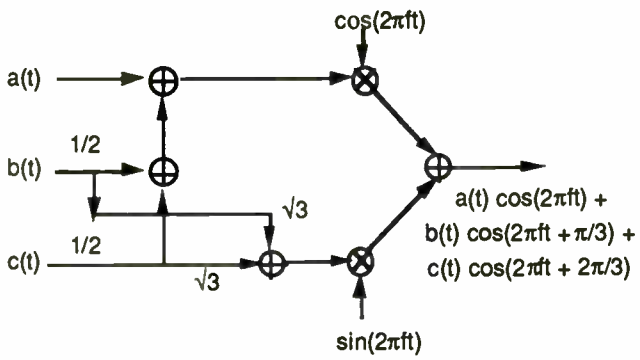

Figure 12. Ternary PSK, where three sequences are transmitted simultaneously. An extra 6 dB of isolation between the sequences is obtained as a result of the 60-degree phase offsets. This can be helpful especially during acquisition.

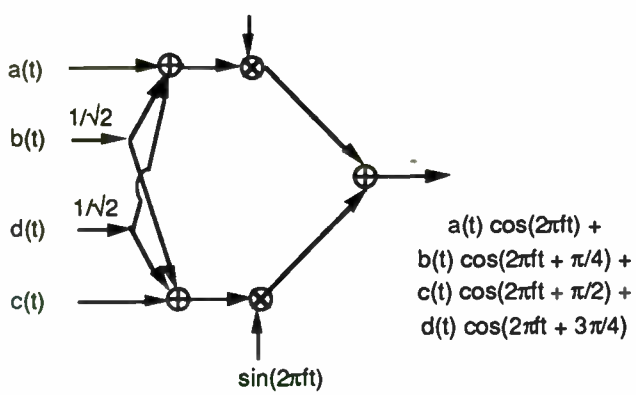

Figure 13. Quaternionary PSK (named in honor of the great Irish mathematician William Rowan Hamilton and in remembrance of my teacher, Gordon Pall, who enriched Hamilton's theory). Four simultaneously transmitted sequences are offset in phase by 45 degrees. The signal output can be interpreted as the real part of the product of two of Hamilton's (not Herod's) quaternions. The 45-degree offset provides an extra 3 dB of isolation between the four sequences.

9. An Example.

A *20* Mhz chip rate is a good choice for operation in ISM bands, since the smallest bandwidth is *28* MHz and the others are roughly multiples of that bandwidth (this is the chip rate used by Omnipoint, for example). Suppose that a chip rate of *20.32* MHz, a spreading code of length *127*, *128* sequences per user, and quaternionary PSK are employed. Four sets of *32* sequences are used to convey information, with one sequence from each set (*5* bits of information per sequence) being sent every period. Then a total of 20 bits per period, 160000 periods per second, and 3.2 Mbps are transmitted. If a rate-1/2 code is used, the the information rate is 1.6 Mbps, which is sufficient to transmit MPEG or T1 data.

By sending four sequences simultaneously, the power allocation for four users has been used. In the ISM bands, this may not be an option, since the power allocated to any one user cannot exceed one watt. In that case, the viable range of transmission will be reduced if multiple sequences are employed without an increase in power.

10. Summary.

A flexible, straightforward method for generating and detecting sequences for use in a multiple-sequence spread spectrum network has been described. The sequences generated are almost orthogonal and therefore near-optimal for use in a CDMA network. The technique has a number of advantages over other methods that have been proposed, including flexibility in data rates and processing gains, thereby providing an extra degree of freedom in system control and extending the range of feasible applications. Fourier/Hadamard transform block correlation techniques can be used to perform simultaneous correlations of the received signal with all of the possibly transmitted sequences. In situations where Doppler shifts are a problem, accurate carrier tracking (and synchronization) can be achieved by transmitting an informationless signal in quadrature with the information-bearing signal. Data rates can be increased even further by allocating additional power to a user, who then can transmit multiple signals simultaneously using "ternary PSK" or "quaternionary PSK." An MPEG/T1 rate of 1.5 MHz can be supported with a chip rate of 20 MHz, which is suitable for operation in the license-free ISM bands.

used as a subscript indicating the integer, g_i, say, that has $\underline{e}_i$ as its binary representation; that is, $\overline{\gamma}_i = \underline{e}_i$). Define $\{d_1, d_2, \cdots, d_{2^n-1}\}$ by $d_{u_k} = c_k$, $0 \le k \le 2^n-2$, where the vector u_k is similarly used as a subscript. Since f is primitive, these correspondences are one-to-one. Then,

$$d_k = \sum_{i=0}^{2^n-1} z_i(-1)^{\overline{i \cdot k}}, 1 \le k \le 2^n - 1.$$

Let $d_0 = \sum_{i=0}^{2^n-1} z_i = \sum_{j=0}^{2^n-2} y_j$., the correlation of $\{y_i\}$ with the all-0 sequence (the "other" sequence generated by f). Then, $\{d_k\}$ is the Hadamard transform of $\{z_i\}$, which is obtained by setting $z_0 = 0$ and then filling the position with binary representation $\underline{e}_k$ in the vector $\underline{z} = (z_i)$ with y_k, for $0 \le k \le 2^n-2$. The coefficients $\{d_1, d_2, \cdots, d_{2^n-1}\}$ are a permuted version of the correlation coefficients $\{c_0, \cdots, c_{2^n-2}\}$. Thus, the cyclic correlation of the data sequence $\{y_i\}$ and the M-sequence $\{u_k\}$ can be computed by appropriately rearranging $\{y_i\}$ and appending a 0, computing the Hadamard transform, and then permuting the transform coefficients.

7. Carrier tracking using an informationless signal in quadrature.

As indicated above, it is important that the signal be brought to baseband accurately prior to application of a bank of matched filters. Carrier tracking is more difficult for multiple-sequence spread spectrum than for conventional direct sequence spread spectrum signals. In a system that employs a single spreading sequence (as in Figure 1), that sequence is mixed with the incoming signal to spectrally "collapse" the signal to a narrow bandwidth (the "information bandwidth") where the signal has positive SNR. Carrier acquisition and track can then be accomplished using phase-locked loops or other methods traditionally applied to high-SNR signals.

When multiple sequences are used, the sequence to mix with the incoming signal to despread it is unknown *a priori*. Thus, there is no positive-SNR signal available for carrier tracking. This can be a significant problem in mobile, underwater, or other applications in which Doppler frequency shifts of significant size and variability can occur. The situation can be remedied by sending an informationless sequence in quadrature with the information-bearing multiple sequence signal, as shown in Figure 10.

In the receiver, the signal can be brought to baseband by collapsing the informationless signal to a sinusoid at the carrier frequency, phase shifting it by *90* degrees, and mixing it with the original signal to extract the baseband information-bearing sequence. This process is shown in Figure 11.

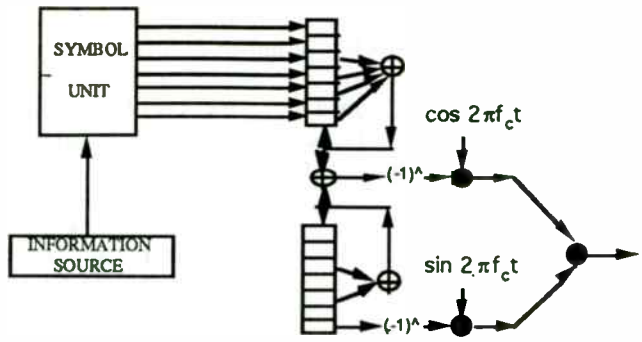

Figure 10. An informationless signal is sent in quadrature with the information-bearing signal. This signal can be used for synchronization and carrier tracking, which is especially important in applications where significant Doppler frequency shifts can occur.

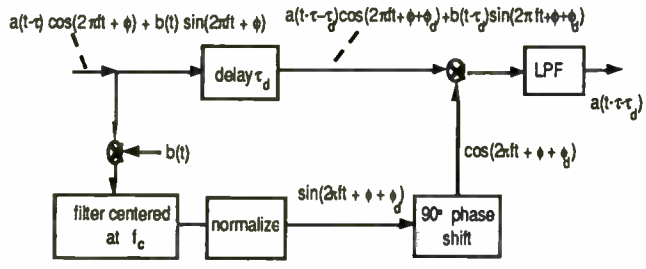

Figure 11. The informationless arm is despread and filtered, amplitude variations are removed, the phase is shifted by 90 degrees, and the resulting estimate of the carrier is mixed with the information-bearing portion of the signal. Delays caused by performing these functions must be compensated prior to mixing.

8. Transmitting multiple sequences simultaneously.

Data rate can be further increased by transmitting multiple sequences simultaneously. Isolation between simultaneously transmitted sequences can be maximized by shifting the phases of their respective carriers, by *90*, *60*, or *45* degrees if two, three, or four sequences are employed, respectively. Illustrations of the technique is shown in Figure 12, where three sequences are transmitted simultaneously at a *60*-degree phase offset, and in Figure 13, where four sequences are transmitted simultaneously on carriers that are *45*-degrees offset in phase. Whatever isolation there was between the sequences due to their cross-correlation properties is increased by *6* dB by the 60-degree phase offsets and by *3* dB by the *45*-degree phase offsets. Of course, an increase in power must be allocated to a user transmitting multiple simultaneous sequences.

The increase in data rate obtained by this technique can be seen by an example. Consider a user that has been

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CODES FOR MULTIPLE ACCESS COMMUNICATIONS

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11/27/93

Multiple access techniques are traditionally divided into three different formats, frequency-division, time-division, and code-division. Recent interest has focused on the technique of code-division multiple-access (CDMA) for use in a variety of wireless applications, notably in cellular personal communications and local-area networks. There are many reasons for this growing interest. First, CDMA does not need to ensure accurate frequency or time-interval separation between users. Therefore, transmissions may overlap in time and spectrum. Secondly, it allows considerable flexibility in the number of simultaneous users transmitting into a given channel. Lastly, it provides superior operating tolerance to both multipath and narrowband interference.

CDMA users are uniquely identified by a code sequence embedded as an address within the carrier waveform. This gives the receiver the capability of selective addressing. To recover a signal, the receiver cross-correlates the sum of incoming signals against an address sequence. This process maximizes the output of the signal matching the address sequence. However, the receiver must know the address sequence in the first place. Therefore, address coding provides communications privacy.

Recovering the desired data requires the received signal to have properties that minimize interference resulting from the presence of other signals. This is achieved by using code sequences that have spectral properties similar to noise. Such sequences when compared are significantly different from each other. Therefore, a lower cross-correlation output results for sequences not matching the desired address sequence. In general, cross-correlation output is the result of similarity or dependence between sequences.

The problem with cross-correlation output is that it appears at the input of the demodulator as multi-access interference. Here the level of interference increases as the number of users accessing the channel increases. Furthermore, the multi-access interference adds to the Gaussian background noise. The result is a lower signal-to-noise (plus interference) ratio at the input to the demodulator. This has the effect of increasing the probability of decoding error, which is the motivation for constructing codes with low cross-correlation properties.

To construct useful codes for CDMA systems, we first need to describe the system. Figure 1 shows a direct-sequence CDMA system, where users are individually transmitting phase-coded signals simultaneously into the same channel. In this system, the user's data sequence is directly multiplied by his address code sequence. The data bandwidth is uniformly spread into a wideband signal by setting the code rate considerably higher than the data rate. A higher code rate allows each data bit to be chipped by the code sequence into many equally probable v^+ and v^- values.

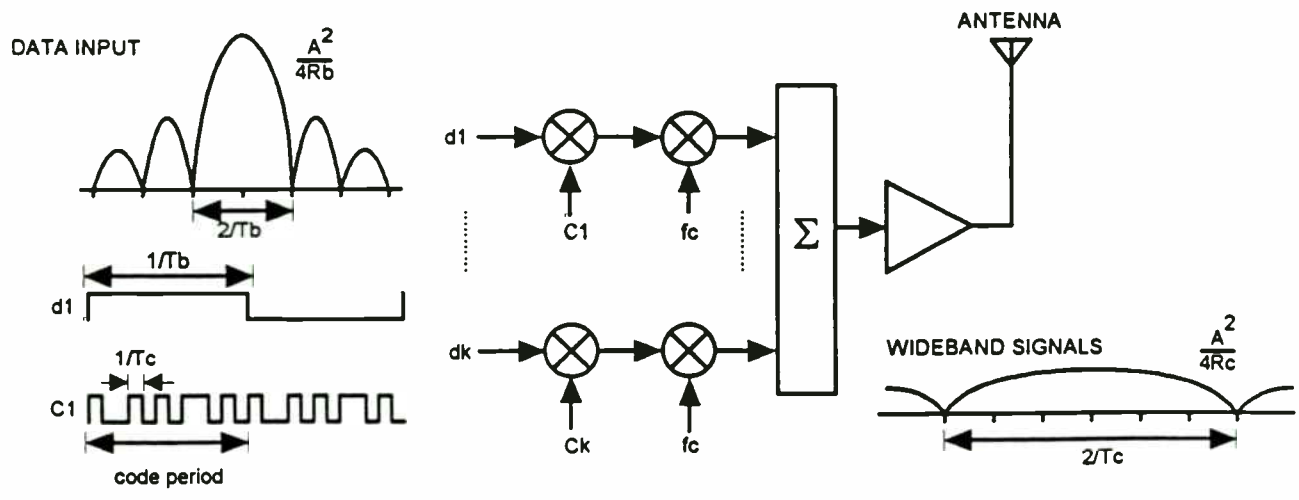


FIGURE-1

If we assume that the transitions of the data and the spreading code are aligned, then each data bit is spread by transmitting it as an *N-bit* code sequence that inverts with the data bit state. Finally, the product phase-shift-keys a common carrier frequency. The phase-coded modulation can be either binary or quaternary.

Thus the transmitted signal for the *k*-th user of a binary direct-sequence system is:

$$s_k(t) = (2P)^{1/2}\, c_k(t)\, d_k(t) \cos(w_c t + p_k)$$

where $c_k(t)\, d_k(t)$ is the product of the code sequence and data sequence of the *k*-th user, p_k represents the phase of the *k*-th carrier, w_c represents the common carrier frequency, and *P* represents the common transmitter power. When we transmit the wideband signal, the signal's power is spread across a bandwidth described by the function $\mathrm{sinc}^2(x)$. This shape is due to the composite sequence having a rectangular pulse shape when it phase-shift-keys the carrier. The act of spreading the data signal into a wideband signal causes the power-spectral-density in the data bandwidth to reduce to a lower density in the RF bandwidth.

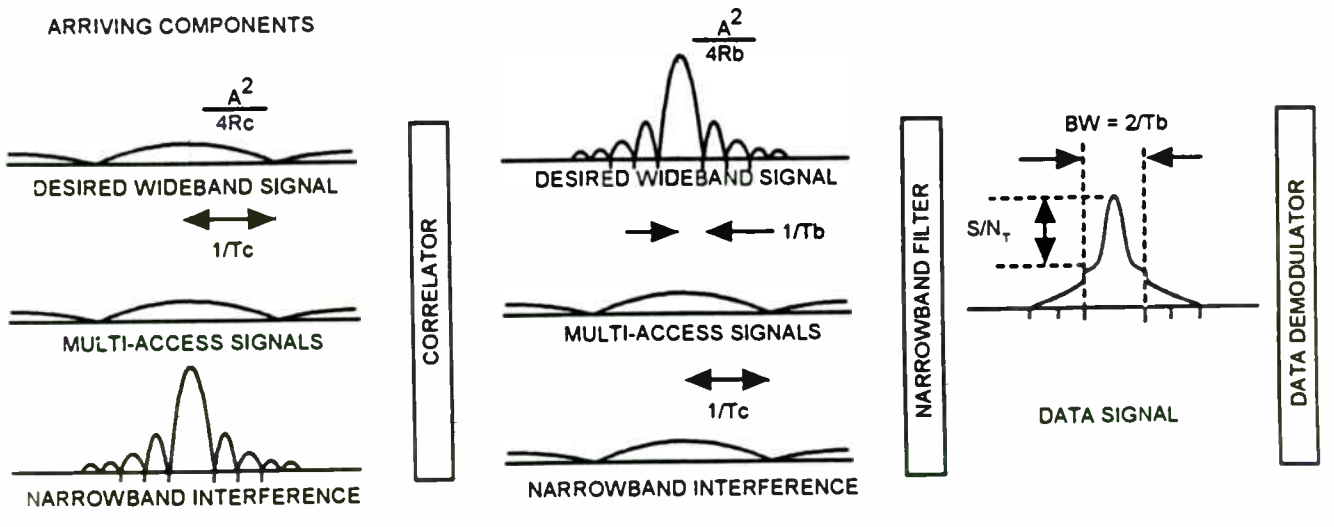
At the input to the demodulator the baseband signal is:

$$r(t) = s(t)\, c_k(t) + i(t)\, c_k(t) + n(t)\, c_k(t)$$

where i(t) is the interference, s(t) is the composite of all *k-users*, and n(t) represents the zero-mean white Gaussian background noise. The correlator multiples each term in the expression by the matching code sequence $c_k(t)$, Figure-2. If the interference is the result of statistically independent narrowband signals the factor $c_k(t)$ in $i(t)c_k(t)$ will spread the interference power over a bandwidth equal to the spreading rate. Since $n(t)$ and $c_k(t)$ are statistically independent of each other, the noise $n(t)$ is unaffected by $c_k(t)$. Therefore, the noise level at the input to demodulator is $N_o/2$, where N_o is the one-sided noise power-spectral-density. The action of $c_k(t)$ in $s(t)c_k(t)$ is to reverse the spreading process, since $[c_k(t)]^2 = 1$.

Now, suppose we have a direct-sequence CDMA system using binary-phase-shift-key modulation and 5 kbps data rate R_b per individual user. Also, suppose we plan to spread our signal over 20 MHz of available RF bandwidth. To achieve the desired RF bandwidth, we set the code rate to allow only the energy in the main lobe to pass through the available RF bandwidth B_{rf}. Thus, the minimum code chip width T_c must equal $2/B_{rf}$ or 100 ns, which yields a spreading code rate R_c equal to $1/T_c$ or 10^7 chips-per-second.

When the receiver, by autocorrelation, processes the wideband signal the total energy in the main lobe of the $\mathrm{sinc}^2 x$ envelope is collapsed into the smaller data bandwidth. Thus the average power spectral density of the received signal is increased by the ratio $R_c/(R_b \log_2 M)$ or 33 dB of "processing gain." Where the term M, is 2 for binary phase-coded modulation and 4 for quaternary phase-coded modulation.



Rc = 4Rb

FIGURE-2
RECEIVER

To fully appreciate the significance of processing gain, assume that the demodulator requires a minimum a signal-to-noise power ratio of 13 dB at the correlator's output. Since our correlator has a processing gain of 33 dB, we maintain reliable detection even when the power of the input noise or narrowband interference is 20 dB above the correlator output signal. Since, direct-sequence wideband signals can be made to have low power spectral densities, it is possible for such signals to overlay the RF spectrum in use by narrowband users without causing noticeable interference to narrowband receivers.

To achieve isolation between CDMA users, it is necessary to select code sequences with properties by which a correlation process would build up the signal of the matching sequence while maintaining low output values for non-matching sequences. Ideally we would prefer code sequences to have zero cross-correlation values and a single maximum self-correlation value when aligned. However, this ideal is not possible in practical binary code sequences. What is wanted here is a list of "pseudo-randomness" properties that a code sequence can be expected to achieve. There are four criteria commonly used in judging the randomness properties of code sequences.

1. The number of ones in each sequence differs from the number of zeros by at most one. That is, a good code sequence has balance.
2. Among the runs of consecutive ones or zeros in each sequence, one-half are of length one, one-forth are of length two, one-eighth are of length three, etc.
3. The self or auto-correlation function of each sequence should show a sharp main peak and uniformly low sidelobes.
4. The cross-correlation values between any two sequences should be uniformly small compared to the peak autocorrelation value.

These properties will be defined further by examining an important class of cyclic code sequences. Our examination begins with maximal-length cyclic code sequences. Such sequences have good randomness properties and are easily produced by generators constructed from shift registers with linear feedback. The number of register stages and feedback connections is defined by the terms in polynomials whose coefficients are one. Not all feedback shift registers give sequences of maximal-length.

Maximal-length sequences are the longest periodic sequences that can be generated by a *m*-stage shift register with linear feedback. A maximal-length sequence takes on all 2^m possible states except the all zero state. Thus, the period *n* equals 2^m-1.

Only a feedback shift-register whose characteristic polynomial is primitive produces maximal-length sequences. The polynomial is primitive if it meets certain mathematical properties. Assuming binary field operations GF(2), a polynomial f(x) of degree *m* is irreducible if f(x) is not divisible by any polynomial of degree less than *m* but greater than zero. An irreducible polynomial f(x) of degree *m* is said to be primitive if f(x) divides X^n+1 but does not divide any X^n+1 for $n<2^m-1$. Finding primitive polynomials is not normally a trivial task. Fortunately, tables of primitive polynomials are available in most coding textbooks [5]. Some primitive polynomials are listed in Table-1.

If one chooses to construct a 31-chip pseudo-random pattern of binary sequences, he may start by selecting a primitive polynomial of degree 5 to produce a 31-chip maximal-length sequence. For example, consider the characteristic polynomial

$$f(x)=X^5+X^4+X^2+X+1.$$

This polynomial is primitive, because f(x) divides $X^{31}+1$ but does not divide any X^n+1 for $n<31$. The number of register stages and the feedback connections is defined by the terms in f(x) whose coefficients are one. Therefore, the maximal-length sequence generator for the above polynomial is as illustrated in Figure 3a. Given a maximal-length sequence generator, a periodic cycle of register states will start repeating when the initial state vector stored in the shift register repeats. Thus, the shift register cycles through 31 states where each state vector consists of 5-chips.

An important characteristic of a maximal-length sequence is its excellent periodic autocorrelation property. For maximal-length sequences the autocorrelation function takes on only two values. A peak value of 2^m-1 at the zero shift point and -1 elsewhere. Autocorrelation shows the degree of self-correlation a sequence has with the shifted versions of itself. This property is important in communications because the receiver acquires code acquisition and tracking by locking onto the maximum or peak

correlation value. When code sequences do exhibit poor autocorrelation properties, offset correlation values or sidelobes will appear at the correlator's output. If large enough, these sidelobes can cause false locking during the code acquisition phase. To find the autocorrelation function of a binary sequence, simply compute the "number of agreements minus number of disagreements" when the sequence is compared term by term with shifted versions of itself.

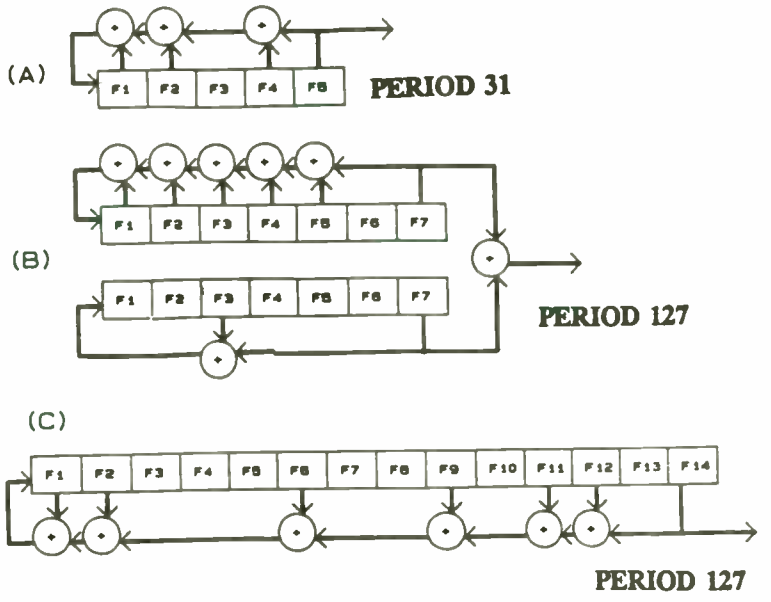
In the direct sequence CDMA system the cross-correlation properties are as important as the autocorrelation properties because multiple users can simultaneously transmit into a common channel. What distinguishes one user from the other is the address code sequence embedded within each carrier. If there is any degree of similarity between code sequences, cross-correlation sidelobes will appear at the output of the correlator. Like autocorrelation sidelobes, cross-correlation sidelobes if large enough can also cause decoding errors.

A preferred set of code sequences should minimize the cross-correlation interference between signals, and the interference between a signal and an echo of the signal found in a multipath environment. Such cross-correlation properties allow the receiver to match the desired sequence while rejecting all other sequences not matching the sender's code sequence. Although maximal-length sequences have excellent

TABLE I. FEEDBACK CONNECTIONS FOR MAXIMAL LENGTH SEQUENCES

PERIOD	NO. OF STAGES (M)	MAXIMAL LENGTH POLYNOMIALS		
31	5	[1] (0,2,5)	[3] (0,2,3,4,5)	
		[5] (0,1,2,4,5)	[11] (0,1,3,4,5)	
		[15] (0,3,5)	[7] (0,1,2,3,5)	
63	6	[1] (0,1,6)	[5] (0,1,2,5,6)	
		[11] (0,2,3,5,6)	[31] (0,5,6)	
		[23] (0,1,4,5,6)	[13] (0,1,3,4,6)	
127	18	[1] (0,3,7)	[23] (0,6,7)	[21] (0,2,5,6,7)
		[27] (0,1,4,6,7)	[15] (0,1,2,3,5,6,7)	[55] (0,2,3,4,5,6,7)
		[47] (0,3,4,5,7)	[3] (0,1,2,3,7)	[11] (0,2,4,6,7)
		[63] (0,4,7)	[13] (0,1,7)	[43] (0,1,2,5,7)
		[19] (0,1,3,6,7)	[7] (0,1,2,4,5,6,7)	[9] (0,1,2,3,4,5,7)
		[5] (0,2,3,4,7)	[31] (0,4,5,6,7)	[29] (0,1,3,5,7)

NOTATION: [15] (0,3,5) → FIELD ELEMENT α^{15} IN GF (2^M)
→ $F(X) = 1 + X^3 + X^5$



a. MAXIMAL-LENGTH SEQUENCE GENERATOR,
b. GOLD CODE SEQUENCE GENERATOR,
c. ALTERNATIVE GOLD CODE GENERATOR.

FIGURE-3

autocorrelation properties, there are a limited number of sequences with good cross-correlation properties. In fact, the available number of sequences is too limited to satisfy most CDMA applications.

CONSTRUCTION OF GOLD CODES

We can construct large families of codes by adding, modulo-2, the outputs of two preferred maximal-length sequences of same length. Such code sequences were developed by Gold [2], however, there are many other sequences such as those credited to Kasami. From a pair of maximal-length sequences with peak periodic cross-correlation magnitude *W*, we can construct a set of sequences with peak periodic cross-correlation magnitude and peak out-of-phase periodic autocorrelation of magnitude equal to *W*. Gold showed that if {x,y} is any preferred pair of maximal-length sequences then G(x,y) has a maximum peak correlation value equal to $2^{\{(m+2)/2\}}+1$, where {r} denotes the integer part of the real number r. The set G(x,y) defines the code sequences resulting from a preferred pair of primitive polynomials of period $L = 2^m+1$. That is, G(x,y) defines

$$(x,\ y,\ x+y,\ x+Ty,\ x+T^2y,\ \ldots,\ x+T^{L-1}y)$$

Gold constructed preferred pairs of maximal-length sequences belonging to G(x,y). These code sequences have correlation functions that take on a three-valued correlation function with values

$$\{ -1, -t(m), t(m)-2 \}$$

where $t(m) = 2^{(m+1)/2}+1$ for m odd,
$2^{(m+2)/2}+1$ for m even.

Thus, Gold code sequences have a bound on the cross-correlation values for any pair of sequences, taken over the full sequence period. Furthermore, a single Gold code set can produce a large number code sequences that take on uniformly low cross-correlation values. Such properties make Gold codes attractive for applications in which many CDMA carriers are present.

A set of Gold code sequences have period 2^m-1 and correlation values no larger than $2^{\{(m+2)/2\}}+1$. From a single Gold code generator, we can produce 2^m-1 non-maximal-length sequences (one for each value of relative phase-shift between the maximal-length sequences) plus two maximal-length sequences for a total of 2^m+1 new sequences. The maximal-length sequences come directly from the output of the individual registers.

To construct a Gold code from a preferred pair of maximal-length sequences refer to Table 1 and note that for degree 7 there are 9 primitive polynomials and 9 reciprocal polynomials. The reciprocal polynomial of f(x) is simply obtained from $g(x)=X^m f(x^{-1})$, where m is the degree of f(x). A Gold code sequence requires that we select a pair of primitive polynomials satisfying the three-valued cross-correlation function. Such a pair is found if the primitive root of sequence $f_t(u)$ is a decimation by q of the primitive root of sequence $f(u^q)$, where $q=2^k+1$ or $q=2^{2k}-2^k+1$, provided $c=\gcd(m, k)$ is such that m/c is odd.

Now that we have formulated the criteria by which preferred pairs are evaluated, we are in a position to construct sets of Gold sequences. It will be helpful to begin by constructing the preferred pairs of primitive polynomials for a Gold code of period 63. Constructing preferred pairs for larger Gold code periods involves some tedious mathematical effort. To construct Gold sequences of period 63, the preferred pair of primitive polynomials must have correlation functions that take on the values in the set {-1,-17,15}.

Hence the maximum cross-correlation for the pair of maximal-length sequences is 17. Since $m=6$ is even, c must be even so that m/c is odd. So we shall select $c=2$ as the greatest common divisor of (6, k), which allows $k=2$. Therefore, the only available decimation values are 5 and 13. However, one will find that decimation by 13 will give the same results as that for decimation by 5.

From Table 1, we find that for maximal-length sequences of degree 6, there are 3 primitive polynomials and 3 reciprocal polynomials. Begin by selecting the primitive polynomial (0,1,6) corresponding to $1+X+X^6$ and noting its field root element u^1 in GF(2^6) is denoted by u[1]. Decimating the element u[1] by 5 we derive the element u[5], which is the root of the primitive polynomial (0,1,2,5,6) = $1+X+X^2+X^5+X^6$. Hence, we have our first pair of preferred maximal-length sequences denoted by G(u[1],u[5]). Proceeding with field root element u[5] and decimating by 5, we derive the field root element u[11] corresponding to the polynomial (0,2,3,5,6) = $1+X^2+X^3+X^5+X^6$ shown in Table-1. We now have our second pair of preferred maximal-length sequences denoted by G([5],[11]) for Gold period 63. Continuing this way, we find that there are 4 additional pairs of preferred sequences. These are listed in Table-2 by their root elements, the corresponding polynomials are found in Table-1.

Using the construction method described above, one can find sets of Gold codes for various sequence periods. To reduce the amount of computations, I have constructed the preferred pairs of primitive polynomials for sets of Gold sequences of periods 31, 63, 127, and 255. These are listed in Table 2. It shows, for example, 90 sets of Gold codes of period 127, constructed from 90 pairs of preferred primitive polynomials, where each set can produce 129 Gold sequences. Hence, the total number of Gold sequences is 11,610 and the correlation functions for these sequences take on the values {-1, -17, 15}.

Note that there are no Gold codes of period 255. This is the result of not finding pairs of primitive polynomials for which the correlation functions take on the values {-1, -33, 31}. However there are other binary sequences of period 255, constructed from a

pair of maximal-length sequences, for which the correlation functions may take on a larger set of correlation values. Some of these are known as small set Kasami sequences, large set Kasami sequences, and Reciprocal sequences.

The correlation functions of small set Kasami sequences take on the values in the set $\{-1, -2^{m/2}-1, 2^{m/2}-1\}$. There are $2^{m/2}$ sequences in a Kasami code, each having a period of 2^m-1. For example, a Kasami code with m=6 has 8 sequences of period 63. Any two of the Kasami sequences of period 63 have a correlation function with a maximum value of 9, while a Gold code with m=6 has 65 sequences of period 63. Any two of the Gold sequences of period 63 have a correlation function with a maximum value of 17.

Reciprocal sequences are pairs of polynomials that include the primitive polynomial and its reciprocal polynomial. Reciprocal sequence generators are constructed in the same manner as Gold code generators. However, Reciprocal sequences have correlation functions that take on a larger set of correlation values.

Let us consider a simple example to see how Gold codes are constructed to meet the need for a wireless Local Area Network that must support a minimum of 20 users. For this application we agree on a direct-sequence CDMA scheme that meets all FCC requirements. To minimize decoding errors, we choose to use a Gold code that bounds the correlation peaks to at least 14 dB below peak autocorrelation. To meet the correlation bound and support at least 50 users, we select a Gold code of degree 7. This code will have 129 sequences of period 127, and a peak cross-correlation value no larger than 17, which is $20\log 2^7/17 = 17.5$ dB below the peak autocorrelation.

To construction the Gold code generator of period 127, select a preferred pair of primitive polynomials from Table 2. For example, select the following pair of primitive polynomials given by G([1], [9])

$$f_1(x)=X^7+X^3+1,$$

$$f_9(x)=X^7+X^5+X^4+X^3+X^2+X+1.$$

First construct the Gold code generator shown in Figure 3b. Here the feedback connections of the two shift registers are defined by the terms of the polynomials $f_1(x)$ and $f_9(x)$. Note the outputs of each shift register is added modulo-2 to produce a Gold sequence of period 127.

From the same pair of primitive polynomials it is also possible to generate Gold codes from a shift register of length $2m$ with connections defined by the terms of the product polynomial $f_1(x)f_9(x)$. Since we are working in the field of integers, modulo-2, all polynomial operations are such that

$$(X+1)(X^2+X+1) = X^3+1.$$

TABLE II. PREFERRED PAIRS OF MAXIMAL LENGTH SEQUENCES OF PERIODS 31, 63, 127 AND 255

PERIOD	PREFERRED PAIRS [a^1, a^2]						# PAIRS
31	[1,3] [1,5]	[3,5] [5,7]	[5,15] [7,1]	[15,7] [3,15]	[7,11] [11,3]	[11,1] [15,11]	12
63	[1,5]	[5,11]	[11,31]	[31,23]	[23,13]	[13,1]	6
127	[1,23] [47,3] [19,7] [1,9] [19,11] [63,55] [1,3] [47,7] 19,23] [1,5] [3,15] [11,55] [1,13] [47,31] [43,27]	[23,21] [3,11] [7,9] [9,13] [11,15] [55,23] [3,9] [7,21] [23,11] [5,19] [15,23] [55,21] [13,21] [31,11] [27,7]	[21,27] [11,63] [9,5] [13,47] [15,1] [23,5] [9,27] [21,63] [11,5] [19,63] [23,31] [21,29] [21,19] [11,1] [7,55]	[27,15] [63,13] [5,31] [47,21] [27,29] [5,43] [27,13] [63,31] [5,15] [63,47] [31,7] [29,9] [19,15] [29,63] [55,5]	[15,55] [13,43] [31,29] [21,31] [29,7] [43,6] [13,29] [31,55] [15,43] [47,27] [7,13] [9,43] [15,9] [63,23] [5,3]	[55,47] [43,19] [29,1] [31,19] [7,63] [6,27] [29,47] [55,19] [43,1] [27,1] [13,3] [43,11] [9,47] [23,43] [3,29]	90
255	None						0

Note: Period 127, G (U [1], U [5]) → [1,5] From Table I → U[1] (0,1,6) and U[5] (0,1,2,5,6)

Therefore, the Gold generator characterized by the product polynomial

$$f_1(x)f_9(x) = X^{14}+X^{12}+X^{11}+X^9+X^6+X^2+X+1$$

is shown in Figure 3c. Furthermore, the sequence output will depend on the initial states of the registers. As stated earlier, there are only 2^m+1 initial starting states that result in 2^m+1 different Gold code sequences.

INTERFERENCE TOLERANCE

In order for the receiver to recover the data message, it must have knowledge of the transmitters spreading code sequence. Given the code sequence the correlator performs a despeading process, which reduces the wideband signal to that of the original data bandwidth. The correlator can be a matched filter whose impulse response is a time reversed replica of the desired code sequence.

In the direct-sequence CDMA system, the matched filter treats narrowband signals as uncorrelated interference whose amplitude is reduced by the processing gain while simultaneously building up the peak amplitude of the desired signal. As for code sequences not matched to the filter, they will cross-correlate to produce an additive multi-access interference term at the output of the correlator. This additive term has the undesirable effect of lowering the output signal-to-noise (plus interference) ratio.

Matched filters are ideal in white additive Gaussian noise channels where the filter maximizes the output signal-to-noise ratio in the sense that it minimizes the probability of error. However they are not optimum in multi-access channels, because multi-access interference has statistical properties that are not Gaussian unless the user population approaches infinite. Yet the analysis of system performance is simplified if the spreading sequences are assumed to be random. Thus, multi-access interference is often modeled as additional broadband Gaussian noise.

Consequently, multi-access interference limits the number of users that can fit in a CDMA system. This is because the more users added to the system, the greater the total cross-correlation interference power. Given that the signals are not perfectly orthnogonal at the corresponding receivers, the maximum number k of users that can be supported in a given RF bandwidth is

$$k = B_{rf}/(2R_b)\ (E_b/N_t)^{-1}$$

where B_{rf} is the available bandwidth and R_b is the data rate per user. Together the terms $B_{rf}/2R_b$ represent the processing gain. The term E_b/N_t represents the energy-per-bit to the noise density ratio required for a specific bit-error-rate. The term N_t represents the total presence of Gaussian background noise, multi-access interference from the (k-1) other users, and if present narrowband interference.

In a wireless radio channel the transmitted signal reaches the receiver from a number of different paths due to reflections. Normally the receiver will synchronize to the strongest signal, as long as the weaker multipath signals arrive delayed by more than a chip interval from the synchronization signal. When multipath delays are less than one chip interval, the multipath signals can combine to distort the autocorrelation peak. In the digital matched filter, the arriving signal slides past the stored replica code sequence until the two are in synchronism (peak autocorrelation), at which point it will exceed a pre-defined threshold setting. At the time of threshold crossing the receiver samples the matched filter output. The sampling should occur once per data bit interval. If multipath signals distort the autocorrelation peak, threshold crossing may occur repeatedly in a data bit interval. As a result the demodulator can receive spurious samples which may cause decoding errors. Such is the case if a direct-sequence BPSK signal, spread by 2 Mchips/sec code sequence, travels to the receiver by multipaths that differ by 197 feet or more. To avoid distortion of the autocorrelation peak, the chip interval must not exceed 200 ns. Thus the code sequence chip-rate must exceed 5 Mchips/sec.

A receiver can distinguish multipath signals if the codes have sharp autocorrelation peaks and uniformly low correlation sidelobes. Furthermore, the matched filter process may be designed to search a window of chips for the maximum correlation peak, wait a full data bit interval, and then resume peak detection in order to reduce the possibility of false triggers occurring before the next bit interval. This is just one of many ways of applying signal processing to the code acquisition problem in multipath environments.

Selecting codes for CDMA applications requires the careful study of code properties, especially autocorrelation and cross-correlation. Codes exhibiting poor correlation properties can interfere with receiver acquisition and tracking functions, and limit the number of users simultaneously accessing the channel. Besides the importance of code properties, the direct-sequence CDMA system suffers from the well-known near-far problem. This problem occurs when the energies of the received signals are very different. That is, if some signals arrive very weak in comparison to others the detector may not reliably recover the data of the weaker signals.

The near-far problem is especially challenging when direct-sequence CDMA is considered for mobile radio applications. The present practice for coping with the near-far problem and multi-access interference has been to use adaptive power control and codes with very stringent cross-correlation properties, respectively. From the literature [6], it appears that, alternative approaches to the near-far problem may come from research on multi-user detection theory. However, no new approach can overlook the importance of code cross-correlation properties.

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Acoustic Echo Cancellation for Digital-Cellular Applications

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Unlike POTS and analog-cellular phones, digital-cellular phones introduce a long transmission delay (> 150 ms) due to speech coding. This delay can make the acoustic and network echos that arise in digital-cellular systems very annoying to users, even for local calls. In some circumstances, this delay can be very long (e.g., >500 ms for a half-rate long-distance call). These delays are so great, that for hands-free operation, conventional voice switching may provide unacceptably-poor performance.

In these cases, echo cancellation is required. While an appropriate solution in theory, however, echo cancellation has been plagued by problems such as instability, poor performance in time-variant environments, and high cost.

Crystal Semiconductor has expended considerable effort to develop algorithms and silicon to solve these problems. Crystal's solution, the CS6400 Echo Canceller, includes a 64 ms echo canceller and a voiceband codec, all in a single 28-pin PLCC package.

DECT and DUCT: Digital cellular telephone with wireless LAN capability

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A TDMA multichannel telephone base station supports up to 12 hand-held cordless telephones which can also be used for data communications. Each channel supports 32 kb/s or up to 500 kb/s if other channels are idle. A two-chip set handles the base station signal processing with the aid of a low-cost controller. The RF block uses assigned 1800-MHz carriers in Europe or spread-spectrum radios on SMR channels in the United States. This paper describes the system implementation and performance.

UV-CURABLE CONFORMAL EMI SHIELDING COATINGS FOR CELLULAR AND CORDLESS PHONES AND WALKIE-TALKIES

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Abstract

Electromagnetic interference (EMI) problems due to crosstalk, radiated emissions and radiated susceptibility result in degradation of performance in cellular and cordless phones and walki-talkies. There is a need for minimizing radiated electromagnetic emissions and improving the overall electromagnetic compatibility of these systems and devices. There are three electromagnetic interfernece problems with these devices, namely, (a) crosstalk which is the unintentional coupling of lectromagnetic waves between adjacent signal traces and adjacent circuits, (b) radiated elctromagnetic emissions PC board performance due to elctromagetic emissions from neighboring PC boards and (c) radiated susceptibility which is the degradation in these devices due to elctromagnetic radiations originating from distant sources (communication links, radiao transmitters, etc.)

In this paper, a new generation of conformal EMI shielding coatings will be presented. These coatings contain silicone, polyurethane or hybrid resin as backbone structure with chiral side groups. They do not have d.c. conductivity for shielding, but induce delocalized electron movement in the molecular chain when electromagnetic wave interferes with the coating. Conformal coatings can be heat-sured or ultraviolet(UV)-cured. Advantages of UV-curing include rapid cure times, energy efficiency and processing flexibility.

Experimental results will be presented with walkie-talkies and a demonstration will be done in the Symposium.

New technology for low-cost RF connectors

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Traditional methods for the design and construction of RF connectors is no longer cost effective for low-cost connectors. New markets for LANs, consumer products, and other high-volume, cost-sensitive applications require the use of new technologies. This paper will examine some of the new manufacturing methods and the impact on the performance of the connector interface. Zinc diecasting, injection molding, cold-heading, and progressive die stamping will be examined as alternatives to the traditional screw-machine connectors.

The impact of these new methods will be reviewed as they relate to the mechanical, electrical, and environmental performance of connectors using these new methods versus their traditional equivalents. A discussion on the quality performance will be included.

It is the intention to demonstrate that low-cost products can be more cost effective in many applications, and that an understanding of their limitations will allow proper product specification.

Wireless Measurement Strategies

Session Chairperson: Thomas Brinkoetter,
Tektronix, Inc. (Beaverton, OR)

Testing GSM Mobile Phones

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Summary

Mobile phone networks based on the European GSM standard have been in full operation for almost two years now. With well over 1 million subscribers in this short time, a remarkable rollout rate has been achieved. One of the critical factors during the start-up phase was the availability of adequate testing facilities for the mobile terminals. Not only was a rigorous type-approval regime necessary to meet the requirements of multinational market introduction, there was an equally pressing need for high-throughput testing in the production area. With the installed base growing rapidly, the repair and maintenance sector is also beginning to grow. This paper briefly describes the novel aspects of the GSM radio interface and the measurement tasks arising from them. It concludes with a review of Rohde & Schwarz test equipment for the various applications.

Historical development

With the growth of conventional analog cellular radio networks within Europe it became clear at an early stage that plans were needed for a future system of much greater capacity. A further aim of such a system was to provide international compatibility to replace the patchwork networks of the analog era.
The breakthrough came in 1982 with the formation of a special working committee - the Groupe Spécial Mobile (GSM) - within the conference of European telecommunications administrations (CEPT). The work of this committee was put on solid footing by the establishment of a Permanent Nucleus (PN) based in Paris in 1986. This was soon followed by the commitment of the European nations to the project by the signing of the GSM Memorandum of Understanding (MoU) in May 1987. Standardization work goes on today under the auspices of the European Telecommunications Standards Institute (ETSI). Since early 1992 some 25 operators in 18 countries have introduced new services under the revamped GSM acronym now standing for the **G**lobal **S**ystem for **M**obile Communications.

ETSI has also issued a complementary standard (DCS 1800), describing a 1.8-GHz variant of the GSM network intended to be used as the basis for Personal Communication Networks. Operators in the UK and Germany have already been licensed and are working on their new networks today.

The GSM Radio Interface

The entities of the network (FIG 1) are interlinked via standardized interfaces. In order to achieve a manageable structure both in the work of standardization and during the engineering phases, these interfaces follow the protocol guidelines of the Open Systems Interconnection (OSI) layer model (FIG 2).

On the wireline side these interfaces can, for the most part, be tested using well-established protocol analyzers and other line testers. Major new challenges were presented by the unique radio interface (known as the U_m interface). This paper will

thus concentrate on the special aspects of the radio interface and how testing solutions have been worked out.

Our exposé of the radio interface starts at the physical level, or the OSI layer 1.

The mobile stations transmit at frequencies between 890 and 915 MHz, the base stations between 935 and 960 MHz. RF channels are spaced at intervals of 200 kHz. In addition to the duplex spacing of 45 MHz in frequency there is also a time displacement of 3 time slots between transmission and reception.

The TDMA Structure

Time division multiple access (TDMA) and frequency division multiple access (FDMA) are both characteristic of the GSM system.

The basic transmission element on the RF path is the timeslot. A normal burst (signal packet) occupies the timeslot in such a way that the useful information is contained in two blocks of 57 bits each (FIG 3).

The signalling flags (F) indicate the status of these information blocks. In a traffic channel, the information will normally be a representation of speech or user data. Under certain circumstances, such as when changing channels, additional capacity is required for signalling. This additional capacity can be had by "stealing" information blocks normally used for speech. The flags are thus known as "stealing flags", because they indicate this special use of the information blocks.

The guard time (G) of 28 µs (or 8.25 bit periods) gives the mobile station time to switch the RF power on and off. A precise power ramping mask has been specified to regulate this behaviour.

The tail bits (T) and the training sequence (TS) are known at the receiving end in advance and thus form a frame from which exact timing information can be derived. By the use of signal processing techniques such as crosscorrelation, the receiver can use the training sequence to take a snapshot of the transmission characteristics of the RF channel. This process is known as equalization and permits the distorted information bits to be interpreted in order to recover the useful content of the message.

There are several types of burst. A timeslot is usually filled by a normal burst. When first transmitting into the network, however, the mobile stations use a shortened access burst. This ensures that the unsynchronized bursts from the MS do not overlap into adjacent timeslots at the BS receiver. Other standard bursts are the frequency correction burst and the synchronization burst.

Systematic changes of frequency are used in GSM to compensate for dips in fieldstrength caused by multipath reception. This frequency hopping is based on a hopping sequence agreed between the base station and the mobile and thus also provides security against eavesdropping.

Physical and Logical Channels

The term physical channel is used in the GSM standards to specify a sequence of timeslot (which may be at different frequencies of hopping is used) in which communication between a base station and a mobile takes place. Full-rate channels

occupy one timeslot in each frame or one timeslot in eight. Half-rate channels are also possible, using one timeslot in every second frame.

Logical channel is the term used for specific functions. Several logical channels will generally be combined according to well-defined multiplex scheme within a physical channel. The logical channels can be divided into traffic and control channels.

Traffic channels (TCH) carry digitized speech or used data. A further distinction is made on the basis of the data transmission rate. Two rates have been defined for speech channels:

- Traffic channel with full-speed data transmission (full-rate TCH) with a data rate of 22.8 kbit/s
- Traffic channel with half-speed data transmission (half-rate TCH) with a data rate of 11.4 kbit/s

In data transmission services the user can also choose full or half-rate channels and may also specify data rates from 2.4 kbit/s to 9.6 kbit/s.

Control channels are provided to carry signalling and synchronization information.

The broadcast channels send frequency correction information to the mobiles and permit them to synchronise to the frame pattern. Once a mobile has identified the base station and synchronized to it, it reads further information about the base station from the broadcast channels. The common control channels are used for the first exchange of information during call setups for example. Calls are completed on special dedicated control channels. These dedicated channels transfer information between base station and mobile before and during the voice or data connection.

Coding, interleaving, ciphering

Coding is used to protect the logical channels against bit errors occuring during transmission. Three types of coding are commonly used:

- block coding, to permit fast recognition of errors
- convolution coding for error correction
- interleaving, to compensate for the typical bursty nature of the errors

The coded data are systematically reordered and divided into eight subblocks, each transmitted burts consisting of two subblocks. By means of block-diagonal interleaving these subblocks are further mixed with those of adjacent speech frames.

By **ciphering** the transmitted data, protection against eavesdropping is provided. During the authentication phase, the mobile receives a ciphering key sequence number from the base station. Once the mobile responds correctly the ciphered transmission can start.

Mapping

The protected, ciphered bits of the logical channels are finally multiplexed together to form a single bit stream - the physical RF channel.

This process is known as mapping and determines the combinations of information present on each physical channel. Thus a control channel may carry a combination of:

- Frequency Correction CHannel (FCCH),
- Synchronization CHannel (SCH) for frame synchronization and
- Broadcast Control CHannel (BCCH) for BS identification.

In a typical traffic link, the actual Traffic CHannel (TCH) will be multiplexed together with monitoring information in a Slow Associated Control CHannel (SACCH).

The higher layers

The data link layer of GSM, layer 2 of the OSI model, is responsible for safe transport of data telegrams from one side of the link to the other. It uses a number of mechanisms to this end, including an acknowledgement procedure. It is realized as an intelligent processor unit making a large number of decisions in real time.

Layer 3, the network level of the OSI model, also specifies an intelligent exchange of data telegrams between communicating parties.

Each data telegram handshake causes the link to go into an appropriate well-defined state. These states are the basis for handling the communication services such as speech, video or data transmission.

In this context, we encounter terminology that is familiar from analog cellular radio networks:

- Registration
- Call setup by the mobile subscriber
- Call set up by the fixed-network subscriber
- Call clear-down
- Channel changeover in side cell or to another cell
- Power control levels
- Queue mode

The Measurement Challenge of GSM

These novel radio access techniques require test functions that cannot be handled by conventional equipment. As far as test and measuring equipment is concerned, the main differences between conventional mobile radio and the new digital radio network can be categorized in the following way:

- The transmitted information is completely digitized and assigned to time slots. Continuous analog signals that were employed for testing in the past would obviously be out of place in this digital environment.
- Modern digital modulation techniques affect the phase and amplitude of the RF carrier continuously over time. Generating digital signals of this kind, or analyzing them, is beyond the capabilities of conventional test equipment such as signal generators, modulation analyzers and power meters.

- The transmission of information blocks in precisely defined time slots is another challenge for test equipment. To work correctly, TDMA requires precise synchronization between the radio stations involved. Timing advance is the term used to describe the synchronization mechanism used (FIG 4). As far as testing is concerned, the test sets must be able to operate in synchronism with the data streams flowing in the network. Sampling rates which are several times greater than the data rate are required to obtain satisfactory time resolution.
- The amplitude range of radio signals also poses problems for the measurement equipment. There can be differences of up to 70 dB between maximum transmission power and power off. Conventional A/D-converter technology is, therefore, being stretched to its limits.
- Frequency hopping, even at relatively low rates, requires new features in the test instruments. Depending on the measurement to be made, it will be necessary to generate or analyze signals of this kind.
- With the introduction of compressed speech coding, conventional AF measurements have become a thing of the past. Single-tone test signals do not approximate speech very well. In this field, new test methods have thus been introduced, combining analog and digital aspects.

The Basic Measurements

Physical-layer Receiver Measurements

Signal-generator characteristics

Signal generators for GSM applications convert a given bit sequence into the corresponding modulated RF carrier signal. Conventional signal generators are unsuitable for this because there is no direct way of controlling the phase of the carrier. Modern generators use I/Q modulators (In-phase/Quadrature phase) to provide this function (FIG 5).

Fast digital signal processors are used to condition the (analog) I and Q modulation signals. These processors replace classic "analog" functions such as filtering or integration by equivalent digital processes which increase precision and stability as a function of time and temperature.

As the I/Q modulator itself is still analog, this circuit largely determines the accuracy of the signal generator. In addition to the usual quality criteria for signal generators, three more must now be considered: I/Q imbalance due to unequal gains in the two modulation paths, skew caused by a phase difference between the carriers differing from exactly 90° and the residual carrier component in the output signal.

Simulation of the radio channel

The simulation of multipath reception (fading simulation) is becoming more and more important in the testing of digital radio systems, particularly at the type-approval stage.

Fading simulators for GSM tests must be capable of electronically simulating the propagation conditions over various types of terrain. The effects of the speed of the

vehicle must also be built into the simulation model, ranging from 3 to 50 km/h in the city to 100 km/h in hilly country or even 250 km/h on fast open roads.

In the fading simulator, the signal is first split into several paths. Each path contains simulated loss, delay and modulation (Doppler effect) functions. Finally the signals are recombined, before being fed to the receiver under test.

Sensitivity measurement

The sensitivity of the receiver is a crucial GSM parameter, as it is for other types of radio system. As measurements directly after the demodulator are, in general, not possible and would in any case give different results for different designs, GSM test methods which do not involve opening the radio set have been defined. The loop back method, effectively makes the radio part of the test setup. If the decoder in the receiver detects an errored telegram (incorrect parity check), this fact is reported to the test set by the radio's own transmitter. This is indicated by a bad-frame indication (BFI) in the transmit telegram.

This leads to three new test parameters which, depending on application, can be used as a measure of transmission quality:

- BER (bit error rate - number of bad bits found in the transmission as a whole)
- FER (frame erasure rate - number of bad frames)
- RBER (residual bit error rate - BER measured only in the "good" frames).

As these measurements are carried out on the logical GSM channels (e.g. traffic channel, control channel), very long measurement times may result under certain circumstances because of the various data rates and the required BER values.

Other receiver measurements

The quality criteria (BER, FER, RBER) described above replace the parameters S/N and SINAD of analog radio systems. With regard to the reception quality, other well-known receiver measurements are also carried out:

- co-channel rejection
- adjacent-channel rejection
- blocking
- spurious responses to 12.75 GHz

In most cases, the interfering signal generator has to meet stringent spectral purity requirements. Depending on the test method, unmodulated or GSM modulated static or frequency-hopping interference generators are required.

A special case of adjacent channel measurement is worthy of mention. Because of the TDMA principle, there are adjacent channels in both the frequency domain and the time domain.

This has led to the introduction of a new measurement called

- adjacent-time-slot rejection.

This measurement is carried out implicitly by defining an appropriate level for the adjacent time slots when sensitivity measurements are carried out.

Physical-layer Transmitter Measurements

Signal analysis

Conventional power meters and modulation analyzers can only handle settled (static) test signals. This means they cannot be used to analyze signal packets (TDMA bursts).

Even the latest display units for analyzing digitally modulated signals (constellation analyzers) are of limited use.

A precise analysis of dynamic behaviour can only be obtained by fast sampling of the RF signal or the corresponding I/Q signals. By storing these samples in a memory of sufficient size, they can be post-processed for comprehensive and flexible analysis of the transmitter (FIG 6a/6b).

In-channel measurements

Some of the most important measurements on digitally modulated transmitters are:

- power levels (down to 13 dBm for the MS)
- power ramp-up and ramp-down using stipulated tolerance mask
- phase noise, measured as the deviation from the ideal phase curve
- frequency offset, also derived from the phase data

Measuring transmitter spectral components

The spectral components near the carrier are specified by a mask. Due to TDMA, the transmitted signal is not continuous, however, so that the measurement cannot be made by simply connecting up a spectrum analyzer. This difficulty can be overcome by **triggering** the spectrum analyzer in synchronism with the TDMA frames and displaying the results in zero-span mode. Further spectrum analyzer settings are given in the specifications, a distinction being made between

- **spectrum due to modulation**
  measurements in the central (modulated) section of the burst with resolution BW = 30 kHz, video BW = 30 kHz, average mode
- **spectrum due to switching**
  measurements at the edges of the burst with resolution BW = 30 kHz, video BW = 100 kHz, max.-hold mode

Spurious transmissions up to 12.75 GHz must also be checked.

Signaling Measurements

Above the physical radio layer, the GSM standards follow the OSI model in providing for data exchange mechanisms and protocols in layers 2 and 3 to ensure secure signaling within the network. Equally complex, although not strictly-speaking covered by the OSI conventions, are the coding of speech and user data in the traffic channels.

Test equipment is required to simulate and/or analyze these data exchanges in order to fully exercise the devices under test. This calls for processing speed and power unknown in classical RF test gear. Multiple digital signal processors will typically be needed to handle the data flow in real time. It must be remembered that test equipment makers generally cannot take advantage of custom large-scale integrated circuits in the way the terminal or infrastructure manufacturer may do. One reason is that the limited market size will not justify the high investments required. On the technical side, it also turns out that test gear is often needed to be much more flexible than the radios themselves, so that access to the protocols and messages is needed in a manner not achievable in high-volume custom solutions.

Practical Test & Measurement Solutions

Each stage in the engineering process places its own demands on performance, flexibility, speed and price of the equipment used for testing. In the GSM arena, four major application areas have appeared: design engineering, type-approval testing, production testing and the installation, repair & maintenance market.

At Rohde & Schwarz we identified a number of generic requirements for GSM test equipment. These functions are made available in today's family of instruments on an as-needed basis.

- GSM message handling. A powerful software tool - called the message editor - may be used to define specific messages. Thanks to the use of an intelligent data base, the user is saved much of the trouble of referring to the GSM specifications.
- Layer 3 (network) signalling sequences for simulation of call connection and management procedures can be user-specified.
- Layer 2 (data exchange) mechanisms. Besides automated (correct) data link operation, error implantation is often needed for simulation of practical transmission problems.
- Layer 1 coding functions. Binary data are coded and interleaved for protection against transmission errors. Ciphering further ensures confidentiality of the user traffic.
- Logging of signalling activities. Due to the speed and complexity of the signalling process, the only way to locate protocol trouble spots is to record interface activity in a large memory. Once again, it is the task of comfortable software to present the logged protocol in an understandable fashion for rapid and meaningful analysis (FIG 7).
- Layer 1 physical transmission functions. Modulation and demodulation, frequency hopping and power ramping all have to be simulated and analyzed in the test equipment.
- Speech coding/decoding. The final test of a GSM radio comes when the voice connection is established. Vocoder functions in the test set ensure that true-to-life speech tests can be made on the finished radio before delivery to the customer.
- GSM-specific RF measurements. Receiver sensitivity based on BER tests, transmitter power-ramping and phase-noise performance: these tests are best

handled by high-speed digital signal processors in order to achieve accurate results in acceptable times.

- Synchronization facilities. With its timebase of 13 MHz and its complex TDMA structure of frames and multiframes, the GSM network poses some special problems in the synchronization of instrumentation. New equipment provides GSM-specific timing inputs/outputs, while powerful accessories also permit existing instruments with the usual 10-MHz sync to be tied into GSM test setups.

Design Engineering

Highest requirements on flexibility and accuracy usually lead to the choice of single high-performance instruments such as signal generators and spectrum analyzers. The new RF measurement methods of GSM made special models and software add-ons for these standard products essential. Furthermore, the complexity of the GSM signaling and the tight timing requirements were sufficient reasons to introduce special-to-type testing platforms, integrating transmit, receive and signaling functions.

Type-Approval Testing

The extreme complexity of the GSM type approval test systems was written-in by the standards makers. GSM being a new and extremely complex network It was understandable that no chances should be taken.

The contract for the design and development of a mobile station type-approval test system (known appropriately as the System Simulator) was awarded by the MoU group to Rohde & Schwarz, who thus became the sole authorized supplier of such test stations (FIG 8).

The sheer complexity and lack of maturity of the standards led to inevitable delays in the validation of the individual "test cases" used to verify the functionality of the mobile station.

Concerned about delays in reaching market, the operators pushed for an abbreviated type-approval process, involving a reduced number of tests: Interim Type Approval. Once again, Rohde & Schwarz was identified as the only company with the knowhow and capacity to meet the tight schedule. After a massive efforts on all sides, the first GSM mobiles achieved interim type approval in the spring of 1992. Since a time limit was set on the validity of interim approvals, initially to the end of 1993, it is to be expected that only fully type-approved mobile stations will be taken into service as of January 1994.

Production Test

With the mixed prospect of a mass market and tumbling prices, the manufacturing industry was driven by cost-saving measures from the start of GSM. A major target of these saving efforts was the test bay. Digitization and large-scale integration contributed to minimizing test requirements, but for the critical RF parameters of power, modulation and receiver sensitivity there was really no alternative but to test. With speed being of the essence, successful production test tools will be fast and easy to use, especially under remote control.

Installation, Repair and Maintenance

Portability was not a virtue of the first generation of GSM test sets.

With the infrastructure now in place and over a million terminals with the subscribers, there's currently a need for test gear that can be taken out into the field (FIG 9). This calls for compact, light-weight equipment. Ease of operation counts high on the list of priorities for testers to be used by personnel not trained in-depth in the intricacies of GSM.

Illustrations

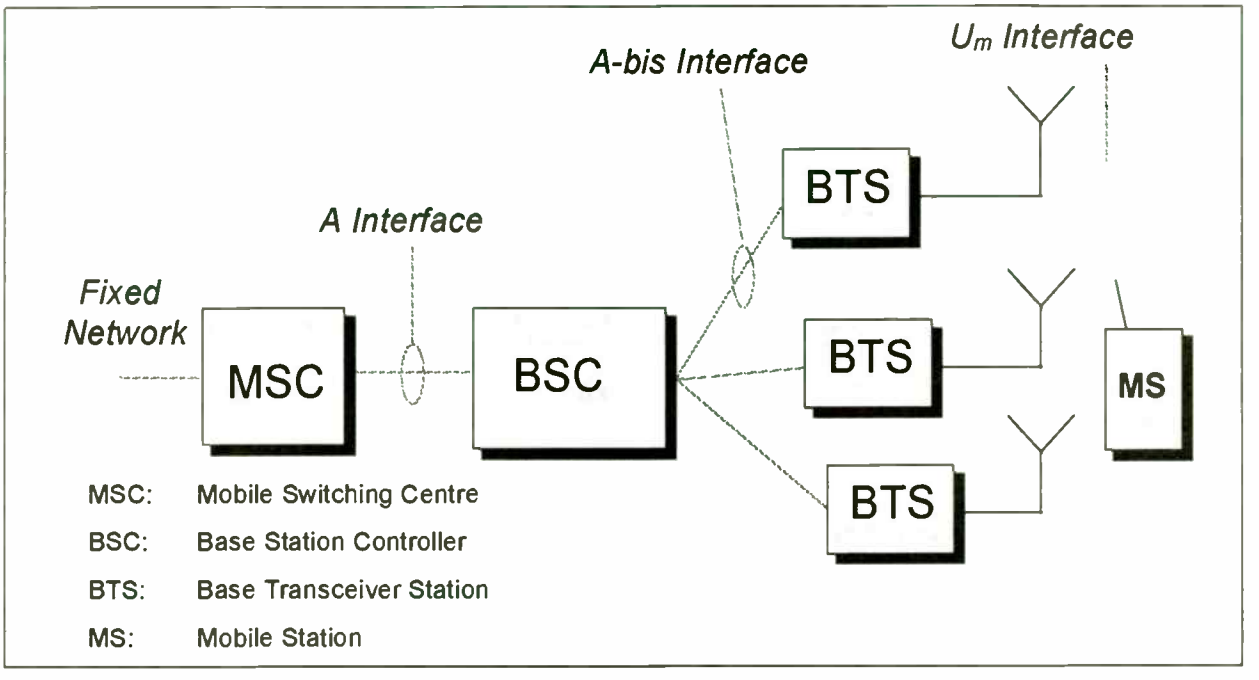

FIG 1: The GSM Network Architechture

Layer 7: Application	
Layer 6: Presentation	
Layer 5: Session	
Layer 4: Transport	
Layer 3: Network	GSM Network Control
Layer 2: Data Link	$LAPD_m$ Protocol
Layer1: Physical	RF Modulation, Hopping, Coding, TDMA

FIG 2: The Open Systems Interconnection Model applied to GSM

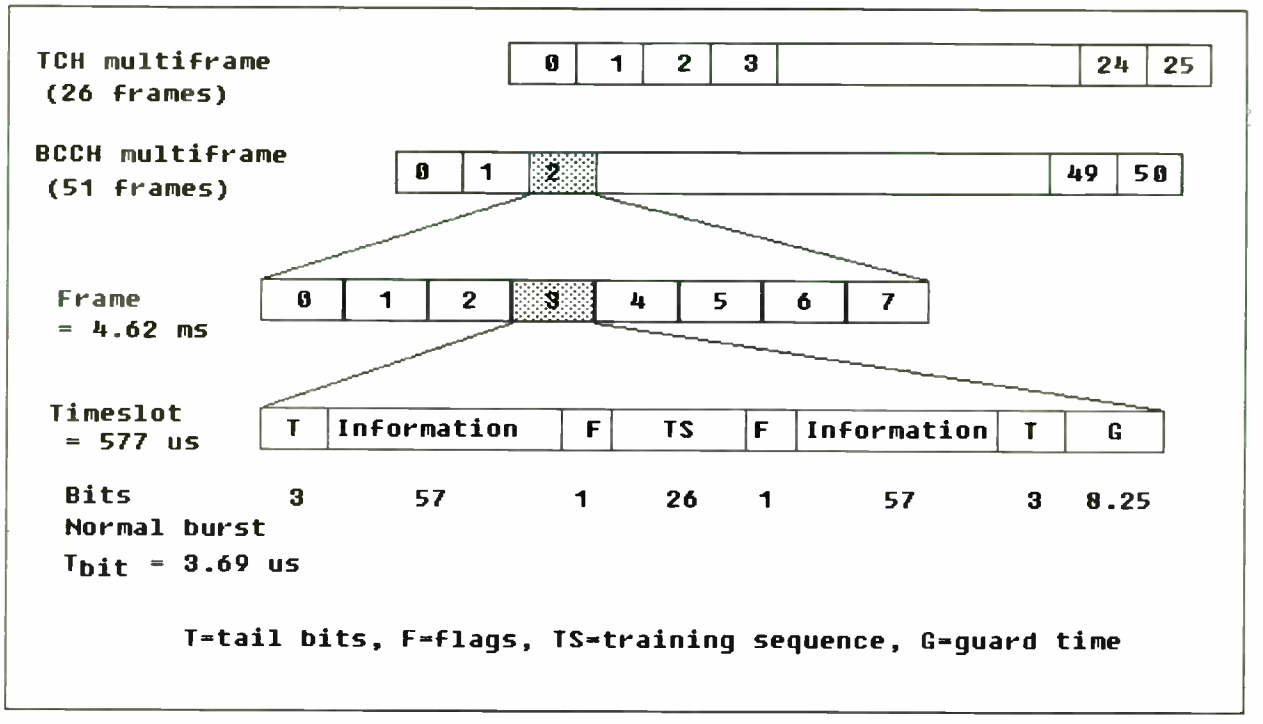

FIG 3: The TDMA Structure of GSM

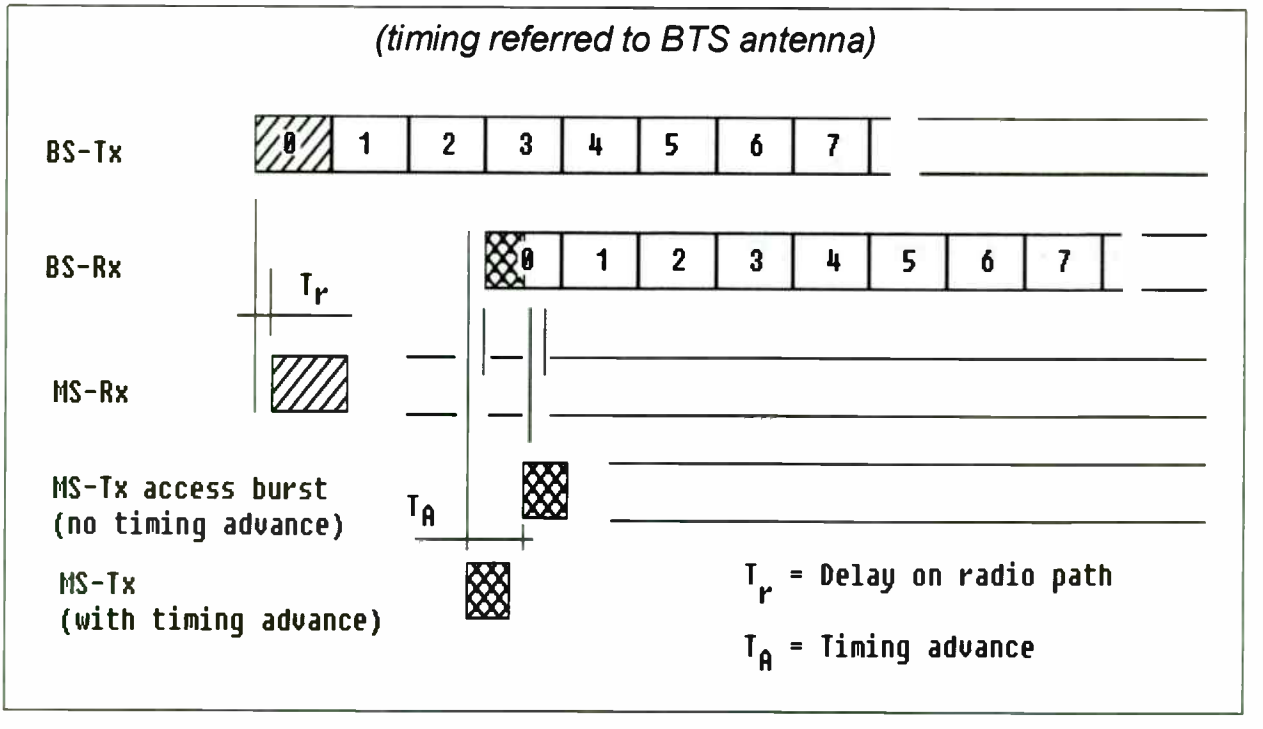

FIG 4: The Timing Advance Mechanism

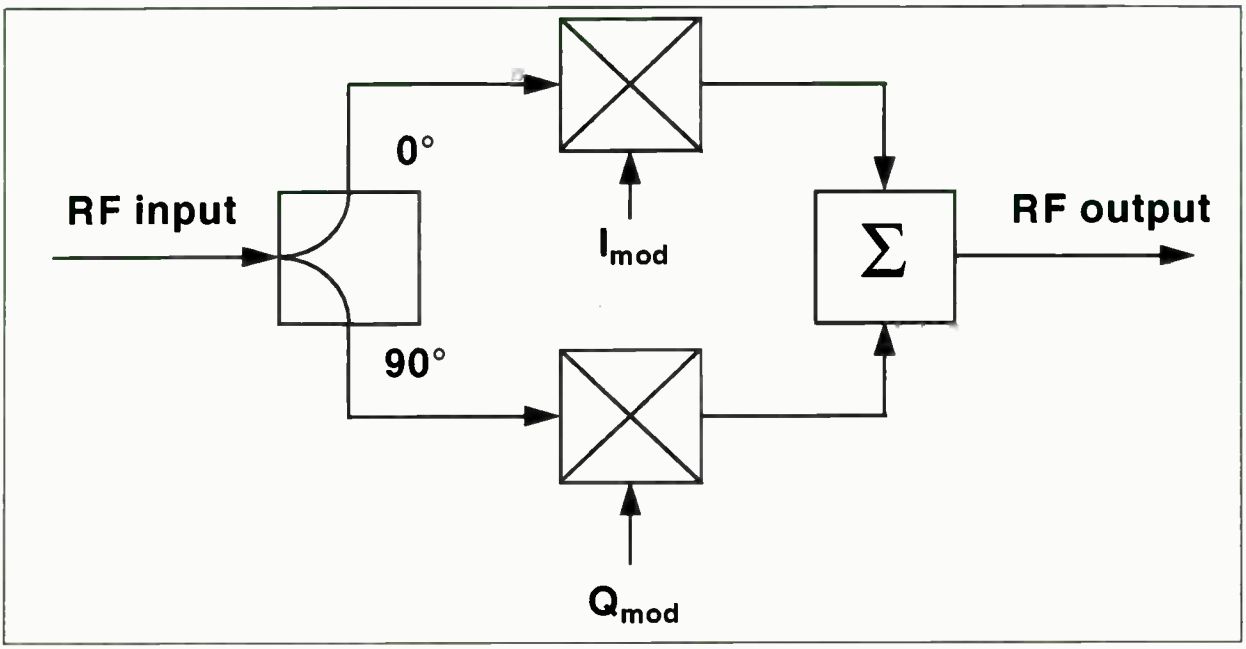

FIG 5: The I/Q Modulator

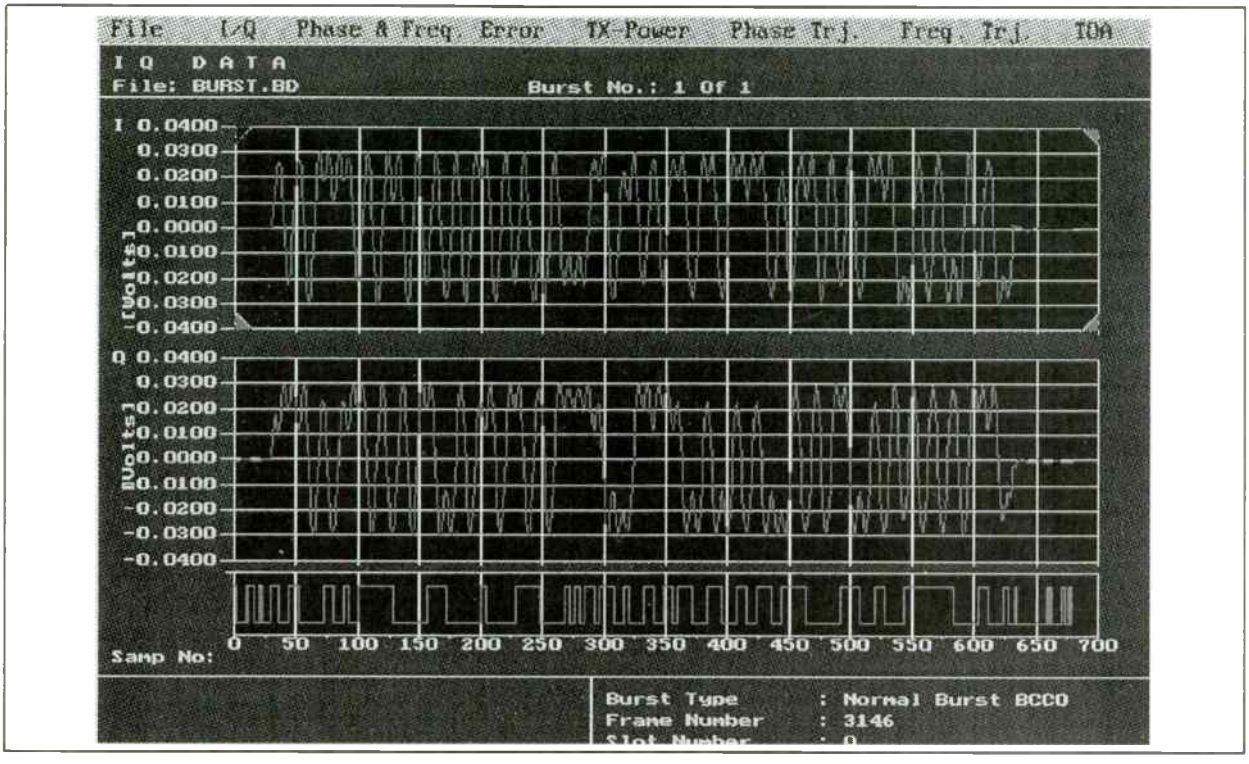

FIG 6a: Recorded Samples of an RF Signal Shown in an I/Q Representation

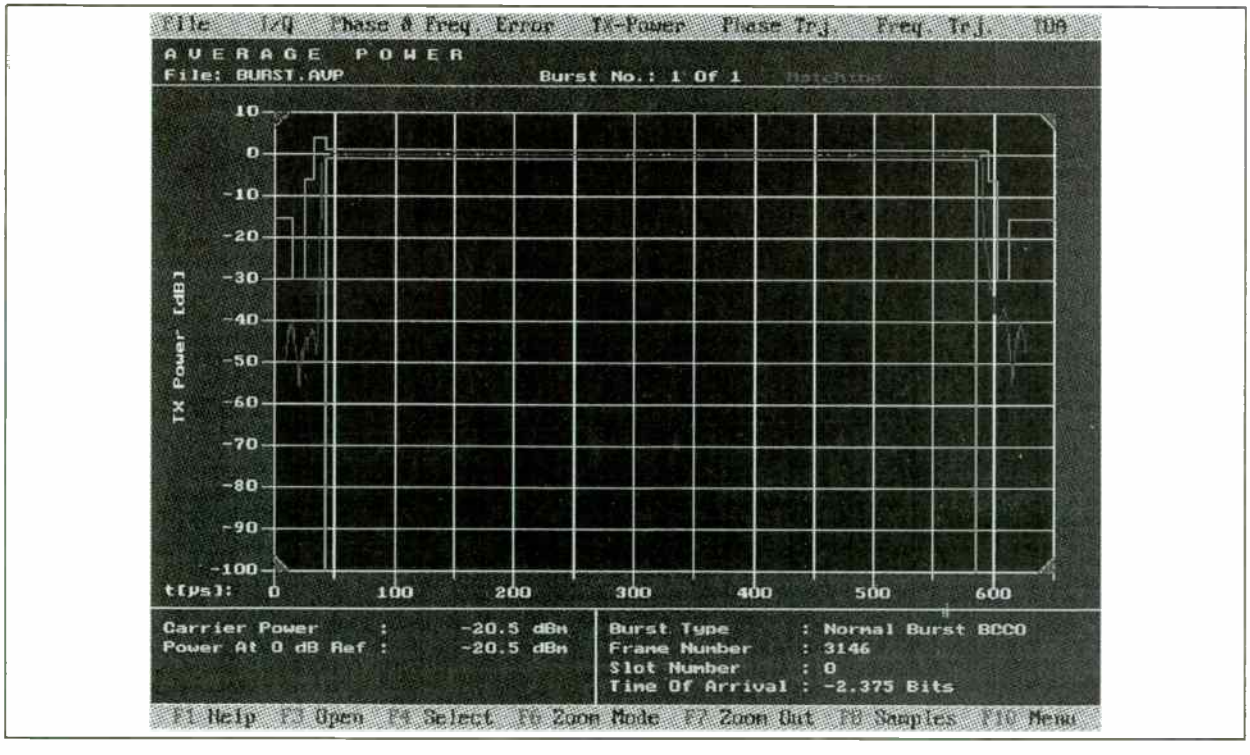

FIG 6b: Power-ramp Measurement on a Sampled RF Signal

File Edit Buffer Log

	Log - Mnemonic	Bs	Chan	Channel	Frame Number
RX	DL-RA-Ind	0	0	RACH	6433
TX	Immediate Assignment	0	0	AGCH	6461
RX	CM Service Req	0	1	SDCCH	6495
TX	Authentication Req	0	1	SDCCH	6582
RX	Authent Response	0	1	SDCCH	6648
TX	Ciphering Mode Command	0	1	SDCCH	6735
RX	Ciphering Mode Complete	0	1	SDCCH	6801
RX	DL-Establish-Ind	0	1	SDCCH	6852
RX	CP-Data	0	1	SDCCH	6954
TX	CP-Data	0	1	SDCCH	7500
TX	CP-Ack	0	1	SDCCH	7551
RX	CP-Ack	0	1	SDCCH	7566
TX	CP-Data	0	1	SDCCH	7602
RX	CP-Data	0	1	SDCCH	7617
RX	CP-Ack	0	1	SDCCH	7668
TX	CP-Ack	0	1	SDCCH	7755
TX	Channel Release	0	1	SDCCH	7857
RX	DL-Release-Ind	0	1	SDCCH	7923
RX	DL-Release-Ind	0	1	SDCCH	0
TX	Paging Req Type 1	0	0	PCH	11667

F1-Help F2-Save F3-Load F4-Expand F5-Contract F8-Buffer/Log F10-Menu

FIG 7: Signalling Measurements - The Message Log at Layer 3

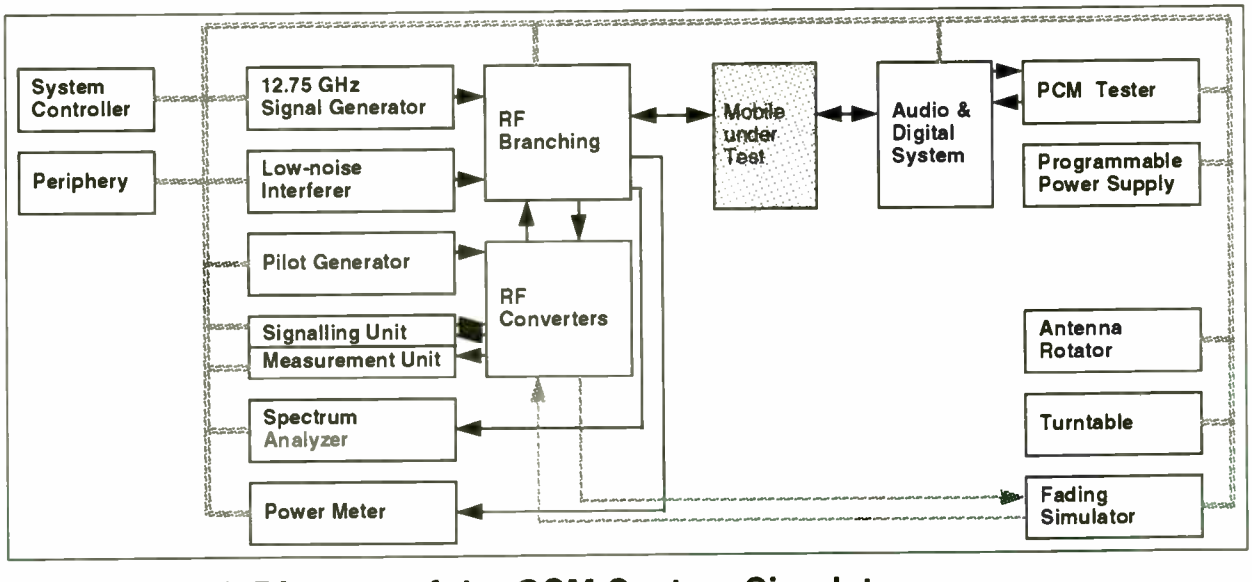

FIG 8: Block Diagram of the GSM System Simulator

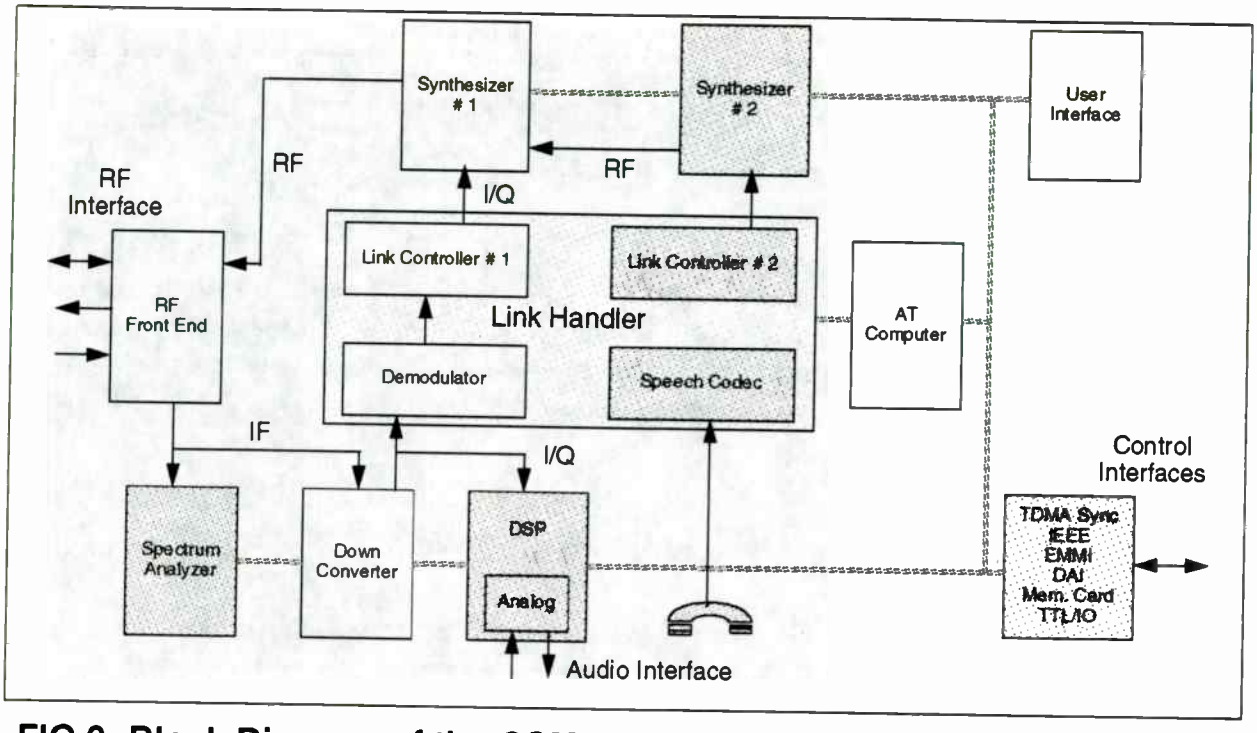

FIG 9: Block Diagram of the GSM Tester CMD

MULTI-TONE IMD MEASUREMENT ACCURACY IS ASSURED WITH PHASE-ALIGNED TEST CARRIERS

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As RF communication systems compete for cost effective operation, designers have focused on the circuitry that can handle multiple RF carriers. Intermodulation distortion (IMD) products that are generated by multi-carrier systems can not be accurately measured using standard two-tone techniques. A signal generator designed especially for multi-carrier IMD measurements provides measurement accuracy not possible from standard test setups.

Multi-carrier communications systems can be designed for cost effectiveness by utilizing amplifiers and other circuitry capable of handling multiple RF carriers. As an example, cellular radio "cell sites" may broadcast up to thirty-two carriers simultaneously. Rather than combining the outputs of thirty-two individual transmit amplifiers, a single amplifier may be used (see figure 1).

When an amplifier processes more than one carrier, intermodulation distortion (IMD) products are generated. The IMD products appear as spurious signals at multiples of the frequency spacing between the carriers, causing interference in adjacent channels or other frequency bands. For this reason regulatory agencies have placed strict limits on the amplitude of IMD products; typical specifications range from -60 dBc to -80 dBc.

IMD products must be accurately measured in the design and manufacture of multi-carrier linear amplifiers. A true worst-case test must be used to account for all possible field conditions. Otherwise, it is possible that an amplifier which passes a factory IMD test will be returned from the field at a later date due to excessive IMD products.

Peak power handling capability of multi-carrier amplifiers is also of primary concern and must be measured accurately. Since the instantaneous peak power level in a multi-carrier transmission can far exceed the average power level, multi-carrier amplifiers are subject to limiting and even burn-out if instantaneous peak power exceeds the expected limits.

Standard IMD measurement techniques, using combined phase locked frequency sources or free-running oscillators, will not provide a worst-case IMD measurement. When more than two carriers are used for an IMD test, the IMD products will depend significantly on the *phase relationships* between the carriers. A special condition of *carrier phase alignment*, above and beyond phase locking of test carriers, is essential to guarantee a worst-case measurement.

Before exploring the technical basis of phase alignment, a physical analogy will help to visualize the problem. If two runners are circling a track at different speeds, it is certain that they will both "meet" periodically. If three runners are circling the track, one will periodically meet another but it is not certain that all three will ever meet at the same time. One condition that will guarantee that all three runners will meet periodically is if their speeds are multiples of a common denominator and if they all start running at precisely the same time and position.

The same is true for multiple sinusoidal signals used as RF test carriers in an IMD or peak power measurement setup. Unless the carriers are multiples of a common frequency (i.e., phase locked to a common reference) and the starting phases are perfectly aligned, it is not certain that the waveform peaks will coincide in a predictable manner.

When three or more RF carriers are combined, the phase relationship between the carriers plays an important role. This can be seen by examining the mathematical representation of four RF carriers:

$$V_1 = A_1 \cdot \cos(\omega_1 t + \phi_1)$$

$$V_2 = A_2 \cdot \cos(\omega_2 t + \phi_2)$$

$$V_3 = A_3 \cdot \cos(\omega_3 t + \phi_3)$$

$$V_4 = A_4 \cdot \cos(\omega_4 t + \phi_4)$$

Figures 2a and 2b show the composite of the four carriers under two conditions of carrier phase. In figure 2a, the carrier phases (ϕ_n) are randomly distributed. In figure 2b, the carrier phases are "aligned" at equal phase. It is apparent that the phased-aligned carriers periodically regroup in phase at a period equal to the inverse of the frequency spacing. The randomly phased carriers do not periodically regroup in phase.

The RF power envelope of the combined carriers is of primary concern since the amplifier under test is subject to the combined power of the RF carriers. The peak combined power of the four randomly phased (see figure 2c) carriers is 6.0 watts or +37.8 dBm. In contrast, the peak combined power of the same four carriers is 16 watts or +42.0 dBm when the phases are aligned (see figure 2d). Thus, various possible combinations of carrier phase will result in instantaneous peak power levels ranging from 16 to 6 watts, or a ratio of 2.67:1. If more than 4 carriers are combined the ratio may be even more pronounced.

Multi-carrier IMD products are strongly dependent on the instantaneous peak power level of the combined carriers. This is because instantaneous power peaks drive the amplifier closer to its compression point for a fraction of each waveform cycle. The higher the peak, the more the amplifier is driven into compression. For this reason, the phase alignment of the RF test carriers is a critical parameter in IMD test setups.

To evaluate the effect of peak power level on IMD products, a class-A linear amplifier was tested using eight combined phase locked carriers. The test setup is shown in figure 3. The eight carriers were generated using an RDL IMD-803D multi-carrier signal generator. The IMD-803D has the ability to precisely control carrier phase to provide phase aligned or randomly phased carriers. A directional coupler and power detector were used to monitor the peak power waveform of the combined carriers.

IMD products were first measured with the eight carrier phases randomly distributed. Figure 4a shows the detected power envelope of the eight combined test carriers. The measured IMD spectrum of the amplifier is shown in figure 4b. All of the IMD products are -70 dBc or lower.

The test was then continued by configuring the IMD-803D signal generator to provide aligned carrier phases. Figure 4c shows the detected power envelope of the eight combined phase aligned carriers. Phase alignment has raised the peak power level by approximately 6:1 compared with the peak power of the combined randomly phased carriers. The measured IMD spectrum of the amplifier is shown in figure 4d. The measured IMD products have degraded to -

54 dBc. This 16 dB degradation is attributable entirely to the phase alignment of the eight test carriers.

Because of this property of carrier phase dependence, IMD test setups that do not use phase aligned carriers may suffer from inconsistent or inaccurate results. Suppose that phase locked loop (PLL) frequency synthesizers are combined to create a multi-carrier test signal. PLL frequency synthesizers typically utilize digital dividers that acquire a different starting phase each time the synthesizer is activated. In addition, thermal drifts, combiner phase mismatches, and different coaxial cable delays will all result in an unknown distribution of carrier phases when the PLL synthesizers are combined. Thus, each time the test setup is used the peak power level of the multi-carrier test signal may be different than the last time. IMD measurements will be inconsistent even when the same test setup is used over time.

The same problem arises when free-running oscillators are combined to create a multi-carrier test signal. Since the carrier phases are noncoherent, it is unlikely that all carrier phases will align at the same time instant to produce a worst case peak power level. If a spectrum analyzer is used to measure the IMD products, a "maximum hold" measurement would be required over an arguably infinite time span in order to insure that the worst case amplitude peak has been achieved. This method is not practical for measurement of multi-carrier IMD products.

It is now clear that the standard formula for predicting two tone IMD products,

$$IMD_{dB} = 2 * (IP3_{dBm} - \text{OUTPUT POWER}_{dBm})$$

is not valid for three or more RF carriers. Indeed, the average power level of N combined RF carriers is (N/2) watts regardless of the carrier phases. This demonstrates that the standard two-tone IMD formula does not account for instantaneous peak power dependence on carrier phases.

Phase aligned test carriers provide repeatable, accurate, and simple multi-carrier IMD measurements. Because the amplitude peaks are maximized at every period of the combined power waveform, the measured IMD products are repeatable over time and among different test stations. A single spectrum analyzer sweep will suffice to make the IMD measurement, without the need for long term waveform averaging or maximum hold monitoring.

Phase aligned carriers are especially critical for factory testing of multi-carrier amplifiers and systems. Multi-carrier systems deployed for field operation will need to operate under any condition of carrier phase relationships. Whether the carriers used at the field site originate from phase locked or free-running sources, the peak amplitude of the combined carriers will vary greatly from one site to an other. If the multi-carrier amplifier or system is tested using phase aligned carriers, the worst case scenario is assured. All field conditions of carrier phase will be accounted for in a single measurement.

In summary, IMD measurements on multi-carrier components and systems requires the use of phase aligned test carriers. Phase dependency can not be overlooked when evaluating a design for production readiness or in the large-scale manufacture of multi-carrier systems.

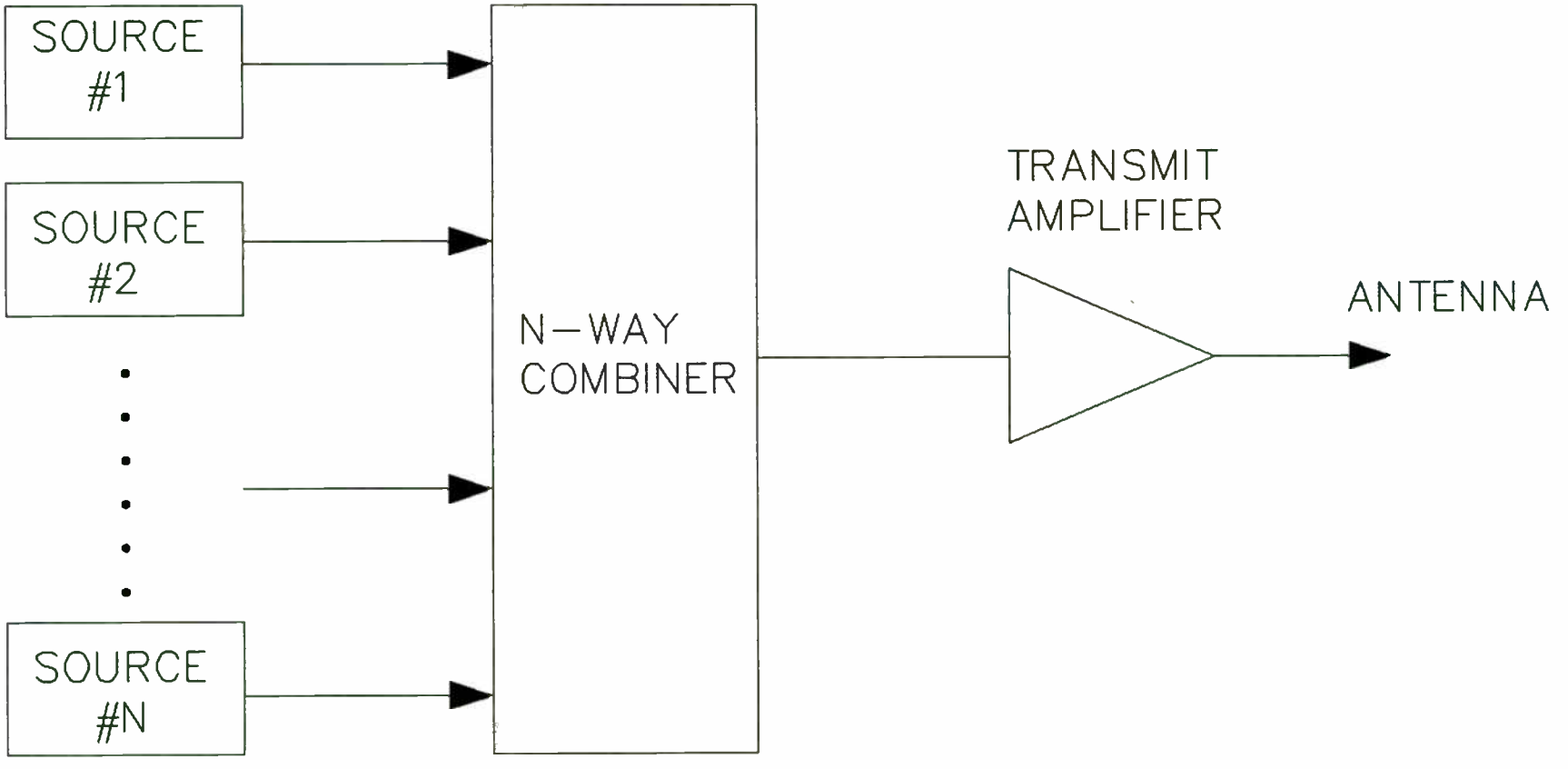

FIGURE 1 – MULTI-CARRIER AMPLIFICATION

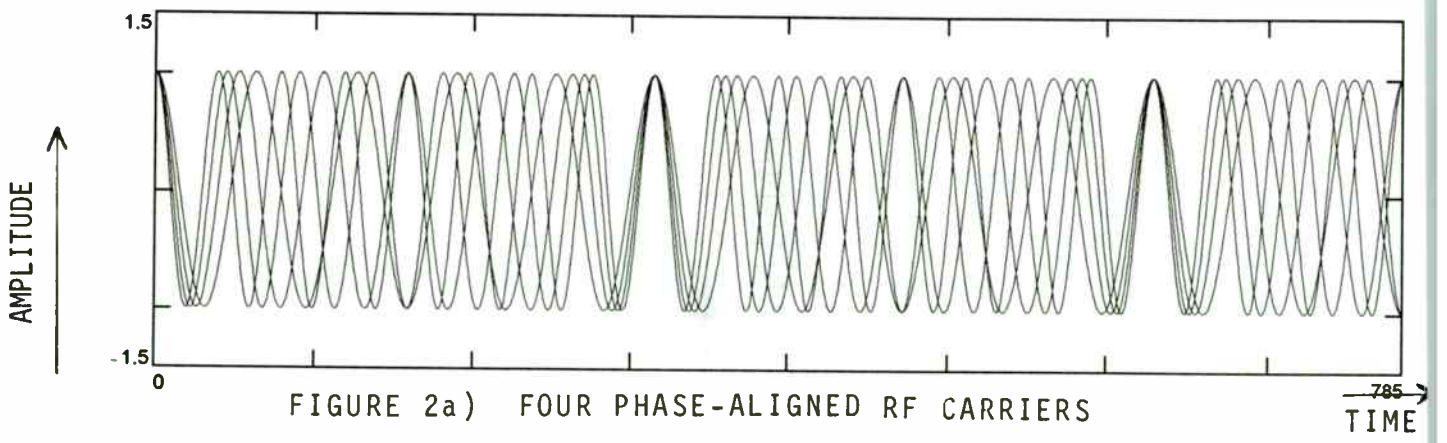

FIGURE 2a) FOUR PHASE-ALIGNED RF CARRIERS

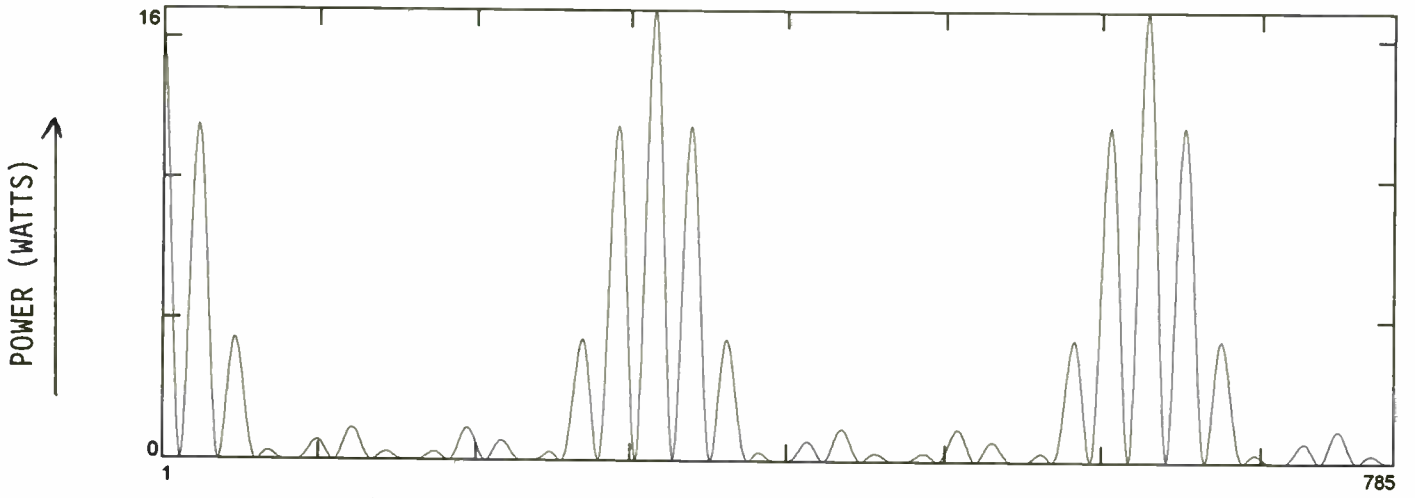

FIGURE 2c) INSTANTANEOUS POWER ENVELOPE OF FOUR PHASE-ALIGNED CARRIERS

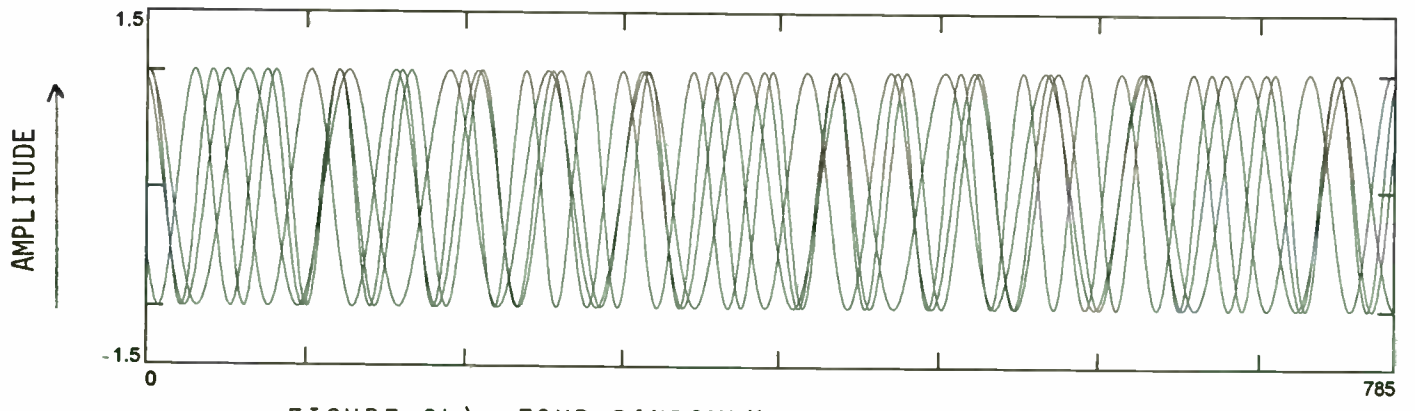

FIGURE 2b) FOUR RANDOMLY PHASED RF CARRIERS

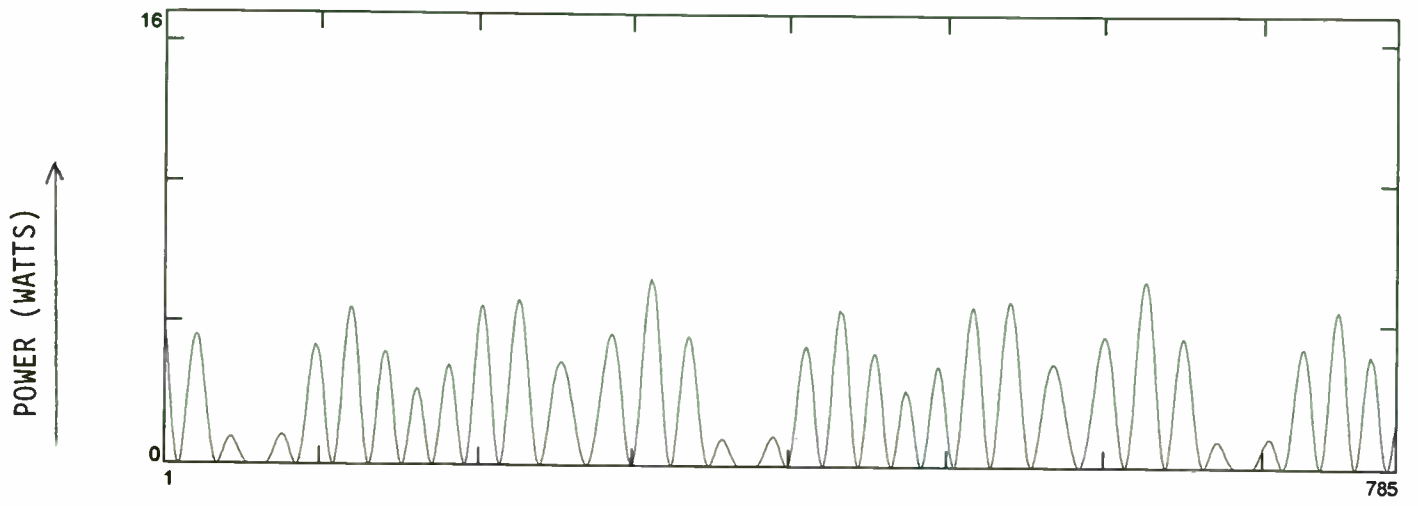

FIGURE 2d) INSTANTANEOUS POWER ENVELOPE OF FOUR RANDOMLY PHASED RF CARRIER

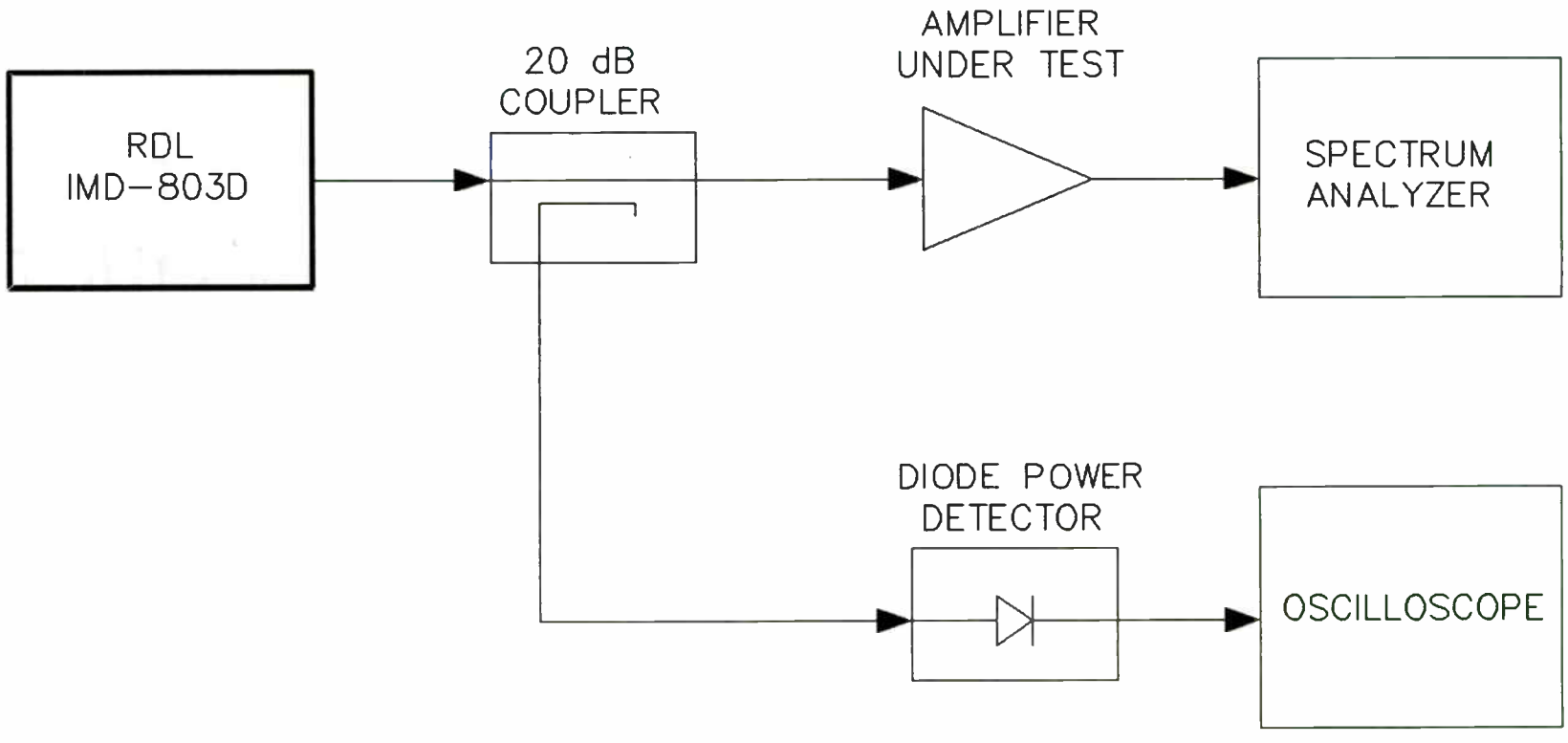

FIGURE 3 – MULTI-CARRIER IMD TEST SETUP

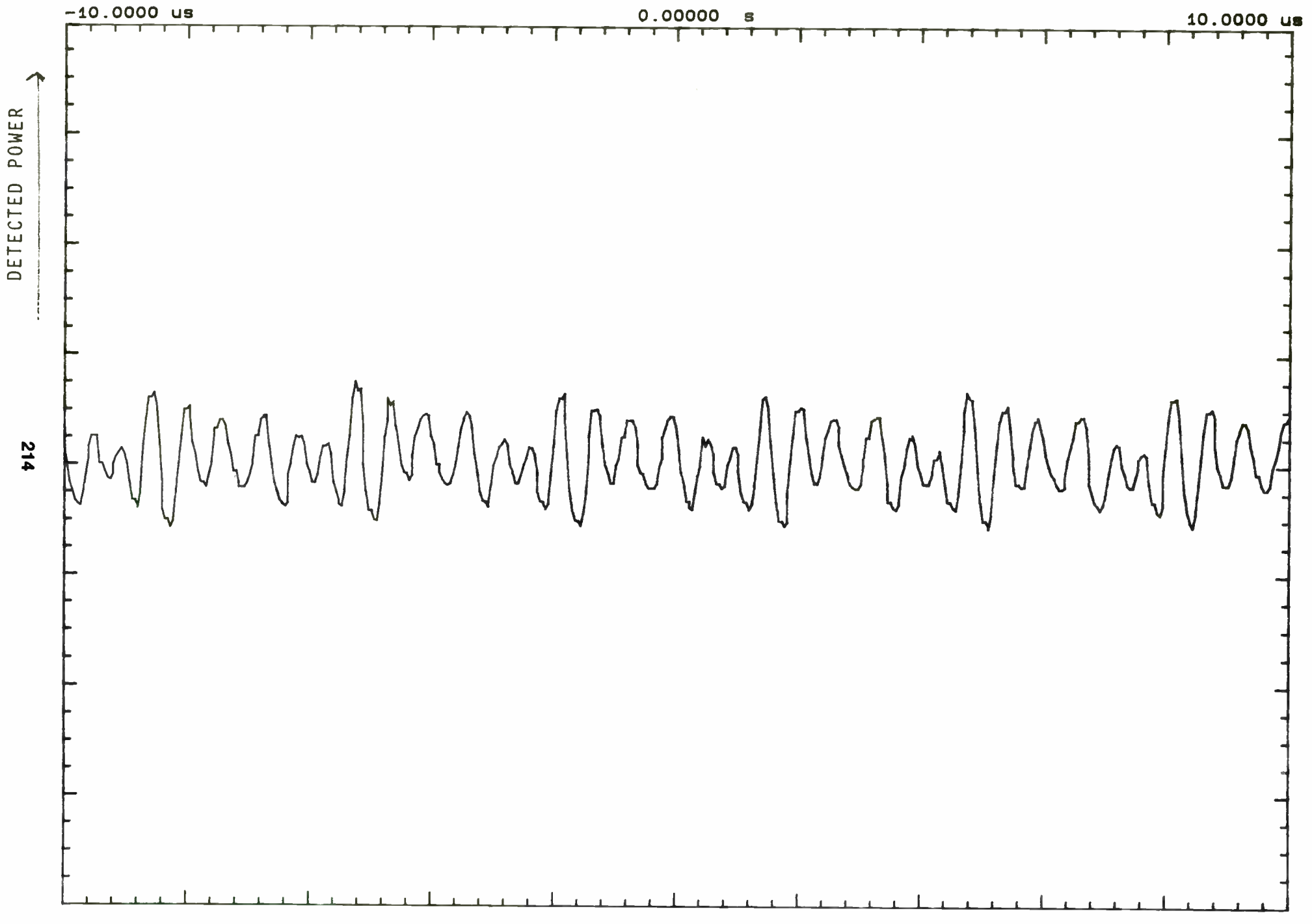

FIGURE 4a) TIME DOMAIN DETECTED POWER OF EIGHT RANDOMLY PHASED RF CARRIERS

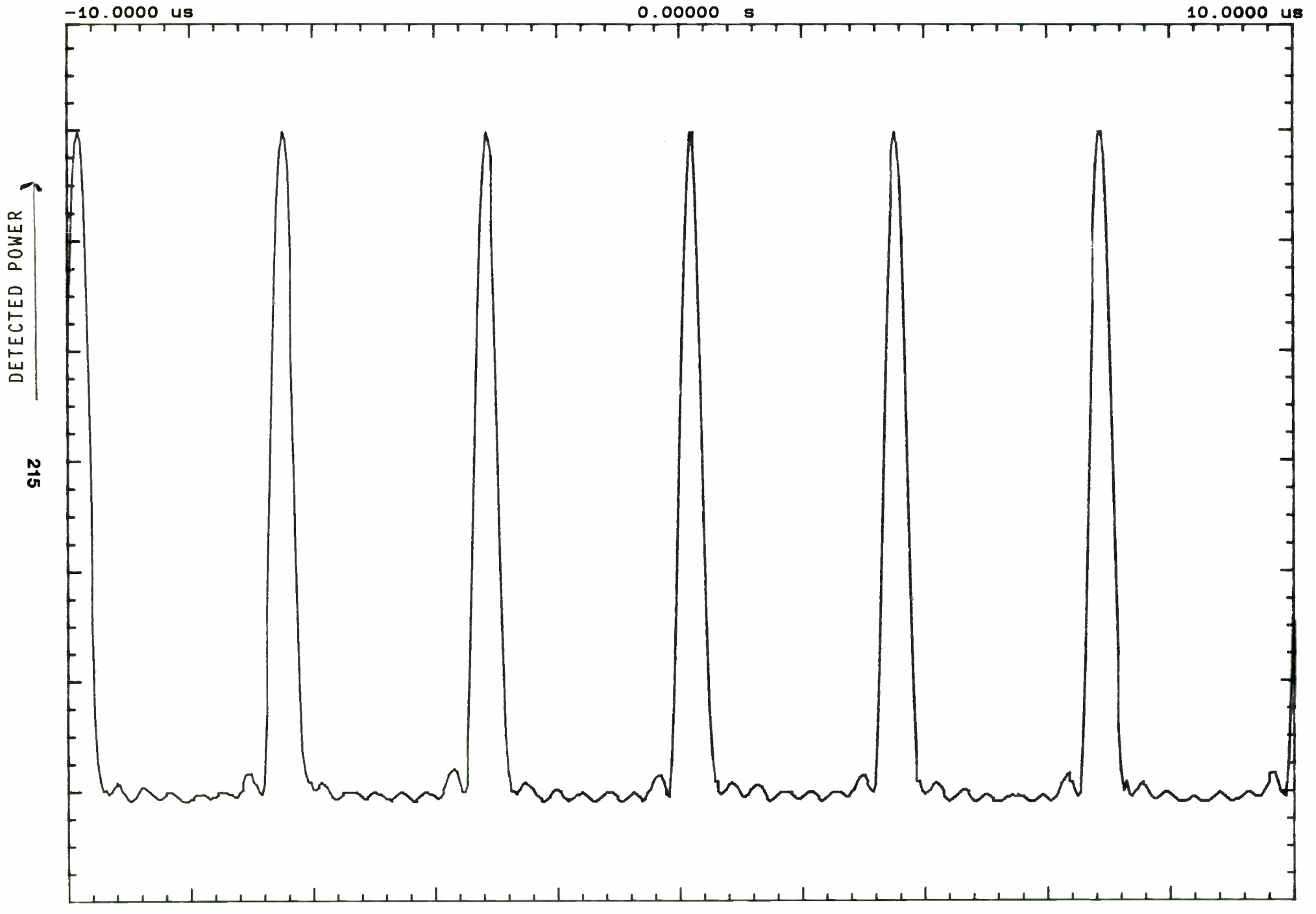

FIGURE 4c TIME DOMAIN DETECTED POWER OF EIGHT PHASE-ALIGNED RF CARRIERS

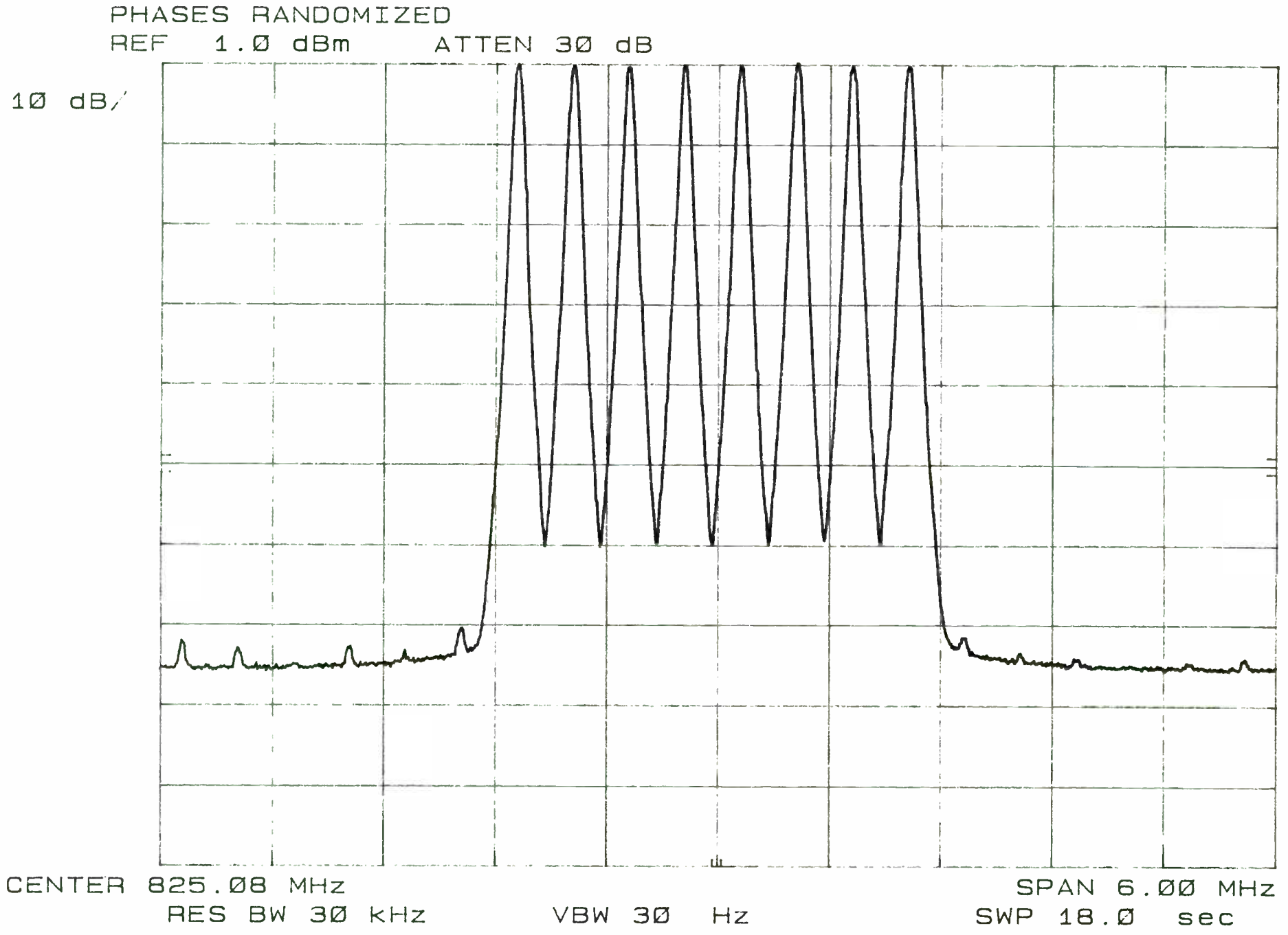

FIGURE 4b) MEASURED IMD SPECTRUM USING EIGHT RANDOMLY PHASED RF CARRIERS

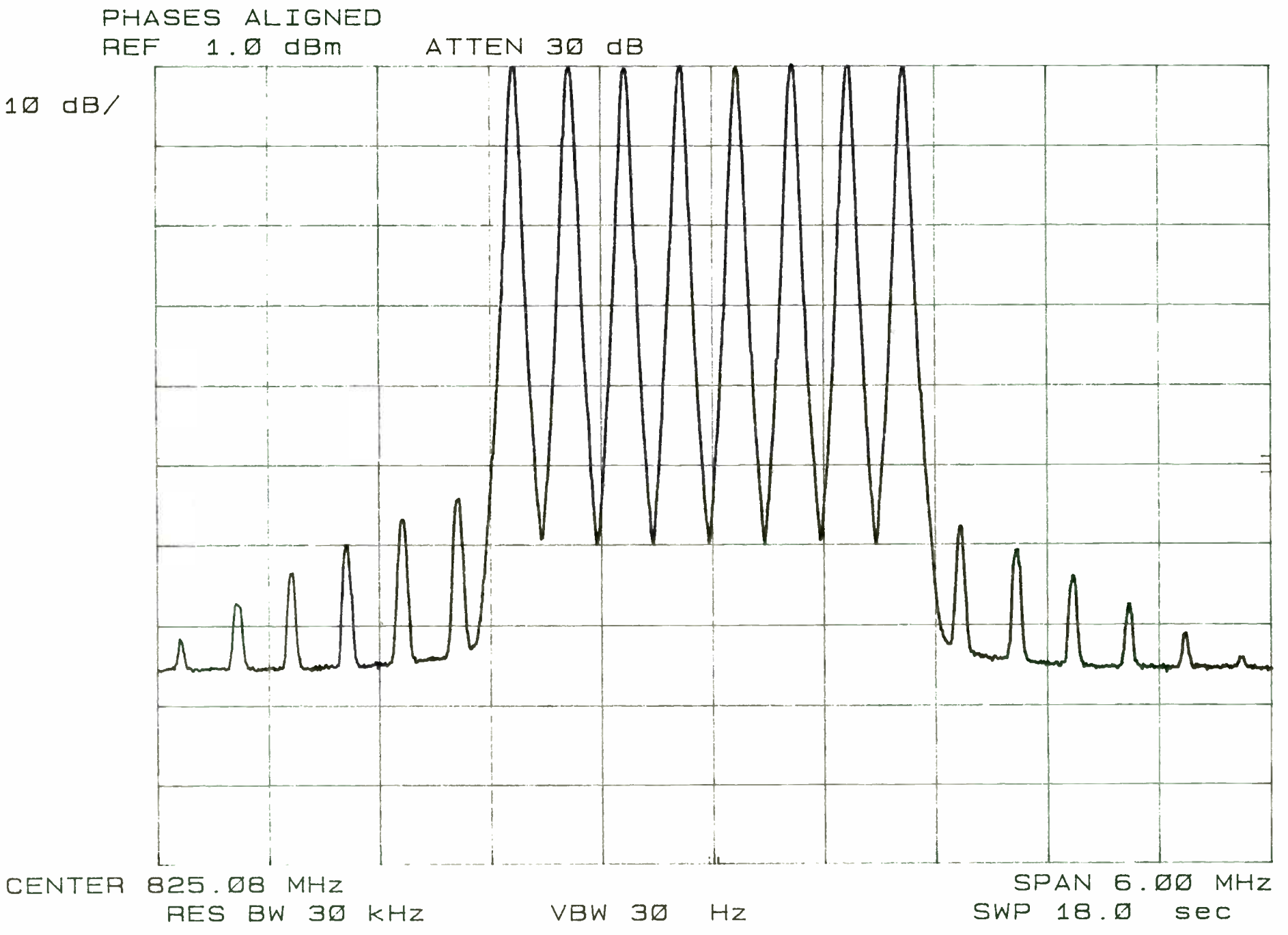

FIGURE 4d) MEASURED IMD SPECTRUM USING EIGHT PHASE-ALIGNED RF CARRIERS

Wireless Market: Implications for RF Test & Measurement

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In the face of a static or declining defense budget, the microwave industry is placing its hopes on the growth in commercial markets particularly in the wireless area. In this paper we will discuss how the market is segmented, the anticipated developments in these segments and the implications for test and measurement.

The emerging character of this market makes it hard to segment in any simple way but an attempt to group it by application (Figure 1) gives the impression that an identity is imminent. Almost all of these market segments have been characterized as wireless at one time or another and perhaps the most common feature of all of them is the probability of using MMICs in either GaAs or silicon.

Many of the characteristics of these markets are very unfamiliar to the traditional RF practitioner (Figure 2) and the implications for test and measurement are powerful. (Figure 3)

It is anticipated that the total market for MMICs will grow by a factor of more than three from 1993 to 1998. At the same time the total units will grow by a factor of five as a result of sharp decrease in unit price. One of the market forces shaping this price decrease will be over capacity in the

industry since the number of wafers required is a fraction of current industry capacity; a situation which is likely to drive price wars. (Figure 4)

To delineate the issue of cost, we have surveyed the industry on the probable 1998 average selling price for GaAs MMICs in a variety of these segments. The result is shown in Figure 5. These represent much lower prices that we are used to thinking about. There is just much less money to be spent testing each of these devices.

At the component level the broad range of characteristics to be measured is very familiar to the microwave industry. (Figure 6) At the system level application specific tests will require new knowledge.

A variety of solutions have been proposed to reduce test cost and increase volumes (Figure 7) and the use of a particular solution will be peculiar to specific customers and specific applications.

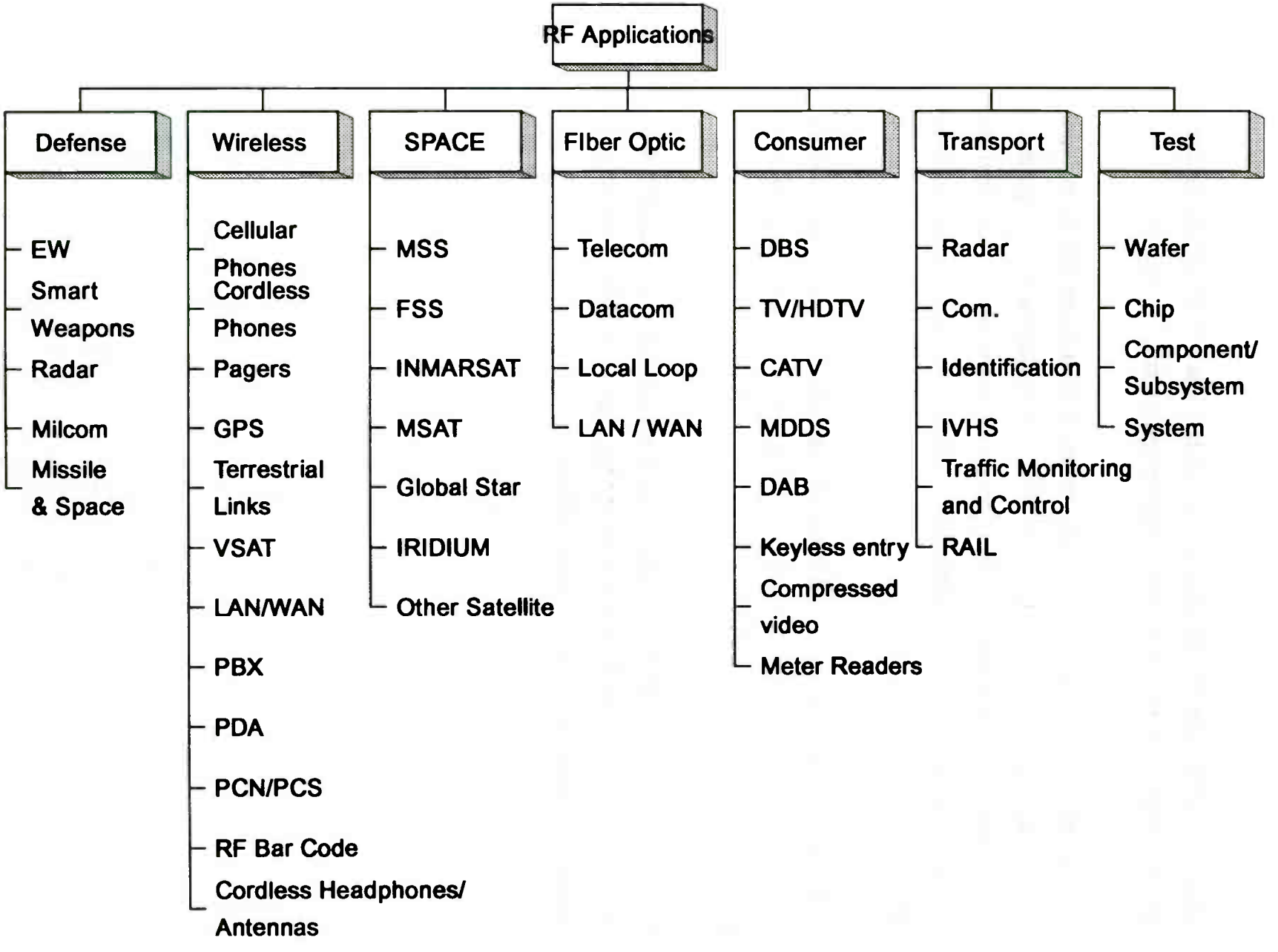

figure 1

Wireless Market Characteristics

- Low Cost
- High Volumes
- No NRE
- Rapid Product Cycles

figure 2

Implications for Test and Measurement

- Testing Volumes will Increase
- Testing Cost Must Come Down
- Accuracy and Repeatability Must be Maintained
- Low Capital Budgets

figure 3

MMIC Market Growth

	1993	1998
Total Market $ Millions	200	700
Total Units Millions	25	125
Total Wafers	8000 (3")	17000 (4")

figure 4

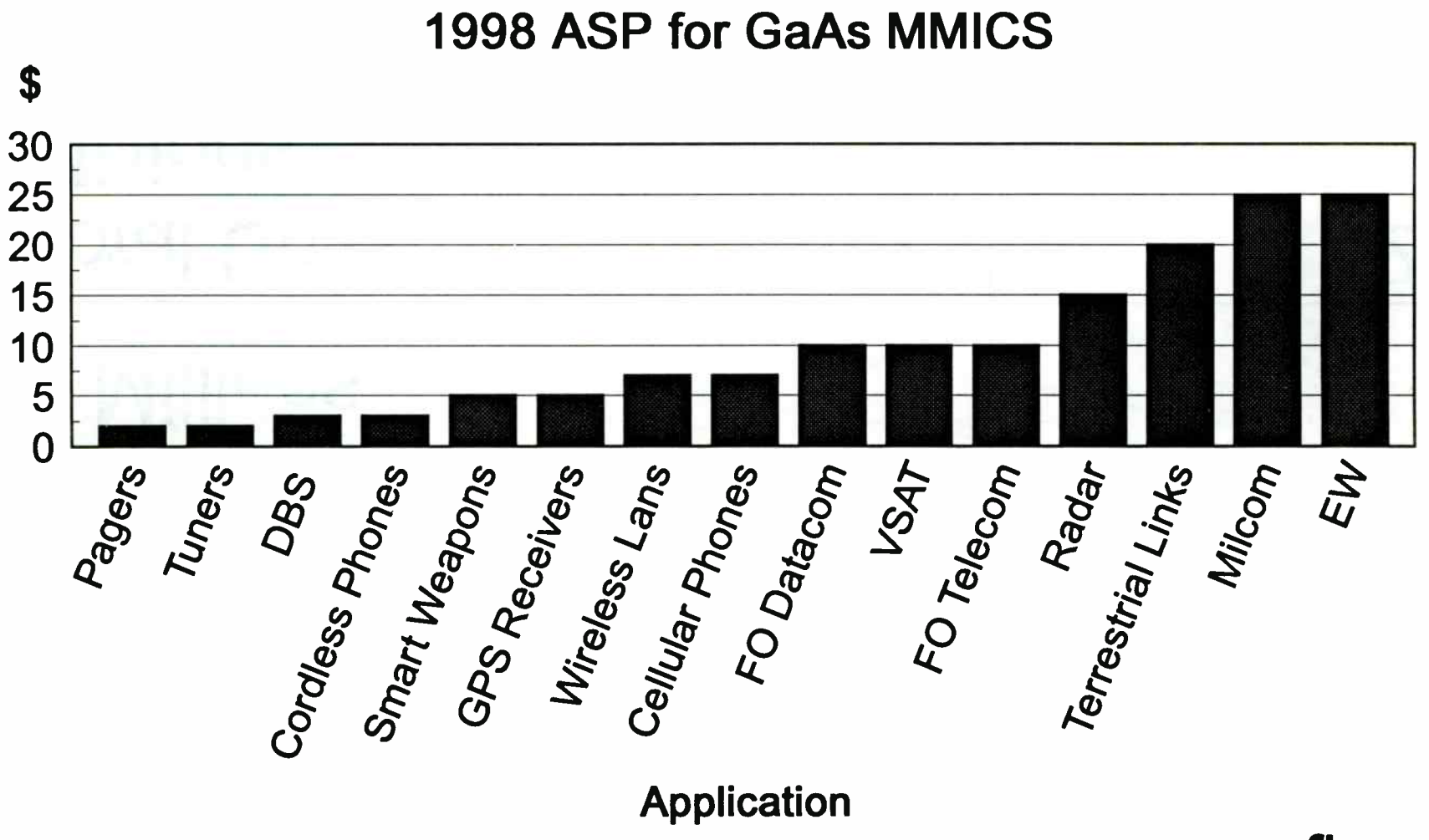

figure 5

Performance Characteristics

Application	IF Amplifier	Down Converter	Down Converter	Power Amplifier
Frequency GHz	.03-.5	.5-2.5	10.95-11.7	.89-.95
Power Out dBm	-14 to -6	----------	----------	31
Efficiency %	----------	----------	----------	60
Noise Figure dB	6.5	3.2	6	_____
Conversion Gain dB	----------	50	35	----------
AGC Range dB	65	50	----------	----------
Power (Vdc)	+5	----------	----------	3.5

figure 6

Solutions

Solutions	Advantage	Disadvantage
Buy More Equipment	Helps T&M Companies	Costs $
Design Out Test	Reduces Test Costs	Effects Manufacturing Yields
Test DC Only	Reduced Costs	Inadequate Correlations with RF Performance
Selected Tests	Reduces Test Times	Incomplete Characterization
Faster Testing	Complete Testing	Requires Expensive New Equipment

Figure 7

Noise Figure and Gain Measurement on High Speed Bipolar Junction Transistors

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INTRODUCTION

It is a fact that no electronic system is completely free of random noise. Small voltage fluctuations due to noise are always occurring in electronic circuits because electrons are discrete and are constantly moving in time. Noise obscures low level electrical signals, therefore it can be a limiting factor on component and system performance.

This analysis studies the noise and gain characteristics of the basic component in an amplifier block, the transistor, in the microwave frequency range. After identifying the noise sources in the transistor, the effect of each noise source on the performance of the device is discussed. This analysis will provide spot noise figure and gain data for two high speed silicon bipolar transistors manufactured on two processes from Tektronix Microelectronics (SHPi and GST-1). They are N16 from the SHPi process and G14V102 from the GST-1 process. SHPi is Tektronix' Super-High frequency bipolar process. The f_T of the SHPi transistor is close to $9GHz$ under the condition of $V_{CE} = 4V$. GST-1 (Giga-Speed Si-Bipolar Technology) is a high speed self-aligned double-polysilicon process. GST-1 is designed for the purpose of building high density, high performance analog and digital circuits. The f_T of the GST-1 transistor is $13GHz$ with $V_{CE} = 4V$.

NOISE FIGURE

To compare the performance of high frequency devices, an important figure of merit is the noise factor/figure, which is a measure of how the noise generated in a device degrade the signal-to-noise ratio. The noise factor F of the network is defined as the ratio of the available signal-to-noise ratio at the signal generator terminals to the available signal-to-noise ratio at its output terminals. The ideal noise factor is unity or $0dB$, where there is no degradation in signal-to-noise ratio after the signal passes through the network

$$F = \frac{S_i/N_i}{S_o/N_o} \tag{1}$$

Noise figure is a parameter that applies both to components and systems. The overall system noise performance can be predicted from the noise figure and gain of the components that go into it. For a number of networks in cascade, as shown in Fig. 1, the system spot noise factor is given in terms

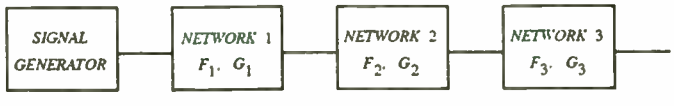


Figure 1. Noise figure of network in cascade.

of the component spot noise factors and available gain by

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \tag{2}$$

From Eq. (2), the significance of the first stage gain and noise factor are evident. The first stage in the chain has the most significant contribution to the total noise factor of the chain. The total noise factor of the system is at least equal to the noise factor of the first stage. If the first stage gain is significantly large, then the noise contributions from the succeeding stages will be small.

AVAILABLE POWER GAIN

A signal generator with an internal impedance R_s and output voltage V_s can deliver $\frac{V_s^2 R_l}{(R_s + R_l)^2}$ watts into a resistance of R_l. This power is maximum and equal to $\frac{V_s^2}{4R_s}$ when the output circuit is matched to the generator impedance. Therefore, $\frac{V_s^2}{4R_s}$ is called the available power of the generator, and it is, by definition, independent of the impedance of the circuit to which it is connected. The output power is smaller than the available power when R_l is not equal to R_s, since there is a mismatch loss. In amplifier input circuits a mismatch condition may be beneficial due to the fact that it

may decrease the output noise more than the output signal. The available gain of the network is defined as:

$$G_A = \frac{\textit{power available from the network}}{\textit{power available from the source}} = \frac{S}{S_g} \quad (3)$$

Note that while the gain is independent of the impedance which the output circuit presents to the network, it does depend on the impedance of the signal generator.

NOISE FIGURE MEASUREMENT

NOISE IN BIPOLAR TRANSISTOR

The noise sources in a bipolar junction transistor are categorized into four major types:

1. Flicker noise;
2. Burst noise;
3. Shot noise;
4. Thermal noise.

Flicker Noise

Flicker noise is caused by traps associated with contamination and crystal defects in the emitter-base depletion layer. It is associated with a flow of direct current and displays a spectral density of the form [3]:

$$\overline{i^2} = \frac{K_F I^{A_F}}{f} \Delta f \quad (4)$$

where K_F is a constant for a particular device, A_F is a constant between 0.5 and 2, and Δf is the bandwidth in Hertz. This expression shows that the noise spectral density has a ($1 / f$) frequency dependence, therefore, it is also called $1 / f$ noise. Since flicker noise is most significant at low frequencies, it is not discussed here.

Burst Noise

It has been found experimentally that the low frequency noise spectrums of some bipolar transistors show a different frequency dependence than flicker noise. This could be the result of the existence of burst noise. It is caused by the imperfection in the crystal structure. The power spectrum of such signal is given by [4]:

$$\overline{i^2} = \frac{K_B I}{1 + \left(\frac{\pi f}{2k}\right)^2} \Delta f \quad (5)$$

where K_B is a technological dependent constant for a particular device, and k is the mean repetition rate of the signal. This noise is insignificant at microwave frequencies because it is inversely proportional to f^2, and it will not be addressed further.

Shot Noise

Shot noise is due to generation and recombination in the pn junction and injection of carriers across the potential barriers, therefore it is present in all semiconductor diodes and bipolar transistors. Each carrier crosses the junction in a purely random fashion. Thus the current I, which appears to be a steady current, is, in fact, composed of a large number of random independent current pulses. The fluctuation in I is termed shot noise and is generally specified in terms of its mean-square variation about the average value I_D, and it is represented by [3]:

$$\overline{i^2} = 2qI_D\Delta f \quad (6)$$

where q is the electronic charge. Eq. (6) shows that the noise spectral density is independent of frequency. In a transistor, there are two such noise sources. They are the shot noise in the emitter-base junction (i_b) and in the collector-base junction (i_c).

Thermal Noise

Thermal noise is due to the random thermal motion of electrons in a resistor, and it is unaffected by the presence or absence of direct current, since typical electron drift velocities in a conductor are much less than electron thermal velocities. As the name indicates, thermal noise is related to absolute temperature T.

In a resistor R, thermal noise can be represented by a series voltage source $\overline{v^2}$. It is represented by [3]:

$$\overline{v^2} = 4kTR\Delta f \quad (7)$$

where k is Boltzmann's constant, and T is temperature in Kelvin. Like shot noise, thermal noise is also independent of frequency. Thermal noise is a fundamental physical phenomenon and is present in any linear passive resistor.

Equivalent Circuit

Fig. 2 is the small-signal equivalent circuit, including noise sources for the bipolar transistor at high frequency [3]. Three noise sources are evident from the figure. They are thermal noise from the series input resistance (r_b) and shot noise due to the base and collector currents (I_b, I_c) and their values are:

$$\overline{v_b^2} = 4kTr_b\Delta f \quad (8)$$

$$\overline{i_b^2} = 2qI_b\Delta f \quad (9)$$

$$\overline{i_c^2} = 2qI_c\Delta f \quad (10)$$

Neither thermal noise nor shot noise is frequency dependent, and both exhibit uniform noise output through the entire useful frequency range of the transistor. The internal gain of the transistor does vary with frequency, however, and it falls off as frequency increases. As a result the noise figure begins

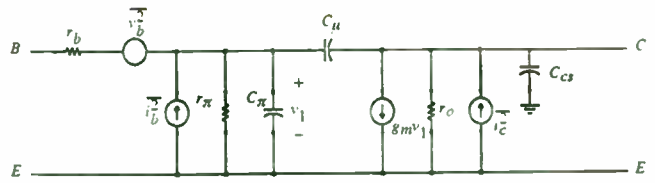


Figure 2. Bipolar transistor small-signal equivalent circuit with noise sources.

to rise when the reduction in gain becomes appreciable. Since the power gain falls inversely as frequency squared, the noise figure rises as frequency squared, or $6dB$ per octave [5]. Fig. 3 graphically shows the noise figure of a G14V102 transistor with $V_{BE} = 0.8V$, $V_{CE} = 4V$, and $R_s = 50\Omega$ in common emitter configuration.

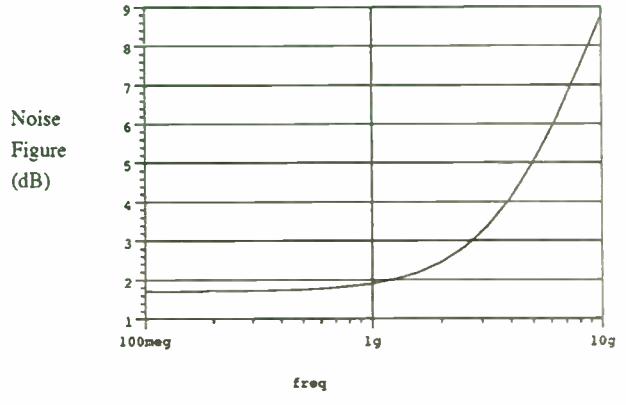


Figure 3. Noise figure vs. frequency for G14V102.

DETERMINATION OF NOISE PARAMETERS

Definition

As defined in 1960 by the IRE Subcommittee on Noise [6], noise figure depends upon the internal structure of the transducer and upon its input termination, but not upon its output termination. The noise factor F of any linear transducer, at a given operating point and input frequency, varies with the admittance Y_s of its input termination in the following manner [7]:

$$F = F_o + \frac{R_n}{G_s} \mid Y_s - Y_o \mid^2 \tag{11}$$

where G_s is the real part of Y_s, and the parameters F_o, Y_o, and R_n characterize the noise properties of the transducer and are independent of its input termination.

Two methods of computer-aided determination of noise parameters have been reported in the literature.

One of them, Kokyczka et al [8], can be thought of as an automatic version of the graphic procedure suggested by the Institute of Radio Engineers [6], which required tedious and time-consuming adjustment of some input termination admittances with constant real part and of some other with constant imaginary part.

The other one, Lane [9], is an application of the least-squares method, which reduces the determination of noise parameters to the solution of a four linear equation system, obtained as fit of noise figures measured for different source admittances.

Noise Parameters Computation

Ten sets of data for the N16 and the G14V102 are obtained with different source admittances and are tabulated in table I and will be used to calculate the noise parameters of the devices.

Table I

Noise Figure Measured at Various Source Impedances with V_{BE}=0.8V, V_{CE}=4V at F=1000MHz

G_s mmhos	B_s mmhos	NF dB	
		N16	G14V102
16.9	−2.94	2.86	1.83
13.4	−9.40	2.96	1.90
21.5	−12.3	3.65	1.99
22.7	−23.4	4.87	2.49
37.7	−17.1	4.81	2.44
67.0	−25.8	6.39	2.32
47.1	11.8	5.18	2.74
30.5	17.1	4.66	2.61
20.0	20.8	4.88	2.94
12.7	4.52	2.70	2.08

After the noise figure data for different source impedances are obtained, the noise parameters F_o, Y_o, and R_n can be determined. Eq. (11) is transformed to a form that is linear with respect to four new parameters A, B, C, and D [11].

$$F = A + BG_s + \frac{C + BB_s^2 + DB_s}{G_s} \tag{12}$$

where

$$F_o = A + \sqrt{4BC - D^2} \tag{13}$$

$$R_n = B \tag{14}$$

$$G_o = \frac{\sqrt{4BC - D^2}}{2B} \tag{15}$$

$$B_o = \frac{-D}{2B}. \tag{16}$$

In principle, four measurements of noise factor from different source admittances will determine the four real numbers (F_o, R_n, G_o, and B_o). Eq. (12) becomes overdetermined if more than four measurements are taken, but by minimizing the square of error as expressed in Eq. (17), more than four measurements can be used to find those parameters which

give the best least squares fit to Eq. (12). It has been shown that only slight variations of noise parameters occur versus redundancy if the number of data sets processed is greater than 7 [10]. A least-squares fit of the ten sets of noise figure data noise from table I to Eq. (12) is sought: therefore, the following error criterion is established [9]:

$$\varepsilon = \frac{1}{2}\sum_{i=1}^{n}\left[A + B\left(G_i + \frac{B_i^2}{G_i}\right) + \frac{C}{G_i} + \frac{DB_i}{G_i} - F_i\right]^2 \qquad (17)$$

Base on the noise figure data in table I, the noise parameters for the N16 and G14V102 transistors are obtained.

Table II

Noise Parameters of N16 and G14V102 Transistors with V_{BE}=0.8V, V_{CE}=4V at F=1000MHz

	Fo dB	Rn ohms	Go mmhos	Bo mmhos
N16	1.94	42.5	5.32	-1.41
G14V102	1.82	13.6	15.6	-4.44

NOISE FIGURE CIRCLES

To plot noise figures on a Smith chart, Eq. (11) is expressed in terms of reflection coefficients.

$$F = F_o + \frac{4R_n\,|\Gamma_s - \Gamma_o|^2}{(1 - |\Gamma_s|^2)\,|1 + \Gamma_o|^2} \qquad (18)$$

This equation can be used to seek Γ_s for a given noise figure. To determine a family of noise figure circles, an intermediate noise figure parameter, N_i, is defined [1].

$$N_i = \frac{|\Gamma_s - \Gamma_o|^2}{1 - |\Gamma_s|^2} = \frac{F_i - F_o}{4R_n}|1 + \Gamma_s|^2 \qquad (19)$$

The center and radius of the circles are:

$$C_{F_i} = \frac{\Gamma_o}{1 + N_i} \qquad (20)$$

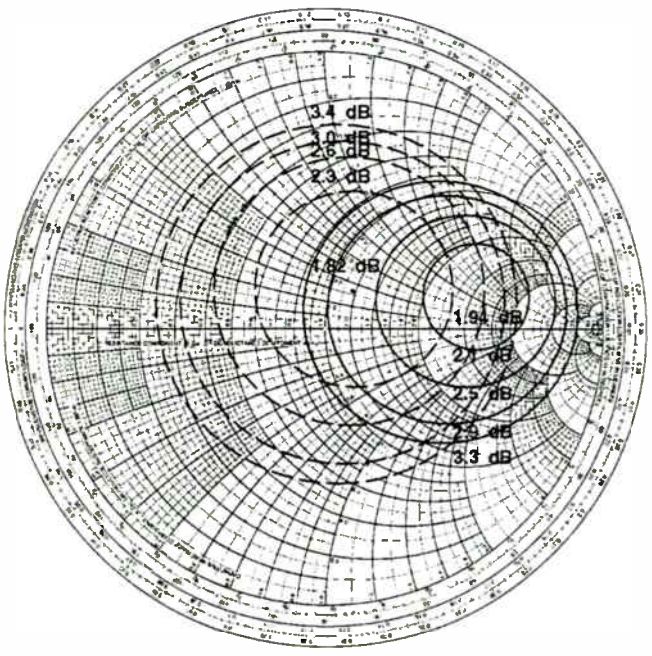
and

$$R_{F_i} = \frac{1}{1 + N_i}\sqrt{N_i^2 + N_i\,(1 - |\Gamma_o|^2)} \qquad (21)$$

Eq. (19), Eq. (20), and Eq. (21) show that when $F_i = F_o$, then $N_i = 0$, $C_{F_o} = \Gamma_o$, and $R_{F_o} = 0$. That is, the center of the F_o circle is located at Γ_o with zero radius. From Eq. (20), the centers of the other noise figure circles are located along the Γ_o vector.

COMPARISON

From the data obtained, the equivalent noise resistance (R_n) of the G14V102 is smaller than the one of the N16. This is verified by wider spacing of noise figure circles of the G14V102 as compare to the ones of the N16 (Fig. 4). The lower of R_n will result in reduced sensitivity of the noise figure to changes in source impedance. Therefore, a circuit designer can have more freedom on choosing source impedances for better power gain and/or better input matching for a given noise figure.



G14V102 ___ N16 ____

Figure 4. Noise figure circles for G14V102 and N16 with V_{BE}=0.8V, V_{CE}=4V at F=1000MHz.

GAIN MEASUREMENT

GAIN AND STABILITY

Stability Criteria

As the operating frequency of the transistor is being pushed upward, the transistor is more prone to unwanted oscillation due to parasitic elements. The necessary conditions for stability of a two-port device like bipolar transistors, had been studied by Kurokawa[12], Bodway[13], and Woods[14]. In terms of s-parameters, they are:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \qquad (22)$$

and

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}S_{21}|} > 1 \qquad (23)$$

Two-port devices that meets the above criteria are

unconditionally stable for any positive source and load impedance.

Stability Circles

To maximize the gain, we need to conjugately match the input and the output. For unconditionally stable two-ports networks there is no unwanted oscillation to worry about. But for those networks which cannot meet the above stability criteria, we will have to look at what might happen to the network in terms of stability--will the amplifier oscillate with certain values of impedance used in the matching process?

In a two-port network, oscillations are possible when either the input or output port presents a negative resistance, since noise generated in the adjoining network enters the port, the negative resistance generates more noise rather than dissipating the incident noise, and some of this generated noise combines with the incoming noise to input more noise. Negative resistances correspond to the points outside the Smith chart, which imply either $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$. Therefore, we have the boundary for the input and output stability circles defined:

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_l}{1 - S_{22}\Gamma_l} \right| = 1 \tag{24}$$

and

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \right| = 1 \tag{25}$$

Solving for the values of Γ_l and Γ_s in Eq. (24) and Eq. (25) shows that the solutions for Γ_l and Γ_s lie on circles [2]. The radius and center of the input stability circles are:

$$r_s = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \tag{26}$$

$$C_s = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \tag{27}$$

and the radius and center of the output stability circles are:

$$r_l = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \tag{28}$$

$$C_l = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \tag{29}$$

Having measured the s-parameters of a two-port device at one frequency, Eq. (26) to Eq. (29) can be evaluated, and plotted on a Smith chart. Fig. 5 illustrates the graphical construction of the stability circles where $|\Gamma_{in}| = 1$. On one side of the stability circles boundary, in the Γ_l plane, we will have $|\Gamma_{in}| < 1$ and on the other side $|\Gamma_{in}| > 1$.

When the input and output stability circles lie completely outside the Smith chart the network is called unconditionally

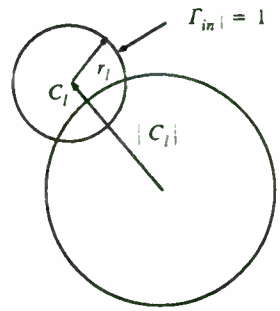


Figure 5. Stability circles construction on a Smith chart.

stable for all Γ_s and Γ_l. This comes from the fact that no matter what positive termination is put at the input or output of the network $|\Gamma_{in}|$ and $|\Gamma_{out}|$ will be always less than unity.

Gain Circles

S-parameters can be used to predict the available power gain of a transistor for any input termination Γ_s. This available gain is that gain achieved when a transistor is driven from some source reflection Γ_s while terminated with a load impedance equal to Γ_{out}^* (matched output). The available power gain in terms of reflection coefficients is [1]:

$$G_A = \frac{(1 - |\Gamma_s|^2)}{|1 - S_{11}\Gamma_s|^2} |S_{21}|^2 \frac{1}{(1 - |\Gamma_{out}|^2)} \tag{30}$$

where

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \tag{31}$$

Because G_A is a function of the source reflection coefficient, constant available power gain circles can be plotted on a Smith chart together with the constant noise figure circles, and the trade-off result between gain and noise figure can be analyzed.

For a given gain G_A, the radius R_a and the center C_a of the circle can be calculated using the relations [2]

$$g_a = \frac{G_A}{|S_{21}|^2} \tag{32}$$

$$C_1 = S_{11} - \Delta S_{22}^* \tag{33}$$

$$R_a = \frac{\sqrt{1 - 2K|S_{12}S_{21}|g_a + |S_{12}S_{21}|^2 g_a^2}}{|1 + g_a(|S_{11}|^2 - |\Delta|^2)|} \tag{34}$$

and

$$C_a = \frac{g_a C_1^*}{1 + g_a(|S_{11}|^2 - |\Delta|^2)} \tag{35}$$

For a given G_A, the constant available power gain circle can be plotted. All Γ_s on this circle produce the gain G_A.

COMPARISON

Gain circles, stability circles, and noise figure circles for the N16 and the G14V102 are plotted in Fig. 6 and Fig. 7. Under the conditions $V_{BE} = 0.80V$, $V_{CE} = 4V$ at $f = 1000MHz$, these two transistors can provide similar power gains. Looking at these figures, one can see that a N16 will provide a gain of about $17dB$ and a noise figure of $3.0dB$ with 50Ω source impedance, while a G14V102 will provide $18dB$ of gain but with a superior noise figure of $1.9dB$.

CONCLUSION

Noise is created by many physical processes which cannot be avoided. Living with noise means we must be able to measure and predict it. The noise sources in a bipolar transistor have been identified. At microwave frequencies they are thermal noise due to base resistance and shot noise from the base and collector currents. The base resistance consists of two parts. The external base resistance, R_{b_i}, is the resistance of the path between the base contact and the edge of the emitter diffusion. The active base resistance, R_{b_a}, is that resistance between the edge of the emitter and the site within the base region at which the current is actually flowing. R_{b_i} can be reduced by decreasing the separation between the base and the emitter. This method is straightforward, but it is technology-limited. While the effect of current crowding in the base at high current level will reduce the effect of R_{b_a}, but more shot noise will be generated by the higher current.

The technique of measuring noise parameters (F_o, R_n, G_o, and B_o) of a bipolar transistor has been presented. This same measurement technique can also be employed to measure the noise parameters of a general two-port network. Power gain information is obtained through s-parameter manipulation. The noise figure and available power gain data are plotted on Smith Chart to give a clear view of how a particular device will perform in various source impedances.

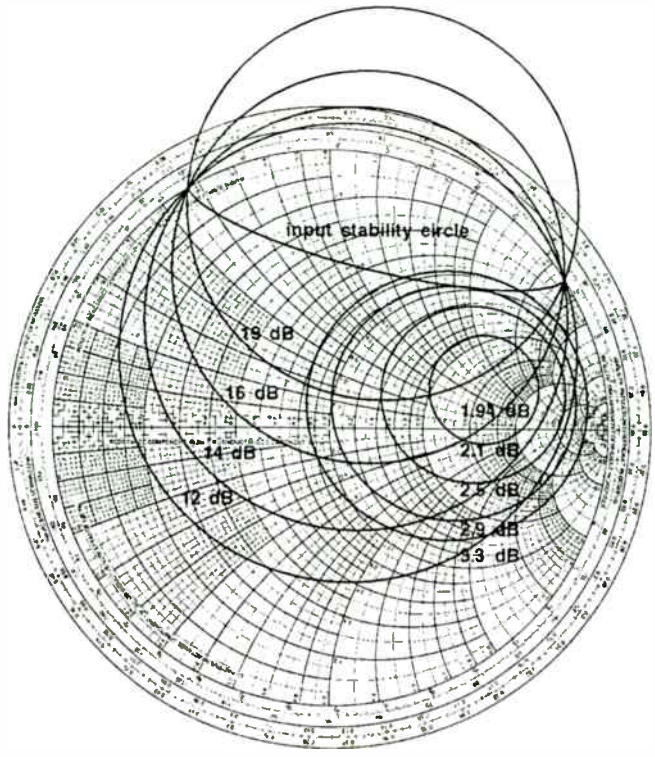


Figure 6. Gain and noise figure circles for N16 at F=1000MHz.

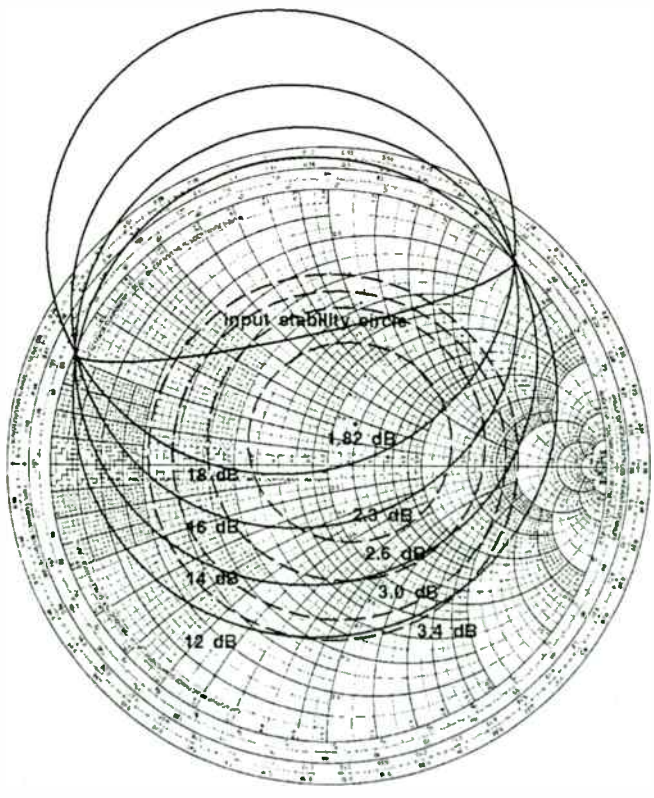


Figure 7. Gain and noise figure circles for G14V102 at F=1000MHz.

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FLEXIBLE INSTRUMENTATION FOR WIRELESS SPREAD SPECTRUM SIGNAL TRANSMISSION TESTING

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Abstract

Measurement of group delay of frequency converters for satellite receivers

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Wiltron Co., 490 Jarvis Drive, Morgan Hill, CA
95037-2809; (408) 778-2000, FAX: (408) 778-0239.

The use of vector network analyzer to measure the S-parameters including group delay of frequency conversion devices used in satellite receivers is described. A Wiltron 360 VNA and application-specific test set was developed for the measurement of the S-parameters of a downconverter subsystem. The design requirements for an application-specific test set that includes the inverse conversion of the subsystem being measured are described. Measured data on a SHF 7.9 to 8.4 GHz dual downconverter will be presented. The downconverter test set incorporated an upconverter utilizing the same local oscillator as used in the downconversion. The uncertainty of the group delay measurements was less than 1 ns.

Computer-Aided Engineering, I

Session Chairperson: Raymond S. Pengelly,
Raytheon Company, Advanced Devices Center (Andover, MA)

Designing Surface Mount Boards for RF Applications using Device Libraries and Modern CAD Tools

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Introduction

Today, more and more RF subsystems are being built using low-cost printed circuit board materials with reflow-soldered surface-mount components. In many cases these components themselves are completely functional circuits, such as mixers and amplifiers, apparently requiring straight-forward DC and RF connections. Access to accurate device library data is, therefore, of considerable importance in designing "fast-to-market" products. This paper will concentrate on some linear and nonlinear design examples in the UHF/L-Band frequency ranges using surface mount PCB design techniques. Even though the frequencies of operation of these circuits are low it is important that out-of-band performance is also simulated during the design cycle such that unwanted spurious signals are not generated. The layout of the RF boards is achieved automatically using the Serenade Layout Editor of Compact Software following simulation using either the Super-Compact or Microwave Harmonica linear and nonlinear simulators. Information on the circuit topology is supplied to both the simulators and the layout tool using the Serenade Schematic Editor. A description is also given of the way that large-signal, Spice-compatible transistor models, contained in a standard device library, are generated using the Scout PC for Windows parameter extraction software.

Designing RF Subsystems with "Building Blocks"

A few years ago many circuit designers used discrete active and passive components to build circuit functions such as amplifiers, switches, modulators, oscillators and mixers. Today, more and more circuits are being produced in integrated format so that the task of a designer has shifted towards interfacing such circuits on a single printed circuit board that can be produced at low-cost after a short development cycle. Therefore, the emphasis of CAD simulator vendors, such as Compact Software, has been focused recently at low microwave and RF frequencies to supplying useful device data for IC "building blocks". A simple example of this is the device data available for the MSA series of Si MMIC amplifiers from Hewlett-Packard/Avantek. This data is available in a standard small-signal device library that comes as part of the Super-Compact simulator software. Table 1 shows an example of the MSA- series data of which there are 30 different types in the device library. Small-signal data consists of s-parameters and noise parameters at a number of frequencies and device bias conditions.

AV086 100MHZ 6000MHZ 14 50.0 1

AV086 AVANTEK MSA0870 V= v, I = 36mA

0.1GHZ	.65	-19	42.04	161	.015	40	.64	-22
0.2GHZ	.60	-35	37.54	145	.021	47	.58	-43
0.4GHZ	.48	-60	28.49	122	.030	51	.47	-74
0.6GHZ	.40	-76	21.90	108	.040	50	.38	-97
0.8GHZ	.35	-88	17.48	97	.049	50	.33	-113
1.0GHZ	.32	-102	14.85	87	.057	51	.28	-128
1.5GHZ	.29	-118	10.14	70	.071	47	.22	-151
2.0GHZ	.30	-133	7.55	56	.081	45	.16	-167
2.5GHZ	.31	-139	6.01	49	.100	46	.12	-172
3.0GHZ	.32	-149	4.87	39	.106	41	.07	-170
3.5GHZ	.34	-158	4.09	28	.121	35	.07	-143
4.0GHZ	.34	-168	3.48	17	.131	31	.12	-112
5.0GHZ	.33	161	2.63	-3	.147	21	.19	-103
6.0GHZ	.39	128	2.04	-22	.155	10	.21	-115

AV087 100MHZ 6000MHZ 14 50.0 1

AV087 AVANTEK MSA0835 V= v, I = 36mA

0.1GHZ	.63	-17	42.02	161	.013	55	.63	-19
0.2GHZ	.58	-33	37.52	145	.021	47	.56	-37
0.4GHZ	.49	-56	28.50	119	.033	54	.42	-66
0.6GHZ	.40	-70	21.54	103	.040	55	.32	-84
0.8GHZ	.35	-80	17.01	92	.050	53	.24	-98
1.0GHZ	.33	-89	13.98	82	.057	52	.18	-107
1.5GHZ	.30	-111	9.45	64	.079	51	.09	-126
2.0GHZ	.30	-133	7.03	48	.098	44	.07	-141
2.5GHZ	.32	-150	5.53	39	.110	42	.06	-166
3.0GHZ	.34	-170	4.56	26	.122	36	.06	-106
3.5GHZ	.38	175	3.86	14	.133	32	.08	-100
4.0GHZ	.39	162	3.33	2	.146	27	.12	-101
5.0GHZ	.41	132	2.47	-21	.165	19	.21	-113
6.0GHZ	.52	95	1.94	-45	.187	7	.20	-149

Table 1 Extract of S-Parameter Data from the Avantek Device Library in Super-Compact Format

Similar device libraries are available for companies such as Siemens, Philips, NEC and Motorola.

If we take the device data for a typical MSA-series amplifier module, such as the MSA-0870, we can plot the gain, input and output reflection coefficients and stability factor, K, of the amplifier as a function of frequency using a linear circuit simulator such as Super-Compact. The gain, |S21|, and stability factor, K, are

plotted in Figure 1 and Figure 2 shows the input and output reflection coefficients, |S11| and |S22| of the amplifier.

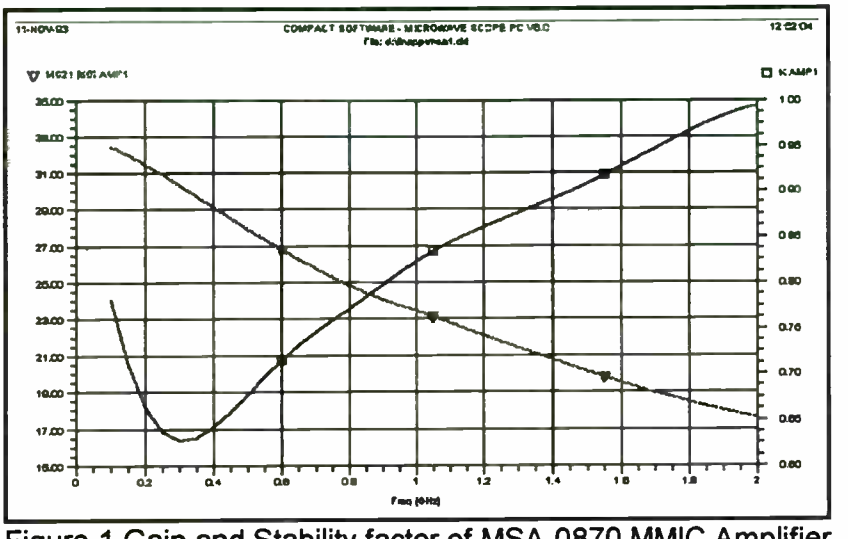

Figure 1 Gain and Stability factor of MSA-0870 MMIC Amplifier

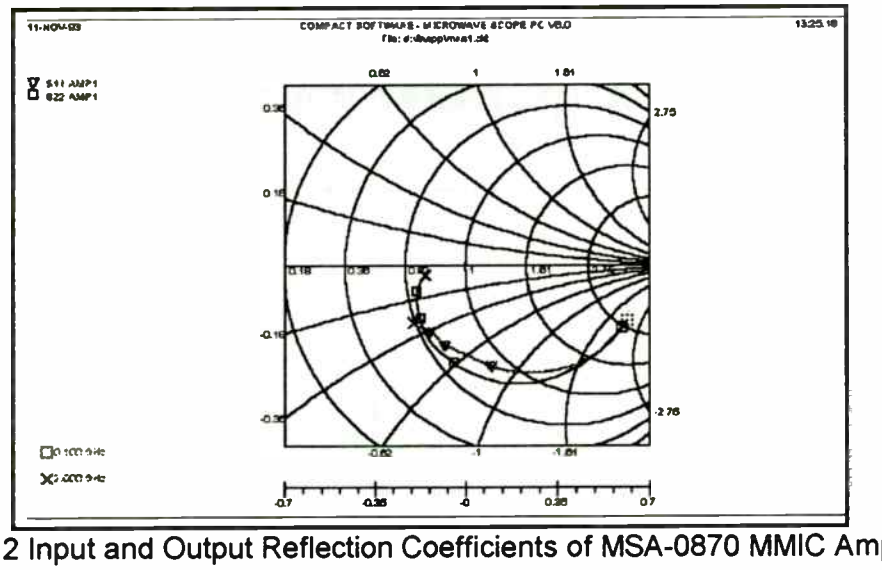

Figure 2 Input and Output Reflection Coefficients of MSA-0870 MMIC Amplifier

The stability factor of the amplifier is less than 1 over the entire 100 MHz to 2 GHz frequency range. The gain of the amplifier also increases as frequency decreases - a recipe for the amplifier to be capable of oscillating at one or more frequencies if presented at its input or output with a certain impedance. Both the input and output return losses are less than 10 dB at 800 MHz. In order to improve the performance of this amplifier we both stabilize and match the MMIC module. Matching is centered at 800 MHz for the example application. Figure 3 shows a schematic of the modifications done on the basic MSA0870 amplifier to produce a stable, well-matched amplifier design. 10 ohm series resistors are used at the input and output of the amplifier together with a 300 ohm shunt resistor on the amplifier input to stabilize the amplifier. Figures 4(a) and (b) show

the K-factor of the amplifier after stabilization with the gain and the input and output return losses respectively. Notice that the gain now decreases below 600 MHz. It is important in RF circuit design to consider the potential out-of-band performance of broadband "building blocks" as this may cause unwanted problems.

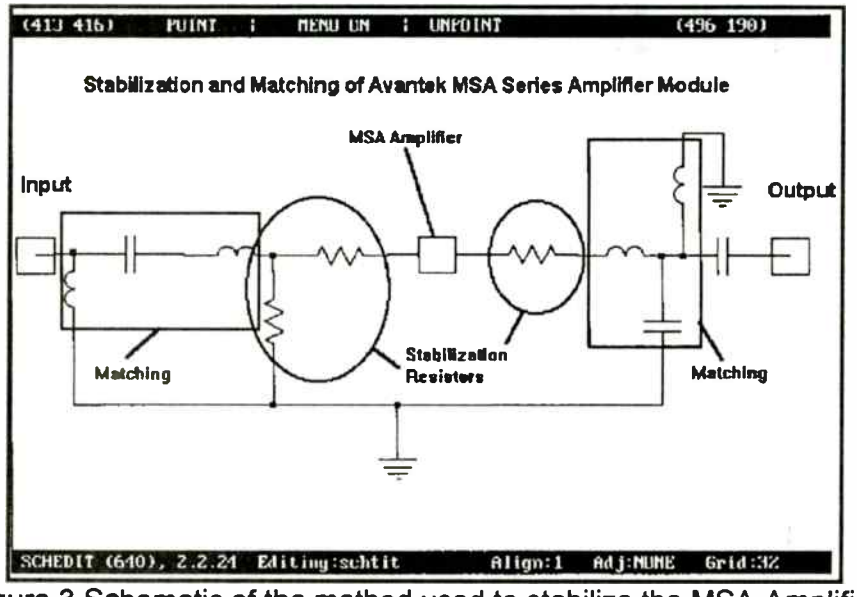

Figure 3 Schematic of the method used to stabilize the MSA Amplifier

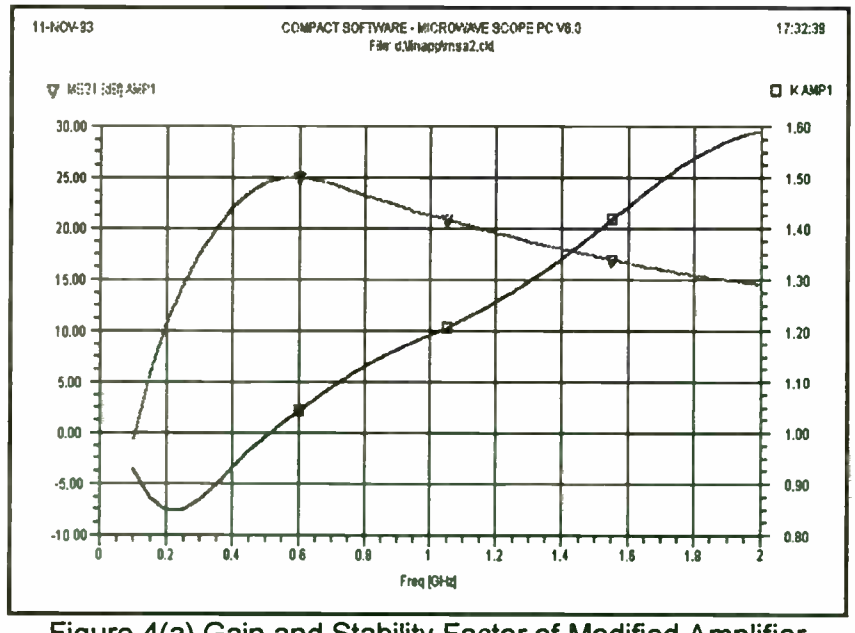

Figure 4(a) Gain and Stability Factor of Modified Amplifier

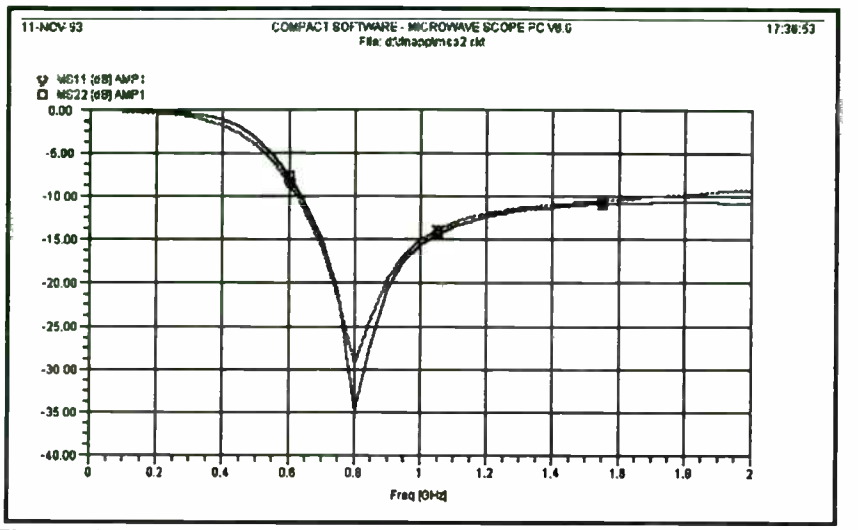

Figure 4(b) Input and Output Return Losses of Modified Amplifier

Generating Large-Signal Models for Simulation

In order to achieve meaningful simulation of RF circuits and sub-systems it is necessary to model both the active and the passive components used in the designs. Accurate, large-signal, nonlinear models of active devices, such as transistors, are commonly available at low frequencies as Spice models. However, at frequencies above a few hundred megahertz, these models give inaccurate results. Amongst other reasons the bias-dependent equivalent circuit models that are used generally "lump" the parasitic reactances into the device model so that at RF and microwave frequencies the s-parameters can be very inaccurate.

To overcome this situation we have developed a method of extracting the large-signal models of diodes and transistors using multiple-bias point s-parameter data either supplied by the device manufacturer or measured at Compact Software. In a later section of this paper we describe the design of a UHF amplifier employing surface-mount devices. In order to simulate both the small-signal, linear and large-signal, nonlinear characteristics of this amplifier it is necessary to have RF models for the transistors as well as the passive components. The UHF amplifier employs a Siemens CFR 182 bipolar transistor packaged in a SOT-23 package having an f_t of 8 GHz and a noise figure of 1.2 dB at 900 MHz. The manufacturer supplies s-parameters from 100 MHz to 3 GHz in the data-sheet for the device at a variety of V_{ce} and I_b values but no Spice or large-signal model. Using the Scout™ PC for Windows parameter extraction program we have produced a modified Gummel-Poon large-signal model for the device. Table 2 shows the values for the equivalent circuit components in this large-signal model. The model simultaneously fits the D-C current-voltage transfer curves and the multiple-bias s-parameters of the transistor. For example, Figure 5 shows the DC I-V curves for the CFR 182 transistor modeled by the Gummel-Poon model as well as measured points.

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END
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  BF     OPT    100.00          118.61          200.00      ;
  NF     FIX    .10000          .99620          2.0000      ;
  VA     OPT    28.000          31.225          45.000      ;
  IKF    OPT    .10000E-02      1.1730          3.0000      ;
  ISE    OPT    .10000E-16      .10000E-16      .10000E-05  ;
  NE     FIX    .10000          1.7820          20.000      ;
  BR     FIX    1.0000     ;
  NR     FIX    1.0000     ;
  VB     FIX    2.9000     ;
  IKR    FIX    .50000     ;
  ISC    FIX    .10000E-17      .10000E-16      .10000E-11  ;
  NC     OPT    .10000          2.0000          4.0000      ;
  RBM    OPT    .10000E-04      5.0000          5.0000      ;
  RB     OPT    .10000          16.479          200.00      ;
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  CJE    OPT    .00000          .10271E-11      .20000E-10  ;
  VJE    FIX    .45000          1.0150          2.0000      ;
  MJE    FIX    .20000          .35600          1.0000      ;
  CJC    OPT    .00000          .14670E-12      20000E-10   ;
  VJC    FIX    .45000          .63500          1.0000      ;
  MJC    FIX    .20000          .71100          1.0000      ;
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  FC     FIX    .30000          .50000          1.0000      ;
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  XTF    OPT    .10000          .10000          30.000      ;
  VTF    OPT    .10000          .10009          20.000      ;
  ITF    OPT    .10000E-02      .80000          .80000      ;
  TR     FIX    .10000E-13      .12000E-11      .10000E-09  ;
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  RC2    OPT    .10000          .20172          50.000      ;
  LB     OPT    .00000          .13820E-08      .50000E-08  ;
  LE     OPT    .00000          .32086E-10      .50000E-08  ;
  LC     OPT    .00000          .15534E-08      .50000E-08  ;
  CBCD   OPT    .00000          .15516E-12      1.0000      ;
  RB2    OPT    .10000          6.0484          20.000      ;
  CBEP   OPT    .00000          .60764E-14      1.0000      ;
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  CCEP   OPT    .00000          39446E-13       1.0000      ;
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  ZCT    FIX    50.000     ;
  LCT    OPT    .10000E-03      .20056E-02      .38000E-02  ;
  ZET    FIX    50.000     ;
  LET    OPT    .00000          .50322E-02      .68000E-02  ;
END
*
DCDATA
DCDATAFILE Bfr1.bfr  ;
END
*
SDATA
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 SDATAFILE      BFR10.SMP      BFR1.FLP  ;
 SDATAFILE      BFR15.SMP      BFR1.FLP  ;
 SDATAFILE      BFR20.SMP      BFR1.FLP ;
 SW     FMIN    0.1E9    FMAX    3E9
* SW    VCEMAX 6.5      IBMIN 30E-6      W 10 5  8 2  5 5  10 3 ;
* 30E-6 W 10 5  8 2  5 5  10 3 ;  SW VCEMAX 12.0 FMIN 1E9 FMAX 1E10 W 30 10  8 5  5 1  15 5 ;
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Table 2 Gummel-Poon Model of CFR 182 BJT within Scout Netlist

Figure 6 shows a typical set of s-parameters for the transistor as provided by the model compared to the s-parameters provided in the manufacturer's data-sheet.

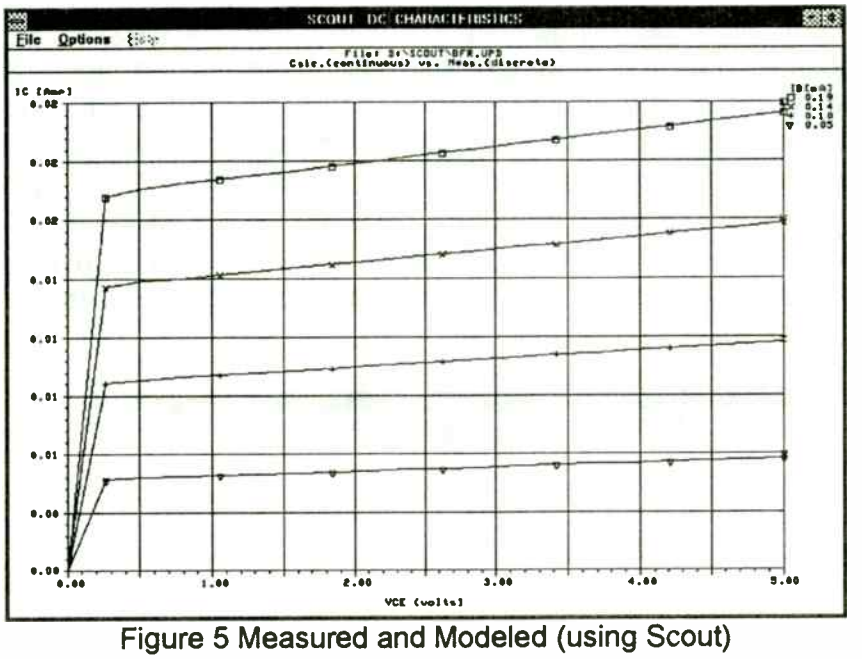

Figure 5 Measured and Modeled (using Scout)
DC Characteristics of BFR182 Transistor

The large-signal model of the BJT is then inserted into the Microwave Harmonica nonlinear harmonic balance simulator. A basic biasing circuit can be used to check the DC characteristics of the device and a small-signal equivalent circuit can be generated automatically. This small-signal equivalent circuit is consistent with the large-signal circuit -- s-parameters derived from the large-signal model at very low RF power levels agree with the s-parameters derived from the small-signal equivalent circuit. Microwave Harmonica also has the unique ability to automatically provide noise parameters of the transistor from the bias-dependent equivalent circuit. The noise model for bipolar junction transistors is based on the work of Hawkins (ref. 1). This model is extended to allow the simulation of the noise properties of circuits operating under nonlinear conditions (typically, mixers).

Modeling Passive Surface-Mount Devices

It is equally important to model accurately the RF characteristics of passive surface-mount devices (SMDs). SMDs should be generally chosen for lowest parasitics and highest frequency of operation, if possible. At Compact Software we measure SMDs using a variety of test fixtures including those employing microstrip on glass-fiber board. s-parameter measurements are generally required because the majority of SMD manufacturers only supply such characteristics as self-resonant frequency, Q and very low frequency component value. RF equivalent circuits are developed to Include mounting and solder pad

parasitics. Typical equivalent circuits for chip resistors, capacitors and inductors are shown in Figures 7, 8 and 9. SMD resistors can be effectively modeled as a cascade of transmission lines and resistors -- for example, the physical length of the resistor chip can be divided by ten (and the corresponding individual resistors become 1/10 the original) with ten transmission lines having the physical width of the chip producing a broadband, distributed RF model (Figure 7). SMD capacitors can be modeled using the lumped equivalent circuit shown in Figure 8 where the resistor models the Q-factor of the capacitor, the transmission lines model the distributed, parasitic effects of the chip. Similarly, chip inductors can be modeled using the equivalent circuit of Figure 9 where the resistor models the Q-factor of the inductor and the capacitors model the self-resonant frequencies.

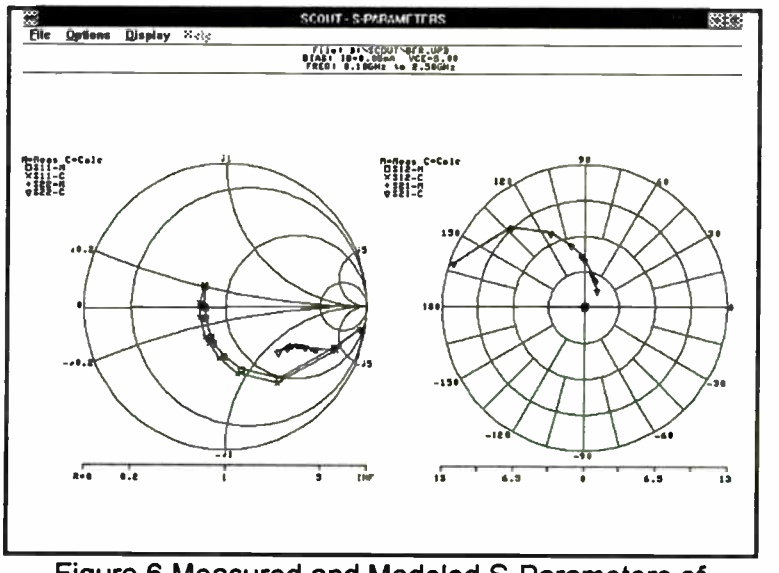

Figure 6 Measured and Modeled S-Parameters of BFR182 Transistor at V_{ce}=5v; I_b=.05mA

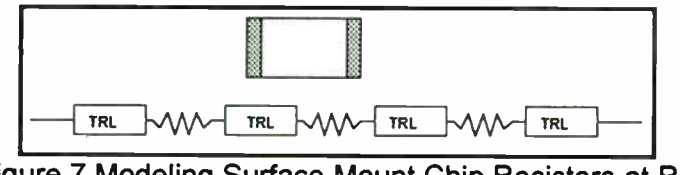

Figure 7 Modeling Surface-Mount Chip Resistors at RF

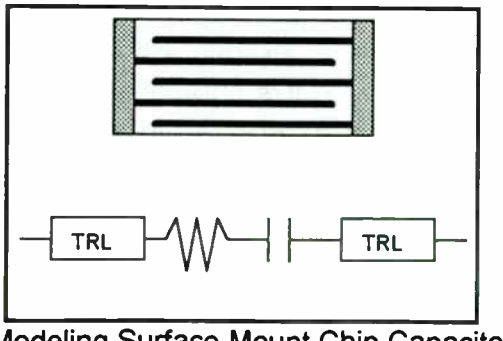

Figure 8 Modeling Surface-Mount Chip Capacitors at RF

Figure 9(b) shows a comparison in the phase angles of S11 and S21 for a 20 nH SMD chip inductor where only the indctance is assumed or an equivalent circuit model is assumed.

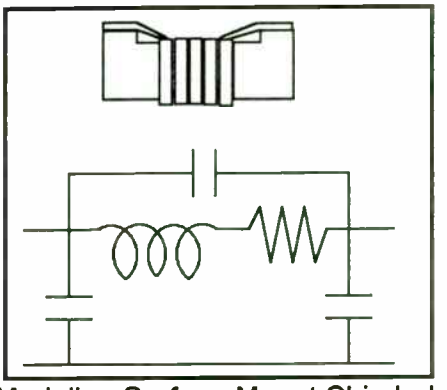

Figure 9(a) Modeling Surface-Mount Chip Inductors at RF

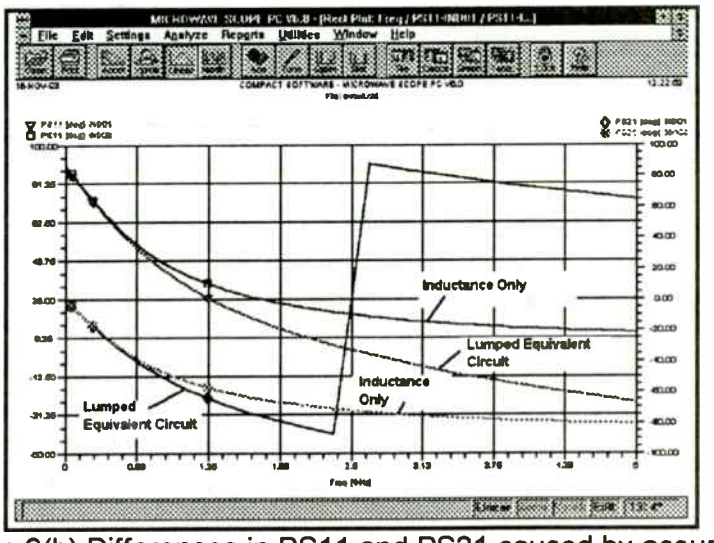

Figure 9(b) Differences in PS11 and PS21 caused by assuming chip inductor is purely inductive or is represented by lumped equivalent circuit

The electrical models of the SMD components are "linked" to layout footprints. Compact Software's Serenade Layout Editor takes data supplied by its companion Schematic Editor and provides auto-generation of planar circuit layouts. The Layout Editor is a software overlay to the popular AutoCAD package from Autodesk. Scaled drawings of SMDs are contained in a footprint library and are accessed from the relevant part names in the property pages of the schematic components.

An Example of an RF Surface-Mount Circuit Design

An example is given in this section of the paper on the design of a UHF BJT amplifier employing the CFR 182 transistor. The maximum available gain, GMAX, and stability factor, K, can be derived from the small-signal s-parameters

of the transistor. These are shown in Figure 10 from 100MHz to 1000MHz. Note that the K factor of the transistor is less than 1 over the 400 MHz to 500 MHz frequency range. The transistor can be stabilized in that frequency range by adding a parallel feedback resistor of 4700 ohms between base and collector (the resulting K-factor is also shown in Figure 10(a)).

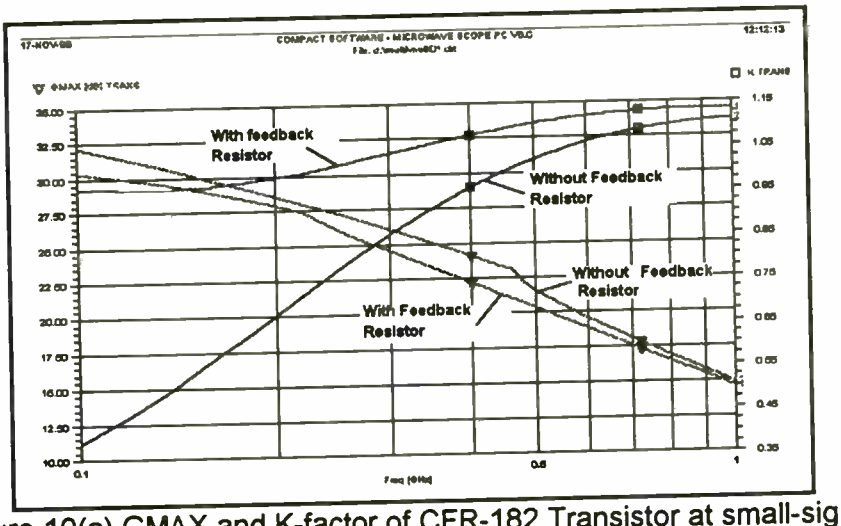

Figure 10(a) GMAX and K-factor of CFR-182 Transistor at small-signal

The noise figure of the transistor can be calculated directly from the small-signal equivalent circuit (derived from the large-signal, Spice-compatible model at the required bias point). For example, the minimum noise figure at Vce=5volt and Ic=6mA is plotted in Figure 10(b). The squares represent the noise figures quoted in the device data sheet. Noise parameters include the effect of low frequency flicker (1/f) noise. A schematic of the UHF amplifier is shown in Figure 11. The small-signal performance of this amplifier including a complete electrical description of the surface-mount components, directly related to the layout of the circuit, is shown in Figure 12.

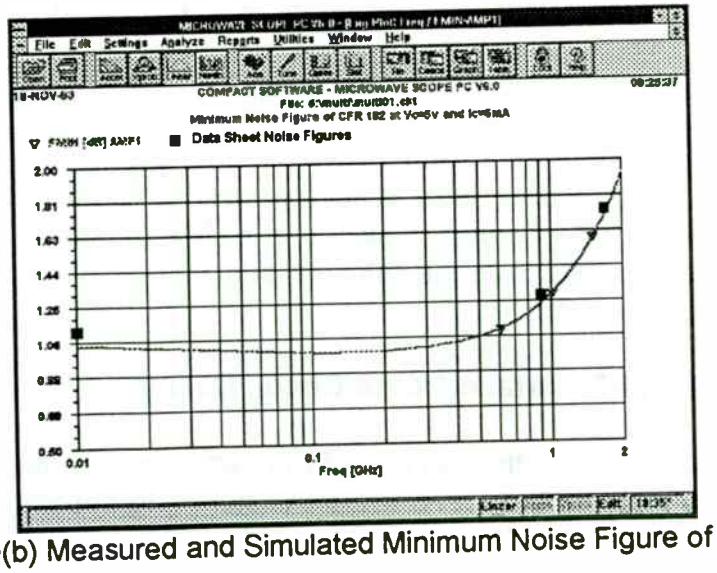

Figure 10(b) Measured and Simulated Minimum Noise Figure of CFR 182

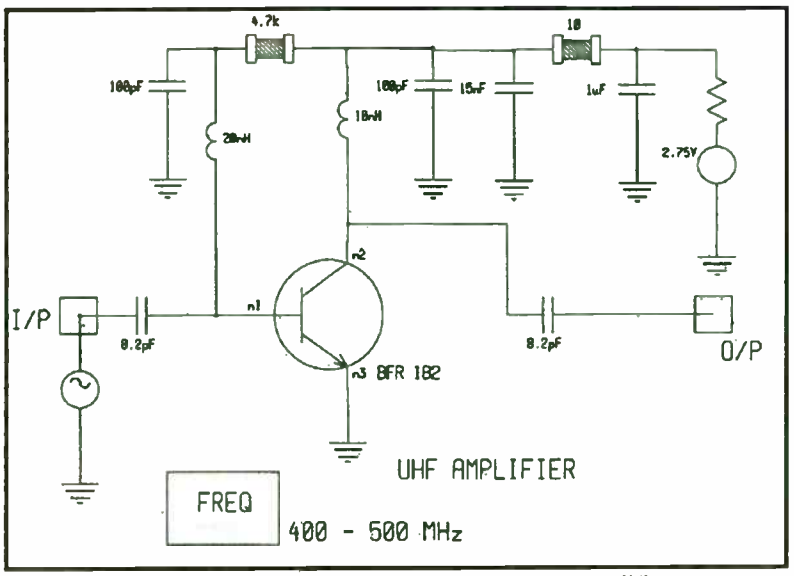

Figure 11 Schematic of UHF BJT Amplifier

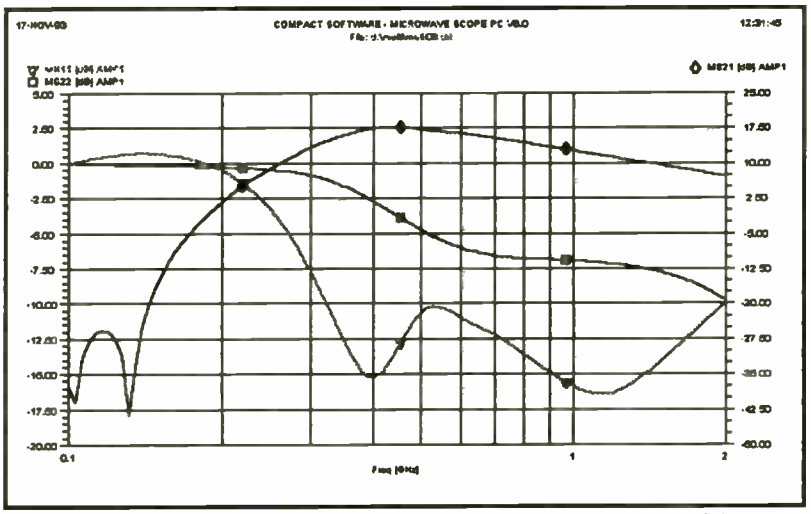

Figure 12 Small-Signal Performance of UHF Amplifier

Next a nonlinear simulation of the amplifier is performed using Microwave Harmonica to investigate the compression characteristics. Figure 13 displays the simulated large-signal gain as a function of swept RF input power -- the output 1 dB gain compression point of the amplifier is + 7dBm. The fundamental, second and third harmonic levels are shown in Figure 14 again as a function of RF input

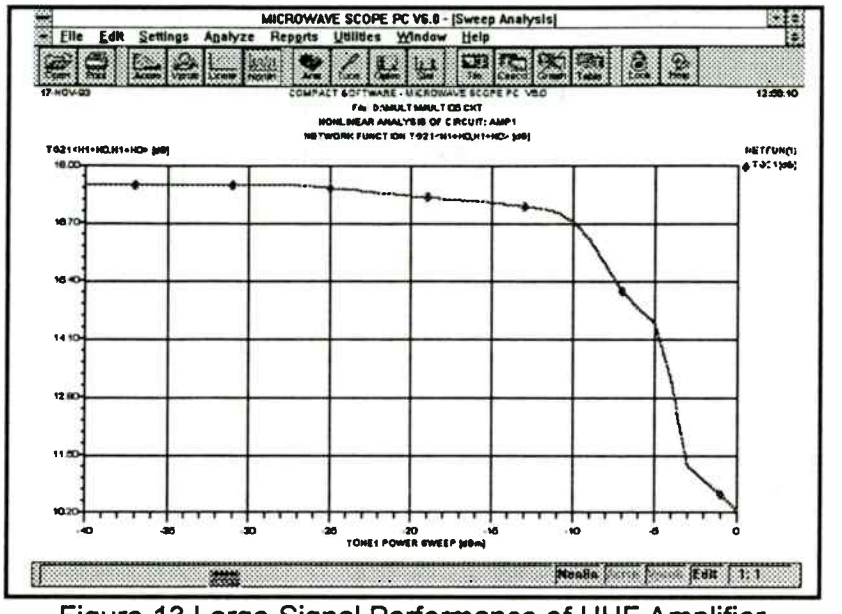

Figure 13 Large-Signal Performance of UHF Amplifier

power level, where at low RF power levels they have a 1:2:3 ratio. This type of plot allows the designer to calculate the third-order intercept point of the amplifier, which in this case is +28 dBm. The measured performance of this amplifier when fabricated on PCB material having a dielectric constant of 2.2 was within 0.5 dB of the simulated small-signal gain and 1dB gain compression point. However, it was noticed that the amplifier was prone to oscillations when the input RF power was close to that needed for 1 dB compression. Simulations using Microwave Harmonica allow the large-signal conversion parameters to be calculated and the RF power dependent amplifier stability factor to be determined. Figure 15(a) shows the K-factor plotted over the -40 dBm to 0 dBm RF input power level. It will be noticed that the K-factor value decreases significantly below unity in the region of the 1 dB gain compression value confirming that the amplifier may oscillate under certain loading conditions and may produce harmonically unrelated oscillations compared to the input signal frequency. The intermodulation performance of the amplifier was tested by injecting three tones into the amplifier input at levels of -17dBm, -23dBm and -23dBm. the intermodulation products were 30 dB down on the input signals due to the fact that the amplifier is designed to operate from a 2.5 volt rail at 20 mA only.

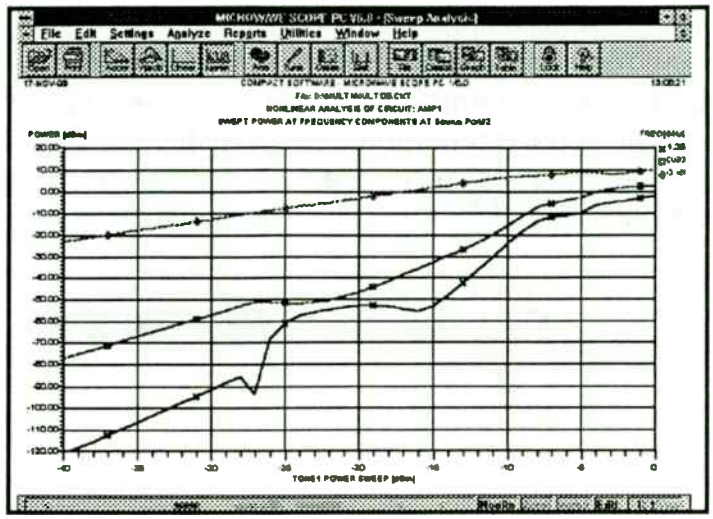

Figure 14 Fundamental, Second and Third Harmonics at Output of Amplifier as a function of RF Input Power

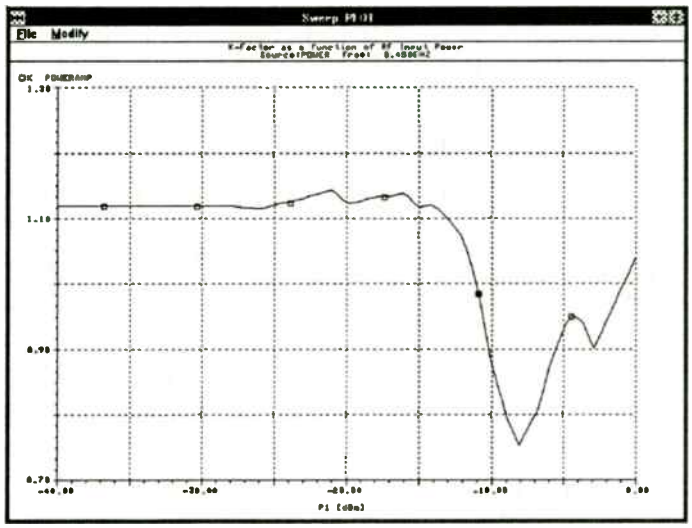

Figure 15(a) Stability Factor of Amplifier at 450 MHz as a function of RF Input Power

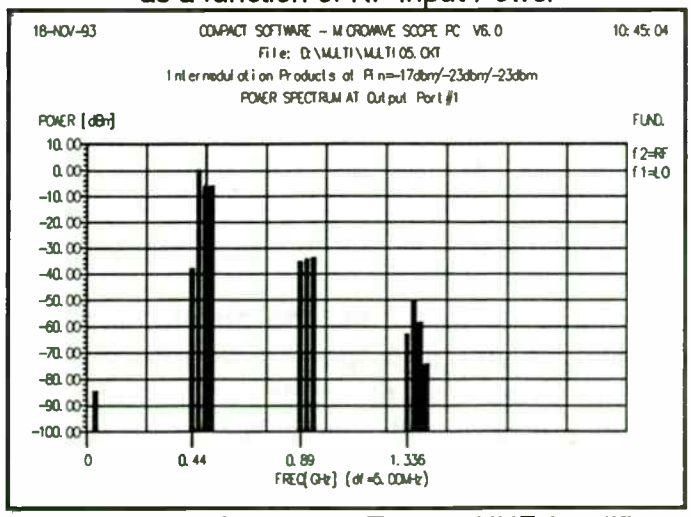

Figure 15(b) Three-Tone Test on UHF Amplifier

Manufacturing yield is most important in commercial RF products so that re-works are minimized (or that the number of potential re-works is so low that they can be discarded) and performance is reproducible. Figure 16 shows a histogram of the small-signal gain of the UHF amplifier at 450 MHz when all the components (including the transistor) have 10% normally distributed tolerances. 1000 trials yields a pass rate of 58% for amplifiers with gains between 16 and 18 dB, for example.

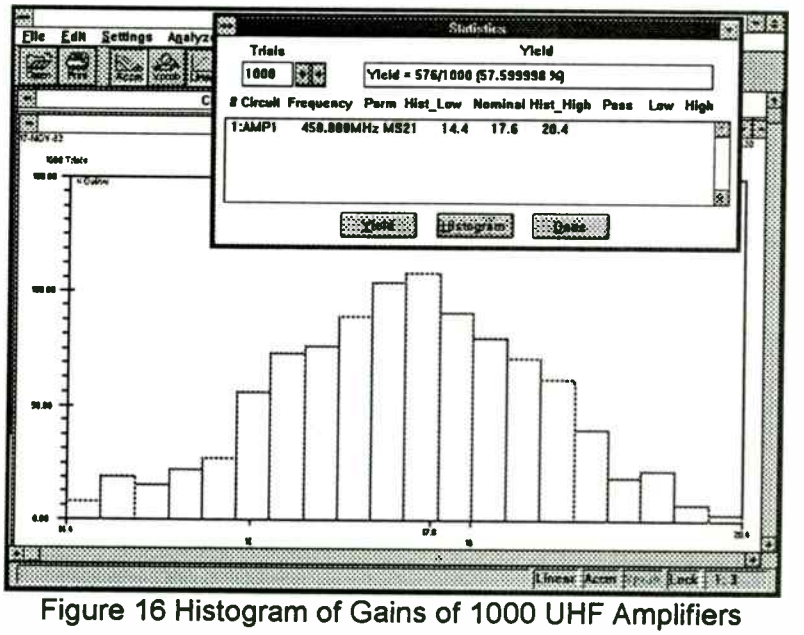

Figure 16 Histogram of Gains of 1000 UHF Amplifiers

Finally, the same schematic that was used to generate the circuit netlist for simulation is used to automatically generate the layout. The layout editor can provide multiple layers for metals, dielectrics, drill holes etc..The SMDs are represented in layout using footprints. The footprints are drawn to scale in the layout to represent the actual size of the SMD. Some intellegence is given to the footprints, by specifying the location of the connection points and the angles at which transmission lines should be connected to the footprint. The footprint name for the SMD is specified in the schematic within the property page of the element or sub-circuit. The above footprint name and connectivity information is used to automatically generate the layout. The orientation of the elements are obtained from schematic and therefore give the user the capability to control the orientation of the entire layout. Text can be added to the footprint or the layout in any layer, depending on the type of output that will be generated.

Some of the other features for layout include maintenance of the footprints in footprint libraries, editing element properties, regeneration, back-annotation, step and repeat of the layout and title block information for documentation. Figure 17 shows the layout of the UHF amplifier as an assembly drawing with the SMDs in place.

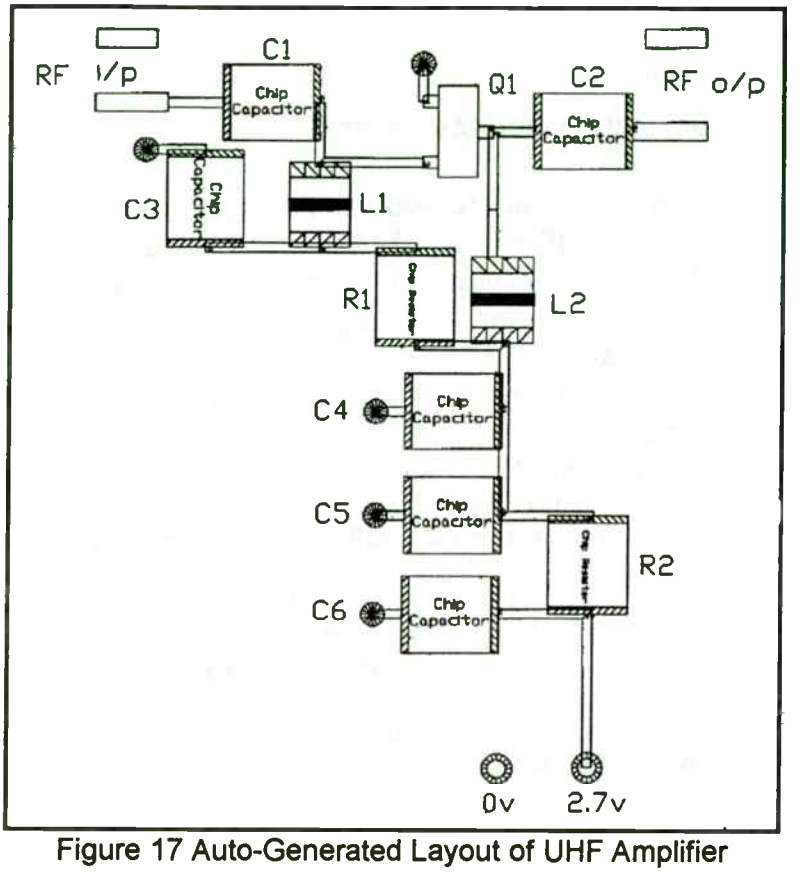

Figure 17 Auto-Generated Layout of UHF Amplifier

Conclusions

This paper has given an overview of the use of modern linear and nonlinear simulators in the design of RF circuits and subsystems using surface-mount devices. Techniques have been described for the small- and large-signal modeling of transistors and the RF modeling of passive SMDs. Input to the simulation engines is provided by schematic entry which is also linked to an automatic planar layout tool.

Reference

1. Pucel R. A., Rohde U. L., "An Exact Expression for the Noise Resistance R_n for the Hawkins Bipolar Noise Model" IEEE Microwave and Guided Wave Letters, Vol. 3, No. 2, February 1993, pp. 35-37

The Accurate Simulation of Oscillator and PLL Phase Noise in RF Sources*

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Compact Software, Inc.

1 INTRODUCTION TO SIDEBAND NOISE

One of the key criteria in oscillators is the signal-to-noise ratio of an oscillator at certain offsets from the carrier. The main sources of the phase are flicker noise contribution of the semi-conductor, the noise figure of the semi-conductor under large signal conditions and the filter effect of the resonator.

The actual phase noise of an oscillator is a composite of near- and far-carrier noise.

If the spectral power density is measured at the output of an oscillator, a curve such as that of Figure 1 is observed. Rather than all of the power being concentrated at the oscillator frequency, some is distributed in frequency bands on both sides of the oscillator frequency.

As noise is a form of stability, it is useful to characterize frequency stability in the time domain in several areas. Short-term stability extends between a very small fraction of a second to 1 s, maybe under some considerations up to 1 min, and the value for the stability between 1 s and 1 min will be about the same. For longer time periods, we talk about long-term stability or aging. The aging is typically expressed in forms of how many parts in 10^{-10} or 10^{-11} per day the frequency changes. This information is in the time domain; in the frequency domain, we find terms like "random walk," "flicker," and "wide phase noise" which describe the slope of spectral density. The Fourier frequency, at times labeled f_m, is at times called sideband frequency, offset frequency, modulation frequency, or baseband frequency. In this book we will refer to it as *offset frequency*, describing the signal-to-noise ratio of an oscillator at a certain offset off the center frequency. The most common characterization of phase noise of a source is the frequency power density, and the probable reason for this is that it can be seen only as a spectrum analyzer when the AM noise contribution is insignificant. The spectrum analyzer display is then symmetrical.

Each one takes one side and by looking at sideband noise in a 1-Hz bandwidth leads to the definition of $\mathcal{L}(f_m)$. $\mathcal{L}(f_m)$ is defined as the ratio of the single sideband power of phase noise in a 1-Hz bandwidth f_m hertz away from the carrier frequency to the total signal power. This is plotted in Figure 1.

These unwanted frequency components are now referred to as *oscillator noise*. The oscillator output $S(t)$ can be expressed by the equation

$$S(t) = A(t) \cos [\omega_o t + \theta(t)] \qquad (1)$$

where $A(t)$ describes the amplitude variation as a function of time and $\theta(t)$ is the phase variation. $\theta(t)$ is referred to as *phase noise*. A well-designed, high-quality oscillator is very amplitude stable and $A(t)$ can be considered constant. For a constant-amplitude signal, all oscillator noise is due to $\theta(t)$. Leeson [1] has developed a linear model that describes the origins of phase noise in oscillators, and since it closely fits experimental data, the model is widely used in describing the phase noise of oscillators and frequency synthesizers. Leeson's linearized oscillator model for phase noise will be described, but first a relation between the observed power spectral density function and $\theta(t)$ will be developed.

**Based on "All About Phase Noise in Oscillators" to be published in QEX in December, 1993/January, 1994 by the American Radio Relay League. Re-used by permission.*

A carrier signal of amplitude V which is frequency modulated by a sine wave of frequency f_m can be represented by the equation

$$S(t) = V \cos\left(\omega_o t + \frac{\Delta f}{f_m} \sin \omega_m t\right) \qquad (2)$$

where Δf is the peak frequency deviation and $\theta_p = \Delta f / f_m$ is the peak phase deviation, often referred to as the *modulation index* β. Equation (2-2) can be expanded as

$$\begin{aligned} S(t) = V[&\cos(\omega_o t) \cos(\theta_p \sin \omega_m t) \\ &- \sin \omega_o t \sin(\theta_p \sin \omega_m t)] \end{aligned} \qquad (3)$$

If the peak phase deviation is much less than 1 ($\theta_p \ll 1$),

$$\cos(\theta_p \sin \omega_m t) \approx 1$$

and

$$\sin(\theta_p \sin \omega_m t) \approx \theta_p \sin \omega_m t$$

Thus for $\theta_p \ll 1$, the signal $S(t)$ is approximately equal to

$$\begin{aligned} S(t) &= V[\cos(\omega_o t) - \sin \omega_o t\,(\theta_p \sin \omega_m t)] \\ &= V\left\{\cos(\omega_o t) - \frac{\theta_p}{2}[\cos(\omega_0 + \omega_m)t - \cos(\omega_0 - \omega_m)t]\right\} \end{aligned} \qquad (4)$$

That is, when the peak phase deviation is small, the phase deviation results in frequency components on each side of the carrier of amplitude $\theta_p/2$. This frequency distribution of a narrowband FM signal is useful for interpreting an oscillator's power spectral density as being due to phase noise. The phase noise in a 1-Hz bandwidth has a noise power-to-carrier power ratio of

$$\mathcal{L}(f_m) = \left(\frac{V_n}{V}\right)^2 = \frac{\theta_p^2}{4} = \frac{\theta_{rms}^2}{2} \qquad (5)$$

The total noise is the noise in both sidebands and will be denoted by S_θ. That is,

$$S_\theta = 2\frac{\theta_{rms}^2}{2} = \theta_{rms}^2 = 2\mathcal{L}(f_m) \qquad (6)$$

With this interpretation of the noise power, the noise can now be described in terms of its origin, see Figure 2.

Noise can be expressed in a number of ways; therefore, we want to try to cover the various methods of describing other forms of stability before we analyze the oscillator.

2 SPECTRAL DENSITY OF FREQUENCY FLUCTUATIONS, RELATED TO $S_{\Delta\theta}$ AND $\mathcal{L}$

Stability measurements with using frequency comparators give the *spectral density of frequency fluctuations*,

$$S_{\Delta f}(f_m) = \Delta f_{rms}^2 \qquad (7)$$

To relate the spectral density of frequency fluctuations to the spectral density of phase noise, we recall that

$$\Delta f(t) = \frac{1}{2\pi} \frac{d\,\Delta\theta(t)}{dt} \qquad (8)$$

Transformed into the frequency domain,

$$\Delta f(f_m) = f_m\, \Delta\theta(f_m) \qquad (9)$$

$$S_{\Delta f}(f_m) = \Delta f_{rms}^2(f_m) = f_m^2 S_{\Delta\theta}(f_m) = 2 f_m^2 \mathcal{L}(f_m) \qquad (10)$$

NBS proposes to standardize the definition of the spectral density of fractional frequency fluctuations. The instantaneous frequency deviation is normalized to the carrier frequency f_o.

$$y(t) = \frac{\Delta f(t)}{f_o} \tag{11}$$

$$S_y(f_m) = \frac{1}{f_o^2} S_{\Delta f}(f_m) = \frac{f_m^2}{f_o^2} S_{\Delta\phi}(f_m) = \frac{2f_m^2}{f_o^2} \mathcal{L}(f_m) \tag{12}$$

Characterizing fractional frequency fluctuations allows better comparison between sources with different carrier frequencies.

3 RESIDUAL FM RELATED TO $\mathcal{L}(f_m)$

Residual FM, the total rms frequency deviation within a specified bandwidth, is another common way to specify the frequency stability of signal generators. Commonly used bandwidths are 50 Hz to 3 kHz, 300 Hz to 3 kHz, and 20 Hz to 15 kHz.

$$\Delta f_{res} = \sqrt{2} \sqrt{\int_a^b \mathcal{L}(f_m) f_m^2 \, df_m} \tag{13}$$

Table 1 correlates Δf_{res} and $\mathcal{L}(f_m)$ for specific slopes of $\mathcal{L}(f_m)$ and $\mathcal{L}$ at 1 kHz = −100 dBc.

TABLE 1

	Slope of $\mathcal{L}(f_m)$		Residual FM Δf_{res}		
$\mathcal{L}$[a] at 1 kHz (dBc)	Exponent	dB/oct	50 Hz to 3 kHz	300 Hz to 3 kHz	20 Hz to 15 kHz
−100	0	0	1.34	1.34	15.0
−100	−1	−3	0.95	0.94	4.74
−100	−2	−6	0.77	0.73	1.73
−100	−3	−9	0.90	0.68	1.15

[a]For any $\mathcal{L}$ at 1 kHz different to −100 dBc, multiply Δf_{res} of the table by

$$\text{antilog} \frac{100 - |\mathcal{L} \text{ at 1 kHz/dBc}|}{20}$$

The table does not take into account any microphonic or spurious sidebands.

Example: $\mathcal{L}$ at 1 kHz = −88 dBc, slope −9 dB. For bandwidth 20 Hz to 15 kHz:

$$\Delta f_{res} = 1.15 \text{ Hz} \times \text{antilog} \frac{100 - 88}{20} = 4.6 \text{ Hz}$$

4 ALLAN VARIANCE RELATED TO $\mathcal{L}(f_m)$

For many applications, such as high-stability crystal oscillators or doppler radar systems, it is more relevant to describe frequency stability in the time domain. The characterization is based on the sample variance of fractional frequency fluctuations. Averaging differences of consecutive sample pairs with no deadtime in between

yields the *Allan variance*, $\sigma_y^2(\tau)$, which is the proposed standard measure of frequency stability.

$$\sigma_y^2(\tau) \sim \frac{1}{2(M-1)} \sum_{k=1}^{M-1} (\bar{y}_{k+1} - \bar{y}_k)^2 \qquad (14)$$

$\bar{y}_k$ is the average fractional frequency difference of the kth sample measured over sample time τ.

Conversions from frequency- to time-domain data and vice versa are possible but tedious. The power spectrum $\mathcal{L}(f_m)$ needs to be approximated by integer slopes of 0, −1, −2, −3, −4. Then conversion formulas (see Table 2) can be applied. A good description of this procedure is given in Refs.[2]and [3] .

TABLE -2 CONVERSION TABLE[a]

	Slope of $\sigma_y^2(\tau)$	$\sigma_y(\tau) =$	$\mathcal{L}(f) =$	Slope of $\mathcal{L}(f)$
White phase	−2	$\frac{\sqrt{\mathcal{L}(f) f_h}}{2.565 f_o}\tau^{-1}$	$\frac{[\sigma_y(\tau)\tau f_o(2.565)]^2}{f_h} f^0$	0
Flicker phase	−1.9	$\frac{\sqrt{\mathcal{L}(f) f[2.184 + \ln(f_h\tau)]}}{2.565 f_o}\tau^{-1}$	$\frac{[\sigma_y(\tau)\tau f_o(2.565)]^2}{2.184 + \ln(f_h\tau)} f^{-1}$	−1
White frequency	−1	$\frac{\sqrt{\mathcal{L}(f) f^2}}{f_o}\tau^{-1/2}$	$[\sigma_y(\tau)\tau^{1/2} f_o]^2 f^{-2}$	−2
Flicker frequency	0	$\frac{1.665\sqrt{\mathcal{L}(f) f^3}}{f_o}\tau^0$	$0.361[\sigma_y(\tau) f_o]^2 f^{-3}$	−3
Random walk frequency	+1	$\frac{3.63\sqrt{\mathcal{L}(f) f^4}}{f_o}\tau^{1/2}$	$[(0.276)\sigma_y(\tau)\tau^{-1/2} f_o]^2 f^{-4}$	−4

[a] τ = measurement time, $y = \Delta f_o/f_o$, f_o = carrier, f = sideband frequency, f_h = measurement system bandwidth.

We have covered the most frequently used measures of phase noise and have interrelated them. Before we take a look at the generation of phase noise in amplifiers and oscillators, let us take a look at the noise-conversion nomograph in Table 3. The example given there is self-explanatory.

As most of these relationships, for reasons of convenience, are expressed in decibels rather than absolute values, the following formulas are commonly used:

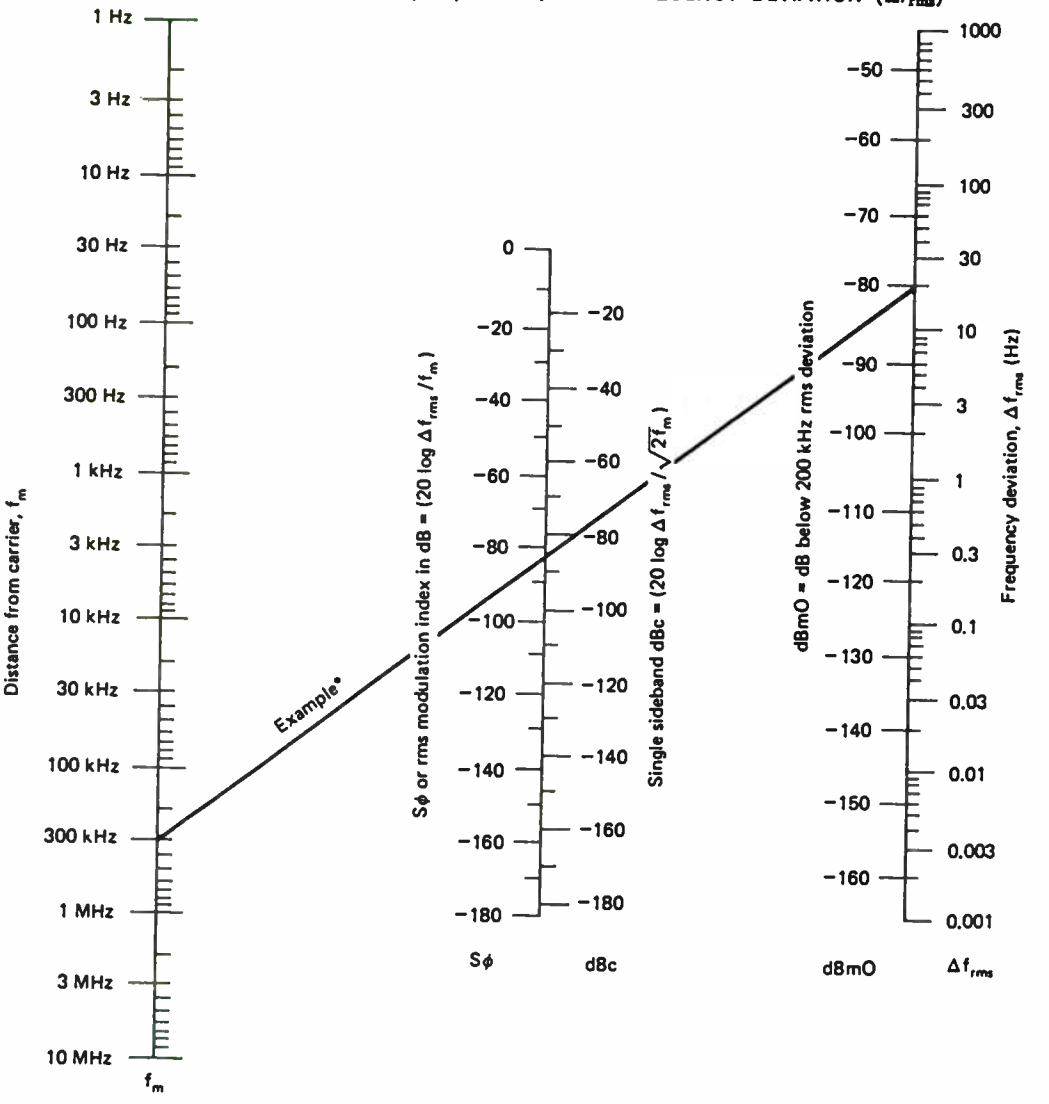
$$\mathcal{L}(f_m) = 10 \log_{10} \left(\frac{\Delta f_{peak}}{2 f_m}\right)^2 \qquad (15)$$

$$\mathcal{L}(f_m) = 10 \log_{10} \left(\frac{\Delta f_{rms}}{\sqrt{2}\, f_m}\right)^2 \qquad (16)$$

$$\mathcal{L}(f_m) = 20 \log_{10} \frac{\Delta f_{rms}}{\sqrt{2}\, f_m} \qquad (17)$$

$$\mathcal{L}(f_m) = 20 \log_{10} \frac{\theta_d}{2} \qquad (18)$$

TABLE 3 NOISE-CONVERSION NOMOGRAPH: RELATIONSHIP AMONG MODULATING FREQUENCY (f_m), POWER SPECTRAL DENSITY OF PHASE (S_ϕ), MODULATION INDEX, SIDEBAND TO CARRIER RATIO (dBc), dBmO, AND FREQUENCY DEVIATION (Δf_{rms})[a]



[a]Use consistent measurement bandwidth. Example: 20-Hz deviation in a 1-kHz band at 300 kHz from carrier = single-sideband dBc of −87 dB in a 1-kHz band.

5 CALCULATION OF OSCILLATOR NOISE

A. Linear Model

We will assume that the oscillator is composed of a linear amplifier with gain A and a high-Q resonant circuit, as illustrated in block diagram form in Figure 3. the gain of the resonant circuit has been normalized to unity at the resonant frequency f_o, the amplifier gain A must also be unity in order for the circuit to oscillate. Let S_θ represent the amplifier noise referred to the amplifier input. The white noise N per unit bandwidth at the amplifier input is given by

$$N = N_i + N_a = FkT \tag{19}$$

where F is the amplifier noise figure. Therefore, the ratio of noise power per unit bandwidth to signal power P_s is FkT/P_s, which is a component of S_θ. In addition, amplifiers generate an additional *flicker*, or $1/f$ phase noise, about the carrier frequency due to carrier density fluctuations in the base resistance. A plot of S_θ for frequencies greater than the carrier frequency f_o is contained in Figure 3. For frequencies close to the carrier, S_θ has a $1/f$ spectrum. At high frequencies the spectrum is flat and equal to FkT/P_s. The frequency f below which the spectrum has a $1/f$ shape depends on the characteristic of the individual amplifiers. For the circuit of Figure 3 with positive feedback and $A = 1$, the closed-loop steady-state transfer function between the amplifier output and the amplifier input is given by

$$B(j\omega) = \frac{1}{1 - H(j\omega)} \tag{20}$$

where

$$H(j\omega) = \frac{1}{1 + jQ\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)} \tag{21}$$

Since $H(j\omega)$ is a high-Q filter and we are interested in describing the noise power distribution about the center frequency ω_o, $H(j\omega)$ can be replaced by its low-pass equivalent,

$$H_L(j\omega) = \frac{1}{1 + j\omega/\omega_L} \tag{22}$$

where

$$\omega_L = \frac{\omega_o}{2Q} \tag{23}$$

is the equivalent bandwidth. Since the noise spectral density $S_o(\omega)$ at the output of a filter with a transfer function $G(j\omega)$, in terms of the spectral density $S_i(\omega)$ of the input noise, is given by

$$S_o(\omega) = S_i(\omega)\,|G(\omega)|^2 \tag{24}$$

the equivalent phase noise of the closed-loop system

$$\begin{aligned} S_o &= S_\theta \frac{1}{|1 - H(\omega)|^2} \\ &= \frac{S_\theta}{\left|1 - \frac{1}{1 + j\omega/\omega_L}\right|\left|1 - \frac{1}{1 - j\omega/\omega_L}\right|} \\ &= \frac{S_\theta(1 + \omega^2/\omega_L^2)}{\omega^2/\omega_L^2} \\ &= S_\theta\left(1 + \frac{\omega_L^2}{\omega^2}\right) \end{aligned} \tag{25}$$

which can be written [using Eqs. (5), (19), and (23)]

$$S_\phi(\omega) = \frac{FkT}{P}\left(1 + \frac{\omega_o^2}{4Q^2\omega^2}\right) \qquad (26)$$

which is the expression proposed by Leeson for describing the noise at the output of an oscillator.

As mentioned at the beginning of this chapter, there are various types of noise, and so far Leeson's model does not contain an allowance for the flicker noise. We will, therefore, modify our equation into

$$\mathcal{L}(f_m) = \frac{1}{2}\left[1 + \frac{1}{\omega_m^2}\left(\frac{\omega_o}{2Q_{\text{load}}}\right)^2\right]\frac{FkT}{P_{\text{sav}}}\left(1 + \frac{f_c}{f_m}\right) \qquad (27)$$

This equation describes the phase noise at the output of the amplifier of the oscillator.

Earlier figures showed the difference depending on the Q of the oscillator. In accordance with Ref. 18, we will expand Leeson's equation further for an actual oscillator to show how the noise performance can be optimized. Q loaded can be expressed as

$$Q_{\text{load}} = \frac{\omega_o W_e}{P_{\text{diss, total}}} = \frac{\omega_o W_e}{P_{\text{in}} + P_{\text{res}} + P_{\text{sig}}} = \frac{\text{reactive power}}{\text{total dissipated power}} \qquad (28)$$

where W_e is the reactive energy stored in L and C,

$$W_e = \tfrac{1}{2}CV^2 \qquad P_{\text{res}} = \frac{\omega_o W_e}{Q_{\text{unl}}}$$

$$\mathcal{L}(f_m) = \frac{1}{2}\left[1 + \frac{\omega_o^2}{4\omega_m^2}\left(\frac{P_{\text{in}}}{\omega_o W_e} + \frac{1}{Q_{\text{unl}}} + \frac{P_{\text{sig}}}{\omega_o W_e}\right)^2\right]\left(1 + \frac{\omega_c}{\omega_m}\right)\frac{FkT_o}{P_{\text{sav}}} \qquad (29)$$

input power over reactive power

resonator Q

signal power over reactive power

flicker effect

phase perturbation

This equation is extremely significant because it contains most of the causes of phase noise in oscillators. To minimize the phase noise, the following design rules apply:

1. Maximize the unloaded Q.
2. Maximize the reactive energy by means of a high RF voltage across the resonator and obtain a low LC ratio. The limits are set by breakdown voltages of the active devices and the tuning diodes and the forward-bias condition of the tuning diodes.
3. Avoid saturation at all cost, and try to either have limiting or AGC without degradation of Q. Isolate the tuned circuit from the limiter or AGC circuit. Use anti-parallel tuning diode connections to avoid forward bias.
4. Choose an active device with the lowest noise figure. Currently, the best bipolar transistor is the Siemens BFQ81 and the lowest noise field-effect transistors are U310 and 2N5397 up to 500 MHz. The noise figure of interest is the noise figure obtained at the actual impedance at which the device is operated. Using field-effect transistors rather than bipolar transistors, it is preferable to deal with the equivalent noise voltage and noise currents rather than with the noise figure, since they are independent of source impedance. The noise figure improves as the ratio between source impedance and equivalent noise resistance increases. In addition, in a tuning circuit, the source impedance changes drastically as a function of the offset frequency, and this effect has to be considered.

5. Phase perturbation can be minimized by using high-impedance devices such as field-effect transistors, where the signal-to-noise ratio of the signal voltage relative to the equivalent noise voltage can be made very high. This also indicates that in the case of a limiter, the limited voltage should be as high as possible.

6. Choose an active device with low flicker noise. The effect of flicker noise can be reduced by RF feedback. An unbypassed emitter resistor of 10 to 30 Ω in a bipolar circuit can improve the flicker noise by as much as 40 dB. In a later example we will study such an oscillator.

The proper bias point of the active device is important and precautions should be taken to prevent modulation of the input and output dynamic capacitance of the active device, which will cause amplitude-to-phase conversion and therefore introduce noise.

7. The energy should be coupled loosely from the resonator rather than another portion of the active device so that the resonator limits the bandwidth. A crystal oscillator using this principle is described later.

Equation (29) assumes that the phase perturbation and the flicker effect are the limiting factors, as practical use of such oscillators requires that an isolation amplifier be used.

In the event that the energy is taken directly from the resonator and the oscillator power can be increased, the signal-to-noise ratio can be increased above the theoretical limit of − 174 dB, due to the low-pass filter effect of the tuned resonator. However, since this is mainly a theoretical assumption and does not represent the real world in a system, this noise performance cannot be obtained. In an oscillator stage, even a total noise floor of 170 dB is rarely achieved.

What other influences do we have that cause the noise performance to degrade?

So far, we have assumed that the Q of the tuned circuit is really determined only by the LC network and the loading effect of the transistor. In synthesizer applications, however, we find it necessary to add a tuning diode. The tuning diode has a substantially lower Q than that of a mica capacitor or even a ceramic capacitor. As a result of this, the noise sidebands change as a function of the additional loss. This is best expressed in the form of adjusting the value for the loaded Q in Eq. (27).

There seems to be no precise mathematical way of predetermining the noise influence of a tuning diode, but the following approximation seems to give proper results:

$$\frac{1}{Q_{T\,\mathrm{load}}} = \frac{1}{Q_{\mathrm{load}}} + \frac{1}{Q_{\mathrm{diode}}} \qquad (30)$$

The tuning diode is specified to have a cutoff frequency f_{max} which is determined from the loss resistor R_s and the value of the junction capacitance as a function of voltage (i.e., measured at 3 V). This means that the voltage determines the Q and, consequently, the noise bandwidth.

We will go into more detail in dealing with the mechanism and influence of tuning diodes in the oscillator section, where we will evaluate the various methods of building voltage tunable oscillators using tuning diodes and switching diodes. Here we limit ourselves to practical results.

The loading effect of the tuning diode is due to losses, and these losses can be described by a resistor parallel to the tuned circuit.

It is possible to define an equivalent noise R_{eq} that, inserted in Nyquist's equation

$$V_n = \sqrt{4KT_oR\,\Delta f} \tag{31}$$

where $KT_o = 4.2 \times 10^{-21}$ at about 300°K, R is the equivalent noise resistor, and Δf is the bandwidth, determines an open noise voltage across the tuning diode. Practical values of R equivalent for carefully selected tuning diodes are in the vicinity of 1000 Ω to 50 kΩ. If we now determine the noise voltage $V_n = \sqrt{4 \times 4.2 \times 10^{-21} \times 10{,}000}$, the resulting voltage value is $1.265 \times 10^{-8}\ \mathrm{V}\sqrt{\mathrm{Hz}}$.

This noise voltage generated from the tuning diode is now multiplied with the VCO gain, resulting in the rms frequency deviation

$$(\Delta f_{rms}) = K_o \times (1.265 \times 10^{-8}\ \mathrm{V}) \text{ in 1-Hz bandwidth} \tag{32}$$

In order to translate this into the equivalent peak phase deviation,

$$\theta_d = \frac{K_o\sqrt{2}}{f_m}(1.265 \times 10^{-8}\ \mathrm{rad}) \text{ in 1-Hz bandwidth}$$

or for a typical oscillator gain of 100 kHz/V,

$$\theta_d = \frac{0.00179}{f_m}\ \mathrm{rad} \text{ in 1-Hz bandwidth}$$

For $f_m = 25$ kHz (typical spacing for adjacent channel measurements for FM mobile radios), the $\theta_c = 7.17 \times 10^{-8}$. This can be converted now into the SSB signal-to-noise ratio

$$\begin{aligned} \mathcal{L}(f_m) &= 20 \log_{10} \frac{\theta_c}{2} \\ &= -149\ \mathrm{dB/Hz} \end{aligned} \tag{33}$$

This is the value typically achieved in the Rohde & Schwarz SMDU or with the Hewlett-Packard 8640 signal generator and considered state of the art for a free-running oscillator. It should be noted that both signal generators use a slightly different tuned circuit; the Rohde & Schwarz generator uses a helical resonator, whereas the Hewlett-Packard generator uses an electrically shortened quarter-wavelength cavity. Both generators are mechanically pretuned and the tuning diode with a gain of about 100 kHz/V is used for frequency-modulation purposes or for the AFC input. It is apparent that, because of the nonlinearity of the tuning diode, the gain is different for low dc voltages than for high dc voltages. The impact of this is that the noise varies within the tuning range.

If this oscillator had to be used for a frequency synthesizer, the 1-MHz tuning range would be insufficient; therefore, a way had to be found to segment the band into the necessary ranges. In VCOs, this is typically done with switching diodes that allow the proper frequency bands to be selected. These switching diodes insert in parallel or series, depending on the circuit, or additional inductors or capacitors, depending on the design.

In low-energy-consuming circuits, the VCO frequently is divided into a coarse-tuning section using tuning diodes and a fine-tuning section with a tuning diode. In the coarse-tuning range, this results in very high gains, such as 1 to 10 MHz/V, for the diodes, and therefore the noise contribution of those diodes is very high and can hardly be compensated by the loop. For low-noise applications, which automatically mean higher power consumption, it is unavoidable to use switching diodes.

Let us now examine some test results. If we go back to Eq. (27), Figure 4 shows the noise sideband performance as a function of Q, whereby the top curve with $Q_L = 100$ represents a somewhat poor oscillator and the lowest curve with $Q_L = 100{,}000$ probably represents a crystal oscillator where the unloaded Q of the crystal was in the vicinity of 3×10^6. Figure 5 shows the influence of flicker noise.

Corner frequencies of 10 Hz to 10 kHz have been selected, and it becomes apparent that around 1 kHz the influence is fairly dramatic, whereas the influence at 20 kHz off the carrier is not significant. Finally, Figure 6 shows the influence of the tuning diodes on a high-Q oscillator.

Curve A uses a lightly coupled tuning diode with a K_o of 10 kHz/V; the lower curve is the noise performance without any diode. As a result, the two curves are almost identical, which can be seen from the somewhat smeared form of the graph. Curve B shows the influence of a tuning diode at 100 kHz/V and represents a value of 143 dB/Hz from 155 dB/Hz, already some deterioration. Curve C shows the noise if the tuning diode results at a 1-MHz/V VCO gain, and the noise sideband at 25 kHz has now deteriorated to 123 dB/Hz. These curves speak for themselves.

It is of interest to compare various oscillators. Figure 7 shows the performance of a 10-MHz crystal oscillator a 40-MHz LC oscillator, the 8640 cavity tuned oscillator at 500 MHz, the 310- to 640-MHz switched reactance oscillator of the 8662 oscillator, and a 2- to 6-GHz YIG oscillator at 6 GHz.

The above outlined theory for the linear approach has clearly indicated that the key factors for success in building a low noise oscillator are:

1. High Q resonator, referring to the loaded Q.
2. Obtain the highest possible output from the oscillator while maintaining the smallest possible large signal noise figure of the transistor.
3. Minimize the flicker noise and/or AM to PM conversion.

Figure 8 shows the spectral phase noise of the Carrier to Noise Ratio versus Frequency Deviation from the Carrier for Low- and High Q Resonators.

It is necessary to look at this plot to understand that the breakpoint for the corner frequency of the flicker frequency can move around as the Q changes. Remember also that Q is a function of loading the resonator with the transistor and therefore the highest open loop gain should be used. Oscillators are frequently used in similar generators and are multiplied up to the actual desired output frequency. For microwave applications, frequencies between 2 - 10 GHz are often required. Figure 9 shows a phase noise comparison of YIG and varactor tuned oscillators normalized to a center frequency of 6 GHz. This represents state-of-the-art in tunable oscillators; of course, crystal oscillators, oscillators with ceramic resonators and dielectric resonators have much better performance.

B. Nonlinear Model

The two most important active devices in oscillators are either the bipolar transistor or a member of the FET family. Depending on the frequency range, FETs used for oscillators are either "N" junction FETs, MOS devices or GaAs FETs. In the case of bipolar transistors, the nonlinear model of choice for nonlinear analysis is the Gummel-Poon bipolar transistor model, typically in a modified version.

From the FET family, several nonlinear models are available. In the case of the GaAs FET, popular models are Curtice-Edenberg, the Raytheon-Stutz , TOM , and Materka models. For MOS-devices we choose a MOS-level 3 Spice type model. These models are typically found in nonlinear circuit simulators like Compact's Microwave Harmonica. These active devices have a variety of nonlinear elements such as diodes, voltage- and/or current-dependent capacitance which are the major form of nonlinearities. The device change and noise figure as a function of bias and therefore the noise figure at each bias point is different. At high current levels, the noise, of course, will increase significantly. This requires the generation of a bias-dependent noise model which then is available for applications such as mixers and oscillators. A detailed introduction into this theory was presented in my paper [4].

6 GENERAL CONCEPT OF NOISE CONTRIBUTION

In the evaluation of a noisy two-port, it is important to know the amount of noise added to a single passing through a network.

$$\frac{S_{in}}{N_{in}} \rightarrow \text{Network} \rightarrow \frac{S_{out}}{N_{out}} \tag{34}$$

An important parameter for expressing this characteristic is the noise factor (or noise figure).

$$\text{Noise Factor} = F = \frac{S_{in} / N_{in}}{S_{out} / N_{out}}$$

$$\text{Noise Figure} = NF = 10 \log (F) \tag{35}$$

The sources of the internal noise in a general circuit are:

- Noise from Linear Elements

- Thermal noise related to the admittance of the elements.

Figure 10 shows a noiseless circuit with noise sources at the input and output.

$$C_n(\omega) = \frac{1}{\pi} K_B T \delta\, \omega\, [Y(\omega) + Y^*(\omega)] \tag{36}$$

A noise network can be treated as a noiseless network with equivalent noise current source at each external port.

The correlation of the noise current sources of a linear network is related to the Y matrix of this network.

The intrinsic noise sources of an active device (MESFET, BJT, ...) can be separated into a noiseless FET with noise sources at the input and the output as shown in Figure 11.

The intrinsic noise model can be expressed by the four measured parameters:

F_{min} - Minimum noise figure
R_n - Equivalent normalized noise resistance = $r_n/50$
M_{Go} - Magnitude of the optimal noise reflection coefficient
P_{Go} - Phase of the optimal noise reflection coefficient.

From these four parameters, the Van der Ziel noise model of the GaAs FET as an example can be derived as:

$$C_n(\omega) = \frac{2}{\pi} K_B T \delta\omega \begin{bmatrix} \frac{\omega^2 C_{gs}^2}{g_m} R & -j\omega C_{gs}\sqrt{PR}\, C \\ j\omega C_{gs}\sqrt{PR}\, C & g_m P \end{bmatrix} \tag{37}$$

This conversion for all active devices like FETs and bipolar transistors has been implemented in linear simulators like Compact's Super-Compact and Microwave Harmonica.

In addition, we have to add the flicker noise contribution of an active device (1/f Noise).

Figure 12 shows the flicker noise as a function of frequency.

Large Signal Condition of the Active Device:

We now look at the noise model of an active device when pumped by an LO. The noise sources and equivalent circuit model parameters are modulated by the LO.

Figure 13 shows the variation of some parameters as a function of the LO power.

The noise correlation matrix of the device is now modulated by the LO. This means the noise correlation component and nonlinear parameters such as:

$$R, P, C. g_m, C_{Gs}, \ldots = F(V_{Gs}, V_{ds}) \quad (38)$$

In addition for FETs as an example, the flicker noise is modulated by the drain current using the following equation:

$$\langle |I_f|^2 \rangle = 2K_B T \delta\omega Q \frac{|I_D|^\beta}{f^\alpha} \quad (39)$$

For the bipolar-model we have to use a similar approach.

Calculation of the Phase Noise Spectrum of the Oscillator

For the calculation of the phase noise spectrum of the oscillator a numerical approach is considered to provide nonlinear analysis. It can be shown that the phase noise is composed of two parts.

a. The Near-Carrier noise consists of contributions from the perturbation of the oscillating frequency caused by the noise sources at each side- and frequency. This part is the major noise source at the near-carrier frequencies.

b. The Far-Carrier noise consists of contributions from each sideband noise source through sideband - to - sideband transfer functions. This part is similar to a mixer noise calculation and is the major noise source at the frequencies far away from the carrier.

Figure 14 shows that the oscillator noise consists of the near- and far-carrier noise.

THE NOISE FIGURE OF THE MIXING CIRCUIT

In order to calculate the noise figure we assume that the pumped active device acts like a mixer circuit; we need to calculate the total internal noise of the circuit at the IF frequency.

Noise Analysis Step 1

By using a nonlinear simulator, we perform the harmonic balance analysis to determine the steady-state of the mixer. Figure 15 shows the mixing arrangement.

The harmonic balance calculation of the nonlinear simulator determines the Fourier coefficients of voltages and currents of the circuit. Any receiver configuration (e.g. LNA's, IF, AMP, etc.) may be considered.

Noise Analysis Step 2

We have to calculate the transfer functions of the sideband signals to the IF band signal. Figure 16 shows a summary of noise sources mixed to the IF. The noise at each sideband frequency contributes to the noise at the IF through frequency conversion. Figure 17 shows a summary of the IF noise contributions in a general nonlinear mixer circuit: Please note the large number of contributing elements which make up the total noise at the output. The calculation of dN is performed by equation (42) where the intermediate steps are given in [5].(See [6-17].)

$$\left\langle |\delta\Phi|^2(f_d)\right\rangle = \frac{\left\langle |V_l(f_d)|^2\right\rangle + \left\langle |V_u(f_d)|^2\right\rangle - 2\,\mathrm{Re}\left\{\left\langle V_l^*(f_d)V_u^*(f_d)\right\rangle \exp(2j\Phi_0)\right\}}{|V_0|^2} \tag{40}$$

$$\left\langle |\delta A|^2(f_d)\right\rangle = 2\frac{\left\langle |V_l(f_d)|^2\right\rangle + \left\langle |V_u(f_d)|^2\right\rangle + 2\,\mathrm{Re}\left\{\left\langle V_l^*(f_d)V_u^*(f_d)\right\rangle \exp(2j\Phi_0)\right\}}{|V_0|^2} \tag{41}$$

$$\begin{aligned} dN(\omega_{IF}) &= R_{IF}\sum_p T_{0p}C_L(\omega_{IF}+p\omega_0)T_{0p}^* \\ &+R_{IF}\sum_{p,q} T_{0p}\left[\sum_s H_{p-s}C_{dc}(\omega_{IF}+s\omega_0)H_{s-q}\right]T_{0q}^* \\ &+R_{IF}\sum_{p,q} Y_p^s \begin{bmatrix} \left\langle |V_u(\omega_{IF})|^2\right\rangle & \left\langle V_u(\omega_{IF})V_l^*(\omega_{IF})\right\rangle \\ \left\langle V_u^*(\omega_{IF})V_l(\omega_{IF})\right\rangle & \left\langle |V_l(\omega_{IF})|^2\right\rangle \end{bmatrix} Y_q^{s*} \end{aligned} \tag{42}$$

In (42), T0x are the sideband-to-IF conversion matrices, Hx are the spectral modulation components of the device, the p,q,r, and s are sideband spectral indecies, R_{IF} is the IF load, Y is a conversion admittance matrix between the LO noisy source and the IF load at the IF frequency, and w_{IF} is a small frequency deviation in the neighborhood of the baseband frequency. The first term represents the noise contribution of the linear network, the second term is the noise contribution from the modulated nonlinear devices, and the third term is the noise contribution of the noisy LO.

Calculation of the Total Carrier Phase Noise Spectrum

Under the assumption that the noise signals are small compared to the oscillator signal, the noise analysis is carrier out as a perturbative analysis. The manner in which we determine the contributions is as follows:

a. Far-carrier noise analysis (see mixer mode):

$$J_{BB}\delta X_B = -N_B(\omega) \tag{43}$$

b. Near-carrier noise analysis:

$$J_{HH}\delta X_H = -N_H(\omega) \tag{44}$$

The near-carrier noise is the noise-inducted jitter of the oscillatory steady state. The $\delta\,\omega$, one of the entries of δX_H, can be solved as

$$\delta\omega(\omega) = T_F\left[N_U(\omega) + N_L(\omega)\right] \tag{45}$$

and the resulting phase noise is

$$\begin{aligned} \langle|\delta\Phi_k(\omega)|^2\rangle = (k^2/\omega^2)\,[&T_F \langle N_U(\omega)N_U(\omega)^+\rangle T_F^+ \\ &+ T_F \langle N_L(\omega)N_L^+(\omega)\rangle T_F^+ \\ &+ 2\mathrm{Re}\,\{T_F\langle N_U(\omega)N_L^+(\omega)\rangle T_F^+\}\,] \end{aligned} \tag{46}$$

In the linear case, the assumed simplification did not consider the AM/PM conversion and the change of the loaded Q as a function of the oscillator condition. The approach shown here is the exact solution for the calculation of the oscillator phase noise. Further details about the mathematical approaches are founded in the literature cited.

7 Verification Examples for the Nonlinear Mathematical Approach of Calculating Phase Noise in Oscillators

Example 1 - a 10 MHz crystal oscillator

Figure 18 shows the abbreviated circuit of a 10 MHz crystal oscillator. It uses a high precision high *Q* made by companies such as Bleily. Oscillators like this are made by several companies and are intended for use as both frequency and low phase noise standards. In this particular case, the crystal oscillator has been considered to be a part of the HP 3048 phase noise measurement system.

Figure 19a shows the measured phase noise for this frequency standard by HP and Figure 19b shows the predicted phase noise using the mathematical approach as outline above.

Example 2 - 1 GHz Ceramic Resonator VCO

A number of companies have introduced resonators built from ceramic materials with an epsilon ranging from 20 - 80. The advantage of using this type of resonator is that they are a high Q element which can be tuned by adding a varactor diode.

Figure 20 shows a typical test circuit for use in a ceramic resonator. These resonators are available in the range of 500 MHz to 2 GHz. For higher frequencies, dielectric resonators are recommended. Figure 21 shows the measured phase noise of the oscillator shown in Figure 20. The noise pedestal above 100 kHz away from the carrier is due to the reference oscillator model HP 8662.

Figure 22 shows the predicted phase noise of the 1 GHz ceramic resonator VCO without a tuning diode and Figure 23 shows the predicted phase noise of the 1 GHz ceramic VCO with a tuning diode attached. Please note the good agreement between the measured and predicted phase noise.

Example 3 - Low Phase Noise FET Oscillator

A number of authors recommend the use of a clipping diode to prevent the gate-source junction of an FET from becoming conductive and thereby lowering the phase noise. In reality, it turns out that this has been a misconception. A popular VCO circuit as described in the American Radio Relay League's (ARRL) manual shown in Figure 24 has been analyzed with and without the diode. Claims also have been made that the diode was necessary to obtain long-term stability. Figure 25 shows the measured phase noise of an oscillator of this type and Figures 26 and 27 show the simulated phase noise of the type of oscillator as shown in Figure 24, with and without a clipping diode. Please note the degradation of the phase noise if the diode is used. David Newkirk of the ARRL found that by removing the diode it did not change or degrade the stability. Additionally, it did degrade the phase noise close-in. We have, however, developed a VCO which clips the negative peaks in the sense that it prevents the oscillator from shutting off. This VCO as shown in Figure 28 was incorporated in a scheme with a digital direct synthesizer. This synthesizer will be the subject of a later publication in QST.

The phase noise of the combined system was significantly improved. The phase noise of the oscillator shown in Figure 29 despite having only one VCO for the total range from 75 to 105 MHz as compared to a very recent design like the synthesizer in the TS-50 give still a 10dB bettter S/N ratio at 10 kHZ and further away, which is shown in Figure 30.

Previous authors have tried to build similar wideband oscillators with varying degrees of success. The VCO shown in Figure 31 violates several rules of designing a good VCO. First, resistor R2 of 68 kΩ, together with C2, provides

a time constant which gets close to the audio frequency range. This bears the possibility of building a super-regenerative receiver, which of course is counter-productive. Second, the diode from gate to ground working as a clipping diode also generates more noise. This was outlined above. Finally, the feedback selected between the two tuning diodes reduces the operating Q of the resonator to unreasonably small values. If this particular circuit is favored, then the tuning diode D2 should be made out of several (3 - 5) diodes in parallel. It is therefore not surprising that the measured phase noise show in Figure 32 is significantly below state-of-the-art.

Example 4 - Recommended Circuits for Higher Frequency Application

The following VCOs are ideal for low phase noise oscillators. Figure 33 shows a schematic which is a spin-off of Figure 28 and uses a 3 dB power divider at the output. Also, the loop filter for the synthesizer application is shown.

Figure 34 shows a high power low phase noise VCO system recommended for the frequency range from 400 to 700 MHz. Please note that the tuning element again uses several diodes in parallel.

Finally, Figure 35 shows a recommended VCO covering the frequency range from 700 MHz to 1 GHz. The rule of thumb is that FETs do not have enough gain for high Q operation in oscillators above 400 MHz and bipolar transistors are a better choice. Only at frequencies above 4 or 5 GHz should we consider GaAs FETs because of their higher flicker noise contribution.

8 CONCLUSION

In the past, the determination of phase noise required a great deal of guess work The analytical approach presented herein allows - for the first time - not only an accurate prediction of the phase noise but also allows the use of CAD tools to optimize the circuit. From a designer's point of view, the most critical assessments have been the issues of determining the proper loaded Q and the noise figure under large-signal conditions. This has always been subject to wild guesses. The nonlinear mathematical approach allows- again for the first time - a combination of all these things and provides the correct answer.

I am particularly grateful to my colleagues at Compact Software, Inc. and to Professor Vittorio Rizzoli, University of Bologna, who made this work possible.

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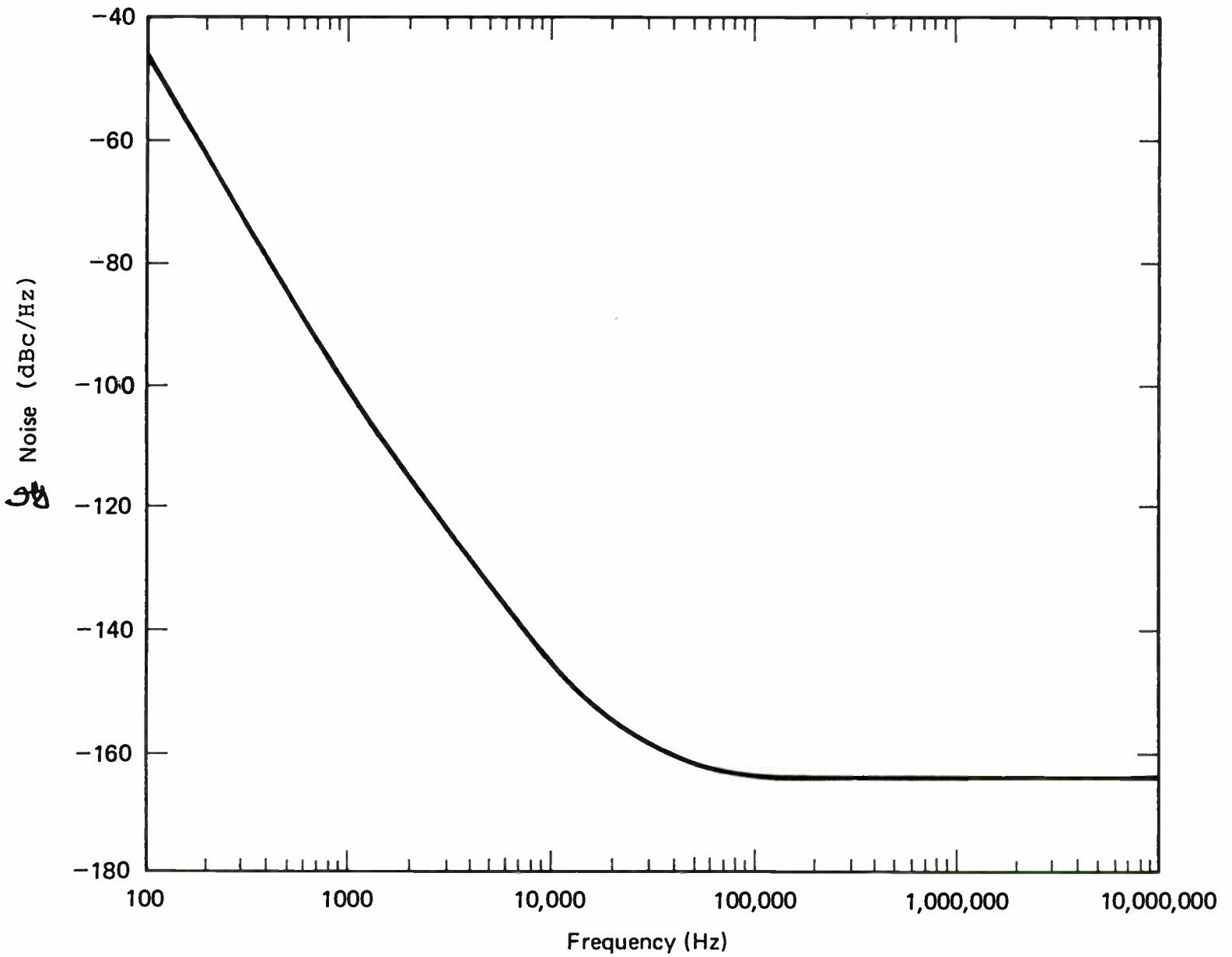


Figure 1 Typical noise sideband curve of a free-running oscillator, Rohde & Schwarz signal generator SMDU.

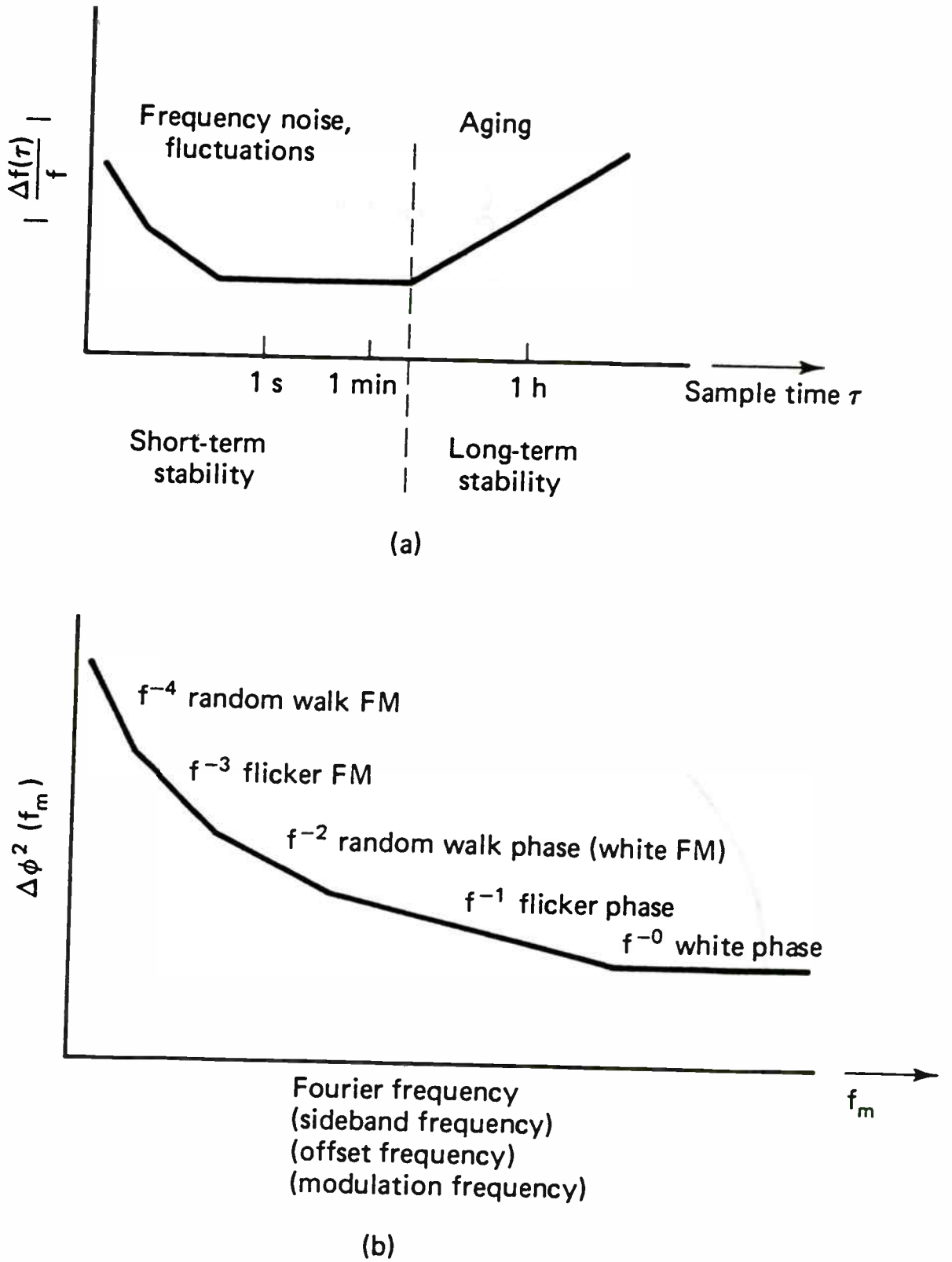


Figure 2 Characterization of noise sideband in the time and frequency domain and its contributions: (a) time domain; (b) frequency domain.

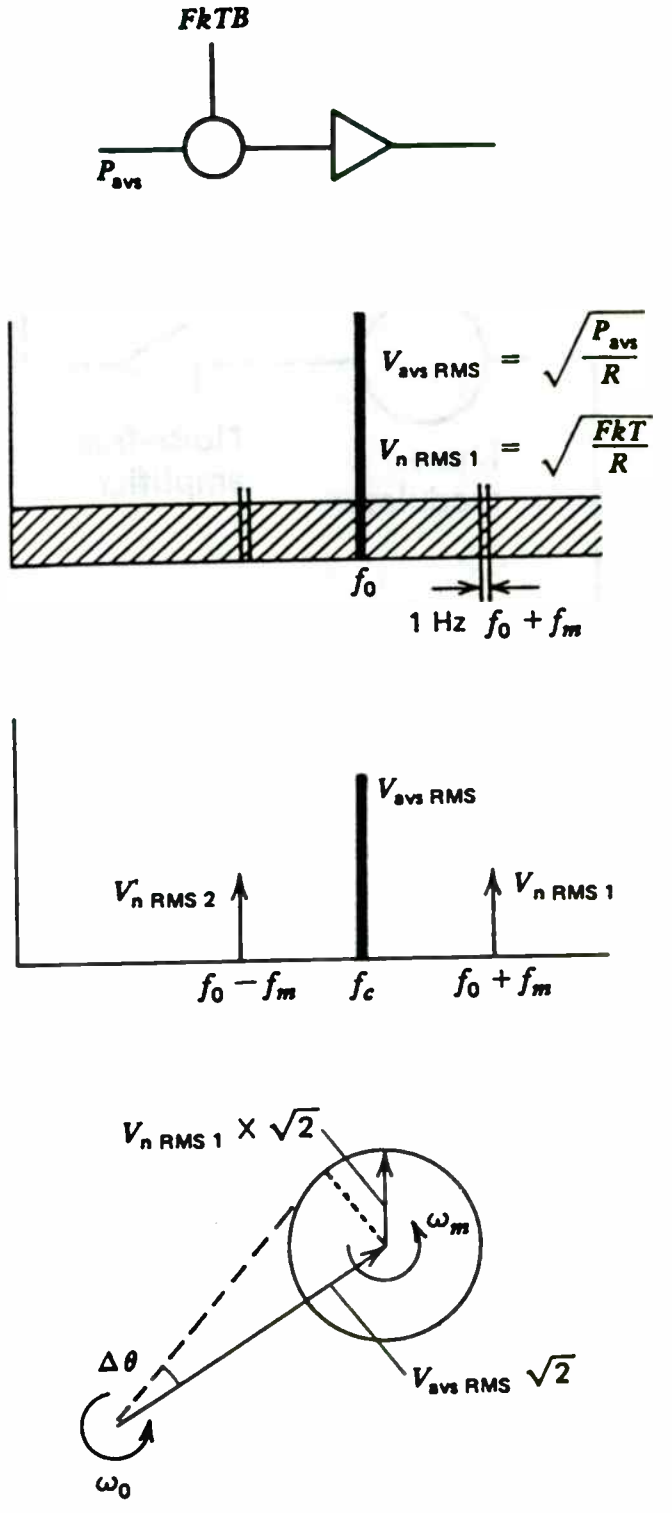


Figure 3a. **Modulation medium that adds phase noise to carrier**

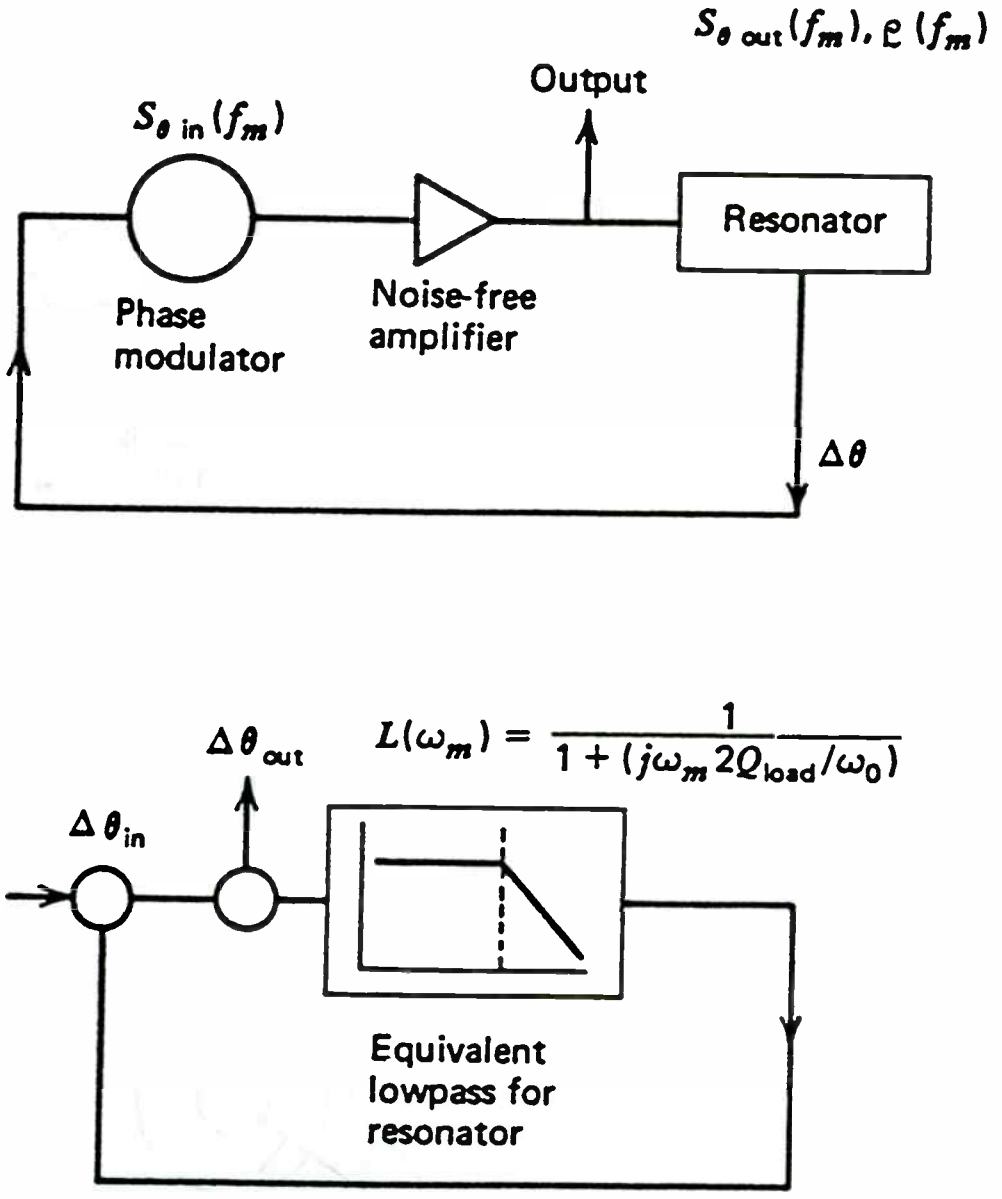


Figure 3b. **Block Diagram of the feedback model of an oscillator consisting of a phase modulator, noise-free amplifier and resonator**

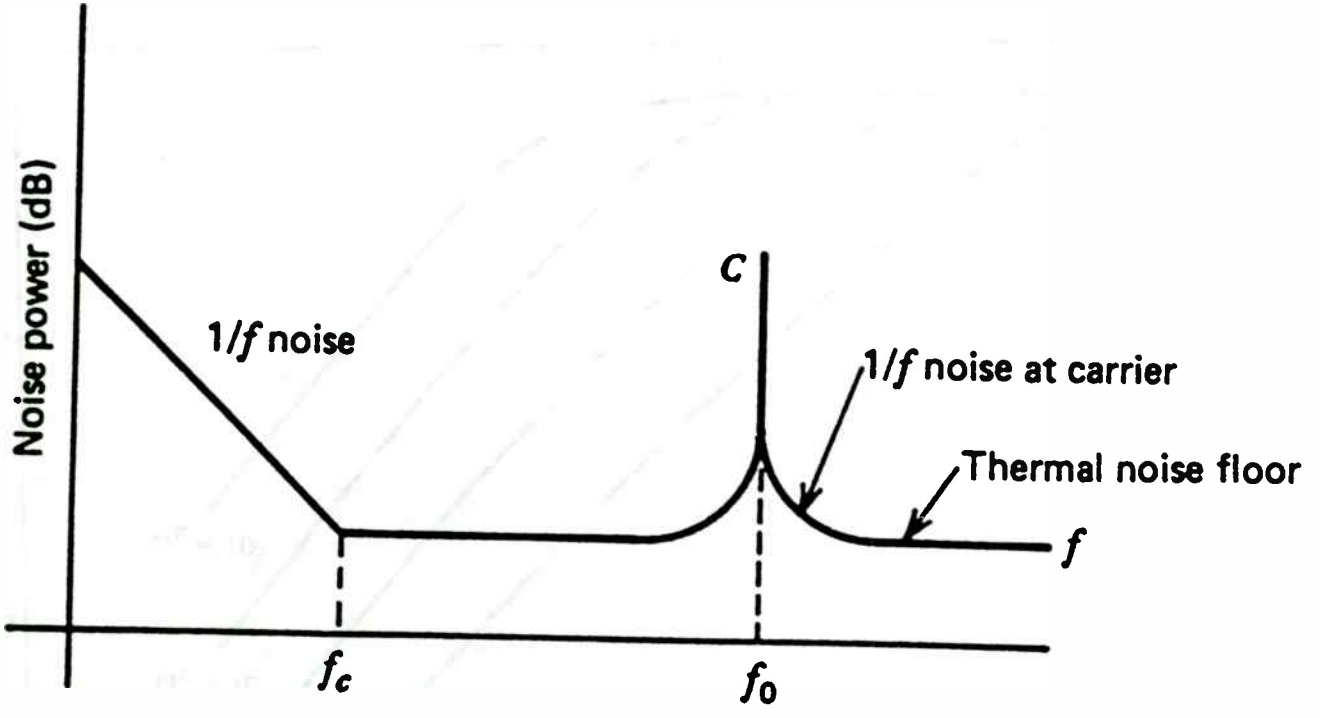


Figure 3c. Noise power versus frequency of a transistor amplifier with an input signal applied.

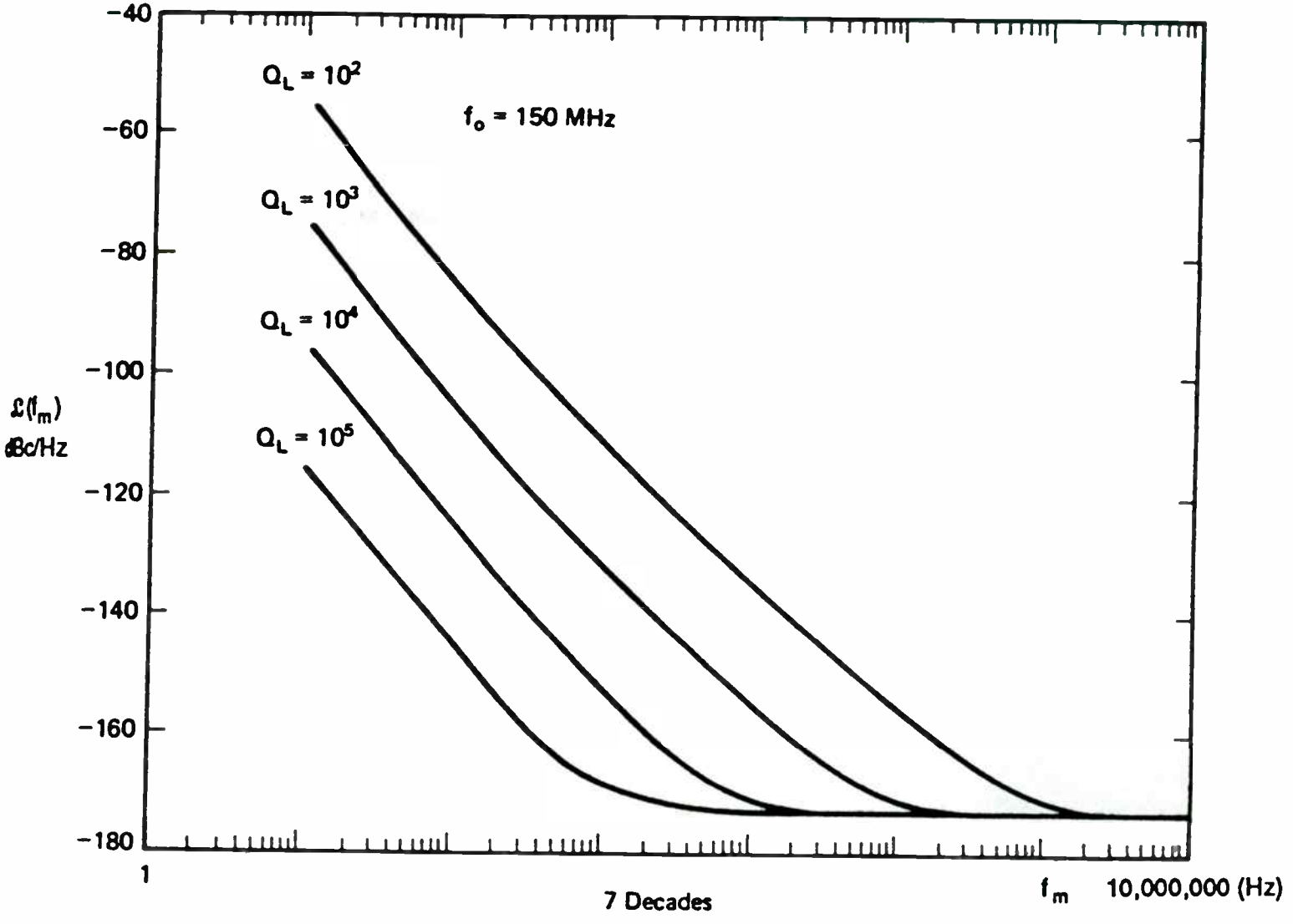


Figure 4 Noise sideband of an oscillator at 150 MHz as a function of the loaded Q of the resonator.

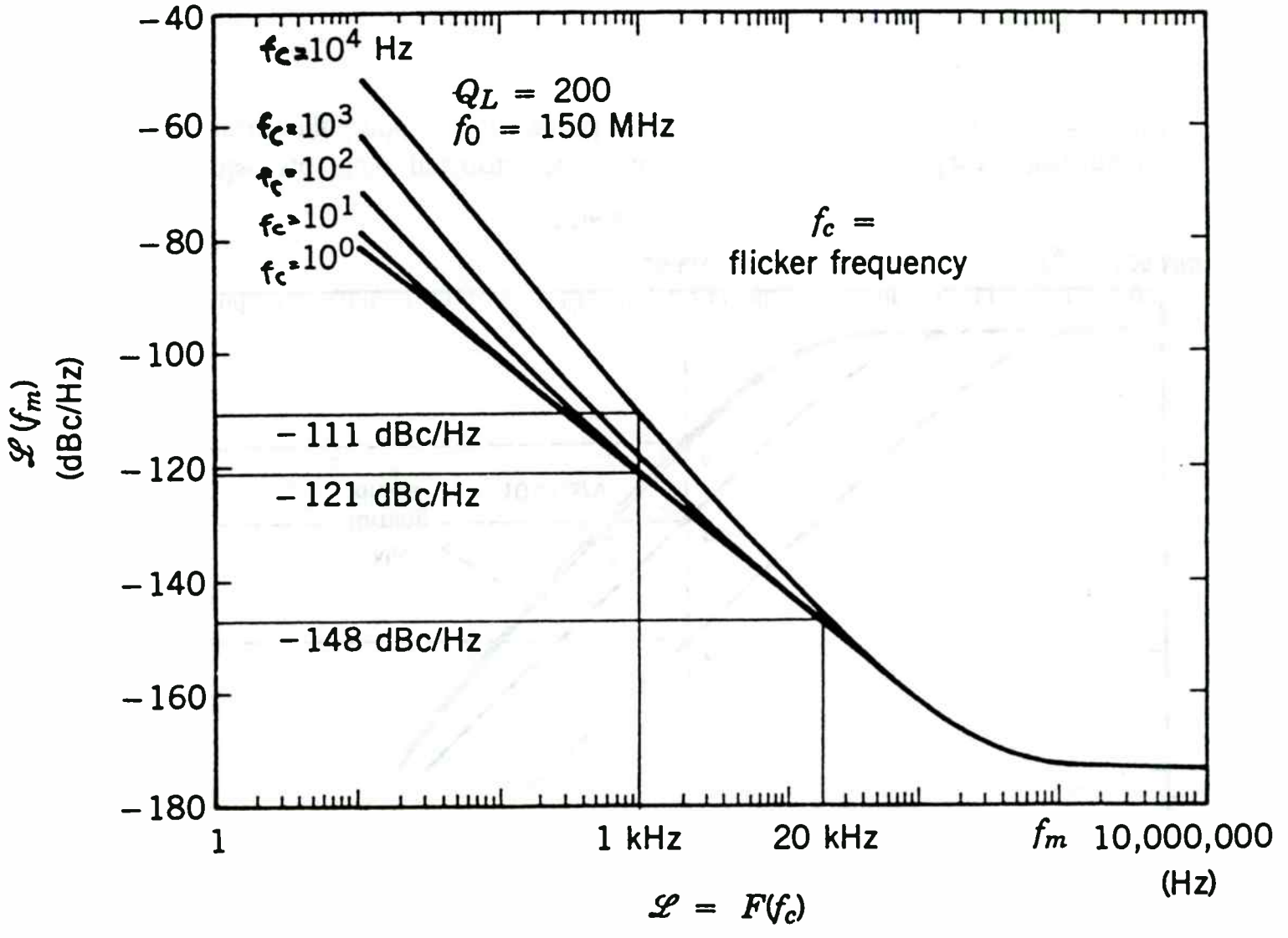


Figure 5 Noise sideband as a function of flicker frequency.

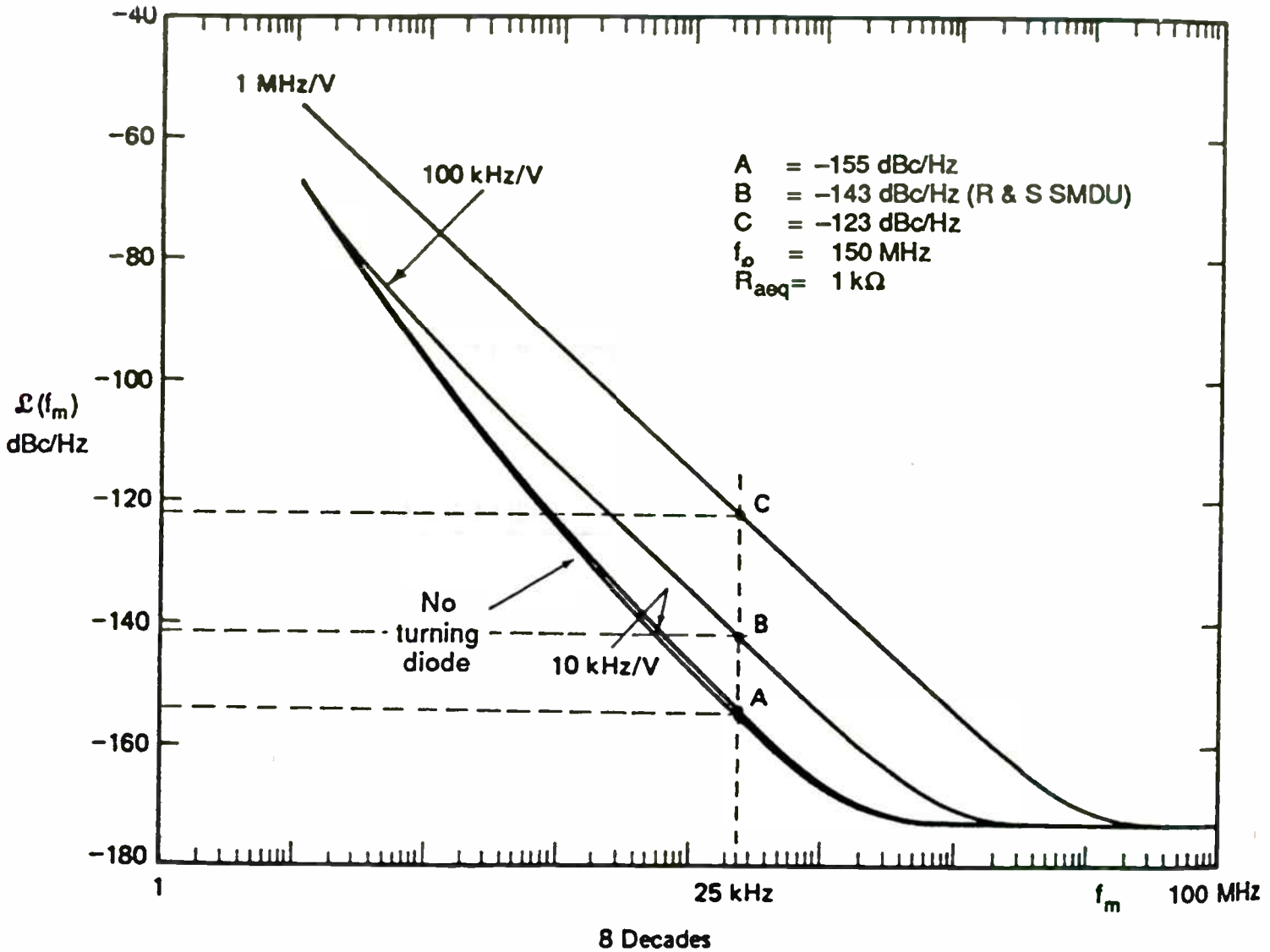


Figure 6 Noise sideband performance of an oscillator at 150 MHz, showing the influence of various tuning diodes and increased noise as a function of modulation sensitivity.

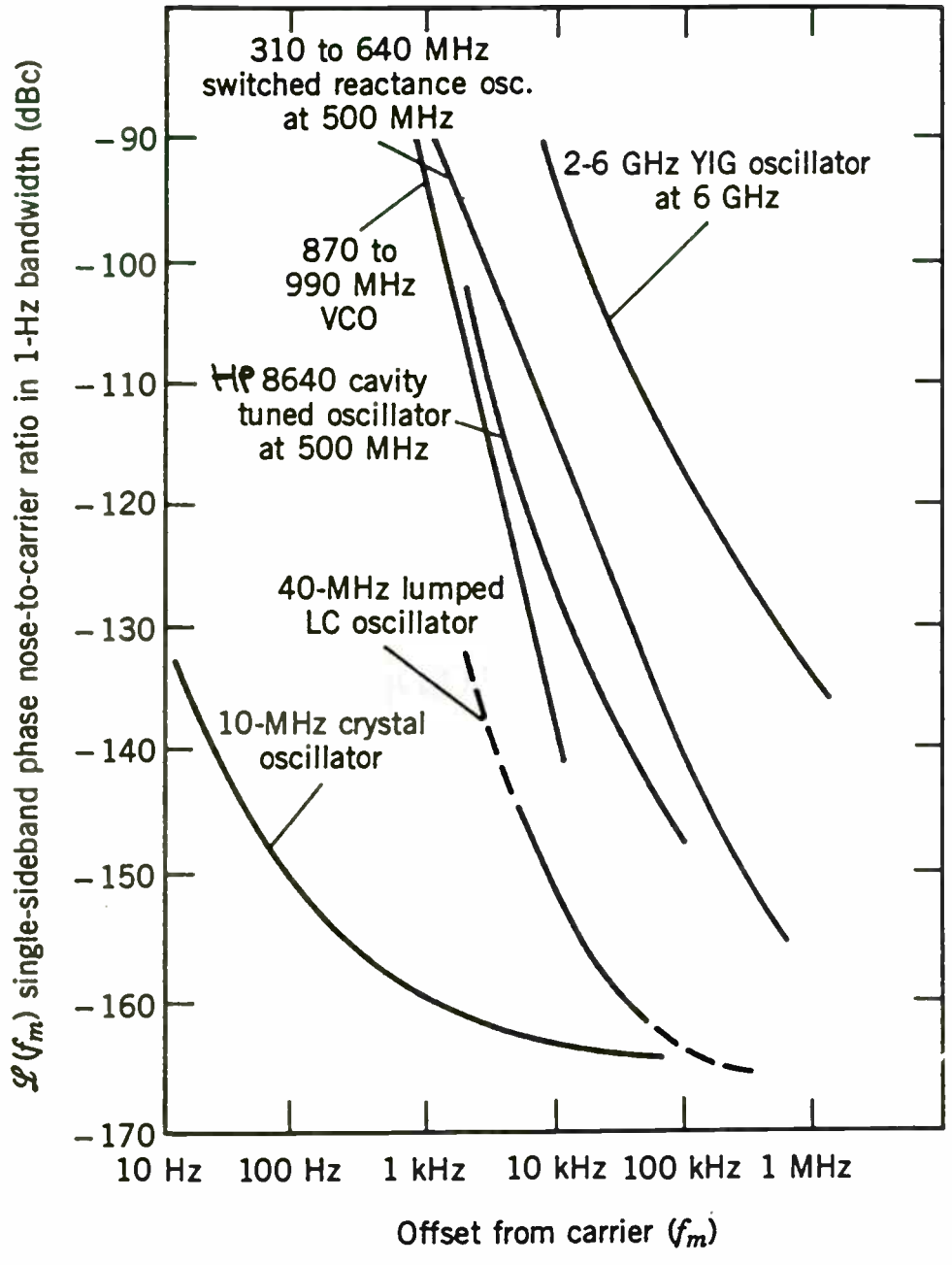


Figure 7 **Comparison of noise sideband performance of a crystal oscillator, *LC* oscillator, cavity-tuned oscillator, switched reactance oscillator, and YIG oscillator.**

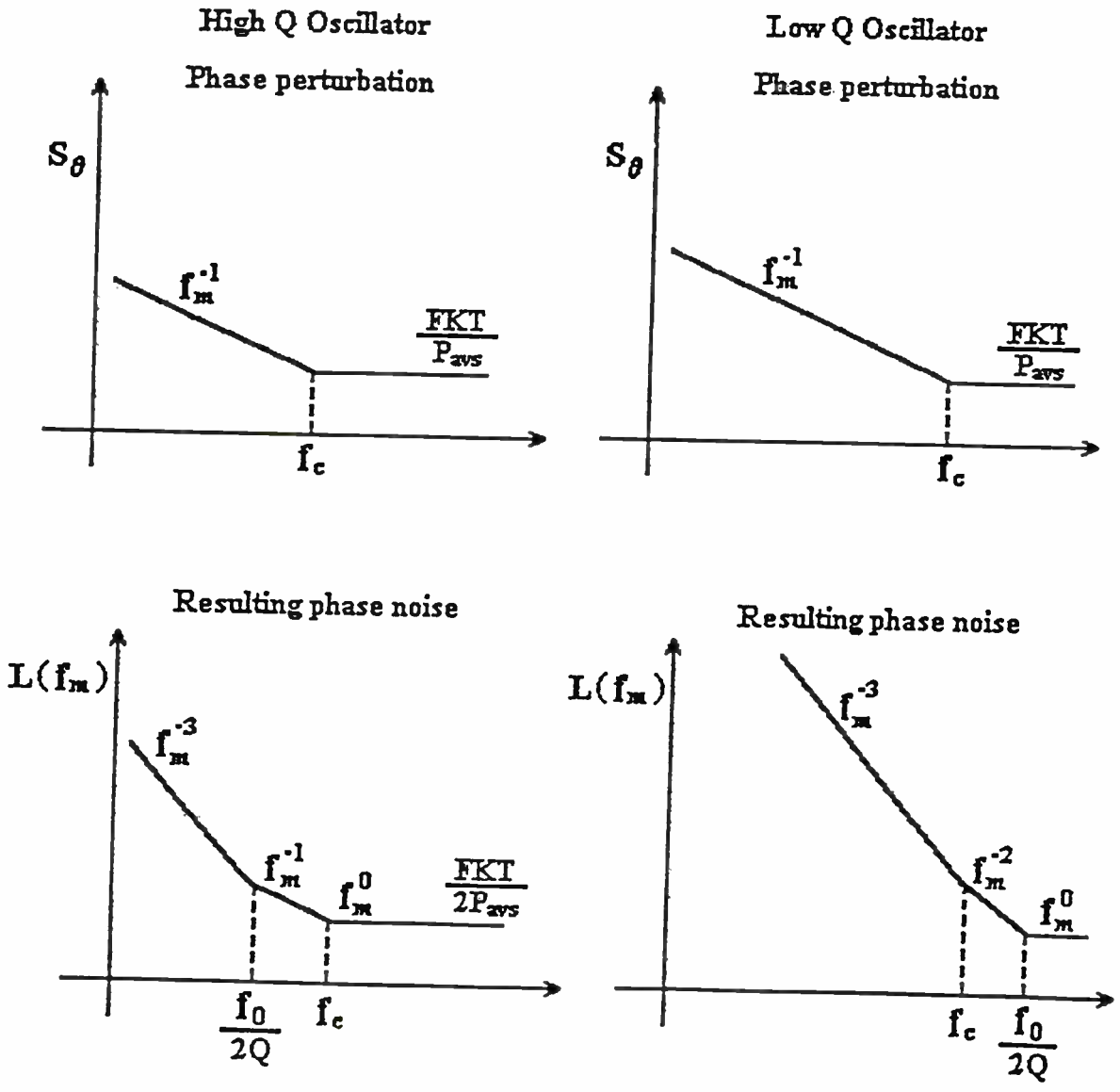


Figure 8 Shows the spectral phase noise of the Carrier to Noise Ratio versus Frequency Deviation from the Carrier for Low- and High-*Q* Resonators.

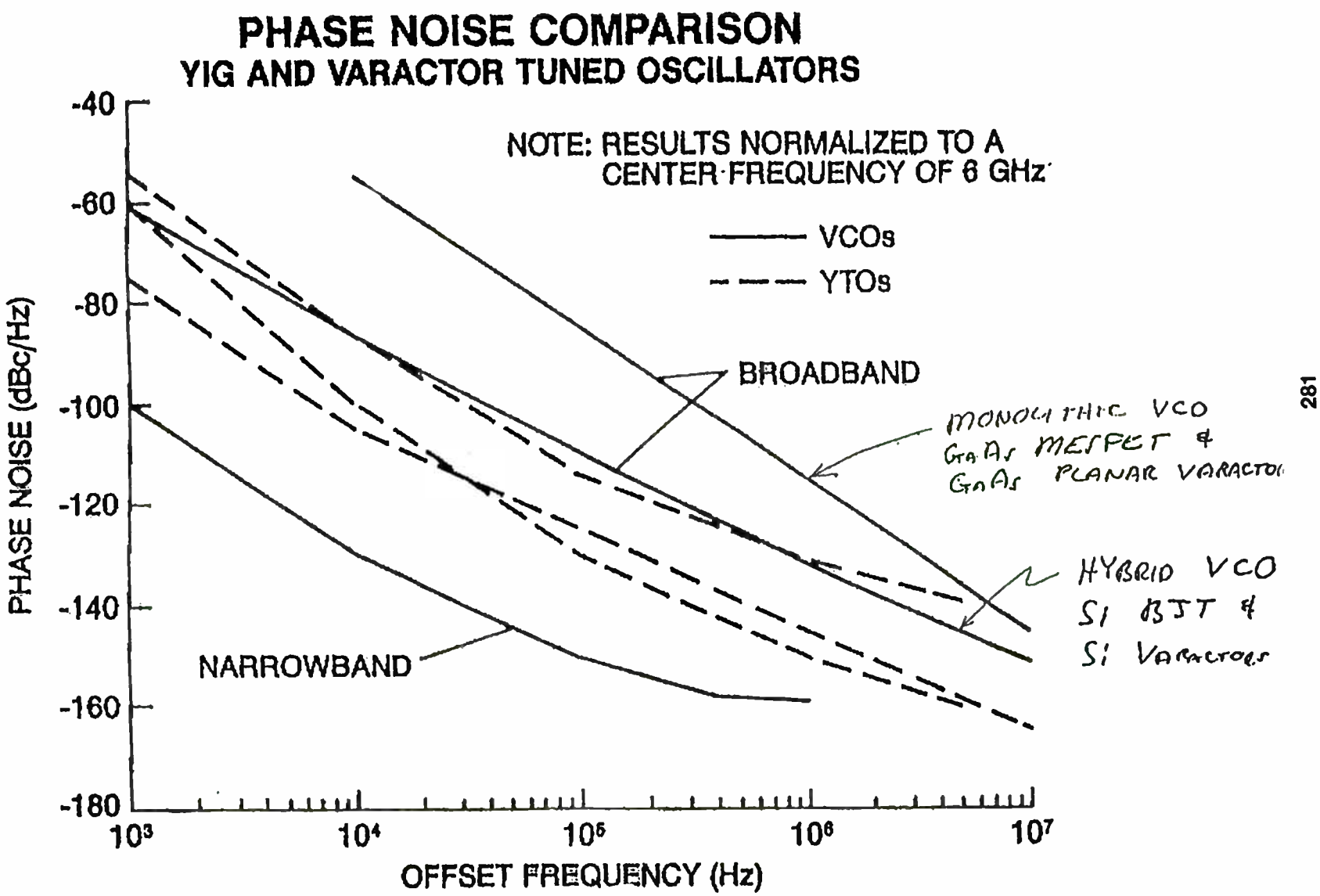


Figure 9 Shows a phase noise comparison of YIG and varactor tuned oscillators normalized to a center frequency of 6 GHz.

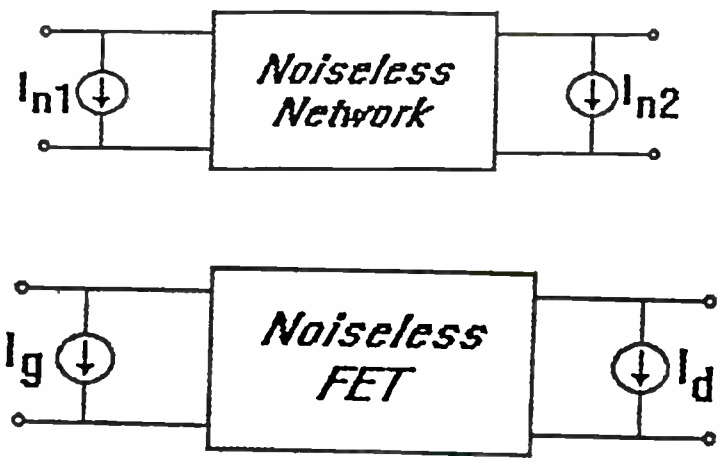


Fig. 10 Noiseless FET with noise sources at the input and the output

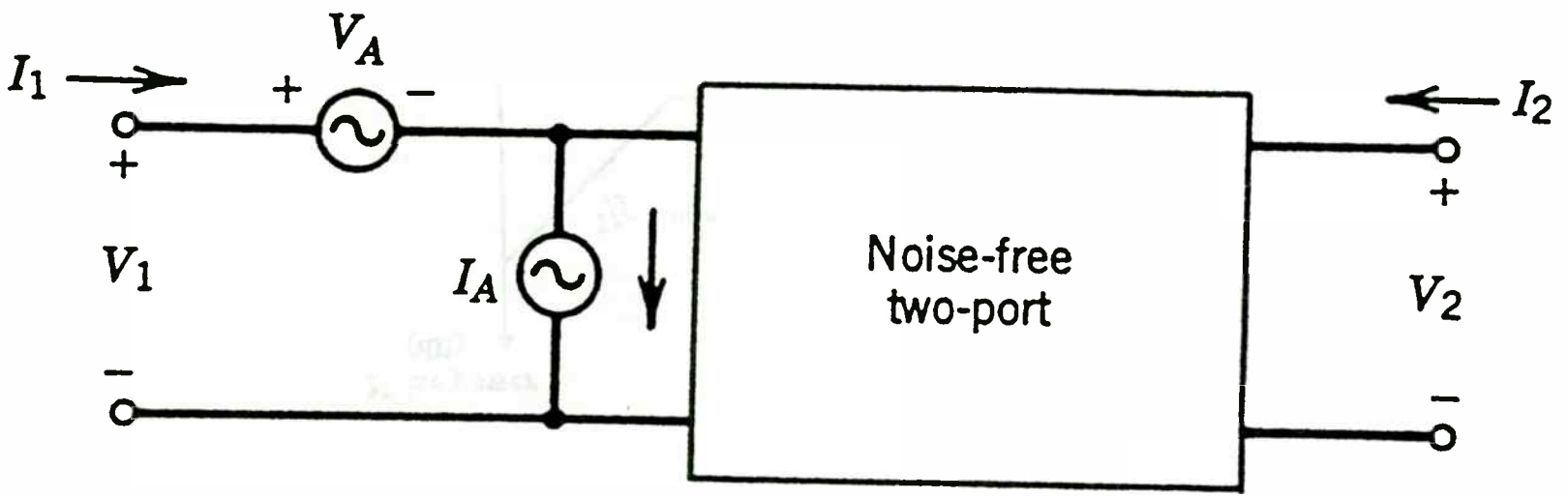


Figure 11 Shows the intrinsic noise sources of an active (MESFET, BJT, . . .) can be separated into a noiseless FET with noise sources at the input and output.

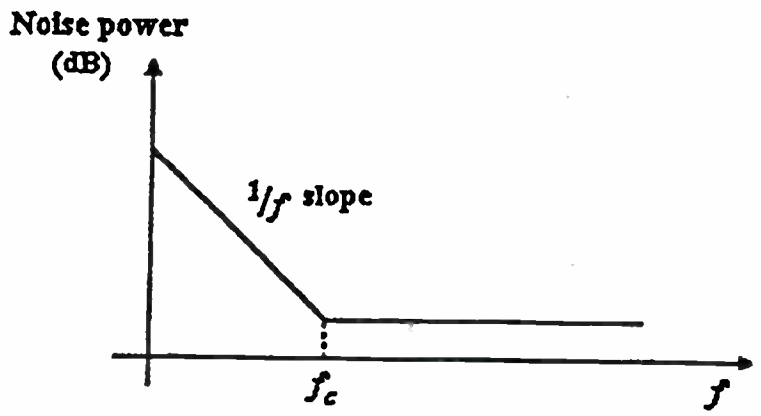


Fig.12 The major parameter used to describe the flicker noise is Fc - corner frequency.

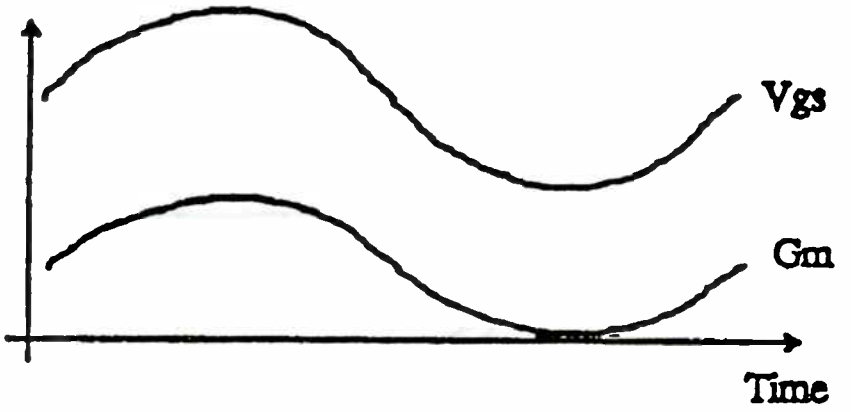


Fig. 13 The voltages and currents of devices are determined by harmonic balance calculations.

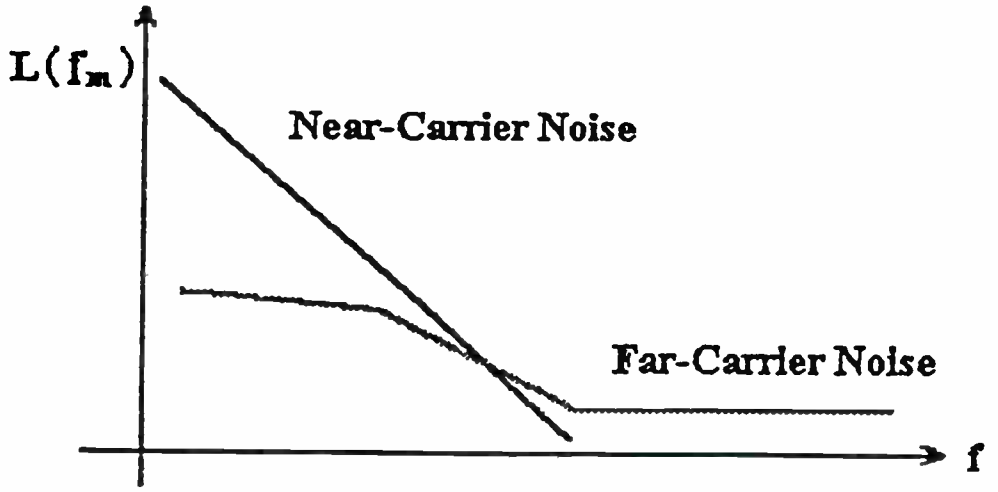


Figure 14 Shows that the oscillator noise consists of the near- and far- carrier noise.

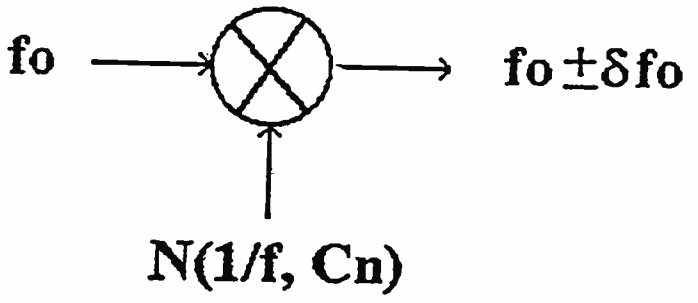


Figure 15 Shows the mixing arrangement within the oscillator whereby the carrier frequency (f_o), assumed noiseless, gets modulated with the various noise sources as outlined.

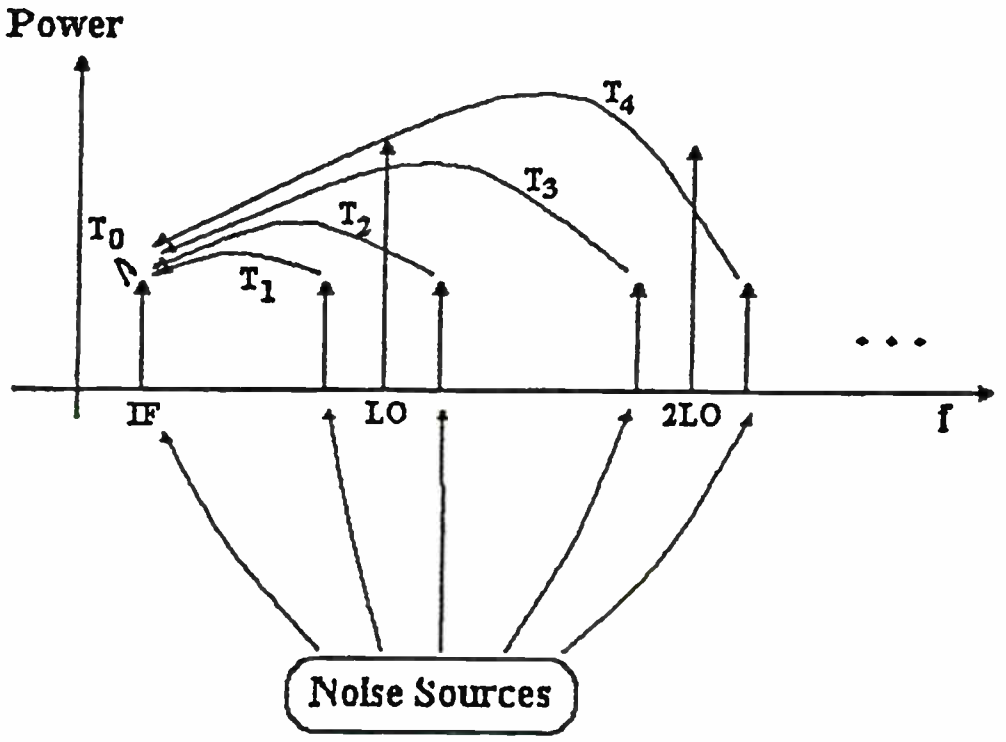


Fig. 16 Summary of noise sources mixed to the IF.

The noise at each sideband frequency contributes to the noise at the IF through frequency conversion.

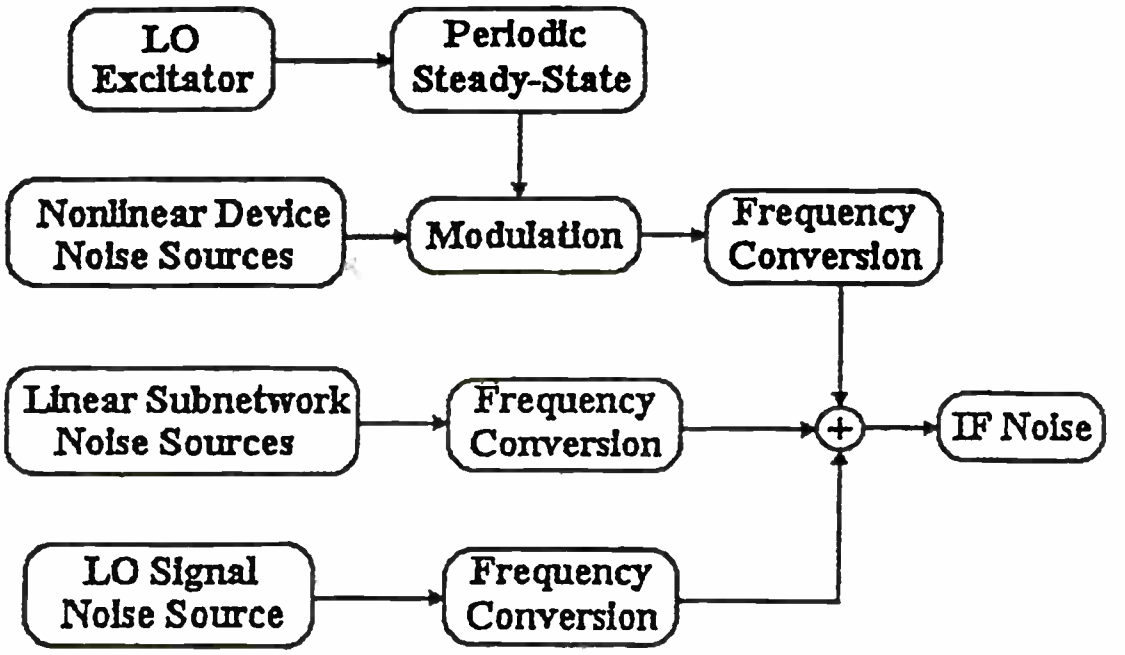


Fig. 17 Summary of IF noise contribution

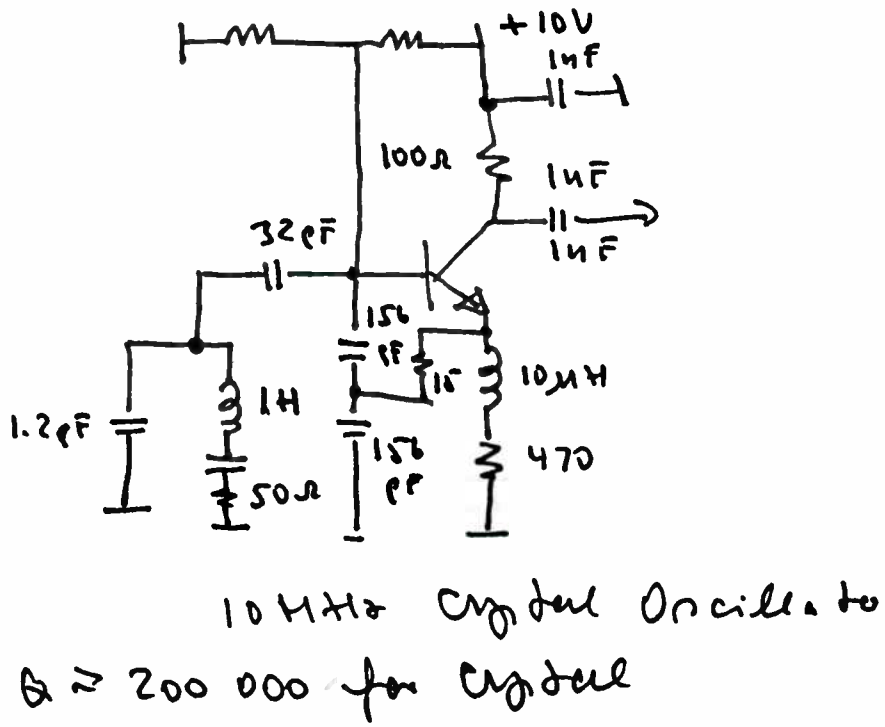


Figure 18 Shows the abbreviated circuit of a 10 MHz crystal oscillator.

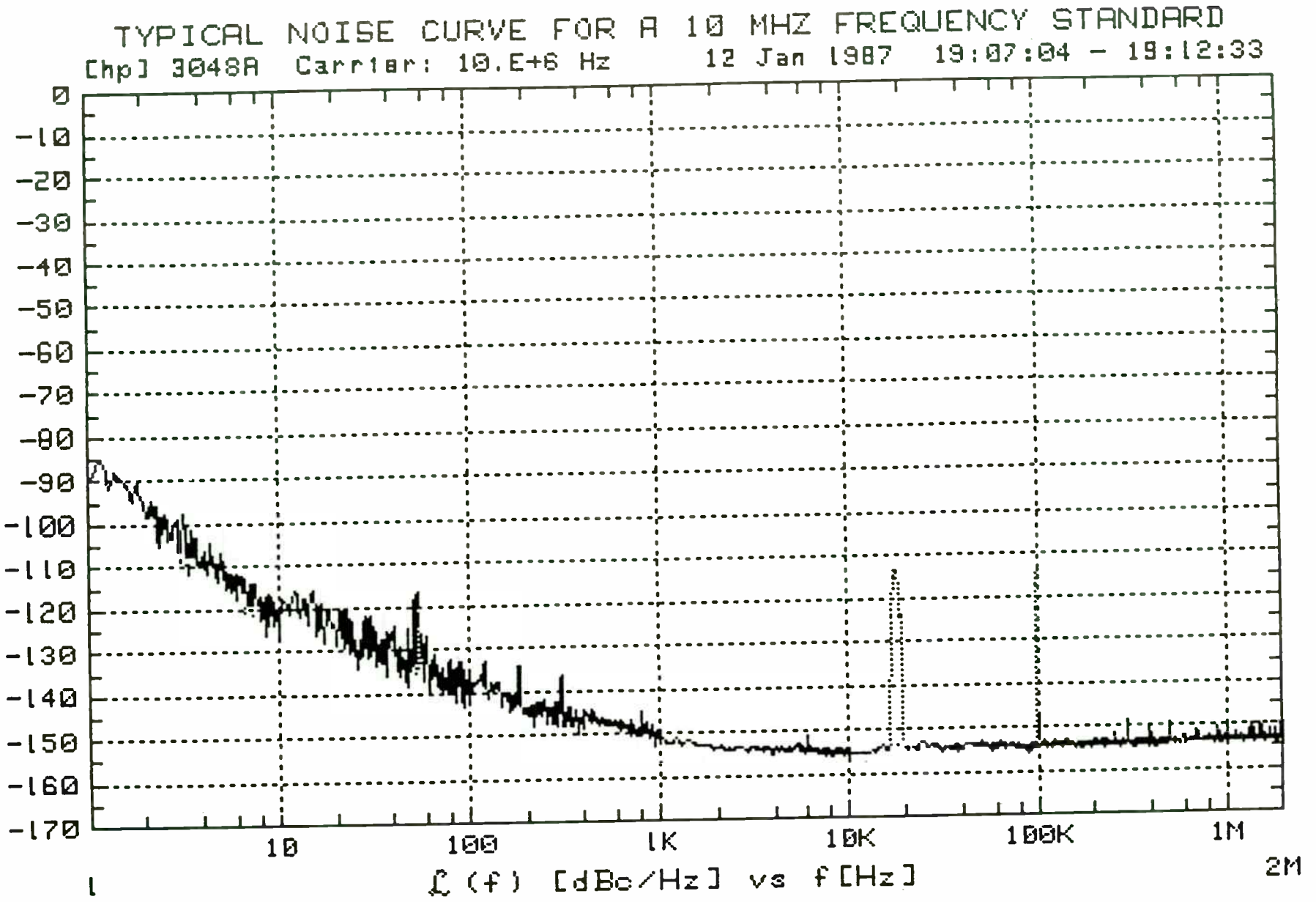


Figure 19a Shows the measured phase noise for this frequency standard by HP

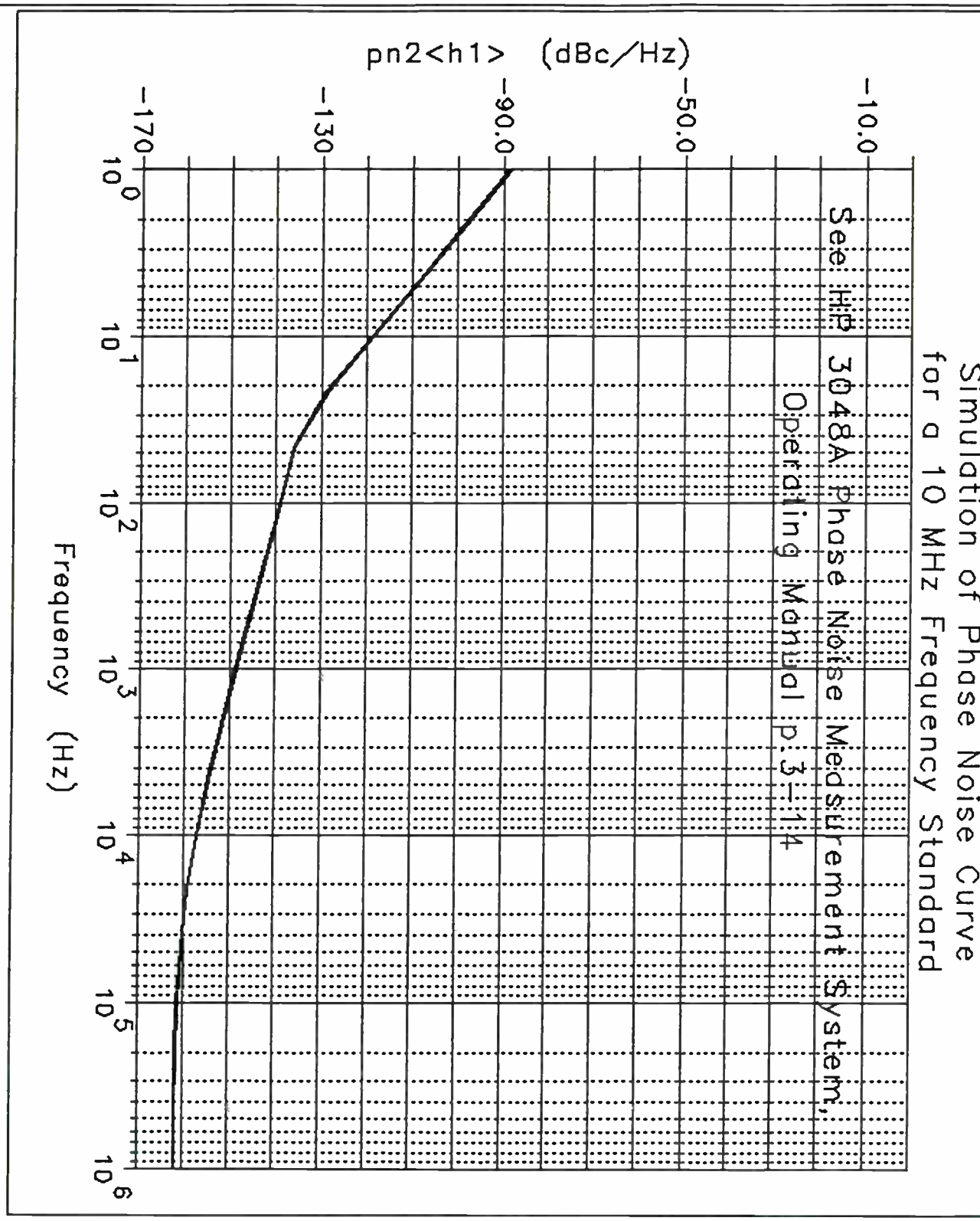
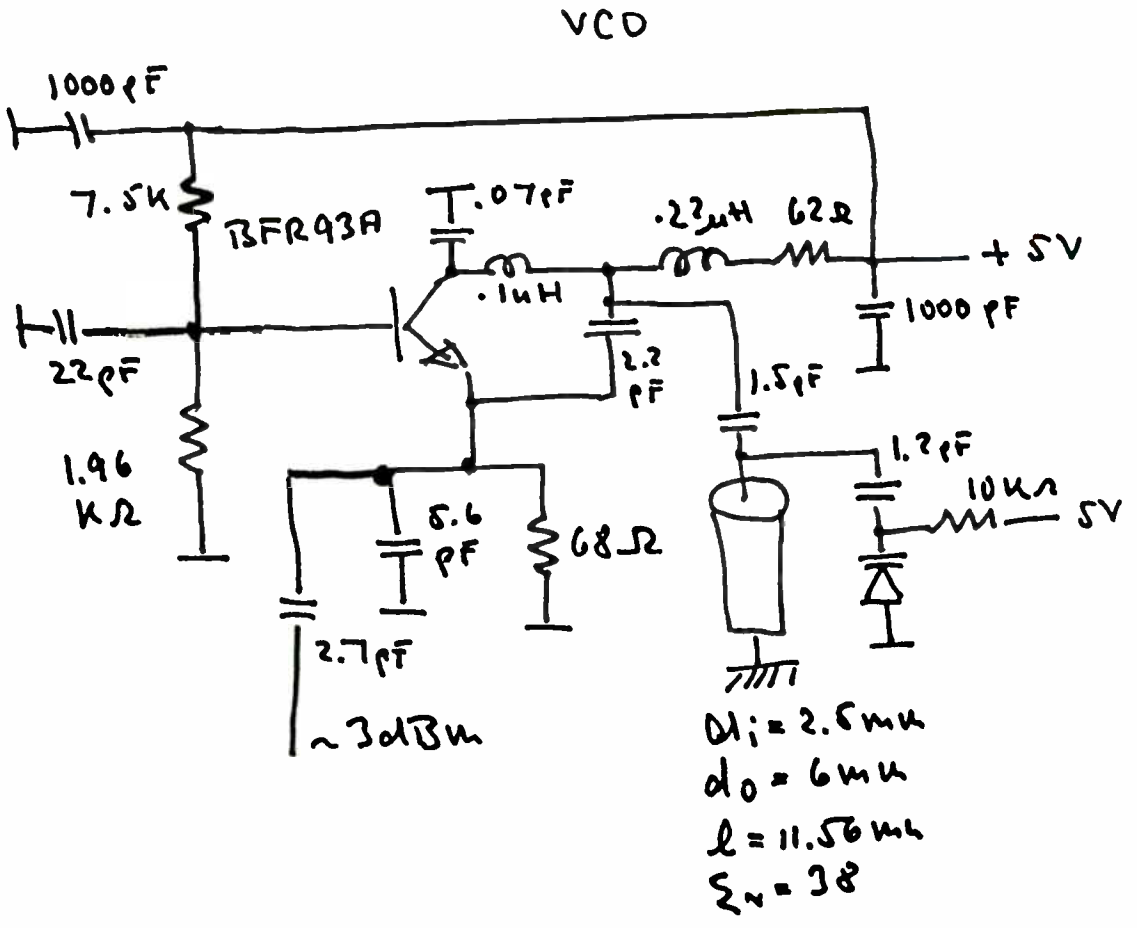


Figure 19b Shows the simulated phase noise of the oscillator as shown in Figure 18.



23 July 1990

Figure 20 Shows a typical test circuit for use in a ceramic resonator. These resonators are available in the range 500 MHz to 2 GHz. For higher frequencies, dielectric resonators are recommended.

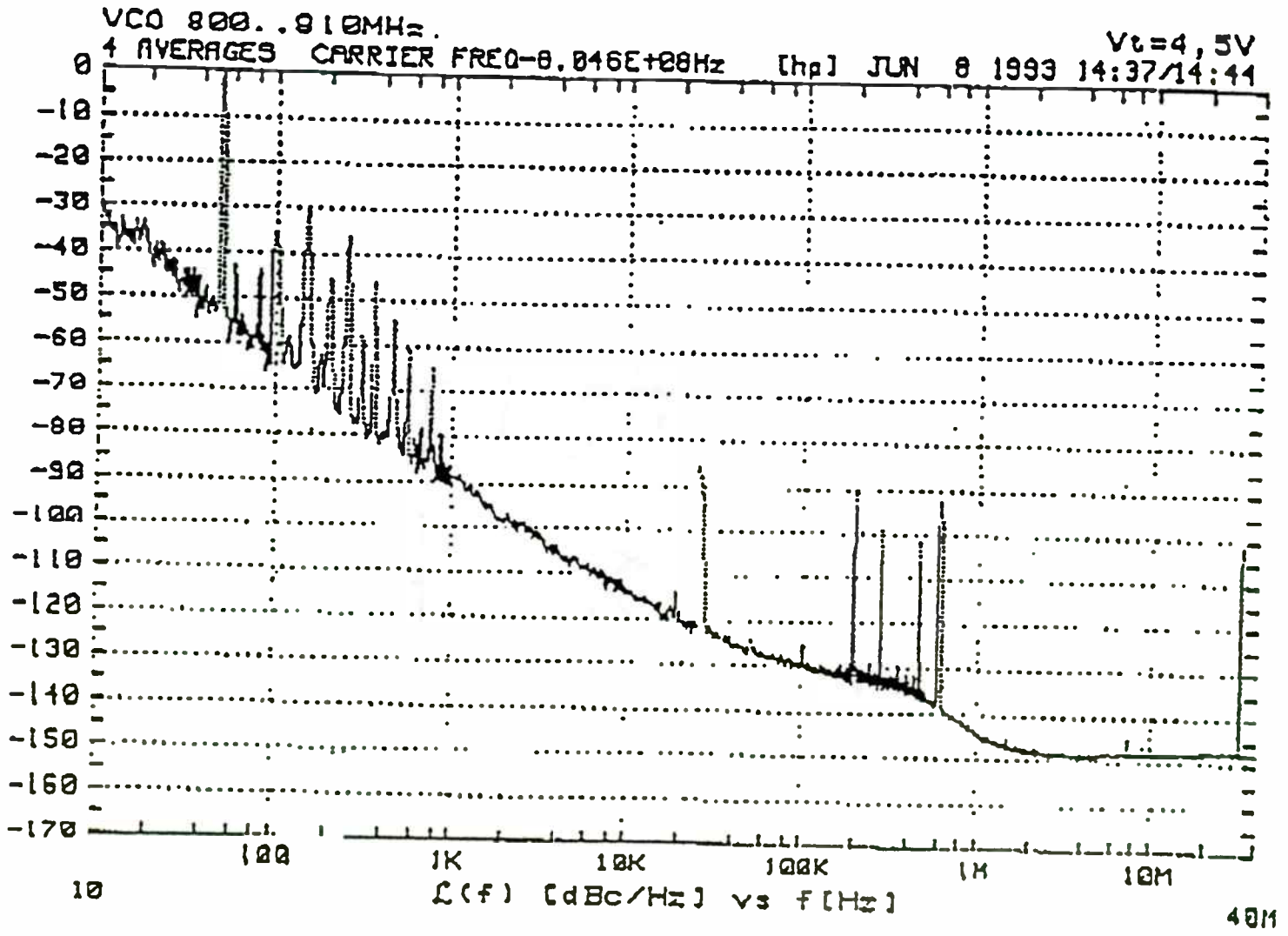


Figure 21 Shows the measured phase noise of the oscillator shown in Figure 20.

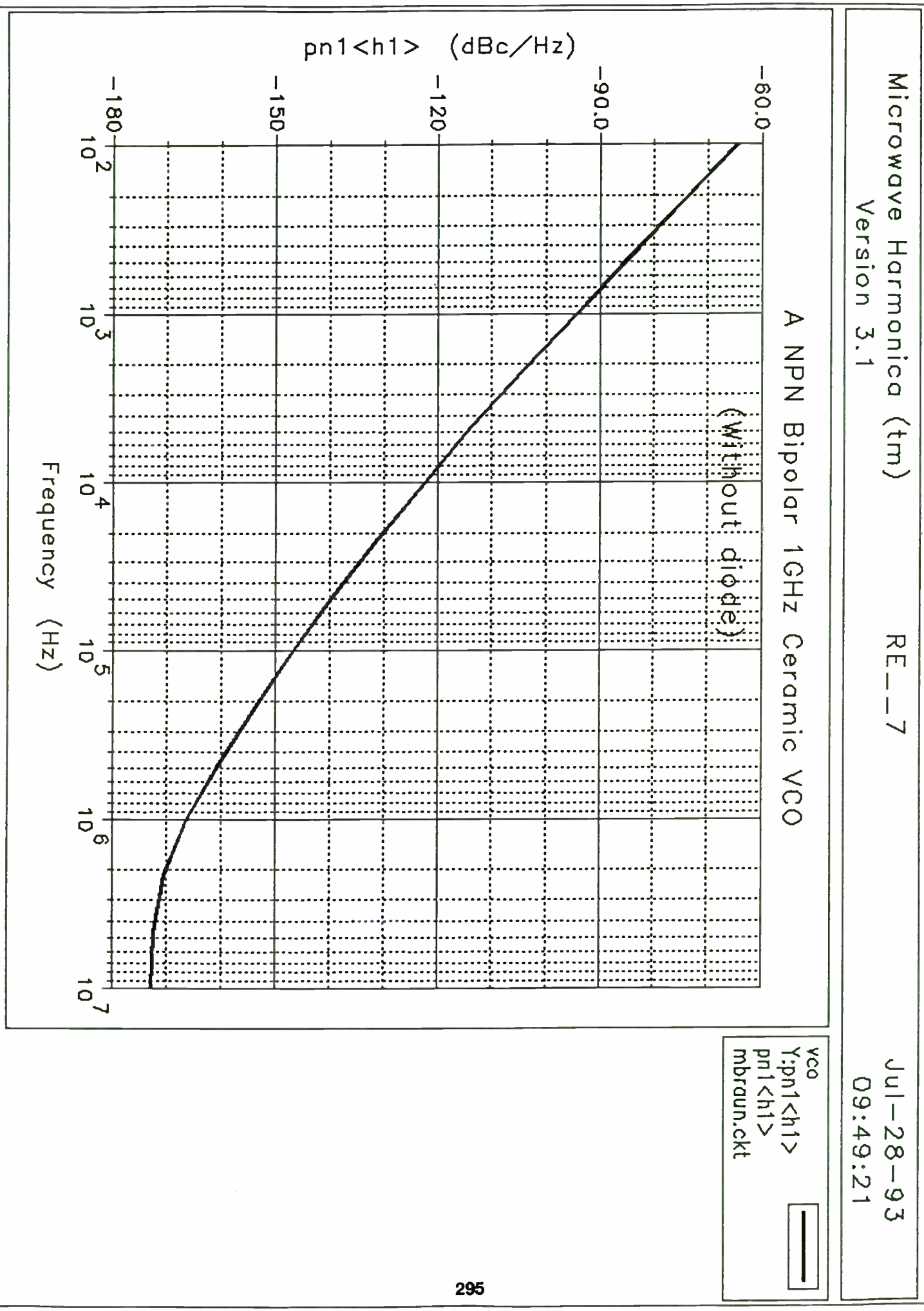


Figure 22 Shows the predicted phase noise of the 1 GHz ceramic resonator VCO

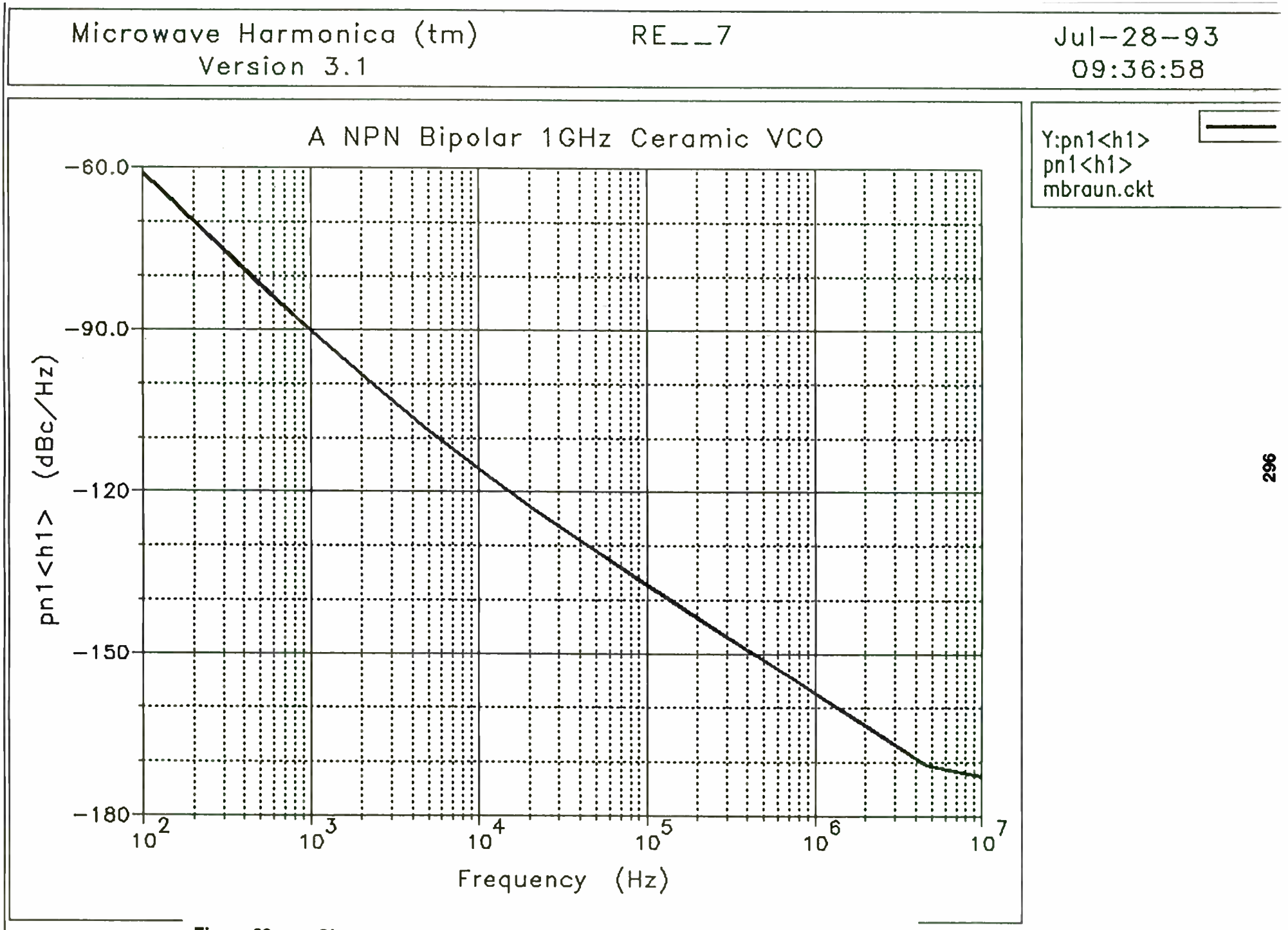


Figure 23 **Shows the predicted phase noise of the 1 GHz ceramic resonator VCO without the tuning diode attached. Please note the good agreement between the measured and predicted phase noise.**

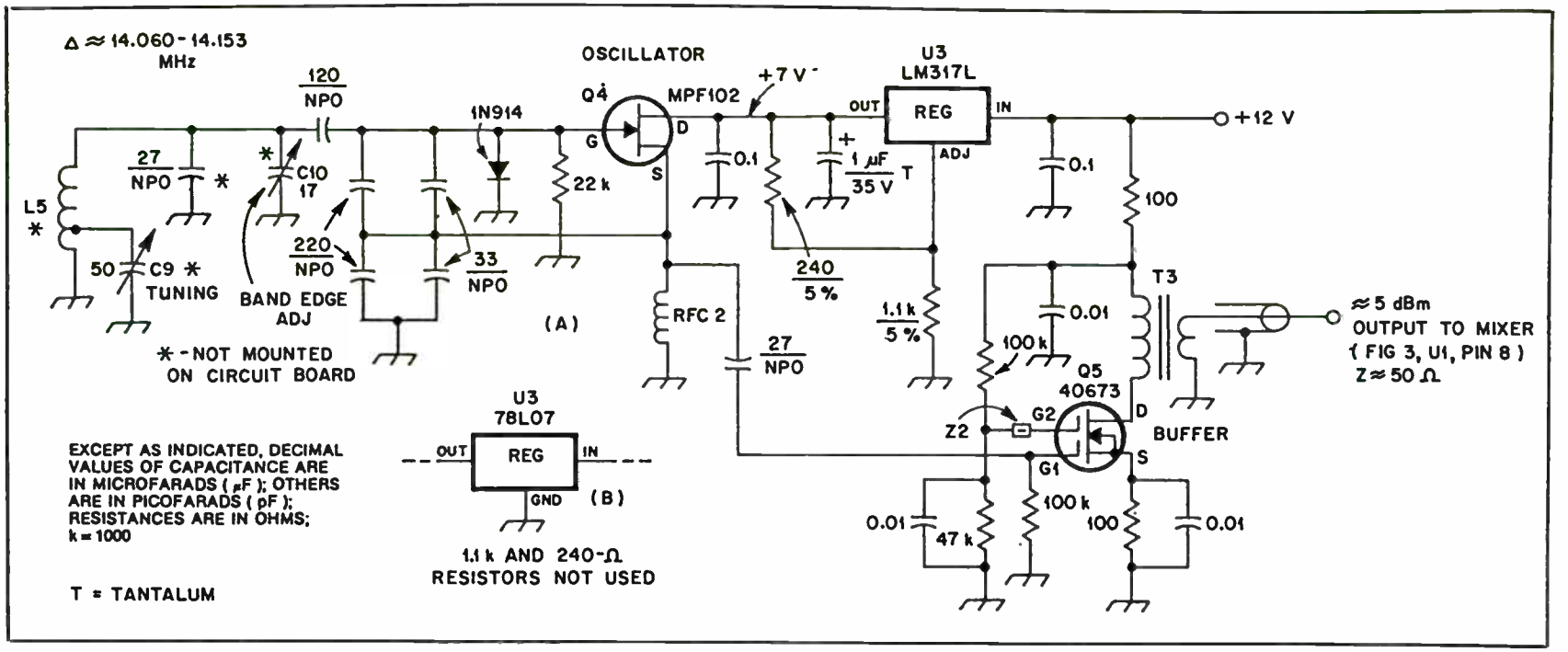


Fig. 4 — Schematic of the band-imaging receiver LO and buffer circuit. Capacitors are disc ceramic unless otherwise noted. Capacitors marked with polarity are electrolytic. All resistors are ¼-W, 10% units unless otherwise noted. At A, an LM317L adjustable regulator is used at U3. The inset at B shows connections for an 78L07 regulator at U3. For best stability, use only NP0 (C0G) capacitors in the circuitry associated with the gate and source leads of Q4. Space L5 by at least its diameter from other components and the LO shield box. See text and Fig. 8.

C9 — 50-pF air variable (Jackson Bros 4667-50 or equiv).

C10 — 17-pF air trimmer (Johnson 189-506-5 or equiv).

L5 — 1.4 μH: 11 turns no. 22 tinned wire, 24 turns per inch (Barker & Williamson 3038 Miniductor). Tap at 2 or 3 turns from ground end. See text and Figs. 8 and 9B.

Q4 — MPF102 JFET.

Q5 — 40673 dual-gate MOSFET.

RFC2 — 39 μH: Miller 70F395AI, or 24 turns no. 26 enameled wire on Amidon FT-50-61 ferrite toroid core.

T3 — Transformer wound on Amidon FT-37-43 ferrite toroid core or equiv. Primary (50 μH): 11 turns no. 26 enameled wire. Secondary (3.8 μH): 3 turns no. 26 enameled wire.

U3 — Voltage regulator, LM317LH, LM317LZ or (with circuit changes shown at inset B) 78L07.

Z2 — Ferrite bead on Gate 2 lead of Q2, Amidon FB-43-101 or equiv.

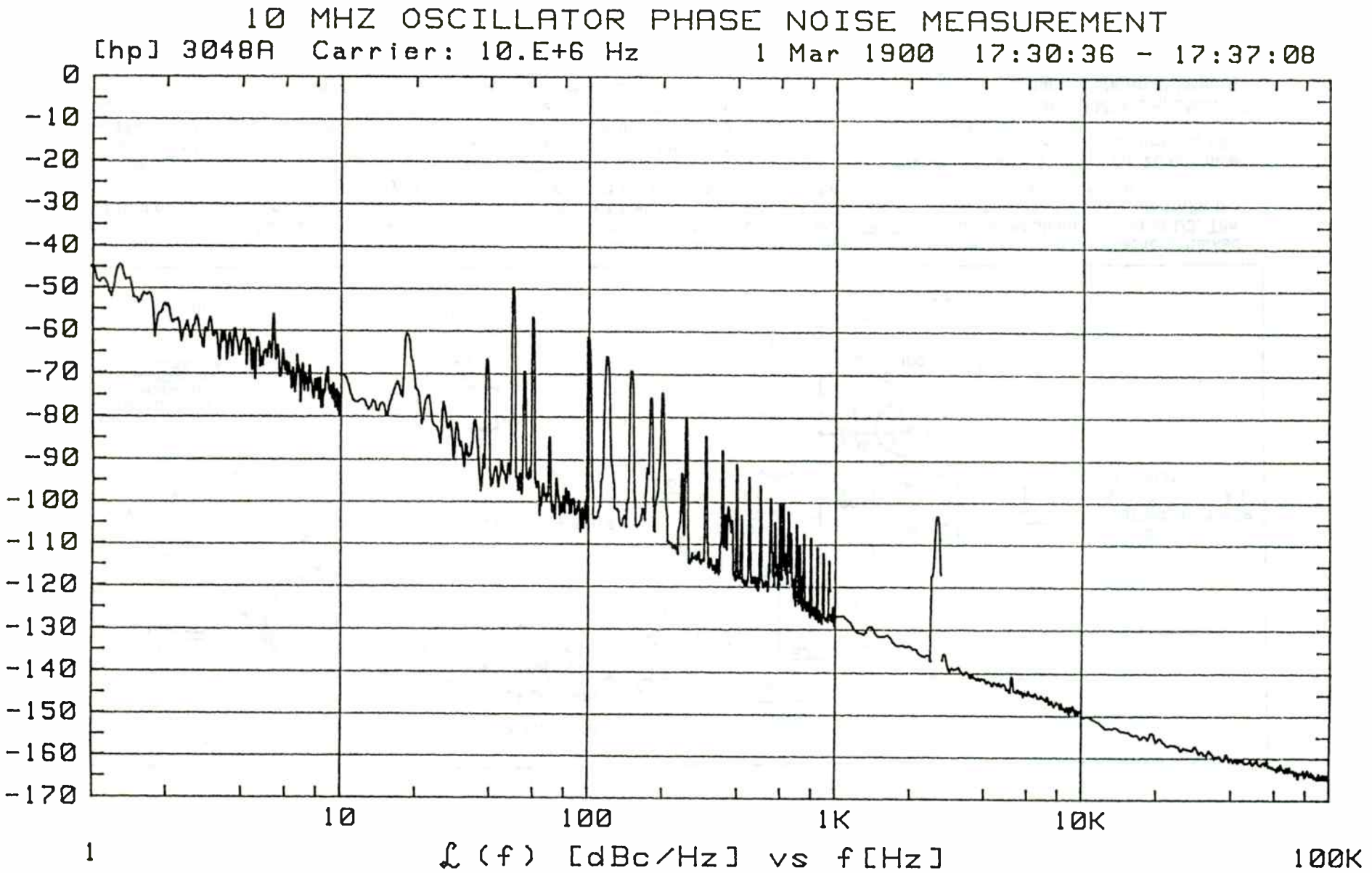


Figure 25 **Shows the measured phase noise an oscillator of this type.**

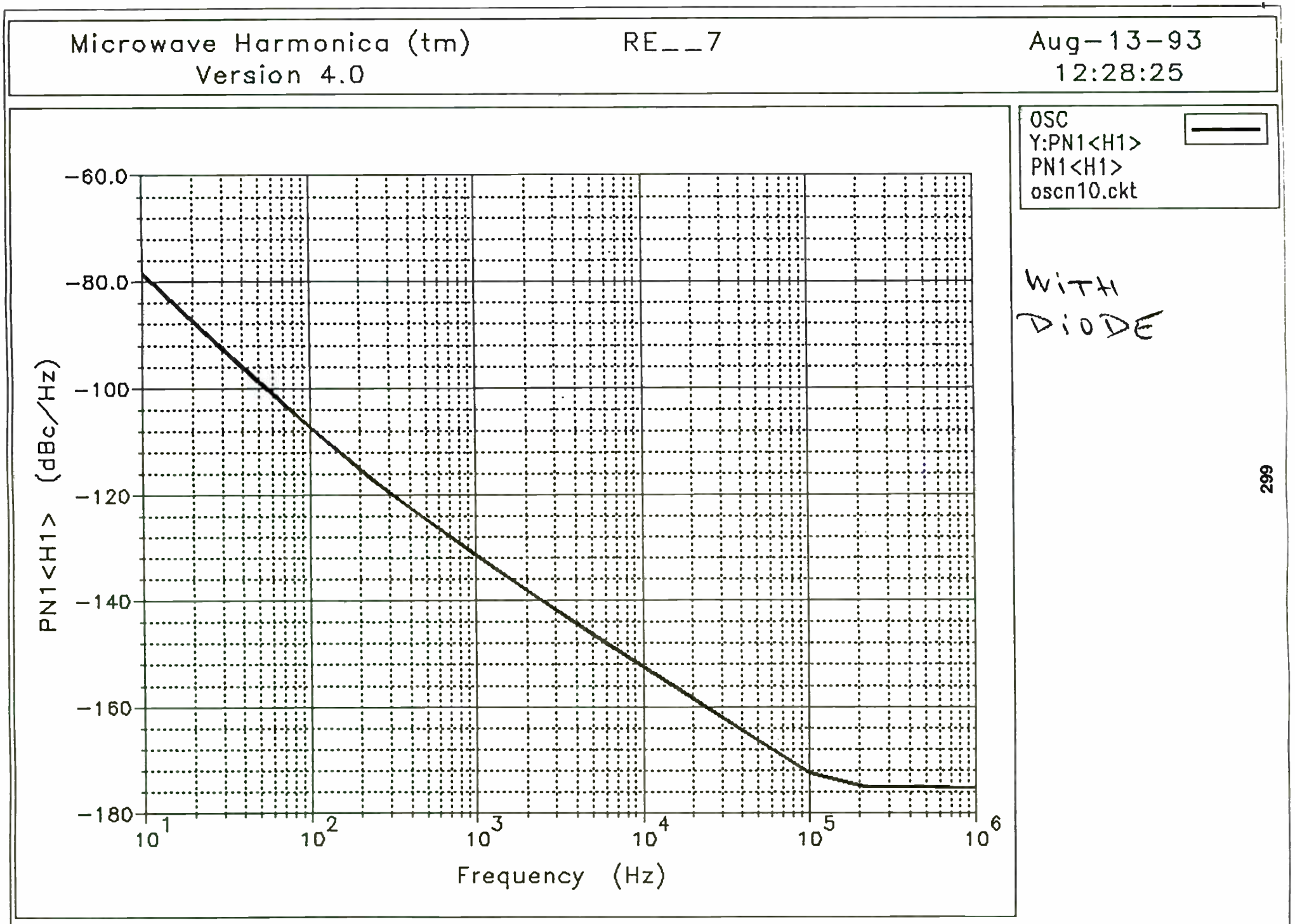


Figure 26 **Shows the simulated phase noise of this type of oscillator with**

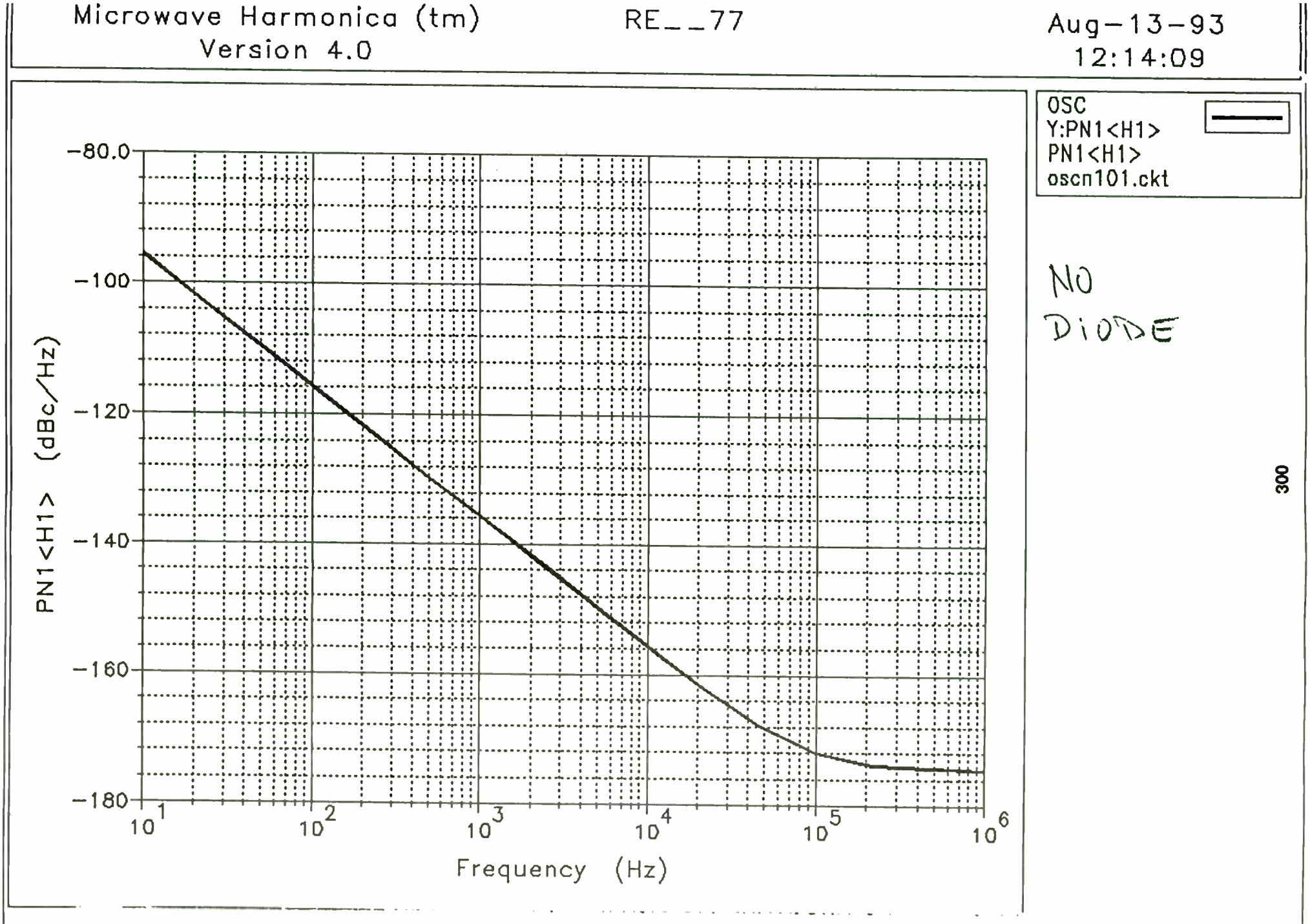


Figure 27 Shows the simulated phase noise of this type of oscillator without a clipping diode attached.

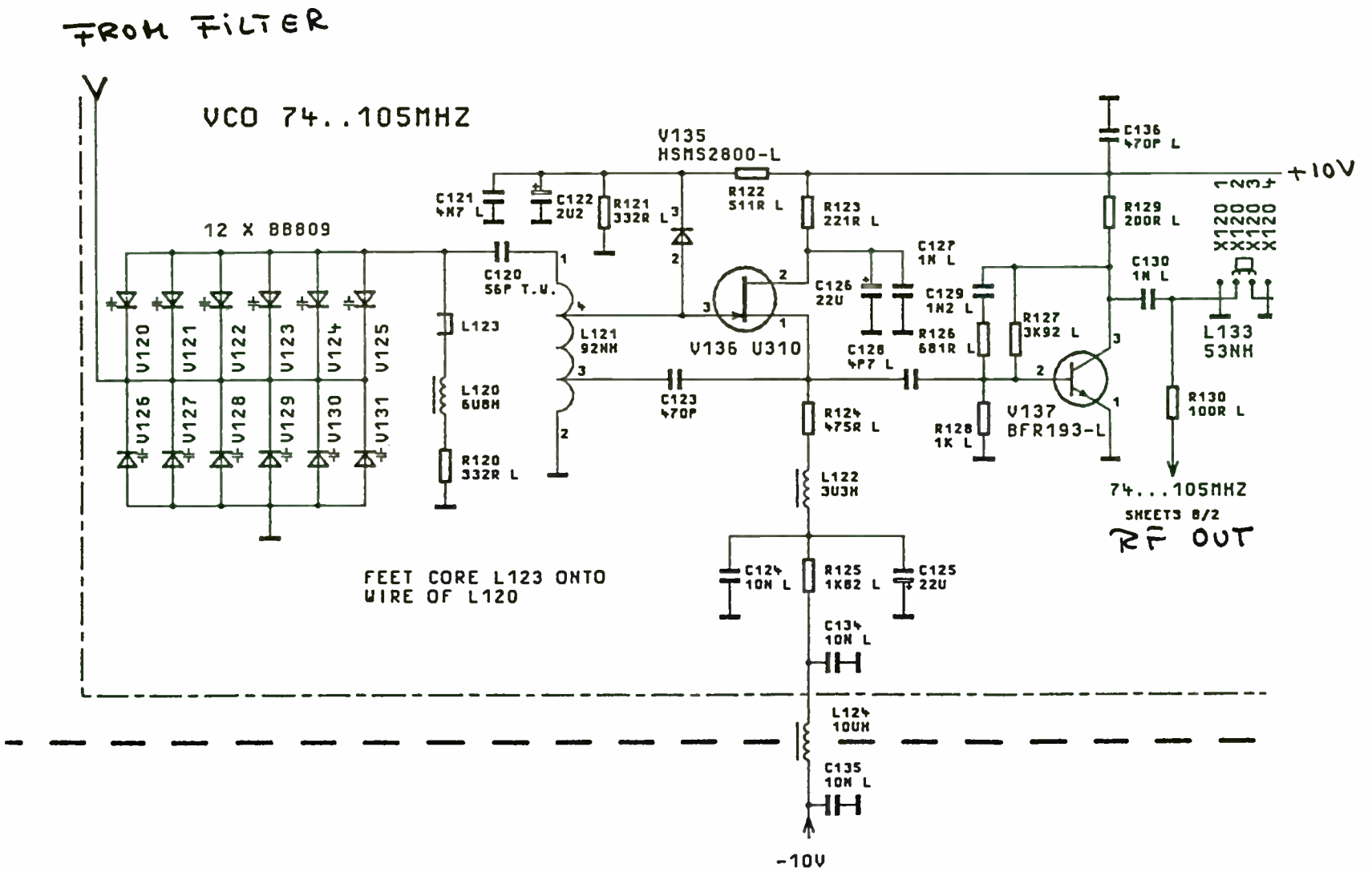


Figure 28 Wideband VCO with a large number of tuning diodes to improve phase noise. Note that the diode is biased in reverse and does not follow the positive clipping as published by other authors.

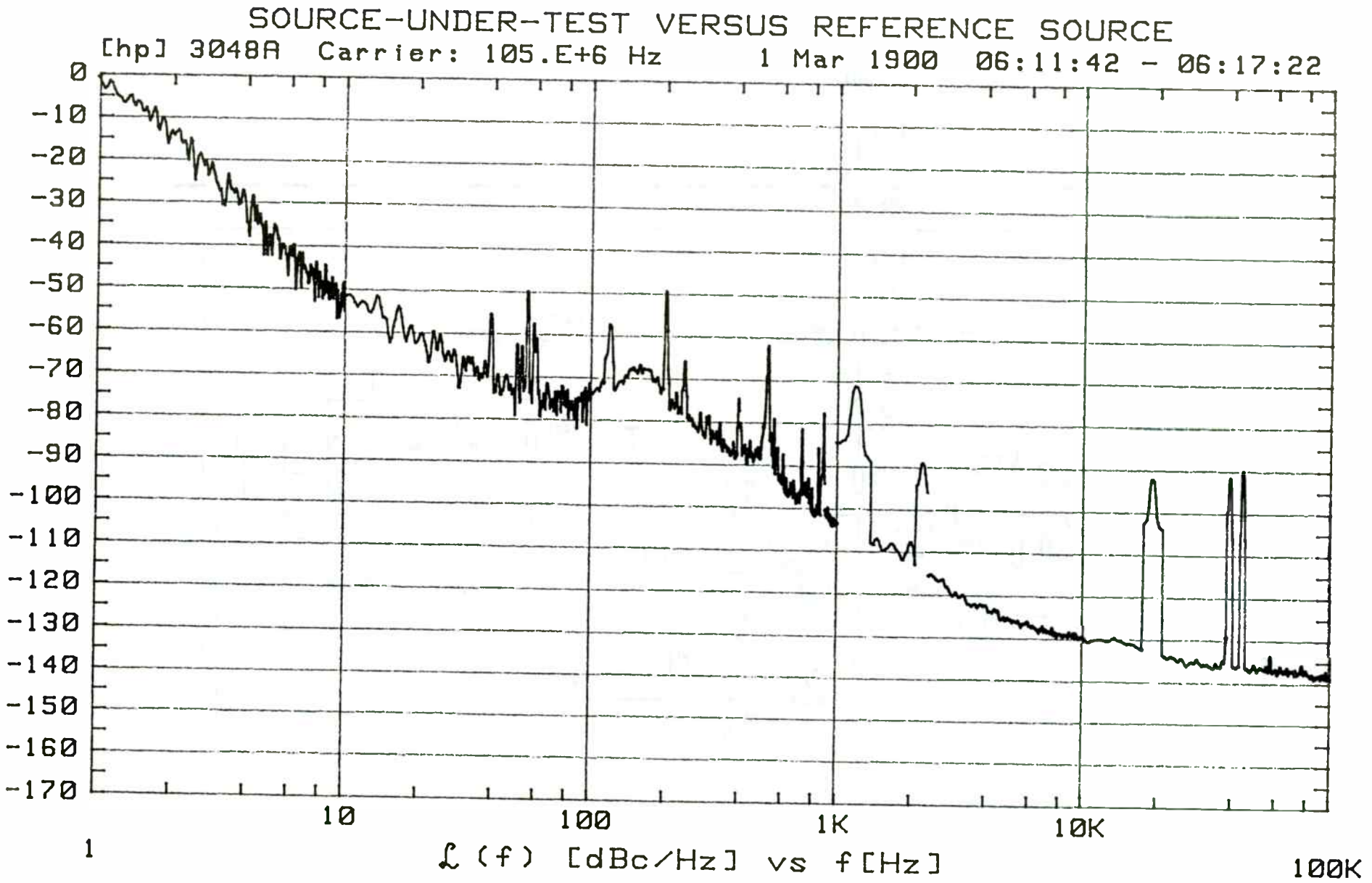


Figure 29 **Shows phase noise of the multi-diode VCO in a PLL system**

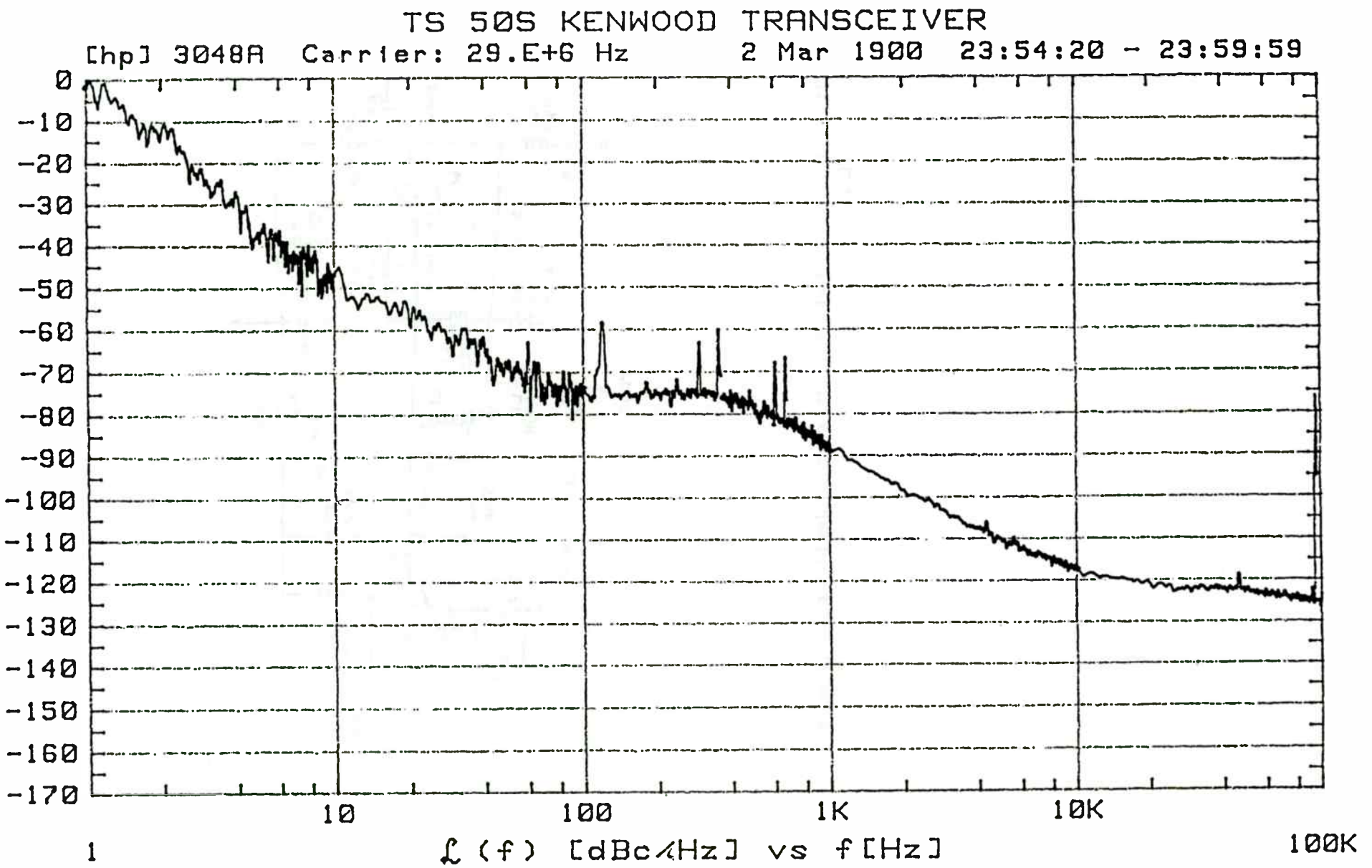


Figure 30 Shows phase noise of the TS-950, which is 10dB worse than the multi-diode system

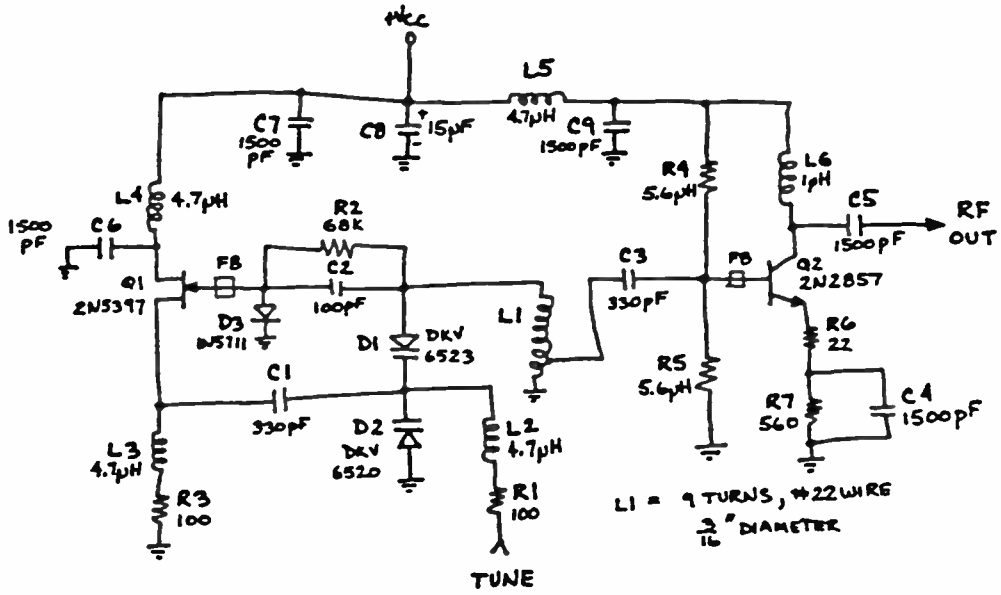


Figure 31 Shows a VCO which violates several rules in designing a good VCO

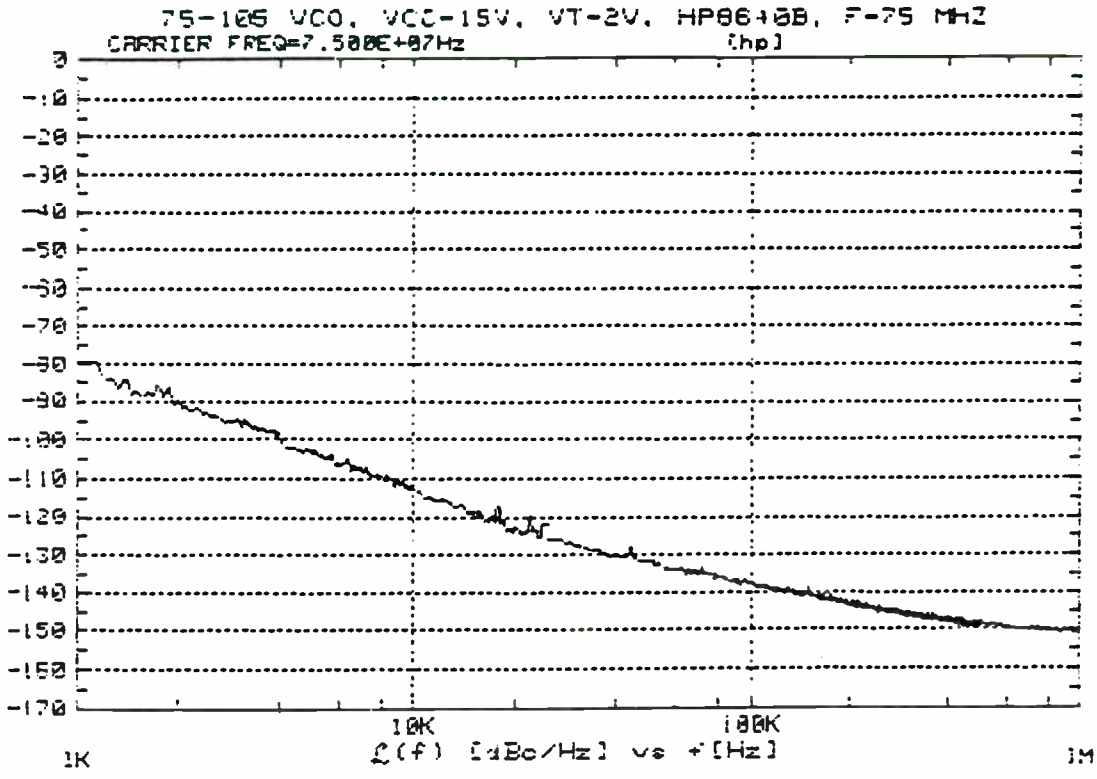


Figure 32 **Shows phase noise which is significantly below state-of-the-art**

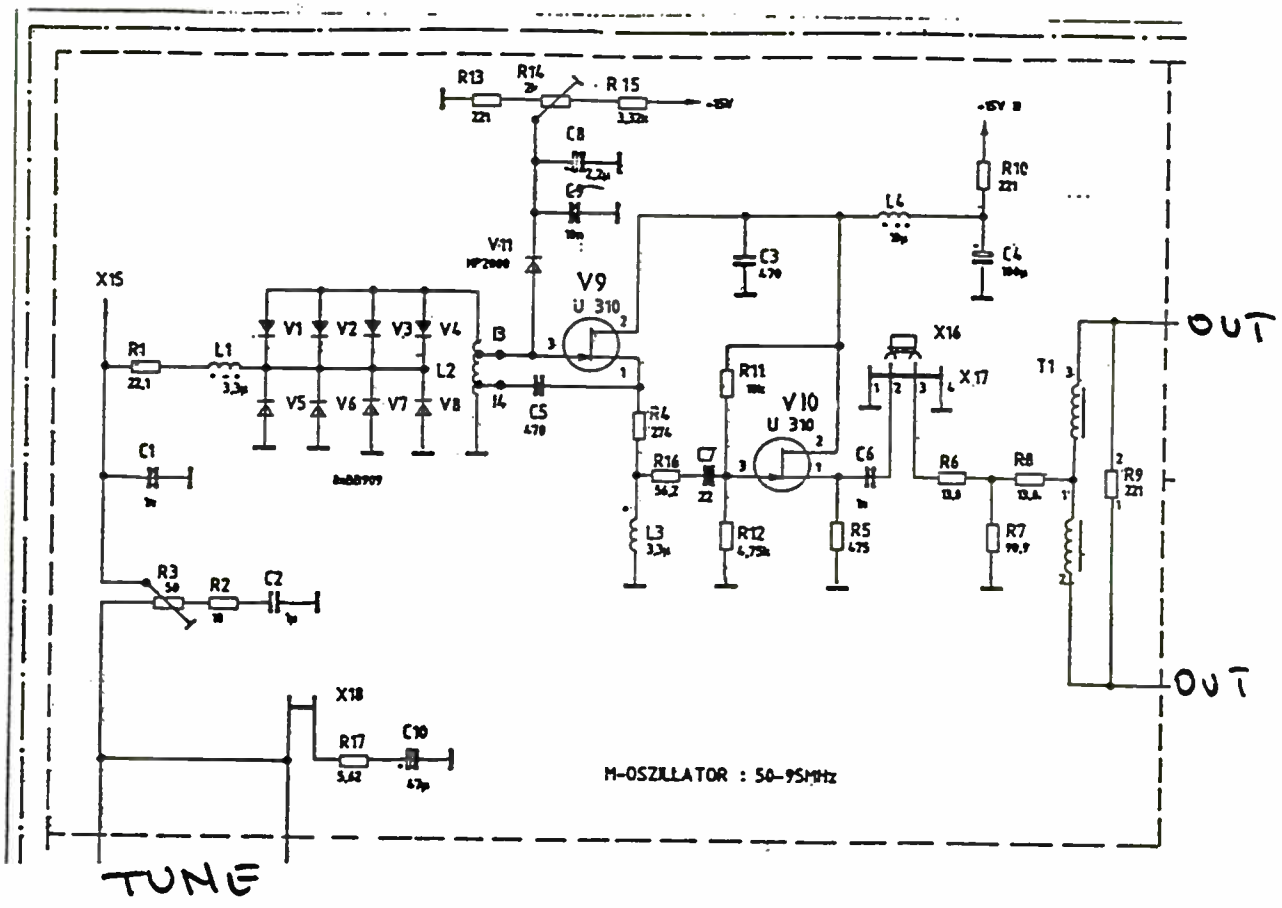


Figure 33 Shows a schematic which is a spin-off of Figure 28 and uses a 3 dB power divider at the output

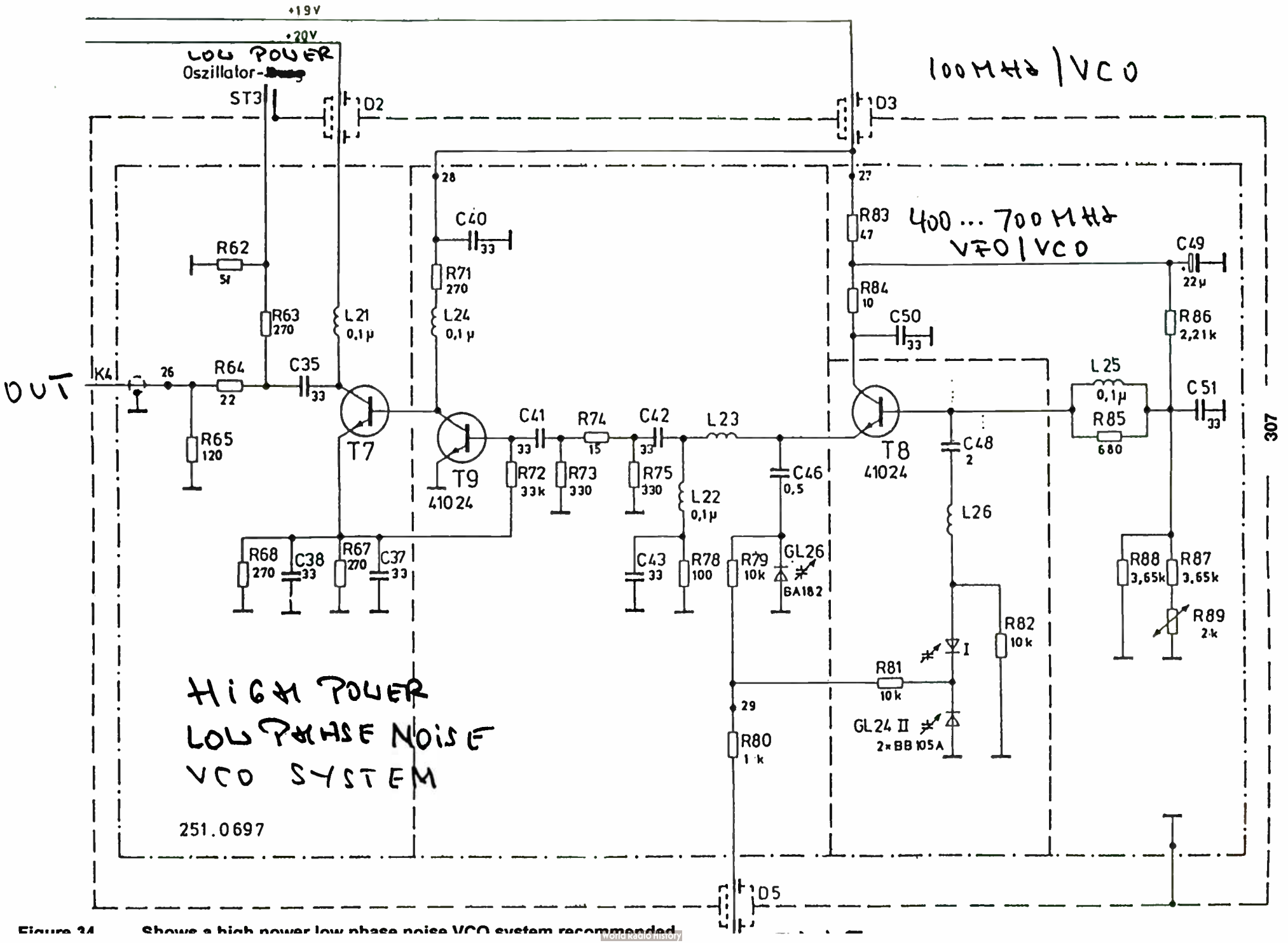


Figure 34 Shows a high power low phase noise VCO system recommended

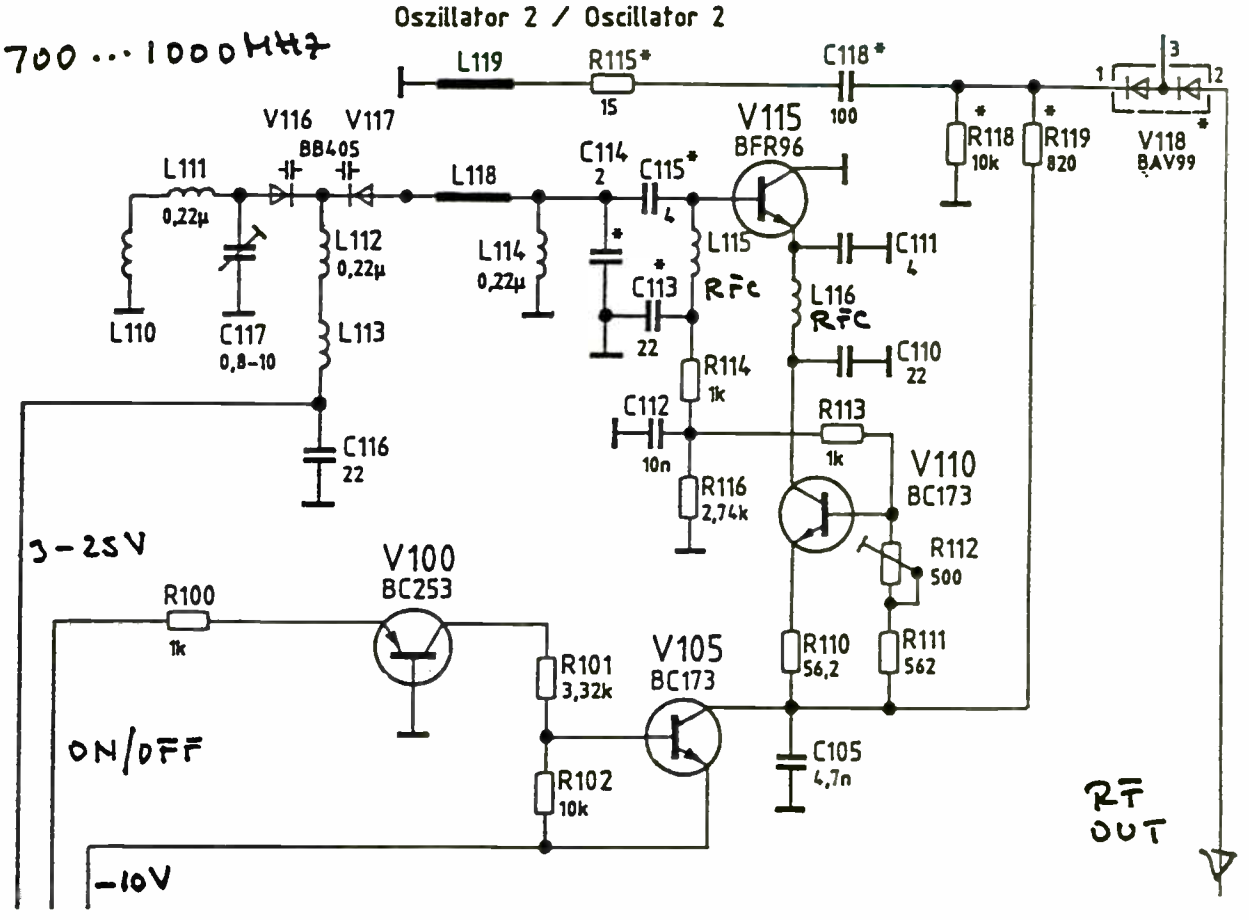


Figure 35 Shows a recommended VCO covering the frequency range from 700 MHz to 1 GHz

The Application of Super-SPICE in the design of Multi-layer Boards

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Compact Software, Inc., 201 McLean Boulevard, Paterson, NJ, 07504, USA

Introduction

RF and microwave circuits frequently use distributed elements as circuit components in amplifiers, oscillators, mixers, phase shifters, and switches. These circuits operating in the RF/Microwave range are simulated using a combination of linear frequency-domain analysis and harmonic-balance frequency-domain analysis. Accurate models for transmission lines, discontinuities, coupled lines and active devices are required for meaningful simulation results.

Frequency domain simulators cannot model transient effects. To properly analyze startup conditions and transient effects, a time domain simulator capable of handling high end RF/Microwave frequencies is required.

In high speed digital circuits, traces on the PCB can act as coupled signal lines causing unwanted parasitic effects that create crosstalk, reflections, loss and bounce. These effects can lead to false triggering of logic circuits and degrade system noise margins. While crosstalk has often been omitted from PCB design analyses, increasing clock speeds and board densities will necessitate crosstalk analysis on high speed signals to ensure future success.

Traditional Approaches

Microwave and RF designers have used a combination of frequency and time domain simulation techniques for a number of years. The harmonic balance technique is used for steady-state nonlinear analysis and optimization in tools such as the Microwave Harmonica nonlinear simulator. However, the analysis of true transient effects such as oscillator start-up and step recovery is impractical using such a technique, as this technique is valid only for steady-state solutions. Harmonic balance methods are limited to circuits containing less than about 30 transistors and signals with slow/finite rise-times. These simulators are currently limited to a harmonic balance product

[2 x # of harmonic products] x [# of transistors]

of about 600 using current workstation technology.

Time domain simulators such as SPICE are widely used but they generally lack the capability of providing accurate models for microstrip components such as bends and junctions (tees) as well as dispersive, lossy distributed elements such as single or multi-layer transmission lines. Popular versions of SPICE typically lack models for high frequency components that are often found in microwave frequency domain simulators. These SPICE implementations also do not provide S-parameter data without special augmented circuitry.

For digital applications, rising clock rates and increasing circuit densities are causing transmission line effects and electromagnetic coupling to take on increased importance. Traditional PCB design techniques have either treated layout effects using a single lumped model, or have used SPICE-type simulations on a single critical path to examine signal reflections and bounce. EM effects are usually neglected by PCB designers, and only a few crosstalk tools are commercially available. Recent developments in PCB design software have included heuristic rules-based approaches to avoiding crosstalk and ensure EMI/RFI compliance.

Super-Spice

Super-Spice is an enhanced time domain simulator that combines advanced models of RF/Microwave circuit components with a two-dimensional electromagnetic solver to accurately calculate crosstalk. Super-Spice is integrated with a graphics framework that includes integrated schematic capture (Figure 1.) The

simulator can also use standard SPICE syntax netlists and models.

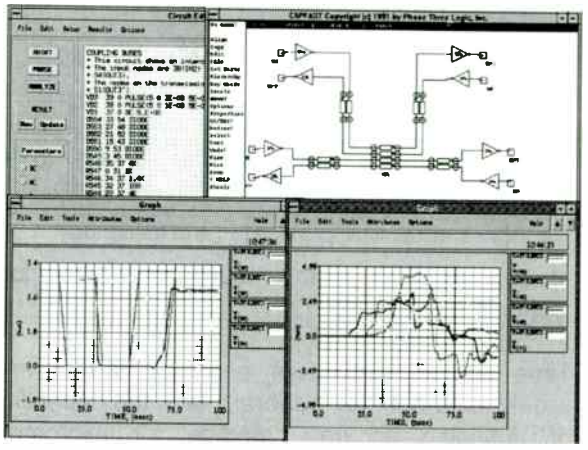

Figure 1. Typical Super-Spice session showing schematic diagram, netlist, and performance plots.

The two-dimensional electromagnetic solver calculates the field effects around distributed elements and discontinuities. This solver has been tested for accuracy in PCB applications with rise times down to 100 picoseconds. Super-Spice automatically generates equivalent circuits and implements them into the matrix equations, resulting in fast setup times.

Included are enhanced capabilities for modeling lossy coupled structures in microstripline, stripline, coplanar waveguide and other media. This facilitates the accurate modeling of transmission lines for high frequency applications. The Wirth technique[1] is used for the analysis of lossy multiple-coupled lines. This is a fast technique when coupled to the 'method of lines', and is used for the calculation of the characteristic transmission parameters. Loss computations for finite metal conductor thickness result in accurate simulations. A large variety of microstrip-line discontinuities typically encountered in high-speed board layouts are modeled. These include steps, right-angle bends (with and without chamfers), tee junctions and cross junctions.

Super-Spice can accurately analyze a system of parallel coupled transmission lines. The model supports up to five dielectric layers and four signal layers as shown in Figure 2. The signal lines can assume a finite thickness with some loss. This is particularly relevant for digital circuits where the conductor thickness can be of the same order as the conductor width. Possible propagation structures that can derived from this very general structure include microstripline, stripline, slotline, coplanar waveguide, and suspended substrates. Edge-coupled lines on the same layer, broadside coupled lines on different layers and transitions between various media can also be analyzed.

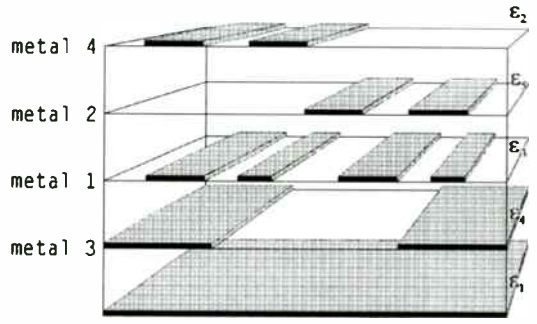

Figure 2. Super-Spice can model up to 5 dielectric layers and 4 signal layers

Digital Application Example

In digital applications, unwanted crosstalk between signals can cause false triggering of logic signals. Super-Spice can be used to accurately simulate transmission line and coupled behavior of PCB traces to determine if the PCB layout will cause functional logic problems.

A system of four coupled lossy transmission lines excited by a pulse is shown in Figure 3. This system is accurately modeled using the multiple coupled element. The microstrip lines were fabricated on a 1.27 mm thick Duroid™ substrate from Rogers Corp (Rogers, CT) with a dielectric constant of 10. The lines were 1.1 mm wide with a length of 230 mm separated by a distance of 0.42 mm. The pulse response (top, right) of the signal line is shown with an input signal of 6 ns duration and 4 ns rise time when all the lines are terminated in 50 ohms. The response on the forward-coupled line (bottom, left) and the backward-coupled line (bottom, right) indicate potential for crosstalk and erroneous switching in a digital circuit.

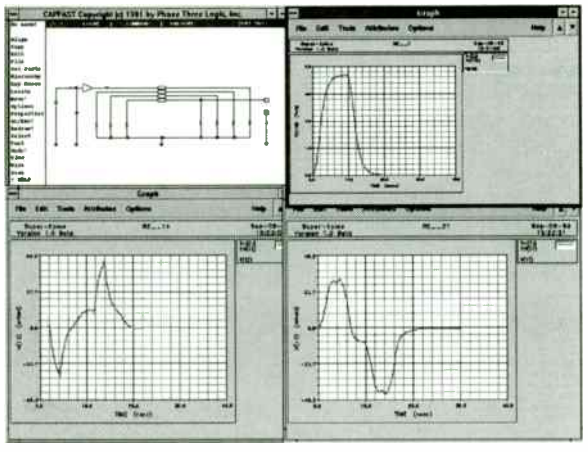

Figure 3. Simulation of EM coupling in a high speed PCB. Original pulse (top, right) created resulting forward coupled (bottom, left) and backward-coupled (bottom, right) signals

Analog Application Example

Consider the design of a dielectric resonant oscillator (DRO) whose schematic is shown in Figure 4. The topology shown here is commonly used for DROs in the microwave frequency range. A high-Q parallel resonant equivalent circuit is used to model the resonance of the dielectric puck in the neighborhood of the resonant frequency. Initial design of the oscillator in a linear manner can be performed using well-known methods in the frequency domain.

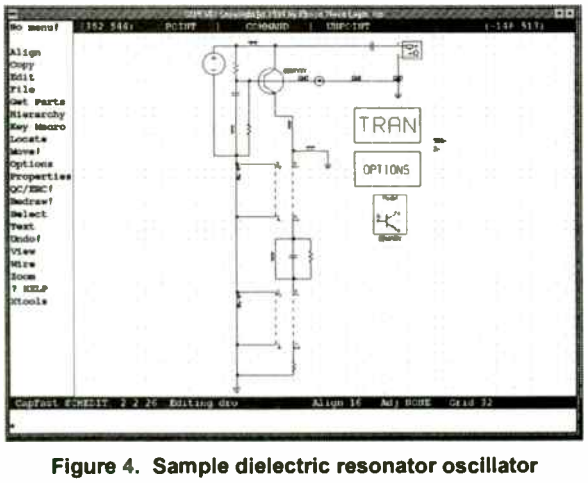

Figure 4. Sample dielectric resonator oscillator

The reflection coefficient of the entire circuit (S_{11}) including the resonator reflection coefficient can be plotted using Super-Spice and is shown in Figure 5. The presence of a negative resistance at the resonant frequency indicates that oscillations are possible. Large-signal transient simulation reveals oscillator startup conditions as well as the steady-state wave forms. Wave forms from the simulation are analyzed using post-processing functions within Super-Spice. For example, the Fourier transformation of a single period from the steady-state response into the frequency domain is shown in Figure 6. Harmonic content and efficiency can also be computed from the wave forms.

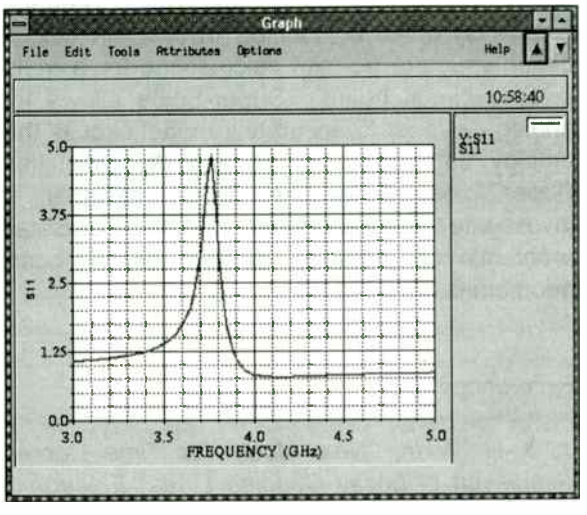

Figure 5. Super-Spice can plot the reflection coefficient of the DRO as well as the reflection coefficient of the resonator alone.

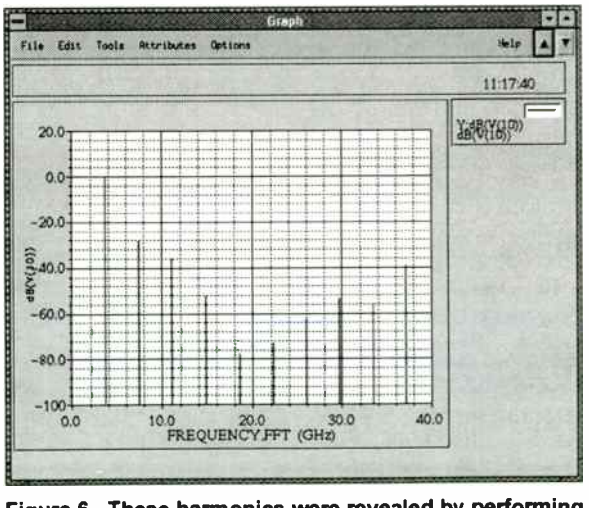

Figure 6. These harmonics were revealed by performing a Fourier transform on a single period of the DRO's output waveform.

Summary

Accurate simulation of RF/Microwave analog circuits requires models that include coupling, losses and microstrip discontinuities. Both linear, frequency domain simulation and nonlinear transient simulation depend on accurate models. High-speed digital PCB applications also require modeling of coupling between traces and losses on a single trace. An efficient two-dimensional electromagnetic solver has been implemented in Super-Spice to enable simulation of lossy coupled traces. A flexible circuit structure permits calculations for a multi-layered circuit board. Super-Spice allows the analog designer to accurately model circuits that employ both EM coupling and discontinuities. Super-Spice allows the digital designer to investigate signal-integrity and crosstalk problems on complex printed circuit board geometries.

Reference

1. K.-H. Wirth, "New Model for Time Domain Simulation of Lossy Coupled Lines" Electronics Letters, Vol. 26, No. 20, pp. 1723-1724, September 1990.

A SPICE-Model for Passive Diode Ring Mixers

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Abstract

Prediction of mixer performance is an easy task with state-of-the-art harmonic balance simulators like MDS (Hewlett Packard) or LIBRA (Eesof). However, it is much more difficult to find the appropriate models and model parameters for particular devices. A possible solution to this problem is the use of macromodels. They represent exactly the electrical behavior of the device, independently of the internal structure.

This article describes a macromodel for passive diode ring mixers for frequency range up to 1 GHz. The models are usable for all commercial harmonic balance simulators as well as for the standard SPICE 2G6 simulator.

The model structure is very similar to the real topology of a passive mixer. It is characterized according to the RF performance by optimization. Basis for the optimization are the data sheet and measurements. Mixer measurements are performed by an automatic PC based measurement system with a Rohde & Schwarz FSBS network/spectrum analyzer.

The mixer model describes as well the transfer characteristics like conversion loss and isolation, the reflection performance as the linearity (compression and third order intermodulation).

The procedure of computation of the model parameters is also presented. For effective characterization a semi-automatic test system has been implemented with the MDS simulator from Hewlett Packard. It allows the complete characterization of a passive mixer in a few days.

Comparisons of a mixer model (SRA-1 from Mini-Circuits) with data sheet and measurements are also presented. The model´s performance of conversion gain shows exellent agreement within 0.5 dB. VSWR at the LO and RF port performance is better than 5 %.

1 Introduction

For realization of technical concepts in RF technology - like in other sectors too - the use of analog simulating tools is growing. This is nearly impossible without accurate models for commercial RF devices. At the moment accurate models of more complex RF components like mixers are not available.

At the Fraunhofer-Institute for Integrated Circuits models for frequency-synthesizing devices are developed. The work is funded by the Federal German Ministry of Research and Technology (BMFT) in a joint research project called "A Library for Complex Analog Devices". Within the scope of this project passive diode ring mixers and active mixers are

modeled based on the analog simulator SPICE-2G6. Diode ring and active mixer are used in many ways for communication and in the area of RF technology:

- Measurement technology for spectral and network analysis
- Transmitting and receiving equipment
- Front ends for telecommunication

The common structure of a diode ring mixer and results from simulations compared to data sheets and to measurements are presented. The model covers the mixer charactaristics conversion loss, reflection at the input ports and isolation. Furthermore nonlinear effects like compression or intermodulation are reproduced in acceptable accuracy. A selected passive diode ring mixer from Mini-Circuits is modeled.

2 Structure of a Passive Diode Ring Mixer

The physical configuration of a passive diode ring mixer (´Double Balance Diode Mixer´) comprises of a ring of Schottky diodes and two baluns (´Balanced-To-Unbalanced-Transformers´) as shown in **figure 1**. One pair of the four diodes is switched on during a half-wave of the LO signal. The other pair is turned off at the same time. Thereby a multiplication of the RF signal with the LO signal is produced. The topology of the model is very similar to the real structure. Every physical component in the mixer is modeled by the corresponding device model of the simulator.

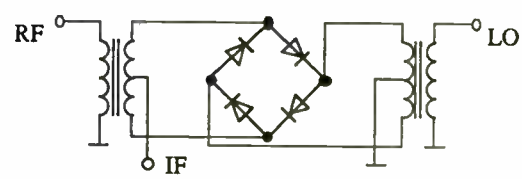

Figure 1 Common structure of a diode ring mixer

Before describing the structure of the model a short definition of the terminology of the most important mixer parameters is given.

3 Definition of the Circuit Parameters

The following characteristics are important:

- Conversion Loss
  The ratio between the power at the IF output and the given power at the RF input is described by the term conversion loss. Further information can be taken from **figure 2**.

- Isolation and Reflection
  Isolation means the coupling of an input signal to another input or output port. Reflection is the mismatching of a mixer to a driving source. These facts are also outlined in figure 2.

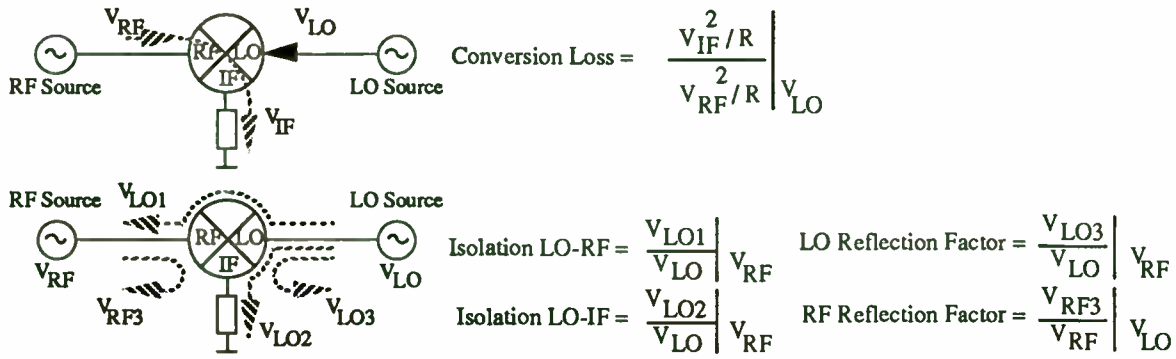

Figure 2 Definition of conversion loss, isolation and reflection

- 1dB-Compression-Point
  In ideal the conversion loss should be constant with rising RF power. In reality an increase can be seen from a certain RF power onwards. The RF power level corresponding to an increase of 1 dB of the conversion loss is called 1dB-compression-point - see **figure 3** -.

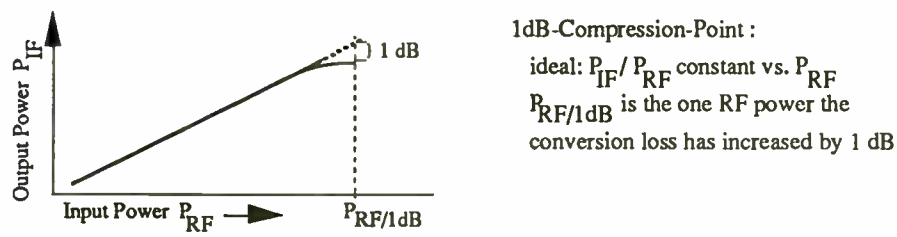

Figure 3 Definition of the 1dB-compression-point

- Intermodulation (IP3)
  An important criterion for a mixer´s quality is the intermodulation. It is characterized by the response to the two-tone RF signal of variable power. By measuring the power levels at terms of 1st and 3rd order the ideal behavior shown in **fig. 4** can be observed. The extrapolated intersection of the both straight lines is the so-called third-order-intercept-point (IP3).

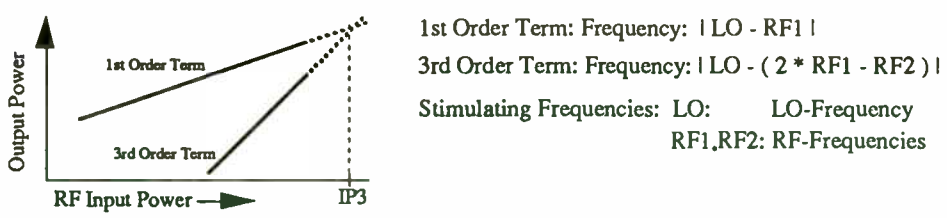

Figure 4 Definition of the third-order-intercept-point

According to the above characteristics the model parameters can be evaluated for a desired mixer by simulating the model and comparing the results to the data sheets. Only conversion loss, reflection and isolation will be used for parameterizing. When the values are determined correctly, nonlinear effects like compression or intermodulation will be reproduced in acceptable accuracy.

The stategy to parameterize the model is shown in chapter 5. The achieved results for the passive diode ring mixer SRA-1 from Mini-Circuits will be presented in chapter 6. At first the developed model structure will be described entirely in the following section.

4 Model Structure

The common model structure is orientated to the physical device construction as far as possible. It is shown in **figure 5**.

The diodes are described by the diode model existing within the simulator. The baluns are modeled by coupled inductors - L and K devices -. The core losses are built up by the resistors connected in parallel to the primary windings. Couplings between a port and the case are modeled by capacitors.

To take the isolation into account the way of modeling close to the reality was left. The isolation is implemented by insertion of separate filter elements between the ports. The DC-decoupling existing in reality between the ports was furthermore considered. This modular construction was favourable during parameterizing. By this way of modeling the isolation, the behavior concerning the isolation could be separated much better from the behavior concerning conversion and reflection.

The presented model can be run on any simulation system, which is compatible to Spice-2G6 and is able to perform a correct frequency transformation (FFT) - e.g. PSpice® from MicroSim Corp..

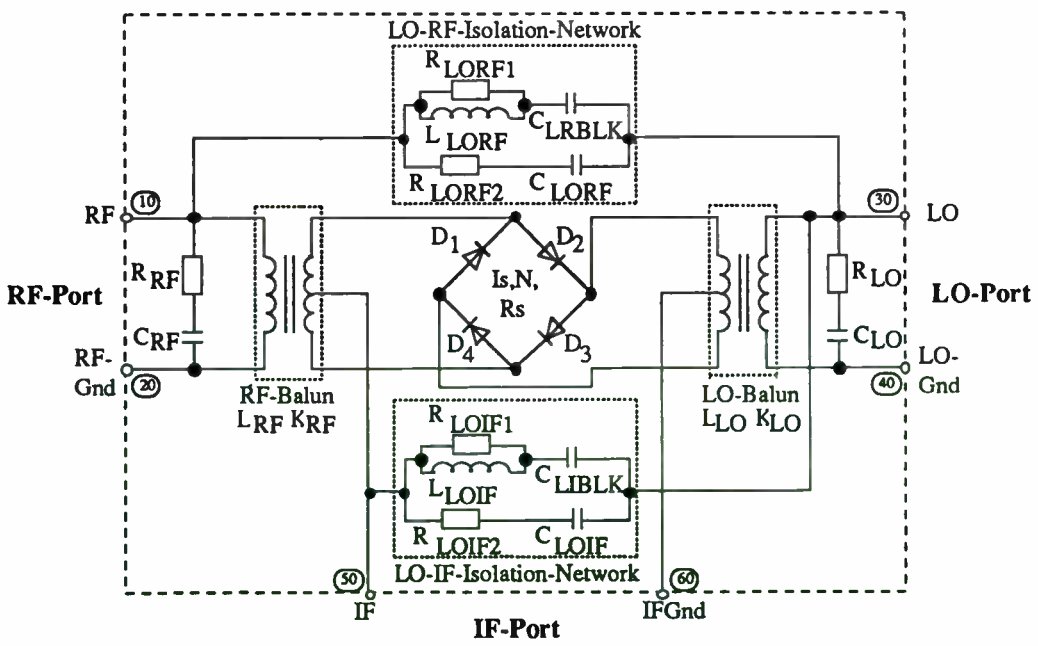

Figure 5 Common structure of the model for passive diode ring mixers

5 Parameterization

Parameterizing the model shown in figure 5 is very time consuming using the transient analysis, which is the only way to simulate frequency synthezising components in time domain simulators like Spice. It is impossible to calculate the model parameters analytically. The desired model characteristics have to be implemented by fitting the simulation results with data sheets or measurements.

Therefore simulation programs with an extensive user interface like the Microwave Design System (MDS) from Hewlett Packard are recommended. For effective parameterization a semi-automatic tool was developed based on MDS [4]. The time for characterization a diode ring mixer can be reduced then to a few days. The strategy to parameterize the model for mixers from Mini-Circuits is shown in **figure 6.**

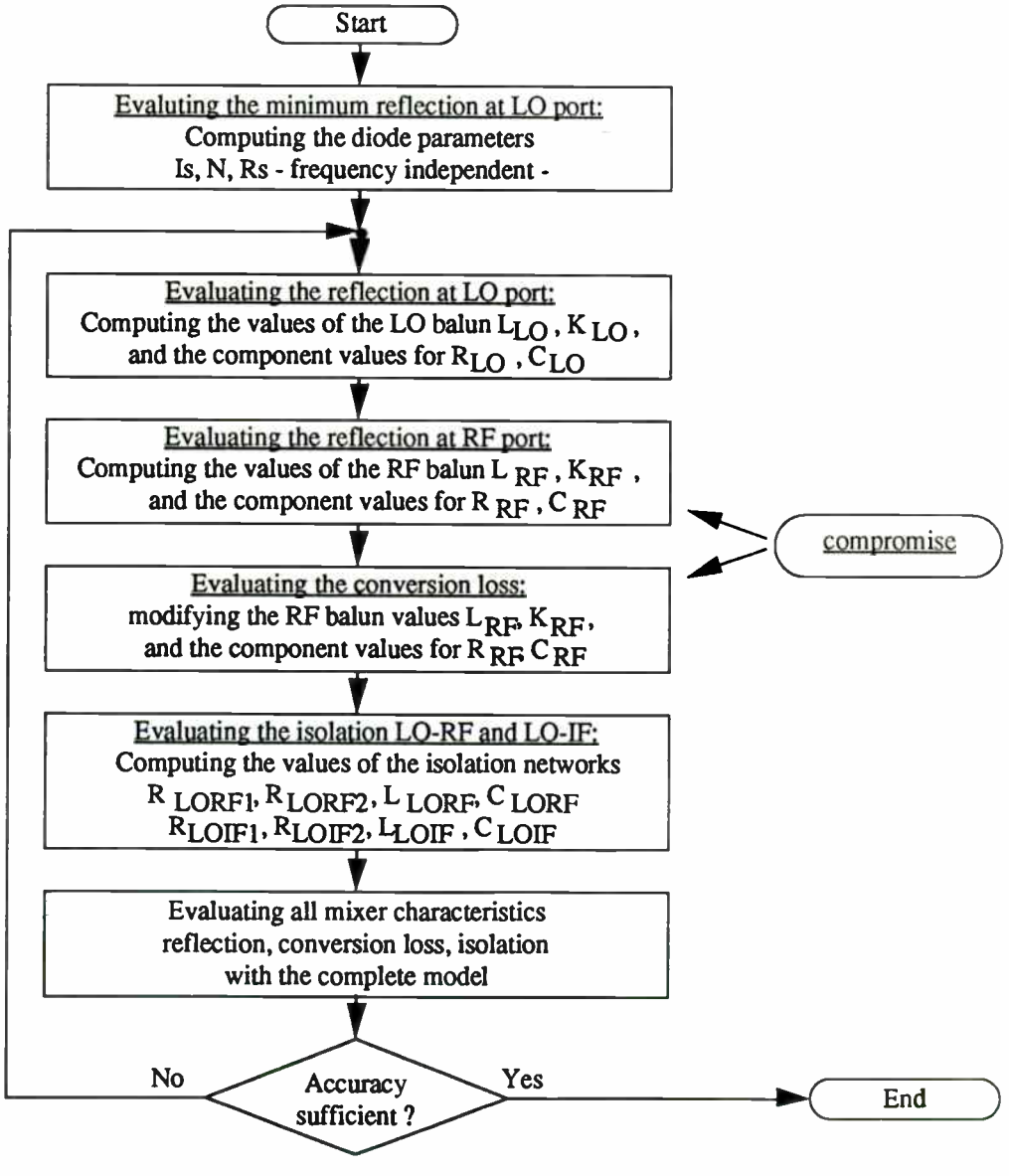

Figure 6 Strategy for parameterization

In the first step the model is adapted statically - neglecting the frequency-dependent behavior - by computing the diode parameters. The dynamic behavior is implemented by fixing the values of the baluns and the additional components afterwards. In most cases the values of the diodes have to be modified. Finally the component values of the isolation networks are calculated.

5.1 Diode Parameters

To calculate the diode parameters the reflection at the LO port is used. Due to symmetry the RF part of the model can be neglected. To establish frequency independence the LO balun is substituted by an ideal transformer built up by controlled sources. The simulation circuit is shown in **figure 7**. The 50Ω-resistor in series to the source represents the impedance of the generator.

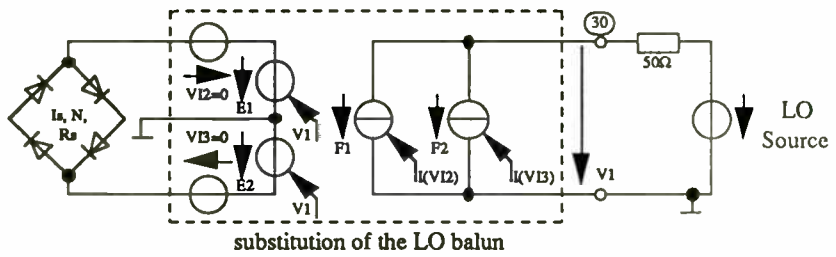

Figure 7 Simulation circuit to calculate the diode parameters

In the data sheets from Mini-Circuits the reflection at LO port is listed at three different LO power levels. Furthermore the dependence over a frequency range is documented. In the first step the model shall be considered frequency independent. Therefore only the minimum value in each case of the three LO levels is used. By these reflection values the static diode parameters saturation current Is, emission coefficient N and series resistance Rs can be calculated.

To fit Is, N and Rs transient simulations with the circuit shown in figure 7 have to be executed. A FFT afterwards will give the simulated reflection which is to compare to the data sheets. By correct choice of the parameters the simulated reflexion at the LO port will be constant over the whole frequency range and be the same as the minimal values listed in the data sheets.

5.2 Reflection at the LO Port

After adapting the model statically, the dynamic behavior of the LO port reflection within the frequency range must be implemented. Like above the RF part of the model is not necessary.

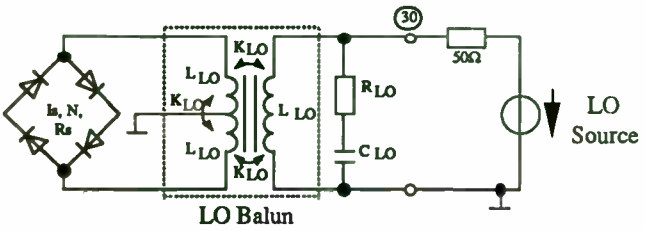

Figure 8 Simulation circuit to calculate the LO balun parameters and the values of the additional impedances

The simulation circuit is shown in **figure 8**. The inductor and coupling values L_{LO}, K_{LO} and the values of the components R_{LO}, C_{LO} can be calculated by simulations mentioned by computing the diode parameters. Furthermore in most cases the diode parameters must be modified.

5.3 Reflection at the RF Port

The parameters of the RF balun L_{RF}, K_{RF} and the values of the impedances R_{RF}, C_{RF} can be calculated by means of the reflection at the RF port. The simulation circuit shown in **figure 9** can be used.

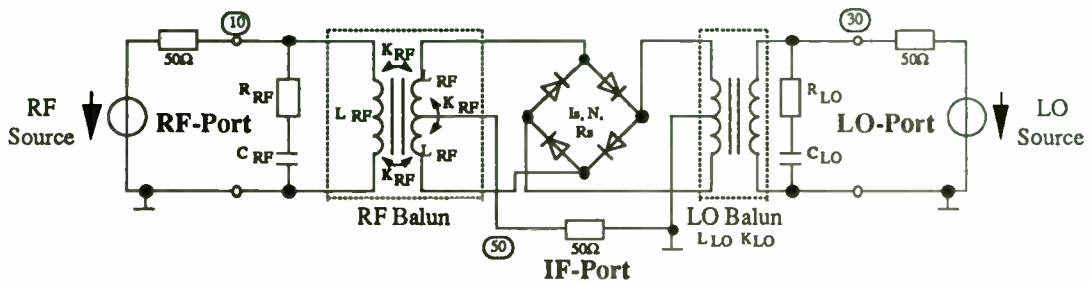

Figure 9 Simulation circuit to calculate the RF balun parameters and the values of the additional impedances

5.4 Conversion Loss

Good simulation results concerning the conversion loss could be achieved in most cases by parameterizing the model through the reflection at the LO and RF port as described above. The conversion loss is calculated as the ratio at the IF port - over the 50Ω-resistor, see figure 9 - to the available RF input power

If the accuracy of the conversion loss is not sufficient, it can be optimized by varying L_{RF}, K_{RF}, R_{RF}, C_{RF}. By doing so, in most cases a compromise has to be found between the implementation either of RF reflection or conversion loss.

5.5 Isolation

In the last step the isolation is implemented. To calculate the values of the components in the isolation networks the whole model from figure 5 is connected as shown in **figure 10**.

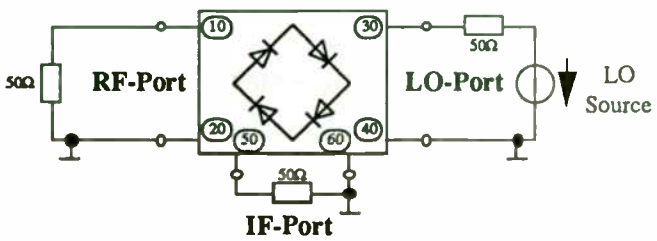

Figure 10 Simulation circuit to calculate the component values of the isolation networks

To simulate the LO-RF isolation the components C_{LORF}, L_{LORF}, R_{LORF1}, R_{LORF2} are used. The LO-IF isolation is given by the filter network consisting of C_{LOIF}, L_{LOIF}, R_{LOIF1}, R_{LOIF2}. The capacitors C_{LRBLK}, C_{LIBLK} serve as DC-decoupling existing in reality between the ports. They should be set to 1 Farad.

5.6 Re-Optimization

Like outlined in the strategy - see figure 6 - the model parameters will have to be re-optimized. This will be necessary at least after addition of the isolation networks Therefore all simulations must be repeated with the complete model. The characteristics can be improved by modifying the corresponding parameters. The user has to decide when the model accuracy is good enough.

In the following the achieved results are presented for the mixer SRA-1 from Mini-Circuits.

6 Simulation Results

For simulations, the model will be connected as shown in **figure 11**. The 50Ω-resistors in series to the sources represent the impedances of the generators. The IF port is also terminated by 50Ω. For stimulation, sources with sinusoidal waveform have to be taken. In the cases of LO reflection and isolation the RF source can be replaced by a DC source with DC value of 0. Transient analysis with frequency transformation afterwards were performed. The parameter values for the mixer SRA-1 from Mini-Circuits are listed in **table 1**.

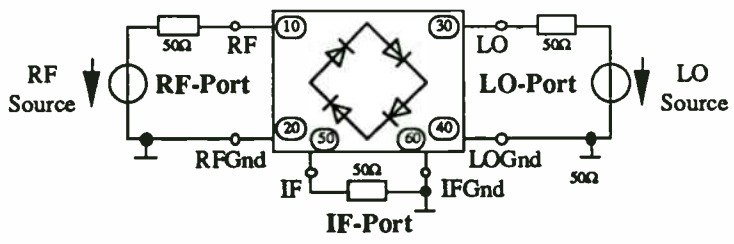

Figure 11 Circuit to simulate the model for passive diode ring mixers

L_{LO}=4.080uH	L_{RF}=11.61uH	Is= 73.5uA	C_{LORF}= 400fF	C_{LOIF}= 258fF
K_{LO}=0.998041	K_{RF}=0.999067	N= 3.42	R_{LORF2}=1.5kΩ	R_{LOIF2}=1kΩ
C_{LO}=1.000pF	C_{RF}=3.106pF	Rs=0.0Ω	R_{LORF1}=15kΩ	R_{LOIF1}=10kΩ
R_{LO}=1uΩ	R_{RF}=188Ω		L_{LORF}= 13.67mH	L_{LOIF}= 1H
			C_{LRBLK}=1F	C_{LIBLK}=1F

Table 1 Values for model parameters (Mixer SRA-1 from Mini-Circuits)

6.1 Conversion Loss and Compression

The conversion loss is documented in **figure 12**. Please note that an offset of 2 dB and 4 dB was added to the data in the cases of 7 dBm and 10 dBm LO power respectively.

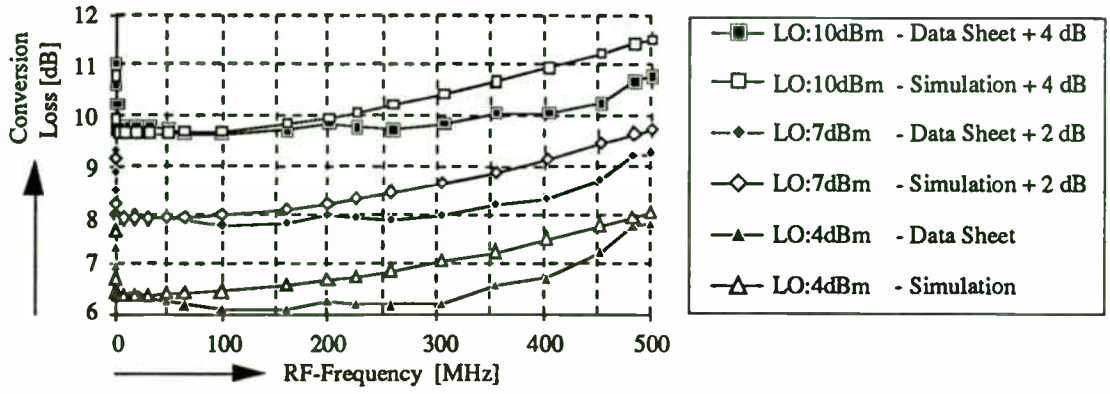

Figure 12 Simulated conversion loss (Mixer SRA-1 from Mini-Circuits)

To the 1dB-compression-point no information exists in detail in the data sheets. Simulation and measurement show good matching (**figure 13**). Please note, that in the same way as above, an offset of 2 dB was added to the traces for 10 MHz RF frequency. The measurement set-up is shown in **figure 14**.

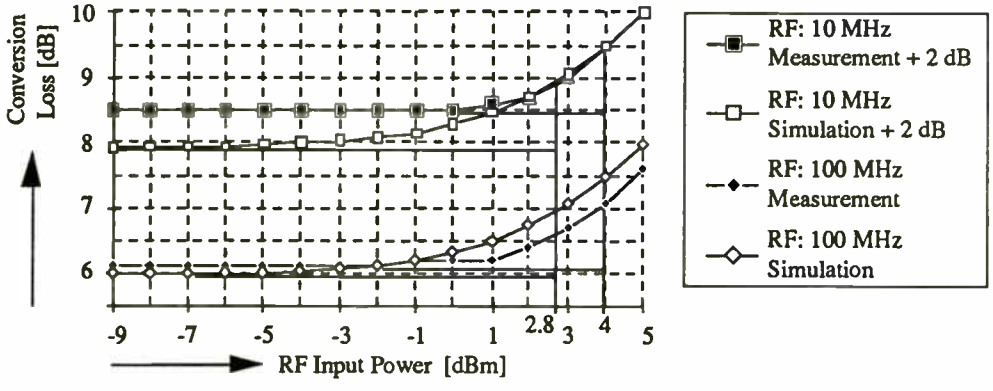

Figure 13 Simulated and measured conversion loss to compute the 1dB-compression-point (Mixer SRA-1 from Mini-Circuits)

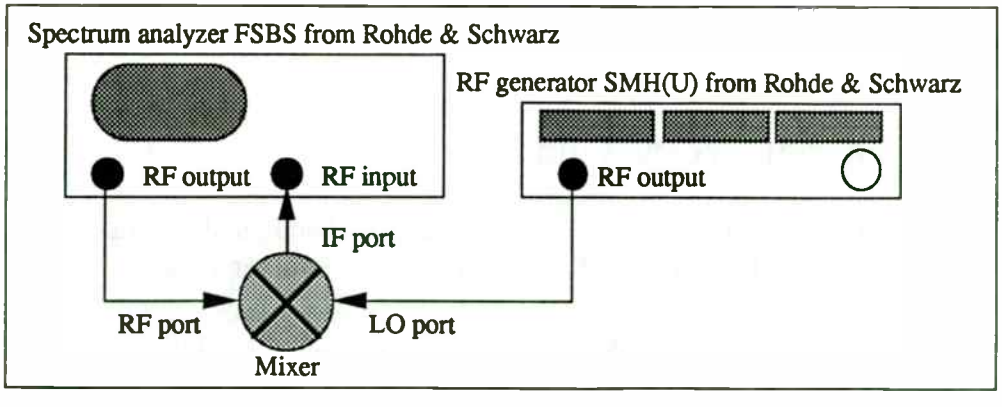

Figure 14 Set-up to measure conversion loss and 1dB-compression-point

6.2 Reflection and Isolation

The behavior of the model concerning the reflection at RF and LO port is shown in **figure 15**.

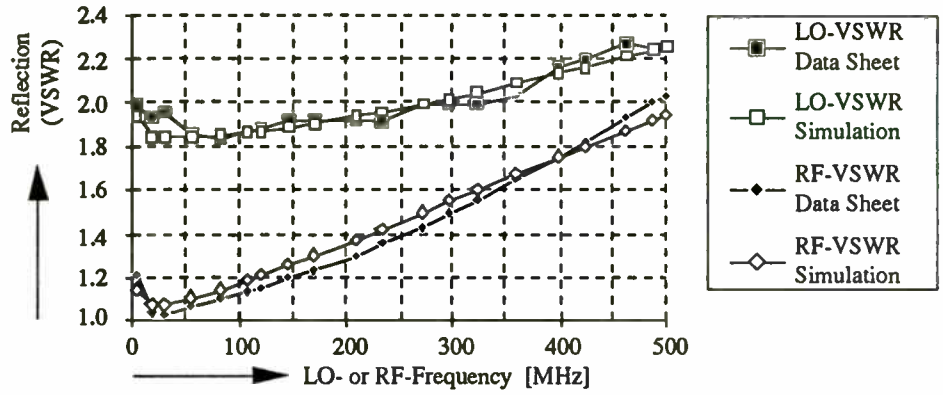

Figure 15 Simulated reflection at LO and RF port (Mixer SRA-1 from Mini-Circuits)

The isolation between the LO and the RF or IF port respectively is implemented by separate passive networks. Simulation results are displayed in **figure 16**. As done in some cases above, the data for the isolation LO-RF was increased by 10 dB.

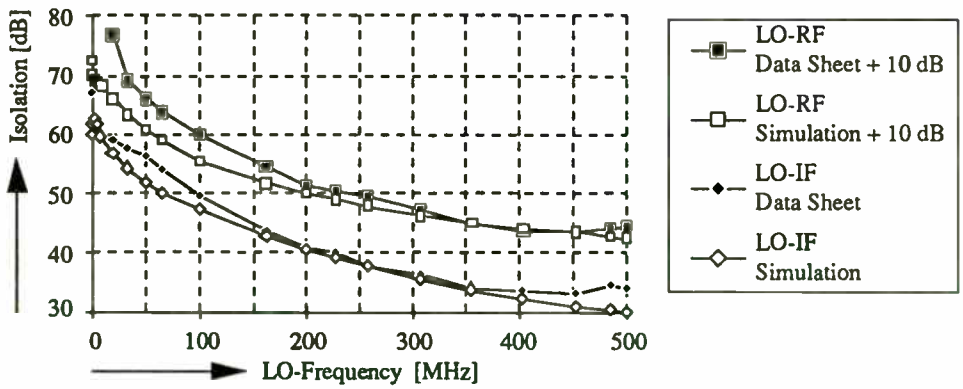

Figure 16 Simulated isolation LO-RF and LO-IF (Mixer SRA-1 from Mini-Circuits)

6.3 Third-Order-Intercept-Point

For the Third-Order-Intercept-Point (IP3) no details are listed in the data sheets by the manufacturer. Therefore in **figure 17** the behavior of the mixer model is compared to measurements taken from the real device. The simulation shows good agreement to measurement. It must be mentioned however, that the simulation results deviate from the measured values at the 3rd order term noticeable, when testing at RF frequencies higher than 200 MHz. The differences between simulation and measurement are about 10 dB typically.

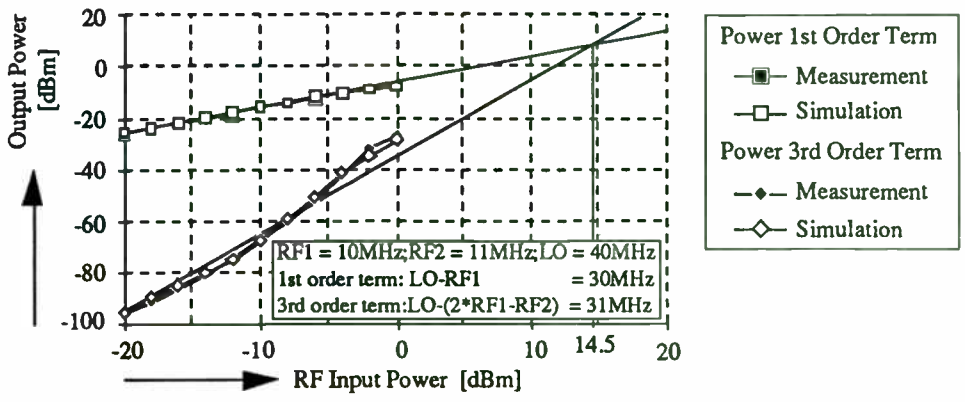

Figure 17 Simulated and measured intermodulation performance (Mixer SRA-1 from Mini-Circuits)

7 Conclusion

This paper presented a model for passive diode ring mixers. The model is based on the network simulator SPICE-2G6. The most important mixer characteristics like conversion loss, reflection and isolation are implemented. By a suitable choice of the device values the model can be adapted to any type of a passive diode ring mixer. Nonlinear effects like compression or intermodulation are reproduced with acceptable accuracy. The achieved results were presented for the mixer SRA-1 from Mini-Circuits.

8 Acknowledgement

This work was carried out as part of a joint research project called "A Library for Complex Analog Devices" funded by the Federal German Ministry of Research and Technology (BMFT).

The authors wish to thank Mr. Kremp for his work on implementing the model and the strategy for parameterizing into the Microwave Design System (MDS). Furthermore they wish to thank Mr. Korte for programing a software tool for automatic mixer measurements.

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Simulating Short Duration Electrostatic Discharge Events in a Printed Circuit Board Using the Finite Element Time Domain Technique

by
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Abstract—Short duration electrostatic discharge (ESD) events in a prescribed circuit board configuration are simulated using multi–dimensional finite elements in the time domain. ESD from a charged human through a printed circuit board is simulated in which circuit elements representing a charged human are connected to a conventional finite element model representing a printed circuit board. The impact of discharging the source over a contact area versus a single point contact is quantified.

INTRODUCTION

Electrostatic discharge processes through circuit boards or other devices are difficult to predict due to their complicated geometries and surrounding materials. Electrostatic discharge is typically predicted through either highly approximate formulas, or through measurements which are often difficult to reproduce.

The finite element method can inherently analyze complicated geometries, and thus one might expect it to be universally used to predict the electrostatic discharge process. To the author's knowledge however, the finite element method has not yet been applied to simulate an ESD process. Reasons for why the finite element technique is sparingly applied to simulating ESD may be attributed to difficulties in modeling complex three–dimensional geometries, the transient nature of the ESD process, and difficulties in accounting for the effects produced by the finite impedance of the discharging source.

In the present study, the finite element method is applied to simulating a transient ESD response through a three dimensional printed circuit board. The simulation is performed in the time domain and includes the use mixed–dimensional finite elements to account for the interaction between the human discharging source and the printed circuit board, and to simulate infinitely thin traces mounted on the circuit board which carry discharge currents. Results are shown which quantify the impact of different grounding strategies on discharge voltage waveforms.

THEORY OF FINITE ELEMENT SOLUTION TO MAXWELL'S EQUATIONS

The variation of electromagnetic energy can be expressed as [1]

$$\delta w = \int_{vol} dv \left\{\delta w_{el} + \delta w_{mag} + \delta w_{loss} - \delta w_{in}\right\}$$
$$+ \int_{surf} ds \int_{t_o} dt\left\{\delta\vec{A} \cdot (\vec{H} \times \hat{n}) \quad - \delta\psi\left[(\hat{n} \cdot (\vec{J} + \dot{\vec{D}})\right]\right\} + \left[\int_{surf} ds\, \delta\psi \left(\hat{n} \cdot \vec{D}\right)\right]_{t=t_0} = 0 \qquad (1)$$

where the only unusual variable is ψ, the time integral of electric scalar potential (in volt–seconds). Setting the variation of (1) to zero and performing the volume and surface integrals over finite elements gives the dynamic equation [1]

$$[M]\{\ddot{u}\} + [B]\{\dot{u}\} + [K]\{u\} = \{P\} \qquad (2)$$

where the [M], [B], and [K] matrices are proportional to permittivity, conductivity, and reluctivity, respectively. For linear simulations, material properties are assumed to be constant. The unknown column vector {u} is comprised of the scalar quantity ψ, and the vector quantity $\overline{A}$ at the nodes of finite elements. The right hand side {P} vector contains the excitations. Equation (2) satisfies all of Maxwell's equations in frequency or time domain problems using MSC/EMAS™ [1].

Equation (2) can be solved in the time domain using a variation of the Newmark Beta method [2]. The time derivatives of the unknown column vector {u} are replaced by discrete time differences yielding:

$$\left(\frac{1}{\Delta t^2}[M] + \frac{1}{2\Delta t}[B] + \beta[K]\right)\{u\}_{n+2} = \begin{cases} \left(\beta\{P\}_{n+2} + (1-2\beta)\{P\}_{n+1} + \beta\{P\}_n\right) \\ + \left(\frac{2}{\Delta t^2}[M]-(1-2\beta)[K]\right)\{u\}_{n+1} \\ + \left(\frac{-1}{\Delta t^2}[M] + \frac{1}{2\Delta t}[B]-\beta[K]\right)\{u\}_n \end{cases} \qquad (3)$$

For unconditional stability, the potentials are evaluated using $\beta \geq 1/4$.

Initial voltages at t=0 may be provided by specifying $\dot{\psi}$ in the following substitution [2]

$$\{P_0\} = [K]\{u_0\} + [B]\{\dot{u}_0\} \qquad (4)$$

MATRIX CONTRIBUTIONS OF MIXED DIMENSIONAL FINITE ELEMENTS

The [M], [B], and [K] matrices of Eqs. (2) – (4) are built up of contributions from individual finite elements. The finite elements can be of various dimensions and intermixed in the same finite element model using the theory discussed below.

The [M], [B], and [K] matrix entries for one, two, and three dimensional elements are three dimensional integrals over the entire element volume for A and ψ. The matrix contribution of each element is proportional to:

$$\int_{vol} dx\ dy\ dz\ f(x,y,z) \qquad (5)$$

where f(x,y,z) is related to element shape functions and their spatial derivatives. For the lower two dimensional elements, potentials and shape functions are assumed to be independent of position through the element thickness leading to an integral proportional to:

$$t \int_{surf} dx\ dy\ f(x, y) \tag{6}$$

where f(x,y) is the two dimensional shape function in its local xy plane, z is the direction normal to the element, and t is the element thickness in the z direction. The assumptions in Equation 6 enable the matrix entries for 3D, 2D, and 1D elements to have the same units and degrees of freedom, allowing all of these elements to be intermixed in one finite element model [3].

Zero dimensional finite elements attached only to the ψ degrees of freedom of the [M], [B], and [K] matrices can represent capacitors, resistors, and inductors, respectively [4]. Each of these elements has only two nodes. The capacitor C, resistor R, and inductor L elements contribute to the matrices of Eqs. (2) – (4) as respectively shown below:

$$[M] = C\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \qquad [B] = (1/R)\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \qquad [K] = (1/L)\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{7}$$

Substituting Equations (7) into Equation (2) gives two identical equations of the type:

$$C\frac{\partial V}{\partial t} + V/R + (1/L)\int Vdt = I \tag{8}$$

where V is the difference between $\partial\psi/\partial t$ at the two nodes. The significance of Eq. (8) is twofold. First, Eq. 8 is the familiar equation of electric circuits enabling the zero dimensional finite element formulation to agree with classical electric circuit theory. Second, Eq. 8 describes the link which provides the the ability to successfully intermix lumped circuit elements and conventional finite elements in a single analysis.

SIMULATION OF ELECTROSTATIC DISCHARGE

Figure 1 illustrates a view of the printed circuit board assembly. Each infinitely thin strip is modeled using two–dimensional finite elements which are sandwiched between conventional three–dimensional finite elements simulating the surrounding air and substrate material. The input and output impedance of each strip is set to 50 Ω using zero–dimensional resistor finite elements attached to the strip grids at the model boundaries. Two different electrostatic discharge events are simulated in the assembly described above. In the first case, human contact with the model occurs at a single, infinitesimally small point. The second condition simulates realistic contact area between the human discharging source and the device.

Transient voltage discharge is quantified through the model for the two aforementioned excitations. The finite element models used in the simulations contain approximately 2100 elements, 7,500 grids and 23,500 unknowns.

Figure 2 illustrates the equivalent circuit of a human which acts as the discharging source in this simulation. This equivalent circuit of the human is coupled to the conventional finite element model of the printed circuit board by making the output node of this circuit a grid on the input of a trace of the printed circuit board assembly. To represent realistic contact between the human and circuit board, the circuit output can be distributed, or fanned out, over an area near the point of contact. To accomplish this task, multiple point constraint techniques are employed which equate the potentials on a series of grids adjacent to and at the point of contact as shown in Figure 3.

An initial condition is used on the circuit to represent a human charged to 3000 Volts as shown in Figure 2. This initial condition supplies the only excitation required for the analysis performed here. To capture the detail at the beginning of the discharge process, the transient analysis is performed using a Δt of 1 picoseconds (ps) from 0 to 100 ps. The remainder of the simulation is carried out to 100 ns using a Δt of 1 ns.

Figure 4 illustrates the voltage waveforms as a function of time on both the input and output of trace 1. Note that the trace current takes approximately 9 ps. to reach the end of the trace. Figure 5 shows the difference created by the two different human contact conditions on trace 2 voltages. Note that the single point contact induces 31V whereas the area contact produces 130V on trace 2. Contour plots illustrating the conduction current density in the traces and ground plane are shown in Figure 6 for the two human contact conditions.

For finite element simulations, the voltage waveforms induced on a device are highly dependent upon discharging device geometry and materials, equivalent circuit configuration of the discharging source, and the contact area between the device and source. In the analysis performed here, the discharge waveforms display expected behavior and are in good agreement with typical over–damped discharge waveforms [5].

CONCLUSIONS

In this paper, the finite element technique has been employed using mixed–dimensional elements to simulate an electrostatic discharge process. Results produced by the finite element simulation can be used to locate discharge paths, quantify induced voltage waveforms, and assess the effects created by finite–sized contact areas between the discharging source and the device.

FIGURES

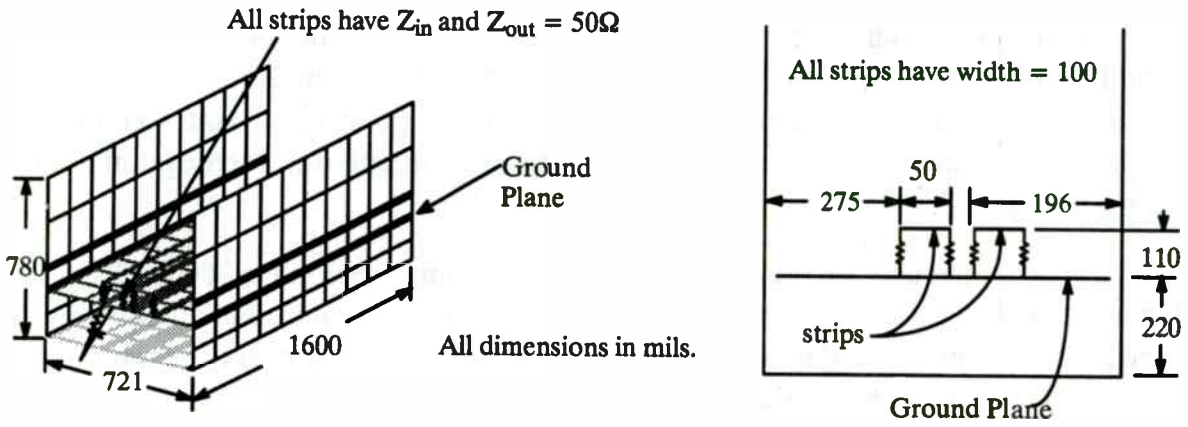


FIGURE 1. The printed circuit board assembly.

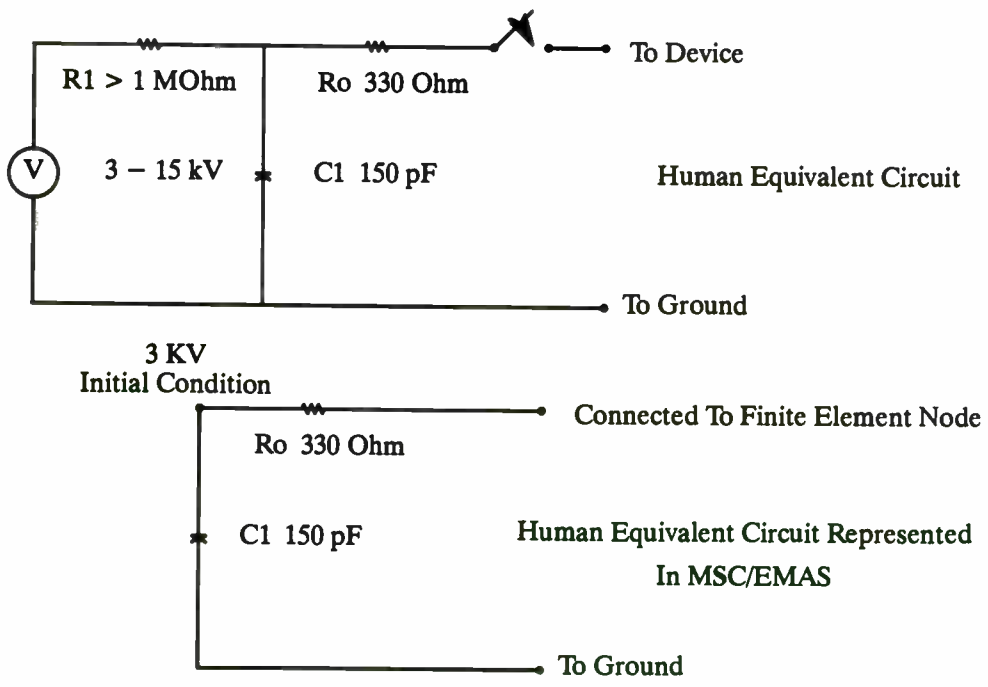


FIGURE 2. Lumped element equivalent circuit representing a human discharging source.

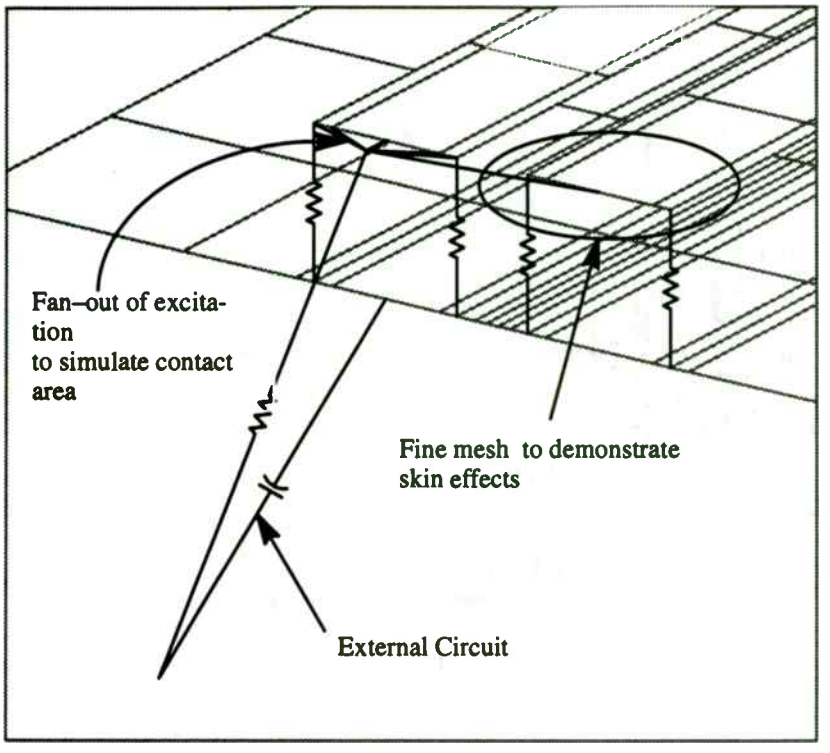


FIGURE 3. The connection between the lumped element circuit of Figure 2 and the printed circuit board finite element model accounting for a finite sized contact area between the human and circuit board

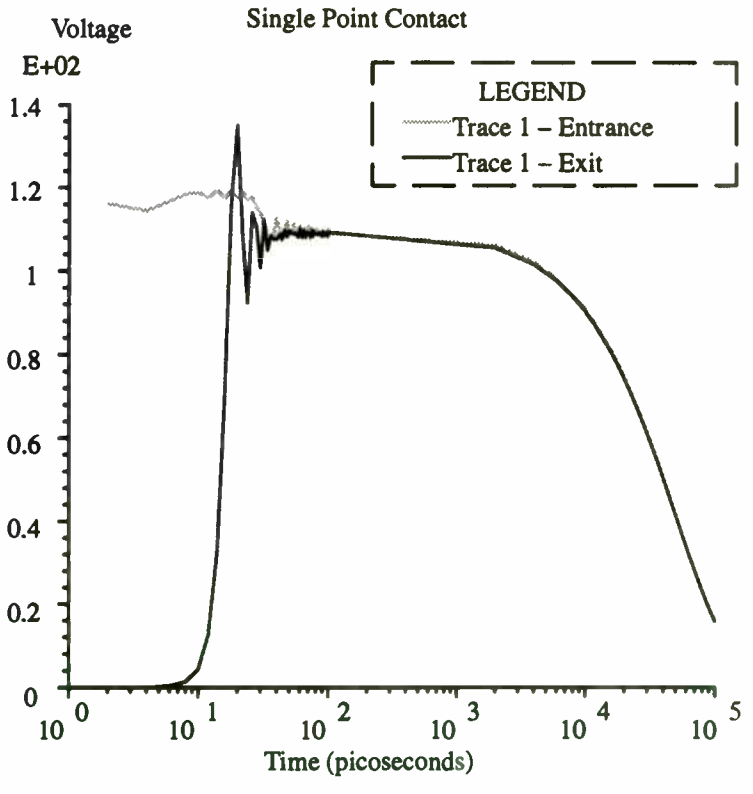


FIGURE 4. Voltage waveform of the discharge in trace 1.

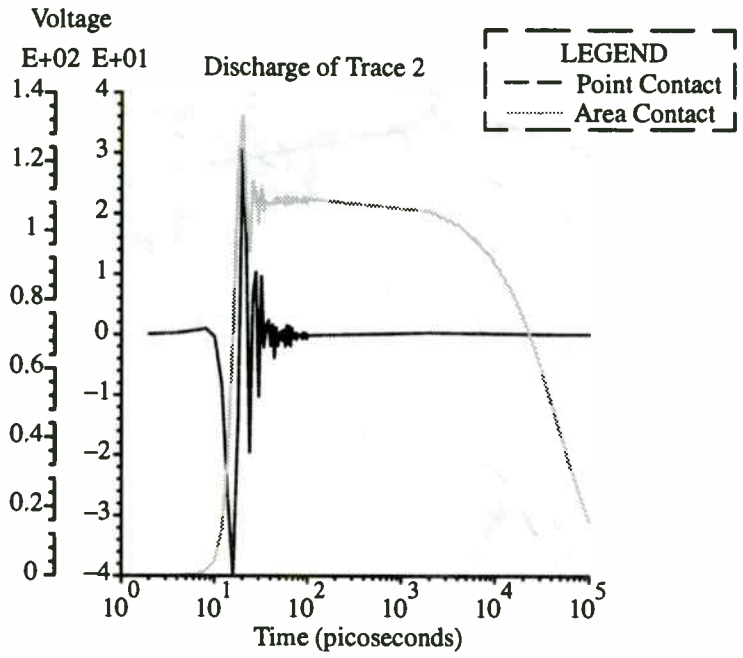
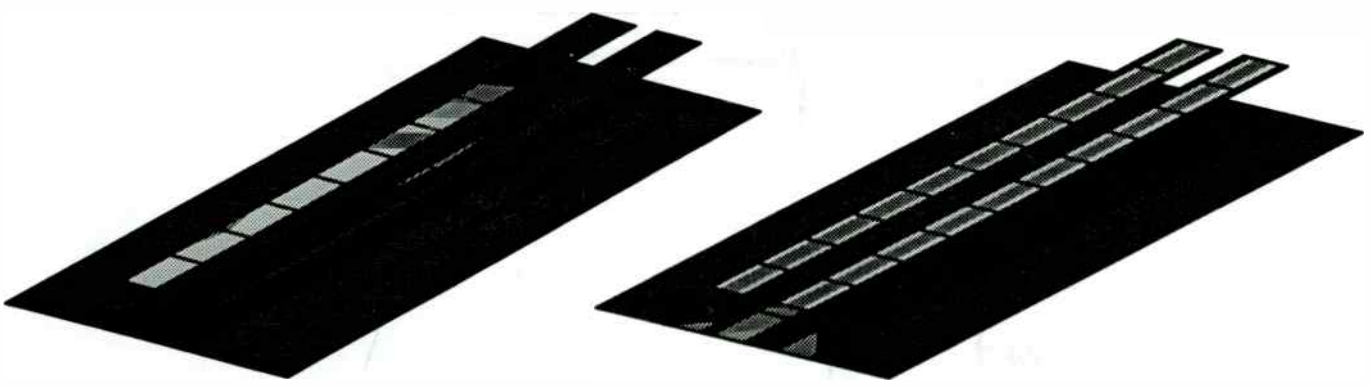


FIGURE 5. Voltages present in trace two illustrating the effect of single point versus area contact discharge.



Single Point Excitation

Contact Area Excitation

FIGURE 6. Conduction current density contours in the conducting members of the circuit board assembly illustrating the impact of different human contact configurations.

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CAD of LNAs for DBS Applications from Statistical Modeling of Pseudomorphic HEMTs

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Abstract

Conventional and pseudomorphic high electron mobility transistors (HEMTs and pHEMTs) have demonstrated excellent features in the design of the low-noise stages involved in communication systems due to their high gain and very low noise figure.

An original modeling procedure is here described which provides a detailed and reliable description of the transistor performance. By simultaneously fitting the scattering and noise parameter sets, the statistical noisy models of different device series in packaged form are extracted.

The model reliability is then tested in CAD applications by designing the low-noise module of a 12-16 GHz DBS system and evaluating the performance spreads in the whole amplifier frequency band.

I. Introduction

The design of communication systems, expecially those dealing with very small signal levels (such as DBS systems), requires to fulfill very tight specifications in terms of the trade-off between noise and gain. Significant progress has been made by using active devices with excellent noise and gain properties due to their physical structure, such as HEMTs and pHEMTs.

The accurate computer-aided design of the low-noise stages of DBS systems is based on a very detailed representation of the transistor noise and small-signal performance by means of an equivalent circuit model. To this aim, a very accurate and reliable modeling procedure has to be employed.

All the conventional modeling techniques for HEMTs and pHEMTs are based on the extraction of the small-signal equivalent circuit from the measured scattering parameters vs frequency and a few additional DC measurements. The noise performance is then predicted by simple models which fit the measured minimum noise figure only, in a given frequency range.

In this way, the strong correlation between the noise and gain features is not taken into account, since different noise models can reproduce the same values of the minimum noise figure while the other noise parameters (namely, the optimum source reflection coefficient and noise resistance) show remarkable differences.

Our original modeling procedure is based on the simultaneous fitting of the measured noise and scattering parameter sets, thereby providing a unique description of the device noisy properties.

This procedure is supported by a well-assessed measuring methodology, developed in our Laboratory, which allows the simultaneous determination of the scattering, noise, and gain parameters of a transistor with high accuracy. All these parameters are obtained using a noise figure measuring set-up only, since they are derived from noise figure measurements vs source reflection coefficient through proper data processing techniques [1].

Starting with the complete characterization of several devices of the same series, we extract the noisy circuit model of the typical device, thus giving a statistical significance to the modeling procedure.

As a result, we report the circuit model of the CFB001-03 series (by Celeritek) of packaged pHEMTs in the 8-16 GHz band employed in the design of a low-noise amplifier (LNA). The amplifier topology is optimized with respect to the model performance. Subsequently, we evaluate the spreading of the LNA performance when realized with each sample of the measured set.

II. Modeling procedure

We represent the transistor performance by means of a circuit model whose parameters fit all the measured data (i.e. both the scattering and noise parameter sets). This model is oriented at CAD applications, therefore it is not predictive from the manufacturing process viewpoint.

For packaged devices, we carry out the model topology building on the basis of the well-known chip circuit and subsequently add the elements of the parasitic package network. These elements are determined by accomplishing a preliminary analysis of the correlation between the measured data and the model topology. By giving a statistical significance to the model extraction, the circuit element values are obtained by assuming as objective functions of the optimization process the measured parameter spreads relevant to a device family.

State-of-the-art software packages for microwave circuit optimization provide excellent results if only a small number of goal functions is considered. Therefore, they are very suitable for modeling HEMTs and pHEMTs in terms of scattering parameters only.

If the four noise parameters are to be considered too, the convergency of the optimization routines is strongly compromised, since the mutual influence of the high number of weight functions (associated to the goal functions) is not controllable, expecially in a wide frequency range.

A suitable approach followed in large-scale circuit optimization is based on the element decomposition into subsets, each remarkably affecting only one parameter. By using a decomposition technique a complete partition of the circuit elements can be obtained if the interdependency analysis involves the scattering parameters only. In our case, by considering the global noisy behavior the decomposition can not be complete since the correlations existing between the scattering and noise parameter sets make some circuit elements strongly affecting more than one parameter.

Our software-assisted procedure is based on a sensitivity analysis on the measurement-derived topology. The results of this analysis, arranged in a matrix form, allow the model decomposition into different sections and, consequently, the optimization subdivision into separate cycles, which assures the fast convergency of the modeling procedure.

All the modeling procedure steps are reported in the block diagram of Fig. 1.

III. Results

The described procedure has been employed to extract the noisy model of the typical device of different HEMT and pHEMT series [2,3].

In this paper, we report the model of the CFB001-03 series (by Celeritek) of packaged pHEMTs over the 8-16 GHz band (Fig. 2). The transistor noise source in the conducting channel is schematized by associating a noise temperature to the output resistor (R_{DS}) of the chip circuit. This noise model is the most suitable schematization for packaged devices since it is based on one fitting factor only (i.e. the noise temperature associated to R_{DS}) which determines the minimum noise figure, namely the only noise parameter not influenced by the impedance-transforming properties of the package.

The comparison between the measurement results (ten samples) and the model responses is shown in Fig. 3.

Once the modeling procedure has been completed, we test the effectiveness of this statistical model by showing that it represents with high accuracy the noise and gain performance of the entire device family in the design of a LNA.

In particular, we consider an amplifier operating over the 12-16 GHz band with the following requirements:

Gain = 11 dB ± 0.7 dB

Noise figure < 1.4 dB

Input/Output VSWR < 2.

These stringent specifications have been obtained by means of a preliminary analysis of the performance obtainable from the modeled transistor.

By using the model of the typical device, the LNA design is represented by the schematic layout shown in Fig. 4. When all the measured pHEMTs take place of the typical device, a very small spread occurs in the noise and gain performance, as shown in Fig. 5.

IV. Conclusions

An original statistical modeling procedure has been described aimed at the extraction of the noisy model of the typical device of an HEMT series completely characterized by means of a noise figure set-up only.

This model represents with good accuracy and reliability the performance of the entire measured family in CAD applications, as shown by the design of a LNA for DBS systems with stringent noise and gain specifications.

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[1] A. Caddemi, G. Martines, and M. Sannino, "Automatic characterization and modeling of microwave low-noise HEMT's", *IEEE Trans. Instrum. Meas.*, vol. 41, pp. 946-950, Dec. 1992.

[2] A. Caddemi, G. Martines, and M. Sannino, "HEMT for low noise microwaves: CAD-oriented modeling", *IEEE Trans. Microwave Theory and Tech.*, vol. 40, pp. 1441-1445, July 1992.

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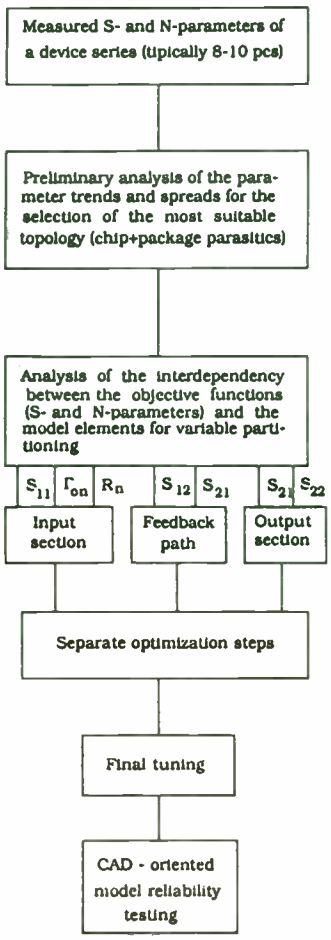


Fig. 1 - Block diagram of the modeling procedure.

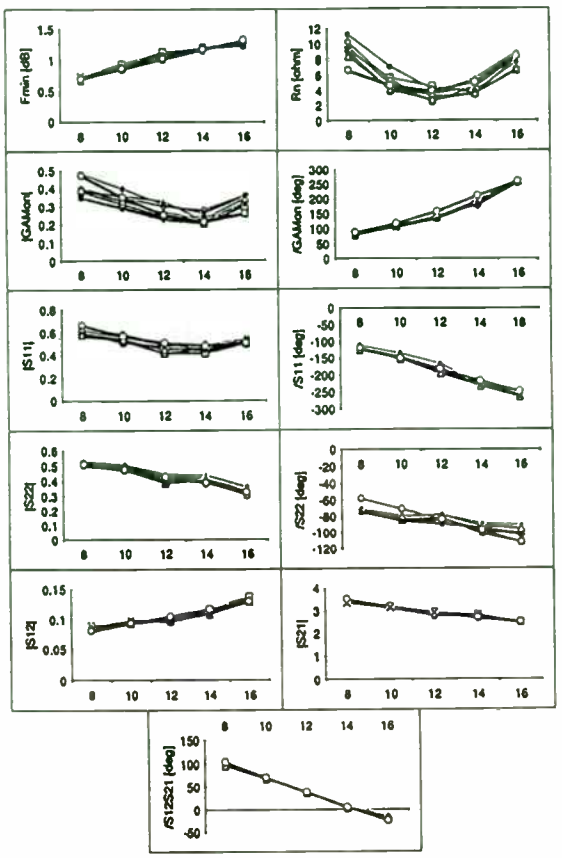
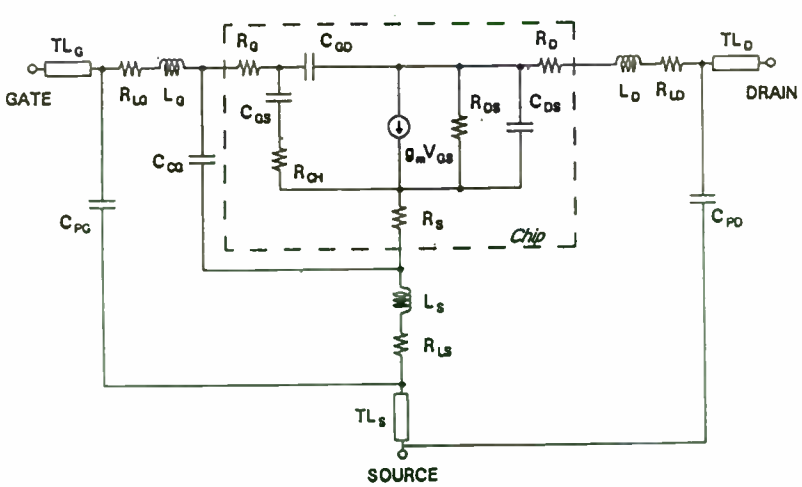


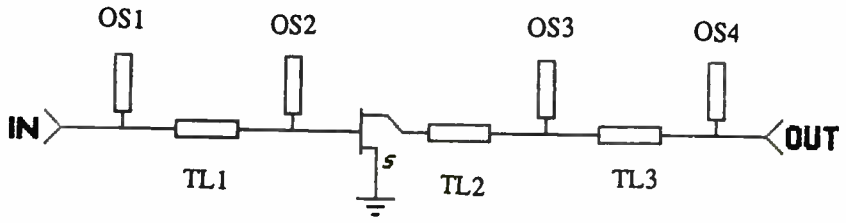
Fig. 3 - Comparison vs frequency between the measurement results and the model (bold) responses.



R_{LG}	= 0.3 ohm	R_D	= 1.5 ohm
L_G	= 0.47 nH	L_D	= 0.49 nH
R_G	= 2.2 ohm	R_{LD}	= 1 ohm
C_{CG}	= 0.03 pF	R_S	= 1.1 ohm
C_{PC}	= 0.06 pF	L_S	= 0.033 nH
C_{GS}	= 0.23 pF	R_{LS}	= 1.2 ohm
R_{CH}	= 1.4 ohm	R_{DS}	= 180 ohm
C_{GD}	= 0.023 pF	g_m	= 66 mS
C_{DS}	= 0.07 pF	τ	= 2.1 ps
TL_G	L= 840	TL_D	L= 280
TL_S	L= 500		

E = line physical lenght in microns @ 8GHz;
Z=50 ohm
All resistors are warmed @ 290 °K;
R_{DS} @ 3950 K

Fig. 2 - Circuit model of the CFB001-03 series of packaged pHEMTs (by Celeritek) over the 8-16 GHz range.



OS1:	E = 32	OS3:	E = 39
TL1:	E = 38	TL3:	E = 40
OS2:	E = 43	OS4:	E = 27
TL2:	E = 38	a	10 GHz
Z =	50 ohm		

Fig. 4 - Schematic layout of the LNA based on the typical pHEMT.

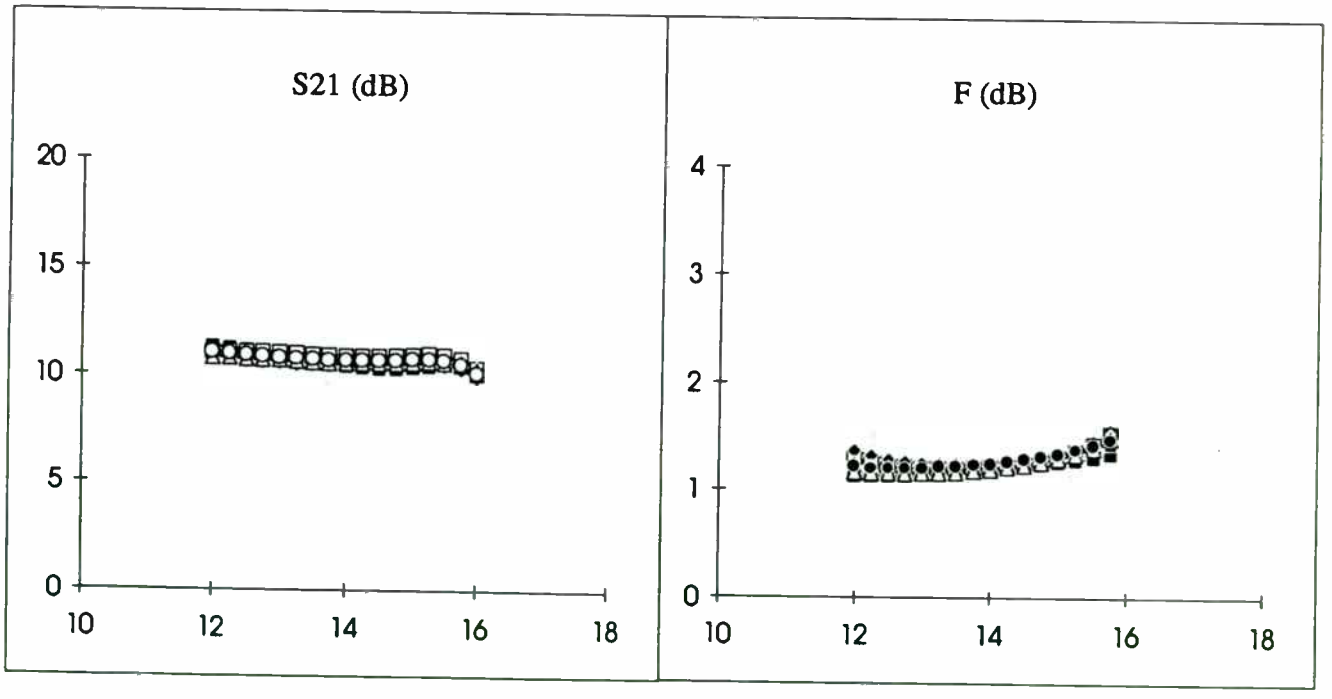


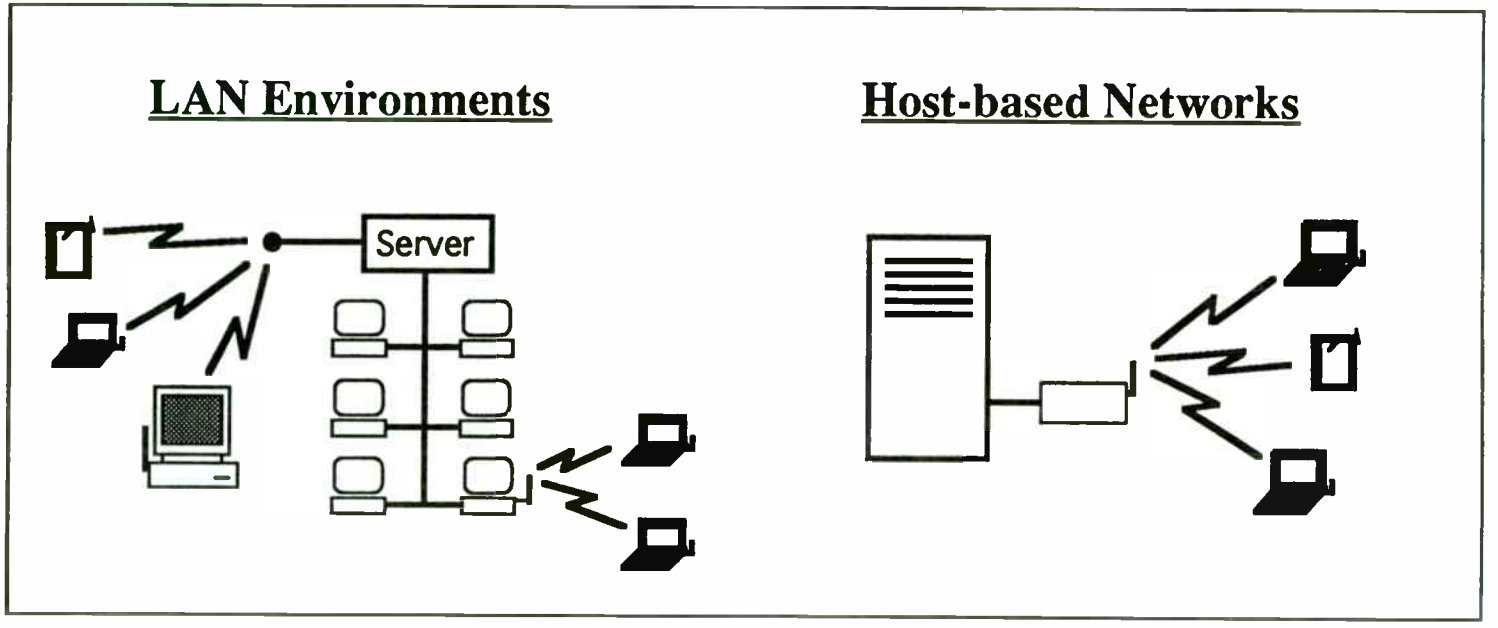
Fig. 5 - Noise and gain spread of the performances of the LNA produced by the measured pHEMTs.

Wireless Data Communications

Session Chairperson: Algis Juodikis,
Juodikis & Associates (Newport Beach, CA)

Proxim Mission and Markets

Mission: To become the leading provider of wireless local area data networking solutions for mobile computer users



WIRELESS LOCAL AREA NETWORKING

MACK SULLIVAN

DIRECTOR OF MARKETING

proxim

Proxim History

	Era 1	Era 2	Era 3
	Military RF Network Developer	Commercial OEM Spread Spectrum Supplier	Corporate Wireless LAN Pioneer
	1984-1988	1989 - Present	1992 - Present
Application Focus	Mobile inventory tracking system	Mobile data collection & telemmetry	Mobile LAN solutions
Target Market	U.S. Military	Handheld terminal device manufacturers	Notebook PC and PDA users
Product Lines	Network control units and RF tags (Intelligent Traveller)	OEM RF tranceivers and RS-232 modules (RXA, RDA, ProxLink)	Wireless LAN adapter families (RangeLAN, RangeLAN2)

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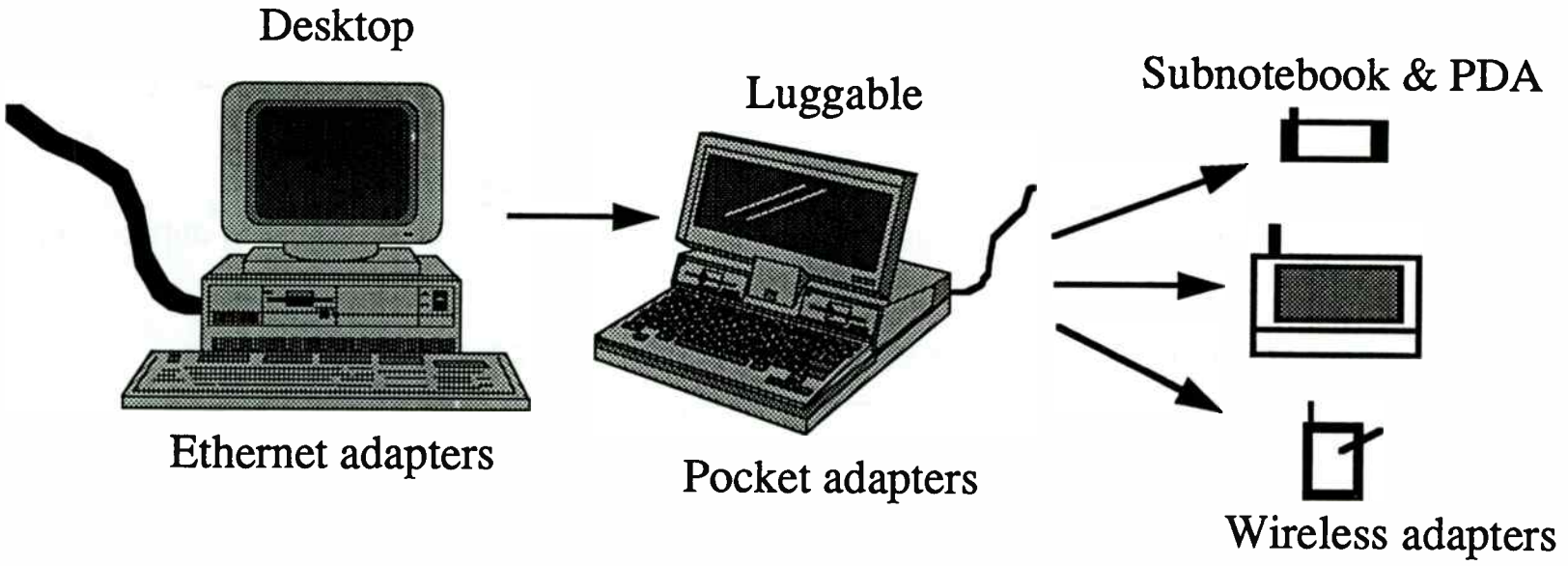
Data Communication Trends



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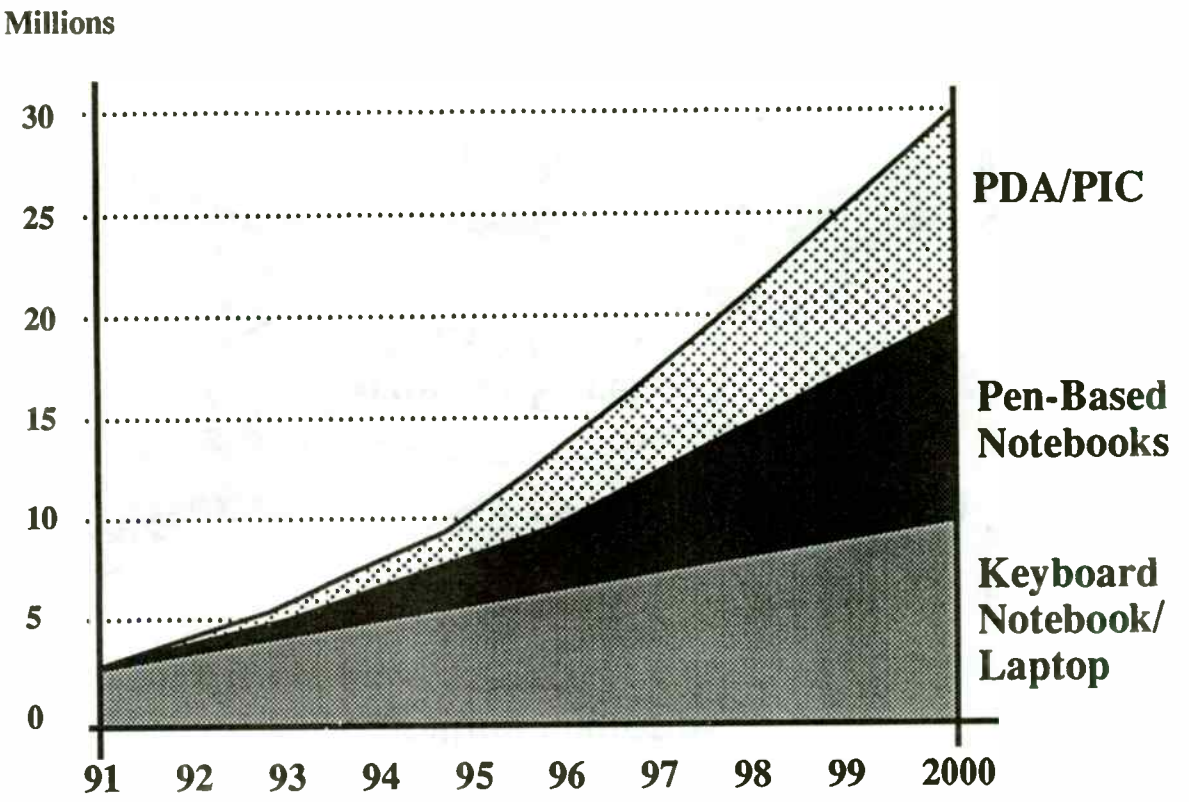
Installed Base of Mobile Computers



Source: Booz-Allen & Hamilton (3/92)

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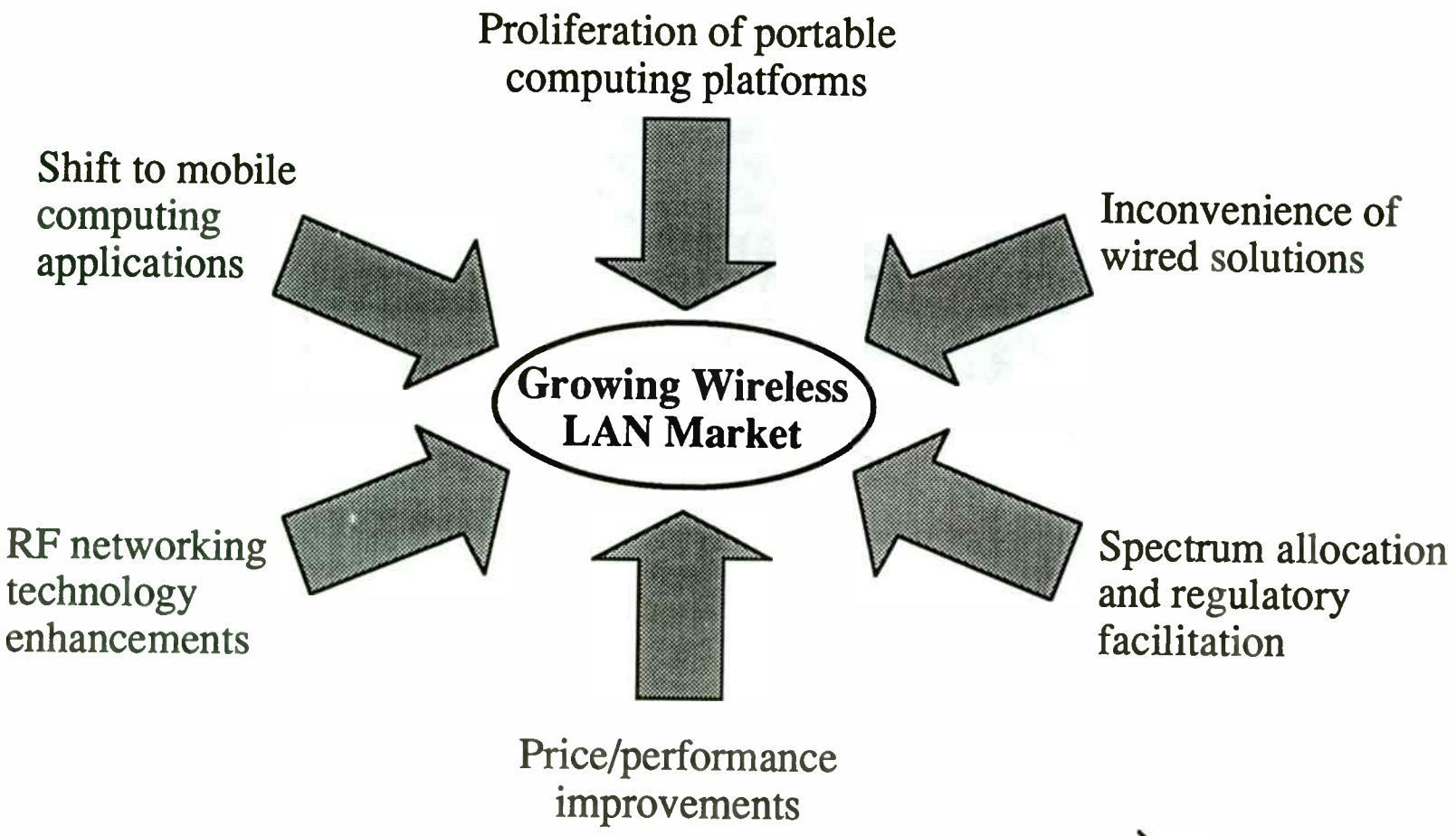
Key Forces at Work



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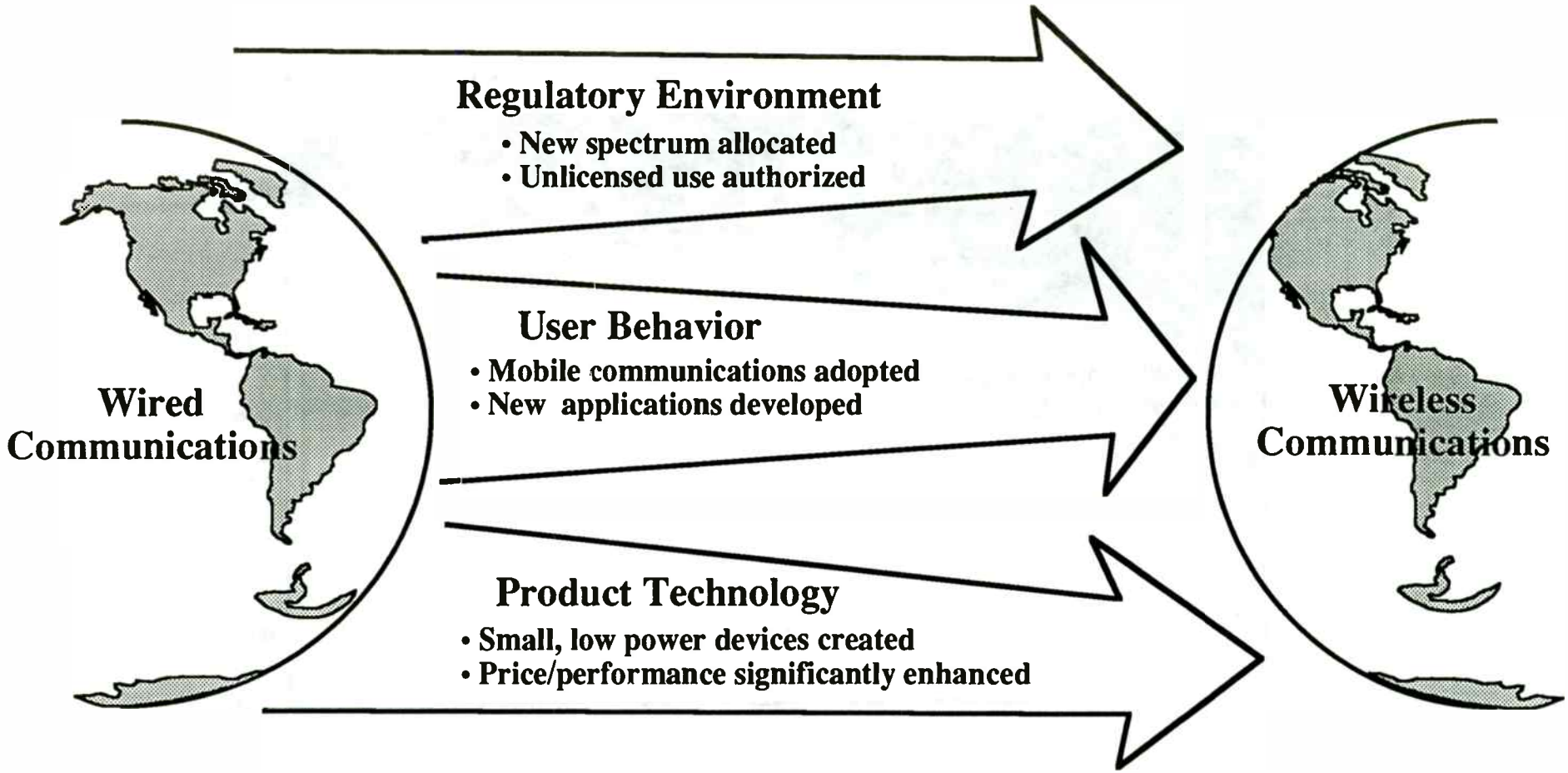
Paradigm Shift



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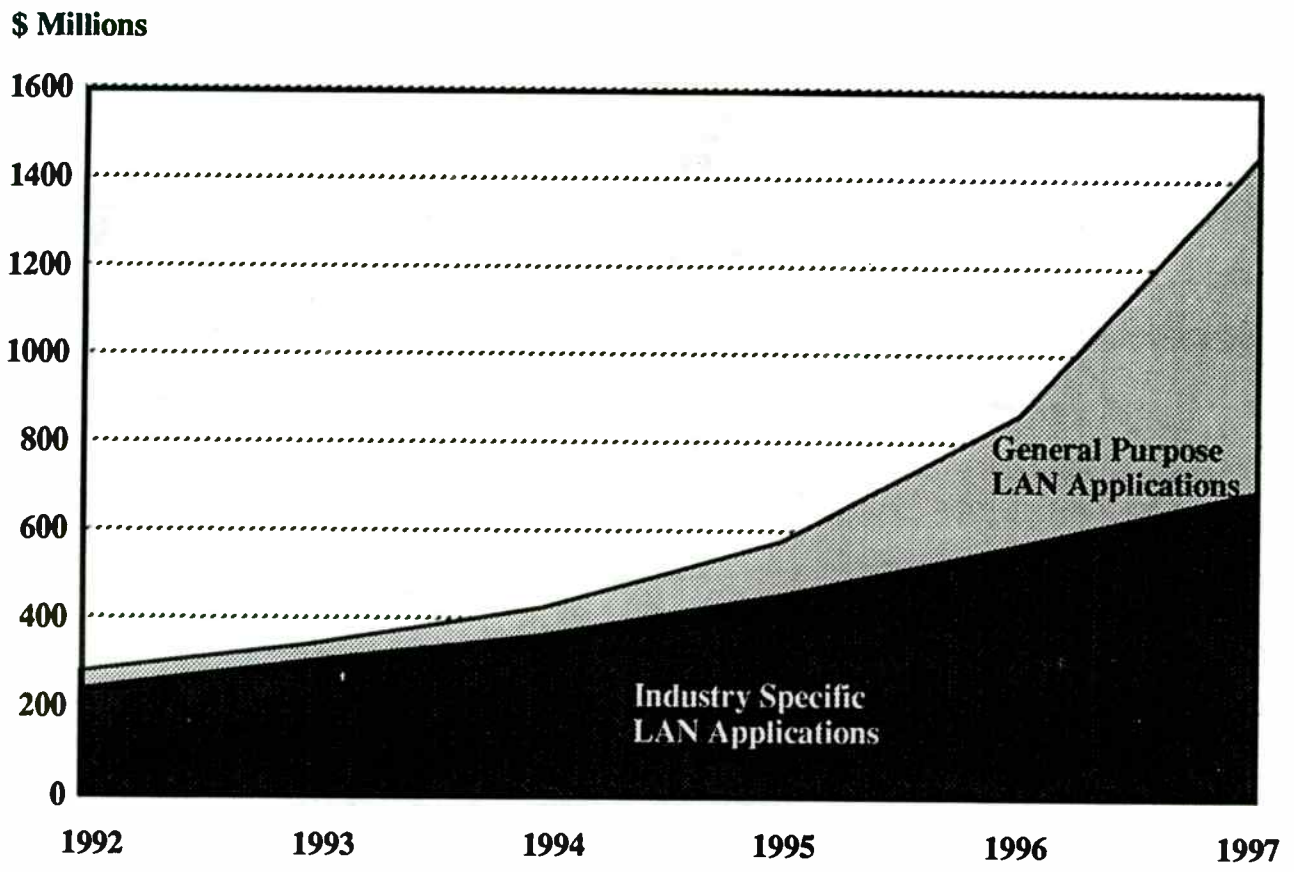
Wireless LAN Market Size



Source: Dataquest (10/93)

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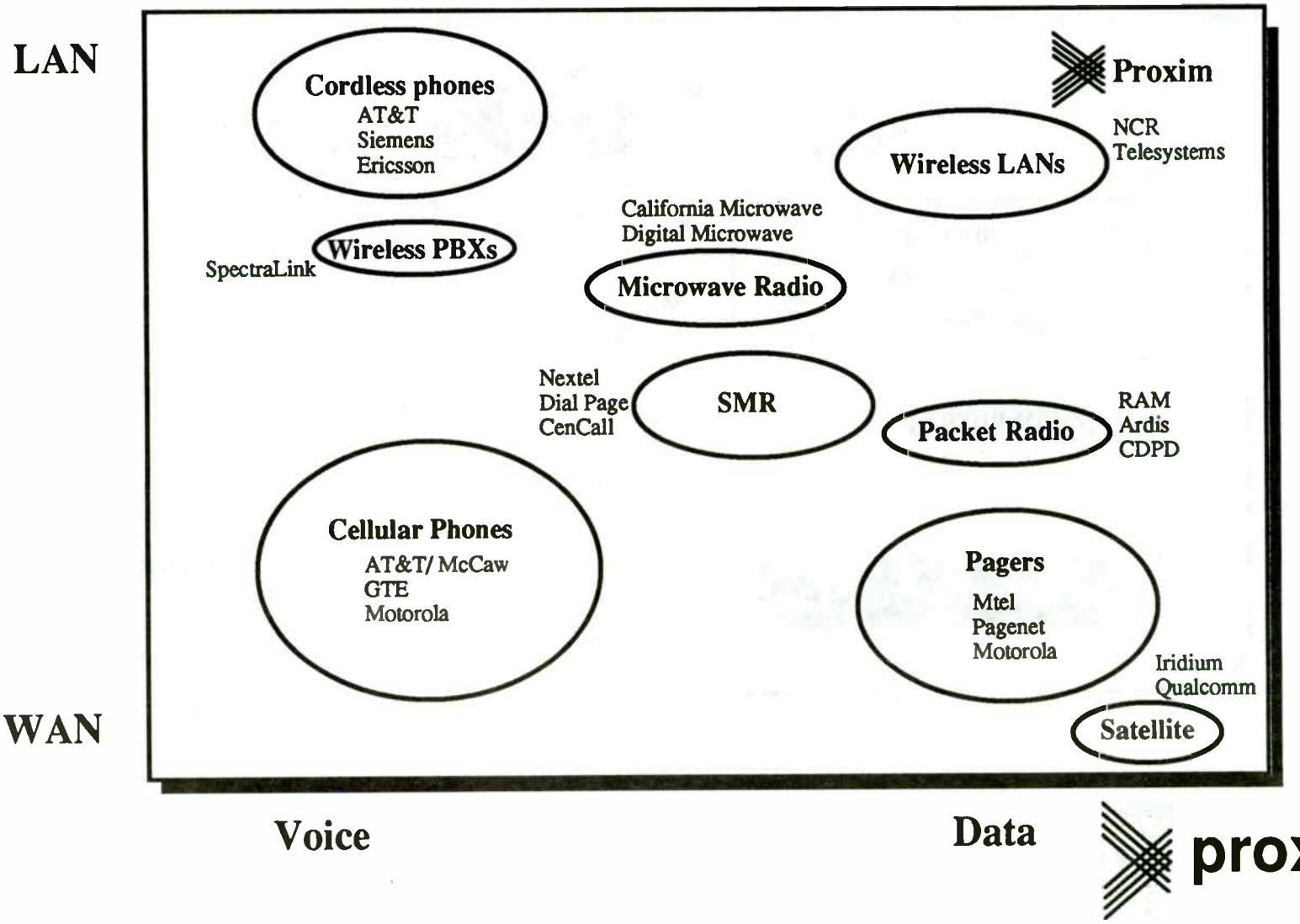
Wireless Landscape



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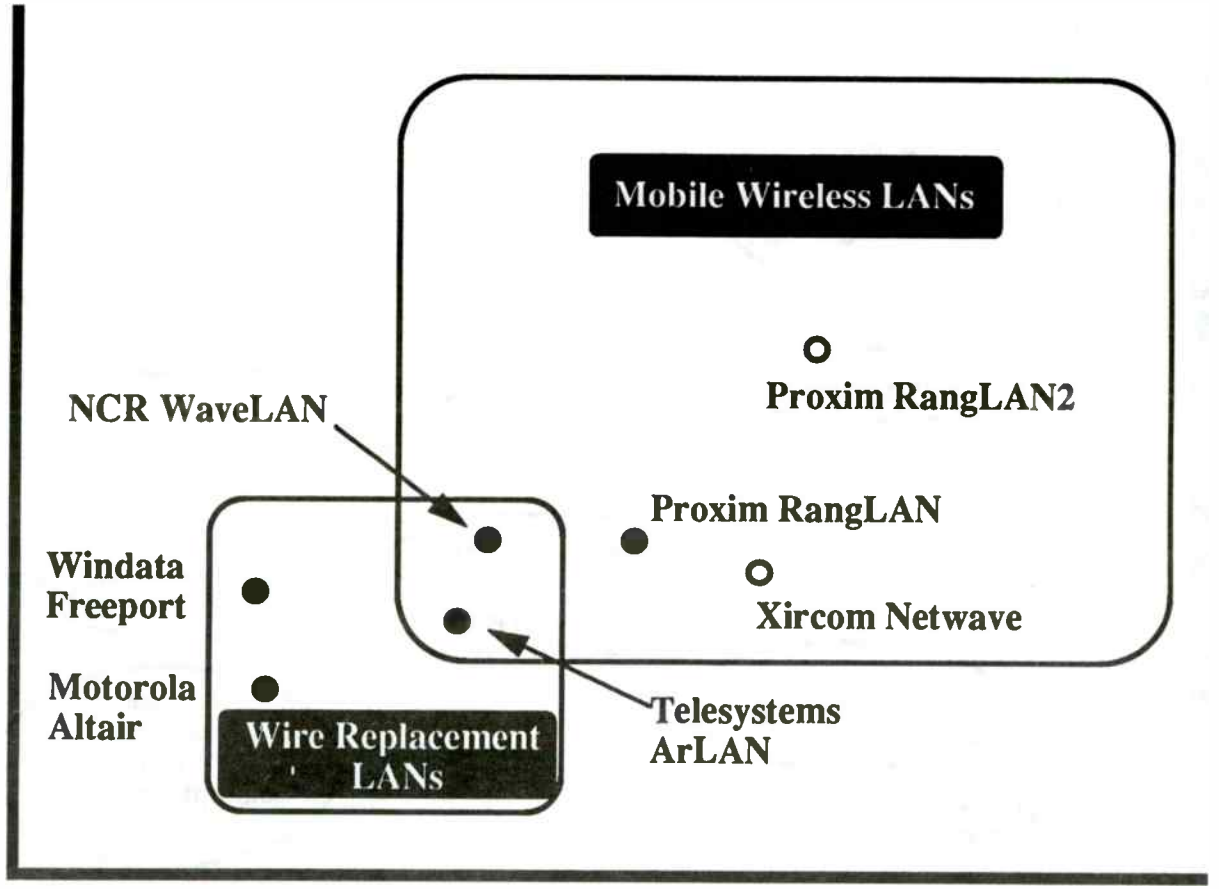
Wireless LAN Competition

Functionality
- Range
- Reliability
- Throughput
- Power Consumption



Scope of Usage

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Wireless LAN Technologies

	Advantages	Disadvantages
Spread Spectrum Radio	• Inherent noise-immunity and interference protection • Potential for higher data rates • No end user license required	• Secondary user vs. higher priority user
Licensed Narrowband Radio	• User given priority access in specific locations	• Requires individual license for each network location • Limited to sole or few suppliers
Infrared Light	• Potentially cheap, low functionality solution • No end user license required	• Cannot penetrate solid objects (i.e. glass and walls)

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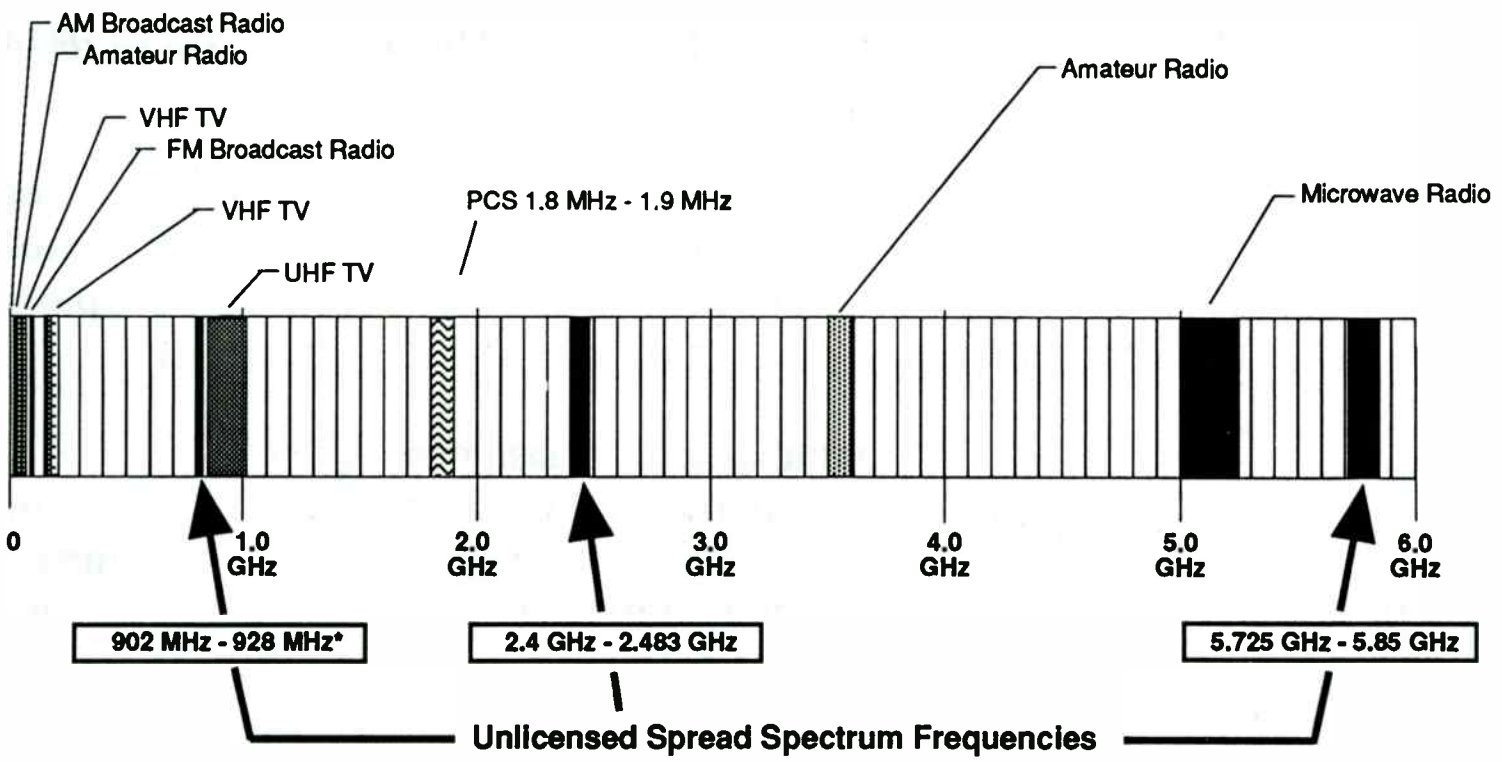
U.S. Wireless Spectrum



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Spread Spectrum

Attributes

- Three FCC-authorized frequency bands
- "Spreading" of scrambled encoded data across broad frequency band
- Limitation on power output (1 watt) and emissions

Advantages

- Noise resistant, interference immune transmissions
- High data rate and throughput potential
- Frequency reuse facilitated
- No end user license required

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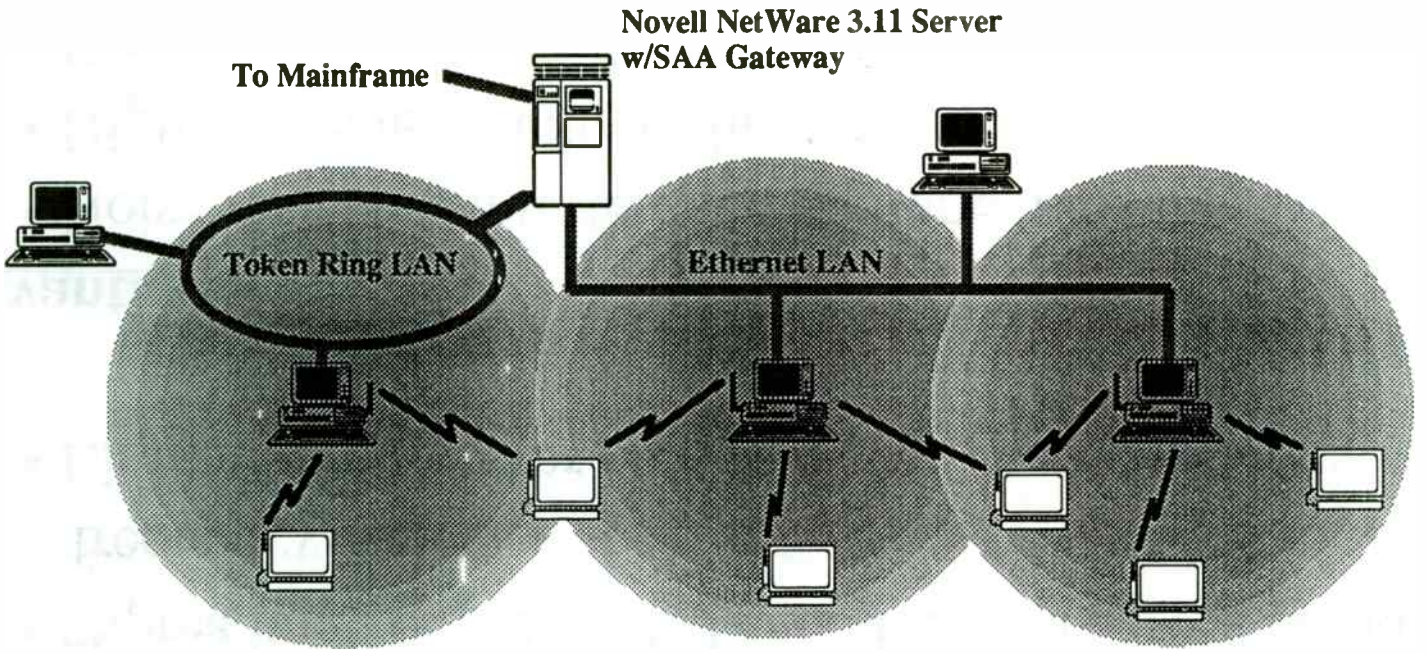
Wireless Protocol Expertise



- Multipath interference
- Hidden nodes
- Near/far problem
- Fair access
- Intermittent connection
- Overlapping networks
- Power management
- Seamless roaming

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Key Mobile Connectivity Technologies

- Robust long range radio architecture
- Highly minaturized analog/digital components
- Minimum power consumption
- Networking software designed for mobility

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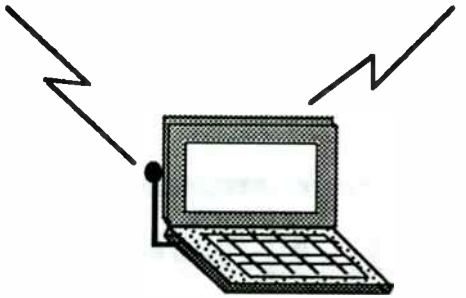
Mobile Applications/Markets

Horizontal Applications

- E-mail
- Printer sharing
- File transfer
- Terminal emulation

Vertical Markets

- Health care
- Manufacturing
- Retail/POS
- Professional services



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Leading Proxim OEMs

Customer	Application
Alps Electric	Printer Sharing
Comtec Information Systems	Distribution, Retailing
Fujitsu Personal Systems	Restaurants, Field Services
Granite Communications	Hotels, Restaurants, Financial Exchanges
GRiD Systems	Healthcare, Transportation, Retailing
Intermec	Retailing, Warehousing
John Fluke Manufacturing	Monitoring and Control Systems
Scientific Technologies	Factory Floor Automation
Teklogix	Inventory Control
Trimble Navigation	Surveying

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Case Study: USC Hospital

Customer: Large full service university hospital and trauma center

Application: Mobile E.R. admissions
Bedside data entry/access

Products used: RangeLAN/PCMCIA
RangeLAN/Roaming

proxim

Case Study: Simmons Mattress

Customer: Leading bedding products manufacturer

Application: Mobile inventory management

Products used: RXA-1000 RF tranceiver

Proxim partner: Intermec

proxim

Case Study: CSX Trucking

Customer: Large freight forwarding company

Application: Mobile freight inspection

Products used: MSU-500 RS-232 module

Proxim partner: Grid Computer

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Proxim Accomplishments

- Developed sophisticated RF transceiver and mobile wireless network architecture (1984-1988)
- Among first to ship commercial spread spectrum products (1989)
- Established substantial OEM business with handheld computer and terminal manufacturers (1990-Present)
- Delivered first portable spread spectrum wireless LAN adapter (including PCMCIA) for mobile computer users (1992-Present)

Over 50,000 spread spectrum products shipped to date

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WIRELESS SYMPOSIUM & EXPOSITION
Santa Clara Convention Center -- February 15 - 18, 1994 -- Santa Clara, CA

WIRELESS LAN'S IN INDUSTRIAL ENVIRONMENTS

Abstract

The wide growing interest in wireless applications to a variety of markets and applications has created a great demand for technology innovations in components, systems architechtures, and marriage of software and hardware solutions. Although the concept of personal communications has been around for many years, its implimintation possibilities have just recently been realized through availability of technology. Wireless LAN systems have been in operation for many years in the industrial environment. The integration of barcode reading, data collection terminals, RFDC (radio frequency data collection), have improved productivity and business operations manyfold. This paper looks at the various technologies, past present and future and their implications for the business/industrial user as well as the personal user. The similarities and differences of the "new" emerging wireless LAN technology targeted for "mobile office" environments and the mature RFDC (radio frequency data collection) systems used in "blue collar" applications are explored. Portable wireless interactive data collection (RFDC) has been around for many years in warehousing, distribution, retail, manufacturing and transportation applications. Ford, GM, the Port of Singapore, Boyd Coffee, AVIS, Apple Computer, K-Mart, Wallmart, Skil, Toshiba, FEDCO, are a small sample of wireless spread spectrum and narrow-band LAN users. Case histories describing the positive impact on operations, customer service, and realized cost savings of typical network installations supporting 700 wireless terminals covering several square miles to 2 wireless terminals and 10,000 square feet are presented.

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Biography:

Mr. Juodikis provides consulting services in application and integration of wireless data networks in industrial, retail, and government environments. He has over 30 years experience in hi-tech business development, startegic planning, product development, program management, and system integration. He has held various technical, sales, and marketing positions, most recently with Symbol Technologies. Mr Juodikis earned a MSEE from Cal Tech, Pasadena in 1963.

Flexible UHF Data Transmission System with Broad Tuning Range

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Abstract

For the use in wireless applications a new versatile data transmission system (receiver / transmitter) has been developed. Typical applications are telecontrol / telecommand links or wireless modems.
Using a PLL synthesizer the system offers a large tuning range from 407 to 480 MHz.
All important functions are controlled by a built-in microcontroller and can easily be set on site by an interactive programming unit. The settings are stored in a nonvolatile memory and can be adressed by external hardware.
The performance of the system is conformal to the European CEPT standard.

The transmitter offers a programmable output frequency with steps of 10, 12.5 and 25 kHz and a programmable output power (1 to 30 mW).
Phase noise is better than -112 dBc/Hz (10 kHz). A special modulation technique allows true DC coupled FM modulation. Transmisssion of arbitrary NRZ code and pulse width modulated signals is possible without transcoding.
Special layout and mounting provides very low vibrational sensivity. Transmitter is as small as 70 x 30 x 25 mm^3 and operates on a 9 V battery with 45 mA.

The receiver is also tunable in steps of 10, 12.5 and 25 kHz and provides a built-in scanfunction. Important parameters like received signal strength indication (RSSI), squelch level etc. are available at the digital interface. It employs dual conversion with 45 MHz first and 455 kHz second IF and analog quadrature FM detection. A special signal shaping unit provides AFC function and recovers the digital signals. Sensivity is better than 1 uV over the whole tuning range.
The receiver is comparably compact 100 x 45 x 25 mm^3 and needs 60 mA from a 9 V power supply.

The paper presents an overview of the architectural concept and principles of operation and describes the complete functionality of the system. Results of measurements are also shown.

1. Introduction

Wireless data transmission systems have gained great importance in industrial and commercial applications.
Traditionally they have worked in remote control of machines, but the use in wireless data terminals has turned out to be a rapidly growing market.
To meet the different requirements of most European countries a rugged, versatile and cost efficient modem for the 70 cm-band has been realized.
With a large tuning range from 400 to 480 MHz and 10, 12.5 and 25 kHz channel spacing the system covers nearly all frequency bands allocated for professional data transmission.
In order to avoid a restriction to specific line codes, DC-coupled frequency shift keying (FSK) is possible. So the system can easily be integrated in a different system environment.

2. General topics

2.1 Overall Performance

The system consists of a high performance transmitter- and receiver module. Its functionality is guaranteed within a temperature range of -30 .. +70°C. The technical specifications meet the requirements of the European CEPT-Standard [3].
For cost effective production a modular design has been employed. Different circuit parts, e.g. PLL, power amplifier, digital circuits have been realized on different layers, which are plugged together and allow easy repair and maintainance.
All important channel parameters like center frequency, frequency deviation, output power of the transmitter, squelch level of the receiver etc. are user programmable via a PC-program. These parameters can be stored in an EEPROM for 16 preprogrammed channels. They are controlled by a 8-bit-microprocessor and adjusted by a 8 channel DA-converter.
An automated alignment and final test of the complete system is possible using one single service monitor.

2.2 Main Design Challenges

Working with small channel spacings (e.g. 10 kHz) requires an oscillator with very low phase noise to realize a good signal to noise ratio and a high channel selectivity of the receiver.
In general for those applications quartz oscillators are used, which however are restricted to single channel operation.
In this system a PLL-stabilized VCO is used, which is tunable over a frequency range of 80 MHz. The design goals have been minimum phase noise and low microphonics.
In order to get really transparent data transmission broadband DC-coupled FM must be possible.
In most applications the system has to be battery powered, so low power consumption is very important. According to this a high-efficiency broadband output amplifier has been developed, which provides a maximum power of 30mW
Another important specification is the sensitivity of the receiver, which is mainly influenced by the loss and the noise of the tunable preselector.
For the use in portable radio equipment the modules have to be very small. Therefore the circuits are realized in surface mout technology on several layers.

3. Realization

3.1 Transmitter

3.1.1 Overview

Fig.1 shows the simplified block diagram of the transmitter.
The heart of the transmitter is the PLL-stabilized voltage controlled oscillator , which is tunable over the frequency range from 407 to 480 MHz.
To prevent feedback from the antenna output to the VCO three buffer stages are used to provide more than 100 dB isolation. The last buffer stage is a variable gain amplifier to control the power of the output stage. The lowpass filter is realized with surface mount coils and capacitors and printed inductances. It provides a supression of more than 60 dB of the second harmonic.The frequency responce of the filter is shown in fig.2.
The microcontroller sets the center frequency, the output power and the frequency deviation and then returns into a sleep mode to lower power consumption.
16 channels can be preprogrammed via a serial data interface in the specified frequency range.
The whole transmitter is realized on 4 layers of FR4 / epoxy-substrate.

3.1.2 VCO

By a special design and a careful layout very low phase noise can be achieved.
The phase noise of the VCO depends on several factors:
- The Q-factor of the resonator
In order to minimize vibrational sensitivity a ceramic resonator with a high Q is used.
- The Q-factor of the varactor diodes
The frequency tuning is realized by using varactor diodes in parallel to the resonator. The diodes should have a low series resistance and a low leakage current.
- The oscillator circuit
Critical parts of the circuits like coupling to the resonator, feedback of the oscillator transistor etc. have been optimized using an automatic phase noise measurement system.
Considering all these points a typical phase noise of -112dBc/Hz could be achieved over the whole frequency range. Fig.3 shows a typical plot of a phase noise measurement.

3.1.3 DC-coupled FM

Using a synthesizer in a FM-data transmision system usually has one disadvantage:
You cannot apply DC-coupled codes (NRZ) like POCSAG [2] or similar because slow frequency deviations will be interpreted by the PLL as a disturbation and will be "corrected".
A special circuit, on which a worldwide patent [1] was applied for, provides true FM modulation down to frequencies of 0 Hz. Fig 4 shows the principle of operation.
First the data signal is filtered by a Bessel filter with flat group delay to limit the bandwidth to 5kHz and then split into a high frequency and a low frequency path. The high frequency signal modulates the VCO loop in the usual way, and the low frequency signal modulates the reference oscillator directly.

3.1.4 Output stage

The power amplifier consists of a bipolar driver stage and Class C MESFET stage with approximatly 60% efficiency.
It provides an overall gain of 20dB and a maximum output power of 17dBm.
The amplifier is designed to have a bandwidth of 10 MHz and can be tuned from 407 to 480 MHz.

The output power can be switched off within 1ms from +15dBm to -70dBm.
The frequency response of the output stage is shown in fig.5 for maximum output power and different tuning voltages.

3.1.5 Summarized performance

- frequency	407...480 MHz	programmable
- channel spacing	10, 12.5, 20, 25 kHz	programmable
- frequency drift	± 5ppm	
- output power	max. 50 mW	programmable
- modulation	DC to 4.8 kBd	programmable
- frequency deviation	typ. 2.4kHz	programmable
- temperature range	-30...+70°C	
- vibrational sensitivity	5g acceleration (100 Hz RMS FM)	
- power consumption	45 mA, 9V	
- size	70 x 30 x 25 mm^3	

3.2 Receiver

3.2.1 Overview

The receiver is a double superhet-system with a first IF of 45 MHz and a second IF of 455 kHz.
The block diagram is shown in fig.6.
The local oscillator for the first frequency conversion is a low phase noise VCO according to the principle previously described.
The demodulated data signal passes a special circuit, which detects rising and falling edges and forms a TTL-compatible signal for digital data transmission.
The parameters controlled by the microprocessor are the center frequency, the squelch level and the tuning of the preselector.
16 channels can be preprogrammed via the RS 232 - interface.
The receiver has a built in scan routine to step through the programmed channels until a data signal is detected.
The whole circuit is realized on 2 layers of FR4/epoxy substrate.

3.2.2 Frontend

The preselector consists of a two stage amplifier with an overall gain of 20 dB.
Filtering is achieved by four coupled LC-circuits.
The shape of the filter curve is formed by 4 tuning voltages to provide optimum gain, noise figure and image rejection for each channel in the specified frequency range.
The image rejection is better than 72 dB.
The noise figure of the whole circuit is less than 5 dB.
In practical use there is often the situation where several remote control systems are working in adjacent frequency channels. To prevent intermodulation a high input intercept point of the receiver is required. With this circuit an input intercept point of -8dBm has been be achieved.
Fig.7 shows a plot of the frequency response for different channels.

3.2.3 IF-chain

A double balanced diode mixer converts the input frequency to the first IF of 45MHz.
A crystal filter with flat group delay provides for the image rejection for the second frequency conversion to 455 kHz.
To realize a channel selectivity better than 60 dB two Ceramic filters with flat group delay are used. A FM-demodulator with high dynamic range provides the data signal and a signal strength indication voltage which is A/D converted and detected by the microcontroller.

3.2.4 Summarized performance

- frequency	407...480 MHz	programmable
- channel spacing	10, 12.5, 20, 25 kHz	programmable
- frequency drift	± 5ppm	
- sensitivity	<1µV (20 dB SINAD)	
- IIP3	> - 10 dBm	
- demodulation	FM 2.4kHz, FSK	
- channel selectivity	>60dB, 64dB typical	
- image rejection	>70dB, 75dB typical	
- squelch level	programmable	
- vibrational sensitivity	5g acceleration (100 Hz RMS FM)	
- temperature range	-30...+70°C	
- power consumption	60mA, 9V	
- size	100 x 45 x 25 mm^3	

4. Acknowledgements

This developement has been supported by the German Ministry of Research and Developement. The authors wish to thank Mr. Ferber and Mr. Bretz from hetronic Steuersysteme GmbH for their work on testing and the fruitful technical discussions.

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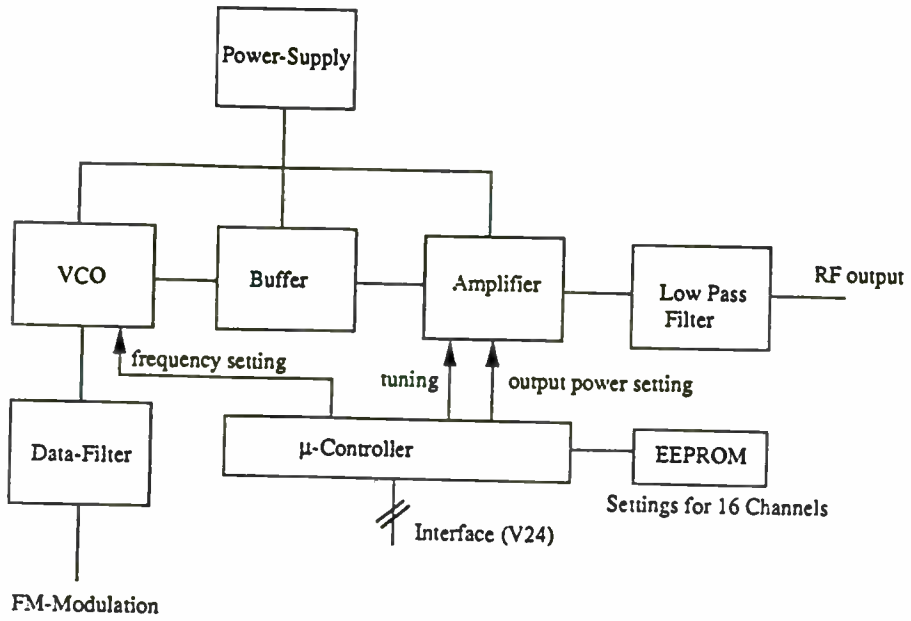

Fig.1 Block diagram of the transmitter

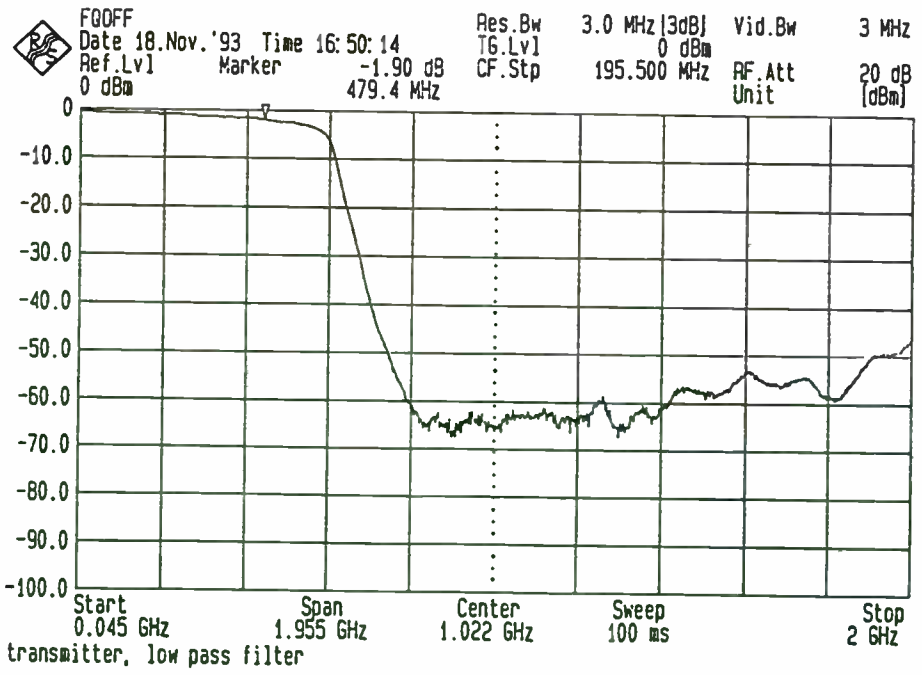

Fig. 2 Frequency response of the low pass filter

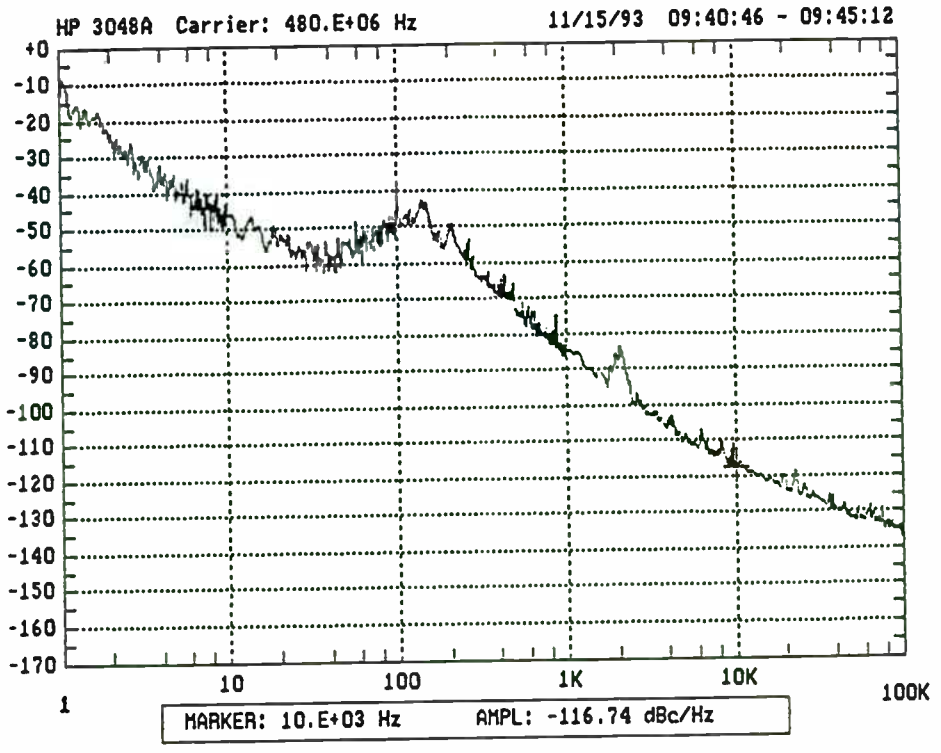

Fig. 3 Phase noise measurement result

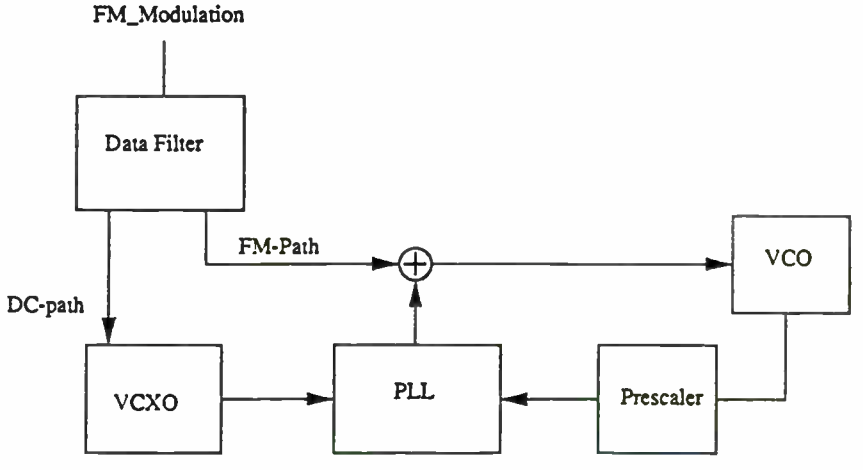

Fig. 4 DC-coupled modulation

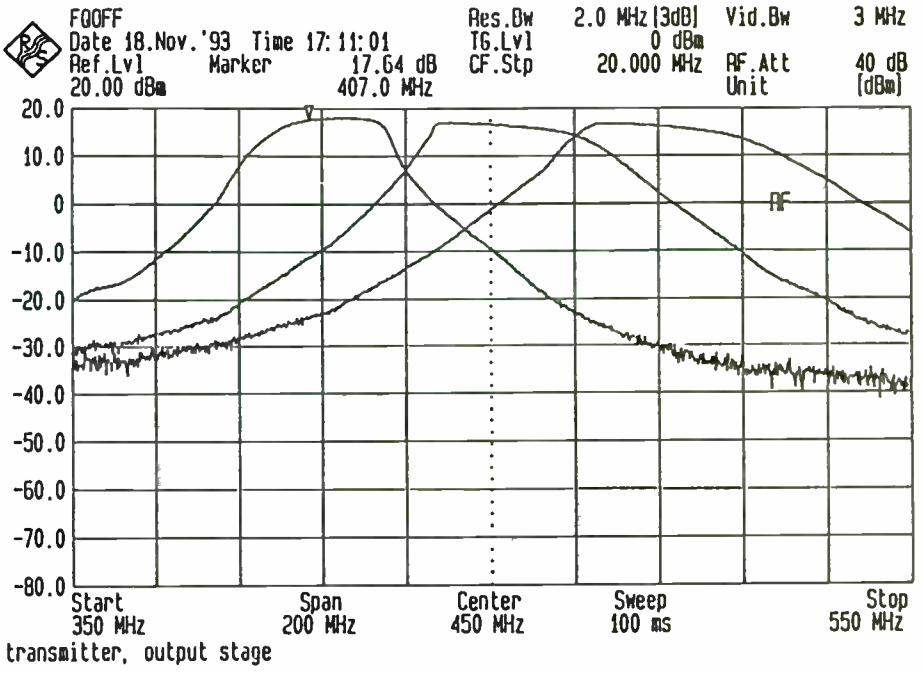

Fig. 5 Frequency response of the tunable output stage

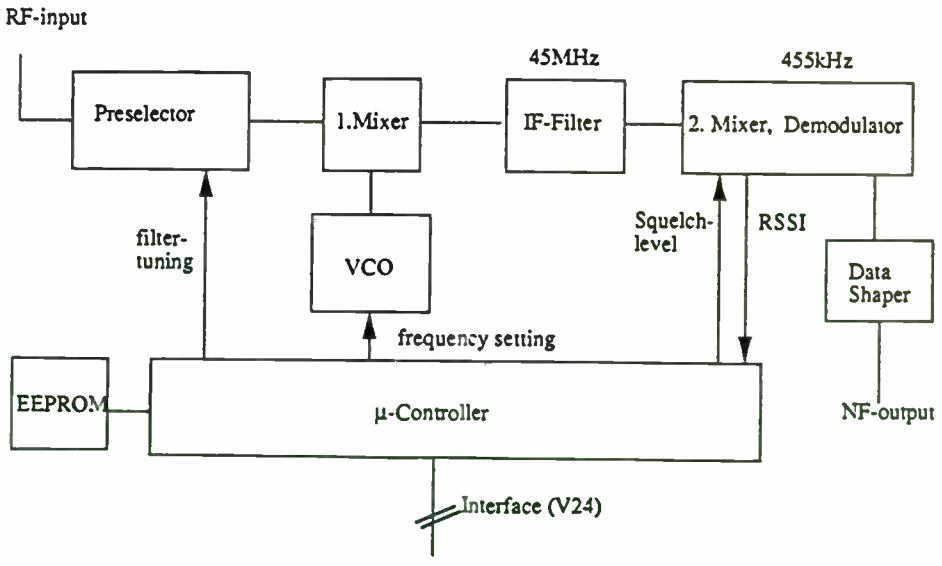

Fig. 6 Block diagram of the receiver

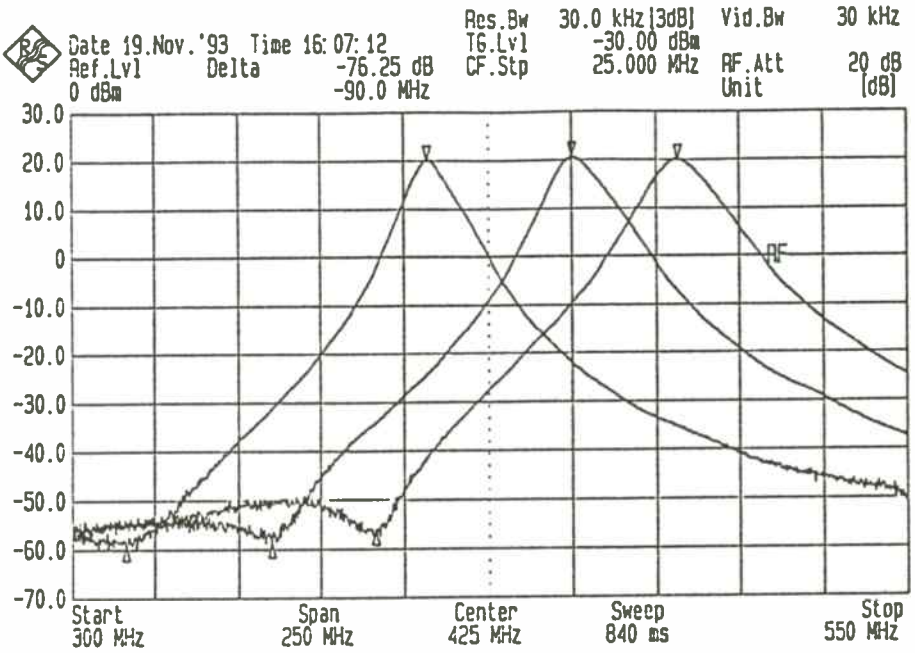

Fig.7 Frequency response of the preselector

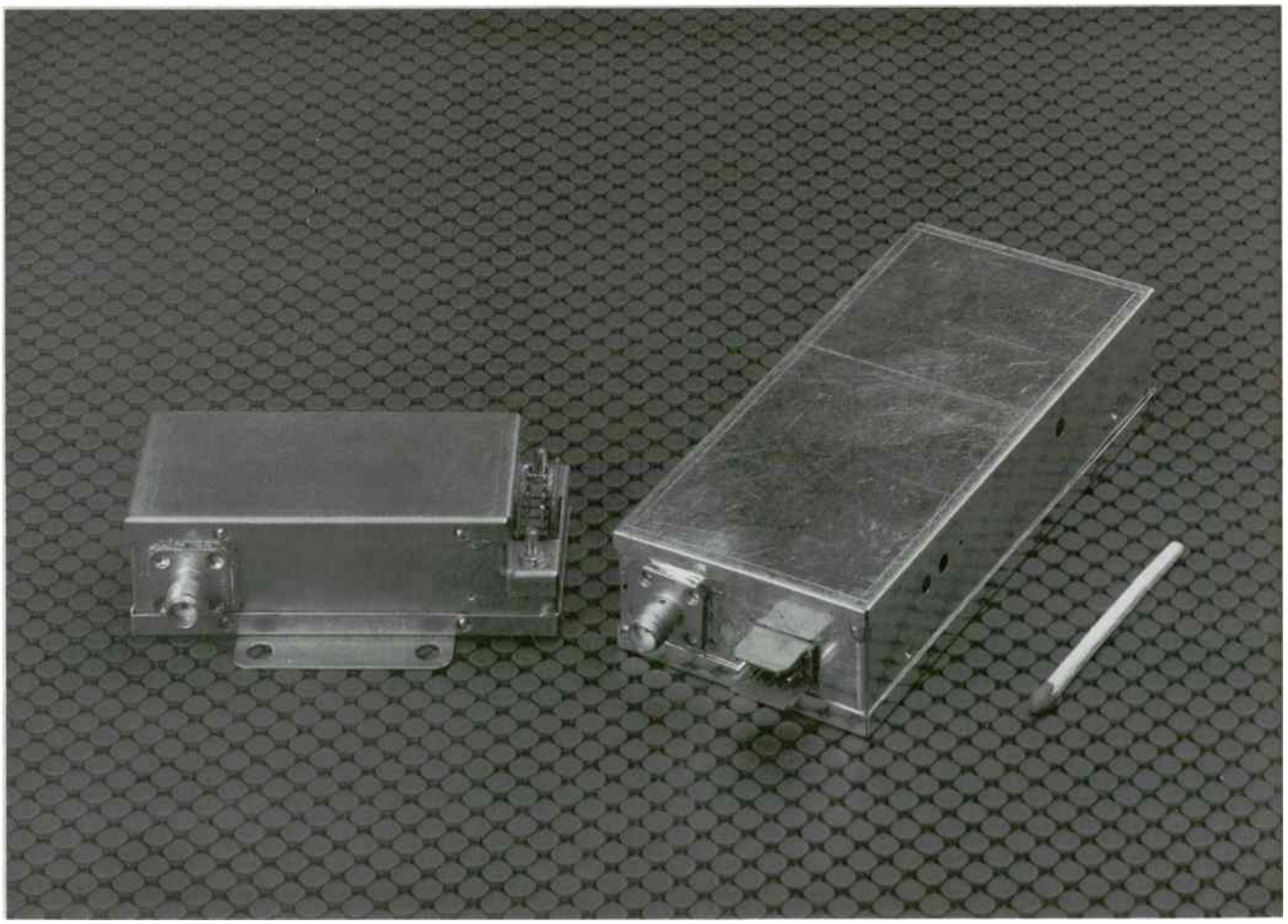

Fig. 8 Photograph of the modules

COMMAND-RESPONSE DATA LINK LAYER FOR WIRELESS MOBILE COMMUNICATIONS

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ABSTRACT

As part of research being conducted by California Polytechnic State University San Luis Obispo for the California Department of Transportation, the Cal Poly Transportation Research Group is developing a wireless digital communications system that can communicate with a large number of mobile stations. This system supports research being completed on a test-track and laboratory facility for Advanced Transportation Management and Information Systems (ATMIS). The ATMIS systems are designed to improve the effectiveness of the vehicle-highway system. One element of the wireless digital communications system is an OSI level 2 data link layer. This layer utilizes a bit oriented link control operating in unbalanced normal response mode.

The data link layer utilizes a slotted ALOHA protocol to allow stations to log into the network periodically and a command-response protocol to maintain active communications with logged-in stations. Operation of the data link layer in command-response mode allows a fixed station (primary) to control access to the network, with mobile stations (secondaries) logging in either anonymously or with known user ID's.

The command response data link layer does not exhibit saturation and breakdown characteristics as load approaches system capacity. Throughput and response time performance degrade linearly as system load increases. Throughput is improved through the use of abbreviated command packets. Channel time is optimally allocated between login and data modes using an adaptive algorithm. Analysis of system throughput and response time performance is described.

A command response scheduling system provides different levels of network service to stations of different priorities. Stations with high priority have increased available channel bandwidth and reduced response times. Lower priority stations are guaranteed minimum levels of service. Station addresses contain geographic location obtained from GPS, which allows selective broadcast to polygon-shaped geographic areas.

Efficient transportation management depends on communication with large numbers of densely packed vehicles. The command response data link layer outlined can provide the link level control required to support the communications needs of transportation management systems.

1. INTRODUCTION

The state of California, like other locations, faces growing problems with safety, congestion, pollution, and delay on its freeway and surface street systems. To address these problems, there is now an increasing emphasis on the development and implementation of more effective and intelligent vehicle highway systems.

The California Department of Transportation (Caltrans) is conducting an Advanced Transportation Management and Information Systems (ATMIS) testbed research program that is developing, testing, and implementing an integrated package of new technologies and techniques for managing highway congestion, safety, and pollution. The ATMIS program is a coordinated effort involving cooperation among Caltrans, California universities, and private enterprise. California Polytechnic State University at San Luis Obispo supports the testbed research program by employing the facilities and software resources of the Cal Poly Transportation Management Center (TMC) simulation laboratory, vision laboratory, field test facility, and communications development laboratory to provide support for testing and refining ATMIS systems in a controlled environment prior to real world field testing in other locations.

Vehicle to TMC communications are a vital component of any ATMIS system. By providing a communications link between individual vehicles and a TMC, it becomes possible to manage traffic congestion and other highway problems immediately, and to keep drivers aware of changing road conditions. In particular, such a communications link can provide:

1. Ability to inform vehicles of changing road conditions and emergencies, and to offer in-vehicle routing directions
2. Ability to monitor vehicle speed and density on a section of roadway
3. Ability for the TMC to monitor vehicle position
4. Ability to monitor the engine and emissions status of a vehicle automatically and compile statistics for a section of roadway
5. Ability to collect tolls automatically and transparently, and perform other vehicular transactions while ensuring individual privacy and security

Researchers at the Cal Poly communications development laboratory have designed and implemented a command-response data link layer that operates in conjunction with Utilicom Code Division Multiple Access (CDMA) modems to provide reliable packet service in a mobile environment.

2. COMMUNICATIONS REFERENCE MODEL

The Open Systems Interconnection (OSI) reference model partitions network communications into seven layers of functionality, allowing the task of designing and implementing network communications to be broken down into manageable sub-tasks. The seven OSI layers may be summarized as [1]:

Layer 7	(application):	Network services to the end user
Layer 6	(presentation):	Formatting, encryption, and compression of data
Layer 5	(session):	Setup and management of end-to-end conversation
Layer 4	(transport):	End-to-end delivery of messages
Layer 3	(network):	End-to-end transmission of packets
Layer 2	(data link):	Reliable transmission of packets on a given link
Layer 1	(physical):	Transmission of bits

Each of the seven OSI layers provides services to the layer directly above it, and utilizes services of the layer directly below it. In general, each layer might add control information, increasing system overhead.

2.1 Reduced OSI reference model

Because the OSI reference model is intended to be a general tool to help with the description of all types of network communications, it provides more layers of functionality than may be required for some systems. For dedicated short range communications, the network, transport, session, and presentation layers may be minimized or eliminated [2], [3], thereby reducing framing overhead and saving transmission bandwidth.

The network layer is eliminated because endpoints of communication are the vehicle and the primary station, and no routing is required. Because routing is eliminated, and all communications are across a single link operating with one unified protocol, there is no need for a transport layer to provide protocol negotiation for end-to-end message passing. The data link layer may provide all transport functions such as flow control, error detection, frame sequencing, and frame addressing. Since the transport layer is not needed, session management reduces to data link layer management.

The session layer is minimized because only one dialogue, command-response, is allowed, and all stations are designed to implement it. Session layer control is not needed. The only session layer functionality used is in the adaptive login process (sec 4.1.2), and the prioritization of commands (sec 4.2) at the primary.

Pre-defined data formats are used, so no presentation layer is required. This layer will be added when encrypted service is implemented.

2.2 Implemented OSI reference model

The wireless system is implemented using only the physical, data link and application layers (Fig. 2.1). Session layer functions are implemented using prescribed data link layer capabilities, thus the session layer is incorporated in the data link layer. The physical layer is described in section 3, and the architecture and implementation of the data link layer is described in section 4. The application layer is not described in this paper as it is dependent on the ATMIS system implementation.

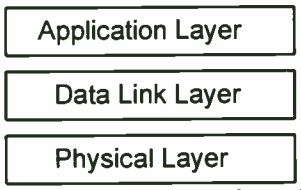

Fig. 2.1 Implemented OSI layers.

3. SPREAD SPECTRUM PHYSICAL LAYER

The application of wireless radio to a mobile metropolitan environment involves many considerations due to the dynamic, multi-user, multi-path nature of the channel. A robust radio link is essential for reliable communications, and was the basis for the selection of spread spectrum technology. While more complex than traditional narrow band approaches, spread spectrum provides the following advantages:

- Greater immunity to interference, jamming and multi-path distortion
- Inherent security of the transmitted message
- Compatibility with multi-access and multi-user requirements
- License free operation in specific frequency bands

Interference immunity was a vital consideration in the decision to use spread spectrum modems. Freedom from licensing requirements during development and field testing was also important.

Spread spectrum derives its interference immunity through processing gain resulting from the modulation of the signal with a fixed pseudo-noise (PN) pattern. Processing gain can be achieved through two modulation techniques; direct-sequence and frequency-hopping. Frequency-hopping spread spectrum was not cost effective due to the high cost of very fast frequency synthesizers required to attain high hopping rates. Without high hopping rates, frequency-hopping does not provide the required processing gain and immunity to multi-path interference. Direct-sequence spread spectrum offers excellent processing gain at lower cost. Utilicom Inc., a company with experience in spread spectrum development for military and commercial applications, was tasked to design a spread spectrum system. Cost containment was also required.

Utilicom, working with Stanford Telecom, developed a design using a single low-cost ASIC combining the functions that were previously in a three chip set. The resulting system incorporates a very robust RF front end with long direct-sequence PN codes, providing excellent performance and high interference immunity. The spread spectrum system is configurable through an RS-232 port by means of Hayes-compatible commands. Configurable modem parameters include transmit power level, data rate, RF center frequency, PN code and length, and synchronization time. All modem parameters are stored in non-volatile memory to maintain system configuration through power cycling.

4. DATA LINK LAYER

The data link layer (DLL) uses a command-response multi-point protocol and dynamic priority scheduling to allocate the time resource of the channel.

4.1 Command-Response protocol

Specific design objectives included:

- Maintain regular communication with all stations under periods of heavy load. The network must be able to function during traffic gridlock when the number of users is at a maximum.
- Exhibit linear performance degradation under heavy load. Network capacity should not diminish at a rate more rapid than the rate of load increase.
- Prevent station starvation under periods of heavy load. No station should ever be locked out of network communications.
- Provide centralized control of channel time allocation so the general public may access the network, but may not use excessive bandwidth.

4.1.1 Data Link Layer architecture and ISO High-level Data Link Control

The DLL is implemented using High-level Data Link Control (HDLC), a well established and standardized bit oriented link control. The DLL utilizes HDLC's capability to operate in Normal Response Mode (NRM) [4], where a single primary station controls multiple secondary stations, and secondary stations may not transmit unless given explicit permission by the primary. The primary station controls all operations on the link through the use of HDLC command frames, and all secondary stations respond with HDLC response frames.

In normal operation, the primary station continuously cycles through the following four modes of operation, which constitutes a command cycle: (see Fig 4.1)

1. General Broadcast Mode
2. Slotted ALOHA Login Mode
3. Login Confirm Mode
4. Normal Response Mode

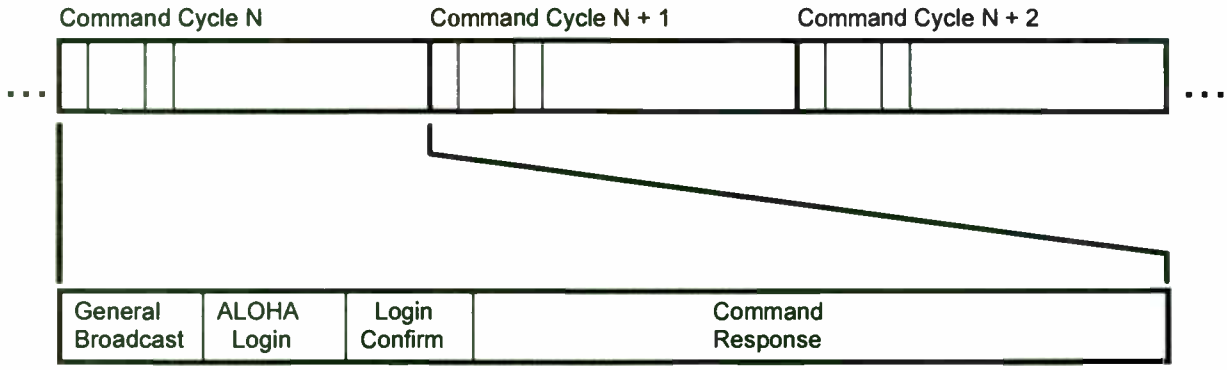

Fig 4.1 A single command cycle as it occurs repetitively in time.

General Broadcast Mode In general broadcast mode, the primary station sends messages to secondaries via system defined HDLC XID [5] frames. Broadcast messages may be addressed to all secondaries, or pre-defined subgroups of secondaries. Secondary stations are capable of being members of more than one broadcast subgroup. Secondary stations do not acknowledge broadcast messages.

Slotted ALOHA Login Mode A slotted ALOHA login time period occurs once per command cycle. The login period is divided into time slots. Secondary stations may only transmit within a single slot. The primary station signals the beginning of the login time period with the transmission of an HDLC XID frame defined to be a *start of login time period command.* The *start of login time period command* provides the slot length, number of slots, and other link initialization parameters such as window size and maximum packet size. After transmitting the *start of login time period command,* the primary station listens for all login attempts.

Fig 4.2 A start of login time period message followed by ALOHA login time slots.

To attempt a login, a secondary station waits until a *start of login time period command* is received, and then transmits an HDLC XID frame within a randomly selected slot. The transmitted XID frame is defined to be a *login request response*, and contains a randomly generated fourteen bit address (see sec 5 for extended HDLC addressing) that uniquely identifies the secondary while it is logged in. When two or more secondaries make login attempts within the same slot, the *login request responses* collide and are lost. These stations will not receive login confirmation. Secondary stations may login anonymously or with a permanent identification number.

Login Confirm Mode Upon completion of the ALOHA login time period, the primary station sends an HDLC Set Normal Response Mode command (SNRM) as a *login confirm command* to each secondary station it is permitting to login. Secondary stations logging in anonymously transmit an HDLC Unnumbered Acknowledgment (UA) as a *login confirm response* upon receipt of a *login confirm command,* and consider themselves logged in. When the primary receives a *login confirm response* from a secondary, it adds the secondary to a confirmed login list for the current command cycle.

If the fourteen bit address in the secondary station's *login request response* is being used by another secondary, the primary station confirms the login using an XID frame defined to be a *login address reassignment command.* The login address reassignment command to a secondary is followed immediately by a *login confirm command* (SNRM), placing the secondary in normal response mode.

If the secondary is logging in identified, it responds to a *login confirm command* with an XID *identified service request response* frame, which contains a four byte unique identifier for the secondary.

Upon completion of sending *login confirm commands* to all secondaries, the primary updates the confirmed login list. The confirmed login list is used by the priority scheduler (sec 4.2).

Secondary stations that have made a login attempt and do not receive a *login confirm command* before either their login complete timer has expired, or another *start of login time period command* is received, consider themselves logged out, and make another login attempt the next time a *start of login time period command* is received.

Command-Response Mode When operating in command-response mode, the primary station follows standard HDLC Normal Response Mode (NRM) protocol, utilizing HDLC supervisory frames as commands when there is no application data for a secondary, and HDLC Information frames when there is. Command-response mode is the principal method used by the primary station to communicate with secondary stations that are logged into the network.

Secondary stations are required to respond with HDLC information frames when they are commanded and have data ready to send to the primary, or an HDLC Supervisory frame when they have no application data. Reference [6] describes of the use of information and supervisory frames for HDLC NRM operation.

4.1.2 Adaptive mode balancing

Adaptive mode balancing utilizes an adjustable login time period to ensure that there are enough ALOHA slots to minimize the probability of collisions during login, but not so many that there is excessive idle channel time. The length of a login time period is determined by two factors:

1. The percentage of successfully used time slots during the previous two login time periods.
2. The average number of attempts required for stations to successfully login. Secondaries report the number of failed login attempts as a part of the login process.

The effect of adaptive mode balancing is best described by an example:

1. Upon start up of a primary station that has been off the air, all secondaries within the broadcast area will desire to login. There may be many secondaries waiting to login. The primary will initially send a *start of login time period command* that specifies a large ALOHA login period. (Fig. 4.3a)

2. After the initial command cycle, the primary will have received some valid login attempts so there will be secondaries to command, but there may also be secondaries that need to login - some that failed due to collisions on the previous login period and some that are making their initial attempt.

3. In the second command cycle, the primary will reduce the length of the login time period and add a period of command-response mode (Fig 4.3b) to support the newly logged in secondaries.

4. As more secondaries are logged into the network, the primary will continually redistribute the time spent in different modes of operation within a command cycle (Figs 4.3c).

ALOHA Login	Login Confirm	Command Response

Fig 4.3a Initial command cycle with extended login time period and no general broadcast.

General Broadcast	ALOHA Login	Login Confirm	Command Response

Fig 4.3b Second command cycle with more stations logged on.

General Broadcast	ALOHA Login	Login Confirm	Command Response

Fig 4.3c Third command cycle - approaching normal operation.

4.2 Command-response priority scheduling

The command-response priority scheduler provides different levels of network service to stations of different priorities. High priority stations are guaranteed to have more available channel bandwidth than low priority stations, that is, they receive more transmission opportunities in each command cycle. Low priority stations are guaranteed some transmission opportunity. That is, starvation is not possible.

The priority scheduler was designed with flexibility as a primary concern. No limit is placed on the number of priorities in the network, nor is there a limit on the number of stations that may occupy one priority level. To satisfy these two conditions, dynamic allocation of transmission time (per priority) is performed at the beginning of each command-response cycle.

4.2.1 Priority bandwidth allocation

The scheduler first calculates the relative distribution of stations by priority. The relative frequency for a given priority is defined by

$$freq_{rel(priority)} = \frac{\#stations_{priority}}{\#stations_{total}} \tag{4-1}$$

After the scheduler calculates the relative frequencies of all priority levels, it then calculates $P(n)$ for each priority level, representing the number of times each station is commanded in each command cycle. The $P(n)$ are computed in ascending order of priority, from lowest to highest. See equation (4-2).

$$P(n)_{priority} = P(n)_{priority-1} + \frac{freq_{rel(priority-1)}}{freq_{rel(priority)}} \tag{4-2}$$

The number of times each station within a priority level is commanded in a given command cycle is directly related to the number of times each station in the lower adjacent priority level is commanded. In the case of the lowest existing priority in the network, where there is no lower adjacent priority level, stations receive exactly one transmission opportunity per command cycle.

A model of user demand and simulation studies to validate this proposed algorithm are currently being developed.

4.2.2 scheduling of commands

After the number of commands per command cycle has been calculated for each priority level, they are loaded into the scheduling table for use during the next command response mode. The scheduling table determines when all

stations are commanded, and ensures that when a station is to be commanded more than once per command-response cycle, the commands will be distributed evenly through the cycle.

5. EXTENDED HDLC AND GEOGRAPHIC ADDRESSING

HDLC provides the capability to use address fields larger than one byte, allowing the address of a station to be expanded according to specific needs.

5.1 Extended HDLC

Standard HDLC uses a one byte address field. Extended HDLC provides the capability to extend the address field by some number of bytes, allowing for larger addresses to be used. Each HDLC address field byte contains seven bits of address information, and one bit to indicate the end of the address field. A fourteen bit (two byte) address allows for 2^14 (~16K) unique link level numeric addresses.

5.2 GPS coordinates as part of extended HDLC addressing

In addition to a numeric address, the physical position of a mobile station is a useful component of its identity. The HDLC address is further extended to contain GPS derived position information. To minimize the number of bytes required, secondary station coordinates are reported relative to the primary station position in units of meters. The secondary station is able to calculate relative position because the primary station transmits its latitude and longitude as a link initialization parameter during the *start of login time period command.* Relative position is represented using four bytes, two for delta x (east-west) and two for delta y (north-south). Each of the two byte delta fields contain fourteen usable bits, allowing for representing +8191/-8192 meters. This provides the capability for one meter resolution within a ten mile by ten mile broadcast area.

A feasibility analysis of using differentially corrected GPS for mobile secondaries is ongoing. It is anticipated that accuracy will be on the order of ten meters, well within the resolution of the delta x and delta y relative position fields described above.

6. PERFORMANCE ANALYSIS

In designing the protocol for the network, communication performance was roughly estimated using analytic techniques. Once the network prototype was developed, performance calculations were verified using a software simulation. Simulation is an important part of predicting performance for this system since network behavior is complex. There are many parameters, and some parameter values for one command cycle are dependent on results of previous command cycles.

6.1 Performance measurement objectives

Turnaround time is defined to be the time of one complete command cycle. Analysis of turnaround time is important for determining network robustness and responsiveness.

Effective bandwidth as a percentage of absolute bandwidth, or *network efficiency,* is important as a measure of performance, especially in comparison to network alternatives.

6.2 Definitions and assumptions

To simplify calculations, a number of assumptions are made for the following formulas:

1. Distance between vehicles is constant.
2. Density or number of vehicles per length of highway per lane is constant.
3. Volume or number of vehicles per unit of time per lane is constant.
4. All secondary stations are served at the same priority level.
5. Stations (primary and secondary) always have exactly one message to send.

Nine types of packets are assumed to exist: start of login, send login attempt, send login confirm, login confirm response, long information (primary to secondary), short information (primary to secondary), long information (secondary to primary), short information (secondary to primary), and disconnect from broadcast area. All are of constant length and require constant transmission times. Transmission propagation time is considered zero since the messages are traveling at nearly the speed of light over small distances (< 10 mi.). Carrier synchronization time for each packet is assumed to be constant.

Let D = vehicle density (vehicles/mi/lane)
V = volume (vehicles/sec/lane)
L = length of highway covered by primary broadcast area (mi)
l = total number of lanes

Then DLl = Number of vehicles in a broadcast area at any given moment.

N is the average number of stations logged in during a command cycle, and varies with DLl, V, turnaround time, number of ALOHA slots, and bit error rate.

M is the percentage of stations sending long packets. This is used in the simulator test cases to provide load performance data. Several time values are of interest. All time parameters are in units of seconds.

Let T_L = transmission time for a start of login packet
T_{Slot} = transmission time for a send login attempt packet
$T_{LConfirm}$ = transmission time for an send login confirm packet
$T_{ConfirmR}$ = transmission time for a login confirm response packet
T_{lLps} = transmission time for a long information (primary to secondary) packet
T_{lSps} = transmission time for a short information (primary to secondary) packet
T_{lLsp} = transmission time for a long information (secondary to primary) packet
T_{lSsp} = transmission time for a short information (secondary to primary) packet
T_{DISCNT} = transmission time for a disconnect from broadcast area packet

All packet transmission times include carrier synchronization time.

T_{LOGIN} = length of slotted ALOHA login period
$T_{CONFIRM}$ = total time for new stations to be confirmed as logged-in
T_{POLL} = total time for the protocol to poll and receive responses from all logged-in stations
T = total turnaround time for current cycle
T_{Last} = total turnaround time for previous cycle

VlT_{Last} = Number of vehicles to enter (and exit) the broadcast area during the previous command cycle.

6.3 Predicted results

To find T, first determine the time period for each of the parts of T.

First, let the slotted ALOHA period have K slots, where K is determined by the adaptive mode balancing algorithm. If K is large relative to stations wishing to log in, this alleviates congestion caused by collisions in the slotted ALOHA protocol. The offered load G is then

$$\frac{\text{number of stations attempting to log in}}{\text{number of slots available}} = \frac{VlT_{Last}}{K}.$$

It can then be expected that $G\,Ke^{-G} = VlT_{Last}\ e^{-1/K}$ vehicles attempting to log-in will do so successfully during that period [8]. The others will lose their login packets through packet collisions. By enlarging the capacity of the login period, fewer packet collisions are expected during the login period.

It follows that:

$$\begin{aligned}
T_{LOGIN} &= T_L + KT_{Slot} \\
T_{CONFIRM} &= VlT_{Last}e^{-VlT_{Last}/K}(T_{LConfirm} + T_{ConfirmR}) \\
T_{POLL} &= (N - VlT_{Last})(M(T_{ILps} + T_{ILsp}) + (M-1)(T_{ISps} + T_{ISsp})) + VlT_{Last}(MT_{ILps} + (M-1))T_{ISps} + T_{DISCNT})
\end{aligned}$$

Therefore,

$$T = T_{LOGIN} + T_{CONFIRM} + T_{POLL} = T_L + KT_{Slot} + VlT_{Last}e^{-VlT_{Last}/K}(T_{LConfirm} + T_{ConfirmR}) +$$
$$(N - VlT_{Last})(M(T_{ILps} + T_{ILsp}) + (M-1)(T_{ISps} + T_{ISsp})) + VlT_{Last}(MT_{ILps} + (M-1)T_{ISps} + T_{DISCNT})$$

Because T is dependent on T_{Last}, and both are dependent on overall load on the system as well as the random factor of how many entering stations avoid packet collisions while logging in, this formula can not be simplified for an average turnaround time $\overline{T}$.

From the above, it can be seen that reducing the value of K will reduce T. However, if K is too small, not all secondaries will be able to log in to the network while they are in the primary broadcast area. From [8], the average number of login attempts for a station is

$$\frac{G}{S} = e^G = e^{\frac{VlT_{Last}}{K}}, \text{ where S represents throughput or } \frac{\text{successful logins}}{\text{number of slots available}}.$$

For this network it is desirable to maintain $\frac{VlT_{Last}}{K}$ to approximately 0.25, thereby allowing secondary stations to log in faster, even though total turnaround time is increased. At $\frac{VlT_{Last}}{K} = 0.25$, $G = 25\%$, which represents the "knee of the curve" phenomena for ALOHA protocols. As G exceeds this value, the proportion of packet collisions increases sharply.

Finally, for the network configuration described:

$$\%\ \text{efficiency} = \frac{\text{time transmitting useful information}}{\text{total time of transmission}}$$

$$= \frac{N(M(T_{ILps} + T_{ILsp}) + (M-1)(T_{ISps} + T_{ISsp})) + VlT_{Last}(MT_{ILps} + (M-1)T_{ISps})}{T}$$

6.4 Simulated channel performance

A multi-node simulator was developed to test the wireless communications software through a simulated Gaussian channel, allowing network functionality to be tested. All transmission delays were set to approximate those expected for the Utilicom modems. The software was tested under various bit error rates (probability of error) and channel loading conditions (see Tables 6.1, 6.2, and 6.3). Channel loading was set to simulate different proportions of short and long messages, with short and long messages equivalent to two and forty byte data fields respectively.

The multi-node simulator provided the ability to log stations in and out of the network at pre-defined rates, simulating vehicles entering and exiting the broadcast area of a primary station. The entrance rate was set to 1.6 vehicles per second. The exit rate was the same as the entrance rate, except scaled by the percentage of the maximum number of stations logged on. The number of transmission retries was set to one, and all stations were given the same priority, allowing one transmission opportunity per station per command cycle. All simulations began with 120 stations attempting initial login. The maximum number of stations was set to 140.

Probability of Error	Efficiency (%)	Turnaround Time (sec)	Average # Stations Logged In
5.0 E-4	21.0	15.2	110
1.0 E-4	27.1	13.5	122
5.0 E-5	28.9	14.9	124
0	30.1	14.3	132

Table 6.1 Network performance with 20% long messages and 80% short messages.

Probability of Error	Efficiency (%)	Turnaround Time (sec)	Average # Stations Logged In
5.0 E-4	33.0	17.4	99
1.0 E-4	43.3	18.2	119
5.0 E-5	44.8	17.2	125
0	47.2	17.3	129

Table 6.2 Network performance with 50% long messages and 50% short messages.

Probability of Error	Efficiency (%)	Turnaround Time (sec)	Average # Stations Logged In
5.0 E-4	39.7	17.3	73
1.0 E-4	53.0	19.9	114
5.0 E-5	54.6	20.1	122
0	57.0	20.8	129

Table 6.3 Network performance with 80% long messages and 20% short messages.

Things to notice about the simulation results:

1. Average number of stations logged in falls as BER raises.
2. Efficiency falls as BER raises.
3. Turnaround time behaves in a more complex fashion. It is determined by variables having effects on one another in nonlinear ways. More studies, both analytic and simulation, are being conducted.

7. CONCLUSIONS

The network prototype being designed and implemented at Cal Poly is intended for a rather specialized area of application (ATMIS). A first prototype has been developed, along with testing, simulation, and diagnostic tools. The absence of the OSI layer 3 protocol in the network means that congestion management will primarily be implemented by restraint of message transmission at level 7 and in the network applications. In the initial development of the prototype, several important issues have been examined, including the effect turnaround time and network congestion have on each other. The relationship between turnaround time and network congestion has been shown to be complex, and is a subject for further investigation. Because all simulated channel testing was completed at 9.6 Kbps asynchronous, and the system will eventually operate at 32 Kbps synchronous, system performance is expected to increase by a factor of about four.

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An OOK Modulation Data Receiver for Periodic Part 15 Operation Using a Low Cost Silicon Monolithic Integrated Circuit

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1. Introduction

This paper describes a low cost solution for an OOK (On-Off Keying) receiver in the Periodic Operation Part 15 band from 260 to 470 MHz that is designed to track and lock to the carrier of a SAW resonator transmitter. The simplest form of ASK (Amplitude Shift Keying) is OOK in which the carrier is simply swiched on and off by the PCM (pulse code modulation) waveform. Generally, a low cost OOK transmitter consists of a SAW resonator and a transistor used as a Colpitts oscillator (see Figure 1). Frequency stability is only fair compared to a crystal controlled source which offers excellent frequency stability. Because of poor frequency stability due to time and temperature effects, the frequency of a 300 MHz SAW resonator oscillator typically shifts ± 150kHz. A standard OOK receiver is designed with a wideband response to capture the drifted transmitter at the expense of sensitivity and selectivity. The OOK receiver presented in this paper offers greater range of operation due to improved sensitivity and is consistent and reliable in its ability to automatically tune to the received carrier.

2.. Application Overview

In the U.S.A., the Federal Communication Commission (FCC) has allocated the 260 to 470 MHz for periodic Part 15 operation. The FCC regulations are found in the Code of Federal Regulations (CFR), Title 47, Part 15 (paragraph 15.231). It is strongly recommended that this document is reviewed before pursuing an application in this band. In the U.S.A., most of the consumer applications are regulated under Part 15, covering nonlicensed intentional radiators. CFR Title 47 can be found at most libraries in the reference section or may be obtained from the U.S. Government Printing Office.

Periodic operation refers to the amount of time that a system is active. A manually operated transmitter shall employ a switch that will automatically deactivate the transmitter within 5 seconds; likewise a transmitter that is activated automatically shall cease transmission within five seconds after activation. Periodic transmissions at regular intervals are not allowed. However, polling to determine the integrity of the transmitters used in security or safety applications is allowed if the periodic rate of transmission does not exceed one transmission of more than one second duration per hour for each transmitter in the system.

The field strength of emissions from intentional radiators from 260 to 470 MHz shall be limited to 12500 microvolts/ meter measured at 3 meters. At band edges the tighter limit of 3750

microvolts/meter applies. Field strength of spurious emissions are 1/10 of the fundamental frequency of the intentional radiator. The bandwidth of the emission shall not be wider than 0.25% of the center frequency. Bandwidth is determined at the points 20 dB down from the modulated carrier.

Although continuous transmissions such as voice, video and data are not permitted, the transmission of recognition codes is allowed. These codes are used to identify a sensor or switch that is activated or to identify the particular component as being part of the system. The intentional radiator is restricted to the transmission of control signals such as those used with security alarm systems, door openers, keyless entry, remote switches, remote sensing/telemetry, etc.

The general system may consist of a number of transmitters used to provide control signals from remote sites. The receiver demodulates the signal and recognizes the remote sites; then the system may initiate a response in several ways such as sounding an alarm, making an automatic distress call, turning on a light, opening a door , turning on sprinklers, etc. Each site may use a coded address that would be broadcast to indicate the intended receiver. Some applications are more critical than others, such as a security alarm or distress calling systems; it is important that the system is dependable.

The receiver has the job of extracting and reproducing information from the modulated RF signal that has been corrupted by noise in the channel. Consistent recovery and error free replication of the modulating signal requires a receiver which has reliable performance. There are two main classes of radio frequency receivers: (1) Tuned Radio Frequency (TRF) and (2) Superheterodyne receivers.

The TRF receiver (Figure 2) may consist of several cascaded high gain RF amplifier and tunable bandpass filter stages followed by an appropriate detector (envelope detector, product detector, FM detector, etc.). A reliable TRF receiver at UHF frequencies is difficult to achieve because appreciable parasitic feedback between the output and input of the high gain RF amplifier chain creates oscillation at the center frequency. Reducing the gain in the RF amplifier chain may prevent oscillations but lower gain will reduce the sensitivity of the receiver. These receivers generally use discrete semiconductors since integrated circuits are not available for low voltage, low power applications. A TRF receiver may be very simple in design and component count such as a simple "crystal set" built by hobbyists.

The more reliable and stable receiver described in this paper is a superheterodyne type receiver. In this receiver the RF carrier is filtered and amplified using an RF preamplifier and is downconverted using a mixer and local oscillator (LO) to a convenient lower frequency called the intermediate frequency (IF). The IF signal is amplified and filtered and then demodulated by using an appropriate detector. The OOK receiver shown in Figure 3 has many advantages over a TRF receiver. It utilizes a monolithic integrated circuit, the MC13156 as the main building block component; this device offers very stable operation with over 95 dB of stable gain. Typical sensitivity is -100dBm which allows for a greater operating distance between transmitter and receiver. By utilizing a varactor controlled LO locked by an external automatic frequency control (AFC) circuit, the receiver has the ability to lock onto the transmitter. This system relieves the need to use a more expensive crystal oscillator for the LO while providing a means to capture a transmitter that may drift an appreciable amount of the receiver's IF bandpass.

3. Description of the MC13156

The MC13156 is an integrated wideband FM receiver system intended for digital and analog modulation formats. Its functions are divided up in accessible blocks as shown in the block diagram (Figure 4). It was developed as a high performance IC to be used in battery operated radio systems; as it can be operated below 2 Vdc. It is an ideal receiver for the recovery of GMSK, FSK, or FM signals. A typical circuit for a CT-2 (900 MHz Digital Cordless Telephone) receiver backend application is shown in Figure 5. The MC13156 is available in 24 lead wide-body SOIC and 32 lead QFP packages. The circuit detailed in this paper shows how the MC13156 system blocks can be reconfigured to recover OOK signals. Further details about the MC13156 not covered in this paper are found in a comprehensive device data sheet.

Referring to Figure 5, the MC13156's functional blocks include the following:

1. Differential Input Mixer
2. 40 dB IF Amplifier

3. 55 dB Limiter Amplifier
4. Externally Tuned FM Quadrature Detector.
5. Received Signal Strength Indicator (RSSI)
6. Patented Data Slicer Comparator
7. Carrier Detection Comparator

The mixer has differential RF inputs allowing it to be used in balanced and single-ended configurations. Its single-ended input impedance is 1kohm in parallel with 4 picoFarads. Access is provided to the base and emitter of an internal oscillator transistor. This is available for attaching the oscillator resonant tank circuit. The oscillator transistor is directly tied to the mixer and can be operated as an LC oscillator to approximately 200 MHz. The base input provides a direct LO input connection so an external source can drive it. In this manner, the mixer is functional to over 500 MHz. The application circuit of Figure 8 uses an external varactor controlled VCO to provide LO drive at approximately 309 MHz.

The IF chain is split into two sections to allow IF bandpass filtering in two places: 1) between the mixer and IF amplifier and 2) between the IF and Limiter amplifiers. Output impedance driving each filter port is 330 ohms, which is ideal for common ceramic IF filters centered at 10.7 MHz. The IF and limiter amplifiers inputs will require 430 ohm to ground to match the 10.7 MHz ceramic filters.

The limiter is coupled internally to the quadrature detector inputs. An external RLC tank provides selection of the demodulator tuned frequency and detection bandwidth. The detected response is a current output, which can be converted to a voltage by using a resistive divider or a transimpedance amplifier. The output is biased to stay between a diode drop below V_{CC} and a diode drop above V_{ee}.

The RSSI (Received Signal Strength Indicator) output provides an output current that is proportional to the logarithm of the receiver input voltage (Note: externally load it with a resistor to Vee). Its typical transfer gain is 0.4 μA per dB of input drive level. The RSSI dynamic range is over 70 dB, which is achieved by sensing signal strength at each stage of the IF and limiter amplifiers and summing them together. The RSSI linearity is affected by the loss placed between the IF amplifier and the limiter amplifier; 12 dB is optimal. The RSSI output rise and fall times are adequate to follow signal amplitude variations to rates greater than 50 kHz. (see Figure 6).

The data slicer comparator has 500 kHz of toggling capability. The threshold is internally biased at 1.1 Vdc above V_{ee}. The input is self biased near this threshold. Therefore, input AC coupling is required. An internal input clamping circuit maintains the comparator input within one half a diode drop of threshold and allows for fast capacitor charging. This prevents lost data should the comparator be driven with an extended single data state. The externally controlled hold pin shuts off the comparator input and output in such a way that the input AC coupling capacitor charge is held constant. This allows for speedy data recovery once the data slicer is reenabled. The carrier detect comparator response time is not adequate to recover ASK signals for most applications presented in this paper; it is mentioned only for completeness in this description.

4. Application Circuit Description/Design

The block diagram of the OOK receiver is shown in Figure 3 and details of the MC13156 application circuit are shown in Figure 7. An external VCO is used as the LO source in order to downconvert the received 320 MHz RF carrier signal. The VCO tuning frequency is controlled by an automatic frequency control (AFC) circuit created with the MC13156 frequecy demodulator and an external loop filter. ASK demodulation is achieved by using the MC13156 fast RSSI port. The RSSI output is fed to the data slicer. The data slicer shapes the recovered RSSI data into a rail-to-rail logic swing. In the following sections each part of the OOK receiver is explained in more detail.

External Varactor Controlled Local Oscillator

Figure 8 is a schematic of the external local oscillator circuit only. The components are labelled for easy reference in the following discussion. The LC oscillator transistor is an MPS901 (RF low power transistor in a TO-92 plastic package; also MMBR901 is available in a SOT-23 surface mount package). The MMBV909L is a low voltage varactor suitable for UHF

applications; it is a dual back-to-back varactor in a SOT-23 package. This oscillator is tunable over a range of approximately 1.5 MHz (308.9 to 310.4 MHz) with the control voltage Vvco from the AFC. Figure 9 is a curve of LO frequency versus AFC Vvco.

This circuit is breadboarded using the custom PC board shown in Figures 12 and 13. The RF ground is VCC and RF path lengths are minimized. High quality surface mount components were used except where specified. The absolute values of the components used will vary with layout placement and component parasitics.

In the VCO circuit (Figure 8), R1 is the emitter bias resistor. R2 and R3 form the base bias circuit. C1 and C2 make up the Colpitts capacitive divider network. C3,C4, and CV are capacitive trimmers for L. Only one of the varactors in the MMBV909L is used in order to reduce the tuning range. The equivalent L, L' is the equivalent inductance considering the capacitors. The following equation shows this relationship.

(1) $X_{L'} = X_L - X_C = 2\pi fL - 1 / 2\pi fC$

where C is the equivalent capacitance of C3, C4, and CV.

To increase $X_{L'}$ and to lower the oscillator frequency, the equivalent capacitance is increased. The relationship for C is shown below.

(2) $C = C3 + ((C4)(CV))/ (C4 + CV)$

The oscillator tuning range is controlled by $\Delta X_{L'}$ resulting from the voltage variable ΔCV. C4 can be used to trim the range; C3 will provide a capacitive offset. The following equations by similarity to equations (1) and (2) above show this relationship.

(3) $\Delta X_{L'} = X_L - \Delta X_C$

(4) $\Delta C = C3 + ((C4)(\Delta CV))/(C4 + \Delta CV)$

The oscillator operating frequency may be estimated by the following equation which is derived from the basic equation for a parallel resonant LC network.

(5) $f = (0.159)/\left[\{[(C1)(C2)] / [(C1+C2)\, L']\}^{1/2}\right]$

Automatic Frequency Control

The MC13156 OOK receiver uses an AFC to adjust the VCO with respect to the RF in order to downconvert it to the desired IF frequency. The VCO's output frequency is adjusted by the output voltage from a transimpedance amplifier which doubles as the loop filter. The loop filter input is the current output provided by the frequency discriminator of the MC13156. Its I_{out} versus frequency response is set by the resonant frequency and bandwidth of the external quadrature tank circuit.

The loop filter is required to convert the output of the discriminator into a VCO control voltage. An op amp transimpedance amplifier configuration (Vout/Iin) suits this requirement well (see Figure 7). This amplifier is built using the MC33204 quad op amp which provides rail-to-rail performance with a single, low voltage supply, thereby allowing maximum VCO control. The AFC loop gain and settling time is set by the transimpedance amplifier feedback resistor and capacitor respectively. The values of these loop characteristics are left to the designer's discretion depending on the system requirements. Stable frequency acquisition responses within milliseconds have been achieved with the schematic values of this simple single-pole circuit. The closed loop frequency error is 12 kHz per 100 KHz change in RF frequency. A reference ranging from 0.3 to Vcc - 0.3 Vdc needs to be provided to the non-inverting input of the transimpedance amplifier. This provides 1) a bias to the discriminator output and 2) an offset to dc match the loop filter frequency versus voltage out response to VCO control characteristic. This loop was

designed for low side mixer conversion. Should the LO be above the RF, an inverter would be needed after the loop filter or the ground reference of the varactor can be taken to Vcc (AC ground).

The RLC values shown will tune the tank to 10.7 MHz and allow for approximately 400 kHz AFC tuning bandwidth. An adjustable coil is used to tune the quadrature detector. The resistor sets the bandwidth by lowering the Q of the LCR tank circuit. The following relationship shows how to calculate the response of the discriminator resonant tank.

(6) $Q = R/X_L$

for $R = 2.7k\Omega$; $X_L = 2\pi(10.7)(1.5) = 100.8\ \Omega$

then $Q = 26.8$

(7) $BW_{-3dB} = fo/Q$

thus, the -3dB Bandwidth = 10.7 MHz /26.8 = 400 kHz

Should the overall transmit/receive system be prone to extreme frequency drift, the quadrature coil circuit bandwidth may need to be increased to provide adequate tracking range.

IF Interstage Filtering

Ceramic bandpass filters are placed between 1) the mixer output and the IF amplifier input and 2) the IF output and the limiter input (see Figure 7). They allow improved sensitivity by bandwidth limiting the noise to the RSSI detectors, especially the limiter. The filters shown in the schematic have a 3 dB bandpass response centered at 10.7 MHz which is 280 kHz wide. Choice of IF filter bandwidth will affect the fidelity of the recovered baseband signals. As the data rate is increased, the filter bandwidth should be wider.

The filter bandwidth is affected by its source impedance and output load impedances which are 330 ohms. The MC13156 mixer and IF amplifier output impedances are 330 ohms to match the typical 10 .7 MHz ceramic filters. The IF amplifier and the limiter input impedances are 1.4Kohms so it is necessary to use a shunt resistor of 430 ohms to have an effective match. Note that the 430 ohm shunt resistors are connected to the decoupling pins of the IF and limiter amplifiers where they are AC grounded. If the termination is made directly to ground, the internal bias would be interrupted.

Data Recovery Circuit

The received OOK signal is converted from RF to baseband by the MC13156 RSSI function. The RSSI output sources a current to an external load connected to Vee to produce a voltage. The choice of this load resistance affects the receiver performance. Obviously, the resulting RSSI gain (Vout/RFin) is directly proportional to this load. When this load is large enough, the RSSI output will saturate, which compresses the high RF input end of the RSSI transfer response. A load of 47 Kohm is a good choice to obtain 70 dB of monotonic RSSI dynamic range with no compression. The load impedance chosen also affects the RSSI rise and fall times (see Figure 6). This must be considered for systems with data rates higher than 10 kHz.

For data rates of 10 kHz or less, 680 pF and 47k may be connected from pin 20 to Vee. These components form a low pass filter with its corner at approximately 10 kHz; this helps clean up the RSSI response under low signal conditions. Data rates up to 50 kHz have been achieved without low pass filtering.

The RSSI is AC coupled to the data slicer. In order to obtain good sensitivity of low data rate signals the coupling capacitor used in the application circuit is 0.47µF. For a higher data rate which remains constant a smaller capacitor may be used.

The data slicer can be disabled by connecting the data slicer hold pin to greater than 1.5 Vdc (Vcc will suffice). Should the receiver system be integrated with a transmitter, this will prevent any invalid data slicer output from causing any problems.

Layout and Practical Considerations

Figures 11 and 12 show the component placement and layout of the circuit side and ground side of the PCB used to demonstrate the OOK receiver. The artwork is supplied in Figures 13 and 14. The following layout considerations are suggested:

1) Use double sided PCB in which one side is the circuit side where all surface mounted component are placed and where the interconnect and circuit traces are done; the other side is the Vee ground side where leaded components are mounted and only a few necessary circuit traces are done.
2) Keep all RF traces as short as possible.
3) Avoid point-to-point wiring; it is best to run the trace on the PCB.
4) Use controlled impedance microstrip lines in high frequency portions of the circuit.
5) Use ground return paths through ample size holes to the ground side of the PCB.
6) Decouple Vee where the pins of the IC contact the trace on the PC board.

5. Performance in Application Circuit

An input carrier level of -85 dBm allows recovery of the PCM waveform without jitter or tearing at 2kbps (Figure 7 - OOK receiver). This may be improved approximately 20 dB by using a preamp and bandpass filtering before the mixer. Design of a preamplifier matching network should also consider interfacing to an antenna system. Since this is very "application specific" depending on the size and other physical constraints of the particular system, it is not considered part of the scope of this paper.

The pull-in range and hold-in range are dependent on the input drive level. In general under higher drive, the hold-in and pull-in ranges are greater. Figure 10 shows a plot of the hold-in range and pull-in range versus the RF input level. The pull-in range is consistent with the selectivity of the IF bandwidth.

The application circuit supports data rates up to 50 kHz . This has been confirmed in the lab with relaxed interstage and baseband filtering. The wider filtering is much more susceptible to interference.

6. Conclusions

The MC13156 is an excellent solution for a stable OOK receiver to fit Part 15 applications such as keyless entry and security systems where high reliability and performance is essential. The following performance attributes have been demonstrated and can be successfully integrated in a low cost OOK communication system.

The varactor controlled LC oscillator is capable of tuning over a suitable frequency range at low supply voltage. Driving the VCO with the AFC network provides compensation for expected transmitter carrier drift. This overcomes the need for an expensive crystal controlled transmitter/receiver system. Narrow band filters improve selectivity and assist in achieving the receiver's low sensitivity of -85 dBm (without a preamplifier or preselector filter). Data recovery using the MC13156 patented data slicer enhances the exceptional sensitivity of the receiver by extending the RSSI dynamic range. Low cost is accomplished with only three ICs and a minimum number of external components.

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Figure 1 - Typical SAW Resonator ASK Transmitter

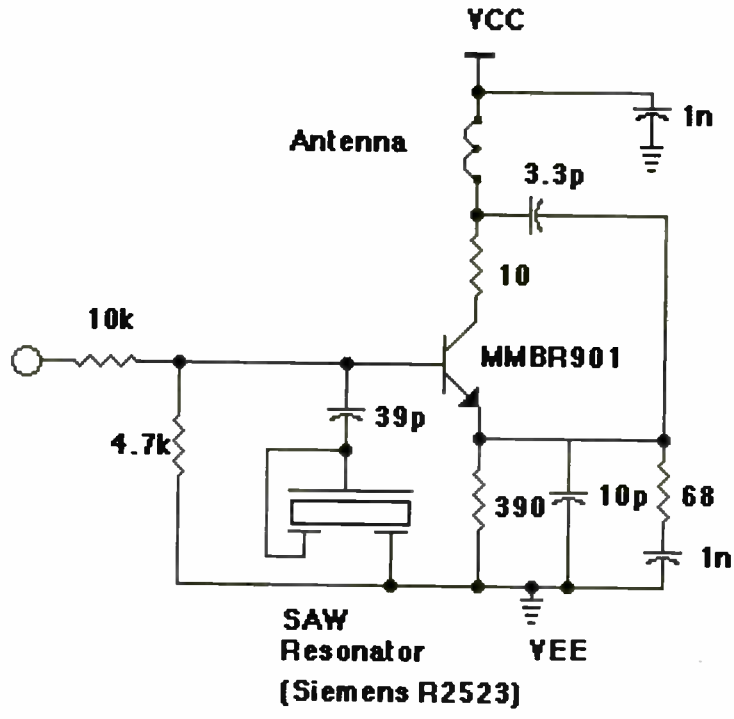


Figure 2 - Tuned Radio Frequency Receiver

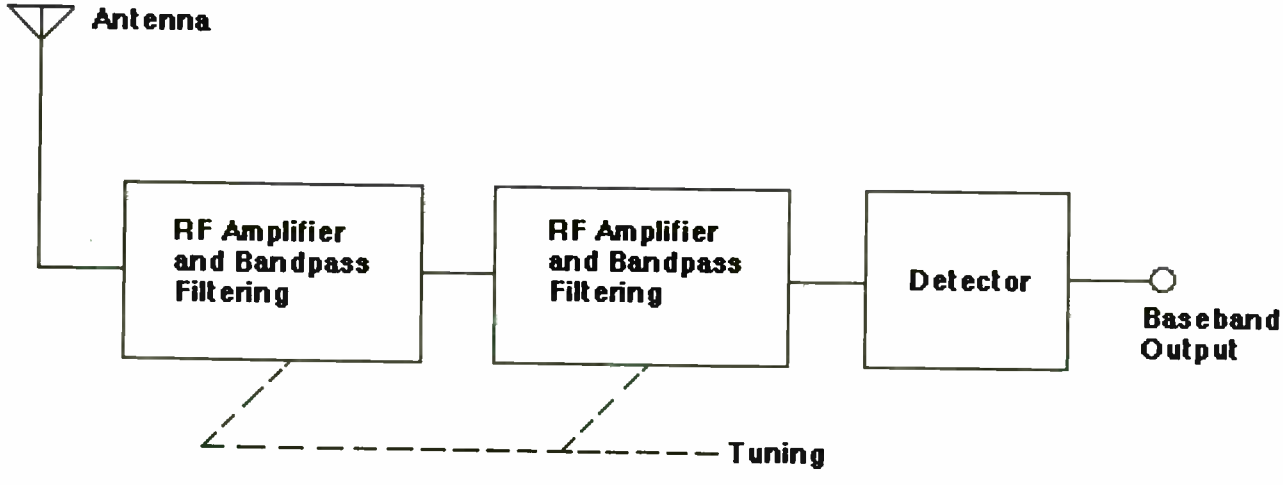


Figure 3- OOK RECEIVER BLOCK DIAGRAM

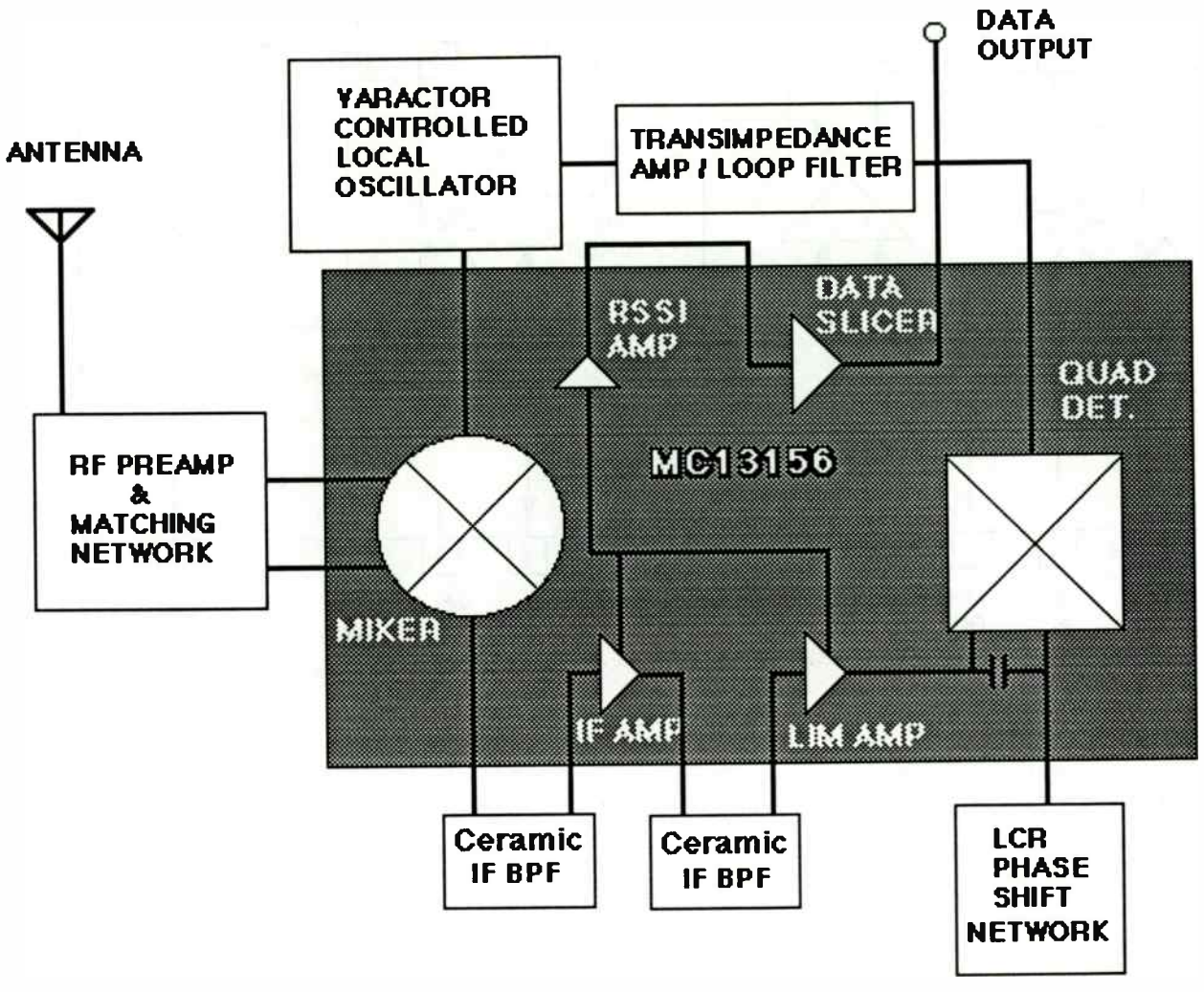


Figure 4 - MC13156 Block Diagram

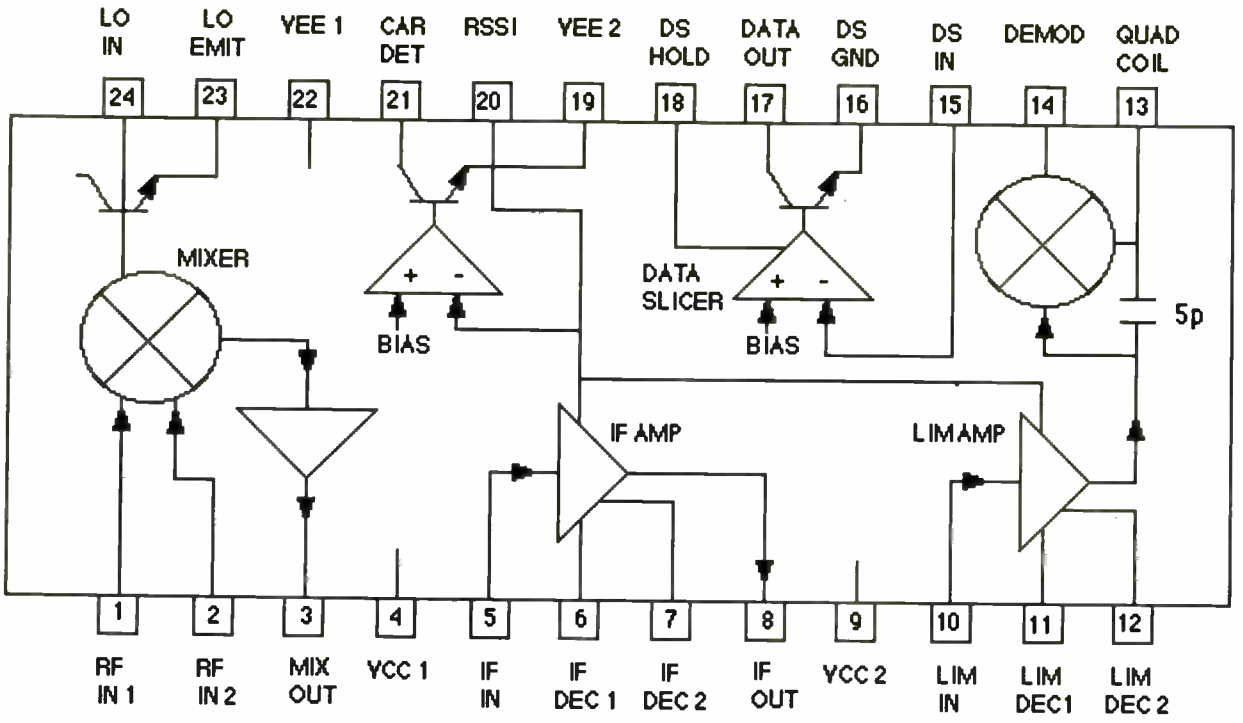
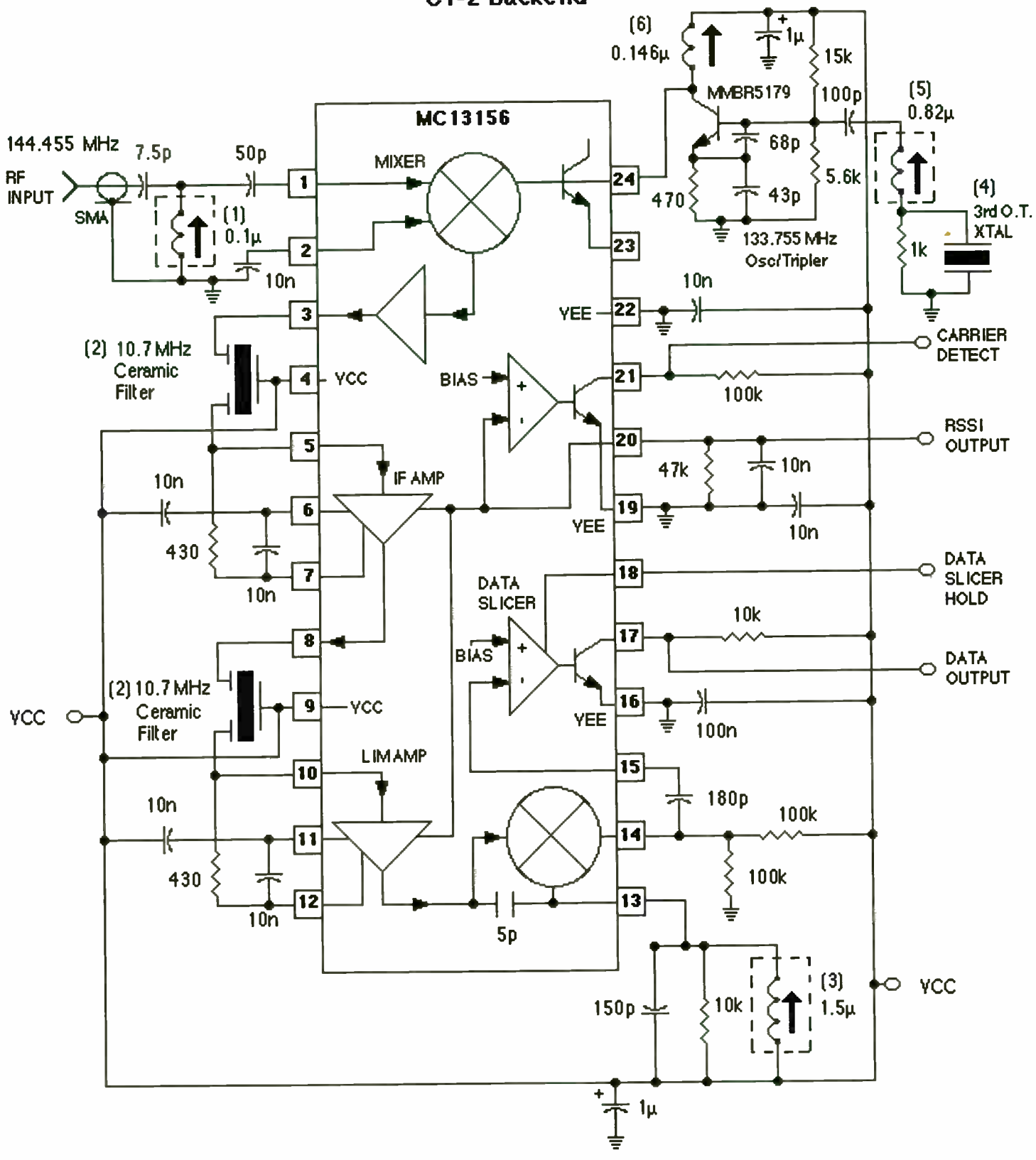


Figure 5 - MC13156DW APPLICATION CIRCUIT
CT-2 Backend



Notes:

(1) 0.1 µH Variable Shielded Inductor: Coilcraft Part # M1283-A or Equivalent.

(2) 10.7 MHz Ceramic Filter: Toko Part # SK107M5-AO-10X or Murata Erie Part # SFE10.7MHY-A

(3) 1.5 µH Variable Shielded Inductor: Toko Part # 292SNS-T1373

(4) 3rd Overtone, Series Resonant, 25 PPM Crystal at 44.585 MHz.

(5) 0.814 µH Variable Shielded Inductor: Coilcraft Part # 143-18J12S

(6) 0.146 µH Variable Inductor: Coilcraft Part # 146-04J08

Figure 6 - RSSI Output Rise and Fall Times versus RF Input Signal Level

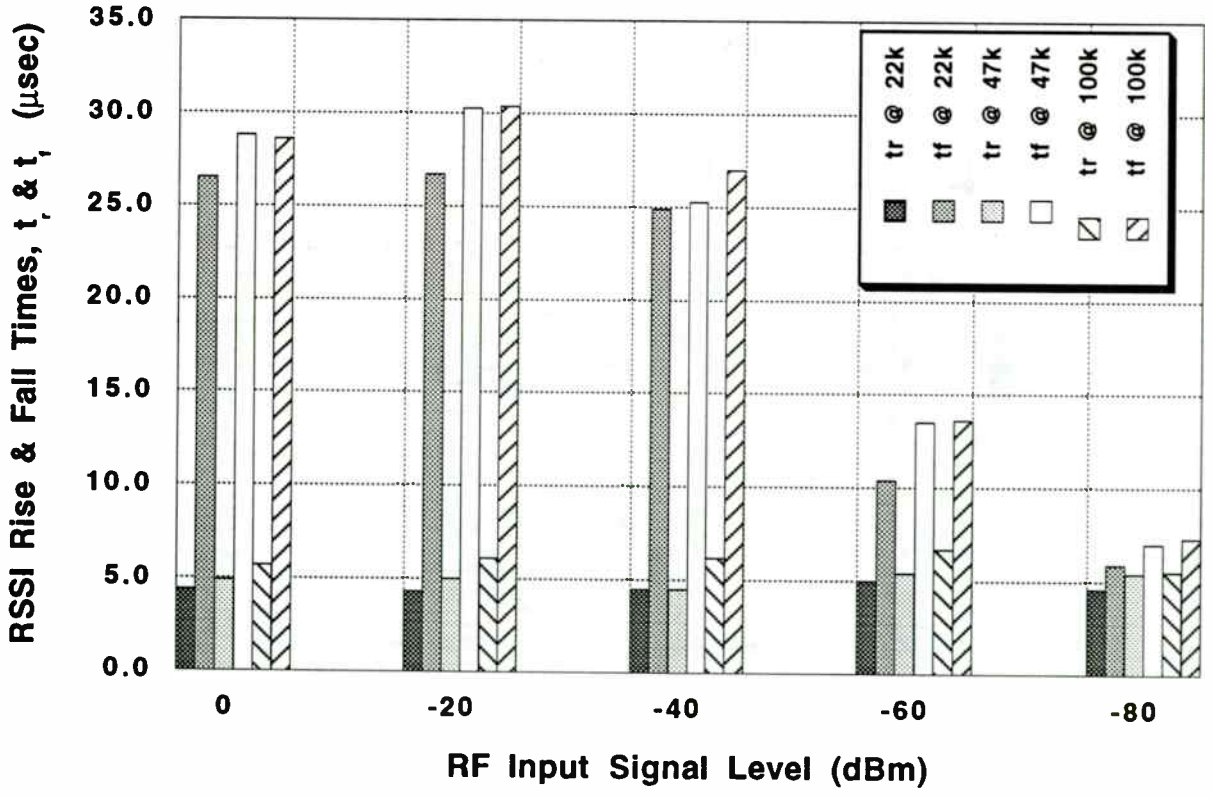
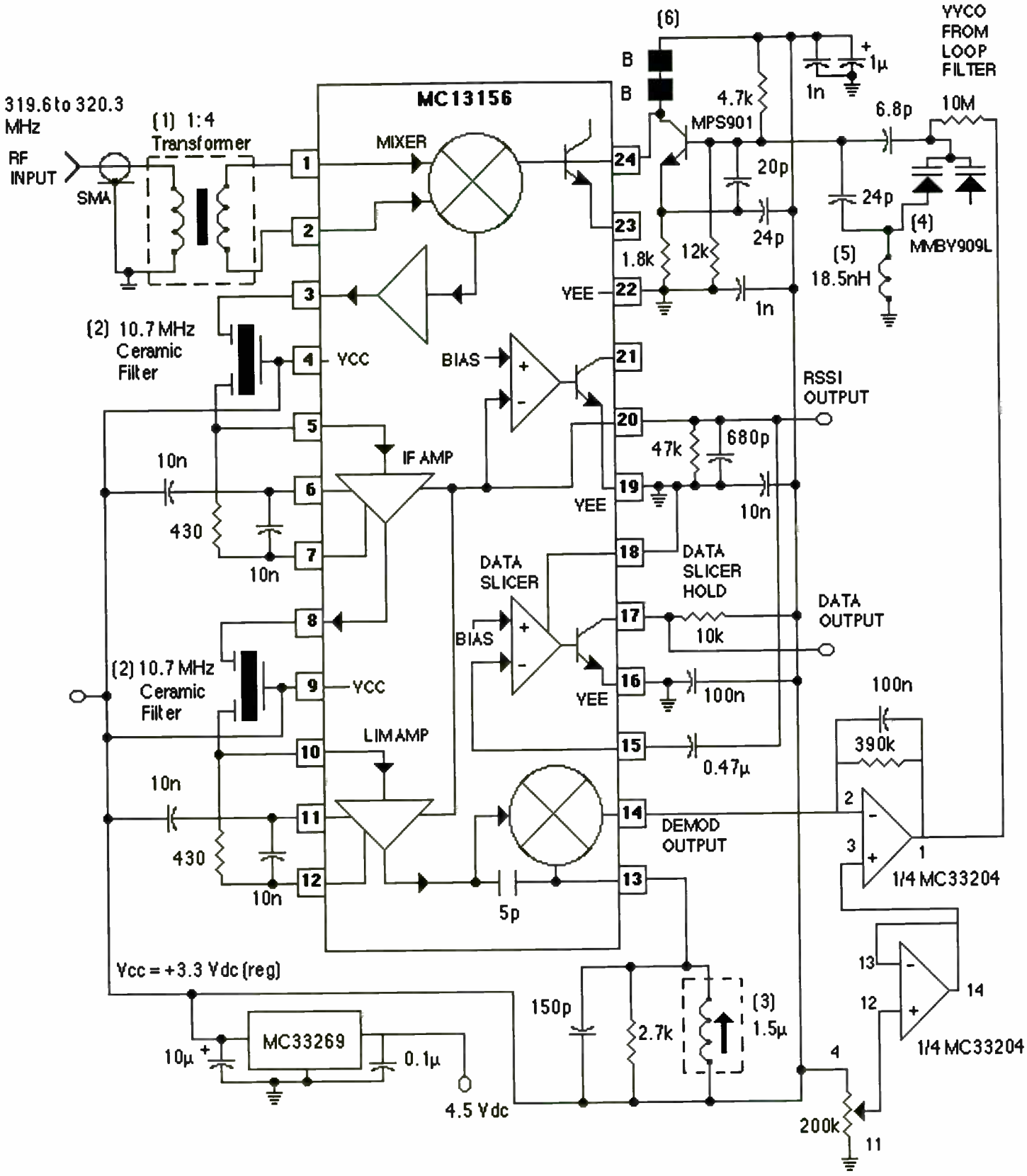


Figure 7 - MC13156DW OOK RECEIVER



Notes:

(1) 1:4 Impedance Transformer: Sources are Mini-Circuits and Coilcraft.
(2) Ceramic Bandpass Filter (Murata Part # SFE10.7MJA10-A); 330 Ω Source and Load Impedances.
(3) 1.5 µH Variable Shielded Inductor: Toko Part # 292SNS-T1373 or Equivalent.
(4) Dual Varactor in SOT-23 Package.
(5) Coilcraft Part # AO5T- Spring coil; Face Value 18.5nH at 150 MHz.
(6) Ferrite Beads with a Short length of 20AWG Wire

Figure 8 - External Varactor Controlled LC Oscillator

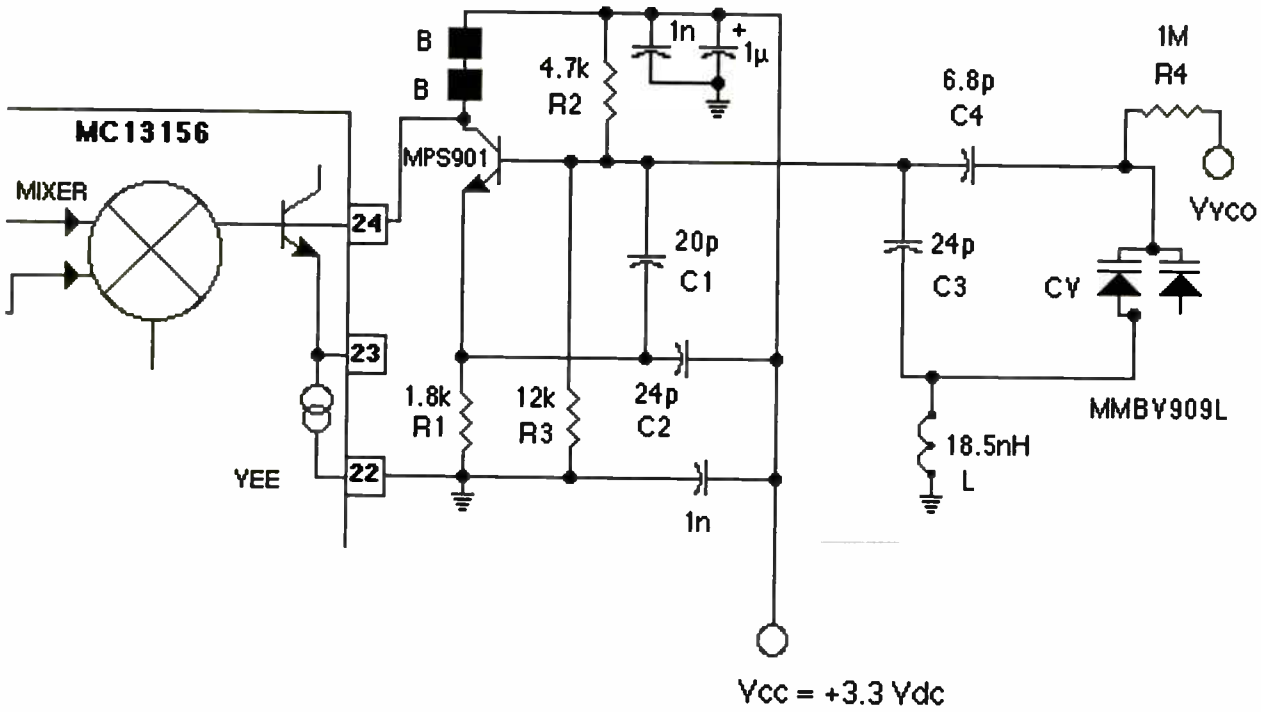


Figure 9 - VCO Frequency versus VCO Control Voltage

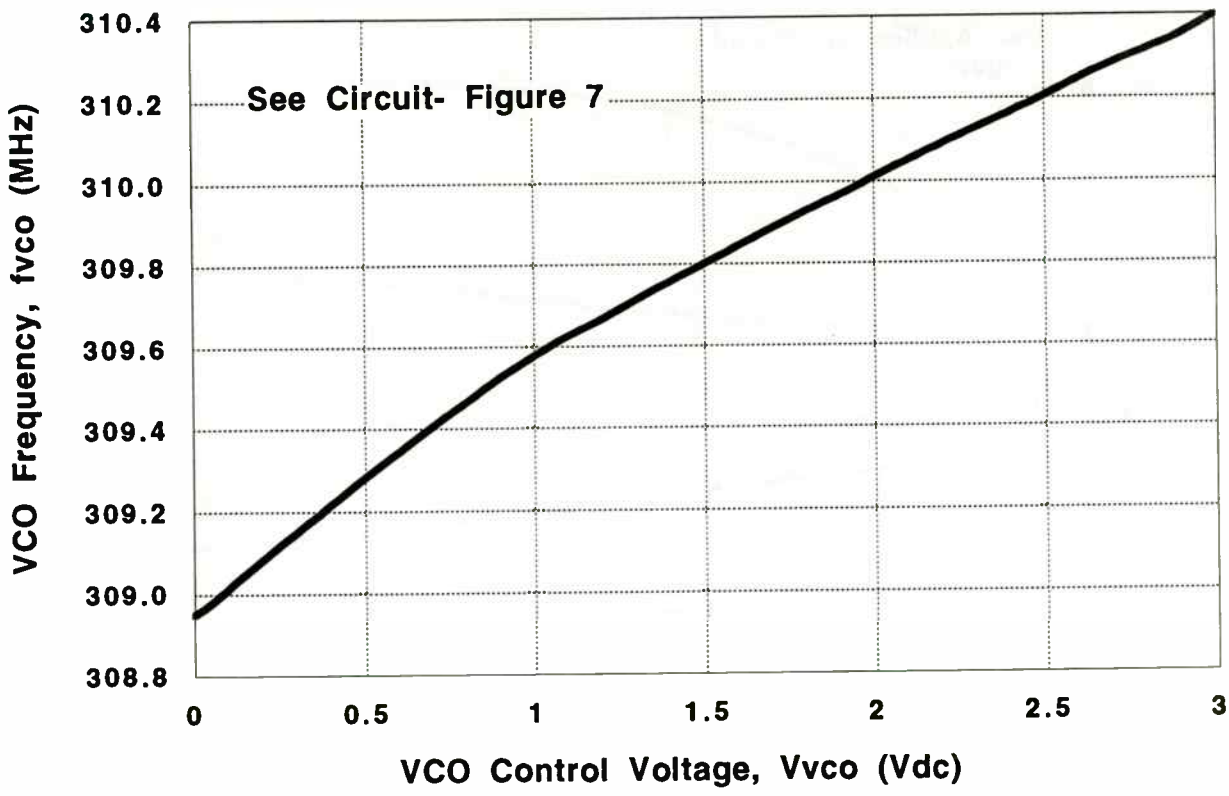
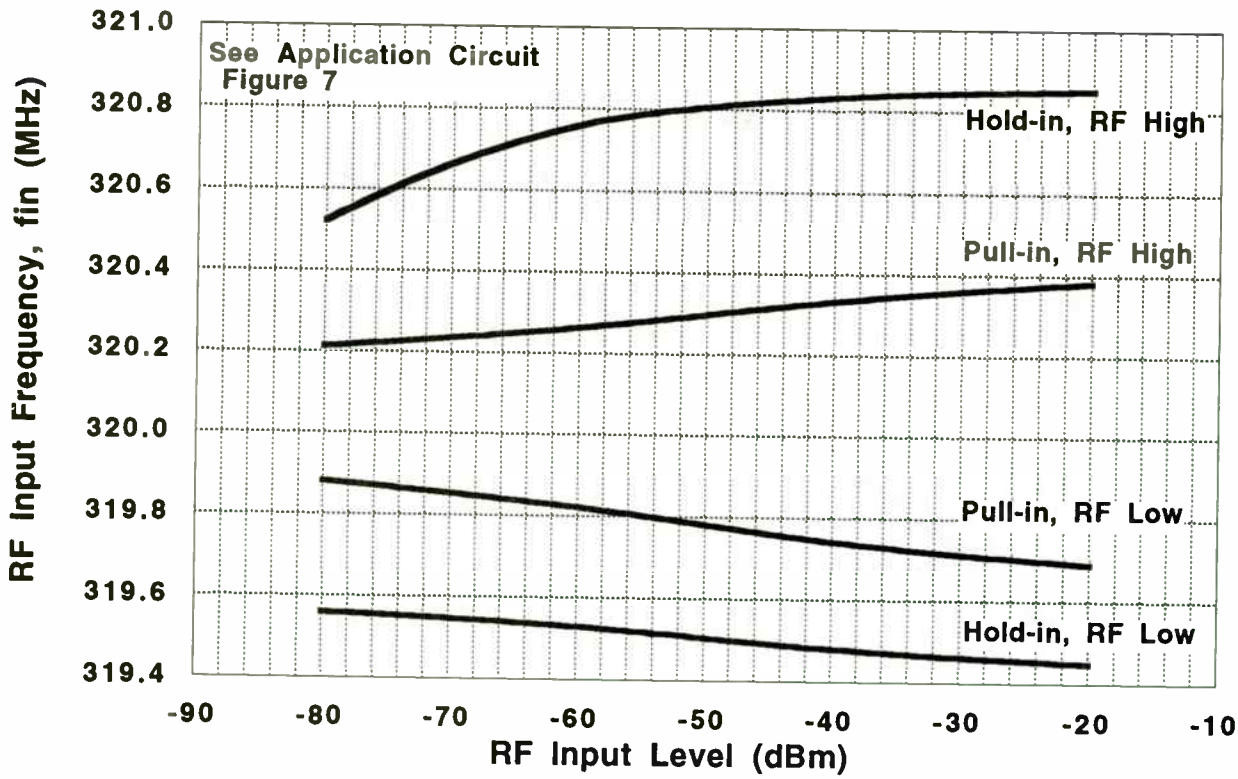


Figure 10 - AFC Capability: Hold-in and Pull-in Limits versus RF Input Level



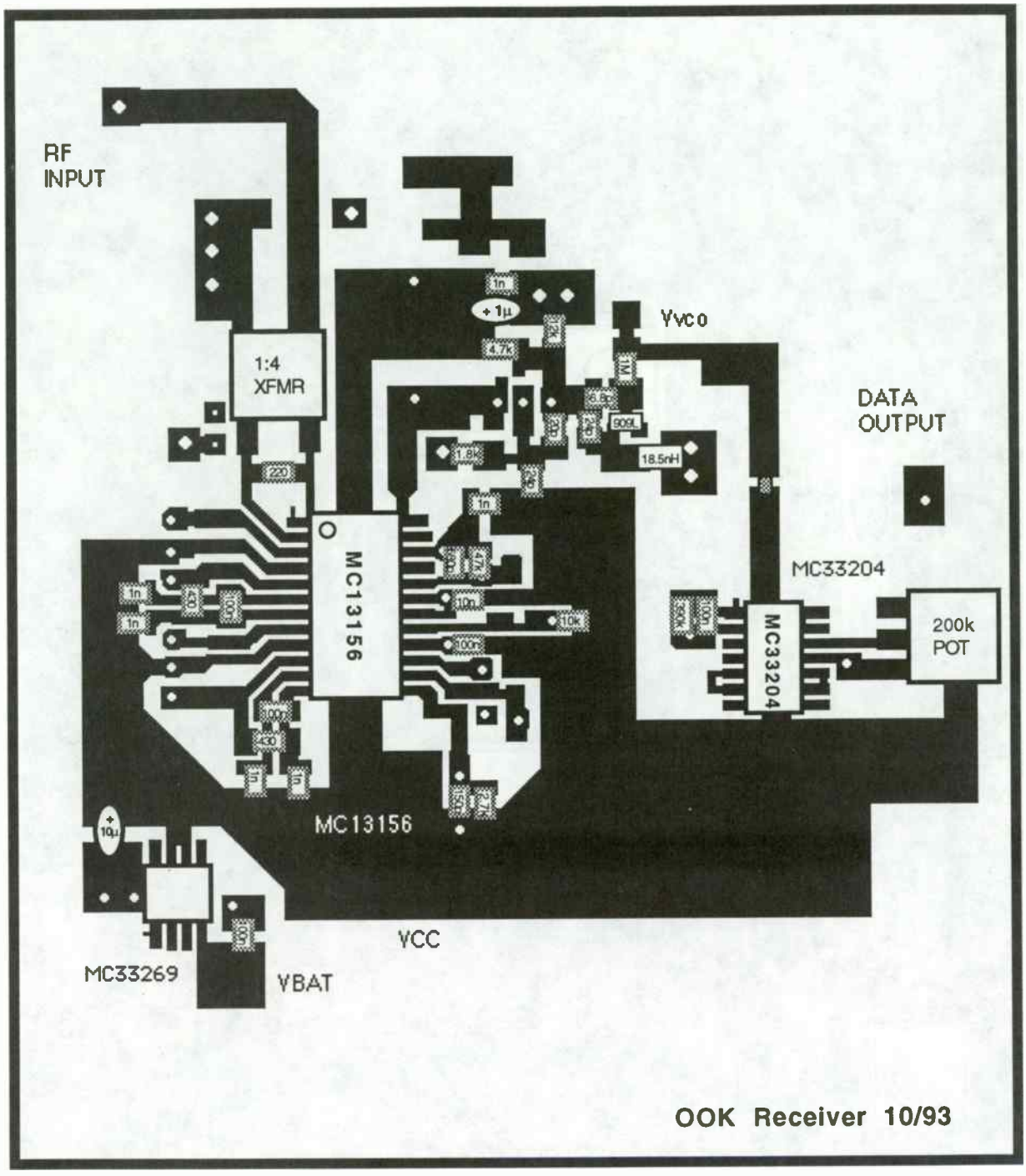


Figure 11 - Circuit Side Component Placement

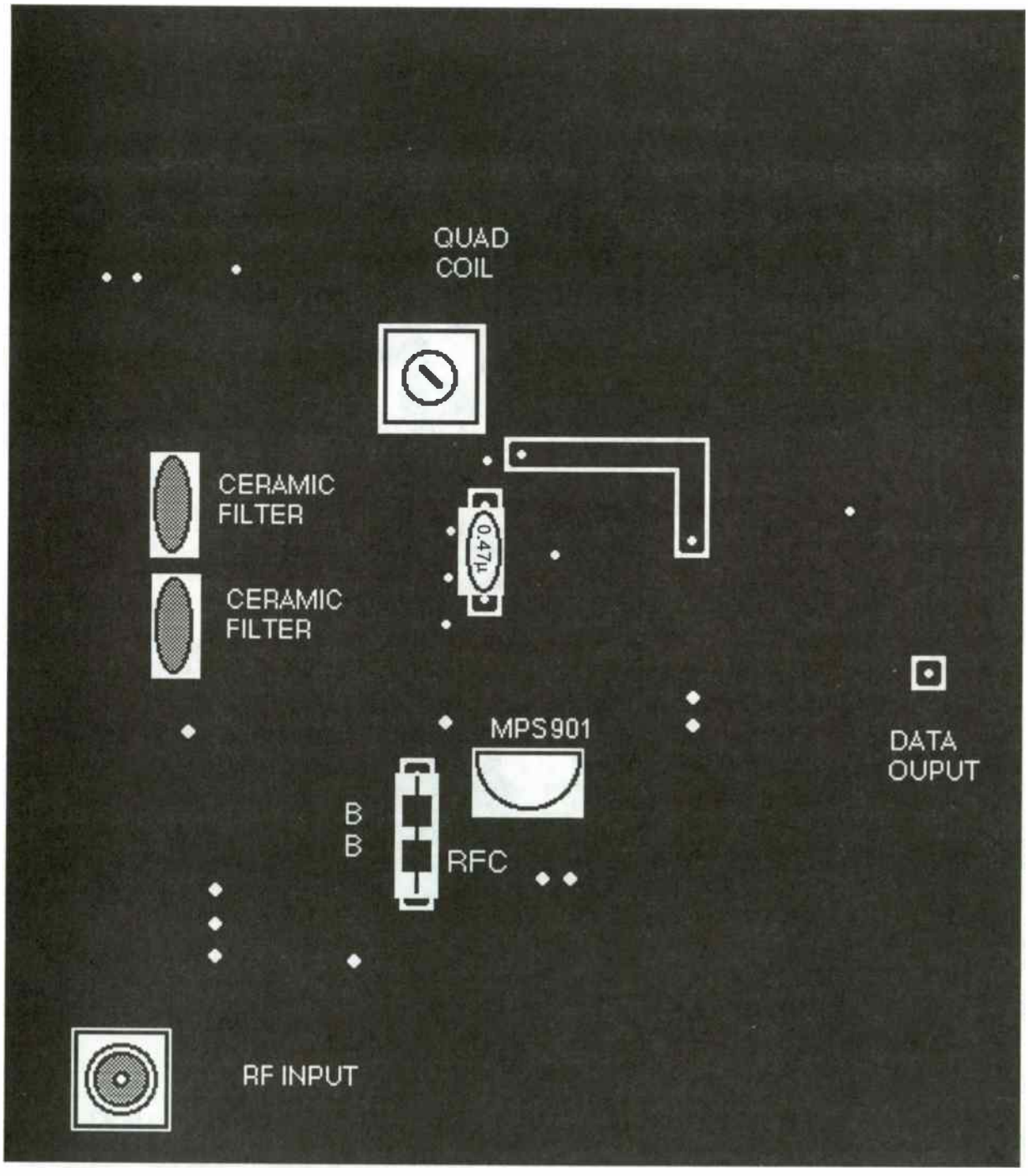


Figure 12- Ground Side Component Placement

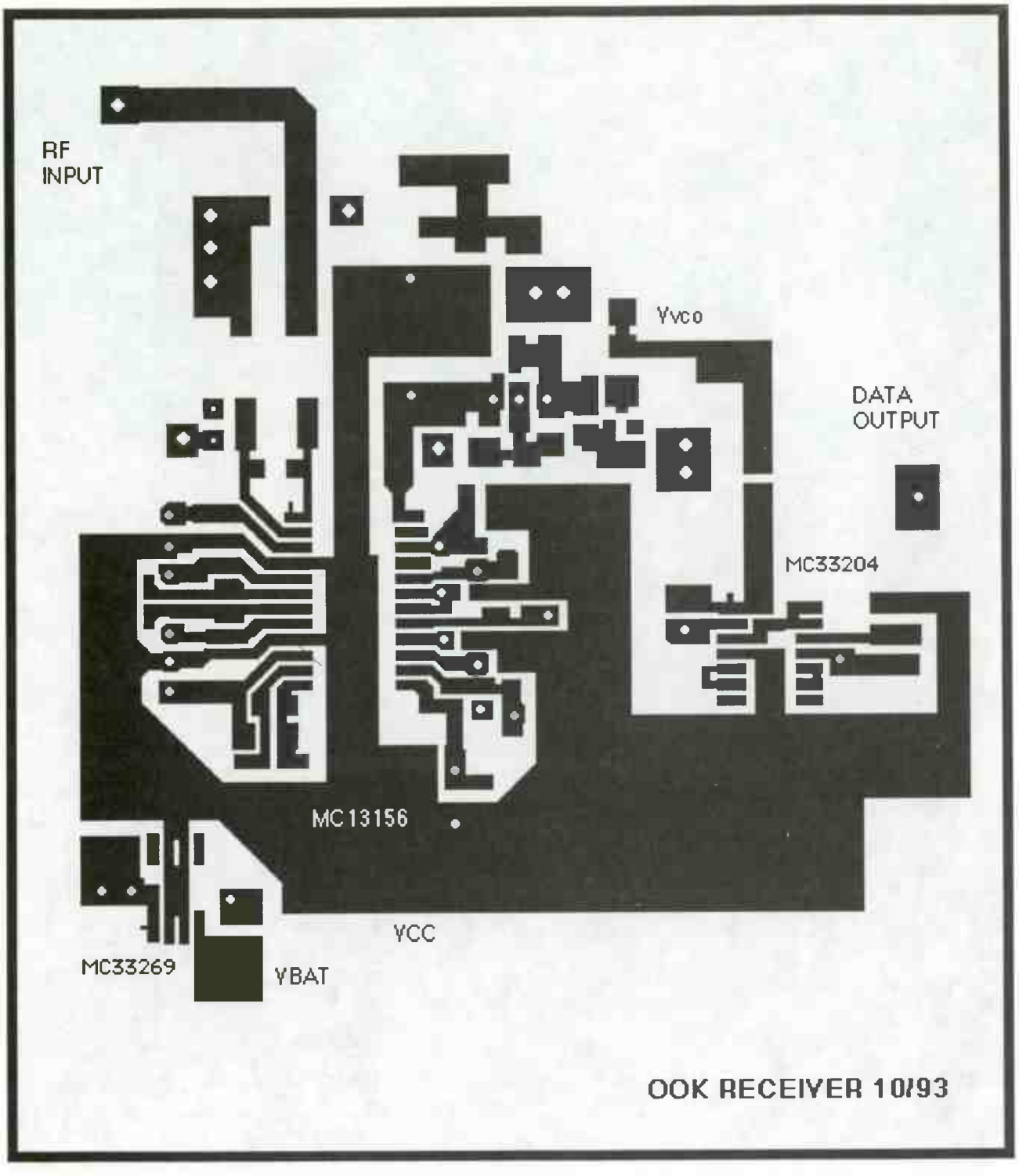


Figure 13 - Circuit Side View

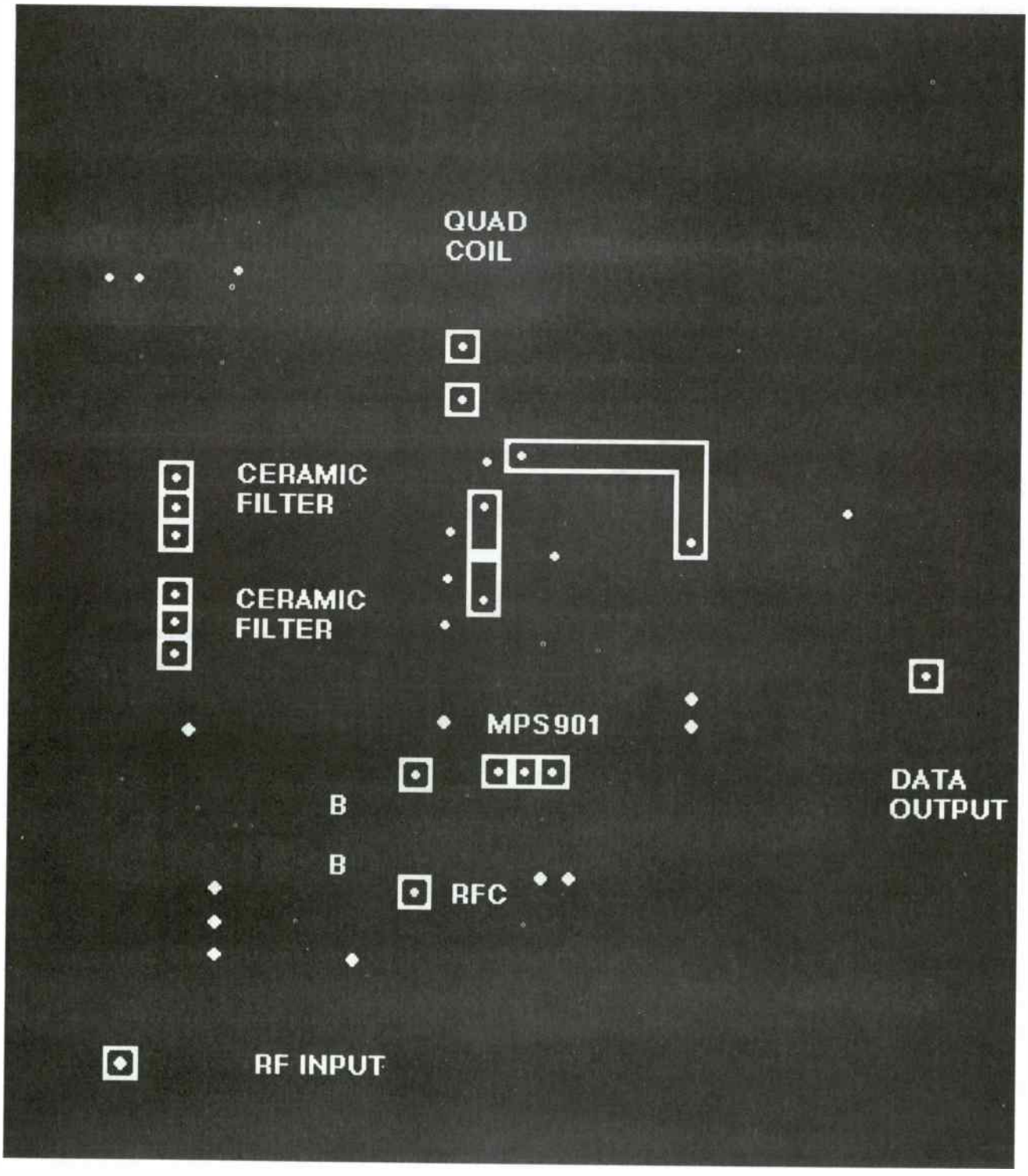


Figure 14 - Ground Side View

A High-Rate Direct-Sequence Spread-Spectrum Demodulator ASIC

Sam Kingston, Steve Barham
Glen Rattlingourd, Harold Simonsen
Ayyoob Abbaszadeh, Randal Sylvester

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Abstract

This paper describes a high-rate spread-spectrum demodulator architecture and ASIC (application-specific integrated circuit) implementation that offers the inherent advantages of digital signal processing, such as precise parameter control and elimination of analog tuning, with the added advantage of higher chipping rates than conventional oversampling methods. This architecture has been implemented in a 1.0 micron CMOS ASIC that provides chipping chipping rates up to 32 Mcps over the full military temperature range. Unisys calls this device the PA-100™. The key features that allow processing at 1 sample per chip include complex baseband sampling and novel circuits for chip-rate matched filtering and timing error detection. The architecture includes all required functions for spread spectrum signal acquisition and tracking, such as a 2nd order carrier recovery loop (CRL), a 2nd order code lock loop (CLL), a PN code sequential detector (with an external matched filter option), symbol synchronization circuitry, and automatic gain control (AGC). The architecture also includes dual 16-stage PN generators (with optional external inputs), and supports BPSK, QPSK, OQPSK, Bi-BPSK, MSK, and other modulation formats. All operational parameters are continuously variable via a standard 8-bit controller interface.

Introduction

The use of digital signal processing (DSP) techniques for implementing various functions within communication receivers has been growing steadily for over three decades [1-3]. The advantages of using DSP techniques are well-known and include elimination of parameter drift and tuning problems, a high degree of versatility, and very predictable and repeatable performance. In addition, improvements in semiconductor technology have produced remarkable increases in speed and density, and equally impressive decreases in size and cost, allowing DSP-based systems to provide a cost-effective solution for an increasingly broad range of communication applications.

One of the fundamental limitations of DSP approaches is the maximum processing rate of the digital circuitry. For example, in a direct-sequence spread-spectrum (DSSS) application, many current DSP approaches require a minimum of 2 to 4 samples for every PN (pseudo-noise) chip. This is particularly true for systems that use a free-running clock, since the timing resolution of the entire system is limited to the system clock times. The consequence of over-sampling the PN chips is a limit on the maximum chipping rate, and therefore on the spread spectrum processing gain (the ratio of chipping rate to data rate). This limitation is acceptable in some applications, however it can represent a significant problem for applications that require maximum interference rejection.

This paper presents a DSSS architecture and ASIC implementation that can operate at a rate of 1 sample per chip, providing the maximum chipping rate possible for a given digital technology. The architecture also provides nearly optimum bit error rate performance (typically less than 1 dB from theoretical results), and is suitable for unspread or spread BPSK (binary phase-shift keying), QPSK (quadriphase shift keying), OQPSK (offset QPSK), MSK (minimum shift keying), Bi-BPSK (bi-orthogonal phase shift keying), and other modulation types. Data rates and chipping rates can be continuously varied from nearly DC

up to the maximum rate of the digital technology.

Demodulator System Configuration

A simplified block diagram of a typical DSSS demodulator based on the PA-100™ ASIC is provided in Figure 1. As shown in Figure 1, the received carrier or IF signal is down-converted to near-baseband with an analog quadrature downconverter. Since a free-running local oscillator is used, there will be a residual frequency and phase error on the signal, which will be removed downstream by the HRDS ASIC. Following down-conversion, the near-baseband signals are filtered with simple RC filters, and then sampled and quantized by analog-to-digital converters (ADCs). The samples are then processed by the PA-100™ ASIC, which performs all remaining signal processing. Note that the PA-100™ provides a control signal for the analog AGC to minimize the quantization error at the ADCs. The PA-100™ also provides a control signal to the programmable clock generator (typically a numerically-controlled oscillator) to align the ADC sample clock with the incoming chips. A simple 8-bit controller is often used to configure the PA-100™ and to monitor the status of the acquisition and tracking procedures.

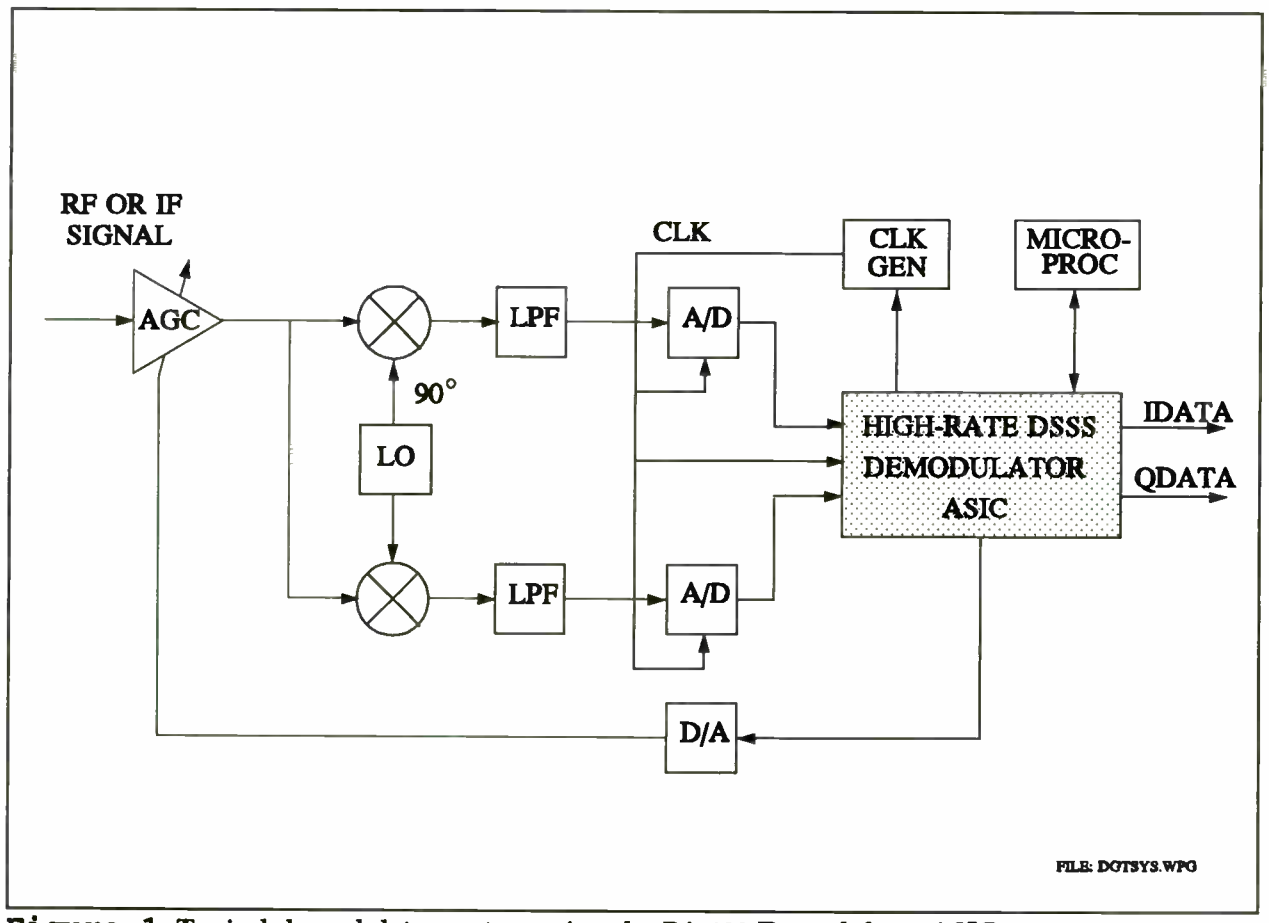

Figure 1. Typical demodulator system using the PA-100 Demodulator ASIC.

ASIC architecture

A simplified block diagram of the PA-100™ is provided in Figure 2. The main functions performed within the ASIC include chip-rate and symbol-rate matched filtering; estimation and removal of residual frequency and phase errors; acquisition, tracking, and removal of the PN code; chip and symbol timing recovery; and automatic gain control. The entire architecture is designed to operate at a maximum rate of 1 sample per chip, although it is also capable of oversampling the chips to accomodate lower chipping rates and reduce external circuitry requirements.

Chip-rate matched filtering of the I and Q signals is accomplished by using single-tap FIR (Finite-Impulse

Response) filters shown in Figure 2 in series with the analog RC filters that are depicted in Figure 1. The FIR filter effectively removes the inter-chip interference caused by the RC filter, and the over-all result closely approximates the response of a chip-rate integrate-and-dump (IAD) matched filter. This method is described in [4]. In theory, the performance of the filter can be made arbitrarily close to ideal by increasing the ratio of τ/T_c, where τ is the RC time constant, and T_c is the nominal chip time. In practise, the size of this ratio is limited by the dynamic range of the ADC. When using a 6- or 8-bit ADC and a τ/T_c ratio of 4, the measured degradation compared to an ideal IAD matched filter is less than 1.0 dB, as shown by the measured data shown in Figure 3.

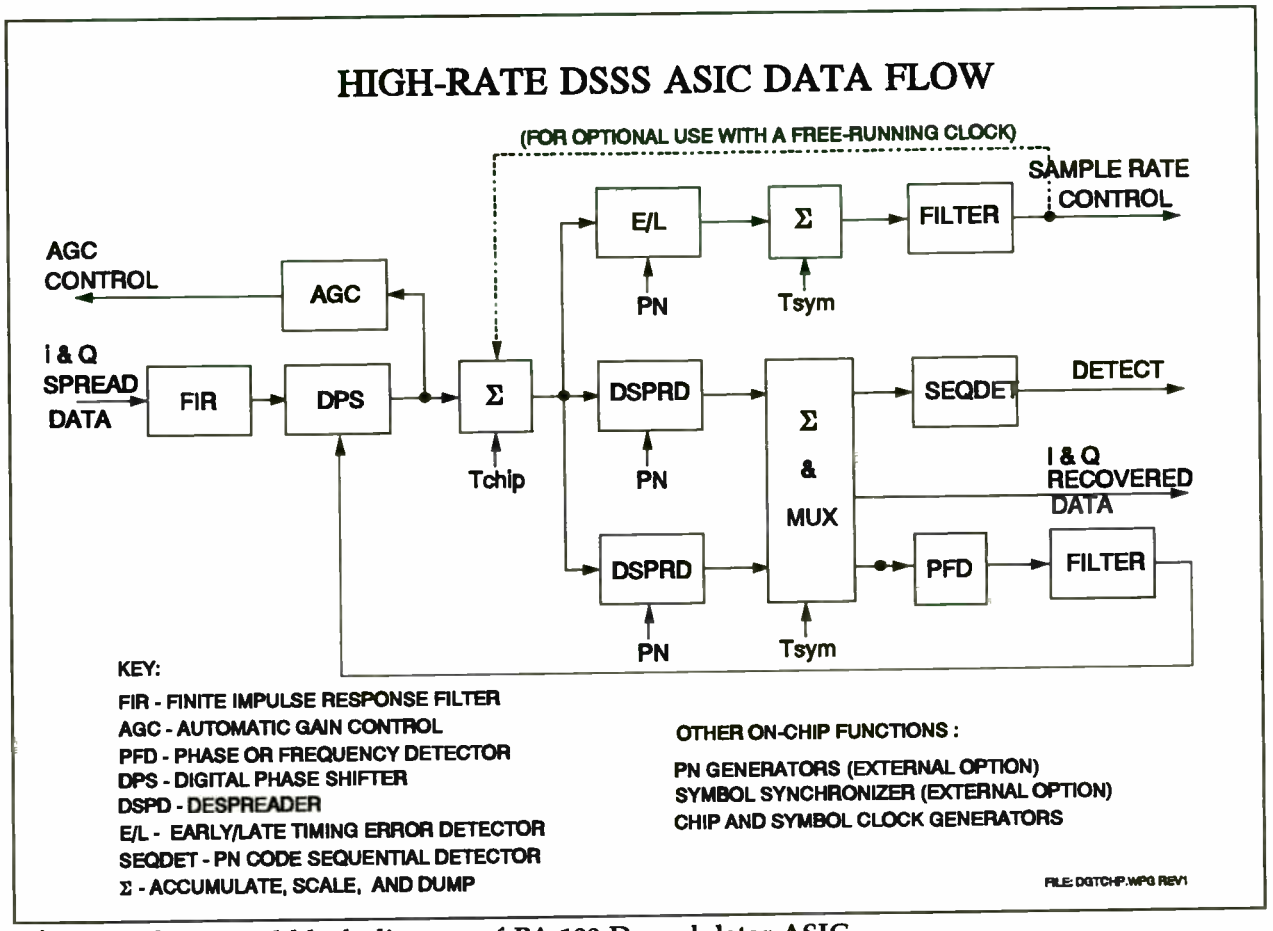

Figure 2. Internal block diagram of PA-100 Demodulator ASIC.

Following the chip-rate matched filter, the resulting I and Q signals are processed by a digital phase shifter (DPS), which is used to remove residual frequency and phase errors that are a consequence of using a free-running local oscillator in the down-conversion process. If the I and Q signals are viewed as a complex vector, the DPS performs vector rotations, producing an output that is (approximately) free from the effects of frequency and phase errors. Simulations and test results have demonstrated less than 1 dB degradation for doppler rates up to approximately 0.25 times the sample rate with this configuration. As depicted in Figure 2, the DPS is the control element in a 2nd order digital phase locked loop (DPLL). The loop also includes a programmable loop filter and a phase/frequency detector (PFD). Typically, frequency detection is selected during initial acquisition, and phase detection is used once the signal frequency has been successfully acquired.

As depicted in Figure 2, the architecture also includes chip and symbol timing recovery circuitry. Chip timing recovery is accomplished with a 2nd order loop that uses an external clock generator as the control element, as noted previously. The timing error detector uses a method that is described in [5], which performs correlations of early and late data with the on-time PN code. This approach offers the advantage of 1-sample-per-chip operation, in contrast to traditional early-late gate techniques that require a minimum of 2 samples per chip [6]. Symbol timing is obtained by using programmable counters to generate symbol clocks, with symbol transitions normally synchronized to a known PN code state (epoch). For other synchronization schemes, provisions are made for using external symbol synchronizers.

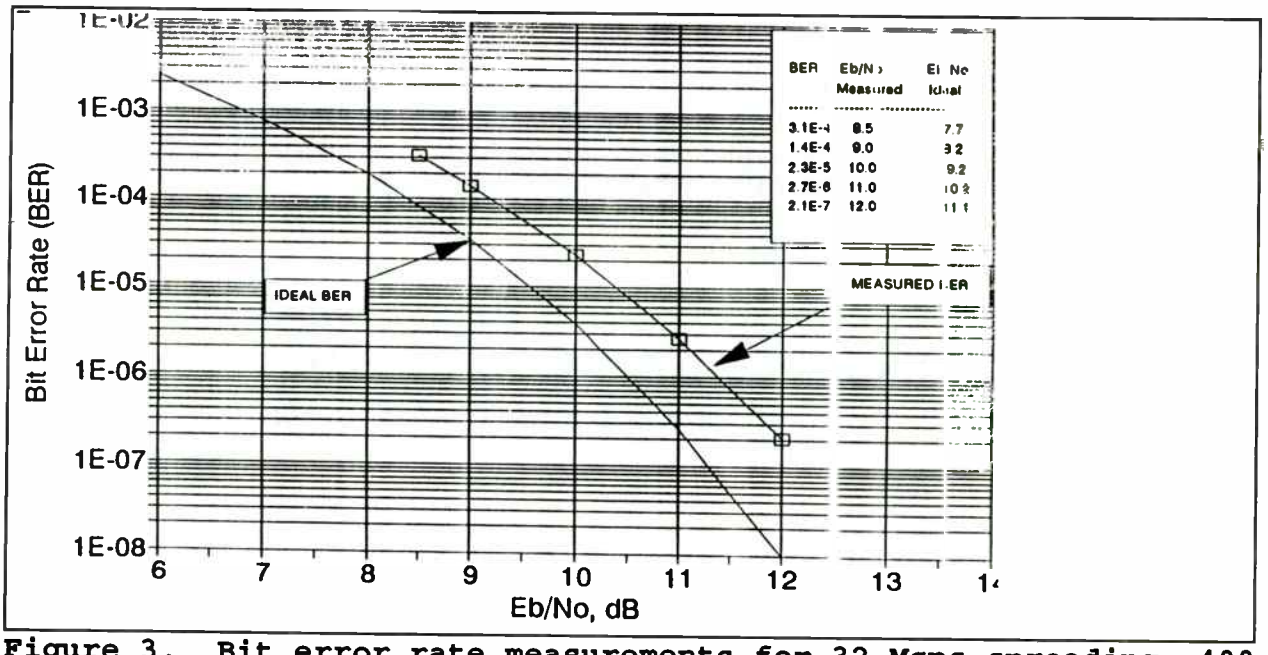

Figure 3. Bit error rate measurements for 32 Mcps spreading, 400 bps data, BPSK modulation.

PN code acquisition can be accomplished using the on-chip sequential detector depicted in Figure 2, or with an external matched filter. The sequential detector has programmable thresholds and dwell times, and requires less circuitry. However, an external matched filter can provide faster acquisition, at the cost of additional hardware. The PN codes used for despreading can be obtained from the on-chip 16-stage LFSR (linear feedback shift register) PN generators, or from external code generators (e.g. for transec applications). This architecture provides two independent complex despreaders and a multiplexer as depicted in Figure 2. This allows the chip to search for an alternate code or code epoch while data decisions and tracking loops use a previously-acquired code. This architecture can be used to reduce the acquisition time for long codes, or to search for alternate time shifts of the same code due to multi-path effects or multiple antennas.

Conclusion

A novel architecture and an ASIC implementation have been presented for DSSS systems. This approach offers well-known advantages of using DSP, such as no parameter drift, and highly repeatable performance. The architecture also provides chipping rates up to the system clock rate, and a high level of versatility in terms of modulation formats, chipping and data rates, acquisition procedures, and tracking modes. The PA-100™ has been successfully tested at the chip and system level, with typical performance typically less than 1.0 dB from theoretical, as shown by the BER results in Figure 3.

References

[1] George L. Turin, "An Introduction to Digital Matched Filters," Proceedings of the IEEE, VOL. 64, No. 7, July 1976, p. 1092-1112.

[2] William C. Lindsey, and Chak Ming Chie, "A Survey of Digital Phase-Locked Loops," Proceedings of the IEEE, Vol. 69, No. 4, April 1981, p. 410-431.

[3] Francis D. Natali, "AFC Tracking Algorithms," IEEE Transactions on Communications, Vol. COM-32, No. 8, August 1984.

[4] Samuel C. Kingston, "Variable Rate Rectangular Matched Filter," U.S. patent no. 4,808,939.

[5] Samuel C. Kingston, Steven T. Barham, and Harold Simonsen, "Digital Time Error Signal Generator," U.S. patent no. 5,128,958.

[6] J.K. Holmes, Coherent Spread Spectrum Systems, Chapter 12, John Wiley & Sons, Inc, New York, 1982.

RFID/Personal Communications

Session Chairperson: Paul Khanna,
Avantek, Inc. (Santa Clara, CA)

Digital RF/ID Enhances GPS

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Forms of radio frequency identification (RF/ID) have been used since WWII. But because of their large size, the high cost of these systems and the lack of industry standards, few applications were developed for this technology. Instead, bar code and magnetic stripe became the primary technologies for automatic data collection. However, these technologies require human interface and cannot be used effectively in harsh environments and places where humans are uncomfortable.

RF/ID systems can be used to collect data in more harsh environments and for applications where there is no line-of-sight between the reader and the tagged object, or in cases where the object lacks a suitable surface for bar code labels such as:

- in dirty environments or in temperatures up to 200°C where bar codes could become unreadable and the environment too harsh for humans
- for livestock, lumber, or inventoried parts that cannot easily be labeled or placed in a scanner's line-of-sight at a predictable depth of field
- when security is a concern. RF tags, unlike bar codes, are very difficult to counterfeit and they are extremely accurate. Calculated error rates are as low as 1 in 100 trillion.

Recent advances in RF/ID technology have produced an efficient, compact, lower cost system that can be linked to GPS. This technology will revolutionize surveillance and tracking systems and could make RF/ID the chosen technology for automatic data capture in law enforcement and the shipping industry.

Using an RF/ID system linked to GPS, drug enforcement officials could clandestinely monitor the trip log of a truck crossing a border without physically connecting to the truck's GPS track log. GPS data from an RF/ID tag attached to the truck or its contents could be downloaded from a roadside interrogator at the border crossing. As the truck drives by, the interrogator would automatically download the GPS track log. The digital interrogator could be used to clandestinely track shipments across a border.

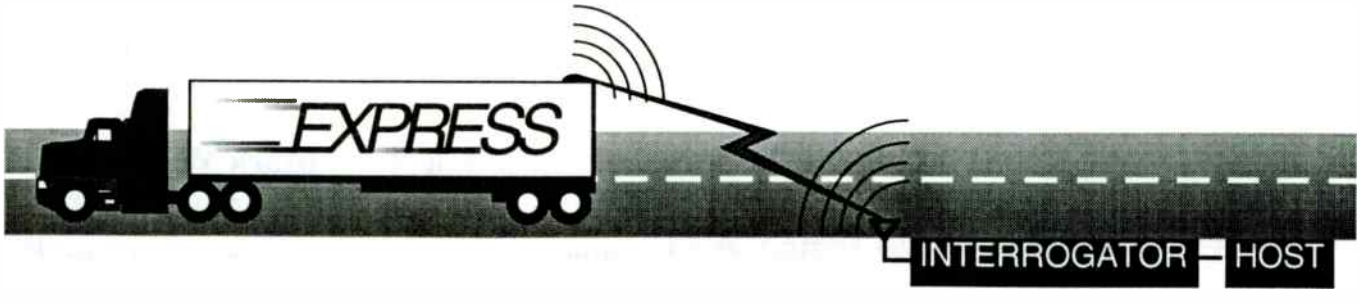

Figure 1. Remote track logging can be used in clandestine surveillance operations.

An RF/ID tag could be used with GPS to track stolen vehicles. A mobile interrogator inside a patrol car could monitor traffic on the freeway. The tag on the stolen vehicle would respond to the remote interrogator and covertly identify the vehicle as it drove by the patrol car. Once the vehicle was identified, the GPS track log information could be automatically downloaded to give authorities the exact route of the stolen vehicle.

GPS RF/ID systems could also have useful commercial applications for shipment or inventory tracking. For example, a base station at corporate headquarters could locate tagged shipments and get their exact GPS location by querying the interrogator on-board the truck or ship transporting the freight. And this system has other applications such as:

- inventory and process control
- materials resource planning
- important shipment, hazardous waste, or highly sensitive material tracking.

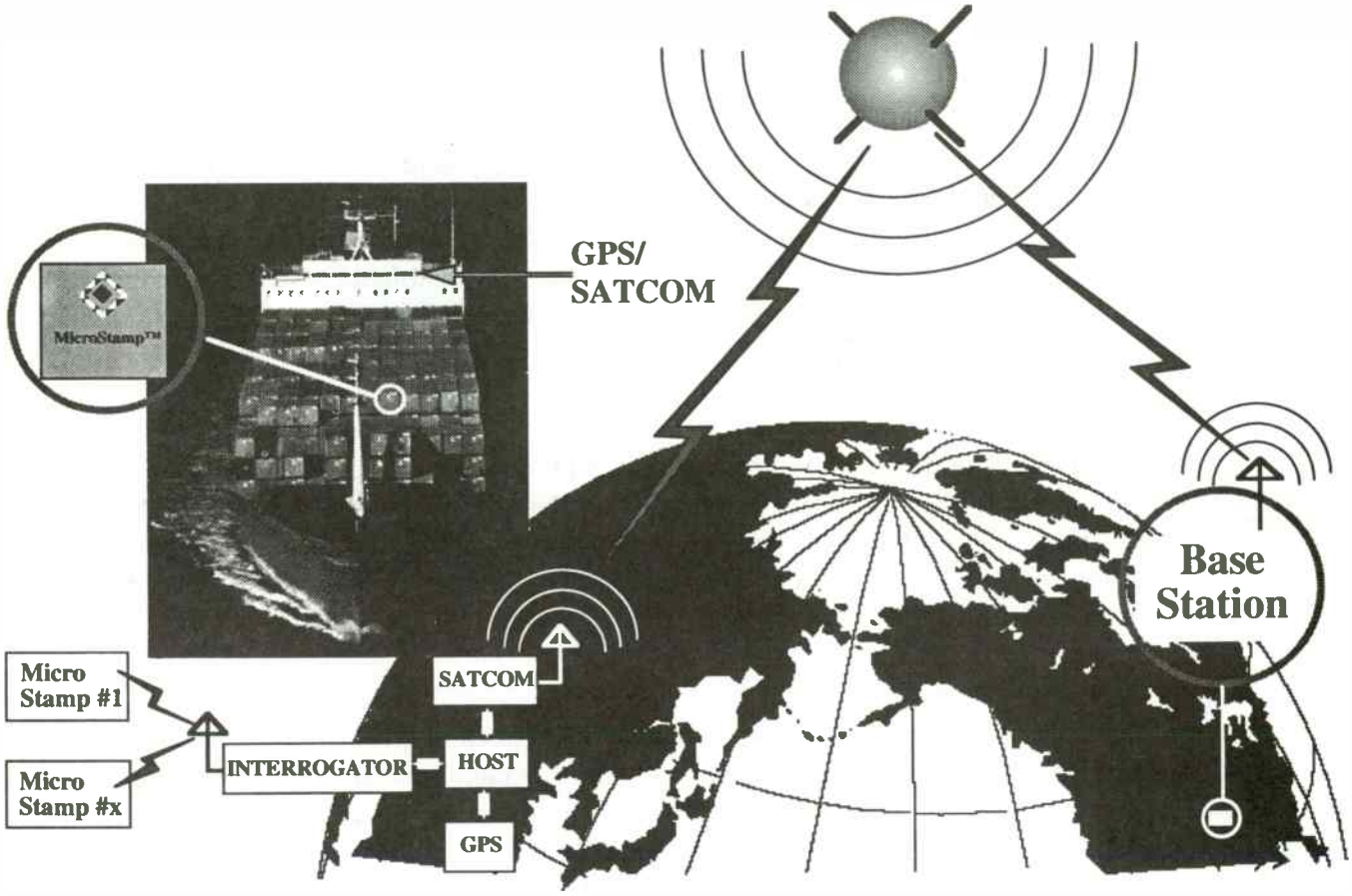

Figure 2. Worldwide item location is possible with GPS RF/ID systems.

The MicroStamp™ System

The MicroStamp RF/ID system developed by engineers at Micron Communications reduces the size of the tag to a postage stamp (1.25" x 1.25" x .04"). This read/write tag, built with lower-cost CMOS technology, is a reprogrammable data carrier. The tag contains a .5mg lithium battery, a small radio transceiver/transmitter, an omnidirectional antenna, and 256 bytes of programmable, partitionable SRAM memory with a 10 byte user programmable ID number. It is hermetically sealed in a proprietary package that is moisture resistant.

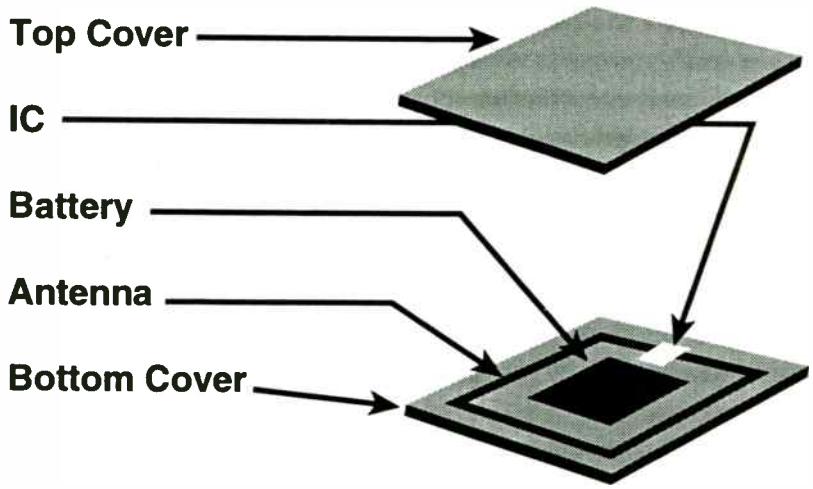

Figure 3. The MicroStamp™ RF/ID tag assembly.

The MicroStamp IC is available in a 14-pin SOIC package that allows a customer to create designs for specific applications with the addition of a battery and antenna. Coupled with an inexpensive CMOS microprocessor, the design could be used in GPS track log applications. The Micron RF/ID Communications Protocol is a licensed "open" protocol that allows manufacturers to design and build tags, antennas, interrogators, and applications software for specific customer needs. Interchangeability is achieved by incorporating a "minimum tag" concept. So any tag can be identified by any standard interrogator.

Physical Communications Protocol

The Micron Physical Communication Protocol uses a Direct Sequence Spread Spectrum scheme in the 2.4000 to 2.4835 GHz frequency band, operating under Part 15 (unlicensed) rules of the Federal Communications Commission (FCC). This half-duplex system has a forward link (interrogator-to-tag) that is ON- and a return link (tag-to-interrogator) that is modified Differential Binary Phase Shift Keyed (DBPSK).

Multiple Tags and Interrogators

It is possible for two or more tags to reply simultaneously to an interrogator's command. Various commands are available to sort and arbitrate tags if collisions occur. The Micron RF/ID Communications Protocol also allows the use of multiple interrogators by including the capability to pass the Interrogator ID (InterrID) between the interrogator and the tag on most commands. With the exception of the WriteTagStoredInterrTagIDRange command, no commands ending in "Range" will process a command unless the InterrID sent with the command matches the interrogator ID that is stored in a tag (TagStoredInterrID).

TagID Structure

The identification structure (TagID) is ten bytes wide with an 8-digit Standard Industrial Classification (SIC) code contained in the first four bytes. An interrogator in conjunction with the SIC code may quickly isolate tags which are associated with a particular industry. The UCC/EAN codes may be used in place of the SIC Codes. Since the protocol does not define the type of memory to be used for the TagID data, a manufacturer can implement the TagID (or any portion of it) as any type of memory (i.e. EEPROM, one-time programmable, etc.). Codes other than SIC codes may be used in the first four

bytes for special purposes provided they do not conflict with the SIC code. These special codes are not covered by the standard protocol. For example, the code B7654A21H (hexadecimal) is not contained in the SIC code list; therefore, the code is allowed for special applications.

Memory on Tags

Memory on a tag may be divided into partitions. Each partition may be protected by assigning a password for that partition. The read and write memory commands use a block transfer approach. The user specifies the StartAddress and the StopAddress. These addresses must be within the requested partition. Supplying the start and stop addresses allows an interrogator to request a range of locations that is less than a full memory partition. This results in prolonged battery life because needless updates are not executed.

A tag manufacturer may configure a portion of the memory space to be nonvolatile memory (such as EEPROM, fusible link ROM, battery-backed RAM, etc.). The protocol is independent of the type of memory included on a tag. This protocol does not define the amount of memory included on a tag although the memory address space is limited to a 3-byte address space encompassing 16 megabytes. The protocol permits tags containing only a TagID and no other user memory. If more than three bytes of address space is needed, a manufacturer may use the expansion command to implement a scheme to address as much memory as required for an application.

A feature revision code (FeatureRevision) on the tag may be used to determine the amount of memory that the manufacturer has included on a tag. The four byte code allows approximately 232 unique manufacturer and version combinations.

Three Levels of Security

Three levels of security are provided in the Micron RF/ID Communications Protocol. They are referred to as the System Administrator (SystemAdmin), Private, and Public levels. In addition, a partition that is password protected may allow read access while restricting write access. Each password is assigned to a memory partition. Up to 256 partitions may be assigned. Partition 0 is a special partition; it is assigned to the System Administrator. All of the passwords are 4 bytes long.

Each partition must be initialized by the System Administrator, and only the System Administrator is allowed to change the partition definitions. Users must have prior knowledge of the assigned partitions, and passwords may be updated by any user who knows the old password. Only a System Administrator may read the partition start and stop addresses. A partition whose password is set to zero is considered to be unprotected; anyone may read the contents of a partition if the StartAddress and StopAddress are known. The addresses are physical addresses and are not relative to a partition.

Private memory exists when a password for a partition is set to a nonzero value. A password is 32 bits long. The most significant bit in a password determines whether a partition may be read without knowing the password for that partition. If the bit is set to zero, a password is not needed for read access. If the bit is a one, the password is needed for both read and write access. Public memory is any memory that is not otherwise restricted for use by the System Administrator or other private memory. Various data encryption schemes (on the application level) may also be used to further protect a tag's data.

DataBand Switching™

Micron has developed a revolutionary feature called DataBand Switching which allows an interrogator to communicate with tags of interest while others remain dormant. An interrogator's RF transmitter utilizes multiple data rates (frequency bands) so that only tags programmed to acknowledge a particular data band will respond. This unique feature allows large quantities of known tags to stay dormant (conserving battery power and reducing the number of data collisions) while a subset of tags is pro-

cessed. A non-matching data band tag does not process any interrogator commands, resulting in significantly less battery usage.

With DataBand Switching, tags may be programmed to detect external events. A tag may be programmed to switch from one data rate to another when a voltage threshold has been violated on an analog port. For example, a tag may be set to the low data rate and a voltage setpoint initialized for one of the analog ports. An interrogator would then transmit at the high data rate. While the threshold on the tag has not been violated, the tag will not reply since the interrogator is attempting to communicate on a frequency the tag is not monitoring. When a threshold on the tag's analog port is violated, the tag switches to the high data band. Since the interrogator and the tag are now on the same frequency, the tag will receive the next message the interrogator transmits.

Digital and Analog I/O

The Micron RF/ID Communications Protocol includes a synchronous serial I/O capability. The digital I/O port can be used to send or receive data, or to interface with external logic such as a multiplexer. A block of data may be transmitted to a tag which can, in turn, output the block to the digital port. Similarly, a block of data may be read from the digital port and transmitted back to an interrogator.

The Micron RF/ID Communications Protocol also provides an analog input capability. The user may select from external analog inputs using the digital I/O port and an external multiplexer. The analog input voltage may range from 0 to 2.5 volts. The analog port may be programmed to source up to 2 milliamps (in 0.0078 milliamp steps). Floor and ceiling setpoints may be set for any of the analog inputs. A tag can be programmed to switch data bands if the input violates either setpoint.

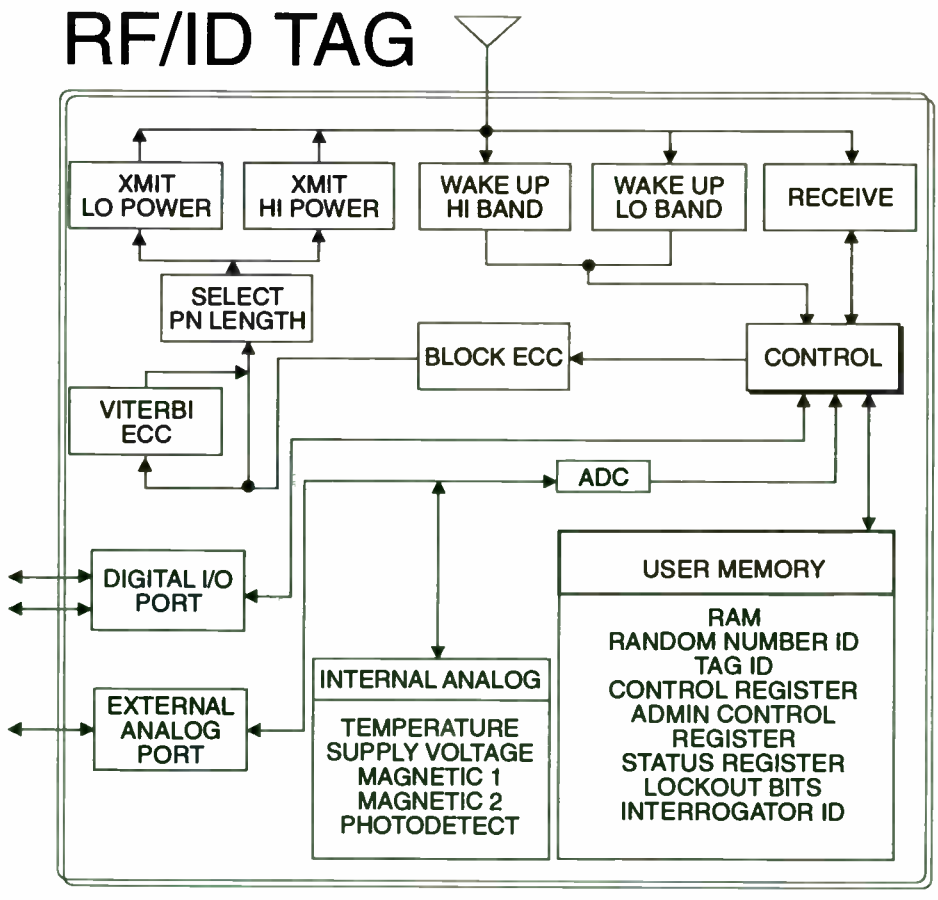

Figure 4. Typical RF/ID block diagram.

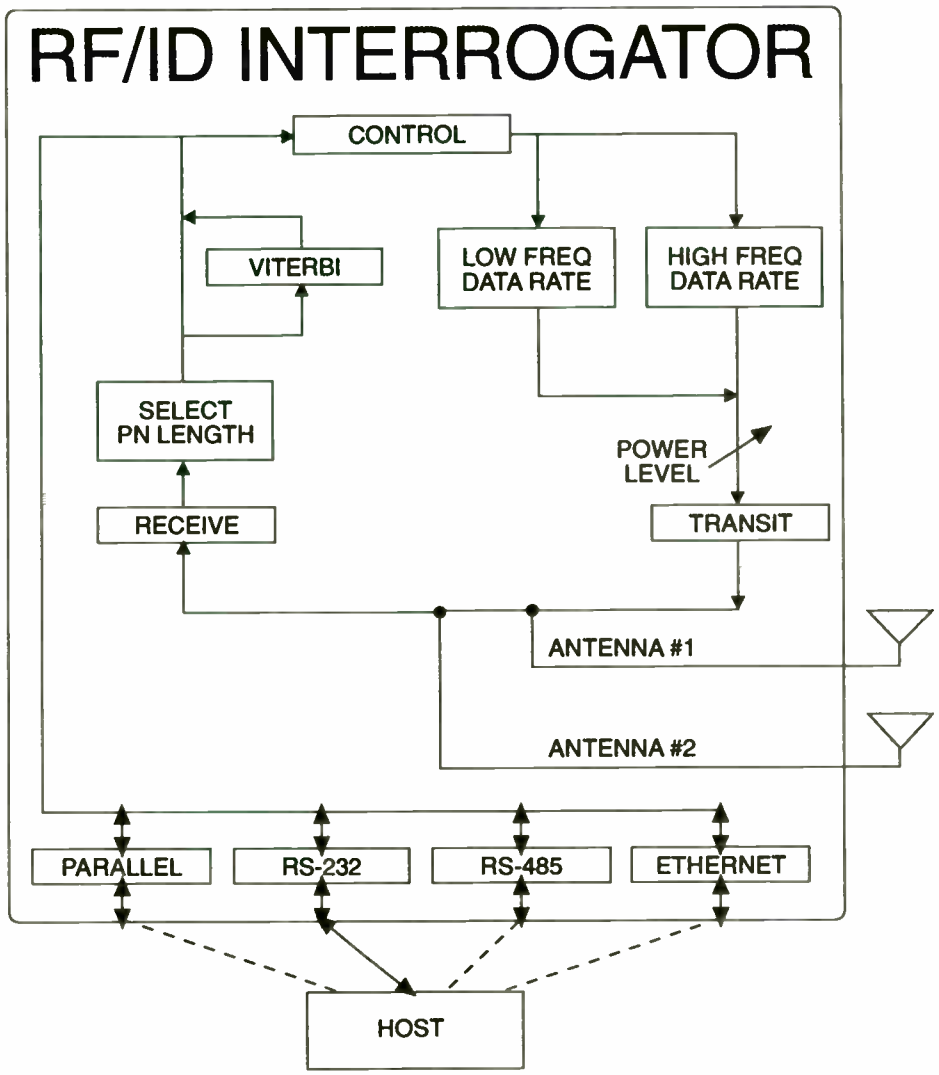

Figure 5. Typical interrogator block diagram.

Conclusions

Engineers at Micron Communications have developed new battery and package technology to produce the smallest high performance RF/ID tag available. The MicroStamp RF/ID tag, manufactured with CMOS technology, has more memory, longer range, and more programming flexibility than previous designs. Thirty commands, including password security, can be used to program the tag for individual applications.

The ability to manufacture RF/ID tags with cheaper CMOS technology and link them to GPS will revolutionize automatic data capture systems for surveillance and tracking applications. GPS-linked RF/ID gives law enforcement agencies a more affordable and effective system for clandestine surveillance. And the system can be used in the shipping industry for parcel tracking and "real-time" inventory control.

RFID Systems SAW vs CMOS

Paul A Nysen
X-cyte inc.
San Jose CA.
(408) 428 9911

Abstract

Radio Frequency IDentification (RFID) is one of the essential computer inputs that allows objects, people or animals to register their presence and to be uniquely identified without the need for conscious cooperation with a key pad or bar-code reader system. Specifically RFID finds the most appropriate applications in access control, animal identification, factory automation, vehicle identification (tolls, parking and priority lanes) and warehousing inventory control.

In this paper the design issues will be addressed as a top-down design driven principally by the market requirement. The functional requirements will first be addressed and then followed through to system design and options. Finally the critical design issues, that allow for product differentiation between SAW and CMOS operating around the 'L' band region, will be analyzed and discussed. This will conclude in an analysis of the type of SAW devices used in RFID systems.

X-cyte Inc.
Automatic Identifcation Systems

FUNCTIONAL REQUIREMENTS:

1. Tag Location
2. Reader Location
3. Relative Speed
4. Number of Objects
5. Security Requirement
6. Tag Life
7. Tag Environment
8. Programmability
   - Factory
   - Field
   - Remote
9. Safety / Compliance

X-cyte Inc.
Automatic Identification Systems

SYSTEM OPTIONS:

1. **ID**
   - Fixed
   - Programmable
     - Factory
     - Field
     - Remote
2. **Tag Power**
   - R.F.
   - Battery
3. **Security**
   - Passive
   - Active (Transactional)

X-cyte Inc.
Automatic Identifcation Systems

PRODUCT OPTIONS:

1. **S.A.W.**
   - Multi Tap Delay
   - Multi Frequency

2. **CMOS**
   - Reflection Modulation
   - Product Modulation
   - Active

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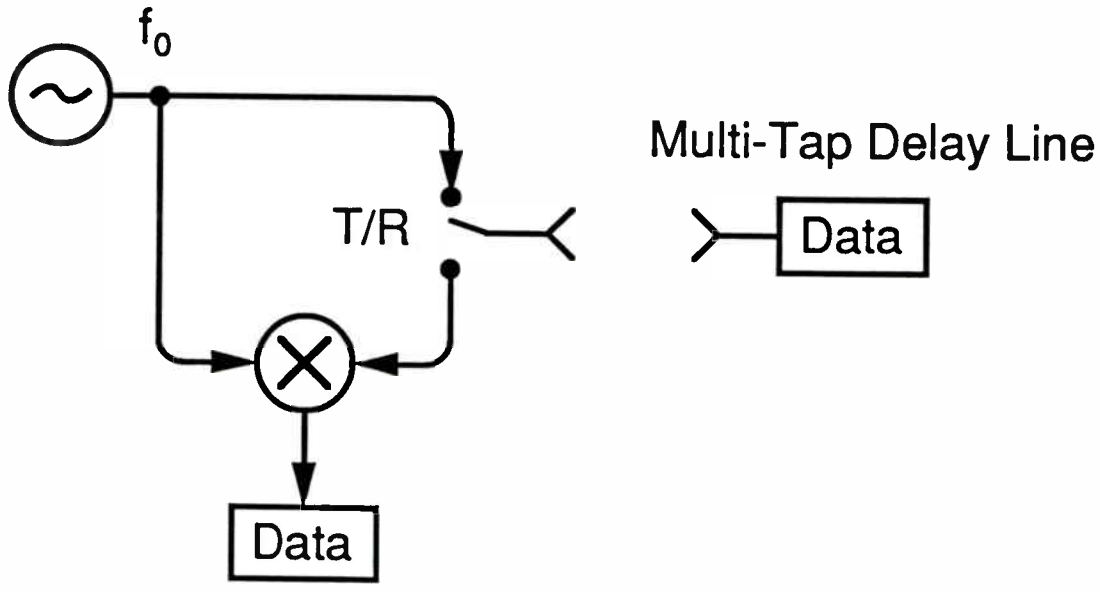
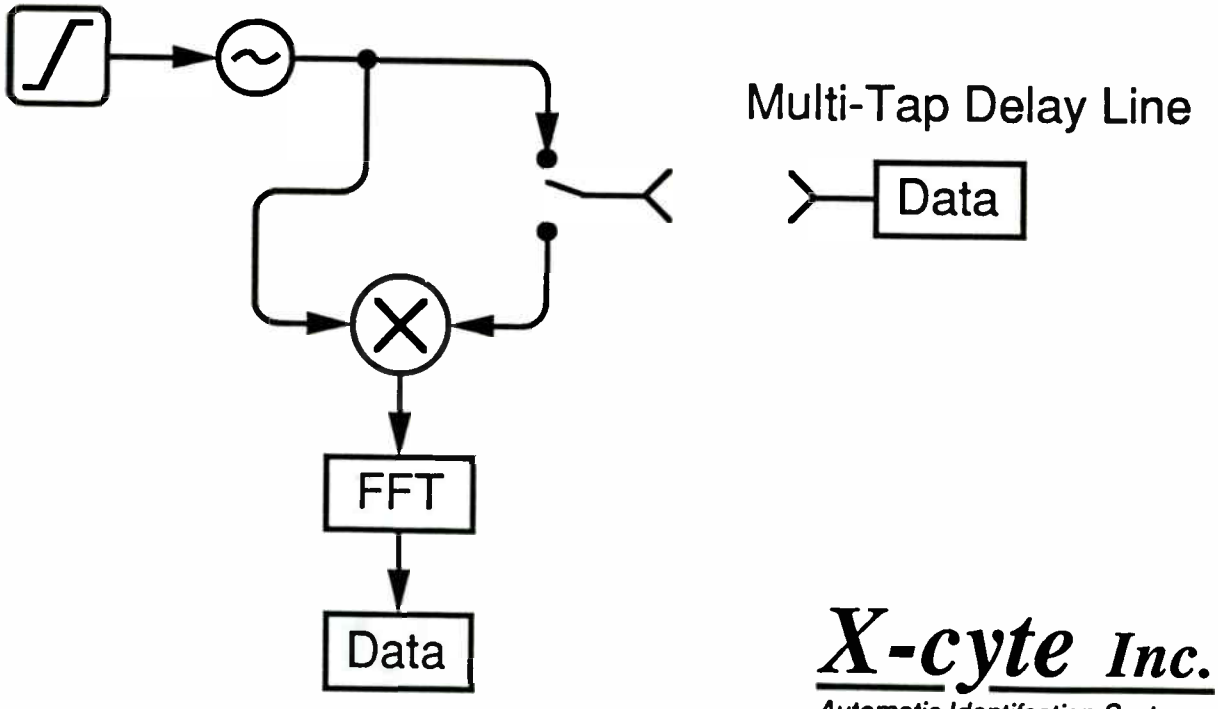
Automatic Identifcation Systems

SAW SYSTEMS

PULSE ECHO



CHIRP



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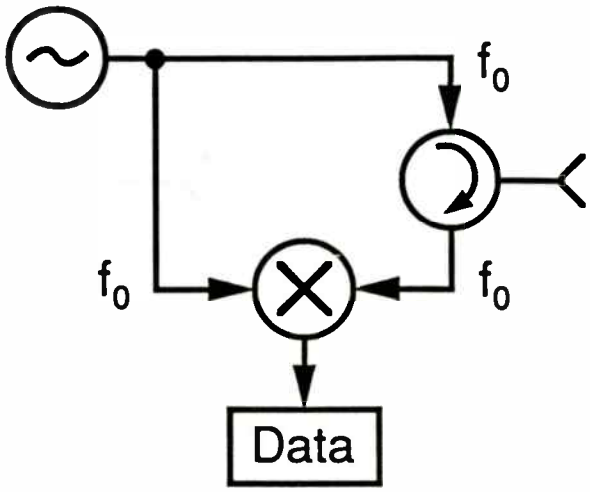
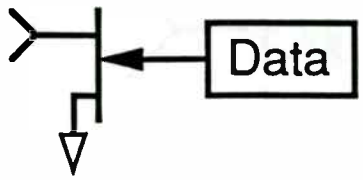
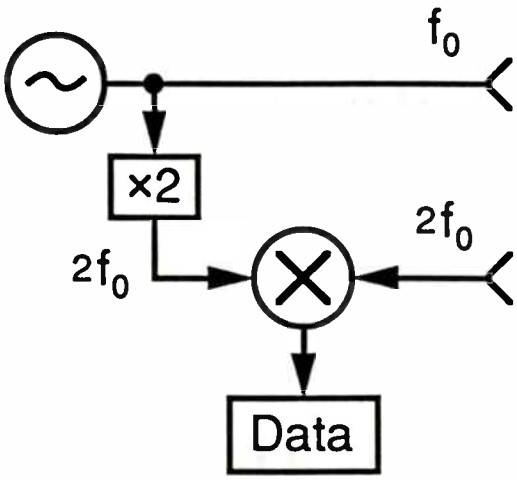
CMOS SYSTEMS

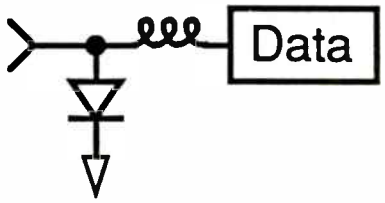


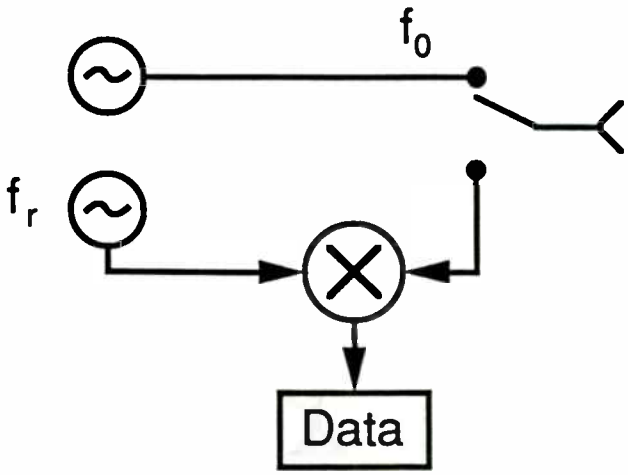
Reflection Mod.



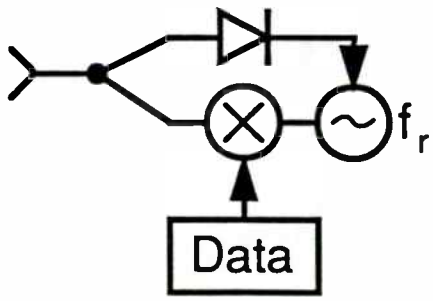


Product Mod.





Active Transponder



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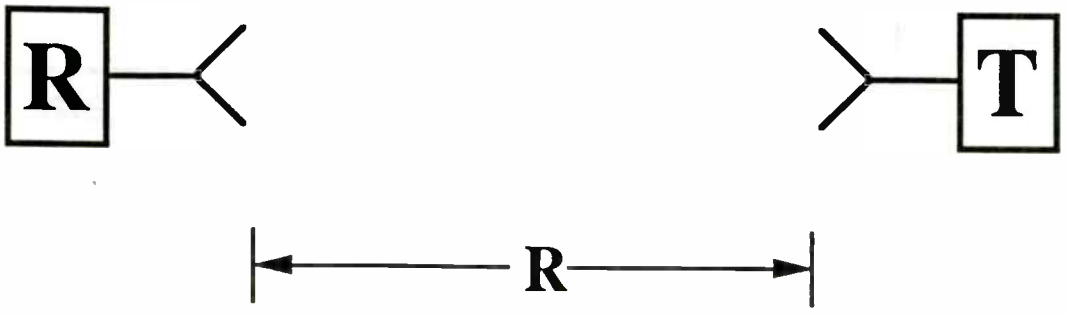
LINK EQUATION



$$S/N = \frac{P_T \alpha_T}{N_0 B_w} \frac{(G_R G_T)^2}{(4\pi R/\lambda_0)^4}$$

SAW:

$$\alpha_T = \frac{1}{N_a^2} \rho_r^2 \alpha_r \alpha_\Omega \alpha_a$$

$$B_w = 1 / T_{SCAN}$$

$$N_b = N_a \cdot N_r \cdot N_c$$

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LINK COMPARISON

CMOS:

$$\alpha_T = \rho^2_{BS}$$

$$B_w = 1.5 \quad N_b / T_{blk}$$

IF C = COMMON TERMS

$$S/N_{SAW} = \frac{N_c}{N_a} \alpha_r \alpha_\Omega \alpha_a \quad C$$

$$S/N_{CMOS} = \frac{1}{1.5} \cdot C$$

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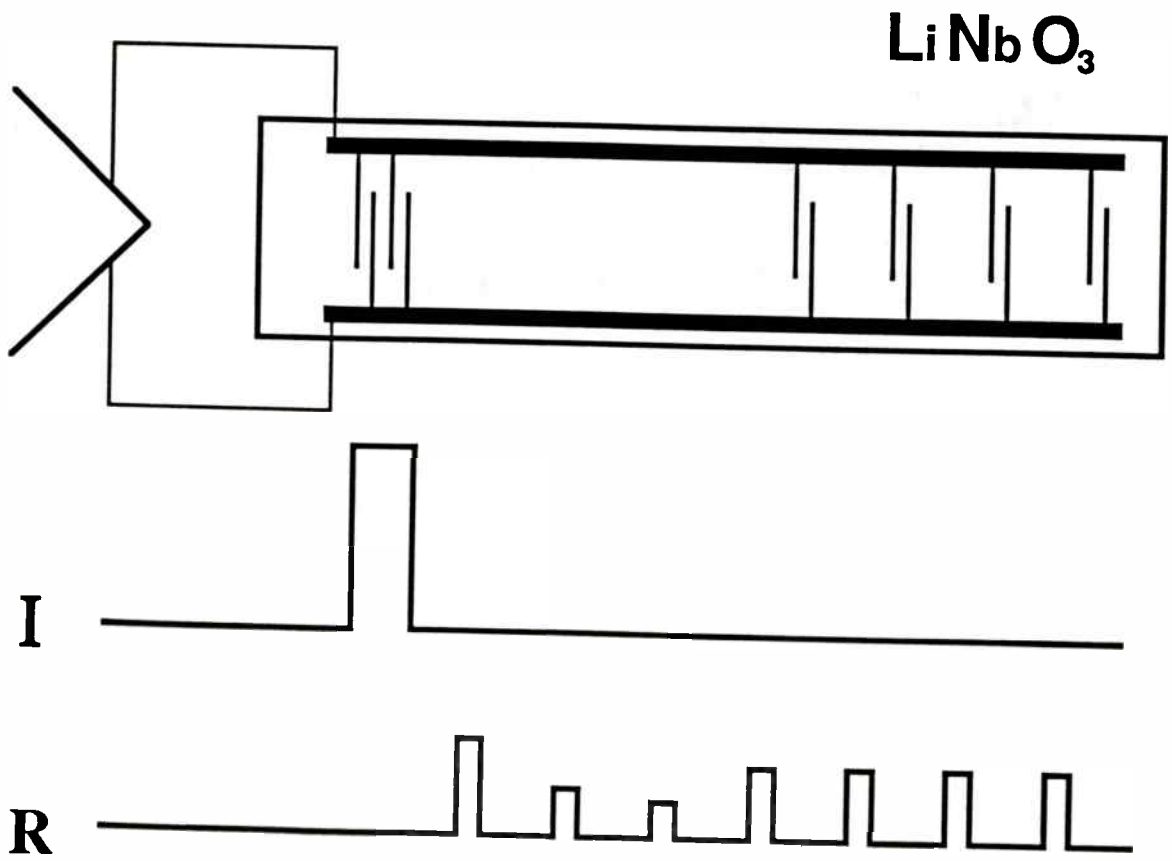
MULTI TAP SAW TAG TRANSMISSION MODE



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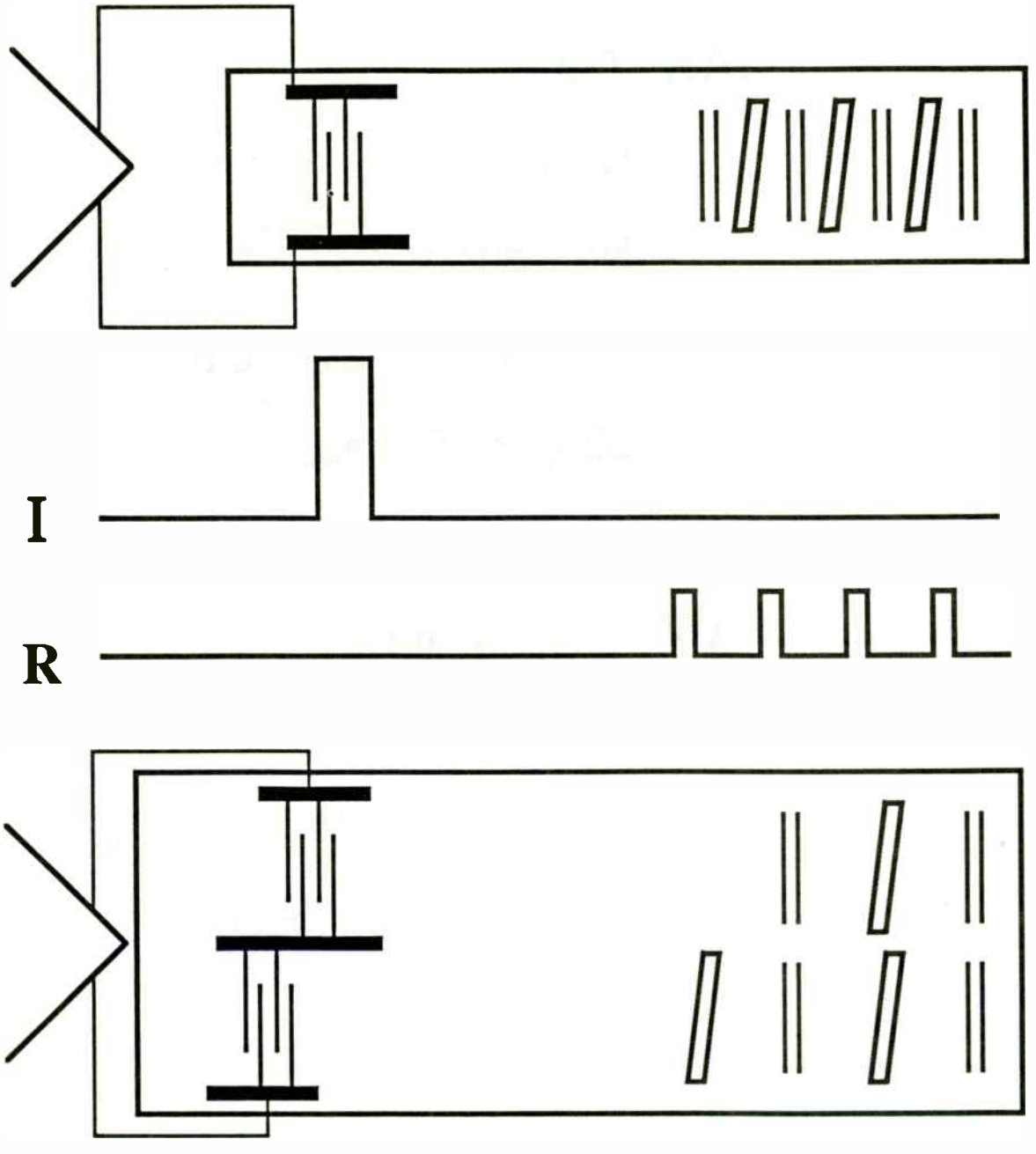
MULTI TAP SAW TAG REFLECTION MODE



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CONCLUSIONS:

1. **SAW TAG**
   - Secure
   - No Battery
   - Environmentally Tolerant
   - Simple / Reliable

2. **SAW Tag System**
   - Low Power
   - Fast Read Rate
   - Signature Verification

X-cyte Inc.
Automatic Identifcation Systems

Low voltage RF power amplifiers for handheld communication equipment

By Rudolf van der Last
Philips Semiconductors

Communication systems like AMPS, ETACS (900 Mhz) and NMT (450 and 900 Mhz) are quite well known analogue systems. New digital systems are in development today. Examples are CT2, GSM and D-AMPS working in the 900 Mhz bands, and DCS1800 and DECT, both working at about 1.8 GHz. Emerging technologies, such as spread spectrum for applications like wireless LAN, are becoming available in the 1.8-2.4 Ghz band.
The current subscriber units or handsets operate with a 6.0 to 7.5 volt battery pack. Low voltage (3V) IC chip sets, which provide the logic and signal processing functions, that draw lower current are becoming available for the subscriber handsets. These 3 volt chip sets, with improved efficiency, allow the use of smaller battery packs, reducing the overall size and weight of the unit, - a benefit for the subscriber. It is clear that the RF power amplifier technology is forced into the same directions, i.e.: lower supply voltages at higher frequencies.
This paper compares the general performance of GaAs FET's and bipolar transistors at higher frequencies and lower voltages as power amplifier stages, and presents a design example of a discrete bipolar 1.9 Ghz, 3 volt transmitter amplifier. Items to be discussed are:

1) Power transistors for high frequency and low voltage
   - General amplifier concept,
   - What makes a transistor a good RF transistor for low supply voltage
   - Comparison of technology, i.e.: discrete and integrated, GaAs and bipolar,

2) Application example of a 1.9 GHz amplifier for 3.6V supply voltage,
   - Components,
   - Design method,
   - Measurement results.

General amplifier concept.

The most important characteristics of a complete amplifier (see fig. 1) are:
- Output power
- Gain
- Frequency behavior
- Efficiency
- Cost and weight

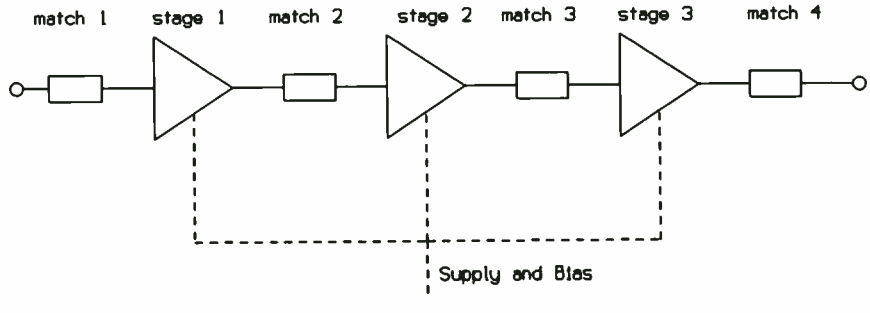


fig. 1 Block diagram power amplifier

The first amplifier stage is chosen to be class A as a high gain buffer between the VCO and the rest of the amplifier, which can also be used as a variable gain stage for power level control. Since the efficiency is dependent on the mode of operation (see table 1 for theoretical efficiency), the last two stages are normally operated in class-AB which provides the best compromise between gain and efficiency.

mode of operation	Gain	Efficiency max.
Class A	High	50 %
Class AB	|	50 - 78.5 %
Class B	|	78.5 %
Class C	Low	90 %

Table 1, Gain & efficiency vs. mode of operation

The efficiency of the RF power amplifier is very important, as this is a factor in the battery life or discharge time. To obtain a good overall efficiency, the power gain of the final transistor is most important. A simple calculation (see fig. 2) demonstrates that a final stage transistor with a low power gain causes a lower overall amplifier efficiency.
For digital TDMA systems, the rise and fall times of the amplifier are important, while some digital systems also require better linearity than analog systems.
The transistors in a high performance amplifier will be devices with high power gain, high efficiency, and low cost and weight.

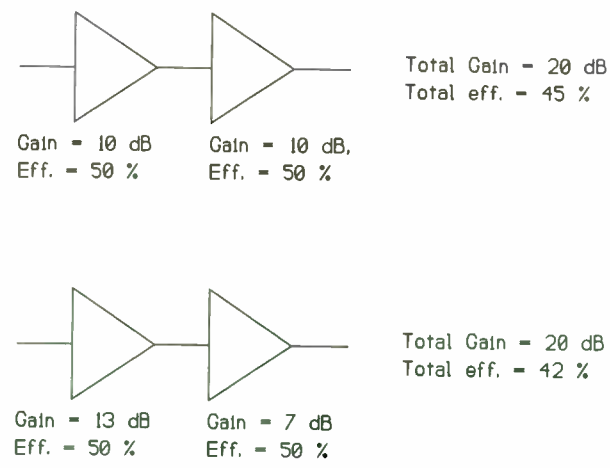


fig. 2 Overall efficiency of 2 stage amplifier

What makes a transistor a good RF transistor for low supply voltage?

Since output power is the product of current and voltage, devices operating at low voltage must be able to handle higher currents to produce the same power than devices operating at high voltage. The current handling capability of a device is proportional to the amount of active die area. Increasing the active area results in increased feedback capacitance, which reduces the gain. In addition the larger collector (or drain) current in the emitter or source, causes additional negative feedback, which reduces the gain even more.

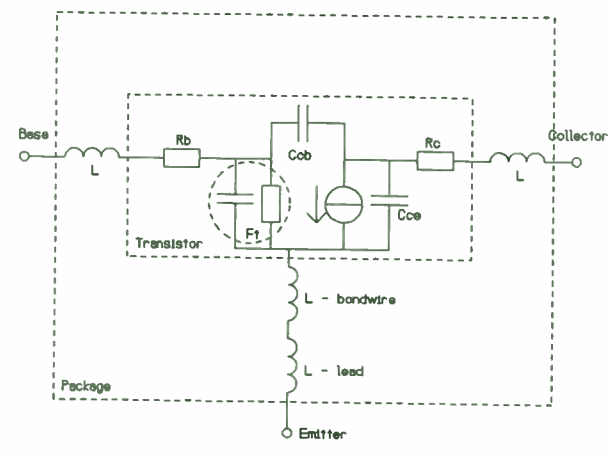


fig. 3 Transistor model

A good device should have a high f_T, low feedback capacitance (C_{cb}) and a low emitter or source inductance (L bondwire, L lead). (fig 3.) The emitter or source inductance is mostly determined by

the self inductance of the bondwires and the leads (package related). Fig4. shows the influence of emitter inductance and feedback capacitance on power gain of a low voltage bipolar device.

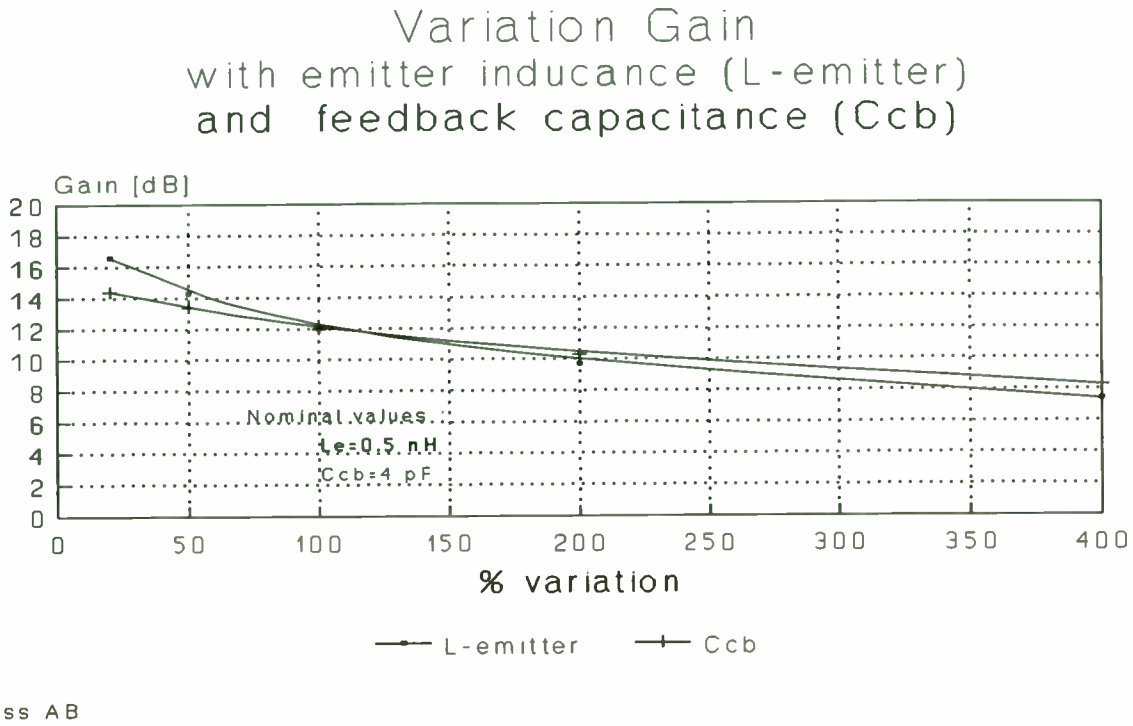


fig. 4 Gain vs. % variation in emitter inductance and feedback capacitance

Comparison of technology

Power amplifiers can be built up with transistors based on either GaAs, silicon MOS or bipolar technlogy. Each of these technologies has advantages and disadvantages over the other. Transistors can be put together by integration (IC or MMIC), on a ceramic substrate (hybrid) or as packaged devices on a printed circuit board (discrete).

The following solutions are most widely used:

- Discrete GaAs (Gallium Arsenide) SMD (surface mount device)
  GaAs transistors mounted in a plastic package, put together with SMD capacitors and inductors/striplines on a PCB
- Module GaAs
  GaAs transistors mounted on a substrate with SMD capacitors and inductors/striplines mounted on a ceramic substrate.
- GaAs MMIC
  Integrated circuit of transistors, capacitors and coils.
- Discrete bipolar
  Bipolar transistors mounted in a plastic package, put together with SMD capacitors and inductors/striplines on a PCB
- Module bipolar
  Bare bipolar transistors mounted on a substrate with SMD capacitors and inductors/striplines.

Table 2, compares the GaAs and bipolar technologies as these are the most commonly used (MOS is not yet available for low supply voltages and reasonable performance).

	For all systems						Digital systems only	D-Amps, JDC
Technology	Pout (Vs)	Gain (Vs)	Efficiency	Size	Price	Simplicity	Fast power control	linearity
Discrete GaAs	o	+	+	-/o	-	-	-	+
Module GaAs	o	+	+	o/+	-	-	-	+
MMIC GaAs	o	+	+	+/++	-	-/+	-/+	+
Discrete bipolar	+	-	o	-/o	+	-	+	-
Module bipolar	+	o	+	+	o	+	+	-

Table 2, Comparison of technologies

+ high, o moderate, - low

Explanations:

Pout (Output power vs. supply voltage)

- The maximum available output power of a die decreases as the supply voltage is lowered,
- For the same amount of output power, the active area of GaAs-FET's must be larger than for bipolar transistors (because of the horizontal structure of GaAs), resulting in higher cost.

Gain (Large signal gain vs. supply voltage)

- At low supply voltages the feedback capacitance of bipolar transistors increases. (voltage dependent capacitance) This results in a lower gain.
- GaAs fets can be assembled with much shorter source wires when compared with the emitter wires of bipolar transistors. This is because of the non conductive substrate (fig.5). Compare in this figure the wire length (inductance is proportional to wire length) from the internal emitter or source (point 1) to the outside world (point 2) for the bipolar and GaAs transistor. At point 2 a good ground contact can be made.

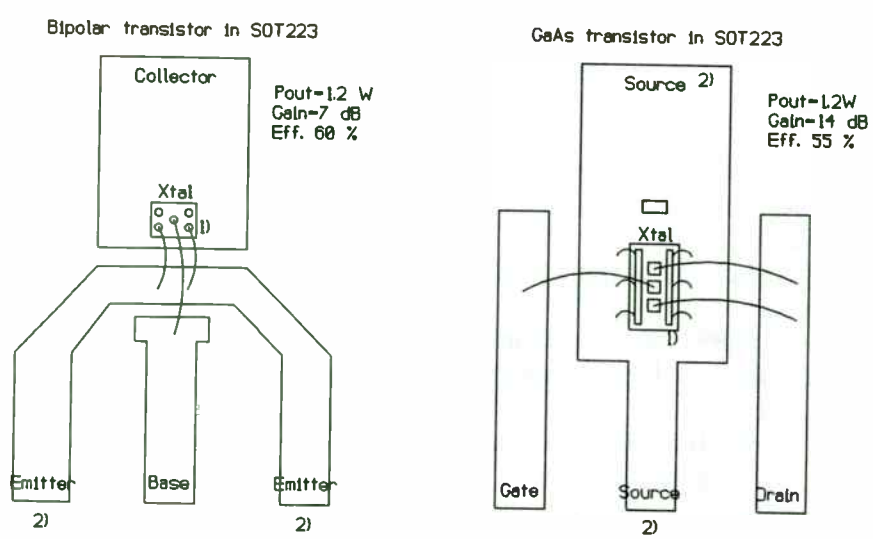


fig. 5 Emitter/source grounding bipolar vs. GaAs transistor in SOT223

Efficiency

- Efficiencies of GaAs and bipolar transistors are comparable at maximum output power level. The efficiency of a bipolar transistor, operating in class-AB, is higher than GaAs for operation at lower power levels.
- The drain switch and negative gate bias needed for GaAs transistor decrease the overall efficiency of the amplifier.
- The efficiency of MMIC's could be limited by higher losses in the matching circuits on the chip.
- Efficiency is less important for TDMA systems than it is for analog systems because the actual transmitting time is less.

Size

- Height of a discrete solution is lower than a module, especially for pulsed power amplifiers where SMD power transistors can be used.
- GaAs modules need more external components and therefore take up more board space.
- If negative voltage generator and switch can be integrated in GaAs MMIC the complete size of these solutions will be very attractive.

Simplicity

- GaAs solutions require a lot of additional components to perform the following functions :
  - negative gate bias
  - switch in the supply line
  - buffer transistor in the control line
  - control circuit for timing of gate bias and drain switch to secure the gate bias is always on before the drain is switched on.
- GaAs modules require a higher input level, because these modules have less stages than bipolar amplifiers.
- Discrete solutions need more design effort than modules, with the advantage of lower cost. The amplifier described in this paper has a total component cost of approximately 3 dollars in large quantities.

Fast power control

- The power control of a bipolar is very simple. Power control and on/off control is combined in the same control pin. For on/off control of GaAs an additional switch transistor in power line is needed.

Linearity

- Bipolar transistors in class AB have a reasonable linearity.
- GaAs transistors are very linear and normally operated close to class A, thereby offering a high gain.

The design of a 1.9 GHz amplifier for low voltage.

In this design example of a power amplifier for DECT, we demonstrate that a discrete bipolar transistor solution as effective in performance as GaAs, while less costly at the same time.
The targets for the technical specifications of this amplifier, based on reported performance of similar GaAs line-ups [1], are:

Targets:

The technical specifications for this amplifier are :

Frequency 1.9 GHz
Supply voltage 3.6V
Output power 0.4 W
Efficiency > 40 %
Input power 3 dBm
Maximum duty cycle 1:8, period <= 10ms

Physical specifications:

Use of discrete transistors and capacitors on printed circuit board.
Board area 20 x 10 mm for RF part.

Demonstrate that a bipolar power amplifier can be designed with modern CAD tools.

Components

Bipolar transistors specially designed for these applications are the BFG10 (driver) and BFG11 (final stage) in the SOT143 package. The specifications for these are:

BFG10 :	Gain	: > 7 dB
	Pout	: > 200 mW
	Efficiency	: > 50 % (power added)
	Operating class	: AB
	Maximum duty cycle	: 1:4

BFG11 :	Gain	: > 5 dB
	Pout	: > 500 mW
	Efficiency	: > 50 % (power added)
	Operating class	: AB
	Maximum duty cycle	: 1:4

The line up for this amplifier is show in fig. 6. The first stage in the line up is the BFG540, operating in class A, which gives 12 dB gain at 1.9 GHz. With 40 mA bias current, we get 35 mW output power and 25 % efficiency. The impedance matching has been done with chip capacitors and microstrip inductors.
For the transistors Gummel Poon models are available. The models for the Philips chip capacitors where derived from measured S-parameters. For simulations of the amplifier the Microwave Design System from Hewlett Packard has been used. This system is capable of doing linear and non linear (with harmonic balance method) simulations.

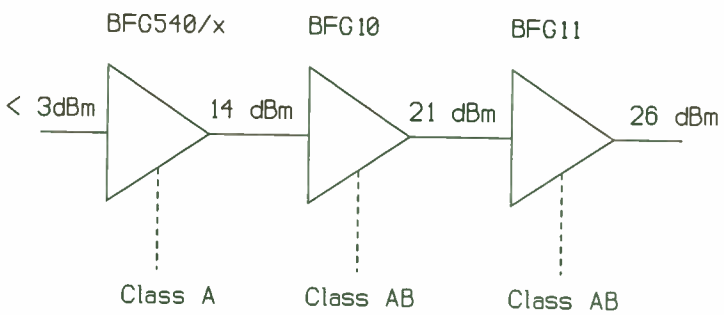


fig. 6 Lineup 1.9GHz, 3.6V power amplifier

Design method

This sequence was followed for the design:

1) The source and load impedance were derived for each transistor for optimum performance, i.e. maximum gain at the nominal output level. Efficiency, gain and output power were verified. (See note 1.)

2) A low Q matching network for each section was designed for the desired load impedance and the desired source impedance. For the first pass ideal capacitors and microstrips with small width as inductors were used. Then the circuits were optimized for maximum S21 using a S-parameter simulation. (See note 2.) [App. A-1]

3) Bias stubs, as short as possible, were added.

4) The ideal components in the matching networks were then replaced with models of chip capacitors with resonance and losses, and another optimization for maximum S21 using S-parameter simulation was completed. At this point, as the layout was known, the straight microstrip inductors were replaced with more exact models describing the actual layout. [App. A-2]

4a) A sensitivity analysis for this network was performed, and improvements were made to make it insensitive for component variations. (See note 3.)

5) The circuit layout was designed. [App. B]

6) Step 4 and 5 were repeated until the optimum between size and performance was achieved.

7) A simulation was run for the power, efficiency, and frequency response of the complete amplifier. [App. C-1]

8) Bias circuits were added for the Class A and Class AB settings. [App. D]

NOTES:

1. The optimum source and load impedance will vary from transistor to transistor. The source impedance depends on base inductance (imaginary part) and emitter inductance (real part). The optimum load impedance for these transistors depends on the output power, supply voltage, collector inductance and collector capacitance. Less spread in source and load impedance is to be expected because these parameters are well controlled during the production of transistors.

2. Already at this point a tradeoff between size and performance has to be made to keep microstrips at a realizable length. For overall gain of the amplifier the performance of all matching networks is important. For efficiency only the performance of the last two matching networks is significant.

3. There is a relationship between the sensitivity for component variations and the Q or bandwidth of the network. A bandwidth analysis can be used to get a quick insight into the sensitivity for component variations.

Measurement results

The circuit has been build up according to the last simulation (step 6, above). Appendix B gives the final layout and list of components, and appendix D the final schematic. The results are shown in the table on page 8 and in appendix C-2 (measured performance). A comparison of the curves (app. C-1) for the simulation and the built up circuit measurement results (app. C-2) indicates that the simulation and the built up circuit compare well.

Parameter	Measured value	Comments
Output power	> 26 dBm	@3.6V supply voltage
Input power	< 3 dBm	
Efficiency	42 %	
Supply voltage	3.3 - 4.2V	
Frequency	1.88 - 1.9 GHz	
Size	8.5 x 21 mm	FR4, Er=4.7, h=0.51 mm
Passive components	0603 sized resistors & capacitors	Philips
Transistors	BFG11/x BFG10/x BFG540/x	Philips
Power control	Vc	-34 dBm to 26 dBm
Harmonics	< -40 dBc	

Conclusions

- An amplifier for high frequency (1.9GHz) and low supply voltage (3V) can be built with discrete bipolar transistors, which is suitable for large volume production.

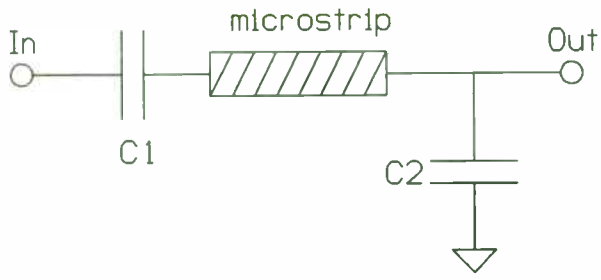
- The amplifier is lower cost, and size and performance competitive with solutions using GaAs and bipolar modules and GaAs MMIC's.

- Future improvements for discrete bipolar transistor technology would be to improve even further the RF performance of the transistor case or package (by reducing the inductive losses) and reducing the transistor case size.

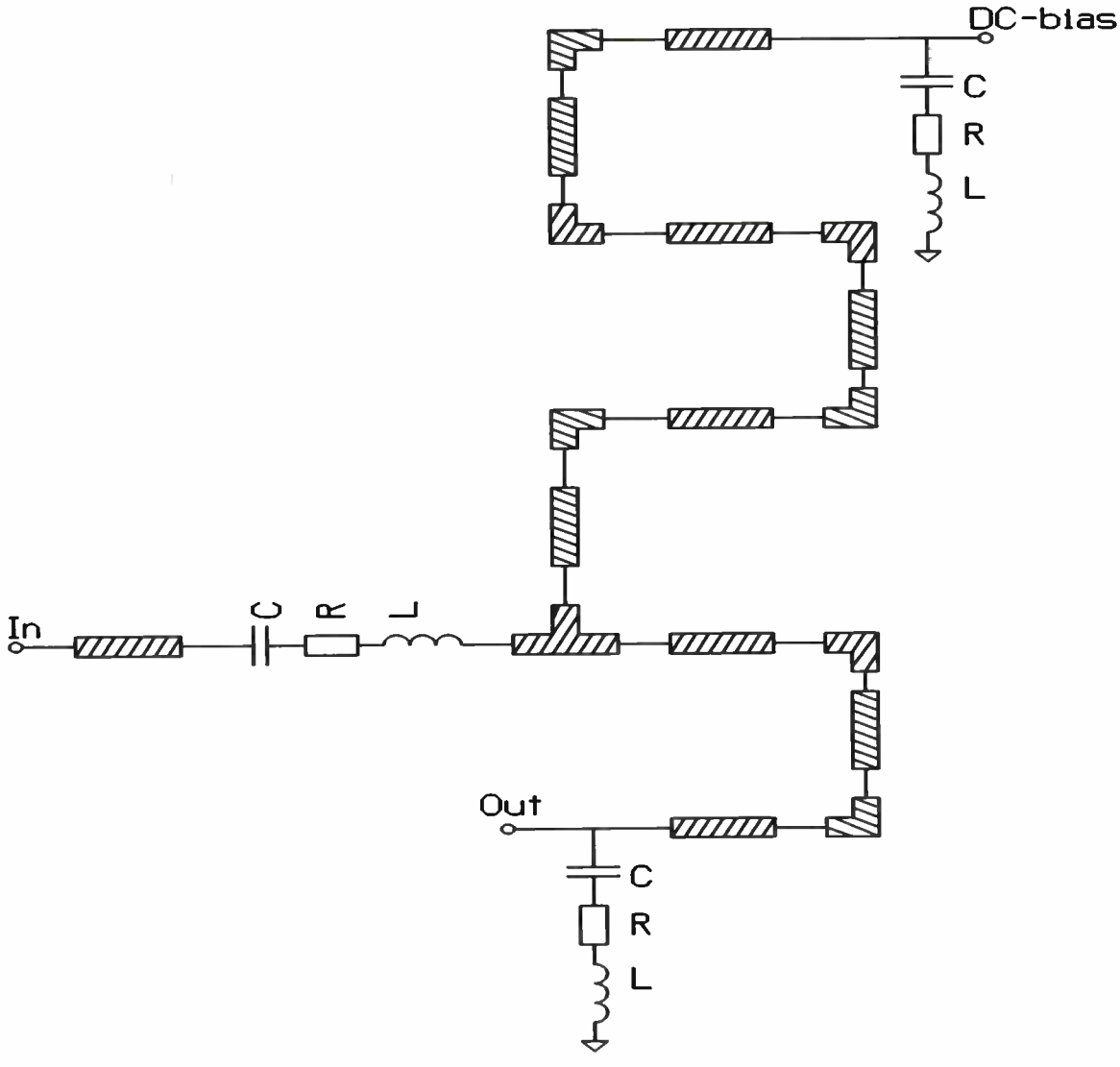
Future developments

Philips Semiconductors is currently introducing the next smaller transistor case size, the SOT343, which is 30% smaller than the SOT143 types used in this design. The BFG11 die type in this SOT343 indicates improved RF performance, since the lead inductance has been reduced. Measurements to date indicate a gain improvement at 1.9 GHz of about 2 dB. With this smaller package low cost bipolar power amplifier designs will become feasible at 2.4 GHz and possibly higher.

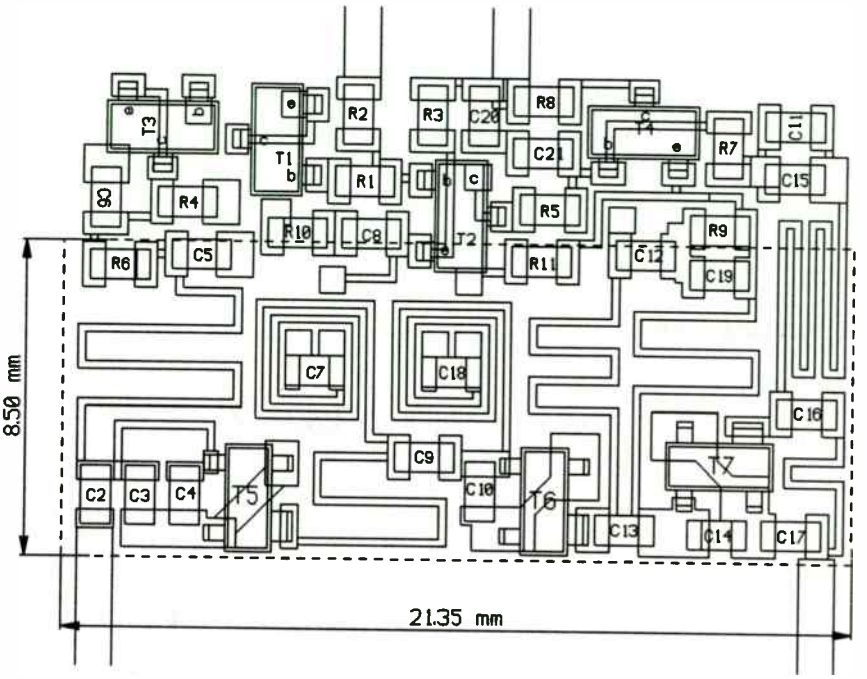
[1] Low voltage GaAs Power amplifiers for personal communications at 1.9 GHz.
D.Ngo, B.Beckwith, P.O'Neal, N.Camilleri



App. A-1 Principle matching circuit.



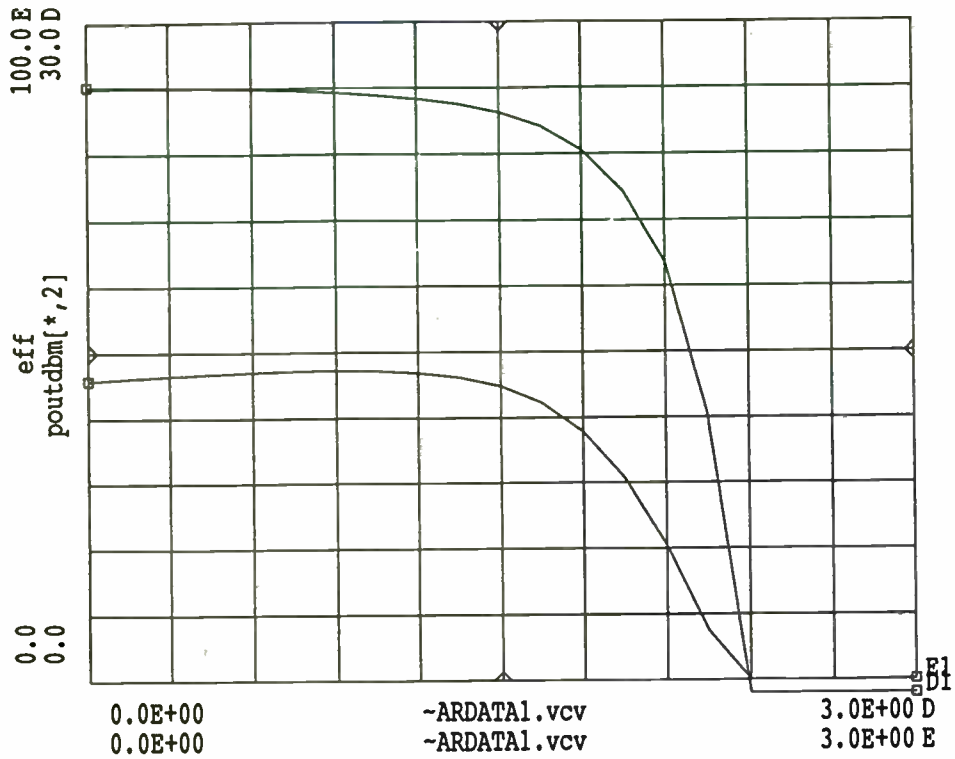
App. A-2 Matching circuit, according to layout, with models for SMD capacitors



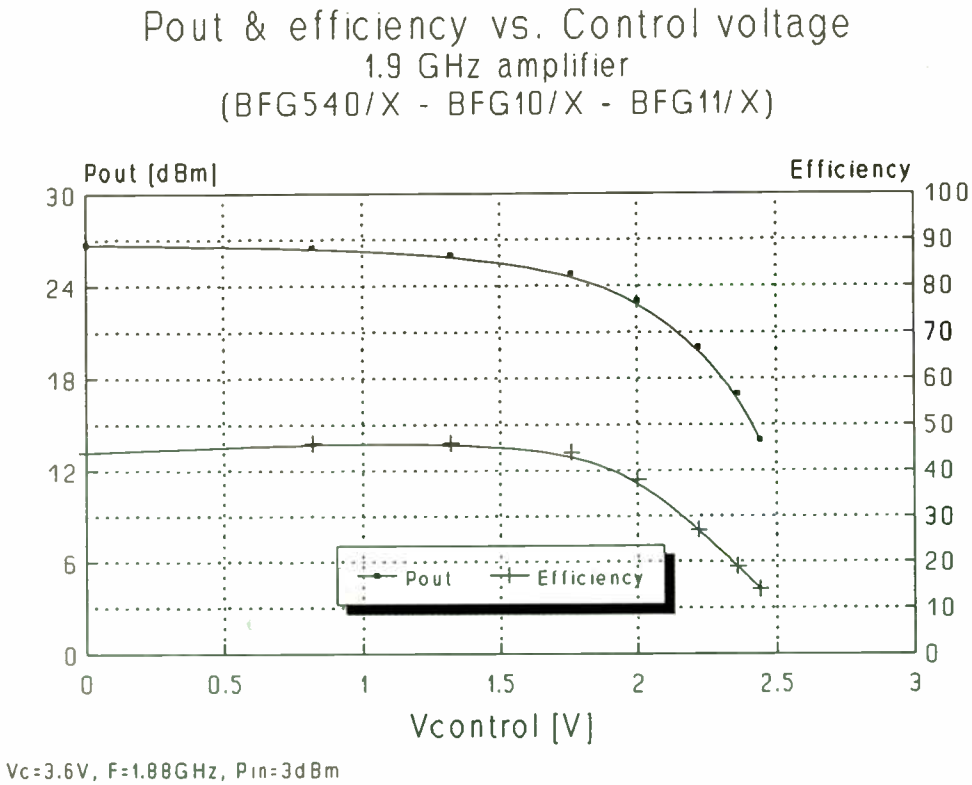
Layout 1.9 GHz, 3.6V power amplifier

Component list 1.9 GHz Power Amplifier

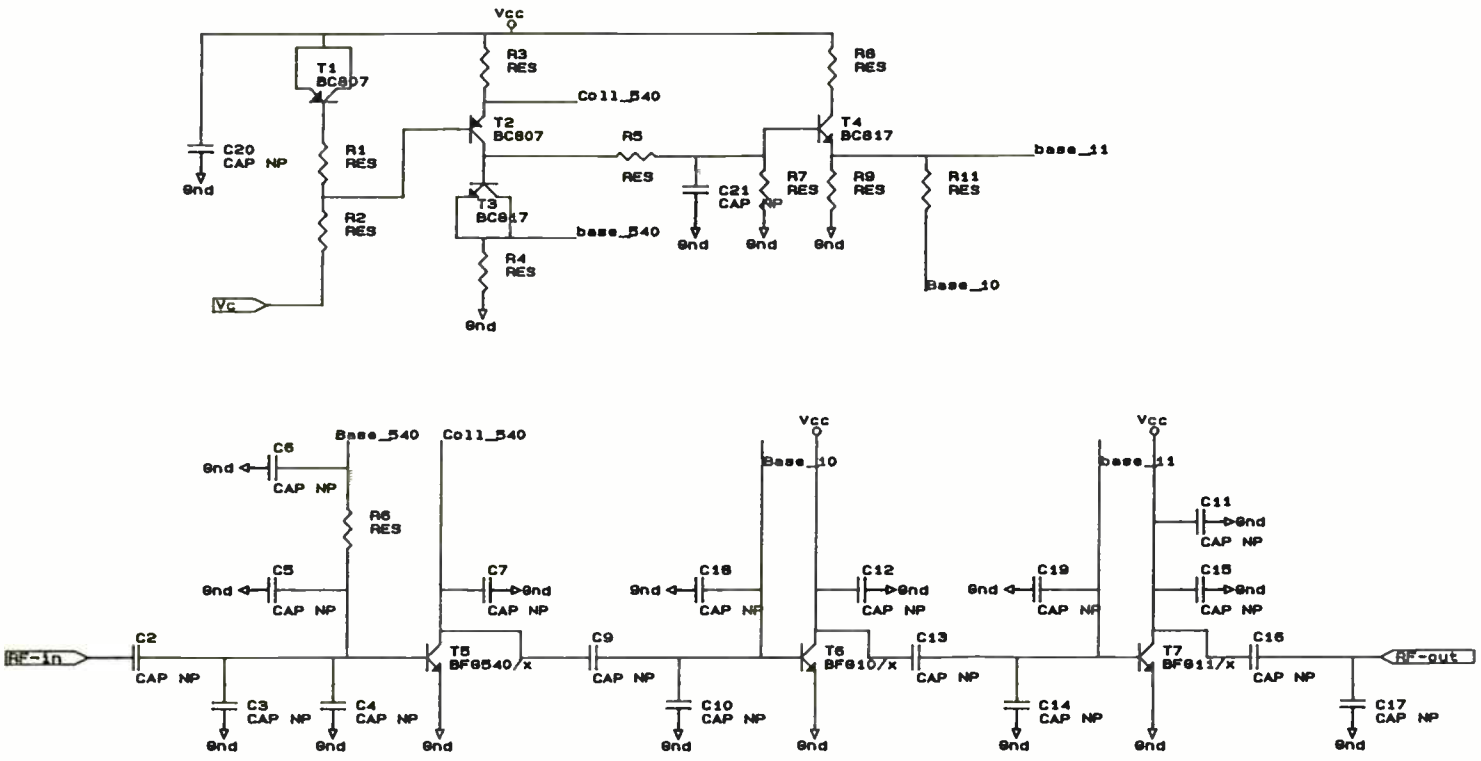
T1	BC807	R1	330E	C1	-
T2	BC807	R2	3K3	C2	8p2
T3	BC817	R3	10E	C3	0p68
T4	BC817	R4	820E	C4	3p3
T5	BFG540/X	R5	220E	C5	8p2
T6	BFG10/X	R6	47E	C6	1n
T7	BFG11/X	R7	2K7	C7	8p2
		R8	220E	C8	-
		R9	180E	C9	2p2
		R10	-	C10	2p7
		R11	15E	C11	1n
				C12	8p2
				C13	3p9
				C14	3p0
				C15	10p
				C16	3p9
				C17	2p2
				C18	8p2
				C19	8p2
				C20	10n
				C21	560p



App. C-1 Simulated performance 1.9 GHz, power amplifier



App. C-2 Measured performance



Schematic 1.9 GHz power amplifier

A LOW VOLTAGE RECEIVER DOWNCONVERTER WITH DISCRETE RF TRANSISTORS

By Bart Balm
Philips Semiconductors

Introduction

Every receiver needs an RF downconvertor, to convert the frequency of the antenna signal, with a minimum addition of distortion and noise, into a much lower intermediate frequency. Looking to today's personal communication systems (like PCS and PCN), the system trend is towards increasing RF frequency, lower supply voltage and lower current consumption, making new design challenges, and putting greater demands on the components and system designers. Philips Semiconductors has developed a new range of small signal RF transistors in an advanced silicon bipolar process, which are available in a variety of SMD packages and designed for a wide range of currents, facilitating the design task.
This paper will describe the design of two low voltage downconvertors for the 900MHz as well as the 1900MHz band.

Items which will be discussed is this paper are:

- Die and package characterization; what makes a transistor a suitable RF transistor?

- Demonstration of the performance of the new transistors in a receiver downconvertor; the design method, using CAD tools, and measurement results.

- Different technologies offer different advantages; comparing the bipolar design with silicon IC, GaAs MMIC and GaAs discrete designs.

Die and Package characterization

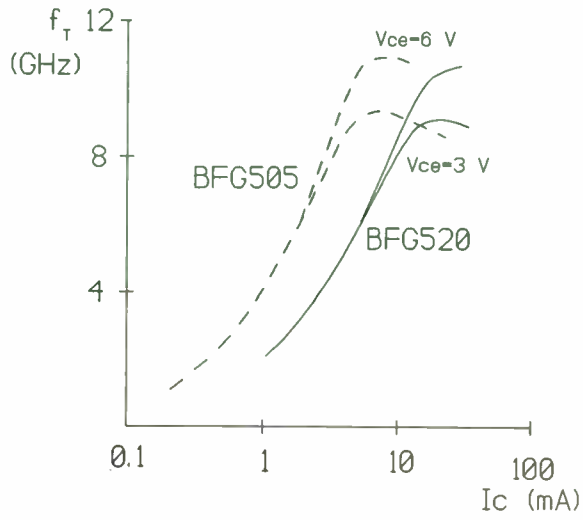


Fig.1 Transition Frequency vs. Collector current (BFG505 & BFG520)

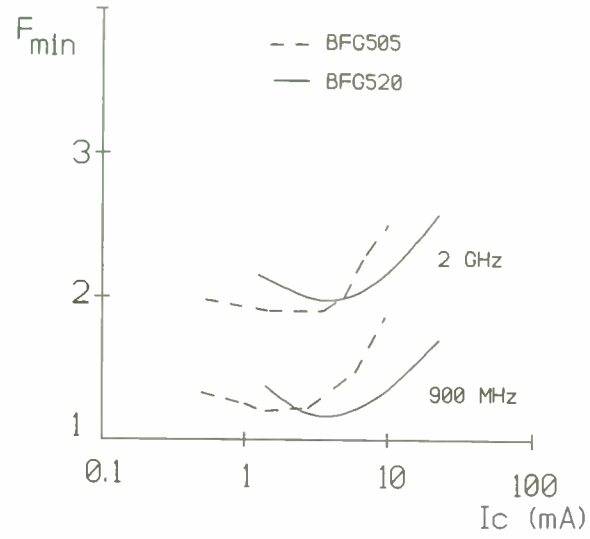


Fig.2 Minimum Noise Figure vs. Collector current

Two of the new die types, selected for low current operation are the BFG505 and BFG520 types. These new die types are indicative that the improvement process for the silicon bipolar technology is still continuing, that the silicon processes are still in development and every process upgrade still shows a considerable improvement. The critical parameter, involved in increasing the RF performance of the bipolar transistor is the emitter finger pitch. By decreasing this pitch, the transition frequency (f_T) can be increased. The f_T value for the new generation small signal devices has increased to 9 GHz, compared to 6 GHz for the previous generation.

Transition frequency is only one characterization.The RF performance can also be examined by calculating the product of base collector capacitance and base series resistance under the assumption that the internal collector resistance is negligible. This is valid for a discrete process due to the vertical structure (however, this is not valid in an IC process). Typical values for the new generation are 4 psec compared with 8 psec for the previous generation. Also to obtain devices with a low noise figure, a high h_{FE} and a low R_b are required.

The RF properties of the transistor package or case are very important. Fig 3. shows the RF limiting elements in the equivalent circuit diagram for transistor die and package. For the grounded emitter configuration the best gain performance is found when both the collector-

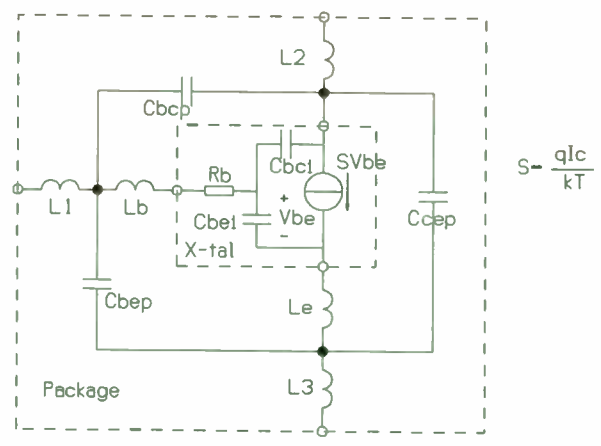


Fig.3 Die and package equivalent circuit diagram

base package capacitance (C_{bcp}) and emitter inductance (L_e+L_3) are as low as possible. For smaller die, the capacitance is more important while for larger die the emitter lead inductance is the restricting factor. The SOT143 leadframe provides a low C_{bcp} as well as a low emitter inductance (see fig 4), since the collector is shielded from the base and the emitter lead inductance is minimized by using dual emitter wires and dual emitter leads.

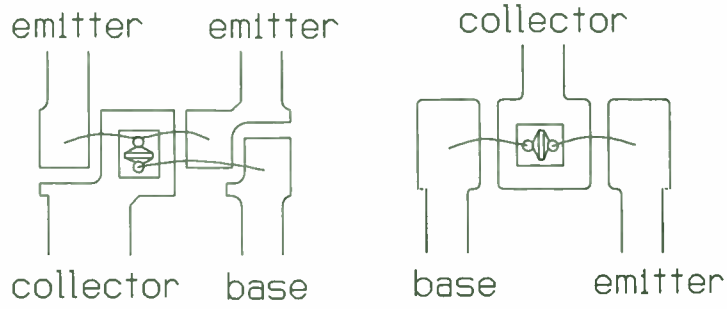


Fig.4 The SOT143 leadframe (left) has a lower Cbcp and Le compared with the SOT23 leadframe (right)

Looking into the BFG505 and the BFG520 types, which have been design-optimized for low current, a better understanding can be realized of the importance of the package. These low current types (die that have an f_T maximum at currents as low as 20 mA or less), have an intrinsic base collector capacitance (C_{bci}) as low as 0.2 pF, even at supply voltages below 2 V, so the leadframe capacitance (C_{bcp}) of the SOT143 at 17 fF is of smaller consequence than the 100 fF of the SOT23 leadframe. The second advantage of the SOT143 package is the emitter inductance L_e, which is approximately one-half that of the SOT23.

Design example: a low current RF downconverter

Target specification

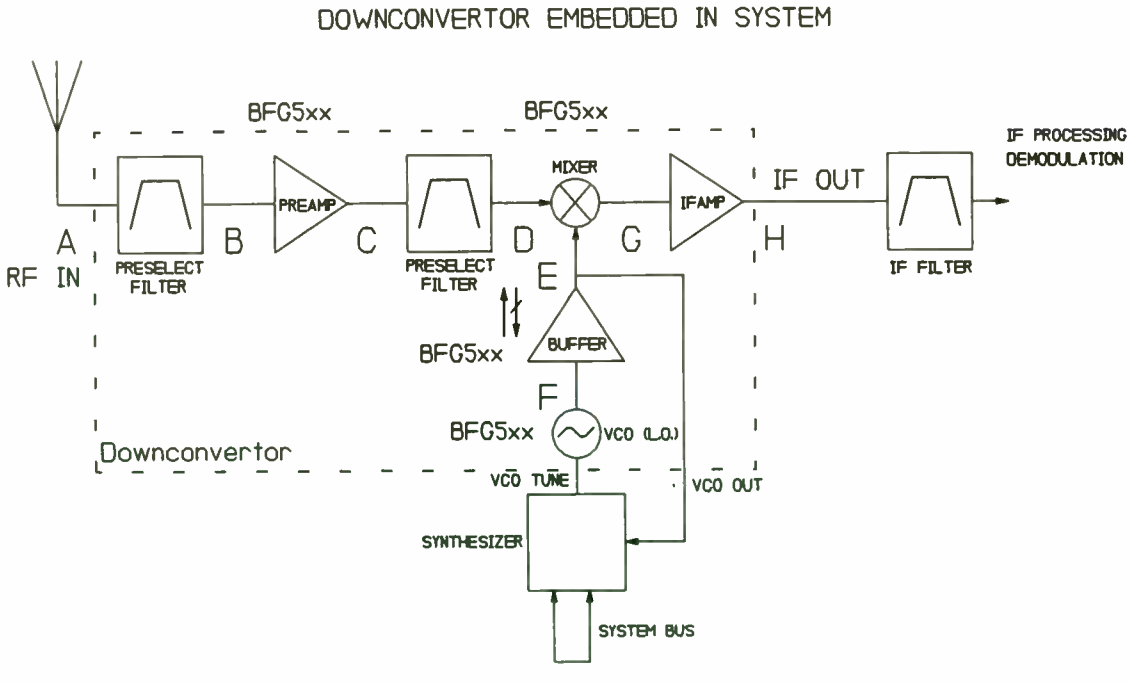


Fig.5 General system configuration of an RF downconverter

Figure 5 on the previous page shows the general system configuration of an RF downconvertor, basically consisting of a LNA, a MIXER and a VCO with a buffer amplifier.
Using the Philips small signal transistors BFG505, BFG520 and BFG540, a RF downconvertor for both the 900 MHz and 1900 MHz band was developed with the following target specification:

Target specification:

RF conversion power gain	:	> 15 dB, typical 20 dB
Noise figure	:	< 10 dB, typical 6 dB
Intercept point (input 3rd order)	:	typical -15 dBm (less important for digital system)
Image rejection	:	> 60 dB
Local oscillator leakage	:	< 1 nW at antenna
Oscillator shift	:	< 1/10 channel spacing
Supply current/ voltage	:	< 20 mA for 3 V supply typ 15 mA

These targets were used to design a 933 to 60 MHz converter (based on a 900 MHz analog CW system) and a 1890 MHz to 110 MHz converter (based on the requirements for the Pan-European DECT system). In actual practice, target specifications will differ from one system to another.
The frequency band is determined by the RF bandpass filters used in the circuits between points A and B, and C and D in figure 5. These filters can be realized using coupled striplines, coaxial or helical resonators, or SAW filters, which will determine size, weight, performance and cost.
In the 1890 MHz design, the BFG505 was used as the LNA, mixer, buffer and VCO. For the 900 MHz design, the BFG505 was used as the LNA and the buffer. Where a higher IP3 is required, the BFG520 could be used for the LNA instead. The BFG520 is used in the mixer for the 900 MHz design as well. For the VCO in the 900 MHz system, either the BFG520 or BFG540 can be used, depending on the phase noise requirements for the VCO.

Power Budget and Gain distribution

It is known that the intercept point (IP3) and the power gain of the converter can be improved by increasing bias current, which also increases power consumption. Because of the presence of a selective filter at the IF output of the converter, the overall IP3 is determined primarily by the mixer IP3. Based on the battery supply limitations, the available current for the mixer is approximately 2mA. Using this as a starting point, the IP3 of the mixer can be calculated or simulated using harmonic balance analysis. Depending on circuitry, for a mixer current of 2 mA and a LO-power of 0 dBm, the intercept point can be calculated to be around 0 dBm at the mixer input.
In order not to degrade the overall intercept point (IP3) of the converter, the input intercept point of the LNA has to be at least -10dBm, which puts a lower limit on the current setting of the LNA. Taking into account a filter loss of approximately 2dB, the LNA gain goal was set to 12dB. The main purpose of the LNA is to reduce the overall noise figure of the converter. To meet the converter gain requirements, the mixer gain should be at least 12dB, again taking into account the filter losses of approximately 2dB per filter.

LNA design

The matching networks at the input and output of the LNA (fig 6) are a compromise between: optimum gain matching, optimum matching for noise figure and optimum impedance matching to the filters. With the help of the Microwave Design System, accurate impedance information for the low noise amplifier can be obtained. The Noise/Gain trade off graphs (fig 7) were created in this way. Matching for optimum noise figure can only be realized at the cost of gain loss. A good match to the filters, while maintaining low noise match, is realized by lossless (no series resistor) feedback, using a small series inductor in the emitter. This can be realized by a small microstripline on the pcb. In the 933 MHz design, the optimum output (collector) matching configuration was omitted and replaced by a simple resistor since the gain loss was small (0.5 dB) and the circuit is smaller. The input coil was realized using a spiral inductor, which makes it smaller.

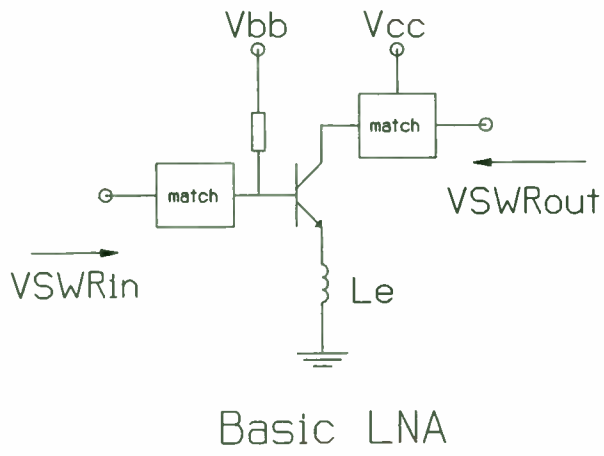


Fig.6 Input and output match for LNA .

The 1890 MHz design is slightly different, with LC-matching at both the input and output which are determined using simple matching techniques. A final simulation will indicate the effects of parasitic circuit losses due to the real matching components, the PCB, etc. Finally, a stability analysis is used to predict if the design is unconditionally stable. While a bypassed emitter resistor is usually makes for worse stability, a small emitter inductor will improve stability. The final schematics are shown in appendix A.

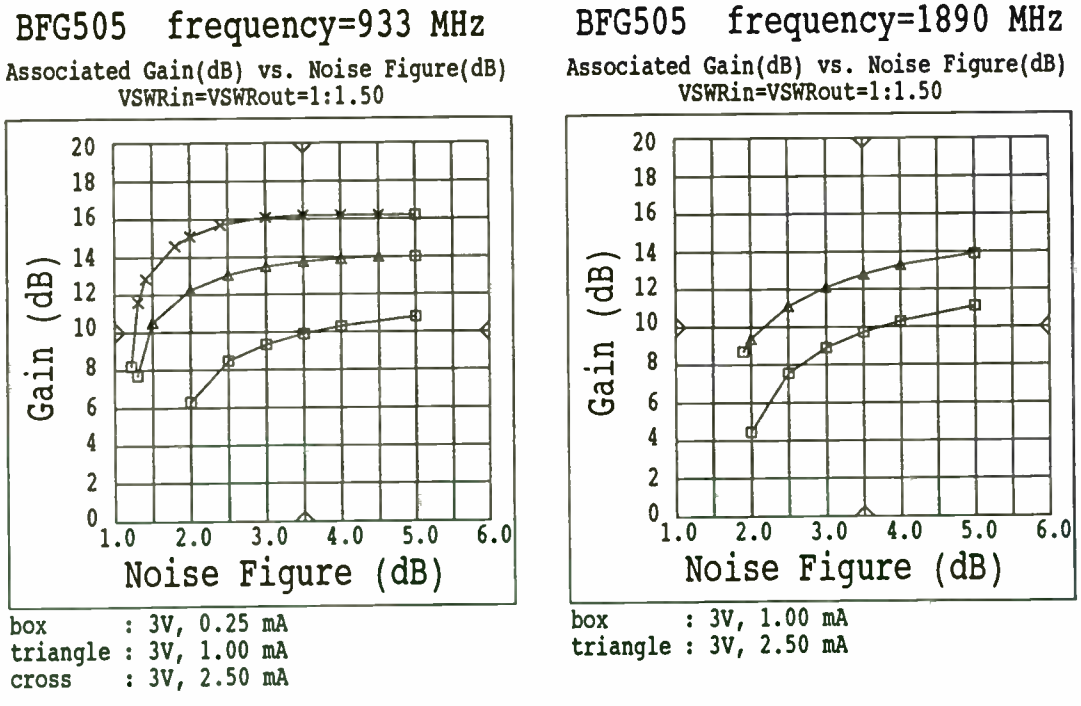


Fig.7 Trade off between noise and gain at different frequencies and currents, matching at input and output.

With the gain selected at 12 dB, the minimum noise figure is about 1.3 dB for a 2.5 mA current, 2 dB for a 1 mA current, 3 dB for a 0.5 mA current. The approximate intercept point is shown in fig 8.
This was also derived from the same circuit, now using a two-tone harmonic balance analysis. The level of the intercept point need not be determined too precisely as it will be influenced by low frequency decoupling in any case. The intercept point at 1 mA is around -9 dBm, this would be sufficient, but to allow for some design contingency 2 mA was chosen. From the optimization using this information it is possible to find the match we need at input and output.

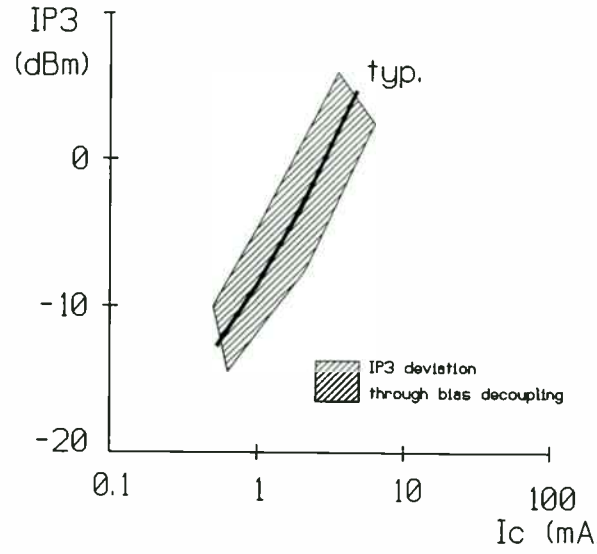


Fig.8 Input intercept point related to Bias current in a Low Noise Amplifier.

Mixer design

An ideal mixer would switch the RF signal at the rate of the LO frequency, would add no noise, and have an ideal transfer characteristic. Non linearity (distortion) is introduced since instantaneous switching is not possible and because of the exponential behavior of the device in the on-state. The new RF small signal devices from Philips are capable of very fast switching at low power levels, because of a high f_T and low capacitances. This is an advantage, because high LO-power levels are difficult to obtain because of the current restrictions of today's systems, which has a direct impact on battery size and weight. The mixing power gain of the "new generation" devices can exceed 10 dB with LO power as low as -10 dBm, depending of course on IF frequency (In most modern superheterodyne receivers, the IF frequency is about 2-20% of the RF frequency. Lower IF frequencies give problems concerning image rejection, higher IF frequencies give problems with the Q-factor of the IF channel select filters.).

The mixer noise figure is affected by:
- Switching; due to switching, conversion of harmonic noise to the same IF frequency occurs. This process is unavoidable in a switching mixer and is one of the reasons why the minimum mixer noise figure is higher than the minimum noise figure of a linear amplifier built with the same transistor.
- Too low LO power; if the amplitude of the converted IF current is too small, it will be lost in the shot-noise current. This is basically why the switching type of mixer is preferable, since the IF current is higher.
- Poor local oscillator signal; noise with its origin in the local oscillator and at intermediate frequency offset will also convert to the IF frequency. This is not affected by the close-in phase noise, but has a wideband character and can be caused by a poorly designed buffer amplifier. Normally, discrete VCO's have a narrowband output match and therefore this is not a problem (the noise is simply filtered-off). This is problem to be aware of when mixer performance is measured with a signal generator as LO, since the wideband noise performance of a signal generator can be poor.
- Image rejection; the internal transistor noise, generated at the image frequency is difficult to filter. Noise out of the LNA can be filtered, and in this case a preselect filter between LNA and mixer can help. However, if this filter has high passband losses, it will have a negative effect on overall noise figure. System noise calculations can give us an idea of these effects.

It is common to specify the DSB noise figure of a mixer. One has to be aware that the DSB noise figure is about 3 dB better than the SSB noise figure, when comparing different mixers. The realistic noise figure is the latter. In the laboratory, typical SSB noise figures as low as 6.5 dB were measured at frequencies between 1-2 GHz. The finally designed mixer had a 8 dB noise figure. The design of the mixer is done directly using the MDS (Microwave Design System). The final circuit diagram can be seen in Appendix A.

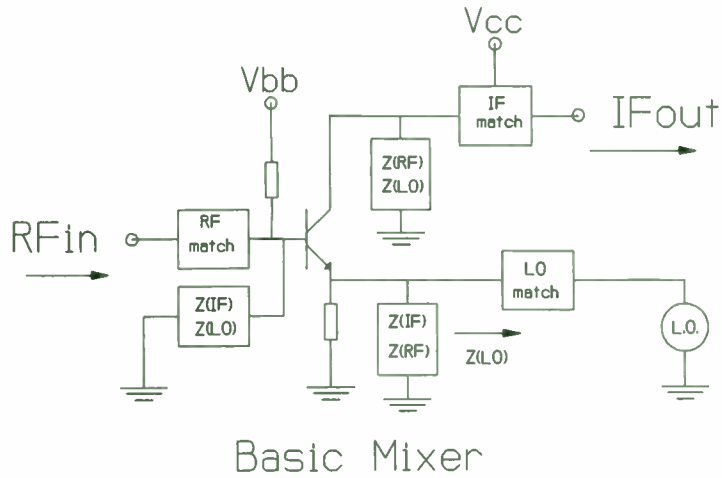


Fig.9 Impedances at all transistor terminals at f(IF), f(LO) and f(RF) are important.

Before designing, the following assumptions have been made (see fig 9): Maximum IF gain occurs when the internal IF current from base to emitter is also maximum. This means that both emitter and base have to be decoupled for IF, providing in effect low Z(IF) from base and emitter to ground in fig 9. To obtain high mixing gain, the emitter must also see a low impedance for RF (low Z(RF) in fig 9). Figure 10 indicates the trade-off between noise, gain and intercept point of a one transistor mixer. Low LO power will cause a decrease of the mixer IP3. To avoid current or voltage clipping of the LO (where LO is the combination of the VCO and buffer), which will result in less LO output power, the LO source impedance was choosen between 30 and 60Ω. Depending on the design of the LO, some impedance matching between LO and mixer might be necessarry to avoid current clipping and thus less LO output power. This can be done by using a small inductor. At the base terminal, a PI-match is used. Optimization can be done in a harmonic balance analysis.

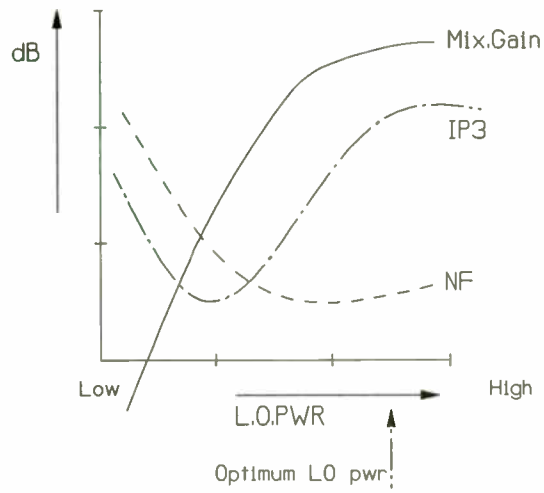


Fig.10 The trade-off between noise and distortion in a single transistor mixer biased at Ic. Higher Ic's shift the optimum to a higher LO-pwr

The choice of using base or emitter as input for RF or LO can be left to the designer. The solution requiring simple circuitry has to be preferred. A little improvement in isolation can be expected when LO and RF are not at the same transistor terminal.

The collector match consists of two parts:
1) Low impedance for f(RF) and f(LO) is needed for RF-IF and LO-IF isolation, which (as the collector is an effective ground at these frequencies) also eliminates some influence of the C_{bc} Miller effect.
2) The IF matching is basically done using the diagram in fig 12. A practical value for the collector load resistance is 1-3 kΩ. A large mixing gain can be achieved since the collector terminal is almost a perfect current source at IF. If two IF coils are a problem, a single transformation section could be used at the cost of a somewhat lower gain if tuning is to be avoided. Higher loads give problems with matching complexity and linearity, as a IF voltage that is too high also results in saturation and a decreased linearity.
Matching can be made spread insensitive using an optimization method. In the simulation the values of the matching elements are optimized for constant load impedance, and the absolute values are swept between -10% and 10%. This results in a conversion gain vs. frequency as shown in fig. 11.

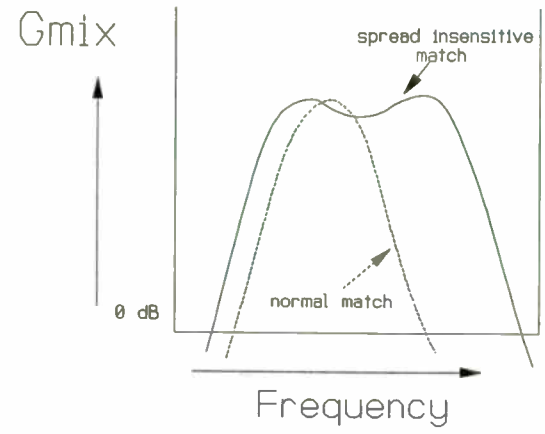


Fig.11 Frequency response of spread-insensitive IF matching. (no sharp optimum)

Care must be taken in using a good model for the small SMD coils used for IF matching. In particular the first parallel resonance must be modelled (parallel capacitor). See Appendix B for the layouts of mixer and preamp (LNA).

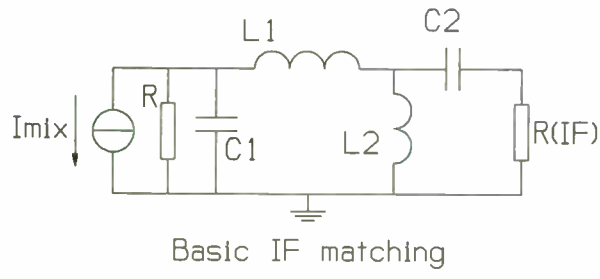


Fig.12 Possible realization of IF match with lumped elements.

Local Oscillator (Buffer and VCO)

The buffer amplifier is a neutralized amplifier that uses no matching. Neutralization is provided by an SMD inductor which tunes out internal feedback capacitance to improve isolation by more than 10 dB. Better isolation improves the pulling resistance of the VCO. (VCO pulling is the frequency shift due to load variation). A VCO with a poor pulling resistance can cause a reduction of the IP3 of the convertor. The pulling is caused by RF signals entering the VCO because of the low mixer isolation, and thus FM modulate the VCO, causing FM sidebands. These FM sidebands can not be separated from the 3rd order distortion products, and are thus seen as an IP3 reduction of the converter.
To improve the buffer isolation, resulting in a better pulling figure for the LO, a buffer amplifier with two transistors in cascode configuration (fig 13) could also be used. Another way to improve isolation is to use a balanced mixer which can be made with a pair of differential transistors.

The oscillator is a colpitts with stripline resonator. It delivers about 0 dBm of output power and puts the buffer into gain compression. Operating the buffer in gain compression will increase efficiency and eliminates variations in oscillator power due to component spread.

The advantage of using these transistors for buffer/oscillator are clear: low device capacitance gives improved isolation, and low base resistance in the oscillator gives low phase noise. Layouts are given in Appendix C.

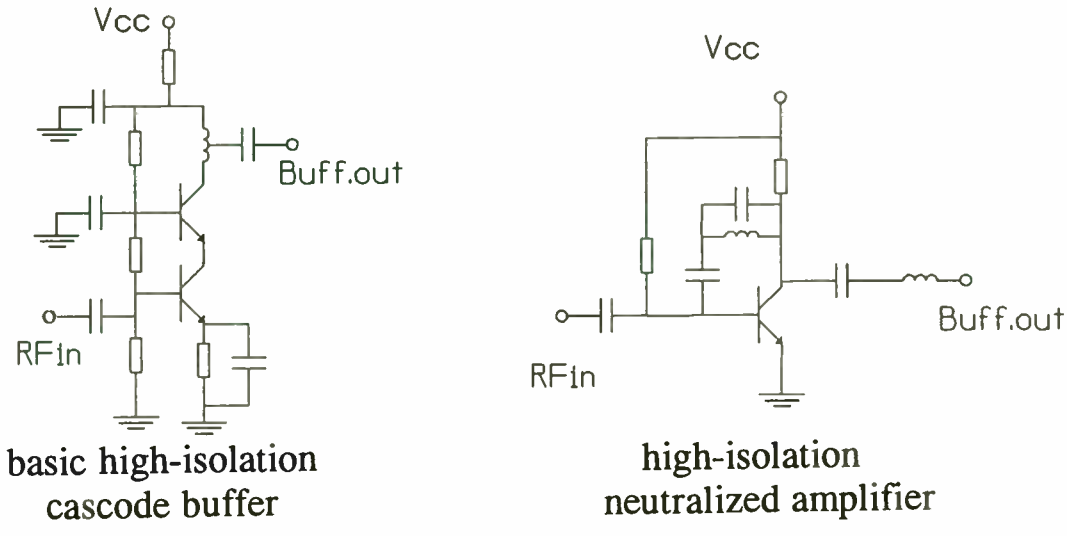


Fig.13 Two possible ways of realizing a buffer amplifier, with two transistors (left) or with an extra coil (right). The first solution is wideband, the second narrowband. Performance is about equal.

Biasing circuits

In low voltage circuits the method of bias point stabilizing by putting a resistor in the emitter is avoided as this will drop the available voltage across the collector to emitter even more when it is already quite low. When the emitter of the RF transistor is grounded without a series emitter resistor, the DC bias stabilization is still needed to provide compensation for temperature and h_{FE} changes. Another way is to put a resistor in the collector supply with a feedback resistor tying the collector back to the base. Then an increase in collector

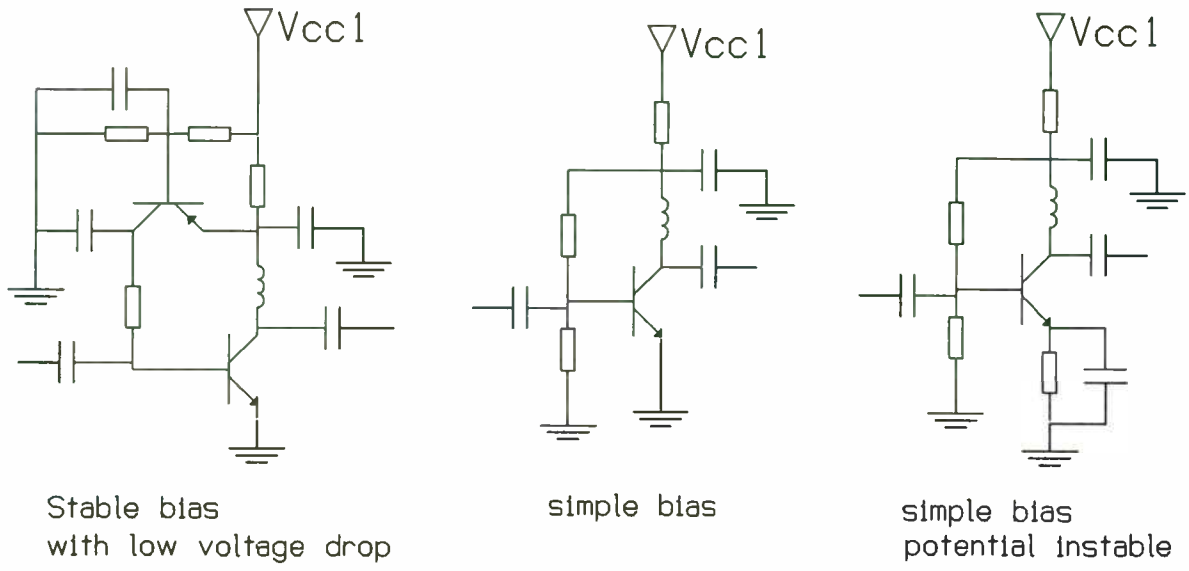


Fig.14 Three ways of biasing an rf transistor

current will cause a larger voltage drop over the collector resistor, thus also lowering the base voltage. Because of the high gain of the transistor, this is (even at 3 V supply) not a serious problem. However, this method will not eliminate completely the effects of h_{FE} spread. The designer must decide if the bias point shift has a detrimental influence on the performance. Selection on a narrow h_{FE} range is very undesirable. To overcome the biasing problem in this design, a low frequency PNP transistor was used to stabilize the current of the preamp and buffer. This biasing method may not be absolutely necessary, and if reduction in the number of components is more important, the biasing circuits would be an area to reduce the parts count.

Measurement results

Total system measurements are shown in Appendix D. The design easily fulfills the target specifications as indicated in the table below.

fin= 931/1890 MHz; fout=60/110 MHz; (fLO=871/1780 MHz tuned by means of Vtune)

SPEC	VALUE (933/1890 MHz converter)	REMARKS
CONVERSION POWER GAIN	typ. 20 dB/21 dB	includes filter losses
NOISE FIGURE	typ. 5.5 dB/6.5 dB	includes filter losses
IP3	typ. -10 dBm/-15 dBm	at input
1 dB COMPRESSION	typ. -3 dBm/-8 dBm	at output
LO RADIATION	< 100 pW/<1 nW	on RF input
OSCILLATOR SHIFT	< 5 kHz shift LO	RF input < 10 dBm (free running oscillator)
IMAGE REJECTION	typ. 78 dB/60 dB	imagefreq=811/1670 MHz
SUPPLY VOLTAGE	typ. 3.3 V	Vcc1=Vcc2
SUPPLY CURRENT	typ. 11 mA	mixer/pre= 4 mA LO/ buff = 7 mA
VCO CNR(1Hz)@100 kHz (phase noise)	typ -110 dBc/-105 dBc	not optimised
REPRODUCABILITY	GAIN +/- 0.5 dB	no alignments
BOARD SIZE	28x16x6 mm 15x23x2 mm	preamp+mix+filt. LO+buffer
PCB material	epoxy FR4 h=0.5 mm	Er=4.6
in/load impedance	50 Ohm	at meas. frequency

Comparison of different Technologies.

When comparing receiver performance, the Spurious Free Dynamic Range is a good performance related parameter. Because it depends on information bandwith, it is better to normalise it in a certain bandwith, for instance 1 MHz. The SFDR(1MHz) depends on the IP3 and the Noise Figure according to the following formula:

SFDR (dB, 1MHz) = 2 x (IP3 +114-NF)/3 with IP3 in dBm and NF in dB.

which in this case = 66dB.

If we take into account the low supply power (only 35 mW), the SFDR(1MHz) of 66 dB is outstanding. The system SFDR greatly depends on mixer IP3 and a system built with devices with a higher inherent gain (such as GaAs devices) does not give a higher SFDR, because the gain requirement for a receiver downconverter is not to make it as high as possible but rather to provide an adequate gain. Bipolar devices already satisfy this gain requirement and the LNA matching can be almost noiseless (in an integrated solution, this is not possible). Furthermore mixer IP3's are comparable for both technologies. Because the high Q image reject filters and VCO resonator cannot be integrated, the size advantage of an integrated solution such as MMIC or silicon IC dissapears. In short, a discrete bipolar solution offers GaAs MMIC performance at even lower current, and in a comparable size at a lower price. The only disadvantage of a discrete solution could be the design complexity, but with modern CAD tools and device characterisation this is no longer a problem.

Conclusions

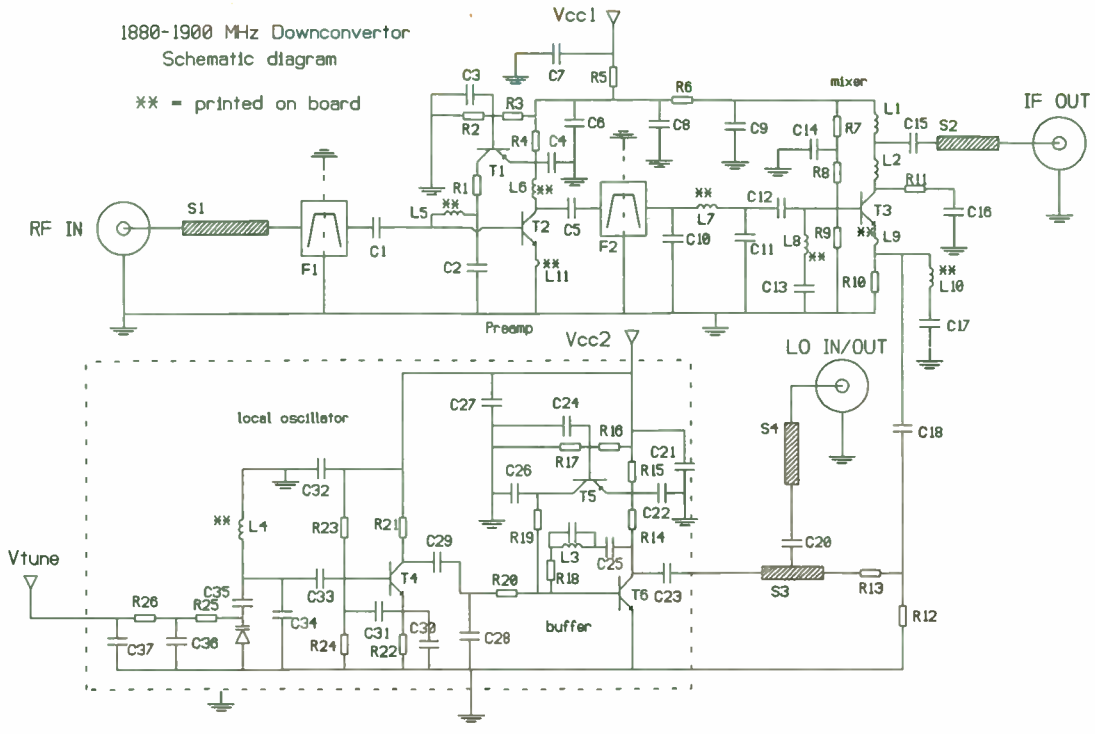
A very competitive discrete semiconductor downconvertor has been developed:

- Small board size; the combination of the mixer/preamp including the filters is mounted in an area of (28x16x6) mm. When using the new SOT343/SOT323 components and when multilayer techniques are used, the size can be smaller. Because it remains impossible to integrate the preselect filters, no 'Integrated' superheterodyne converter can be much smaller.
- Very low current consumption.
- Spread insensitive, no tuning points needed except for the LO frequency adjustment. The traditional argument (spread sensitive) against a discrete solution can be put aside with todays CAD possibilities and yield analysis.
- Low price; SMD bipolar transistors are already in mass production for a long time and the technology is mature.
- Maximum design flexibility. The circuit is everywhere accessible.

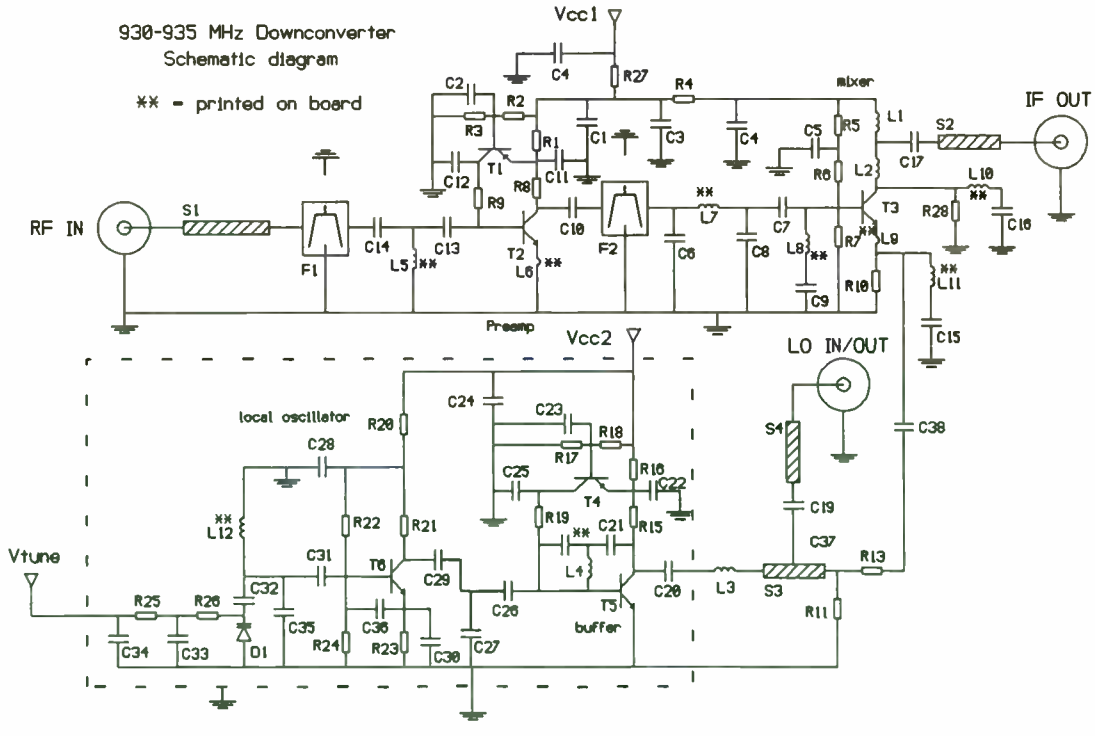
References

For a detailed description of the circuits, reference is made to Philips Semiconductors Application notes:

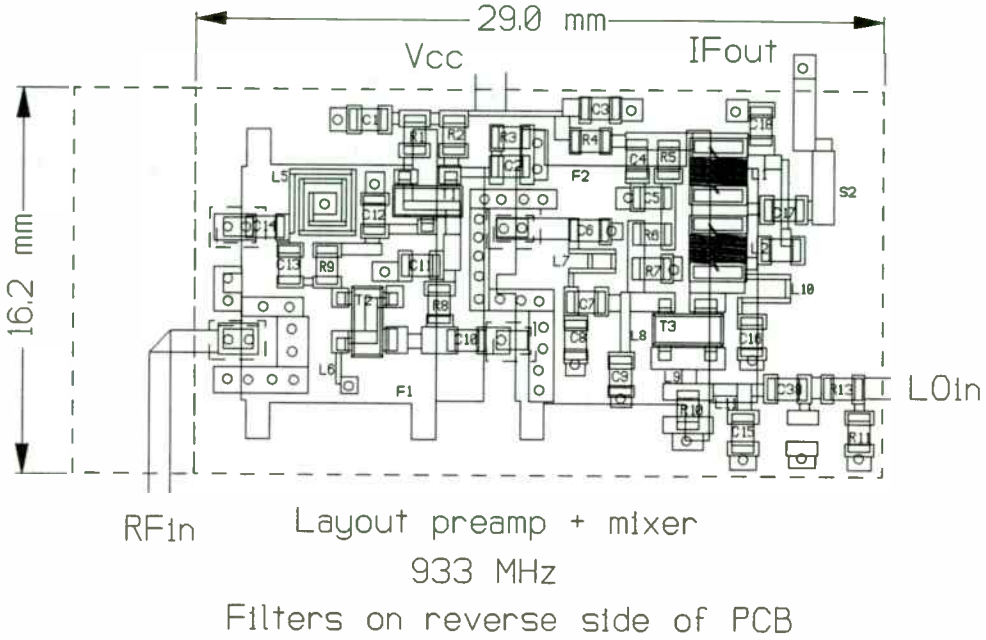
1. 1890 MHz low power Downconverter ..... RNR 45/464/1993
2. 933 MHz low power Downconverter ..... RNR 45/465/1993



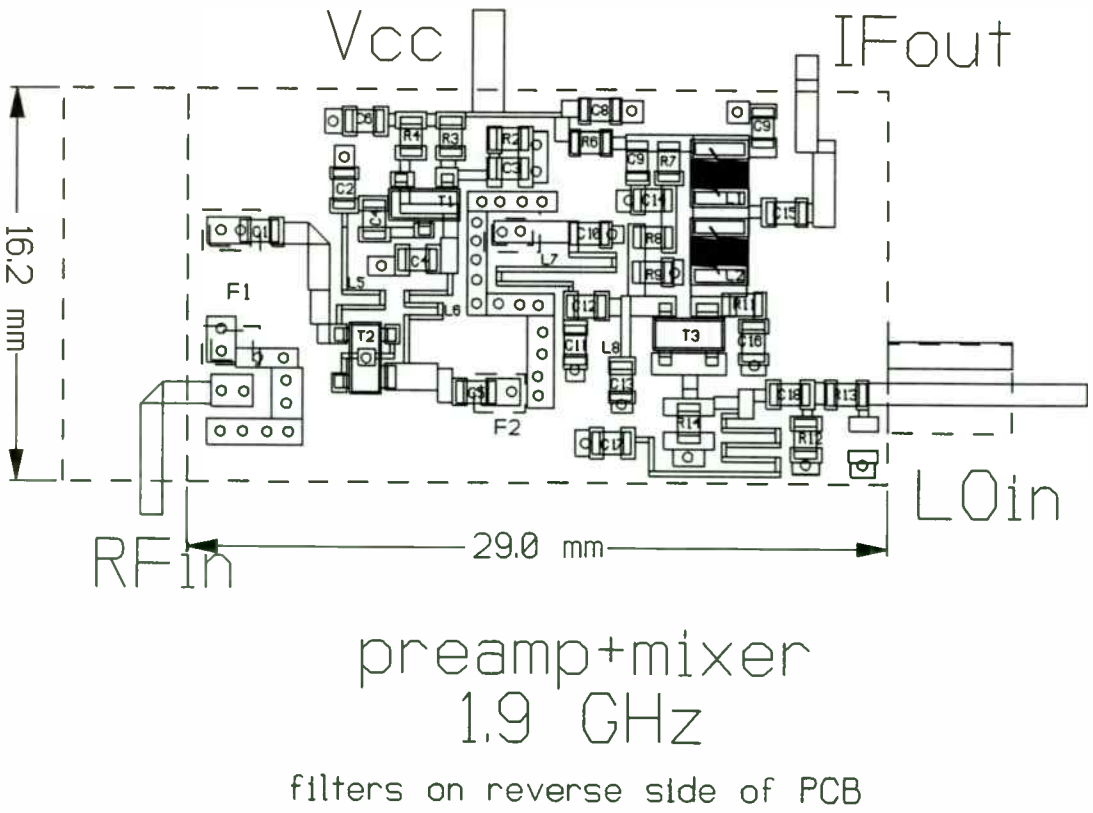
schematic diagram 1890-110 MHz converter.



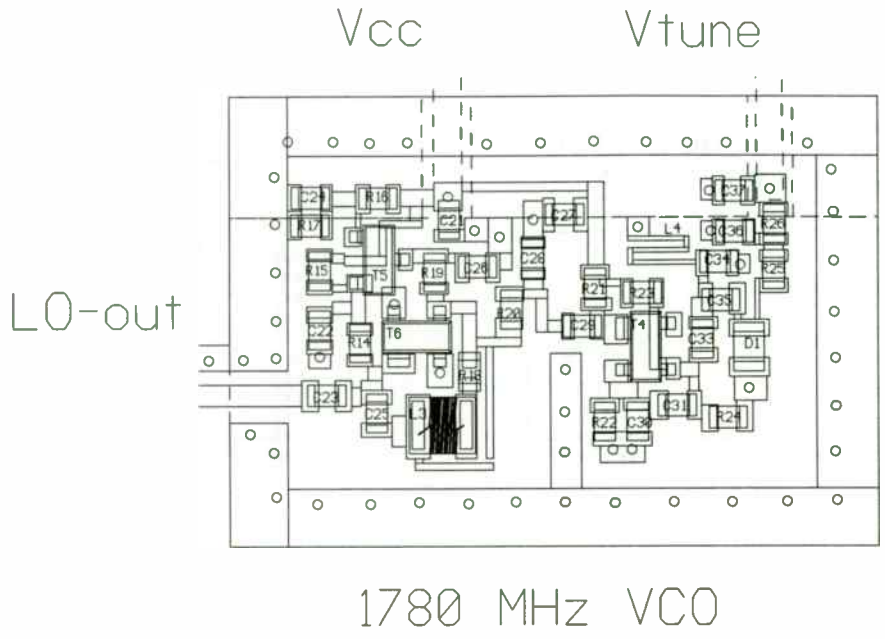
schematic diagram 933-60 MHz converter.



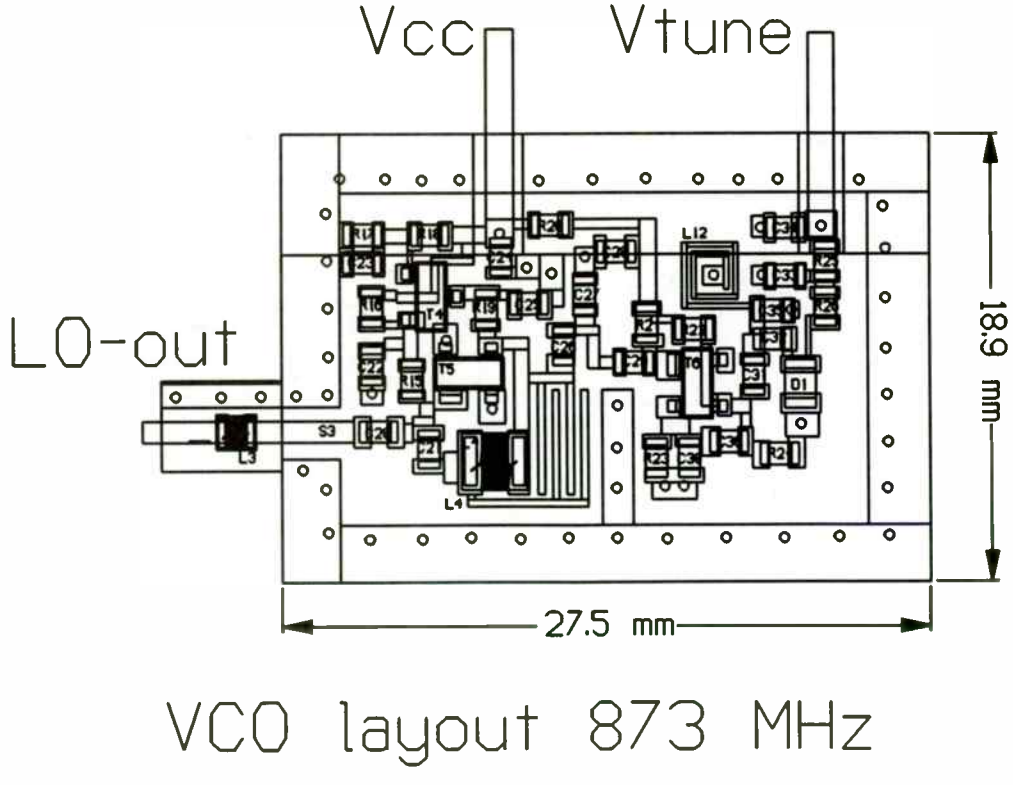
layout preamp+mixer 1890 MHz



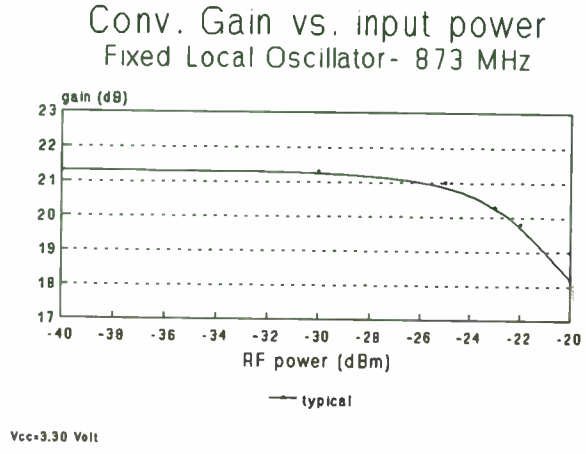
PCB layout preamp+mixer 933 MHz



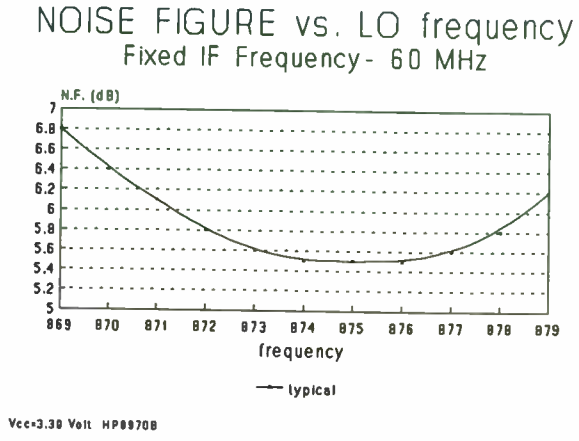
PCB layout VCO 1780 MHz



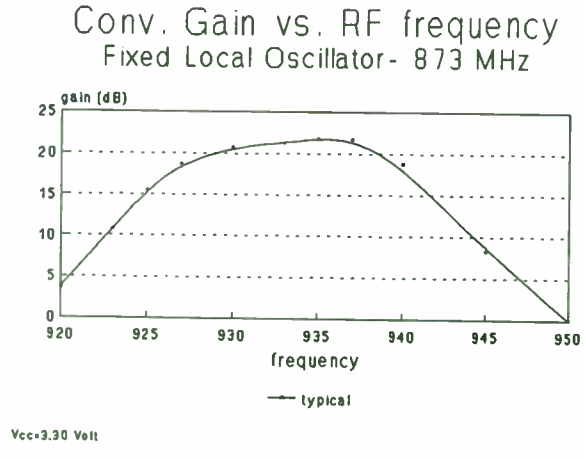
PCB layout VCO 873 MHz



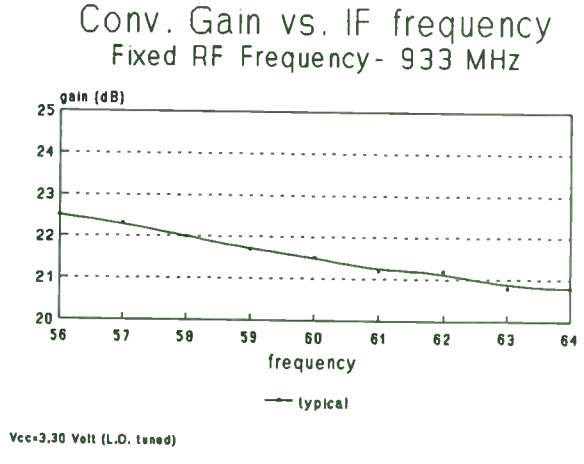
gain compression (933 MHz converter)



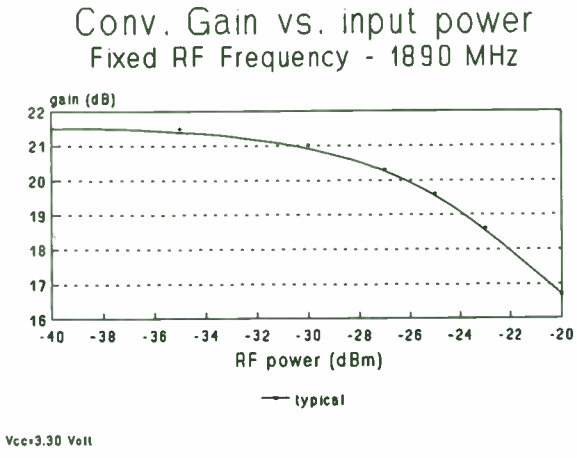
noise figure vs frequency



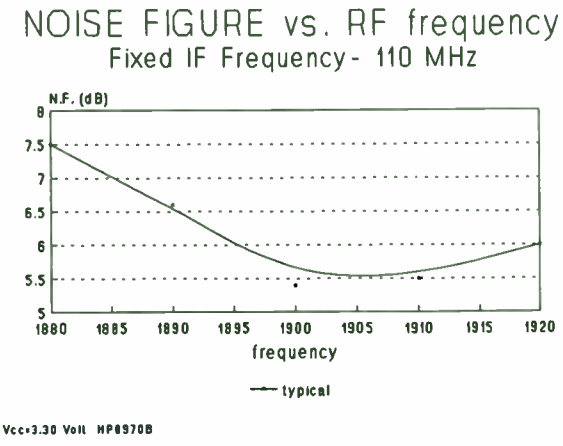
conv. gain vs rf input frequency (933 MHz)



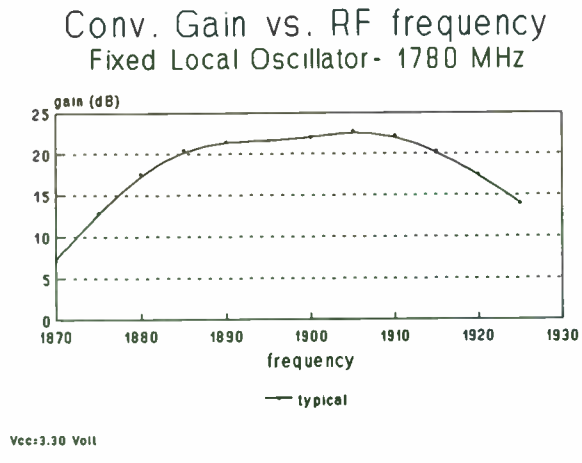
conv.gain with variable IF frequency (933 MHz)



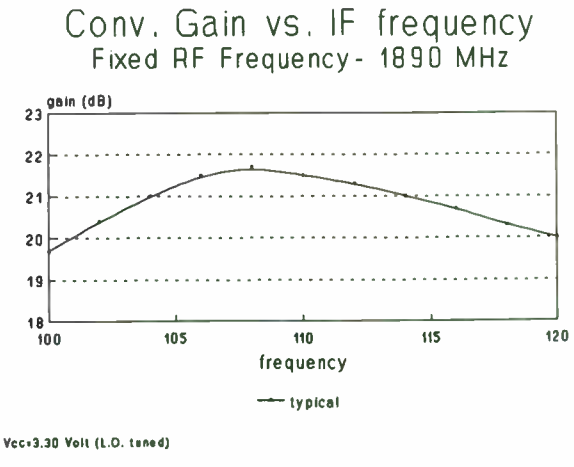
Gain compression (1890 MHz)



noise figure vs input frequency



conv. gain vs RF frequency (1890 MHz)



conv. gain with variable IF frequency.(1890 MHz)

Low Power GaAs MMIC Down Converter for Portable Communication Applications

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Abstract

A low power GaAs MMIC amplifier/mixer was designed and characterized for portable communication applications in the 900 MHz band. A complete receiver system was built using the GaAs LNA and mixer IC, cascaded with a narrowband FM double conversion receiver IC (MC3363DW) and an audio amplifier(MC34119D). The single chip integrated front-end IC (90 mil X 110 mil) achieved -118.9 dBM sensitivity at the cellular band. The extremely low power dissipation, high level of integration, and very good RF performance of this MMIC down converter make it an ideal candidate for portable communication applications.

Introduction

In portable communication units GaAs MMIC receivers lead to a reduction in the number of parts and interconnects and, hence, their size and weight. However, to conserve the battery drain in portable units, devices and circuits have to be designed to operate at very low current levels. Enhancement mode and depletion mode MESFET MMIC amplifiers with excellent RF performance at low current levels have been published by several authors(1-5).

This paper reports on the development of a GaAs MMIC down converter with low power dissipation for portable communication applications. A single chip down converter consisting of GaAs low noise amplifier and dual gate FET mixer was designed, fabricated and characterized. A key feature of the circuit is the utilization of on-chip lumped LC matching circuits to realize small size and to lower power dissipation.

Circuit Design

The goal of this project was to demonstrate a monolithic single chip amplifier/mixer to meet the front-end receiver needs in 800 - 900 MHz portable communication equipment. The system requirements dictated that down converter chip should operate at a total current of 3 mA at 3.0 V and LNA should achieve ≥12 dB gain and ≤3.5 dB noise figure. In addition, the mixer should have on-chip matching except for the IF at 45 MHz. The down converter IC should also meet the receiver sensitivity requirement of portable applications (-112 dBm to -121 dBm)

The first step in the design of the IC was to develop a GaAs MESFET technology for the low current application. Several GaAs MESFET lots were characterized and noise figure parameters were measured in a system specially designed for low current measurement. In order to minimize the current drain and to achieve the required RF performance, devices with gate widths of 400 µm, 600 µm, 800 µm and 1000 µm were modeled. Based on this study, a two stage LNA utilizing 600 µm MESFET and a dual gate FET mixer were designed to meet the design objectives. Dual gate MESFET was modeled as a cascode combination of two single gate MESFETs. Several matching techniques were also explored. Even though active matching would have decreased the chip size, it was not pursued due to higher power consumption. Off-chip matching approach was also not utilized since it resulted in larger chip size. An on-chip lumped element LC matching network was found to be the best approach to minimize the size and power dissipation.

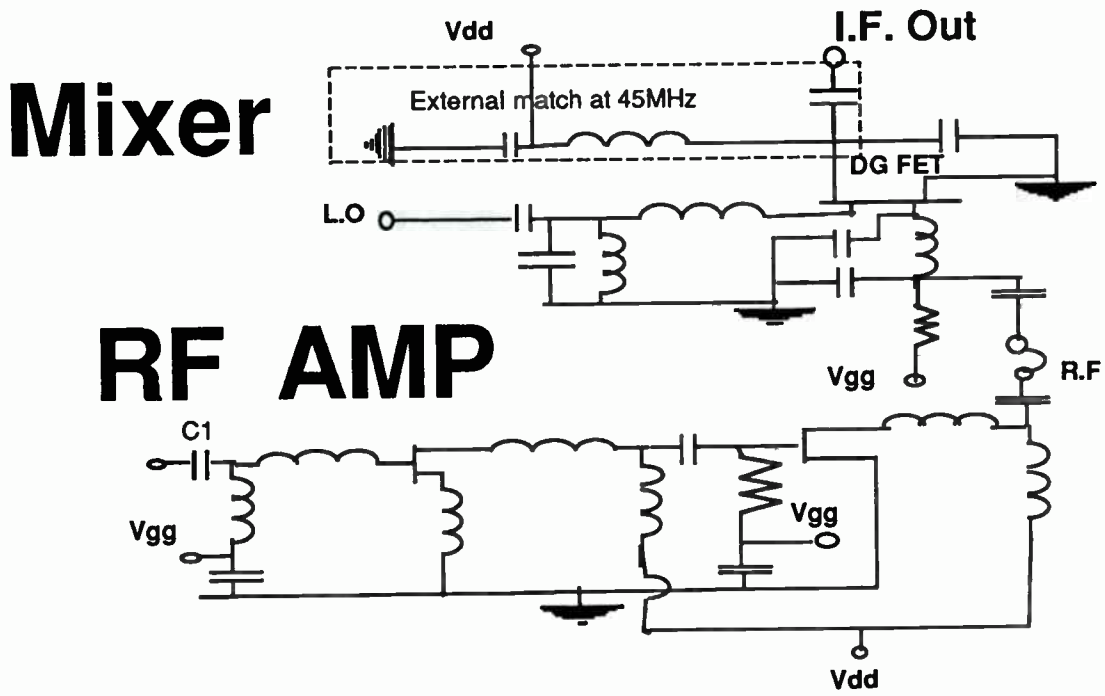


Figure 1. Down Converter Schematic

The circuit was optimized to give the frequency response and return loss as close to the design goal as possible, while maintaining unconditional stability inside and outside the frequency pass band. The only external matching used in the circuit was for the mixer IF port at 45 MHz. Monte Carlo analysis was employed to study the sensitivity of the circuit to variations in component values due to fabrication tolerances. The circuit was laid out to facilitate on-wafer characterization of the amplifier and the integration of a single amplifier/mixer circuit. Fig.1 shows the schematic diagram of the GaAs down converter MMIC.

Fabrication

The wafers were fabricated using a 0.7 μm GaAs MESFET MMIC process. This process employs ion implanted MESFET with Ni/Ge/Au ohmics, Ti/PT/Au Schottky gate and two level metal interconnects with no airbridge, and no via holes. The Si_3N_4 MIM capacitors and 3μm thick Au inductors were fabricated for on-chip matching of the circuits. The fabricated die (chip size 110 mil X 90 mil) is shown in Fig. 2.

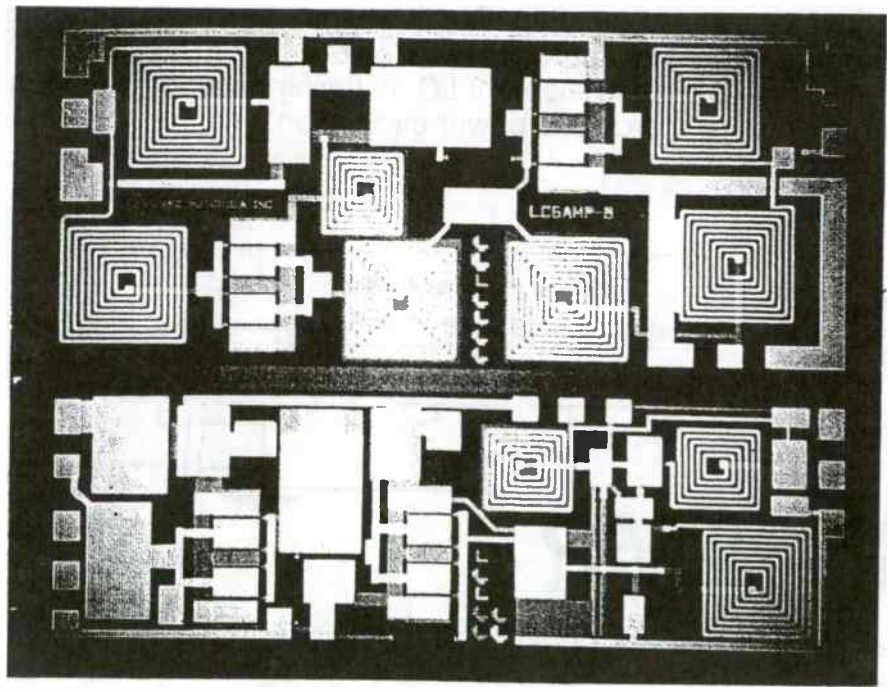


Figure 2. GaAs MMIC Down Converter

Results and Discussion

Low Noise Amplifier

The gain, return loss, noise figure and intermodulation characteristics of the LNA were measured on-wafer using an integrated test system developed in-house. The measured gain and return loss of the amplifier are plotted in Fig. 3. Amplifier achieved a peak gain of 16 dB and better than 10 dB return loss at a drain current of 1. 5 mA @ 3.0 V. The output third order intercept point for the amplifier was calculated from the two-tone measurement. The RF characteristics of the amplifier were measured at 3V and 1V for different current levels. Fig. 4 shows gain, noise figure and the third order intercept point of the amplifier at different bias levels. At 880 MHz, LNA achieved 13 dB gain and 3.6 dB noise figure at Idd =1.5 mA and Vdd = 3.0V. At Idd = 2mA and Vdd = 1.0 V a gain of 12 dB and noise figure of 3.5 dB was achieved.

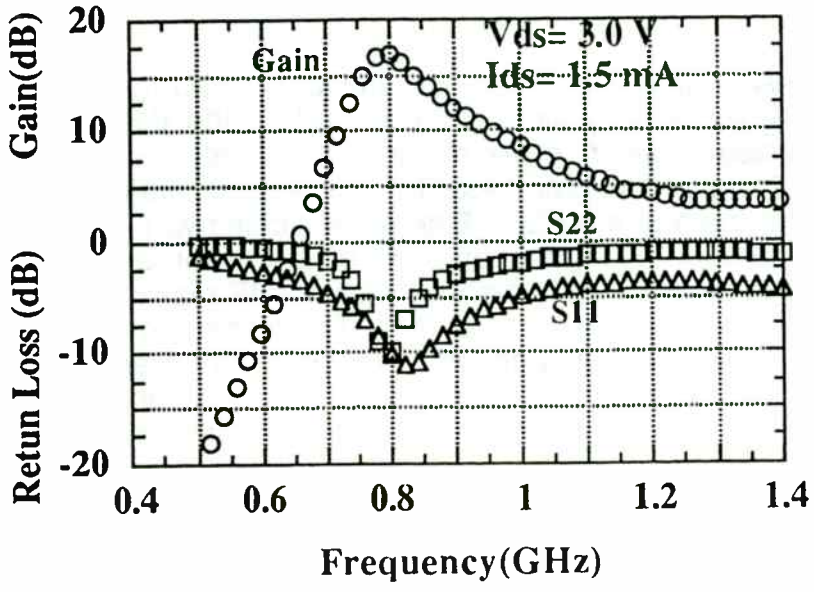


Figure 3. Measured Frequency Response of the LNA . Vds= 3.V, Ids = 1.5 mA

The intercept point of the amplifier exhibited a strong dependence on the supply voltage. At 2mA of bias current, IP3 decreased about 4 dB when the drain voltage was decreased from 3V to 1V.

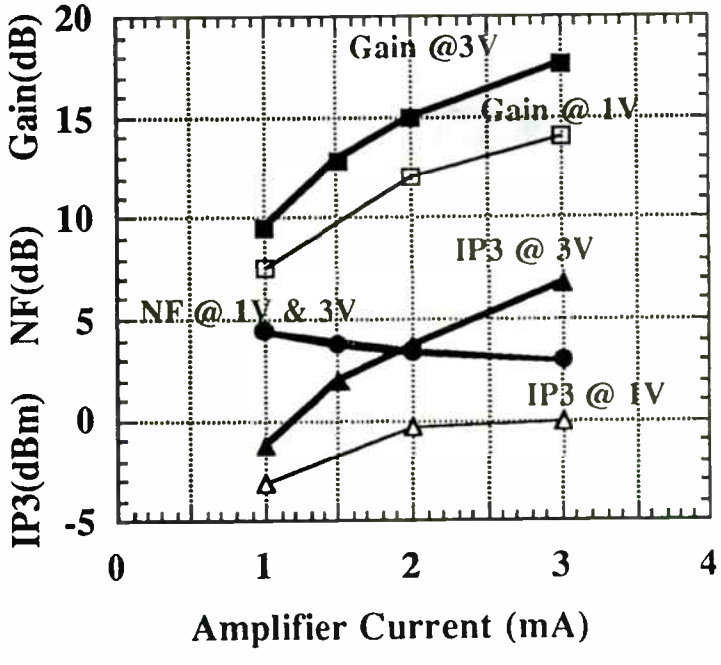


Figure 4. Gain, NF and output IP3 of the LNA for different bias levels (F = 880 MHz)

Dual Gate FET Mixer

Mixer conversion gain was measured on-wafer using the system displayed in figure 5. The RF input was applied to the gate 1 of the dual gate FET. On chip matching was provided to achieve the required frequency response. The L.O. was applied to the gate 2 of the dual gate MESFET with appropriate on-chip matching. The IF is taken out of the drain of the FET. External matching was needed only IF stage. No IF amplifier was used in the measurement of the mixer characteristics. The on-wafer conversion gain measurement reported includes IF matching network losses.No IF amplifier was also used in the measurement. The measured conversion gain of the mixer at Vds= 3.0 V, Ids= 3.0 mA is shown in Fig. 6. The mixer exhibited a minimum conversion loss of 3 dB. The conversion loss were also measured as a function of the gate 1 and gate 2 voltages and L. Power, These results will be reported at the symposium.

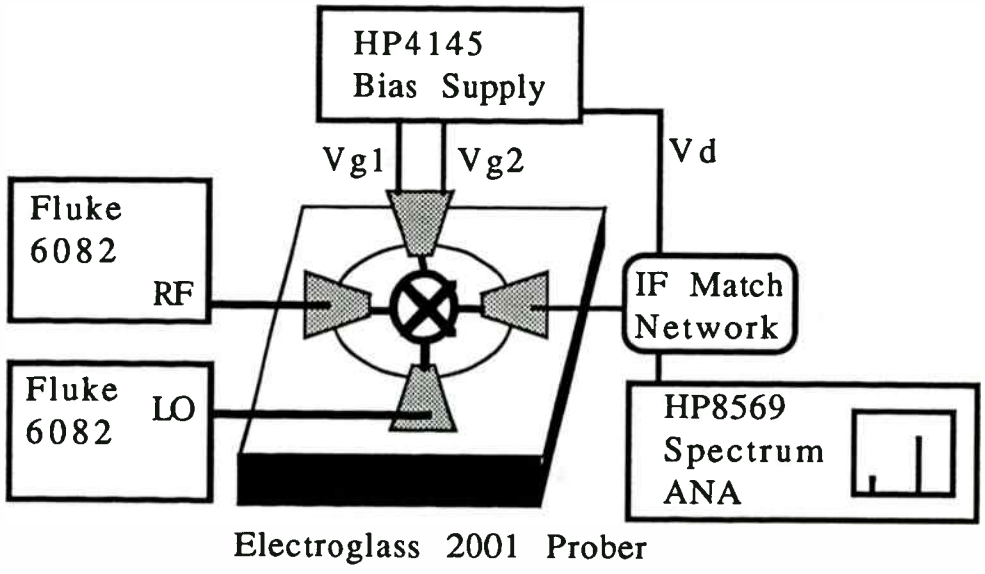


Figure 5: On Wafer Test System for Mixer Evaluation

Down Converter IC

In order to evaluate the performance of the gas LNA and mixer ICs, the wafers were thinned, scribed and assembled in the 14 pin SOIC and ceramic packages. A complete receiver system was built using the GaAs LNA and mixer IC cascaded with a narrow band FM double conversion receiver IC (MC3363DW) and an audio amplifier (MC34119D). The 12 dB SINAD sensitivity was measured using a communication system analyzer (Motorola Model 2600A). Figure 7 shows the block diagram of the test system. 12 dB SINAD is a specified standard for sensitivity measurement of professional radio receivers such as land mobile and cellular radios. The measurement is specified in the Electronic Industries Association (EIA) Standard, RS-204-C.

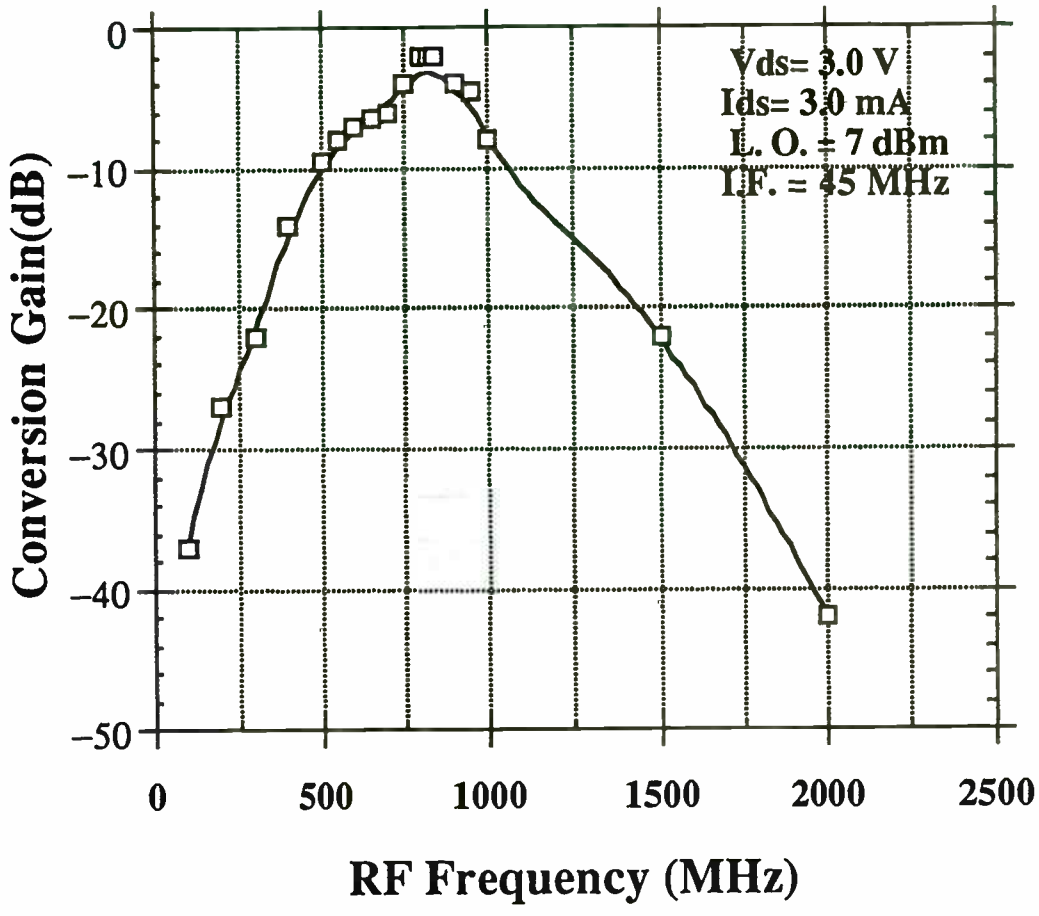


Figure 6. Conversion Gain of the mixer IF= 45 MHz

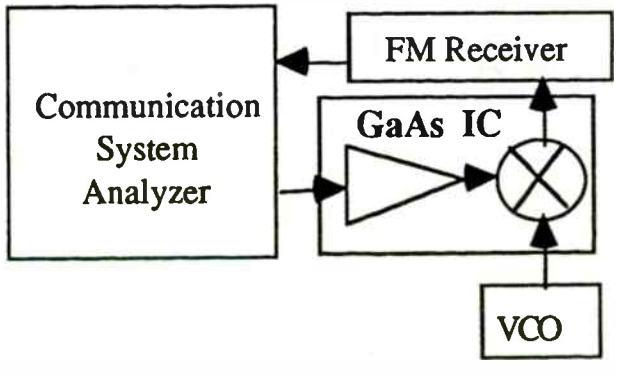
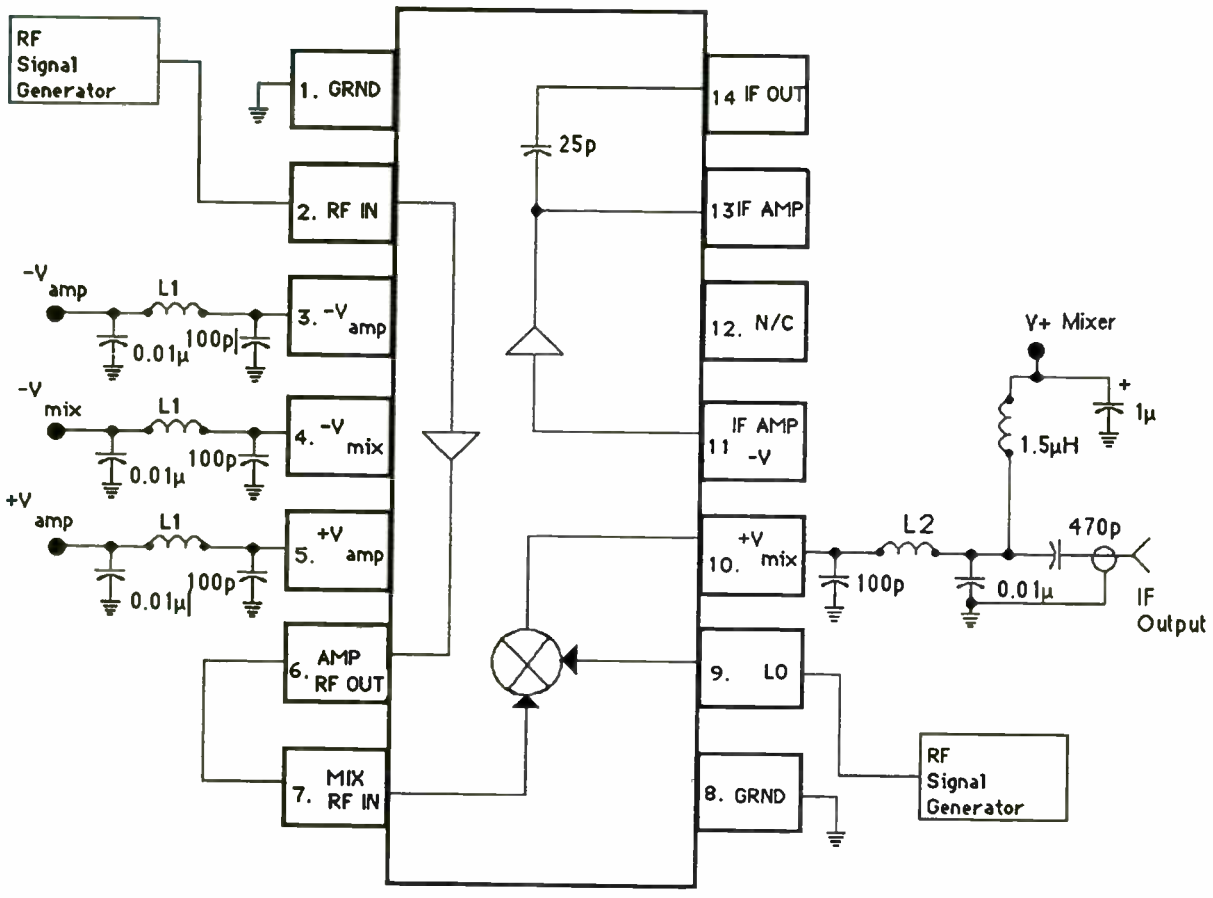


Figure 7. Receiver Sensitivity Measurement System Configuration

Figure 8 - GaAs MESFET Down Converter

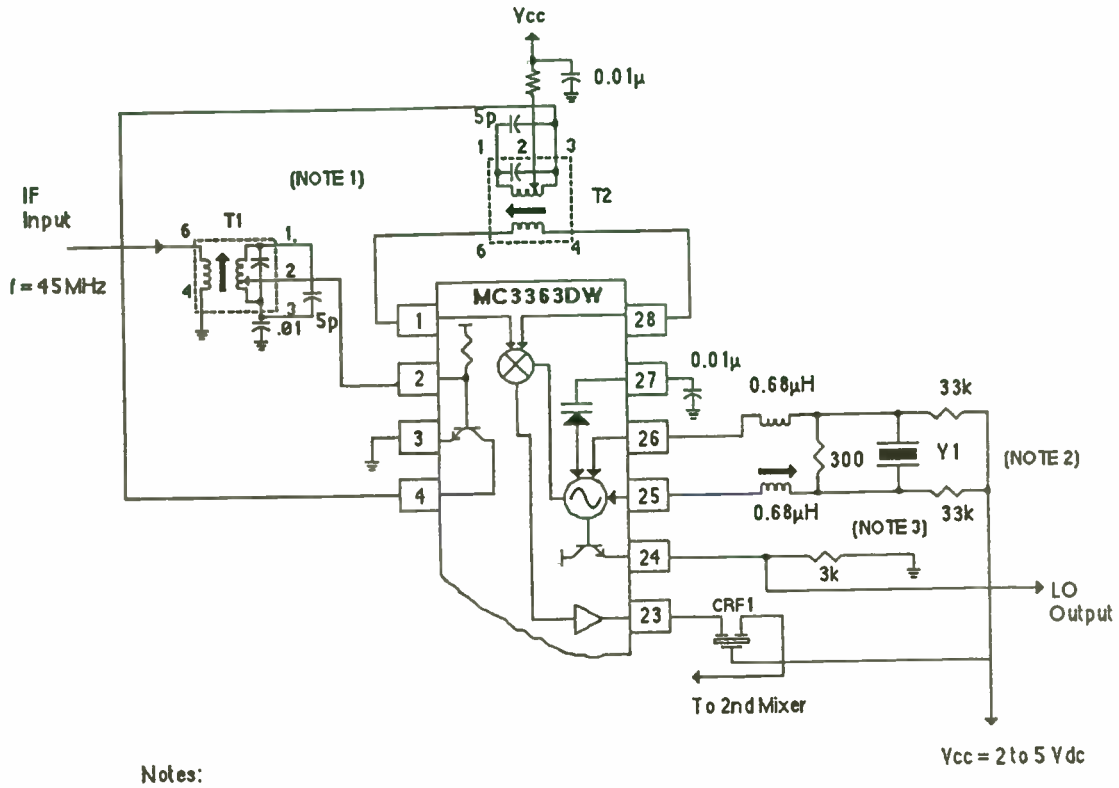


L1 = 5 turns, 1/16" I.D.
#24 AWG enameled wire

L2 = 4 turns, 1/4" I.D.
#20 AWG enameled wire

(1) Post IF Amp may be used as an IF Amp with 390pF-470pF coupling caps or as an RF Amp for L.O Driver with 25pF coupling cap. RF Input and interstage matching can improve performance.

Figure 9 - Interstage Matching to MC3363DW



Notes:

(1) T1 and T2 are 7mm Shielded Transformers - Toko Part # 291GCS-5810N.

(2) Y1 is 34.3 MHz Series Resonant, 3rd Overtone Crystal.

(3) CRF1 is a 10.7 MHz Ceramic Filter, Murata Erie Part # SFE10.7MJ-A.

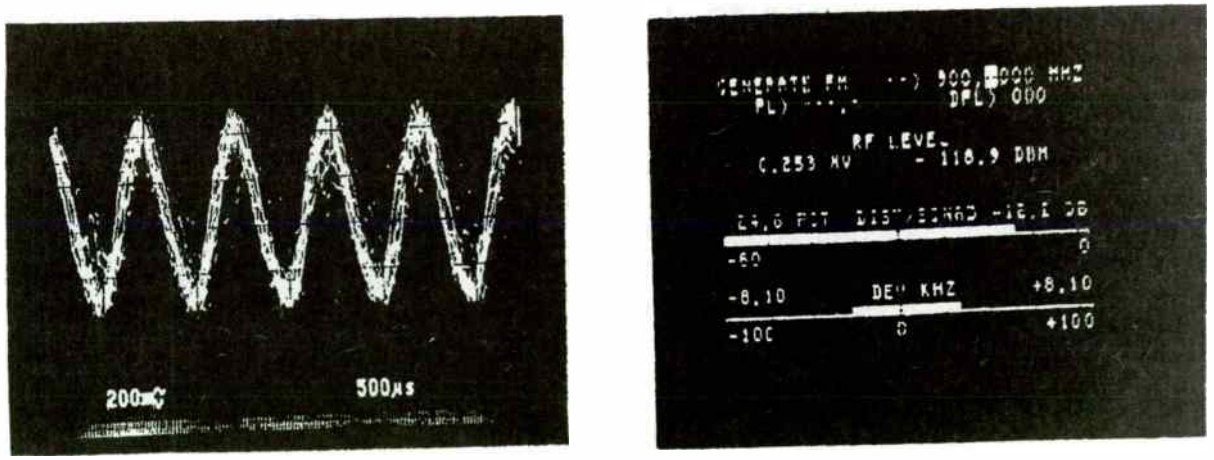


Figure 10. Down Converter Sensitivity - Measured Result. (a) Recovered Audio Signal at 12dB SINAD (Corresponds to 25% distortion). (b) Communication Sytem Analyzer Plot. RF = 900 MHz

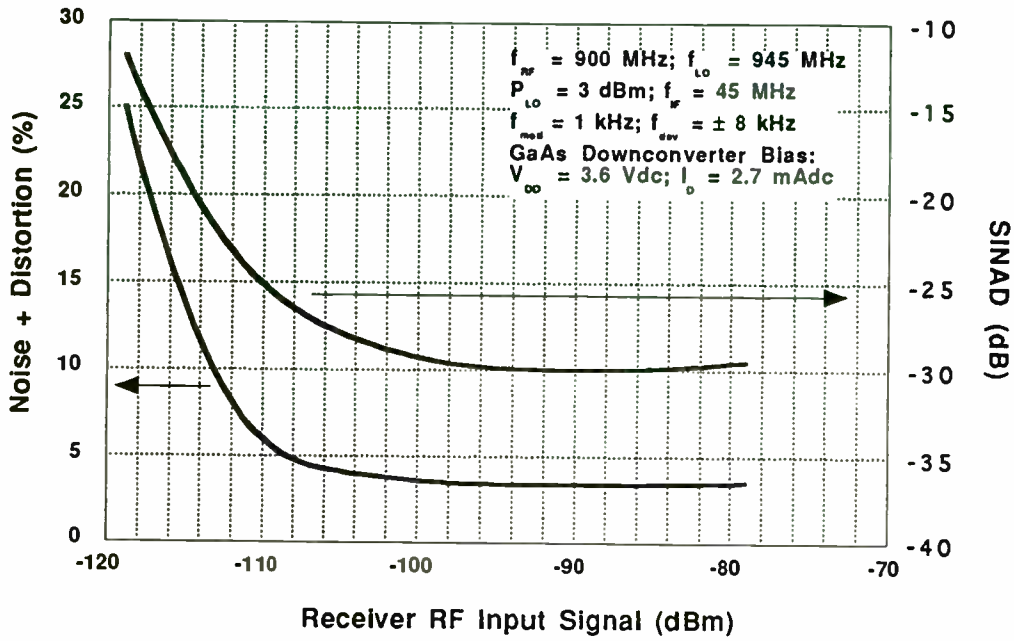


Figure 11. SINAD and Noise + Distortion versus Receiver RF Input Signal Level

The GaAs MMIC down converter and its external circuit is shown in Figure 8 Interfacing the 1st IF output of the dual gate MESFET mixer to the back end narrowband receiver is accomplished using bandpass interstage matching networks with the on-board transistor preamplifier in the MC3363DW (Figure 9 Interstage Matching to MC3363DW). The MC3363DW narrowband receiver has excellent sensitivity at 45 MHz (12 dB SINAD of better than -119 dBm). Refer to the device data sheet for details of the full circuit (MC3363DW/D).

The measured receiver sensitivity of the complete receiver system is shown in figures 10a and 10b. The input signal conditions are f_{RF} = 900 MHz; f_{LO} = 945 MHz and a modulation frequency of 1 kHz with a frequency deviation of ± 8 kHz. The GaAs down converter is biased at Vdd = 3.6 Vdc and a total drain current of 2.7 mAdc. A 12 dB SINAD sensitivity of -118.9 dBm was achieved . In figure 11, a plot of the SINAD in dB and the corresponding percentage of noise and distortion versus the RF input level into the receiver front end signal is shown.

Conclusion

A fully monolithic single chip GaAs MMIC amplifier and mixer was designed, fabricated and tested for potential application in a portable communication system. complete receiver system was built using the GaAs LNA and mixer IC cascaded with a narrowband FM double conversion receiver IC (MC3363DW) and an audio amplifier (MC34119D). This single chip integrated front-end IC (90 mil X 110 mil)

achieved -118.9 dBm sensitivity in the 900 MHz cellular band. The extremely low power dissipation, high level of integration and very good RF performance of this monolithic IC make it an ideal candidate for portable communication applications.

Acknowledgments

We are thankful to J. Escher, C. Monroe, C. Weitzel and R.Potyka for their strong support and encouragement of this work. We also thank J. Kline, R. Vaitkus, S. Dorn and D. Halchin for their characterization support. Help of C.E. Wu, K. Hilgers and N. Mellen is also appreciated.

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(2) Y. Imai, et al, " Very Low Current Small Size GaAs MMICS for L-band Front-end Applications," IEEE GaAs IC Symposium. Tech. Digest., 1989, pp. 71- 74.

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(5) V. Nair et. al., "Low Current GaAs Integrated Down Converter for Portable Communication Applications", IEEE GaAs IC Symposium. Tech. Digest., October 1993, pp. 41-44.

A New RF / Microwave Proximity Tag System

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ABSTRACT

Industrial, commercial and consumer applications requiring the ability to locate, identify, track, and sometimes pass data to objects have greatly expanded within the past few years. Example applications include automatic toll collection, vehicle identification, vehicle location, container/freight tracking, access control, and inventory control. Radiofrequency or microwave-based proximity tag systems are ideally suited to these types of applications. We have recently developed a new microwave tag technology that provides considerable benefits over existing systems. The basis of the system is a unique CMOS integrated circuit that was designed specifically for low-cost, high-performance tagging applications. The IC incorporates an rf/microwave detector, a modulator, a demodulator, microcomputer logic, and read/write data memory. The only external connections required are to an antenna and a battery. The battery is required only to preserve the stored data and to power the IC logic during an interrogation. Passive backscatter modulation techniques combined with on-chip power conservation logic results in a tag operating life that approaches the shelf life of the battery. The interrogator portion contains the transmitter, receiver, and logic sections. This paper describes the operating principles and unique features of this new tag system.

INTRODUCTION

Applications requiring the accurate and efficient location and identification of objects and personnel are now rapidly expanding. Major growth areas for these applications include personnel security and access control, container/freight tracking, and inventory control. In addition, Intelligent Vehicle Highway Systems (IVHS) and other vehicle control systems, that are now in the planning stages, will include vehicle location and identification, vehicle speed control and automatic toll collection.

For many applications, object identification can be sufficiently addressed using optical techniques such as bar code scanners or close-proximity magnetic stripe readers. Because these techniques require short-range and/or line-of-site operation, they are most useful for situations where the location of the object relative to the reader can be well-controlled and where the information carried by the object is permanently fixed.

There are many applications however where optical and short-range operation is not practical or desirable. In these cases the use of rf/microwave tags provides cost/performance benefits that cannot be met by other technologies.

The use of rf or microwave energy to provide communication between an interrogator and a tag offers several key advantages over other technologies. Microwaves are relatively unaffected

by rain, smoke, dust or other factors that would otherwise obscure optical-based systems. Nor are microwaves affected by ambient light, wind, atmospheric, temperature or thermal gradients.

With appropriate antenna designs, microwave energy can provide well-defined coverage patterns ranging from spherical to fan-shaped to narrow beams. Thus, depending on the applications, interrogators can be designed to sense tags over a broad area or within a narrow field-of-view.

Furthermore, information can be conveyed by microwave energy via a variety of techniques. These include narrowband or spread-spectrum operation, pulse-width, frequency, or amplitude modulation, and their combinations.

TYPES OF TAG SYSTEMS

RF tags vary in complexity from very inexpensive, short-range, passive devices having no stored information to long-range fully-active transponders with kilobytes of data storage. Tags can be classified according to their complexity as follows:

Passive

Passive tags are those that utilize no internal power source. Although most of the systems use frequencies below the microwave bands, there are many applications that are using microwave tagging. A common application is the inventory-control or anti-theft tags used in stores and libraries. These are uncoded tags containing a diode that re-radiates impinging microwave energy at the second harmonic. The detection of this signal by a receiver indicates the presence of the tag. Another passive approach employs tuned resonant circuits within the tag that perturb the transmitted microwave field. By using several tuned circuits and a swept frequency transmitter, it is possible to provide multiple tag codes; however, because of the lack of internal logic circuitry, coding capability is limited.

RF Driven

Active logic circuitry within the tag can be powered using energy derived from the incident microwave signal. A diode rectifier and storage capacitor are used to provide dc power for logic and timing circuitry that provide for more complex data communication schemes. The tag can respond using passive approaches as well as by using the stored energy to modulate information onto a reflected portion of the microwave signal. Timing circuitry can also be employed to add another degree of freedom in the information transmitted to or received from the tag. Most rf driven tags have relatively short operating range and are read-only, meaning their data is fixed either at the time of manufacture or via a one-time write operation. Some rf driven tags are capable of being re-programmed by the use of EEPROM technology.

Semi-Passive

Semi-passive tags require an internal power source to operate logic and coding circuitry but not to actively transmit rf energy. The tag still responds passively via harmonic, modulated/reflected, or time-delayed signals, but since the dc power is internally generated, the operating range can be greater than that of rf-driven tags Using low-power components, a tag can be powered for years from a miniature battery or even longer using rechargeable sources. The on-board power source permits more complex logic circuitry for implementing coding schemes and can also provide the means for electronic data retention. Such tags can be programmable, enabling the transmitter to not only read its data but also write data back to it without any specialized programming equipment and with no reduction in operating range. This capability can be very advantageous in secure applications since the tag's code does not have to be fixed.

Active

Active tags are those that use an internal power source both for operating internal circuit functions and for transmitting rf energy. Coding and information storage is the same as for semi-active tags however the use of powered transmitters and receivers can provide greatly increased operating range and very robust communication methods employing collision detection and error correction.

SARNOFF PROXIMITY TAG SYSTEM

Sarnoff has experience in a wide range of tag-based systems employing both identification and location capabilities. We have developed long and short-range tag systems for both military and commercial applications including vehicle identification, industrial control, and personnel access control. Our most recent development is a tag system designed for medium-range applications requiring read/write capability at a very low cost.

The basis of the system is a unique CMOS integrated circuit that was designed specifically for low-cost, high-performance tagging applications. The IC incorporates an rf/microwave detector, modulator, demodulator, microcomputer logic, and read/write data memory. The only external connections required are to an antenna and a battery. The battery is required only to preserve the stored data and to power the IC logic during an interrogation. Passive backscatter modulation techniques combined with on-chip power conservation logic result in a tag operating life that approaches the shelf life of the battery.

Important features of the system approach are:

- A semi-passive, inhibited tag using a custom-designed CMOS integrated circuit;
- A secure coding scheme whereby the tag never directly transmits its ID data;
- The ability to unambiguously identify multiple tags simultaneously;
- Read/write capability;
- Interrogator-to-tag communication via narrowband modulated rf;
- Inexpensive fundamental system components; and
- Long tag operating life.

The tag IC is a custom-designed, mixed-signal device with an instruction set and I/O functions specially designed for tagging applications. A block diagram of the IC is shown in Figure 1. Figure 2 shows a credit card-sized tag configuration suitable for personnel identification systems.

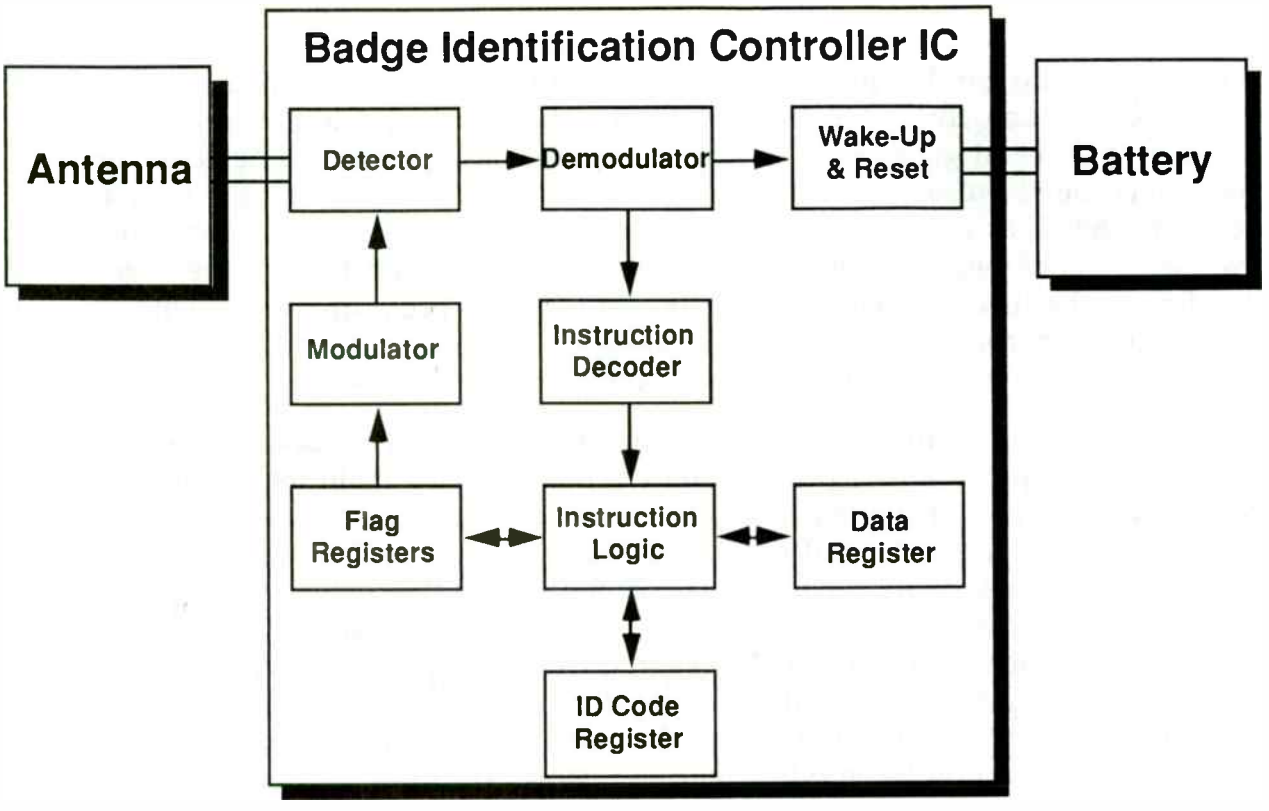

Figure 1. Block diagram of the tag IC.

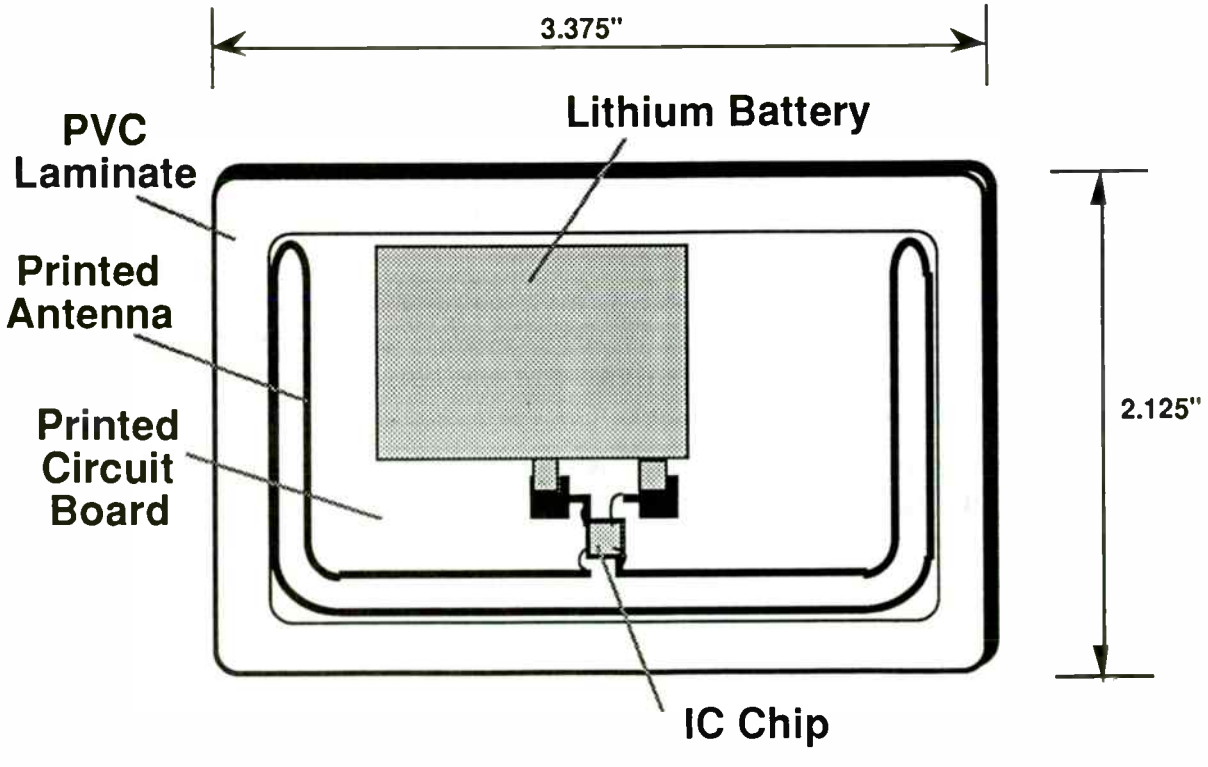

Figure 2. Personnel access control card.

The IC accepts and conditionally responds to commands and data via a single serial I/O pin. With a suitable antenna connected to the I/O pin, the IC is capable of directly detecting signal frequencies up to several gigahertz. For higher frequencies, an external detector can be added to envelope-detect the rf pulses. The incoming bit stream, transmitted by the interrogator unit, is interpreted by the IC as either control instructions, query instructions, or data. Instructions and data are used in conjunction with a search algorithm performed by the interrogator unit in an effort to identify the ID code register contents of a tag or to program the tag with new data. The current IC design incorporates 36 bits of data storage arranged as six individually addressable six-bit registers and provides for approximately 62 billion unique codes.

The IC is normally in a low-power standby mode requiring only about 0.5μA of current from a 3V battery. When a particular rf pulse pattern is detected, the main logic portions of the IC are activated. Determination of the tag ID code is then accomplished by a series of several hundred 'transactions' between the interrogator and tag. For all but a few of these transactions, the tag's presence is undetectable. Only for the relatively few query instructions which evoke a response does the IC turn on its modulator. The modulator produces sidebands on the rf energy reflected from the antenna, which are detectable by the interrogator's receiver. Ultimately, by this series of commands, questions and answers, the interrogator firmware can deduce the contents of the ID code registers within the tag IC. The IC can then be instructed to then turn off, or, ultimately the IC will revert to its standby mode when no more rf input is detected. In the current implementation, interrogation time is less than 15 milliseconds. A similar process is used to send data to the tag.

Interrogator/Programmer

The interrogator/programmer unit consists of a transmitter, receiver and logic/control circuits. The transmitter consists of an 915 MHz rf signal source, amplifier and switch. A block diagram of the interrogator is shown in Figure 3. The logic circuitry controls the rf switch timing to produce a pulse-width modulated output signal. Received signals are homodyned and filtered to checked for the presence of the modulation sideband signal during a specific time window. By sending a sequence of instructions and interpreting the responses, the interrogator logic can determine the information stored in the tag. In addition, special instruction sequences can be transmitted to send new data to the tag.

The operating range of the system depends on a number of design considerations for both the interrogator and tag. These include transmitter power, interrogator and tag antenna gains, receiver sensitivity, and tag detector sensitivity. In the current configuration, with 18 dBm into the transmit antenna, a credit-card sized tag can be read reliably at 3 feet.

The interrogator communicates with a host system via an RS-232 interface. In addition, it provides both Weigand and mag-stripe outputs.

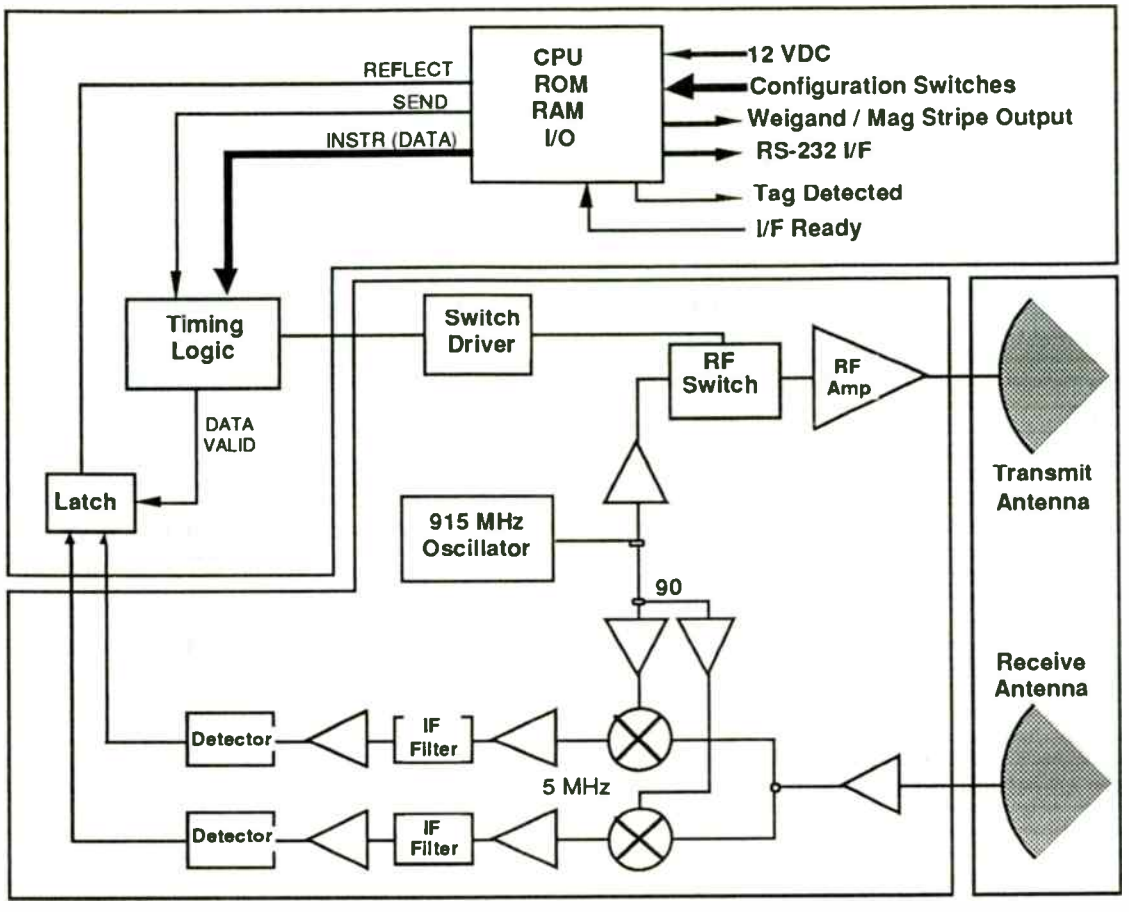

Figure 3. Interrogator/programmer unit.

CONCLUSION

A new rf/microwave tag system has been developed using a unique coding and identification strategy. The system provides billions of possible code combinations and read/write capability. All tag functions are accomplished by a single CMOS IC providing signal detection, modulation and logic functions via a single I/O connection.

There are many applications that can take advantage the low-cost read/write capabilities of this system. For example, automated revenue collection systems (vehicle tolls, mass transit fares, etc.) can utilize the tag as a debit card, thus eliminating the need for a centralized billing system. In manufacturing environments, the tag could be used to accumulate test status data as an item is being assembled. For inventory control, tags could be used to identify an item or container and to store the number of items within the container. Other applications requiring the ability to sense multiple tags simultaneously include location-finding, sorting, and scanning.

Both the tag and interrogator portions of the system can be tailored to a variety of applications, such as personnel identification, vehicle identification, inventory control, and manufacturing control, by appropriate design of operating frequency, operational range, and tag and interrogator geometry. Additional capabilities that could be incorporated into the system include increased data storage capacity, long-range operation, external sensing and interface functions.

A 1.9GHz Chipset for Personal Communicators

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PCS Defined

In his paper of 1987, Don Cox presented a vision of universal portable communications which would evolve from cordless telephone, cellular radiotelephone and paging services.[1] The mobility of our society has made all of these portable communications services very popular. But none provide the quality and low cost of wireline service. The next generation cordless service, as described by Cox, has evolved into the cornerstone of what we are now calling Personal Communications Services, PCS. The service will provide not only mobility and portability, but the quality, cost, reliability, and privacy of wireline services. The services are appearing under many names, CT2, Digital European Cordless Telephone (DECT), Japan Personal Handy Phone (PHP), to name a few, but all have the same goal of reproducing the desirable qualities of wireline services in wireless form.

This paper addresses the requirements for the RF portion of a wireless personal communicator and presents progress on a family of RF integrated circuits for 1.9GHz applications.

PCS Systems Requirements

In reviewing the service requirements of PCS, system requirements and their impact on the personal communicator, or wireless handset portion of the system are revealed.

PCS could be implemented by simply issuing a universal telephone number to each subscriber which could be assigned to the equipment most convenient to the user at any given time. But the popularity of wireless handsets, as demonstrated by the meteoric rise in cellular subscribers after the introduction of handheld units, makes a wireless communicator almost inseparable from any realistic implementation of PCS.

To qualify as a viable portable communicator, the unit must be of size and weight consistent with current pocket sized cellular phones or cordless telephones. To achieve this small size, a high level of integration must be achieved. Batteries are a major contributor to size and weight so the circuitry must operate at low voltage to minimize the number of batteries required. Portability is of little value if actual use is limited to an hour or so. Therefore, long talk time is essential to public acceptance of wireless PCS. Circuit efficiency must be high and a "sleep" mode must be available to minimize current drain thus optimizing talk time for a given battery charge.

Cellular currently provides the mobility required for PCS but reduced voice quality and high connect charges limit it's ability to meet the full definition of PCS. The narrow-band FM modulation used in analog cellular does not allow the bandwidth required for high quality digital speech and data transmission. Nor does it allow for the increased channel

capacity required to bring the cost of use down. These issues are being addressed through the use of sophisticated signal processing and complex digital modulation schemes which, until recently, have been used primarily in military and satellite communications. These schemes, such as differential quadrature phase shift keying (DQPSK) and Gaussian minimum shift keying (GMSK), maximize the information density in a given channel bandwidth. In addition to spectrally efficient modulation, channel utilization is maximized by time sharing of channels between users in a scheme call time domain duplexing (TDD). The available channels are multiplex among users at a rate which is transparent to the user. Another candidate for maximizing the number of users per channel is spread spectrum signal processing. With this scheme, many users can simultaneously use the same channel because their signal are "coded" either through mixing with a digital code which spreads the signal over a much larger bandwidth or through a pattern of frequency hopping with time. Obviously these schemes require complex digital signal processing and computational power to keep track of who is occupying which time slot, who is on which frequency, or who has which code. The effect of all this on the RF portion of the communicator is that the circuitry must not distort the carefully filtered signal or spectral regrowth and adjacent channel interference will occur, defeating the purpose of these complex schemes. The linearity required depends on the modulation used with GMSK being less sensitive than DQPSK due to a lower peak to average power ratio.

PCS RF COMPONENT REQUIREMENTS

Customer expectations		Solutions
End user	Designer	
Small size and weight	High level of integration	RFICs
	Chip compatibility	Partitioned for ease of integration
	Low voltage	3V or less designs
Long talk time	High device efficiency	High efficiency functions
	Long battery life	Standby mode
Low Cost	Low cost but easy to use	Lowest cost technology
	Flexibility across platforms	Meet several platform requirements
		On-chip system functions
Landline quality	Functions which meet system requirements	Functions which meet system requirements

Figure 1

Another aspect of cost is the cost of the subscriber equipment. The communicator cost must be similar to that of current high-end cordless telephones. To achieve these cost targets while providing the quality and portability, the level of circuit integration and ease of interface of components must be balanced against cost of these components. While a "single chip radio" would be desirable from a communicator manufacturing standpoint, RFIC manufacturing and packaging capability is not mature enough to deliver all the functions in one package at reasonable cost.

In summary, from an RF circuit standpoint, these requirements translate into the need for low cost, easy to use, highly integrated building blocks which operate at low voltages and high efficiency which provide standby modes and support the complex modulation schemes being implemented in the new PCS systems. These points are summarized in figure 1.

PARAMETER	DECT	PHP
R Frequency	1889-1898MHz	1895-1907MHz
Number of Channels	10	52
Channel Spacing	1.728MHz	300KHz
Peak Output Power	250mW	80mW
Data Rate (per channel)	1.152Mb/s	384kb/s
Modulation	GMSK	$\pi/4$ DQPSK
Baseband Filtering	B_bT=0.5(Gaussian)	α=0.5 (Root Nyquist)
Access	TDMA/TDD	TDMA/TDD
Threshold Sensitivity	-83dBm @ 0.1%BER	-97dBm @ 1%BER
IF Frequency (Typical)	110.592MHz	240.05MHz

Table 1. DECT and PHP Selected Technical specifications

DECT and PHP System Specifications

While cellular equipment and service providers work to improve the current 900MHz cellular service, by international agreement new services are being planned at frequencies near 2GHz. DECT and JPHP are two PCS contenders planned for this new band. The technical requirements for these two systems are shown in Table I.

Figure 2 shows a block diagram of the RF portion a typical DECT or PHP handset. In receive mode, the signals from the antenna are pre-select filtered and directed by the antenna switch to the low noise amplifier. The unwanted image frequencies are filtered before the signal is mixed down to the first intermediate, or IF, frequency. Further downconversion, filtering and processing is used to reduce the signal now at the IF frequency to speech or data. The IF portion of the communicator, as well as the baseband processing circuitry, are available in IC form from Motorola and other vendors and will not be presented here. On the transmit side, the IF signal with modulation from the baseband processor and IF portions of the communicator is mixed up in frequency and the unwanted sidebands are filtered. Alternatively, the modulation can be applied to the local oscillator, in which case the IF will be unmodulated. Several

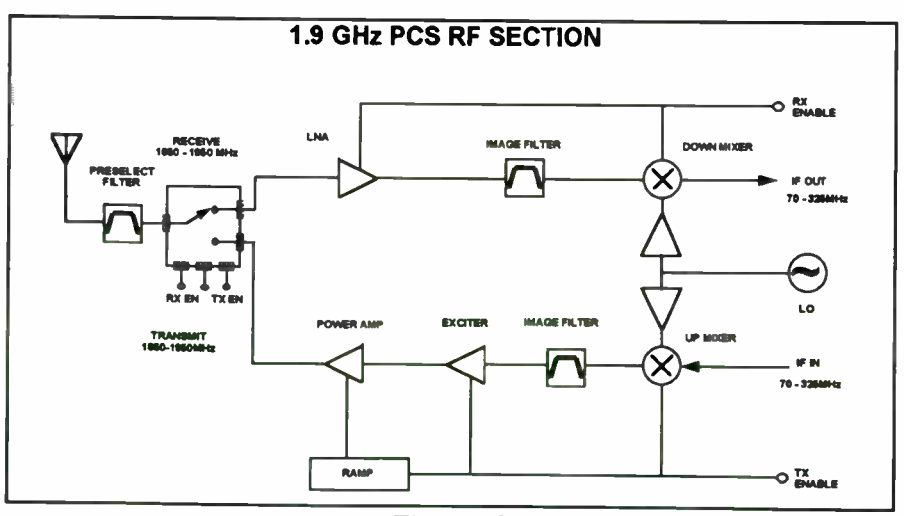


Figure 2

stages of amplification bring the signal to the desired signal level before it is directed to the preselect filter and antenna by the antenna switch. Ramping, or shaping of the transmit signal is required to limit splatter into other adjacent channels.

Tradeoffs for Integration

Level of integration, performance and cost can often be mutually exclusive. All three are required simultaneously in PCS applications. Partitioning of the radio into RFICs and the semiconductor and packaging technology are critical. Silicon bipolar IC technologies have increased in frequency capability making them useful for RF applications. They are also very cost effective. Advanced BiCMOS technologies offer higher performance and offer greater design flexibility with MOS and BJT circuitry. With the increase in flexibility comes greater wafer manufacturing cost. GaAs offers the highest performance but material cost make the cost per wafer high. Interestingly enough, GaAs processing cost can be lower than BiCMOS due to fewer mask layers. In packaging, RFIC production volumes do not yet allow for specialized packaging beyond developing special leadframes for standard package outlines. This limits the partitioning decisions mainly due to limitations in available pinouts if assembly cost are to remain low.

Motorola's 1.9GHz RFIC Chipset

Motorola's RFIC Operation, part of the Communications Semiconductor Products Division, is developing a chipset targeted for DECT and PHP. Portions of the chipset are applicable to DCS1800 (PCN) which is being implemented in the UK, and to the US PCS when it is defined. Figure 3 shows the partitioning of the 1.9GHz radio using the MRFIC1800 series. This partitioning was driven by trading off the architecture requirements shown in figure 2 and packaging constraints. Four chips are offered; an antenna transmit/receive switch, an LNA/downconverter, an upconverter and a power amplifier. The switch, LNA/downconverter and upconverter are packaged in SOIC packages allowing manufacture in Motorola's high-volume IC packaging factories. The initial work on the power amplifier has been done in a single-layer ceramic package but a two-chip plastic version is planned for final release. The block diagram (figure 3) includes Motorola's MC33128 power management chip which supplies not only a regulated 3 Volts output for the supply voltage (Vdd) for the IC's, but also -2.5 Volts for the gate bias of the depletion mode

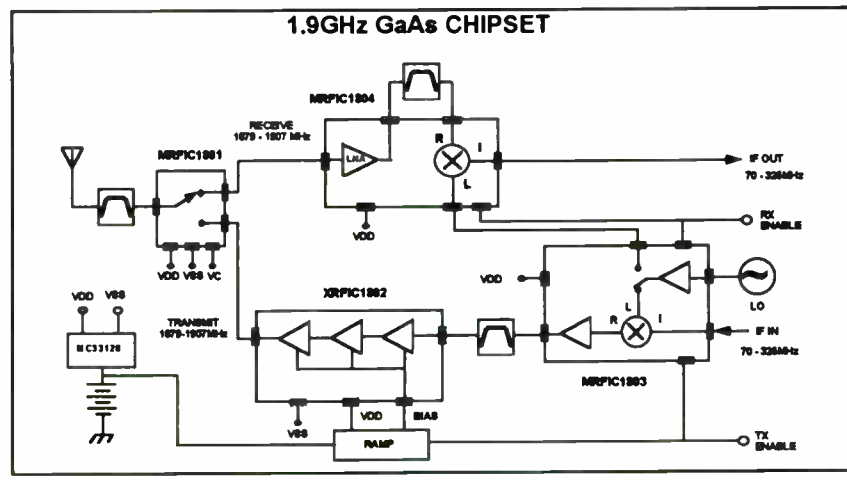


Figure 3

devices (Vss) of the switch and power amplifier.

The chipset has been implemented in GaAs to meet the performance demands of portable 3 Volt operation at 2GHz. To offset the potentially higher cost of GaAs, Motorola's proprietary MAFET planar GaAs MESFET IC process has been used.[2] This planar process yields 0.8 micro gate lengths while not requiring the highly variable etching used in the more common recessed gate GaAs MESFET process. Neither ground vias nor air bridges are employed to reduce processing complexity. The mobility advantages of GaAs can therefore be had for a wafer cost similar to advanced BiCMOS. Figure 4 shows a cross section of the MAFET vertical process.

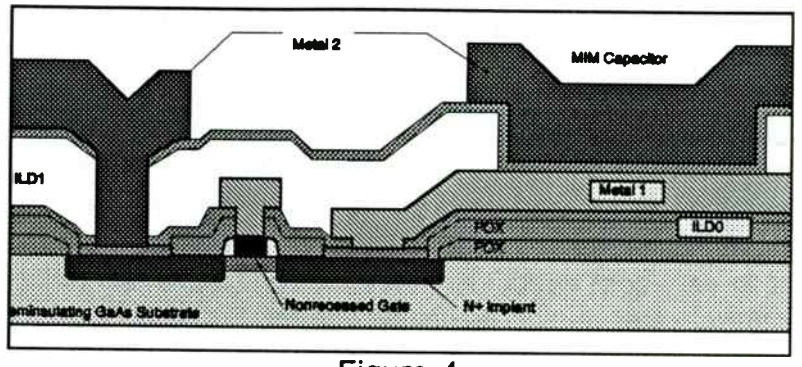
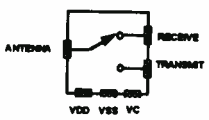


Figure 4

Antenna Transmit/Receive Switch

The antenna switch is a reflective, four MESFET design which incorporates power FETs in the transmit path allowing it to handle up to 1 Watt. Key performance specifications are shown in figure 5. On-chip interface circuitry allows for easy interface through one pin to CMOS compatible control signals. The power consumption is much less than can be had for an equivalent PIN diode switch. Chip layout has been arranged to optimize the isolation between the transmit and receive port during in the transmit mode. An industry standard SO-8 8 lead plastic package is used. As can be seen in figure 6, insertion loss versus frequency, the antenna switch is usable over more than just the 1.9GHz PCS band. Typical insertion loss as a function of input power is shown in figure 7.



MRFIC1801
TRANSMIT/RECEIVE SWITCH
(DECT/PHP)

PARAMETER	TYPICAL PERFORMANCE MIN	TYP	MAX	UNITS
RF FREQUENCY	800		2500	MHz
1 dB COMPRESSION (input)	28	30		dBm
Tx INS. PATH LOSS (@ Pin = +28 dBm)		0.75	1.0	dB
THIRD ORDER INTERCEPT (output)	39	45		dBm
ISOLATION (TX TO RX)	20	22		dB
CONTROL VOLTAGES				
TX ENABLE		3.0		V
RX ENABLE		-2.5		V
SUPPLY VOLTAGE: Vdd	2.7	3.0	5.5	V
Vdd-Vss			5.5	V
SUPPLY CURRENT (Idd, Iss)		0.28	0.35	mA
TEMPERATURE	-30		+85	°C

Figure 5

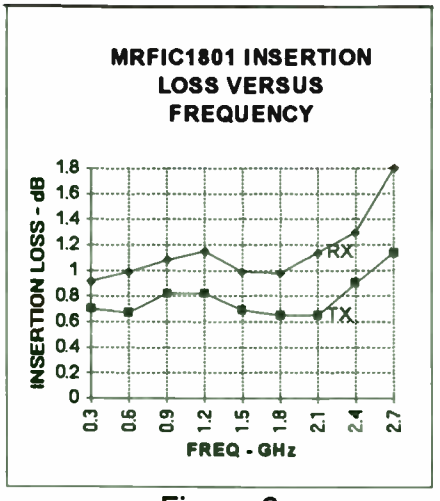


Figure 6

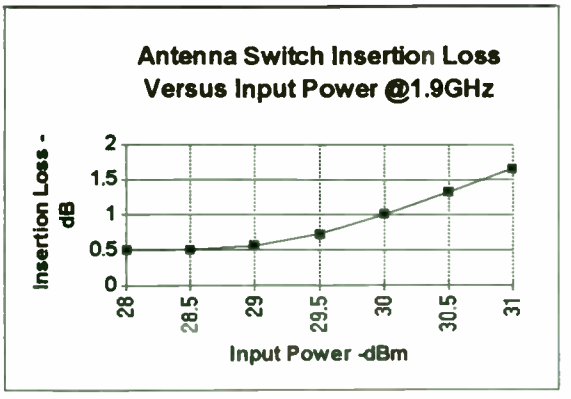
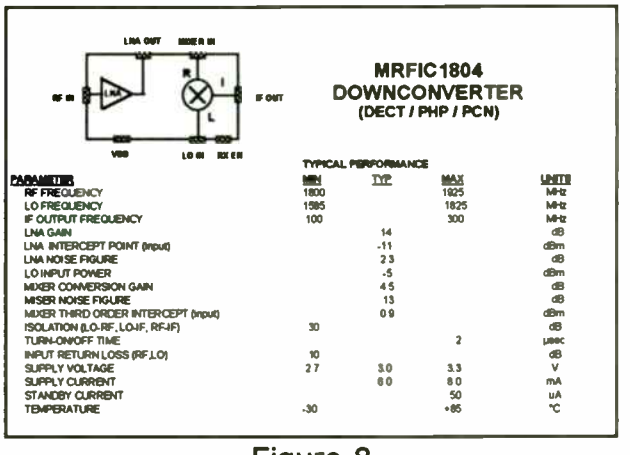


Figure 7

composed of a two-stage MESFET low noise amplifier and a single-ended active MESFET downmixer in one package. The key performance specifications are shown in figure 8. The LNA output and mixer input are available for image filtering off chip. The MESFETs are enhancement mode or self-baised depletion mode so only a positive supply is required. The RF circuits are activated by applying a CMOS high signal to the receive enable pin and otherwise is in standby mode drawing less than 50uA. The design was optimized for efficiency somewhat at the expense of noise figure and so draws less current than

LNA Downmixer

The MRFIC1804 downconverter is



MRFIC1804
DOWNCONVERTER
(DECT / PHP / PCN)

PARAMETER	TYPICAL PERFORMANCE MIN	TYP	MAX	UNITS
RF FREQUENCY	1800		1925	MHz
LO FREQUENCY	1585		1825	MHz
IF OUTPUT FREQUENCY	100		300	MHz
LNA GAIN		14		dB
LNA INTERCEPT POINT (Input)		-11		dBm
LNA NOISE FIGURE		2.3		dB
LO INPUT POWER		-5		dBm
MIXER CONVERSION GAIN		4.5		dB
MISER NOISE FIGURE		13		dB
MIXER THIRD ORDER INTERCEPT (Input)		0.9		dBm
ISOLATION (LO-RF, LO-IF, RF-IF)	30			dB
TURN-ON/OFF TIME			2	μsec
INPUT RETURN LOSS (RF,LO)	10			dB
SUPPLY VOLTAGE	2.7	3.0	3.3	V
SUPPLY CURRENT		8.0	8.0	mA
STANDBY CURRENT			50	uA
TEMPERATURE	-30		+85	°C

Figure 8

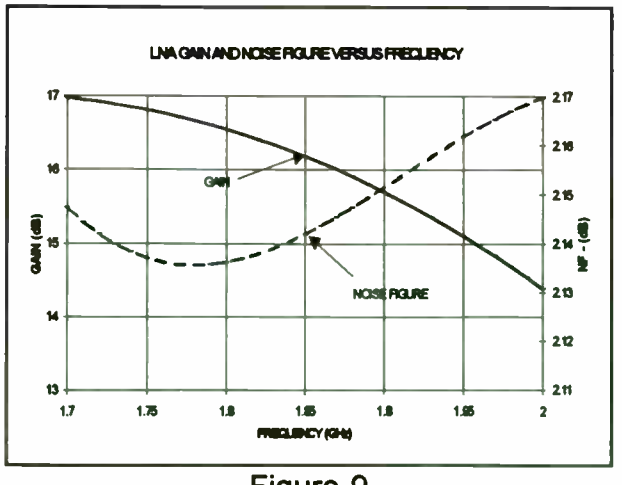


Figure 9

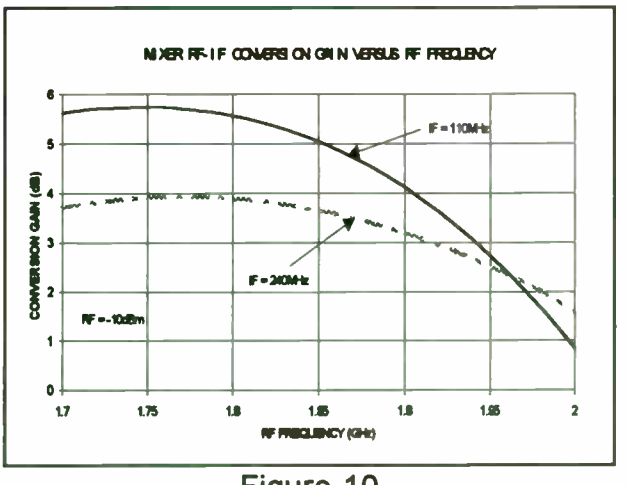
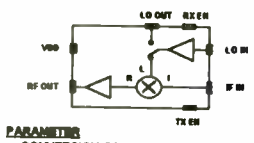


Figure 10

typical commercially available downconverters. The device is packaged in an industry standard O-16 miniature 16 lead package. A slight amount of off-chip inductance, 0.3nH, at the input and output optimizes the LNA noise performance which is still better than that of a comparable bipolar downconverter while drawing less current. This inductance is easily implemented on the PC board. Matching for the selected IF frequency is implemented off-chip as part of the power supply decoupling. LNA gain and noise figure versus frequency are shown in figure 9 and mixer gain versus frequency is shown in figure 10.

Upconverter



MRFIC1803
BALANCED UPCONVERTER
(DECT / PHP / PCN)

TYPICAL PERFORMANCE

PARAMETER	MIN	TYP	MAX	UNITS
CONVERSION GAIN		10		dB
IF INPUT FREQUENCY	70		325	MHz
LO INPUT FREQUENCY	1500		1900	MHz
RF OUTPUT FREQUENCY	1700		1900	MHz
RETURN LOSS (ALL PORTS)	10			dB
LO INPUT POWER		-10		dBm
IF INPUT POWER		-15	-7	dBm
1dB COMPRESSION (output)		-2		dBm
THIRD ORDER INTERCEPT (output)		9		dBm
LO-RF FEEDTHROUGH		-10		dBm
SUPPLY VOLTAGE	2.7	3.0	3.3	V
TX SUPPLY CURRENT		28	40	mA
RX SUPPLY CURRENT		3.0		mA
STANDBY CURRENT		10	500	uA
TEMPERATURE	-30		+85	°C

Figure 11

The upconverter, MRFIC1803, employs a balanced active mixer, a local oscillator buffer with diversity switch, and a exciter amplifier in one SO-16 package. Key performance parameters are shown in figure 11. No off-chip matching is required over the range of LO and IF frequencies. To allow use of a 16 lead package, image/LO filtering is performed at the exciter output and the exciter amplifier was sized to accommodate the image power. The upconverter circuitry is activated by a CMOS high signal being applied to the transmit enable pin. When the receive enable pin is brought high, the LO diversity switch directs the buffered LO to the LO output pin at the correct level to drive the MRFIC1804 downconverter. With both enable pins low, the IC is in standby and draws less than 50uA. As with the downconverter, all the MESFETs are enhancement mode devices or self-baised requiring only a positive supply. Conversion gain versus frequency is shown in 12.

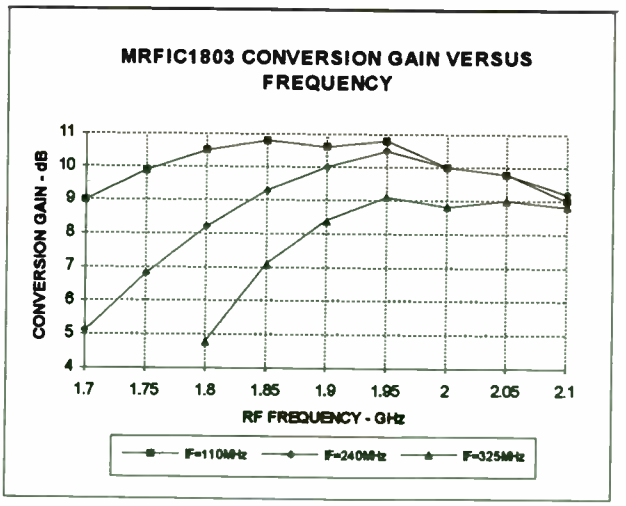
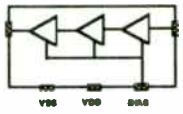


Figure 12

Power Amplifier

The power amplifier has presented the greatest challenge in the development of the chipset. The initial work was done in a single-layer ceramic package with a ceramic lid. The design employs three MESFET amplifiers, two in class A bias and the third, the



XRFIC1802
POWER AMPLIFIER
(DECT/PHP)

PARAMETER	TYPICAL PERFORMANCE MIN	TYP	MAX	UNITS
RF FREQUENCY	1850		1950	MHz
1 dB COMPRESSION (output)		27		dBm
HARMONICS		-40	-20	dBc
THIRD ORDER INTERCEPT (output)		36		dBm
RETURN LOSS (input)		12		dB
REVERSE ISOLATION (on or off)		36		dB
SMALL SIGNAL GAIN	30	32		dB
STABILITY (no oscillation)	3:1			VSWR
SUPPLY VOLTAGE: Vdd	2.7	3.0	3.5	V
Vss	-2.75	-2.5	-2.25	V
Idd @ Pout=+27dBm, Vdd= 3.0V			430	mA (DECT)
Idd @ Pout=+22dBm, Vdd=3.0V			300	mA (PHP)
Iss		0.2		mA
TEMPERATURE	-30		+85	°C

Figure 12

output, in class B. This configuration optimizes power added efficiency while maintaining the linearity required for digital modulated RF signals. The drain voltages for the two input stages are supplied from one drain voltage pin while the output device has its own drain supply. Gate biasing of the depletion mode devices is accomplished through control voltage pins, again one for the input stages and one for the output, which can be ganged together for convenience. By applying a positive voltage near 1V to these pins, the quiescent drain current is set. The quiescent point of the input and output stages can be set for the best linearity/efficiency tradeoff for the application. Key performance goals for the power amplifier are shown in figure 12. Gain, 1dB compression and efficiency versus frequency are shown in figure 13.

The design has worked acceptably with the exception of stability. Unlike other microwave power amplifier applications, one designed for portable equipment must have high tolerance to output mismatch. This design has demonstrated stability up to about 4:1VSWR. 10:1 or better is desirable in portable applications due to the uncertain environment at the antenna and the 2.5dB or less "isolation" afforded by the transmit/receive switch and the preselect filter losses. Isolators common in other microwave equipment will prove too costly to include in portable communicator designs. Slight tuning on the output of the device reduced the gain to around 32dB at 1.85GHz while improving the efficiency to the mid 30's. Since the final version is to be packaged in plastic like the other chips in the chipset, and the stability is marginal in a ceramic package where isolation is optimum, it was decided to split the PA into two parts. Details of this final version will be presented at a later date.

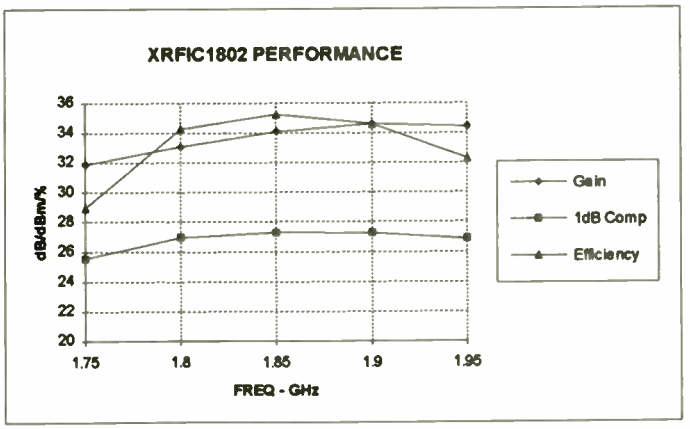
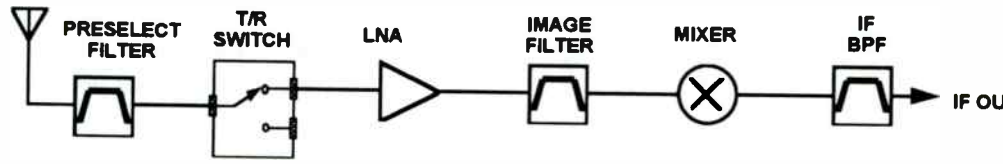


Figure 13

RECEIVER SENSITIVITY ANALYSIS

MRFIC1800 series is designed to give adequate performance in DECT and PHP

1.9GHz WORST-CASE RECEIVER ANALYSIS



DECT							
Min Gain (dB)	-2.0	-1.0	+14	-2.0	+4.0	-7.0	
Max NF (dB)	2.0	1.0	2.5	2.0	13.5	7.0	
Max BW (MHz)	200			200		0.576	
Signal Level (dBm)	-83.0	-85.0	-86.0	-72.0	-74.0	-70.0	-77.0
Eb/No (dB)							25.4
PHP							
Min Gain (dB)	-2.0	-1.0	+14	-2.0	+4.0	-7.0	
Max NF (dB)	2.0	1.0	2.5	2.0	13.5	7.0	
Max BW (MHz)	200			200		0.096	
Signal Level (dBm)	-97.0	-99.0	-100.0	-86.0	-88.0	-84.0	-91.0
Eb/No (dB)							16.0

Figure 14

applications. A number of variables enter into the actual performance. Figure 14 shows a worst-case analysis using available filters. The preselect and image filters are 2-pole ceramic surface mount. The IF bandpass filter is a surface mount SAW. Trade-offs are available in bandwidth, pass band insertion loss and out-of-band rejection. The worst case gain and noise figure for the components was used. For simplicity, the IF filter bandwidth was set at the data bandwidth. The bit energy to noise power ratio, Eb/No can be defined as:[3]

$$\frac{E_b}{N_0} = \frac{CT_b}{\frac{N_p}{B}} \qquad (1)$$

where C = Signal Power
T_b = Bit duration
N_p = Noise power
B = Data Bandwidth

and

$$NoisePower = kT_0F_n \quad (2)$$

where k = Boltzman's Constant, 1.38054 x 10^{-23} K/J
T_0 = Temperature in degrees Kelvin
F_n = Noise Factor

E_b/N_0 can be related to bit error rate for a given detector and modulation. The IF portion of the radio has not been analyzed, but with reasonable noise figure IF's of, say, 10 or better, the IF will not contribute significantly to the reduction of E_b/N_0 set by the frontend but simply amplify the signal level. Practical detectors for GMSK require 10-12dB E_b/N_0 to achieve the required 0.1% bit error rate while DQPSK detectors require 8-10dB to achieve 1%. As can be seen in figure 14, the downconverter sets acceptable noise figure, and therefore Eb/No for both DECT and PHP. Note that for both PHP and DECT the data bandwidth is significantly less than the data rate shown in table 1. This is due to the coding gain of the modulation schemes used and demonstrates the spectral advantage of digital modulation.

Transmitter output power analysis

Referring to table 1, the output power requirement for DECT is 250mW or 24dBm. With 2.5-3.0dB loss due to the preselect filter and the antenna switch, the power amplifier must supply 26.5-27dBm. A power amplifier operated at 1dB compression is acceptable to meet the linearity requirements for GMSK. As can be seen in figure 13, this requirement is met by the XRFIC1802. To meet the linearity requirement for $\pi/4$ DQPSK as used in PHP, the power amplifier must be "backed off" another 3dB from 1dB compression. For 80mW peak output and the same 2.5-3.0dB loss, the power amplifier must supply 21.5-22.0dBm at 3dB backoff. Again the design meets the requirements.

Summary

Four GaAs RFIC designs for the first-phase hardware for the DECT and PHP systems have been presented. The chips were designed to meet the system requirements, both cost and performance, for the new candidates for Personal Communications Services in Europe and Japan. Three of the parts, the antenna switch, downconverter, and upconverter, are scheduled for volume production in the first quarter of 1994. The fourth, the power amplifier, is a stepping stone to a final two-chip PA/switch combination which should be sampled by mid-1994.

1. Donald C. Cox, "Universal Digital Portable Radio Communications," *Proceedings of the IEEE*, vol. 75, no. 4, April 1987.

2. P. O'Neil et al, "GaAs Integrated Circuit Fabrication at Motorola", IEEE 1993 GaAs IC Symposium.

3. L. W. Couch II, *Digital and Analog Communications Systems*, New York: Macmillon Publishing Company, 1990.

A CALTRANS COMPLIANT AVI SYSTEM

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This presentation will describe the MFS/TI AVI system that will be used in California on SR91 and the toll bridges. The presentation will include a discussion of (1) the RF link, (2) the data protocol, and (3) lane discrimination. Included in the RF link discussion will be comments about backscatter and the radar cross section. Included in the data protocol discussion will be a listing of the various poll messages, the response messages, and the acknowledge messages. The lane discrimination discussion will show the need for this feature and our approach.

WLAN and Digital Wireless Applications

Session Chairperson: Ganesh R. Basawapatna,
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MICROWAVE COMPONENT REQUIREMENTS FOR PERSONAL COMMUNICATIONS AND WIRELESS LAN APPLICATIONS

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The increasing popularity of Wireless Communications has had a significant impact on the Microwave Technologies used in these applications. There are a number of aspects to this

1. Data transfer rates within computers are continually increasing, and already much of the high speed data transfer is occurring at R.F. rates within personal computers. Clock rates of 100 MHz are here, and it is only a matter of time before this will even get doubled.

2. In large data networks, the significant limitation on the system performance is data throughput or speed. Thus outside the computer also, in network elements such as buffers, switches, cables and modems, higher data rates are paramount.

3. At the same time, due to the increased interest in wireless communications and the continuously decreasing size of personal computation equipment, there has been a need to integrate the wireless transmit and receive circuits into smaller and smaller sizes. A lot of the circuits being developed address applications either in PCMCIA format or in hand held computation and telephony.

4. Coupled with all this has been the need to move applications to higher and higher frequencies as the spectrum in the 800 - 1000 MHz and 2 - 3 GHz ranges get more and more saturated.

There are two sets of solutions to this dilemma, both of which are being pursued rather vigorously in the market. The first is to integrate functions to the maximum possible in single chip format, which we call Higher Level Integration. The other is to use Multi-Chip-Module approaches to use available commercial components and achieve a system at the lowest cost and the fastest time to market. In this paper we compare the two approaches and point out the relationship to development time, development cost, and time to market. We use a term, Market Penetration Index, defined as the ratio of Product Life to Time to Market to compare the efficiencies in both approaches.

The AC Powerline as a Wireless Medium

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Abstract

The AC powerline has long been recognized as a wireless medium potentially offering communications connectivity within a building, but in the past its use has been precluded by the seemingly insurmountable difficulties of receiving data corrupted by powerline noise and attenuation. By understanding these obstacles, reliable powerline communications becomes possible, providing simple, low-cost, easily-installable connections to an existing medium already used for AC power.

As demonstrated in a number of commercial and industrial applications, reliable powerline communications is ensured through a hierarchical approach, building upon a spread spectrum physical layer enabling short-duration powerline transmissions and adaptation to changing powerline conditions, and upon a packet structure designed for error correction. A robust token passing protocol supports network access and device response under worst-case powerline impairments.

In-Building Wireless Communications

Control and monitoring systems require communications among a multitude of networked devices, distributed throughout a building and dependent upon shared information for proper operation. Examples of control and monitoring applications include energy management, material handling, building automation, point-of-sale transaction processing, automated meter reading, lighting controls, and security and access control.

The common key requirement of these systems is the need for data communications connectivity within buildings, requiring the frequent transfer of short messages at data rates between 10 and 100 kilobits per second (kbps), rather than the transfer of large files at megabit per second data rates.

The installation of networked systems has been hindered by the costs, delays, inconvenience, and complexities of installing communications wiring and cabling, particularly in existing buildings. These installation problems include scheduling delays, dislocations during installation, asbestos regulations, preserving building appearances, and the logistics of allocating installation personnel. Installing communications wiring can account for up to 60% of the total cost of installing a network. Furthermore, with installed cabling, the network is neither flexible, reconfigurable, nor easily expandable.

Wireless communications, including both radio-frequency (RF) and powerline communications, is an alternative. In building-wide wireless communications where the communications environment suffers from interference and signal attenuation, even if a system is successfully installed, the changing characteristics of these

impairments can render the system inoperative. The baffled user knows only one fact: the system does not work. Clearly the underlying technology must be robust and reliable enough to handle its intended environment.

In an indoor environment, outside of a localized area or within areas subject to interference, RF communications can be subject to impairments that limit range and achievable error rates. An alternative existing medium which is present in all buildings is the AC electrical wiring. Clearly, given a technology for reliable network communications over powerlines, one would have a solution for such environments offering universal access and minimal installation time and cost. The AC powerline has long been recognized as a possible wireless alternative, but in the past its use has been precluded by the seemingly insurmountable difficulties of receiving data corrupted by powerline noise and attenuation. By understanding these obstacles, new approaches make reliable powerline communications possible, providing simple, low-cost, easily-installable connections to a medium already used for AC power.

Approaches to Powerline Communications

Powerline carrier (PLC) communications has been used for very low data-rate communications (300 bits per second or less) for several years, primarily for energy management systems. Coupling to the powerline is accomplished with isolation circuitry, which couples only the low-voltage high-frequency data to the powerline, while providing isolation from the high-voltage 50 or 60 Hz AC and powerline spikes and surges.

PLC modems using traditional techniques modulate a carrier between 50 and 500 kHz using frequency shift keying (FSK) or amplitude shift keying (ASK). However, there is no guarantee, because of the frequency-dependent attenuation and impulsive noise, that a particular carrier frequency will work at any particular site or even provide communications among all outlets at a site. Experience has shown that these narrowband PLC modems can work up to a raw data rate of a few kilobits per second in some installations; however, there is no guarantee that electrical components newly plugged in, or unplugged and moved--anything from a PC to a battery charger--will not change the powerline characteristics and require manually changing the carrier frequency or even render the device inoperable.

Central to the powerline technology described in this paper is the design of each component of the technology specifically for the powerline environment, as opposed to modifying conventional technology. Rather than using traditional communications techniques and solidifying a design by adjusting component values to cover as many sites as possible, as is usually done, powerline characteristics should first be analyzed for a wide selection of sites, to arrive at a worst-case model. Then, using such a noise and signal-attenuation model, a hierarchical approach optimized for powerline communications at each level can be developed.

Because the powerline is an extremely hostile environment for data communications, a low-level link protocol must be designed to make the powerline as reliable as dedicated wire. Such a low-level link protocol must be built on the foundation of a powerline-optimized physical layer.

There has been little recorded development of data link protocols or network architectures specific to the powerline; rather, the little focus there has been on powerline communications has been devoted to different modulation techniques. In

fact, however, the powerline imposes requirements on a data link protocol which in turn lead to requirements upon the physical layer.

A network providing reliable powerline communications should therefore offer a data-link layer interface, building on the powerline-optimized physical layer and powerline-optimized media access sublayer (Figure 1). This approach allows the application to treat the powerline the same as any other medium. The technical issues of powerline communications are transparent to the user's application.

A Powerline Physical Layer

While in general spread spectrum exhibits improved noise immunity over narrowband approaches on the powerline, the difficulty of signal synchronization on the powerline in the presence of noise and frequency-dependent attenuation leaves traditional spread spectrum systems (direct sequence, frequency hopping, and chirp) providing an ineffective physical layer foundation and a 9.6 kbps raw data rate. Quoting from R.C. Dixon in *Spread Spectrum Systems* [1, p. 214], "More time, effort, and money has been spent developing and improving synchronizing techniques than in any other area of spread spectrum systems."

Our approach is based on a physical layer spread spectrum technology that provides for rapid synchronization. Rapid synchronization is achieved in an adaptive detection process that initially allows for a detection followed by the elimination of the possibility of false detection. Additionally, the physical layer delivers a raw data rate sufficiently high to implement protocol messages in single frames. Finally, the physical layer provides a foundation for rapid equalization.

A Robust Data Link Layer Protocol

Several key features of a data link layer are required for reliable operation of large, multi-node networks on the powerline:

- decomposition of larger packets to shorter powerline frames to create reliable communications
- rigorous error correction and detection
- effective adaptive equalization
- reliable transfer of control

Only a certain amount of contiguous information can be sent before it is almost a certainty that a transmission will be corrupted. This suggests a requirement for transmissions of short frames on the powerline. To further ensure the integrity of any frame of data, it is necessary to use both error correcting and detecting codes--forward error correction to minimize the number of retransmissions, and error detection to know if there is a need for a retransmission on a frame basis. Each frame should be acknowledged by the receiver before the transmission proceeds to the next frame. To implement this low-level link protocol, the higher level packet is broken up into such short frames.

Another benefit of the low-level link protocol is the effectiveness of adaptive equalization. Powerline conditions can change on the order of a few milliseconds, and the receiver must also be able to adapt to these changing conditions. Using a

low-level link protocol built upon short frames, the receiver can adapt on a frame basis, and, because acknowledgments are required, no information is lost.

Using forward error correction (FEC) and automatic repeat request (ARQ) developed specifically for the powerline environment, current products transfer data with an effective throughput of 19.2 kbps at an error rate of 10^{-9}, using a raw data rate of 135 kbps. This provides both the required reliability and bandwidth.

To provide reliable multi-access network communications, we have developed a noise-immune token passing protocol. For example, transfer of the token between nodes is done via a three-way handshake ensuring a transfer of control with effectively zero probability of a lost token. A comparison of channel access methods for the powerline has been described in [2].

Implementation

With the above approach, a reliable powerline LAN is achieved. An implementation of this powerline network architecture in a two-IC chip set concentrates the noise-immune token-passing data-link layer and adaptive, spread-spectrum physical layer into low-cost, miniaturized powerline communications components that can be easily incorporated into compact commercial and industrial automation devices.

Network Architectures

A communications architecture specific to control and monitoring networks best fits the user's requirements. The wrong network standard, such as one for a high-speed computer-to-computer file transfer network, can be a Procrustean bed, for which the user must alter existing protocols already successfully in use. However, there are standard communications protocols that are well-suited to distributed control and monitoring applications. These protocols fall into three communications architectures which meet most requirements, as described below and shown in Figure 2.

Transparent Multiple Serial Links

A distributed system often simply consists of dedicated RS-232 serial connections between devices. Such configurations of multiple serial connections are best handled transparently to the network user, such that each attached device "thinks" it is attached to an RS-232 serial cable.

Single Master, Multiple Slaves

Many control and monitoring systems consist of a number of sensors, scanners and actuators controlled by a single intelligent node. In such single-master, multiple-slave networks a simple software driver usually resides on the host computer. The monitoring and control devices support either a minimal driver or require a transparent serial interface to the communications hardware. We have found such a communications architecture can be implemented with either a command-response master-slave network or a round-robin master-slave network.

In a command-response network, the master node initiates all communications and the slave nodes respond to the master over a transparent serial interface. In round-robin polling, any device can initiate communications and talk with any other device

on the network. A master device uses round-robin polling in the background to allow all slaves access to the network with only minimal host interaction.

General Command Set

There is no single user network architecture which is suitable for all applications. Sometimes the user may need to configure the network from the host devices, at the link level.

In its most general configuration, a network can consist of a token-passing loop of master nodes that each control associated groups of slave nodes. Control of the medium access functions can be left to the host without creating a communications bottleneck. Furthermore, the network can then be dynamically configured to handle changing loads and uses.

Typical Applications of a Powerline Network

The above approach, as implemented by Adaptive Networks' products (the AN192 Powerline Network Communications Chip Set, AN192 Powerline Network Communications Module and AN192 Standalone), is field-proven in a broad range of data-critical applications, such as vending machine monitoring, automated meter reading, security and access-control, and industrial automated storage and retrieval material handling systems. For example, the technology has been selected and widely used as an ISO standard (remote monitoring networks of refrigerated cargo containers aboard ships and in terminal storage yards). Vending machine monitoring includes tracking the amount of product in vending machines and the machines' operational status throughout a public facility or shopping area. In material handling applications, a computer controls moving stacker cranes which store and retrieve inventory in an automated warehouse.

Summary

A large variety of control and monitoring applications require simple, low-cost, flexible data communications solutions instead of cabled LANs that were developed for high-speed computer-to-computer networking. The powerline represents an ideal medium for such applications because it eliminates the expense and inconvenience of installing dedicated wiring. The availability of this medium promises to facilitate the increased use of networked systems in buildings.

The hierarchical powerline network architecture builds upon a token passing media access control sublayer, reliable low level link protocol enabling error correction, and spread spectrum physical layer, each optimized for the powerline and for mutual interaction. The interface at the data-link layer provides the required powerline backbone for both current and potential control and monitoring applications.

References

[1] Dixon, R.C., *Spread Spectrum Systems Second Edition*, New York, Wiley, 1984.

[2] Gershon, R., Propp, D., and Propp, M., "A Token Passing Network For Powerline Communications," *IEEE Transactions on Consumer Electronics*, 37(2):129-134, May 1991.

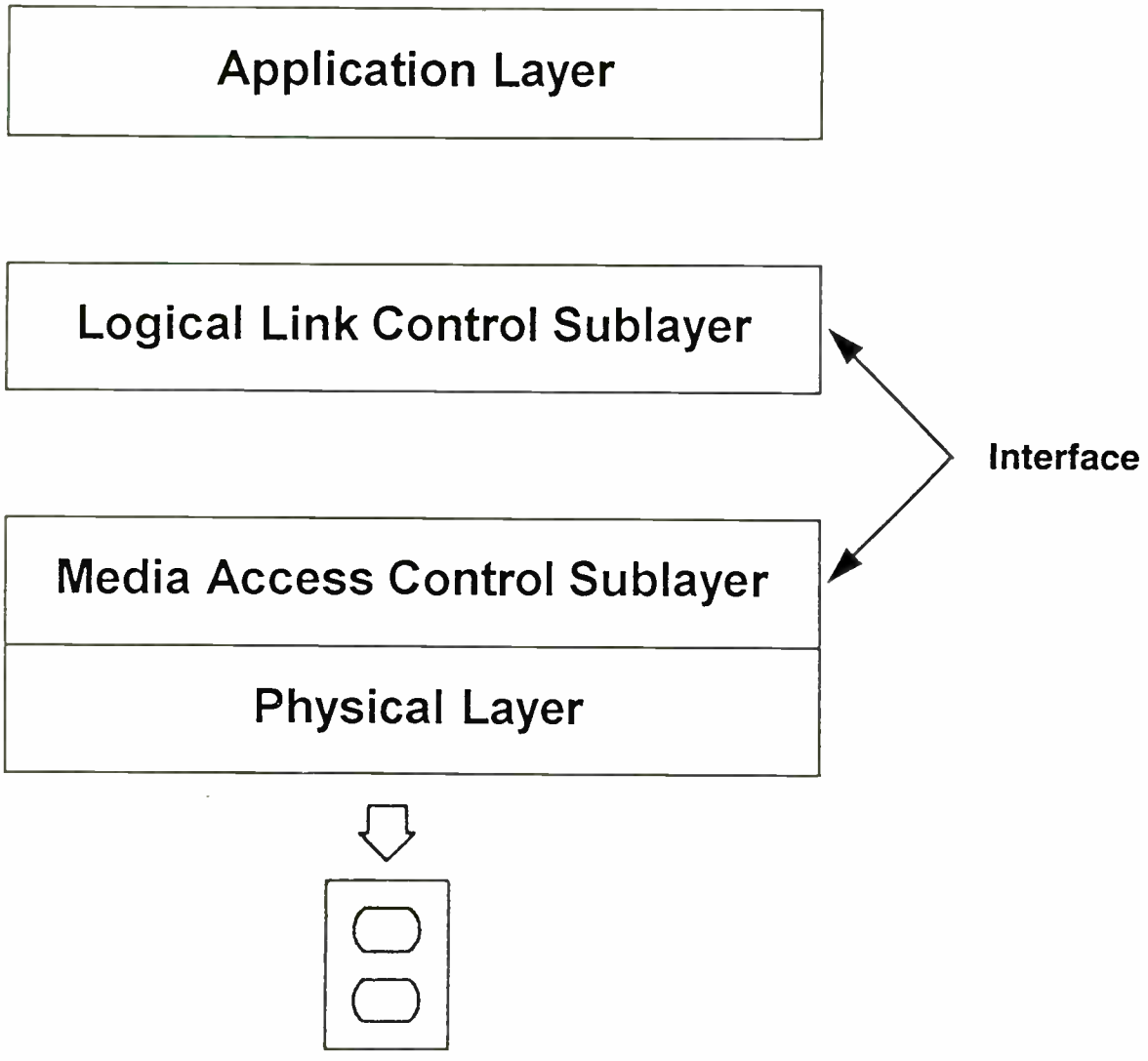

Figure 1. The Data Link Layer Interface to the Powerline-Optimized Lower Layers

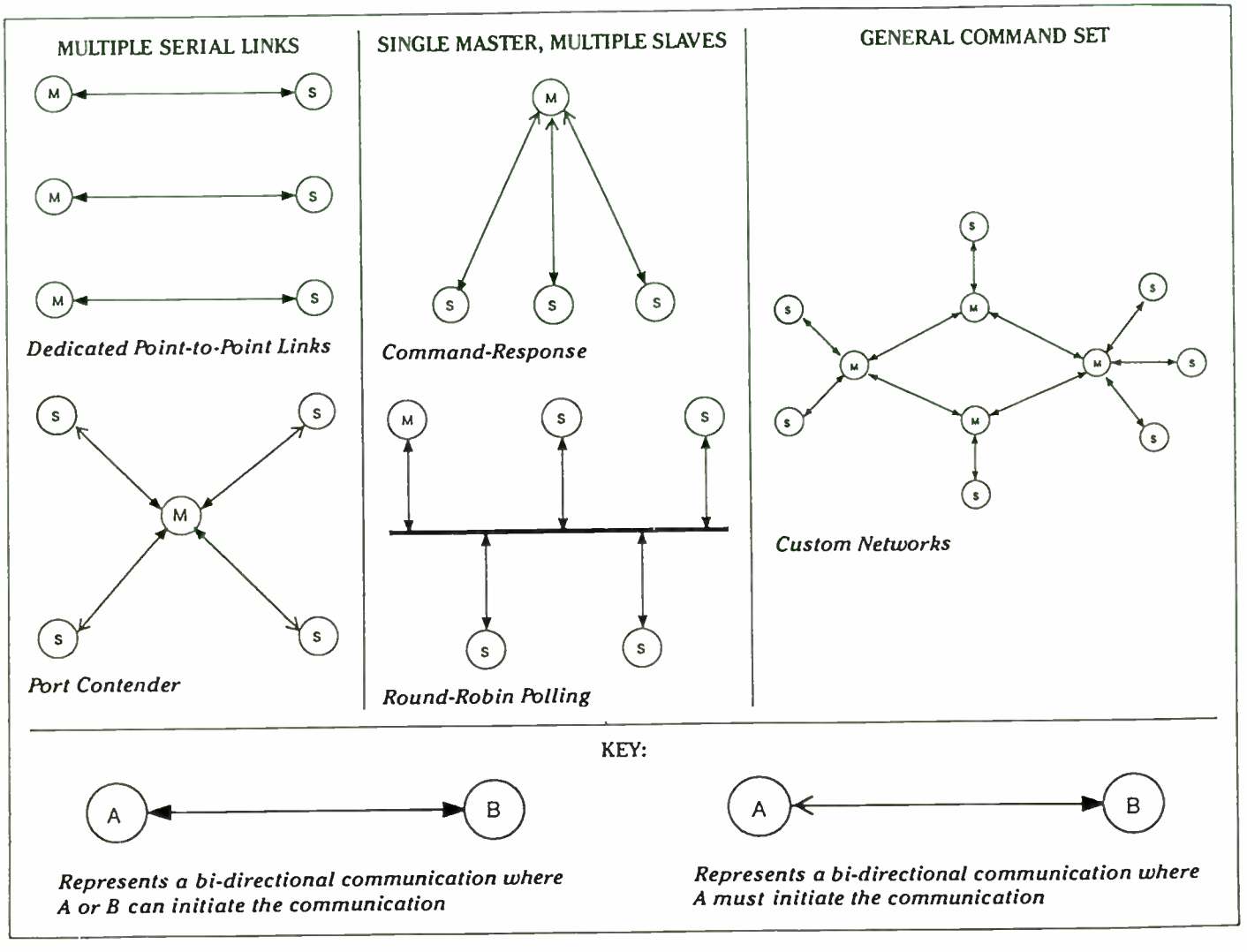

Figure 2. Example Network Architectures

INCREASING SPECTRAL EFFICIENCY IN PERSONAL COMMUNICATION SYSTEMS

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The next generation of cellular systems will require more efficient use of the underlying time-varying channel to accommodate both voice and data transmissions. We will examine several power control techniques aimed at reducing interference in these systems while maximizing the number of users and their corresponding data rates. We propose a hybrid approach to power control that maintains all users at some minimal performance level (e.g. voice rate and quality), and uses variable-rate coding and modulation to increase the performance when fading conditions are mild. This scheme, when coupled with dynamic channel allocation, provides maximum flexibility in the network, allowing it to adapt to variable traffic levels in the overall system as well as to individual quality, data rate, and priority requirements. Finally, we will present numerical results of throughput and capacity for our scheme and for other approaches.

Spread Spectrum Systems:

Evaluating Performance Criteria for Your Application

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INTRODUCTION

Technological developments and changes in Federal Communications Commission (FCC) rules over the last few years have made it feasible to use spread spectrum communications for commercial applications.

This paper presents a brief overview of spread spectrum development and technology and describes the advantages offered by spread spectrum communications in commercial applications. Specific topics include:

> Spreading techniques allowed by the FCC and the relative merits of these techniques in terms of system immunity to interference, jamming, and multipath.
>
> U.S. and international regulations and frequency allocations.
>
> Spread spectrum performance parameters and their effects on interference immunity.
>
> Tradeoffs between maximum attainable communication range and data rate.
>
> System design techniques for ensuring long-term reliability of spread spectrum systems in the face of anticipated band crowding.

The paper will conclude with a discussion of guidelines for selecting systems to serve specific applications.

OVERVIEW

Background

It is characteristic of conventional modulation schemes that they attempt to maximize the concentration of energy for a given message. A spread spectrum system takes the opposite approach, spreading the signal out over a bandwidth much wider than the message bandwidth (figure 1). Various methods are used to spread the signal, but common to all spreading schemes is the use of a reciprocal process at the receiving end to "despread" the signal.

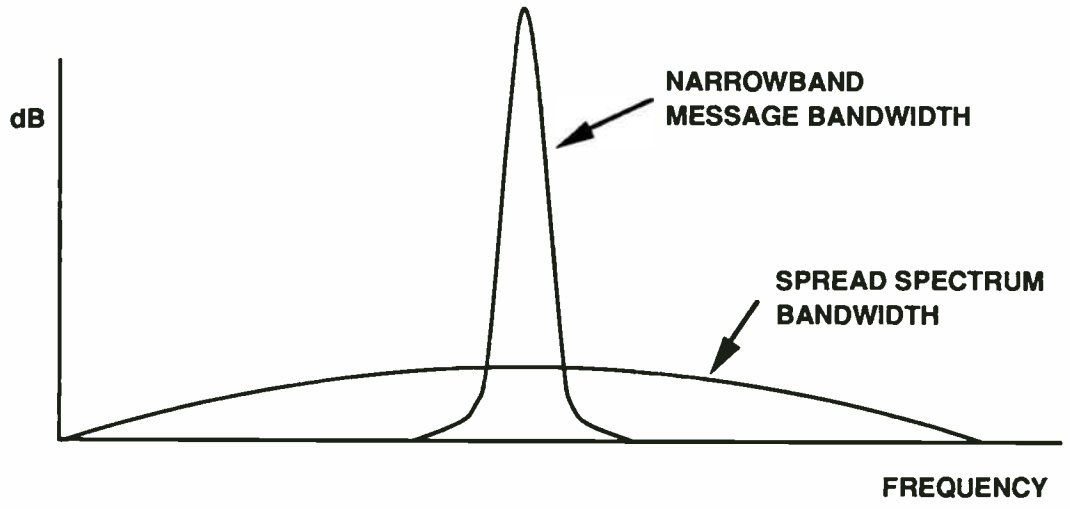

Figure 1. Narrowband Vs. Spread Spectrum Bandwidth

Since the spread spectrum system distributes transmitted energy over a wide band, the signal-to-noise ratio at the receiver input is low – in many cases below the noise floor of a conventional receiver and thus invisible to it. However, by despreading, the spread spectrum receiver restores the level of the desired signal. In addition, while the despreading process restores the desired spread signal, it has the opposite effect on narrow-band interferers – it spreads and thereby suppresses them. Thus the despreading process can recover the desired signal even in the presence of narrow-band interferers with a much greater power density than that of the desired signal.

This characteristic makes spread spectrum systems useful for secure communications: they suppress interference while making it difficult for any unintentional receiver to detect their own transmissions, extract messages, or jam the intended receiver.

Development and Use by the Military

Because they offer secure communications, spread spectrum systems have been of particular interest to the military, which has been developing and using such systems since the 1940s. Until recently the military has operated nearly exclusively in this arena because of the complex signal processing required and because regulating authorities, such as the FCC in the U.S., did not permit spread spectrum transmission by non-military users except on an experimental basis.

Availability for Commercial Applications

Over the last few years, commercial applications of spread spectrum technology have become practical because of technological developments and changes in FCC regulations.

Technological Advances

In the technical area, digital signal processing and very large scale circuit integration have advanced hand in hand, and the very complex circuitry required for baseband spread spectrum signal processing can now be obtained on a single ASIC (Application-Specific Integrated Circuit). All that is required for a complete spread spectrum system is to interface such an ASIC to a properly designed receiver front end and a transmitter.

Though the initial cost of spread spectrum signal processing ASICs was prohibitive for commercial production, this technology has followed the usual pattern for large-scale circuit integration, and cost has fallen dramatically as sophistication has increased. Current prices make commercial application a very attractive proposition.

New FCC Rules

Evidently perceiving the potential for commercial use of spread spectrum systems, the FCC began considering rules for spread spectrum operation in the mid 1980s. Rules were adopted on June 14, 1990, and released on July 9, 1990, in General Docket No. 89-354. These rules, which come under Part 15.247, allow unlicensed spread spectrum operation in the Industrial, Scientific, and Medical (ISM) bands. In addition, the FCC is now deliberating rules for unlicensed Personal Communications Systems (PCS).

Frequency assignments established for ISM and under consideration for PCS are as follows:

Frequency	Bandwidth
ISM BANDS	
902–928 MHz	26 MHz
2400–2483.5 MHz	83.5 MHz
5725–5850 MHz	125 MHz
PCS BAND	
1890–1930 MHz	40 MHz

For ISM, maximum transmitter power output is 1 watt and maximum effective radiated power (ERP) is 4 watts.

For PCS, maximum power is tentatively set equal to

$$100\ \mu W \times \sqrt{BW\ (Hz)}$$

For example, with a 1-MHz spreading bandwidth, maximum power is 100 milliwatts. If 20-MHz bandwidth is used, maximum power is approximately 450 milliwatts. Directional antennas with a maximum gain of 3 dBi are allowed. Power density should be limited to 3 milliwatts in a 3-kHz bandwidth.

Permissible spreading techniques are frequency hopping, direct sequence, and hybrid (combination of frequency hopping and direct sequence). These techniques and the regulations concerning their implementation are discussed below.

Because it has become extremely difficult to find available channels for licensed operation in metropolitan areas, it is a tremendous advantage to the user community that spread spectrum systems are allowed to operate at reasonable power with no licensing requirements. In contrast, power levels for unlicensed conventional modulation are extremely low. For example, in the 902–928 MHz band, transmitter output for non-licensed conventional systems is limited to a maximum field strength of 50 mV/m @ 3 m. This is approximately equivalent to .0007 watts into a dipole antenna, i.e., about 32 dB less than the 1 watt allowed for spread spectrum. This gives spread spectrum systems a substantial edge in range and reliability, an edge which is further increased to 38 dB because the FCC allows the use of directional antennas to produce up to 4 watts ERP.

International Rules

Regulating authorities in Mexico, Canada, and Australia have followed the U.S. FCC in adopting spread spectrum rules for the 902–928 MHz band, though in Australia, operations are limited to 915–928 MHz. A number of other countries are considering similar rules for 902–928 MHz, particularly where there is no conflict with the GSM network (European Cellular System).

Rules for the 2.4-GHz band are also being adopted in other countries. For example, the U.K. has released an interim standard, MPT1349. It is anticipated that unlicensed operation in Europe will be in the 2.4–2.5 GHz band, though European regulations are still being deliberated. The RES2 standard proposed by ETSI (European Telecommunications Standards Institute) will be available shortly as a draft application. Japanese regulations have not yet been finalized; however, proposed regulations are for an ISM band of 2.471–2.497 GHz (26-MHz bandwidth).

Advantages of Spread Spectrum Systems

The performance characteristics and FCC regulations just described combine to give spread spectrum systems a number of advantages over conventional systems. These include:

- interference immunity

  Spread spectrum systems can operate reliably in the presence of high-power jamming signals. In addition direct sequence spreading techniques (see below) offer effective rejection of multipath signals.

- low interference production

  Spread spectrum signals appear as low-level noise to conventional receivers and may be well below receiver threshold.

- high data rates

  Allowed bandwidth for spread spectrum makes very high data rates attainable.

- non-licensed operation at practical power levels

  The licensing process is avoided, and there is now a practical alternative in metropolitan areas where licenses may be unobtainable.

Of these advantages, the latter three are available from equipment complying minimally with FCC requirements, but the first – interference immunity – is realized effectively only by equipment embodying design principles that go beyond FCC requirements. The elements necessary for effective interference immunity – processing gain, receiver linearity, and AGC range – are discussed in later sections.

COMMERCIAL APPLICATIONS

A wide range of applications will benefit from the security, reliability, high data rate, and range offered by the best commercial spread spectrum systems. These applications include point-to-point, point-to-multipoint, or multipoint-to-multipoint data communications; remote control; and remote sensing systems such as the following:

- wireless LAN
- personal communication networks (PCN)
- security systems
- voice communications
- bridge and router networking
- instrument monitoring
- factory automation
- remote bar code reading
- automatic vehicle location/IVHS applications
- pollution monitoring
- extended-range cordless phones
- videoconferencing
- traffic signal controls
- medical applications
- point of sales
- remote sensing (temperature, seismic, etc.)
- factory data collection
- inventory control
- SCADA systems
- vending machine monitoring

SPREAD SPECTRUM TECHNOLOGY

Overview of Basics

Definition – Frequency Band Spreading

As stated above, spread spectrum transmission bandwidth is much greater than the minimum required to transmit the information. More specifically, a system transmitting digital information must have the following characteristics to be classified as spread spectrum:[1]

1. Transmitted signal energy must occupy a bandwidth much larger than the information bit rate and independent of the information bit rate.

2. Demodulation must be achieved by correlation of the received signal with a replica of the signal used in the transmitter to spread the information signal.

Techniques of Spread Spectrum Modulation

Two basic techniques are allowed by the FCC for bandwidth spreading, direct sequence and frequency hopping. The FCC also allows the combining of both techniques in a hybrid scheme.

Direct Sequence

In a direct sequence system, the baseband data is directly modulated by a much higher frequency spreading signal, referred to as a *pseudonoise (P/N) code*. The P/N code is a very fast binary bit stream designed to appear random, i.e., a mix of approximately equal numbers of zeroes and ones. Each P/N code bit is called a *chip*.

Spreading signal bandwidth should be large relative to the data bandwidth to ensure that signal bandwidth is dominated by the spreading signal and therefore nearly independent of the data signal.

At the receiving end, the P/N code is duplicated and synchronized for signal despreading and is selected to have properties that facilitate the despreading process at the intended receiver while making demodulation by unintended receivers difficult. These properties also allow the intended receiver to discriminate between the signal and interferers or jammers.[2]

Modulation is usually achieved by a form of digital phase modulation such as binary phase-shift keying (BPSK) or quadrature phase-shift keying (QPSK). Other methods, such as amplitude or frequency modulation, are less immune to interference and compromise privacy, since amplitude modulation can be recovered by an envelope detector and frequency modulation by a squaring device and frequency discriminator.[3]

The interference immunity of a properly implemented direct sequence system is indicated by *processing gain* and *jamming margin*. These terms are defined and discussed in a later section.

FCC rules require that direct sequence spread spectrum systems have the following characteristics:

minimum bandwidth (6 dB)	500 kHz
minimum P/N code length per bit	10 chips
maximum power density	8 dBm over a 3-kHz bandwidth

Frequency Hopping

In a frequency hopping spread spectrum system, the bandwidth of a data-modulated carrier is spread by periodic changes in the carrier frequency. The amount of time the carrier remains on a single frequency (channel) is called the dwell time; to avoid interfering with conventional users and achieve immunity to interference from conventional users, the dwell time must be very short.

Although not essential to the frequency hopping technique, frequencies are chosen from a set of 2^k frequencies spaced approximately at the width of the data modulation spectrum.[4] The frequency hopping sequence is fixed and is replicated at the receiver where it is mixed with the received signal for despreading.

As presently implemented in commercial systems, frequency hopping offers no processing gain (see below for definition). These systems rely on interference avoidance rather than interference suppression.

FCC rules require that frequency hopping systems have the following characteristics:

minimum number of hopping channels: 50 in the 902–928 MHz band, 75 in the two upper bands

maximum occupancy in single channel: 400 ms

minimum time before reuse of channel: 20 seconds in 902–928 MHz band, 30 seconds in the 2400–2483.5 and 5725–5850 GHz bands.

Hybrid

A hybrid spread spectrum system is a direct sequence system in which the carrier frequency changes periodically. This offers four advantages:

(1) Because it can frequency-hop over a much greater band than it can occupy with practical direct sequence techniques, the frequency hopper can use available bandwidth more effectively.

(2) By combining direct sequence and frequency hopping techniques, the frequency hopper combats interference in two ways: hopping avoids the interference signal part of the time, and when the system hops into the interference band, the interference is spread and filtered by direct sequence techniques.[5]

(3) A hybrid system offers the multipath rejection of a direct sequence system. (Multipath rejection is not available in commercial frequency hoppers.)

(4) A hybrid system can use the available band with fewer hopping channels than a pure frequency hopper.

Thus by taking advantage of the best features of both techniques, a hybrid system can provide very robust performance.

A system that meets FCC requirements for direct sequence spread spectrum can employ a variant of the hybrid design by hopping selectively. Such a system seeks the channel with the lowest noise and interference and operates on that channel without further frequency hopping as long as interference remains low enough to be combated by direct sequence techniques. When interference exceeds this level, the system sequences through the hopping channels until it finds the next low-interference channel.

The variant hybrid system just described is particularly suited to commercial applications, where deliberate jamming does not normally occur and signal decoding by unintended receivers is not a primary concern.

Processing Gain and Jamming Margin (Direct Sequence Only)

Definitions

Processing Gain

Processing gain is a consequence of the reciprocal spreading/despreading process in a direct sequence spread spectrum system.[6] The receiver correlates the signal with its locally generated P/N code; when the two signals are matched, the data signal is despread to its original bandwidth, while unmatched signals are spread to the P/N code bandwidth. In other words, the receiver enhances the desired signal while suppressing noise and interference,[7] thereby increasing the signal-to-noise ratio of the output signal over that of the input signal. The ratio of the output and input signal-to-noise ratios is defined as *processing gain.*

In a properly implemented direct sequence spread spectrum system, processing gain can be estimated by the equation

$$\text{processing gain} = G_p = \frac{BW_{RF}}{\text{data rate}}$$

where BW_{RF} is the bandwidth of the transmitted spread spectrum signal.

Jamming Margin

The system may not be able to perform in the presence of an interference signal whose power is greater than the desired signal by the amount of the processing gain. The capability of a system to perform in the presence of such interference is its *jamming margin*. Jamming margin takes into account the requirement for useful signal-to-noise

ratio in the system output and allows for internal losses and is thus always less than the processing gain:

$$\text{jamming margin} = G_p - \left[L_{sys} + \left(\frac{S}{N}\right)_{out}\right] = M_j$$

where L_{sys} = system implementation losses

$\left(\frac{S}{N}\right)_{out}$ = signal – to – noise ratio at the information output.

A system with 30-dB processing gain, minimum 3 dB $(S/N)_{out}$, and 2 dB L_{sys} would have 25 dB jamming margin: It could not be expected to operate with interference more than 25 dB above the desired signal.[8]

Comparison of Frequency Hopping, Direct Sequence, and Hybrid Spreading Techniques

The basic spreading techniques, frequency hopping and direct sequence, can be compared in the following areas: complexity of implementation, interference immunity, multipath rejection, and data rate capability. Remarks about both techniques apply to hybrid systems.

Complexity of Implementation

Frequency hopping is easiest to implement. A frequency hopper is essentially a frequency-synthesized FM system, preferably with a fast-settling synthesizer loop for quick switching among channels. Off-the-shelf designs consisting of a conventional limiting receiver and a class-C transmitter amplifier suffice for frequency hopping systems and are generally used in commercially available equipment. For reliable performance, packet communication with error correction and retry must be used.

A properly designed direct sequence system is substantially more complex. It requires a high-linearity receiver front end with automatic gain control (AGC) – preferably more than one AGC loop for widest possible dynamic range. The transmitter amplifier must also have linear performance because BPSK or QPSK modulation is used for best interference rejection. In addition, modulation and demodulation techniques are more complex than for frequency hopping, and matched filters or other elaborate circuitry is needed for despreading.

Interference Immunity

Interference rejection is achieved differently by each technique – the frequency hopper avoids interference, while the direct sequence system reduces interference level by despreading. The two systems also differ in their response to increasing interference. the frequency hopper degrades gracefully by a reduction in data throughput. This occurs because transmissions in jammed channels are not received and must be repeated in free channels. For example, a frequency hopper with a nominal 500 Kbit/second data

rate will continue to operate even if 90% of the channels are jammed, but data rate will drop to 50 Kbit/second.

In contrast, a direct sequence system will maintain its data rate as long as jamming is below margin; however, once jamming exceeds margin, performance may collapse completely. To prevent this, jamming margin can be increased by raising processing gain, but this may result in unacceptably low data rates. As an alternative, special techniques such as transform-domain processing and adaptive filtering can be used to increase jamming margin without a loss of data rate. This subject is discussed in a later section.

(As suggested in the previous paragraph, high data rates and high processing gain are tradeoffs, since high processing gain is realized by increasing the P/N code length per data bit, and this reduces data rate. See below, "Effects of Data Rate on the Performance of a Communication System.")

Multipath Rejection

A frequency hopping system has no inherent multipath rejection, so extrinsic techniques such as diversity antennas and error correction are used to combat multipath. Multipath rejection is inherent in direct sequence design and increases with processing gain.

Data Rate

Maximum data rate for a frequency hopping system complying with FCC rules is 500 Kbit per second in the 915 MHz band and 1 Mbit in the 2.4 GHz band. This is a consequence of the maximum bandwidth allowed per hop. In the presence of interference, data rate throughput is reduced, as discussed above.

Maximum data rate for direct sequence depends on P/N code rate, code length and implementation, frequency band, and modulation type. For example, a system using a 13-chip Barker code at a 13-Mchip code rate and QPSK modulation in the 915 MHz band has a 2-Mbit data rate. A system using a 13-chip Barker code at a 40-Mchip rate and QPSK modulation in the 2.4 GHz band has a 6.0-Mbit data rate. Data rate is maintained in the presence of interference below the jamming threshold.

Conclusion

For lower data rates, a direct sequence spread spectrum system is potentially superior to a frequency hopper in interference immunity and multipath rejection. On the other hand, with reduced processing gain, a direct sequence system offers higher data rates than a frequency hopper. Against these advantages is the increased complexity and cost of a direct sequence system. Choice of spreading technique will depend on the intended application, as will be discussed below in the section dealing with system evaluation.

SPREAD SPECTRUM FREQUENCY BANDS – COMPARATIVE ADVANTAGES/ DISADVANTAGES

This discussion will be limited to the 915 MHz and 2.4 GHz bands. No equipment has yet been made available for the 5.8 GHz band because of the higher costs required for implementation at the higher frequency,[9] and use of the PCS band is not yet authorized.

The 915 MHz band has two advantages over the 2.4 GHz band: 8.4 dB lower free-space attenuation and less constraint to line-of-sight communications. On the other hand, the 2.4 GHz band offers offsetting advantages: higher data rates and smaller antennas. (Reduced size makes it practical to design a high-gain directional antenna.) As a result, certain applications are better served by one or the other band. This topic will be explored further in the discussion of evaluation criteria, below.

RELIABILITY OF SPREAD SPECTRUM SYSTEMS

Use of the 902–928 MHz band is increasing rapidly – indeed, 902–928 MHz is sometimes characterized as the "kitchen sink band" or "jungle band" because unlicensed spread spectrum users coexist with licensed government and ham operations, ISM equipment, and Automated Vehicle Monitoring (AVM) equipment. The congestion and user mix in this band have raised questions about the ability of commercial spread spectrum systems to cope, and with some justification. With few exceptions, available commercial systems are designed with cost as the governing concern. Their performance barely meets minimum FCC standards for spread spectrum qualification, and their reliability is likely to be compromised by increasingly adverse conditions.

However, such systems poorly represent the potential of spread spectrum. With proper design, the military has used spread spectrum technology with notable success in extremely hostile environments, contending with deliberate high-power jammers. The worst conditions anticipated in the 902–928 MHz band are benign in comparison. Advances in digital signal processing and large-scale integration have made it possible for commercial systems to offer the interference suppression and avoidance capabilities used so successfully by the military.

A number of manufacturers have chosen to use the 2.4 GHz band, claiming that their equipment offers greater reliability than systems operating in the 902–928 MHz band. This claim will be valid only as long as there is less activity in the higher-frequency band, but use of this band is increasing rapidly, and the only way to ensure reliability in the long run is to employ proper design techniques to ensure high processing gain and interference rejection.

It is important to keep in mind that properly designed direct sequence and hybrid systems can operate compatibly in the same band if different P/N codes are used. In fact, Code Division Multiple Access (CDMA) – a scheme that allows multiple users simultaneous access to the same band by assigning a different P/N code to each user – has been successfully evaluated for PCS applications.

Additional Interference Suppression Techniques for Direct Sequence Systems

Spread spectrum systems can be compromised by high-power narrow-band interference, but direct sequence spreading offers a number of interference rejection techniques which have already been discussed. In addition to the interference rejection properties inherent in good direct sequence design, there are a number of special techniques that can be used to enhance rejection of high levels of narrowband interference. Among these are *transform-domain processing* and *adaptive filtering.*

Transform-Domain Processing

The Fourier transform of a direct sequence signal and that of a narrowband interference signal have distinctly different pulse widths. Transform-domain processing takes advantage of this difference to detect and counteract interference signals. When an interference signal is detected, the composite output of the Fourier transformer is multiplied by an appropriate gating signal to produce a notched signal, removing a large amount of interference power and relatively little of the desired signal power. As an alternative to using a gating signal, the transform can be clipped. An inverse Fourier transformer then restores the direct sequence signal slightly distorted but with much less interference power.[10]

Adaptive Filtering

An adaptive filter adaptively estimates interference from a block of sample values of a received signal and subtracts the estimate from the signal. An adaptive transversal filter is used with an adaptive algorithm that can distinguish between the signal and narrow-band interference. The algorithm takes advantage of the fact that the interference components at the filter output are correlated with each other, while the direct sequence components are largely uncorrelated. The algorithm adjusts the weights by which each filter tap is multiplied to minimize filter output, canceling interference while leaving the direct sequence signal essentially unaffected.[11]

EFFECTS OF DATA RATE ON THE PERFORMANCE OF A COMMUNICATION SYSTEM

Since most of the applications discussed in this presentation involve data communication, is it relevant to address the subject of data rate and its effect on communication system performance.

In many applications – though certainly not all – efficient performance depends on maximizing data transfer rate within the limits imposed by cost, media, and regulation. In wireline communication, physical limits allow only low or moderate data rates, and the demand for higher data rates has motivated the transition to coaxial and fiber optic cables – at considerable cost.

In wireless communications – both conventional and spread spectrum – data rate limits are imposed more by regulations than by cost constraints. For example, transmitter power level regulations effectively set a limit on data rate because receiver sensitivity drops by 3 dB for every doubling of data rate. Transmitter power can be doubled to make up for this loss, maintaining system gain, but only up to the regulation limit. Past

that point, data rate increases require a sacrifice of system gain. This results in range reduction, since range is cut in half by each 6 dB loss in system gain (assuming free-space attenuation). For example, a system with a 20-mile line-of-sight range operating at 8 Kbit/second will have a 1-mile range at 2 Mbit/second.

In a direct sequence spread spectrum system, bandwidth regulation forces a tradeoff between data rate and processing gain. As shown in the following equation, introduced above, processing gain is inversely proportional to data rate.

$$\text{processing gain} = G_p = \frac{BW_{RF}}{\text{data rate}}$$

Bandwidth can be increased to maintain processing gain, but only up to the maximum allowed by regulation. Therefore, in a spread spectrum system, a point is reached where maximum range is reduced by losses both in system gain and in the interference rejection provided by processing gain. Typically, high-data-rate spread spectrum systems (≥1 Mbit/second) have reliable ranges on the order of a few hundred feet. For reliable long-range communication, data rates must be kept low or moderate.

EVALUATING PERFORMANCE CRITERIA FOR YOUR APPLICATION

The evaluation process for selection a spread spectrum system can be broken down into three steps: selection of spreading technique, selection of operating band, and evaluation of performance specifications.

Selection of Spreading Technique: Direct Sequence, Frequency Hopping, or Hybrid

Selection of spreading technique depends on the data rate, range, and robustness required by the application.

Computer Connectivity (LAN)

For computer connectivity applications (LAN), the choice may be fixed by IEEE standard. The 802.11 committee of the IEEE appears to favor frequency hopping for the wireless LAN standard, and the committee is supported by a number of companies because of the easier implementation and lower cost of frequency hopping technology.

Long-Range Low/Moderate Data Rate Applications

A direct sequence system with high processing gain is a good choice for long range applications with low -to-moderate data rate requirements. Special interference suppression techniques are desirable to improve the robustness of the system, and for maximum reliability, a hybrid system using selective frequency hopping may be required.

Critical/Vital Applications

A hybrid system combining frequency hopping with high-processing-gain direct sequence is a must for critical applications such as traffic light control, life support

monitoring, remote control of dangerous equipment, etc. Special interference suppression techniques should be employed for maximum reliability.

Frequency Band Selection (915 MHz vs. 2.4 GHz)

Selection of frequency band is the next area to be considered in evaluating spread spectrum systems. Selection criteria are grouped by application.

Long-Range Multipoint Communication

Lower free-space attenuation and reduced constraint to line-of-sight make the 915 MHz band the logical choice for long-range multipoint communications. Omnidirectional ranges up to 20 miles are feasible, providing low data rates (≈8 Kbit/second) are acceptable. At such data rates, processing gains up to 24 dB are easily attainable, and adaptive narrowband interference cancellation techniques can be used for increased reliability. Reliability can be increased further by the use of selective frequency hopping: with an 8 Kbit/second data rate and 24-dB processing gain, as many as 12 non-overlapping hopping channels are available.

Point-to-Point Communications

The 915 MHz band also offers the longest ranges for point-to-point communications, but its advantages over the 2.4 GHz band are not as great as for multipoint. This is because the smaller size of a 2.4 GHz directional antenna makes it possible to obtain higher gain at a lower price than with a 915 MHz antenna, offsetting increased attenuation.

It must be noted, however, that FCC rules limit ERP to 4 watts (36 dBm), and it may be necessary to cut back transmitter power output. For example, a 16-dBi yagi antenna will require that output power be limited to 100 milliwatts (20 dBm). Thus the 36-dBm ERP limit means that the benefits of antenna directionality are realized only at the receiving end.

High Data Rate Applications

The 2.4 GHz band is the logical choice for high data rates. As stated earlier, a frequency hopper can achieve a data rate of 1 Mbit/second in this band vs. 500 Kbit in the 915 MHz band. A direct sequence system can operate at 6.0 Mbit/second with QPSK modulation at 2.4 GHz vs. 2.0 Mbit/second at 915 MHz.

As discussed above, however, the range for reliable communication is drastically reduced at high data rates, since there is a 3-dB loss in receiver sensitivity for each doubling of data rate.

In-Building Communications

In-building communications are better served by 2.4 GHz because shorter wavelengths offer better propagation in this environment.

System Specifications

A review of system specifications should be the final step in evaluating spread spectrum systems. Unfortunately, no commercial specification standards have yet been established for this rather new technology, and each manufacturer presents specifications in his own way, inadvertently confusing the prospective user. In some cases specifications give minimal information such as "900-MHz spread spectrum radio," along with data rates and interfaces. Not even the spreading technique – direct sequence, frequency hopping, or hybrid – can be inferred from this information, and an informed selection is not possible.

The following performance parameters should be sought and considered.

Frequency Hopping Systems – Most Important Parameters

Number of Hopping Channels

A frequency hopper with a high data rate will most likely use the minimum number of hopping channels required by the FCC – 50 channels in the 915 MHz band and 75 channels in the 2.4 and 5.8 GHz bands. If data rates are lower, the system may use many more channels. For example, an 8 Kbit/second system can use up to 2000 channels in the 915 MHz band and up to 7000 channels in the 2.4 GHz band. Select the system with the greatest number of hopping channels if synchronization time is of secondary importance (see next item).

Synchronization Time

Synchronization time is the time required for the receiver to synchronize to the transmitter; synchronization must occur before data can be sent. Synchronization time increases with the number of hopping channels, so a compromise may have to be made between the two parameters, especially for applications in which a message is to be sent through a number of repeaters. A long synchronization time may cause unacceptable time delays.

Channel Hopping Time

The time required to hop from one frequency to the next is also an important parameter, since it affects data throughput: the shorter time, the higher the throughput.

Other Important Parameters

- Transmitter Power Output

This parameter is usually specified. Maximum power allowed is 1 watt. Select a full-power unit, if possible, for maximum link margin.

- Receiver Sensitivity

This parameter is typically specified in dBm at 10^{-6} bit error rate. A low figure signifies high sensitivity, required for maximum link margin.

- Adjacent Channel Rejection Ratio

A high ratio indicates that a high-quality IF filter is used.

Direct Sequence Systems – Most Important Parameters

Processing Gain

This is the most important parameter generally available from the manufacturer because it quantifies the robustness of a direct sequence spread spectrum system – the higher the processing gain, the better the interference rejection. (Jamming margin, which is a better indication of interference rejection, is usually not specified by manufacturers.)

Processing gain is specified in dB, and 10 dB is the minimum processing gain required for qualification as a direct sequence spread spectrum system according to FCC rules.

In some cases, manufacturers specify P/N code length without stating processing gain. If the full P/N code is used for each data bit, processing gain in dB (G_p) can be calculated:

$$G_p = 10\log(\text{code length per data bit})$$

If the manufacturer does not state explicitly that the full code length is used per data bit, you must inquire, since the processing gain depends on this relationship. For example, a 32-chip code gives a 15-dB processing gain if it modulates a single data bit but only 12 dB if it modulates two data bits.

Receiver Linearity and AGC Control Range

Unlike frequency hoppers, which use limiting receivers, a direct sequence system must use a high-linearity automatic gain control (AGC) receiver front end in order to take advantage of processing gain. This is because limiting of interference signals reduces the suppression of these signals in the despreading process. A well designed receiver will typically employ at least two AGC loops, one loop immediately after the antenna to prevent saturation of the low-noise front end amplifier (LNA), and another loop in the IF stages. A robust system might have AGC control range in excess of 100 dB.

Synchronization Time

Synchronization time in direct sequence systems involves the same considerations discussed above for frequency hoppers. However, in direct sequence systems, techniques using digital matched filters can provide virtually instantaneous synchronization (within 1 data bit). These techniques are not available in commercial frequency hoppers.

Look for short synchronization time, particularly if your system will be sending data over long distances through a chain of repeaters.

Modulation Method

For robustness, look for systems using BPSK or QPSK modulation. Systems using FSK modulation also use a limiting receiver and therefore offer inferior interference rejection.

Other Parameters

Transmitter Power and Receiver Sensitivity

As described for frequency hopping systems, transmitter power output and receiver sensitivity are important for maximum link margin.

- Adjacent Channel Rejection

Because a direct sequence system has processing gain, adjacent channel rejection is not as critical as for frequency hoppers.

Hybrid System Specifications

Direct sequence parameters are of primary importance in a hybrid system. Frequency hopping parameters will essentially be set by FCC rules, since the number of channels will be limited by the available bandwidth, and synchronization time for the hopping mode will be very fast because of the limited number of channels used.

If selective frequency hopping is used, channel hopping time is relatively insignificant, since channel hopping does not occur frequently.

SUMMARY

Spread spectrum technology, formerly restricted to military use, is now practical for commercial applications because of technological advances and new FCC regulations. Regulating bodies in other countries are following the example of the FCC, making spread spectrum a viable technology for equipment intended for sales abroad.

Spread spectrum offers a number of advantages over narrowband techniques, principal among them interference immunity, low interference production, high data rates, and non-licensed operation at practical power levels.

Spread spectrum is appropriate for a wide range of commercial applications in areas including point-to-point and multipoint data communications, remote control, and remote sensing.

Spreading techniques allowed by the FCC are frequency hopping, direct sequence, and hybrid. Frequency hopping offers the advantages of simpler and less expensive technology. Direct sequence offers processing gain and jamming margin, which yield interference and multipath rejection. In addition, immunity to interference can be enhanced by special techniques. Direct sequence also provides the highest data rates, though data rate may have to be traded off for maximum interference rejection. Hybrid systems provide the highest reliability by combining interference rejection and interference avoidance.

One PCS frequency band and three ISM bands are available. (Regulations have not yet been set for PCS, and equipment is not yet being produced for the highest-frequency ISM band.) Each of the ISM bands offers advantages and disadvantages which must be taken into consideration when selecting for specific applications.

Evaluation for specific applications requires a careful review of specifications which may not be offered by some manufacturers. It may be necessary to obtain essential specifications by direct inquiry.

CONCLUSIONS

Spread spectrum offers an extremely attractive means of reliable data communication. Technological advances have made it affordable and new FCC regulations allowing unlicensed operation at reasonable power levels have made its use convenient and effective. Increasingly, spread spectrum may become the only alternative in areas where heavy use of licensed channels makes new licenses impossible to obtain.

Its interference rejection potential makes spread spectrum particularly attractive for applications requiring reliable data transmission. Because of this characteristic, an unlicensed spread spectrum system may be preferred even when licensed channels are available.

Spread spectrum equipment is now available offering a wide range of performance, and the newness of the technology makes performance difficult to evaluate in choosing a system for a specific application. The performance specifications discussed in this presentation are intended to make it possible to make an informed choice of a system that will offer excellent performance in your application now and in the future.

FOOTNOTES

[1] Rodger E. Ziemer, Roger L. Peterson, *Digital Communications and Spread Spectrum Systems* (Macmillan, New York, 1985), p. 328.

[2]Ziemer and Peterson, page 332.

[3]Don J. Torrieri, *Principles of Secure Communication Systems* (Artech House, Boston, 1992), p. 95.

[4]Ziemer and Peterson, page 348.

[5]Torrieri, p. 272.

[6]Although frequency hopping systems used by the military have processing gain, currently available commercial frequency hoppers do not, and the topic of processing gain in frequency hoppers is not discussed in this presentation.

[7]Robert C. Dixon, *Spread Spectrum Systems*, 2nd ed. (John Wiley and Sons, New York, 1984), p. 10.

[8]Dixon, p. 10.

[9]As low-cost large-scale-integrated circuits become available, the 5.8 GHz band will be an excellent choice for non-licensed microwave point-to-point communications because of the small antenna size required. At this frequency, dish antennas are practical.

[10]Torrieri, p. 190.

[11]Torrieri, p. 192.

TLE-95 and TLC Bridge the Microwave and Digital Worlds

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The materials needed to bridge the digital and microwave worlds has now evolved. Utilizing PTFE (Teflon) resin and building-block construction techniques used in digital laminates, Taconic has developed TLC and TLE-95 laminate materials for low-cost, high-reliability, stripline, microstrip, plated-through-hole, double-sided and multilayer circuit boards. These materials exhibit consistent, tight-tolerance dielectric constants, thicknesses, and low-loss properties as well as excellent mechanical and thermal stability. TLE-95 and TLC are used to construct the complete circuit package or in combination with digital substrate materials such as FR-4. The circuit-board processing procedures are more forgiving than traditional PTFE-based materials, resulting in improved efficiency and lower processing costs.

The TLE-95 and TLC material properties will be compared with traditional PTFE-based materials as well as common digital substrates. Constructive techniques to utilize TLE-95 and TLC in multilayer boards including in combination with FR-4 and circuit-board processing procedures will be highlighted.

A New Modulation/Radio Technique for Wireless Applications

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Abstract

A power and spectrally efficient double jump filtered FQPSK with cross-correlator (DJ-FQPSK) is proposed for higher data rate FH, DS spread spectrum wireless LAN's applications. With the simplest threshold detectors (binary robust eye diagrams in I and Q channels), this system has an increased data rate of more than 1.5 Mb/s in a 1 MHz bandwidth, which is 50% more spectrally efficient than the recently standardized GFSK system. The bandwidth here is defined at -20dB power spectral density(PSD) which is the "conservative" interpretation of FCC definition.

The BER performance of the proposed DJ-FQPSK in a NLA-AWGN environment is also evaluated. As compared to GFSK, with 50% higher bit rate, DJ-FQPSK has 2.5dB Eb/No advantage at BER = 10^{-5}. Results indicate that DJ-FQPSK is a power and spectrally efficient candidate for wireless LAN's, especially for higher data rate applications.

I. Introduction

The increasing demand for radio spectrum by wireless communications and limited radio spectrum resources make spectral efficiency one of the most important issues in any modulation/radio techniques being considered for wireless applications. On the other hand, in order to achieve higher power efficiency, i.e. increase battery life time, a non-linear power amplifier is required. Therefore conventional linear modulation schemes, which

usually have good spectral efficiency, are not suitable for wireless applications because of the spectrum spreading after non-linear amplification. A power and spectrally efficient NLA modulation technique is needed for the emerging wireless communications.

In this paper, we propose a double jump filtered cross-correlated FQPSK (DJ-FQPS) modulation system for wireless communications, especially for the higher data rate FH/DS spread spectrum wireless LAN's applications. With the simplest threshold detectors (binary robust eye diagrams in I and Q channels), this system has an increased data rate of more than 1.5 Mb/s in a 1 MHz bandwidth, which is 50% more spectrally efficient than the recently standardized GFSK system[4]. Furthermore. with 50% higher spectral efficiency, the proposed system has 2.5 dB Eb/No advantage over GFSK at $P_e = 10^{-5}$ [4]. Research results indicate the DJ-FQPSK system is a power and spectrally efficient modulation technique suitable for wireless LAN's, especially for higher data rate applications.

This paper is organized as follows. After the introduction, DJ-FQPSK system including both modulator and demodulator is described in detail in section 2. Spectral efficiency and BER performance of DJ-FQPSK in a non-linear environment is presented in section 3. Section 4 is a summary of this paper.

II. System Description

1. Modulation

The block diagram of DJ-FQPSK modulator is presented in Figure 1. The DJ-FQPSK baseband signal can be generated by passing the cross-correlated FQPSK(FQPSK-X) baseband signal through a DJ filter as shown in Figure 1. FQPSK-X was invented and patented by S. KAto and K. Feher[8], which introduces cross correlations between the in-phase channel and quadrature channel signals. By controlling the cross correlation factor, FQPSK-X can be designed to have an envelope fluctuation from 3 dB (FQPSK) to approximately 0 dB (quasi constant envelope) depending on specific system non-linearities. The signal space diagrams of FQPSK-X with different cross correlation factor, A, are illustrated in Figure 2.

In order to achieve higher spectral efficiency, we introduce a modified double jump filter to FQPSK-X, which, as we can see later, leads to a significant spectral efficiency improvement in non-linear HPA environments.

Double jump filters have been studied and investigated by many researchers for different applications in digital communications systems. Franks first proposed double jump filters, and optimized the roll-off shape for the minimum sensitivity to phase jitter[10]. Tugbay employed DJ filters to obtain the maximum signal energy in a given time interval[11]. Oshita optimized DJ filter for the minimum BER caused by timing and phase errors[12]. In this paper, we modify and apply DJ filters in the DJ-FQPSK system to achieve the highest spectral efficiency in a non-linear channel. A square root DJ filter with very small jump rate factor has been found to be the optimal filter for this application. As compared to conventional DJ filters, this modified DJ filter also provides the least discontinuity which could lead to a simple implementation. The frequency response of the square root DJ filter can be expressed as following.

$$H(f)=\begin{cases} 1 & 0 \le f < f_1 \\ \sqrt{(1-k)-\dfrac{(1-2k)(f-f_1)}{f_2-f_1}} & f_1 \le f < f_2 \\ 0 & f_2 \le f \end{cases} \qquad (1)$$

where $f_1=(1-\alpha)\times f_n$, $f_2=(1+\alpha)\times f_n$, and k is the jump rate factor. Figure 3 presents the spectrum of the square root DJ filters with different k, and compares with that of conventional DJ filters.

After passing through the DJ filters, I, Q channel baseband signals go to the quadrature modulator. The output is DJ-FQPSK modulated signals.

2. Demodulation

DJ-FQPSK signal can be demodulated by a conventional OQPSK demodulator. This is another advantage of this scheme over other similar constant envelope modulation methods

such as TFM, which requires a more complex signal processing approach[13]. Figure 4 is the block diagram of DJ-FQPSK demodulator. For best BER performance, Buttworth BPF or LPF with BTb = 0.55 are recommended. Figure 5 presents the demodulated baseband eye-diagrams.

III. System Performance

1. Spectral efficiency

The power spectral density(PSD) of hardlimited DJ-FQPSK is presented and compared with other modulation techniques in Figure 6. We note that the PSD of DJ-FQPSK is significantly narrower than that of other systems. By selecting different parameters, cross correlation factor A, and DJ filter rol-off factor α, DJ-FQPSK could be optimized for different applications[6].

Spectral efficiency η_f (b/s/Hz) of a digital modulation scheme is defined as $\eta_f = 1 / (WT_b)$, where W is channel spacing and T_b is the one bit duration. In a multi-channel system, normalized channel spacing, WT_b, is usually determined by the maximum acceptable adjacent channel interference (ACI) level. For different applications, there are different definition for the normalized bandwidth WT_b. For example, for wireless LAN's, -20 dB PSD point is the channel spacing, which is the conservative interpretation of FCC regulations. Based on this definition, DJ-FQPSK has a spectrum efficiency of more than 1.5 b/s/Hz, which is 50% higher than GFSK as presented in Table 1.

2. BER Performance

BER performance of DJ-FQPSK is evaluated in a non-linear channel by computer simulations. System parameters, k, α, A, are selected as the same as that to obtain the spectral efficiency of $\eta_f = 1.52\ b/s/Hz$. Coherent detection is used for demodulation as shown in Figure 4. Receiver BPF is 4th order Buttworth BPF with BTb = 0.55.

Figure 7 presents the BER of DJ-FQPSK in AWGN. As compared to the newly standardized GFSK, DJ-FQPSK has about 2.5 dB Eb/No advantages at $P_e = 10^{-5}$, which is obtained

with 50% higher data rate in the same bandwidth. The superior BER performance not only represents higher power efficiency (longer battery life time), but also leads to a shorter data file transfer time/message delay and increased throughput which are the most important issues in wireless LAN's applications.

IV. Conclusion

A power and spectrally efficient DJ-FQPSK system is proposed for wireless LAN's, especially for higher data rate FH/DS spread spectrum applications. The performance of this system including spectral efficiency and BER in a non-linear channel is evaluated. Results show that DJ-FQPSK can provide a higher spectral efficiency as well as a better BER as compared to other modulation schemes.

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Table 1. Performance of DJ-FQPSK

	Spectral efficiency @ -20 dB PSD (b/s/Hz)	Eb/No in AWGN @ 10^{-5}
GFSK	1	19.5 dB
DJ-FQPSK	1.52	17 dB
FQPSK	1.06	11 dB
FQPSK-X	1.08	11 dB

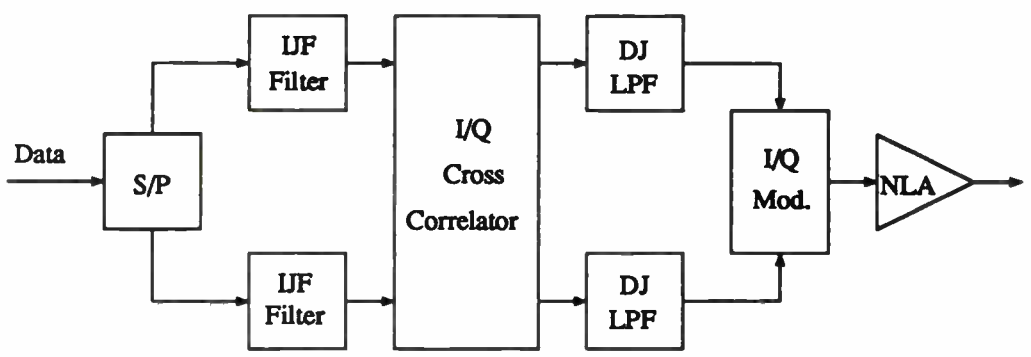


Figure 1. Block Diagram of DJ-FQPSK Modulator

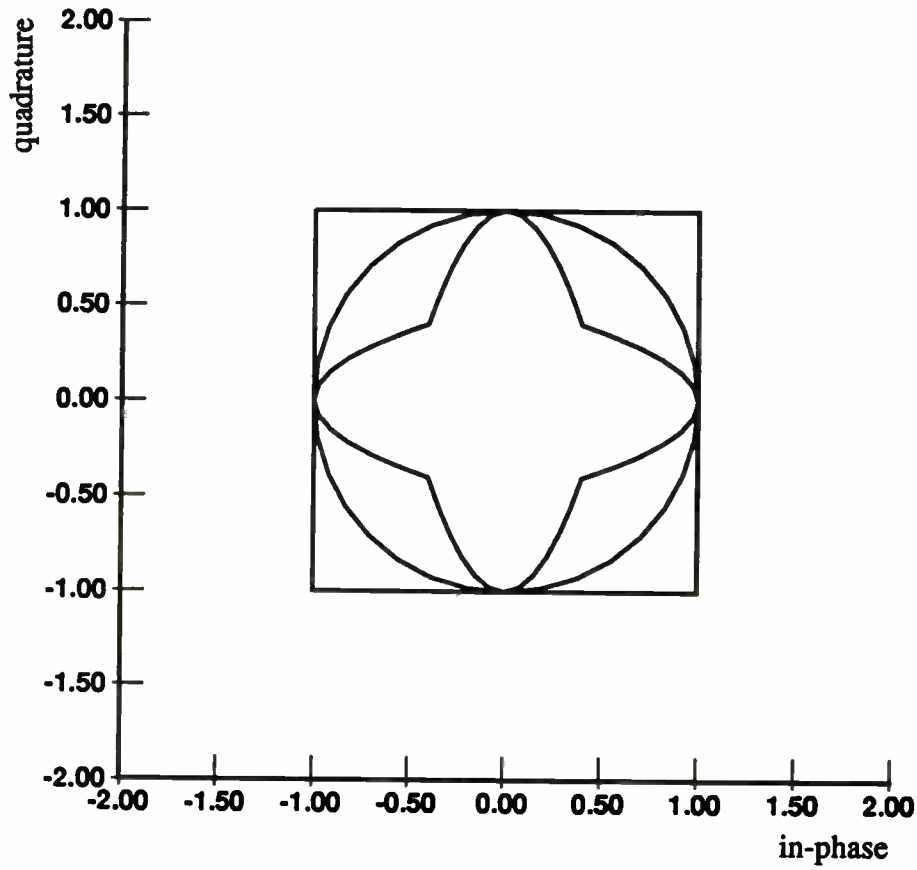
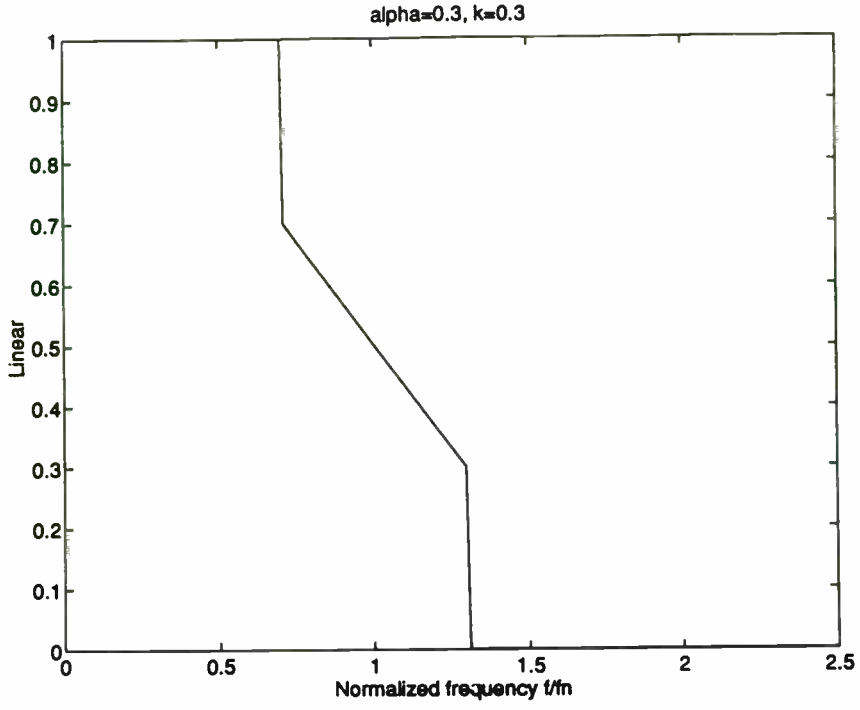
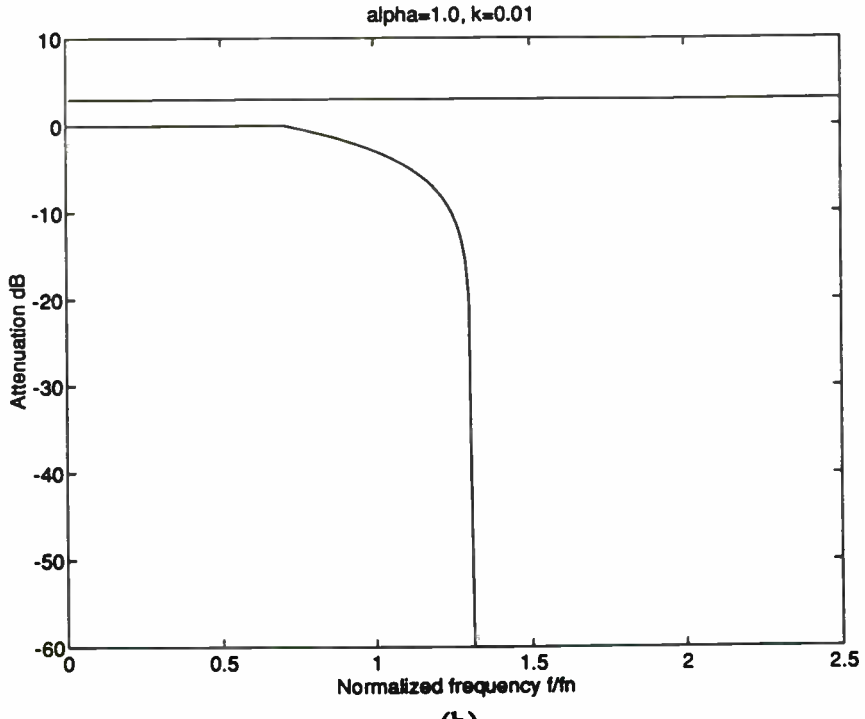


Figure 2. Space Diagrams of FQPSK-X (A=0.4, 0.707, 1)



(a)



(b)

Figure 3. Frequency response of DJ filters. (a). Conventional DJ filter ($\alpha = 0.3$, $k = 0.3$). (b). Modified DJ filter ($\alpha = 0.3$, $k = 0.01$).

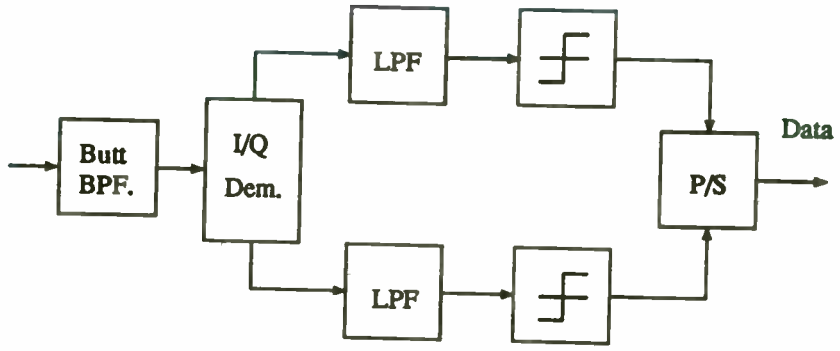


Figure 4. Block Diagram of DJ-FQPSK Demodulator

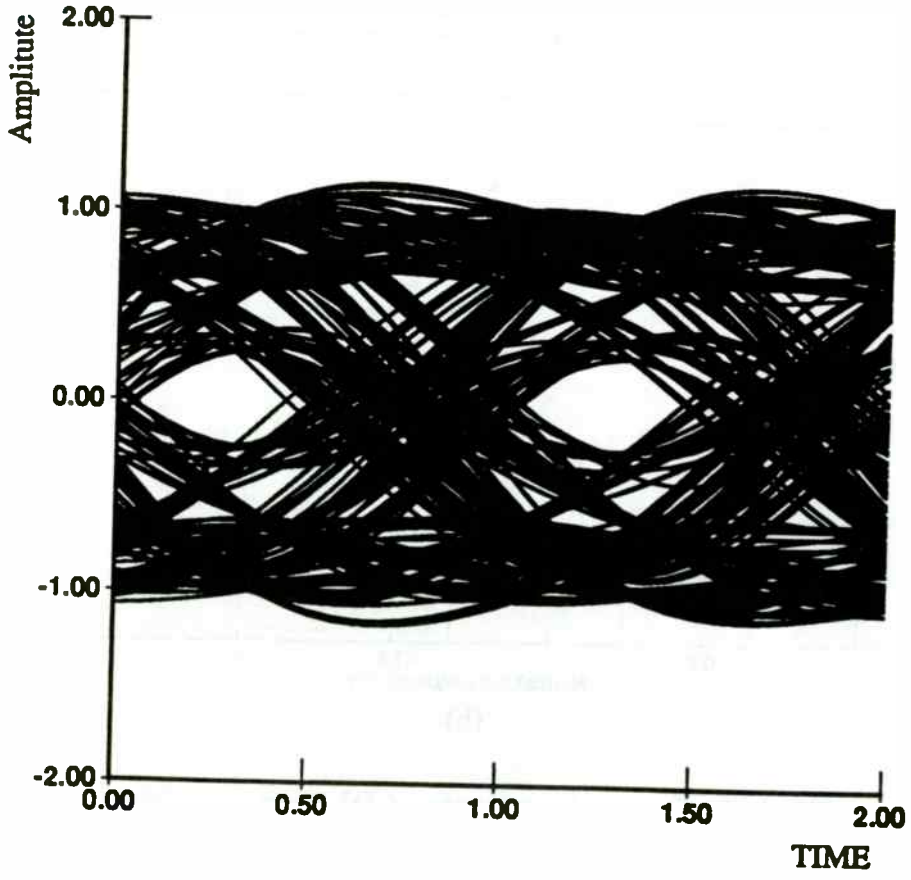


Figure 5. Baseband Eye-diagram of DJ-FQPSK (A=0.4, α=0.3, k=.01, Rx BPF: 4th order Butt., BTb=0.55)

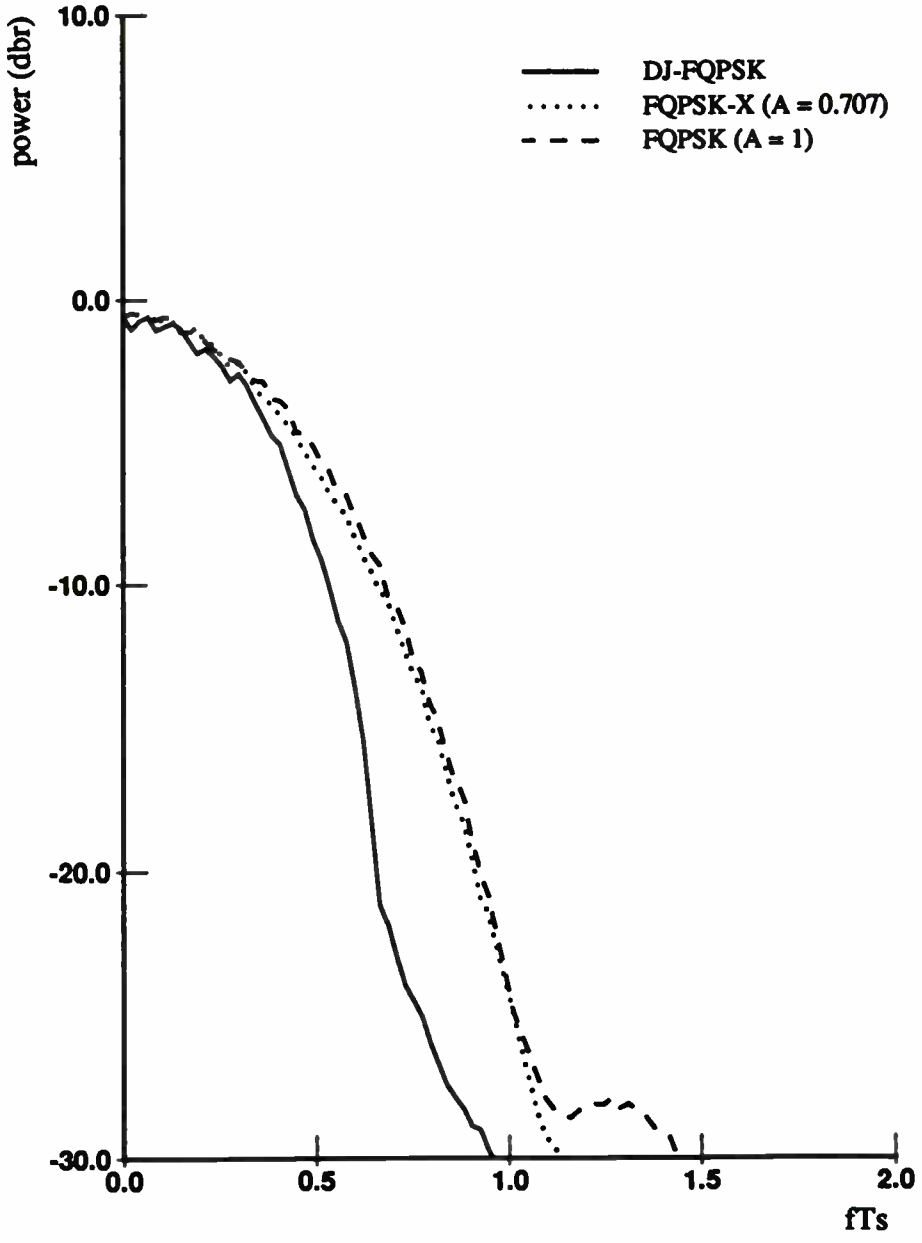


Figure 6. PSD of FQPSK, FQPSK-X, and DJ-FQPSK

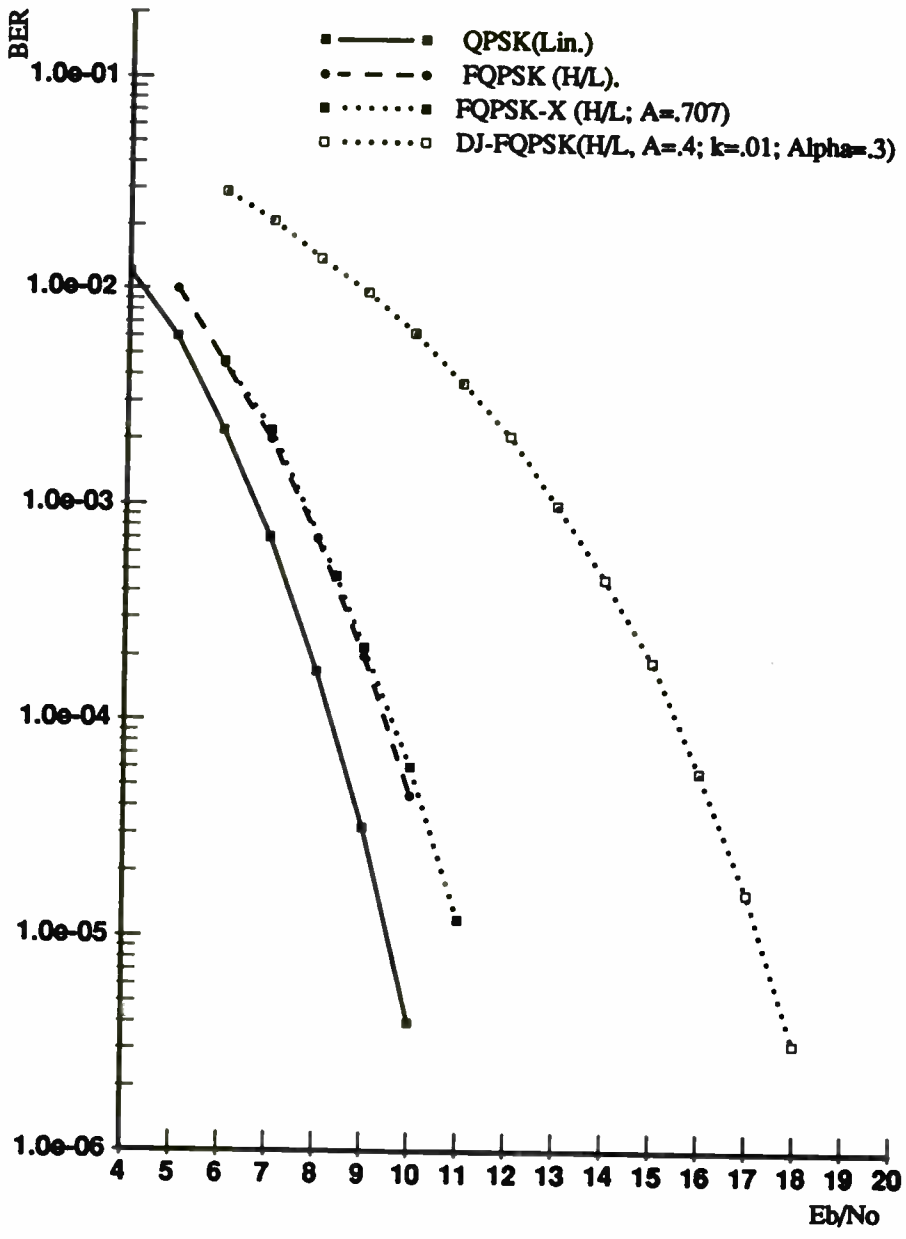


Figure 7. BER of DJ-FQPSK in AWGN. (Rx BPF: 4th order Butt. BTb=0.55)

SURFACE ACOUSTIC WAVE (SAW) DEVICES IN THE DIGITAL WIRELESS MARKETPLACE.

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ABSTRACT
Yearly, the electronics industry uses tens of millions of SAW devices in various applications. These applications are as diverse as the SAW devices themselves. SAW devices are used to enhance the stability of oscillators in transmitters and as front-end filters to set the bandwidth as well as improve intermodulation performance of receivers. Cellular telephone and the Cellular Digital Packet Data (CDPD) industries have benefited from using low-loss, high-rejection SAW filters as intermediate frequency (IF) filters in the receiver stage. SAW devices offer the advantages of compact size, low-loss, stable temperature performance and precision frequency control. This paper will review several types of SAW devices and their applications in the emerging wireless industry.

INTRODUCTION
Since their functional introduction in 1965[1], SAW devices have experienced many modifications and improvements. Resonators, used for frequency and temperature stabilization in oscillators, have increased in frequency and decreased in insertion loss. Circuits that once used high-loss SAW filters (≈ 20 to 40 dB) have been redesigned to use newer SAW filters that exhibit insertion losses in the range of 2 to 10 dB. Many new applications require filters with stringent close-in rejection specifications and require very low insertion losses. These requirements initiated the development of SAW devices with 60 dB rejection as close as ± 1 MHz offset from the center frequency of the device with insertion losses of approximately 3 dB. SAW technology is still in its infancy, therefore new developments seemingly occur daily. Overall tolerances are tighter and prices have dropped, making SAW technology the best choice for many system applications.

SAW DEVICES IN WIRELESS APPLICATIONS
One of the first uses of a SAW device in a wireless application was in the oscillator section of a remote transmitter. This application requires a fundamental mode, high-Q, low-loss, temperature stable, frequency control element. This application is ideal for the SAW resonator. SAW resonators come in two different configurations, the one-port (RO-XXXX) or two-port resonator (RP-XXXX or RS-XXXX). The one-port resonator is the logical selection when a basic oscillator is required. This style resonator offers a low motional resistance (Rm) term, normally 15 to 50 Ω (1.2 to 3.5 dB insertion loss in a 50 Ω system). In most instances, this form of resonator offers the engineer the opportunity to design a stable oscillator that will not require any variable elements. Figure 1 is a one-port SAW resonator circuit used in a simple transmitter application, such as a garage door opener or a medical alert pendant. The resonator is connected between the base of the transistor and circuit ground. The antenna (L1) is normally a printed loop on the PCB. In the 300 to 400 MHz range, this transmitter offers a 30 to 50 meter operating range and a 100 to 250 meter range may be achieved in the 902 to 928 MHz frequency range. With proper circuit design, battery life may be extended to over a year.

The two-port resonator is the preferred choice of designers who desire the ability to pull the oscillators operating center frequency as much as ±250 ppm. The insertion loss of the two-port resonator ranges from 5 to 12 dB, unmatched in a 50 Ω system. However, in a matched condition

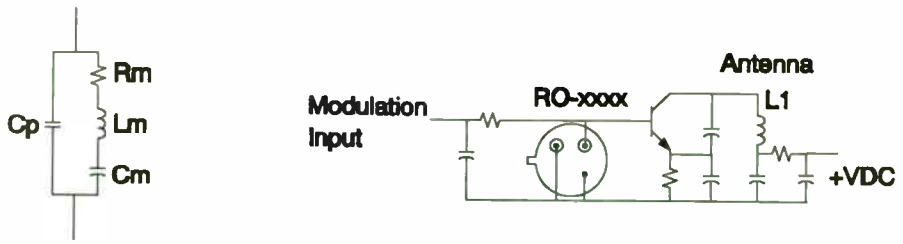

Figure 1
One-port Resonator Equivalent Circuit and use in a Transmitter Application

or an impedance environmentment of approximately 80 to 150 Ω, the resonator loss decreases to 3 dB or less while the 3 dB bandwidth increases a factor of two or greater. A simple two-port SAW resonator oscillator is shown in Figure 2. Two-port SAW oscillators are used as temperature stable, local oscillators for receivers.

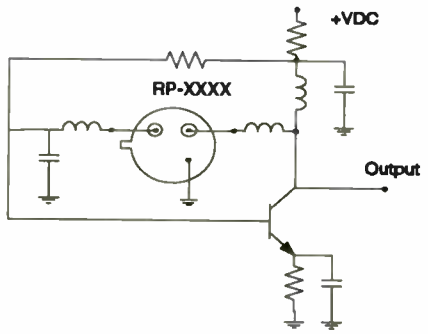

Figure 2
Two-port SAW Resonator Oscillator

The one-port and two-port SAW resonator oscillators require careful PCB layout and component selection to design a competent transmitter that will operate within FCC guidelines. To attempt to simplify the design process, RFM has developed a surface-mount hybrid for local oscillator and transmitter requirements. This product line (HX line) is a surface-mount SAW solution with package dimensions of 0.4 x 0.34 x 0.107 inches. Inside this surface-mount package is a custom IC and two SAW Coupled Resonator (CR) filters. One CR filter and the IC generate the oscillator function[2], while the other CR is in the output line of the oscillator and is used for filtering. This second SAW filter adds additional harmonic suppression which, with a properly designed antenna, achieves compliance to FCC, FTZ and various other governmental specifications concerning the spurious harmonic levels. Utilization of a HX device in a transmitter application is shown in Figure 3. This device requires a power source of 3 VDC and has an output of 0 dBm typical with a 7 mA peak current draw.

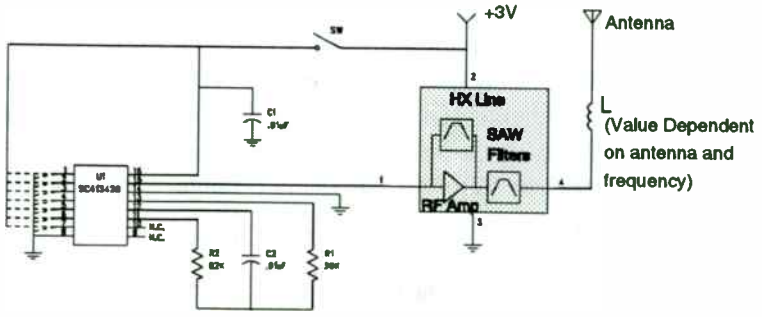

Figure 3
HX Device in a Transmitter Application

TEMPERATURE CONSIDERATIONS

SAW devices provide excellent temperature stability. For this reason alone, they are a correct choice for oscillator applications. The temperature curve is parabolic and repeatable, from wafer to wafer, to within a few degrees Celsius. The center frequency of the SAW device may be accurately calculated at any temperature upon knowing the center frequency of the device at turnover as well as the turnover temperature. The equation for calculating any point on the temperature curve is as follows:

$$Fc_{t(MHz)} = Ft_{0(MHz)} - \left[Ft_{0(MHz)} \left(\frac{T - T_0}{5.6} \right)^2 * 1.0E-06 \right]$$

Where:

$Fc_{t(MHz)}$ is the SAW center frequency in MHz at any selected temperature.

$Ft_{0(MHz)}$ is the turnover frequency in MHz of the SAW device.

T is the current temperature condition of the SAW device.

T_0 is the turnover temperature of the SAW device.

An example of the temperature characteristics of a 300 MHz SAW resonator would be as follows, if the following condition exists:

T = 0.0 °C

T_0 = 50. °C

Ft_0 = 300 MHz

In this example, the Fc_t of the SAW resonator at 0.0 °C would be 299.976 MHz. Using this method, the entire temperature characteristics of the quartz SAW device may be calculated and plotted, as shown in Figure 4.

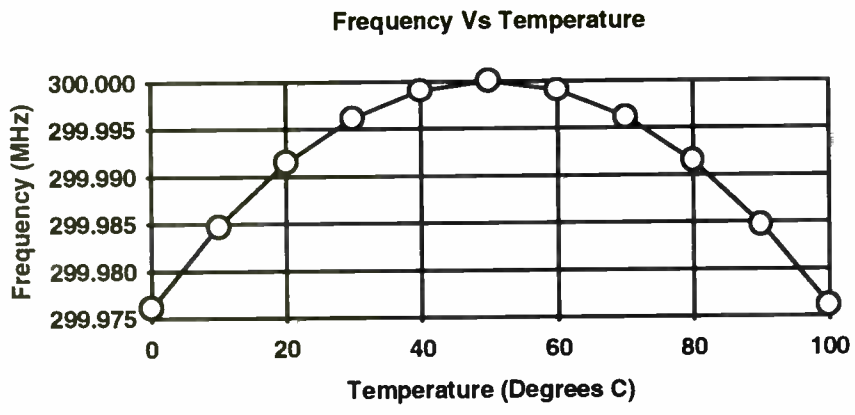

Figure 4
Calculated Temperature Curve

Due to the temperature characteristics of the lumped element components (positive, linear temperature term) in the oscillator circuit and the quartz SAW resonator (parabolic temperature term), the effective turnover of the SAW oscillator circuit decreases by 20°C. This temperature shift may be pre-compensated by notifying the SAW manufacturer that the device is specifically for an oscillator application. The manufacturer will add the required temperature offset to the SAW design to ensure proper centering of the oscillator within the operating temperature range. An example of the pre-compensation would be if the temperature range is -25 to +85°C, then the center of the temperature band is +30°C. In this example, the required turnover temperature of the SAW device would be +50°C to ensure the turnover of the SAW oscillator circuit is at +30°C.

SAW FILTERS AND THEIR APPLICATIONS

SAW filter have been used for many years in the IF stage of receivers. The devices, however, tended to be large, have high insertion loss (≈ 20 to 35 dB) and to be costly. Lower insertion loss devices (≈ 4 to 10 dB) have been available, but require a complex matching network to achieve the lower loss[3]. In spite of the limitations of older SAW devices, they did place a fundamental mode filter precisely on frequency with excellent shape factors. And even with the higher insertion loss or complex matching networks, these devices were desirable to system designers because they were physically smaller and simpler to use than alternative technologies. Over the past fifteen years, the introduction of several new types of SAW devices has solved the limitations cited previously. These new devices are smaller (SMT, TO-39 and 14 pin DIP), have lower insertion loss (≈ 2 to 7 dB) and are inexpensive to manufacture. These SAW filters, known as Coupled-Resonator filters[4], Proximity Coupled Resonator filters[5] and Single-Phase Unidirectional Transducer (SPUDT) filters[6] are used throughout the industry.

Coupled Resonator (CR) filters are two one-pole resonators that are acoustically coupled into a single device. This type of SAW filter can have a fractional bandwidth of 0.03 to 0.25% of center frequency with tuned insertion losses of 2 to 8 dB. Narrow-bandwidth versions of the CR filters may be used without tuning while achieving an insertion loss of 6 dB or less, depending on the impedance environment. As the bandwidth requirement increases, a simple matching network is required to minimize the insertion loss and in-band ripple. Without tuning, the in-band response would resemble an untuned, two-pole helical filter. Although this type of SAW filter does not have the close-in rejection capability of the traditional transversal filters, design techniques have been developed to selectively place nulls in the skirts of the filter response[7]. These nulls may be used to reject the image and LO signals in a single conversion receiver[8] or to provide a reject point as close as 455 kHz away from the passband of the device. CR filters may be manufactured from 10 to above 1500 MHz[9]; however, practical limits are from 200 to 1000 MHz. This form of SAW filter solution is available in SMT, TO-39 and various DIP packages.

Because of the low insertion loss, narrow fractional bandwidth and frequency placement accuracy, the SAW CR filter is well suited as a front-end filter in various receivers. In receiver applications that require 10-to-50 feet of reception, a SAW-based, tuned RF receiver may be used (Figure 6). This form of receiver uses a SAW CR filter between the antenna and a gain stage. The filter sets the receiver bandwidth to 600 kHz nominal, while the gain stage provides +40 to +60 dB of signal amplification. The output of the gain stage is connected to a diode detector that recovers the transmitted information from the amplitude component. Attempting to increase range or sensitivity with additional gain may drive the gain stage into oscillation. This form of receiver may be easily designed and manufactured to over 900 MHz.

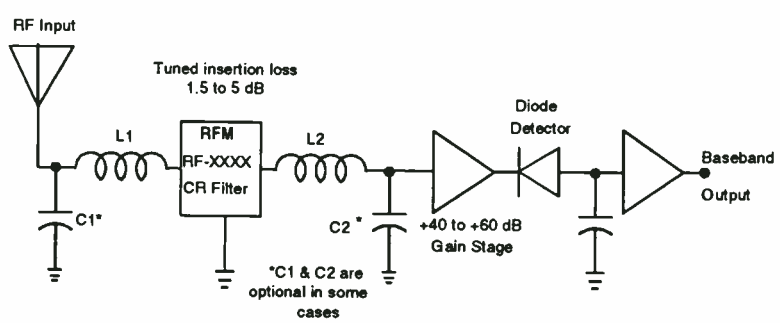

Figure 6
SAW-Based Tuned RF Receiver

For receiver applications that require greater range, one possible choice is a superregenerative (superregen) receiver. The superregen receiver has been an industry staple for many years. Even with the high usage of this receiver, there have been no major changes, other than replacing vacuum tubes with transistors, in over 50 years. Problems, such as frequency drift due to temperature change and component aging, and utilization of LC components to set not only the operating frequency but receiver bandwidth, have plagued engineers since the earliest design of a superregen receiver. Figure 7 is a simplified block diagram of a superregen receiver.

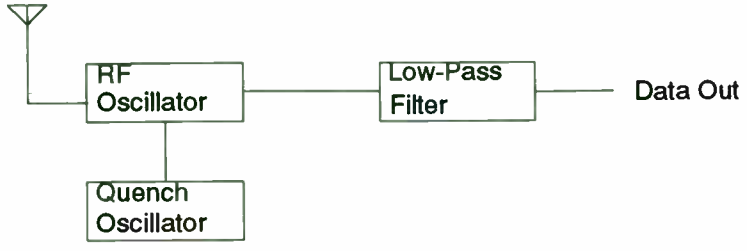

Figure 7
Superregen Receiver Block Diagram

Since the majority of superregen receivers are in the UHF band, engineers have repeatedly tried to use various SAW devices in attempts to alleviate some of the previously mentioned problems. However, SAW resonators were discarded due to the high-Q of the device, which limited the rate of the quench signal; and, conventional SAW delay lines were rejected because of the high insertion loss historically associated with this form of SAW device.

Breakthroughs, however, at RFM have led to the development of a low-loss delay line[10,11] that brought SAW technology into the superregen world. This SAW-based solution eliminates the problems associated with LC components. This low-loss delay line (SL-XXXX) has an insertion loss of 10 to 12 dB and a delay of 150 nsec. The low insertion loss is required to design a quench oscillator using a one-transistor common emitter amplifier with the SAW in the feedback loop. The 150 nsec delay is the shortest practical delay for a SAW device capable of meeting the insertion loss requirement. The delay of 150 nsec suggests a maximum quench rate of 170 kHz (sine wave) but when optimized, offers a quench rate of approximately 56 kHz (trapezoidal)[12]. The SAW-based superregen receiver[13] is an important development because it is capable of matching many of the performance parameters of the superheterodyne (superhet) receiver for low data-rate applications. In particular, the sensitivity of the SAW-based superregen matches that of the more costly and complex superhet receiver technologies. The SAW-based superregen design, which operates at a typical current drain of 550 µA, is a perfect solution for battery powered applications. Additional front-end selectivity may be achieved by using a CR filter to limit the receiver bandwidth to a nominal 600 kHz. Table 1 offers a comparison between SAW-based and traditional superregen receiver circuits. (Additional information on the SAW superregen is available from RFM in Application Note 25.)

Parameter	SAW-Based Superregen	Traditional Superregen
Typical Sensitivity	-100 dBm	-80 dBm
Lab Tuned Sensitivity	-103 dBm	-90 dBm
Sensitivity BW	0.6 MHz	6.0 MHz
Response BW at -50 dBm	2.0 MHz	8.5 MHz
Radiated Spectrum Level	-60 dBm	-60 dBm
10 dB BW of Radiated Spectrum	0.27 MHz	40.0 MHz
Quench Rate	0.045 MHz	0.500 MHz

Table 1
Performance Comparison of SAW and Traditional Superregen Receivers

To compliment other receiver capabilities using SAW devices, a SAW-based superheterodyne (superhet) receiver[14] was developed. This design approach meets the stringent emission requirements outlined under the German FTZ regulation 17TR2100. The basic block diagram of a superhet receiver is shown in Figure 8. Only a cursory outline of the theory of operation of superhet receivers is offered here due to time and space constraints, however, many excellent sources of information are available.[15]

The RF signal is received at the antenna and amplified by the tuned RF gain stage. The signal is heterodyned (translated) down in frequency, using a mixer and local oscillator, to an IF. Typically, the receiver noise bandwidth limit is set by using a filter in the IF stage. The IF is filtered and amplified before being applied to the detector. The detector demodulates the signal and recovers the desired information. To fully restore the transmitted information, a final baseband amplifier is used.

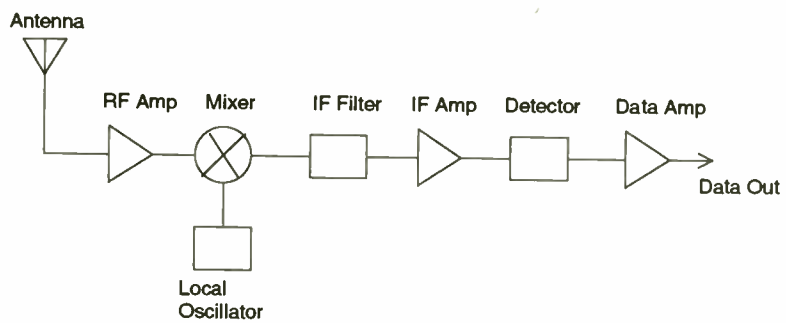

Figure 8
Block Diagram of a Superhet Receiver

There are some distinct advantages to using a superhet receiver. The topology of the receiver places the majority of the signal gain at the IF, where it is simpler to realize and has a reduced potential for instability due to stray feedback paths. The traditional superhet receiver, however, has a disadvantage of being susceptible to spurious frequency responses. The best known and most troublesome spurious response is the image frequency. The image frequency is a signal that, when applied to the mixer, will also create an output at the IF. This response will be processed as if it were the desired signal. Along with this problem, the traditional superhet receivers also use either LC or multiplied crystal stabilized oscillators; but, LC oscillators pose temperature stability difficulties and multiplied crystal oscillators present undue circuit complexity issues.

To solve these problems inherent to the traditional superhet receiver, a SAW-based superhet receiver was developed. RFM's SAW superhet receiver may be operated in either AM or FSK operation. With the jumper connected as shown in Figure 9, the receiver is in FSK mode of operation. A description of the operation of the receiver is as follows:

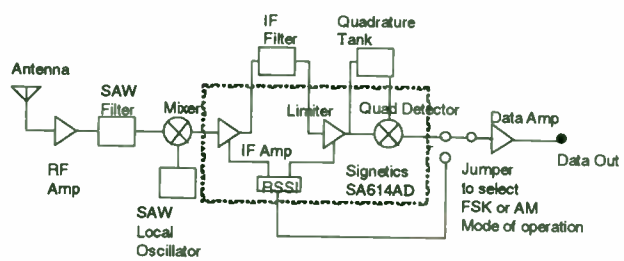

Figure 9
Block Diagram of a SAW based Superhet Receiver

The received signal is applied directly to a low-noise RF amplifier, with a gain of 15 dB and a noise figure of 2 dB. The amplified output is filtered by the CR filter, shown in Figure 10, to limit

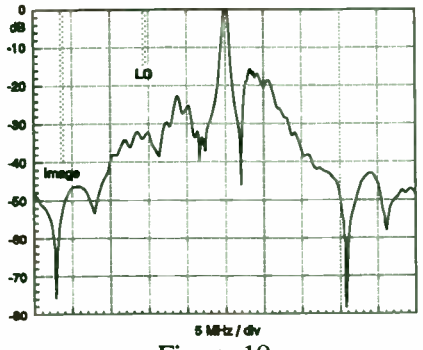

Figure 10
Coupled Resonator Filter at 433.920 MHz (RFM PN RF1172)

the RF spectrum. The CR filter has approximately 3 dB of loss and 650 kHz of bandwidth. The band-limited RF signal is mixed down using a bipolar active mixer with 10 dB of conversion gain. The applied LO is a SAW-stabilized oscillator that is tuned for 10.7 MHz below the nominal receiver center frequency so that an IF of 10.7 MHz is realized. This SAW-stabilized oscillator is relatively simple to implement. It also solves the temperature and complexity issues expressed in the traditional superhet receiver. The IF signal is amplified by the first IF amplifier that has gain of 35 dB. RFM has chosen the Signetics SA614AD low-power IF integrated circuit to provide IF gain and quadrature detection circuitry. Traditionally, in a superhet receiver, a ceramic IF filter is used to set the receiver noise bandwidth and selectivity. Due to the narrow bandwidth of the SAW CR filter used in the front-end, the ceramic filter has been replaced with a simple LC filter with a 3 dB bandwidth of 700 kHz. Thus, the SAW filter sets the receiver noise bandwidth and selectivity, as well as provide rejection of spurious signals such as the image frequency. In this manner, a SAW solution eliminates the traditional superhet problem concerning image signal processing. The output of the IF filter is connected to the limiting amplifier that has approximately 60 dB of gain. The limited signal is applied to both the quadrature tank circuit and the internal frequency comparator of the SA614AD chip. The output of the quadrature tank circuit is applied to the other input of the frequency comparator. This signal is shifted in phase by 90° so that the output of the comparator is a changing voltage that represents the transmitted data. The voltage is applied to the data amplifier where it is amplified, filtered and pulse shaped so that the output levels are CMOS compatible.

Moving the jumper connections to the alternate position will place the receiver in AM mode. As can be seen in Figure 9, the AM mode is identical to FSK mode except for the method of detecting the data. In AM mode of operation, the Receive Signal Strength Indicator (RSSI) circuitry will track the input signal level. As the input amplitude is varied, the voltage present at the RSSI output will also vary. This changing voltage is then processed by the same data amp used in FSK operation.

SAW FILTERS FOR THE CELLULAR MARKET[16]

Virtually all new radiotelephone systems employ digital modulation. From cordless phones to satellite-based radiotelephone systems, digital modulation offers a number of important benefits:

1. It provides excellent voice quality with lower average RF power.
2. It is suitable for both data and voice transmission.
3. It supports TDMA and CDMA channel sharing techniques.
4. Transmissions may be encrypted for security.

The RF circuitry of a digital radiotelephone is simpler than its analog counterpart. For example, an analog cordless phone must use a duplexer filter to allow the transmitter and receiver to operate simultaneously from one antenna. In contrast, CT-2 and DECT digital cordless phones use time division duplexing, eliminating the need for a duplex filter.

DIGITAL RADIOTELEPHONE RECEIVER IF FILTER REQUIREMENTS

Digital radiotelephones can achieve good performance on received signal-to-noise ratios of 8 to 12 dB. However, they are sensitive to pulse ringing on the desired signal. This can create intersymbol interference (ISI). Group-delay variations in the passband of the IF filter can be a major contributor to ISI. Consequently, group-delay deviation (GDD) limits on IF filters for digital radiotelephones are much tighter than for analog radiotelephones.

The first IF frequency of most radiotelephones is in the range of 70 to 250 MHz. The second IF frequency is typically between dc (zero IF) and several megahertz. The first IF must provide image rejection for the second IF and protect the second IF from 3rd-order intermodulation distortion, blocking, etc. Minimizing GDD is generally more important in the first IF of a digital radiotelephone than high adjacent-channel rejection.

Depending on the standard, a digital radiotelephone signal will occupy 1 to 25 times the bandwidth of a NBFM analog signal. Consequently, a range of IF filter bandwidths is required to cover all digital radiotelephone requirements.

Radiotelephone packaging requirements place a premium on small filter size. This also extends to the matching components used with the filter. For handheld radiotelephones, SMT filter packaging is generally a requirement. In service, radiotelephone IF filters must tolerate the shock of a phone being dropped, plus the temperature range found in an automotive installation.

SAW FILTERS FOR DIGITAL RADIOTELEPHONE IF APPLICATIONS

RFM offers four types of SAW filters for digital radiotelephone IF applications, Proximity Coupled, Coupled Resonator, Low-Loss Transversal and the Precision Transversal Filters. The basic characteristics and applications of each filter type are discussed below:

Proximity Coupled Resonator Filters (PX, shown in Figure 11) are narrow-band SAW filters designed for IS-54 (NADC) and CT-2 digital radiotelephone IF filter requirements. Digital pagers and analog cellular systems, including AMPS, TACS and NMT, use PX filters extensively. PX filters are usually designed on quartz with fractional bandwidths ranging from 0.05 to 0.075%. These filters exhibit excellent close-in rejection, achieving shape factors around 2.5:1.

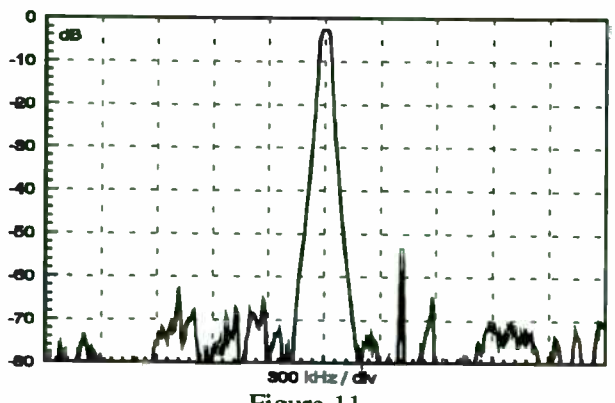

Figure 11
Proximity Coupled Resonator Filter

Coupled Resonator filters (CR, refer to Figure 10) are used in air-to-ground radiotelephone systems and in U.S. 915 MHz cordless telephone handsets. They may be designed with fractional bandwidths ranging from 0.03 to 0.25% of their center frequency. CR filters offer broader bandwidth capabilities than the PX style of filter while also offering the unique capability of accurately placing nulls in the skirt of the filter to provide selective rejection of problem frequencies.

Low-loss Transversal filters (SF, shown in Figure 12) are ideal for GSM, PCN, DECT and Inmarsat radiotelephone applications. RFM's SF filters are pre-compensated to provide very flat group delay[15] across the filter passband. As a result, these filters exhibit very low ISI distortion and are relatively insensitive to source and load mismatches. RFM SF filters can be designed with fractional bandwidths ranging from 0.25 to 2%, depending on the substrate used.

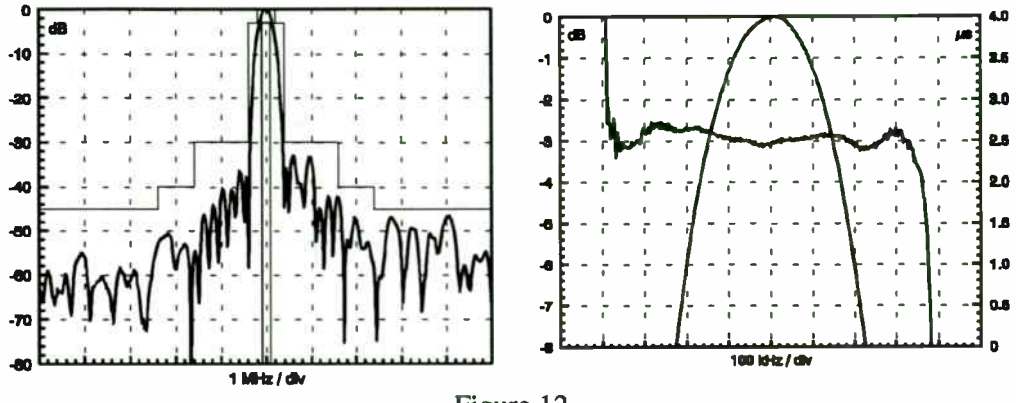

Figure 12
Low-loss Transversal Filter

Precision Transversal filters (BP, shown in Figure 13) are frequently used in CDMA (spread spectrum) radiotelephone applications. Although BP filters exhibit relatively high-loss, this form of filter provides excellent amplitude and group-delay flatness for fractional bandwidths of 10% or more. This makes them the best choice for IF filtering of uncorrelated spread spectrum signals and other very high data-rate transmissions.

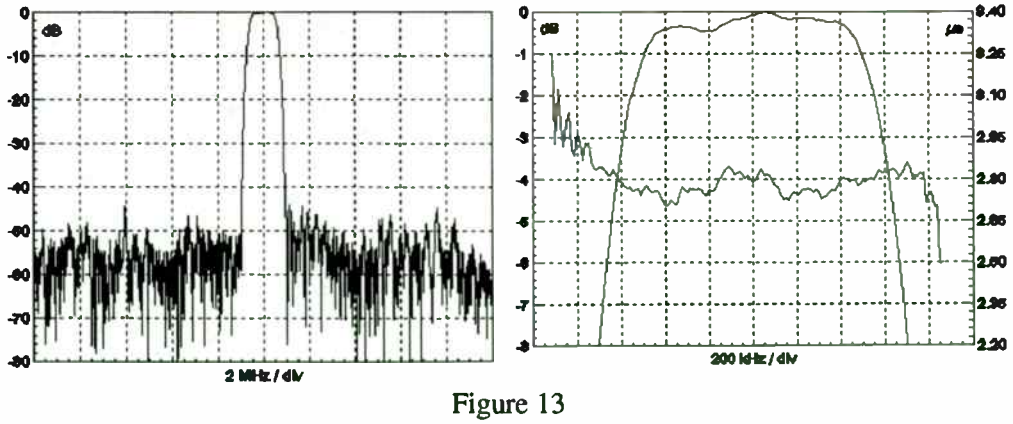

Figure 13
Precision Transversal Filter

The general performance characteristics of the SAW filters discussed above are shown in Table 2. Table 3 summarizes the digital radiotelephone system information.

SAW Filter Type	Substrate Material	Center Frequency	Fractional Bandwidth	Insertion Loss	GDD 1 dB Bw	3:30 dB Shape Factor	Ultimate Rejection	Temp Drift -25 to 85° C	Digital Radiotelephone IF Applications
Proximity Coupled	Quartz	70 - 500 MHz	0.05 - 0.075 %	1.50 - 4.00 dB	6.0µs @ 90 MHz	1:2.50	65 - 70 dB	0.025 %	NADC, CT-2
Coupled Resonator	Quartz	70 - 950 MHz	0.03 - 0.25 %	2.00 - 8.00 dB	3.0µs @ 90 MHz	Image Reject Notch	50 - 60 dB	0.025 %	Aircraft, US 916 MHz Cordless Phones
Low-Loss Transversal	Quartz	70 - 300 MHz	0.25 - 0.75 %	4.00 to 10.0 dB	0.3µs @ 71 MHz	1:2.75	45 - 55 dB	0.025 %	GSM, PCN, Inmarsat
Low-Loss Transversal	Lithium Tantalate	70 - 300 MHz	0.75 - 2.0 %	3.00 - 9.00 dB	0.2µs @ 110 MHz	1:2.50	40 - 50 dB	0.200 %	DECT
Precision Transversal	Quartz	70 - 650 MHz	0.25 - 0.75 %	18.0 - 23.0 dB	0.2µs @ 71 MHz	1:2.00	45 - 55 dB	0.025 %	CDMA Cellular, GSM, PCN Base
Precision Transversal	Lithium Tantalate	70 - 650 MHz	0.75 -2.0 %	18.0 - 23.0 dB	0.1µs @ 70 MHz	1:1.50	40 - 50 dB	0.200 %	DECT Base
Precision Transversal	Lithium Niobate	70 - 650 MHz	2.0 - 10.0 %	23.0 - 30.0 dB	0.1µs @ 70 MHz	1:1.30	45 - 55 dB	0.825 %	CDMA Base

Table 2
Typical SAW Filter Specifications and Capabilities

System	Geographic Regions	Multiple Access Techniques	Modulation Type	Transmitted Data Rate	Channel Spacing	Standard RFM Filter	Filter Package
NADC (IS-54)	US / Canada	TDMA	π/4 DQPSK	48.6 kbps	30 kHz	PX1001 83.16 MHz	SMT 13.3 x 6.5 mm
CDMA	US	CDMA	Spread Spectrum	1.2288 Mbps	N/A	BP1024 70.00 MHz	DIP 22.5 x 13.0 mm
GSM / PCN	European Pacific Rim	TDMA	0.3 GMSK	270.833 kbps	200 kHz	SF1041 71.00 MHz	DIP 21.0 x 13.0 mm
CT-2	UK / Hong Kong	TDMA/TDD	0.5 GMSK	72 kbps	100 kHz	PX1003 150.0 MHz	SMT 9.10 x 7.1 mm
DECT	Europe	TDMA/TDD	0.5 GMSK	1.152 Mbps	1.728 MHz	SF1045 110.0 MHz	SMT 13.3 x 6.5 mm

Table 3
Digital Radiotelephone Systems

CONCLUSIONS

In the twenty-nine years since the introduction of SAW devices, many technological advancements have occurred to make SAW products a first choice component in wireless design. The advantages of SAW-based transmitters are obvious over competing technologies, while SAW filters continue to improve and modify to meet the needs of this dynamic marketplace. SAW resonator and filter requirements are in constant flux to meet the demands of the Wireless industry. This symbiotic relationship will continue to drive the two industries to develop new ideas and products.

ACKNOWLEDGMENTS

The author wishes to acknowledge Drs. Peter Wright and Ben Abbott for the continued innovations they bring to the field of SAW technology. Thanks are also in order for Darrell Ash, Earl Clark and Frank Perkins for the excellent sources of information they provided. Special appreciation is offered to the people who build the parts on the manufacturing line, support people and secretaries because you are the backbone of RFM. Your work and support provide me with the time and documentation necessary to detail and describe our technology and products. Finally, I want to thank Christina McFarland for surviving the many arduous editing sessions. Thank you all. I couldn't have completed this without you.

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Computer-Aided Engineering, II

Session Chairperson: Alan ("Pete") Conrad,
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Simulating oscillator phase noise

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Introduction

Phase noise is one of the most important specifications for oscillator design. This article describes a new technology for simulating oscillator phase noise, and discusses some of the details that a designer must include to simulate phase noise. We cover how the HP Microwave Design System (HP MDS) does the analyses, what the designer needs to include in each simulation, and how to do the simulations.

Phase noise basics

Ideally, a signal displayed on a spectrum analyzer would appear as a single vertical spike at the oscillation frequency. However, noise skirts (sidebands) appear around the signal because the signal's frequency varies with time due to phase noise. Phase noise is analyzed theoretically by assuming that the signal is stable and that the noise skirts are due to phase modulation of the signal. The phase noise of an oscillator is usually quantified by its single-sideband (SSB) phase noise, which is defined as the ratio of noise power in a 1 Hz bandwidth at an offset, f_m, to the signal power (or carrier power), as shown in Figure 1.

A signal at nominal frequency f_0, with phase modulation at a rate, f_m, can be described by the following equation:

$$v(t)=V_s \cos(2\pi f_0 t + \Delta\Phi_{peak} \sin(2\pi f_m t))$$

This equation describes a signal with the spectrum shown in Figure 2. HP MDS computes the amplitude of the noise sidebands (V_{ssb}, in Figure 2) at each offset frequency, f_m. The phase noise can then be computed as the ratio of this sideband power to the signal power, and plotted versus offset frequency, f_m.

References [1], [2], and [3] have more detailed information on phase noise theory and phase noise measurements.

How does HP MDS compute oscillator phase noise?

HP MDS computes oscillator phase noise by first doing a harmonic balance analysis to solve for the frequency of oscillation and the amplitude of the signal at the output specified by the user. All phase noise comes from the various noise sources in a circuit, for example, thermal noise from resistors and lossy elements, and shot, 1/f, and burst noise from BJTs. Any noise source from an active device model, or that the user adds to the circuit, will contribute to phase noise.

Noise sources contribute to phase noise via two mechanisms. One is direct up conversion of noise from baseband to the oscillation frequency due to the nonlinear effects in the circuit. Via this mechanism, thermal noise contributes white noise around the output signal, and 1/f noise sources contribute a 1/f noise spectrum around the output signal. The other mechanism is due to the same noise sources actually varying the frequency of oscillation. To compute the contribution from this effect, HP MDS computes the derivative of the oscillation frequency with respect to the amplitude of each noise source. From these derivatives, the mean square frequency noise contributed by each noise source is computed. This mean square frequency noise is then converted to phase noise (since phase is the integral of frequency, frequency noise in the frequency domain can be converted to phase noise in the frequency domain by multiplying by $1/f_m^2$ using Fourier transform theory). The equations are shown in Figure 3. Noise sources with white frequency spectra contribute $1/f^2$ phase noise spectra. Noise sources with 1/f frequency spectra contribute $1/f^3$ phase noise spectra. These noise calculations are carried out for each noise source and added independently.

Modeling requirements for accurate phase noise simulations

Accurate phase noise simulation starts with accurate oscillator simulation. A good nonlinear model for the active device(s) and a model for the resonator (or frequency-selecting element), as well as accurate models for the other passive circuit elements are required. In addition, it is necessary to model the 1/f noise of the active device. Several considerations for low phase noise design are:

* 1/f noise of the active device(s)
* Resonator 1/f noise or residual phase noise (in some cases)
* Resonator Q
* Circuit design such that the frequency of oscillation is the same as the resonator's center frequency

Resonator simulation

Generally speaking, the higher the Q of a resonator, the lower the oscillator phase noise. For simulation purposes, the designer must obtain an equivalent circuit or use measured data. Crystal resonator manufacturers usually supply an equivalent circuit model. For oscillators using an LC type resonator, it is important to have good models for the actual circuit elements that will be used. These models can be derived from measurements with a network analyzer, or from libraries such as the HP 85174A RF SMT Library. If axially leaded parts are used at RF frequencies, it is wise to measure their impedance versus frequency to derive an equivalent model, rather than just using their nominal values in a simulation. For dielectric resonators, equations are available for the equivalent circuit elements. These can be used as a first approximation, but again, measurements may be necessary. YIG resonators are commonly used in broadband, tunable microwave oscillators, and equations are also available to describe equivalent circuits based on sphere sizes and coupling geometries. However, it is often necessary to measure these resonators and derive an equivalent circuit. Other resonator elements include varactor diodes and microstrip transmission lines. References [4] and [5] provide information for deriving equivalent circuit models.

Circuit analysis for optimum phase noise

Oscillator circuits can be analyzed qualitatively to see if they are designed for optimum phase noise performance. In low phase noise oscillators, a high-Q resonator is used to select the frequency of oscillation. To minimize the oscillator phase noise, the frequency of oscillation should be the same as the resonator's center frequency. The resonator's derivative of phase with respect to frequency will be a maximum at the center frequency, and consequently the resonator will have its highest Q.

This condition will only be achieved if the circuit is designed so that there is no excess phase shift generated by the circuit, excluding the resonator. To accurately model the phase characteristic of the circuit, excluding the resonator, it is necessary to model the components accurately, including transmission line lengths.

Figure 4 shows a simplified feedback oscillator with a crystal resonator equivalent circuit.

The following describes how the circuit in Figure 4 can be analyzed for optimum phase noise performance. First, the circuit is broken into two parts: the resonator, which determines the frequency of oscillation, and the active circuit, which amplifies the oscillating signal. The limiting mechanism of the active circuit determines the amplitude of oscillation. Two simulations are done, 1) a simulation of the large-signal impedance of the active circuit seen by the resonator at the resonant frequency, and 2) a simulation of the resonator's impedance versus frequency.

In Figure 5a, the resonator is replaced with a large-signal current source, and the large-signal impedance seen by the resonator is simulated at the resonant frequency, as a function of current source amplitude. The impedance of the resonator as a function of frequency is also simulated, as shown in Figure 5b.

At the frequency and current amplitude where the sum of the two impedances is 0, the steady-state oscillation conditions are satisfied:

$$Z_{res}(f)+Z_{\text{active circuit}}(\text{amplitude})=0$$

If this occurs at the center frequency of the resonator, as shown in Figure 6, and the impedance trajectories intersect at a right angle, then the oscillator's phase noise should be optimum (for the particular device and resonator being used).

If the two impedance trajectories do not intersect at the resonator's resonant frequency, then circuit element values can be adjusted to improve the design.

Device 1/f noise

Perhaps the most critical thing to model when simulating oscillator phase noise is the 1/f noise of the active device(s). Unfortunately, device manufacturers do not supply 1/f noise parameters or models for their devices. Currently, the only way for a designer to model 1/f noise is to measure it.

Most low-frequency or RF oscillators use bipolar junction transistors (BJTs) as the active device. A commonly used BJT noise model is shown in Figure 7. In most cases the base current shot and 1/f (flicker) noise sources dominate the noise at the output. This noise model is implemented in HP MDS. The shot noise depends only on the DC currents flowing in the device, and is computed automatically. Thermal noise due to various device resistances and all lossy circuit elements is also computed automatically. To include flicker and burst noise in a simulation, it is necessary for the designer to input values for the flicker and burst noise coefficients:

K_f, A_f, K_B, A_B, and f_B, in Figure 7.

These coefficients can be derived by making measurements using the block diagram shown in Figure 8. The objective is to bias the device without adding any noise, and to provide an input impedance large enough to force the base current noise to go through r_π, which causes it to appear at the output where it is measured by the spectrum analyzer. The noise at the output might typically be measured from 10 Hz to 1 MHz or until the device's noise floor is reached. Because of the presence of large spurious signals in this frequency range (especially 60 Hz and its harmonics), shielding the test system may be necessary. We have used a battery to avoid 60 Hz noise that might appear on the signal from AC power supplies.

From a derivation by Motorola (to be published soon), the noise at the output will be dominated by the base current shot and flicker noise, assuming the burst noise is neglected. The output noise spectrum of the BJT will have a corner frequency, f_c, at which the base current shot and flicker noise contributions are equal. There is a linear equation that can be formulated which relates the two unknowns, K_f and A_f, and the two measured parameters, the base current and the noise corner frequency, f_c.

MESFETs can be measured using a set-up similar to that described above for BJTs, except that setting the input resistance to the device equal to 50 ohms (or a value it will see in actual operation) is better.

If a designer is using a nonstandard device, or is modeling a device using the HP Root Model, the 1/f noise can be measured using a set-up similar to that used for BJTs as described above. Noise current and voltage generators can be used at the input or output to model the measured output noise spectrum. Figure 9a shows the measured equivalent input noise voltage spectrum for a MODFET device developed by Hewlett-Packard. Figure 9b shows the equations that were used to generate the equivalent input noise voltage source. These equations were generated via curve fitting. This device is used in an example, which is described later in this article.

Modeling Resonator Phase Noise

Measurement techniques

Some resonators (SAW and crystal) add phase noise to signals that pass through them. The added phase noise can be measured using residual phase noise measurement techniques described in [2] and [3]. Good correlation between the phase noise of measured SAW resonators and the oscillators into which they are assembled is described in [6].

The measurement set-up described in [6] is shown in Figure 10, and is described here.

A signal source (typically an HP 8662A or a different source, depending on the frequency) is split, with one signal passing through the resonator under test, and the other signal passing through a variable delay line. The output from the variable delay line becomes the L input to the HP 3048A phase noise measurement system, and the output from the resonator under test becomes the R input. The variable delay line is adjusted until the signals at the input to the HP 3048A are 90 degrees out of phase. In this condition, the HP 3048A will detect phase differences (phase noise) between the two signals as a function of offset frequency from the carrier. Crystal resonators can be measured using a similar technique. These measurements require care to prevent mechanically induced phase fluctuations, and the components may require RFI (radio frequency interference) shielding.

Modeling the noise

Using the symbolically defined device (SDD, reference [7]) in HP MDS, it is possible to construct a component that adds phase noise to a resonator. There are at least two ways of modeling resonator phase noise in an oscillator. One is to add a component that adds phase shift to a signal, with the amount of phase shift dependent on a control voltage. If the control voltage is a noise source with a $1/\sqrt{f_{offset}}$ spectrum, where f_{offset} is the frequency offset from the fundamental, then resonator 1/f phase noise can be modeled.

This implements 1/f phase noise. Another approach is to use an SDD to implement 1/f frequency noise. If a resonator is modeled with a series RLC circuit, the resonant frequency can be shifted slightly by adding, for example, a small capacitor in parallel with the resonator's series resonant capacitor. See Figure 11.

If we assume that the frequency of oscillation is the same as the resonator's resonant frequency, then changes in ΔC also change the frequency of oscillation, which models frequency noise. If ΔC is a voltage-dependent capacitor, where the control voltage is a noise voltage source, then the noise voltage can be related to frequency noise and, consequently, phase noise.

Details concerning these two methods are included in reference [8].

Oscillator Phase Noise Simulation Example

Recently Hewlett-Packard developed a new YIG oscillator to be used in test instrumentation (see reference [9]). During the oscillator's development, this phase noise simulation capability was not available. We used this oscillator to see how accurately phase noise can be simulated.

In order to carry out the simulation, we had to derive an equivalent circuit model for the YIG resonator. This is a parallel RLC circuit with transmission lines to model the coupling loop effects, and the L and C are functions of the resonator's resonant frequency. We also extracted an HP Root Model for the active devices (MODFETs), and we derived an equivalent input noise voltage source to model the low frequency noise of the device.

The simulation and measurement results are shown in Figure 12. There is good agreement of the results, except at 1 KHz. The deviation could be due to noise sources that we are not modeling, such as current noise in the DC current that is required to generate the magnetic field, which biases the YIG.

Conclusion

This article has discussed the basics of phase noise analysis and how HP MDS simulates phase noise. It has also covered how to do some of the modeling required to do accurate phase noise simulation. The following references provide more detailed information.

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$$L(f_m) = \frac{\text{noise power in a 1 Hz bandwidth at offset } f_m \text{ from carrier}}{\text{carrier power}}$$

Spectrum Analyzer Display

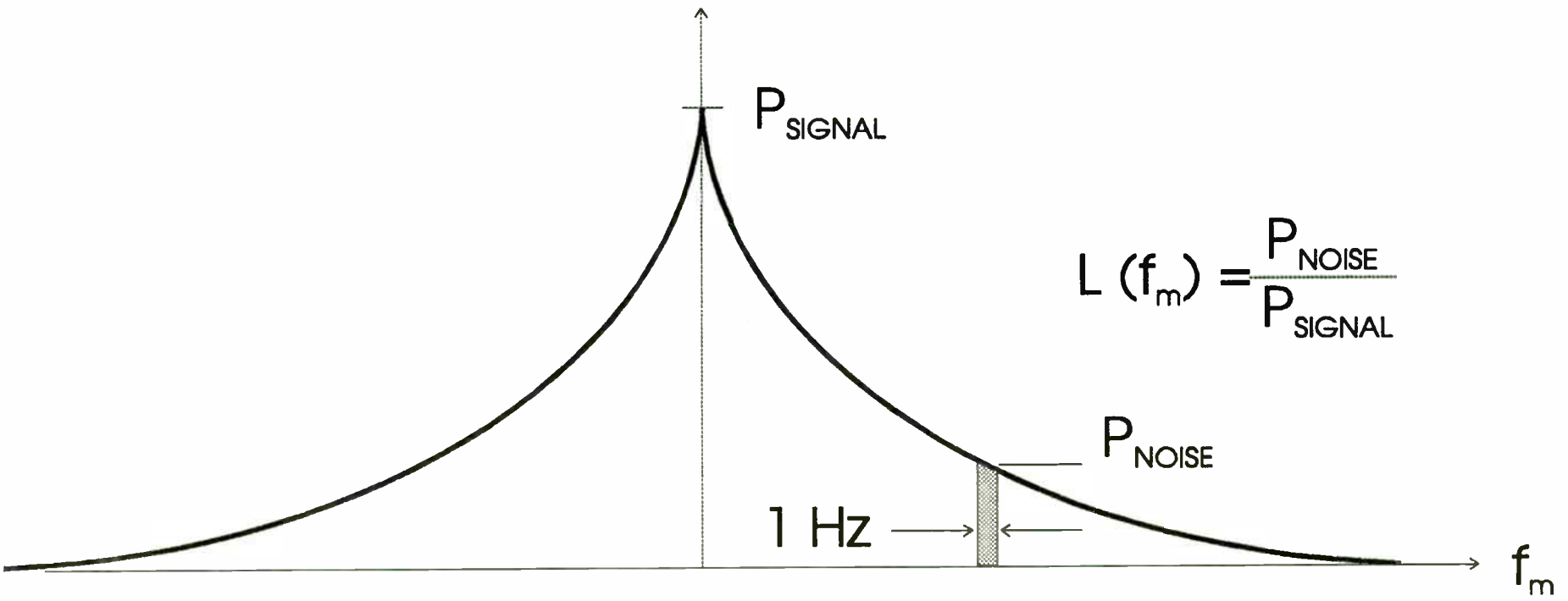


Figure 1: Definition of single-sideband (SSB) phase noise.

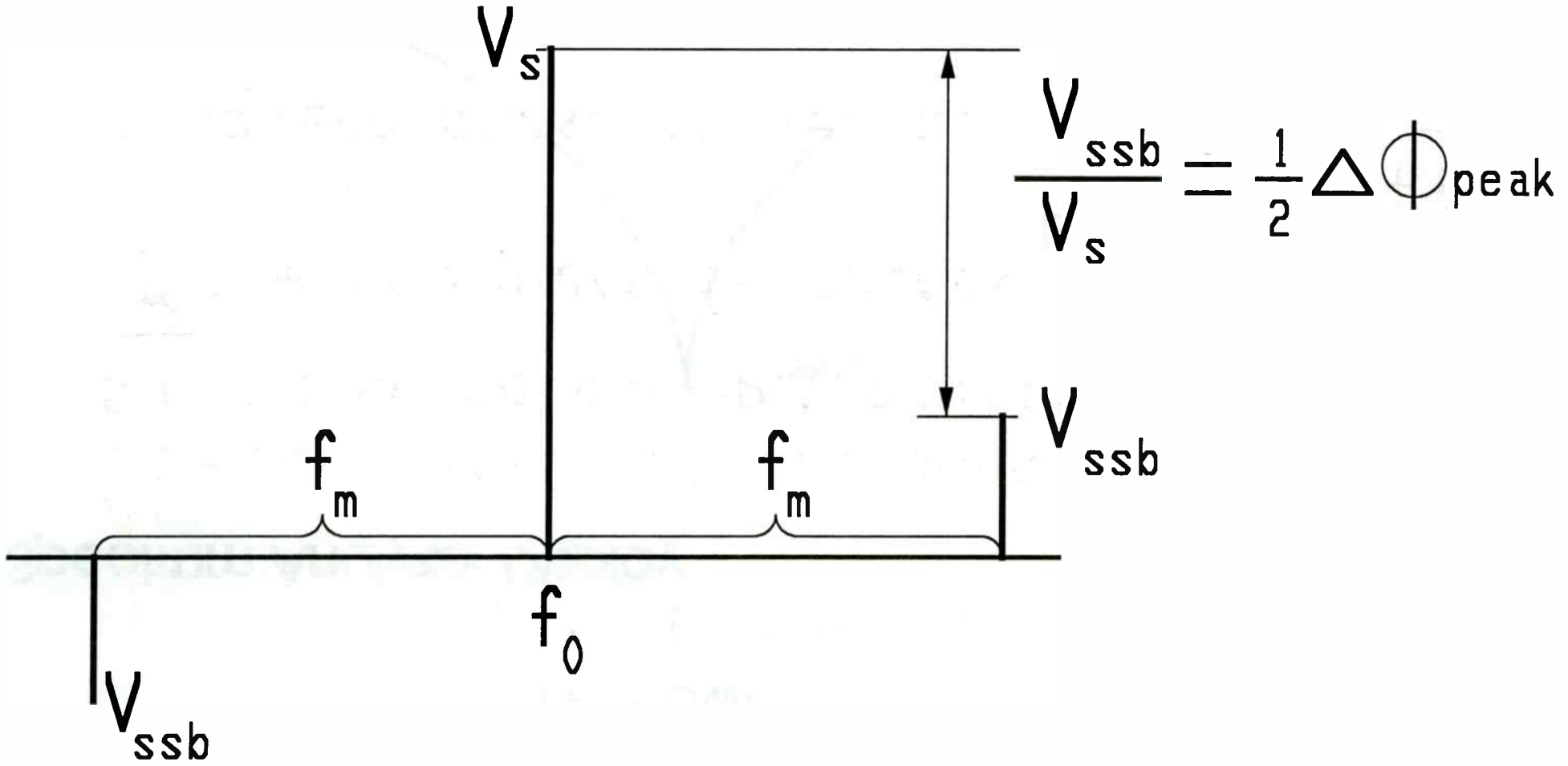


Figure 2: Spectrum of signal with phase modulation.

$$\overline{f^2} = \frac{df}{di}\,\overline{i^2}\,\frac{df}{di}$$

$\overline{i^2}$ = mean square current noise

$\frac{df}{di}$ = derivative of frequency with respect to noise current amplitude

$\overline{f^2}$ = mean square frequency noise

Mean square phase noise is: $\overline{\phi^2(f_m)} = \frac{\overline{f^2(f_m)}}{f_m^2}$

f_m = frequency offset from carrier

Figure 3: How noise sources cause random frequency fluctuations and phase noise.

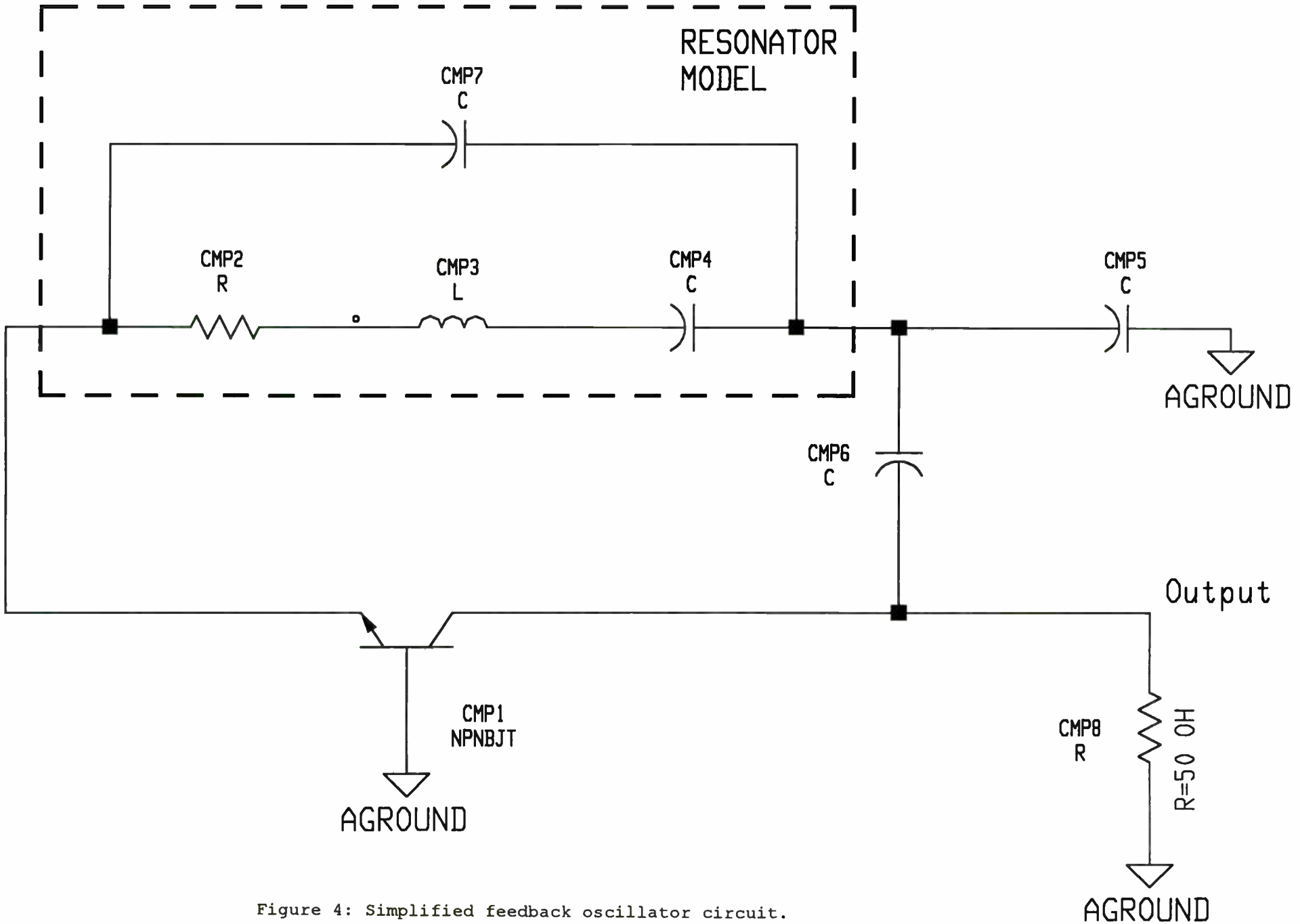


Figure 4: Simplified feedback oscillator circuit.

Large-signal impedance seen by resonator:

$$Z_{\text{active circuit}} = \frac{V_{plus} - V_{minus}}{I}$$

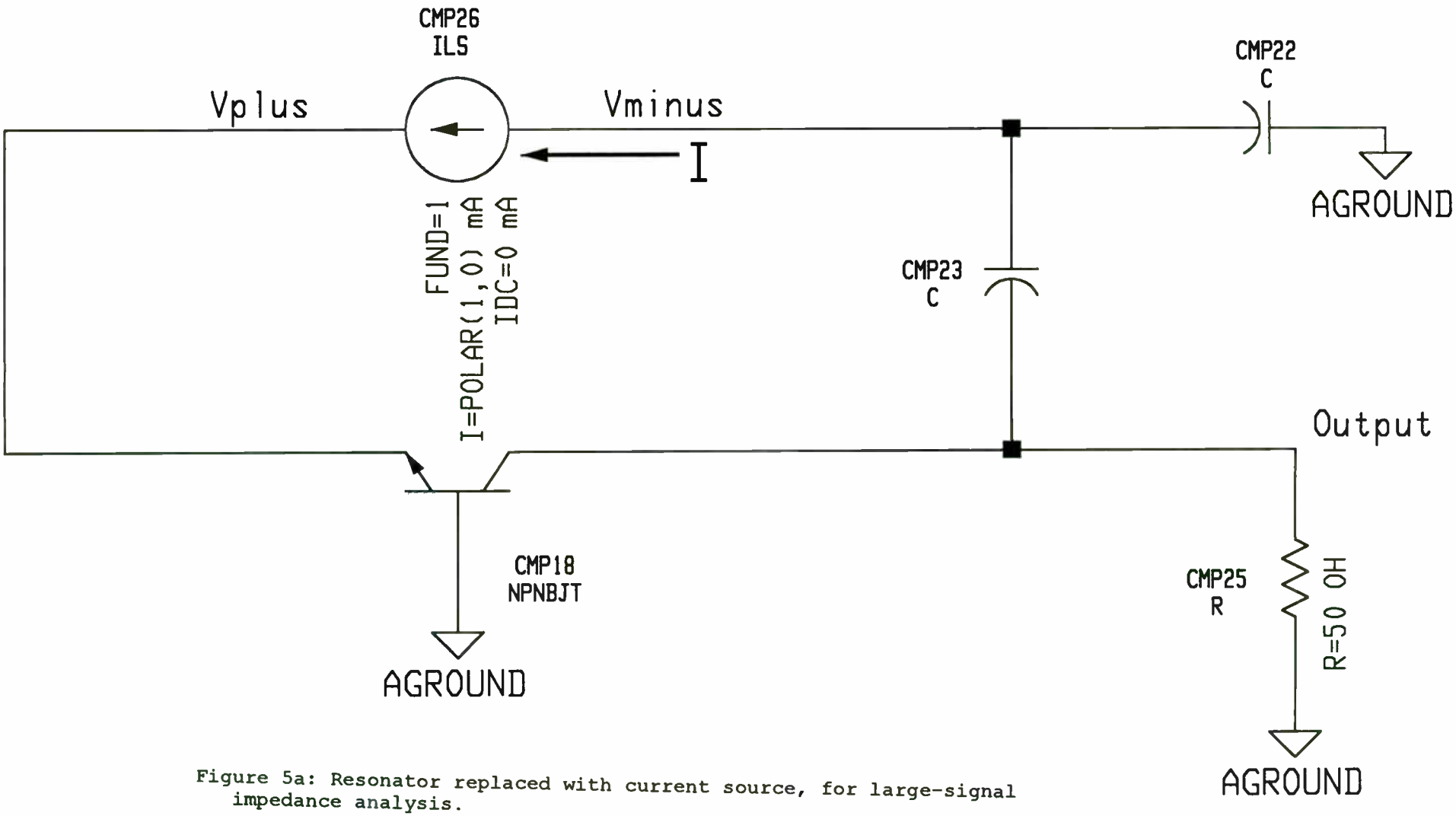
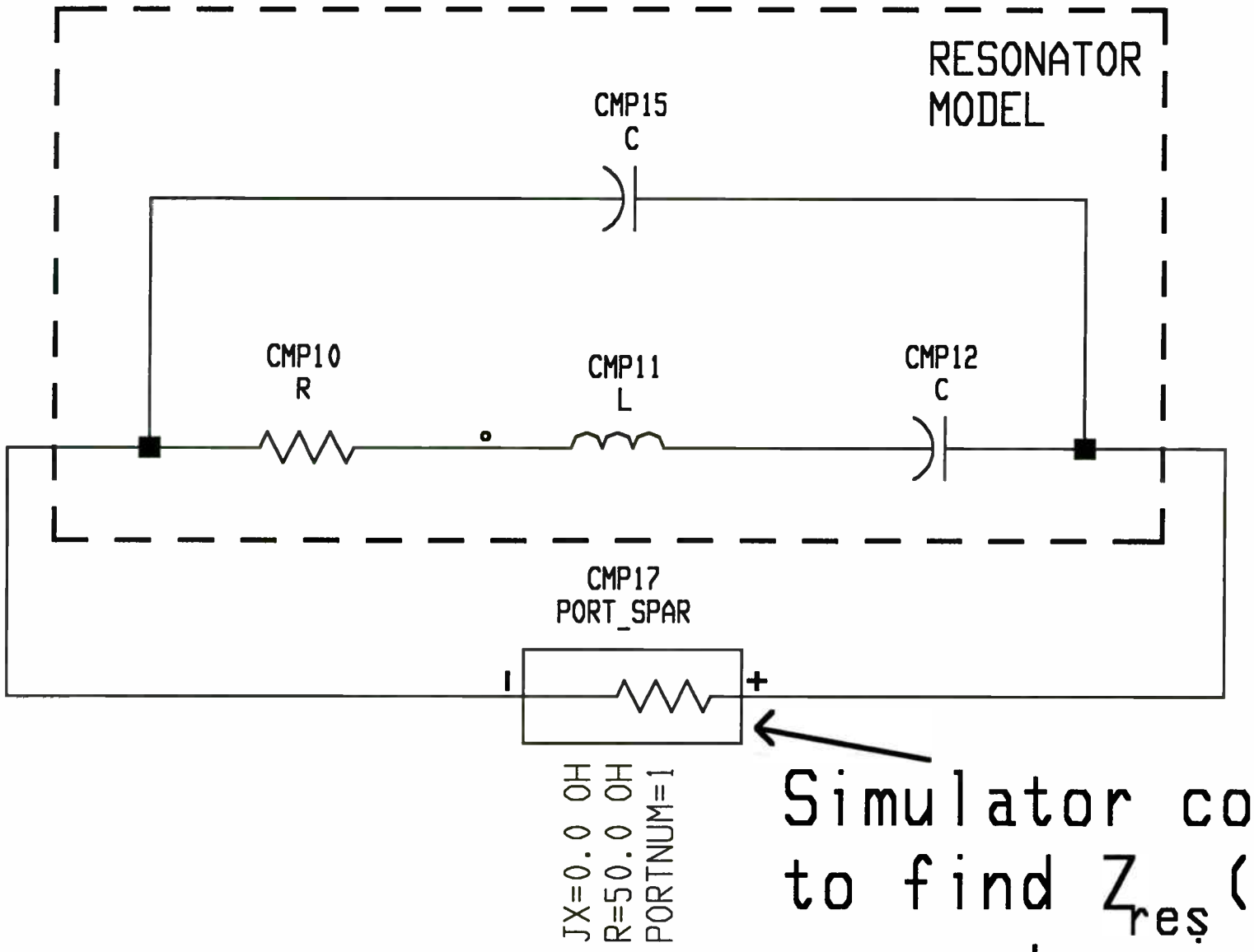


Figure 5a: Resonator replaced with current source, for large-signal impedance analysis.



Simulator component to find $Z_{res}(f)$, resonator impedance vs. frequency.

Figure 5b: Simulating resonator impedance as a function of frequency.

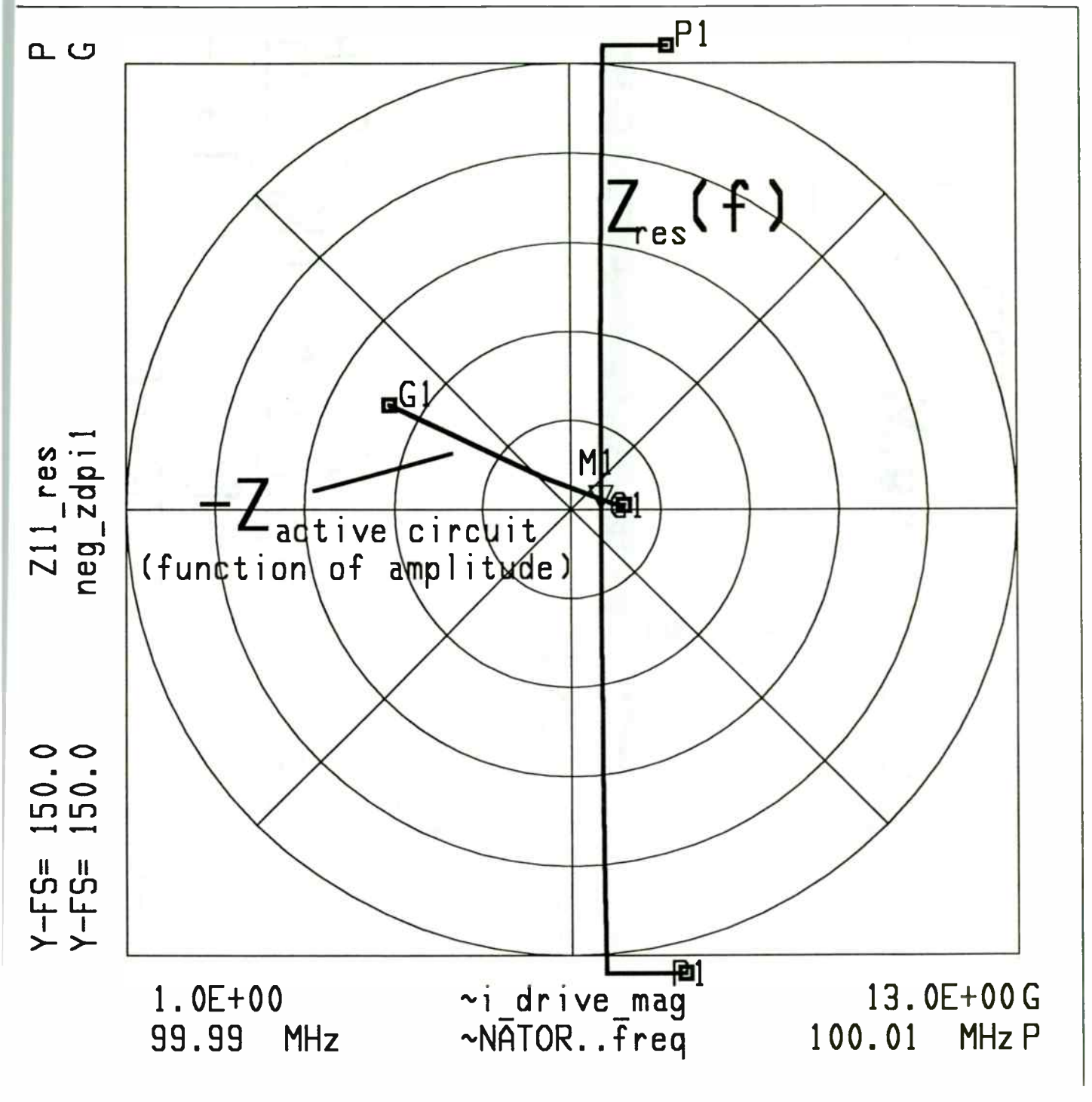


Figure 6: Plot of resonator impedance versus frequency, and negative of active circuit impedance versus drive level.

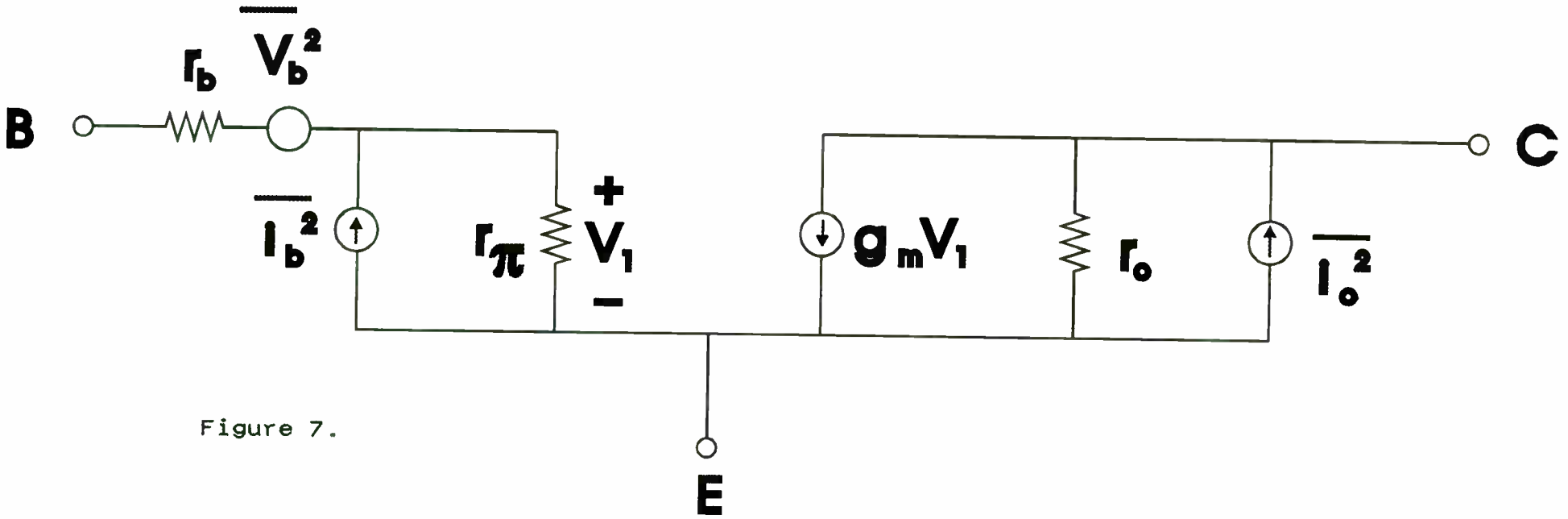


Figure 7.

$$\overline{V_b^2} = 4kTr_b \triangle f$$

$$\overline{i_c^2} = 2qI_C \triangle f$$

$$\overline{i_b^2} = 2qI_B \triangle f + K_f \frac{I_B^{A_f}}{f} \triangle f + K_B \frac{I_B^{A_B}}{1 + \left\{\frac{f}{f_B}\right\}^2} \triangle f$$

SHOT NOISE

FLICKER NOISE

BURST NOISE

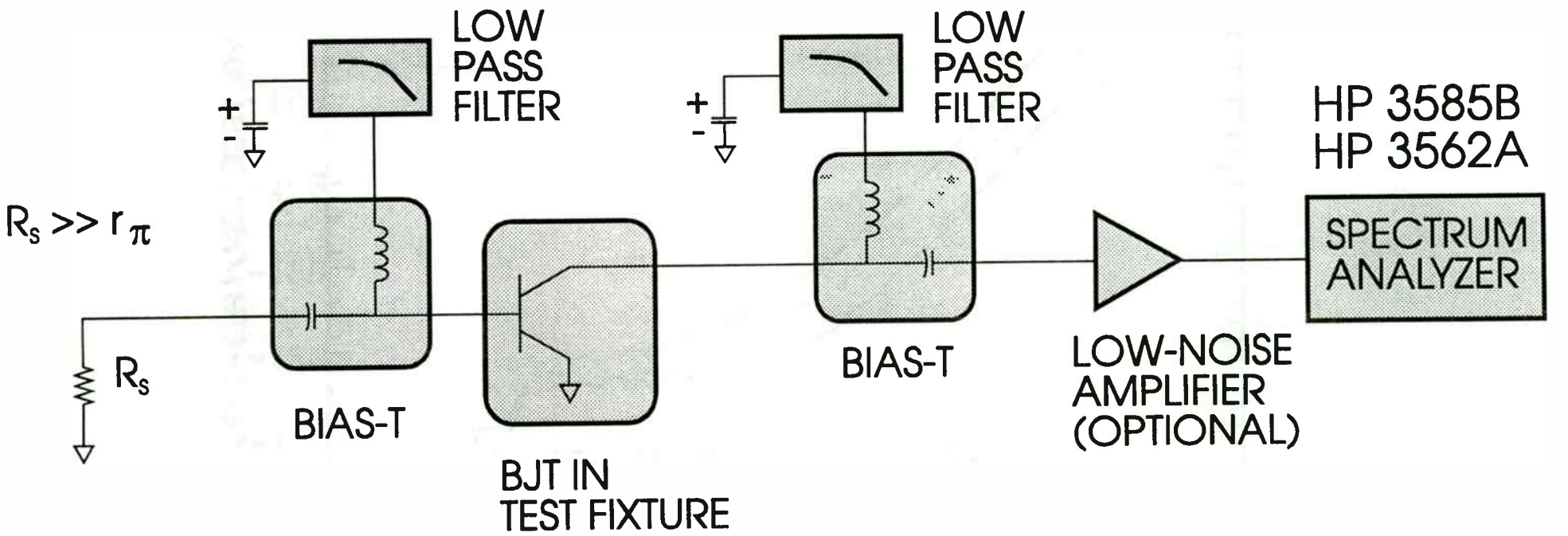


Figure 8.

1/f Noise Characteristics of MODIC

(Conventional PM MODFET)

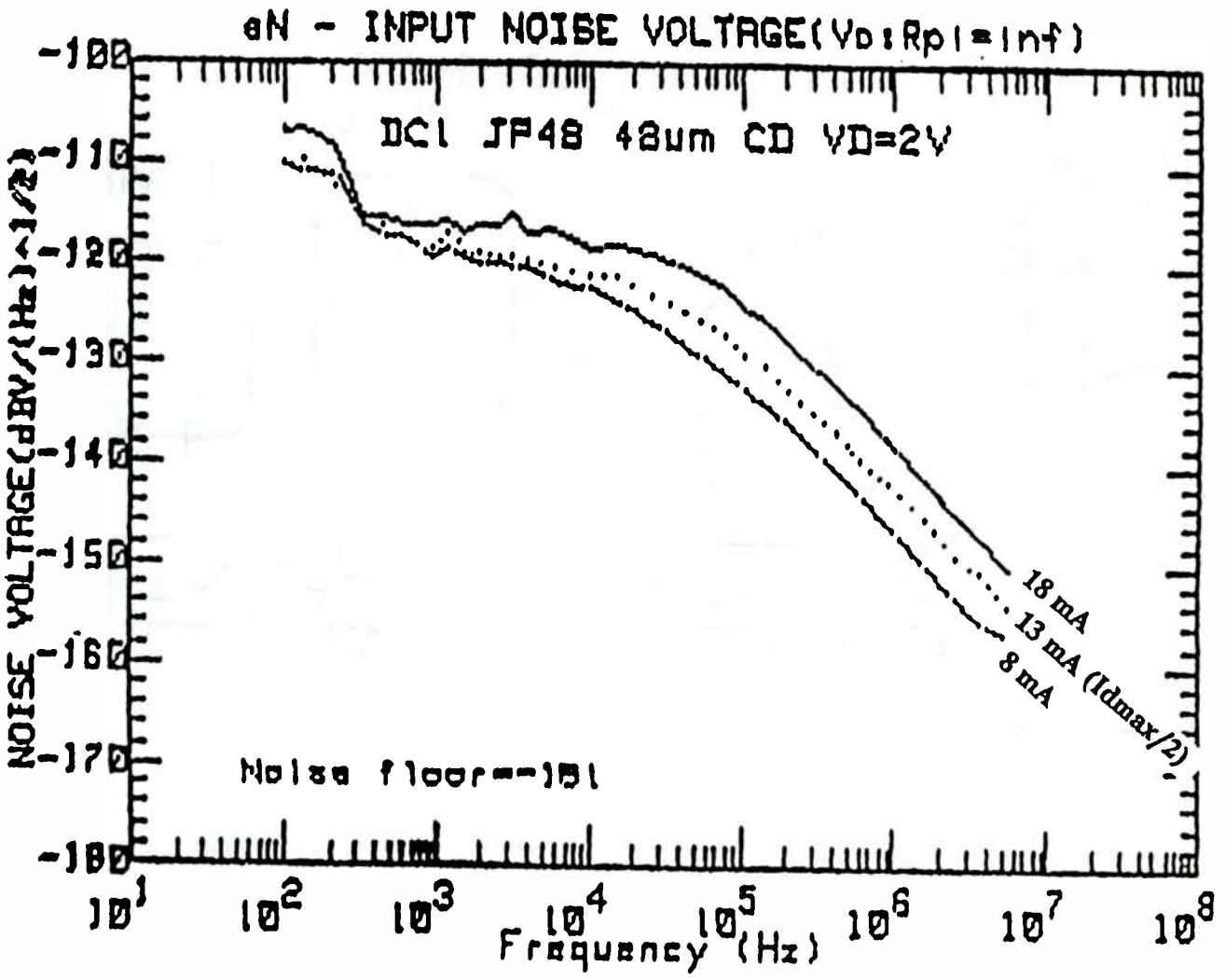
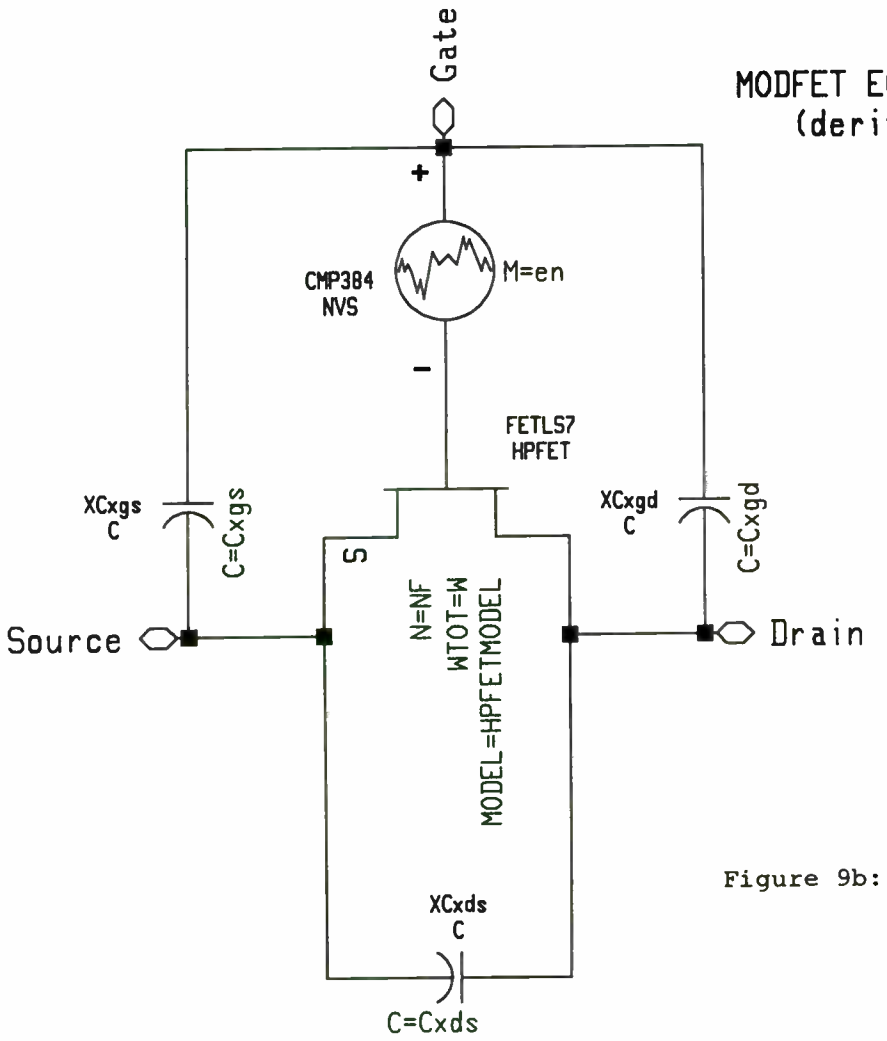


Figure 9a: Measured equivalent input noise voltage spectrum of MODFET.



MODFET EQUIVALENT INPUT NOISE VOLTAGE EQUATIONS:
(derived from curve fitting)

Low Frequency Noise Model

```
EQUATION Width=W
EQUATION engr_dBV=-120          g-r noise plateau dBV
EQUATION engro=10^(engr_dBV/20)
EQUATION fgr=40e3               g-r noise corner

EQUATION engr=engro/sqrt(1+(FREQ/fgr)^2)

EQUATION enf_dBV=-99            1/f noise at 1 Hz dBV
EQUATION enfo=10^(enf_dBV/20)

EQUATION enf=enfo/sqrt(FREQ+1e-49)
EQUATION Width_LFn=0.048        width of FET for 1/f noise (mm)

EQUATION en=sqrt((enf^2+engr^2)*(Width_LFn/(Width*1000)))
```

Figure 9b: Equations to model MODFET's equivalent input noise voltage.

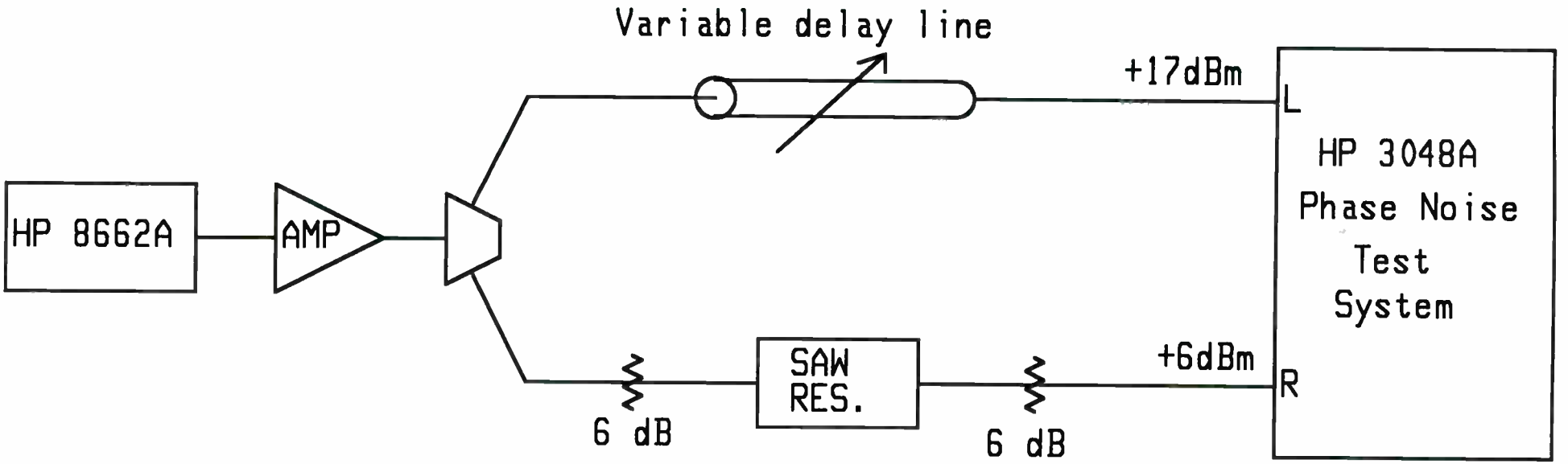


Figure 10: Residual phase noise measurement set-up.

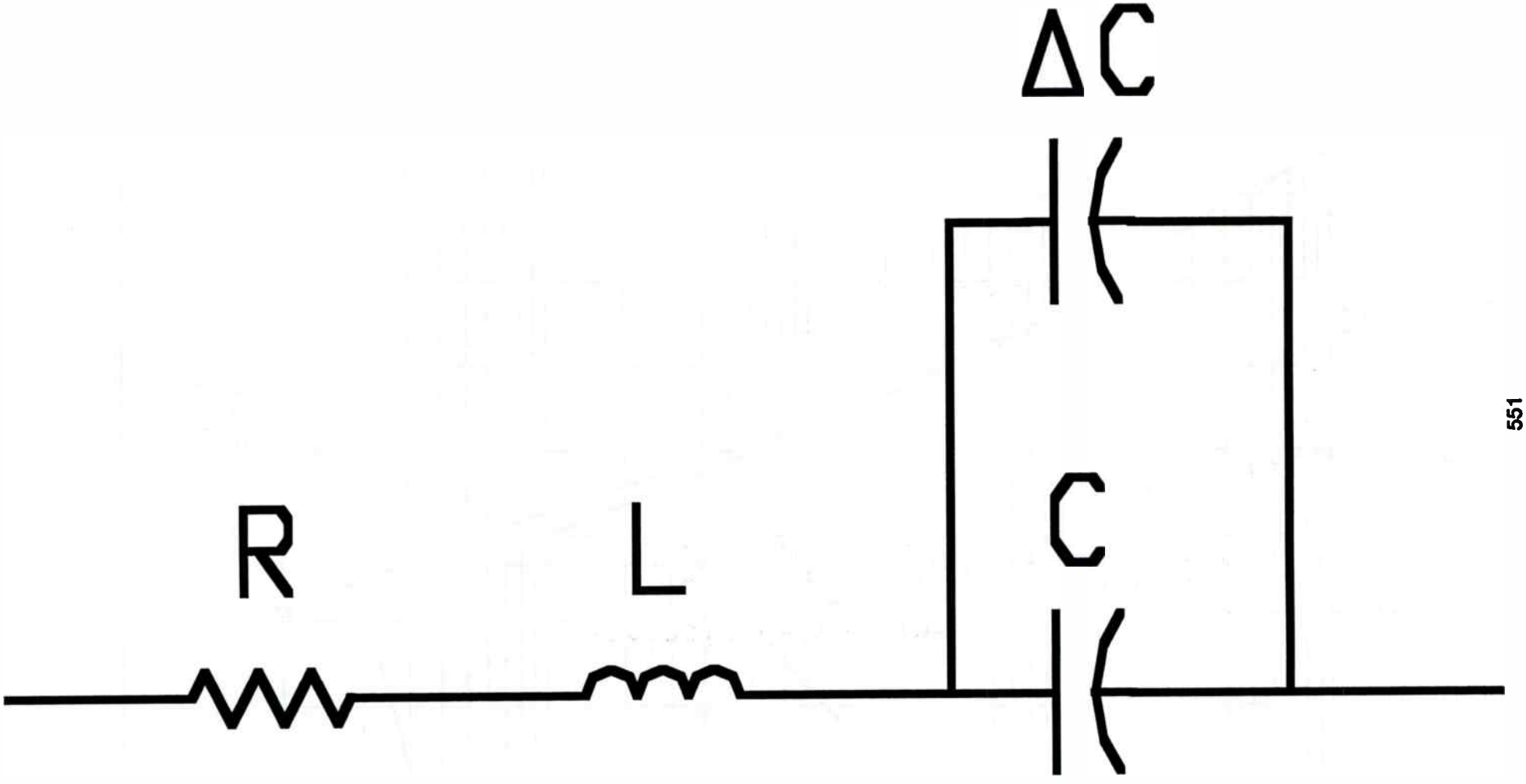


Figure 11: Resonator equivalent circuit, with differential capacitor, ΔC, to model 1/f frequency noise.

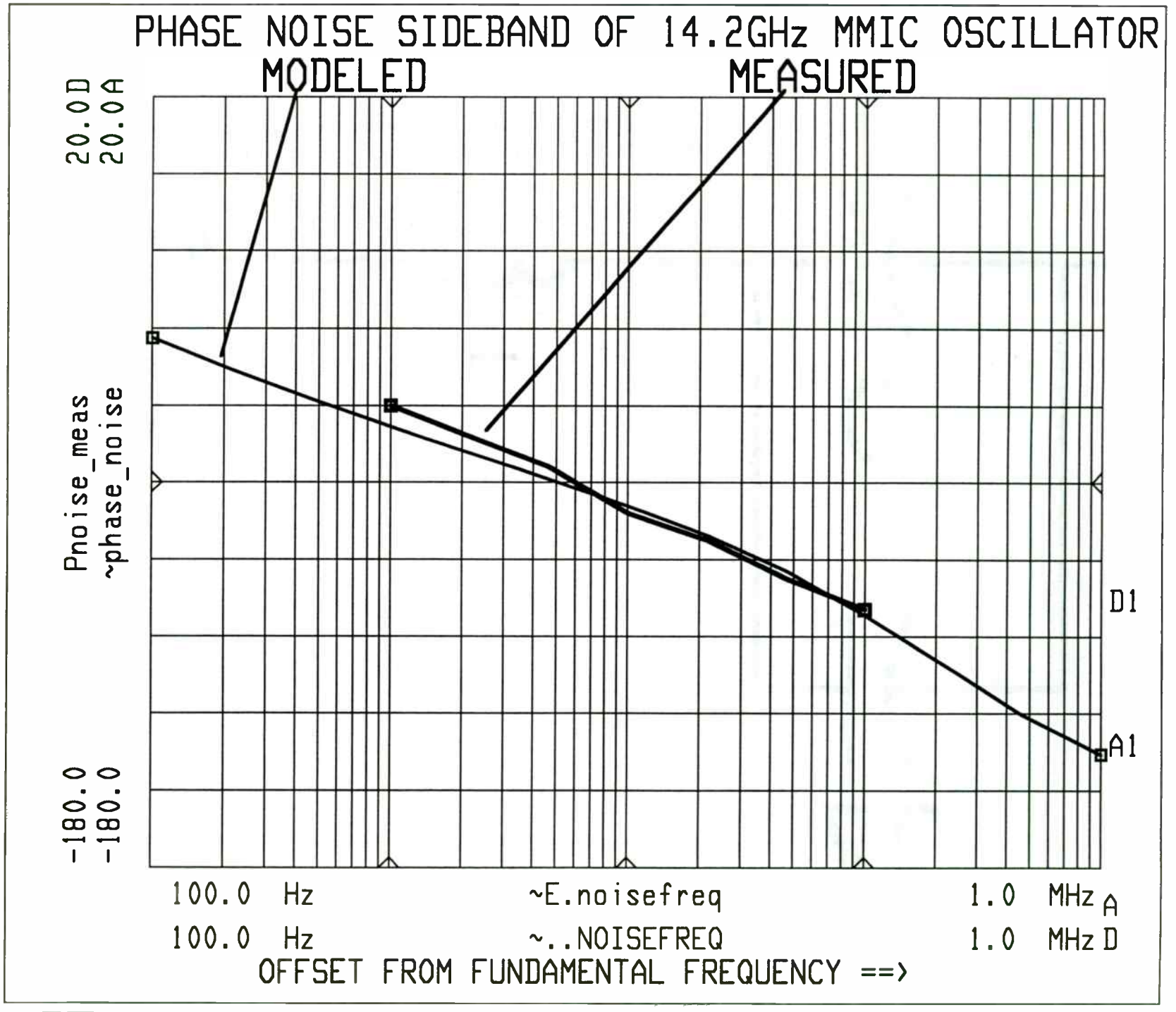


Figure 12: YIG oscillator phase noise simulation and measurement.

WHERE DID RF GROUND GO ?

by

SAMSUNG MICROWAVE SEMICONDUCTOR STAFF

INTRODUCTION

A LARGE VARIETY OF BUILDING BLOCK PARTS ARE BECOMING AVAILABLE TO THE SYSTEM DESIGNER AND WIRELESS PRODUCT MANUFACTURER. SPECIFICALLY, THERE ARE FAMILIES OF GaAs SWITCH PRODUCTS, ATTENUATORS, LOW NOISE PREAMPLIFIERS, GAIN STAGES, POWER STAGES AND NON-LINEAR ELEMENTS SUCH AS DOWN CONVERTORS AND UP CONVERTORS. THE COMMERCIAL WORLD WHERE THESE PRODUCTS ARE TO BE USED IS EXTREMELY COST CONCIOUS AND THE DEVICE VENDORS ARE RESPONDING WITH AGGRESSIVELY PRICED UNITS IN LOW COST PLASTIC PACKAGING. MOST OF THE PRODUCTS MENTIONED ARE AVAILABLE IN STANDARD OUTLINE INTEGRATED CIRCUIT, SOIC, PACKAGES WITH 8 AND HIGHER LEAD COUNT.

WHILE THE FREQUENCY OF OPERATION CAN GO DOWN TO DC, MOST PRODUCTS ARE USEFUL TO FREQUENCIES UP AS HIGH AS 8 GHz. THERE IS ALSO A SPECIAL CONCENTRATION ON PARTS FOR THE 900 MHz, 1.4 TO 1.9 GHz, 2.4 GHz AND 5.7 GHz FREQUENCIES OF APPLICATION. THE CONCERN ADDRESSED IN THIS PAPER IS THE NEED FOR PROPER BOARD MOUNTING OF SUCH PARTS ESPECIALLY AS THE FREQUENCY OF APPLICATION GOES UP. MANY OF THE POTENTIAL USERS OF THE GaAs SOIC PACKAGED PRODUCTS HAVE GOOD RF EXPERIENCE WITH LOWER FREQUENCY Si BASED PRODUCTS YET RUN INTO CONSIDERABLE DIFFICULTY IN GETTING VENDOR CLAIMED PERFORMANCE WITH THEIR INITIAL ATTEMPTS AT MOUNTING AND OPERATING THE HIGHER FREQUENCY PRODUCTS. EXPERIENCE HAS SHOWN THAT THE PRIMARY ISSUE IS AN UNAPPRECIATED NEED FOR MINIMIZING PARASITIC LEAD INDUCTANCE AND, MOST SIGNIFICANTLY, FOR UNDERSTANDING THE AFFECTS ARISING FROM LACK OF GOOD RF GROUND OR FROM GROUND RETURNS MADE TOO FAR AWAY FROM THE POINT OF NEED.

A BASIC TENET FROM TRANSMISSION LINE THEORY IS THE INCREDIBLE FACT THAT A SHORT BECOMES AN OPEN AND VICE-VERSA FOR A MERE QUARTER WAVELENGTH OF LINE TERMINATED IN A SHORT OR OPEN, RESPECTIVELY. FOR FREQUENCIES IN THE TENS OR LOW HUNDREDS OF MHz, A QUARTER WAVELENGTH IS ON THE ORDER OF 750 TO 40 cm IN AIR AND ALTHOUGH REDUCED APPROXIMATELY BY THE SQUARE ROOT OF THE BOARD DIELECTRIC CONSTANT, THESE DIMENSIONS ARE LARGE RELATIVE TO THE PACKAGE SIZE AND BOARD SIZE. AT, SAY, 2.4 GHz OPERATION, HOWEVER, THE PHYSICAL LENGTH OF A QUARTER WAVELENGTH ON A TYPICAL LOW DIELECTRIC BOARD IS UNDER 2 cm AND IF HIGH DIELECTRIC BOARDS ARE USED, SAY $\varepsilon = 10$, THEN THE LENGTH IS REDUCED TO UNDER 1 cm. THE CONSEQUENCE IS THAT QUITE PRONOUNCED TRANSMISSION LINE EFFECTS CAN OCCUR FROM MISSING AND DISPLACED GROUND CONNECTIONS AND A GENERAL INATTENTION TO GOOD MICROWAVE CIRCUIT PRACTISE.

TECHNICAL BODY

EXAMPLE CASES ARE PRESENTED THAT WILL SHOW THE KINDS OF EFFECTS THAT OCCUR WHEN POOR TO MEDIOCRE TO NEAR OPTIMUM BOARD MOUNTING IS REALIZED. AN SOIC-8 PART WITH THE FUNCTION OF LOW NOISE PREAMP[1] AND AN SOIC-8 VARIABLE WIDEBAND ATTENUATOR PART[2] WILL BE STUDIED.

THE SINGLE BIAS, LOW NOISE GaAs MMIC PRODUCT (LNA) WAS DESIGNED PRIMARILY FOR 1.8 AND 1.9 GHz WIRELESS AND THE 2.4 GHz ISM BAND APPLICATIONS AND PROVIDES USEFUL OPERATION OVER A BAND FROM ABOUT 1.5 TO OVER 3 GHz. THE DIE USED IN THE SOIC-8 PRODUCT IS SHOWN IN FIGURE 1. A SINGLE VDD FROM 3 TO 7 V CAN BE USED WITH A GATE CONTROL VOLTAGE OF FROM -3 V TO -9 V. NOMINAL BIAS FOR THE PACKAGED PART IS A SINGLE +5 V APPLIED TO BOTH THE VDD AND THE VGG TERMINAL. THE USE OF AN EXTERNAL RESISTOR ON THE MOUNTING BOARD SETS THE DESIRED IDD CURRENT LEVEL.

IDEAL REFERENCE PERFORMANCE TYPICAL FOR THE LNA UNENCUMBERED BY ANY PACKAGING PARASITICS AND MOUNTING DIFFICULTIES IS SHOWN IN FIGURES 2 AND 3. THE DIE IS MOUNTED ON A HIGH FREQUENCY CARRIER IN A GOOD 50 Ω ENVIRONMENT AND THE DATA SHOW WHAT THE DESIGN IS CAPABLE OF ACHEIVING. ONCE IN THE SOIC-8 PACKAGE ENVIRONMENT, THERE IS SOME DEGRADATION EXPECTED IN PERFORMANCE DUE TO PARASITIC EFFECTS OF THE LEAD FRAME ESPECIALLY AT THE HIGHER FREQUENCIES OF OPERATION.

WITHOUT REGARD TO MOUNTING OPTIMIZATION, THE FIRST TIME USER MIGHT VERY WELL SIMPLY SOLDER THE PACKAGE LEADS DOWN ON A BOARD WITH STRAIGHTFORWARD LINE CONNECTIONS WHICH PROVIDE THE BASIC RF-IN AND RF-OUT AND BIAS CONNECTIONS IN A MICROSTRIP OR EVEN A COPLANAR TYPE OF CONFIGURATION LIKE THOSE SHOWN IN FIGURE 4. RF GROUND IS GENERALLY SUPPLIED BY THE METALLIC PLANE ON THE BACK OF THE BOARD AND TOPSIDE GROUND CONNECTIONS ARE MADE BY AN OCCASIONAL VIA OR EDGE-AROUND METALIZATION. THE SCHEMATICS IN FIGURES 5 AND 6 ARE TYPICAL OF LAYOUTS THAT HAVE BEEN ENCOUNTERED. A SIMILAR MOUNTING ARRANGEMENT WAS MADE ON AN ACTUAL PART AND PERFORMANCE DATA WERE MEASURED. WHILE ALL THE REQUISITE CONNECTIONS WERE MADE, IT IS SEEN IN THE DATA SHOWN IN FIGURE 7, THAT THERE IS A SUBSTANTIAL MISS IN EXPECTED PERFORMANCE. THE GAIN LEVEL AND GAIN BANDWIDTH ARE REDUCED CONSIDERABLY FROM DATA SHEET EXPECTATIONS ESPECIALLY AT THE HIGHER FREQUENCIES OF OPERATION. THE DATA SHOWN ARE SMOOTHED SINCE REFLECTION DETAIL WAS OBSERVED.

THE POORER PERFORMANCE IS A DIRECT CONSEQUENCE OF NOT PROVIDING RF GROUND RETURN AT A POINT WHERE THE RF INPUT AND RF OUTPUT ARE RESPECTIVELY LAUNCHED AND COLLECTED. THE EFFECTIVE PATH LENGTH FOR THE CLOSEST PACKAGE GROUND LEAD TO THE POINT WHERE BOARD BACKSIDE GROUND IS FIRST CONNECTED WAS EASILY 1 cm OR MORE WHICH IS SOME SUBSTANTIAL FRACTION OF A WAVELENGTH FOR THE $\varepsilon = 2.4$ BOARD USED. DUE TO THIS LENGTH OF "TRANSMISSION LINE" THERE IS AN UNWANTED PARASITIC IMPEDANCE INTRODUCED TO THE DEVICE THAT CAUSES A REFLECTION OR AN ABSORBTION OF SIGNAL WHICH THEN AFFECTS GAIN OR OTHER IMPORTANT PARAMETERS. THE AMOUNT OF DRASTIC RIPPLE IN THE INPUT AND OUTPUT RETURN LOSS IS ESPECIALLY AFFECTED.

BY RECONSTRUCTING THE MOUNTING SO THAT IMMEDIATE RF GROUND RETURNS ARE MADE VERY NEAR THE APPROPRIATE PACKAGE LEADS, THE EXTRA "LINE

LENGTH" IS DRASTICALLY REDUCED. A SCHEMATIC OF THE IMPROVED BOARD LAYOUT IS SHOWN IN FIGURE 8. LOCAL TOPSIDE TO BOTTOM SIDE GROUNDING IS PROVIDED BY FILLED VIA HOLES ARRANGED AS CLOSE TO THE PACKAGE LEADS AS POSSIBLE. THE BIAS LINES ARE BROUGHT IN AS IF THEY WERE RF LINES AND PROVISION IS MADE FOR CAPACITOR BYPASSING AT THE RESISTOR AND AT OTHER POSITIONS ON THE LINES. THE PERFORMANCE OF THE LNA SHOWN IN FIGURE 9 REVEALS SUBSTANTIAL IMPROVEMENT OVER THE FIRST MOUNTING EXPERIMENT. THE GAIN IS AT EXPECTED DATA SHEET LEVELS AND THE HIGH FREQUENCY PERFORMANCE IS MUCH IMPROVED. FIGURE 10 SHOWS THE GAIN AND INPUT RETURN LOSS FOR A BROADER FREQUENCY RANGE AND FIGURE 11 CONTRASTS THE NOISE FIGURE OF THE SOIC-8 DEVICE WITH THE CARRIER MOUNTED DIE. THE RESULTS ARE QUITE CLOSE AND WITHIN 0.2 dB AT 2.4 GHz.

FURTHER IMPROVEMENT IN THE MOUNTING PROCEDURES ARE POSSIBLE. THE RF GROUNDING CONNECTIONS MADE AT THE INPUT AND OUTPUT SIDE OF THE SOIC-8 PACKAGE LEADS WERE CRITICAL IN IMPROVING THE LNA PERFORMANCE. OFTEN, HOWEVER, THERE CAN BE ADDED IMPROVEMENT IN CONTINUING THE TOPSIDE GROUNG METALIZATION FROM THE INPUT SIDE TO THE OUTPUT SIDE DIRECTLY UNDER THE PLASTIC PACKAGE BASE.

OTHER CONSIDERATIONS INVOLVE TECHNIQUES TO MINIMIZE THE "CROSSTALK" OF SIGNALS EXISTENT ON THE BOARD AND THE AVOIDANCE OF HAVING THE OUTPUT SIGNALS ELECTRICALLY INTERACTING WITH INPUT SIGNALS AND THEREBY SPOILING THE ISOLATION PROPERTIES OF THE PART OR WORSE. LAYING OUT OF SUCH CRITICAL SIGNAL CONNECTION LINES SHOULD BE DONE WITH AS MUCH SPACING APART AS IS PRACTICALLY POSSIBLE TO AVOID THESE POTENTIALLY ADVERSE "COUPLINGS".

THE SECOND PRODUCT EXAMPLE IS THE VARIABLE ATTENUATOR/SWITCH WHICH WAS ORIGINALLY DESIGNED FOR DC TO 20 GHz OPERATION IN DIE FORM BUT IN SOIC-8 PACKAGED FORM HAS PRIMARY USAGE FROM 800MHz THROUGH 6 GHz IN WIRELESS AND OTHER CIRCUIT APPLICATIONS. THE DIE USED IN THE SOIC-8 PRODUCT IS SHOWN IN FIGURE 12. BESIDE THE RF INPUT AND OUTPUT THERE ARE TWO CONTROL VOLTAGES USED TO SET THE ATTENUATION OR INSERTION LOSS LEVEL AND TO ADJUST THE VOLTAGE STANDING WAVE RATIO AT A GIVEN SET INSERTION LOSS LEVEL. THE INTRINSIC DIE PERFORMANCE WHEN MOUNTED IN A GOOD HIGH FREQUENCY 50 Ω TEST SYSTEM IS SHOWN FOR REFERENCE IN FIGURE 13.

AS IN THE CASE OF THE LNA, THE MOUNTING OF THE PACKAGED PART CAN AFFECT THE PRODUCT PERFORMANCE. IN MOST USAGE OF THE DEVICE THERE IS CONCERN FOR THE MINIMUM INSERTION LOSS AND THE MAXIMUM INSERTION LOSS OR ISOLATION THAT CAN BE OBTAINED AT THE FREQUENCIES OF OPERATION. THE SAME ISSUES OF RF GROUNDING VERY NEAR THE RF INPUT AND RF OUTPUT EXIST AS FOR THE LNA. ANY EXTRA LINE LENGTH USUALLY RESULTS IN A HIGHER INSERTION LOSS. ADDTIONALLY, NEARLY ALL THE LAYOUT AND CONNECTION CHOICES WILL HAVE SOME EFFECT ON THE MAXIMUM ISOLATION THAT CAN BE OBTAINED. PROVIDING LINE AND LEAD SEPARATION ARE USUALLY GOOD PRACTISE TO ACHIEVE ISOLATION AND OFTEN THE EXTENSION OF TOPSIDE GROUNDING METALIZATION CAN HELP BY ALLOWING STRAY ELECTRIC FIELD LINE TERMINATIONS.

IMPROVED MOUNTING PROCEDURES WERE APPLIED INCLUDING CARRYING THE TOPSIDE GROUND CONNECTION FROM INPUT TO OUTPUT AS MENTIONED ABOVE. THE SCHEMATIC OF THE MOUNTING BOARD IS SHOWN IN FIGURE 14. MEASURED RESULTS SHOW CLEARLY THAT THE MINIMUM INSERTION LOSS IS VERY CLOSE TO

THE INTRINSIC BEHAVIOR OF THE CARRIER MOUNTED DIE. FIGURE 15 SHOWS THE TWO RESULTS OVER A 1 TO 7 GHz FREQUENCY RANGE.

[1]THE LNA DEVICE IS AN HMP-130203 SOIC-8 PACKAGED PRODUCT FROM SAMSUNG MICROWAVE SEMICONDUCTOR.

[2]THE VOLTAGE CONTROLLED ATTENUATOR DEVICE IS AN HMP-100008-1 SOIC-8 PACKAGED PRODUCT FROM SAMSUNG MICROWAVE SEMICONDUCTOR.

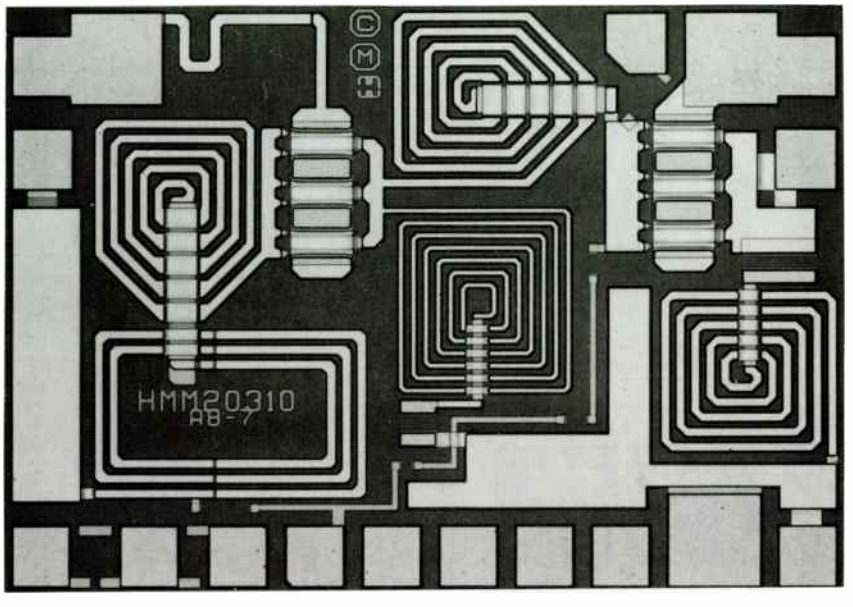


FIGURE 1. DIE MICROGRAPH OF HMM-20310 LOW NOISE AMPLIFIER MMIC

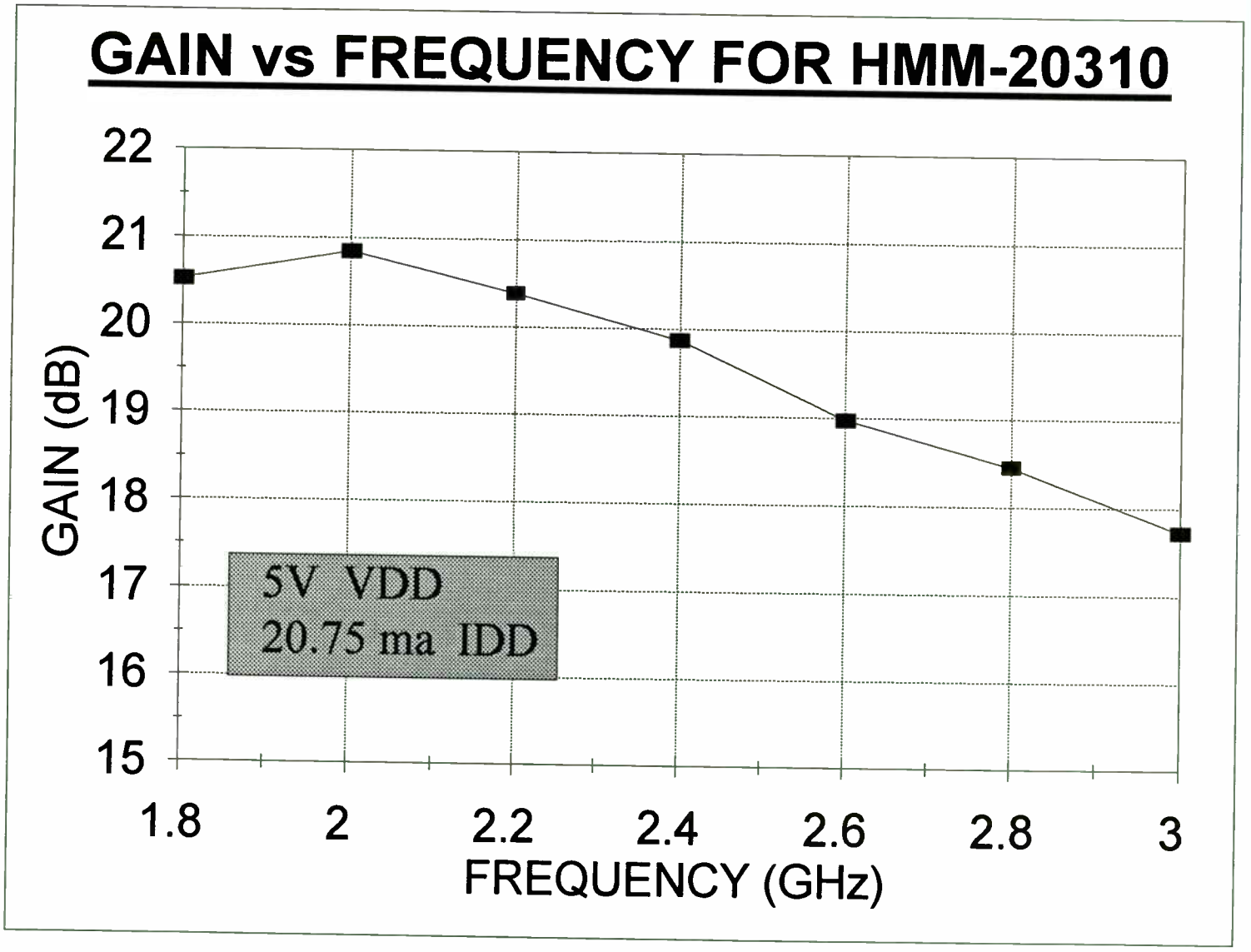


FIGURE 2. INTRINSIC GAIN PERFORMANCE OF LNA DIE MEASURED IN WIDEBAND SYSTEM

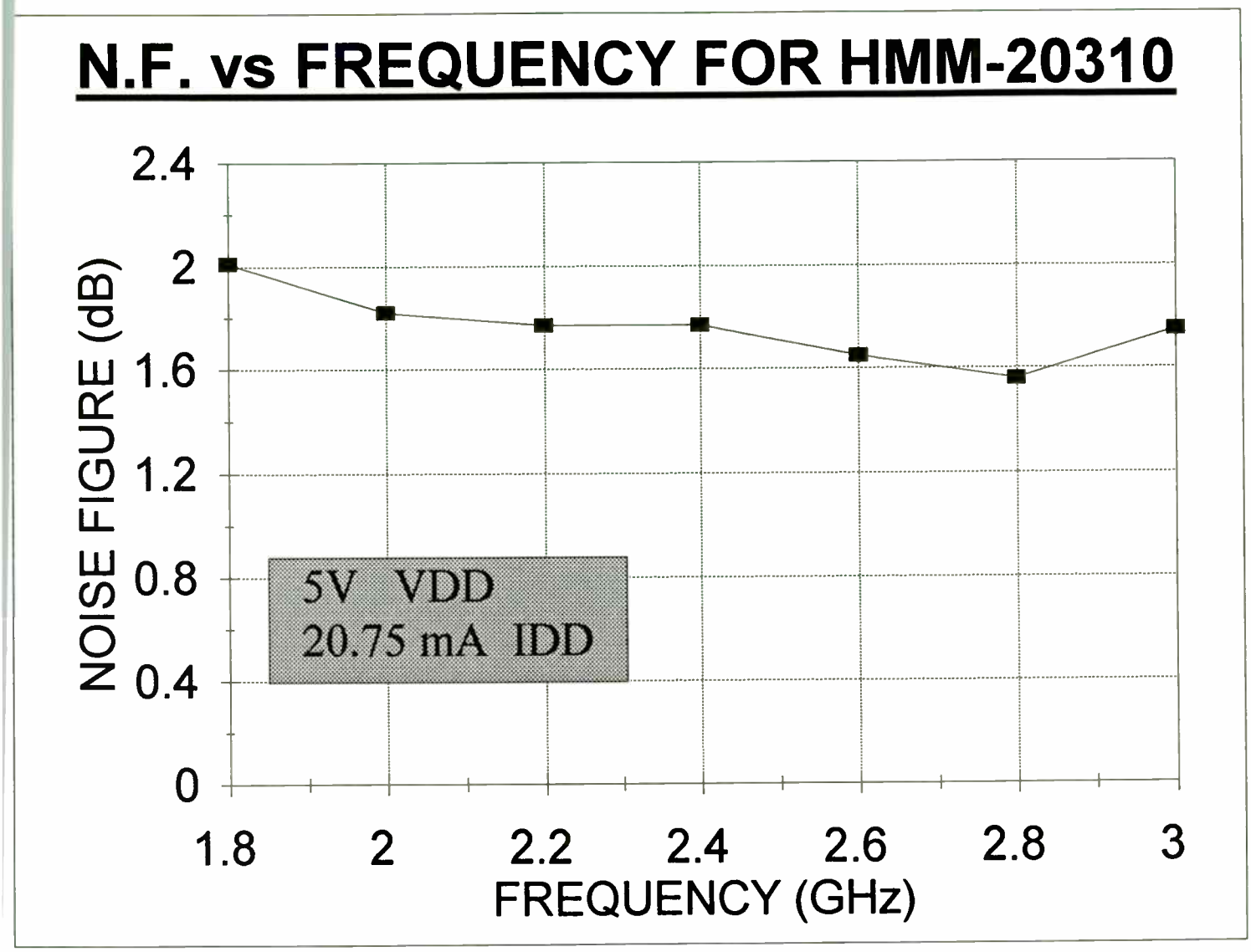
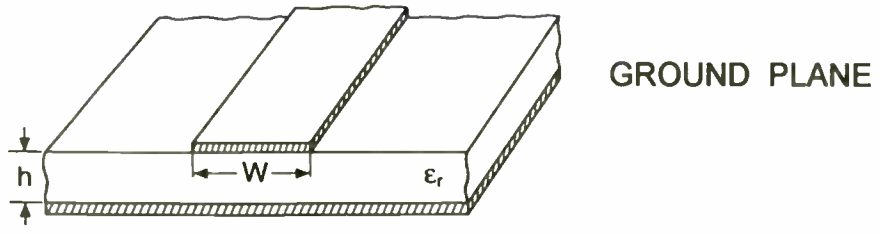
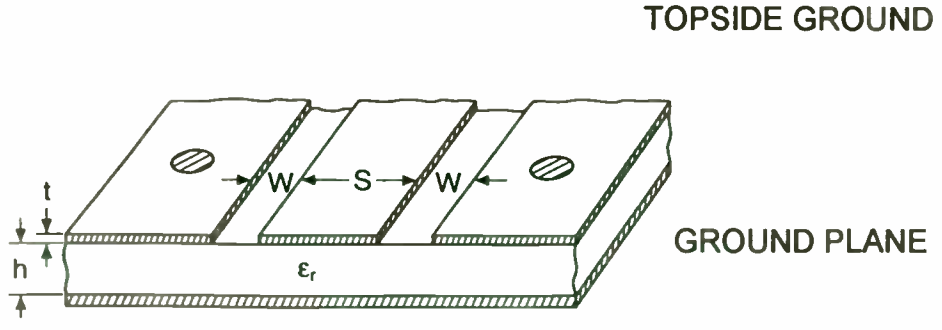


FIGURE 3. INTRINSIC NOISE FIGURE OF LNA DIE MEASURED IN WIDEBAND SYSTEM



MICROSTRIP TRANSMISSION LINE



COPLANAR TRANSMISSION LINE

FIGURE 4. SCHEMATICS OF MICROSTRIP AND COPLANAR TRANSMISSION LINES USED FOR RF AND MICROWAVE CIRCUITS

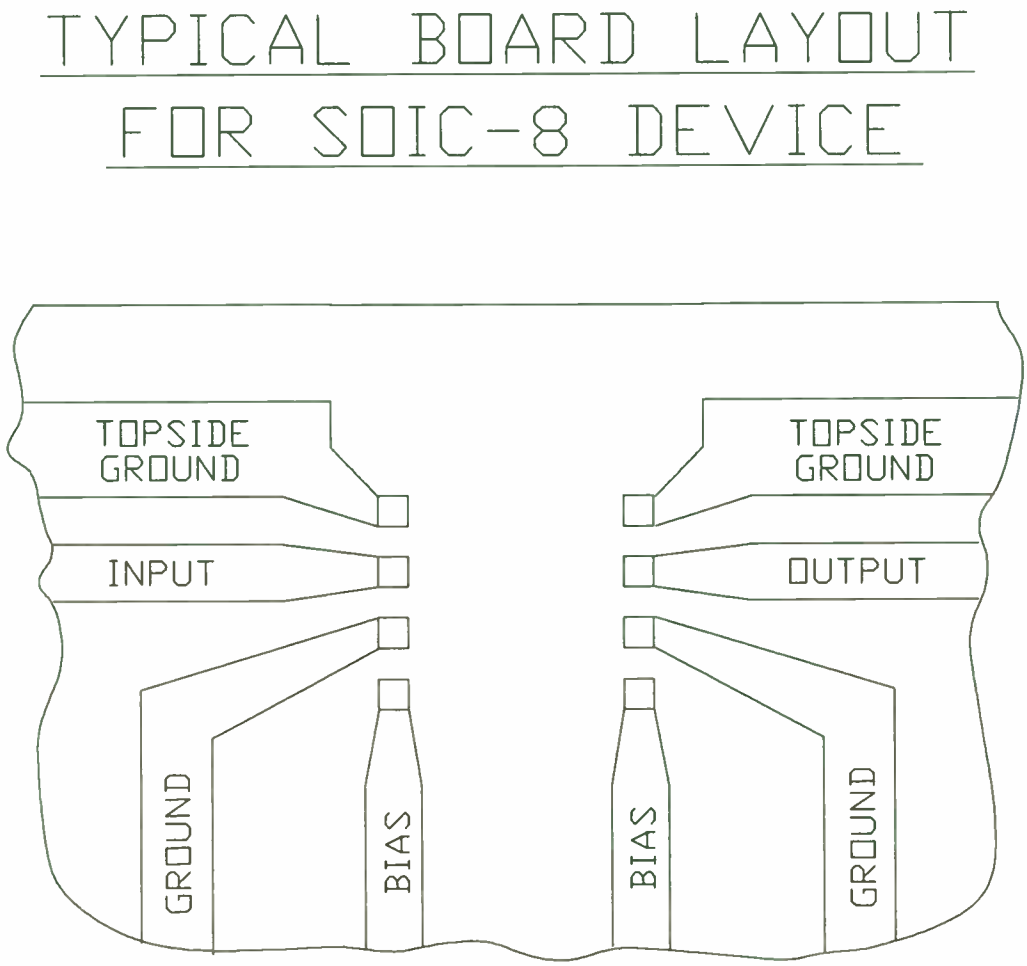


FIGURE 5. SCHEMATIC OF TYPICAL MICROSTRIP-LIKE BOARD CONNECTIONS FOR SOIC-8 DEVICES

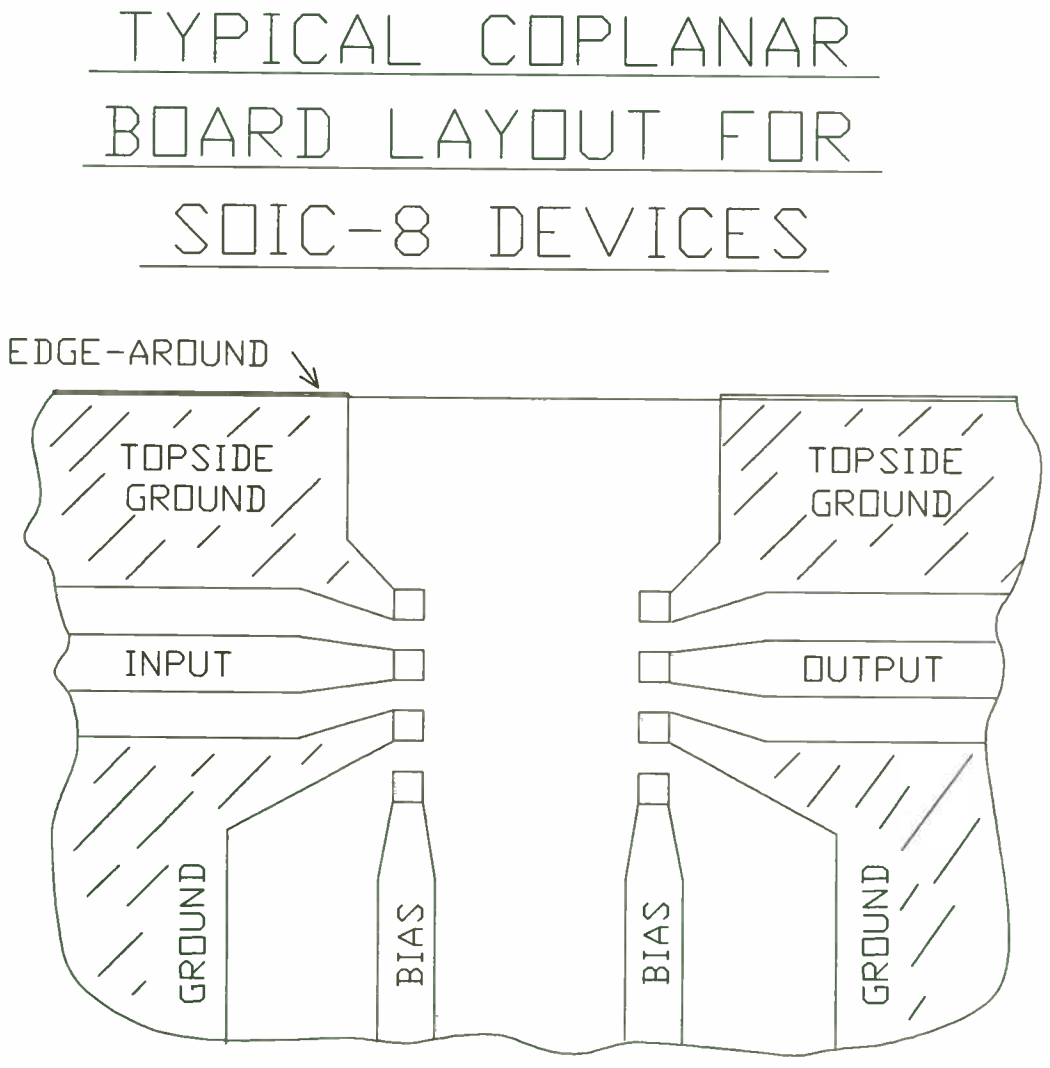


FIGURE 6. SCHEMATIC OF TYPICAL COPLANAR-LIKE BOARD CONNECTIONS FOR SOIC-8 DEVICES

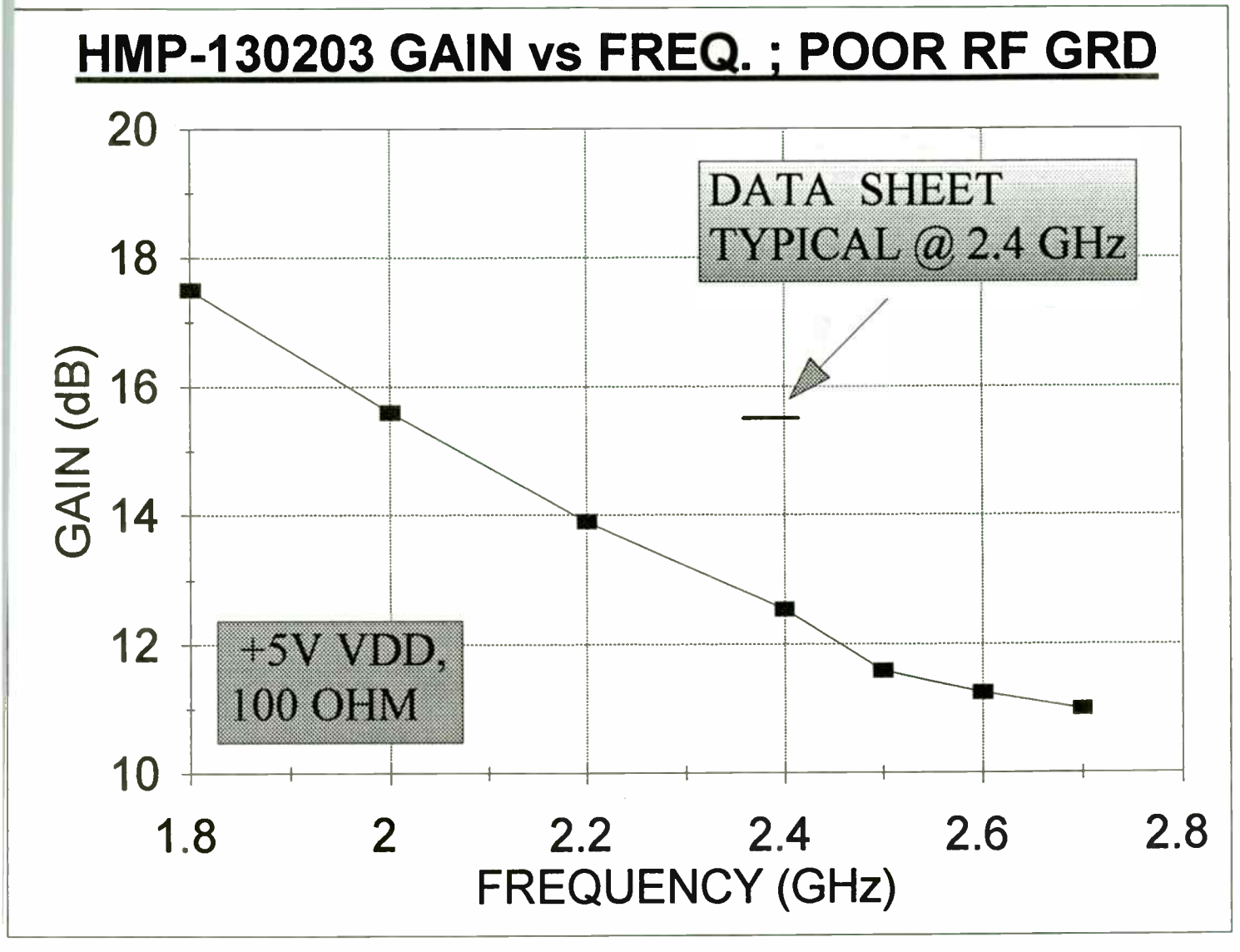


FIGURE 7. GAIN PERFORMANCE OF SOIC-8 LNA WITH POOR RF GROUND BOARD MOUNTING

IMPROVED BOARD LAYOUT FOR SOIC-8 LNA DEVICE

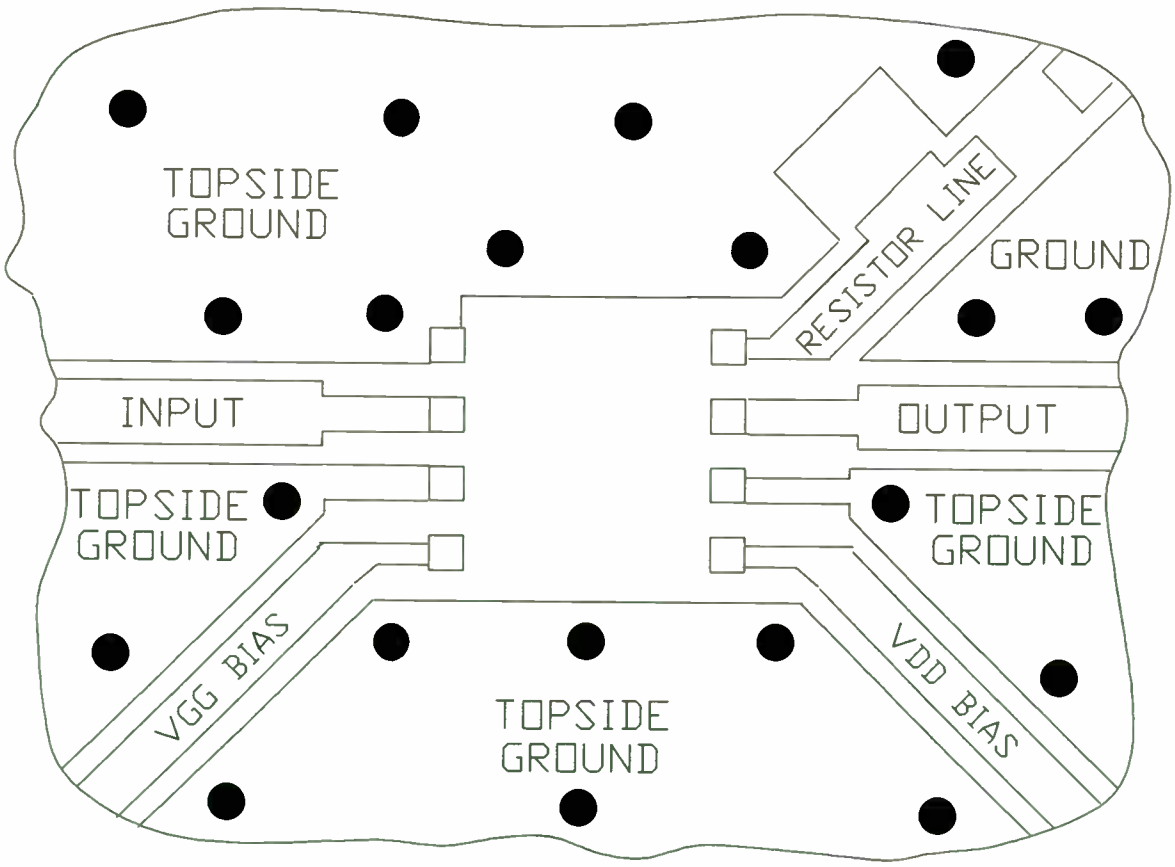


FIGURE 8. SCHEMATIC OF IMPROVED RF GROUNDING BOARD CONNECTIONS FOR SOIC-8 LNA

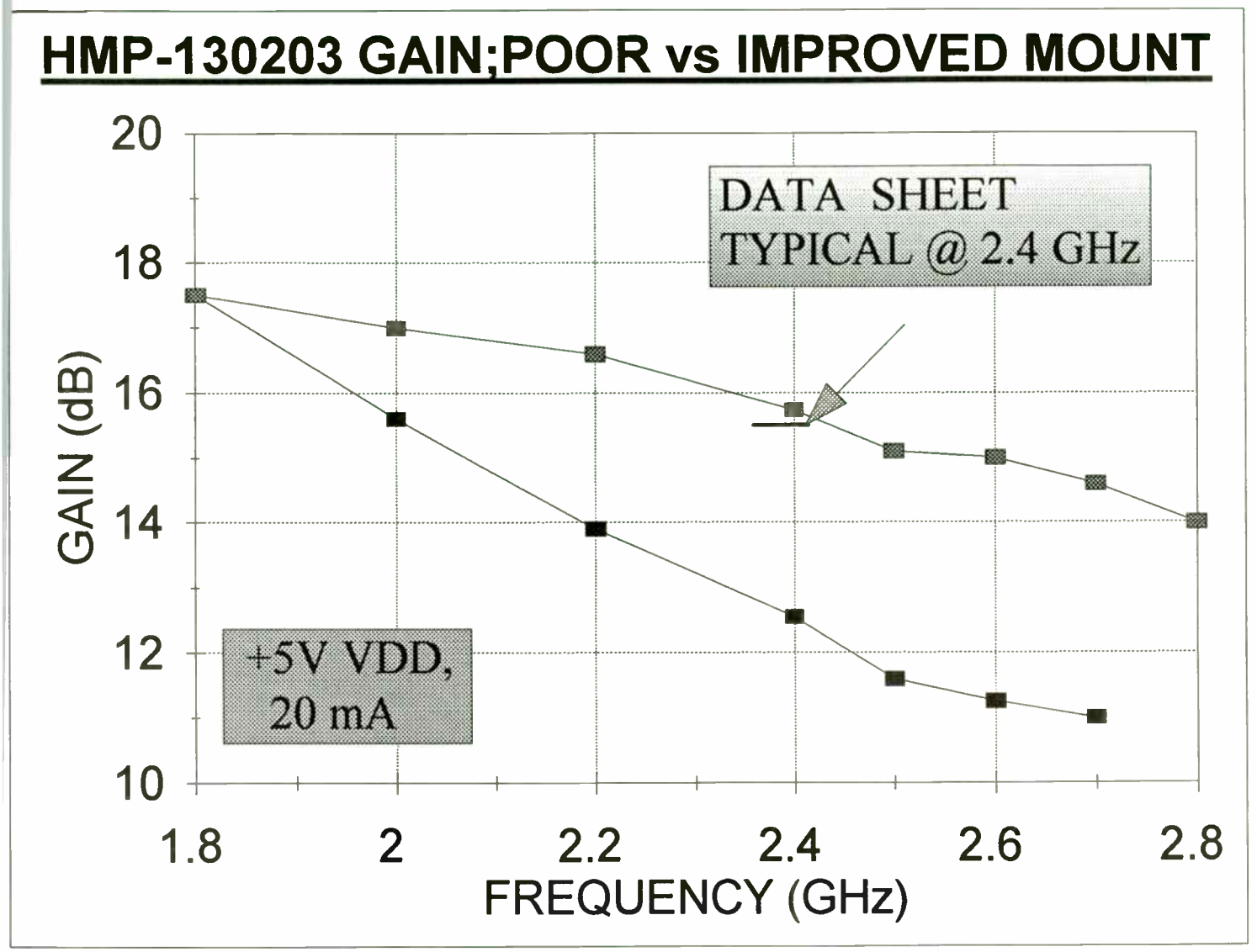


FIGURE 9. LNA GAIN PERFORMANCE CONTRAST BETWEEN POOR AND IMPROVED GROUNDING BOARD LAYOUT

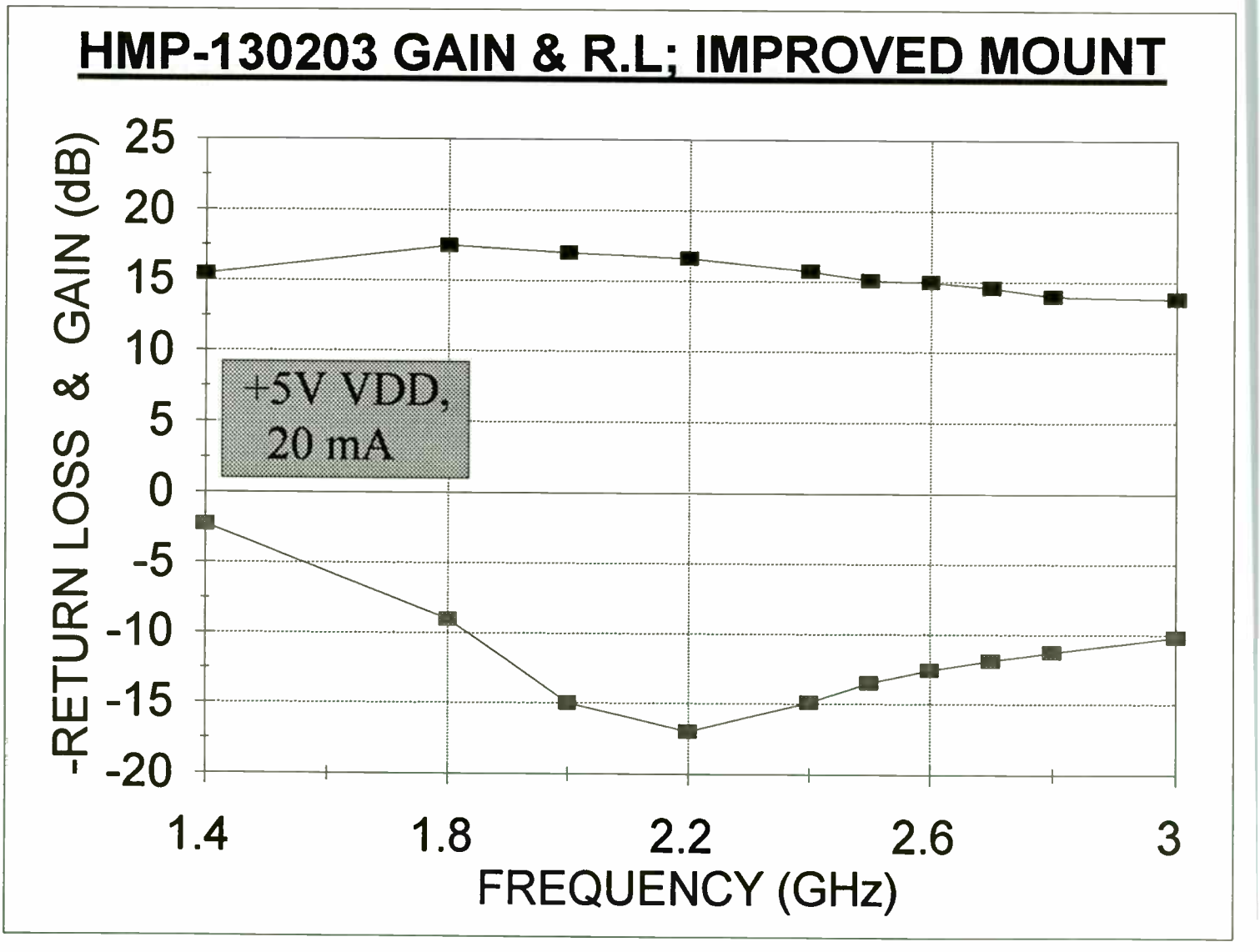


FIGURE 10. GAIN AND INPUT RETURN LOSS PERFORMANCE OF SOIC-8 LNA WITH IMPROVED BOARD LAYOUT

N.F. vs FREQ.; HMM-20310 vs HMP-130203

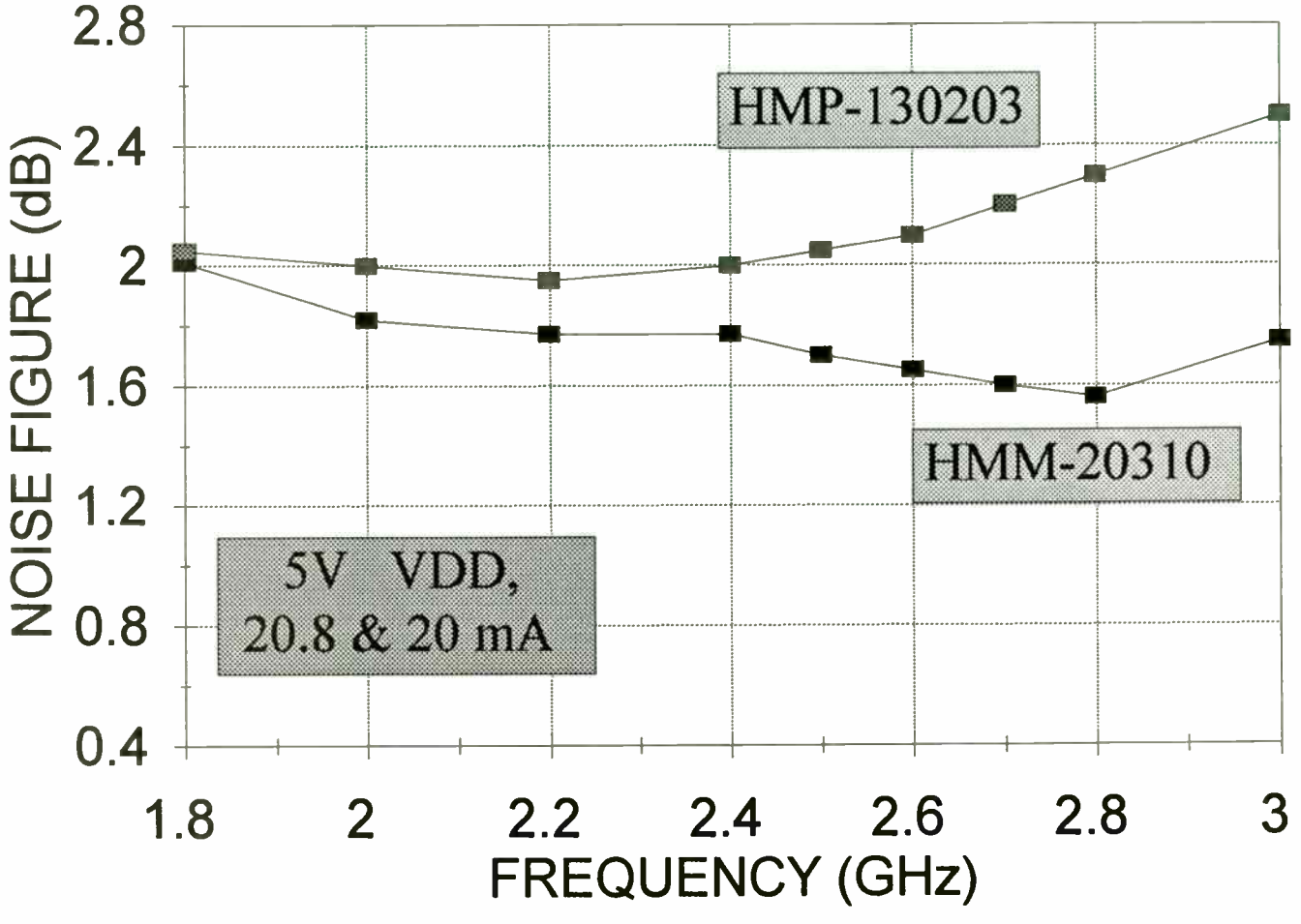


FIGURE 11. NOISE FIGURE PERFORMANCE OF SOIC-8 LNA WITH IMPROVED BOARD LAYOUT VERSUS INTRINSIC PERFORMANCE OF DIE

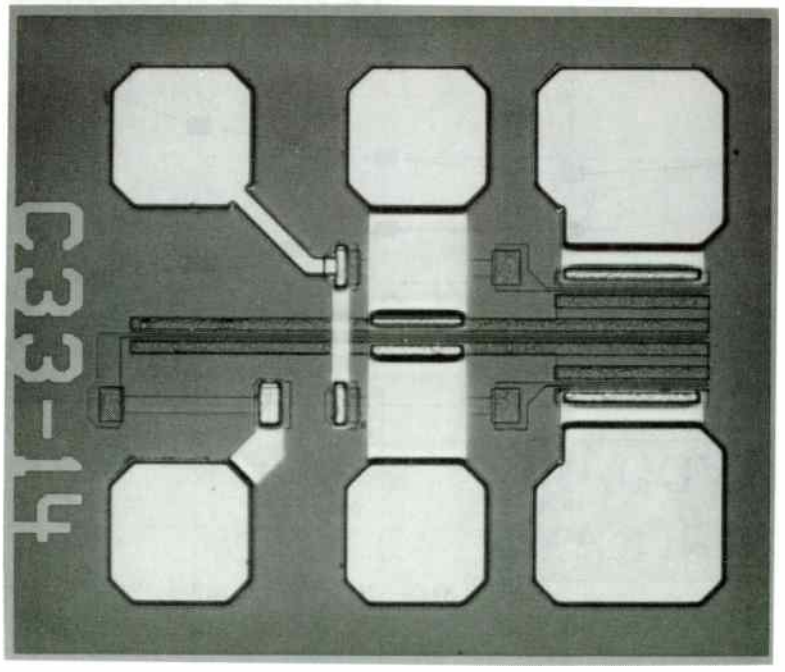


FIGURE 12. DIE MICROGRAPH OF HMM-11000 VOLTAGE CONTROLLED ATTENUATOR MMIC

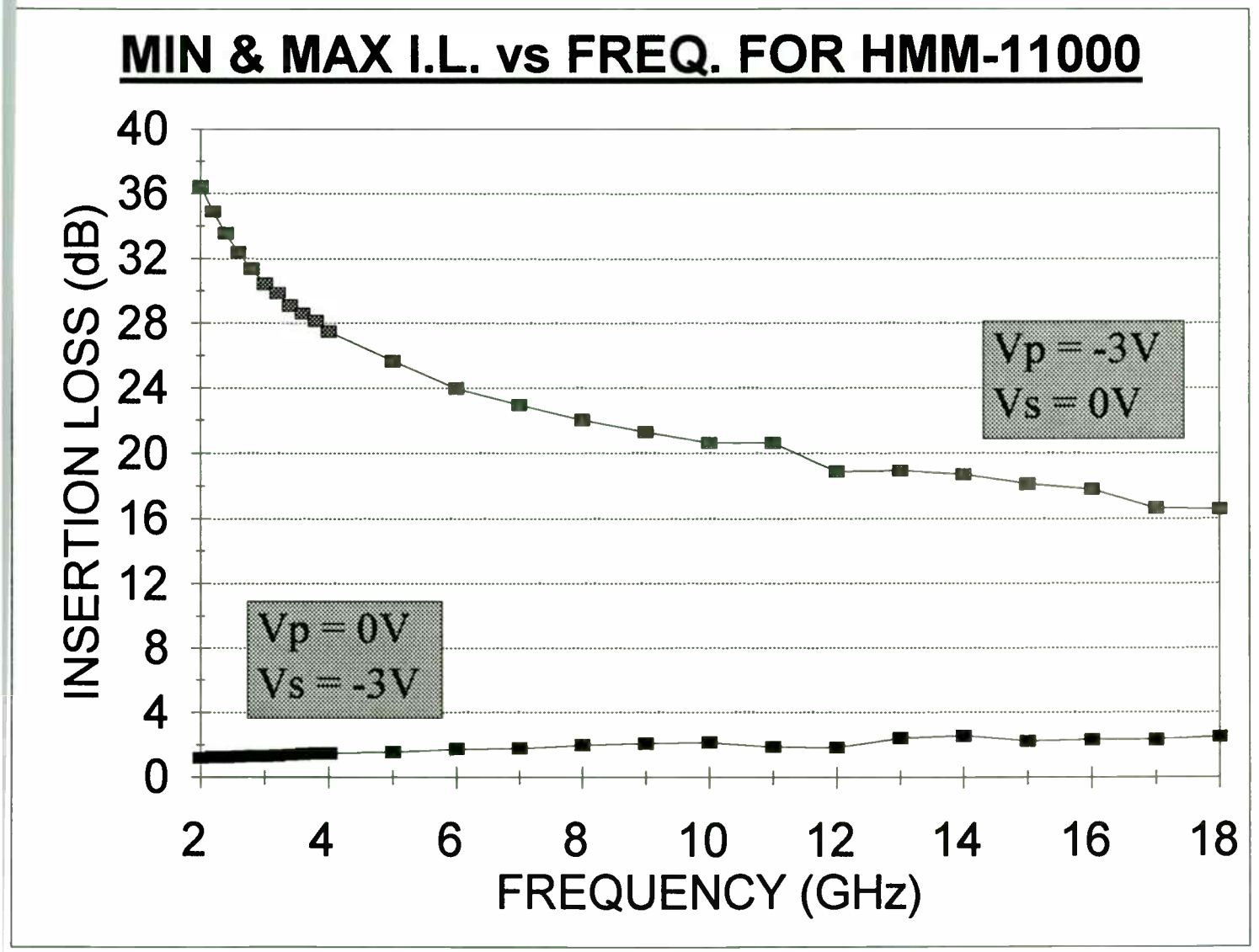


FIGURE 13. INTRINSIC DIE PERFORMANCE OVER FREQUENCY FOR ATTENUATOR MMIC: MINIMUM AND MAXIMUM INSERTION LOSS

BEST BOARD LAYOUT FOR SOIC-8 ATTENUATOR DEVICE

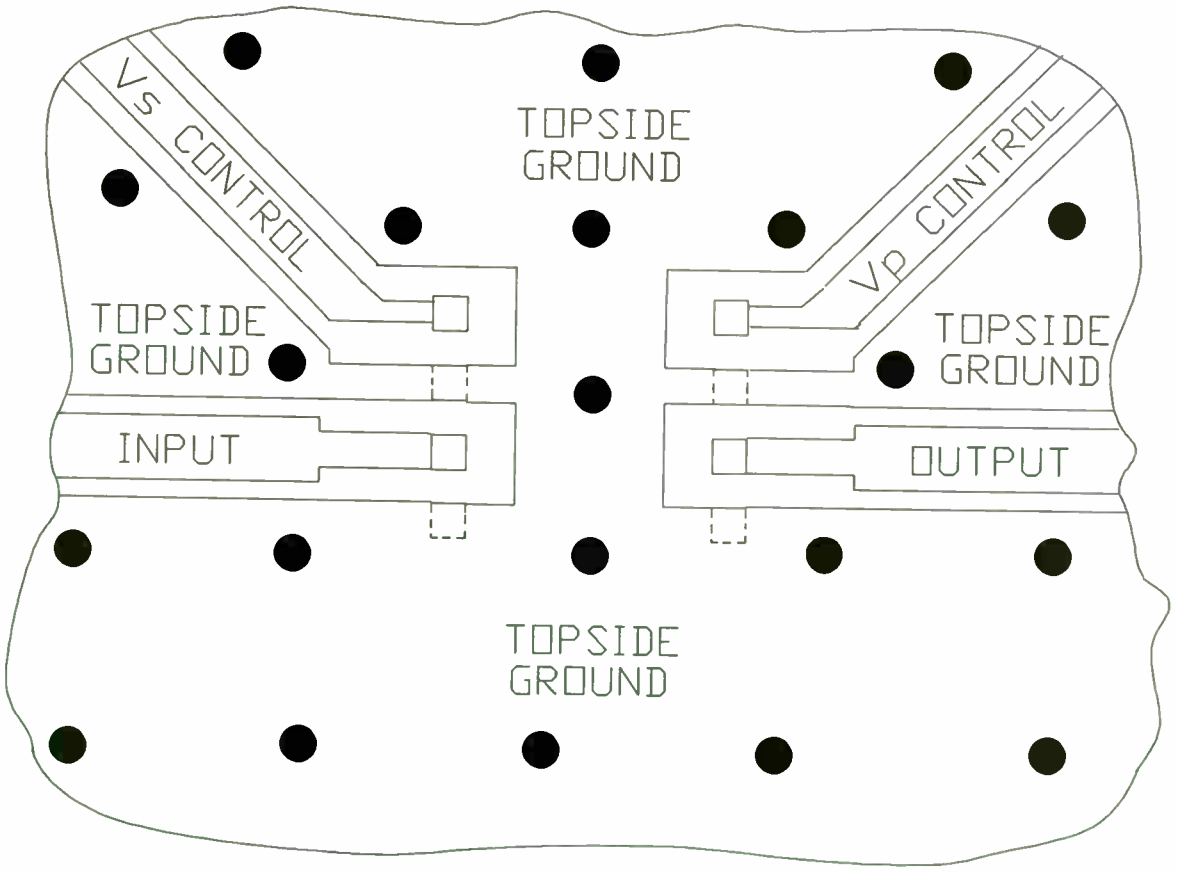


FIGURE 14. SCHEMATIC OF BEST BOARD LAYOUT USED FOR MOUNTING THE ATTENUATOR MMIC

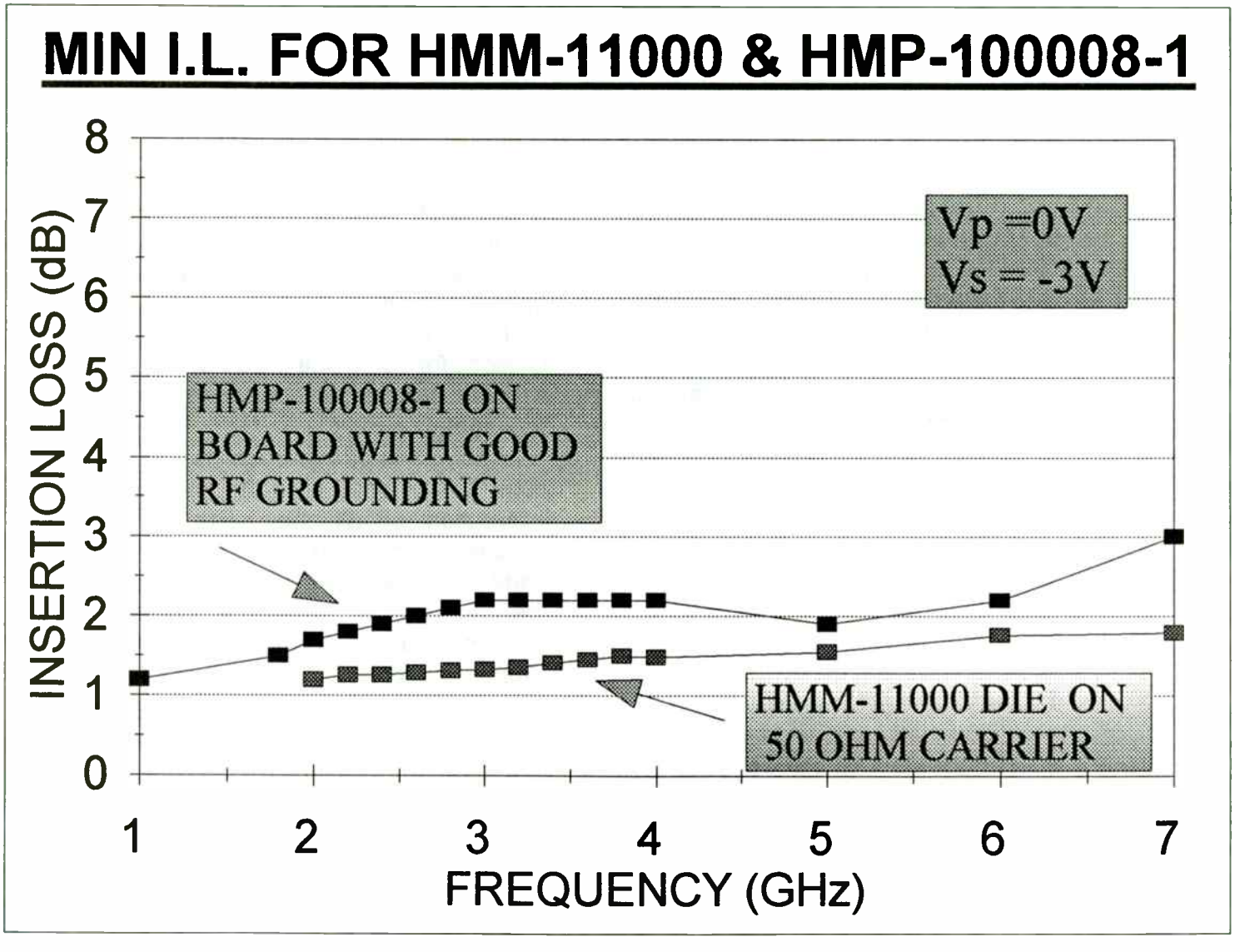


FIGURE 15. MINIMUM INSERTION LOSS PERFORMANCE OF SOIC-8 ATTENUATOR MMIC VERSUS INTRINSIC DIE PERFORMANCE

USE OF COMPUTER-AIDED ENGINEERING IN SPREAD SPECTRUM DESIGN

BY

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The purpose of this paper is to briefly describe the simulation of a direct sequence spread spectrum BPSK data link. This data link does not correspond to an actual product requirement, but rather is an example of a particular approach to this type of problem.

This paper consists of three parts:

1.First is a discussion of the various parts of a spread spectrum system that could be optimized through the use of computer simulation.

2.An area of optimization is demonstrated.

3. Finally, a design procedure is suggested as a reasonable, generic approach to general digital data link design.

This paper covers only a very brief explanation of a small part of spread spectrum technology. In addition to the material presented briefly here, the subjects of low probability of interference, inherent anti-jamming (included briefly here) and code division multiple access (CDMA) are covered elsewhere.

There are several excellent texts on the subject. A particular favorite of this author is R. C. Dixon.[1]

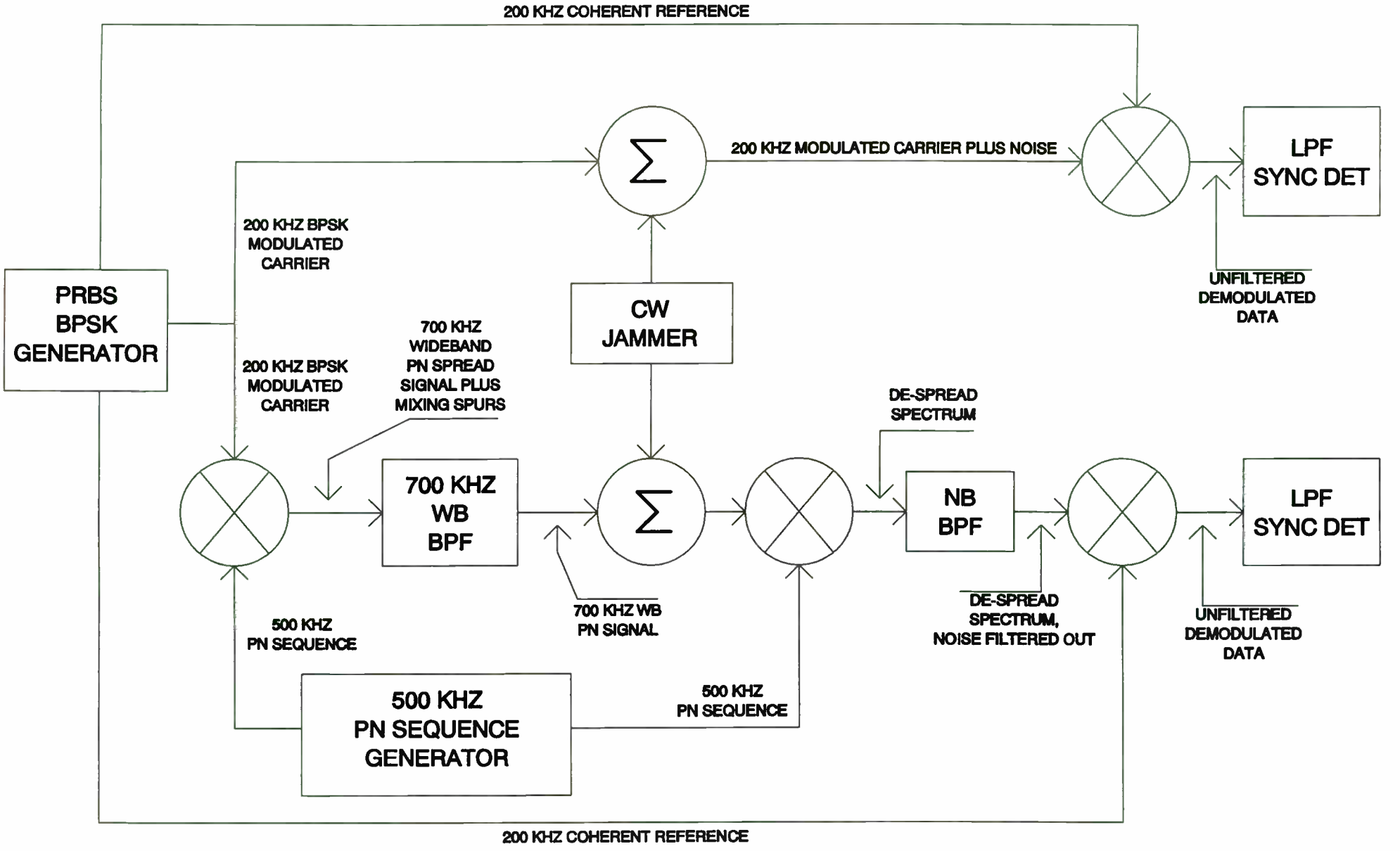
In general, there are two ways to approach a data link design; analysis and simulation. While there are reasons for using both approaches in a given design, this paper focuses on simulation.

Analysis is based upon having a complete knowledge of the complex interaction of all the parts of a system. Simulation, on the other hand, is based on the premise that the behavior of individual system elements can be described relatively simply, cascaded in a computer program, and then the composite behavior of all those parts examined.

Spread Spectrum Simulator

The spread spectrum simulator developed for this project is shown on the next page. This is simply a software model of the simpler elements of a hardware implementation of a possible data link. This simulation is performed using TESLA, from TESOFT, Inc.[2]

This data link includes both a spread spectrum path and a non spread spectrum (plain BPSK) path. These paths are then compared as



SPREAD SPECTRUM SIMULATOR

to their reliability in the presence of interference.

In examining the spread spectrum simulator, it should be noted that both the coherent carrier and the synchronized PN codes that are needed at the receiver are provided directly from the transmitter. This convenience, is, of course, a fiction, used only to simplify the simulation and reduce the simulation time. An actual, complete simulation would include code and carrier recovery systems.

The basic BPSK portion of the link is a 200 kHz modulated carrier, to which a CW jammer is added. This composite signal, BPSK plus noise, is then demodulated using the coherent 200 kHz reference. The resulting baseband signal is filtered to remove the carrier and then the data is compared to the transmitted signal.

In the spread spectrum case, the 200 kHz modulated carrier is mixed with a wideband 500 kHz PN code modulated BPSK signal. This results in a very wide signal of lower amplitude then the original signal.

The ratio of the PN code rate to the baseband signaling speed is known as the processing gain. In this case it is 10 dB. That means that a given interfering signal would need to be 10 dB higher to have the same effect on the spread spectrum signal BER as the ordinary BPSK signal BER.

When the second mixing with the 500 kHz PN signal occurs, the original PN modulated signal is "collapsed" into a signal with a bandwidth the same as the original BPSK signal. The interfering jammer, on the other hand, is spread out by the second mixing.

This spread out signal has a power density one-tenth of what it originally was, and when filtered out by the narrow-band receiver IF filter, the total interfering power is reduced to one-tenth of what it was.

Test Results

The theoretical processing gain of this system is 10 dB, and the test results were very close to this. Ordinary BER measurements were not made on this system because of the time required to accumulate sufficient bits. Instead the synchronizing of the BER receiver is used as the measurement criteria.

In modeling a spread spectrum system, it is necessary to take small enough time steps to properly simulate the high-speed code and yet take enough samples of the much slower data to make a realistic BER measurement. The data rate in this system is a reasonable 19200 bps. The PN code rate, also known as the chipping rate, is 192000 bps. The resulting spectral bandwidths (between first nulls) are 38.4 kbps for the data modulated signal and 384 kHz for the PN modulated signal.

In order to have good resolution in the simulation, the system needs to sample at 10 times the highest frequency involved. This explains the choice of 700 kHz as a carrier frequency, instead of something more realistic. It would, of course, be unlikely to build a system like this, but the data and PN signals don't know or care if they are at 700 kHz or 900 MHz (to a first order approximation).

Simulating at 900 MHz would, of course, take three orders of magnitude longer then simulating at 700 kHz. The fact that this is a spread spectrum system results in very long simulation times anyway

because the high PN code rates must be simulated, but bits are collected for analysis at the lower bit rate, in this case a factor of ten difference.

To avoid the problem of needing to collect large numbers of bits in a low-speed data link, BER analyzer synchronization was used to evaluate the system performance. The interfering jammer level is adjusted until the BER receiver no longer achieves synchronization. The points at which the BER tester no longer achieves synch in .01 seconds of simulation time is considered to be the point at which the link failed. This is obviously only a rough measurement technique.

The BPSK link failed at a Jammer/Signal ratio of -6.9 dB. The spread system failed at a jammer/signal ratio of +4.08 dB. This leads to a processing gain of 10.98 dB.

That this exceeds the theoretical best-case is only due to the coarseness and imprecision of the measurement. If a more traditional BER measurement were made, no doubt a more reasonable value would be obtained.

System Optimization

The system to this point is a very basic one. There are many components of the system that need to be evaluated and optimized. Only one of those will be examined here, because it is easy to modify and its effect is easy to demonstrate. The parameter to be optimized is the filtering of the baseband signal into the BPSK modulator.

The filtering of the modulator signals effects two things, the spectrum of the transmitted signal and the appearance of the received "eye" pattern. The received eye is the demodulated, filtered data, synchronized to the data clock signal and provides a qualitative indication of the quality of the link.

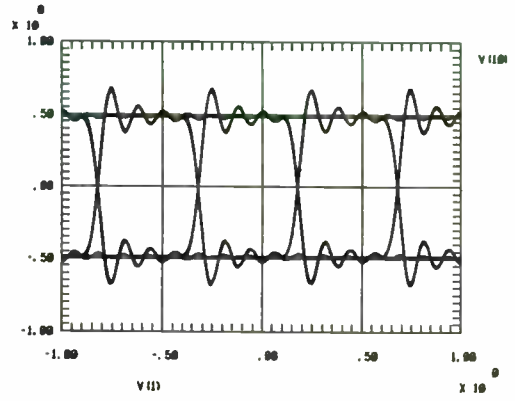
There are two basic tradeoffs involved in filtering the modulator input signal; if you decrease the bandwidth the transmitted signal becomes narrower, but the inter-symbol interference increases. If the bandwidth is increased, the inter-symbol interference is reduced, but the occupied RF bandwidth increases. This latter is usually a regulatory concern, although more so with a non-spread spectrum system, because they tend to be used in channelized portions of the spectrum.

Some of the results of trying different filter bandwidths are shown on the next page.The first eye pattern and spectrum shown is that resulting from no baseband filtering. This provides a very nice eye pattern, but fills the adjacent channels with very high levels of interference.

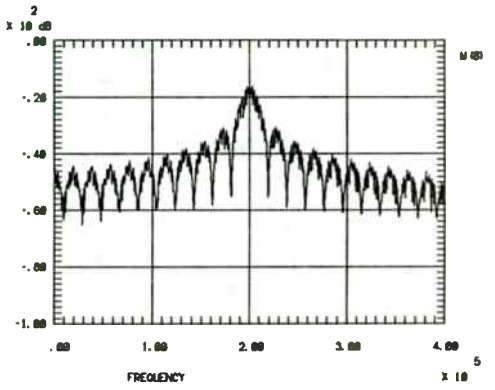
The second eye pattern and spectrum shown indicates very narrow filtering at the baseband. This particular filter is a 4 pole Gaussian-6 dB filter with a 3 kHz bandwidth. As can be seen, this is very spectrum-efficient, but the inter-symbol interference is extraordinary.

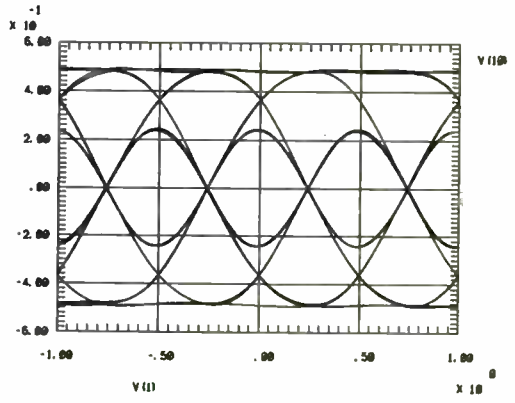
One possibility here, though, is that some form of baseband equalization[3] could remove some of the inter-symbol interference. Which could possibly result in a usable signal.

A third possibility is shown here which seems to represent a reasonable compromise between occupied RF bandwidth and inter-symbol interference. This represents



No BB Filter





Narrow
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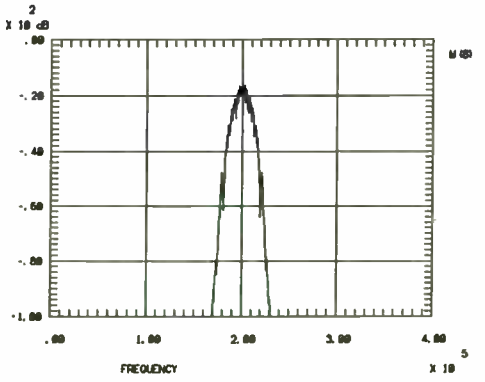

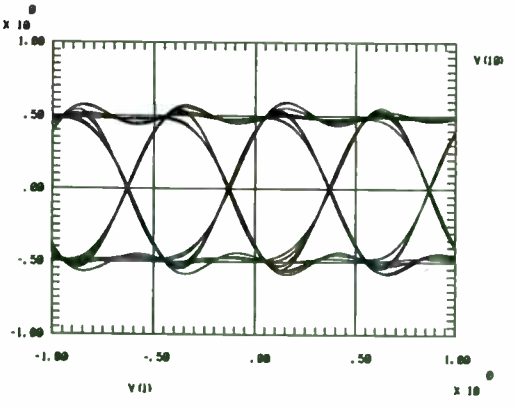

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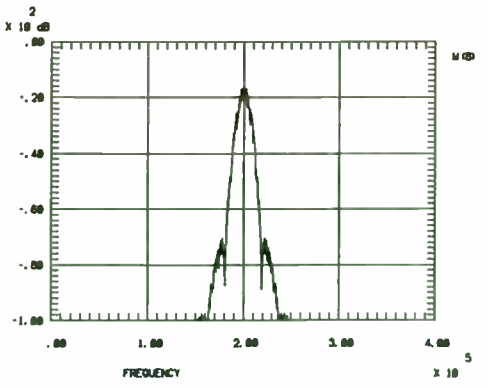

EDA applications in CDMA system design

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Government regulatory agencies worldwide are declaring rulings that are fueling the wireless revolution. In the United States, the Federal Communications Commission just carved out a 160-MHz band of the RF spectrum for a new wave of wireless devices. This will enable companies to develop a multibillion dollar industry based on a broad array of new wireless products. By the end of the decade, an estimated 60 millions Americans will subscribe to new wireless services which transfer voice, data, and video information in the 0.8-to-3-GHz frequency range.

Because wireless technology offers so many benefits, its commercial applications continue to expand--from vehicle identification and meter reading to Global Positioning System (GPS) receiver units and wireless local area networks (LANs). Wireless consumer electronics are becoming increasingly sophisticated, such as pocket phones, palm-sized computers, and laptop computers that receiver video pictures. Unlike many of today's voice communications devices, newer wireless products use digital technology to offer more privacy, better clarity, and increased data handling. Designing these complex wireless devices and systems presents new engineering challenges.

Virtually every company in the communications industry is targeting the wireless market. The companies that will succeed in this highly competitive arena must deliver high-quality, low-cost products with the fastest time to market. By capitalizing on progressive electronic design automation (EDA) software tools and implementing efficient design methodologies, companies can gain the competitive advantage to become market leaders. This article reviews the use of EDA tools in the design of two key elements of a digital code division multiple access (CDMA) receiver: a clock/data-recovery circuit and a sliding block correlator.

CDMA Systems

CDMA technology is the latest in a series of commercial-use signal-modulation schemes that aim to include as many individual channels as possible in a single frequency bandwidth. Perhaps more familiar are frequency-division and time-division multiplexing techniques

which break channels into discrete frequency or time slots before reconstitution at the receiver. CDMA, through its use of spread-spectrum modulation techniques, improves signal-to-noise ratios by increasing the signal bandwidth. Because the transmitted signal is intentionally spread over a greater bandwidth, the transmission has greater immunity to interference from narrow-band signals. The benefits in military applications, where frequency-hopping spread-spectrum techniques originated, are in increased jamming immunity and security. In commercial digital applications, the increased security is a benefit in voice and data communications as is the increased channel capacity inherent in spread-spectrum techniques. The term code division in CDMA is derived from the "secret" code that is used to modulate the individual channels. This code is then used by the receiver to extract its specific channel from the noise-like nature of the broadcast spectrum which contains multiple channels spread across the same bandwidth.

The most widely used spread-spectrum systems today use a technique called direct-sequence modulation. A typical system is shown in Figure 1. In direct sequence, the data signal is multiplied by the digital code signal which has a much higher bit rate than the information signal. The coding signal is commonly referred to as a PN or PRN (pseudorandom noise) code. To distinguish between the information and the code signals, the digital bits of the PN signal are termed chips. The spectrum spreading is accomplished when the coded chip sequence of the PN signal is multiplied by the original data bits. Since multiplication in the time domain corresponds to convolution in the frequency domain, it follows that the broader frequency spectrum of the coded chip sequence spreads the original data spectrum. This spread spectrum signal is then upconverted and transmitted. The difficulty arises at the receiver when an internally-generated PN code sequence must be aligned (or correlated) with the incoming PN code chip sequence to enable proper demodulation (or despreading) of the desired signal and spreading of any undesired signals.

For direct-sequence spread-spectrum systems, research and development efforts have been focused on developing and improving synchronizing techniques. Direct-sequence spread-spectrum systems require the coded signal arriving at the receiver to be accurately

timed in both its code pattern position and its rate of chip generation with respect to the receiver's reference code. Once the received PN code is synchronized with the PN code in the receiver the received data can then be despread. Since the despread data has been corrupted by noise, it is essential to extract a clock from this data and use this clock to trigger a digital gate which makes the hard decision as to the true bit state. This operation is accomplished using a clock-recovery and data-detection circuit. Such a circuit is often termed "bit-synchronization" circuitry. These two processes are illustrated in the design examples featured in this paper.

EDA Applications

A CDMA system's implementation is a hybrid of RF analog and digital components and until now commercial software capable of efficiently analyzing the complete performance of carrier- and clock-recovery systems has not been widely available. At best, engineers could use software to predict the performance of only small portions of these systems. Complete system performance analysis required taking actual measurements on the bench combined with the time-consuming task of integrating information from a series of point-solution software design tools.

The Communications Design Suite (CDS) from HP-EEsof in the first commercially available software package that integrates the analysis of combined RF analog and digital networks specifically used in wireless systems. Series IV, Version 5.0 of the CDS includes a new discrete time engine that performs a time-domain analysis of combined analog and digital networks significantly faster than a SPICE-type simulator. This is achieved through envelope analysis and uses time steps more closely related to the data signal whereas SPICE is required to track at the carrier frequency. This technique was used to design the clock-data-recovery circuit and the sliding block correlator demonstrated in the following examples.

Designing Clock/Data Recovery Circuits

In wireless communications systems, the receiver's local carrier frequency must be synchronized with the transmitter's carrier for accurate signal demodulation. This can be accomplished using circuits such as Costas-loop carrier-recovery networks and these circuits can be easily analyzed with the CDS. In a digital system, additional complex circuitry is required to extract a clock from the baseband data. This clock is then used to trigger a digital gate (data detector) which makes the hard decision as to whether the

received bit is a one or a zero. The clock-recovery circuits, in conjunction with the data detection circuitry, forms the heart of a digital communications receiver.

The top-level block diagram for a PLL-based clock-recovery system is shown in Figure 2. This circuit also incorporates a data-recovery network. This system has been designed to recover a 1.5-MHz clock signal from a 1.5-Mb/s pseudorandom input data stream. All the elements shown here, as well as additional elements in the PLL subnetwork, are included in the CDS' element set.

After RF demodulation, a random data stream associated with the transmitted data is input into the network in Figure 2. Averaging this signal and analyzing its frequency would result in a frequency exactly half that of the required clock signal because each digital zero-one sequence corresponds to two clock bits. The ideal lowpass raised-cosine (Nyquist) filter with a corner frequency of 0.75 MHz attenuates the higher harmonics in order to band-limit the data. The subsequent frequency-doubler network comprising the data splitter and the multiplier generates the required 1.5-MHz tone which is extracted by the PLL. The limiter just prior to the PLL is used to square up the signal, since the PLL uses a digital phase-detector element. As well as the digital phase detector, the PLL subnetwork also features a VCO and a loop filter which in this case is specified by a complex pole-zero representation which offers significant simulation speed improvements over a lumped circuit representation.

The PLL produces the system clock and a signal splitter routes the clock to the sample-and-hold/integrate-and-dump configuration shown in Figure 2. This circuit therefore acts as a combined clock-recovery and data-detection network.

Sliding Block Correlator

Direct-sequence spread-spectrum systems require the coded signal arriving at the receiver to be accurately timed in both its code pattern position and its rate of chip generation with respect to the receiver's reference code. One popular method of performing this acquisition uses a system called the sliding block correlator. This system performs partial correlation by comparing N chips entering the receiver with N chips generated internally in the receiver. An example of a sliding block correlator is shown in Figure 4. All of the digital logic components shown are included in the Series IV Combinational Logic Element set.

If the received signal includes a channel that is destined for this particular receiver, there will be a channel modulated by the PN code generated in the receiver. A certain setup time is required during which the sliding correlator's internal PN sequence is synchronized with the incoming PN sequence. The XOR gate at the receiver's input is used to compare each received chip with a chip generated by the receiver's own internal Linear Feedback Shift Register, which generates the identical PN code as the transmitter. When the two chip sequences are insufficiently correlated, a large number of "0" states appears at the output of this XOR gate. Thus, when there is insufficient correlation between the chip sequences, a large number of 1's will enter the integrate-and-dump element. The integrate-and-dump element's output is then connected to the input of the Schmitt trigger. The integration time for the correlated chip sequence is controlled by the divide-by-N counter element. In this design, N = 127. Thus, the integrator determines the average value of each block of 127 chips, which is compared in the XOR gate.

When there is insufficient correlation, the output exceeds the upper threshold level of the Schmitt trigger. The remaining logic circuitry then delays the internally-generated PN chip sequence by half a chip. This process continues until the internally-generated and received PN chip sequences are correlated. The process of delaying the internally-generated PN chip sequence by half a chip per each block of 127 chips is analogous to "sliding" this block of chips with respect to the incoming chip sequence, giving rise to the name sliding block correlator.

The operation of the sliding block correlator can be verified by comparing the time-domain waveforms of both the received and internally-generated PN chip sequences. The initial error between these two signals can be observed by measuring the two signals from t = 0 to t = 15 usec, as shown in FIgure 4. The initial error is approximately 1.5 chips.

Figure 5 shows the increased alignment between the internally-generated PN code sequence and the received PN sequence. Although in the range of 505 to 509 usec correlation has been achieved, by t = 515 usec, the sliding block correlator has incrementally delayed the internally-generated PN code sequence so that it is in closer alignment with the received PN sequence. Once correlation is achieved, the receiver is ready to despread the desired data signal.

The sliding block correlator demonstrated here incrementally improved the correlation between the received and internally-generated

PN chip sequences by half a chip per iteration. Therefore it is possible for the correlation at this stage to be off by up to half a chip. In practice, after maximum correlation is achieved with a sliding block correlator, a delay locked loop takes over and makes finer, continuous (as opposed to digital steps) adjustments to guarantee perfect correlation.

EDA for Wireless System Design

The use of digital techniques in commercial wireless communications is becoming prevalent. At the same time, the needs to reduce manufacturing costs as well as unit size, weight, and power consumption dictate that all the DSP, digital, analog, and RF sections of a design are implemented on the same printed circuit board. It follows that design teams working on these systems, formed from groups of engineers from each discipline, need a unified design tools suite that can handle every aspect of the design. The design examples presented here show how a modern EDA tools can meet the various aspects of a spread-spectrum receiver design. Consequently, as digital techniques continue to merge with traditional analog designs, so too are digital techniques being incorporated into wireless EDA tools.

CDMA Receiver

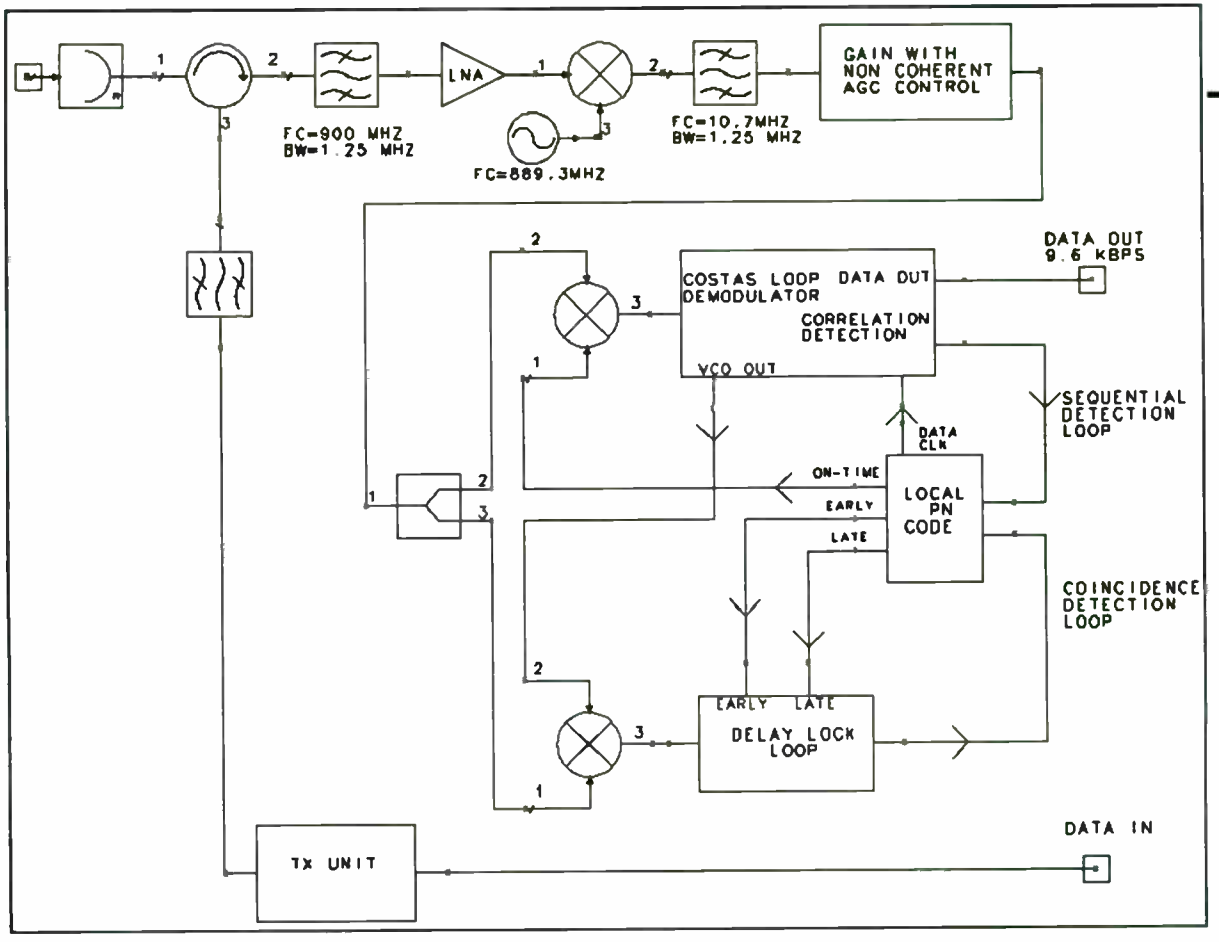

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Figure 1: A typical direct sequence spread spectrum receiver used in CDMA applications

Clock-recovery circuit

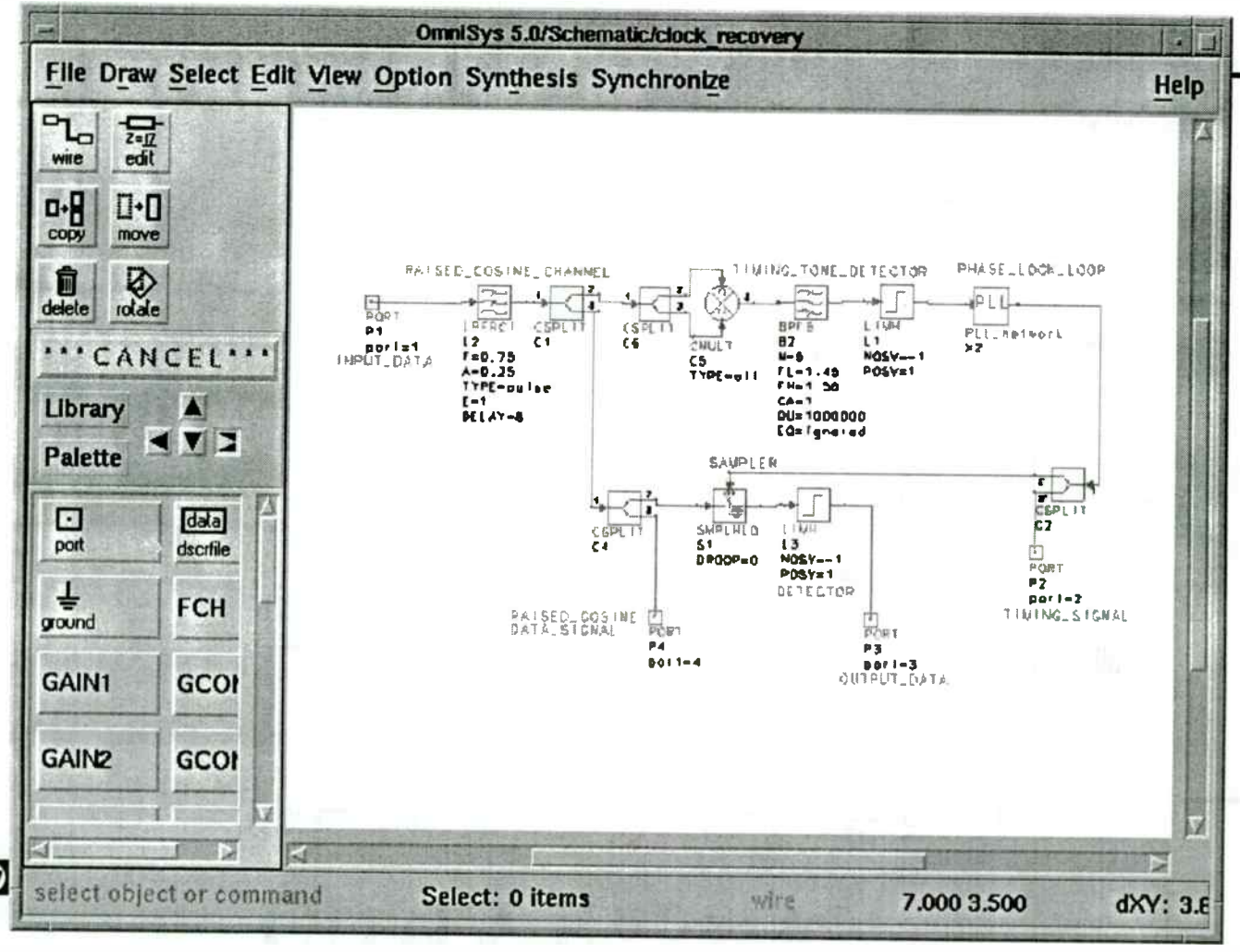

Figure 2. The clock/data recovery network used in the spread spectrum receiver

The PLL sub-network

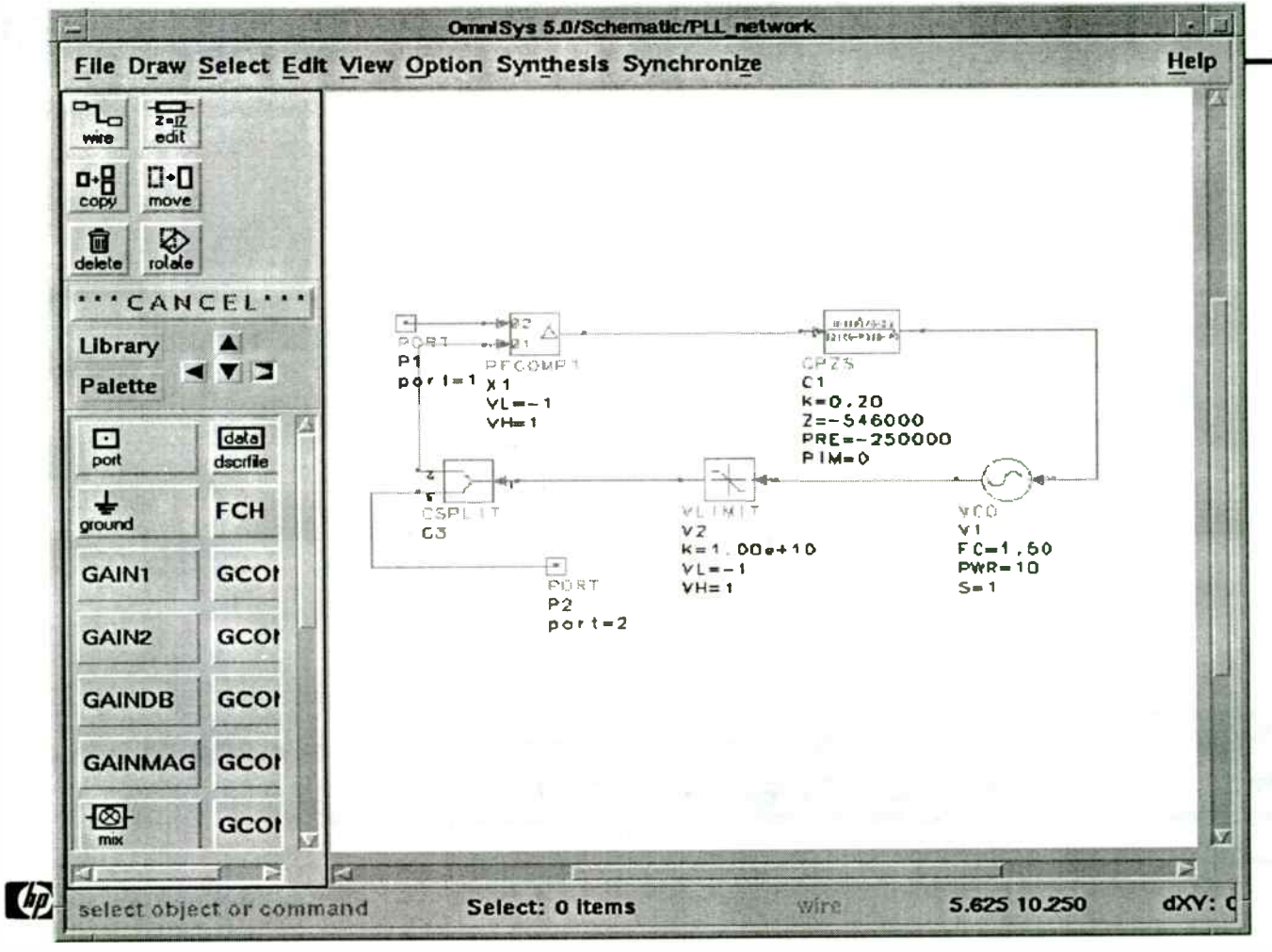

Figure 3:

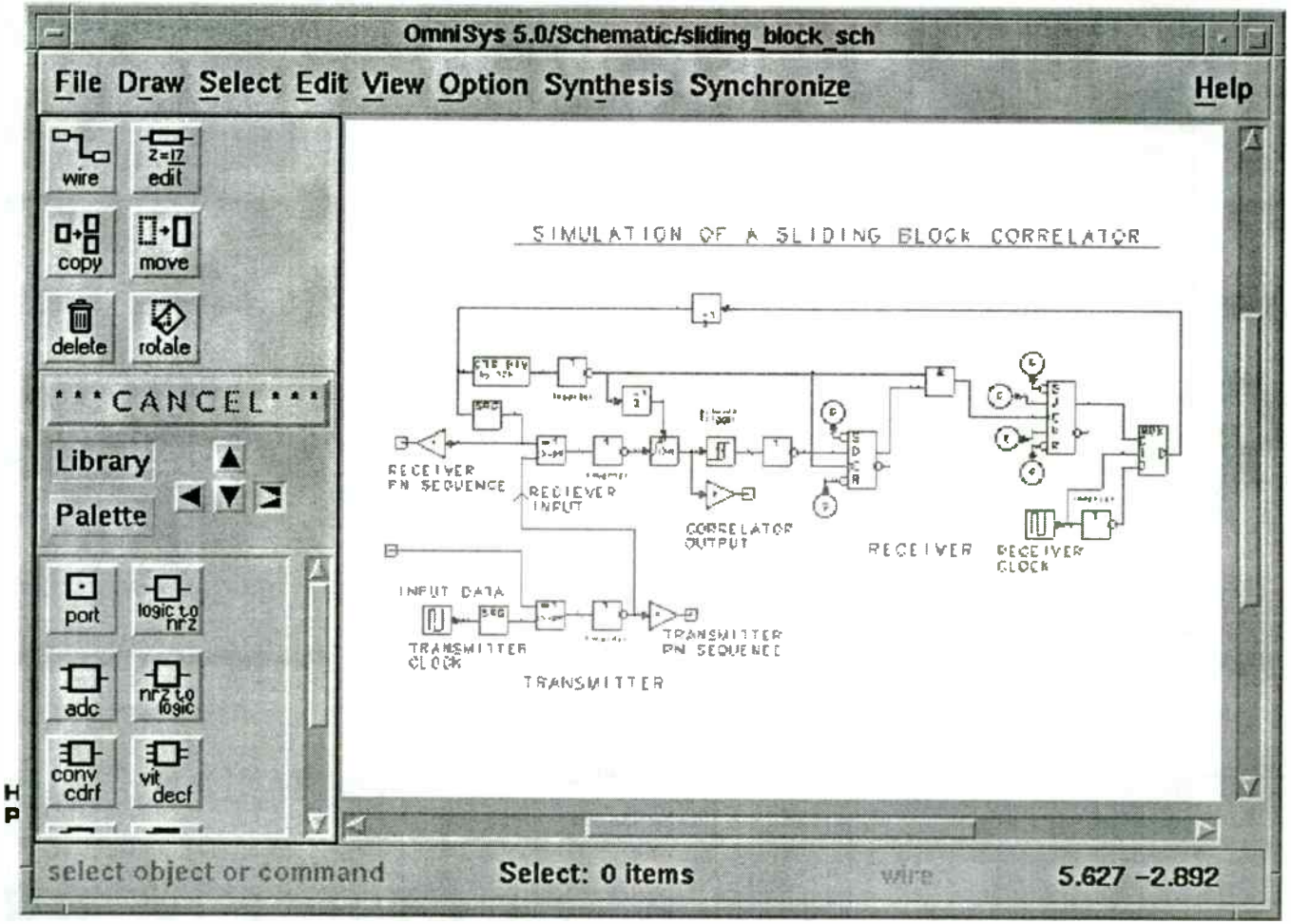

Figure 4. Schematic for a sliding block correlator. This design compares a sequence of 127 chips at the input with the same chip sequence generated internally with a Linear Feedback Shift Register.

Figure 5.

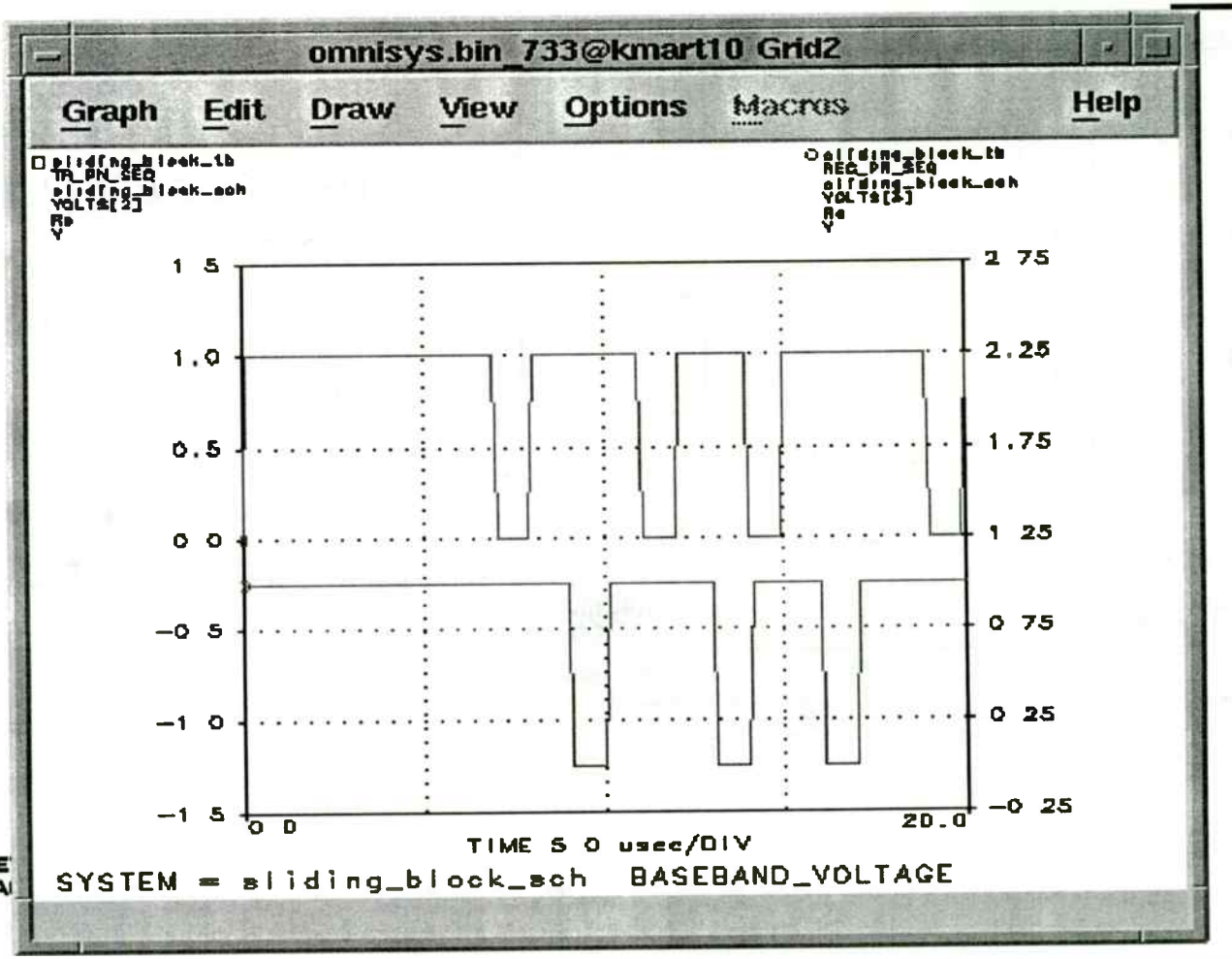

Figure 5. The initial error between the received PN code chip sequence and the PN code generated internally in the receiver is 1.5 chips.

The correlation process

After 127 more chips are evaluated, the internally-generated chip sequence is shifted to be in perfect correlation with the received chip sequence.

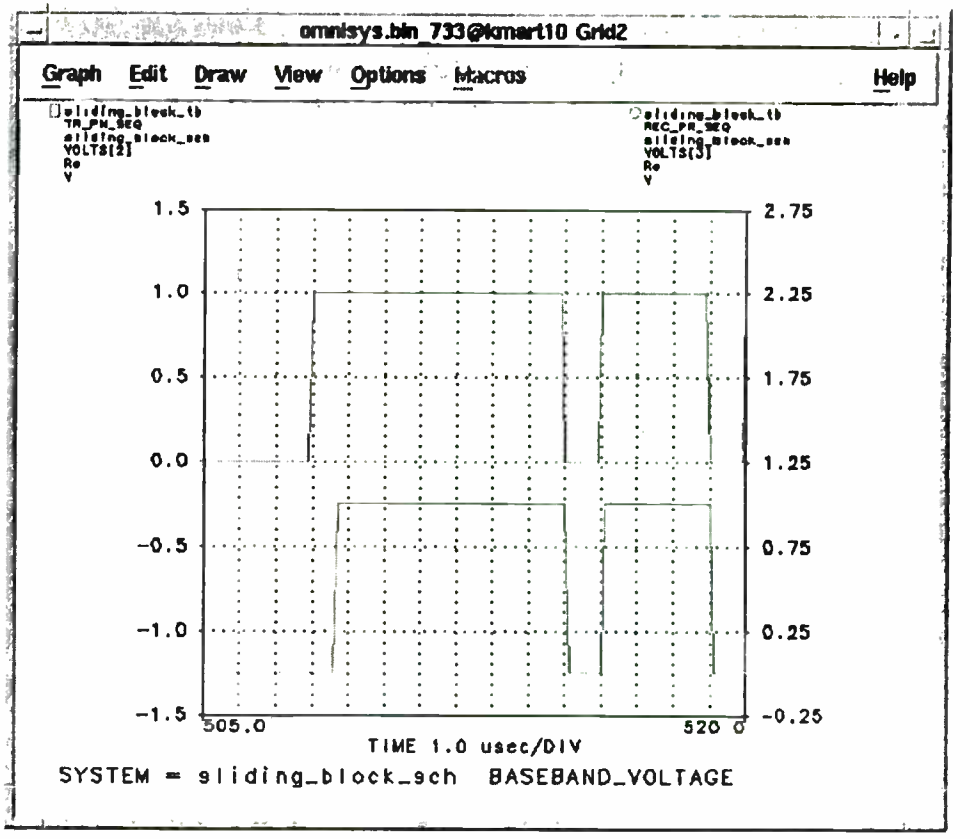

Figure 6. By t = 500 usec, there is sufficient correlation to despread the desired signal.

A Transmission Line Model for Single Layer Capacitors

M. Ingalls, P. Romanowski and G. Kent

November 18, 1993

Abstract

A transmission line model for single layer capacitors (SLCs) is presented. The model uses physical dimensions, the dielectric constant, dissipation factor and series resistance as input variables to predict the input impedance (Z_i) from 1 to 26.5 GHz. An algorithm for computer programmers is presented. The model is compared with measured data.

The single layer capacitor equivalent circuit

The single layer capacitor (SLC) equivalent circuit is based on an open ended parallel plate transmission line.[1] From this viewpoint, the input impedance, Z_i, is:

$$Z_i = Z_c \coth[(\alpha + j\beta)\ell] \qquad (1)$$

where Z_C = characteristic impedance
α = attenuation per unit length
β = phase shift per unit length
ℓ = effective length

Two simplifying assumptions are made. First, the modeled SLC is constructed of low loss dielectric. Second, its electrodes are good *in situ* conductors. When these assumptions are valid, the characteristic impedance is real and constant, and the phase shift is a linear function of frequency.

The characteristic impedance of a low loss parallel plate transmission line is:

$$Z_c = 120\pi\sqrt{\frac{\mu_r}{\varepsilon_r}}\frac{t}{w} \text{ or } \sqrt{\frac{L}{C}} \qquad (2)$$

where t = distance separating the conductors
w = width of the conductors
μ_r = relative magnetic permeability
ε_r = relative dielectric permittivity
L = equivalent inductance of an identical short circuited transmission line
C = equivalent capacitance of the open circuited transmission line

Since $\mu_r = 1$ for SLCs, the phase shift per unit length is:

$$\beta = \omega\sqrt{\mu_0\varepsilon_0}\sqrt{\varepsilon_r} \qquad (3)$$

where ω = (angular) frequency of interest,
μ_0, ε_0 = permeability and permittivity of free space.

The attenuation per unit length is approximately:

$$\alpha \cong \frac{1}{2\ell}\left(R\sqrt{\frac{C}{L}} + G\sqrt{\frac{L}{C}}\right) \qquad (4a)$$

where $R\sqrt{\frac{C}{L}}$ = total conductor loss
$G\sqrt{\frac{L}{C}}$ = total dielectric loss

At 1 GHz, conductor losses become large enough and dielectric losses become small enough that:

$$\alpha\big|_{1GHz} \approx \frac{R/\ell}{2Z_c}, \quad R\sqrt{\frac{C}{L}} \gg G\sqrt{\frac{L}{C}} \qquad (4b)$$

At 1 MHz, dielectric losses dominate. Since G can be expressed in terms of df, C, and ω, and since β can be expressed in terms of ω, L, and C, the SLC's attenuation at 1 MHz is very nearly:

$$\alpha\big|_{1MHz} \approx \frac{\beta}{2} df, \quad G\sqrt{\frac{L}{C}} \gg R\sqrt{\frac{C}{L}} \qquad (4c)$$

Equations (4a, b, & c) can now be used to relate attenuation to measurable parameters, given two final notes. First, the resonant line technique historically used for measuring a capacitor's series resistance drives the capacitor from the center, while the capacitor mounted above a ground plane is excited from one end.[2] The different driving point causes measured series resistance to be *one half* the value indicated in equation (4). Second, conductor losses increase due to skin depth above 1 GHz. Given this information,

$$\alpha \equiv \frac{R/\ell}{Z_c}\sqrt{\frac{f}{1GHz}} + \frac{\beta}{2} df \qquad (4)$$

Where R = series resistance value measured at 1GHz using a resonant coaxial line.

Dielectric permittivity

At bridge frequencies (≤1 MHz) the measured capacitance (C) and the physical dimensions of the SLC are related by the equation:

$$K \equiv \frac{Ct}{\varepsilon_0 \ell w} \qquad (5)$$

where K = relative dielectric 'constant' for quasi-static electric field conditions

Dielectrometer measurements show that low loss dielectrics are indeed sensibly constant with frequency.[3]

At the lowest parallel resonance frequency (f_0), $\beta \equiv \pi/\ell$. Equation (3) yields:

$$\varepsilon_r = \frac{1}{(2\ell f_0)^2} \cdot \frac{1}{\mu_0 \varepsilon_0} \qquad (6)$$

Logically, measured K and derived ε_r should equate. However, f_0 measurements on capacitors of various dielectric materials and linear dimensions show they do not. The apparent difference can be assigned to the electric energy in the fringing fields.

By varying the parameters ℓ, w, t, and K, and analyzing the results, an empirical relationship between K and ε_r may be written[4]:

$$\varepsilon_r\big|_{t,w} \equiv \frac{(1+\eta)}{(1+\xi)} K \qquad (7)$$

Where ξ is a function of $t \div w$
η is a function of ξ and K

The functions ξ and η may be approximated by:

$$\xi \cong 0.222\sqrt{\frac{t}{w}} + 0.947\frac{t}{w} \qquad (8)$$

$$\eta = \xi\left[0.06 + \frac{0.94}{K}\right] \qquad (9)$$

Experimental observations

Insertion loss and return loss were measured by Hewlett Packard 8510 (vector) and Wiltron 5600 (scalar) network analyzers. All devices tested were mounted on 50Ω microstrip transmission lines.

Vector measurements were made on twelve different SLC designs. Samples were swept from 0.1 to 7.5 GHz in 0.1 GHz steps and from 2 to

18 GHz in 0.5 GHz steps. The SLCs were conductive epoxied to 0.0143 inch wide traces on 0.015 inch thick alumina. Two gold wire bonds were applied from the top plate of the SLC across a 0.005 inch gap to the trace.

The microstrip, SLC, wirebond network was mounted in an Intercontinental Microwave de-embedding fixture. A through/reflect/load (TRL) calibration scheme was used.

Scalar measurements were made on twenty-one different SLC designs. Samples were swept from 0.01 to 26.5 GHz in 0.026 GHz steps. The SLCs were soldered to 0.025 inch wide traces on 0.025 inch thick alumina using indium solder. A silver ribbon lead, 0.025 inches wide and 0.065 inches long, was formed to match the height difference between SLC and microstrip and indium soldered to the SLC and microstrip, bridging a 0.005 inch gap. An open/short/through calibration was used, with each microstrip test fixture having its own through calibration.

From the large quantity of data, three general observations can be made: 1) Resonance effects as small as 0.5 dB could be detected with the vector analyzer, but not with the scalar analyzer. 2) When the width of the SLC did not closely match the microstrip width, measured and modeled performance did not agree well at high frequency. 3) Low frequency (<1 GHz) measurements agree with modeled behavior when df$\langle\langle$ 0.01, but not when df $\rangle$ 0.01.

The SLC model

The purpose of these equations is to relate measurable characteristics to SLC performance over a broad frequency range. Figure 1 depicts an algorithm for converting measured data to modeled impedance. Figure 2 shows the model written in Mathcad® 4.0.

The first line of figure two contains the constants of the capacitor (*l*, *w*, and *t* are in inches; *K* and *df* are dimensionless; and *R* is in Ohms).

The second line shows frequency (*f*) in units of 0.1 GHz; the formula for 1 MHz capacitance (C_0); and the calculated value of C_0. (The capacitance formula is a rearrangement of equation five with ε_0 expressed in pF/inch.)

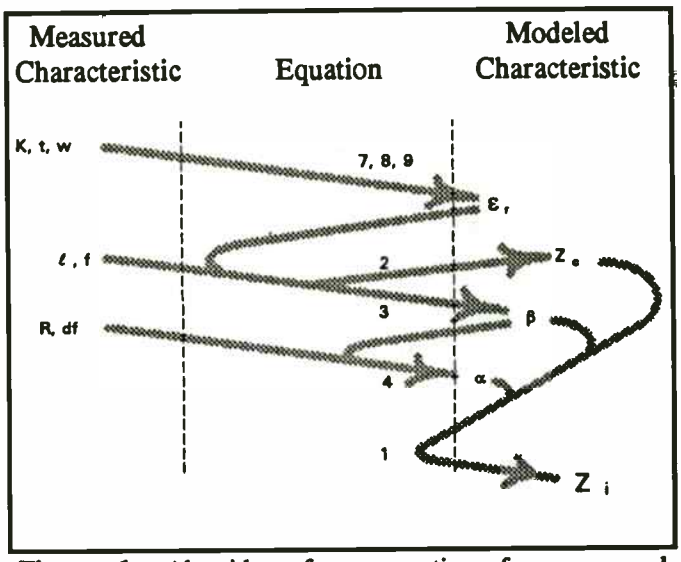

Figure 1. Algorithm for converting frequency and measurable characteristics *K, t, w, ℓ, R, and df* to Z_i

The third line shows the derivation of ε_r from K, t, and w.

Line four begins with characteristic impedance (Z_c). The next two equations describe the first parallel resonance frequency (f_0) and the total phase shift along the capacitor (B_f). The constant 5.906 is $1/\left(2\sqrt{\mu_0\varepsilon_0}\right)$, expressed in GHz-inches.

Line five shows the total attenuation along the capacitor and the input impedance. (Note in the equations for B_f and A_f that frequency has been normalized back to units of GHz. The reason for using units of 0.1 GHz is to provide that level of resolution for plots.)

$$l := .015 \quad w := .015 \quad t := .004 \quad K := 7500 \quad df := .025 \quad R := .2$$

$$f := 1..180 \qquad C_0 := .225 K \cdot l \cdot \frac{w}{t} \qquad C_0 = 94.922$$

$$\xi := .222\sqrt{\frac{t}{w}} + .947\frac{t}{w} \qquad \eta := \xi \cdot \left(.06 + \frac{.94}{K}\right) \qquad \varepsilon_r := K \cdot \frac{1+\eta}{1+\xi}$$

$$Z_c := 120\pi \cdot \frac{t}{w \cdot \sqrt{\varepsilon_r}} \qquad f_0 := \frac{5.906}{l \cdot \sqrt{\varepsilon_r}} \qquad B_f := \sqrt{\pi \cdot \frac{f}{10 f_0}}$$

$$A_f := \left[\left(\frac{R}{Z_c} \cdot \sqrt{\frac{f}{10}}\right) + \frac{B_f}{2} \cdot df\right] \qquad Z_{i_f} := Z_c \cdot \coth\left(A_f + B_f \cdot j\right)$$

Figure 2. Di-cap model written in Mathcad® 4.0

Figure 3 is a modeled insertion loss (S_{21}) plot of a series connected SLC, vendor part number D25BU101K5PX. The physical parameters of this device are shown in the first line of figure 2 (physical dimensions are in inches). Modeled Z_c and f_0 are respectively 1.34Ω and 5.26 GHz.

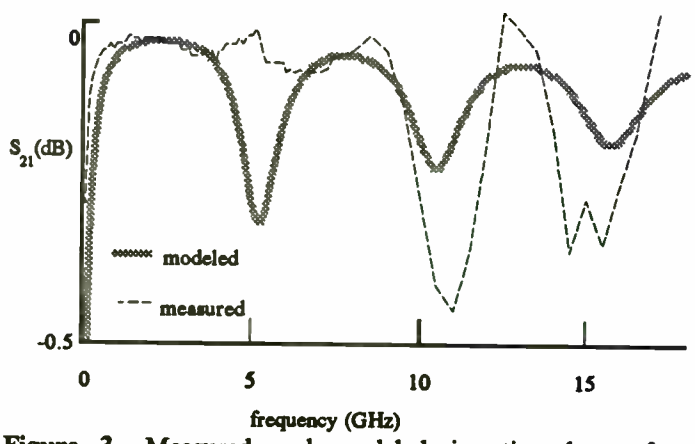

Figure 3. Measured and modeled insertion loss of D15BU101K5PX, plotted in Mathcad® 4.0

Figure 4 is a model of the insertion loss of series connected SLC D25NR6R8J5PX. Its physical parameters are: ℓ=0.030", w=0.025", t= 0.0038", K=155, df=0.0015, and R=0.02Ω.

Figure 5 depicts measured versus modeled behavior of SLC D15BG100K5PX. Its physical parameters are: ℓ=.015", w=.015", t=.0044", K=900, df=.015, R=.5Ω. Its 1 MHz capacitance is 10.36 pF.

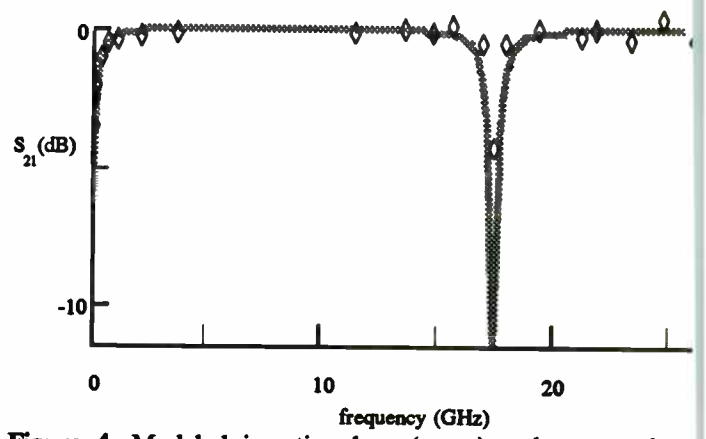

Figure 4. Modeled insertion loss (curve) and measured data points (diamonds) for D25NR6R8J5PX, plotted in Mathcad® 4.0

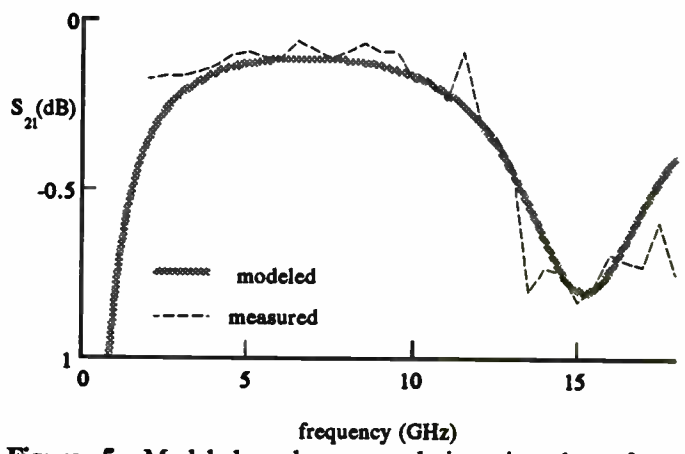

Figure 5. Modeled and measured insertion loss for D15BG100K5PX, plotted in Mathcad® 4.0.

Figure 6 again depicts the behavior of a D15BG100K5PX SLC. This device was made from the same ceramic formulation as the SLC in figure 5, except it is thinner (t = .0036") and shorter (ℓ = .012"). Its 1 MHz capacitance is 10.13 pF. Note the difference in f_0 of these two devices. Evidently the model and the measured data show the primary physical parameters of ℓ, w, t, and K accurately predict an SLC's behavior while its capacitance value does not.

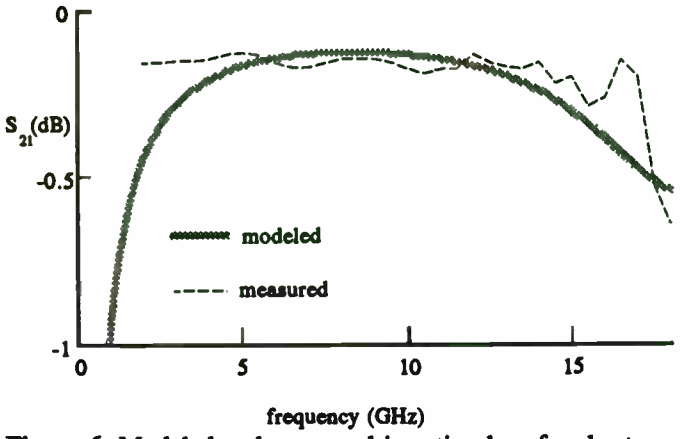

Figure 6. Modeled and measured insertion loss for shorter version of D15BG100K5PX, plotted in Mathcad® 4.0.

Conclusion

Transmission line theory, with adjustments for fringing fields, was applied to single layer capacitors. Electrical characteristics of individual capacitors were related back to the physical constants of the SLC. The resulting equations predicted the behavior of SLCs over a broad frequency range. Therefore the model, with physical constants supplied by the SLC manufacturer, is an effective tool for the microwave engineer.

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[1]G. Kent and M. Ingalls, "The behavior of parallel plate capacitors on microstrip," *Hybrid Circuit Technol.*, Lake Publishing Corp., Libertyville, IL., Nov. 1988

[2]M. Ingalls and G. Kent, "Measurement of the characteristics of high-Q ceramic capacitors," *IEEE trans. on Comp., Hybrids and Manuf. Technol.*, vol. CHMT-12, No. 4, Dec. 1987.

[3]G. Kent, "An evanescent-mode tester for ceramic dielectric substrates," *IEEE Trans, Microwave Theory Tech.*, vol. MTT 31, Oct. 1988.

[4]G. Kent, "Di-cap characteristics," Engineering Bulletin EB-0017, Dielectric Laboratories, Cazenovia, NY, June 1989.

RF Printed Circuit Layouts:
A practical tutorial for wireless applications

Allan Coon, Senior Applications Engineer,
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FAX: (214) 387-8148.

This paper will review practical design approaches to typical circuits used in wireless applications. The presentation will cover meeting performance goals within a given cost budget.

Automotive Electronics/Satellite Communications

Session Chairperson: Raymond Camisa,
David Sarnoff Research Center (Princeton, NJ)

TWO VEHICULAR ANTENNAS FOR THE MOBILE SATELLITE SERVICE

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INTRODUCTION

Plans for a Mobile Satellite Service are underway which will provide seamless coverage to mobile and fixed telephone users within the continental United States. The satellites used will be geostationary with an L-band downlink. As a consequence, equipment designers and manufacturers are pressed to provide compact, low cost mobile terminals suitable for a commercial market. An important element in the success of this service are the mobile antennas and how they integrate both functionally and *visually* with the mobile equipment terminal. Vehicular antennas operating at L-band and providing circular polarization tend to be on the large side, so they must be designed to appear non-obtrusive to the end user who must be willing to put one on her/his car. Two vehicular antenna are considered in this paper which address both service and market requirements.

The first of the antennas presented is a quadrifilar mast which uses a manual mechanical adjustment to steer its omnidirectional azimuth beam to different elevation coverage; the second is a low profile disk antenna which uses an external tracking system to mechanically steer its shaped elevation beam in azimuth. Some brief background on the theory, design, and performance for each of these antennas will be described.

QUADRIFILAR MAST ANTENNA

The mast antenna is a multi-turn quadrifilar helix antenna fed in phase rotation at its base for circular polarization. Designed in the backfire mode, the quadrifilar is omni-directional in azimuth with directive beams in the elevation plane, making it particularly useful as a mobile vehicular antenna accessing stationary satellites. By proper selection of height, diameter, helix pitch and so on, it is possible to achieve 8 dBic of antenna gain, which is a lower limit requirement for the MSAT mobile terminals. Since its elevation beam is too directive to provide complete coverage, a mechanical feature has been incorporated into the mast design which allows its elevation beam to be scanned between zenith and horizon as becomes necessary. The helix elements are fixed at the mast base then suspended along their length and attached at the top to a rotatable knob. Turning the knob in on direction or the other adds or reduces the number of turns in each helix, which changes their pitch angle causing a change in the launch angle of the elevation beam. Figure 1 shows the outline of the mast antenna.

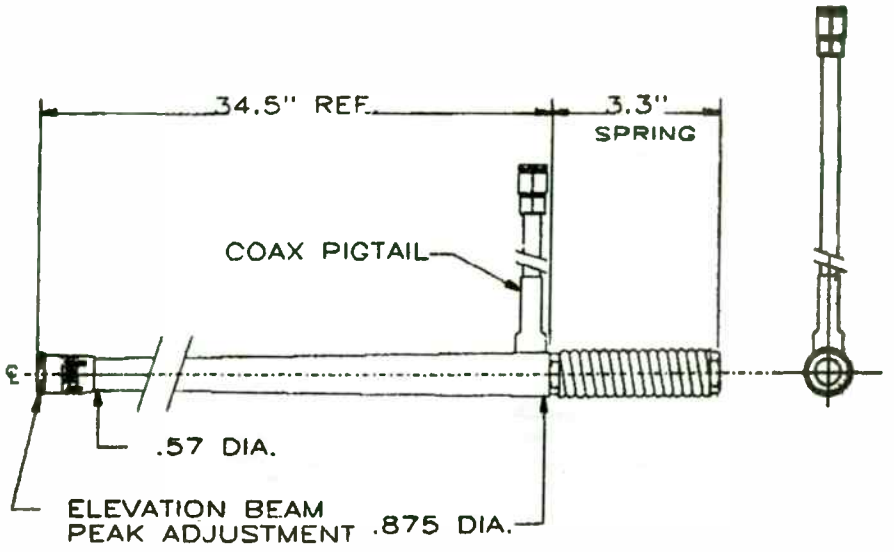

Figure 1 Outline drawing of mast antenna.

A characteristic exists within this antenna which can potentially jeopardize its utility as a medium gain omni if not properly accounted for. As with all traveling wave antennas, the location of the peak radiation beam varies with frequency, giving rise to a phenomenon called "frequency scanning". This results in an unfortunate reduction in antenna gain between the transmit and receiving modes of operation. This reduction in gain has been termed "cross-over loss". The mast described in this paper has been optimized to compensate for frequency scanning.

MAST PROTOTYPE CONSTRUCTION AND DESIGN

Radome

A fiberglass radome with 0.030 inch wall thickness and a 7/8 inch base diameter tapering to 0.625 inches over a 33 inch length was chosen to house the antenna, partly because these are readily available as salt water fishing rod blanks. The optimum helix diameter has been determined to be about 0.40 inches with an axial length of 30 inches, so the elements are easily accommodated within the radome. The microstrip feeding circuitry formed into a cylindrical shape to fit within the radome as well. The helix elements/combiner circuit is described in the following section.

Feeding Circuit and Helix Elements

The power combiner and four helix elements form a continuous circuit of etched copper on 5 mil Mylar film (see Figure 2). An important feature of the Mylar film is that it permits the helix elements to be suspended in developed form, and carries pitch change uniformly along the helix length during adjustment. The combiner section of the circuit is sandwiched between two tubular sections of 0.063 inch wall Polypropylene, which when overlaid act as microstrip super- and substrates. Sliding this assembly over a brass rod for a ground plane completes the circuit. A coaxial line soldered to the microstrip power combiner provides external RF access.

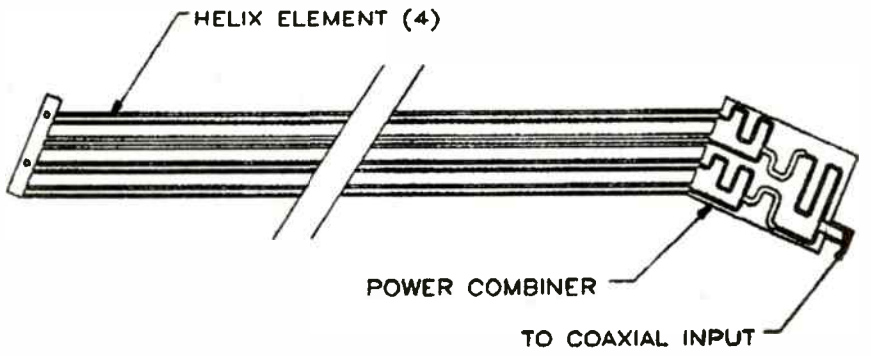

Figure 2 Helix elements and power combiner circuit printed on Mylar.

MEASURED ELECTRICAL PERFORMANCE OF MAST ANTENNA

The gain at cross-over, VSWR, and axial Ratio for the low, middle, and high frequencies of both the receive and transmit bands for scan angles of 20°, 40°, and 60° elevation above horizon are listed in Tables 1a through 1c. Table 2 lists the frequency scanning behavior between the frequency limits of 1525 MHz and 1660.5 MHz also for 20°, 40°, and 60° elevation above horizon.

Table 1 Measured electrical data on the mast antenna at a) 20° elevation, b) 40° elevation, and c) 60° elevation.

a) Mast steered to 20° elevation.

Frequency (MHz)	Gain (dBic)	Axial Ratio (dB)	VSWR
1525	8.0	1.0	1.7
1542	8.1	1.5	1.7
1559	8.1	1.0	1.5
1626	8.1	1.5	1.6
1643	8.2	1.7	1.5
1661	8.2	1.0	1.7

b) Mast steered to 40° elevation.

Frequency (MHz)	Gain (dBic)	Axial Ratio (dB)	VSWR
1525	8.1	1.0	1.8
1542	8.0	0.5	1.8
1559	8.1	0.5	1.5
1626	8.1	2.0	1.8
1643	8.2	2.0	1.6
1661	8.1	2.0	1.9

c) Mast steered to 60° elevation.

Frequency (MHz)	Gain (dBic)	Axial Ratio (dB)	VSWR
1525	8.2	1.0	1.7
1542	8.3	1.0	1.6
1559	8.3	1.0	1.5
1626	8.3	1.5	1.5
1643	8.1	1.0	1.6
1661	8.1	1.0	1.8

Table 2 Measured frequency scanning behavior, 1525 to 1660.5 MHz.

Elevation Angle	Frequency Scan	Cross-over Loss
20°	4°	0.25 dB
40°	6°	0.30 dB
60°	11°	** dB

** Note: Cross-over loss not applicable at this elevation angle.

LOW PROFILE DISK ANTENNA

The disk antenna was developed to meet the need for a relative low profile (1-inch tall) antenna with medium gain levels throughout elevation coverage. Unlike the mast, the disk antenna is directive in both elevation and azimuth. The elevation beam is shaped for complete elevation coverage so that steering is required in the azimuth plane only. The focus on the disk antenna is on how beam shaping is accomplished and the features which provide mechanical beam steering. Figure 3 shows an outline drawing of the disk antenna enclosed within its radome.

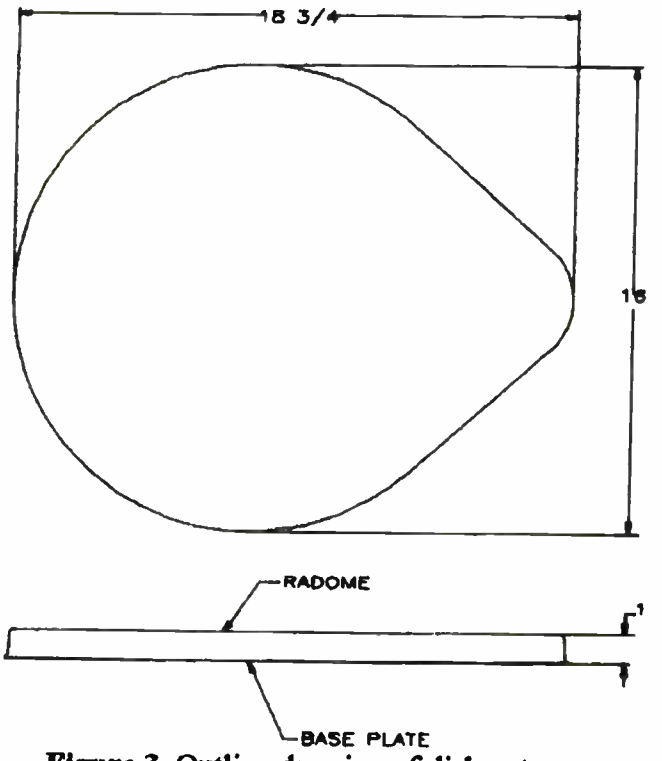

Figure 3 Outline drawing of disk antenna.

RF DESIGN

The RF components of the system include a non-contacting rotary coupler, the microstrip power combining network with driver elements, and a beam shaping array. These are described in the following subsections.

Rotary Coupler

A sketch of the rotary coupler is shown in Figure 4. Its purpose is to carry the RF transmission signal between the antenna and MET transceiver allowing for 360° rotation of the antenna circuitry relative to its fixed platform. It operates as a series parallel-plate capacitor, with one plate coupling the ground shield of the coax line to the ground plane of the antenna circuit, and the other plate coupling the center conductor of the coax to the microstrip power combining network.

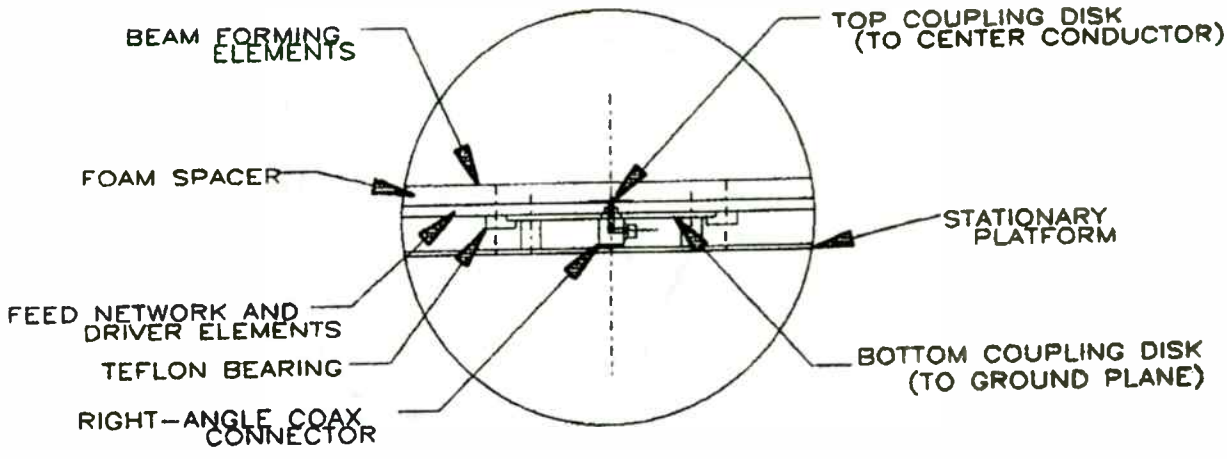

Figure 4 Side view of rotary coupler.

The in-line reactance due to the coupler is tuned to resonance using a tuning stub etched into the power combiner. Spacing tolerance is maintained with a Teflon bearing, as will be further discussed in the section on steering mechanics. A UT141 coaxial cable carries the RF signal between the coupler and a SMA male connector located on the sidewall of the radome. It was decided to exit all electrical interfaces through the side of the antenna rather than its bottom to avoid the need for drilling cable access holes through the vehicle body for temporary installations.

Power Combining Network

The power combining network uses a microstrip transmission line medium of tin-plated copper etched on a 15.5 inch diameter of 0.125 inch thick Teflon-fiberglass substrate ($\varepsilon_r = 2.5$). The network, shown in Figure 5, consists of a set of matched tees and 90° phase shifting hybrids which combine four driver elements used for exciting the beam shaping array. The driver elements are TM_{11} mode patches excited to produce a right-hand circularly polarized field. The combiner terminates into a single 50Ω port at the rotary coupler described earlier. A total of 0.6 dB in losses is attributed to this network.

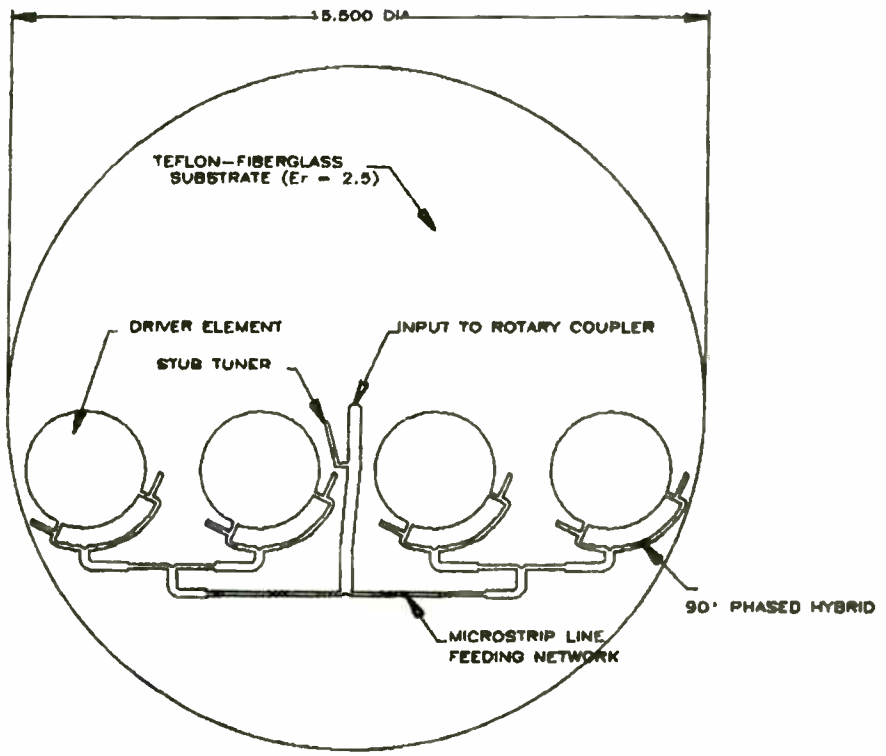

Figure 5 RF power combiner and driver elements.

Beam Shaping Array

An array of eight tin-plated copper elements configured in a 2x4 matrix is etched on a 15.5 inch diameter of 3 mil thick Mylar film. The two rows of four elements are printed on opposite sides to allow a slight overlap for increased coupling without making physical contact. See Figure 6 for details. Spacing this array above the driver elements with a 0.25 inch sheet of foam causes a reshaping of their elevation beam for 25° to 60° coverage.

The principle behind beam shaping of this type is simple. It involves reforming the dominant TM_{11} mode radiation into a TM_{21} mode that is characterized by a conical shaped beam with a null at zenith and main beam directed at some elevation angle above horizon. The azimuth cut in the classic case would be omnidirectional, but for the MSAT application it is desirous to maintain a pointing beam directed from broadside of the array.

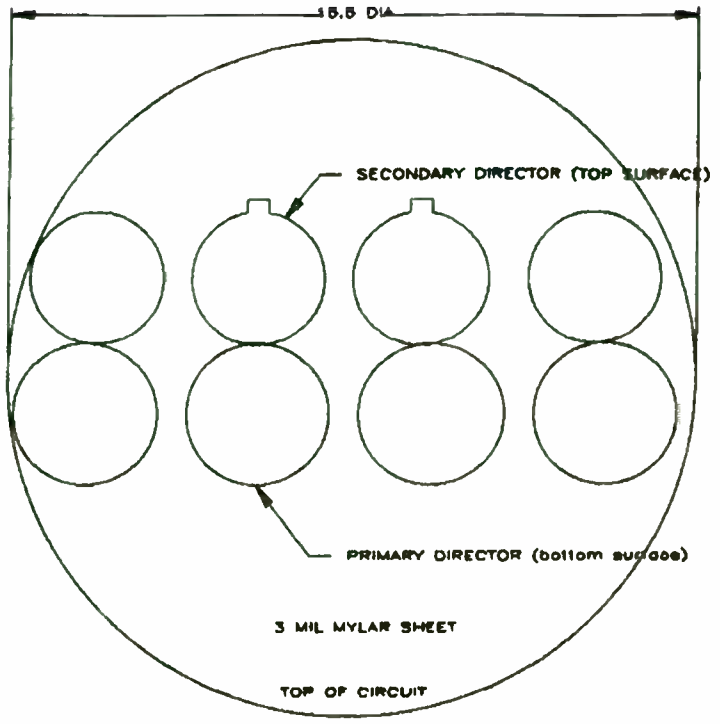

Figure 6 Beam forming circuit layer.

The beam shaping elements are proportioned and located so as to generate this special mode with the added feature of suppressing the radiation power in the back lobe and redirecting it into the forward lobe of the elevation plane. To do this, each pair of coupled elements is formed as a two-element subarray fed approximately in anti-phase, generating a split beam in elevation and a directive beam in azimuth. These subarrays are then positioned for differential phasing with other adjacent element pairs, suppressing the elevation back lobe. Since the RF energy is passed among the elements through coupling, the radiation characteristics are less sensitive to frequency than a direct contact feeding network.

STEERING MECHANICS

The basic mechanical components of the flat plate array are the rotating disk, stepper motor, friction drive and supporting bearing. A base plate and radome act as a cover to protect internals from the environment. These components are shown in Figure 7.

Stepper Motor

A stepper motor was chosen of a conventional analog type because of its ability to accelerate and decelerate within a short period of time and simplicity to control, both advantages in antenna tracking. The stepper motor selected for this antenna is the low profile Series 80000 "pancake" design manufactured by Haydon Switch and Instrument, Inc. It has an overall height of 5/8", similar to the one used for the JPL Yagi in their MSAT-X project. It operates on 12VDC and is capable of producing 20 oz-in of holding torque. A separate controller board is supplied for input from the transceiver tracking system. Control inputs to the tracking electronics exit the side of the radome.

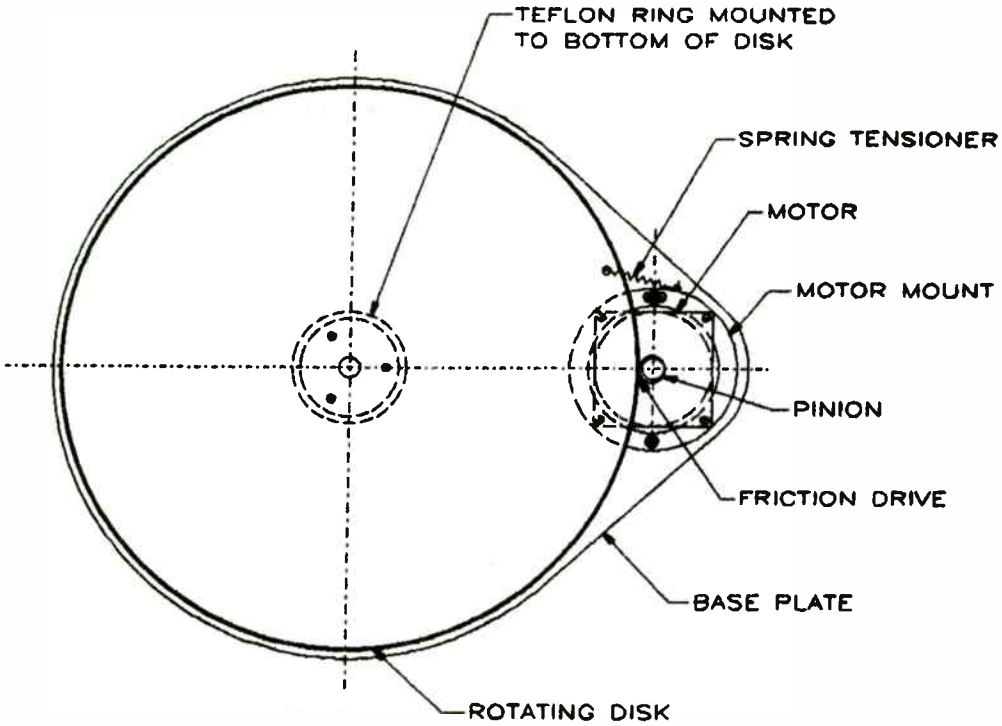

Figure 7 Components for steering mechanics of disk antenna.

Friction Drive

To maximize the headroom within the radome, the stepper motor was located at the perimeter of the antenna disk rather than directly beneath it. A decision was made to drive the antenna with friction rather than the usual belt and pulley arrangement, reducing the number of moving parts and loading on the motor. The friction drive uses a neoprene band permanently bonded to the outer edge of the rotating disk. Similarly, the motor has a neoprene band positioned around its pinion.

The motor is mounted to the outer edge of the disk by a pivot on one end of its housing and a spring on the other. Tension from the spring maintains contact between the motor pinion and the disk eliminating slippage. Ratio of disk to motor pinion is approximately 25:1. The motor response is set by a potentiometer on the controller board to accommodate a vehicle turning 90 degrees in 2 seconds. The required torque on the motor is 7.3 oz-in, which is well within the motor's capability.

Supporting Bearing

The supporting bearing is incorporated into the RF joint in the center of the disk. The bearing not only supports the rotating disk but also resists the lateral movement of the motor via the spring. The bearing utilizes a machined Teflon ring that rides into a brass disk used as the grounding plate for the rotating RF coupler. The Teflon ring is attached to the rotating disk and thus turns with it.

Base plate and Radome

The base is a teardrop shaped aluminum plate to which the rotary joint and motor are mounted to. It serves as the stationary platform for the moving parts of the antenna assembly. The radome is also teardrop shaped and is designed to be sealed at its base perimeter to the base plate to protect the antenna, motor, etc. from the environment. A thermoformed sheet of white cellulose acetate butyrate (CAB) was selected as the radome material for its low cost, durability, and resistance to ultra-violet rays.

ELECTRICAL PERFORMANCE

The antenna was tested for radiation characteristics and return loss using and indoor anechoic antenna test range. Measurements were made at 1525, 1600, and 1661 MHz which correspond to the low, mid, and high frequencies of the operating MSAT band.

Test Results

The results of electrically testing the low profile mechanically steerable array is summarized in Table 3.

Table 3 Summary of electrical performance for disk antenna.

	Frequency (MHz)		
	1525	**1600**	**1661**
Gain (dBic)@ 25° Elevation	9.0	9.1	9.1
@ 45° Elevation	11.5	11.7	11.7
@ 60° Elevation	10.7	10.5	10.8
Azimuth HPBW	27°	25°	23°
Elevation HPBW	46°	42°	42°
Axial Ratio (dB)*	4.0	3.0	4.0
VSWR	1.62	1.65	1.45

CONCLUSION

A quadrifilar mast and a low profile disk antenna with a shaped elevation beam were built and tested. The mast antenna is omnidirectional in azimuth with a typical gain of 8 dBic requiring beam steering in the elevation plane for MSAT coverage. The disk antenna is directive in azimuth with a shaped elevation beam that must be mechanically steered to maintain MSAT coverage. It has a typical gain of 9 dBic. The purpose of this paper is to present these two antennas as logical designs for the MSAT service, and as much attention has been paid to their construction as to their performance.

77 GHz Automotive Radars: The Markets, Technologies and Production Costs

by Lamberto Raffaelli

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This paper will present the design methodology and test results of several GaAs monolithic circuits (MMICs) specifically designed for 77 GHz collision avoidance radars. In addition, test data for an integrated transmitter will be presented, along with projected 1995 cost tradeoffs between fundamental (77 GHz VCOs using 0.15 micron pseudomorphic HEMTs) and multiplied (38.5 GHz VCOs used with 0.25 micron power MESFET amplifiers and a multiplier) transmitter approaches.

Study of automotive electronic interference in the Brazilian satellite system

Cladimir Jose Benvenutti, Mauricio Anastacio Costa, and Edmar Munhoz Pensutti, BASTEC, Rua Chile, 836 - Reboucas, Curitiba - Parana - Brasil; 55-41-321-7752, FAX: 55-41-321-7800.

INTRODUCTION

Bastec is a enterprise that has been offering solutions in both Telecommunications and Data Processing Systems since 1986. The Satellite Division is a department of the Telecommunications Area that was created in 1989 to work with a new technology that was emerging in the country: " Private VSAT Systems ". Nowadays, the Satellite Division offers services of Site Survey, Project Developments, Interference Analysis, Installation, Aceptance Tests and Maintenance in both Master and Remote Stations of VSAT, SCPC and TDM technologies. Other Departments of the Telecommunications Area develop work in Voice and Data Terrestrial Communications, Telephonic Systems and Banking Automation, with a large experience.

THE BRAZILLIAN SATELLITE SYSTEM

As both the Brazillian Satellite System and the Terrestrial Microwave Network in the entire country are operating on " C " band, there is a strong possibility of interference between these two kinds of technologies. This situation obligated the use of a sophisticated processes and equipments to evaluate and to preserve the integrity of the operations without possibility of mutual interference. One of these processes is the Interference Analysis, which consists in measurements of the interefering signals in the exact site where the antenna will operate, to evaluate precisely the probability and the cause of the interference.

Bastec has a large experience in Interference Analysis, with more than a hundred analysis performed. This experience has helped us to isolate, evaluate and to find the best solution to the case described below.

THE AUTOMOTIVE INTERFERENCE CASE

This text goes to report our experiments based on works developed at the VSAT (Very Small Aperture Terminal) station integrated to a private banking network in the city of Piracicaba/SP/Brazil.

In april 07th of 1992, this station was activated, with MCPC - BPSK - FDMA technology, and it was implemented with a 1,8m focal-point antenna. This station showed some hardware problems that were systematically solved.

After a new activation we observed that the station showed a high incidence of space link failures, with a average of five times per day. These failures were sporadics and seemed to be without relationship with previous failures.

Thus, we started a detailed analysis at the indoor modules, trying to identify the failure motive. We could conclude that the station was in perfect operational condictions, therefore, the probable cause were not in the station but definitively from outside of it. Due this fact, we conduct all of our attention to space segment.

We noted that 80% of data link failure occurred between 8a.m. and 8p.m.. Using a spectrum analyser we made a preliminar test monitoring the signals on the indoor module input, in the UHF band on the period mentioned above. Using a splitter, we started to observe the reception frequency spectrum with the terminal in normal operation. Then, we verified that sporadically appeared impulsive noise signals along the satellite spectrum overtaking the data signals breaking the data link. Observing the average level of this noise and the failure time, we concluded that if this noise overcame the level of -85 dBm (-8 dBc related to the satellite carrier signal reception), the relation C/N would be compromised, consequently the station would fail.

Defined the failures cause, we started finding out the probable noise source that was generating this noise. Thus, we concentrated our observations in the possible sources between 8a.m. and 8p.m., such as: chamber machines, air conditioners, eletrical equipments, etc. After sometime monitoring, we went not that far to conclude that the noise was not coming from the building, because there was not relation between the time that the noise appeared and the activity of such equipments.

There was a building in construction on the next block, very close with the antenna direction to the satellite , so we tried to relate the noise with the elevator operation, solder machine and other equipments. Then, we concluded there was not in the construction building the noise source that was interfering us.

Thus, we suspected of the automotive noise. We have already observed in some interference analyses that in certain conditions (proximity, exposition, etc), the noise generated by vehicle became quite significative, resulting different measurements. At this station, the antenna was on the building highest point, above the big water reservatory. However, by user's suggestion, the antenna was installed at the edge of the building. In this condiction, it stayed exposed to every noise variety that came from Moraes Barros street. With short time of monitoring we proved the automotive noise theory. The noise that came from the street came into the lobe of the antenna situated approximately 90 deg. from the satellite direction, called spill-over, reached the LNB where was amplified and went down until the module mixed with the satellite carriers.

Observing the instantaneous noise level measured and the vehicles crossing the street in front of the building, we could conclud that the small motorcycles (50 cc, two engines), were the responsible by systems downfalls. The noise levels generated by these motorcycles were quite superior comparing to the other kind of vehicle.

According to this context, we concluded that we had two possible alternatives to solve the problem. The first one was the installation of an artificial shield capable of attenuate the noise. The second was to remove the antenna to another place taking account natural barriers (clutters) like other buildings. After a technical - economic analysis, we defined that, firstly, we should remove the antenna to another place trying to get the necessary attenuation, otherwise would be necessary to use an artificial shield.

We came back to Piracicaba carrying on a setup of measurements composed of a spectrum analyser, capable of measure signals in the 4GHz band, a SHF corrugated horn, LNA and necessary accessories.

Thus, we mounted the setup beside the antenna and started to measure the noise generated by vehicles crossing the street under of us. Once more, we could observe that the small motorcycles were the biggest noise generator. As the horn gain was greater than the antenna spill-over, with this sensibility increment was possible to observe that older vehicles (more than 10 year) generated noise level more significant than newer ones, however, approximately 15 dB lower than the small motorcycles. New vehicles (less than 10 years) generated noise with level very close or under the setup sensibility threshold (-130 dBm), not significant for the satellite station.

To effect the test, we selected among some small motorcycles that we had disposed, the one that generated the biggest noise levels. First we tried to put the small motorcycle in a way to get the biggest noise amount as possible. We could conclude that due to motorcycle structure, it had a "pattern irradiation" with approximately a gain of 12 dB in the perpendicular direction to the motorcycle axis relationed with the levels irradiated in the axis direction. It came to explain somewhat we had observed.

On the other side of Moraes Barros street there was a bank agency, where one of its guards possessed a small motorcycle. The system always suffered downfall on the exact moment that the guard got in or came out of the agency parking. This certainly occurred because of a short period of time, in the exat instant that the motorcycle position was perpendicular at the antenna direction to the satellite, the noise level received in the antenna increased dramatically, breaking the data link.

With the small motorcycle positioned in the more critical situation, we effectuated new measures beside the antenna, and verified that was impossible to maintain the antenna on that position . We did noise measurements again in the digital UHF input, and verified that in this condition the noise level stayed at about -75 dBm (+3 dBc) . Therefore, we concluded that was necessary to find an alternative point to offer us a new attenuation around 20 dB at least, to have operational equipment security.

Then we placed the setup to the alternative point one floor down behind the big water reservatory (alternative point 1). In this point, the big water reservatory would be used like a barrier, protecting the antenna against the signals that came from Moraes Barros street. The measurements comproved our expectative about the noise attenuation of this street provided for the big water reservatory. Although, we observed that between the angles 215 deg. to 270 deg. the antenna was on the line of sight direct to the XV de Novembro street, on the other side of the block. As 313 deg. angle was to the satellite direction, was dangerous newly the interference by spill-over of the antenna. We effectuated the measurements in this directon, and we verified that the high levels continued, in spite of distance. Comparatively, the point showed an attenuation at about 10 dB connected with the original point.

Thus, we tried to find another alternative point four floors down the original point over the agency ceiling (alternative point 2). If we did not get the expected attenuation in this point, we should build an artificial shield to protect the antenna. After the tests in this point, we verified that on the direction of Moraes Barros street the attenuation that we got was overtaking 20 dB, and the highest levels were coming from the building edge, where the noise was diffracting. On the direction of XV de novembro street we did not get any noise. Therefore, we suggested to the customer to change the antenna to this point.

In October, 8th the station was activated again with the antenna positioned on the place suggested by us. Using a splitter we effectuated again all the tests, now in real condictions of operation, on the digital module UHF input. Then we verified that the noise level did not change, despite having the motorcycles crossing in front of the agency. In October, 23th the customer called us to inform that the station had overcome 15 days without any failure, that was the best result that we could have received.

CLADIMIR JOSÉ BENVENUTTI - Telecommunications Engineer
MAURICIO ANASTÁCIO COSTA - Telecommunications Engineer
EDMAR MUNHOZ PENSUTTI - Telecommunications Engineer

FREQUENCY COORDINATION

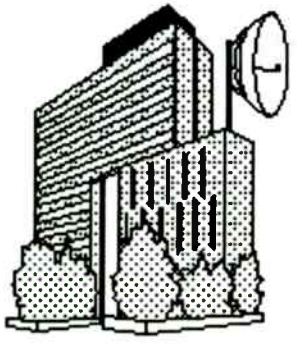
Liberated Bands to the use

"C" Band ***TX - 5.925 GHz a 6.425 GHz***

RX - 3.7 GHz a 4.2 GHz

FREQUENCY COORDINATION

Terrestrial microwave links



F_{TX} (f1,f2)

F_{RX} (f1',f2')

RX 4GHz

TX 6GHz

F_{TX} (f1',f2')

F_{RX} (f1,f2)

f1,f1' - 4 GHz Band

f2,f2' - 6 GHz Band

FREQUENCY COORDINATION

Objective:

-Avoid interference between satellite stations

-Avoid interference between transponders (Polarization)

-Avoid interference between terrestrial stations and microwave terrestrial links (Interference Analysis)

Organ Involved

1- UIT / CCIR

2- SNC (Transport and Communications Ministry)

3- EMBRATEL

PROBLEM CHARACTERISTICS

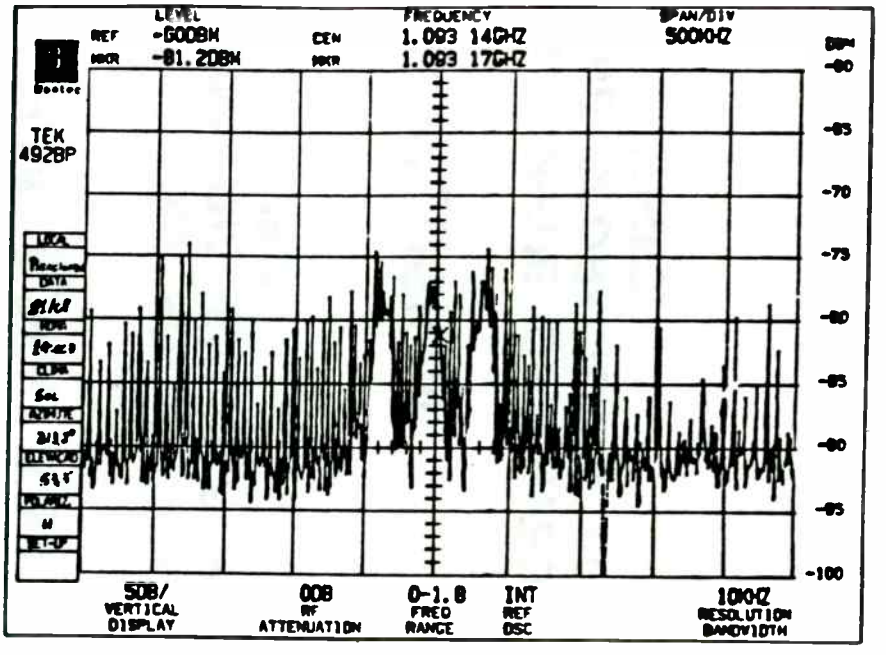
- *VSAT STATION-MCPC/BPSK/FDMA TECHNOLOGY*
- *1.8 METER FOCAL POINT ANTENNA*
- *HIGH INCIDENCE OF SPACE LINK FAILURE (FIVE TIMES PER DAY)*
- *THE FAILURES WERE SPORADICS AND 80% OCURRED BETWEEN 8 a.m. AND 8 p.m.*
- *THE HARDWARE AND SOFTWARE EQUIPMENT PARTS WERE FULL OPERATIONAL.*

FIRST PROBLEM ANALYSIS

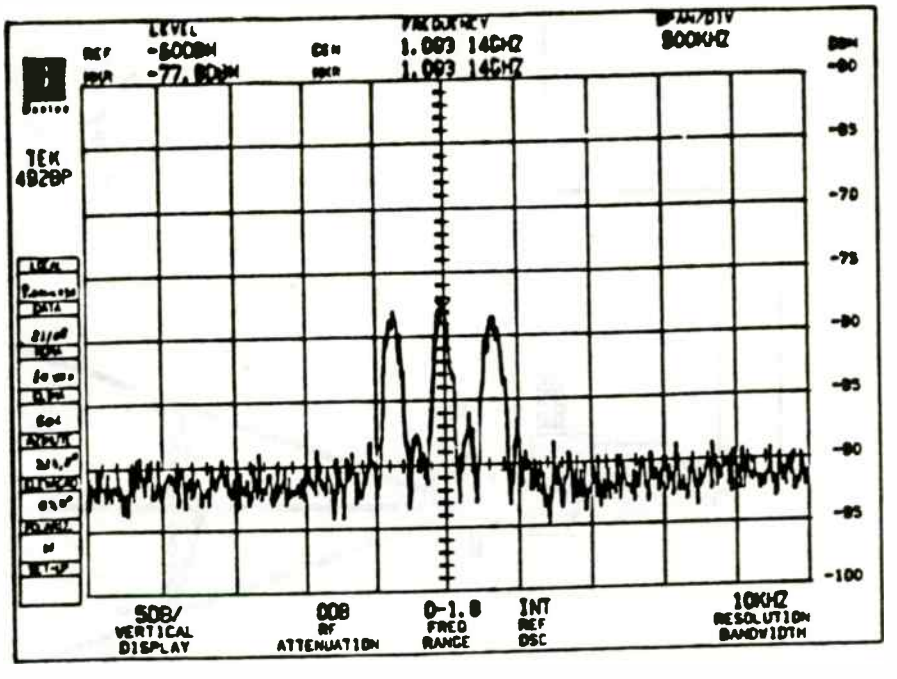
- *USING A SPECTRUM ANALYSER AND A SPLITTER WE STARTED TO MONITORING THE SIGNALS RECEIVED BY THE FOCAL POINT ANTENNA.*

FIRST CONCLUSION:

- *INTERFERING SIGNALS WERE OBSERVED AT LNB OUTPUT WHICH WERE SPORADICALS AND WERE CAUSING SPACE LINK FAILURES.*

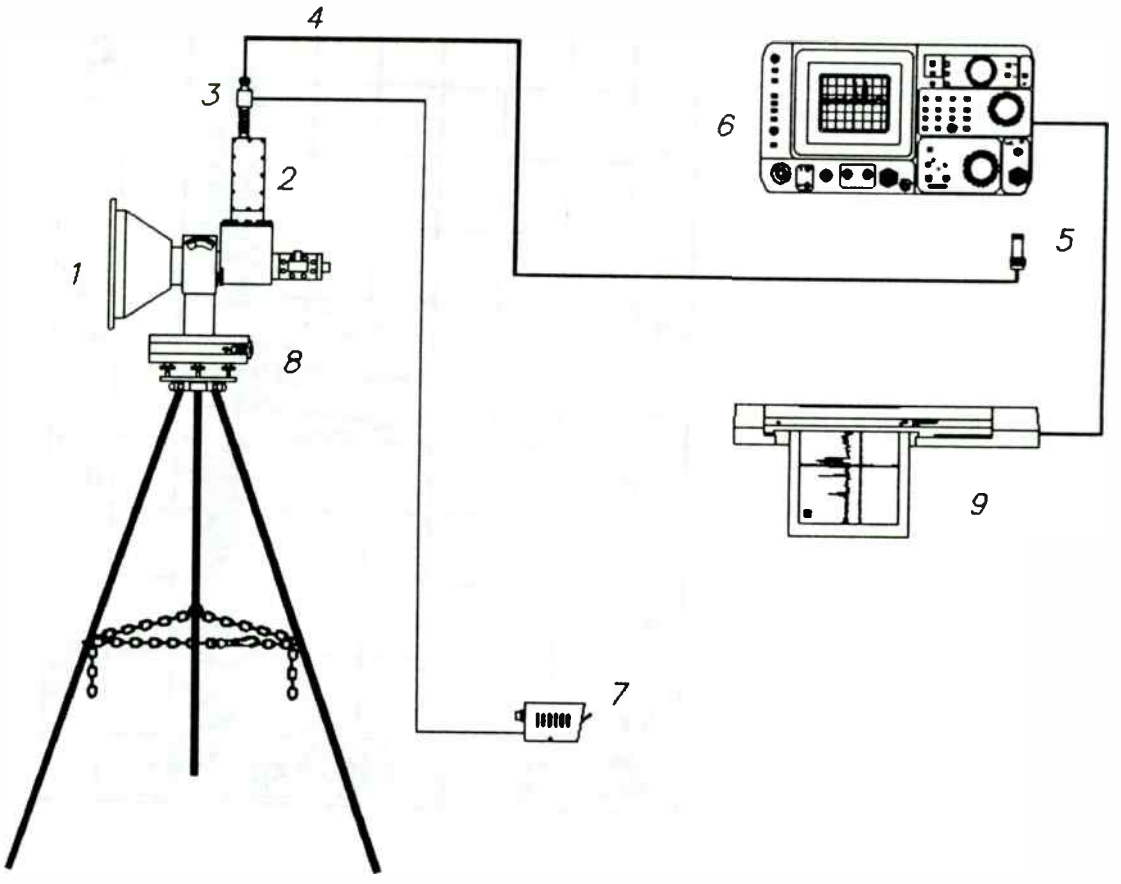


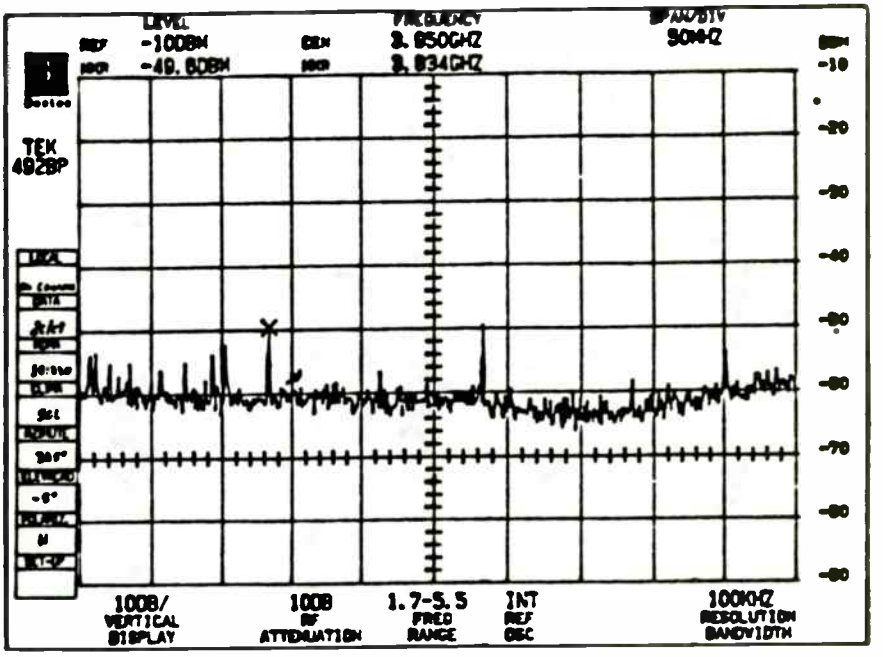
- Outbounds with noise in the digital module UHF input, original point.



- Outbounds without noise in the digital module UHF input, original point.

SET-UP ASSEMBLY DIAGRAM





- Original point without noise, beside the antenna.

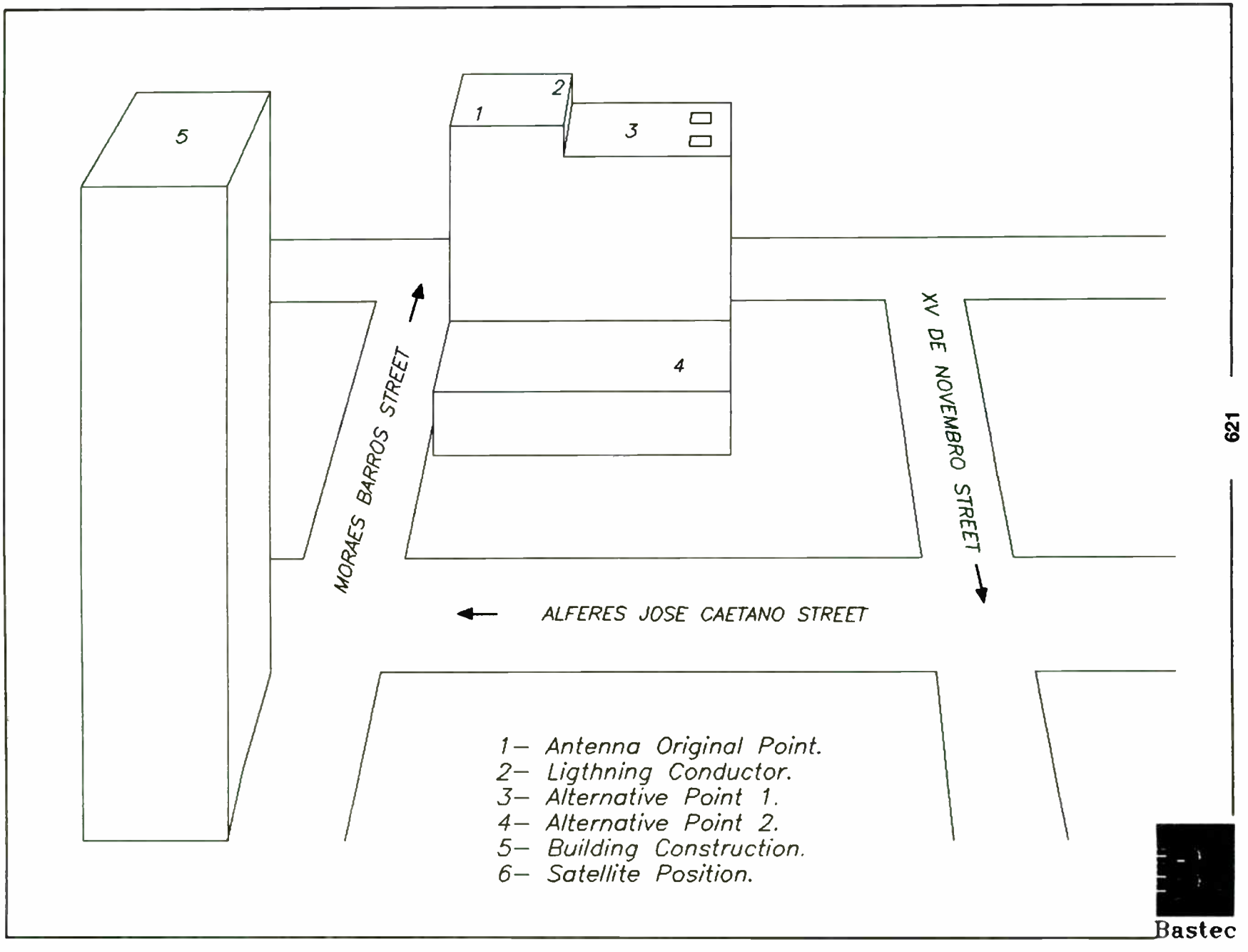
CHOSEN ALTERNATIVE

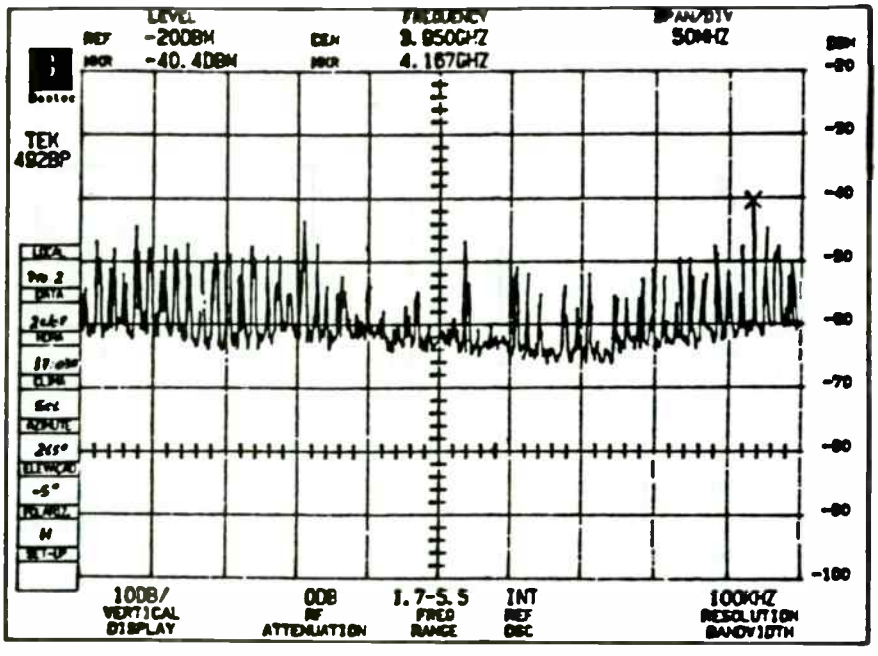
- *TO CHANGE THE ANTENNA POSITION SITE*

TO CHOOSE THE BEST PLACE TO THE ANTENNA POSITION

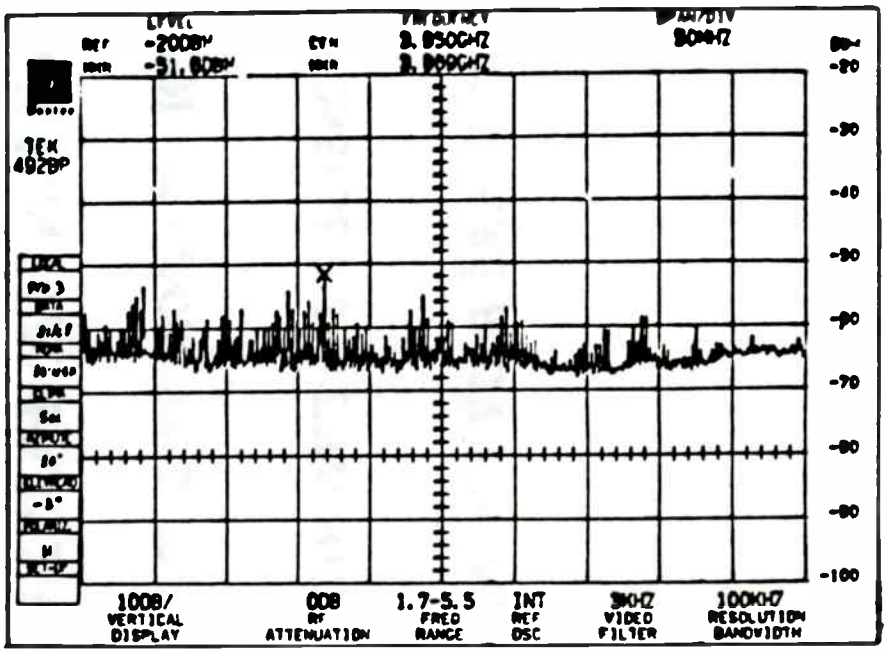
- *SIGNALS RECEIVED COMPARED WITH THE ANTENNA ORIGINAL POINT*

- *TO PROTECT THE ANTENNA FROM THE STRONGEST SIGNAL LEVELS*





- Alternative point 1, with noise from XV de Novembro street.



- Alternative point 2, with diffracted noise at the building edge.

DEFINITIVE ANTENNA POSITION

- *THE MOST DISTANT POINT FROM THE STREET*

- *THE LOWEST POINT POSSIBLE IN THE BUILDING*

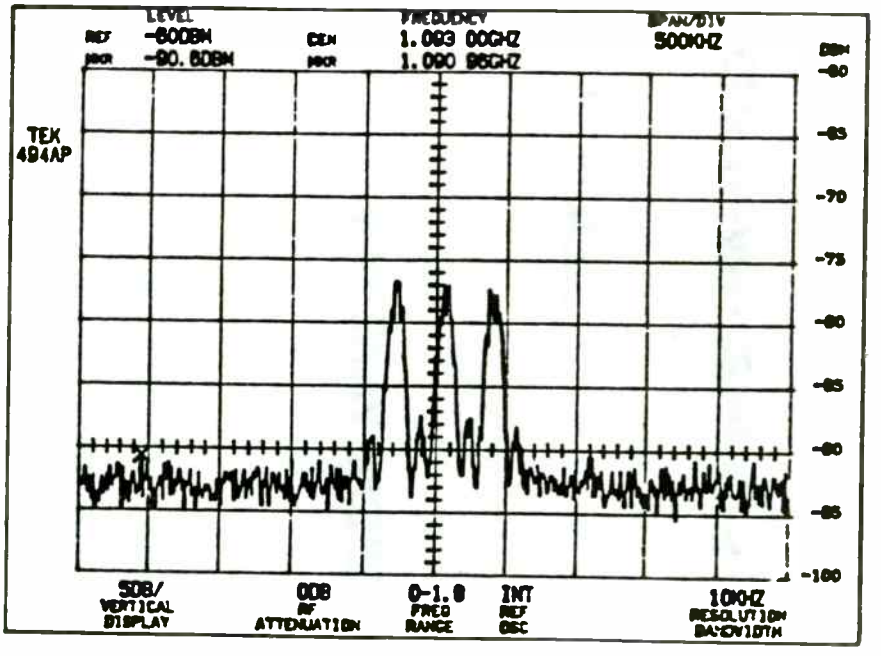
- *THE BEST CARRIER TO NOISE RATIO (C/N)*

FINAL MEASUREMENTS

- *1.8 METER FOCAL POINT ANTENNA INSTALLED IN THE NEW POSITION*

- *APPROPRIATED EQUIPMENTS*

- *NEW OUTPUT LEVELS MEASUREMENTS ON THE LNB*



- Alternative point 2. Outbound received with noise, in the digital module entrance.

FINAL CONCLUSIONS

- THE USE OF LOW NOISE AMPLIFIERS IMPLICATE IN THE POSSIBILITY OF SUFFERING INTERFERENCES OF ANY KIND OF SOURCES.

- FOR SYSTEMS THAT OPERATE IN SO CRITICAL CONDITIONS AS THE SATELLITE SYSTEMS, NOISE SOURCES WITH APPARENTLY INSIGNIFICANT LEVELS BECOME VERY IMPORTANT IN THE CONTEXT.

- THE CORRECT ANTENNA POSITION IN RELATION TO THE TRAFFIC JAM IS ESSENTIAL TO PREVENT AUTOMOTIVE INTERFERENCE.

- THE BACKGROUND NOISE IN THE INTERFERENCE ANALYSIS LEAD US TO THE DIAGNOSTIC AND SOLUTION

ELECTRIC VEHICLE CHARGER DEMAND SIDE MANAGEMENT COMMUNICATIONS SYSTEM

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ABSTRACT

With recent regulations (California, Massachusetts, others to follow) mandating the usage of zero emissions vehicles by 1998 [1] Electric Vehicle (EV) chargers will represent a significant future load on many utility networks. California utilities have indicated that they could handle over one million EV's without new generation capabilities given an effective demand side management (DSM) program. DSM enables customers to make choices about initiating lower "Off peak" rates by turning some control of electricity-intensive activities over to the utility company. The ability to provide cost effective two-way communication between the utility and its customers is the key to an effective DSM program.

The advanced Electric Vehicle Charger DSM system described combines automatic meter reading, load management, and EV charger monitoring and control functions into a single integrated system whose information is easily accessible by utilities and homeowners.

Two different communications technologies are used in this charger station application. The first is a low frequency spread spectrum system that allows data communication over AC power lines. This technology, called Integrated Circuit, Spread Spectrum (IC/SS) was developed by CYPLEX and ITRON, and subsequently licensed to National Semiconductor. IC/SS creates a local area network, linking EV chargers, meters and home display units served by a single low voltage transformer.

Once concentrated at a Master device, the IC/SS power line data is then interfaced to a wide area network (WAN) via a radio modem. Data is then transmitted over the network to a host computer located at the utility control center. The MOBITEX™ radio network, a 900 MHz switched packet data system, operated in the United States by RAM Mobile Data has been selected as the WAN for this application.

I INTRODUCTION

EV Charging Systems

GM Hughes Electronics is developing a family of Electric Vehicle (EV) chargers for use by fleet operators (i.e. utility service vehicles, delivery vehicles, etc.) and private home owners. The company's goal is to have an EV charger infrastructure in place prior to the 1998 regulations becoming effective. Charge time is limited primarily by the current battery technology and the design and size (in KW) of the particular charger. These limits effectively restrict fast charging to a minimum of 20 minutes for an 80% charge. A more typical 6KW residential charger can fully charge an EV in about 3 hours on fast charge.

EV charging systems are relatively simple in theory. The driver of the EV positions the vehicle to within a few feet of the charger, and inserts a paddle-like induction connector, into the EV. There are at least two charging options: Economy "Overnite" Mode or Express. Selection of the Overnite mode may delay the charging of the vehicle until off-peak hours, when the price of electricity is lower.

Another class of EV chargers exist, called "Opportunity Chargers." These EV chargers represent a future version of today's gas stations, in which EV owners purchase electricity through retail outlets, i.e. at work, malls, or restaurants.

Two-way communications to EV chargers is required for several reasons:

(1) Utilities must have a means of controlling the load placed on the electric distribution system by EV chargers to avoid having to add new generation capability.

(2) Consumers must have the ability to select charging options, based on their life-style requirements. For example, if an EV owner arrives home at 6:00 p.m., and needs the EV to get to an 8:00 p.m. dinner appointment, charging off-peak is simply not an option.

(3) Credit/Debit card verification for Opportunity EV chargers is required for payment of electricity.

(4) Meter reading information must be available for billing purposes.

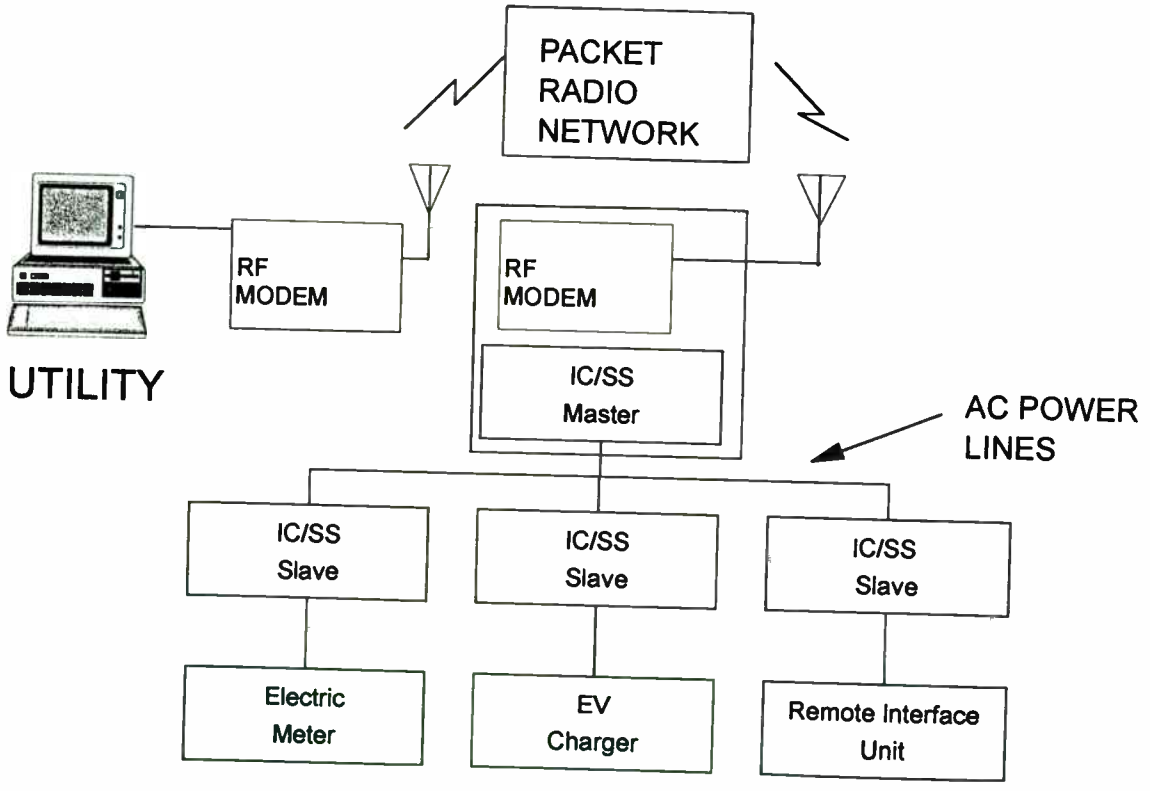
Meeting all of these requirements is mandatory to ensure the acceptance of Electric Vehicles by consumers, utilities, regulators, equipment manufacturers and service providers.

II ELECTRIC VEHICLE CHARGING SYSTEM

CYPLEX has developed an EV charger communication system, which demonstrates two-way data path from a utility control center to individual EV chargers. It is a hierarchical system, whereby each node in the network is individually addressable from the system host computer(s). The major system elements are:

- Host Computer with Data Acquisition Software
- Packet Radio Network
- LAN Interface Radio
- Multi-Tariff Meter
- EV Charger
- Remote Interface Unit (RIU)

FIGURE 1



EV Charger

The GM Hughes Electronics (GMHE) EV charger is a microprocessor based device with two communication capabilities. First, when the paddle connection is made to the EV, the charger communicates with the EV to determine the state of battery charge. It then optimizes the rate at which the battery is charged. This is done via an optical or low power RF link. Secondly, each EV charger, equipped with a Slave IC/SS modem (i.e., Slave address 01), can communicate its status and receive commands from the homeowner or if selected, the utility over the power lines. The IC/SS system can accommodate up to 1020 individually addressable devices on a single low voltage network. (In the United States, there are on average 8 - 12 homes served by a single low voltage transformer).

Remote Interface Unit

A Remote Interface Unit (RIU) inside the home is similarly equipped with an IC/SS modem (i.e. Slave address 02). The RIU can be plugged into an AC wall outlet, for instance in the bedroom or kitchen, depending on the homeowner's choice. The RIU can both monitor and control the status of the EV charging system, or interrogate the electric meter for up to date information on billing or electricity usage information. A Vacuum Fluorescent Display (VFD) is provided, along with a number of simple buttons and LEDs relating to the following functions:

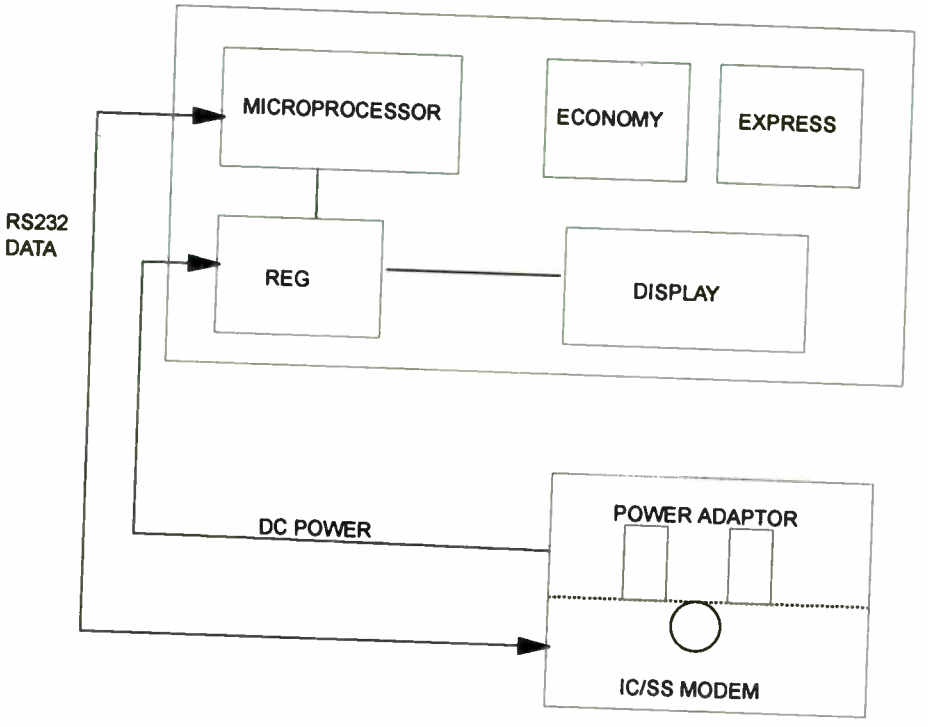
Display current EV Charger status
- -Overnite Mode, Express Mode, Off

Display current EV status
- -0 - 100% battery charger

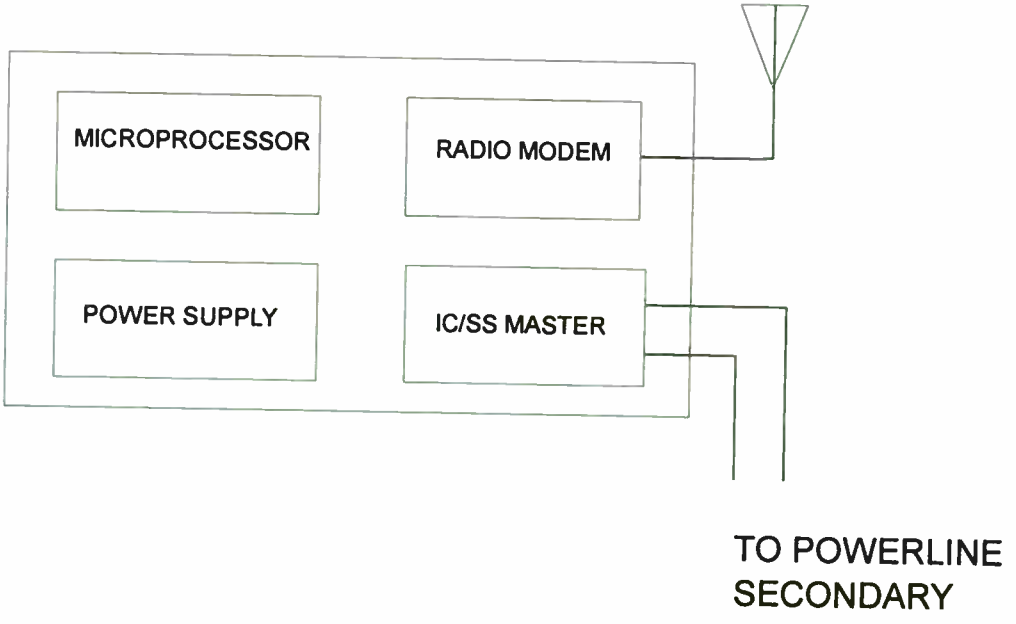
Change EV Charger status
- -To Overnite Mode, Express Mode, Off

Override Overnite or Express Mode
- -Yes, No

REMOTE INTERFACE UNIT (RIU) - FIGURE 2



LAN INTERFACE RADIO - FIGURE 3



Electric Meter

The Electric Meter used in the demonstration system is a Quad 4 meter from Process Systems. The Quad 4 provides multiple registers and will record electricity usage over an extended period of time. For instance, it can monitor and record at what time of day the charger was on. It communicates to another IC/SS modem (i.e., Slave address 03) via its serial port.

The information from the Quad 4 may be used by the utility for billing purposes, and will enable the customer to make choices about electricity usage based on access to real time information.

LAN Interface Radio

The LAN Interface Radio is a small enclosure housing a Master IC/SS modem, about the size of a business card, and an RF packet modem, about the size of a pack of cigarettes. Additional data flow intelligence in the form of a low cost microprocessor is included in this package. Distributed control reduces the burden on the utility host computer for managing communications. A power supply increases the total package size somewhat, but it is still quite compact and can easily be mounted on a utility pole or at a residence.

The IC/SS Master in the radio enclosure continuously polls each of the IC/SS Slave devices on its power line distribution in turn, looking for a request from them to communicate. Depending on the number of devices on the network, the scan rate may vary from several times per second to several seconds. Rigid data security is maintained between the customers sharing the same power line secondary. Typical examples of how this system might work follow:

- The homeowner requests through the RIU the current status of the charger. The RIU is polled 600 msec later, and sends this request to the IC/SS Master. The Master establishes a link with the charger, requests the current status, and then transmits this information to the RIU. Total elapsed time is typically in the 2 - 3 second range.

- The homeowner requests through the RIU that the charger be set in Economy Mode. The charger will turn on automatically during off-peak hours, when rates are less, and will be fully charged by 6:00 a.m. the following day.

- The utility experiences high demand at 4:00 p.m. on a hot summer day. It sends a broadcast command to half of the EV chargers, turning them off. Fifteen minutes later, it turns them back on, and the other half of its chargers off. This is accomplished via the radio modem at the host sending a broadcast message to a subset of the total number of LAN interface radios in the network. The on board IC/SS Master then broadcasts the same message over the power lines to the individual chargers.

- ACME delivery service's fleet manager wants to monitor which vehicles are on each charger every fifteen minutes, and the electricity consumption of each vehicle. Its host computer polls each charger, via the LAN interface radio, every fifteen minutes. Software in the host computer stores this information in a data base, which is periodically used to prepare management reports by the MIS department.

Host Computer

The host computer, which may be located at a utility control center or at a fleet manager's office, is typically an IBM-PC™ or equivalent machine operating using Windows 3.1™ or higher. A series of screens enable the operator to either monitor or control specific nodes in the network by simply clicking on the appropriate icon.

III INTEGRATED CIRCUIT SPREAD SPECTRUM (IC/SS) PRIMER

A practical multiple residence or fleet EV DSM charging system as proposed must first overcome the interference, electrical noise and transmission line losses associated with the use of AC power lines as the LAN in a more effective manner than as accomplished with traditional single residence common carrier systems.

Noise and Attenuation

Communications over the power line presents a very difficult problem for the modem designer, because of the severe noise and signal attenuation involved, and because conditions on the line vary greatly over time. The power distribution network is designed to operate in order to efficiently distribute power, without consideration of its behavior at communications frequencies. Consequently, in the range from 10 to 100 KHz, the impedance can vary widely from a few ohms or less to impedances in the 1000's of ohms with an unloaded line (equipment turned off or disconnected). In addition to attenuation issues, the system designer needs to be concerned with three primary noise types found on the power line: Impulse noise, continuous-wave (CW) interference, and white noise.

Impulse noise results from the mechanical or electronic switching of inductive loads and can produce levels that may saturate radio receivers for periods of tens or even hundreds of microseconds. These impulses may have rapid rise and fall times and are sometimes impossible to filter out completely. Periodic half cycle switching responses occurring at double the power line frequency are typical of this type of noise. Worse yet, resonant effects, high voltage extended ringing wave forms among them, can be initiated by impulse noise.

CW interference is generated when these resonant effects extend or "ring" the wave form for many cycles in the communications band. These somewhat unpredictable signals act exactly like CW jamming to the modem.

Finally, ordinary white noise becomes an issue, particularly when operating at the highest receiver gains available. A power line modem must operate well with respect to the classical criterion of bit error rate vs. signal/noise ratio with additive Gaussian noise.

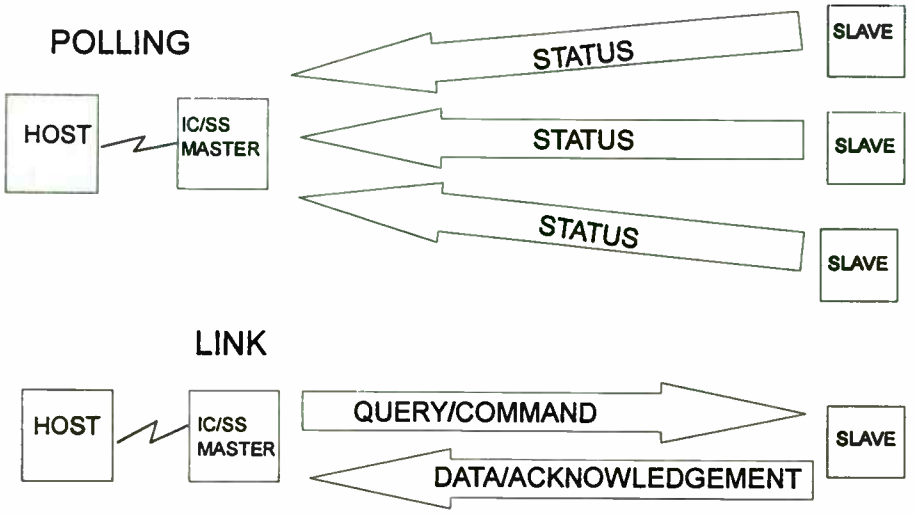
Accuracy, security and real time command and reporting capability is essential in any control or polling system; and our EV charger application is no exception in these regards. However, data throughput (baud rate) need not be lightning fast as files are not typically massive (as with E-MAIL LAN applications). Certainly, any real solution needs to be low in cost per node which for a product of this complexity, translates into a high degree of required semiconductor integration.

Integrated Solution

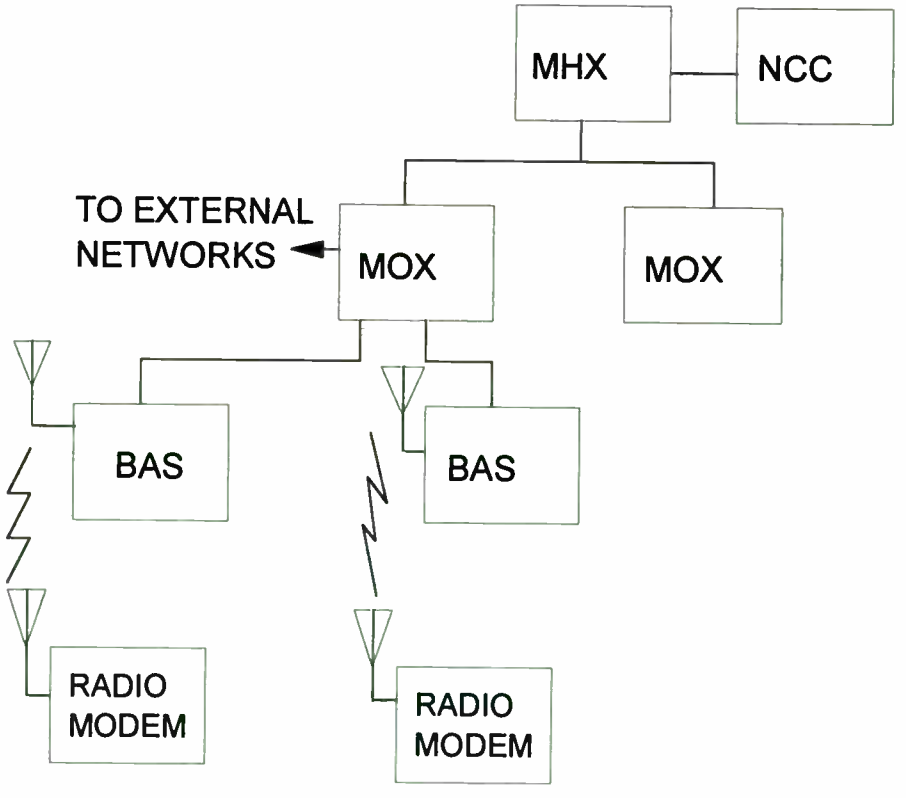
The IC/SS modem chip set was developed jointly by CYPLEX, ITRON and National Semiconductor. The primary design goals included providing a cost effective and error free data transmission solution over power lines that complied with FCC and VDE emissions standards and one that could meet the CENELEC requirements for utility communications on the distribution secondary. Although operating in the band between 10 and 100 KHz, power line communication with IC/SS combines the benefits of several techniques found in many proven higher frequency data communications systems:

* Frequency Agility (Hopping)
* Frequency Shift Keying (FSK)
* Frequency Diversity
* Received Signal Strength Indication (RSSI) Gain Control
* Transmitter Power Control
* Digital Signal Processing
* Adaptive Bit Rate
* Packet Error Correction

IC/SS POWERLINE LAN PROTOCOL - FIGURE 4



PACKET RADIO NETWORK - FIGURE 5



The frequency hopping system employed in IC/SS is unlike typical spread spectrum military systems that must perform against non-friendly intelligent jammers or Part 15 ISM band systems that must conform to FCC defined processing gain and power guidelines. Once a clear frequency has been found based on a previously defined signal to noise threshold, the system locks on that frequency and stays put until the ambient line conditions degrade beyond the point of the system to compensate for them. IC/SS modems utilize full-time frequency diversity. All masters and slaves in the LAN actually share pairs of frequencies. Under degraded conditions, the master and slave will begin hopping in a pseudo-random manner until another set of clear frequencies is found. Any of the slaves on the line that fail to receive the change frequency command (because of an impulse noise burst for instance) will "hunt" for the newly selected pair. Slaves are interrogated and pass data on a polled basis.

IV THE WIDE AREA NETWORK

CYPLEX chose to utilize RAM's MOBITEX network, a packet switched, 900 MHz, data-over-radio system to provide the link between the utility and the EV user clusters. The MOBITEX system has coverage in more than 6300 U.S. cities, in Canada, the United Kingdom and in portions of Europe and Australia. The system is optimized for low cost data transmission and makes use of ten to thirty licensed channels in each of its market areas. By using MOBITEX linked with IC/SS, a single radio modem and a fixed antenna may be connected anywhere along the power line secondary to provide an efficient and cost effective means to link the utility to the customer group.

V COMMUNICATION ALTERNATIVES

There are a variety of communications media alternatives available for both Local Area and Wide Area Data Networking. In most slow rate two-way and polling data networks, a hybrid system is likely. System selection should be based on availability, reliability, cost and ease of use.

Common LAN alternatives include the use either twisted pair wiring, low power RF, both fixed frequency and spread spectrum, or infrared. Installation cost is a major drawback of twisted pair systems, although they rank high in reliability. Low power RF, presumably unlicensed ISM band equipment, provides the ability to communicate several hundred feet under optimal conditions. Its primary limitation is signal degradation, whether it be from other unlicensed systems operating in the area, or path loss due to physical obstructions, such a metal reinforced walls. Infrared systems work best with line of sight, which is often not available in practical LAN setups.

Numerous WAN alternatives may also be considered, including land line telephone, cellular, and fiber optic. Land line telephone service is still the most widely available option, although installation may be difficult in some sites, such as in parking garages. The MOBITEX system provides the added network benefits of its group broadcast,

store and forward and polling features. Cellular modem service remains costly, and suffers from the same limitations as MOBITEX in respect to signal propagation as they both operate in the 900 MHz band. In addition, cellular network capacity is already a problem in many urban areas during peak periods and data loss during these conditions is a real concern. Fiber optic use is growing, and in areas where the backbone is laid, offers a high bandwidth transmission media for linking various systems.

VI SUMMARY

Communications to Electric Vehicle charging systems is an important element in the successful adoption of EV technology by utilities and consumers alike. Utilities require the ability to remotely monitor and control EV charger loads in order to avoid having to build new power generating facilities. Consumers require the ability to efficiently and economically charge Electric Vehicles with minimum impact on their lifestyle.

The technology exists today to implement the types of communications systems required. GM Hughes Electronic's IC/SS-based power line LAN, combined with the MOBITEX WAN, offers a reliable means of two-way communication in many applications.

VI APPENDIX 1 ABOUT ELECTRIC VEHICLE ENGINEERING

EV electrical design is all about high efficiency power control and conversion techniques, on-board batteries and associated chargers and drive motor systems. Modern commuter vehicle designs are capable of maintaining speeds in excess of 60 MPH and are capable of reaching this speed in less than 9 seconds. Much of this kind of performance improvement can be traced directly to recent improvements in solid-state switching devices and digital controls technology as applied to converters and inverters.

Accessory Power Electronics

Since electric vehicles do not have an alternator, many auxiliary systems like the heater and fan or lights contribute significantly to overall battery power drain. At one time these systems cut severely into the vehicles' operational time between charges so older designs were, by necessity, spartan in many respects. Modern EV's unlike their grandparents sport power assisted steering, brakes and essentially every other electrical accessory found in fossil fueled vehicles including air conditioning. These systems are now feasible because of the availability of comparatively low cost high efficiency DC to DC converter and DC to AC inverter designs in the 1 to 3 Kilowatt range. Zero voltage switched full bridge pulse width modulated converters in this class are operating at frequencies above 100 KHz and reach efficiencies of greater than 95%.

Battery Voltage

Most modern Electric Vehicle battery piles have a nominally charged potential of between 270 to 450 volts depending on the manufacturer. The benefits of using a high voltage low current power transmission system are not lost in EV applications, in fact higher voltages would be run if low cost semiconductors and approved isolation components were presently available. These voltages also turn out to be a good choice for 200/240 AC mains charging systems up to the 6 KW range residentially and for 3 phase 208-480 VAC 25 KW range chargers commercially.

Drive System

Todays EV's attain a higher drive train performance than was previously thought possible. Some of this is simply due to the basic benefits derived from using AC polyphase induction motors in the drive train. This motor type is noted for its high starting torque, good regulation and superior efficiency over its entire range. Efficiency aside, in its basic form, the absence of brushes and a commutator as well as simplicity of rotor construction makes the induction motor more economical than an equally rated DC motor, from the standpoint of initial cost and maintenance. One other interesting advantage to using this motor type is the fact that motor speed is directly proportional to applied AC power frequency. The "gas pedal" is in effect a variable frequency control.

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THE GLOBALSTAR MOBILE SATELLITE SYSTEM FOR WORLDWIDE PERSONAL COMMUNICATIONS ABSTRACT

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1.0 INTRODUCTION

Loral Aerospace Corporation along with Qualcomm Inc. have developed a satellite system which offers global mobile voice and data services to and from handheld and mobile user terminals with omni-directional antennas. By combining the use of low-earth orbit (LEO) satellites with existing terrestrial communications systems and innovative, highly efficient spread spectrum techniques, the Globalstar system provides users with low-cost, reliable communications throughout the world. The Globalstar space segment consists of a constellation of 48 LEO satellites in circular orbits with 750 NM (1389 km) altitude. Figure 1 shows the global coverage. Each satellite communicates with the mobile users via the satellite-user links and with gateway stations directly via the feeder links.

Voice and data communications are routed through the gateway stations. Each gateway station communicates with three satellites simultaneously. The gateway stations handle the interface between the Globalstar network and the PSTN/PLMN systems. Network Control Centers (NCC) provide management of the Globalstar communications networks. The NCC fuctions include: registration, verification, billing, network database distribution, network resource allocation, and other network management functions.

Globalstar transceivers are similar to currently proposd digital cellular telephones in size, and at a price only slightly higher. Each digital transceiver will have a single call-up number and unique serial number that will allow the end user to make and receive calls from or to that device anywhere in the world where service is authorized.

The Globalstar system is designed to operate as a complement to existing local, long-distance, public, private and specialized telecommunications networks. Service is primarily designed to serve the rural and thin route communications needs of consumers, government users, and private networks.

GPS Technology in a PCMCIA Format

By: Terry Dawson, Stuart Thomson and Ed Vignone

Rockwell International Corporation, Telecommunications

ABSTRACT
NavCard™: GPS Technology in a PCMCIA Format

The focus of this paper will be the combination of a PCMCIA format, OEM Global Positioning System (GPS) receiver and mobile computers. The ready mobility of portable computers brings with it the uncertainty of location. Real-time location information is available utilizing the Global Positioning System. The packaging of a GPS receiver in the PCMCIA format has opened up a wide variety of opportunities in automatic vehicle location, marine navigation, aviation and industrial applications. Coupled with the growing availability of software that provide maps and travel related information, the NavCard™ from Rockwell is quickly making GPS a standard feature in mobile communications devices.

Introduction

The Global Positioning System (GPS) is a space-based radio navigation system. This system provides worldwide all weather continuous coverage for position, altitude, time and velocity determination, It is available to an unlimited number of users using a passive radio receiver.

The completion of the GPS constellation brings with it 24 hour a day, world wide, all weather operation. The availability of low cost, compact GPS receivers have been available at the OEM level for several years. Many OEMs have built GPS specific products based on these products. These products have had the basic components of:

display, keyboard, power supply, processor and housing. Recognizing that these are the basic components of a computer, it is was easy to conclude that portable computers would be an excellent platform to utilize GPS technology.

Market Requirements

The ready mobility of portable computers brings with it the uncertainty of location. Companies often need to locate their mobile employees at a moment's notice. Tracking one's location is equally important in emergencies, in avoiding delays, for automatic vehicle location and for marine and aviation applications. The need for a product which can easily integrate with the wide range of mapping, navigation and location software available for the mobile computer user was expressed by both hardware and software manufacturers.

The largest users of GPS have been what could be termed the upgrade market. This market consists of those users of alternative location/navigation technologies such as Loran C and have primarily been in the marine and aviation markets. These users viewed GPS much as a PC user views the availability of new processors. As such, the first large application of GPS was simply replacing the old technology (Loran C) with the new technology (GPS) in the same package. As mentioned above, these GPS application specific packages consist of the same basic components of a PC. These products initially offered a very simple non-graphical user interface . Recent product introductions have begun to offer limited graphical user interface(GUI). These interfaces fall short of those available on the typical PC products.

Manufacturers of PCs recognized that the market being served by the application specific GPS handhelds could easily be addressed by their products. The introduction of smaller notebook computers and Personal Digital Assistants (PDAs) only accentuated the similarity between the GPS application specific products and their own offerings. The inhibiting factor remained that with OEM board level products the decision to incorporate GPS into the platform needed to be made at the time of manufacture. To overcome this issue, several companies offered external products which interface into PCs via one of the serial ports. The drawback to these products was the resistance of PC users to external boxes and cables and the need to dedicate the serial port to GPS. PC manufacturers insisted that for GPS to be accepted it would need to be essentially an after market add on. Their advice was that the GPS product should utilize and be contained completely within the PCMCIA port. This eliminates the need to make a manufacturing decision and eliminates the external components.

A second demand for the embedded capability of GPS was expressed by the growing number of software companies which are offering digital map based products. These products offer the user the interface look of a paper map which is what they are accustomed to using. In addition to the typical road locations, many of these products include landmark and destination information. This information could include hotel, restaurant, emergency services, shopping and entertainment locations. The advantage of the real time location capability of GPS offered an obvious feature which the software companies wanted to add to their products. The addition of GPS would offer the user their exact location and the ability to display their route as a series of dots on the screen. The real time location information is valuable in unfamiliar areas and even in familiar areas if you are forced by traffic or road conditions to detour from your usual route. The hurdles faced by software manufacturers in offering GPS were the same as those faced by the hardware manufacturers.

The challenge was obvious. To make GPS an embedded technology, the current product configuration would need to change. The availability of computers incorporating PCMCIA slots appeared to be the perfect solution for both the hardware and software manufacturers. The goal was to offer the functionality of the current GPS product within a package compliant with the PCMCIA standard. This included the addressing the issue faced by other wireless products which is the antenna placement. An external antenna would appear to users as another external box and cabling. But since GPS is a line-of-sight system, the antenna needs to be capable of being placed in a position for maximum visibility of the sky. The compromise between these two contrasting requirements was to integrate the antenna on an extended PCMCIA format but allow for the easy removal of the antenna for remote placement. This compromise offers the NavCard user the flexibility to utilize GPS technology without cumbersome external components without rendering the product useless in demanding operating environments.

SYSTEM OPERATION

The Rockwell NavCard™ receiver is a PCMCIA, five parallel-channel, Global Positioning System (GPS) receiver with its architecture derived from Rockwell's NavCore V™ and MicroTracker™ (figures 1, 2, 3). This architecture is suitable for integration into a wide variety of Original Equipment Manufacturer (OEM) products. The NavCard™ receiver uses spread-spectrum receiver technology for reception of L1 GPS, 1575.42-MHz Standard Positioning Service (SPS) signals. This highly integrated digital receiver incorporates four custom Rockwell devices, including a fully integrated Gallium Arsenide (GaAs) RF front-end. This minimizes the receiver's size to a self-contained PCMCIA compliant Type II extended form factor. At the same time, this maximizes the reliability of the product. Designed for high performance in a wide

range of applications, the NavCard™ receiver is built to satisfy the requirements of the PCMCIA standards.

Ease of acquisition is realized upon power-up by providing the receiver its Position, Velocity and Time (PVT) data from a completely powered down state. Rapid Time to First Fix (TTFF) is achieved utilizing efficient search algorithms that make use of the five parallel channels of the receiver. A typical TTFF is 30 seconds with a current almanac loaded in EEPROM, ephemeris data stored in static Keep Alive RAM and user initialization parameters that are provided, which have position within 100 km, velocity within 75 m/s, and time within five minutes. Acquisition can be achieved with vehicle dynamics as high as 950 m/s in velocity and 10 m/s/s in acceleration. Typical re acquisition times caused by obscuration with duration's less than 15 seconds are less than 10 seconds once the obscuration is cleared. Navigation solutions can be maintained with vehicle dynamics as high as 950 m/s in velocity and 40 m/s/s in acceleration.NavCore V™ Architecture

Navigation solutions can be achieved and maintained in several different modes. A Satellite Navigation solution (3-D solution) will be generated automatically from the acquisition state. In instances when five or less satellites are available, the NavCard™ receiver tracks each simultaneously. However, when more than five satellites are available, the NavCard™ receiver utilizes one of the five channels to track up to five additional satellites for a total of nine satellites tracked . The unit accomplishes this task by designating one channel as a utility channel. Therefore, if one channel experiences an outage, the utility channel will supply an alternate satellite which is in view. When the satellite data is available, the NavCard receiver will use the measurements from the satellite(s) that it is tracking on the utility channel to compute an over determined solution.

A commanded three satellite (2-D) solution can be approached from an acquisition state with a user supplied altitude via an initialization message. A three satellite (2-D) solution, Altitude Hold, can also be approached from a Four Satellite Navigation state automatically if only three satellites become visible due to obscuration or by OEM commands. The OEM can command an altitude to be used in the navigation solution via an "Amended Altitude" command. In all cases, the OEM can command a Satellite Viewing Mask Angle from -15 to +35 degrees with respect to the horizon. Provision is also made for the OEM to manually select or de-select specific satellites.

A navigation solution can be approached from an acquisition state with no user input parameters. The TTFF for such a start is longer than that for an initialized start or a warm start, but generally less than 10 minutes.

Selective Availability (SA) and inherent GPS inaccuracies can be reduced through the utilization of differential corrections. The NavCard™ receiver will accept RTCM-104 Differential GPS (DGPS) messages from a Coast Guard beacon receiver or other commercial Differential receivers to minimize the effects of SA and other GPS system inaccuracies.

Navigation solutions, referenced to the WGS-84 Earth model, in both geodetic and Earth-Centered-Earth-Fixed (ECEF) coordinates complemented with Universal Time Coordinated (UTC) are provided to the OEM once a second.

The OEM or system integrator is provided with a licensed applications program interface (API) which will support the integration of his application to DOS or Windows.

NavCore V™

The NavCore V™ was the original commercial GPS product offered by the DCD division. Within a module 2.630 by 4.000 by 0.730 inches, the NavCore V™ implemented a five channel receiver accepting a 1.57542 GHz signal from an antenna and providing the navigation solution via a 9600 bps serial interface. The only necessary power requirements were plus and minus five volts. All communication to and from the NavCore V was via the two way serial channel. An on-board real time clock and low power static RAM would maintain time and last position if the NavCore V was placed into a power down state.

Figure 1 details the system architecture of the NavCore V receiver. The RF signal is applied via a pre-select filter to the LNA input of the GaAs front end. The output of the LNA is passed through the post-select filter through the input to the first mixer. The remainder of the GaAs front end implements a dual conversion receiver with the LO reference supplied by a low noise 1ppm 10.94 MHz TCXO. The 1.28 MHz I and Q IF signals are then applied to the second IF/AGC circuits implements in another custom five channel DSP IC. The five channel DSP receives the siginal from the IF device, performs code and carrier demodulation,quantization, signal correlation and provides a multifunction interface (MFI). The AAMP II provides program control and memory access. The RAM, ROM and EEPROM hold the necessary programs and data to support the DSP and AAMP II microprocer in performing the navigation solution. The MFI provides the bi-directional serial data interface host.

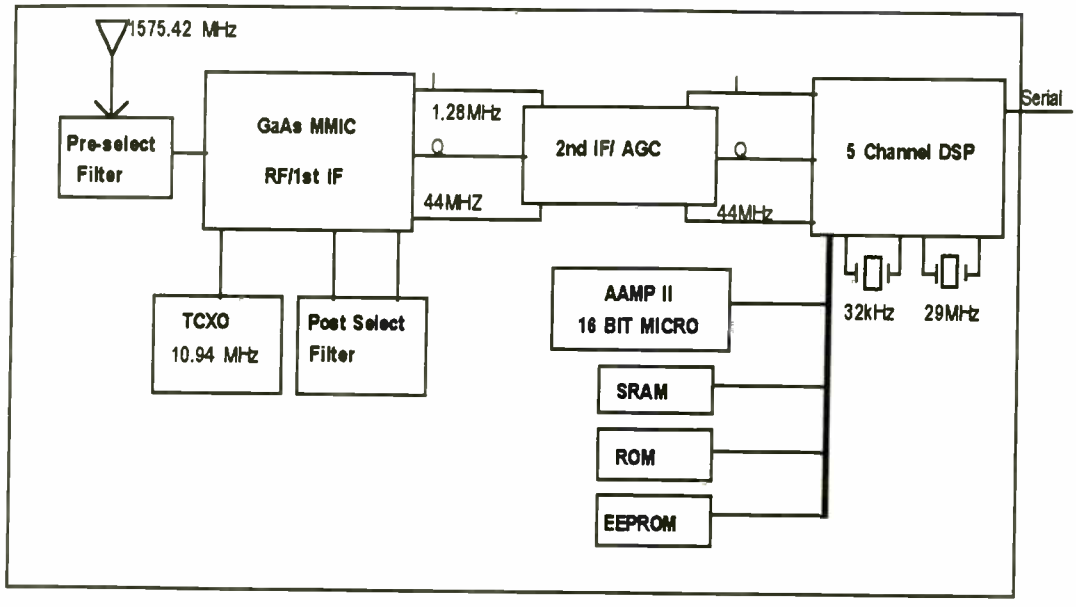

Figure 1. NavCore V Architecture

MicroTracker™

The MicroTracker™ reduced the size of the NavCore V down to 2.0 by 2.8 by 0.53 inches. In addition, the requirement for -5 volts was eliminated, and voltage supervisory circuitry added to guarantee RAM integrity during power up and power down transitions. Power management was added, cycling power to the RF circuitry to further conserve precious battery life. The duty cycle of the RF front end can be varied from a low of 20% to a maximum of 100%.

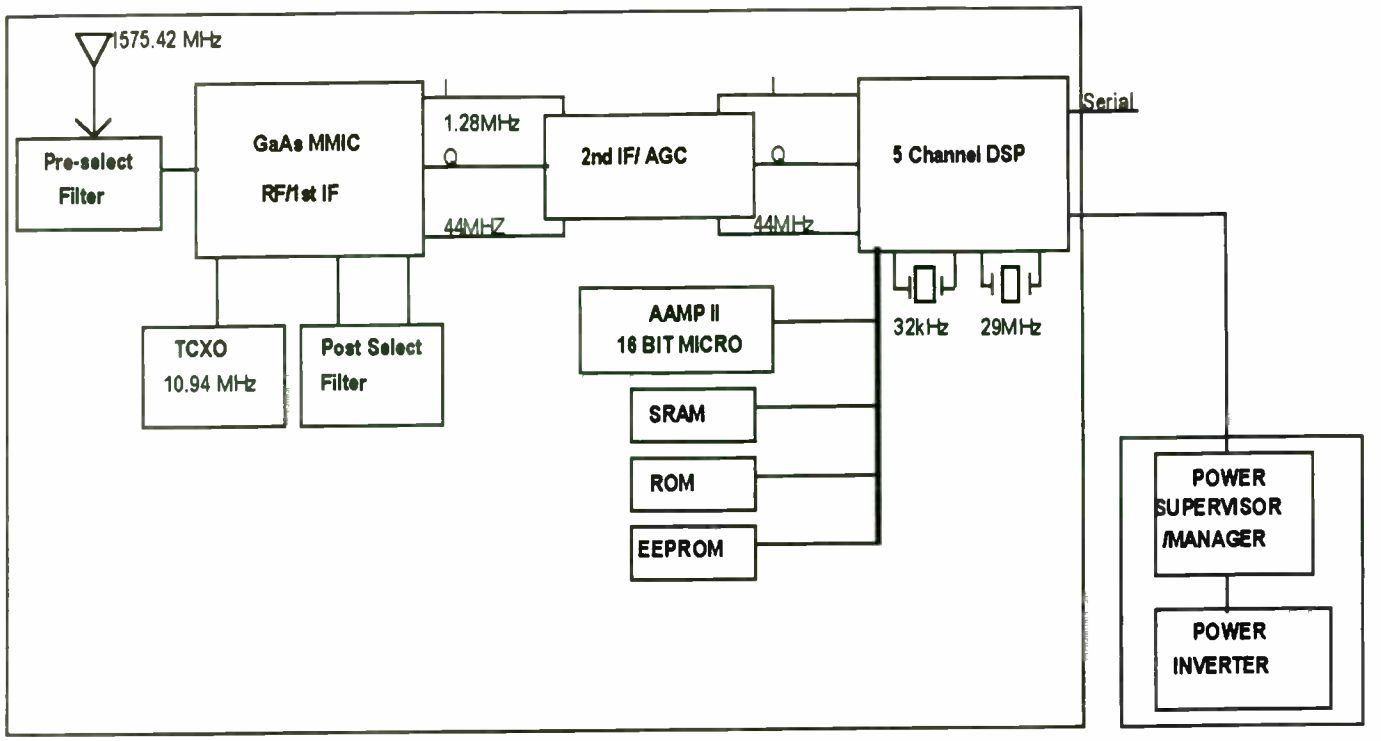

Figure 2. MicroTracker Architecure

NavCard™ Architecture

The NavCard™ system architecture is built upon the system architecture of the MicroTracker. In addition to adding the PCMCIA interface circuitry (described below) to the NavCard™ the power supervisor circuits present in the MicroTracker are removed.

PCMCIA Interface

The PCMCIA PC Card 2.01 Standard defines two types of cards, memory and I/O. All PC cards are required to power up in the memory only state to ensure backward compatibility with PCMCIA PC Card Standard 1.0. The capabilities of the card are stored in the card information structure (commonly called the CIS table) which is read by the host platform during a card insertion or during host boot (if the card is already inserted). For I/O cards, if the necessary host platform resources are available, the card may be configured into the I/O state. If the necessary resources are not available (I/O address space, power, interrupts, etc.) the card will be rejected by the host platform and will not be initialized. This process of initialization is performed by a generic card enabler through the card and socket services software residing on the host.

The PCMCIA interface is accomplished In the NavCard by using a gate array to implement card configuration registers, ROM to hold the card information structure and a UART to convert the serial data stream from the NavCard navigation engine to a parallel format suitable for the PCMCIA bus.

The custom gate array handles the PCMCIA bus protocols, performs address decoding for the UART and ROM, generates NavCard clocks, controls NavCard power management and implements the three card configuration registers necessary for proper initialization and setup of the NavCard. One requirement of the NavCard was to appear as a standard COM port for PC host platforms since the vast majority of PCMCIA platforms and 80X86 PCs. This requirement also maintains backward compatability with the existing NavCore V PC compatable software base.

The Card Information Structure (CIS) is a series of tuples (linked list of data structures) stored in read only memory. The CIS starts at the base of attribute memory for the card and is approximately 128 bytes in length for the NavCard. The CIS for the NavCard defines the card as a serial device, capable of responding to the four standard IBM PC Compatable COM ports plus a fully decoded address window for other host platforms. Additional information stored in the CIS includes manufacturer, card name and model number, power requirements and handshaking requirments. An index value pointing to the card configuration registers is stored in the CIS. During card insertion or host platform boot, a generic card enabler can read the CIS table and properly initialize the NavCard.

The NavCard implements three of the defined card configuration registers. The first register, the configuration option register, switches the card from memory mode (power on default) to the correct I/O mode (COM1-COM4, I/O Window) and selects the type of interrupt desired, pulse or level. The SRESET bit will reinitialize the NavCard PCMCIA interface and place the card into memory mode.
The second of the three registers, the card configuration and status register implements interrupt control functions on the PCMCIA bus, plus controls the main power on the card. If the power down bit is set, then the card is de-activated with the exception of the PCMCIA interface.
The final register is the pin replacement register. In I/O mode, the ready/busy line on the 68 pin connector is replaced by a ready/busy bit in this register.

Since the basic navigation engine in the NavCard is a serial device, some means of converting the serial data to 8 bit parallel format across the PCMCIA bus is required. The desire to implement a standard COM port configuration and the desire to work under the Windows 3.1 environment narrowed the choice of a Universal asyncrious receiver transmitter (UART) to the 16550. When configured to the standard COM port addresses, the UART appears to the host platform in an identical fashion as a standard serial interface.

Power Management

Generic card enablers enable the NavCard with power supplied. While this is acceptable for a modem, the NavCard does not offer a sleep mode which reduces power during periods of no activity. Such a sleep mode is difficult to implement in a GPS receiver, since the associated application tends to be passive, that is, merely accepting data from the receiver.
Since the GPS data is of little value unless the application is knowledgeable about GPS, a second control bit was added to power up the actual navigation engine. This bit is not implemented in the card configuration registers, but rather makes use of one of the handshake control bits in the UART.
Thus a GPS knowledgable application would set this bit to enable power to the navigation engine. Thus the dual requirements of generic card enabler compatability and battery power conservation are met.

During card initialization the power down bit in the card configuration registers is cleared (applying power to the NavCard), but the power control bit in the UART is held in the off state. Thus the PCMCIA interface to the NavCard is powered, allowing inspection of the CIS table and configuration of the card. Setting the power control bit in the UART applies power to the navigation engine and serial communications to and from the host platform is enabled. The two power control bits are independently set and cleared. Both bits are OR'd together to turn on power. Resetting of either bit removes power to the engine, but keeps a keep-alive voltage on the navigation engine RAM and real time clock. This allows rapid re-acquisition of signals if the card is powered down by a suspend power event from the host platform or under command from the host application.

Power cycling of the RF circuitry is controlled by serial messages to the NavCard from the host application. As in the case of the MicroTracker, the power may be cycled from a 20% to 100% duty cycle. Optimum settings of the power cycling feature are determined by the dynamics of the GPS platform (how fast it is moving, etc.) and the platform power source.

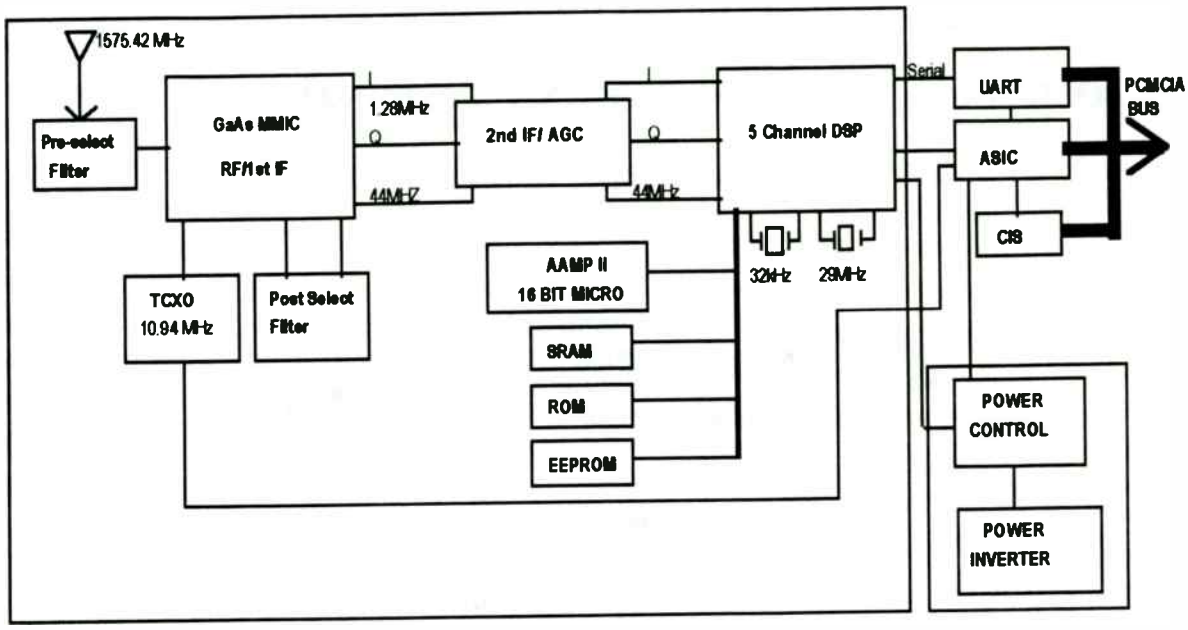

Figure 3. NavCard Architecure

The standard GPS API (Applications Programming Interface) is designed to greatly simplify the task of developing end user applications which take advantage of the power of dynamic position information provided GPS. The application developer who is familiar with higher-level language applications running under standard operating systems is able to code using high level functions which initialzie and control the GPS receiver engine and provide current position, velocity, time and status information. This allows the application programmer to quickly take advantage of GPS without needing to develop an understanding of detailed receiver engine protocols.
The standard API allows communciation (both transmit and receive) with the GPS receiver without familiarity with detailed hardware and software interfaces, data and word formats and/or protocols, since these related functions are handled within the API and are transparent to the application code.
In addition, the standard API performs the necessary position conversion between the GPS WGS-84 datums and other datums in use world-wide.

Summary

Rockwell International has applied its world leading PCMCIA (Personal Computer Memory Card International Association) technology to its GPS NavCore products family to produce the world's first OEM GPS Receiver completely contained in a PCMCIA Type II format, the NavCard. This latest step continues the continued reduction in the size and power of GPS receivers. More importantly, the NavCard brings GPS within the reach of becoming an embedded technology available to a wide variety of portable computer platforms.

ELECTRONICALLY STEERABLE MILLIMETER WAVE AUTOMOBILE COLLISION WARNING ANTENNAS WITH TUNABLE CERAMIC PHASE SHIFTERS

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Abstract

In this paper, a new electronically steerable ceramic millimeter wave automobile collision warning microstrip antenna will be presented. These antennas are lightweight, low volume, low profile and conformal. They have low fabrication costs and are easily mass produced. They are thin and do not perturb the aerodynamics of a host automobile. Linear, circular, and dual polarization are achieved with simple changes in feed position. Beam steering is accomplished by varying the relative phase between radiating elements. In planar array, both horizontal and vertical beam can be combined to provide full scanning capabilities. Tunable ceramic phase shifters are used in these antennas. They offer several advantages over other devices such as PIN diode phase shifters, ferrite phase shifters, etc. The ceramic phase shifters are inexpensive, rugged (leading to low failure rates), are low power, and are easily reproducible and can be incorporated into the feed structure of the microstrip planar array antenna.

Electronic ceramics such as Barium Strontium Titanate suitably doped can be tailored to have a curie peak and dielectric constant in a wide range of desirable values with low loss tangents. By applying a static bias voltage, the dielectric properties of such ceramics can be changed by 30% to 54%. The dielectric constant itself can range from a value of 15 to 10,000. The application to compact antennas that can be conformal to the curved front or rear bumper of an automobile is obvious. The paper will review the research on the production of tunable ceramics and steerable antennas.