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A VNU BUSINESS PUBLICATION

OCTOBER 1988

# Electronics

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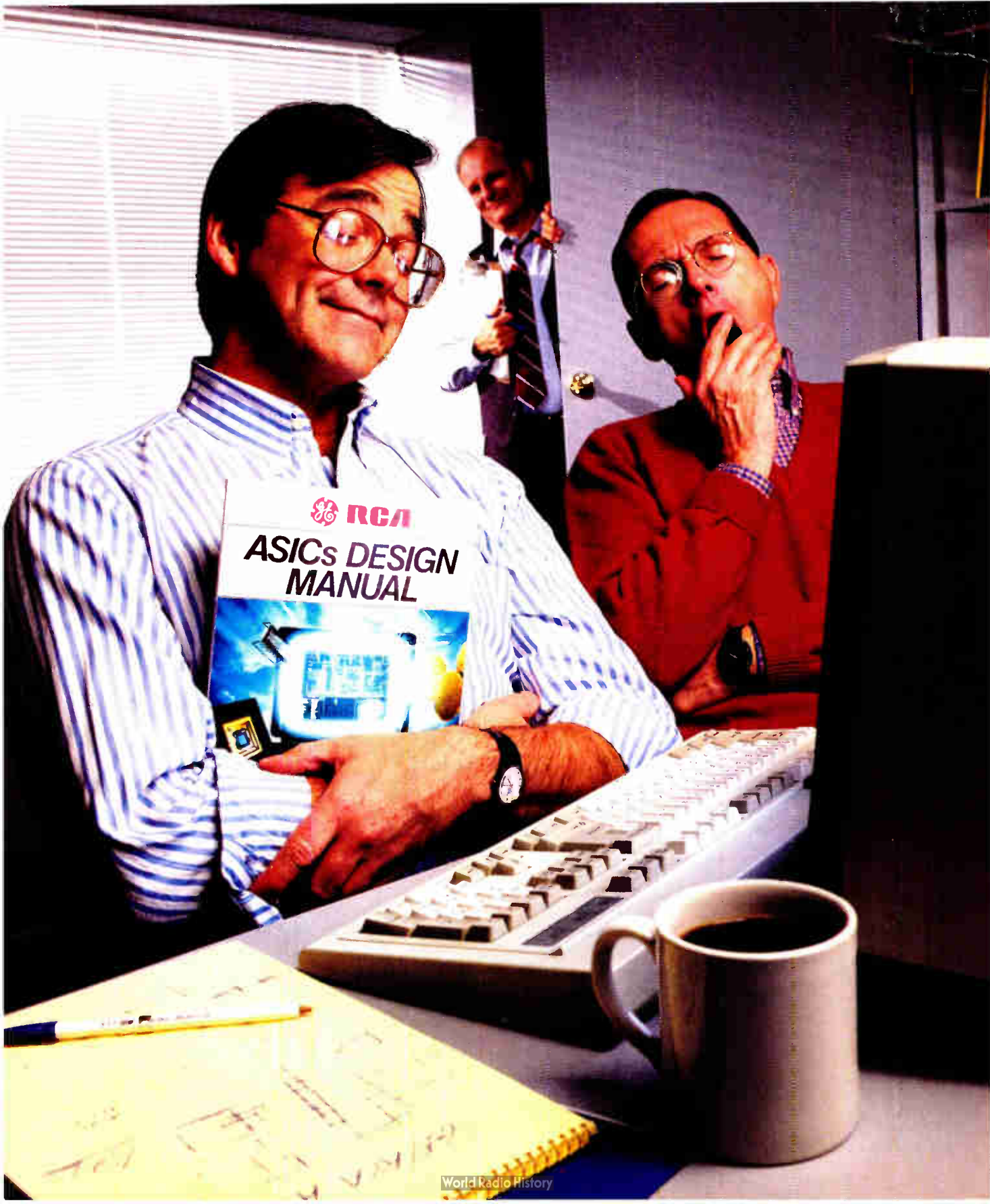
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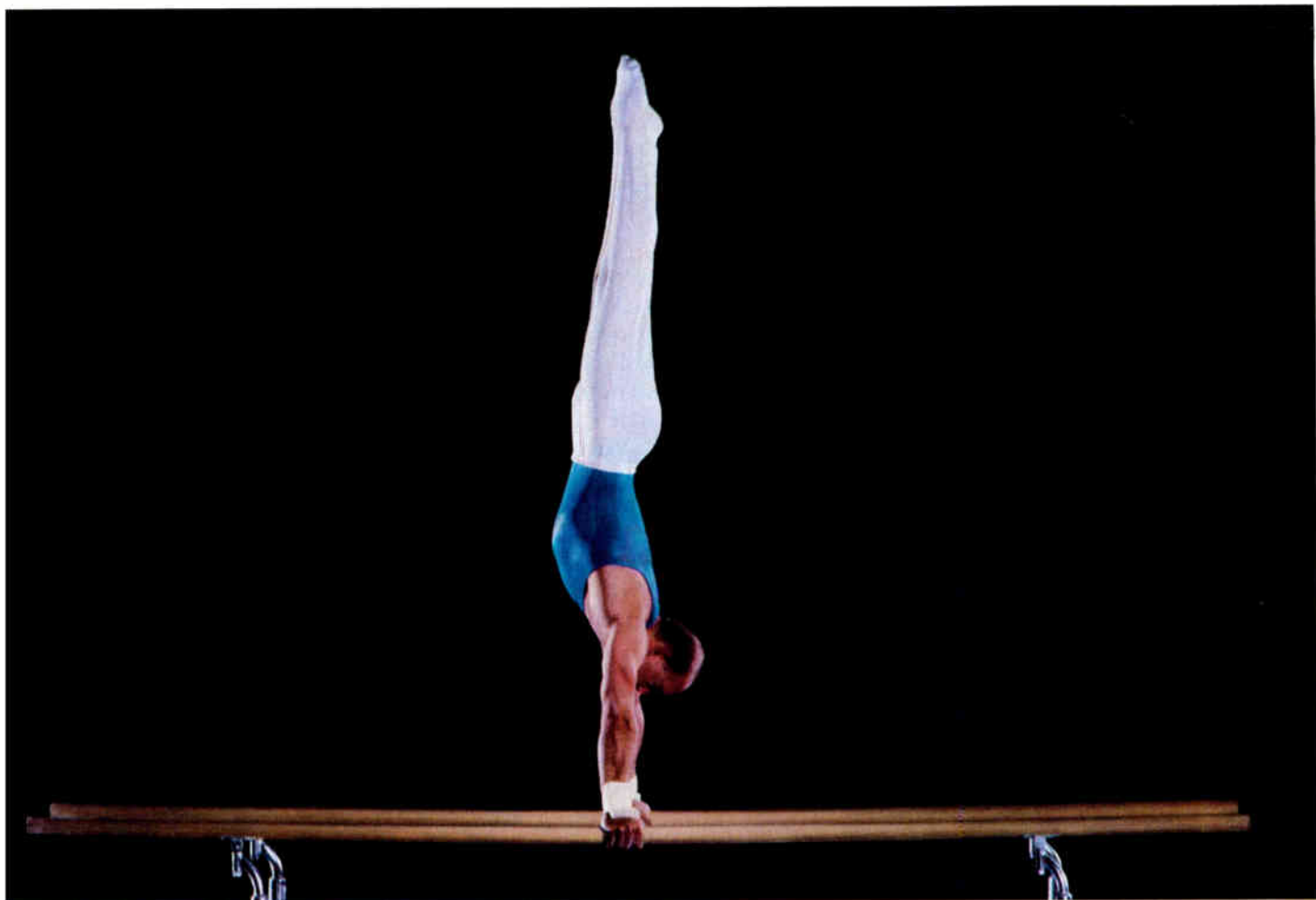
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## WEAK-KNEED WALL STREET HARD TO BEAR

But one benefit of the market's quirky treatment of the electronics industry could be weaning startups off stocks in favor of more stable financing sources



**M**ost investors won't have trouble remembering exactly where they stood the day stock markets crashed—Black Monday, Oct. 19, 1987. That's because they've been nowhere since.

For the capital-needy electronics industry, investor phobia is proving especially frustrating and costly. Many emerging-growth firms have been without the means to raise money—as their once-in-a-boom-time chance evaporated. And stock investors are still not ready to jump back into the market, no matter what the indicators look like.

If chip and system orders are at record levels, the fear is they've peaked. If prices go up, wary investors wonder how the industry can defy its history of always making things cheaper. If prices drop, Wall Street comes to the

screaming conclusion that profits will end. Misguided fears have given high tech a bad rap.

Even the pace of technology is worrying investors, as faster products hit the markets quicker (see *Technology Outlook*, p. 70). Analyst Gary Smaby, managing director of Needham & Co. in Minneapolis, says the concern is linked to perpetual product transitions and shrinking product-development cycles. That raises questions about amortizing heavy research and development expenditures over just 18 months for something like a minisupercomputer, he says.

With much of the industry reporting lower-than-expected second-quarter earnings, attention is now focused on third-quarter reports. Silicon Valley analyst Ed Henderson in Los Altos, Calif., says the early anecdotal indicators in September show a slow down for multilayer printed-circuit board suppliers, which were seeing a boom along with chip makers. "Now rather than worrying about how to fill a customer order, they are worried about where the orders are coming from," he says. His formal short-term indicators still say boom, however.

But some good may result from all the angst pervading investor psyches—it could lessen the industry's dependence on profit-pressing stock markets by redirecting the high-tech sector's money hunt to new channels of financing. Already, established manufacturers are backing more startups in moves to get into new technology or markets. With more stable funding, entrepreneurs could waste less time fanning market forecasts in hopes of raising investor interest. That alone could help save the industry a heap of money by keeping expectations in check.

**J. ROBERT LINEBACK**

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# Electronics

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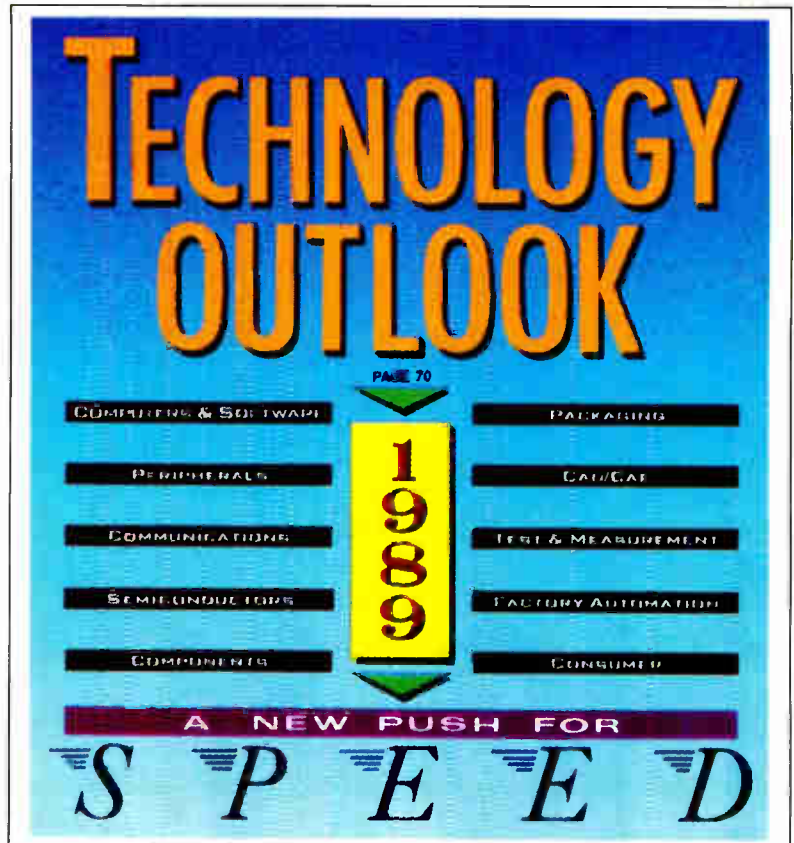
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LSI Logic and Motorola keep pushing giant gate arrays

# How the fa

Our new 75ns PAL<sup>®</sup> device is fast enough to prove that standard logic shouldn't set the standard anymore.

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Decoder				
74151	tPD	11.0	15.0	7.5
Mux				
Register/Latch				
74374	tCO	10.0	9.0	6.5
Octal Register				
74373	tPD	8.0	6.0	7.5
Octal Latch	tLEO	13.0	11.5	7.5
Counters				
74161	tS	5.5	8.0	7.0
Four bit Ctr	tCO	11.0	13.5	6.5
74269/869	tS	2.5	5.0	7.0
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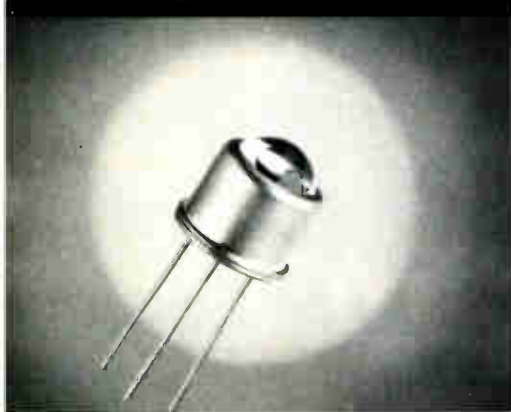
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### LETTER FROM WASHINGTON

## THE INFLUENCE INDUSTRY GEARS UP FOR 1989

### WASHINGTON

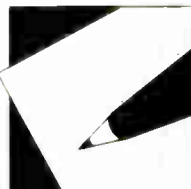
**A**utumn in the nations' capital: the mercury is falling, the Redskins are trying to repeat as champions of the National Football League, and the 100th Congress is back in town to wind up its final session.

After summer recesses that included the two major-party conventions, President Reagan and the Congress returned in September to haggle over a revised fiscal 1989 defense budget; new bills to regulate defense procurement; and a tax bill designed to clear up confusion over the last tax bill. But since this is an election year, the action isn't in Congress.

It's the city's giant influence industry—lobbyists, cooperative councils, and trade associations—that are making things happen. They're revving up for the transition from the Reagan administration to its successor. It is then that these organizations must focus their skills to influence the new government's agenda.

For the electronics industry there are some big issues on the table. Waiting to be resolved is the extension of the research and development tax credit and the formation of a coherent national science and technology policy led by an influential national science adviser. To a lesser degree, the agenda also includes a range of issues relating to U. S. competitiveness in world markets.

The spectre of new legislation regulat-



ing defense buying practices has the greatest immediacy now because there are already more than a half-dozen bills waiting for congressional consideration. Those bills, proposed by Sen. David Pryor (D-Ark.) and Rep. Barbara Boxer (D-Calif.), among others, are provoking worries in the defense industry, where the prevailing viewpoint is that too many rules already apply.

"I would hope we know more about what the illness is before we start prescribing a cure," says Don Fuqua, a former 12-term congressman from Florida and now the president of the Aerospace Industries Association. "They should wait for all the facts to come in."

But that doesn't mean some legislation might not be appropriate. Both Fuqua and J. Richard Iverson, president of the American Electronics Association, support a plan to eliminate price from all but the last stage of the bidding process, so that contractors initially deliver only technical and management plans. A big part of the scandal—"the weak point in the system," Fuqua says—revolves around the selling of confidential information about bid prices before companies submit their "best and final" offers. By permitting each bidder only one chance to name a price, much of the incentive to discover secret bid information is removed.

Also of primary concern to the AEA



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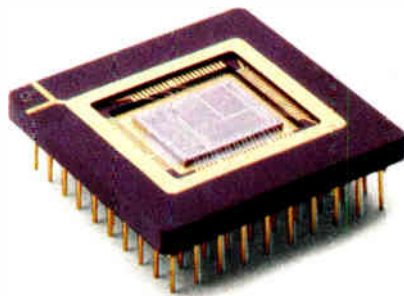
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**AMERICAN JOURNALIST, 1879**



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and such groups as the Electronic Industries Association, the Computer and Business Equipment Manufacturers Association, and others, is the research and development tax credit, which will expire at the year's end. At issue is what these groups call the single biggest financial incentive for driving technology—a 20% credit companies can claim on their tax returns for investments in R&D.

The House is now looking at a technical corrections bill that would extend the credit for two years, but cut in half write-offs for R&D equipment costs. The full cost of such equipment can now be written off, but the House measure would allow only a 50% write-off. The result is an effective credit of 13%, says a staff assistant at the Cortech Council on Research and Technology, a Washington-based group that is coordinating the lobbying efforts for 160 companies, trade associations, universities, and laboratories.

A Senate bill, meanwhile, would extend the credit in its present form for six months so that Congress and the next president can devise a long-term strategy for the credit. That's more to the liking of Cortech's members, which range from IBM Corp. to the Semiconductor Industry Association, and from Harvard University to industry consortium Microelectronics and Computer Technology Corp. They're hoping to convince legislators that an expanded credit would not only stimulate investment, but is also key to making U. S. products competitive in a global economy.

**MORE FOR ALL.** "We believe the R&D tax credit should be permanent and maybe larger," says the AEA's Iverson. "We're trying to get the credit back up to 25% [where it stood before tax reform] and make it applicable to startup companies and firms that aren't growing. We need a provision that helps when times are bad." Adds Oliver R. Smoot, executive vice president at CBEMA: "This is an issue of competitiveness, not politics."

Picking up on that theme is the Council on Competitiveness, a study group headed by John Young, president of Hewlett-Packard Co. The group issued a wide-ranging but detailed report on the issue Sept. 7, and is hoping that the next administration will adopt all or some of its recommendations on helping the private sector regain its technological edge and boost productivity and quality; improve the educational system; and create legislation that can help business help itself.

The American Physical Society and the Institute of Electrical and Electronic Engineers, along with 21 other science and engineering organizations, are pushing both candidates to increase the power of the

presidential science adviser by giving the individual direct access to the President. They also want a quick appointment. In open letters to the candidates, the societies urge that since "leadership in science and technology policy must come from the White House... a hiatus in filling the position of science and technology adviser at the start of a new administration could prove costly to the nation."

That's true no matter who wins the presidency, Massachusetts Gov. Michael Dukakis or Vice President George Bush. Lobbyists say it's still not really clear what many of the differences between the candidates for the presidency are and how those differences might manifest themselves. "There are a lot of issues where either new administration, Dukakis or Bush, will take different views from the present one," says CBEMA's Smoot. Both Dukakis and Bush are likely to take a harder line on enforcing

### The industry asks: will the 20% tax credit for R&D be renewed?

antitrust legislation than the Reagan administration did, for example, but it's not clear that Dukakis would be any tougher than Bush. And while defense policy and ex-

perience have become the main campaign theme for the Vice President, most Washington insiders don't think either candidate, as President, will have many options in the defense budget.

"Everybody agrees the budget's not going to grow for the next two to three years," says a Washington-based policy analyst for a defense firm. "There won't be any new weapons systems until something is done about the [federal] deficit." Adds the EIA's Rosenker: "There needs to be a recognition that deficit reduction is probably as important for the future of this nation, or more so, than building a strong defense."

With the national debt now well beyond the \$1 trillion mark, the Pentagon's next five-year plan will be the most telling predictor of the fate of major defense programs. It will detail which programs can be cut, which can be stretched out, and which older programs can be upgraded through retrofits of new technology.

The future for the plan will be sketched out soon after the election, now only a month away. The influence industry is lying back, quietly waiting for its outcome, and preparing to aid the transition from one administration to the next. White papers, reports, and analyses are being prepared on everything from reestablishing a consumer electronics industry in the U. S. to basic issues of U. S. industrial competitiveness. These issues will be presented, some privately and some publicly, in the autumn months to come as the lobbyists try to convince the new Congress and administration to take up their causes in 1989.

—Tobias Naegele

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# ELECTRONICS NEWSLETTER

## NOW, A JAPANESE ACTIVE-MATRIX LCD THAT MEASURES 14.26 IN...

A pair of Japanese companies has nudged the record for the largest active-matrix liquid-crystal display up to 14.26 in. from 14 in. The new display, developed by IBM Japan Ltd. and Toshiba Corp., boasts resolution of 1,440 by 1,100 pixels in monochrome, and 720 by 550 pixels in color. Despite its area, the panel's dot pitch is a tiny 200  $\mu\text{m}$ . But commercial production, which is two or three years away, won't be an easy task because it will probably take huge fabrication equipment to make the panels economically. What that means is that equipment must be able to turn out at least four to eight panels on one sheet of glass so that a single defect doesn't destroy the whole production run. That's why color TV sets with active-matrix panels are now limited to the 2- to 5-in. range. □

## ...AND TWO CONSORTIUMS HAVE EYES ON A BIG DISPLAY FOR HDTV

Even as U.S. companies are being exhorted to get back into consumer electronics via high-definition TV (see p. 61), the Japanese aren't letting the grass grow under their feet. Now, two consortiums want to perfect large screens for the onrushing technology, also known as advanced TV. The Ministry of International Trade and Industry and 12 companies are aiming to develop a liquid-crystal display measuring 1 m<sup>2</sup> and have asked the government for about \$40 million to fund the seven-year project. Meanwhile, the Ministry of Posts and Telecommunications is planning a similar project with four other companies and has applied to the Japan Key Technology Center for \$30 million. The technology center's decision is due before the end of the year. One reason for all the interest is that the technology could be adapted to large paper copiers and optical computers. □

## DATA GENERAL PROVIDES A BIG POWER BOOST FOR ECLIPSE MV USERS

Even though Data General Corp. is supporting Motorola's 88000 reduced-instruction-set computer chip [*Electronics*, April 28, 1988, p. 32], it is not forgetting its current customers. In fact, it is giving them a tremendous boost in power and enabling them to stay with the family by souping up its Eclipse MV complex-instruction-set architecture with new processors implemented completely in emitter-coupled logic. The chips deliver more than 50 million instructions/s in a symmetric, four-processor configuration. And while Data General was at it, the Westboro, Mass., company unveiled a 400-million-bit/s channel subsystem that links several MV systems and peripherals in a high-speed network. It also brought out AOS/VS II, a version of the AOS operating system that enhances communications and increases system uptime. Earlier MV systems include ECL and TTL, but the MV/40000 family is all ECL, delivering 14 mips per processor. The family can support one to four processors and is aimed at data-base processing involving multiple users. □

## THE ON-CHIP-RF MARKET GETS ANOTHER PLAYER

Suddenly, the still-developing market for wireless rf integrated circuits is getting busy. Catalyst Semiconductor Inc. of Santa Clara, Calif., is going to market with a chip for markets that now use hybrid multichip solutions—smart cards, intelligent identification tags, memory cards, and electronic door keys. Unlike the multichip, battery-powered hybrid solution built around a microcontroller offered by Dallas Semiconductor Corp. and intended for industrial control [*Electronics*, September 1988, p. 28], the Catalyst offering is a single-chip, serial, electrically erasable programmable read-only memory that uses an on-chip rf transceiver to communicate data and to transmit enough power to the chip to modify the EEPROM, if necessary. □

# ELECTRONICS NEWSLETTER

## TI LOOKS LIKE A WINNER IN MILITARY ASIC CONTEST . . .

**L**ook for Texas Instruments Inc. to be the major winner this month in the Defense Department's Microelectronics Manufacturing Science and Technology program. Sponsored by the Defense Advanced Research Projects Agency and the Air Force, MMST is the Pentagon's aggressive plan to develop a futuristic, peopleless, paperless, quick-turnaround production capability for military application-specific integrated circuits [*Electronics*, Sept. 3, 1987, p. 31]. TI isn't talking. But competing contractors say that MMST program managers have been negotiating with the Dallas firm since early this year, and concede that TI is the heavy favorite to receive the bulk of the \$75 million allotted for the effort. □

## . . . AND JOINS UP WITH SPIRE TO OFFER SIMOX WAFERS

**T**hings are looking up for semiconductor manufacturers seeking wafers incorporating a silicon-on-insulator layer for device isolation. Texas Instruments Inc., Dallas, and Spire Corp., a Bedford, Mass., supplier of specialty wafers, have teamed up in an agreement that has TI providing 4-in.-diameter Simox wafers to Spire for it to sell to device makers. Wafer annealing and deposition of an epitaxial layer will be done by Spire, if the customer desires. The Simox process employs ion implantation to build a silicon dioxide insulator between the bulk silicon and the later-deposited epitaxial layer, in which active devices are fabricated. The insulator makes devices resistant to radiation because it inhibits electron mobility between the substrate and epi layer. SiO<sub>2</sub> also prevents latchup between adjacent CMOS transistors, allowing closer packing densities. The catch is that until recently SOI wafers have not been widely available. But the TI-Spire agreement, coming at the same time as an announcement that Kopin Corp. of Taunton, Mass., is making SOI wafers using a different process (see p. 56) could change that. □

## MAKER-USER DRAM PARTNERSHIPS? IT'S NOT LIKELY, AGREE INDUSTRY LEADERS

**I**f makers and users of dynamic random-access memories are planning to set up a facility together to produce the critically short chips, it won't happen soon, say industry experts. The reason: economics. Talk of the possibility was generated when Murray A. Goldman, senior vice president of Motorola Inc., said at a forum in Boston that Motorola was discussing such an alliance. A Motorola spokesman confirms that talks have taken place, but adds that they were "very exploratory in nature." One industry official says cost is the main obstacle to such a deal. A facility would cost about \$200 million and take 18 months to get into production. Even if a group of companies could afford to make that kind of investment and wait for a return, there's the cyclical nature of chip shortages to consider and what is likely to happen to DRAM prices when anticipated production comes on stream in the next year or so. Any customer committed to 1990 prices of, say, \$6 per megabit would be mighty unhappy when the market drives the figure down to \$4. □

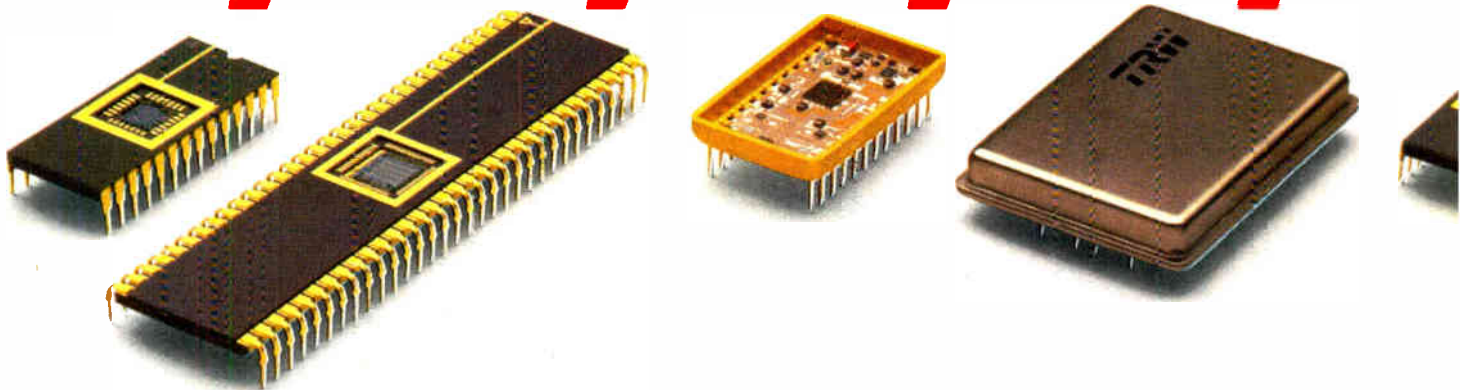
## READY OR NOT, HERE COMES THE ELECTRONIC STILL CAMERA

**W**ill the electronic still camera be the next consumer craze? Two Japanese companies think so, and are rushing cameras to Japanese markets. Fuji Film Co. started sales this month of a \$1,300 model; for an additional \$1,500, the picture buff can get an audio-still video player that not only plays back pictures, but can handle 9.6 seconds of music or voice to be recorded on tracks left blank while taking pictures. Camera maker Canon Inc. is going after the moderately priced segment with a \$750 compact camera weighing 1 lb 9 oz that it expects to start selling Dec. 1. □

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			Channels	Resolution (bits)	Throughput (kHz)	Channels	Resolution (bits)	Throughput (kHz)	
LOW COST	DT2811-PGH	Low Cost A/D, D/A, Interrupt	16SE/8DI	12	20	2	12	50	8 In, 8 Out
	DT2811-PGL	Low Cost, Low-Level A/D, D/A; Interrupt	16SE/8DI	12	20	2	12	50	8 In, 8 Out
	DT2814	Low Cost A/D, Int.	16SE	12	25	—	—	—	—
	DT2815	Low Cost D/A	—	—	—	8	12	3.3	32
GENERAL PURPOSE	DT2817	Low Cost DIO	—	—	—	—	—	—	16
	DT2808	Low Cost, DMA	16SE	10	3.3	2	8	10	16
	DT2801	General Purpose, DMA	16SE/8DI	12	13.7	2	12	14.8	16
	DT2801-A	Higher Throughput, DMA	16SE/8DI	12	27.5	2	12	29.5	16
	DT2801/5716A	High Resolution, DMA	8DI	16	20	2	12	14.8	16
	DT2805	Low Level, DMA	8DI	12	13.7	2	12	14.8	16
	DT2805/5716A	Low Level, DMA	8DI	16	20	2	12	14.8	16
	DT2805/5716A	Low Level, DMA	8DI	16	20	2	12	29.5	16
	DT2818	Simultaneous Sample & Hold, DMA	4SE, SS&H	12	27.5	2	12	29.5	16
	HIGH SPEED	DT2824-PGH	High Throughput, Low Cost A/D; DMA, Ints.	16SE/8DI	12	50	—	—	—
DT2824-PGL		Low Level, Low Cost, High Throughput A/D	16SE/8DI	12	50	—	—	—	16
DT2821		High Throughput, DMA, Interrupts	16SE/8DI	12	40	2, De-glitched	12	130	16
DT2821-F-16SE, DT2821-F-8DI		Very High Throughput, DMA, Interrupts	16SE or 8DI	12	150	2, De-glitched	12	130	16
DT2821-G-16SE, DT2821-G-8DI		Ultra High Throughput, DMA, Interrupts	16SE or 8DI	12	250	2, De-glitched	12	130	16
DT2823		High Throughput, High Res., DMA, Ints.	4DI	16	100	2, De-glitched	16	100	16
DT2825		High Throughput, Low Level, DMA, Ints.	16SE/8DI	12	40	2, De-glitched	12	130	16
DT2827		High Resolution, High Throughput, DMA, Int.	4DI	16	100	2, De-glitched	12	130	16
DT2828		High Throughput, SS&H, DMA, Interrupts	4SE, SS&H	12	100	2, De-glitched	12	130	16
DT-Connect™		DT2841	High Throughput, DT-Connect™ Transfer	16SE/8DI	12	40	2, De-glitched	12	130
	DT2841-F-16SE, DT2841-F-8DI	150kHz Throughput, DT-Connect™ Transfer	16SE or 8DI	12	150	2, De-glitched	12	130	16
	DT2841-G-16SE, DT2841-G-8DI	250kHz Throughput, DT-Connect™ Transfer	16SE or 8DI	12	250	2, De-glitched	12	130	16
	DT2841-L	750kHz Throughput, DT-Connect™ Transfer	4DI	12	750	2, De-glitched	12	130	16
	DT2847	16-bit Resolution, DT-Connect™ Transfer	4DI	16	100	2, De-glitched	12	130	16
FLEXIBLE I/O	DT2848	High Throughput, SS&H, DT-Connect™ Transfer	4SE	12	100	2, De-glitched	12	130	5
	DT2806	iSBX A/D	Up to 80	12	20	Up to 24	12	—	Up to 72

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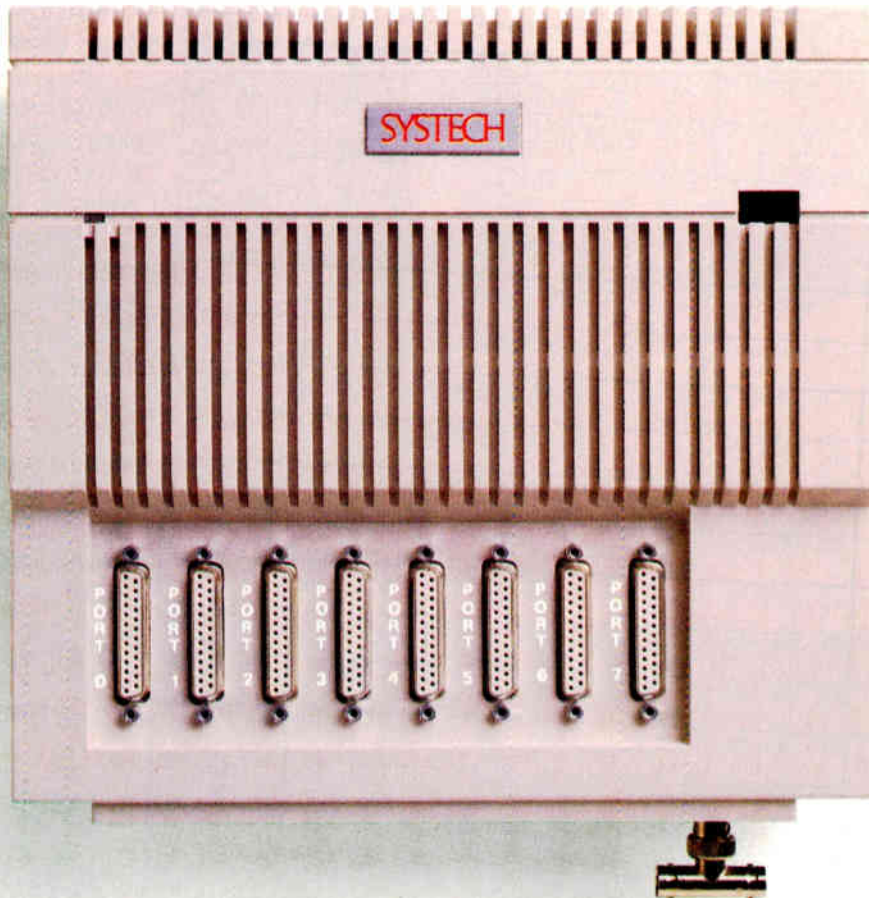


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# PRODUCTS TO WATCH

## INTEL MAKES IT EASIER TO BUILD MULTIBUS II SYSTEMS

Intel Corp. has released a fully documented open architecture for Multibus II systems products—software, protocols, and procedures that greatly simplify the task of mixing modules based on different microprocessors in original-equipment-manufacturer systems. The system architecture includes transport and message-passing protocols, multiprocessor system boot and configuration procedures, and diagnostics—all as a systems extension of the Multibus II IEEE/ANSI 1296 standard. With it, OEMs can build microcomputer-based products on par with or superior to traditional minicomputers, says Intel's OEM Modular Systems Group in Hillsboro, Ore. But Intel also unveiled a slew of products for systems based on the Multibus I, including the iSBC 386/12 series of 80386-based 32-bit CPU boards that double the performance of 80286-based systems by simply plugging in new hardware. □

## TI MIXES EPROM AND EEPROM TO MAKE A MORE VERSATILE MICROCONTROLLER

Texas Instruments Inc. has greatly expanded microcontroller versatility by integrating 16 Kbytes of ultraviolet erasable programmable read-only memory and 512 bytes of electrically erasable PROM on its new TMS370C756 8-bit microcontroller. In a typical application, the larger EPROM space would hold most of the program code. The EEPROM then could be used in a factory to select software routines stored in EPROM for specific equipment configurations, to calibrate systems in the field, or hold downloaded software that tailors product features for users. Sample kits cost \$100, say TI managers in Houston. The 370C756 makes TI the first to market a microcontroller with both EPROM and EEPROM. Archival Motorola Inc. is planning to mix the two memory technologies in a future member of its MC68HC11 family, which—like TI's 370 line—was originally developed for General Motors Corp. □

## AT \$2.60 PER MEGABYTE, IMPRIMIS' 766-MBYTE WINCHESTER COULD START A PRICE WAR

Price competition at the high end of the 5.25-in. Winchester market is likely to ignite with the introduction of the 766-Mbyte Wren VI drive from Imprimis Technology Corp. in Minneapolis. The Wren VI's capacity matches that of the 760-Mbyte XT8760 from Maxtor Corp., San Jose, Calif., but at a price of \$1,995 in 5,000-unit quantities. That pushes the price per megabyte down to \$2.60, well below the \$3 to \$5 per megabyte that Maxtor quotes on its two-year-old XT8760. Wren VI production units will be available around yearend. More competitors and price dueling is in the offing. Micropolis Corp., Chatsworth, Calif., and Siemens Information Systems Inc.'s Memory Products Division, Newbury Park, Calif., say they also plan the first shipments of 760-Mbyte drives before 1989, and other vendors also expect to move up from current-generation 380-Mbyte 5.25-in. drives next year. Imprimis is Control Data Corp.'s newly-named disk drive subsidiary (see p. 175). □

## BENCHMARK'S ACCELERATOR UPGRADES TO 200 MFLOPS IN 50-MFLOPS STEPS

A multiple-processor floating-point accelerator from Benchmark Technologies Ltd., lets VMEbus original-equipment manufacturers add up to 200 megaflops of computing power in increments of 50 million floating-point operations/s. Optimized for graphics and signal-processing applications, the accelerator, called the Blitz, uses from one to four floating-point chip sets from Bipolar Integrated Technology Inc. of Beaverton, Ore. The Blitz architecture consists of three processor sections: one to handle data transfers, one to perform control functions, and one to execute the math. Benchmark Technologies, a subsidiary of DuPont Inc., Wilmington, Del., sells the basic 50-megaflops board for \$20,000. Additional math units cost \$12,000 to \$15,000. □

# PRODUCTS TO WATCH

## BROOKTREE'S ANALOG-TO-DIGITAL CONVERTER WILL BE THE CORE OF VIDEO CHIPS

**A**n 8-bit, 20-million-sample-per-second, analog-to-digital video converter from Brooktree Corp., is tailored for video hardware, particularly high-performance work stations, where its \$19 unit price will make it competitive. Just as important, Bt208 circuitry will become the core conversion device in San Diego-based Brooktree's single-chip solutions for image-acquisition functions that now require many components. The image-acquisition chips will be available in a few months. By using the Bt208 core, system houses can eliminate external circuitry required for video applications—including video amplifiers, dc restoration circuits, and references. Features such as clamping circuitry for periodically restoring the signal are now on-chip. The architecture lines up 256 comparators in parallel to digitize the video input signal. □

## GaAs ARRAYS FROM TRIQUINT RUN AT 1 GHz AND HIT THE 4,200-GATE LEVEL

**T**riquant Semiconductor Inc. is upping the ante in the gallium-arsenide gate-array business by introducing a new family of devices that support speeds of up to 1 GHz and densities up to 4,200 equivalent gates. The Beaverton, Ore., company's three devices are the 4,200-gate TQ3420, the 3,000-gate TQ3300, and the 2,000-gate TQ3200, which support 40, 64, or 84 dedicated input/output pins, respectively. They can be programmed for either TTL, CMOS, or ECL compatibility, yet consume 50% less power than comparable arrays on the market. The arrays are fabricated using the company's 1- $\mu$ m Q-ED process, an enhancement/depletion-mode GaAs metal-semiconductor FET process featuring two layers of metal interconnect and a proprietary air-bridge technology. Available with a turnaround time of 8 to 10 weeks, nonrecurring engineering costs range from approximately \$45,000 to \$60,000. □

## DISPLAY CHIPS FOR PORTABLE PCs SUPPORT MULTIPLE STANDARDS AND TECHNOLOGIES

**T**he portable- and laptop-computer market is getting the advanced chips it needs to handle advanced display technology. The VG600 from Vadem Corp., San Jose, Calif., provides the interface to support a liquid crystal display of either 640-by-200- or 640-by-400-pixel resolution in any of a number of formats, including CGA, double-scan CGA, Monochrome Display Adapter, or AT&T's graphics adapter and can simulate color output in an eight-level grey scale. It is priced at \$20 each in 1,000-unit sample quantities. Even more impressive is the 82C455 flat-panel controller from Chips and Technologies Inc., San Jose, Calif., priced at \$52.80 each in volume. It supports CRT, LCD, or plasma displays of up to 720 by 480 pixels and is compatible with the EGA, CGA, Hercules, and MDA graphics standards. □

## TEK'S WORK STATION OFFERS HIGH-END GRAPHICS AND DIRECT NETWORK LINK

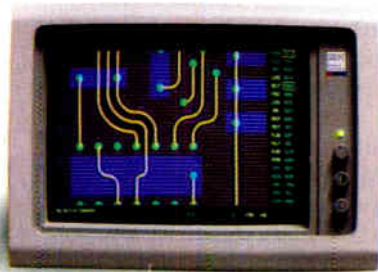
What do you call a graphics terminal too powerful to be called a terminal? You can call it a Graphics Netstation, at least that's what they're doing at Tektronix Inc., Beaverton, Ore. The pioneer in computer graphics technology was set to introduce its latest graphics terminal, the model 4311, a dual-processor (Intel 386SX and TI TMS 34010) powerhouse with direct support for local network connections and the X Windows user-interface standard. But during meetings with customers and industry observers prior to the introduction it became obvious that the 4211 is more than a terminal. It is a new class of product—a merged work station, diskless network node, and terminal. The base-configuration Tektronix 4211 Graphics Netstation includes a 15-in., 1,024-by-768-pixel, 16-color display; three RS-232-C ports; a Centronics port; VT200-style keyboard; and 750 Kbytes of memory. It is priced at \$6,495 and will be available in November. □

# The P-CAD Software That Made This Famous Laptop Computer Is Now Made To Fit Your Budget.

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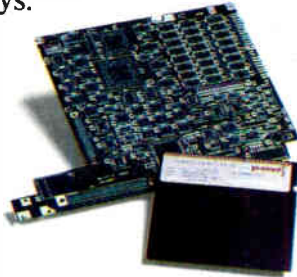
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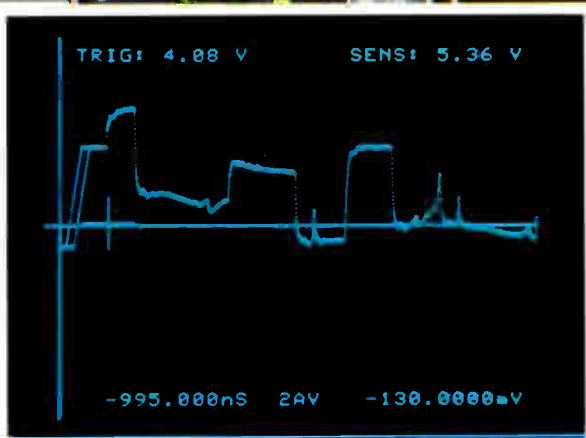
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INSTRUMENTS OF DISCOVERY

# Electronics

## HERE COMES THE FIRST 2.5-IN. WINCHESTER DRIVE

Light, low-power unit could open the way to notebook-size laptops

### SAN JOSE, CALIF.

The fast and small high-capacity Winchester disk drive that the laptop computer market has been waiting for is finally here. Its arrival opens the way to a notebook-size laptop that packs the power of a desktop model, and may also touch off a marketing war among drive makers.

There have been book-size machines before, but their limited memory and disk capacity and undersized screens kept them from chalking up mass sales. But screens have improved markedly, and now the first ever 2.5-in. Winchester disk drive, from two-year-old PrairieTek Corp. of Longmont, Colo., brings within reach the tantalizing goal of one with capabilities that will make it attractive to the general business user. The drive occupies only 12 in.<sup>3</sup>—70% less than a 3.5-in. Winchester, says Steve Volk, an investor and vice president of marketing at PrairieTek. It holds 20 Mbytes on two disks with 28-ms average access time. Moreover, it never uses more than 1.8 W of power. A typical 3.5-in. disk drive consumes up to 8 W during startup and around 2 W while in operation.

The industry will not leave the field to PrairieTek, however, as other drive makers are believed to be working on their own 2.5-in. Winchesters. And there is also a new 3.5-in. model that its maker, Areal Technology Inc. of Santa Clara, Calif., says is less power-hungry and faster than others its size. Like PrairieTek's, Areal's drive breaks new technology ground. It uses a single glass disk, a unique head and spindle motor design, and a plastic frame instead of a metal one to keep down cost, weight, and size. Yet, it will offer higher capacity—100 Mbytes—on its one 3.5-in. glass disk and an average access time of under 30 ms.

But the 2.5-in. form factor will probably catch the eye of computer makers trying to downsize their laptops. One industry analyst who had an early peek at the new PrairieTek drive, Philip Devin of Dataquest Corp. in San Jose, Calif., agrees that it will finally provide the technology needed to realize the notebook computer.

And it appears to have arrived at the right time, with the laptop market poised to chalk up some big gains. Even though sales this year will amount to just 682,900 units, that will represent an increase of nearly 70% over 1987, according to Dataquest. For next year, growth is forecast at just over 40% to 1 million units. For 1990, a 30% hike to 1.3 million is projected, and for

minimum needed to hold a hub large enough to have a spindle motor inside.

But at Conner Peripherals, a leading supplier of 3.5-in. disks for laptops, the official word is skepticism. Finis Conner, the San Jose, Calif., company's founder, chairman, and chief executive officer, says he is unimpressed by the smaller drive. "I don't think it is clear that the 2.5-in. form factor

is the right size for the laptop portable," he says, adding that the smaller size may actually increase the unit's cost. That view is borne out in the case of the PrairieTek drive, which uses two disks and four heads. That could keep its price higher than single 3.5-in. disks with two heads.

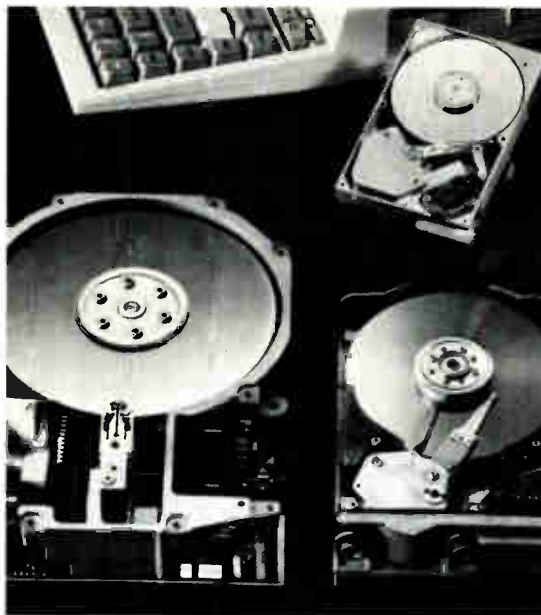
**TOUGH ENOUGH.** Despite that, the PrairieTek drive has at least one big advantage over competing 3.5-in. models, says Dan H. Wilkie, president of DynaBook Technologies Inc. in Westlake Village, Calif. That advantage is its ruggedized design—an important feature in a machine designed to be carried around. Wilkie's company was formed in May 1987 to build laptop computers.

Unlike most Winchesters, the PrairieTek drive uses ramp-loaded heads. As a result the heads never touch the disk surface during operation. Rather, the drive's actuator retracts the read/write heads up a ramp off the disk surface when power is removed from the disk drive and extends the heads

to the disk surface as power is applied. Because the heads are off the disk surface when power is off, heads and disk do not slap together if the drive is shocked, nor is the disk subject to stiction.

The hunt for a full-featured computer that fits into an attaché case goes back at least 10 years. The closest anyone has come was Alan Kay, who built a model of one at the Xerox Palo Alto (Calif.) Research Center and called it Dynabook—Kay has no links to the company of the same name. Coming closest to realizing Kay's vision commercially is the master of miniaturization, Sony Corp., in a product called Produce. The computer is a dedicated Kanji word processor that the company has given to its executives worldwide.

—Jonah McLeod



The Winchester family's baby is PrairieTek's 2.5-in. disk drive, upper right; it may change the laptop market.

1991, a 25% jump to 1.6 million.

Attempts to carve out a chunk of disk sales in that market is creating fierce competition. In addition to Ariel with its 3.5-in. product, there is growing interest in offering a 2.5-in. version, says one industry watcher. James Porter, president of Disk/Trend Inc., a disk drive market research firm in Mountain View, Calif., says he believes that Conner Peripherals, IBM, and Miniscribe are all working on them.

Adding credence to Porter's view is the fact that all three have expressed interest in a 2.5-in. disk that Domain Technology Inc. of Milpitas, Calif., has developed for PrairieTek's drive, says David Pierce, Domain's chief executive officer. The Domain disk has an outside diameter of 65 mm and an inside diameter of 20 mm, the

# JAPAN'S BIG SPLASH IN GRAPHICS STATIONS

**TOKYO**

No longer is the graphics superworkstation club exclusively made up of U. S. companies. The Japanese are joining up—and they're starting off with a bang. Their new machine will rank near the top of the category, powerful workstations that are adept at performing interactive three-dimensional graphics.

In the culmination of a national project, Oki Electric Industry Co. will build a prototype system with a target completion date of June 1989. No one is saying when a commercial version will appear, but U. S. competitors aren't waiting to find out: they're pushing out to market several new models, including one from Silicon Graphics Inc. that will outperform all graphics superworkstations that have been delivered so far.

But the impressive Japanese hypercube design immediately places it among the top performers. In a hypercube design, multiple processors are linked in multidimensional-cube arrangements with direct connections between neighboring nodes. An n-dimensional cube has 2<sup>n</sup> nodes. Oki's 16-processor machine is capable of 8 million floating-point operations/s and a peak throughput that tops 100 megaflops.

Even though the development project is backed by the Japanese government, Oki is going to a U. S. manufacturer for its reduced-instruction-set chips: the processors will consist of three Weitek Corp.

chips mounted on a single board.

Each board also includes 8 Mbytes of data memory and provides either 8 megaflops or 8 million instructions/s of processing power. The display will have a resolution of 2,000 by 2,000 pixels.

The 16 boards are connected into a 2<sup>4</sup> hypercube with each processor connected to four others through gallium arsenide input/output ports and coaxial cable. The I/O ports also provide parallel-to-serial conversion. Serial transfer rates exceed

The Japanese effort will turn to Weitek Corp. for RISC chips

100 Mbits/s, enabling the system to process data at better than 100 megaflops, even though each individual processor can do only 8 megaflops. Each processor is also connected to the host by a 32-bit bus. The hypercube performs the object transformation and clipping needed for graphics displays. It can also be used for other types of graphics processing, such as ray tracing, or for scientific and technical computing.

As the Japanese fine-tune their machine, the emphasis back in the U. S. is on getting designs to market. Silicon Graphics, one of the pioneers and the leader in the relatively new field, is introducing

two significant systems this month. The Mountain View, Calif., 3-d graphics company is bringing out a top-of-the-line machine, the 4D/240 GTX, which begins at \$60,000. The other system, called the Personal Iris workstation, scores at the other end of the price spectrum. It opens a new entry point in Silicon Graphics' family of compatible 3-d workstations. The system brings the price of a high-performance graphics workstation below \$20,000 for the first time—configurations of the Personal Iris range from \$16,000 to \$35,000.

As one of Silicon Graphics' biggest original-equipment-manufacturer partners, Control Data Corp. will also be offering the Personal Iris workstation as its Cyber 910-400 series.

Two other new graphics products joined this growing category of computer systems at the Siggraph show in Atlanta in early August. The Animation Super Workstation from Hewlett-Packard Co. is a fast version of the Palo Alto, Calif., company's Model 835 Turbo SRX station optimized for animation performance.

And the VFX/82 Visualization Supercomputer, introduced at the show by Alliant Computer Systems Inc., Littleton, Mass., although a stand-alone workstation, provides the same capabilities in a configuration of a supercomputer host with graphics terminals. The VFX/82 is the top product in the company's line of Alliant Visualization Supercomputer products.

—Charles L. Cohen and Tom Manuel

## THE 10-MIPS SUPERGRAPHIC FAMILY GROWS

	Alliant	Apollo	Ardent	Hewlett-Packard	Oki	Silicon Graphics	Stellar	Sun
<b>Product</b>	VFX/82 Visualization Super-computer	Series 10,000	Titan	Animation Super Work-station	Prototype Hypercube	4D/240 GTX	GS 1000	SUN-4/260 CXP
<b>Processor(s)</b>	16 proprietary computation elements plus 16 graphics processors	Four 64-bit proprietary RISC processors	16-MHz MIPS RISC and Weitek Floating Point Units	Proprietary RISC HP Precision Architecture	16 Weitek RISC processors	Four 25-MHz MIPS R3000 processors	Multiple proprietary processors	Sparc 16-MHz RISC
<b>Mips</b>	na	72	64	14	100	80	25	10
<b>Megaflops (peak)</b>	377/processor	140	64	2	100	50	64	1.6
<b>Max. memory (Mbytes)</b>	512	128	128	208	128	128	128	128
<b>Max. resolution</b>	1,280 by 1,024	1,280 by 1,024*	1,280 by 1,024	1,280 by 1,024	2,000 by 2,000	1,280 by 1,024	1,280 by 1,024	1,152 by 900
<b>Max. bit planes</b>	24	80*	48	24	48	64	32	8
<b>3-d vectors/s</b>	1,000,000	1,000,000*	600,000	50,000	1,200,000	400,000	500,000	150,000
<b>Base price</b>	\$125,000/user	\$69,900	\$150,000	\$67,600	na	\$90,000	\$104,900	\$59,000

\*Estimated performance of future graphics subsystem

SOURCES: VENDORS AND PUBLISHED LITERATURE

# OCTOBER COULD REVEAL WHERE CHIP INDUSTRY IS GOING

**LOS ANGELES**

The suspense is about to end—maybe. For the semiconductor industry, October is the month when people expect answers about the chip business—will it slump? Hold steady? Soar some more? But even if October's figures spell out the industry's fortunes for the fourth quarter, there is still much uncertainty about how it will fare next year, several influential industry watchers are saying.

Experience has taught them that in October orders customarily recover from the usual summer dip, which was evidenced by the book-to-bill ratio's slide this August, for example. But no seer would be caught without a caveat. In this case, it's the fact that the current cycle is relatively old. The strong upward course of nearly two years is nearing the point in the cycle where troubles sprang up in the past. In late 1984, the collapse of personal computer sales made bookings dive 50% within months.

So analysts are waiting to see what the last quarter brings. And what they are watching more closely than anything else is the situation in shortage-plagued dynamic random-access memories. There is some worry that the race to catch up with demand could become a problem with oversupply as manufacturers accelerate production of the new 4-Mbit chips (see table).

Despite all the volatility that has marked the chip business since the orders peak of \$1.3 billion in June, predictions for at least a 30% rise for this year—and considerably less growth for 1989—are holding steady for the most part. Jack Beedle, the market analyst of In-Stat Inc., Scottsdale, Ariz., and Dataquest Inc. of San Jose, Calif., are both projecting a 33% jump in 1988.

**NEW NUMBERS.** But this year, for statistical-forecast purposes, is just about history. That leaves the analysts waiting anxiously to see what the publishers of the World Semiconductor Trade Statistics predict for next year. The Semiconductor Industry Association, which compiles WSTS from the confidential figures of its members, predicted in April that 1988 would see a 30.1% increase over 1987 and that 1989 would be up just 3.9% over 1988.

The 1989 prediction is likely to be updated with figures from September's an-

nual forecasting session, and one observer who closely tracks the WSTS statistical base says he expects little change from the 3.9% forecast. Beedle, a forecaster with a bearish bent whose projections often are the first to signal a dip, also expects single-digit U. S. growth next year. Dataquest, however, is on record with its prediction of a 12.5% increase.

More important than variations of a few percentage points in the chip outlook are factors working to forestall a repeat of the debacle of 1984-85, say some observers. The most important is the continued tight supply of dynamic random-access memories, a shortage that experts figured would end months ago.

The short supply has led to a scenario in which users have had to put off buying parts that would go with the DRAMs in new equipment, thus pushing overall demand into the future. "Thanks to the DRAM shortage, inventories have not built up as in past cycles," says Charles M. Clough, president of Wyle Laboratories Inc., a major distributor in the western U. S. "DRAMs are in shorter supply now than two months ago," says Clough. He expects the flow to accelerate late in the year, acting as a strong driver for the U. S. semiconductor business for the first half of 1989.

Clough's view of component inventories, one he concedes is in the minority, is that their buildup "is the prime cause of any decline, followed by pricing and demand factors." Most others put demand at the top. And, like other market watchers, Clough sees higher orders from a resurgent computer industry continuing well into next year.

**DRAM OUTLOOK.** Further confirmation that DRAMs could smooth the usual ups and downs of the chip cycle can be found in industry reports that worldwide manufacturers of these memories have stopped

booking orders until year end. And denying reports circulating that it is having yield troubles that are delaying its 1-Mbit chips, Motorola Inc., a prospective big producer in Mesa, Ariz., says it expects to deliver one million parts by year end. Both Texas Instrument Inc. and Toshiba Inc. say they have been allocating chips. 1988 is sold out, and 1989 looks tight also.

If it is true that orders have been cut off, the chip makers would not only be helping their own production schedules next year by delaying sales, but would be giving a boost down the line to the whole industry, observers say.

Also paying close attention to the fourth quarter's performance are Wall Street traders. Chip makers' stock prices have been taking a beating again, sinking to levels nearly as low as those following Black Monday last year. The reason is that the stock market is supposed to forecast the future and by looking at present prices it's easy to conclude that the industry is in "a classic down cycle," points out analyst Thomas Kurlak of Merrill Lynch Corp.

-Larry Waller

## WHO'S MAKING 1-MBIT DRAMs

(MILLIONS OF UNITS)

	4th quarter	Year
Toshiba .....	21.0	56.0
NEC .....	11.4	28.5
Mitsubishi .....	10.8	25.5
Hitachi .....	7.5	20.0
Fujitsu .....	7.5	15.8
TI .....	5.5	10.9
Motomshito .....	5.0	9.9
Samsung .....	3.0	5.5
Okii .....	2.5	5.4
Micron .....	1.3	2.5
NMB .....	1.6	2.5
Siemens .....	1.5	3.5
Motorola .....	0.5	1.0
Sharp .....	0.4	1.0
Hyundai .....	0.3	1.0
Vitellic .....	0.3	0.7
Alliance .....	0.2	0.5
<b>Total</b>	<b>80.3</b>	<b>190.2</b>

SOURCE: IN-STAT INC.

But the industry still must get through the fourth quarter. "The caution flags are flying," says Beedle, adding that chip manufacturers "by and large are not yet crying the blues." The weakest spot is in disk drives, where oversupply and price-cutting have caused havoc. Also potentially worrisome is the personal computer market, where there are reports of slowing sales of machines to end users.

So Beedle is holding to his spring prediction of only a slight improvement in October over summer levels, with orders showing declines for the entire fourth quarter [*Electronics*, May 12, 1988, p. 31]. The number to watch: orders must top \$1 billion for October to ensure continuing healthy growth, he says.

Although he agrees with Beedle that prospects for the semiconductor industry are at a crossroads, Adam F. Cuhney of New York's Kidder Peabody & Co. is taking a more optimistic view. Says the San Francisco-based financial analyst, "Our view is that the semiconductor recovery will continue into 1989 and that bookings will begin a normal rebound."

# HOW WILL IBM DEAL WITH THE EISA THREAT?

## NEW YORK

Things have not worked out well for IBM as it turned its back on the input/output-bus standard it set for the Personal Computer AT and launched the new incompatible 32-bit Micro Channel. PC users—and consequently, PC and PC-peripheral makers—are just not ready to leave the 16-bit AT bus behind. And last month, the PC industry did something about it, introducing an AT-compatible 32-bit bus developed by a loose consortium of manufacturers. The 32-bit Extended Industry Standard Architecture is a serious threat to IBM's ability to make the Micro Channel the leading standard.

Users have too much invested in AT add-in cards and peripherals, and they're making their point with purchases: well over half the PC market is in AT-compatible machines. Even IBM has tacitly admitted its mistake, and last month it introduced a new member of its PS/2 line that has an AT-compatible bus instead of a Micro Channel: the PS/2 model 30 286.

**NEXT MOVE.** What will IBM's next move be? One possibility is that the company could drastically lower or eliminate the licensing fees it charges to makers of Micro Channel hardware, to make that bus more attractive as a standard. That would be a major about-face for IBM, which has surrounded its Micro Channel patents with a cloud of fear, uncertainty, and doubt from day one, and which now demands royalties of up to 5% in its license agreements.

Can the PC industry, which for two generations has let IBM set the bus standards, turn around and dictate terms that IBM must accept if it is to maintain a significant share of the PC market? No one can say as yet, but IBM will surely make a fight of it. The company's first blast is a marketing counterthrust that centers on the fact that 32-bit capability is here now in the form of Micro Channel PS/2 machines, and EISA-based PCs may not show up until late next year. But peripherals that require a 32-bit bus don't yet exist, and by the time they do, EISA machines will be on the market.

A large group of dog-eat-dog competitors is trying to teach IBM a lesson in the open-architecture philosophy in a remarkable act of cooperation. The EISA group represents a stark contrast to IBM's formal, close-to-the-vest, highly legalistic, proprietary approach.

Prodded by customers waving purchase orders, nine sponsors who build PCs and about 60 other PC-industry companies formed the alliance. The job of distributing the EISA specification has been turned over to an independent law firm—

Bishop, Cook, Purcell & Reynolds in Washington. A low fee of \$2,500 has been set for a copy of the specifications. System developers also have an option of sharing certain patents contributed by sponsors through licensing. Beyond this there is no formal organization.

The fact that the EISA specification was developed by the usually fiercely competitive PC vendors—all major players in the AT-compatible market—re-

## PC users are voting for AT-bus compatibility; will IBM fall into step?

mains cause for wonder. "I am still shaking my head over the level of cooperation between the companies and how well it went," says Alan Kraemer, vice president for system engineering at one of the nine, AST Research Inc. The eight others are Compaq, Epson, Hewlett-Packard, NEC, Olivetti, Tandy, Wyse Technology, and Zenith Data Systems.

As the bus specifications were set, "no one dominated," says Kraemer. The mechanics of the drafting session were that "Compaq set up a straw man and the rest of us tried to knock it down," he says.

"All nine sponsors had their say in establishing the EISA specification."

The biggest reasons for the cooperation, says Kraemer, who was closely involved in the technical sessions with the other sponsors, were "the vacuum left by IBM" and "such an overwhelming common interest people decided not to fight about it." The market has made a loud and clear statement that it wants AT bus machines now and wants its next machines (32-bit I/O versions) to remain backward-compatible with the 8-bit PC and 16-bit AT expansion slots.

One obvious indication of this dissatisfaction is in PC shipments. During the second quarter of 1988, the number of AT-bus-equipped units delivered by dealers were 60% of the total, reports Storeboard Inc., the Dallas market-research company that tracks PC dealer sales. Micro Channel machines represented only 21% of the shipments.

Statistics such as these and inputs directly from customers and dealers sent a strong message to PC vendors. Microsoft Corp., the operating system supplier, and Intel Corp., the source of the microprocessor architectures used in IBM-compatible PCs, were key agents in getting the EISA effort under way, because the system vendors are continually discussing issues with them. —Tom Manuel

## MICROPROCESSORS

# BATTLE LINES ARE DRAWN FOR RISC-BASED SYSTEMS

## SAN JOSE, CALIF.

When Digital Equipment Corp. hitched its wagon to a reduced-instruction-set-computer architecture from MIPS Computer Corp., it gave DEC's work-station competitors, especially Sun Microsystems, something to think about. What's more, it changed the odds of Sun's Sparc architecture dominating the RISC field, even with Texas Instruments Inc.'s decision in late September to put its chip-making muscle behind Sparc by becoming a second source to Cypress Semiconductor Corp.

So while the technical work-station crowd sorts out their RISC strategy, the chip makers are jockeying to get an edge too. The DEC endorsement vaults Sunnyvale, Calif.-based MIPS into the running with Sun and Motorola Corp.'s 88000 RISC chip. And it strengthens DEC as a work-station competitor, says Vicki Brown, senior analyst at International Data Corp., Framingham, Mass.

"DEC will finally have the integer performance to enable them to get beyond the 3- to 4-mips range, making them competitive with Sun and Apollo at the high end," Brown says. She does not expect to see products from DEC incorporating MIPS' chips until after the first of the year, at the earliest.

In its deal with MIPS, DEC receives the RISC chip design and compiler technology. DEC is a prime mover in the Open Software Foundation and MIPS is likely to join soon. "DEC will most likely integrate our compilers in their RISC effort, and we'll both converge on whatever Unix standard emerges from OSF, says Robert C. Miller, MIPS chairman and president.

DEC's move means that any work-station vendor looking at the high-performance computer marketplace must have a RISC offering, says Michael Slater, editor of the Microprocessor Report, a monthly newsletter in Palo Alto, Calif.

One DEC rival, Data General Corp. of



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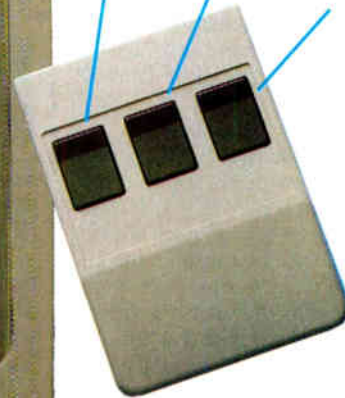
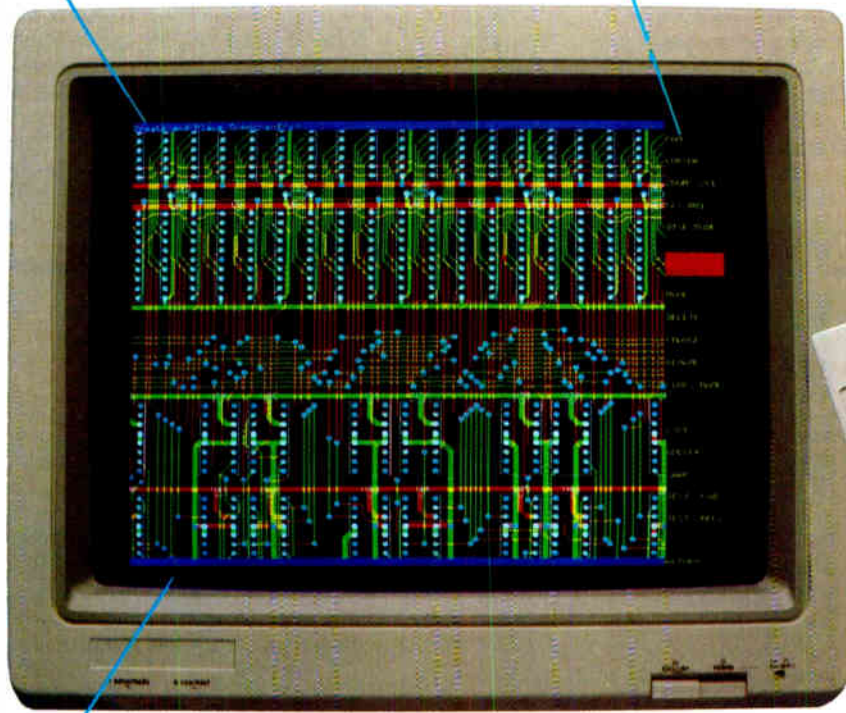
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Westboro, Mass., got a head start by adopting Motorola's 88000 for its future-generation computer system [*Electronics*, April 28, 1988, p. 32]. And Hewlett-Packard Co., Palo Alto, Calif., has developed its own RISC architecture as well.

The market for RISC chips in technical work stations is quickly becoming a prize worth competing for, says market researcher In-Stat Inc., Scottsdale, Ariz. In 1988-89, 34.2% of a projected \$1.7 billion in microprocessor sales will be in 32-bit chips. Of the \$500 million 32-bit microprocessor revenue, about 8%—\$40.1 million—will be RISC processors, In-Stat says. By 1992, \$1.3 billion—or 51.9%—of microprocessor revenue will be from 32-bit chips. RISC processor sales will amount to 26%, or \$342.9 million.

In the merchant-market RISC-chip battle, Sun executives in Mountain View, Calif., are quick to point out that because RISC applications go beyond work stations its agreements with semiconductor and software houses still give Sparc the overall edge. One advantage of Sun as the fray intensifies is that Sparc-compatible systems and applications software, as well as the development system needed for software, are available now, says Bernie LaCroute, executive vice president. Of the 1,500 packages that run on Sun work stations, third-party vendors have converted more than 200 to Sparc. Once adapted, the software will run on all future versions of Sparc-based work stations.

**LOST TIME.** Although software developers will eagerly support MIPS-based DEC platforms, because of the existing DEC software base, that will take time. In fact, DEC may have lost valuable time when it tried to develop its own RISC chip before abandoning the effort in favor of seeking a third party's technology.

Of the three major RISC contenders, Motorola, which is pushing its 88000 architecture through an open-systems strategy with the 88open Consortium, has the least available amount of software. Nonetheless, there are a number of software companies creating compilers for the 88000, says Robert Anundson, executive director of the 88open Consortium Ltd., Stratham, N.H. He says they include Green Hills Software Inc., Glendale, Calif.; Language Processors Inc., Framingham, Mass.; and others. Moreover, Unisoft Ltd., Berkeley, Calif., is developing a port of Unix System V for the 88000.

Other aspects of the RISC war are being hotly debated, however, such as Sun's strategy of allowing multiple semiconductor houses to fabricate their own incompatible versions of Sparc. Among the vendors are Bipolar Integrated Technology, Cypress, Fujitsu, LSI Logic, and TI.

MIPS' Miller sees this sourcing of incompatible chips as a problem for Sparc. "The difference between MIPS and Sparc is that

we own the design data base that we give to each of our chip partners so all the MIPS chip suppliers provide pin-compatible chips," Miller says. This means all the chips are software-compatible. "As a result we have a common applications programming interface between all MIPS customers," he says. The MIPS camp consists of Integrated Device Technology, LSI Logic, and Performance Semiconductor.

The 88000 has the same advantages as the MIPS implementation except that Mo-

torola will be the primary source of the CMOS version of the chip. Data General will produce an ECL version. Moreover, the 88open Consortium will ensure all software are has a consistent interface to the 88000.

None of Sun's chip suppliers offer the same chip architecture or have pin-compatible chips except TI and Cypress, says Miller. And the Fujitsu, LSI Logic, and Cypress chips are not interchangeable because they use different memory-addressing schemes. —Jonah McLeod

## TRADE RELATIONS

# WILL THE NEW TRADE ACT REALLY MAKE IT EASIER?

### NEW YORK

**T**he Trade Act of 1988 was supposed to simplify tariff regulations, work to improve U. S. competitiveness, and narrow the balance of trade. But its immediate effect is confusion, and for a while at least, the biggest beneficiaries may be lawyers, not U. S. manufacturers.

When the measure goes into effect Jan. 1, a new tariff schedule will be in place. Imports from Korea, Taiwan, and Hong Kong—many of which are now exempt from tariffs—will face full import duties and U. S. companies will have increased protection against dumping. In addition, controls on high-technology exports will be relaxed and the government will have the legal right to prevent foreigners from buying key U. S. companies.

Fueling the confusion, however, is the switch from the old Tariff Schedules of the U. S. to something called "harmonized code," a revised set of tariff definitions that is supposed to bring the U. S. more in line with its trading partners. Although the changes were designed to be revenue-neutral, they will significantly affect companies that import components, subassemblies, and finished equipment.

"Harmonized code could be likened to a Cecil B. deMille production—10 years in the making with a cast of thousands," says Harold Grunfeld, a partner at the New York law firm of Grunfeld, Desiderio, Lebowitz & Silverman, one of about a dozen U. S. law firms that specialize in trade and customs law. Ironically, tariffs on some consumer electronics items, such as clock radios with cassette players or combination compact disk/radios, will actually decline—from 4.7% to 3.9% of manufactured value. And that's not going help the trade deficit any.

These kinds of changes don't have much impact on OEMs, but that doesn't mean those companies escape unscathed.

For example, many OEMs depend heavily on components and subassemblies produced in Taiwan, Korea, and Hong Kong, and they will face a whole new tariff structure Jan. 1. Many items imported from these places are still exempted from tariffs by the Generalized System of Preferences—regulations that are designed to encourage growth in underprivileged economies.

As of the new year, however, OEMs will have to start paying duties of 3% to 7% or more on these goods, adding significantly to the cost of their products—enough, some are saying, to price products out of the market. The effect will be felt most stringently in Taiwan

and by manufacturers who source material from Taiwan. That's because 75% of all Taiwanese electronics imports to the U. S. are to OEMs, says Lisa Kjaer, executive director of government relations at the Electronic Industries Association.

**THE GOOD SIDE.** Kjaer concedes some OEMs will be hurt, but says the overall bill does more to strengthen U. S. industry than to hurt it. Take dumping: the new bill empowers the U. S. Trade Representative to accelerate investigations and to more severely punish repeat offenders. It also allows expansion of antidumping orders to include "screw-driver operations," says Bruce M. Mitchell, an attorney at Grunfeld, Desiderio. That means TV makers, for example, can't bring in nearly finished TVs to circumvent antidumping orders.

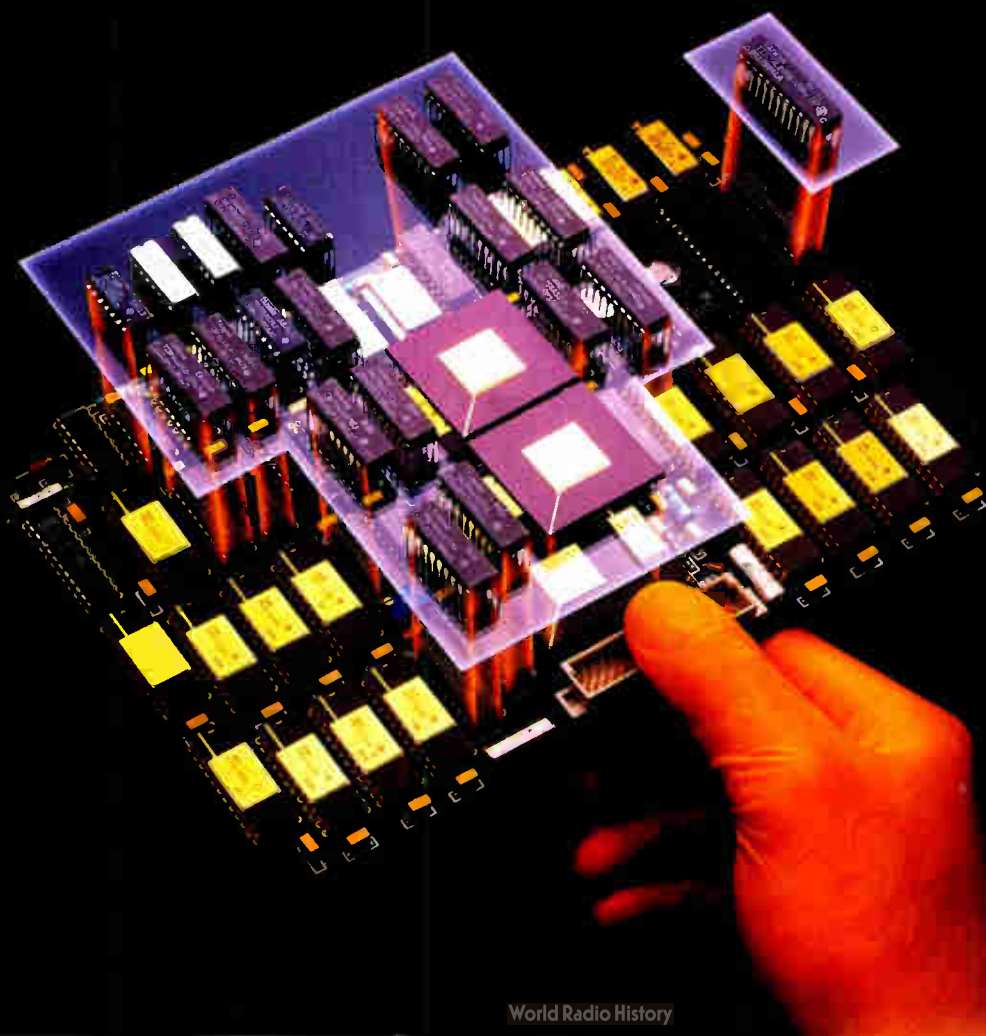
Finally, the bill includes a provision to protect the U. S. industrial base from foreign takeovers. U. S. companies doing business in areas deemed vital to national security will be protected from foreign raiders—whether hostile or friendly. The measure was inspired by Fujitsu Ltd.'s attempt to buy Fairchild Semiconductor Corp. two years ago; Fujitsu eventually withdrew its offer under U. S. government pressure. —Tobias Naegle

Fueling the confusion is the switch to a revised set of tariff definitions

TEXAS INSTRUMENTS REPORTS ON  
**SYSTEMS  
LOGIC**

IN THE ERA OF

**MegaChip** <sup>□</sup>  
TECHNOLOGIES



Systems logic in the Era of MegaChip Technologies:

# No system should ever be limited by its to help your design perform at its best.

Up to 65% of the components in today's systems are logic. Such a large proportion demands that your logic devices perform on a par with other advanced building blocks—and be chosen with equal care. Systems logic alternatives from Texas Instruments can help you better realize the performance potential of your system design.

**W**ithin months after demonstrating the first working integrated circuit 30 years ago, Texas Instruments introduced a commercially available logic function, an RS flip-flop. With that beginning, TI established a tradition of development and innovation in logic that encompasses the industry-standard SN54/74 Series TTL and the new families of advanced logic described here that can add significantly to the value and performance of your overall system.

For example, for systems that require off-the-shelf flexibility with a degree of customization, TI's Programmable Logic Devices (PLDs) include popular 10-ns PALiCs available in high volume. And, to keep pace with today's high-speed microprocessors, TI plans to continue to drive PLD performance to sub-10-ns speeds.

TI's Advanced CMOS Logic (ACL) supports the design goal of high perfor-

mance combined with low-power operation, while TI's new BiCMOS bus-interface family delivers very high drive current at very low power compared to bipolar circuits.

## TI's MegaChip Technologies

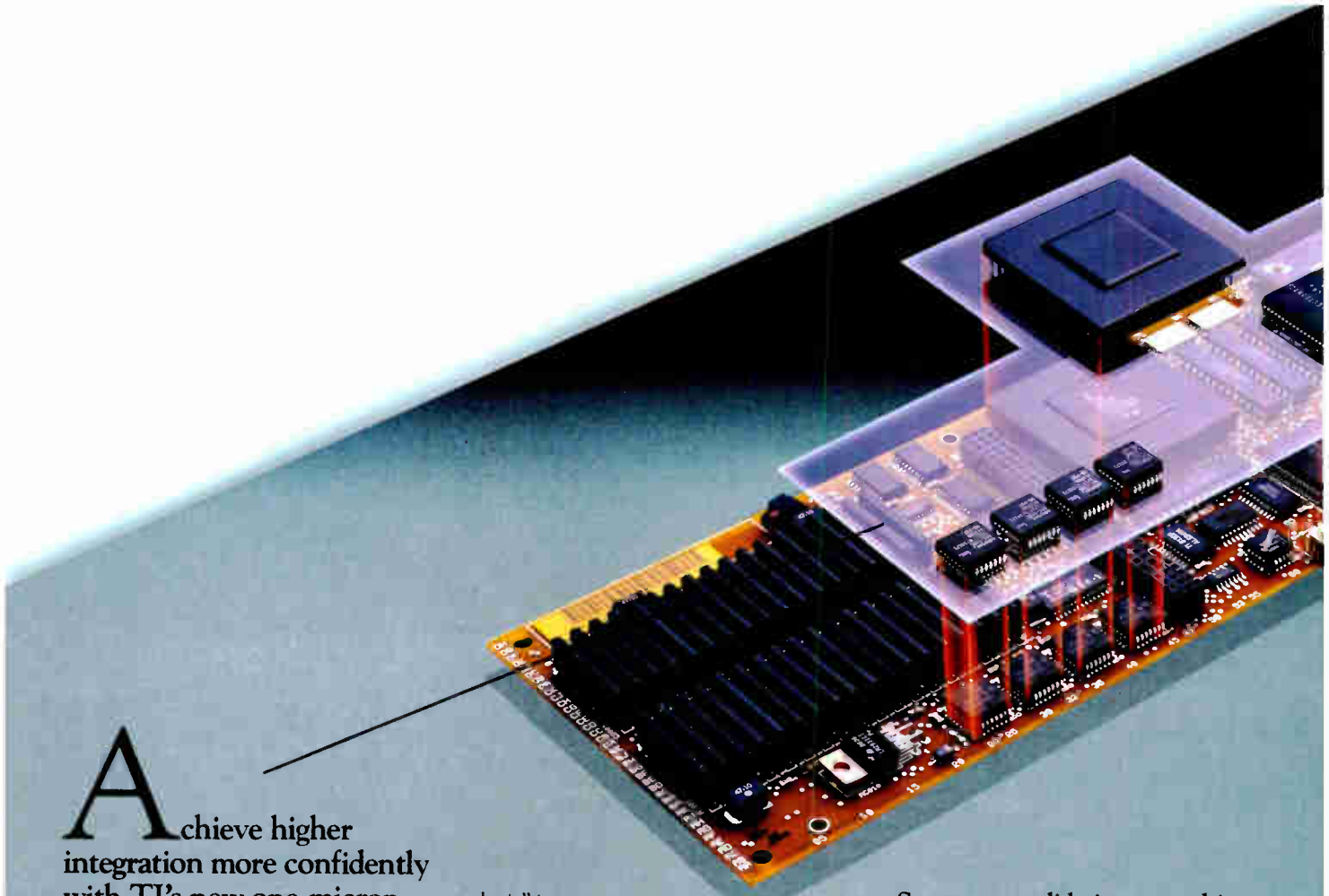
Our emphasis on high-density memories is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip™ Technologies, and they are the means by which we can help you and your company get to market faster with better products.

For systems requiring moderate densities and fast prototype cycle times, TI offers a new series of one-micron CMOS gate arrays. When you need higher levels of integration plus increased design flexibility, TI's one-micron CMOS standard cells provide the means for system consolidation.

And for military applications, TI offers a wide choice of high-reliability logic functions.

On the following pages are details of what you can expect from TI's range of logic options:

**ON THE COVER:** Suspended above the board, provided by Rockwell International, Missile Systems Division, are military versions of TI advanced logic devices.



**A**chieve higher integration more confidently with TI's new one-micron ASIC family.

Now, you can integrate more of your systems logic using TI's new one-micron CMOS ASIC (application-specific integrated circuit) family—the TGC100 Series gate arrays and the TSC500 Series standard cells. Each offers different degrees of design flexibility and system integration. The result is significantly reduced component count which cuts board size and system cost while improving reliability and performance.

And TI is supporting the family with comprehensive kits that help minimize design cost, risk, and time by providing a comfortable, easy-to-use design environment.

#### **Efficient logic consolidation**

Using TI's new TGC100 Series gate arrays, you can sweep major chunks of "glue

logic" into a single device while realizing fast design and prototype cycle times. Array densities currently range to more than 8K usable gates and 142 bond pads; the Series will be extended to more than 16K usable gates and 216 bond pads in a major production release planned for late 1988. Prototype delivery is typically two to three weeks from approval of postlayout simulation results.

The TGC100 Series Design Kit gives you complete autonomy and control over the design process. It is a comprehensive set of the tools required for successful gate-array design and validation (see last page for details).

Standard packages for the TGC100 Series range from 28-pin DIPs to 84-pin PLCCs, with optional packages up to 144 pins.

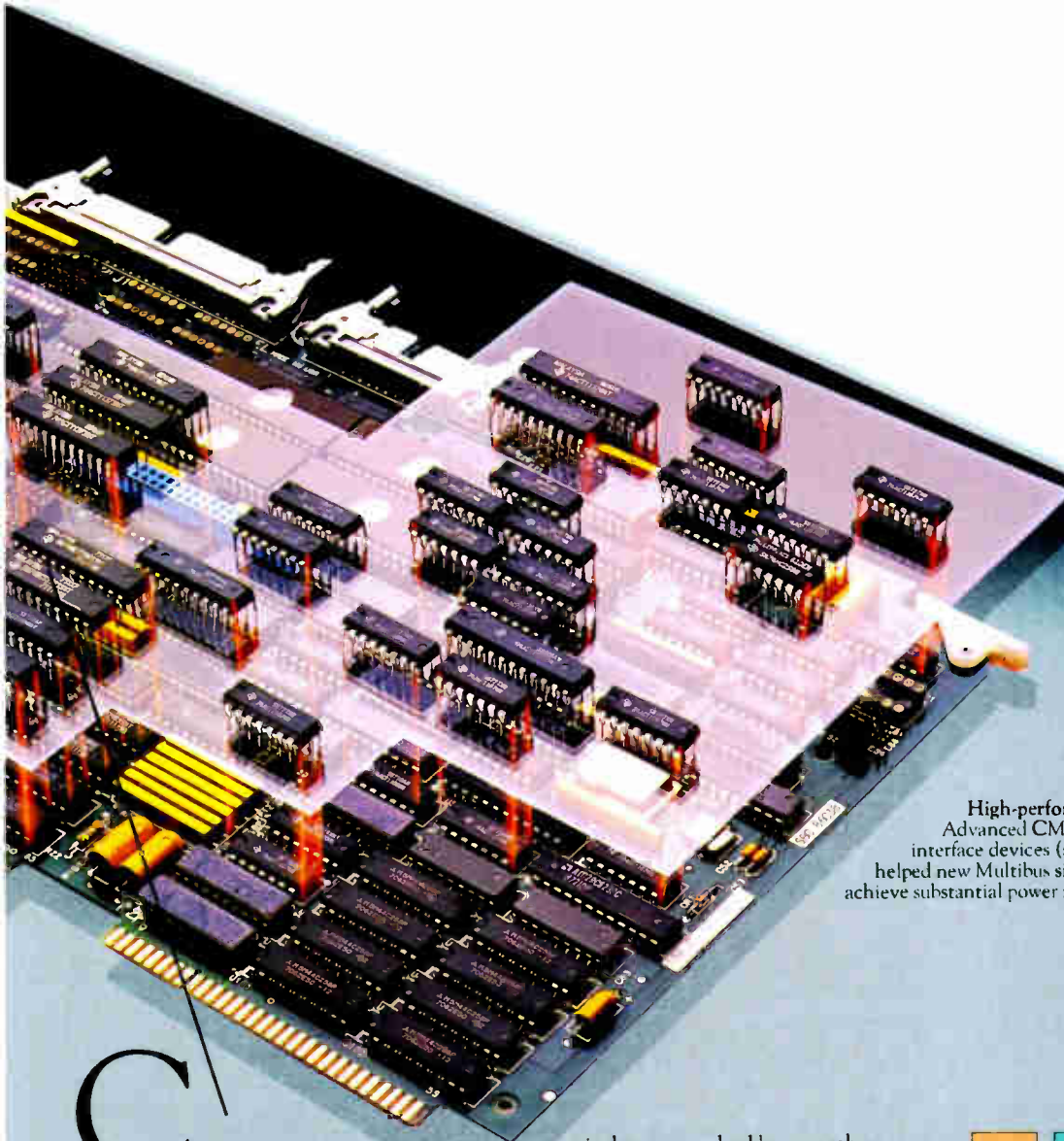
#### **System consolidation on a chip**

For applications requiring maximum design flexibility and higher levels of integration, TI has disclosed its third-generation standard-cell family, the TSC500 Series.

Complex system designs can be implemented using a growing core of basic SSI/MSI functions, as well as scan cells for testability and MegaModule™ building blocks such as register files, FIFOs, bit-slice family functions, RAM, and ROM are other aids to implementation. Output cells with drive capability up to 64 mA are available.

Package options include conventional through-hole DIPs, surface-mount PLCCs, and plastic quad flatpacks (QFPs) in both JEDEC and EIAJ standards, as well as high-pin-count plastic pin-grid arrays.

Both the TGC100 and TSC500 Series have a typical propagation gate delay of



High-performance, low-power EPIC Advanced CMOS Logic and BiCMOS bus-interface devices (suspended above the board) helped new Multibus single-board computer achieve substantial power reductions.

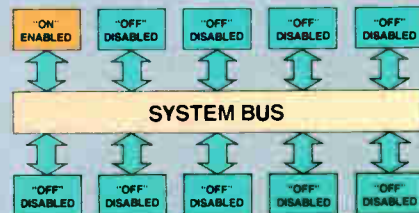
## Cut power, not speed or drive, with TI's BiCMOS bus-interface ICs.

This new family is a simple, effective means to reduce system power consumption without compromising advanced performance.

As the BiCMOS name implies, TI combines bipolar IMPACT and CMOS processing to achieve switching speeds comparable to advanced bipolar products and provide the 48/64-mA drive current needed for high-capacitive loads and backplanes. In particular, family members meet the drive requirements of

industry-standard buses such as Multibus® and VMEbus™. In addition, TI's BiCMOS devices can reduce disabled currents by 95% and active currents by 50%-80% compared to bipolar equivalents. Result: System IC power savings can be more than 25%.


There are more than 60 functions comprising TI's BiCMOS bus-interface family. Included are 8-, 9-, and 10-bit latches, buffers, drivers, and transceivers—a wide choice that means you can easily find what you need to implement high-performance bus-interface designs.



An innovative circuit design in TI's BiCMOS bus-interface logic helps lower disabled currents. This is key to overall power savings because in a typical bus network only one device is enabled at a time.

Turn page for more information





# Get high speed, low power, and low noise with TI's broad ACL family.

It's an extensive family that includes gates, flip-flops, latches, registers, drivers, and transceivers. It's a readily available family in DIP and SOIC packages. It's TI's high-performance EPIC™ ACL family, bringing with it an important bonus—major reductions in noise.

Family speed is comparable to advanced bipolar 54/74F: 24 mA of



When every nanosecond counts, TI's new high-performance ACL family can help you significantly improve system speed.

sink/source current will drive 50-ohm transmission lines; and low power is characteristic of TI's EPIC technology. All this with "ground bounce" substantially reduced compared with end-pin ACL. The reasons are innovative packaging and a circuit-design technique called OEC™ (Output Edge Control) which softens the transition states that cause simultaneous switching noise. In fact, EPIC ACL noise levels are typically 10% less than those of bipolar devices.

The rapidly increasing customer acceptance of TI's ACL family confirms its noise-reduction advantages and its ease of use.

## System design advantages

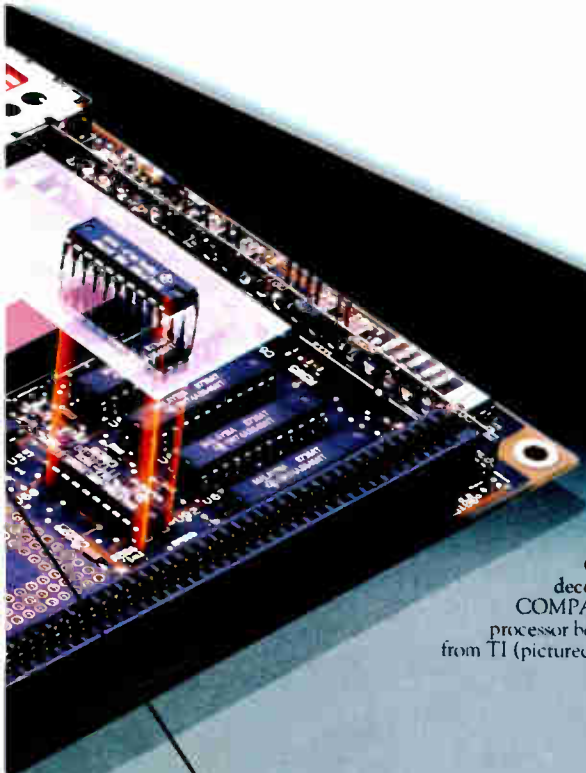
A unique "flow-through architecture" simplifies board design, layout, and troubleshooting. Inputs surround power pins on one side, outputs on the other, and control pins are strategically located at the package ends.

From a systems perspective, TI's arrangement offers the lowest-cost design when compared to end-pin ACL.

Because in circumventing noise problems, end-pin designs can require additional components that take up to 32% more board area and slow system performance.

There are 146 functions, in both AC and ACT versions, currently announced in TI's ACL family, including such innovative, highly complex functions as advanced transceivers, line drivers, latches, feedback registers, multiplexers, and counters.

This ACL family, developed in cooperation with and supported by Philips/Sigmetics, fully meets JEDEC industry-standard No. 20 specifications for Advanced CMOS Logic.



Contributing significantly to fast address decoding in speed-critical paths of the COMPAQ DESKPRO 386/20™ personal computer processor board are two TIBPAL16L8-10 PAL circuits from TI (pictured above a segment of the board).

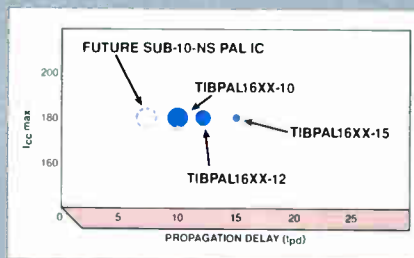
## Speed your system to market with TI's superfast PLDs.

PLDs are a functional alternative to standard logic ICs and gate arrays or standard cells.

Because TI's PLDs are off-the-shelf items you program yourself, you avoid the longer design cycle times of custom ICs and move on to market faster. These PLDs offer very attractive performance advantages. Consider these:

- **TIBPAL16XX-10 PAL ICs** from TI deliver a 10-ns propagation delay and are available in quantity. Clock-to-Q time is 8 ns, and output-registered toggle frequency is 62.5 MHz. IMPACT-X™ technology gives these PAL ICs their superior speed; they are well suited for use with high-speed processors such as the Motorola 68030, the Intel 80386, and RISC-based architectures. The 10-ns performance brings a higher level of integration to speed-critical paths.

- **TI's TIEPAL10H16P8-6 IMPACT™ ECL PAL circuit** delivers even faster operation: 6-ns propagation delay max. You can now streamline conventional ECL designs by consolidating several discrete components into a single custom function.
- **TI's new 7-ns Programmable Address Decoder** is intended to help you squeeze more performance out of memory interface systems. By performing address decoding much faster than conventional PAL architectures—in 7 ns—the TIBPAD16N8-7 allows you to take advantage of the new processors



TI's PAL IC road map shows consistent power and consistently higher speeds, with even faster versions on the way.

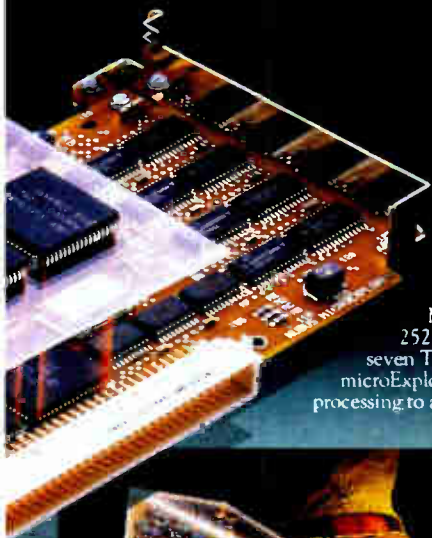
- to increase overall system performance.
- **TI's 50-MHz Programmable State Machines (PSMs)**, TIB825S105B (16 x 48 x 8) and '167B (14 x 48 x 6), are ideal for use in high-performance computing, memory interface, telecommunications, and graphics. These PSMs may be used to implement custom sequential logic designs such as peripheral I/O controllers and video-blanking controllers.
- **The TIBPAL22VP10-20**, with a 20-ns delay, is 20% faster than the competition's "A" version and much more flexible. A programmable output macrocell allows two extra, exclusive output configurations, for a total of six.
- **TI's TICPAL16XX Series 20-pin CMOS PAL ICs** are the cure for power problems. They operate at virtually zero standby power and are reliable, high-performance replacements for conventional TTL and HCMOS logic. The devices can be erased and reprogrammed repeatedly.

Turn page for more information





# logic. TI offers advanced logic families



Major logic consolidation, the equivalent of 252 MSI and LSI devices, was possible using the seven TI ASIC functions shown above the microExplorer™ board which brings symbolic processing to a Macintosh II™ desktop computer.



480 ps for a two-input NAND gate with a fanout of three; flip-flop toggle rates range up to 208 MHz. Both series offer output and bidirectional buffers with variable slew-rate control. And both series are fabricated in TI's high-performance EPIC process.

**A**pply TI's advanced logic to improve the performance of military systems.

Among TI's broad selection of logic devices produced to military requirements is a large PAL family. Propagation delays as fast as 15 ns are available over the military temperature range. The introduc-

tion of a 12-ns, 20-pin PAL circuit is planned, as well as military versions of the TIB825S105B and '167B Programmable State Machines.

TI is offering military counterparts selected from its ACL family, as well as 54F functions. Soon to come will be the BiCMOS family of bus-interface functions.

Included among TI's lineup of military ASICs are versions of the one-micron TGC100 Series gate arrays discussed at left, as well as two-micron standard cells.

TI's logic devices are among the more than 800 military functions offered compliant to MIL-STD-883C, Class B. Of this total, TI provides more than 200 to DESC-standard military drawings and is qualified to supply 285 JM38510 Class B devices (QPL 75).



## Milestones in Innovation

- TI's tradition for milestone innovations extends from the infancy of semiconductor technology into the MegaChip Era. Among the major highlights:
- First commercial silicon transistor (1954)
  - First commercially produced transistor radio (1954)
  - First integrated circuit (1958)
  - First integrated-circuit computer (1961)
  - First hand-held calculator (1967)
  - First single-chip microprocessor (1970)
  - First single-chip microcomputer (1970)
  - First single-chip speech synthesizer (1978)
  - First advanced single-chip digital signal processor (1982)
  - First video RAM (1984)
  - First fully integrated trench memory cell (1985)
  - First gallium arsenide (GaAs) LSI on silicon substrate (1986)
  - First single-chip Artificial Intelligence microprocessor (1987)

Turn page for more information.



# Comprehensive support from TI helps you improve your design performance as you improve system performance.

To enable you to excel in designing the logic portion of your system for maximum performance, TI has compiled or is making available a wide range of design tools and aids:

**PLDs:** The TI PLD data book (472 pages) contains design and specification data for 78 device types. Four application notes are incorporated as a reference tool. A qualification book is available, and a state-machine design kit is forthcoming.

**ACL and BiCMOS Bus Interface:** TI's ACL data book (348 pages) contains detailed specifications and applications information on the members of the one-micron ACL family. The ACL designer's handbook (299 pages) spells out the technical issues confronting advanced-logic design engineers and describes methods for handling the issues. A qualification book (358 pages) features extensive reliability and characterization data, die photos, and application derating factors. Customer evaluation capability is enhanced by TI's system evaluation board (available for demonstration through TI field sales offices) and third-party characterization boards.

Data sheets are available on each member of TI's BiCMOS bus-interface family.

**ASICs:** The TGC100 Series Design Kit gives you the tools needed to successfully complete a gate-array design: A



Extensive design support available for TI's systems logic families includes that for the new TGC100 Series gate arrays (at top), Programmable Logic Devices (at left), and Advanced CMOS Logic.

macro library for Daisy or Mentor engineering workstations containing the graphic symbol and functional and simulation models for each macro; a software library of TI-specific software tools that streamline and simplify the design process; a design manual that answers "how to" questions about design-

ing with the TGC100 Series; a two-volume data manual providing detailed specifications for each macro in the TGC100 Series software library; and a software user's manual.

An equally comprehensive design kit for the TSC500 Series is currently in development.

**For more information** on TI's advanced systems logic ICs and their support tools, complete and return the coupon today. Or write:

Texas Instruments Incorporated  
P.O. Box 809066  
Dallas, Texas 75380-9066

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Yes, please send me the following:

- RY01 \_\_\_\_\_ ASIC Information Packet  
DZ01 \_\_\_\_\_ Programmable Logic Device Data Book  
CA01 \_\_\_\_\_ ACL/BiCMOS Information Packet  
CB01 \_\_\_\_\_ BiCMOS Data Sheet Packet

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World Radio History

**TEXAS INSTRUMENTS**

# NOW A LED CAN TAKE ON THE LIGHT BULB

## SAN JOSE, CALIF.

That light shining from street signs, emergency beacons, and even stadium scoreboards could soon be coming from a new source—an aluminum gallium arsenide light-emitting diode developed by Hewlett-Packard Co. HP has taken advantage of advances in semiconductor laser technology to develop the device which, when combined with new packaging and light-flux management techniques, will ultimately provide light output 125 times greater than HP's most recent LED products.

The new red LEDs are expected to compete for the first time with incandescent lamps in high-intensity applications, such as automobile taillights and brake lights, large-area sign illumination, obstruction lighting on radio transmitter towers, and airport runway lights—a big departure from traditional LED uses. In addition to the increased brightness, the company's optoelectronics division in San Jose has also made advances that improved rated life and overall operating costs to the point of being competitive with lamps.

"HP was able to develop its new LED technology by taking advantage of 15 years' experience in developing infrared LEDs and low-threshold lasers," says marketing engineer Chris LeBlanc. By slight modifications in the structure, he says, it was found that LEDs using AlGaAs could be built that shifted the output into the red portion of the spectrum.

They far outstrip the first AlGaAs devices, which were single-heterojunction, absorbing substrate structures (see figure, top left) consisting of at least two layers of AlGaAs on a GaAs substrate. Light generated in the active layer escaped out the sides and through the top. These devices are the easiest to grow because they have the fewest layers and good thickness control. But they are also the dimmest, because the GaAs substrate absorbs light. Also, they are only marginally brighter than the best GaAs phosphide red LEDs.

**BRIGHTER.** For applications where it is necessary to see the LEDs in bright ambient light, most manufacturers use a double heterojunction with three AlGaAs layers on a GaAs substrate (see figure, top right), LeBlanc says. A much higher efficiency device, it is at least twice as bright as the single heterojunction device.

The new "transparent" substrate double-heterojunction AlGaAs LEDs constitute another step forward. They consist of at least two wide-bandgap active layers on each side of a thin active layer, similar to the absorbing substrate version. But, in this case, the substrate is

etched away (see figure, bottom), eliminating the internal absorption and resulting in extremely high-efficiency LEDs—at least four times the brightness of single-heterojunction AlGaAs LEDs and GaAsP LEDs using equivalent drive currents. And because at least one layer is extremely thick (150  $\mu\text{m}$  vs 30  $\mu\text{m}$ ), it can be driven at much higher voltages and currents. This produces brightness higher than anything previously achieved in LEDs, says Michael Clarkin, an optoelectronics division applications engineer.

## HP device uses chip technology, new packaging and light-flux management

But the superthick AlGaAs layer has made the transparent substrate AlGaAs LED difficult to use in commercial applications because it is extremely difficult to fabricate with any degree of reliability and consistency.

That's where HP's latest development comes in. It is a manufacturing technology based on a post-epitaxial-growth wafer process that requires no photolithography, allowing it to reproduce this complicated structure in very high volumes.

The numbers are impressive. When a new LED was incorporated into a redesigned version of the standard 12-mil-by-12-mil T1-3/4 LED package, the light output was three candela, with a forward

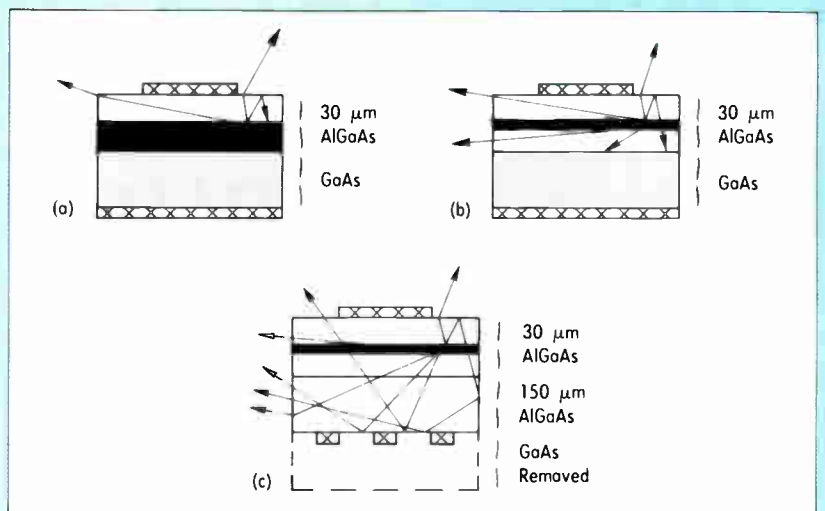
current of 20 mA, about three times the light output of previous absorbing substrate AlGaAs LEDs HP introduced last year. It is about 10 to 15 times that of high-efficiency red LEDs made with GaAsP, which constitutes 90% of the current LED chip production because of the low cost.

**MORE IS COMING.** But even better results are possible, says Clarkin. When incorporated into a new T4 LED package designed for TS AlGaAs LEDs, the new device's light output will be at least three to five times higher, as much as 10 to 15 cd at 20 mA, he says.

Under development, Clarkin says, is a new modular package design that incorporates parabolic reflector surfaces for use with arrays of such LEDs in large signaling applications. In the modular package design, each cell can easily achieve light outputs as high as 20 to 25 cd at 20 mA. And, unlike previous LED structures that suffer from degrading rapidly at higher forward currents, the TS AlGaAs process developed by HP can handle currents as high as 300 mA, which results in light outputs as high as 125 cd.

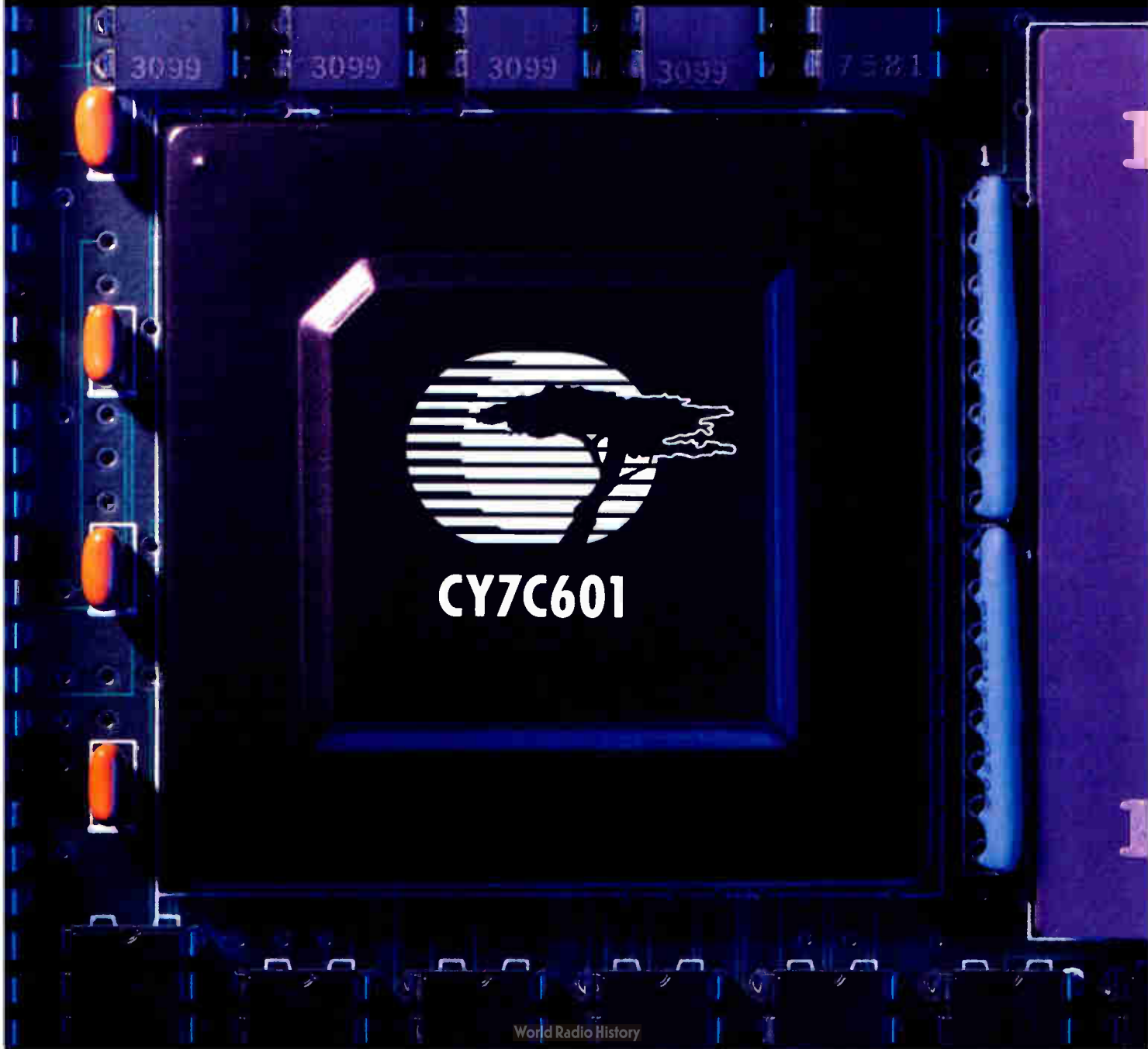
This is equivalent to or better than what can be achieved with incandescent light sources, says LeBlanc. And the LED also has a longer overall operating life than incandescent sources. For example, a lamp in a T1-3/4 package operating at 1.35 V and 15 mA has a 500-hr. operating life, and a roughly comparable 1.7 V, 20 mA TS AlGaAs LED has a 100,000 hour lifetime, he says. —Bernard C. Cole

## HOW TO MAKE BRIGHTER LEDs



The new HP AlGaAs red LED (c) outshines both the single-heterojunction, absorbing-substrate model (a) and the double-heterojunction, three-layer type (b).

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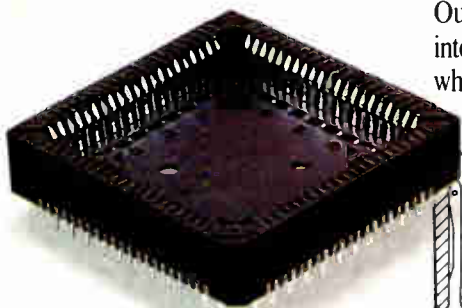
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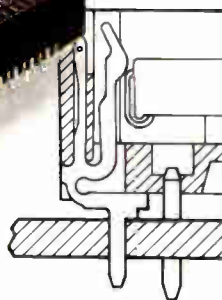
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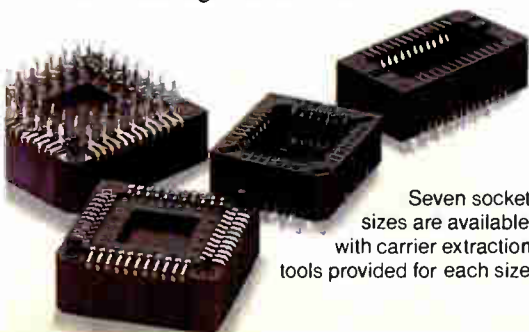
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# AMD'S CHIP SET BOOSTS LASER-PRINTER SPEED

SUNNYVALE, CALIF.

Advanced Micro Devices Inc.'s two-chip entry in the burgeoning market for high-performance embedded controllers for laser-printers lets low-end printers achieve throughputs at up to eight pages/min—that's four to six times present technology. It joins other chips—such as those from Acer Technology, Cirrus Logic, and National Semiconductor—designed to speed laser printing [*Electronics*, July 1988, p. 95].

The Sunnyvale company's Am95C75 raster-printer controller and Am95C76 orthogonal rotation processor provide the boost by implementing in silicon many functions now done in software. Both chips are fabricated in 1.5- $\mu$ m CMOS.

Essentially a slave processor optimized for raster-printer-control applications, the Am95C75 contains a 16-bit ALU, an instruction set optimized for graphics and printer applications; font, CPU, and video interface logic; color combination logic, a barrel shifter, and row and column address logic. The Am95C76 implements the rota-

tion fonts of a complete character set prior to page printing, and the character set can be cached and retrieved as needed, says Richard Irving, product marketing manager. If fonts do not need to be rotated, the ORP can be easily bypassed, because the CPU can command the controller to dispatch a character without rotation.

The chips efficiently handle new laser printers that cover both sides of a page

The controller performs processing functions much more efficiently than general-purpose controllers. Rather than having to transfer every word of a font character's bit map, for example, the host CPU can simply tell it to fetch the character from its cache and transfer it to a bit-aligned location in the page buffer.

The controller integrates several important functions to optimize its printer

dataflow. It has a 32-bit barrel shifter, allowing faster bit alignment than if done by the CPU. Its private bus interfaces allow the most efficient page buffer and font cache accesses.

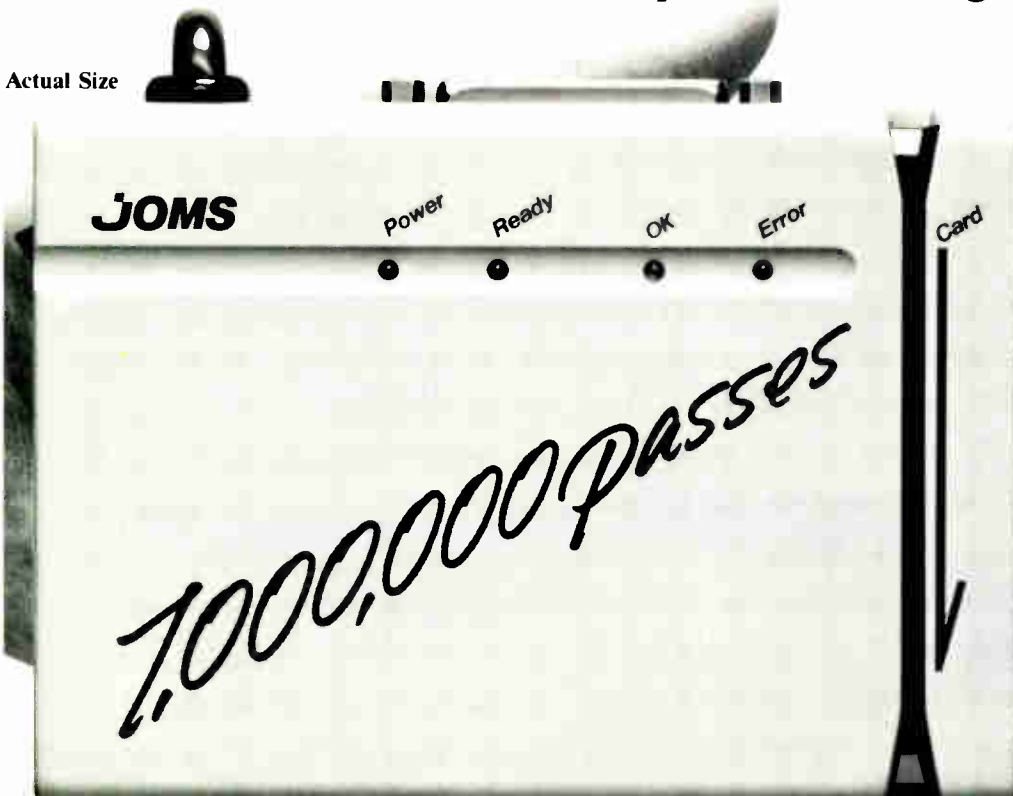
Where the 95C76 comes into play, says Irving, is in complex page-description-language applications, where much of what is printed consists of text. Most often, documents are produced in portrait mode, where the text runs across the narrower dimension of a page. But sometimes documents must be printed in landscape mode, where text runs along the wider dimension of a page. In addition, new printers print on both sides of the page. This means the text cache memory has quadrupled in size: where once only portrait-mode fonts were stored, a 90° rotated character set is now needed to support landscape printing, in addition to 180° and 270° rotated sets to print in portrait and landscape on the back of a page.

This problem is solved in the Am95C76 rotator processor through the incorporation on-chip of a 64-by-64-bit data array into which a font character is written. The processor's single programmable register contains the character rotation angle (0, 90, 180 or 270 degrees). Once a character has been written in, it can be read out via the same 16-bit data bus in its rotated form. *—Bernard C. Cole*

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# PROCESS CONTROL GOES HIGHER TECH

**PHILADELPHIA**

Third-party vendors are getting a new, more powerful breed of process control system to complement their cutting-edge expertise. A raft of hardware and software upgrades is coming from Honeywell Inc., which has implemented changes in its industry-standard TDC3000 process control system.

Real-time performance, high-level compatibility with Digital Equipment Corp.'s VAX family, relational data bases, a 5-Mbit/s system bus, and 32-bit processing power have been integrated into Release 210 of TDC3000 without compromising downward compatibility in the TDC family, introduced in 1975. That opens up an installed base of more than 3,500 systems in 61 countries and a projected new market of \$3 billion, says Markos Tambakeras, marketing vice president for Honeywell's Industrial Automation Systems Division, Phoenix, Ariz.

Of particular interest to third-party software vendors is Honeywell's commitment to Digital Equipment Corp.'s VAX as a totally integrated computing module on the TDC3000 Local Control Network. At the business strategy level, Honeywell will purchase and integrate VAXes into the system—as well as provide hardware and software support.

At the technology level, the jointly developed CM50S hardware-and-software bridge lets VAX applications programs access real-time process data from the distributed control system on the factory floor. This means business and operational strategies can be merged. Profit maximization software running on the VAX, for example, can direct the operation of the process control system.

**GROWTH.** Although there is already a large process-control software base for the VAX, the upgraded TDC3000 will open more opportunities, says Don Bell-Irving, manager of DEC's Computer Integrated Manufacturing applications marketing sector. Examples are information management and scheduling as well as statistical quality control, he says.

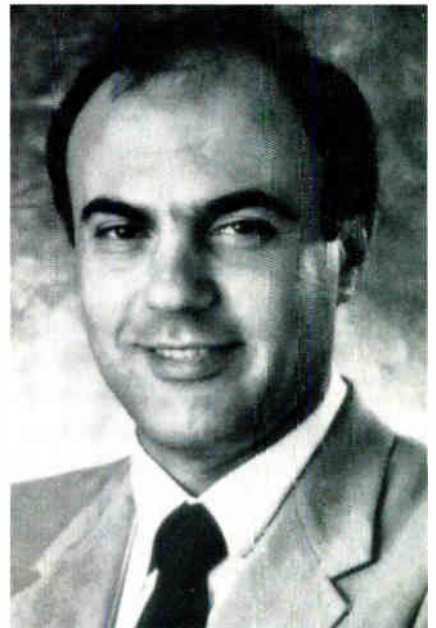
As evidence of its commitment to an open system, Honeywell disclosed agreements with three third-party vendors who have process-control applications software: Weyerhaeuser Co., for plant-wide automation; Texas Instruments Inc., for tank gauging; and Novacorp Ltd., Alberta, Canada, for pipeline transportation.

Applications programs running on the DEC VAX address the system's control, supervisory, and plant information functions. But there is also something new at the sensor and control levels. Honeywell has opted for multivendor interoperability by imple-

menting process control with a network based on a redundant, real-time Manufacturing Automation Protocol. Both the redundant and real-time aspects of a MAP network are firsts in the industry, says Tambakeras. In fact, MAP standards have not yet addressed these functions, but Honeywell has committed itself to migrating to them as they develop.

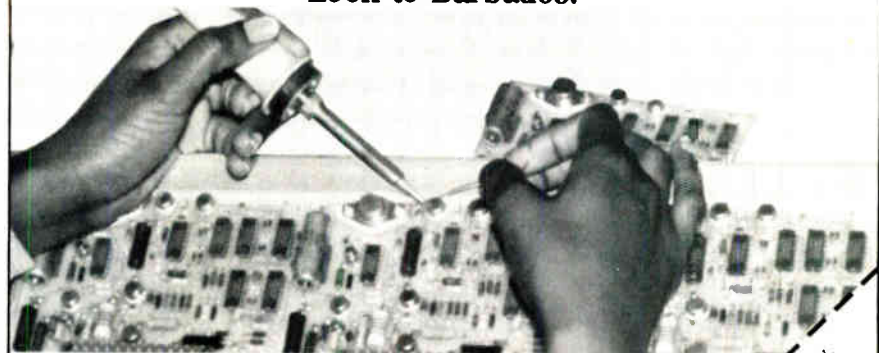
Honeywell's real-time MAP implementation—the Universal Control Network—is a 5-Mbit/s, carrier-band, token-passing network based on Open System Interconnection recommendations. It uses redundant coaxial cables, and supports peer-to-peer communications among network devices.

The TDC3000 has also been enhanced to leverage relational data-base technology—both through the VAX and a new Honeywell product called Event History, says Ernest M. Smith, senior product manager. Running on a Honeywell Bull Model 200 minicomputer, Event History can accommodate 100 files, each with up to 10,000 records with up to 200 user-defined data-value fields. —*Jack Shandle*



Honeywell marketing vice president Tambakeras is looking at a \$3 billion market.

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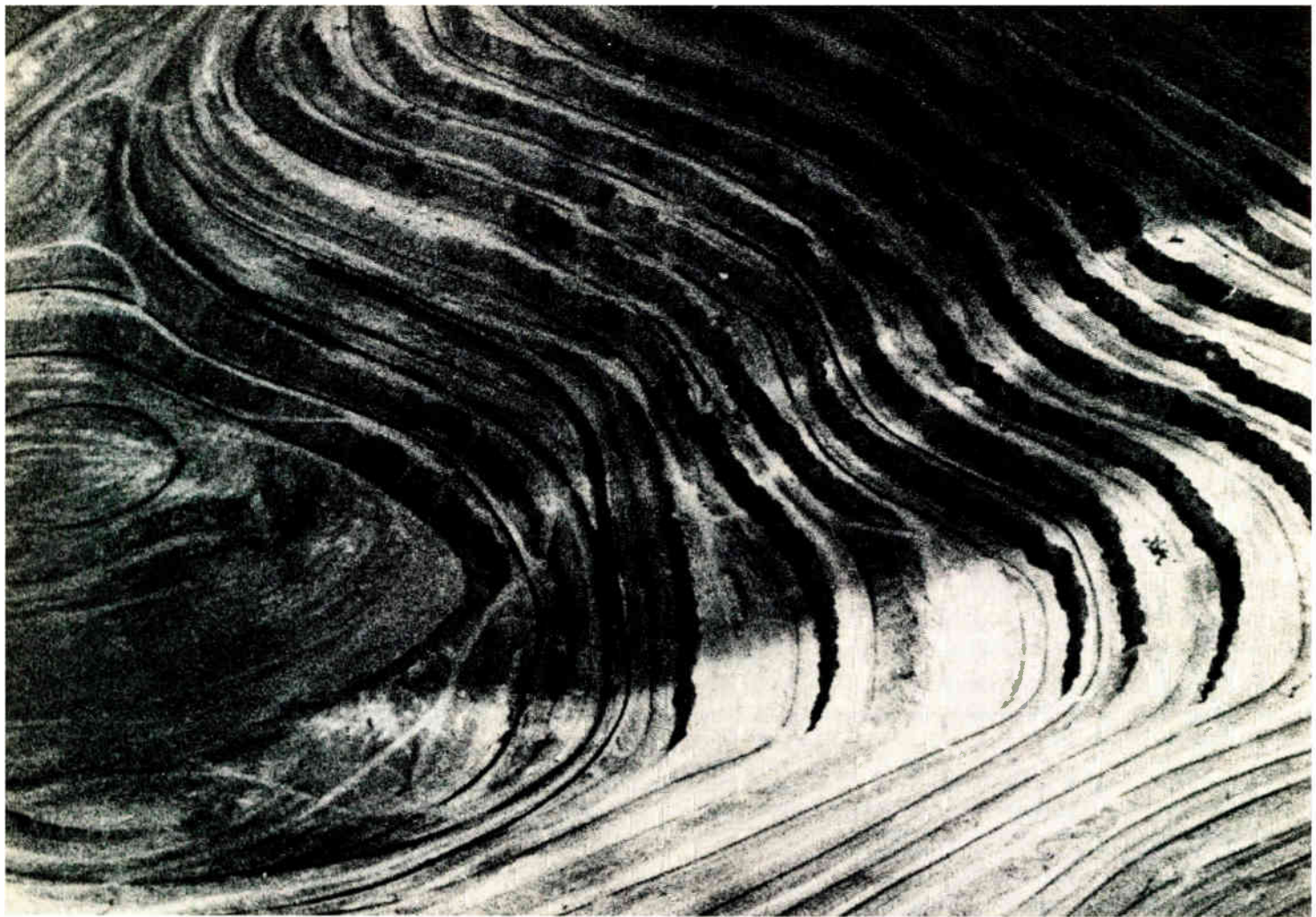
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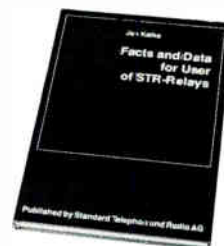
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# X-RAY STEPPERS? THIS STARTUP IS READY

## MARLBORO, MASS.

When will optical lithography steppers finally run out of gas in resolving circuit details? It has taken longer than expected—and it won't come too soon for the makers of the X-ray stepper systems that are poised to succeed them. When it does happen, a Marlboro, Mass., startup called Hampshire Instruments Inc. is preparing a system with what the company calls a can't-miss combination of features. What's more, it even uses conventional photoresists.

Hampshire has combined in its high-throughput Series 5000P a patented laser-based X-ray source with advanced mask/reticle materials. "It's a great machine—the most advanced stepper available compared to others I've seen," says Joseph Grenier, associate director of the semiconductor equipment and materials service at Dataquest Inc., the San Jose, Calif., market researcher. Still, Hampshire faces an uphill battle, he says. "The semiconductor industry is extraordinarily conservative and will continue working with the technology it knows."

The market in 1991 for X-ray systems

will hit \$40 million, compared with "whatever Hampshire ships" this year, says Grenier. For optical machines, the 1991 market will be \$970 million, up from \$680 million this year. Already, Hampshire executives say they have orders for "between 5 and 10" of its \$2 million X-ray lithography stepper systems. Hampshire

## \$2 million system features high throughputs, and uses conventional resists

co-founder and president Moshe Lubin believes the 5000P is two years ahead of optical steppers in its ability to deliver circuit geometries finer than 0.5  $\mu\text{m}$  today.

Today's optical steppers, which sell for about \$1.5 million, can resolve geometries to about 0.8  $\mu\text{m}$ . At least one improved optical stepper, from GCA Corp. of Andover, Mass., uses an excimer laser light source to deliver 0.5- $\mu\text{m}$  resolution.

Current tube-based X-ray systems deliver submicron geometries, but are develop-

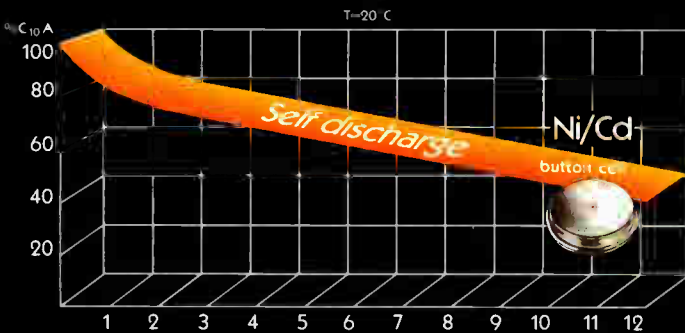
mental systems that sell in the \$3 million range. Synchrotron-based X-ray steppers are in development in the U. S., Japan, and Europe that will resolve less than 0.2  $\mu\text{m}$ , but production versions could be priced 20 times higher than the 5000P.

The Hampshire system employs a high-brightness neodymium glass laser that directs pulsed power onto an alloyed target, creating an extremely bright X-ray source with a small spot size. The laser's interaction with the target generates a dense plasma, rich in electrons. The source is about 10 times more powerful than those in conventional tube-type X-ray systems, says James Forsyth, Hampshire's vice president for technology.

That power is best measured in milliwatts/cm<sup>2</sup> delivered to the photoresist. Hampshire's prototype delivers 2 to 5 mW/cm<sup>2</sup>; production systems will deliver 10-15 mW/cm<sup>2</sup>, Forsyth says. In contrast, a typical tube X-ray source might deliver 0.2 mW/cm<sup>2</sup>. Forsyth says that particular combinations of lasers and targets deliver soft X-rays having the short wavelengths (0.8 to 2.2 nm) needed for submicron lithography. —Lawrence Curran

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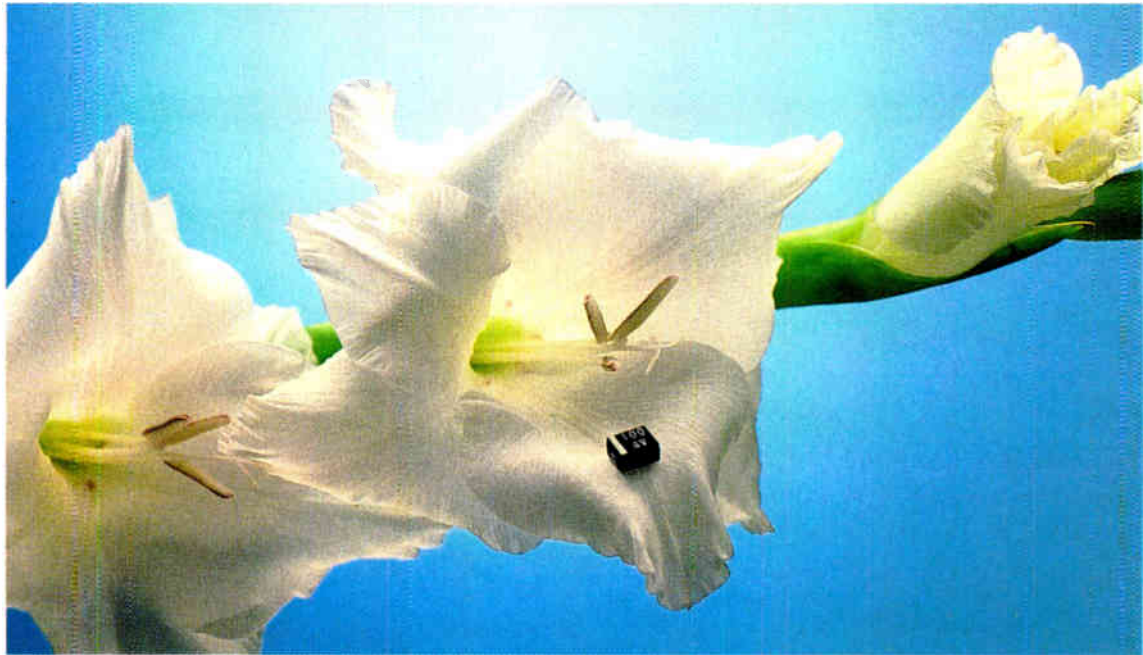


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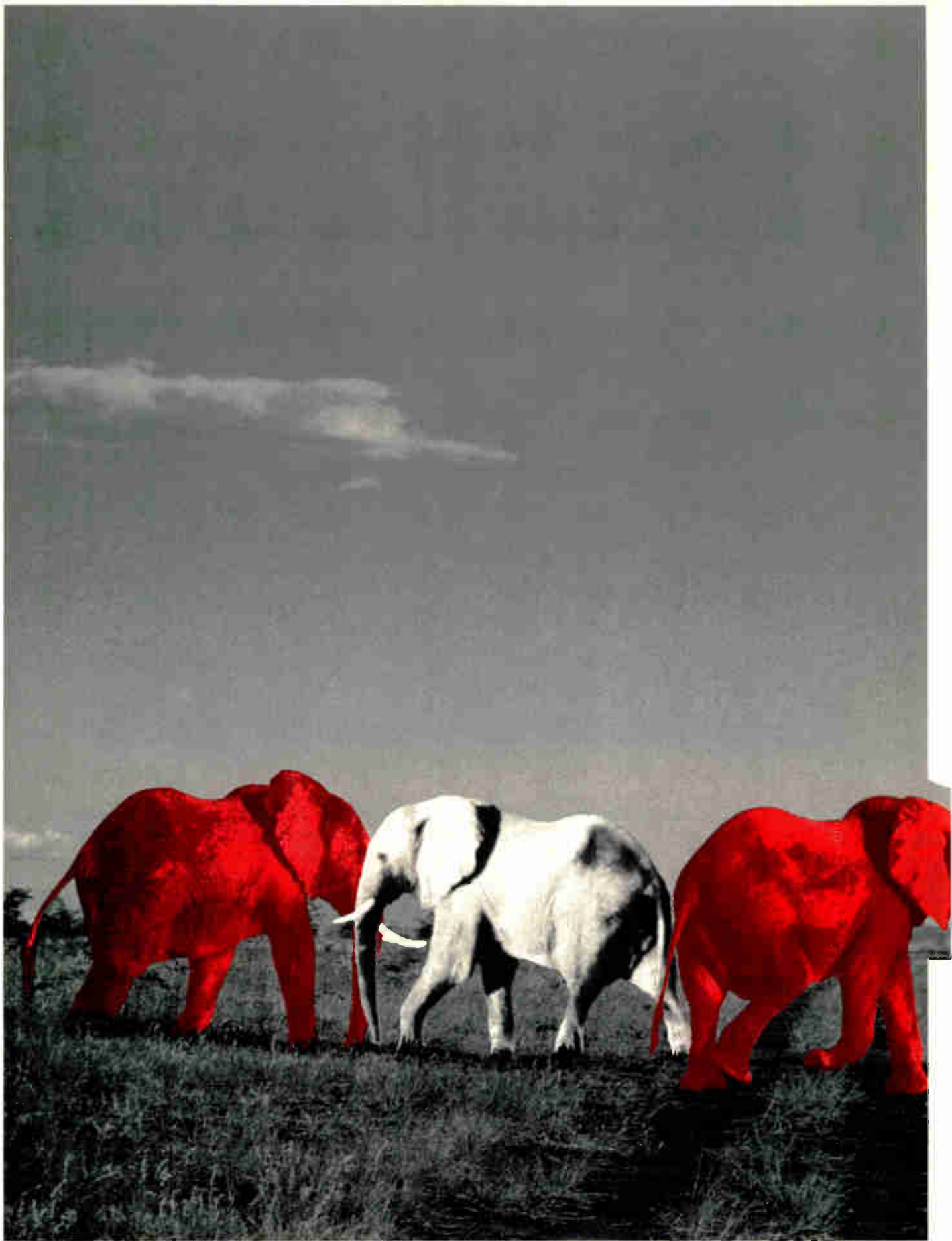
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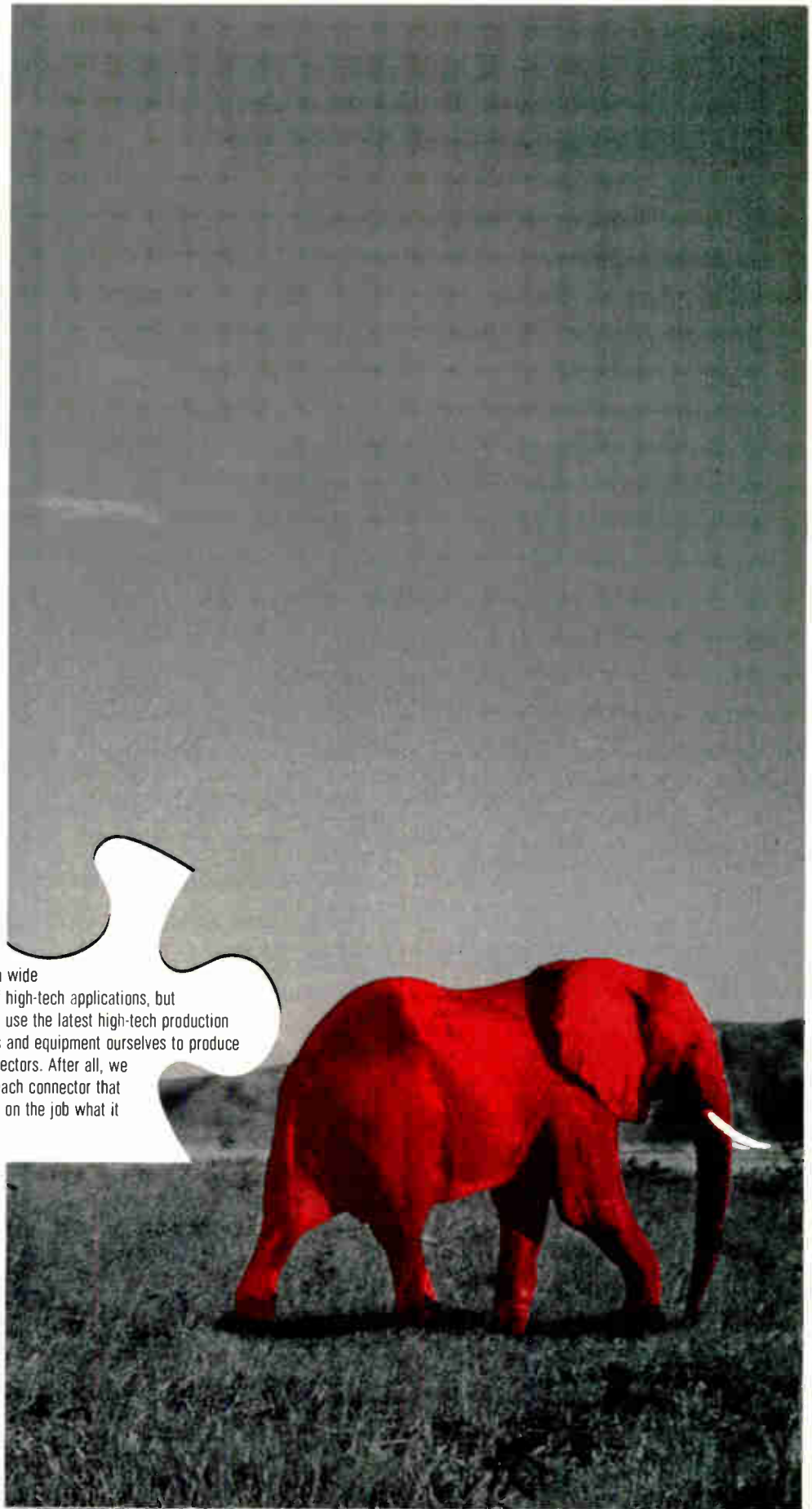
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# PLAIN-JANE POWER SUPPLIES BEGINNING TO GET SEXY

## LOS ANGELES

The technology doldrums have ended for the power supplies used in military electronics. It will be difficult for anyone to take power supplies for granted in the future because several companies are expanding the supplies' capacities and promising more on the market. Not only have the power densities doubled, but products on the drawing board promise to double them once again in leading-edge products. Just as important is the development cycle for the units, which is growing markedly shorter. Giving all these changes a push are advances in components, magnetic materials, and packaging.

The latest proof of this headway comes from GMHE/Hughes Aircraft Corp., which has a prototype of the previously-unheard-of power densities of 21.7 W/in.<sup>3</sup>, more than double the 10 W/in.<sup>3</sup> products Texas Instruments

Inc. came out with last year, which sparked the renaissance [*Electronics*, March 17, 1986, p. 22].

Even bigger advances are in sight at AT&T Bell Laboratories where researchers are working on an experimental supply that already has achieved 50-W/in.<sup>3</sup> densities in tests. Funded by the Air Force, the program at Bell Labs' Power Conversion Technology Department, Parsippany, N. J., has also demonstrated switching speeds of about 20 MHz and an 81% efficiency.

**AVIONICS NEEDS.** Driving these advances are the needs of avionics gear, which use an ever-improving generation of airborne processors based on chips produced by the Pentagon's Very High Speed Integrated Circuit Program.

The Hughes prototype power supply delivers the 500-W output at densities of 21.7 W/in.<sup>3</sup>, at 83% efficiency. The workhorse HVS-200 model in the TI line of high-density supplies has a 200-W output, 10 W/in.<sup>3</sup> density, and 80% efficiency.

Hughes markedly cut previous development time by finishing in less than one year, compared to nearly five years for the TI project. The improved time has more to do with the availability of a number of better components than with any breakthrough in engineering ability, says Derek Lidow, executive vice president at

International Rectifier Corp., El Segundo, Calif., which sells the lion's share of the power-MOS field-effect transistors that are replacing conventional discrete-bipolar parts.

For example, improved military versions of commercial MOS FETS offer faster switching speed, (the supply is rated at 600 kHz frequency), lower input levels, and power dissipation levels reduced by some 20% over earlier components.

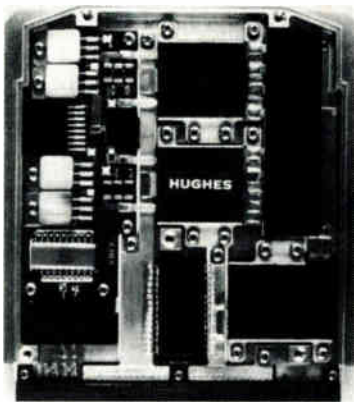
The new multilayer ceramic capacitors have better resistance and inductance values. Probably the most difficult task for the suppliers to accomplish was coming up with the lower-loss materials used to design the magnetic cores with lower profiles.

The availability of the new high-performance power supplies could heat up the business scene. Because of its early start, TI has a lock on the military market, with some 350

units slated to be sold this year, according to Gary Dobbs, marketing manager of Advanced Power Supplies Inc., Dallas, Texas. The \$100/W price tag (the HVS-200 is \$20,000), makes it a profitable line, even though the prospect is for these prices to be halved within several years. But TI knows competitors are edging up. "We were two years ahead, now it's only eight months," Dobbs concedes.

Hughes is considering the step it will take after its own programs pick up the new supply. Since the military electronics firm is not geared to make these products economically, it is looking for an outside specialist to carry the ball. It already has received bids to mass produce for as little as \$30/W. If it does subcontract, spokesmen for the company say they would expect to undercut the TI line in pricing to third parties.

The vast commercial power-supply market lying beyond the military market can use peak performance at the upper end but is sensitive to cost. Prices for the best commercial supplies would need to be at about \$5/W. This sensitivity means only the military can afford the new supplies right now, says International Rectifier's Lidow. But he believes current happenings "portend dramatic changes [in commercial supplies] in the next two to three years." — Larry Waller



Hughes improved its power supplies using recently advanced components.

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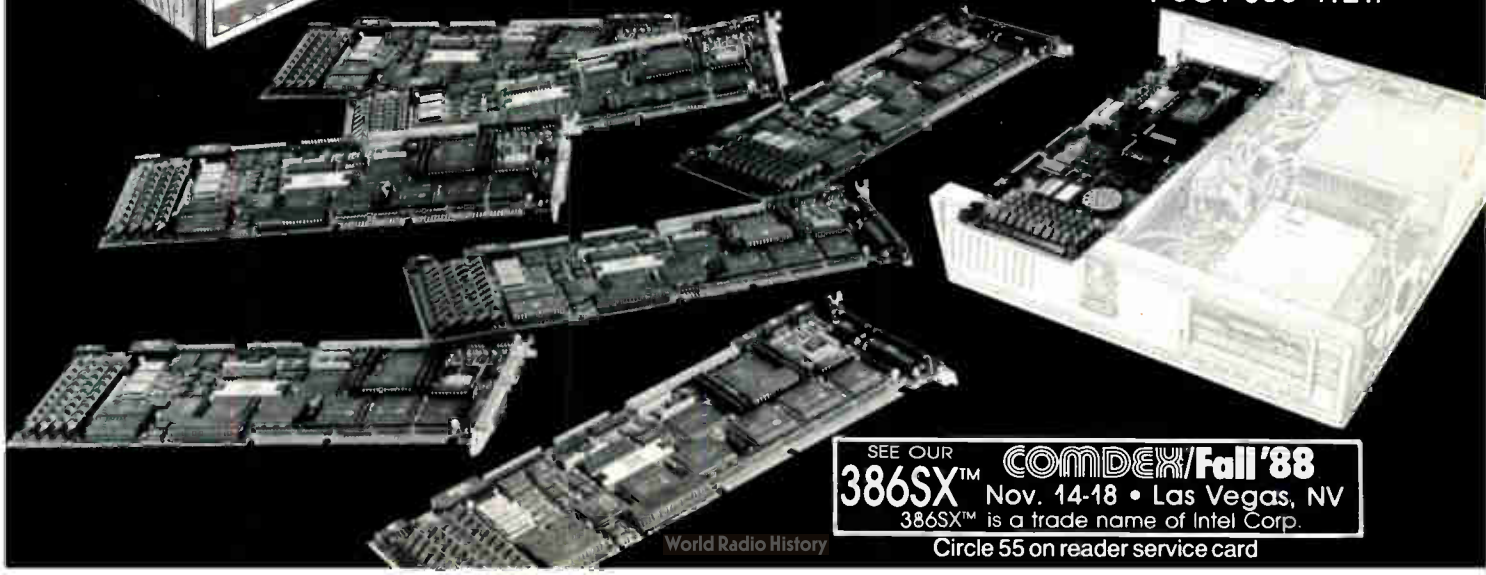
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# COULD THIS PROCESS BE IT FOR SILICON-ON-INSULATOR?

## TAUNTON, MASS.

The prospects are enticing: power integrated circuits with oxide layers able to withstand 5 kV; CMOS or biCMOS device densities 30% greater with no geometry shrinks; and inherently good radiation resistance. These are just a few of the promises held out for new silicon-on-insulator technologies.

One of the first successful processes using SOI techniques has now arrived from Kopin Corp. of Taunton, Mass., which calls its proprietary process Isolated Silicon Epitaxy. ISE is said to yield an insulating silicon dioxide layer that is less expensive than sapphire in silicon-on-sapphire structures—another approach to achieving device isolation. Nor is SOI as prone to performance-degrading defects at the interface with silicon as sapphire is, says John Fan, Kopin's chairman and chief executive officer.

Kopin is already supplying semiconductor manufacturers with 3-, 4-, and 6-in.-diameter gallium arsenide-on-silicon wafers [*Electronics*, Oct. 15, 1987, p. 47]. Now, after some five months of selected beta testing, the company is ready to ship more samples of its 3-, 4-, and 5-in. SOI wafers to device makers. Early indications from the beta sites are that the ISE wafers are compatible with just about any subsequent device processing, including bipolar, CMOS, biCMOS, and dielectric isolation, Fan says.

Kopin isn't alone in SOI work. Several other companies, including Texas Instruments, Harris Semiconductor, and Honeywell have projects under way. Most of those employ a Simox process, which uses ion implantation to deposit an oxide layer between a silicon substrate and a top layer of single-crystal silicon. TI's Si-

mox SOI project is about to graduate from its Central Research Laboratories in Dallas to prototype production.

Harold Hosack, director of the SOI project at TI's lab, reports that the company has already fabricated 16- and 64-Kbit static CMOS random-access memory devices on 4-in. wafers that show "excellent characteristics." However, Hosack says he is not aware of any other commercially available SOI wafers, adding that TI has ordered wafers from Kopin to evaluate.

Out of a market for silicon wafers that

## TI, Harris, and Honeywell are also working on SOI techniques

stands at \$1.2 billion this year, and will grow to perhaps \$2 billion in five years, Kopin can realistically target about 10%, Fan believes.

But Fan is hoping that most potential users will respond favorably to the price premium attached to the ISE wafers, which will sell for about three times the price of bulk silicon wafers. Those wafers sell for about \$20 each. He adds that most of the beta site users say they'd pay \$60 to get better device performance because their payback would more than offset the higher cost.

High-performance biCMOS and semiconductors that must operate at high temperatures will especially benefit from SOI, whether it is Kopin's process or another, says Drew Peck, a semiconductor analyst at Donaldson, Lufkin & Jenrette Securities Corp. in New York. "John Fan probably has more experience in exotic

materials than anyone else I know," adds Peck. "He's also aware of both the technical and marketing barriers to new materials and seems to have a sensible strategy for commercializing SOI."

But Peck cautions that the SOI market is still in its infancy. "There's a long testing period ahead. We could see commercial products using SOI within two years, though, and Kopin is likely to be a major player in this market when its time comes."

Kopin's ISE process is a substantial refinement of Zone-Melt Recrystallization (ZMR), a technique developed by Fan and others when he worked at MIT Lincoln Laboratory, Lexington, Mass., in the late 1970s. Kopin has exclusive licenses to use MIT's ZMR patents.

The company won't divulge its recipe in detail, but the process begins with a bulk silicon wafer over which Kopin thermally grows a layer of SiO<sub>2</sub>. The wafers then go into another furnace, where a polysilicon layer is deposited, on top of which another oxide layer is later grown.

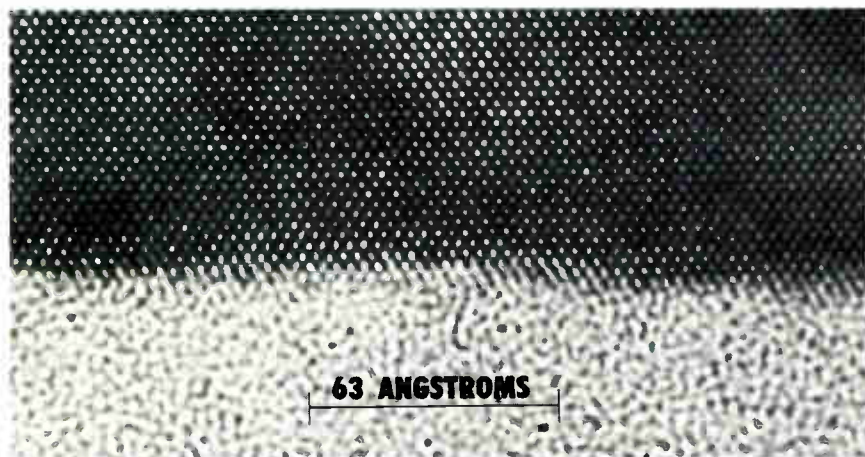
Kopin works its magic somewhere between the polysilicon and top oxide growth. A seed of single-crystal silicon comes in contact with the silicon substrate and is drawn across the wafers using a movable strip heater. The polycrystalline film turns into single-crystal silicon in that drawing process. Eventually, the top oxide layer is etched away, leaving a three-tier structure: single-crystal silicon epitaxy atop SiO<sub>2</sub> atop the silicon substrate.

**HIGH VOLTAGE.** The SiO<sub>2</sub> layer's thickness can be varied easily, Fan maintains. For high-voltage devices able to withstand as much as 5 kV, the oxide layer would be between 1 and 2  $\mu\text{m}$ ; the silicon epitaxy would be 2 to 3  $\mu\text{m}$ . Fast CMOS devices could be made in an epitaxial layer of about 0.3  $\mu\text{m}$  on top of a 1- $\mu\text{m}$  oxide. The same dimensions would hold for radiation-resistant devices, while bipolar circuits might require 1.5- to 2- $\mu\text{m}$  of epitaxy atop a 1.0- $\mu\text{m}$  oxide.

CMOS devices can be packed more closely on Kopin's SOI wafers, Fan says, because there's no need to devote substantial real estate to the insulating oxide trenches now used to prevent latchup between nearby devices. The SiO<sub>2</sub> prevents latchup.

Nor is there the carrier mobility from the underlying silicon substrate to the epitaxial layer, which is what interferes with normal device operation under alpha particle radiation. The natural radiation resistance results from the carriers being trapped under the oxide, unable to reach the surface epitaxial layer where the active devices reside.

No detectable metallic impurities result from the process, and defect densities on the surface are between 10<sup>7</sup>/cm<sup>2</sup> and 10<sup>8</sup>/cm<sup>2</sup>. That compares with 10<sup>8</sup> to 10<sup>9</sup> in SOS, Fan says. —Lawrence Curran



A key to Kopin's new silicon-on-insulator structure is a proprietary process that takes place between the polysilicon and top oxide growth shown in this micrograph.

# AT LAST, A STANDARD ON-CHIP TEST BUS

## FRANKFURT, WEST GERMANY

Test and quality-control engineers have long hungered for a standard for an on-chip test bus that will allow fast and easy testing of printed-circuit boards containing complex very large-scale integrated circuits. But marketers have been opposed, arguing that it would make chips more expensive and harder to sell. Now it appears that the engineers have won out, and a standard is close to approval.

The driving force is the Joint Test Action Group, an organization of major European, U. S., and Japanese equipment and semiconductor manufacturers. Philips of the Netherlands started JTAG in 1985, and its members are all behind the standardization drive now. The group has drawn up a standards proposal that has been adopted by the Test Bus Standardization Committee of the Institute of Electrical and Electronics Engineers. Approval could come as early as December.

"Final standardization is then only a formality," says JTAG chairman Harry Bleeker, who is also manager of the Computer-Aided Testing and Manufacturing department at Philips' Telecommunication and Data Systems Division in Hilversum, the Netherlands. "We should have it by early 1989," he says.

The P-1149 proposed standard specifies a test bus on microprocessors, application-specific ICs, and complex merchant-market devices. It is made up of a chain of shift registers along the periphery of each chip, enabling it to perform what is called boundary scan test. Developed at Philips, the BST encompasses three important classes of checks that are made on the pc board: external tests, which check the circuitry between ICs; internal tests, which check the functioning of internal IC logic; and sample tests, which monitor signals flowing into and out of the device during system operation.

Because major semiconductor firms like National Semiconductor and TI, and equipment makers such as GenRad and Teradyne are already involved in BST activities, implementation is expected within the next two years, Bleeker says. "Commercial VLSI devices using the BST architecture will then be available." A number of ASIC producers already have BST elements in their libraries for full- and semicustom parts.

The early opposition of marketing executives faded when engineering executives at big firms put their weight behind the technique and the efforts to standardize it. Typical is the position of George H. Heilmeier, senior vice-president and chief technical officer at Texas Instruments Inc., who says, "The goals and objectives

of JTAG are consistent with TI's philosophy of providing products that are both functional and testable."

And there was lot of weight. Besides AT&T, British Telecom, IBM, Philips, and TI, a number of other firms in the U. S. and Europe are endorsing BST standardization as members of JTAG. Among them are Digital Equipment Corp., GenRad, National Semiconductor and Teradyne in the U. S. The European list includes: Denmark's Elektronik Centralen; France's Honeywell Bull and Thomson; Sweden's L. M. Ericsson; West Germany's Nixdorf Computer, Siemens, and Standard Elektrik Lorenz; and the UK's

put and output connections and carries appropriate clock and control signals. When a board contains a number of chips with the test bus, the chips' shift-register chains can be interconnected to form a single path through the whole board.

In the external test mode, which tests the interconnections between chips, test data is shifted into all cells associated with the output pins and loaded in parallel to those cells associated with the input pins. The internal mode, which checks out the IC's internal logic, delivers test data to the chips and examines test results through the serial path.

The sample test mode, the third that

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General Electric and Plessey.

In testing digital boards, BST offers a solution to a serious problem in semiconductor testing: the increasing complexity of ICs and the limited accessibility of surface-mounted devices on a board make in-circuit testing a time-consuming job that requires costly hardware. Also, applying test signals to the board can damage the chips with backdriving.

**NOT THE ANSWER.** One solution is functional testing. Here the functions of the entire board are performed by feeding test signals to the normal inputs. The drawback, however, is the need to generate comprehensive test programs for each board design. That can be a costly process for large, functionally complex boards.

BST is the answer. The on-chip bus consists of boundary scan cells, each containing a shift-register latch. The cells, adjacent to each pin, are interconnected to form a shift-register chain around the chip's periphery. This path has serial in-

puts and outputs, monitors signals flowing into and out of the chip without affecting circuit operation. It can be used in, say, debugging or as an aid in fault diagnosis and system maintenance.

Originally, the BST architecture was a simple scan interface to support board-level tests. But as the group's membership grew, other needs had to be considered. So the architecture was expanded and made part of the final version of the standard proposal, Version 2.0.

The new architecture contains a few additional elements, among them a test access port providing access to many support functions built into the circuit; a test-access-port controller receiving the dedicated test clock signal and generating the clock and control signals for the test data registers; and a bypass register composed of a single bit register and used to bypass a chip's shift register. Provisions have been made to the test-access-port controller to enable implementing self-tests in the future.

—John Gosch

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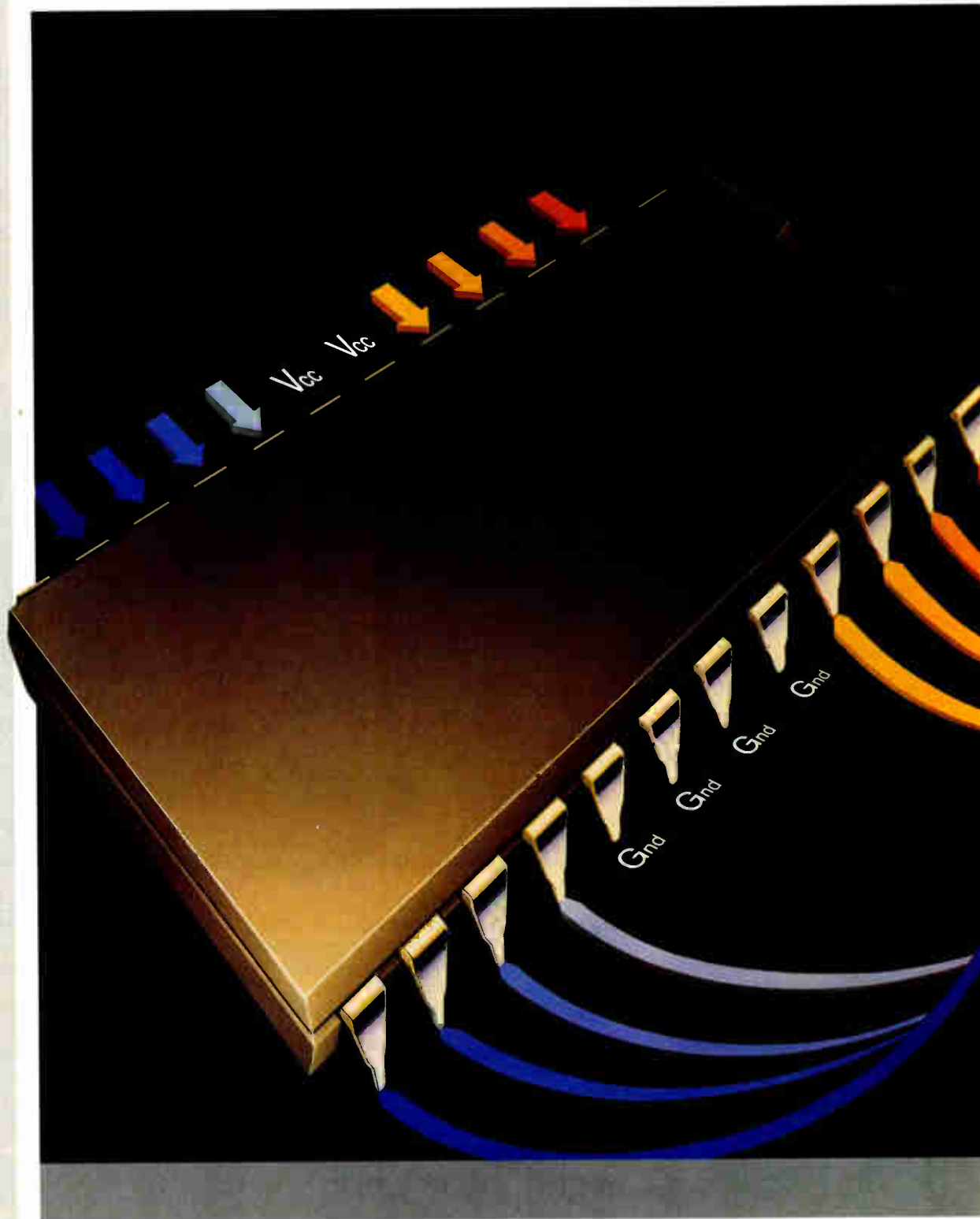
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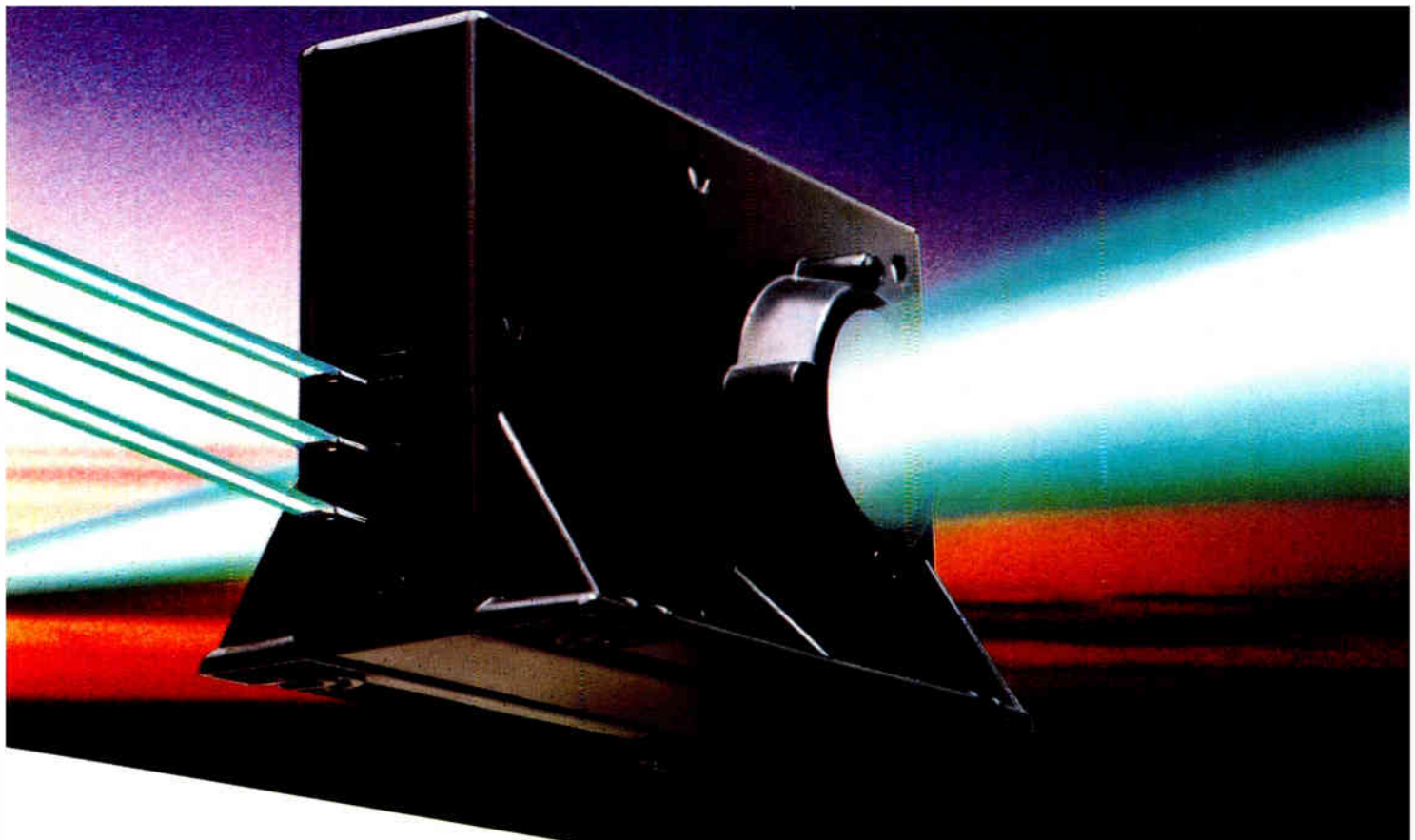
### **For Advanced CMOS Logic, the name is Signetics.**

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# PHILIPS



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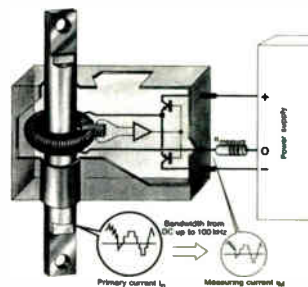
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# WASHINGTON NEWSLETTER

## THE FCC WON'T ALLOCATE NEW SPECTRUM FOR ADVANCED TV BROADCASTS . . .

**T**he Federal Communications Commission took its first steps toward setting a broadcast standard for advanced—or high-definition—TV in September. In announcing that no new spectrum will be given to broadcasters and requiring that any new systems be compatible with existing NTSC standards, the ruling leaves three possible routes to ATV, says William Hassinger, assistant engineering chief in the FCC's Mass Media Bureau. Broadcasters can add data to their current 6-MHz signal in such a way that current TV receivers would not be disturbed, while advanced TVs would benefit; supplement the existing 6-MHz signal with either a 3- or 6-MHz expansion so that the NTSC signal is carried in the original spectrum, while the new spectrum is used to transmit the ATV enhancements; or broadcast NTSC signals on one 6-MHz station, while transmitting a separate ATV signal on another 6-MHz channel. The ruling boosted the NTSC-compatible schemes being considered by the FCC's Advisory Committee on Advanced Television Systems. But it sounds the death knell for the system Japan is using over a nationwide satellite network, MUSE, which needs a minimum bandwidth of 8.1 MHz. "The implication is that if your system is incompatible and requires more than 6 MHz, we won't use it," says Hassinger. □

## . . . AND THE AEA SEEKS FEDERAL AID FOR A U. S. ATV CONSORTIUM

**W**hile the Federal Communications Commission wrestles with issues involving advanced TV systems, the American Electronics Association is cranking up efforts to restore U. S. competitiveness in consumer electronics. The AEA sees ATV as both a vehicle for the U. S. electronics industry to reenter the consumer arena and a crucial opportunity to protect other industry segments—personal computers, semiconductors, and communications equipment—from domination by foreign competitors. The AEA would like government help in setting up either a consortium on the order of Sematech, the industry-government effort to develop U. S. chip-fabrication know-how, or a limited partnership among electronics companies that would develop and license TV-making technology. "But it's going to take time, and money," says Pat Hill Hubbard, the AEA's vice president for technology policy. She reckons it will be at least eight years before anyone sees a return on investment from what will likely be a multibillion-dollar project. □

## SHOULD DOD MAKE CONTRACTORS GUARANTEE ETHICAL BEHAVIOR?

**D**efense contractors are up in arms over interim Pentagon regulations that not only require contractors under investigation to certify the integrity and ethics of their businesses and employees, but also give the DOD authority to recapture profits it deems were earned with the help of illegally obtained inside information. What the DOD is asking for, in effect, is a money-back guarantee that contractors will stick to the strictest interpretation of the law. The rule, which took effect July 29, is termed "interim," but has no expiration date, and contractors fear that it could be extended to include all defense contractors. The Council of Defense and Space Industry Associations worries that the measure holds "substantial implications for the defense industry as a whole" if that happens. In a September letter to Deputy Assistant Secretary of Defense for Procurement Eleanor R. Spector, the council decried the interim rules as "administratively unworkable" and charged that they "fail to ensure due process." Executive branch personnel, the council says, will have too much leeway in determining what sorts of communications between contracting offices and prospective bidders are—and are not—allowed, for example. The council and some members of Congress want the measure withdrawn, but the Pentagon is not likely to do so soon. □

# WASHINGTON NEWSLETTER

## THE PENTAGON PRESSES FORWARD WITH 'PAPERLESS' PROCUREMENT

**T**he Pentagon is putting new teeth into its requirement that military contractors begin moving toward "paperless" documentation. Beginning this month, solicitations for new weapons systems will require bidders to provide specific schedule and cost proposals on how they plan to comply with CALS, the Defense Department's multibillion-dollar initiative in Computer-aided Acquisition and Logistics Support [*Electronics*, Nov. 12, 1987, p. 45]. CALS calls out standards and protocols for electronic data interchange. The goal is to have a common digital interface for intelligent, interactive exchange of technical data between DOD and contractor databases starting in the early 1990s. A core set of CALS standards was published late last year, with a second set of protocols due for release in December. Contractors can get the lowdown on the latest CALS requirements and the program's future direction at a special session scheduled at Autofact '88 in Chicago Oct. 31-Nov. 2. □

## AN UPSTART BEATS THE BIG GUNS TO WIN A KEY SDI SIMULATION CONTRACT

**W**ith in-flight testing looming as both expensive and a potential violation of treaties with the Soviet Union, simulation will be the key to developing and testing technology for the Strategic Defense Initiative. And in a key \$5.1 million contract battle to develop a facility for simulating incoming ballistic missiles and testing potential sensors, Aura Systems Inc., a Los Angeles startup, has beaten out three heavyweight rivals—TRW, GMHE/Hughes Aircraft, and Rockwell International. Aura will integrate its infrared scene projector with a three-axis flight motion simulator into an environmental conditioning chamber at Eglin Air Force Base, Fla. The chamber is so large—25 by 25 by 10 ft—it can hold a full-sized interceptor missile. Aura's laser-driven projection hardware offers frame rates 10 times faster than the prevailing 100-Hz standard and a dynamic range over 1,000 times wider than that of commonly used systems. □

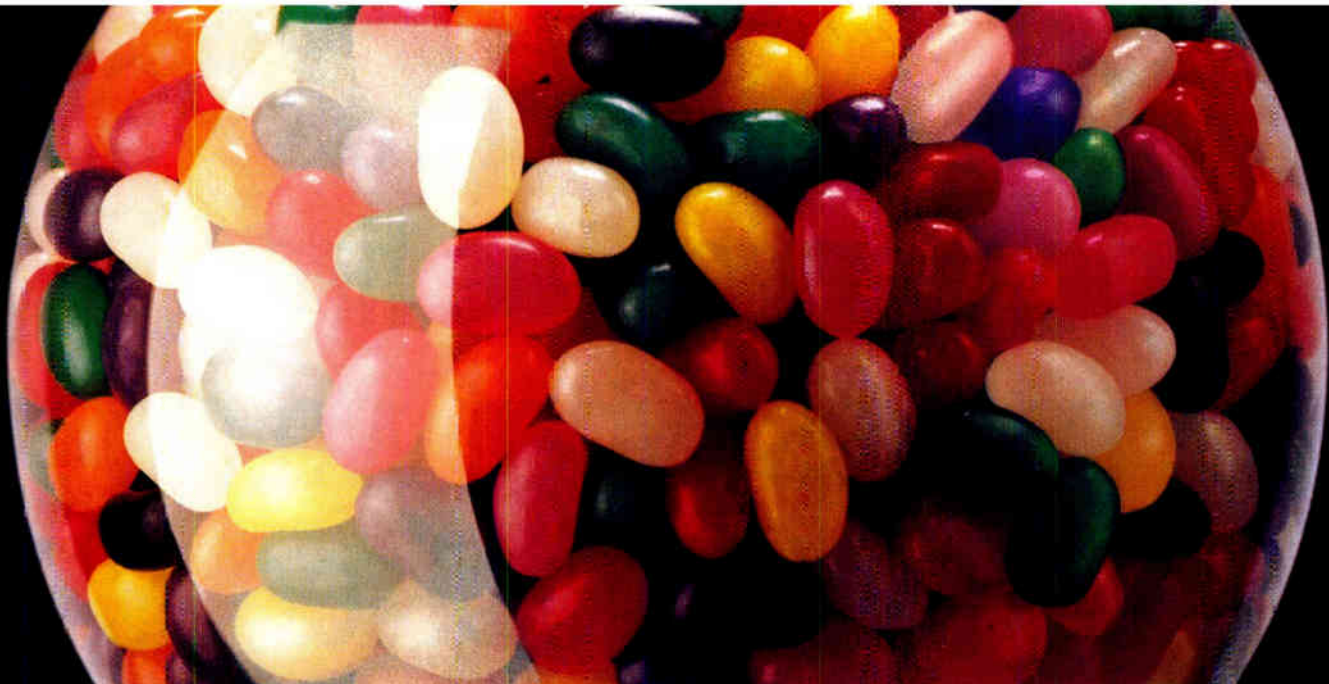
## PENTAGON BUDGETS WILL STAY FLAT, BUT DEMAND WILL RISE FOR MILITARY CHIPS

**P**entagon budgets will be lucky to keep pace with inflation in the early 1990s, analysts say, so defense-electronics growth will be slim. But the rising use of training and simulation systems, coupled with an increased reliance on system upgrades—as opposed to all-new systems—will keep the military chip market growing at a healthy 9.8% through 1992, predicts market researcher Frost & Sullivan Inc. in New York. Demand for bipolar chips will rise slowly from \$800 million in 1987 to \$890 million in '92, but MOS technologies, including CMOS and biCMOS, will jump by 50% in the same period, from \$794 million to almost \$1.2 billion. Other hot markets include application-specific integrated circuits, optoelectronic and microwave-discrete chips, and radiation-hardened chips for space applications. □

## WHAT THE U. S. NEEDS TO BECOME COMPETITIVE AGAIN

**R**eports on competitiveness and high technology in the U. S. seem to come out almost weekly, these days but a new study by the Council on Competitiveness, offers a road map to recovery that may be more navigable than most. *Picking Up the Pace: The Commercial Challenge To American Innovation* names reducing the federal budget deficit as the No. 1 priority for the next president. But just as important, the council says, is a long-term strategy, formed by a more powerful White House science and technology adviser, that would include two-year budget authority for R&D items; permanent tax credits for R&D; encouragement and assistance for cooperative R&D initiatives; and more federal support for science and technical education. □





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naturally, exceptional customer service is essential to their success. That philosophy can only be good for Adaptec's product offerings and ultimately, our customers. Congratulations IMP! You more than met our strictest requirements and have made life at Adaptec a lot easier. Congratulations to the runner-ups for *Vendor of the Year* as well—Motorola, Eric Electronics, and Arrow/Kierulff. With partners like you, we can continue to produce the industry's best I/O solutions.

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World Radio History

# PACIFIC RIM TRENDS

## IBM JAPAN ATTACKS THE OS/2 APPLICATION SHORTAGE WITH A PORTING STRATEGY

In what could be a precursor to IBM Corp.'s next marketing strategy to boost sales of the high-end models of its Personal System/2, IBM Japan Ltd. has embarked on a program to convert software that normally runs on larger office computers, such as its System 36, to the PS/2 Model 55. Sales of the 32-bit PCs have lagged because of the absence of applications programs that run under its powerful OS/2 operating system. Only 20% of IBM Japan's Model 55 computers that have been sold so far use OS/2, and that holds down overall sales because OS/2 is needed to exploit the PS/2's power. Besides its own efforts, the Tokyo-based subsidiary will also enlist help from outside. Ricoh Ltd., Tokyo, which has been selling private-label versions of the Model 55 as its own product, has already adapted to the machine many application software packages originally developed for office computers. Almost all the Model 55s marketed by Ricoh almost all incorporate OS/2. □

## FUJITSU LAYS CLAIM TO THE FIRST BICMOS PROM

The high-speed/low-power combination of biCMOS technology is now available for the first time in programmable read-only-memories. Fujitsu Ltd.'s 128-Kbit PROM offers a 30-ns access time by retaining bipolar memory cells but replacing power-hungry peripheral circuits, including decoder circuits, with biCMOS. The MB71C46 has a typical power consumption of 200 mW and maximum power consumption of only 315 mW, compared with the 1-W maximum power consumption of the firm's 64-Kbit MB7144, its highest capacity bipolar PROM. Typical power consumption is 200 mW. Speed goals are achieved by using bipolar sense amplifiers that are designed to amplify and read small signals and by an improved bipolar process. The Tokyo-based company expects its PROM to be used in computers, communications equipment, test and measuring equipment, and control equipment for applications including logic-circuit replacement, code converters, and microprogramming stores. Production is scheduled for 10,000-unit volumes a month beginning in early 1989. □

## NEC RESEARCHERS UNRAVEL A STUBBORN PARTICLE-CONTAMINATION PROBLEM

Particle-contamination problems in vacuum processes for such technologies as metal evaporation and silicon molecular-beam epitaxy may have been solved, and as a result there could be a big yield increase in store for highly integrated devices. Researchers at NEC Corp.'s Fundamental Research Laboratories in Kawasaki found the contaminants—polysilicon granules ranging in size from 1 to 10  $\mu\text{m}$  that stick to substrates and prevent epitaxial silicon from growing—mostly carry a negative charge. Since silicon molecules are almost all uncharged, positioning a deflecting electrode with a negative voltage in excess of 6 kV or a positive voltage of more than 4 kV eliminated all the silicon particles, without affecting the rate of silicon epitaxial-layer growth. □

## JAPAN'S ELECTRONICS OUTPUT TO TOP \$7.4 BILLION IN 1988

With integrated circuits' 34% growth leading the way, Japan's electronics industry has rebounded from 1987's slump and is heading for its biggest year ever by turning out products valued in excess of 20 trillion yen—about \$7.4 billion. Electronics production overall—including ICs, industrial, and consumer markets—will be 14.8% greater than last year, says the Electronics Industries Association of Japan. Consumer-electronics output is projected to be up 6.2%, and industrial electronics should turn in a 17.4% rise in 1988. Electronic components output should climb by 16.5%. The EIAJ's projections are based on its recently released market analysis of 1988's first half. □



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DEVICE*	ORGANIZATION	ACCESS TIME	AVAILABILITY
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LH52251	256k x 1	35 ns/45 ns/55 ns	3Q 1988
LH52256	32k x 8	70 ns/90 ns/120 ns	Immediate
LH5261	64k x 1	25 ns/35 ns	1Q 1989
LH5262	16k x 4	25 ns/35 ns	4Q 1988

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# EUROPEAN OBSERVER

## PHILIPS SETS A 1.2-MICRON PROCESS FOR ITS STATIC RAMs

Philips of the Netherlands has signaled its commitment to remaining a player in the high-performance static random-access-memory market with the release of two fast 1.2- $\mu\text{m}$  64-Kbit CMOS SRAMs. Boasting power consumption as low as 100  $\mu\text{A}$  in standby—low enough for battery-only operation—the FCB61C61 and FCB61C62 are fully pin- and performance-compatible with industry-standard 64-Kbit SRAMs. Available with access times of 35, 45, and 55 ns, they target applications where speed, power consumption, and ease of use are critical. Mainframes and minicomputers, as well as telecommunications gear and signal processing, are all possibilities. The FCB61C61 has 64-K-by-1-bit organization and the FCB61C62 16-K by 4 bits. □

## IT'S A SIX-WAY RACE FOR SECOND-GENERATION UK MOBILE PHONES

Six British mobile-communications companies are off and running in the race for the estimated three million UK customers expected to purchase second-generation digital telephones. The second-generation system uses digital multiplexed signals in lieu of analog technology. The six companies—British Telecom plc, Ferranti Creditphone Ltd., GPT Ltd., Orbitel Ltd., Shaye Communications Ltd., and STC plc,—will compete for four operator licenses to be issued by the British Department of Trade and Industry. Head-on competition had been held up for six months by the DTI, which told the companies they had to agree on common radio-interface and signaling protocols so that their hardware would be compatible. Now the companies are looking across the channel for larger markets. "It puts British manufacturers in a position to establish a de facto European standard," says Bill Jeffrey, managing director of Shaye Communications. □

## PC BOARD MARKETS ARE GROWING AT A 10% CLIP

Look for the worldwide pc board market to grow at a rate of 10% per year despite a decline in the number of boards used per system. The seeming anomaly will come about through increased use of surface-mount technologies and more complex design methodologies, says a study released by organizers of the Electronica Components show to be held in Munich Nov. 8-12. Last year, 7,000 producers turned out some \$14 billion worth of pc boards, with U. S. companies accounting for one-third and Japanese firms for 28% of output. West Germany was third with 7.7%, which is more than the production of the UK, France and Italy combined. But Electronica's research concludes that high labor rates in West Germany will force more and more of its 300 to 400 firms to shift production to Taiwan and Korea. □

## ALBANIA OPENS IMPORT DOOR TO WESTERN ELECTRONICS FIRMS

By sealing a deal for television equipment with Philips of the Netherlands, Albania is taking the first steps toward importing electronics products from nations outside the Communist bloc. The small Balkan nation is ending its self-imposed economic isolation, say observers, because it needs electronics hardware—particularly a national television system—to spur education and industrialization. But prospective trade partners should not expect to see hard cash from Albania. Its 10-year trade agreement with Philips, for example, is a barter deal in which Albania will receive television parts and circuits as well as related measuring equipment in return for tobacco and cement. Later Philips will deliver color TV kits for assembly into complete receivers in Albania, as well as lighting and studio equipment for TV broadcasts. The exact amount and type of electronics equipment that the Albanians will receive for the \$1.5 million in commodity goods remains to be negotiated. □

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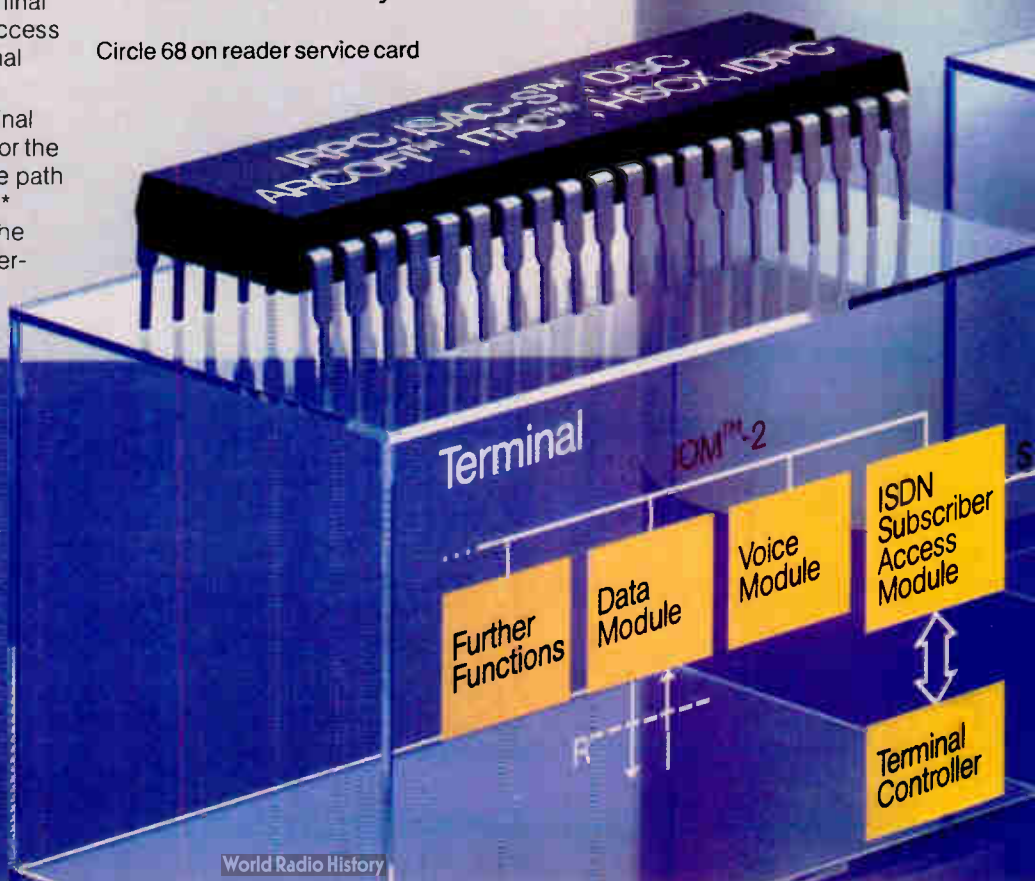
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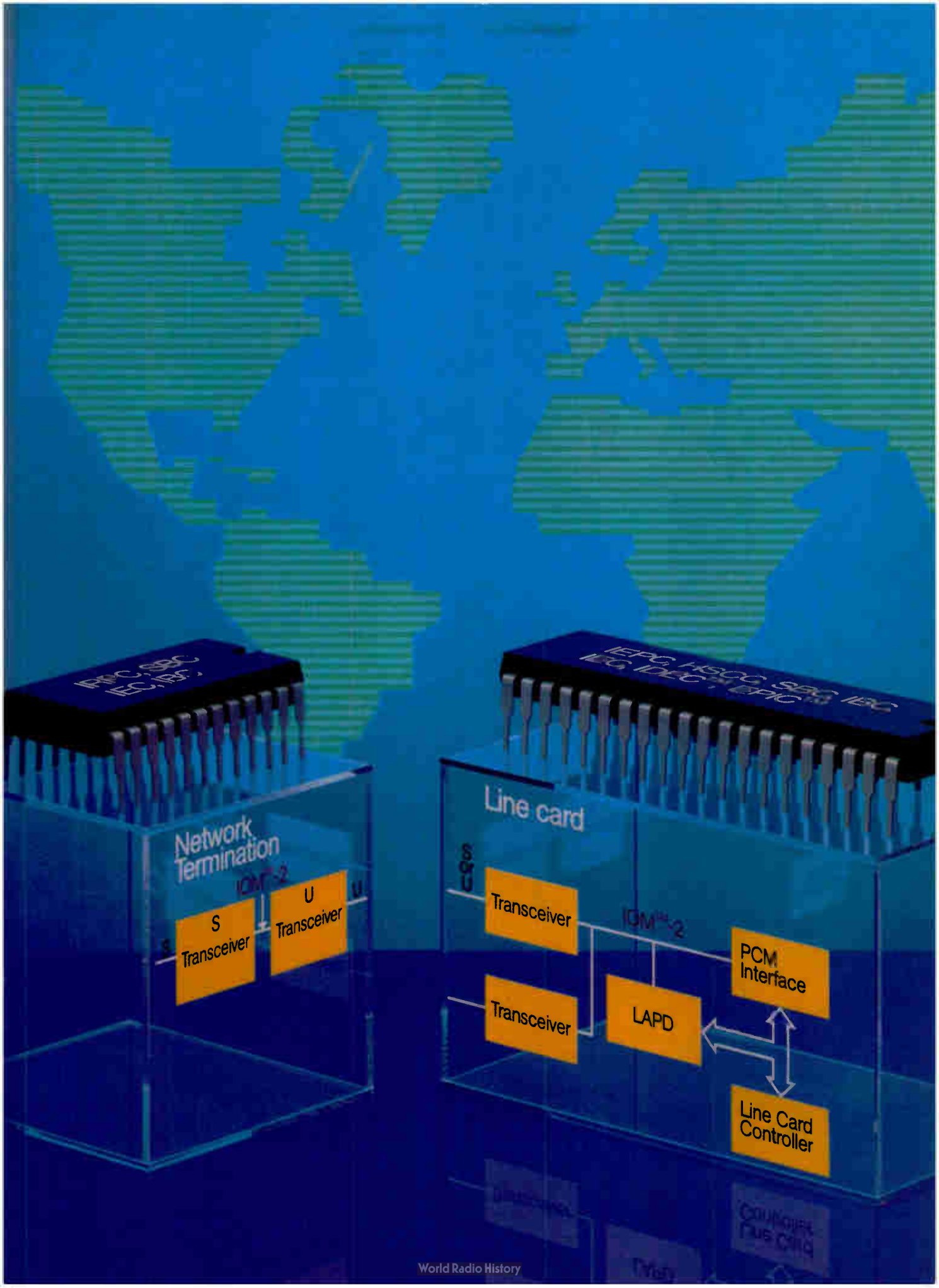
### TopTech Components from Siemens: the key to digital communication systems

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1EPC, 150C  
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1EG, 150C, 1EPC

Network Termination

Line card

S  
U  
S Transceiver  
U Transceiver

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Transceiver  
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# TECHNOLOGY OUTLOOK

1989

**T**he electronics industry's relentless push for higher speed is in high gear, driving nearly all technology segments on a fast and often tricky course as the 1980s race to a close. The new emphasis on speed has its roots in computer markets, where equipment manufacturers have turned to higher performance as the most profitable way for differentiating their products from the competition. While speed reigns as the leading force in moving technology, advances will continue on three other historical fronts—the interwoven areas of making systems cheaper, better, and smaller.

But like falling dominoes, the

system-speed push has come to shove many linked technology advances towards higher performance. Many of these advances are likely to debut next year.

On the system scene, look for a sudden growth in parallel processing, as a new wave of equipment makers make the move into concurrent computing architectures. Part of the trend will result from new compilers and development software. With more power on tap—via multiple processors or ever faster single-processor technologies—graphics-intensive visual computing will appear in new mainstream market applications.

Speed demands are also driving

A NEW PUSH

S

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developments in peripherals, from smaller disks to fast laser printers. In communications, major advances will be achieved in the integration of voice and data, optical-fiber transmission systems, interoperability software links, and network management.


Speed is also the watchword for 1989 in the semiconductor industry, where chip makers are now pushing memory and peripheral logic technology to keep up with the fast 32-bit microprocessors appearing in 1988. To do that, chip production technologies will move well below 1 micron. To get parts out faster, many IC makers will turn to new minifabs.

The speed accent is reaching down to the component level and is reshaping new chip-packaging technologies. And it is changing the computer-aided-design world, providing more-powerful work stations to run software that tackles the design of faster circuits.


In industrial circles, reduced-instruction-set-computing will boost the speed and precision of robotic muscle. And for consumers, new technology is emerging that could start a new market for portable "personal video" via the marriage of liquid-crystal-displays and miniaturized VCRs.

**FOR**

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# THE PUSH FOR SPEED SPURS WORK ON PARALLEL SYSTEMS

**A**dvances in the fast lane of computer technology will be the leading trend in systems during the coming year, and that means parallel processing should get a major shot in the arm. More equipment houses will be making the move to parallel architectures to break speed bottlenecks. Together, parallel computing and the never-ending emphasis on faster component technology for more conventional single-processor systems will continue to squeeze equipment life cycles ever shorter in 1989 as manufacturers try to top each other.

With new advances in more powerful systems, an emerging new form of information processing—called visual computing—is expected to make a move into the mainstream of applications after years of incubation in such niches as mechanical design and molecular chemistry markets. The movement will take the form of photorealistic three-dimensional graphics, visualization programs to display what the human eye can not see, and image processing. Related to the visual-computing trend, rapid advances are ahead in the proliferation of graphical user interfaces or windowing systems into nearly all corners of the market.

New computer architectures, such as reduced-instruction-set computers, will continue growth launched over the past year, causing dramatic changes in tomorrow's computing landscape. Hardware advances in personal computers will set the stage for desktop units with mainframe muscle, but the continuing lag in available system and application software will keep most new PCs relegated to their traditional work roles in the office and home. New software, however, will begin to put an end to that frustrating situation next year.

**FROM THE LABS.** Also in 1989, look for expert-system technology to at last take on more of an important role in data-processing applications, and watch for neural-network technology to make its first steps from the laboratory towards use in commercial products. And with the search for faster computing systems, the industry is expected to increase its drive for a complete operating environment that touches all corners of high-performance processing. The immediate hope is to have the pieces for that harmonious environment—such as local-area networks, work stations,

## COMING SOON

- The move of parallel processing into the mainstream of high-performance computers as more compilers and software-development tools become increasingly available
- Widespread visualization applications for seeing the unseeable made possible by growth in the power of computer graphics processing
- A beginning to the end of the frustrating lack of software that will put the mainframe-magnitude power of new personal computers finally into play
- The first steps of neural-network architectures out of the lab and into roles in commercial products

graphic systems, user interfaces, and visualization applications—resting upon an industry-standard operating system: a version of AT&T's Unix, according to most experts in the industry today.

Clearly, the underlying computer theme of 1989 will be speed. And to that end, more systems vendors and users are thinking about and will soon start using parallel-computer architectures to reach not only higher performance but performance at a lower price with the ability to upgrade in modular additions. Massively-parallel architectures, where thousands of small processors work together on a single problem, will begin to move into wider use. Development software for building applications that make efficient use of parallel hardware designs will be one of the biggest challenges and business opportunities next year.

But around the computer-equipment world, officials are agreeing that parallel processing is coming of age. Each year more systems are launched with multiple processors. And software development for parallel processing is moving full speed ahead. In fact, Electronic Trend Publica-




Photorealistic 3-d computer graphics images are becoming an important part of design automation systems, like this rendering of an auto design done on a HP work station.

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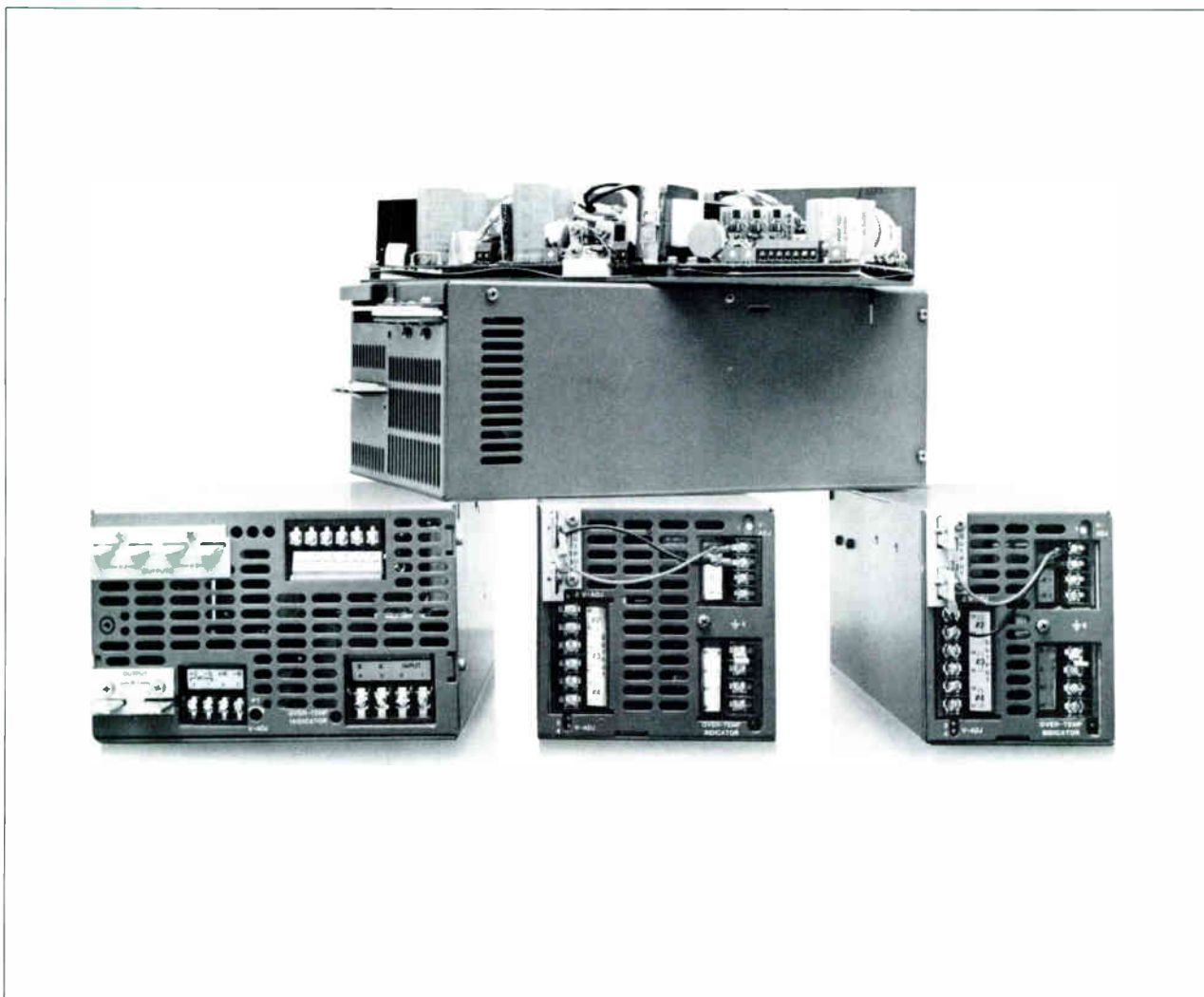


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				40°C	50°C	60°C	40°C	50°C	60°C			QTY. 1	QTY. 250	QTY. 1000
LFQ-26	1	5V ± 5%	5	325	276	227	50.00	42.00	34.00	26	2.5 × 4.75 × 13	\$ 450	\$375	\$325
	2	11.4-15.75	12				6.00	5.10	4.20					
			15				4.80	4.10	3.40					
	3	11.4-15.75	12				6.00	5.10	4.20					
LFQ-26-1	1	5V ± 5%	5	325	276	227	50.00	42.00	34.00	26	2.5 × 4.75 × 13	450	375	325
	2	11.4-15.75	12				6.00	5.10	4.20					
			15				4.80	4.10	3.40					
	3	11.4-15.75	12				6.00	5.10	4.20					
LFQ-27	1	5V ± 5%	5	475	420	362	75.00	66.00	57.00	27	4.0 × 4.875 × 11	570	485	435
	2	11.4-15.75	12				9.00	7.90	6.90					
			15				7.20	6.40	5.50					
	3	11.4-15.75	12				9.00	7.90	6.90					
LFQ-27-1	1	5V ± 5%	5	475	420	362	75.00	66.00	57.00	27	4.0 × 4.875 × 11	570	485	435
	2	11.4-15.75	12				9.00	7.90	6.90					
			15				7.20	6.40	5.50					
	3	11.4-15.75	12				9.00	7.90	6.90					
LFQ-28	1	5V ± 5%	5	635	578	502	100.00	91.00	79.00	28	5.0 × 4.875 × 11	675	575	510
	2	11.4-15.75	12				12.00	10.80	9.50					
			15				9.60	8.60	7.60					
	3	11.4-15.75	12				12.00	10.80	9.50					
LFQ-28-1	1	5V ± 5%	5	635	420	362	100.00	91.00	79.00	28	5.0 × 4.875 × 11	675	575	510
	2	11.4-15.75	12				12.00	10.80	9.50					
			15				9.60	8.60	7.60					
	3	11.4-15.75	12				12.00	10.80	9.50					
LFQ-29	1	5V ± 5%	5	920	830	700	150.00	130.00	105.00	29	7.75 × 4.875 × 11.5	840	710	635
	2	11.4-15.75	12				18.00	15.70	12.60					
			15				14.40	12.50	10.00					
	3	11.4-15.75	12				18.00	15.70	12.60					
LFQ-29-1	1	5V ± 5%	5	920	830	700	150.00	130.00	105.00	29	7.75 × 4.875 × 11.5	840	710	635
	2	11.4-15.75	12				18.00	15.70	12.60					
			15				14.40	12.50	10.00					
	3	11.4-15.75	12				18.00	15.70	12.60					
LFQ-30	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
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	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
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LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.40	14.00					
			15				16.00	13.90	11.20					
	3	11.4-15.75	12				20.00	17.40	14.00					
LFQ-30-1	1	5V ± 5%	5	1200	1050	850	170.00	148.00	120.00	30	7.75 × 4.875 × 11.5	1000	835	750
	2	11.4-15.75	12				20.00	17.4						

# LFQ SERIES

# Specifications

## DC OUTPUT

Voltage range shown in tables.

## REGULATED VOLTAGE

regulation, line	0.1% for line variations from 187 to 265VAC and from 95 to 132VAC. On LFQ-29, 30, 0.1% for line variations from 85 to 132VAC and from 170 to 265VAC.
regulation, load	0.1% for load variations from 0 to full load for main output; 0.2% for fourth output (5V) of LFQ-26-1, LFQ-27-1, LFQ-28-1; 1% for 12V/15V outputs*; 2% for 24V/28V outputs*; (*5V outputs require a preload of 12.5A on LFQ-26, 19.0A on LFQ-27, 25.5A on LFQ-28 for full power on other outputs, and 4.0A on output #2 of LFQ-29, 30 for max power out on outputs 3 and 4. Output #2 must be greater than or equal to output #3). 0.2% for second 5V output of LFQ-29-1, 30-1.
ripple and noise	15mV RMS, 100mV pk-pk for 5V outputs. 25mV RMS, 150mV pk-pk for 12V/15V outputs. 25mV RMS, 250mV pk-pk for 24V/28V outputs.
cross regulation	5V outputs: 0.1% max for load variations on auxiliary outputs from no load to full load; Auxiliary outputs: 0.1% max for load variations on 5V output from preload to full load current.
remote programming resistance	1000 $\Omega$ /V nominal (main output and output 1, 2, 3 on LFQ-29, 29-1, 30, 30-1).
remote programming voltage	volt per volt.
temperature coefficient	0.3%/°C.

## AC INPUT (User selectable)

line	95 to 132VAC/187-265VAC, 47-440Hz. 85 to 132VAC 170 to 265VAC on LFQ-29, 29-1, 30, 30-1.
power	LFQ-26, 26-1: 434 watts maximum. LFQ-27, 27-1: 633 watts maximum. LFQ-28, 28-1: 880 watts maximum. LFQ-29, 29-1: 1310 watts maximum. LFQ-30, 30-1: 1710 watts maximum.
RMS current	LFQ-26, 26-1: 7.0A RMS maximum. LFQ-27, 27-1: 11.0A RMS maximum. LFQ-28, 28-1: 15.0A RMS maximum. LFQ-29, 29-1: 20.0A RMS maximum. LFQ-30, 30-1: 26.0A RMS maximum.

## EFFICIENCY

75% minimum on LFQ-26, 26-1, 27, 27-1. 72% minimum on LFQ-28, 28-1. 70% minimum on LFQ-29, 29-1, 30, 30-1.

## DC INPUT

260 to 370VDC. (Units must be configured for 220V input.) 250-370VDC on LFQ-29, 29-1, 30, 30-1.

## OVERSHOOT

No overshoot at turn-on, turn-off or power failure.

## STORAGE TEMPERATURE RANGE

-55°C to +85°C.

## AMBIENT OPERATING TEMPERATURE

Continuous duty 0° to 60°C with suitable derating above 40°C. Guaranteed turn-on at -10°C with reduced specifications.

## OVERLOAD PROTECTION

### ELECTRICAL

External overload protection. Automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

## HOLD UP TIME

All outputs will remain within regulation limits for at least 16.7 msec after loss of AC power when operating at maximum output power and 105VAC input at 60Hz. (When configured at 220V input: 20 msec holdup when operating at maximum output power and 210VAC input at 50Hz.)

## IN-RUSH CURRENT LIMITING

The turn-on in-rush current will not exceed 40 amps peak on LFQ-26, 26-1. (75 amps peak on LFQ-27, 27-1, 28, 28-1, 29, 29-1, 30, 30-1.)

## OVERVOLTAGE PROTECTION

5V outputs only. If output voltage exceeds a preset value, inverter drive is removed.

## COOLING

The LFQ-26, 26-1 are convection cooled. The LFQ-27, 27-1, 28, 28-1, 29, 29-1, 30, 30-1 are fan cooled. A fan failure circuit will shut down the inverter in the event of fan failure or interference of fan rotation. AC input power must be momentarily interrupted to reduce output after fault condition is corrected.

## LED INDICATOR

An LED fan failure indicator will illuminate in the event of fan failure or interference of fan rotation.

## DC OUTPUT CONTROLS

Simple screwdriver adjustment over entire voltage range.

## INPUT AND OUTPUT CONNECTIONS

PC Board mounted barrier strip: AC input, 5V DC sensing and remote turn-on/turn-off of LFQ-27, 27-1, 28, 28-1; AC input, remote turn-on/turn-off, DC sensing outputs 1, 2, 3 of LFQ-29, 29-1, 30, 30-1. DC output 4 of LFQ-29, 29-1, 30, 30-1; Auxiliary outputs of LFQ-27, 27-1, 28, 28-1.

PC Board mounted terminal block: AC input, 5VDC, sensing and remote turn-on/turn-off and auxiliary outputs of LFQ-26, 26-1. Chassis stud: all ground connections.

Bus Bars mounted on PC Board: 5VDC outputs of LFQ-26, 26-1, 27, 27-1, 28, 28-1; DC outputs 1, 2, 3 of LFQ-29, 29-1, 30, 30-1.

## MOUNTING

Two mounting surfaces and two mounting positions on LFQ-26, 26-1. LFQ-27, 27-1, 28, 28-1, 29, 29-1, 30, 30-1 have one mounting surface. Forced air cooling will allow multiple mounting positions.

## REMOTE TURN-ON/TURN-OFF

TLT compatible signal enables remote turn-on/turn-off of the power supply. A voltage of 2.8V to 5.0V applied to remote on/off terminals will initiate turn-off. Open circuit or short circuit condition, or a zero to 0.5V signal will cause turn-on.

## REMOTE SENSING

Provision is made for remote sensing to eliminate the effects of power output lead resistance on DC regulation. (5V outputs only of LFQ-26, 26-1, 27, 27-1, 28, 28-1 and outputs 1, 2, 3 of LFQ-29, 29-1, 30, 30-1.)

## ISOLATION RATING

3750V RMS input to output, (8mm spacing).

## EMI

Conducted EMI conforms to FCC Docket 20780 Class A and VDE 0871 Class A above 150 kHz.

## PHYSICAL DATA

Package Model	Weight		Size (in.)
	Lb. Net	Lb. Ship	
LFQ-26, 26-1	6	7	2.5 × 4.75 × 13
LFQ-27, 27-1	12	14	4.0 × 4.875 × 11
LFQ-28, 28-1	13	15	5.0 × 4.875 × 11
LFQ-29, 29-1, 30, 30-1	17	20	7.75 × 4.875 × 11.5

## FINISH

Grey, Fed. Std. 595, No. 26081

## GUARANTEED FOR 1 YEAR

One-year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of one year.

## UL/CSA/TUV/IEC

Under evaluation.

# The Five Best Reasons To Purchase A Lambda WATTBox



	ADVANTAGES	BENEFITS
1. WATTBOX CONCEPT	<ul style="list-style-type: none"> <li>• Wide range outputs</li> <li>• One power supply with multiple output configurations</li> <li>• Totally self-protected</li> <li>• High density</li> <li>• High reliability</li> </ul>	<ul style="list-style-type: none"> <li>• Stock availability</li> <li>• Ease of implementation in prototype design phase allowing for margins on each output</li> <li>• Reduced packaging costs</li> <li>• Reduced maintenance costs</li> </ul>
2. STATE-OF-THE-ART SMD MODULES (SURFACE MOUNTED DEVICE), ONE FOR PRIMARY, AND ONE FOR AUXILIARY REGULATION	<ul style="list-style-type: none"> <li>• Increased component efficiency</li> <li>• Reduced parts count</li> <li>• Ease of manufacturing</li> <li>• Economies of scale production efficiencies</li> <li>• Virtually independent regulation (less than 0.1% cross regulation)</li> </ul>	<ul style="list-style-type: none"> <li>• Fully regulated</li> <li>• Reduced packaging costs</li> <li>• Reduced system cost</li> <li>• Increased power supply reliability</li> <li>• Reduced size</li> </ul>
3. SINGLE ENDED CONFIGURATION FOR MAIN POWER SUPPLY SWITCHING NETWORK	<ul style="list-style-type: none"> <li>• Ease of design for 110/220 Volt input</li> <li>• Reduced parts count for drive control circuitry</li> <li>• Eliminates complicated circuitry associated with base driven switching power supplies</li> <li>• Increased switching frequency and lower switching losses</li> </ul>	<ul style="list-style-type: none"> <li>• Satisfies US and European end system designs</li> <li>• Reduced cost and improved reliability</li> <li>• Reduced size</li> </ul>
4. SYNERGETIC EFFECT OF HIGH FREQUENCY SWITCHING DESIGN AND MAG-AMP TECHNOLOGY	<ul style="list-style-type: none"> <li>• Inherent ruggedness associated with MAG-AMPS</li> <li>• Maximum density obtainable</li> <li>• Commonality through LF power supply family</li> </ul>	<ul style="list-style-type: none"> <li>• Improved reliability</li> <li>• Reduced system cost</li> </ul>
5. PROPRIETARY MAIN CONTROL IC (LAS 4082)	<ul style="list-style-type: none"> <li>• Provides a direct gate drive to the low voltage MOSFET device</li> <li>• Reduces the power supply parts count</li> </ul>	<ul style="list-style-type: none"> <li>• Lambda designed and produced to ensure maximum reliability, efficiency and availability</li> <li>• Reduced cost</li> </ul>

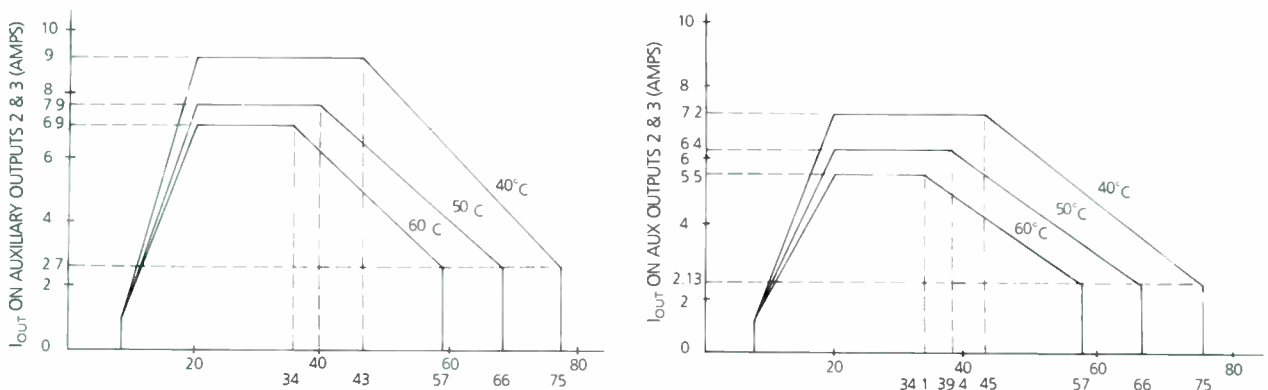
## MINIMUM LOAD REQUIRED

The minimum load specified for the LFQ Series is not required for reasons of cross regulation. Line and Load transients happen frequently in industrial applications throughout the world. This imposes the need for a wide variation in duty cycle and precise control under all circumstances, including the effects of power supply load variations. Minimum loading requirements are specified for the LFQ Series (shown for the main 5V output on single inverter designs employed in LFQ-26, 27 and 28, and output number 2 in LFQ-29 and 30 which use a double inverter approach). The minimum loading specified is required to ensure that the minimum duty cycle of the inverter does not fall below the design limit when maximum current is required from the dual auxiliary outputs. In the majority of applications, where the full rated output is not required from the auxiliaries, the minimum loading on the main output can be reduced. Figure 1 (a) and 1 (b) exemplify this option for LFQ-27. Similar data is provided with the operating instructions for all Lambda LFQ Series Models.

## OUTPUT CURRENT ON AUXILIARY OUTPUTS 2 AND 3 VERSUS 1 ON MAIN OUTPUT

(Auxiliary output 4 at maximum output current at appropriate ambient temperature as per TABLE I)

Figure 1. LFQ-27 Output Current Profile



(a) Auxiliary Outputs 2 and 3 Adjusted To 12V ± 5%

(b) Auxiliary Outputs 2 and 3 Adjusted To 15V ± 5%

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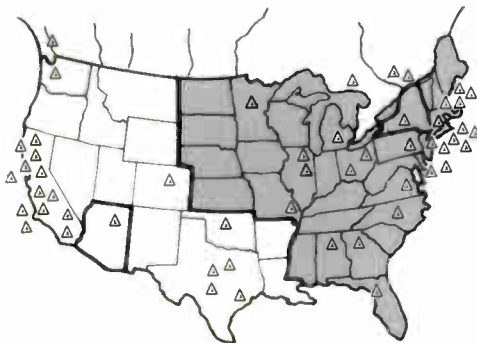
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tions of Saratoga, Calif., concludes that "parallel processing will impact every part of the computer industry within the next five years." In a recent report on parallel processing, the technology-market research firm says between 1986 and 1991 "parallel-processing architectures will grow quickly from being used in 22% of the total number of computer systems shipped to 48% of system shipments."

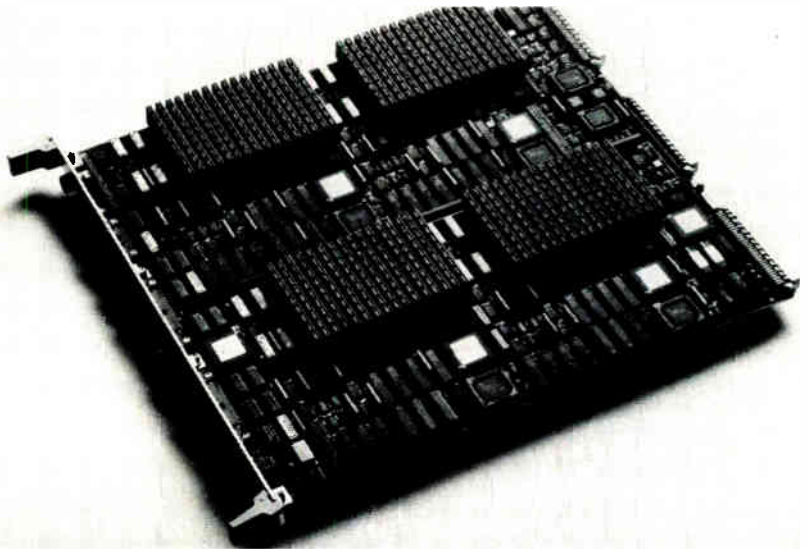
Before that can happen, there still are some significant technological problems for systems houses to solve, suggests William Avery, senior vice president of product development at Encore Computer Corp. in Marlboro, Mass. One of the biggest short-term challenges is finding innovative ways to build parallel-processing systems that can take advantage of the continuing improvements in micro-processor performance. Another challenge is to write algorithms for effective parallel processing, he adds.

Parallel processing is winning the endorsement of IBM Corp. for its biggest systems, especially those geared towards scientific and technical applications. But the Armonk, N. Y.-based computer giant also is planning for a wider impact. "I see more systems from work stations to supercomputers moving to parallel processing," says Allan H. Weis, vice president of the Data Systems Division in IBM Enterprise Systems operation. Weis has worldwide responsibility for the strategy, development, and technical support of large systems for engineering and scientific markets targeted by IBM.

**SOFTWARE FOCUS.** The move to parallel processing will continue to grow at a faster rate, says Weis, but "one of the problems is software—a major challenge is software that supports parallel architectures efficiently." Such software is beginning to emerge, however, and many more compilers for the most popular languages are expected to appear next year to restructure programs for parallel machines.

For the next 12 to 18 months, IBM will continue to enhance the software technologies to support its powerful hardware, such as the new top-of-the-line six-processor 3090 S Model 600 with up to a half dozen vector processors. It is using several hardware strategies to support high performance: vector and parallel processors, large memories, and fast parallel input/output channels. IBM and the other vendors of high-performance computers are developing software to efficiently use these resources in parallel.

Already, several versions of Fortran have been developed with extensions to support parallel processing. Expected to follow soon are extended versions of other popular languages, such as C, Ada, and Pascal. The Parallel Computing Forum, sponsored by equipment vendors promoting parallel architectures, is developing a standard for parallel Fortran.



**A parallel-processor board** from Topologix Inc. carries four transputers to accelerate floating-point math, thereby boosting work-station power eightfold.

"The extensions to Fortran that allow it to do parallel computing will be standardized," promises Scott Gibson, executive vice president and chief operating officer of Sequent Computer Systems Inc.

However, the greatest impact on the future may not hinge on Fortran, but rather the movement of C into the parallel-processing world. The powerful C language is quickly becoming the language of choice for technical computing, while

### The big news in languages for parallel processing likely will be a new version of C

Ada is a strong runner because of its endorsement by the Department of Defense. For that reason, efforts to create standards for Parallel C—and eventually a Parallel Ada—are not expected to lag far behind the Fortran effort.

"Students are graduating from universities knowing C, and some now don't know Fortran," notes IBM's Weis. "With the enormous base of Fortran software and growing popularity of C, my personal view is that a lot of new things are needed in C—for example, the need for an easy way for programs in C to call Fortran routines and vice versa. Future applications will have a mixture of languages."

Another challenge in parallel computing is creating new tools for debugging parallel software. "We will see a lot of parallel architecture in the future, but a lot of good tools will be needed to build applications along with debugging tools," says Weis. Both he and Sequent's Gibson say such parallel-program debugging tools will appear on the market in the next 18 months.

Another key software challenge is the development of algorithms and applica-

tions software that can take advantage of supercomputer architectures and parallel processing. "There are hundreds of applications out there that don't take into account newer architectures and supercomputer performance. Older programs that are simply ported forward don't do it, and that's a technical challenge for third-party developers and universities to tackle," says James R. Berrett, chairman and chief executive officer at Honeywell-NEC Supercomputers Inc. in Burlington, Mass.

Look also for scientific/technical applications to be written in new codes that are attuned to parallel processing, predicts Craig Mundie, vice president for business development at Alliant Computer Systems Corp. "We now have codes that were written long before [the advent of] parallel processing," he states. "But we've had a parallel vectorizing machine for three years now, and we'll begin to see new codes for such applications as mechanical and electrical CAD and computational chemistry."

**SPECIALIZED.** In 1989, the hottest field in parallel processing will be massively parallel architectures, where systems can have over 1,000 processors. Many of these massively parallel systems are specialized to an application or certain types of applications, compared to the general-purpose parallel computers with fewer than 1,000 processors. For example, a number of massively parallel machines feature single-instruction, multiple-data architecture, which is designed for data-parallel applications where a single instruction stream executes on multiple streams of data.

For now, the king of the mountain in data-parallel computers is Thinking Machines Inc.'s Connection Machine, which can be ordered with as many as 64,000 processors. The next in line is the 4,096-processor DAP 610 computer, just unveiled by Active Memory Technology Inc. The Ir-

vine, Calif. company also makes a low-cost desk-side massively parallel machine, the 1,024-processor DAP 510.

"We are beginning to see real acceptance of massively parallel computers as a valid technology," says M. Rodney Hornstein, president of Active Memory Technology. "The key is available software, but that is starting to appear." For example, the fruits of 150 man years of software effort are available for the DAP 500 and 600 series of machines, "and customers can use massively parallel computing here and now," he adds.

Useful as these massively parallel machines may be, says Alliant's Mundie, the dominant form of parallel processing for scientific applications is more likely to be vector-processing systems like those developed by his Littleton, Mass., super-computer firm. He argues that massively parallel machines, such as the Connection Machine and the DAP 610, "will become the array processors of the 1990s for [only] those applications that fit."

Massively parallel computers do, however, hold great promise because they can process certain types of applications much faster than any other computers. "There are interesting applications waiting for massively parallel computing, such as DNA sequencing," says Hornstein. DNA matching could be used for the ultimate finger-print identification system, and it has shown great promise in major areas of medical research, such as acquired immune deficiency syndrome and cancer. "In some of these areas, for example, our DAP 610 can reduce the computation to a few seconds on a work station from a few hours on a Cray," says Hornstein. "That is what massively parallel computing is all about—ultra-high performance for certain applications."

**LOOKING GOOD.** With the general growth in computer speed and power, many in the industry believe visualization software and photorealistic graphics will quickly spread from mechanical computer-aided design and molecular chemistry applications to the mainstream of the market. To many industry observers, image computing represents the next major evolution in information processing. "Visualization is essential for improving productivity and understanding data," says James Clark, founder and chairman of Silicon Graphics Inc., Mountain View, Calif.

"The role of graphics is becoming increasingly important in technical computing," says Alliant's Mundie. "That's because users want to visualize the results of their computations quickly rather than wait to work with long strings of numerical results." That's exactly why Alliant bought Raster Technologies Inc., a Westford, Mass., vendor of high-performance displays and display controllers. The two collaborated on what Alliant calls Visualization series, which debuted at August's

Siggraph conference. The systems use high-speed shared memory to link Alliant's FX parallel-processing supercomputers with Raster's 3-d displays.

"High-performance computing closely coupled with dynamic graphics used to be thought of only as a desktop [work-station] function," Mundie says. "But we believe that [network] servers can handle the combination of number crunching and graphics better because we can provide more megaflops."

In graphics, real-time performance will be a key issue in 1988, and here pixel-based graphic systems have the edge over geometry-based graphics systems. Geometry-

### Image computing may be the next major evolution in information processing

based graphics produce images through geometric calculations, and many vendors offer geometry graphics accelerators. Pixel-based graphics processes pixels and is used primarily to enhance and manipulate existing captured images.

"One of the big questions in geometry-based graphics today is how much can be done in real time," says Alvy Ray Smith, vice president of Pixar, the San Rafael, Calif., image computing company. In fact, most geometry graphics processing cannot be done in real time today. Pixel imaging accelerators, such as Pixar's, excel at real-time work, he asserts.

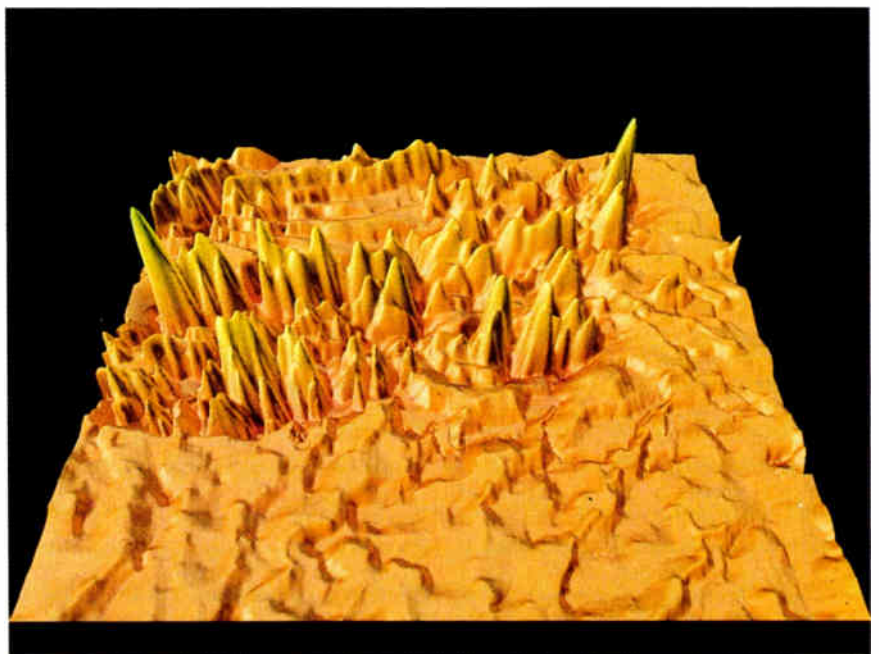
To help boost geometry-based graphics into the real-time mode, more graphics standards will arrive this year, such as the Programmers' Hierarchical Interac-

tive Graphics Standard (PHIGS) and PHIGS+. And Pixar is promoting a new standard for real-time photorealistic rendering of geometry-based images, RenderMan. "RenderMan will address all those things you can't do in real time today," says Smith.

Whatever else happens in computer hardware next year, it's safe to predict there'll be no truce in the recently launched war between reduced- and complex-instruction-set computers—it's expected to continue in full swing. "The first thing in computers—in the immediate future—is that the instruction-set battle between RISC and CISC will continue," promises Sequent's Gibson.

RISC wave has even swept into an old-line CISC house. "I foresee that systems such as our MV family with conventional CISC architecture continuing for decades for business and practical reasons," says Donald Lewine, senior technical consultant at Data General Corp. "A lot of good software runs on it, but that architecture won't be used for leading-edge machines. RISC architectures and Unix are important issues in both the near and long term." That's why the Westboro, Mass., minicomputer manufacturer has cast its lot in favor creating industry standards around both. For example, Data General is developing a family of RISC processors based on the Motorola Inc. 88000 CMOS microprocessor, and is also designing an ECL version of the 88000 under contract to Motorola.

Lewine says the big advantage in today's RISC machines stems from compiler improvements in the past several years. "Ten years ago, compilers were hard to write," he states. "They weren't very good, so designers worked hard to

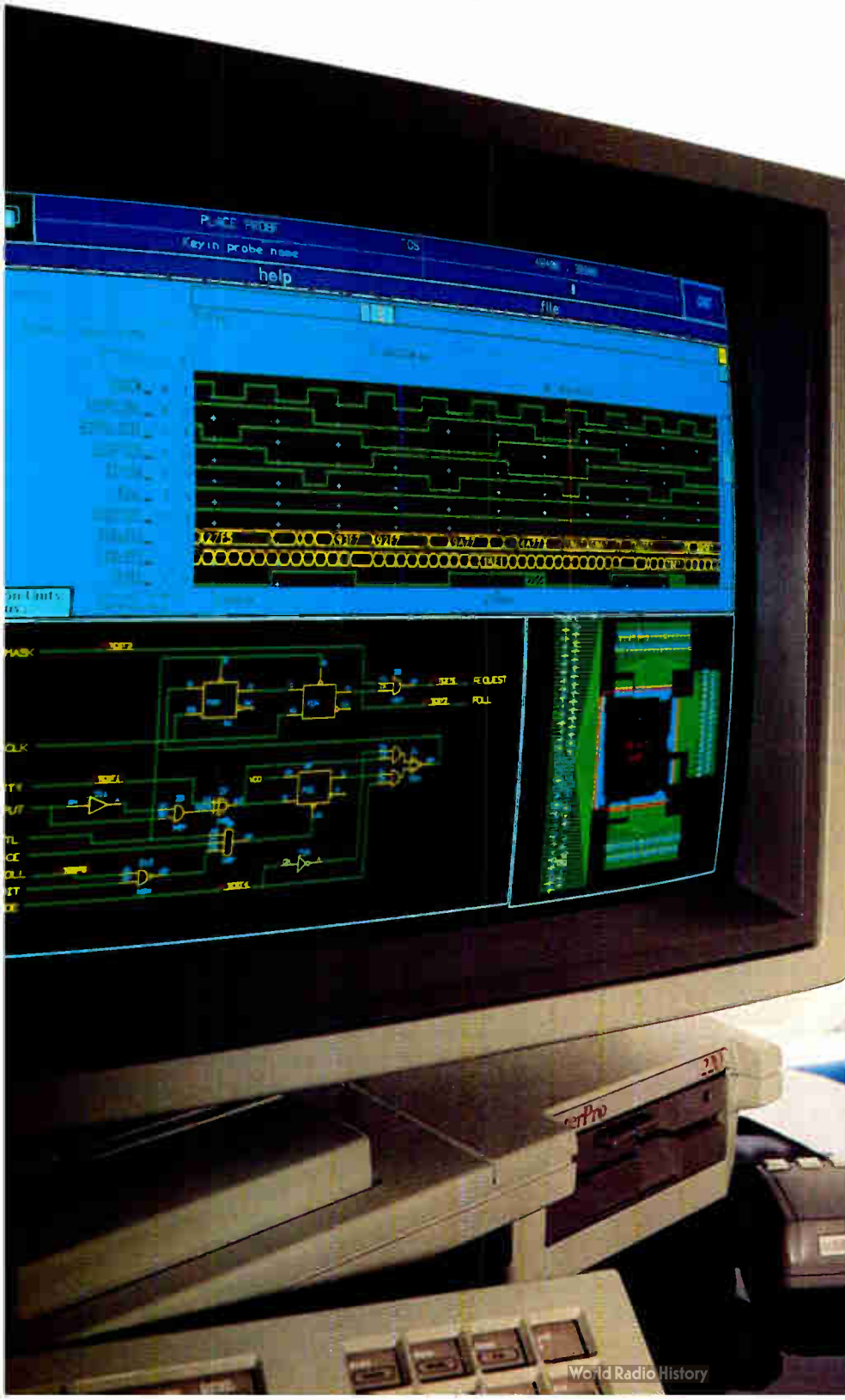


**An example of computer visualization**, this image of a section of Oklahoma shows the effect of terrain on local gravity anomalies. It was produced by a Pixar image computer.

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put as much into the instruction set to make it easy to encode. Now, compilers have become very good, so we're taking work out of run time and putting it back into compile time instead of continuously decoding at run time."

RISC hardware improvements in the next few years are expected to push the number of clock cycles per instruction below one, Lewine predicts. "It will be done by using 64-bit buses instead of 32-bit, so that you can fetch two instructions and operands at a time," he adds.

So Lewine looks for RISC machines to continue getting faster while CISC architectures run into some fundamental limitations on performance improvements. For example, he believes Intel will be able to build a 486 CISC chip that's almost as fast as Motorola's 88000 RISC chip. But he predicts that if Intel has a 586 processor, it "will run into an insurmountable [performance] gap, compared to the next-generation 88000."

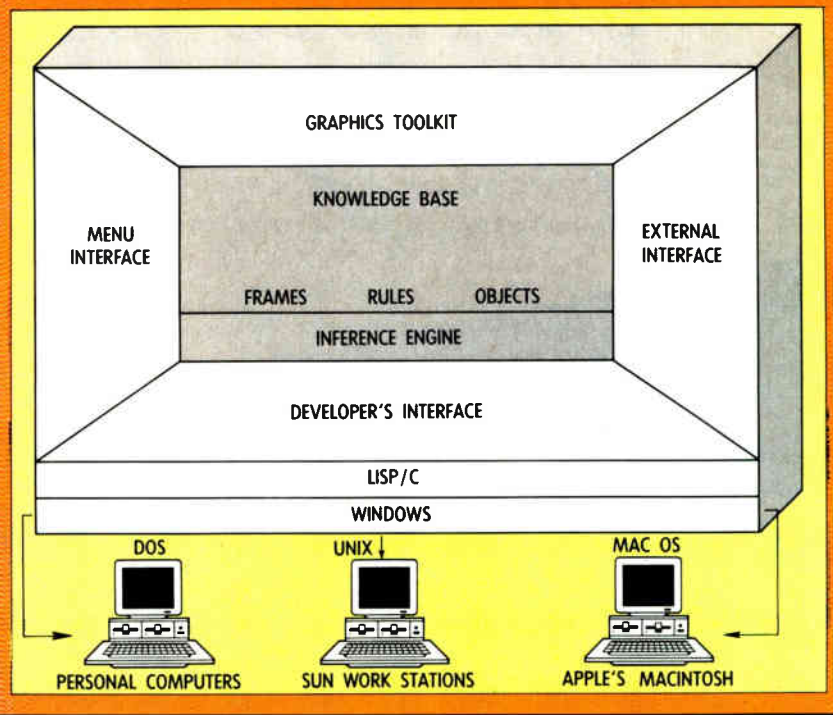
Sequent's Gibson does not totally agree. "Off-chip delays will limit RISC speeds at some point," he says. One RISC problem that's likely to be overcome is difficulties with parallel processing, he adds. For example, the first generation of RISC chips doesn't address the communications needs of parallel processing. But Gibson predicts the second-generation RISC chips will have architectures to support parallel processing.

The major trend ahead in desktop personal computers is definitely more power—so much so that some will match the power of a mainframe. Look for a flood of products built with Intel Corp.'s fastest 80386 microprocessors, speedy cache memories, and huge main storage based on more plentiful 1-Mbit dynamic random-access memories.

While speed is a factor, lowering costs is also a concern. Intel's new 386SX processor makes such a movement possible: it replaces the 386's 32-bit I/O channels with 16-bit buses, so it is smaller and less costly to build with. Compaq Computer Corp. of Houston was among the first PC makers to tap the 386SX. Expect more to follow in late 1988 and early 1989, say industry watchers.

But while hardware advances are happening quickly in the PC arena, software continues to be the stalling factor in putting all the power to work. Complete operating system suites are just now starting to appear, and its tardiness has slowed a major influx of application software using the full power of the fast new microprocessors, multitasking features, and large-memory programs. Unix and the IBM-Microsoft OS/2 are the top candidates for system houses wishing to move beyond the limitations of DOS. With Unix now available for the 386 and other 32-bit microprocessors, there's a good chance that Unix versions of some

## BRINGING EXPERT SYSTEMS TO THE MAINSTREAM



Expert system technology is now coming in complete packages, such as Gold Hill Computers' Gold Works II system, easing integration of rule-based modules into mainline computing.

mainline PC programs will start to appear. And with OS/2 now finally available, IBM's extended version coming late this year, and the Presentation Manager user interface due any day, applications should start pouring into the market in early 1989.

But two new advanced software technologies that are now coming to the fore are expert systems and neural networks.

### Software continues to be the stalling factor in putting all the PC power to work

Expert systems, which have been touted for several years now, will finally begin to be used extensively in mainstream computing. That's because they can now be easily built on conventional mainframes. That means programmers do not have to be experts in artificial-intelligence languages. So in the year ahead, expert systems will start performing a broad spectrum of useful functions in computing as AI software is integrated into conventional applications.

New tools, running on personal computers and work stations, are now appearing to ease the development and integration of expert systems. One example of this kind is from Gold Hill Computer Inc., Cambridge, Mass. The company recently announced Gold Works II, which is

intended to be a complete package for expert-system development running on IBM-compatible personal computers and work stations from Sun Microsystems Inc., as well as on Apple Computer Inc.'s Macintosh computers.

Neural-network technology, which at its current stage attempts to simulate certain adaptive functions of the human brain in software, should begin to pay off with its use in commercial products in the coming year. In certain applications, programs that can perform adaptive behavior and learning will be able to solve some problems much more efficiently than conventional logic-based computers.

**NEW POWER.** In other cases, these systems will be able to solve problems that cannot be addressed by today's computers. Neural networks will help build computer vision systems that perform much more like the human eye/brain combination with its rapid pattern recognition and discrimination. In addition, neural-network-based computers will be able to listen to and understand continuous speech from anyone.

One big problem cropping up with today's neural-net applications is training: the nets must be presented with a large amount of case data or examples before they can learn to do their intended job. "I am interested in seeing if self-organizing networks can be used on a larger scale to get around the big training cost of neural networks," says Scott Kirkpatrick, manager of advanced architecture studies at

## DISKS AND PRINTERS RACE TO KEEP UP WITH SYSTEMS

IBM's Thomas J. Watson Research Center. These self-organizing nets are the result of research conducted by one of the IBM Watson lab scientists, Ralph Linsker.

One software trend that isn't likely to change in 1989 is the burgeoning popularity of AT&T's Unix. "Unix is becoming an important operating system as more and more scientists and engineers want a seamless interface between work stations and their supercomputers," says IBM's Wies. In fact, many today believe Unix is the only possible base for providing application compatibility across all computer classes—from work-stations and personal computers all the way up to supercomputers.

**EXTENDING UNIX.** A major step towards greater harmony among all computer classes lies in the efforts to rework Unix to better suit multiprocessing equipment, supercomputers, and networked work stations. Data General's Lewine says his firm has worked on overcoming the operating system's limitation in multiprocessing applications. DG recently introduced a symmetrical-multiprocessing Unix called DG/UX, which is the first use of technology developed over the past four years by its Research Triangle Park, N. C. operation. Lewine says it results from "a major revision of the Unix kernel to support fully symmetric multiprocessing."

At Honeywell-NEC Supercomputer, Berrett says he is also concerned about the ability of the industry to provide Unix with extensions that are suitable for supercomputers and parallel processing. "No one is sure Unix is the best operating system for supercomputers, but that's what the market demands, so we'll continue to attack the Unix extensions in the next year or two to try to make it the robust environment needed for supercomputers," he promises.

Among the needed extensions, Berrett especially cites the need to change the batch orientation of Unix, as well as the way the operating system handles database management, job scheduling, and security. "Many applications for supercomputers require tight security," he notes, and Berrett says the industry has yet to develop a "strong, secure kernel that still offers the responsiveness that Unix provides."

Like others in parallel processing, Apollo Computer Inc. has had to modify Unix. David Nelson, vice president and chief technical officer, says Unix does not have the features to support tightly coupled parallel CPUs addressing shared memory. "We've had to modify the kernel to handle that," Nelson says, adding that the official AT&T version of Unix also is not good at supporting disk stripping or mapping files into virtual memory.

—Tom Manuel and Lawrence Curran

The relentless drive to store more data in less space will yield big dividends next year in all forms of magnetic media. And the result will be innovative new products, such as a portable computer that fits inside a briefcase with room to spare. But getting increasing attention in other computer peripheral areas, especially in optical-disk technology and laser printers, will be improvements in the speed at which peripherals get their jobs done.

Floppy disks and their drives will get smaller and cram more information on each disk, thanks to new drive designs and higher-capacity media. Winchester drives will get smaller and store more megabytes, by utilizing better heads and media. Tape drives will get a capacity boost too, by borrowing helical-scan recording technology from consumer video and audio products. In addition, more tape drives will appear on the market that use the higher-capacity IBM 3480 1/2-in. cartridge.

But for optical-disk-drive technology, development will focus not so much on boosting capacity as it will on improving access times and data-transfer rates so that they are more on par with those of Winchester drives. Likewise, improvements in laser printers will be aimed at getting better performance, mainly in the controllers that interpret PostScript commands to build images.

In the magnetic-storage realm, the ubiquitous floppy disk will be starting the next big step towards smallness next year. The 3.5-in. drive is now commonplace, and some demand will be building in 1989 for the next generation: 2- and 2.6-in. floppy disks and drives, says Philip Devin, senior analyst at Dataquest Inc., a market research firm in San Jose, Calif. Such small floppies have been in existence for a couple of years now but have not been designed into computer systems. Two Japanese manufacturers, Sony Corp. of Tokyo and Matsushita Communication Industrial Co., Ltd. of Yokohama, introduced 1-Mbyte 2-in. drives in 1987.

Devin believes these drives have finally

found a home and are destined for the next generation of lightweight "notebook" computers. The computer niche gets its name from the fact that it approximates the size of a three-ring notebook binder. Early generations of these 3-to-5-lb computers did not come with integral disk drives, but the 2-in. drives will bring the convenience and power of built-in disk drives to such small machines, says Devin. Sony is one company that already has such a lightweight disk-based product in Japan called Produce. Small enough to fit into a briefcase with full-screen display, two 1-Mbyte floppy drives, and page printer, the product is used as a Kanji word processor. The company has made them available to all their Japanese executives in Japan and the U. S.

There are skeptics who downplay the importance of the impending announcement of the disk-based notebook computer. Scott Holt, vice president of sales and marketing at Conner Peripherals Inc. of San Jose, Calif., contends that users have gotten accustomed to high-performance portable computers with 80286 and 80386 microprocessors. Any new notebook computer will have to match this performance and storage capacity, he feels, which means not only a 2-in. floppy but a 2-in. Winchester with 20 Mbytes of capacity.

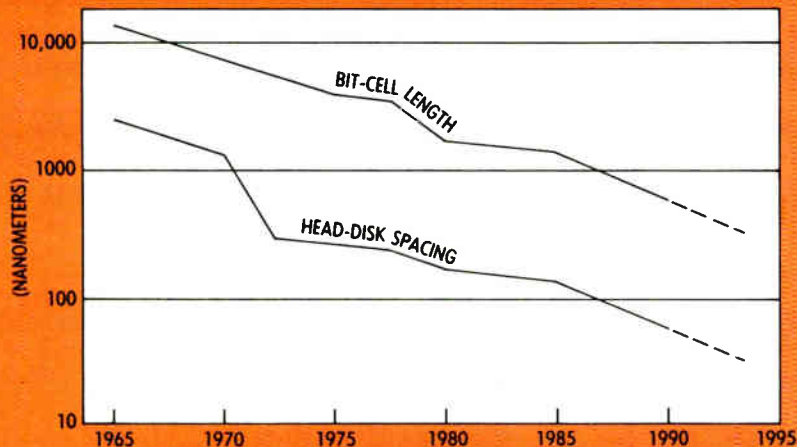
**GETTING SMALL.** To build such a system in a notebook-sized package that runs on battery power is not yet possible, Holt points out; he believes the product is at least a year and a half away. On the other hand, many portable users will likely welcome a breed of computer that brings full floppy-based personal-computer functionality to a package that weighs about half or less of what current offerings do.

Next year will also finally see the arrival on the market of high-capacity 3.5-in. floppy-disk drives having 20 Mbytes of capacity or more, says Robert Gasgoyne, senior analyst at Dataquest. These drives will add to the usual floppy functions the ability to back up data stored on Winchester hard disks, thus replacing the cartridge tape

### COMING SOON

- Demand builds for 2- and 2.6 in. floppy disks and drives
- Lightweight 'notebook' computers with built-in disk drives
- Winchester drives with better heads and media for more capacity
- Laser printers using RISC microprocessors designed for PostScript interpretation

## RECORDING-SYSTEM SCALING TREKS DOWNWARD



SOURCE: IBM CORP.

Winchester drives will soon hit packing densities of 30,000 bits/in., meaning bit sizes must shrink, and drive read/write heads must fly closer to surfaces.

drives currently sold in many systems for this purpose. Insite Technology Inc. and Brier Technology Inc., both of San Jose, Calif., have announced such drives and at least one new startup will announce a similar unit at this the Comdex show that will be held in Las Vegas in mid-November.

Winchesters, meanwhile, will follow the trend in floppies disk drives toward smaller-diameter drives and toward higher capacity in the larger-diameter disk drives. One startup company called PrairieTek Corp., Longmont, Colo.—formed by Terry Johnson, the former founder of Miniscribe Corp.—is working on a 2.5-in. Winchester disk drive.

The 2.5-in. product will offer 20 Mbytes of storage capacity and draw only 1.5 W, for battery-powered operation. The drive will use thin-film heads and media to achieve that capacity in such a package that's so small (1 by 2.8 by 4.3 in.) and lightweight (0.6 lb).

One supplier already making samples of media for these tiny drives is Domain Technology Inc. of Milpitas, Calif. The company is making for PrairieTek a disk with an outside diameter of 65 mm and inside diameter of 20 mm.

Some drive makers have complained about the inside diameter, saying that it should be smaller to allow more area to store data. Nonetheless, Conner Peripherals, IBM, and Miniscribe, have all indicated their interest in the media, says David Pierce, chief executive officer of Domain. He points out that 20 mm is as small as the inner diameter can go if the spindle motor is to be mounted inside the drive's hub for miniaturization purposes.

Next year will also see the advent of 100-Mbyte 3.5-in. and 1-gigabyte 5.25-in. Winchester disk drives. This new capacity range will come not from a radical new

technology like vertical recording but rather by increasing areal density with current-generation thin-film heads and media. Thin-film media suppliers such as Komag Inc. of Milpitas, Calif. offer disks that can support 25,000-bit/in. linear data densities; products are under development that can support 30,000 bits/in.

These higher bit densities require a smaller bit cell, and writing a smaller bit cell means a lower magnetic flux to rep-

### A big change for tape drives will be moving to helical-scan recording technology

resent each bit stored on the disk surface. To read and write, then, means flying the read/write head closer to the media; this in turn will make smoother disks necessary. Komag's vice president of sales and marketing, T. Hunt Payne, says thin-film media can support flying heights of 7 to 8  $\mu$ m. today.

**LOW FLIGHT.** Such flying heights will support capacities of 200 Mbytes in a 3.5-in. disk drive. But the 1-gigabyte 5.25-in. drive may not make it until a slightly lower flying height, 4 to 5  $\mu$ m., can be achieved. Media manufacturers expect to provide disks smooth enough to make this happen next year. The first such disks to be practical, however, may replace the standard aluminum substrate with glass substrates [*Electronics*, August 1988, p. 80].

In addition, 1989 will see the use of what is known as zoned bit density to increase storage capacity on drives with Small Computer System Interfaces. Control Data Corp. of Minneapolis uses the

technique to squeeze 702 Mbytes onto their 5.25-in. Wren disk drives. The technique is being used by makers of optical disk drives—such as Maxtor Corp., San Jose, Calif.—to boost density.

With zone bit density, the drive will write more data in a track on the outer edge of a disk than it will in tracks towards the inside. In the Control Data implementation, progression outward from the center of the disk sees a new sector of data added to a track as soon as tracks grow long enough to support another full sector.

Support of differing number of sectors in different tracks is made possible by the drive's embedded intelligent SCSI-based interface. With SCSI, the computer system views the disk drive as a virtual storage element, and simply asks for data by supplying the controller a sector number, instead of specifying a specific sector in a specific track.

Magnetic tape drives will also make significant gains in capacity in 1989. However, unlike disk drives, which by and large will stick to improvements of existing technology, tape drives will be moving to new-generation technology using helical-scan recording techniques—like the ones used in consumer videocassette and digital-audio equipment—to achieve storage capacities of 1 gigabyte on a single small cartridge.

Prototype drives of the helical-scan type will appear at this year's Fall Comdex, with production shipments beginning in 1989, says Louise Bigs, senior analyst with Dataquest. These drives will be marketed for the scientific and engineering computers, not personal computers, she says. Three helical scan formats will vie for support in 1989. One is the 13-mm T120 VHS format, the same as used in video cassette recorders. This is the backed by Hitachi.

A second is the 4-mm digital audio tape format being promoted by Sony Corp. and Hewlett-Packard Co. It uses the DAT tape cartridges that the U. S. recording companies have fought to keep off the consumer market because they fear it will be used to copy material sold on compact disks.

The third is the 8-mm cartridge tape used in video camcorders. This format is being supported by Gigatape, a West German company. Dataquest's Bigs believes that long-term, the Sony and Hitachi factions will prevail in the U. S. and Gigatape will win in Europe.

On the big-system front, tape drives built around the IBM 3480 ½-in. tape cartridge will continue to appear in 1989. There is a plug-compatible market forming to supply low-cost (\$7,000 to \$15,000) IBM-compatible 3480 tape drives, says Bigs. One company early into this market is Aspen Peripherals Corp. of Longmont, Colo.

In addition, 1989 will see yet one more company attempt to bring to market a

tape drive which uses the IBM 1/2-in. tape cartridge, predicts Bigs. This company will follow Cipher Data Products Inc. of San Diego, which has just introduced a long-heralded family of 3480-compatible cartridge tape drives.

Cipher's 3000i family of products include a line of drives in the 8-in. form factor for midrange to small mainframe computers and others with a 5.25-in. form factor targeted at microcomputers, work stations, and small minicomputers. Control Data brought a 5.25-in. drive that used the 3480 media to market over two years ago. It is likely now that Cipher has brought out their offering that Control Data will begin promoting their 3480 offering more actively.

Optical disk drives, the main competition for tape drives in some applications, will also enjoy technical improvement next year to address two problems: low data-transfer rates and high average access times. Companies will be looking to beat the high-water mark for performance set by Maxtor with their Tahiti erasable optical drive, introduced this year. The Tahiti drive has an average access time of 43.5 ms and an im-

pressive 13.7-bit/s data-transfer rate.

Although average access time is important in write-once optical disk drives, data-transfer rate is a more significant performance specification, says Philip Shires, vice president of sales and marketing at Laser Magnetic Storage International Inc. in Col-

### Laser printers will use special RISC chips for PostScript interpretation

orado Springs, Colo. Laser Magnetic offers write-once drives with average access times of 70 ms; most other drives are over 100 ms. The Laser Magnetic drive also has a transfer rate of 10 Mbits/s—and a high data rate is paramount, because write-once drives are used more for the growing application area of image storage rather than for storing small increments of data, says Shires.

The average access and latency times of optical drives will, over the long term, get closer to those of magnetic drives, predicts

Garrett Garrettson, vice president of research and magnetic recording technology at Control Data. But the data-transfer rates for the two classes of drives will tend to diverge slightly, he says.

The focus for performance improvements in laser printers is not so much in the printing mechanisms—rather, it's on the electronics that control them. The problem comes in interpreting the high-level statements of the versatile PostScript page-description language: if an image is complex, current printer controllers bog down and drastically limit the performance of the printer.

Most laser printers rated at 8 pages per minute can churn out hard copy at this rate if there are making several copies of the same page, but they can't do Steele, director of marketing of Alps America division of Alps Electric U. S. A. Inc., San Jose, Calif. In 1989, some new-generation reduced-instruction-set-computer microprocessors that are designed specifically for PostScript interpreting—Weitek Corp. of Sunnyvale, Calif. offers one—will enable laser printers overcome the problem, he says. —Jonah McLeod

## COMMUNICATIONS

# NEW VOICE-DATA SYSTEMS ARE COMING FASTER THAN EXPECTED

Communications technology is moving faster than expected towards the full integration of voice and data services. That's because innovative engineering has been able to overcome the deficiencies of the existing public telecommunications network that have held back these integrated services. Often these advances stem from technology being developed for the integrated services digital network—so, while the full ISDN is still years away, its impact is already being felt.

It looks like 1989 will be the year when integrated voice/data products deliver enough performance to gain widespread acceptance and utilization. As that develops, users will also begin linking up over video units attached to phone lines.

Major plateaus in communications technology will be reached, as well, in desktop-to-desktop fiber-optic transmission systems, interoperability software linking disparate computers, and network management products to handle all the advances in throughput, functionality, and complexity.

Without making any significant changes in the existing nets, for example, data bandwidth can be boosted from the present

### COMING SOON

- A wave of products will deliver voice, high-speed data, and good-quality video images together
- Use of fiber-optic cable for desktop-to-desktop transmission in local- and wide-area nets

top speed of 19.2 Kbits/s to 64 Kbits/s, says Ken Guy, vice president of corporate product strategy at Micom Systems Inc., Simi Valley, Calif. The widespread use of pulse-code modulation techniques in phone-company central offices means that the bandwidth necessary for digitized voice and data is in place between central offices. The bandwidth problem had existed in the local loop from central office to customer premises, says Guy. But echo cancellation and other conditioning techniques being used in field trials for ISDN have overcome this problem in a high percentage of cases.

By coupling this higher bandwidth with

the enormous advances being made in digital-signal-processing technology, says Guy, manufacturers will initiate a wave of products capable of delivering voice, and high-speed data, as well as good-quality video images. "DSP chips running at 40 MHz teamed with innovative modeling algorithms can achieve effective voice-data rates of 20 times the nominal rate. Modeling algorithms are still an art more than a science," he says, adding that an intuitive tweak in the algorithm can boost performance quite a bit. "Now you can get very-good-quality voice at 9.6 Kbits/s, and with enough DSP power you can do it at 4.8."

**SEEING RESULTS.** Video signals can realize even greater gains in effective bit rates by using both modeling and data-compression techniques. The newly available bandwidth coupled with DSP power will spawn products such as picture telephones without resorting to the expense of T1 service or fiber-optic local loops. Entrepreneurs using DSP chips will be able to realize effective 1-Mbit/s video throughput from 50-Kbit/s service.

A leader in the field is PictureTel Inc., Peabody, Mass., which is now marketing

the V-2050 videoconferencing system, which delivers good-quality video over two 56-Kbit/s lines. The heart of the system is the company's C-3000 video codec, which integrates custom gate arrays, and stores the algorithm on a tape cartridge because of the quick changing nature of the technology. The goal of delivering the same quality video over a single 56-Kbit/s line could be met as early as 1989, says Jeff Bernstein, director of research.

Data communications cannot use modeling and thus must content itself with data-compression methods that generally deliver 3-to-1 boosts in effective throughput. Hewlett-Packard Co., Palo Alto, Calif., and Xerox Corp., Stamford, Conn., for example, have developed compression algorithms that boost 9.6 Kbits/s to an effective 30-Kbit/s rate, says Guy.

Merging these technologies and applying them to the 144-Kbit/s bandwidth that will be used for ISDN's Basic Service can deliver voice, video and data: 9.6 Kbits/s for voice, 64 Kbits/s for video and 70 Kbits/s for data. Using a 3-to-1 boost in effective throughput for the data component delivers in excess of 200 Kbits/s—which approaches the requirements of real-time communication between personal computers.

Micom has already started down that path with a product that uses statistical multiplexing to cram 12 data channels and four voice channels onto one 56-Kbit/s line, and Guy says the company is going full steam ahead with developing products that leverage these technologies. Micom has released a cutting-edge product that takes advantage of the half-duplex nature of voice transmission and the pauses during normal conversation by filling in the silences with packetized data. Stat-V also packetizes voice, and runs on 9.6-, 14.4-, or 19.2-Kbit/s leased analog lines; or, on 64-Kbit/s leased digital lines. Next year, look for Micom to lift V-Stat's point-to-point limitation with a product that allows multipoint applications.

**BIG SWITCH.** Although ISDN has been getting the lion's share of media of attention, the universality it promises depends on the deployment of central-office switches compatible with its protocols. As a result, areas of ISDN services served only by ISDN switches will predominate through the mid-1990s at least.

In the meantime, complementary technologies are taking a crack at delivering ISDN-like services over the installed central-office switching systems that were primarily envisioned for voice and low-speed data. Not surprisingly, these data-over-voice technologies depend on multiplexing signals and must face the difficult trade-off between attaining a useful

local-loop transmission distance and the level of interference between voice and data channels. A breakthrough is likely next year with Integrated Network Corp.'s Universal Data/Voice Multiplexer system, which delivers 19.2 Kbits/s of encoded digital data capacity with simultaneous voice over dial up of lines.

Instead of using frequency-key-shifting techniques, the Bridgewater, N.J., company's patented algorithm reduces energy in the voice frequency band by using partial-response alternate-mark-in-



**Bellcore researchers** are developing an all optical switch that runs at the equivalent of 1 terahertz.

version sinusoidal coding techniques. The technology works its magic by minimizing energy overlap (and consequently, signal interference) between the 4-KHz band reserved for voice and the remainder of the 56-KHz baseband that handles data. The result is an interference-free signal over a 18,000-ft local loop—compared to the 6,000-ft maximum of other data-over-voice technologies.

One of the regional Bell operating companies, Nynex Inc. of White Plains, N. Y., has already put the technology through extensive tests and may reach the point of establishing tariffs for it next year. Tests are going on in four of the remaining six regional Bell operating companies, says Craig Bender, Integrated Network's vice president of marketing. Nynex intends to use the technology as a springboard to a series of enhanced services.

"Data-over-voice is not new," Bender says, "but digital data over voice is." Part of the technology is implemented on the customer's premises, including an analog hybrid module and a custom CMOS time-compression-multiplexing chip that sends data in 56-Kbit/s bursts. Different cards

in Integrated Network's line-interface shelf (see diagram, p. 88) in the phone company's central office hand off the information into the world beyond the central office with ISDN-like services.

It's not just hardware that is driving change in the communication field. The evolution of software—particularly in the world of Open Systems Interconnection protocols—will also have a profound effect on communications. A major challenge lies ahead in developing a wave of end-user OSI products, says John Stephenson, senior vice president for technology and marketing at Retix Inc., a leader in OSI software implementations in Santa Monica, Calif. Up until now, Retix has concentrated on providing original-equipment manufacturers with libraries of OSI-protocol software and boards implementing them, which the OEMs incorporate in their products. The advent of protocols for electronic data interchange—request for proposal information, which is X.12; electronic mail, X.400; and its complement, the globally distributed directory, X.500—will move OSI closer to the desktop. Developing a user interface to handle that functionality "is a major undertaking," says Stephenson. The anticipated user techniques—menu-driven interfaces and a windowing system—will play an important role in end-user OSI products. Retix has chosen Microsoft Corp.'s Windows as its user interface. Next year, Retix will come out with end-user products that should follow closely the latest series of turnkey products, which offer compatibility with Microsoft's OS/2 and Unix System V.3 as well as MS-DOS.

The rapid development pace of universal networking and OSI-based interoperability will initiate another major software technology challenge: network management. "A set of surrounding technologies limit our ability to manage networks," says David Woodall, assistant vice president for product marketing at Timeplex Inc., Woodcliff Lake, N. J.

The problem with present network-management systems is that they operate off-line, depend heavily on human intervention, and are incapable of reconfiguring themselves in response to changes within the network. The present generation of rule-based systems incorporating the knowledge of human experts are evolving toward knowledge-based network management systems that modify themselves, says Woodall, who expects them to return big dividends in productivity. A parallel development is in distributed object-oriented data bases that model the problem. Each object has a behavior repertoire and a message-passing protocol that allows each object—node in the network—to change state to reflect



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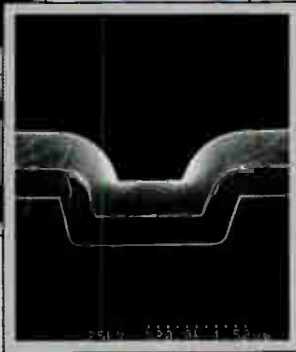
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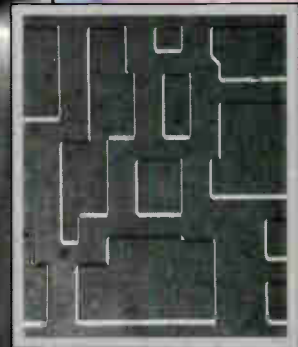
*Temperature-sensitive photoresist after high-dose implantation with the Precision Implant 9200 (SEM courtesy of Cypress Semiconductor Corporation).*



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changes that occur in the network.

Problems inherent to distributed data systems, such as synchronizing changes in data bases, must still be worked out. But Woodall sees great potential not just in tracking down malfunctions, now a manual job—but in finding the least-cost route dynamically. “Networks generate a large amount of data,” he says, “and if you took it all as input to an expert system it would help you plan growth by doing ‘what if’ analyses.”

Fiber-optic technology is on the move as well, according to industry observers. Among the reasons for its growing success are recent advances in connector technology and rapidly decreasing costs, says Bill Seifert, vice president of advanced engineering at Wellfleet Communications Inc., Bedford Mass. Advanced controller devices will emerge next year, which will be another big step, he says. “Fiber will cause a fundamental change in data communication from long-distance common carriers to the backplane of PCs,” Seifert explains. Transmission data rates as fast as a computer’s internal bus will make it possible.

The use of fiber-optic cable as a desktop-to-desktop transmission system for both local-area and wide-area networks is waiting for two things to happen. One is how to successfully “hop” signals from the multimode fiber normally used in LANs to the single-mode fiber characteristic of wide-area networks and the 250,000 miles of fiber already installed in the U. S. public network. The second problem is switching, which must be improved to handle a variety of network functions.

Forcing the industry to deal with the incongruity of single- and multi-mode media used in different applications are the applications’ power requirements and the

different trade-offs between power and cost appropriate for them. Transmitting over long distances requires high-power laser light, which travels best on single-mode fiber.

LANs, on the other hand, can get along nicely using relatively inexpensive light-emitting diodes as their energy source, despite the 2-to-4-km distance limitation that results, says Hal Spurney, director of marketing for Fibronics International Inc., Hyannis, Mass. The leading fiber LAN specification—Fiber-optic Distributed Data Interface—calls for a multimode transmission medium, and Spurney believes that FDDI will eventually fill the leading technology position that Ethernet has been occupying for copper conductors.

### A major challenge lies ahead in developing a wave of end-user OSI products

Building interfaces to connect systems using single-mode and multimode technologies became a problem for Fibronics when it won a three-year contract to install beginning in 1989 fiber-based communications between toll stations on the Autostrade, the Italian superhighway system. The distance of 30 to 40 km between toll stations called for Fibronics to custom design a multimode-to-single-mode converter, which Spurney says will be developed into a standard product.

Another method of increasing the bandwidth that can be delivered economically from common carriers is simply by changing the switching gear, says Timeplex’s Woodhill. Present fiber trunks run at data throughputs of hundreds of

megabits per second, but commercial systems such as AT&T Network Systems’ upgraded FT Series G, which will be available early next year, offer transmission rates of up to 3.4 gigabits/s. Systems still in development will push the ceiling to 10 gigabits/s, says Woodhill.

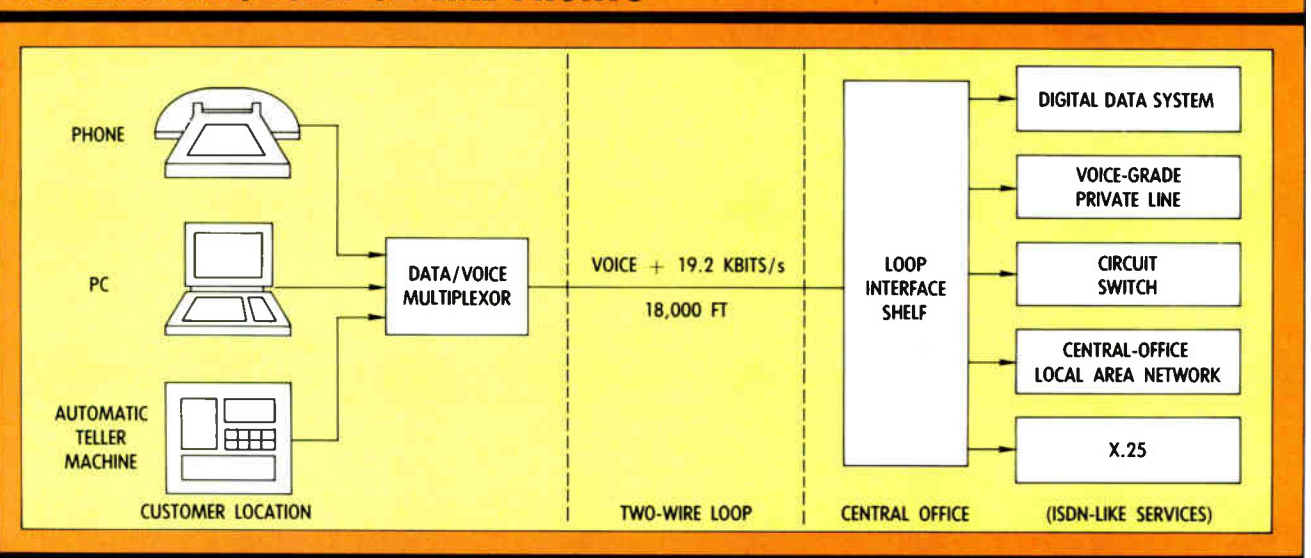
Fast packet switching appears to be the architecture of the future for such systems, and Timeplex and others have key switch products under development now. “We are right now technologically on the edge of whether the first fast packet [switch] is viable,” he says.

**OPTICAL SPEED.** But in using today’s optical-fiber networks, which have higher and higher bit rates, a bottleneck in the electronics used for switching and routing signals needs to be overcome. Researchers at Bell Communications Research’s Navesink Research and Engineering Center, Red Bank, N.J., have successfully tested an all-optical switch that operates in 0.1 ps. The switching speed, which equals cycle-time frequencies approaching 1 terahertz, comes from using optical instead of electronic controls, says researcher Peter Smith. The key to achieving the switching speed is using a material that changes its optical properties with the intensity of light passing through it. In this case, varying intensity causes the signal to switch from one channel in the fiber to another.

“Previous all-optical switching devices have suffered from heating problems caused by light absorption,” says Smith. The result was relatively low switching rates. But Bellcore was able to fabricate its device out of a transparent material that eliminated thermal problems.

Survivability and reliability is another concern about fiber, and a switching technology integrated into a optical ring net-

## PUTTING DATA/VOICE ON-LINE PRONTO



ISDN-like services can be provided over 18,000-ft. local loops with INC’s Data/Voice Multiplexor technology, which minimizes energy overlap and consequently signal interference by using partial-response alternate-mark-inversion sinusoidal coding techniques.

work developed by Northern Telecom Inc.'s Federal Networks division, Vienna, Va., appears likely to be adopted by other vendors as they field their optical ring products, says Wayne Ergle, product manager.

Developed to guard against data loss after a cable is completely cut on a fiber-ring network of up to 31 nodes, the Northern Telecom system reroutes the data around the ring. The system's pri-

mary innovation is in its switching technology. With the fiber capable of carrying up to 12 multiplexed 44-Mbit/s DS-3 signals, the multiplexed signal can be switched to a 560-Mbit/s protection channel if the line is cut. But the system can also switch any one of the 12 lower-speed signals into a protection channel.

Protecting both high-speed (multiplexed) and low-speed signals is a unique combination. In conventional systems, all

12 low-speed channels switch to protection channels when there is a problem on just one channel. This makes for timing problems as the different protection units synchronize, and if the switch interprets the timing delay as a bad signal it will then shut the switch itself off. In Northern Telecom's system, it takes about 2 ms to demultiplex the signals. Software is employed to restore the signals to their original form.

-Jack Shandle

## SEMICONDUCTORS

# THE PUSH IS ON FOR FASTER CHIPS AND FASTER TURNAROUND

The semiconductor industry is working double time on speed. Chips are getting faster, and makers are aiming to get them out faster. The double whammy comes from a heightened demand for higher speeds in circuits that support fast new processor architectures and for faster turnaround of new chip designs in response to shrinking product life cycles in highly competitive systems markets.

At nearly every level, equipment houses buying advanced memory, logic, and analog circuits are realizing that speed—not lowest price—will be the main battleground for business in the early 1990s, say chip executives. And as goes the systems emphasis, so goes mainstream IC technology.

In the year ahead, semiconductor houses will push a broad range of their wafer-production processes below the 1- $\mu$ m barrier. Submicron CMOS integrated circuits will support 50- to 75-MHz clock cycles, and new bipolar integrated circuits will handle 2- to 6-GHz speeds. And in 1989 chip merchants will continue to roll out more application-oriented memories, aimed at eliminating processor wait states by integrating more logic on the die.

Many semiconductor firms will also turn to new production equipment to shorten the time it takes to ship prototypes to key customers. Laser-based direct-write wafer fabrication systems, for example, are expected to be deployed by some companies to churn out prototypes in hours rather than what typically takes weeks today. Semiconductor-manufacturing equipment suppliers also report that in the U.S. a growing emphasis on fast-turnaround, small-volume semicustom ICs is creating a new demand for wafer minifabs, oriented more towards ASICs instead of pumping out millions of one commodity design.

The biggest factor in the speed move-

ment has been the advent of fast 32-bit complex- and reduced-instruction-set-microprocessors. The ever-increasing speed of CISC and RISC computing continues to outstrip the performance of surrounding peripheral logic and memories. Chip makers are attacking this marketing challenge two ways: finer-line process technologies, and IC designs that tightly couple a circuit to an application or even a specific processor type.

### COMING SOON

- Submicron CMOS logic ICs with 200,000 to 500,000 gates and 50- to 75-MHz speeds
- Submicron bipolar chips with 20,000 to 50,000 gates running at 2 to 6 GHz
- Megabit EPROMs and EEPROMs with 35-ns read-access times
- Silicon bipolar and GaAs RISC processors sporting 200- to 500-MHz clock rates
- Bipolar programmable logic devices with 1- to 5-ns propagation delays
- Megabit DRAMs faster than 65 ns for zero-wait-state main memory
- Laser-based direct-write wafer fabrication for quick prototyping
- Fast turnaround ASIC-oriented minifabs with islands of equipment designed for flexibility

A new generation of high-density 1- and 4-Mbit dynamic random-access memories is also coming into play, creating the potential for huge main memory spaces to serve 32-bit processors but also presenting an access-speed vacuum. That vacuum is being filled by a number of types of memory chips, such as fast 1-Mbit static RAMs, specialized SRAMs for targeted applications (such as cache), higher-speed erasable programmable read-only memories, electrically erasable PROMs, and even speed-enhanced DRAMs. Also taking up the call for more speed is an army of makers of gate arrays, standard-cell ASICs, and user-programmable logic devices.

**SPEED SHRINK.** Responding to the need for ever higher performance in their logic and memory ICs, manufacturers in 1989 can be expected to continue an aggressive technology march that will push some processes well below the 1- $\mu$ m range. CMOS processing, with 0.7- to 0.8- $\mu$ m drawn gates, will start to become common in memory and digital logic. As a result, gate delays will drop to the 200- to 800-ps range, supporting clock rates in the 50- to 100-MHz range—double that of today's top-performing ICs.

In the bipolar arena, new devices will hit the market in high volumes with 1- $\mu$ m geometries. Some bipolar prototypes are also expected to be made in 1989 with feature sizes as small as 0.5  $\mu$ m. Typical gate delays will range from 80 to 200 ps in the new bipolar technologies, with clock cycles reaching 1 to 2 GHz versus present limits of 250 MHz to 1 GHz. Just as aggressively, gallium arsenide chip manufacturers are expected to continue their fine-line push, moving mainstream enhancement/depletion GaAs processes from 1  $\mu$ m to the 0.5- $\mu$ m range, resulting in gate delays as low as 100 ps.

By and large, experts in the field say

optical lithography will continue to be the most used wafer-patterning technique well into the 1990s. Most now expect lithography will handle at least  $0.5\ \mu\text{m}$  and possibly  $0.3\ \mu\text{m}$  in most production lines.

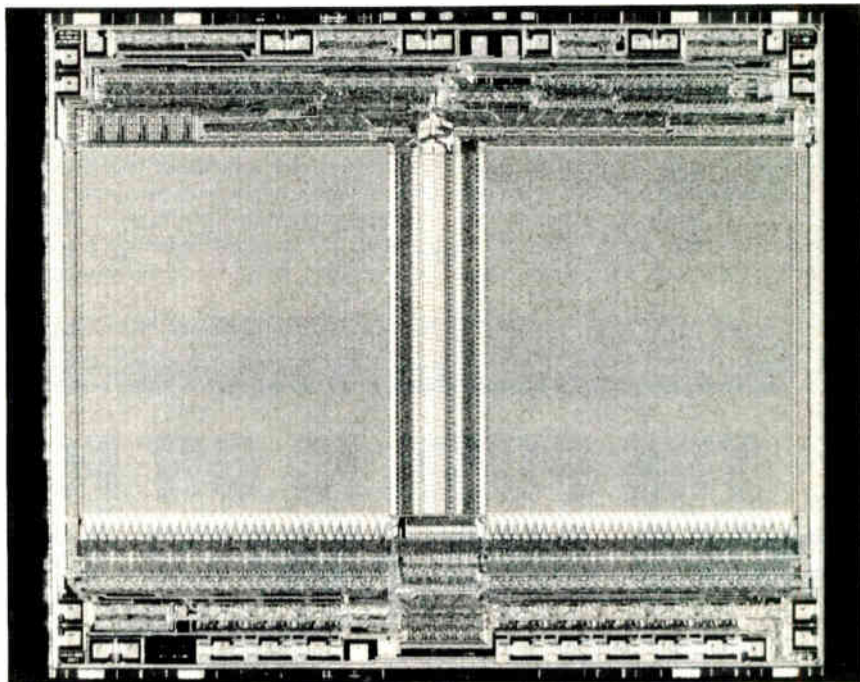
Complementing the improvements in lithography will be a mixed bag of process enhancements that will become more widespread in the coming year. In silicon, these developments will include multilevel metallization, advanced isolation techniques such as sidewall masking, trenching, and selective-epitaxial growth. There will be an increase in ion implantation by chip makers as well.

Of all these techniques, the one that appears to offer the most wide-ranging impact in silicon-based transistor fabrication is selective epitaxial growth. This technique will find widespread applications in not only CMOS, but bipolar and biCMOS mixtures too.

Selective epitaxial growth involves the targeted growth of single-crystal silicon over bulk silicon material through process windows of oxide layers. Developed originally as a circuit-isolation alternative to local oxidation or trenching techniques, selective epitaxial growth is generating wide interest among chip makers. One area of interest is as a way to eliminate the so-called "bird's beak," the unwanted encroachment of material layers that makes process shrinks difficult below  $1.5\ \mu\text{m}$ . Eliminating the problem opens the door for much smaller geometries, perhaps as fine as  $0.25\ \mu\text{m}$ , without many of the second-order effects that currently plague CMOS devices.

**TRENCHED.** In biCMOS, selective epitaxial growth can be used to refill deep-trench isolation structures that don't sacrifice valuable real estate to buffer the bipolar and CMOS devices from each other. What's more, it can also be employed without significant increase in process complexity. Manufacturers are also turning to the selective growth technique in new biCMOS mixtures to form independent bipolar and CMOS doping levels. In bipolar structures, for example, it is being used to form independent npn and pnp devices, thin bipolar base structures, and sidewall base contact transistors. The result, regardless of the type of structure, is a much denser circuit that is also capable of operating at much higher speeds, but without any substantial increase in process complexity.

In the GaAs arena, look for device improvements to stem from greater use of metal-organic chemical vapor deposition and chemical-beam epitaxy to replace molecular-beam epitaxy. GaAs wafer sizes will increase from today's 3- and 4-in. diameters to 5 in. as some suppliers upgrade their process lines and push geometries towards the  $0.5\ \mu\text{m}$  barrier. Also, many GaAs technology observers now believe the industry will make strides towards using gallium arsenide materials



Flash EEPROMs, such as this 512-Kbit part from Seeq, will continue their fast growth in the year ahead. Chip-bit densities are expected to double by the end of 1989 to the 1-Mbit level.

atop silicon substrates, or possibly germanium. The hope is that GaAs-on-silicon wafers will decrease wafer breakage in fabrication, thus lower costs of gallium-arsenide circuits.

In general, the greatest impact of new high-performance processes will be most apparent in microprocessors in 1989. Already using  $0.7\text{-}0.9\text{-}\mu\text{m}$  CMOS technol-

### As goes the systems emphasis, so goes mainstream IC technology

ogies, companies such as Cypress Semiconductor Corp. of San Jose, Calif., are reporting cycle times in RISC-based designs exceeding 50 MHz. Under development by silicon houses are several processors to be made in biCMOS, which should push speeds to at least the 75-MHz range. In pure bipolar technologies, a couple of silicon houses are working on RISC chips based on advanced technologies that will push microprocessor performance into the 100- to 350-MHz range.

The RISC movement, with simpler architectures for 32-bit processors compared to CISC, has turned the microprocessor game into more than purely a CMOS arena, says William D. Jobe, executive vice president of MIPS Computer Systems Inc., Sunnyvale, Calif. CISC processors typically have gate counts of 500,000 to 750,000, making them difficult to produce in anything but the most advanced CMOS technology, he says. Since stripped down RISC processors seldom exceed 100,000-gate counts, it is

feasible to fabricate them using the lower-density but faster emitter-coupled logic or even GaAs processes.

Another spinoff of the RISC movement is the incorporation of these processor cores into cell-based ASIC libraries, notes Russell L. Steinweig, VLSI Systems product marketing manager of VLSI Technology Inc. of San Jose. "In essence, a RISC machine is a CISC processor, stripped to the bare essentials," he says. "Using it as a core element in a standard-cell methodology, a systems designer can build up a processor specific to his particular systems requirements, with significant improvements in throughput." For equivalent design rules and processes, an application-specific RISC chip could conceivably run at least twice as fast as a RISC processor using external glue logic and four times as fast as a CISC machine in the same application.

**MEMORY CRUNCH.** The bit-crunching capabilities of these faster processors is placing a new emphasis on speed in memories. Although DRAMs will continue a predictable march towards higher densities—4-Mbit and some 16-Mbit prototypes are expected in the coming year—the vast majority of activity in memory markets will be focused at reducing access times of the 1-Mbit DRAMs and SRAMs now hitting volume production. There is a big performance gap because main-memory DRAMs average between 100 and 120 ns, says C. N. Reddy, vice president of engineering at Alliance Semiconductor Corp., San Jose, Calif.

That's much too slow for the current-generation of 16- to 25-MHz 32-bit processors, which require main-memory access times below 90 ns. And with even faster

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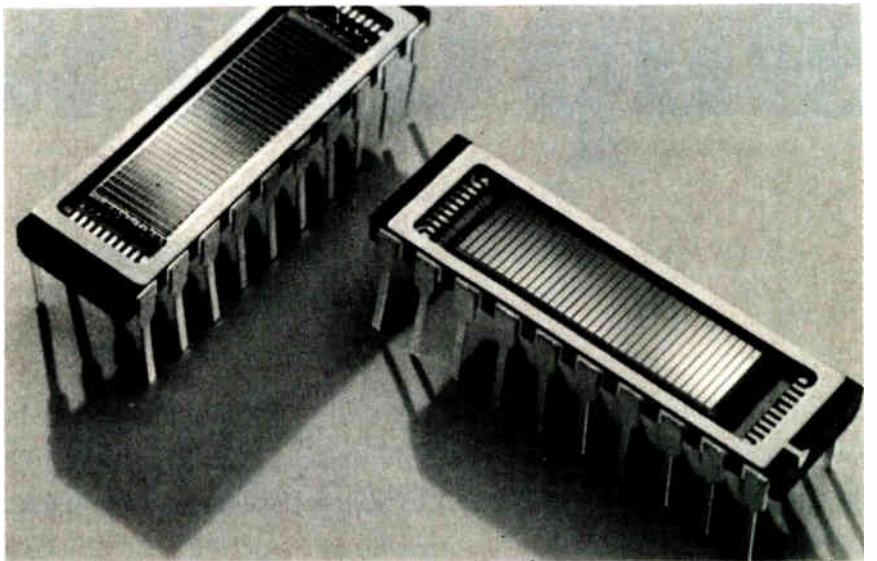
processors coming on line, main-memory access times will need to fall below 60 ns in order to avoid performance-stalling wait states. In the absence of such high-speed main-memory alternatives, systems designers have had to turn to lower-density fast SRAMs and cache SRAMs to fill in the speed gap. But this may all change during 1989, with the appearance of a new generation of sub-60-ns 1-Mbit DRAMs and sub-45-ns 1-Mbit SRAMs, Reddy says.

To support the operation of high-performance superminis and mainframes, as well as the new generation of bipolar RISC machines, 256-Kbit ECL-biCMOS SRAMs will hit the market in the coming months sporting fast access times below 25 ns, and 1-Mbit parts are not far behind.

A similar trend is occurring in nonvolatile memories, where CMOS-based ultraviolet-light and electrically erasable PROM devices (in the 16- to 128-Kbit range) are taking the place of bipolar PROMs for storage of microcode in bit-slice and RISC-based computer designs. Again, in order to keep the processors running without wait states, typical read-access times with these nonvolatile memories are needed to be in the 25- to 45-ns range. To achieve such speeds, previously only possible with bipolar PROMs, manufacturers of CMOS EPROMs and EEPROMs are using a variety of circuit-design improvements. By early next year, higher density 1-Mbit EPROMs and 256-Kbit EEPROMs are expected to emerge with access times below 45 ns. However, at such densities circuit improvements will not be enough, forcing manufacturers to move to smaller geometries to achieve the smaller and faster transistors required.

The so-called flash EEPROM (a marriage of EPROM and electrically-erasable technologies for high-density potential) should stay in lockstep with related nonvolatile parts, according to the projections of such companies as Intel Corp. and Seeq Technology Inc. Already at the 512-Kbit level, flash EEPROMs have typical access times in the 150- to 200-ns range, and are expected to begin pushing just below 100 ns by mid-1989. And lower-density parts should be available in sample quantities from a number of companies with access times in the 45- to 60-ns range by the end of the year, says Alan Ankerbrand, director of marketing for MOS Memory products at National Semiconductor Corp., Santa Clara, Calif.

On the logic side of the speed campaign, gate arrays and programmable logic devices—both in CMOS and bipolar—are expected to track performance improvements in both processors and memories. In low-density bipolar PLDs, for example, current 2- $\mu$ m bipolar processes are yielding 5- and 7.5-ns gate delays. In the mid-1989 timeframe, ECL should be able to push those



**The first commercial** prototypes of 16-Mbit DRAMs are soon likely to appear; parts such as these from Matsushita Electric debuted at 1987 technical conferences.

speeds well under 5 to 7 ns. In the TTL world, bipolar PLDs are already available with 7.5- to 15-ns propagation delays. The coming generation being readied will push delays under 7.5 ns.

Upping the speed ante even further in the PLD market will be new entries from GaAs suppliers. Currently only one firm, Gazelle Microcircuits Inc. of Santa Clara, Calif., has been making a version of the industry standard 22V10 available for sampling that is capable of supporting 7.5-ns delay times, a significant upgrade

### In gate arrays, bipolar ECL circuits should benefit first from 1- to 1.5- $\mu$ m processes

from its 10-ns initial offering. By mid-1989, at least one other GaAs PLD player is planning to enter the market with an ECL-compatible GaAs PLD family.

In gate arrays, bipolar ECL circuits should be among the first to benefit from the new 1- to 1.5- $\mu$ m processes with densities going from 10,000 and 15,000 gates to about 20,000 to 25,000 gates next year. Meanwhile, the bipolar processes are expected to cut the typical gate delays of the fastest parts from 150 ps to less than 100 ps. At the same time, 1.0- $\mu$ m enhancement depletion mode-based GaAs arrays (compatible with ECL signal levels) should be become available from a couple of sources with chip densities of 10,000 to 12,000 gates and speeds roughly comparable to bipolar parts.

Density increases in CMOS arrays are expected to plateau momentarily at the present 200,000-gate level, while manufacturers work on new ways that will increase gate utilization from what is now generally 50% to around 80%. Many are

looking at borrowing concepts used in bipolar part, such as three- and four-level metal interconnection, as well as improved sea-of-gates designs. To increase performance, CMOS manufacturers are also considering the use of biCMOS as one way to reach higher clock frequencies and lower gate delays without giving up the traditional low-power and high-density advantages of CMOS.

While silicon makers push the speed of ICs, they are also working on ways to reduce the lag between design and prototypes for their chip-buying customers. System houses can expect to see progress made on three fronts in the coming year: the emergence of new high-density programmable logic devices and user-configurable gate arrays; new laser-based direct-write equipment for use with high-density gate arrays, and a movement by silicon houses towards ASIC-oriented flexible "minifab" lines that are particularly well-suited for small-to medium-volume unit manufacturing.

Users of field-programmable logic chips will see the EPROM-based technology take densities from 6,000 gates to the 10,000-gate range in the coming year. That increase will make for faster turnaround of system designs by replacing more glue logic and masked gate arrays.

In addition, SRAM-based logic cell arrays, now available with up to 9,000 gates, will reach 15,000 gates in 1989. Because these parts are user-configurable, between \$10,000 to \$70,000 in nonrecurring engineering costs associated with masked arrays can be eliminated.

Intended to reduce semicustom-chip prototyping cycles, too, are laser-based direct-write production systems, which are coming from the likes of Elron Technology in Haifa, Israel; Lasa Industries Inc. of San Jose; and Lasarray Corp. of Los Angeles. These systems are expected



**All your  
perceptions  
about EPLDs  
are about to  
go out the  
window.**



**If you believe EPLDs are  
constrained by their architecture,  
this should open your mind.**



# Introducing MAX.

## A totally new architecture that will change your thinking about EPLDs.

Still think that EPLDs can't be fast and dense?

Then prepare to erase and reprogram your thinking.

The new MAX family from Altera has a radically different EPLD architecture that can make your fastest, densest designs fly out the door in no time.

With twice the speed and three times the density of conventional EPLDs.

At the heart of the MAX architecture are Logic Array Blocks (LAB) incorporating three major innovations:

First, streamlined, totally programmable macrocells with multiple control product terms that cover all your basic design needs.

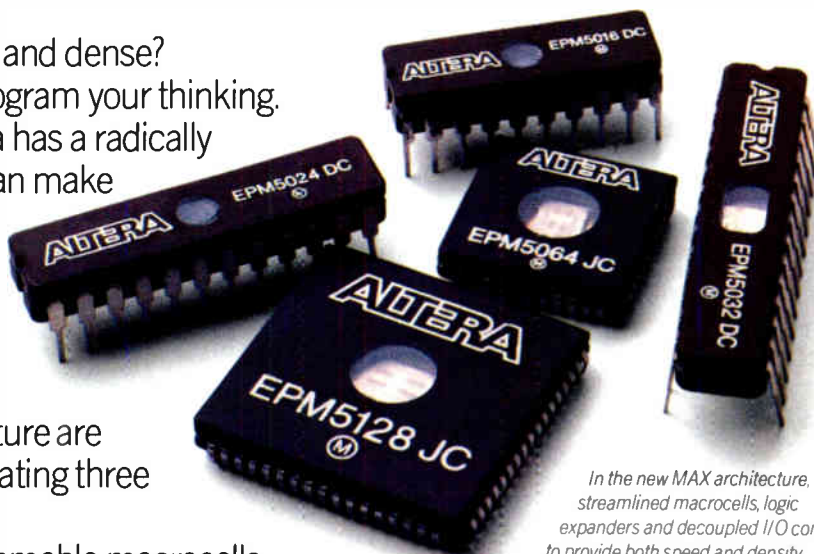
Secondly, Logic Expanders that let you assign additional product terms to any macrocell, for even more complex logic structures. So you can put additional logic where it's needed, for better chip utilization and more buried logic capacity.

Finally, decoupled I/O that lets you use all your pins and flip-flops independently. So you can add huge amounts of logic, and still keep all your I/O options open.

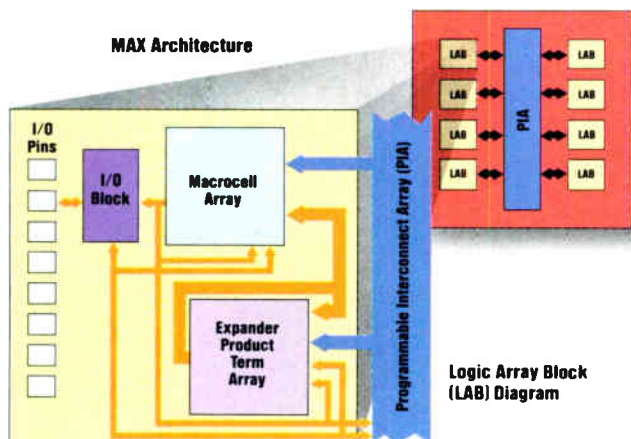
Tying it all together, a Programmable Interconnect Array links MAX's multiple LABs efficiently.

And when you combine the PIA with a high speed, 0.8 micron CMOS process, you get high density devices with small device performance.

And an EPLD architecture that won't confine you.



*In the new MAX architecture, streamlined macrocells, logic expanders and decoupled I/O combine to provide both speed and density.*



*At the highest densities, MAX incorporates a Programmable Interconnect Array that lets you connect all your logic without routing bottlenecks. The result is high array density with small array performance.*

**Get ready to can the idea  
EPLDs can't be dense.**



# Now you can pack the functions of 50 TTL devices on a single MAX family EPLD.

The key to MAX is density and speed combined.

But first, let's do a little cramming on density.

Because of its streamlined logic array blocks, PIA and advanced process, MAX delivers three times the density of the largest conventional EPLDs.

For instance, the MAX EPM5128 can take the place of 50 or more TTL devices. Or 20 plus PALs.\*

In fact, you can put the entire TTL Data Book on a few MAX EPLDs. Because MAX can accommodate exact functional equivalents of all popular 7400 type MSI and SSI standard-logic parts.

Which means you can still design by The Book, while enjoying all the benefits of user-configurable logic. Plus

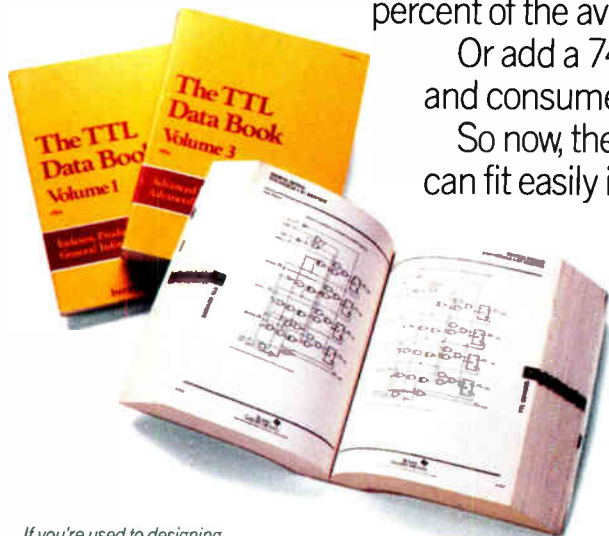
you get the simplicity of using just a few MAX devices in place of hundreds and hundreds of TTL part numbers.

For example, you can place a 74161 counter in the EPM5128. And take up only three percent of the available space.

Or add a 74151, 8-to-1 multiplexer to the same MAX device and consume less than one percent of space.

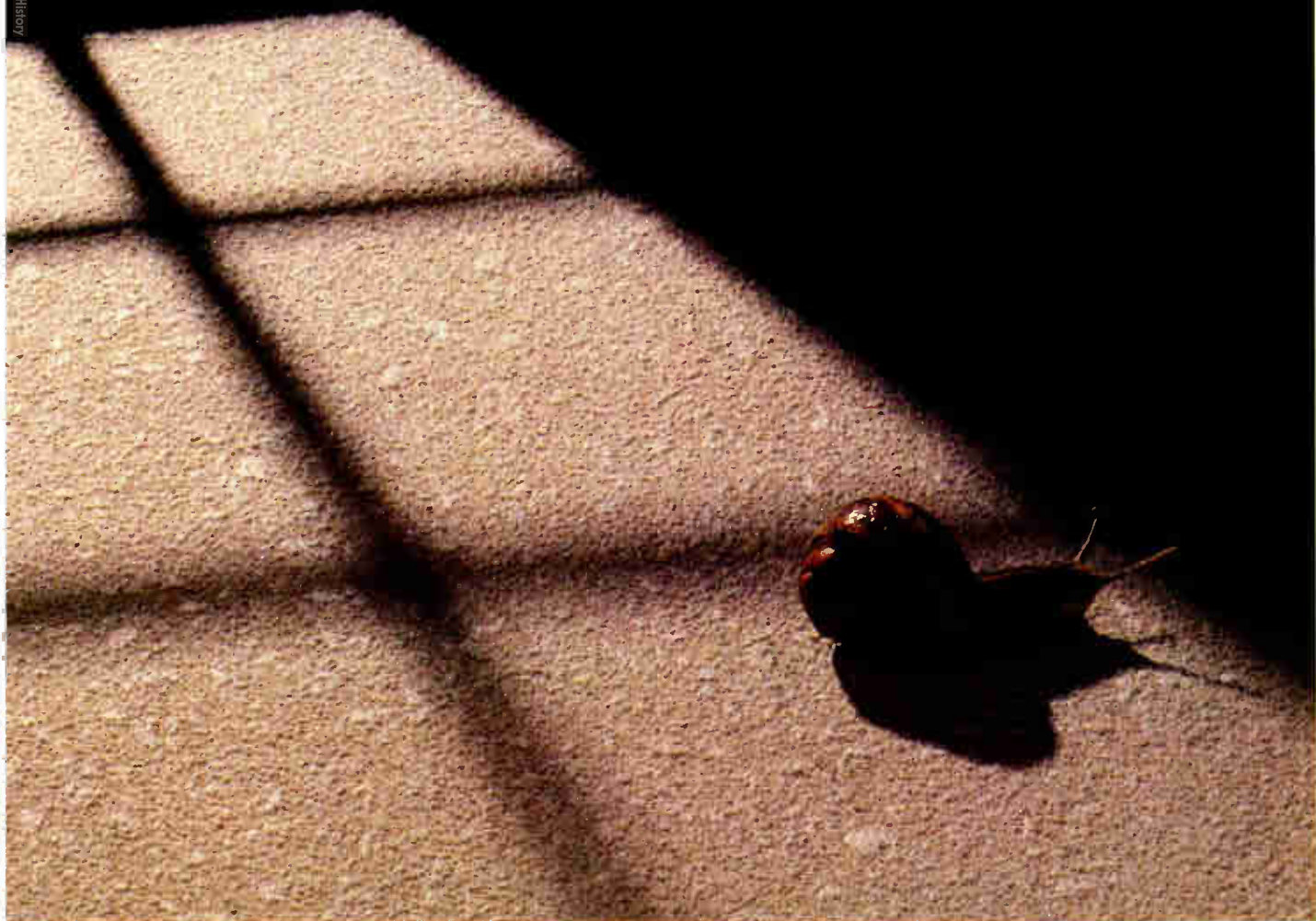
So now, the functions that used to take up an entire board can fit easily into one extremely dense MAX part.

A part that you'll also find to be extremely fast.



*If you're used to designing with TTL, you don't have to change your way of thinking. MAX accommodates exact functional equivalents of all popular TTL part numbers.*

**If you think EPLDs are slow,  
let us bring you up to speed.**



# The MAX family runs at system clock rates up to 50MHz. Twice the speed of any other high density EPLD.

Only the MAX family can give you the combination of speed and density you need in your next system design.

And not just raw speed, but predictable speed as well.

Because at higher densities, our Programmable Interconnect Array gives you predictable delays between all corners of the chip.

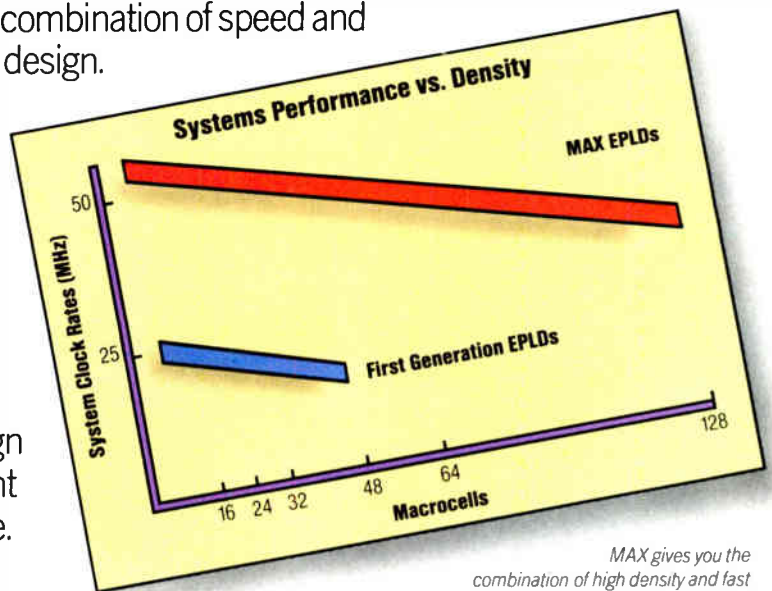
And that means no more hair-pulling over lost speed. No gate array timing skews. No more multiple design iterations to get the speed you thought you were going to get in the first place. The result is more useable system performance at system clock rates up to 50 MHz.

Which makes MAX the fastest, high density CMOS EPLD in the world. For example, with our EPM5032, you can design a bus controller that runs at 32MHz while utilizing 32 registers and up to 32 product terms feeding a single register.

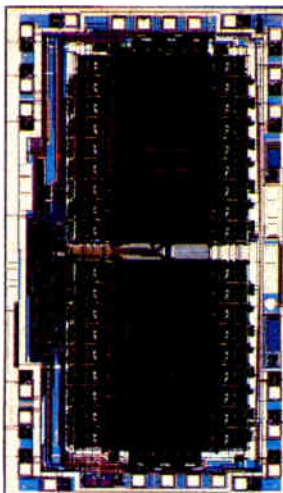
And with our EPM5064, you can breeze through a 25 nanosecond address decoder for a cache controller and still achieve a fan-in of 25.

For really big jobs like state-of-the-art DMA controllers, our EPM5128 has an array of expanders and macrocells that can easily soak up all the logic you need.

All of these logic functions can be designed fast, too. In just a matter of hours, in fact. Because MAX is supported by software that's easy and quick to design with.



*MAX gives you the combination of high density and fast performance you need for your most advanced designs*



*Fast, high density controller designs can be implemented with the EPM5032, 32-macrocell MAX EPLD.*

**And block any thoughts  
about EPLDs being  
difficult to design with.**





# The new MAX+PLUS™ software makes every step of the design process quick and easy.

Working with MAX EPLDs can be very much like play.

Thanks to MAX+PLUS.

It's software that uses powerful logic synthesis techniques that make design simple and intuitive. And it runs on your IBM PC AT™ or compatible, or IBM PS/2.™

MAX+PLUS gives you a whole set of programs under the control of a supervising database manager module.

Included are a variety of design entry methods, a design processor, a timing simulator and programming software.

A hierarchical graphics design editor lets you build your design from the top-down, starting with an overall device block diagram. Or you can go from the bottom-up, by first simulating small logic functions.

You can select logic symbols from the complete 7400 series library or build your own custom library for your specific needs.

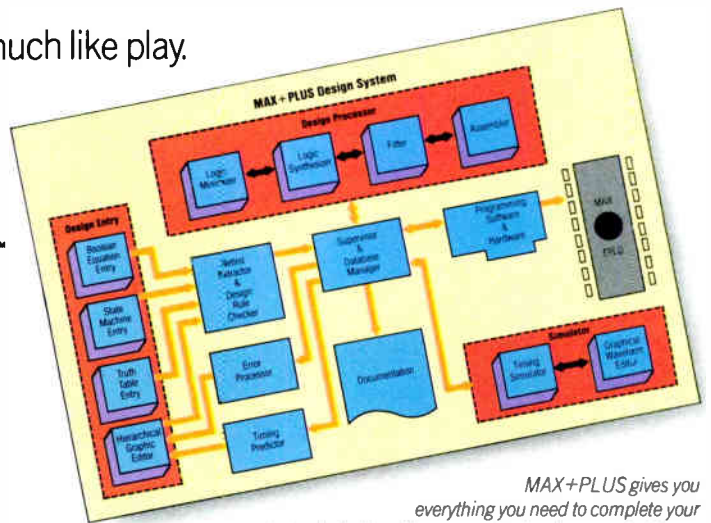
And when you're ready to compile, the software will minimize and automatically place your design in MAX. So you don't have to. And it does it in minutes.

MAX+PLUS even locates your design entry errors automatically, highlighting problem nodes on your schematic. Thus saving you time and trouble.

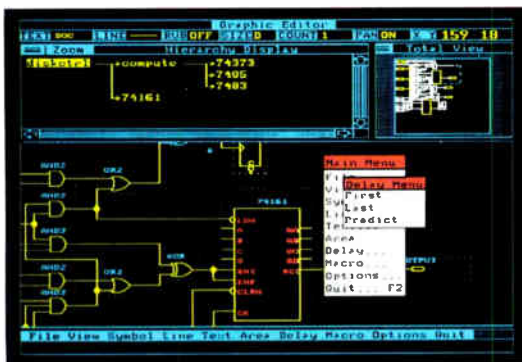
MAX+PLUS also offers a convenient timing calculator that instantly displays your worst case delay between two points. Plus full timing simulation software to simulate

your entire design.

MAX+PLUS software even solves the most important timing problem of all. Because it lets you put your custom design on your board in hours instead of weeks. Speeding you to market right on time, ahead of the competition.



MAX+PLUS gives you everything you need to complete your design. Including all programming hardware and software.



The MAX+PLUS hierarchical graphics editor lets you organize your design from either the top-down or the bottom-up.

**Now here's the clincher.  
It's about the cost of EPLD design.**



# Faster design time, fewer parts on your board means MAX saves you money.

The MAX family is your fastest, lowest cost way to get to market.

Which has never been more important in the competitive electronics marketplace.

In fact, a study by McKinsey and Company shows that getting to market six months ahead of a competitor can triple profits over the life of a product.

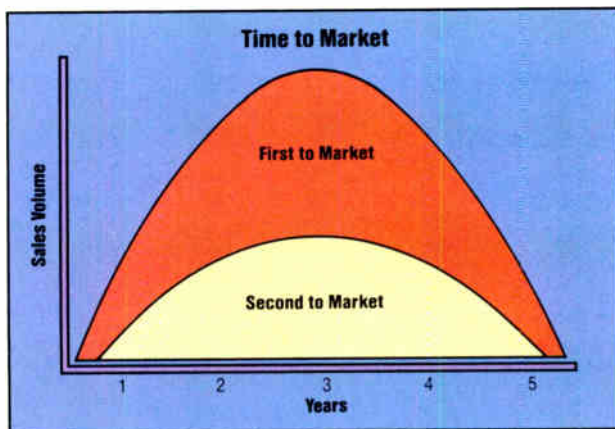
And the same study shows that even with a 50% development cost overrun, after tax profit would be reduced by only 3.5 percent.

But the beauty of MAX is not only that it offers the shortest time to market of any logic technology, but it's also one of the least expensive ways to go. Compare it to expensive NRE charges and the high risks of time consuming gate arrays. And you'll find there's no comparison at all.

Compared to discrete TTL, CMOS or PALs, MAX not only speeds the design process,

but also dramatically reduces your parts count and your board size. That's why MAX can mean all the difference between winning the largest piece of the pie, or getting stuck with what's left of the crust.

With MAX you design for peanuts and end up with a fistful of dollars.



*Getting to market six months earlier than the competition could mean a tripling of profit over the life of the product.*



*To insure the lowest production unit cost, we also offer OTP plastic devices.*

# If you're ready to take the lead in logic design, here's your window of opportunity.

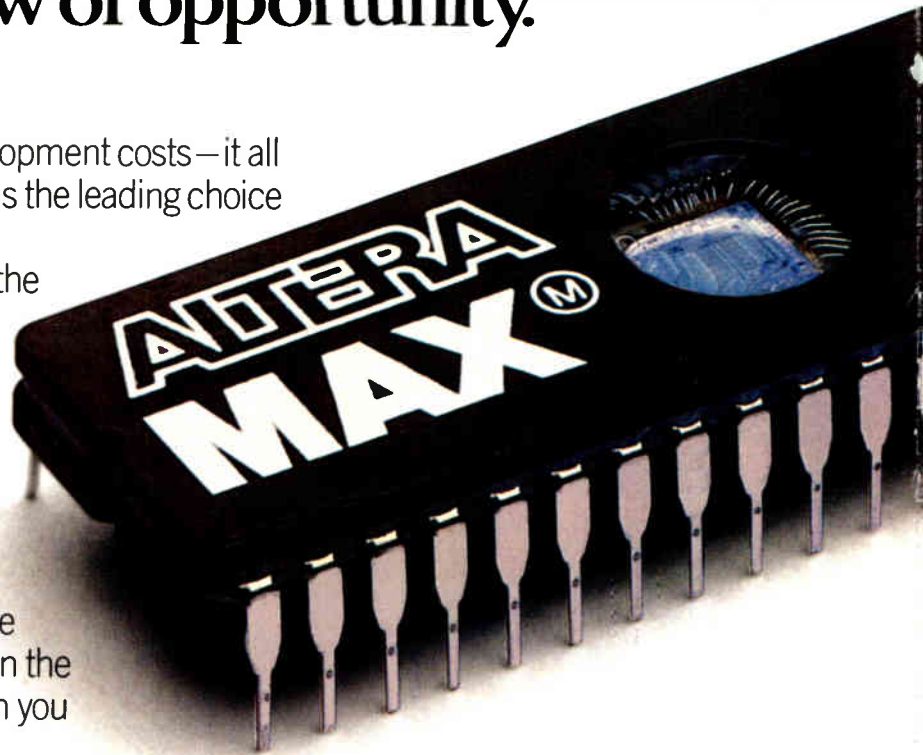
Density, speed, ease-of-use, development costs—it all points to the MAX EPLD family as the leading choice for any level of logic design.

So why not get started? Select the MAX device that's right for your application. You can choose from a family of pin-compatible devices with a full range of densities from 16 to 128 macrocells.

Get your new project off to a quick, profitable start today. And to an equally fast finish. In the U.S. call 1-800-545-3377, or return the attached reply card, and we'll rush you more information on MAX.

But do it now.

While your window of opportunity is wide open.



MAX Family Members							
Feature	EPM	5016	5024	5032	5064	5127	5128
Macrocells		16	24	32	64	128	128
MAX Flip Flops		16	24	32	64	128	128
MAX Latches <sup>(1)</sup>		32	48	64	128	256	256
MAX Inputs <sup>(2)</sup>		15	19	23	35	35	59
MAX Outputs		8	12	16	28	28	52
Packages		20D	24D	28D	40D	40D	68J
				28J	44J	44J	68G

Key: D—DIP    J—J-Lead Chip Carrier    G—Pin Grid Array  
Notes: (1) When all Expander Product Terms are used to implement latches.  
(2) With one output.

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to have the most impact on speeding the turnaround of programmable gate arrays in the 15,000- to 50,000-gate range.

To address the production cycle, makers of arrays and standard-cell-based ASICs are working on new automation strategies that will use flexible minifabs. Until relatively recently, most ASIC manufacturers have been tapping the industry's surplus of capacity, which was mostly in the form of large underutilized lines at commodity chip makers. These conventional fabrication lines are characterized by high capital costs in plant and equipment and are oriented towards running large volumes of one design at a time. But such "megafabs" are not geared towards turning out ASICs quickly, and they usually suffer low yields in small-volume runs.

So a new breed of minifabs is expected to emerge in the coming year at a cost of \$20 to \$50 million, compared to the \$200 million pricetag of larger fabs. Experts say the minifabs will consist of islands of small equipment designed for maximum flexibility. What's more, these fabs can be built in as little as six months. Chip-making companies planning these minifabs believe they will be able to use new

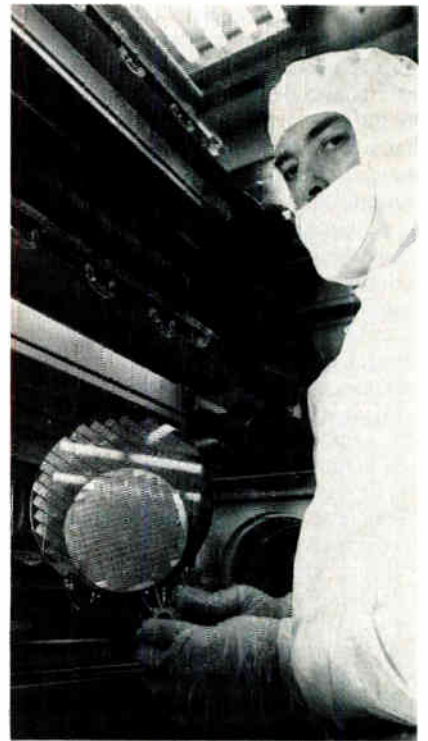
equipment and processes faster than the giant commodity-chip plants.

The smaller minifabs are expected to be the first widespread users of 8-in. slices, except for a few large megafab facilities—such as IBM Corp.'s new 1-Mbit DRAM fab in Essex Junction, Vt. The new minifab equipment's tightly controlled tolerances is also expected to pro-

**A new breed of minifabs will produce ASICs and will cost \$50 million or less**

vide high yields. Entire ASIC production runs will be completed with as few as a half-dozen 8-in. wafers. Plans for these ASIC minifabs also include direct-write systems, such as with lasers and electron-beam systems. A further motivation is that the smaller fab facilities will more quickly reach the Class 1 level of cleanroom ratings—a tenfold improvement over today's typical Class 10 megafab lines. That would result in higher yields and potentially lower costs, say production experts.

—Bernard C. Cole



IBM was the first with 8-in. wafers, but others with new minifabs will follow soon.

## COMPONENTS

# PC-BOARD SUPPLIERS LOOK FOR MATERIAL AND DESIGN GAINS

The printed-circuit board—the basic component and bedrock on which most electronics systems rest—is undergoing profound changes in structure and performance capability. Form follows function, the axiom goes. And in the case of the pc board, there is growing demand for more function per unit volume from systems manufacturers, coupled with constantly escalating requirements for high speed. That's forcing pc board manufacturers, designers, and users alike to respond with new materials, shapes and, most importantly, techniques for interconnecting the growing number of packages and components that need support.

On the way to ease board-to-board or board-to-component connections are new techniques such as a multilayer extension of tape-automated-bonding technology; a system that uses controlled-impedance microstrip flexible circuits; and a solderless scheme that is based on a liquid-crystal-polymer module. Also coming is help for makers of multilayer boards, including more manageable ultrathin copper laminates. And to release more space on

### COMING SOON

- Ultrathin copper cladding for lighter multilayer boards and easier etching
- Resistive layers that free up board space in high-speed logic systems by eliminating discretes
- Establishment of blind and buried vias as a commonplace method for forming interconnections that cut the length of lines

dense boards, new concepts in resistive-layer materials are in development.

One major factor that is influencing the pc-board evolution is the growing pervasiveness of surface-mount technology. As more and more components with hundreds of input/output pins are carried on both sides of a board, the number of in-

terconnections explode. Not only are more interconnections required, but the space between them must be drastically reduced. More pc-board layers are needed, and through-holes must be smaller, presenting new problems in plating.

The higher speeds of today's digital systems also place great demands on pc boards. Impedance of the interconnections must be controlled to avoid reflections and transmission losses. Low-dielectric-constant materials are required to reduce propagation delay and crosstalk.

"Systems designers are looking for more performance per cubic foot," says Donald J. Pucci, vice president for technology and quality at Hadco Corp., a maker of multilayer boards in Salem, N.H. "That's why the drive [is on] for surface mounting and for higher densities and speed—to get more and more performance in the same amount of space and for the same or less money."

That means more layers, explains Pucci. "In this company, we have a term we call weighted-average layer count, a mathematical expression of all the square

feet of product we ship weighted by the volume of each technology. Five years ago, our mix of products was 50% double-sided boards, 40% four-layer boards, and the balance more than four layers. So that translated to a weighted-average count of around 2.8. Today the weighted-average layer count is around 5. That's a big change and it's increasing over time."

Line width is another parameter that is changing significantly. The average line width a few years ago was 10 to 12 mils, Pucci says. "Today it's 7 mils, and we believe the average line width will be in the 5-mil range in a couple of years."

Another technical challenge is posed by the shrinking of holes imposed by surface-mount technology. Typical diameters of conventional through-holes are in the 30- to 40-mil range, and moving downward rapidly.

"From what I've seen you can't get a reliable small through-hole because of the metallization problem," says Mary Mollison, a chemical engineer with Tektronix Inc.'s printed-circuit board division in Forest Grove, Ore. "We're talking about 13.5 mils or less. You can drill them, but plating them is a big issue." As

a result, a trend is under way in multilayer boards toward more use of blind and buried vias—interconnections between the surface and inner conductive layers, or between inner layers only, she says.

"We have the process in place to do buried vias, but we're ahead of the customer base just a little bit. I've seen a lag time between buried vias and surface mount, but they are being designed in

### Resistive layers can ease board density problems, particularly in ECL designs

now on a small scale. We're seeing more interest and getting more frequent requests, typically on 8- to 10-layer boards. We're also doing test boards for some customers."

In addition, trace width and spacing have been put under pressure by VLSI components. With VLSI device packages sporting leads with 25-mil spacing, chip users have had to make reductions in board-trace width and spacing from 12/12

(12-mil traces and 12-mil spaces) to 8/8. And 4/4 is just around the corner, adds Mollison.

Thus the push for higher density and more performance is stressing interconnection problems of pc boards in two dimensions: internally, between layers, and externally between board and component or between boards. Board makers, material suppliers, and designers are responding in a variety of solutions to the problem.

One help for makers of multilayer boards is coming from M&T Chemicals Inc., a supplier of processes and materials for pc-board manufacturing. M&T has developed Metclad, an ultrathin copper foil laminate offered as an alternative to the typical 1/2- or 1-oz copper laminates. In addition to making lighter and thinner multilayer boards possible, at 2- to 5- $\mu$ m thick, Metclad also helps solve the problem of loss due to prolonged exposure to etching, which is exacerbated in thicker copper due to undercutting of very fine lines at high density.

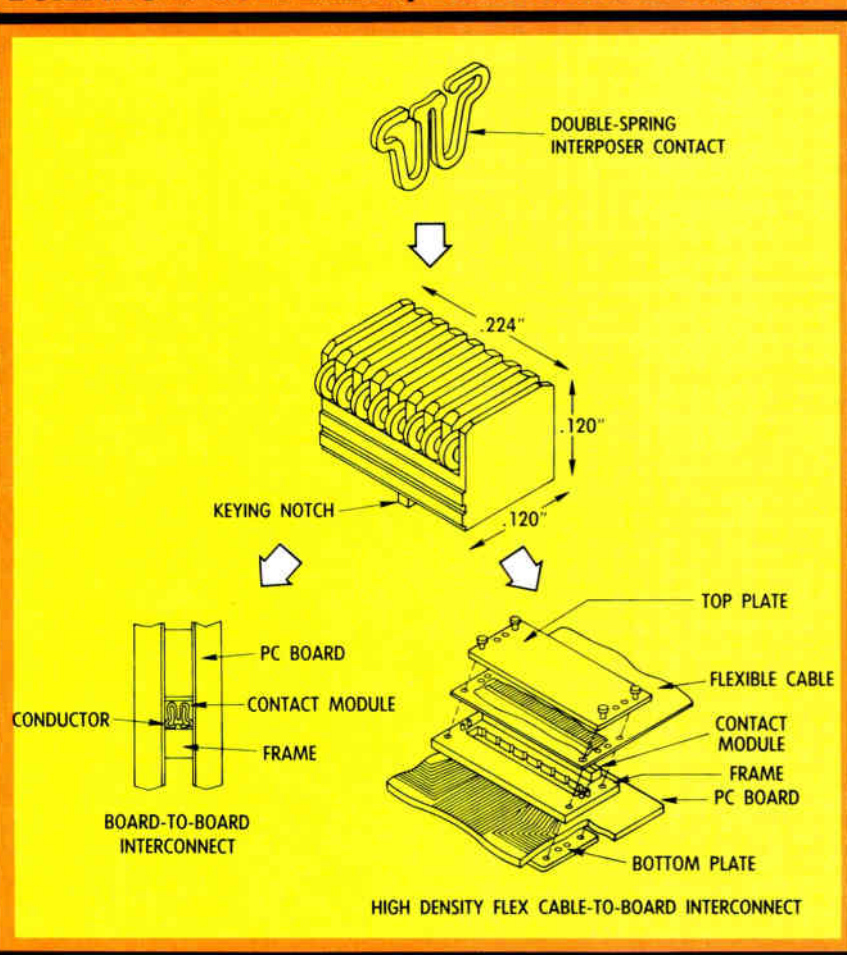
Because of the difficulty of handling ultrathin copper foil, it previously had to be plated onto an aluminum foil substrate, says Ralph Nussbaum, general manager of the M&T's pc-board systems business. After lamination to the board, the aluminum backing then had to be removed, which was a tedious process. "We have developed a proprietary technique where we plate copper directly on the stainless steel plates used in the lamination process," he says. "That's laid up in the hydraulic press along with the glass epoxy prepreg [glass fabric preimpregnated with a glass epoxy resin], and under temperature and pressure during the press cycle, the copper is transferred to the laminate without any prior release." The result is a high-quality defect-free copper surface that can be etched without high-yield loss due to etching, and where high-density traces with highly controlled dimensional tolerances to achieve uniform impedance.

**ELIMINATING RESISTORS.** Resistive layers laminated within the board can also ease board-density problems by eliminating the need for hundreds of terminating resistors usually required in high-speed digital boards, particularly in emitter-coupled logic designs.

A leader in developing the concept of resistive layer materials is Omega Technologies Inc. of Culver City, Calif. The firm's product, called Omega-Ply, is a combined materials and processing system using thin-film technology for incorporating resistor-conductor networks in pc boards, either on the surface or on internal layers.

The material is made up of an insulating substrate with a bilayer cladding of copper and nickel-alloy thin film on one or both sides. Patterns of resistors and conductors can be etched to produce circuits

## BUILDING A SOLDERLESS, DEMOUNTABLE SYSTEM



The Interposer solderless system from Amp Inc. uses double-spring contacts on 20-to-25-mil centers in a liquid-crystal polymer module to provide tight, low-resistance contacts.

with integral resistors using easily modified conventional printed-circuit processes. In high-speed digital electronics, the system is ideal for forming pull-up/pull-down resistors on open collectors or gate inputs, and as line terminators to match impedances.

Other uses are popping up too as computer systems emphasizing speed are made with new materials. "As super-minis, minis, and minisupers go to higher and higher speeds with the use of ECL, high-speed CMOS, and gallium arsenide, which require lots of terminating resistors, the technology is being used more and more to release more space on densely populated boards," says Bruce Mahler, Omega's vice president of sales and marketing.

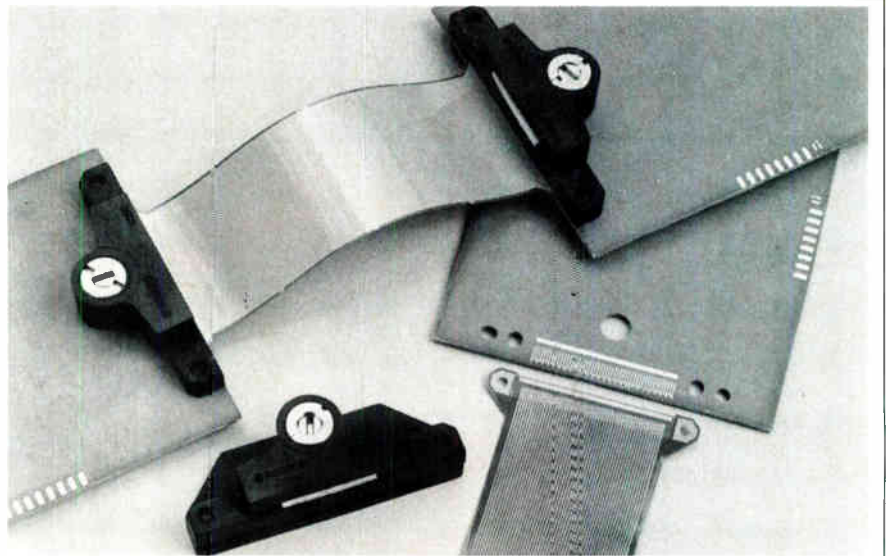
Omega-Ply has been available with resistivity of 25 and 100  $\Omega$  per-square. And 1,000- $\Omega$ -per-square materials have just been made available.

The combination of increased density and the short signal rise times of high-speed digital circuitry has substantially worsened the interconnection problem. Conventional connectors such as post-and-box types or pin-grid arrays give rise to high crosstalk, pulse-shape degradation, and reflections due to impedance mismatch. Today's state of the art is about 2,000 I/O pins for a 100-chip substrate about 16 in.<sup>2</sup> in area, points out a paper given recently at the 1988 Electronic Components Conference by Tom Chung and R. T. Smith of the Microelectronics and Computer Technology Corp., where an interconnection program is showing progress. Available logic families often require that interconnects for such assemblies must handle signals with rise times as short as 1 ns and maintain crosstalk values below the threshold of the devices employed.

A number of new approaches to board-to-board and component-to-board interconnections have been developed in response to these interconnection problems. They include a system that is essentially a multilayer extension of tape automated bonding (TAB) technology at the MCC, a system that employs flexible interconnects from Rogers Corp., and a system developed by Amp Inc. that is based on a liquid-crystal polymer module.

Chung, who heads MCC's Packaging/Interconnect Program in Austin, and Smith, who is assigned to the consortium as 3M Co.'s liaison representative, have developed the system with TAB technology features. It can be used to make permanent or demountable connections.

In MCC's system, vias placed on polyimide tape are used to fabricate either raised contacts for demountable connection, or bonding sites for permanent attachment to a substrate by thermosonic bonding. The raised contacts are in the form of bumped pads plated with noble



**Rogers Corp.'s Invisicon system**, shown here in a board-to-board connection, is designed to handle fast digital electronics where high circuit density and controlled impedance are vital.

metal that can be clamped in position over suitable receptor sites on the substrate. The traces are in the form of a microstrip, which requires a second metal-layer ground plane.

One advantage of using TAB tape is that a great deal of TAB-assembly technology is available, Chung says, "We are basically replacing the pin socket, which has density limitations of about 150 I/Os per square inch." The MCC demountable connection is

### Three new schemes are attacking the interconnection problems of fast chips

equivalent to 1,250 contacts in.<sup>2</sup>

The MCC system is characterized by a trace width of 2 mils, and race spacing on 5-mil centers. Ground planes are of 1/2-oz. copper. The tape can be 35 or 70 mm or any other format, Chung says. Measurements on experimental tape constructions show 10% cumulative crosstalk from pulsed edge transitions as fast as 100 ps—good enough for a variety of high-speed applications, he adds. But much work remains to make the system manufacturable in volume.

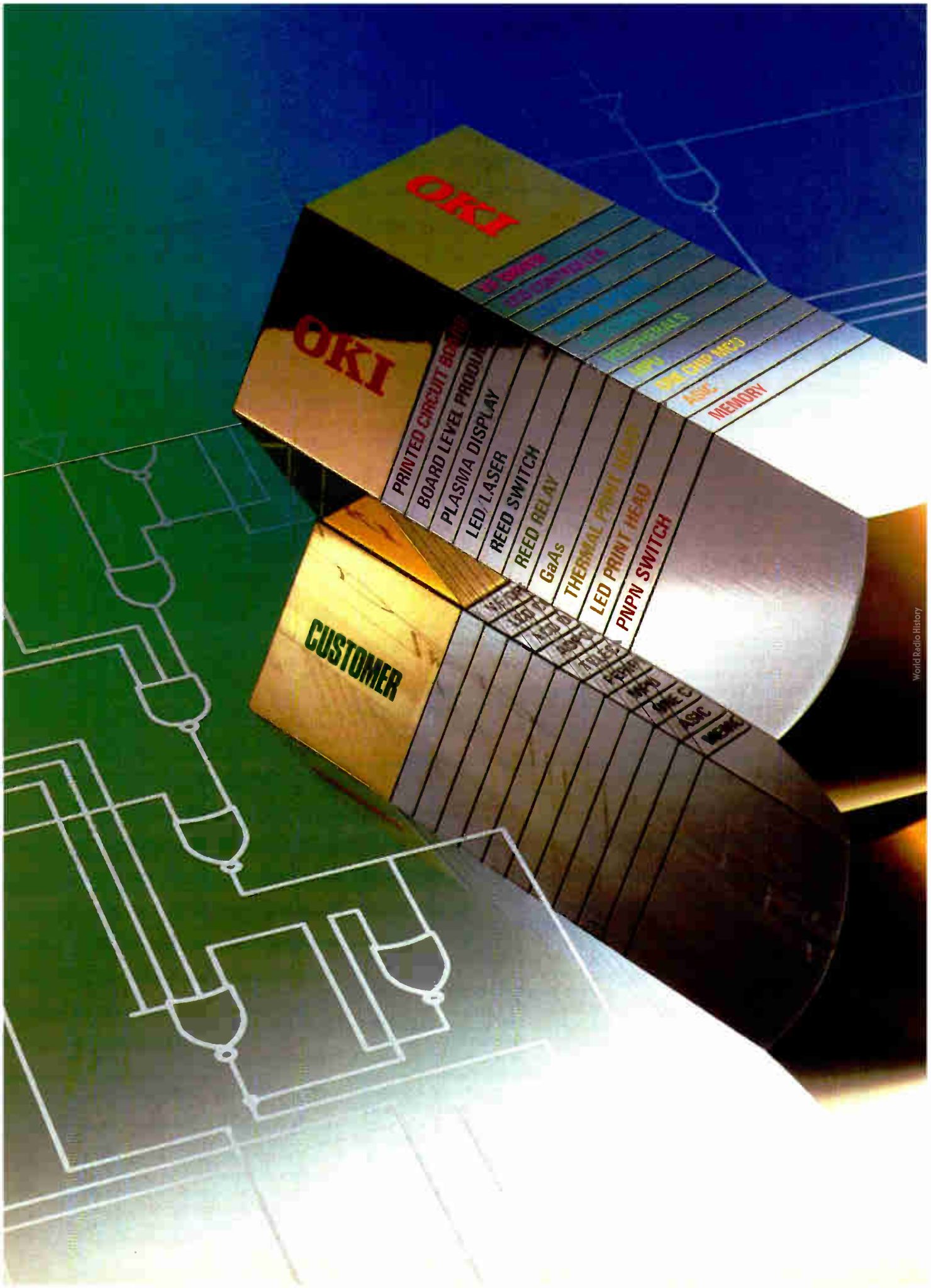
A similar high-density, high-performance system that employs flexible interconnects has been developed by Rogers. The Invisicon interconnection system also uses controlled-impedance microstrip or stripline flexible circuits and a pressure-mated pad connection to another flexible circuit or circuit board (see photo, p.109). Rather than using polyimide tape, the Invisicon uses a low-dielectric-constant microglass-reinforced fluoropolymer composite, RO2500, developed by Rogers.

The Invisicon system has achieved contact-resistance values of less than 10 m $\Omega$

and board-to-board impedance mismatches of 5% to 10% at rise times of 50 ps, using a trace pitch of 25 mils, says Steve Lockard, Rogers' market development supervisor of the flexible interconnections division in Chandler, Ariz. Wiping contacts of 25-mil spacing and nonwiping contact pitches of 15 mils have been proved out and 10-mil spacing is in development, he says. But the difficulty lies in learning how to register hundreds of fine lines across a couple of inches of tape and make contact to all of them.

"One idea we're working on very hard today is to come off a 15-mil or 10-mil pitch with hundreds of lines on a multi-chip module down to a circuit board, which can handle at best 25-mil pitches, and you're trying to fan out while controlling the impedance match through the interconnection," says Lockard. "Right now, our module-to-board Invisicon system can convert from a 12-mil pitch at the module side to a 25-mil pitch at the board side. We've designed an interconnection with 800 signal I/O ports coming off a 4-in.<sup>2</sup> module with a 12-mil pitch to a board having 25-mil pads."

**SOLDERLESS.** A prototype of a different approach to the interconnect problem has been developed by Amp of Harrisburg, Pa. Called the Interposer contact system, it is based on a liquid-crystal polymer module containing 8 to 10 contacts on either 20- or 25-mil centers. In this solderless-interconnection scheme, the contacts use a high-normal-force double-spring design with wiping surfaces. Interconnection is achieved through compression of contacts between parallel mating surfaces. The signal path through the contacts provides extremely low inductance and capacitance through an extremely short signal path. The system can be used for interconnecting board to board directly or high-density flex cable to boards. —Samuel Weber



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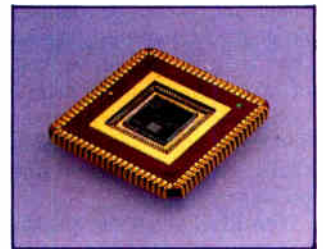
*The solution is at hand, with parts, design and production assistance from OKI*

OKI is ready to help you speed product development, improve your production efficiency and shave costs with integrated system technologies and constant technical support. OKI is more than a one-stop source of the highest-quality electronic devices and state-of-the-art ASIC design and production. We provide total project assistance, from design and manufacturing of system components and modules to technology assistance, available at any development stage, through design centers in the U.S., Europe, and Asia.

## *100K-Gate Super Integration*

The OKI advanced ASIC line-up now includes high-density channelless gate arrays. With our automatic test generation, they can help you break through the new-applications design bottleneck.

OKI leadership in advanced IC manufacturing is based on a commitment to the future — through the development of 4M DRAMs, a submicron CMOS process, and now, design and production of high-density channelless gate-arrays.



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# IT'S A THREE-WAY FIGHT IN HIGH-PIN-COUNT IC PACKAGES

Some big changes are coming in fine-lead-pitch flatpack packages for VLSI circuits. Three new families of 25-mil pitch, gull-wing leaded plastic packages—one from Japan and two from the U. S.—are now vying for a dominant position in surface-mounted printed-circuit boards of the future. These new families can handle VLSI chips with more than 100 input/output connections apiece, whereas 50-mil packages will still be limited to I/O counts of 68 to 84.

Chip users who make the switch to these new packages will have to adopt new soldering and IC-placement techniques as well as fine-line inspection systems. But packaging experts say the fine-pitch, gull-wing flatpacks will be worth the trouble. Among their advantages are fewer chips (due to multifunction VLSI), faster speeds, and higher board density.

The drive for fine-lead-pitch chip carriers comes from the need to keep packages small while supporting increasing I/O lead counts in the VLSI age. The 50-mil-pitch leaded chip carriers populating today's pc-boardscape will no longer do. To remedy this situation, the Electronic Industries Association of Japan, the Joint Electron Devices Council in the U. S., and National Semiconductor Corp. of Santa Clara, Calif., each have devised finer-pitch package types.

The EIAJ and Jedec packages are based on standard IC assembly techniques, while the National package is based on tape-automated bonding. The latter is smaller, in general, for the same lead count as the other two, but requires the use of special excising and lead-forming production equipment.

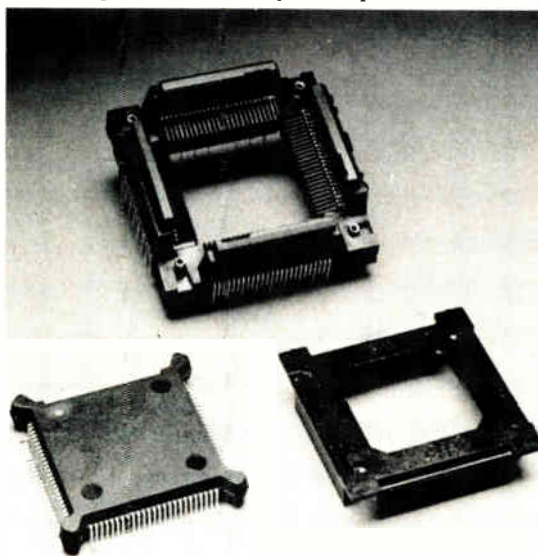
**IN JAPAN.** Plastic quad flatpacks are coming on strong in Japan, where they are finding use in consumer electronics, as well as doing well in a number of surface-mounted chip systems in the U. S. Backed by the EIAJ, the plastic quad flatpack family comes in both square and rectangular shapes; standard package sizes are fixed while the lead pitch and I/O counts change. Among the most popular types in the EIAJ-backed family are square-shaped flatpacks with lead counts of 32 to 240 and pitches of 31.5 to 25.6 mils.

Although the EIAJ packages are space-

## COMING SOON

- An explosion of fine-pitch plastic packages for high-lead-count integrated circuits
- Advances in board-assembly systems fueled by the payoffs manufacturers get from greater IC-packing densities

efficient, they must be handled in special trays or carriers to prevent lead damage. In addition, the wide range of lead lengths, terminal lengths, and package thicknesses of the variable-pitch package family make it impossible to use standard chip sockets. The layout of pc boards is



This Jedec-backed plastic quad flatpack from National Semiconductor has corner bumpers that aid handling.

also complicated because there are no standard chip footprints with the family.

These problems led Jedec to create a new family of plastic flatpacks sporting gull-wing leads on 25-mil centers. The Jedec-backed flatpack has a constant pitch but variable body size. Intel, Motorola, National Semiconductor, and Texas Instruments are already supplying products in this package type, and much of

the IC industry appears to be ready to adopt the new package. Tooling now exists for the line with 84, 100, 122, and 164 pins, and more is on the way.

A key feature of the Jedec plastic quad flatpack is the special "bumper" located at each corner. The bumpers—along with tight dimensional tolerances—make the packages easy to handle with automated assembly equipment.

Connector manufacturers such as Amp, 3M's Textool Test and Interconnect Products division, and Texas Instruments have already designed standard sockets for Jedec's bumpered quad flatpack. Assembly equipment houses have also designed handlers for the packages.

A second U. S. fine-pitch package emerging is National Semiconductor's TapePak family, which is based on chips mass-bonded to microinterconnections on an all-copper tape. The outer lead pattern of each frame is the final package's outer leads. A square package is molded over each chip along with a protective outer ring. Presently, only National and Motorola are tooled for this package, but TI is considering it for high-density memory packages. In addition, General Motors Corp.'s Delco Electronics unit will produce TapePak packages for internal use.

Regardless of which fine-pitch package is selected, challenges face the chip customer in making the shift from 50-mil chip carriers to the new flatpacks. For example, soldering and circuit placement of the new fine-pitch packages are extremely difficult. In soldering, the closeness of the leads makes them susceptible to solder bridging. To overcome this, it is necessary to go to special thin solder stencils and vision-system-augmented solder screeners.

Many experts in surface-mount technology believe that only the thermode or hot-bar methods are appropriate for lead pitches below 25 mils. This type of soldering is routinely done on leads on 8-mil pitch in tape-automated bonding. In placing the new fine-pitch carriers on board-pad patterns, highly accurate pick-and-place machines will be needed to reach positional accuracies of 1 to 3 mils and rotational accuracies of 0.05 to 0.1 degrees.

—Jerry Lyman

# IRONING OUT BUGS FASTER IN TOP-END LOGIC, ASIC CHIPS

It is a costly irony. The task of designing with today's fast, complex CMOS and bipolar circuits is slowing down product development. And delays experienced in product introductions are costing systems houses more money than ever. A major culprit in these delays is the need to rework designs to correct for secondary analog effects popping up in digital signals as clock rates become faster.

In the year ahead, computer-aided-design and -engineering systems companies will tackle that problem with new tools. Their aim will be to anticipate those troublesome secondary analog effects before prototype products are made.

Faster product turnaround is also the goal of new virtual in-circuit emulators. The emulators will be used to debug code as software and hardware engineers work in parallel on application-specific integrated circuits with embedded microcomputers. And look for the spread of logic synthesis to quicken as CAE vendors tie these tools into their software environments and synthesizer suppliers strike deals to offer design libraries with their products. CAE houses are also expected to load up their packages with a variety of new functions, like thermal-analysis aids, to enable fast board development.

**SPEED CHALLENGE.** The push for fast design turnaround comes from profit pressures. If a manufacturer ships a product six months late he can kiss a third of the expected profits goodbye, according to McKinsey & Co., a market research firm in Boston. The urgency to get products to market faster is driving CAE and CAD technology towards tools that not only speed up individual steps in the design process but also improve the throughput of the process as a whole.

One factor in the increasing number of design iterations is the problem of dealing with high-speed CMOS and emitter-coupled logic. Because of the high operating frequencies, the analog components of digital signals have begun to affect circuit functions, says Geoffrey Bunza, director of engineering at Mentor Graphics Corp. in Beaverton, Ore.

Others agree. Clock frequencies of standard components, such as the Intel Corp. microprocessor family, have steadily increased over the past 10 years, says David Stamm, executive vice president of

## COMING SOON

- New simulation tools that cut the number of design iterations for fast digital systems by anticipating secondary analog effects
- System-level simulation capabilities that bring more front-end analysis to the product-development cycle
- Design packages that are better integrated with the disparate functions of board layout, thermal analysis, and emi checks

sales and marketing at Daisy Systems Inc. in Mountain View, Calif. The frequencies reached 33 MHz last year and the trend is expected to continue.

At 33 MHz, a digital pulse begins to

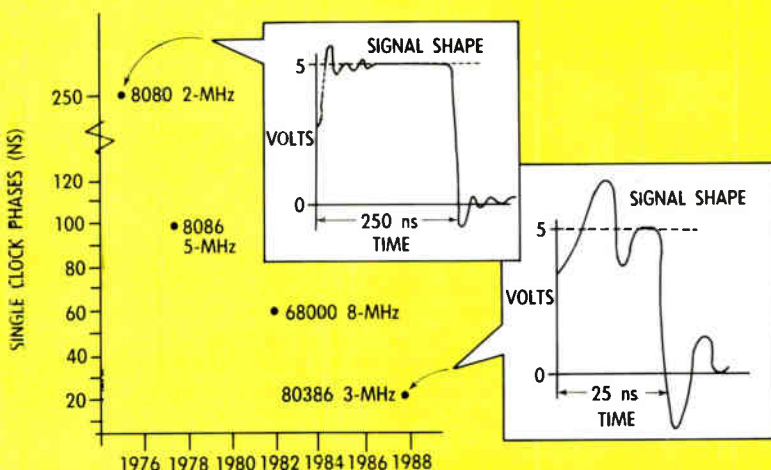
have noticeable secondary sinusoidal analog effect. The oscillations known as ringing, which occur whenever the signal goes from one logic state to another, do not have time to settle down before the next state change hits. Setting logic thresholds and setup and hold times becomes very tricky because the signal can not be counted on to hold steady at a given logic level for a significant period within the clock cycle.

What is needed is a method of "teaching" a digital simulator about analog effects so they can be taken into account in the design-simulation process, Stamm says. This way the analog effects won't be left for discovery during the design debug phase after boards are prototyped.

In the past, analog and digital simulators have been used together, but only in a limited way. The analog tools have not generally been applied to the analog characteristics of digital signals: they have been used only on the analog sections in a mixed analog/digital design.

One block to the use of analog simula-

## ANALOG EFFECTS GROW IN FAST DIGITAL SIGNALS



SOURCE: DAISY SYSTEMS

**Ever faster clock rates** of microprocessor systems are changing the shape of digital signals, opening up a new need for design systems that anticipate unwanted analog effects.

tors in the digital side of a design is the need for more computer power. It can literally take months to analyze a complex digital design with an analog simulator. The lack of adequate models of high-speed digital circuits—models with the analog effects built in—has also held up the application of analog simulators to the design's digital side, Bunza says.

But new platforms—such as the Series DN10000 from Apollo Computers Inc. of Chelmsford, Mass., and the faster version of the Sun 4 planned in 1989 by Sun Microsystems Inc. of Mountain View, Calif.—will soon start addressing the question of available computation power. Also in 1989, Mentor Graphics' Bunza expects to see new tools to create the kinds of models needed to carry out these larger simulations. Simulators will be able to perform more digital and analog analysis as well as timing and fault analysis. Mentor plans to do just that with the use of analog expertise the company gained in its purchase of the CAE Division of Tektronix Inc., also of Beaverton, Ore. Mentor also gained access to analog modeling tools through its acquisition of Contour Design Systems Inc. of Menlo Park, Calif.

But it's not just that analog simulation must be done for digital circuits; new functions must be added to the simulation environment to handle large high-speed designs. Another challenge is dealing with the effect of power surges from a large number of devices switching simultaneously on 32- and 64-bit wide buses, Daisy's Stamm says. Up to now, static tools separate from simulators have been used to analyze these effects, Stamm notes. But a more complete solution is a simulator with integrated dynamic tools, such as dynamic timing analysis, he says. This capability lets a user tackle another sticky design debugging problem, that of reconvergent fan-out, where a pulse fans out from a common source through more than one set of logic circuits and the signals that result come together later at another location. Such a circuit is susceptible to glitches that are difficult for current-generation simulators to model adequately.

**SERIOUS TASK.** New facilities for embedded-microcontroller ASIC designs will also soon be built into simulators, say CAE experts. Chip customers are moving towards greater use of ASICs that contain a microcontroller as a core cell. These ASICs face a serious problem: with customized circuitry surrounding it, the microcontroller is often inaccessible to in-circuit emulation systems, the most common tools used to debug the firmware code that executes on microcontrollers. Furthermore, code must be debugged before the ASIC is in silicon, because the

firmware will be a part of that silicon.

It's simpler for board-level microcontroller design: a software engineer programs the first pass of his code into a programmable read-only memory; it is then plugged into a prototype board and the code is debugged with an in-circuit emulator as the code is executed. But for an ASIC with an embedded microcontroller, code must be developed and debugged in some other way, before the chip itself is implemented. This problem will be addressed next year by new tools called virtual in-circuit emulators, says Stamm.

One approach to the problem has al-

One essential element in making system-level simulation generally available is more modeling capability. A high-level modeling language that allows users to create a model of each ASIC that goes into his final system before design begins is available from Silicon Compiler System Corp. in San Jose, Calif. These models can then be used in a system-level simulation to perform extensive "what-if" analysis before any chip is implemented, says Misha Burich, the company's vice president of engineering. Proprietary behavioral-description languages are widely used today, but more CAE vendors will offer systems using the

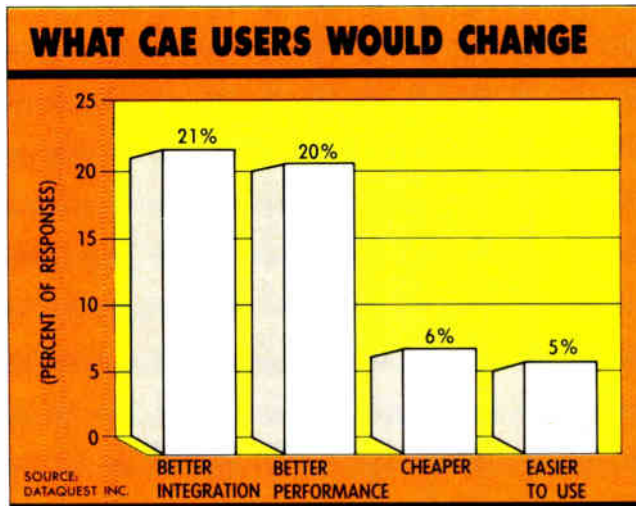
Pentagon's VHSIC Hardware Description Language, or VHDL, which is emerging as an industry standard.

As high-level system simulation comes into broader use, it will have another extremely important result that will speed up system design. If high-level-language chip descriptions used for such simulation can be provided to a logic-synthesis program, that tool in turn will produce an optimized logic design ready to be laid out. Logic synthesizers can remove a huge part of the drudgery involved in designing digital systems. Daisy's Stamm says logic synthesis will be an essential part of a CAE vendor's tool kit in 1989.

So in the coming year, experts tracking the field expect major CAE vendors to offer more logic synthesizers. They will be either internally developed or acquired from independent logic-synthesizer suppliers such as Algorithmic Systems, Silc Technologies, Synopsis, and Trimeter Technologies.

One factor that will encourage these relationships is the synthesizer supplier's need for cell and macro libraries. During the logic-synthesis operation, a user specifies a new design using a hardware description language, Boolean expressions, or some other form of input. From this description, the synthesizer creates the circuit and then performs logic minimization to make the design as efficient as possible, given the constraints of speed and chip area. Then the synthesis program must map this design into actual gates for a particular ASIC foundry using that foundry's cell or macro libraries or the libraries of independent CAE equipment suppliers such as Daisy, Mentor, Valid, and others.

Foundries have no economic incentive to make their libraries available to the independent synthesis suppliers. But the CAE systems house, whose systems are used to design the chips the foundry builds, can develop relationships with the synthesis-tool vendors on the one hand and the foundries on the other, bringing



ready been brought to market by Interact Corp. of New York City in a product called System Design Environment. By using a model of the microprocessor in a CAE system's logic simulator, the system lets the designer load software the processor will

### Simulators will be able to perform more digital and analog analysis

run into the simulator; that code is then used as stimulus patterns to the microprocessor model during simulation. A symbolic debugger monitors and controls the execution of the simulation. It can examine processor memory, input/output registers, and internal registers once a breakpoint is reached. All of this analysis can be performed before a design prototype is created, reducing the number of hardware changes in development.

This system-level simulation of hardware and software is indicative of a trend towards doing more analysis before a design's implementation. "Designers want to analyze more of a design," notes Bunza. "The designer wants to model the entire system, and this means an order-of-magnitude increase in complexity for the tool supplier."

the two parties together.

After the front-end design work is completed, design rework is often caused by the problems of handing off a project from one group of engineers to another, says Kenneth Willett, founder and development engineer with Mentor Graphics Inc. in Beaverton, Ore.

The system designer hands off his debugged design to a board layout engineer. After layout, the original system engineer must then verify that the layout will not affect the design performance. The laid-out design then goes to engineers who perform thermal analysis and electromagnetic-interference analysis. Each of these handoffs can represent one or more design iterations—the board layout may have to change to reduce board hot spots or to eliminate emi from board components interacting and producing high levels of radiation.

To reduce the number of iterations, many design systems will be equipped with new abilities to direct component placement and routing. Although the front-end designer using these tools will not have to perform detailed layout, he will use them to pass along guidelines that the layout engineer needs, says Richard Oettel, chief scientist at Seattle Silicon Corp.

With the Bellevue, Wash., company's ChipCrafter system, a designer can specify critical paths, which must have some minimum timing, and the layout engineer is left with placement decisions to achieve this result, Oettel says. He says the designer will be given even more capability to make general specifications about a design that the layout engineer will use to guide his layout.

**MORE INTEGRATION.** The thermal-analysis and emi engineers will have similar tools enabling them to indicate to the layout engineer component placement and routing that can produce thermal or emi problems. In order to achieve this interaction level, however, the entire process must become more integrated. Not surprisingly, better integration is at the top of the priority list of CAE system users, according to a survey by Dataquest Inc. of San Jose, Calif.

One area that lacks sufficient integration is the process of thermal analysis. Today's stand-alone thermal-analysis packages require data on the board layout from engineers, as well as operating characteristics of each board component from the designer.

Next year, CAE systems will have integrated relational data bases containing all of this information, predicts Jeff Edson, director of the electronics division of Integraph Corp. in Santa Clara, Calif. In the Integraph system, he says, data bases will contain the logic-simulation models, Spice models, reliability data, TTL Data Book data, and, eventually, emi information.

—Jonah McLeod

## TEST & MEASUREMENT

# THE CHALLENGE IS TO KEEP UP WITH FAST CIRCUITS

A common thread running through the field of test and measurement equipment next year will be the mad rush to keep pace with performance advances in digital and analog electronics. Instruments are struggling to keep up with industry's move to faster chips and systems. But other kinds of trends, such as to new standards for instrument-on-a-card systems and the need to cope with the latest frequency-hopping radio and radar products, are also driving changes in instrument technology.

Digital designs are getting faster—clock rates have doubled in the past couple of years. They also have much wider data paths—16-bit buses of a few years ago have given way to 32-bit buses today. In response, logic analyzers will acquire oscilloscope characteristics—and vice versa—to better debug high-speed, wide-bus designs. Probes, a major weak point in instruments in general, will improve to keep pace with performance advances in the basic instrument. Next year will also see counter/timers that can more accurately measure the timing of signals in supercomputers with very fast clocks.

Instrument-on-a-card systems built to the VXI specification (for VME extensions for instrumentation) will debut in 1989 for design verification and manufacturing test of faster digital systems. For rf and microwave analog systems, instruments like digital spectrum analyzers will become available for characterizing the newest frequency-hopping radios and radar systems. And keeping instruments in the field at peak performance will be new technology to make calibration more convenient, more automatic, and more accurate.

The world of analog rf and microwave measurement is a foreign one to the digital designer, but increasingly this world is infringing on digital circuit designs. The analog effects inherent in digital signals of high-speed CMOS and ECL logic are beginning to affect circuit performance, says Robert Bousquet, marketing manager at Tektronix Inc., Beaverton, Ore. Digital systems using these fast logic types are creating a need for logic analyzers with oscilloscope capabilities, and

vice versa. A logic analyzer with what amounts to a digitizing scope built in can be used to look at signal shapes to examine analog components of digital signals more closely, says Tom Long, vice president of Tektronix's Technology Group.

Likewise, an oscilloscope with the large number of channels common to logic analyzers can allow a designer to more easily

verify high pin-count designs. One example of this trend is found in the Tektronix 11800 series oscilloscope when equipped with its multichannel plug-in module, the 11801.

With the module, the 20-GHz digital oscilloscope can view 136 channels at once with a timing resolution of 1 ps on

all channels. This resolution is an order of magnitude better than what's available on big ATE systems. Increasingly, scopes like the 11800 series will be used in conjunction with logic analyzers and verification systems during debug of application-specific integrated circuits.

**TRADING FEATURES.** Logical triggering is another capability that will be coming to oscilloscopes—especially digital ones—from the logic-analysis realm, says Thomas Saponas, marketing manager at Hewlett-Packard Co., Palo Alto, Calif. It will allow a scope to examine selected events in a digital system; for example, when a microprocessor executes an interrupt routine to handle an RS-232-C communications link.

Such capability convinces Saponas that 1989 and beyond belongs to digital oscilloscopes, although there will still be market niches in which analog scopes will find application, he says. There are digital scopes with time bases 1,000 times more accurate better than those in analog scopes, he observes, thanks to the crystal-controlled oscillators used in digital-scope time-base electronics in place of the RC oscillators used in analog scopes. With better control of timing, the digital scope can make very accurate delayed measurements. Thus, for example, it can measure the width and position of a bit in the middle of a long bit stream—like the synchronization pulse in an extended

### COMING SOON

- Logic analyzers with oscilloscope functions to better debug high-speed, wide-bus designs
- Instrument-on-a-card systems, built to VXI specification, for design verification and test of digital systems

stream of communications data.

New logic analyzers in 1989 will be able to handle the latest high-performance microprocessor-based systems, including systems based on the new crop of reduced-instruction-set chips. These instruments continue to get faster clock speeds, more channels for wider buses, and deeper capture memory.

Analyzers are being drawn into service for system-level analysis more and more often, says Charles Wiley, logic solutions marketing manager at Tektronix. Currently, system-analysis capability is available on high-end systems, such as Tektronix's top-of-the-line DAS 9200 products and the Hewlett-Packard HP16500. In 1989, the trick will be to provide this kind of high-level functionality at the lowest possible price.

In the under-\$10,000 range, for example, Robert Roth, product manager at the Philips T&M Group of John Fluke Manufacturing Co. in Everett, Wash., says that the company's PM3655 logic analyzer announced in June was the first to provide 100-MHz state analysis capability on an instrument with up to 96 channels. Previously, 100-MHz capability was available to perform timing analysis and 80 channels was considered a big number.

The Philips/Fluke instrument also comes with 2-Kbit-deep memory per channel at a time when the industry is shipping most systems with channel-memory depths of only 512 bits. Next year will see a competitive response to the Philips instrument in this price range.

An analyzer with a large number of channels can analyze the workings of multiple processors in a large system. In addition, deeper memory allows the instrument to capture many more CPU cycles before and after a trigger event. This lets the user view the movement of data in and out of registers, for example, and from this make faster determinations about system operation. Logic analyzers with vastly increased channel memories will come out next year to allow recording of system activities over extended periods of time.

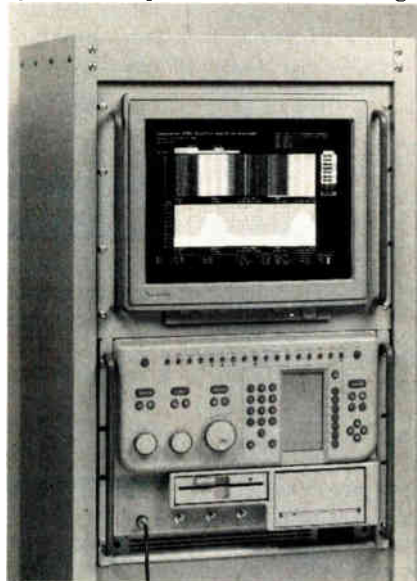
The ability of logic analyzers and oscilloscopes to handle higher-speed, wider-bus digital designs is also being affected by probe technology. RISC microprocessors implemented in CMOS will hit the market next year with cycle times on the order of 30 ns, Saponas says. It was only five years ago that ECL circuits were the only ones able to operate at these speeds.

High-impedance probing for CMOS is needed to reduce circuit loading, which affects the operation of the system being probed and thus lowers measurement accuracy. Today's probes have capacitive loading on the order of 40 to 50 pF, says Bill McAllister, DAS marketing manager at Tektronix. The state of the art in capacitive loading of a probe, 1 pF, is available on Tektronix's high-end DAS92HS8

2-GHz logic analyzer. In coming years, midrange instrument probes will offer loading in the range of 10 to 20 pF.

However, there is a limit on the bandwidth of oscilloscopes with high-impedance probes: they top out at about 300 to 500 MHz. In 1989 there will be more efforts to use low-resistance probing for high-speed CMOS logic. But to make low-impedance 50- $\Omega$  ohm probing possible in CMOS logic, says Saponas, designers must build precision resistor-divider networks into their chips, a major drawback.

Another type of instrument is responding to the rising clock rates of computer systems. Computers that will be in design



**Future testers**, like this Tektronix analyzer, will test frequency-hopping radios and radar.

in 1989, especially new supercomputers, will need instruments that can measure time very accurately. There is a lucrative market niche developing for high-speed counter/timers for measuring both time and distance with great accuracy, says Dennis Leisz, president of Wave Technologies Corp. in Plymouth, Minn.

**BETTER RESOLUTION.** Counter/timers on the market are just not up to the task, he says. The high-end products currently on the market have resolutions on the order of 10 ps and must take hundreds of thousands of samples to achieve the 10-ps performance. What Leisz says is needed is the kind of instrument his company is bringing out, the \$30,000 Timing Measurement Instrument. It has a resolution on the order of 850 fs, which it achieves with a single sample, and it can improve on that resolution by taking multiple samples.

A designer using such a high-resolution timer can better characterize the signal paths of a high-speed computer. Improving performance as much as 10% at the high operating speeds of supercomputers, which can be done in part through high-accuracy timing measurements,

adds a great deal of computing power to the end product, Leisz points out.

One thing the instrument can be used for in supercomputer applications is accurately measuring cable lengths. Using what Leisz says is a new technique for time-domain reflectometry, the instrument measures the time it takes a pulse to propagate down a length of cable in picoseconds and from this calculates the length of the cable.

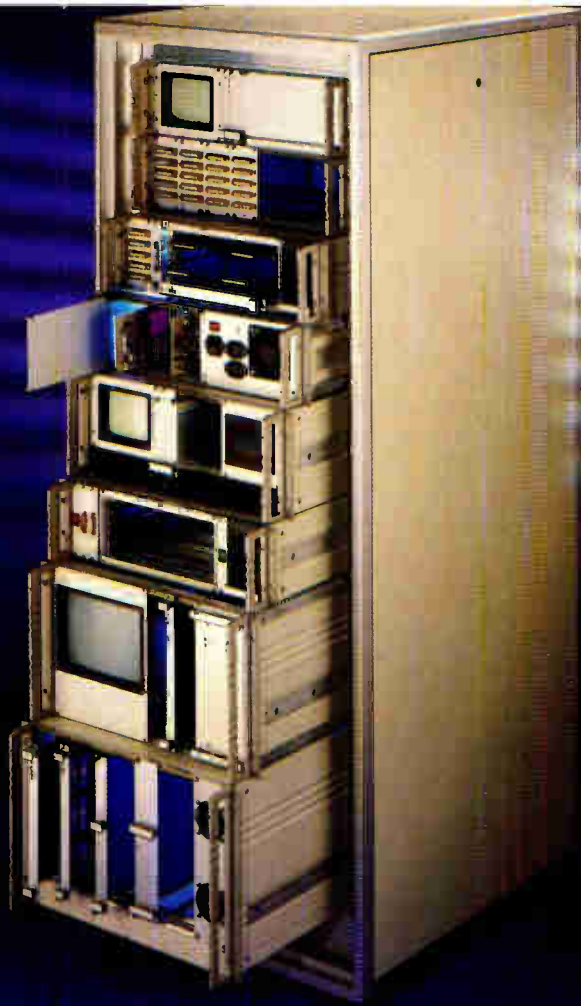
The Wave Technologies product is one of many specialized tools a test engineer needs to perform his broadening general-purpose test function. The currently popular way to combine these tools is to build "rack-and-stack" systems containing a controller and a collection of instruments connected over an IEEE-488 instrumentation bus. But such systems fall short when it comes to testing the higher-performance systems being built today.

Many of the shortcomings inherent in the rack-and-stack approach are being addressed by up-and-coming modular instrument-on-a-card test systems. In 1989, chassis and instrument cards for the VXI specification, which was developed by a consortium of instrument companies, will start hitting the market. VXI permits custom configuration of higher-performance, more tightly integrated, and more compact test systems than is possible with IEEE-488 instruments.

At the Autotestcon '88 conference held Oct. 4 to 6 in Minneapolis, Minn., Hewlett-Packard, Tektronix, and Colorado Data Systems each are introducing a VXI chassis. Instrument manufacturers, including chassis makers, will begin making cards to plug into the various chassis.

Al Schamel, measurement system division engineering manager at Tektronix, says that with VXI, data-transfer rates between instruments can hit 1 gigabyte/s. For very precise triggering of multiple instruments, VXI has a provision to skew the trigger from instrument to instrument to compensate for varying cable lengths from the trigger source; this function adds greatly to overall system timing accuracy, which is needed for work on high-speed systems. The standard VXI chassis also has provisions for shielding to prevent electromagnetic interference—radiation emissions from one instrument affecting the operation of an adjacent unit.

VXI systems bring higher-performance testing to the modular test field, but the requirement for speed finds its ultimate expression in rf and microwave equipment, a realm where instrument-on-a-card systems cannot compete, due to the inability of VXI to provide tight electromagnetic shielding required by rf and microwave equipment, says Joseph dePond, HP modular program manager. In rf and microwave, next year will see more and more frequency-hopping radio and radar



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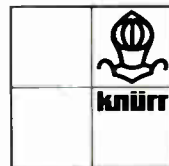
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# FASTER PROCESSORS WILL DRIVE HIGH-END CONTROL

systems, which will create a demand for new kinds of instruments to test these systems. Typical of the type of instrument becoming available to serve the frequency-hopping segment is the Tektronix 3052 spectrum analyzer.

During frequency hopping, a transmitter broadcasts at one carrier frequency for a period of time, perhaps around 10 ms. It then abruptly shuts off, switches to another frequency, and resumes broadcasting. In military applications, excess spurious transmission between hops could possibly allow enemy receiving equipment to pinpoint the position of a transmitter.

Testing these radios requires a spectrum analyzer with a wide real-time bandwidth over a broad spectrum of frequencies, says Douglas Goodman, marketing manager for the strategic project unit at Tektronix. In addition, a wide dynamic range is needed to display the transmitted carrier frequency as well as any spurious frequency emanating from the transmitter when it has been shut off in preparation for a hop.

The Tektronix 3052 digital spectrum analyzer, designed specifically for this application, has a dynamic range of 100 dB, 10 to 20 dB better than other analyzers currently available. In addition, the instrument has a real-time bandwidth of 2 MHz over a 10-MHz spectrum. By contrast, a conventional analog spectrum analyzer has a real-time bandwidth of 80 kHz over this frequency spectrum.

**MORE AUTOMATION.** One more issue that affects the accuracy of high-performance instruments is calibration, another area where new technology developments will be seen in 1989. Calibration techniques have become a lot more automated than they were, say, in 1975, but instruments still are taken periodically to a calibration lab to be checked out and adjusted by a skilled calibration engineer. Changing this tradition is Fluke's 5700A multifunction calibrator, announced in September and going into use this year and next. The instrument is the first calibrator that can be used in the field by any engineer—he need not necessarily be a calibration specialist. The calibrator continually checks its set of internal standards to determine how much error has crept into its own measurements.

The next step is to add statistical process-control software to the instrument, says John Flowers, product manager at Fluke. This software will develop an accurate profile of the calibrator by tracing historical data on the amount of error that develops in each calibrator over time. From this, the error level that will occur in each calibrator in the field can be accurately predicted. A coming capability, called predictive compensation, will be the next major advance in calibration, says Flowers.

—Jonah McLeod

**M**icrochip intelligence will continue its determined march into all levels of the factory in the year ahead. Reduced-instruction-set computer technology will make its industrial presence felt with the emergence of 16- and 32-bit RISC or RISC-like processors working at high-performance embedded real-time factory jobs. Conventional 8- and 16-bit controllers, as well as personal computers, will continue to spread into every nook and cranny of the world's factories.

Computing power will also become more widely distributed, with everything from sensors to motor starters increasingly carrying low levels of solid-state intelligence. New software will also emerge to help shop foremen make better use of their resources in new and more efficient ways.

Another major trend in industrial-automation systems is being led by auto makers, whose factories will use the Electronic Data Interchange and bar coding systems to forge stronger links with their suppliers next year. That will enable them to get the most out of systems heavily dependent on the timely flow of manufacturing materials and components. The move to automate business practices such as ordering and shipping components and subassemblies while coordinating the flow with inventory fluctuations will let manufacturers adopt more of the "just-in-time" practices that have been so successful in Japan.

Applications that demand peak performance from control hardware will see the first use of RISC and RISC-like architectures in factory automation. Though most RISC chips currently on the market are well suited as high-speed engines for 32-bit engineering work stations and superminicomputers, processors are beginning to appear with RISC-inspired architectures that are instead engineered for embedded real-time control.

For example, Intel Corp. introduced its 32-bit 80960 processor line last April, and the Harris Semiconductor Products Division brought out its Forth-based 16-bit RTX 2000 chip last May. Both processors rely on unique RISC-like designs aiming to hold down cost and component count for

embedded real-time jobs. Both are expected to show up in initial factory products next year, as may chips with RISC-inspired architecture made by other vendors.

High-speed RISC processing will be a natural for robotics, in which robot-arm speed is frequently limited by the speed at which the control loop can be calculated, says Lewis R. Pacey, 80960 product

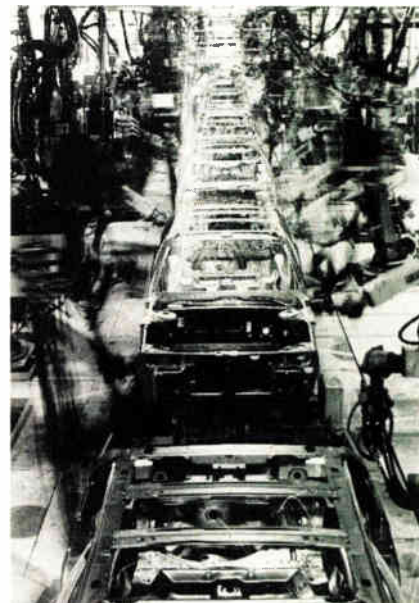
manager for Intel's Chandler Microcomputer/ASIC division, in Hillsboro, Ore. In a typical robotics application, the RISC processor will serve at the top of a hierarchical structure of one or more high-speed controllers supervising the operation of several con-

ventional 8- and 16-bit processors that handle the actual arm movement.

RISC processors are also expected to find uses in process-control equipment for high-speed scanning and operating on large numbers of input/output points on a network, Pacey says. RISC processors will also find use in vision systems, multi-axis machine control, and machines cutting with lasers, predicts David G. Williams, RTX 2000 market development manager in the Harris Semiconductor unit in Melbourne, Fla.

## COMING SOON

- RISC-based technology that will help control factory operations
- New electronic systems linking manufacturers to suppliers



**U. S. car makers plan more use of the Electronic Data Interchange in manufacturing.**

Transforming the factory as well as the newly-found uses for low-end computers. Personal computers will see more shop-floor use next year, thanks to the increasing availability of add-in boards priced at \$400 to \$1,000 that can configure PCs specifically for factory operations control, predicts David Penning, director of manufacturing automation services at Dataquest Inc., a market research company in San Jose, Calif.

As more and lower-priced intelligence becomes available at all levels, an increasing amount of computing power will be used to improve programming environments and operator interfaces, industry executives are predicting. New factory software will provide more powerful analytical tools such as expert systems for the shop floor, which will allow factory managers to use data more efficiently. Furthermore, as manufacturers strive to fine-tune their production processes next year, they plan to require their suppliers

to provide necessary computer support technologies—such as EDI and bar coding—needed to make factories run smoothly. The U. S. automotive industry is leading the drive and using the technology to improve efficiency under just-in-

### Factory-configured PCs will eat their way into traditional controller business

time manufacturing schemes.

“By our own admission, we are not doing just-in-time manufacturing to the extent that our Japanese competition is,” says Jean N. Mayer, managing director for the Automotive Industry Action Group, a trade organization with 700 members that includes the Big Three U. S. auto makers and their suppliers.

Mayer sees technology like EDI links

between suppliers and their customers as “just-in-time enablers” that will help U. S. car makers close the gap between themselves and the Japanese.”

Beginning in January, Ford Motor Co. will be the first of the Big Three to require that its major component suppliers be equipped to do business electronically using EDI standards developed by the AIAG. The requirement will affect some 3,300 suppliers who do business with nine separate Ford manufacturing divisions in the U. S., Canada, and Mexico.

Suppliers will be required to send an advance shipping notice electronically when a loaded truck leaves their dock; receipt acknowledgment will be sent electronically after the truck reaches Ford. Suppliers will also put a bar-code label on every container sent to Ford, which is scanned to create the electronic shipping notice. And Ford may not be alone. Chrysler Corp. is expected to announce a similar EDI requirement for its suppliers soon.

—Wesley R. Iversen

## CONSUMER

# ADVANCES IN PERSONAL VIDEO COULD FIRE UP A NEW MARKET

**A** brewing battle in ultraminiature video equipment will heat up the competition in consumer electronics markets in the coming year, say industry watchers. Throwing fuel on the fire too will be higher-resolution TV technology and an improved 8-mm video recording format. The first products related to a home automation communications standard are on the way as well, and they could bring the industry more growth as it heads into the next decade.

On the video front, new ultraminiaturized 8-mm video-head drum technology will drive hand-held video gear from Sony Corp. and other companies. The new miniaturization could help the underdog 8-mm format gain ground against larger 1/2-in. VHS formats. And more manufacturers are poised to jump into the market with products that combine tiny liquid-crystal display TV receivers with miniaturized video-cassette recorders in the same hand-held unit.

“One of the big things we’re going to see in 1989 is the emergence of the personal video market, with the marriage of VCR and LCD TV,” says Robert Gerson, editorial director for *Twice*, an industry trade publication in New York. “At the moment, these units cost \$1,000 and up. But one advantage is that the price you’ve got to pay for quality LCD tech-

### COMING SOON

- Miniaturized componentry that could bring about a new portable personal video market
- The first products based on Home Products Link, a new North American home automation standard

nology doesn’t seem so bad when you combine it with the VCR. Five hundred dollars for a 3-in. TV set somehow seems like a lot more money than does \$1,000 for a TV/VCR combination.”

Two emerging technologies—high-definition TV and digital audio tape—are not yet available in the U. S.: HDTV because more research and standards development needs to be done; DAT because of politics.

But better TV resolution will be available to U. S. consumers next year. Improved-definition TV home receivers that have been developed in Japan are expected in 1989 from about a half-dozen vendors, including Panasonic, Philips, Sanyo, Sony, and Toshiba.

As an interim step toward HDTV, the IDTV sets will maintain compatibility with existing broadcast standards, but use digital techniques to produce resolution 30% to 40% better than conventional sets, IDTV sets, each of which carries about a megabyte of memory, have been delayed in their appearance by this year’s memory-chip shortages.

On the audio front, the U. S. market entry of digital audio tape is still hung up in controversy, and DAT is already being marketed in Japan and Europe. And some DAT play-only units are being sold to the U. S. automotive market. But whether DAT play/record units will hit U. S. store shelves in 1989 is still uncertain. The question may hinge on a solution to record-industry concerns that the format could lead to widespread unauthorized copying of prerecorded material. The dispute with the recording industry has already delayed DAT’s U. S. entry by more than two years.

**NETWORK STANDARDS.** The delay in introducing DAT technology into the U. S. is leaving plenty of room for other developments at upcoming industry shows. One attention-getter is likely to be the debut of products related to the Home Products Link, which was known earlier as CEBbus. HPL spells out a common home networking standard for two-way com-

munication over a variety of media types, including power lines, twisted-pair wiring, coaxial and fiber cable, and transmission using rf and infrared devices.

Developed under Electronic Industries Association sponsorship with participation by some 50 major home product manufacturers, the HPL specification aims to create a "communications highway." That communications highway would link a diverse range of equipment from differing manufacturers for a variety of home-automation functions. Consumer electronics gear, appliances, security systems, and heating and ventilation equipment can all fit into HPL-equipped homes. As manufacturers begin to build HPL compatibility into their products, the standard's multiple-media flexibility will allow consumers to automate their homes in small steps without making any previously purchased appliances obsolete, HPL backers say.

Initial HPL-compatible products from various manufacturers are expected to show up by mid-1989, says Thomas D. Mock, director of engineering for the EIA's Consumer Electronics Group in Washington. And while some industry watchers are taking a wait-and-see attitude, HPL's most enthusiastic backers see the standard as the catalyst for what could finally become a mass market for U. S. home-automation products by the early 1990s.

HPL is due out in draft form by this year's end. And the EIA plans an HPL demonstration next January in a special booth at the Las Vegas Winter Consumer Electronics Show. The booth demonstration is expected to use equipment from about 15 manufacturers, including Marantz, Mitsubishi, Panasonic, Sony, Tandy, and Thomson.

"In the booth, we'll be trying to show some capabilities that are not available today in any combination of devices you can buy," says Donald Pezzolo, president of Diablo Research Corp. The Sunnyvale, Calif., firm is handling system integration for the demonstration.

**THE WIRED HOME.** As one example, Pezzolo says, someone who is getting ready to turn in for the night might control various appliances in the home using an IR remote control on a TV in the bedroom. "You can tell a VCR somewhere else in the house to send its signal to the TV set that you're watching," Pezzolo says. "And if you forget whether you turned down the thermostat, you can ask it to send its status to your TV screen, and make changes accordingly. If the doorbell rings, you can [switch the TV input] to a security camera out front and see who's standing on your doorstep."

What probably is the surest bet for turning on the industry next year, until

advances in home automation networking are proven, lies with expected video introductions. And when it comes to more miniaturization, Sony will lead the charge with new 8-mm products. The company announced development of the world's smallest video-head drum in July. At only 2.67 cm in diameter, the new drum is a third smaller than those used in current 8-mm equipment. The miniaturized drum head is the key component in Sony's new FL Mecha 8-mm tape-drive mechanism, which is only about half the weight and

porating the tiny drive mechanism are expected next year.

Sony plans not only to incorporate the FL Mecha in its own 8-mm video products, but will also sell the mechanism for use by other consumer manufacturers. That could help fuel a trend next year toward a new category of miniaturized hand-held TV/VCR combination units.

An early example of the breed is Sony's GV-8 Video Walkman, which combines 3-in. LCD receiver for watching standard broadcast programs and a 8-mm VCR in a package measuring 5 by 8 by 2.5 in. It was introduced in June. As small as the Video Walkman is, it doesn't incorporate the new FL Mecha unit. Casio and Panasonic also already offer similar, slightly larger hand-held TV/VCR products based on VHS and VHS-C formats. Industry watchers expect other handhelds to be rolled out by a bevy of other vendors next year.

In addition to improved miniaturization, the 8-mm format may also make progress on another front next year. A group of 10 consumer vendors—Aiwa, Canon, Fuji Film, Hitachi, Hitachi Maxell, Konica, Matsushita, Sanyo, Sony and TDK—announced agreement last March on a specification for a new enhanced 8-mm video format called 8-mm Hi-Band. First products based on the new 8-mm format could appear as early as the latter part of 1989, the companies say.



Hand-held personal video products like Sony's Video Walkman, combining an LCD TV with a VCR, will be hot in 1989.

thickness and a third the size of its predecessor.

The Sony development one-ups the VHS camp and apparently reestablishes an inherent size advantage for 8 mm in the video-format wars. Sony "has cut the size of its head drum and reduced the size of the entire mechanism, which is something that the VHS people can't do because they've already done it with VHS-C," says David Lachenbruch, editorial director at Television Digest, an industry trade publication in New York. VHS-C (for VHS-Compact), introduced in 1984, achieved similar gains in VHS format miniaturization by reducing drum diameter to about 4 cm, matching that of 8-mm products available at the time.

The first product to incorporate the new miniaturized 8-mm mechanism is Sony's CCD-V88, a camera/recorder introduced in September in Japan. The unit is about the size of a 35-mm single-lens-reflex still camera, and is the industry's first camcorder to weigh in at less than a kilogram, Sony says. A U. S. version of the machine, the CCD-V11, will be rolled out this month, and other products incor-

porate Hi-Band performance parameters have not yet been nailed down, says R. Jay Sato, national sales manager for 8 mm products at Sony Corp. of America, in Park Ridge, N. J. But the objective is an enhanced picture with more than 400 lines of resolution, Sato adds. That would put 8-mm Hi-Band in the same neighborhood as the high-resolution Super-VHS format, which was rolled out by the VHS camp last year. S-VHS is capable of resolution of about 420 to 430 lines.

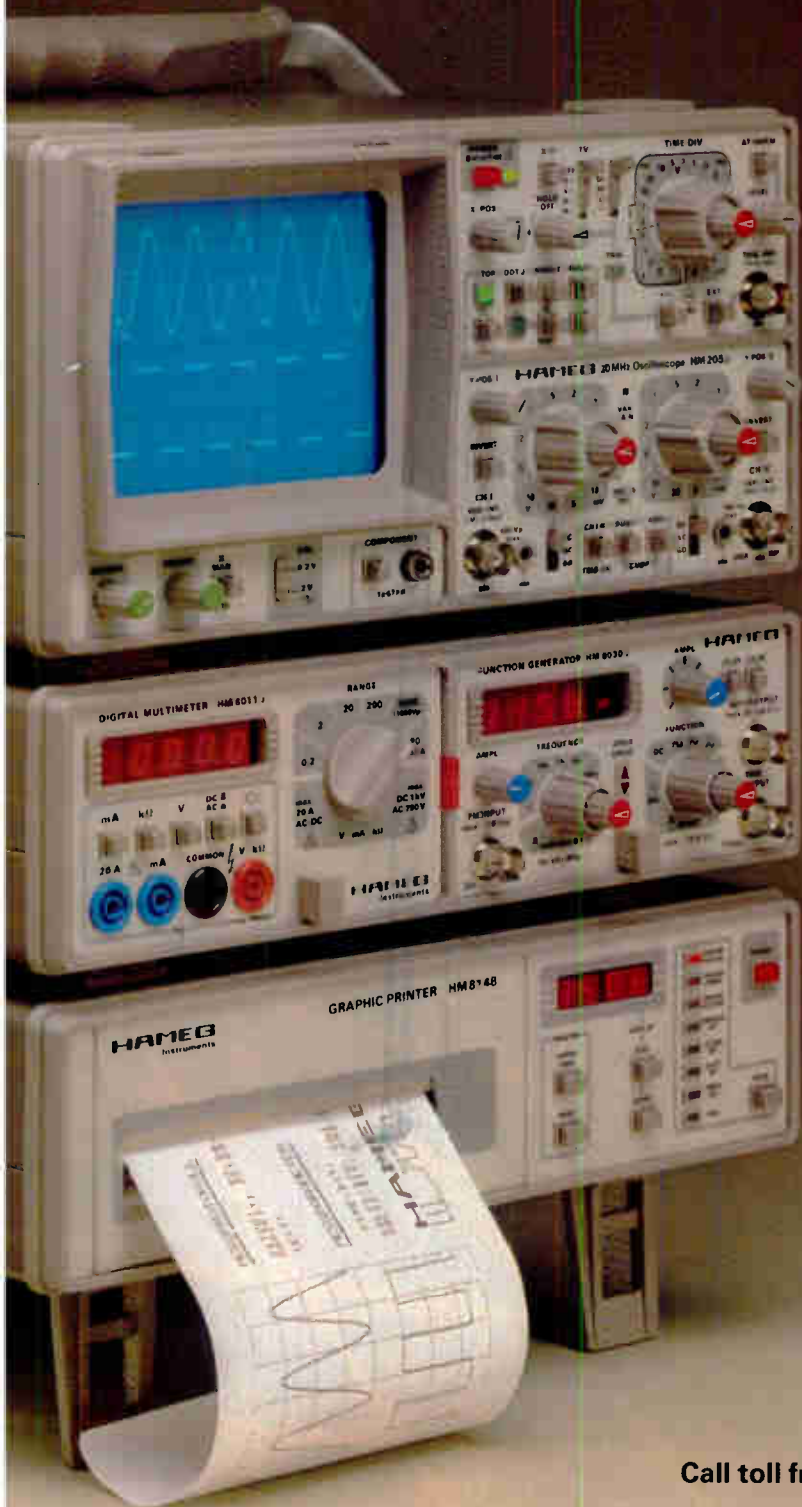
**VIDEO CATCH-UP?** For their part, people backing VHS say that with Hi-Band, the 8-mm camp is playing a game of catch-up in areas such as high resolution. "We've already got S-VHS," says one executive with JVC Company of America, in Elmwood Park, N. J.

But Sony's FL Mecha technology gives it the miniaturization edge, concedes the JVC executive, who asked not to be named. "VHS-C has a drum size of 4.2 cm and that's about as far as we can go," he says. But he adds that smaller is not always better. "We've got [VHS] camcorders with weights of almost 1 kg already," he says. Camcorders such as the new Sony unit which go below that target weight may be too difficult to hold steady, he contends. —Wesley R. Iversen

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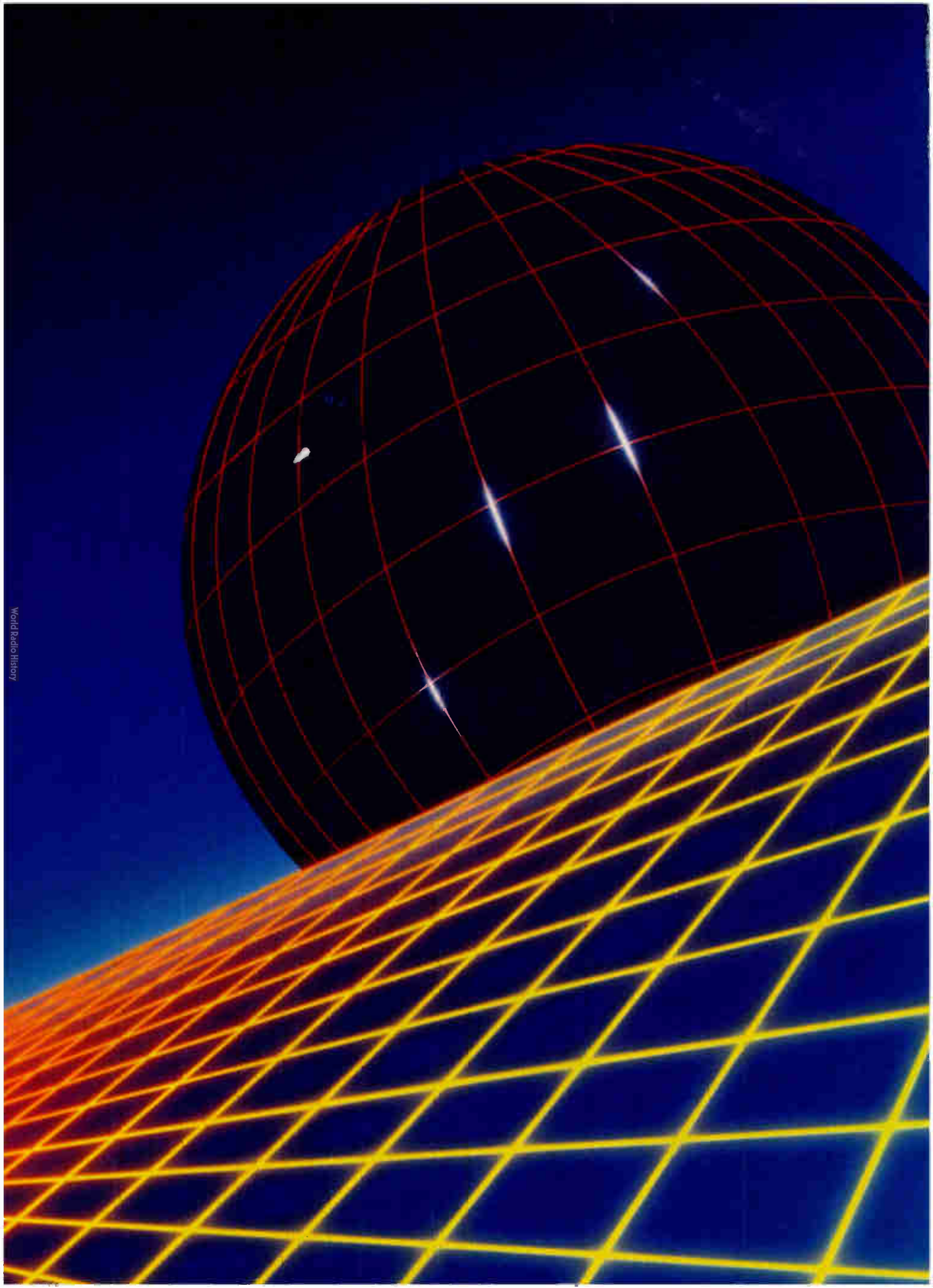
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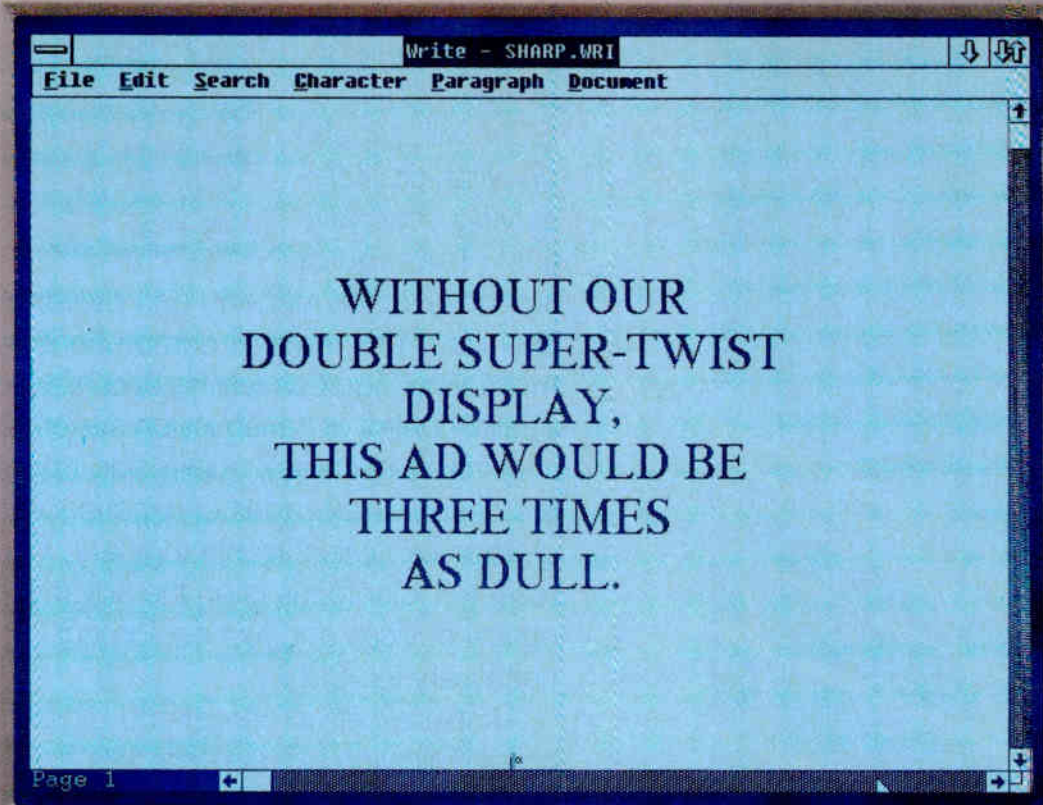
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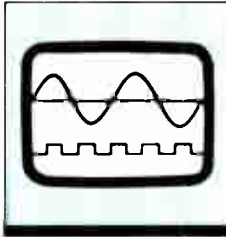
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# AT LAST, THE MARRIAGE OF DSP WITH MICROCONTROLLER FEATURES

A single chip combines DSP speed and muscle of microcontroller peripherals

There's an important new wrinkle in the chip market: the merger of high-performance microcontrollers and digital signal processors. The product of that marriage is being called a digital signal controller, arriving in the form of the DSC320C14 developed by Microchip Technology Inc. of Chandler, Ariz., with help from its DSP second-sourcing partner, Texas Instruments Inc. of Dallas.



and 4,096 by 16 bits of read-only memory, plus six pulse-width-modulation outputs with 50-ns resolution and four inputs for pulse detection with 160-ns resolution. Also bundled on the CMOS chip are 16 configurable I/O lines, a serial port, 16 interrupts, four 16-bit timers, and hardware support for communications protocols.

Compared with conventional microcontrollers, DSPs are somewhat like a racehorse; bred for high-speed performance. The workhorse microcontrollers, by contrast, are not usually built for speed—but they have the muscle through integrated features to tackle many jobs.

But now, high-performance control applications need both characteristics in one device: the speeds of DSP for complex mathematical calculations alongside the flexibility of microcontroller features. The latter include sophisticated I/O structures, watchdog timers, pulse-width mod-

ulated outputs, and flexible interrupt structure. Error-observant watchdog timers, for example, insure reliability when control systems must run for long periods of time. A flexible interrupt structure can be used to change software-execution sequences in response to real-time events. A flexible I/O structure is often required to deal with off-chip devices in control applications.

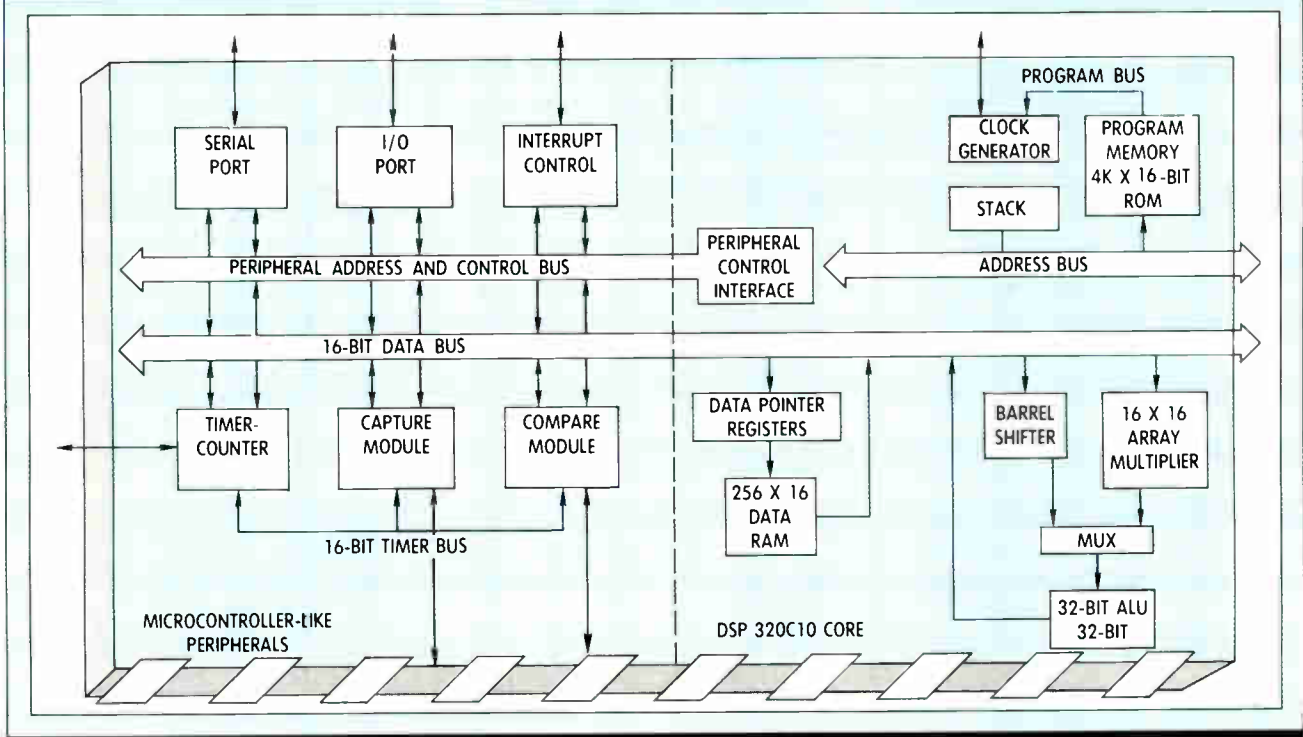
The 320C14 has those kinds of features and more, says Rahul Sud, marketing vice president at Microchip, which until April was the Microelectronics Division of General Instrument Corp. (see p. 133). First, he says, the digital-signal controller is four to five times faster than existing 16-bit microcontrollers. And it operates under the industry's most popular DSP instruction set—it's software-compatible with TI's prolific 32010 processor.

Moreover, its peripheral features compensate for the traditional shortcomings of DSPs in control. Along with a DSP core that has 160-ns cycle times and can exe-

Targeted at real-time, closed-loop control, the 25.6-MHz integrated circuit is a 16-bit controller with tightly coupled peripheral and input/output functions normally associated with monolithic microcontrollers. It also has the number-crunching processor core of TI's 320 DSP architecture.

The DSP portion of the 320C14 executes 6 million instructions/s. The microcontroller features provide 256 by 16 bits of on-board static random-access memory

## COMBINING DSP WITH MICROCONTROLLER FEATURES



The new 40- and 44-pin 320C14 digital-signal controllers being ready by Microchip Technology and Texas Instruments will have a Harvard architecture with multiple internal buses, mixing a fast DSP core with the peripheral features of microcontrollers.

cute multiply-accumulate operations in one cycle, the 320C14 has an active I/O subsystem capable of operating in parallel with the central processing unit. Sud says the result is enough speed and features to address a wide range of real-time, closed-loop applications such as servo-motor control for high-density disk drives and a variety of automotive-systems applications such as engine and active-suspension control. Until now it hasn't been feasible to serve many of these speed- and I/O-intensive processing applications with standard DSP or with microcontroller ICs, Sud adds.

**MORE MEMORY.** Samples of the 90,000-square-mil 320C14, which is fabricated with 1.5- $\mu$ m CMOS, are available from both Microchip and TI in either a 40-pin plastic dual in-line package or 44-pin plastic leaded chip carrier. Production quantities should be available in the first quarter of 1989. In 100-piece quantities, the device costs \$75 apiece, but the price drops to \$10 or under for high-volume purchases, Microchip managers say. Later this year, the firm will offer an expanded-memory version, packaged in 68-lead PLCCs; and TI will sell a version—the 320CE14—with erasable programmable ROM on board.

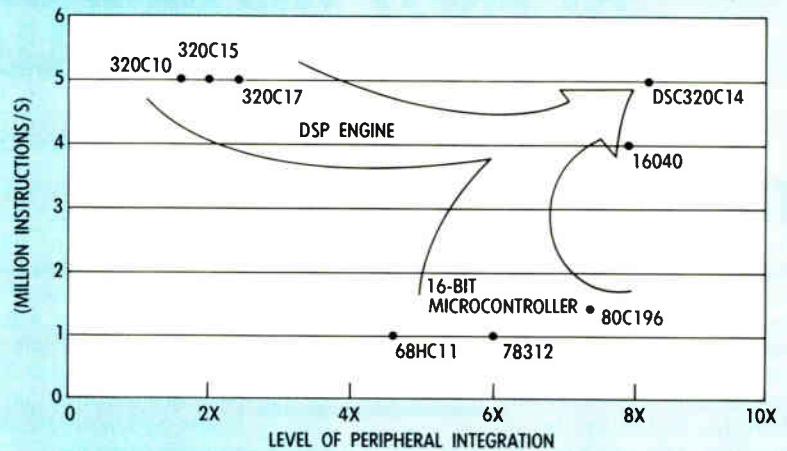
The controller is a precursor of what Sud promises will be a long line of processors that combine even more features of traditional controllers and DSPs. As a new company, Microchip plans to pioneer this field, he says. Already in development are a number of DSP parts with a range of I/O features and integrated peripheral options, such as ultraviolet EPROM, electrically erasable PROM, and high-speed versions tapping the increased power of faster 320-family designs.

It all starts with the 320C14, which has interface logic to address up to 4K words of external RAM. The chip has a Harvard architecture with multiple internal buses that further increase execution speeds. For high precision and fast results, the 320C14 has a 32-bit arithmetic logic unit, 32-bit registers, and two hardware shifters that allow scaling simultaneously with other operations. Also in the DSP core is a hardware 16-by-16-bit multiplier—a function that is often implemented in software on standard microcontrollers.

Incorporating a wide range of DSP and general-purpose instructions, the digital-signal controller is object-code-compatible with the 320C10, which means customers in both DSP and microcontroller camps can tap existing software, says Sud. Both Microchip and TI will offer assemblers, linkers, and simulators, as well as full in-circuit emulators and personal-computer-based development systems.

Surrounding the DSP core are a bevy of on-chip peripheral functions such as timers, a capture subsystem for direct optical encoding, and a compare subsystem

## THE MARRIAGE OF TWO PROCESSOR WORLDS



The 320C14 digital-signal controller stands ahead of conventional DSP chips in the number of integrated on-chip features and above 16-bit microcontrollers in speed.

for pulse-width-modulated interfaces. Its serial port can operate in four different modes: 6.4-MHz synchronous; 400-MHz asynchronous; as a coder/decoder interface for analog subsystems; and as a hardware interface for serial networking and other communications protocols.

As important as the number of func-

### The chip is software-compatible with TI's 320C10 processor

tions on-chip is the design that allows peripherals to operate as an active I/O subsystem, notes Ajay Padgaonkar, DSP design manager at Microchip. The active I/O subsystems will perform bit manipulation and event monitoring in parallel with the CPU, enabling the chip to sample and process data at real-time speeds while it performs its control job. In essence, he says, the DSP core accesses each of these subsystems as I/O-mapped peripherals via special in and out instructions, which transfer both commands and data between the blocks. The peripherals interact with the CPU using 16 interrupts, which are distributed among the timers, capture-and-compare pins, serial port, and I/O port. All but one of these interrupts is maskable, and each is mapped into a single CPU interrupt.

To provide time references for its I/O subsystems, the 320C14 incorporates four timers. One is for generating CPU interrupts and implementing a baud-rate generator for the serial ports; a second is used as a watchdog timer. The other two timers drive the capture subsystem, which pro-

vides edge detection, and the compare subsystem to generate output pulses. In the 320C14, a watchdog timer has been designed to prevent errors due to accidental resetting. In many real-time control applications, it is important that the software can recover from errors such as infinite loops or loss of synchronization, says Padgaonkar. In traditional implementations, a timer will reset periodically. Occasionally, though, it may reset accidentally when a program goes astray. To stop this from happening with the digital signal controller, Microchip designers made the reset procedure complex, which reduces the odds of the device resetting itself by accident. And unlike traditional microcontrollers, the watchdog time-out delay is programmable, making it suitable for a much wider range of applications that are dependent upon interrupt delays.

The company expects auto applications to be a prime market for the digital signal controller, says Matt Hussey, Microchip's DSP product marketing manager, who envisions the chip being used in active-suspension systems and real-time engine control. In an active-suspension system, he says, a single 320C14 could perform real-time adaptive control to compensate for varying road conditions, driver habits, and changes in the way cars ride when rounding corners, making quick stops, and accelerating suddenly, for example.

These functions all require feedback and control, he says, making them ideally suited for the marriage of DSP and control functions. In the past, such active-suspension control subsystems usually needed three processors: a standard microcontroller, a DSP chip, and a third microprocessor to handle supervisory tasks.

—Bernard C. Cole

# PC I/O BREAKTHROUGHS

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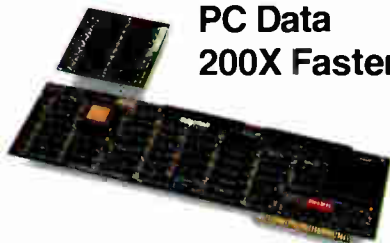
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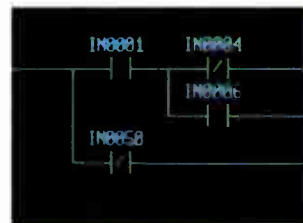
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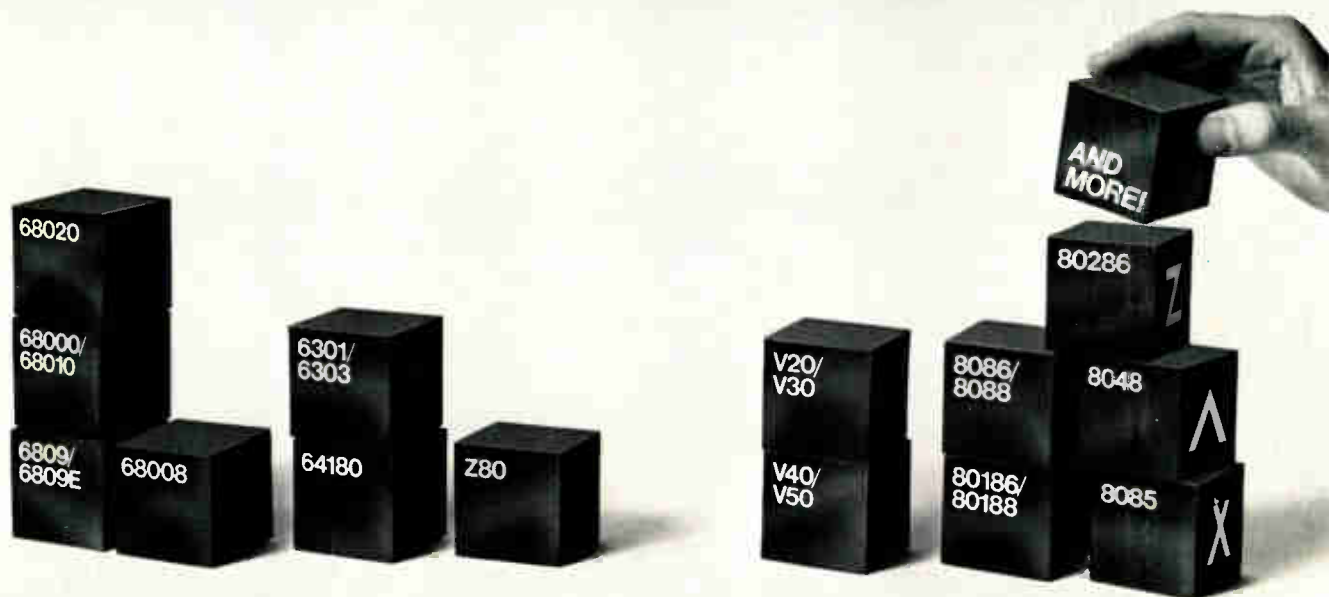
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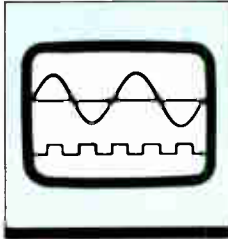


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# FLEDGLING MICROCHIP GETS FIGHTING CHANCE

**A**troubled history is not keeping Microchip Technology Inc. from braving the waters of independence. The operation suffered a string of losses as the chip-making division of General Instrument Corp. Now—even with a turnaround well under way, help from the former parent, and a strong product line—efforts to shore up Microchip's position in the booming chip markets are being frustrated by a delayed initial public offering.



Still, despite its horrendous losses as GI's Microelectronics Division, the Chandler, Ariz., operation has been profitable for five straight quarters, including the first quarter of fiscal '89. And with its launch as an independent firm last April, Microchip is free of debt. Furthermore, GI is pitching in \$10 million for operating costs during the transition, and for the next five years, it will foot the legal bill in numerous patent suits pending against Microchip—such as its share of an industry-wide dispute over the right to technology for electrically erasable programmable read-only memories. New York-based GI is providing this support because it holds a 44% stake in the new firm as part of the spinoff agreement it made with Microchip's management.

Principal architect of the turnaround and the prime mover for independence is Microchip's chairman, president and chief executive officer, Donald R. Sorchyeh. He was recruited by GI in 1986 to revive the operation. Today, the 57-year-old semiconductor veteran is confident Microchip will make it.

Part of that optimism is based on Microchip's product line in two burgeoning chip markets: EEPROMs and digital signal processors. The firm's EEPROMs reach up to 256-Kbit densities and top speeds of 35 ns. With greater manufacturing capacity, Microchip estimates that it could boost its EEPROM revenues by about \$3 million every month in the current boom market.

In DSPs, the company continues to build momentum with this month's debut of the 320C14, a DSP with the integrated features of a microcontroller (see p. 127). DSP-market analyst William R. Strauss of Forward Concepts in Tempe, Ariz., says Microchip has assembled one of the top DSP teams around, and he believes it is seeing manufacturing yields on those products at higher rates than its larger second-source partner, Texas Instruments Inc., Dallas. Other industry observers think Microchip's turnaround may be more a result of better market conditions than shifts in strategies.

Still, Microchip has a fresh start. GI shouldered the fallout from heavy writeoffs and the resulting red ink until the legal separation in April. Details of the spinoff's state are spelled out in a stock prospectus published this summer in preparation for Microchip's initial public offering of 2.5 million common shares. Aiming to raise \$20 to \$25 million, the offering price was set at \$8 to \$10 a share—nearly book value. But weak market conditions for technology issues resulting from last fall's market crash forced a delay.

The postponement in raising capital has been a major concern to management, because about \$16 million of the proceeds have been earmarked as part of a \$20 million campaign that is aimed at expanding Microchip's wafer fab resources. Those plans include a new 1- $\mu$ m CMOS process slated to begin production early next year.

Today, Microchip has a workforce of 1,450 employees, with more than 800 at assembly and test facilities in Taiwan. "It didn't happen overnight and hasn't been easy," concedes Sorchyeh, who was brought in by GI after an ambitious plan to restructure the business foundered with delays in getting new CMOS and

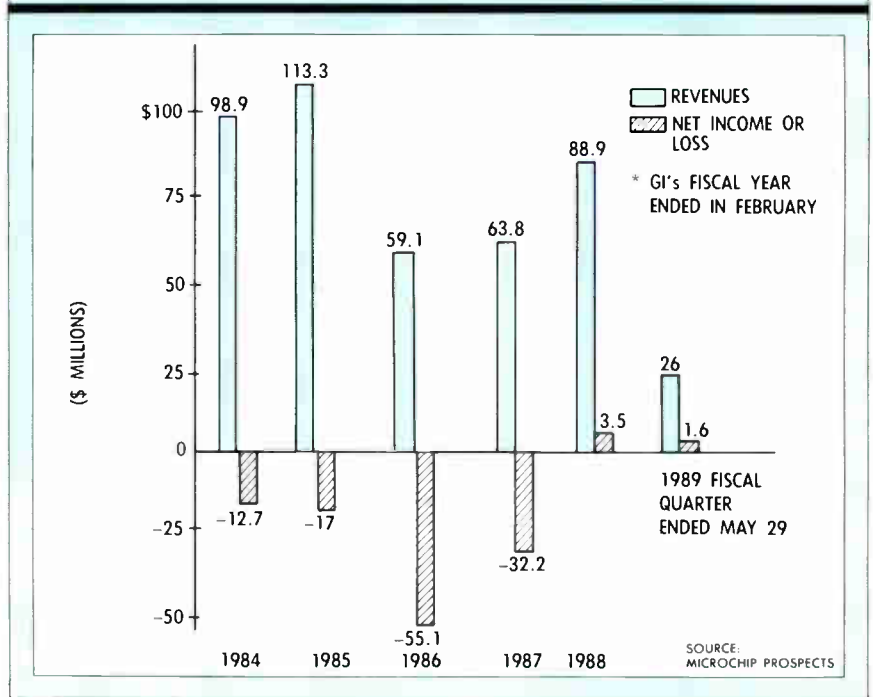
nMOS silicon-gate technology running in the plant. Sorchyeh had already earned a reputation as a deft manager of chip operations when he spearheaded a growth phase at the Semiconductor Group of Harris Corp. in Melbourne, Fla.

"I wanted to do the same thing there [spin out the chip business from Harris], but they wouldn't go along," he recalls. Sorchyeh left his Harris post as vice president-group executive in 1979 to run a medical electronics startup, Medcomp Inc. in West Melbourne, Fla.

**TOUGH TASKS.** When Sorchyeh arrived at GI, the prospects for success were bleak despite a still-stable core of technology. Ironically, the root of the division's chip woes was its success in supplying masked ROMs to the video game markets of the late 1970s and early 1980s. Masked ROMs revenue peaked at \$185 million during the 1983 fiscal year. But by the mid-1980s, GI was overdependent on supplying ROMs to a slumping market.

So in mid-1987, GI wanted out of the chip business, and Sorchyeh jumped at the opportunity. He convinced GI that it was in its best interest to launch the strongest possible spinoff. Sorchyeh won't claim that all Microchip's problems are solved, but he believes the worst is behind the company: "We turned the corner last year." —Larry Waller

## A REBOUND IN THE MAKING



GI's chip division, which became Microchip Technology last April, suffered heavy losses but started turning around in the 1988 fiscal year.

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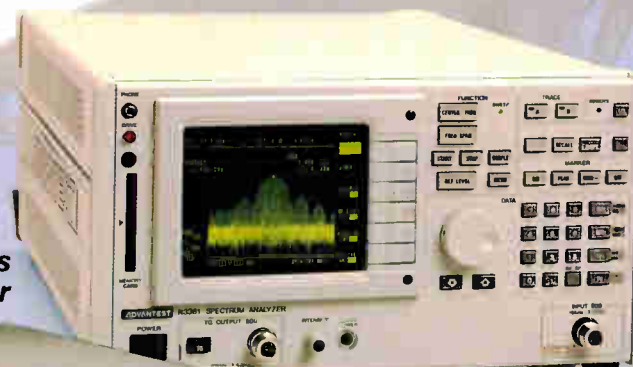
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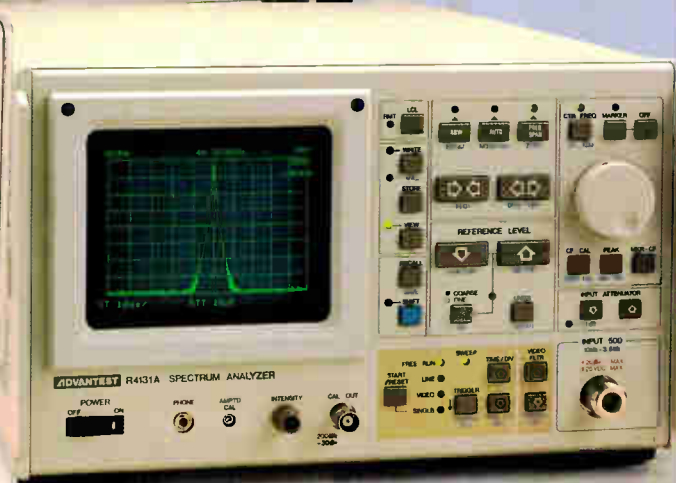
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# DSP GETS A REAL-TIME OPERATING SYSTEM

Startup Spectron creates a virtual DSP machine that frees programmers from assembly-language constraints

Developers of complex digital-signal-processing applications have been crying for tools that go beyond the difficult and costly assembly-language programming methods they have had to work with until now. A small Santa Barbara, Calif., startup is coming to the rescue with the first real-time operating system designed for DSPs.

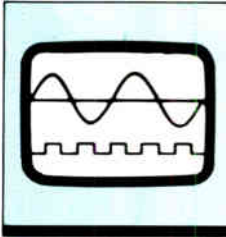
The SPOX DSP operating system from Spectron MicroSystems Inc. works initially with the TMS320C30, Texas Instruments Inc.'s most powerful DSP chip. But SPOX has been designed to be device-independent, and so will be able to work with other DSP chips. The first SPOX package will debut later this year, with two other versions due by mid-1989.

The product is unique in the DSP field, a burgeoning technology that has been tethered only by the lack of development software [*Electronics*, March 31, 1988, p. 57]. Some C compilers have appeared recently for DSP chips such as AT&T Co.'s DSP32C, Motorola Inc.'s 56000, and TI's 320 families. They have made DSP programming easier, quicker, and less costly compared with doing the work in assembly language. But a compiler alone isn't enough.

Spectron's SPOX, by contrast, creates a virtual DSP machine, thanks to a set of high-level software primitives that makes it more than just an operating-system kernel. Along with the general-purpose operating-system functions, the virtual machine is bolstered by such DSP-specific primitives as math routines and math functions, memory management, real-time stream I/O, and device drivers.

Such a package could help systems houses, which are increasingly turning from analog circuits to DSP for higher reliability, greater accuracy, smaller size, lower power, and reduced costs. Consequently, the DSP-chip market has mushroomed, growing from under \$1 million in 1981 to over \$100 million in 1987. In 1991, it will hit \$600 million, says Electronic Trend Publications, Saratoga, Calif.

Using DSP for more complex applications means that programs have to handle I/O operations and other tasks in addition to the signal processing. So customers need new tools to ease their programming burden. Spectron's solution centers on four key functional components of the SPOX virtual DSP machine: math, memory man-



agement, stream I/O, and the real-time kernel. The DSP math is a set of application-level software modules for implementing such commonly used DSP routines, like vector, matrix, and filter functions. These are built in so that the applications programmers do not have to reinvent this code for every use.

The integrated memory-management code gives the application explicit control in allocating data storage from different segments of system memory. The stream I/O capability is an easy way for a programmer

**SPOX could be a boon to systems houses, now turning more to DSP**

to input and output blocks of data at a time from a variety of peripheral devices. This is because the stream I/O code is independent of the type of I/O devices. Separate device-driver codes are written for specific devices so that application programs do not have to be changed if I/O devices are. Finally, the real-time operating-system ker-

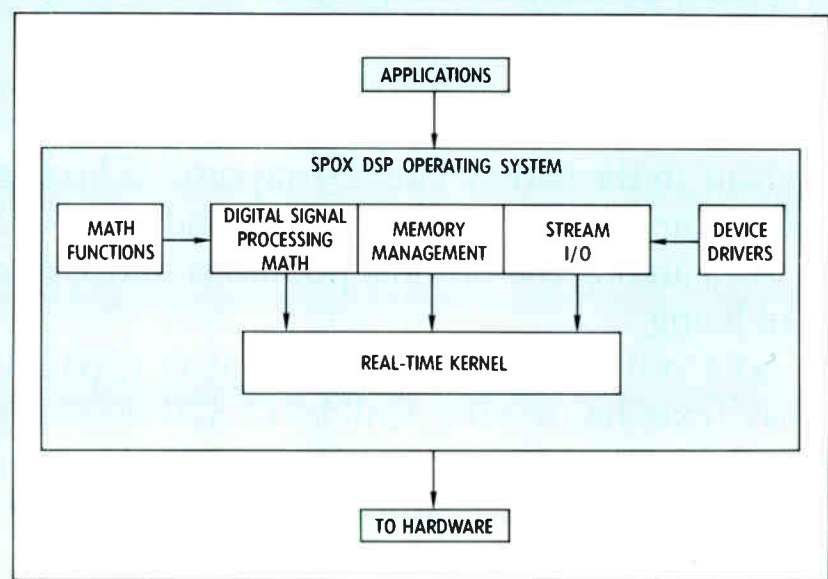
nel provides callable routines and functions for scheduling and synchronizing multiple prioritized tasks in a real-time system environment.

All this means that many benefits will result for DSP programmers, says Robert Frankel, the SPOX system architect. For example, by using a software simulator that is available for the target DSP chip, SPOX lets the programmer execute his application on the host computer used for development. Timing analysis can be performed using the simulator so that real-time code can be debugged on the host. What's more, SPOX's structure and its DSP device-independence provide software portability, allowing application software modules to be reused in new applications.

SPOX's major disadvantage is that it takes code space and execution time to overlay such operating-system and application-level software on the DSP system. Against the costs of somewhat slower-running programs is the gain realized by SPOX, says Frankel—namely, lower dollar costs in developing and maintaining DSP applications thanks to reduced development time.

The first SPOX version, due in December, will be offered as part of the TI XDS 1000 PC-based development system for the 320C30. The whole package will cost \$16,000; separate SPOX-only pricing is not available. A software-only version for Sun work-stations, including the DSP chip simulator, will be available in the first quarter of 1989, and a version for use on Digital Equipment Corp. VAX machines, also equipped with the simulator, will be ready by mid-1989. —Tom Manuel

## DSP SOFTWARE GOES REAL TIME



In SPOX, three functional components—DSP math, memory management, and stream I/O—feed into a real-time kernel, which then interfaces to the hardware.

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Effective throughput, or the rate at which data actually moves between applications, is really the only important measure of network performance. It matters little how fast the maximum speed of the basic link is or even what the average data rate over a link is, if the overall effective throughput for applications is only about 10%.

So the UltraNet breakthrough is a significant one for computer networking. What's more, this new supernetworking environment offers raw data-link performance of up to 1 Gbit/s. But the real achievement lies in UltraNet's powerful system design, which is what allows the company to guarantee an effective throughput of at least 50%.

The timing of the introduction of UltraNet, the San Jose, Calif., startup's first product, is important for the company's future and for the industry: right now, a significant rise in network speed is vital. The newest applications for supercomputers, minisupercomputers, and work stations need vast volumes of data

and they need it fast. Such tasks as three-dimensional visualization and photorealistic imaging in many engineering and scientific disciplines; high-speed data capture, reduction, and analysis; and complex image processing are coming on stream and require high data input/output rates to be effective.

Other networks currently competing for this business include the 1.44 Gbit/s VectorNet from Scientific Computer Systems Inc., a 404-Mbit/s TopLink net from Integrated Photonics, the 100-Mbit/s Hyperchannel DX from Network Systems Corp., and Proteon's 80-Mbit/s ProNet.

**FOUR CLASSES.** The UltraNet family of products will serve supercomputers, minisupers, superminicomputers, and work stations. The first hosts to be supported are the Cray 2 and XMP; the Alliant and Convex minisupers and the MIPS Computer Systems superminicomputer; and the Sun 3 and 4, Silicon Graphics 4D/60, and Stellar work stations. UltraNet supports industry-standard protocols, such as the ISO TP4 transport-level protocol and the TCP/IP protocol.

A typical UltraNet 1000 configuration that would connect a supercomputer, two minisupers, and eight work stations costs about \$283,000. The smaller UltraNet 250, which supports multiple minisupercomputers and work stations, costs about \$145,000 in a configuration for one minisuper and eight work stations. And an UltraNet Cluster for work stations sells for

\$49,000 for four stations and \$79,000 for eight. All hubs are available now.

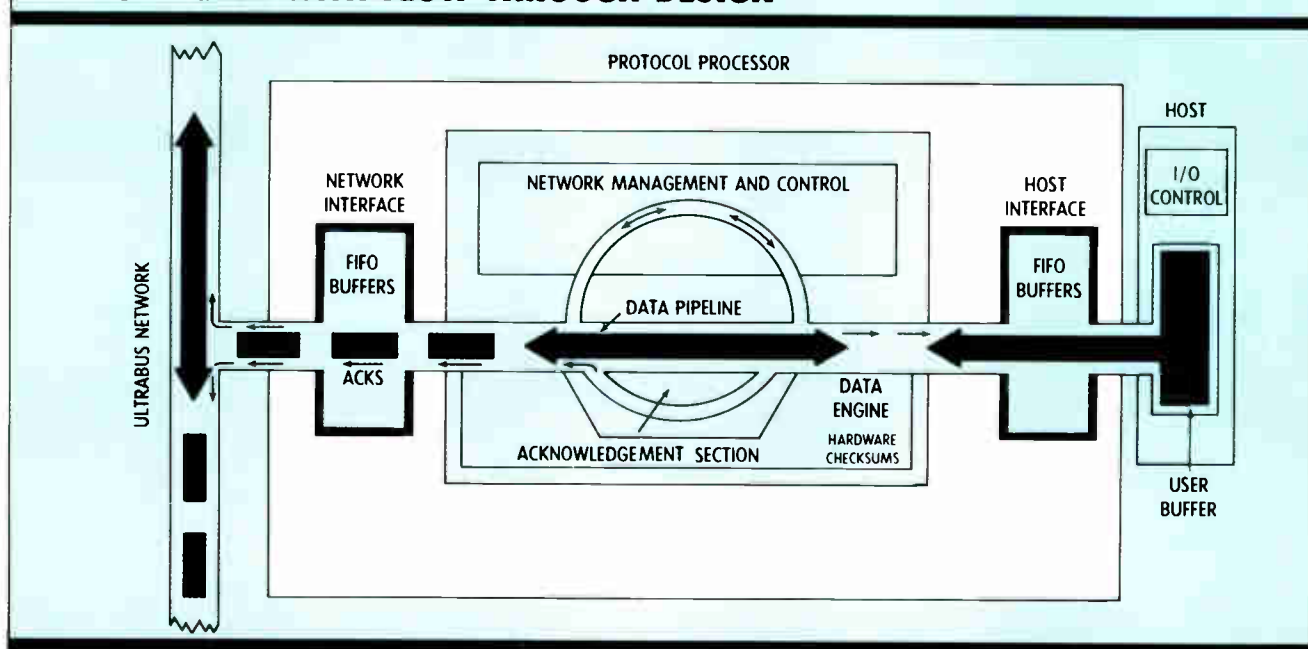
To reach their new throughput record, the creators of UltraNet looked at the entire system, rather than just concentrating on one aspect, like link speed. As a result, they designed performance into all the critical parts of the network.

They started with very fast data links—1.44 Gbit/s. To take advantage of as much of that basic speed as possible, they developed what is probably the first flow-through architecture for an inter-computer net. Instead of moving data in packets that have to be processed at every node, UltraNet allows data to flow through intermediate nodes without any processing.

Another area critical to network throughput is the ability of the device-driver software to work in conjunction with the operating systems running on the computers that form the network's nodes. So Ultra Network took another novel step: it is working closely with host-system vendors to integrate the network device drivers into their Unix operating-system software.

Ultra Network's fast intelligent protocol processor supports the flow-through architecture. Whenever a protocol must be processed—and this has been kept to a minimum in UltraNet—it is done with great speed. All these design features add up to the 50% efficiency that Ultra Network guarantees. —Tom Manuel

## NETWORK LINK WITH FLOW-THROUGH DESIGN



Effective throughput with an UltraNet high-performance computer network is at least 50%, thanks to the flow-through architecture. For example, in the protocol processor, data acknowledgements and network management and control functions do not interrupt the flow of data.

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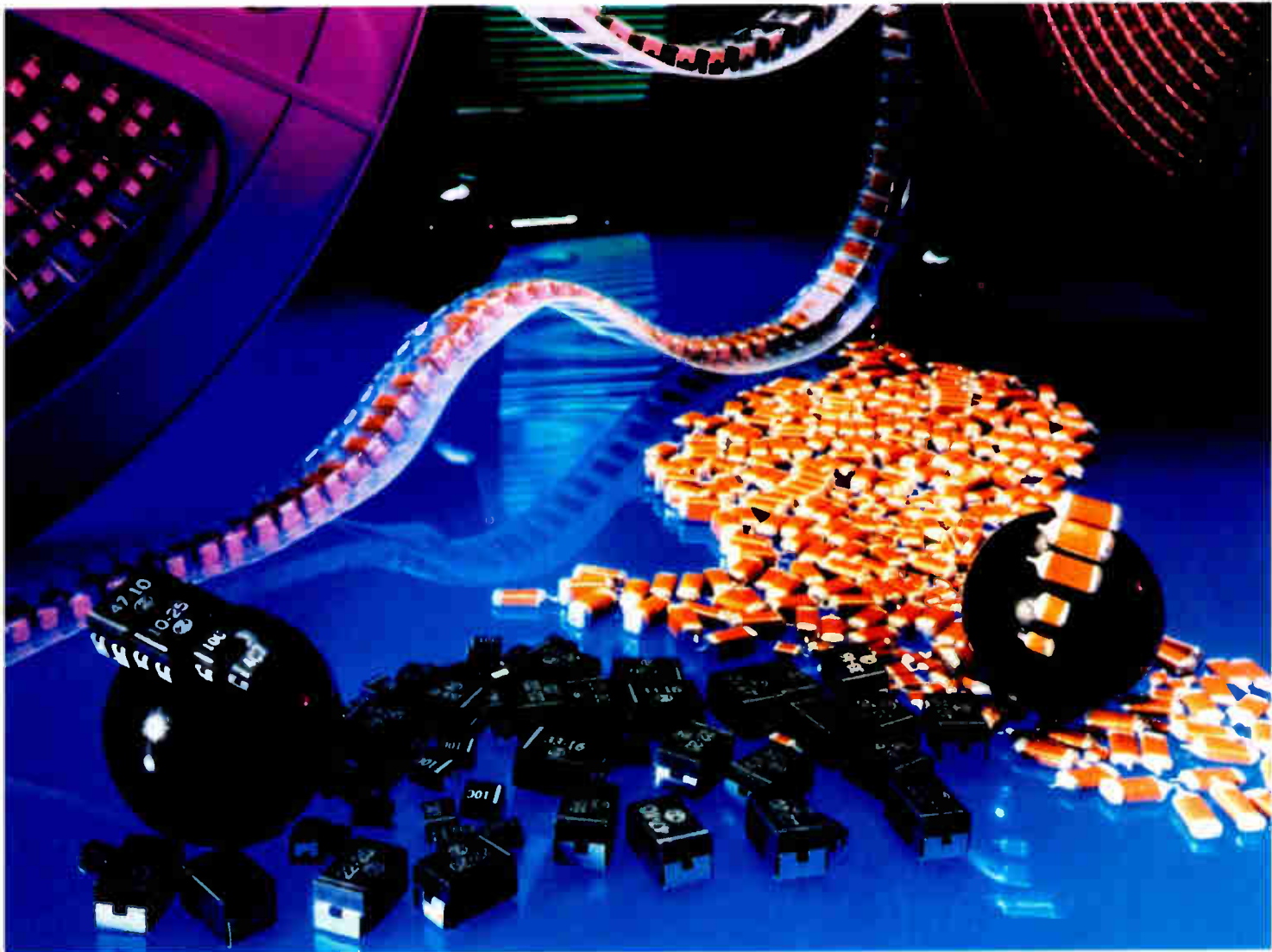
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# WILL QUANTUM-EFFECT TECHNOLOGY REPRESENT A QUANTUM JUMP IN ICs?

Researchers make advances in hunting for successor to conventional transistor

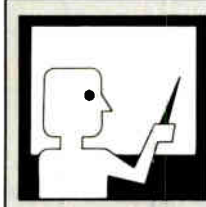
by Samuel Weber

Imagine a new semiconductor technology that cannot be improved because it has reached the fundamental limits of solid-state physics. What pops into the minds of those searching for such a revolutionary successor to today's 40-year-old transistor are quantum-effect devices, which compared to conventional circuits rely on vastly different characteristics of how electrons behave in ultras-small dimensions.

These quantum devices are now showing promise as potential building blocks of superchips with minimum geometries of 0.01  $\mu\text{m}$  and functional densities approaching a million megabits early in the 21st century. Applications for these super ICs will be one-chip supercomputers, real-time pattern recognition, advanced expert systems, and functional densities that approach 1 million Mbits per in.<sup>2</sup> achievable without resorting to cryogenics or exotic techniques for greater 3-d integration.

The electronics world is finally getting a clearer laboratory glimpse of that future age. Device physicists are reporting key advances in applying quantum-mechanical principles in experimental transistor structures. One big step came in September at AT&T Bell Laboratories in Murray Hill, N. J., where researchers revealed development of the first resonant-tunneling bipolar transistor with two peaks in its transfer characteristics. The device—which integrates quantum-effect devices into a conventional bipolar structures—is the first of its kind to achieve multiple peaks. Its developers have demonstrated that it can greatly simplify the implementation of such complex functions as analog-to-digital converters, parity-bit checking, frequency multipliers, and logic.

And at Texas Instruments Inc., scientists in the company's Central Research Laboratories are well under way in efforts to create what they hope will be the world's first true quantum-effect transistor—a three-terminal resonant tunneling device that some believe represents a way station on the road to what is being called the nanoelectronics age. TI, performing the work under U. S. military contracts, is expected in the year ahead to



*EXECUTIVE BRIEFING is a monthly feature of Electronics that provides managers with a concise review of developments in fields that are making frequent headlines.*

apply the quantum-effect transistor concept to an integrated circuit. The work comes on the heels of TI's announcement last spring that its lab had demonstrated the first quantum-coupled device: a resonant-tunneling diode.

As TI and AT&T continue to make progress, device and material work is also picking up pace at leading labs at universities worldwide, IBM Corp., Hughes Aircraft Corp., Philips of the Netherlands, the Walter-Schottky Institute in Munich, West Germany, and at leading Japanese firms, such as Nippon Telegraph and Telephone.

So the research race is on to find a practical replacement for today's silicon transistor, which is expected to run out of

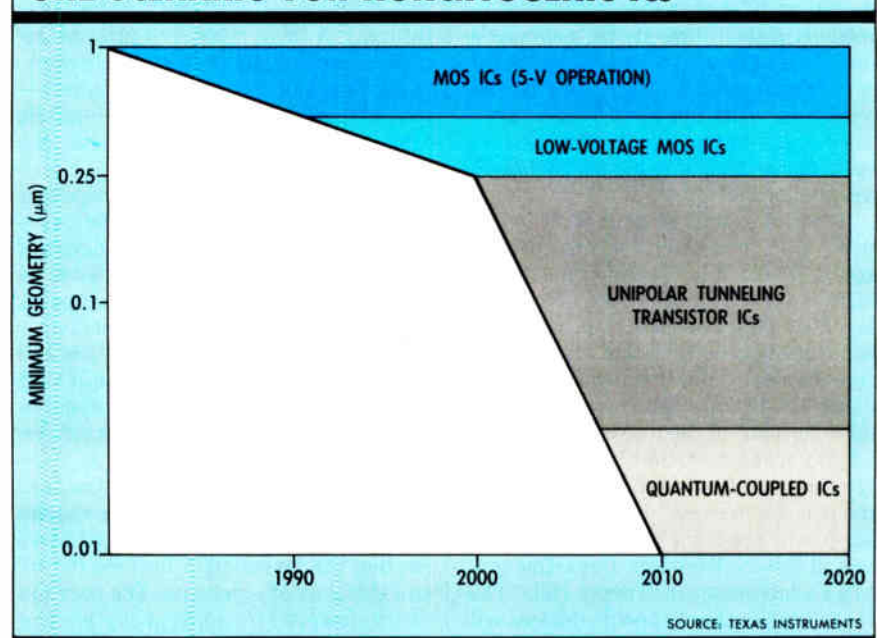
steam as minimum device geometries push below the 0.25- $\mu\text{m}$  barrier in the late 1990s. A technological revolution must occur at that point, if growth in the levels of chip integration is to continue at its historical pace. Right now, most observers are betting on quantum devices.

Modern processing techniques such as molecular beam epitaxy and metal-organic chemical-vapor deposition, along with advanced lithography, have made it possible to produce structures with extremely thin, precisely controlled layers in the form of superlattices and abrupt boundaries with these dimensions.

Ironically, quantum effects have been a problem in shrinking conventional devices, says L. L. Chang, a member of the research staff at IBM's Thomas J. Watson Research Laboratories in Yorktown Heights, N. Y. "Quantum interference causes a lot of leakage. But as you get smaller and smaller, quantum interference occurs naturally and you can't avoid it. If that's the case, you'd better make use of it," Chang says.

In these structures, electrons take on wave characteristics to pass through ma-

## ONE SCENARIO FOR NONCRYOGENIC ICs



As scaling of MOS ICs progresses below 1  $\mu\text{m}$ , operating voltage will be reduced in mid-1990's. "Gap-filler" devices will arrive next, followed by ultimate quantum-coupled superchips.

terial barriers that are normally impenetrable. With quantum-effect devices, researchers believe it will be possible to do away with the space-consuming pn barriers and depletion regions now used in conventional transistors. Heterojunction barriers could be made as small as 100 Å wide using two different semiconductor materials with different energy gaps.

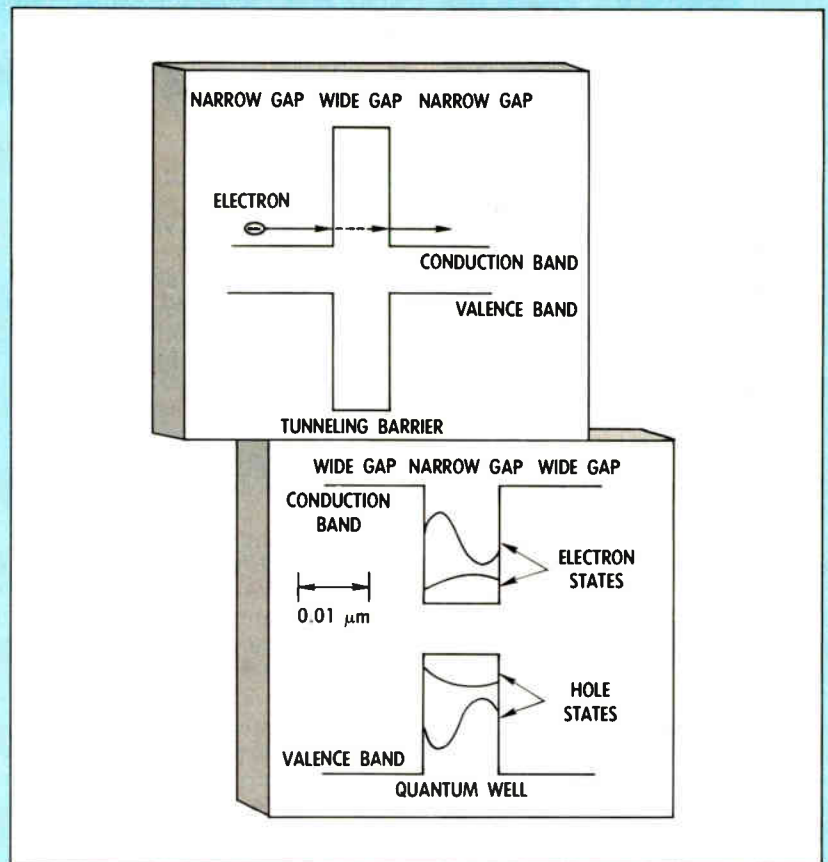
With such a solid-state technology, the hope is to eventually produce quantum-coupled integrated circuits early in the next century that represent the ultimate in density and speed in IC technology. At that point, there would be no more advancements in reaching higher functional densities, says Robert Bate, who heads up TI's push into quantum-effect devices. "That's an important issue because if you can do this, no one is going to do better. No one can beat you," adds Bate, manager of advanced concepts in TI's Systems Component Laboratory of the Central Research Laboratories. "This is the only way that is now being suggested as a way to get beyond the fundamental scaling limits—except for something like biological chips. The alternatives are bigger chips using conventional technology—all of the way up to wafer-scale and three-dimensional integration, which get exponentially more difficult as you stack things up. In my opinion, there is no other feasible alternative."

**WHAT NEEDS DOING.** But before that can happen, much more work lies ahead, even enthusiastic researchers point out. Research work by IBM physicist Richard Webb and others suggests that in the quantum-effect region, interaction of currents and voltages take on strange and anomalous behavior that could render conventional measurement techniques inoperative. Bate says that before the superchips of the future arrive, a circuit-design revolution must occur to establish new principles and design tools for the creation of quantum ICs. He also says a major breakthrough in materials must be made to create a suitable silicon heterojunction technology.

"It is not exactly obvious what to do," he says, in the search for a material to use with silicon in creating energy-gap barriers for quantum devices. "Mostly today, it's a physicist's world. It makes use of physical phenomena that electrical engineers really don't know that much about. The EEs are just now becoming involved in some of the research labs."

But research at Bell labs is already opening up "new avenues of thinking about novel devices," says Federico Capasso, who heads the Quantum Phenomena and Device Research Department at AT&T's laboratory in Murray Hill. "This doesn't mean these specific devices will be used five or six years from now, but we are trying to increase functional density," he says. "We would be foolish to

## TWO BUILDING BLOCKS FOR QUANTUM DEVICES



In tunneling barriers, impinging electrons take on wavelike characteristics to pass through a thin region of wide-bandgap material. In quantum wells, electrons are trapped after moving into a well of narrow-bandgap material from a higher energy level in a wide-bandgap region. Researchers are using these two basic structures to probe the use of quantum effects in ICs.

say that resonant tunneling transistors would replace VLSI circuits in the near future. But there is a broad class of circuits—a-d converters, parity-bit checkers, memories, and frequency multipliers—that we have demonstrated can be achieved with an order-of-magnitude fewer components."

Most semiconductor experts agree that conventional IC technology, which uses pn junctions or depletion layers to control the current flow, will run out of steam before the end of the century. At that point, these conventional devices will no longer function if they are pushed below the 0.25-μm level. What's more, even if they did, the interconnection problem would be almost insurmountable, many device researchers believe.

There are several reasons for the dead end. Electronic switching devices require pn junctions or depletion layers as barriers that can be raised or lowered to control the flow of electrons. The barriers can be lowered by appropriate biasing with a voltage, or narrowed by increasing the doping in the barrier regions. However, a limit will be reached if the barrier is

made too narrow—the electrons just tunnel through and the flow can no longer be controlled.

As the junctions and layers get thinner, the voltage has to be reduced to avoid punchthrough and hot-electron injection, phenomena that can cause reliability problems or device failure. But the voltage cannot be lowered beyond the device's threshold if the transistor is to switch.

**THE CUTOFF POINT.** The point at which operating voltages will have to be reduced for conventional transistor devices will most likely occur at the 0.5-μm range, says TI's Bate. "Changing from a 5-V to a 3.3-V system will get us another generation," he says, referring to earlier expectations that conventional transistor structures were going to run out of gas at the 0.5-μm level. He says the move to three-dimensional integration is also buying conventional technology more time. But "to get below that 0.25-μm you'd have to go to cryogenic operation, which brings another set of problems. So that will leave the door open to something entirely different, a whole new set of device con-

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cepts and architectures," Bates predicts.

That leaves an opening for quantum-mechanical effects, which can come into play when device geometries approach 0.1  $\mu\text{m}$  or the 100- $\text{\AA}$  range. Dimensions of this order approach the resonant wavelength of an electron in a semiconductor material; for example, 200  $\text{\AA}$  in a gallium-arsenide compound at room temperature.

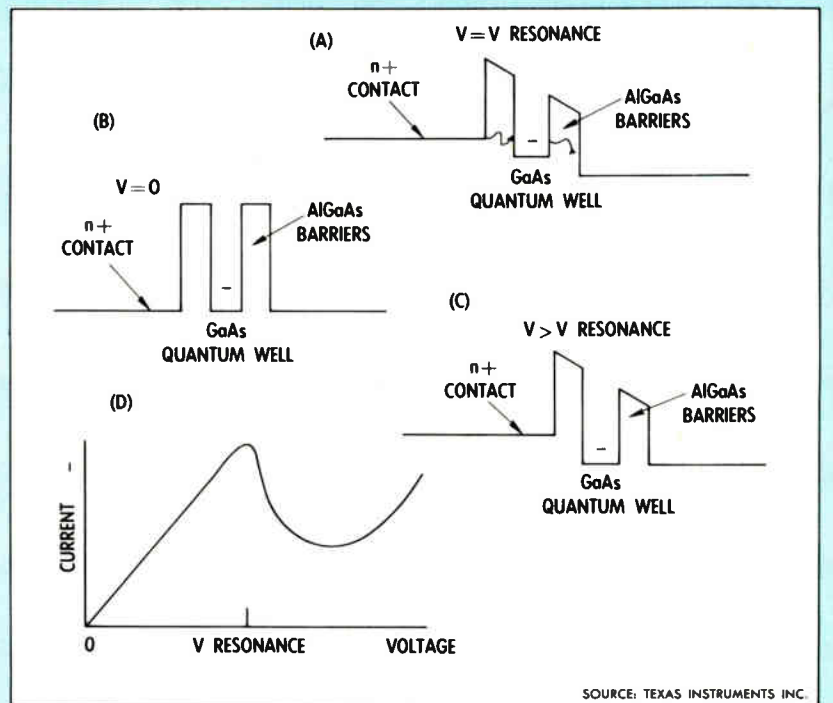
**ENERGY BARRIERS.** In quantum devices, the barriers that control the flow of electrons are differences in energy levels between adjacent regions, rather than the physical barriers presented by depletion layers in conventional devices. A simple quantum structure forms a barrier by means of a heterostructure made up of a wide-bandgap material (one where the conduction and valence bands are relatively far apart) separated by two narrow-bandgap materials.

Because of the ease of making controlled regions with III-V series of materials, GaAs and aluminum gallium arsenide are the most popular semiconductor materials used in research of quantum-effect devices. The regions are thin, on the order of 0.01  $\mu\text{m}$ ; such a barrier cannot be lowered for an electron to cross by conventional means. But if the barrier is made sufficiently thin, the quantum-mechanical effect called tunneling can take place: the electron takes on wave characteristics and crosses the barrier and reappears on the other side instantaneously. Such a structure is one basic building block of quantum devices that is being explored by researchers today.

If instead two such barriers of wide-bandgap materials are separated by a narrow-bandgap material (GaAs between AlGaAs, for example), a so-called quantum well is formed in the GaAs, a region having lower average conduction energy—the Fermi level—than AlGaAs (see diagram, p. 144). Electrons cannot normally pass over this barrier. If a voltage bias is applied across the barrier, however, the bands of conduction states of the barriers become "tilted" in such a way that the Fermi level of the well coincides with that of the barrier, and electrons can then tunnel through.

The tunneling action is very fast, and essentially noiseless. If the dimensions of the well are comparable with the electron wavelength, the band structure and density of electron states is altered. A resonance effect then occurs in the well and substantially increases the tunneling current. As the bias is increased, the current will reach a resonant peak. A further increase in the bias pulls the Fermi level down and destroys the resonant condition. The result is a reduction in current to what is named the "valley" current. The negative differential resistance characteristic exhibited by the device can be utilized in electronic functions such as mixing or switching. But as a two-termi-

## HOW RESONANT TUNNELING TRANSISTOR WORKS



A quantum well is formed by sandwiching a narrow-bandgap material between two barriers formed by wide-bandgap materials (a) with a voltage bias. The energy-conduction bands "tilt," allowing electrons to tunnel past barriers (b). As voltage rises, current peaks at resonance (c), and further increase results in a current "valley" (d).

nal device, it is not very attractive for integration in large-scale functions.

Such well structures—the second building block of quantum devices—have already been used to enhance and tune the light outputs of lasers and other op-

### Device physicists hope to exploit the double-barrier resonant-tunneling diode

toelectronic devices such as detectors and modulators. Enhancing the sheet conductance of a quantum well by doping the neighboring layer of AlGaAs gives the electrons in the well increased mobility without scattering, the basis of such high-speed devices as the modulation-doped FET and the high-electron-mobility transistor and others. But these discrete devices are primarily modified conventional transistors and ultimately are expected to have limitations in fine device geometries and process technology.

The double-barrier resonant-tunneling diode is the basic structure that most device physicists hope to exploit in overcoming the limitations of conventional devices. They aim to accomplish that by placing tunneling diode structures within or in series with conventional FETs or bi-

polar transistors. What's more, resonant-tunneling structures have been built into the bases and emitters of bipolar transistors, aiming at their potential in high-speed switching and microwave devices.

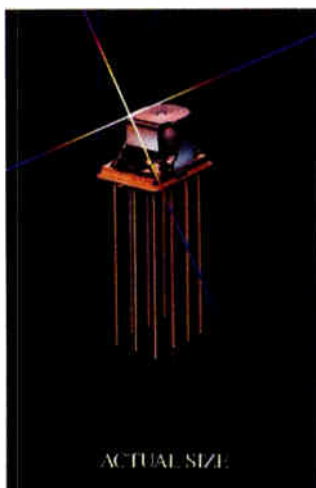
Capasso's group at AT&T announced in 1987 the development of a twin-peak device built by essentially integrating two resonant-tunneling diodes in parallel. The group showed that the twin-peak device could be used as a three-state logic circuit that was switchable from one stable state to another with a voltage pulse. The group extended the concept in September to produce the first resonant-tunneling transistor exhibiting two peaks.

**A BIG ADVANCE.** The advance was obtained, Capasso says, by stacking two double barriers on top of each other, forming two quantum-well sandwiches and placing them between the transistor's emitter and base (see figure, p. 150). The well material is gallium indium arsenide, and the barrier material is aluminum indium arsenide. The substrate is indium phosphide. The resulting bipolar transistor's characteristics can be tailored to locate the peaks anywhere along the voltage axis by varying the well thickness, Capasso says.

Capasso uses a parity-bit generator as an example of one way to put the new transistor to work. "If you try to make a parity generator in the most compact pos-

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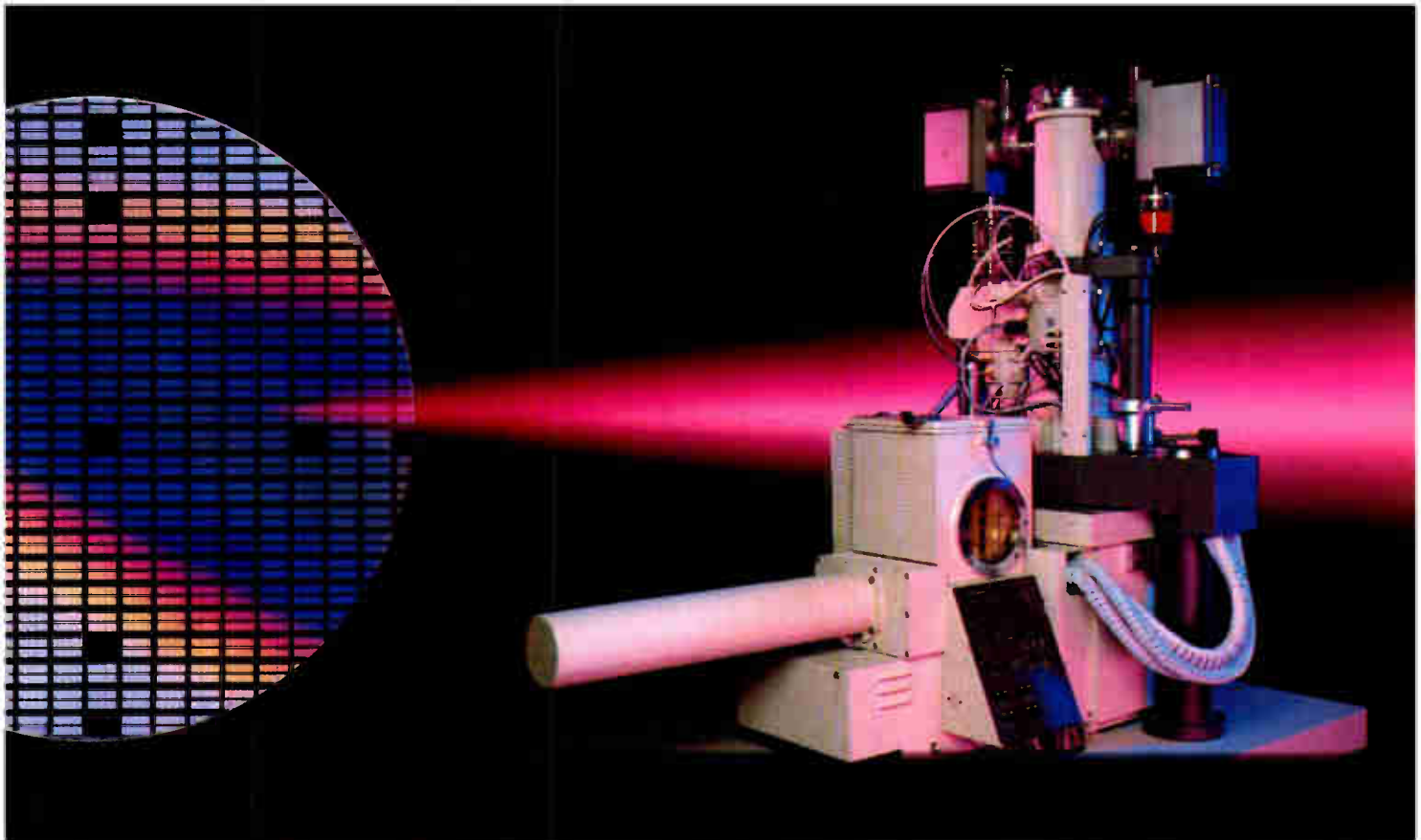
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urrent microelectronic development has attained such a high level that semiconductors containing many millions of transistors will be in mass production by the end of this decade. ▶ And by the mid-nineties the degree of integration is expected to exceed an astonishing 100 million transistors on a single chip. ▶ Philips is playing an important role in this advance. ▶ With ultra-high resolution E-beam pattern generators, called Beamwriters, that can create structures down to the sub-0.1-micron region. ▶ Initially developed by Philips for its own submicron research and production programme, Beamwriters are now also being used by many of the world's leading semiconductor research and industrial organisations. ▶ Including Delft Technical University in the Netherlands; Siemens, the Fraunhofer Society and Karlsruhe Nuclear Research in West Germany; Raytheon, Hughes, TRW and Avantek

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sible way, using MES FETs, you need three exclusive ORs, each of which requires eight transistors," he says. "So you are talking about 24 transistors. I can give you a parity generator with a single transistor of mine." Capasso's vision of the future is one in which conventional design techniques will give way to what he describes as "bandgap engineering" methods.

"You can design devices by thinking directly in terms of the energy band diagrams of the materials," he explains. "Conventionally, the designer thinks in terms of equivalent circuit and layouts. With these devices there is no equivalent circuit. Just tell me what you want, and I will put together certain materials with certain layer thicknesses, and I will achieve the function you want with the right characteristics."

For TI's Bate and others pursuing the pure quantum transistor approach, one of the most difficult challenges is developing three-terminal quantum devices and then interconnecting them in vast arrays to constitute a working nanoelectronic function. In developing a true three-terminal device, a contact must be made to the quantum well, thus giving the equivalent of a transistor base. But making a reliable and low-resistance contact to these very thin layers "will require ingenuity," Bate concedes.

What could be called a "gap-filling" technology will be achieved with such unipolar transistors using limited interconnection, Bate says, predicting that the technology would bridge the span when conventional MOS ICs no longer will hold sway (after 0.25  $\mu\text{m}$ ) and the time when true quantum devices are ready with an architecture that eliminates interconnections altogether. Bate acknowledges that difficult problems are ahead to reach those points, but he adds that the first research steps taken indicate that success is possible.

**LOTS OF DOTS.** The basis of that optimism is research work at TI laboratories and elsewhere on resonant tunnel diodes using what are called quantum dots. A quantum dot is achieved by restricting the lateral dimensions of the GaAs well to the same width as the vertical dimension, essentially forming a "zero-dimensional" well. In such dots, the electronic energy spectrum is so affected that the peak-to-valley ratio of the current is increased and amplified.

Tunneling can occur between the dots. This is the basis of TI's proposed nanoelectronic IC, an array of quantum dots coupled electrostatically with no interconnections. "If spaced within a micron of each other, any of the dots can have two states depending on whether there are electrons in one well and none in the other," Bate says. "You can switch the electrons back and forth between the wells

by creating the resonant tunneling condition with the direction of the bias. You get charge coupling between the two—coulomb coupling action between the electrons in neighboring wells."

New architectural concepts will have to be developed in order to make the quantum-coupled array practical, Bate says. One concept being investigated at TI is "cellular automata," in which quantum-coupled cells in an array are constrained to obey near-neighbor rules and all communicate electrostatically with their neighbors in accordance with prescribed rules. Such arrays have been simulated

### One hurdle is developing contacts inside three-terminal quantum devices

and can perform logical functions with inherent fault tolerance, something that would be essential in a system where there are no nodes to probe.

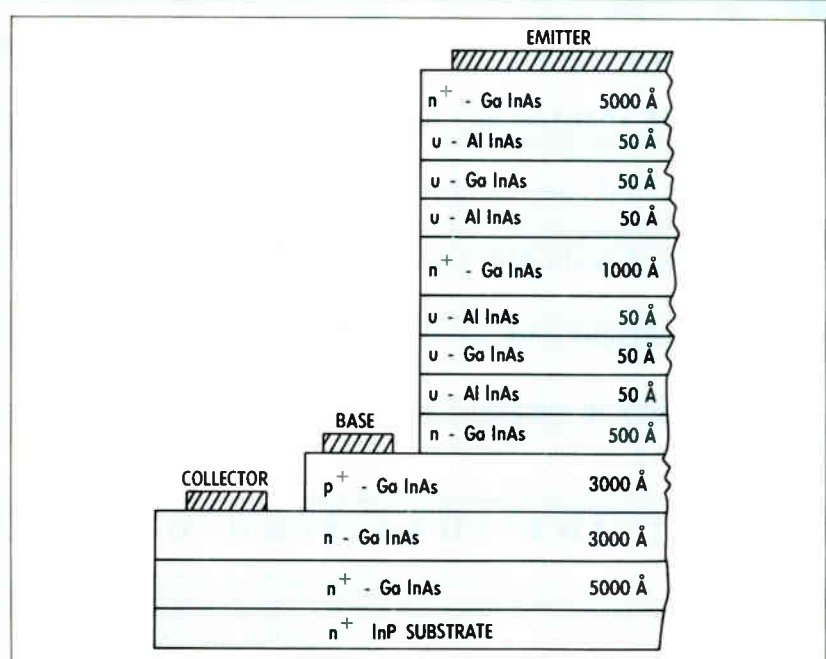
What kind of applications are envisioned for the new era of nanoelectronics? Bate, for one, talks about one-chip supercomputers, real-time pattern recognition systems, and systems that emulate the human brain. AT&T's Capasso thinks in terms of applying the high speeds from quantum devices with the optical communications systems requirements of the fu-

ture. For Gerald R. Iafrate, director of the Electronics Materials Research division of the Electronics Technology and Devices Laboratory, Ft. Monmouth, N. J., the attraction of nanoelectronics lies in the potential for systems in which silicon just won't do the job.

"In a battlefield situation, you need to process a huge amount of data at a very fast rate because you want to know where it's coming from and who's sending it, what the data means," says Iafrate. "You have a horrendous problem of sensing and data processing. I would like to be able to sense information over a very wide frequency spectrum—from mm waves through infrared to the visible—preprocess that information intelligently, move it through a-d conversion and look at some decision-making system. Doing all this in real time is not a trivial feat. I want to be able to process and integrate and correlate at the same time, and address such problems as target recognition, electronic warfare, and smart munitions."

Most everyone agrees that the era of quantum-electronic devices will arrive; the only question is when. It seems clear that the new age is not around the next corner. And some observers believe it is questionable whether the devices will ever totally displace conventional VLSI technology. "Let's face it," says Iafrate, "when the world comes to an end, silicon will still be 80% to 90% of the market." □

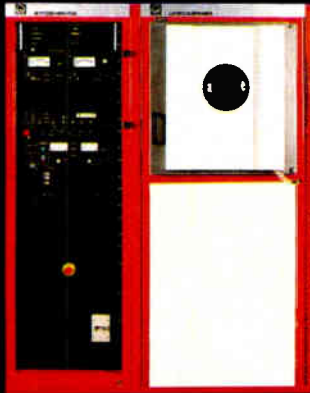
## WHAT APPROACH BELL LABS IS TAKING



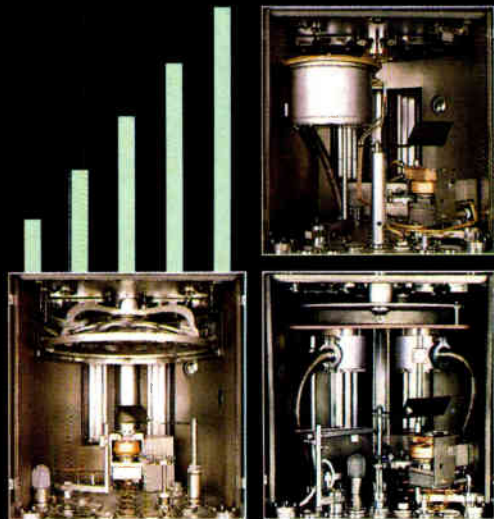
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TC511000AP/A/AZ	1MbX1	CMOS	04'88	05'88	70 80 100	PJ/Z
TC511001P/J/Z	1MbX1	CMOS	YES	YES	85 100 120	PJ/Z
TC511001AP/A/AZ	1MbX1	CMOS	04'88	05'88	70 80 100	PJ/Z
TC511002P/J/Z	1MbX1	CMOS	YES	YES	85 100 120	PJ/Z
TC511002AP/A/AZ	1MbX1	CMOS	04'88	05'88	70 80 100	PJ/Z
TC514256P/J/Z	256KX4	CMOS	YES	YES	85 100 120	PJ/Z
TC514256AP/A/AZ	256KX4	CMOS	04'88	05'88	70 80 100	PJ/Z
TC514266AP/A/AZ	256KX4	CMOS	04'88	05'88	70 80 100	PJ/Z
TC514258P/J/Z	256KX4	CMOS	YES	YES	85 100 120	PJ/Z
TC514258AP/A/AZ	256KX4	CMOS	04'88	05'88	70 80 100	PJ/Z
TC514268AP/A/AZ	256KX4	CMOS	04'88	05'88	70 80 100	PJ/Z
TC524256P/J/Z	256KX4	CMOS	YES	2Q'88	100 120	PJ/Z
TC524257P/J/Z	256KX4	CMOS	YES	2Q'88	100 120	PJ/Z
TC521000P	256KX4	CMOS	YES	YES	N/A	P
TC41000L	1MbX4	CMOS	06'88	07'88	70 80 100	L
THM41000S/L	1MbX8	CMOS	YES	YES	85 100 120	S/L
THM91000S/L	1MbX9	CMOS	YES	YES	85 100 120	S/L
THM91020L	1MbX9	CMOS	02'88	04'88	70 80 100	L
THM9212L	512KX8	CMOS	YES	YES	85 100 120	L
<b>STATIC RAMS</b>						
TMM2060AP	8KX8	NMOS	YES	YES	70 100 120	P28 600mil DIP
TMM2063AP	8KX8	NMOS	YES	YES	70 100 120	P28 300mil DIP
TC5565APL	8KX8	CMOS	YES	YES	100 120 150	P28 600mil DIP 4T Cell
TC5565APL	8KX8	CMOS	YES	YES	100 120 150	SOG28 4T Cell
TC5563APL	8KX8	CMOS	YES	YES	100 120 150	P28 300mil DIP 4T Cell
TC5564APL	8KX8	CMOS	YES	YES	150 200	P28 6T Cell Ultra Low Power
TC5564APL	8KX8	CMOS	YES	YES	150 200	SOG28 6T Cell Ultra Low Power
TC55256PL	32KX8	CMOS	01'88	06'88	(85) 100 120	P28 6T Cell Ultra Low Power
TC55256PL	32KX8	CMOS	01'88	06'88	(85) 100 120	SOG28 6T Cell Ultra Low Power
TC55257APL	32KX8	CMOS	YES	YES	85 100 120	P28 4T Cell Low Power
TC55257APL	32KX8	CMOS	YES	YES	85 100 120	SOG28 4T Cell Low Power
TC51832PL	32KX8	CMOS	YES	YES	85 100 120	P28 Pseudo Static
TC51832SPL	32KX8	CMOS	YES	YES	85 100 120	P28 300mil DIP
TC51832FL	32KX8	CMOS	YES	YES	85 100 120	SOG28 Flat Pack
TC518128P	128KX8	CMOS	YES	03'88	100 120	P32 Pseudo Static
TC518128P	128KX8	CMOS	YES	03'88	160 190	P32 Virtual Static
<b>HIGH SPEED STATIC RAMS</b>						
TMM2018AP	2KX8	NMOS	YES	YES	25 35 45	P24
TMM2068AP	4KX4	NMOS	YES	YES	25 35 45	P20
TMM2068P	8KX8	NMOS	YES	YES	35 45 55	P28
TMM2088P	8KX0	NMOS	YES	YES	35 45 55	P28
TC5561P	64KX1	CMOS	YES	YES	55 70	P22 4T Cell Low Power
TC5561P	64KX1	CMOS	YES	YES	55 70	SOJ24 4T Cell Low Power
TC5562P	64KX1	CMOS	YES	YES	35 45 55	P22 4T Cell Low Power
TC5562P	64KX1	CMOS	YES	YES	35 45 55	SOJ24 4T Cell Low Power
TC55416P	16KX4	CMOS	YES	YES	25 35 45	P22
TC55416P	16KX4	CMOS	YES	YES	25 35 45	SOJ24
TC55417P	16KX4	CMOS	YES	YES	(20) 25 35 45	P24 OE
TC55417P	16KX4	CMOS	YES	YES	(20) 25 35 45	SOJ24 OE
<b>EPROMS</b>						
TMM2764AD-	8KX8	NMOS	YES	YES	150 200	D
TMM2764ADL	8KX8	NMOS	YES	YES	150 200	D
TMM27128AD-	16KX8	NMOS	YES	YES	150 200	D
TMM27128ADL	16KX8	NMOS	YES	YES	150 200	D
TMM27256BD-	32KX8	NMOS	YES	YES	150 200	D
TMM27256BDL	32KX8	NMOS	YES	YES	150 200	D
TC52756AD	32KX8	CMOS	YES	YES	120 150 200	D
TMM27512AD-	64KX8	NMOS	YES	YES	200 250	D
TMM27512ADL	64KX8	NMOS	YES	YES	200 250	D
TC571000D	128KX8	CMOS	YES	YES	170 200	D
TC571001D	128KX8	CMOS	YES	YES	170 200	D
TC571024D	64KX16	CMOS	YES	03'88	200	D
<b>ONE TIME PROGRAMMABLES</b>						
TMM2464AP/AF	8KX8	NMOS	YES	YES	200	FF
TMM24128AP/AF	16KX8	NMOS	YES	YES	200	FF
TMM24256BP/BF	32KX8	NMOS	YES	YES	170 200	FF
TC4256AP/AF	32KX8	CMOS	YES	YES	200	FF
TMM24512AP/AF	64KX8	NMOS	YES	YES	250	FF
TC541000P	128KX8	CMOS	YES	YES	200 250	P
<b>MASK ROMS</b>						
TC5327P/F	32KX8	CMOS	YES	YES	200	F P28
TC531000AP/AF	128KX8	CMOS	YES	YES	200	F P28
TC534000P	512KX8	CMOS	YES	YES	200 250	FF
P = PLASTIC C = CERAMIC F = FLAT PACK D = CERDIP Y = DIE T = PLCC J = SOJ L = LEADED MODULE Z = ZIP *CMOS = TRANSISTOR CELL LOW POWER ** = 10% Vcc AVAILABLE S = SOCKET MODULE * = SELECTABLE SPEED SORT AVAILABLE ** = IN DEVELOPMENT						

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# Telecommunications Industry Update

A REPORT FROM THE NETHERLANDS FOREIGN INVESTMENT AGENCY

*In 1989, the Netherlands will be one of the first European countries to substantially open up its telecommunications equipment and services market—a response to deregulation and market conditions, globalization, and telematics progress. The Dutch telecommunications equipment market is projected to reach nearly \$800 million by 1990, while the European-wide market for equipment and services could exceed \$50 billion.*

*Holland has ensured that its infrastructure — including PTT Nederland which will become a private company January 1 without regulatory responsibilities—will be able to handle not only today's basic speech, text and data exchanges, but tomorrow's needs for fast total digitalization, mobile and other new value-added services.*

*Here are some examples of Dutch developments in advanced telecommunications services that will be available to consumers, industry and governments.*

✂ **ISDN Picture Phone**—Since 1983, the Dutch have been helping to define the operational standards, compatible with both CCITT and CEPT, for a worldwide small band ISDN videophone terminal. This international effort is being coordinated by the PTT Dr. Neher Laboratories and foresees low-priced picture phones for office and home use in 1992. High-quality moving pictures accompanied by high-quality voice are transmitted over a 64kbit/second network. The bit rate is achieved by data compression techniques that eliminate redundant information using a hybrid method combining DPCM- and transform-coding. Encryption will ensure privacy. To enhance a possible videophone service, high quality videotext images can be transmitted with the same equipment.



✂ **Teleports**—Designed jointly by Rotterdam's municipal authorities and its business community, the teleport uses the International Transport Information System (INTIS) for the electronic exchange of standardized messages between shippers and suppliers of all modes of transportation. Shippers and freight forwarders already access the network to send shipping instructions to deep-sea carriers and liner agents. They, in turn, communicate electronically with container terminals. Both PCs and mainframes, equipped with a 3780 emulator and a V22bis modem, can access the network. Access by X.25 protocol will be available soon. Amsterdam is also developing a teleport.

✂ **Transportation Databases**—A standard IBM SNA system with videotext is providing more than 1,500 subscribers throughout Europe with cost savings and real-time information about space availability, type of cargo handled, destinations, departure and arrival times for trucks, trains, ships and airplanes throughout Holland. Called Transpotel, this Dutch database service has expanded through franchising to the United Kingdom, Switzerland, Belgium, Austria, France, Germany and Scandinavia, and soon will extend to Italy and Denmark.

In addition, Holland is a major manufacturing location not only for N.V. Philips's data communications products, but also for Alcatel, N.V., which builds and markets its System 12 for small and medium-sized firms; for Swedish multinational L.M. Ericsson, which manufactures telephones for the Dutch PTT and other telecommunications equipment; for West German multinational Siemens, which produces data communications products; and for the AT&T/ Philips joint venture, which is building a new generation PBX.

Further, three technology universities—at Delft, Twente and Eindhoven—and more than 100 technical institutes along with the Netherlands Organization for Applied Scientific Research (TNO) and major software houses assist companies, regardless of location, with research and development from defining systems needs to designing networks to building prototypes or writing code.

## Netherlands Foreign Investment Agency

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For more information about THE NETHERLANDS; RIGHT IN THE CENTER FOR INVESTMENT, complete the coupon below and mail it to: Executive Director, Netherlands Foreign Investment Agency, One Rockefeller Plaza, New York, NY 10020

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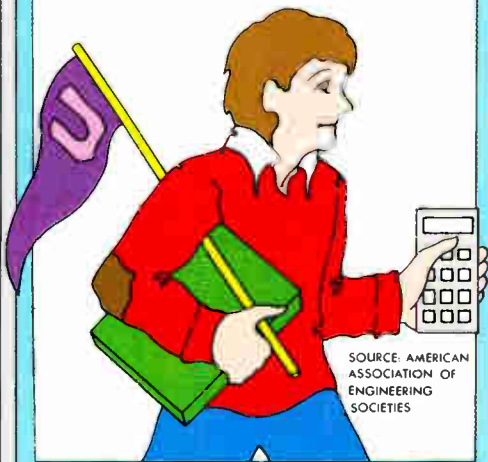
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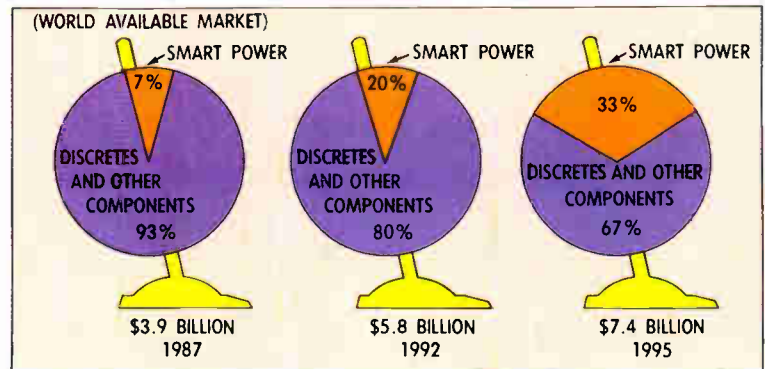
# INDICATORS

## U.S. ENGINEERING ENROLLMENT TURNS DOWNWARD

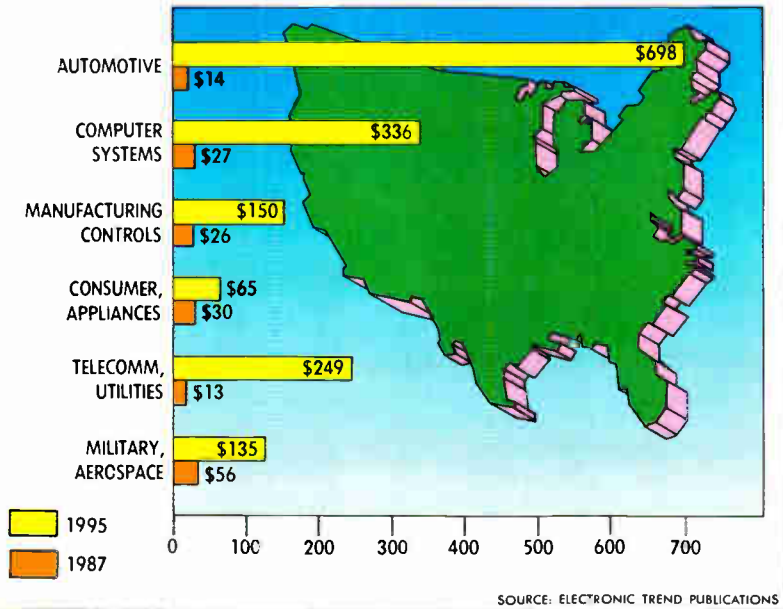
	All engineering undergraduates	BSEE	Computer Degrees
'78	311,237	64,524	8,632
'79	340,488	70,123	10,908
'80	365,117	77,103	13,901
'81	387,577	86,146	17,901
'82	403,390	94,374	21,838
'83	406,144	106,240	22,242
'84	394,635	110,666	21,367
'85	384,191	112,205	20,712
'86	369,520	112,143	19,060
'87	356,998	104,634	19,060
'88	Early reports suggest figures will hold steady with 1987 levels.		



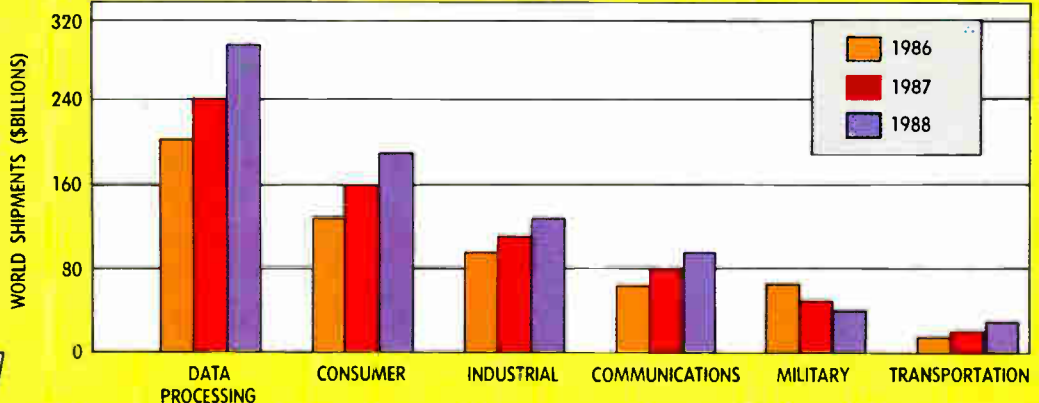
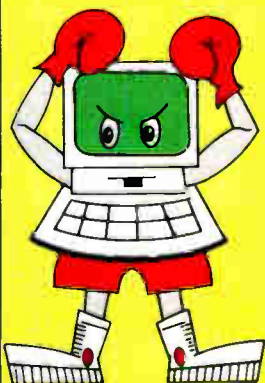
## INTEGRATED POWER ICs LOOKING SMART



## HOW SMART POWER WILL GROW IN U.S. INDUSTRY



## COMPUTERS AND CONSUMER SYSTEMS WIN BIG



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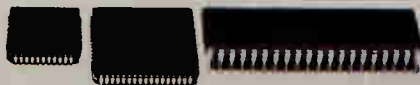
costs. And your system gets more reliability.

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CA 95054, mentioning "8051 micro-  
controllers".



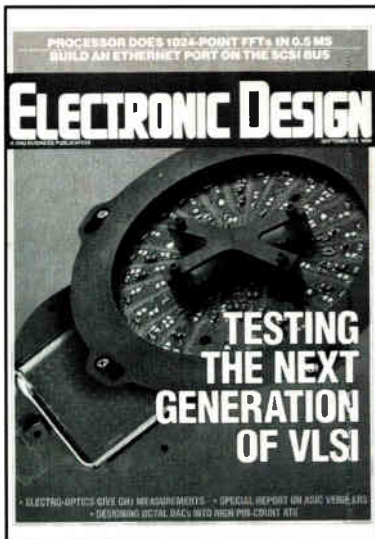
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# EMBEDDED CONTROL: MORE THAN MIPS

**N**o single microprocessor architecture can meet all the diverse requirements of both the general-purpose programmable market and the embedded-control applications market. Make no mistake, the two markets are distinctly different.

Selection of an architecture for programmable use is driven solely by the targeted application's software—Unix, DOS, et al. However, three criteria drive the buying decision for a high-end 32-bit embedded architecture: breadth of product line; hardware and software tools; and supplier strength.

Embedded designs can be divided into four classes: high-functionality, data control, event-control and systems control. The key point is that original equipment manufacturers' are demanding a single high-end 32-bit family that spans all classes of embedded applications. Breadth of line is now a requirement, not a luxury.

The microprocessor architecture "buy" decision is no longer made by design engineers. Gone are the days when a unique processor and its supporting tool-set could be chosen on a project-by-project basis. Instead, senior management demands a single architectural base that can serve all its needs.

Applications include high-functionality systems, parallel-processing systems, and military systems. The system-control segment includes applications in image processing, robotics, process control, and telecommunications. Data-controller applications include protocol handlers and input/output controllers. Event-control systems include engine, motor, machine, and instrument control devices. That's a lineup that can only grow more diverse.

Features such as on-chip integration of peripheral functions and ease of systems-level design join total system costs as critical selection criteria. Blazing speed in the millions of instructions/s range are important, but mips alone can't define high-performance in an embedded machine. System performance is what's important—characteristics like bus bandwidth, interrupt response time, and the ability to achieve high data-transfer rates are key, as is a highly tunable interface to the external hardware environment.

A responsive interrupt controller is

an absolute necessity. And the interrupt controller must consist of multiple input sources, along with sophisticated interrupt-control logic to handle prioritization and synchronization of external events. If the interrupt controller is integrated on-chip, the chip-count reductions go right to the bottom line.

Compute-intensive embedded nu-

higher-priced video RAMs.

Software is responsible for the "hidden intelligence," or functionality of embedded-application products. While application-program problems on a personal computer may cause some temporary end-user aggravation, embedded-system-program problems can destroy expensive end-user systems.

Embedded architectures should offer ease of programming in a high-level language such as C, as well as software-debugging capabilities and reliability. Along with easy coding, a robust software-debugging capability must be resident on-chip to guarantee correctness. A high-performance embedded processor must also support high-level languages and real-time kernels in order to provide an appropriate software-development environment.

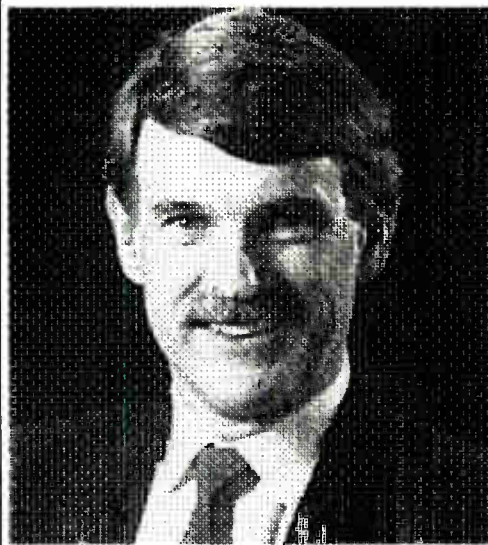
In the embedded market, the program developed by the OEM system programmer controls the functional destiny of the end product. Because the program may not be easily accessed, tested, or debugged once in use, a processor architecture designed for embedded applications should include self-test and on-chip debugging.

Performance can also depend on programming. The fast-response, time-critical missions of embedded controllers requires that critical portions of code must still be generated in assembly language. This means that pipeline hazards and forbidden instruction sequences should be avoided.

All that aside, the hottest topic of debate right now revolves around which is better—complex or reduced instruction set computers. A compromise solution, drawing on the best of both, is called for.

Practical embedded-computing solutions may exploit specific RISC techniques—load-and-store memory addressing, register-to-register operations, or register scoreboarding—to increase execution-speed performance. But benefits such as straightforward instruction sets for easy programmability and on-chip self-testing and debugging are not characteristic of RISC design.

The last factor in choosing an embedded architecture is the issue of supplier strength. This is not a matter of a big versus a small company. It is a matter of having the service and commit-



**DAVID L. HOUSE**

*Senior V.P. and General Manager, Microcomputer Components Group, Intel Corp., Santa Clara, Calif.*

*Age: 45*

*Career path: Joined Intel in 1974 and Intel's executive team in 1982. Took control of Microcomputer Components Group in 1984.*

**HOUSE'S STANCE:**

**"Don't measure 32-bit embedded controllers by mips alone."**

merics or image-processing applications require not only integer math, but floating-point math precision as well. Integrated on-chip floating-point processor units contribute not only to increased performance levels, but reduce systems cost.

Embedded-system costs are directly affected by the costs of both glue logic and memory subsystems. If an embedded processor architecture requires seven programmable-logic arrays—instead of 17 or 27—those savings go right to the bottom line. A system that can deliver performance using standard DRAMs will save money for a manufacturer over one that requires

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ment to meet the needs of embedded-architecture customers. This kind of commitment is demonstrated by complementing a broad line of silicon offerings with documentation, application notes, and a knowledgeable sales staff that is able to give support.

Again, no single microprocessor archi-

ture will fit the distinct requirements of both the embedded and reprogrammable markets. So it makes a lot of sense for Intel—or any chip supplier—to spend its transistor budget by offering its customers different architectural solutions designed to fit the specific requirements of each of the markets.

**Q ELECTRONICS:** How would you define the difference between the two markets—reprogrammable general purpose chips and embedded chips?

**A HOUSE:** The reprogrammable market is driven by application software. The embedded market is driven by four things: the flexibility of the architecture and its technical features, software and hardware development tools, the breadth of product line, and the stability of the supplier.

**Q ELECTRONICS:**

When you talk about dedicated processors, where do ASICs fit in?

**A HOUSE:** What people are doing today is applying 32-bit processors to embedded applications and putting either standard parts or custom chips around them. I think in the future we'll see application-specific derivatives of these embedded processors aimed at the highest-volume applications. I suspect that optimization around the laser-printer type of applications will be one of the first, because that's one of the largest markets around 32-bit processors.

**Q ELECTRONICS:** How important is the 32-bit market for microcontrollers? How big is it?

**A HOUSE:** It's a small but leading-edge segment of the market. In terms of actual volume today, the numbers are pretty infinitesimal. In dollars it represents a larger percentage, because these are higher [profit] products.

**Q ELECTRONICS:** One of the things you bring up in your article is that speed isn't the only thing...

**A HOUSE:** MIPS aren't the only thing. A unique thing about embedded controllers is that interrupt response time is often the most critical parameter. Also, running some critical inner-loop programs is more important in the embedded market place. For example, an inner loop can include floating point capability, and having on-chip floating-point makes a difference in performance. In other cases, maybe in event control, where you're responding to interrupt conditions, speed might be measured not in MIPS or in me-

gaflops, but in interrupt-response time. There's a much wider range of performance requirements in this market than in the reprogrammable market. So it's not quite as easy to measure horsepower.

**Q ELECTRONICS:** How does a customer protect himself from being caught up in—and falling victim to—the MIPS war?

**A HOUSE:** He's got to understand his application and what the chip will do. I mean it might have all the MIPS in the world, but not have a fast enough interrupt-response time, or enough megaflops or whatever the critical performance factor is.

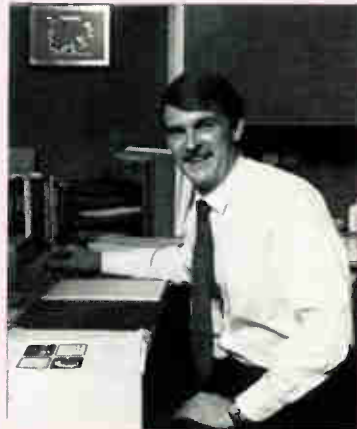
**Q ELECTRONICS:**

What about CISC vs. RISC, which you touch on toward the end of your piece?

**A HOUSE:** RISC, in its purest form, is a real problem for embedded-control design. Typically in embedded-control design the tight inner loops, the performance-sensitive areas, wind up getting programmed in assembly language. A pure RISC machine with a very limited number of instructions and very limited addressing modes is very difficult to program in assembly language. You'd like to have a little more robust instruction set, a little more forceable memory addressing, if you're going to be dealing with this thing on a human level. The whole principle behind RISC is that everything's programmed in high-level language. Increasingly, high-end embedded applications are programmed in high-level languages, like C, but invariably, the real performance-critical work gets recoded in assembly language. You can always optimize for higher performance with assembly language than if you're using a compiler. In the programmable market you can handle a pure RISC machine, but in the embedded market, I think you'd like it slightly enhanced, and that's what we've done with the 80960.

**Q ELECTRONICS:** Are there plans to use the 80960 to build an ASIC core?

**A HOUSE:** That's in our long-term plans. I think ultimately you'll see customers getting customized versions of standard products. □



# A TALE OF TWO ROADS LEADING INTO JAPAN

How a pair of U. S. firms got footholds in the market

**F**or U. S. high-tech companies, penetrating markets in the Far East has always been tough on the ego and on the bottom line. In addition to legislated barriers, there are cultural differences and deals breaking quickly across several time zones, all of which makes for too many fumbles. To prevent them, a U. S. executive can either settle down in Japan or find a good, reliable representative there able to do business his way.

That's why the chief executive officer of one East Coast semiconductor house has lifted a page from Marco Polo's journal and settled down—for a while at least—in the land of the 4-Mbit dynamic random access memory. But while Marco Polo set off for Cathay seeking rubies—and returned with macaroni—Standard Microsystems Corp.'s Paul Richman looked further east—to Japan—in his quest to get an edge on the competition. So far, he's set up a new subsidiary and netted a big-time Japanese corporate partner and a Far East order book that just keeps getting fatter.

But success, like ice cream and operating systems, comes in many different flavors. Retix, the California-based leader in Open Systems Interconnection software, opted for the more conventional approach of using a distributor. Its criteria for choosing tiny Custom Technology Inc. of Tokyo, however, was anything but conventional. It didn't rise to the bait dangled by bigger Japanese firms. "We liked the fact that it showed real aggressiveness in a Western way," says Retix vice president of international sales Bjorn Ahlen. "Its whole structure is Western."

SMC's Richman had quite a different personality in mind for his subsidiary. From the start, he says, Toyo Microsystems Corp. was to have "a Japanese face and a Japanese mind." Back in Hauppauge, N. Y., headquarters for two months to catch up with SMC's operations, Richman adds that at least one critical aspect of Toyo's personality will be directly inherited from its

parent. "SMC has always been market-driven," he says. "We ask our customers what they want and need." This wasn't happening in the Far East because "we didn't have the opportunity to build high-level business relationships."

Forging those relationships had become imperative to survival. Through



the 1980s, SMC and other small- to mid-sized semiconductor houses have seen the markets for data communications chips and computer peripheral integrated circuits for storage and display applications gravitate to the Pacific Rim. SMC decided to follow its markets with more than a sales force. Design expertise for altering application-specific and customer-specific ICs also had to be local.

Having struck on the idea of forming a Japanese subsidiary as a means of market entry in the Far East, SMC faced three interrelated problems: attaining for it the corporate prestige so important in Japan; attracting the best and brightest local talent; and, building long-term, high-level relationships with

by Jack Shandle

customers. SMC figured the best solution was to find a strong Japanese partner that would be willing to take a minority share of Toyo Microsystems as a means of accessing SMC's technology. Prestige, recruiting and high-level contacts would, it was believed, come along with the right partner.

"Yes, partners are there," says Richman, "and it's a lot easier to find one than you might imagine." What's more, the Japanese will act quickly, particularly when the U. S. firm's CEO is on the scene. By using its investment banker, Merrill Lynch Capital Securities, SMC discussed alliances with several companies before negotiating an equity deal for Toyo with Sumitomo Metal Industries Ltd. of Osaka, a leading Japanese steel maker.

On Nov. 11, 1986, Sumitomo purchased 20% of Toyo for the equivalent of \$13 million in common and preferred stock. Sumitomo has a spot on Toyo's five-member board of directors. When the deal was struck, Toyo had no office, no employees, and no sales. Standard Microsystems contributed technology: it gave Toyo nonexclusive patent licenses, nonexclusive technology rights, and an exclusive right to sell its standard products in Japan.

Thanks in part to the galloping value of the yen, Toyo is still operating on the Sumitomo funding, even though it is running an operating loss that will continue in its "formative years," according to Richman.

Not too long after SMC sealed its deal with Sumitomo, Retix was struggling with a similar set of problems. It already had a big lead in the emerging market for software and systems that let disparate computers communicate via OSI protocols, and wanted its lead to be worldwide. Japan and the Far East were posing the biggest problem. "We were afraid it would take too long to hire the right people," says Bjorn Ahlen, Retix's vice president of international sales. "We could easily have spent a year and \$2 million and still not have the right people."

So the company began looking for a distributor. Instead of hooking up with a big one, Retix chose tiny Tokyo-based Custom Technology Corp. in March 1987. The choice solved the same three problems Richman and SMC faced. Although a small company with only 28 employees, Custom Technology is partially owned by SRC Corp. Ltd., a Japanese software conglomerate. "They

had the contacts," Ahlen explains.

Besides the prestige factor that came along with SRC's part ownership, Custom Technology was able to help itself in recruiting by taking advantage of a recent change in Japanese culture. Some young Japanese looking for a fast track up the corporate ladder are not content with the traditional path of working 15 years in the vineyards. "They [Custom Technology] were able to attract good people from large companies—young people who had made contributions that they felt were not recognized," says Ahlen.

Recognizing that Far Eastern customers want a high level of service, both SMC and Retix have structured their Japanese strategies to offer more than marketing capabilities. Although Toyo began life as a liaison office, its mission now is to learn how to modify SMC's products to customer specifications. It has already delivered a local-area-network board, says Richman, and its complex-instruction-set-IC-design capability went on line in September. "We hope that a few years from now, we'll have a crack design team there that can do jobs that used to be done in the U. S.," he says.

Similarly, Custom Technology is adapting Retix's products to the Japanese market. "There are close to two million NEC Corp. PCs in Japan—nearly the whole market," says Ahlen, "and it has a different bus so we have to adapt our board." Retix is also considering a partnership with equity arrangements going both ways, he says. "It would be involved with support for OEM customers and [product] development—especially adapting to local government standards. That's certainly the case in Japan, where they're doing their own thing and you comply or you don't sell."

A key difference in the SMC and Retix strategies is the one Richman seems to enjoy most: personally forging high-level relationships across the Far East from his home-away-from-home base in Tokyo. Regardless of how a U. S. chip maker approaches the Japanese market, says Richman, growth will be slow because of intense loyalty to Japanese firms and proven vendors. But the same SMC products that are meeting resistance in Japan are readily accepted in Korea and Taiwan. Richman uses Japan as a base to make frequent trips to both countries. After a CEO-to-CEO meeting, Richman says, "I can pick up the phone and talk to him in the same time zone instead of staying up until early morning to place the call."

Having a CEO in the Far East pays other dividends. In one instance, the president of a competing Taiwanese

company, who Richman declines to identify, wanted to see Richman in a hurry. Since Richman had already scheduled a trip to Korea, he suggested they meet there. The result was an ASIC that will be designed in the U. S.

The pace of business in Japan is also quickening. Toyo received its first major order to develop a customer-specific IC for data communications last December from Kokusai Denki Co. of Tokyo. "Since Toyo's inception," says Richman, "our orders from Japanese companies have been slowly but steadily increasing. But the opportunities we have to penetrate the Japanese market are now appearing at a rapid rate."

Richman acknowledges there is a downside to being on the Pacific Rim: handling the transition when he leaves Tokyo. To smooth the changeover, he has worked out a plan that follows his "Japanese face and mind" tenet. Toyo will get a Japanese president when Richman returns to Hauppauge, and it's board will rely heavily on its partner Sumitomo's advice in the selection, he says. "It doesn't make much sense to get a Japanese partner to help you learn the ropes and then overrule him."

With multimillion-dollar bookings on the horizon, SMC and Retix rate their Far East strategies successful. Sales have grown in the spurts characteristic of startups. Success can be fleeting, and with a cautious eye on the competition, neither company is disclosing the financial details of their moves. "Selling in the Far East takes about five times more patience than selling in Europe," says Ahlen. "At first, the Asian customers seem to be tire-kickers, but then, bam, they want to buy; and then they want to move fast—faster even than in the U. S."

## PITCHING BONUSES TO KEEP EMPLOYEES GETS MORE POPULAR



It's an old story: hiring good people is sometimes easier than holding on to them. So today, more and more companies are as innovative in developing their bonus and incentive strategies as they are in designing the products they sell.

Some companies now integrate factors such as overall product quality into their bonus payout, while others, have merged the concepts of bonuses with profit-sharing. Still others have worked a value-over-time factor into their programs to award inventors when patents are issued.

Archive Corp., a Costa Mesa, Calif., maker of cartridge tape drives for computer data backup, bases bonuses on

three elements. Two of these are commonplace—total corporate profit and individual performance—but the third is unique. B.J. Rone, vice president for finance and administration, calls it the Q-factor, and it carries equal weight with the other two in the bonus formula Archive has worked out. The Q-factor takes into account the statistical measurements of quality, defects, and on-time shipment, for the entire company. Rone says he knows of no other similar approach, and says he's been approached by other companies interested in cloning it.

Incentives aren't limited to bonuses at Archive, though. The company also has a profit sharing plan for managers. "Below the management level, they like cash better than anything else," Rone says. "But managers like to build net worth and want a mix of some cash and some equity." Payouts come quarterly for profit sharing and annually for bonuses. Non-managers can expect an 8% to 12% profit sharing contribution and managers from 15% to 30%.

Cray Research Inc., the Minneapolis supercomputer maker, has a two-tiered profit-sharing plan that gives bigger incentives to the 10% of its employees in the management ranks. At the officers' level, for example, the profit-sharing portion of compensation amounts to four times the base in the company-wide plan. "People at the top have more of their compensation at risk," says John F. Carlson, executive vice president and chief financial officer.

The overall program is tied to annual results, with each year's payout split between cash and deferred compensation. The cash portion is significant: last year the average bonus was equal to about one month's salary for each Cray employee. And the deferred portion makes up for the fact that Cray doesn't offer a pension program.

Texas Instruments Inc., like many other technology companies, awards bonuses for successful patents and inventions—\$739,500 in 1987, for example—but what makes its program unique is that the company reviews the value of the patent to the company twice after the initial award—three years later and then after another six years. Over a nine-year period, inventors have received from \$1,000 to as much as \$175,000. "The cash awards both motivate and recognize employees," says Mel Sharp, corporate staff senior vice president. "As a result, we have kept some inventors at TI."

And that pays off handsomely, says Sharp. "Intellectual property is fundamental to our technological leadership," he says. "It is the basis of our future products and profits." —Wesley R. Iversen and Larry Waller

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# COMPANIES TO WATCH

## WILL THE GE PIECES BE ENOUGH TO PUT HARRIS BACK ON TRACK?

Acquisitions give it a name in new markets and triple semiconductor operations

### MELBOURNE, FLA.

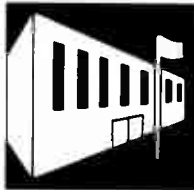
A decade ago, Harris Corp. was riding a rocket to stardom. Strong growth in semiconductors, government systems, communications, and computers helped Harris nearly double its sales in the five years from 1978 to 1982, and analysts predicted more of the same through the rest of the decade. Then things went bad: sales growth slowed to a snail's pace and profits plummeted. While Harris earned \$128.1 million in pretax profits in its fiscal year 1982, it has exceeded the \$100 million mark only twice since. The last fiscal year, which ended June 30, was no different with pretax profits that came in at a disappointing \$86.5 million.

But Harris is trying to get back on track. In August, the company shelled out a reported \$250 million to buy GE Solid State—the combined operations of the former RCA Solid State Division in Somerville, N. J., and Intersil of Cupertino, Calif.—from General Electric Co. The move almost triples the size of Harris' semiconductor operations, and it gives the company an established name in several markets—including automotive electronics—that it has not been in before. But debate lingers—can Harris translate its new bulk into growth?

Elsewhere at the Melbourne company, Harris is tightening the bolts to squeeze more performance out of some lifeless businesses. Last year, Harris realigned some of its operations, consolidating the struggling Lanier division, which makes office automation equipment, into the Information Systems Sector, which has stumbled lately.

**NEW SIZE.** Indeed, Harris has been looking over its shoulder for a while, says James Magid, of Magid Research in New York. There were rumors, he says, that it might be ripe for a takeover. "The company is all sizzle from the 1970s," he adds. "It's been a lackluster performer since then. Harris was running out of options."

The Solid State purchase, and its integration into Harris' existing structure, is the key to Harris' strategy to revive itself. While the operations don't offer cutting-edge technology, they do offer size:



sales were almost \$550 million in 1987, nearly double that of Harris, and much of it comes from high-volume, low-overhead product lines, or from well-protected niches. With the combined chip business, Harris leapfrogs National Semiconductor Corp. to become the No. 1 supplier of ICs to the U. S. military market, and joins AMD, Intel, National, Motorola, and Texas Instruments as one of the six biggest merchant chip makers in the U. S.

The added muscle in the military market, where Harris as a whole does about half of its business, will be a big boost. "They've just about cornered the [radia-

**'Harris will be getting size, but are they getting technology?'**

tion-hardened] chip market," says a marketing executive who has worked for both Harris and GE. "Rad-hard ICs are an old technology, but Harris has had it and cultivated it over the years, and they're known for it. The addition of GE's silicon-on-sapphire technology only strengthens them in a market that's going to be more and more important because of the increased need for rad-hard technologies both on earth and in space."

Although no accurate figures are available on the size of the rad-hard chip market, Harris and GE were acknowledged to

be the top two producers of the technology before the deal. The executive, who asks not to be identified, adds that with the addition of Intersil's analog products, Harris is now "a formidable competitor" in that market too.

But it takes more than bulk to be competitive, says Dan Hutcheson, president of VLSI Research Inc., a market research outfit in San Jose, Calif. "Harris is getting size, but are they getting technology?" he asks. "The added size will help fund advanced R&D, but only if they can keep GE's operations profitable." There's no guarantee that Harris can, he adds. "Nine out of 10 acquisitions don't work."

That job will fall to Jon Cornell, the president of Harris' Semiconductor Sector. Described by a former colleague as "brilliant" and "very demanding," Cornell will have to move quickly to meld the two organizations and to settle down a sales staff at Solid State that has suffered through almost three years of rumors that variously had the operation sold off to Chrysler, Philips, and SGS-Thomson, among others.

With Harris growing in one quick leap from a \$300 million semiconductor business to one that is now worth over \$850 million, Cornell has some juggling to do in his management ranks. Carl Turner, the vice president in charge of GE's semiconductor businesses, will retire after the deal is consummated, whether at its planned completion in December or later, but the fate of other GE executives remains to be seen. A rocky transition from one management team to the next could

### HARRIS GRABS THE MILITARY IC LEAD

1986		1987		1988	
Company	Sales (\$ Millions)	Company	Sales (\$ Millions)	Company	Sales* (\$ Millions)
Texas Instruments	160	National	245	Harris	296
Harris	150	Harris	180	National	265
Fairchild	148	AMD	170	AMD	175
AMD	139	TI	160	TI	170
National	118	GE**	114	Matarala	110

\* Projected.  
\*\* Includes about \$11.5 million from GE Microelectronics Center, which was not included in the sale to Harris.

SOURCE: INTEGRATED CIRCUIT ENGINEERING CORP.

spell trouble for Harris.

There are also radically different cultures at the two companies, hints one former employee of both. "Harris has a much faster-moving management," he says. But Harris is thin in middle management, he adds, and with the size of the new organization, "GE's middle managers will be very important."

Harris has faced management turmoil in the chip sector before. When Don Sorchych, who built up the division in the 1970s, departed in 1980, it took almost four years for the unit to recover, says Magid. Top corporate management failed to comprehend the delicate manufacturing processes, uncertain yields, and cyclical nature of the chip business, he adds, and several promising young executives left—including James Dykes, who has since run the chip operations for GE (until the RCA merger) and Taiwan Semiconductor Manufacturing Corp. (see p.169). In some ways the company has never recovered: it was an early leader in CMOS technology, but has not seen the broad success that has helped other CMOS chip makers. "Nothing against Jon Cornell, but they lost their vision when Sorchych left," Magid says.

**RARE MIX.** Still, the merger has the makings of a very good deal, most experts agree. Rarely have two chip operations been so complementary. Both companies specialize in CMOS, the military, analog ICs, and in application-specific chips. The bonus for Harris is GE's merchant businesses, which are strong in power MOS and audio and video components for consumer electronics, and have a history of close working ties to the major automotive companies. "You're going to see Harris come out a much more potent merchant supplier, where in the past they were kind of sleepy," Hutcheson says.

Harris is particularly interested in the automotive business, which brought GE more than \$110 million in 1987 sales. Like the military market, which accounts for just over half of Harris' chip sales, automotive customers demand extensive documentation, strict quality control, and strong price controls. Although the business is tough, Solid State executives say, it is worth it because the auto makers buy products in huge volume and the sales life for a given product can run for three, four, or more years. So even though the margins on those parts are slim, the volume helps keep plants running at full capacity, and that, in turn, keeps yields high.

Despite Harris' new muscle, there are those around the industry who don't think either company has much to offer. Critics at GE's Microelectronics Center in Research Triangle Park, N.C.—the one part of GE's chip-making hierarchy that it did not sell to Harris—deride the Solid State division for its old-line 2- and 3-µm

technology, the age of many of its engineers, and its lack of a leading-edge chip technology—or even a route to develop one. Harris, in the mean time, "has always had a reputation for being out in left field somewhere because, well, they're from Florida and they do a lot of work for the military," Hutcheson says.

But that reputation is not entirely fair, he adds. "Harris is no slouch technologically," he says. "In CMOS, they've been running circles around some of the Silicon Valley firms, because they've been doing CMOS longer and better than companies like Intel." —Tobias Naegle

## BATTLE-HARDENED MICRON SEEKS NEW CONQUESTS

### BOISE, IDAHO

**M**icron Technology Inc. has survived more than its share of battles. It has walked through a considerable amount of red ink, and has even taken on and beaten back the mighty Japanese semiconductor establishment. So if the company were now content to sit back and make money in a tight market, everyone would understand. But that's not Micron's style: rather than sit on its laurels, it is out looking for new worlds to conquer.

Boise-based Micron—the only U. S. maker and seller of dynamic random-access memories besides Texas Instruments Inc.—is preparing for the time when the current DRAM shortage becomes a glut. That means new markets: in early 1989 the company plans to add first-in, first-out registers and cache memories; and just added to the portfolio are fast static RAMs. Earlier this year, Micron also diversified into the "value-added" memory area by adding memory modules and high-performance personal-computer memory cards. And it's going to sell burn-in ovens.

"We are diversifying into the value-added area to prepare for the time when memory chips are abundant," says Joe Parkinson, chief executive officer. "I expect the sales of memory cards and modules, which can absorb a good portion of memory-chip production, to sell well into market areas that [would be] mostly unaffected by the glut of chips."

**BOOST ON THE WAY.** In the meantime, the 1-Mbit DRAM, the forthcoming 4-Mbit DRAM, as well as the 256-Kbit and forthcoming 1-Mbit video RAMs are bolstering the company's dynamic memory sales, says Raj Rajaratnam, semiconductor analyst at Needham & Co., a New York investment firm. And, he adds, "The static RAM area, in which Micron really hasn't received much recognition yet, will be a

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major growth market for them. The company already has some of the fastest 16-, 64-, and 256-Kbit static RAMs and is developing a 1 Mbit static memory."

There is also a specialty area in which Micron has gained a significant amount of expertise: the equipment for burn-in testing of chips. Micron hopes to turn this niche into a profit sector.

Later this fall, the company will start selling a family of ovens—the AMBYX series—that perform burn-in and functional testing. It developed the ovens and test electronics for its own use. These enable its test engineers to track complete lots, pinning down failures and production problems before the chips reach the customer. Although Parkinson says he doesn't expect to take the market by storm, he adds that the ovens, which range in price from less than \$100,000 for the smallest to close to \$1 million for the largest, offer more capability than those on the market.

**TOUGH SKIN.** The plans are ambitious, but the bumpy road that Micron has traveled to get to this point has toughened it. Started a decade ago as a semiconductor design consulting firm, Micron entered the commercial market in 1982 with a 64-Kbit DRAM and has since added 256-Kbit and 1-Mbit memories. Since entering the market, it has weathered the Japanese in-

vasion as well as the price-cutting and glut conditions of the mid-1980s that caused its red-ink years. Now Parkinson sees 1988 as a watershed year when the company becomes firmly established as a significant memory chip supplier and positions itself for the future.

And the company is growing. Now one of the top five employers in Boise, Micron has about 2,500 workers and has several

### The company is adding several fast static RAMs to its portfolio

new buildings going up that will more than double its floor space and manufacturing capacity. Just next door to its current facility the company is putting up a 250,000 ft<sup>2</sup> manufacturing facility that should be ready in mid-1989. It will produce chips on 6-in. wafers and can easily be upgraded to 8-in. wafers when the economics of production justify the switch. An office structure and a test facility are also under construction.

The keys to Micron's success—the things that have turned its balance sheet around—are its stick-to-it, don't-give-up efforts to produce memories very cost ef-

fectively, and its victory in its antidumping law suit against the Japanese vendors. In that case, Micron proved to the U. S. International Trade Commission's satisfaction that Japanese makers were dumping memory chips—that is, selling them at less than manufacturing cost to gain market share. As the Japanese sold those low-priced memories in late 1983 through 1985 U. S. companies gradually withdrew from the market, leaving Micron and TI as the last two U. S.-based manufacturers, except for IBM's internal operation.

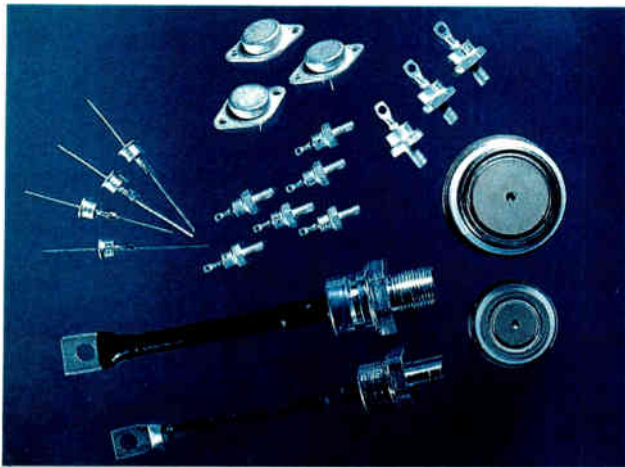
One consequence of Micron's efforts was the U. S.-Japan semiconductor trade agreement, signed in August 1986. It forces Japanese and other memory manufacturers to charge "minimum" prices calculated by the U. S. government as the fair market value. Those prices, combined with the increasing value of the yen, no longer gave the Japanese suppliers a significant price edge.

While that was happening, many new large systems and personal computers that demand huge amounts of memory went into production. So demand for chips has escalated, resulting in prices for DRAM chips well over those set by the government.

The result has been good news for Micron. The combination of high demand

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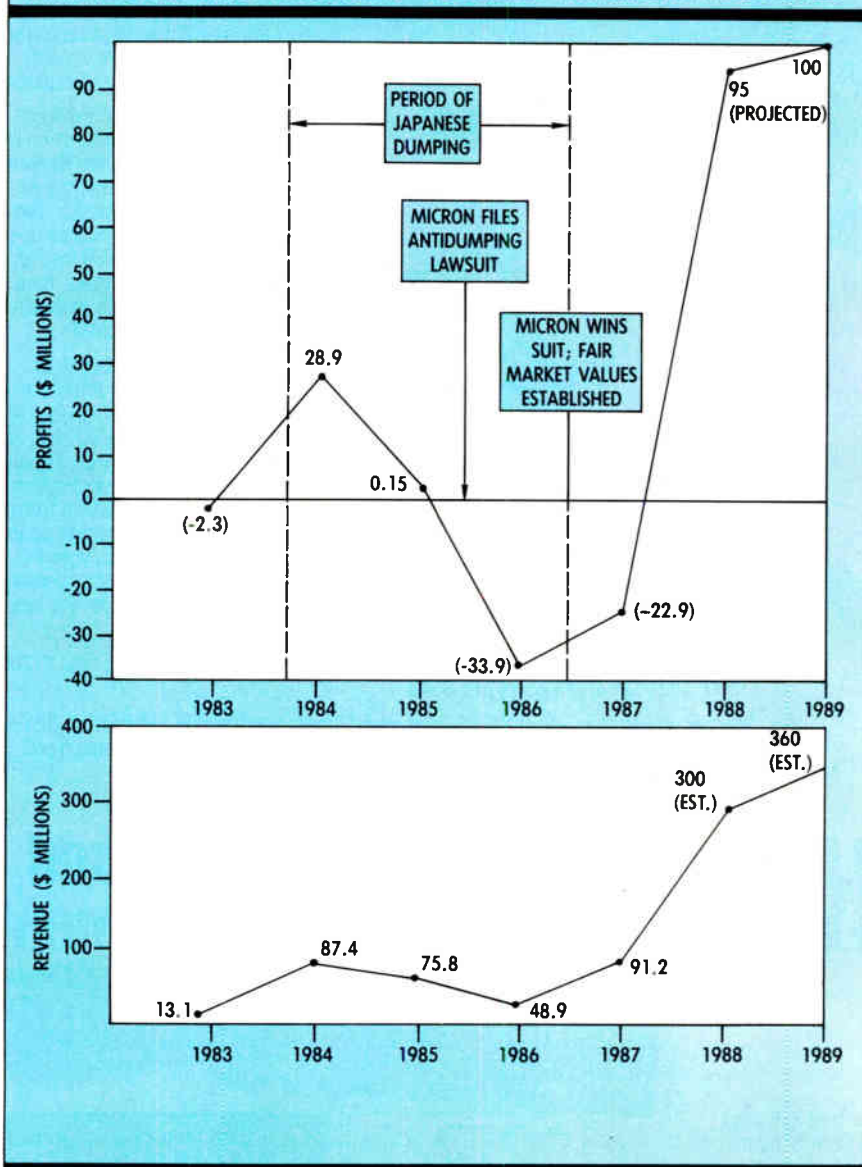
and more competitive pricing has washed away the red ink. In the company's third quarter of 1988 (ending June 2), it registered a net profit of just over \$29.2 million, while for the same quarter in 1987 the company lost a little more than \$3.7 million. And the fourth quarter results are expected to be even stronger. Estimates by Needham's Rajaratnam peg Micron's net income at about \$37 million based on sales of \$110 million for the quarter ending Sept. 1.

"The near term for Micron looks excellent," agrees Mike Gumpert, an analyst for the New York investment house of Drexel Burnham Lambert. That's because about 90% of Micron's sales are accounted for by DRAMs, estimates Gumpert. Volume prices are in the \$10 to \$12 range for 256-Kbit parts, he adds, and are expected to hold steady or increase slightly.

Although Parkinson says he is disheartened by the withdrawal of all but one of the U.S. manufacturers from the DRAM market, that withdrawal has helped his company. Not only has it eliminated competition, but it allowed Micron to hire some of the best memory design talent from around the country. Already, a research center in Austin, has been set up so designers who prefer to live and work in Texas can. And, that will make it easier for employees to visit Sematech, the Austin-based semiconductor production consortium of which Micron is an member.

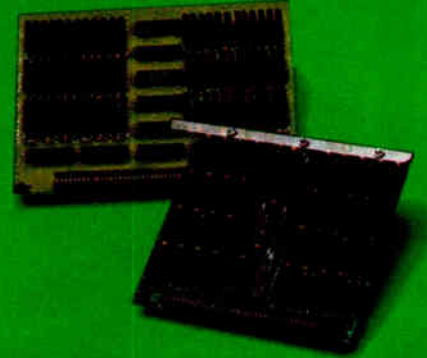
"That talent has greatly aided Micron in designing not only some of the smallest memory chips in the industry, but some of the simplest manufacturing processes to build them with as well," says Parkinson. "For example, our 1-Mbit dy-

## ANTIDUMPING VICTORY TURNED MICRON AROUND



Micron's victory in its legal action against Japanese semiconductor makers, which were found by the U.S. to be guilty of dumping, reversed its fortunes.

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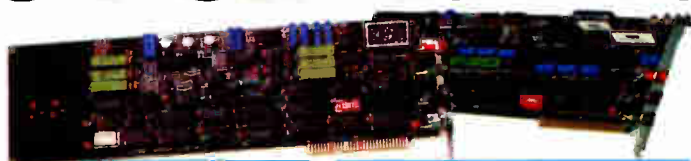
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dynamic RAM, which has a chip area of 88,000 mils<sup>2</sup> has just been shrunk by over 37% to just 55,000 mils<sup>2</sup>, or about 30% smaller than the closest competitor's." And, the chip requires just 10 mask steps in production versus 15 for all the other Mbit memories. That means extremely high wafer yields. High yields, in turn, mean reduced manufacturing costs, more chips per wafer, fast, reliable chips, and, most important, higher profit margins.

One way that Micron has leveraged its memory sales is by hammering out several noncancellable multiyear contracts with its major memory customers. The agreements commit the customers to go to Micron for about 20% of their total memory requirements, an arrangement that Needham analyst Rajaratnam expects will enable the company to weather some of the anticipated memory oversupply conditions. —*Dave Bursky*

## THE TIMING WAS JUST RIGHT FOR TAIWAN SILICON FOUNDRY

### SAN JOSE, CALIF.

It started as an experiment: a chip company that would not design or market semiconductors—just manufacture them for others.

Less than two years later, the experiment is a rousing success. Taiwan Semiconductor Manufacturing Co. is cranking out 6,000 6-in. wafers a month—triple the rate of last January—and production is expected to reach a capacity of 11,000 wafers a month by year-end. And customers are clamoring for more. "We're booked through 1989," says Steve Pletcher, vice president for marketing and the head of TSMC's office in San Jose, Calif. "Our timing couldn't have been better."

Taiwan had just three IC houses two years ago, now there are 40

That's an understatement. When TSMC was formed just over 18 months ago, the worldwide semiconductor industry was still suffering through a two-year-old depression. The last thing most companies were interested in was investing in chip plants. But when the industry revived in 1987, TSMC proved the beneficiary of a worldwide capacity shortfall. Credit the Taiwanese government, which owns 48.3% of TSMC, and Philips of the Netherlands, which owns 27.5%, with the foresight to make the necessary investments. Philips wanted an off-shore plant it could depend on; Taiwan wanted to provide its fledgling electronics industry with a world-class fab.

**BIG MOVE.** Along with a handful of Taiwanese companies, which together own the remaining 25% of TSMC, they set up a fab and recruited Morris Chang, former general manager of General Instrument Inc. and vice president of Texas Instruments Inc., to be their chairman and chief executive officer. Chang, in turn, brought in James Dykes, late of General Electric Co.'s Semiconductor Business, as president and chief operating officer.

Before TSMC, there were only three integrated-circuit design houses in all of Taiwan. Now there are well over 40, Chang says, explaining that a design firm

can be set up with only about \$3 million to \$4 million in capital, or about \$100 million less than it would cost to set up a full-fledged chip company with its own fab. The Taiwanese government, he says, was primarily interested in creating a manufacturing facility for these design houses—profit was secondary.

But profits don't hurt, and now they're seeing them anyway. "We are profitable—we turned our first profit in June, and September should put us in the black for the year," says Pletcher. Revenue for

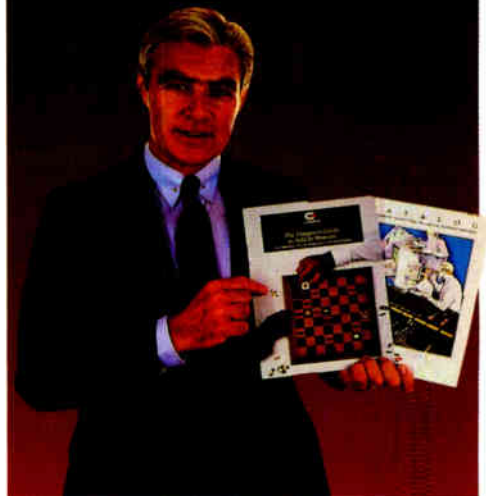
1988 will be in excess of \$30 million. And as TSMC switches more of its lines over from its original 2- $\mu$ m CMOS process to 1.5- $\mu$ m CMOS, Pletcher says, yield and profits are rising.

By early 1989, TSMC will be producing the majority of its product in 1.5- $\mu$ m, he says, and profits will be even higher.

Not everything has gone TSMC's way, though. Dykes had to leave this year for personal reasons, and the company is almost a year behind its original production plan of 10,000 wafers a month by December 1987. Lastly, the three- to six-month turn-around time that Dykes and Chang originally anticipated for validating a given chip design, has turned out to be closer to six months to a year.

But TSMC is not discouraged. Dykes was replaced this summer by Klaus Wiener, who like Chang, is a TI veteran. The company is also expanding. Construction began in April on TSMC's second fab, a \$250 million facility that will ultimately be able to produce 30,000 wafers a month. The first half of that plant will begin production late in 1989, and will be capable of producing 15,000 6-in. wafers a month. If further capacity is needed, Pletcher says, TSMC will proceed with phase 2 in 1990 or '91, which will be either an identical 6-in. wafer fab or have a more advanced 8-in. facility. By then, if all goes well, TSMC executives are predicting they will be cruising along with annual sales approaching \$200 million a year. —*Tobias Naegele*

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# PEOPLE TO WATCH

## CAN INTEL'S FINE BRING SUCCESS TO ITS ASIC BUSINESS?

His first job will be to integrate ASIC business into the Microcomputer Division

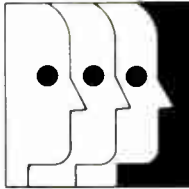
### CHANDLER, ARIZ.

Since application-specific integrated circuits are a relatively recent industry development, not many executives have been around the track with them already. But Kenneth B. Fine, the new general manager of Intel Corp.'s Chandler Microcomputer Division, is someone who sports a resume that looks tailor-made for his job—melding ASICs into the division's operations.

Fine planned and produced the successful 80186 and 80286 chips in an earlier stint at Intel that ended in 1985. During his tenure as the general manager of Intel's vital Microcomputer Division, the unit's market share tripled. From the time he left Intel until returning last February, Fine spent two years in the midst of the all-important computer-aided-design field as the president of Valid Logic Systems Inc., the San Jose, Calif., CAD work-station company.

Now, the energetic Fine will need all that experience because corporate management put the pressure on in a June shakeup by adding Intel's ASIC operations, which had been a separate unit, to his division's charter. His job will be a crucial one for the company: to make a success of a business that up to now has been disappointing to Intel. As a remedy, management has decided to centralize ASIC work at Chandler and move the related CAD tools and processes to operating divisions that could better use them to develop standard products. At the Microcomputer Division, the aim will be to expand the library of a critical asset, integrated circuit cells.

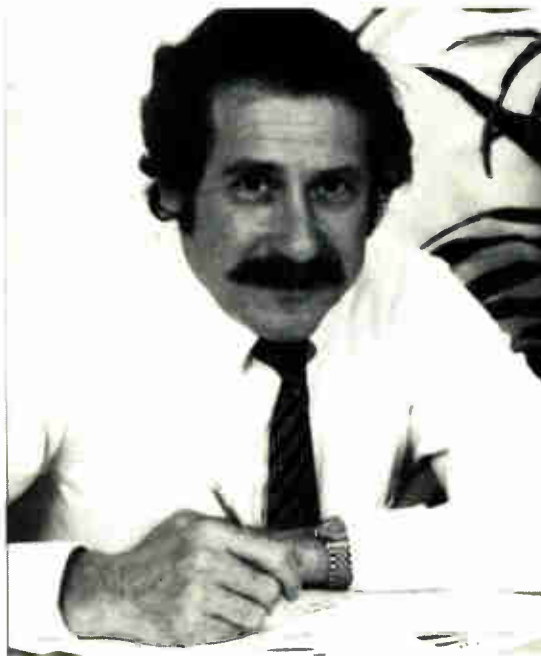
Fine, who reports to senior vice president David L. House, recognizes that corporate management has set an important strategic goal for the division and it must deliver. "It is important to try to diversify from the microprocessor business," says Fine. The need for Intel to diversify is an ironic fallout from the company's runaway success as the preeminent microprocessor supplier worldwide, because in the eyes of many this strength has made the



firm essentially a one-product company. The financial community views that as a potential weakness.

That's where Fine comes in. From the way he was welcomed back to Intel, it is evident he burned no bridges be-

hind him when he left for supposedly greener pastures. In fact, top Intel officials recognize their people are in demand elsewhere, and Fine "wanted to experience the full responsibility of management" at the Valid Logic post, as one executive puts it. "But he is back home, in semiconductors, where he belongs."



Fine's job at Intel will be to integrate the company's disappointing ASIC unit into the Microcomputer Division.

Fine agrees that the mystique of the chip business began to attract him even in his days at Digital Equipment Corp. in the mid-1970s where, as manager of advanced development, his operation was the first user of Intel's 8048 controller. He also was on a fast career track at DEC in those days, but the lure of semiconductors was proving to be too strong for him to resist, "even though it was a Richter 10

decision," he recalls.

By his own account, the DEC experience still strongly influences Fine's views, particularly in understanding things from the user side, a quality some critics say is generally lacking at Intel. "He easily puts himself in the customer's shoes," a strength that is considered central to ASIC success, says the executive who knows him well.

**CATCHING ON.** He'll need that strength, because Intel has found non-microprocessor growth difficult to come by, and the microcomputer unit—formed to specialize in embedded controllers—is deemed to offer the best springboard to growth.

During this decade, these controllers have caught on in a big way. They are often the logic elements buried in a growing list of industrial equipment, such as motor controls and tools. The best-selling part is the 8-bit 8051; others are the 16-bit 8096 and the 32-bit reduced-instruction-set 80960.

But most customers for controllers "take the standard architectures and customize them with on-chip wrinkles of their own," Fine says. The objective is the ability to reprogram for different tasks, which can be accomplished by having large input/output blocks that lend flexibility. The whole process that has evolved in Chandler "spotlights our ability to proliferate our architectures," which is a big advantage for Intel, says Fine. To help streamline the process, a wide choice of ASIC options, pulled from a standard-cell library, are necessary.

The work of building a good library has lagged badly, though. That's why Fine, 46, was lured back to the company to manage the development of standard cells.

Fine says there are several reasons the program ran behind, prime among them an internal attitude that was ambivalent about its support for the development. Because controllers are in competition with standard parts, "they succeed at the expense of standard products," he says. Another reason was that it took three years or so to learn—especially at the cor-

porate level—that ASICs involved a lot more emphasis on CAD tools and processes and they can't be treated as a stand-alone business.

Another challenge for Fine is getting results from the joint-development agreement with Dallas-based Texas Instruments Inc. to build cells for the library. Fine says he believes that people expect-

ed too much too soon from the companies, which are as far apart in business culture and product thrust as they are geographically.

"We were going at it from such different points of view, TI from the TTL vantage point, and Intel from microprocessors," he says. But the rough spots have been worked out and the first results of

the alliance are in sight, adds Fine.

As for how the fortunes of the newest Intel division can be expected to unfold, Fine has the characteristic optimism of a fast-track chip executive who is accustomed to doing well. "This [microcontroller-ASIC] is a good business that ought to succeed. There is no reason that it shouldn't." —Larry Waller

## THE NEW AEA CHAIRMAN CALLS FOR HARMONY

### SANTA CLARA, CALIF.

The new chairman of the American Electronics Association has just one goal: Save the U. S. electronics industry. "Everything I do will be to improve competitiveness," says L. William "Bill" Krause, who is also chairman and chief executive officer of 3Com Corp. "We are launching an economic renaissance for the industry."

Cynics might brush off those remarks as exactly what an AEA chairman would be expected to say. But Krause's track record makes him worth taking seriously. This is a man who rose from being Hewlett-Packard Co.'s first computer salesman in 1967 to become a division manager who helped guide the Palo Alto, Calif., company into such key markets as personal computers and application software. And since moving to 3Com in 1981, he has engineered a thousand-fold increase in sales.

Now, he wants to share his expertise. Times have changed, and the industry has to change with them if it hopes to beat overseas competition and grasp new opportunities, Krause warns.

"The key element is to provide an en-



Krause will play peace-maker between rival industry factions as AEA's new chairman.

vironment that encourages growth and innovation," he says. "At the core of that is the cost of capital. The Japanese cost of capital—taxes, interest rates, and whatever other costs are associated with bor-

**'We're realizing each part of the electronics industry is dependent on the other'**

rowing money—is one-sixth of ours. That means that where we can afford to take a year to get a payback on investment, the Japanese can wait six years." To get the U. S. on track, what's required is cutting

the cost of capital through programs that encourage reduced consumption and increased investment and savings, says Krause, 46.

Reviving the industry will begin by identifying "the long-term programs to improve competitiveness which we can rally our members and government around," he says. In Krause's view, there are opportunities beckoning in high-definition television and dynamic random-access memories, where he says measures must be taken to increase production in the U. S.

The industry must also make a transition, Krause says, from a group of self-centered sub-industries—semiconductors, components, subsystems makers,

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and systems integrators—and learn that each industry segment needs the other. “In the early days of electronics, the primary interest was growth and independent action in each part of the industry,” he says. “But times have changed. Growth is still important, but we’re moving toward an understanding that each part of the electronics industry is dependent on the other—a sort of electronics food chain, if you will. What we’ve recognized is that united we stand and divided we fall.”

That’s forced a change in the role of chairman at the AEA. “The chairman’s job used to be inward-looking, managing

the operations of the association,” he says. “Now it’s more of an external public relations job—facilitating harmonious relations between sectors of the industry.”

Krause sees his mission at AEA as the beginning of the concluding phase of a three-phase career he mapped out while still a cadet at The Citadel: the phases were learning, building and sharing.

The learning part began at The Citadel, where he earned a BSEE in 1963, and enjoyed a basketball career that was highlighted by “holding Jerry West to 41 points during his senior year at West Virginia.” After serving two years in the

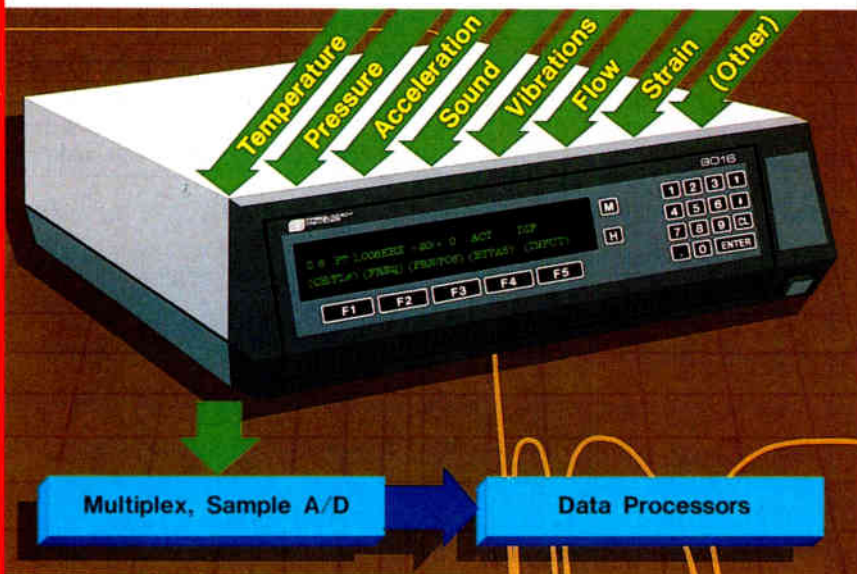
Army Air Defense Corps, he bounced around a bit before joining HP in 1967. Krause finished his 14-year stint there—and the first phase of his career—as general manager of the General Systems Division.

Building was the objective for Phase 2, and he’s succeeded beyond all expectations since joining 3Com in Santa Clara, Calif., seven years ago. He took over a small networking consulting firm billing about \$250,000 annually and turned it into a major force in computer networking. Sales reached \$252 million in fiscal 1988, which ended May 30.

So now Krause wants to begin serving. Not that he’s quitting 3Com, though. “I’ve still got seven or eight years in my current phase,” he says—but he’s ready to begin laying the groundwork for a career in public service. Krause admits he won’t be able to cause any drastic changes in the U. S. industry in his one year as AEA chairman. But he says he can get the ball rolling for his successor. “What you can do in a year is to provide a focus,” he says. “We’re just damn sick and tired of being considered a second-rate electronics nation—we are not second-rate at all.”

—Tobias Naegele

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## CAN BECKER SELL HIS PRIVATE EYE TO THE PUBLIC?

### CAMBRIDGE, MASS.

It’s a good thing Allen Becker has considerable experience with venture capitalists. The company he founded last year has no track record, a proprietary technology that he won’t discuss, and a secret list of customers.

Becker is president of Reflection Technology in Cambridge and developer of the Private Eye, a miniature 2-oz device. It displays an image roughly equivalent in resolution to that of a 12-in. monitor in a device measuring 1.2 in. high by 1.1 in. deep by 3.2 in. wide. The viewer gets the impression of looking at a screen that is “floating” in space.

The company will offer a standard model with a resolution of 720 by 280 pixels and a high-resolution 1,024-by-280-pixel version. The display can be handheld, mounted on a lightweight headset, or clipped onto eyeglasses and flipped down like a jeweler’s loupe. It could cost under \$100, depending on quantities.

Reflection Technology is not Becker’s first startup. He cofounded Cadmus Computer Systems Inc., and served as vice president for hardware engineering of the Lowell, Mass., company from 1983 to 1986. Cadmus was a vendor of computer-aided design and manufacturing work

stations that was disbanded after its technology, which simplified running Apple Macintosh applications, was sold to Apple Computer Inc., in Cupertino, Calif. Before that, Becker was also cofounder and vice president for hardware engineering at Kurzweil Computer Products Inc., an optical-character-recognition company in Cambridge, Mass., that was acquired by Xerox Corp. in 1980.

"You don't go through being founder of two companies without learning about venture capital," Becker says. "What I think I bring to the party at Reflection Technology is not just the knowledge of figuring out how to produce the technology. That's almost secondary. You also have to know how to sell, protect the technology [through patents], and manage the whole thing into success."

Despite Becker's public reticence to divulge technical details, some well-known backers are convinced that he's got a good chance to succeed. In the company's second round of financing, which was just completed, Becker says about \$3 million in venture capital was raised.

He's apparently convinced some reputable backers that he can bring that off. Seed-money investors in Reflection Technology include Jerome Wiesner, former president of Massachusetts Institute of Technology and science adviser to Presidents Kennedy and Johnson; Raymond Kurzweil, founder of Kurzweil Computer; and David Boucher, founder and president of Interleaf Corp., the Cambridge-based desktop publishing firm.

**WHERE THEY'RE GOING.** If not for his résumé and those backers, Becker would likely be among the legion of unrequited entrepreneurs seeking backing for their can't-miss schemes. Now, Becker guesses that judging from initial reaction by prospective customers, the number of Private Eyes on the market in customer products by 1990 could number in six figures. "In all candor, we don't know how many to expect we'll ship," he says. "That will be a function of how fast we and our licensees can ramp up. We know of consumer applications that would reach the low seven figures per year." That's millions of displays for, among other things, high-performance calculators, pocket computers, telephone handsets, radio pagers, and hand-held instruments. Military applications, such as in aircraft where size and weight are key considerations, offer further promise.

Industry analysts are also optimistic. There is "interesting and significant potential" for the device and the company, "provided they get past the startup phase," says Russell Craig, director in management counseling at Arthur D. Little Inc., the Cambridge, Mass., research and consulting firm.

Craig says Private Eye could make portable personal computers more truly por-



**Becker—now on his third startup—**has high hopes for a new tiny display technology that gives viewers the impression they are looking at a 12-in. screen.

table. "because it would eliminate one of their major constraints—size of the screen and associated battery pack." He foresees "a whole series of untapped applications," including court usage by lawyers accessing an optical-disk-resident data-base and flight line maintenance use by personnel who would be relieved of carrying voluminous manuals.

Engineering prototypes exist and Re-

lection Technology will soon have "a limited supply of kits available within three months for customers who want to move forward with development," Becker says. He adds that "several companies" have already committed themselves to developing products that are based on the Private Eye or have licensed the technology for use in products under development.

—Lawrence Curran

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# MR. SMITH GOES TO SILICON VALLEY TO START OVER

## SAN JOSE, CALIF.

If this were a movie, it could be called *Mr. Smith goes to Silicon Valley*.

It is the chronicle of Tim Smith, once one of the rising young stars of Texas Instruments Inc., who suffered a fall from grace two years ago during a corporate reorganization. His 21-year career at TI took him from circuit designer to senior vice president in the Semiconductor Group, but when responsibility for memo-

ry chip technology was shifted to TI's Japanese subsidiary, Smith was placed for reassignment. Two months later he left TI, and now, after a difficult two-year stint in optoelectronics, Smith is back in the silicon world.

Smith is starting over at Fujitsu Microelectronics Inc. in San Jose, Calif., with a mandate to lead its fledgling Advanced Products Division into a sizable operation. "They want to make this thing into a

big business," he says of the unit, which though small, is the largest volume producer of Sparc RISC chips in the world. "I was brought in to grow it quite substantially, and I wouldn't be here if that wasn't the case."

But Smith couldn't be happier than to be in San Jose. He left TI to take over LaserCom, then a one-year-old Los Angeles optoelectronics startup, but ran into problems immediately. "At LaserCom, I had to make decisions on technology that was outside the field of my expertise," he recalls. "I couldn't rely on past experience."

**WHAT WENT WRONG.** Not all of those decisions panned out, and Smith takes full responsibility for LaserCom's troubles. "It wasn't a success. With the timeframe and resources that we had, we just had too many problems making the technology commercially viable," he says. But difficult as it was, the experience was worth it.

He learned how to make the most out of limited resources (by using consultants, for example), something that hadn't been a concern at robust TI. And he learned that no two businesses are exactly alike. "When you're going to do a startup, it's really important to do it in a field where you have some expertise."

In Smith, Fujitsu saw a capable chip executive who already had the experience of working with a multinational diversified electronics company. As the head of TI's memory operations, Smith had worked extensively with TI's plants in Japan and actually had oversight responsibility for its Singapore operation. But Smith didn't only have executive experience. Although there were whispers at TI that Smith was often too concerned with his own personal career goals, his resume reads like a history of TI in the semiconductor business.

Everything was going well. But when the reorganization left his career up in the air, Smith wasn't willing to wait what else TI might have in store for him. "I didn't stay around long enough to find out what my next job would have been," he recalls. But when he left, he promised TI he also wouldn't go into competition with the Dallas giant for two years. And having weathered the storm at LaserCom, Smith and Fujitsu have a message for TI and the rest of the industry: he's back.

-Tobias Naegele

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**THE IC CELEBRATES ITS 30TH BIRTHDAY**

Integrated circuit technology turned 30 in September, and Texas Instruments Inc.'s claim to fathering the industry has been duly memorialized by Texas. An historic marker honoring Jack St. Clair Kilby now stands in front of the corporate headquarters—about 400 yards from the lab in TI's semiconductor building where Kilby first demonstrated a working IC to executives on Sept. 12, 1958.

The Texas historical marker notwithstanding, the debate is continuing over whom to credit as the inventor. Kilby's competition amounts to Robert Noyce, a manager at Fairchild Camera and Instrument Corp. 30 years ago. Noyce, chief executive officer of Sematech in Austin, Texas, hasn't planned a similar commemoration of his role in inventing the technology that made ICs mass-producible.

**X/OPEN LAUNCHES A BRANDING PROGRAM**

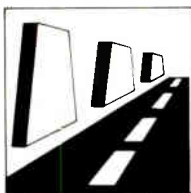
The goal of achieving a common applications environment for computer vendors reached a major plateau in September with the arrival of X/Open Co. Ltd.'s verification suite of software.

Testing will be conducted by the UniSoft Group at locations in Boston, Emeryville, Calif., London, and Tokyo. To receive the X/Open brand, computers must successfully complete the verification suite in a single run without modifications or errors. A trademark licensing agreement with San Francisco-based X/Open is also required to use the logo.

Among the first companies to field branded products is Unisys of Blue Bell, Pa., which says its U 5000 and 6000 computers have passed verification. Sun Microsystems Inc., Mountain View, Calif., and Hewlett-Packard Co., Palo Alto, Calif., are among companies that have announced their intention to brand their products with X/Open's logo. Sun expects to have products in the beginning of 1989, and HP says its work station line will earn an X/Open logo this year.

**NIPPON MINING LTD. TO ACQUIRE GOULD INC.**

Another U. S. high-tech company has been bought by a Japanese firm. Gould Inc. of Rolling Meadows, Ill., announced Aug. 30 that it has agreed to be acquired by Nippon Mining Co. Ltd., a Tokyo-based metals, petroleum refining, and petrochemical giant. The \$1.1 billion deal will reportedly be the fourth-largest acquisition of a U. S. company by a Japanese firm, and should provide Gould with a deep-pocketed parent to shore up its



sagging balance sheet. Nippon Mining's sales were \$6.5 billion in fiscal 1988. Gould lost \$96 million last year on sales of \$933 million.

Nippon Mining says that the acquisition will enhance its plans for global expansion in markets where Gould holds a position, including electro-deposited copper foil that is used in printed-circuit boards, fuses, and fiber-optic and optoelectronic components. Gould's superminicomputer business will likely prove less complementary, and may ultimately be sold, some industry watchers speculate.

**CDC SPINS OFF ITS DISK-DRIVE BUSINESS**

In what could be a first step toward exiting the disk-drive business, Control Data Corp., Minneapolis, last month converted its former Data Storage Products Group into a separate, wholly owned subsidiary called Imprimis Technology Corp.

By setting up Imprimis as a stand-alone unit, with a separate set of books,

Control Data may be preparing to sell the business. Company executives don't rule out that possibility, but say the move will allow it to explore alternatives, including joint ventures and partnerships.

The operation had sales of about \$975 million last year, more than a fourth of Control Data's revenue, and recently returned to profitability following disastrous losses in 1985. Imprimis is the industry's largest supplier of high-performance, high-capacity magnetic disk drives to original-equipment makers.

**HP HITS 1 MILLION DISPLAY TERMINALS**

Hewlett-Packard Co. shipped its one millionth display terminal in September—14 years after its first terminal rolled off the assembly line.

When the Palo Alto, Calif., company started making terminals in 1974, they cost \$3,000 apiece. Manufacturing efficiency and design have helped sink the price on the lowest-end model to \$375.

About 95% fewer parts and 92% less time goes into building terminals today than in 1974, says HP. The owner of the millionth: 3M Co., St. Paul, Minn.

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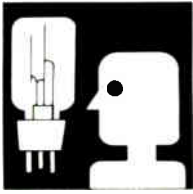
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## LOOKING BACK



The year was 1938. The U. S. was still struggling to emerge from the Great Depression, Franklin D. Roosevelt was in the middle of his second

term in the White House—and at 320 West 42nd Street in New York the editors of *Electronics* were excited about the TV set managing editor Donald G. Fink had built and used to receive the first outdoor TV broadcast.

The October issue of *Electronics*, an eight-year-old magazine that described itself as being about “radio, communication, industrial applications of electron tubes . . . engineering and manufacture,” didn’t make the kind of fuss about TV that hindsight tells us the infant technology deserved. There are just two pictures related to the new technology contained in the issue, one showing the NBC broadcasters before a camera on the RCA building, the other a remarkably clear shot taken off the TV receiver’s screen. One of the articles in the issue is the fourth installment in a series by Fink describing in great detail how the staff built the circuitry needed for the TV set.

In the new books section, a reviewer lauded J.C. Wilson’s 492-page *Television Engineering* as “a solid book, carefully written, well illustrated, and except for the high price at which it must unfortunately be sold, it has all the qualifications requisite to a place on the radio engineer’s shelf.” The book cost \$10.

The rest of the issue carries out the magazine’s mission by covering subjects ranging from a discussion about whether research should be stopped (“None of our readers believe it should”) to a program for the upcoming fall meeting in Rochester, N. Y., of the I.R.E.R.M.A. The group was a combination of the Institute of Radio Engineers, one of the predecessors of the Institute of Electrical and Electronics Engineers, and the RMA, the Radio Manufacturers Association. One of the meeting’s scheduled events: a “Tenth Anniversary Dinner (Stag).”

In radio, the reader could learn in the article “Laminated plastics for radio,” that “laminated plastics have had considerable growth in the radio industry because of light weight, easy machining, high resistivity, and freedom from moisture absorption.” In “A shielded loop for noise reduction in broadcast reception,” the writer declares, “Today the most serious technical problem in radio, so far as the user in large cities is concerned, is noise.”

It seems that noise was even a problem in the movies. An article written by a transmission engineer at Metro-Goldwyn-Mayer Pictures describes a new way of

reducing ground noise on sound tracks, a technique he calls “squeeze or matted track.”

In the issue’s ads, Ampere Electronic Products Inc., Brooklyn, extolled its water-cooled transmitting and rectifying tubes, and Collins Radio Co. of Cedar Rapids, Iowa, pitched the new Collins 26C limiting amplifier. Also, Weston Electrical Instruments Corp., Newark, N. J., offered multir-

ange test instruments. And in a full-page ad that conjured up images of football and fall, Western Electric’s Graybar unit claimed its “22-type portable speech input” scored on every play. —Howard Wolff

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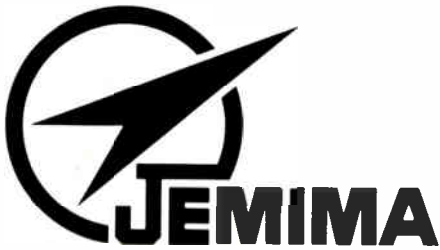
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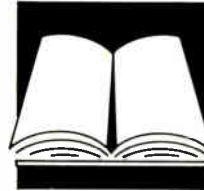
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### BOOK REVIEW

## IBM'S PC STORY: AN ELEPHANT DANCES

### BLUE MAGIC

by James Chposky and Ted Leonsis  
New York: Facts On File, \$19.95



Take a look at your desktop computer. The fact that you have one is probably the result of a crash IBM project code-named Acorn that in 1980 developed and delivered the first IBM Personal Computer to market in just a year. As told by James Chposky and Ted Leonsis in "Blue Magic," the story of how the people in blue suits at International Business Machines Corp. rewrote their corporate canon to get the job done is a fascinating study of skill, talent, luck, and timing.

Therein lies a lesson for today's manager: no matter how large the company, it must be able to react quickly. In IBM's case, it had lost considerable total market share—from 60% at the start of the 1970s to 40%—largely because of 13 years spent under the stultifying cloud of an antitrust suit that was finally dropped by the Justice Department. So it created independent business units to bring new concepts to market quickly. Maybe, as chairman Frank Cary put it, they could even "teach an elephant how to tap dance."

They taught quite a dance. Though the IBM PC was not the first desktop computer, its enormous success has shaped and defined the market.

But eight years ago, only a few visionaries thought that could happen. Apple "had fumbled its advantage as the first company to introduce a product successfully with potentially broad uses," according to Chposky and Leonsis. So a 13-year IBM veteran named William C. Lowe, who had been promoted in 1978 from manager of the Entry Level Systems unit at Boca Raton, Fla., to overall lab director there, was trying to convince IBM's overlords to give him a year to turn out a personal computer.

Then came one of those instances of brilliant judgment—or maybe just good luck—that dot the history of such enterprises. Lowe, whose contacts at IBM headquarters in Armonk, N. Y., told him he was about to be promoted to vice president of the Information Systems Division, was casting about for a new manager for the PC project. He settled on Mark Estridge.

It was an inspired choice. Estridge is described by the authors as a man who could "get his way without creating enemies." His secret, it turns out, was humility.

Estridge put together a team of 13 engineers and marketing men that was quickly dubbed the Dirty Dozen. They made another well timed, and very un-IBM-like, decision to use off-the-shelf parts; there was no way the machine could have been turned out in a year otherwise.

Particularly illuminating is the description of the negotiating and selection process used by Estridge and his associates to pick William Gates and his fledgling Microsoft Corp. to develop the software for the PC. And the descriptions of how Sears Roebuck and Computerland were named the official retailers afford a look behind the facade of the marketing process.

With its workmanlike prose making it an easy read, "Blue Magic" delivers what its subtitle promises—the story of "the people, power and politics behind the IBM Personal Computer." Although IBM refused to cooperate with the authors, many of the Dirty Dozen who have left the company did. Their testimony went right into the book notes, which Chposky and Leonsis kept on an early model of the original PC.

—Howard Wolff

## MEETINGS

**M**anagers looking for a road map through the era of distributed information and telecommunications technologies might well find it at the Open Systems



Interconnection Conference for Decisionmakers and Implementors Oct. 31-Nov. 2.

To be held at the Peabody Hotel, Orlando, Fla., the conference will focus on strategies for building, integrating and migrating information-network applications using the OSI standards.

Charlie Bass, Chairman of Touch Communications, Scotts Valley, Calif., will deliver the keynote address, "The Creation of a Worldwide Multivendor Marketplace."

The conference has two tracks. One targets management strategies for executives and planners, while the other focuses on system development for engineers, programmers and technical managers. For more information, contact Omnicom Inc., 115 Park St., S. E., Vienna, Va., 22180. Phone (800) 666-4266.

**T**he North American Telecommunications Association's Unicom 2 Exposition and Conference also targets executive and managerial concern on distributed information and connectivity.

About 80 experts will address many concerns of manufacturers and users. There will be over 800 booths and an Integrated Services Digital Network demonstration. The conference will be held Nov. 29-Dec. 1 in Dallas. For details, contact NATA, 2000 M St., N. W., Washington, D. C. (800) LET-NATA

**A**lso on *Electronics'* calendar of key conventions, shows and expositions:

**Symposium on Defense Requirements: A 10-Year Forecast of Defense Needs**, Oct. 11-13, San Francisco Airport Marriott, Burlingame, Calif. Contact John Geron, Electronics Indus. Assoc., 1722 Eye St., N. W. Ste. 300. Washington, D. C. 20006. (202) 457-4944.

**International Congress on Transportation Electronics**, Oct. 17-18 at the Hyatt Regency Hotel Dearborn, Mich. Contact Louis Nagy, Electrical and Elec-

tronics Engineering Dept., General Motors Research Laboratories, GM Technical Center, Warren, Mich. 48090; (313) 986-1636.

**Federal Computer Conference and Defense and Government Computer-Graphics Conference**, Oct. 26-28. This joint conference is being held in the Washington Convention Center, Washington, D. C. Contact National Council for Education and Information Strategies, 15200 Shady Grove Road #350, Rockville, Md. 20850; (301) 670-2818.

**Seventh International Congress on Applications of Lasers & Electro-Optics (ICALEO '88)**, Oct. 30-Nov. 4. Santa Clara Convention Center, Santa Clara, Calif. Contact Larry Lottridge, OPTCON '88, 1816 Jefferson Pl., N. W., Washington, D.C. 20036; (202) 223-8130.

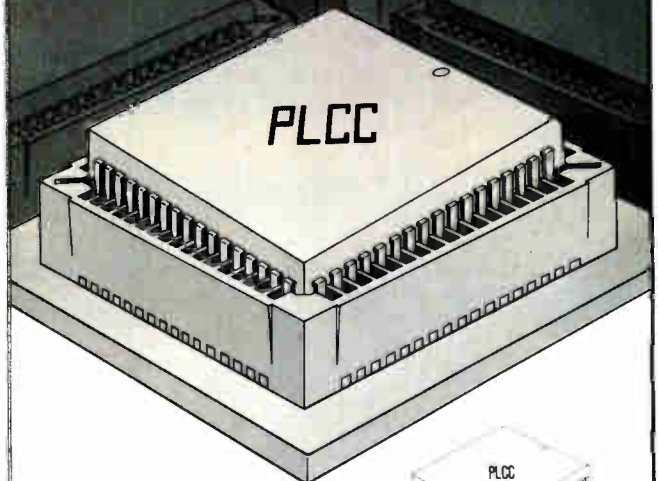
**Scan-Tech 88, International Trade Show for Automatic Identification Technologies**, Oct. 31-Nov. 3 at McCormick Place North, Chicago, Ill. Contact AIM Inc., 1326 Freeport Road, Pittsburgh, Pa., 15238; (412) 963-8588.

**Autofact**, Oct. 31-Nov. 2 at McCormick Place East, Chicago, Ill. Contact Jill Vanderlin, Society of Manufacturing Engineers, 1 SME Dr., P. O. Box 930, Dearborn, Mich. 48121; (313) 271-0023.

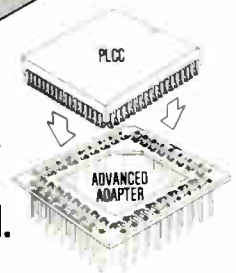
**The Unix Operation System Exposition and Conference**, Oct. 31-Nov. 2 at the Javits Center, New York, N. Y. Contact National Expositions Inc., 15 W. 39th St., New York, N. Y. 10018; (212) 391-9111.

**1988 GaAs REL Workshop**, Nov. 6 at the Opryland Hotel, Nashville, Tenn. Contact William Roesch, TriQuint Semiconductor; (503) 644-3535, extension 4143.

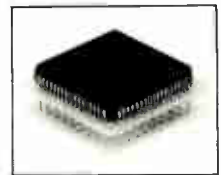
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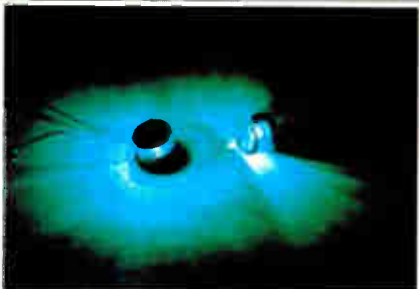
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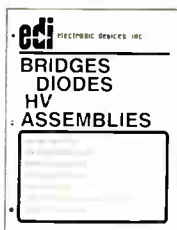
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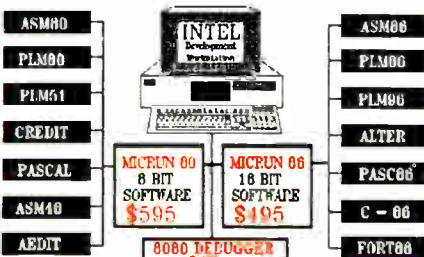
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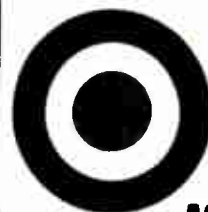
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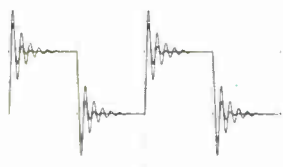
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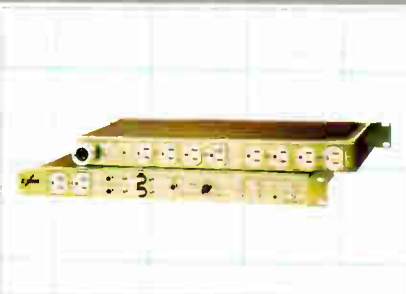
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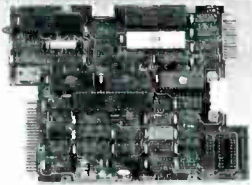
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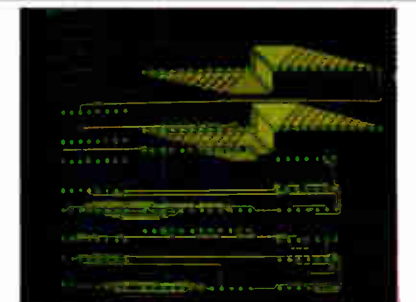
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# UPDATE: LSI LOGIC AND MOTO KEEP PUSHING GIANT ARRAYS

**N**ow that the dust is settling after a frantic year in which a few gate array suppliers pushed densities past the 100,000-gate level, competitors and critics are still wondering just how useful these giant gate arrays are. But that's not an issue for LSI Logic Corp., which is holding tight to its market-leading position: the Milpitas, Calif., company says it's having no problems winning designs.

LSI raised the stakes in the gate array game last year with its CMOS LCA100K Compacted Array Plus family, which boasted more than 100,000 usable gates [*Electronics*, Oct. 29, 1987, p. 55]. Two weeks later, Motorola Inc. countered with its HDC family of high-density CMOS arrays, which offered up to 100,000 gates and 80% utilization. And while competing suppliers predictably introduced their own large CMOS arrays in the ensuing months, LSI and Motorola have both withstood the onslaught.

Clustered at the 50,000-and-up usable gate level, the rest of the array pack is running just about even, says Gerald S. Rau, product marketing manager for gate arrays at LSI. "Motorola maybe is a half-step ahead of the others" with its triple-level metal CMOS process and 80% gate utilization [*Electronics*, Nov. 12, 1987, p. 99].

The rest of the field includes SGS-Thomson Components of Carrollton, Texas, which introduced its ISB 12000 series in November, 1987; VLSI Technology Inc., which delivered its VGT200 series this March, and a trio of Japanese heavyweights: Toshiba, Fujitsu, and NEC. SGS-Thomson's 1.2- $\mu$ m CMOS array offers 51,200 usable gates out of a total of 128,000, and while currently limited to double-level metallization, the company has already seen first silicon on a triple-level metal version. VLSI's family comes in sizes up to 65,000 usable gates, uses a 1.5- $\mu$ m process, and is claimed to be 10% denser than other dual-metal arrays.

But with so many companies hitting the market with super-dense arrays, it remains unclear how many real-life customers are waiting in the wings to use them. Rau says that with nearly 50 design wins already, LSI Logic's LCA100K has clearly proven that "there really is a set of customers that will take whatever you give them if it can increase functionality." But others have their doubts.

Skeptical consultants and sour-grapes suppliers, who haven't developed a high-density capability yet, keep saying the whopping arrays are little more than a curiosity.

"They won't be too important very soon," says William J. McClean, vice president and chief number-toter at Integrated Circuit Engineering Corp. Scottsdale, Ariz. "They're too much to handle for most customers."

The premium prices the giant arrays command are steering most users to more economical smaller arrays or cell-based designs, adds Donald Skilken, VLSI Technology's ASIC Division product marketing manager. Their experience is that standard gate arrays average 6,000 to 8,000 gates, and the cell-based arrays average 20,000.

But that hasn't deterred Motorola, which does not have a wealth of experience in making and marketing CMOS arrays of any kind. Motorola's entry was a bold attempt to leapfrog established competitors with a technology that some said was too advanced to succeed—a family of 1- $\mu$ m triple-level metal arrays in which 80% of the gates could be used in a typical implementation. That's up from about 50% for most chips of comparable size.

The idea was that better gate utilization would give it a price advantage, says John Carey, Motorola's product marketing manager for the HDC series. More efficient use of silicon real estate would be gained by the ability to program gates with all three metal layers, and by flexible power-bus routing.

While competitors admired the plan, not many thought Motorola could pull it off successfully. "What we heard was 'it sounds good, but let's see them make it,'" Carey says. But Motorola did build the arrays—and has had a number of design wins, including one chip that will be featured in an advanced laser printer built by Personal Computer Products Inc. of San Diego, Calif. And Andor International—Eugene Amdahl's latest computer startup that will make mainframe computers compatible with IBM Corp. machines—has chosen Motorola's HDC as its custom central-processing architecture.

Carey also points out that the 64K HDC array won over a competitor's 129K product in a test by a major company. Since the announcement last year [*Electronics*, Nov. 12, 1987, p. 99], the family has been expanded to five densities from the original three, from 8K to 115K. Macros have been added as well to bring the cell library total to 115. Motorola is building the parts at its new Mesa, Ariz., fab line, which handles 6-in. wafers, and was designed for sub-micron geometries with a Class 10 cleanroom. "We're finding that this is more important to some of our customers than [the fancy] software tool claims of others," Carey says.

—Larry Waller

**PROBING THE NEWS**

**LSI LOGIC'S GIANT ARRAY BREAKS THE RECORD FOR USABLE GATES**

**ITS 100,000-GATE CHIP IS FIRST OF A NEW GENERATION COMING**

By J. Robert Cramer

**LSI LOGIC'S** new 100,000-gate CMOS array, the LCA100K, is the first of a new generation of gate arrays that will be available in the next few months. The new array is the first to use a 1- $\mu$ m process, and it is the first to use a triple-level metal process. The array is the first to use a 100,000-gate chip, and it is the first to use a 100,000-gate chip that is the first of a new generation of gate arrays that will be available in the next few months.

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**TECHNOLOGY WATCH**

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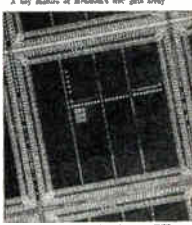
*They do it with triple-metal CMOS and flexible power-bus routing*

By J. Robert Cramer

Motorola's new HDC series of CMOS arrays is the first to use a triple-level metal process, and it is the first to use a 100,000-gate chip. The array is the first to use a 1- $\mu$ m process, and it is the first to use a triple-level metal process. The array is the first to use a 100,000-gate chip, and it is the first to use a 100,000-gate chip that is the first of a new generation of gate arrays that will be available in the next few months.

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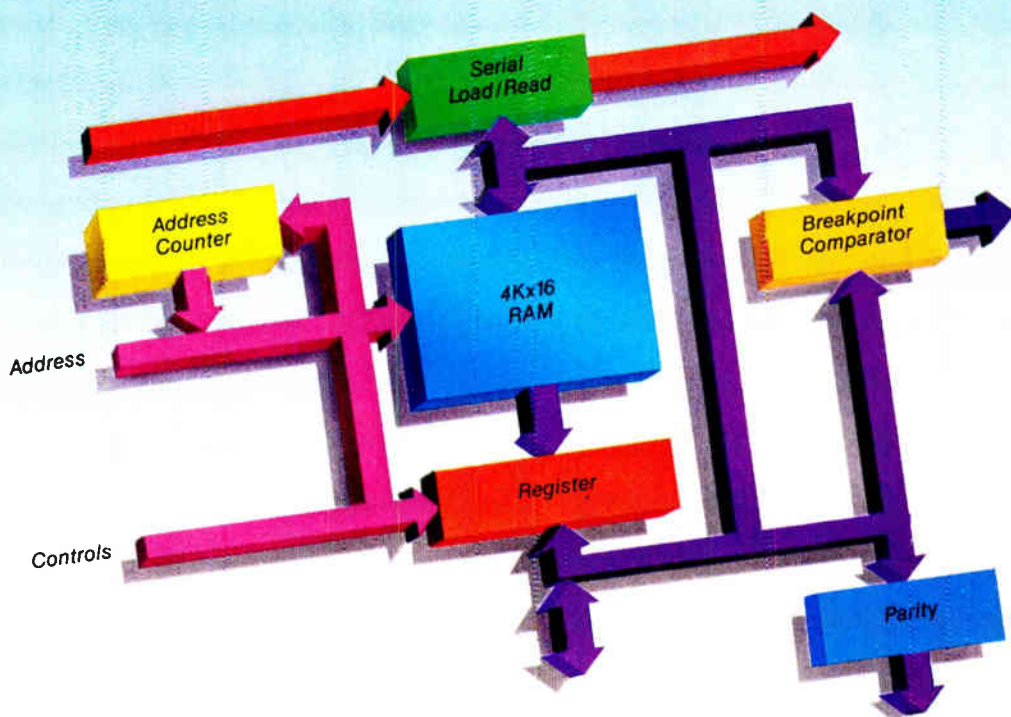
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A Motorola HDC array chip showing the complex circuitry and metal layers.

*Works Like 3 Chips in 1!*

# A 4Kx16 CMOS SRAM Plus a Whole Lot More



The core of the IDT 71502 is a 4Kx16 CMOS static RAM. But surrounding that core are features that will make your mouth water. Features that make the IDT 71502 work like 3 chips in 1.

### **It's a Writable Control Store**

The IDT 71502 SRAM is ideal for microprogram writable control store use. There are on-chip features like width and depth expandability plus high-speed serial load and readback. A pipeline register with selectable flow-thru bits. There's a parity generator for better system reliability. And a breakpoint comparator coupled with IDT's Serial Protocol Channel (SPC™) that allows in-system debug and diagnostics. All these features combined with a 35ns clock set-up time make the IDT 71502 a one-chip solution to your control store design.

Our expertise in the writable control store product area also allows us to offer you a wide range of high-speed module solutions: the IDT 7M6032 (16Kx32), the IDT 7MB6042 (8Kx112), and the IDT 7M6052 (4Kx80).

### **It's a Data Recorder**

In its data acquisition mode, the IDT 71502 captures 16 bits of data at a fast 20MHz clock rate. Simply clock the on-chip address generator and store up to 4K sequential samples. Block data recording is a piece of cake. And you can monitor system performance in real-time.

### **It's a Logic Analyzer**

Want to include logic analysis capability in your system? With the IDT 71502 it's a simple matter to perform diagnostic bus monitoring combined with real-time stop-on-event system analysis. And SPC with the on-chip comparator lets you preset addresses or data breakpoints.

### **Packaging**

Package options include 48-pin plastic or side-braced DIPs, a 48-pin LCC and a 52-pin PLCC. MIL-STD 883C versions are also available.

### **Call For More Information**

If you have questions concerning price, availability or technical issues, call our Marketing Hotline at (800) 544-SRAM.

If you need technical literature, call (408) 492-8225 and we'll send you a FREE copy of the IDT Data Book. It contains complete information on our other CMOS lines including SRAMs • FIFOs • Dual-Ports • ADCs • DACs • ultra-fast RISC Processors and Bit-Slice ALUs • DSP Building Blocks • ECL RAMs • TTL Logic • Modules • and much more.



*Leading the CMOS Future*



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Circle 26 on reader service card



# Toshiba LED Module Achieves Delicate Display with 16-Gradient Control.

The forms and functions of information and its handling are diversifying with great speed. Toshiba, a world leader in the opto-electronics field, has developed a 16 × 16 LED dot matrix module that opens new possibilities in information display. By combining these modules, a display equivalent to that of a TV can be realized. By use of Toshiba's outstanding two-color LED together with its unique gate array for driving, 16-gradient control is achieved in this new product. Compact design makes the module lightweight and optimally thin. Unique heat radiation design greatly improves the dispersion of heat from the module, and connections are simple, ensuring freedom from maintenance. In applications ranging from simple messages to visual displays such as message boards, entertainment and projector use, Toshiba's LED module is a standout.

CHARACTERISTICS	DETAIL					
	TLMM501B2	TLGM501B2	TLSM501B2	TLMM502A1	TLGM502A1	TLSM502A1
Type Name	TLMM501B2	TLGM501B2	TLSM501B2	TLMM502A1	TLGM502A1	TLSM502A1
Color Display*	Red, Green, Amber	Green	Red	Red, Green, Amber	Green	Red
Dot Size	ø5mm			ø3mm		
Dot Pitch	6mm			4mm		
Weight (Typ.)	170g	165g	165g	95g	85g	85g

\*Amber color is made by a mixture of red and green.



# TOSHIBA

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Circle 204 on reader service card