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A VNU PUBLICATION

Electronics

MAY 26, 1988

SUPERFAST SIMULATORS

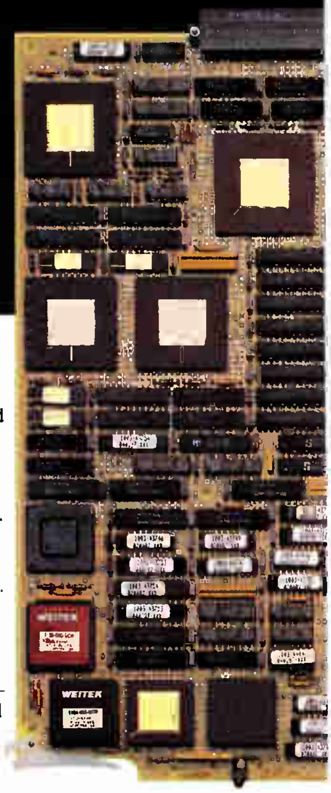
IT GETS A LOT EASIER TO SKIP PROTOTYPING

PAGE 61

GATEWAY SIMULATES FAULTS 10 TIMES FASTER/63

GENRAD ELIMINATES DESIGN-TO-TEST TRANSLATION/65

This year, you'll hear a lot of claims that "systems" design automation has arrived.



This 32-bit processor board was designed and simulated on Mentor Graphics workstations by Sequent Computer Systems for its multi-processor Symmetry computer system. It contains over 175 IC components including 80386 processors, a 14,000-gate standard cell and two 10,000-gate arrays.

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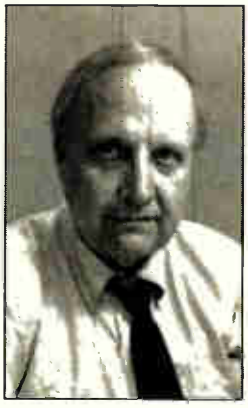
Circle 1 on reader service card

IS THIS THE ULTIMATE TECHNOLOGY ALLIANCE?

Al Stein's VLSI Technology had to have a 1-micron CMOS process fast, and Hitachi badly needed design help in ASICs; a good deal for both?



Has chip making reached the stage where no single producer—no matter how good or how big—can do the entire job worldwide? I think so. Why? For one thing, the ultimate technology alliance may have just occurred. Al Stein is trading the store.

The current market environment seems to be the catalyst for the deal between Al's VLSI Technology Inc. and Japan's giant Hitachi Ltd. Al had to get a 1-μm CMOS process fast to keep up in the ASIC market and Hitachi badly needed ASIC design technology to move into that fast-growing business in a big way. This deal should really open the door for Hitachi; until now its efforts can best be described as embryonic. VLSI Technology will hand over its leading ASIC design technology and its current and future ASIC cell libraries, while Hitachi will trade its CMOS processes and manufacturing expertise.

While at first blush the deal sounds much like the camel getting his nose under the tent, Al is no pushover. I've known him for nearly two decades, and I know of no stronger industry manager. But he does have a problem most ASIC houses are stuck with now: lack of profits. ASIC houses need big profits to invest in order to keep up with fast-moving process technologies. Al had to do something fast. "It would have been very costly for us to do it ourselves," he says, "and if we didn't get a 1-μm process pretty soon, we'd be in serious trouble."

Hitachi also seems to bowing to the inevitable. Besides getting crtical ASIC design tools, it seemed to be trying to avoid trade friction by establishing a major overseas alliance. Although VLSI Technology began pitching such an alliance aggressively in Japan more than three years ago, it was only a year ago that Hitachi management "at a very high level" came back to Al anxious to make such a deal. "Hitachi was very open with us—like a U.S. company," Al recalls.

Still, getting into bed with Hitachi seems like getting into bed with an elephant. "We were concerned," Al admits, "because they are 20 times bigger than we are, and they could run over us!" But he has written in plenty of safeguards, and 40 key people are deeply involved in the alliance. Al says he and his new president, Jim Fiebieger, are also spending a lot of time on the agreement. "Jim just cancelled a ski trip to meet with Hitachi—and he's an avid skier."

In June, *Electronics* will begin publishing monthly from VNU Business Publications' headquarters in Hasbrouck Heights, N.J. We will continue to turn out, as well as keep improving, the best coverage anywhere of technology and business trends for worldwide industry managers. Editors formerly based in Manhattan can now be reached at (201) 393-6000. **ROBERT W. HENKEL**

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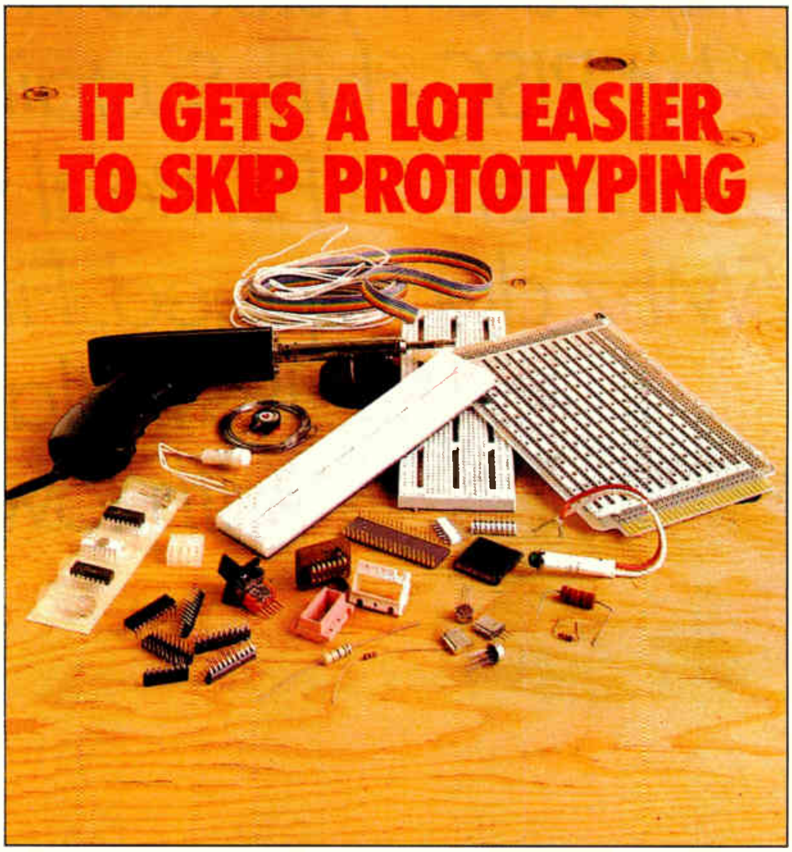

PAGE 61

NEW PRODUCTS

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Circle 7 on reader service card

An argument for digital neural nets

To the editor: I am writing in response to the Editor's Letter, "It takes time, but justice does triumph" [*Electronics*, April 14, 1988, p. 3].

I, too, am happy to see Federico Faggin finally achieve the acclaim that he deserves for his pioneering work on the microprocessor. What troubles me is his latest work in artificial neural networks and his statements about "massively parallel structures of analog computation elements." Such brainlike networks are thought to offer a way for computers to understand what they see and hear. The inference, however well-justified, that I draw is that since he was right once about the microprocessor, the odds are good that he will be right again—that artificial neural networks will be analog.

Everywhere I look, I see articles about why artificial neural networks should use analog elements for construction. The reasoning seems to be that since the brain is analog, then electronic realizations of it should be analog as well. Yes, there are good arguments to be made about the high density of resistor networks, such as those being made at AT&T for storing weight matrices, or how a single transistor can act as a multiplier and that a wire-and-amplifier connected to many such transistors can easily sum their products as currents. However, let us not forget that the brain operates at a constant temperature of 98.6 degrees.

How many electronic circuits can we sell if we must maintain them at a fixed temperature in order to maintain their performance? All of the nasty little problems about the effects of changing temperature upon resistor values, leakage currents and offset voltages cannot be ignored. One of the reasons that DSP chips became such a hit 10 years ago was that temperamental analog circuits could be replaced by well-behaved digital ones.

The point that I am trying to make is that I find the thought of using massively parallel analog chips frightening. Intriguing, but frightening. The prospect for a "whole wafer . . . containing 1 billion components" is even more disturbing. The variations in transistor parameters across even a small chip are bad enough. Naturally fault tolerant? Maybe. But how many digital, wafer-scale circuits work?

Let us get back to basics. Two technology-independent lessons that come to my mind from artificial neural networks are the following. First, one needs a compact, low-power, basic structure that stores a large matrix and has a mechanism that is intimately connected to it (breaking the von Neumann bottleneck) so that a vector of stimuli may be multiplied quickly. This structure should be inexpensive and must gracefully allow various precisions and matrix dimensions to be handled as befits the needs of the application. Second, one must be able to build networks of such basic structures in a wide variety of ways, providing feedforward, feedback, and adaptive capabilities.

Given these basic lessons, we at startup Oxford Computer have found another solution to the problem. We are planning to use memory technology in a novel way. Memory technology, not memory chips. This will enable us to build "intelligent memory chips" that store a matrix and a vector, and quickly multiply them together in a highly efficient, low-cost way. Such a matrix contains information that represents patterns, and the vector represents acoustic or visual stimulus. Each simple chip combines two dense, high-capacity memories with hundreds of very, very simple processors. One column from each memory is connected to each of the processors, and the results from all of the processors are summed.

This solution is totally digital, and as a result of some simple, built-in shift registers, can implement ordinary convolution and correlation operations for image processing as well. Furthermore, since interconnections between chips are few and time-division multiplexed, complex structures may easily be built.

Steven G. Morton
Founder and Chief Technical Officer
Oxford Computer, Oxford, Conn.

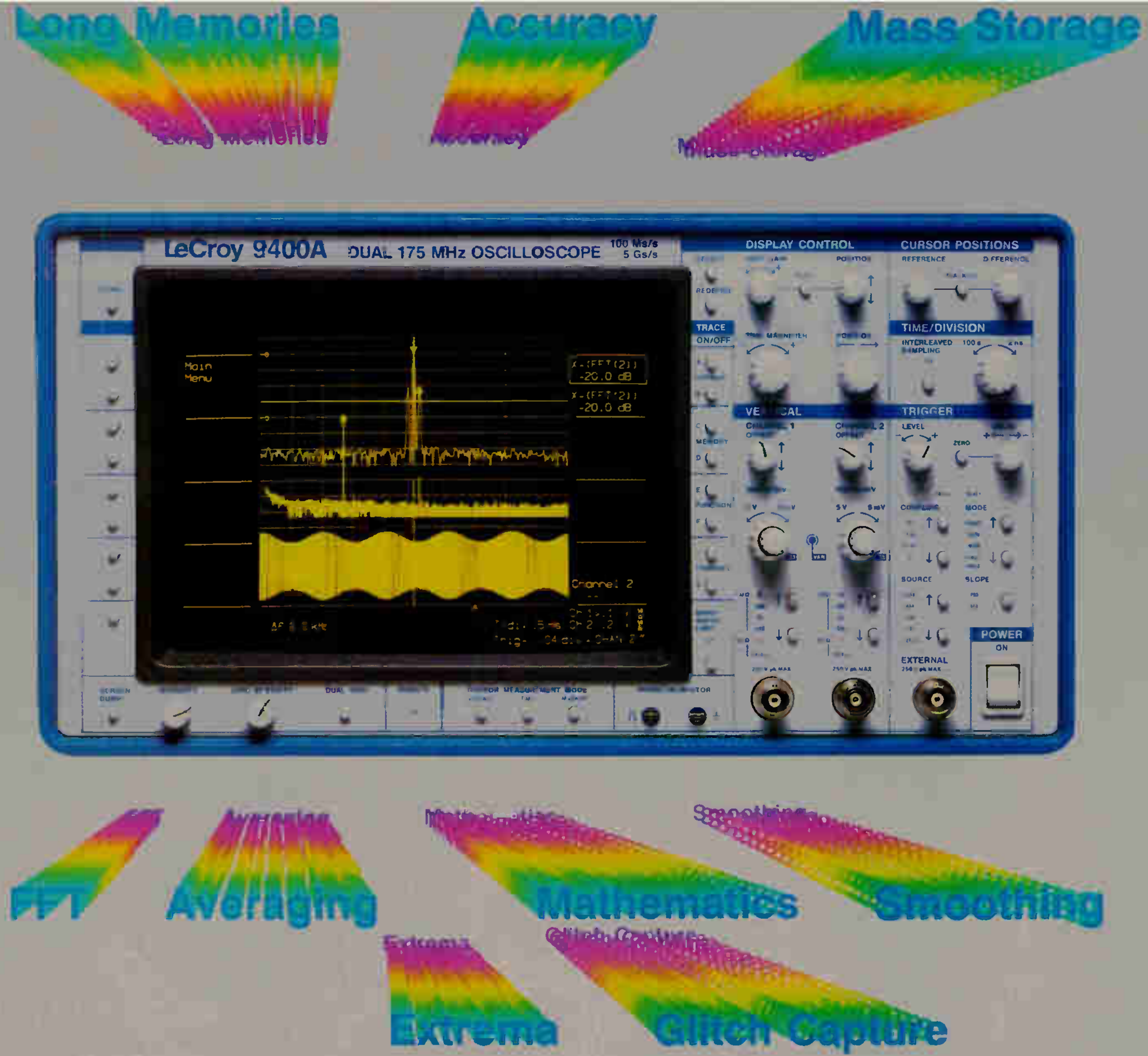
DSP speed depends on how you count

To the editor: The Analog Devices ADSP-2102/2 DSP microcomputer can perform a 1,024-point complex, in-place, radix-4 FFT in 3.0 ms and a radix-2 version in 4.4 ms, as correctly reported in your magazine [*Electronics*, March 31, 1988, p. 70]. (The ADSP-2100A DSP microprocessor can also achieve this performance, as also reported in *Electronics*). The benchmarks for our competitors, taken from their published literature, were also correct.

You chose to do an apples-to-apples comparison by listing benchmarks for *in-place* FFTs. If the requirement of being in-place is relaxed, the fastest announced Motorola 56000/1 (at 10.25 MHz) does improve to 3.4 ms, as Kevin Kloker of Motorola states in his letter of April 28. The ADSP-2101/2 remains the fastest announced general-purpose, fixed-point DSP processor at executing a 1,024-point complex FFT.

David Fair
Product Marketing Manager
Analog Devices Inc., Norwood, Mass.

Correction: *In the article describing Texas Instruments Inc.'s erasable PLDs made with the the HVEPIC process [Electronics, May 12, 1988, p. 70], power dissipation of the devices is cited as "fewer than 500 mW." That should be μW.*



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HOW FISCHER IS INTEGRATING COMPUTERVISION INTO PRIME

BEDFORD, MASS.

Down-to-earth, as comfortable as an old shoe: that's the way people who know him describe Robert A. Fischer, the new president of the Computervision Division of computer maker Prime Computer Inc. Add those people skills to solid credentials in the computer-aided design and computer-aided manufacturing business and the combination suggests that Fischer has a good chance to integrate CAD/CAM-pioneer Computervision Corp. into Prime with a minimum of upheaval. That task became Fischer's job in the wake of Prime's unfriendly takeover of Computervision [*Electronics*, Feb. 4, 1988, p. 22].

The move created the second largest competitor in the CAD/CAM arena. The merged company, with combined sales last year of about $1.5 billion, claims a 17% market share, trailing only IBM Corp. by 5% or 6%. Achieving that kind of critical mass is what the merger was all about, Fischer says. He was president of Prime's CAD/CAM and work station/terminals group before the merger after coming to Prime in Natick., Mass., in 1986 from McDonnell Douglas Corp.'s CAD/CAM operation—the Information Systems Group—where Fischer had been chief executive officer.

Now he's shifted his office a dozen miles north to Computervison's Bedford headquarters, which has become Prime's sales and marketing organization for the manufacturing industries. Fischer relishes the opportunities in a market he says is consolidating rapidly. That consolidation is what drove Prime to move on Computervision in the first place and is the backdrop against which Fischer says the Computervision organization will ultimately accept the takeover.

Fischer: "Computervision wasn't big enough to succeed in a consolidating market."

He acknowledges that there was "a dip in morale" after the takeover. The merger was vigorously resisted by Computervision management, led by former president Robert L. Gable, who has since resigned. "Computervision would have preferred to remain independent," Fischer says, but since the merger, "when we talk to the employees and explain that Computervision wasn't large enough to succeed long-term in a consolidating market, most of them accept that as reality."

Fischer says morale has since improved from negative to neutral; he's optimistic it will swing to positive soon. "The early caution is changing as the people here see that we want to continue Computervision as a good place to work and a successful business. And the further we go, the more people realize that consolidation with someone was inevitable."

The new organization combines into one entity the attributes Fischer says are needed in a market that will have only "four or five significant players by the end of 1989." Those attributes are a substantial market share, a large installed base and what he sees as a superior product line. "We're probably the only company that 'owns' two world-class CAD/CAM products," Fischer says—Computervision's CADDS and Prime's Medusa. "We can control the development of those products, and that's important."

ALREADY DUG IN. Fischer explains that Computervision's CADDS integrated software for mechanical engineering, design and manufacturing is well entrenched in very large manufacturing organizations, including a leading U.S. auto maker. Prime's Medusa software for two-dimensional drafting and three-dimensional solids modeling is established in manufacturing organizations ranging from $5 million to $1 billion in size. "So now we have customers ranging from small to medium to the largest companies in the world," he says.

Since moving to Bedford in early February, Fischer's time has been occupied mainly in getting to know Computervision's customers, "putting together a management team and agreeing on product and market directions," he says. "Now it's time to get most of our attention focused on opportunities in the market. The potential is there to be wildly successful." *–Lawrence Curran*

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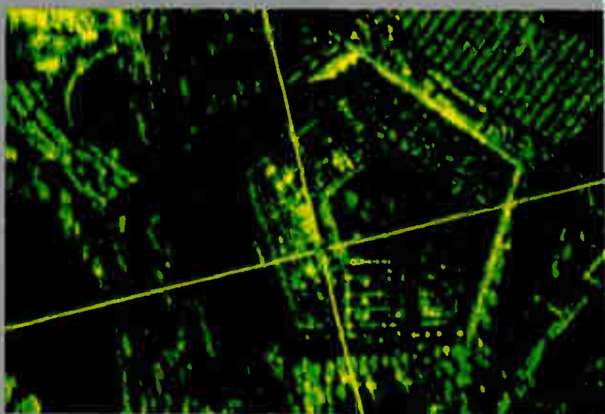

While developing software for the B1-B Bomber radar system, Westinghouse Defense landed on a tough problem – integrating its computer resources. "We needed a complete network that would allow hundreds of software engineers across the country to interact, create, enhance and modify the software," says Ron Clanton, Manager of Software and Information Systems.

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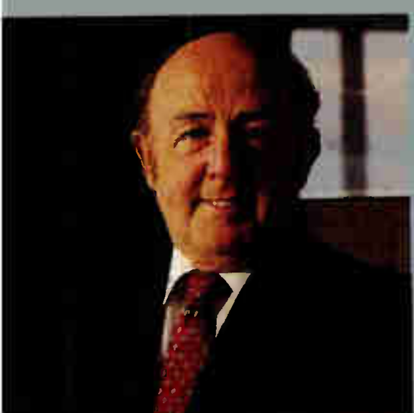
Remarks Clanton, "The network is so comprehensive, it extends even to the air in our Flying Software Lab. Giving us real-time, in-flight software testing and development capabilities. The Software Lab alone provides a cost savings of up to 98% versus traditional in-flight testing in the B1-B Bomber."



"A networked software engineering environment that helped Westinghouse Defense zero in on ways to cut in-flight test costs by 98%."

"But our savings don't stop there," continues Clanton. "With the VAX™ architecture and the VMS™ operating environment, engineers both on the ground and in the air can react instantly to each other's modifications." He adds, "That's sharing their knowledge and expertise faster and more productively than they ever thought possible. Which, of course, provides for a better end product."

Clanton sums it up this way, "Our Digital network and The Flying Software Lab allow us to cut software development time and costs across the board. And that's increasing our productivity and ability to compete for similar projects."

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ELECTRONICS NEWSLETTER

A MEGABIT OF MEMORY SWIMS IN A 72K SEA OF GATES

Toshiba Corp. is coming to the aid of designers who want a lot of semicustom logic and a big block of memory on a single chip for applications in graphics and speech processing. The Tokyo firm has developed an experimental chip that combines a 72K sea-of-gates array with 1 Mbit of memory that can be configured as either pseudo-static random-access memory or virtually static RAM. The gate array has a remarkably low propagation delay of only 400 ns for a 2-input NAND gate with a fanout of two, and 2-mm of output metal interconnections. Configured as 128-K-by-8 bits, the memory has an access time of 60 ns in the pseudo-static mode and 120 ns in the virtually-static mode. The large chip—it measures 14.95 by 14.95 mm—has 1-μm features. Toshiba described the chip at the mid-May Custom Integrated Circuits Conference in New York, and says it could reach the market in 1989. □

SURPRISE! TI STARTS SELLING IC TEST EQUIPMENT

Take a close look at what Megatest Corp. is showing at Semicon/West 88 in San Mateo, Calif., in late May, and you'll get a big surprise. Megatest will display new chip test and production gear from an unusual source: Texas Instruments Inc. The Dallas chip maker is breaking with its past policy of keeping out of the commercial equipment business and has inked a distribution pact with Megatest of San Jose, Calif. TI managers decline to discuss the scope of their thrust, but the first systems to hit the market will include TI's high-speed logic tester, called Impact-1, and two systems for inspection and conditioning of leads on surface-mounted chip packages. The Impact-1 tester, offered by TI in the past to selected integrated-circuit customers was developed two years ago to support ever-increasing chip speeds. The system can have up to four test heads for 32- and 64-pin ICs, and can handle wafers or packaged ICs [*Electronics*, Jan. 8, 1987, p. 38]. Impact-1 testers are expected to cost between $200,000 and $800,000. □

NATIONAL TESTS THE WATERS WITH A COMPLEX RISC DESIGN

Responding to the slew of reduced-instruction-set-computer chips springing from Silicon Valley, National Semiconductor Corp. is circulating preliminary specifications on its own RISC chip. The NS32764, however, is not a pure RISC design. Instead, it is a complex-reduced-instruction-set processor—or Crisp. While retaining compatibility with other members of National's 32000 family, it will also incorporate most, if not all, of the features used in more traditional RISC architectures to reduce the number of cycles per instruction from the current 2.5 to between 1.5 and 2. Current RISC processors, which are theoretically able to achieve one cycle per instruction, are in the 1.25- to 2-cycles-per-instruction range. Depending on the response to the current specifications and the number of redesigns required, the Crisp chip will debut some time in late 1989. □

MOZART SHOULD HAVE HAD IT THIS EASY

Consumers who can't read or write music may have an easy way some day to compose their own musical scores—provided they can at least carry a tune. A personal-computer-based music system developed by NEC Home Electronics Ltd. not only transcribes songs that are hummed or sung into a microphone, but it also generates a three-part accompaniment of chord backing, bass, and percussion. The melody and generated accompaniment can then be played together on a synthesizer. NEC will discuss the system at the International Conference on Consumer Electronics June 8-10 in Chicago, but marketing plans aren't yet clear. □

ELECTRONICS NEWSLETTER

NCR WILL ADD MORE ARTIFICIAL INTELLIGENCE TO ITS ASIC DESIGN TOOLS

NCR Corp.'s Microelectronics Division intends to make it easier for designers of application-specific integrated circuits to tap the power and productivity improvements that artificial intelligence can bring to their work. At the June 12-15 Design Automation Conference in Anaheim, Calif., the division will roll out NCR Design Synthesis, a front-end software tool based on expert rules. Based on technology developed by Silc Technologies Inc., Burlington, Mass., Design Synthesis works with many of the same design rules used by NCR Design Advisor, the back-end design-analysis tool introduced last year. This year, the Fort Collins, Colo., firm will announce versions of both tools that run on Mentor Graphics work stations, for use at customer sites beginning in the third quarter. As a prelude to its DAC introductions, the company in late May formed a separate business unit to market its ASIC design tools. □

THIS STEPPER CAN AUTOMATICALLY KEEP ITSELF IN LINE

One problem chip makers have always had when expanding a product from a single pilot line to full-fledged production is precisely calibrating stepper systems. Typically, external metrology tools are used to determine the precision of each machine, which are then adjusted manually to accommodate differences in magnification or alignment. If improperly calibrated, large discrepancies may arise between parts produced on different machines. But now ASM Lithography Inc. says it's licked the problem by integrating a metrology subsystem into its PAS 2500 line of wafer steppers. Thanks to the high-precision optics used in the new steppers to produce submicron line widths, the Tempe, Ariz., company was able to make the stepper its own metrology tool, using two-point through-the-lens alignment directly referenced to the reticle. A set of 23 parameters determines misalignment, and servo controls automatically move the stepper into line. □

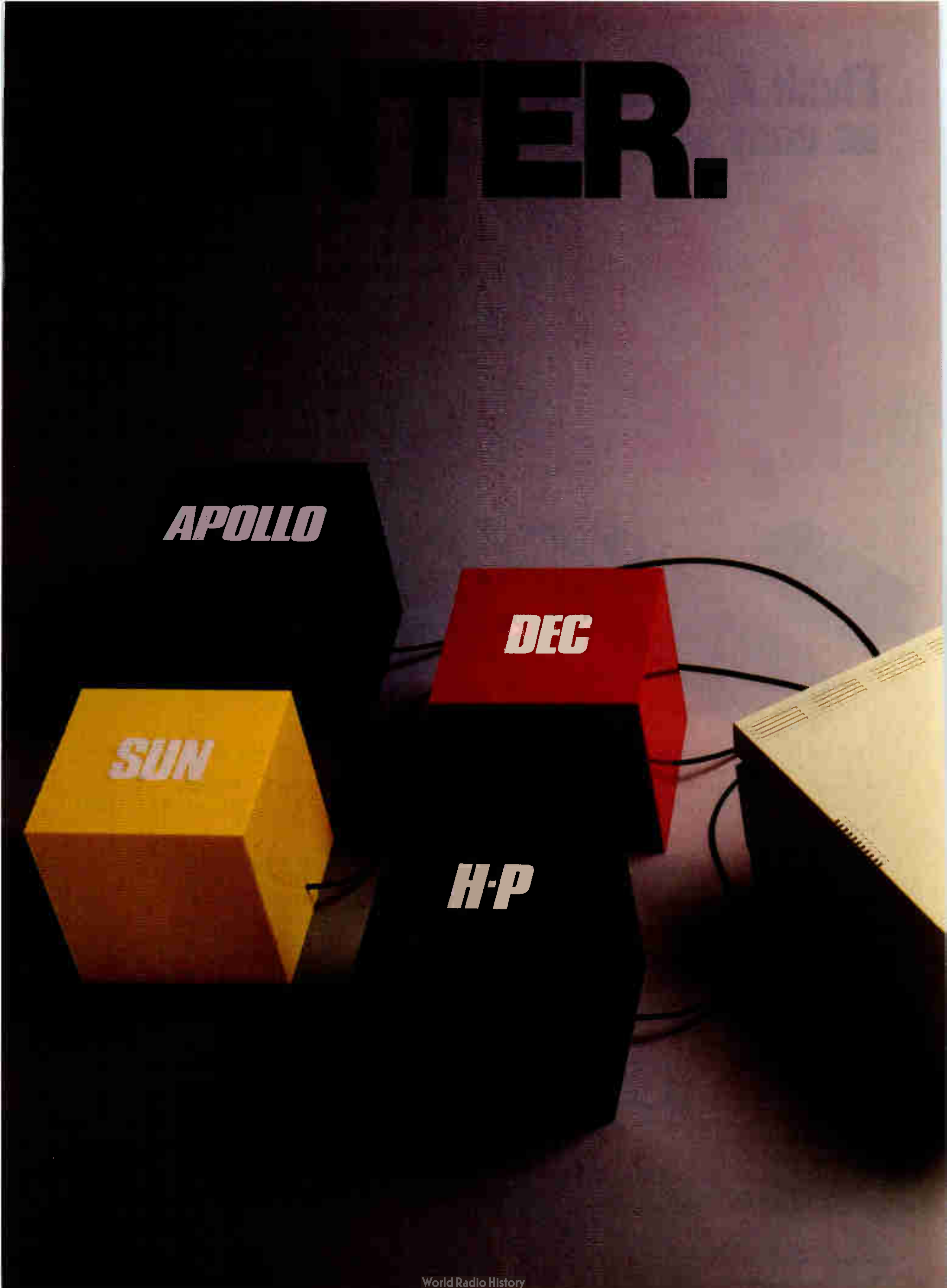
ARE FEDERAL LABS CONSTRAINED FROM WORKING WITH INDUSTRY?

Federal laboratories would like to get more of their work picked up by private business and developed, but cannot because of a variety of constraints, says a U. S. General Accounting Office report for the House Committee on Space, Science, and Technology. In interviews with officials at 10 federal labs, including the Naval Research Laboratory, Sandia National Laboratories, and NASA's Langley Research Center, the GAO found that because the labs' work resides in the public domain, businesses are unwilling to invest in marketing it—for fear that a competitor will have equal access to the underlying research. Software, for example, cannot be patented; hardware inventions, which can be patented and exclusively licensed, may not be developed because the early research behind the invention may be in the public domain; and lastly, federal regulations cause delays in collaborative efforts that inhibit industry participation. □

AMD SHARPENS ITS EMBEDDED-CONTROLLER RISC STRATEGY

Advanced Micro Devices Inc., which is aggressively pushing its 32-bit Am29000 chip into controller sockets, contends that embedded controllers offer a far richer market for reduced-instruction-set-computer chips than Unix computers. The Sunnyvale, Calif., chip maker says most of the 65 beta sites examining the 29000 are considering it for control applications. The Unix system market sought by many RISC suppliers "isn't interesting to us because it's too limited," claims Ben Anixter, AMD vice president. He estimates 250,000 Unix-based systems were sold last year compared with 10 million personal computers, which have ample control applications. □

Circle 23 on reader service card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PRODUCTS NEWSLETTER

TRIAD'S 64-KBIT STATIC RAM BOOSTS CYCLE SPEEDS 30% OVER THE COMPETITION

By integrating address-register functions on chip, Triad Semiconductors Inc. delivers a 30% speed boost in cycle times, compared with existing solutions, in its 64-Kbit static random-access memory—while reducing external memory component count by 25%. Organized as a 16-K-by-4 bits, the CMOS TRC1640's on-chip address registers and transparent data-output latches are a first for fast commercial SRAMs, says the Colorado Springs, Colo., startup. The on-chip registers eliminate the need for outboard bipolar registers, and by latching data outputs, the TRC1640 can eliminate address skew, allowing memory-access time to be longer than memory cycle time. It comes in three speed versions—25, 35, and 45 ns. Samples are available now in standard 22-pin dual in-line packages, with production volumes scheduled for July availabiity. In 1,000-unit quantities, the 25-ns version will be priced at about $15 each. National Semiconductor will be an alternate source for the part. □

SIMPLE-NET SYSTEMS' PC-AT CLONE RUNS AT 6 MIPS

Simple-Net Systems Inc. is delivering 6 million instructions/s in its IBM Corp. Personal Computer AT-compatible computer, as measured by the PowerMeter Version 1.2 benchmark, by boosting the clock speed on Intel Corp.'s 80386 microprocessor to 25 MHz. The NetPro 386/25 is the first PC AT clone to boost the 80386's speed to 25 MHz, claims the Brea, Calif., division of BCSoft Corp. The NetPro 386/25 also integrates 64 Kbytes of zero-wait-state cache memory and a 25-MHz 82385 cache controller. It comes in three configurations, with the high-end model 2 having a 120-Mbyte hard-disk drive, a 1.44-Mbyte, 3½-in. floppy-disk drive and a Video Graphics Adapter color display system. At a suggested price of $13,500, the model 2 is intended for applications as high-end network servers, design work stations, and standalone systems. □

GMFANUC'S TABLETOP ROBOT TAKES AIM AT ELECTRONICS ASSEMBLY

North American robot leader GMFanuc Robotics Corp. is sharpening its aim on electronics manufacturing with a faster and more accurate tabletop robot arm for high-speed pc board stuffing and disk-drive assembly. The SCARA-configured (for Selectively Compliant Assembly Robotic Arm) A-600 features 0.0005-in. repeatability, for example, compared to 0.001-in. on the Auburn Hills, Mich., company's current floor or ceiling-mount assembly models. Maximum linear arm velocity on the A-600 is specified at 326 in./s. The A-600 will be available immediately after the Robots 12 show in Detroit June 5-9. It can be paired with a new $20,000 GMF vision system called Insight [*Electronics,* Dec. 17, 1987, p. 22], which is also set for formal introduction at Robots 12. Pricing of the A-600 will be released at the Robots 12 show. □

TOSHIBA'S 1-MBIT STATIC RAM SAVES 30% ON POWER CONSUMPTION

Designers using 1-Mbit static random-access memory chips can squeeze a 30% power saving out of their high-speed systems, compared with competing SRAMs—and still get 70 ns access times—with Toshiba Corp.'s TC551001PL/FL. Fabricated with 0.8-μm design rules, the chip consumes only 70 mA during operation and 100 μA in standby. Power consumption is reduced by using a divided word-line configuration so that only necessary portions of the device operate, and by auto power-down circuits. The fast access time of 70 ns was made possible by reducing time delay in bit lines and innovative design of sense amplifiers. The chip, which teams CMOS in peripheral circuits and NMOS in memory cells, will be available as samples in June for 30,000 yen in the domestic market and $250 in overseas markets. Production quantities will be available in the fourth quarter. □

PRODUCTS NEWSLETTER

ION-BEAM SYSTEM HANDLES ASIC DESIGN CHANGES WITHOUT NEED TO MAKE NEW MASK

Semiconductor manufacturers can eliminate the time and costs associated with making a new mask for each modification in an application-specific integrated circuit design by using Micrion Corp.'s latest version of its focused-ion-beam system. The company's model DMOD—for Direct Modification—system can direct its ion beam precisely enough on fully processed silicon wafers, for example, to drill new vias or to selectively add metals like tungsten or gold by passing the ion beam through a selected gaseous mixture. A major advantage of the new system is its higher resolution compared with machines for the same task based on laser technology. A follow-up and major enhancement of the Beverly, Mass., company's model 8089 mask-repair system, the DMOD will be shown at Semicon West '88 [see p. 101]. Available now with delivery in four to six months, it costs between $600,000 and $1 million depending on application and configuration. ☐

HP'S MAP 3.0 INTERFACE CARD OFFLOADS COMMUNICATION CHORES FROM HOST COMPUTER

System integrators looking for a fast, efficient way of controlling a multivendor network of factory products conforming to the Manufacturing Automation Protocol Version 3.0 can do it without degrading host processor performance using Hewlett-Packard Co.'s HP OSI Express MAP 3.0 interface card. Based on a 12.5-MHz Motorola Corp. 68020 processor, two HP-designed VLSI controller chips, and a carrier-band modem, the card plugs into HP 9000 series 800 computers, and takes over all factory-floor protocol and communications functions. It addresses up to 100 nodes—more than three times the number possible with MAP 2.1. Offering full MAP functionality, it is the first device to implement the full seven layers of the Open Systems Interconnection protocol, say executives at HP's Networks Division in Roseville, Calif. Available in the fourth quarter, the card will cost about $5,000. ☐

DATEL'S 12-BIT ADC COSTS HALF THE COMPETITIONS' PRICE

A high-speed, hybrid 12-bit analog-to-digital converter boasting 1-μs conversion delivers a combination of features that its developer, Datel Inc., says is unrivaled on the market—for half the price. The ADC-511 is functionally complete, integrating an internal clock and internal reference that can supply +10 V at 1.5 mA externally. It comes in a 24-pin package, dissipates just 925 mW, and sells for $99 in quantities of 1,000. The Mansfield, Mass., company says roughly competitive units offering 12 bits of resolution either need external circuitry—such as the reference—come in a larger package, or sell for about $100 more than the ADC-511. It is available now. ☐

EPROM IDENTIFIER ALGORITHM FROM SGS-THOMSON SPEEDS PROGRAMMING

Programming a new ultraviolet-erasable programmable read-only memory from SGS-Thomson Microelectronics will be a snap on the assembly line thanks to a high-speed algorithm that automatically tells programming equipment the device type and manufacturer. Fabricated in CMOS technology, the 256-Kbit 27C256 is organized as 32-K-by-8 bits and comes in 300-, 250-, 200-, 170-, and 150-ns versions. It is housed in an industry-standard Jedec 28-pin cerdip package. To further strengthen its programmable-memory line, the Franco-Italian company is also fielding three one-time programmable ROMs in low-cost plastic packages: the 27C64/P and 27C64/FN are 8-K-by-8-bit devices, with the P version housed in a 28-pin plastic DIL package and the FN version housed in a Jedec 32-pin plastic leaded chip carrier. The 32-K-by-8-bit 27C256/P comes in a 28-pin dual in-line package. The products will be available in the third quarter. Pricing has not been released. ☐

ARRAY FOR BiCMOS!

180 MHz with low power.

It's cause for celebration. AMCC extends its lead as the high performance/low power semi-custom leader with three exciting, new BiCMOS logic arrays that optimize performance where today's designs need it most. In throughput (up to three times faster than 1.5µ CMOS).

Today, system designers look at speed, power and density. For good reasons. As CMOS gate arrays become larger and faster, designers can't meet their critical paths due to fanout and interconnect delay. As Bipolar arrays become larger and faster, power consumption becomes unmanageable. So AMCC designed a BiCMOS logic array family that merges the advantages of CMOS's low power and higher densities with the high speed and drive capability of advanced Bipolar technology. Without the disadvantages of either.

Q14000 SERIES	Q2100B	Q9100B	Q14000B†
Equivalent Gates	2160	9072	13440
Gate Delay* (ns)	.7	.7	.7
Maximum I/O Frequency (MHz)	180	180	180
Utilization	95%	95%	95%
Power Dissipation (W)	1.8	4.0	4.4
I/O	80	160	226
Temperature Range	COM, MIL	COM, MIL	COM, MIL

*(2 loads, 2 mm of metal) †Available soon

Our new Q14000 BiCMOS arrays fill the speed/power/density gap between Bipolar and CMOS arrays. With high speed. Low power dissipation. And, mixed ECL/TTL I/O compatibility, (something CMOS arrays can't offer).

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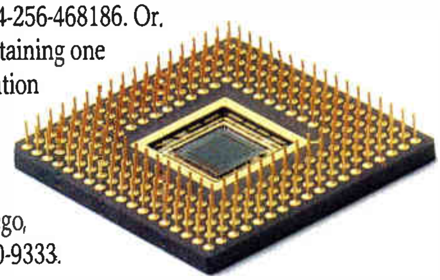

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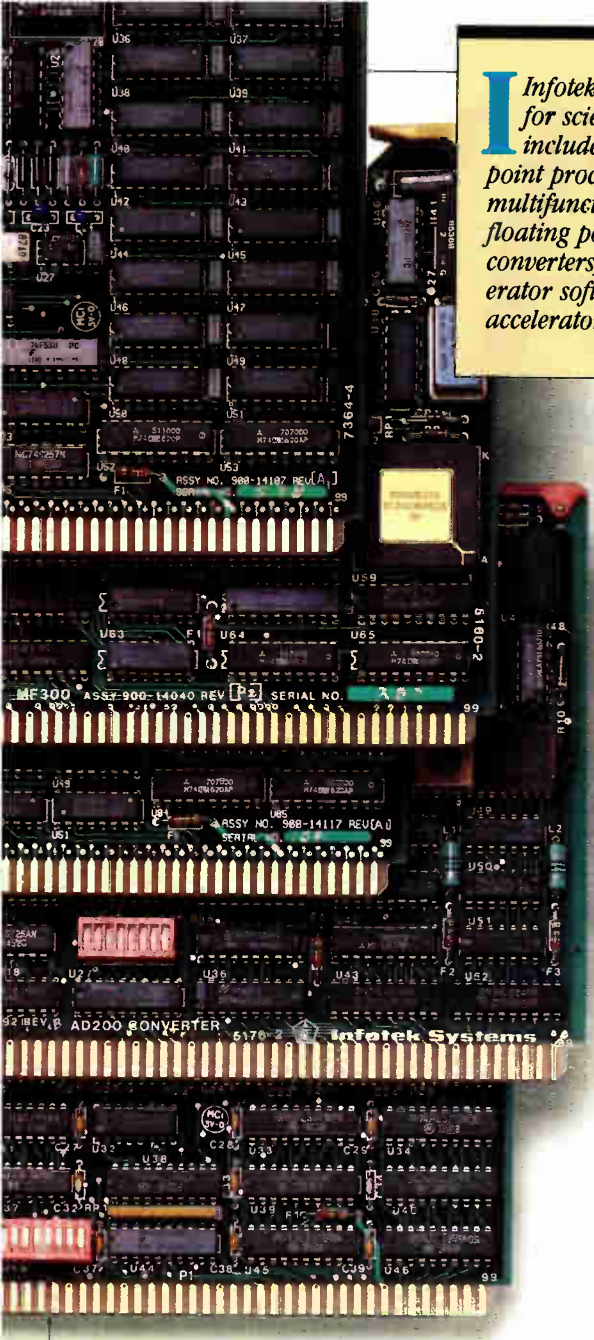
A Better BiCMOS Array is Here.

AMCC

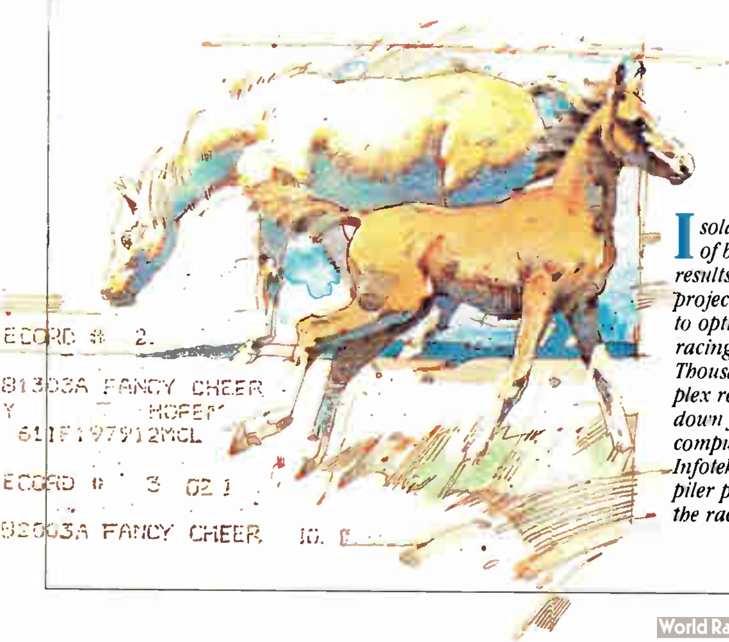


Infotek's full family of enhancements for scientific and engineering computers includes: high-performance floating point processors, memory to eight MBytes, multifunction cards which put memory and floating point in a single slot, A/D and D/A converters, BASIC compilers, matrix accelerator software and a new line of graphics accelerators.

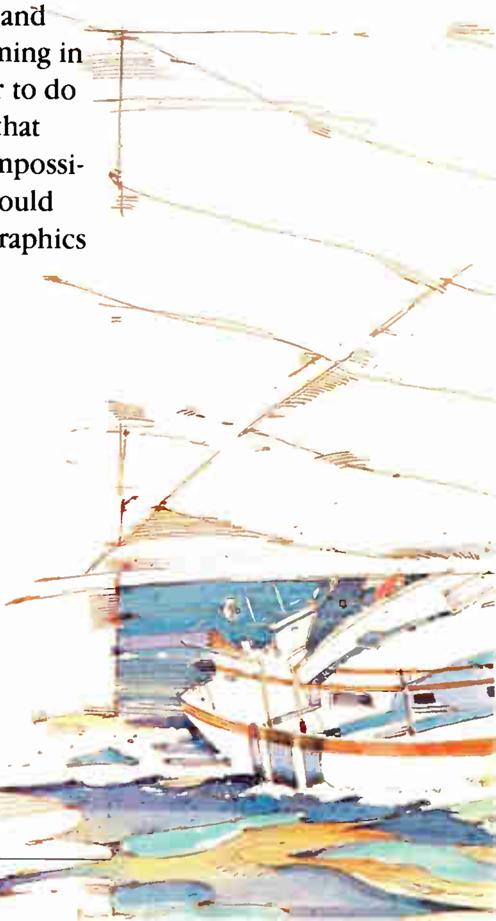
Infotek and

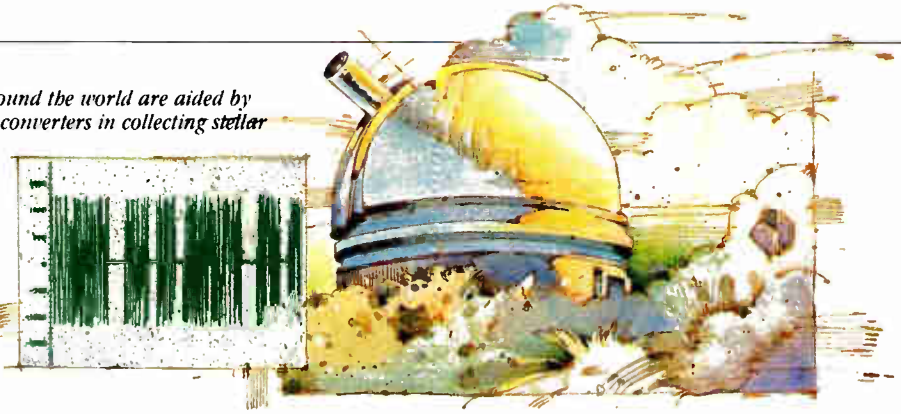
Perhaps you're never going to race a horse, build a log cabin, design a yacht or track a space craft—but imagine what you could do if your technical computer could perform real math or transcendental functions faster—a lot faster!—Or if you could find the precision, speed and ease of programming in an A/D converter to do data acquisition that was previously impossible.—Or if you could accelerate your graphics ten or more times.

That's the kind of capability that has opened a world of imaginative new ideas and developments to Infotek customers worldwide. Users regularly say that "no other product would do the job" until they found Infotek. And that's why



Isolating the effects of breeding on race results is a personal project of John Willey to optimize his horse-racing business. Thousands of complex records bogged down John's technical computer, until an Infotek BASIC compiler put him back in the race.





Telescopes around the world are aided by Infotek A/D converters in collecting stellar images to infer atmospheric distortions. No other converters offer the required linearity, speed and ease of programming to reach the stars.

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Infotek is considered the world leader in enhancements for HP engineering and scientific computers. In a market where excellence is expected, Infotek stands out for its unparalleled reliability as well as performance—a fact reflected in long warranties and happy customers.

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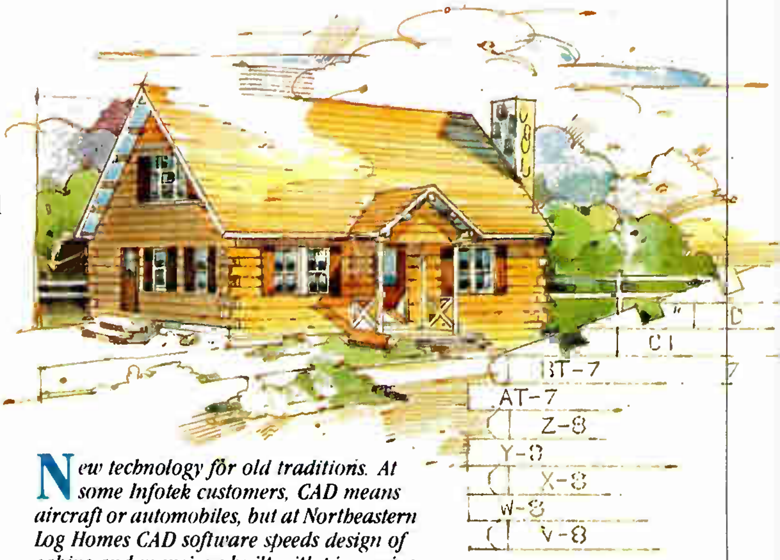

New technology for old traditions. At some Infotek customers, CAD means aircraft or automobiles, but at Northeastern Log Homes CAD software speeds design of cabins and mansions built with pioneering style. Infotek supplied the memory to run the software—"and great service, too!"

Infotek's high-capacity, high-reliability memory boards and fast BASIC compiler help put Ammarc/Design Systems under full sail with FAST YACHT,© a CAD software system for naval architecture.

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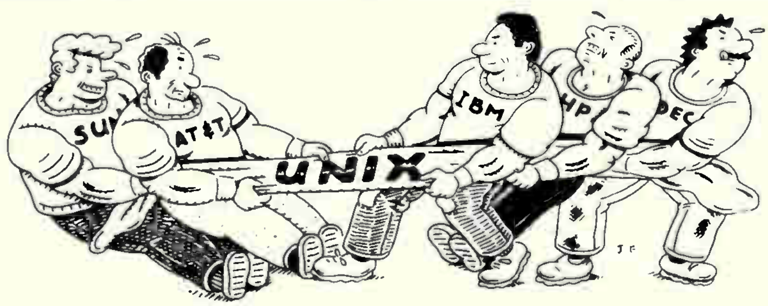
Electronics

INDUSTRY LEADERS WILL CHALLENGE AT&T WITH THEIR OWN UNIX STANDARD

Do IBM, DEC, and HP hope to gain from the resulting confusion in the industry?

NEW YORK

There is growing feeling in the computer industry that it's time to yank Unix out of the hands of AT&T Co. The operating system developed at Bell Laboratories is gaining market share fast as a software platform, and it's become a major factor to big computer vendors and users alike. But work-station vendors, in particular, don't feel they can trust AT&T as the steward of so important a standard.



Now IBM Corp. has joined forces with members of the so-called Hamilton Group [*Electronics*, Jan. 21, 1988, p. 33] led by Hewlett-Packard Co. and Digital Equipment Corp. Together with Apollo Computer, Honeywell Bull, Siemens, and Nixdorf Computer, the trio set up early this month a new organization to implement and license a nonproprietary operating system based on Unix. The organization, funded by $90 million from the seven sponsors, is called the Open Software Foundation, and is based in Billerica, Mass., until a permanent headquarters is set up elsewhere.

Observers don't see the motives of the sponsoring companies as entirely pure—after all, each of them sells systems built around proprietary operating systems, and industry giants DEC and IBM in particular stand to benefit from confusion in the Unix community. But no one sees AT&T as entirely noble in its motives, either. It has used changes in Unix software as competitive weapons before, sources say, and there's no reason to believe it won't do so again, despite protestations to the contrary from AT&T and its new partner, Sun Microsystems Inc.

The founders of the Open Software Foundation say that the operating system it develops will be open and "vendor-neutral." They invite other computer and software companies to join the corporation and have voting and technical input to the development process. But the result is that while Sun and AT&T go about developing the next version of Unix—System V Release 4, due out in the autumn of 1989—the Open Software Foundation will be putting together a different, competing, version. The new corporation intends to follow guidelines very similar to those set up by X/Open Co. of San Francisco, embracing the IEEE Posix and MIT X-Windows standards; it will be based on code developed for a future version of IBM's AIX Unix-derived operating system.

But Unix users want a single standard, not two. Much work has gone into bringing the splintered variations of Unix back together, and the moves of the new group seem to subvert that effort. Many think that such confusion, and the repercussions that could follow in the marketplace, are exactly what IBM and DEC want. "I think IBM and DEC are quite content to throw fuel on the fire," says Michael Tilson, president of HCR Corp., a Unix software house in Toronto, Canada.

At the same time, many see HP's Unix commitment as far less ambiguous than DEC's or IBM's. "We are concerned about recent moves by AT&T that would tend to make Unix less open, in our view," says an official company statement. "We have expressed our concern to AT&T at the highest levels, but are not satisfied with their assurances."

Vittorio Cassoni, outgoing president of the AT&T Data Systems Group, sees some irony in the situation. The war, he says, "is being led by companies that made proprietary systems a key strategic thrust." He calls it "an historical paradox—proprietary, closed vendors that are suddenly converted to a new religion . . . claim that Unix is not open enough." Moreover, he notes, there have been no changes in AT&T's Unix licensing policies to justify the furor.

But it's not AT&T licensing that has the other companies nervous, it's the recent alliance with Sun. So long as AT&T was not a major factor in the computer-system market, the use of Unix as a marketing weapon was not a big threat. The picture is very different now, "because Sun is an effective marketer of computer systems," says HCR's Tilson.

The fact that the Mountain View, Calif., company is helping AT&T develop the next version of Unix is highly disturbing to companies like HP and Apollo, who are Sun's direct competitors in the Unix-based work-station market. The fear is that the new Unix will run better—as well as sooner—on systems using Sun's Sparc reduced-instruction-set computer chip.

"I have always had trouble understanding how AT&T could play both the above-it-all standard-bearer and be in the middle of it, a competitor," says Larry Michaels, president of The Santa Cruz Operation, a major reseller of Unix. "And although AT&T has not been particularly successful as a competitor, by forming an alliance with Sun, that changes. I really do sympathize with Hewlett-Packard. They've got to be scared out of their wits to have an operating system controlled by a direct competitor."

But on the new user group's side, "you have a bunch of people in this alliance that don't have common cause," says Michaels. In DEC's suit last year over the large Air Force Unix-system contract the firm "really wanted to slow down the progress of the System V Interface Definition," Michaels believes. "Given that, you've got to say that DEC's purpose is to confuse, to obfuscate. HP clearly has a desire for a standard, and it wants freedom from Sun. The fact is, you've got a lot of mixed motives here." *–Jeremy L. Young*

DEBUGGER FINDS NEW LIFE AS TESTER

SAN JOSE, CALIF.

You build an instrument to solve a specific problem. Then, no sooner do you get the machine into the field when customers discover that it can be used for entirely different purposes. That's called serendipity, and it's what happened to a diagnostic system from the Advanced Products Group of Schlumberger Technologies ATE Division, San Jose, Calif. Now the group has moved to capitalize on the new opportunity.

When Schlumberger introduced its IDS5000 hardware last year [*Electronics*, April 30, 1987, p. 51], the $495,000 system was intended to debug prototype chips during the design phase. But it turned out that many are being used to locate problems in chips returned from the field. So to more quickly isolate troubles in returned chips, the company is introducing a new version, the IDS4000, that incorporates a feature called dynamic fault imaging.

The new system "will cut the time it takes to locate a fault from weeks to days," says Sabbas Daniels, senior failure engineer at VLSI Technology Inc. of San Jose, an IDS5000 user.

IC PROBE. The IDS4000 consists of a work station controlling an electron beam that can probe inside an IC nondestructively and without affecting the circuit operation. That is exactly the way an oscilloscope can be used to probe a printed-circuit board. A test system applies stimulus to and receives stimulus from the chip being debugged.

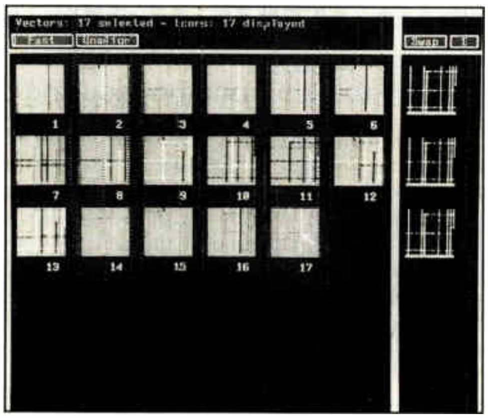
On the work-station CRT screen are software tools that display schematic, chip layout, and actual video images of the chip in windows. The work station allows the designer to quickly correlate a point in the schematic with a node on the chip itself. The electron beam allows him to probe the point and look at its waveform displayed in another window on the screen.

The designer looking for bugs is familiar with the chip's operation and can use that knowledge to isolate bugs, but in failure analysis engineers typically are not familiar with the operation of a chip. "Because we are an ASIC company, we have thousands of designs in the field," says Daniels. "We cannot be familiar with the logic function of every one of them."

That's where dynamic fault imaging comes in. By comparing the operation of a known good chip with that of a bad chip to pinpoint a problem, it eliminates the need to understand how a chip works. In dynamic fault imaging, the electron beam operates like a strobe light synchronized to the application of a test vector. As the vector is applied, the beam creates an image of the chip at the same instant.

The system takes a picture of a good chip when a vector is applied and compares it with a picture of the faulty chip with the same vector applied. "Then by subtracting on a pixel-by-pixel basis the failing image from the known good image, the system produces a difference image, which then shows where the failing node is on the device," says Christopher Talbot, staff marketing engineer at Schlumberger.

Because the good and faulty images are taken from two different chips, one of the tasks of the dynamic-fault-imaging software is to align the two before their images are subtracted. Also, it processes both images to reduce noise.



Window with a sequence of 17 images shows logic state of a device corresponding to each test vector.

During dynamic fault imaging, the system acquires a sequence of images from both the good and the faulty parts. This occurs at the time the fault is detected at the output pins and for several vectors backward in time (see figure). "The engineer can see from the images how a fault developed and propagated out toward the input/output pad where it is detected," Talbot says.

The sequence of images shows the logic state of a failing device for some 17 vectors. Each image is typically some smaller section of the chip. A white or black horizontal or vertical line indicates a logic 0 or 1 state at that point on the silicon. The engineer can examine the point with a scanning electron microscope to see the metal or oxide failure that causes the problem.

"Dynamic fault imaging will help us quickly find the failures," Daniels says. "In failure analysis, 80% of our time is spent trying to pinpoint where on the chip a failure has occurred. Using manual probing, you can spend anywhere from a week to a month trying to find a failure, especially if you do not know the logic of the chip. With DFI it takes a couple of days." *–Jonah McLeod*

FACTORY AUTOMATION

MAP IS FINALLY SETTLING DOWN TO BECOME A STANDARD

NEW YORK

It looks as if the Manufacturing Automation Protocol is finally ready to settle down and become a reliable standard. At least, some 50 exhibitors who will be hawking MAP products at the Enterprise Networking Event in Baltimore from June 5 to 9 think so. They point to a series of developments that are boosting acceptance of the factory-automation protocol.

First, MAP/TOP 3.0, the latest version of the protocol and its companion Technical Office Protocol, includes a stability statement intended to dispel fears that changes in MAP will render earlier versions incompatible with newer ones. Second, MAP's promoters promise that Version 3.0, unlike earlier versions, has undergone extensive conformance testing. Finally, and most important, MAP's protocols have been tied tightly to the Open Systems Interconnection model.

Some vendors are still taking a wait-and-see attitude before they commit themselves to building and selling MAP-compliant systems. Some users are equally wary about buying any such systems. But MAP's backers feel sure the doubters can be won over.

Those backers point out that the stability statement guarantees the vendors, essentially, that what they see in this edition of MAP is what they'll continue to get. The statement guarantees that no incompatible additions will be adopted for at least six years. "This means users will be able to buy products with the confidence they will get a reasonable lifetime out of them," says Robert Crowder, president of Ship Star Associates, a Newark, Del., consulting firm

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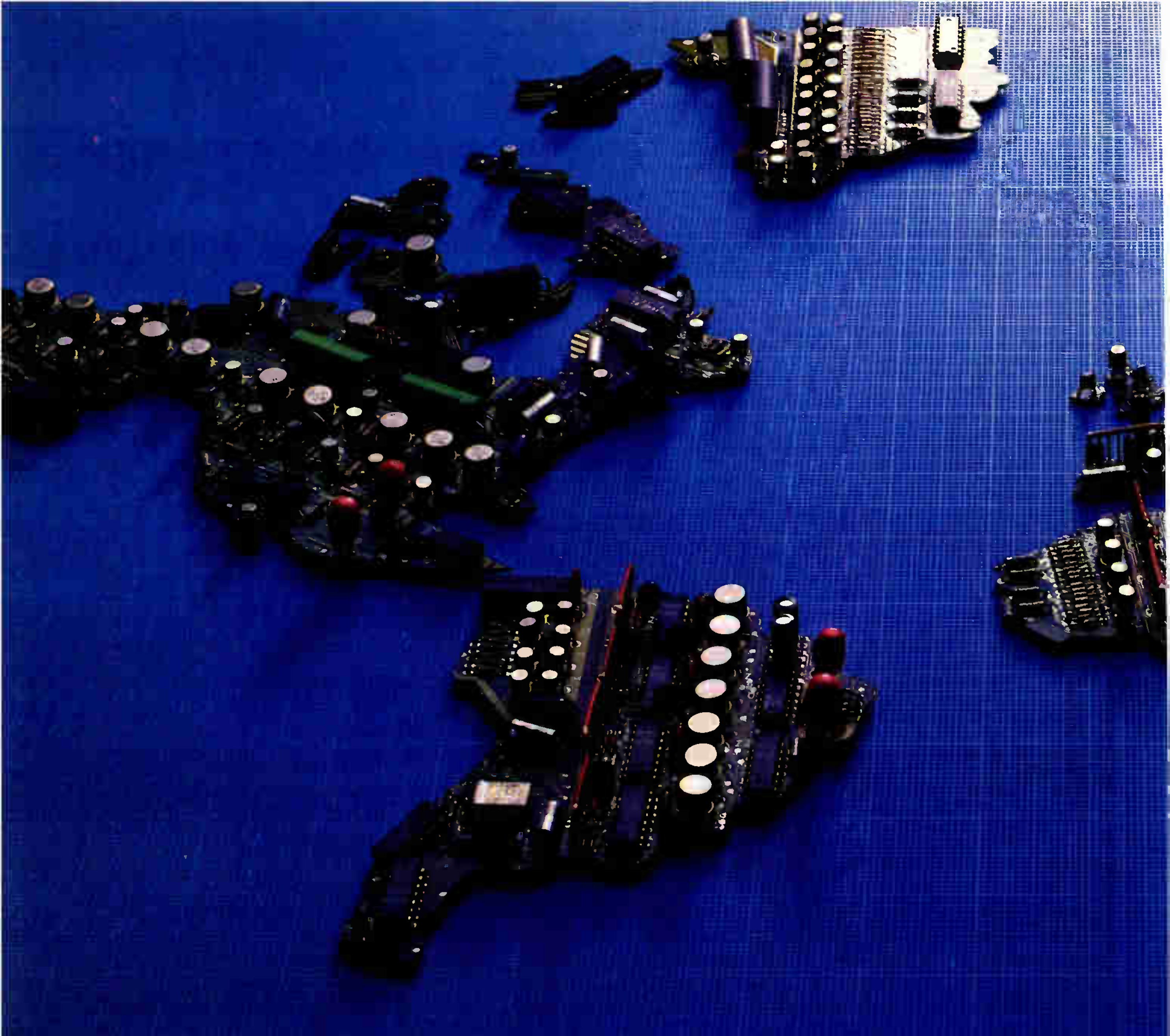

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that publishes technology reports focusing on MAP.

Furthermore, the MAP promoters say, the conformance testing that preceded and that will follow the Enterprise show should help convince vendors and factory-automation-product users to forget the painful experience of the 1985 Autofact show. At that show, prototype systems built around MAP/TOP Version 2.1 went on display, but then production versions bogged down in conformance testing and later were shunned by potential users—they saw Version 3.0 on the horizon and balked at installing a soon-to-be-obsolete system.

This time, Version 3.0 is undergoing a $20 million shakedown, says Charles J. Gardner, manager of Standards and Protocols for Eastman-Kodak Co. and chairman of the MAP/TOP Users Group Steering Committee. Half of the testing is being done by the Corporation for Open Systems and the other half by a European consortium, Standards Promotion Applications Group. The European input is particularly signficant; the major vendors all take a global perspective of the networking market.

However, neither the stability statement nor the conformance testing answers the biggest question the doubters have. That concerns OSI. While a dozen computer vendors endorsed OSI in a pre-Enterprise news conference May 4 [*Electronics*, May 12, 1988, p. 21], they pointedly omitted an endorsement of MAP/TOP. "The future of MAP is directly tied to its interoperability with OSI," says Linda Sanders, public relations manager for Digital Equipment Corp.'s Computer Integrated Manufacturing Market Group, Marlboro, Mass. "The further away it gets from OSI, the less viable it will be—that's DEC's position."

Recognizing that fact, the MAP/TOP Users Group has proclaimed its willingness to guide MAP and TOP by the OSI's seven-layer networking model. Nevertheless, questions remain about the stability of MAP's OSI connection. In particular, MAP/TOP Version 3.0 has enhanced its functionality in the OSI's network-management layer. But the OSI standard for the network-management layer is still incomplete, and there is no clear assurance that its final version will conform with MAP/TOP's implementation.

Not to worry, counters Gardner. MAP has taken a critical subset of OSI's incomplete network-management protocols "and filled in the voids where needed. We will follow up with a complementary version when the OSI standard becomes mature," he says, "but that won't be until 1992 or thereafter, and we don't want to wait that long." – *Jack Shandle*

MICROPROCESSORS

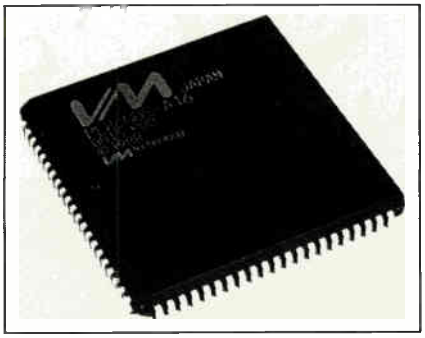
JAPAN'S PC MARKET GETS EVEN MESSIER

TSUKUBA, JAPAN

What happens when you add two new microprocessors to the already muddled Japanese MS-DOS computer marketplace? The answer is, an even worse mess.

The devices, from a startup called VM Technology Corp., are a powerhouse 32-bit version now offered as samples and a 16-bit device now being developed. Both use virtual-microprocessor technology architecture. But what promises to cause the consternation in the marketplace is the fact that the devices can replace any member of Intel Corp.'s 8086, 80286, and 80386 family or implement partial or full original instruction sets. The result may be that Intel will face lower-priced substitutes for its microprocessors that don't violate its copyrights—and that NEC Corp. will take a direct hit, as well.

NEC thought it was home free in its bid to take market share away from In-



Powerhouse microprocessor from Japan can replace devices from Intel and NEC.

tel with its new V33, a souped-up replacement for the 8086 [*Electronics*, April 14, 1988, p. 25]. Now it will have to contend with a V33 substitute that, among other things, is faster, handles more instructions, and boasts larger memory space.

The troublemakers are the 32-bit VM8600S and the 16-bit VM860S. At first, they probably will be used mostly as a way to economically upgrade systems that use Intel processors or NEC "enhanced" V-series versions of Intel processors—including both embedded applications and MS-DOS machines. Industry watchers speculate that devices might be sold to makers of AT-like computers for the U. S. market, some of whom—including the Hewlett-Packard Co.—use the V30 for XT clones.

SOLID BACKING. The new processors have a sound technical background and VM Technology has strong backing. The devices were developed under the supervision of Masatoshi Shima, developer of Intel's groundbreaking 4004 4-bit and 8080 8-bit processors. Shima later designed the more advanced Zilog Z80 8-bit and Z8000 16-bit processors. VM Technology is backed by Mitsui and Co., a giant general trading company, and also by the publishing and software house ASCII Ltd., whose president, Kazuhiko Nishi, has been a driving force in the popularization of personal computers in Japan.

The devices skirt copyright problems because they do not include microcode. Instead, their flexible architecture features hardwired instructions implemented in programmable logic arrays. Industry-standard instruction sets can be implemented without infringing on copyrighted microcode, and original instruction sets can be implemented as desired. VM Technology calls them application-specific integrated processors, because their instruction sets of 155 orthogonal instructions can be mixed with Intel instructions, and others can be implemented too.

Separate 16-bit data and 29-bit address buses make possible a memory cycle of only two clock cycles. For the same clock speed, up to the maximum rated 20 MHz, the VM8600S is estimated

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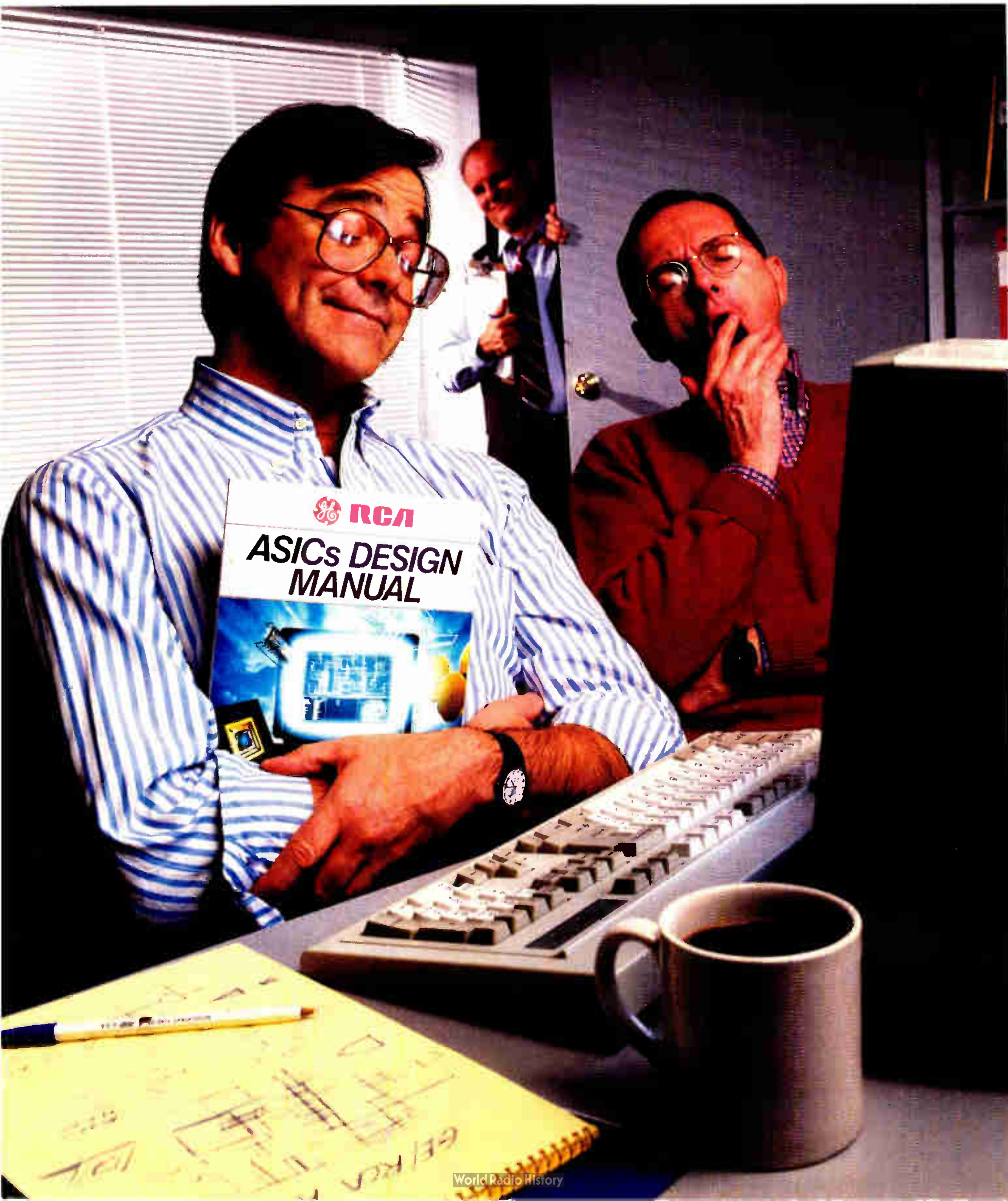

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to provide 1.3 times the processing performance of the 80286 and about 75% the performance of the 80386. But consider the lower cost: the initial sample price of the 860S will be only $240 in Japan, and prices should be much lower next year, when production reaches 100,000 devices per month.

Only real-mode applications are supported, but the majority of applications (other than Unix) available today only run in the real mode. Besides the segment and offset addresses of the 8086 that extend only to 1 Mbit, the VM8600S can also provide 4 gigabytes of linear addressing. Physical memory is 512 Mbytes.

The processor is implemented in 1.2-μm CMOS technology for high-speed and low-power operation, as well as small chip size. It features a total of 32 separate 32-bit general-purpose registers. In addition to hardwired logic, pipelined hardware further increases the execution speed. *–Charles L. Cohen*

SEMICONDUCTORS

SEMATECH SHIFTS INTO HIGH AS CASH STARTS FLOWING

WASHINGTON

Now the money should flow. Sematech finally has its memorandum of understanding with the Pentagon, and that clears the way for the U. S. chip industry's manufacturing research consortium to get the $100 million it was promised in the 1988 federal budget. But delays caused by changing plans, the lack of executive leadership, and fiscal uncertainty have eclipsed Sematech's original goal of producing first silicon in 1988. The challenge now is to get the program rolling.

Sematech's fortunes have ridden with the tides. All of its Christmas 1987 goals—attracting 30 member companies, hiring a chief executive officer, choosing a plant site, and assuring federal support—were unmet. Since then, it has selected a site in Austin, Texas, and now has its money. But it still has only 14 members and no chief executive. In fact, at least two candidates for the post declined the position. And to top off a difficult winter, the DOD switched responsibility for Sematech from its Office of Science and Technology to the Defense Advanced Research Projects Agency.

That rattled Sematech officials because of Darpa's reputation as a specialty house experienced in handling advanced research, not short-term manufacturing development. "Initially we were dismayed," says Clark McFadden, a partner at Dewey, Ballentine, Bushby, Palmer & Wood, the Washington law firm that helped draw up the agreement between Darpa and Sematech.

"We were very leary," adds Sanford Kane, an IBM Corp. vice president and chairman of Sematech's executive committee. "But those fears were allayed after our first discussions with Darpa." However, Darpa did insist on changes. "They wanted to be certain that we were focused not just on tomorrow's plans, but on those plans beyond tomorrow. They wanted a roadmap for the future," Kane says. "For instance, we had a pretty good idea of what we were going to do in ion implantation to improve present equipment, and of what we would need in the next generation of equipment. But we really hadn't given much thought to what we would want beyond that. Darpa made us look at that more closely, which is good."

Kane adds that fears that Darpa might try to micromanage the program are unfounded; rather, it will be treated as a member company. Darpa will not get a seat on Sematech's board and will not have veto power.

But there could be one problem: the Pentagon will be able to transfer Sematech technology to nonmembers doing defense work. They will be barred from using the technology in commercial products, but Kane admits it will be difficult to police such use.

All that aside, Sematech still has a long way to go before any technology is pumped out of its facility. The clean room, already under construction, won't be complete until October and a chief executive may not be hired until summer. But with the first $15 million payment on its fiscal 1988 federal money due immediately—and assurances that fiscal 1989 funding is all but assured—Sematech officials are now recruiting new members, and getting current members to live up to their financial commitments. Its deal with Darpa states that federal funds cannot be released until matching member funding is already in hand. *–Tobias Naegele*

CONSUMER

PLAY IT AGAIN, SAM: DAT IS STILL DELAYED

CHICAGO

It's a story that's beginning to sound more like a warped record than one chronicling the emergence of a hot new consumer audio technology. First a development appears that favors the introduction of play-and-record digital audio tape units in the U. S. consumer market. Then something happens that points toward even longer delays. DAT is already being sold to consumers in Japan and Europe. But as the Summer Consumer Electronics Show in Chicago approaches, most industry watchers are betting against DAT's chances for a U. S. marketing rollout at the June 4–7 show.

Harman America Electronics, for one, is getting a taste of the frustration. The Woodbury, N. Y., firm has been forced to put its June introduction plans on indefinite hold, because it can't get components.

Likewise, Marantz Co., Chatsworth, Calif., has been promising U. S. deliveries of its DT-84 DAT home deck for a year, but has been unable to get parts. And Casio Inc.'s plans to market its DAT-1 portable player/recorder in April here were apparently waylaid when its Japanese parent abruptly decided to delay U. S. shipments.

The major hangup remains objections to DAT by the record industry, which fears that the high-quality copies could lead to widespread unauthorized DAT reproduction of copyrighted records, analog tapes, and compact disks.But the Electronics Industries Association's Consumer Electronics Group is trying to speed the process. Last month it established a six-figure matching legal defense fund to be available to the first member company to be sued over marketing DAT recorders here.

CAR PLAYERS. Meanwhile, DAT is beginning to make inroads here in the form of play-only units for automobiles that don't run afoul of record-industry objections. Initial car DAT players have been shipped by at least three firms: Alpine Electronics of America, Torrance, Calif.; Clarion Corp. of America, Lawndale, Calif.; and Kenwood Electronics, Long Beach, Calif.

Also, Ford Motor Co. is ready to provide Sony DAT players as a $2,000 option on some 1988 Lincoln Continentals in June. And General Motors Corp.'s Delco Electronics Corp. unit this month said it has DAT players available for optional installation. *–Wesley R. Iversen*

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PROBING THE NEWS

THE EIGHT-INCH WAFER CASTS ITS SHADOW OVER SEMICON WEST

Large wafers—and the move to islands-of-automation production—are hot issues

The problems of working with very large, 8-in. wafers and the accelerating move from in-line semiconductor production to islands of automation will be major topics for discussion at Semicon West starting May 24 in San Mateo, Calif.

At a session called "Beyond six-inch wafer technology," one of the six papers to be presented will predict that the early movement to large wafers will be for production of dynamic random-access memories, where large wafer sizes will reduce costs and increase productivity. That's the conclusion of a study by Robert E. McGeary, director of semiconductor equipment at Dataquest Inc., the San Jose, Calif., market research firm. He also says suppliers of application-specific integrated circuits may have to participate in the movement to large wafers, depending on how quickly their foundries utilize them. However, the Dataquest study shows that 8-in. (200-mm) wafers will achieve only minor market penetration even by 1991. Their adoption will be inhibited by the large capital investment required, coupled with the reluctance to abandon current capacity (see fig. 1).

Nevertheless, the technology has its believers. Prasad Nevrekar and Alan Levine of Ultratech Stepper Inc., Santa Clara, Calif., in their analysis of step-and-repeat lithography requirements for 200-mm wafer processing, say that the advent of large chip sizes will hasten the movement to 200-mm wafers. For example, at the projected chip sizes of the 16- and 64-Mbit DRAMs, the usable area of a 125-mm wafer will only be around 60%; while 80% of the area of a 200-mm wafer should be usable.

For successful production of 150-mm and larger wafers, Nevrekar and Levine recommend the use of a photolithography tool with site-by-site alignment, site-by-site focusing, and site-by-site leveling to yield tighter registration tolerances, better critical-dimension control, and improved productivity. They add that a 1:1 lens with broadband spectral correction nearly eliminates the effect of standing waves and provides extremely uniform imaging over large chips and wafer sizes.

Perhaps no one can testify with more authority on the problems of starting up in 8-in. wafer production than IBM Corp. Its experience with the introduction of 200-mm wafer production to the IBM General Technology Division, Essex Junction, Vt., begun in 1984, will be described by George E. Thyng and George G. Collins.

At that time, no vendor was capable of supplying 200-mm wafers, so IBM's silicon manufacturing products group in East Fishkill, N. Y., was asked to develop and supply them. Initial processing was begun on the first delivered wafers in May 1984 while an on-site feasibility line was being constructed.

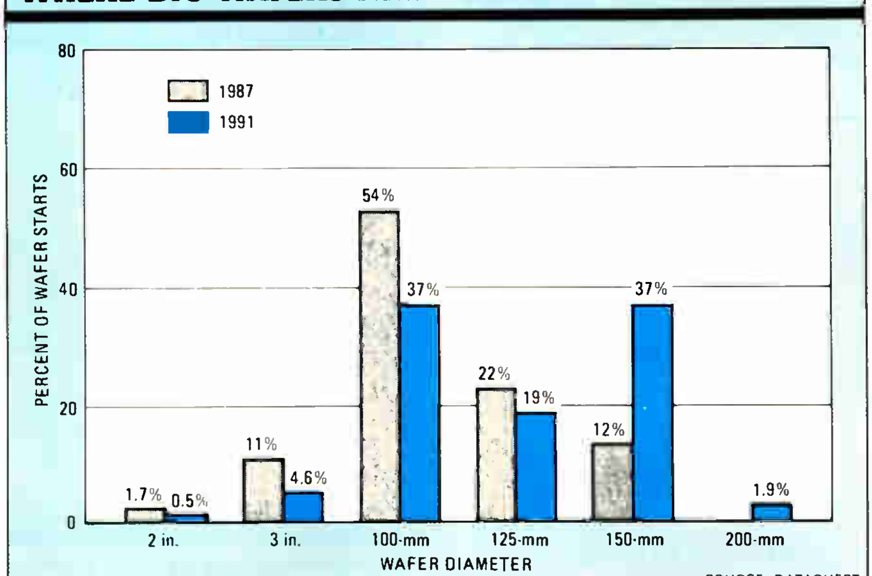
By 1985, the feasibility line was producing 64-Kbit RAMs to demonstrate parametric control and some defect learning on the 200-mm format. By 1986, the feasibility line was converted to the 1-Mbit process and the initial production tool set was defined for the manufacturing line. Manufacturing tool installation and debugging began in January 1987, followed by engineering wafer starts in June. Normal production commenced in January 1988.

The actual facility was built into an existing structure adjacent to a 125-mm line. The new line is a modified vertical laminar-flow facility capable of manufacturing two generations of product and piloting a third with some required upgrade. There was considerable focus on cutting contamination for the site, tools, and facility. For example, gases of the highest purity available were used along with low-particulate chemicals. Where it was consistent with tool architecture, through-the-wall installations were built. To hold down the introduction of tool-based particulates, certain equipments were required to be single-wafer units with manual cassette-to-cassette-transfer while others used robotics for wafer handling.

A major effort by both IBM and its vendors was required for debugging this added automation. In many cases, the level of software complexity had been underestimated. Fixing these problems delayed the learning process needed to mature the 1-Mbit memory line. To circumvent this problem, machines were run in a semiautomatic mode and the feasibility line was left in place longer than planned to gain experience on the new process.

In an unusual paper that departs

WHERE BIG WAFERS ARE HEADED



SOURCE: DATAQUEST

from the 200-mm-wafer tone of the session, lithography as applied to large areas of material other than silicon gets special attention from a group of scientists from Xerox's Palo Alto Research Center. They will describe progress in lithography for large-area electronic devices such as active matrix liquid-crystal displays and linear arrays of amorphous silicon thin-film transistors as applied to page-wide print heads and document-scanning sensor arrays. Such devices typically measure 200 mm on a side as compared with a typical VLSI chip that is 10 mm on a side.

Unlike silicon wafers, large-area substrates do not come in standard sizes. This nonstandardization makes it impossible to buy equipment without a certain amount of costly customization.

Early large-area lithography (with typical 15-μm details) relied on contact printing and suffered from the limitations of this technique, which include finite mask lifetime, resist cracking, overlay errors, and poor yield. To eliminate these problems, Xerox went to a 1:1 stepper with a light-source wavelength of 436 nm, a numerical aperture of 0.08, and a field diameter size of 106 mm. This system was capable of 4-μm design rules.

Even with this very large field diameter, large-area devices cannot be completely covered in a single exposure, so seamless stitching of several exposure fields is required.

Using stepper lithography, manual coating, and wet processing, Xerox's researchers were able to reproduce 3.2-μm feature sizes on their large-area substrates. In the future, Xerox would like to reproduce in the neighborhood of 2-μm resolution on large-area substrates.

And another session, called "In-line vs. islands of automation," comprising seven papers, clearly indicates that the pendulum is swinging away from conveyor-belt-type production lines to islands of automation—stand-alone automated pieces of semiconductor-processing stations.

Phil Stapelton of Intel Corp., Chandler, Ariz., and Wouter Verwoerd of ASM-FiCO, the Netherlands, compare the relative advantages of the two automation methods when applied to IC assembly. They note that in-line automation offers the advantages of relatively simple mechanical interfaces with low system throughput time, absolute control over work in process inventories, and minimal work in progress in the system. But, they say, in-line automation is rigid in terms of line-balance flexibility, adjusting to process flow deviations, and changing package types.

Islands of automation, on the other hand, offer flexibility of line balance and process-flow deviations have minimal impact. However, system cost is typically higher.

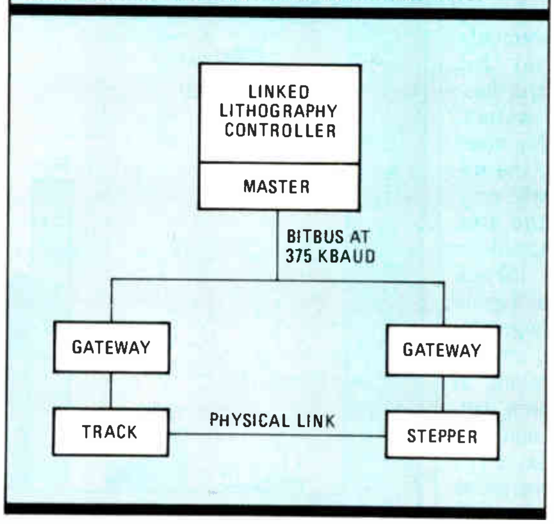
Ellen Long of CIMCORP Inc., Aurora, Ill., also emphasizes the importance of flexibility. She points out that the amount of time required for new products to go from design to production is shrinking, so lines must be able to change over quickly from product to product. In addition, there is pressure to get products into production faster to be first on the market. The demand for fast changeovers and the push to get to market both call for the flexibility of the island-of-automation approach rather than the dedicated in-line method, which is expensive and which cannot be modified easily.

Charles Bayliss of Bayliss Automation Inc., Scotts Valley, Calif., and Stanley Chin of Semiconductor Systems Inc., Fremont, Calif., describe an approach that reconciles both techniques. It's an island-of-automation line built with standard components that can be made to look like an in-line system, yet retain the flexibility of the stand-alone automation approach.

The system is a linked-lithography station consisting of a photoresist coater/developer track that is physically linked to a step-and-repeat lithography system (either a Nikon reduction stepper or an Ultratech 1:1 stepper). All three machines can be controlled by a special station controller through a distributed-processing network.

The linked-lithography controller (see fig. 2) uses a 386-based IBM PC or compatible connected to the production

PRODUCTION CONNECTIONS



The linked-lithography controller is based on an IBM PC linked to equipment via a communications network.

equipment via the network. The PC contains a Bitbus (a network developed by Intel for industrial control) interface card. The PC acts as the operator interface through the Bitbus to two gateways, one for the track and one for the stepper.

The gateways serve a dual function as both a SECS communication protocol—which was developed by the Semiconductor Equipment and Materials Institute Inc.—connecting to the equipment, and as a means of executing the control programs to operate the equipment. The gateways can be configured for use with protocols other than SECS and can also provide direct analog and digital input/output for equipment with no serial communication interface. The system can be expanded by adding gateways.

With this system, one operator controls three process steps from one station, the IBM PC providing a central status display and control point. This reduces the number of decisions required of the operator during routine processing. In the future, the authors predict, CAM systems will communicate with the station controller via an interface to the DOS file server. The CAM system will initially augment and eventually replace the operator interface program in the station controller.

Another paper covers a different application of the PC and the SECS protocol. Peter Byrne, Bitstream Inc., Belmont, Calif., and Karl Heiman, Lam Research Corp., Fremont, Calif., discuss "Equipment analysis with the SECS protocol and personal computers." Today, the authors note, practically all semiconductor-processing equipment has an embedded microprocessor constantly monitoring sensors that are watching critical parameters. Getting the data already in the memory of the embedded microcomputer consumes many hours and is often done by connecting external sensors to the equipment. A more natural path is to ask the embedded microcomputer for its data over a serial connection through the SECS protocol.

Until now, mainframes or minicomputers have been used to get access to the data. However, the main task of these computers is to keep track of work in progress; the added work of tracking multiple sensors strains the capacity of these computers.

An alternative is a dedicated personal computer connected to a piece of processing equipment. With a PC, one can obtain sampling frequencies limited by the serial channel, SECS overhead, or equipment response. The authors found that about 10 parameters can be monitored three times every second using the SECS protocol.

—Jerry Lyman

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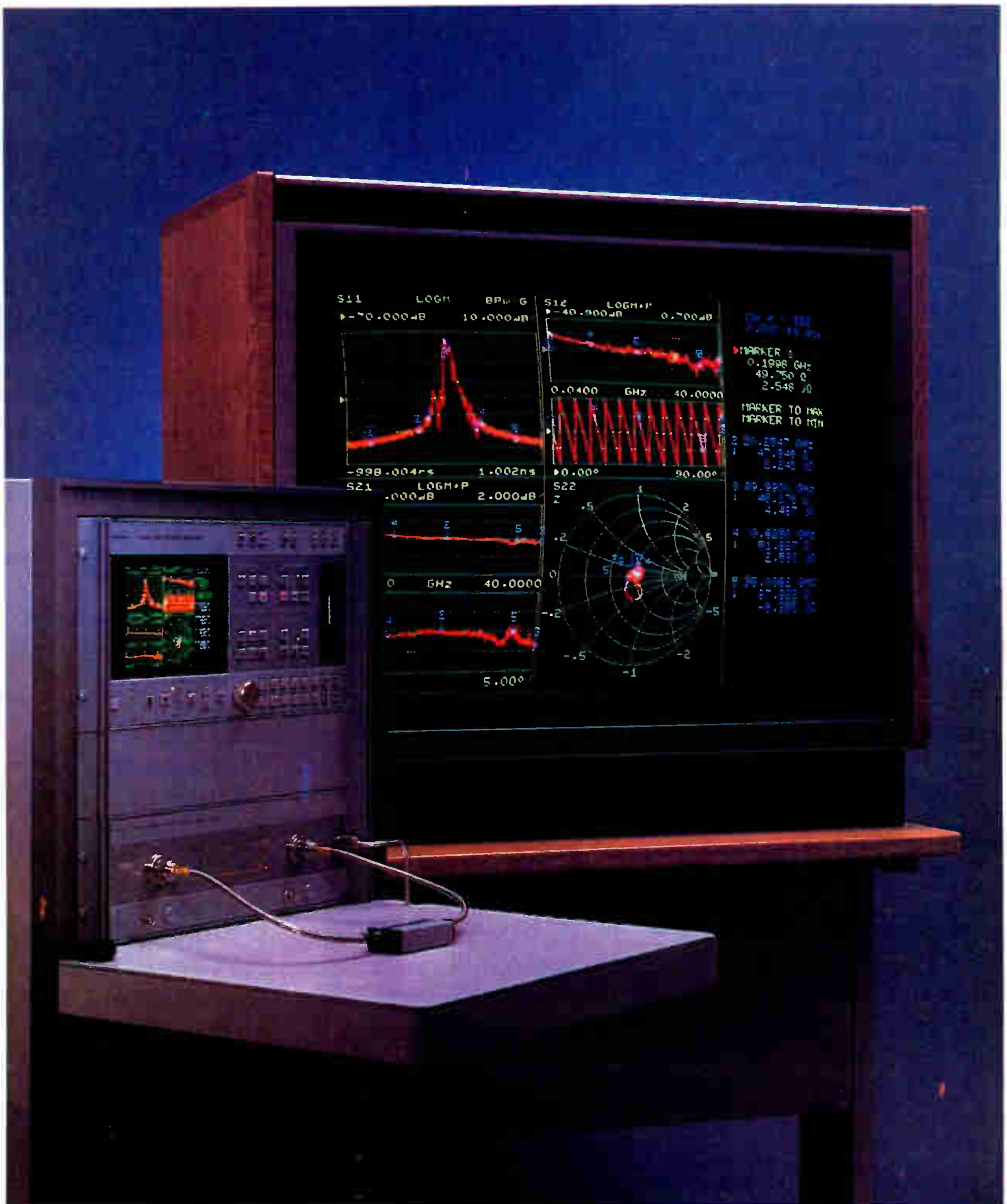

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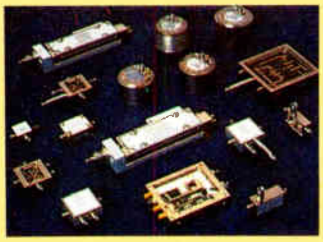
Using our Calibration and Verification Kits, you can make error-corrected, NBS traceable measurements.

Measure with confidence over a truly usable 130 dB range.

Automatic electronic reversing lets you save time measuring the DUT.

Errors are minimized through automatic setting of the correct electrical delay compensation.

By selecting N discrete, non-sequential test frequencies, you can make frequency hopping tests.



Exclusively among all vector network analyzers, the Wiltron 360 displays four characteristics simultaneously in full color. That feature in itself would be reason enough to choose the 360.

Actually, it's only one of the many step-ahead features and user benefits to give you new pleasure and confidence in making network analyzer measurements.

A Unique Marker Sweep.

Your measurements can now be as simple as selecting a broadband sweep, moving markers to bracket key characteristics, and initiating the data taking process. Limit lines identify and display frequencies at go/no-go performance points. You can make a yes or no decision at a glance.

Uninterrupted Measurements.

An external plotter or printer gives you a record of test parameters and data. Productivity soars as a buffer memory prints out results while you are continuing to make further tests.

Single Calibration.

Because the 360 automatically maintains itself in calibration as the number of measurement points or frequency range is changed, test results flow without interruption.

Single System Adequacy.

Wiltron's 360 gives you all the test and measurement capability you need. Measure phase, magnitude, complex values, time or distance domain, and group delay. Results are always provided in 12-term, error-corrected data at phase-locked test frequencies.

Eminently Affordable.

You'll be pleasantly surprised at the price of Wiltron 360 systems. They're probably about 20 percent less than you would expect to pay for all this performance.

For more information, please address Wiltron Co., 490 Jarvis Drive, Morgan Hill, CA 95037-2809. Phone (408) 778-2000. FAX (408) 778-0239.

WILTRON

Circle 49 on reader service card

INTERNATIONAL NEWSLETTER

NEURAL NETWORK GIVES NEC A BRAINY CHARACTER-RECOGNITION SYSTEM

High-performance character-recognition systems may start turning up in a year or so on personal computers and work stations from NEC Corp. The Tokyo firm reports its new recognition equipment—based on neural-network technology that apes the organization of neurons in the human brain—can identify 62 alphanumeric characters printed by dot-matrix printers, with an accuracy of more than 99.8%. Conventional character-recognition systems are accurate only 98.5% of the time. The improvement in NEC's new system stems from a repeated-character-learning method, called a back-propagation learning algorithm. The neural network checks characters and corrects them, if necessary, before the character is output by the system. □

UK COMPANIES PRESS ON WITH CT2 CORDLESS-TELEPHONE STANDARD

British firms whose embryonic CT2 standard for second-generation digital cordless telephones failed to win pan-European acceptance still hope they can convince the Council of the European Communities to accept it as a Norme Européenne pour Télécommunications—a European telecommunications standard. Seven equipment manufacturers and would-be operators of the new service will get together to draw up detailed specifications such as signaling protocols and adjacent-channel interference levels. There is broad agreement already on general specifications: 40 channels 100-kHz wide have been allocated in the 864- to 868-MHz bands in the UK for the service. The group expects that details can be ironed out in time for a new standard to be submitted to the EC council well before 1992. By then, industry observers estimate that the market demand could be higher than 2 million CT2 telephones in the UK alone, with some 600 base stations serving the London area. The phones would cost about £200 each; the base stations, £1,500 each. □

SUMMER SAMPLING SET FOR JAPAN'S 32-BIT TRON FAMILY

Japanese microcomputer makers can now plan to market 32-bit engines based on a native Japanese architecture—TRON, the real-time operating-system nucleus. In July, Hitachi Ltd., which developed the first TRON chip [*Electronics,* Jan. 21, 1988, p. 31], Fujitsu Ltd., and Mitsubishi Electric Corp. will offer samples of the processor for about $1,150. Peripheral integrated circuits such as a direct memory-access controller, a high-speed tag memory, and an interrupt controller will be ready at the same time. Fabricated in 1.0-μm CMOS, the 20-MHz version of the microprocessor runs at 7 million instructions/s, nearly one-and-a-half times the performance of Intel Corp.'s 80386. Mass production is scheduled to begin in December; there are no plans at present to market the chips in overseas markets. □

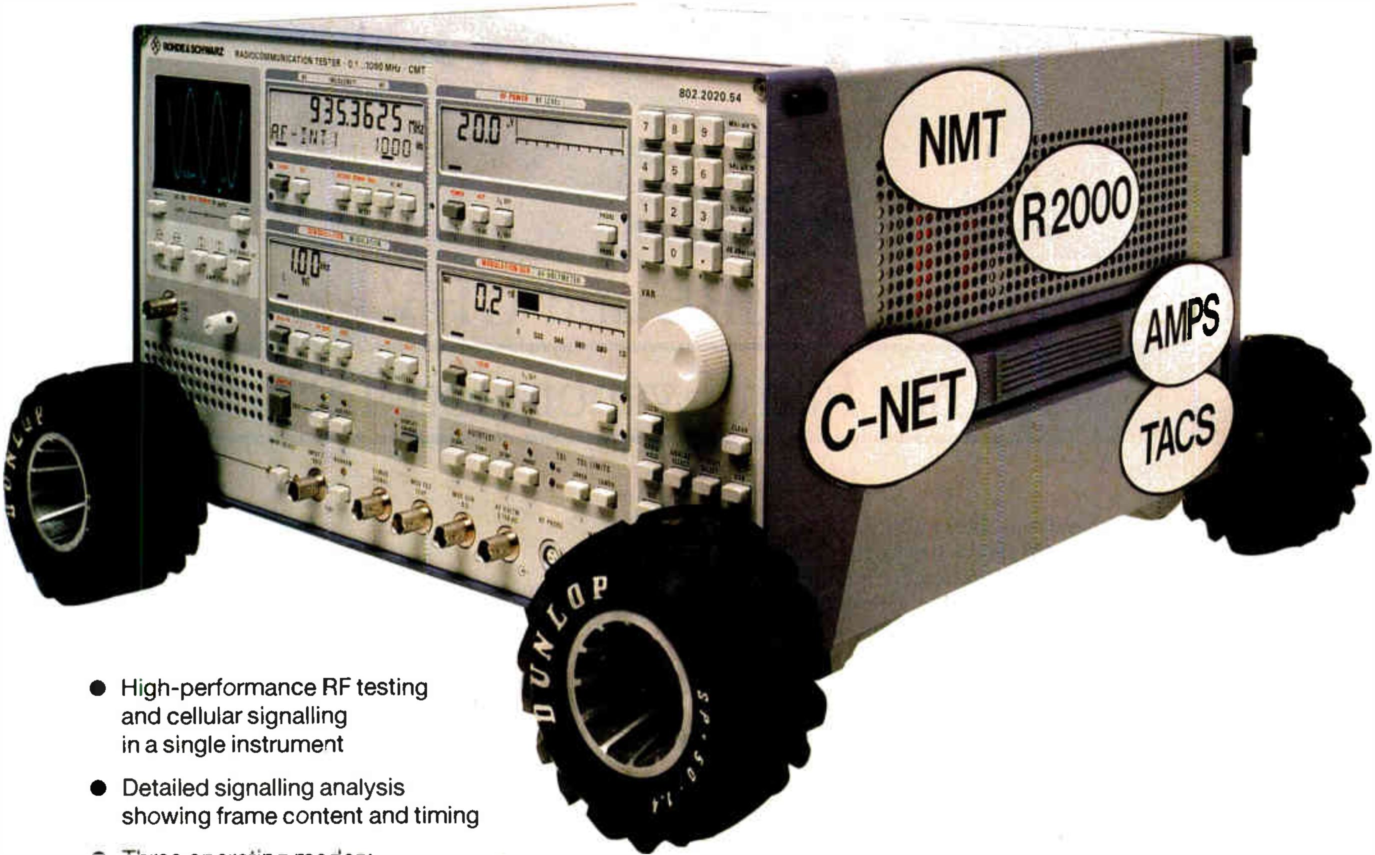
GERMANY'S COMPUTER-VISION AUTO TAKES A ROAD TEST

West Germany's experimental autopilot car is hitting the road: in recent tests on public roads over stretches of more than 12 miles, the "Autonomobile" got up to 60 miles an hour, changed lanes, passed cars, and avoided obstacles—all without a human at the wheel. Under development at the Armed Forces University in Munich [*Electronics,* July 24, 1986, p. 50], the autonomous vehicle is built around a real-time image-processing computer that uses the input from two road- and traffic-scanning video cameras to calculate and generate the signals for the vehicle's steering, throttle, and braking systems. The long-range goal is to develop an autopilot that can relieve a human driver during arduous trips or warn him of critical traffic situations. □

Cellular Mobile Testing

CMT

Radiocommunication Tester CMT
New models handle international cellular networks:
NMT, C-Net, Radiocom 2000, AMPS, TACS



- High-performance RF testing and cellular signalling in a single instrument
- Detailed signalling analysis showing frame content and timing
- Three operating modes:
  Menu-guided manual testing
  Versatile autorun test sequences with printer protocol
  IEEE-bus interface

Ask for details on
CMT Cellular Models

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Federal Republic of Germany
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ROHDE & SCHWARZ

Circle 110 on reader service card

INTERNATIONAL WEEK

SONY EYES EUROPE'S LASER DISK MARKET

Look for Sony Corp. to be marketing a laser disk player to European consumers by August. The product will be a three-in-one type capable of playing all disks in the video and audio optical-disk family, which consists of laser disk, compact disk, and compact disk with video. The Tokyo company will sell two models, the same models that have been sold in the domestic market and will be released in the U.S. this month. Prior to Sony's entry, Pioneer Electronic Corp, Tokyo, has been selling three-in-one type players in the U.S. and Europe at a rate of more than 2,000 units a month since last year.

GROUPE BULL UNVEILS 10 UNIX COMPUTERS

Groupe Bull is attempting to broaden its product offerings with 10 new Unix-based computer models including multifunction work stations, high-end work stations, high-end servers and fault-tolerant systems. The four families—Bull DPX 1000, 2000, 3000, and 5000—target three major markets: departmental data processing in large companies and organizations; business processing in small and medium-sized companies; and scientific and technical processing. All 10 run under the company's SPIX operating system and are fully compatible with the X/Open Group's interface standards. Depending on model and configuration, prices range from 50,000 to 1 million French francs.

OPTOCOUPLER LIFE NOW MORE ACCURATE

Quality control engineers at Siemens AG's components group in Munich have developed a controlled burn-in method for optocouplers that allows their operating behavior to be predicted with greater accuracy and their lifetime to be forecast for longer periods. The new method measures the coupling factor both before and after the burn-in. Being more precise on forecasting lifetimes results in cost savings because optocouplers in plastic packages can now be safely qualified for applications where thus far only metal packages were specified. Siemens has developed the burn-in equipment for use not only in the laboratory but also for volume production.

10% GROWTH SEEN FOR PC-BOARD SALES

The world's 7,000 printed-circuit-board makers, who together employ some 200,000 workers, did $15.5 billion worth of business last year, and global annual sales are predicted to rise 10% annually at least through 1995. The figures came to light at the Printed-Circuit Board '88 conference staged by the Association of German Engineers. The leading European pc board maker is West Germany. Its $1.3 billion in sales also ranked it third globally.

SHARP TO BUILD PLANT IN WALES

Sharp Corporation of Osaka will build an electronic components and piece-parts production plant in the UK at a reported cost of £3 million. To be located at Wrexham in North Wales, it will be operated by Sharp's Precision Machinery Division and will manufacture small parts for consumer electronic equipment and automobiles. Sharp already has a manufacturing facility in Wrexham, producing microwave ovens, domestic video equipment and electronic typewriters.

HERE'S A ROBOT WITH A SOFT TOUCH

Robots will be getting a decidedly more gentle image now that Toshiba Corp. has developed a prototype to tend young plants at automated plant factories. The five-axis, multijoint robot uses a soft gripper that exerts a force of only 3 grams. A laser beam and sensor determine the position of the young plants on culture medium. The prototype is the world's first robot that can cut plant stems into proper sizes and transplant them all unaided in about 20 seconds.

FRENCH CENTER AIMS TO SPEED ISDN'S PACE

France's government-run Centre National d'Etudes des Telecommunications is hoping to speed the acceptance of Integrated Services Digital Networks with the creation of a new research center in Lannion, France. The research facility will concentrate on improving the S interface, which is the standard interface needed for users to plug into ISDN's 64 Kbit/s basic rate service. The center will offer measuring methods, simulators, and access to different networks in order to allow selected industry representatives to run tests needed to perfect future new products.

SUN SETS ON UK TELECOM EMPIRE

British Telecom's last monopoly over telephone equipment—pay phones—has finally been broken by the British Telecommunications Office, a move that opens the flood gate of competition. The first company to submit a pay phone for approval under the new scheme is the UK subsidiary of the U.S. company Southwestern Bell. The phone has already won an award for good design by the British Design Council and will sell for £215 through multiple retailers and specialized phone shops.

SIEMENS' ISDN SWITCH DOUBLES IN SALES

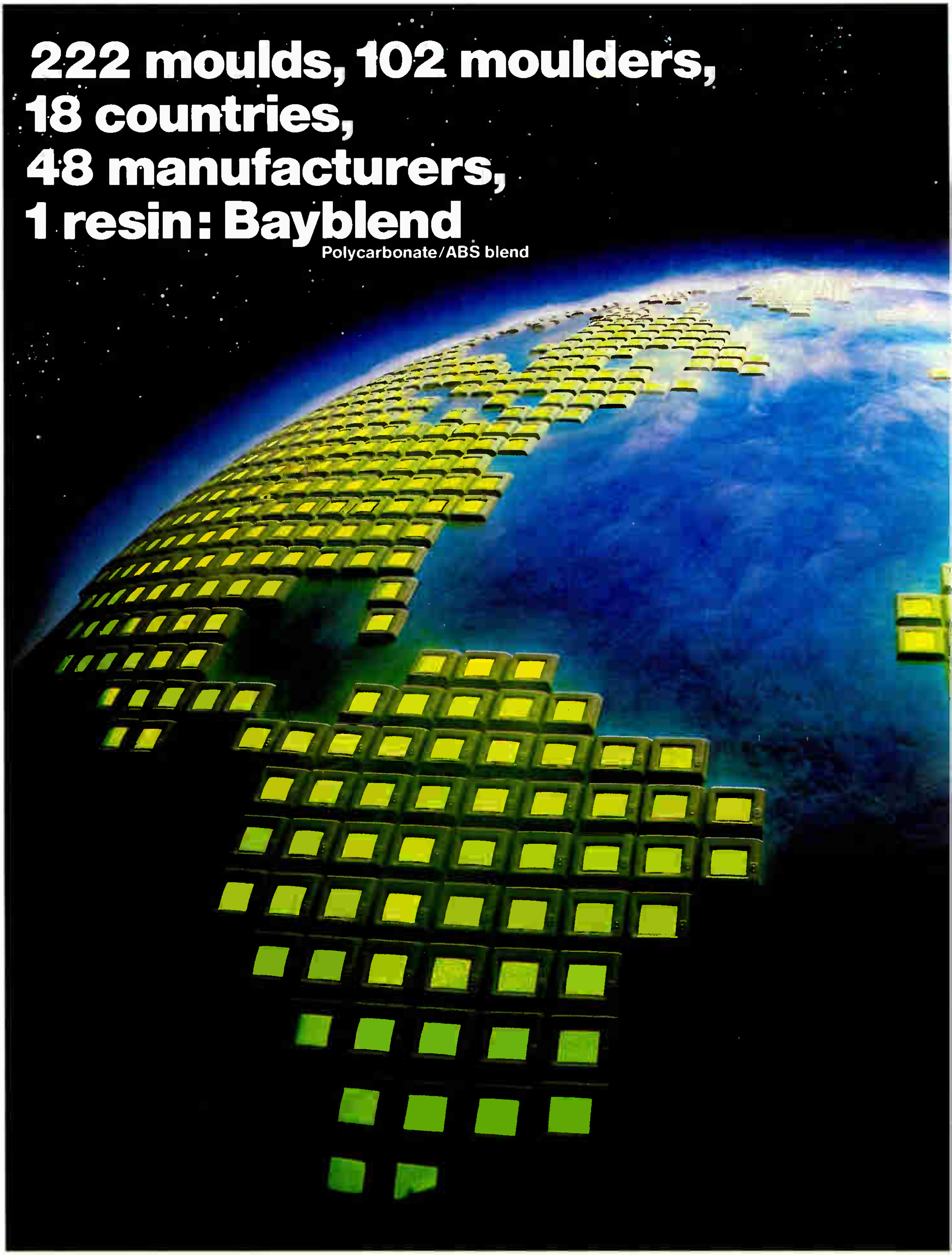
Siemens AG expects sales of its Hicom switch for private Integrated Services Digital Networks to double this year from last year's volume of $120 million. That makes the Hicom switch one of the Munich firm's hottest selling communication systems, with quarter-to-quarter gains of around 20%. In the past two years, Siemens has bagged orders for about 3,000 Hicom systems, with 2,000 already installed. Hicom, the company says, is the world's first ISDN communication system for nonpublic use that conforms to CCITT standards.

JAPAN TO UPGRADE COMPUTER SECURITY

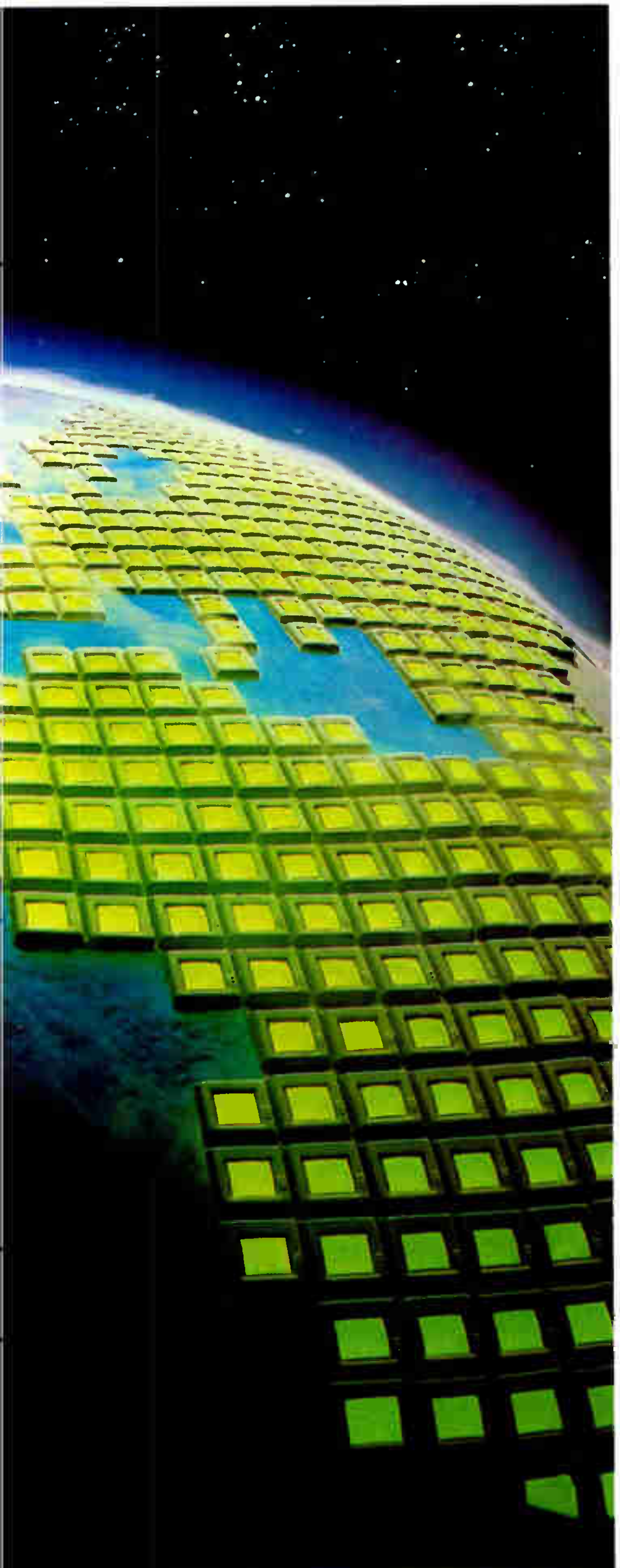
In response to growing concern over computer security, Japan's Ministry of International Trade and Industry is considering establishing an organization to guard against hackers and leakage. MITI will ask to establish the organization in fiscal 1989, which starts April 1, 1989. The organization will study computer security measures, facilitate the growth of a new industry to check the security of computer systems, and disseminate a list of names of specialists who pass MITI's data-processing system checkers examination.

AEG EXPANDS ITS COMPONENTS HOLDING

AEG AG is casting an acquisitive eye in the direction of Telefunken Electronic GmbH, a leading European components producer. AEG wants to buy out United Technologies Corp.'s 49% share in the Heilbronn, West Germany, company. AEG already owns 49% of TEG; the remaining 2% is held by a German investment house. Hartford, Conn.-based United Technologies favors the divestiture because it is in line with the company's overall policy of getting out of the electronic components business. TEG employs 6,000 people and rang up $360 million in 1987 sales.



* Tektronix is a registered trademark of Tektronix, Inc.



Many of the largest business machine makers in the world specify Bayblend FR 1439-1440-1441 resins.

From Singapore to San Francisco to Stuttgart business machine giants like Tektronix*, Hewlett-Packard, Bull-Transac, Nixdorf, CPT, and Ricoh are using Bayblend FR (Flame Retardant) 1439-1440-1441 resins. For keyboards, printer covers, CRT housings, bezels, typewriter housings, copiers and plotters. Making it one of the most utilized resins in the world.

Excellent processability

Bayblend FR 1439-1440-1441 are new generation resins characterized by excellent melt stability, easy flow and a wide processing window. Perfect for intricate housings and parts with long flow length requirements.

Inherent colour stability

The Bayblend FR 1439-1440-1441 series represents new technology in resins. They are colour-stable resins that meet the rigid requirements of business machine OEMs. They resist colour ageing for years even under repeated exposure to indoor light.

No plate out or bloom

Plate out can cause a slowdown in production. Bloom can accelerate corrosion and degradation of sensitive electronic parts. These new generation resins are free of plate out or bloom, eliminating expensive mould cleaning steps and giving moulders a big production plus. This also results in a reduction of electronic breakdowns giving OEMs a performance plus.

Bayblend FR 1439-1440-1441 series resins. A world of uses from each resin. For more information write

Bayer AG, Plastics Business Group
D 5090 Leverkusen, Bayerwerk

Bayer BAYER

KU 3979 C

Circle 112 on reader service card

M. L. & S.

THE MESSAGE.

When it comes to quality, our semiconductors and components speak for themselves. And that's not all. There's a broad spectrum of products to choose from and you're guaranteed economy of use.

Reliable low cost laser modules in various packages. An impressive choise of ready-to-build-in components.

wave length	*λ_p780, 1300, 1550nm*
output power	*P_{out} 0.1 to 4mW*
Package	*Pigtail, DIP, Butterfly, FC, SMA Connector.*

FU43SLD-2
P_{out} 0.1mW,
1300nm,
Single Mode

Easy-to-adapt GaAs FETs and HEMTs. Here is a splendid example from our wide range for K-Band:

MGF-K37V-4045:
P_{out} 37dBm at
14 - 14.5 GHz,
ηadd 30%

Versatile cross-point switches. 4 x 4 oder 4 x 8 versions featuring fast switching speeds and high reliability.

EPROMs in different organizations. Also in CMOS. Memory sizes from 64Kbit to 2Mbit. An attractive feature of these EPROMs is their short access time (min. 85ns).

Chip Cards with big memory capacity. As outer memory or debit and credit cards for multi-function telephone systems or telefax/telephone combination. Package-on-board technology and buffered interface circuits ensure the highest degree of reliability and quality. Memory capacity of up to 512KByte, soon even available up to 2MByte.

Fast HC and HC-1 CMOS Logics with improved performance characteristics. A wide product range covering all popular functions.
Available in DIL and SO packages.

	HCMOS	*HC-1*
FAN-out	*6mA$_{max}$*	*24mA$_{max}$*
Speed	*11ns*	*8ns*
Functions	*115types*	*32 + 32types*
SO package	*yes*	*yes*

ASSP CMOS microcomputer family with over 10 peripheral functions such as keyboard-scanning, speech recording, phone number storage, UART, A/D and DTMF functions. A family including 50 various Single Chips.

M50932 8-bit μC:
8KByte ROM and
512Byte RAM. On chip:
LCD driver (128 segments),
Clock and Stop functions
V_{CC} = 2.7 to 5.5V

All reset functions now on one chip. This novel Mitsubishi IC family is available for a wide supply voltage range from 2 to 17V in various space-saving packages.

SRAMs and SRAM Modules in CMOS. With shortest access times of 15ns. For high-capacity cache memory.

Organization	*Access time*
32 Kbit x 8	*70 ns*
128 Kbit x 8	*70 ns*
64 Kbit x 1	*15 ns*
256 Kbit x 1	*25 ns*
64 Kbit x 4	*25 ns*

FAST FEEDBACK

Please send details as soon as possible on:

- ☐ Laser Modules
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MITSUBISHI
SEMICONDUCTOR

Circle 113 on reader service card

INTERNATIONAL PRODUCTS

TRANSIENT-VOLTAGE SUPPRESSOR CUTS BOARD SPACE BY THREE FOURTHS

SGS-Thomson combines eight clamping diodes with common ground electrode

SGS-Thomson Microelectronics' transient-voltage suppressors integrate eight clamping diodes in one package, cutting board space by three quarters. The devices also reduce design and production time in systems that protect against electrostatic overloads on computer input/output ports, modems, and other parallel-port devices.

The monolithic TH6P04T6V5CL and TH6PO4T25CL outclass solutions that use discrete clamping diodes not only in space and design cost but also because multiple discrete devices can create more capacitance than the I/O bus's driver can handle—typically 500 pF per device or more.

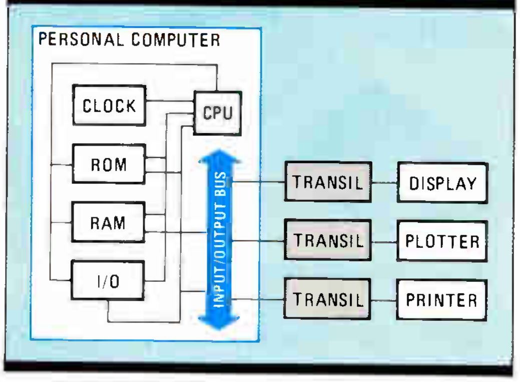
STM's devices solve the problem by combining eight bidirectional clamping diodes, called "Transils," with a common ground electrode. The devices have capacitance one half to one fifth as low as discrete solutions, depending on the solution chosen. At 5-V bias, the maximum capacitance of each diode is 500 pF for the 6V5CL and 300 pF for the 4T25CL.

The arrays contain eight clamping diodes and 16 fuses and replace a total of 24 discrete devices that now must be soldered to the board. If both suppressors and fuses are taken into consideration, the STM solution takes up one quarter of the space of competing discrete solutions, says Alain Bernabe, the Tours, France-based STM manager in charge of marketing the device in France and Northern Europe.

Each diode has a symmetrical current/voltage characteristic that presents a high impedance to ground for line voltages up to the 6.5-V breakdown voltage for the 6V5CL and 25 V for the 4T25CL. High impedance means that most of the time there is very little current to disturb the circuit, says Bernabe.

The monolithic solution also delivers better clamping performance because it creates less inductance between the device and its leads. A typical discrete device has leads connected to each end of a die and can handle fewer than 10 V. Even if the die limits the voltage to a low value, a higher value is measured across the device due to the inductance of the wire, Bernabe says. With a single-chip solution, the circuit "sees" only the clamping voltage across the dies—not the overvoltage in the wire caused by the inductance. This means overvoltage protection is closer to the value resulting from the peak current rather than the rise time of the surge.

PERIPHERAL PROTECTION



In a typical application, SGS-Thomson's Transil arrays protect the peripheral devices of a personal computer.

For short overvoltage pulses, the fast-acting diodes provide an almost instantaneous response, clamping the voltage to 12 V for the 6V5CL or 35 V for the 4T25CL. The peak pulse power that can be handled by a diode depends on the pulse duration, ranging from around 10 W for a long 100-ms pulse to well over 1,000 W for a 10-μs pulse.

Besides the computer peripherals market, STM sees a variety of new applications developing for the product. In particular, France's success with the Minitel videotex system indicates that more devices in the home will combine the computer and the telephone. This market trend can only accelerate as the Integrated Services Digital Network comes into use. Another application is to stabilize measuring equipment hooked to a variety of devices.

Each device can withstand an electrostatic overstress of 25 KV, measured according to the military standard MIL-STD-883C. Available now, the 6V5CL and the 4T25CL cost $5 each in 1,000 piece quantities. Both devices are available now. *– Jennifer Schenker*

SGS-Thomson Microelectronics, Centre des Etudes et Fabrication de Tours, Rue Pierre et Marie Curie, 0155
3700 Tours Cedex France.
Phone: 33-47-42-40-16 [Circle 500]

DISPLAY IS ONLY 90-mm THICK

A 15-in., high-definition, ac plasma display from Fujitsu Ltd. boasts 1,024-by-768-pixel resolution in a self-contained package thin enough to be mounted on a wall. An optional tilt stand adapts it to desktop use with a work station.

The 90-mm thick FPF1200S requires no auxilliary equipment when wall-mounted because of a sandwich-like design that puts the plasma panel on the topmost layer, driver circuits in the middle, and power supply on the bottom.

Applications include work stations for both office and engineering environments where space-saving, high-definition monochrome displays are desired. But the FPF1200S is equally suited for built-in equipment or vending-machine displays.

The display offers a 160° viewing angle, brightness of 70 candelas/m^2 (filter in place), and a contrast ratio of better than 20 : 1. Its effective viewing area of 307-by-230 mm delivers a dot spacing of 0.3 mm in both the horizontal and vertical directions. The rated lifetime of the plasma panel is 50,000 hours.

Deliveries are scheduled to begin in September. Pricing varies, depending on the quantity ordered.

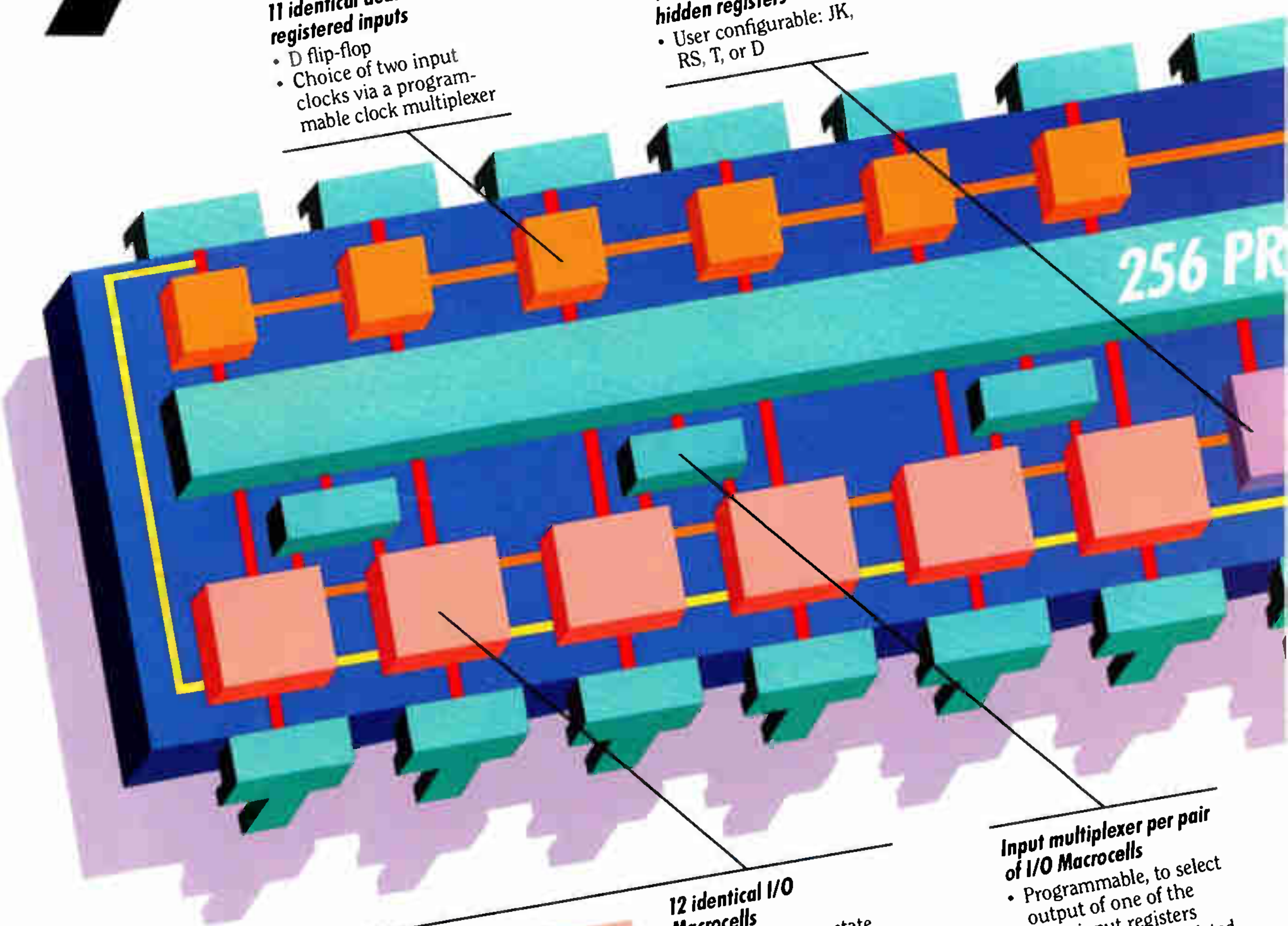
– Charles L. Cohen

Fujitsu Ltd., Electronic Components Marketing Divsion, 2-6-1 Marunouchi, Chiyoda-ku, Tokyo 100, Japan
Phone 81-3-215-2398 [Circle 501]

Synchrono

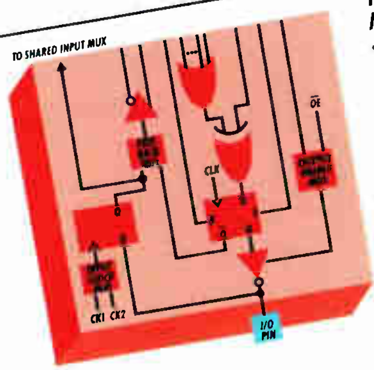
11 identical dedicated registered inputs
- D flip-flop
- Choice of two input clocks via a programmable clock multiplexer

4 identical dedicated hidden registers
- User configurable: JK, RS, T, or D



Input multiplexer per pair of I/O Macrocells
- Programmable, to select output of one of the pair's input registers
- Allows I/O pin associated with a hidden Macrocell state register to be saved for use as an input

12 identical I/O Macrocells
- Registered, three-state I/O pins
- Output state register, configurable as a JK, RS, T or D flip-flop
- Macrocell Input Register, choice of two input clocks via a programmable clock multiplexer
- Output enable multiplexer, programmable, to select common $\overline{OE}$ signal or Macrocell $\overline{OE}$ product term
- Input feed back multiplexer, programmable, to select either state register output or Macrocell Input Register output (creating a bi-directional I/O pin)



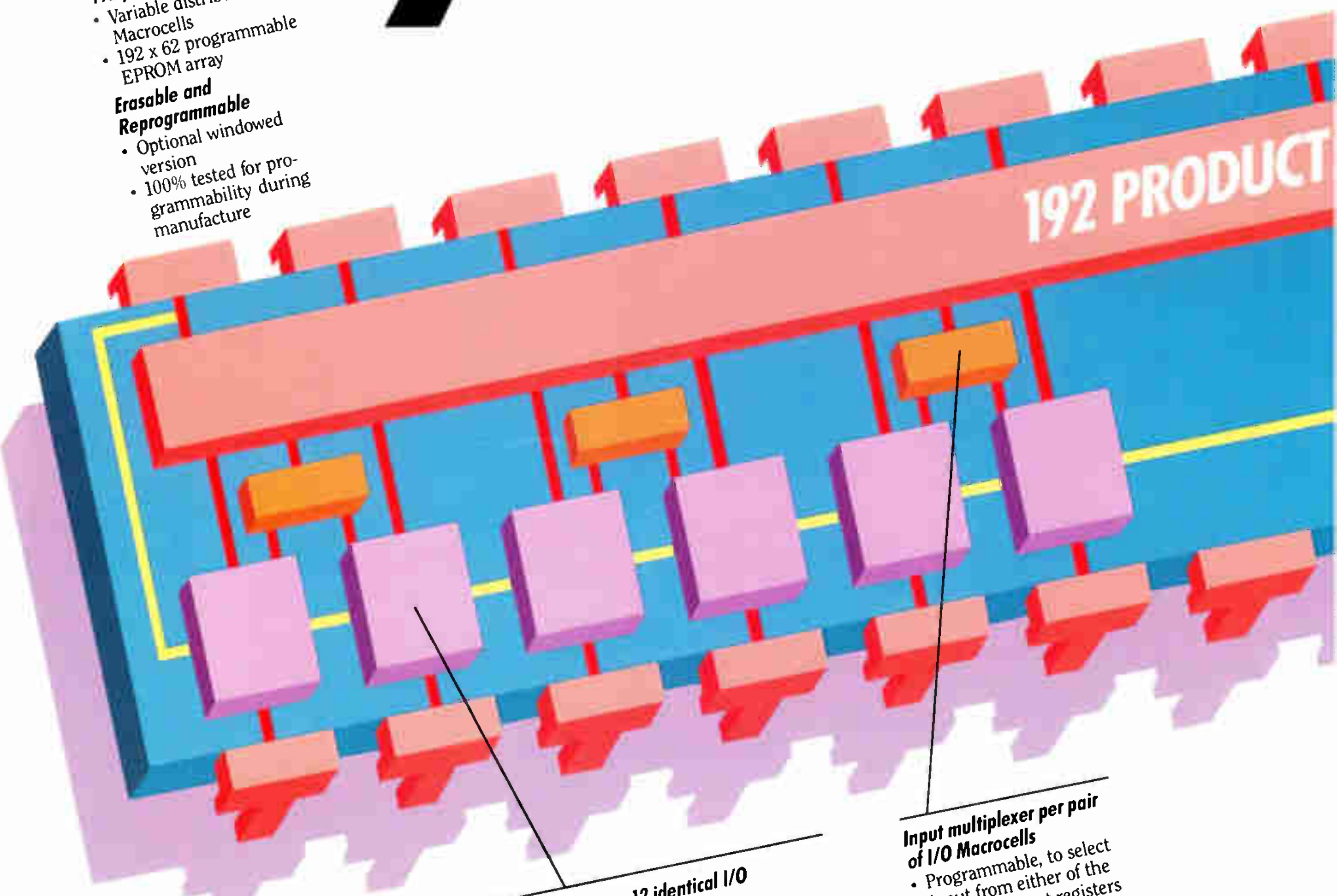
50 MHz operation
- Speed for high performance systems
- 5ns input set-up
- 15ns clock-to-output
- 20ns input register clock-to-state register clock

Low power
- 90 mA maximum quiescent I_{CC}
- 120 mA maximum I_{CC}

Asynchro

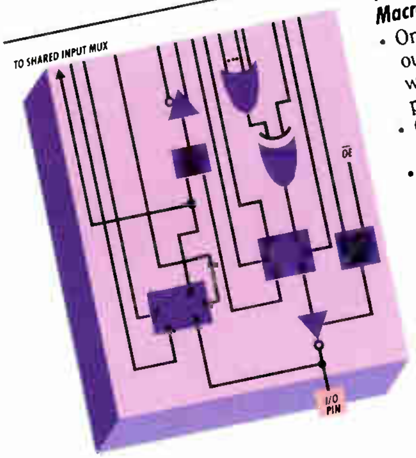
192 product terms
- Variable distribution to Macrocells
- 192 x 62 programmable EPROM array

Erasable and Reprogrammable
- Optional windowed version
- 100% tested for programmability during manufacture



Input multiplexer per pair of I/O Macrocells
- Programmable, to select input from either of the Macrocell input registers
- 96 variably distributed product terms from minimum 4 to maximum 12 per Macrocell, and 96 control product terms, for a total of 192 product terms
- 32 product terms are shared between two adjacent Macrocells, yielding 192 total product terms

12 identical I/O Macrocells
- One asynchronous output/state register with XOR sum-of-products input
- One asynchronous input/feed back register
- Independent (product term) set, reset, and clock inputs for both input and state register
- Asynchronous register bypass capability under product term control
- Global or local output enable



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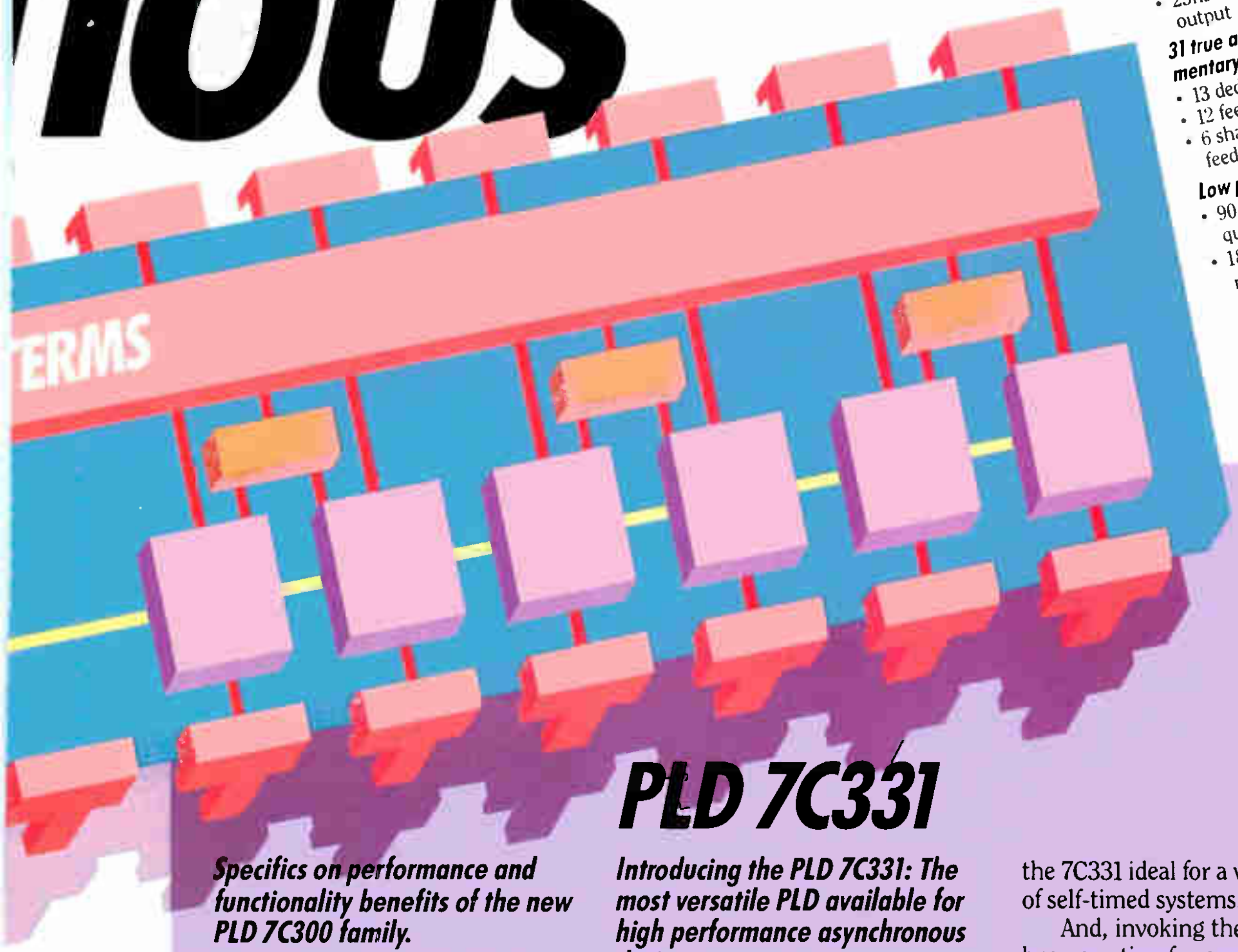


27 MHz Asynchronous operation
- Speed for high performance systems
- 20ns input set-up
- 25ns clock-to-output
- 25ns max input to output

31 true and complementary inputs
- 13 dedicated inputs
- 12 feed back I/O pins
- 6 shared I/O Macrocell feed backs

Low power
- 90 mA maximum quiescent I_{CC}
- 180 mA maximum I_{CC}

PLD 7C331

Specifics on performance and functionality benefits of the new PLD 7C300 family.

0.8 micron CMOS technology delivers blazing switching speed, using very little power.

Even better, it means denser, more powerful circuits that are delivered in very small packages.

As a result, the PLD 7C300 family parts are available in 28-pin slimline packages or PLCC packages, to ensure maximum board logic density.

Using these space-efficient parts, designers can create designs using as few as one quarter the number of parts required to implement a conventional PLD design.

This saves board space and cost, and even further improves system performance by reducing board interconnection delays.

All of these advantages are provided by a family of parts which stay cool, with the power saving benefits of leading-edge CMOS technology.

Introducing the PLD 7C331: The most versatile PLD available for high performance asynchronous designs.

Versatility through high *functionality:*

You get 2.5 times the logic density and register content of current generation programmable logic parts like the 20RA10.

Think of the design problems you can solve with 192 product terms at your disposal, in a system that runs at 27MHz!

Versatility through *flexibility:*

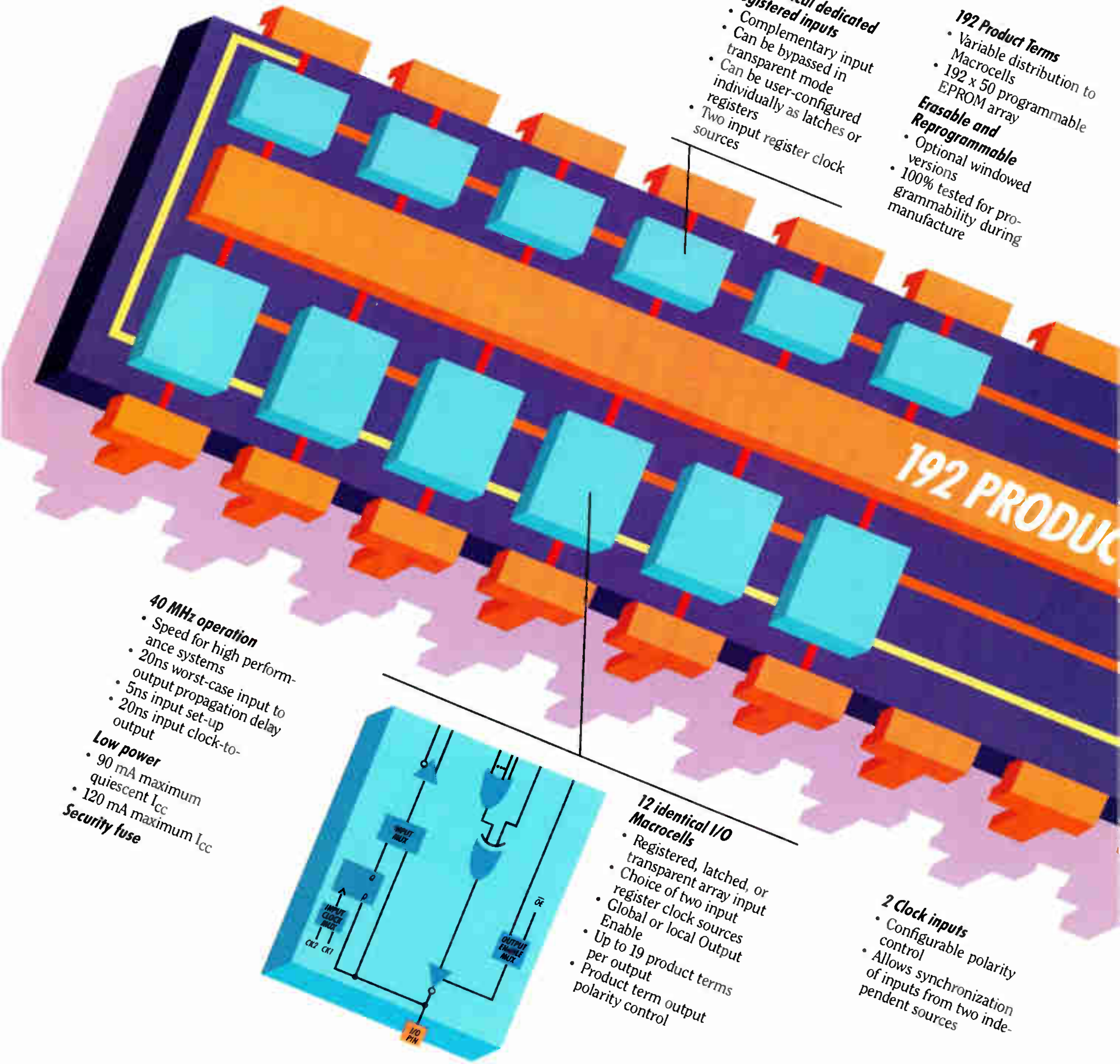
Input registers and output registers both feature product term control of set, reset, and clock, making the 7C331 ideal for a wide variety of self-timed systems.

And, invoking the register bypass option for combinatorial paths, you create a PLD ideally suited for use as a high density, general purpose random "glue" logic replacement.

Our PLD 7C300 Preview Kit will show you how the 7C331 can help you tackle the toughest asynchronous system objectives, and come out a winner.

PLD 7C300

Combinat



13 identical dedicated registered inputs
- Complementary input
- Can be bypassed in transparent mode
- Can be user-configured individually as latches or registers
- Two input register clock sources

192 Product Terms
- Variable distribution to Macrocells
- 192 x 50 programmable EPROM array

Erasable and Reprogrammable
- Optional windowed versions
- 100% tested for programmability during manufacture

40 MHz operation
- Speed for high performance systems
- 20ns worst-case input to output propagation delay
- 5ns input set-up
- 20ns input clock-to-output

Low power
- 90 mA maximum quiescent I_{CC}
- 120 mA maximum I_{CC}

Security fuse

12 identical I/O Macrocells
- Registered, latched, or transparent array input
- Choice of two input register clock sources
- Global or local Output Enable
- Up to 19 product terms per output
- Product term output polarity control

2 Clock inputs
- Configurable polarity control
- Allows synchronization of inputs from two independent sources

orial

PLD7C300

PLD 7C332

How the PLD 7C330 family saves you design time.

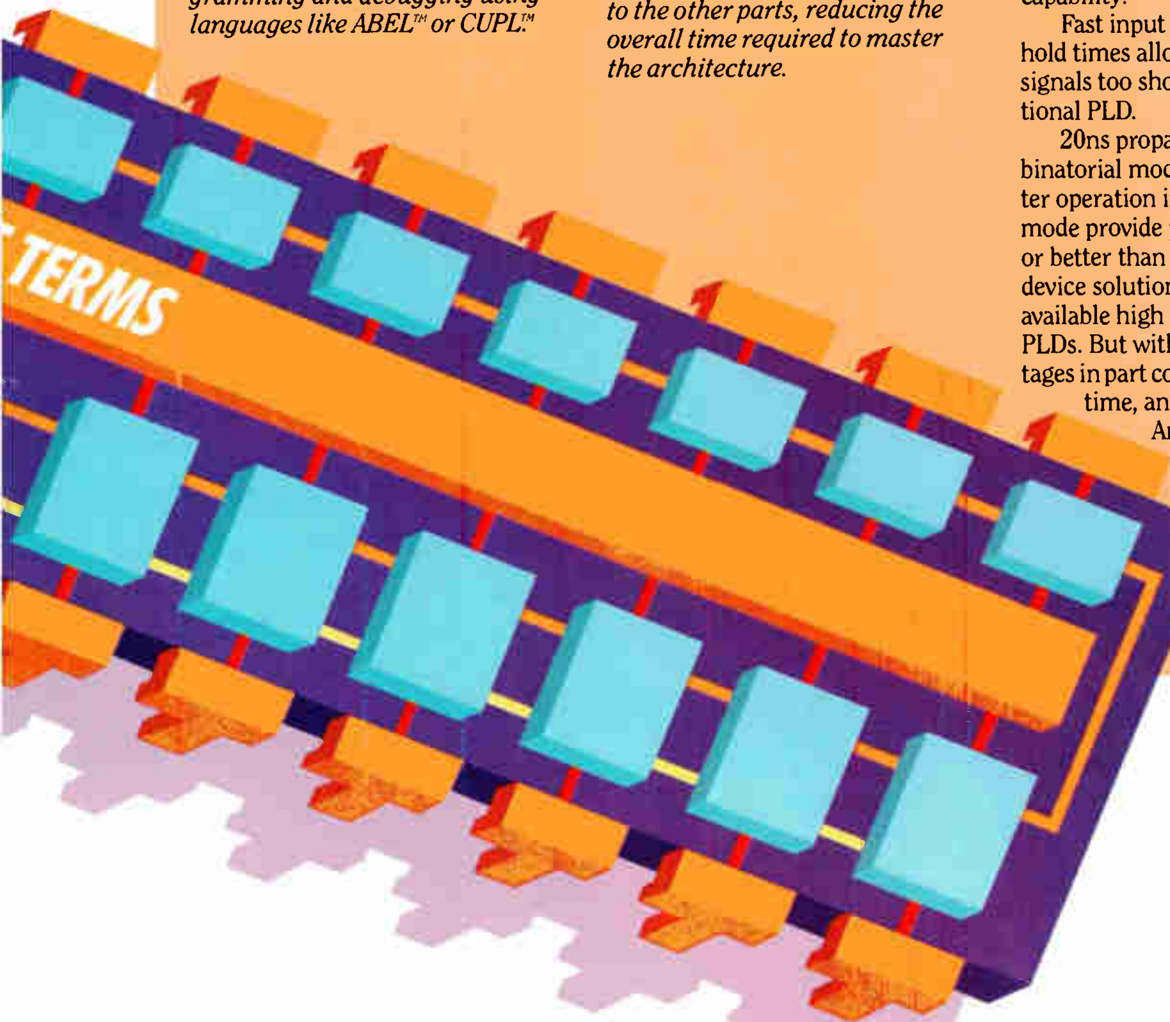
The high functionality of these new parts gives you the ease of PLD programming for applications where you may have once had to consider semicustom, or juggle multiple programmable parts to get the same functionality.

If you've designed with PAL20 or 22V10 programmable logic, you're familiar with the ease of programming and debugging using languages like ABEL™ or CUPL.™

If not, know that these languages let you design quickly, on a PC or equivalent, high level statements such as boolean expressions.

Because the PLD 7C300 family, with EPROM array technology, is available in windowed versions, you can program and reprogram easily, trying different designs, often in a matter of hours.

Because these parts are designed as a family, what you learn designing with one part carries to the other parts, reducing the overall time required to master the architecture.



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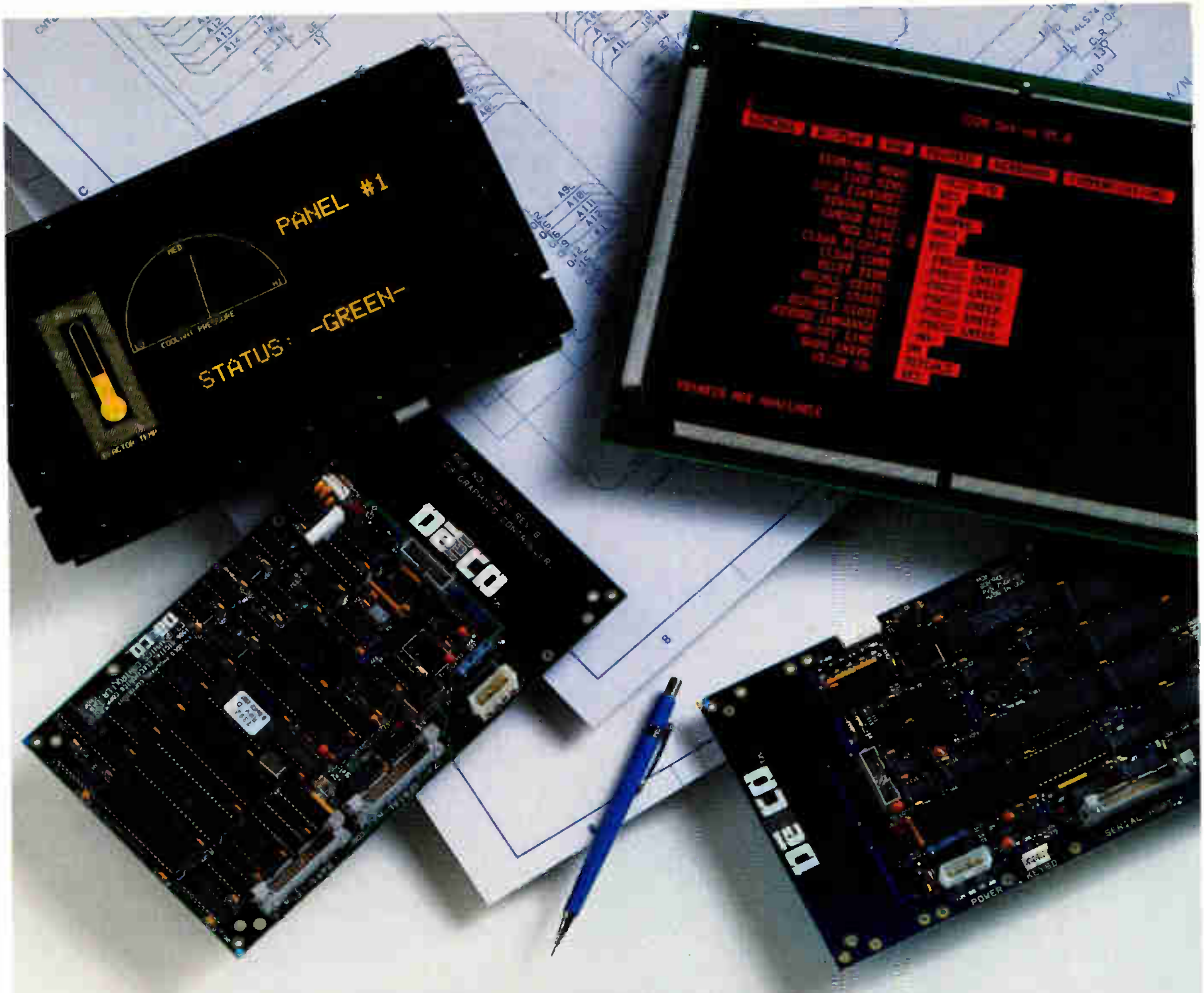

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INSIDE TECHNOLOGY

SUPERFAST SIMULATORS MAKE IT A LOT EASIER TO SKIP PROTOTYPING

Designers can now use a new generation of systems that do both fault and logic simulation, represent analog and digital circuits, and take on the biggest, most complex application-specific ICs and printed-circuit boards

by Jonah McLeod

The day of the prototype is almost over. Computerized simulation is coming into its own. The few integrated-circuit designers and many circuit-board designers who continue to build prototypes will soon gain a new level of confidence in simulators. They will find more and better models, running faster and representing both analog and digital circuits.

These changes already are reflected in a burgeoning market for simulation products, spurred on by the nightmare of having to design higher-quality products in less and less time (see fig. 1). In fact, the San Jose, Calif., consulting firm Dataquest Inc. expects that simulators will be the fastest-growing segment of the overall design-automation market, with growth exceeding 15% while the rest of the market stays between 10% and 15%.

Both logic and fault simulators are feeding this growth, and both are providing the models needed to perform effective multiple-chip simulations. Models are coming from various sources: the simulator supplier, who builds models for his own library; third-party suppliers such as Logic Automation and Quadtree; and computer-aided-engineering vendors, who offer physical models for complex circuits.

Suppliers are reducing the time it takes for a simulation to execute. New-generation logic and fault simulators, from Gateway Design Automation, for one, cut computation times by more than an order of magnitude. On top of that, hardware accelerators, especially the Daisy Gigalogician, reduce the simulation run time by several orders of magnitude.

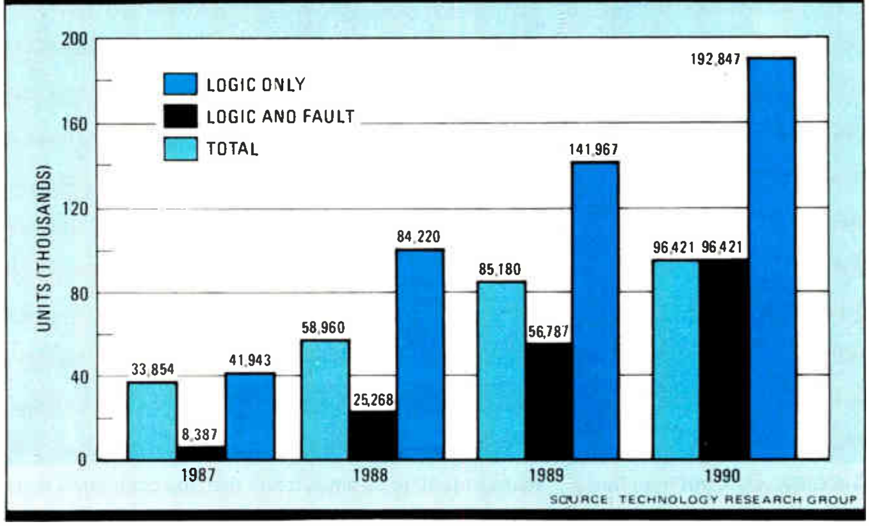
Simulators are improving in other areas too. Newer ones handle logic and analog circuits, and the latest versions of Spice allow designers to perform circuit optimization more easily.

With so much new capability being added to simulators, it is no wonder that the market for these design tools is beginning to take off. The market for total simulators will more than double this year over last, growing from 41,943 units in 1987 to 84,220 in 1988, according to Cindy Thames, vice president at the Technology Research Group, a market research firm based in Boston. She says that unit shipments will grow 70% in 1989 and 36% in 1990, at which time a total of 192,842 units will have been shipped. The market for simulators is about half of the total CAE business, says Isadore Katz, senior industry analyst at Dataquest.

One reason for this increased demand for simulation is the growth in application-specific ICs. ASIC design starts are going from 12,000 starts in 1987 to 50,000 starts in 1990, says Sanjiv Kaul, product manager for accelerators at Daisy Systems Corp. in Mountain View, Calif. And the average size of those ASICs is growing, he says. Their increasing complexity is motivating designers to simulate ASICs in the final system environment to eliminate costly design iterations.

One reason for design iterations is that some ASIC chips work during simulation, but fail once they are put onto a printed-circuit board. Typically, this occurs because the chip's specifications conflict with the larg-

WHAT'S AHEAD FOR SIMULATORS



er circuit-board specification. To solve the problem requires a multichip simulator that performs the same task as a pc-board simulator. But two problems have held back simulation of large multichip designs. First, models for all the possible chips that could be found on a board have not been readily available. Second, even if the designer could acquire all the models, the simulation run could take days to execute.

In recent months, there have been efforts by most simulator vendors and third-party model suppliers to provide extensive model libraries. For example, GenRad Corp.'s new System HILO has extensive modelling support (see p. 65).

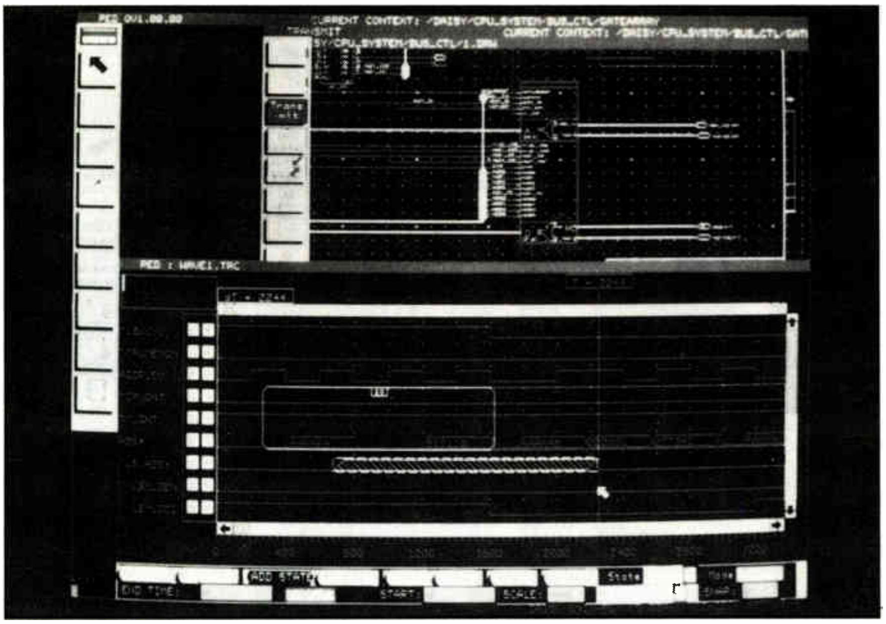
These libraries are starting to contain models of even the newest VLSI chips. Mohan Nair, marketing manager of design and analysis at Mentor Graphics Corp. in Beaverton, Ore., boasts, "When Intel Corp. announced its new 80960 microprocessor, we were ready with a physical model of the chip." When Motorola rolled out its new 88000 reduced-instruction-set microprocessor, Logic Automation Inc. of Beaverton, Ore., was quick to announce a behavioral-level simulation model of the device.

Semiconductor vendors have recognized that early design wins depend on getting models to the designer as soon as the chip becomes available. Another requirement for multiple chip simulation is to be able to model the connections between chips on a board. That is the only way to achieve a true representation of how a design will operate. Silicon Compiler Systems Corp. of San Jose, Calif., in February announced one such behavioral-modeling capability for wires. "With this capability, a designer can define the behavior of a bus without having to create a functional description of each wire," says Peter Odryna, product marketing manager at Silicon Compiler.

With models for every component in a multichip design, the problem facing the designer is running the simulation in a reasonable amount of time—preferably on a work station or a compute server on a network. One of the ways to cut the time is to develop algorithms that run the simulation faster; another is to create a faster hardware accelerator. One company that has made its reputation on fast logic simulators based on proprietary simulation algorithms is Gateway Design Automation Corp. of Westford, Mass. (see p. 63). Its Verilog XL simulator runs ten times faster than other logic simulators. The company has applied the same algorithm to a new fault simulator called Verifault-XL. The Verifault-XL runs some 10 to 20 times faster than the company's existing fault simulator product. By contrast, the approach Daisy took was to build a bigger, faster simulation accelerator. Called the Gigalogician (see fig. 2), it is 10 to 30 times faster than the company's previous product, the Megalogician. Faster simulation speed on the Gigalogician comes from a unique multiprocessor architecture. Hardwired processors accelerate switch- and gate-level simulation tasks and microcoded processors accelerate behavioral-simulation tasks and inputs from Daisy's physical modeler, PMX.

Designing a single chip or a system of chips invariably involves simulating an analog circuit somewhere in the design. According to the Technology Research Group, 39% of all semicustom IC designs will have analog functions by 1990. The percentage of pc boards with analog functions will be much higher. The holy grail that simulator suppliers are seeking, therefore, is analog and digital simulation rolled into one. One solution is to simply tie an analog and digital simulator together. One successful implementation of this approach is the marriage of the Viewsim from Viewlogic System Inc. of Marlboro, Mass., to the P-Spice simulator from Microsim of Laguna Hills, Calif.

Analogy Inc. of Beaverton, Ore., and HHB System Inc. of Mahwah, N. J., offer a more tightly coupled solution. It integrates Analogy's Sabre analog simulator with HHB's digital simulator (see p. 68). A similar capability is available from Silicon Compiler in its L Sim simulator. The simulator can handle feedback loops between analog and digital circuits, and do it in a reasonable amount of time.



THE GIGALOGICIAN from Daisy Systems runs 10 to 30 times faster than the company's earlier Megalogician by using a multiprocessor architecture.

The critical elements in the acceptance of simulation are the amount of time required for the software to execute and the compute power required to run the program. One of the drawbacks to Spice is that it takes an inordinate amount of time to run a simulation because it divides a large circuit into smaller, more manageable sections, which it simulates individually.

One new, more efficient product is Timemill, which comes from Valid Logic Systems Inc. of San Jose, Calif. (see p. 67). "With Timemill, a designer can run a transistor-level simulation of 100,000 transistors and the results will be within 15% of the results achieved with Spice," says Donna Rigali, product marketing manager. □

GATEWAY'S NEW SIMULATOR TURNS UP FAULTS IN A HURRY

Verifault-XL eases ASIC testing and speaks the same language as the company's logic simulator

Complex application-specific integrated circuits and printed-circuit boards containing them are the cause of many a testing nightmare. One reason is that fault simulators—programs intended to dig out potential problems in chip-design programs—are neither sophisticated nor fast enough to handle them. In addition, fault simulators are not well integrated with logic simulators, the programs that help ensure chip functionality. Or they lack a sophisticated hardware-description language and are difficult to use, as a result. Finding a way out of this maze of difficulties is troublesome, but Gateway Design Automation Corp. of Westford, Mass., says its Verifault-XL fault simulator can end such testing nightmares.

Intended to replace the company's first-generation TestGrade fault simulator, the Verifault-XL simulator runs at least an order of magnitude faster than its predecessor and competitive products. The speed improvement comes from two areas. The Verifault-XL simulator employs an algorithm already used in the company's sister product, the Verilog-XL logic simulator. Also important is the ability to perform concurrent fault simulation of behavioral (high-level) models. Another speed advantage is that the Verifault-XL is the first simulator that can simulate faults over a local-area network, Gateway Design says.

What's more, the company's fault and logic simulators both speak the same hardware-description language. Others vendors' products do not, the company says. The common language is terse, yet produces large amounts of stimuli with relatively few input statements. So closely are the two simulators allied, that Verifault-XL and Verilog-XL will be sold together. Work station versions of the combined software sell at a starting price of $30,000 for existing Verilog-XL users. The software runs on a variety of hardware platforms, including systems from IBM Corp., Digital Equipment Corp., Sun Microsystems Inc., and Apollo Computer Inc. Gateway says it will begin shipping in July.

With the steady increase in the number of gates on ASICs as well as the swelling number of ASICs on boards, it's no wonder that the demand for simulation is growing too. Technology Research Group, a Boston market research firm, estimates that the number of fault simulators sold will grow to 96,000 in 1990 from 8,400 in 1987. A more conservative estimate, however, comes from Dataquest Inc., the San Jose, Calif., market research firm. Dataquest places the 1990 total at 50,000 units. Just the same, it is clear that there will be a whopping demand for fault simulators within the next few years.

Fault simulation's goal is to find all the potential manufacturing defects that could show up in a chip's functional circuit, that is, one which has been verified to be "good" by the designer. During simulation, a test engineer inserts a fault into a model of a circuit design. A test pattern is then applied to two models—one containing the fault and one known to be good. If the test pattern detects the fault, the pattern is kept; if not, it is discarded and another pattern tried. The designer repeats these steps for every fault that could occur. Because this is a serial process, the testing can be very time-consuming with older fault simulators.

Concurrent fault simulators, which simulate many faults at the same time, drastically reduce compute time. But these newer simulators need expensive hardware accelerators when working with very complex circuit designs. That accelerator hardware can cost from $100,000 to more than $1 million and it is no wonder engineers would like to avoid the expense.

Verifault-XL is the way to do that, says Gateway Design, because it works as fast as any accelerator. "One benchmark we ran on a 5,728-gate logic design took 63.3 minutes on a 2-mips Sun 3/160 work station," says Prabhu Goel, president and founder of

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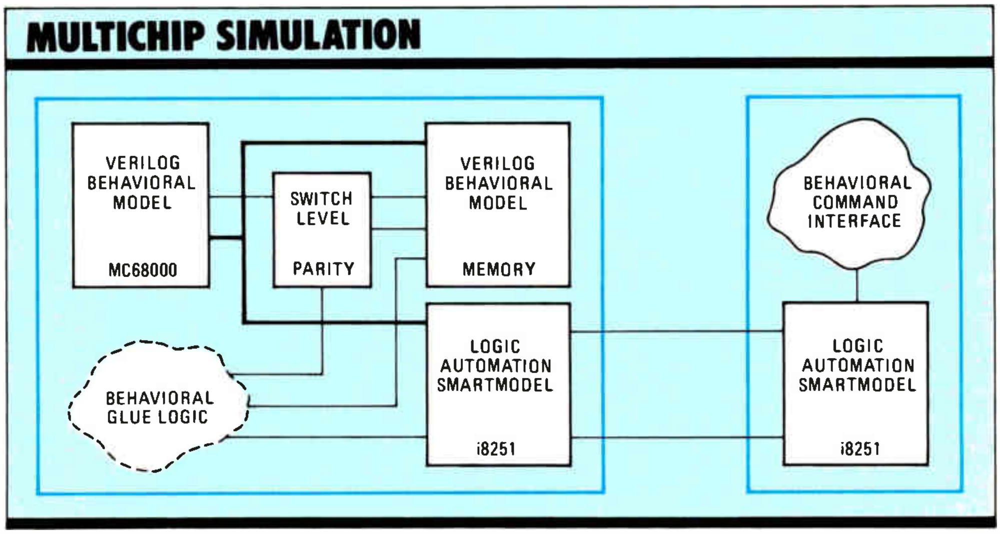

1. Simulation of multichip models containing various logic circuits and memories, as well as processors like the Motorola 68000, is crucial for today's more complex designs.

Gateway. "The simulation produced 98% fault coverage and produced 5,000 test patterns, which detected nearly all of the 14,140 possible faults in the design."

Verifault-XL runs an order of magnitude faster than any other fault simulator thanks to its adaptive-behavior recognition algorithm, an advanced form of a technique called clock suppression. The reduction in time comes from only simulating models in which data has changed. "With the technique, if the data input to a model has not changed," Goel says, "you can avoid having to evaluate the model. What we have in our algorithms is something that carries the concept much further."

Another special feature of the Verifault-XL is that it is the first to simulate faults over a local-area network. The task of comparing outputs from test vectors applied to good and faulty models can be easily split up among networked processors. Each can process some portion of the total set of faults to be evaluated. "Overnight, you can bring supercomputing power to fault simulation by putting as many work stations to the task as are available," Goel says.

As one example, Goel cites the following: "Running on DN660 [Apollo work station] nodes, 4,800 seconds is all that is needed to do a full fault simulation of a 6,600-gate circuit on a single node," he says. "When the job is distributed among six work stations on a network, the time is reduced to 800 seconds. The cumulative CPU time across the network does not climb very much because there is very little cross communications required between the various processors."

Another way the Gateway simulator reaches high speeds without acceleration is by concurrent simulation. Although concurrent fault simulation is not new, the Verifault-XL adds a twist by performing behavioral level simulations in a mixed-simulation environment. In some systems, fault simulation of gate- and switch-level components occur in parallel, but a behavioral model might have to be simulated serially. An MC68000-based system is an example of a design containing mixed levels of models (see fig. 1). In the figure, are a behavioral Smart model from Logic Automation Inc. of Beaverton, Ore.; a Verilog behavioral model of a 68000 microprocessor; another of a memory module; a Verilog behavioral description of some glue logic; and a switch-level description of a circuit.

Other simulators defining the behavioral models of the microprocessor and memory in this example must perform a serial fault simulation of these models. "While the [other] simulators can perform a concurrent simulation elsewhere in the design, they bring all the faults to the boundary of the behavioral model and then propagate one fault at a time serially through and collect the results at the output," Goel explains.

Verilog is the common language used on both the logic and fault simulators. This contrasts sharply with the multitude of different languages typically used in varying simulations. For example, it is not unusual to find one language for gate-level description, a second language for behavioral description, a third for stimulus, and still another to describe timing. "The user has to speak many languages to get his job done," Goel says. "By contrast, Verilog is a very simple lan-

HOW GATEWAY GOT ON THE FAST TRACK IN CAD

Prabhu Goel founded Gateway Automation Design Inc. six years ago with an initial investment of all of $500. That investment has grown into a company that will hit $5 million in sales at the end of its current fiscal year in July. In the last two years, the company has grown 100% a year; before that, it was doing 50% a year. "Gateway is the fastest growing company in the computer-aided engineering market," says Isadore Katz, senior industry analyst at Dataquest Inc., a San Jose, Calif., market research firm.

The man behind Gateway's meteoric rise is Prahbu Goel, who founded it and is now president and chief executive officer. Goel's career began after he earned a doctorate in electrical engineering from Carnegie Mellon University, when he joined IBM Corp. He spent eight years at IBM and ended up with a corporate achievement award—one of IBM's highest honors—for contributions to the testing of the 3081 computer. "On receiving the award in 1980, I decided that although IBM was a great company, my personal growth opportunities were limited," Goel says. After a year with Wang Laboratories Inc. in Lowell, Mass., Goel struck out on his own.

He was joined by two cofounders, Chilai Wong and Philip Moorby, both of whom continue as technical experts within Gateway. The first year and a half was tough because no revenues were coming in from product sales. Goel turned to consulting to finance the development of Verilog, Gateway's first product.

The investment paid off and in December 1983, the infant company shipped its product to Raytheon and Texas Instruments. From then on, the company earned enough to pay for its operations—it needed no outside financing and sought none.

Nevertheless, three venture capital firms sought out Gateway and in 1986 approached it with offers to invest in the startup. "We were able to get financing on much better terms than we otherwise could have," says Goel. "And we were able to choose to our investors." Gateway chose Greylock Management Corp. and Fidelity Investment. The two provided $2 million in financing in return for a minority position in the company and seats on the board of directors.

In 1987, the company made a move into Japan. Gateway became the Japanese distributor for SC High Tech, a subsidiary of Sumitomo Corp. of Tokyo. It was a sweet deal for Gateway, guaranteeing $1 million a year in revenue for two years. "We already have seven major Japanese computer and semiconductor companies as customers," says Goel.

From Japan, the company went on to Europe. "We now have distributors in England, France, Italy, and Germany," says Goel.

Analysts are high on Gateway. "It's one of the hottest growth companies," says Peter Schleider, a partner in the investment firm of Wessels, Arnold, and Henderson in Minneapolis. Katz, at Dataquest, points to the company's new Verifault simulator as evidence that the technical innovation that vaulted Gateway to prominence in logic simulation is going to continue with fault simulation. *–J. McL.*

Prabhu Goel

guage but it can represent all the hardware constructs a hardware designer would need."

A typical command-line "conversation" for detailing fault simulation of a 4-bit adder might look like this (see fig. 2): $insert faults; stim=0 "for (stim=1; stim<256; stim = stim * 2) #10$strobe faults (carry out, sum). The first command tells the system to insert faults and perform a concurrent fault simulation of the circuit. Until the system sees the command, it performs a good-machine type simulation. The second command tells the system to start the simulation with an all-logic-0 input to the adder. The "for (stim=1; stim<256; stim = stim * 2)..." portion of the third statement tells the simulator to iterate through a loop 256 times and, on each iteration, multiply the previous stimulus by 2. This increments the stimulus value.

The remainder of the statement—which is #10$strobe faults (carry out, sum);—directs the system to strobe the outputs of the adder for faults after 10 units of time delay. The system cycles through pattern application, waits 10 units of time, and strobes the output for faults. It repeats this process 256 times. In these few statements, nine vectors are generated and the system is told when to measure the response.

Verifault has incremental simulation capability. This means the user can stop a simulation and restart it exactly where it left off, an important capability in a compute-bound process. It also has the ability to take random samples of faults, fault-grade them, and use the samples to project what the fault coverage for the entire design will be. It is an accurate way to determine fault coverage without spending a lot of computer time, but the technique only tells the user whether the sampled faults are tested or not. *–Jonah McLeod*

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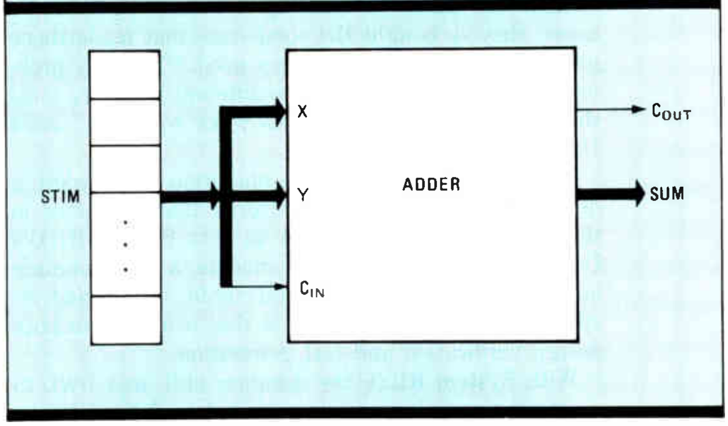
A COMMAND-LINE CONVERSATION



2. One language serves both design and fault simulation. Here, a conversation builds a fault file for an adder.

GENRAD PUTS EVERYTHING TOGETHER IN ITS HILO PACKAGE

The integrated software combines all the tools designers need for ASIC and pc-board simulation

Designing application-specific integrated circuits and printed-circuit boards may be fast-track engineering, but when it comes time to test the results, the situation becomes hurry up and wait. The disparity between the weeks it takes to design a chip or board and the months it takes to write test programs for it is becoming so obvious that upper-level managers are beginning to take notice. The problem is the time it takes to translate the large number of vectors from the design simulator into a form usable for developing test patterns. So much data is lost in the translation that the test engineer has to create additional vectors to ensure finding all possible chip or board faults. In addition, automating pc-board test generation has lagged because of the lack of models for the wide variety of devices possible on a board.

The situation is about to change, GenRad Corp. believes, because of the Concord, Mass., company's new System HILO, a tool set that integrates all elements of IC and pc-board simulation. For starters, System HILO comes with a new Design Waveform Language that enables a programmer to write subroutines that mimic the hardware of a target tester. With the language, an engineer can take the design data and write a test program tailored specifically for a tester. That program can be downloaded into the tester and run with no translation.

To automate the generation of tests for pc boards, System HILO has extensive modeling capability. First, it starts with a library of 6,000 commonly available chips. If those are not enough, it offers software hooks into models provided by third-party suppliers—Logic Automation Inc. of Beaverton, Ore., and Quadtree Inc. of Mahwah, N. J., for instance. Then, it tackles more complex devices with its physical modeling capability, a technique that calls on actual devices during simulation. There is more: still another facility generates ASIC libraries, and plans are under way for one to handle programmable logic devices.

System HILO is a complete simulation tool kit. It is made up of design analysis and verification tools and test-generation tools for ICs and pc boards. The set is modular, and can be configured to specific design or test needs. Design validation is the province of Hisim; Hitime is the dynamic timing analyzer (see figure). For test generation and fault simulation, Hitest and Hifault come into play. The system runs on a variety of hardware platforms—systems from Apollo, Digital Equipment, Hewlett-Packard, IBM, Intergraph, Prime, Ridge, and Sun. Prices for System HILO modules start at $25,000.

"Where the competitors are lacking is that they have provided point solutions," says Peter Denyer, GenRad's marketing manager for design automation products. By that, he means the competitors have bought the rights to existing products—or in some cases, they've bought the companies that made those products—to get the tools they need. "The only problem is that these solutions are different software tools that have got to be made to work together," says Denyer.

Typically, in simulating the operation of a design, a designer creates stimulus patterns that no tester in the world can duplicate. Not so with System HILO's Design Waveform Language module, a programming language for describing digital-circuit stimuli and responses. The beauty of DWL is that it applies to both design verification and test generation.

With System HILO, the designer still uses DWL to create the complex patterns needed to fully debug a design. The difference is, a test engineer can work in parallel with the designer; he can suggest ways to change the design for better testability, rather than wait until it has been completed and cannot be changed. As the designer creates debugging vectors, the test engineer creates a software model of the tester. "With DWL, a test engineer can define a subroutine containing the complex structures and timing relationships between various tester signals," says Denyer. "For example, for a test system with six timing sets—vectors and formats—he can write subroutines to emulate the behavior of the sets, and include other tester hardware components. The greater the parallelism, the faster the time to market."

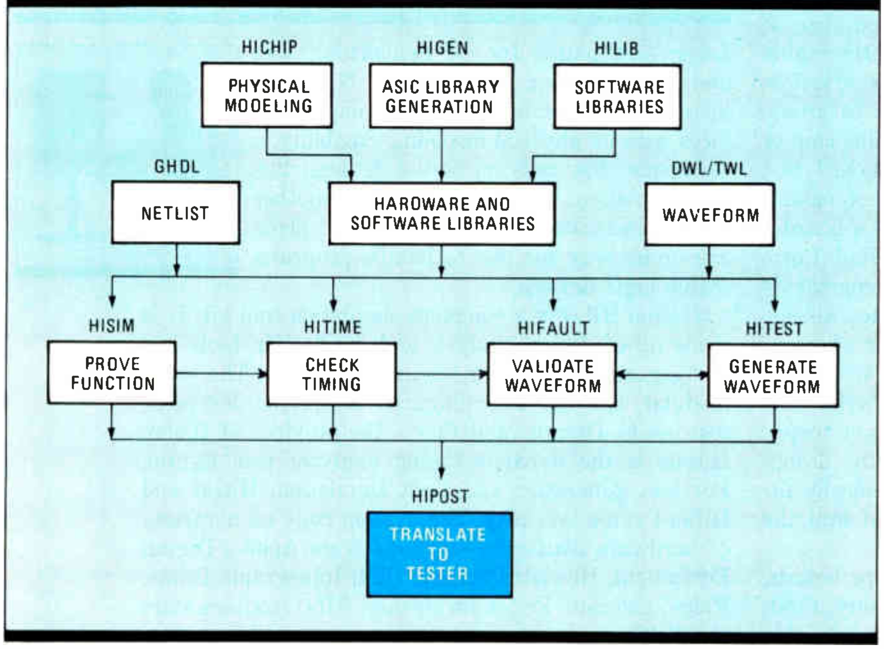
In addition, the test engineer can create a model of the target tester in System HILO and determine which of the vectors created by the designer are usable by the tester. Moreover, it is easy to add test vectors to achieve a desired amount of fault coverage. Fault coverage is a measure of the number of faults a test program can detect. Most specifications call for a coverage of 95% or even more. With a GenRad test system on-site, the test engineer can define device stimuli with GenRad's Tester Waveform Language, or TWL. The stimulus data created with the language will be ready to run on GR275x board testers. There is no need to construct a tester environment with DWL.

One of the stumbling blocks to more automated pc-board design and test has been the lack of component models. Because of the wide variety of available devices, Denyer says, "you can't simulate a circuit board unless you have libraries with large numbers of component models." To address this need, GenRad has embarked on a large-scale library development program. At introduction, System HILO comes with Hilib, which contains 6,000 devices. "We have more than 20 people assigned to continually add more components to this library," Denyer says.

GenRad is developing its own library so as not to be dependent on third-party model suppliers. "We recognize that System HILO users will want to use third-party models, so we have built software hooks into third-party models, like those from Logic Automation and Quadtree." But even with a team dedicated to creating models and the increasing availability of models from other vendors, software models of new devices typically will not be available when the devices are first announced.

To get around that, GenRad offers a physical modeling system called Hichip. "When Intel announced its new 80960, we had a physical model of the chip," Denyer claims. "Chip manufacturers are beginning to realize that to achieve early design wins they are going to have to provide models of their devices. One problem in the past is that a physical model may work well in design verification and fault simulation but not in timing analysis and test generation. Our physical modeler works with the timing-analysis tool to ensure we have considered all the timing limitations."

GO STRAIGHT TO TEST



System HILO saves time because design vectors no longer need translation before entering the test environment, and because engineers do not have to write more test vectors.

System HILO's Higen generic ASIC library-generation tool provides a means to easily generate and maintain high-quality ASIC libraries. Higen consists of a generic library tool that contains a set of parameterized component models. Output from Higen is a configured ASIC library written to GenRad's modeling standard. On top of Higen, a PLD module generator, an option to Hilib, provides a path between PLD design and pc-board logic simulation. The module generator uses a data base of PLD device types and the Jedec file created in the PLD design phase to create a custom PLD model in System HILO's Hardware Description Language format. The model can then be used in a board-level simulation of the design containing the PLD. *–Jonah McLeod*

For more information, circle 481 on the reader service card.

VALID'S TOOLS MAKE TIMING ANALYSIS FAST AND EASY

Timemill lets designers analyze complex designs with many transistors without leaving layout mode

Ensuring that a laid-out integrated circuit runs at a specified speed is a time-consuming and error-prone process. The usual method forces designers to stop layout, call up a simulator, and run a timing analysis. For accuracy, engineers usually go to a version of Spice, a public-domain simulator that handles only 100 transistors at a time. An IC with 50,000 gates could take days to analyze.

Now Valid Logic Systems Inc., the San Jose, Calif., design automation tool supplier, has introduced a simulator, called Timemill, that gives designers a better analysis path. The tool serves both the system designer who works with standard cells and the IC designer who creates the library of cells or engages in full-custom design. Analysis can be pattern-independent, where a designer gets a breakdown of the longest paths in his circuit, or it can be pattern-dependent, and provide the actual set-up and hold times of critical paths in the design.

Because the simulator is completely integrated into the Valid design system, a designer can enter Timemill while still in the layout mode and execute a timing analysis that tells him how his layout affects timing. He can move back into the layout tool instantly and make changes to speed up or slow down a portion of the circuit. Timemill also solves the problems faced by Spice, the only other simulator with comparable analysis capability. It can handle large designs, which Spice cannot. It executes very rapidly even on complex designs with a large number of transistors.

Timemill is a simulator designed for performing timing analysis of entire CMOS circuits. It runs on VAXstation II and VAX3000 series work stations from Digital Equipment Corp. and the Sun 3 and Sun 4 work stations from Sun Microsystem Inc., as well as Valid's proprietary SCALDstar work stations. The $15,000 tool is available 90 days after order.

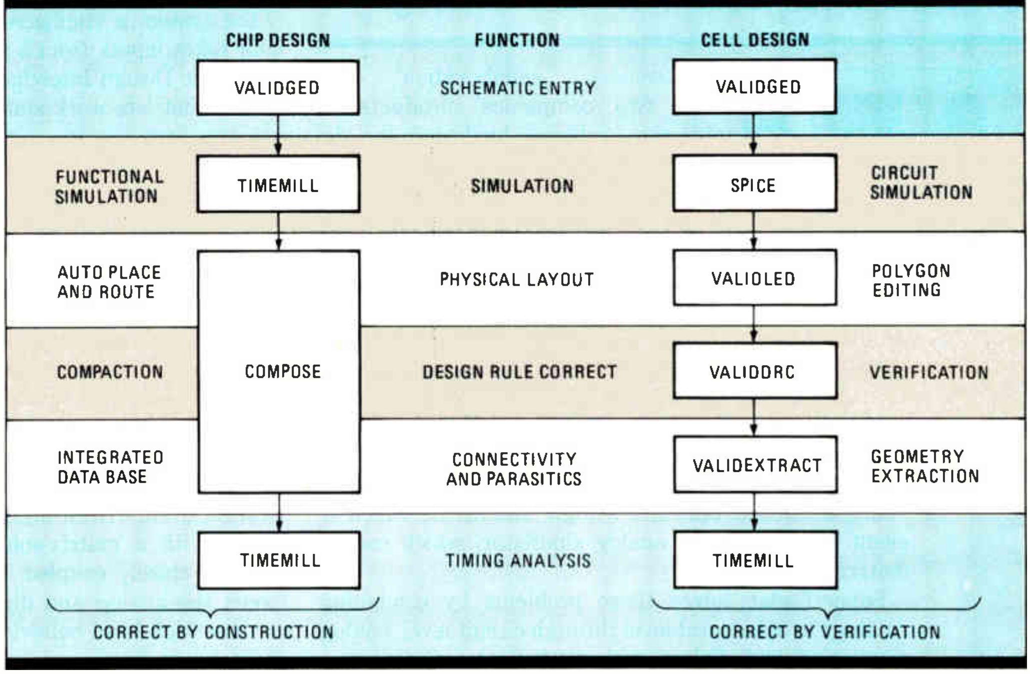
Valid acquired the software from Epic Design Technology Inc. of Santa Clara, Calif., in a strategic partnership agreement between the two companies signed in October 1987. Valid, which holds a minority interest in Epic, integrated the software into its own design tool set.

What is new in this implementation of Timemill is its integration into a larger tool set. Up until now, a designer gave his netlist to a foundry for layout or moved the netlist from his design simulator to his own layout tool, where a layout was produced. After the layout was completed, the layout tool created a file containing the values of resistances and capacitance in the connections between gates and the delays through the gates. "The file would then be reformatted into a netlist that a simulator could understand," says Donna Rigali, product marketing manager at Valid. The reformatting step was time-consuming and prone to error. By contrast, Timemill performs timing analysis directly from the extracted layout, thereby eliminating the reformatting step.

Creation of a cell begins with schematic entry (see figure). Since cells typically run no more than 100 transistors, a Spice simulation works fine. Then the designer creates a cell layout with ValidLED, a layout editor. Next, he runs a design rule check using ValidDRC and extracts, with ValidEXTRACT, a netlist containing all the resistance and capacitance values. Timemill then executes a transistor-level simulation, using the extracted data to verify the timing of the cell.

The cell "welder" goes through a similar process. He enters his schematic via ValidGED and, using Timemill, runs a functional simulation of the design. Timemill

DESIGNING THE EASY WAY



Valid's timing-analyzer tool is aimed at both the system designers who work with standard cells and the IC designers who create libraries of cells. It handles many more transistors than can Spice.

can perform either a functional- or transistor-level simulation because it is a true mixed-level simulator. Concurrently, it performs behavioral, register-transfer, gate, and transistor switch-level simulation.

Once simulation proves that a cell-based design is functionally correct, the designer gives the netlist to Compose, Valid's automatic place-and-route and compaction tool. It creates a layout of the standard cells. While in Compose, the designer can issue a command that automatically creates a netlist containing the routing delay capacitances. Then he can then enter Timemill and perform one of two timing analyses: pattern-independent or pattern-dependent. The former applies no test vectors to the simulation; the latter does.

In executing a pattern-independent analysis, the simulator can perform the timing analysis using simultaneous behavioral, register-transfer, gate, and transistor switch-level models in the netlist. If there are no higher-level models, then the entire simulation will occur at the transistor switch-level, which means that simulation will be slower than if higher-level models were present.

In the independent mode, the simulator looks at every possible path and finds the longest paths. The designer can perform critical-path analyses to determine the maximum clock speed. For example, if the chip must run at 30 MHz, and it is not quite that fast, the critical-path analysis capability of Timemill will trace the paths and determine which signal or signals fail to meet the specification. In the pattern-dependent mode, the designer provides the simulator test vectors. The mode reveals the delays and set-up-and-hold times of the critical paths, Rigali says.

After timing analysis is complete, the designer can bring up the Compose place-and-route tool and interactively reroute a signal path so that it is shorter, or run the compactor to try to bring the size down further. The entire process takes no more than a minute.

The designer then creates a Timemill netlist and goes back into Timemill to see if the critical path has been shortened, and if the chip finally meets specification. "The benefit of the whole system is that it lets designers build chips to specifications, a plus for high-performance chips," says Rigali. Not only is the simulator fast, it is also very accurate.

Simulation results are within 15% of those achieved with Spice, and accurate transistor-level simulations are possible on devices containing more than 100,000 transistors. Using Spice would require breaking up the design into small sections, 100 transistors or fewer, and analyzing each individually. In fact, one of the greatest strengths of the simulator lies in its transistor models. They allow the detection of problems associated with ratioed logic, charge sharing, pass transistors, heavy feedback, resistance-capacitance trees, and static and dynamic devices. *–Jonah McLeod*

For more information, circle 482 on the reader service card.

TECHNOLOGY TO WATCH **SIMULATION**

ANALOGY AND HHB TEAM UP ON ANALOG/DIGITAL DESIGN

They merge their products to form Saber/Cadat, a simulator that can tackle mixed-function design

A coast-to-coast collaboration has fused two companies' products to solve the problems hindering the development of simulators for mixed analog and digital systems. The two companies are Analogy Inc. of Beaverton, Ore., and HHB Systems Inc. of Mahwah, N.J., and their new simulator is called Saber/Cadat.

The simulator tackles two interrelated problems in simulating mixed functions. One is the need for an analog simulator that can do modeling from the behavioral through the primitive level. Until now, such modeling has not been possible; engineers have had to rely on prototyping. The other problem is the technical challenge involved in coupling and providing feedback between a logic simulator, which is event driven, and an analog simulator, which uses a matrix approach.

Saber/Cadat solves these problems by combining Analogy's behavioral-level-through-circuit-level analog simulation tool, Saber, with HHB Systems' Cadat, a popular digital simulator. The new product provides modeling of analog elements (including nonelectronic elements) as well as digital elements. It incorporates a proprietary algorithm that enables both simulators to run at their optimum speeds while handling feedback between the analog and digital elements. It also solves the problems imposed by the ambiguities of "X," or unknown states that can occur at the interface between analog and digital logic circuits.

The system is engineered so that the combined simulator takes inputs from a single EDIF netlist. EDIF, the Electronic Design Interchange Format, is an ASCII data format that lets work stations with a diversity of internal data representations access common files of design objects. The use of an industry-standard netlist provides users with the flexibility to interface any computer-aided-engineering system with Saber/Cadat.

The majority of today's mixed-mode problems involve large-scale complex systems with tightly integrated feedback structures and complex devices such as microprocessors and phase-locked loops; circuit-level devices such as diodes and transistors; and non-electrical elements such as motors and actuators. Thus, the mixed-mode simulation solution must be sophisticated and robust. Saber/Cadat provides such a solution by handling digital elements of the design with an event-driven digital simulator and analog elements with a matrix-solution analog simulator. The two are closely coupled, with accurate interfaces between the analog and digital parts. In addition, both can use high-level behavioral and hardware models to shorten run time.

The two simulators are synchronized by the proprietary algorithm dubbed the "Calaveras Algorithm" (see fig. 1). "Instead of slowing the process by forcing the simulators to work in lockstep, we allow the analog simulator to leap ahead of the digital simulator whenever it can," says David Smith, Analogy vice president. "This is important in making the simulation run efficiently. We named the algorithm after the site of the celebrated frog-jumping competition because we wanted to imply a grander concept than mere leapfrogging."

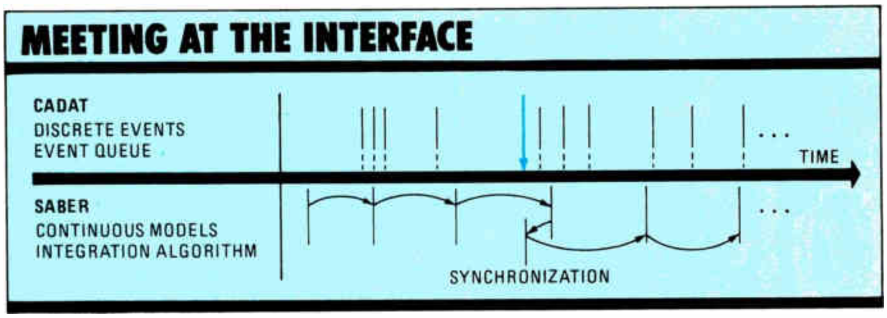
When working in lockstep, Smith explains, the analog simulator is constrained in how far forward it can go in the simulation by where the next event occurs in the digital simulator. "That means the analog simulator is always going to be taking significantly smaller time steps than it needs to to reach its solution, thereby increasing the simulation time. So what we wanted to do is to allow the analog simulator to progress as far forward in time as it can, based on the error criteria specified by the user, and then respond with any change necessary to that solution only when a significant event occurs in the digital simulator. If anything happens, then the Calaveras algorithm provides a technique to back up without doing backtracking—going back to the beginning of the simulation and starting from scratch—to find a solution where something did happen."

Once the issue of synchronization was solved, the issue of how users describe their circuits, and in particular how they describe the analog/digital interface, was facilitated by the choice of simulators. Interface mechanisms are intrinsic functions built into both Saber and Cadat modeling languages. This allows any required interface to be developed at the behavioral level. Where an analog/digital interface occurs in a circuit, nodes are split into two interface models, one digital and one analog. The EDIF netlist is automatically split, and interface models are automatically inserted.

At the interface, the software represents correct current flow and loading by dealing with reactances, drive strengths, threshold levels, exception handling, and level translation. Warnings are given when limits are exceeded.

Handling the X state is another important interface issue (see fig. 2). In essence, there are four reasons that X states exist. One is that logic simulators do not initialize every node. This results in many nodes being set to "unknown" at the start of a simulation. Another is that two signals tied to a single node may be in a state in which one is driving a one and the other a zero. This creates a conflict in which the the actual status of the node is unknown. The third occurs when two signals on the input of a device transition simultaneously. For a period of time, the output will be in an unknown state. Finally, a node may oscillate between zero and one with zero delay in the logic simulator.

In all four cases, a digital simulator sets the node to the X state. In addition, the simulator will minimize the propagation of X in many cases. Saber/Cadat's analog side also minimizes the propagation of X.



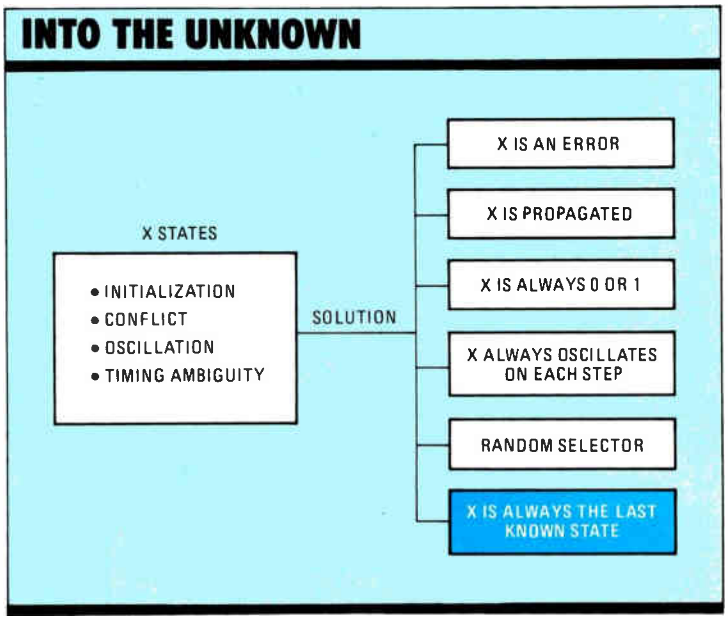
1. The Calaveras algorithm synchronizes Cadat's event-driven simulation (above the line of the interface) with Saber's matrix solution (below the line).

If the X state were allowed to propagate, every analog output could potentially be driven to X, and with feedback to the digital part of the system, X could appear everywhere. Users would burn up a great deal of simulation time only to obtain an ambiguous or useless result.

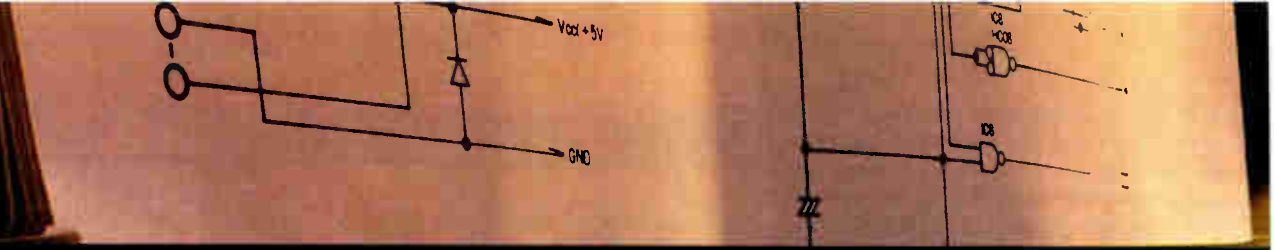
Instead of indiscriminate propagation, Saber/Cadat simply flags the operator and deals with the X state as a specific analog condition. That is, it leaves the affected node at its last known state, if there was one, or it arbitrarily selects a value of one or zero if the node was initialized to X.

Beta-site testing of Saber/Cadat is now under way at Rockwell International Corp., which is also providing product specifications and guidelines that will ensure that Saber/Cadat fits the requirements of systems designers. Racal-Redac of Tewkesbury, England, is providing input on development of both the digital and analog simulators and in the specification of the Saber/Cadat interface. It has integrated Saber/Cadat with the schematic-capture and data-analysis packages that are part of its Visula line of electronic design-automation systems. The full release of Saber/Cadat will be available at the end of 1988. *–Jonah McLeod*

For more information, circle 483 on the reader service card.



2. Saber/Cadat handles the X state as it occurs by leaving the affected analog node in its last known state and flagging the user.



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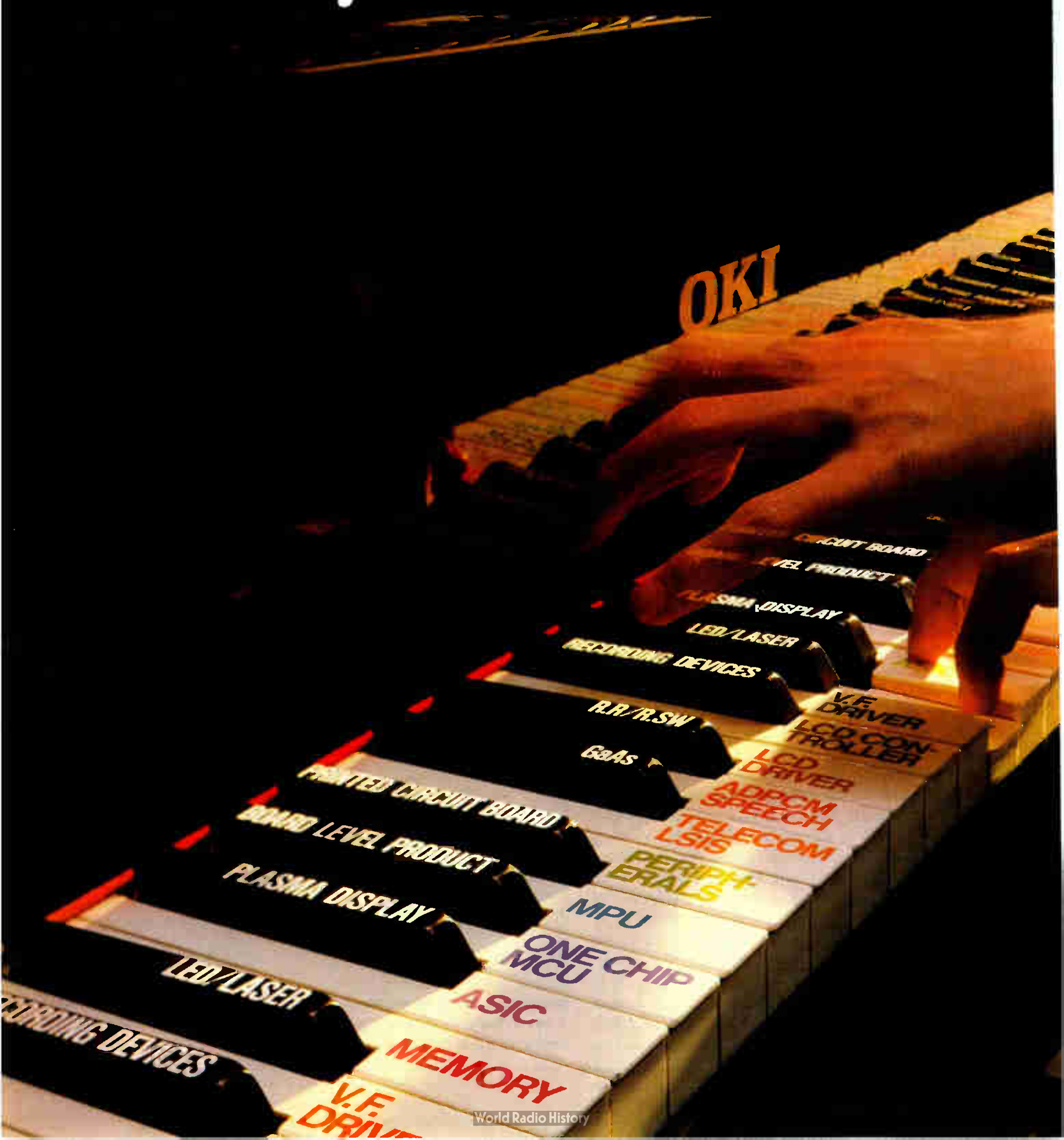

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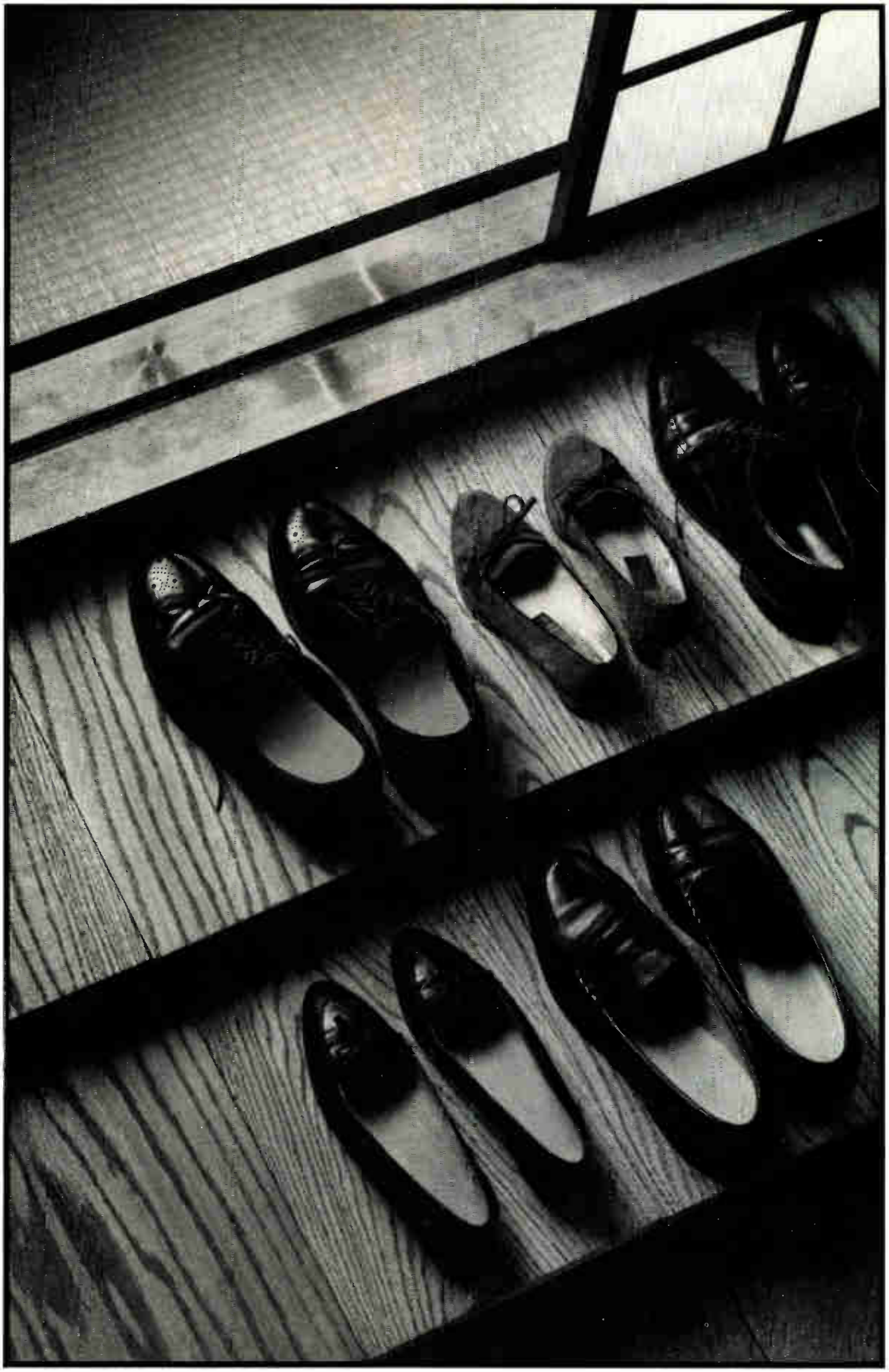

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A FULL-COLOR EL DISPLAY IS DEMONSTRATED BY PLANAR

The flat-panel unit uses a stripe-patterned phosphor complex to create eight colors

The first public demonstration of a full-color electroluminescent flat-panel display is taking place May 23-27 at the Society for Information Display show in Anaheim, Calif. The prototype EL display from Planar Systems Inc. uses red, green, and blue phosphors that are bright enough to create a small pixel pattern of three color stripes to produce full-color images. The Beaverton, Ore., company has also developed symmetrical-drive electronics to control the tricolor pixels.

The prototype displays demonstrated at SID were developed for the U. S. Army and have a 320-by-240-pixel matrix. Each pixel has three subpixels—one for each color. The active display area is 4.8 by 3.6 in. (see photo) and the pixel pitch is 0.005 in., resulting in a resolution of 200 lines/in. The demonstration panel interfaces to a standard personal computer with a commercially available display controller.

The prototype displays deliver only eight colors because there is no gray-scale control to vary each color subpixel's intensity—the subpixels are either on or off. A frame buffer can capture the display information coming from the data source, however. It is possible, therefore, to utilize what is called a frame-sequential gray-scale technique as well as pixel dithering to achieve a somewhat wider palette of colors.

On a longer-term basis, Planar is working on improving driver electronics for true gray scale to develop a much wider array of colors. The company is developing column drivers that vary the intensity of the colors by changing the frequency of the ac voltage applied. The goal is to provide four bits of gray scale information to produce 16 levels of gray scale for each color. Doing that would yield a color palette of 4,096 colors.

The color phosphors, the patterned-phosphor structure, and the electronics to support multiple colors were developed under two contracts with the Army's Electronic Technology and Devices Laboratory, at the Laboratory Command Division (Labcom) in Fort Monmouth, N. J. The Army is using the prototypes in a variety of battle-management-system experiments.

Planar is now working with the Army on improving the manufacturing process and reducing costs. The company's objective is making color EL displays that will eventually cost only 25% to 50% more than what monochromatic EL displays are expected to cost in a couple of years—historically, monochromatic display costs have been dropping by about 20% every year. Planar expects that the full-color flat-panel displays will be available in two or three years, says Roland van Stroh, vice president of marketing and sales.

Planar's research progress was already in evidence last year when it delivered prototypes of a stacked-phosphor limited-color display to Labcom [*Electronics*, May 28, 1987, p. 63]. To develop full-color EL displays required painstaking research for phosphors that would produce red, blue, and green light in intensities bright enough to use small pixels. The easiest phosphors to develop were the red and green ones. The big challenge was improving the blue phosphor.

A fundamemental limitation in building multicolor EL displays has been in the low luminance and efficiency performance of color phosphors, except for the yellow-emitting, maganese-doped zinc sulfide, used in today's commercial monochrome displays. All EL phosphors consist of a host material—typically ZnS—and a light-emitting dopant called an activator. Rare earth fluorides are most often used as activators. The concentration of the activator is on the order of 1%, which is several orders of magnitude larger than dopant concentrations found in semiconductor transistor devices.

The limited-color display Planar first developed used only red and green phosphors and it was practical to stack them on top of each other to achieve a small pixel. For three colors, however, stacking them was impractical. So Planar scientists and engineers switched to the three-strip patterned phosphor scheme used now. The scientists are still working on improving the phosphors, especially the brightness of the blue one.

Planar uses a reactive-ion etching technique to lay down the pattern of red, green, and blue thin-film electroluminescent phosphors. The red and green phosphors are produced using rare earth fluorides to dope zinc sulfide—$ZNS:SMCl_3$ for red and $ZnS:TbF_3$ for green. The struggle to achieve a blue phosphor with enough intensity ended when Planar researchers finally hit upon strontium sulfide doped with cerium fluo-

Eight colors are produced in Planar's color electroluminescent display from a stripe-patterned phosphor complex of red, green, and blue phosphors.

ride (SrS:CeF_3). The individual subpixels in the pattern are rectangular with dimensions 3 mils by 11 mils.

The driver electronics consist of a common row electrode for all three subpixels and individual column electrodes for each color stripe. Utilizing this symmetric-drive technique for independent control of the three modulation voltages allows for the variations in the three phosphors' threshold voltages—currently up to a 10-V spread. The drive electronics can refresh the panel at rates up to 240 Hz for higher brightness levels and future gray scale.

Both the timing and control signals are driven by software so that variations in drive waveforms and refresh frequency changes can be implemented easily. Drive frequencies of 60, 120, and 180 Hz are possible now with an increase to 240 Hz to follow, Planar says.

For the best color balance for white, the color phosphors need to have the following percentages of the total white brightness: 25% red, 65% green, and 10% blue. Planar's current state of the art for 60-Hz phosphor luminance is 1.5fL (5%) in the red, 25fL (79%) in the green, and 5fL (16%) in the blue. One way to compensate for the dominance of the green is to narrow the width of the green phosphor stripe, but that lowers the overall brightness. Planar is working on brighter red and deeper blue phosphors for better color balance.

In the first prototype three-color displays, Planar has limited the green brightness to 4fL to achieve a good color balance for white. This results in a relatively low luminance level of 5fL. Planar still achieves a good contrast ratio of 6 : 1 in a typical office environment of 500 lux illumination, however, because of the intrinsically low-diffuse reflectivity of the thin-film EL display and circular polarizer combination.

This high contrast ratio coupled with the wide viewing angle of EL displays yields a quite acceptable display quality, which will be improved significantly by the time the color-EL display is made commercial. When commercial color-EL products are available, Planar expects that they will compete very favorably with color liquid-crystal displays that are just beginning to emerge as well.

Planar's flat-panel color displays will feature the same performance advantages as monochrome EL displays, such as high brightness, sharp contrast, and a wide 160° viewing angle. Because the EL displays are completely thin-film solid-state devices, they offer more endurance and reliability than cathode-ray tubes.

Planar is continuing to optimize the processes for the deposition and patterning of the color phosphors. Specific areas of exploration include new depositing techniques for the insulators and phosphors, innovative etching processes, and new phosphors with increased efficiencies and brightness. *–Tom Manuel*

For more information, circle 484 on the reader service card.

AT SID: A RASH OF R&D RESULTS IN COLOR FLAT-PANEL DISPLAYS

Planar Systems' full-color electroluminescent display technology was just one of the many advances reported in color flat-panel displays at the Society for Information Display conference in Anaheim, Calif., May 23-27. Some other major flat-panel display technologies are on the verge of full color as well. Developments were announced in several full-color liquid-crystal displays and in gas-plasma technology, for example.

In LCDs, there are 11 papers describing research efforts with varying approaches to creating full-color for different applications. There are also five papers that deal with color gas-plasma display technology.

A pair of Japanese companies are working on multicolor supertwisted-nematic LCDs and one company is working on a color ferroelectric LCD. But the bulk of the color-LCD work is being done with active-matrix LCD technology, where thin-film transistors for driving each pixel are fabricated right on the display.

Sharp Corp. in Nara, Japan, is presenting a prototype model of a 200-by-384-dot color display using a double-layered supertwisted nematic process. And the Asahi Glass Electronic Products R&D Center in Yokohama, Japan, is revealing a 9-in. diagonal color display that combines transparent electrodes on micro color filters with a black and white double-layer supertwisted-nematic LCD. Meanwhile, Toshiba Corp., also in Yokahama, describes a large-area, 12-in., 400-line LCD driven at video rates. It employs RGB filters in a black matrix to increase contrast.

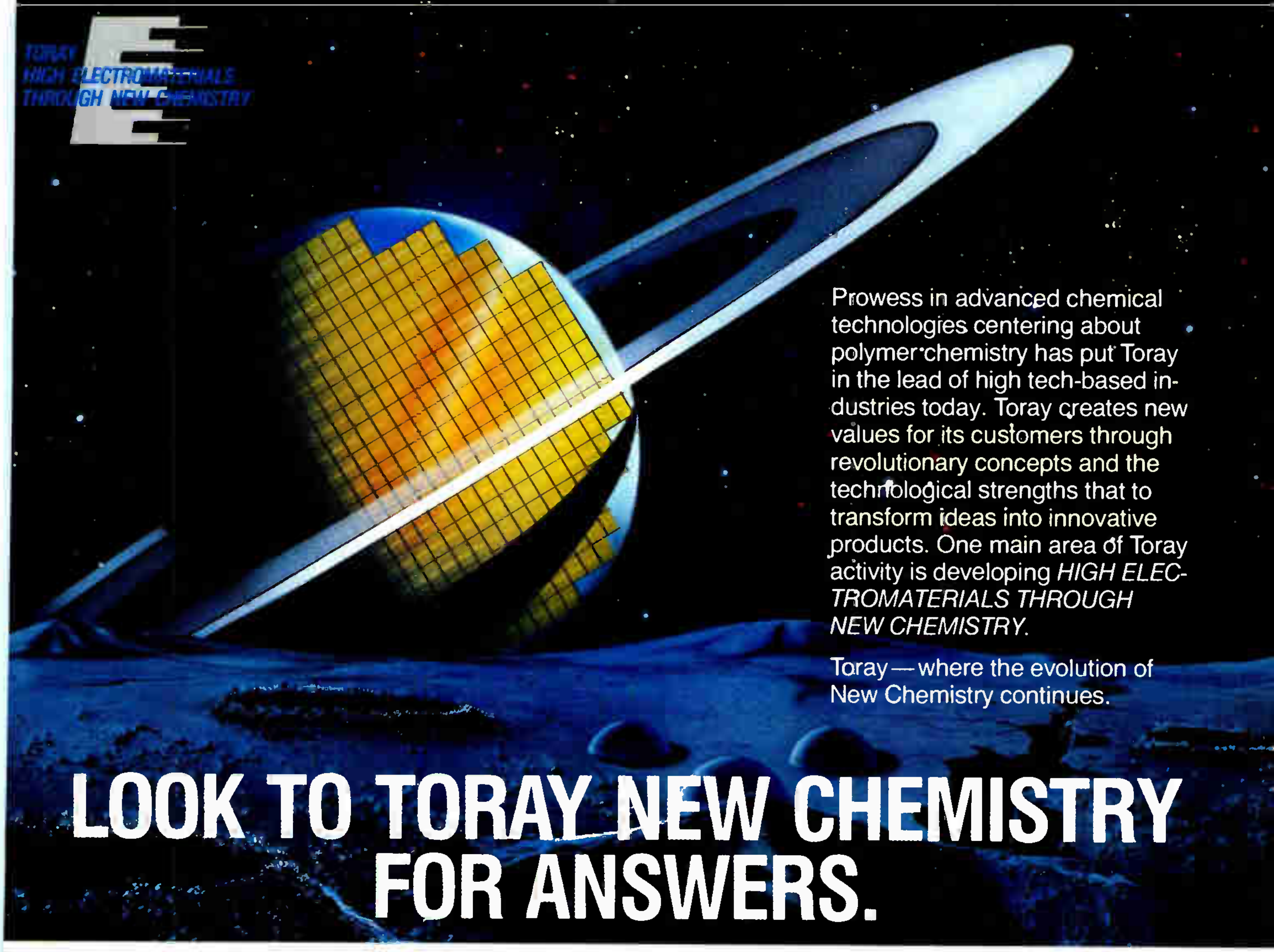
No fewer than eight developments in active-matrix color LCDs—the most active area for color flat-panel display research—are reported at SID. This time, they are not all in Japan. Three papers are from General Electric Co.'s Corporate Research and Development laboratories in Schenectady, N. Y. The GE researchers have demonstrated a thin-film-transistor driven color LCD with one million pixels (1,024 by 1,025) in a 6.25-in. square format.

Another paper describes GE's pilot fabrication line for this and a 4-in.-by-4-in. (400 by 400 pixel) color LCD. It features a simple four-mask thin-film transistor process. The third GE paper describes the use of custom-blended triphosphor RGB fluorescent lamps to provide the optimum backlighting for color LCDs.

The Japanese active-matrix color LCD projects include a 5-in. diagonal, 309,000-pixel display from Sharp, another 5-in. display at lower resolution (115,200 pixels) from Hitachi Ltd., Yokahama, and a big 10-in., 640-by-450-pixel panel from Mitsubishi Electric Corp. in Amagasaki. Two other Japanese companies are also doing work on active-matrix color LCDs. Stanley Electric Co. of Yokama is demonstrating a 6-in. color display for avionics and Oki Electric Co., Tokyo, has developed a 9-in. display panel using high-mobility thin-film transistors.

Meanwhile, gas-plasma display technology is not standing still. Plasma is suitable for making very large flat-panel displays and now the players in this technology are starting to add color.

NHK Science and Technical Research Laboratories, Tokyo, report a 20-in. diagonal color plasma display with 640 by 448 pixels. Progress in research to develop technologies for color plasma displays is reported from three sources—Bell Communications Research, Red Bank, N. J., Hiroshima University in Higashi-Hiroshima, and Thomson-CSF in Boulogne-Billancourt, France. *–Tom Manuel*



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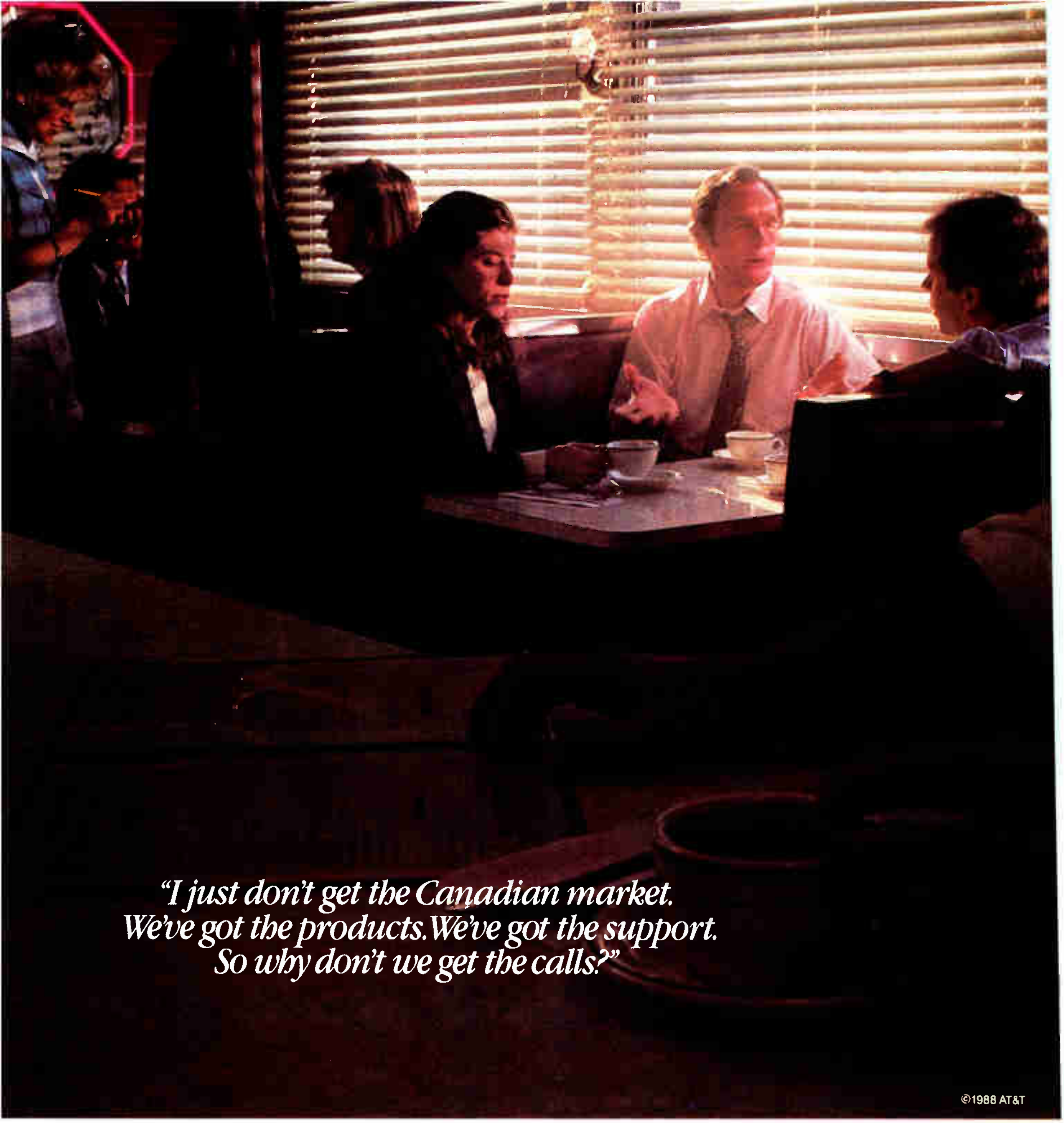

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GROOVED BOARDS CHALLENGE CONVENTIONAL PC BOARDS

Dimensional Circuits' 3-d trace geometry can carry the current required by today's board assemblies

Since the rigid printed-circuit board first appeared, the standard board interconnection geometry has been based on a planar trace with a rectangular cross section. But as geometry gets finer, planar traces often cannot handle the growing use of surface-mounted components and the higher power densities of today's board assemblies—the fine lines don't have the current-carrying capacity.

Now engineers at Dimensional Circuits Corp. in San Diego have come up with a molded circuit board using a new, three-dimensional trace geometry that overcomes the disadvantages of conventional geometry. It does so by combining rectangular grooves that are molded into the board or substrate surface with a U-shaped cross section. The technology is implemented in the latest platable high-temperature thermoplastics. The combination means circuitry can be manufactured with high interconnect density and good current-carrying capacity in a form that allows self-location of component leads.

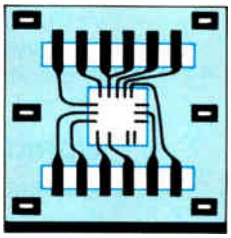
Molded circuit boards are not in themselves a breakthrough, but so far they have been developed mostly by molding houses or raw material suppliers. Their usual practice is to make ordinary trace cross sections. Metallization is not recessed significantly—no grooves, only shallow channels, whose top is flush with the surface. Thus, the electrical and mechanical advantages are often minor. The incentive offered has been reduction of manufacturing cost, particularly in assembly, rather than providing a flexible engineering solution.

Dimensional Circuits' new plastic boards, by contrast, can be designed as replacement parts, which do not require significant changes in a customer's manufacturing equipment or technique. And because they are flat, the tooling cost is considerably lower, as only the grooves have to be tooled and simpler molding techniques can be used.

This new type of circuit trace has been developed and tested as a design option for special applications, particularly in surface-mount technology and power electronics. It uses the third dimension—depth, in the form of subsurface, vertical sidewalls into the substrate—to provide unique properties with notable implications for circuit designers and manufacturing personnel in tackling prevailing electrical and mechanical challenges.

The technology offers two major features (see fig. 1). First, the deep, plated, U-shaped qrooves—typically 5 mils wide and 15 mils deep—that are used as traces can contain significantly more conductive material, by an order of magnitude or more, with no increase in the area of the board surface. Second, the technology provides a fixturing/self-locating effect when fine-pitch component leads are inserted into the grooves for assembly and soldering. In addition, the same technique that allows Dimensional Circuits to mold the narrow grooves can also be used to mold recessed cavities that can house entire devices, such as passive components.

These advancements form the basis for the design and manufacture of cost-effective molded circuits—the grooves and sunken pads are molded in at no extra cost per unit. They also provide advantages for products such as surface-mounted assemblies and power-conducting boards that use automated assembly and soldering or need high conductivity.



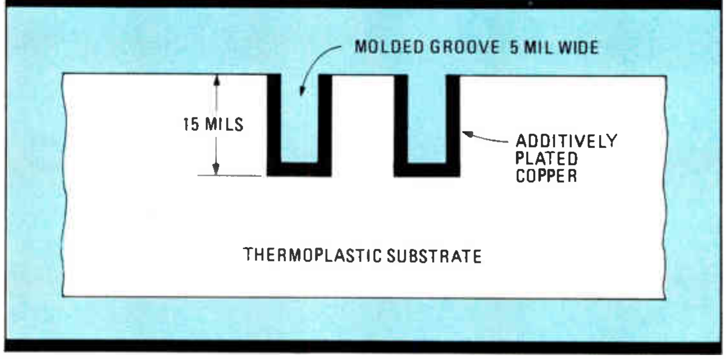
An important aspect of grooved metallization is that the electrical path in the grooves is along both sidewalls and the bottom of the groove. This allows as much as five to 15 times the amount of metallization per unit of surface area as ordinary pc-board technology (depending on groove depth and whether the groove is subsequently filled with copper or solder).

Other merits of the new molded dimensional circuits are their precise tolerancing of package/circuit features such as pads, holes, and especially the metal lines in grooves—±0.001 in. is possible. Also, traces cannot short by "whisker" growth, since all metal is below the surface.

The vertical traces eliminate several manufacturing steps in surface-mount attachment. For example, elimination of solder mask may be possible, as well as solder paste applications, drying, and the use of solder reflow equipment.

A direct result of the grooved circuitry is a potential for higher density by eliminating annular rings around through-holes. The increased metallization on the groove sidewalls can be designed to smoothly enter the through-hole. In addition, solder typically fills the groove completely. Finally, the grooved traces are extremely resistant to handling abuse—the sunken traces cannot be easily be broken.

A GROOVED CIRCUIT BOARD



1. Dimensional Circuits' circuit-board technology is based on grooved traces molded into a thermoplastic substrate and then metalplated.

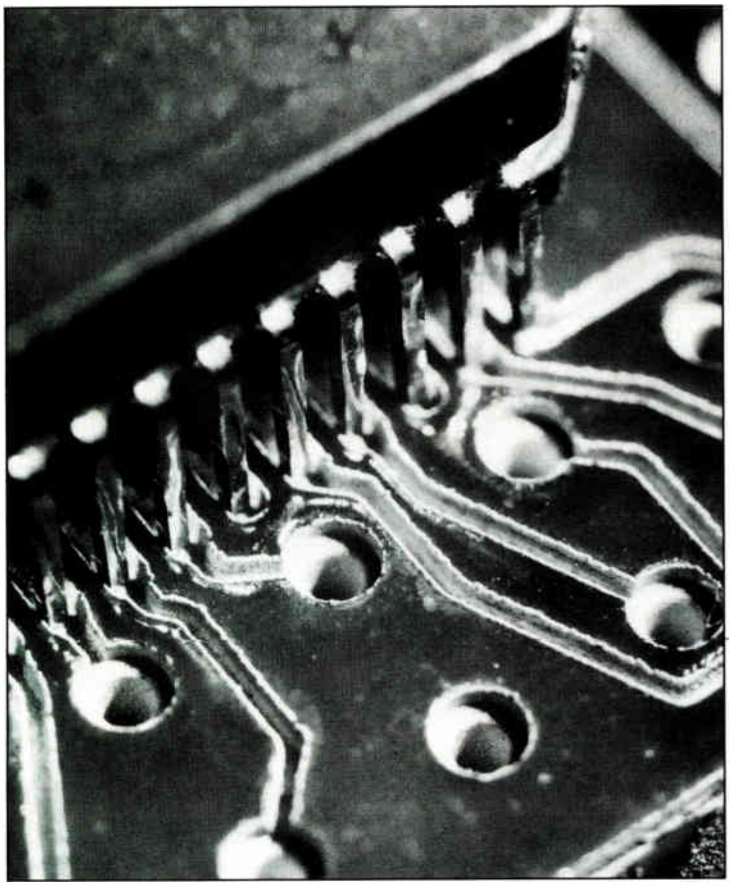
The precise nature of the grooved traces result in better electrical characteristics. Precise spacing of the grooves results in tight control of signal and ground spacing resulting in a controlled impedance and capacitance control. For even higher conductivity, grooves can be deepened. Finally the 5-mil grooves, comparable to pc traces on today's fine-line pc boards, allow for a high-density interconnect.

Some applications that could take advantage of dimensional circuits are pin grid arrays and leadless chip carriers. In the case of the leadless chip carrier, it could be soldered directly to a board of the same thermoplastic material, eliminating any problems with temperature coefficient of expansion between the carrier and the motherboard.

WORKING WITH TAB

Another possible application would be to mount a tape-automated-bonded chip to the grooved traces. The delicate outer lead beams of the TAB chip would be self-aligned into the grooves. Adapters to convert fine-pitch IC packages to a 100-mil grid pinned or leaded package are still another possible application.

Boards capable of carrying high currents are another area where grooved circuits may find a niche, particularly in high-power-density switching supplies. Dimensional Circuits, in fact, is currently in the midst of producing a board for a switching-power-supply application. In such applications, the thicker copper and resulting higher conductivity of the technology is the key. A measure of design of switching power supplies is the number of watts of output per cubic inch of volume. Thicker copper for better conductivity has been difficult to obtain previously because of the limitations, such as excessive undercutting, of the subtractive etching processes used to make conventional circuit boards. The additive process for plating grooved circuits is limited only by the thickness of the substrate itself and the depth and width of the grooves.



2. Fine pitch leads can be accurately self-aligned in the grooved traces, allowing surface-mounted components to be wave soldered.

The new 3-d trace would not be possible without high-temperature thermoplastic materials—among them as polyethersulfone, polysulfone, and polyetherimide—which are capable of withstanding the soldering temperatures required in electronics production. In addition to matching the major characteristics of ordinary epoxy-glass circuit-board material, these thermoplastics have the considerable advantage of being suitable for molding.

Since they were designed specifically for molding, grooved boards bring the cost, quality, and flexibility advantages that come with plastic molding processes. Enhanced formulations of thermoplastic materials are now available with exceptional characteristics—platability, dimensional stability, and a lower dielectric constant than that of epoxy-glass.

Many of the applications for molded/plated circuits that seem practical actually would not be—they would use ordinary methods for tooling and plating, which have been difficult to justify and produce in the past. The relatively few applications in high-density, fine-line circuits have been successful only because the volume is high enough to offset five-figure tooling costs.

One such application, which is now being produced with the grooved-trace method, is a pin-grid-array adapter from Northern Telecom Inc., Nashville. Northern Telecom's small board converts a plastic leaded chip carrier on 30-mil centers to a pin-grid array on 100-mil centers (see fig. 2). The leaded chip carrier is mounted on an adapter board using grooved traces to self-locate the device, thereby improving yields dramatically. In addition, using the grooved-trace method allowed the manufacturer to hand-mount up to 1,200 ICs per hour and completely eliminate solder paste, as molten solder was able to flow up from below and wick up the pre-tinned grooves. This allowed the assembly to be wave soldered using ordinary equipment, rather than reflowed.

Unlike the rest of the companies making molded circuit boards, Dimensional Circuits is concentrating on making a high-density planar board rather than focusing on boards with 3-d features such as built-in connectors, ribs, bosses, and so on. The company's proprietary advances in tooling technology and alternative molding techniques have brought the tooling cost and lead time on planar boards down to less than one-tenth of what was previously expected. Tooling is generated from ordinary circuit artwork. It is now feasible, in specialty applications, to use molded boards with dimensional (grooved) circuit features as an economical alternative to conventional circuit-board technology. *–Jerry Lyman*

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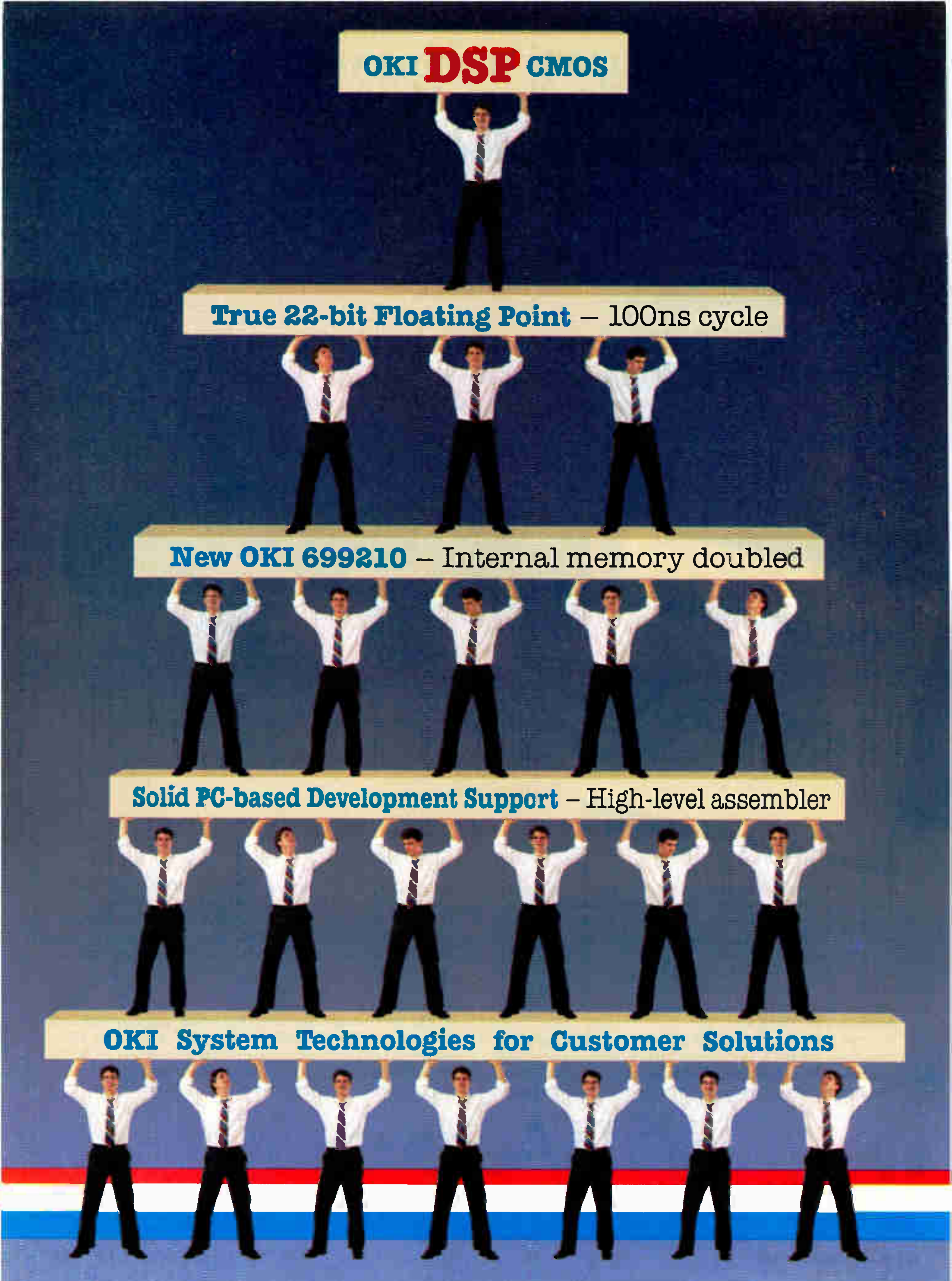
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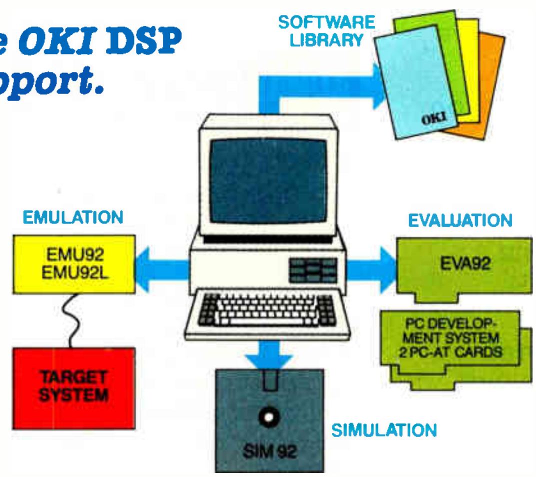

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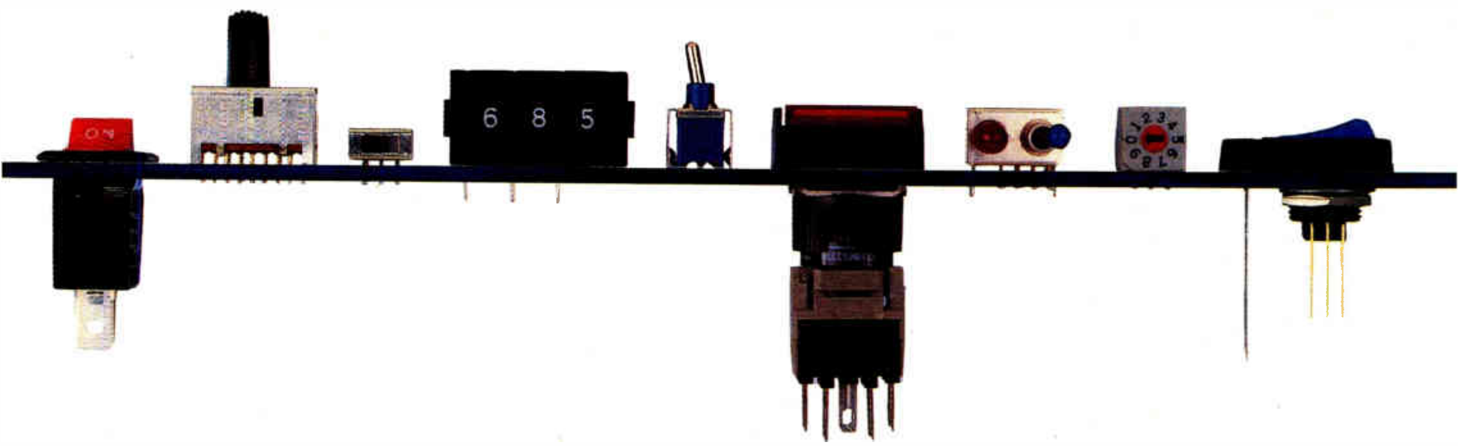

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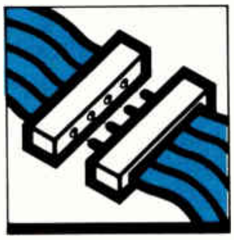
TECHNOLOGY SERIES

SPECIAL REPORT: CONNECTORS FOR PC BOARDS GET SMALLER AND DENSER



Driven by VLSI technology's component density, connectors are turning to surface mounting; manufacturers are looking for ways to reduce or eliminate gold content and cut out soldering

By Gene Heftman, *Contributing Editor*

To match the component density of VLSI-based systems, printed-circuit-board connectors are getting smaller, offering more contact points, and turning to surface-mount technology. For that reduced size and greater contact density, they are moving towards so-called half-pitch 0.05-in. (50 mils) spacings between contacts and pins. Although most pc-board connectors still have full-pitch 0.1-in. (100 mils) spacings, the market share for these conventional types will steadily shrink as high-density applications increase. At the moment, 50-mil pc-board connectors account for only 15 to 20% of the total U. S. connector market, but that share is expected to double over the next two years. Moreover, 50-mil units are already fairly well-established in the Far East.

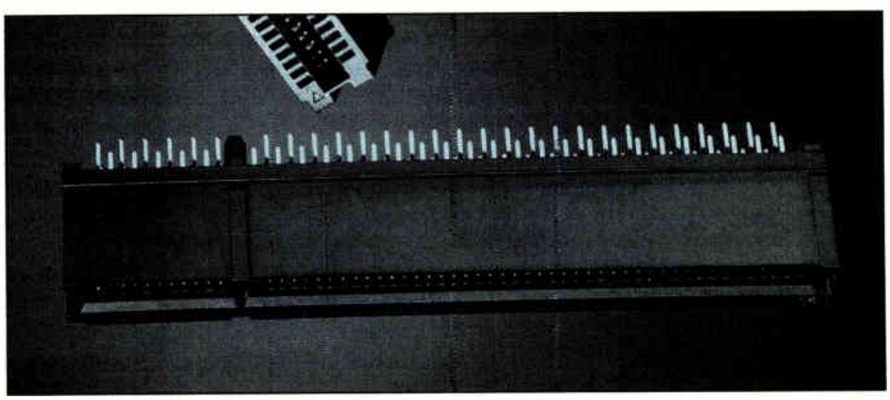
In the coming years, surface mounting will become increasingly important for pc-board connectors. Although surface-mount units are available, they do not yet come in the wide variety of types and configurations as through-hole units. In fact, all surface-mount connectors account for only about 5% of the total connector market. Growth has been slow because surface mounting for connectors is still in its formative stages, so standards have yet to be established for factors such as lead configurations, hold-down methods, and handling by automatic-placement machinery.

Despite the relatively small market size, there is an extraordinary diversity of high-density 50-mil pc-board connectors (see table, p. 85) already available in both through-hole and surface-mount styles. Single-piece card-edge connectors handle board-to-board interconnections, while two-piece pin-and-socket and plug-and-receptacle types mate boards to boards and boards to cables. Moreover, pin counts can range anywhere from tens to hundreds of contacts, and a variety of termination methods are possible, including crimping, wirewrapping, or soldering.

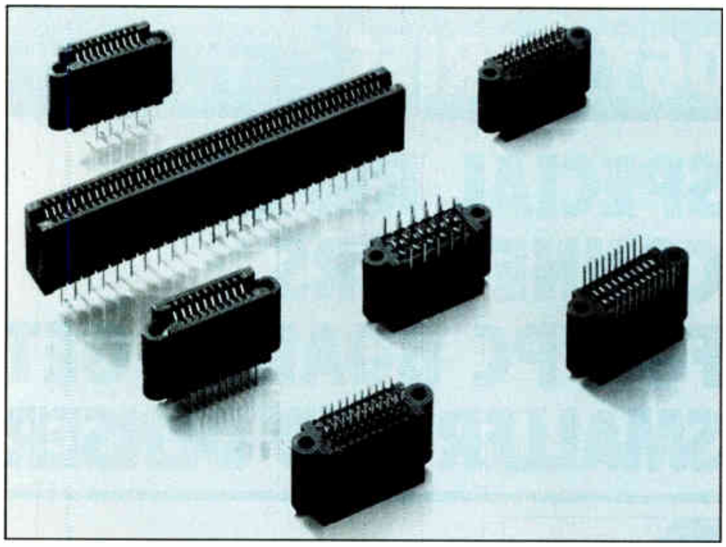
Due to substantial increases in the price of gold over the last two years, connector manufacturers and users alike are looking for ways either to reduce gold content or to eliminate it. Leading the way in that effort is the P-5.1 subcommittee on connectors of the Electronic Industries Association. Recently, the group obtained approval from the U. S. military to cut the gold plating on MIL-C-39029 contacts by one-third—from 75 microinches to a minimum of 50 microinches. The subcommittee is also evaluating the performance of contact finishes other than gold, but has yet to make any firm recommendations. The lower gold content of military connectors could be a bellwether for a comparable reduction in commercial products, which usually employ 30 microinches of gold over 50 to 75 microinches of nickel.

Just as the search is under way for alternatives to heavy gold content, so are ways being sought to eliminate soldering, which can cause problems in high-pin-count systems that involve multiple terminations per pin. In through-hole technology, soldering is being displaced by press-fit or compliant-pin methods, which rely on pressure to provide dependable and long-term metal-to-metal contact between the connector pins and the pc-board's plated-through holes. Once the pin and the board are pressed together, the design of the contact provides the elastic energy needed to maintain sufficient pressure at the interface.

Microcomputers, in particular, influence the configurations of high-density one-piece card-edge connectors for linking one board to another. To handle both busing and memory interconnections in these increasingly complex machines, connector makers are start-



1. These card-edge 50-mil connectors from AMP offer up to 91 dual contacts, which top off a plating of nickel and palladium with a flashing of gold.



2. Designed for through-hole mounting, Methode's 50-mil card-edge connectors offer from 5 to 50 dual contacts.

ing to tailor their parts to the family-like internal structure of the microcomputers themselves.

In many cases, the basic interconnection medium is a backplane or motherboard. Connecting to the motherboard are one or more daughtercards, which in turn can spawn granddaughter boards. Each of these bus-type interfaces requires a connector of some type.

Such a family structure for microcomputer applications is evident in Burndy's new high-density connectors, named Computerbus to clearly indicate their primary function. The 50-mil card-edge units are designed to mount compactly in through-holes on the backplane of a microcomputer and to accept optional

Connector makers are starting to tailor their parts to handle the increasingly complex interconnections necessary for buses and memory in microcomputers

memory cards. The connectors contain two rows of 2 to 120 positions, thereby allowing a minimum of 4 contacts and a maximum of 240 contacts. Standard contacts are plated with palladium-nickel and then flashed with gold, while the solder tails that mate with the backplane are plated with a minimum of 50 microinches of nickel. To withstand the heat of vapor-phase reflow soldering operations, the connector bodies are made with a special plastic that can take temperatures as high as 215°C.

In the same family way, the series FCN224J and FCN225J card-edge connectors from Fujitsu America permit daughtercards to be mounted either in line with or perpendicular to a motherboard. Designed for through-hole mounting, the motherboard termination pins are solder types. The parts come in nine different sizes, ranging from 30 to 120 contacts. Contact plating is a combination of metals—gold over palladium over nickel—a combination that is becoming increasingly popular as a substitute for heavy gold coverings. Likewise, the 50-mil card-edge connectors from AMP (see fig. 1) also employ a combination of gold-palladium-nickel plating for their contacts. Called Duragold, it consists of a nickel-barrier plating followed by a pure palladium plating and topped with a flashing of gold. The connectors, which are intended for small systems such as personal computers, offer 56, 66, or 91 dual contacts.

When a card-edge application requires heavy gold contacts, Texas Instruments believes that its cladding process offers performance superior to conventional plating techniques. The process uses pressure to bond wrought gold to a spring-like base material. The bonding process begins by rolling long strips of hard 18-carat gold foil onto the base metal, followed by annealing to complete the bond. Subsequent rolling of the composite material under high pressure reduces it to the desired contact thickness. The result is a gold surface that is smooth, virtually nonporous, and highly resistant to abrasion and corrosion. At the point of contact, gold thickness is a minimum of 50 microinches—much thicker than the approximately 20 microinches or less of flashed gold.

Also targeting microcomputer applications, Methode Electronics recently introduced a series of high-density, 50-mil card-edge connectors for through-hole mounting with standard 0.062-in.-thick pc boards. The series 240 units (see fig. 2) have 5 to 50 dual contacts, which are formed from a copper alloy that is selectively gold-plated. They are designed for handheld electronics equipment such as portable computers, mobile telephones, and test instruments.

A variety of two-piece pin-and-socket and plug-and-receptacle connectors allows users to interface one board to another or to connect a cable to a board. Besides offering a choice of mounting styles, these parts can accommodate a variety of interconnection configurations. For example, the Mini 50 series of 50-mil plug-and-receptacle connectors from ITT Cannon can handle either inline or right-angle interconnections. Plugs and receptacles are both designed for through-hole mounting and come with or without mounting flanges. Sizes range from 20 to 100 contacts, and users can select the amount of gold plating—gold flashing, a minimum of 25 microinches, or a minimum of 75 microinches. One of the series even provides power and ground contacts in the flanged portion of the connector housing. While the signal contacts are rated for 0.5 A, the heavier power and ground pins can handle up to 2 A.

Either through-hole or surface-mount 50-mil connections are possible with the two-piece board-to-board connectors made by DuPont Connector Systems. Ten two-row models are available that provide from 10 to 100 contacts. Designed for high-density systems, a typical 50-mil connector occupies just one-eighth the volume of a 100-mil connector with the same number of contacts. Because of the small size and low profile of the parts, boards can be stacked tightly. Through-hole versions allow boards to be separated by just 0.225 in., while surface-mount versions let boards be as close as 0.235 in. Both polarized (to ensure proper mating) and nonpolarized models are available.

Those high-density Dupont connectors are based on the company's patented Rib-Cage design, which employs ribbed female contacts on 50-mil centerlines and bullet-nosed male pins. The ribs inside the female contact angle down in the direction of pin insertion, but insertion requires more force than withdrawal because the contact must expand when the pin enters. The number of ribs determines the insertion and withdrawal forces—the more ribs, the greater the forces. The structure yields low contact resistance—only about 9 to 10 mΩ. The contact material is 0.003-in. mill-hardened beryllium copper, plated with 30 microinches of gold.

Despite the fact that 50-mil connectors are considerably smaller than their 100-mil counterparts, they may still not be small enough for some handheld electronic equipment because the size of their envelope is too large. To meet the needs of such compact equipment, Molex makes what it claims is the smallest two-piece 50-mil board-to-board connector on the market. When mated, the connector measures just 0.4-in. high by 0.25-in. wide. Not only that, the connector is hinged so it can rotate 90°. One of the primary applications for the hinged connector is in test or calibration when one board must be rotated with respect to another during checkout. The connector is designed for through-hole mounting with solder terminations. Available with an even number of 4 to 20 contacts, the part has passed 50 rotating cycles and 30 mating cycles.

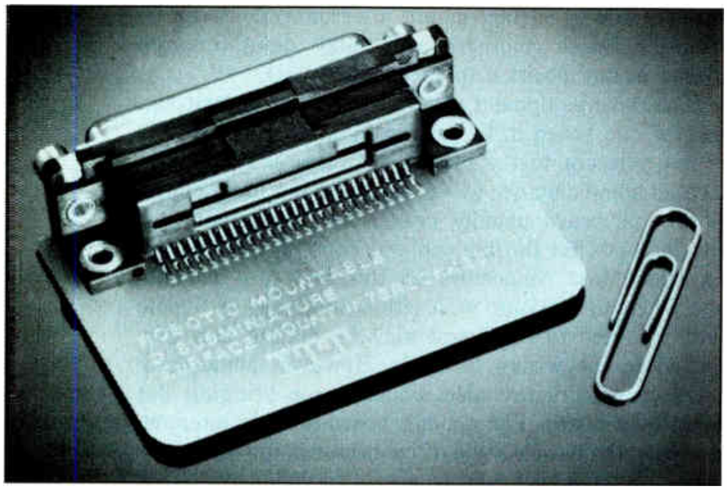
Within two-piece connectors, different manufacturers have different approaches for avoiding soldering. For instance, the compliant-pin technology developed by Thomas & Betts employs a pin that features two flexible contact beams, each of which functions as an independent spring during insertion. Called Flex-Fit, the technology lets a pin provide maximum compliance with minimum permanent deformation after insertion. The company uses Flex-Fit in its 609 series of headers (male connectors) intended for solderless backplane and pc-board applications. Those headers mate with female connectors which, in turn, connect to flat flexible cable. Headers are available in 10 sizes having from 10 to 64 pins, and the connectors offer a lock/eject option for ensuring positive connector latching. The phosphor-bronze contact material has a plating of gold over nickel in the contact area.

To eliminate soldering, Viking Connector uses yet another method for its surface-mount controlled-impedance connector, which matches the impedance of surrounding components at frequencies up to 8.5 GHz. A compression joint makes a connection by exerting a force of 100 g. Surface-mount interconnections can be made between motherboards and daughtercards placed in any position to each other.

Electronic equipment often requires the output signals of one board to be carried to another board that is not adjacent to the driving board or may even be located some distance away. To make the interconnection, a pc board usually uses a two-piece connector that accepts flat flexible cable or some type of wiring harness. Most connectors of this type are pin-and-socket configurations, with either the male or female half mounted to the board and the mating half connected to the wiring or cable. However, some card-edge connectors are also available for bringing flat cable to a board. For making board-to-cable interconnections, the classic style of connector is the subminiature-D type, which now comes in high-density 50-mil

REPRESENTATIVE PC-BOARD CONNECTORS

Company	One-piece	Two-piece		Circle No.
	Card edge	Board to board	Board to cable	
Airborn Inc. Addison, Texas (214) 931-3200	—	X	X	380
AMP Inc. Harrisburg, Penn. (717) 564-0100	X	X	X	381
Burndy Corp. Norwalk, Conn. (203) 838-4444	X	X	X	382
DuPont Connector Systems Camp Hill, Penn. (717) 975-2000	—	X	X	383
Fujitsu America Inc. Lake Bluff, Ill. (312) 295-2610	X	X	X	384
ITT Cannon Fountain Valley, Calif. (714) 964-7400	X	X	X	385
Methode Electronics Chicago, Ill. (312) 867-9600	X	X	X	386
Molex Inc. Lisle, ILL. (312) 969-4550	X	X	X	387
Teradyne Connector Systems Inc. Nashua, NH (603) 889-5156	—	X	X	388
Texas Instruments Inc. Connector Products Attleboro, Mass. (617) 222-2800	X	X	X	389
Thomas & Betts Bridgewater, NJ (201) 685-1600	—	X	X	390
Vernitron Corp. Laconia, NH (603) 524-5101	—	X	X	391
Viking Connectors Co. Chatsworth, Calif. (818) 341-4330	—	X	—	392



3. The subminiature-D connector now comes in surface-mount styles like this ITT Cannon unit, with up to 25 contacts.

versions. For example, Airborn offers a choice of 50-mil subminiature-D connectors in both metal (MK models) and plastic (ML models) housings, with 2 to 4 contact rows and pin counts ranging from 9 to 100. The receptacle half, which requires through-hole mounting, bolts in place with screws and nuts. The mating plug is a right-angle type.

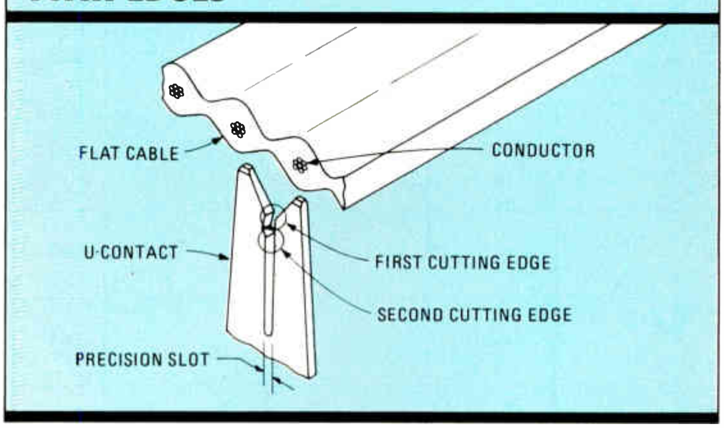
Also employing 50-mil centerlines, the Ribbon family of subminiature-D connectors from Molex accepts standard 28-gauge ribbon cable. They come in three connector sizes of 24, 36, and 50 contacts for either inline (the 71519 series) or right-angle (the 71520 series) interconnections. For 26- or 28-gauge stranded-wire ribbon cable, the 40312 series provides 10, 14, 16, and 20 contacts.

To handle surface-mount applications, ITT Cannon's subminiature-D connectors (see fig. 3) have plastic bodies whose thermal coefficient of expansion mimics that of surface-mount boards. The connector is designed to be soldered in place with the same vapor-phase techniques used to mount other components on a board. They come in four contact configurations consisting of 9, 15, 19, or 25 contacts.

A popular method for speeding and simplifying the linkup between a connector and flat ribbon cable is insulation displacement, which eliminates the need to strip a wire's insulator to make a connection. The cable-mating contacts of an insulation-displacement connector have knife-like edges that punch through the cable insulation to make a connection. Since insulation displacement is a mass-termination technique—all connections are made simultaneously—it is much faster than joining wires individually to contacts. Insulation-displacement connectors are available in a variety of styles, but most have centerlines on 100 mils, rather than 50 mils. Typical are the FCN series of flat-cable connectors made by Fujitsu America, which include card-edge and subminiature-D types. The connectors employ a mass-termination technique that relies on a U-shaped contact (see fig. 4). Two cutting edges in the contact slot ensure a tight connection: one edge first pierces and displaces the cable's insulation, while the other edge strips away any remaining stray insulation. The contacts employ the same combination of plating—gold over palladium over nickel—that many card-edge connectors use. In contrast, terminals that mount to the pc board are plated with solder over nickel. The nickel plating safeguards contact purity by preventing the copper—the base pin material—from diffusing into the dip-solder bath.

The new 9300 series of insulation-displacement connectors from Methode offer a single-inline format with 2 to 30 contacts for accepting individual wires ranging from 22 to 28 gauge in size. Contacts have a phosphor-bronze base with a choice of platings: either tin over copper or selective gold plating. The connector body is a glass-filled polyester that has a high resistance to flame.

TWIN EDGES



4. The U-shaped contacts on Fujitsu's FCN series of insulation-displacement connectors have two cutting edges for quick and reliable mass termination.

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Another way to mass-terminate flat cable or flexible circuitry is with a zero-insertion-force connector. After the ends of the wires have been exposed, the cable assembly simply slips into a slot provided on the connector, and then a sliding lock mechanism on the connector secures the connection. Pushing the slider latch down fixes the conductors in place, and reversing the procedure allows easy removal.

To join pc boards to either flat cable or flexible circuitry, Burndy makes three types of two-piece ZIF connectors with 50-mil centerlines. The SLP series offers from 4 to 20 contacts, the SLEM series from 7 to 30 contacts, and the HLEM series from 7 to 40 contacts. Known as Ziflok, the units eliminate the usual requirement for gold-plated contacts. The geometry of the contacts, which are based on a tin alloy, forms a gas-tight high-pressure connection between the contact and conductor.

For pc-board connectors, the technology trends that will prevail in the coming years are already apparent today. High-density 50-mil centerlines will ultimately dominate the market, and connector bodies will continue to shrink in size. Surface mounting has nowhere to go but up as the appropriate standards emerge. Furthermore, an increasing number of alternatives to gold and soldering will bring increasingly acceptable and comparable results. □

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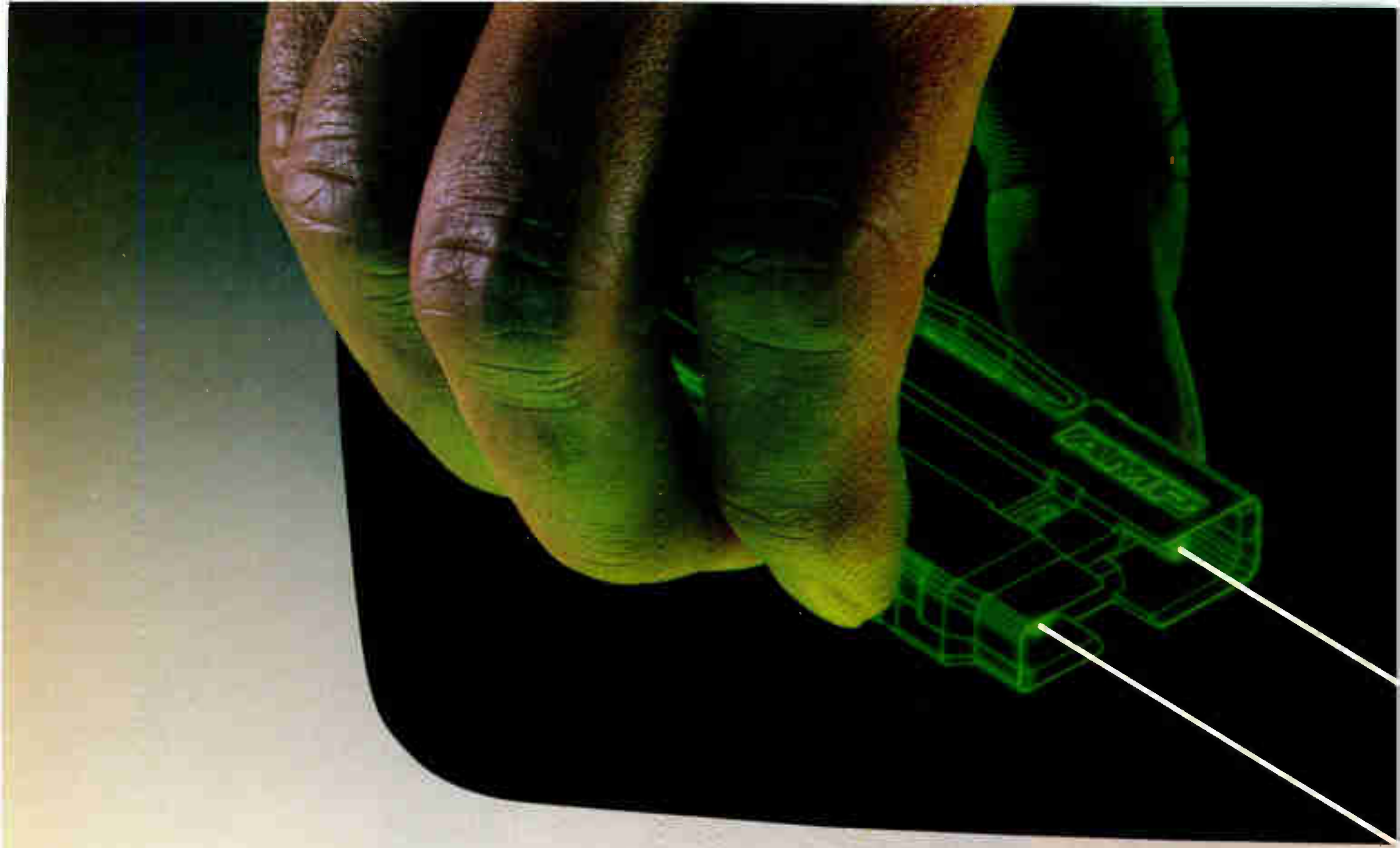

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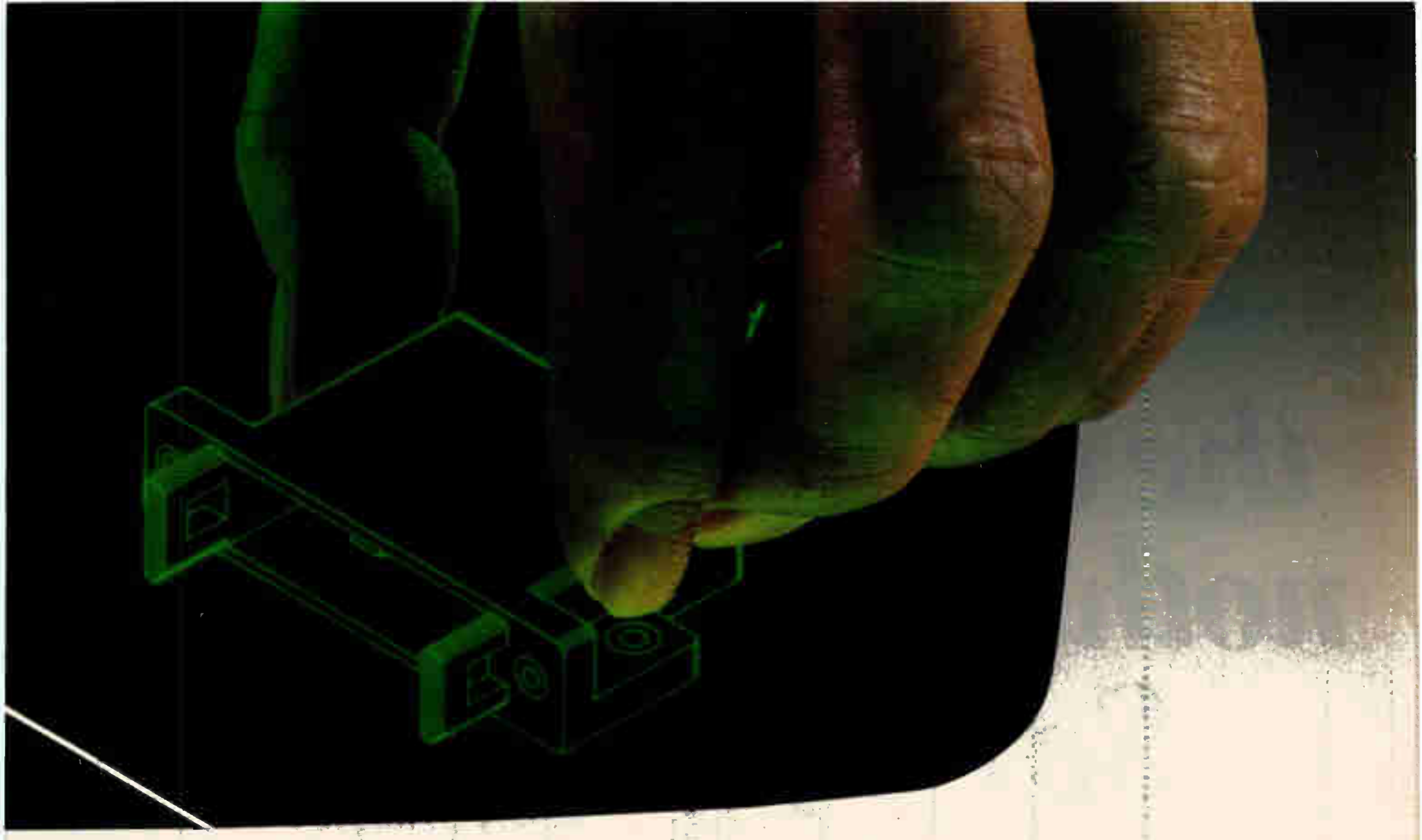

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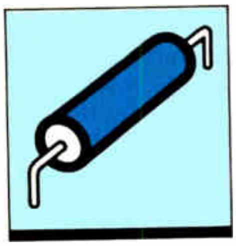


TANTALUM CAPACITORS KEEP GETTING BETTER

Improved materials and manufacturing mean surface-mountable tantalum chip capacitors are squeezing more capacitance and higher voltage ratings out of ever smaller package sizes, as application-specific designs come onstream

By William Hyland and William Kauffman, *Mepco/Centralab*

When the application calls for high capacitance, high performance, and miniature size—all at the same time—surface-mount tantalum capacitors are pretty much the only game in town. And now a number of factors are combining to improve these chips still further.

To begin with, advances have been made in tantalum powder—among them higher powder purity and greater particle surface area—which are increasing volumetric efficiency for smaller physical size with higher capacitance density and higher operating voltages. Additionally, modern manufacturing technology is permitting high-volume production of tantalum capacitors that have consistent electrical characteristics. And finally, improvements in capacitor design are leading to new types of surface-mount tantalums and even to application-specific chips that are optimized for a particular use.

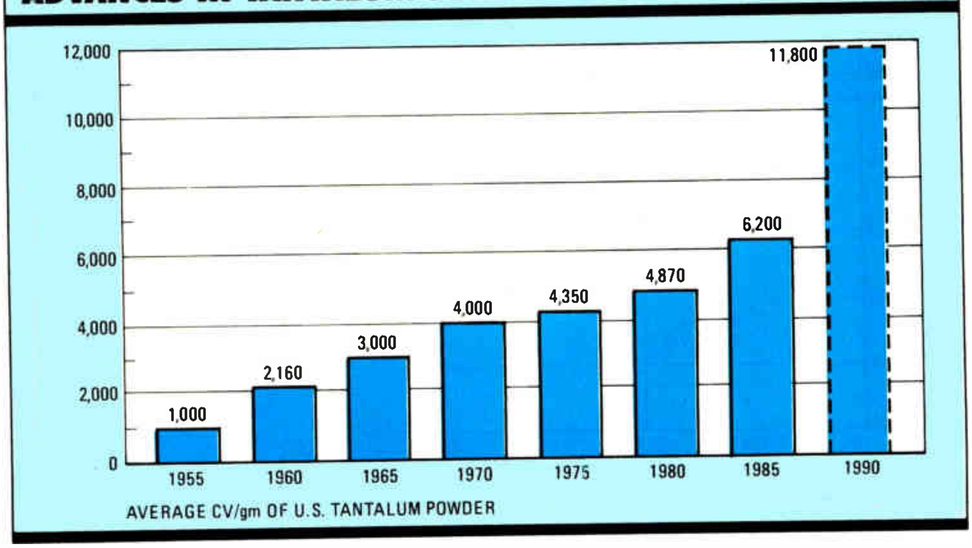
Today, virtually all surface-mountable tantalum capacitors employ a solid electrolyte, with two chip styles dominating—molded and conformally coated. Molded units come encased in a plastic housing, while conformal units come with just a protective coating over the bare chip. That difference may seem small, but it causes measurable differences in performance and size.

To accommodate the multifaceted requirements of surface mounting, both molded and coated tantalum chips offer a variety of shapes and sizes, many of which meet the requirements of military and industry standards around the world. The most widely used capacitance values range from 0.1 to 100 uF, with rated operating voltages of 4 to 50 V dc. At present, 38 different series of solid tantalum chips are available from a total of 21 worldwide vendors, but they have limited interchangeability primarily because of differences in the geometries of their mounting pads.

Dramatic improvements in the purity and particle surface area of tantalum powder have led to a marked increase in capacitance and voltage ratings as chip size has continued to shrink. The telltale parameter for tantalum powder is its surface factor, which is expressed as CV/gm of tantalum. Surface factor is determined by weighing a tantalum anode, electrochemically growing the tantalum dielectric to a certain thickness for a standard voltage rating, say, 100 V dc, and then measuring the resulting capacitance. The product of the measured capacitance (C) in microfarads and the anodization, or formation, voltage (V) for 1 gram of tantalum is the surface factor (CV/gm) for that powder.

Every five years or so, the average CV/gm of tantalum powder increases significantly (see chart). The last five years alone, for example, have brought nearly a 70% increase in surface factor: this has risen sharply from an average of 5,000 CV/gm in 1983 to today's average of 8,400 CV/gm. In general, the particle size of standard-melt powders ranges from 7 to 9 μm at 3,000 to 6,000 CV/gm down to 2 or 3 μm at

ADVANCES IN TANTALUM SURFACE FACTOR



15,000 CV/gm. Current workhorse powders are typically in the range of 6,000 to 12,000 CV/gm and have average particle sizes of 4 to 5 μm. Even now, some powders offer as much as 18,000 to 23,000 CV/gm. However, there is usually a substantial time lag from the point when a new high-CV/gm powder becomes available in volume until capacitor manufacturers are able to adapt their processes to make satisfactory capacitors with it.

Most tantalum powders are agglomerated—that is, they are a fabricated blend of very small and larger particles sintered together to increase the effective surface area of individual particles. Agglomerated powder mixes offer the greatest potential for reducing capacitor size still further for a given capacitance-voltage rating.

The prices of tantalum powder and tantalum wire vary over time, as do the prices of semiprecious metals. For instance, last year, tantalum powder and wire stock ranged in price from $110 to $150 per pound. This year, the prices for tantalum capacitors are expected to go even higher because of the rising unit-ton price of tantalum-bearing ore. However, these price increases do not reflect an imminent lack of tantalum availability. There are adequate supplies of tantalum-bearing ores and available metal inventories to preclude a shortage in the foreseeable future.

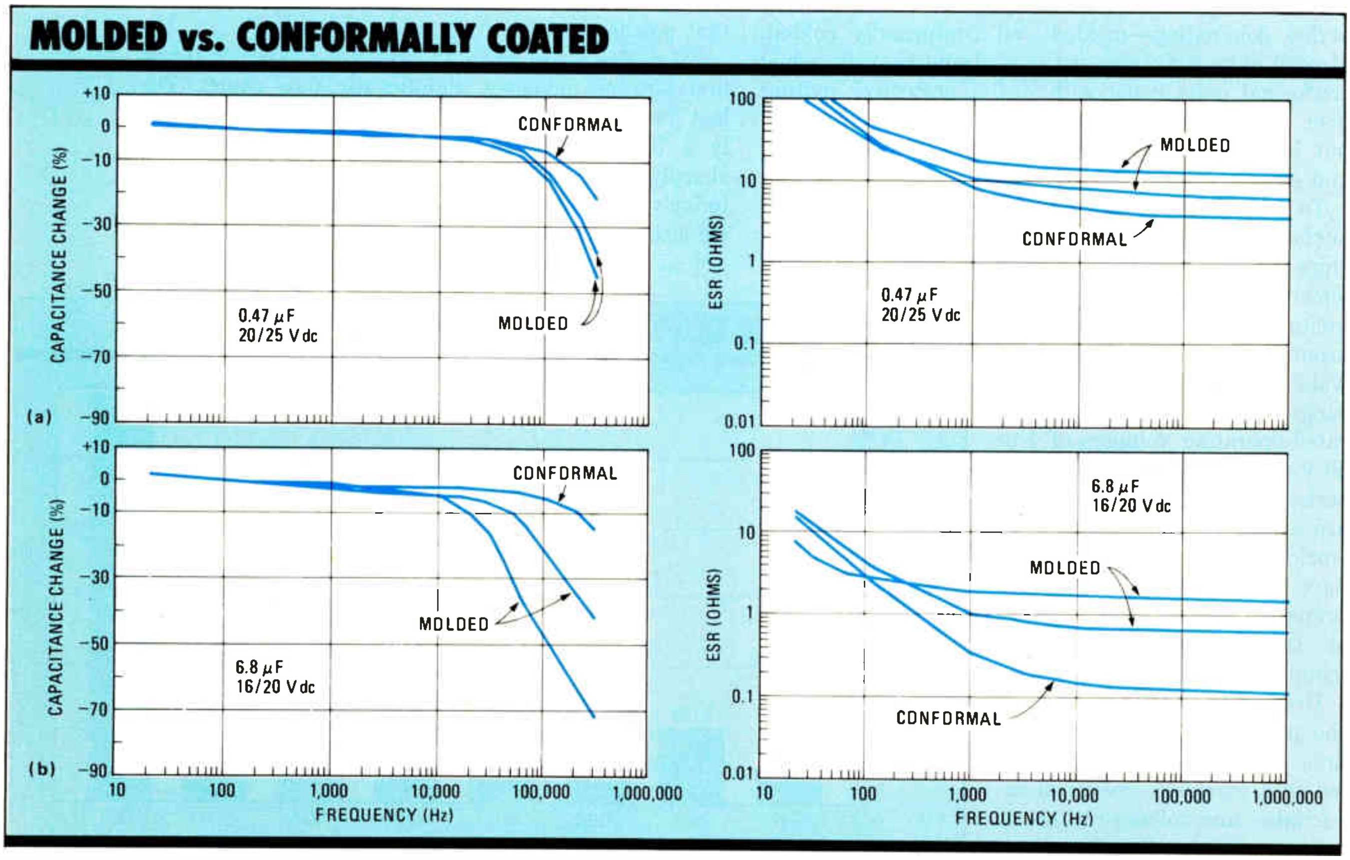
With the cost of tantalum now exceeding that of silver, makers of commercial tantalum capacitors will probably adapt their manufacturing processes to materials having a greater surface area. As a result, look for a given CV rating to come in a reduced case size or a given voltage rating to provide twice the capacitance in the same case size.

The basics of manufacturing are about the same for all tantalum chip capacitors. As for any capacitor, the surface of the plate electrode is the principal factor in establishing capacitance value. The surfaces of the individual power particles determine the overall surface area of the plate for the chip's anode, thereby deciding the maximum capacitance density for any fixed package size.

The fabrication of the anode begins with compacting tantalum powder to a specified density in a rectangular shape. Next, embedding a high-purity tantalum wire within the rectangular body to a given depth produces the capacitor's positive termination. Then, sintering the anode pellet at 1500° to 2000°C under high-vacuum conditions drives out any impurities to create a physical and metallurgical bond between the powder particles and the tantalum riser wire. For some tantalum chips, the riser wire is welded to the top of the anode after the anode has been sintered.

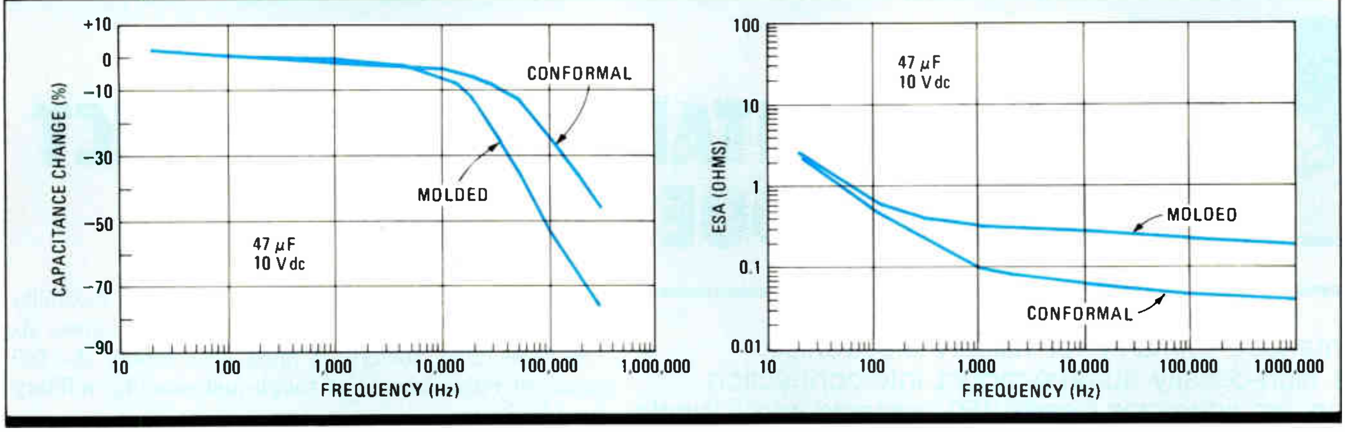
The sintering process, which thermally fuses individual flake particles, reduces the surface area of the pressed anode and results in a highly pure and physically rugged porous tantalum anode. Subsequent electrochemical processes produce the tantalum-pentoxide dielectric and the manganese-dioxide cathode. Other internal chemical coatings—including carbon, conductive silver, and plated coatings—complete the active capacitor element.

Despite the similarities in manufacturing, molded and conformally coated tantalum chips perform differ-



1. Conformally coated chips perform with less capacitance loss and lower ESR beyond 50 kHz for both low values (a) and moderate values (b).

BEST FOR SWITCHING SUPPLIES



2. Application-specific tantalum chip capacitors can be optimized for a particular task, like switching power supplies.

ently. Conformally coated chips minimize the packaging-material volume, so they are the clear choice when size and performance, not price, are the overriding considerations. They provide maximum capacitance at a given operating voltage in the smallest package. Their manufacturing is easily adapted to special capacitor sizes and tailored electrical parameters. However, when low cost is the main concern, molded tantalum is the obvious winner.

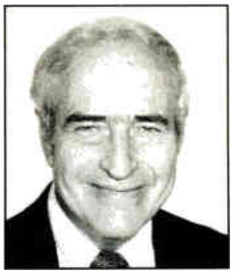
Differences in the electrical performance of the two types (see fig. 1) are apparent. The curves show the normal variations in capacitance and equivalent series resistance of molded and industrial-grade conformally coated devices over the frequency range of 20 Hz through 300 kHz. The comparisons reflect typical performance for low-value (0.47 uF) chips and moderate-value (6.8 uF) ones. In a nutshell, above 50 kHz, conformally coated capacitors exhibit less capacitance loss and consistently lower ESR than molded units having the same ratings.

Besides performance differences between molded and coated tantalum chips, there are also major differences in the environmental performance of equivalent devices made by different manufacturers. Even the military's established reliability data for component specifications lags the actual state-of-the-art electrical and environmental performance under dynamic circuit conditions. Therefore, when one manufacturer's series of tantalum chip capacitors will not meet a system's needs, an equivalent series from another manufacturer should be investigated and application-specific designs considered.

In fact, to fill the needs of a broad array of systems, molded and coated tantalum chips now come in a wide assortment of application-specific designs. The devices are tailored by varying tantalum powders, densities, sintering conditions, and other processing conditions. For example, the frequency response and ESR of tanatalum chip capacitors can be optimized for use in switching power supplies (see fig. 2). Other application-specific designs include low-profile chips for circuit packages with height restrictions and chips with very low leakage currents over wide temperature ranges for battery-powered circuits.

In the future, new choices are likely appear for surface-mount designs. For instance, on the immediate horizon is a new wet-electrolyte surface-mountable tantalum chip. The device betters a solid-electrolyte unit in two key ways—it can survive limited low-impedance surge currents, and it can handle overvoltage stresses with little or no degradation of reliability. Still undergoing final engineering evaluation at Mepco/Centralab, the new chip will come in a hermetically sealed molded case and offer capacitance values from 6 to 68 uF at operating voltages of 6 to 50 V dc. Furthermore, it can operate over a temperature range of -55°C to +125°C, retaining two-thirds of its rated voltage at +125°C. □

WILLIAM J. HYLAND, the manager of research and development at the Mepco/Centralab division of North American Philips, develops new tantalum capacitors and improves existing ones. An 18-year veteran of the company, he has been involved with the design and fabrication of tantalum capacitors since 1951. He is a recognized authority on surface-mount tantalum chip capacitors and holds three patents in wet-slug capacitors and surface-mount solid-electrolyte tantalum chip capacitors.



WILLIAM E. KAUFFMAN is manager of technical services at Mepco/Centralab, where he evaluates products, reviews technical data, and coordinates technical programs and reliability test programs. He has held various positions at Mepco/Centralab for the past 13 years and been involved with the design of aluminum, tantalum, and film-dielectric capacitors for 26 years. He serves on two committees of the Electronic Industries Association and holds two patents for arc-supression networks for telecommunications.

THIS MILITARY INTERCONNECT SYSTEM DOES IT ALL

Intended primarily for military electronics, a high-density surface-mount interconnection system squeezes nearly 350 contacts into a single connector, carries its own tooling for easy installation, and compensates for misalignment

by Larry Johnson and Larry Mowatt, *Texas Instruments*

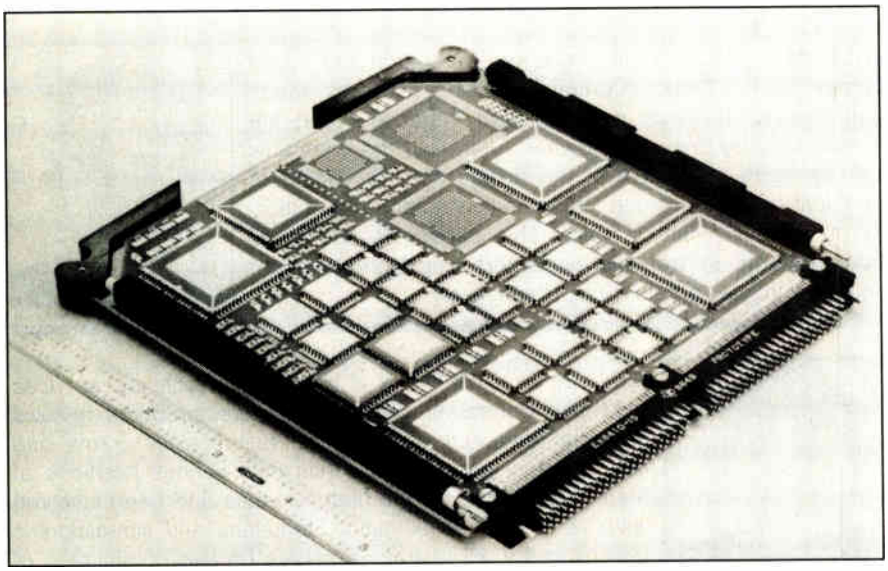
Military electronics and other high-performance applications call for extremely high component density but minimal system size and weight. Surface-mount technology appears to be the only way to realize this high-density packaging, which stacks printed-circuit boards only 0.4 in. apart. However, the combination of high density and surface mounting places a phenomenal burden on the connectors that must link all the boards. It mandates a system-level design approach for all the packaging components.

Because of the hundreds of contacts and the multiple boards that are involved, it has become impossible to align connectors and boards alike without a well-designed surface-mount packaging system. Such a system must anticipate and address interconnection difficulties at every step of the assembly process. To succeed, the system must also incorporate integral tooling that will ease alignment and built-in flexibility for initial assembly and subsequent modifications. At the same time, though, it must also satisfy the full array of requirements of tough and exacting military standards.

A new surface-mounting interconnection system meets these goals through the clever use of plastics and metals in a judiciously integrated packaging approach designed to adapt to the needs of today's and tomorrow's high-density electronic equipment. With this system, daughtercards can be stacked on 0.4-in. centers. Individual daughtercards can have up to 344 surface-mount solder connections on 0.025-in. centers. Similarly, the motherboard connector can accommodate up to 344 through-hole terminations in only a 0.05 by 0.075-in. footprint. Overall, the connectors have a density of approximately 173 contacts/in.^{2}—about 250% higher than a typical system using 0.1-in. centerline spacing. And even with that high pin count, mating force averages a low 2 oz. per contact. Moreover, both the daughtercard and motherboard connectors (see fig. 1) come in full-size (344 contacts) and half-size (172 contacts) configurations.

The new system provides a number of convenient features for simplifying the installation of its tightly packed contacts. For instance, flexible mounting bridges and flexible terminations allow the motherboard connector to move laterally, or float, by up to ±0.02 in. to adjust for any misalignment with a daughtercard. Also, an injection-molded lead organizer quickly and reliably directs the alignment and insertion of motherboard terminations through the tiny 0.016-in.-diameter holes needed in the pc board. Similarly, the leads of the daughtercard connector can also float up to ±0.02 in., and a built-in tool on the carrier strip of the daughtercard connector quickly and precisely aligns the leads on that connector with the pads on the daughtercard board itself. What's more, the polarity of the motherboard hardware can be rekeyed after soldering without removing the connector.

Electrical characteristics are also excellent, complying with the requirements of Mil-C-55302 (see table, p. 97). In spite of its miniature geometries for high pin density, the new interconnec-



Only high-density surface-mount packaging systems can meet the demands of military electronics and other space-sensitive applications.

tion system keeps contact resistance and insulator isolation within the specification limits for a connector having a 3-A current rating. Contact resistance is 20 mΩ for an individual mated-contact pair and 15 mΩ for all contact pairs, while the dielectric withstanding voltage is 750 V root-mean-square at sea level and 200 V rms at an altitude of 70,000 ft.

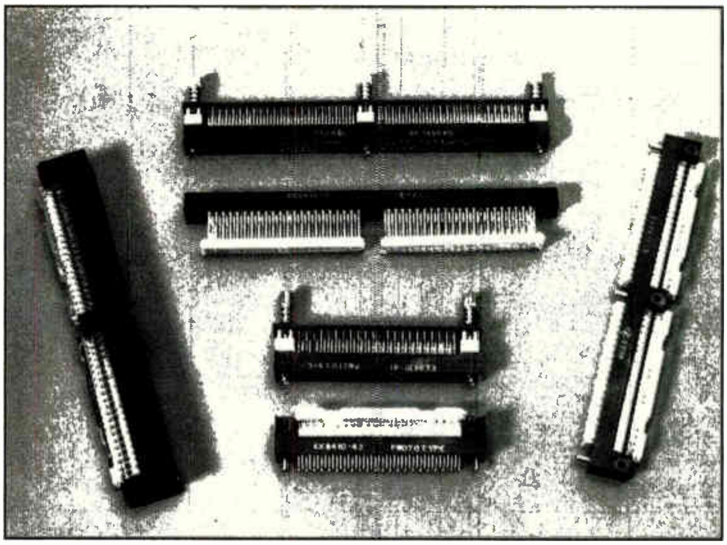
Three flexible mounting bridges—one in the center and one at each end—guide the motherboard connector body to its pc board, allowing lateral movement. They are carefully designed to flex sideways to take up daughtercard misalignment without damaging the boards, the connectors, or the contacts. In addition, long ductile motherboard terminations provide minimal resistance to permit the movement required for proper alignment.

With up to 344 leads being stuffed into the motherboard at one time, it is not possible to align that many leads of the motherboard connector with their corresponding plated-through holes in the motherboard itself without the aid of a tooled organizer. The key here is a funnel-shaped molded piece attached near the end of the terminations on the motherboard connector body. Called the lead organizer, this piece captures the lead tips and precisely registers them to the footprint on the pc board through a mounting boss.

A very thin plastic web serves as the mounting boss. It positions the organizer exactly where it is supposed to be on the feet of the mounting bridge before the connector is actually mounted to the board. Pushing the bridge legs through the motherboard mounting holes easily pierces the web. At the same time, all terminations are channeled through their respective pc-board holes. The interconnection system uses two identical organizers, one for each end of the motherboard connector.

Like the motherboard connector, the daughtercard connector also incorporates built-in tooling. Its carrier strip allows the position of its leads to be adjusted by ±0.02 in. with respect to the solder pads on the daughtercard. This carrier-strip alignment not only brings the connector's leads to the proper position on the pc board but also sets those leads to the correct ±0.002-in. position tolerance with respect to each other for their interface pitch of 0.025 in. Furthermore, the self-alignment feature permits standard tolerances to be used in the fabrication of the board itself.

Besides aiding the mounting and alignment of the connectors themselves, the integral adjustability of the system allows the user to compensate for adverse accumulated tolerances in the card cage. It is not uncommon for such tolerance stackup to occur during assembly because of misalignment between the chassis wall and the motherboard when the manufacturing tolerances for individual parts add up



1. A new interconnection system has 344 contacts in full-card sizes, 172 in half-card sizes.

the wrong way. In a typical system, there are over 20 component elements that can contribute to the overall variation in the relative positions of the motherboard connector and the daughtercard connector.

In addition, even after final assembly and the motherboard connector has been soldered in place, the new interconnection system makes changing the polarization of that connector easy. A clearance hole in the organizer's mounting boss and in the motherboard itself leaves enough room for loosening the hardware nut. That means the connector hardware can be replaced or rekeyed without disturbing the soldered connections.

The ability to rekey connectors during assembly is a critical feature for a motherboard, which may have as many as 50 connectors mounted to it, each with at least 300 leads soldered in place. Removing and replacing any of these connectors for rekeying is highly undesirable,

MEETING MILITARY STANDARDS

Electrical

Contact resistance: Mil-Std-1344, method 3004, 3 A, 15 milliohm maximum average, 20 milliohm maximum individual

Low-level circuit resistance: Mil-Std-1344, method 3002, 1 mA, 15 milliohm maximum average, 20 milliohm maximum individual

Dielectric withstanding voltage: Mil-Std-1344, method 3001, 750 V rms minimum at sea level, 200 V rms minimum at 70,000 ft

Insulation resistance: Mil-Std-1344, method 3003, 4,000 megohms minimum at 500 V dc

Mechanical

Oversized pin exclusion: 21 oz with a 0.033-in.-diameter pin for 10 s

Contact retention: 5 lb for 5 s, 0.015-in. maximum displacement

Engagement/separation: 4 oz maximum engagement, 0.5-oz minimum separation

Mating/unmating: 0.25 lb per contact, maximum mating; 0.04 lb per contact, minimum unmating

Life: 500 mate/unmate cycles

Solvent resistance: Boiling trichloroethylene for 78 s

Solderability: Mil-Std-202, method 208

Environmental

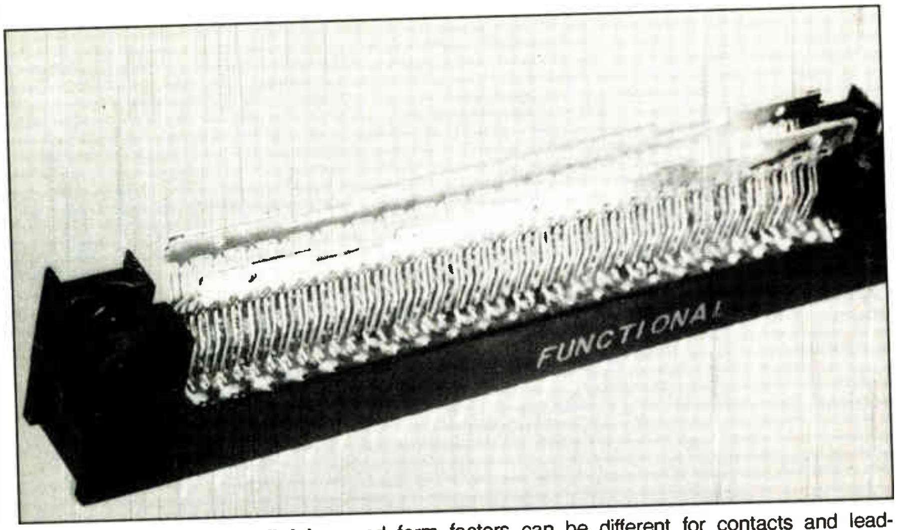
Vibration: Mil-Std-1344, method 205, 10 to 2,000 Hz, 15 g peak, 4 h per axis, 100 mA, 1-μs discontinuity

Shock: Mil-Std-1344, method 2004, 6 ms, 100-g sawtooth, six shocks, 100 mA, 1-μs discontinuity

Salt spray: Mil-Std-1344, method 1001, 5% salt solution at 95°F for 48 h

Temperature cycling: Mil-Std-1344, method 1003, five 1-h cycles, −65°C to +125°C

Humidity: Mil-Std-1344, method 1002, type II, 10 days at 25°C, 80 to 98% relative humidity, 100 V dc



2. Material finishes and form factors can be different for contacts and lead-termination combs because they are manufactured separately, then welded together.

because the procedure could cause damage to assemblies that are otherwise good—and the likelihood of an assembly mistake increases as the number of installed connectors goes up.

In contrast, rekeying a daughtercard is a relatively simple, single-step operation, because it involves the removal and reinstallation of just one connector. Moreover, the daughtercard connector could also have been designed to permit rekeying after assembly, although building in that capability would have meant significant trade-offs. To allow for this feature in the daughtercard half of the connector and at the same time still use standard hardware would reduce the interface area available for contacts and, therefore, the connector pinout. In this case, the formidable advantage of a high number of contacts far outweighs any benefit derived by being able to rekey the daughtercard connector after it has been installed.

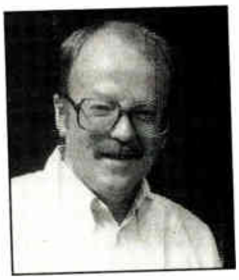
All of the elements of the interconnection system are optimized for high density, including separate manufacturing operations for the contacts and the lead-termination combs. This separation of contacts and termination combs readily allows different material finishes and form factors to be used for each. The combs are etched or stamped and then subsequently welded to down-sized, but standard, screw-machined contacts. The machined contacts employ a 24-gauge 3-A design for 0.025-in. centerlines, scaled down from the 22-gauge 5-A design that is typical for 0.1-in. centerlines. The scaling reduces the nominal diameter of male pins from 0.03 in. to 0.025 in.

At the welding operation, the machined contacts are married to 21- or 22-position combs. The welded subassemblies are then loaded into insulators a row at a time. A fully loaded connector requires 16 combs, eight with 21 contacts and eight with 22. Rows of welded subassemblies can be easily combined to provide any number of positions up to 344 in increments of 21 or 22. Finally, contacts are epoxied in place and the connector hardware installed (see fig. 2).

The actual measured performance of the connectors tends to bear out the merits of their design. For instance, the gang-mating force for fully populated connectors is in the vicinity of 50 to 60 lbs., or only about 2.3 to 2.8 oz per contact. Truly low-force, individual contacts have a typical mean of about 45 g (1.6 oz) for insertion and 35 g (1.2 oz) for withdrawal. Despite those low forces, contact retention is approximately 30 pounds. Moreover, the dielectric withstanding voltage between pins exceeds 1,000 V, and insulation resistance is above 4 gigaΩ by orders of magnitude. Finally, both full-size (344 pins) and half-size (172 pins) connectors have successfully survived up to 500 life cycles, while motherboard connectors have flexed sideways and yet remained stable through the flexing.

As for the future, a number of enhancements are already in development for this high-density surface-mount interconnection system, including the use of metal shells and different physical configurations. Using metal shells, instead of plastic ones, can provide pin protection, electrical shielding, and increased strength. Although a metal shell would add 0.10 in. (from 0.37 to 0.47 in.) to the overall width of the connector, motherboard connectors could still be placed on 0.5-in. centers. Moreover, a metal shell could accommodate, on the connector ends, fiber-optic contacts or other special power or coaxial contacts not requiring electrical insulation, provided there were an appropriate reduction in the quantity of conventional contacts. In addition, modifying how the terminations are formed would permit different motherboard footprints and daughtercard boards having a thickness above 0.125 in. □

LARRY JOHNSON is a project engineer working on the development of new military connectors in the Connector System Department of Texas Instruments. He has 19 years of electromechanical design experience in instruments, keyboards, and military connectors. He earned his BS in mechanical engineering from Northwestern University and his MS in mechanical engineering from the University of Minnesota. Johnson holds five U. S. patents for advances in connector technology.



LARRY MOWATT is a member of the technical staff and a lead mechanical design engineer working in surface-mount packaging in the Microelectronics Packaging Systems Department of Texas Instruments. For the last six years, he has worked with surface mounting; for eight years before that he worked on mechanical design in seismic equipment and military packaging. He holds a BS in mechanical engineering from the University of Missouri-Rolla and an MS in mechanical engineering from Southern Methodist University.

MILITARY/AEROSPACE NEWSLETTER

NORTHROP IS DEVELOPING A MILITARY VERSION OF THE FDDI

Northrop Corp. is developing a militarized version of the Fiber-optic Distributed Data Interface, the forthcoming 100-Mbits/s commercial networking standard. Northrop's goal is to produce a fiber-optic data-distribution network for future aircraft—beyond the Advanced Tactical Fighter, says Marc Cohn, an engineering specialist at Northrop's Advanced Systems Division in Pico Rivera, Calif. Northrop is funding the effort internally and is now trying to get the Society of Automotive Engineers, which assists the Air Force in standards activities, to help establish industry-wide specifications optimized for the temperature, radiation, and vibration requirements of military aircraft. The aim is to define everything—from the kind of fiber to the proper militarized connectors and optoelectronic components—and to use commercial standards wherever possible, he says. Care must also be taken to keep the standard generic, he adds. "We don't want to reinvent the wheel; we want to build on what's already available in the commercial world." □

AMD UNLEASHES ITS 29000 RISC CHIP ON THE MILITARY MARKET

Advanced Micro Devices Inc. has taken a key step toward making its Am29000 microprocessor a standard for 32-bit military systems. Martin Marietta Corp. will use the part in its Enhanced System Growth Network, the first announced military design win for AMD's RISC offering. It comes just as the company has announced its offer to freely license the 29000's instruction-set architecture for use as an Air Force standard [*Electronics*, May 12, 1988, p. 39]. About 10% to 15% of the beta-site requests for the chip have been for defense-system applications, says Mike Woodpian, an AMD program manager. He says the Sunnyvale, Calif., company will have a militarized 29000 qualified to Mil Std-883-C on the market by the end of the year. □

USING A CRYSTAL BALL TO FEND OFF LOW-FLYING AIRCRAFT

Thorn EMI Electronics Ltd. has developed a portable aircraft-detection system that identifies and tracks low-flying aircraft. The Air Defense Alerting Device meets a British Army requirement for a detection system that would not give away the position of its users. Rather than incorporate radar, acoustic, or laser detection technologies, the system uses a rotating pyroelectric scanner that can detect temperature variations of just 0.1°C across an area 8 km in diameter. As it rotates, the unit produces a temperature map of a 240° sector of sky, identifying signal variations between successive scans. Software identifies the temperature signatures of targets, and discriminates between threats and nonthreats, such as birds. These outputs can be linked either to portable displays or to compatible anti-aircraft systems. □

THIS SOFTWARE CAN HANDLE DOD'S ONEROUS LIFE-CYCLE COST DOCUMENTATION

Defense contractors frustrated by the costly and time-consuming need for complex contract-requirements management and documentation mandated by the Defense Department's Mil Std 2167A—a Pentagon life-cycle development methodology—now have a new software tool to ease the burden. Nastec Corp., a Southfield, Mich., computer-aided-software engineering firm, says its CASE 2000 RTrace package is the first that can track and allocate requirements across multiple document levels, linking low-level software and hardware subsystem detail to high-level system requirements. Competitive packages typically handle a single document level only, Nastec says, while RTrace can reduce the time it takes to produce documentation by about 20%. The RTrace package, which runs on VAX/VMS systems (Version 4.6 or higher), costs $30,000. □

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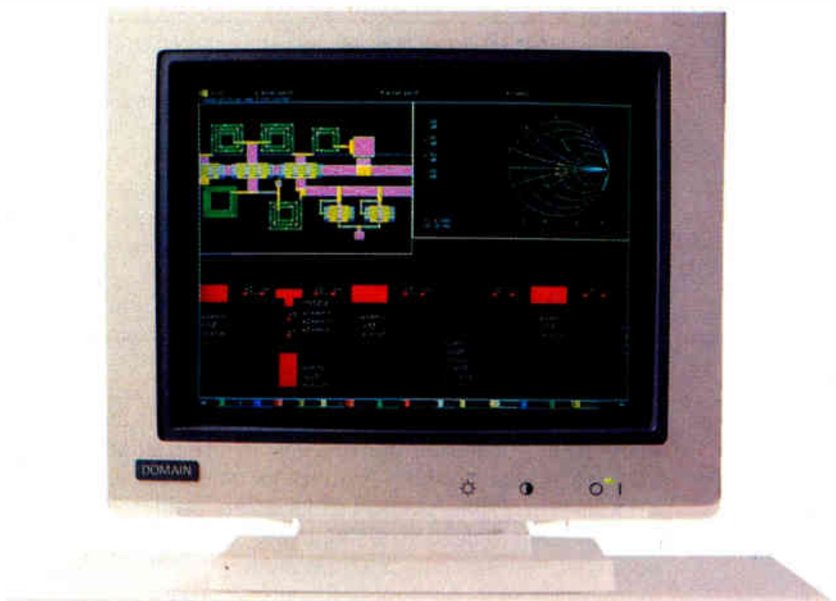

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NEW PRODUCTS

VARIAN'S ION IMPLANTER PUSHES WAFER-FAB AUTOMATION TO THE LIMIT

Extrion 1000's closed-loop feedback controls more processes than ever before

A high-current, ion-implantation system from Varian Associates takes automated wafer-fab operation further than it's ever gone: closed-loop control of more process parameters than ever before, automatic setup and operation, and automatic self-diagnostics and self-correction in real time. In short, the company says, the third-generation Extrion 1000 embodies full automation for "lights-out" operation, including compatibility with robot-guided vehicles for distributing wafer cassettes.

Use of 25 embedded microprocessors provides the advanced automation, which, in turn, contributes to high throughput and wafer yields. The Extrion 1000 also has a usable beam current range of up to 27 mA—almost a 100% improvement over second-generation devices, which offered 15 mA. Other key features are a 2-to-200 keV energy range, greater process flexibility, and the ability to handle numerous device types.

The closed-loop process control goes beyond any other available, says R. Bruce Thayer III, product marketing manager in the Semiconductor Equipment Group's Extrion Division, Gloucester, Mass., and the feedback loop built into the implanter will contribute to improved product yield. "We can monitor yield in relation to performance parameters that are interlocked into the control system, making sure they are within specification," Thayer says.

Varian's throughput specification for 150-mm wafers is 100 wafers/hr when the system is implanting 10^{16} ions/cm_2 (1E16). Its throughput is 200 wafers/hr at 10^{15} ions/cm_2 (1E15). Thayer says that one customer's throughput projections suggest that the company can cut costs by about one-third using the Extrion 1000.

Throughput considerations include not only the number of wafers processed in a given time but also the amount of equipment uptime and utilities costs associated with use of the system, Thayer says. Included in the closed-loop feedback system are 15 Motorola Inc. MC68008 microprocessors and seven Intel Corp. microcontrollers. Three MC68020 microprocessors comprise the main system central-processing unit, communications CPU, and wafer-handler CPU.

The closed-loop system handles an energy range of 2–200 keV; dopant dose uniformity and reproducibility (both to within 0.05% standard deviation); wafer charging of ±3V surface potential buildup, which is compatible with gate oxide structures less than 100-Å thick; wafer cooling to below 100°C at 4 kW; and particles-added rating of less than 0.05/cm^2 at 0.05 μm.

The Extrion 1000 can implant dopants in devices with submicron features, including 64-Kbit static random-access memories and 16-Mbit dynamic RAMs. It accommodates processes including thin gate oxides, face-on and sidewall implants that require a broad range of single- and double-charged dopants in large-diameter (3-in. to 200-mm) wafers.

Extrion 1000 holds 13 200-mm wafers, 18 150-mm wafers, 22 125-mm wafers, or 27 100-mm wafers.

To date, an implanter's energy range of about 20-160 keV has prevented the systems from processing some CMOS devices, Thayer says. The lower ranges of the 1000's 2–200 keV span are especially suited to CMOS.

As device geometries shrink, oxides are also getting thinner, with 50 Å the goal of many manufacturers. Thayer says the Extrion 1000 will handle oxides substantially thinner than the 100-Å specification—probably in the 30–40-Å range—which is especially useful for MOS devices with thin gate oxides. Keeping wafers cool is important because photoresists can be damaged or ruined above 125°C. And particulate control is critical to achieve good yields, because today's processes demand such fine geometries "that you can't have a particle across a one-micron line," Thayer says.

The system's single scanning disc holds the following wafer selections: 13 200-mm, 18 150-mm, 22 125-mm, or 27 100-mm. The wafers are "hugged" around their circumference without clamping to each wafer site, allowing full-surface implantation. As the disc spins during implantation, centripetal force presses the wafers to cooled sites on the disc without sliding or sticking.

Horizontal wafer scanning is done at a high rate, typically 1,250 rpm. Scanning is monitored and automatically adjusted to get continuously uniform dose control.

S E M I

The best products the semiconductor fabrication industry has to offer will be on display at Semicon/West '88 on the San Mateo, Calif., fairgrounds May 24-26. More than 40,000 visitors are expected at the show, where a wide variety of equipment will be shown, including two innovative ion-implantation systems. Each represents a new generation of ion implanters addressing the special requirements of MOS biC-MOS and ASIC devices. Both these products are described in this special Semicon West section.

Slow vertical wafer scanning is achieved by raising or lowering the implant disc.

The system uses a proprietary single-cusp ion source instead of the Freeman source used in most implanters. The new source contributes to both longer life and the system's higher beam current. The source has a rated life of 168 hrs—three times longer than the sources in other implanters, Thayer says. That's important because "one of the greatest causes of lost time in implanters has been the 5-7% of available production time consumed changing sources."

Automatic setup is accomplished by having process recipes stored on the system's 20-Mbyte hard disk and quickly called up to configure the implanter. Process monitoring is also automatic, with either numeric or bar-graph representations of parameter high and low values and provision for automatic correction by the system.

Enhancing the system's automatic diagnostics, each module performs microprocessor-controlled self-test. The CPU constantly queries those subordinate modules to check their status.

Three vacuum load elevators, each handling one wafer cassette, are included in the system. Wafer handling is via horizontal pick and place, with tactile backside contact. A single-drive load arm selects each wafer from a cassette and carries it to the scanning disc, accurately centering and orienting it during transport. Wafer breakage is specified as less than one wafer in 50,000 handled, compared with less than one in 20,000 for earlier Extrion implanters.

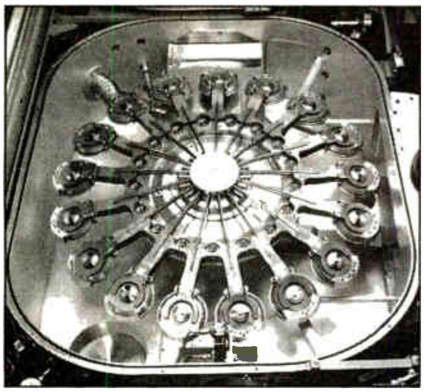
The Extrion 1000 sells for $2.5 million and will be available in the first quarter of 1989. – *Lawrence Curran*

Varian Semiconductor Equipment Group, Extrion Division, Blackburn Industrial Park, Gloucester, Mass. 01930.
Phone (617) 281-2000 [Circle 420]

ION IMPLANTER CAN HANDLE 200-MM WAFERS

The Precision Implant 9200 ion-implantation system from Applied Materials Inc. incorporates into the company's previous-generation implanter the ability to handle the 200-mm silicon wafers that will increasingly be used in the near future for improved productivity.

Although the basic technology of the 9200 follows that used in the Precision Implant 9000, another major improvement is an enhancement of the Light Touch automation package, called the AutoBeam system. The Autobeam package allows the process engineer to iden-



tify specific ion implantation recipes by code numbers, leaving the operator to do nothing more than load cassettes of wafers into the load lock.

The 9200 uses the same target wheel as the 9000, which holds wafers by centrifugal force to avoid contamination and breakage. In the 9200, the wheel has been modified to optimize throughput on larger wafers, with a capacity of 17 200-mm wafers on the wheel and three wafer cassettes in the load lock chamber.

Wafers are implanted on individual, water-cooled planar heat sinks, which are used to ensure low temperature processing. Wafer temperatures on the 9200 are routinely less than 50°C. The 9000 maintained wafers at below 80°C.

The 9200 delivers usable beam currents over a energy range of 2—180 KeV as compared to 10—180 KeV on the 9000. It handles a wide range of process requirements for doses between 1E11 and 5E16. This flexibility allows the replacement of two conventional implanters with a single, multipurpose system.

Active monitoring of 9000s in the field led to directed engineering programs on the 9200 to improve performance and reliability. For example, the 9200 development process included verification of wafer-handling performance in which more than 80,000 transfers of 200-mm wafers were done without major error.

The routine particle-level performance of the 9200 meets the most stringent requirements for leading edge VLSI devices. The unit routinely operates in different production environments at particle levels between 0.02 and 0.07/cm^2.

The Autobeam VME computer system is fully compatible with factory-automation requirements such as links to host computers via a SECS-II interface and robotic handling of cassettes.

Shipments of the 9200 have already begun to selected customers. Pricing on the system ranges between \$1.4 and 2.8 million depending on configuration. Delivery is within four to six months after order. – *Jerry Lyman*

Applied Materials Inc., 3050 Bowers Ave., Santa Clara, Calif. 95054.
Phone (408) 727-5555 [Circle 421]

PROGRAMMABLE FILTER PUTS TOP FEATURES IN SMALL BOX

Frequency Devices' model 9002 fits into a half-width of a 19-in. rack and lets users program two active-filter channels with up to six parameters

Frequency Devices Inc.'s model 9002 programmable filter fits into a space half the width of a standard 19-in. instrumentation rack yet it allows users to independently program up to eight configurations on each of two mix-and-match active filter channels. The eight configurations can have up to six presettable parameters each.

Measuring 3½ by 8½ by 15 in., the 9002 is the only instrument its size with such an advanced feature set, claims the Haverhill, Mass., firm. The unit sells for $2,495; competing units range up to $7,000 in price. The unit targets applications such as interactive aliasing, industrial process control, or vibration and signal analysis.

BROAD RANGE. The 9002 offers single-ended or differential input, compared with single-ended only for the lowest-priced competition, which is priced at $3,000. It also provides a broader range of filter types while selling for $500 less than the lowest priced competition.

Each of the two available channels is continuously tunable, without range switching, over a range of 0.1 Hz to 102.4 kHz. Each filter has a resolution of 3½ digits. Competitive instruments require multiple range switches for adjustment and readout.

The controller can be programmed from either its own front-panel keypad or remotely using a personal computer and the industry-standard IEEE-488 instrumentation bus. Standard programming features include pregain from +1 to +13.5 in steps of 0.05; post gain from +1 to +13.5 in the same steps; corner frequency to 3½-digit resolution; single-ended or differential input; ac- or dc-coupled inputs and outputs; and filter-active or bypassed modes.

Among the 9002's other important features is the ability to store a channel's configuration for as long as five years in battery-backed random-access memory. The RAM can store as many as eight combinations of these parameters and settings, enabling users to change channel parameters quickly and with fewer keystrokes than are required to manually enter such data.

Any of a broad selection of channel filters can occupy either channel of the 9002, but the location and type of filter must be specified when the instrument is ordered. Users can cascade a low-pass and high-pass filter to get a bandpass response, or cascade two similar low-pass filters to obtain a faster roll-off rate and a deeper stop-band floor.

A broad selection of filters including Butterworth, Bessel, and elliptic can occupy either of the 9002's two channels.

Users can specify any two of the following filter-response characteristics: 8-pole Butterworth low pass with no ripple in the passband; 8-pole, 6-zero elliptic low pass with 82-dB stop-band floor; 8-pole Bessel low pass with 48 dB/octave roll-off rate in the stop band; 8-pole, 6-zero constant delay low pass that maintains a flatter passband than a Bessel; 8-pole Butterworth high pass with no ripple in the passband; and 8-pole, 6-zero elliptic high pass with a theoretical 0.01-dB ripple in the passband.

Frequency Devices promises delivery of the 9002 within nine weeks after the customer places his order. For applications in which more than two tunable channels are required, the company offers as an option a kit for $150 that allows two 9002s to be mounted side by side in a rack. The basic price tag of $2,495 includes both the instrument itself and two channel filters in any of the listed combinations. *– Lawrence Curran*

Frequency Devices Inc., 25 Locust St., Haverhill, Mass. 01830.
Phone (617) 374-0761 [Circle 380]

ANALYZER DOUBLES AS PC

By delivering a full 100-MHz data-acquisition rate for state and timing analysis on up to 96 channels, Philips' PM3655 logic analyzer gives engineers clock rates five times higher than the competition without sacrificing channel capacity. What's more, the logic analyzer offers MS-DOS software compatibility as well as a price of under $10,000.

Competing instruments in the same price range are either limited to a 20- to 25-MHz performance for state analysis or sacrifice available channels to run at higher speeds, says Philips, based in Eindhoven, the Netherlands.

The instrument has both a high-speed instrumentation bus and a standard PCbus. Its high speed comes from the use of emitter-coupled-logic technology and innovative design, says Hans Binnerts, product manager for logic analyzers at the Philips Test and Measuring Instruments Group.

The modularly constructed PM3655 is user-configurable from 24 channels up to 96 channels in any combination of state and timing modes. Expansion takes place in 24-channel steps. The PM3655 offers glitch-capture performance of 5 ns on all 96 channels.

Compatible with IBM Corp. Personal Computers XT, the PM3655 gives users access to software for data analysis, word processing, and spread sheets.

As a high-speed analyzer, it can evaluate reduced-instruction-set-computer processors; as a PC, it can handle tasks usually performed by an emulator. It is this twin capability that makes the company "see big sales potential ahead for the 3655," Binnerts says.

A dual-screen display mode shows state and timing analysis diagrams on the same monitor. In addition, there are 2,048 bits of memory available for each of the instrument's data channels. That capacity is two to four times that of more expensive models on the market, Binnerts says. The high-resolution display allows viewing of any 24 channels at the same time.

The logic analyzer supports 8-, 16-, and 32-bit processors. Its 96-channel width, 100-MHz speed for state analysis, and 2-Kbit/channel memory depth, give it the performance needed to support future high-speed, high-pin-count devices with parallel processors and RISC CPUs.

Deliveries of the PM3655 will start in August. Delivery time will initially be about six weeks. The instrument is being marketed in the U. S. by John Fluke Manufacturing Co. and will sell for $9,500. *– John Gosch*

John Fluke Manufacturing Co., P. O. Box C9090, Everett, Wash. 98206.
Phone (800) 443-5853 [Circle 381]

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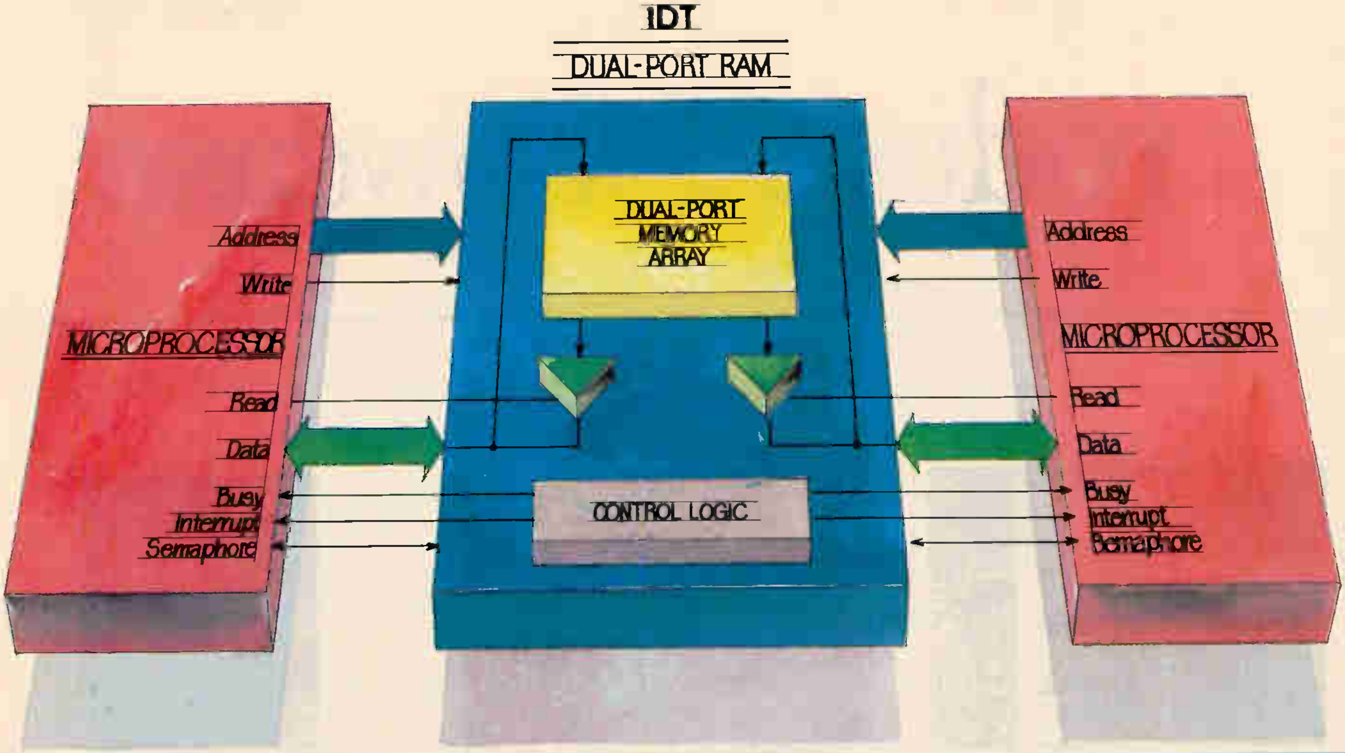

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"	[illegible]	[illegible]				x
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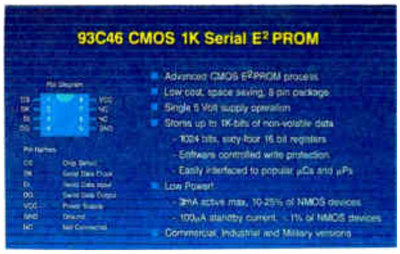

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ELECTRONICS WEEK

IBM JOINS NETWORK COMPUTING FORUM

It's taken more than a year, but IBM Corp. has finally joined the Network Computing Forum. The Forum was established in March 1987 to consider technical approaches for computing on networks of multivendor systems. Apollo Computer Inc. of Chelmsford, Mass., spearheaded the project and is the group's organizational sponsor. IBM's participation brings the membership to more than 100 end users, hardware and software suppliers, and academic institutions, including Apple Computer, Control Data, and Hewlett-Packard.

PRIME COMPUTER WILL LAY OFF 700

Prime Computer Inc. finished the first phase of its merger with Computervision in bloody fashion in mid-May, saying it will lay off 700 people, or about 5% of its workforce. The two companies merged in February. Positions in research and development and direct sales will not be affected, Prime says. The Natick, Mass., company is hoping attrition and the redeployment of workers to other operations will keep the number of affected workers under 700.

ROCKWELL ADDS CHIPS TO TELECOM UNIT

Rockwell International Corp. is realigning its telecommunications and semiconductor businesses into Rockwell Communication Systems, which will be based in Richardson, Texas. By combining its chip operations in Newport Beach and Newbury, Calif., with its telecommunications businesses in Downers Grove, Ill., and Richardson, Rockwell aims to focus on three areas: end-user network applications, customer-premises data communication, and network transmission and management. G. F. "Gil" Amelio, who has headed Rockwell's telecommunication businesses since February, will run the new group, which had total sales of $860 million in 1987.

CAN DEC AND COMPAQ OUTDO IBM's PC LINKS?

Moving to bypass IBM Corp. and establish an alternative mainframe-to-personal computer link, Compaq Computer Corp. and Digital Equipment Corp. have signed a technology exchange deal to make an optimal link between Compaq's PCs and DEC's VAX systems. DEC, Maynard, Mass., already has a DECnet-DOS interface that runs on Compaq PCs and works with DECnet/OSI, but the new agreement will lead to a more optimized facility, says Michael Swavely, vice president for sales and marketing at the Houston PC maker. Swavely contends that IBM is becoming more proprietary, making it less easy to integrate its PCs into enterprise-wide networks.

WESTINGHOUSE BUILDS A VHSIC-BASED 1750A

Westinghouse Electric Corp. says it has developed a Mil Std 1750A avionics processor module based on very-high-speed-integrated-circuit technology. The company's Electronics Systems Center in Baltimore developed the module under the Air Force's VHSIC Avionics Modular Process Program and will deliver six systems for evaluations and software development beginning in October.

COMPUTER EXPORTS AHEAD OF IMPORTS

The information technology industry showed a positive trade balance of $69 million in the first two months of this year, thanks mostly to the computer industry, the Computer and Business Equipment Manufacturers Association says. A positive computer trade balance of $866 million on exports of $3.5 billion—in part due to the strong Japanese yen and weak U. S. dollar—helped to offset the severe negative balance in telecommunications and business equipment. In those markets, imports outpaced exports by a total $902 million, CBEMA says. It took an unlikely market—supplies—to keep the balance positive, CBEMA says. U. S. exports of floppy disks, printer ribbons, and the like were $132 million in January and February—$109 million more than imports.

SIR CLIVE'S LATEST PC HITS U. S. SHORES

Sir Clive Sinclair's latest personal computer, the Z88, is coming to the U. S. market in a typically unusual fashion. Diversified Foods Inc., a grocery wholesaler in Portland, Me., will handle U. S. distribution of 13,000 computers and peripheral systems—worth $7.1 million in all. Diversified Foods has already set up a subsidiary, Sinclair Systems Inc., to distribute the $549 battery-powered portable computer, which weighs less than 2 lbs, and includes built-in word processing, spreadsheet, and time management software.

UNISYS: SOLE SOURCE FOR NAVY PROCESSOR

Unisys Defense Systems, McLean, Va., has finally beat out Control Data Corp. in its bid to be sole supplier of the Navy's AN/AYK-14 (V) airborne computers. The Navy will buy 14 units from Unisys this year, and holds options for up to 365 more, giving the contract a potential total value of $30 million. The AN/AYK-14 (V) is the general purpose computer for embedded processing functions aboard Navy tactical aircraft, and is the heart of fire control, navigation, and signal processing systems. It was originally developed by Control Data. Unisys began supplying it as a second source in 1984.

CONCURRENT WINS KEY SUPPLY DEAL

Concurrent Computer Corp. will supply $88 million worth of superminicomputers to Unisys Corp. for a new federal weather radar system. Called Nexrad, for next-generation weather radar, the system is designed to increase the warning time for tornadoes, hurricanes, wind shear, and flash floods. The $450 million project is a joint effort between the U. S. departments of commerce, defense, and transportation. Concurrent's piece of the action will be a trio of superminicomputers for each of the 175 Nexrad stations to be installed throughout the U. S, the Caribbean, and in Western Europe and the Pacific. The systems are high-end 3280s, to process Doppler radar at high speeds, and 3212s, one to interface with the radar equipment, and a second to distribute data.

TEST & MEASUREMENT DRIVES OP AMP SALES

The U. S. market for operational amplifiers will take off over the next five years, thanks to a big boost from applications in test and measurement systems, says market researcher Venture Development Corp. Military systems have been the biggest consumers of the parts, the Natick, Mass., firm says, accounting for 28% of the $497.5 million market in 1987. But with military systems makers shifting toward digital circuitry, Venture expects the military market to flatten by 1990. Test and measurement systems, meanwhile, are growing more complex and using larger numbers of op amps. The result should be 14% annual growth over the next decade, Venture predicts.