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MARCH 31, 1988

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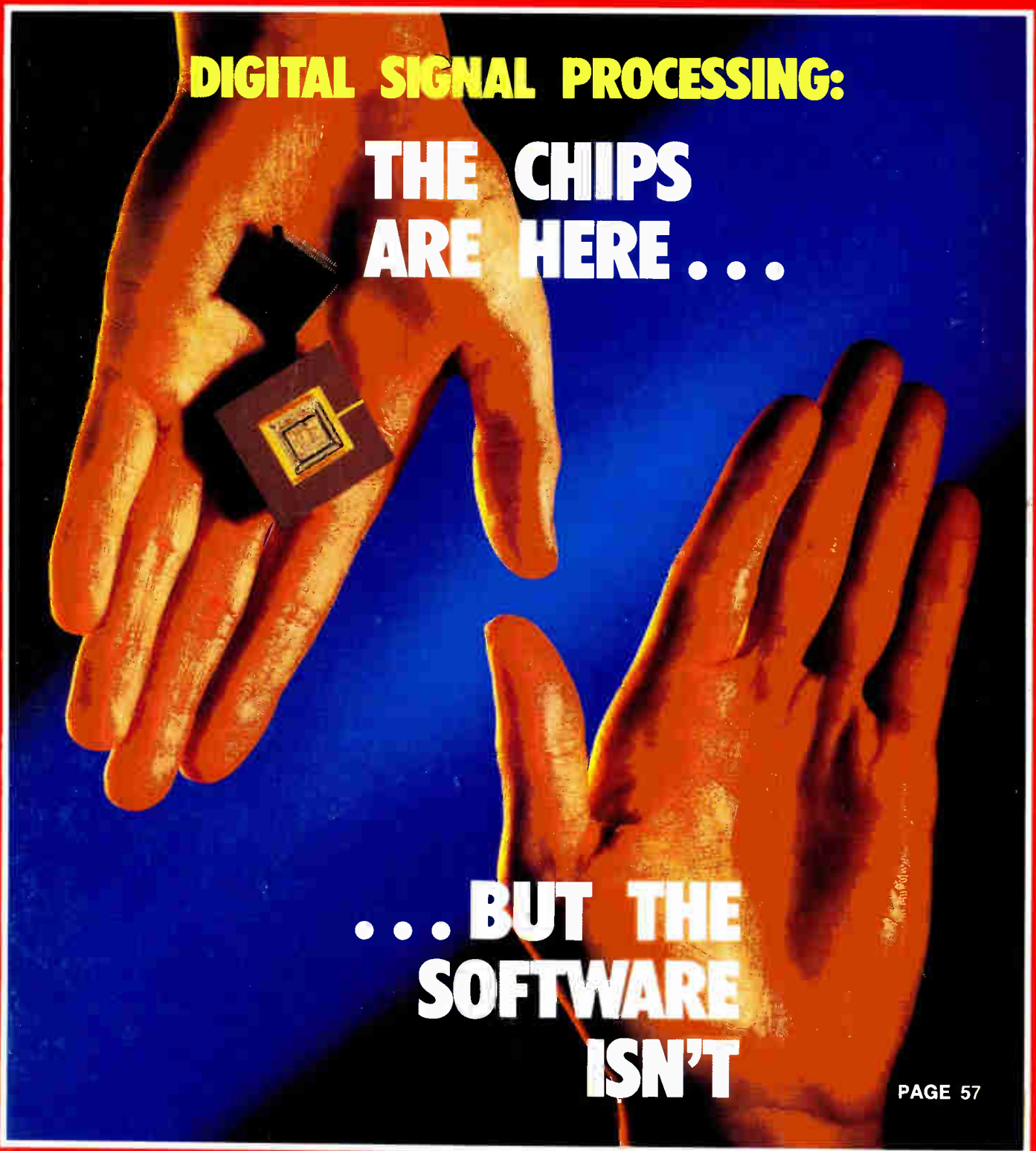

DIGITAL SIGNAL PROCESSING:

THE CHIPS ARE HERE . . .

. . . BUT THE SOFTWARE ISN'T

PAGE 57

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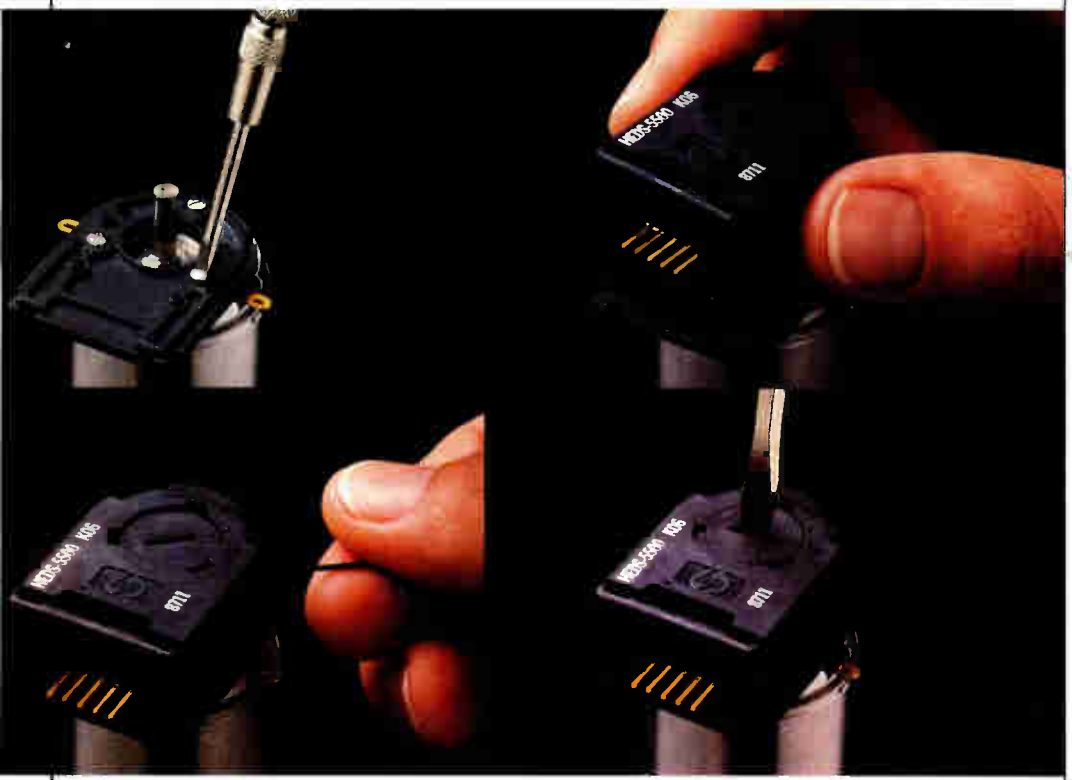

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Circle 1 on reader service card

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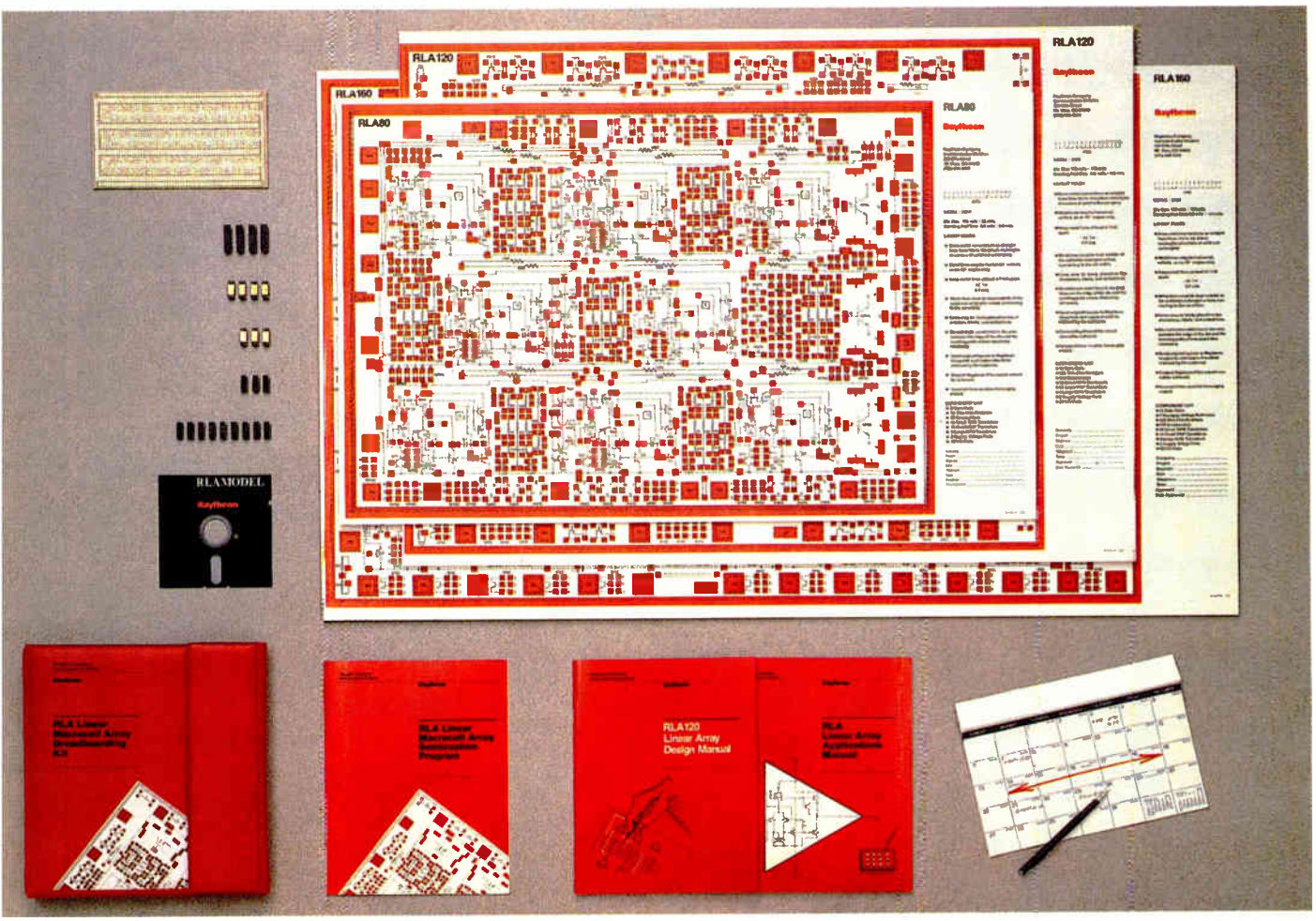

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[1]PSPICE is a trademark of MicroSim Corporation.
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Putting together a news story can be as simple as getting a phone call from someone with something to say. Or it can be as complex as collecting bits and pieces over weeks and months the way a detective picks up clues. When it comes to getting information from the Defense Department, the technique of necessity is definitely that of Sherlock Holmes.

Naegele has to be a detective to cover the Pentagon.

"Covering the Pentagon is not like covering the electronics industry," says Tobias Naegele. "An electronics company will sometimes tell you that something is coming, but with the military you have to find the news."

Tobias, our military/aerospace editor, did just that with his article on the Pentagon's new approaches to procurement policy that leads off our military package on p. 83. "The story kept changing and growing until what I wound up with was something different, and quite a bit more, than what I thought I had when I started."

It started simply enough when Tobias suggested a story on the changing specifications for military systems. Pursuing that, he attended a seminar in December sponsored by the Semiconductor Industry Association. "People there were talking about changing specs, so I figured I had the beginnings of a good piece." In February, Tobias went to Dayton, Ohio, to talk to the people at DESC, the Defense Electronics Supply Center. And later that month, to get industry's side of the equation, he spoke to officials at Martin-Marietta Corp. and Harris Corp. in Florida. All this time he was gathering information for what he thought was an article on specs.

But that changed. "The more people I talked to, and the more I looked at the subject, the more I realized that the things I had learned pointed to a lot more than mere changes in specs. Rather, they were actually outgrowths of a broader policy change. The thing I needed was confirmation from the people at the Pentagon itself."

That someone turned out to be Robert B. Costello, under secretary for acquisition. "I finally got to Costello on March 16, and that tied the whole thing together," says Tobias.

On March 18, *Electronics* was acquired from McGraw-Hill Inc. by VNU Business Publications, a wholly owned U.S. subsidiary of VNU United Dutch Publishing Co., the largest publisher in the Netherlands. It publishes more than 50 computer and electronics titles in 10 international markets. In the U.S., VNU publishes *Electronic Design*, *Microwaves & RF*, *Engineering Tools*, and *Personal Computing* magazines.

This is a very special addition for VNU. It gives us the opportunity to expand our scope beyond our design-oriented magazines to include computer and electronics management. Readers and advertisers will benefit from the synergies.

The sale of a magazine transcends the mere exchange of assets: a torch is passed with the buyer assuming a weighty mantle of service and editorial tradition. With the acquisition of *Electronics*, we feel an awesome responsibility to maintain—and build—the quality of a publication that has served an industry for almost 60 years.

Thus, we are especially pleased to welcome the award-winning editorial staff of *Electronics* to the VNU family. With Editor in Chief Robert Henkel continuing in charge, VNU is committed to maintaining the magazine's high editorial standards.

The acquisition of *Electronics* means more than just a change in ownership. The publication has a strong, new financial commitment, as well as access to resources that will be used to make a great magazine even better. We are investing heavily in the magazine to serve the most important people in the world—the readers of *Electronics*.

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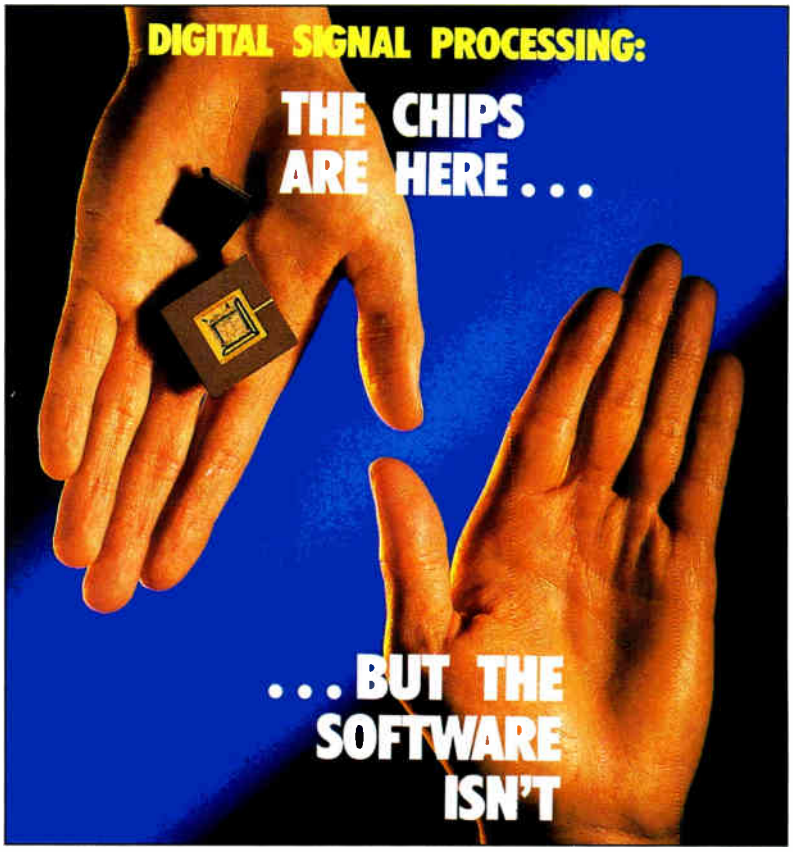
MARCH 31, 1988

Electronics

NEWS

INSIDE TECHNOLOGY

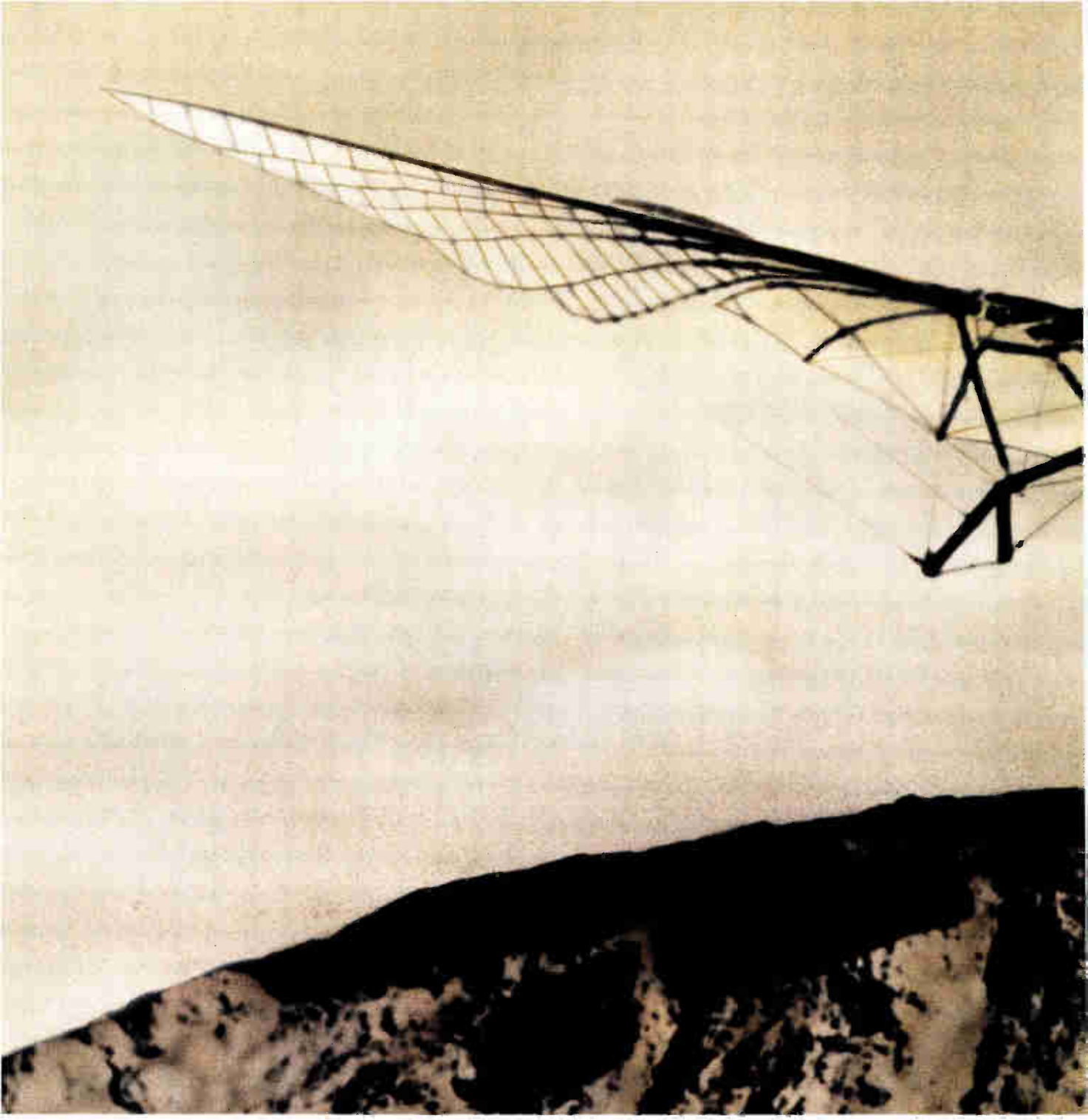
COVER: CHRISTOPHER GOULD



PAGE 57

NEW PRODUCTS

DEPARTMENTS



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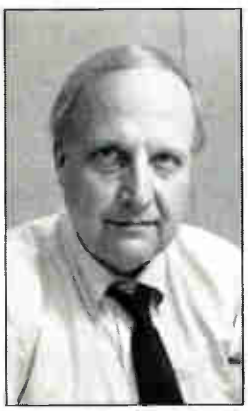
Circle 7 on reader service card

CAN WE MAKE CHIP R&D MORE EFFICIENT?

$4 billion a year is now being spent on chip R&D, "but this full investment is not being utilized," says SRC's Sumney; "25% is lost through duplication"



I completely missed it. And I'll bet you did too. But an end-of-the-year amendment tacked onto the U.S. trade bill that's now languishing on Capitol Hill is well worth talking about. While passage by Congress could end up creating just one more government committee turning out no more than tons of never-read reports, it just might end up becoming one of the most important things that the Congress will do this year—at least it could for the U.S. electronics industry. I owe my newfound knowledge to Larry Sumney, president of Research Triangle's Semiconductor Research Corp., as well as managing director of Sematech, who laid the plan on me in Cocoa Beach, Fla., at a recent Harris Semiconductor seminar. Larry, by the way, would be delighted to have his SRC provide staff support.

The bill would set up a National Advisory Committee on Semiconductors in the executive branch, with its own budget, and made up of government and industry managers. Its goals would be resource allocation, setting chip R&D priorities and directions. It would set up a data base on semiconductor R&D, carry out technology assessments, and develop a national semiconductor strategy.

This strategy should improve the coordination of all chip R&D as well as increase the amount of cooperative R&D. The result should be improved efficiencies in R&D that would equal or exceed the present level of Federal funding for such work, he believes. The federal government alone spends $500 million annually in semiconductor R&D. This would be enough to restore the competitiveness of U.S. chip makers, Larry says. The grand total spent in the U.S. on chip R&D amounts to a surprising $4 billion a year. "This full investment is not being utilized," Larry maintains. "Nearly 25% is lost through unnecessary duplication." One inefficiency he cites is the time lost by not transferring R&D to other product areas.

If the trade bill doesn't make it, Larry says the amendment would be attached to another bill or even introduced on its own hook. "I think the semiconductor committee will happen this year," he says. It should be viewed as a modern test case for industry-government cooperation in restoring and maintaining technology capability that is important to the nation, Larry points out. It is not a government committee telling the industry what to do, he says, nor is it an industry committee telling the government what to do. It is a partnership that is attempting to address a national priority.

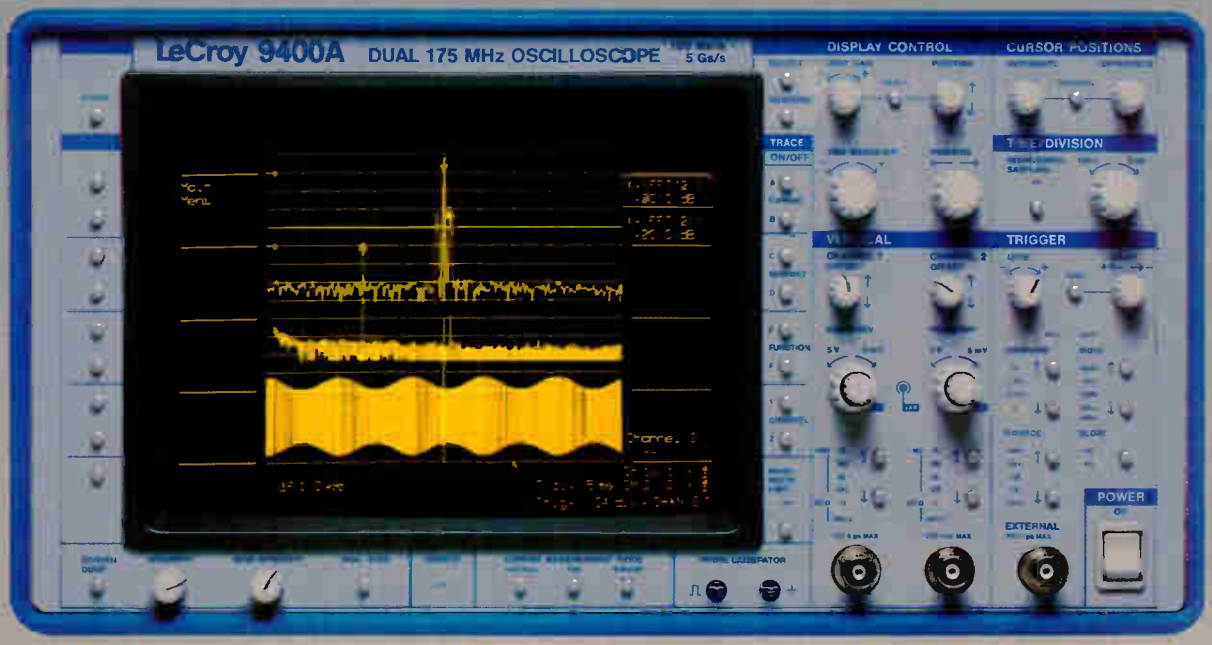
I have never believed in tightly managing R&D in a naive attempt to make it "more efficient." R&D should be viewed as exploration; if you don't explore, you don't discover.

ROBERT W. HENKEL

Long Memories

Accuracy

Mass Storage



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Circle 180 for Demonstration.

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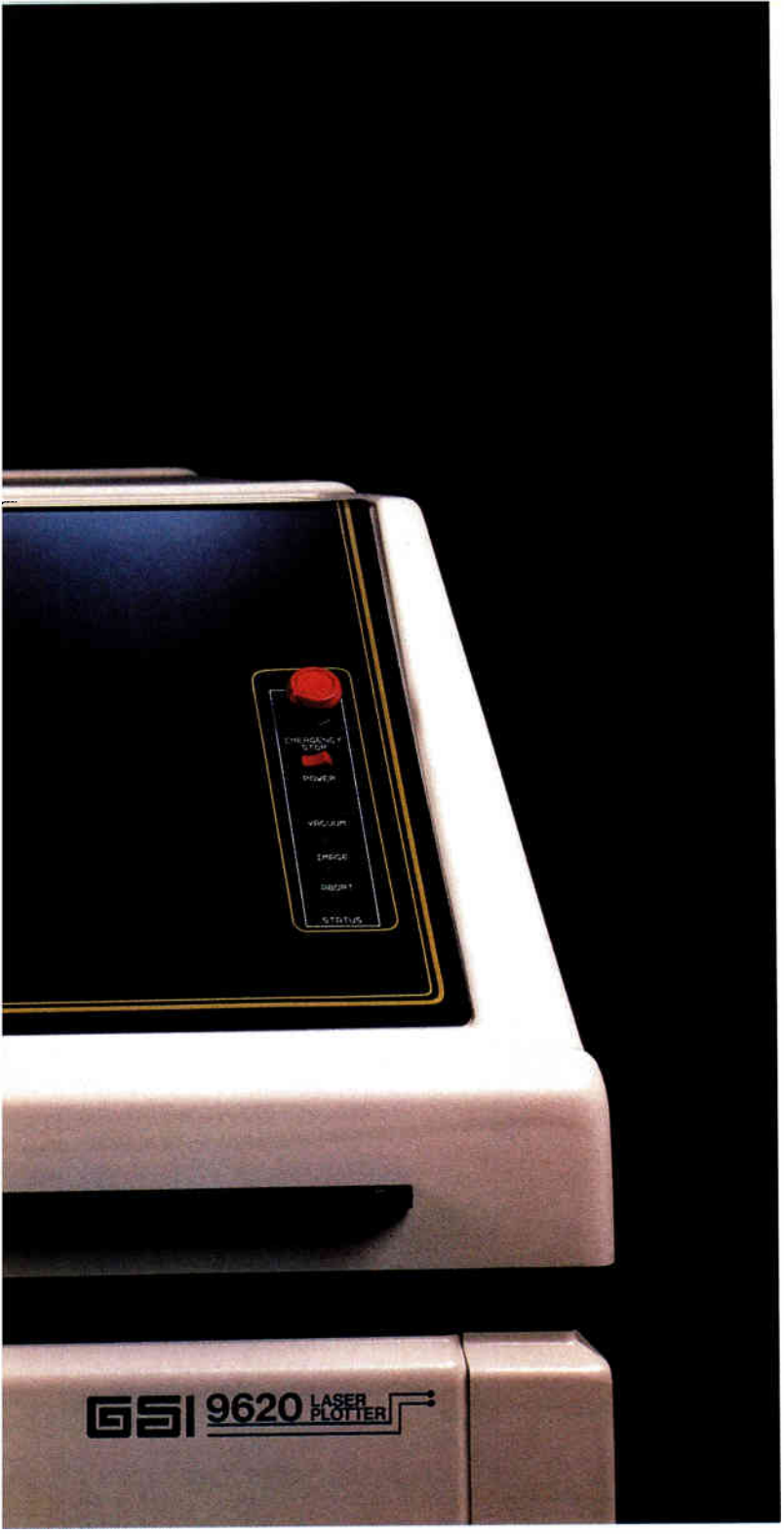

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Gerber

HIGHER TECH

620 beats competition.

Circle 11 on reader service card

LETTERS

That's 15 GHz, says Signetics

To the editor: Your special report on biCMOS [*Electronics*, Feb. 4, 1988, p. 55] was both timely and balanced. There was, however, an error in the description of Signetics' new biCMOS process. Our process is based on an advanced, self-aligned bipolar process, which has an npn maximum cutoff frequency (f_t) of 15 GHz, rather than the 7 GHz cited—the difference is significant. Adding the CMOS transistors to the process does not degrade the npn performance; it only adds to the design flexibility.

George Conner, Manager
Bipolar Technology Development
Signetics Corp.
Sunnyvale, Calif.

Who's first and who's latest?

To the editor: In an Electronics Newsletter [*Electronics*, Mar. 3, 1988, p. 22], reference is made to a study of smart-power devices completed by Electronic Trend Publications. That report is not the "first detailed report" on the smart-power market. In January 1986, BIS Mackintosh began its Power Integrated Circuits study, the results of which were delivered to 40 clients worldwide in July of that year.

The market values cited in the article by Mr. Selven correlate pretty well with those in the BIS Mackintosh study. Good work, Electronic Trend Publications, but you're two years too late!

George I. Stojsavljevic
Senior Marketing Representative
BIS Mackintosh Inc.
Natick, Mass.

☐ Gene Selven, publisher, Electronic Trend Publications, Saratoga, Calif., replies: *I feel a two-year-old report needs updating, especially where automotive markets, representing almost a third of the smart-power market by 1995, are concerned. We update some reports within two months of publishing them, normally within 1½ years as market conditions shift.*

I'm not disputing the fact that Mackintosh published the first study on smart power almost two years ago. But being first doesn't always mean you're the ultimate authority—unless our industry has gone "mature."

Correction: *In the table of supercomputer systems on p. 53 of the article "Supercomputers: The Proliferation Begins" [Electronics, Mar. 3, 1988], we goofed on the peak megaflops rating for the Ametek Series 2010. We gave 80 million floating-point operations as the peak—but that's with only four processors. At 20 mflops per processor, the 512-processor Series 2010 system should have been rated at 1,024 mflops, peak.*

ANALOG DEVICES

1mV, 1.5ppm Monolithic Voltage Reference

AD588

FEATURES
- Low Drift – 1.5ppm/°C
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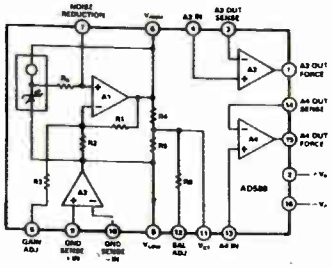

AD588 Functional Block Diagram

PRODUCT DESCRIPTION

The AD588 represents a major advance in the state-of-the-art in monolithic voltage references. Low initial error and low temperature drift give the AD588 absolute accuracy performance previously not available in monolithic form. The AD588 uses a proprietary ion-implanted buried zener diode, and laser-wafer-drift-trimming of high stability thin-film resistors to provide outstanding performance at low cost.

The AD588 includes the basic reference cell and three additional amplifiers which provide pin-programmable output ranges. The amplifiers are laser trimmed for low offset and low drift and maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high-current loads, delivering the full accuracy of the AD588 where it is required in the application circuit.

The low initial error allows the AD588 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD588 can provide a known voltage for system calibration in software and the low drift allows compensation for the drift of other components in a system. Manual system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD588 and autocalibration software.

PRODUCT HIGHLIGHTS

1. The AD588 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the zener or the buffer amplifiers and thus does not increase the temperature drift.
2. Long-term stability is excellent and the CD and TD versions are 100% tested and guaranteed for 25 parts-per-million stability in a 1000-hour period.
3. Output noise of the AD588 is very low – typically 6μV p-p. A pin is provided for additional noise filtering using an external capacitor.
4. A precision ±5V tracking mode with Kelvin output connections is available with no external components. Tracking error is less than one millivolt and a fine-trim is available for applications requiring exact symmetry between the +5V and −5V outputs.
5. Pin strapping capability allows configuration of a wide variety of outputs: ±5V, +5V & +10V, −5V & −10V dual outputs or +5V, −5V, +10V, −10V single outputs.

FOR THE WORLD'S MOST ACCURATE MONOLITHIC REFERENCE, REFER TO THIS PAGE.

If the voltage references you've been using have forced you to choose between low initial error and low drift, we'd like to refer you to our new AD588. With only 1mV of initial offset and 1.5ppm/°C of drift over temperature, it offers the best absolute accuracy possible in a monolithic reference.

This exclusive combination provides a range of user-programmable voltage outputs. You can choose from single +10V, +5V, −10V, and −5V ranges, simultaneous outputs of +10V and +5V, or −10V and −5V, or even a ±5V tracking range.

All of this is available with typical long-term stability of 15ppm, with selected versions tested for 1,000 hours and certified to be less than 25ppm. And you can get the AD588 for about half the cost of similar hybrid or in-house designs. Prices start at $12.75 in 100s, to be exact.

For the most accurate reference on the AD588, call Applications Engineering at (617) 935-5565, Ext. 2628 or 2629. Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

ANALOG DEVICES

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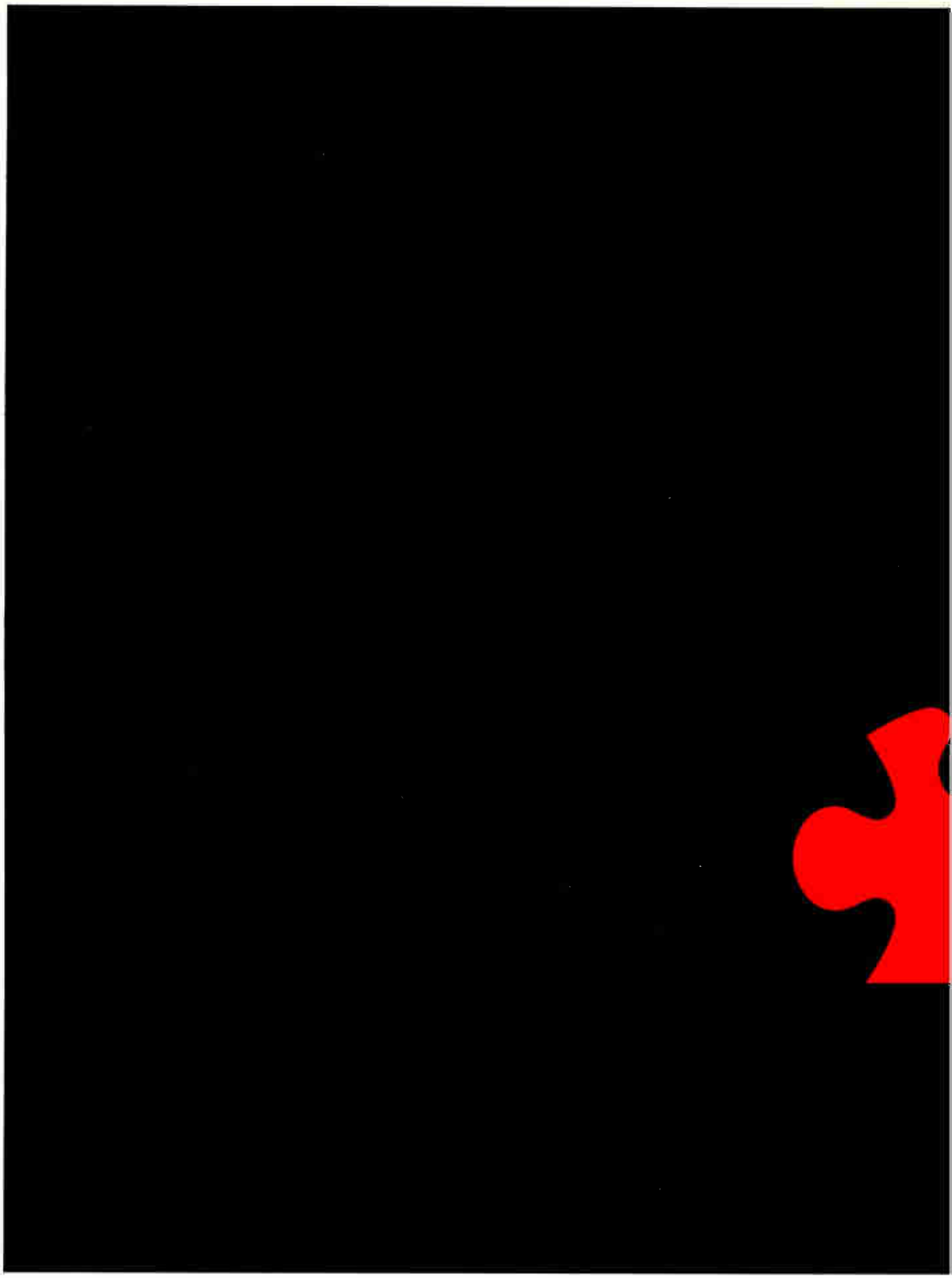
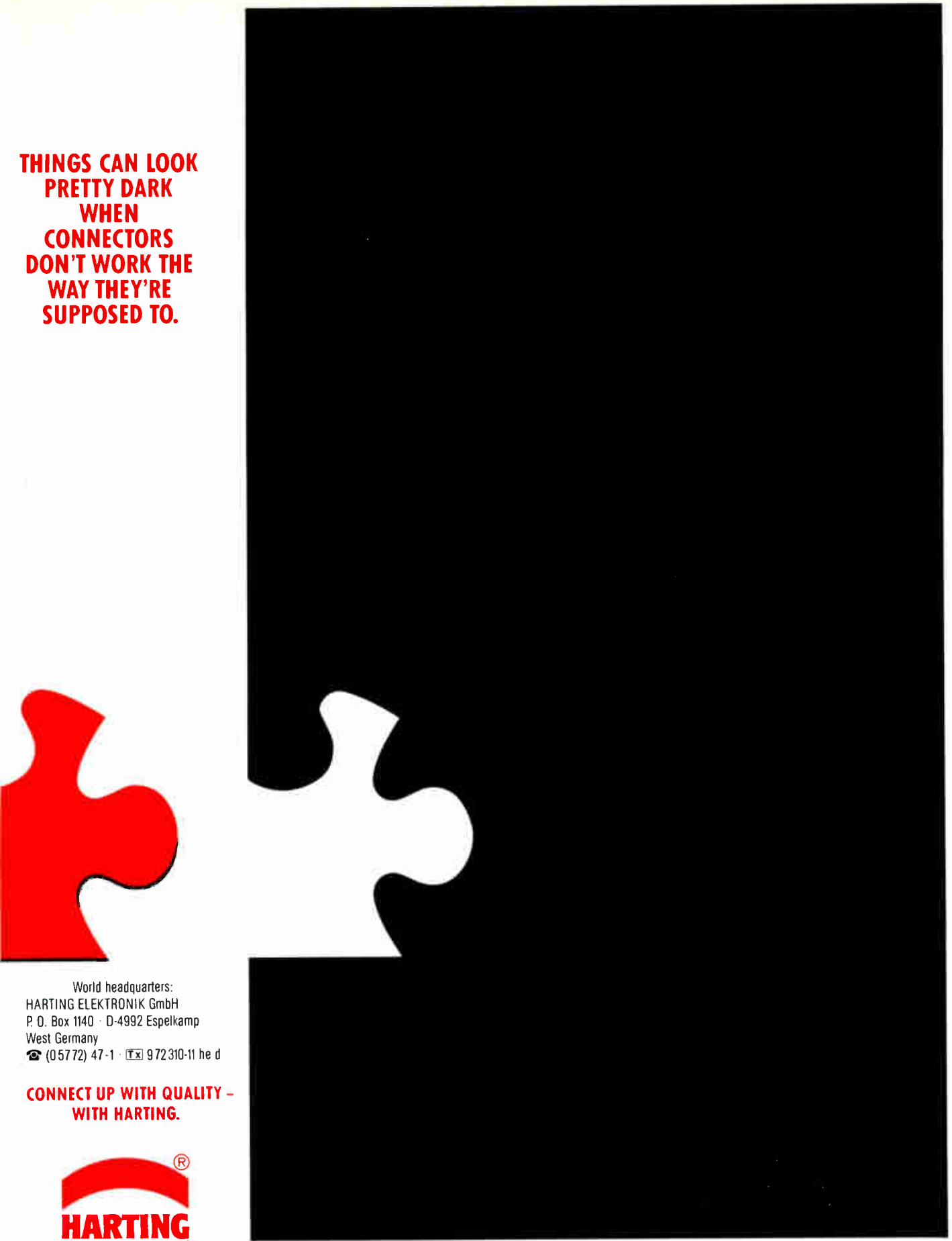
Circle 13 on reader service card



THINGS CAN LOOK PRETTY DARK WHEN CONNECTORS DON'T WORK THE WAY THEY'RE SUPPOSED TO.



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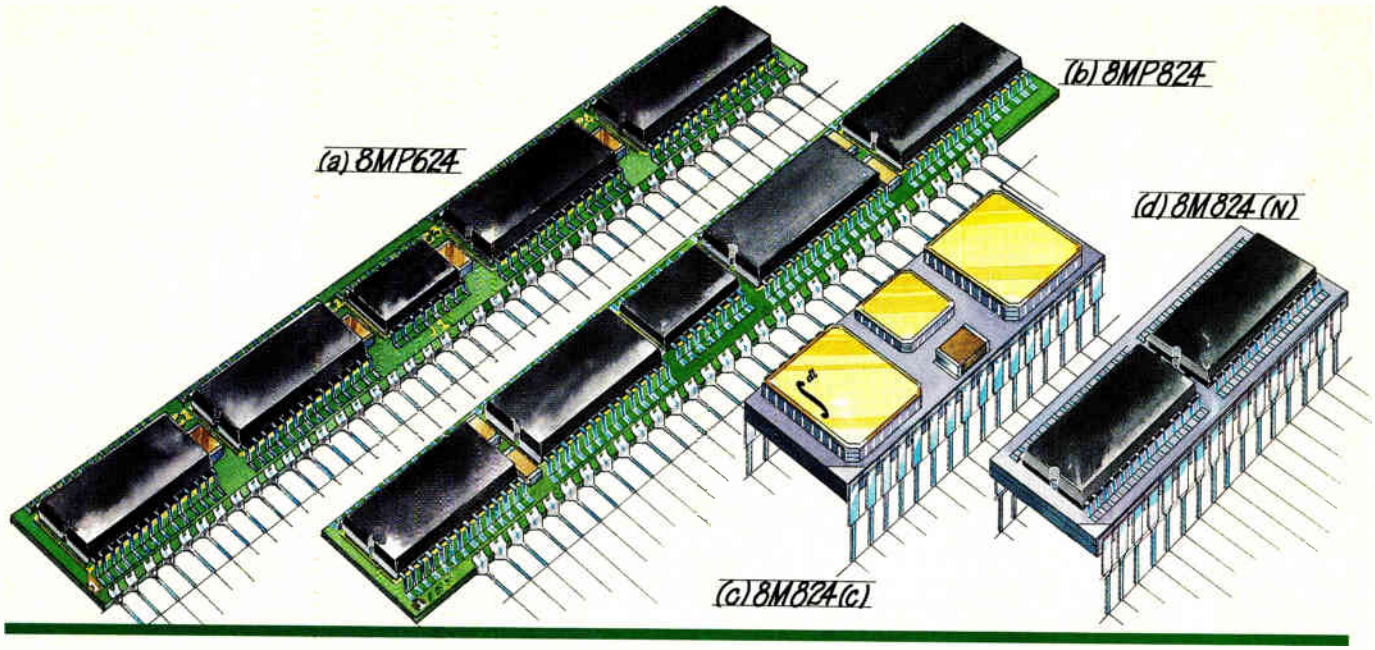

High-speed megabits give you an "unfair" advantage.

For example, the IDT8M824 JEDEC standard 128Kx8 is now at **45ns**. The IDT7M624 64Kx16 is **30ns**.

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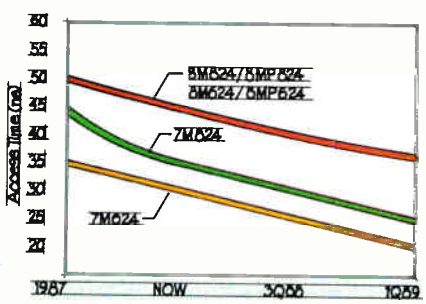

All of our very high-speed megabit modules undergo constant improvements in speed.

(a)	64Kx16	8MP624
(b)	128Kx8	8MP824 SIP
(c)	128Kx8	8M824(C) monolithic pinout
(d)	128Kx8	8M824(N) monolithic pinout w/SOICs
(e)	128Kx8	7M824 memory subsystem
(f)	64Kx16	7M624
(g)	64Kx16	8M624

128Kx8 memory subsystem cycles at 20MHz clock rate.
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On April 28, we'll reveal whether designing future computer systems will be worth the RISC.

Are standard microprocessors running out of steam? Many computer makers accustomed to building their products around them are now demanding performance that is outstripping what chip makers can deliver.

So in the frantic search for more speed, a growing number of computer system design managers are designing their systems around a burgeoning number of reduced-instruction-set computer (RISC) chips. What are the tradeoffs? Will RISC be a savior, or just a passing fad? In an important special issue, the editors of *Electronics* will examine the latest trends, and introduce the newest entries in the field.

What's more, this issue will also have the next installment in our 1988 Technology Series on Analog and Power. Coverage will include a special report on multiple-output OEM switching power supplies, plus technical articles on instrumentation amplifiers and smart power technology.

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80188	8048	68000	146805E2		6305V		6507		CDP6805D2		Z8002
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	8050	68010	6808		6309		6513	**Harris:**	80C86	**NEC:**	V20 V40
	8051		68B08		6309E		6514		80C88		V30 V50
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ELECTRONICS NEWSLETTER

MIPS RAISES THE ANTE IN THE HIGH-STAKES RISC GAME

The stakes in the fast-moving marketplace for reduced-instruction-set computers are going up again. MIPS Computer Systems Inc., of Sunnyvale, Calif., is making three announcements March 28 aimed at forcing its competitors in the Sparc camp (see story p. 34) to rethink their strategy. In rapid-fire succession, MIPS is unveiling its second-generation 32-bit RISC chip and floating-point coprocessor, announcing AT&T Co.'s endorsement for the application-binary interface that MIPS is using for its RISC chips, and disclosing its plans for a joint-venture company that will concentrate efforts on adapting software for MIPS-based hardware. MIPS speeded up the new chips, by scaling down from a 2-μm CMOS process to 0.8 μm and by revamping the internal architecture to reduce the number of cycles per instruction from 1.5 to 1.25. The result is a 25-MHz central processor that can run 20 million instructions/s, twice what the 16-MHz previous generation could handle. On the software front, MIPS and three chip partners—IDT, LSI Logic, and Performance Semiconductor—have formed Synthesis Solutions Inc., a new joint venture to develop software for MIPS-related systems. The new firm will be run by Owen Brown, former president of Sun Microsystems Inc., which is the chief backer of the arch-rival Sparc chip. □

MICROWAVE SEMICONDUCTOR AND TRIQUINT SHARE GaAs CHIP PROCESSES

Microwave Semiconductor Corp. and TriQuint Semiconductor Inc. are joining in what they say is the tightest second-sourcing agreement ever to hit the gallium arsenide chip industry. Because of the difficulties in fine tuning analog chips, such as MMICs (microwave/millimeter-wave integrated circuits), a traditional second-source agreement doesn't guarantee performance-compatible parts, says MSC president Saul Lederhandler. That's because it takes more than identical design rules to make identical analog chips—it takes identical processes too. So the two companies are using a 1-μm depletion-mode technology that can support linear, digital, or MMIC designs. They spent a year proving out the technology transfer, running a combined total of 400 wafers testing three designs in both fabs. The result, says TriQuint president Alan Patz, is that "we fall into a tighter window [of compatibility] than either company guarantees from run to run or wafer to wafer." Electrical performance comparisons between parts made at TriQuint's Beaverton, Ore., plant and those made by MSC in Somerset, N. J., were consistently closer than the 15% tolerance each company guarantees on its own line. □

ZILOG SHOOTS TO EXPAND ITS SHARE OF THE 8-BIT MICROPROCESSOR MARKET

While battles rage over 32-bit and reduced-instruction-set computer processors, Zilog Inc. is launching a souped-up, highly integrated version of its popular, but aging, 8-bit Z80. The Campbell, Calif., subsidiary of Exxon Corp. hopes the Z80180 will expand the life and size of its fading 8-bit star, now 10 years old. The new CMOS part marries a Z80 central processor with on-board memory management, two direct-memory-access channels, two universal asynchronous receiver/transceivers, two counters, timers, an interrupt controller, and an on-chip oscillator. The chip, which will be available in 8-MHz versions for about $11.45, is being aimed at embedded-control applications, says Jim Magill, components product marketing manager. He believes the Z80180 could potentially double Zilog's 8-bit microprocessor sales by providing a new migration path for higher performance to current Z80 users. But analysts suggest that the move is designed to head off defections to 16-bit chips. Dataquest Inc. estimates that Zilog's Z80 sales accounted for nearly 10% of the more than 60 million 8-bit microprocessors shipped world-wide last year. □

ELECTRONICS NEWSLETTER

COMING SOON: AN AI TOOL TO CONFIGURE MAP 3.0 NETWORKS

With Version 3.0 of the Manufacturing Automation Protocol factory networking scheme due out at midyear, the Industrial Technology Institute of Ann Arbor, Mich., is set to roll out a new tool to spur the lagging MAP market. MAPcon is an expert-system-based network configurator for MAP 3.0 that will initially run on a Texas Instruments Inc. Explorer computer under Knowledgecraft, an AI language offered by Carnegie Group Inc. of Pittsburgh. MAPcon is also being readied for use on work stations from Sun Microsystems Inc. MAPcon queries the user on a half-dozen key parameters on each device—computer, peripheral, machine, or robot—on the network. It then graphically constructs data-link, network, and transport parameter values—up to six dozen per device. In addition, if a particular set of devices cannot be configured under MAP 3.0, MAPcon alerts the user and suggests alternatives. MAPcon is available to members of the Institute's Group for Advanced Implementation of Networked Systems (Gains), a research cooperative. □

SHOULD INDUSTRY PLAY A LARGER ROLE IN FUNDING R&D?

Science and technology investments may be vital to the future of the U. S., but "the federal government can no longer do it alone," says Robert Dawson, associate director for natural resources, energy, and science in the Office of Management and Budget. "The old way of funding science and technology programs won't cut the mustard anymore. There is no money." Dawson says industry has to pick up more of the tab, but he isn't ready to recommend tax incentives or other financial perks to encourage R&D investment. "The government doesn't have the money for it," he says. Dawson would like to see more of private enterprise pursuing projects like the Industrial Space Facility, a privately funded man-tended space research station [*Electronics*, Sept. 17, 1987, p. 105]. Dawson says that by offering to guarantee $700 million in business for the system, the Reagan Administration is providing an incentive for the facility's owners to launch it. The administration is also trying to reinstate the R&D tax credit as a permanent tax incentive, he says. The credit is scheduled to expire at the end of this year. □

MITEL HAS AN INTEGRATED SOLUTION FOR ISDN's R-INTERFACE

Mitel Corp. is out to make it easier to design Integrated Services Digital Network systems for high-speed voice, data, and video communication. Its Semiconductor Division in Kanata, Ont., is offering a new hybrid device, the MH89500, that replaces the 20 to 25 discrete components now required to build an ISDN terminal adapter. The Mitel circuit handles functions of the R-interface in the ISDN reference model, which allows present-generation terminals, printers, and facsimile machines to tie into an ISDN network using current serial communication techniques, such as RS-232-C. Mitel plans to have a single-chip implementation of the R interface within 18 months. □

GTE'S 22-GHz LASER PROMISES HIGH-DATA-RATE VIDEO

Scientists at GTE Laboratories Inc. have produced diode lasers that operate at 22 GHz, topping GTE's own world record by 4 GHz. The Waltham, Mass., lab says the lasers could be used as sources in ultra-high-capacity optical-fiber transmission systems, carrying voice, data, and especially video signals. The light-emitting layer of the laser, made up of indium, gallium, arsenic, and phosphorous, is embedded between two layers of indium phosphide. GTE scientists used the same basic structure they developed for the 18-GHz laser, until now the fastest ever, but by thinning the light-emitting layer by almost 50% to 0.8-μm, they were able to boost the laser's speed. □

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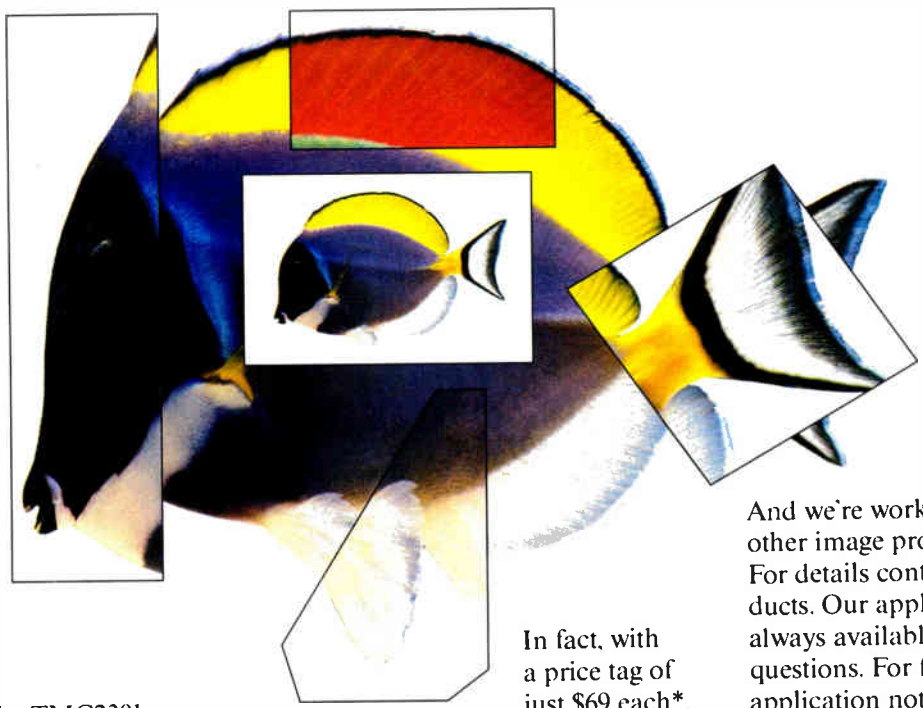

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DT2861 Frame Grabber	IBM PC AT	512x512	256	Yes	Yes	0–12 MHz	8*	Yes	Yes	16 buffers 512x512x8 each (4 Mbytes)	Yes	DT-IRIS IRIStutor	$4995

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PRODUCTS NEWSLETTER

G2'S PC AT CHIP SET LETS DESIGNERS RECONFIGURE PRODUCTS FROM SOFTWARE

Systems houses that target the IBM Corp. Personal Computer family can now build an AT-clone motherboard that handles future design changes—such as implementing faster memory—without redesign. G2 Inc.'s three-chip set integrates state machines that orchestrate a reconfiguration by using down-loaded software in on-board registers. The state machines on the CMOS GC131, 132, and 133 also let designers configure assembled host units for synchronous or asynchronous operation. The Milpitas, Calif., company's set implements an intelligent memory interface, a bus bridge for Intel Corp.'s 80386 running at 20 MHz, and peripheral support functions such as direct-memory controllers, clock generators, and interrupts. A motherboard requires the three-chip set, microprocessor, keyboard controller, clock, bipolar drivers, and memory. Available in May, the set costs $195 in 1,000-piece lots. □

RAYTHEON'S 1-MICRON CMOS GATE ARRAYS CUT POWER DISSIPATION IN HALF

A CMOS gate-array family from Raytheon Co. delivers a 50% power-dissipation advantage over the competition by using a proprietary 1-μm high-speed CMOS technology. Typical unloaded gate delays of the RL1000 series are 300 ps and core-cell dissipation is 8 μW/MHz—compared with 1.2 μW/MHz for competing 1-μm CMOS cells and 18 μW for the more common 2-μm technologies. Densities of the channelled arrays range from 5,670 to 20,440 gates and gate utilization on a typical design should be about 80%, say executives at the Mountain View, Calif., company's Semiconductor Division. Devices designed with the arrays operate at a 250-MHz flip-flop frequency, are compatible with TTL and CMOS input/outputs, and come with up to 160 I/O pins. Production prices based on 10,000-units/year sales are about $0.20/unit and design costs start at $25,000. □

TRANSTREAM'S T-1000 DOES AWAY WITH MODEMS AND TRANSMITS AT 64 KBIT/S

Modems are facing a stiff challenge in a data-transmission product from startup Transtream Inc. that delivers full-duplex, circuit-switched synchronous or asynchronous data transfers over two-wire telephone lines at up to 64 Kbits/s. The T-1000 switched-digital-data unit is the first product to make digital transmission between customer-premises equipment a reality, says the Agoura Hills, Calif., company. Instead of modulating and demodulating a voice line, it depends on the burgeoning use of digital switches by regional Bell operating companies. The first version of the T-1000 is compatible with Northern Telecom Co.'s DMS-100 central office switch and SL-100 PBXs. It is available now for an end-user list price of $1,095, with volume discounts available. Transtream will add support for switched digital services from AT&T by the end of the year through plug-in read-only memory software modules.□

KOPIN'S GaAs-ON-GaAs WAFERS BOAST LOWER DEFECTS

Kopin Corp. is now providing standardized GaAs-on-GaAs epitaxial wafers that outstrip the competition in defect densities by at least a 2.5 factor. The Taunton, Mass., firm's defect densities are less than 10 particles/cm² compared with 25 to 100 for competitors who measure defects. Having fewer surface defects contributes to higher speed in devices made on the wafers. Three-inch wafers with a buffer layer for low-noise applications sell for $450 each in quantities of 100; the same diameter with a power FET structure costs $555 each. Prices for 2-in. wafers with the same types of layers are $265 and $316, respectively. Prices for 4-in. wafers are not established. Kopin is also a supplier of gallium arsenide-on-silicon epitaxial wafers [*Electronics*, Oct. 15, 1987, p. 47]. □

PRODUCTS NEWSLETTER

VITESSE'S GaAs MULTIPLEXER HANDLES TELECOM DATA AT 1.24 GIGABIT/S

A major barrier has been hurdled to designing equipment that can handle the 1.24-gigabit/s data speeds called for in a proposed optical-fiber, broadband telecommunications standard. The VS8010, a gallium arsenide multiplexer/demultiplexer integrated circuit from Vitesse Semiconductor Corp., implements an 8-to-1 or 1-to-8 mux-demux on a single chip to meet the Synchronous Optical Network standard. Parallel 8-bit data received at a 155-Mbyte/s rate can be converted to a 1.24-gigabit/s serial bit stream, or the bit stream can be converted to bytewide data. Most of today's systems are limited to a 565-Mbit/s serial communications rate, according to the Camarillo, Calif., chip maker. The chip is the result of collaboration between Vitesse and Bell Communications Research, Livingston, N. J. Samples cost $980 and will be available in April. Production volumes will be ready in May. □

MOTOROLA'S MILITARY MOS FETS TAKE UP ONE-THIRD THE SPACE

Designers of military and high-end commercial systems that depend on high-packing-density printed-circuit boards can get a three-fold space saving with Motorola Inc.'s latest series of power field-effect transistors. Using a new, hermetically sealed package developed by Omnirel Corp., Leominster, Mass. (see p. 91), the devices take up about one-third the space of the standard TO-3 package. Specifications for the n-channel and p-channel power MOS FETS range from the MHR5N100's 5 A and 1,000 V to MHR35N10's 35 A and 100 V. Initially, Omnirel will assemble units for Motorola's Semiconductor Products Div., in Phoenix, Ariz. The devices have outlines similar to standard TO-218 and TO-220 plastic packages and will cost from $40 to $100 each in 50-unit quantities when they ship in the second quarter. □

NCR GIVES ITS STANDARD-CELL ASICS A 60% BOOST IN SPEED

A speed boost of about 60% is in store for circuits based on NCR Corp.'s 1.5-μm CMOS VS1500 standard-cell library, thanks to eight new high performance cells now available. The cells—five flip-flops, two latches, and a toggle—run from 30% to 100% faster than the original cells, NCR says. This provides a nominal toggle rate of 140 MHz with system clock rates up to 80 MHz. NCR's Microelectronics Division, Fort Collins, Colo., achieved the speedup through a redesign of the cells using nonstandard architectures. The new D flip-flop, for example, features extra transmission gates, added between the master and the slave portions of the circuit to perform look-ahead operations. NCR says the new cells make the VS1500 as fast as or faster than any competing 1.5-μm CMOS standard-cell library. Prototypes are in production, and typical nonrecurring engineering costs begin at around $44,500. □

INTERSIL'S CMOS FLOATING-POINT CHIP IS TWICE AS FAST AS BIPOLAR COMPETITION

By integrating multiply-and-accumulate functions on-chip, Intersil Inc. is making its ISP9326 32-bit floating-point-processor CMOS chip twice as fast as the bipolar competition. Designed to be compatible with Advanced Micro Devices Inc.'s AM29325, the 144-pin 9326 can perform a single-cycle 32-bit floating-point multiply-accumulation in 150 ns and handle 16 million floating-point operations/s in the multiply-accumulate mode. The 1.25-μm processor also holds a big edge in power dissipation—1 W compared to 9 W for the 29325. Targeted applications include math accelerators for single-board computers, digital-signal-processing systems (such as radar and sonar), computer graphics, and image processing. Available now, the processor sells for $495 each in 100-piece quantities. □

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Today, system designers look at speed, power and density. For good reasons. As CMOS gate arrays become larger and faster, designers can't meet their critical paths due to fanout and interconnect delay. As Bipolar arrays become larger and faster, power consumption becomes unmanageable. So AMCC designed a BiCMOS logic array family that merges the advantages of CMOS's low power and higher densities with the high speed and drive capability of advanced Bipolar technology. Without the disadvantages of either.

Our new Q14000 BiCMOS arrays fill the speed/power/density gap between Bipolar and CMOS arrays. With high speed. Low power dissipation. And, mixed ECL/TTL I/O compatibility, (something CMOS arrays can't offer).

For more information on our new BiCMOS logic arrays, in the U.S., call toll free (800) 262-8830. In Europe, call AMCC (U.K.) 44-256-468186. Or, contact us about obtaining one of our useful evaluation kits. Applied MicroCircuits Corporation, 6195 Lusk Blvd., San Diego, CA 92121. (619) 450-9333.

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Utilization	95%	95%	95%
Power Dissipation (W)	1.8	4.0	4.4
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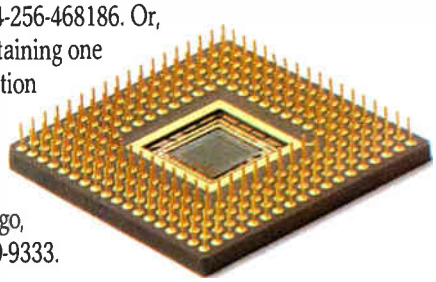

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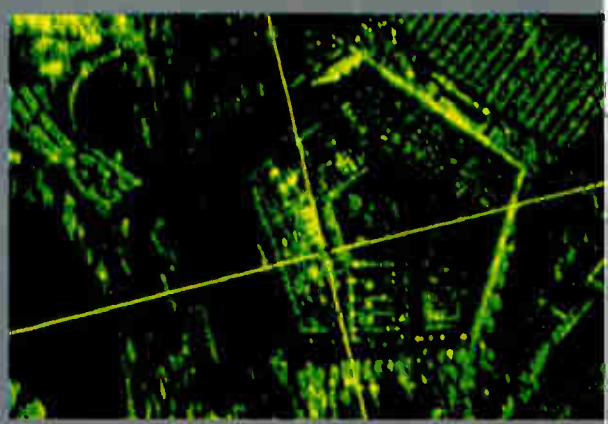
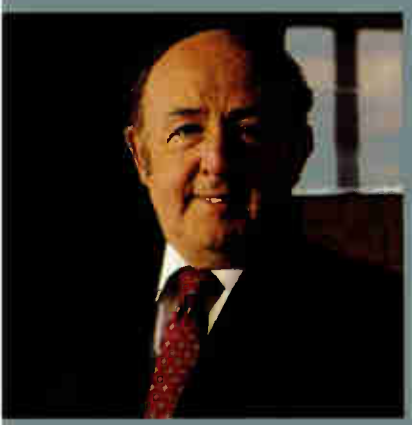


While developing software for the B1-B Bomber radar system, Westinghouse Defense landed on a tough problem – integrating its computer resources. "We needed a complete network that would allow hundreds of software engineers across the country to interact, create, enhance and modify the software," says Ron Clanton, Manager of Software and Information Systems.

The solution was a network from Digital.

Remarks Clanton, "The network is so comprehensive, it extends even to the air in our Flying Software Lab. Giving us real-time, in-flight software testing and development capabilities. The Software Lab alone provides a cost savings of up to 98% versus traditional in-flight testing in the B1-B Bomber."



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PAINT THE INTEL-MICRON DEAL RED, WHITE, AND BLUE

First all-American reseller pact carves out a new route for U. S. in DRAMs

SANTA CLARA, CALIF.

The selling of American-made dynamic random-access memories is taking on a new twist as U. S. electronics executives continue to rally around efforts to save domestic DRAM technology. Intel Corp. is rejoining the small ranks of American chip makers supplying domestic-made DRAMs—not as a maker but a reseller of chips fabricated by Micron Technology Inc. of Boise, Idaho.

The strategic agreement for 256-Kbit parts was unveiled by the two companies in Washington, D. C., on March 23 with fanfare that is common in the capital but unusual for announcements of industry alliances. One reason for the hoopla is that, although U. S. chip merchants have struck similar deals with Asian memory makers, this is the first between two American firms.

GREATER COOPERATION. Furthermore, proponents of greater U. S. industry cooperation can point to the Micron-Intel accord as evidence that such cooperation is occurring—the chip business is consolidating through partnerships aimed at reducing the risks of making commodity chips. The next move could come from National Semiconductor Corp., which is still deciding how to re-enter the DRAM market.

However, some analysts worry that such arrangements could actually worsen the shortage of DRAMs, at least initially, by lengthening the supply pipeline. And others note that the deal does not put any new fabrication capacity directly on stream.

But in Boise, Micron officials are jubilant. They say that the added security of having Intel as a steady customer plus the money from the planned sale of 600,000 shares of stock (at $19.375 a share) to the Santa Clara company will enable them to expand more aggressively in dynamic memories. "It enhances our ability to make decisions on investments," says Juan Benitez, president of Micron, which had 1987 sales of $91 million compared with Intel's $1.9 billion overall.

The agreement is part of a much larger Intel strategy to broaden into important but often risky commodity semiconductors while maintaining a focus on microprocessors and erasable programmable read-only memory products. The agreement is also Intel's second such DRAM deal. Last August, Intel eased back into the business by striking its

first DRAM-reseller agreement with South Korea-based Samsung. That agreement, similar to the one with Micron, allows Intel to buy DRAMs, label them as its own products, and resell them to distributors and customers. Since last year, Intel has been supplying limited volumes of Samsung-made 64-K-by-1-bit, 256-K-by-1-bit, and 64K-by-4-bit n-MOS DRAMs. Once Intel starts selling the Micron-made chips, in the third quarter of this year, it won't tell customers which parts are which.

VOLUME UP. Intel expects its volume of Micron 256-Kbit chips to increase as fab lines in Boise continue to produce more products. Micron is adding a new $100 million 6-in. line at its headquarters for 1-Mbit DRAMs and fast static RAMs, and the firm expects to use more of its existing capacity on 256-Kbit chips as the other memories are shifted over to the new fab next year.

"Intel is adding the key commodity semiconductors that are sold with Intel products," says Barbara Nelson, manager of Intel's nine-month-old Santa Clara Commodity Operation, which now focuses on memories but is expected to branch out. "Samsung was the first with their DRAMs, and now Micron is the second on the list. We will go from there into other commodities. We are aiming at high enough volumes to get our distributors excited, but it will be low enough that we are not going to make a difference in the market share of the business." *–J. Robert Lineback*

GALLIUM ARSENIDE

FORD BUCKS THE TREND BY SWITCHING TO ANALOG GaAs

COLORADO SPRINGS, COLO.

Just as other companies appear ready to push large-scale digital gallium arsenide integrated circuits into the real world, Ford Microelectronics Inc. is turning its focus to analog GaAs microwave ICs for the military. One reason: poor digital yields.

Ford has not cut back on overall GaAs funding at its Colorado Springs, Colo., facility—in fact, officials say it has upped spending "by several hundred percent" over the past two years. But most of the money is now being spent on technology aimed at the Defense Department's Mimic program (for microwave/millimeter-wave monolithic ICs), says Anthony J. Tether, vice president of technology and advanced development at Ford Aerospace, a Ford Microelectronics division.

Indeed, thanks to an innovative semicustom approach to building monolithic microwave ICs, Ford believes its team has a good chance of winning one of several Phase 1 Mimic contract awards expected from the Pentagon next month [*Electronics*, Nov. 26, 1987, p. 121]. Unlike the custom approach to Mimic circuits proposed by the 15 other Mimic

Phase 0 award winners, the team headed by Ford Aerospace is pushing an approach it dubs application-specific Mimic, or ASMimic.

The technique relies on a standard "footprint" circuit containing FETs, resistors, diodes, and other basic circuitry, which can then be personalized into any of several GaAs microwave circuit types by adding the final metallization layers. Ford says the method can slash Mimic circuit costs and development time to half that required for conventional custom approaches.

The Ford decision to deemphasize digital GaAs is being met with disappointment. Many other digital GaAs backers have been reporting improving yields and increasing shipments of digital semicustom GaAs parts [*Electronics*, Feb. 18, 1988, p. 40]. "It certainly is disappointing, because we had hoped we could extend our agreement with Ford to include products over the next six to 12 months," says Lou Tomasetta, president of Vitesse Semiconductor Corp., Camarillo, Calif. Vitesse announced an alternative-foundry source agreement with Ford last year to produce commercial LSI digital GaAs devices [*Electronics*, Sept. 17, 1987, p. 48].

Ford won't say how much it has spent so far on GaAs. But William I. Strauss, president of Foward Concepts Co., a Tempe, Ariz., consulting firm, estimates the figure at around $50 million. "We thought we could help offset the cost of this facility by also selling digital GaAs commercially," explains John R. Wallace, Ford Microelectronics president. But so far, "we've been very disappointed in our ability to do so," he concedes.

SPORADIC YIELDS. Good yields on Ford's self-aligned gate enhancement/depletion-mode digital GaAs process have been "sporadic," Wallace says. The firm took orders and did manage to ship a few prototypes of a 1,000-gate equivalent GaAs array, the 21G06, introduced to the merchant market about a year ago. "But it was at an internal cost that would have been outrageous if we had tried to recoup in the commercial market," says Ford Aerospace's Tether.

Both Wallace and Tether emphasize that Ford has not given up on digital GaAs. Spending levels are being held steady, says Tether. "Our plan calls for us to be at yields in the 5%-to-10% range by this time next year," he says. And Wallace doesn't rule out a move to license another firm's digital GaAs process later.

On the Mimic front, Tether says the company has already demonstrated an ability to produce "five or six" different GaAs microwave circuit types operating in the 0-to-30 GHz range based on a single ASMimic footprint. Likewise, Comsat—one of Ford's Phase 0 partners—has the process "well in hand" for faster 30-to-65-GHz circuits, Tether adds. Feasibility for 65-to-100-GHz circuits, the highest frequency targeted by Mimic, has yet to be demonstrated. "But we can't think of any reason we can't do it," Tether says.

Besides Comsat, Ford is teamed in the Mimic project with Harris Microwave Semiconductor, IBM, Pacific Monolithics, Singer, and TriQuint. If the team fails to win a Phase 1 contract, Ford will continue ASMimic development, "but at a much slower pace, and more for our internal needs," Tether says. "The current business plan is very aggressive," notes Wallace, and it is "keyed to winning Mimic." *–Wesley R. Iversen*

INTEGRATED CIRCUITS

LEADERSHIP HUNT LEAVES SEMATECH HANGING

COCOA BEACH, FLA.

Sematech is way behind schedule in naming a chief executive officer and the delay could be damaging. Recruitment for the semiconductor manufacturing consortium is at a standstill, and that imperils its goal of matching within two years the finest manufacturing line widths produced in Japan.

Everything is on hold until Sematech names a CEO and a separate chief operating officer. Until the two choices are made, a series of other moves intended to staff the Sematech facilities in Austin, Texas, is on hold.

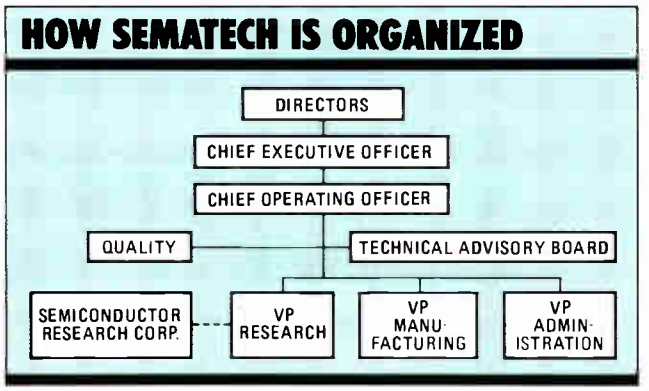
Larry Sumney, who has been Sematech managing director, acknowledges that delay in filling the top spots means "we'll have to work a lot harder" to meet the consortium's goals. He expects a CEO to be chosen within a month, but the original goal was to have one aboard last September [*Electronics*, May 28, 1987, p. 33]. Meanwhile, Sumney's managing-director position is being phased out. Sumney is also president of the Semiconductor Research Corp., Research Triangle Park, N. C., which will have a technology advisory role with Sematech.

But selection of the chief executive and chief operating officers is the linchpin that must be in place for all other recruitment efforts. Sumney says that Congressional funding and site selection had been important considerations for senior executives who are candidates for those jobs. In addition, any qualified candidate already has an important job that requires substantial travel, limiting availability for an interview.

"We want to have the CEO picked first because his opinion will be important in picking the chief operating officer," Sumney says. "The CEO will be Mr. Outside, working with the Congress and the industry. The chief operating officer will be Mr. Inside. I envision that person as being in his late 30s or early 40s, and just coming off a manufacturing line. He won't have a closed mind; he'll be someone with innovative ideas—a different view of how a manufacturing operation should run."

After Sumney's managing-director job is eliminated, its functions will be handled by an executive committee, which was chosen in the past few weeks to fulfill the functions of a chief executive until that person is in place. Members of that committee are Sanford Kane, vice president for industry operations in IBM Corp.'s General Technology Division; James Peterman, a vice president in the Semiconductor Group at Texas Instruments Inc.; and George Schneer, vice president and director of component quality and reliability at Intel Corp.

The second position to be filled, the chief operating officer, will be in charge of working out how Sematech meets its goals in device geometries. Phase 1 will rely on optical lithography to achieve an 0.8-μm baseline. Phase 2 has a target of 0.5 μm in optical lithography using a 1-Mbit static random-access memory as a demonstration vehicle; Phase 3 has dual goals of 0.35 μm in optical and 0.3 μm in X-ray



Now that Sematech has decided on its organization, it is still late in starting toward its goal: matching Japanese line widths in two years.

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lithography, using a 4-Mbit SRAM or 16-Mbit dynamic RAM as demonstration vehicles.

As for what Sematech has already accomplished, Sumney says that the top-level organization plan (see figure) and the consortium's five-year operating plan are in place. An annual operating plan is being written. So is the memo of understanding that is required before the federal government can implement the grants under which Sematech will be funded. The money probably will come in four equal payments, dividing the $100 million Congress appropriated for Sematech in the fiscal 1988 budget.

Further, Sumney says the Austin facility's clean room will be ready by September. Staffing the office will begin in April, however. The interim office in San Jose, Calif., will be closed in April or May, when the first members of a work force that will reach about 800 moves to Austin. *–Lawrence Curran*

COMMUNICATIONS

NOW, AN OPTOELECTRONIC IC REPLACES HYBRIDS FOR LANS

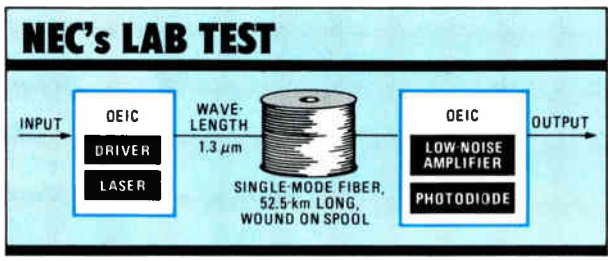
KAWASAKI, JAPAN

Researchers in Japan have come up with optoelectronic integrated circuits that could replace the hybrid circuits now in use and make optical local-area networks easier to implement. The researchers—working at NEC Corp.'s Optoelectronics Research Laboratories—have demonstrated that their long-wavelength devices can communicate reliably up to 52.5 km at 1.2 gigabits/s.

NEC's new entry consists of a transmitter chip with an indium phosphide laser and metal semiconductor FET drivers, as well as a receiver chip based on an InP photodiode. Commercial products should become available in about two years, says Mitsuhito Sakaguchi, general manager of the labs, who has high hopes for optoelectronic ICs. Sakagushi says he expects that demand for devices in LANs and subscriber circuits, including intelligent buildings and metropolitan networks, will eventually outstrip that for backbone telephone company lines.

The new devices should be easy to use in LANs because they are small and there is no need for assembly. Thus they should replace the hybrid devices now being used, mainly because earlier optoelectronic ICs could not match hybrids' performance.

In their experiments, NEC researchers injected a 1.3-μm-wavelength laser beam from an optoelectronic transmitter IC at a power level of -1 dBm into a 52.5-km optical fiber with a loss of 0.39 dB/km. The laser was modulated at 1.2 Gbits/s non-return-to-zero. Since loss in the line totaled 20.5 dB and the optoelectronic receiver IC's sensitivity is -26 dBm, there was a margin of 4.5 dB.



In this lab setup, NEC researchers used optoelectronic ICs to communicate reliably over 52.5 km of fiber at 1.2 Gbits/s.

Until now, designers of optoelectronic ICs for LAN s faced a cruel dilemma in materials. All their circuit-device experience in compound semiconductors has been with gallium arsenide, but indium phosphide is needed to make optical devices that operate in the 1.3- and 1.55-μm long-wavelength bands favored for long, repeaterless spans.

The NEC engineers found a way around this problem: they used molecular-beam epitaxial growth to fabricate a heterostructure with single-crystal GaAs on a semi-insulating InP substrate. Devices are fabricated in a 0.2-μm-thick GaAs layer atop a 0.8-μm GaAs buffer layer. The quality of the GaAs epitaxial layer is equal to that of layers grown on GaAs substrates. The InP laser on the transmitter chip and the p-i-n photodiode on the receiver chip are fabricated by standard liquid-phase epitaxial growth or vapor-phase epitaxial techniques. Integrating the GaAs driver metal semiconductor FETs and the InP laser on the transmitter enables operation at signal rates up to 2.4 Gbits/s. Maximum laser power output is more than 10 mW.

The receiver chip has an InP photodiode connected to GaAs MES FETs that are configured as a low-noise wide-bandwidth transimpedance preamplifierthat converts a low-power photocurrent input into a higher-power voltage output.

The sensitivity of the chip is rated at -26 dB below 1 mW with a dynamic range of more than 25 dB. Unlike the transmitter chip, which is efficient at all frequencies up to about 2.4 Gbits/s, the receiver is optimized for operation at 1.2 Gbits/s by a feedback resistor in the amplifier. *–Charles L. Cohen*

SOLID STATE

MORE AND MORE, IT'S SPARC VS. SPARC

SAN JOSE, CALIF.

The Sparc campaign is entering a new phase as the chip houses that have enlisted behind Sun Microsystems Inc.'s reduced-instruction-set microprocessor prepare to battle each other. That is a major change; up to now, the chip makers concentrated on capturing individual pieces of the speed spectrum as they worked to develop and promote their own versions of Sparc—Scalable Processor Architecture.

But it's no more Mister Nice Guy. Fujitsu Ltd.—currently the only supplier of circuits for Sparc systems, with chips rated at 10 million instructions/s—now has a product road map leading straight to 40 mips by mid-1990 (see figure, p. 45). That will put it head to head with the Sparc chip due from Bipolar Integrated Technology Inc. of Beaverton, Ore., in early 1989. The territory in between—30 mips—is occupied by the Sparc chip coming from Cypress Semiconductor Corp. of San Jose, Calif.

Managers at Fujitsu's Advanced Products Division, which recently moved to San Jose from nearby Santa Clara, are pressing the new-product strategy because they say Sparc has gained momentum faster than they expected since they introduced their 10-mips 20,000-gate-array-based product last summer.

Full-custom design of a new integer unit is underway, and Fujitsu is planning CMOS microcores for semicustom processors, a powerful new 64-bit Sparc-oriented floating-point unit, and a memory-management unit.

Fujitsu's broadened commitment isn't the only indication of a new Sparc era. It comes on the heels of LSI Logic Corp.'s decision to become the fourth firm to back Sparc (while also embracing a competing RISC design from MIPS Computer Systems Inc.). The Sparc backers are fighting for what is still a tiny segment of the 32-bit microproces-

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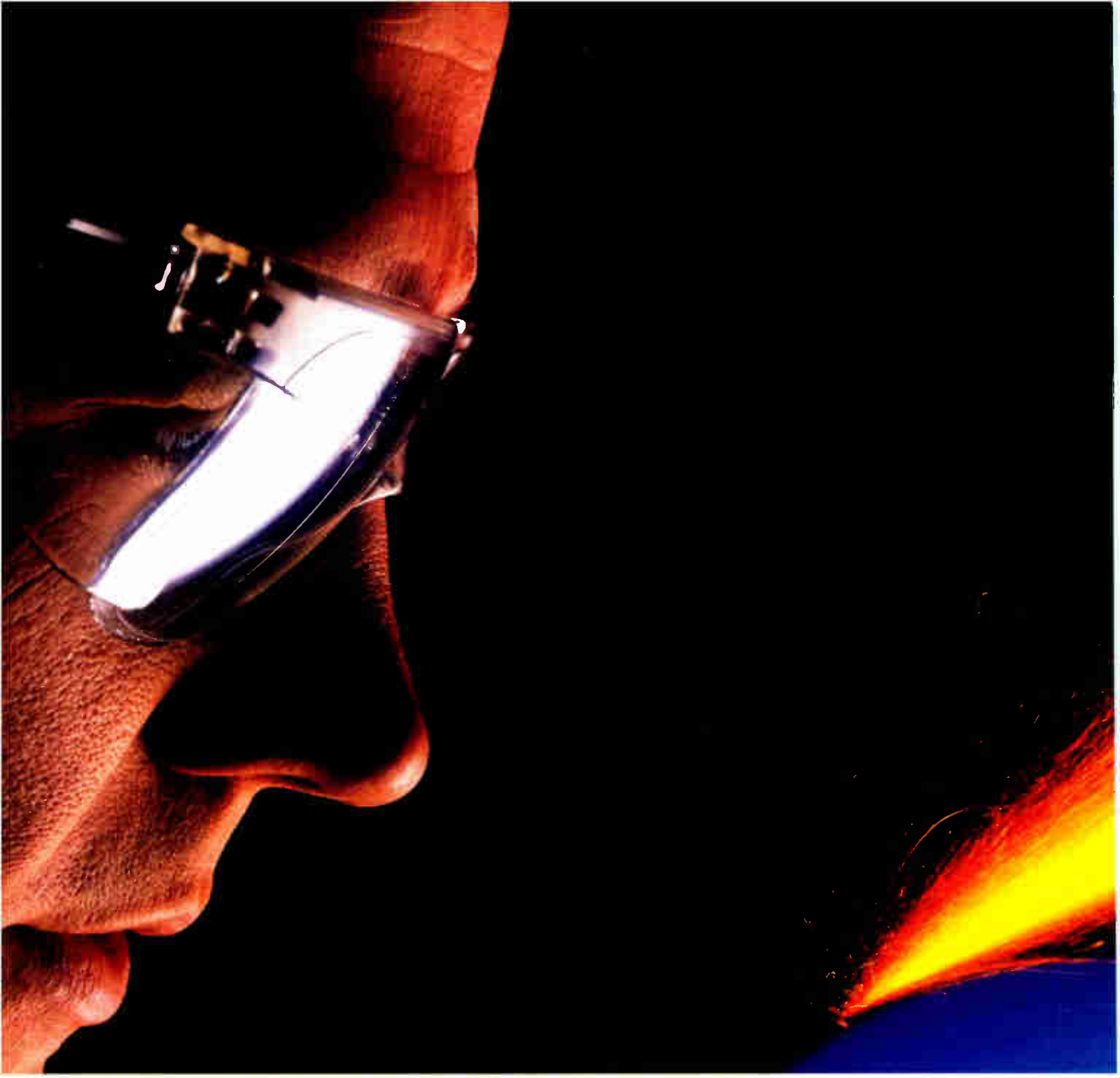

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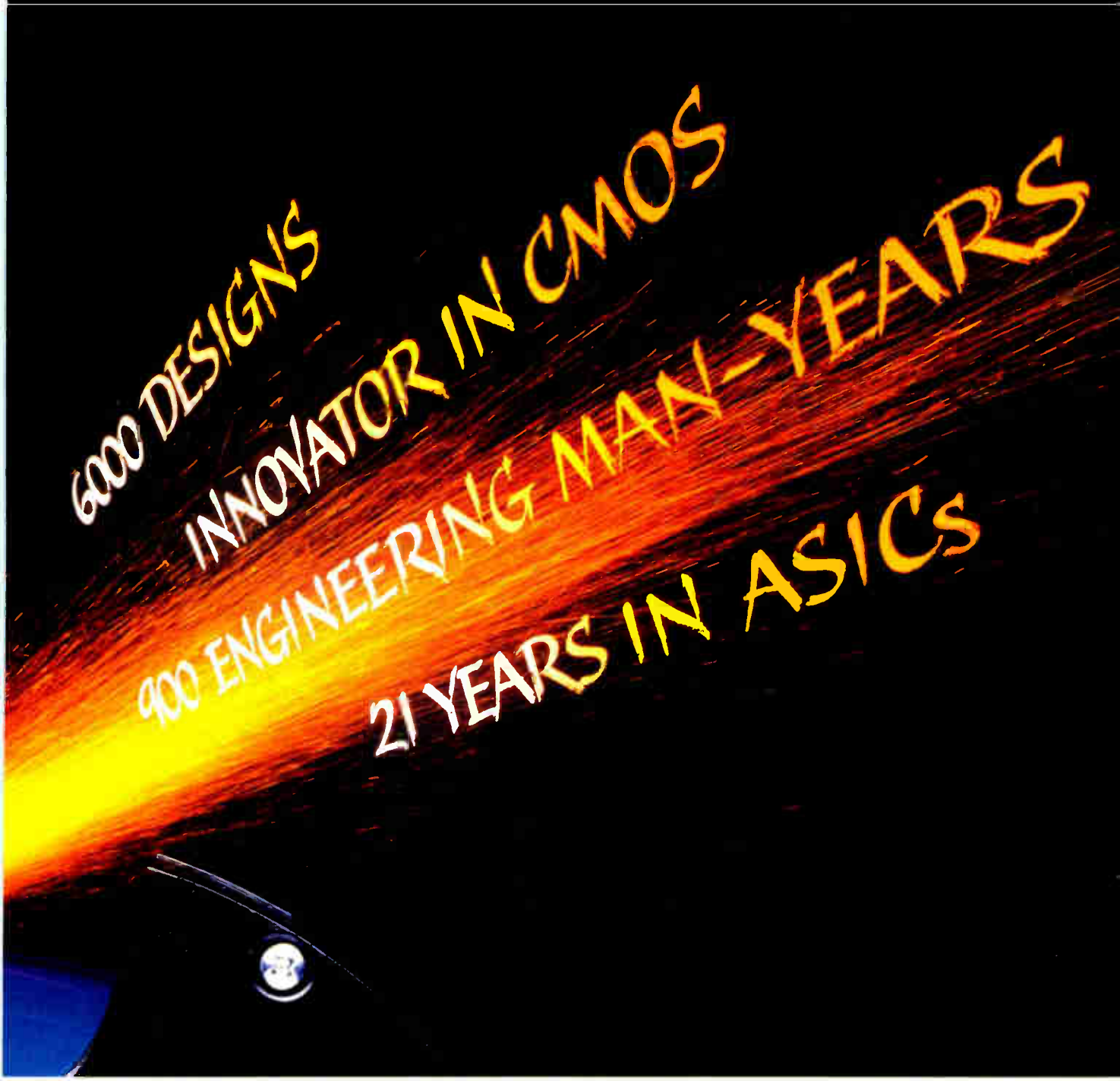

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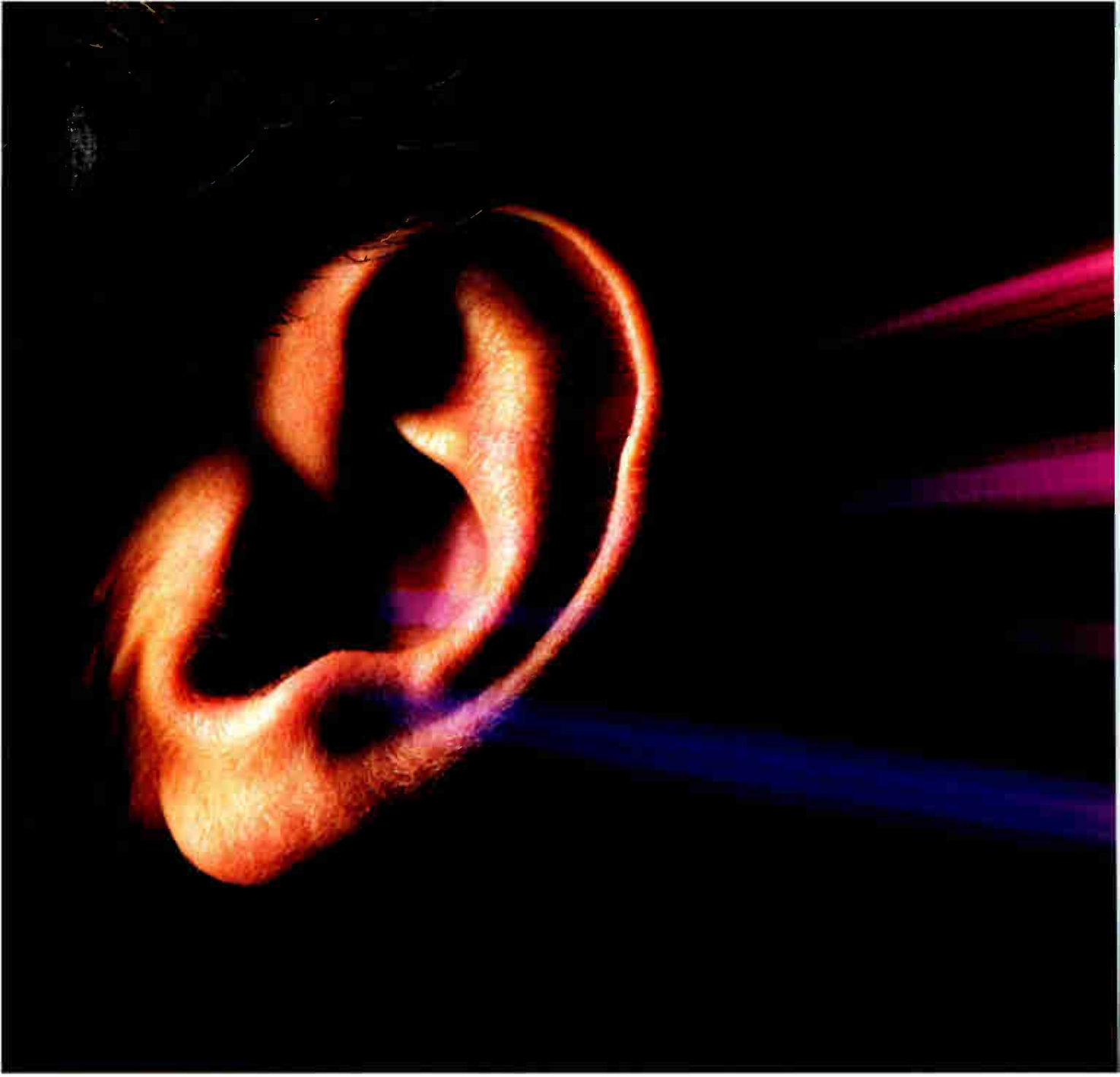

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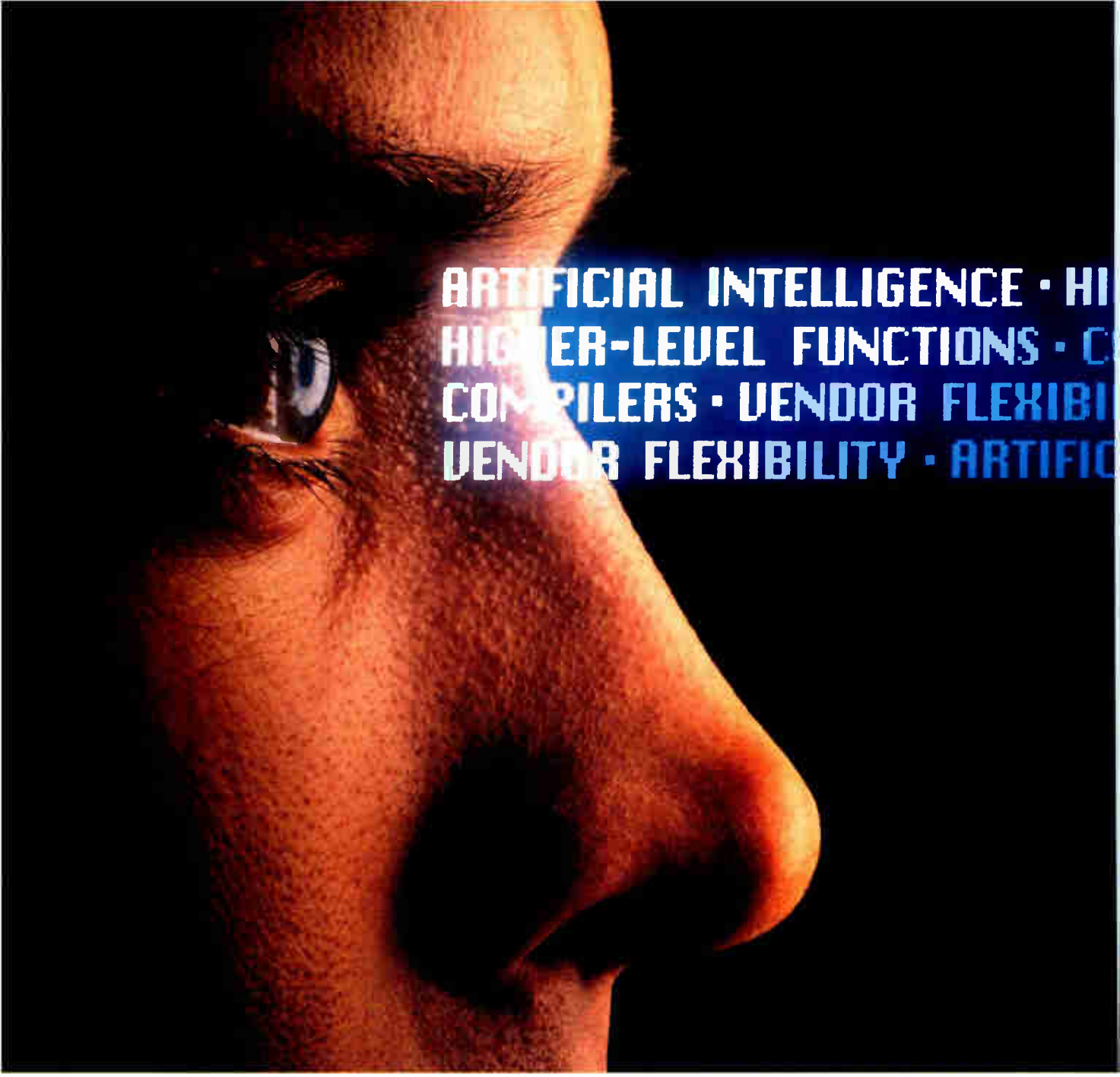

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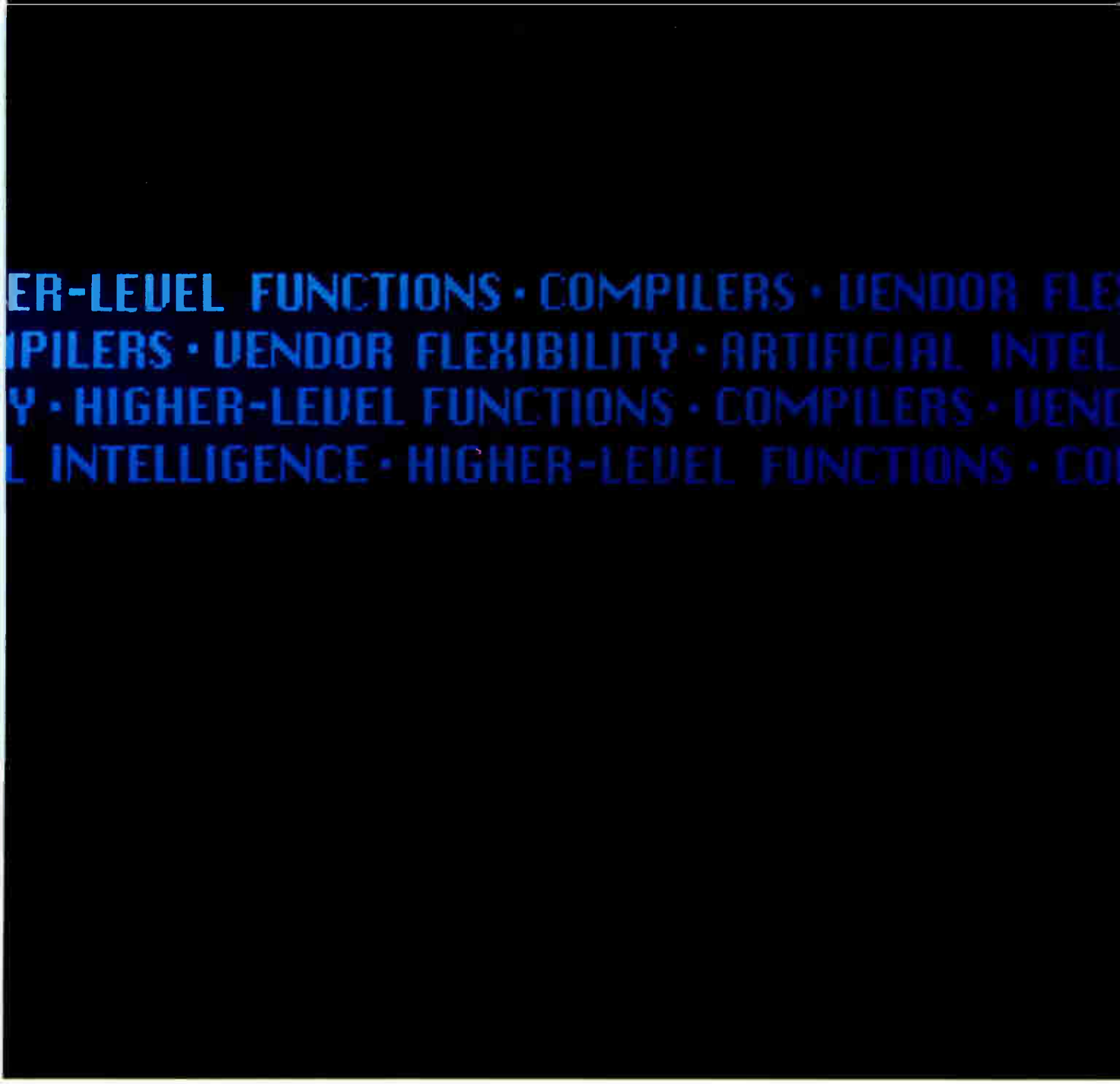

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sor market, but one that is about to explode.

Dataquest Inc., the San Jose-based market research firm, estimates that all the RISC camps combined will account for 20% of the roughly 27 million 32-bit processors that will ship in 1992.

Dataquest analyst Alice Leeper notes that because each Sparc chip maker is planning different implementations of the architecture, they are not alternate sources. And that means each must win customers. "It is still a confused market," she says. "There is no question when you've got as many players in a small arena, there is going to be a shakeout within just a few years."

Meanwhile, both LSI Logic and Fujitsu are going full speed ahead. They aim to ship this summer competing, yet software-compatible, integer and floating-point controller chips capable of delivering 15 mips at 25-MHz clock rates. Cypress is preparing to ship samples of its 20-mips Sparc products in the summer, and 40-mips emitter-coupled-logic Sparc is expected from Bipolar Integrated Technology in the second half of the year.

LSI Logic plans within 18 months to have a 40- to 50-mips Sparc processor made with biCMOS. The company will start in mid-1988 with a 1.5-μm drawn gate CMOS product offering 15 mips, and increases in performance are likely every 6 to 12 months, says Wilfred J. Corrigan, chairman of the Milpitas, Calif., company.

FUJITSU'S SPARC SCHEDULE

Mips	Scheduled	Chips	Technology	MHz	Features
10	First Sparc chip: summer 1987	4	1.3-μm CMOS	16	• Based on 20,000-gate array • Integer unit; floating-point controller
15	Samples: July 1988	2	1.5-μm CMOS	25	• Standard-cell-based IU • Custom FPC from outside
20	Samples: March 1989	3	1-μm CMOS	33	• IU, FPC, floating-point unit • Full custom • Could include a memory-management-unit chip
40	Mid-1990	NA	To be selected	NA	NA

Fujitsu, meanwhile, is gearing up to reach 40-mips performance in three stages, starting in July with a 1.3-μm standard-cell-based integer unit. With a Sparc-specific floating-point controller, it will run at 15 mips. The new part, to be called S-25, will be housed in a 179-pin plastic pin-grid array and is expected to cost less than the current 256-pin 10-mips part, which requires a separate 20,000-gate array floating-point controller unit. Fujitsu plans to introduce a 20-mips three-chip set, running at 33 MHz, in March 1989. Susan Mason, marketing development manager for the product, says the process will be 1-μm CMOS.

The 20-mips integer unit, called S-33, is being designed from the ground up with a full custom layout. Fujitsu is also working on a high-performance floating-point controller and its own floating-point coprocessor compatible with IEEE standards. Then, within a year, there will be a memory-management unit.

Beyond 40 mips, Fujitsu is working with two or three U.S. customers to determine if a higher performance offering should be based on ECL technology, and if so, whether it will be a custom product or available commercially. Ken Katashiba, senior vice president for the Advanced Products Division, says the issue is a matter of cost and size of market potential. In addition, he hints that the Japanese-based firm also has in its technology bag gallium arsenide and high-electron-mobility transistors for even higher performance should market need appear. – *J. Robert Lineback*

MILITARY

HERE'S A WAY TO CLOSE THE GaAs WAFER GAP

PARIS

Two French companies have come up with what they say is a sure-fire combination to overcome the expected shortage of gallium arsenide wafers for the U.S. Department of Defense's Microwave and Millimeter Wave Integrated Circuit program.

One company is ISA Riber, a division of Instruments SA in the Paris suburb of Rueil-Malmaison. It has come up with a molecular-beam-epitaxy machine—the first of its kind—that can handle a dozen GaAs wafers at a time instead of the usual one [*Electronics*, March 5, 1987, p. 38]. The other company is Picogiga SA, a two-year-old startup and a producer of wafers that come with epitaxial heterostructures. Paris-based Picogiga intends to boost its output at least tenfold by using ISA Riber multiwafer machine.

Besides the boost in output, the price will be right, says Lihn T. Nuyen, president of Picogiga. He maintains the yield of the new machine, which was designed to Picogiga's specifications, will run as high as 90%, much better than possible with the main two competing technologies—ion implantation and metal-organic chemical vapor depostion. As result, Nuyen says, chip costs can come close to meeting the Pentagon's target of $20 chips for phased-array radar transceiver modules [*Electronics*, Nov. 26, 1987, p. 121].

The multiwafer machine, not yet named or formally announced, will be able to produce about 2,000 high-quality wafers per month, reports Pierre Bouchaib, director of ISA Riber's Semiconductors and Advanced Materials Department. Delivery of the first machine to Picogiga is slated for late 1988.

"The challenge was designing a machine that can handle a lot of wafers with the same specs [1% to 2% uniformity in the expitaxial layers] a mono-wafer machine," says Bouchaib. ISA Riber's computer-controlled machine—the base price is between $1 million and $1.2 million—will achieve anywhere from 5 to 10 in-spec 3-in. wafers or one in-spec 6-in. wafer for each batch of 12. "With metallic organic chemical vapor deposition, you can do maybe 20 wafers in the same reactor but to get to specs you lose 18 wafers at $1,000 each," he says. And he adds that the new machines turn batches out much faster because there are no gases to be flushed out after each run as there are in metallic organic chemical vapor deposition.

All of which should be welcome news for the Pentagon, where Picogiga's Nuyen has been airing his ideas on GaAs this week. He's trying to get the DOD to urge Mimic participants to use his company as a second source for wafers. The $500 million Mimic project could call for as many as 200,000 GaAs chips per month, compared with the current annual output of 300,000 [*Electronics*, Jan. 21, 1988, p. 83].

Such a sudden boost in chip demand would swamp the current capacities of U.S. wafer suppliers, who are using time-tested technology with low fabrication yield for military projects. Meanwhile, Nuyen points out, the Japanese have shown that the capability needed for the Mimic project—a combination of GaAs wafers with molecular-beam epitaxy and high-electron mobility transistors—does exist. They are using it for

heavily produced consumer products like direct-broadcast satellite-receiver front ends. And they are using molecular-beam epitaxy GaAlAs wafers to make the diodes used in compact-disk players.

With the machine being built for it by ISA Riber, Picogiga alone could supply, at the right price, 20% of the wafers needed for the entire Mimic program. The key, Nuyen says, is utilizing advanced GaAs wafers, which have very thin epitaxial layers of GaAlAs and GaAs atop a semi-insulating substrate, to fabricate HEMT or heterojunction bipolar transistor structures. "The reason people like MBE is because you can control the doping and thickness of your epitaxial layers very closely," says Eliot Cohen, director of the DOD's Mimic Program. "But the problem with MBE is that it's very slow."

Nuyen figures the new machine can banish that problem. Therefore, he says, "for the Mimic program, this is really the way to go." He admits that at first glance, wafers processed using molecular-beam epitaxy look expensive. At $2,000 for a 3-in. wafer on the average, they cost seven times as much as those processed with ion implantation and more than half again as much as $1,200 wafers with epitaxial layers put down by metal organic chemical vapor deposition.

But when fabrication yields are factored in, molecular-beam epitaxy turns out to be the most cost effective, Nuyen insists. Right now, he explains, with 150 Mimic chips per wafer, cost per chip runs $153 for molecular beam, $573 for vapor deposition, and $716 for ion implantion. By 1992, by which time the new generation of process equipment should be in full swing and chip prices dramatically lower, the difference will be almost as marked: $27 per chip for molecular beam, $56 for vapor deposition, and $93 for ion implantation.

Still, Nuyen knows he has another problem—convincing U.S. semiconductor specialists to put molecular-beam epitaxy on the production floor. "MBE is so sophisticated, many people think of it as just a research tool. We believe we have demonstrated that it can be done in a production environment." Japanese firms, he points out, have snapped up Picogiga's first generation of HEMT wafers for consumer products. Picogiga, in fact, shipped 700 wafers in 1987, for prices between $1,000 and $3,000. The company now sells three types of wafers: one for HEMTs and pseudomorphic HEMTs (with gallium indium arsenic alloy); one for heterojunction bipolar transistors; and one for quantum-well lasers.

–Jennifer Schenker

BUSINESS

JAPANESE MANUFACTURERS FLOCK TO MEXICO

TIJUANA, MEXICO

Japanese companies are rushing into Mexico to take advantage of cheap labor and other favorable economic factors that make it among the world's cheapest manufacturing places. And the boom along the U.S. border is expected to grow even more as other Pacific Rim countries build and expand plants.

Giant companies such as Sanyo, Hitachi, and Matsushita are leading the Japanese incursion. Growth is most rapid south of San Diego, Calif., particularly in the Otay Mesa section of Tijuana, although activity is apparent all along the boundary.

The investment growth rate by the Japanese in the area is 25% annually, according to the San Diego Economic Development Council. The council, instrumental in attracting such investment, says that the latest surge began late 1986 when the yen gained strength against the dollar. The net effect forced Japanese firms to shift high-priced domestic manufacturing offshore to less expensive locations.

An even stronger investment wave may be in sight, says a consulting firm that offers services in establishing start-ups in Mexico. Enrique Esparza, president of AIM Inc. in Chula Vista, Calif., predicts that companies from Korea, Taiwan, and Hong Kong will intensify the boom. "They will be setting up business in Mexico very soon," within a year, he says. AIM says it has 38 clients, including Fortune 500 companies, and is grossing about $30 million yearly.

In fact, the first major Korean invest-

As Japanese companies flock to Mexico, the biggest concentration of plants is south of San Diego.

ment surfaced a few weeks ago. Seoul-based Samsung Group, the consumer electronics firm, announced it will start doing subassemblies for its television sets in Tijuana later this year. The company plans to later expand into other goods.

Mexican plants are attractive because of hourly labor rates of $1.00 to $1.25—about one-seventh the level of the U. S. and other industrialized nations. U. S. electronics companies in California have taken advantage of the disparity since the 1960s by establishing plants under what Mexico calls its maquiladora program. The plants assemble components shipped south from the U. S. and send back finished products; taxes are levied only on the value added.

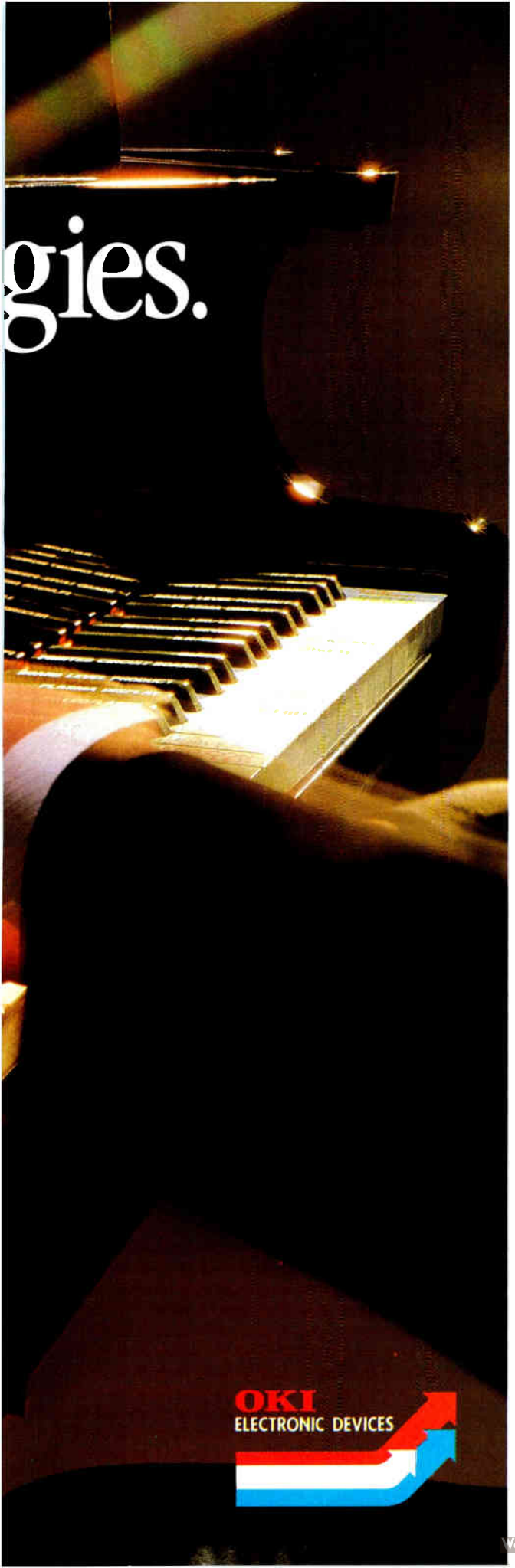
Not all companies may qualify for the maquiladora program's tariff advantages that are available. But even then there are other enticing reasons to build large plants. sources say. In addition to the cheaper labor, reasons for shifting production to Mexico include the low cost of the infrastructure needed to manufacture products as well as the proximity to U. S. markets.

The case of Sanyo Electric Co.'s new automated battery plant, which opened this month in Tijuana, makes a good example. Labor constitutes only about 10% of battery-production costs, estimates Yasuo Sasaki, who is in charge of property investments in North America for Sanyo. But factoring in the lower costs for real estate, utilities, and support services along with efficient equipment brought from Japan brings production expenses for Sanyo batteries down to nearly half that in industrialized countries.

Sanyo plans to aggressively exploit the advantages—production capacity at the plant initially is set at 800,000 batteries a month, and will be expanded for the world market.

BIG IN TIJUANA. Sanyo is a major presence in Tijuana, with three other plants for television sets, refrigerators, and fans. Its TV plant is expected to be the largest electronics operation in Tijuana with some 500,000 ft² of space. It will house nearly 3,000 employees when it gets into full-scale production, according to a study compiled by the U. S. Embassy staff.

But the maquiladora concept will also remain a strong inducement. The same U. S. Embassy study predicts that there will be an increase in companies that take advantage of the value-added tax rule, in addition to the anticipated jump in direct investments from Asian nations. It estimates that Japanese companies alone will be opening about 100 plants a year that qualify for maquiladora status through the early 1990s—with at least half of them electronics operations. *-Larry Waller*



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INTERNATIONAL NEWSLETTER

APPLE COMPUTER SETS UP AN INTERNATIONAL HEADQUARTERS IN PARIS . . .

It's back to Europe for Michael Spindler. Having been called home to Apple Computer Inc.'s Cupertino, Calif., corporate headquarters in 1984 to unify the company's international businesses, the president of Apple Computer International is now off to Paris to run the fast-growing division from a base being set up there. Spindler expects that the company's total international business, including Japan and the Pacific Basin, will represent more than a third of the company's sales before 1990 [*Electronics*, Dec.17, 1987, p. 8]. Its European sales, which he believes will surpass $1 billion in 1988, are growing at a blazing 80% annual rate—compared with 50% for the company as a whole. Nearly all Apple products sold in Europe are built there, thanks in large part to a state-of-the-art flexible-manufacturing plant in Cork, Ireland. The automated production line in Cork can respond instantly to new orders so that systems and peripherals can be delivered anywhere in Europe in less than 72 hours while local stocks contain only low-cost parts such as keyboards. □

. . . AND OUTLINES A NEW INTEGRATION STRATEGY FOR OPEN SYSTEMS

Part of Apple's new Paris facilities will be a new research-and-development center for work on data communications, peripherals, and software. A big part of the R&D task will be to implement a new plan called Oasis, for open-architecture systems-integration strategy. Essentially a commitment to the Open Systems Interconnection standards that are evolving most rapidly in Europe, Oasis will be crucial to Apple's ability to tie its personal computers and local-network products into larger networks linking mainframes, minicomputers, and server hardware. Apple's move away from a proprietary approach towards open-system standards will be aided, says Michael Spindler, president of Apple Computer International, by technology alliances and original-equipment-manufacturers agreements with European manufacturers, as well as joint work with other European R&D facilities, including those at universities. □

MOBILE PHONE SYSTEM RESPONDS TO SPOKEN COMMANDS

Philips Kommunikations Industrie AG has demonstrated a hands-free car telephone system with voice-recognition capabilities. When a driver speaks into a small directional microphone on the dash, the unit dials the wanted party, or looks up in its memory the number of the intended party and then dials. The prototype system understands phrases like "I would like [such and such a number]," "dial," and "correction," which corrects wrong numbers. The Nuremberg-based communications-equipment subsidiary of the Dutch company Philips says its system will not only make using car telephones more comfortable, but also less dangerous: a driver can keep both hands on the wheel and his eyes on the road at all times. □

WEST GERMAN TELECOM-DEREGULATION LAW GOES TO DEBATE

The West German parliament will start debating in April a bill that would deregulate the country's terminal-equipment markets and communication services such as telex, telefax, data transmission, videophones, and mobile and satellite communications. The law, drafted earlier this month by the Bundespost—the state-run communications authority—could be enacted in about a year, if the parliament approves. The draft law leaves untouched the Bundespost's monopoly over the core telephone service itself, but it would finally open many parts of the big German communications market to foreign suppliers. As a demonstration of the fact that it's serious about market liberalization, the Bundespost has started seminars in the U. S., where potential telecom suppliers can learn how to do business in West Germany. □

INTERNATIONAL NEWSLETTER

EXPERIMENTAL JAPANESE NEUROCOMPUTER HAS ASSOCIATIVE IMAGE MEMORY

A Japanese government-sponsored research project is developing an experimental optical neurocomputer said to be the first to use learning to improve its ability to recognize images. The optical associatron, as it is called, is still in an early stage of development at the Ministry of International Trade and Industry's Industrial Products Research Institute, Tsukuba, which is working with Hamamatsu Photonics K.K., Hamamatsu. The system uses optical analog calculation to implement an associative image memory, a type of content-addressable memory. One key part of the system is a microchannel spatial light modulator. This device, developed by Hamamatsu Photonics, transforms an incoherent-light input image striking a photo cathode into a charge image on a lithium-niobate plate. The charge image can be read out by a helium-neon laser as a coherent image using the Pockels effect (changes in a crystal's refractive properties that are proportional to the strength of an applied electric field). Feedback that corrects the charge distribution on the lithium-niobate plate constitutes a form of learning. Researchers expect to increase memory capacity by improving the resolution of the microchannel spatial light modulator. □

SIEMENS STRENGTHENS ITS POSITION IN UNIX-SYSTEM MARKET

Reaffirming its commitment to Unix, Siemens AG is introducing five new computer models that run the company's version—Sinix—of the AT&T Co. operating system. Two high-end models, the multiprocessor MX500-70 and MX500-80, accommodate as many as 64 terminals operating simultaneously, twice the capacity of the earlier MX500. The midrange models, MX300-10 and MX300-20, cover applications needing up to 12 terminals. The single-user X20 system has been upgraded from its forerunner with a more powerful processor. All five Sinix systems use 32000-series 32-bit microprocessors from National Semiconductor Corp. and can communicate with mainframes from Siemens and IBM Corp. With about 20,000 Sinix systems sold, Siemens is Europe's number one supplier of multiuser Unix machines. □

NATIONAL'S LOGIC CHIPS WILL BE PACKAGED THE JAPANESE WAY

High-speed bipolar and CMOS logic chips that National Semiconductor Corp., Santa Clara, Calif., added to its line by acquiring Fairchild Semiconductor Corp. last year will be assembled into packages in Japan by Mitsubishi Electric Corp., Tokyo. The small-outline surface-mount packages are of a type approved as a standard by Japan's Electronic Industries Association, because Japanese equipment makers prefer them. In the U. S., such packages are not used; they are not a Jedec standard. After assembly, Mitsubishi will ship the packaged devices to a National facility in Nagasaki for sale in Japan. □

MORE GERMAN FIRMS ENTER U. S. MARKET DESPITE A HIGHER-PRICED DEUTSCHEMARK

Convinced that their products can overcome the currency problems that beset many European companies [*Electronics,* Jan. 7, 1988, p. 51], two West German firms are set to enter the U. S. market. Harting Elektronik GmbH, based in Espelkamp, is betting that its high-reliability connectors and solenoids will find a friendly reception in the U. S. The devices, manufactured at German and Swiss facilities, will be sold through Harting Electronics Inc. in Chicago and a network of distributors. Another company testing the waters is Spea Software AG [*Electronics,* Nov. 12, 1987, p. 90]. Via a U. S. subsidiary, Spea will soon launch an offensive on the original-equipment-manufacturer market with computer boards based on the Clipper processor from Intergraph Corp.'s Advanced Processor Division in Palo Alto, Calif. □

INTERNATIONAL WEEK

SANYO WILL BUILD MAGNETRONS IN UK . . .

By August, microwave ovens and the magnetron engines that drive them will be manufactured in the UK by Sanyo Electric Co. Ltd., the first time a Japanese company has made magnetrons outside Japan. The move was prompted by growing European demand for microwave ovens—and fear of future tariffs. The European Communities already penalizes some electronic products, although not yet microwave ovens, that have less than 40% European-made components. The plant in Newton Aycliffe, Durham, should boost European components in its ovens to 60%. The new firm expects to build up to 600,000 magnetrons and 200,000 ovens a year.

. . . AS SHARP BOOSTS ITS OUTPUT OF OVENS

Meanwhile, Sharp Corp., Osaka, has decided to increase its capacity to manufacture microwave ovens next year at its subsidiary, Sharp Manufacturing Company of UK Ltd., Wrexham, North Wales, to 350,000 units a year, up from the present 200,000 units. Other Japanese microwave-oven makers such as Brother Industries Ltd., Hitachi, Matsushita, and Toshiba are expected to follow the lead of Sanyo and Sharp.

EUROPE NAMES RADAR SATELLITE R&D TEAM

Designing an advanced satellite-borne mapping radar for the next century is the task of four companies recently selected by the European Space Agency. France's Thomson-CSF, the Munich-based group MBB, the Canadian company CAL, and the Danish firm RS Consult will define the operational characteristics and architecture of the radar for the European Earth Observation Satellite that will be operational in 1995-2000. The radar will rely on an electronic-scanning antenna and offer several modes of operation to fulfill advanced mapping roles. One mode will deliver a high-resolution image—10 to 30 m—of a designated area of the earth.

PHILIPS, CHINA INK FIBER-OPTIC PACT

The Chinese government and Philips of the Netherlands have agreed to set up a joint venture to manufacture optical fibers and cables for telecommunications. The venture, Yangtze Optical Fiber and Cable Co. Ltd., Hubei Province, will use Philips technology and equipment to eventually turn out some 50,000 km of fiber a year. Annual production of cables using these fibers will total 4,500 km. Production will start in early 1990.

SAUDIS TO START UP SOLAR-MODULE PLANT

Saudi Arabia is set to produce solar modules for powering communications gear at remote sites and for irrigation equipment in desert areas. The Al Jazirah Solar Energy Factory Ltd. facility in Riyadh—established with the help of West Germany's AEG AG—will initially produce modules totaling a 500-kW output. Capacity will later be raised for an output of 1.5 megawatts.

GOULD, INDIAN FIRM TEAM UP ON SCOPES

Gould Electronics Ltd. has set up a joint venture with Larsen & Toubro Ltd., one of India's largest engineering groups, to manufacture electronic test equipment in India. Oscilloscopes will be the first products out of the Mysore Province plant but the range will be extended to include recorders and logic analyzers in Gould's line. Initially, products will be assembled from kits made in Gould's Hainault, Essex, UK, facility but local content will eventually reach 90%. The 25,000-ft² plant will be ready in June, the company says.

W. GERMANY SETS UP AI RESEARCH CENTER

Nine West German electronics companies, two research institutes, and two universities will set up and cooperate in a research center for artificial intelligence in data processing. The government-supported facility—the amount of support has not yet been fixed—will be located in Kaiserslautern and will take up its work this summer and eventually employ about 100 scientists. Among the firms participating in the project are AEG AG, Nixdorf Computer AG, Siemens AG, and the German affiliate of Philips. The center will emphasize basic research in AI and its applications.

EUROPE TO GIVE CARS NAVIGATION SYSTEM

An integrated automobile navigation, communication, and diagnostic system that promises to help drivers find the best route, drive safer, and improve a car's performance is in the works. Europe's Carminat research group consists of French car maker Renault, Philips, both in the Netherlands and France, and two other French firms, Sagem and Telediffusion Francaise. The first two phases of the project, which is being funded by the companies and the French and Dutch governments, will take four years to complete.

UK COMPANY WINS AWACS CONTRACT

One of the first Awacs offset contracts to be awarded to a small British firm has gone to Pascall Electronics Ltd. of Sunbury-on-Thames. Pascall will supply logarithmic amplifiers worth $1.3 million to Westinghouse Electric Corp. for use in the new Mode 'S' beacon sensor that Westinghouse is making for the Federal Aviation Administration. The order qualifies for full credit against the Boeing Aircraft offset obligation to the British government under the E-3 Awacs program.

BOOK-TO-BILL RATIO RISES AGAIN IN UK

Semiconductor book-to-bill ratios in the UK are steadily improving over the first few months of 1988, according to the Electronic Components Industry Federation (ECIF). But expansion is restricted to certain types of integrated circuits for data processing. Book-to-bill for February 1988 was 1.17. Figures for January 1988 and December 1987 were 1.08 and 1.04, respectively.

CO-OP EFFORT TARGETS HDTV

Europe's two leading companies in television-studio equipment, BTS Broadcast Television Systems GmbH (a joint venture of West Germany's Robert Bosch GmbH and Philips of the Netherlands) and France's Thomson Video Equipment SA, will work together in developing leading-edge TV technologies. The aim of the venture is to bolster the two companies' position in digital and high-definition TV systems for TV studios and film producers.

ISDN DEBUT IS SET IN 3 JAPANESE CITIES

Integrated services digital network will start in three major Japanese cities—Tokyo, Osaka, and Nagoya—as early as April. On March 17, Nippon Telegraph and Telephone Corp. applied for approval of tariffs for basic services at 64 Kbit/s. Services include telephone communications, high-speed data transmission, high-speed facsimile, and video communications in several combinations.

INTERNATIONAL PRODUCTS

FUJITSU'S PHASE-LOCK-LOOP CHIP CAN DELIVER UP TO A 30% POWER SAVINGS

The single-chip biCMOS solution is said to be first with an on-chip prescaler

Designers of cellular-radio telephones, mobile radios, cordless telephones, and other battery-operated consumer communications equipment that demand low-power operation can get at least a 30% power saving over the competition with a group of phase-locked-loop products from Fujitsu Ltd.

For customers who want a single-chip solution, Fujitsu is offering two biCMOS chips—each for a different market—that save 30% and go one up on the competition by being the first combined prescaler/PLL chips on the market, says the Tokyo-based firm.

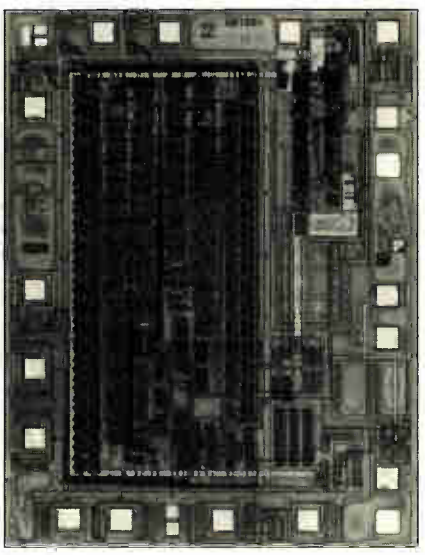
In addition, for designers willing to trade the costs associated with multiple-chip solutions for even lower power dissipation, Fujitsu has unveiled a two-chip, CMOS-emitter-coupled logic set. The two-chip set provides an 88% saving over the competition.

MIXED PROCESS. Even though the mixed bipolar/CMOS is more complex than a single process, Fujitsu engineers implemented the single-chip solutions in biCMOS to retain the advantages of earlier chip sets fabricated as a bipolar prescaler and CMOS PLL. Part of the design process involved changing many high-speed gates from ECL to current-mode logic in order to develop circuits that work down to 2.7 V. By reducing voltage requirements, they are delivering 45-mW performance for the MB1501 and 30-mW performance for the MB1504. Many gates remain ECL, however, and circuits are designed with sufficient margin for operation at power supply voltages up to 5.5 V. Even at the low power levels, the prescaler circuit operates in the low gigahertz range. The devices can be operated directly from three dry cells, or from two dry cells with a voltage step-up circuit.

The MB1501 targets applications in cellular telephone and multichannel access equipment. The MB1504 targets cordless telephones.

The MB1501 operates up to 1.1 GHz with a power-supply current of only 15 mA, which means the device consumes just 45 mW from a 3-V power supply. The MB1504 also trades a lower top frequency for a maximum power requirement of only 30 mW. The 520-MHz top frequency, however, is more than adequate for cordless telephones, says the company.

Both devices have the same design, which differs markedly from the biCMOS approach in gate arrays from NEC Corp. and other companies where CMOS and bipolar transistors are intermixed in each gate [*Electronics*, Aug. 6, 1987, p. 82]. In the Fujitsu devices, curent-mode logic and ECL are used in the prescaler because only these bipolar circuits can achieve high-frequency operation required at the low-power-supply voltages available. Low-power CMOS is used exclusively in all other circuits except for the bipolar charge pump, which must handle high currents as it sets the voltage on the voltage-controlled variable frequency oscillator.



Fabricated with 1-μm emitter stripes, the MB1501 boasts 7-GHz cutoff speeds.

The major difference between the two chips is the current level in the constant-current circuits of the ECL gates. Lower current levels in the MB1504 reduce the cutoff frequency of the transistors in the logic circuits and thus the maximum frequency of operation of this chip. The prescaler in the MB1501 is designed for operation with division ratios of 129 to 128 and for ratios of 65 to 64, while in the MB1504 the ratios are 65 to 64 or 33 to 32. In both chips, the maximum frequency to the CMOS programmable dividers is either somewhat less than 20 MHz for the lower prescaler division ratio pair or somewhat less than 10 MHz for the higher ratio pair.

CML and ECL circuits are fabricated with 1-μm emitter stripes fabricated with diffusion from polysilicon contacts to achieve cutoff frequencies of about 7 GHz. CMOS circuits are fabricated with much looser 1.8-μm design rules because of the relatively low maximum frequency. A standard n-and-p-well configuration is used. Where possible, process steps are combined—the n+ bipolar collector-contact diffusion and CMOS n+ source-drain diffusion are done in the same process. Fujitsu will not reveal other common processes or disclose the number of masks because this information is proprietary.

PACKAGING. The devices are fabricated on a 2.77-by-3.62 mm chip and packaged in either a dual in-line or a small outline package with 16 pins.

Samples of the single-chip MB1501 and MB1504 are available immediately priced at 1,450 yen for the MB1501 and 1,400 yen for the MB1504. Production devices in lots of 10,000 per month are expected this autumn.

The chips were designed by Fujitsu VLSI Ltd., a design center organized as a wholly owned subsidiary of Fujitsu Ltd. Fujitsu VLSI is located in Kasugai, a city near Nagoya. Fabrication is by Fujitsu Ltd. in Kawasaki.

For applications that require even lower energy consumption, Fujitsu has unveiled the CMOS MB87076 PLL and the bipolar MB509 prescaler for use in pagers, cordless phones, and the like. These chips achieve their low power consumption with a special power saving function that means they are in active mode typically only 10% of the time while spending the remaining time in the power-down mode.

In systems using the MB87076 and MB509, the microcontroller chip that controls the pager or cordless telephone controls must also be called upon to control the on/off duty ratio. Two chips are

needed because Fujitsu engineers have not yet implemented the power savings in a mixed-process biCMOS chip. The company, however, expects to develop such a device soon.

The prescaler draws 11.6 mA when operating, 180 μA during standby. The PLL draws 3 mA when operating, 100 μA during standby.

The prescaler is implemented on a 1.6-by-1.1-mm chip and sealed in an 8-pin DIP or SOP. The PLL is implemented on a 2.34-by-4.16 mm chip and sealed in a 16-pin DIP or SOP.

Both the MB509 and the MB87076 are in production now. Sample price of the MB509 is 900 yen, while the MB87076 costs 800 yen. – *Charles L. Cohen*

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Phone 81-3-216-3211 [Circle 500]

POWER-SUPPLY IC MONITORS 5 VOLTAGES

Single-chip monitoring of up to five voltages in switched-mode power supplies can be achieved with Siemens AG's TDA 4917G. The device can also be set externally to monitor any voltage up to 2.5 V, compared with most competing devices which can only monitor preset voltages.

With 12 comparators on-chip, the TDA 4917G uses five pairs to detect rise or fall in the five voltages being monitored. One of the additional two comparators can be configured to work with a microprocessor to signal a backup battery to turn on when voltages are out of tolerance.

The remaining comparator may be used to signal the power supply so it can take self-correcting actions. The TDA 4917G is available now. Price depends on importing country.

Siemens AG, P.O. Box 103, D-8000 Munich 1, West Germany.
Phone 49-89-2340 [Circle 701]

ONLY £360 FOR A STEBUS DEVELOPMENT SYSTEM

British Telecom Microprocessor Systems Ltd.'s STEbox offers designers a ready-to-run STEbus development system for as little as £360.

The computer consists of a processor card, a five-slot backplane, and a 40-W switched-mode power supply packaged in an aluminum enclosure. Two software packages are also included: a debug monitor and a terminal emulator that lets designers use a personal computer to develop an STEbus system.

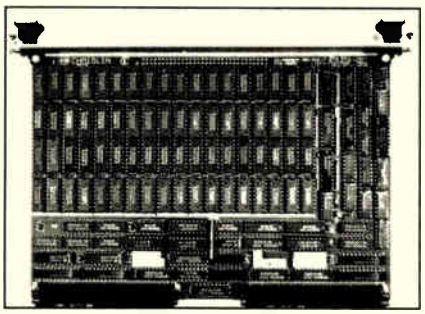
The standard processor board is based on an Intel Corp. 8052 microprocessor, but three additional boards can be obtained—up to the power of a 16-bit Motorola Inc. 68000 microprocessor. That board costs £495. All are available now.

British Telecom Microprocessor Systems Ltd., Martlesham Heath, Ipswich. IP5 7RE, UK.
Phone 44-473-645120 [Circle 702]

VMEBUS MEMORY BOARD PACKS UP TO 16 MBYTES

A memory module from Chrislin Industries Caribe Inc. permits upward expandability of VMEbus systems to 16 Mbytes of dynamic random-access memory on a single card.

Fitting into a single VMEbus backplane slot, the CI-VMEmory card handles word sizes of 8, 16, 24, and 32 bits. Access times are 190 ns for the read cycle and 100 ns for the write cycle.



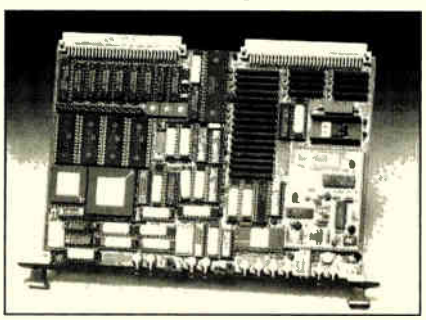
A maximum of 4 gigabytes can be addressed from the board and power requirements are 2.4 A typical and 2.8 A maximum for the fully loaded 16-Mbyte configuration. The CI-VMEmory board is available now. Price depends on importing country.

Chrislin Industries Caribe Inc., P.O. Box 1657, Canovanas, Puerto Rico, 00629.
Phone 1-809-879-5205 [Circle 703]

IMAGING BOARD DOES 15 MEGASAMPLES/S

Eltec Elektronik GmbH's IPC image-processing computer packs a complete image-processing unit capable of digitized data rate of 15 million samples/s on a double-height Eurocard.

The sampling speed produces square pixels that minimize programming effort when specific pixels must be located. The VMEbus-compatible board contains video acquisition circuitry, frame buffer, connections to a control monitor, two serial input/output lines, and a Motorola Inc. 68020 microprocessor.



Four video inputs are multiplexed under microprocessor control to an analog-to-digital converter for digitizing into 8 bits of video data. The video format is programmable.

The IPC board is available from stock at a price of 6,800 DM. Delivery takes about three weeks.

Eltec Elektronik GmbH, Galileo-Galilei-Strasse, D-6500 Mainz 42, West Germany.
Phone 49-6131-50630 [Circle 704]

2400-BAUD MODEM HAS 10-MS SYNCHRONIZATION

The Synchro 24 modem from Mayze Systems Ltd. boasts a 10-ms synchronization time and operates at 1,200- and 2,400-bit/s data-transfer speeds. It also runs in asynchronous mode and handles full-duplex communication on four-wire telephone lines and half-duplex on two-wire lines.

Its fast synchronization speed makes it well-suited for multipoint and point-to-point applications on leased lines. In dial-up operation, it can be used for micro-to-mainframe communication, remote data collection, and other file-transfer applications.

The Synchro 24 is compatible with the CCITT V.26 bis standard for 1,200/2,400-baud operation on four-wire leased lines. It supports the Hayes AT command set and is software configurable. A dozen frequently used configurations can be called up by using buttons on the modem's front panel.

Available now, the modem costs £445 as a standalone unit. It is also available as a card for rack mounting for £395.

Mayze Systems Ltd., Delta 900, Great Western Way, Swindon, Wiltshire SN5 7XQ, UK.
Phone 44-793-511789 [Circle 705]

VMEBUS MODULE HAS 16 OPTO-ISOLATED INPUTS

The VDIN module from PEP Modular Computers GmbH for VMEbus systems features 16 individual and electrically separated opto-isolated channels. Designed to serve as a simple interface in industrial control, the module's opto-isolation offers a high degree of protection against inversion and overvoltages.

The module has a dc input voltage range of up to 24 V. Data polling for easy programming is available. An optional light-emitting diode display for showing the input line status. The single-height Eurocard occupies only one slot in a VMEbus system.

The VDIN module is available from stock at a price of 690 DM in large quantities.

PEP Modular Computers GmbH, P.O. Box 1652, D-8950 Kaufbeuren, West Germany.
Phone 49-8341-81001 [Circle 707]

HDTV TUBE DELIVERS 1,800 PIXELS/LINE

Designed for the High-Definition TV standard, the TH X898 camera tube from Thomson-CFS's Electron Tube Division boasts a limiting resolution of about 1,800 pixels per line and high-end light sensitivity. Sensitivity is 120 μA/lumen for red light and 155 μA/lumen for green light.

A 1-in. Primicon photoconductive layer is used in the tube to achieve color response. The gun also employs advanced electrostatic deflection/magnetic focus design and has a dispenser type cathode for long life.

The tube is available now. Price depends on importing country.

Thomson Electron Tube Div., 29, rue Vauthier, BP 305, 92102 Boulogne-Billancourt Cedex, France.
Phone 33-1-46048175 [Circle 706]

10 MBIT/S CARD LINKS FACTORY PCs IN FACTORY

Blue Chip Technology Ltd.'s SIO-2 communications interface card lets IBM Corp. Personal Computer XTs and ATs communicate with other PCs and instruments on the factory floor without the distance and noise limitations associated with normal IEEE RS-232C serial communications.

Data transfer takes place at speeds up to 10 Mbits/s and at distances up to 1 km—compared with 50 m for an RS-232C connection.

The card plugs into a PC's backplane and offers two serial channels: an RS-232C port and another selectable to RS-422 or RS-485, which is identical to RS-422 except that several devices can share a common cable in a multidrop configuration.

Using the additional ports, which are normally associated with instrument buses, means the PC can communicate with data loggers, dedicated controllers, and other instruments.

The card costs £175 and is available now.

Blue Chip Technology Ltd., Main Avenue, Hawarden Industrial Park, Deesdie, Clwyd CH5 3PP, UK.
Phone 44-244-520222 [Circle 708]

UNIT COMBINES SIGNAL GENERATOR AND TESTER

The DST-1 tester from Wandel & Goltermann GmbH includes a signaling generator, distortion meter, and contact tester in one package.

The hand-held, battery-operated unit's generator targets pulse-code-modulation systems, delivering dialing pulses between 20 and 80 ms duration for controlling the device under test. The distortion

meter determines the deviation of the received signal from the transmitted signal.

The display indicates the distortion measured, the display being ±9 ms or ±2.25 ms. At the same time as the measurement is made, the contact resistance of the system is checked and contact bounce is monitored.

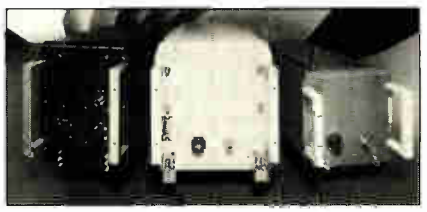
The DST-1 is available from stock. Price will be given on request.

Wandel & Goltermann GmbH, P.O. Box 1262, D-7412 Eningen, West Germany.
Phone 49-7121-1570 [Circle 709]

ANTENNA TUNERS OFFER FAST AUTOMATIC TUNING

Rohde & Schwarz GmbH's tuning units for its HF 850 radio equipment family offer fast automatic tuning, typically within a second, thanks to a digital-control technology.

The compact model FK 852 C1 is for general-purpose use; the naval-version FK 852 C3 and the fast FK 852 H2 are for frequency hopping. They match any



electrically short antenna—whip, rod, longwire, or broadband antennas, for example—to the transmitter output stage. Output power ranges up to 150 W in the 1.5 to 30 MHz range. The tuners conform to military standards.

Other features common to all models include low probability of intercept—thanks to silent tuning within less than 20 ms in 100 preset channels; continuous monitoring of operational status; and continuous 24-hour operation.

The tuners are available from stock. Prices are quoted upon request.

Rohde & Schwarz GmbH, Muhldorfstr. 15, D-8000 Munich 80, West Germany.
Phone 49-89-41292625 [Circle 711]

DIP SWITCHES HANDLE SURFACE-MOUNT HEAT

The NM series of DIP switches from P. Caro & Associates Ltd. comes in a body molded of polybuthylene terephthalate resin and coated with epoxy to achieve tight sealing and soldering resistance up to 200°C—high enough for use in many surface-mount applications.

The switches come in several versions with 4, 6, 8, or 10 switches in each package. Terminals and contacts of gold plate on nickel deliver high performance and an expected life of 2,000 switching operations.

Body sizes range from 3.5 by 11.4 mm for the four-switch version to 3.5 by 26.2 mm for the 10-circuit version. All are rated at 100 mA at 5 V and 25 mA at 25 V dc.

The switches are available now. Price depends on importing country.

P. Caro & Associates Ltd., 2347 Coventry Rd., Sheldon, Birmingham, B26 3LS, UK.
Phone 44-21-742-1328 [Circle 710]

RECORDER'S SETTINGS GO FROM 50 NS TO 600 S

The Analog Data Acquisition Memory (ADAM) transient digital waveform recorder from Réné Maurer AG boasts sample speed settings from 50 ns up to 600 s by combining high-speed analog-to-digital converters with large random-

access memory buffers.

Since the unit contains a resident menu-driven signal and acquisition analysis software package, complex testing can be performed without writing additional software.

The system recorder can test on up to 12 channels with a sampling resolution of 12 bits at 10 MHz. Each channel has a 64-Kbit data-storage memory. Options include RS-232C and RS-488 communications channels and an MS-DOS controller for sophisticated data analysis.

For more complex analysis, the ADAM sytem offers as an option the EVA evaluation monitor. EVA allows the use of standard software and features programmable analog differential amplifiers from 100 mV to 100 V.

Available now, the recorder's price varies with importing country.

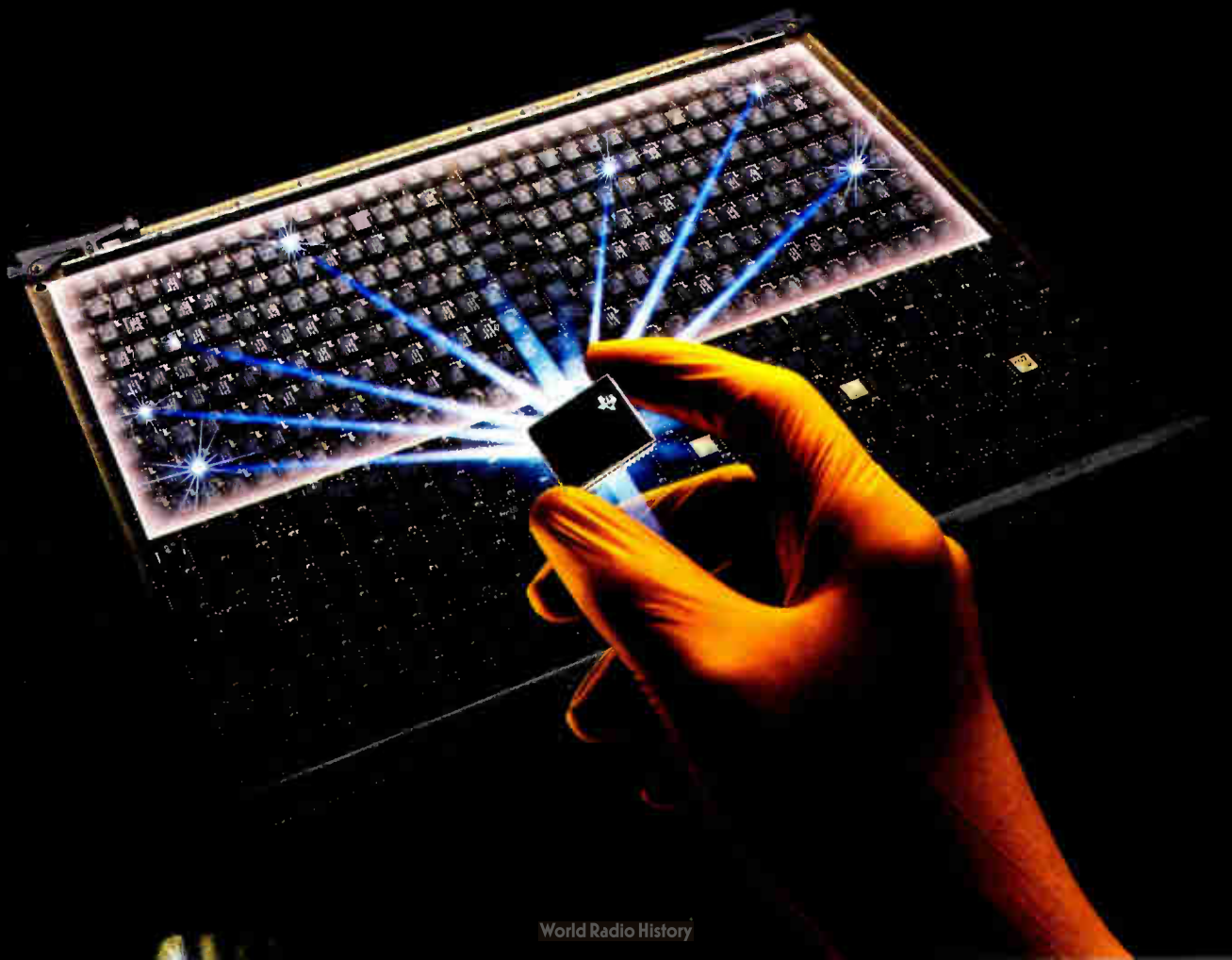
Réné Maurer AG, Electronic Instruments Div., Rotzberstr. 7, CH-6362 Stansstad, Switzerland.
Phone 41-61-48-64 [Circle 712]

TEXAS INSTRUMENTS REPORTS ON

MEMORY MANAGEMENT

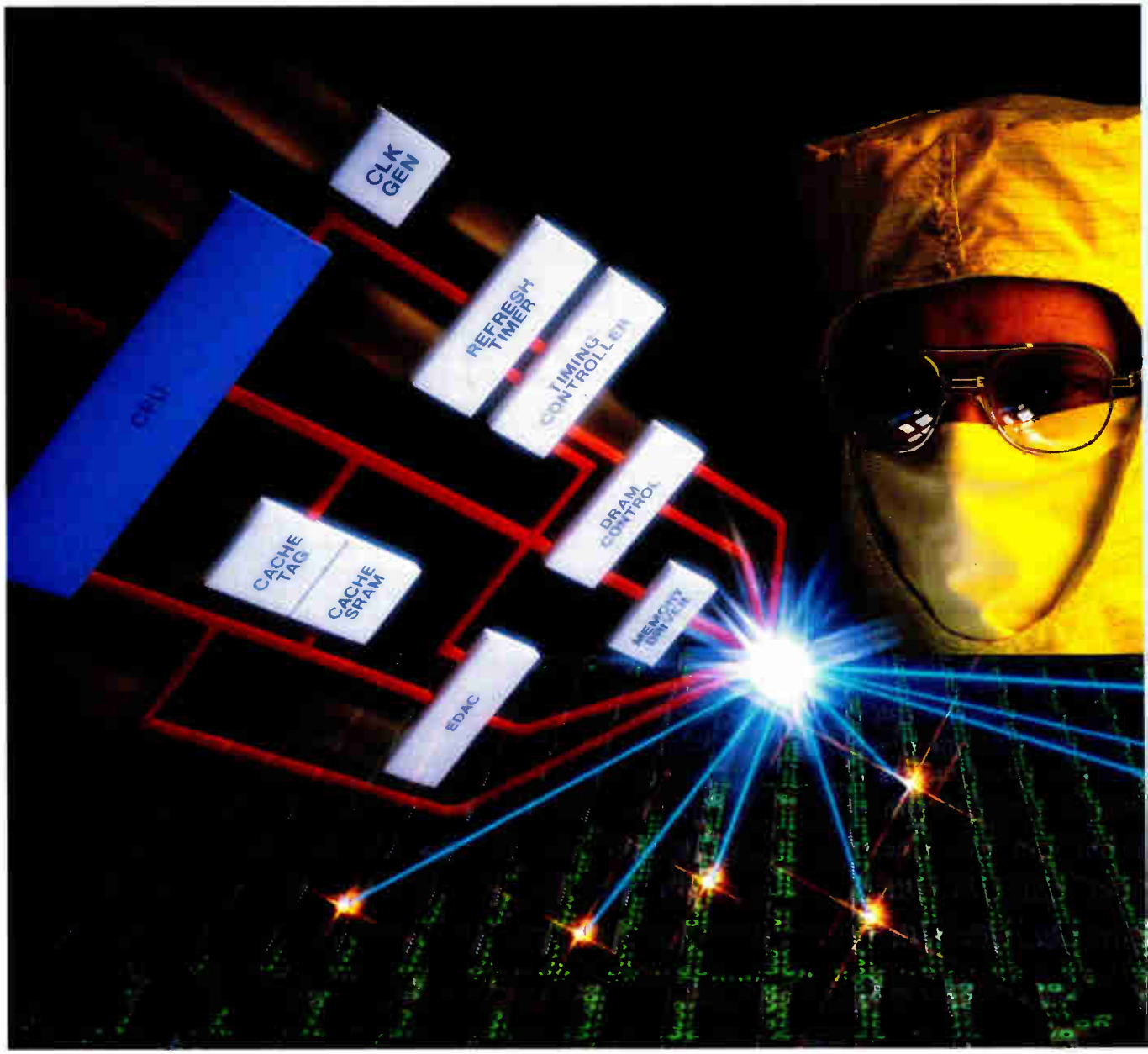
IN THE ERA OF

MegaChip TECHNOLOGIES



Memory management in the Era of MegaChip Technologies:

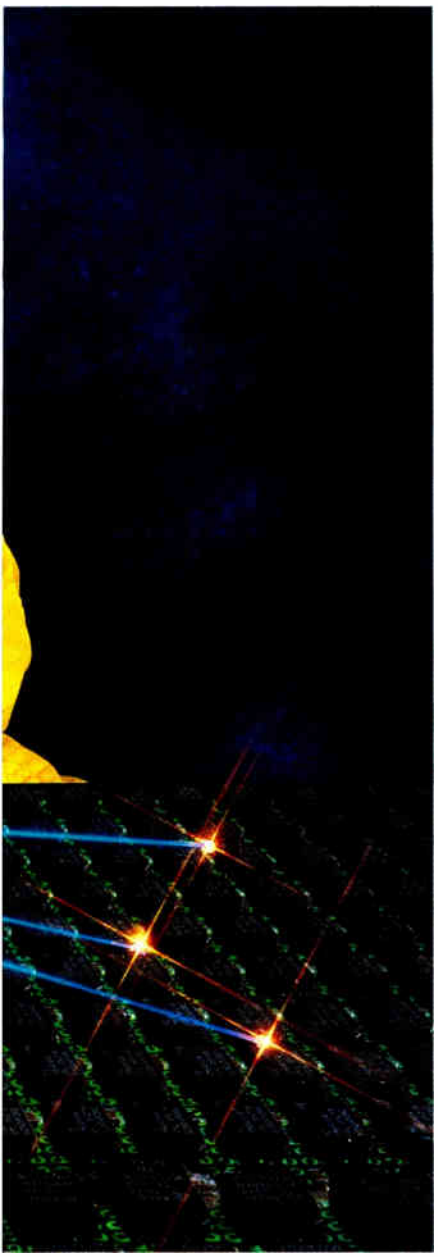
Memory-management ICs from you bring memory arrays up to



Memory systems are a prime area for significant improvements in overall system throughput. Read how TI's memory-management ICs can get you in and out of memory faster no matter which processor you choose.

You can now solve a problem whose solution has eluded design engineers for years: How to catch memory speeds up to CPU speeds. The solution lies with TI's advanced memory-management circuits, and you can use them with whichever processor best suits your application.

Texas Instruments can help processor speeds.



A universal architecture enables these TI devices to work with — and enhance — virtually any high-speed microprocessor or bus structure, even custom engines.

In addition, your component count is cut because these are single-chip VLSI circuits. Your design time and effort are shorter and easier because of TI's comprehensive Memory Management Design Kit *(see page 4)*.

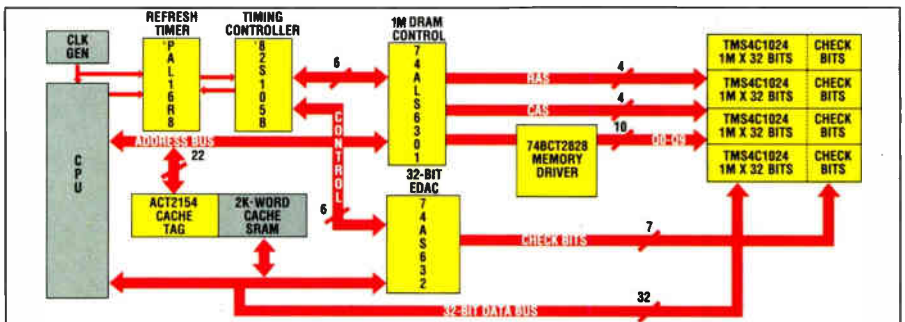
TI addresses your major memory-design concerns

To immediately improve memory-access time, use both main and cache memories, as shown in the block diagram. This approach can produce up to a 3X increase in system performance.

Frequently accessed data and instructions are stored in a few high-speed static random-access memories and "tagged" by a TI industry-standard cache controller (SN74ACT2151/4). These 2K×8 CMOS controllers are the fastest available and can support deep cache architectures of 16K or even 32K.

TI's MegaChip Technologies

Our emphasis on volume manufacturing of high-density circuits is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip™ Technologies. They are the means by which we can help you and your company get to market faster with better, more competitive products.



High-speed memories can be designed with less effort and implemented more cost-effectively by using TI's family of universal memory-management ICs. These devices, all of which are contained in TI's Memory Management Design Kit, will work with and enhance almost any high-speed processor.

This scheme is cost-effective because slower, less expensive dynamic random-access memories (DRAMs) can be used for main memory.

When you must assure system integrity, use of an error-detection-and-correction (EDAC) circuit can improve system reliability 500-fold. Since this approach is necessary with memory arrays larger than half a million bits, TI offers its leadership 32-bit EDAC.

The SN74AS632 detects dual-bit errors and detects and corrects single-bit errors while avoiding processor wait states. And at 25 ns for error detection, it meets your high-performance needs.

Interfacing between processor and main memory gets tougher as speeds increase. But TI has the SN74ALS6301 DRAM timing controller. It can handle any DRAM up to 1 Mbit and incorporates only the essential functions on chip to improve flexibility and speed and to allow for custom timing routines. This controller supports nibble- and page-mode access and scrubbing-mode refresh to increase memory output.

Soon to come: An ASIC (application-specific integrated circuit) solution.

Reducing over/undershoot is accomplished by TI's 2000 Series buffers and drivers — 25-ohm series-damping resistors on the output prevent false reads at DRAM input. For example, the SN74BCT2828 driver can reduce undershoot by 40% compared to traditional approaches. TI's 2000 Series has a high-drive current suitable for VME and MULTIBUS® II bus structures.

You can use any or all of TI's memory-management ICs to obtain the superior performance that marks a market winner. And there's no design rule that says your memory-management chips and your CPU have to come from the same supplier.

▶ *Turn page for more information.*

The tools you need to design a high-performance memory-management system are between these covers:

At $149, the value of TI's Design Kit far outweighs its cost. In one compact file, we've included just about everything you'll need to bring your memory array up to speed. Everything, that is, except your imagination in creating your own unique product differentiators. Here's what you get:

- All necessary high-performance ICs, including
  - —SN74ACT2154 2K×8 Cache Address Comparator
  - —SN74AS632 32-bit EDAC
  - —SN74ALS6301 16K to 1 Mbit DRAM Controller
  - —SN74BCT2828 10-bit Buffer/Driver with series-damping resistor
  - —TIBPAL16R8-10 and TIB82S105B High-speed Programmable-logic Devices for user-defined timing control
  - —TMS4464 256K DRAM
- *Memory Management Applications Handbook* containing applications reports and briefs that supply valuable insights into memory-management system design.
- Data sheets on TI circuits designed for efficient memory management.
- Memory-management-product software graphic-symbol libraries and supporting documentation for use with Futurenet™ or Mentor Graphics™ CAE systems.

For more information on TI's Memory Management Design Kit, call 1-800-232-3200, ext. 3203, or contact your nearest TI field sales office or authorized distributor.

SDV063EC800C

Texas Instruments Incorporated
P.O. Box 809066
Dallas, Texas 75380-9066

YES, please send me more details on TI's universal memory-management ICs.

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TITLE

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TEXAS INSTRUMENTS

INSIDE TECHNOLOGY

DIGITAL SIGNAL PROCESSING: CHIPS ARE HERE, BUT SOFTWARE ISN'T

But new solutions are starting to show up—high-level language compilers and other strategies for easier programming, plus specialized emulators—and they hold the key to faster growth for these chips

by Jonah McLeod

Digital signal processor chips are coming on the market fast and furiously, but the software-development tools to support them have been lagging far behind. The dearth of such tools is putting a crimp in the DSP market, keeping it from the triple-digit growth rates experienced by other hot new chip markets, such as general-purpose microprocessors. But now a number of new solutions are appearing, holding great promise for the many semiconductor houses that produce DSPs and for the system designers who use them.

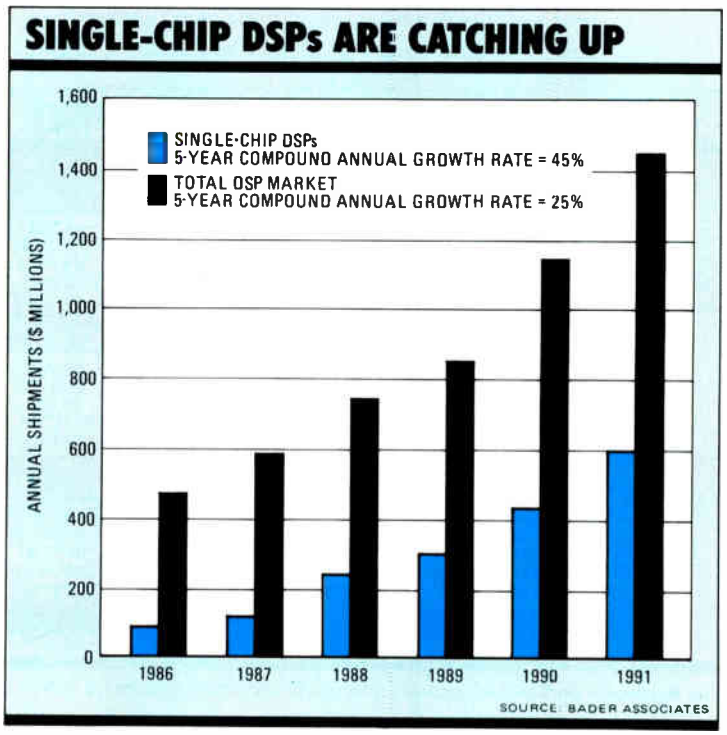
Among the most promising are high-level language compilers and other strategies that offer easier programming, as well as specialized emulators that allow the emulation of multiple DSP chips. Industry watchers have predicted that without the wide availability of such tools, DSP market growth will be held to a fairly modest 45% compound annual growth rate over the next five years. By comparison, the market for 32-bit microprocessors is expected to grow 126% in that time, according to Dataquest Inc. The total DSP market should grow from $470 million in 1988 to almost $1.5 billion by 1991 (see chart), says Bader Associates, a Mountain View, Calif., market research firm.

The slow rate at which DSP development tools have been arriving arises from a basic difference between microprocessor and DSP development. Anyone who can program can write microprocessor applications. But for DSP applications, a programmer must be knowledgeable about signal processing. The challenge lies in cramming a great deal of complex code into the fairly small code space dictated by the real-time applications typical of signal processing.

In recent months, software and hardware tools to simplify the programming of DSP applications have begun to appear. Optimizing high-level C-language compilers, for example, are now available from DSP chip suppliers such as AT&T Technologies, Motorola, Philips, and Texas Instruments. They will speed the development of DSP-chip software, because it is much simpler to program in a high-level language than in machine-level assembly language.

Others are offering alternative techniques that allow programmers to create applications by using waveform templates. Still other chip suppliers are embedding algorithms for common DSP functions, such as filters and fast Fourier transforms, into the DSP chip itself. Finally, more sophisticated emulators that can accommodate multiple DSP chip emulation have also begun to show up.

The real-time nature of most DSP applications makes it tough to create programs for them. With its small instruction set, a DSP chip is like a reduced-instruction-set microprocessor. "Programs that DSP-software developers write are small kernels of instructions repeated over and over," says Philip Roberts, senior DSP product marketing engineer at Honeywell Signal Processing Technologies Inc. of Colorado Springs, Colo. Typical applications include signal recognition and classification in speech recogni-



tion or electronic warfare. "An early application of digital signal processing was filtering and demodulation in a modem," Roberts says. "This application required about 1,000 lines of code," compared with 10,000 or so for early microprocessor programs. But as DSP processing power increased, so did the number and complexity of applications for that power—and the complexity of their code.

But code size could not expand proportionately, because the need to react in real time demands short, tight programs. With faster signal-processing chips such as Motorola Inc.'s 96000 [*Electronics*, March 17, 1988, p. 64], the amount of code can increase somewhat. But there will always be a need to minimize code size, and this creates programming headaches.

Until the introduction of C compilers for DSP applications, the basic minimal development tool set has typically been an assembler containing a linker and a loader. With an assembler, a programmer can write mnemonic instructions in the assembly language rather than binary 1's and 0's. The loader converts the symbolic addresses used in assembly code into binary addresses in the DSP address space, while the linker ties independently developed program segments together into one program.

Besides this software support, a DSP tool kit also contains a hardware in-circuit emulator, which allows the programmer to download his application program to the DSP target system for testing and debugging. Texas Instruments Inc. has become a leader in the single-chip DSP market partly because of its strong development support, in the form of compilers, debuggers, and in-circuit emulators, says Keith Johnson, a DSP systems engineer at NCR Corp.'s microelectronics center in Fort Collins, Colo. "The NEC Corp. 7720 family was actually introduced before TI entered the market," he says, "but it didn't catch on because of perceived lack of support. By contrast, TI has not only provided good development tools, but has also supported its DSP chips by offering newsletters, organizing users' groups, and so on."

TI is committed to continuing this kind of user support. For its latest TMS320C30 DSP chip, the Dallas-based company has just come out with a C compiler, which performs some optimization. "What we're going to be doing is looking at how our customers are using the compilers, and implementing those optimizations that seem particularly well suited to DSP applications," says Ray Simar, the chip's principal architect at TI in Austin. For example, the TI chip has a capability called delayed branch. A feature found on RISC processors, it is useful for optimizing branches and loops. The C compiler can take advantage of this.

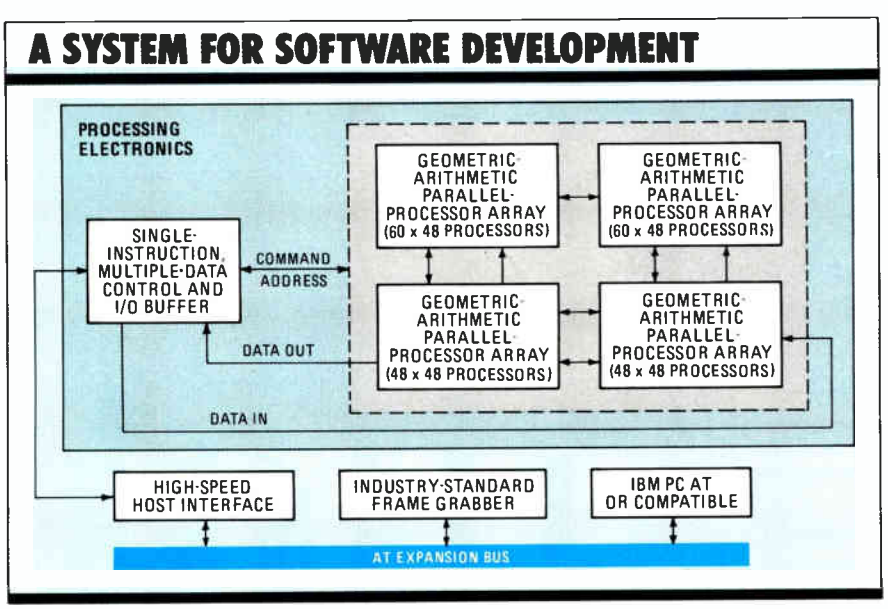
Other companies have gotten the message. "Everybody that's getting into the business these days is supporting their chips adequately," says NCR's Johnson. A high-level language compiler is part of the NCR45SPDS development system recently announced for his company's Geometric-Arithmetic Parallel-Processor chip (see figure, below). The chip's development system allows users to program applications in a C-like language.

Among the other new compiler entries is a C compiler called C-DSP 5010, which its maker, Philips of the Netherlands, calls the world's first optimizing C cross-compiler for DSPs. Designed for use with the Philips 5010 and 5011 DSP chips, the compiler is now being tested and will hit the market in a few months, says Ton van Kampen, who is responsible for strategic marketing for MOS telecom integrated circuits at the Eindhoven-based Electronic Components Division.

The compiler is the result of a cooperative effort between Philips and Tasking Software BV, a Dutch software house. It comes with a library of the most common DSP algorithms such as filters and fast Fourier transforms, and a set of other software tools to provide an environment that allows short development times, fast programs, and dense coding. The DSP software tools, which run on the Digital Equipment Corp. VAX/VMS and personal computers, include assembler, linker, simulator, and program library.

Philips is not alone. AT&T Bell Labs in Holmdel, N.J., has had an optimizing compiler in beta site testing since January for both its DSP32 and the DSP32C devices [*Electronics*, July 23, 1987, p. 69]. It will be released in July. "We're developing an optimizing compiler because it helps programmers program efficiently," says John Hartung, supervisor of the DSP systems development group. "They will never accept a compiler if it produces inefficient code."

Besides performing global register allocation and the other tasks done by most optimizing compilers, the AT&T compiler goes further. "It also performs optimization that is specific to pipelined architectures," Hartung explains. "On a pipelined machine, the compiler's aim is to keep the pipeline busy all the time." For example, in compiling program code, the compiler examines data dependencies to see if the current contents of a pipe-



The hardware part of a PC-based software development system for NCR's GAPP processors includes four geometric-arithmetic parallel-processor arrays, a controller/I/O buffer, and a PC.

line must first be flushed or if it can start using a pipe immediately. The compiler takes advantage of the pipeline by reorganizing instructions.

In an effort to make DSP programming simpler still, DSP Development Corp. has introduced software that allows DSP designers to prototype DSP algorithms on a common spreadsheet. The product is called DADiSP, for Data Analysis and Digital Signal Processing, and works in much the same way as financial modeling. However, instead of an array of cells containing single numbers, the spreadsheet contains up to 64 windows of entire waveforms.

With DADiSP, "software developers don't have to write assembly-language programs on DSP chips to try out new algorithms," says Randy Race, cofounder of the Cambridge, Mass., company. After developing an algorithm on an actual DSP system, a developer can use DADiSP to run test data and compare it with actual chip output to verify that the algorithm works or to isolate bugs in the software or hardware.

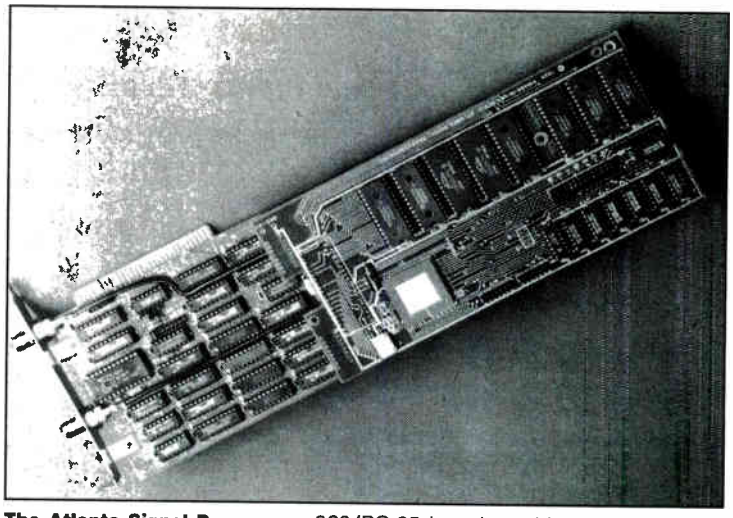
DADiSP can perform 160 different analyses on waveforms, including signal arithmetic, signal calculus, fast Fourier transforms, and other routines. Waveforms can be stored in a data base, overlayed, and manipulated graphically (zoomed, scrolled, compressed, expanded). DSP Development has just added a signal-editing capability and later this spring will be offering a version that lets users design their own DSP filters.

But there is another way to develop algorithms: by writing them in assembly language on a software DSP development system, a personal computer, or a work station, and then debugging them on a prototyping board. Typical of such a product is the 320/PC-25 daughter board for the Digital Signal Processing Workstation made by Atlanta Signal Processors Inc., Atlanta, Ga. (see figure, above right).

The future of DSP depends upon making the technology available to users who are not signal-processing experts. "We have a strategy to simplify DSP programming in the future with Motorola chips," says Bryant Wilder, product marketing manager for DSPs at Motorola in Phoenix, Ariz. "We're working on a C compiler for the [Motorola] 96000," he says [*Electronics*, March 17, 1988, p. 64], "but for the future, we're working on a higher-level DSP type of language." He declines to give details.

Zoran Corp. offers one way to simply the DSP programming problem on its VR34161 and the newer ZR34325 Vector Signal Processor [*Electronics*, Sept. 17, 1987, p. 25]. "The chips come with a library of high-level subroutines in read-only memory on the chip," including Fast Fourier transforms and finite impulse response filters, says Michael Stauffer, director of marketing at the Santa Clara, Calif., company. "Implementing a fast Fourier transform becomes one or two instructions instead of the tens of instructions normally required," he says. In this way, "a DSP program becomes a half dozen calls, which makes the programmer's job almost trivial."

The down side of this approach is that wired-in algorithms make a chip inflexible, says David Fair, strategic marketing manager for Analog Devices



The Atlanta Signal Processors 320/PC-25 board provides a development system for the TI TMS320C25 DSP chip.

Inc.'s DSP Division, Norwood, Mass. "Zoran's chip is good for only six functions," he says. "We're looking for complete, general-purpose programmability." Stauffer concedes that the prewritten algorithms limit where the Zoran chips can be used. Still, developers with requirements that match the on-board library have a quick means of implementing their application with a minimum of software development, he notes.

Once the software has been written, the applications developer is faced with finding the bugs in it when he puts the software and hardware together. The problem is compounded by the fact that most DSP applications contain more than one processor. "Over 80% of DSP designs contain a DSP chip and another microprocessor such as an 8086 or 68000," says William Fleck, product manager at Hewlett-Packard Co.'s Logic Systems Division in Colorado Springs, Colo.

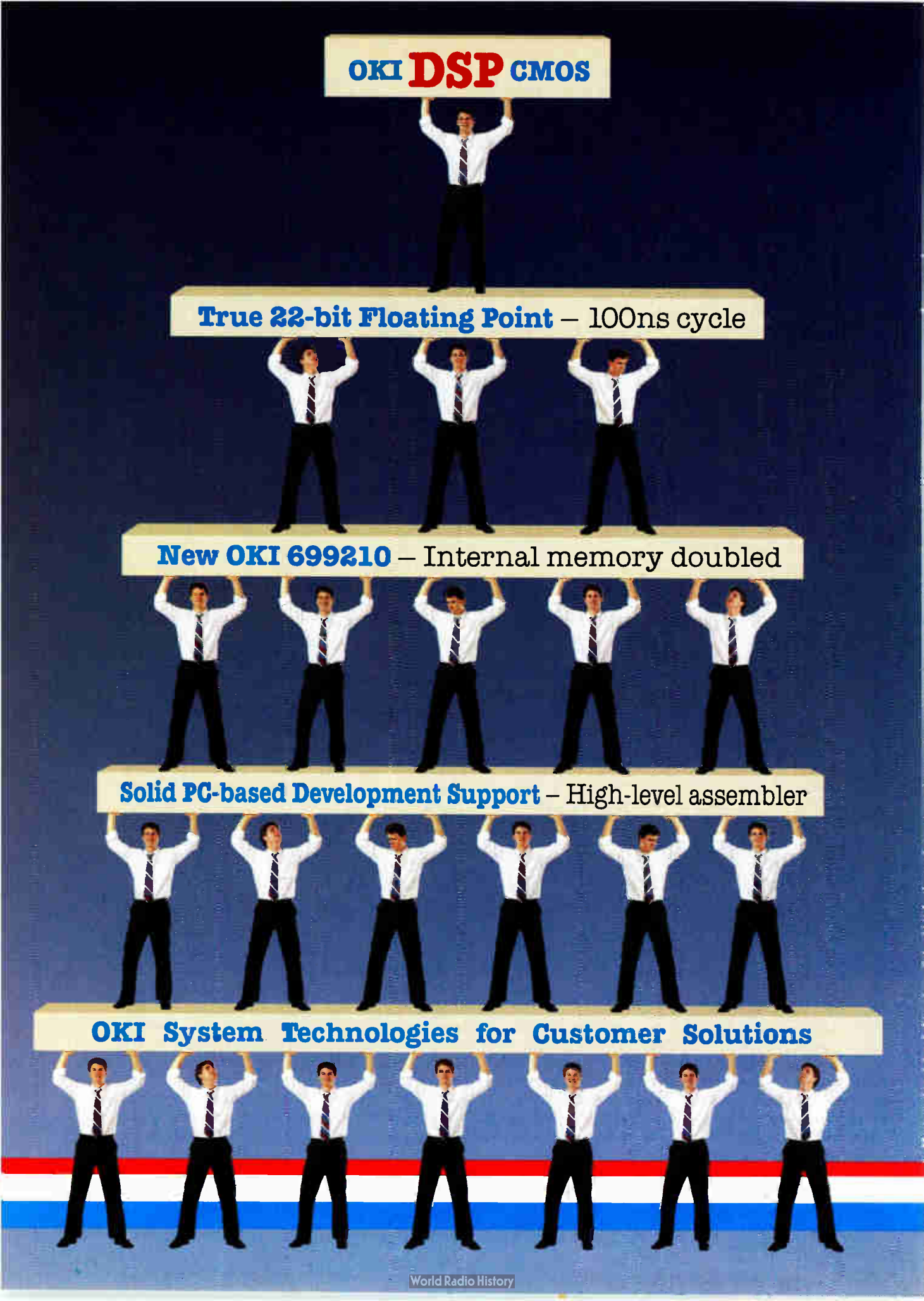
An applications developer who wants to create systems containing processors from a variety of different chip vendors can wire together in-circuit emulators from or buy a turnkey solution from HP. The company is the only supplier of general-purpose development-system software tools and emulators, Fleck claims.

The developer can connect several of the new low-cost HP 64700 in-circuit emulators into a personal computer. From the computer, the user can synchronously start all the emulators, cross-trigger them, and halt them. An integral logic analyzer in each of the emulators helps diagnose logic and timing problems.

The company already offers support for the Z80, 8086, and 68000 families of microprocessors. Starting in April, it will provide support for TI's TMS32020 and TMS320C25. Other DSP chips will follow.

The new and thriving market for DSP chips is finally drawing vendors into the development-system arena. As the market gets larger, it will doubtless entice more suppliers to produce software and hardware tools to further simplify DSP software development.□

Additional reporting by Paul Angiolillo, John Gosch, Wes Iverson, Larry Waller, and Jeremy Young.



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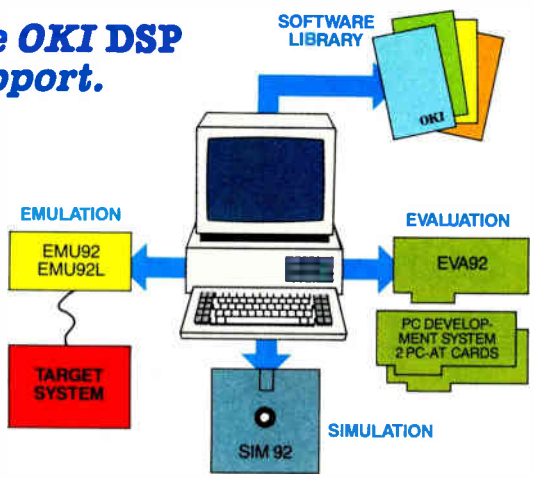

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DSP's BIG CONFERENCE ENTERS THE REAL WORLD OF PRODUCTS

The 1988 conference will draw many chip vendors as multiprocessor DSP systems gather steam

Always an important technical meeting for engineers and researchers in the digital-signal-processing field, the International Conference on Acoustics, Speech, and Signal Processing now is taking on more of a real-world, commercial cast. Exhibits and papers at this year's ICASSP show clearly the impact semiconductor makers are having as their interest grows in DSP and more chips hit the market.

The new commercial bent will not detract from the quality of technical papers describing research done in DSP subdisciplines like image, audio, speech, radar, and underwater signal processing. But more product-related information will be evident at the ICASSP, sponsored by the Institute of Electrical and Electronics Engineers. Hot topics at the New York Hilton on April 11-14 will include commercial DSP chips, peripheral chips, systems built with the new generation of very large-scale integrated circuits, and algorithms and methods applied to those real-world systems.

Papers to be presented reflect important trends. One is the move to multiprocessor DSP systems—finding ways to combine multiple VLSI processing elements to get the kind of power needed for real-time signal processing. Some of the new DSP chips are designed from the start with provisions for combining them in one way or another. Another trend, although not rooted in commercial reality, is the expanding attention being given to signal-processing with neural networks.

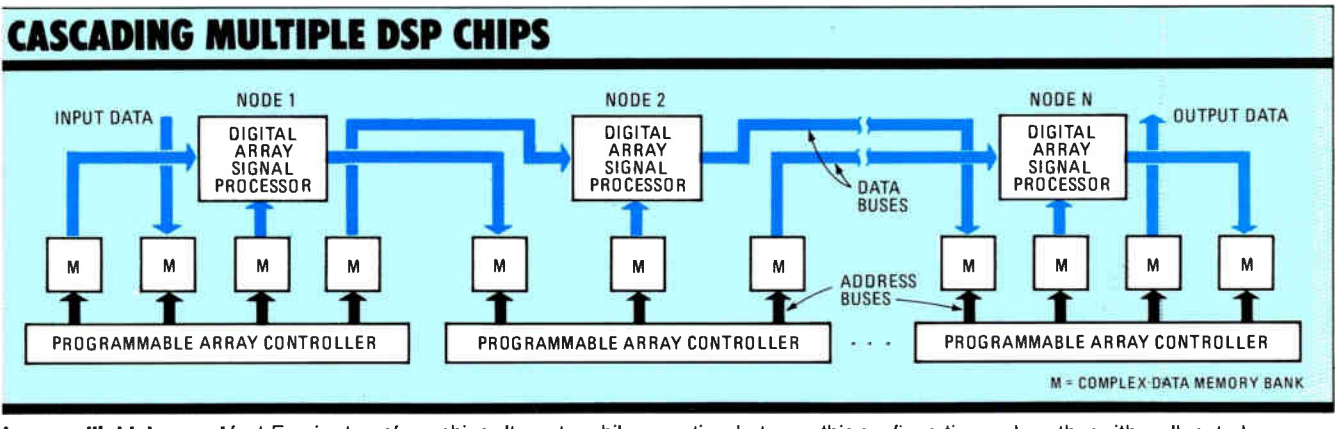
"I can see a marked difference in the conference over four or five years," says Ray Simar of Texas Instruments Inc., Dallas. "It used to be very theoretical and there was very little in the way of vendors showing anything," says Simar, the principal architect of the TMS320C30, the latest addition to the most widely used family of DSP chips. "But now the papers themselves quite often talk about implementation of algorithms on real hardware. More of the silicon houses will be there, a lot more than in the past."

TI will be there, describing how the recently introduced TMS320C30 was designed with the aim of supporting C-language compiled software. Papers from AT&T Co. will discuss how its newest floating-point DSP chip, the DSP32C, was also designed for compiled software. Other companies presenting papers include LSI Logic Corp., Milpitas, Calif., which will describe new members of its image-processing chip family and Zoran Co., Santa Clara, Calif., which will report on its newest 32-bit vector signal processor, a chip with provisions for attaching multiple processing units to a single bus.

Honeywell Inc.'s Colorado Springs, Colo., signal processing technologies operation will describe a pair of DSP chips designed for multiprocessor systems—chips it plans to market later this year (see figure). The HDSP66110 digital array signal processor and HDSP66210 programmable-array controller target extremely high-performance fast-Fourier-transform applications through a cascaded-processor architecture. A single pair of the 1.2-μm CMOS chips performs a 1,000-point FFT in 61 μs, the company says, and a multiple-stage implementation handles data rates of up to 100 MHz.

Zoran and Honeywell are examples of chip vendors on top of the growing trend towards multiprocessor systems. Real-time DSP applications are a big number-crunching challenge, and ICASSP papers reflect the natural progression towards combining many VLSI processing elements to get the performance needed. Multiprocessor DSP "is a trend that started several years ago, but in terms of implementations in VLSI signal processing, it's more pronounced now," says K. Wojtek Przytula, a member of the technical staff at Hughes Research Laboratories in Malibu, Calif., who chairs an ICASSP session on VLSI signal processors.

"The field [of multiprocessor DSP] has been developing very fast," he says. "A few years ago it was at the level of university research, first as algorithmic designs, later designs of architectures, and gradually moving into the VLSI-based designs. Now I see this shifting into the implementation of prototypes either in joint pro-



Honeywell's high-speed fast-Fourier-transform chips alternate, while operating, between this configuration and another with reallocated memory.

grams between universities and industry or just in industrial labs. We have most of the advanced industrial labs here." Przytula adds that papers about multiprocessor DSP systems are coming from all over the world.

One way to combine multiple DSP elements is in systolic arrays, and there is an entire session devoted to this subject. A standout paper in this session describes work at the Massachusetts Institute of Technology's Lincoln Laboratories in Lexington, Mass., on a wafer-scale systolic array for adaptive-nulling-antenna applications. The task is to keep updating an array of values used to cancel out signal interference on multiple antenna elements. "The math for doing that is pretty well known," says Charles Rader, senior staff member. "But if you have a lot of antennas to work with, it can be a computationally ghastly problem.

"We're implementing a systolic array with 32 processors" on a single wafer, he says. The processors are tested and then wired together by a laser-based process developed and proven at Lincoln Labs. "We expect to do the equivalent of about 3 billion operations per second in a package not much bigger than a cigarette package," Rader adds. The array is not working yet, he says, although the theory and architecture are done; the researchers are now checking the layout of the 2-μm CMOS masks. "It's meant as a demonstration of the ability to go way beyond what people have done before. It represents about a factor-of-33 more difficult problem [in terms of the number of antenna elements, which is 64] than anything we've done before."

Another area where research aims to demonstrate a new technology is that of neural networks in signal processing. It is not clear whether neural nets will make it big in this area, but much research is being done to see if neural-net models can be used to solve intractable DSP problems. Such topics, which have received only very isolated attention at ICASSP in previous years, are the subject of seven papers this year, a large portion of the session chaired by Przytula of Hughes Research.

The papers "are not only a general exploration of the approach, but attempts at applying it to specific problem areas," he says. A number of signal processing problems, such as pattern recognition, connected-word speech recognition, direction-finding in radar, and multiple target tracking, have long defied practical real-time processing solutions.

Many of the neural network papers involve simulating a solution to such problems using neural-net models. If the concepts can be proved well enough to get the necessary financial backing, work may then proceed to implementing such networks in silicon. "I think we can anticipate a full session on neural nets next year," says Przytula. *—Jeremy Young*

TECHNOLOGY TO WATCH **DIGITAL SIGNAL PROCESSING**

ARRAY BOARDS GIVE IBM PCs NEAR-MINISUPER SPEED

Communications Automation & Control's low-cost array processors run between 8 and 25 megaflops

A new family of board-level accelerators from Communications Automation & Control gives personal computers near-minisupercomputer levels of floating-point performance at prices starting at $695—a sharp improvement over plug-in array-processor boards that have typically cost from $5,000 to $15,000. Based on AT&T Corp.'s high-speed digital-signal-processor DSP32 chip family, the boards provide personal computers with a cost effective way to tackle computationally-intensive applications in image processing, graphics, scientific computing, and signal processing.

Communications Automation & Control, a Bethlehem, Pa., startup, was founded by former employees of AT&T's DSP group. And the company makes good use of versions of AT&T's DSP32 family, including one that will pack up to 25 million floating-point operations/s peak performance—the power of a complete floating-point chip set—in a single low-cost chip [*Electronics*, July 23, 1987, p. 69]. The family is programmable in either C or assembly language, and Communications Automation & Control's designers use that feature for another breakthrough in floating-point add-in boards. The company offers a set of software development tools that makes it easier for users unfamiliar with DSP programming to write applications for the accelerator.

There is more to the family of boards, however, than just the DSP chip's performance. Typically, the overhead required to access an attached array processor may eat up much of the promised performance boost. But Communications Automation & Control has designed an efficient host interface to get around the problem. Another speed enhancement introduced is an input/output mapping scheme, rather than a memory-map scheme, to assure efficient access to the fast memory on the array processor board. In addition, the board family sports analog interfaces to enhance signal processing applications, as well as digital interfaces.

The first-generation product, known as the DSP32-PC, uses a 250-ns n-MOS version of the DSP32 chip (see figure). The $695 board, which plugs into the IBM PC bus, provides an 8-megaflops peak performance. The standard 32 Kbytes of zero-wait-state static random-access memory can be upped to 128 Kbytes for $50 more. Next-generation products for the IBM PC AT and VMEbus, to be available in the fourth quarter of 1988, will use the 80-ns CMOS DSP32C chip. The boards will provide 25-megaflops peak performance at a cost of less than $1,500, the company says. The PC AT version will come with 64 Kbytes of SRAM but additional on-board sockets allow for expansion to 256 Kbytes.

For applications that require a lot of multiply and accumulate operations, the DSP32-PC will provide as

much as 300 times the speed of PC coprocessors such as the 8087 (66 Kflops at 8 MHz) and 80286 (74 Kflops). In key benchmarks, the DSP32C-based PC_AT version of the board executes a 1,024-point complex fast-Fourier-transform operation in 3.25 ms, a finite-impulse-response filter at 80 ns/tap, and a 3-by-3 multiplication in 2.2 μs.

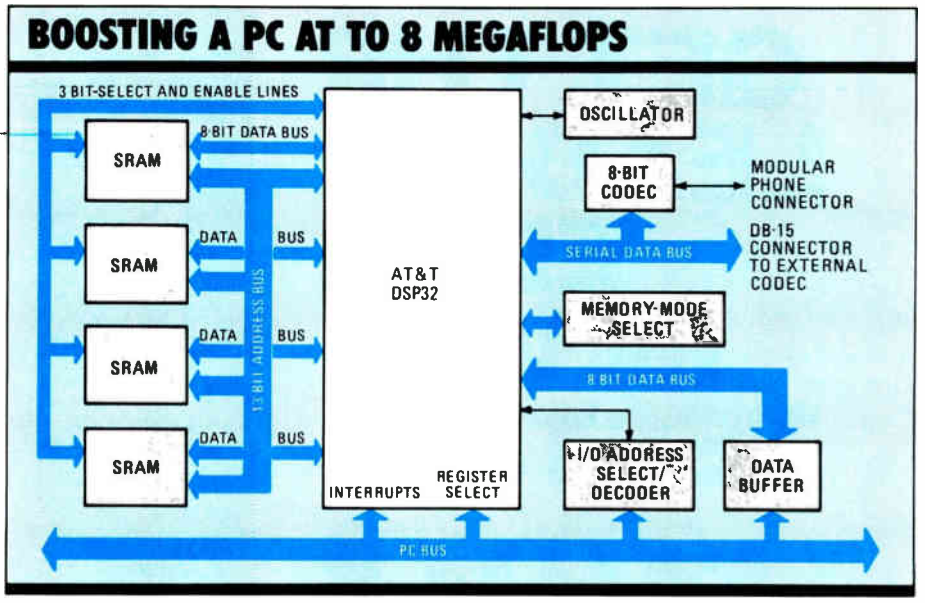
Other product enhancements are also available. A development system, which includes the board, assembler, window-based emulator, math library, and demonstration programs, costs $995. The development package is immediately available. A C compiler with a mathematics library will be available in June for $1,500.

C compiler availability is good news for system developers. Writing applications software for DSP chips has not been easy because users have had to program in microcode using wide words that controlled a number of parallel operations. To ease that burden, Communications Automation & Control is offering a full suite of software development tools, including a user-friendly window-based emulator, and the C compiler. Programmers can use a combination of C and DSP32 assembly language codes, coding the bulk of their programs in C, and the speed-critical routines in assembly language. The assembly routines may be either coded inline or linked with the main C program.

As an additional development aid, Communications Automation & Control provides two function libraries. The C run-time library provides most commonly used functions. And an optimized applications library, written in DSP32 assembly language, provides 57 commonly-used math routines, as well as a number of signal-processing, image-processing, and graphics routines. Examples are real and complex FFTs, FIR filters, Hamming window functions, a graphics routine that converts 16-bit color pixels to 5-bit gray-scale values, and an image-processing routine that performs a histogram equalization algorithm for gray-scale imaging.

Though the performance of the array processor in the DSP chip sets the system's peak performance, it is the overhead associated with invoking the array processor and passing it instructions and data that generally limits the real system throughput. To help minimize host/array processor overhead, the DSP32-PC provides a simple and efficient host interface.

To invoke the DSP32-PC from an application program running on the host, the host passes it the name of the routine and its arguments, and sets a flag by writing to the DSP32-PC's memory. When the DSP32-PC sees that the flag is set, it executes the necessary routine, computes the result, uploads the result to the host, and clears the flag. The routine that the DSP32-PC executes is usually downloaded from the host to the DSP32-PC's local memory prior to program execution. That routine may either be a library routine, or an application written by the user.



Communications Automation & Control's array processor board uses AT&T DSP chips to provide from 8 to 25 megaflops.

To improve the efficiency with which the host and the DSP32-PC board access the on-board memory, the DSP32-PC uses an I/O-mapped interface. In a PC environment, an I/O mapped interface provides two significant advantages over a memory-mapped interface, which was used in earlier array processors to simplify address decoding.

First of all, the use of an I/O-mapped interface relieves overcrowding in the PC's address space. In a memory-mapped architecture, a portion of the PC's address space must be reserved for the array processor. When this architecture was first adapted for the PC environment several years ago, overcrowding was not a problem. Much of the PC's 640-Kbyte address space (limited by MS-DOS), was unused at that time.

Today, however, a number of third-party vendors are beginning to stake out portions of this previously unused address space. For example, the EGA graphics card uses the extended I/O space. Consequently, an array processor that uses that space cannot be used in the same system with an EGA card. In an I/O-mapped architecture, such conflicts do not arise. The I/O memory map lies outside of the PC's 640-Kbyte address space.

The DSP32-PC provides analog interfaces to handle signal-processing applications, in addition to its digital interfaces for scientific computing and processing of computer-generated images. For example, a modular phone-handset connector allows speech to be recorded and stored on a hard disk, analyzed, and played back. An 8-bit codec provides digital-to-analog and analog-to-digital conversion, as well as low pass and bandpass filtering for speech signals. To interface to higher-precision external ADC and DAC boards, or to other DSP32-PC boards, the board provides an 8-Mbit/s double-buffered direct-memory access serial port via a 15-pin female D-type connector. *–Tom Manuel*

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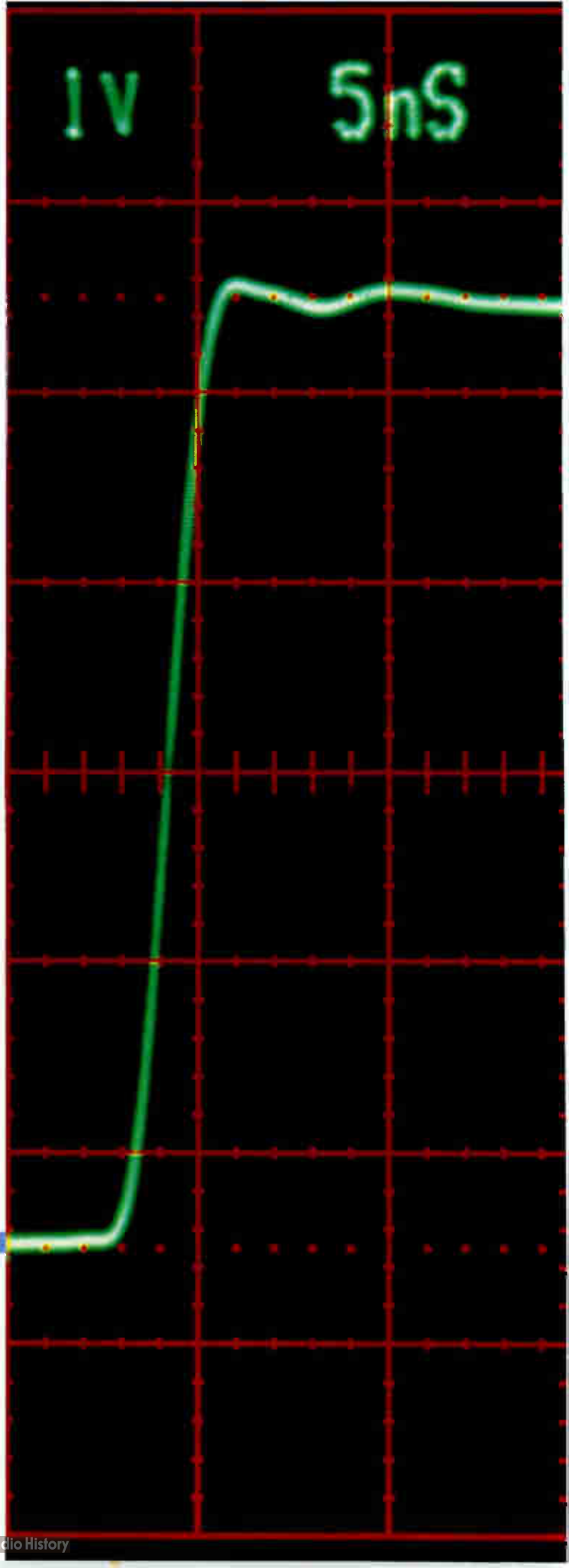

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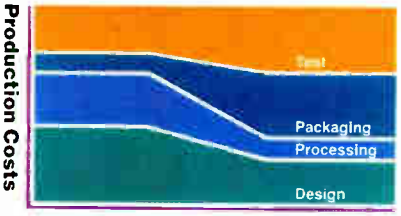

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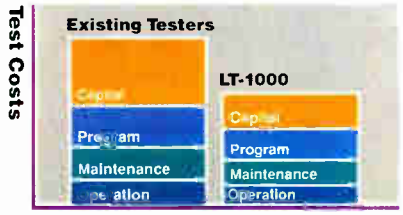

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APTEC LINKS INTEGRATED PROCESSOR TO I/O SYSTEM

Vector/scalar board seeks to replace array processors in 32-bit intensive calculations

Signal and image processing is getting a big boost in applications that rely on high-speed input/output computers to handle 32-bit floating-point calculation-intensive applications. Aptec Computer Systems Inc. is marrying a vector/scalar processor to its I/O computer architecture. The company says integrating vector processing into its fast I/O systems offers performance and cost advantages over the more common approach of attaching external array processors.

The Beaverton, Ore., company is introducing an integrated vector/scalar processor board for the Aptec IOC-24 I/O computer (see fig. 1). The VSP-1 board contains a powerful scalar processor and a vector processor that can do 20 million 32-bit floating-point operations/s. Both processors share 1 Mbyte of 35-ns static random-access memory on an 80-Mbyte/s internal bus. The VSP-1 connects to the IOC-24 through the I/O computer's data interchange bus. Multiple VSPs can be installed in an IOC-24 to provide a peak potential of more than 300 megaflops—up to supercomputer performance level.

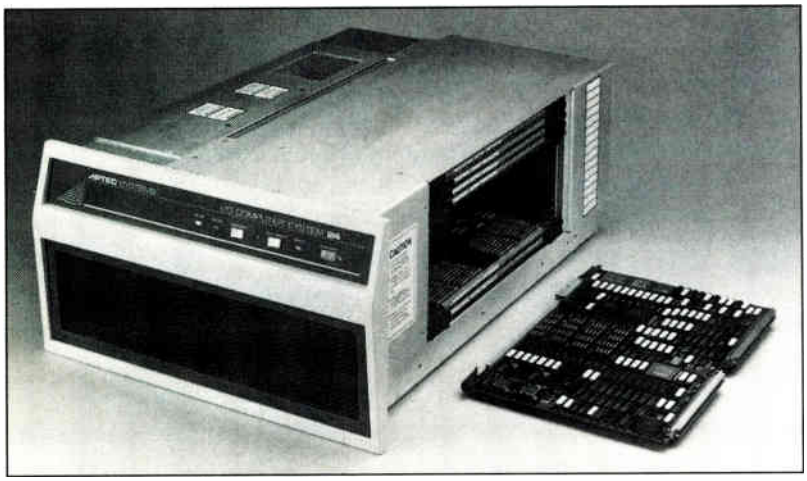
Aptec's I/O computers are popular in signal- and image-processing applications because their architecture can easily handle high volumes of input data. Aptec's strategy is to leverage its architecture by providing built-in special-purpose processors as an alternative to the external accelerators that many of its customers now attach to the system. More special-purpose processors in addition to the VSP-1 may be on the way.

"Over 50% of our current customers are involved in some type of signal processing, so integrating a vector/scalar processor made perfect sense as the first in a family of special processors we are planning for the IOC," says Richard Bowles, Aptec product marketing manager. "Because of our unique I/O architecture, we will be able to integrate other special-purpose processors with our I/O computer when customer demand is significant," Bowles adds. He won't say what the other family members will be.

Aptec says it chose a vector/scalar processor as the first introduction because an integrated processor offered price/performance advantages over attaching array processors to its I/O computers. For signal processing applications, the IOC-24 and VSP-1 combination is the most cost-effective solution available, Aptec says. For example, a fast Fourier transform, the most common algorithm used in signal processing, is performed on an IOC-24 with one VSP-1 installed for a cost of about $2,000 a megaflop. The cost of using attached array processors would be $4,000 to $5,000 a megaflop, the company says. What's more, the integrated VSPs require much less overhead to access and start up than those attached externally. Data can also be transferred between the integrated processors and the I/O computer at a much faster rate—12 Mbytes/s rather than 2 Mbytes/s for an attached processor.

The hardware architecture of the VSP-1 is basically a 32-bit scalar processor, a 32-bit vector processor, and 1 Mbyte of fast SRAM, tied together with a very high-speed internal bus and connected through an interface to the IOC-24 data interchange bus (see fig. 2). Such hardware is of minimal use, however, if customers cannot readily implement applications on it. So Aptec is also providing a complete software development tool kit with the VSP-1. The VSP-1 operates more efficiently by having both the program and data installed in its 1-Mbyte local memory instead of fetching them from the host memory. Aptec's original product philosophy for its I/O computer was to design a special computer to manage the data flow between high-speed peripheral devices and special-purpose processors. It succeeded in that goal and now offers two I/O computer models, the 24-Mbyte/s IOC-24 and the 200-Mbyte/s IOC-200 [*Electronics*, Nov. 13, 1986, p. 54]. But while the VSP-1 has arrived to piggyback on the IOC-24's success, plans are not settled for developing an integrated vector processor for the IOC-200, Aptec's high-end product. "We are taking a wait-and-see attitude with respect to the IOC-200—waiting to see what chips and software will become available to match the performance of the 200," Bowles says.

The VSP-1 complements the IOC-24 by adding high-speed 32-bit computational capability to fast I/O operations. It is well suited to executing a broad range of numerical algorithms in signal and image processing, commonly found in radar, sonar, and surveillance applications. The 20-megaflops 32-bit floating-point performance is targeted to signal- and image-



1. A vector/scalar processor board for digital signal processing and high-speed floating-point applications is designed to fit into the Aptec IOC-24 system.

processing applications that do not require 64-bit precision. Signal- and image-processing applications typically have fixed algorithms that operate on big streams of data.

A single VSP-1 processor is priced at $24,900. A complete IOC-24 system with a VSP, 16 Mbytes of memory, and a complete application development tool kit including an application subroutine library, is priced at $99,500. This system contains 10 empty slots ready for expanding the number of VSPs and the amount of main memory. An expansion cabinet provides 12 more slots. "A realistic maximum number of VSPs in an IOC-24 system is 10 because you have to leave room for memory," Bowles says. Aptec will have the first production VSP-1 processor ready to ship by Sept. 1.

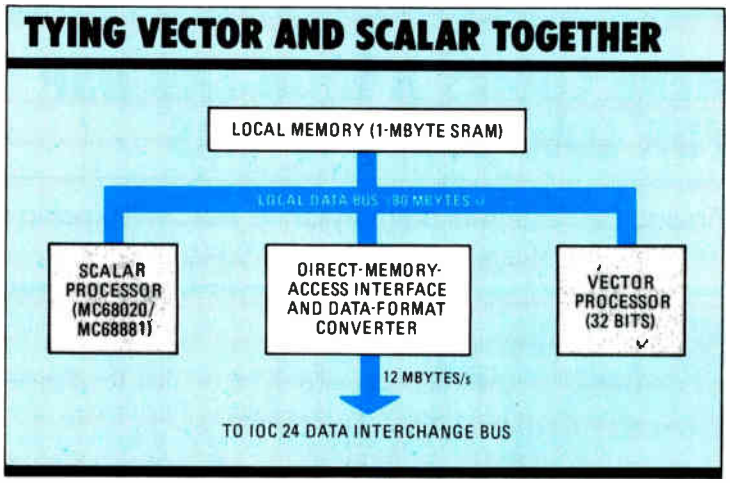
The VSP-1 architecture includes a general-purpose 32-bit microprocessor-based central processing unit as the scalar processor, a direct-memory-access interface and data-format converter, and a 32-bit floating-point vector processor, all sharing access to 1 Mbyte of SRAM on an 80-Mbyte/s local data bus. The general-purpose CPU is based on a Motorola Inc. MC68020 microprocessor, operating at 10 MHz. An MC6881 scalar floating-point unit and an MC68851 memory-management unit complete the CPU. The vector processor part of the VSP-1 vector/scalar processor uses the Weitek Corp. 1232/1233 32-bit adder/multiplier and the 1066 shift register. "We chose the Weitek parts because of the amount of software available for them and because it is a mature component family," Bowles says. The Weitek chips come with a complete application subroutine library.

Low-level control of the VSP-1 is provided through registers accessible through the I/O computer data interchange bus. This allows the I/O computer to start the VSP-1, run diagnostics on the VSP-1, and initiate vector processing. This control path also provides direct communication from any other processor in the I/O computer to the VSP-1.

The DMA interface is controlled by the VSP-1 CPU's supervisor program and provides high-speed, low-overhead transfers between the 1-Mbyte local memory and the I/O computer's main memory. Transfers directly across the data interchange bus can be regulated to run between 0.2 and the full 12 Mbytes/s. By being able to control and minimize the transfer rate when full performance is not needed, more VSPs can be accommodated. Transfers to or from another VSP-1 and transfers between I/O processors connected to the I/O computer's Unibus and Openbus interfaces for VAX and other host-computer peripherals in the I/O computer are done through the DMA.

An important feature for signal and image processing supported by the DMA is a broadcast mode in which all the VSPs in the system can be sent the same data simultaneously. The broadcast capability results in a significant system performance improvement.

The VSP-1 hardware is not useful without application software. To make the building of applications for the VSP-1 as simple as possible, Aptec is providing an extensive kit of software for program development to be ready when the VSP-1 is ready to ship. The set



2. The VSP-1 board ties together a vector processor with a scalar processor and 1 Mbyte of fast static random-access memory.

of program development tools for the VSP-1 includes an assembler, linker, librarian, and loader for the scalar processor. And for the vector processor there are a simulator, assembler, linker, application subroutine library, and VSP supervisor, which runs on the scalar processor.

Code that is being targeted for the scalar processor is typically developed on a Digital Equipment Corp. VAX superminicomputer using the language compilers and source-code debugger supplied by Aptec and the standard VMS operating system utilities.

A big boost is given to application-program development for the vector processor by Aptec's library of application subroutines. "It is very comprehensive and has been optimized for the VSP-1 architecture," Bowles says. The subroutine library maintains standard calling conventions and procedure and subroutine names. The parameter syntax is standard throughout the library for simplicity.

The most popular routines for signal and image processing, simulation, and seismic research are included in the library. For example, it has vector and matrix operations; one-, two-, and three-dimensional FFTs, both real and complex; dot-product function; and coordinate tranformations.

Applications programs are written either in assembly language, Fortran, or C, and can also include calls to subroutines in the library. Programs execute from the local VSP-1 memory and find their data there also. The programs manage and access blocks of the IOC-24 memory and shuttle data and code in and out of the local memory through the DMA interface.

When needed, the program calls upon the vector processor to perform the high-speed vector-computing tasks. The vector processor's code runs out of its writable control store. A program can also call on other system processors to perform various file management, I/O synchronization, and computing tasks. The VSP-1 receives data or control interrupts on the data interchange bus in two ways: either through its own unique address or on one of the four broadcast addresses. *–Tom Manuel*

For more information, circle 481 on the reader service card.

HERE COMES A HIGH-END DSP FOR LOW-COST SYSTEMS

Analog Devices puts memory on its best-selling chip for systems where volume and price are crucial

Analog Devices Inc. is turning its digital-signal-processing microprocessor into a microcomputer that can handle cost-sensitive high-volume applications. The new microcomputer is faster than other single-chip DSPs, says Analog Devices, and it offers some functions they don't—such as automatic data buffering and flexible buffer definition.

The Norwood, Mass., company is creating its ADSP-2101/02 DSP microcomputer by embellishing its best-selling ADSP-2100 microprocessor chips. It added data and program memories, an oscillator, two serial ports, an interval timer, and two multiplexers. Yet the new DSP microcomputer chips are housed in 68-pin packages whereas the 2100 microprocessors need 100-pin packages for the extra signals to access external memory. The smaller package makes the 2101/02 suitable for designers who want to build simple DSP systems at low cost.

The 2101/02 can do a 1,024-point in-place radix-2 complex fast Fourier transform in 4.4 ms with scaling; and that, says the company, compares with 6.4 ms and 22.5 ms, respectively, for two other popular single-chip DSPs, the Motorola DSP56000 and the Texas Instruments TMS320C25. The Analog Devices chips do a 1,024-point radix-4 FFT complex in 3 ms, with scaling, compared with 17.5 ms for the TMS320C25. And the 2101/02 can do a finite-impulse-response filter at 80 ns per tap; comparable figures are 97.5 ns per tap for the Motorola chip and 100 ns per tap for the TI chip.

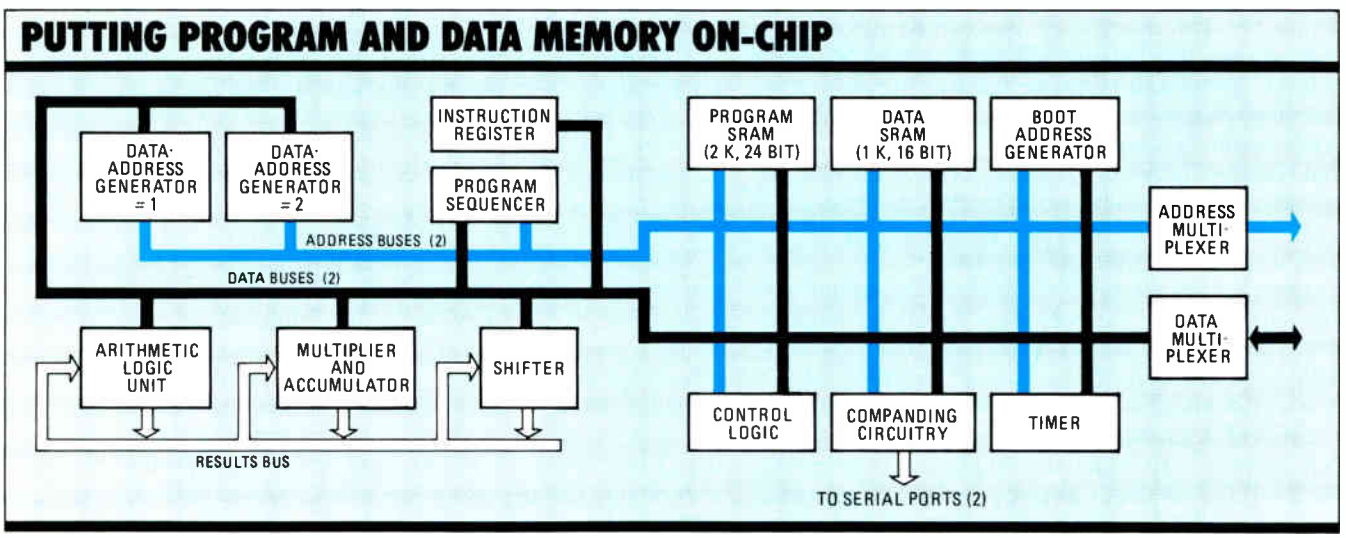
In a little more than two years, the 6- and 8-MHz ADSP-2100 microprocessor chips have become the second most widely used programmable microprocessor architecture for high-speed DSP applications, trailing only the TMS 32000 family from Texas Instruments Inc. in design wins. And Analog Devices recently introduced 10- and 12.5-MHz versions of the 2100 series, called the ADSP-2100A. Both the original 2100 and the newer A versions are being used in image-processing, missile-control, high-performance-modem, speech-recognition, and data-compression applications.

The ADSP-2100 and 2100A processors incorporate computational units, data-address generators, and a program sequencer all on one chip. However, their data and program memories are external devices. The need for outboard memory devices makes them less attractive for cost-conscious users in volume applications—the external devices cost more and take up more board space.

Now come the new microcomputer chips, the ADSP-2101 and 2102, in which the data and program memories reside on the chip (see fig. 1). The on-board memories allow Analog Devices to aim them at applications where the 2100/2100A series does not fit well because systems built around them end up being overqualified and too costly. Additional on-chip features help designers keep their DSP systems simple and inexpensive and therefore suitable for high-volume production. Two double-buffered serial ports, for example, provide automatic data buffering, and the integrated oscillator can be driven from an inexpensive crystal. In addition, a set of software development tools is available to make it easier to design systems that use the chips.

Even though simple and low in cost, these new DSP systems offer impressive performance. Like the 2100A processors, they sport an instruction-execution rate of 10 or 12.5 MHz.

Their main advantage, though, is the on-chip memory. The feature is not unique to the 2101/2102, but it and the other features combine to make the devices especially suitable for a broader range of DSP uses, some of which Analog Devices had to walk away from



1. The new DSP microcomputer chips from Analog Devices Inc. include large on-chip program and data memories with a choice of RAM or ROM.

until now because heir high-volume, cost-sensitive nature made use of the 2100 impractical. Those include telecommunications, such as European mobile radio, where system size and cost are important considerations.

The difference between the two models of the new microcomputers, the 2101 and 2102, is in the types of memories used. The ADSP-2101 is a random-access-memory-based device intended for lower-volume products and for prototyping. The 2102 is a mask-read-only-memory version aimed at volume usage—that is, usage encompassing at least 10,000 pieces per year. Both units will sell for $54 each in quantities of 1,000, compared with $132 each for the 6-MHz version of the 2100 in quantities of 500.

Samples of commercial versions of the devices are scheduled for availability in the fourth quarter of this year, with production quantities set for the first half of 1989. Units that meet MIL-STD 883B Revision C are scheduled for sampling in the first quarter of 1989. The company expects volume production to follow in the third quarter.

To get the memories and additional functions onto the new chips and still shrink the package, Analog Devices designers have taken advantage of a newer CMOS process with finer geometries. The old 2100 is fabricated in a 2.0-μm drawn, 1.5-μm effective process. By contrast, the newer parts use a 1.0-μm drawn, 0.8-μm effective process.

The 2101/2102 series internal DSP architecture is identical to that of the 2100 except that the latter's 24-bit-by-16-word instruction cache is supplanted by the on-chip program memory. The two product series are object-code program compatible.

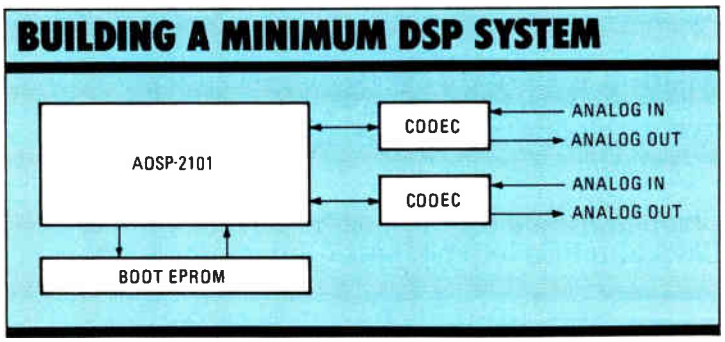
TWO TYPES OF MEMORY

Two types of on-chip memory are provided: a 1-Kbyte-by-16-bit data RAM, which is expandable to 16 Kbits off chip; and a 2-Kyte-by-24-bit program/data memory, also expandable off the chip to 16 Kbits. The latter can store both programs and data. The difference between the 2101 and 2102 is in this block's implementation. In the 2101, the program/data memory is all RAM; in the 2102, any fraction of it can be implemented in masked ROM for systems in which the volume is sufficient to justify the mask costs.

"Having both program and data memory available means that the microcomputer can fetch the next instruction and the next two data values in a single cycle, even if one of those accesses is an external fetch," says David Fair, strategic marketing manager in the Digital Signal Processing Division. In the 2100, only one data value is fetched per cycle.

Further, internal program memory can be loaded from an external byte-wide 2764 erasable programmable ROM. "Customers indicated an interest in having that ability because it allows them to update their systems simply by changing the EPROM, which is a $2 or $3 part," Fair says. He points out further that as many as eight programs can be loaded into the 2101/2102 using a 27512 EPROM.

Like the on-board memories, the two double-buffered serial ports are not unique in the DSP market.



2. A simple DSP system is easy to build with the ADSP-2101; all that's needed is two codecs, an EPROM, and a clock.

But, again, they make possible other functions such as automatic data buffering and flexible buffer definition. These are available only on the 2101/2102, according to Fair. Two full-function data address generators are included.

Flexible buffer definition means that the system designer can specify the length of the buffer, depending on the complexity of the algorithm to be executed. Then when the receive buffer is full or the transmit buffer is empty, a data-transfer instruction is automatically generated without a system-slowing program interrupt. Program interrupts not only slow the system, but they also require software overhead to accommodate the switching necessitated by interrupts. On the other hand, if interrupts are desirable in a given application—for example, when checking for certain data or a range of data values—one of the serial ports can be reconfigured for two additional external interrupts.

Analog Devices designers put an oscillator on the 2101/2102 chip to further minimize costs for system designers. Instead of the more expensive off-chip clock required by the 2100, the new microcomputer's oscillator can be driven from an inexpensive crystal or clock that runs at four times the processor instruction rate—40 MHz for the 10-MHz chip, for example.

With so much complete computer capability on the 2101/2102 chips, a minimum system that is very simple and inexpensive to build can be designed to perform advanced signal-processing applications. Such systems can be made very small for embedded and mobile applications. One example of a minimum system (see fig. 2) would need only four parts in addition to the ADSP-2101 chip—two decoders/encoders, an EPROM chip for booting programs into the DSP chip's program memory, and a clock or crystal.

Software development tools will be available on a similarly phased schedule. They include cross software for the IBM Corp. PC, the Digital Equipment Corp. VAX/VMS, and Berkeley 4.2 Unix; an in-circuit emulator with a trace option; and a C compiler.

The cross-software modules include a system builder that translates a user-defined description of the target hardware system into a form that can be used by other cross-software modules. The other cross-software modules are a linker, a PROM splitter, and an ADSP-2101/2102 simulator. *–Lawrence Curran*

For more information, circle 482 on the reader service card.

THE FASTEST DSP ADD-ON BOARD AROUND HITS 8 MIPS

Chips from Analog Devices help West Germany's CMS turn PCs into high-speed number crunchers

The fastest digital signal processing add-on board now available for IBM Corp. PC AT and compatible personal computers runs at a blazing 8 million instructions/s. It turns a PC into a high-speed signal processor and a number cruncher for real-time applications. The board comes from a company in Ettlingen, West Germany called CMS GmbH.

When four of CMS's DSPB 2100 boards are plugged into a PC, it becomes a powerful 32-mips number cruncher selling for less than $25,000. But for most real-time applications just one board will do, says Jürgen Walter, co-owner of CMS—the name stands for Computergestützte Mess-systeme, German for computer-aided measuring systems—and head of development at the four-year-old, 18-person firm. Plugged into a PC, a single board will handle frequency analysis jobs "about 50 times faster than an IBM PC AT fitted with Intel's 80386 microprocessor and 80387 arithmetic processor," Walter says.

Thus far, CMS has built about 100 of its DSPB 2100 boards. Deliveries are starting now, with marketing abroad scheduled to start this spring. A version for the Apple Macintosh II will be available by mid-year, and a faster version of the board—12.5 mips—is planned for later this year. The price of the current 8-mips board, including software and documentation, is about $4,450.

The board owes its speed to three factors. One is the use of a fast DSP chip made by Analog Devices Inc. of Norwood, Mass. The second is a large amount of fast memory that keeps data ready for the processor. The third is the DSP architecture, which CMS has designed to avoid timing and communication delays, incorporating input/output sections that offer a fast link between the PC and the board.

The basis of the 2100 is the Analog Devices ADSP-2100 single-chip digital signal processor. Running at a 125-ns clock speed, the DSP chip delivers the board's peak performance of 8 mips. The chip uses a modified Harvard architecture with separate paths for data and instructions.

The architecture of the DSP chip allowed the CMS designers to be creative in the memory architecture of their DSP board, installing on the DSPB 2100 an unusually high memory capacity for a DSP board. Included on the board is a boot-paging read-only memory for the boot program of up to 8 Kbytes by 24 bits and a 16-Kbyte by 24-bit random-access memory in the program-memory section. Also included are a 16-Kbyte-by-24-bit data RAM in the program memory and a 16-Kbyte-by-16-bit data RAM in the data-memory section (see figure).

The board architecture is based on design principles used for decentralized process control and data management systems in real-time applications. Therefore, the interfaces between the board and the host PC facilitate a fast and independent exchange of data and programs, which helps to avoid overloading the PC bus.

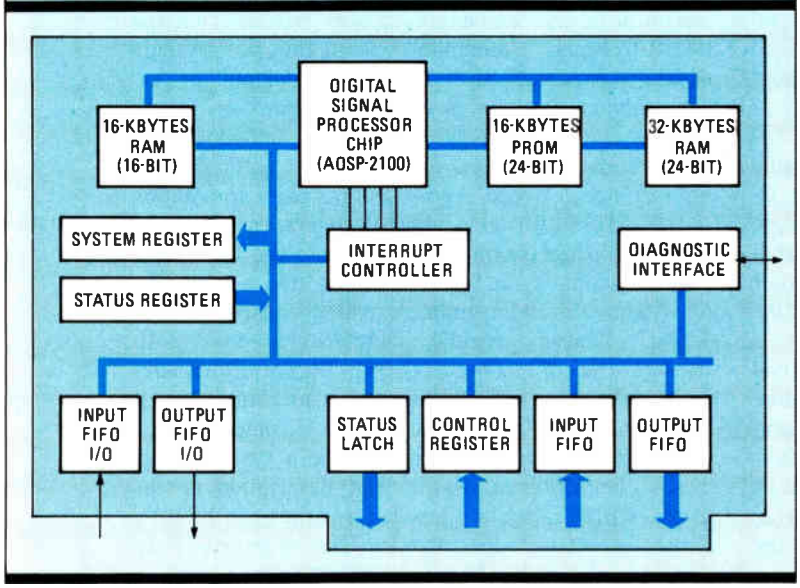
Data can be read into the board at a rate up to 70 Mbytes/s. Each of the board's two inputs and two outputs handles a 16-bit word and has a 1-Kbyte first-in, first-out buffer.

Another design element that further enhances the board's speed is the way the board is coupled to the host PC. To prevent overloading of the PC's data bus, the incoming signals are fed via an on-board parallel bus and the FIFO buffer memories into the board's processing section. With this concept, the data throughput is boosted even when the PC uses several DSP boards. The signals coming in at up to 70 Mbytes/s are distributed over the input FIFOs of up to four boards. Data reduction takes place on board. The compressed data is fed to the PC's data base for storage or to its monitor for display.

A follow-up product to the DSPB 2100, a 12.5-mips board, is now in development at CMS. It will use a faster version of the ADSP-2100 DSP chip and will reach the market four to six weeks after Analog Devices starts delivering that chip in volume—Walter figures the 12.5-mips boards will be available during the fourth quarter of this year. *–John Gosch*

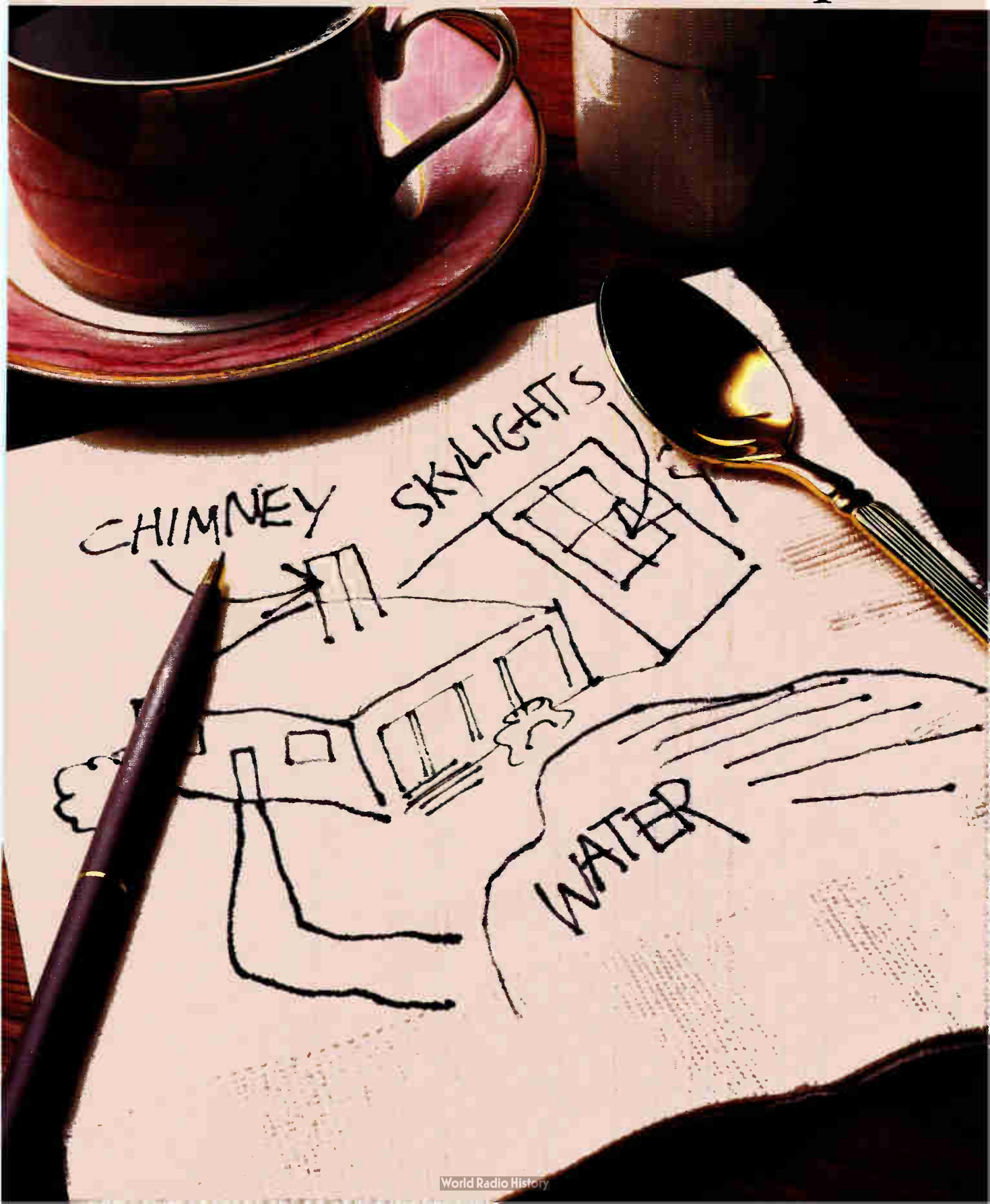
For more information, circle 483 on the reader service card.

A MEMORABLE DSP BOARD



CMS GmbH incorporates a great deal of memory on its DSPB 2100 boards, which keeps data handy for processing and therefore speeds the board's operation.

What do you need to build on a rough application concept?



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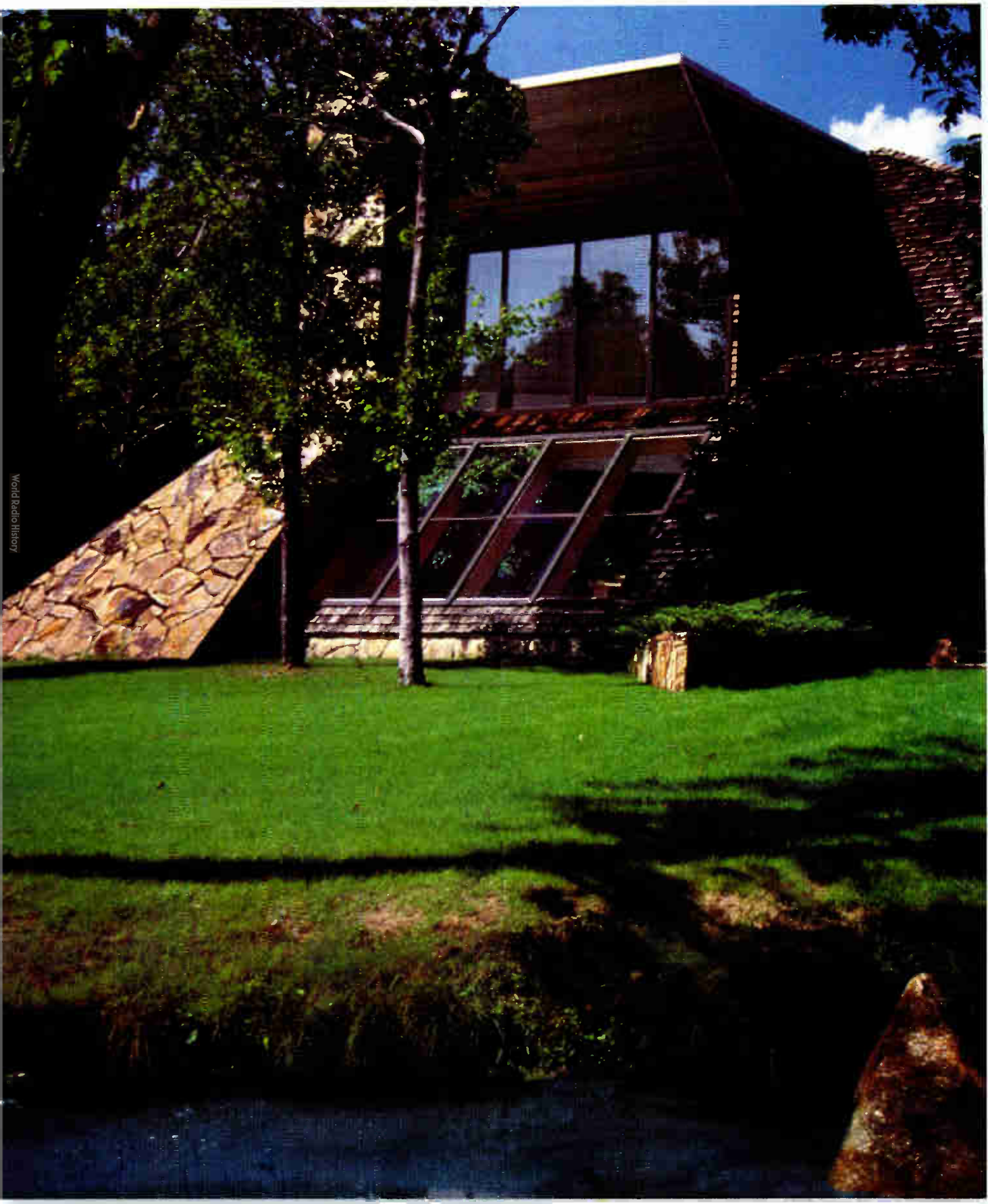

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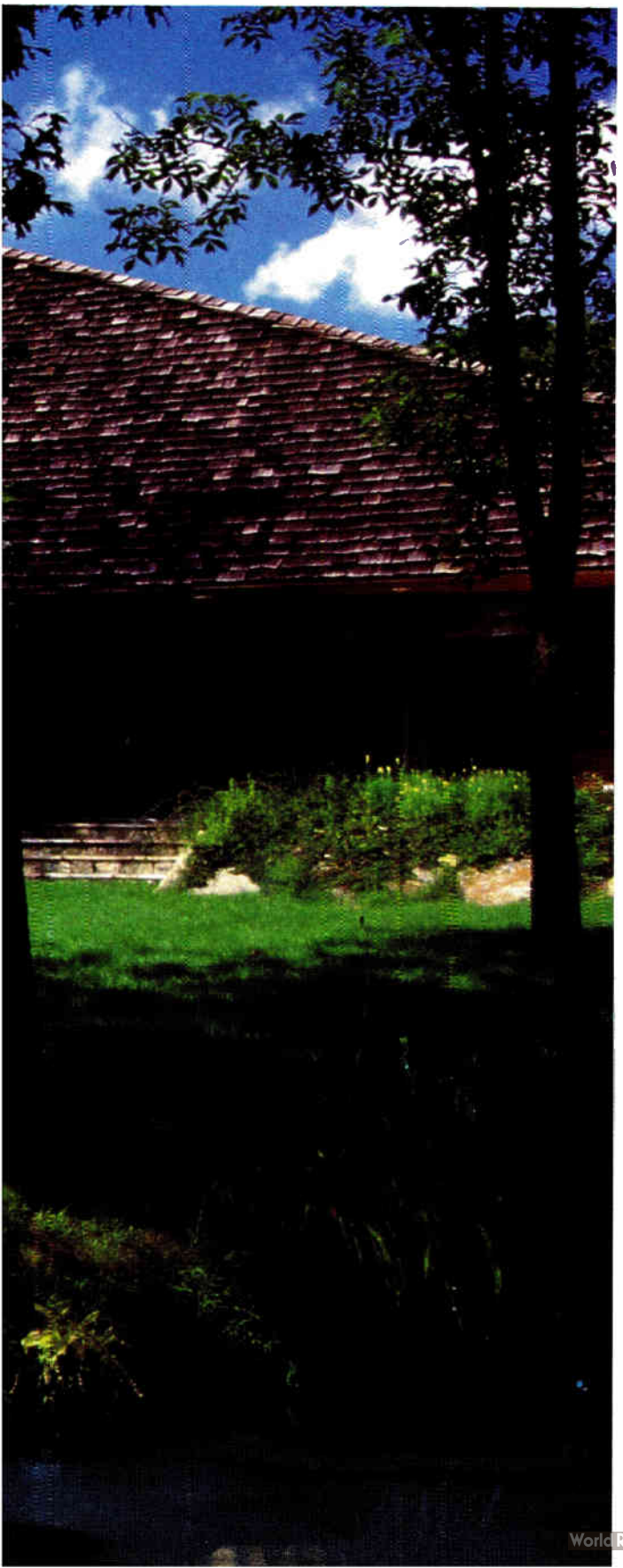

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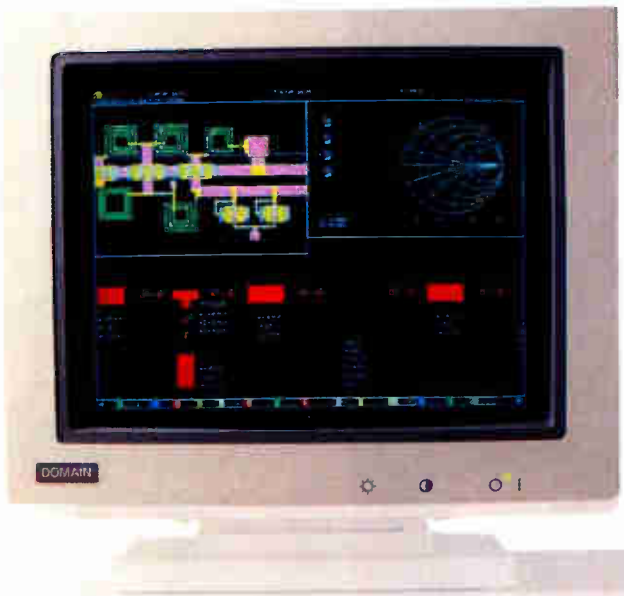

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FUJITSU UPS THE GATE-ARRAY ANTE: 90,000 USABLE GATES

A basic gate cell is the key to achieving high density without sacrificing speed or utilization

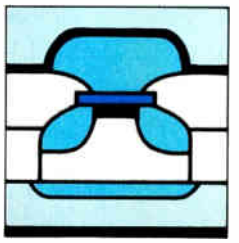
The limits are being stretched again in the drive to combine high density and high gate utilization in CMOS gate arrays. Jumping ahead of its competitors, Fujitsu Microelectronics Inc. of Santa Clara, Calif., has developed a new family of 1.25-μm CMOS gate arrays that combines three levels of metal interconnection with what it calls a sea of basic cells to achieve densities as high as 100,000 gates and gate utilization rates as high as 80% to 90%.

Designated the AU series, the new family (see fig. 1) ranges from the 30,000-gate C-30KAU to the 100,000-gate 100KAU. And depending on application and the mix of memory and logic, Fujitsu specifies a basic cell-utilization rate of up to 75%, says Zohair Mogri, the company's semicustom product marketing manager. However, when calculated the way the industry does, he says, gate-utilization rates translate into about 80% for a pure logic implementation and to about 90% for a mixed memory and logic design. By comparison, he says, most present three-level implementations using standard sea-of-gates implementations are capable of gate-utilization rates of no more than 80% for designs that mix memory and logic. The Fujitsu arrays are capable of implementing embedded static random-access memory blocks of up to 16 Kbits, with access times of 20 ns. On embedded read-only memory with densities up to 64 Kbits, access time is only 25 ns.

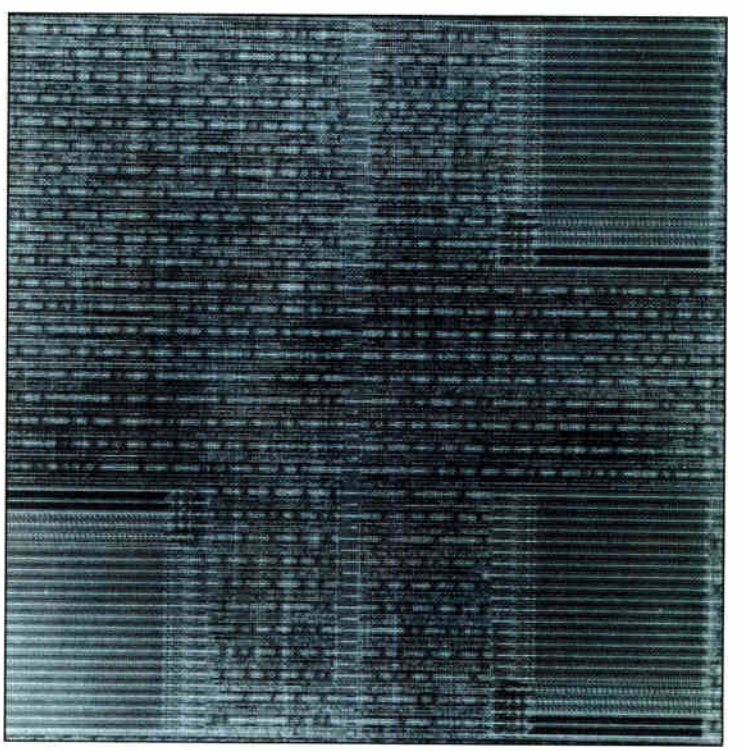
Key to achieving such high densities without sacrificing either speed or high gate utilization is the use of a proprietary basic gate cell. The cell consists of four normal-size transistors, two n-channel and two p-channel, similar to a standard gate, to which four more smaller n-channel transistors, optimized for memory, have been added (see fig. 2). The exact size of both sets of transistors is proprietary, Fujitsu managers say, but the smaller transistors are no more than a tenth the size of normal-size n-channel transistors and a twentieth the size of the p-channel devices. This arrangement results in a basic cell about 5% to 10% larger than typical two-input NAND or NOR gates used in most arrays, Mogri says, but the larger size is more than offset by the increased gate utilization in a typical design.

Each device in the family consists of an array of anywhere from 30,000 to 100,000 gates. Unlike present arrays, they have no dedicated wiring channel regions in between the columns or rows—dedicated channels restrict the way arrays can be connected and sometimes result in a long interconnecting line, which cuts down speed. Basic cells are spread throughout the chip, except in the input/output region, with wiring channels that can be allocated freely in discrete units wherever necessary. In addition, logic and memory blocks can be placed in arbitrary positions anywhere in the array.

Fujitsu's design contrasts with other approaches to uncommitted-gate-array design, which are generally based on basic gate structures optimized for logic rather than memory design—even though many applications require a mix of the two, especially at higher densities. A typical uncommitted gate array consists of four transistor gates suitable for implementing such basic logic functions as two-input NAND or NOR gates. It is usually implemented with basic cell columns separated by dedicated wiring channels between them. The disadvantage of this approach, says Mogri, is that to implement a memory cell requires the use of anywhere from two to eight gates. While this is acceptable for small density memories below 4 Kbits, he says, at higher densities—anywhere from 16 to 64 Kbits—the arrangement results in considerable wasted space being consumed by the unused channel regions between gates.



One alternative that allows chip designers to incorporate large memory blocks without wasted space and the reduced gate utilization that results is to use a structured array approach. In such an approach, blocks of RAM or ROM of predetermined size reside in specific locations. This allows an array to be built with normal-sized logic transistors in the logic portion and with smaller n-channel transistors in the memory blocks. Doing so does increase the overall overall gate

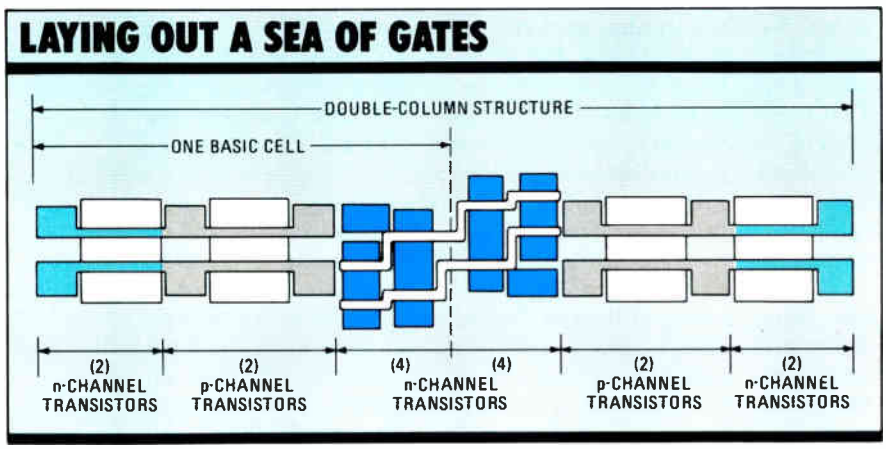


1. In the 75KAU, one member of its AU family, Fujitsu achieves gate utilization of 75% by combining three-level-metal and proprietary gate design.

count, says Mogri. However, it also cuts down on gate utilization in the logic portion. And it tends to increase cost, because the structured array must be designed with predetermined applications in mind.

Another solution that has been pursued by many manufacturers is a variation on the sea-of-gates approach, in which small memory cells are embedded under predetermined wiring channel regions. While this approach allows a memory block to be located anywhere on the array, it is still requires more than one gate to implement a single memory cell, Mogri says.

Fujitsu engineers have overcome the limitations of each of these approaches by taking the opposite tack. That is, rather than adding transistors to the array outside the basic logic cell in order to reduce the number of gates required to build a memory cell, Fujitsu designers have instead used as their starting point an entirely new building block, a basic cell. With its four logic transistors and four n-channel transistors, the devices in the new family can serve as either memory or logic elements with equal efficiency. Unlike the structure of traditional gates, the logic transistors have separate source/drain regions while the n-channel transistors have a common source/drain region for each pair.



2. Key to high density and high gate utilization in the series is a proprietary basic cell with four normal-size logic gates and four smaller n-channel transistors.

The advantage of such a structure is that memory and logic cells can be fabricated separately or in combination in the same basic cell. Twenty-four vertical wiring channels, using the first aluminum layer, can be allocated in one column of basic cells and six horizontal wiring channels, using the second aluminum layer, can be allocated in one row of basic cells.

But the most important benefit, at least in memory-intensive designs, is that a six- or eight-transistor SRAM cell can be constructed with a single basic cell, or one logic gate. In conventional uncommitted-gate-array implementations that are not optimized for memory design, a comparable memory cell requires anywhere from two to four logic gates, says Mogri.

To further improve gate utilization in mixed memory and logic designs, the Fujitsu array uses a double-column structure as its basic repetitive element. In this structure, each set of basic cells consists of mirror images; that is, in each set, one of the cells has been flipped over so that the n-channel transistors abut each other. The result of such a configuration, says Mogri, is a significant improvement in the ratio of the cell area to wiring channel area over the standard single column structure by at least two to three times.

In an eight-transistor SRAM, the transmission gates and latches can be built using normal-sized transistors only or using normal-sized p-channel devices for the transmission gates and the smaller n-channel transistors for the latches. In a six-transistor SRAM, transmission gates are built using normal-sized n-channel transistors and the latch with smaller n-channel devices.

In the Fujitsu arrays, designers can take advantage of higher-density layout alternatives not available in other arrays. Using conventional techniques, a logic element can be built in a Fujitsu array using normal-sized transistors, with the small-transistor regions used for wiring channels. In this approach, a column of basic cells between columns of logic cells is used as a wiring region for 24 channels. Alternatively, every column of basic cells can be configured so that 10 wiring channels can be allocated in the small transistor regions of adjoining basic-cell columns. This eliminates the need for using alternating basic-cell columns as wiring channels, in effect doubling the density of the array. A third possibility is to take advantage of the fact that the driving capability of a pair of parallel-connected small transistors is the same as that of normal-sized transistors. Taking advantage of this, a higher level logic implementation such as a 4-bit full adder and a shift register can be built in a much smaller area by using two adjoining columns. This approach doubles the gate density over comparable designs built with one column of basic cells.

Indicative of the higher efficiency of this new approach is the complexity and gate density of some typical test designs using a two-level-metal, 1.8-μm CMOS 30,000-gate implementation of the same basic architecture. For example, a 16-by-16 multiplier with a 32-bit block-carry lookahead added, a 16-by-16 array, and 32-bit input and output registers can be achieved with as few as 10 basic gate cells with a gate density of about 320 gates per mm^2, equivalent to that of many standard cell layouts, say Fujitsu engineers. The multiplier array alone, the company says, contains about 3,000 gates, has a gate density of about 230 gates/per mm^2, about 1.5 times that of a conventional uncommitted gate array. A 16-bit-by-64-word eight-transistor SRAM has a density of 230 bits/mm^2, two to three times that of conventional arrays, the company says. A 16-bit-by-256-word ROM, on the other hand, has a bit density of 1,900 bits/mm^2, about five times higher than conventional gate arrays. In the triple-metal CMOS implementation of the same architecture, says Mogri, gate densities and complexities should be at least doubled. *-Bernard C. Cole*

For more information, circle 484 on the reader service card.

SCSI RIVALRY HEATS UP AS NEW CONTROLLER CHIPS VIE

Chip makers turn their attention to computer OEMs; will IBM endorse SCSI for personal computers?

The race is heating up to develop high-performance, multifeatured controller chips for disk drives using the Small Computer System Interface. Emulex Corp. and NCR Microelectronics, its second source, are rolling out a new chip to counter the recently introduced controller from Adaptec Inc. The new generations of chips are the main weapons in the two camps' fierce competition for first place in the high-end SCSI market. And the stakes could go even higher: speculation is mounting that IBM Corp. is about to endorse the SCSI standard for personal computers. Adding IBM's Personal System/2 line and upcoming PS/2 compatibles would give the SCSI market a big boost.

The third-generation SCSI device from Emulex, of Costa Mesa, Calif., and NCR, of Ft. Collins, Colo., matches many of the innovations in the AIC-6250 controller chip from Adaptec, of San Jose, Calif. Notable among these innovations are a 16-bit data bus and separate 8-bit control bus, a configuration first introduced in SCSI controller chips in Adaptec's AIC-6250 [*Electronics*, Aug. 20, 1987, p. 61]. In previous SCSI chips, one bus carried both data and commands.

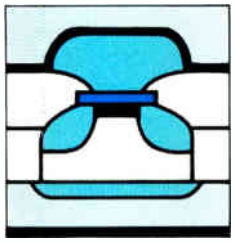
Emulex and NCR are introducing two versions of their new controller chip. The Emulex ESP+1 and the NCR 53C94 offer single-ended input/output pins, and the ESP+2, and NCR 53C95 offer differential I/O pins. They'll be available in the third quarter, and Emulex says they'll cost less than $25 each in original-equipment manufacturer quantities.

If IBM adopts the SCSI interface, the market for SCSI chips will explode. But even without the additional demand that IBM would represent, Joe Molina of the Technology Forum in Chanhassen, Minn., says that unit sales of SCSI chips will grow at an annual 30% rate, from 3.8 million units in 1988 to 6.5 million units in 1990.

What fueled the latest heat in the SCSI race was Adaptec's move to a separate 8-bit control bus and its widening of the data bus from 8 bits to 16 bits. The separate control bus overlaps commands and data, which speeds up the execution of commands. The wider data bus enables the Adaptec AIC-6250 to transfer data at 20 Mbytes/s—four times faster than earlier SCSI chips. The new Emulex/NCR chips boast a 16-byte buffer—twice as deep as Adaptec's—to achieve a burst data transfer rate of up to 24 Mbytes/s.

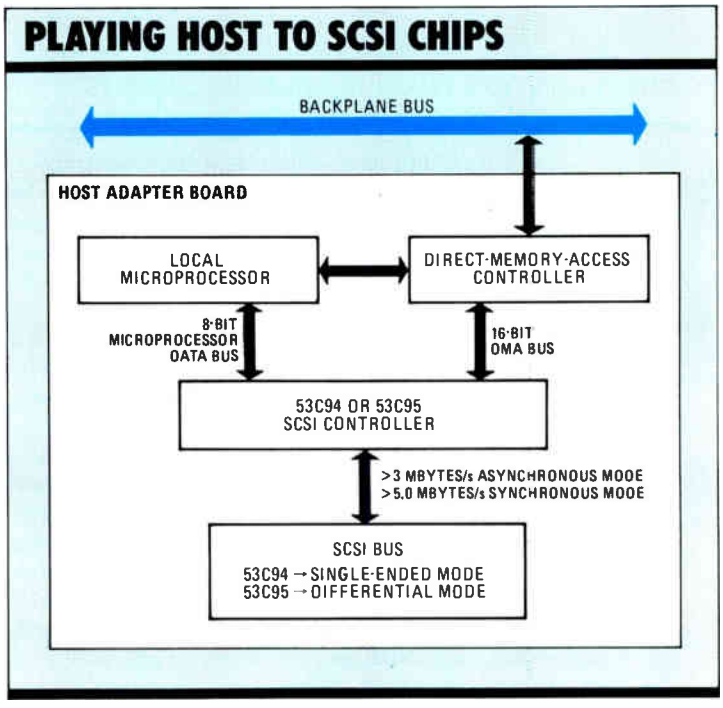
An important plus for the new Emulex/NCR chips is the reduced time required to transfer blocks of data, says Harry Mason, product line manager at NCR. The key, he says, is adding the 16-bit data bus and improving the on-board state machine, which handles bus overhead. He says throughput—the time it takes data to go from a peripheral device, through the SCSI controller chip, to the SCSI bus—has two components: the overhead to get on and off the bus and the transfer period for a data block.

The second-generation chip, the Emulex ESP, or NCR 83C90, took 1.5 ms total—0.5 ms of bus overhead and 1 ms for data transfer—to transfer a 1-Kbyte block from a disk drive to the SCSI interface. Other chips need anywhere from 1.2 to 1.8 ms. Now, the new Emulex/NCR chips reduce the 1-Kbyte transfer time to 900 μs, Mason says.



A number of the new ESP+ chips' features are responses to innovations on the Adaptec AIC-6350, concedes Gary De Rochers, director of marketing at Emulex. One such feature of the Emulex/NCR chip is the ability to combine and link multiple commands; for example, a seek command linked to a read command. Another feature, aimed at the computer-system OEMs, is through parity—bits added to the data and transfered along with the data to the host computer's memory. This feature is a response to the trend toward checking data going to and from random-access memory, which is more error-prone than earlier, lower-density RAMs.

Meanwhile, the stakes may be rising in the sharply competitive SCSI market—as more computer-system manufacturers are won over and begin adopting SCSI interfaces (see figure). "Until now, most computer manufacturers have not adopted the SCSI interface as aggressively as have the drive manufacturers," says Kenneth Hallam at ENDL Inc., a market research firm in Saratoga, Calif. Two exceptions are Apple Comput-



SCSI controller chips can find work on a host computer, as shown here, although until recently, the chips were embedded mostly on disk drives.

er and NCR's General Systems Division—both of whom are NCR customers.

So the struggle between Adaptec and Emulex/NEC is shifting to winning design starts among computer system makers. Adaptec admits says it has not been as successful in selling to drive manufacturers as Emulex and NCR, but it says it is doing well in the competition for computer manufacturers installing SCSI ports.

And it's also getting some ideas for its next-generation chip. "When we showed the 6250 to computer system manufacturers, they liked its 16-bit host bus interface. But most new designs are built with 32-bit microprocessors so they wanted a a 32-bit version of the 6250," says G. Venkatesh, marketing manager at Adaptec. To use the 16-bit-wide SCSI chip on a 32-bit computer design, a computer manufacturer calls for two chips, with some external interface and control logic, to create a 32-bit-wide controller.

The Adaptec AIC-6250 was a response to the success of the ESP and 53C90, the second-generation Emulex/NCR chip. "The ESP and 53C90 won a number of design-ins with various disk-drive manufacturers—Micropolis and Maxtor, among others—which embedded the SCSI controller on their drives at the expense of Adaptec," say Dal Allen, an ENDL market researcher. The Emulex/NCR chip's success encouraged Logic Devices Inc. of Sunnyvale, Calif., and Advanced Micro Devices also of Sunnyvale, Calif., to enter the market with almost identical products.

What made the Emulex/NCR second-generation chip so attractive was the availability of a companion chip, the Merged Architecture Controller chip. The MAC performs the control functions needed to carry out SCSI commands received by the SCSI chip. For example, if the command is a seek, the MAC chip directs the disk drive to move the read/write head to the desired track location.

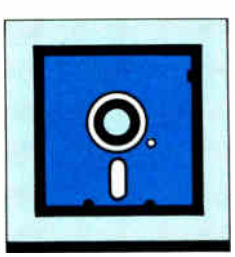
That is one area where Adaptec concedes a disadvantage. "We have not had as complete a solution," says Venkatesh. "However, we have recently addressed the problem by teaming up with National Semiconductor. Their 8466 disk-controller chip is a good match for our 6250 and the combination makes us more attractive to drive manufacturers."

But there's no question that the battle is now shifting to design wins at computer makers, and that's why IBM's endorsement of the SCSI standard for PCs is so important. Word from a recent analysts' meeting held recently in Boca Raton, Fla., is that an IBM representative showed an I/O specification for a future product and said that it was an implementation of the SCSI interface. "It appears that IBM is about to announce synchronous SCSI," says Philip Devin, senior analyst at Dataquest in San Jose, Calif. The speculation is that the SCSI port will appear on the upcoming PS/2 model 70. The port will enable the system to accommodate a wide variety of I/O devices—CD-ROM, document scanners, printers, write-once optical disk drives—and possibly even a 5¼-in. erasable magneto-optic disk drive. *–Jonah McLeod*

TECHNOLOGY TO WATCH **SOFTWARE**

NOW, A PRACTICAL WAY TO RUN DOS CODE UNDER UNIX/80

With Hunter software, the conversion is a one-time operation with no limit on the number of users



Until now, a user of a time-shared computer terminal or a work station who wanted to run an MS-DOS application program on a Unix system had two choices: use third-party software that emulated the MS-DOS application in the work station or computer's Unix environment, or buy an add-in board to plug into the computer backplane. The former usually turned out to be very slow; the latter, very expensive.

But Hunter Systems Inc., a Mountain View, Calif., third-party software supplier, has solved the dilemma with a new software product, XDOS. Unlike a software emulator, XDOS converts the binary code of the MS-DOS application into binary code that can run on a 68020 central processing unit under the Unix operating system. It is being licensed to computer original-equipment manufacturers and has a suggested price of between $425 and $2,000, depending on system size—a far cry from the costs of providing each computer or work station with its own $2,500 add-in card. And like any Unix application, it can be shared by any number of users.

A front-end processor in XDOS (see figure) performs a global-flow analysis—a method of learning and then imitating logical operations—to determine how an MS-DOS application uses the operating system and hardware environment. It then converts the MS-DOS program into a Unix application, which can run on the target system as fast as or faster than the original MS-DOS program would on a personal computer. The converted application is passed to a back-end processor, which executes the program in the Unix environment. Because the program has been converted into a Unix application, it can be shared among any number of users.

The techniques used for global-flow analysis have been used in the past by optimizing compilers. "Compiler techniques that make programs run quickly on RISC computers are the same techniques we use to convert an 80286 machine-language program efficiently into 68020 and eventually RISC machine language," says Colin Hunter, president of Hunter Systems. "But we use global-flow analysis to determine how best to convert one machine language program into another, instead of compiling a high-level language efficiently into machine code for a processor."

Back-end processors use a library of system functions that emulate in the Unix environment the operating system features of the MS-DOS environment. So XDOS supports different 68020-based Unix systems; in

the future, it will support several different reduced-instruction-set processors running on Unix. XDOS has only one complex front-end processor and several simpler back-end processors, keeping the cost to modest levels with a potentially large market in the installed base of Unix systems.

The front-end processor is the key element that distinguishes XDOS from other software-emulation solutions. It makes the conversion of the MS-DOS application into a Unix environment a one-time task as opposed to the use-by-use approach of the other emulator-based converters. Each time the user with emulator software calls the MS-DOS application, the emulator runs concurrently, generating the same number of additional 68020 instructions for every original instruction. This can generate as many as 15 instructions for every instruction in a PC application, because an emulator program evaluates each instruction in real time and gives equivalent orders to the target system.

With XDOS, by contrast, the front-end processor analyzes the MS-DOS application off-line and then converts it into a Unix application, a one-time task which can take between five and ten minutes of computer time. Thereafter, the MS-DOS application exists as a Unix application on the target system; the original program need not be used again.

To do this conversion, the front-end processor's global-flow analysis follows a sequence of instructions in the program being converted until it encounters a conditional branch instruction. The analysis follows the flow through one branch until it reaches the leaf procedures—those routines that do not call or jump to any other program. The analysis repeats for every possible path in the program.

One example of the superiority of global-flow analysis to a simulator is its intelligent approach to the condition codes, or flags, that result after the execution of an instruction. It is able to determine what must be evaluated and what is irrelevant to the program. An emulator, on the other hand, cannot determine what is vital and what is not.

An arithmetic or logical operation can produce a number of results—overflow, a zero result, a negative or positive result. Each of these conditions sets a flag which the application can evaluate after the arithmetic instruction is executed. In many cases, however, the flags are not relevant to the program. For example, if the applications programmer writes an add instruction, he may never examine the flags after the operation because the outcome of the operation may not be relevant to the flow of the program. Global-flow analysis looks ahead in the program flow to determine which, if any, flags are checked following an arithmetic operation. If none is checked, no flag is simulated. An emulator, however, has no way of knowing if the flags will be checked later in the program or not. Thus, it must assume that they all will be tested and must simulate each flag.

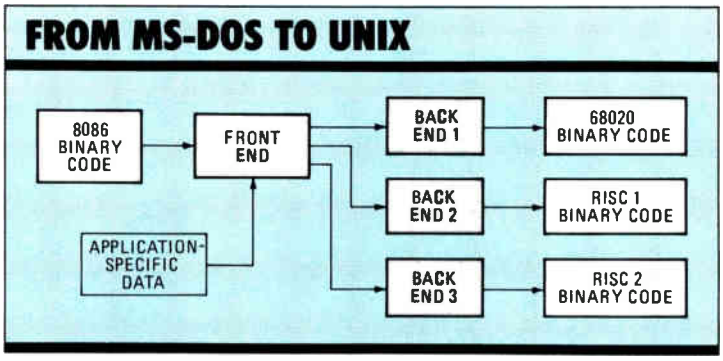
Another example of how the global-flow analysis pays off is by determining when to compensate for differences in programming conventions on the 80286 and 68020. On the 80286, a move instruction does not change the flags during an operation. But on the 68000, a move instruction sets all flags to 0. A program simulating the 80286 on a 68000 will have to save all flags because the simulator has no way of knowing what will occur after later instructions.

Using global-flow analysis, however, the XDOS software only saves the flags when there is an arithmetic operation, followed by a move instruction, followed by a flag-test instruction. This situation will typically occur once per program. If the flags do not require testing, they are not saved.

After the front-end processor performs its flow analysis, it converts the application into binary code for the 68020 microprocessor. However, the code cannot execute as is. The front-end processor provides the code to a back-end processor that performs two functions: configuring the code to execute in a given 68020 environment and directing calls made by the converted program to the correct Unix equivalent in a special library.

Different back-end processors are required for individual 68020 Unix systems, because system manufacturers implement their hardware environment differently. Accordingly, the XDOS back-end processor configures the code to execute in a particular 68020 environment.

A second job for the back-end processor is to direct any calls that the converted program makes to an MS-DOS operating-system function to the correct Unix



A front-end processor converts MS-DOS into 68020-based Unix code; a back-end processor tailors it for a specific Unix system.

equivalent of the function in a special Unix function library. The library contains a set of functions to provide emulation for operating system features of DOS, the BIOS, and the PC hardware.

The library contains functions that emulate the three elements of the operating system with which the DOS application usually interacts during execution. "When the application opens or closes a disk file, accesses the BIOS, or writes a bit pattern to the control register of a device, the back-end processor knows what the application is attempting to perform because of the previous global analysis," Hunter says. "It accesses the library function that provides the Unix resource to perform the function most efficiently.

"Mostly what the back-end processor does is redirect the DOS call down to the appropriate Unix resource," Hunter says. "As a result, the overhead associated with XDOS is small. Instead of simulating the whole behavior of the device, we're just mapping it down into Unix." —*Jonah McLeod*

For more information, circle 485 on the reader service card.

TODAY'S DEFENDER WEARS A DIFFERENT KIND OF ARMOR.

Modern military platforms need more than firepower to survive. Fighter aircraft must jam enemy radar to conceal their positions. Cruisers must coordinate their guns and missiles with split-second timing. Artillery batteries must use laser-guided munitions to strike with pinpoint precision.

Today's defense depends on advanced electronic systems for its success. That's why electronics is such a fast-growing part of military business opportunities, and why Lockheed has positioned itself to be a key participant in this growth.

In 1986, Lockheed's business profile included 20 different lines of business in electronics; and sales can be characterized as approximately one-third electronics and software. By 1991, Lockheed projections show more than half its revenues being derived from these vital technologies. Nearly 40% of Lockheed's engineers now work in these disciplines, and plans started in 1984 should put more than $700-million in new electronics facilities and equipment in place by 1988. The purchase of Sanders Associates in 1986 adds even more capabilities from one of the outstanding companies in the field.

On land, at sea, in the air, and now on-orbit, electronics is the new armor that gives modern military systems their winning edge. Lockheed is making sure this armor fits, no matter where the defense stands guard.

Lockheed

Giving shape to imagination.

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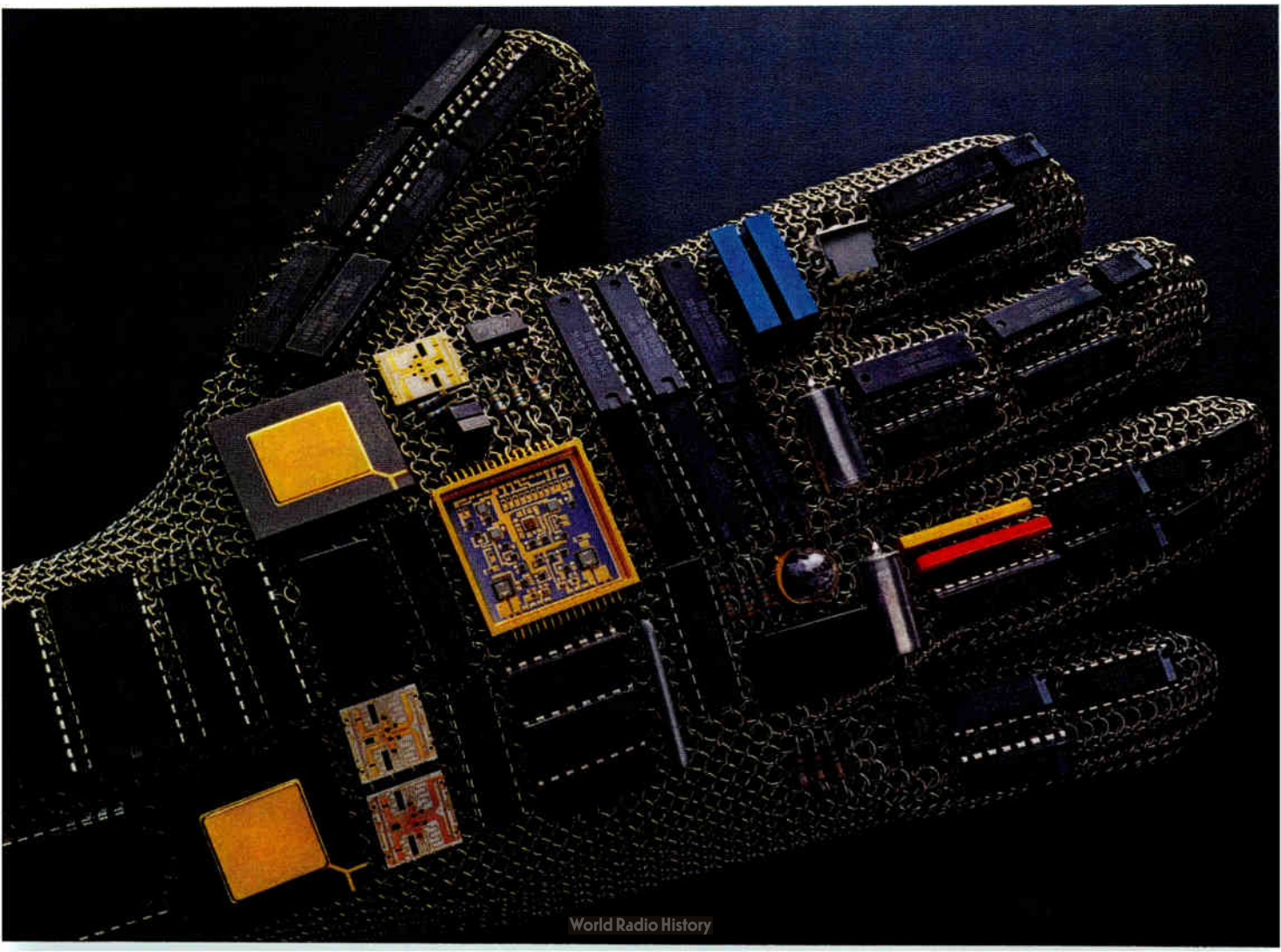
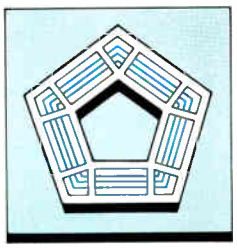




SELLING TO THE MILITARY: IS IT ABOUT TO GET EASIER?

A rash of bills before Congress threatens to fundamentally alter the business practices of defense suppliers, and a new undersecretary for acquisition at the Pentagon aims to make major cultural changes in procurement procedures

by Tobias Naegele

These are tough days in the defense business. Spending is down, competition is up, and government regulations are stringent. The burdens of paperwork, documentation, and multiple audits—the legacy of the public's furor over $640 toilet seats and $435 hammers—are forcing contractors to make ever-harder decisions. With fewer new programs to go around, companies are finding they must bid on more contracts than ever, just as preparing those bids is getting more expensive. It's a jungle out there.

And watch out: a slew of changes is in the works. In Congress, legislators are working on bills aimed at streamlining Pentagon management, stripping out waste, and limiting the profits contractors can earn (see figure). At the Pentagon, Robert B. Costello, the newly appointed undersecretary of defense for acquisition, is pushing for major changes in the way the Pentagon does business. In the middle of the fray are the defense contractors, worrying about an uncertain economic future and hoping to fend off legislative attacks on their bottom lines.

The bill that has defense companies most worried is the Defense Contractor Profits Act (HR 3134), which would require contractors to open up their financial books—for both government and non-government work—for review by federal auditors. The bill poses a serious threat to the well-being of any government contractor, says Dan Heinemeier, director of the Government Procurement Relations Council at the Electronic Industries Association in Washington. "Everybody agrees there's already too much oversight going on," he says. "We are concerned about a statutory mandate for profit reporting. It raises the issue of renegotiations."

Most contractors already consider auditing a major problem, says Seymour Zeiberg, vice president of research and technology at Martin Marietta Corp.'s Electronics and Missiles Group. "The amount of auditing, of looking over your books and processes and methods and operations in the factory, is enormous. It's too much."

Moreover, opening a company's books to the General Accounting Office will also open them up for Congres-

WHAT CONGRESS IS PROPOSING

Bill / Backer	Purpose	Potential Effects	Status
Defense Contractor Profits Act (HR 3134) Rep. Charles Bennett (D-Fla.)	• Establish a mandatory profit-reporting system through the Defense Contract Audit Agency • Provide a method of identifying excess profits in government contracts • Allow government access to contractors' business records for both government and non-government work	• Give Congress access to financial details of the non-government businesses of government contracts • Provide the Pentagon with more detailed information on profits • Improve the Pentagon's position when negotiating contracts • Cause some companies to reduce their level of government work to protect financial information	• Referred to the House Armed Services Committee • Hearings have not yet been scheduled
Defense and Industrial Base Improvement Act (being drafted) Sen. Jeff Bingaman (D-N.M.) Sen. Phil Gramm (R-Texas)	• Abolish cap on independent research and development • Require contractors' reward to be commensurate with risk • Provide uniform training for DOD procurement work force • Eliminate restrictions on multiyear procurement • Coordinate the audit process to eliminate duplication • Provide a uniform policy for indemnifying contractors against liability caused by acts or omissions of the government	• Improve the U.S. industrial and technological base by encouraging investment and innovation • Improve the business relationship between contractors and government by reducing audits and adding security with multiyear procurement contracts • Protect contractors from liability in cases such as the space shuttle Challenger, where equipment failures are the fault of the government and not the contractor	• None of the provisions has been endorsed yet by either senator, but aides for the Senate Subcommittee on Science and Technology hope to have a bill ready by July • The goal is to attach the measure to the fiscal 1989 appropriations bill in September

sional scrutiny, says a Congressional aide familiar with the bill, but he adds that a portion of it provides for confidentiality. The contractors aren't sure how confidential the audits might be, however. And they don't want Congressional investigators pointing, for example, to the difference in price between a commercial memory chip and a similar chip that meets military specifications, and asking why the latter costs so much more.

"Industry is opposed to any profit-reporting bill which would require the reporting of commercial profits," says Leroy J. Haugh, vice president of procurement and finance at the Aerospace Industries Association. "The intrusion of the government into contractors' business by requesting commercial profit data can only lead to further allegations that defense profits are too high. It's an apples-to-oranges comparison, and it's not valid."

Haugh says Congress should worry more about costs and less about profits, "which is only 10% of the pie." But killing the legislation will be tricky, he adds, because of the public's distrust of the defense industry. If the bill can survive the House Armed Services Committee, he says, it has a good chance of passing. "If this thing goes to the entire House, it's hard to imagine many people would oppose it. It's a motherhood issue," he says.

Another measure on the horizon is getting much more support from defense contractors. The Defense and Industrial Base Improvement Act, which is still in the draft stage, addresses a number of issues brought up in a report to the Senate Subcommittee on Defense Industry and Technology by an advisory group of industry executives representing such companies as Lockheed, Martin Marietta, and GE/RCA Aerospace and Defense. Among other things, the bill would protect contractors from undue risk in developing new systems, eliminate restrictions on multiyear procurement, and coordinate the auditing process to eliminate duplication of effort.

The measure is in its earliest stages now, and hasn't yet won the endorsement of any senator. The AIA supports most of the advisory group's recommendations, but isn't convinced new laws are needed. "This is an area where the less legislation we have, the better," Haugh says. "We don't need more legislation, except for legislation to correct for the overcorrections we saw in the last few years."

That's also a key issue for the Pentagon, which doesn't want Congress to impose any more legislative restrictions on the department. The DOD argues that such restraints will force it to do business only under rigid ground rules—making it harder for the Pentagon to reform its internal management. Undersecretary Costello, who is leading the effort toward those reforms, says, "It's obvious that most of our constraints are regulatory."

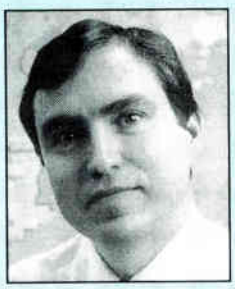
HOW THE DOD WILL CUT RED TAPE TO SPEED UP CHIP BUYING

The Defense Electronics Supply Center is radically changing the way the DOD buys and specifies chips, with new programs designed to boost quality, cut costs, and speed leading-edge technology into weapons systems.

It hopes to produce what Undersecretary of Defense for Acquisition Robert B. Costello calls "living specifications" that don't change with each technology advance. The ability to grow with technology, Costello hopes, will accelerate the often excrutiatingly slow process of getting leading-edge technology into military systems.

DESC is experimenting with so-called generic specifications; developing a new method of part certification to speed technology insertion; and giving more responsibility for certification to the manufacturer.

Generic specs qualify a manufacturer's process and fab line, rather than individual chip designs. They will most likely eventually become the prevailing military specification for integrated circuits. They already exist for hybrid circuits and gate array application-specific ICs [*Electronics*, Sept. 17, 1987, p. 32], and are being considered for standard-cell ASICs and possibly some very-large-scale integration chips, says L. Darrell Hill, chief of DESC's Qualifications Division. Meanwhile, DESC is looking at other ways to handle its microelectronics specs.



HILL

"We want to expedite the release of detailed performance mil specs [for individual parts], and we want to expedite and capture new technologies quicker," Hill says. Revised specs for military ICs came out this winter and revisions for passive chips are coming.

To accelerate the use of new designs, DESC is pushing the Performance Matrix, which "attacks the standardization process earlier than ever before," says DESC engineer Michael Frye. With the Performance Matrix, chip makers can supply DESC with performance characteristics early enough in the product cycle to produce a spec in three months to a year. Three years are needed now.

A related effort involves the standard military drawing, which DESC seeks as a replacement for source-code drawings. They are custom-made military specs written for parts for which a mil spec doesn't exist. Each source-code drawing (or SCD) costs the DOD roughly $8,000; 400 or more SCDs have been known to describe the very same part, says Steven Searcy, chief of the Circuits Division at DESC.

The standard military drawing (or SMD), on the other hand, is a document shared among contractors as a sort of temporary mil spec for all vendors. But critics say it takes too long for the documents to be produced. "If the SMD program was working properly and we were getting part numbers issued on a real-time basis, the need for SCDs would be eliminated," says Gary Cohrt, director and general manager of the government products division at VLSI Technology Corp. "We continue to issue an extraordinary number of SCDs."

Cohrt says change won't come easily. "We need less of the DOD telling us how to do things," he says. "Tell us what you want—and we'll do it."

That's just what the DOD wants, Hill says. The revised specs "will provide us with substantial savings, but it's also going to place a lot more of the burden where it belongs—on the manufacturers. We're not going to hold their hands." *–T.S.N.*

Costello took over as the DOD's acquisition czar last September. He is attempting, in effect, to make a major cultural change in the DOD by streamlining procurement practices, bypassing unnecessary regulations, and aggressively seeking out waste. His goal is to cut costs by at least 20% over the next five years by eliminating cumbersome extra layers of management and reducing the paper work involved with military specifications.

But, Costello says, "we need a stable environment in order to do all these things." The ongoing legislative upheaval over defense budgets and procurement regulations will only hinder the streamlining process, he believes; most of the reforms he wants can be handled internally, through directives and policy changes.

Among the changes Costello is seeking are reforms based on the notion of a "living specification," one that does not need to be changed every time technology advances by a small step. He applauds the work in this area being done at the Defense Electronics Supply Center, in Dayton, Ohio (see panel, left). Similarly, he says, the Pentagon needs living regulations and policies that don't require acts of Congress every time the economic winds change direction.

Whether Costello can institute enough of a change to survive the end of the Reagan presidency is open to question. "I don't know how far he's going to get, because it's the last year of this administration," says a legislative aide for the House Armed Services Committee. "Nobody has much expectation. What we're looking for is a change in attitude and mindset. We don't think that can happen in the last year of an administration."

Costello, however, thinks that by acting decisively and quickly, he can set in motion the kinds of changes the Pentagon needs. "We are putting in place demonstration and pilot programs to test our ideas now," he says, referring to the 36 efforts going on under his Pilot Contracting Activities Program, among them DESC's Quality Vendor Program (see panel, right). "Are you going to go back to those people 12 months from now and tell them to stop? You'll have a riot on your hands."

For contractors, Costello's streamlining initiative is of great importance. His aim is to broadly institute what he calls the "could cost" concept. In practice, the concept involves eliminating everything the Pentagon and contractors do that adds cost but no value to a product the DOD is buying. It means less concentration on end-of-the-line testing and more on in-line process controls. The intention is to ensure that a quality product comes off a production line and to catch small problems before they become major ones later on in the manufacturing process.

Defense systems companies are excited by the effort because it addresses what they see as their biggest problem: paperwork. The detail required to bid on military contracts is out of line with what is really needed, says Allan F. Beaupre, vice president and general manager at Harris Corp.'s Government Communications Systems Division. "When we're writing proposals, there are requirements for us to get competitive price quotes for all the materials and components we'll use," he says. "Price quotes are generally short, 60 or 90 days. Looking at quotes for every screw gets to be too expensive." By the time the Pentagon awards a contract, it often has to be renegotiated because the deadline has come and gone, and parts prices may have changed. To help minimize the extra work, Harris is trying to sign long-term agreements with suppliers of commonly used components.

That's fine with Costello. Part of his goal is to get the contractors, as well as the DOD program managers, thinking about ways to cut costs. Recent legislation, he notes, helped create an adversarial relationship between contractors and the DOD that has been counterproductive. The two need to work together to solve their problems. EIA's Heinemeier agrees: "It's a balancing act—you need a good arm's-length business relationship. You need a partnership." □

BIDDING LOW IS NOW ONLY PART OF WINNING

Military contracts are traditionally awarded on a simple price basis: the lowest bidder wins. But as the Defense Department struggles to keep its costs down, it's looking to adopt commercial buying practices that take delivery and quality into account. Leading the way is the Defense Electronics Supply Center, which spends over $600 million on 160,000 contracts every year.

DESC's Quality Vendor Program, one of 36 pilot contracting activities sponsored by the Office of the Secretary of Defense, lets the agency award contracts to certified suppliers even if their bids are 20% higher than the lowest competitor.

Gathering enough industry support for the program may take some time, however. DESC invited 5,000 companies last summer to apply for certification in five areas: communications equipment, discrete semiconductors, integrated circuits, antennas and waveguides, and synchros and resolvers.

But only 144 companies responded in writing, and fewer than half of those followed through with full-scale applications. When the list of qualified companies was released in mid-March, only 18 companies were included on it [*Electronics*, Mar. 17, 1988, p. 139]. Of those 18 companies, however, three were qualified in more than one category.

Companies were required to document their quality and delivery history in detail for the prior 12 months. To qualify, they had to meet very strict standards: no more than one major defect in every 200 parts, no more than one minor defect in every 100 parts, and an on-time delivery rate of at least 90%.

DESC will review the performance of quality vendors every six months. If their deliveries slip or their defect rates climb, they'll be dropped from the list. "Regulations got so tight it was putting a stranglehold on the acquisition process," says Col. Louis Diel, director of contracting and production at DESC. "Rather than all the negative restrictions and punishments we've imposed in the past, this is a positive incentive." *–T.S.N.*

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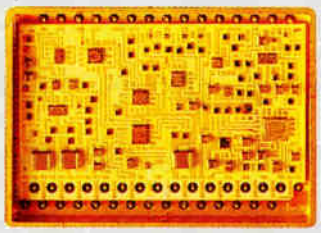

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TI FINDS A NEW WAY TO PREDICT PACKAGE RELIABILITY

Computer modeling can estimate the reliability of IC package designs and show the predictions graphically

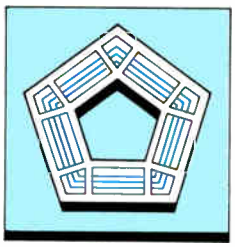
Computer-based modeling is radically changing the way Texas Instruments Inc. deals with the thorny problems of integrated-circuit package design. The technique, a modification of the Finite Element Analysis used widely in mechanical-engineering stress modeling, can quantify and graphically reveal the effects of materials, form factors, and processing methods on IC packages. So far, the Dallas-based company has achieved excellent correlation between model predictions and observed device failures.

Using the technique as a computer-aided-design tool, a semiconductor packaging engineer can characterize stresses and deformation throughout a package for any type of mechanical or thermal load. This data eliminates the trial-and-error approach to the experimental analysis and design of IC packages. Computer modeling is also much faster and cheaper than constructing and modifying physical samples.

The development of Finite Element Analysis modeling is directly linked to the growth of VLSI high-density semiconductor technology, which not only demands fine geometries but also requires the housing of very large chips in ever smaller packages, says Walter Schroen, a TI Fellow and department head of semiconductor packaging. What's more, he says, since many more functions must be accommodated inside new VLSI packages or housings, designers must be even more confident that the housing can be depended upon to prevent catastrophic system failures, especially in unmanned aerospace equipment where replacement of ICs is impossible. Because they are often subjected to the most severe operational and storage environments, high-reliability military and aerospace ICs are especially in need of efficient packaging.

Without the proper packaging, even the best product can fail. That's because package design is a key factor in device reliability (see fig. 1). The effect of stresses on devices is reflected in their mechanical integrity, electrical characteristics, or both. A poor package and leadframe design can often result in the accumulation of corrosion-causing moisture on a chip's surface. Moreover, improper packaging design can cause slower switching speed and an insufficient surface area for heat dissipation. A poor packaging process can also lead to failures through lead breakage and bending or decreased lead pull strengths. Accurate modeling of potentially destructive mechanical and thermal stresses offers enhanced electrical reliability for both ICs and their packages. By devising models upon which to simulate the effects of stress on a device's critical structural elements—materials, leadframes, oxides, metallization, and overcoats—manufacturing processes can be designed to reduce stress at sensitive points, minimizing IC failures.

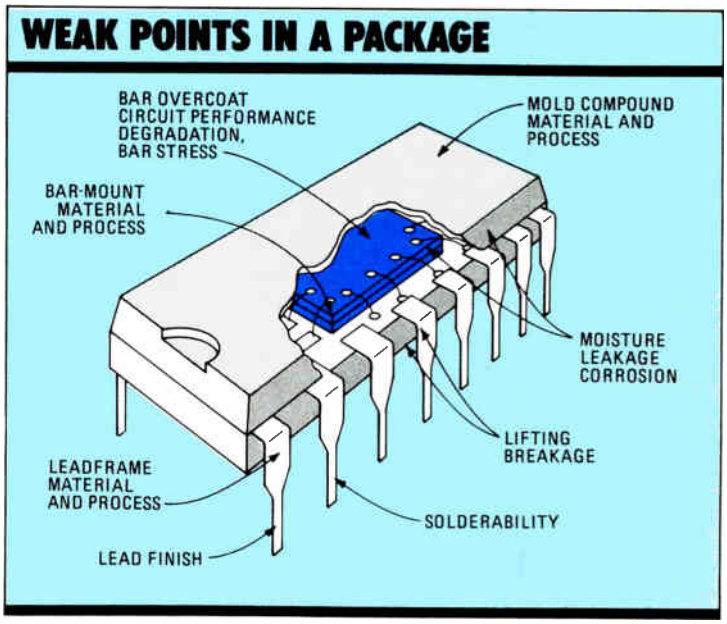
Finite Element Analysis demonstrates the importance of understanding exactly where and why excessive stresses occur in an IC package. If the analysis indicates strengthening a structurally weak package by increasing its thickness, the packaging designer must realize that such a course can result in greater thermal stresses. Thermal stresses, on the other hand, change over time and with environmental conditions. The stress magnitudes predicted by the model under analysis may not agree with actual magnitudes, but the shape of the distribution and relative magnitudes have proven to be accurate.



Because high-speed computers are a necessary adjunct to the successful implementation of computational-intensive Finite Element Analysis routines, the work is performed on 32-bit Apollo work stations. The analysis requires a numerical description of a shape's geometry. An equation must be written in the computer program for each degree of freedom at each node.

The number of equations is determined by the number of nodes. A two-dimensional model of an IC package can generate 3,000 equations, so the computer must be able to handle a matrix of 9 million terms. If the model is expanded to three dimensions, 10,000 equations and 100 million terms are needed. Fortunately, most model problems can be broken down to fit on the Apollo machines using matrix partitioning or substructuring.

Finite Element Analysis works by dividing a physical structure into a large number of small elements. Elements are interconnected at a discrete number of nodal points that describe the geometry. A set of mathematical operations embodied in a computer pro-

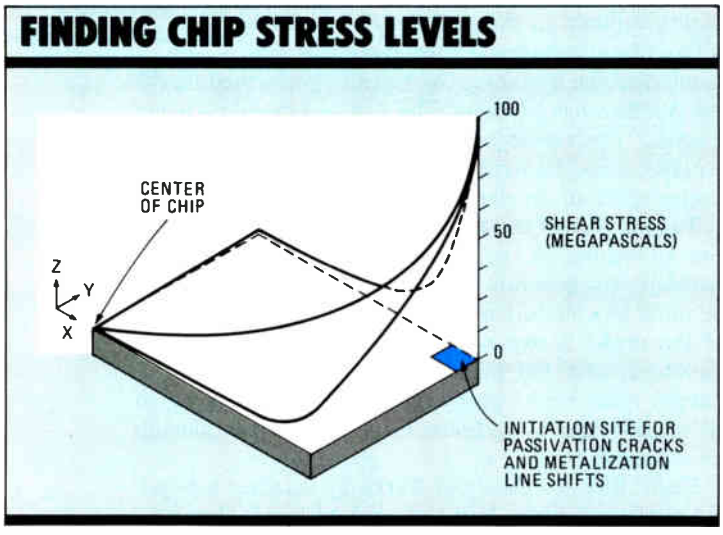


1. The IC chip/package combination has many mechanical, material, and thermal factors that can cause device failure or degradation.

gram allows a piece-wise approximation to the mechanical equations governing equilibrium. The basic premise of the process is that a solution to a set of equations can be approximated analytically by replacing the set with an array of discrete elements.

A structure such as an IC package can be modeled by dividing it into a large number of small elements tied together at a number of common points and superimposing that physical geometry on a coordinate grid system. After the grid is established, coordinate values of the element corners are identified. The values are arranged according to a prescribed formula into a strain or B matrix for each element. This matrix is defined as the proportionality constant between the strain and displacement vectors.

A second matrix called the elasticity or D matrix is defined from the elastic properties of the package materials. This matrix is the proportionality constant between the stress and strain vectors. When both matrices are established, a set of matrix operations transforms the B and D matrices into a third or stiffness matrix (called K). A number of K-matrices are assembled into what is called a master stiffness matrix for the IC package.



2. A 3-d model reveals chip stresses not shown in a simpler 2-d model. The chip corner has an especially high-stress level.

At this point, the effects of temperature on strain must be considered. Specific elements within the K matrix are combined with the applied thermal load to reveal displacements (strains) imposed by the load. The displacements indicate thermal stress as calculated by Hooke's Law.

Testing a model undergoing Finite Element Analysis against a theoretical prediction verifies only that the model—not the actual physical world—agrees with theory. The model must, then, be shown to conform to physical reality. To prove this, TI designers prepare test chips that contain diffused strain-gauge test structures or sensors based on the property of semiconductors to exhibit a measurable piezoresistance effect under strain (resistance changes with strain). Since the sensors generate quantitative resistance values, measurements can be taken from various locations on a chip and compared with the model predictions. The correlation between measurements and model predictions often turns out to be very close.

This process allows VLSI package designers to see many stress-related failure mechanisms that they would not be aware of using conventional methods. For VLSI devices having large silicon chips with elaborate surface structures, Finite Element Anaylsis can establish package design rules.

For example, a three-dimensional model has been developed by TI designers to verify the assumption that relatively high stress concentrations occur at various locations over the cross-section of a device. Initially, the device was modeled using two-dimensional analysis, showing stress contours in the area of the chip edge and lead attachment.

After analyzing the stress contours of several types of leadframe arrangements, the TI design team discovered that none of them offered any apparent advantages in relieving stress. The three-dimensional model was then generated to gain further insight into the stress problem.

Shear stress parallel to the chip's surface reaches a maximum at the corners and decreases to zero at the center (see fig. 2). The intense concentration of stress within 0.4 mm of the chip's corner (at least 50 MegaPascals) explains potential failures such as passivation cracks, metal line shifts, and sheared ball bonds.

Since the shear stress immediately above the chip surface is highly concentrated—and within fractions of a millimeter of the corner—any bond or soft metallization in this neighborhood can be placed only with caution. For example, if the metallization becomes too ductile and yields when subjected to small strains, the passivation is left unsupported, or only partially supported, and may crack.

Finite Element Analysis modeling can also determine how tight assembly and packaging processes must be to ensure packaging integrity. Cracks in the housing material covering the silicon chip can result if the overhang distance between the chip and its leadframe pads are too short. Repetitive modeling of the distance can predict the optimum chip placement control required in production. For example, analysis revealed that, in one case, a pad overhang of 5 mils can relieve the dangerous stress concentration that builds up when the overhang is only 1 mil.

But correct leadframe packaging alone is only half the battle. "Stress distribution alone is not sufficient data to evaluate a package design," Schroen says. "A packaging designer must understand that the strength of various materials determines whether a material can withstand a specific stress state." The modified Coulomb-Mohr theory of brittle failure can be applied at the output of models to define a "safety" number N based on the material's tensile strength T and compressive strength C.

The safety number for an element of the model is calculated from the sign and magnitude of the maximum and minimum stresses at the element. A safety number equal to or greater than 1 identifies a material that will be less susceptible to brittle fracture than a material whose number is less than 1.–*Jerry Lyman*

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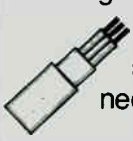

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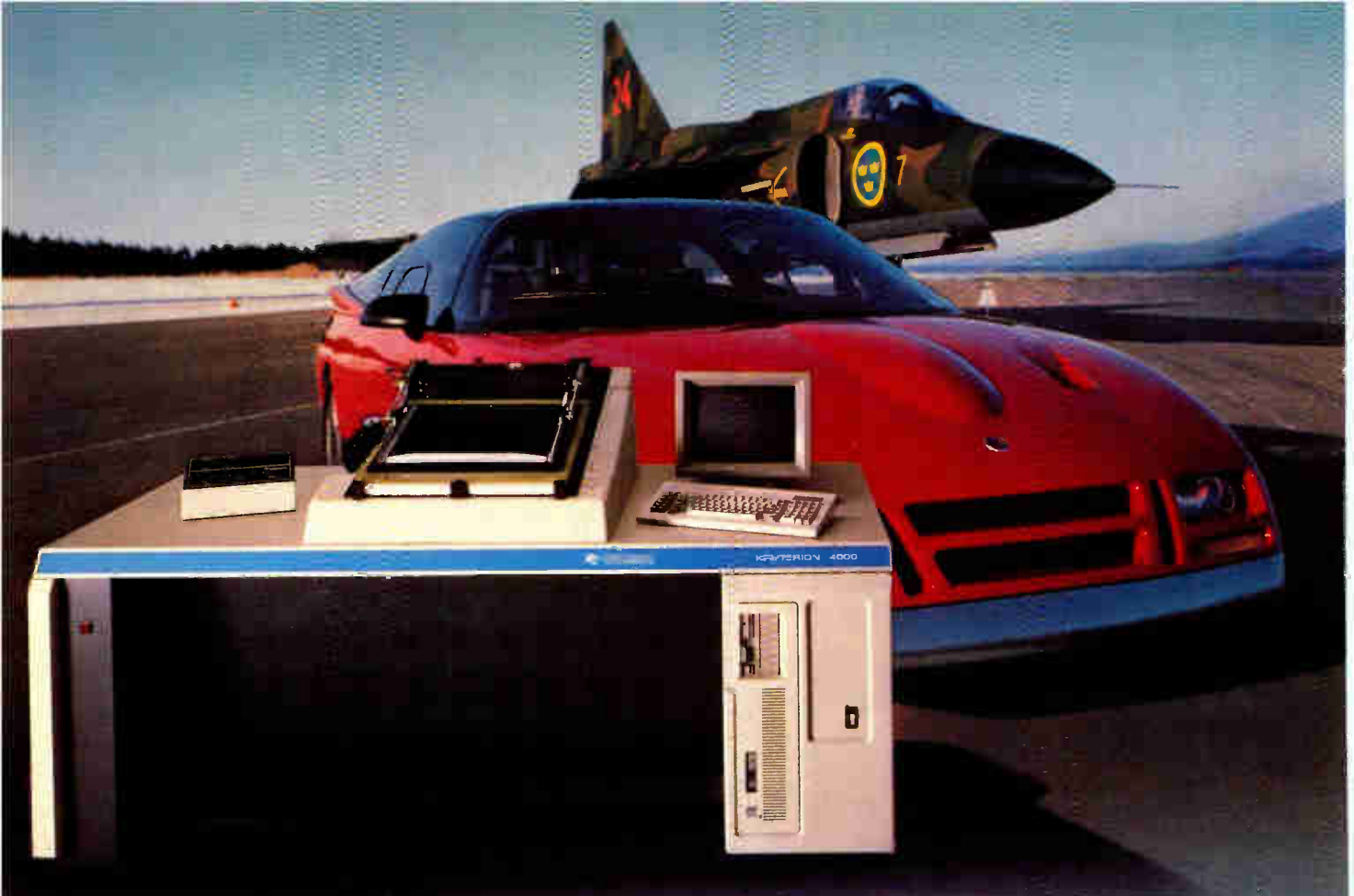

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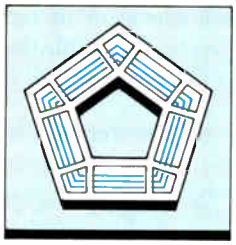


AN EASY WAY TO MAKE POWER HYBRIDS: BUILDING BLOCKS

Omnirel's family of standard metal packages and circuit modules is an alternative to custom design

Custom circuitry is no longer the only game in town for users of power hybrids. Omnirel Corp. is launching a family of standard metal packages and circuit modules that considerably simplify the job of designing and assembling a power hybrid. Because these new units (see fig. 1) provide standard building blocks for power hybrids, they cut the time and expense of a complex in-house design effort or of ordering a custom hybrid from an outside source. They'll be particularly useful for military applications, where many power hybrid designs are used.

The new packages are one-for-one equivalents of standard plastic packages, so they sport familiar form factors. They allow Omnirel to put combinations of power semiconductors into small, hermetically sealed, thermally efficient thick-film modules. The Leominster, Mass., company is also selling packages to Motorola Inc. for a line of power MOS FETs (see p. 26).

Omnirel also is going a step further with the OM 9015FS module that adds control circuitry to the power semiconductor circuitry, making it practically a complete power supply. With the simple addition of a few passive and active components to this module, a user can quickly assemble a complete supply—a high-power, pulse-width-modulated, push-pull dc-to-dc converter that meets military specifications.

Power hybrids, consisting of power semiconductor and integrated circuits wire-bonded to a thick-film pattern on a ceramic substrate with a high thermal conductivity, are one of the best ways for a designer to meet the military's demands for reduced size and weight, and increased power density for high-power circuitry such as supplies and motor controllers. However, the technology needed to produce a power hybrid is quite different from that of a conventional hybrid, particularly in the areas of the thermal, mechanical, and electrical properties required for a power hybrid's package, substrate, wire bonds, and solder attach. As a result, design, assembly, and production of power hybrids is a complex, costly, and time-consuming process requiring an expertise beyond the capabilities of most electronic firms and even of the great majority of the suppliers of thick-film hybrids.

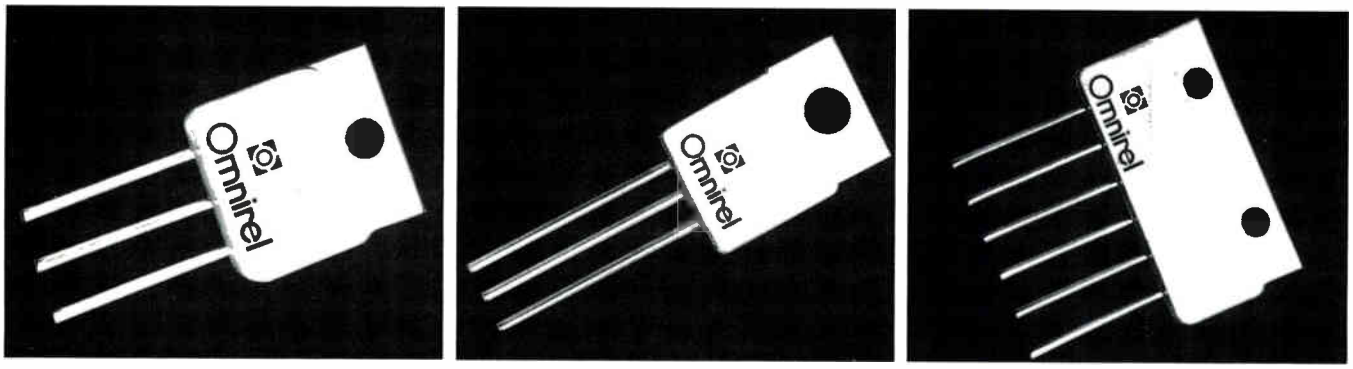
Ordinarily, to meet the military's tight specifications, a designer has three choices: discrete power devices, smart power devices, or thick-film hybrids. For most high power-density applications, packaged discrete power devices are simply too large. At the present time, smart-power devices (monolithic integration of low-power logic and medium-power components on a single chip) can provide output power levels up to 50 W in some applications. Beyond that, the real-estate requirements of the output power transistor and rectifiers are so great that they make further integration uneconomical. The power hybrid has neither the power nor the real-estate limitations of smart-power devices. In addition, the hybrid power approach can accommodate any number of useful nonchip components to achieve optimum performance.

A key goal for Omnirel was the design of a standard series of packages that can be used in a variety of power-hybrid applications. Most power-hybrid packages today are custom designed to fit the users' requirements. The exception is some low-density hybrids that fit into T0-3 and T0-66 metal packages with forms which are undesirable for high density packaging and are fairly inefficient in space utilization. Their main attractions are cost and availability.

Omnirel's new family of power packages are hermetic-metal packages with the same dimensions as standard plastic packages: T0-220, T0-218, T0-247, and single in-line and dual in-line packages. They are easy to mount and have been designed for the thermal, mechanical, and electrical characteristics of power hybrids.

The new hybrid packages can carry currents of up to 50 A steady state and 500 A pulsed and can dissipate up to 500 W steady state (1 kW pulsed). To do this, they use copper or copper-cored pins 60 mils in diameter, thick-film substrate metallization, and 20-mil-diameter aluminum wires for interconnection.

The power rating of a power hybrid module is di-



1. Omnirel's new family of hermetic metal packages are one-for-one replacements for such standard plastic packages as the TO-220, TO-247, and SIP.

rectly related to its thermal impedance and its ability to withstand thermal fatigue during its operating life. The critical parameters in thermal impedance are the thermal conductivity and thermal capacity of the substrate, the dice and substrate attach materials, and the package.

The substrate material chosen for Omnirel's new modules is beryllium oxide, which has a thermal conductivity of 2.5 W/cm/°C. In the future, substrates of aluminum nitride (2 W/cm/°C) may be used. The attach material for the modules' power chips is solder chosen for low thermal resistance as well as for high resistance to thermal fatigue. For the smaller (lower-power) packages, copper has been chosen as the package material since it provides the lowest thermal resistance because of its high thermal conductivity (3.9 W/cm/°C), and is the most cost-effective. However, from a thermal fatigue viewpoint, the high thermal coefficient of expansion of copper requires special attention in choosing the right substrate attach material and substrate size. So for higher power packages, Omnirel is using a compromise materials like molybdenum (1.5 W/cm/°C) or molybdenum-copper laminate (1.8 W/cm/°C).

HYBRIDS FOR ALL OCCASIONS

With the introduction of Omnirel's wide array of standard power packages, producing standard and custom power hybrid circuit modules for a broad range of applications is achievable. These hybrids can be more cost-effective because of larger production volume and ultimately more reliable through the use of fixed processes. Different standard hybrid blocks can encompass a number of standard switching power-supply topologies, some of which are shown in fig. 2.

In the flyback converter of fig. 2a, a hybrid circuit consisting of a power MOS FET, zener-diode gate protection, and the output Schottky high-efficiency rectifier has been assembled in the SIP of fig. 1. This hybrid greatly reduces the board space consumed by a discrete TO-3 package, and axial leaded diode.

A forward converter topology (fig. 2b) can be built up by using a MOS FET-zener hermetic module and a center-tapped Schottky module. These two assemblies are presently available in TO-247 packages and would again reduce overall board space when compared with two TO-3 assemblies. The push-pull converter of fig. 2c is the same as the forward converter, but with the addition of one more TO-247 containing a power MOS FET and a zener diode.

A further reduction in the size of a power supply can be realized by combining logic and power functions in a hybrid module. And Omnirel has done just this in a voltage-mode-control power supply module that will be available in the first quarter of this year. Basically, the circuit consists of a 1525A pulse-width modulator, two 2N6770 MOS FETs, an LM158 feedback amplifier, two 2N6391 Schottky diodes, and associated resistors, capacitors, inductors, and small-signal transistors, diodes, and zeners.

This circuit is a basic building block of the power supply industry and is referred to as a pwm push-pull dc-to-dc converter. This supply usually operates from a dc input (18 to 36 V) and provides an output of 5 V at 10 A. The pwm control and MOS drive circuit on the primary side of the power supply will serve as a standard hybrid circuit component for voltage-mode-control power supplies.

In Omnirel's new module, the circuitry is partitioned into logic and power subassemblies allowing for the high-dissipation components (MOS transistors) to be fabricated on BeO, and the logic section on aluminum oxide, the typical substrate for a low-level hybrid. This procedure provides for good thermal and electrical isolations of power and logic—a feature that is not readily achieved in smart power technology. The result is a reduction of noise coupling from the power switches to the logic section and the elimination of difficult board assemblies.

In the actual assembly, the BeO and Al_2O_3 substrates are 2.9 cm^2 and 3.7 cm^2, respectively. The theoretical junction temperature rise for the power substrate is only 15°C above case temperature for a 5-V 10-A power supply. A 2.5-by-5.0-by-1.0-cm 16-pin molybdenum power package was chosen to house the circuit. The module's operating temperature range is from −55°C to +150°C. *—Jerry Lyman*

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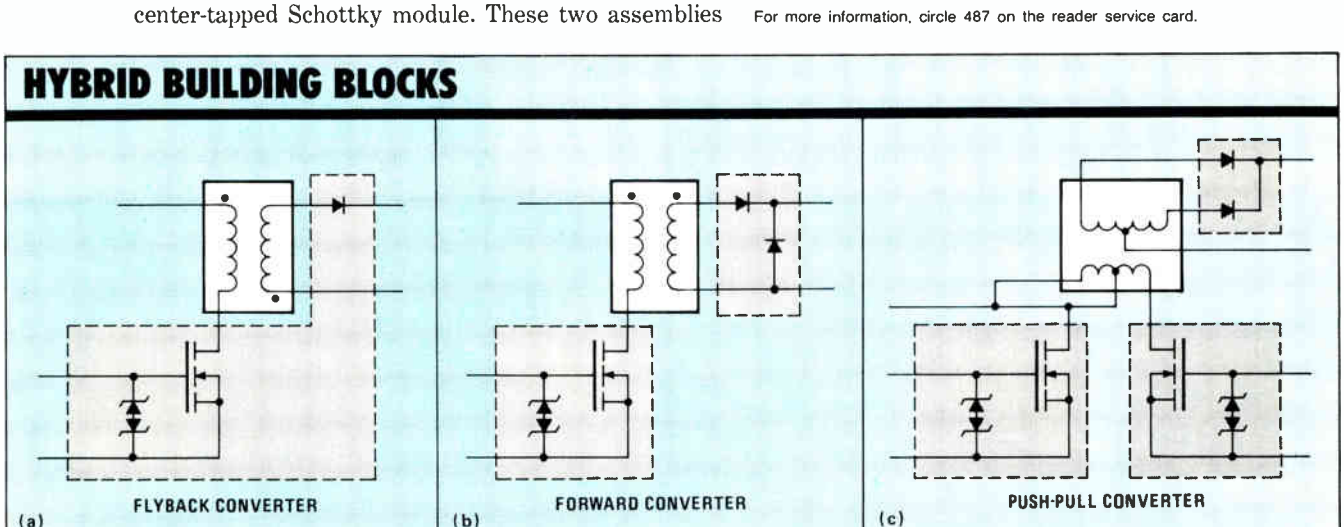
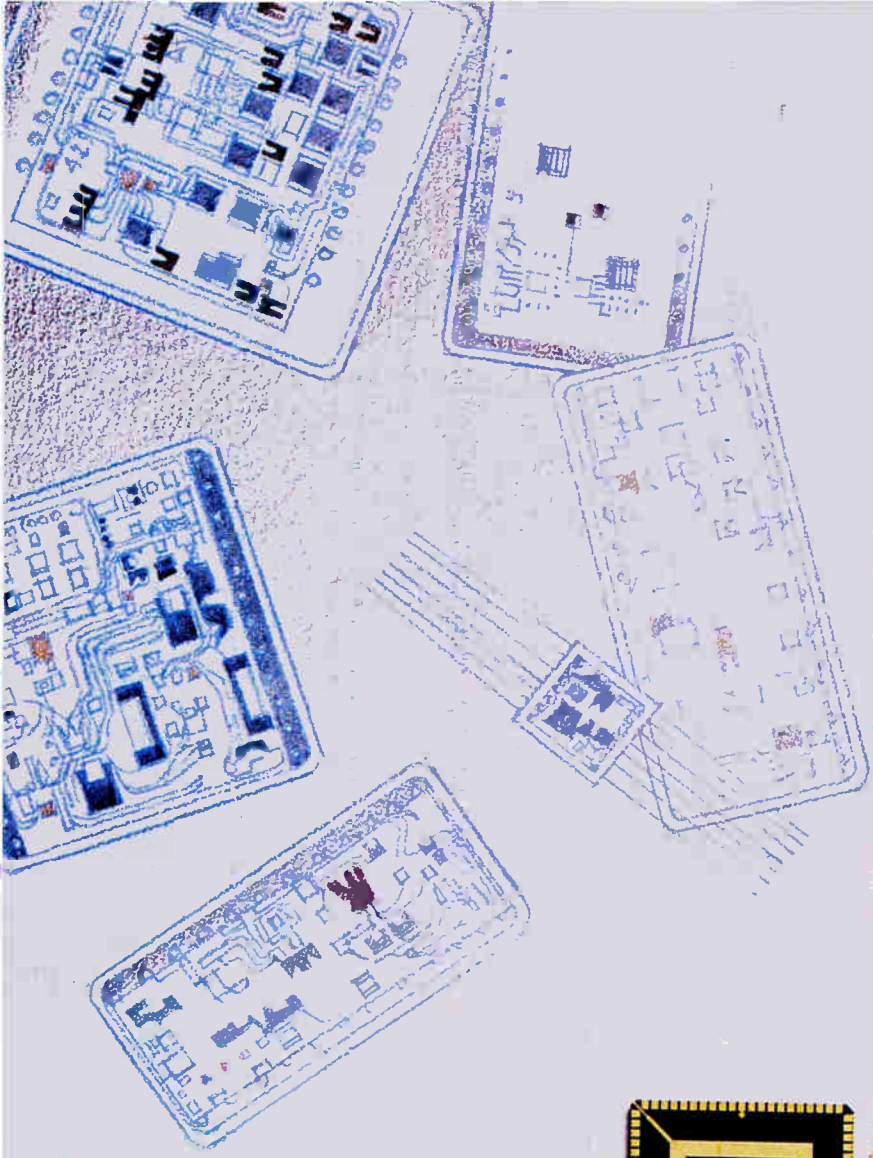


2. With the new packages, Omnirel can offer hybrid units that replace discrete implementations of standard switching-power-supply circuitry.



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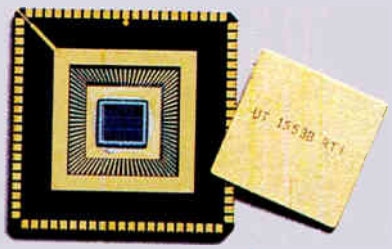

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MILITARY/AEROSPACE NEWSLETTER

HONEYWELL: BiCMOS WON'T MAKE IT AS A MILITARY TECHNOLOGY

BiCMOS may be emerging as one of the hottest new process technologies for high-speed and low-power commercial integrated circuits, but Honeywell Inc. believes the technology won't be needed in the military chip business. "We've chosen not to continue to invest in biCMOS technology," says David Wick, ASIC product line manager at Honeywell's Solid State Electronics Division, in Colorado Springs, Colo. "Honeywell is focused primarily on the military, where system performance hasn't moved up enough to require a biCMOS technology now. And when it does, we'll be able to satisfy the requirement with submicron CMOS," Wick explains. "Our studies have shown that when you get down to below 1 μm, the intrinsic advantage of biCMOS disappears." Honeywell is in production on 1-μm CMOS gate arrays and expects to introduce products based on 0.5-μm CMOS in late 1989. □

DEFENSE SUPPLIERS MAY FACE REDUCED PROFITS

Defense contractors will borrow more money and end up with vastly reduced returns on investment in the next several years, thanks to piecemeal changes in the way the Defense Department buys goods and services, says a new study made for the Aerospace and Electronics Industries associations and the National Security Industrial Association. The report, prepared by The Mac Group, a Washington consulting firm, predicts sharp reductions in company profits in the early 1990s resulting in decreased private funding for research and development and a smaller, less-competitive defense industry. Electronics companies may be the first to feel the squeeze. "I don't see any relief in sight," says Dan Heinemeier, director of the Government Procurement Relations Council at the EIA in Washington. "It's going to be a lean few years." The Mac Group says financial hard times will impact subcontractors first. "They're going to be most affected because they're small companies," says Mac Group analyst Russell Aney. "They don't have the diversity the larger companies have. They work on a shorter-term basis. And there's a good chance that some of these are going to fall off the face of the earth." □

VITESSE WILL SUPPLY GaAs STATIC RAMs TO SUPPORT DARPA's 32-BIT GaAs PROCESSOR

Vitesse Semiconductor Corp. of Camarillo, Calif., will supply 16-Kbit gallium arsenide static random-access memories for the Defense Advance Research Projects Agency's GaAs microprocessor effort. The memories were designed for high-speed computer-cache-memory applications and use Vitesse's enhancement/depletion mode transistor technology. Darpa is funding an effort to develop a 32-bit GaAs microprocessor capable of running 200 million instructions/s [*Electronics*, Oct. 1, 1987, p. 93], and the Vitesse parts will be used in support of early prototypes of those parts. Vitesse will deliver the SRAMs in May to Texas Instruments Inc. and McDonnell Douglas Corp., which are each developing microprocessors under the Darpa program. □

THESE SOFTWARE PROGRAMS HELP MANAGE MILITARY CONTRACTS

With all the paperwork and detail required to handle a military contract, Mainstay Software Corp. has come up with a pair of software packages that it says answers the prayers of every military product manager: two programs for cost and schedule analysis. Mainstay CPR, for Cost Performance Report, and C/SSR, for Cost/Schedule Status Report, provide cost performance analysts with analysis tools that run on IBM Corp. Personal Computers and compatibles and can be licensed for as little as $1,000 per year. The programs let users plot information on over 20 types of graphs within six categories to get up-to-date data on a program's status. □

MILITARY/AEROSPACE NEWSLETTER

TERMINATING AN ACCIDENTAL MISSILE LAUNCH: A NEW USE FOR SDI?

The Strategic Defense Initiative Organization is studying the feasibility of developing an added capability for President Reagan's Star Wars missile defense shield—the ability to knock down an accidentally launched missile. Speaking before the House Subcommittee on Research and Development on March 16, SDIO director Lt. Gen. James A. Abrahamson said initial results will be available this spring and summer. Although he did not disclose what options are under consideration, Abrahamson did say that several alternative architectures are being considered. The idea of developing a system to abort accidental launches comes in response to suggestions made by Sen. Sam Nunn (D-Ga.), chairman of the Senate Armed Services Committee, and a number of other senators and science policy advisors, Abrahamson said. Current studies are looking at the cost, practicality, and effectiveness of accidental-launch options, especially as they relate to their compatibility with the so-called Phase 1 architecture, which includes space-based surveillance and tracking systems and a space-based interceptor. □

NASA AIMS TO FILL THE GAPS IN ITS TECHNOLOGY BASE...

The National Aeronautics and Space Administration is aiming to "redress gaps in the technology base" with several nonmilitary development efforts. Joseph Alexander, NASA's assistant associate administrator for space science applications, says NASA's Pathfinder program will begin in 1989 if it gets the $100 million NASA is seeking. The program aims to develop a range of technologies, including optical communications, a planetary rover, space nuclear power, and equipment that will allow in-space assembly and construction of space-based equipment. "If one looks at what we aim to do in the 21st century with the space station, there are a lot of technologies that will be required that simply don't exist today," Alexander says. NASA is spending $115.2 million its Civil Space Technology program in 1988, and is asking for an increase in 1989 to $156.8 million. Most of that growth will be in the propulsion area, where NASA is looking to develop new Earth-to-orbit and booster rockets, but the initiative will also address high-capacity power systems, robotics, and sensor technology. □

...AS IT GEARS UP THE NEXT GENERATION OF SPACE-SCIENCE PROJECTS

The space-science projects now under way at the National Aeronautics and Space Administration will all be completed by 1993, and NASA officials are hurrying to prepare for the next wave. Beginning in 1989, NASA plans to launch at least one small-scale experiment per year, using a small new rocket known as Scout. The compact launcher will carry only "technically mature" experiments "in traditional science disciplines," such as astronomy, physics, and geology, says Joseph Alexander, NASA's assistant associate administrator for space science applications. A request for proposals for experiments is expected in April. Other planned science-oriented schemes include the Advanced X-Ray Astrophysics Facility, a $1.5 billion X-ray telescope project set to begin in 1989 with $27 million in start-up funding; the Mariner Mark II space explorer, which won't begin in full scale until 1990, but is still budgeted to get $15 million in 1989; and the Earth Observing System, aimed at deploying an automated space-based observatory, which won't begin in earnest until 1991, although NASA is seeking $15 million for the early stages of the program in 1989. "The space-science program that we're working on today will be completed by 1993," says Alexander, referring to the advanced programs that are already under way. "We have to look now at what we are doing in the second half of the 1990s, because if we don't, we won't have a program to speak of." □

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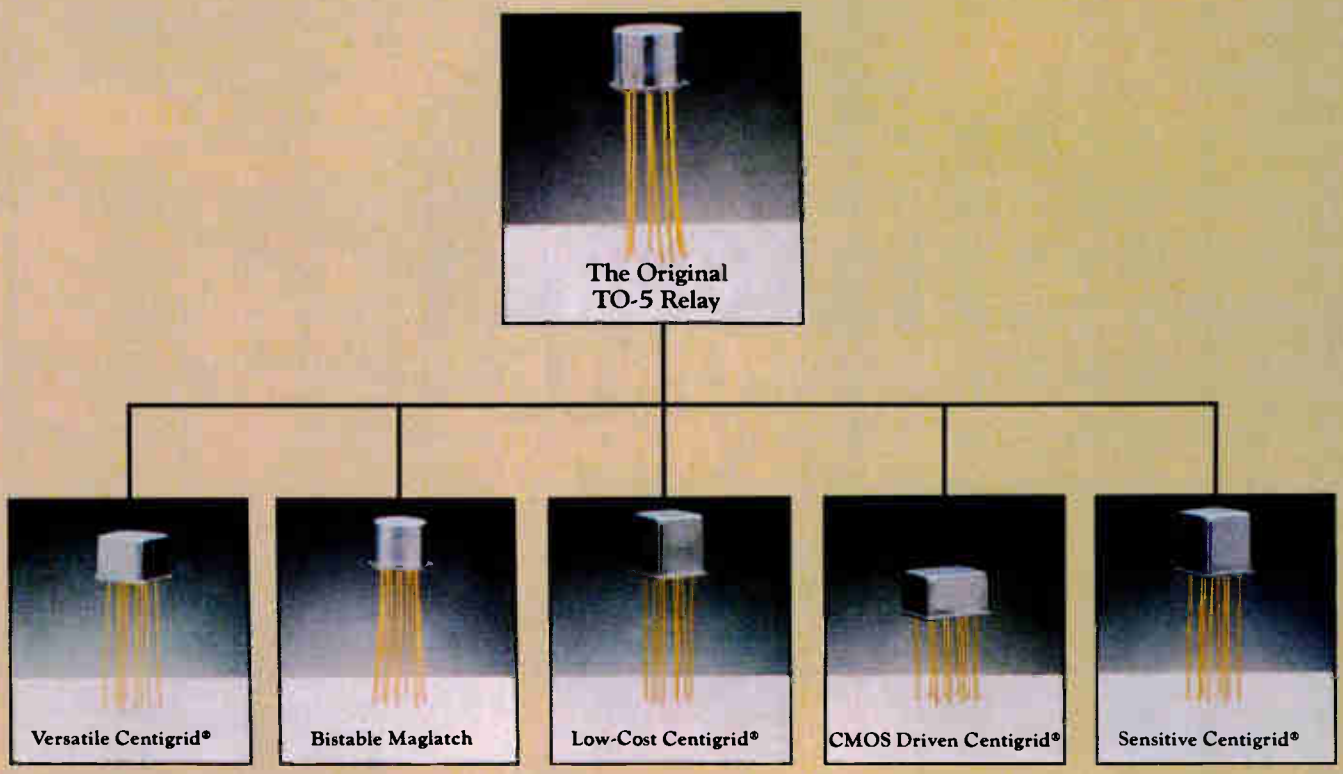

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Circle 98 on reader service card

NEW PRODUCTS

IC DRIVERS FOR LCDS BOOST VOLTAGE THREEFOLD FOR BRIGHTER DISPLAY

Micrel's MIC8031 for dichroic displays weds 5-V CMOS logic and 100-V DMOS power

Micrel Inc.'s integrated-circuit driver for dichroic liquid-crystal displays overcomes the high-voltage limitations of CMOS that have barred dichroic technology from producing bright, sharp images. The MIC8031 achieves this performance by integrating 5-V logic with diffused metal-oxide semiconductor (DMOS) 100-V push-pull outputs—three times the voltage of existing dichroic LCD drivers that depend on CMOS drivers.

The high output voltage sharpens LCD images, increases viewing angles, and—because it does not have to run at peak power limits—boosts reliability. These are all essential assets for military, avionic, and industrial displays.

Until now, engineers who wanted to design in dichroic LCDs have been limited to power IC drivers of about 32 V—that's the upper end of what can be done with standard CMOS processing, says Marvin Vander Kooi, director of power CMOS applications at the Sunnyvale, Calif., company.

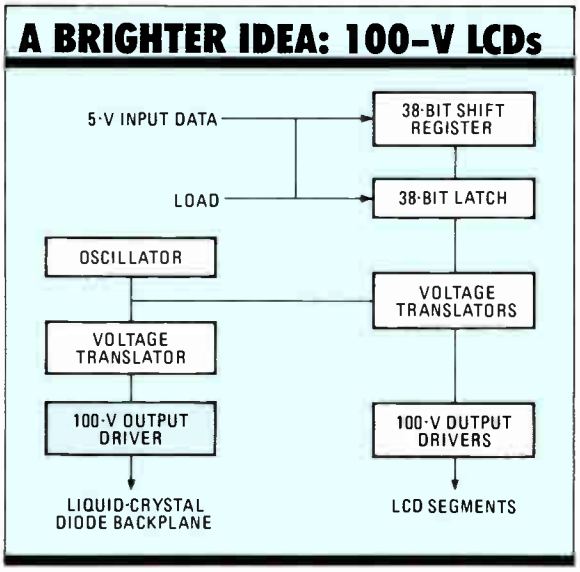
Micrel boosted driver output to 100 V by using a proprietary, 17-mask-layer CMOS/DMOS process that allowed its engineers to pack analog circuits and 5-V CMOS logic close to the high-voltage, 100-V vertical DMOS drivers without cross-talk—and to do it all on a 190-by-192-mil die.

FASTER. Dichroic LCD displays are superior to current LCD technology in battery-operated consumer products such as watches and calculators because they operate faster at low temperatures and boast both better contrast and wider viewing angles.

In addition to LCD displays, the processor can drive flat panels based on plasma, vacuum fluorescent, and ac or dc electroluminescent technology. "Because the 8031 is fundamentally a push-pull 100-V driver IC with latches and a shift register, it applies to anything that needs those functions—a printhead driver or any capacitive load, for example," says Kooi.

The 8031 incorporates a serial 38-bit input shift register, 38-bit latch register, voltage translators to boost 5 V to 100 V, and 38 push-pull 100-V output drivers. Load- and chip-select inputs provide host microprocessor control.

The chip's flexible clocking path includes a relatively high-voltage analog input, RC-controlled internal oscillator to manage the clock setting, voltage translator, a divide-by-256 frequency stabilizer for the 100-V backplane output, and automatic detection circuitry that can set the chip to a self-oscillation or slave mode.



The 8031 integrates a 38-bit input shift register, 38-bit latch register, voltage translators, and 38 100-V output drivers.

Since no off-chip logic is needed to set up the slave mode, fewer pins are necessary. The divide-by-256 circuits run the internal oscillator at relatively high frequencies while the driver delivers the 200-Hz switching speeds common to LCD backplanes. The higher internal frequency increases stability, which means smaller capacitors and resistors can be used to save board space and cost. The chip can automatically detect the presence of another 8031's voltage on the LCD backplane when multiple devices are cascaded.

A bonding option in the 8031 allows customers to match the chip's pinout and package size to the number of display segments in the LCD panel. A 48-pin dual in-line package brings out all 38 high-voltage drivers. A space-saving 44-pin leaded chip-carrier package (conforming to Military Standard 883C) will hold chips configured for 30- and 32-segment control.

The 8031 draws 0.25 mA and requires a +5 to +15 V supply for logic. The military version in 44-pin cerquad packages costs $54.50 each in 100-unit lots. A commercial 44-pin cerquad version costs $39.50 each and $27.90 in a 48-pin plastic DIP. – *J. Robert Lineback*

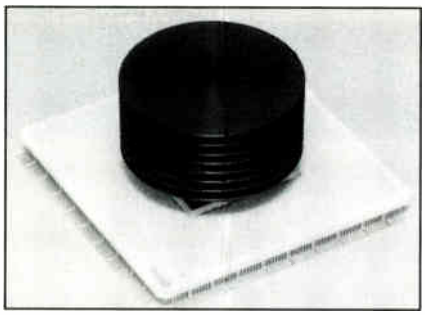
Micrel Inc., 1235 Midas Way, Sunnyvale, Calif., 94086.
Phone (408) 245-2500 [Circle 360]

FUJITSU'S BIPOLAR ARRAY BOASTS 100-PS DELAYS

By implementing its 10,000 gate bipolar gate arrays in an advanced bipolar ECL process, Fujitsu Microelectronics Inc. engineers are delivering unloaded gate arrays that outperform the competition by a factor of three.

The ET10000H boasts 100-ps unloaded gate delay at 2.44 mW and 180 ps at 1.22 mW. Loaded gate delay is 400 ps per gate at 2.44 mW. Keying the performance is the company's three-level-metal self-aligned emitter base process that incorporates polysilicon electrodes and resistors and combines groove isolation with more traditional field oxide isolation, says Joseph M. Schwartz, bipolar custom/semicustom product marketing engineer at the Integrated Circuits Division, San Jose, Calif.

The process features 0.5-μm emitters using a 1.0-μm mask, 2-μm channel lengths, and 4.5-μm metal pitch on the



interconnections. The polysilicon-emitter-based self-aligned structure makes possible extremely shallow active areas resulting in a significant reduction in parasitic capacitance, allowing the gates to run faster with less power, Schwartz says.

A thick oxide layer also contributes to reducing the parasitic capacitance of the resistors and the wiring channels. And the use of the grooved isolation structure reduces collector substrate capacitances. In the case of the collector base structure alone, says Schwartz, a 30% decrease in capacitance results in a 10% improvement in gate delay.

Compatible with both 10K and 100K ECL circuits as well as mixed ECL-TTL, the arrays offer 25, 50, or 100 Ω ECL output options. ECL input/output delay, including that of the package, is 950 ps, input buffer delay is 1.0 ns, and output buffer delay is 3.5 ns.

The ET10000H contains 9,856 equivalent gates in the internal array and up to 200 gates in the I/O section. These gates are organized into 1,792 basic cells that are capable of toggle rates up to 1.1 GHz.

The arrays are designed using Fujitsu's integrated design system, which is available on several popular computer-aided-design work stations, including Daisy Systems Corp., Mentor Graphics Corp., and Valid Logic Systems Inc., in conjunction with an Amdahl Corp. 5840 mainframe computer.

Fujitsu offers an extensive cell library of over 90 logic cells and 83 I/O cells. Implemented using a hierarchical design structure, the Fujitsu CAD tools allow, says Schwartz, up to 90% cell utilization of the array, with a guaranteed 100% fully automatic place and route without any interactive intervention on the part of the designer.

Available now, packaging options for the 512-by-512 mil device include a 208 ceramic-pin grid array and a ceramic flat package supplied with pre-attached heat sinks. Multiple heat sink options are also available. – *Bernard C. Cole*

Fujitsu Microelectronics Inc., Integrated Circuits Div., 3545 N. First St., San Jose, Calif. 95134.

Phone (408) 922-9000 [Circle 363]

AMD BOOSTS MICROCONTROLLER RELIABILITY

A watchdog timer circuit with extended error-detection features gives Advanced Micro Devices Inc.'s newest 8-bit microcontroller, the 80C521, a leg up on the competition by solving the three major reliability problems that pester those devices.

The new microcontroller is more tightly coupled to the central processor unit, which enhances the watchdog timer's ability to interpret keyed input data, says Robert O'Dell, senior engineer for microcontroller products at the Santa Clara, Calif., company. He says the watchdog timers of previous-generation microcontrollers sometimes transmitted an "all is well" signal to the on-board CPU by misinterpreting keyed input data.

The device is also protected from a second problem—software errors, which crop up when the program counter branches to an illegal address. This, in turn, leads to executing pseudo random instructions. Third, the 80C521 does not switch off during high voltage spikes caused by electrostatic discharge or voltage noise.

A CMOS pin-compatible version of the industry standard 8051, the 80C521 comes in 12- and 16-MHz versions. It is programmable over a range from 128 μs to 4 s, and also features twice as much memory as the 8051—8 Kbytes of read-only memory and 256 bytes of random-access memory. Also being introduced is a ROMless version, the 80C321.

In addition to the three reliability problems, the new design also avoids the performance drop that occurs in most 8051 derivatives whenever external memory is accessed. This bottleneck occurs because of the programmer's constant need to set up data pointers in the internal register field with the correct address before data is loaded or stored.

This is resolved in the 80C521 by the use of two identical 16-bit pointers which can be selectively enabled. Throughput is increased, says O'Dell, since fewer instructions are required to complete the same task.

Available now in production quantities, the 80C521 costs $8.80 each in 1,000-lot quantities, while the ROMless 80C321 is $8.83 each in 100-lot quantities. An EPROM version of the device is under development. – *Bernard C. Cole*

Advanced Micro Devices Inc., 901 Thompson Place, P.O. Box 3453, Sunnyvale, Calif., 94088.

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SQUEEZING IBM PC POWER INTO A BOOK-SIZED UNIT

Paravant uses state-of-the-art packaging and memory chips to build a rugged hand-held personal computer that runs MS-DOS software

By combining the latest commercially available memory chips with state-of-the-art packaging technology in its RHC-88 handheld computer, Paravant Computer Systems Inc. has squeezed the functionality of an IBM Corp. Personal Computer into a rugged, book-sized box.

The Melbourne, Fla., company uses four 1-Mbit dynamic random-access memory chips to implement the RHC-88's 512-Kbyte operating memory. Because the ruggedness standard demanded by the Department of Defense's MIL-STD-810D rules out moving-disk storage, designers opted for battery-backed 256-Mbit static RAMs that deliver 512 Kbytes of secondary storage, says Richard McNeight, vice president.

The RHC-88 also has two internal expansion slots, giving users the option of adding up to 1.5 Mbytes of storage. For easy memory expansion, the system will accept 1-Mbit SRAMs when they become readily available, thus boosting secondary "disk" memory to 8 Mbytes.

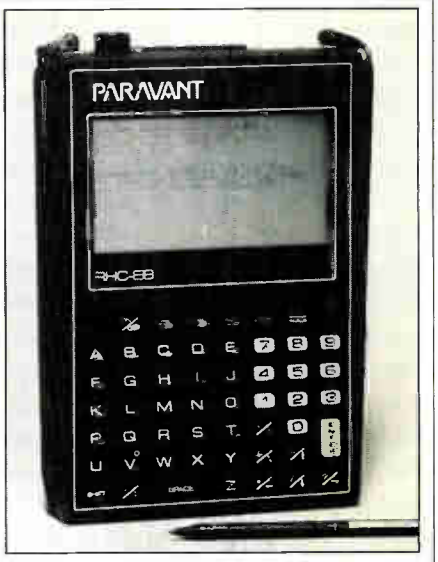
Paravant's designers also integrated 192 Kbits of erasable programmable read-only memory into the RHC-88 to handle application-specific functions. An original-equipment manufacturer adapting the computer for a specific application, for example, might use the EPROM to store an expert-system or graphics program, says McNeight.

Other technologies contributing to the ultra-dense package are NEC Corp.'s 16-bit V-40 microprocessor, programmable logic devices for glue logic, and six- and eight-layer pc boards using through-hole and surface-mount fabrication technologies. The NEC V-40—besides being compatible with the Intel Corp. 8086—boasts a higher level of integration than the Intel part, which reduces part count.

The company has targeted four broad application areas: government, specifically military; manufacturing control; field maintenance, where tutorial programs can direct technicians toward troubleshooting solutions; and gas and electric utilities for logging data.

Communications are handled by an 19.2 Kbit/s RS-232-C serial port and an optical port for downloading data. It runs on rechargeable NiCad batteries, or on ac current with an adapter. Five alkaline batteries can be used in a pinch.

Its liquid-crystal diode screen measures 5-by-2¾-in.—about one-third the size of a typical desktop PC. It is backlighted and offers 256-by-128 pixel resolution. The nonstandard keyboard has 52 keys and is waterproof.



The RHC-88 integrates a NEC Corp.'s 16-bit V-40 microprocessor and PLDs for glue logic.

The RHC-88 measures 9.4-by-6.4-by-2.6 in. and weighs 4½ lbs. Because it uses Microsoft Corp.'s MS-DOS 3.2 operating systems, the computer is compatible with virtually all software written for the IBM PC. Data acquistion boards can be plugged into its expansion slots.

Available now with delivery within 60 days, the RHC-88 costs $3,995 in single unit purchases. – *Jack Shandle*

Paravant Computer Systems Inc., 7800 Technology Dr., Melbourne, Fla. 32904. Phone (305) 727-3673 [Circle 341]

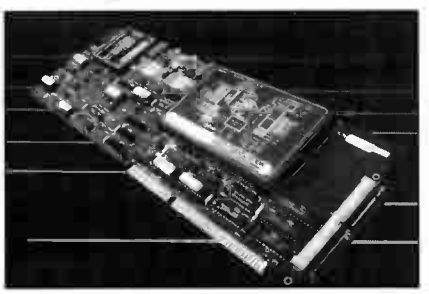
PC BOARD COLLECTS ANALOG DATA 3 TIMES FASTER

IBM Personal Computer ATs and compatibles can now collect analog data at 750 KHz—triple the current speed. Data Translation's DT2822-L board achieves its faster speed by storing incoming data in a 1,024-word, first-in first-out buffer while the system performs overhead operations such as interrupts, direct-memory-access buffer switching, and disk operations.

Previously, a designer had to channel data into a separate coprocessor board geared for digital signal processing applications to achieve a throughput of 750 MHz—or else settle for input speeds of less than 250 KHz. The FIFO buffer is a simple, nonproprietary idea, says Richard Pleau, director of marketing at the Marlboro, Mass., company. "Once we added it, the obvious question was why we didn't do it before. The obvious answer was that the cost of FIFO chips is down from about $100 three years ago to about $15 today."

Besides its FIFO buffer, the DT2822 uses a proprietary dual switching technique to gather large amounts of data continuously. The mechanism chains data through two buffers, each linked to a separate direct-memory-access channel. The board is intended for data-intensive applications including waveform, vibration, speech, radar/sonar processing, particle analysis, materials testing, and advanced biomedical research.

The board provides 12-bit resolution for 16 single-ended or four differential inputs. The sampling of input analog and digital signals is controlled by a list with 16 locations in the random-access memory.



The D12822-L board handles waveform, vibration, speech and materials testing.

During the output of analog signals, two deglitched, 12-bit digital-to-analog converters reduce noise. Each converter has a throughput rate of 130 KHz, 16 lines of digital I/O, a programmable clock, and interrupt support. The company says software programs written for its earlier DT2821 series are fully compatible with its latest model. Also, the new board is supported by Atlab, a library of subroutines for uninterrupted data transfer to memory and disk, error processing, and high-level interfaces to Fortran, Pascal, and C languages.

The 250-MHz DT2822-G costs $3,195 and a 750-MHz L costs $3,495. Available now, both run on popular work stations and PCs. – *Paul Angiolillo*

Data Translation Inc., 100 Locke Dr. Marlboro, Mass., 01752. Phone (617) 481-3700 [Circle 340]

68030 COMPUTERS OFFER MINI POWER AT 1/10TH THE COST

Two new 68030-based microcomputer systems from Motorola Inc. have been added to the VMEbus Delta series to offer original-equipment manufacturers a range of performance roughly equivalent to a minicomputer—but at prices an order of magnitude lower.

The price/performance of the model 3300, model 3600, and the previously introduced model 3800 computers in the Delta series of work group and departmental computer systems stand out far above typical 32-bit superminicomputers. For example, the 3300 models, which range in price from under $7,000 to just over $20,000, match the performance of VAX 8600 systems costing over $400,000.

HIGH END. At the high end, the model 3800 from the company's Microcomputer Division in Tempe, Ariz., matches the Digital Equipment Corp. VAX 8650 in performance and surpasses that of the IBM 4381-2. Model 3800 systems range from $40,000 to over $100,000 but the DEC VAX 8650 systems and the IBM Corp. 4381-3 cost between $600,000 and $800,000.

The model 3300, rated at 4.5 million instructions/s, is driven by a new single-board computer which combines the procesing power of a 20-MHz 68030 with 4 or 8 Mbytes of memory, a 68882 floating-point coprocessor, a Small Computer Systems Interface, Ethernet interface, four serial input/output ports, and a Centronics printer interface. Because so many functions are on this one board, there are five open slots for expansion equipment in the 3300.

The six-slot VMEbus multi-user open system targets commercial, technical, and networking applications where industry standards are important. The model 3300 in a basic configuration will sell for $6,995 in 10-system purchases and is available now.

The other models, the 3600 and 3800, are bigger and faster versions of the same basic single-board computer. Using a 25-MHz 68030, 64 Kbytes of cache, 8 to 40 Mbytes of memory, and 450- and 1,200-W power supplies, these systems are rated at 6.5 mips. The 12-slot model 3600 will ship in June for $11,895. The $27,970 (quantity 100), 20-slot 3800, introduced at Comdex last November, will ship in July. – *Tom Manuel*

Motorola Inc., Microcomputer Div., Marcom Dept., DW283, 2900 S. Diablo Way, Tempe, Ariz. 85036.
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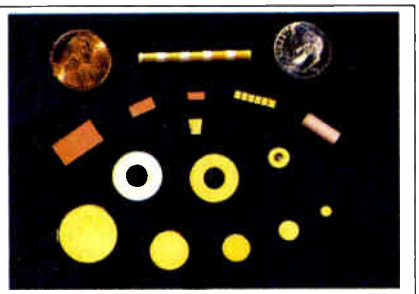

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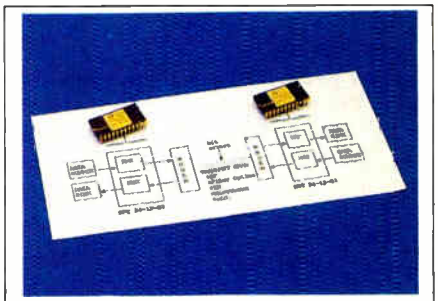

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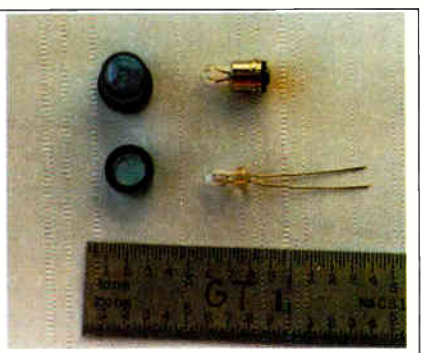

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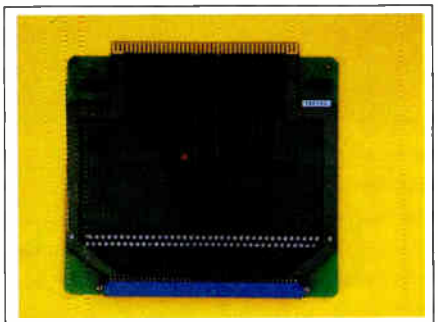

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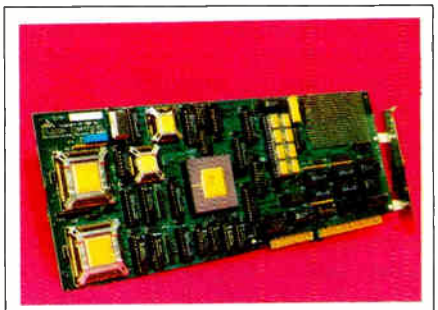

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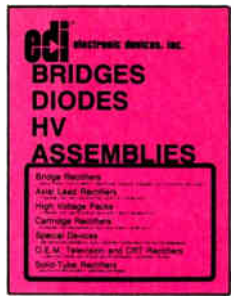

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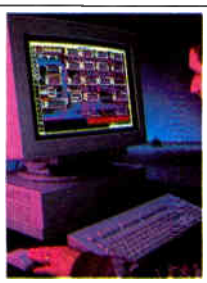

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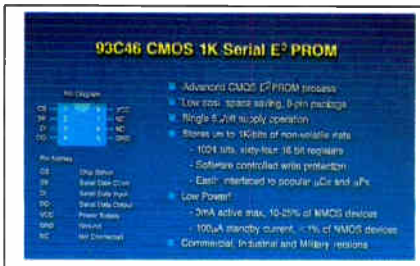

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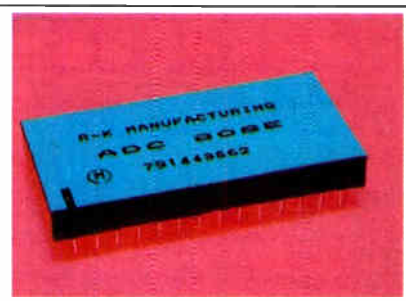

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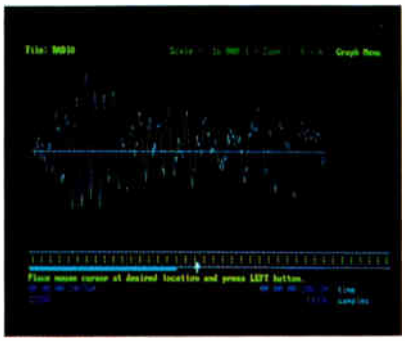

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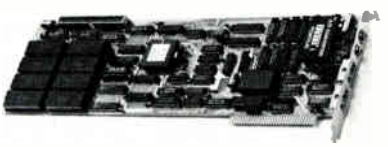

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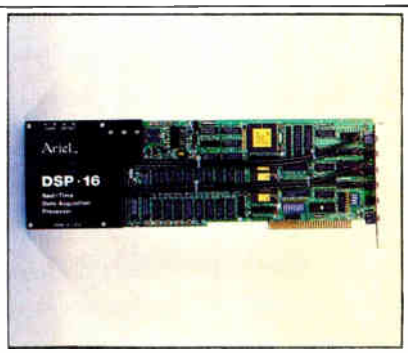

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ELECTRONICS WEEK

FLOATING POINT SEEKS COMPUTER DEAL . . .

Floating Point Systems Inc., a technology leader in array processors and minisupercomputers, says it will suspend development of its next-generation T-Series systems unless it can find a financial partner. The T-Series is a massively parallel hypercube design, and Floating Point has had trouble finding support for the exotic design, which is not compatible with the Beaverton, Ore., company's other systems [*Electronics*, March 3, 1988, p. 56]. The company says it will continue to support the T-Series systems it has already sold, and will continue with limited sales.

. . . AND UNVEILS NEW M64 PRODUCTS

Just as it put its most advanced computer project on hold, Floating Point Systems Inc. unveiled five new models of its M64 series of parallel-processing minisupercomputers. The Beaverton, Ore., company claims that the new machines are 70% more powerful than products from the competition. Peak performance of the M64/145 models ranges from 33 million floating-point operations/s to 341 megaflops. Pricing ranges from $395,000 to $1.75 million.

DOD SEEKS MORE CONTROL OF R&D FUNDS

The Defense Department is attempting to get more control over how it spends university-based research-and-development funds. The DOD plans to spend about $700 million on university R&D in 1989, says George Millburn, the acting deputy undersecretary of defense for research and development, but federal law prohibits the DOD from spending more than 14% of that in any one state. Millburn says the DOD is working to try to remove the restriction, so that research contract awards can be "made solely on technical merit and DOD needs."

EPOCH WILL UNVEIL FIRST FILE SERVERS

Epoch Systems Inc., a one-year-old startup in Marlborough, Mass., is about to unveil its first products—high-capacity file servers for networked work stations. The company, which is headed by president Kenneth D. Holberger, a former vice president for engineering at Data General Corp., will disclose its plans for a line of servers that are compatible with Sun Microsytems Inc.'s Network File System later this year. Holberger says there's a need for such file servers, especially for 32-bit graphic work stations, where he says on-line storage needs are rapidly becoming inadequate. Epoch plans to offer system file servers with capacities ranging from one to several hundred gigabytes.

APPLE SUES HP AND MICROSOFT

Apple Computer Inc. is suing two competitors on allegations that they mimicked the look and feel of its user-friendly Macintosh screen. The Cupertino, Calif., company claims Hewlett-Packard Co. of nearby Palo Alto and Microsoft Inc. of Redmond, Wash., illegally copied the Macintosh user interface in two new programs—the Hewlett-Packard New Wave software and the Microsoft Windows 2.03. Apple's suit, filed in U. S. District Court in San Jose, Calif., charges that the programs violate protected rights to the Mac's audio visual interface.

NYNEX GETTING SRX CONTROLLER

Nynex, the regional Bell operating company based in White Plains, N. Y., has signed a multiyear development agreement with SRX Corp. of Dallas, to develop and supply a new central office controller. The controller will be installed in central offices of New England Telephone Co. and New York Telephone Co., both Nynex companies. Nynex will fund the project, which aims to put the controller into service next year. SRX has the right to sell similar products to other telecommunications companies outside Nynex's service area.

GCA FINDS NEW HOME IN GENERAL SIGNAL . . .

GCA Corp., a struggling maker of microlithography semiconductor production systems that has failed to turn a profit since 1984, is being merged into General Signal Corp., Stamford, Conn. GCA, an Andover, Mass., company, will become part of General Signal's Semiconductor Equipment group, which already includes the Ultratech Stepper subsidiary. Analysts applauded the move, saying it will strengthen both companies, which will continue to offer customers a choice: GCA's mask reduction lithography or General Signal's 1:1 approach.

. . . AS GENERAL SIGNAL SELLS MASK DIVISION

Just a day after its $76 million merger agreement with GCA Corp., General Signal Corp. of Stamford, Conn., sold another operation, the Ultratech Photomask Division—which is not part of Ultratech Stepper operation—to Rexotech, a Colorado Springs, Colo., company. The $12 million division makes photographic plates for imprinting circuit patterns on semiconductor wafers. Jack Halter, a General Signal vice president, says the sale will allow General Signal to concentrate its efforts on semiconductor manufacturing equipment rather than materials for the chip industry.

STORMY WEATHER FOR THE MAKER OF 1-2-3

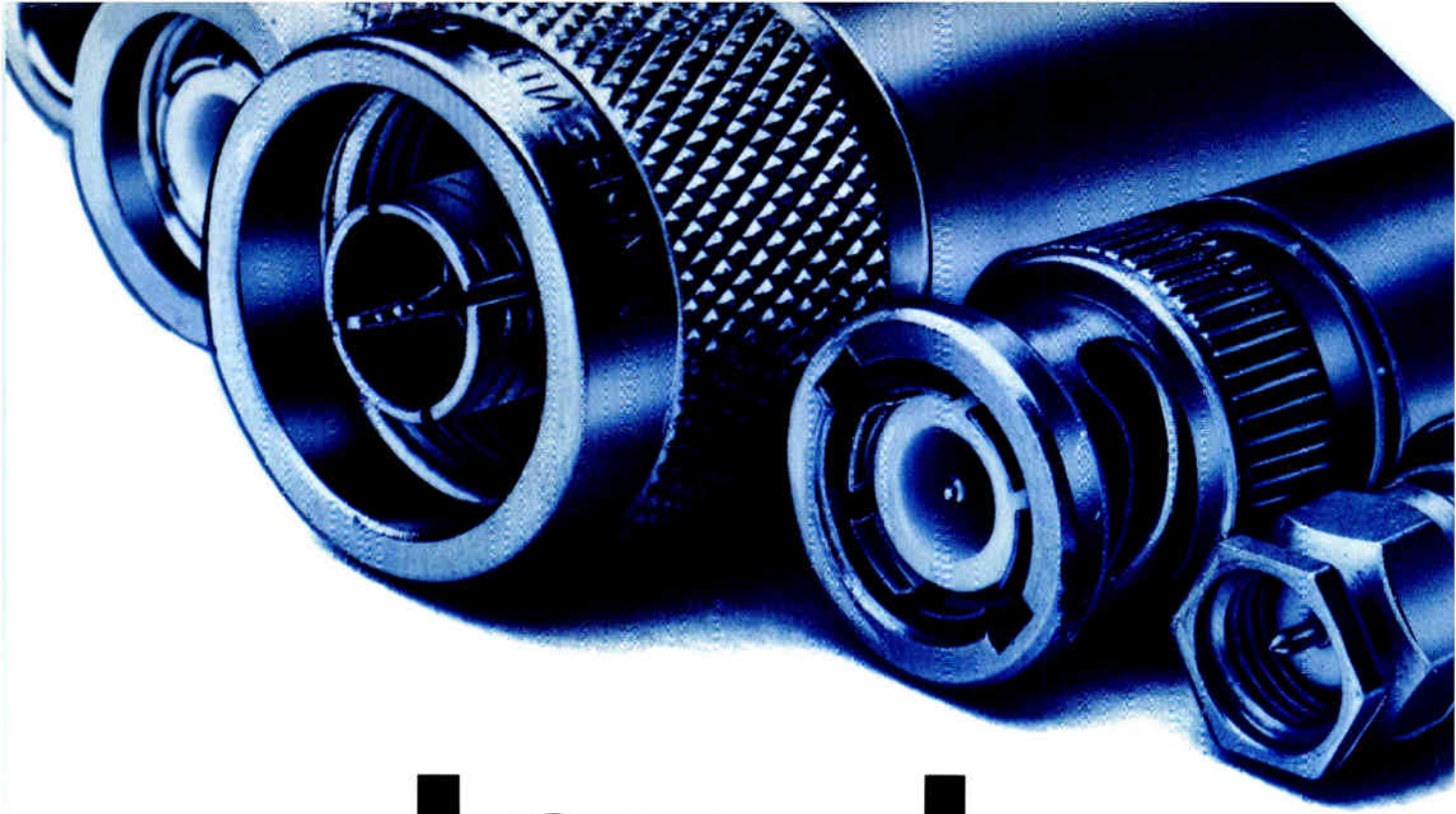
High-flying Lotus Development Corp., maker of the best-selling personal computer spreadsheet Lotus 1-2-3, is running into turbulence. Seven Lotus executives recently sold off a total of 550,000 shares of their personal stock holdings. Soon afterward, Charles J. Digate, head of software development, was forced to resign. And last week the Cambridge, Mass., company announced that shipments of the latest version of 1-2-3 will be delayed six months until late this year. Help may be on the way, though. W. Frank King III is taking over for Digate as senior vice president for the Software Products Group. King's previous post was vice president of development for the Entry Systems Division at IBM Corp.

PLEXUS RAISES NEW CAPITAL

Plexus Computers Inc. says it will use $15 million in new financing to develop its planned Extended Data Processing System. The San Jose, Calif., company wants to expand its product line in departmental computers, merging Unix-based departmental computers with a relational data base for MS-DOS personal computers.

WESTERN DIGITAL BUYS DISK BUSINESS

Western Digital Corp. has completed its deal to buy Tandon Corp.'s Winchester disk-drive business for a total of $49 million. The deal gives Western Digital, of Irvine, Calif., Tandon's engineering and manufacturing facilities in San Jose, Calif., and Singapore, as well as its plated media operations located in Santa Clara, Calif. Tandon, now solely a computer manufacturer, will buy and use disk-drive systems from its former subsidiaries.



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*Freq. (MHz)	Atten. Tol. (Typ.)	Atten. Change, (Typ.) over Freq. Range		VSWR (Max.)	
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DC-1500 MHz	±0.3	0.6	0.8	1.3	1.5

*DC-1000 MHz (all 75 ohm or 30 dB models) DC-500 MHz (all 40 dB models)

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