IT'S SHOWDOWN TIME IN INTERACTIVE VIDEO FOR GE AND PHILIPS/SONY/92

MIMIC'S NEXT CHALLENGE: SLASHING PRODUCTION COSTS/121

A McGRAW-HILL PUBLICATION SIX DOLLARS NOVEMBER 26, 1987

Electronics

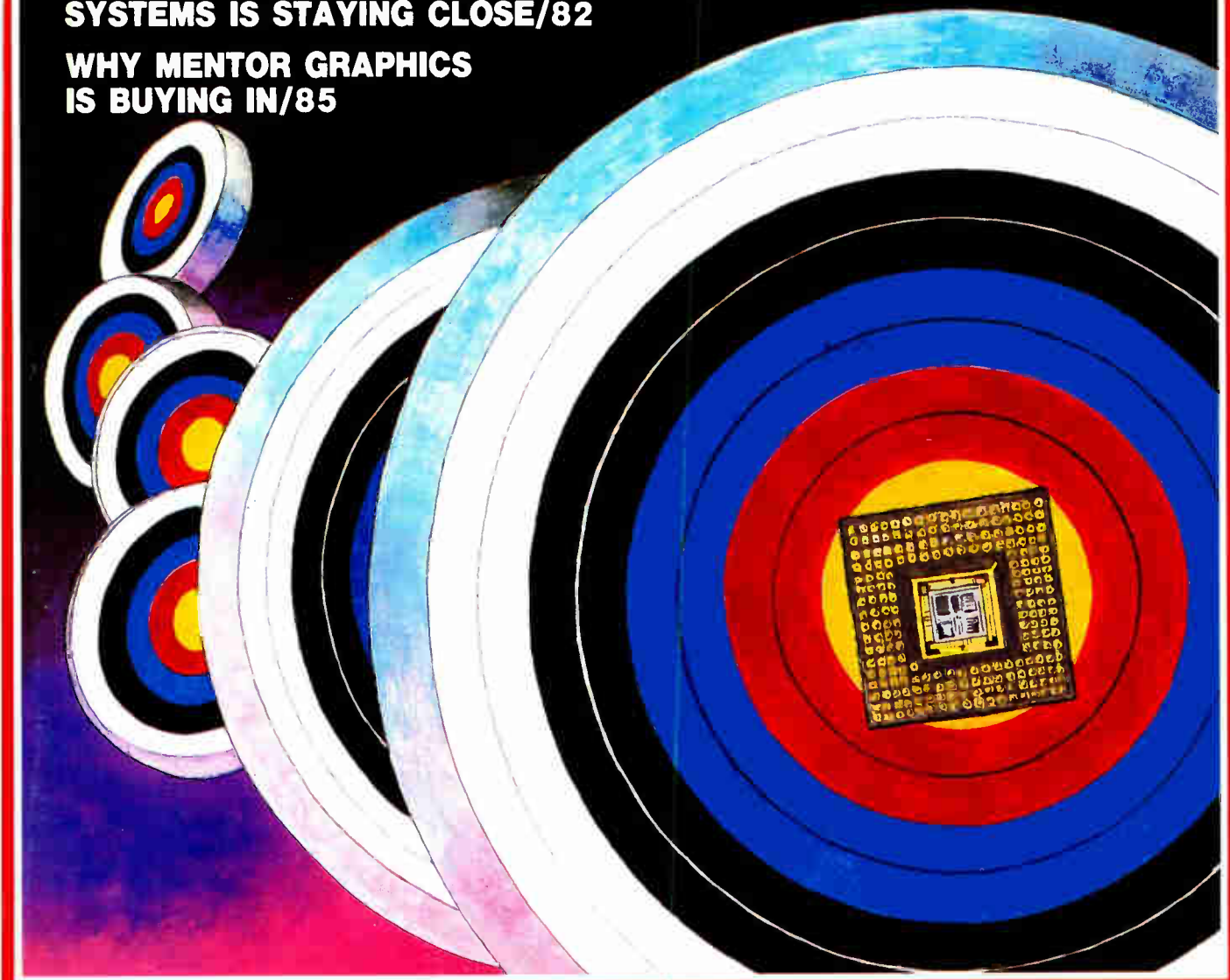
ASIC VERIFICATION:

CHASING A MOVING TARGET

PAGE 79

HOW INTEGRATED MEASUREMENT SYSTEMS IS STAYING CLOSE/82

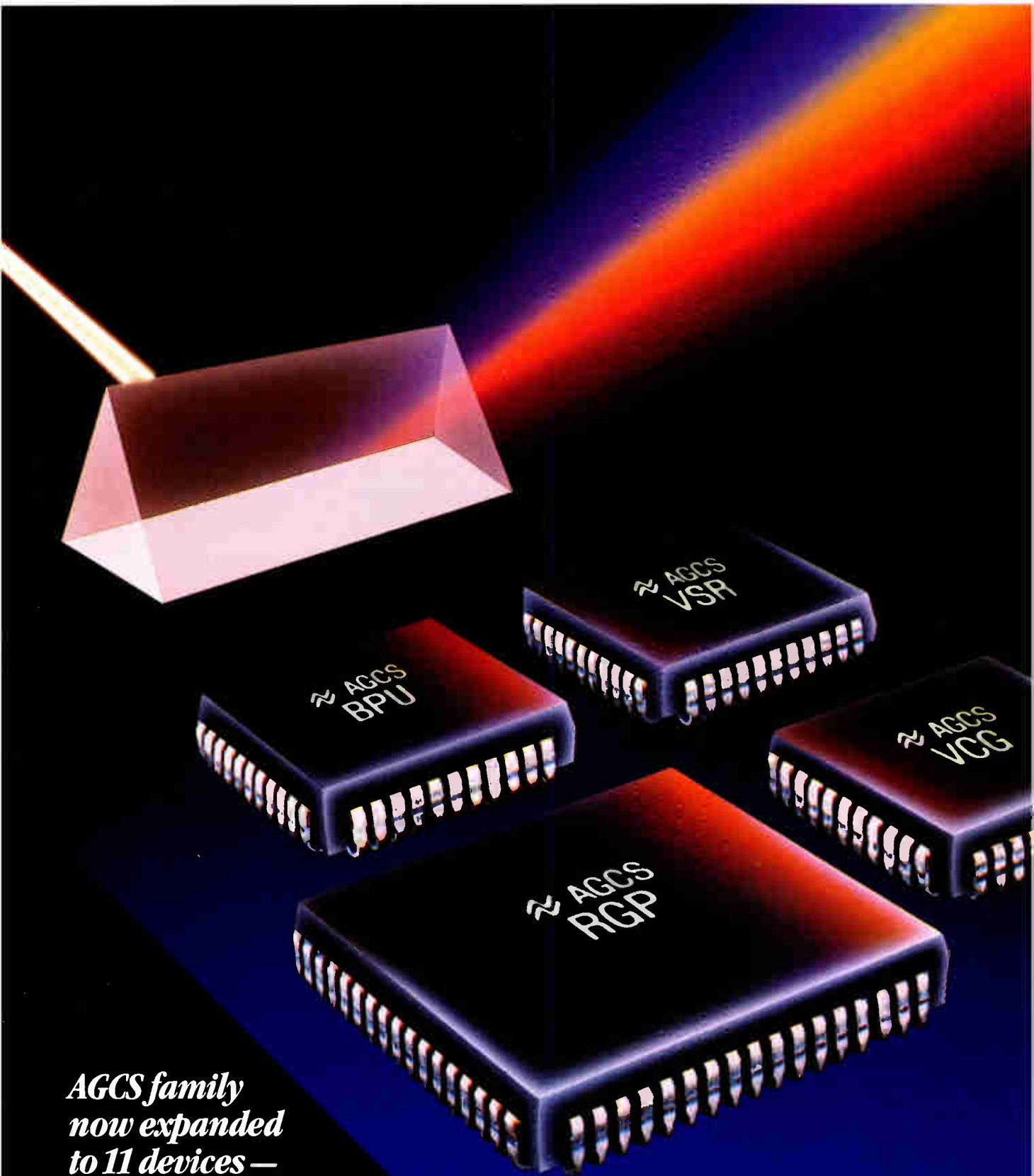
WHY MENTOR GRAPHICS IS BUYING IN/85



National Semiconductor

AGCS family now expanded to 11 devices — see box at right for details.

National Semiconductor



AGCS family now expanded to 11 devices — see box at right for details.

Finally, graphics to match your imagination...now more than ever.

INTRODUCING THE FIRST EFFECTIVELY PARTITIONED VLSI ARCHITECTURE FOR TRULY FLEXIBLE GRAPHICS SYSTEMS DESIGN

Imagine a graphics architecture so powerful, you can achieve 16K-by-16K resolution. So effective, you can add virtually unlimited planes of color without degrading performance. So flexible, you can integrate it into an existing design or use it to build an entire range of new systems.

That's the Advanced Graphics Chip Set from National Semiconductor.

By using a multiple-chip, modular approach, the Advanced Graphics Chip Set avoids the design compromises and limitations of single-chip solutions.

That gives you two unprecedented benefits: *performance* and *flexibility.*

Which means you can design exactly the type of system you need with exactly the level of performance your application demands.

For example, you can integrate part of the chip set with an existing general-purpose microprocessor for a low-end display.

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A total of 11 chips — all introduced in a single year between Siggraph 1986 and Siggraph 1987. An unmatched commitment to graphics system design.

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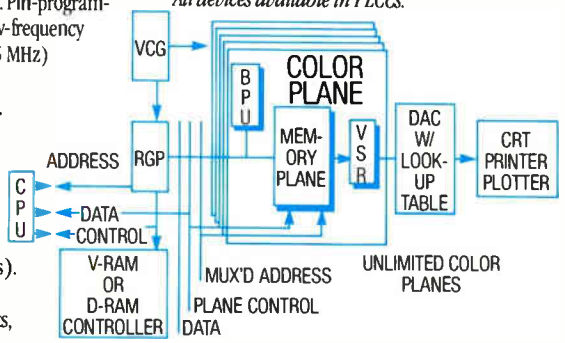

THE MULTIPLE-CHIP SECRET

The secret to all this flexibility and performance is our unique multiple-chip, modular approach. Rather than trying to squeeze all the important graphics functions onto a single chip — which would require some significant design and performance compromises — we've partitioned appropriate functions onto individual building-block ICs. This allows us to optimize the design of each chip, and allows you to optimize your own design for your particular application.

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So what are you waiting for? If you're tired of those limited single-chip solutions bogging down your designs, take a look at the Advanced Graphics Chip Set. And learn how you can design a graphics system to match your needs... as well as your imagination.

For more information and availabilities, just contact your local National Semiconductor Sales Engineer or write:

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Circle 1 on reader service card

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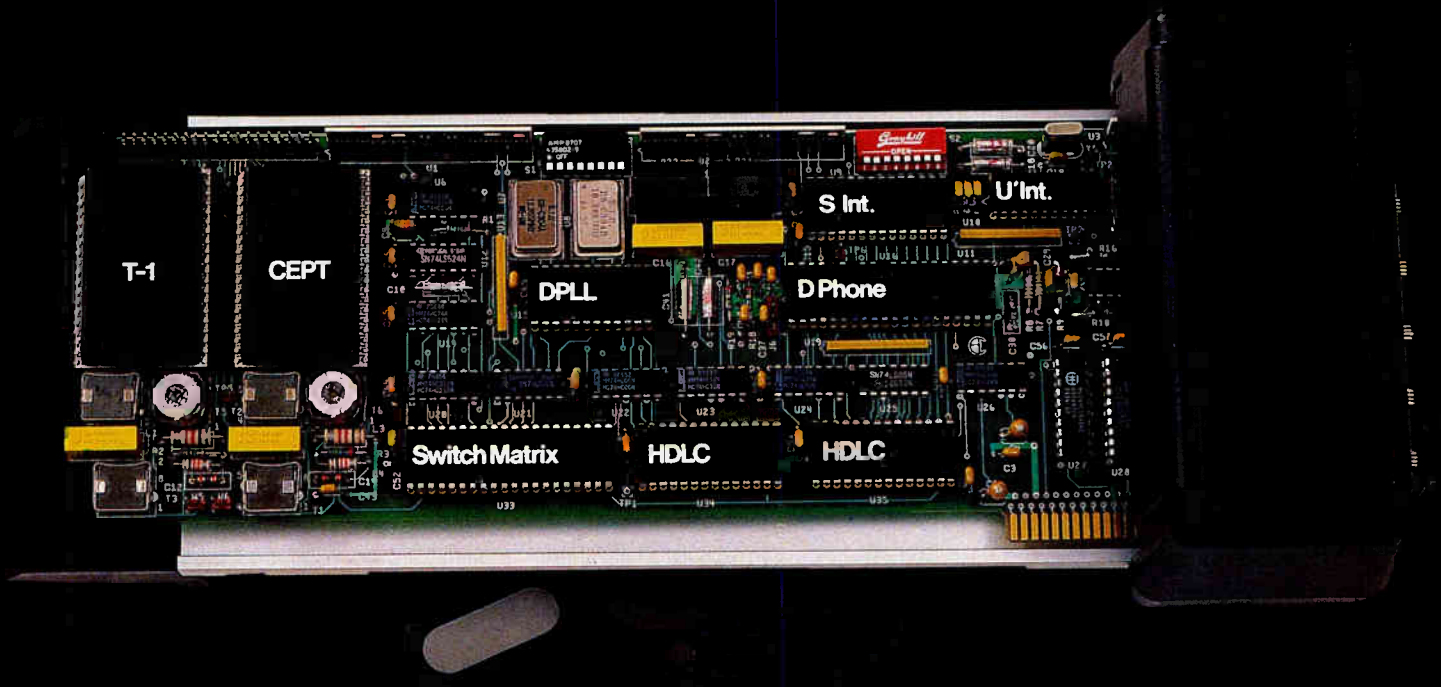

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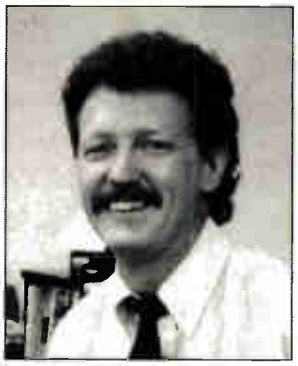
PUBLISHER'S LETTER

In its 10-year history as the premier factory-automation show, Autofact has just about undergone a complete metamorphosis. "When it first started, there was a lot of emphasis on robotics and the equipment side of the business," says Wes Iversen, our Chicago bureau manager. "But now it has a heavy emphasis on CAD/CAM."



IVERSEN: Following the twists and turns at Autofact.

Wes, who earlier this month journeyed to Detroit, where he covered his sixth Autofact—the word is a contraction of "automated factory"—says that "robots are almost nonexistent there now; in fact, they have their own show." Also, he says, "You used to see a lot of vision equipment at Autofact, but now there isn't much of it anymore."

He also remembers Autofact fondly for the excitement that was caused there by MAP (for Manufacturing Automation Protocol), General Motors Co.'s attempt to create a networking standard for the automated plant. "Two years ago GM set up a sample MAP factory at the show and there was a great deal of animated comment about the pros and cons of the whole idea. Some people thought it was the answer, others had some reservations. Given MAP's slow progress since then, it looks as if the naysayers were more right than wrong. Those were exciting days."

As a CAD/CAM show, Autofact still generates a lot of news, Wes finds. In the Nov. 12 issue, he wrote a preview about the show's day-long session on CALS, Computer-Aided Acquisition and Logistics Support, the Pentagon's multi-billion-dollar effort to convert its weapon-system documentation from paper to an electronic data base. And in this issue, on p. 40, he records and interprets the reactions of CAD/CAM software suppliers at the conference when they learned from General Motors that it was qualifying only two of them as vendors.

That approach to the story is a prime example of how we treat the news at *Electronics*. "I had heard early that GM was about to notify vendors about its decisions, and I knew that the competition would also have the story," says Wes. "So the key to my coverage was to go beyond what the others would do, which is merely report that something had happened, and add some extra value to the story."

Now, Wes notes, the show has outgrown its home in Detroit's Cobo Hall: "It's been held mostly at Cobo since it started, but it's going to Chicago next year while Cobo Hall is being enlarged. Then, the plans are to return to Detroit in 1989." Wes points out that the show started with just 16,500 square feet of floor space. This year, the 300 exhibitors in Cobo Hall needed more than 10 times that much space—185,000 square feet.

Whatever it takes, the 40-year-old has the experience and skills to handle such changes of direction with aplomb. A former newspaperman, he first came to *Electronics* in Dallas in 1978 after a stint as a business-news reporter on the Dallas *Times-Herald*. After working for us in our Dallas bureau, he went to Chicago as bureau manager for McGraw-Hill World News. He switched back to *Electronics* in 1981 in Chicago with the same title and has been there since.

Laurence Altman

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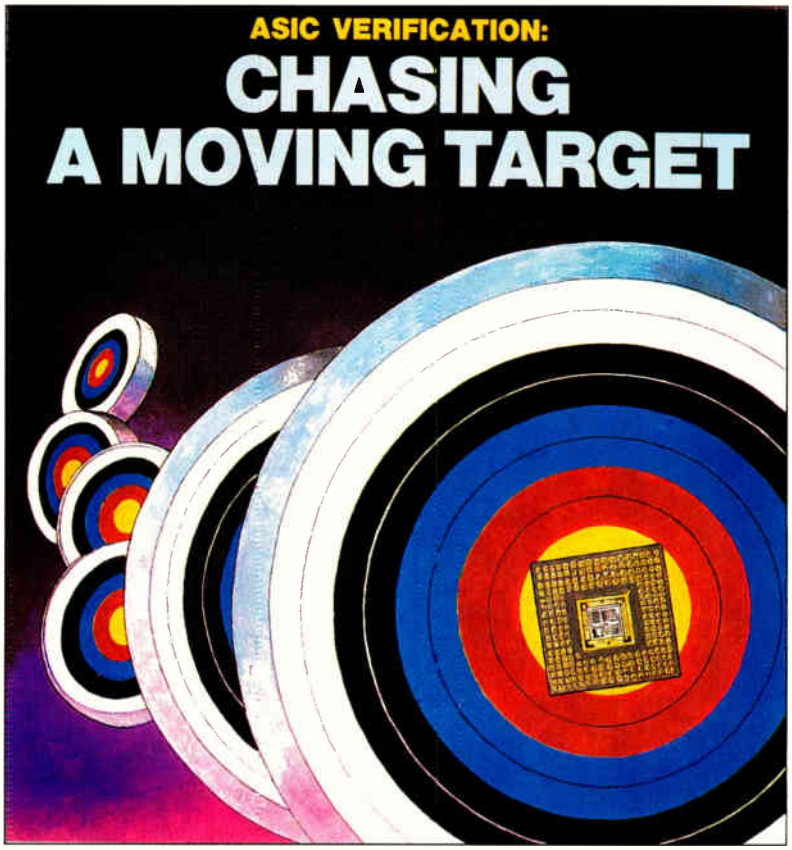
NOVEMBER 26, 1987

Electronics

NEWS

INSIDE TECHNOLOGY

COVER: ART DIRECTOR FRED SKLENAR



PAGE 79

NEW PRODUCTS

DEPARTMENTS

Narrow your horizons.

Put your hard disk controller on a single chip.

Twenty chips and a board is too much hardware for a hard disk controller. Any engineer would agree. So we focused our attention on turning all that into a single chip: the Am9590 Hard Disk Controller.

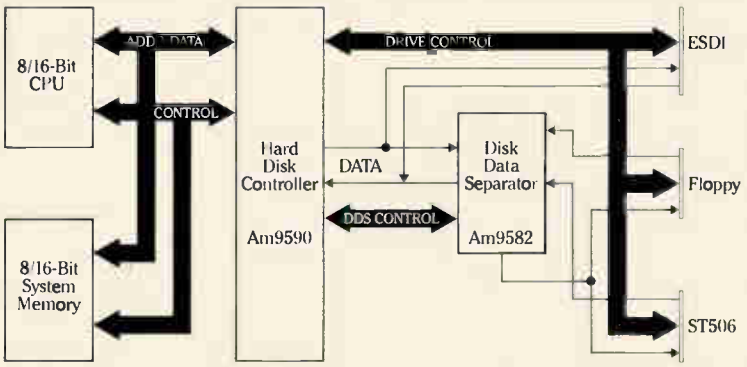
The Am9590 can control up to 4 drives allowing for any mix of hard and floppy drives. It supports ESDI, ST506/412 or standard double density floppy disk interfaces. Use the Am9590 with its companion chip the Am9582 Disk Data Separator to design your current ST506 system and you've got an easy upgrade to ESDI system performance for the next generation. Or you could always start that next generation now with the Am9590 as a stand alone.

On-board EDC.

The Am9590 even has on-board EDC. Select an error detection code (CRC-CCITT) or one of two error correction codes (Single or Double Burst Reed-Solomon). Or if you prefer, the Am9590 provides handshake interface to your own external ECC circuitry. All this adds up to maximum data integrity.

And it's easy to use. A comprehensive high level command set (with command chaining) allows for independent operation without constant CPU intervention.

You can even shorten your design cycle with an evaluation board, development software and a BIOS driver.



On-chip DMA with data mapping.

We gave the Am9590 on-chip DMA with data mapping (which will come in handy when you're working with UNIX). Then we added dual on-board sector buffers to allow for Zero Sector Interleave. This simple way of organizing sectors means that access time is bounded by drive capabilities—not controller limitations. And it leaves the CPU free to do the things it does best.

If all this sounds interesting, get in touch with us for more information. Once you've used the Am9590 Hard Disk Controller, you'll understand why the narrower view can be very broadening.

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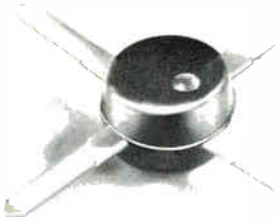

dc to 2000 MHz amplifier series

SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	• MAX. PWR. dBm	NF dB	PRICE Ea.	$ Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

NOTE: Minimum gain at highest frequency point and over full temperature range.
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*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

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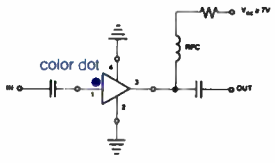

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

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Want to turbocharge your current system? No problem. Our exclusive Link Adaptor IC's allow Transputers to be connected to other microprocessors or peripherals.

Other team members include the pin compatible T414 Transputer, offering lower cost, 10 MIP performance and 0.75M Whetstones. Lined-up to provide all the I/O processing you need, the T212 16-bit Transputer is the ideal high performance controller and the M212 Disk Processor combines disk controller hardware and a Transputer on a single chip, supporting both Winchester and floppy disks. And the C004 Link Switch makes the design of software reconfigurable multiprocessor systems as easy as kicking an extra point.

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Transputers to MIL-STD 883C will be available in the first half of 1988.

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IMS T212-17	16-Bit	17	8000	–	Now	Q2 88	68 PGA
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IMS M212-17	16-Bit	17	8000	–	Now	–	68 PGA
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Part No.	Description		Communication Speed		Commercial	Military	
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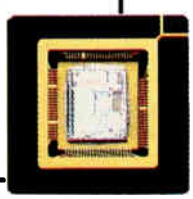

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So we're offering you comprehensive solutions. One, a leading-edge, bipolar op amp. The other a state-of-the-art JFET op amp. Both superb combinations of performance, versatility and low-power efficiency. With exclusive, all-NPN output stages providing unique advantages.

So you can use them for a myriad of designs without stepping into a black hole of endless device analyses.

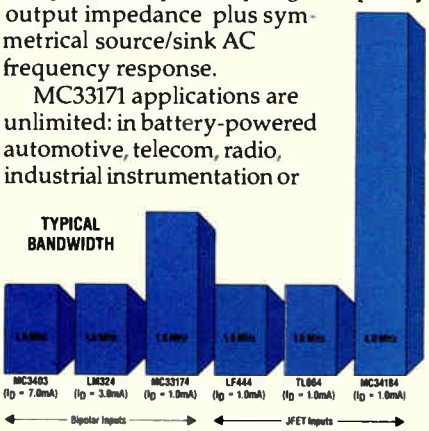
Single supply MC33171 uses one-eighth the power.

Operating from a single, +3 to +44 V supply, or dual ±1.5 to ±22 V supplies and with a common mode input which includes ground, the MC33171 family provides superior performance to industry standard bipolar single supply op amps. While consuming one-third the drain current of the LM324 and one-seventh the drain current of the MC3403 quad op amps, the MC33174 offers nearly double the bandwidth and slew rate of the popular devices.

The MC33171 provides 1.8 MHz bandwidth (nearly twice that of ordinary JFETs), and a 2.1 V/μs slew rate. This bipolar family has performance comparable to low-power JFET input op amps such as the TL061 and LF441 series but it provides a much better output voltage swing: 28.4 V p-p with ±15 V supplies.

What's more, its all-NPN output stage, characterized by no deadband crossover distortion and large voltage swing, provides high capacitive drive capability, excellent phase (60°) and gain (15 dB) margins, low open-loop high-frequency output impedance plus symmetrical source/sink AC frequency response.

MC33171 applications are unlimited: in battery-powered automotive, telecom, radio, industrial instrumentation or



active filters. In strong RF fields and other high-noise environments such as remote sites and robotics. And in lower-current D/As where the series settles to within 1/2 LSB of 12 bits in 4.8 μs for a 10 V step.

Where low-power and versatility are paramount, the MC33171 bipolar op amp fits beautifully.

High performance MC34181 JFET sizzles at 4 MHz.

That's four times more bandwidth than the LF444 and TL064.

What's more, this new family provides extremely fast settling times, 1.1 μs to 0.1% and 1.5 μs to .01%, ideal for A/D sample-and-hold circuits.

Its 10 V/μs slew rate is three times greater than the TL061's and ten times more than the LF444's. Combine these parameters with the MC34181's low, 2 mV V_{IO}, very high input impedance for low input bias and offset currents of 3 and 1 pA, respectively, and you have the answer to precise performance in instrument amplifiers.

Plus, output voltage swing of the MC34181 is up to 35% better than comparables when operated with low supply voltages.

Like the MC33171, you can use it to improve performance in communications networks, audio designs, and battery-powered applications where low power and a substantial boost in performance payload are design goals.

Multiple choice for your launching pad.

Both families are available in plastic dual-in-line, SOIC and ceramic dual-in-line packaging over all temperature ranges in single, dual and quad configurations—a total of 24 choices to master your world of op amp applications.

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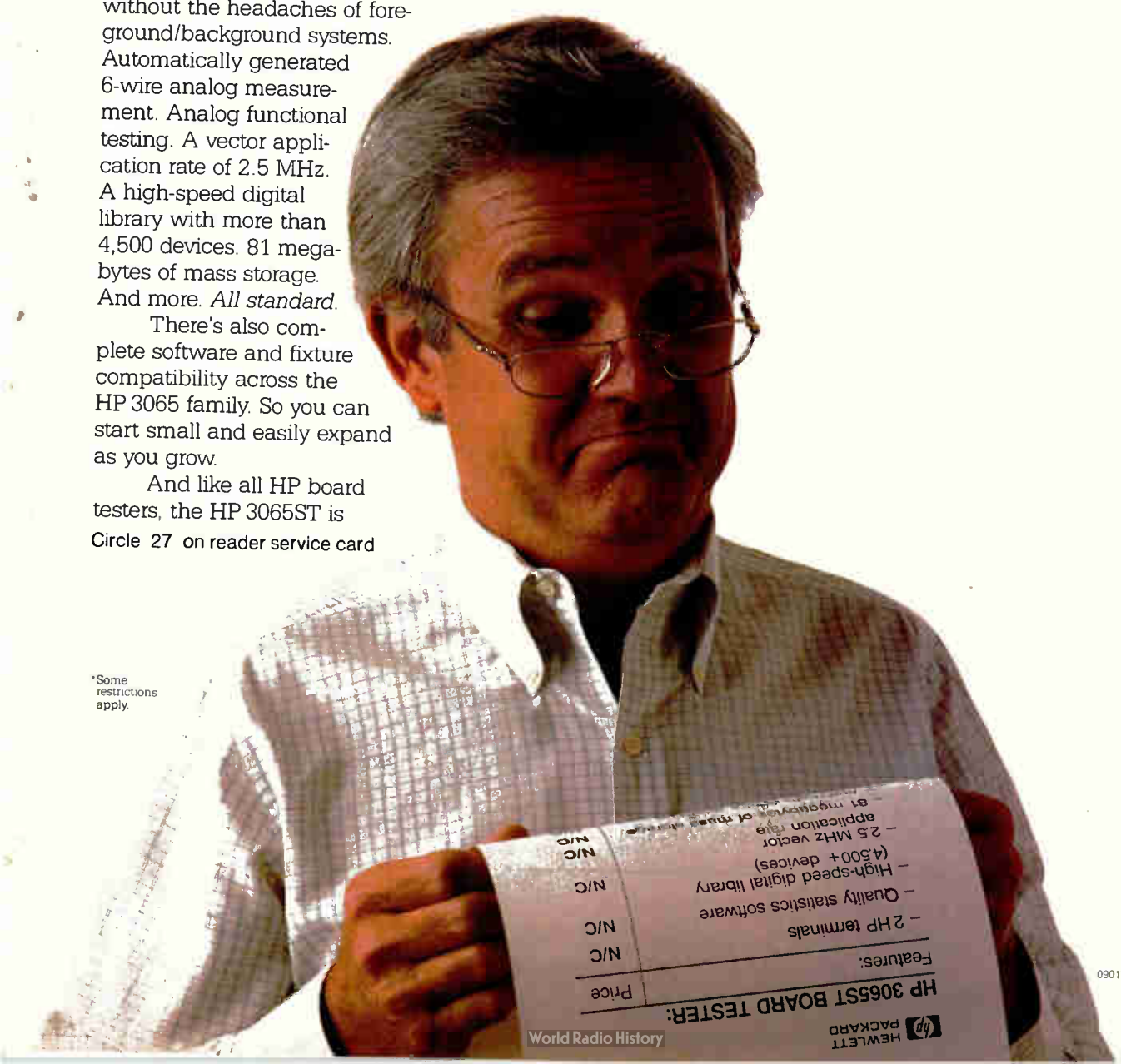

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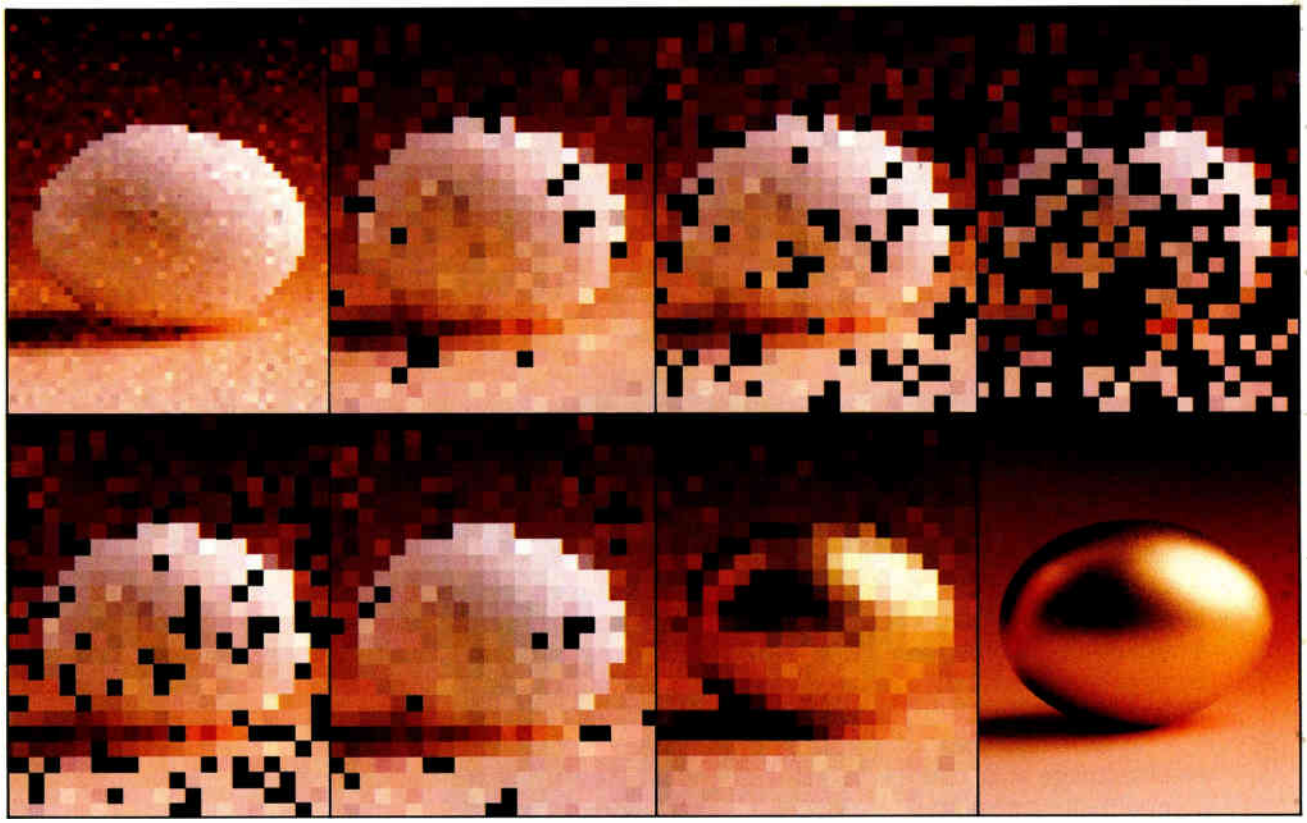

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ELECTRONICS NEWSLETTER

MOTOROLA UNVEILS AN AMBITIOUS RETURN TO COMMODITY MEMORIES

Motorola Inc. finally went public on its widely expected re-entry into the commodity memory business, but it's a lot more ambitious than had been expected. Motorola surprised observers by moving into the static random-access memory business as well as dynamic RAMs. The U. S. chip maker also is aiming at a big chunk of the world market by 1992: Its plan calls for memory sales of nearly $1 billion out of a 1992 market of $11.2 billion. It wants 10% of a $5.5 billion dynamic and video RAM market and more than 10% of both the $1 billion fast SRAM and $1.3 billion slow SRAM business. Motorola will get wafers from Toshiba, under their five-year technology agreement, until 1988, when it will start making its own wafers. Final production of all memory parts, including assembly, burn-in, and test, will take place at Motorola's huge Malaysia plant. A 64-Kbit and a 256-Kbit SRAM will go into production next year at three Motorola plants, and a 4-Mbit DRAM and 1-Mbit SRAM will be phased in later. Motorola's strategy "sounds good, but the proof of success will come only with volume production of RAMs," cautions market watcher William J. McClean at Integrated Circuit Engineering Corp. He notes West Germany's Siemens has had a similar deal with Toshiba for years but still hasn't penetrated the commodity memory business. □

ALLEN-BRADLEY WILL INSTALL THE FIRST MAP 3.0 PRODUCTION NETWORK

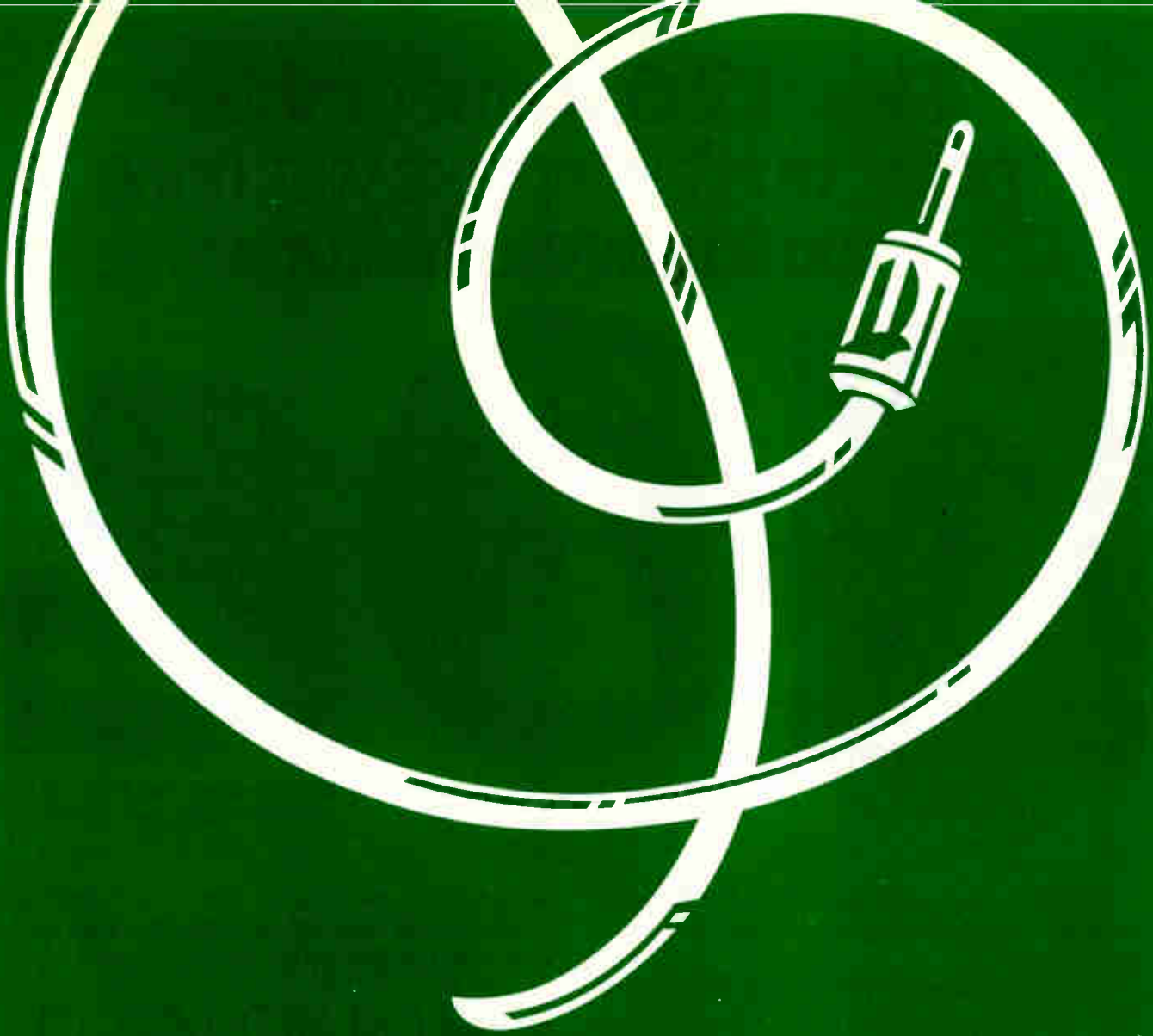
Even though version 3.0 of the Manufacturing Automation Protocol is not due in final form until next June, Allen-Bradley Co. says it's not waiting. The company will install what may be the first production network based on a preliminary version of MAP 3.0 late this month at a General Motors Corp. plant in Oshawa, Ont. What's more, the network will be one of the first production MAP nets to rely on an IEEE 802.4H fiber-optic transmission medium, instead of the broadband cable used in most MAP installations. The GM net will tie together 150 Allen-Bradley PLC-3 programmable controllers and implement the full MAP protocol, including MMS (for Manufacturing Message System), a key to MAP 3.0's improved functionality over MAP 2.1. □

VTI MAKES ITS PORTABLE LIBRARY MORE PORTABLE

VLSI Technology Inc. is making its Portable Library more portable. The library gets its name from its ability to translate semicustom-chip designs from gate array to standard cell technology, but now VTI's doing it one better. The San Jose, Calif., semicustom chip maker's latest strategy seeks to sell the library through third-party venders of computer-aided engineering systems, thereby tapping into the installed base of CAE systems and software. First to sign up is Daisy Systems Corp. of Mountain View, Calif., which will merge VTI's libraries with its own CAE schematic capture and simulation tools in an agreement to be announced after Thanksgiving. Until now, VTI's gate arrays and CMOS standard cells have only been available as part of its own set of design-automation tools.□

AT&T FIBER-OPTIC NET TO GROW 4X IN CAPACITY AND 2X IN LENGTH

AT&T Co. is spending $6 billion over the next two years to double its worldwide fiber-optic network to 88,000 miles by 1991 and to quadruple transmission speeds to 1.7 gigabits/s in each pair of optical fibers. The increased capacity comes from improvements in the repeaters that appear every 46 km along the long-distance lines. The repeaters use advanced avalanche photodiodes in their receiver elements, instead of the p-i-n photodiodes of old. Fast gallium arsenide integrated circuits, meanwhile, have replaced silicon ICs as regenerators. Most important, however, are powerful new 1.3-μm lasers that can switch four times faster than their predecessors. □



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PRODUCTS NEWSLETTER

CIPRICO'S DISK CONTROLLER DOUBLES THROUGHPUT OF SUN WORK STATIONS

Users of Sun Microsystems Inc. series-3 and series-4 work stations can speed up disk-drive read and write throughput by 25% to 100%—or more—with Ciprico Inc.'s Rimfire 3220 SMD-E disk-controller board. The performance boost over the standard Sun SMD-E drive control comes from a number of built-in 3220 features, including the use of look-ahead cache memory, says the Plymouth, Minn., company. Based on an Intel Corp. 80186 microprocessor, the 3220 supports drive data rates up to 24 MHz and can burst data across the system bus at rates exceeding 30 Mbytes/s, Ciprico says. The 3220 can control up to four disk drives. It is available in small quantities now, with production volumes scheduled for delivery starting in December. Single-unit price is $3,495. □

INTEL'S 8-BIT MICROCONTROLLER IS LOW-COST AND AN EASY UPGRADE

An easy upgrade path and a cost of less than $5 are the main attractions of Intel Corp.'s latest embedded-microcontroller offering: a 16-bit architecture for the mature 8-bit market. The 48-pin 8098 has the same die design as the 16-bit, 68-pin 8096 but uses an 8-bit data bus. It offers a full 16-bit central processing unit, 14-bit analog-to-digital converter, 16-by-16 hardware multiplier, 32-by-16 divider, three operand instructions, and register-to-register architecture. Product managers at Intel's Embedded Control Operation in Chandler, Ariz., say they're luring 8-bit system designers with the prospect of software libraries compatible with the 16-bit chip for future upgrades. Available in December, the 8098 will cost $6 in single units and $4.75 in 100,000-unit orders—one-half to two-thirds the cost of a 16-bitter. □

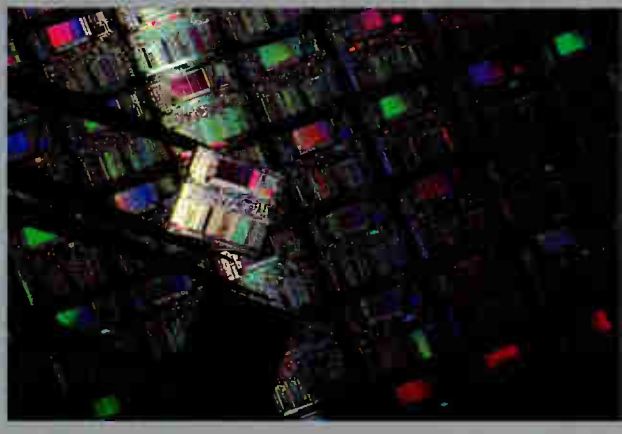
NOW, ASIC DESIGNERS CAN CREATE THEIR OWN CELL LIBRARIES PAINLESSLY

Using artificial-intelligence techniques, Trimeter Technologies Corp.'s Knowledge Consultant lets designers of application-specific integrated circuits develop their own cells modified from existing cells either to save silicon real estate or to achieve higher speeds. Knowledge Consultant makes creating optimized cells easy by presenting users with a familiar circuit-schematic format in graphic form—but unlike most AI applications, users don't need to know rule-based programming. Once a cell is created, Knowledge Consultant verifies functionality against the circuit it replaces and calculates the speed and area requirement of both circuits, telling the user how much advantage his new cell offers. The new cell goes into the cell library of the Pittsburgh company's other product—Logic Consultant, which automatically optimizes ASIC designs. Available now for Mentor Graphics Corp. work stations, Knowledge Consultant costs $49,500 and Logic Consultant costs $30,000. □

PHILIPS'S VOLTAGE COMPARATOR CLAIMS LEAD IN GAIN, POWER DISSIPATION

A precision voltage comparator from Philips of the Netherlands boasts 32-ns propagation delays and 0.04 least-significant-bit accuracy in 10-V systems—that's performance equal to the best on the market. But the 12-bit NE/SE5105 easily outstrips the competition in other areas including gain, power dissipation, and offset voltage and current. Targeting the high end in such applications as analog-to-digital converters and precision signal regenerators, it offers a gain of 20,000 compared with 16,000 for the competition; power dissipation of 130 mW compared with 155 mW; offset voltage of 250 μV compared with 600 μV; and offset current of 20 nA compared with 80 nA. Available now in samples, pricing depends on importing country. The U. S. price is projected at about $2.50 each in lots of 1,000 units. □

Digital has it now.



"Our Dracula™ layout design verification software was developed and based on Digital systems, and for very good reason," states ECAD President Jim Hill. "Our customers in Integrated Circuit design regard Digital's VAX™ systems as the standard. Recognizing that, we've developed a line of software products that have made us the standard of our industry."

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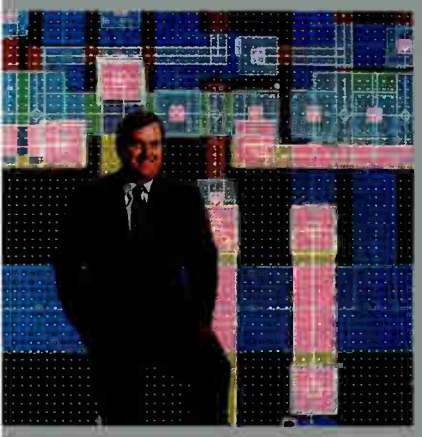

"ECAD seized an 80% world market share – the key was writing our design software to the industry standard, Digital."

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Electronics

A NEW SGS-THOMSON STARTS GETTING ITS ACT TOGETHER

THE GIANT CHIP MAKER'S WORLDWIDE ORGANIZATION IS 90% COMPLETE

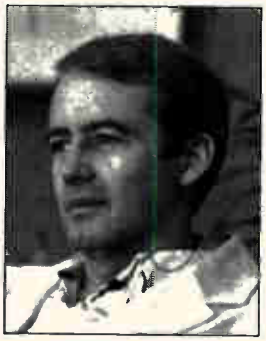
PARIS

Ambitious projects like putting together a billion-dollar semiconductor company almost always take longer to pull off than their backers figure they will, and SGS-Thomson Microelectronics BV is no exception.

Europe's new world-class chip maker had a baptism of sorts at last week's biennial Paris Salon des Composants, pitching products for the first time under the joint banner of the firm forged early this year by the merger of Italy's SGS-Microelettronica SpA and France's Thomson Semiconducteurs SA, both of which were government-owned companies. But as showgoers flocked to the newly named company's stand, Pasquale Pistorio, who headed SGS before the merger and now is running the Franco-Italian combine, was still piecing together the team he expects to propel the new company into the ranks of the top 10 semiconductor makers. At the moment, with estimated 1987 sales of $850 million, SGS-Thomson ranks No. 12 among world chip makers and second in Europe, behind Philips of the Netherlands.

PASQUALE PISTORIO

DANIEL QUEYSSAC



JAMES FIEBIGER

Pistorio quite likely won't have his five-year plan wrapped up until late this year or early next. "The new worldwide organization is about 90% complete," reports a ranking SGS-Thomson executive. The people are not yet all in place, but the overall structure is clear: a matrix linking three regional organizations—Asia-Pacific, Europe, and America—with a handful of product divisions operating worldwide.

TWO AIDES. To help him keep the matrix meshed, Pistorio has named two key aides. Maurizi Ghirgha, SGS's controller, will handle the financial side; Philippe Geyres, from Thomson's planning group, will serve as strategy manager, with legal, technical, and economics and marketing chiefs reporting to him.

The headquarters staff of the company, which is incorporated in the Netherlands, could wind up either in Paris or the Milan suburb of Agrate, but as yet, SGS-Thomson has no legal status in either France or Italy. Says one official, "People are shuttling back and forth every week and you might pinpoint the geographical headquarters as a plane flying over the Mont Blanc."

In addition to top headquarters executives, other appointments have been made. Voichy Somogy, a Hungarian, will run the Asia-Pacific region from Singapore. And to head the U.S. operation, Pistorio settled on Daniel Queyssac, a U.S. citizen born in Paris.

Queyssac for the past seven years has headed SGS Semiconductor Corp., the Phoenix-based U.S. subsidiary of the Italian parent company. His main competitor for the U.S. job was James Fiebiger, who previously headed Thomson Components-Mostek Corp. in the Dallas suburb of Carrollton.

Actually, Fiebiger was not simply passed over. Pistorio offered him a top slot in Europe as assistant general manager of the merged company. "Pasquale had a tough decision [selecting the head of the U.S. operation]," says Fiebiger. "He offered me the best job he felt he had and that was to help him run the worldwide activity. But I felt for personal reasons . . . I really want to stay in the U.S. and take on something that needs to be turned around." After Fiebiger turned it down and left the company, the post was excised from the organization chart.

And for the next few months, at least, Queyssac will shuttle between Phoenix and Carrollton. At the outset, he says, the two operations will be kept separate while the merging companies go through a review period with the U.S. Justice Department. He expects the review to be completed by the end of the year.

As it stands now, the U.S. arm of SGS-Thomson figures to take the lead role in application-specific memories, some telecom products, and semicustom application-specific integrated circuits like the leading-edge channelless gate arrays the merged company will soon offer [*Electronics*, Aug. 20, 1987, p. 42]. Queyssac says the SGS-Thomson operation in Phoenix will most likely become the pole for sales and marketing in the U.S. operation. The Carrollton operation will carry the load in research and development, manufacturing, product engineering, and have some strategic-marketing and product-marketing functions. Queyssac insists that no major layoffs are in the offing for the companies' U.S. operations. "In fact," he adds, "we intend to upgrade our facility in Carrollton to 6 in. [from the 4-in. wafers processed there now] and that could actually increase employment."

Queyssac says he is still waiting to use SGS's production facility in Phoenix. The wait, he feels, may well continue. "Every time I feel we are almost there, something happens," he says. "Now, with the economic situation and the uncertainties in the financial marketplace, we are again being a little cautious in committing to major investments."

BACK TO DRAMs. One major investment that Queyssac and Pistorio must puzzle over is a return to the dynamic random-access memory market. "I'm interested in dynamic RAMs," Queyssac admits, referring to growing pressures from U.S. customers wanting another domestic source. Texas Instruments Inc. and Micron Technology Inc. are the only two right now,

but Motorola Inc. plans to start producing DRAMs in the U.S. designed by Japan's Toshiba Corp. (see p. 29). "We may be selectively looking at some DRAM activity, but that does not mean we have made any decisions to reenter the market.... We have the technology capability with a new 0.8-μm process being finalized. It would fit well for either static or dynamic RAMs." He quickly adds, however, that other factors enter into the decision, such as additional manufacturing capacity.

By and large, semiconductor-industry analysts rated the merger as a strong move when the two governments okayed the deal in late April [*Electronics*, May 14, 1987, p. 60]. Even now that he is an outsider, Fiebiger is optimistic about the success of the new SGS-Thomson company. "The outlook is very positive for the combined companies. I think it is great—the portfolios are super and not much of an overlap," he says. No one inside SGS-Thomson would quarrel with that. *–J. Robert Lineback and Jennifer Schenker*

SOFTWARE

HOW GM CHANGED THE CAD-CAM WORLD

DETROIT

The next catchword to be coined in the CAD/CAM/CAE software industry may well be "GM compatibility"—reflecting the Detroit automotive giant's move to develop internal standards for transparent data exchange among its suppliers and customers worldwide.

By pruning its list of preferred CAD/CAM/CAE software vendors to two, General Motors Corp. may heavily influence the direction of industry standards and the relative strength of suppliers. Cadam Inc. of Burbank, Calif., and the McDonnell Douglas Manufacturing and Engineering Systems Co. of St. Louis, Mo., are the two immediate winners.

The GM session at the Autofact Conference and Exhibition on Nov. 9 generated everything from praise to confusion. There was plenty of skepticism over the automaker's ability to enforce the vendor selections in-house. GM's myriad divisions have traditionally exercised considerable autonomy in their equipment buying decisions, and have sometimes been at odds with Electronic Data Systems, GM's system integrator, which was acquired by the auto maker in 1984, over an allegedly heavy-handed approach to internal systems integration.

"There are groups within the traditional GM, not EDS, who would liked to have seen some other vendors included," notes Laura Conigliaro, an industry analyst with Prudential-Bache Capital Funding in New York. "This whole thing seems reasonably political to me."

Some at the Detroit show suggested that despite GM's considerable buying clout, its strategy could be risky in an industry that's already moving rapidly toward its own set of de facto and formalized standards. If other suppliers don't fall in line, the automaker could eventually find itself paying premium prices for C3-compliant systems that could be outside the industry mainstream.

But at GM, corporate manufacturing information manager Frederick R. Caffrey notes that the C3 program push will emphasize development of emerging standards that are in the industry mainstream. No one should doubt that the automaker is serious. "We've got the top officers of the corporation behind it," Caffrey says.

GM's decision, delivered at the show, sparked much controversy among industry officials, but its effect remains to be evaluated. Cadam and McDonnell Douglas were selected from a field of five finalists—the other three were Computervision, IBM, and Intergraph. (Though Cadam software currently runs almost exclusively on IBM equipment, the IBM bid was based on Dassault Systèmes's Catia software.) The process was administered by EDS.

By pruning vendors, GM could affect the industry's suppliers and standards

In the end, GM reached out to companies it already knew well. McDonnell Douglas teamed with EDS earlier to bid on a major Navy program and Cadam already claims the second largest installed CAD/CAM software base within GM at 28%—behind only GM's own Corporate Graphics System.

GM says the winners will work as strategic partners with EDS in a five-year software-development effort known as the C3 data pipeline (C3 computer-aided design, manufacturing, and engineering). The project is part of an overall scheme by GM to develop a set of internal hardware and software standards. Software developed under the effort will be portable among any of three engineering work station platforms—Apollo, Hewlett-Packard, and Sun.

The selection means that Cadam and McDonnell Douglas will work closely with EDS in developing GM specifications to be based on emerging industry standards, says Tony Affuso, division manager of technology for the EDS technical systems development group. The two firms will be the preferred vendors for new GM product programs over the next three years, Affuso notes. He adds, however, that "there are no volume [purchase] commitments stated" in the agreements. Executives at both Cadam and McDonnell Douglas say details such as the specific tasks and schedules under the partnership agreements have yet to be negotiated. "The GM supplier community has been flooding us with requests for information, telling us that all they wanted to know was who the partners would be so they know who to buy from to be fully compatible with GM," says David Owens, Cadam's director of marketing and business planning.

McDonnell Douglas sees similar benefits. "This is definitely going to help us gain additional market share among GM suppliers," says a company source, even if the agreement doesn't result in more direct GM business.

EDS plans to periodically update other vendors on the program's progress, Affuso explains. "After three years, we're planning to issue to the public our C3 data pipeline requirements. At that time, any C3 supplier out there who is able to conform his product to those standards we will entertain as GM/EDS suppliers," he says.

When the standards are published, GM expects that a number of other vendors will move toward compatibility. Within five years, GM plans to limit its purchases almost exclusively to software that complies with the C3 data pipeline guidelines. "Our strategy is definitely not to go around and unplug everything that is not supplied by one of the strategic partners," says Affuso. "And we definitely want to continue to use those other systems in an ongoing support and maintenance type of role."

Reaction from Intergraph and Computervision was subdued. Since GM is one of the world's largest buyers of CAD/CAM systems, this month's selections "have got to have a long-term impact," concedes Robert A. Glasier, executive director for Intergraph Corp. of Huntsville, Ala.

Thomas A. Charland, a spokesman for Computervison Corp., Bedford, Mass., says "This is obviously news that we didn't want to hear. But it's not real big news. It doesn't mean that we won't be doing business with GM anymore." *–Wesley R. Iversen*

GOVERNMENT

SEMATECH ISN'T OUT OF THE WOODS YET

WASHINGTON

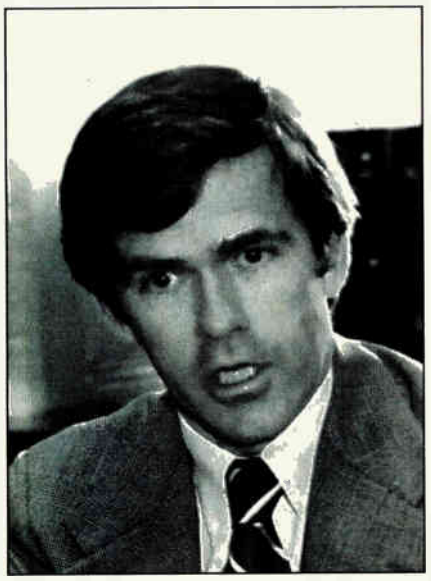
Trouble is brewing for Sematech. The proposed semiconductor research consortium may get only a quarter of the $100 million in federal funding that the industry says is needed to challenge foreign competition. Another timebomb: a congressional move to exert tighter government control over the consortium.

The strong possibility of Pentagon budget cuts is responsible for that prognosis from a leading consortium supporter, Sen. Jeff Bingaman (D., N. M.), chairman of the subcommittee that initially approved Sematech legislation.

Industry experts say that a reduced figure of $25 million would seriously hamper the Sematech project, which U. S. chip makers hope will develop advanced manufacturing technology. "The $100 million is required to meet Sematech's full task," says Bob Berger, a vice president at the Semiconductor Research Corp. in Research Triangle Park, N. C. "Anything less will not solve the [chip-manufacturing] problem."

The joint Senate-House defense authorization bill had already authorized $100 million for the endeavor [*Electronics*, Nov. 12, 1987, p. 122], but the consortium still faces another hurdle during the actual appropriation process.

As if that weren't enough bad news, a group of House Democrats led by Rep. Les AuCoin (D., Ore.) is fighting to change the liaison between Sematech and the government. Their plan would shift responsibility from the Department of Defense to an interagency committee chaired by the Secretary of Commerce—a setup that would give the government considerable power over Sematech. The Senate backs an alternate plan, which would establish a steering committee chaired by the Secretary of Defense. Opponents of the House plan say it would create unnecessary barricades in Sematech's path.



BINGAMAN: Sematech may get as little as $25 million rather than $100 million.

Just what this all means to Sematech's prospects is still unclear. But if the budget cuts are big enough, Sematech could be ambushed. "If disaster strikes" and Sematech gets just $25 million, "I think that's killing," says Ed McGaffigan, Bingaman's staff expert on the matter.

A Sematech spokesman, however, is more cautious. "We've been so confident that we would get the funding at the full level," he says, "that we didn't give much thought to finding a critical level" at which the project would not be viable. Sematech's financial fate hinges largely on the DOD budget. If Congress squeezes it to the Gramm-Rudman-Hollings level of $283.5 billion, "Sematech hangs on with its fingers—probably the $50 million level," McGaffigan says.

At $286 billion—the figure favored by President Reagan—Sematech would likely get full funding. The worst-case scenario would be if the President and Congress can't work out a package of tax hikes and spending cuts to eliminate the $23 billion mandated by Gramm-Rudman-Hollings: then Sematech would get only $25 million at best.

Under the original Sematech plan, chip-making companies would collectively kick in about $100 million, contingent on the government donation. With U. S. support so iffy, no one is sure about the industry contribution. For now, Sematech is operating with a skeleton staff borrowed from member companies on a modest budget in "the small millions of dollars."

AuCOIN: Seeking interagency council with "veto power over Sematech's plans."

The new House pressure on the management structure for overseeing Sematech further clouds the picture. Under the Senate-backed proposal, the Secretary of Defense would chair a committee that would have no direct control over how Sematech spends its money. But AuCoin is leading a charge for an interagency council with "veto power over Sematech's operating plans," according to Ron Fitzsimmons, an AuCoin aide.

That's not what the industry wants. "We like the terms and conditions that were included in the Senate plan," says a Sematech spokesman. "We think that the more complex the oversight requirements become, the more difficult it becomes for us to run our program." SRC's Berger adds, "The DOD is close to the technology. It seems to be more prepared to deal with our problems than other government agencies." *–Tobias Naegele*

CONSUMER

MOTOROLA RETURNS TO THE TV CHIP WARS

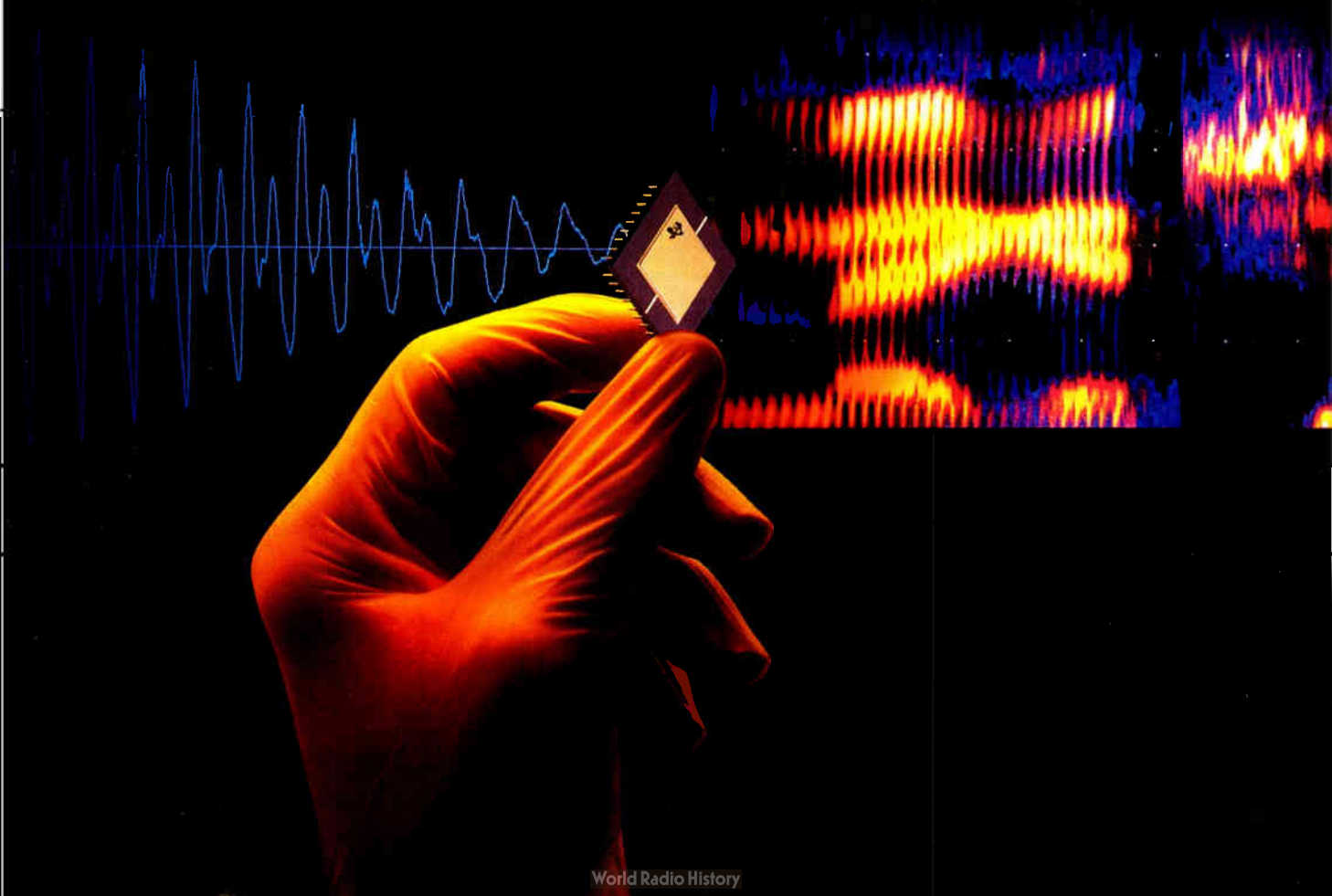
PHOENIX

Once a major supplier of chips for color television sets, Motorola Inc.'s Semiconductor Products Sector got pushed out of the game in the mid-1970s by the Japanese. But now it's dealing itself back in with a hand that it figures holds an ace which should appeal to cost-conscious manufacturers: a bus architecture in which single-chip digital parts, working under the direction of a selected Motorola microcontroller, replace several key analog functions requiring many components.

The move "could be a landmark or a turning point," observes William I. Strauss, president of Forward Concepts Inc., a Tempe, Ariz., market and process consulting firm. It is the first significant new entry by a U. S. chip producer into

TEXAS INSTRUMENTS REPORTS ON DSP

IN THE ERA OF MegaChip TECHNOLOGIES



from Texas Instruments in all sorts of places.

These advantages can make a difference in applications as wide ranging as modems, disk servo controllers, sonabuoys, and voice multiplexers to spectrum analyzers and graphics workstations.

Getting started in DSP design is easier with Texas Instruments training and support. But once you see what the TMS320 family can do, you'll want the features TI DSP can give your designs.

"Handling performance is up there next to speed in Formula 1 racing. TI's TMS320 gives us a real advantage — enough to win a Grand Prix." **Peter G. Wright, Technical Director, Lotus Engineering**

Lotus designed the active suspension in their Camel-Lotus-Honda Formula 1 car to approach the theoretical maximum-control point which gives the best balance between handling and performance. At racing speeds, each wheel is positioned by the TMS320-controlled hydraulics. A single TMS320 chip measures wheel forces and displacements and reads data from a body-mounted inertial platform. Then, in real time, the chip computes wheel position and controls actuators that adjust the suspension components to precise settings.

The TMS320 can also handle closed-loop engine control and more responsive braking systems, as well as many other automotive applications.

"The TMS320 helps us with one of our toughest tasks — designing toys with exciting features at prices that will sell." **Dave Small, VP Engineering, Worlds of Wonder, Inc.**

Worlds of Wonder is a pioneer in developing interactive toys and now has an innovative new doll named Julie™ Using a single TMS320 chip, Julie's designers are able to give her voice-recognition ability, coupled with synthesized speech and coordinated facial movement.

The TMS320 design expands the applications for affordable consumer products like solid-state answering machines, cellular phones, improved hearing aids, and animated electronic games.

TI's MegaChip Technologies

Our emphasis on volume manufacturing of high-density CMOS circuits is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip™ Technologies. They are the means by which we can help you and your company get to market faster with better, more competitive products.

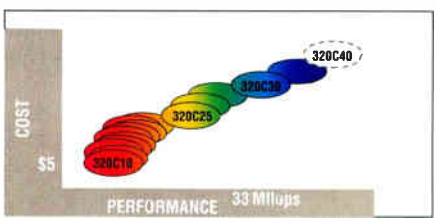
Winning designs come from a family of winners

There are 15 compatible members in the TMS320 family *(see the road map below)*, featuring two new DSPs with on-chip EPROM, the TMS320E15 and the TMS320E17. For applications requiring off-chip memory, there is the new CMOS EPROM, the TMS27C292, with 35-ns speed.

New interface alternatives include the low-cost CMOS TCM29C18/19 Combo Codecs with A/D, D/A, and filters all on a single chip.

The high-performance TLC32040 Analog Interface Circuit has 14-bit A/D and D/A and programmable filters.

For higher performance in digital signal processing, you can use building-block products like TI's microcodable ACT88XX 32-bit processor family.



From $5 to 33 Mflops: With three generations covering 15 products, the TMS320 family offers software compatibility to protect your development investment and provide a smooth path to future applications.

For more information on support for the TMS320 family, please turn the page.

From hands-on training to a "C" compiler, TI has the tools you need to get your designs to market fast.

Whether you're moving into DSP or moving up in DSP, Texas Instruments can help you move your design into production faster.
Hands-on DSP Workshops using the TMS320 development tools cover all you need to know from architecture to software. Courses are scheduled at TI Regional Technology Centers.
Get Started in DSP with the TMS320 Design Kit, which contains data sheets, chip samples, and applications notes to make starting easy.
Count on EPROM DSPs for realtime code development, form-factor emulation, and early production runs, with the option for last-minute changes.

Applications Notes and Textbooks contain literally thousands of pages that are readily available to give you assistance in application concepts and designs.
Optimizing "C" Compiler reduces your time to market and preserves your software investment.
The Assembler/Linker and Simulator speed software development for you.
Realtime In-circuit Emulators allow you to integrate software and hardware and give you a final check.

For more information on the Julie doll from Worlds of Wonder, Inc., call (415) 656-3171.

™MegaChip is a trademark of Texas Instruments Incorporated. Julie is a trademark of Worlds of Wonder, Inc.

More than 80 Third-party Hardware Suppliers and Consultants are featured in our *TMS320 Family Development Support Reference Guide* and in our DSP newsletter *Details on Signal Processing.*
TMS320 Bulletin Board is an on-line service that provides you with the latest technical and application information.

The TMS320 Technical Hotline is staffed by applications experts and is ready to take your call.

How to get a fast start

For more information on TI's TMS320 DSP family, call 1-800-232-3200, ext. 3508. Or use the coupon below.

Texas Instruments Incorporated
P.O. Box 809066
Dallas, Texas 75380-9066

SPR173EC700C

YES, please send me information on the following TI Digital Signal Processing products and support services:

- ☐ PR01: TMS320 DSP Products
- ☐ PR02: Analog Interface Devices
- ☐ PR03: ACT88XX 32-bit Processor
- ☐ PR04: TI Regional Technology Center Workshops

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TEXAS INSTRUMENTS

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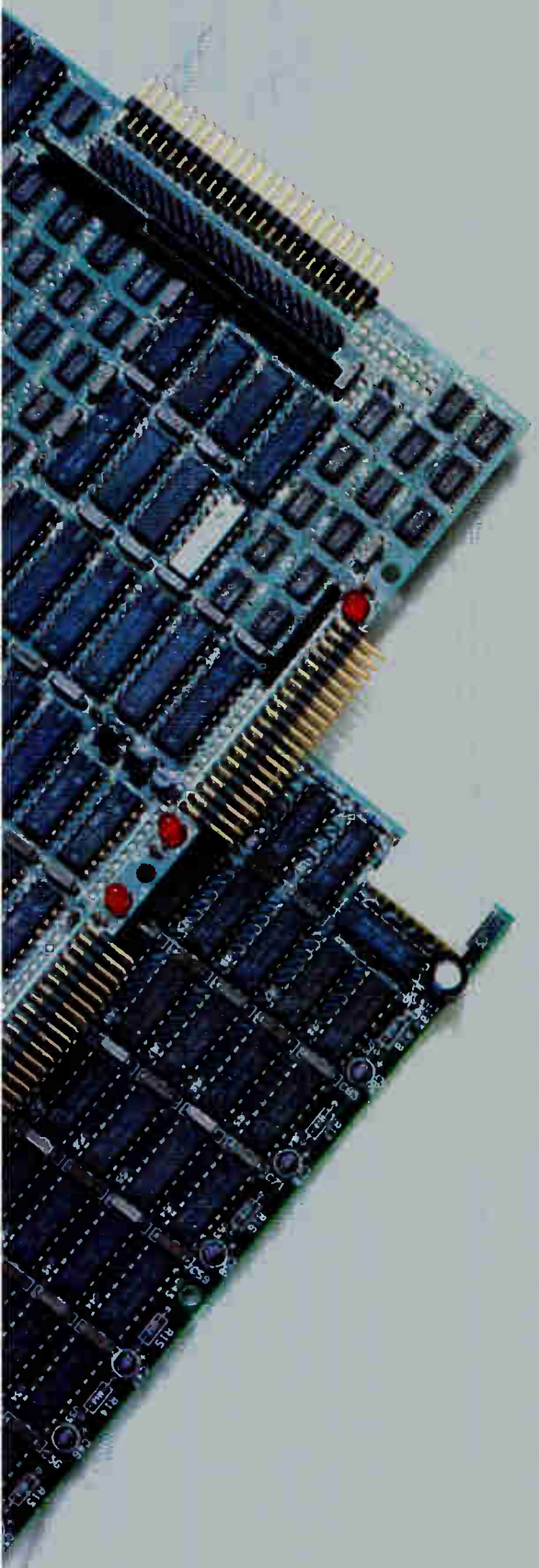

There's absolutely nothing else like the new TurboCache™ cache buffer system on the market today!

So, when you TurboCache your multi-user system, you'll notice the difference immediately. Here's why...

- TurboCache reduces the industry average data access time of 70 ms to 1.5 ms.
- Sends data as fast as the host adaptor is capable of receiving it.
- Completely self-contained — with its own memory and controller. Uses no main system resources and requires no main system processing time.
- Requires no software changes to either the system or user programs.
- The software provided for communication through the RS-232 is screen-oriented and menu driven with "help" available for all options.
- Simple plug-in boards install up to 35 feet from the host adaptor...AND...up to 35 feet from the disk controller.
- Stores up to 3,073 disk areas.
- "Transparent" operation.

TurboCache is a unique storage subsystem that installs quickly and easily between the host CPU and the SASI/SCSI controller.

The minimum TurboCache configuration of 2 megabyte capacity consists of a CPU board containing the processor and bus interface and a 2 megabyte random access memory (RAM) board. Capacity is increased simply by adding memory boards — up to a maximum of 8 boards or 16 megabyte capacity.

That's TurboCache. And that's why it'll significantly increase your system's productivity and cost efficiency.

Now that you have all the facts, don't delay. Add on TurboCache today — *and lose wait fast!*

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Circle 47 on reader service card

Only one company has the technology, the resources, and the vision to top the 68020.

Introducing the 68030.

The next generation.

In 1984, we introduced the 68020. Now, three years later, it has the largest installed and broadest application base of any 32-bit MPU on the market. Having set that standard in the first place, we feel qualified to raise it. Which is why the only microprocessor that really surpasses the 68020 is our second generation 68030.

Meet the *oh thirty!*

The '030 is twice the microprocessor its predecessor is. It's the first to sport an instruction cache, data cache and MMU on-chip. Combined with a Harvard-style parallel bus architecture that allows simultaneous, multiple fetches of instructions and data, processor throughput is pushed to unmatched levels.

What can you do with all that performance? Anything you like—from low-cost personal workstations to super-computers—and the 68030 will help you to do it less expensively.

With its burst fill mode for the dual caches, you'll be able to squeeze SRAM performance from low-cost DRAMs. It gives you graphics capability without the need for a graphics co-processor. And there's true object-code compatibility between the '030 and the '020. All this adds up to economies you can count on.

An architecture you can build on. And count on.

Application software that runs on any 68000 family MPU runs on the 68030. There's also a full array of development tools, and a new 68882 floating point co-processor, with up to 4x the performance of its predecessor. All of which gives your product plans an enormous amount of continuity. And that's not going to change. Since the 68030 supports both MS-DOS™ and UNIX® V.3, you can have your pick of over $12 billion worth of applications— and the broadest possible market.

With Motorola, you can see forever.

Our plans for the rest of the 68000 family extend well into the future, offering continuing compatibility and leading-edge performance. So you can go with Motorola, not just for what our microprocessors can do now, but what you'll be able to do with them later on.

For more information about the new 68030, call us toll-free at 800-521-6274 or write, Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

We're on your design-in team.

MOTOROLA

To: Motorola Semiconductor Products, Inc. 345ELEX112687
P.O. Box 20912, Phoenix, AZ 85036

Please send more information on the *oh thirty!*

Name _____

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Company _____

Address _____

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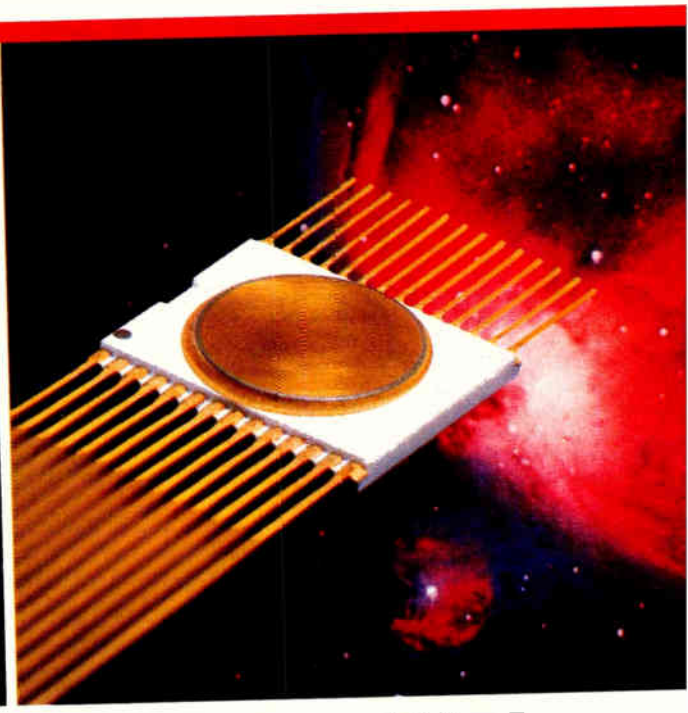
broader line of rad-hard products.



RCA Logic

We've long been the leader in High-Rel rad-hard logic, with the time-tested CD4000 series, with more than 100 functions, and total dose tolerance of 10^6 Rads (Si).

Now we've got a new high-speed rad-hard logic series that's an outstanding drop-in, low-power replacement for bipolar LS and ALS circuits. These circuits are as fast as ALS with only a fraction of the quiescent current.

For example, our new HCTS240 octal buffer has a quiescent current of only 5μA, SEU immunity, latch-up immunity, insensitivity to neutron irradiation, and a transient-upset rate $>10^{10}$ Rads/second. It's available now in volume.

And we'll be introducing many new devices this year, including a 4-bit counter, an octal buffer/line driver, a dual JK flip-flop and a hex inverter.

RCA 16K RAMs

We're delivering rad-hard 16K static RAMs, screened to Class S, in high volume.

These 16,384 x 1 RAMs are latch-up free; have SEU of $2x10^{-9}$ errors/bit/day; a transient upset rate $>10^{10}$ Rads/second; and total dose tolerance >100K Rads (Si).

Add to this access time of 125 ns (80 ns typical) at 25°C (post-RAD access of 150 ns), and the wide CMOS operating temperature range of -55°C to +125°C, and you can see why we're producing these RAMs as fast as we can.

We also offer 4096x1 and 1024x4 rad-hard SOS CMOS static RAMs, which are being qualified to M38510 Class S.

So if you need rad-hard memories, or any other rad-hard devices, there are only three things you need to remember: CMOS/SOS; GE Solid State—the technological leader; and our toll-free number 800-443-7364, extension 18.

GE Solid State

GE/RCA/Intersil Semiconductors

These three leading brands are now one leading-edge company. Together, we have the resources—and the commitment—to help you conquer new worlds.

EXIT.

Sit at your workstation. Enter an image. And exit with color hardcopy. That's all you have to remember about compatibility with a Seiko Color Hardcopier.

Because it doesn't matter what workstation you work with—Sun, Apollo, H-P, DEC, IBM, Silicon Graphics or one of 50 others. Our hardcopier works with them all. Without forcing you to write any software.

Plus, Seiko Color Hardcopiers are the only ones that let you connect up to 4 dissimilar systems to it at the same time. Making it a very cost-effective shared resource.

Of course, there's a lot more to the story. Like colors—thousands of them. And proven installations—thousands of them, too.

So exit this ad and enter our phone number. We'll be happy to show you how to get the industry's best looking color hardcopy from any workstation you use.

Call Martin Nelson at
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SEIKO

Seiko Instruments USA

Circle 59 on reader service card

INTERNATIONAL NEWSLETTER

UK PLANT LETS LSI LOGIC MOVE FAST INTO ANALOG ASICS AND BICMOS...

Little notice was taken last year when LSI Logic Corp. bought a wafer-fab plant from STC plc, a London-based telecommunications company. But the acquisition is letting LSI Logic move quickly into two hot areas: ASICs that mix analog and digital functions on a single chip, and biCMOS process technology. Until the acquisition, the Milpitas, Calif., company had stuck to all-digital gate arrays built with CMOS. Now its UK affiliate, LSI Logic Ltd., based in Bracknell, is opening up a biCMOS fab line located in Sidcup. The plant will become LSI Logic's world center for high-performance biCMOS devices, says Robert Blair, managing director of LSI Logic Ltd. The biCMOS process technology was developed by STL Ltd., STC's research arm in Harlow. STC, following a change in management thinking and experiencing a cash crisis, last year offered the plant and biCMOS process to LSI Logic for a relatively low cash figure and an 18% stake in LSI Logic Ltd. □

...AND ITS FIRST PRODUCTS WILL MIX ANALOG TILES WITH DIGITAL GATES

LSI Logic Ltd.'s first biCMOS products, application-specific integrated circuits with a mix of analog and digital functions, are slated to go into production at the end of the second quarter of 1988. Products in the LAD 310 line will be similar to digital gate arrays but will also carry analog "tiles," as they are called. Each tile comprises an uncommitted array of nine bipolar transistors, a programmable resistor, a programmable capacitor, plus one n-MOS and three p-MOS transistors. Complexity will range from a low-density part carrying 1,100 digital gates and 60 analog tiles to arrays of 114,000 gates and 492 tiles. A polysilicon emitter structure is used in the bipolar transistors, which have a gain bandwidth (f_T) of at least 4 GHz. □

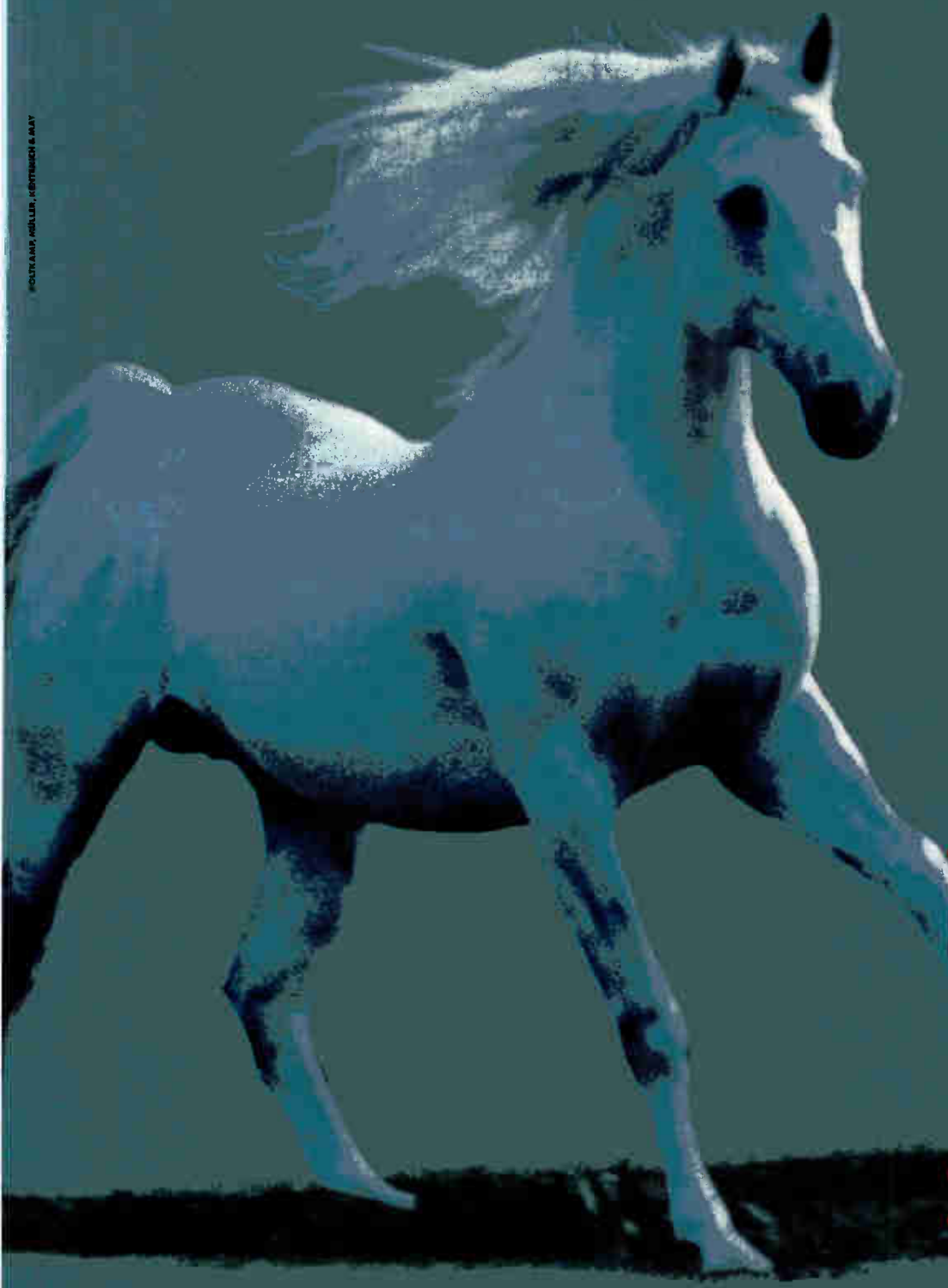
EUROPEANS WOULD LIKE TO PUT AN ENTIRE TELECOM SWITCH INTO ORBIT

The Technical Center of the European Space Agency is investigating sending into orbit an entire telecommunications switching system—not just a collection of relay transponders. Estec has awarded contracts to three European companies to develop designs. The aim is to produce a 16,000-line fault-tolerant time-division digital switch for telephone, data, and video transmission. Designs should be ready by September 1988. The agency's Technical Center, based in Noordwijk, the Netherlands, awarded about $350,000 in contracts to Advanced Systems Architectures Ltd., Camberly, England; Telespazio SpA, Rome; and Itelsa SA, Madrid, a subsidiary of Sweden's LM Ericsson. The British company will manage the project and design the switch and ground-station equipment. Telespazio will concentrate on the system's radio-frequency segments. Intelsa will be responsible for the master control station that handles call routing. □

IBM JAPAN GEARS UP THIRD-PARTY SOFTWARE PROGRAM

Hoping to encourage sales of IBM computer systems in Japan, IBM Japan Ltd., Tokyo, is launching a new operation to sell software developed by other companies. IBM Japan will select products of software types it does not offer itself, then sell them in cooperation with the software vendors. The company says it is now working on five such packages. The first, announced earlier this month, is a two-year-old suite of tools from Software Assist Inc., Tokyo. The package is for developing software for a range of processor chips, from 4-bit microcontrollers to 32-bit microprocessors. It runs on IBM 370-architecture mainframes and IBM's RT-PC work station. Software Assist has already sold 450 sets of the cross-development tools, which include assemblers, compilers, and debuggers. □

ABOUT THE SPEED AND RELIABILITY OF TOSHIBA OPTO COUPLERS.



Among animal lovers, white thoroughbred Arabs are regarded as the finest example of the Equus genus. Toshiba opto couplers share more than just hereditary reliability and outstanding speed with these noble creature – for instance, the 6N series with a switching speed of up to 10 MB/sec. They also have the colour white in common – Toshiba's white moulding ensures a high current transfer ratio and high isolation voltage.

In other areas, too, Toshiba semiconductor technology is setting standards: from memories via GTR modules, LED lamps, CPU's, custom IC's, bipolar IC's and transistors down to CMOS logic. Tell us about your problems and needs. You won't have to wait long for an answer.

☐ Please send me detailed information on Toshiba opto couplers

☐ and on _____

☐ I wish to arrange a visit from one of your engineers, without any obligation on my part.

Name: _____

Company: _____

Telephone: _____

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Tomorrow

TOSHIBA

Toshiba Europa (I.E., GmbH, Electronic Components Group, Hansaallee 181 – 185, D-4000 Düsseldorf 11, West-Germany, Tel. (0211) 5296-0, Telefax: (0211) 5296-404 Büro München Arabellastraße 33, D-8000 München 81, West-Germany · Stuttgart Office, Eltinger Straße 61, D-7250 Leonberg, West-Germany · Toshiba U.K. Ltd., Toshiba House, Firmley Road, Frimley, Camberley, GB-Surrey GU 16 5JJ, England · Toshiba Europa I.E. GmbH, Paris Liaison Office, four de bureaux de Rosny 2 Avenue de General de Gaulle, F 93118 Rosny Sous Bois, France Toshiba Electronics Italiana S.r.l., Centro Direzionale Colleoni, Pallazzo Andromeda Ingresso 1°, I-20041 Agrate Brianza Milano Italy · Toshiba Electronics Scandinavia AB, Box 438 S-101 25 Stockholm, Sweden.

Circle 190 on reader service card

INTERNATIONAL WEEK

ALCATEL TO SUPPLY FIBER DOWN UNDER

Submarcom, a unit of Alcatel NV, Europe's largest telecommunications concern, bid 100 million Australian dollars to win a contract for linking Australia and New Zealand with optical fiber cable. It is the initial part of an undertaking to link Down Under with the U.S. and Southeast Asia by 1995. The 2,500-km project will provide 565-Mbit/s fiber links operating at 1,500-nm wavelengths and carrying more than 20,000 digital circuits, the company said. The contract, with the Overseas Telecommunications Commission of Australia and the New Zealand Telecommunications Authority, will be signed Dec. 15.

SONY, PHILIPS TEAM ON WRITE-ONCE CDs

Sony Corp, Tokyo, and Philips of Eindhoven, The Netherlands, have agreed on basic specifications to be used for a compact-disk write-once system. Based on the CD digital audio system jointly developed by the two companies, the new specifications, available in January, include groove and tracking characteristics, a writing speed of 1.2 to 1.4 m/s, a track pitch of 1.6 μm, a capacity of 600 Mbytes of data—approximately 60 minutes of audio. The two firms expect the new system will be used for data storage, with the ability to play conventional data CDs, and for professional audio recording, with the ability to play current audio CDs.

WRITE-ONCE OPTICAL DISKS GET FORMATS

The International Standards Organization has accepted two tracking methods, sampled servo tracking and continuous groove servo tracking, for 130-mm write-once optical disks. The two methods were both part of a draft proposal submitted to last month's ISO meeting in Washington by Japan's Ministry of International Trade and Industry. The sampled servo tracking method was jointly proposed by Sony, Alcatel-Thomson Gigadisc, the Optical Storage International Division of Laser Magnetic Storage International, and Philips and Dupont Optical Co.

EPSON ATTACKS NEC LAPTOP PCs

Seiko Epson Corp., of Suwa, Japan, hopes to take market share from NEC Corp, Tokyo, by introducing three laptop personal-computer models that can run more software products developed for NEC's popular desktop PCs than can NEC's laptop PC. The three models—PC-286L-STD-S, STD-N, and H10-N—have a 256-Kbyte graphic memory and a color cathode-ray tube interface, making them compatible with NEC's desktop PC-9801UV series, which use 3.5-in. floppy disk drives. Seiko Epson will start marketing the STD-S and STD-N at the end of this month at 318,000 yen and 348,000 yen, respectively. Both have 3.5-in. floppy disk drives, but the STD-S has a green LCD and the STD-N has a white LCD. The H10-N, which will go on sale for 468,000 yen at the end of December, will have a 10-Mbyte hard disk drive and one floppy drive with a white LCD.

PHILIPS LANDS BIG POST OFFICE ORDER

Philips of The Netherlands has signed an $85 million contract with the Dutch government to automate teller services at the country's post offices. The contract provides for the Eindhoven-based firm to supply more than 3,800 teller terminals and 150 terminal computers worth a total of $57 million. Accounting for the remaining $28 million are installation, service in the coming years, and joint software development. The project should be completed by the end of 1989.

BOSCH AND PHILIPS SET CELLULAR TEAM

Add another consortium to the growing list of partners in communications equipment determined to cash in on Europe's potentially lucrative cellular radio market. This time it's West Germany's Robert Bosch GmbH and ANT GmbH as well as Philips of The Netherlands who are planning to team up in developing a digital cellular system. At stake is a border-crossing system operating in the 900-MHz range that 13 European countries have decided to introduce in 1991, with bidding to start next year. The formation of the Bosch-ANT-Philips consortium follows the recent agreement by France's Alcatel and Finland's Nokia Group to embark on a similar venture [*Electronics*, Nov. 12, 1987, p. 54E].

GERMANS, SWISS GET VIDEO LINK

A 2-Mbit/s video codec from Philips Kommunikations Industrie AG, a Philips subsidiary, links West Germany's 140-Mbit/s data network with Switzerland's 2-Mbit/s lines to provide video conferencing between the two countries. The PKI video codec compresses the 140-Mbit/s bandwidth 70 times to the 2-Mbit/s rate to allow video communications with sufficient picture quality. West Germany is one of Europe's few countries working with 140-Mbit/s lines. Most others have 2-Mbit/s lines.

SIEMENS, DEC TEAM IN DATA SWITCHES

West Germany's Siemens AG, with Digital Equipment GmbH as subcontractor, has won an order from the Bundespost, the country's communications authority, to install seven EWSP-V data-switching systems. These switches will link text and data nets with integrated services digital networks and offer users value-added services such as intermediate storage of calls and message-handling functions for electronic mail. Siemens will implement the service and network interfaces while DEC will take care of message-handling functions. The EWSP-V is based on Siemens's high-performance packet-switching system EWSP, a system that can switch up to 40,000 data packets per second.

INDIA TO PRODUCE APOLLO COMPUTERS

HCL Ltd., India's largest computer manufacturer, will be the first to make work stations in India. The company has signed an agreement with Apollo Computer Inc., the Chelmsford, Mass., manufacturer of work stations, to make Apollo's series 3000 in its facility outside New Delhi. By January 1988, HCL expects to begin delivering about 500 work stations a year to its Indian customers, and eventually to expand its production up to some 2, 000 units a year.

INTEL MAY ADD PLANT IN ISRAEL

Intel Corp., of Santa Clara, Calif., is negotiating to build another large plant in Israel, government officials say. The proposed $80 million plant would make and assemble semiconductors. To take advantage of Israel's customs-free export agreement with the European Community, some assembly work would be transferred from Intel's assembly plant in the Philippines. Most of the production would be exported, as is the case with Intel's existing wafer fabrication facility in Jerusalem. Intel had no comment about the proposed Israeli plant.

OLIVETTI MINIS DELIVER UP TO 9 MIPS

By configuring its new minicomputer line with standard hardware and operating systems, Ing. C. Olivetti & Co. is offering cost-conscious buyers a family that offers top-end performance of 9 million instructions/s for $400,000. Systems using proprietary circuitry may offer higher performance, but they cost much more.

Based on Motorola Inc. 68020 microprocessors, the engines in the Ivrea, Italy, company's LSX 3000 line deliver performance ranging from 1.5 to 9 mips—and cost from $15,000 to $400,000. Except for the smallest model, which is a no-frills work station, the models run operating systems based on Unix Version 5 with some additional features, like robust C-language server modules from the Berkeley 4.2 version of Unix.

All but the two largest machines in the line offer as an option the proprietary Multifunction Operating System, so that users of existing Olivetti minis won't lose their software investments.

Olivetti's open-architecture strategy is designed to boost it from eighth place in Western Europe's minicomputer market into the top four over the next five years, says Giovanni Gurrieri, director for Systems and Networks marketing. Gurrieri notes that work stations tied into LSX 3000 mini systems will probably have MS-DOS operating systems. Although even the smallest of the minis can support up to eight work stations, he figures the average system will have four or five work stations tethered to each minicomputer. Olivetti will offer networking standards like StarLAN and Ethernet. Possibilities for wide-area networks include Open Standards Interconnection, packet-switched public networks, and IBM's Systems Network Architecture.

The bottom-of-the-line LSX 3005 can handle up to eight work stations. It has a single processor and a system bus speed of 10.6 Mbits/s. Internal memory starts at 2 Mbytes and can run up to 14 Mbytes; there is no cache memory. The possibilities for mass storage range from 20 to 140 Mbytes. The LSX 3010 is similar, but handles 16 work stations and has 220 Mbytes of storage.

Moving up the line, a trio of machines runs at 16-Mbit/s bus speed and has cache memory, a floating-point coprocessor, and mass storage from 70 Mbytes to 1.28 gigabytes. The single-processor LSX 3020 runs at 2 mips and can handle up to 32 work stations; the LSX 3030 has two processors, supports up to 48 work stations, and runs at 3.5 mips; and the 5-mips triple-processor LSX 3040 can handle 64 work stations.

At the top, are two systems with 61.5-Mbit/s system-bus speed and internal memory as large as 3.78 gigabytes. The single-processor LSX 3070 runs at 5 mips and can handle up to 96 work stations. The twin-processor LSX 3080 runs at 9 mips and can handle up to 192 work stations. Its maximum memory capacity is 3.78 gigabytes.

The 3010, 3020, and 3070 models are available now. The others will be available in the first half of 1988.

– *Arthur Erikson*

Ing. C. Olivetti & Co., Via Caldera 21, 20153 Milan, Italy.
Phone 39-2-45273-1 . [Circle 501]

DOT-MATRIX DISPLAY WITHSTANDS 100° C

The MPD2545/47 matrix displays from Siemens AG cover a temperature range from −55°C to +100°C and feature 6.4 mm-high symbols that can be read from a distance of 4 m. Their viewing angle is ±50°.

Designed for aerospace applications, the hermetically sealed units offer up to four digits with a 5-by-7-dot matrix. The MPD2545 emits orange light and the MPD2547, green light. The test program complies with the MIL-STD-D-87157 standard.

Integrated into the displays are a memory, decoder, multilexer, and driver.

The devices are available as samples at $180 apiece for the MPD2545 in 100-unit lots and at $190 apiece for the MPD2547, also in 100-unit lots. Prices are expected to drop sharply next year.

Siemens AG, P.O. Box 103, D-8000 Munich 1, West Germany.
Phone 49-89-2343613 [Circle 703]

80386-BASED PC RUNS AT 16 MHz

The CEM 386 personal computer from Cemtech Ltd. integrates a 16-MHz Intel Corp. 80386 microprocessor with high-end operating software that includes multiuser/multitasking Unix System V Release 3 and DOS Merge 386 from Microport Systems Inc.

Single-user MS DOS is also part of the standard package. The 80386 motherboard includes two serial ports and one parallel communications port. It can accommodate either an Intel 80287 or 80387 math coprocessor and runs at 16 MHz with zero wait states.

On-board ROM-BIOS is fully compatible with the IBM Personal Computer AT, and the board also offers two add-on slots compatible with 8-bit IBM PC/XT systems, four 16-bit AT slots, and two 32-bit add-on slots.

The CEM 386 is available now. Price including a 44-Mbyte hard disk, CGA graphics controller, and software is $3,900. U. S.

Cemtech Ltd., 220 Laurier Ave., W., Suite 750, Ottawa, Ontario, Canada K1P 5Z9.
Phone (613) 232-2600 [Circle 701]

SHIELDED CONVERTERS MINIMIZE NOISE

Multiple-layer shielding on five sides of the package eliminates electromagnetic- and radio-frequency emissions in the MMC Series of dc-to-dc converters from Volgen Electric Co.

For added versatility and space saving on pc boards, the converters also offer a low profile and small package size. They measure 10 mm high, and 36.4 mm on each side.

Input voltage is 5 V for both units in the family. Output voltage is 12 V ±0.36 V for the MMC03B-DDW and 15 V ±0.45 V for the MMC03B-EEW. Maximum power is 3 W and maximum rise

time, 50 ms. Available now, the converters carry a sample price of 2,500 yen.

Volgen Electric Co., 4-12-5 Meguro, Meguro-ku, Tokyo 153, Japan.
Phone 81-3-710-5179 [Circle 702]

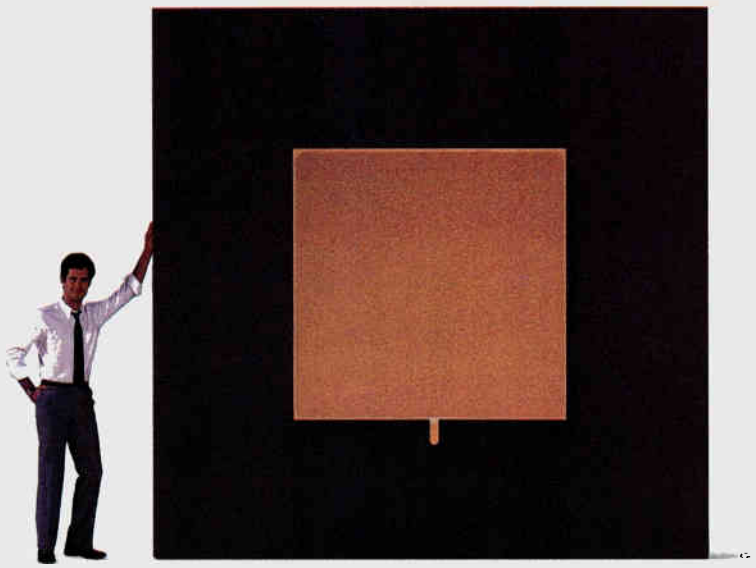
BOARD COMPUTER USES 68030

Tadpole Technology plc's TP30V single-board computer for the VMEbus combines the performance of a 16-MHz Motorola Inc. 68030 microprocessor with proprietary memory-control circuitry and 8 Mbytes of dynamic random-access memory.

The dual-port memory is parity-protected. The board supports Tadpole's version of AT&T Co.'s Unix System V version 3.1, and support for TCP/IP communications is available as an option.

On-board features include two RS-232-C ports, a battery-backed real-time clock and 2 Kbytes of static random-access memory. Its VME Subsystems Bus—the VSBbus—provides fast processor-to-memory communication by offloading

A LOT OF PEOPLE THINK WE ONLY HANDLE GIANT PROJECTS.



The entire state of New Jersey on a chip.

EVEN THOUGH WE OFFER 100,000 GATES, YOU DON'T HAVE TO USE THEM ALL.

It's no wonder people expect big hings from LSI Logic.

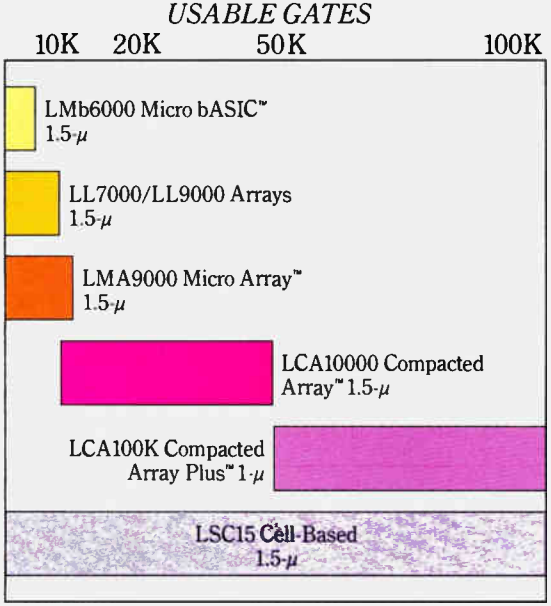
We're the largest HCMOS ASIC company there is.

But that doesn't mean you have to be he largest in your field o come to us.

You just need to be doing ASIC. No matter f it's a few hundred gates or a complete system on a chip. Or even a multi-ASIC system.

It's plain and simple, really: We understand your ASIC might not need 100,000 gates today. But it's good to know it's here when you need it.

To simplify your ASIC design task, we have the largest library available of SSI and MSI building blocks. And more than 400 industry-standard LSI and VLSI building blocks for Channeled and Channel-Free™ Arrays, and Cell-Based designs.



LSI Logic's family of products covers the entire ASIC spectrum.

So whether you need an array or cell-based product, you're covered.

If you change methodologies, you don't have to re-design or change vendors. Or worse, change design tools. Simply, our design tools support both.

There's something else you won't get anywhere else. Our turnaround for prototypes.

It's only two to three weeks for arrays and five to six weeks for cell-based prototypes. All fully tested and guaranteed to work to your specifications.

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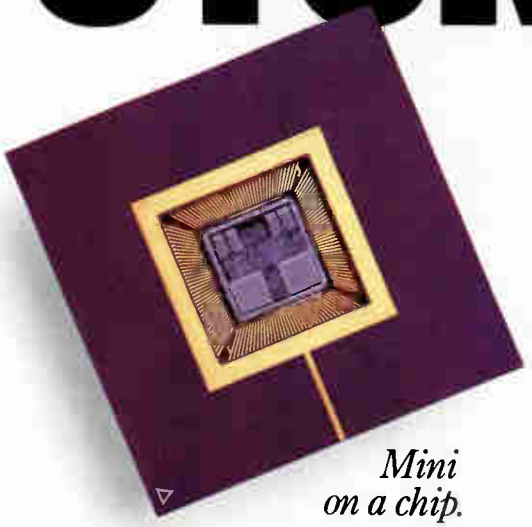
So don't worry about how big or small your ASIC need is. We're the right size for you.

WE HAVE SEEN THE FUTURE.



Mini on a chip.

AND IT IS VERY TINY.

Saying our new Modular Design Environment (MDE)™ is the most advanced ASIC design software anywhere isn't small talk.

Using MDE, we've already accurately designed and simulated systems with more than two million gates of logic. And that's just for starters.

Our software easily migrates into the latest technology. So your design will always have the highest performance and densities.

MDE is actually comprised of three modules.

The *Logic Integrator*™ is an entry-level module containing the design and simulation tools for building single ASIC chip designs.

The *Silicon Integrator*™ module handles the design and simulation of complex ASICs ranging from a few hundred to 100,000 usable gates. Its Silicon Compilers allow you to automatically develop logic and memory. Your compiled designs, of course, all have complete simulation and test vectors.

MDE's interactive graphics deliver fast, flawless design and simulation.

You can also effortlessly convert PALs to arrays with our Logic Synthesizer.

Our *System Integrator*™ module has mixed-mode behavioral and gate-level simulation capabilities. Use it to design your entire system, including multiple ASICs and standard components.

All with surprising ease and economy. So you can "electronically breadboard" your complete system before going to prototype.

And you can design your ASICs on more platforms than anywhere else. Like all the popular workstation and mainframe environments. Or commercial CAE systems through our CAD Connection Program. Or at one of our 24 Design Resource Centers—the world's largest ASIC support network.

MDE is also tightly coupled to our worldwide manufacturing facilities. Which is why LSI Logic delivers working parts 100% of the time. Guaranteed.

And why you'll see your future a lot sooner with us.

With more than 4,000 working designs under our belt, one clear fact emerges.

Our system works.

That's true whether your needs call for an entry-level gate array or cell-based design. Or for the world's most advanced ASIC-based system.

Whatever direction your designs take, you can always use the same proven software: LSI Logic's MDE.

MDE can be tailored to your specific situation. Just select the appropriate design modules.

We have all the performance you'll need. Such as ECL-like speed in 1 or 1.5-micron HCMOS technology with gate delays of 460 picoseconds. And even more coming soon.

We also have more than 230 package options with up to 299 pins. Including a full range of plastic, ceramic pin grid arrays and chip carriers.

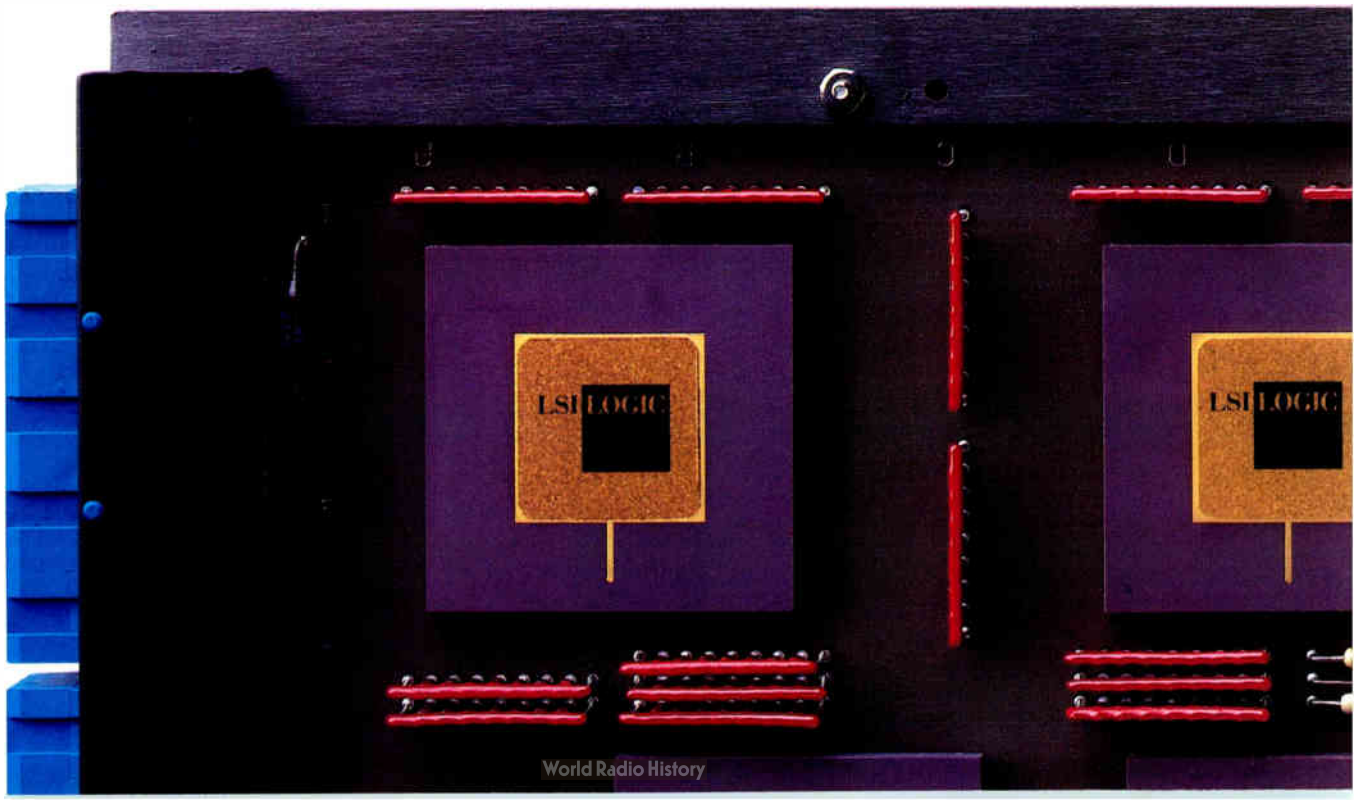
Just as important as our high level of technology is our high level of service. Choose as much as you need. You can design at your own workstation. Or at one of our Design Resource Centers. Or we'll do the entire design for you.

What's most important is that our relationship with you works as well as your device.

We see to it that it does. With an iron-clad guarantee that states that your device must operate precisely as simulated.

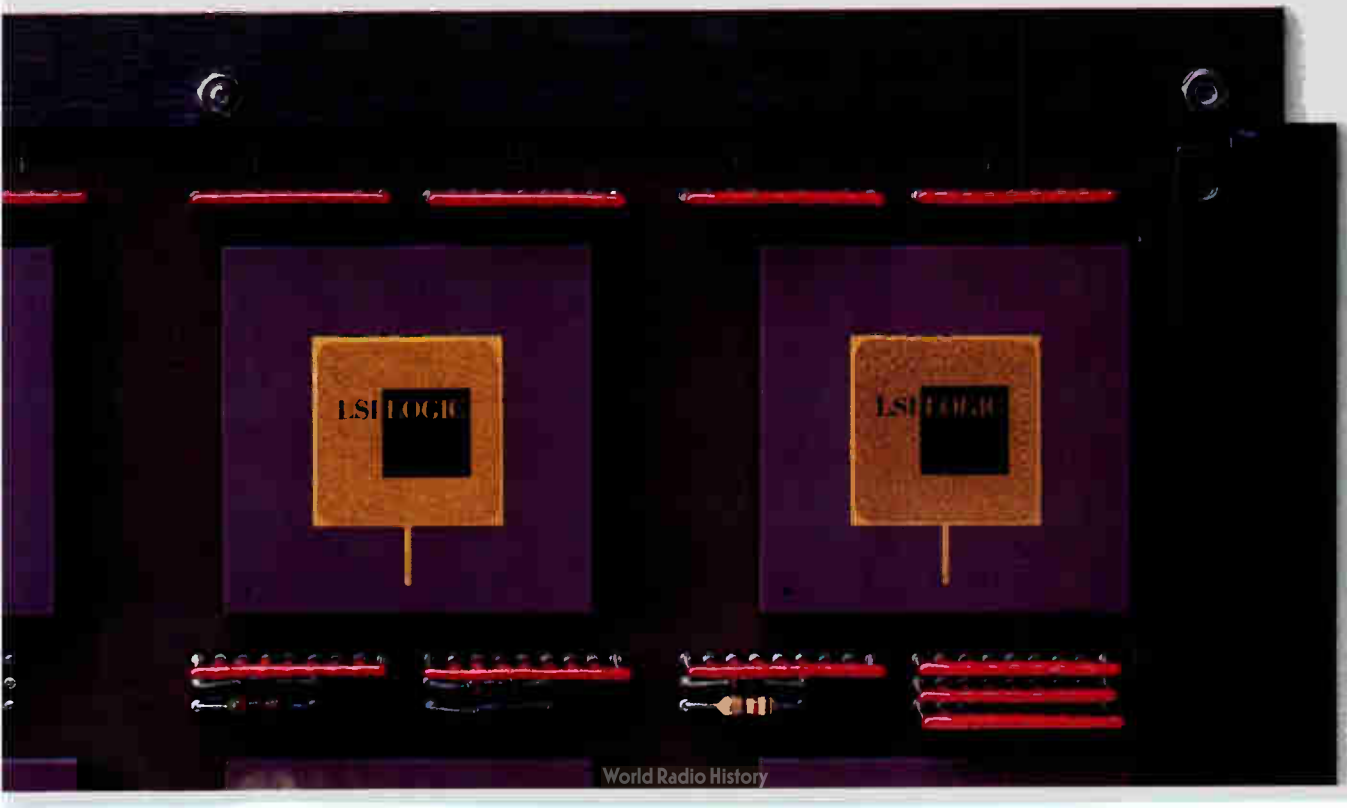
That's our system.

You can't beat it.



WE HAVE ASIC DOWN TO A SYSTEM.

Supercomputer on a board.



CALL US WITH EVEN YOUR SMALLEST PROBLEM.

Sure, we handle the biggest ASIC projects. But you don't need a big reason to call LSI Logic.

It can be about designing a low complexity part or buying a small quantity of parts.

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Our unique integrated approach means we're the only ASIC company you should ever need. And our worldwide manufacturing facilities are dedicated to ASIC. Which means you can quickly turn your designs into working parts.

Contact your nearest LSI Logic Design Resource Center or Sales Office. It's a small step that will lead to much bigger things.

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HEWLETT PACKARD

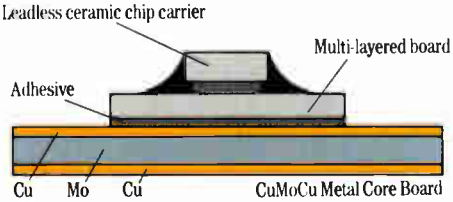
Circle 71 on reader service card

Which core mate keep their cool in

Copper-Clad Invar

High density surface mounting of leadless ceramic chip carriers has created new thermal and mechanical problems for those working on high reliability electronic projects.

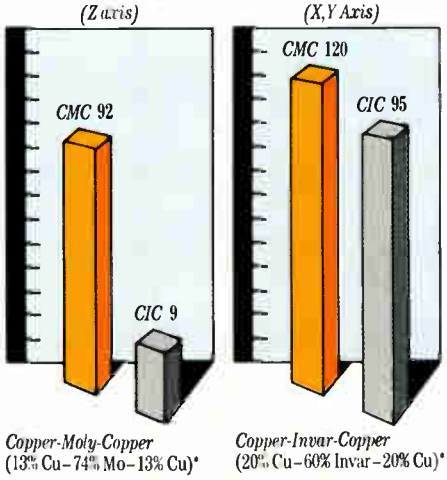
More and more companies are addressing these problems by incorporating metal cores as thermal mounting platforms in their printed circuit board assemblies. The choice of metal laminate comes down to two: Copper-Clad Molybdenum or Copper-Clad Invar. Both do an equally good job of solving the problem of the coefficient of thermal expansion (CTE) mismatch between chip carrier and substrate. But, that's where the similarity ends.



Dissipating the heat.

Higher packaging densities create higher watt densities. Dissipating this heat can be as critical as matching the CTE of an assembly. The thermal conductivity of Copper-Clad Molybdenum is comparable to aluminum and much higher than Copper-Clad Invar, making it a superior heat sink. Compared to Copper-Clad Invar, Copper-Clad Molybdenum is 25% more conductive in the x and y axis, and 900% more conductive in the z axis!

Comparison of Thermal Conductivity
(BTU/hr-ft F°)



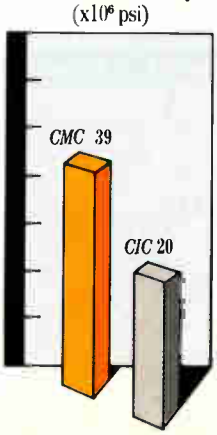
rial helps LCCC's heated situations?

Copper-Clad Molybdenum

Providing mechanical rigidity.

Solder joint failures also can be caused by vibration, shock, and flexure. Copper-Clad Molybdenum has a much higher modulus of elasticity than Copper-Clad Invar. A core of Copper-Clad Molybdenum provides maximum rigidity to the chip carrier assembly.

Comparison of Modulus of Elasticity ($x10^6$ psi)



Copper-Moly-Copper
(13% Cu–74% Mo–13% Cu)*

Copper-Invar-Copper
(20% Cu–60% Invar–20% Cu)*

Saving weight and space.

Since it is substantially stiffer and a better thermal conductor than Copper-Clad Invar, a Copper-Clad Molybdenum core can be thinner and lighter. That makes it possible to reduce the overall assembly's weight and size.

Lowering magnetic susceptibility.

For some applications, magnetic susceptibility is a design consideration. Molybdenum is only slightly paramagnetic (4×10^{-6} emu/g), whereas, Invar is a ferromagnetic material (100+ emu/g).

**The necessity for equivalent CTE's is the criterion for comparison.*

Contact us today.

For more information about Copper Clad Molybdenum, contact AMAX Specialty Metals Corporation at:

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AMAX SPECIALTY METALS
AMAX Minerals+Energy

Circle 75 on reader service card

68000™ FAMILY UPDATE NO. 3

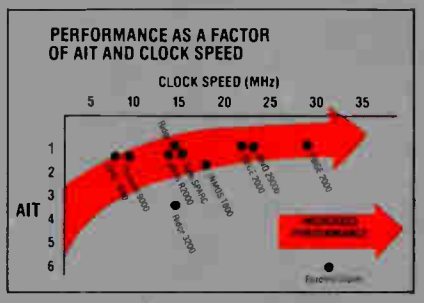
NOVEMBER, 1987

"CISC VS. RISC" DEBATE IGNORES KEY ISSUES OF SYSTEM SOFTWARE AND ON-GOING SUPPORT COSTS

The continuing debate over whether CISC or RISC technology is the answer to boosting computer performance levels tends to focus on machine speed, often ignoring an equally important issue: architectural compatibility. Computer manufacturer's with 68000-based CISC architectures considering a move to RISC technology for their high-end product offering need to recognize the enormous costs they face. Current systems software must be adapted and supported on different architectures. Two different operating systems as well as diagnostics have to be ported and supported. Compilers for high level languages need to be developed. And these are just a few of the obstacles.

The EDGE 2000 Series VME board set recently introduced by Edge Computer proves that a 68000-compatible CISC system can operate with RISC-like efficiency. But performance is only one side of the coin. Value and the ability to leverage your investment in existing 68000-based software are equally important. By driving costs to approximately $1K per MIPS in OEM quantities, while maintaining 68000-compatibility, Edge makes CISC a more attractive option than other implementations of CISC or RISC. 68000-based manufacturers can stay with CISC and forego a sizeable portion of software porting costs, as well as the on-going expense of supporting and maintaining two different architectures.

In the industry's continuing quest for improved machine performance, Edge has set the pace by achieving faster clock speeds and reducing cycles per instruction. At 1.4 cycles per instruction, the EDGE 2000's AIT (Average Instruction Time) is already lower than most products on the market today.



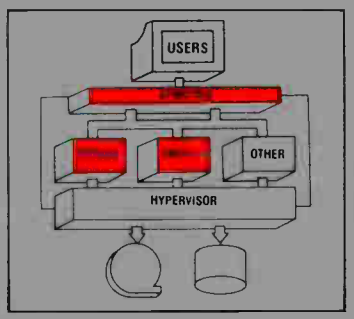
Nonetheless, the CISC/RISC debate will continue. But for 68000-based manufacturers faced with the need to expand their product lines and bring high-performance 68000-compatible products to market economically and on time, the EDGE 2000 is a clear winner.

SYMETRIX UNITES PICK, UNIX V.2 OTHER OPERATING SYSTEMS TO FOLLOW

Edge Computer now offers SYMETRIX™, a concurrent operating system environment, on its line of high performance computer systems.

SYMETRIX provides an architecture that allows multiple standard operating systems to operate at the same time on the same system.

The first implementation of SYMETRIX integrates the solutions and applications oriented environment of the PICK* Open Architecture with the programming and systems environment of UNIX V.2+.



SYMETRIX provides a seamless, menu-driven PICK/UNIX interface that allows transparent access to PICK and UNIX. The end-user literally never need know which operating system is being used.

SYMETRIX is undergoing further enhancements that will allow transparent interfacing of as many as three, four or more popular operating systems.

EDGE COMPUTER

Compatible With Your Future

For more information, contact Pamela Mayer, Edge Computer Corporation, 7273 E. Butherus Drive, Scottsdale, AZ 85260, 602/951-2020. European Operations contact, Heiner Krapp, 5 Avenue des Jordils CH 1000 Lausanne Switzerland, 41-21-275315.

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Circle 78 on reader service card

INSIDE TECHNOLOGY

ASIC VERIFICATION: CHASING A MOVING TARGET

A new generation of verifiers is struggling to keep up with faster and more complex ASICs; picosecond resolution and accurate on-chip test circuits help with the task

by Jonah McLeod

Application-specific integrated circuits are troublesome devices. Troublesome to verify, that is, because onrushing ASIC technology is pushing the speed and complexity of the chips to new records. And ASIC verifiers are struggling to keep up.

The core of the problem is the speed of the newest ASICs: it's fast approaching 100 MHz. Second, the newest chips can contain the equivalent of a printed-circuit board full of microprocessors, peripheral circuits, logic arrays, memory chips, and more. Yet most of the internal nodes of such an IC are just that—not available for outside probing.

In addition, ASICs are being implemented with faster technologies—CMOS, emitter-coupled logic, and gallium arsenide—to achieve the demanding performance of today's applications. These increasingly fast and complex designs are becoming nightmares to verify and test.

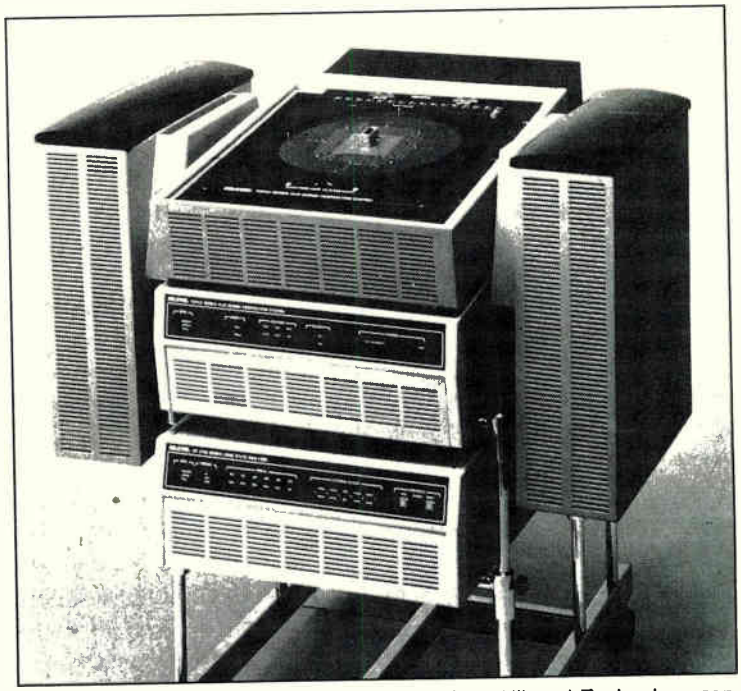
Testing here is truly a hardball situation calling for something more from both the chip and its tester. For their part, the new ASICs are coming to the test head predisposed to testing; they meet the verifier halfway by giving up a portion of their valuable area to built-in self-test circuitry. The tester must go a bit further, and so the makers of ASIC verifiers are introducing a new generation of machines that go a long way toward solving the verification crisis.

An ASIC verifier not only must be prepared for various types of built-in test circuits, it must be fast enough not to shirk at 100-MHz test rates. It must be flexible, too. It must fool an ASIC into thinking there is an individual tester at each of its pins. Its accuracy and resolution must be nonpareil—measured in picoseconds. On top of those assets, it is becoming essential for verifiers to link with the CAE systems that designed the ASICs in the first place.

Just as important, an ASIC verifier must be affordable. Considering that ASICs are characterized by relatively small runs and voluminous functions, verifiers cannot afford to carry million-dollar price tags. A good example of the new breed of affordable ASIC verifiers that can handle fast, complex chips is the Logic Master XL (see p. 82) from Integrated Measurement Systems Inc. of Beaverton, Ore.

ASIC verification systems face the unenviable and probably impossible task of ensuring the proper operation of every node inside the chip using only the input/output pins to stimulate and acquire responses. "The ASIC verifier needs a way to isolate these large macrocells as it stimulates the input lines of the cells and checks responses on its output lines," says Garth Eimers, vice president of marketing at Cadic Inc., a Beaverton, Ore., maker of verifiers.

That's why the struggle to test complex ASICs begins with the chip designer. Many designers now think the way to handle testing of the large amount of logic in an ASIC is to incorporate test



1. SCAN DESIGN. The Topaz II ASIC verifier from HiLevel Technology can handle scan circuits that are built into an IC to improve testability.

HOW IMS IS STAYING CLOSE WITH ITS FAST ASIC VERIFIER

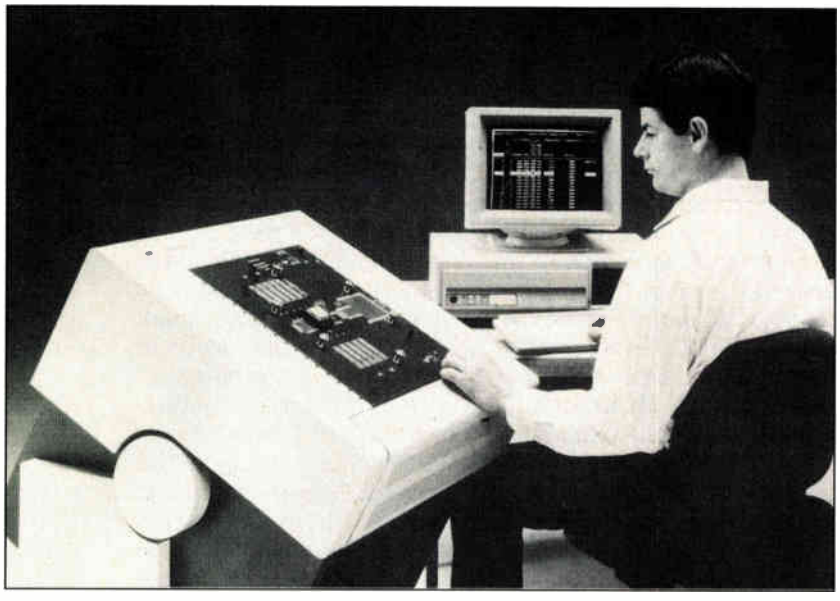
Its third-generation verifier can hit a crackling 100 MHz and boasts a distributed architecture that lets it vary the timing or voltage on each pin

by Jonah McLeod

The company that pioneered the verification of application-specific integrated circuits is stepping up the pace. Integrated Measurement Systems Inc. of Beaverton, Ore., is introducing a third-generation ASIC verifier that hits a crackling 100-MHz top speed so that it can keep pace with fast-changing ASICs.

IMS's Logic Master XL is designed to meet the verification problems imposed by ASIC's spiraling speed and burgeoning complexity. ASIC performance—as measured by clock speed—has risen beyond 50 MHz, thanks to finer geometry and faster processes. And the chips are getting more complex, too. Besides merely collecting the glue logic on a printed-circuit board, an ASIC can encompass on-board microprocessors, programmable logic arrays, and other complex IC functions. It can mix technologies, too. Some come with ECL cores and TTL input/output configurations. As if those assets did not make testing tough enough, ASICs can bristle with more than 256 pins.

Enter IMS's Logic Master XL, successor to the Logic Master 2000 [*Electronics*, June 23, 1986, p. 39]. To zip through higher speed devices, the IMS system's 100-MHz clock and data rates are twice that of other verifiers now on the market. Its frequency can be set, or resolved, to a fine 125 ps. It can place a pulse edge with a hairbreadth accuracy of 100 ps. To effortlessly wring out a variety of complex ASIC devices, especially those with embedded microprocessors or mixed-process technologies, the new IMS system sports a distributed architecture that allows it to vary the timing or voltage on each pin.



1. SUPERFAST VERIFIER. The Logic Master XL wrings out ASICs at 100-MHz clock and data rates and provides 100-ps timing resolution at each pin with ±1-ns skew.

True, much of this firepower is not new—million-dollar ATE systems have both blazing speed and per-pin architecture, and some inexpensive verifiers have similiar architectures. But Logic Master XL, which will carry a price tag of between $250,000 and $425,000 when it begins shipping in December, will be the first moderately-priced verifier to combine 100 MHz speed and a distributed architecture.

The Logic Master XL has already mightily impressed one CAE house: Mentor Graphics Corp. is buying IMS lock, stock, and barrel because it sees the Logic Master technology as the solution to the testing bottleneck (see p. 85).

The Logic Master XL (see fig. 1) can be configured with 16 to 224 bidirectional channels or with 32 to 448 separate chan-

WHAT MENTOR HOPES TO GET FROM IMS

Mentor Graphics Corp. wants to sell more CAE systems. It can't do that, the Beaverton, Ore., company believes, until it solves one of the biggest bottlenecks in producing ASICs designed with CAE systems—verification and testing of the prototypes. Its solution is to acquire Integrated Measurement Systems Inc., also of Beaverton, the company that pioneered the concept of ASIC verification.

On Oct. 22, Mentor did just that—for a cool $30 million in Mentor stock. "Mentor Graphics is buying into the idea of new-generation computer-aided testing," says Gerald Langeler, Mentor's president and chief operating officer. Such tools as IMS's Logic Master XL (see p. 82) are the wave of the future, he believes.

"As CAE and CAD tools become necessities, the bottleneck in the design process has moved to the test function," he says. "Many of our customers are coming back and saying they now have a test problem, one that cannot be solved by stand-alone ASIC verifiers."

The bottleneck to which Langeler refers is one of generating test programs for increasingly complex ASIC devices. For instance, it is not unusual to find a microprocessor on board a large ASIC, and it can take months to develop a test program. Solving this problem, he thinks, requires a much closer coupling between the design and test systems.

Closer coupling of the systems is the first goal of a combined Mentor-IMS operation. "Mentor Graphics and IMS [will] develop synergy in that the designer will be able to move his design data base over to his verification test system much more easily," says Langeler. Now, coupling between design and test is rather loose. A designer sends his data base, with its test pattern, to the test system where it is converted to stimulus patterns. The patterns must be modified and interpreted before they are shoehorned into a test system. With close coupling, test vectors developed on the design system are tailored for the physical criteria of the test system.

IMS president Steven R. Palmquist says that the merger evolved from discussions aimed at working out a joint marketing agreement. "It became obvious that it was in both of our best interests to merge," he says. The companies' founders all once worked at Tektronix Inc. and say they share a philosophy and view of market direction, as well as a customer base.

LANGELER: Buying IMS was integral to the Mentor president's long-term strategy.

The merger doesn't mean that IMS will become a captive supplier. "It will in no way affect our ability to support other CAE vendors' equipment," Palmquist says.

The IMS purchase fits right in with Mentor's long-range growth plan. "We will continue to extend our product line into the newly emerging areas of computer-aided design, test, and manufacturing," Langeler says. "We started that progression in 1984 by forming an automated layout division, then got into documentation through our acquisition of Context Corp. in 1986. Now we have moved into the computer-aided-test area and plan to get into computer-aided electronic packaging and software engineering."

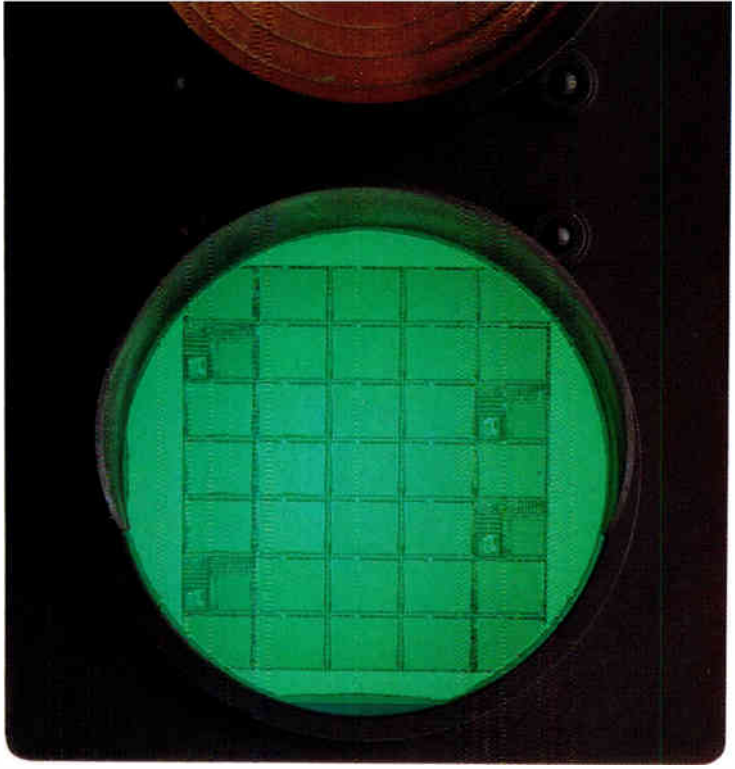
Langeler believes the entire fabric of the testing industry is changing, and he wants Mentor to be in on it. "Computer-aided testing is as ripe for technological change as CAD/CAM was in 1980," he says. "And IMS is the catalyst. The kinds of products IMS produces are precursors of a sweeping new generation, test equipment that recognizes that both ASICs and CAE systems exist."

Langeler contends that CAE/CAD suppliers made a quantum jump in the early 1980s. The automation tools they introduced then were a radical departure from the by-hand process then in practice. Now, a similar leap is about to take place in the ATE business, he believes. Companies such as IMS are developing a new generation of highly automated, high-performance, dedicated testing tools that cost much less than the general-purpose, million-dollar systems being sold by traditional ATE manufacturers. For example, the Logic Master costs between $250,000 and $450,000, but it runs at a breathtaking 100 MHz and boasts a distributed architecture that allows it to vary the timing or voltage on each pin.

Langeler sees a fundamental change coming in the ATE business. He thinks traditional instrument manufacturers don't recognize the business in which they are competing. "It is fundamentally a software business," he says. "The platforms are vehicles for the software."

It's software that is the strength of companies like IMS. Langeler says some instrumentation companies have shown skill in the hardware end of ASIC verification and test, but they lack the expertise in software to compete effectively in this new market. "None of these guys cut their teeth on software as we did," he says.

–Jonah McLeod



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NUMBER 138

DIGITALIZATION EXPANDS IN LATIN AMERICA.

In keeping with the ultimate goal of a global ISDN, telecom authorities in Latin America are stepping up their digital network programs.

Telecomunicações Brasileiras S.A. recently awarded NEC do Brasil S.A. a giant order for state-of-the-art digital equipment. It includes NEAX61 digital switching systems (360,000 lines), 5GHz 140M-bit digital microwave communication equipment (1,800 sets), fiber optic communication equipment (200 sets) and PCM transmission equipment (1,300 sets). Most of the systems are to be produced locally with delivery starting this year.

Meanwhile, Empresa Nacional de Telecomunicaciones, Argentina has awarded PECOM-NEC S.A. a contract for NEAX61 digital switches (300,000 lines) and PCM transmission equipment to be installed in the metropolitan and northern areas of Argentina. Local production is scheduled to begin soon. In 1982 NEC constructed a 320-km fiber optic digital telephone system, interconnecting 6 tandem exchanges and 60 telephone offices in the metropolitan area.

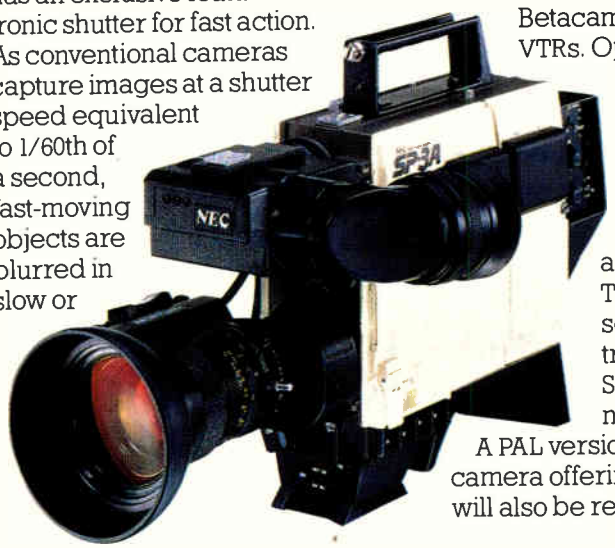
NEC is also contributing to the 5-year telecom digitalization project by Compañía Anónima Nacional Teléfonos de Venezuela by supplying NEAX61 digital switches to 97 exchanges in Maracaibo, Puerto La Cruz, and other important areas. For interconnection of these exchanges NEC will supply a 200-km fiber optic communication system.

As one of the world's leading suppliers of digital exchanges, microwave and fiber optic systems, NEC is helping to further the digital revolution throughout the world.

NEW CCD CAMERA STOPS ACTION ELECTRONICALLY.

The trend in color cameras for broadcast use is irrevocably "solid-state". CCD cameras are more compact, dependable and durable than tube types and have no comet tails and burn-in when shooting extremely bright objects.

On top of these inherent benefits, NEC's new SP-3A CCD Color Camera has an exclusive feature—the electronic shutter for fast action. As conventional cameras capture images at a shutter speed equivalent to 1/60th of a second, fast-moving objects are blurred in slow or still playback on VTR. To remedy this problem, our SP-3A stops the action electronically at 1/60th to 1/2000th of a second, offering precise, clear-cut images.



The SP-3A uses 3 new CCD chips that are anti-smear and -blooming—two for the green channel and one for the combined red/blue channel. This dual green system provides much higher resolution and sensitivity than the conventionally-structured RGB system.

The new CCD camera displays widespread versatility. Besides standalone use it forms an efficient shoot/record system with integral Betacam, MII or 8mm-format VTRs. Options are available for multi-core or triax remote control.

Users' acceptance of this versatile new camera has been remarkable. NBC, a major U.S. TV network, recently sealed a five-year contract to purchase the SP-3A for electronic news gathering.

A PAL version of NEC's CCD color camera offering broadcast quality will also be released.

WORLD'S FASTEST ECL GATE ARRAYS.

The performance of high-speed silicon logic LSIs is rapidly accelerating. NEC's new ECL-4 gate arrays are the swiftest in the world with a 100ps basic gate delay or 220ps fully loaded.

Combining unprecedented speed and flexibility, the ECL-4 family includes the μPB6312 with 1,200 gates (400 Full-adders) and the μPB6303 with 600 gates (200 Full-adders). Both offer 100K or 10KH interface options and ample I/O up to 108 pins.

NEC's ECL-4 gate arrays are available in a choice of 72- or 132-pin PGA packages, and operate in ordinary forced-air-cooling environments since sophisticated heat sinks are standard.

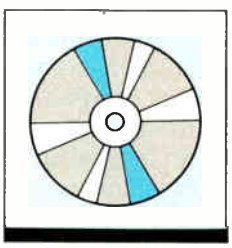
NEC offers 61 internal macros and 33 I/O blocks plus complete CAD tools. The ECL-4 family should hasten the development of speed-oriented computers, graphic terminals, LSI testers and telecom equipment.

NEC

IT'S SHOWDOWN TIME IN INTERACTIVE VIDEO

GE and Philips/Sony square off in interactive video systems based on compact-disk technology: both camps say they'll have products no later than mid-1988

by Tom Manuel



Interactive video systems based on compact-disk technology are on their way: Both General Electric Co. and the team of Philips/Sony Corp. are preparing to launch products in 1988. The big question now is whether one of the two systems will come to dominate the marketplace.

On the heels of the first live demonstration of the Compact-Disk Interactive system in Amsterdam, Philips is now promising its first products by mid-1988, with full production by year-end. CD-I players and disks are anticipated as well as authoring tools and related services. GE's first Digital Interactive Video products (see p. 97) should arrive at approximately the same time, say the technology's developers at the David Sarnoff Research Center in Princeton, N. J.

Both sides have kept at bay potential application developers, who are eager to see what the two competitors had to offer. Both technologies bring different characteristics to the marketing fray, however, and the two camps are publically claiming that the systems may, in fact, be non-competitive.

From Philips, the CD-I developer, come words like these: "General Electric's DVI is meant for the professional market and CD-I is targeted at the consumer/institutional sector. So DVI will have no direct impact on CD-I," says Joop Witvoet, director of communications, New Media Systems Division in Eindhoven, The Netherlands. "Both systems will coexist with different market emphasis," adds Witvoet, conceding only that "in the long run, the different systems may influence each other." The words are the same for Sony in Japan. Haruo Hiki, general manager of CD Systems Division and Super Micro Systems Group and Susumu Shinbori, CD Systems Division manager, also say different markets are being targeted. "There is interest" about DVI in Japan, says Hiki. "However, the one-hour movie capability is probably not sufficient for the consumer market."

From the DVI side, Arthur Kaiman, Sarnoff Research Center director of digital products research, says GE anticipates that DVI's compression/decompression techniques will not be cost-competitive for consumer products until the early 1990s. He concedes as well that not every application will require full-screen motion video.

Despite claims of a non-adversarial relationship, however, the two camps can't resist taking potshots at each others' systems. CD-I supporters criticize DVI's video picture quality while GE's proponents point to CD-I inability to do full-screen, full-motion video. Even with that shortcoming, CD-I is expected have significant entertainment and training applications.

The public announcement of CD-I was made at the first CD-ROM conference in Seattle in March 1986. At that time the first CD-I prototypes were projected for mid-1987 and the backers estimated that the first products would be on the market by early 1988. The CD-I proposed format was circulated in May 1986 for comment among Sony and Philips' world wide licensees of CD tech-

1. ACTIVE VIDEO. With the digital video interactive system developed at the David Sarnoff Research Center, users have full-motion video, graphics, and stereo sound at their command.

nology. The number and nature of comments and suggestions prompted the CD-I developers to go back to the drawing boards.

While interactive video per se is not a new technology, the current excitement is over the prospect of being able to offer it on low-cost CD media and drives and thus greatly increase the size of the market. However, a sizable and growing market for interactive video already exists using 12-in. diameter video disks (see p. 94). U. S. market projections for these so-called IVD systems, out of SK&A Research Inc., predict that the number of systems (they range widely in complexity from simple disk players to full personal computer-based systems) sold in the U.S. will be 75,000 in 1988, climbing to 252,000 in 1992. The Irvine, Calif. market research company further estimates that hardware expenditures will grow to $1.2 billion in 1990 from $700 million in 1988. Further, the nonhardware expenditures—costs for video production, system support, software, and courseware—will grow to $1.25 billion from $660 million.

"It is not clear whether the new [CD-based] technologies will cut into these [the 12-in. system] sales or help expand them," says Stewart Krasney, SK&A Research president. He says the arrival of DVI and CD-I on the scene "adds credibility to the 12-in. market," because they represent new technology for the same kinds of systems. In addition, Krasney projects that current applications developed for 12-in. analog systems will eventually be transferable to the CD-based systems.

In a sense, both CD-I and DVI will help the credibility of CD-ROM technology because they use it as the delivery medium. "They will be a big catalyst for CD-ROMs," says Frederick P. Meyer, president of Meridian Data Corp. His Capitola, Calif. company is introducing a catalyst of its own into the CD-ROM marketplace. The microcomputer-based product will also give an economic boost to the new interactive video technologies by dint of a system designed to reduce the cost and speed of the disk mastering process (see p. 101).

A recent intriguing element to the interactive video disk marketing situation was the cancellation of a major announcement in November by GE. It had called a press conference the first week of November, apparently to announce a new joint business venture with an unidentified partner for commercializing DVI technology. A few days later, GE cancelled the conference because negotiations had reached an impasse, according to an insider. One report is that GE's intended business partner for marketing DVI was Lotus Development Corp. of Cambridge, Mass. An official at Lotus denied any involvement, however.

The CD-I specification under development by Sony and Philips creates, in effect, a stand-alone player product. The CD-I standard has designated a central processing unit, operating system, and the minimum hardware and functions required of disk players. Every disk will play on every machine. The hardware and functions required in every CD-I player include a CD drive; Motorola 68000 family microprocessor; a 1-Mbyte read-only memory; 8 Kbytes of nonvolatile RAM, CD-RTOS operating system, a specialized real-time operating system designed to handle the files on a CD-I disk; normal resolution video images (360 by 240 pixels for NTSC monitors and 384 by 280 for PAL monitors); a pointing device such as a joy stick, mouse, or track ball; and standard character set.

Both GE and Philips/Sony have kept at bay potential application developers, who are anxious to see what the two competitors have to offer for development

CD-I players will be able to play CD-ROM and CD audio disks as well. Basically, CD-I is an extension of the CD and CD-ROM formats to store, deliver and decode types of information in addition to two-channel audio and data, such as graphics, still frame video, and limited motion video.

Philips has been busy designing and fabricating a complex video decoding chip and a 68070 microprocessor, a 16/32-bit 68000-compatible device. So far, tests of these chips have been positive and production at Philips is on schedule. Late this year, the company will announce when and where these components can be obtained by potential CD-I product developers and the current CD-I licensees. Meanwhile, Sony is working on three CD-I chips: an audio chip, a control chip, and a CPU interface, which it says are all on schedule.

Overall, CD-I is said to provide better computer graphics than its 12-in. analog competitors, but its natural picture reproduction is less satisfac-

2. ENABLER. Interactive video derived from CD audio will use CD-ROM disks and drives like these made by Laser Magnetic Storage International.

GE TAKES THE WRAPS OFF ITS INTERACTIVE VIDEO SYSTEM

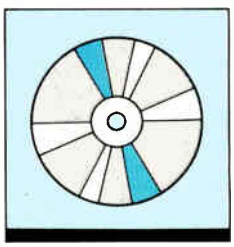
Sarnoff team readies compression techniques and an application development system

by Tom Manuel

General Electric Co. surprised everyone earlier this year when it announced a new way to mix full-screen full-motion video, three-dimensional and animated computer graphics, high-quality multichannel audio, and data on a single all-digital medium. Since then, researchers at GE's David Sarnoff Research Center in Princeton, N. J., where the technology was invented, have improved the quality of the full-motion video pictures and developed a comprehensive package for third-party application development.

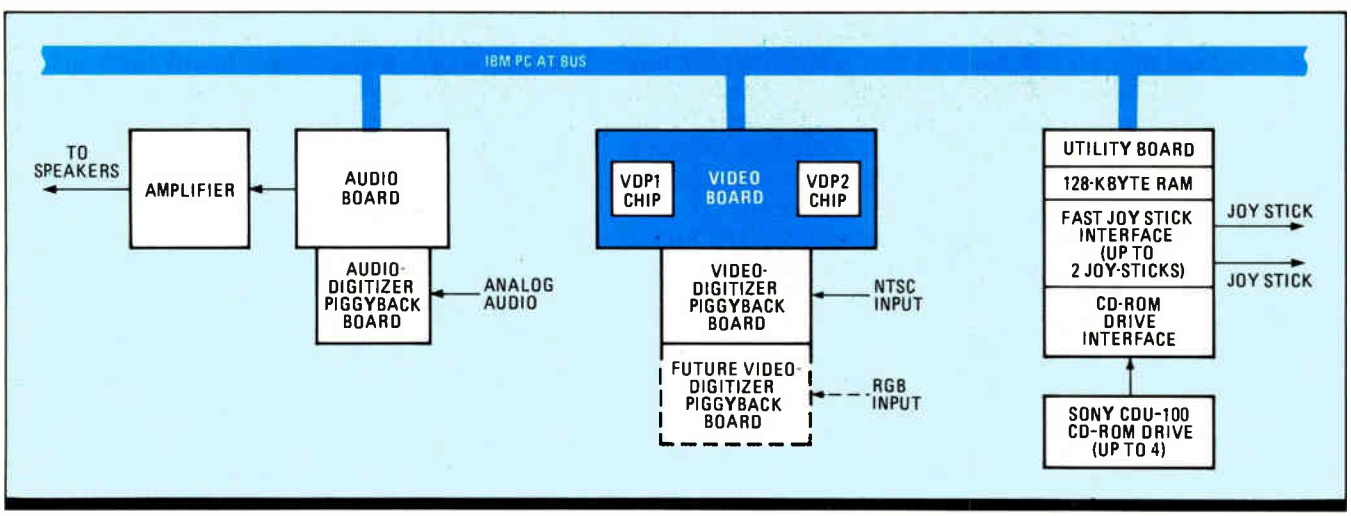
Now the company is providing the first details of its DVI (digital video interactive) system, on the data-compression techniques essential to the system's operation, and on the applications development package. GE and the Sarnoff research center hope to move the system to market through a new company they will launch early next year.

DVI technology [*Electronics*, March 19, 1987, p. 33] combines the interactivity of computer graphics and text retrieval with the realism of television video and digital stereo sound. The DVI development subsystem will include a six-board set, (see fig. 1), three of which plug into expansion slots of an IBM PC AT or compatible. These three consist of a video board, an audio board, and a utility board for the basic system. Three optional piggy-back boards—a video digitizer, an audio digitizer and 1-Mbyte video random-access-memory board—complete the set. A software development package, written with a C programming interface, will use a real-time multi-tasking executive that runs under PC/MS-DOS, an audio video support-system program, and a graphics package. Authoring tools to aid application development include a microcode assembler and simulator.



To enhance DVI's chances of succeeding commercially, however, the new GE venture company also plans to offer a video compression service, which will take uncompressed digital video segments from a product developer, compress it by a factor of 120:1, and deliver the result back to the customer. The compression service will employ a powerful parallel computer built by Meiko Ltd. of Bristol, England. Another aid to application developers will be a real-time compression algorithm to be run on the DVI development system, albeit with much lower picture quality. It will provide authoring quality video for the testing and tuning of applications.

Armed with these development tools, about 10 to 20 beta-site development projects are expected to begin utilizing DVI technology early in 1988. Potential applications include educational areas such as geography, biology, history, archaeology, and astronomy as well as vocational training in auto or aircraft repair, photography, and flight simulation. Other possibilities lie in landscape design, interior decoration, home learning and entertainment, interactive maps for autos



1. FUTURE SYSTEM. GE's first DVI system consists of a six-board set—three PC add-in boards and three optional piggy-back boards.

LOW-COST CD-ROM MASTERING IS HERE

A breakthrough in the speed and cost of producing CD-ROM disks is at hand. A microcomputer-based system from Meridian Data Inc. performs the complex data preparation chores that are now done by superminicomputers at a handful of CD-ROM mastering facilities.

The CD Master System is the second production tool offered by Meridian. The Capitola, Calif., company has added a powerful circuit board with about 22 chips to its CD Publisher system, introduced in 1986. The new board performs the error-detection and correction-coding required of large data volumes prior to pressing (see fig. 1). Called the Layered ECC Augmentor, or LEA board, it processes data-plus-audio, and can potentially handle the emerging mixed-mode formats such as Compact Disk-Interactive and Digital Video Interactive.

In addition to the LEA board, the new system includes the same IBM PC or compatible or Apple Macintosh, disk-drive subsystem, and nine-track tape-drive hardware as CD Publisher, a system designed to prepare and check CD-ROM data prior to delivery to a mastering facility. The disk subsystem gives the Meridian product high-speed data transfer to complement the LEA board's processing power. Together, they boost the Meridian system's mastering capability to four times that of custom mastering systems, company executives say.

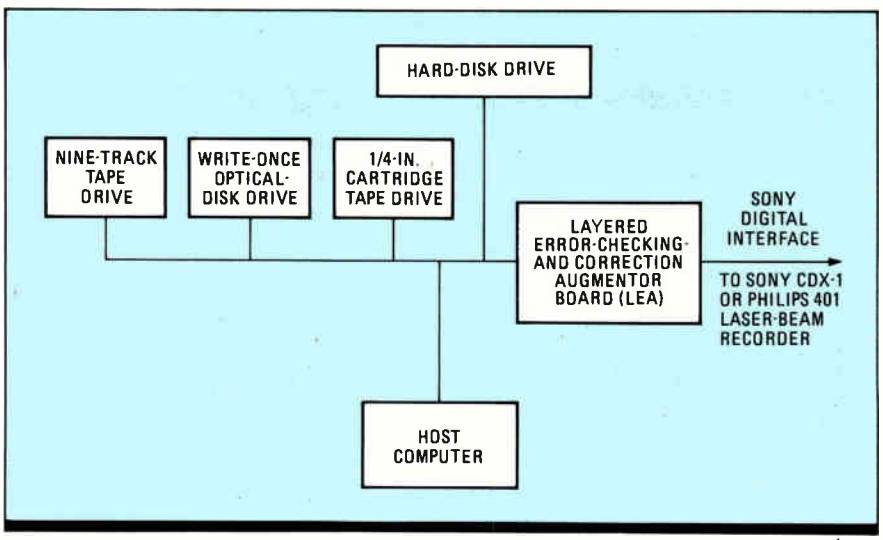
Typically, mastering facilities have bought VAX superminicomputers with nine-track tape drives, developed their own CD-ROM premastering procedures, and thus created custom systems. "A production tool such as the CD Master System will encourage more mastering facilities to offer CD-ROM and eventually CD-I and DVI production services at lower prices," says Frederick P. Meyer, Meridian's president. Companies developing CD-ROM applications will also benefit by having more choices for mastering services.

The LEA board has two sections. The board controller portion consists of an Intel 80188 microprocessor, 512 Kbytes of random-access memory, and 32 Kbits of ROM to hold the start-up code. The other board section is the ED/EEC generation engine. This engine is tied together and connected to the controller by a communication bus and a four-port 512-Kbyte RAM. A Small Computer System Interface peripheral controller is included on the board, connecting the CD Master System to a variety of input devices.

The CD Master system will be ready to ship in January 1988, Meridian officials say, and is priced at $89,750 with 1.2 gigabytes of disk storage, capable of producing up to 20 CD-ROMs a day. Custom VAX-based systems costing $250,000 and more can at best produce four or five masters a day, according to Meridian. Meridian systems with disk capacity ranging from 300 Mbytes to 2.4 gigabytes are also available.

In addition to the existing nine-track tape drive for input, future models of the CD Master system will interface to standard devices of the audio and video business such as 0.75-in. Umatic tape cartridge drives. Interfaces for 5.25-in. write-once, read-many (WORM) and erasable optical drives will also be added, Meridian says. Meridian engineers are developing software tools for both the CD Publisher and CD Master systems to allow developers to handle the CD-I and DVI formats. CD-I includes graphics, still video, and limited motion video along with audio and data; DVI utilizes video compression to add full-screen motion video (see story on p. 97).

CD-ROM is the data version of the popular optical compact-disk audio product. The 600-Mbyte storage capacity of read-only data on one CD-ROM disk has attracted the attention of information providers and publishers for the distribution of text and graphics information. The CD optical disk technology and both the audio and data formats were developed and standardized jointly by NV Philips of Eindhoven in the Netherlands and Japan's Sony Corp. in Tokyo. The new mixed-mode formats—such as CD-I, under development by Philips and Sony, and the DVI system



1. GETTING READY. The LEA board adds the required synchronization, header, error detection, and the error-correction bytes to data on its way to a CD-ROM.

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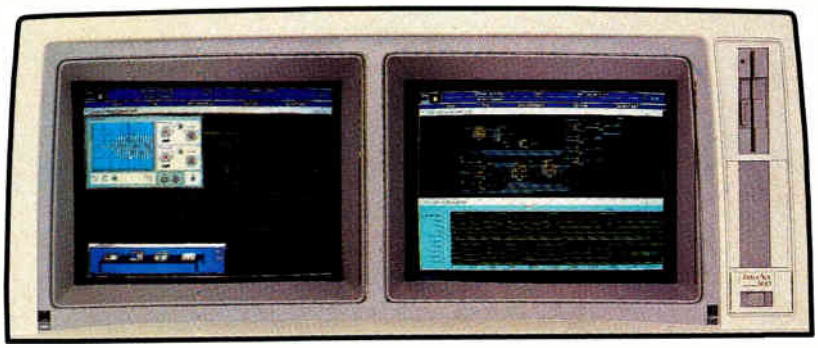
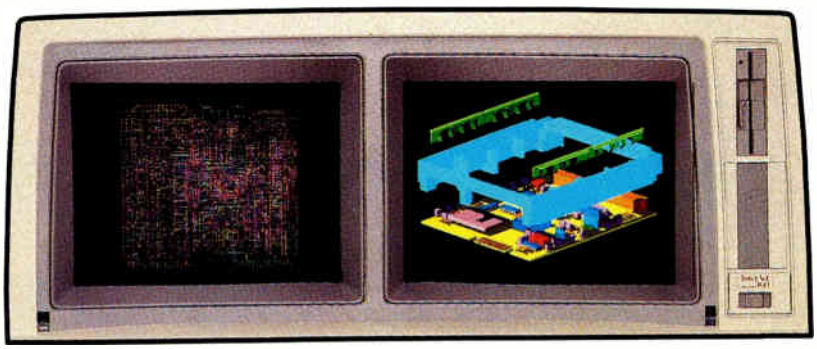
It could take six different systems to do the engineering, layout,



1... Schematic Design with Analog Analysis 2... Schematic Design with Digital Analysis



3... PCB Layout with Manufacturing Interfaces 4... Mechanical Packaging

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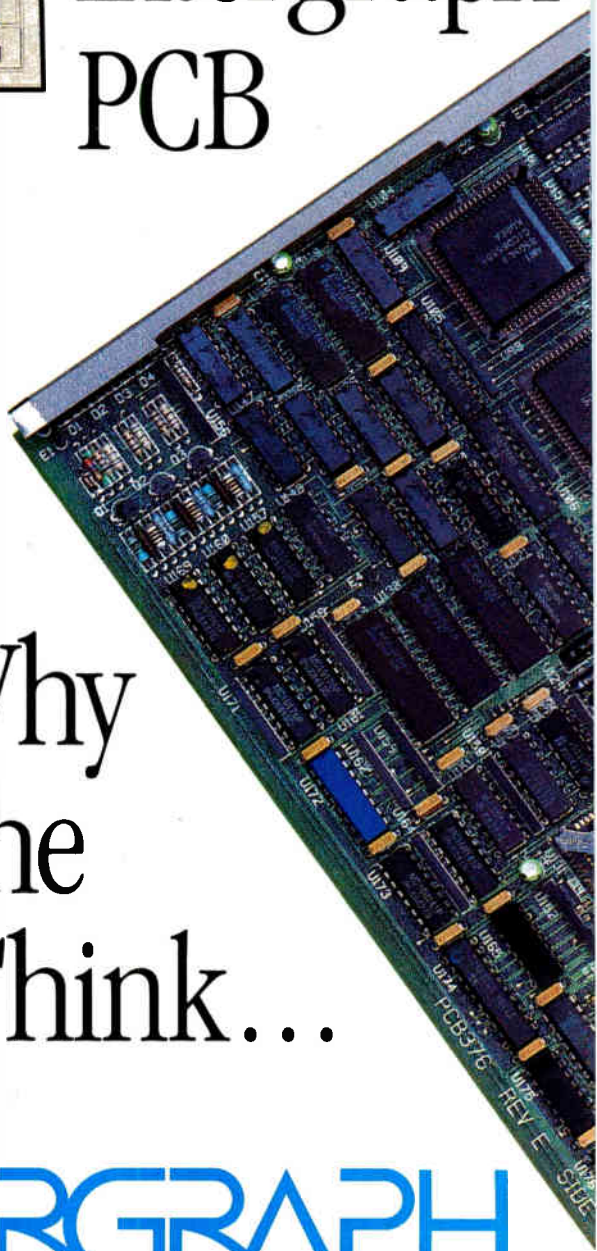

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SELECTIVE GROWTH AND NEW DRAM CELLS SHARE THE IEDM SPOTLIGHT

High-density EPROMs, new flash EEPROMs, and megabit static RAMs will also star

by Bernard C. Cole

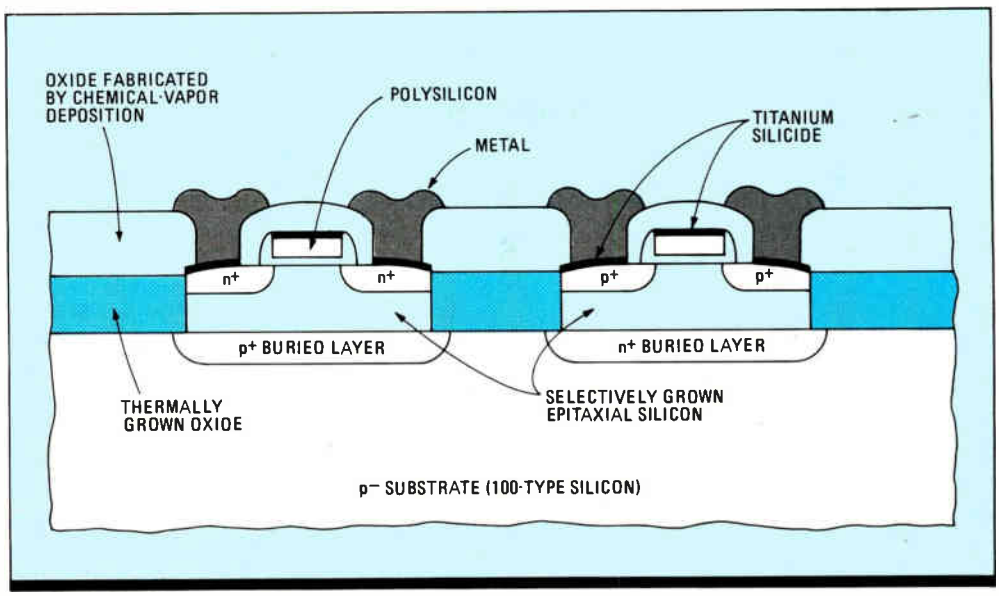
For semiconductor technologists, Christmas usually comes three weeks early when the International Electron Devices Meeting convenes in Washington. Attendees are almost never disappointed, finding novel developments galore in their stockings.

This year's IEDM, set to run Dec. 6 to 9, will be no less of a toy-store delight than past editions. Among this year's highlights will be process technologies, for the selective growth of silicon to solve some submicron-CMOS problems, from Fairchild Semiconductor and Applied Materials and from Fujitsu. This year, memory-chip technology will command a lion's share of attention. Papers will describe a clutch of different cells for building 16-Mbit dynamic random-access memories; these are from NEC, Hitachi, Mitsubishi, and Toshiba. Toshiba will tell how it has built a 4-Mbit erasable programmable read-only memory; there are two entries from Hitachi and Toshiba in the field of flash electrically erasable PROMs; and two efforts aimed at 1-Mbit static RAMs will be discussed by Philips and Sony. Other IEDM topics range widely, covering biMOS variations, gallium arsenide technology, power transistors, detectors and lasers, and vacuum tubes.

In silicon processing, the biggest story at the IEDM will be the emergence of selective epitaxial growth as a method for building submicron CMOS devices without many of the short-channel and hot-electron effects that plague traditional bulk-CMOS devices. Selective epitaxial growth borrows from silicon-on-insulator technology to selectively grow single-crystal silicon in seed windows of a silicon dioxide mask. For example, researchers from Fairchild Semiconductor Corp. (now a part of National Semiconductor Corp.), Palo Alto, Calif., and Applied Materials Inc., Santa Clara, Calif., will describe a submicron dual-buried-layer twin-well CMOS process that depends on selective epitaxial growth (see fig. 1). No less interesting is an offering from Fujitsu Ltd., Kawasaki, Japan, which describes a technique that combines growth of polysilicon and epitaxial silicon to reduce parasitic capacitance and resistance in logic and memory devices.

Members of the semiconductor-memory community generally agree that it will be necessary to use trench isolation and stacked or buried structures to achieve 16-Mbit densities and beyond—but there are a wide range of other problems that must be overcome as well before the megadensity levels can be achieved. Two problems in the spotlight at this year's IEDM are soft-error immunity and self-alignment.

To address soft-error immunity, NEC Corp. of Tokyo has developed a new DRAM cell and fabrication technology for 16-Mbit parts. In what it calls a TOLE cell (transistor on lateral epitaxy), a transistor is fabricated atop a lateral epitaxial-silicon layer which in turn is formed—using an SOI technique—above a capacitor built in a trench (see fig. 2). The charge-storage electrode is isolated from the bulk-silicon substrate by silicon dioxide and the channel region is left connected to the substrate. In addition to providing high alpha-particle immunity, say the researchers, this structure has a low bit-line capacitance and stable dynamic transistor action. It also



1. SELECTIVELY GROWN. Fairchild and Applied Materials have developed a process based on selective epitaxial growth of silicon. The target is hot-electron and short-channel-effect problems in submicron CMOS.

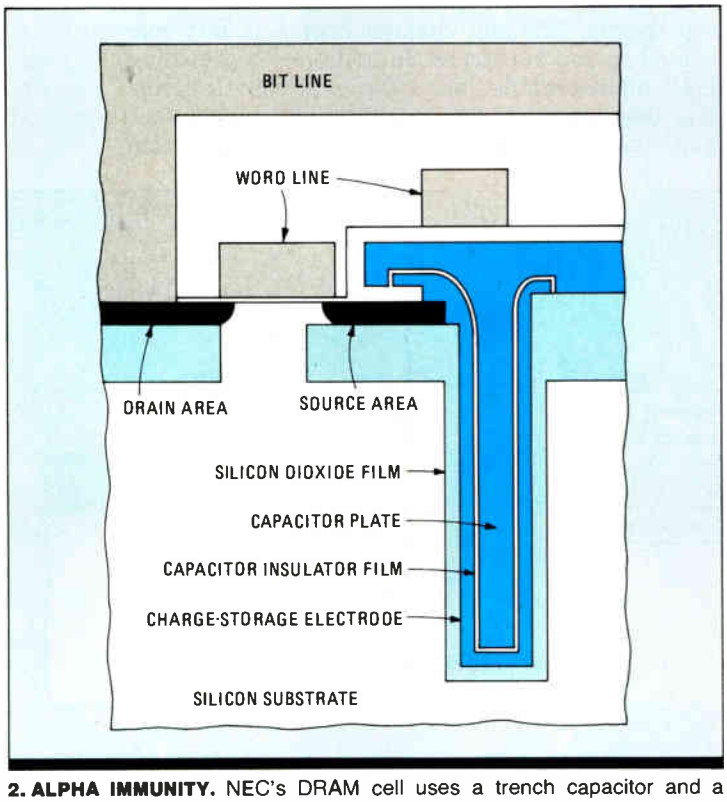
eliminates punchthrough current between adjacent cells.

Self-alignment in dense DRAMs is the target of Hitachi Ltd. of Tokyo. It reports that it has been able to build a 4.2-μm^2 16-Mbit cell using a combination of four self-alignment techniques: a plated-wiring structure using a buried n^+ layer, a sidewall contact, storage-node isolation, and a pad for the bit-line contact.

The 16-Mbit entry from Mitsubishi Electric Corp., Tokyo, also uses self-alignment to produce a very small DRAM cell. Its novel cell structure combines a double stacked capacitor with a transistor whose source and drain are formed of self-aligned polysilicon. Two capacitors are stacked in a trench, and beside each is either a source or a drain region formed by an impurity diffusion into the first level of polysilicon. This builds an access transistor that is inherently self-aligned. With 0.7-μm design rules, this structure results in a cell size of only 5.95 μm^2.

A new structure intended to eliminate leakage currents in buried stacked-capacitor cells is the subject of a fourth 16-Mbit DRAM paper, from Toshiba Corp. of Kawasaki, Japan. The 6.12-μm^2 cell consists of a stacked capacitor in a trench, topped by a sidewall diffusion layer from the first level of polysilicon that halts the junction leakage current that usually results from sidewall damage during etching.

Super-small memory cells are not just found in DRAMs. Toshiba also will open eyes at IEDM with a 4-Mbit EPROM sporting a cell size that at 9 μm^2 is only 30% to 50% larger than a 16-Mbit DRAM cell. In order to scale down the cell, the thickness of the first gate oxide and the interpolysilicon dielectric is reduced to about 20 nm, compared to a typical range of 50 to 200 nm. Downscaling is also performed in the lateral direction. To prevent generation of cracks due to stress at the edges of the floating gate, polysilicon thickness is reduced to about 100 nm.



2. ALPHA IMMUNITY. NEC's DRAM cell uses a trench capacitor and a transistor atop an epitaxial silicon layer to reduce the soft-error rate.

Toshiba is also making a bid to push EEPROMs to the density levels it is achieving in EPROMs. Hitachi will describe a parallel effort. Both companies have developed flash-EEPROM structures that combine the hot-electron-write approach of EPROMs with the cold-electron floating-gate read structure of an EEPROM.

The Hitachi EEPROM cell consists of a single floating-gate transistor with a built-in select transistor created by implanting slightly asymmetric source and drain regions. That contrasts with the approach used by Seeq Technology Inc., San Jose, Calif. [*Electronics*, Aug. 21, 1986, p. 53], the only company successfully marketing a flash EEPROM. Seeq's select transistor is created by slightly offsetting the top layer of the floating gate in relation to the bottom one. The Hitachi cell is programmed by hot electrons at the drain edge and by electrons tunneling from the floating gate to the source. Using 0.8-μm rules, the result is a 9.3-μm^2 cell—only slightly larger than Toshiba's 9-μm^2 4-Mbit EPROM cell.

Even more impressive is the EEPROM cell from Toshiba: the effective size is 6.43 μm^2, or about 30% smaller than that of its 4-Mbit EPROM. Toshiba researchers say this density was achieved without the aggressive scaling necessary for the Hitachi approach—Toshiba uses 1-μm design rules—and without merging the read/write and select transistors. The key is the use of a unique four-NAND-gate structure measuring only 8.3 by 3.1 μm versus 11.6 by 3.1 μm using conventional techniques.

In the world of SRAMs, the push for higher densities is accompanied, as always, with an abiding concern for high speed. Bidding for membership in the high-speed, high-density SRAM club is Philips of Eindoven, The Netherlands, with a 1-Mbit SRAM that accesses in 25 ns—speed equivalent to that of today's 256-Kbit SRAMs. The circuit uses 0.7-μm design rules, a retrograde twin-well technique with 1-μm isolation and extremely small—2.5 μm—n- and p-channel spacings, and titanium salicide to lower resistance on the two levels of metal interconnection.

And there may soon be one more player in the fast megabit SRAM market. Although Sony Corp. of Kanagawa, Japan, has built only low-density test devices, it has developed a six-transistor SRAM cell that measures only 60 μm^2, about the same as competitive devices using four-transistor structures. Sony researchers use a new SOI fabrication technique called position-controlled crystallization, in which transistors are fabricated on individual isolated 1-by-1-μm islands. This makes it possible to place the devices much closer together. □

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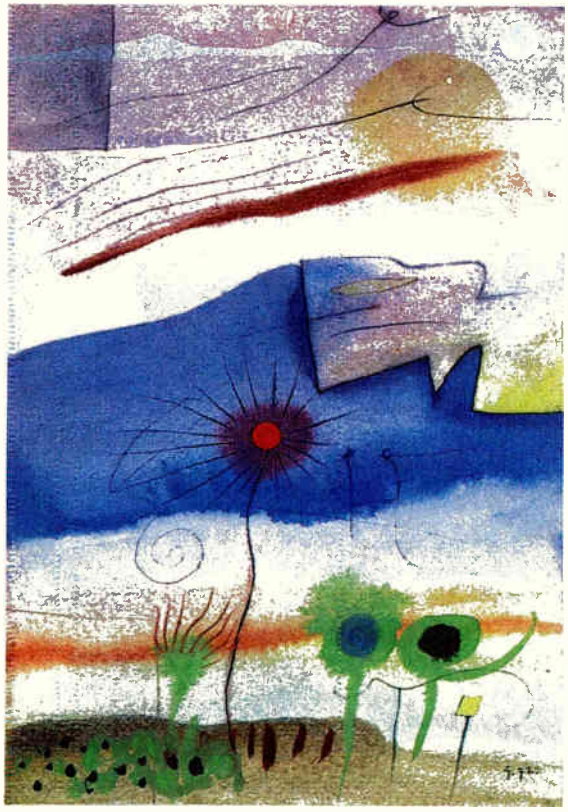

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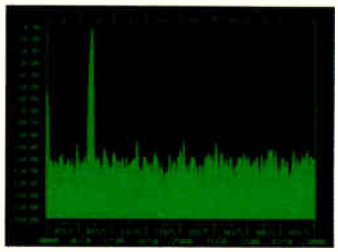

Actual spectral performance of ZAD2846

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LV-E SERIES EXTENDED RANGE — SINGLE OUTPUT 85-265VAC INPUT

MODEL	MAX CURRENT (AMPS AT) 40°C	50°C	60°C	PRICE QTY 1	QTY 100	QTY 250	QTY 1000
5V ±5% ADJ.							
LVS-42E-5	2.0	2.0	1.50	$43.00	$38.50	$35.00	$34.00
LVS-43E-5	3.0	3.0	2.25	51.00	46.00	40.75	38.50
LVS-44E-5	5.0	5.0	3.75	79.00	71.00	63.25	59.75
LVS-45E-5	10.0	10.0	7.50	106.00	95.50	85.00	80.50
12V ±5% ADJ.							
LVS-42E-12	0.9	0.9	0.67	43.00	38.50	35.00	34.00
LVS-43E-12	1.3	1.3	0.97	51.00	46.00	40.75	38.50
LVS-44E-12	2.1	2.1	1.57	79.00	71.00	63.25	59.75
LVS-45E-12	4.2	4.2	3.15	106.00	95.50	85.00	80.50
15V ±5% ADJ.							
LVS-42E-15	0.7	0.7	0.52	43.00	38.50	35.00	34.00
LVS-43E-15	1.0	1.0	0.75	51.00	46.00	40.75	38.50
LVS-44E-15	1.7	1.7	1.27	79.00	71.00	63.25	59.75
LVS-45E-15	3.4	3.4	2.55	106.00	95.50	85.00	80.50
24V ±5% ADJ.							
LVS-42E-24	0.5	0.5	0.37	43.00	38.50	35.00	34.00
LVS-43E-24	0.7	0.7	0.52	51.00	46.00	40.75	38.50
LVS-44E-24	1.1	1.1	0.83	79.00	71.00	63.25	59.75
LVS-45E-24	2.1	2.1	1.57	106.00	95.50	85.00	80.50
28V ±5% ADJ.							
LVS-42E-28	0.4	0.4	0.30	43.00	38.50	35.00	34.00
LVS-43E-28	0.6	0.6	0.45	51.00	46.00	40.75	38.50
LVS-44E-28	0.9	0.9	0.67	79.00	71.00	63.25	59.75
LVS-45E-28	1.8	1.8	1.35	106.00	95.50	85.00	80.50
48V ±5% ADJ.							
LVS-42E-48	0.2	0.2	0.15	43.00	38.50	35.00	34.00
LVS-43E-48	0.3	0.3	0.22	51.00	46.00	40.75	38.50
LVS-44E-48	0.5	0.5	0.37	79.00	71.00	63.25	59.75
LVS-45E-48	1.0	1.0	0.75	106.00	95.50	85.00	80.50

LV-E SERIES EXTENDED RANGE — TRIPLE OUTPUT 85-265VAC INPUT

MODEL	VOLT V_o	MAX CURRENT (AMPS AT) 40°C	50°C	60°C	PRICE QTY 1	QTY 100	QTY 250	QTY 1000
5V ±12% FIXED								
LVT-38E-133	+5	1.00	1.00	0.70	$55.00	$49.00	$40.00	$38.50
	+12	0.10	0.10	0.07				
	−12	0.10	0.10	0.07				
LVT-39E-133	+5	2.00	2.00	1.40	78.00	62.75	51.75	45.75
	+12	0.30	0.30	0.21				
	−12	0.20	0.20	0.14				
LVT-40E-133	+5	2.00	1.80	1.20	71.00	57.00	52.50	48.25
	+12	0.30	0.27	0.18				
	−12	0.20	0.18	0.12				
LVT-41E-133	+5	3.00	2.00	1.30	105.00	84.00	67.75	61.75
	+12	1.20	0.80	0.50				
	−12	0.30	0.20	0.13				
LVT-42E-133	+5	3.00	3.00	2.10	116.00	90.00	70.00	61.75
	+12	0.40	0.40	0.28				
	−12	0.40	0.40	0.28				
5V ±15% FIXED								
LVT-38E-144	+5	1.00	1.00	0.70	$55.00	$49.00	$40.00	$38.50
	+15	0.10	0.10	0.07				
	−15	0.10	0.10	0.07				
LVT-39E-144	+5	2.00	2.00	1.40	78.00	62.75	51.25	45.75
	+15	0.30	0.30	0.21				
	−15	0.20	0.20	0.14				
LVT-40E-144	+5	2.00	1.80	1.20	71.00	57.00	52.50	48.25
	+15	0.30	0.27	0.18				
	−15	0.20	0.18	0.12				
LVT-41E-144	+5	3.00	2.00	1.30	105.00	84.00	67.75	61.75
	+15	1.20	0.80	0.50				
	−15	0.30	0.20	0.13				
LVT-42E-144	+5	3.00	3.00	2.10	116.00	90.00	70.00	61.75
	+15	0.40	0.40	0.28				
	−15	0.40	0.40	0.28				

LV-E SERIES SPECIFICATIONS

DC OUTPUT
Voltage range shown in tables.

REGULATED VOLTAGE

regulation, line . . . . . 0.4% for input variations from 105-265VAC or 265-105VAC. 1.0% for input variations from 85-265VAC or 265-85VAC on LVT-38E, 39E, 42E. (LVS-45E: 0.4% for input variations from 95-132VAC or 132-95VAC when wired for 110V operation; 187-265VAC or 265-187VAC when wired for 220V operation.

regulation, load . . . . 0.8% for load variations from no load to full load and full load to no load. (2% for LVT-38E, 39E, 42E.)

ripple and noise . . . . . 15mV RMS for all models with either positive or negative terminal grounded. 150mV pk-pk for 5V models; 300mV pk-pk for 12V through 48V models and second and third outputs of LVT-E models.

temp. coeff. . . . . 0.02%°C for single output models and 5V output of LVT-40E, 41E. 0.03%°C for other two outputs and for main output of LVT-38E, 39E, 42E. 0.05%°C on other two ouputs of LVT-38E, 39E, 42E.

AC Input . . . . . 105-265VAC, 47-440Hz. The LVS-45E is jumper selectable for 95-132VAC or 187-265VAC operation (factory prewired for 220V operation). 85-265VAC, 47-440Hz on LVT-38E, 39E, 42E models.

Efficiency . . . . . 62% minimum. 64% typical on LVT-38E, 39E, 42E models.

DC Input . . . . . 145-370VDC. The LVS-45E allows DC input (260-370VDC) only, when used for 220VAC operation. 110-330VDC for LVT-38E, 39E, 42E models.

OVERSHOOT
No overshoot at turn-on, turn-off or power failure.

AMBIENT OPERATING TEMPERATURE
0-60°C with suitable derating above 50°C (see table).
LVT-40E, 41E derate above 40°C.

STORAGE TEMPERATURE
−30°C to +85°C.

OVERLOAD PROTECTION
Automatic electronic current limiting circuit with automatic recovery, limits short circuit output current to a safe, preset value, thereby protecting the load as well as the power supply when direct shorts occur. Sustained short circuit operation for more than 30 seconds may cause damage to the power supply.

HOLD UP TIME
Output will remain within regulation limits for 16 msec typical (20 msec typical at 100VAC for LVT-38E, 39E, 42E) after loss of AC power at full load with nominal output voltage, and 110VAC input at 60Hz.
On LVS-45E, this is true at 105VRMS when wired for 110V operation or 210VRMS when wired for 220V operation.

OVERVOLTAGE PROTECTION
Standard on LVS-44E, 45E and on main output of LVT-38E, 39E, 42E.

COOLING
Convection cooled, no fans or blowers needed.

PHYSICAL DATA

Package Model	Weight Lbs. Net	Lbs. Ship	Size Inches
LVS-42E	0.44	0.52	1.38 x 3.82 x 3.13
LVS-43E	0.55	0.64	1.38 x 3.82 x 3.88
LVS-44E	0.70	0.82	1.38 x 3.82 x 4.59
LVS-45E	0.86	1.00	1.46 x 3.82 x 6.26
LVT-38E	0.35	0.42	1.38 x 1.97 x 4.33
LVT-39E	0.44	0.52	1.57 x 2.36 x 4.33
LVT-40E	0.84	1.00	1.38 x 3.82 x 4.47
LVT-41E	1.00	1.13	1.46 x 3.82 x 6.05
LVT-42E	0.66	0.75	1.57 x 2.36 x 5.91

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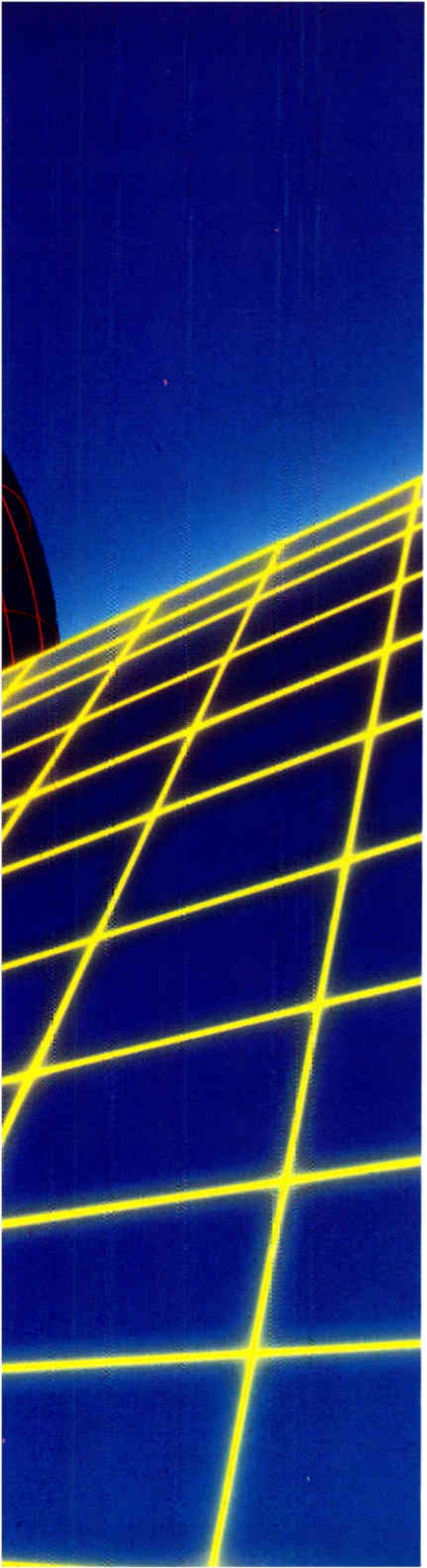

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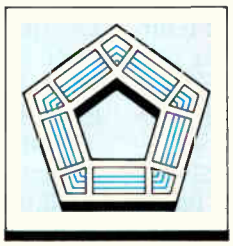
MIMIC'S NEXT CHALLENGE: SLASHING PRODUCTION COSTS

Phase 1 of the Pentagon program to turn out GaAs arsenide analog ICs aims at bringing down their cost; if it succeeds, the payoff will be a $1.8 billion market in 10 years

by Tobias Naegele

The next phase of the Pentagon's ambitious analog integrated circuit program is about to start. Phase 1 of Mimic, the Microwave/Millimeter-Wave Monolithic IC program, poses a critical challenge: can these high-frequency gallium arsenide chips be made for a reasonable cost? It's also critical for the more than two dozen companies who this week are delivering Phase 1 proposals to the Department of Defense. The stakes are high, with a predicted $1.8 billion annual market by 1997.

For the Pentagon, Mimic's payoff will be the microwave and millimeter-wave chips that are considered essential for the coming generation of radar systems, smart munitions, and radio-frequency communications. The DOD is looking for greater sensitivity, increased reliability, and improved functionality over what's possible with existing technology. "The problem is bridging the gap between research and development and manufacturing," says E. D. (Sonny) Maynard, director of computer and electronic technology at the DOD.



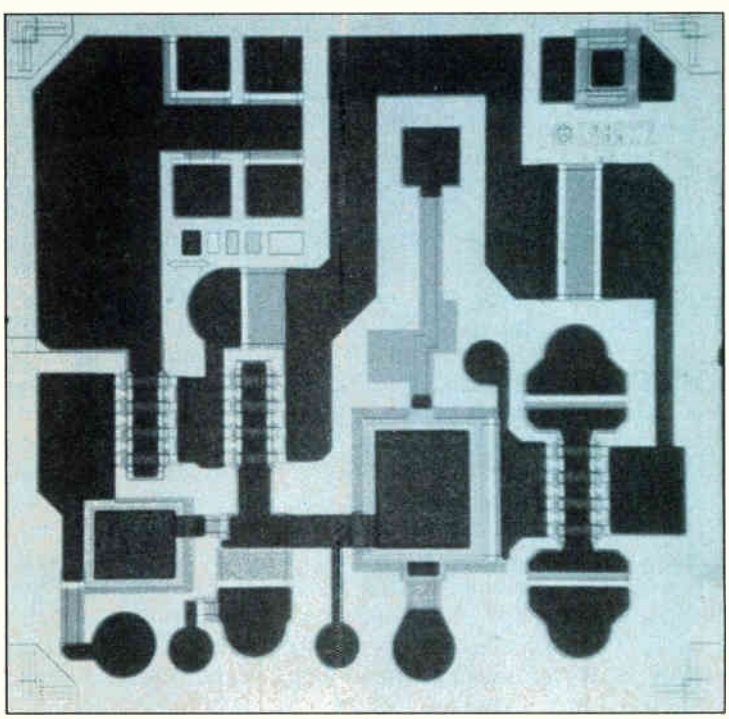
The challenge is not so much in design and complexity, but rather in learning how to build the devices at a practical cost, Maynard says. "The technology has had a difficult time getting over the threshold to where you could buy devices routinely and put them into systems with confidence," he adds.

Until now, hybrid technology has been able to handle microwave frequencies, up to 20 GHz, says Eliot Cohen, director of the Mimic program. But making hybrid modules is expensive and labor-intensive. "Monolithic chips will increase reliability, push cost down, and drive uniformity up," he says.

Mimic will have an even greater effect on higher-frequency devices. "When you go to higher frequencies—millimeter-wave frequencies—you reach a point where hybrids can't operate with much success," Cohen says. Mimic's goal is to replace these hybrids with single-chip solutions that will yield a strong performance edge.

As it stands, manufacturing remains so difficult and costly that most military programs cannot afford to use MMICs, microwave and millimeter-wave ICs. Maynard says the cost of a single MMIC can run into several thousands of dollars. "A fairly complex kind of IC—like a transceiver module for a phased-array radar—now costs from around $3,000 to $10,000" depending on complexity, Maynard says. He estimates that current MMIC costs are typically $100 to $250 for a chip, $250 or more for the package, and up to $2,500 or more for testing. His goal for the program is to drive costs down to about $2.50, $25, and $250, respectively (see "Quantity makes Mimic prices important," p. 122).

Most current MMICs are used in hybrids, but the process involved in building these hybrids is tedious and expensive, says Barry Dunbridge,



LOUDER. TI's microwave monolithic amplifier chip operates at up to 3.5 GHz; Mimic aims to produce chips running at 100 GHz.

ment contract to specific DOD programs. Maynard hopes that will accelerate the development process by avoiding an expensive "insertion phase" of the program.

Requiring that development work be directly related to military systems has had another effect: team bidding on a grand scale. Top defense systems contractors have joined hands with companies with expertise in semiconductors and computer-aided design, as well as with smaller systems houses that are aiming to put MMIC chips into future systems (see table, below). The strategy is to give the bid wide application and appeal, and to design a virtually generic chip set that can be used in a number of applications.

For example, Raytheon Co. and Texas Instruments Inc. brought in Aerojet, General Dynamics, Magnavox, and Norden Systems on the systems contractor side; Compact Software and Consilium for computer-aided-design and -manufacturing help; and Airtron and Teledyne for guidance on technology. This team, which won a $1 million contract in Phase 0, may have the broadest outlook of the Phase 1 competition, says John Harkins, a marketing manager in TI's Defense Systems & Electronics Group in Dallas.

"The Raytheon-TI joint venture was structured to address all of the [Mimic] applications," including electronic warfare, communications, and smart weapons, he says. "We took this course with the intent of looking at all of the applications to determine which chip set would be generic."

And while Maynard admits that the dwindling number of Mimic contracts—16 in the $12.5 million study phase, less than half as many in Phase 1, and probably only two or three in the program's final Phase 2—will effectively trim the number of players, he insists that it won't put the technology solely into the hands of a select few.

To guard against that possibility, Maynard and Cohen inserted a stipulation in the Phase 1 request for proposals which requires that 30% of the wafers and working chips delivered by each team come from a second source not otherwise connected to that team. The second sources will have to get full access to both the design capability and manufacturing know-how developed by the prime contractors, Maynard says.

Giving the second source design capability is a novel idea, he admits, but it should increase the number of vendors a system maker can turn to for custom and standard parts. Several companies, including Harris Microwave Semiconductor, the Milpitas, Calif., division of Harris Corp.'s Chip Sector, are offering their services as foundries—in addition, in many cases, to competing as a partner in a team. For example, Harris is part of a Phase 1 team led by GMHE/Hughes Aerospace Corp.

That's the kind of cooperation and networking the DOD was looking for. Too narrow a field of players could restrict competition and pose a security risk by limiting the sources of parts, while too broad a field might have diluted the technical knowledge base. "There are 25 or 50 companies that can do this job in the U. S.," Maynard says. "What we need is to have a few that can do it in an optimal fashion. Our hope and plan is that those companies that don't get selected here will find a way to get into the teams that do."

Maynard and his DOD colleagues won't know for almost a decade whether Mimic will pay off. It will take that long for the program to run its course—and for the systems that draw on the technology to be fully tested and fielded. But the signs seem good: Phase 0 proved there is a clearly identified, high-volume military market itching to get its hands on Mimic technology. And that, Maynard says, points to a market that's just waiting to explode. □

Additional reporting by Wesley R. Iversen, J. Robert Lineback, and Larry Waller

MIMIC PRIME CONTRACTORS LINE UP THEIR TEAMS

Prime contractor	Team members	Prime contractor	Team members
Allied-Bendix	Pacific Monolithics TriQuint	Loral	Anadigics Comsat Laboratories Dexcel
Ball Aerospace	Cascade M/A-Com	Martin-Marietta	Alpha
Eaton	M/A-Com	Raytheon/ Texas Instruments	Aerojet Airtron Compact Consilium General Dynamics Magnavox Norden Teledyne
E-Systems	Interstate Electronics		
Ford	M/A-Com Pacific Monolithics Singer TriQuint	Sanders	Adams-Russell Lockheed M/A-Com Motorola Varian
Harris	Cornell University EEsof General Electric TriQuint	TRW	General Dynamics Honeywell
Hittite	Adams-Russell Eastman Kodak Harris Microwave	Unisys	Alpha M/A-Com TriQuint Varian
Hughes	AT&T Harris General Electric M/A-Com	Westinghouse	Avantek Cominco EEsof Rockwell TriQuint
ITT	Pacific Monolithics Watkins-Johnson		

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Organization	Part Number	Access Time (Typ.)
Synchronous		
1K x 1	HS-6508RH	160 ns
256 x 4	HS-6551RH	160 ns
4K x 1	HS-6504RH	150 ns
1K x 4	HS-6514RH	150 ns
64K Module 8K x 8 16K x 4	HS-6564RH	250 ns
Asynchronous		
16K x 1	**HS-65262RH**	**100 ns**
2K x 8*	HS-65162RH	100 ns

*Samples available Quarter 2, 1987

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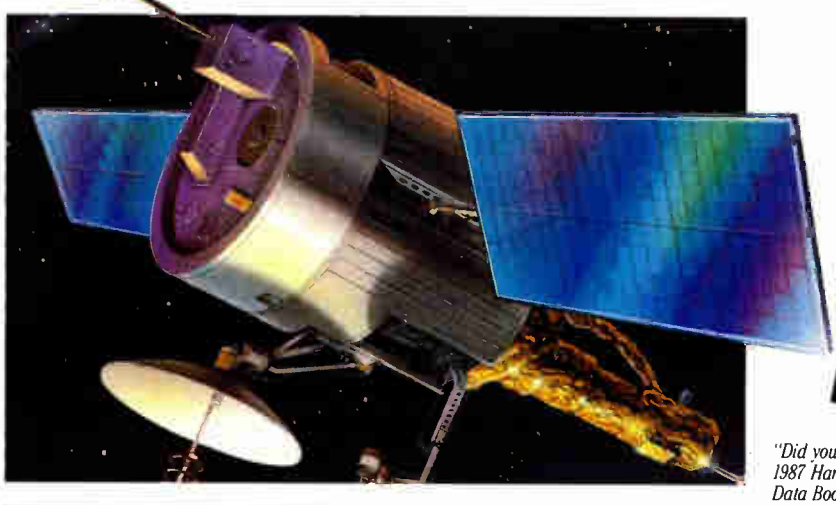

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A BETTER WAY TO PROTECT VLSI CIRCUITS FROM RADIATION

TI's oxide-based processes could replace silicon on sapphire and dielectric isolation

by Samuel Weber

New semiconductor fabrication methods for radiation-hardened integrated-circuit applications are coming that promise to meet the demands of higher-performance devices and greater packing density spawned by the VLSI era. These methods—based on using oxide as an insulator—could replace the old silicon-on-sapphire and dielectric-isolation processes that have long dominated rad-hard applications.

At Texas Instruments Inc., designers are concentrating on four oxide-based processes. They are intended primarily for CMOS applications—which is rapidly becoming the mainstream VLSI technology—but can also handle bipolar circuits.

Of the four oxide-based methods under investigation at TI, two look to be implemented in the near future. One is Simox, for separation by implanted oxygen. Also known as buried-oxide SOI, it offers the best quality single-crystal silicon now available for device fabrication at VLSI densities. The second is wafer bonding, a process first reported by IBM Corp. in 1982. Until recently wafer bonding has been hampered by sensitivity to particulate contamination, but it is attractive to designers since it embodies many of the processing attributes of the present dielectric-isolation technique.

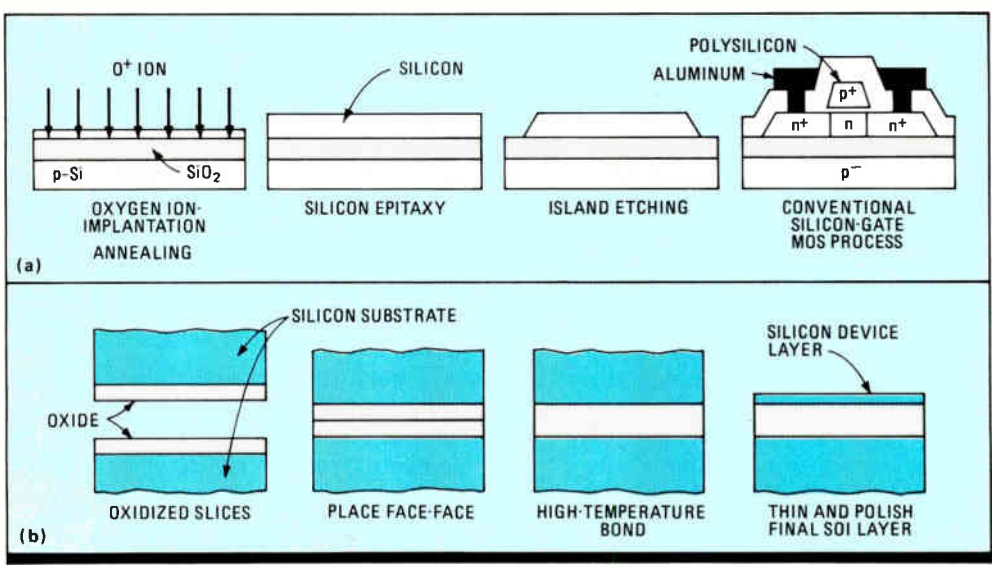
The two other processes are Fipos, for full isolation by porous oxidized silicon, and ZMR, for zone melt recrystallization. Prototype devices have been fabricated on both Fipos and ZMR material, but TI engineers are focusing on the first two techniques because of the excellent materials they produce and because of their commonality with current semiconductor processes.

So far, TI has focused on static random-access memories as implementations of oxide-based methods, because memory devices are well suited fabrication in silicon-on-insulator technology. All four methods are specific implementations of a general process called silicon-on-insulator. So are the two 20-year-old processes that now are used in most rad-hard ICs: silicon-on-sapphire, or SOI, and dielectric isolation.

Although the oxide-based methods are in broad terms related to the two older techniques, the new methods have several advantages over them. Among other things, oxide is inexpensive, particularly compared with sapphire. Also, its use is well understood, since it is the same material that now forms parts of ICs.

More important, an advanced SOI process is needed to overcome the old methods' limitations in VLSI device fabrication. For example, single-poly dielectric-isolation slices have an active device-layer-thickness tolerance of ± 3 μm, while an oxide implant-based process can go down to ± 0.01 μm. The large thickness variation in single-poly dielectric isolation limits packing density to a tank-to-tank spacing of approximately 23 μm. With an oxide-isolated process, the spacing shrinks to 10 μm, but future VLSI requirements will require even tighter spacing, on the order of 2 to 4 μm.

Other drawbacks of the dielectric-isolation pro-



1. LEADERS. TI's leading SOI techniques are Simox (a), which requires adding just two steps to conventional fabrication, and wafer bonding (b), in which two oxidized wafers are sealed face to face.

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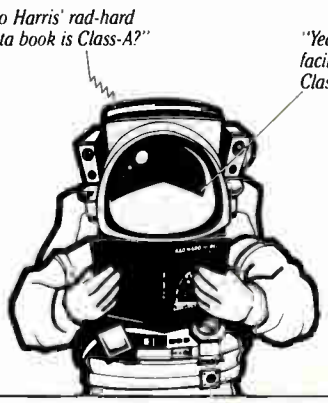

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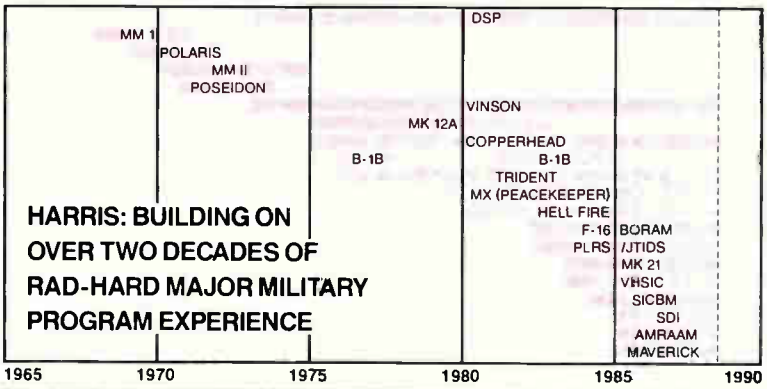

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A RAD-HARD ARRAY FAMILY EVOLVES FROM VHSIC

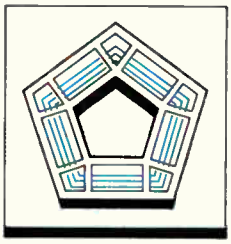
The Defense Department is making heavy demands on semiconductor circuits for the next generation of military systems, but a family of bipolar gate arrays from Honeywell Inc. goes a long way toward giving the Pentagon what it wants. Aimed at advanced military signal-processing applications, the arrays are the kind of circuits that will go into radar, sonar, electronic-warfare, and image-processing systems being developed now for use in the early 1990s.

The requirements for those circuits is formidable. They have to be blazingly fast and very dense. They must consume as little power as possible without sacrificing performance. And for good measure, they should be as resistant to radiation as possible.

To meet these goals, engineers at Honeywell's Solid State Electronics Division in Colorado Springs, Colo., have developed arrays for military applications that require circuit densities ranging from 10,000 to 70,000 gates and clock rates from 50 to 100 MHz. The first array in this family is the HVM10,000 (see fig. 1), a 10,000-gate array developed under the Very High Speed Integrated Circuits Phase 1 Program. It is implemented using current-mode logic, a lower-power variant of emitter-coupled logic that permits significantly higher densities than ECL, providing higher system-level performance.

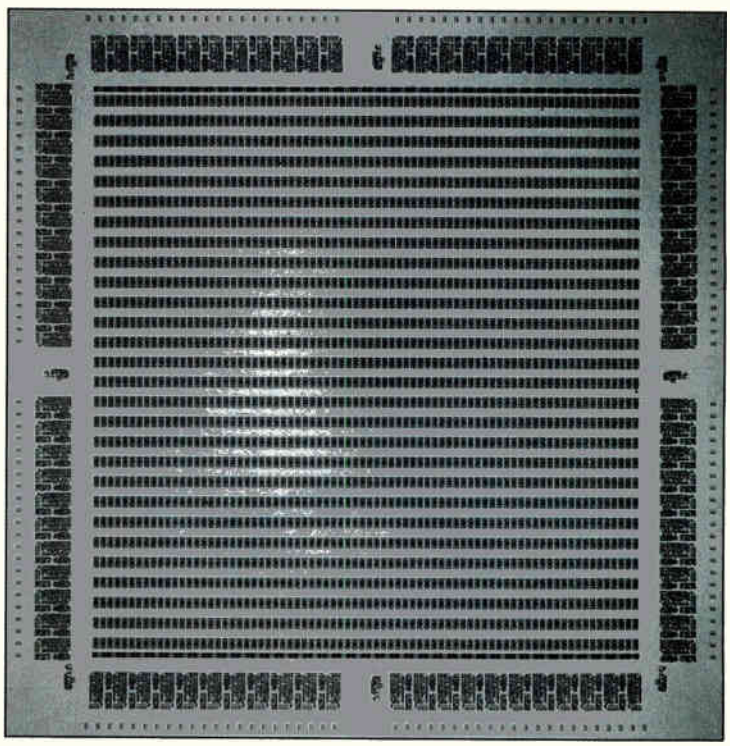
Radiation resistance was added by tinkering with the company's third-generation VHSIC bipolar technology, VDB-III, with which the array is fabricated. A 1.25-μm process, VDB-III is based on nonwalled-emitter structures surrounded by a lightly doped base (see fig. 2). It is also an oxide-isolated process, in which a channel stop implant is used to provide a heavily doped p-region between adjacent devices, says David Still, bipolar design manager. That prevents leakage from buried layer to buried layer. Under pre- and post-radiation conditions, the leakage between adjacent buried layers is caused by the formation of an n-type channel at the interface of the channel stop and the oxide, due to positive charge trapping in the isolation layer.

To make its CML-based arrays radiation-hardened, the company added two steps to its basic process. Backside gettering pulls the defects in the silicon lattice below the active area. It is followed by a neutron irradiation after metalization. These two steps increase the number of recombination sites, decreasing the majority carrier lifetimes of electrons in the substrate and reducing the strength of the buried-layer substrate photocurrents that occur during a radiation burst. As a result, the array meets or exceeds DOD radiation-resistance requirements: to withstand a total dose of 10^6 rads, a transient dosage of 10^9 rads/s for a 20 ns pulse, and a neutron doseage of 10^{15} neturons/cm^2.



The array incorporates three layers of metal, two for macrocell connections and one for power busing. It is capable of handling up to 172 input/output lines and is programmable over a wide range of performance and power options. Depending on complexity and application, typical propagation delay and power of a circuit implemented on the gate array range from about 1.5 ns and 1.3 mW per function for a low-drive, low-power application with a fan-out of 1 and a fan-in of 6, to 580 ps at 4 mW for a high-power, high-drive application with a fan-in of 3 and a fan-out of 16. To expedite circuit design, a library of performance-programmable optimized CML is available. These are macrocells that can be programmed at the cell level by the designer to operate over a wide range of performance and power specifications.

The HVM10,000 is aimed at those military and aerospace applications for which the only alternative to date has been ECL, says David Wick, bipolar product line manager. Used in the same architecture, he says, the CML arrays outperform ECL circuits at the system level. Still says the CML arrays exhibit from 20% to 30% greater logic densities than equivalent ECL arrays.



1. DENSE AND RAD-HARD. Honeywell's 10,000-gate current-mode logic array meets or exceeds the DOD's rad-hard requirements.

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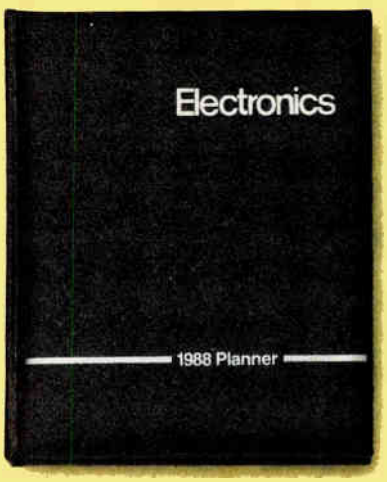

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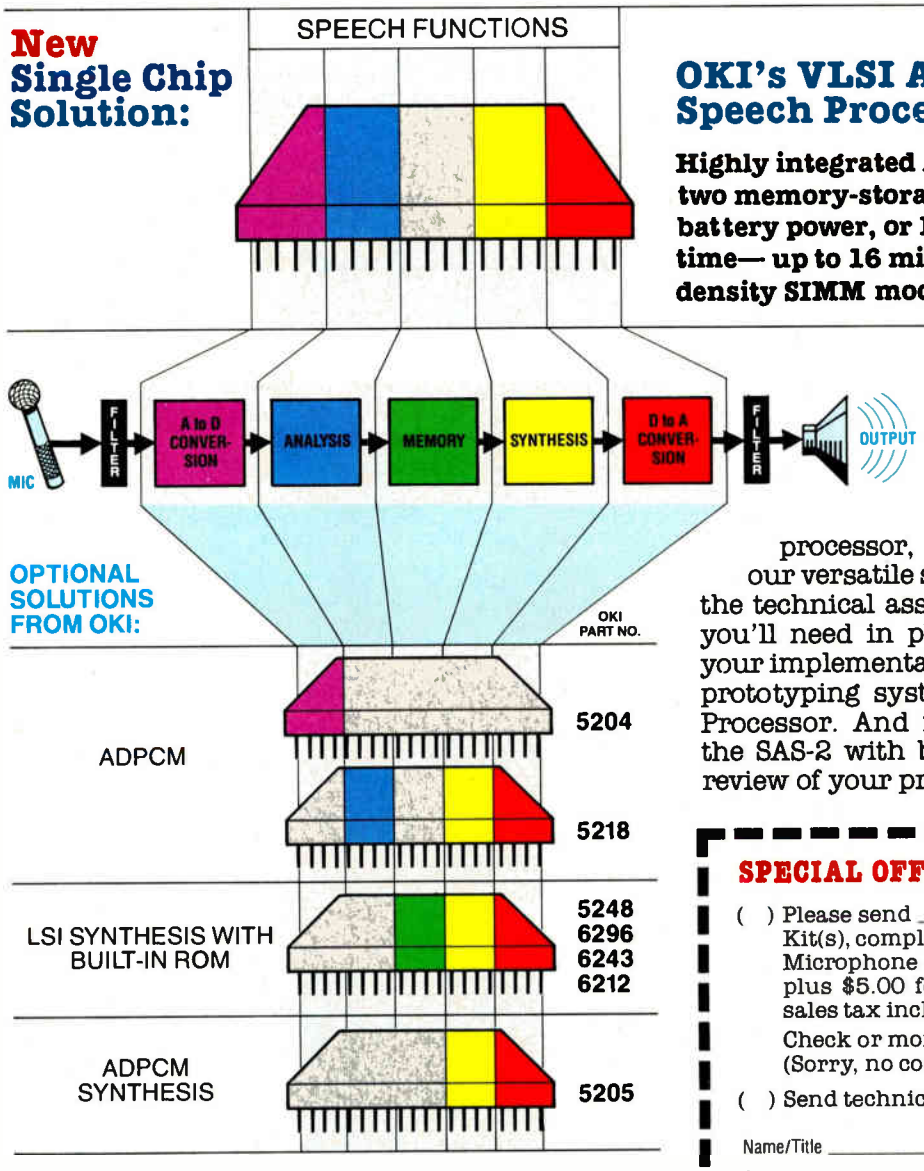

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Max. Clock Freq. (typ)J/K F-F (C_L = 15pF)	150MHz	60MHz	45MHz	2MHz
Quiescent Power Diss. (typ) (GATE)	0.01μW	0.01μW	8mW	0.01μW
Noise Margin $V_{IH(min)}/V_{IL(max)}$	3.5V/1.5V	3.5V/1.5V	2.0V/0.8V	3.5V/1.5V
Output Current $I_{IOH}I(min)/I_{OL}$ (min)	24mA/24mA	4mA/4mA	0.4mA/4mA	0.12mA/ 0.36mA
Op. Volt. Range	2-6V	2-6V	4.75-5.25V	3-18V
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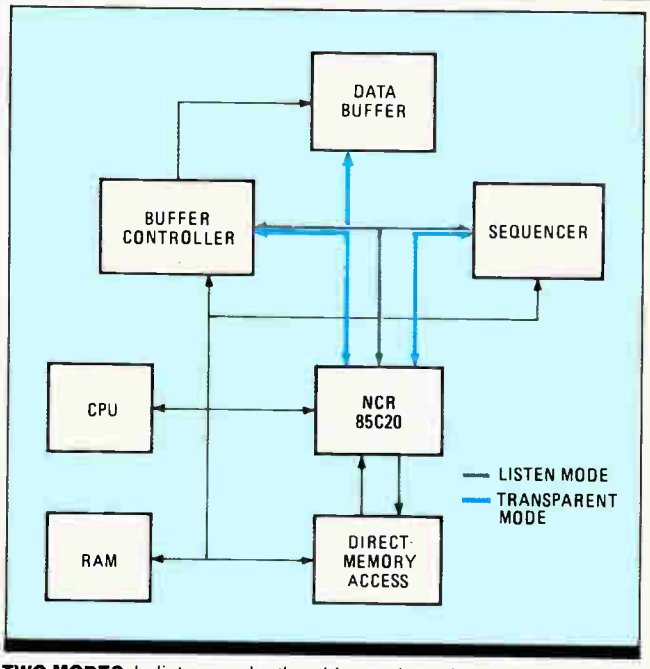
NCR'S 85C20 IS ALSO FIRST TO IMPLEMENT ANSI STANDARD

Designers of controllers for 5¼-in. write-once, continuous-servo optical-disk drives now have an easy way to handle error detection and correction according to the proposed guidelines from the American National Standards Institute. They can harness a single chip from NCR Corp.'s Microelectronics Division with readily available error-correcting software.

Fabricated in NCR's 2-μm, standard-cell CMOS technology, the 85C20 monitors data streams up to 24 Mbits/s and detects errors in up to 80 random bytes per 1,024-byte sector of optical-disk data without significant delay, says the Colorado Springs, Colo., division of the Dayton, Ohio, company.

Available in sample quantities next month, the chip is an early entry in the race to field a solution compliant with recommendations from ANSI's X3B11 committee on 5¼-in. WORM (for write-once, read-many-times) drives.



TWO MODES. In listen mode, the chip monitors the sequencer-buffer controller data path; in transparent mode, data flows directly through.

ECONOMICAL. The 85C20 uses a version of the X3B11-recommended Reed-Solomon Long Distance Code. NCR licenses the code from Data Systems Technology Corp., Broomfield, Colo. Although it performs only error detection—leaving correction to software—this solution will continue to be more cost-effective than an all-hardware approach until optical-drive data rates go well beyond their current levels of about 5 to 10 Mbits/s, says Harold E. Mason, NCR 85C20 project leader. This won't occur until 1990 or later, he says.

The hardware/software scheme's disadvantage in speed compared with an all-hardware implementation can be overcome with data buffers that have insignificant impact on overall system cost. "It's very easy to get the software to perform the corrections and still keep the data flowing," Mason says. Using a 20-Kbyte buffer memory for speed matching and error-correction delay smoothing, the 85C20 will be fast enough for real-time optical-disk applications, says Neal Glover, Data Systems Technology president.

The 85C20 can be used in either of two modes. In listen mode, the CMOS part monitors the byte-wide data path between the system sequencer and buffer controller to generate redundancy and syndrome bytes. In the transparent mode, the bus data flows directly through the 85C20. Once the syndrome bytes are generated—and an error detected—the system microprocessor uses algorithms stored in read-only memory to make corrections. The 85C20 comes in both a standard 44-pin plastic leaded chip carrier and in a 28-pin PLCC.

Users can develop their own firmware based on publicly available Reed-Solomon algorithms, NCR says, or they may use optimized codes developed by Data Systems Technology. Software for Intel Corp.'s 8088, Motorola Inc.'s 68HC11 and 68000 processors, and Zilog Corp.'s Z80 is available from Data Systems Technology for a one-time $20,000 licensing fee, says Glover. Data Systems Technology plans to develop codes for other processors if demand warrants.

The NCR chip targets only 5¼-in. continuous-servo drives, and is not suitable for sampled-servo drives, an alternative tracking method supported by the standards. But NCR says the chip can be used with 3½-in. WORM drives and erasable optical drives. Its 24-Mbit/s data rate also makes it suitable for magnetic-disk-drive applications.

NCR won't be alone in the market for long. Western Digital Corp., Irvine, Calif., plans to field samples of a similar chip in January. Like the 85C20, Western Digital's WD60C80 will use Reed-Solomon algorithms supplied by Data Systems Technology, says Kenneth J. Hallam, Western Digital director of planning. Pricing on the WD60C80 has not yet been set, but will be "under $20" in 1,000-unit quantities, Hallam says.

NCR's 85C20 will cost $23.10 in 1,000-unit quantities when it becomes available in volume in March. Since it is a standard-cell device, says Mason, it will adapt more readily to market conditions than the full-custom Western Digital part.

The NCR 85C20 works by using a Long-Distance-Code implemented in shift registers and on-chip linear feedback networks. These generate redundancy "check-bit" bytes during data writes and generate syndrome bytes—patterns of check-bit mismatches—when the data is read off the disk.

The redundancy bytes are written onto the disk in interleaved fashion following the data field. They form a unique code for the data being protected. When the data is read back, the syndrome bytes (equal in number to the redundancy bytes) are used to produce two status bytes and pointer fields that tell the system microprocessor whether errors are present, and also indicate which interleaves contain the errors.

The 85C20 is programmable for two to 16 redundancy bytes per interleave, in increments of two. When all 16 redundancy bytes are used, errors can be detected in up to eight random bytes per interleave. The number of interleaves per 512-byte or 1,024-byte sector is programmable between three and 10.

Other 85C20 programmability features include the user's option to store syndrome bytes, status bytes, and pointer fields following a read. They can be stored in the system data buffer or—using a direct memory-access channel—in the central processor memory, where the CPU has easier access to them.

–Wesley R. Iversen

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CMOS A-to-D CONVERTER RUNS TWICE AS FAST

A fast, flexible interface to microprocessors, plus a transistor switch-clamp device that speeds the discharge of nodal capacitance, together add up to 2½ times faster conversions than other CMOS parts for Precision Monolithics Inc.'s 8-bit CMOS analog-to-digital converter. Boasting conversion times as low as 6 μs, the ADC-908 also dissipates just half the power of equivalent bipolar successive-approximation converters.

Precision Monolithics' part will be functionally compatible with the market leader, the AD7574 from Analog Devices Inc. and is the Santa Clara, Calif., company's first proprietary CMOS ADC chip. Its power savings and speed are due to a silicon-gate technology using a thin-film to create highly accurate resistors compared with more commonly used diffusion processes, says Walter Heinzer, marketing manager of new data-conversion products. The process gives a faster interface of the converter to host processors, says Heinzer.

AUTOMATIC START. The interface design itself targets ease of use and is implemented with static random-access memories and read-only memories. Data conversion is automatically started at the previous cycle's conclusion. A busy signal to the microprocessor can enable the host to generate wait states in low-cost systems.

In the heart of the converter, the designers have added a transistor switch-clamp device to the summing node to help discharge capacitance and speed up the analog-to-digital work. The quick discharge of nodal capacitance enables the part to make faster decisions on the digital output values, says Heinzer. The converter's summing junction has low-noise margins for clean, quick processing of analog outputs into ADC output codes without hysteresis or oscillation.

The 18-pin ADC-908, like Analog Devices' 7574, has a maximum integral nonlinearity specification of one-half least significant bit and three-fourths LSB differential nonlinearity. But the conversion time of the Precision Monolithics converter can be as low as 6 μs maximum compared with 15 μs for the 7574. Power dissipation of the ADC-908 is 15-mW maximum standby running with a +5-V power supply. (The part, like the equivalent Analog Devices converter, requires a –10-V reference voltage.)

The ADC-908 will generate internal clock signals with a connected external resistor and capacitor. To run at the maximum 6-μs conversion times, the part needs an external 1.35 MHz clock. The ADC-908, which has guaranteed monotonicity, offers data access times of 120-ns and has a data hold time of 20 ns.

The analog input resistance of the part is 10,000 Ω minimum. The converter, like the older 7574 part, will have an untrimmed gain error of ±4.5 LSB and an untrimmed offset error of ±50 mV.

The 8-bit ADC is available in commercial, industrial, and military temperature ranges. It is also being housed in 300-mil-wide 18-pin dual in-line packages and surface-mountable small-outline packages. In 100-piece quantities, the commercial parts cost $7.50 each.

– J. Robert Lineback

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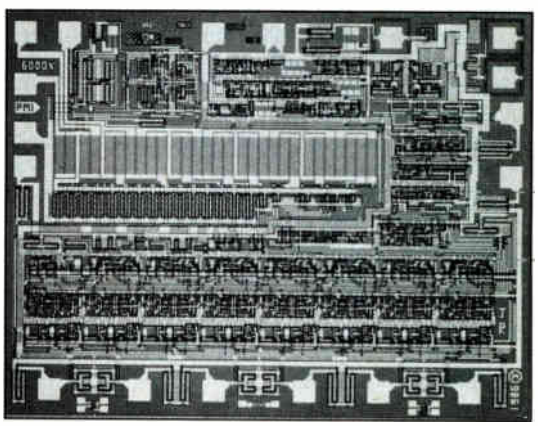

LOW POWER. Thin-film silicon-gate technology boosts the ADC-908's speed and reduces power consumption.

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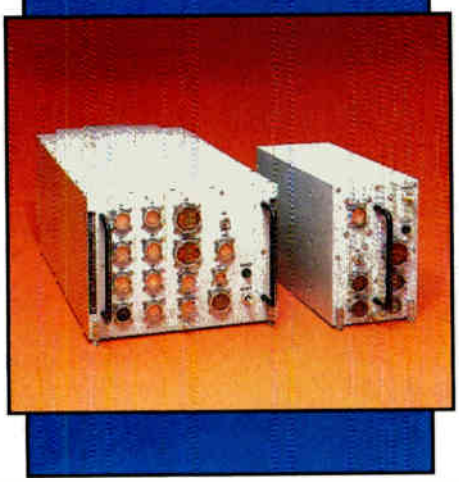

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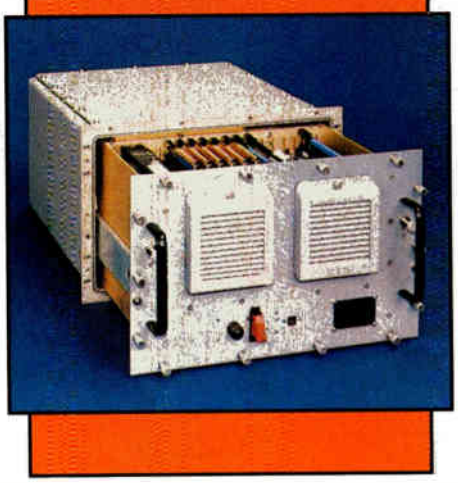

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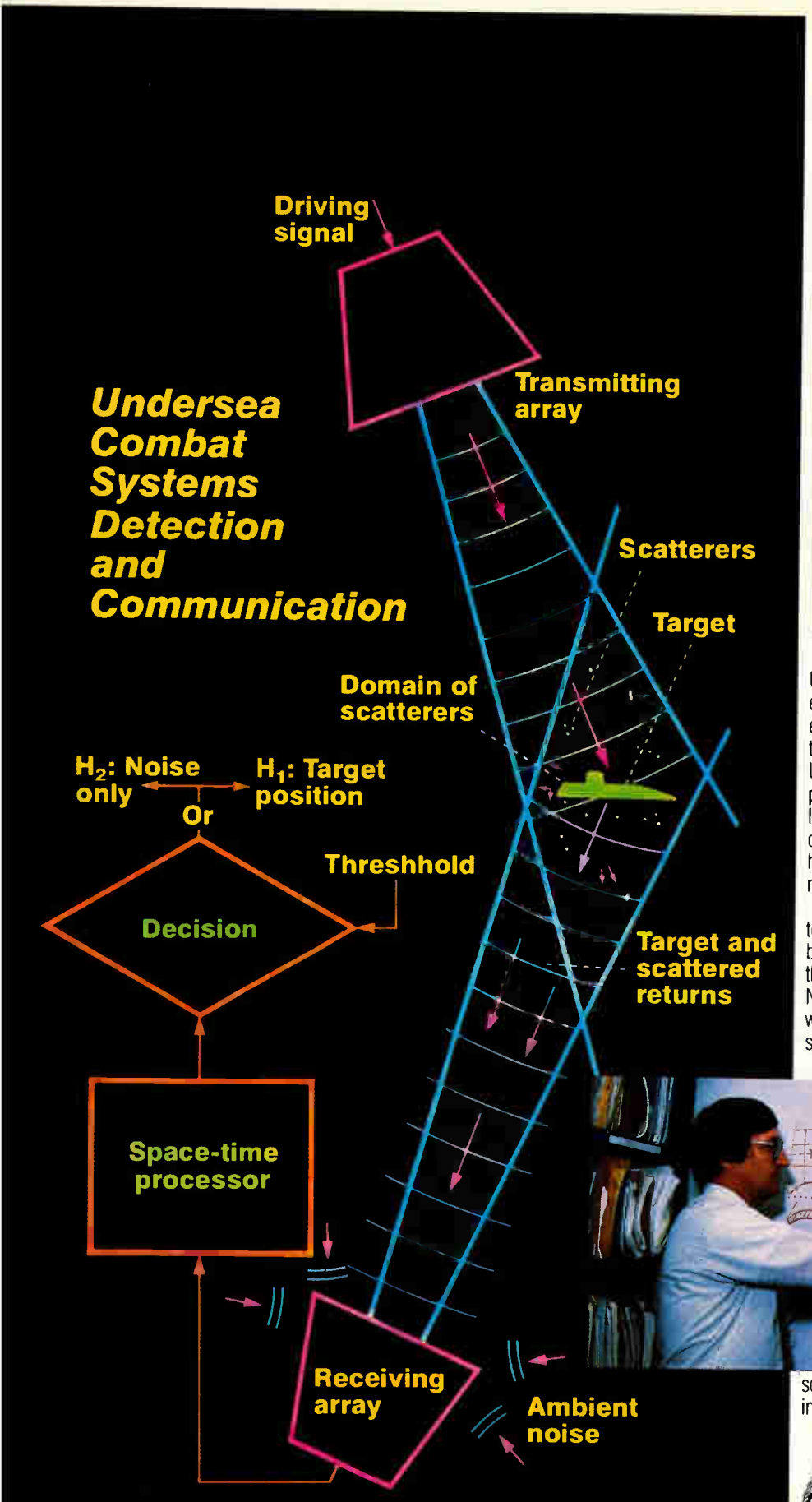

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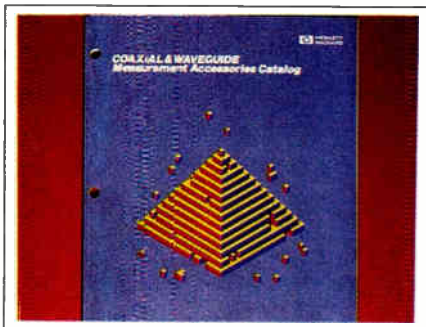

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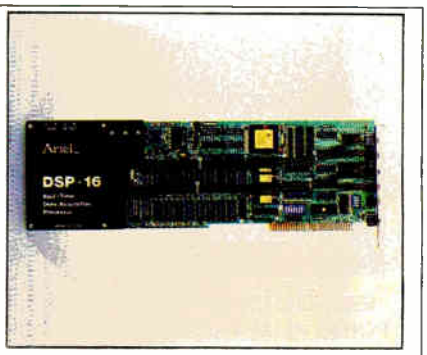

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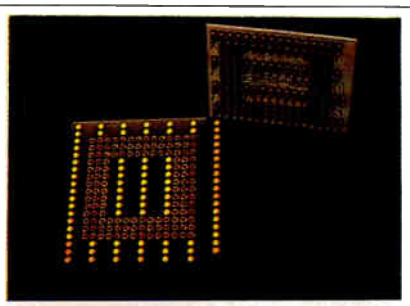

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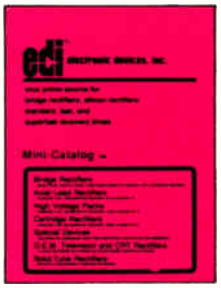

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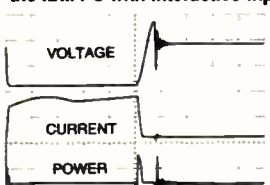

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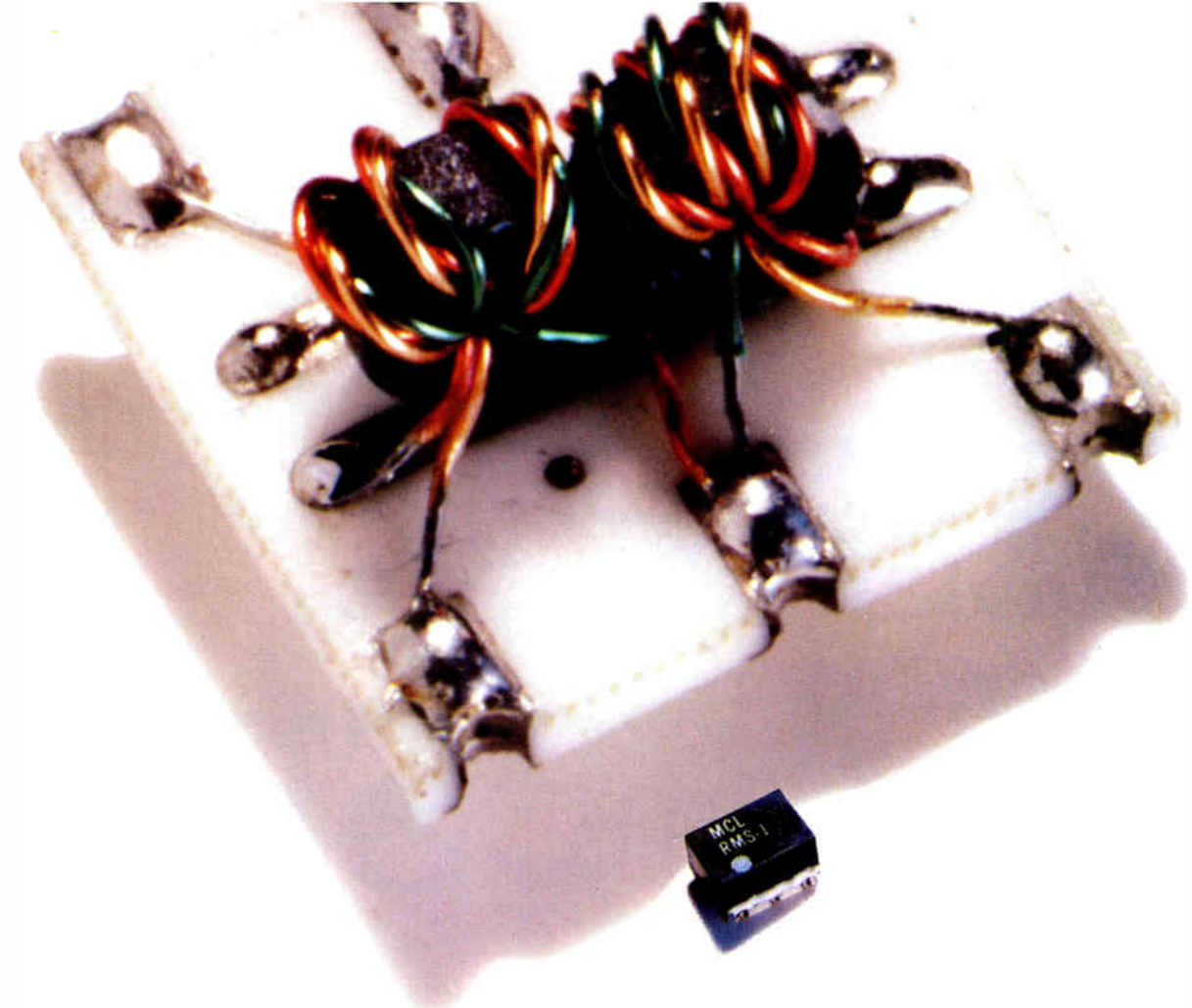

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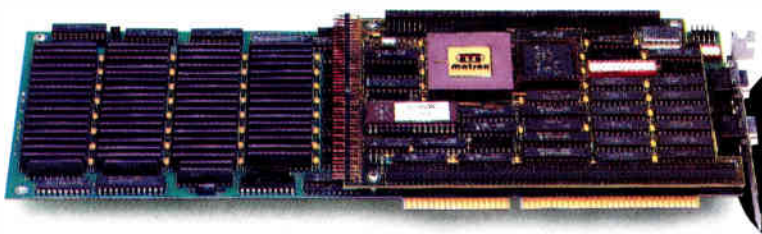

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