

**LSI LOGIC'S GIANT GATE ARRAY BREAKS THE RECORD/55
A WAY TO RUN TWO OPERATING SYSTEMS SIDE BY SIDE/68**

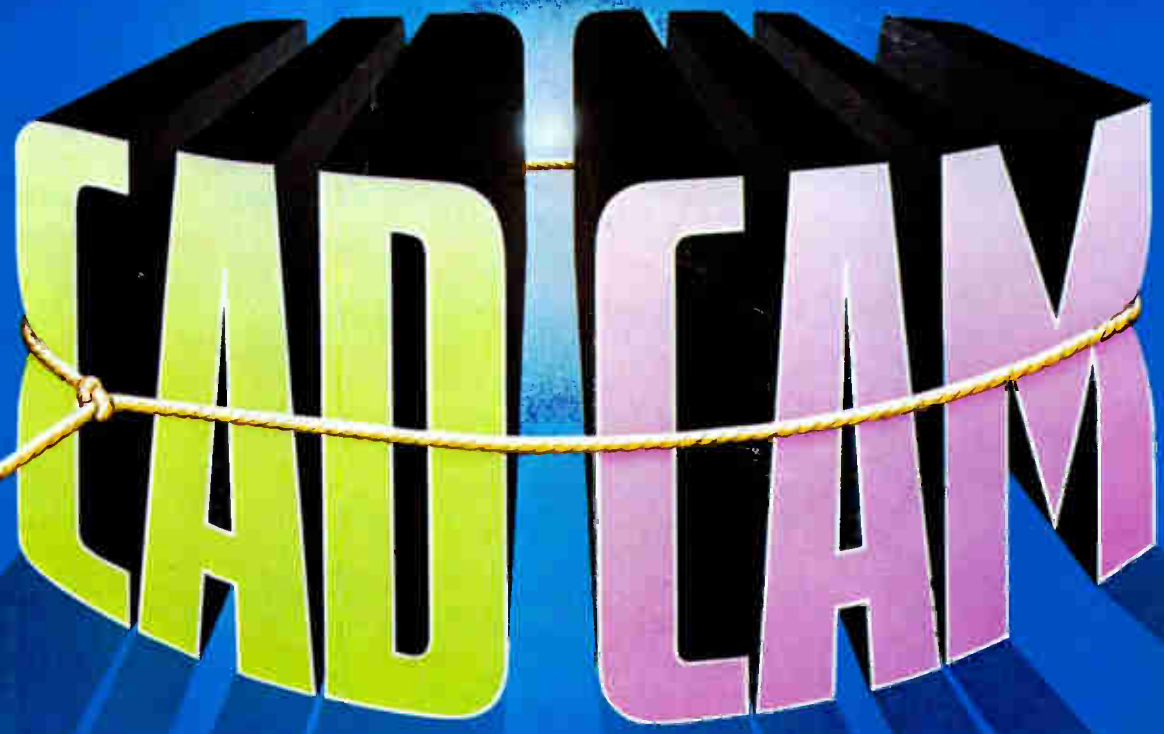
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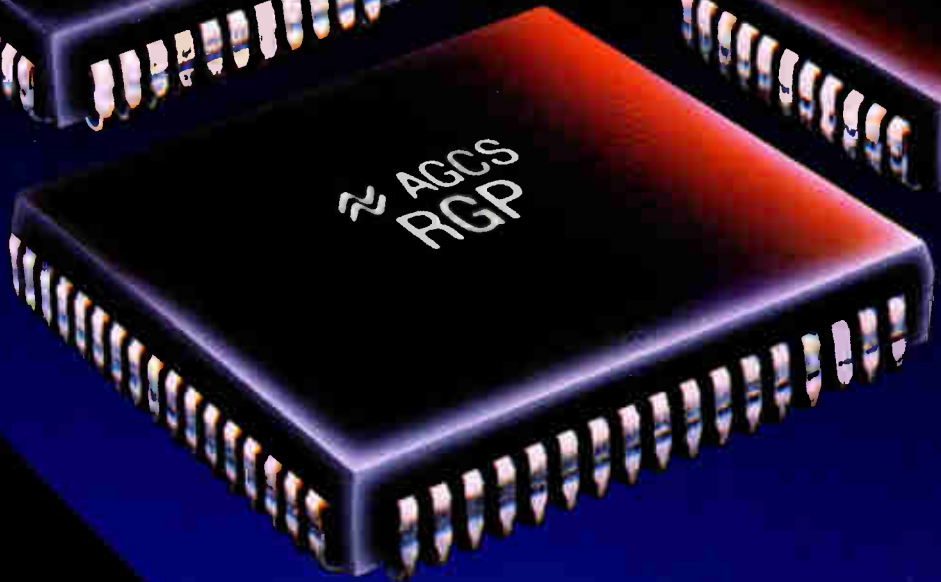
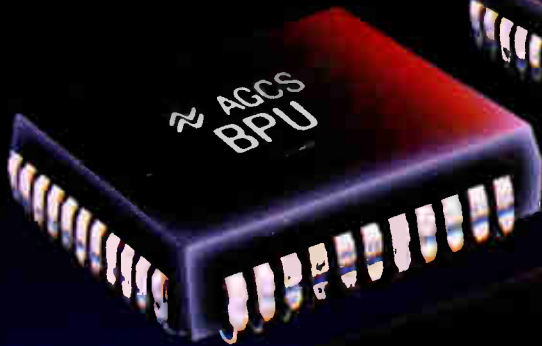
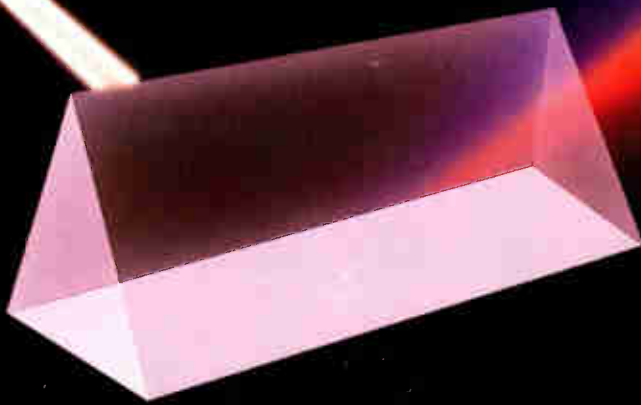
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**CALAY AIMS TO USE CAD DATA
TO BUILD AND LOAD PC BOARDS/61**

**NOW, WILL COMPUTER-AIDED MANUFACTURING
FINALLY CATCH ON?/65**



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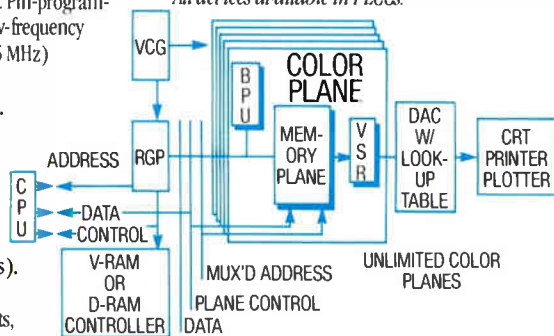
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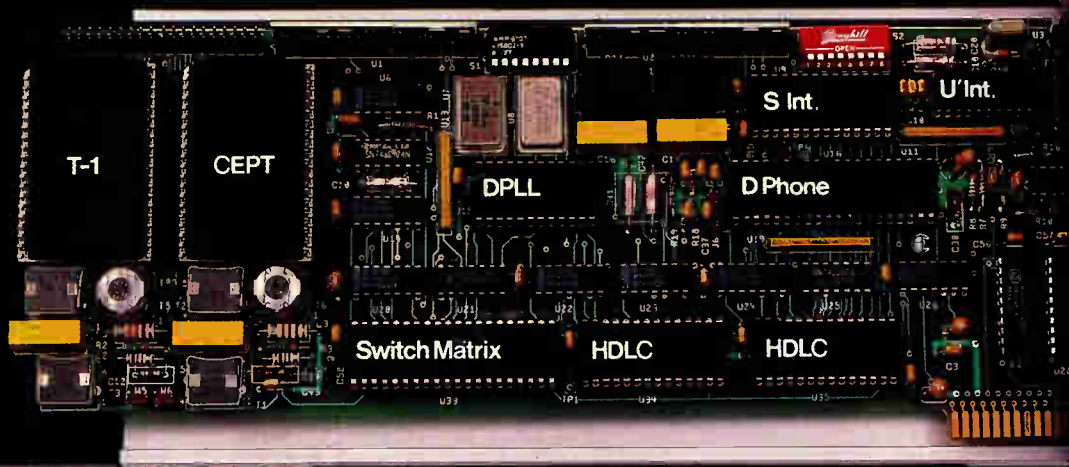
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Covering major stories is nothing new for Larry Curran, our Boston-based veteran who covers computers and communications developments along the East Coast. His latest contribution is the Technology to Watch on BBN Advanced Computer Inc.'s new Butterfly developments on p.77 of this issue. In the article, he interprets how important BBN's parallel-processing architecture and new Mach 1000 operating system are to a computer industry that appears to be migrating to parallel processing for engineering and scientific applications.

Larry has spent a dozen of his 25 years in the business tracking the industry for *Electronics*. "I think my experience gives me a special perspective that's reflected in my coverage," he says. "I was in on the milestone announcements, such as Digital Equipment Corp.'s PDP-11/70 in the early 1970s and Data General Corp.'s Micronova in the mid 1970s. And from our Los Angeles bureau, I also covered Motorola Inc. in Phoenix—when it was a pioneer in emitter-coupled logic in the late 1960s and early 1970s, and ECL was supposed to take over the world."

Also while in Los Angeles, Larry was in on such major developments as ion-implantation as a new technology to boost the speed of MOS devices, and the emergence of what was then Rockwell's Autonetics division as the first U.S. supplier of MOS calculator circuits to Japan's Sharp Corp. Those latter developments all came in the early 1970s, and Larry was on top of them from our West Coast base, where Larry Waller



CURRAN: Keeping focused on the computer business.

now holds forth. After he was transferred to Boston, where the climate seems to favor computer companies more than semiconductor firms, Curran anchored what was probably the earliest special on personal computing more than a decade ago. That opus ran in a 1976 issue—some seven years before the IBM PC turned the personal-computing world upside down.

And the beat goes on for Larry now that he is covering computers from that important hub of the industry. Since rejoining *Electronics* April 1, Larry has reported on Apollo's booming growth in work stations, Data General's plans to recover from recent setbacks, and Digital Equipment's major new MicroVAX 3500/3600 family.

He finds a special challenge in his computer beat. "Unlike semiconductor companies, computer manufacturers historically don't leak information about products in development before the ink is dry on the back-of-the-envelope design." But he believes that this guarded stance lends zest to his job as he applies the *Electronics* touch to the story he's covering: finding the unique angle, be it innovative use of semiconductors, packaging, architecture, or software, then putting it all in perspective.

Right now, he says, the computer bandwagon is rolling for reduced-instruction-set architectures. But Larry is skeptical. "I saw one sure thing, ECL, fail to win everything in sight because MOS moved so quickly. While I'm sure RISC is finding its niche, experience tells me it will face a challenging technology before long."

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Electronics

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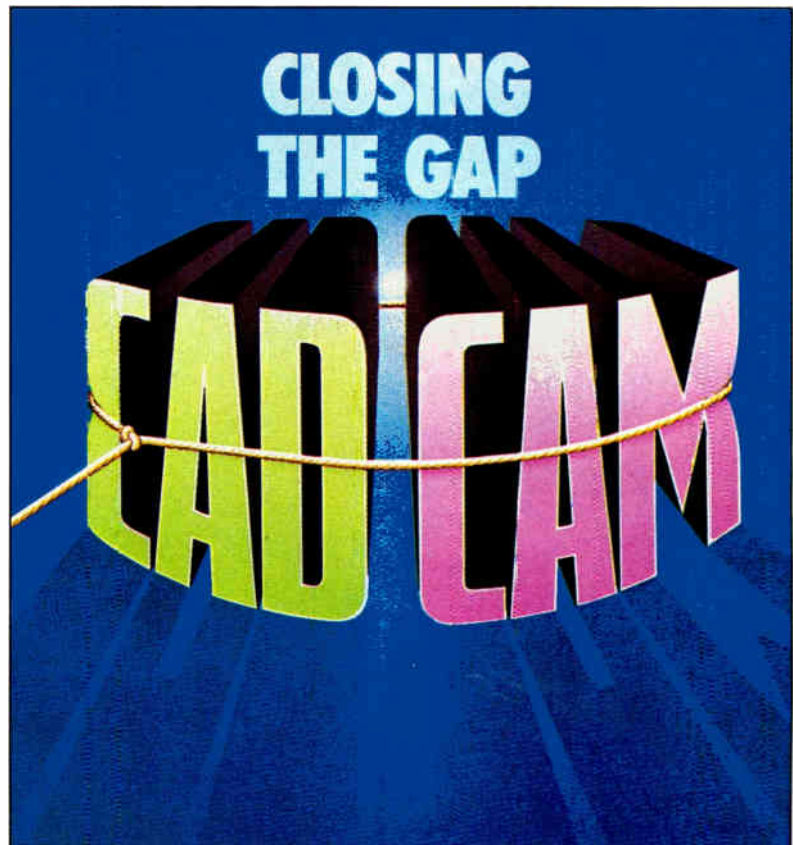
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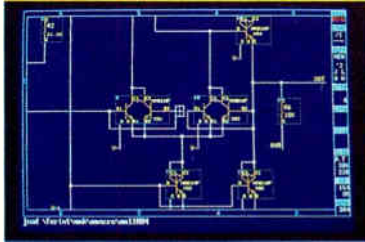
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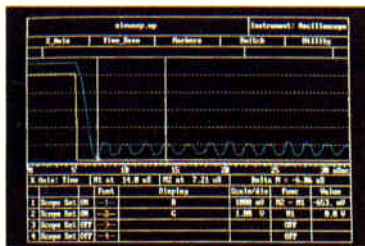


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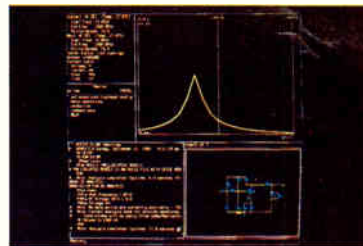
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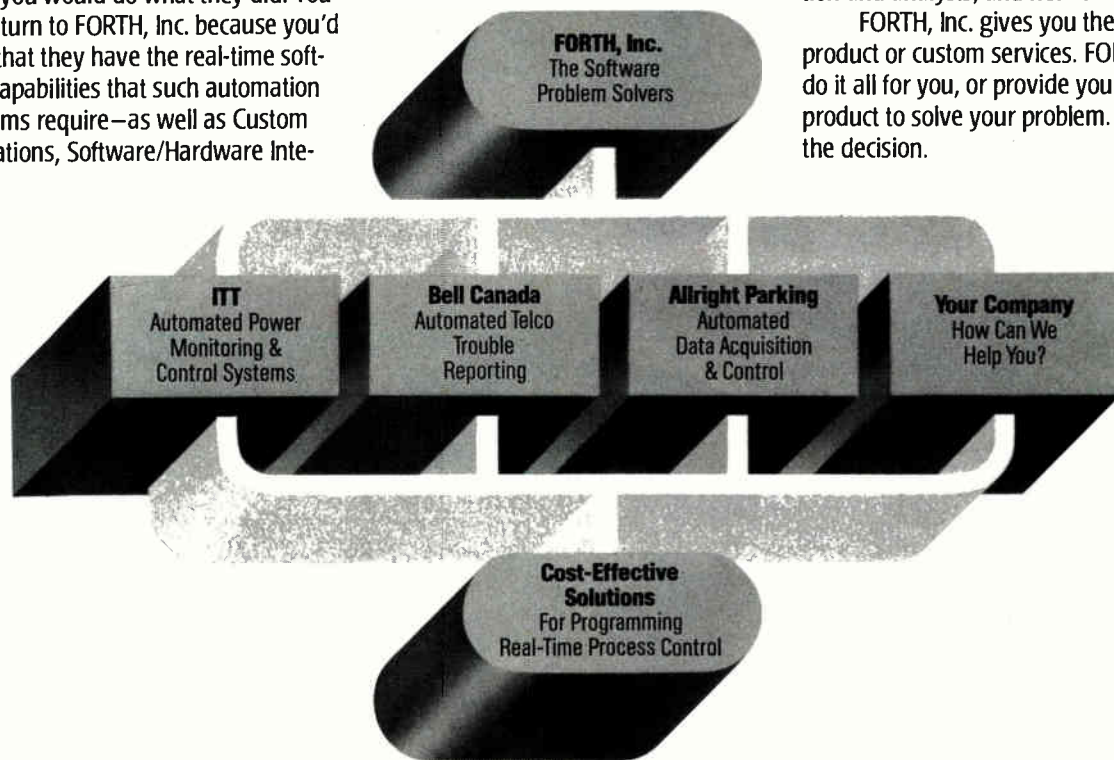
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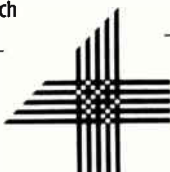
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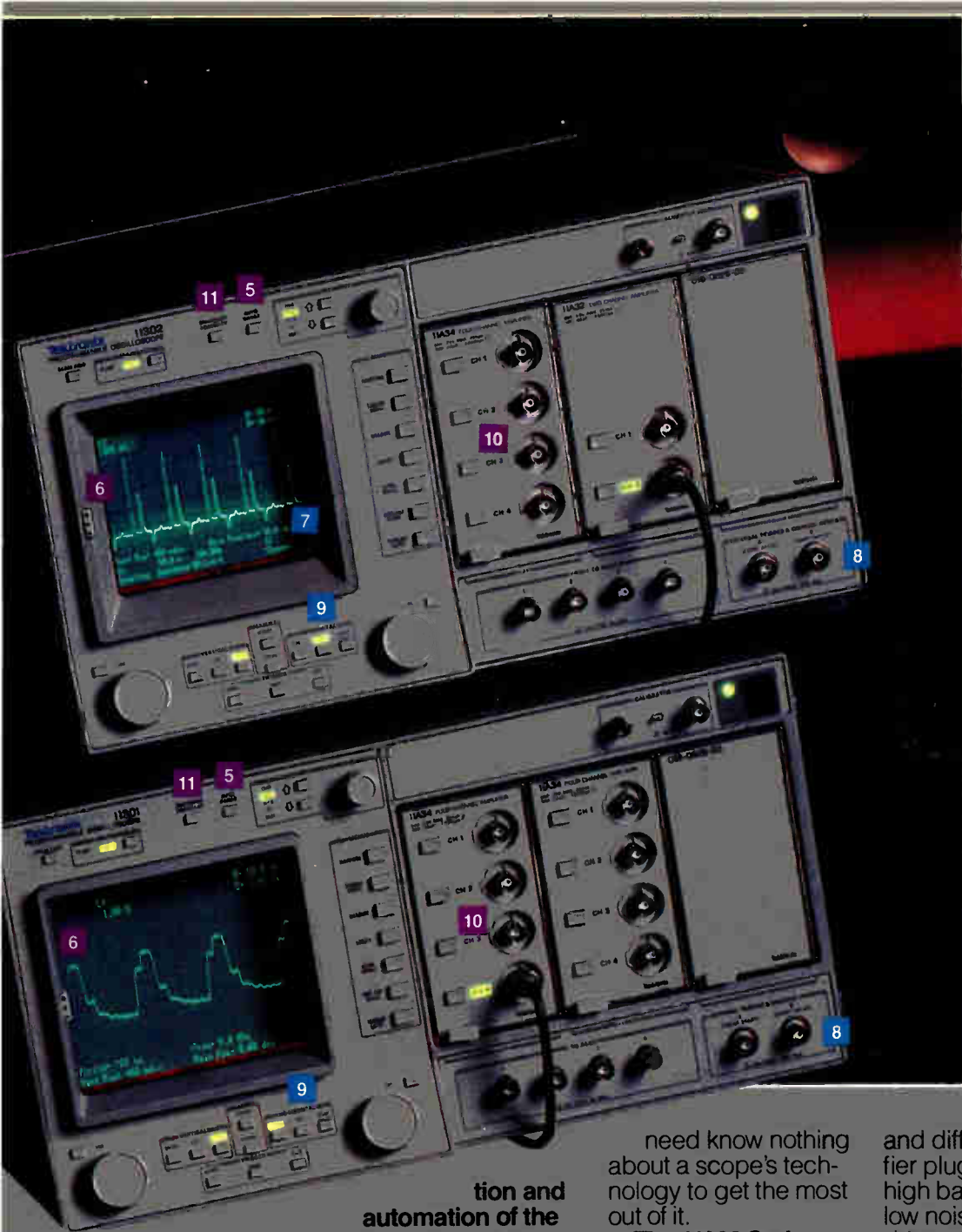
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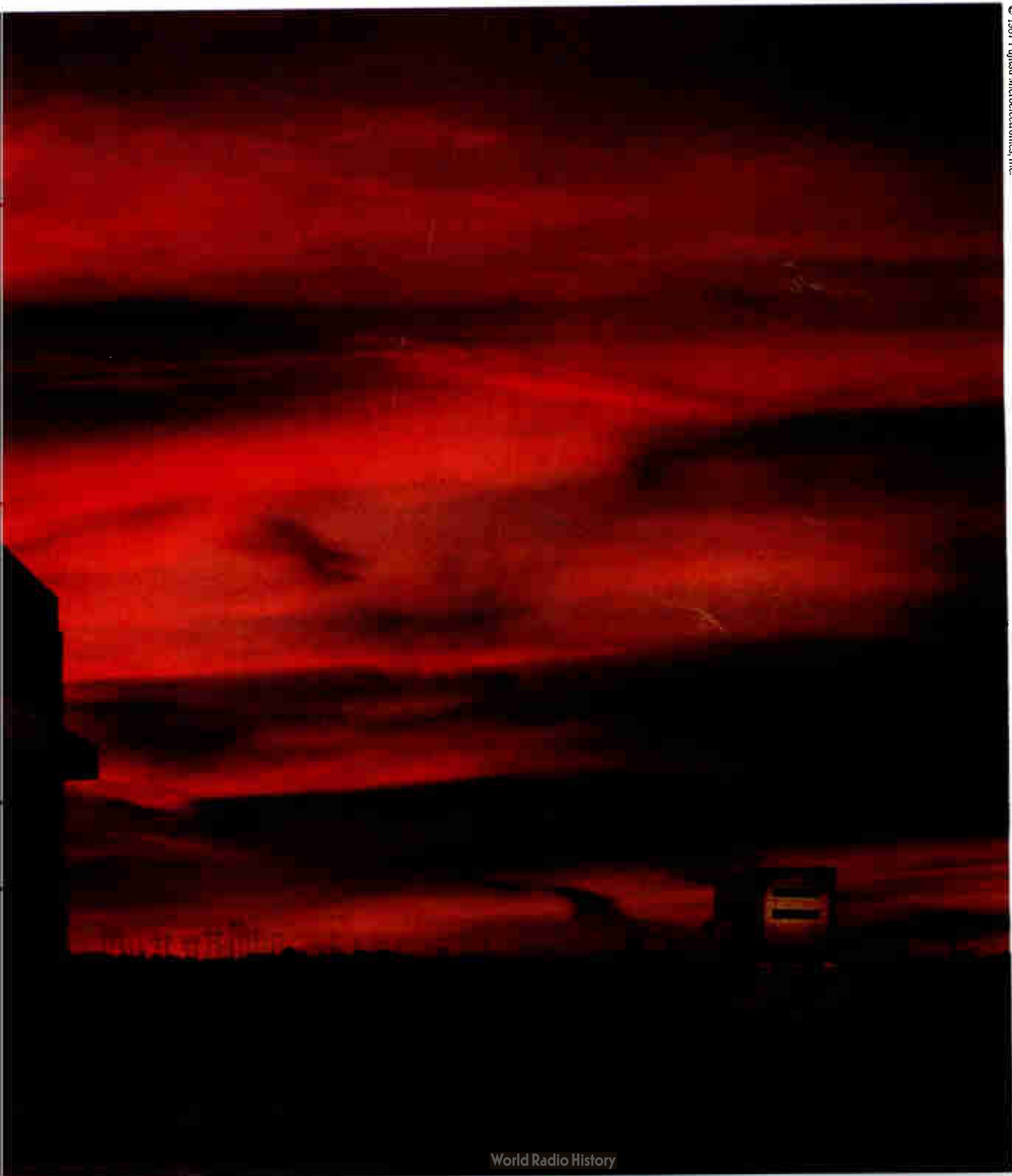
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 **Electronics**

ELECTRONICS NEWSLETTER

INTEL'S 80386 OUTDOES MOTOROLA'S 68020 IN HEAD-TO-HEAD TESTS ...

A benchmark study pitting the two leading 32-bit microprocessors—Motorola Inc.'s 68020 and Intel Corp.'s 80386—has shown the 386 to be "consistently faster than the 68020," says Elizabeth D. Rather, president of Forth Inc., of Manhattan Beach, Calif. Rather's firm supplies polyForth operating systems for both chips, as well as other processors. The head-to-head test compared similarly configured 16-MHz parts, each with cache memory and a polyForth program. The benchmark ran extensive tests that exercised all functions, Rather says. One measurement, a set of 10,000 multiply/divides, for example, showed the 386 to require only 156 ms compared to 244 ms for the Motorola chip. Rather says the results are surprising because, until the tests were completed, "we all thought the 68020 was faster." □

... AS THE LATEST 32-BIT MICROPROCESSORS HIT THE STREET

Get ready for the second-generation 32-bit microprocessors. Motorola Inc. and National Semiconductor Corp. are expected to unveil their newest entries before the end of October. Motorola's 68030 will officially bow in New York Oct. 29, but the company is already taking orders for volume shipments. The price will be about \$400 for a 16.7-MHz 68030 and \$550 for a 20-MHz version in unit quantities. The chip is twice as fast as its predecessor, the 68020, and boasts additional on-chip cache, integrated memory management, and increased parallel functions. NCR, Apple Computer, Unisys, and Sun Microsystems are all expected to use the new part. National, meanwhile, is just beginning to ship samples of its 32532, which adds on-chip data, an instruction cache, and memory management to the core of the existing 32032. A 20-MHz version is due in the first quarter of 1988, and a 30-MHz version will follow later. □

APOLLO'S NEW SERVER LOCKS OUT USERS THAT DON'T HAVE 'KEYS'

Apollo Computer Inc. is touting a more effective way to license and administer software usage on networks and will begin shipping the system, called Network License Server, in March. With NLS, software vendors license their programs with the condition that only a preset number of people will have access at any one time. Once the software is installed, it is guarded by a "lock" for which there is a limited number of "keys," limiting the number of concurrent users. NLS provides logs that monitor the use of application packages, giving license administrators better control over requests for licenses. NLS will work initially only on Apollo work stations, but will eventually run on Digital Equipment and Sun Microsystems machines. A 50-key NLS will carry a one-time charge of \$4,000 or an annual fee of \$1,000. The software-lock license carries a one-time charge of \$5,000. □

AIR FORCE ORDERED TO REWRITE RFP, BUT IT CAN SPECIFY UNIX V

The Air Force was within its rights in specifying the use of AT&T Co.'s Unix System V when it sought bids for a planned order of 20,000 mid-size computers, says the General Services Administration Board of Contract Appeals. Digital Equipment Corp. and Wang Laboratories Inc. had filed suit against the Air Force, claiming that its request for proposals unfairly favored AT&T and other supporters of its System V Interface Definition. The appeals board didn't let the Air Force off completely, however. It ordered the RFP rewritten to eliminate "ambiguities and bias" resulting from the use of a proprietary AT&T test program. DEC will now adopt a wait-and-see posture, a spokesman says: "Whether we can go ahead with our bid and be competitive depends on the how the Air Force implements the decision." □



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PRODUCTS NEWSLETTER

NEC'S CACHE-CONTROLLER CHIPS CAN RUN 32 GIGABYTES...

A cache-controller chip from NEC Corp. that handles up to 128 Kbytes of memory can be cascaded—a feature competitors don't offer. The theoretical limit is 250 cascaded chips controlling 32 gigabytes. Also, other cache controllers work only with a target processor—Intel Corp.'s 80386, for example—but the IC from the Tokyo-based Microcomputer Products Division supports competitors' 16- and 32-bit processors as well as its own V-Series chips. For cache memory of 32 Kbytes or larger, hit rate is 97% or higher. The chip offers a selection of cache-search algorithms: direct mapping, two-way associative, and four-way associative. Implemented in 1.2 μm CMOS, the μPD7164 will be offered in sample quantities in December and go into production in April. Sample price in Japan is 40,000 yen each. U. S. introduction is set for November, but pricing is not available. \square

... WHILE TI'S CACHE-TAG CHIP WORKS WITH THE 68030 AT 40 MHz

Built to run with the 32-bit MC68030 microprocessor from Motorola Inc., Texas Instruments Inc.'s ACT2155 cache-address comparator and data random-access memory features a fast 2-bit counter and bus-interrupt interfaces that keep up with the 68030 at its announced 20-MHz speed—and up to the possible 40MHz of the future. The 1- μm CMOS chip uses its counter to generate the next addresses for internal cache storage during burst-fill mode, and the extra interface logic lets slower static RAMs serve the processor, says the Dallas company. A 2155 rated for 25-ns access easily supports a 20-MHz 68030; and an 18-ns 2155 supports 40-MHz speeds. Cache tags that are more generic would have to be 7 to 10 ns faster than this, and since the Ti part favors no specific caching scheme, memory designers have more freedom than with a highly integrated controller, such as NEC's $\mu\text{mPD7164}$. The 44-pin device sells for \$22.50 each. \square

AST'S PC RUNS LIKE A PS/2 BUT USES AT-COMPATIBLE BOARDS

AST Research Inc. is bidding to steal some of the thunder of IBM's Personal System/2 with a multitasking 20-MHz machine that offers PS/2-like performance but works with the vast base of add-on boards and hardware for IBM's Personal Computer AT. Based on Intel Corp.'s 80386 microprocessor, the Premium/386 uses an arbitrated bus architecture called Smartslot that provides minicomputer capabilities by accommodating multiple coprocessors. Smartslot has three buses: a 32-bit pathway from processor to memory, a feature bus, and an arbitration bus for efficient management of memory and peripherals. Available in January, the Irvine, Calif., company's Premium/386 comes in four models, priced between \$4,695 and \$8,995. \square

AI SOFTWARE DIGS NEW KNOWLEDGE OUT OF LARGE DATA BASES

Software is now at hand that leverages statistical techniques with artificial intelligence to extract knowledge from large data bases. Called IXL: The Machine Learning System, the package analyzes data in dBase III, Lotus, and ASCII formats for hidden knowledge and then formulates simple rules to illustrate the previously unknown relationships, says its maker, IntelligenceWare Inc. of Los Angeles. Running on IBM Corp. Personal Computers and compatibles, IXL handles inexact or incomplete data, and users can specify a level of acceptable error. It does not require preprogramming to analyze a data base. Instead, it accepts defined concepts—such as "large company" or "Pacific Region"—that direct the analysis toward the type of information sought. The \$490 program, available now, can process large data bases overnight, allowing users to collect its results in the morning. \square

Electronics

ASIC HOUSES RUSH TO ADD ANALOG FUNCTIONS TO LIBRARIES

MIXED CHIPS COULD TOTAL HALF OF 1990'S CELL-BASED MARKET

SANTA CLARA, CALIF.

It's turnabout time for the semicustom-chip market. After years of having digital integrated circuits chop away at the age-old turf of analog electronics, there is a sharply accelerating trend the other way as analog functions grow in many digital standard-cell libraries. Now, on-chip linear devices are becoming a key selling point in application-specific ICs.

The result is that demand for analog functions in ASIC libraries should continue to surge, says National Semiconductor Corp. National estimates that only \$50 million of 1987's batch of cell-based semicustom chips will have some analog functions on board (see graph). But by 1990, nearly half of a cell-based ASIC market estimated to reach \$3.5 billion will require analog functions, says Thomas Wong, strategic marketing manager for National's ASIC Division. Some projections are even higher. In Dallas, ASIC managers at National's archival, Texas Instruments Inc., place the figure closer to 60%.

At least one TI executive admits to being amazed at his company's spiraling growth projections. "That number nearly floored me," says Tom Engibous, vice president in charge of TI's linear chip operation, which is handling the development of the LinASIC library.

No matter which estimate is more accurate, it's a sure bet that any market that could grow by some \$2 billion in the next three years will get crowded in a hurry. And National has just become the latest to join the ranks of ASIC suppliers who are jumping on the bandwagon—among them some of the biggest names in the business.

The Santa Clara, Calif., chip manufacturer is rolling out the first linear building blocks for its standard digital 2- μ m double-level-metal CMOS library. A leading supplier of analog chips, National is adapting basic linear functions for its standard digital CMOS process technology. The company is working too on additional technology modules—such as biCMOS and capacitor-oriented process steps—for high-performance analog functions.

National joins an emerging movement among digital ASIC producers and linear-digital niche suppliers, who are scrambling to offer semicustom products spanning the spectrum of solid-state capabilities. TI, for example, is building a combined analog-digital cell library using a linear-oriented 3- μ m CMOS technology. TI's LinASIC library now has 34 functions, and a bipolar module—called LinBiCMOS—is in the works for additional 20-V capabilities [*Electronics*, Sept. 17, 1987, p. 17].

Initially, TI is concentrating on using the library internally to speed up complex linear and custom designs. Several customers have begun using the LinASIC system for chips made in the linear-based CMOS process, which treats digital functions as a subset.

ANOTHER WAY. National is taking a different tack. It is enhancing standard analog functions for fabrication in 5-V digital CMOS technology. In the initial offering, National will include a number of products: three operational amplifiers with a bandwidth of 1 MHz, two comparators with response times of 150 ns, a 2.5-V voltage reference, an analog switch with 100 Ω of on-resistance, and a set of resistors for setting gain and voltage drivers.

More analog functions will be added around March, including a few medium-

complexity macrocells. In the first half of 1988, "we will begin to look at adding more complex telecom functions, expanding the general range of analog capabilities," says Mike Bereziuk, director of marketing for the ASIC Division. Bereziuk believes the growth of analog functions in digitally dominated design libraries represents a critical factor in shifting total semicustom-chip sales toward cell-based ASIC by the early 1990s.

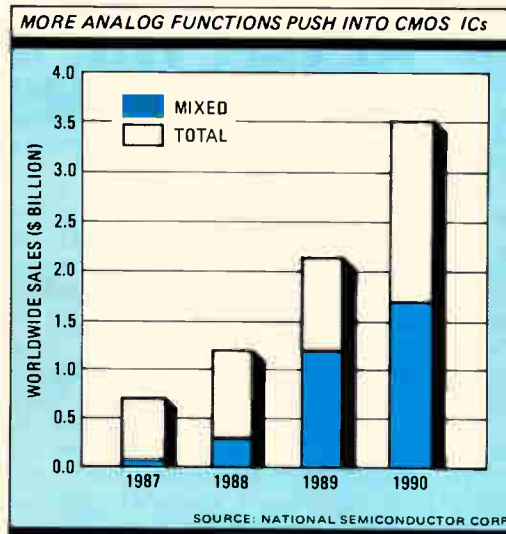
Meanwhile, the movement to mix analog and digital macrocells comes as no surprise to those who were early in the field. NCR Corp.'s Microelectronics Division started offering simple analog macros in its CMOS cell library five years ago. The decision was fueled by requests from consumer-electronics houses wanting to cut pennies from their designs, recalls Gene Patterson, director of the semicustom business unit in Fort Collins, Colo. "Most of our mixed designs are mostly digital, with maybe 5% to 10% analog," he says. He estimates that as much as 30% of the ASIC chips sold by NCR have on-board linear functions.

At Sierra Semiconductor Corp. in San Jose, Calif., which entered the business expressly to mix analog with digital, the trend gets a mixed reaction. While it lends credibility to Sierra's decision to stake out the territory, it also means that competition is going to pick up.

"I'm sorry to hear the big guys are finally catching on," says Mike Friedman, marketing manager. He thinks the key battleground for those who are mixing analog and digital on semicustom chips is the design-automation business, where Sierra offers a mixed simulator called MIXsim.

Sierra now has approximately 40 macro functions in its 2- μ m CMOS library. As is the case with NCR, many of the additions to the library are coming as a result of requests from customers. Sierra plans to boost its chip integration and performance with a process shrink to 1.5 μ m in 1988 and to 1 μ m in 1989, he adds.

—J. Robert Lineback



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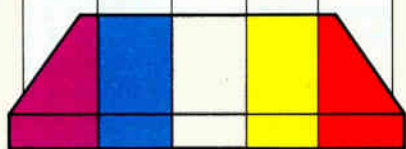
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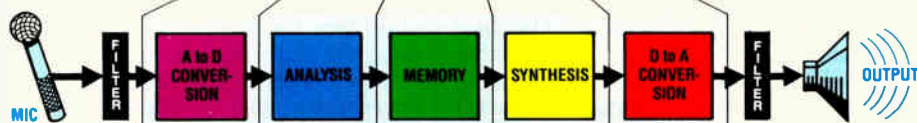
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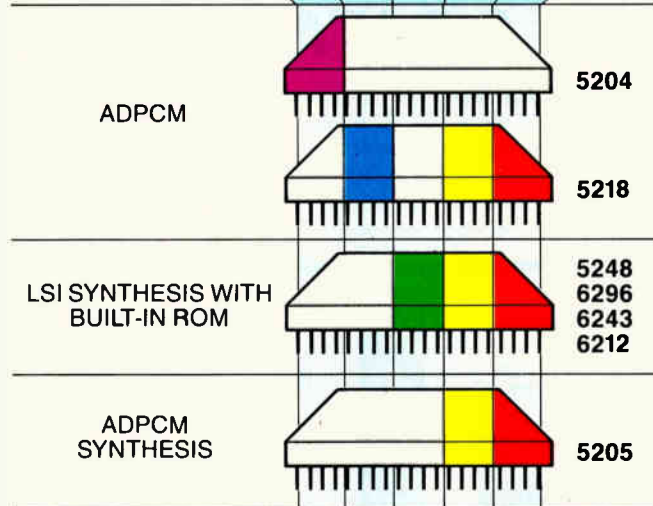


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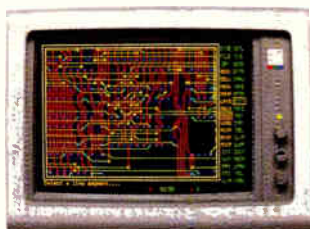
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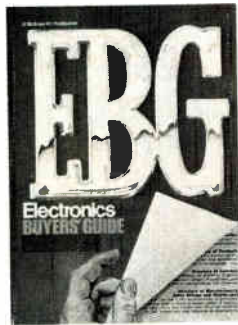
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already lined up several OEMs and has its first boards in beta sites. Nucleus will supply an entire development system for about \$10,000. McLeish says the cost of end products might be about \$3,200 per user. By contrast, Ashton-Tate's dBase sells for about \$700 and the SQL-based data-base management system from Oracle Corp. of Belmont, Calif., is priced at nearly \$1,300.

-Larry Waller

SOFTWARE

WHY AT&T AND SUN HOOKED UP

NEW YORK

Like a sheriff rounding up a posse, AT&T Co. is corraling some key Unix players to chase after a bigger share of the midrange computer market. In its second major announcement in six weeks, AT&T's struggling Data Systems Group said last week that it is joining forces with Sun Microsystems Inc. of Mountain View, Calif., to develop a unified version of its Unix System V and SunOS, Sun's derivative of Berkeley Unix 4.2 bsd. In September, AT&T announced a similar deal with Microsoft Corp., under which the two companies are merging all the features of Microsoft's Xenix operating system into AT&T's System V.

These moves seek to establish System V as the de facto Unix standard in a confusing marketplace abounding with different and incompatible versions of the operating system originated at AT&T. At the same time, AT&T hopes some of the marketing strength of users such as Sun will add muscle to its computer line. However, whether AT&T can get other key players to join in consolidating the Unix world will be the true test of that strategy.

But that is not much of a strategy, figures analyst Jocelyn Young of Future Computing Corp., a Dallas market researcher. "They realize they can't go it alone," she says of AT&T, "so they're trying to leverage some of the market presence of the other players in the Unix and Xenix market," and to establish Unix V as the standard.

BOTH GAIN. Drawing others in may not be easy, but in joining up, AT&T and Sun are hoping that together they can do what neither could do alone. While the deal gives AT&T a bigger role in consolidating the Unix environment, it offers Sun a key backer in its effort to make its Sparc (Scalable Processor Architecture) microprocessor an industry standard for reduced-instruction-set computing. AT&T Data Systems Group president Vittorio Cassoni says AT&T

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Electronics / October 29, 1987

will eventually use the Sparc architecture across its entire line of minicomputers, but the first system to use the chip is still at least two years off.

AT&T's push to expand System V to include features of other Unix versions comes along just as the Institute of Electrical and Electronics Engineers and X/Open—a consortium of European computer companies—are getting closer to defining their own standards. AT&T is not trying to upstage those efforts, says Michael DeFazio, director of software systems for the Data Systems Group. He says, however, that neither standardization effort goes far enough, and he promises that AT&T will incorporate within its expanded System V interface definition, called SVID, any features required by either new standard.

That should be simple, DeFazio says.

Sun gets a key backer in the drive to standardize its RISC chip

The IEEE Posix standard, which is now in draft form, "deals with one volume, one third of the SVID standard," he says. "About 75% or 80% of that is precisely SVID, and the rest is Berkeley extensions." The X/Open standard, which is still in the definition stages, will also be based on SVID.

The enhanced System V, which will be developed by AT&T, will be optimized for the Sparc computing platform, incorporating features from System V, Berkeley 4.2, and SunOS. Sun's Network File System, its variation of the X-Windows graphics interface, NeWS, will also be included.

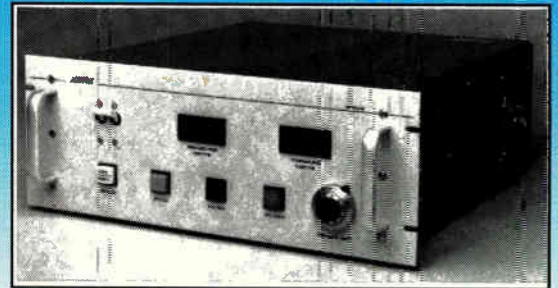
AT&T has struggled as a computer maker since it was allowed to enter the business after the breakup of the Bell System in 1984. The company had some early success with its high-end IBM-compatible personal computers, but more recently has lost money with both those products and its 3B line of mid-range machines. At the same time, it has drawn heavy criticism from analysts who complain that AT&T lacks a coherent strategy for computers.

These analysts give mixed reviews to the latest moves by AT&T, and not all of them are convinced that these moves are evidence of what group president Cassoni calls "a concerted effort to consolidate the Unix-system market." For example, Kenneth Bosomworth, president of International Resource Development Inc. of Norwalk, Conn., says that AT&T is merely "ringing doorbells." In his view, "Sun's answer indicates that they opened their door. It takes them [AT&T] nowhere; it's a mindless strategic alliance."
—Tobias Naegele

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| TOSHIBA MEMORY PRODUCT SUMMARY | | | | | | | | | |
|---|--------|---------|---------|-------|----------------------------|-----|-----|-----------------|-----------|
| PART NO. | ORG. | PROCESS | SAMPLES | PROD. | SPEED SORTS AVAILABLE (ns) | | | PACKAGE OPTIONS | |
| DYNAMIC RAMS | | | | | | | | | |
| TMM41256AP/AT/AZ | 256KX1 | NMOS | YES | YES | 100 | 120 | 150 | P,T,Z | |
| TMM41257AP/AT/AZ | 256KX1 | NMOS | YES | YES | 100 | 120 | 150 | P,T,Z | |
| TMM41464AP/AT/AZ | 64KX4 | NMOS | YES | YES | 100 | 120 | 150 | P,T,Z | |
| TC511000P/J/Z | 1MbX1 | CMOS | YES | YES | 85 | 100 | 120 | P,J,Z | |
| TC311001P/J/Z | 1MbX1 | CMOS | YES | YES | 85 | 100 | 120 | P,J,Z | |
| TC311002P/J/Z | 1MbX1 | CMOS | YES | YES | 85 | 100 | 120 | P,J,Z | |
| TC514256P/J/Z | 256KX4 | CMOS | YES | YES | 100 | 120 | | P,J,Z | |
| TC514258P/J/Z | 256KX4 | CMOS | YES | YES | 100 | 120 | | P,J,Z | |
| THM81000S | 1MbX8 | CMOS | YES | YES | 100 | 120 | | S | |
| STATIC RAMS | | | | | | | | | |
| TMM2016AP | 2KX8 | NMOS | NO | YES | 90 | 100 | 120 | 150 | P |
| TMM2016BP | 2KX8 | NMOS | YES | YES | 90 | 100 | 120 | 150 | P |
| TMM2015AP | 2KX8 | NMOS | NO | YES | 90 | 100 | 120 | 150 | P,300 MIL |
| TMM2015BP | 2KX8 | NMOS | YES | YES | 90 | 100 | 120 | 150 | P,300 MIL |
| TMM2064P | 8KX8 | NMOS | YES | YES | 70 | 100 | 120 | 150 | P |
| TMM2064AP | 8KX8 | NMOS | YES | YES | 70 | 100 | 120 | | P |
| TMM2063P | 8KX8 | NMOS | YES | YES | 100 | 120 | 150 | | P,300 MIL |
| TMM2063AP | 8KX8 | NMOS | YES | YES | 70 | 100 | 120 | | P,300 MIL |
| TC5516AP | 2KX8 | CMOS | YES | YES | 200 | 250 | | | PFY |
| TC5517/18CP | 2KX8 | CMOS | YES | YES | 150 | 200 | | | PFY |
| TC5565P | 8KX8 | *CMOS | YES | YES | 120 | 150 | | | PFY |
| TC5565AP | 8KX8 | *CMOS | YES | YES | 100 | 120 | 150 | | PFY |
| TC5564P | 8KX8 | CMOS | YES | YES | 150 | 200 | | | P,300 MIL |
| TC5564AP | 8KX8 | CMOS | YES | YES | 120 | 150 | | | PFY |
| TC5527P | 32KX8 | *CMOS | YES | YES | 85 | 100 | 120 | 150 | P |
| TC5527AP | 32KX8 | *CMOS | YES | YES | 85 | 100 | 120 | 150 | PF |
| HIGH SPEED STATIC RAMS | | | | | | | | | |
| TMM2018AD | 2KX8 | NMOS | YES | YES | 35 | 45 | 55 | | D |
| TMM2018AD | 2KX8 | NMOS | YES | YES | 25 | 35 | 45 | | D |
| TMM2068AD | 4KX4 | NMOS | YES | YES | 35 | 45 | 55 | | D |
| TMM2066AD | 4KX4 | NMOS | YES | YES | 25 | 35 | 45 | | D |
| TMM2078AD | 4KX4 | NMOS | YES | YES | 35 | 45 | 55 | | D |
| TMM2078AD | 4KX4 | NMOS | YES | YES | 25 | 35 | 45 | | D |
| TMM2088P | 8KX8 | NMOS | YES | YES | 35 | 45 | 45 | | P |
| TMM2089V | 8KX9 | NMOS | YES | YES | 35 | 45 | | | C,300 MIL |
| TC55416P | 16KX4 | *CMOS | YES | YES | 35 | 45 | | | D |
| TC55417P | 16KX4 | *CMOS | YES | YES | 35 | 45 | | | D |
| TC5561P | 64KX1 | *CMOS | YES | YES | 70 | | | | P |
| TC5562P | 64KX1 | *CMOS | YES | YES | 45 | 55 | | | PFY |
| TC51832P | 32KX8 | PSEUDO | YES | YES | 120 | 150 | | | P |
| EPROMS | | | | | | | | | |
| TMM2764AD~ | 8KX8 | NMOS | YES | YES | 150 | 200 | | | D |
| TMM2764AD~ | 8KX8 | NMOS | YES | YES | 150 | 200 | | | D |
| TMM27128AD~ | 16KX8 | NMOS | YES | YES | 150 | 200 | | | D |
| TMM27128AD~ | 16KX8 | NMOS | YES | YES | 150 | 200 | | | D |
| TMM27256AD~ | 32KX8 | NMOS | YES | YES | 150 | 200 | | | D |
| TMM27256AD~ | 32KX8 | NMOS | YES | YES | 150 | 200 | | | D |
| TC57256D | 32KX8 | CMOS | YES | YES | 200 | 250 | | | D |
| TC57256AD | 32KX8 | CMOS | YES | YES | 150 | 200 | | | D |
| TMM27512D~ | 64KX8 | NMOS | YES | YES | 200 | 250 | | | D |
| TMM27512D~ | 64KX8 | NMOS | YES | YES | 200 | 250 | | | D |
| TC571000D | 128KX8 | CMOS | YES | YES | 200 | 250 | | | D |
| TC571001D | 128KX8 | CMOS | YES | YES | 200 | 250 | | | D |
| TC571024D | 64KX16 | CMOS | YES | YES | 200 | 250 | | | D |
| ONE TIME PROGRAMMABLES | | | | | | | | | |
| TMM2464AP | 8KX8 | NMOS | YES | YES | 200 | | | | PF |
| TMM24128AP | 16KX8 | NMOS | YES | YES | 200 | | | | PF |
| TMM24256AP | 32KX8 | NMOS | YES | YES | 200 | | | | PF |
| TC54256AP | 32KX8 | CMOS | YES | YES | 200 | | | | PF |
| TMM24512P | 64KX8 | NMOS | YES | YES | 250 | | | | PF |
| MASK ROMS | | | | | | | | | |
| TMM2256P | 32KX8 | NMOS | YES | YES | 150 | | | | P28 |
| TC53257P | 32KX8 | CMOS | YES | YES | 200 | | | | FP28 |
| TC5312P | 64KX8 | CMOS | YES | YES | 200 | | | | P28 |
| TC531000P | 128KX8 | CMOS | YES | YES | 200 | | | | P28 |
| TC53200P | 256KX8 | CMOS | YES | YES | 200 | | | | P28 |
| P = PLASTIC C = CERAMIC F = FLAT PACK D = CERDIP Y = DIE T = PLCC J = SOJ Z = ZIP *CMOS = 4 TRANSISTOR CELL LOW POWER ~ = ± 10% Vcc AVAILABLE S = SOCKET MODULE | | | | | | | | | |

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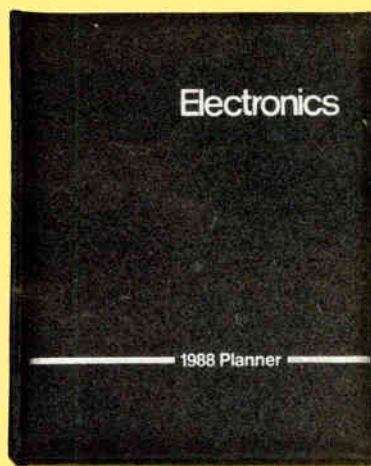
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INTERNATIONAL WEEK

HIGH-CAPACITY LIGHT LINK SET IN JAPAN

Starting next month, NEC Corp. of Tokyo will begin supplying the world's highest-capacity optical-communications system to Nippon Telegraph and Telephone Corp., also of Tokyo. The backbone system will have a capacity of 1.544 gigabits/s, four times the capacity of the current 400-Mbits/s systems installed in Japan. It will link Tokyo and Osaka, and it is scheduled for completion by March 1988.

SAMSUNG, TOSHIBA REACH VCR ACCORD

Samsung Electronics Co., Seoul, will build hi-fi VHS video-cassette recorders using technology from Toshiba Corp., Tokyo. Toshiba says the two firms will sign a formal contract before year's end, and that the pact will be its first technology-transfer agreement in VCR production. Samsung, which now produces about 250,000 VCRs a month, will start manufacturing the hi-fi VCRs next year. Samsung is also negotiating a contract to produce Toshiba-brand hi-fi VCRs for the Japanese company.

EQUIPMENT BUDGET FOR NTT GOES UP

Nippon Telegraph & Telephone Corp. says that during the fiscal year ending in March 1988 it will increase purchases for computer systems to 98.4 billion yen, up from 80.5 billion yen last fiscal year. Without specifying its budget allowances, NTT says it will also purchase other high-tech equipment, including local cable, single-mode optical-fiber cable, digital equipment, single-line telephone sets, desktop coin-operated public telephones, and mobile radio communications equipment. There's an opportunity there for foreign suppliers: last fiscal year, NTT funneled 9% of the 400

billion yen it spent on high-tech equipment to foreign suppliers, mostly in the U.S.

TELECOM FIRMS PAIR UP FOR ISDN

Northern Telecom Ltd. has signed an agreement to purchase for £445 million ITT Corp.'s 24% holding in STC plc, a major British supplier of communications and information systems. STC, in turn, would acquire a 40% interest in the Canadian telecommunications company's British subsidiary. If the purchase of the STC shares is approved by the UK government, the two transactions would enable the companies to jointly develop components for the Integrated Services Digital Network.

EDS TO BUILD SYSTEM FOR ASIAN GAMES

A joint U.S.-Chinese venture will design and develop a \$10 million computerized data-management system for the 1990 Asian games in Beijing. The integrated system will be produced by Beijing International Information Processing Co., a joint venture between Electronic Data Systems, of Dallas, and a mainland Chinese group, the Beijing municipal government's Commission for Science and Technology. It will provide the hardware, software, and communications components to cover the 26 major and 240 minor sporting events, coordinating competition results and providing electronic mail, computer-aided sports analyses, and monitoring and control. The system will be installed in the Chinese capital in 1989.

NIXDORF TAKES POS LEAD IN AUSTRALIA

West Germany's Nixdorf Computer AG has become the leading point-of-sale systems supplier to Australia thanks to a Sydney department store. The Paderborn-

based Nixdorf nabbed an order from Grace Brothers to deliver some 2,000 computerized cash registers to the department store chain, one of the continent's largest. Nixdorf will be supplying its 8812 system; a Nixdorf 8862 computer at each store will collect the data coming from the cash registers and send it to the chain's computer center in Melbourne.

AEG TO SELL SOLAR PACK TO POWER TV

Will people carry their TV sets to the beaches as they now do their radios? That prospect is closer to reality now that West Germany's AEG AG has come out with a solar-power plant the size of a briefcase, which powers color-TV sets made by Grundig AG, also of West Germany. The Solar Power Pack consists of a solar generator fitted with solar cells delivering a total of 40 W. A solar-charged battery ensures TV reception up to four hours under no-daylight conditions.

SOVIET ORDER FOR IBM 9370 BANNED

Overruling approval by the U.S. Commerce Department, the Defense Department has forbidden IBM Singapore from selling a \$250,000 Model 9370 minicomputer to the Singapore Soviet Shipping Co., or Sinsov. Singapore's United Industrial Corp. owns 50% of Sinsov and the Soviet Union the other 50%—a situation that raised Pentagon concerns that the computer might be put to military uses. "Our viewpoint is that Sinsov is owned by the Soviets, and the bottom line is that this line of computers is not for sale to certain countries," says Col. Arnold Williams, U.S. Defense Department spokesman. Sinsov says it wants a computer to process documentation and accounting work for the more than 1,000 Soviet vessels that call yearly at Singapore's harbor,

the world's busiest. Instead of the 9370, it will buy a less powerful \$125,000 IBM System 36 from a local dealer.

THORN TO SUPPLY AIR DEFENSE AID

Thorn EMI Electro Optics Division of Hayes, England, has won a £70 million contract from the UK Ministry of Defence to supply an Air Defence Alerting Device, which is portable or can be mounted on a vehicle. The device warns ground forces of the presence of low-flying aircraft and helicopters by sensing the infrared emissions of intruding aircraft, then gives their bearing to a weapons operator. It remains undetected itself.

SHARP USES SONY'S 2-IN. DISK DRIVE

Sony Corp.'s 2-in. floppy-disk drive [*Electronics*, Sept. 17, 1987, p. 54E] has found a home in another company's product. Sharp Corp., Tokyo, started marketing a portable Japanese and English word processor that incorporates the drive on Oct. 21. The new word processor, which is equipped with a thermal-transfer printer with a resolution of 24 by 24 dots per character, can also process punctuation and characters for German, French, and Spanish, and incorporates a spelling checker for English-language processing. Sharp expects to sell about 10,000 units a month at 85,000 yen in Japan.

SIEMENS PCs ARE #2 IN GERMANY

West Germany's Siemens AG sold more than 21,000 MS-DOS-based personal computers for professional applications during the last fiscal year, which ended Sept. 30. Combined with its sales of Unix-based machines, those sales push the Munich company to No. 2 in its home market, behind IBM Corp.

INTERNATIONAL PRODUCTS

THYRISTORS OPEN NEW VISTAS BY HANDLING 20-KHz SWITCHING

THOMSON'S ZERO-TURN-OFF DEVICES ALSO USE 20% LESS POWER

A new world of high-power, high-frequency applications in power conversion will open up to thyristors now that Thomson Semiconducteurs is pushing maximum switching frequency from 2 KHz up to 20 KHz in its new ZTO devices that can handle up to 1 MW. ZTOs—the name stands for Zero Turn-Off time—also deliver 20% cost savings over gate-turn-off, or GTO, thyristors, so a wide range of users will benefit from reductions in weight, volume, and cost, says the French chip maker.

Thomson foresees initial applications for ZTOs in resonant converters for induction heating. Future applications include traction, motor-drive, and uninterruptible

power supplies. ZTOs will also replace tubes and improve the power range and performance of generators in X-ray, radar, and laser power supplies, says Jean Pierre Abgrall, marketing manager for power devices.

LOW COST. "The cost limitation in all high-power equipment is more the transformers and other passive components, rather than the semiconductors," says Abgrall. "If you today replaced a GTO with a ZTO, your cost for the same amount of output power will be 20% less because you can take more current from the same silicon chip and you will save on passive components."

Until now, high-performance motor-drive techniques with high switching frequencies (10 to 20 KHz) were limited to about 10 to 20 KW because there were no semiconductors capable of handling both high frequency and high power. The turn-off capability of GTOs now being used for applications such as variable motor drives has enabled designers to eliminate commutation networks required by regular thyristors, but GTOs can handle only a limited current during gate switch-off. The GTO also has a dead-time turning switch-off when the device cannot be switched again, and as a result can handle operating frequencies only up to 2 KHz.

To solve these problems, Thomson used a technology based on high interdi-



PAIRS. The ZT340s, front, handle peaks of 500 A at 5 KHz and 400 A at 20 KHz, while ZT570s handle 700 A and 900 A.

gitation of gate-cathode junctions. The gate cathode is divided in a great number of cells to accelerate charge extraction at turn-off. To turn off a ZTO, anode current is first forced to zero by a small commutation circuit. Then a negative gate voltage is applied in order to extract stored charge and restore the device's blocking capability almost instantaneously—1 μ s or less. In this configuration, no focusing current occurs, which keeps power dissipation low.

The power of the gate drive at turn-off is much smaller than for a GTO because charge extraction from the gate can be implemented with a capacitor of a few microfarads. In a chopper configuration of 1,000 A and 1,000 V, for example, where a conventional fast switching thyristor is used, the extinction capacitor will be 40 μ F, and switching frequency will usually be a maximum of a few kilohertz. If a GTO is used, the snubber capacitor requirement drops to 3 μ F, but there will be no improvement on frequency. If a ZTO is used, the snubber capacitor will be only 1 μ F, and frequency will be limited only by the thermal dissipation capacity of the device, with switching frequencies higher than 20 KHz.

For the moment, Thomson is the only company making the device, but it expects others to begin scrambling to come out with similar products. The world market for high-power components—over 100

A—is around \$300 million, with a growth rate of about 5%, says Abgrall. "With these new applications we can expect the market to grow very fast—perhaps 15% for these particular components," he says.

One of the first applications for Thomson's ZTO will be for dc-dc converters aboard the next generation of France's high-speed trains, known as TGVs, for Trains a Grande Vitesse. The present TGVs use regular thyristors and have battery chargers weighing 500 kg. The new ones will use ZTOs and have battery chargers weighing 150 kg.

Until now, high-performance motor drive techniques with high switching frequencies (10 to 20 KHz) were limited to approximately 10 to 20 KW because there were no adequate semiconductors for higher power.

Production will start in Tours in October. Two series of products are now available for sampling, both with blocking voltages up to 1,600 V. The ZT340 series handles currents up to 500 A, and the ZT570 handles up to 900 A. Export prices range from about \$200 to \$300, respectively, in lots of 1,000.

—Jennifer Schenker

Thomson Semiconducteurs, 43 Ave. de L'Europe, 78140, Vélizy-Villacoublay, France.

Phone: 33-39-46-9719 [Circle 500]

IC PERFORMS AT 0.25 MICROSECONDS

Mitsubishi Electric Corp.'s 7700 series of 16-bit microprocessors use 1.3- μ m CMOS technology to achieve instruction-execution times as low as 0.25 μ s.

Four models make up the series. The M37700M2FP offer a 0.5- μ s execution time and the M37700M2AFP boasts an execution time of 0.25 μ s. Both offer 16 Kbytes of read-only memory.

The other two processor chips—the M377002SFP and M37700M2SAFP—offers 0.5- and 0.25- μ s execution times respectively. They do not, however, have on-chip ROM.

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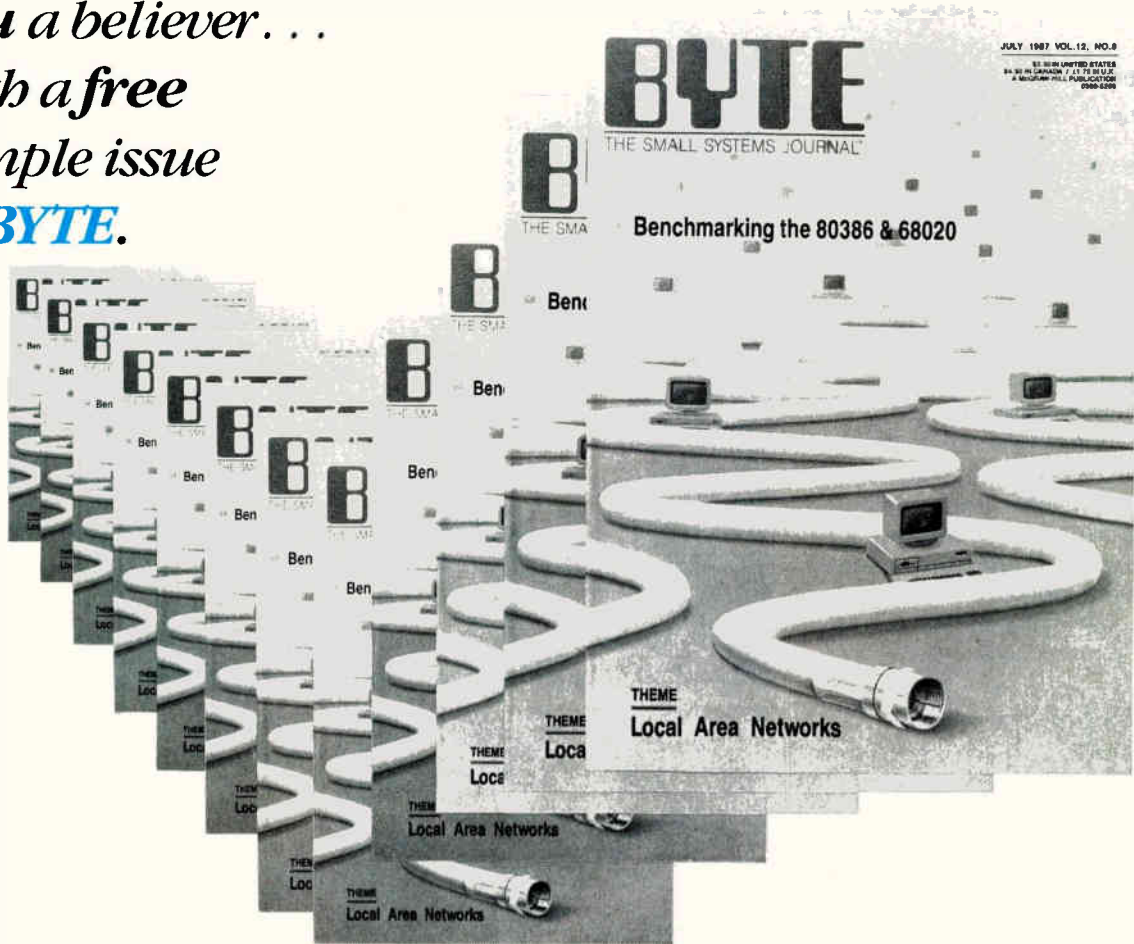
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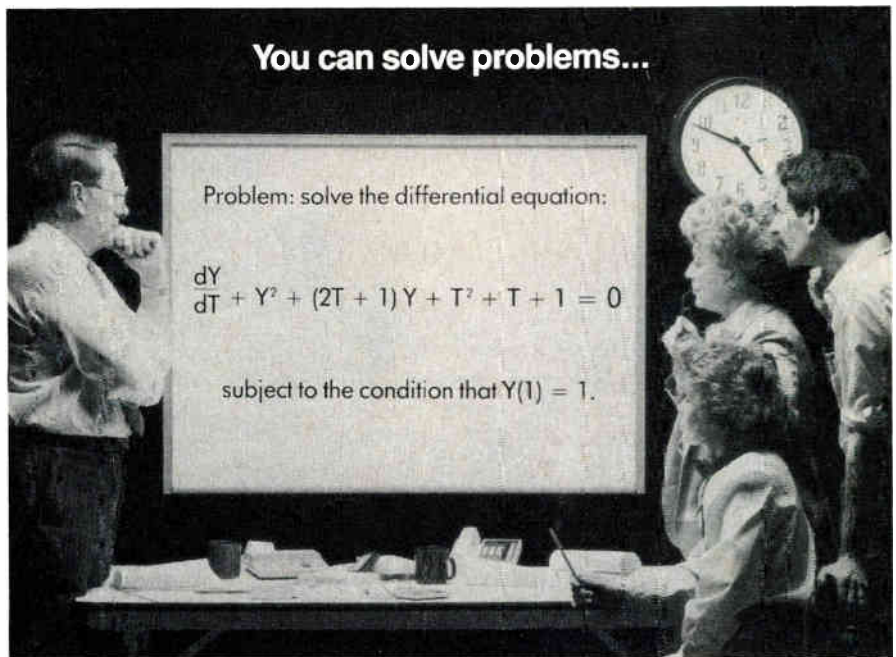
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```
(C1) DEPENDS(Y,T)$
(C2) DIFF(Y,T)+Y^2+(2*T+1)*Y+T^2+T+1;
(D2) dY/dT + Y^2 + (2T + 1)Y + T^2 + T + 1
(C3) SOLN:ODE(D2,Y,T);
(D3) Y = - %C T %E^T - T - 1
          %C %E^T - 1
(C4) SOLVE(SUBST([Y = 1, T = 1],D3),%C),NUMER;
(D4) [%C = 0.5518192]
(C5) SPECIFIC.SOLN:SUBST(D4,SOLN);
(D5) Y = - 0.5518192 T %E^T - T - 1
          0.5518192 %E^T - 1
```

and Numerically.

```
(C6) FORTRAN(D5)$
      Y = -(0.5518192*T*EXP(T) - T - 1)
      1 / (0.5518192*EXP(T) - 1)
```

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Circle 54 on reader service card

World Radio History

HOW THOMSON AIMS TO BUILD A WORLD-CLASS TV BUSINESS

BUT THE JAPANESE COULD UPSET THOSE PLANS WITH HDTV

by Jennifer Schenker

PARIS

Thomson SA is staking its future on a massive effort to build a world-class consumer-electronics business. On top of a spate of purchases that culminated this summer in the acquisition of General Electric Co.'s consumer electronics operations, the French government-owned company has now decided to invest \$3.28 billion over the next 10 years to build up this business. That investment should help Thomson to compete as a world player, but it will by no means guarantee success.

Thanks to its acquisitions, consumer operations already account for most of Thomson's sales (see chart). The company, in fact, is now the world's leading seller of TV sets. But this leadership in TV could disappear almost as fast as it was acquired. The French company faces formidable competition from Japan's TV makers, who are now pushing hard to establish themselves in the next generation of television technology, high-definition TV.

If the Japanese are successful in this drive, it could spell disaster for Thomson's well-laid plans. The Japanese version of HDTV is incompatible both with the TV sets Thomson now makes and with the HDTV technology that it is pursuing (see p. 58). Company president Alain Gomez is well aware of the problem. He sees the Japanese as capable of doing in TV what they've already done in video-cassette recorders: Far Eastern manufacturers now supply 90% of all VCRs sold in the world. Gomez says outright that if that happens in color TV, the heart of Thomson's consumer business, the company could be wiped out completely.

To fight off the Japanese, industry observers believe that Thomson must devote a significant amount of its resources in the next few years to research and development. Focused R&D, they say, should be able to keep the company from being locked out of the emerging HDTV market and help it establish a position in other markets.

At the same time, however, Thomson has to learn the consumer business and consolidate its acquisitions fast. A year ago, most of its sales and expertise were in the defense electronics market-

place. The Japanese, on the other hand, are masters of the worldwide consumer electronics business and will put on a full court press to gain market share. Thomson's consumer operations currently are just a collection of laboratories, plants, and offices scattered around the world, run until recently by a bunch of separate companies. Thomson needs to meld them into a smoothly running global operation.

"Thomson got where it is entirely through acquisitions. They don't have a single identity," says Jim Bottoms, a London-based analyst for Business Intelligent Systems Mackintosh, an international consulting firm. "Everybody knows Sony and Toshiba, and to a slightly lesser extent Philips, but Thomson is unknown by its own name in Britain and the U.S. It is going to have to start moving towards a world identity."

Doing that won't be easy. Thomson started buying other companies in 1974, acquiring GE's consumer electronics operations in Spain. Between 1978 and 1983, it bought four West German companies: the TV makers Normende, Saba, and Telefunken, and an audio firm, Dual. Then, in July, Thomson made its largest acquisition, buying the consumer-electronics division of GE in the U.S., including what had been RCA's consumer operations. Along with the acquisition of that same month of Ferguson in the UK, the deal made Thomson No. 1 in world television sales [*Electronics*, Aug.

6, 1987, p. 32]. The GE/RCA acquisition gave Thomson factories in the U.S. and the Far East, and the biggest marketing and manufacturing facilities on three continents. GE/RCA's color-TV market shares are 24% in the U.S. and 18% in Europe, according to BIS Mackintosh.

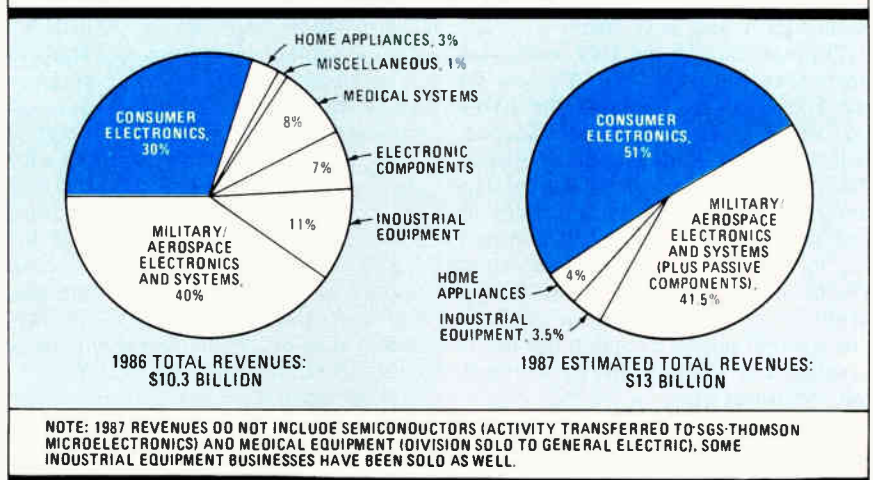
Thomson now projects its total 1987 sales as being \$13 billion. Some \$7 billion, or 55%, will come from the consumer electronics division, which includes home appliances like microwaves. Last year, the company's total sales were \$10.3 billion, and consumer products, including home appliances, accounted for only 33%. Some 40% of sales were in the military/aerospace sector. Components, medical equipment, and industrial products added another 27%.

In 1986, Thomson, GE/RCA, and Ferguson sold \$6.3 billion worth of consumer electronics, according to Bottoms of BIS Mackintosh, most of it based on TV equipment. Of the combined total, TV sets represented 61%, VCRs 30%, cathode-ray tubes 3%, and audio and TV components other than CRTs about 6%.

To compete with the Japanese, says Thomson president Gomez, the company will have to concentrate its investment dollars on TV sets, as well as CRTs, VCRs, and audio equipment. For now, the emphasis is on HDTV.

As proposed by the Japanese, HDTV would require new sets, new broadcast equipment, and new channel allocations. The Japanese are ahead of Europe and

THOMSON BETS HEAVILY ON CONSUMER ELECTRONICS



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plotters from Gerber Scientific, Hartford, Conn., that has become a de facto standard). However, the format contains only the data needed to plot a board layout, so much design data is not present. The work station will also accept files in the National Bureau of Standards IGES (Initial Graphics Exchange Specification) format.

With ECAM's board-editing features, users work on screen to alter a board's physical characteristics—for example, the width of traces. Or, to speed the entry of text—part number, component nomenclature, and so on—the system provides a variable field that prompts the user to provide such information. As he enters these variables, the system automatically places the information at the appropriate location on the board design. On other systems, the engineer must create the text, determine where on the board it should go, and indicate the location to the system.

The ECAM system also removes unused pads. This capability is useful with edge connectors, for example, which have active areas only on the top and bottom layers. Yet every layer contains the connector in its artwork. "The engineer building the board wants to eliminate any unnecessary copper to free up space between active elements," says Zizzi. "By spreading elements apart using the freed space, there is less likelihood of shorts, and the board is more manufacturable."

It is easy for the ECAM work station to find unused pads since it can examine the design data to see which pads are connected to an electrical signal, power, or ground. On many other CAM work stations, there is no such facility and the engineer ends up scraping the pads off the final phototool.

An ECAM user can enlarge or reduce all pads and traces at once or concentrate on individual pads and traces. To free up space on the board, he can squeeze tracks together or spread them apart. He can also add elements to the board. For example, he may want to add a "dead via," a hole drilled through the board with no connection. "Such elements are added to a board for mechanical reasons to improve cooling or to ease structural stress," says Zizzi.

An important part of editing is adding test circuits—called test coupons—at a number of dispersed locations around the printed-circuit patterns. "During manufacturing, pads and traces are added to test coupons on every layer," Zizzi explains. These coupons are removed from the final fabricated panel and tested to see if the laminations hold up under all extreme operating conditions, to determine how well the copper adheres to the fiberglass, to determine the thickness of the copper traces and pads, and to ensure all specifications. "In all, around 150 tests are performed on a test coupon," Zizzi says.

The manufacturing engineer also must add border features (see fig. 3) to the panel. These features, or patterns, are added around the perimeter of each printed-circuit layer on the form in order

to facilitate plating and laminating. Adding the border features takes time on other CAM work stations because the systems lack ECAM's graphics-processing capability to automate the task.

Two border features that must be added to every board layer are venting dots, small spacers between layers that allow the venting of any trapped air, and plating bars added around the layers of a board to facilitate more even distribution of the copper or silver-nickel plating material.

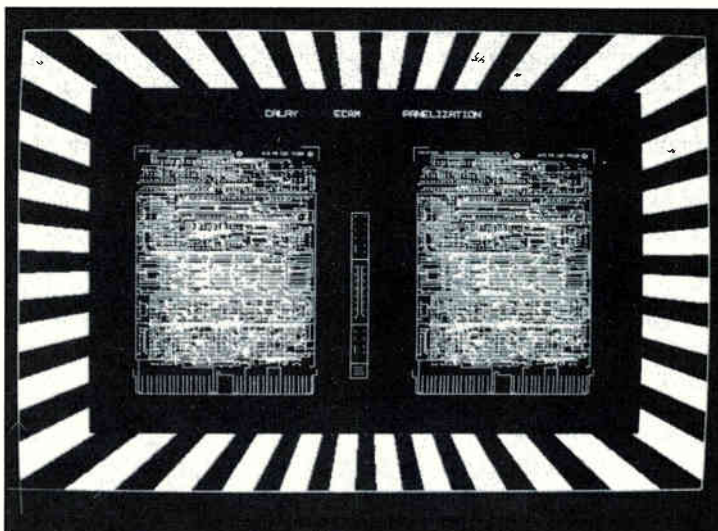
The panelization task, which creates a special file to drive the photoplotter, is only the first step

ECAM can quickly translate design data; so if one n/c drill on a production line goes down, it takes only a few keystrokes to create a driver for another machine

with ECAM. The Calay work station also comes with postprocessors for other machines used in board manufacturing. One, the fabricator postprocessor, contains the drill-tape formatter and profile/router formatter. It also has a design-rule checker which ensures that the correct spacing width exists between traces, that pads are of the correct size, and so on. In the second release of ECAM tools, the fabricator postprocessor will produce files for bare-board testers.

The ECAM system provides "neutral" data-base conversion, that is, it can quickly convert design data into equipment-specific file formats. For example, a manufacturing engineer might create a file for an n/c drill machine that breaks down halfway through a run. With a few keystrokes, he can create a new file for an entirely different machine and resume the production run. On other systems, he would have had to manually change the file over to the new n/c machine. □

For more information, circle 480 on the reader service card.



3. FULL HOUSE. This ECAM-produced phototool builds two copies of one pc-board layer, separated by a test circuit and surrounded by plating bars.

NOW, WILL CAM FINALLY CATCH ON?

Producing printed-circuit boards has always been a tedious, time-consuming task. The advent of laser phototools in the late 1970s, followed by computer-aided-design work stations, began to change all that, and since then the goal has been to automate as much of the job as possible, if not all of it. That goal—full automation—is getting much closer as new work stations for computer-aided manufacturing are beginning to hook up with CAD stations on the front end and laser phototools on the back end. Within a short period, manufacturing pc boards may be a totally hands-off enterprise.

Now valued at \$100 million, the CAM work station market should grow faster than 40% over the next five years. Whereas first-generation CAM work stations concentrated on improving the panelization task, which involves only the laser photoplotter, the current crop is providing data to run ever more production equipment. And the latest CAM work stations are acquiring design data from various CAD data bases despite strong objections from designers who are reluctant to give production engineers the ability to change board designs.

The symbiosis of work station and photoplotter is the catalyst for automating the entire manufacturing process for printed-circuit boards. John Salzer, president of Salzer Technology Enterprises Inc. a market research firm based in Santa Monica, Calif., estimates that the worldwide installed base of laser photoplotters alone will triple, to almost 500 units, by 1991. "One source of sales for laser photoplotters is the installed base of 2,500 conventional photoplotters," says Salzer. These are typically in a board design lab where a designer produces a single-copy film of each board layer, which he provides to the manufacturer of the board. Moreover, each photoplotter sale should generate a demand for more than one work station. A laser photoplotter can cost as much as \$500,000, but it can serve more than one work station, which typically costs less than \$100,000. So it makes economic sense for a photoplotter purchaser to buy several work stations to keep the plotter busy.

Jeffrey Rittichier, product marketing manager for electronic systems at Gerber Scientific Inc. of South Windsor, Conn., estimates that there are between 600 and 700 sites worldwide that could use laser phototools, which represents a total available market of around \$300 million. In

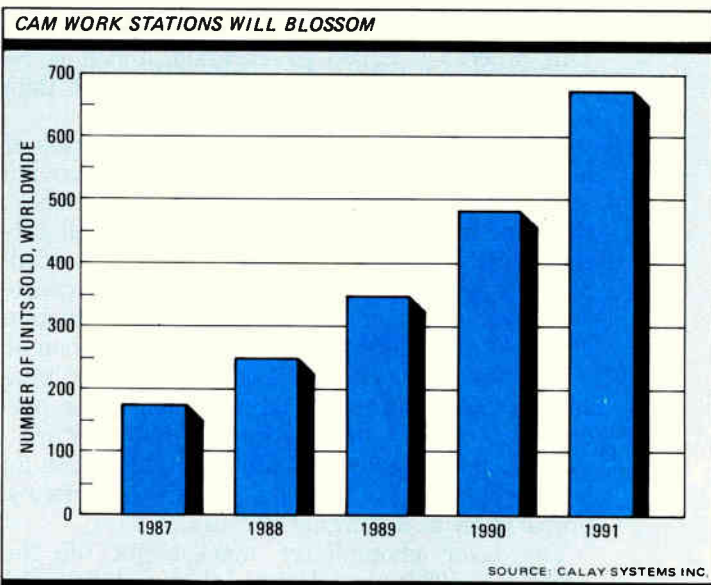
Automation of pc-board production gets closer as CAM stations link up with CAD stations and phototools; but designers slow process by objecting to CAD data going to factory floor

by Jonah McLeod

addition, Steven Zizzi, ECAM product manager at Calay Systems Inc., Irvine, Calif., says that by 1991, sales of CAM work stations could hit 675 units, worldwide (see graph).

Conventional plotters make sense in the design lab because the volume of film (the photoplotter "masks") is relatively low. But "laser photoplotters make much more economic sense on the manufacturing side of the house where many more board designs [pieces of film] are handled," Zizzi explains. Potential customers for laser photoplotters and CAM work stations divide into two categories: captive and merchant pc-board production shops. "Noncaptive shops produce 57% of the pc-board dollar volume, but they represent 72% of all the shops making boards," Zizzi asserts. "The average size of a noncaptive manufacturer is about \$3 million in annual sales, compared with about \$6 million for captive board makers."

In the U. S., there are 930 board manufactur-



ample, the program will instruct the n/c tool to drill adjacent holes rather than have the tool move back and forth across the board surface, drilling holes randomly.

CAM work-station suppliers are working to provide a more complete set of translators. Calay, for example, boasts 31 different translators for various production equipment. At Cadnetix, "we recognize that there is a lot of custom equipment in the manufacturing area," notes Jim LeBrun, product marketing manager. "So we have added an English-like data query language, which allows a foreign piece of equipment to access every piece of data in the Cadnetix work station's data base."

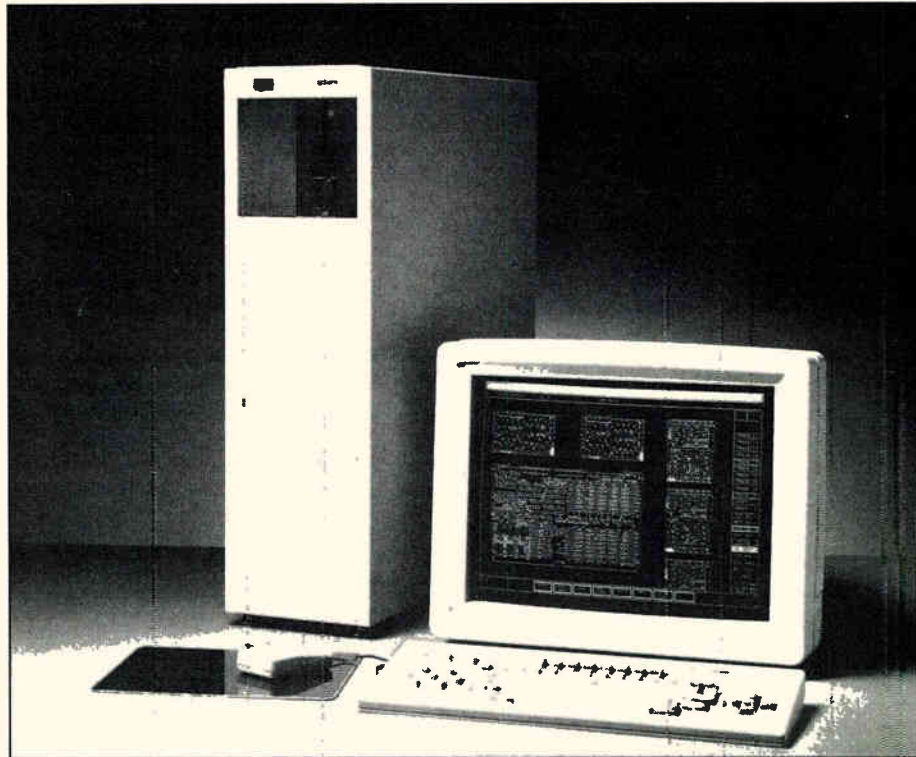
Harvel at Royal Digital Systems agrees that providing open access to CAM data is essential if the production floor is to achieve true computer-integrated manufacturing. "Our work-station data base is available and can be easily configured for any existing or new piece of production equipment," he claims. And computers, as well as automated production equipment, can access the CAM work-station data base. LeBrun cites the instance of a computer wanting information on the manufacturing process. "The Cadnetix system collects data on the number of drill holes in a board and the distribution of the hole sizes," he explains. "In a CIM environment, the central computer could digest that information to determine when to change drill bits in the n/c drill equipment."

The last obstacles to full automation—lack of standards for moving CAD data into CAM work stations—are being hurdled. "Data-base translators alone are not enough," says Harvel. "The problem with moving CAD data into the CAM environment is that designers are resisting releasing the CAD data base to manufacturing," Calay's Zizzi explains. "They do not want manufacturing [engineers] changing board layouts." Designers have relinquished the Gerber file, the familiar format that drives a photoplotter, because it contains only graphical information on locations of pads and routes for every layer. "There are over a couple hundred Gerber formats, but the one running on the older Gerber Vector Plotters is the one cited when everyone refers to Gerber file format today," says Gerber's Rittichier. An Electronic Industry Association RS274D specification standardizes this file format.

IGI's Stritch says that, over the long term, companies building their own pc boards will eventually provide design data to manufacturing in order to remain competitive. "One of the most

compelling reasons for doing so is to improve quality and reduce cost," he explains. He cites the example of automatic optical inspection, which compares a known-good board layer with layers that have just been fabricated. "If the standard is bad, it can easily cost a manufacturer \$50,000 before the error is caught in final board test," he says. The mistake could be avoided easily by comparing the layers that have just been manufactured against an electronic image of the layer, derived from the CAD data base.

Such costly errors are the reason that companies building boards on government contract and



2. FABRICATOR. The CDX-6000 gives fabrication gear CAD data it can use.

major captive-board manufacturers are moving CAD data to manufacturing. With government contracts, the data is likely to arrive in IPC-350 format, a Department of Defense standard. Captive-board makers likely will provide data in the Calma GDS II Streams format or in a CAD-system-specific format—such as the Cadnetix or Calay data-base format.

In the future, once the Electronic Design Interchange Format (EDIF) becomes a standard, it will be universal. "Until that time, we will be developing software tools that will allow production engineers to reverse-engineer CAD data from the Gerber file information," Stritch declares. Such products will be forthcoming in the first part of next year. "Another alternative to having the complete CAD data base is to combine the Gerber data file with a netlist of the design," LeBrun of Cadnetix offers. Data in the netlist is essential if the CAM work station is to provide a file to a board-stuffing machine. □

dibs on the hardware resources of the machine. "The first and foremost design goal was to have Pick and Unix run as co-residents in the supervisor space of the 68000 memory," says Gary Eple, Edge's director of software engineering. "And while it is running, either operating system would have [at its disposal] the full native performance of the machine."

In the overall structure of Symetrix (see fig. 1), the Unix kernel and the Pick monitor sit atop the commonly shared I/O service layer, which contains peripherals drivers. At the top level, users have access to both Unix and Pick applications through the menu-oriented shell, the common user interface. The applications can have standard interfaces to their respective operating systems and need not be altered to run under Symetrix.

The ability to execute two operating systems side by side comes from a software module called the Hypervisor. As a Symetrix system comes up, the Hypervisor first brings Unix up in the supervisor memory space. Then Unix carves out a part of the supervisor space for the Pick operating system and then loads it.

Since the operating systems co-reside, the Hypervisor performs the complete context switching required for both to share the central processing unit. To switch contexts, the Hypervisor saves the contents of all registers and loads up the values for the other operating-system context. The context-switch code is only about 100 instructions—it takes about 10 μ s to execute on the Edge 1000.

The shortest time that the Hypervisor can let one of the operating systems run is 4 ms. Two things determine when a switch is made. First, system administrators can set the number of 4-ms ticks for each operating system, depending on the mix of jobs and users. Secondly, a continuous dynamic balancing takes place automatically. When either operating system goes idle—all jobs are finished before the allotted time slice is over—Hypervisor switches to the other operating system. That way, no time is lost in running the two operating systems concurrently. The computer operates just as it would under one system.

The Hypervisor provides no direct communication between operating systems. But since the systems and the applications share the same machine—CPU, main memory, file system, and I/O subsystems—it makes sense for programs to also share data, and for processes in

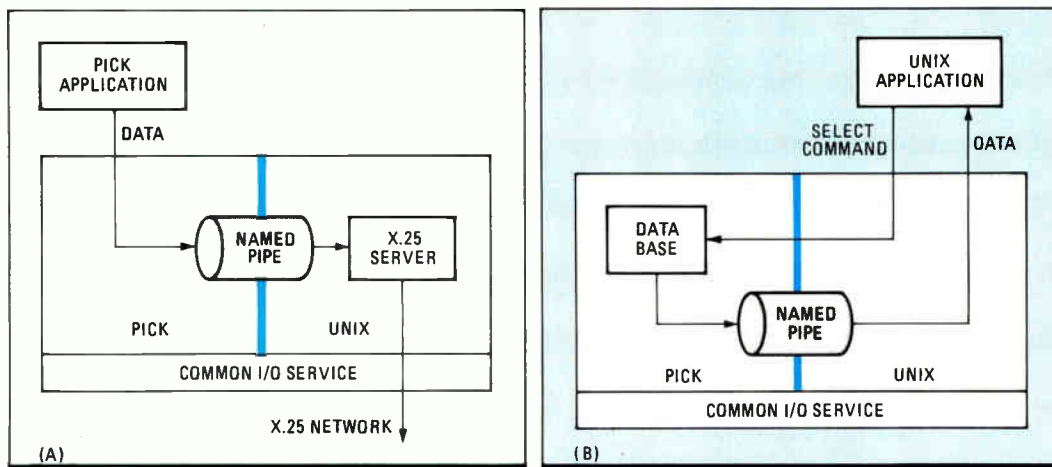
one operating environment to be able to communicate with processes in the other. The engineers used a basic file-sharing mechanism in version 1.0 of Symetrix and are creating much tighter coupling and interprocess communication facilities in version 2.0. This tool gives each operating system a set of jump tables, located on its side of the supervisor space, to use in requesting file and I/O services. In version 1.0, the basic level of file sharing uses these jump tables plus special processes running under each operating system.

For example, when a Pick program wants to access data from a Unix file, it passes a Unix Open command to a so-called Unix daemon, a process waiting on the Unix side for Pick requests. The daemon then performs the Unix file access. Similarly, a process running on the Pick side and called a Pick phantom can access Pick functions when it gets a request from Unix.

The common I/O service layer is implemented with Unix device drivers, so the Pick side transparently gets the benefits of the varied features of the Unix drivers. Standard Pick I/O calls are issued by the programs, but the real Pick I/O drivers have been replaced by virtual device drivers that intercept the calls, reinterpret them as Unix calls, and send them to the I/O service.

Toltec is also incorporating in the common I/O service layer some Unix transaction-processing extensions that it purchased from the now defunct EnMasse Computer Corp. Among them are a fault-tolerant file system using mirrored disks, enhanced terminal handling for large numbers of transaction-processing users, and a full-function transaction-management system containing transaction logging. The mirrored-disk feature automatically records data on two different disk drives to assure data integrity in the event of disk crashes. The intelligent-terminal-handling software improves response time and productivity. In the event of a system fault, transaction logging reconstructs and restores partial transactions.

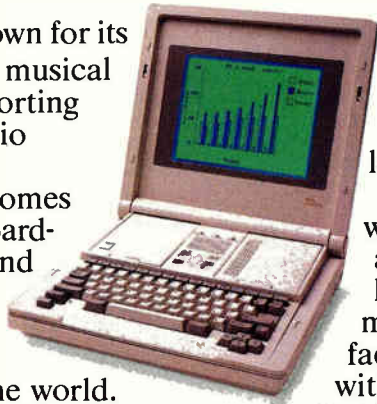
These features are being incorporated gradu-



2. HANDY PIPES. Symetrix uses named pipes (a Unix interprocess communications feature) to link Pick and Unix. A Pick application uses a Unix service (a) and a Unix application can access a Pick data base (b).

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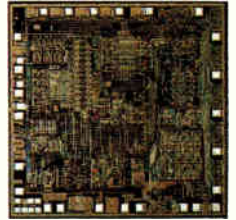
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BBN Advanced Computers Inc. is taking the wraps off a new operating system that promises to make waves in the world of parallel computing: a high-performance, multiprocessor version of AT&T Co.'s Unix. The Cambridge, Mass., parallel-computer pioneer has also unveiled a massively parallel new hardware base, the Butterfly Plus, along with two stand-alone computers built around it.

The new operating system is Mach 1000, the first large-scale, parallel-processing, commercial system to evolve from Carnegie Mellon University's Mach multiprocessor operating-system kernel, which in turn is based on Berkeley Unix 4.3 bsd. It will be offered along with the company's proprietary Chrysalis operating system.

Mach was meant to be a true multiprocessor implementation of Unix. BBN has modified it in its Mach 1000 operating system to offer extensive support for networking protocols, including the TCP/IP standard, and make it easier to implement flexible virtual memory. For example, it allows two processors to share the same memory address space while protecting against overwriting, and it also supports sparse address space more easily than Chrysalis does.

The new hardware, meanwhile, boosts the performance of each node in BBN's current-generation Butterfly architecture from 1 million instructions per second to 2.5 mips. All this power is available at half the price of the hardware it replaces: \$5,000 per mips. What's more, Butterfly Plus increases overall system performance from 250 to 600 mips for the maximum configuration of 256 processors, and also offers 1 gigabyte of shared memory.

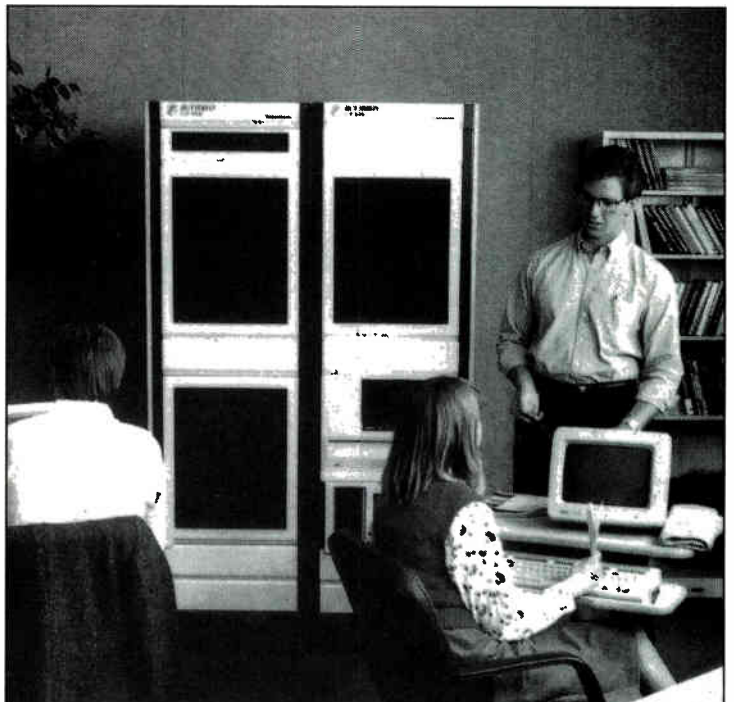
The Butterfly Plus is the heart of a new general-purpose computer, the Butterfly GP1000, which will be available next March. The machine is intended for applications developers seeking higher performance in such tasks as production scheduling, circuit simulation, molecular modeling, and expert systems. Later next year, BBN will unveil the Butterfly RT1000, which is aimed at real-time simulation, scheduling, image understanding, signal-processing, and telemetry applications. Though both machines will share the Butterfly Plus architecture, only the GP1000 will offer the Mach 1000 operating system. The RT1000 will be equipped instead with both a pSOS real-time operating system and a VMEbus now under development. The computer will be beta tested the second half of next year.

For BBN, the two developments represent the first expansion beyond the Chrysalis operating system and the first fruits of a \$32 million fi-

HERE COMES HIGH-POWERED UNIX FOR MULTIPLE CPUs

BBN Advanced Computers is building a multiprocessing Unix around Carnegie Mellon's Mach operating-system kernel—and Butterfly Plus hardware to run it

by Lawrence Curran



1. A MONARCH. The king of the Butterfly computer product line is the new GP1000 with up to 256 of the new double-speed processors.

ancing arrangement and limited partnership with Paine Webber Development Corp. announced just last spring. The financing came less than a year after BBN was spun off in July 1986 as a subsidiary of Bolt Beranek and Newman Inc., the pioneer network and communications company. Its charter is to continue to develop parallel-processing computers based on the Butterfly processor and switch technologies.

While the hardware enhancements embodied in the Butterfly Plus architecture are important to the GP1000's improved performance, the machine's ability to offer the Mach 1000 operating system is crucial. BBN engineers have enhanced Carnegie Mellon's Mach multiprocessing kernel to enable it to make the best use of the inter-processor synchronization mechanisms provided in the Butterfly architecture.

Among these mechanisms, now supported by Mach 1000, are atomic operations. An atomic operation, such as an atomic read, is an operation that can't be interrupted. This protects the integrity of one process from another. For example, a read involving a reference through the switch to a remote memory location can't be interrupted. Atomicadd, atomicor, and atomicand are atomic operations that allow programmers to guard critical regions and maintain data consistency for memory shared among processors.

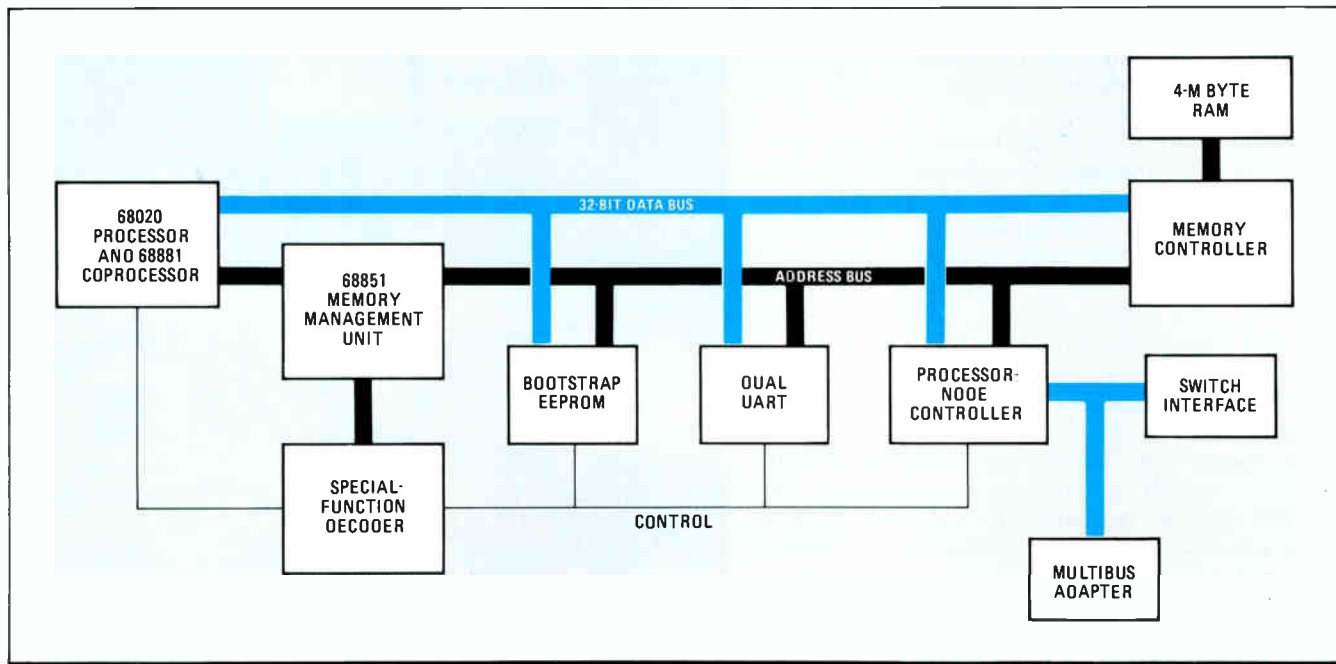
And while Unix is a time-shared system, Mach 1000 allows users to dedicate certain processors to higher-performance applications or other job mixes. BBN has added special calls so that a programmer can create processes or allocate memory on specific processors, dedicate nodes to particular applications, and dictate how many processors should be used for an application.

Mach 1000 supports BBN's applications library,

a development tool for C and Fortran 77 programs that helps programmers to manage system resources and to interface applications to the operating system. The library is called the Uniform System. It provides configuration independence for parallel programs, and creates a single large address space that resembles a familiar uniprocessor development environment. The Uniform System provides dynamic load balancing across all processors for high processor utilization and program efficiency. It also includes a performance-analysis facility for graphically displaying and analyzing program behavior dynamically.

Mach 1000 also supports X Windows, the network-user environment that is becoming a de facto standard. This means that Butterfly programmers can display both text and graphics applications and exchange information between windows. Mach 1000 takes Mach a step further by enabling the system to deal with a nonuniform memory architecture in which it's advantageous to keep some memory references local to the processor board and necessary to refer others through the switch to remote memory.

To take advantage of the capabilities of the new operating system, BBN designers refined the hardware used in the two earlier generations of Butterflies. They managed to push the performance of the Butterfly Plus processor to 2.5 mips per node by integrating 32-bit data and address paths throughout the system. The top performance in the earlier Butterflies is constrained by the 24-bit data path dictated by board architecture and the 24 address pins of the Motorola 68020 microprocessor. The new processor comes with 4 Mbytes of 256-Kbit random-access memory on each processor node, com-



2. NEW NODE. The new processor nodes for the Butterfly system are complete computers with memory and MC68851 memory management units.

UPDATE: FERRANTI IS BUSY WITH ITS BIPOLAR ARRAYS



A BIPOLAR GATE ARRAY THAT RUNS FAST ON LOW POWER

Ferranti puts a new twist on an old process in full gate arrays with 2.5-gate/die and 100-MHz system speeds—with power dissipation ratings that rival CMOS.

Reaction to Ferranti Interdesign Inc.'s DS family of 2,000- to 10,000-gate bipolar arrays [*Electronics*, Oct. 2, 1986, p. 68] has exceeded the company's most optimistic projections, according to Phillip Pollock, marketing manager for uncommitted logic arrays at the Scotts Valley, Calif., company. Pollock is unwilling to say how many designs it has won with the new family, but he will say that the company is postponing the introduction

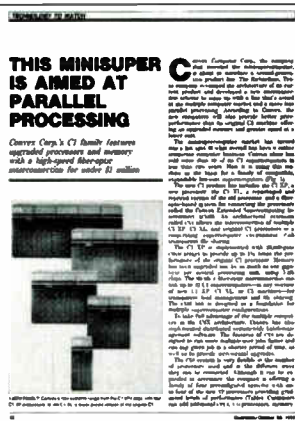
of any higher density versions. "We are finding that with a maximum of 10,000 gates, there are more than enough applications out there to keep us busy," says Pollock. "When the

user community signals that it needs higher densities, we are ready to go, but for now our current range of offerings is more than enough."

Built with the company's advanced bipolar process, the DS series is capable of gate delays in the 1-ns range, clock frequencies up to 250 MHz, and system speeds as high as 100 MHz. The gate arrays are fabricated using a 1.5- μ m version of the company's collector-diffused-isolation process and implemented using a proprietary circuit technique called differential logic.

This process requires only six to eight masking steps, says Pollock, compared with the 12 to 15 steps for competitive bipolar and CMOS processes. The flexibility of the series has been enhanced through the use of a differential logic scheme involving the selective steering of current through a logic tree by means of differential pairs of transistors stacked across the supply rail, but with flip-flop delays that are only marginally greater than delays for single gates. The technique's inherent common-mode rejection removes problems that are associated with noise, crosstalk, supply-voltage drops and temperature variations. —Bernard C. Cole

UPDATE: ITS XP MINISUPER KEEPS CONVEX ROLLING



THIS MINISUPER IS AIMED AT PARALLEL PROCESSING

Convex Corp.'s C1 family features upgraded processors and memory with a high-speed fiberoptic interconnection for under \$1 million.

A year ago, minisupercomputer pioneer Convex Computer Corp. transformed its uniprocessor C1 machine into a family of products expandable from one to four processors [*Electronics*, Oct. 30, 1986, p. 56]. The Richardson, Texas, company also announced at that time a faster processor for the new C1 XP family featuring 1.5 times the performance of the old one: it is built with 20,000-gate CMOS gate arrays, compared with 8,000-gate

arrays in the first CPU. Other enhancements included 1-gigabyte memories and an 80 mbits/s fiber-optic interconnection to link C1 XP computers in a network.

Now, a year later, most of the systems Convex sells are in the XP family. And "approximately 50% of the XP systems sold so far are the [single-processor] XP1s," says Bob Paluck, president. Most of the rest are XP2s, he says, although the company has just delivered its first four-processor XP4—an upgrade from an XP1—to the Scripps Institute in La Jolla, Calif.

While the first buyers of the Convex C1 systems were primarily research labs in industry, government, and universities, now commercial customers are starting to get in on the act. Paluck reports that in the last quarter, the company sold several systems to commercial users.

But the three biggest application markets remain structural analysis, signal and image processing by government and aerospace companies, and geophysical exploration. The most promising emerging market, says Paluck, is in computational chemistry. "We see lots of action [there]; we offer all the key [applications] packages [for computational chemistry]."

Indeed, Convex has worked with third-party application vendors to put up about a dozen chemistry applications. These were among more than 20 such third-party applications Convex added in its last quarter. "We will have about 200 third-party applications up by the end of the year, up from 100 at the beginning of the year," says Paluck.

With these applications running on C1 machines, customers are getting a lot more work done. Paluck quotes a West German client in computational chemistry as saying that the C1 system allows one organic chemist to design up to 12 new organic compounds each week, whereas he was lucky to do 12 per year before.

Another trend noted by Paluck is the increased use of the large main memories made available last year. These big memories are most used today in the geophysical and computational-

fluid-dynamics applications. "A large main memory allows users to do three-dimensional modeling instead of 2-d, and to be able to simulate much larger models, such as a whole airplane—even one as big as a 747," Paluck says.

The one new item introduced a year ago that is not getting much use yet is the fiber-optic link. According to Paluck, most of the hardware connections among Convex systems use Ethernet links.
—Tom Manuel

TECHNOLOGY TO WATCH

Integrated Device Technology Inc. went back to the drawing board last year shortly after it announced that it had just produced samples of the first parts for its new 49C404, a "breakthrough" microprogrammable 32-bit-slice processor [*Electronics*, Oct. 30, 1986, p. 51]. The Santa Clara, Calif., company then spent a year developing a higher-performance version, which is now scheduled for introduction in the first quarter of 1988.

"When we looked at the competitive situation, it was clear to us that to establish a presence in the marketplace we'd have to go into redesign on the part immediately, to generate an even faster follow-on," says Larry Jordan, vice president of marketing at IDT.

That meant the company had to decide whether to go to market with the original 49C404, which was supposed to compete with 32-bit building block designs from the likes of Advanced Micro Devices Inc. and Texas Instruments Inc. It chose not to, figuring the money needed to launch the product would be better spent supporting existing products.

The new processor will boast instruction-execution cycle times in the 40- to 60-ns range, versus about 80 to 120 ns for the earlier part. The

UPDATE: IDT REWORKS ITS 32-BIT-SLICE PROCESSOR

speed improvement, Jordan says, is achieved through architectural and circuit improvements combined with an aggressive new CMOS process with 1.0- μ m geometries, compared with the original's 2- μ m CMOS process.

Otherwise, the newer version incorporates many of the features of the earlier one. Among them are a register file with four output ports and three input ports, an on-board funnel shifter that is linked sequentially to an eight-function, 32-bit arithmetic logic unit. Its three-bus architecture is optimized for bidirectional operations. These features allow shift, rotate, mask and merge operations in a single clock cycle, the company says, rather than in separate cycles as in competitive designs.
—Bernard C. Cole



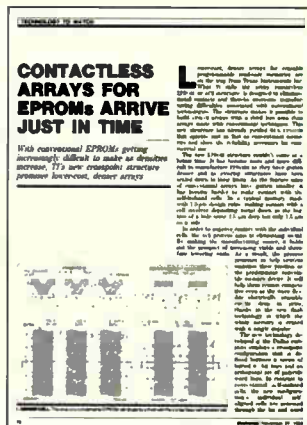
TECHNOLOGY TO WATCH

Denser, lower-cost arrays for erasable programmable read-only memories were the promise held out a year ago by Texas Instruments Inc. for its contactless crosspoint EPROM array structure, dubbed ACE [*Electronics*, Nov. 27, 1986, p. 70]. Now, TI says that prototype EPROMs built with ACE have performed so well over the past year that it is preparing to launch a 1-Mbit EPROM family using the process. The devices will debut in the first quarter of 1988, says Pradeep Shah, manager of advanced nonvolatile product development in TI's MOS memory division, Houston.

ACE's contactless structure overcomes the problem of using metal to make contact with the self-isolated cells of the memory array. Instead, the cells are accessed through buried n+ bit lines and orthogonal polycide word lines. Isolation between the bit lines and the word lines is provided by a layer of thick oxide grown over the n+ layer. Isolation from one bit line to the next is achieved by ion implantation. In practice, TI does use some metal, to reduce bit-line resistance. Expected improvements in polycides will eliminate all of the metal, Shah says.

UPDATE: TI'S 1-MBIT EPROM TO USE CONTACTLESS ARRAY

The first product is the 64 K by 16 bit TMS27C210, which is currently undergoing qualification tests. This device will not quite deliver on the promise of greater density: checking in at 86,000 square mils, the chip is comparable in size to conventional 1-Mbit EPROMs. But Shah points out that the chip will be made with relatively loose 1.5- μ m design rules, while competitive products use 1.2- μ m rules to achieve the same density. As to cost, Shah says the ACE process has the potential for greatly reducing the chip size, a major cost factor. Prices have not been set. TI is also developing a 128 K by 8 bit version, the TMS27C010.
—Samuel Weber



MILITARY/AEROSPACE NEWSLETTER

NOW ADA HAS A REAL-TIME OPERATING SYSTEM

The biggest problem in writing application software in Ada, the mandated high-level language for all U. S. military computers, has always been the lack of a real-time operating system that supports it. Now Ready Systems, a Menlo Park, Calif., software firm specializing in real-time operating systems, has joined with Telesoft, a supplier of Ada compilers, in an attempt to meet that need with RTAda. Targeted at embedded mission-critical systems, such as head-up displays, engine controls, and weaponry, RTAda draws heavily on VRTX, Ready Systems' flagship real-time product. Ready Systems is expected to unveil RTAda and RTAda-1750A, a development system aimed at Mil Std 1750A computer applications, at ADA Expo in Boston Dec. 8-11. □

TRW SEES FIRST SILICON ON A PHASE 2 VHSIC MEMORY CHIP

The first silicon to come out of TRW Inc.'s Phase 2 Very High Speed Integrated Circuits program is a memory chip built to demonstrate self-testing and self-configuring functions. But TRW's Electronic Systems Group in Redondo Beach, Calif., acknowledges that the device does not boast the 0.5- μm dimensions called for by VHSIC Phase 2. Instead, it has designed the part with the 1.25- μm lines developed for Phase 1. The reason: a delivery delay for the Perkin-Elmer Corp. Aebele 150 direct-write electron-beam system needed to reach 0.5- μm dimensions. The design called for a 725-Kbit usable capacity, but on-chip cell yields were high enough to give a 1.2-Mbit capacity, says Thomas A. Zimmerman, director of the company's VHSIC program. Despite the delivery delay for the e-beam system, Zimmerman says TRW expects to meet 1989 Phase 2 delivery deadlines. □

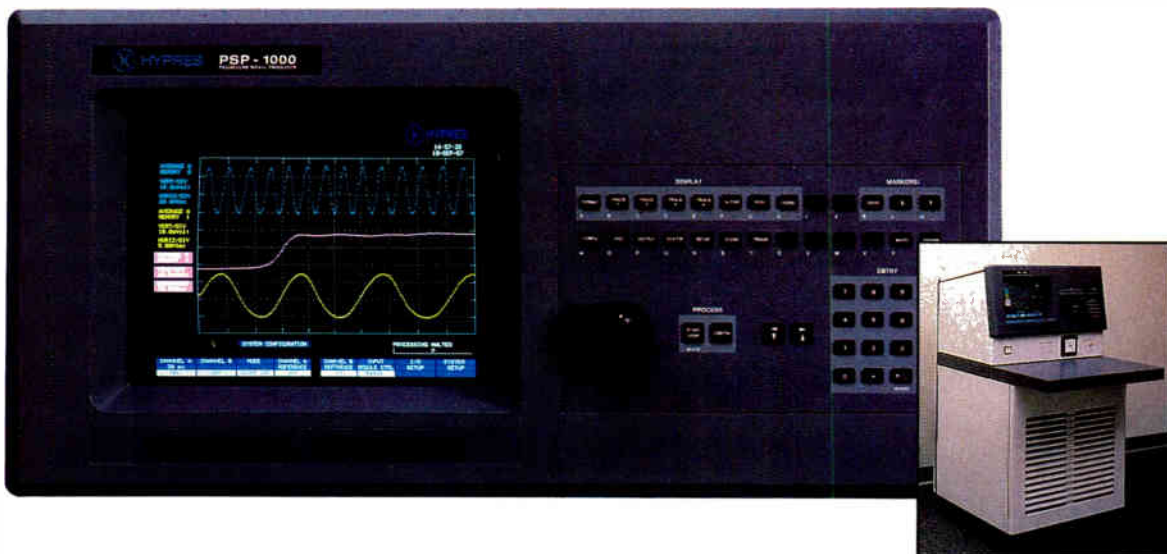
DARPA SCRAMBLES TO FIND THE MONEY FOR SUPERCONDUCTOR RESEARCH

The Defense Advance Research Projects Agency is looking to award contracts for high-temperature superconductor research in early January—but just where the funding will come from is still up in the air. Richard A. Reynolds, director of Darpa's Defense Sciences Office, says the agency is willing to redirect about \$50 million of its own funds over the next three years, but that won't be enough. He figures that a minimum of \$20 million a year for as many as 20 years or more will be necessary to put superconductors in the forefront of useful military technologies. There is hope that one well-funded defense program might be interested in kicking in some money: "It now appears that the Strategic Defense Initiative Organization may join the program," Reynolds says. The proposals cover applications ranging from thin-films for microelectronics and infrared detection to bulk magnets for sophisticated weaponry. □

UNITED TECHNOLOGIES TO ADD LINEAR BIPOLAR CHIPS TO ITS MILITARY LINE

The United Technologies Microelectronics Center, Colorado Springs, Colo., is adding high-voltage linear bipolar circuits to its line of digital CMOS military-standard products. UTMC plans to supply prototypes in next year's first quarter on what are billed as the first standard monolithic transceiver circuits developed for the Air Force Mil Std 1553A and 1553B bus. The UT63M1XX family will be offered in both single- and dual-channel versions designed to meet 1,553 redundancy requirements. The dual-channel version features custom packaging with two physically and electrically isolated cavities, each housing one of the transceiver chips. UTMC says the devices will dissipate less than half the power of conventional hybrid implementations, which typically require a 3.6- to 4.4-W duty cycle. The UT63M1XX family is planned for production in next year's third quarter. □

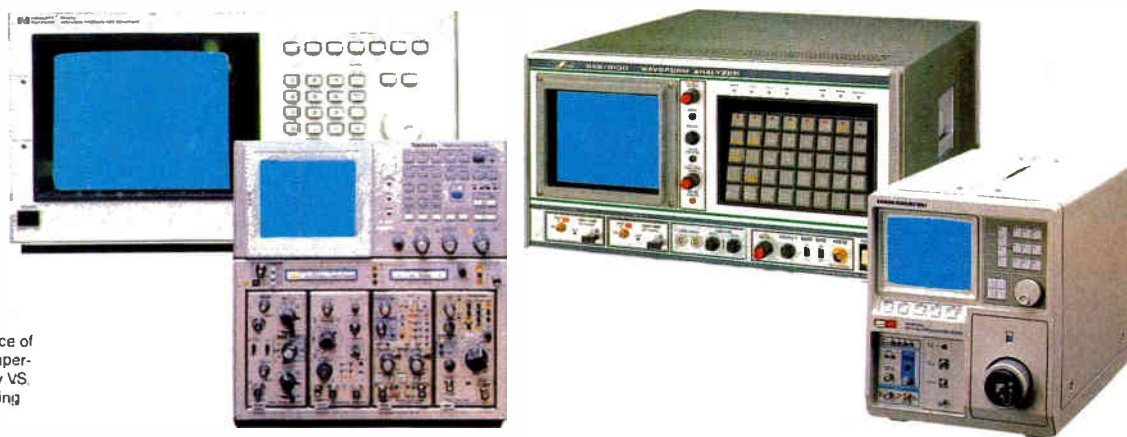
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NEW PRODUCTS

ZYMOS SIX-CHIP SET CUTS COST AND CHIP COUNT FOR PC AT CLONE

POACH/ATF-B FAMILY ELIMINATES SUPPLEMENTARY TTL LOGIC

Zymos Corp. is wooing makers of IBM Corp. Personal Computer AT compatibles with a chip set that would enable them to build 16-MHz performance for about \$300 in an assembled motherboard—that's \$25 less than competitors' chip sets. Pricing on the six-chip set is \$90. A 12-MHz version costs \$75.

Harnessed to CMOS versions of Intel Corp.'s 80286 microprocessor, 80287 math coprocessor, 8042 keyboard controller, and 512 Kbytes of system memory, the six-chip Poach/ATF-B set requires no additional TTL parts to implement an AT system. The solution is based on the Sunnyvale, Calif., company's extensive library of standard-cell "supercells." It offers a total component count of 29 chips—including 20 memory chips—compared to more than 40 chips for the competition. Two more Poach chips can be added to make the design compatible with Intel's 32-bit 80386 microprocessor.

PS/2 RIVAL. Clonemakers can even use the chip set to compete successfully on a cost/performance basis with IBM's recently introduced Personal System/2 Model 30, says Robert G. Andrews, director of technical marketing. This is possible, he explains, because the Model 30 does not support IBM's Micro Channel architecture or its Video Graphics Adapter standard. Several Taiwanese companies, he says, are already hard at work on AT clones that aim at matching the Model 30's functionality.

Operating system compatibility presents no problem because the Zymos chips support Microsoft Corp.'s MS-DOS and OS/2, the company says.

Zymos started by upgrading its Poach 1 and 2 chips, introduced in 1985. Zymos put a lot of effort into keeping the pinouts similar to reduce the time AT designers need to adapt the new chips, says Andrews, but the earlier chips ran at 8 MHz, and additional logic had to be added to bring the enhanced versions up to 16 MHz.

The update of the Poach 1 is the Poach 7. It performs system clocking and control functions, including clock-switch logic that is needed to maintain 100% AT compatibility. Since AT expansion

ZYMOS CHIPS TAKE OVER PC AT FUNCTIONS

| POACH 7 | POACH 8 | POACH 10 |
|--|---|---|
| SYSTEM CLOCKING AND CONTROL, INCLUDING CLOCK-SWITCH LOGIC REPLACES 8259As (TWO); 82288; 82284; 6818 | DIRECT-MEMORY-ACCESS OPERATIONS, INCLUDING TIMER-COUNTER PERIPHERALS REPLACES 8237As (TWO); 8254; 74612; 8284 | ADDRESS-BUS BUFFERS |
| POACH 11 | POACH 12 | POACH 13 |
| DATA-BUS BUFFERS PARITY-GENERATION LOGIC | MEMORY CONTROL: • CONFIGURATION • PAGED, INTERLEAVED SUPPORT • BURST-MODE REFRESH • WAIT-STATE CONTROL • SHADOW-RAM CONTROL • 8-, 16-BIT BIOS SUPPORT | • 1-KBYTE BATTERY-BACKED RAM • SLEEP-MODE CONTROL • REAL-TIME-CLOCK OSCILLATOR • PROGRAMMABLE ADDRESS DECODE • TWO 24-BIT PROGRAMMABLE COUNTERS |

boards run at 8 MHz, the Poach system must have the capability of slowing itself by 8 MHz when addressing an expansion board, says Andrews. In addition to the new logic, Poach 7 also uses Zymos supercells to replace five chips on the original AT motherboard: two Intel 8259A programmable-interrupt controllers, an 82288 bus controller, an 82284 clock generator, and a Motorola Corp. 6818 real-time clock/CMOS random-access memory to hold the date and time as well as configuration data.

MEMORY OPERATIONS. Replacing the Poach 2, the Poach 8 handles direct-memory-access operations, including timer-counter peripherals. It replaces two Intel 8237 programmable DMA controllers, an 8254 programmable interval timer, an 8284 clock generator and driver, and a Texas Instruments Inc. 74613 memory mapper.

Samples of the Poach 7 and 8 chips will be available in mid-November.

The remaining four Poach chips are all new and will be available in sample quantities late in the first quarter of 1988. The Poach 10 chip supports the Lotus-Intel-Microsoft Extended Memory System Version 4 to the system board and to extended memory adapter cards. In other words, it gives the system the ability to address

up to 16 Mbytes of memory. The Poach 11 data buffer handles parity generation logic. The Poach 12 memory controller implements memory-control configuration. This chip allows the use of slower, less expensive dynamic RAMs for system memory. Running on a 16-MHz clock, for example, designers can use 120-ns DRAMs and achieve wait-state performance of half of a clock cycle in a two-way interleaved page mode. Using 100-ns DRAMs, the wait-state drops to a tenth of a clock cycle in four-way interleaved page mode.

The Poach 13 targets laptop applications. It includes circuitry that puts the 80286 microprocessor in standby mode to extend battery life. It can actually put the laptop to sleep between keystrokes, according to Andrews. The Poach 13 also includes 1 Kbyte of battery-backed RAM, which holds system information in memory when the laptop is in the standby mode.

Besides high-performance ATs and laptops, the Poach/ATF-B fits applications such as high-integration, small-footprint desktop AT systems; PC AT-based terminals; and single-board computers.

— Jack Shandle

Zymos Corp., 477 N. Mathilda Ave., Sunnyvale, Calif. 94088

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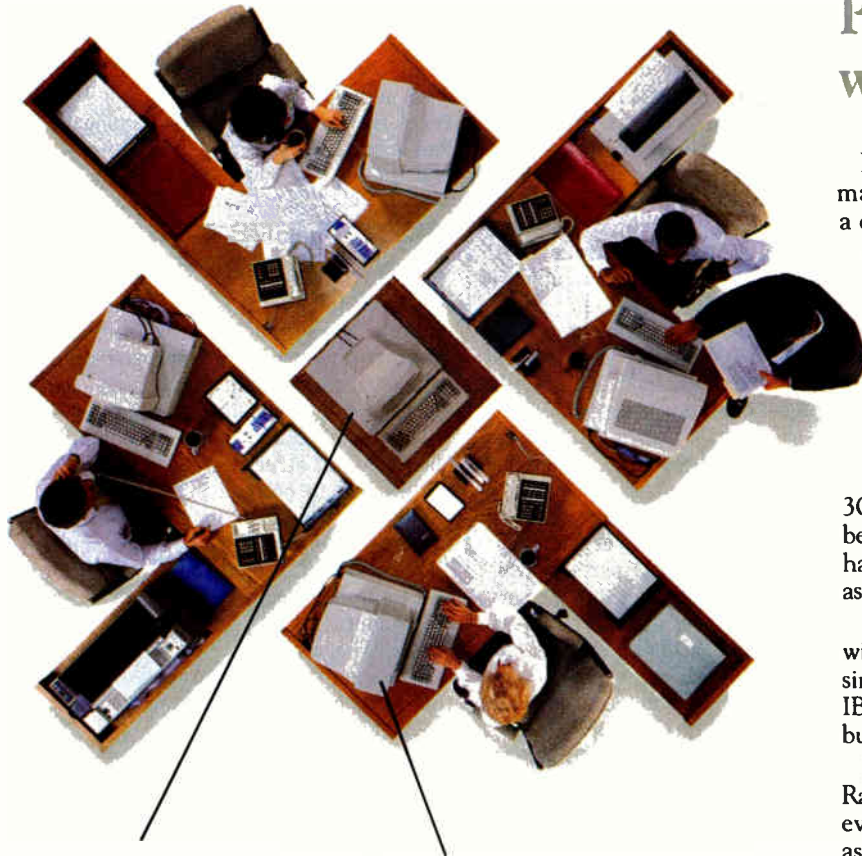


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MICROPOLIS 16-MS DRIVE UNDERCUTS COMPETITION BY 40%

Micropolis Corp.'s 1560/1580 series of 5¼-in. Winchester disk drives delivers 16-ms access times and 765-Mbyte capacity in the same package size as 380-Mbyte drives. And the drives are priced at \$3 per Mbyte in quantity purchases, a cost the Chatsworth, Calif., company claims is about 40% below that of its only competitor.

At this capacity level, the drives join a select circle occupied by only one other product: the 765-Mbyte, 18-ms-access-time Model XT8760 drives that Maxtor Corp. announced a year ago. The cost per megabyte of the XT8760 is a little less than \$5, says Maxtor, of San Jose, Calif.

To round out its upgraded offerings while also addressing the threat from 3½-in drives, Micropolis is also introducing a series of half-height, 5¼-in. drives that store from 85 to 182 Mbytes.

Although the new 765-Mbyte drives basically follow the same technology as their 380-Mbyte predecessors, design engineers made significant improvements to attain the increased performance and capacity. The drives can transfer data at up to 15 MHz, for example, compared with a 10-MHz rate for the previous models. Also, the company has boosted track density from about 1,000 tracks/in. to 1,400—a 40% increase.

INTERFACES. Users may choose either the Enhanced System Device Interface or the synchronous Small Computer System Interface. With the 15-MHz data-transfer rate, the SCSI interface can transfer data at 4.0 Mbytes/s; the rate for ESDI is 1.88 Mbytes/s.

The SCSI interface supports either single-ended or differential interconnection. Reduced command overhead and the drive's 64-Kbyte buffer and read-ahead feature also help speed response. Average seek time with either interface is 16 ms, which Micropolis claims is among the fastest on the market.

The new drive not only targets original-equipment manufacturers incorporating 5¼-in. drives in their products, but also those using larger (8-, 9-, or 14-in. form factor) drives in mini- and main-frame computers, says Chet Baffa, senior vice president of sales and marketing. "The new Micropolis series com-

pares favorably with larger-diameter drives now used for applications where data is frequently accessed," he says.

While Micropolis and Maxtor are now apparently the only companies offering 765-Mbyte drives, they won't be alone for long, predicts Robert Katzive, vice president of Disk/Trend Inc., Mountain

drives is not yet clear, since there are no solid data yet. But Disk/Trend projects a burgeoning market for larger-capacity drives. In 1987, the firm says, some 75,000 300-to-500 Mbyte drives will be sold. In 1988, that figure will spiral to 360,000 units.

Micropolis's new drives are specified at an average of 30,000 hours mean time between failure. For service, all boards and mechanical fixtures are individually replaceable units, with no adjustments required. Consequently, the company says that mean time to repair is only 15 min.

Sample drives for evaluation will be ready during the second quarter of next year. Price for the SCSI model, the 1588-15, will be \$2,395; for the ESDI unit, the 1568-15, \$2,295. These prices are for quantities of 2,500.

Micropolis is also fielding its half-height 1650/1670 series of 5¼-in. drives that store from 85 to 182 Mbytes to target a market niche served by 3½-in. units. The appeal to microcomputer OEMs comes

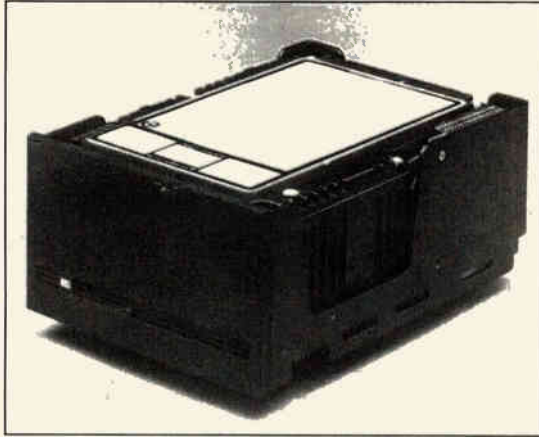
from higher performance—16 ms seek times—and capacities well above 100 Mbytes, which are generally not offered by the smaller drives, say Micropolis executives. "The new 1650/1670 series provides the best balance of form factor, cost, capacity, and performance—and in addition, a growth path to higher capacities not available with smaller drives," says Baffa.

The series is equipped with either the ESDI or SCSI interface and features a newly designed actuator that provides the 16-ms seek performance. On-track head positioning is maintained by a dedicated digital servo system that is based on an advanced digital signal processor, which compensates for variations of components. Data transfer is 10 Mbytes/s. Mean time between failure is 35,000 hours.

Evaluation units will be available in February, with quantity deliveries scheduled for April. Price of the ESDI model 1654 is set at \$1,095. The model 1674 with an SCSI interface will sell for \$1,165. Both prices are for 1,000-unit quantities.

—Larry Waller
Micropolis Corp., 21123 Nordhoff St., Chatsworth, Calif. 91311.

Phone (818) 709-3305 [Circle 340]



SPEEDY. Boasting a 15-MHz data-transfer rate, the 1588-15 with SCSI interface transfers data at 4.0 Mbytes/s.

View, Calif., a consultant to the drive business. He notes that some 14 companies presently market drives of approximately 380 Mbytes, and the marketing pattern for each new drive often resembles that of its predecessor, he says.

The history of 5¼-in. drives since appearing on the microcomputer storage scene early this decade is that a new higher-capacity product is introduced at about 18-month intervals. Deliveries are then scheduled to commence about six months later, although delays have become common due to manufacturing troubles stemming from ever-smaller tolerances.

The likely demand for 765-Mbyte-level

COMDEX/Fall '87

More than 1,300 exhibitors will crowd the floor of the Las Vegas Convention Center Nov. 2 through 6 for the Comdex/Fall '87 show to show the latest applications and products for the computer industry. This product special section previews some of the most exciting products, including leading-edge disk drives, work stations, graphics-display controllers, and data cartridges.

ration—2,048 by 1,024 pixels with 26 bit planes of image memory (1,280-by-1,024-pixel resolution), will sell for \$6,995 and requires a daughterboard. Production shipments will begin in December or January.

—Lawrence Curran

Univision Technologies Inc., 12 Cambridge St., Burlington, Mass. 01803.

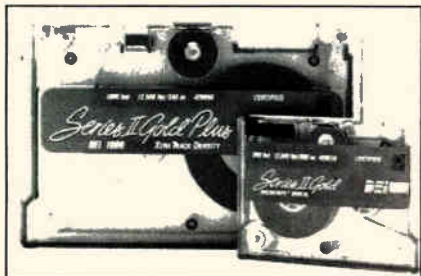
Phone (617) 273-5388

Circle 342]

500-MBYTE CARTRIDGE BOOSTS STORAGE 70%

DEI Inc.'s Series II Gold Plus 5¼-in. data cartridges store up to 500 Mbytes—60% to 70% more data than conventional cartridges.

The new cartridges were built to provide backup for Winchester disk drives and as an alternative to IBM Corp. 3480 cartridge-based drives. DEI is also offering 3½-in. MicroTape 2000XL minicartridges that can store 100 Mbytes.



Sample cartridges of both types are available now. Volume production is scheduled to begin in January 1988. Suggested retail prices are \$59 for the Series II Gold Plus 1000 cartridges and \$35 for the MicroTape 2000XL minicartridges.

DEI Inc., 10170 Sorrento Valley Rd., San Diego, Calif. 92121.

Phone (619) 452-7840

[Circle 345]

WORK STATION RUNS 32 USERS WITH NO LAN

Rexon Business Machines Corp.'s multiuser work-station system is based on Intel Corp.'s 16-MHz 80386 microprocessor and can support up to 32 users concurrently without a local-area network.

The Summit 2000 system uses industry-standard IBM Corp. Personal Computer AT architecture. Its hardware features include a dedicated 32-bit memory bus, a 1.2-Mbyte floppy-disk drive, and a 50-Mbyte fast-access Winchester disk drive.

It has 1 Mbyte of main memory, two 8-bit expansion slots, and six 16-bit expansion slots. On the software side, it uses MS-DOS 3.2 and GW Basic software.

The motherboard is socketed for an Intel 80287 or 80387 coprocessor. The system offers a wide range of configuration options, including disk storage of up to 380 Mbytes, streaming-cartridge

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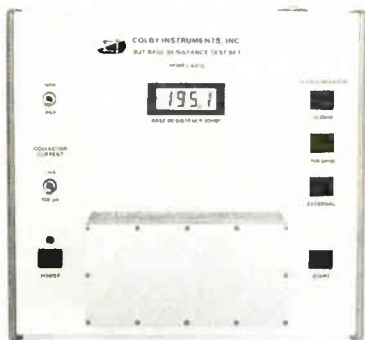
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COLBY INSTRUMENTS, INC., 1810 14th Street, Santa Monica, CA 90404. Phone: (213) 450-0261. FAX: (213) 452-0027.

tape drives, printers, and multiport-terminal support boards.

The Summit 2000 is available now. Pricing starts at under \$4,000.

Rexon Business Machines Corp., 3001 Orchard Pkwy., San Jose, Calif. 95134
Phone (213) 641-7110 [Circle 348]

OPTICAL DRIVES USE STANDARD SOFTWARE

Laserdrive Ltd.'s LaserBank 800 optical-disk drive is compatible with magnetic disk drives, eliminating the need for software routines and access methods different from those used for the magnetic units.

As a result, the LaserBank 800 can, without modification, run application software and operating systems developed for Winchester disks.

The optical-disk drive offers 810



Mbytes of storage, access times of 175 ms, and data-transfer rates of 2.78 Mbits/s. In the Winchester mode, it reads, writes, and appears erasable to the user. It also supports a write-once read-many mode.

Available now, single-drive LaserBank subsystems retail for \$4,995. Double-sided 810-Mbyte optical cartridges cost \$189 retail.

Laserdrive Ltd., 1101 Space Park Dr., Santa Clara, Calif. 95054.
Phone (408) 970-3600 [Circle 346]

ICON COMPUTERS LINK DIVERSE HARDWARE

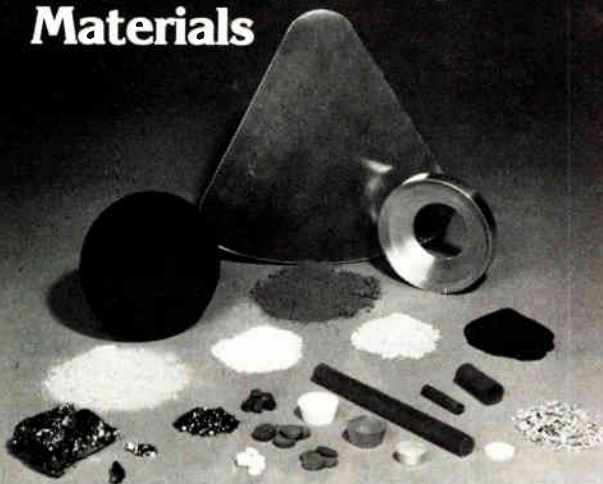
Icon International Inc.'s new MultiMicro/Mainframe family of computers can link a variety of similar and dissimilar computers and operating systems. Using multiple microprocessors in parallel, the computers can connect personal computers, minicomputers, and mainframes running the Unix, Pick, and MS-DOS operating systems.

The family includes the Icon 2000 and 3000, which are available now, and the Icon 4000, which will come to market in November. Prices begin at \$15,000 for the 1-to-16-user Icon 2000 and at \$30,000 for the 16-to-64-user Icon 3000. The Icon 4000 will accommodate 32 to 128 users and will sell for \$55,000 and up.

Icon International Inc., 774 South 400 East, Orem, Utah 84058.
Phone (801) 225-6888 [Circle 347]

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Electronics/October 29, 1987

TOOL LETS DSP DESIGNERS SEE RESULTS IN REAL TIME

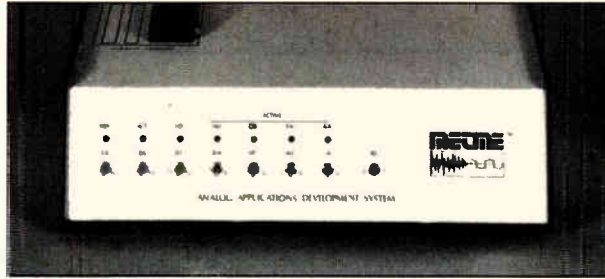
METME CUTS UP TO FOUR MONTHS OFF DEVELOPMENT TIME BY ELIMINATING THE NEED TO BUILD PROTOTYPES

A new development tool for digital-signal processing eliminates the need to build DSP prototypes by letting designers and engineers see the real-time results of changes in software or hardware on an oscilloscope plugged into the system's analog input and output port. The Analog Applications Development System—AADS—can reduce the time it takes to design DSP applications by as much as four months, say executives at Metme Corp.

The AADS unit allows engineers to "tinker with the DSP algorithms, memory configurations, and analog-interface hardware to explore tradeoffs in performance and price for his specific application," says Robert A. Nimmo, president of Metme. AADS was developed while the St. Louis, Mo., company was developing its own DSP-based analog products. "We believe what has been missing [in DSP development] is a tool that allows engineers to make just

a single change or a group of changes and immediately see the effect on the analog signal," Nimmo says.

Metme's AADS unit can be used with an attached IBM Corp. Personal Computer or compatible to implement and



PORTABLE. After software is developed, AADS can be taken into the field with its DSP program stored in battery-backed memory.

examine relatively modest modifications to algorithms prior to embedding them in firmware. In addition, it can also be connected and used with a standard DSP development system for work on complex programs.

The output of a development-system

emulator plugs directly into the top of the AADS, which then runs the modified algorithms through its configured hardware and analog interface. Once laboratory work is completed, AADS can be unplugged and taken into the field for trial runs with the developed DSP software safely stored in its battery-backed random-access memory.

The initial version of Metme's AADS contains a DSP engine in the form of a Texas Instruments Inc. TMS32020 or TMS320C25 chip. The development system's analog port can be provided by either a customer-defined interface, a standard codec, or TI's new 32040 DSP front-end chip [*Electronics*, Sept. 3, 1987, p. 150].

Data-conversion circuits in the unit's analog interface can be set at various analog-to-digital and digital-to-analog resolutions or speeds. A range of memory speeds and configurations can also be plugged into the unit, allowing the system engineer to optimize price and performance for a DSP application.

AADS weighs 15 lb and has a power consumption of 15 W at 120 V. The 15-by-13.3-by-4.3 in. unit costs \$2,945 with analog interfaces. It is available now.

— J. Robert Lineback

Metme Corp., 4623 Morganford, St. Louis, Mo. 63116.

(800) 445-3830

[Circle 380]

IN-CIRCUIT EMULATOR HANDLES Z280 CHIP

Softaid Inc.'s Z280 Icebox in-circuit emulator supports all the features of Zilog Inc.'s Z280 microprocessor, including its extended input/output addressing, 16-Mbyte address space, memory manager, and 16- and 8-bit modes.

Compatible with any computer or terminal, the emulator runs at full 10-MHz speed without wait states. A 64-Kbit overlay of random-access memory that can be mapped anywhere in the microprocessor's address space speeds application development by functioning like part of the target system.

The Z280 Icebox is compatible with Softaid's TraceAlyzer, a real-time trace-and-performance-analysis system. The Z280 Icebox will be available in November; it will cost \$2,500. Available now,



TraceAlyzer costs \$1,495.

Softaid Inc., 8930 Route 108, Columbia, Md. 21045.

Phone (800) 433-8812

[Circle 385]

CODE GENERATOR IS BASED ON DSP32

By adding a code generator that handles AT&T Co.'s DSP32 floating-point digital-signal processor to its DFDP2 Digital Filter Design Package, Atlanta Signal Processors Inc. lets system designers speed algorithm development.

Unlike general-purpose packages that provide only filter coefficients, DFDP2 generates chip-specific code for implementing digital filters. This means the algorithm runs on the actual hardware rather than in simulation, which allows for real-time testing.

The new code generator enhances the original DFDP2 package, which handles Texas Instrument Inc.'s TMS320 DSP family.

The AT&T DSP32-based code generator retails for \$249 and is available now. It is included in the \$1,195 DFDP2 package at no extra charge.

Atlanta Signal Processors Inc., 770 Spring St., Atlanta, Ga. 30308.

Phone (404) 892-7265

[Circle 386]

SYSTEM CONTROLLER RUNS 4 TIMES FASTER

Engineers can now harness the power of Intel Corp.'s 16-MHz 80386 microprocessor and 80387 coprocessor to their instrumentation setups with Tektronix Inc.'s PEP 301 system controller.

For use with RS-422 test and measurement instruments, the controller runs two to four times faster than controllers based on Intel's 80286 chip. It is compatible with a wide variety of instruments, including oscilloscopes, logic analyzers, and digitizers.

Operating on Microsoft Corp.'s MS-DOS, the PEP 301 system allows users to program control functions in Basic. Its RS-323-C port implements an easy connection with a wide variety of printers and plotters.

The PEP 301 has a 40-Mbyte, 28-ms hard-disk drive and a 1.2-Mbyte 5¼-in. floppy drive, with slots for adding two half-height drives. The package includes a high-resolution color-graphics card, a color monitor, a dual voltage system unit, and application software.

Available now, the unit costs \$7,995. Tektronix Inc., P. O. Box 500, Beaverton, Ore. 97077.

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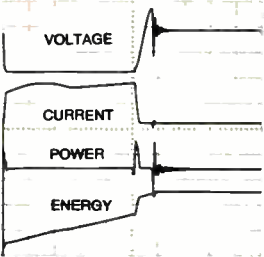
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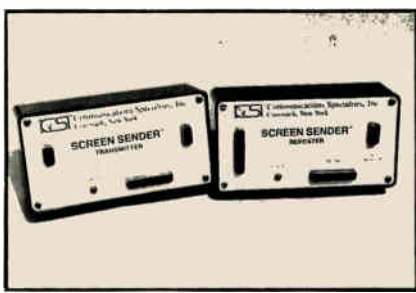
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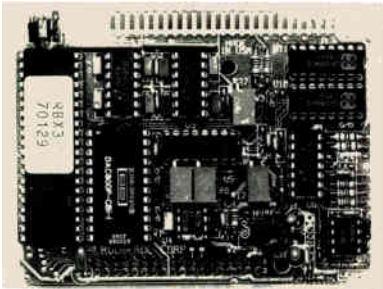
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RBX388

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Classified and employment advertising

Link Computer Graphics Inc. 103
ZTEC 103

■ For more information of complete product line see advertisement in the latest Electronics Buyers Guide
* Advertisers in Electronics International
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Electronics/October 29, 1987

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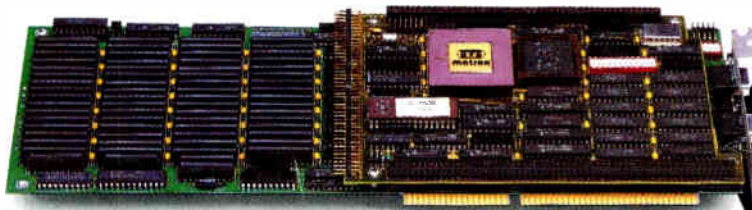
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