PHILIPS FINDS A BETTER WAY TO DO ANALOG CONVERSION/79

AN LCD THAT OUTSHINES CRTs GOES INTO PRODUCTION/90

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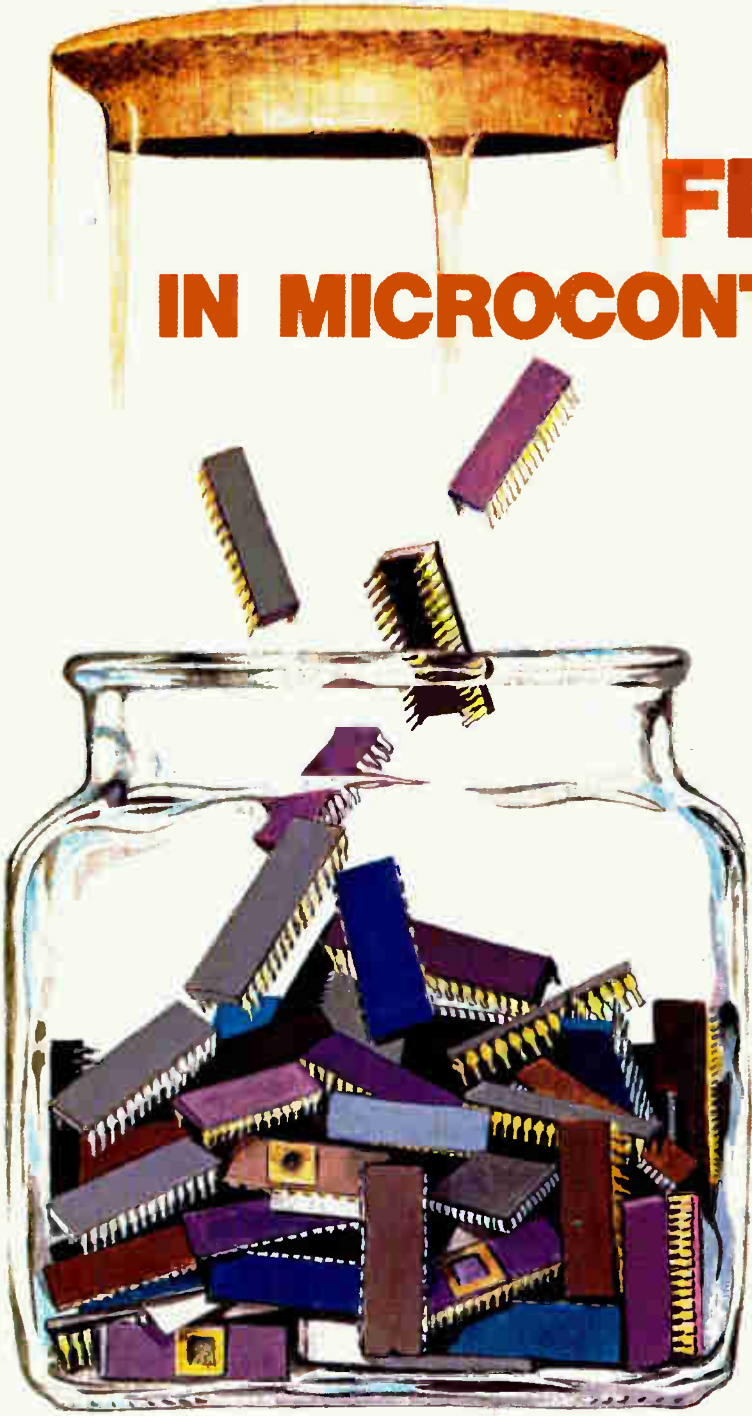


- NEW OFFERINGS, NEW PLAYERS STIR UP THE COMPETITION/55
- INTEL'S RADICAL 16-BIT REDESIGN IS TWICE AS FAST/59

The Series 32000 family. First. Lasts. All ways.

STILL THE ONLY COMPLETE, FULLY COMPATIBLE 32-BIT SYSTEMS SOLUTION FOR A FULL RANGE OF APPLICATIONS

A 32-bit microprocessor isn't just a purchase. It's a commitment.

It's a commitment *by* you to a particular microprocessor architecture.

And it's a commitment *to* you by the microprocessor's manufacturer not to abandon that architecture for some more "innovative" approach — and abandon you and your software in the process.

Without the second commitment, you shouldn't make the first.

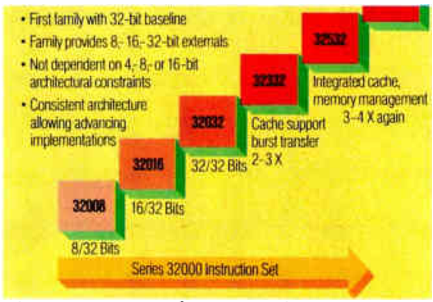
And no one has made a larger, longer, more consistent commitment to 32-bit technology than National.

FIRST: FULL 32-BIT ARCHITECTURE

In 1982, we introduced the world's first commercial 32-bit microprocessor.

Later this year, we'll be introducing the world's most advanced 32-bit microprocessor, the NS32532, with integrated data and instruction caches, integrated memory management, and a four-stage instruction pipeline.

In between, we introduced five other microprocessors, including the NS32332, a hard-working, practical 15-MHz engine that delivers 2-3 times the performance of its predecessor NS32032, and not only offers cache-memory support and bus-error retry features, but also pioneered the use of burst-mode memory transfers in microprocessors. With its variable bus-sizing capability, the NS32332 can address the needs of over 90% of the applications in use



The Series 32000 performance pathway. An integrated family of CPU's with full upward and downward software compatibility.

today, yet it is fully software compatible with the next-generation NS32532.

Five years. Seven CPUs. Interfaces from 8 to 16 to 32 bits. Performance from 0.75 to 15 MIPS peak (VAX® 11/780 MIPS). And all without having to re-engineer your software at any level.

That's remarkable performance continuity. And the reason for it is simple: National's commitment to a full 32-bit architecture from the very beginning.

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So you can spend your time designing new products, rather than re-designing old ones.

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Any microprocessor, of course, is only as good as the tools that help you put it to work.

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So you can design products faster, build revenues sooner, turn profits longer.

ALL WAYS: FULL APPLICATION FLEXIBILITY

Ultimately, however, any microprocessor has to be evaluated against a single criterion: How well does it meet *your* cost-performance targets in *your* application.

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NS32032:	32-bit interface, 24-bit addressing for cost-effective real-time applications
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NS32332:	32-bit interface, 32-bit addressing for real-time and multiprocessing applications and UNIX™-based multitasking, multiuser environments
NS32532:	The next-generation Series 32000 CPU. A highly integrated engine offering 8-10 MIPS average performance, 15 MIPS peak, and employing unique architectural features for real-time and multiprocessing environments.

So you can match your microprocessor to your needs, rather than having to adapt your needs to your microprocessor.

All of which means that our commitment to the Series 32000 family gives you something else you won't find in any other 32-bit approach.

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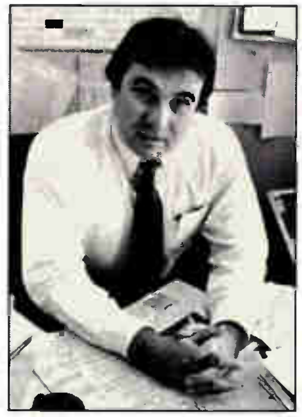
Jack Shandle is getting in deeper, and he couldn't be happier. Jack, who has been our hard-working New Products editor for a year, managed to find the time between producing that section to turn out the two articles in this issue about the Integrated Services Digital Network—a progress report on the long-awaited technology and a report on the ISDN data-protocol controller chip from Advanced Micro Devices Inc.



SHANDLE: The best of both possible worlds for a journalist.

"After a year of grappling with the entire breadth of the electronics industry, it was a challenge as well as a satisfying experience to get into a subject in depth," says Jack. "I didn't realize how much I missed the dynamic reporting side of the business, as opposed to the more static planning and managerial functions that go with being an editor. Doing them both seems to me to be the journalist's idea of utopia.

"It's also good to have an opportunity to dig deeply into the telecommunications area, because with ISDN beginning to come on, it will probably be one of the most dynamic and fast-changing fields in electronics," Jack adds. And as he points out in his overview of ISDN, there will be a lot to write about as designers more accustomed to dealing with equipment for the computer environment struggle to master the complexities of the telecom milieu.

Jack is one of those hard-to-find professionals, the engineer-journalist. He has his EE degree from the University of Pennsylvania and his master's in journalism from Temple University, both in Philadelphia. From that one might gather that Jack has an affinity for the City of Brotherly Love. He has spent the bulk of his professional life in the city or its suburbs, as an engineer for the Philadelphia Electric Co. and as a reporter and columnist for the *Bucks County Courier Times* in Levittown, Pa. Even now that Jack works in New York, he makes the long daily commute from bucolic Bucks County.

Jack says of his dual specialties, "I like them both. This business of covering the industry is the only one I know of where I can use both at the same time."

It's nice to be neighborly, and the folks in Texas have developed the technique into a fine art as well as a tradition. Now a bunch of electronics people—suppliers of semiconductors, original-equipment manufacturers, distributors, and reps—are putting their culinary skill on the line "to promote goodwill with design and purchasing personnel in the local electronics community."

That's what it says in the latest prospectus of the world famous and highly respected North Texas Electronics Chili Council, which is going to show what heat dissipation really means on Oct. 3 with the Electronics Industry Chili Cook-Off. It starts at noon at Farmers Branch, which is five miles east of the Dallas-Fort Worth Airport.

But if they want to be really neighborly, how about some of those good ol' boys comin' on up to New York and showin' us what real prize-winnin' Texas chili can do for a Yankee's disposition?

Laurence Altman

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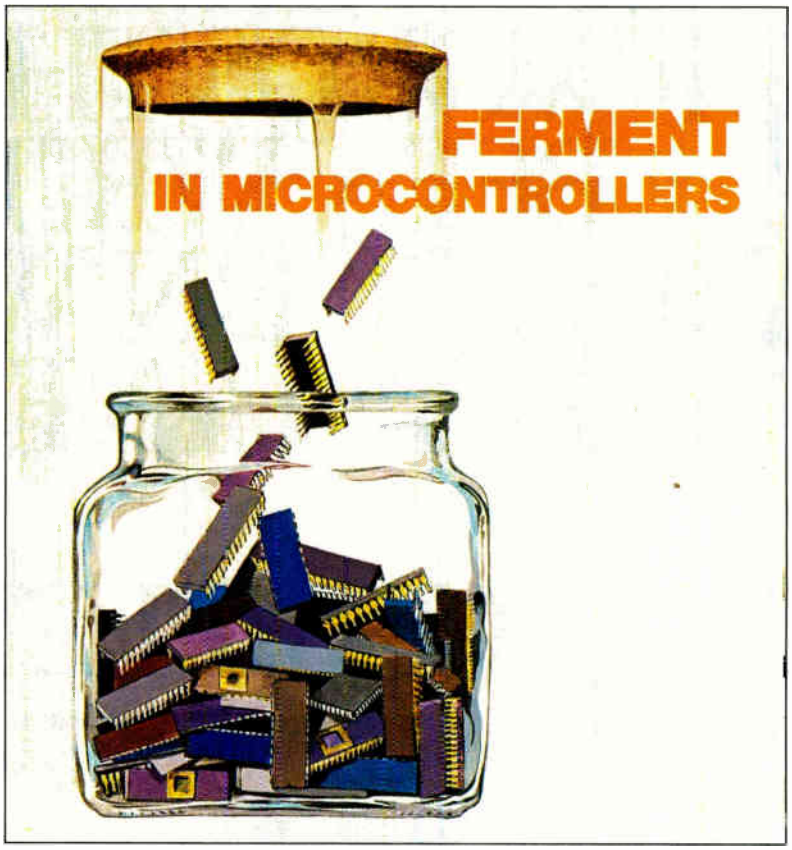

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NEW PRODUCTS

DEPARTMENTS

TO THE MILLIONS OF WORDS THAT HAVE BEEN WRITTEN ABOUT ISDN, WE'D LIKE TO ADD A NEW ONE.

COMPLETE.

For years, you've read about the incredible new products you can design when ISDN becomes a reality. And now, you can stop waiting and finally get started. Because our 29C53 ISDN Kit delivers what most people have only been writing about. A complete ISDN solution.

There's our 29C53 "S" Transceiver, which transmits and receives data at the ISDN basic rate of 192 kbps. And fully implements Open Systems Interconnection (OSI) Layer 1. There's our programmable 29C48 Voice Conversion Chip. And our 80188 CPU, which performs protocol processing.

But that's just the beginning. What really puts you ahead is our ISP188 software, which completes OSI layers 2 and 3.

Co-developed with DGM&S, ISP188 is made up of literally thousands of lines of code. And it's ready to run today. As a result, you save man-years in development time and get to market quicker.

When you use this complete package, it will take care of the most common design issues associated with ISDN protocols and standards. So you can focus your resources on making your product the best of its kind. No matter what you're designing, from a low end terminal adaptor, to PCs, to PBXs. Or even the first products of an entirely new kind.

What about industry standards? We're working on compatibility issues with the world's largest telecommunications equipment suppliers. In fact, we've recently concluded an agreement with AT&T that ensures interoperability between our devices and theirs.

As a result, you can begin to design with this kit right away. And be certain of compatibility with ISDN systems today and tomorrow.

And now that standards are set, the opportunities are wide open. To help you make the most of them, we also offer a full range of development tools, such as our Terminal Evaluation Kit, and our Line Card Evaluation Kit.

So if you've been waiting for ISDN, the wait is over. We have samples and software available now. Call (800) 548-4725 and ask for Literature Department W-369 for more information. And we'll show you the one word about ISDN that's worth a million.

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THE SOFTWARE PROBLEM SOLVERS

If you were ITT and had to automate power monitoring and control systems for telephone power plants, who would you turn to? And what if you were Bell Canada and your purpose was to automate the company's trouble reporting, analysis, and control procedures? Or suppose you were the Allright Parking Company and had to automate the data acquisition and distributed control of a large number of parking facilities?

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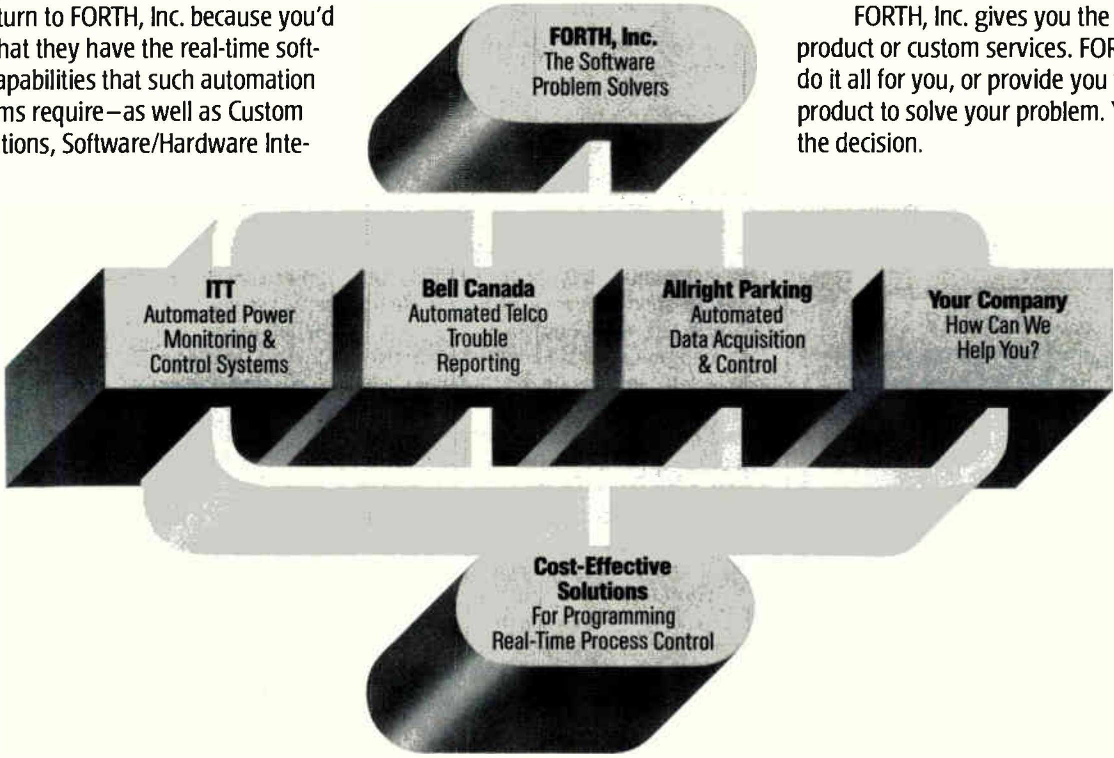

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1. The primary end product (or service performed) at your plant, and the product (or service) that is your own work. (Insert one code for each)

☐ Plant ☐ Own work

A. Computers, data processing and peripheral equipment, office and business machines
B. Communications, data communications, telecommunications systems and equipment
C. Navigation and guidance, aircraft and missile systems and equipment (oceanography)
D. Test and measurement equipment
E. Consumer products (TV, radio, hi-fi, recorders, home computers, appliances)
Q. Medical systems and equipment
R. Industrial control systems and equipment
G. Semiconductor production equipment (component insertion, coil winding, etc.)
H. Electronic sub-assemblies, components and materials (active and passive components, ICs, discretes, hybrids, power supplies)
I. Other manufacturers using electronic equipment as part of their manufacturing process (machine tools, chemicals, metals, plastics, pharmaceuticals, etc.)
J. Government and military
K. Independent research and development laboratories or consultants
L. Research and development organizations which are part of an educational institution
M. Independent software developers
N. Operators of communications equipment (utilities, railroads, police, airlines, broadcasters, etc.)
O. Educational: 2-4 year colleges, universities
P. Other (please describe)

2. ☐ **Your principal job function: (Insert one code only)**

A. Corporate management (owner, partner, president, VP, etc.)
B. Operating management (general manager, group manager, division head, etc.)
C. Engineering management (project manager, chief engineer, section head, VP of engineering, VP of research and development, VP of quality control, etc.)
D. Software engineering
E. Systems engineering/integration
F. Quality control engineering (reliability and standards)
G. Design engineering
H. Engineering support (lab assistant, etc.)
I. Test engineering (materials, test, evaluation)
J. Field service engineering
K. Research and development (scientist, chemist, physicist, etc.)
L. Manufacturing and production
M. Purchasing and procurement
N. Marketing and sales
O. Professor/instructor at
P. Senior student at
Q. Graduate student at
Z. Other (please describe)

3. ☐ **Your principal responsibility: (Insert one code only)**

1. General management
2. Engineering management
3. Engineering
4. Other

4. Estimated number of employees at your location: (Check one box only)

☐ 1 to 49 ☐ 50 to 249 ☐ 250 to 999 ☐ 1,000 or more

5. Your engineering function: (Check all that apply)

A. ☐ I design or develop electronic products and systems (hardware and/or software)
B. ☐ I supervise electronic design or development engineering work
C. ☐ I set standards for, evaluate, test and/or support the manufacture of design components, systems and materials
D. ☐ Other function (please describe)

6. In your company or organization, do you participate in: (Check all that apply)

A. ☐ Business planning and forecasting
B. ☐ Product planning
C. ☐ Technology planning
D. ☐ No involvement in planning

7. Your involvement in the following stages of product development: (Check all that apply)

A. ☐ Evaluate the need for new products
B. ☐ Develop device specifications
C. ☐ Evaluate suppliers
D. ☐ Review prices and availability
E. ☐ Select Vendors
F. ☐ Approve purchases
G. ☐ Place orders
H. ☐ No involvement

8. ☐ **What is your title? (Insert one code only)**

Operations Management

01. President/Chairman/Owner/Partner
02. Vice President
03. Vice President of Engineering
04. Product Marketing Manager

Engineering Management

11. Technical Director
12. Chief Engineer
13. Principal Engineer
14. Research Director
15. Section Head
16. Project Engineer
17. Senior Engineer
18. Software Manager
19. Senior Test Engineer
20. Senior Field Test Engineer
21. Manufacturing/Production Manager
22. Group Leader
23. Department Head
24. Other Management (please explain)

Design or Standards Personnel

31. Systems Engineer
32. Software Engineer
33. Test Engineer
34. Field Test Engineer
35. Manufacturing Engineer
36. Production Engineer
37. Engineer
38. MTS
39. Consultant
40. Scientist
41. Physicist
42. Other Staff (please explain)

9. Products that you specify or authorize purchase of: (Check all that apply)

ICs and Semiconductors

01. ☐ Digital ICs
02. ☐ Linear ICs
03. ☐ Microprocessors
04. ☐ Semiconductor memories
05. ☐ Custom/semicustom ICs

Components

11. ☐ Resistors and capacitors
12. ☐ Interconnections
13. ☐ Switches and relays
14. ☐ Optoelectronic components
15. ☐ Readout and display devices
16. ☐ Fiber-optic components
17. ☐ Printed circuits

Equipment

21. ☐ Power supplies
22. ☐ Test and measurement equipment
23. ☐ Automatic test equipment
24. ☐ Field service test equipment
25. ☐ Analog/digital panel meters
26. ☐ Cabinets and enclosures
27. ☐ Semiconductor production equipment
28. ☐ Robotics components/equipment
29. ☐ Microprocessor development systems

Computer-based Systems and equipment

31. ☐ CAE hardware/software
32. ☐ CAD/CAM hardware/software
33. ☐ Minicomputers
34. ☐ Microcomputers
35. ☐ Computer terminals
36. ☐ Computer boards
37. ☐ Disk/tape memories
38. ☐ Graphic displays
39. ☐ Software packages/services
40. ☐ Printers/plotters
41. ☐ Computer peripherals
42. ☐ Modems
43. ☐ Communications equipment
44. ☐ None of the above

10. Your degree of profit accountability: (Check one box only)

A. ☐ I have direct profit responsibility
B. ☐ I share profit responsibility with others
C. ☐ I have no profit responsibility

11. Your level of sign-off or purchase approval authority for your company or organization: (Check one box only)

A. ☐ None
B. ☐ Less than $1,000
C. ☐ $1,001 to $ 5,000
D. ☐ $5,001 to $10,000
E. ☐ $10,001 to $25,000
F. ☐ More than $25,000

12. Other publications that you read regularly (3 out of 4 issues): (Check all that apply)

A. ☐ Electronic Design
B. ☐ Electronic Engineering Times
C. ☐ EDN
D. ☐ Electronic News
E. ☐ Electronic Business
F. ☐ Computer Design
G. ☐ Electronic Products
H. ☐ None of the above

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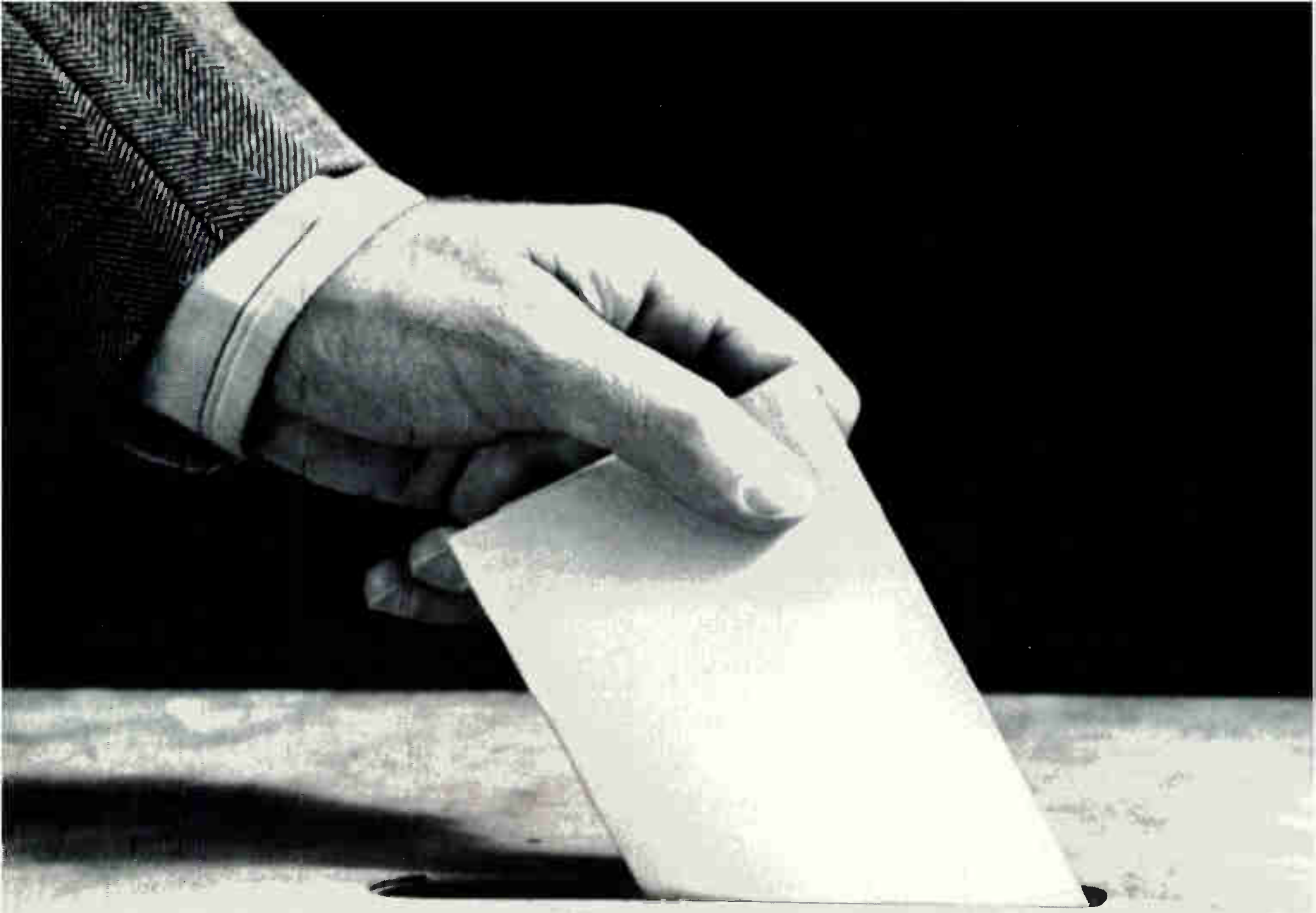

In Costa Rica, we believe in regularly scheduled revolutions.

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When it comes to business, Costa Rica is a revolutionary revelation. For more information, contact the nearest Costa Rican Investment Promotion Office.

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ELECTRONICS NEWSLETTER

SIA WANTS SANCTIONS TO CONTINUE; U.S. SHARE OF JAPANESE IC SALES FALLS

President Reagan is being urged to continue and, if necessary, stiffen sanctions against Japanese chip makers in response to what the Semiconductor Industry Association says is a lower U. S. market share in Japan one year after the two countries agreed to a major semiconductor-trade pact. SIA officials say the U. S. share of Japanese chip markets fell to only 9% in the second quarter of 1987, compared with 9.4% in early 1985. The SIA, issuing its first report on the trade pact, gives it a mixed review. SIA leaders complain that Japan disrupted supplies of key semiconductor products with production controls and minimum floor prices, imposed last April in response to chip-dumping charges by the U. S. The group says chip dumping has eased, but Japan's controls on production and prices are stifling the competitive spirit sought by the trade pact. □

SEYMOUR CRAY PUTS THE HEAT ON SUPERCOMPUTER RIVALS

Cray Research Inc. founder Seymour Cray plans to keep the throttle open despite last month's cancellation of the MP supercomputer project and the departure of project leader Steve Chen [*Electronics,* Sept. 17, 1987, p. 21]. Cray says that the Minneapolis company is ahead of schedule with the 16-processor, 16-gigaflops, GaAs-based Cray 3, and that work will begin next year on the Cray 4, which could appear as early as 1992. That machine will rely on LSI GaAs chips, 64 processors, and 1-ns cycle times to achieve 128 gigaflops. If Cray hits its targets for the Cray 3 and 4, it could spell trouble for Chen, who plans to start his own company, and for Cray's crosstown rival, ETA Systems Inc. "If Seymour's got a machine that will run 16 gigaflops by the end of next year, that's got to put some pressure on ETA," says Gary Smaby, an analyst at Piper, Jaffray & Hopwood Inc. in Minneapolis. The first ETA^{10} was delivered early this year but has still not hit its target 10-gigaflops peak speeds. And the Cray 4 is "going to make it more difficult for Chen to differentiate his product strategy from Seymour's," Smaby says. □

LSI LOGIC LAUNCHES TWO-CHIP SET FOR 1750A PROCESSOR

Applications for 1750A microprocessors should get a fillip from LSI Logic Corp.'s new two-chip set, which implements all the functions called for in the military instruction-set specification. The chip set consists of a central processor and a memory management unit—the first dedicated peripheral chip that can handle all memory management chores, according to Randy Rasmussen, program manager for standard products for the Milpitas, Calif., company. The 1.5-μm HCMOS chips run at 15 MHz, 20 MHz, and 25 MHz, and are priced at $1,250, $1,450, and $1,750, respectively. □

INTEL'S CHIP FOR MILITARY 1553 BUS WILL INTEGRATE NEW FEATURES

Designers working with the Pentagon's MIL-STD-1553B avionics bus will soon have two monolithic interfaces to choose from, now that Intel Corp. of Santa Clara, Calif., is stepping in to compete with the United Technologies Microelectronics Center in Colorado Springs [*Electronics*, June 9, 1986, p. 13]. Intel claims a number of features for its M82553 Protocol Management Unit that the UTMC part does not have, such as a bus-monitor mode that allows it to extract information passed on the bus for later use, without responding to bus signals. In this mode, the chip can be used to implement a flight recorder or a warm-backup system in a fault-tolerant configuration. The M82553, built in 1.5-μm CMOS, acts as a smart interface between the 1553 bus and a microprocessor-based system. It is optimized to work with 8086-type processors and most chips meeting the MIL-STD-1750A standard. □

PRODUCTS NEWSLETTER

NEC CHIP SET BOOSTS TV RESOLUTION UP TO 40%

Look for television picture quality to take a quantum leap forward with a chip set from NEC Corp. that uses digital-signal-storage and processing techniques to implement the Improved-Definition TV standard. IDTV delivers a 30% to 40% improvement in resolution—the best picture possible from current NTSC signals. It features 60 noninterlaced frames with twice as many scanning lines as the 60 interlaced fields used in conventional NTSC TV, as well as advanced techniques for separating chroma and luminance signals. A key chip in the Tokyo company's set is the μPD42270C field buffer. There are seven of these in the kit, each providing almost 1 Mbit of storage—263 lines by 910 pixels by 4-bits. Signal processing is done by six 1-μm CMOS chips. Also included are 11 μPD41101C line buffers, two analog-to-digital converters, and three digital-to-analog converters. Samples will be available in December for $347, with full production set for early 1988. □

CONTROL DATA CRAMS 1.236 GIGABYTES ON ITS LATEST 8-IN. DRIVE

Control Data Corp. has upped the ante in the 8-in. disk-capacity competition to 1.236 gigabytes with its Sabre 1230—a 65% increase over its industry-leading 750-Mbyte Sabre IV series. The Sabre 1230 integrates thin-film media and thin-film heads to achieve the greater capacity, and it can be equipped for any of three interfaces: SMD (Storage Module Drive), IPI-2 (Intelligent Peripheral Interface), or SCSI (Small Computer System Interface). It features a data-transfer rate of 3.02 Mbytes/s and average seek times of 16 ms. Customer evaluation units with SMD or IPI-2 interfaces will be available in the fourth quarter, while SCSI evaluation units will be available in the first quarter of next year. Production deliveries will begin in the second quarter. The Sabre 1230 costs $6,470 in volume purchases. □

KLA WAFER-INSPECTION SYSTEM WORKS FASTER, DETECTS SMALLER DEFECTS

Chip makers can hunt down defects as small as 0.6 μm up to 15 times faster with KLA Instruments Corp.'s Model 2028 inspection system than with the company's 2020—itself a pioneer in automating wafer-defect inspection with image-processing technology. Quick inspection turnaround and high precision mean fab processes can be tweaked earlier to eliminate many defects and increase yield—savings that mean the machine can pay for itself in six months to a year, says the Santa Clara, Calif., company. KLA achieves the performance boost chiefly by adding an operating mode especially tailored for repeating circuit patterns such as memory arrays. The 2028 inspects wafers at a rate of 6.5 min./cm^2 in its repeating mode, compared with 98 min/cm^2 for the single-mode 2020. Available in the second quarter of 1988, the 2028 will cost $875,000. □

MATROX PC AT ACCELERATOR DOES SHADED POLYGONS, 90,000 3-D VECTORS/S

Users of IBM Corp. PC ATs and compatibles based on Intel Corp.'s 80386 microprocessor can get 50% better 3-d solids-modeling performance for less than $7,000 with Matrox Electronic Systems Ltd.'s single-board graphics accelerator. The SM-1281 can perform 90,000 3-d vectors/s and 20,000 shaded 3-d polygons/s, while competing products offer 60,000 3-d vectors/s and no shaded-polygon feature. The SM-1281 implements 3-d rendering with a pipelined architecture and five dedicated microprocessors. Among them is a special VLSI "tile" processor that permits high-speed rendering. The SM1281 must be teamed with the Dorval, Quebec, company's PG-1281 color-display processor board. Available in November, the SM-1281 costs $6,995; the PG-1281, introduced in July, sells for $3,495. □

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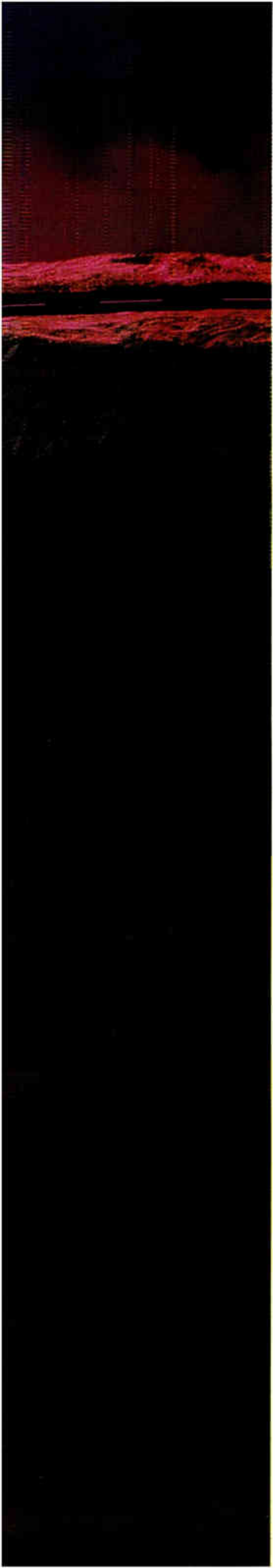

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computer Products Inc. of Norcross, Ga., sell for more than $1,100.

The board, to debut at this week's Tele-Communications Association Show in San Diego, represents "a complete change in technology—not just scaling up from 2,400 b/s," says Frank Micheletti, the Rockwell division's director of engineering. For starters, the jump in speed from 2,400 bits/s called for a major boost in modem signal processing, which Rockwell has handled by going to a 2-μm CMOS process; the company had used 3-μm n-MOS before. The resulting C53SPX processor has doubled the clock speed, to 24 MHz, and halved the instruction-cycle time, to 167 ns.

But perhaps the most notable advance in the R9696 modem is its one-chip echo canceler—also in 2-μm CMOS. The new modem must not only deal with superimposed signals, but also distinguish a received signal from interfering echoes caused by transmission through telephone-network switches. Rockwell calls its solution an algorithm-specific signal processor that performs up to 20 million arithmetic operations per second. It has a 32-bit architecture, a clock rate of 12 MHz, and is programmable for varying degrees of near and far echoes.

Rounding out the R9696 improvements is the integrated analog front end, built in 3-μm CMOS, that interfaces with telephone equipment. The chip's flexibility permits the new board to operate with existing modems at 300 to 4,800 b/s. Shipments will start in three to six months. *–Larry Waller*

INTEGRATED CIRCUITS

COMPETITION SOARS IN PC AT CLONE CHIPS

SUNNYVALE, CALIF.

A late-summer burst of activity by semiconductor makers has brought new zest to the market for IBM Corp. PC AT-compatible chip sets, which Chips and Technologies Inc. has dominated for the past two years.

The Milpitas, Calif., company opened the summer festival in August with a new four-chip solution called NEAT. Faraday Electronics Inc. followed suit with a five-chip set. Then came LSI Logic Corp., which is spinning off an affiliate to market its three-chip solution.

These three companies, along with Zymos Corp., VLSI Technology Inc., and Taiwan's United Microelectronics Corp., are chasing a sizable market. Robert Andrews, technical marketing manager of Zymos, estimates that some 3.5 million PC AT-compatibles based on Intel Corp.'s 80286 central processor were sold this year, with about the same number in the offing for 1988. In addition, some 800,000 personal computers with more powerful 80386 processors will plump out the market, Andrews says.

SPINOFF. For its bid to join the group of PC AT-clone chip suppliers, LSI Logic, Milpitas, formed a new subsidiary, G-2 Inc., and named William O'Meara, a former vice president of marketing and a cofounder of the parent company as its president.

The new company's charter is to identify marketplaces for customizable standard products built with its semicustom tools. And the first such opportunity it identified is, not surprisingly, the PC AT-clone market. At the same time its existence was made known—the company was actually formed about six months ago—G-2 announced it had developed a three-chip set that, in conjunction with 10 peripheral circuits, will reduce by nearly 90% the number of standard, non-memory glue logic circuits now required to build an AT PC clone.

What G-2 is offering to the market is a three-chip solution to integrating the PC AT motherboard, plus a systems controller and an address/data buffer. The chips are fabricated using LSI Logic's 1.5-μm CMOS process; and the firm expects to be turning out production quantities of a 12-MHz version of the chip set by the end of the year, with a 16-MHz version to follow.

G-2 will price the set at $65 in 10,000 unit quantities. At first glance, that appears to make it the price leader: Faraday prices its five-chip set at $95 in quantities of 1,000; Chips and Technologies sells the 12-MHz version of its four-chip NEAT set for $108.90 in quantities of 100. Direct comparisons of raw chip-set prices, however, are misleading because each set needs a different complement of standard devices. "The name of the game is performance and board cost," say Zymos's Andrews. All of the players insist, of course, that their game is the best one for clone-makers to play. *–Bernard C. Cole*

INSTRUMENTATION

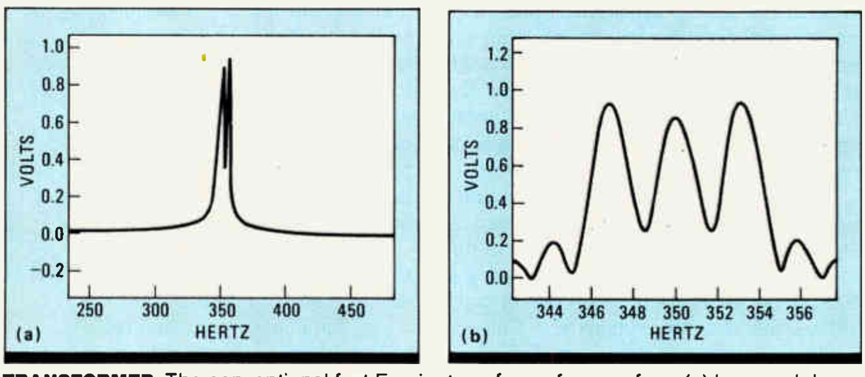
FAST-FOURIER TRANSFORM MEETS ITS MATCH IN CHIRP Z

DANVERS, MASS.

The Chirp Z transform algorithm for evaluating finite-duration phenomena, such as radio signals, is well known in mathematics. Now, for the first time, it has been implemented in an instrument by the Data Precision division of Analogic Corp. The company's engineers did the job by reducing the complex math to an algorithm that can be executed by a Motorola Inc. 68000 microprocessor.

The Danvers, Mass., division has added the capability in the form of an erasable programmable read-only memory to the Data 6100 universal waveform analyzer, which itself was introduced in May. The Chirp Z algorithm provides 65 times greater resolution in time-to-frequency conversions than does a fast Fourier transform, one of today's most popular methods for making the conversion, for the same sampling rate and number of input points (see figure). The accomplishment could make Data Precision a potent competitor for makers of dedicated FFT spectrum analyzers, says Galen Wampler, president of Prime Data, a San Jose, Calif., market analyst.

In resolution, for a sampling period of 1 μs, the frequency of an input signal with 512 data points can be resolved to



TRANSFORMED. The conventional fast Fourier transform of a waveform (a) has much lower resolution than the Chirp Z version, as implemented by Data Precision (b).

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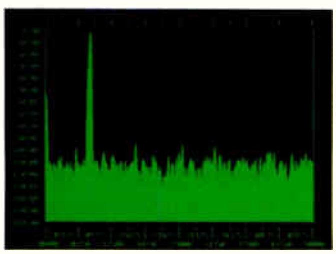

Actual spectral performance of ZAD2846

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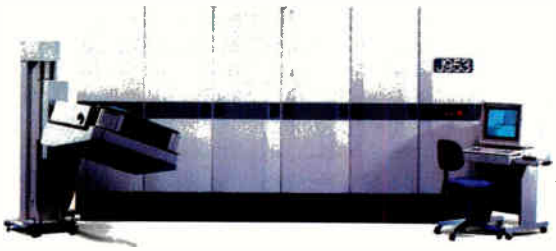

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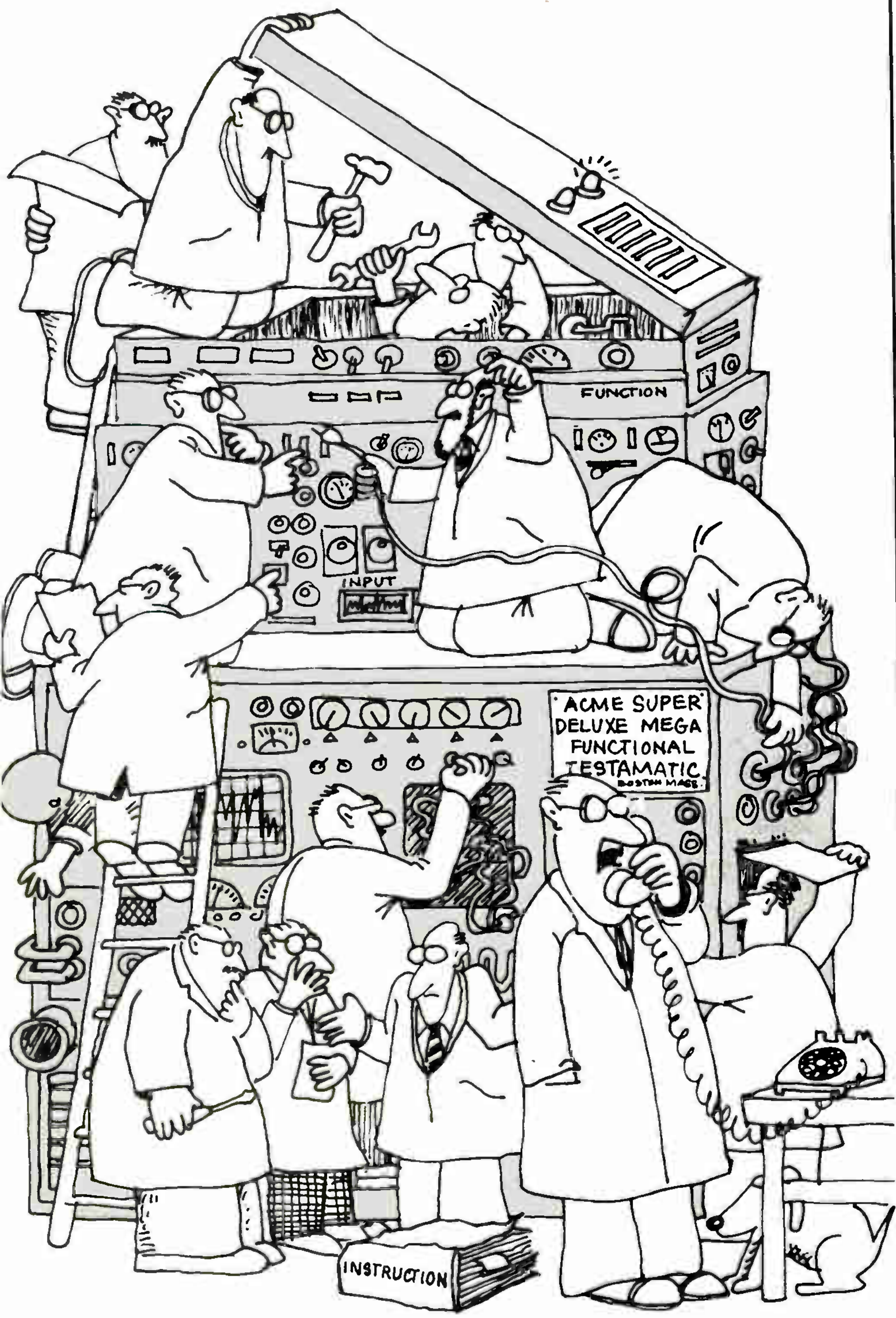

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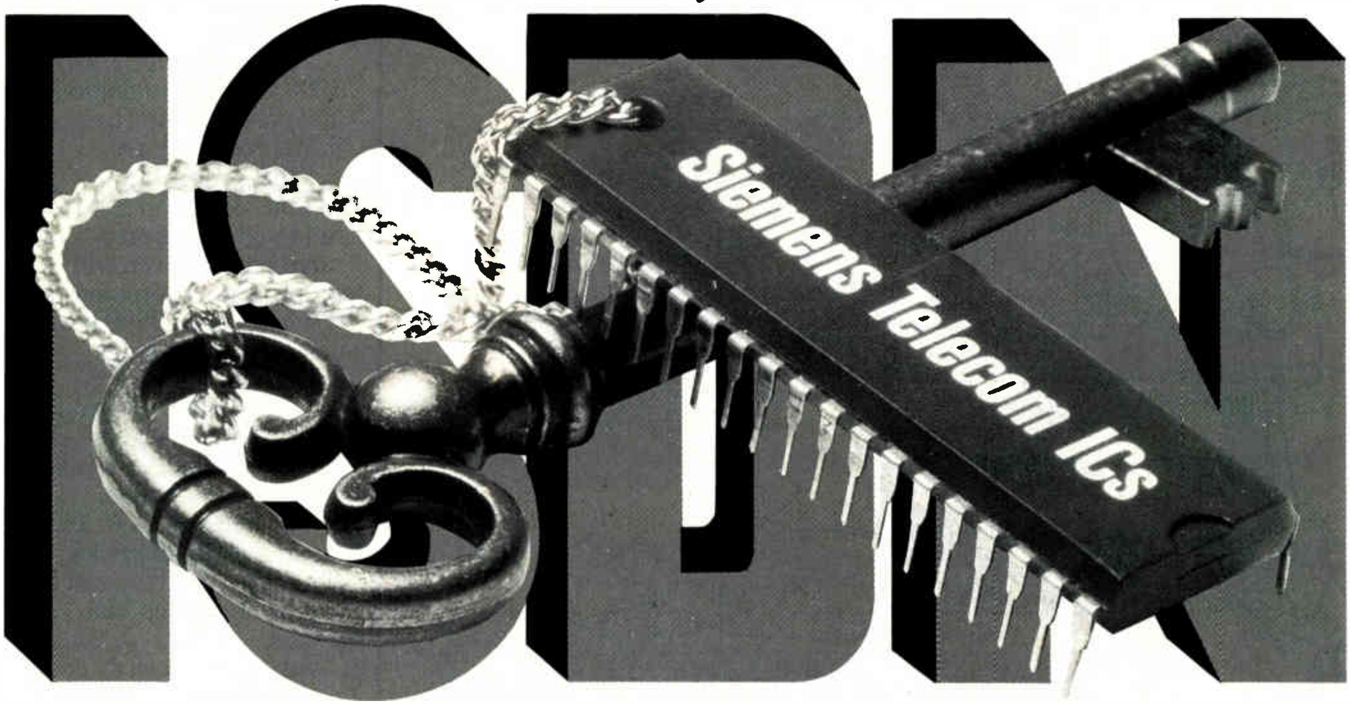

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PROBING THE NEWS

NEW TWIST ON AN OLD IDEA MOVES KODAK DEEPER INTO ELECTRONICS

IT FUNDS STARTUPS, THEN FOLDS SUCCESSFUL ONES BACK INTO COMPANY

by Alan Burdick

ROCHESTER, N. Y.

Question: how does a diversified $11 billion giant move faster and deeper into the electronics industry? One answer: set up an in-house venture-capital group that funds startup operations proposed by employees and then fold these embryonic units back into the parent once they're successful. That new twist on an old idea is just what Eastman Kodak Co. has been trying.

It all started four years ago when Kodak's top managers asked themselves: "How do we make ourselves known as an electronics force?" recalls William Messner, the company's venture portfolio manager. "There are so many people who think of Kodak as a yellow box." The company's answer was to create its own electronics ventures—but at arm's length. This venture thrust is still going through some growing pains, but Kodak managers think on the whole it is well worth the effort.

In-house venture groups are not new, of course. These older "intrapreneurial" operations are being done with varying degrees of success at a handful of electronics manufacturers, including Westinghouse Electric Corp. and Control Data Corp. Kodak's approach, modeled on those plus techniques from the venture-capital world, is part of a "recent trend toward decentralization," says George Stojsavljevic of BIS-Mackintosh, a Boston consultant. The advantage, says Richard Hill, of Tektronix Inc.'s four-year-old Technology Development Co., is that big companies can introduce technologies too uneconomical to address with a large infrastructure. It also affords an early glimpse of the growth potential of the business.

For Kodak, that means trying to keep hands off the venture companies it spins off, allowing them autonomy and keeping them tied only loosely to the parent. The unique aspect of the Kodak effort comes after several years in the marketplace. At that time, the venture is evaluated: if it fits corporate strategy and is commercially viable, it is folded back under the Kodak wing; if not, it's sold or closed.

All of the venture companies that Kodak has funded in the last four years were proposed by employees and more than half of them specialize in electronic technology. So far, one has been closed, two have been merged with Kodak business units, and the rest are still operating as independent concerns (see table).

Total cost has been about $60 million so far. But that doesn't faze top Kodak executives, who believe the venture route is one way for the company to broaden its impact in the electronics industry as it faces stiffer competition and slower growth in its core photographic businesses. "These are future businesses that Kodak wants to be in," affirms market analyst Eugene Glazer of Dean Witter & Co. in New York. "They want the first crack at the market."

One example is Videk, born when Kodak employee Ghassan Kahwati decided he wanted to start a company specializing in machine vision equipment. Kodak offered him backing, and the result is now a thriving three-year-old boasting two products: the Megaplus camera and the RM1000 vision system, both originally designed for use at Kodak.

The Rochester giant's strategy is to seek markets with high growth potential that complement existing Kodak interests, which include office-automation and disk-memory businesses [*Electronics*, May 14, 1987, p. 38]. The new companies specialize in such products as batteries, photo-image-management systems, and molded printed-circuit boards. Many of these, like Videk's machine vision equipment, were originally used in the production of other Kodak devices.

"We had a unique technology to draw from Eastman Kodak," says Videk president Paul Hauler (Kahwati is chief technical officer). "If this had run in normal channels, the bureaucracy would have hampered it."

Kodak considers its most promising venture to be Edicon, a late-1986 startup that recently unveiled its first product line, a photo-image-management system. The Edicon system digitally displays and stores color images—including color prints—transmitted from a video camera, and integrates the data with text and graphics to create photo-image files. Merrill Lynch in New York uses it to handle security and personnel information, and the Los Angeles Police Department is designing a data base of mug shots.

Like the technologies of Kodak's other ventures, Edicon's is aimed at a market too narrow for a large firm to address efficiently, says Robert Tuite, director of new opportunity development. But Kodak's Venture Board of eight senior executives gives it more control over the startup's market di-

WHERE KODAK IS PUTTING ITS VENTURE CAPITAL

1984	
Eastman Communications	Telecommunications software
Videk	Machine-vision products
Ultra Technologies*	High-performance batteries
1985	
Estek	IC wafer-cleaning and inspection equipment
Edicon	Computerized photo-imaging systems
Fastek	Filtration products
Discus	Electronic training products
Beta Physics	Photoconductive films
1986	
Sayett Technology*	LCD overhead projectors
LVT	Digital color-image writer
1987	
KRS Remote Sensing	Remote sensing equipment
Pathtek	Molded printed-circuit boards
K Technologies	Injection-molding product control

*Merged into a business unit of Kodak

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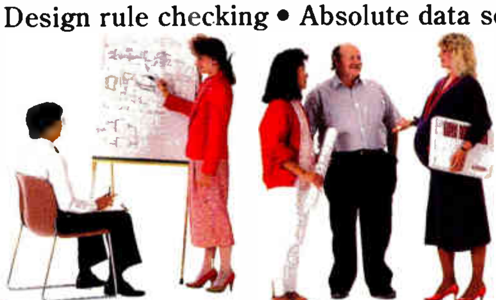

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Circle 49 on reader service card

The outlook for West Germany calls for continued world leadership

Again in 1987, West Germany will keep its front-running position as the world's leading exporter. Sales abroad will remain high, although world trade is slowing, protectionism is increasing, and currency tensions are continuing.

German companies are staying competitive because they have generously invested in new plant and equipment, make high-quality products, use state-of-the-art technology, provide fast service, and have stable prices. On the other hand, the volume of imports will rise as the West German market looks more and more attractive, especially to US, Asian, and other European countries. Foreign firms also

PEP's analog-to-digital converter fits on a Eurocard

With the VMEbus analog-to-digital interface, PEP Modular Computers GmbH of Kaufbeuren introduces a high-performance converter module designed on a single-height Eurocard for the VMEbus. The VADI is a low-cost versatile module assigning digital values to process automation, data acquisition, and monitoring and control systems. It is designed to interface directly to sensors or analog signals and to convert the inputs into standard digital data commonly used in computer systems.

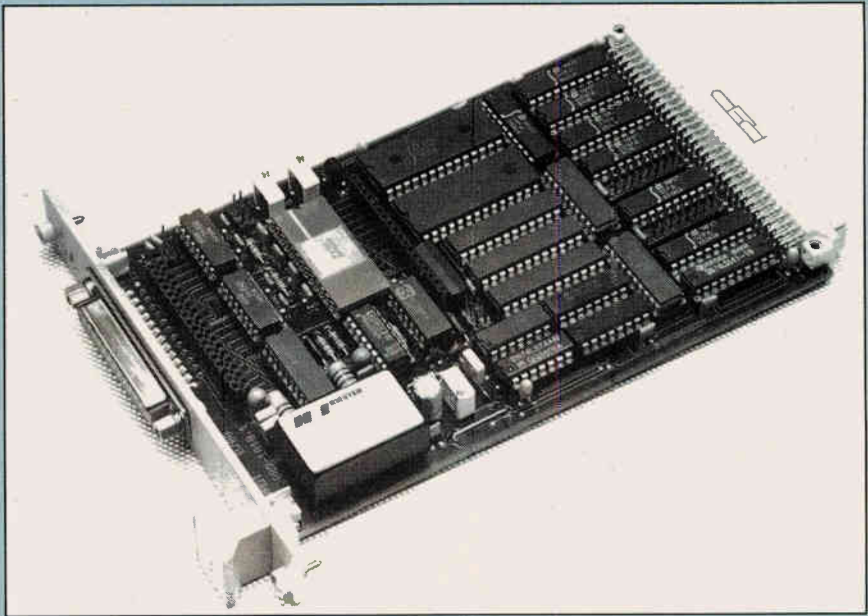
The VADI module consists of 16 single-ended channels for analog input or eight channels of differential mode, jumper selectable. The board contains a standard base module with input voltage protection of ±20 V and three optional piggybacks, software programmable gain, selectable input ranges, and a fully software programmable VMEbus interrupt.

In addition, the board has a 2-Kbyte FIFO for fast on-board data collection and is pin-compatible with Analog Devices Inc.'s series 3B and 5B signal conditioning modules.

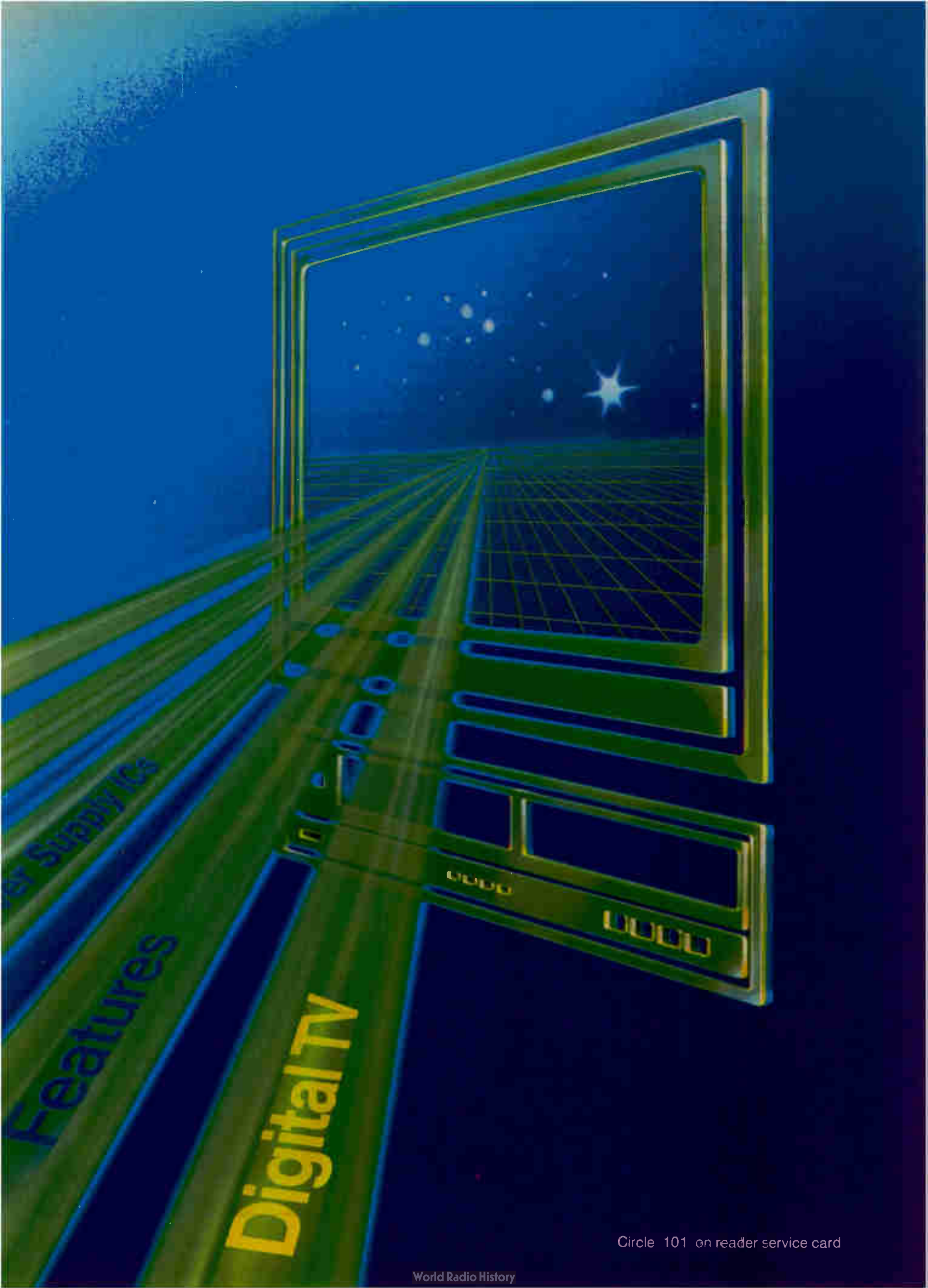
The VADI offers a number of features:

- The VADI piggybacks allow tailoring of the VADI to the application needs and protect valuable investments.
- The FIFOs of the VADI speed up on-board data collection and allow the system CPU to work without many interrupts.
- The VADI's single-height Eurocard design greatly improves reliability and ruggedness and keeps size to a minimum.

The VADI provides a compact and cost-effective solution for industrial applications where analog voltages or currents must be measured with high accuracy in fast sample mode, like in operating machine tools, controlling processes, or observing chemical analysis.

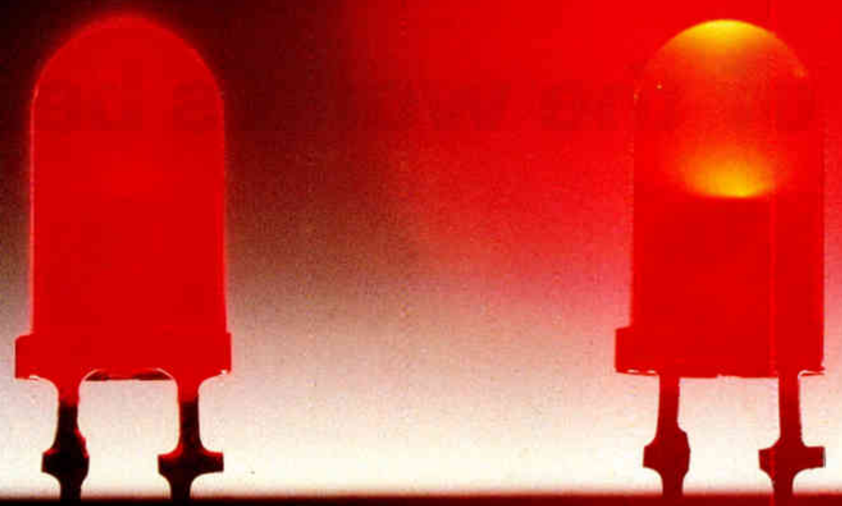


The VADI supports 16 single-ended or 8 differential inputs.



Digital TV
Features
Supply ICs
Circle 101 on reader service card

From now on, ask yourself the following question about LED lamps:



STANDARD?

The standard version of Toshiba's LED lamps has proved itself repeatedly in practice as being just what's needed in most applications. Nonetheless a new generation of Toshiba LED lamps means that you should reconsider your requirements.

OR SUPER?

The brightness of Toshiba's new generation of LED lamps is striking: up to 1,000 times brighter than the standard version. So light, so brilliant that optimum luminosity is guaranted from every viewing angle. As for application, be it stadium or Hi-Fi displays, Toshiba's ultra-bright LED lamps are ideal.

All of this is backed up by Toshiba's know-how, service and production capacity. Find out more by sending us this coupon.

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llance systems

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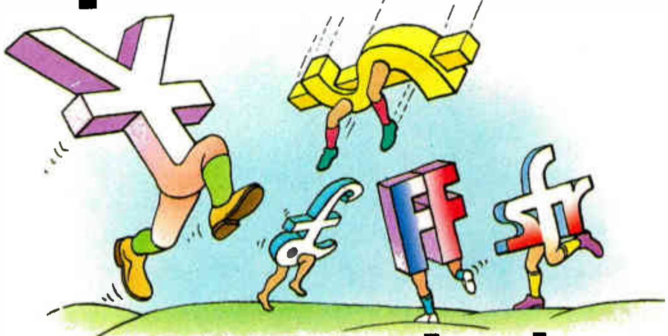
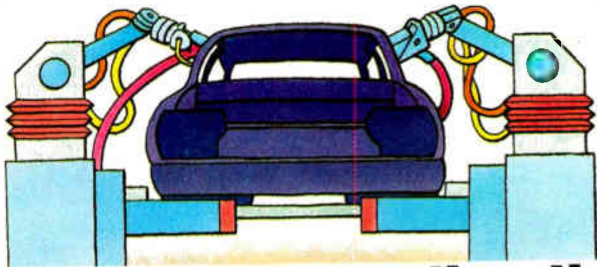
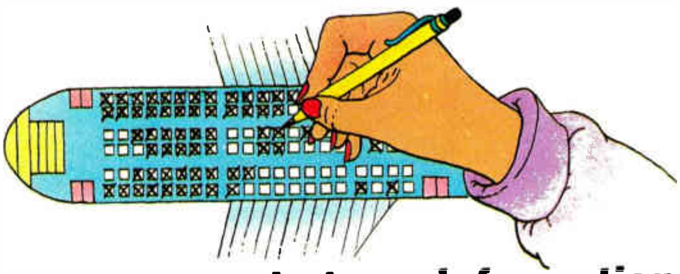
Rapid movement in the stock



markets, today's production figures,



confirmed passenger and freight loading lists,



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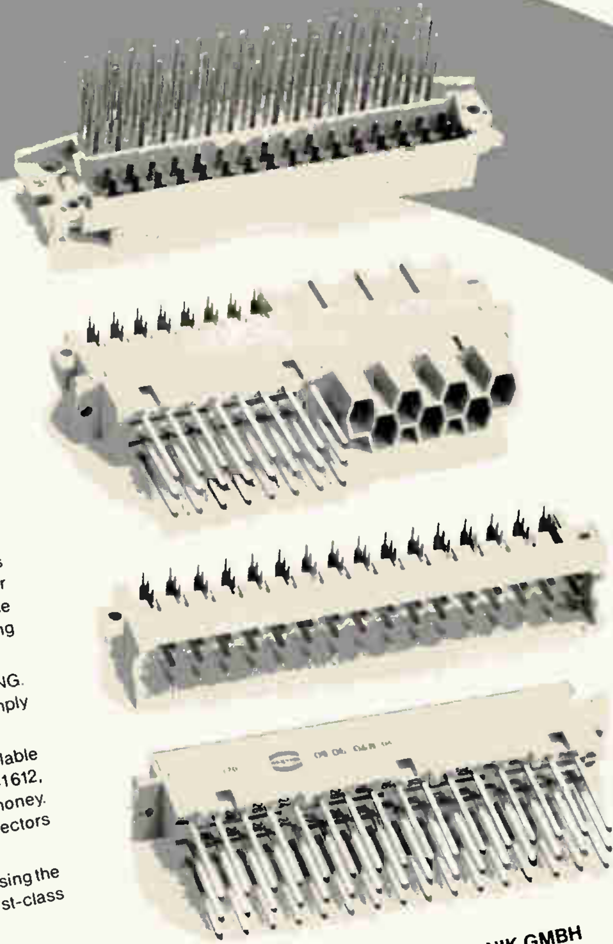

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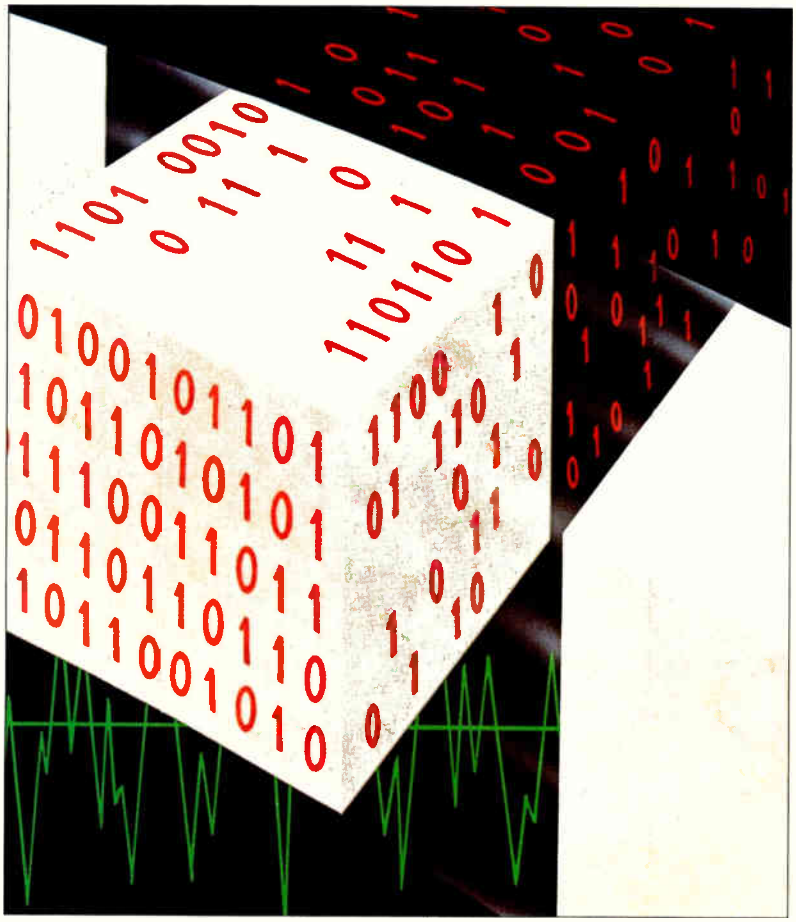

Zoran's vector digital signal-processing chip with 70,000 transistors requires only three instructions to do a 1,024-point fast Fourier transform in 2.4 ms.

Zoran Extends The Range Of Monolithic DSP Applications.

"A speedy new single-chip contender is getting set to make a splash in DSP. Zoran's ZR34161 uses vector-handling techniques to gulp down blocks of data, rather than picking off a single data input at a time. Vector processing alone is a big speed booster, and Zoran enhances it with embedded signal-processing algorithms that radically pare down system overhead.

The company's 16-bit CMOS VSP is the first monolithic signal processor to utilize the powerful vector-handling techniques employed for scientific data processing in large vector computers and minicomputer array processors..."

Excerpted from an exclusive article in the July 24, 1986 issue.

McGraw-Hill **Electronics**

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Circle 114 on reader service card

RISING STAR.

The instrument cards from Wavetek plug vertically into a VMEbus backplane and are controlled by the microprocessor.

Wavetek's Card-Based System Could Set An ATE Standard.

"A young contender is pushing its way to the forefront of the emerging market for instruments on cards. The 680 system from Wavetek Corp. uses cards in a package that can replace a rack of conventional instruments—and Wavetek's approach is already making a strong bid to become a de facto standard in its market.

Wavetek has been joined by Racal-Dana and Datron in a campaign promoting the 680's design as a standard for high-performance, instrument-on-a-card systems. If successful, it could make Wavetek a major player in the instrument-on-a-card segment of the ATE market—particularly the military segment, where growth has been hampered by a lack of standards..."

Excerpted from an exclusive article in the April 16, 1987 issue.

Electronics

THE LEADER IN NEW TECHNOLOGY COVERAGE

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Why don't these new measurement instruments have any control elements?

Now, you can skip unweldy operating procedures when using measurement instruments. Why? Because Siemens has developed new measurement instruments that cooperate with personal computers over an IEEE 488 bus.
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INTERNATIONAL PRODUCTS

SIGNATURE ID SYSTEM DELIVERS TOP SECURITY AT HALF THE COST

USING BIOMETRIC VARIABLES, IT EQUALS FINGERPRINTING FOR ACCURACY

The Sign/On signature verification system from Alan Leibert Associates Ltd. boasts identification accuracy that equals fingerprint readers—good enough for military applications—but costs just half as much. It also has the advantage of being more socially acceptable than fingerprinting, which means it can be integrated into a much broader range of applications, such as retail sales.

Sign/On foils would-be forgers by statistically evaluating 13 biometric characteristics of a signature, instead of measuring the shape of the written characters. Because it bases pass/fail decisions on a statistical analysis, users can make the system more or less strict, depending on its application. In its most stringent mode, suitable for military-security applications, Sign/On has a false rejection rate of 1%. In less stringent applications, such as retail sales, the rate is 5%. Testing to determine the false acceptance rate is not complete, but should be about 2%, the company says. Fingerprint-based systems can have false rejection and acceptance rates as high as 10%.

PROGRAMMABLE. Sign/On can tighten pass/fail evaluations for military applications and loosen them for other uses such as retail sales.

The system costs £850 ($1,360 U.S.) and issues a pass/fail evaluation in 3 seconds. Fingerprint readers generally take 3 to 5 s and typically cost $3,000 or more.

THREE MODULES. Sign/On uses Zilog Corp.'s Z80 microprocessor and the Pascal programming language. The system consists of a low-profile 8.5-by-11-in. digitizing tablet on which the user signs his name with an electromagnetic pen, plus a control unit that can store up to 100 signatures. This control unit also houses the power supplies and the communications interface. The controlling computer can be an IBM Corp. Personal Computer or compatible, a minicomputer, or a mainframe, depending on the application. The data stream can be encrypted as a further security option if required.

Sign/On's biometric data base is proprietary, but it includes the amount of time that the pen spends in the air between surface contacts, the pen's acceleration and deceleration, and the total amount of time taken to complete the signature.

"It is relatively easy for a forger to duplicate a signature visually," says Alan Leibert, Managing Director of the Pinner, Middlesex, UK firm, "but it's virtually impossible to duplicate the way in which a signature is made." He adds that using a signature as a sure means of identification is also "socially acceptable," making the technique more attractive than, say, fingerprinting to a wide range of markets.

"The allowable parametric spread of the 13 characteristics that are measured during the making of a signature can be narrowed or widened, depending on the application," Leibert says. "For example, the parameters could be left wide when the system is being used for retail transactions, but could be narrowed if the system is used to protect highly sensitive data."

Although the end-user's identification system will vary somewhat, depending on the OEM's configuration with peripheral hardware and software, Sign/On's general operation begins with an authorized user registering his name—using the electromagnetic pen—and signing several times on the digitizer tablet. The signature is then stored in a statistically based template in a numbered reference file either in the system itself, on a computer, or on an external mechanism such as a smart card or a magnetic-strip card. When the user next needs to access whatever Sign/On is protecting, he claims identity by submitting a numbered credit card, for example. This causes the appropriate signature template to be loaded. He then signs his name, and within three seconds the newly written signature is checked against the one stored in the reference file and verified.

Sign/On was conceived and developed in the UK by Leibert's development team, but it will be manufactured in the U.S. by Signify Inc. of Columbia, Md. Signify will also be responsible for marketing to systems integrators in North America.

MASS MARKETS. Leibert forecasts applications in mass-production markets, such as financial and retail sectors, and in the computer industry. "Banking organizations and electronic-funds-transfer equipment manufacturers have been exploring signature dynamics, fingerprinting, and other biometric identification devices as being potentially more reliable alternatives to memorized personal identification numbers and passwords," he says. "Sign/On has been designed to work with EFT applications, such as share transactions and home banking."

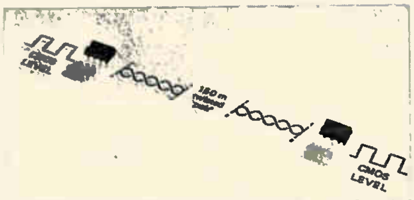
Other potential markets include retail-store chains that issue their own credit and charge cards and major international credit-card companies, such as Visa and MasterCard; it may take two or more years for them to adopt standards, though, says Leibert.

He expects to succeed where other purveyors of signature verification systems have failed on two counts: computer connectivity and price. Others failed because "they did not offer interfaces to other computer products," he says. "Sign/On has been designed to make it easy for manufacturers to systemize the

THE COMPLETE COMPONENT COMPANY

Philips Electronic Components and Materials Division, 5600 MD Eindhoven, The Netherlands

Universal driver/detector pumps data directly across 150 metres of twisted-pair lines



Our SAA1045 universal driver/detector IC transmits data directly across twisted-pair lines up to 150 m long – this is the farthest distance covered by a currently available circuit, most existing drivers being limited to a few metres. As well as connecting directly to our D²B (digital data bus), the CMOS SAA1045 can implement other bus protocols with data rates up to about 1 Mbit/s.
The driver/detector suits office, home, and factory applications, and can be used to connect up all the electronic circuits in a car. The bus provides for a response time within 2 ms, and the twisted-pair wire format makes it inexpensive to implement.
Together with a microcontroller and a bus controller, the SAA1045 provides a serial transmission link between multiple stations (several devices can be parallelled to implement parallel buses). The circuit is small, coming in an 8-pin DIL or SO package, yet contains the detector, driver, digital filter, and analog circuits.
In D²B systems, the SAA1045 can be cascaded to span any distance and works at rates up to 100 Kbits/s. This can be increased to about 1 Mbit/s in non-D²B systems by disconnecting the on-chip digital filter.
The IC can work in single-master I²C bus systems, extending the length of this bus to 20 m. The I²C bus performs a similar function to the D²B, but for ICs within a piece of equipment. It is a two-wire serial link that transmits data across a few metres at speeds up to 100 Kbits/s.
The SAA1045 has a power-on reset circuit for proper initialization. When active, the IC dissipates a maximum of 300 mW from a 5 V supply and works between −20 and +80 °C.

193

Philips announces sampling of first advanced CMOS logic devices featuring new pinning concept

Philips is now sampling the first advanced CMOS logic (ACL) ICs to selected customers. The first devices of the planned family are the 74AC/ACT11002 quad 2-input NOR gate, the 74AC/ACT11020 dual 4-input NAND gate, the 74AC/ACT11027 triple 3-input NOR gate, the 74AC/ACT11030 8-input NAND gate, the 74AC/ACT11074 dual D-type flip-flop with set and reset. Type numbers starting 74AC are for CMOS input-level logic operation and those with 74ACT are for TTL input-level operation.
The devices combine very high speed and high output drive currents comparable to the most advanced TTL families currently available. As an illustration of performance: propagation delay for the 74ACT11002 is just 3,5 ns and the output current is 24 mA.
The devices feature a new concept in logic device pinning: the supply voltage and ground pins are placed in the centre of the packages. Inputs surround the supply pins and outputs the ground pins; control pins are strategically located at the ends of the packages. The new configuration eliminates various faults as lead lengths are shorter and inductance effects less. The ACL family therefore enables designers to implement simultaneous switching applications while allowing maximum performance to be obtained.
Operating temperature range for all the devices is -40 to +85 °C. All the devices in the ACL range will be available in small-outline packages for surface mounted assembly or in dual-in-line packages.

194

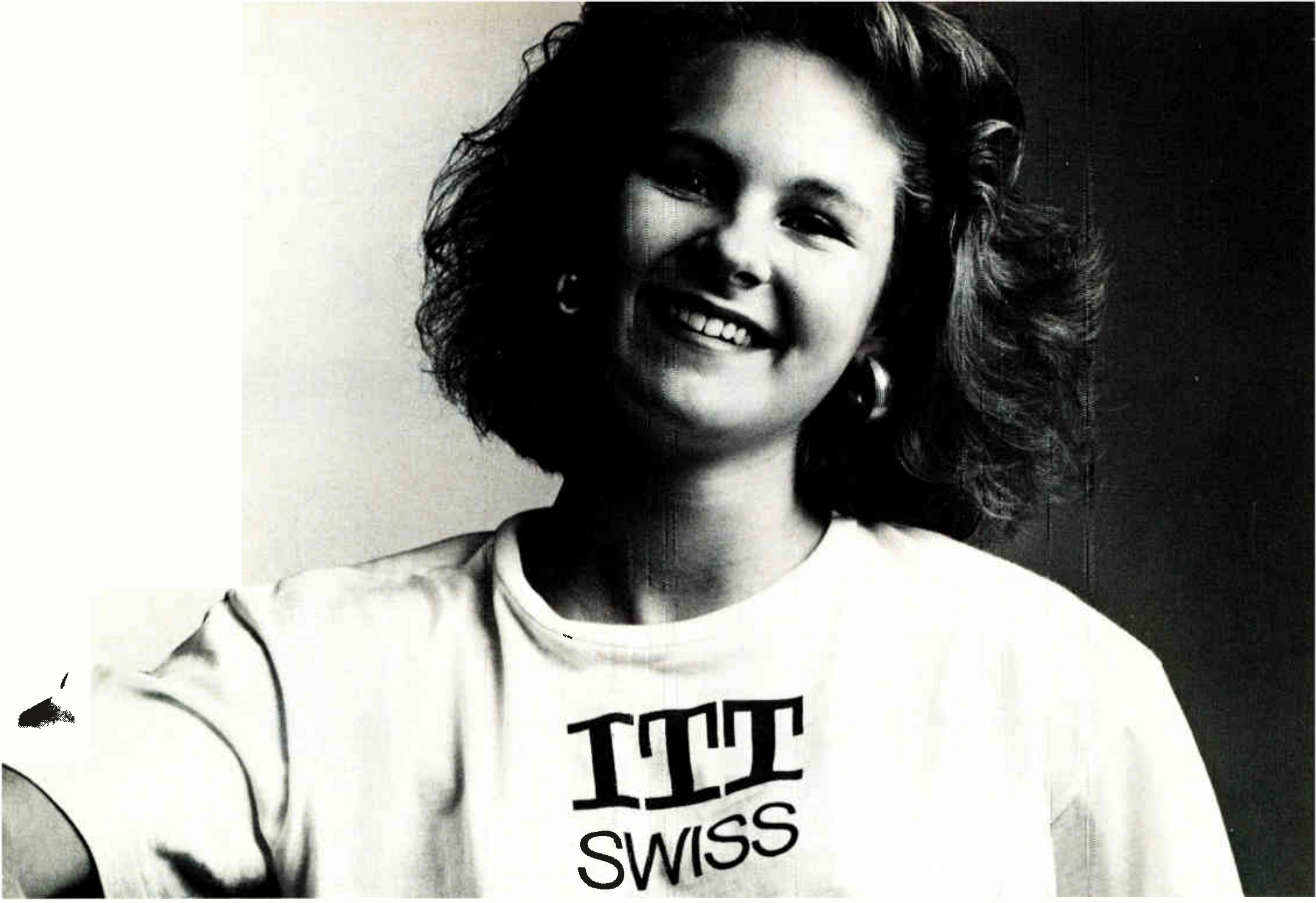
Precision SMD resistors boast low temperature coefficient plus 1 % tolerance

Philips is announcing a new series of precision SMD (surface mounted device) resistors with a specification based upon that of conventional 1 % leaded resistors. Besides having a tolerance of ± 1 %, the RC-02 series features a temperature coefficient of ± 50 ppm, a stability of below ± 0,25 % during soldering, and a stability of ± 0,5 % after 1000 hours operation.
Until now, competitors could normally only supply SMD resistors with 1 % tolerances by rigorous selection of 5 % types. However, these were not true precision resistors, since the other elements of the specification did not comply with the 1 % tolerance on initial resistance value (the temperature coefficients, for example, are 100 ppm and above). Manufacturers needing precision types for surface mounting had to turn to MELF resistors. Although these meet the highest requirements all through the specification, they have several disadvantages when compared with SMD resistors, not least of which is the difficulty of handling them on pick-and-place machines.
The tighter tolerances of the RC-02 series stem from improvements in the materials and manufacturing process of the resistors.

The resistors have a maximum dissipation of 0,125 W, and withstand r.m.s. voltages up to 200 V: temperature range is from −55 to +125 °C. The resistance range goes from 100 Ω to 1 MΩ. They are supplied in bulk, or on 8 mm paper or blister tape, and suit all soldering methods.

195

PHILIPS



THE ONLY DIFFERENCE BETWEEN AN ITT SWISS RELAY AND AN ALCATEL SWISS RELAY IS THE NAME.

But you probably already knew that. ITT Swiss relays now have another name on the front. You can't miss it. The name Alcatel Swiss is in the same place where ITT Swiss was.

So, what's different? Not much. And definitely less than our competition would have liked.

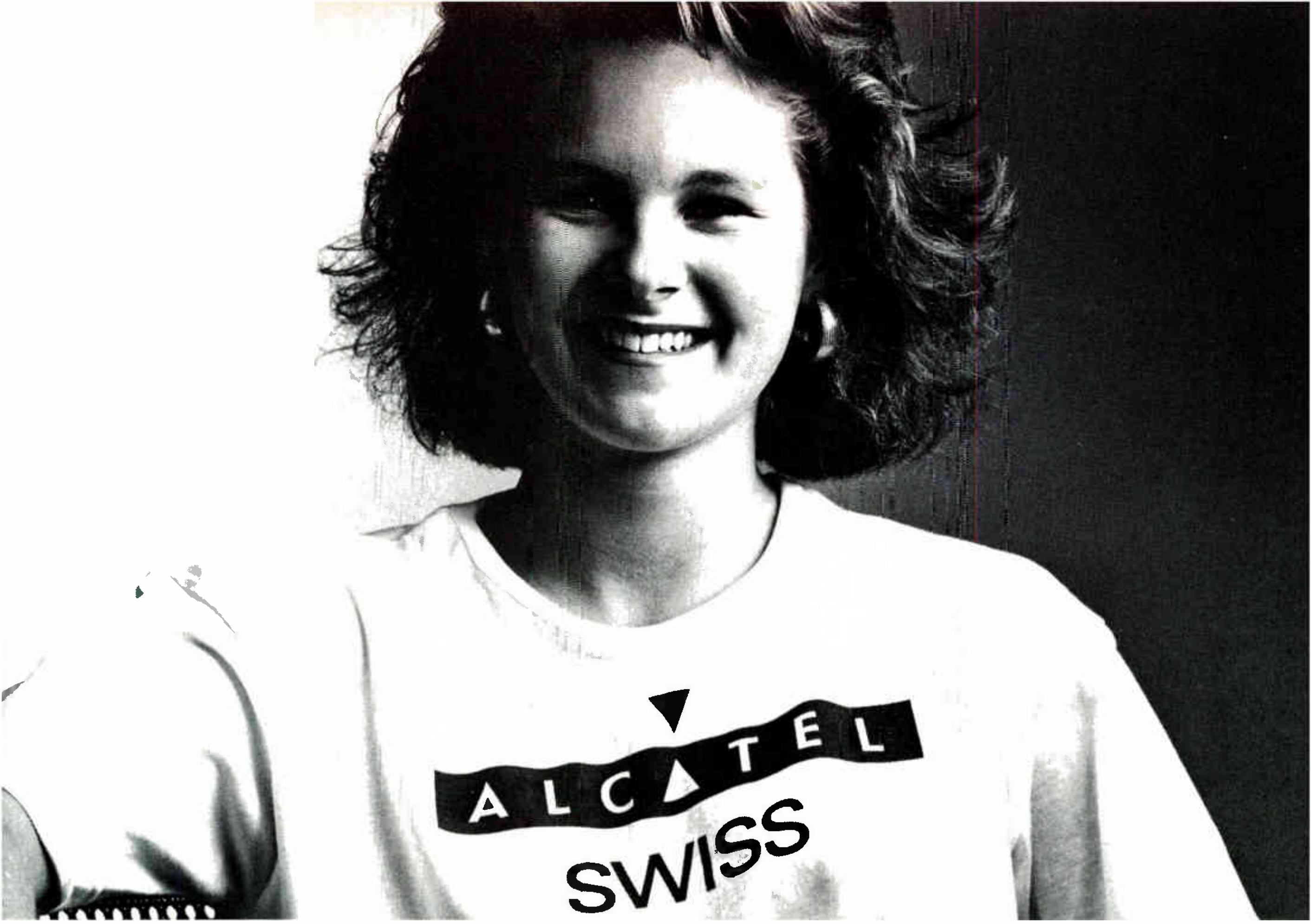
Some details: Alcatel: Despite its youthfulness, this European association of enterprises has become quite well known.

Alcatel's goals have always been set quite high, a fact which is not really surprising when we consider the competition from America and Japan—not to mention that from the Far East.

So it must be clear that our competence in the manufacture of relays is a matter of great importance in this situation. We can offer a list of plus points which will continue to be available in the future, of course.

Indeed, these plus points are precisely those points necessary to meet the competition of today and tomorrow. Therefore they will be changed very little.

Our relay customers know what we mean. If you are not one of them, then this information will be even more important for you. Allow us to make a few points:



Dr. Juchli 780 S1

PZ Relay: a wonderful example of our pioneering in this field. This was the first relay which could be soldered directly into P.C. boards. This is the only series in the world with a choice of 2, 4 or 6 changeover contacts.

SM Relay: Another typical pioneering effort of our relay laboratories featuring extremely flat profile and an extremely quiet operation. Completely plastic coated, this unit exhibits (in contrast to the competition) exceptionally good anti-shock and anti-vibration characteristics as well as resistance to tropical and wet conditions.

MT Relay: a monostable relay that has no peers. Non-polarized. Suitable for very high packing density. Compatible. Never needs re-adjustment. A guaranteed 10 million changeovers under dry conditions. Functionally guaranteed within a temperature range of −55 to +70 degrees centigrade. Failure ratio guaranteed to be under 0,5% over the lifetime of the relay. Can be supplied for coil voltages up to 48 V and 150 mW capacity!

We are sure you will agree that is an impressive list of relay plus points.

Now it should be clear just why, except for the name, it is the same old range of products. After all, they are still the latest state of the art.

Everything you have always wanted to know about relays but didn't know where to find the information, has been compiled in the new STR Relay Hondbook. A competently written indispensable practical aid for everyone who wants to be on top of everything in the world of relays. We would be happy to send you one—free of charge, of course.

Company

Address

Responsible Party

EW 10/1

Standard Telephon und Radio AG, CH-8055 Zurich
Friesenbergstrasse 75, Switzerland

ALCATEL

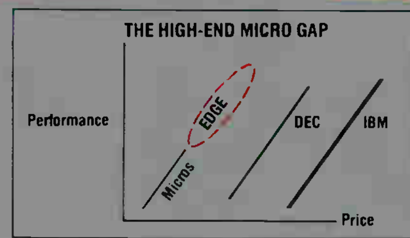
STR

Circle 53 on reader service card

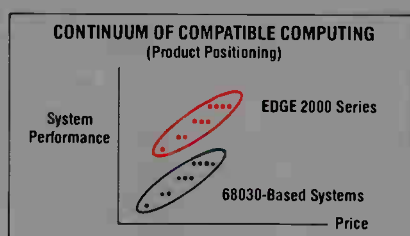
68000™ FAMILY UPDATE NO. 2

OEMs CAN NOW OFFER HIGH-END, LOW-COST 68000 FAMILY COMPATIBLE PRODUCTS WITH 16 MIPS UNIPROCESSOR PERFORMANCE

By any measure, the 2000 Series VME™ board set recently unveiled by Edge Computer represents a quantum leap in 68000-compatible computing. Designed to fill the microprocessor high-end performance gap, the EDGE 2000 has driven performance costs down to about $1K per MIPS (OEM quantities). The 2000 Series is available in a VME 3 high eurocard, 4 board set for easy product integration.



The EDGE 2000 is actually a CISC machine that operates with RISC-like efficiency. The specs are impressive. The uniprocessor version of the EDGE 2000 delivers 16 MIPS sustained performance and 60 MB/sec I/O bandwidth. At 1.4 cycles per instruction, the EDGE 2000's AIT (average instruction time) is lower than any other computer on the market today. Quad configurations of the powerful 2000, which supports scalable, transparent multiprocessing with one to four CPUs, are rated in excess of 56 MIPS sustained performance. The modular 2000 Series is based on a proprietary high-speed EDGEbus structure that offers 64 bit, 128 MB/sec parity protected transfers. Global memory can range from 8 MBytes to 1 GByte. Up to four standard or proprietary secondary I/O busses can be supported through dual I/O controllers. In spite of its incredible price/performance characteristics, the EDGE 2000 features a very small footprint (17″W x 29″H) to fit in a normal office environment.



EDGE SOLVES COSTLY SOFTWARE PORTING AND ARCHITECTURAL COMPATIBILITY PROBLEMS

Those OEMs and System Integrators with 68000-based products looking to develop high-end products outside of the 68000 family must overcome a number of costly, lengthy software compatibility obstacles. Porting the operating system, utilities and application software for target hardware, designing I/O interfaces and compilers are among the most formidable. The ongoing costs for support and maintenance of two architectures are equally important considerations. 68000-compatible products developed by Edge Computer let OEMs and System Integrators move ahead with a high-end compatible 68000 architecture to eliminate substantial software porting expenditures while still maintaining architectural compatibility.

EDGE COMPUTER FORMS SWISS SUBSIDIARY

Edge Computer Corporation has formed a European subsidiary in Lausanne, Switzerland. The new company was established to capitalize on the rapidly growing European demand by OEMs, System Integrators and Value-Added Resellers for compatible high-end Motorola 68000-based products. The subsidiary will be headed by Heiner Krapp, vice president of international operations.

EDGE COMPUTER

Compatible With Your Future

For more information, contact Pamela Mayer, Edge Computer Corporation, 7273 E. Butherus Drive, Scottsdale, AZ 85260, 602/951-2020. European Sales Office contact Heiner Krapp, 5, Avenue des Jordils CH 1000 Lausanne 6 Switzerland, 41-21-275315.

Circle 54 on reader service card

FERMENT IN MICROCONTROLLERS

NEW OFFERINGS, NEW PLAYERS STIR UP THE COMPETITION

Most of the action is at the high end; while these 16-bit parts got off to a slow start in the early 1980s, they're now rocketing along at a 90% growth rate

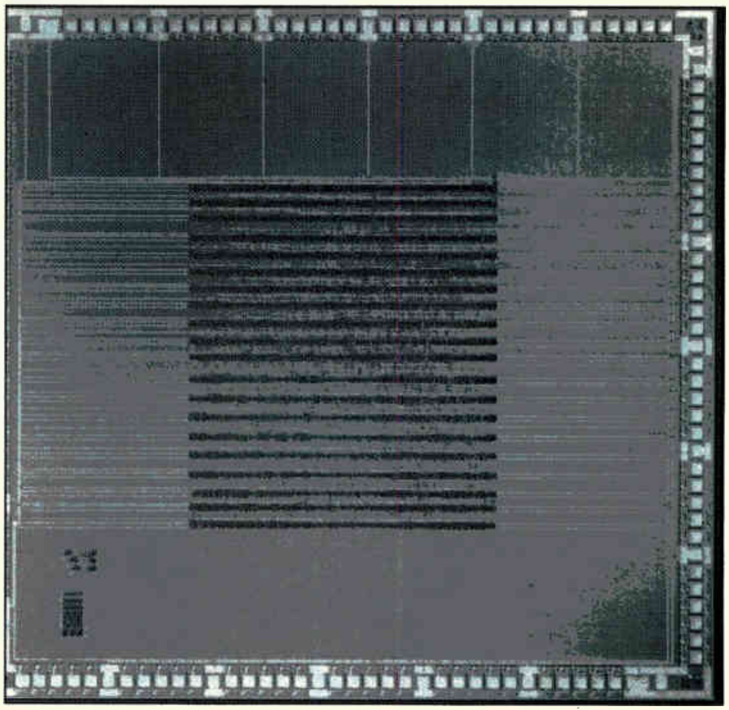
by Bernard C. Cole

The market for microcontrollers is going like a house afire as the number of applications explodes for these cost-effective devices. Semiconductor vendors from around the world, as a result, are investing major resources into a potpourri of new and improved products. And they are developing a wide variety of new strategies and technologies to set off their new chips from the crowd and grab as much market share as they can.

Worldwide sales of single-chip controllers now stand at 500 million units worth \$1.6 billion; after a gradual rise to 555 million units and \$1.77 billion in 1988, the market will begin to overcome design-in lag and could shoot to 1.25 billion controllers worth almost \$3 billion by 1991, estimates Dataquest Inc. of San Jose, Calif.

The most exciting segment of the market is the high end, the 16-bit parts for computationally intensive real-time jobs. This segment got off to a slow start in the early 1980s but is now rocketing at a compound annual growth rate of over 90%, and the number of alternatives the customer has to choose from is expanding quickly. Until last year, Intel thoroughly dominated the 16-bit microcontroller market with its 8096; the only other major competitor was Mostek's MK68200. Since then, however, 16-bit chips have appeared from Harris, NEC, and National Semiconductor. Texas Instruments is expected to jump in, and it already has some design wins for controller applications handled by its 320-series digital signal processor. Intel is looking to defend its market position with the new 80C196 (see p. 59).

But the market for the older 4- and 8-bit microcontrollers is not being neglected; its growth prospects are still considerable. There are many more players already working this territory, so they are scrapping it out, looking for ways to reduce the cost, speed up the programming turnaround time, and enhance both the performance and flexibility of their offerings. There is a trend toward parts optimized for particular applications and market segments, both in terms of hardware features and modified instruction sets. There is also a growing movement toward incor-



1. FORTH CORE. Harris Semiconductor's reduced-instruction-set core cell for microcontrollers is optimized for executing software written in Forth.

IT'S DESIGN-IN TIME FOR ISDN: OEMs FIND THE GOING ROUGH

Too many architectures with incompatible interfaces make mixing chip sets difficult; to get designs moving faster, chip makers are turning out more evaluation boards

by Jack Shandle

The gestation period is over for the Integrated Systems Digital Network. Labor pains have begun, and much of the agony is being suffered by computer designers more familiar with modems and networks tailored to the computer environment than with telecommunications.

ISDN confronts them with the telecommunications world's high voltages and complex protocols and interfaces. To compound the problem, over the past two years chip makers have fielded ISDN chip sets implemented in differing architectures. While ISDN establishes standard interfaces at certain levels, chip-to-chip communication—that is, communication between the chips built for the standard interfaces and the rest of the electronics in the equipment in question—remains nonstandard. That's a dilemma for original-equipment manufacturers, who must ponder which architecture is best for their applications.

The array of options has helped keep OEMs waiting on the sidelines for a clear choice among chip makers' families to emerge. So now chip makers are beginning to field evaluation boards and development software in the hopes they will attract designers. Chip offerings have also continued; for example, AMD is introducing an ISDN controller chip that takes on many functions from the host processor (see p. 66).

The stakes are considerable, now that ISDN is starting to take off. The use of digital switches in local exchanges in the U.S. is a prerequisite for the implementation of ISDN, and Ovum Inc. predicts that will grow from a 25% base in 1987 to 64% in 1995. With the exception of France, where 55% of local exchanges are already digital, Europe will go digital at a slower rate, says the Princeton, N.J., market researcher. By 1995, Germany and Italy will have converted 50% of their switches, and France 95%.

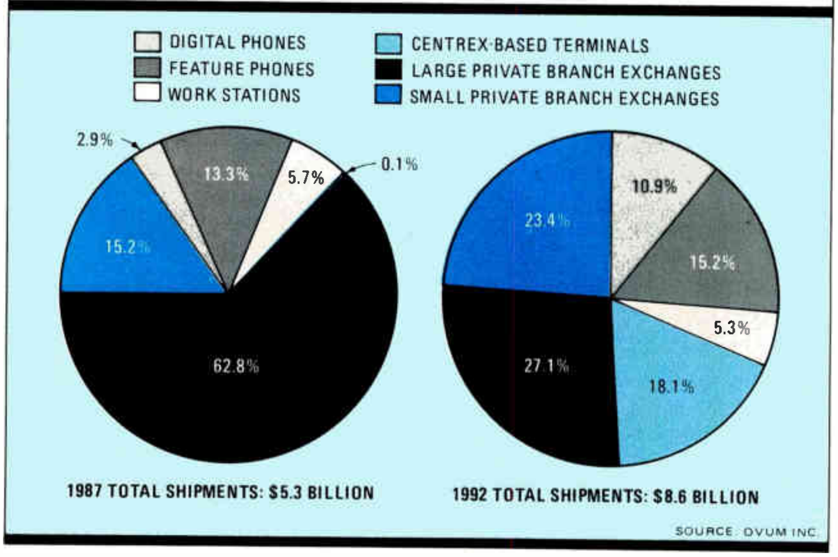
The swing to digital exchanges will pave the way for steadily growing markets for ISDN products. Ovum projects an $8.6 billion U.S. market for ISDN products in 1992—including feature phones, work stations, and private-branch-exchange equipment—up from $5.3 billion in 1987 (see table, right). It predicts that the European market will grow from $1.1 billion in 1987 to $4.1 billion in 1992 (see table, p. 64). Japan is seldom included in ISDN market projections: it has opted to take its own route to digital communications, and Japanese companies have not participated in ISDN standards making.

Designed to bring digitized voice and high-speed data directly to a user's desk, ISDN sets standards for two services: A 192-Kbit/s basic-rate service is for small companies and individual subscribers; and a primary-rate service of either 1.544 Mbit/s in the U.S. or 2.048 Mbit/s in Europe typically will serve *Fortune* 500 companies. Each service level entails its own family of interfaces.

In basic-access service, the 192-Kbit/s channel divides into two data channels—designated B channels—and one 16-Kbit/s signal channel—designed the D channel. The division point is called the U interface. The link between the customer's phones and terminals and his internal distribution is called the S interface.

In the primary-access service, the S_1/S_2 interface provides the connection between the network and the subscriber's line, and the T1 interface provides the connection between the individ-

HOW THE U.S. ISDN MARKET WILL GROW



AMD'S $18 CONTROLLER CHIP EXECUTES ISDN'S KEY PROTOCOL

Its other jobs include linking non-ISDN terminals and acting as bus arbitrator

by Jack Shandle

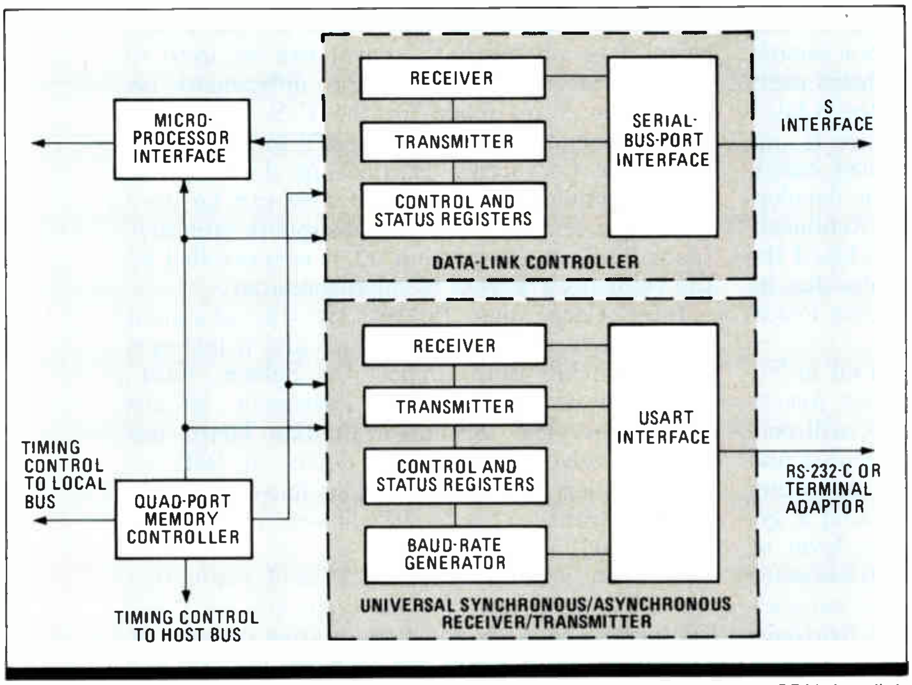
Locking a complex telecommunications protocol into silicon at a time when the standards for the Integrated Services Digital Network are still evolving can be a tricky business. But Advanced Micro Devices Inc. has pulled a price-performance rabbit out of its hat with a chip sample-priced at $18 that delivers big dividends by executing ISDN's key protocol, plus integrating components of an ISDN terminal.

The Am79C401 Integrated Data Protocol Controller (see fig. 1) handles the protocol that establishes, maintains, and terminates data-link connections. It also integrates a universal synchronous/asynchronous receiver/transmitter as a link to non-ISDN terminals via an RS-232-C port. Still another functional module—the dual-port memory controller—acts as a bus arbitrator in shared-memory, multiple-processor applications—allowing system designers to use low-cost static random-access memory instead of dual-port memory.

The chip's primary mission, however, is executing selected portions of ISDN's still-evolving LAPD (Link Access Procedure-Version D) protocol. Its modular architecture accomplishes that goal efficiently, reducing processing time by up to 40%, compared to systems in which the system's microprocessor executes LAPD completely in software, says Terry Lawell, ISDN strategic development manager of the Sunnyvale, Calif., company. By offloading the processor, the 79C401 gives it more time to handle other aspects of LAPD that could change as standards committees complete their work and are therefore better handled in software. It implements handshake procedures, checking data validity, and monitoring the bit stream for special characters that require the microprocessor's intervention.

Some competing chip makers have put more of the protocol's functions on-chip, but these devices cost up to five times the 79C401's sample price. AMD contends complex chips costing $50 to $100 are saddling system developers with undue risk because the LAPD protocol is still evolving.

LAPD is a subset of the International Organization for Standard's HDLC (High-Level Data Link Control), which in turn was derived from IBM Corp.'s SDLC (Synchronous Data Link Control). These protocols manage network data in numerous ways, including frame delimiting, error correction, addressing, and signaling. Since the protocols are similar, the 79C401 also supports applications using pre-ISDN protocols such IBM's SNA (Systems Network Architecture), AT&T's DMI (Digital Multiband Interface), and the CCITT's X. 25 protocol.



1. MULTIPROTOCOL. AMD's 79C401 controller chip was designed to execute the ISDN data-link protocol, but it also can handle SNA, X.25, and other bit-oriented protocols.

In ISDN applications, the 79C401 supports data calls at the S-interface—the point where computers and dumb terminals connect to the ISDN environment. S-interfaces consist of two 64-Kbit/s data channels—called B channels—and one 16-Kbit/s signaling channel called a D channel. The 79C401 can support multiple logical connections on one B channel. Two chips can be used in parallel to support both B channels.

Situated at the chip's doorway to the S-interface, the data-link controller does the on-chip protocol work. To reduce the number of microprocessor interrupts and their latency time, incoming data is parceled into status and control registers and then stored in a 32-byte-deep first-in, first-out memory. In the process, the hardware checks the validity of the data by handling error recognition procedures, flag recognition and generation, and abort recognition and generation. "Many parts out there today spend 30% to 40% of their time trying to find out what shape the data packet is in," says Lawell. One reason is that these chips must interrupt the processor more frequently for instructions that will help determine the data packet's status. The 79C401 handles these duties by executing fewer instructions from the processor.

The data-link controller operates in multiplexed or nonmultiplexed modes. In the multiplexed mode required by ISDN, it interfaces with AMD's Am79C30 digital subscriber controller or Am79C32 data controller (fig. 2), providing access to any of the 64-Kbit/s time slots on the 192-Kbit/s serial bus. The 79C30 or 79C32 can then assign time slots to any of the 64-Kbit/s channels on the S interface. In nonmultiplexed operation, the 79C401 supports full-duplex transfers up to 2.048 Mbit/s.

The chip's USART executes a superset of the industry-standard National Semiconductor Corp. 8250 UART used in Hayes Corp.'s SmartModem and in IBM Corp.'s Personal Computers. It operates in full-duplex mode up to 56 Kbit/s with a baud rate set internally by external clocks—making it a good match for integrating non-ISDN terminals into a network. A bonus feature to save software developers time is a special-character recognizer that checks for command characters arriving in the USART's 4-byte FIFO that require intervention by the microprocessor. Up to 127 character patterns can be programmed into the chip.

Special characters activate a status-tracking circuit so the character can be identified when it becomes resident in the 79C401's output data register. This saves the designer the effort of writing software to locate special characters and offloads the processor because it doesn't have to execute the software.

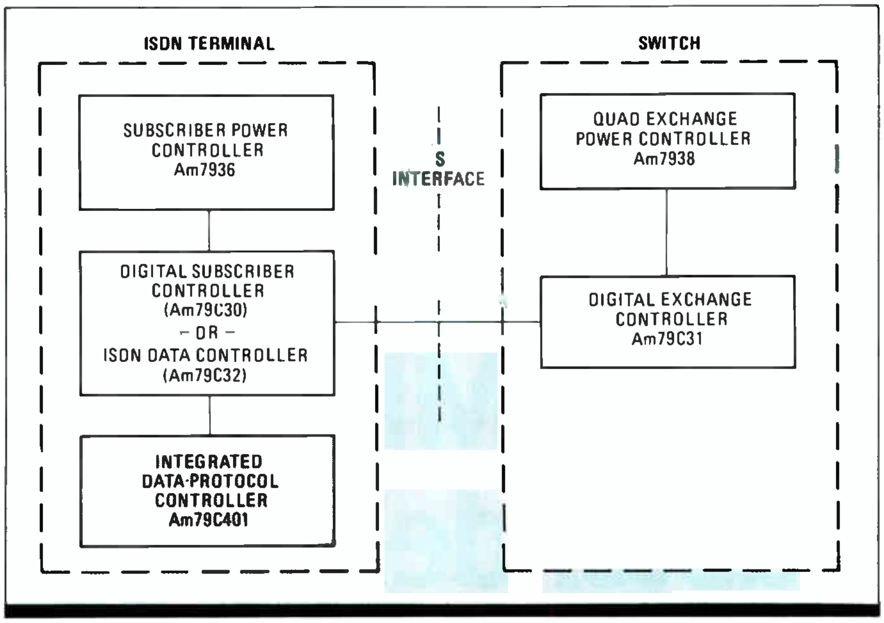
The chip's dual-port memory controller is used only in applications where multiple processors share memory. A typical application would be an ISDN adapter board for a PC in which the computer would have to pass commands and parameters to a local processor on the plug-in card. The controller arbitrates the use of shared RAM on the card by the processors. When both processors request the bus simultaneously, access is given to the local processor. When both processors need to access a common area of memory such as command or status mailboxes, a set of interrupt pins and a semaphore register are provided to manage the sequence of accesses. The memory controller lets systems designers implement shared RAM with low-cost static RAM instead of expensive dual-port RAM.

The 79C401's microprocessor interface performs timing control to the external processor, does the address decoding for module selection, and performs the internal synchronization for the chip's other three modules and the external bus. AMD optimized the bus interface for Intel Corp.'s 80188 processor, but its characteristics are general enough to interface to almost any microprocessor, says Lawell. Internal registers are memory-mapped, allowing the processor to address them directly. This aspect of the chip's architecture was implemented for ease of software development. "Since each register has its own address, designers can make this point look like normal memory locations for read and write techniques," says Ron Ruebusch, director of telecommunication-product marketing.

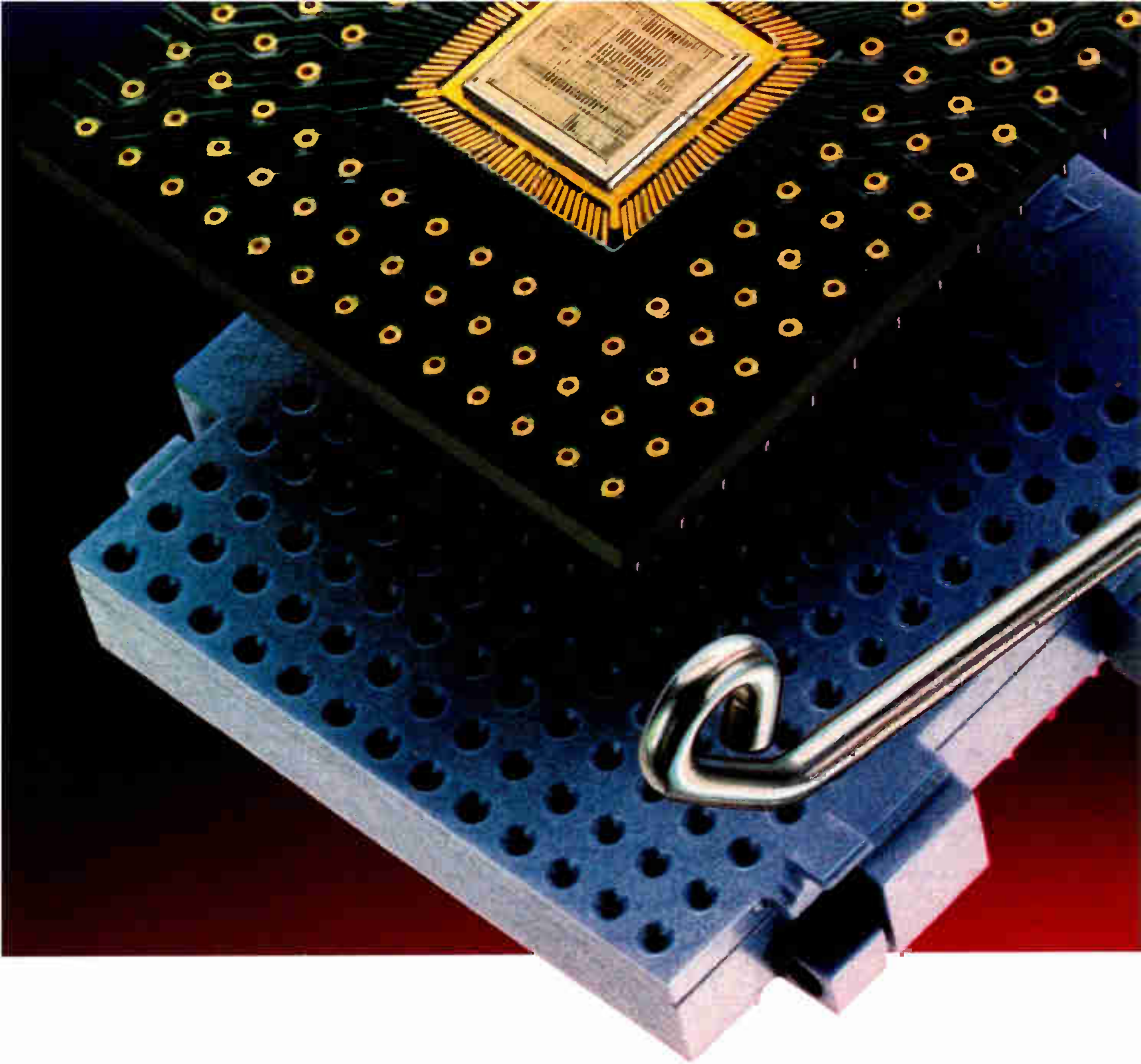
For most ISDN products, software development ties up 10 times more labor than hardware development; so the 79C401 comes with a rich software dowry. It includes the low-level device drivers and LAPD protocol to support ISDN's data-carrying B channels and signaling D channel. □

For more information, circle 485 on the reader service card.

The Am79C401 can determine the status of ISDN data packets on its own; other controllers spend up to 40% of their time querying the host processor for this data



2. FULL HOUSE. The 79C401 completes AMD's chip set for the ISDN S interface; it handles the data-link protocol, offloading these tasks from the host microprocessor.



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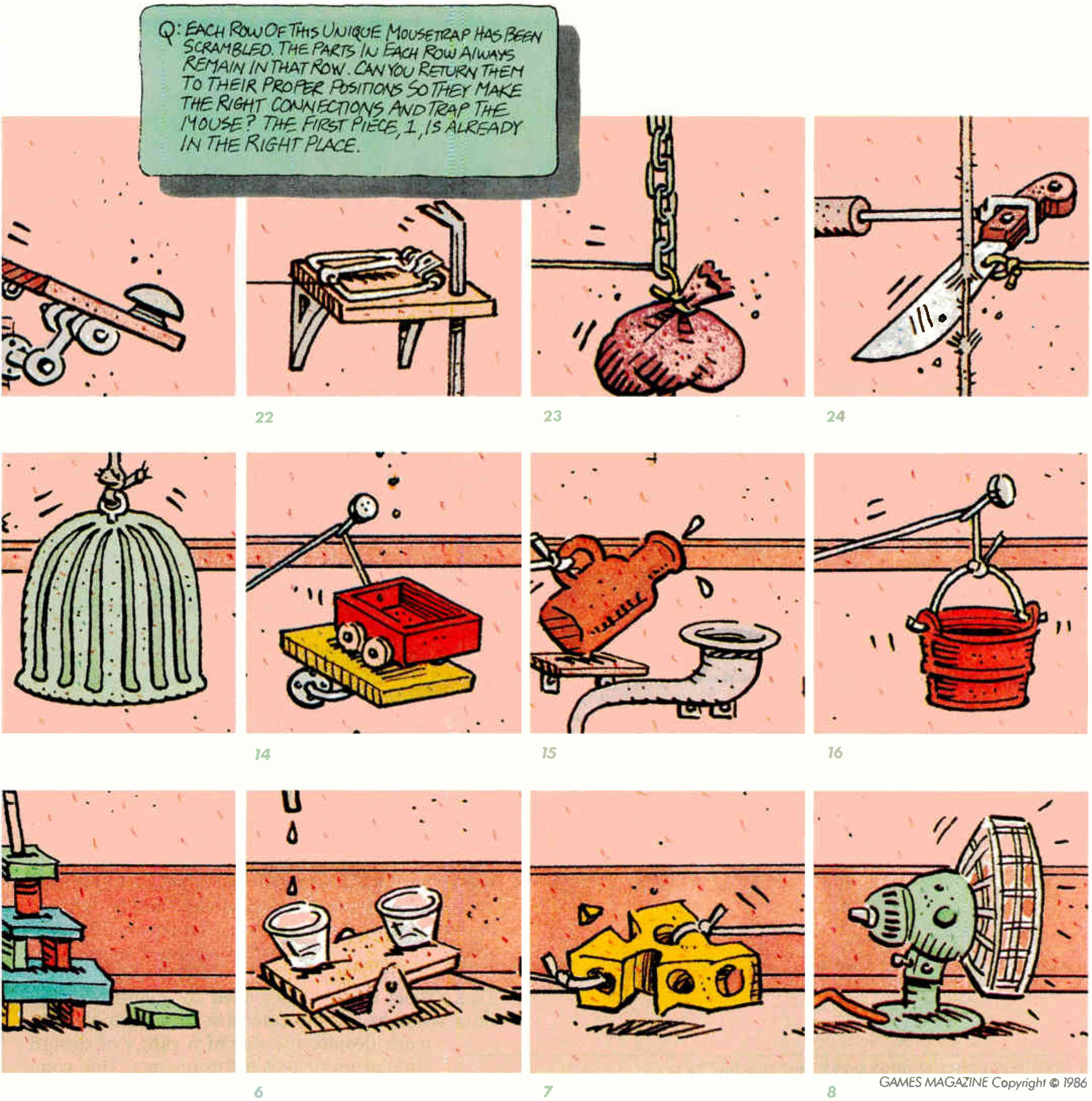
Q: EACH ROW OF THIS UNIQUE MOUSETRAP HAS BEEN SCRAMBLED. THE PARTS IN EACH ROW ALWAYS REMAIN IN THAT ROW. CAN YOU RETURN THEM TO THEIR PROPER POSITIONS SO THEY MAKE THE RIGHT CONNECTIONS AND TRAP THE MOUSE? THE FIRST PIECE, 1, IS ALREADY IN THE RIGHT PLACE.
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SPECIAL REPORT: GAP BETWEEN CAE AND ATE IS NARROWING

Test-gear makers are readying software that translates files developed on CAE systems to an intermediate format so they can be used to produce test programs

by Jonah McLeod

The links between automated design and automated testing of chips and printed-circuit boards are rapidly falling into place. Duplication of effort is being pared away, so that the test engineer developing test vectors no longer has to replicate a large part of what the designer did to simulate the circuit in the first place.

The ability to use the stimulus patterns from design simulation to produce test-system programs is a crucial one, because the amount of effort that goes into test engineering is rising rapidly as the level of chip integration goes up, and the increasing numbers of unique application-specific integrated circuits means more and more unique test programs must be generated. Furthermore, pressures are increasing to move ICs and pc boards to market quickly, as design cycles and product lifetimes shorten.

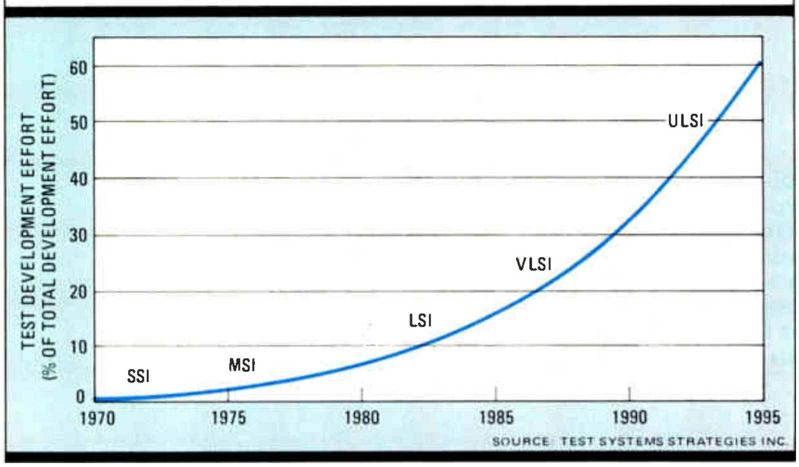
But the simulators that run on computer-aided engineering systems used for chip and board design do not produce stimulus files that can be passed directly to test systems; there are many incompatible design simulators producing output in different formats, and each test system has unique input needs. Some makers of automatic test equipment have set about developing translation programs that bridge the gap between their systems and design simulators.

The most flexible approach to this task involves the use of common intermediate file structures, such as those from Zehntel and Sentry Schlumberger. Programs can then be written to move files from various simulators into the intermediate format, and other ones to produce test programs from the intermediate-format files. Tools can be developed to operate on the data while in the intermediate format, tools that work despite the use of a range of design simulators or test environments. One company, Test System Strategies Inc. of Beaverton, Ore., offers neither CAE nor ATE equipment, but specializes in versatile software for producing test programs for many different ATE systems from the output of many different CAE systems—a big advantage for end users with more than one kind of test system.

The software environments developed by the ATE companies themselves offer less universality in their approaches but a tighter integration path between CAE and ATE. GenRad, Teradyne, Tektronix, and Hewlett-Packard, among others, are developing such links.

One major reason why there has been

TEST DEVELOPMENT BOGS DOWN CHIP DESIGNERS



more emphasis of late on improving the design-to-test connection can be seen in the increase in ASIC design starts. The number of ASICs designed will grow from 6,000 in 1985 to over 90,000 in 1990, according to Technical Insights Inc., an Englewood, N. J., market-research firm. At the same time, "design windows have shrunk from 12 to 15 months down to 6 to 9 months," says Robert Castellano, president of The Information Network, a San Francisco research firm.

ASICs find their way onto pc boards, which are also on tight schedules. "From the time a board is started to the time it is shipped, no more than 15 months have elapsed, and once the product is on the market, it may have no more than 9 months of product life," says Castellano.

While CAE design tools have reduced the time required to design a chip or board, until recently there has been no commensurate reduction in the time it takes to create a test program for them. The problem is aggravated by the fact that as levels of integration rise, test-development times become a much larger portion of the total time to produce a chip (see chart, opposite).

A partial solution has been for the design engineer to provide the test engineer with data files containing the schematic and the vectors used to verify the design. Then the test engineer must convert the vectors into a form that can be used by the test system.

Many ATE suppliers now offer translator programs for various design simulators. For example, Zehntel Inc. of Walnut Creek, Calif., offers its Simlink, which converts the output of the Daisy Logic Simulator from Daisy Systems Corp. of Mountain View, Calif., and the Hilo simulator versions 2 and 3 from GenRad into test patterns that can be used by the company's Model 875, 850, and 3200 testers.

"Simlink converts the simulator data into an intermediate TVF [test vector format]," says Koorosh Mazifi, marketing product manager at Zehntel. "It then converts the TVF into a test program for a specific tester." This intermediate format helps minimize the number of translators that a CAE system must provide to accommodate different test systems.

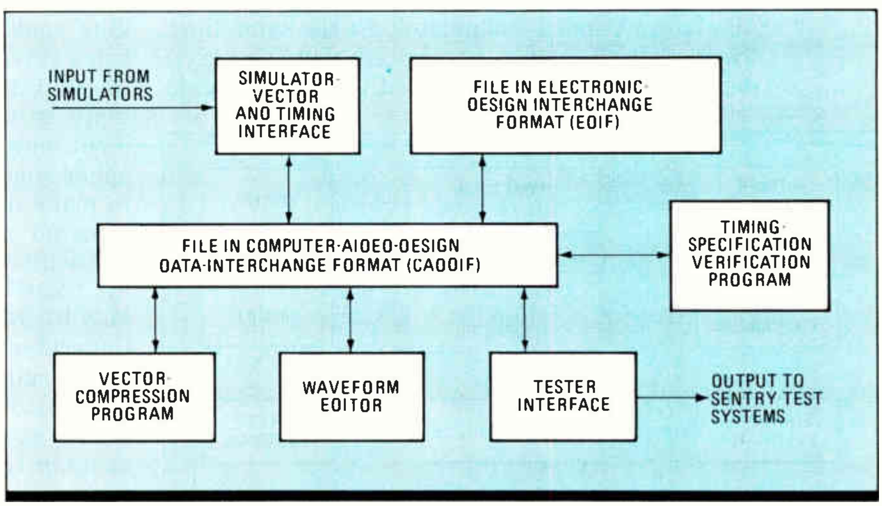
The experience of Sentry Schlumberger of San Jose, Calif., with its intermediate file structure, the Computer-Aided-Design Data-Interchange Format, illustrates how this minimization works. "In our use of this capability, the output of a popular commercially available simulator is preprocessed and converted into Caddif," says Neil Richardson, Schlumberger director of advanced ATE products. "The Caddif file is then converted into tester-specific test vectors," he adds (see fig. 1). Interfaces to Caddif currently support Lasar, Hilo, Cadat, and Tegas simulators, as well as the simulators from Daisy Systems and Mentor Graphics.

Once in the intermediate format, software tools can edit and compress the data. Thereafter, a separate tester-interface translator program converts the Caddif file into patterns that can be used by a target tester.

However, the ATE buyer is faced with a proliferation of intermediate file formats, each from a different test-system manufacturer. Test-system buyers want a standard, one intermediate file structure common to all vendors' simulators and ATE equipment, rather than having a unique intermediate format they must use for a specific brand of ATE gear. The best chance of achieving such a standard rests with SEF (standard events format), the format developed by Test Systems Strategies. The company has also written programs to convert stimulus files from most simulators into patterns which can be used by most ATE equipment. The company's offering has primarily served ASIC designers, but at the International Test Conference held in Washington, D. C., in September, it broadened its offering to include pc-board design-to-test links as well.

SEF and its associated software go beyond providing a common interface between design simulators and test systems. The company's Test Development Series (TDS) software tools, for which SEF is the data-base file structure, helps the test engineer create a final test program in other ways (see fig. 2). After a converter program translates the logic-simulator file into the SEF format, the Simulation Rules Checker produces a report for the test engineer of conflicts between the tester capability and the capabilities called for by the stimulus patterns. For example, the patterns might ask a 5-ns-wide pulse of a tester that can produce a pulse no narrower than 10 ns.

Another TDS tool, the Test Resource Allocation Manager, checks for other kinds of tester-specific incompatibilities. It looks at the intent of the



1. IN BETWEEN. Sentry Schlumberger's CADDIF is typical of the intermediate file formats ATE vendors use to convert vectors from a variety of design simulators into tester-specific patterns.

Circle 75 on reader service card

ETHERNET OR STARLAN? THIS CONTROLLER DOES BOTH JOBS

Fujitsu's new IC also takes over part of the supervisory burden from the host CPU

by Bernard C. Cole

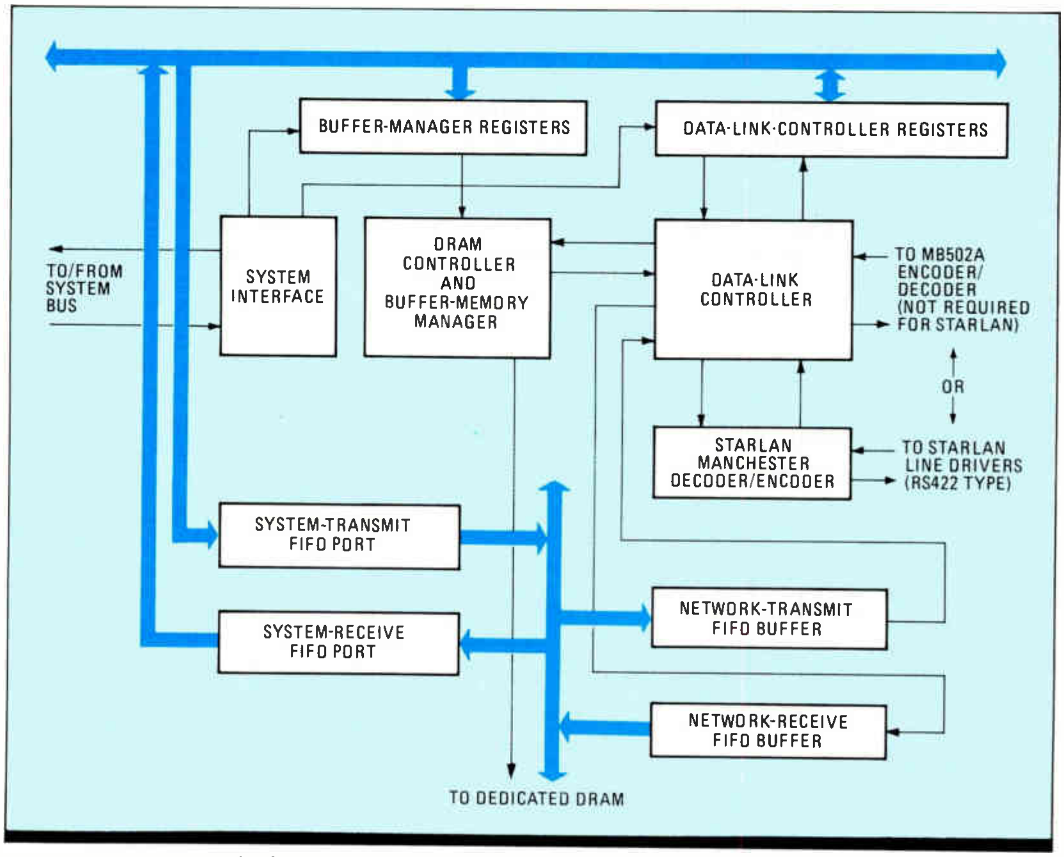
Designers looking to develop local-area-network boards and subsystems for work stations and personal computers will no longer have to choose between chips that implement one of the two main communications protocols, Ethernet or StarLAN. Fujitsu Microelectronics Inc. has come up with a controller, the MB86950 Etherstar, that tucks both protocols within one chip (see fig. 1).

As a bonus, the chip's architecture has been enhanced to reduce the host central processing unit's supervisory responsibilities by 10% to 20%—a major consideration, since with most network schemes the CPU devotes up to 20% of its time overseeing the flow of network information. The enhancements include a larger buffer memory and a serial-in, parallel-out first-in, first-out memory block. Fabricated in 1.5-μm double-metal, double-polysilicon CMOS, the 40,000-mil^2 chip consumes only 500 mW.

"Basically there are two ways to look at what we are offering the system designer and board manufacturer with the Etherstar chip," says Don W. Lake, director of marketing for the Santa Clara, Calif., company's Advanced Products Division. "On the one hand we are offering a LAN controller that will reduce the supervisory load and increase performance, with the bonus of easily implementing either StarLAN or Ethernet. Alternatively, we can also be viewed as offering an all-in-one protocol chip, with the additional benefit of increasing system performance by 10% to 20%."

Samples of the Etherstar chip are available for $35 each in quantities up to 100. For larger orders, the price drops to about $12. Volume production should begin in the first quarter of 1988.

Currently, Ethernet accounts for some 40% of all LAN protocols (about 250,000 to 350,000 units per year) and StarLAN for about 30%. "Previously these two markets were pretty well differentiated into two segments," says Lake. These are "high-performance work stations and minicomputers requiring the higher speed" of Ethernet, which reaches a 10-Mbits/s transmission rate; "and 8- and 16-bit personal-computer systems, for which the lower-speed [1 Mbit/s] StarLAN protocol is more than adequate." But the emergence of lower-cost personal computers and work stations based on the new 32-bit microprocessors has systems designers demanding a cost-effective single-chip solution in the higher-performance LAN arena. This is where the new



1. DUAL MODE. Fujitsu's CMOS MB86950 Etherstar chip includes the logic to implement both the Ethernet and the StarLAN protocols. The chip consumes only 500 mW and includes features to offload a host CPU.

Fujitsu 86950 device will excel, says Lake.

The main buyers, he says, will be vendors who supply LAN plug-in boards to systems designers. Since it will no longer be necessary to design different boards and different sets of software for each protocol, these suppliers will benefit from reduced development costs, he says. With Etherstar, it's possible to devise a single-board solution in which most of the hardware and software are common to both protocols (see fig. 2). "The only additional development work is the programming effort involved in writing the routines necessary to interface to either of the protocols," says Lake.

The Etherstar chip is configurable for use on both 8- and 16-bit-wide bus interfaces, says Albert Chiang, LAN applications engineer at the Advanced Product Division. It incorporates a data-link controller, a 1-Mbit/s Manchester encoder/decoder for StarLAN applications, a dynamic-random-access-memory controller, a buffer memory controller, and associated FIFO buffers. To switch between the two modes, says Chiang, all that is necessary is to toggle a single pin—to high for Ethernet, to low for StarLAN. The only external component required is an analog-to-digital encoder/decoder, used to implement Ethernet's analog collision-detection scheme (StarLAN uses a digital technique).

The data-link controller provides for automatic generation and stripping of the 64-bit preamble, as well as cyclic redundancy checking, serial and parallel data conversions, and contention resolution and address recognition for both protocols. The DRAM controller handles data-packet transfers between a system's main memory and the buffer memory, and between the buffer memory and the LAN. It transfers 1.5-Kbyte data packets from the LAN to a receive buffer memory without host-system intervention.

A number of architectural enhancements boost the chip's performance with either protocol, says Chiang. First, having the buffer-memory controller on-chip eliminates the need for an external microcontroller, which was necessary in earlier single-chip implementations for either StarLAN or Ethernet. The chip contains registers for receive/transmit control, status count, node identification, and port status, so the buffer manager together with the DRAM-controller block can handle all data transfers back and forth between host and network. This setup reduces the overhead processing usually handled by the CPU or the external microcontroller.

The receive-and-transmit FIFO memory further reduces the time the CPU spends with LAN communications. "In other designs, the FIFOs are very small, with only enough room for the 64-bit header preamble of each block of data," Chiang says. "So once the device determines that the block of information has a destination-code match, the CPU must drop its other activities, immediately service such requests, and move the data to external local memory." Such a scheme takes the CPU away from its primary chores, reducing throughput on the user end. It also increases the possibility of losing data if the CPU does not respond quickly enough.

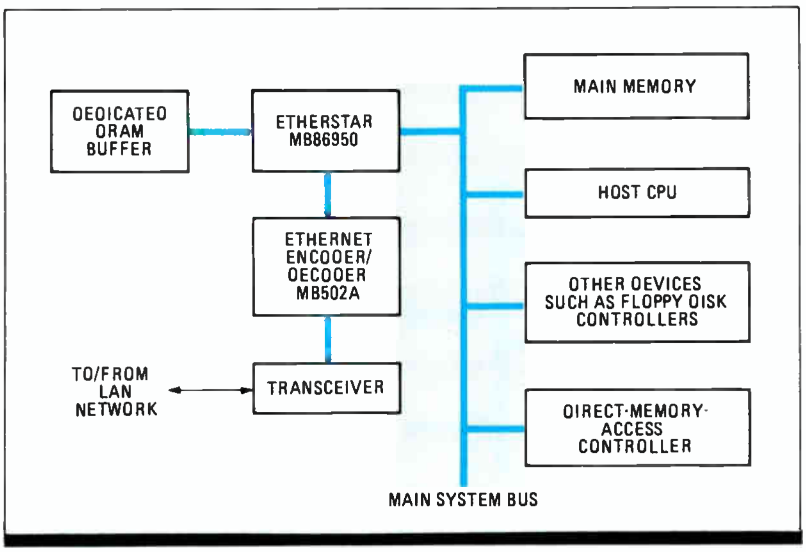
The Etherstar chip overcomes these problems in two ways. First, Fujitsu has increased the size of the internal FIFOs two to three times—to 4 Kbytes in the transmit section and up to 60 Kbytes in the receive section. Second, the chip incorporates logic that allows automatic transfer of 1.5-Kbit data packets into external buffer memory, relieving the host CPU of this task.

To further improve throughput, Fujitsu designers have moved away from the traditional serial-in, serial-out approach to the internal FIFO, going instead to a serial-in, parallel-out architecture. Deserializer logic is incorporated into the receive and transmit FIFO blocks, says Chiang, and it converts the serial data stream into an 8-bit parallel format while automatically moving it to the buffer memory.

A final modification is an external input/output bus structure with separate address and data pins. "Going to a separate data and address scheme increases the number of pins from 48 to 80," says Chiang. "The tradeoff is that this bus scheme is easier to implement in most high-performance microprocessor designs, where the data and address buses are also separate."

While the numbers may vary from system to system, Lake says that the result of all these architectural enhancements is an overall 10% to 20% improvement in the host CPU performance. The actual figure will depend on the characteristics of the particular network scheme and bus utilization. □

For more information, circle 481 on the reader service card.



2. LOWER COST. With the Etherstar chip, designers can considerably reduce development time and the cost of local-area networking boards.

PHILIPS FINDS A NEW WAY TO BOOST ADC CHIP PERFORMANCE

Result: An 8-bit flash-converter family that's more accurate yet has less circuitry

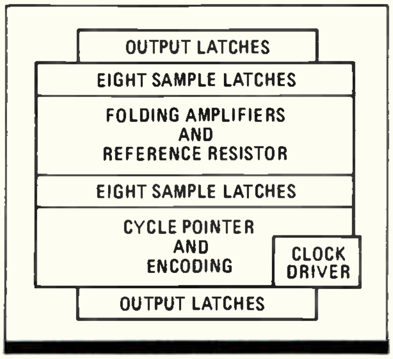
by John Gosch

A three-year development effort at the Philips Research Laboratories in Eindhoven, the Netherlands, has culminated in a family of monolithic 8-bit flash analog-to-digital converters that run rings around other 8-bit competitors. Initially aimed at consumer applications such as digital TV and satellite TV, the converters' performance has proven so good that Philips expects them to find wide use in industrial applications such as radar and sonar gear, test and measuring systems, and image-processing and medical equipment.

The bipolar ADCs, which will be marketed as the TDA/TDE family, are the first such devices to use conversion principles based on folding and interpolation techniques, Philips says. Made in an oxide-isolated process with minimum features of 1.7 μm, they boast parameters that the Dutch company considers far superior to those of competing ADCs, in a design that drastically reduces component count and chip size. For example, Philips has slashed the number of latches from the 255 typically found in an 8-bit ADC to a mere 16. And the number of comparators has been reduced from 255 to 64.

These cuts have enabled the company to squeeze the new ADCs onto a 2-by-3-mm chip (see fig. 1)—about one fifth the size of competing ADCs. What's more, the reduced number of components means a dissipation of less than 300 mW, or one tenth the power consumed by the best available bipolar converters, says senior research scientist Rob van de Grift.

Samples of the new converters, three of which will be available by the end of the year, will start at $12 apiece. But after production gets into high gear early next year, the Philips devices will undersell competing 8-bit ADCs by up to 50%, promises Wil Adriaans, international product-marketing manager for bipolar ICs at the company's Electronic Component and Materials Division—Elcoma, for short.

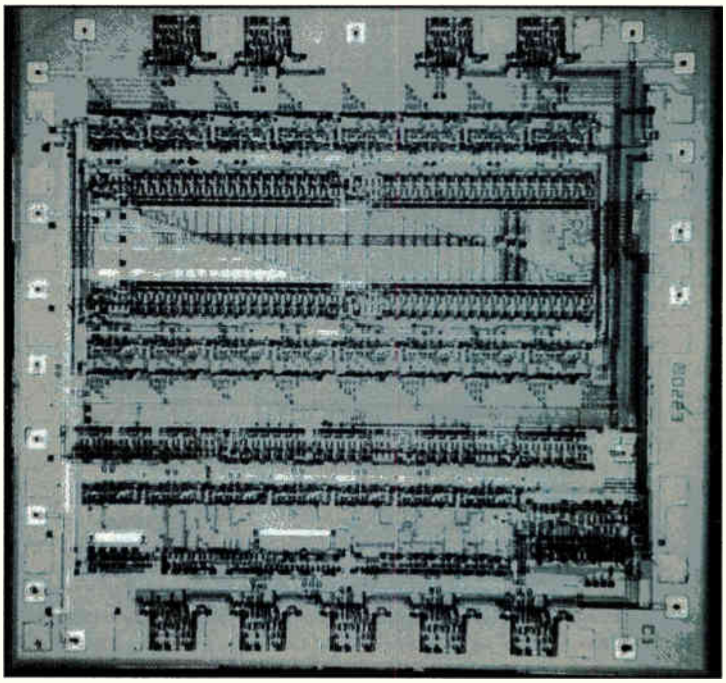


1. SQUEEZE. The number of components in Philips's TDA/TDE family of 8-bit flash ADCs is dramatically reduced thanks to its new "folding and interpolation" techniques. The result: a chip only 2 × 3 mm in size.

Two of the first converters out of the pipeline are for industrial uses and the third is for video. They will differ only in temperature range, package type, and output configuration. At the same time, Philips will also have available digital-to-analog converters suitable for systems using the new ADCs; the DACs are being built using standard techniques, which can easily meet the less stringent requirements of digital-to-analog conversion.

The new ADCs sport an accuracy of ±¼ least significant bit, which compares with ±½ LSB for the best on the market. Their 8-bit effective resolution is at 8 MHz, which means that up to that input frequency, the converter performs to its full specifications. That spec, too, is better than what the competition achieves, says research scientist Ivo Rutten.

For example, when composite video signals must be digitized, available 8-bit ADCs are often down to 4 or 5 effective bits of resolution at the color-subcarrier frequency: 4.4 MHz for the PAL transmission standard and 3.58 MHz for NTSC. "What's more, [these devices] use lots of power,



TI TO ROLL OUT ITS FIRST FAMILY OF PRODUCTS MADE WITH BiCMOS

The interface ICs offer CMOS's low power and bipolar's switching speed, current drive

by Samuel Weber

Texas Instruments Inc. is all set to begin shipping a brand new family of interface chips that are notable for two important reasons: These ICs run cooler than any other high-performance interface chips, delivering bipolar speeds at CMOS power levels. More importantly, at least to TI, they're the first family of products from the Dallas chip maker to be made by its flavor of biCMOS, a process that TI is convinced will be its technology driver of the 1990s. It is not alone: although there are relatively few suppliers or customers of biCMOS circuits as yet, chip makers are rushing to jump on the bandwagon.

The devices are made with a new process based on Impact, TI's mainstream high-performance bipolar technology, which has been modified to accept CMOS on the same substrate. The result is Impact CS (see fig. 1). The company has big plans for its biCMOS process: it will use it across the board, building memories, gate arrays, application-specific ICs and even linear circuits.

"The benefits of such a process for interface logic are twofold," says William A. Thompson Jr., strategic marketing manager, Bipolar and CMOS Advanced Logic Department in TI's Semiconductor Group. "A device can simultaneously offer the low-power dissipation of CMOS together with bipolar's superior switching speed and current drive."

That combination is coming just in time for designers now working on the next generation of 32-bit microprocessor systems, which are requiring far more interface chips than ever before. Add to this the accelerating trend toward surface mounting, and it's easy to see that designers who want their boards to stay cool will need low-power, high-speed interface chips.

The SN74BCT interface family will include 8-, 9-, and 10-bit biCMOS bus drivers, memory drivers, latches, registers, and transceivers. Available this month will be four octal bus transceivers and four 8- or 9-bit-parity transceivers. By the end of the year, this family will number 37 devices, and by the end of next year it will grow to 98.

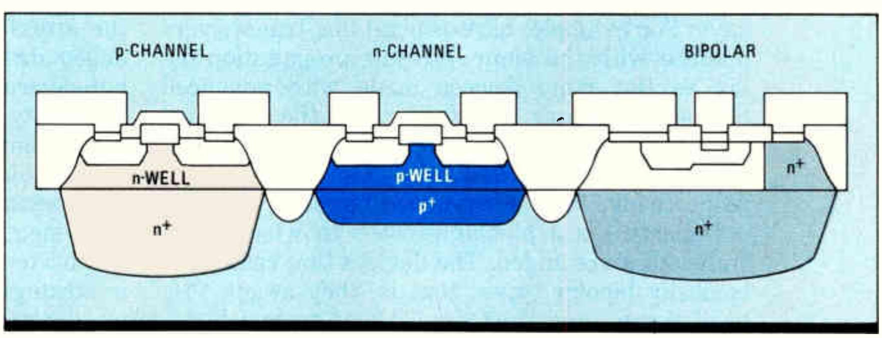
The advantages of biCMOS technology over pure bipolar go far beyond the relative performance of individual drivers or transceivers. A typical 32-bit microprocessor system may contain 10 or more interface devices. Just one bus driver is activated at a time, causing a typical driver to be in the disabled state as much as 90% of the time. When the interface units are pure bipolar, the disabled drivers are all burning up power, since they remain in the high-impedance state awaiting their turns to be activated.

The picture changes radically when the drivers are biCMOS. When the total current draw of all the disabled biCMOS drivers is compared with that of disabled bipolar drivers, the reduction in supply-current demand of biCMOS technology is overwhelming. In some cases, biCMOS devices can bring about a power savings of almost 100%.

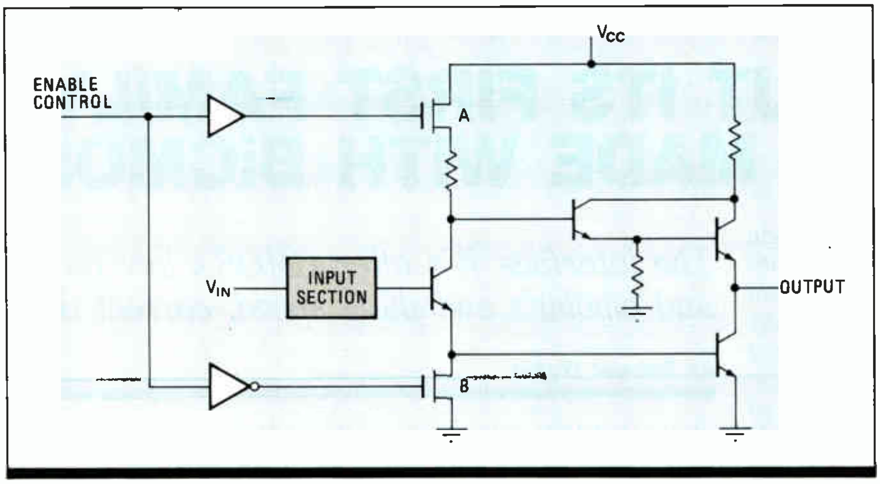
Gate power consumption for the SN74BCT chips remains quite low, even as system operating frequencies increase. For example, power consumption of a biCMOS octal line driver is about one fourth that of the corresponding bipolar device, even across wide operating frequencies, for single-output switching up to 10 MHz. Studies indicate that traditional bus interfaces consume 30% of a system's total current.

System designers are fully aware of the tradeoffs involved in using bipolar logic to drive buses. To get the needed drive currents of 48 to 64 mA, power consumption must be high, because bipolar drivers gobble up chunks of supply current even while idling.

BiCMOS technology eliminates this waste of energy by employing different three-state tactics. To reduce power consumption, TI designers added a pair of n-channel CMOS transistors and two gates—inverting and noninverting—to the basic gate to cut current flow to the bipolar transistors in the disabled state (see fig. 2). During normal operation, in the active state, a logic 1 is applied to the enable-control line to turn on CMOS



1. COMBINATION. TI's Impact-CS process combines the high speed, high output drive, and TTL I/O levels of bipolar with the lower power consumption of CMOS.



2. POWER SAVER. A pair of n-channel CMOS transistors and two gates—inverting and noninverting—cut current flow to the bipolar transistors in the disabled state.

transistor A and turn off CMOS transistor B.

Current flows from the supply through transistor A and into the base of the bipolar Darlington output stage. Current can also flow into the base of the saturating bipolar transistor, since transistor B is off. In the high-impedance state, the logic level on the enable line is reversed (logic 0). Transistor A is now off and transistor B is on. Neither the Darlington nor the saturating transistor can draw base current, putting the gate in its high-impedance state.

The result is a significant reduction in supply current flowing into the basic gate. A biCMOS driver that draws 30 mA when active draws just 10 mA when disabled. Furthermore, a biCMOS driver draws far less current than its advanced bipolar counterpart, which draws 150 mA whether active or disabled.

Although lowering system power is the primary motivation for making biCMOS interface chips, the devices must maintain high performance levels. TI's SN74BCT family offers speed and drive capabilities equivalent to advanced bipolar logic. Propagation delay times for a complete biCMOS gate function are comparable to those of advanced bipolar technology—3 to 5 ns.

"The major difference is that TI devices draw less than half the current of advanced bipolar drivers in the active mode and less than 10% of the current in the disabled mode," Thompson says. For example, biCMOS octal bus transceivers operate with the same 7-to-8-ns propagation delay as the same devices made with advanced bipolar processes. However, in the disabled (high-impedance) state, the biCMOS chips draw only 15 mA, compared with 115 and 170 mA, respectively, for the advanced bipolar types.

Impact-CS is a bipolar process to which CMOS transistors are added. The devices that result are basically bipolar types; that is, they accept TTL-level inputs, and they drive buses to which TTL devices are connected. But thanks to the CMOS transistors, these chips draw less power in both the enabled and disabled states.

The bipolar process produces output transistors capable of supplying the 48-to-64-mA currents needed to drive the capacitive inputs of MOS memories and the low-impedance backplanes of high-speed bipolar systems. Another benefit of bipolar output transistors is their lower voltage swing compared with CMOS transistors (0.5 to 3.5 V, compared with ground to V_{CC}). A narrow voltage-swing range reduces the effect of transient-voltage noise on the ground pins.

With the Impact-CS process, bipolar devices can be fabricated with current gains of 100. The typical n-MOS transistor boasts a normalized current gain of 39 $\mu A/V^2$, while the figure for the typical p-MOS transistor is 12 $\mu A/V^2$. Both n-MOS and p-MOS transistors have internal threshold voltages of 1.0 V.

The disable circuit provided by the CMOS transistors consumes considerably less current than a pure bipolar circuit; CMOS devices draw virtually no current in the standby or unclocked state.

Impact-CS is a combination 2.0-μm bipolar and 1.5-μm CMOS process that uses two metal levels for interconnections. The metal pitch on the first level is 4.0 μm, allowing for high-density packing of transistors. Also, reducing the metal pitch allows the transistors to switch faster, because it shortens the interconnections between devices.

The metal pitch can be as small as it is because Impact-CS incorporates a high degree of surface planarization, or smoothing, of its device surface. MOS devices usually contain greater topographical bumps and discontinuities on their surface. The smoother the surface, however, the better the step coverage, which in turn results in more reliable devices.

"Three additional processing steps are required to add CMOS transistors to what is inherently a bipolar process," Thompson says. "Since the bipolar process uses an n-type epitaxial layer, a masking level is needed to counter-dope selected regions to be p-type. The second masking step involves forming moats and isolation regions. In the third step, polysilicon gates for the CMOS transistors are formed." A lightly doped drain was also implemented to suppress hot-electron effects and to improve the future scalability of n-channel transistors.

The simplest implementation of a biCMOS device requires just two CMOS transistors to control the operation of the bipolar output stage. Future implementations of biCMOS technology may incorporate greater numbers of CMOS transistors in strategic locations, particularly as the Impact-CS process moves toward more-complex and more-advanced devices. □

For more information, circle 483 on the reader service card.

is an average of what's around it. Pixels cannot be turned on or off fully, because of crosstalk between them, and that's why the contrast ratio and brightness decrease as the number of lines increases.

Alphasil gets around the crosstalk problems of multiplexing by placing an amorphous-silicon thin-film transistor at every pixel on the screen so that each pixel is individually controlled (see fig. 2). This is a return to direct pixel addressing, but with an active switch right on the screen at each pixel to turn it on or off definitely. The ratio of current draw between on and off achieved by the Alphasil engineers with their thin-film transistor is a whopping 1 million to 1.

In the past, yield problems have frustrated the adoption of active-matrix LCDs. Building a reliable active matrix with a 100% yield over a wide area has proved to be a very difficult task. It is like fabricating a 5-inch wafer with 100,000 or more transistors without a single defect. It is equal to or more of a challenge than wafer-scale integrated circuits.

Building an active-matrix LCD requires the combination of two technologies: thin-film semiconductors and flat-panel liquid crystals. Display-industry research groups have tried many approaches to adding active-matrix diodes and transistors to their LCD displays. Alphasil's approach is the first from the semiconductor industry. "Our manufacturing process is 80% to 85% semiconductor and 15% display [technology], rather than the other way around," says Flasck. "When we set out to develop our manufacturing process, we laid down three rules for ourselves: standard materials, standard production equipment, and standard processing techniques—all so that we would get high yields, because yield is the name of the game," he adds.

Alphasil uses very thin amorphous silicon layers, which can be deposited on ordinary glass. Making the semiconductor part, the thin-film transistor, is very similar to standard wafer fabrication, but to approach 100% yield "we're using a 5-to-7-μm feature size so that we're not pushing the photolithographic state of the art," Flasck says.

"We also chose standard liquid-crystal technology in terms of the alignment layers, the polarizers, the choice of liquid-crystal material—we are using the type of material used in calculator and watch displays—and the sealing techniques, because these standard techniques do give you superb optical quality," says Flasck. Also, in Alphasil's LCD technology, neither the spacing between the plates nor the drive voltages are critical. Alphasil's conservative approach in both the semiconductor and liquid-crystal parts of the process add up to volume manufacturablility with high yields.

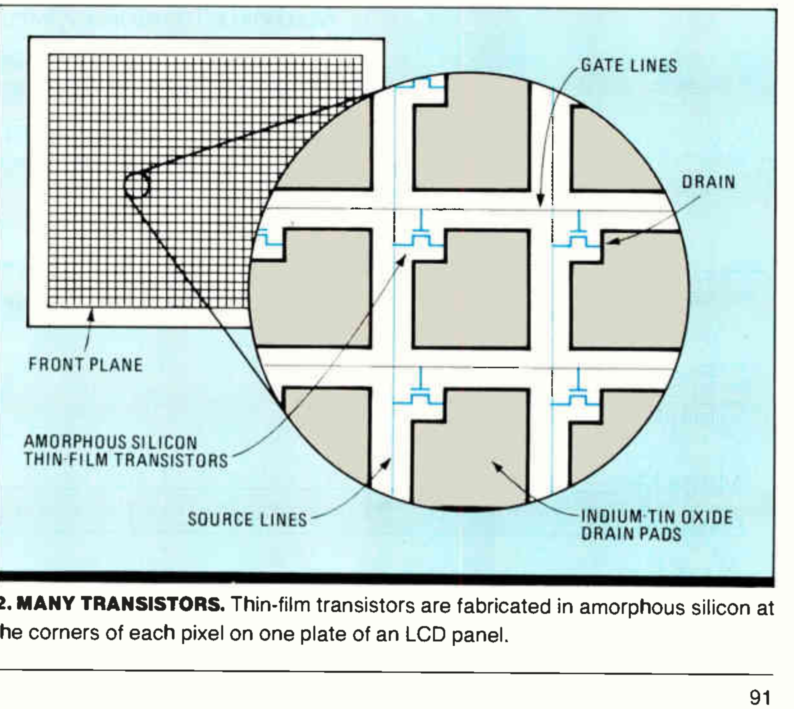
The Alphasil displays are available in a reflective mode for low-cost, very low-power applications. In this mode the display uses 0.25 W. However, for those applications requiring high brightness and contrast, Alphasil has developed a backlighting module that can go to very high levels of brightness as more power is applied. Power consumption is just about linear with brightness.

Other manufacturers of backlit LCDs have used incandescent bulbs, fluorescent tubes, or electroluminescent panels. "What we're using is an old neon tube made by a guy who makes beer signs," says Flasck. The thin, 8-mm-diameter neon tube is bent into a serpentine pattern, and a translucent plexiglass plate between the tube and the LCD panel diffuses the light evenly over the display. The Alphasil engineers have developed a proprietary small, lightweight power supply for the neon tube.

And because neon tubes can be made to emit any color of light, Alphasil display users have a wide choice of character colors. Neon tubes are also very efficient—5 to 10 times more efficient than electroluminescent panels, for example. For a 50-fL display it draws 1 W. Flasck estimates that the current power supply can drive the tube to produce up to 200 fL of surface brightness on the display. To go higher, a different power supply will be needed.

Now the engineers are looking at five areas for future development of Alphasil's active-matrix LCD technology. They expect to offer full-color displays next year. In addition, they are working on gray-scale displays; panels measuring 1 ft or more; and resolution higher than the current 128 dots/in. They are also working on lowering the costs by increasing yields and by integrating drive circuits in thin-film silicon on the glass, instead of putting them on a printed circuit board. □

For more information, circle 484 on the reader service card.



2. MANY TRANSISTORS. Thin-film transistors are fabricated in amorphous silicon at the corners of each pixel on one plate of an LCD panel.

ing to be so much faster that the chances the bridge will encounter any kinds of collisions or congestion is much, much smaller," he says.

The 50-Mbit/s EN603 costs $13,500 in single units, going up against lower-performance 10-Mbit/s bridges priced from about $8,000 to $11,500, says Gust. Network Systems is also offering a 10-Mbit/s bridge of its own, the EN601, which will use a 10-Mbit/s version of Hyperchannel as a backbone. It is priced at $8,500. The third member of the family is the EN602, which for $12,500 offers Ethernet linking via long-distance transmission media such as optical fiber, T1 telephone lines, microwave links, and satellite channels.

MIXED PROTOCOLS. Unlike the TCP/IP-based router product, the EN60X bridge family can handle a mixture of protocol traffic, including DECnet, XNS, and TCP/IP. The units employ a mix of TTL and CMOS chips, including three Motorola 6809 processors, all housed in a 5.5-by-16-by-17-in. cabinet. The bridges require no special software. The EN601 and EN602 are available now, and the EN603 is set for production delivery in the first quarter of 1988.

The introduction of router and bridge products compatible with networking standards other than Hyperchannel is a first for 13-year-old Network Systems [*Electronics*, Aug. 6, 1987, p. 22] and begins a commitment to support all widely used standards based on the Open Systems Interconnection model.

Hyperchannel products that tie in other standards will be introduced later, Gust says. "We're committed to providing the highest-performance work-station-to-mainframe interconnection in the industry, and doing that with industry standards."

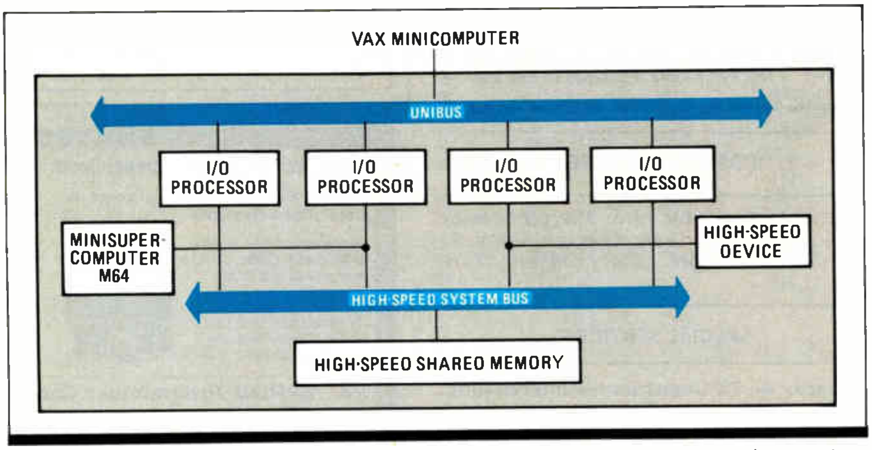
–Wesley R. Iversen

Network Systems Corp., 7600 Boone Ave. North, Minneapolis, Minn. 55428.
Phone (612) 424-4888 [Circle 340]

SUPERMINI I/O RUNS 20 TIMES FASTER

Multiple input/output processors that are capable of handling up to 12 Mbytes/s boost performance twentyfold in Floating Point Systems Inc.'s new P64/210 I/O subsystem. The predecessor subsystem was limiting the performance of the company's M64 Series of 64-bit minisupercomputers.

Because many of the Beaverton, Ore., company's minisupercomputers are used with Digital Equipment Corp. VAX superminis, the P64/210 is tailored to the VAX Unibus environment. It allows the M64 and VAX machines to share disk



DUAL BUS. Parallel buses link VAX computers and M64 minisupercomputer environments.

files and other I/O peripherals. The P64/210's Unibus I/O processors handle data transfers at a 3-Mbyte/s rate over Unibus.

The P64/210 can also connect high-speed non-Unibus peripheral devices to minisupercomputer systems with its Openbus I/O processors, which run at a 12-Mbyte/s rate. This means system integrators can configure M64-series machines into powerful, complex systems using multiple M64s, array processors, VAXes, high-speed disks, high-density tapes, and high-speed analog-to-digital converters. Flexibility of the I/O subsystem is further enhanced by up to 96 Mbytes of buffer memory. It can be accessed by the I/O processors at any speed up to the system bus's 24-Mbyte/s limit.

The P64/210 subsystem has three separate 32-bit buses to allow the system bus to handle concurrent transfers of 8-, 16-, or 32-bit data. The parallel I/O subsystem also has a built-in Unibus that links its multiple I/O processors together and to VAX machines.

The P64/210 offers full compatibility with the VAX VMS operating-system software, providing support for the VAX Files-11 record-management protocol. This transparent coupling with the VMS operating environment means that a VAX and an M64 minisupercomputer can share files on the same high-performance disk drive.

The P64/210 targets real-time applications, such as aerospace and defense simulation, image and signal processing, seismic analysis, and graphics post-processing jobs.

Floating Point Systems will begin shipping the P64/210 in October, at a price starting under $100,000.

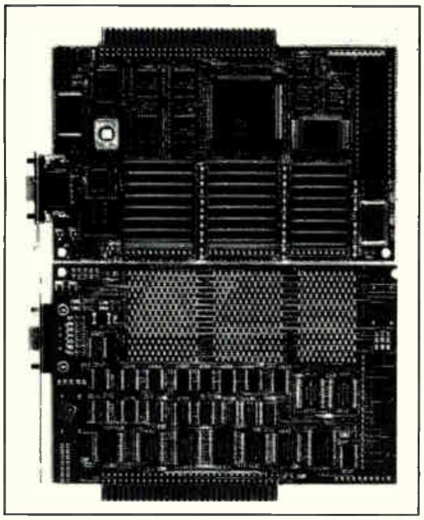
–Tom Manuel

Floating Point Systems Inc., 3601 S. W. Murray Blvd., Beaverton, Ore. 97005. Phone (503) 641-3151 [Circle 341]

CARD FOR PC DRAWS 10 MILLION PIXELS/S

The Model 1104 graphics coprocessor from Metheus Corp. occupies only half a slot in an IBM Corp. Personal Computer or compatible, but it can draw 10 million pixels/s with 1,024-by-768-pixel resolution on up to four bit planes.

The card achieves performance double that of standard graphics cards by implementing 500 Kbytes of video random-



access memory and VLSI circuitry. The compact size of the 1104 represents a combination of high-level chip integration and surface-mount technology.

The 1104 is fully compatible with the company's 1100-series software drivers and supports a wide range of the most popular computer-aided design software packages. The card is available now for $1,395.

Metheus Corp., 5510 N. E. Elam Pkwy., Hillsboro, Ore. 97214.
Phone (503) 640-8000 [Circle 346]

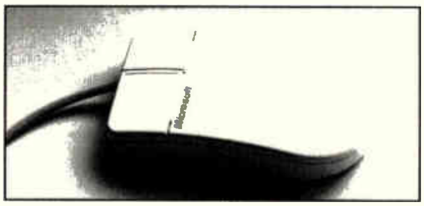
MICROSOFT MOUSE HAS CAD SOFTWARE

The newest version of the Microsoft Mouse features enhanced mechanical design, three versions of high-quality graphics support—including a computer-aided-design version—and compatibility with IBM Corp.'s Personal Computer and Personal System/2.

A key design improvement moves the center of balance from the user's palm to his fingertips for improved control.

Three different software packages are offered. The first costs $150 and is built around Microsoft Paintbrush, a color painting program developed by ZSoft of Marietta, Ga. The second, costing $200, is bundled with PC Paintbrush for Microsoft Windows, the key difference being that it works within the Windows environment.

The third version, at $175, targets the low-end CAD market with EasyCAD from Evolution Computing, Tempe, Ariz. All three versions are available now.



Microsoft Corp., 16011 N. E. 36th Way, Redmond, Wash. 98073.
Phone (206) 882-8080 [Circle 347]

HP'S 80386 VECTRAS TRIPLE PERFORMANCE

Hewlett-Packard Co.'s Vectra RS/16 and RS/20 personal computers integrate Intel Corp.'s 80386 microprocessor to get three and four times the performance of the original Vectras. Both floor-standing units, the RS/16 runs at 16 MHz and the RS/20 at 20 MHz.

The RS/16 includes 16 Mbytes of main memory and comes with a 40-Mbyte hard-disk drive. The RS/20 offers 20 Mbytes of main memory and comes with either a 103-, 155-, or 310-Mbyte hard-disk drive. The drives have an industry-standard ESDI interface and feature an average access time of 17 ms.

The memory in both systems can be expanded by 16 Mbytes by adding modules to the processor board. Both computers will be available in the first quarter of 1988. The RS/16 costs $6,495; the RS/20 ranges from $7,495 to $11,995.

Hewlett-Packard Co., 3000 Hanover St., Palo Alto, Calif. 94304.
Phone (415) 857-1501 [Circle 345]

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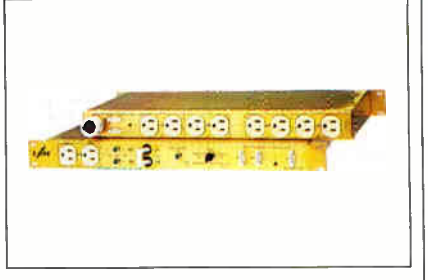

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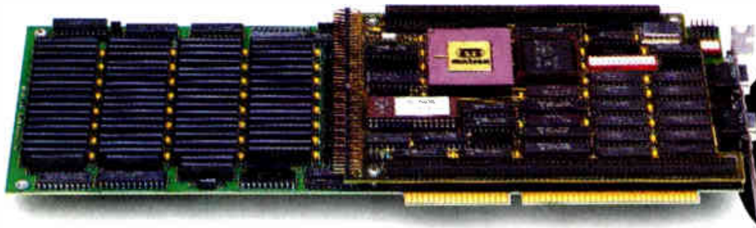

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