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Electronics®

WHEN STANDARD CPU CHIPS CAN'T CUT IT

THE FRANTIC SEARCH FOR MORE SPEED

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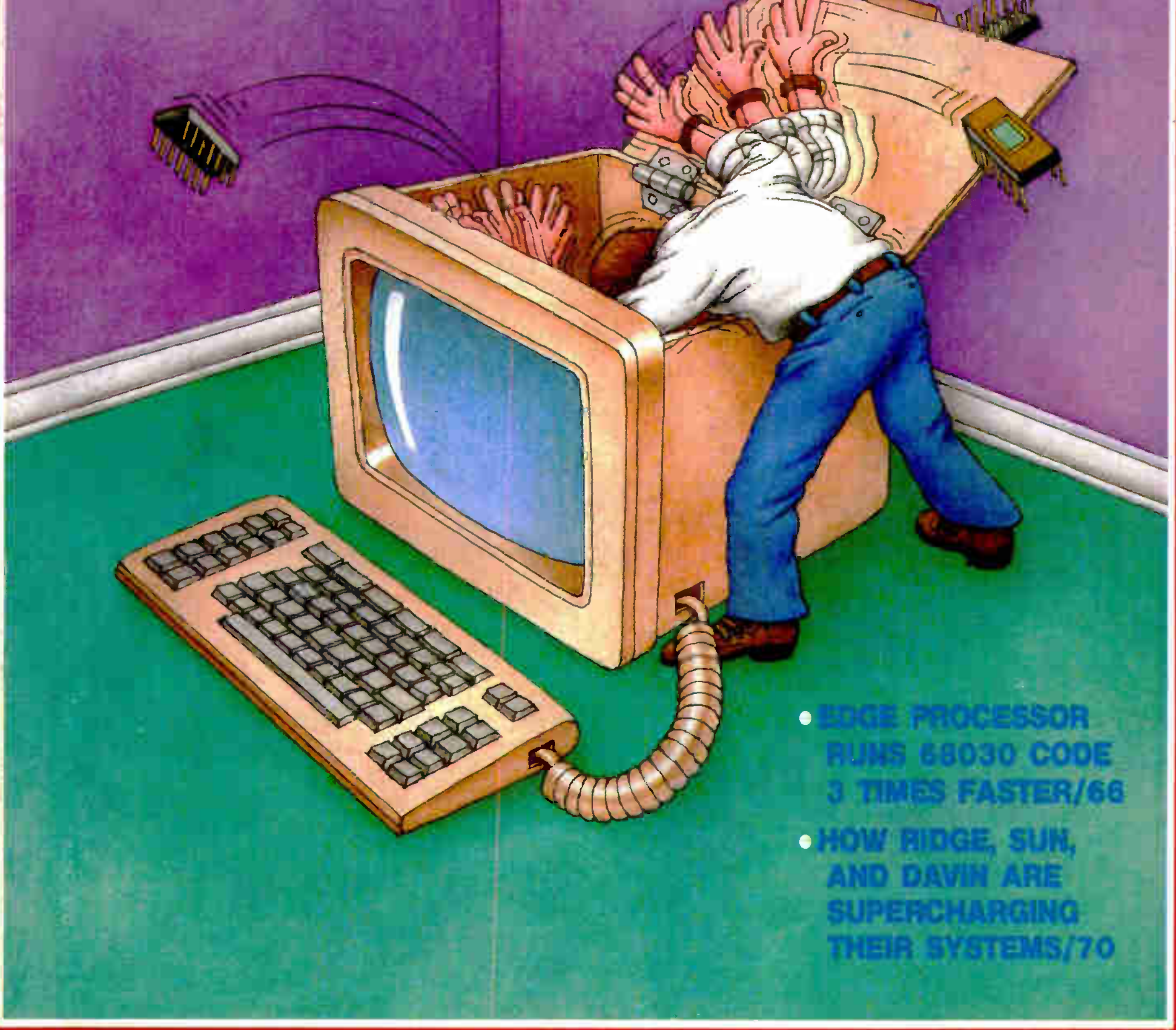

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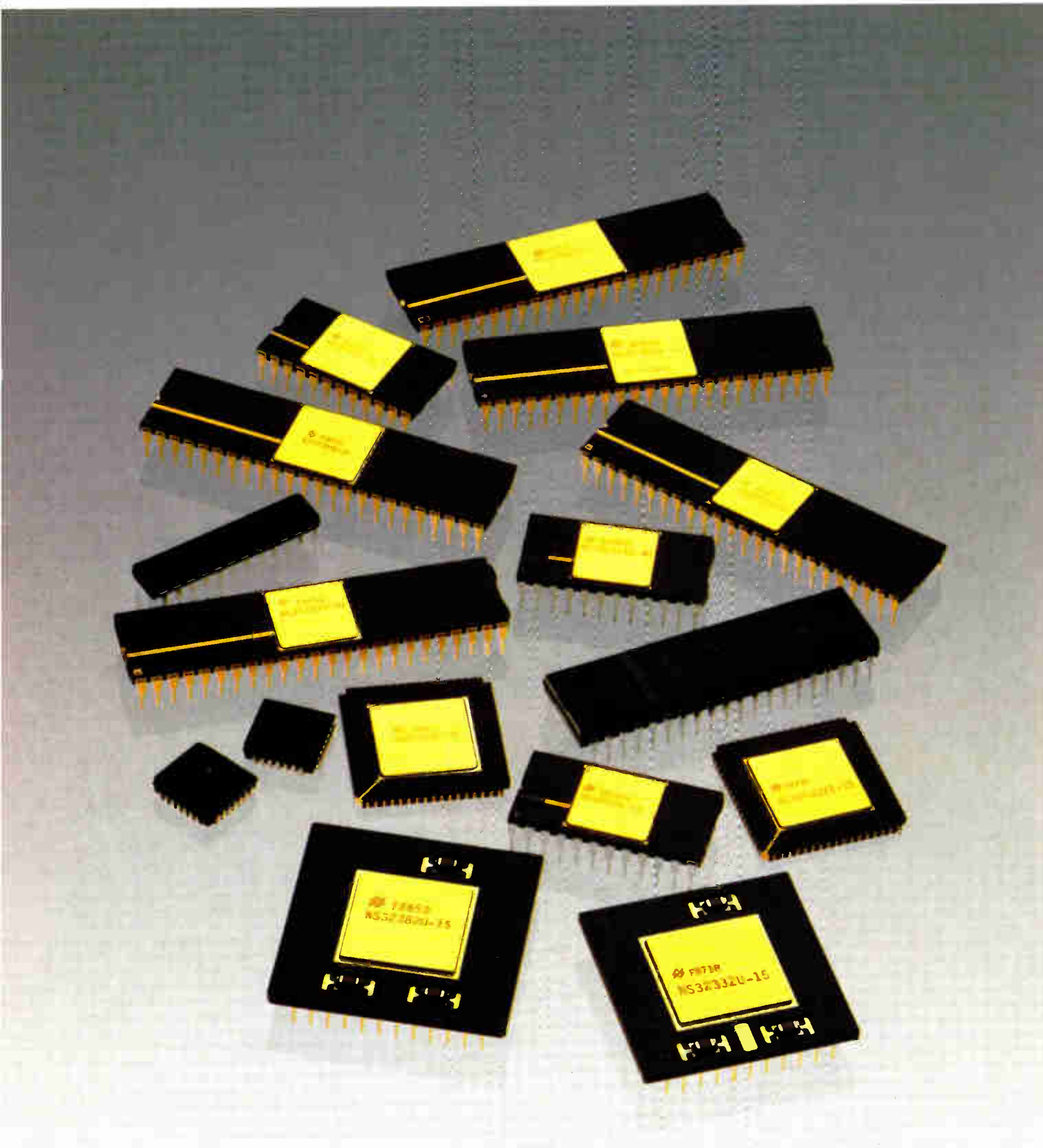
National Semiconductor



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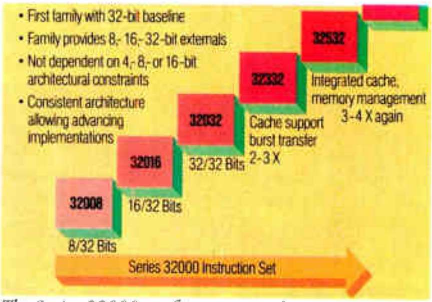

The Series 32000 performance pathway. An integrated family of CPU's with full upward and downward software compatibility.

today, yet it is fully software compatible with the next-generation NS32532.

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Every CPU in our Series 32000® family shares the same 32-bit internal implementation. The same orthogonal architecture. The same highly symmetrical instruction set.

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Any microprocessor, of course, is only as good as the tools that help you put it to work.

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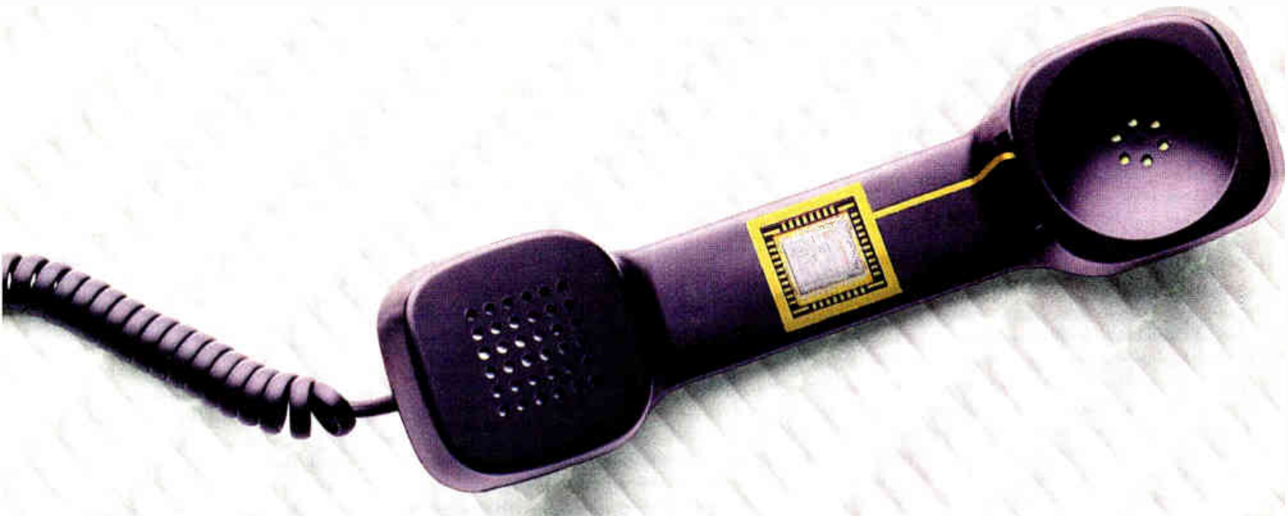
THE $17* DIGITAL TELEPHONE



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April may have been the cruelest month for the English poet T. S. Eliot, but for the journalists who write about what's happening in Europe, the month of August would have to rank right up there. That's the month the continent virtually shuts down for vacation, from government offices to the local bakery. The old saw is that in August, nothing moves in Paris, London, or Munich except American tourists.

GOSCH: Covering Europe isn't easy in the month of August.

But that hasn't slowed John Gosch, our longtime Frankfurt bureau manager. John's primary assignment is coverage of late-breaking technological and business news, but like all our field editors, he is equally at home on the technical side of the fence. So when he contributed two articles to this issue's eight-story cover package, "The frantic search for more speed," beginning on p. 59, the stickiest problem he encountered was the fact that he had to do the reporting during August.

Completing the piece on Hewlett-Packard's time-domain reflectometer on p. 81 didn't present as much of an obstacle as the roundup on p. 62 of what engineers are doing throughout Europe to increase computer performance. For the HP piece, John had to locate the right people at just one company, but for the roundup he had to find them all over the Continent. John surveyed executives in France, Italy, Holland, Sweden, and the UK as well as in West Germany.

"The main difference between covering the European electronics industries during the summer—and especially in August—and the rest of the year is finding the right people to talk to," John says. "Month-long holidays always have been the rule in France, but now this practice has spread to Italy, the UK, and even West Germany. In some cases it took me several days to track down the people I needed to talk to."

However, John—who is the only editor based in West Germany for any U. S. electronic-industry publication—adds that there is something that made the whole project considerably easier than it would have been just a few years ago: the general ease of communication from country to country. "Once I finally managed to get hold of people, getting—and understanding—the information was smooth and easy. Everyone has computers and all the modern communications peripherals to go with them. And, more important," says John, who is fluent in German but not in the other European languages, "everyone speaks English.

"Even in Germany I have yet to meet an engineer who isn't fluent in English. They have to be. For instance, computer language is a mixture of German and English, with most of the technical terms in English."

The two articles by the veteran Gosch demonstrate not only his range but also that of all our news editors. Mainly, our longer technical articles are handled by the experts in New York and San Mateo, who keep abreast of developments in a particular technology or two. But at *Electronics*, field editors wear two hats. In fact, Los Angeles bureau manager Larry Waller contributed to the cover package while doing his usual quota of news stories and newsletters.

Laurence Altman

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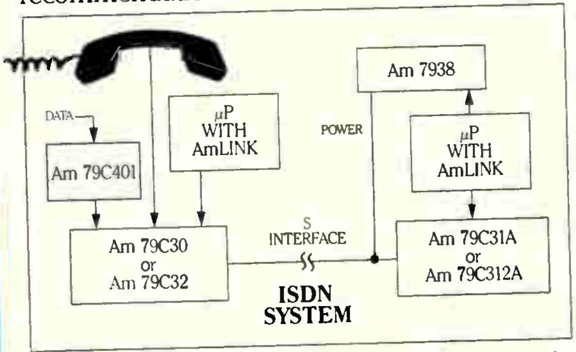
The ISDN chip set that's made for each other.

With AMD's five chip set, everything is included. All designed to work together. And to conform to the CCITT recommendations.



The set is so highly integrated, you won't need extra chips for things like dialing and ringing.

Each of AMD's chips was designed to take advantage of the most efficient technology for its function, including bipolar and CMOS. The set consists of the Am79C30 Digital Subscriber Controller, the Am79C31A/312A Digital Exchange Controller, the Am79C32 ISDN Data Controller, and the Am7938 Quad Exchange Power Controller which works with the Am79C31A/312A. And it won't be long before we'll have protocol devices like the Am79C401 Integrated Data Protocol Controller.

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Once you've got hardware, you'll probably be needing some software. That's easy. AMD has everything from low level device drivers to AmLINK, our LAPD software.

AmLINK implements software interfaces defined in the CCITT Q.921/931 recommendations. AmLINK is modular and it's independent of the operating system, giving you added flexibility. And, because you need it, source code is available.

We also provide well documented development boards that come complete with demonstration software. Understanding the capabilities, flexibility and functionality of complex ISDN chips has never been easier.

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There's one more good reason why you should pick AMD. Our ISDN chips are in field trials with Illinois Bell, Mountain Bell, the Deutsche Bundespost and others. The chips were certified in field trial test beds. And they're still in use today.

Get in touch with AMD for more information. Then get your product off to a great start. And finish.

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Venture capital going into computer-related deals is still running surprisingly strong; second-quarter numbers are up more than 6% over last year, says Technologic's Shaffer

Venture capital going into computer-related deals is still running surprisingly strong. Dick Shaffer, who puts out the *Technologic Computer Letter* from New York, toted it up for the second quarter ended June 30, and it amounted to an increase over the second quarter of the past two years. Dick says $328 million was put into 101 deals, up over 6% from $308 million last year.

The five largest investments in the quarter were made in firms working in integrated circuits or advanced computers. Computer investments: $18 million in Multiflow Computer, a parallel-processor developer; $16 million in Tolerant System, a fault-tolerant-computer builder; and $13.4 million in MIPS Computer, a board-computer maker. ICs: GigaBit Logic, a GaAs chip maker, got $14.9 million, and Cirrus Logic, developers of structured logic arrays, got $11 million.

Cirrus, valued at $70 million, is one of seven chip makers getting money this quarter. Dallas Semiconductor, valued at $160 million, got $5 million; Kopin, a GaAs materials and devices company, received $200,000; Laserpath got $1.2 million for development of quick gate arrays; Gazelle Microcircuits, a developer of GaAs ICs, got $5.5 million; Mosaic Systems, a wafer-scale chip builder, received $4.5 million; and Advanced Power Technology got $5.3 million to develop high-power MOSFETs. Semiconductor entrepreneurs just keep rolling.

Forecasts can get you in a peck of trouble. At the same time, however, they usually make for good reading. Nobody knows that better than Egil Juliussen and Portia Isaacson. Some past forecasts they and others made on personal-computer sales turned out to be a tad on the optimistic side. But that hasn't stopped them; now they're back for another look into the future in their recently published *Computer Industry Almanac.* They predict what a $3,000 office personal computer and a $1,000 PC will look like in 1991 vs. today's comparably priced models.

Their office machine is something: it will have 10 times the computing power, 12 times the main memory (8 Mbytes), nearly 100 times the mass-storage capability (80 Mbyte hard-disk drive), and a 9,600-baud modem. It will run at two to three mips. For only $1,000 in 1991, you should be able to get a 32-bit processor, 4 Mbytes of main memory, and one CD-ROM drive for entertainment and recreation. So order me one.

ROBERT W. HENKEL

GOOD NEWS FOR THOSE WHO DON'T HAVE THE GUTS TO MAKE IT ALONE.

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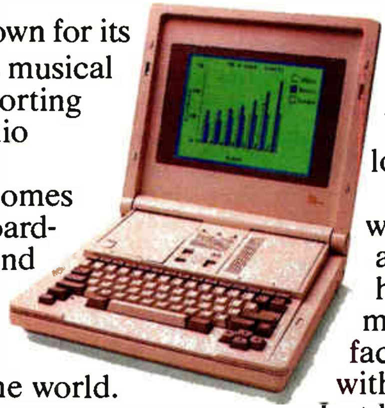
But when it comes to LSI chips, board-level products and computers, Yamaha may be the best kept secret in the world.



Yamaha CRT and flat panel display controllers are in many popular laptop computers.

OUR CHIPS ARE YOUR CHIPS.

For more than 15 years, Yamaha has done some of its best work for companies you probably know.

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Yamaha manufactures sound chips. Graphics chips. Communications chips. And signal processing chips.

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Yamaha can make your next product sound like a cow. Or its graphics display look like a million.

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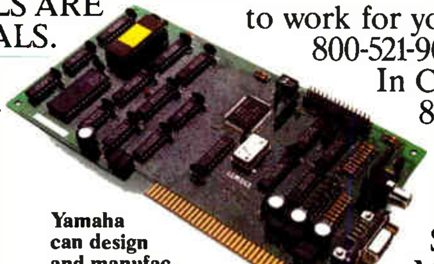

Yamaha can design and manufacture boards with the latest surface-mount technology or less sophisticated assembly techniques.

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Reliability.

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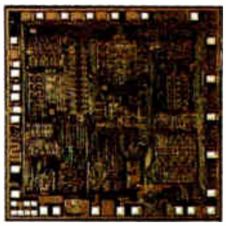

Yamaha engineers use the latest CAD/CAM techniques to customize the functions of a chip.

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PEOPLE

NO 'ELDER STATESMAN' HE, IBM'S POWERS JOINS CDC

ST. PAUL, MINN.

After 28 years in large-system design at IBM Corp., Don M. Powers was afraid at age 53 of being bumped to an "elder statesman" position. "IBM is a youth-oriented company, and it believes in taking people young and growing them. And it uses the older people to groom the younger ones. That was not something I was interested in," he recalls.

So when the offer came earlier this year from Control Data Corp. to manage research and development for that company's high-end hardware, software, and communications products, Powers was quick to take early retirement from IBM and packed his bags for Minnesota. He arrived in St. Paul in May as the new R&D vice president for Control Data's Computer Systems Group. Less than three months later, he's worked out some definite ideas on where Control Data's mainframe product line should go.

Powers's most recent job at IBM was director of development at the Kingston, N.Y., laboratory, where he oversaw work on both the 308X and 309X projects. But he is not looking toward the Hudson Valley for inspiration in his new job. Instead, he's looking just across town toward Control Data's supercomputer subsidiary, ETA Systems Inc., with an eye toward improving Control Data's synergy with this sister operation.

ETA bases its number-crunching hardware on 20,000-gate CMOS arrays from Honeywell Inc., cooled to liquid-nitrogen temperature to obtain performance of 10-billion floating point operations per second. "That technology [ETA's] is certainly one of the most advanced in the industry today," Powers says. "One has to ask why, if you can build a supercomputer with it, you can't use it in a more general fashion across the line." And indeed, if Powers can pull it off, computer users will see ETA-type technology showing up in new Control Data mainframes by 1990.

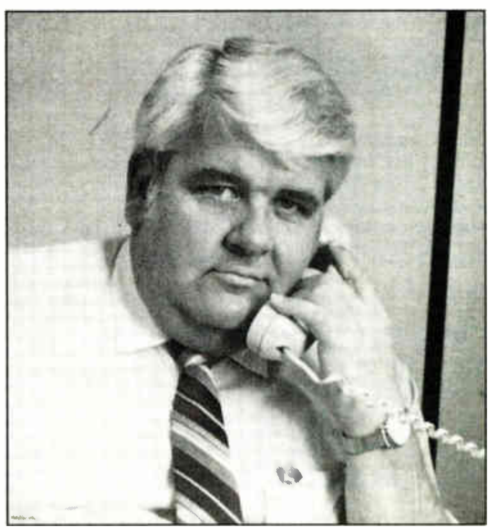
By that time the 20,000-gate CMOS arrays used in the current ETA^{10} supercomputer design will have been replaced by next-generation CMOS arrays in the 100,000-to-200,000-gate range, Powers predicts. And while ETA-style liquid-nitrogen cooling may not be feasible for general-purpose systems that soon, the large CMOS arrays still manage to turn out premium performance when running in air, he says. "I think we can really use that technology, and the challenge I've given my people is to show me why it can't be done."

Meanwhile, Powers says, Control Data will step up the parallelism in its traditional bipolar-based hardware platforms. Its high-end Cyber 180 Model 995E uses two processors, but Powers promises machines over the next few years that will link at least four processors, and possibly more, as a way to keep performance advancing in step with the needs of large-system customers.

Powers plans to emphasize the development of software tools that will let users more effectively employ the power of next-generation systems using larger numbers of tightly coupled processors. Another thrust he will champion involves better silicon compilers, simulation techniques, and other methods to shorten traditional four- to six-year large-system product design cycles.

All this will involve plenty of hard work. But Powers, a Coeburn, Va., native, says he is up to the challenge. He's been involved in large-system design ever since 1959, when he joined IBM following graduation with a BSEE degree from Virginia Polytechnic Institute.

After nearly 30 years of working with mainframes, Powers retains his enthusiasm for tackling the tough problems that go with developing large systems. "This job gives me an opportunity to do that, and to stay young." How long does Powers expect to stay at Control Data? "Probably about 10 years," he answers, "unless I'm having too much fun to quit." *–Wesley R. Iversen*



POWERS: He'll put CMOS in Control Data's high-end computers.

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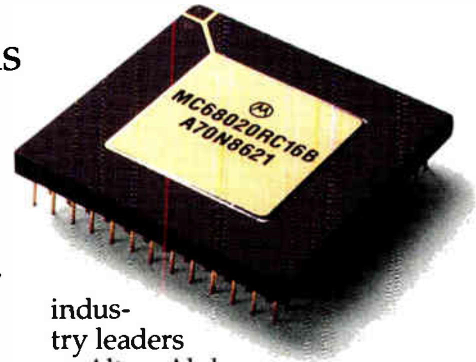


Before millions of people picked Macintosh,™ Apple® picked Motorola's M68000 Family—the brains behind one of the most successful computer products ever launched.

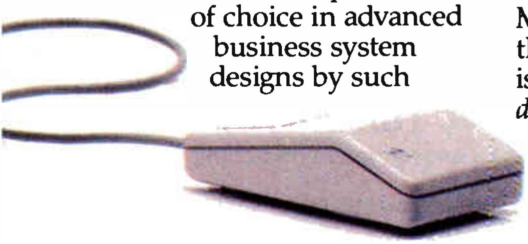
Now Apple has tapped the brainpower of the Motorola MC68020 microprocessor for the Macintosh II, bringing the high performance of a graphics workstation to business desktops everywhere.

72% of all 32-bit systems ever shipped included at least one MC68020. That's more than half a million high-performance systems.

The high-performance business solution.

The MC68020 is not just the overwhelming choice in workstations–it is now setting new performance standards in the office–where it is essential to the computation, graphics and communication necessary for interconnected systems.

While Apple's choice of the MC68020 was a smart move, there's no license on genius: the '020 is the microprocessor of choice in advanced business system designs by such industry leaders as Altos, Alpha Micro, Casio, C.Itoh, Fujitsu, Honeywell Bull, NEC, NCR, Olivetti, Plexus, Ricoh, Sanyo, Sharp, TI, Toshiba and UNISYS.



The graphics solution.

The M68000 family helped Apple implement the visionary "point and click" graphic workstyle that has driven productivity up while driving training costs way down. Businesses of all sizes are discovering dramatic productivity increases in office computing through innovations such as desktop publishing.

The software solution.

Among programmers and designers dedicated to creating the best, most innovative applications, the M68000 architecture has been the leading choice by far–with over *seven million M68000* systems installed since 1979.

Meanwhile, the MC68020, on the market now for three years, is already backed by *two billion dollars worth* of 32-bit software. This is more 32-bit software than all competitive products combined!

The Brain Trust: Where M68000 microprocessors predominate.

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PBX and Telephone Systems
AT&T, Northern Telecom, Siemens.

Fault Tolerant Systems
IBM, NCR, Stratus, Tandem.

Supercomputers
Alliant, BBN, Caltech, Fifth Generation.

Factory Automation
Allen-Bradley, ASEA, Bailey Controls, GM, Mitsubishi, Square D.

Join the Brain Trust.

Challenge us to persuade you of the sound business and technical reasons to join the M68020 Brain Trust. Write to us at Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

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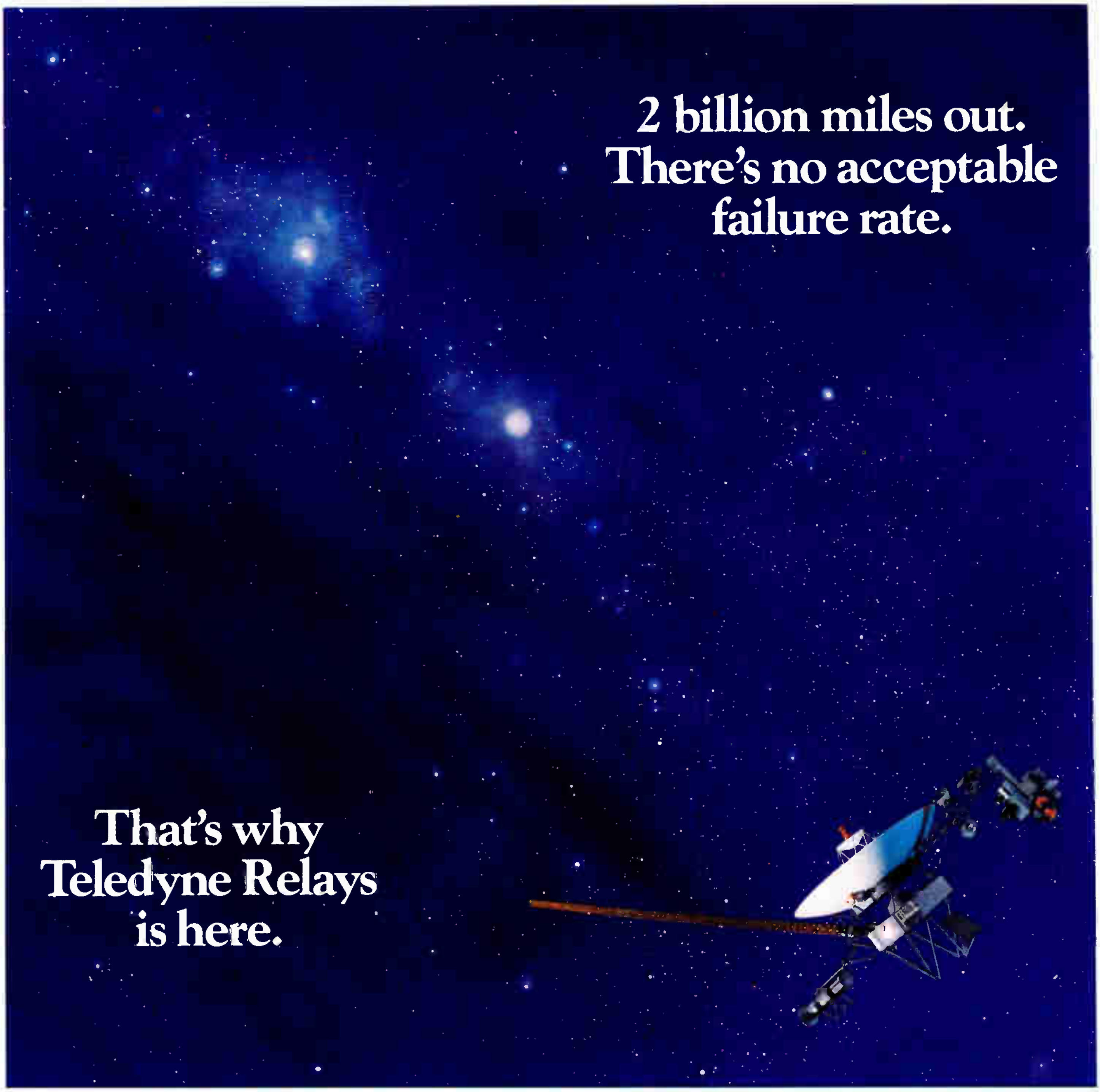

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ELECTRONICS NEWSLETTER

FAA PLANS TO REQUIRE AIRLINERS TO INSTALL COLLISION-AVOIDANCE SYSTEMS

All passenger planes with 10 or more seats will be required to install one of three T/CAS Traffic Alert/Collision Avoidance Systems by 1993, if the Federal Aviation Administration has its way. The agency has published a Notice of Proposed Rulemaking in the Federal Register in August, and companies in the airline and avionics industries now have four months to respond to the notice. At least one FAA official expects the industries to complain that the notice does not afford them enough time to install the systems in the 4,500 affected planes. The ruling would require all air carriers with 30 or more seats to install a T/CAS-2 system within three years, while commuter craft with 10 to 30 seats would have five years to install the less advanced T/CAS-1 system. Larger carriers would be encouraged to upgrade to T/CAS-3, which is currently under development, when such systems become available in the mid-1990s. T/CAS-1 generates traffic advisories on the relative range, bearing, and altitude of aircraft that pose a potential threat to a plane's safety. T/CAS-2 adds a vertical maneuver advisory to T/CAS-1's capability, instructing pilots whether it is safest to stay level, climb, or descend, and at what rate to proceed. The FAA Technical Center in Atlantic City, N. J., is currently completing engineering work on T/CAS-3, which will add a horizontal maneuver capability to the T/CAS-2 system. □

ANTI-DIGITAL-AUDIO-TAPE RECORDER BILL MOVES CLOSER TO LAW

A bill that would outlaw the manufacture and sale of digital-audio-tape recorders unless they are equipped with a device that prevents copying of prerecorded music has cleared its first hurdle on the way to becoming a law. The Digital Audio Recorder Act of 1987, which would remain in effect for three years, got through the House Subcommittee on Commerce, Consumer Protection, and Competitiveness in August, and the House Energy and Commerce Committee is expected to act on it this month. A second version of the bill is in the Senate Communications Subcommittee. The recording industry opposes the introduction of DAT recorders in the U. S. because it claims the technology could be used to pirate existing recordings. But hardware manufacturers have refused to bow to such pressure, and one company—Marantz Co. of Chatsworth, Calif.—says it will introduce a DAT recorder in October [*Electronics*, June 11, 1987, p. 24]. Meanwhile, a National Bureau of Standards study on the copy-code system's effect on DAT audio quality may well determine DAT's fate. The House bill includes a provision to remove the requirement should the Secretary of Commerce conclude that the chip degrades sound quality. □

HP PORTABLE PCs FINALLY BELLY UP TO THE IBM STANDARD

Hewlett-Packard Co. will at long last fully acknowledge the IBM Personal Computer standard in its portable PC offerings later this month, when it will ship a pair of systems that offer the functionality of IBM Corp.'s desktop PS/2 model 30 in a briefcase-size package. The HP Portable, introduced in early 1984, and early HP desktops were not IBM-compatible; the more recent HP Vectra desktops do meet the IBM standard. The new Portable Vectra CS Personal Computers are similar in packaging to IBM's clamshell-design Convertible, but the Palo Alto, Calif., company did not squeeze down the keyboard, instead providing a full-function keyboard with a numeric keypad. HP also made room inside the case for four option slots compatible with PC/XT slots but requiring smaller cards. The base model has two 1.44-Mbyte 3½-in. floppy-disk drives; on the model 20, a 20-Mbyte hard disk replaces one floppy. The low-end unit, priced at $2,495, includes 640 Kbytes of memory and runs 10 hours on a battery charge. The model 20 sells for $3,595 and runs four hours per charge. Both weigh 17.6 lbs. Their 8086-compatible CMOS processor from NEC Corp. runs at 7.16 MHz. □

ELECTRONICS NEWSLETTER

IS JAPAN'S SUPERCONDUCTIVITY INITIATIVE REALLY SUPER?

Japan's superconductivity research effort, which includes the creation of an International Superconductivity Center and other high-profile programs, may be less than it appears to be. The Ministry of International Trade and Industry has changed its policy and is no longer funding large-scale applications development programs as it has in the past, but instead is focusing on smaller contract grants for basic research. MITI's strategy is to control the rights to research that it funds. Patents coming out of large-scale development historically belong to the research facility, but patents derived from contract research belong to the government. The Science and Technology Agency, however, is funding some major materials research programs—including one for a superconducting magnet with a 40-tesla field and another for an electron-beam microscope with a resolution of 1 Å. □

BRITISH TELECOM–DU PONT TEAM COMES ON STRONG IN OPTOELECTRONICS

Anyone tracking the fast-growing optoelectronics market should keep a sharp eye on BT&D Technologies Ltd., which melds the optoelectronics expertise of two heavyweights, British Telecom plc and the Du Pont Co. of Wilmington, Del. BT&D market-development manager Colin S. Munday has set out to capture more than 10% of the market, which he figures will grow from $420 million this year to just over $1 billion by 1991. The company will ramp up production at its chip-making facilities in Ipswich, UK, this month and next; it already has samples of couplers, "logic-to-light" transmitter modules, and "light-to-logic" receiver modules for 1.3- and 1.5-μm wavelengths. BT&D is also developing other products, including a 25-dB optical amplifier. □

IGNORANCE IS NOT BLISS, SAYS REPORT ON U. S. ENGINEERING

Engineering curricula and engineers in the U. S. are ignoring foreign technology and innovation, to the detriment of the U. S. economy and technology base, says a report prepared for the National Science Foundation by the National Academy of Engineering. The report warns that by not keeping abreast of developments abroad, the U. S. technical community risks losing its place among world leaders in electronics and other technologies. Technological protectionism, moreover, "is not a sustainable path . . . since technology inevitably diffuses." The report credits Japan's willingness to learn from others for its rapid rise in engineering expertise. More than 13,000 Japanese students attended U. S. universities in 1984, but only 730 Americans went to study in Japan. The report stresses that the NSF, other organizations, and corporations must encourage international technical cooperation for the U. S. to regain its competitive edge. □

MOSTEK PUTS ITS DELAYED 16-BIT MICROCONTROLLER ON HOLD AGAIN

The pending merger of Thomson Semiconducteurs SA and SGS-Microelettronica SpA is starting to affect Thomson Components-Mostek Corp.—at least in one instance. The Thomson subsidiary's 68HC200 16-bit microcontroller chip, which has already been redesigned once and just made its second debut in April, is now being shelved again, while details of the merger are completed. The 68HC200 could find its way back to the market for a third try in 1988, however. Managers at Mostek's Carrollton, Texas, operation are polling customers to determine if there is demand for the chip even though it has no alternate source. The part has evolved from an n-channel design in 1983 to its current CMOS implementation, which has higher processing speeds and a modular die layout for easier tailoring into custom microcontrollers [*Electronics*, April 2, 1987, p. 22]. □

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PRODUCTS NEWSLETTER

XILINX JUMPS PLD DENSITIES WITH 9,000-GATE ARCHITECTURE

Xilinx Inc.'s latest SRAM-based programmable-logic-array architecture boosts densities as high as 9,000 equivalent NAND gates—which means a quantum leap in the complexity of designs that PLDs can handle. The 9,000-equivalent-gate density is three to four times that of any PLD available, and it adds punch to the PLDs' threat to conventional logic arrays that require design cycles of months instead of weeks. Unlike semicustom gate arrays, PLDs don't have to be sent to the vendor's facility for masking; they can be programmed electrically by the user. The first device is the XC3020, which has a 70-MHz toggle-rate and will allow densities of up to 2,400 equivalent NAND gates. Fabricated using a double-metal 1.2-μm CMOS process, the XC3020 is now available in sample quantities and will be in volume production in early 1988. Pricing in 10,000-unit quantities will be under $20. The 2,400-gate device will be followed later this year with a 9,000-gate device. During 1988 the San Jose, Calif., company will fill out the family with logic-cell arrays of 2,700-, 4,000-, and 6,000-gate densities. □

16-GIGABYTE DISK SYSTEM TO COST ONLY A THIRD AS MUCH AS ITS RIVALS

Look for competition to heat up in the mass-storage market for mainframe computers with the launch of a 16-gigabyte storage system from Amperif Corp. that costs as little as $10/Mbyte—about one-third the per-unit cost of systems from IBM Corp. and Control Data Corp. The 9000-IIB uses Fujitsu Ltd.'s 1-gigabyte, 8-in. Swallow 5 disk drives to attain its price advantage without skimping on performance. Besides 16 gigabytes of rotating memory, it has a 32-Mbyte memory cache and up to 90 Mbytes of system memory. Using a proprietary caching scheme, Amperif has reduced cache access time to 0.5 ms and raised cache and system-memory transfer rates to 9 Mbytes/s. The rotating storage has an average seek time of 16 ms, a 3-Mbyte/s data-transfer rate, and a space-saving footprint of only 12 sq. ft.—one-fifth the floor space required for an IBM 388-/3380E system. In another technology breakthrough, the 9000-IIB's controller lets up to eight central processing units simultaneously access and share data when used with a Unisys 1100-series mainframe, says the Chatsworth, Calif., company. Available now, the 9000-IIB with 16 gigabytes of rotating memory and two controllers costs $150,000. A 32-gigabyte, dual-cabinet system costs about $600,000. □

AMD'S SRAMs USE HALF AS MUCH STANDBY POWER AS THE COMPETITION

High-speed memory designers can save up to half the power in standby mode over competing chips with Advanced Micro Devices Inc.'s 64-Kbit CMOS static random-access memories. The power edge is significant in military applications, where 70 to 80 of the devices might be packed on a single board, or in extending battery life in commercial applications using battery backup, says the Sunnyvale, Calif., company. The Am99C164 and Am99C165 are organized as 16 K by 4 bits. They feature standby-mode current drains of 0.3 mA in the military versions and 0.1 mA in commercial versions, compared with 0.6 mA and 0.15 mA, respectively, for the competition. In the operating mode, the standard-power versions consume a maximum of 605 mW, and the low-power versions consume 20% less. The third chip, the Am99C88H, is an 8-K-by-8-bit device tailored for cache-memory applications. The chips complete AMD's high-speed 64-Kbit SRAM family. Commercial versions boast 35-ns access times; military chips have 45-ns access times. Available now, the Am99C164 has chip-enable and write-enable controls and costs $25.50 each in 100-unit quantities. The Am99C165 adds an output-enable mode and costs $28.30 each. The Am99C88H cache-memory chips are $20 each. □

PRODUCTS NEWSLETTER

TRIMMER CAN SURVIVE A 300°C SOLDER BATH

An injection-molded, proprietary thermoset-plastic package gives Bournes Inc.'s Model 3314 trimming potentiometers the structural integrity to survive 20-second dips in 300°C solder baths. Competitive trimmers experience 50% to 100% failure rates at temperatures above 270°C. The Model 3314's survivability lets printed-circuit-board manufacturers who want to move into the market for surface-mounted products use their existing double-wave soldering systems, instead of having to invest in vapor-phase and infrared systems that operate at a lower temperature. Because trimmers have moving parts and therefore are more susceptible to heat failure, they have blocked extensive use of double-wave soldering in surface-mount production, says the Riverside, Calif., company. Since the Model 3314 is just 4.45 mm square and 2.55 mm high, it permits dense board designs and allows boards to be stacked closer together than with conventional trimmers, which are 5 mm high and take up twice the board area. The devices are available in 17 resistances from 10 Ω to 2 MΩ, with a tolerance of ±1%. All versions cost $1.09 each in quantities of 1,000. □

ALPHA DATA'S FIXED DISK TRIPLES DATA-TRANSFER PERFORMANCE

The race for faster data-transfer rates for fixed-disk storage devices is taking a new turn. Using eight parallel channels instead of single-channel access, Alpha Data Inc.'s 520-Mbyte Atlas 520 drive achieves 15 Mbytes/s—more than three times the rate of conventional systems. Multiple-channel drives have been tried before but have fallen victim to disk-flaw problems: if one channel encounters a flaw, the others must wait while it runs through an error-correction scheme that wastes milliseconds. The Chatsworth, Calif., company sidesteps that problem with 76 recording heads, four of which are spares. During factory test, the locations of disk errors are stored in programmable read-only memory. Then data that would have been written on a flaw is transferred to an unflawed area read by one of the spare heads. Since the reallocation is performed at electronic rather than mechanical speeds, the average disk-access time is 18 ms. The long-term average access is less because of the exceptionally large number of heads. The Atlas 520 fits into a standard 19-in. rack. It is available 90 days after order for a projected price of $15,000 to $20,000. □

AT&T ISDN CHIP REPLACES A BOARD-LEVEL PRODUCT, COSTS 75% LESS

AT&T Co.'s newest addition to its integrated-services-digital-network product line replaces a board-level product that requires far more space and costs at least 50% to 75% more than this single-chip solution. The T7252 interfaces a digital local switch, PBX, multiplexer, or concentrator to ISDN, an evolving system that will tie voice, data, and video signals into a single high-speed digital network. Another advantage the T7252 offers designers is versatility. While the board products had to be customized for each given switch, the T7252 is fully programmable, allowing it to be used with equipment from multiple vendors. Available now, the T7252 costs about $14.50 in 1,000-unit lots. □

FIBER-OPTIC MULTIPLEXER QUADRUPLES CHANNELS ON ONE DUPLEX CABLE

By interfacing with four IBM Corp. 3174 or 3274 comunications controllers instead of one, Pilkington Communications Inc.'s model 3128 fiber-optic time-division multiplexer quadruples the number of channels available over a duplex fiber-optic cable. Each of the cluster controllers handles up to 32 terminals. The model 3128 handles cable faults by performing automatic rerouting and can distribute messages among the controllers, says the Simi Valley, Calif., company. It also interfaces with the Telex 274 controller. Available now, the multiplexer sells for $2,650 and up. □

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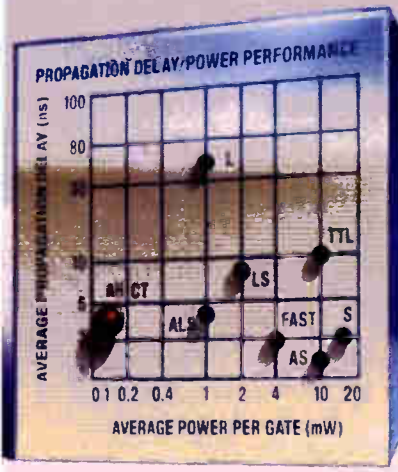

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CMOS LOGIC KS74AHCT Part Types

Gates and Inverters	
00	20
01	21
02	22
03	27
04	30
05	32
08	51*
09	58*
10	86
11	132*
12	133*
14*	266

Buffers & Line Drivers	
125*	367
126*	368
210	465*
240	466*
241	467*
244	468*
365	540
366	541

Flip-Flops	
73	399*
74	534
76	564
78	574
107	670*
109	794*
112	821*
173*	822*
174	823*
175	824*
273	825*
374	826*
377*	

Latches	
75*	793*
77*	841*
259	842*
373	843*
533	844*
563	845*
573	846*

Transceivers/Registered Transceivers		
242*	643	652*
243*	645	658*
245	646	659*
640	648	664*
	651*	665*

Counters		
160	190	590*
161	191	591*
162	192	592*
163	193	593*
168	390*	
169	393	

Decoders/Encoders		
42*	148*	238
138	154*	239
139	155*	

Multivibrators		
121*	123*	423*

Multiplexers	
151	253*
153	257
157	258
158	352*
251	353

Shift Registers	
164	299*
165	595*
166	596*
194	597*
195*	

Arithmetic Circuits	
280*	680*
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679*	

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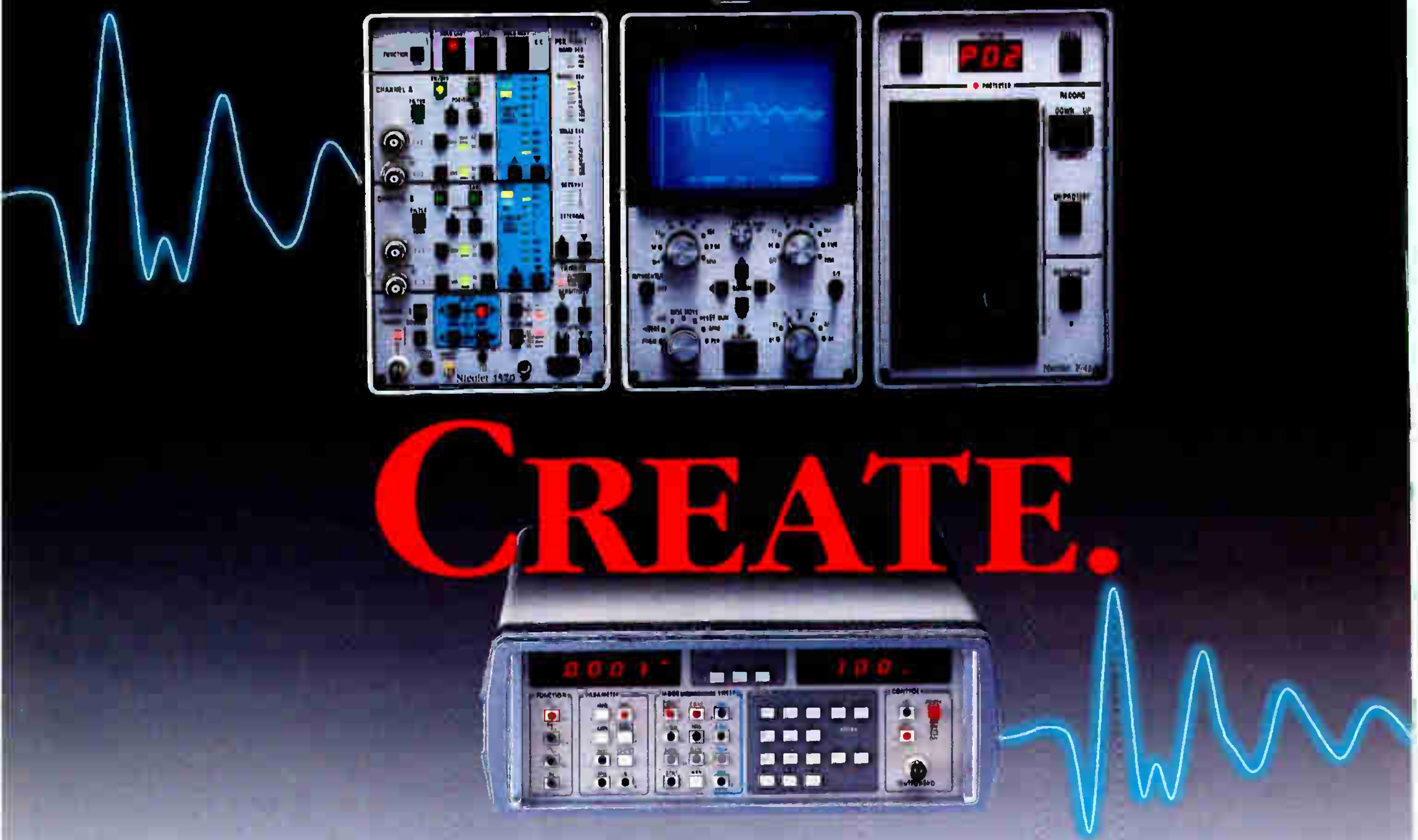

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Electronics

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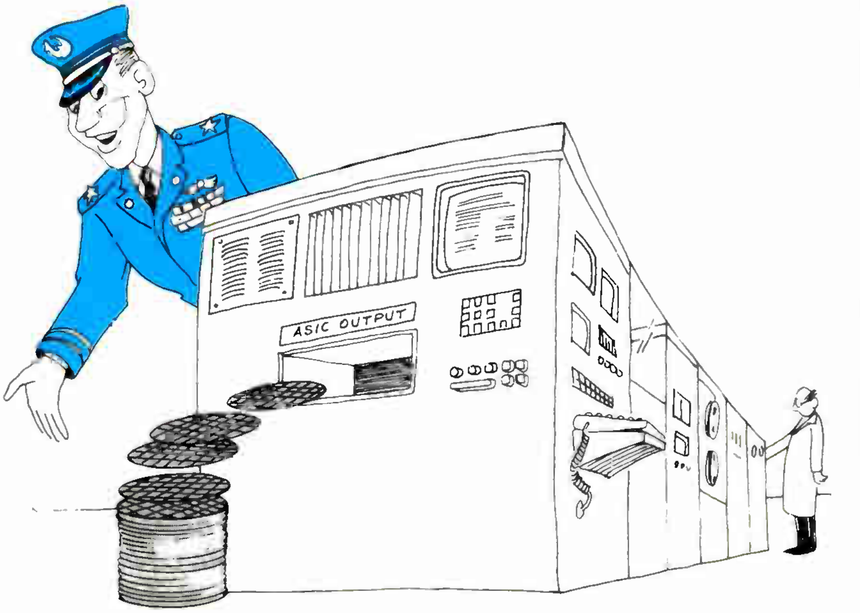


DAYTON, OHIO

The Defense Department wants the ASIC manufacturing line of the future now, and it is casting a $75 million challenge at the U. S. semiconductor industry to build it. The new initiative is known as Microelectronics Manufacturing Science and Technology, and if the Pentagon winds up with even part of what it's hoping for, the result could amount to nothing less than a revolutionary change in the way that military application-specific integrated circuits are manufactured. Making the program even more significant would be the eventual transfer of technology to the commercial sector.

Proposals are due Sept. 28 on the five-year MMST program, which has a strong chance of getting additional funding as the project progresses. The effort will be paid for by the Air Force, the Defense Advanced Research Projects Agency, and perhaps other DOD agencies. An initial contract or contracts should be awarded next February.

FAST AND FLEXIBLE. The MMST focus is on extremely flexible, quick-turnaround, low-volume military ASIC fabrication, unlike the proposed Sematech chip-manufacturing consortium, which will concentrate on high-volume memory-chip production methods [*Electronics*, May 28, 1987, p. 33]. And at a pre-proposal bidders' meeting held in late August at Wright-Patterson Air Force Base in Dayton, Ohio, MMST sponsors laid out a wish list for a futuristic chip-factory demonstration that surprised many contractors by its aggressiveness.

"The extreme view of what they're looking for is that you walk up to the factory and a robot hand reaches out through the air lock, takes your tape, and tells you what time to come back that afternoon for your chips," observes George A. Anderson, director of the Very High Speed Integrated Circuits submicron program at Honeywell Inc.'s Solid State Electronics Division in Plymouth, Minn.

And as noted by Ronald Bruce, manager of government programs at the United Technologies Microelectronics Center, Colorado Springs, Colo., "It's going to take teaming by three to five major corporations to respond to this, because no one company can do it all" (see "Bidders scramble to get their acts together," p. 32).

Indeed, the requirements list for the chip-fabrication line the Air Force expects to have at the end of the program holds back nothing in its aggressive use of high-risk technology. "Essentially, what we're trying to do is take a new approach to cleanliness, and also to capitalize on a number of rather innovative processes that have been demonstrated separately in the laboratory to see if they're integratable into a new kind of process line," says Richard A. Reynolds, director of the Darpa Defense Sciences Office.

Reynolds and other top program brass are reluctant to discuss their objectives in detail, citing security, among other concerns. But conversations with potential bidders and sources close to the project turn up the following picture.

The DOD is looking for a military ASIC fabrication capability essentially free of people and paper. It would emphasize extreme flexibility and fast turnaround on dense military ASICs with minimum geometries of 0.5 μm and smaller. Operating totally under closed-loop, real-time control, the facility would have expert systems making all process adjustments, based on inputs from yet-to-be-developed sensor technology. It might integrate any of a variety of advanced resistless or dry-resist processing techniques, some of which exist today in the U. S. only in a few government and university laboratories.

Wafers would be held in a controlled atmosphere from start to finish, perhaps moving through a vacuum line and a series of load locks from one processing chamber to another. Any so-called *in situ* "selected area processing" or "limited reaction processing" technique might be employed in each chamber. A focused laser spot on the order of 1 μm in diameter could be used in appropriate chamber atmospheres to promote differing localized reactions on a wafer, causing deposition or etching, for example, or writing discretionary metalization patterns directly, without the need for a resist or masking process. The same kind of things could be done using ion beams or electron beams.

The envisioned MMST approach probably would not be suitable for high-volume manufacturing efforts such as that planned by Sematech. But it should be ideal for promoting the Air Force's goals: extremely fast turnaround on high-yield first-pass wafers, and high flexibility for short runs of low-volume military devices, program sponsors say. "They want days for processing turnaround, where we now talk weeks," notes one potential bidder.

Further, the MMST fab line would allow back-to-back mixing of low-volume wafer runs of differing processes, such as CMOS and bipolar silicon, without equipment changeover. And ideally, it would not be confined to silicon. "This is a great opportunity to really make a revolutionary change in the way we go about fabricating microelectronics, because this would be applicable to gallium arsenide, mercury cadmium telluride—or even superconductors, if anybody ever learns how to make ceramic thin films that have high T_c's [temperature coefficients] and then eventually learns to make tunneling Josephson junctions on them," according to Darpa's Reynolds.

What's more, Reynolds adds, "If this works, it could substantially reduce the cost of a submicron fab facility and also reduce the size of the facility that you could build that would be viable." Roughly speaking, the MMST approach might reduce by half the square footage required for a comparable chip fabrication capability that uses today's state of the art, he says. It would also reduce the cost per square foot by a factor of four. *–Wesley R. Iversen*

BIDDERS SCRAMBLE TO GET THEIR ACTS TOGETHER

A gang of chip makers, defense contractors, artificial intelligence houses, and equipment vendors are scrambling to choose sides and decide how to approach the Defense Department's ambitious new Microelectronics Manufacturing Science and Technology program.

Some potential players say they were caught by surprise last month when the Air Force asked for proposals. Those proposals are due Sept. 28. Others, who knew the document was coming, admit surprise over the program's scope.

The MMST thrust calls for demonstration by 1993 of a highly advanced military IC fabrication line. If the program meets its goals, it will require development of a range of risky and unproven technologies. These include new approaches to cleanliness, novel processing techniques, and closed-loop real-time process control, with all their attendant expert-system software, new sensors, monitoring systems, and data-handling capabilities.

Many believe the program objectives are, in fact, too broad for any but the very largest companies to tackle alone. As a result, contractors have been burning up the phone lines in recent days as they feel out prospective teammates. Executives at Honeywell, TRW, and Westinghouse all confirm plans to bid on the effort, though they won't reveal potential partners. And industry sources say Texas Instruments will bid as an independent prime contractor, though the Dallas company itself isn't talking.

The Air Force is encouraging potential prime contractors to involve domestic equipment vendors as subcontractors or team members, to assure that equipment later becomes available to U. S. industry. "Technology transfer is a very large issue," says William J. Edwards, director of the electronic technologies division at the Air Force's Wright Aeronautical Laboratory in Dayton, Ohio, which is managing the program. "We're very much concerned about getting whatever is developed in the program out to the defense industry and the merchant microelectronics industry."

Another unusual element of the program is the use of the Program Research Development Announcement approach to encourage creativity among bidders. Unlike the conventional procedure, which involves a formal request for proposals with a specific statement of work, PRDA program contracts are not written until after the proposals are reviewed. The process allows work to be tailored to innovative industry ideas, as well as give and take on program goals. Bidders may submit proposals for all or part of a project, and the Pentagon can choose all or part. *–W. R. I.*

INTEGRATED OPTOELECTRONICS

THIS POLYIMIDE COULD GIVE OPTOELECTRONICS A PUSH

BLOOMINGTON, MINN.

Optical interconnections built right into electronic packaging—using compatible materials and processes—could go a long way in pushing optoelectronic technology into real-world applications. Now researchers at Honeywell Inc. say they have a polyimide material that promises to do just that.

The material is proprietary, and Honeywell researchers are close-mouthed about the commercially available starting ingredients they used to create it. But what makes it different from other polymers used as thin-film dielectrics in electronic packaging is that optical waveguides etched into it can withstand the high-temperature processes of package fabrication.

"The breakthrough is that we've used standard electrical packaging material," says Charles T. Sullivan, principal research scientist at the Honeywell Physical Science Center in Bloomington, Minn. "This opens up the possibility of putting both electrical and optical interconnects on the same substrate."

Also, the waveguides can be bent through 90° corners without substantial optical attenuation, providing for extremely dense optical interconnect routing, Sullivan notes.

Until now, polyimide waveguides fabricated by others, including IBM Corp., have shown suitable low-loss operational characteristics after low-temperature processing. The problem comes in trying to keep the optical portions stable when temperatures are raised to the 300°-to-350°C levels needed to completely cure the material for stable electrical operation and subsequent soldering.

"There's a host of good organic light guides that just go to pieces when the temperature goes up," says John D. Crow, manager of optoelectronic interconnect technologies at IBM's Thomas J. Watson Research Center, Yorktown Heights, N. Y. Crow blames residual solvents and trapped water within the material. These liquids can boil out, creating voids and pinholes that act as light-scattering centers in the waveguide.

As a rule of thumb, waveguides suitable for integrated optics must exhibit light loss of 1 dB/cm or less, researchers say. IBM last year reported on

SULLIVAN: "The breakthrough is that we've used standard electrical packaging material."

waveguides formed in polyimide that exhibited 0.31 dB/cm losses after drying at 90°C. "And we were able to take it up to about 200°C and still have a pretty good light guide, with losses in a range around 0.5 dB/cm," Crow says. At higher temperatures, however, waveguide loss rose to unacceptable levels.

By contrast, Sullivan says, Honeywell has experimented with temperatures as high as 350°C and produced optical losses below 0.5 dB/cm. Losses were as low as 0.08 dB/cm when the material was dried at about 100°C. When bent through a 90° turn, the waveguides showed losses of about 1 dB per corner, a figure that Sullivan believes can be significantly improved with additional work. The Honeywell tests used wavelengths in the 850-nm range.

Honeywell officials are keeping mum about how they did it, saying only that the key is the combination of the polyimide used and the interconnect fabrication techniques employed. The material itself has already been proven for future high-speed multilayer electronic packaging applications, Sullivan says. And the waveguide-fabrication techniques are all compatible with commonly used electronic packaging processes, he says. A thin layer of the Honeywell material can be spin- or spray-coated onto virtually any common substrate material, and the waveguides are formed using an etching technique.

The Honeywell researcher cautions that results using the polyimide waveguides are still "fairly exploratory." But packages using the material could begin showing up in production optoelectronic systems within five years, maybe sooner, Sullivan believes. If continued research efforts pan out, "this may very well have a significant impact on the potential utilization of optical transmission media in high-density electronic packaging." *–Wesley R. Iversen*

COMMUNICATIONS

A RACE TO DESIGN DECODE CHIPS FOR DBS

LONDON

With the first of a series of European TV direct-broadcast satellites scheduled for launch 12 months from now, European semiconductor companies are scrambling to develop the new circuits that will be needed to decode the satellite signals. The latest entry, one with an approach that could win a large share of the market, is emerging from an effort that combines the semiconductor muscle of Philips and Plessey plus the ingenuity of a small Norwegian design house.

The home-TV share of the decoder market, estimated at 1.4 million sets, is attractive enough. But the first big chunk of the market will probably be for data receivers at the front end of mainframe and minicomputer systems. In the UK, companies that must update data at widespread offices daily on a near-instantaneous basis are now using spare teletext lines. Those companies—banks, finance houses, large retail chains, and the like—should find the new DBS service, with its encryption features and 20-MHz data rate, even more attractive.

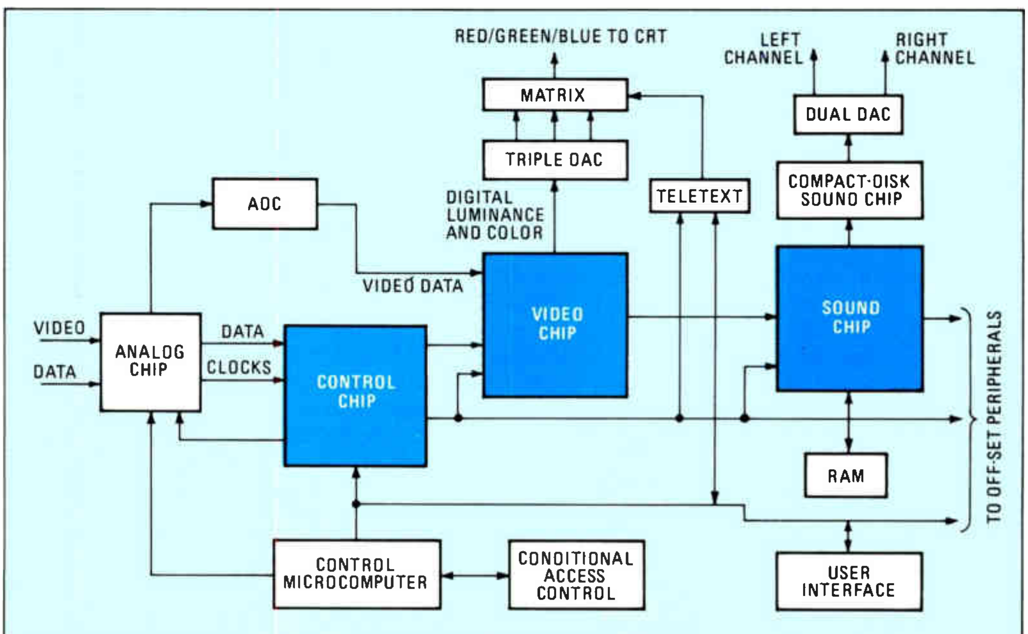
But the chip-design job isn't simple: broadcasters have not yet defined the broadcast signal specifications, and to further complicate matters, at least three standards will be in use by different satellites. All are variants of the original MAC (for multiplexed analog components) system [*Electronics Week*, March 11, 1985, p. 38]. The Scandinavians will use a version called C-MAC, the British have opted for D-MAC, and the West Germans D2-MAC.

The differences among the standards are subtle. C-MAC's sound bursts are phase-shift modulated; D-MAC's are frequency modulated. D2-MAC's data rate is 10.125 Mbit and D-MAC's is twice that; as a result, D2-MAC offers the equivalent of eight sound channels to D-MAC's four. Also, D-MAC implementations provide for encryption and D2-MAC's do not. Finally, D-MAC is designed to be upgraded to provide a high-definition TV picture using a 625-line noninterlaced format.

Already, ITT Corp.'s German subsidiary, Intermetall GmbH, has announced a D2-MAC decoder as part of its Digivision chip set for digital TV. But Philips and Plessey have chosen a different route.

The British-Dutch combine will make a chip set that can decode each standard. The work stems from a C-MAC design by a small company in Oslo, Nordic VLSI. Nordic has licensed Philips' Elcoma Division and Plessey Semiconductors Ltd. to produce the silicon and the glue chips needed to make a system. They have built a 13-chip decoder labeled Multimac (see figure).

THE HEART. Three devices—the control, video, and sound chips—form the heart of the decoder and are Nordic designs. Plessey will make them, initially using its 2-μm CMOS process. The remainder of the chips are a mixture of existing circuits from both Philips and Plessey, along with new designs. For example, the analog chip is a dedicated bipolar design called Macan from Philips, and the teletext decoder is being adapted by Plessey from a production model.



UNLOCKING THE DATA. In the Multimac chip set, the control, video, and sound chips are the heart of the decoder. The set is being developed by Philips, Plessey, and Nordic, a small Norwegian company.

In addition to handling C-MAC, the analog chip demodulates the 479-MHz intermediate-frequency signal from a receiver's tuner down to the 20.25 MHz baseband for D-MAC or 10.125-MHz base for D2-MAC, slices the data, and recovers clock and other signal elements required for the control chip to route the separate signal elements to the video and audio control chips. The compact-disk sound chip converts the analog signal to digital. The whole process is overseen by two microprocessors, one 16-bit and one 8-bit, which are currently supplied by Philips. In production models, sound chips would be cascaded to provide the required number of stereo channels for multilanguage sound tracks or data.

Working models are due by November, says Peter Haywood, Plessey's industrial products marketing manager, with a final demonstration model of the complete board by next March. Working models should appear by September. Haywood won't estimate a price. His only worry now, he says, is that the satellite launchers prove reliable. "If the birds fly, then we are in business," he says. *–Peter Fletcher*

AUTOMATIC TEST

MEGATEST AIMS AT 'GAP' IN ATE MARKET

SAN MATEO, CALIF.

The only niche in the automatic-test-equipment market that showed any growth at all last year was at the high end—testers priced above $300,000. But the market won't stay skewed in that direction for long if Megatest Corp. has its way.

The San Jose, Calif., company expects to cut into sales of the expensive systems with its new $135,000 Genesys II, which it will start shipping next month. In fact, Howard J. Ignatius, marketing manager for the system, believes the ATE market will be nearly evenly divided between systems above and below the $300,000 line by 1989.

By comparison, Prime Data, a San Jose market-research firm, says that in today's market, 61% of the systems sold are on the high end. Sales in that segment soared last year to $116 million, 35% above the 1985 level, while ATE sales overall fell to $175 million, from $260 million in 1985.

Ignatius believes that the pell-mell race to produce expensive testers has left a gap in the market for a moderately priced system with performance near that of the high-end models. That's the target of Genesys II, which offers many of the features of the more costly systems from such competitors as Advantest America, Sentry Schlumberger, and Teradyne.

MORE CHIPS. A prime reason for the spiraling cost of testers is the increase in the number of memory components that can be tested in parallel. Most of the high-priced systems can test 32 chips at a time, and the theory is that test cost per chip is lowered as a result.

But there is a mechanical limit to this approach, says Ignatius. Chips can be tested in two places: on the wafer, by the manufacturer; or in the package, by the manufacturer, the purchaser, or both. "Wafer probers are expensive," he says. "You can only put four at the optimum, eight maximum, on a given wafer." That leaves 24 channels idle in wafer testing.

"Moreover," says Ignatius, "to test eight [chips] in parallel requires the memory maker to put all the input/output pads on one side of each die to allow probers access to the chips—an added step that many will not want to make."

While "our competitors decided to concentrate on the final test area," the package, Ignatius says Megatest has "a solution that addresses both" chip and package testing. The Genesys modular test head can handle four or eight dice in parallel during wafer testing. The head is configured in groups of four dice to handle 4, 8, 16, or 32 RAM chips, or 2, 4, 8, or 16 nonvolatile memory chips in parallel.

In package testing, the Genesys II can simultaneously test 16 dynamic random-access-memory chips with capacity up to 16-Mbits long by 10-Mbits wide. It can also test eight erasable programmable read-only memories or other nonvolatile memory in parallel.

This capability anticipates a continuing rapid rise in memory-chip capacity. "We see demand for production testing of 1-Mbit RAMs and nonvolatile memory chips today; 2-Mbit nonvolatile memory chips and 4-Mbit RAMs by the end of this year; and 4-Mbit nonvolatile memory chips and 16-Mbit RAMs in the next few years," Ignatius says.

The system also comes with features that are not commonly found on its more expensive competitors but which are in demand for new-generation memory chips. For example, "We have a tri-level driver that allows the test programmer to specify three voltage levels on the fly: generally available low-level, high-level, and higher-level voltage up to 20 V," says Ignatius. *–Jonah McLeod*

IS A WAVE OF CONSOLIDATIONS COMING IN ATE?

All the moves in the automatic-test-equipment business aren't being made in the area of new systems. In a development that could be the first of a number of consolidations, Teradyne Inc. of Boston and Zehntel Inc. of Walnut Creek, Calif., have announced an agreement in principle for the two to merge through an exchange of stock.

If both boards and Zehntel's stockholders approve the plan, Zehntel, which provides in-circuit board testers ranging in price from $100,000 to $500,000, would become a division of Teradyne, with no change in management or in location.

Frederick Van Veen, Teradyne's vice president, says that the acquisition of Zehntel's low-end in-circuit board testers would complement Teradyne's emphasis on functional-board test systems that are positioned in the high end of the market, selling for $500,000 to $1 million.

Van Veen adds that he believes the Teradyne-Zehntel deal "could well be the first of several consolidations. You can't have 40 or so U. S. companies competing with Ando and Advantest in Japan. The U. S. is just going to have to concentrate its resources to compete more effectively."

Teradyne has been feeling the pressure. Its revenues have dropped from $389 million in 1984 to $306 million last year, and the company has reported losses in two consecutive quarters in 1987. But it has reported recent new orders for various test systems from a rebounding semiconductor industry, and that might indicate that a recovery from a devastating three-year ATE industry-wide recession may be under way.

Zehntel revenues in fiscal 1987 were $42.2 million, on which the company had net income of $1 million. A Zehntel spokesperson says the company wasn't seeking to be acquired, "but the Teradyne overture was one we couldn't walk away from. There's no other company with whom we match up as well." The merger is expected to become final by December.

Another victim of the ATE slump is GenRad Inc. of Concord, Mass., which recently closed its Semiconductor Test Division in Milpitas, Calif. [*Electronics*, Aug. 6, 1987, p. 126]. The division was losing money at a time when GenRad management is committed to return the company to profitability next year. Those officials declined to comment on possible effects of the Teradyne-Zehntel merger. *–Larry Curran*

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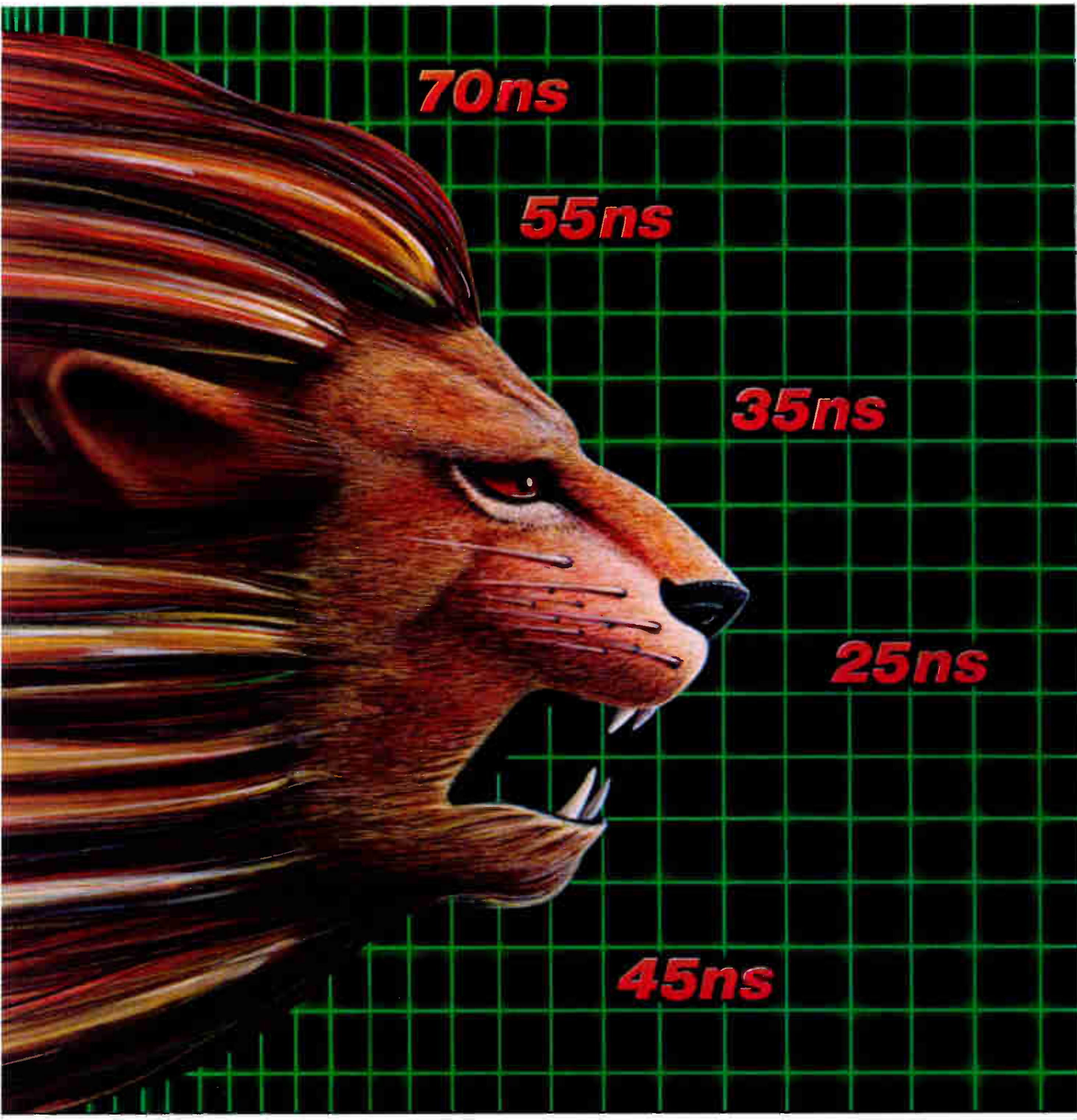

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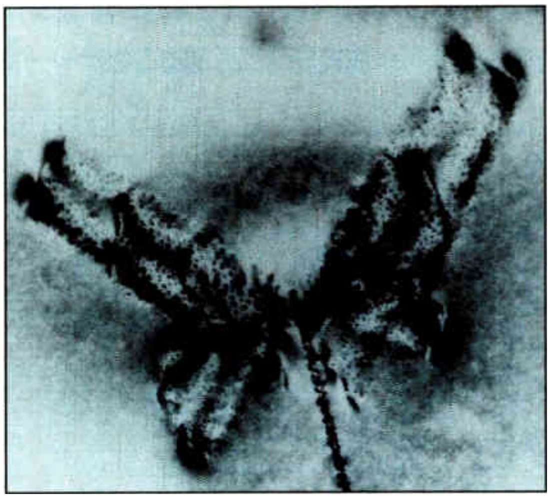
SEMICONDUCTOR PROCESSING

A WAY TO CLEAN WAFERS FAST—WITHOUT OXYGEN

CAMBRIDGE, MASS.

It takes hours to clean metallic contaminants from the critical top layers of a silicon wafer. Now researchers at the Massachusetts Institute of Technology, with help from Texas Instruments Inc., are exploring a promising new method of purifying the material in seconds. And the method may even be capable of "immunizing" wafers beforehand.



ATTRACTION. In MIT technique, butterfly-shaped deformity in the crystal lattice attracts silicon wafer's impurities.

The most common method for ridding otherwise pure crystalline silicon of defects is to supersaturate it with oxygen before the cleaning stage begins. Then, during a three-step annealing process, the metallic contaminants gather around oxide precipitates that form in the nonactive bulk area of the chip, and so can be removed.

But this oxygen-based "gettering" process takes up to 20 hours. To shorten the time needed, the MIT team collects the contaminants instead around butterfly-shaped deformities in the lattice structure of the silicon itself.

So far, the researchers have managed to purify oxygenless silicon wafers in hours, not seconds. They have also prefabricated the "butterfly" defect and are preparing to test whether it can prevent impurities from reaching a wafer's surface layer beforehand.

"There's a lot more testing to be done," says Graydon Larrabee, a research scientist at TI's Materials Science Laboratory in Dallas. "The industry knows how to produce wafers with a known amount of oxygen, so we're not about to abandon that technique. We're helping [the MIT group] run experiments and we're running tests on devices, but mainly we're just waiting for them to produce results." But it is clear that if this rapid, oxygen-free wafer-cleaning process proves repeatable, it could greatly improve wafer yields.

TI is supplying the single-crystal oxygen-free wafers. They are being grown with a new technique that uses a magnetic field instead of a manual mixing process, which would cause oxygen to dissolve in the wafers.

In the first stage of annealing, the MIT researchers surround the wafers with an ambient gas made up of oxygen and hydrochloric acid and then heat them to 1170°C. This causes free-roaming interstitial silicon atoms to be extracted from the top 50 to 100 μm of the wafer.

At the second stage the wafer is cooled to 700°C, and the remaining interstitial silicon atoms in the deeper regions of the wafer dislocate, enlarge, and form microloops that make up the butterfly defect. At the same time, metallic impurities begin to precipitate on the microloops.

During the third stage, when the wafer is heated again to 1000°C, the contaminants are locked into the butterfly defects. Since interstitial silicon atoms move through the lattice in seconds, most of the time is saved between the first and second stages, says Jacek Lagowski, a research scientist in MIT's Electronic Materials Laboratory.

The effect is the result of a fortuitous accident: an MIT graduate student who was studying the oxygen-based method in 1984 decided to use some oxygen-free silicon as a control. "The oxygenless wafer was purified; it was very puzzling," says Lagowski.

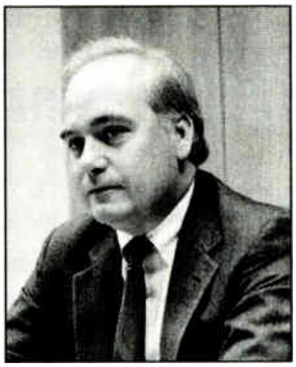
To find out why, the group brought in Osamu Ueda, an electron microscopist from Fujitsu Ltd. Last year Ueda discovered a 1-μm defect in the nonactive deeper layers of the purified oxygenless wafers that contained the precipitated impurities. *–Paul Angiolillo*

SOFTWARE

THIS SYSTEM KEEPS AN EYE ON T&E COSTS

FORT WORTH, TEXAS

American Airlines Inc. aims to become a highflier in the software business with a package designed to give companies a tighter grip on the soaring cost of corporate business travel and entertainment.



CLARK: "The potential for T&E software is immense."

Although not generally considered an information systems power, American Airlines earns more than $300 million a year from Sabre, the reservation system it made available to the travel world a decade ago. The company calls Sabre the world's largest nonmilitary, real-time computer system. Now program managers of the new software, called Capture, say it could equal Sabre's revenues. They hope to capitalize on increased concern by U. S. corporations about spending on business travel, and on new tax laws that are changing the rules for allowable tax writeoffs.

Capture works with Sabre, directly logging costs of booked air flights, hotel rooms, and rental cars. While trips and entertainment are being planned, costs are recorded on automated T&E worksheets for computer-cross-checks against corporate policies. After trips are completed, employees enter all incurred expenses; Capture can again evaluate adherence to policies, automatically allocate costs back to specific projects or business units, and prepare reports for government contracts. The system can also act as a historical data base of T&E expenditures for use in contract talks with travel-industry vendors.

BUY AND MERGE. The air carrier acquired the prototype for the product along with startup Capture Inc. of San Jose, Calif., last year. That company was merged with the airline's Sabre Travel Information Network division and moved to Texas, near airline headquarters.

The highly integrated data base and cost-information program is written in a fourth-generation language, Informix

4GL, from Informix Software Inc. of Menlo Park, Calif. Initially, it will run on departmental minicomputers, licensed for $50,000 or rented for $1,750 a month. Clark says Capture will first be available for IBM Corp. computers. Eventually, new versions will be developed for operating systems from Digital Equipment Corp. and AT&T Co.'s Unix.

Capture is the first automated system to place T&E management on company-owned computers. "I think Capture has taken one giant leap over the hurdles preventing most companies from managing the third largest controllable cost [next to payroll and data-processing expenses]," says corporate-travel consultant Jeanie Thompson-Smith, president of Topaz Enterprise Inc. of Portland, Ore.

Capture, which becomes available in October, also places American Airlines in competition with leading credit-card companies, which have been cultivating corporate accounts with T&E-tracking services and remotely accessible data bases of charges. For example, American Express Co. in New York last November introduced T&E-expense management services based on its Corporate Card System, which audits a corporate client's costs from its computer banks of charges. Citicorp of New York also offers corporate credit-card services with its Diner's Club card.

American Airlines will also compete with more than 50 personal-computer-based travel-related management packages. These are narrowly targeted at market niches and do not serve the entire corporate T&E reporting process, says Philip L. Clark, vice president of sales and marketing for the Capture business unit.

"We all realize that it is a significant market opportunity. U. S. businesses spent $112 billion on travel in 1986, and 10% to 14% growth projections will place it in the range of $400 billion in the 1990s," Clark says. "The potential [for T&E-management software] is immense and the potential is certainly there to be as big as Sabre. It is a new and exciting area for business software. There are no existing systems, no standards, and most corporations don't even know how to deal with this huge problem."

–J. Robert Lineback

AVIONICS

AIR FORCE'S NEW TWIST ON AN OLD IDEA

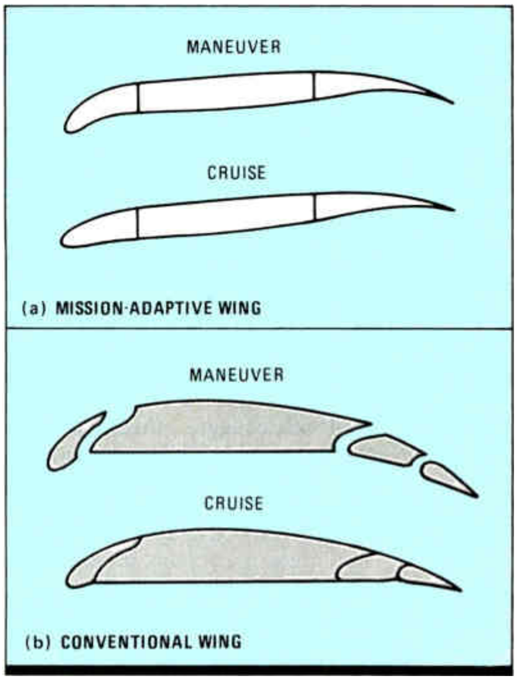
DAYTON, OHIO

The Air Force is working on a program that would, among other things, make accidents like the Detroit plane crash of Aug. 16, caused by undeployed flaps, a thing of the past. The aim of the program, called the Mission-Adaptive Wing project, is a wing that changes shape automatically.

The principle is not new. When the Wright brothers achieved mankind's first powered flight in 1903, their plane was guided not with today's system of slats, hinges, ailerons, and spoilers, but with a wing-warping system. Now, thanks to sophisticated computer control and modern composite wing materials, the Air Force may be about to return to that setup for future fighter aircraft—only this time, electronically guided.

The final phase of flight tests began at Edwards Air Force Base, Calif., last month. "We're using the same primary principle [as the Wright brothers]. We're actually deforming the wing rather than deflecting flaps and slats to change the pressure distribution on the wing," explains Ronald W. DeCamp, at Wright-Patterson Air Force Base, near Dayton.

By automatically minimizing drag and maintaining peak aerodynamic efficiency for varying flight conditions, the wing system is expected not only to allow for tighter sustained maneuvers and quicker response to pilot pitch commands, but to pay dividends in aircraft range and g-force pulling ability, says DeCamp. For example, if wind-tunnel calculations prove out, the computer-controlled wing will boost range by 25%.



BENDING TO IT. The computer-controlled twisting wing, top, would not need the slats and flaps of today's wing.

Likewise, an aircraft equipped with the wing should be able to withstand higher g forces than today's fighter jets, which are typically limited to a maximum of 7.33 g. But the outboard segment of the Mission Adaptive Wing will be deflected upward when that g limit is reached. This will shift pressure to the inner portion, raising the limit to about 9 g.

The experimental wing, designed by Boeing Military Airplane Co., Seattle, is made with a traditional aluminum wing box at its center, so that it can still be used for fuel storage. But the single leading surface from wing root to tip and three trailing-edge surfaces are covered with a flexible, fiberglass composite material that mechanisms can bend to change the wing shape. Under control by a pair of Boeing-built computers that take inputs such as speed, altitude, and acceleration from the plane's flight-control system, the Mission Adaptive Wing can change its shape up to 25 times per second. In all, about 40% of the total wing surface can be deformed.

TEST PROGRAM. The flight tests that began last month will be completed in about a year, and are the final step in the program. During an earlier year of flight tests ending last November, pilots used manual switches to check out separately each of the system's flight modes. The current flights will for the first time test the system operating entirely under computer control, DeCamp says. Total funding for the wing program has been about $50 million, with $35 million from the Air Force and the remainder from the National Aeronautics and Space Administration. While two separate computers are being used for the flight tests, the system's software is designed for incorporation into the integrated central computers in future aircraft.

At Wright-Patterson, DeCamp says that last year's initial flight tests of the wing system went extremely well, with performance meeting or exceeding wind-tunnel predictions. The wing is unlikely to be retrofitted on existing military planes, he says. But if the current round of flight tests goes as expected, "I don't see any reason why this system won't be used on our next aircraft." The technology is being considered for use on the Air Force Advanced Tactical Fighter, planned for production in the mid-1990s.

–Wesley R. Iversen

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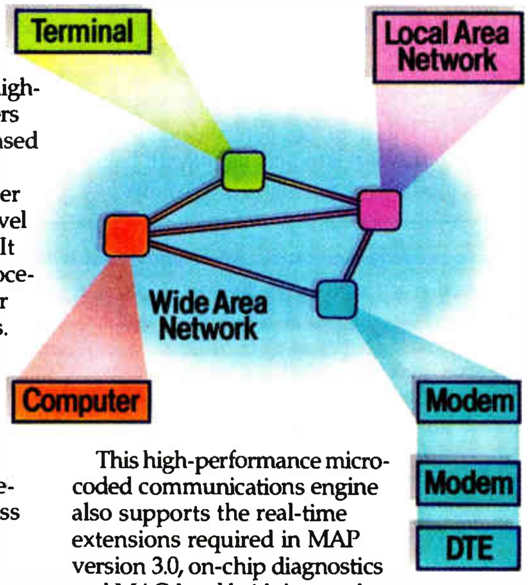


Motorola has developed a family of high-performance communications controllers called Serial Processing Units (SPUs) based on a modular design concept.

The MC68605 X.25 Protocol Controller (XPC) independently generates link-level commands for X.25 and X.75 networks. It expertly terminates the Link Access Procedure Balanced (LAPB) at the full 1.544 or 2.048 data rates provided by T1 facilities. It has passed rigorous Defense Data Network certification tests, and its global acceptance is suggested by use on packet networks all over Europe.

The MC68824 Token Bus Controller (TBC) is the only single-chip VLSI implementation of the IEEE 802.4 Media Access Control (MAC) sublayer defined in the Manufacturing Automation Protocol (MAP) specification.

This high-performance micro-coded communications engine also supports the real-time extensions required in MAP version 3.0, on-chip diagnostics and MAC-level bridging, and implements the recommended standard MAC-to-physical serial interface.

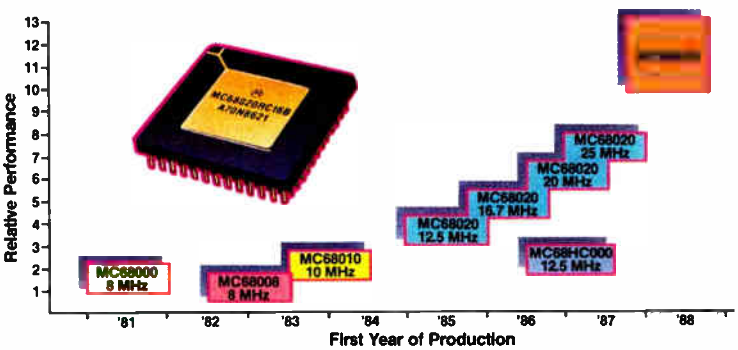
The MC68184 Broadband Interface Controller is, with RF circuitry, the broadband modem required for each node of a broadband MAP network.

In addition to the SPUs, M68000 communications peripherals include the MC68661 Universal Synchronous Communications Controller, the MC68652 Multi-Protocol Communications Controller, several DMA circuits and a variety of miscellaneous single- and multifunction devices. A

The highest-performance 8/16/32-bit MPUs smooth the migration path for your products.

Common internal 32-bit architecture. Object-code software compatibility. Just two of the reasons M68000 Family microprocessors from the 8-bit MC68008 to the 32-bit industry standard MC68020 give your products both the highest performance and the smoothest migration path.

Operating speeds range from 8 MHz for low-cost applications to the industry's fastest general purpose MPUs at 25 MHz.



And, products based on M68000 Family MPUs are the standard for UNIX® operating systems, CAD/CAM workstations, next-generation office automation, multi-user/multi-tasking departmental computers, color graphics as well as for real-time factory automation.

M68000 MPUs are also preferred engines for high-performance artificial intelligence with large linear addressing requirements.

Large, flexible 32-bit register set, large linear address space, powerful yet simple instruction set and flexible addressing modes all add up to the competitive advantage for your M68000 MPU-based product. B

Emulate in real time, debug in record time, with the most powerful M68000 Family development system.

Motorola's HDS-300™ hardware/software development station can give you an important edge in slashing development time and moving your product to market when you design in one of the industry's leading M68000 family MPUs.

It simplifies and speeds up debugging and testing of your MPU hardware and software, and in the appropriate configuration can also provide source-level debug for even greater development-time reduction.

Labor-saving features include real-time no wait-state emulation to 25 MHz, system performance analysis and "C" language source-level debugging. Cost efficiency is achieved with a modular approach that permits operation with any of the available emulator modules, including MC68020, MC68010, MC68000 and MC68008.

There are so many more reasons why the HDS-300 development station is the ultimate emulation and analysis tool for systems based on MC68000 Family processors. Discover them. C

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The design kit has just what you need to create three M68000-based systems.

Three MPUs include the MC68000 16-bit general-purpose standard, the high-performance 16-bit virtual memory MC68010 and the cost-effective 8-bit MC68008 with the 32-bit internal architecture of the MC68000.

Six flexible family peripherals are included so you can design for your specific applications.

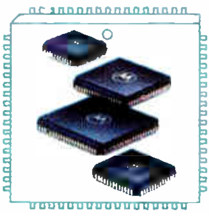
The MC68440 with dual independent DMA channels provides DMA control. System timing and parallel I/O requirements are handled by the MC68230. The MC68901 is a multifunction circuit with a single-channel UART for data communications, in addition to an 8-source interrupt controller, four 8-bit timers and eight parallel I/O lines.

Three different serial communications devices, MC68681, MC68661 and MC68652, complete the parts complement, and the kit also contains the documentation you'll want for converting these high-performance M68000 Family devices into superior systems of your own design.

The MC68000KIT is available only through authorized Motorola distributors. Contact your Motorola distributor to take advantage of this great $98 value. D

M68000 Family now offers surface-mount packaging.

As customers develop the ability to utilize surface-mount packages, Motorola is putting the M68000 Family in "J"-leaded, Plastic Leaded Chip Carriers. Several MPUs and over a half-dozen varied peripherals are already available now or later this year. The MC68000, MC68HC000 (HCMOS) and MC68010 are available now in the 68-lead package. The MC68008 is available now in the 52-lead version.



PLCC-packaged family peripherals include the MC68824 and MC68605 SPUs (84-lead), MC68440 and MC68442 DMA devices (68-lead), MC68681/2681 DUART (44-lead), MC68230 Programmable Interface/Timer (52-lead) and the MC68901 Multifunction circuit (52-lead). And this is only the beginning. E

Heralded Motorola M68000 Family training courses now available on audio cassettes.

Two Motorola-developed training courses for the MC68000 and MC68020 are now available on audio cassettes. Both of these low-cost courses also include course notes and appropriate technical literature.

Course MTTA1 is an overview of the MC68000 microprocessor: pins and bus operation, addressing modes, instruction set and exception processing including interrupts. Course completion offers you basic familiarity with the MC68000.

Course MTTA2 is an introduction to the MC68020: internal architecture, programming model, pins and bus operation, addressing modes, instruction set and exception processing.

MTTA1 is $60. MTTA2 is $95. The price for both courses together is $140.

A new course on the MC68030, MTTA3, is available in mid-September at $95. F

Literature Packs supply M68000 Family device and application information.

M68000 Family product literature has been assembled into three special, distinct assortments for differing interests. They include brochures, technical summaries and data sheets, benchmark reports, application notes, technical article reprints and other useful pieces.

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The M32BITPAK focuses on our top-o'-the-industry 32-bit products, featuring the MC68020, of course.

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PROBING THE NEWS

HOW DATA GENERAL WENT WRONG AND WHAT'S BEING DONE ABOUT IT

IT GOT TOO BIG, TOO FAST; NOW IT'S SLIMMING DOWN AND FIGHTING BACK

by Larry Curran

WESTBORO, MASS.

For Data General Corp., it was the best of times, it was the worst of times. Those times for the controversial, scrappy, yet now troubled minicomputer maker are not happening now, surprisingly; they occurred in 1984.

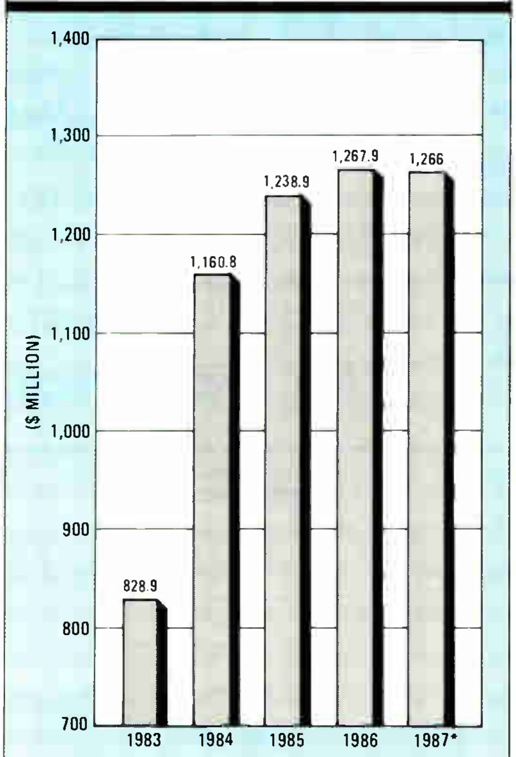
That year certainly qualified as the best of times: it was a record year. The Westboro, Mass., company finally broke through the $1 billion mark in revenues, growing at an astonishing 41% rate over 1983. Profits did even better, nearly quadrupling. But the year ultimately turned out to be the worst of times: management misread the signs, setting in a motion a series of events that now are pushing DG into taking draconian measures to restructure in an all-out attempt to get back on track and recover from the first losing year in its 19-year history. These measures won't work in time to stem this year's rising tide of red ink (charts).

DG had a banner year in 1984 primarily because the computer industry had a banner year. But the company was also making real hay in penetrating the office automation market. The managers running this end-user assault was a band of IBM Corp. emigrés, not the original band of entrepreneurs that had founded the company, and they believed the huge contracts the company had grabbed away that year from such competitors as Digital Equipment Corp. and IBM had propelled DG into the major leagues.

To better compete with these giants, with 5 to 46 times DG's revenues, management quickly poured $167 million into a massive expansion effort. In less than a year, 20% more employees were hired; capital spending doubled over two years; and hundreds of thousands of square feet of space were added. As a result, DG increased its production capacity by an awesome three times and was ready to turn out $3 billion worth of computer systems annually. But something happened on the way to market.

■ Data General managers overestimated their own marketing prowess. They were still outgunned by IBM and DEC when it came to costly pursuits of end-user business. The company drained its resources by investing too much time and money on bids for broad-based business at Fortune 500 companies: its failures included Mobil, United Airlines, and Ford. In some of those fights, DG products scored better technically than did competitors, but the awards still ended up going to IBM or DEC since they already had big installed bases at customer sites.

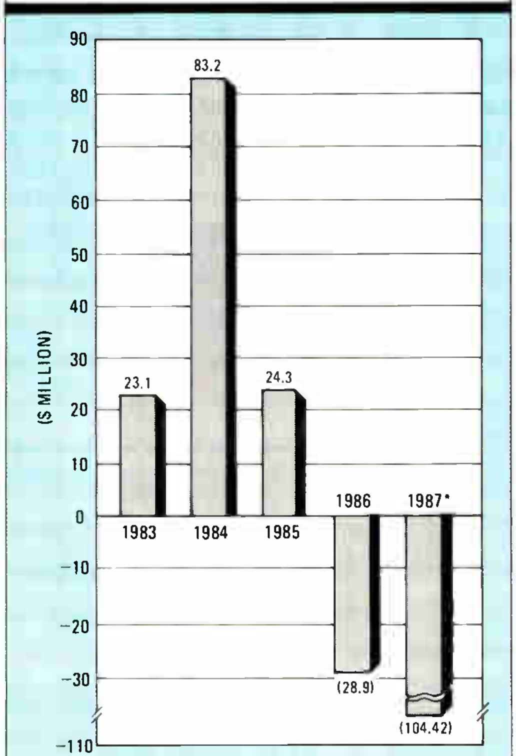
DATA GENERAL'S REVENUES HAVE BEEN FLAT . . .



*ESTIMATED BY DEAN WITTER REYNOLDS INC.

SOURCE: DATA GENERAL INC.

. . . AS LOSSES MOUNTED



*ESTIMATED BY DEAN WITTER REYNOLDS INC.

SOURCE: DATA GENERAL INC.

■ Managers were blindsided by the sharp drop in computer sales in 1985 and didn't react fast enough. One source who knows the company well says its response to the 1985 business downturn came too late. Then, he adds, "DG began to cut its sales force at a time when IBM and DEC were expanding their sales staffs." The company acknowledges it was late in recognizing the downturn. "We were into our third quarter [ending June 30, 1985] before it was clear," says Herbert J. Richman, executive vice president. "And while we did begin to make cuts in the sales force, we're certainly changing that now."

■ DG failed to penetrate the fast-growing and highly lucrative technical work station market; now the company is trying to figure out how to play catch-up to Apollo and Sun Microsystems.

One of the reasons for the poor financial performance was DG's late introduction of a 32-bit minicomputer line. Its machine was introduced in 1980, two years after DEC began delivering its first 32-bit system. Now sales of 32-bit systems have not come on as fast as expected, failing to offset the rapidly declining revenues from 16-bit systems.

Company watchers say DG's troubles started after it began filling key decision-making positions with senior managers from IBM. DG's cofounders, President Edson de Castro and Richman, long regarded as strong, hands-on managers, had become far less involved in running the company. De Castro allows he delegated too much responsibility for plotting the company's course five years ago. "I'm not satisfied with how that worked out," he says.

De Castro doesn't name names, but in recent interviews at the company the implication was that much of DG's current plight was attributable to the ex-IBM managers. The top gun in that group was Robert C. Miller, former senior vice president in charge of the Information Systems Group, who arrived from IBM in 1981 and departed last April to become president of MIPS Computer Systems Inc. in Sunnyvale, Calif. [*Electronics*, April 30, 1987, p. 12].

Many observers say that in the early 1980s, the company strayed away from its roots serving original-equipment makers and value-added resellers to an "overemphasis" on pursuing the end-user business, especially the office automation market. That shift in emphasis resulted primarily from DG's recruitment of other key senior executives from IBM. Besides Miller, they included J. David Lyons, still DG's vice president for business group marketing, and David Chapman, who left DG last year as senior vice president for manufacturing to become president and chief executive officer at Cullinet Software, Inc., Westwood, Mass. It was under Chapman that the huge facilities expansion was begun.

The drastic measures taken by management to downsize the company now leave it "closer to a $2 billion company in capacity," figures Ronald Skates, senior vice president for finance. In July, it consolidated manufacturing, marketing, field service and finance operations, closing offices in Paris, Denver, Milford, Mass., and Hooksett, N. H. Nearly 950 jobs are being eliminated, and $100 million in expenses will be cut. Analysts agree that these harsh measures have positioned DG to be profitable in the fiscal year ending September, 1988. To get sales and marketing back on track, de Castro has put both organizations back under Richman.

De Castro certainly is running the company as tightly as he ever has. For example, he is personally reviewing and setting priorities for every R&D program. As he puts it, "I'm back running the company." But he admits that he may not have done it soon enough. Now he is pledged to: deliver a profit in 1988; return to DG's roots with a major recommitment to the OEM/VAR business; make a strong thrust into computer-based networks; and to be extremely disciplined before competing for end-user business that pits DG against entrenched rivals.

The IBM influence at DG certainly hasn't been all bad. Miller is credited with directing DG's successful penetration of the office automation market. Its CEO integrated office software now has more than 5,600 licenses.

But a former insider at the company says DG has failed to capitalize on more of its end-user opportunities because the end-user part of the business has been underfunded. "There weren't enough dollars for sales people and for advertising because of losses elsewhere in the company," he adds. The losses included the costs of acquisitions, the cost of early retirement of a $150 million debenture, and litigation costs that approached $100 million. Richman denies that the end-user business was underfunded. "We probably invested too much in the end-user business; we should have balanced that by better sustaining the VAR business."

And that's exactly what de Castro and Richman are doing now. They point to the rebuilding efforts of Ward D. MacKenzie, vice president and head of the VAR Marketing and Development Division, as holding the potential for substantial market gains. MacKenzie [*Electronics*, June 11, 1987, p. 16] is trying to bring more balance in the end-user/VAR revenue split at DG. That split is about 50-50 now, but de Castro says the VAR portion "should increase to more than 50%; DEC has focused on gaining market share and has lost focus on the OEM business."

Another source close to DG isn't convinced that it can afford to back the VAR channel heavily now to the detriment of end-user business. "The VAR business didn't sustain the company before and it won't now," he says. "They need both sides of the business; they can't keep running from one side of the boat to the other, as they have been." One analyst cautions against too much reliance on business that others are not pursuing. "You can't make a living by picking up business that IBM and DEC don't want," says John W. Adams, analyst for Adams, Harkness & Hill Inc.

Adams believes DG took a step in the right direction with its spring announcement of its personal-computer integration product (DG/PC*I). It will use a local network to link IBM, IBM-compatible, and its own personal computers with DG's departmental computers and IBM mainframes.

Networked computing, in fact, has the highest priority among the compa-

DE CASTRO: "I'm not satisfied with how [delegating authority] worked out."

RICHMAN: "We were into our third quarter" before detecting the downturn of 1985.

CROOK: Networking is an opportunity for Data General to differentiate itself.

ny's strategic thrusts. One very large deal may be in the offing here. De Castro describes the effort, headed by senior vice president Colin Crook, as "incredibly important for the future." Crook sees it as an opportunity for DG to distinguish itself by its approach to standards. DG will support the International Standards Organization's seven-layer Open Systems Interconnect (OSI) model, IBM's Systems Network Architecture (SNA), the Integrated Services Digital Network (ISDN) approach to combining voice and data, and whatever other standards will help to integrate PCs, departmental computers, and mainframes. Crook stresses that IBM and DEC have vested interests in promoting SNA and DECNet. "In contrast, our strategy is to integrate aggressively with whatever the customer wants."

One hard lesson for Data General has been that it may have lost most of its opportunities in the technical work-station market. Susie Peterson, analyst for The First Boston Corp., is "not sure that it makes much sense for them to make a big effort in technical work stations. I'd rather see them go after the medical or petrochemical markets in a big way."

These are two of the six major end-user markets targeted by management: banking and financial services, insurance, petrochemicals, health care equipment, manufacturing, and the government. DG has historical strengths and solid account penetration in all of them and each of these segments is growing, de Castro says.

Over the long run, the combination of de Castro's leadership, a strong future product plan, and an improving market most likely could put DG back on course. As evidence of the start of a modest market recovery, De Castro cites order increases essentially across all product lines for the March and June quarters. DG must hit the market with "another round of high- and low-end systems in the fall or winter," declares First Boston's Peterson. De Castro's leadership is pivotal to the company's success, she maintains. "If you bet on Data General, you're betting on Ed as the team leader." □

THE SECOND BIPOLAR MEETING LOOKS LIKE A HOT ONE

BIG TOPICS: ANALOG CAD, NOISE-IMMUNE LOGIC, 3-ns SRAM, 8-ns PAL

by Bernard C. Cole

MINNEAPOLIS

This year is only the second time around for the Bipolar Circuits and Technology Meeting, but the fledgling conference is already becoming a top showplace for advanced bipolar technology. Semiconductor specialists who show up for this year's meeting, scheduled for Sept. 21-22 in Minneapolis, will find plenty to stretch their attention spans—from analog bipolar computer-aided-design technology to sub-5-ns 4-Kbit static random-access memories.

Like older semiconductor conferences, the Bipolar Circuits Meeting is taking on an international flavor. Of the 54 papers on the program, eight are from Japan and nine are from Europe, says meeting chairman John Shier, a senior consulting engineer at VTC Inc., in nearby Bloomington, Minn.

Digital circuits, of course, will get the heavy play at the show, but they won't eclipse analog work. One standout will be Sony Corp.'s CAD system for analog bipolar circuits, which slashes design time for large chips. Also sure to garner a lot of attention is a new bipolar logic family, with noise immunity equivalent to CMOS, from the University of Minnesota. Another major attraction is likely to be an ultra-high-speed heterojunction bipolar transistor structure, based on a silicon-germanium combination, from British Telecom Research Laboratories.

Other highlights of the meeting should be a 3-ns, 4-Kbit emitter-coupled-logic SRAM from West Germany's Siemens AG; a 6-ns, 128-by-18-bit ECL three-port register file, from Fairchild Semiconductor Corp.; and a sub-8-ns TTL programmable-array-logic part from Advanced Micro Devices Inc. On the process side, there will be a new self-aligned bipolar ECL process from Hitachi Ltd., featuring gate delays of 50 ps and less, and faster, denser biCMOS technologies.

Bipolar circuit designers at the meeting undoubtedly will take a close look at the Sony offering. CAD tools have been slowly spreading from digital to analog circuits for several years, but they've had the most telling impact on large CMOS chips. However, Sony designers in Atsugi are using CAD to build analog circuits with as many as 8,000 bipolar transistors aboard. Key to the development, say Sony researchers, is the use of a hierarchical design and verification technique, plus a circuit-connectivity comparison tool. For a VCR signal-processing circuit with 8,750 transistors, design time using the CAD system was 11 weeks to obtain a completely error-free chip in the first run. Connectivity verification took only one day, thanks to the tools, instead of the 15 days it would have without them.

NOISE MARGINS. Digital designers should be intrigued by the noise-immune bipolar logic family worked out by the University of Minnesota's electrical engineering department. It boasts noise margins roughly equivalent to those of CMOS—larger than 2 V with a 5-V logic swing—and very attractive simplicity. It has an output on the gate that employs a conventional npn junction transistor, but with a constant-current load. This results in an output logic swing that is very nearly from rail to rail.

But the transistor and load still form a poor logic inverter because the input voltage swing is limited to about 0.7 V. To overcome this limitation, forward-biased control junctions have been added. The necessary constant-voltage element is formed from a simple npn structure, while the constant-current portion is achieved by the use of a depletion-mode junction FET with its gate tied to its source.

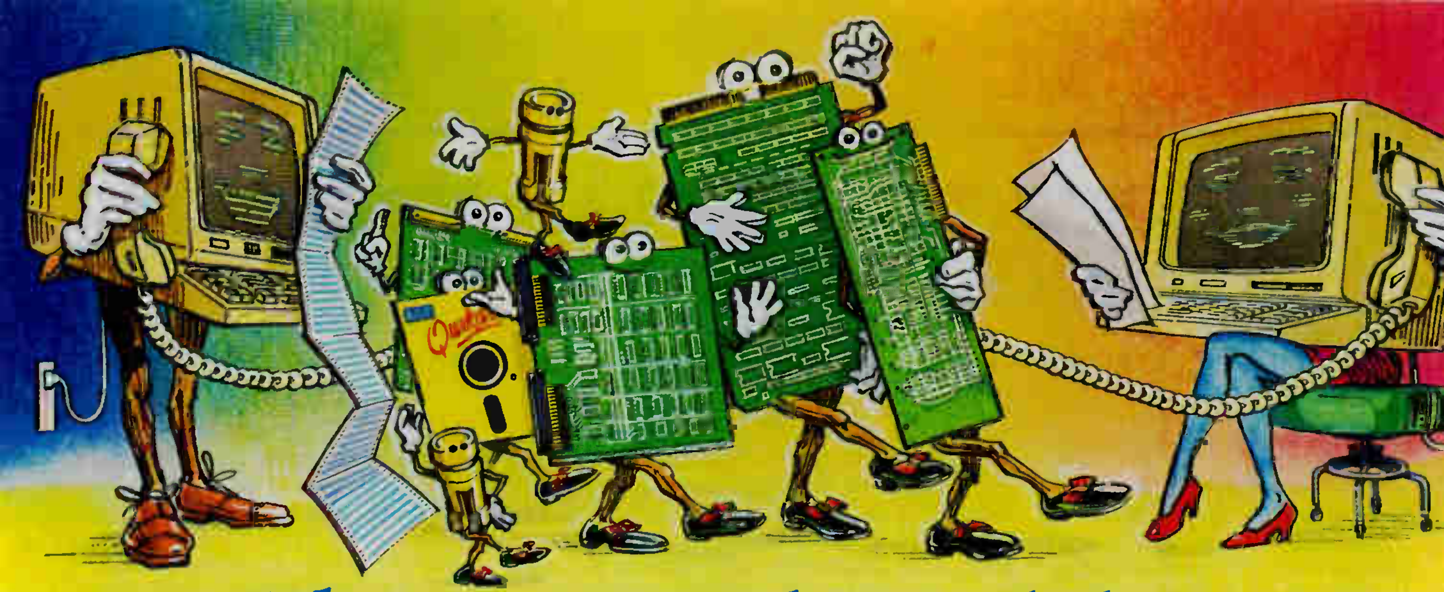
Speed is a passion in the bipolar community and researchers at British Telecom Research Laboratories, Martlesham, have indulged theirs through a combination of silicon and germanium. Heterojunctions of the two materials, they found, offer two to three times the speed of conventional silicon devices. The performance approximates that of gallium arsenide, but instead of hard-to-handle GaAs, the process involved is well-understood silicon fabrication. Also, the devices operate over temperature and electrical ranges similar to those of conventional silicon devices—British Telecom will report toggle frequencies of about 20 GHz with relatively wide base regions of 0.15 to 0.20 μm, better than those possible with silicon bipolar transistors of comparable size.

The ECL register file to be described by researchers from Fairchild's research center in Palo Alto, Calif., is made using the company's single-layer polysilicon technology [*Electronics*, Sept. 4, 1986, p. 55]. This 16-layer, 2-μm process features three metal layers and one silicide interconnect layer. The chip has 25,000 transistors and contains three independent I/O ports, two for reading and one for writing. Transistor cutoff frequencies of 5 GHz and gate delays of 200 ps result in cycle times of less than 6 ns at a power level of no more than 6.5 W.

Siemens of Munich has pushed bipolar ECL even closer to its limits with a 1-Kbit-by-4-bit SRAM having 3-ns access time and power dissipation of 1.5 W. Developed for cache memory and control-store applications, the part uses a scaled version of the company's OXIS process [*Electronics*, Sept. 23, 1985, p. 48] that slims feature sizes down to 1.0 μm. The array comprises 64 by 64 cells organized into a 1-Kbit-by-4 format. Capacitors between the collector nodes of cell transistors makes high cell stability and high alpha-parti-

MEETING HIGHLIGHTS

Field	Development	Developer
Computer-aided design	Tools for designing bipolar analog circuits	Sony
Devices	Noise-immune logic	University of Minnesota
	High-speed silicon-germanium transistors	British Telecom
	6-ns three-port register file	Fairchild Semiconductor
	3-ns 4-Kbit ECL RAM	Siemens
	8-ns PAL	Advanced Micro Devices
Processes	Self-aligned shallow-graft base technology	Hitachi
	12-V analog/digital biCMOS	VTC
	Scaled-down (1.5 μm and below) biCMOS	Motorola



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cle immunity possible without raising delay times due to a high collector-substrate capacitance.

The sub-8-ns speed of the TTL PAL fabricated by AMD in Sunnyvale, Calif., with an advanced bipolar process will run anywhere from half again to twice as fast as many commercially available ECL programmable logic devices. It features a clock-to-output delay of 6 ns and an input-to-output delay of 7.5 ns. The technology is a slot-isolated, double-metal bipolar process that incorporates a Schottky-diode array. A proprietary scheme removes two of the usual five gate-inversion delays in the sense-amplifier buffer area.

In addition to the array of devices, new twists in process technologies will be hot topics in Minneapolis. For example, the self-aligned process for ECL from Hitachi, Tokyo, pushes gate delays from 66 ps down below 50 ps. To achieve this record-low gate delay, Hitachi researchers took their standard sidewall base-contact structure and applied rapid thermal annealing to achieve shallow base and emitter structures and self-aligned diffusions for shallow graft bases. The result is a new structure, in which the graft base has been reduced from 0.5 to 0.2 μm, raising cutoff frequencies from 13 to 19 GHz.

Siemens will describe a 4-Kbit SRAM that accesses in only 3 ns

The conference emphasizes pure bipolar technology, but researchers are also keeping an eye on how mixed bipolar and CMOS can improve density and power without sacrificing speed. Two standouts in this area will be a 12-V analog/digital biCMOS process from VTC and second-generation biCMOS technology from Motorola Inc. VTC's 1.5-μm biCMOS process has been used to build ring oscillators with 400-ps switching speeds, and employs unconventional interconnect materials: platinum silicide, titanium-tungsten, and a copper-aluminum alloy. Bipolar devices bring with them advantages over CMOS alone in driving long interconnect lines: a buffer fabricated using the process achieves speeds 1.5 times higher than a pure CMOS buffer for interconnect metalizations longer than 2 mm.

Motorola's ASIC division in Phoenix, Ariz., will report that it can scale its 2-μm biCMOS process, currently used in a gate-array product line [*Electronics*, July 10, 1986, p. 67 and Aug. 20, 1987, p. 87], to 1.5 μm to achieve a 40% improvement in gate delay—about 450 ps. Scaling to 0.8 μm should bring that figure down near 150 ps. □

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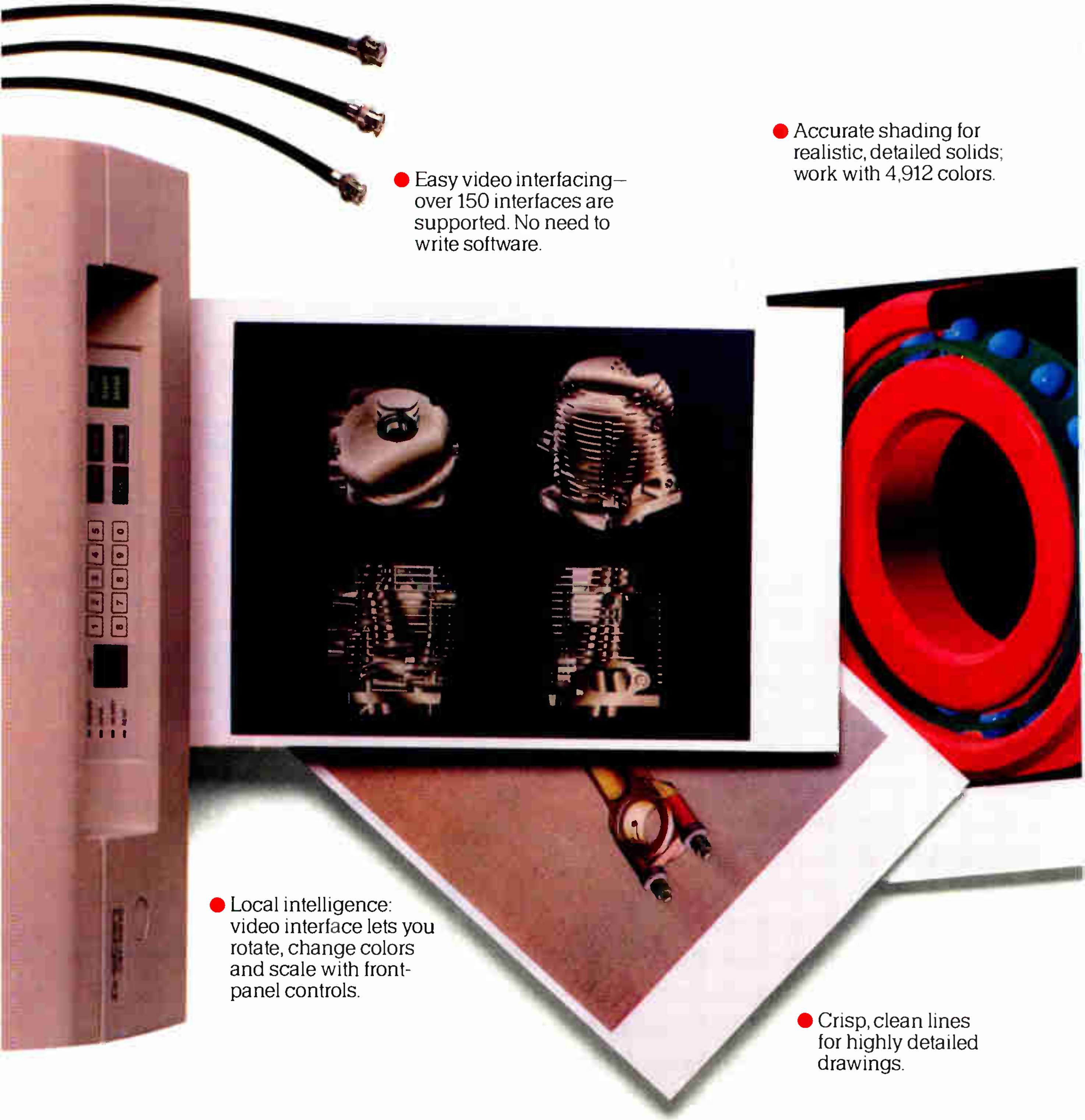

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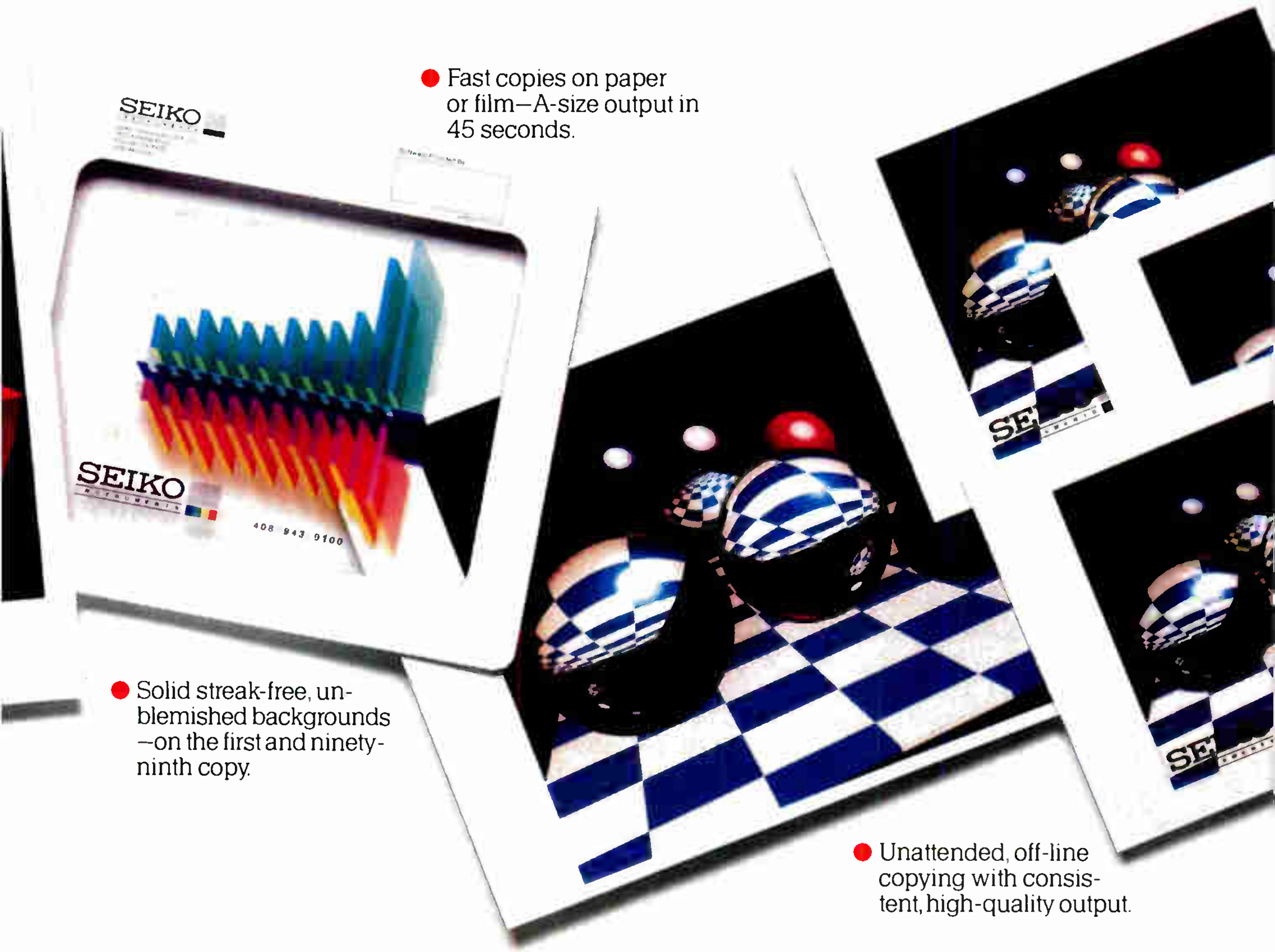

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INTERNATIONAL NEWSLETTER

ROOM-TEMPERATURE HEMTs ARE FINDING HOMES IN RADIO TELESCOPES

High-electron-mobility transistors that operate at room temperature are starting to find practical use in radio astronomy. Fujitsu Ltd., Tokyo, will supply HEMTs for radio-telescope antenna preamplifiers to the U. S. National Radio Astronomical Observatory this fall. The company is also expecting to sell some HEMTs soon to the Australian National Radio Astronomical Observatory. Fujitsu supplied 20 antenna preamplifiers with the same HEMT chips to the Tokyo Astronomical Observatory's Nobeyama Radio Observatory in March 1986. Some industry sources report that with the help of the HEMTs, astronomers at Nobeyama discovered new spectral lines—radio signals signifying the presence of a particular molecule—in a "dark nebula." The HEMT has a noise figure of 1.9 dB maximum at 20 GHz and gain of 6.5 dB when operated with drain bias of 10 mA and 2 V. The device is likely to see use in military applications, the company believes. □

SIEMENS AND PHILIPS JUMP INTO DIGITAL-TV-CHIP BATTLE WITH ITT

The market for digital TV chips is about to heat up. West Germany's Siemens AG and Philips in the Netherlands have together come up with a chip set that implements digital functions in a color receiver, but they have a lot of catching up to do: Intermetall GmbH of the ITT Semiconductors Group is supplying such chips to 16 set makers around the world [*Electronics*, April 5, 1984, p. 89]. Both the Siemens/Philips and the ITT circuits eliminate flicker and are suitable for the PAL, Secam, and NTSC color-TV transmission standards. The difference is Philips and Siemens use a line-lock system for synchronization instead of the burst-lock system. With line lock, the pictures reproduced from video recorders, for example, are more stable. To achieve a virtually flicker-free image, the Dutch/German set operates with twice the normal line frequency—31.25 kHz instead of 15.625 kHz—and twice the frame frequency—100 instead of 50 Hz (or 120 instead of 60 Hz with chips for the U. S.). Siemens says samples of the set are available now. □

E-BEAM COULD SLASH TURNAROUND TIME FOR ULTRAFINE-LINE PC BOARDS

An electron-beam lithography system that writes directly on printed-circuit boards may soon be at work in production lines, providing faster turnaround than conventional systems and speeding critical products to market. It can go directly from design data in a computer-aided-engineering system straight to board fabrication, without first making the master and working-film masks needed for optical lithography. A prototype of the system, developed by Mitsubishi Electric Corp. in Amagasaki, Japan, features extremely fine minimum pattern-feature sizes—60 μm for both lines and the spaces between them. It can accommodate board sizes up to 500 by 600 mm, with an alignment accuracy of ±6 μm. And because the resist and laminate materials used are identical to those used for ultraviolet lithography, the board-processing equipment need not be changed for the steps following lithography. □

SATELLITE TO TEST HDTV BANDWIDTH-COMPRESSION TECHNOLOGY

The Japan Broadcasting Corporation (NHK) and Kokusai Denshin Denwa Co., both of Tokyo, have just started a one-month high-definition television transmission experiment using an Intelsat telecommunication satellite. NHK expects the test will hone its bandwidth-compression technology and thereby help pave the way for international HDTV transmission. NHK's HDTV features 1,125 horizontal scan lines, more than twice the number of the NTSC standard currently used in Japan and the U. S. The test is being run at KDD's Ibaraki Satellite Communications Center, Takahagi. □

Good news for military customers who need highest performance CMOS:

CMOS high speed SRAM.
CMOS high speed PROM.
CMOS high speed PLD.
CMOS high speed Logic.

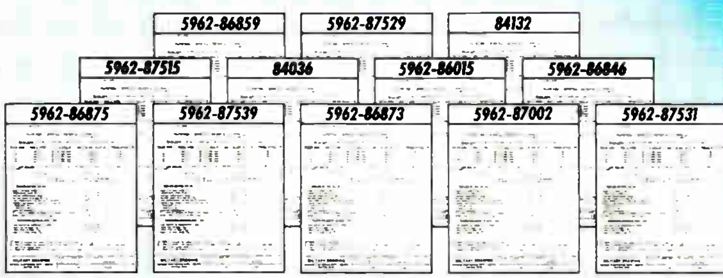
We offer a broad family of integrated circuits that let you build *faster* systems. Systems that run cooler, that take up less space, that use less power.

And now it's easier than ever for you to design us in. We're DESC-certified. And our first JAN parts are shipping. We offer flexible packaging automation so that you can get the packaging you need, including LCCs, pin grid arrays and flatpacks.

4Kx1 SRAM 35 ns.
Our first JAN qualified part, and the fastest JAN 4K Static RAM available.

And our 1.2 and 0.8 micron processes deliver record performance.

In fact, we're already part of many military programs with names like AWACS, B-52, F-111, F-14, F-16, F-18, HAWK, Space Shuttle and Sparrow.



Twelve drawing numbers moving through the DESC approval channel.

The biggest news: Our SMD (Standard Military Drawing) program.

We actively support the DESC-sponsored SMD program. As a result, we have the capability to draft Standard Military Drawings quickly and efficiently.

The payoff so far: We have twelve products certified or pending certification, with many, many more scheduled in the near future. And we intend to see that they become JAN slash sheets as quickly as possible.

Is it important to you to have a certain part available under the SMD program? You will find no vendor more cooperative or better equipped to help.

For the whole story, call for our Data Book.

DATABOOK HOTLINE:
1-800-952-6300, Ask for Dept.
1-800-423-4440 (In CA) Ask for Dept.
(32) 2-672-2220 (In Europe)
(416) 475-3922 (In Canada)

CYPRESS
SEMICONDUCTOR

Cypress Semiconductor,
3901 North First Street,
San Jose, CA 95134,
Phone (408) 943-2666,
Telex 821032 CYPRESS SNJ UD.
TWX 910-997-0753.

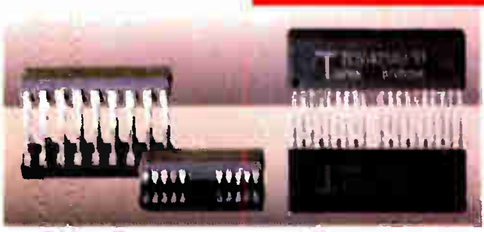
EVERYTHING THAT WON'T HAPPEN TO YOU WITH TOSHIBA MEGABIT DRAMS.

Firstly, you won't be building into your product a part that is not fully proven. You won't be anyone's guinea-pig.

Secondly, you won't be left alone to deal with any problems which may occur during new projects.

Thirdly, you will never come up against empty promises and hot air but will enjoy good service and advice.

Fourthly, you won't be let down by a supplier who fails to meet your delivery date, even when the quantities are large and the schedules tight.



Fifthly, you won't be missing out on the most up to date technology as the new 4 M DRAM from Toshiba has passed through the development stage.

In fact, you are leaving nothing to chance if you use Toshiba's Megabit DRAMs and rely on our know-how. But one thing is certain, you will pull ahead of your competitors. For Toshiba was not only the first to develop the 1 M DRAM, but also introduced and then mass-produced it. That was in 1985 and since then, Toshiba Megabit Chips have proved themselves repeatedly in practical application.

Bear this in mind. Get ahead of the rest.

In Touch with Tomorrow

TOSHIBA

TOSHIBA EUROPE (I.E.) GMBH, Neuss, Tel.: 00 49 21 01/1 57-0; München, Tel.: 00 49 89/92 80 91-0; Stuttgart, Tel.: 00 49 71 52/2 10 61-66 · TOSHIBA UK LTD, Tel.: 00 44 2 76/6 22 22 · TOSHIBA EUROPE I.E. GMBH, Paris, Tel.: 00 33 1 48 55/56 56 · TOSHIBA ELECTRONICS ITALIANA S.R.L., Milano, Tel.: 00 39 39/63 88 91 · TOSHIBA ELECTRONICS SCANDINAVIA AB, Stockholm, Tel.: 00 46 8/14 56 00

Incredible Speed! 250 dot lines/s

Ultra-high-speed High-resolution Thermal Printer FTP-441MCL001/FTP-421MCL001

Fujitsu has developed the ultra-high-speed thermal printers, the FTP-441MCL001 and the FTP-421MCL001, which can print up to 250 dot lines per second. Fujitsu's unique pressure support structure helps the head to print clearly, and the thermal head makes the printer quiet and unobtrusive.
The FTP-441MCL001 and FTP-421MCL001 print clearly, quietly, and quickly. As well as printing hard copies, they are useful for data communication, instrumentation, analysis, and medicine.

FTP-441MCL001

FTP-421MCL001

FEATURES

- High printing speed (250 dot lines/s)
- Long service life (30km: 30million pulses)
- Clear printing
- Two paper paths (One for thick paper)
- Low noise

SPECIFICATIONS

	FTP-441MCL001	FTP421MCL001
Printing method	Thermal line dot	
Dot matrix	640 dots/line	320 dots/line
Effective print width	105.6 mm	52.8 mm
Horizontal dot pitch	0.165 mm (6 dots/mm)	
Printing speed	250 dot lines/s (at 25°C and 60% RH)	
Paper width	114 mm	60 mm
Exterior dimensions (W) × (H) × (D) mm	160 × 40 × 60	107 × 40 × 60
Weight	Approx. 600 g	Approx. 300 g

FUJITSU MIKROELEKTRONIK GmbH:
Arabella Center 9 OG/A, Lyoner Straße 44-48, D-6000 Frankfurt am Main 71, F.R. Germany Phone: 069-66320 Telex: 0411963 Fax: 069-6632122
FUJITSU COMPONENT OF AMERICA, INC.:
3320 Scott Blvd. Santa Clara, California 95054-3197, U.S.A. Phone: 408-562-1000 Telex: 910-338-0190 Fax: 408-727-0355
FUJITSU LIMITED (Electronic Components International Marketing Div.):
Furukawa Sogo Bldg., 6-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100, Japan Phone: National (03) 216-3211 International (Int'l Prefix) 81-3-216-3211
Telex: 2224361 Fax: (03) 216-9771

FUJITSU

Circle 154 on reader service card

INTERNATIONAL WEEK

BRITISH AEROSPACE WINS SATCOM STUDY

British Aerospace plc has won a £250,000 contract from the European Space Agency to study the economic feasibility of a communications satellite system for land-mobile-radio users. The space agency wants the service operational by the mid-1990s and plans to place satellites in elliptical orbits—as are the Soviet Union's Molniya satellites—rather than the usual geostationary orbit. This will make it possible to use small, simple roof-mounted antennas.

ICL's PARALLEL UNIT TO BE DONE BY 1988

International Computers Ltd. feels confident it can meet the goal of 1 million graph reductions/s—between 10 and 100 times faster than a superminicomputer can do them—set for the Alvey 5th Generation graph-reduction parallel computer. The London computer firm, working with High Level Hardware of Oxford and the University College of London, has fully simulated the design and has working prototypes of system components. The group expects to complete a parallel processing machine by the end of the year.

SUPERCOMPUTERS ON TAP IN JAPAN

Anyone in Japan who needs time on a supercomputer will have a choice of four—two from Cray Research, one from NEC, and one from Fujitsu—on Recruit Co.'s time-sharing service starting in June. The Tokyo employment agency, which has offered time-sharing on a Fujitsu VP-400 since last October, added a Cray X-MP-216 in April. Soon, a Cray X-MP-18 and a NEC SX-2 will round out the network. Recruit's customers—there are 60 at the moment—will be able to access any or all of the computers on the net via an IBM Corp. mainframe regardless of the type of terminal they use. Protocol-conversion software will make this possible.

ASEA TO MERGE WITH BROWN BOVERI

A new European heavyweight will join the top ranks of high-technology companies at the beginning of 1988 as Switzerland's BBC Brown Boveri Ltd. and Sweden's ASEA AB combine their operations. The new company, ASEA Brown Boveri, will have 160,000 employees and revenues of some $15 billion. Both companies are most active in electric-power generation and distribution gear, but also produce electronics, automation, and industrial equipment. Goal of the merger: a wider market reach around the world through economies of scale.

CANON UNIT PRINTS 360 DOTS PER INCH

Canon Inc. is counting on a new high-resolution printer to speed sales of its Japanese-language word processor. Along with the usual 14-in. CRT display and two 3.5-in. floppy-disk drives, the Canon 400 has a thermal transfer dot-matrix printer with resolution of 360 dots per inch, the highest among existing thermal transfer printers. The new printer is able to reproduce 7,455 different characters—including the Roman alphabet, Japanese kana, and kanji characters—at a speed of 21 characters/s. The Tokyo firm expects to sell 4,000 of the systems a month at 358,000 yen each.

SIEMENS, ROCKWELL IN AUTO PARTS PACT

Siemens AG of Munich and Paris-based Rockwell International Body Components-Europe have agreed to jointly develop electronic control systems for automobiles. The systems will include those that control sliding roofs, window lifters, seat positioners, and car-locking mechanisms. The German company will manufacture the control systems and deliver them to Rockwell, which will distribute them, mainly in Europe. European sales of what the experts call "car chassis" electronic systems reached $156 million last year—roughly $92 million in West Germany alone—and are expected to double by 1990.

SEIKO CARD HOLDS 512 KBYTES OF RAM

Hard on the heels of Mitsubishi Electric Corp., Seiko Epson Corp. is offering samples of a 512-Kbyte random-access-memory card that can substitute for a floppy disk. The 2.4-mm-thick card measures 54 by 86 mm; it carries 16 256-Kbit static-RAM chips in naked tape-automated-bonding format. Seiko Epson has priced its card at 90,000 yen, undercutting Mitsubishi's 3.4-mm-thick card introduced in early August for 95,000 yen.

AUSSIE FIRM TO ADD 3RD CHINESE PLANT

Australia's largest printed-circuit-board manufacturer, Printronics Pty. Ltd., has beat out U.S. and European competitors to win a contract to build a $10 million pc-board plant in the People's Republic of China. The plant, to be located at Huang Pu New Port, will be owned by a joint-venture company in which Printonics owns 35% and Chinese companies 65%. It is scheduled to start up in October 1988 and will turn out boards with up to 14 layers. This will be Printronics's third pc-board joint venture in China.

SIEMENS, BASF JOINT VENTURE TAKES OFF

Comparex GmbH, the joint computer venture formed last January by West Germany's Siemens AG and BASF AG [Electronics, Nov. 27, 1987, p. 48], is off to a good start. During its first six months of business, sales reached 440 million Deutschmarks ($240 million); the firm had set a 1 billion DM ($546 million) target for all of 1987. Profits during the six-month period were 15 million DM ($8.2 million).

VCR TAPE MAKERS JOIN IN EUROPE

Three major magnetic tape makers have joined together in Europe to counter competition from the Far East that has caused prices of blank video-tape cassettes to plummet 60% over the past five years. In the deal, Agfa-Gevaert AG, a subsidiary of West Germany's Bayer AG, will become a 60% owner of PD Magnetics BV, a Dutch tape company owned by Philips of the Netherlands and Du Pont Co., Wilmington, Del., starting next year. Philips and Du Pont will hold 40% of the new venture.

GERMAN FIRM AIDS CHINA IN COMSAT

Messerschmitt Bölkow Blohm GmbH, the German aerospace firm, will cooperate with China Great Wall Corp. in China's DFH-3 communication satellite project. Under the terms of a recent agreement, MBB will help the Chinese Academy of Space Technology with system definition and will be responsible for various subsystems, such as antennas and the mechanical part of the solar power generator.

INMARSAT BUYS U.S. DELTA-2 LAUNCH

Inmarsat plans to launch one of its three second-generation communications satellites from a U.S. facility using a McDonnell-Douglas Delta-2 rocket. The London-based agency has three Inmarsat-2 birds on order from an international consortium headed by British Aerospace plc and had intended to launch them on the U.S. shuttle and the European Ariane rocket. Because neither now offers near-term launch dates, Inmarsat opted for the Delta-2 launch, set for December 1989.

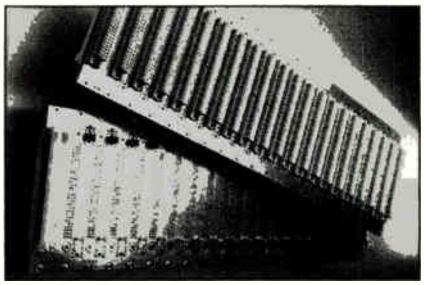
PM5785 sells for about 9,500 Dutch guilders.

Philips Industrial & Electroacoustic Systems Division., P. O. Box 218, NL-5600 MD Eindhoven, The Netherlands.
Phone 31-40-788620 [Circle 706]

21-SLOT BACKPLANE HANDLES FUTUREBUS

A backplane fully compatible with the IEEE Standard P896.1 defining Futurebus combines the reliability of multilayer construction with the constant characteristic impedance of buried microstrip signal tracks.

Available in 10- and 21-slot versions, the BICC backplane from Vero Electronics Ltd. is one of the first such products



available for Futurebus, a link that is microprocessor- and architecture-independent. The backplanes use high-reliability IEC 603-2 connectors and 6.3-mm tab connectors for power pick-up.

The products are available now. Price depends on importing country.

Vero Electronics Ltd., Flanders Road, Hedge End, Southampton SO3 3LG, UK.
Phone 44-703-366300 [Circle 707].

OP AMPs BOOST BANDWIDTH TO 2.5 MHz

Two precision operational amplifiers—one dual and one quad model—from Thomson Semiconducteurs feature a small-signal bandwidth of 2.5 MHz, or 2.5 times the performance of the company's standard μA741 series of op amps.

The bipolar TEB1033 dual-output and TEB4033 quad-output op amps target active low-pass-filter applications and feature an open-loop gain of 100 dB, offset voltage of 1 mV, 0.5-mA power consumption, a 60° phase margin, and a noise voltage of 8 nV/Hz at 1 KHz.

Pin-compatible with conventional op amps, the devices come in 8- and 14-pin dual in-line and small-outline packages, as well as in 20-pin leadless ceramic chip carriers.

The op amps are available now. Export price is 67¢ each in 100-unit purchases for the TE1033 and 88¢ each for the TE4033.

Thomson Semiconducteurs, 45 ave. de l'Europe, 78140 Velizy-Villacoublay, France.
Phone 33-1-39-46-97-19 [Circle 708]

LAN ANALYZER OFFERS SIX DATA CHANNELS

The Model 002 local-area-network analyzer from Nippon Board Computer Co. Ltd. uses two high-performance microprocessors and six data channels to enhance LAN efficiency by monitoring, tracing, capturing, and analyzing signals on token ring networks.

Based on Intel Corp.'s 80286 and Motorola Inc.'s 68000 microprocessors, the

analyzer runs at 4 Mbits/s. Its six-channel filter controls the selection of data packets. Each channel has a 127-byte capacity.

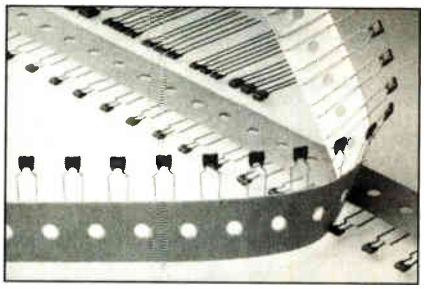
The analyzer also supports high-level protocol analysis for the International Standards Organization's Open System Interconnection protocols. It can be expanded to handle Manufacturing Automation Protocol LANs and Ethernet LANs.

The system includes a plasma display, a 20-Mbyte hard disk, 1.2-Mbyte floppy disk, a Centronics parallel interface and RS-232-C serial interface. Delivery takes two months. Price depends on importing country.

Nippon Board Computer Co. Ltd., 1-16-1 Sotokanda, Chiyoda-ku, Tokyo 101, Japan.
Phone 81-3-253-5670 [Circle 709]

63-V CAPACITORS RATED FLAMEPROOF

The Cap-Style series of ceramic multilayer capacitors from Stettner & Co. are resin-coated rectangular types featuring a rated voltage of 63 V and non-inflammable coating material according to specifications UL94-VO. The taped ver-



sions are available with leads spaced at either 2.5 mm or 5 mm.

The capacitors can be used in telecommunications, automotive, and other industrial applications. Delivery time is from 12 to 24 weeks depending on type. Prices for various models range from 6.60 DM to 150 DM for 100 units when ordered in 10,000-unit lots.

Stettner & Co., P.O. Box 7, D-8560 Lauf, West Germany.
Phone 49-9123-181371 [Circle 710]

OPERATING SOFTWARE RUNS 3 SYSTEMS

The FlexOS 386 operating system from Digital Research Ltd. allows users to run programs based on Intel Corp.'s 8088 microprocessor concurrently with programs based on Intel's 80286 and 80386 chips.

The DOS system supports Microsoft Corp.'s MS-DOS 3.2 as well as PC-DOS programs such as Lotus Development Corp.'s Lotus 1-2-3. Typical applications for FlexOS 386 include factory plant controllers, point-to-point sales operations and banking transactions.

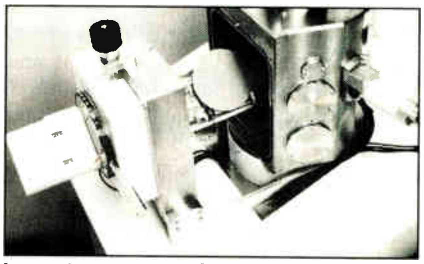
A FlexOS 386 system-builder's kit including MS-DOS, a C complier, and a GEM virtual-memory interface for graphics applications is available now and costs £995.

Digital Research Ltd., Oxford House, Oxford St., Newbury, Berkshire RG13 1JB, UK.
Phone 44-635-35304 [Circle 711]

INSPECTION STATION HANDLES 6-IN WAFERS

A scanning electron microscope from Jeol Ltd. uses a scanning compartment large enough to handle an entire 6-in. semiconductor wafer to shorten wafer-inspection time.

Since the position of the inspection



beam is controlled by a joystick, the operator can move it directly to any area of interest.

Advanced image-processing algorithms and the ability to store and manipulate multiple frames provide a clear image of the target. The JSM-820 is available now. Price depends on importing country.

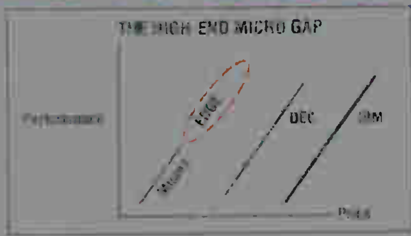
Jeol Ltd., Jeol House, Grove Park, Colindale, London NW9 0JN, UK.
Phone 44-1-205-6376 [Circle 714]

68000™ FAMILY UPDATE NO. 2

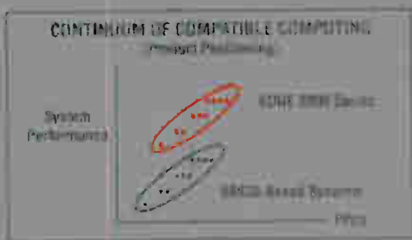
SEPTEMBER, 1987

OEMs CAN NOW OFFER HIGH-END, LOW-COST 68000 FAMILY COMPATIBLE PRODUCTS WITH 16 MIPS UNIPROCESSOR PERFORMANCE

By any measure, the 2000 Series VME™ board set recently unveiled by Edge Computer represents a quantum leap in 68000-compatible computing. Designed to fill the microprocessor high-end performance gap, the EDGE 2000 has driven performance costs down to about $1K per MIPS (OEM quantities). The 2000 Series is available in a VME 3 high eurocard, 4 board set for easy product integration.



The EDGE 2000 is actually a CISC machine that operates with RISC-like efficiency. The specs are impressive. The uniprocessor version of the EDGE 2000 delivers 16 MIPS sustained performance and 60 MB/sec I/O bandwidth. At 1.4 cycles per instruction, the EDGE 2000's AIT (average instruction time) is lower than any other computer on the market today. Quad configurations of the powerful 2000, which supports scalable, transparent multiprocessing with one to four CPUs, are rated in excess of 56 MIPS sustained performance. The modular 2000 Series is based on a proprietary high-speed EDGEbus structure that offers 64 bit, 128 MB/sec parity protected transfers. Global memory can range from 8 MBytes to 1 GByte. Up to four standard or proprietary secondary I/O busses can be supported through dual I/O controllers. In spite of its incredible price/performance characteristics, the EDGE 2000 features a very small footprint (17"W x 29"H) to fit in a normal office environment.



EDGE SOLVES COSTLY SOFTWARE PORTING AND ARCHITECTURAL COMPATIBILITY PROBLEMS

Those OEMs and System Integrators with 68000-based products looking to develop high-end products outside of the 68000 family must overcome a number of costly, lengthy software compatibility obstacles. Porting the operating system, utilities and application software for target hardware, designing I/O interfaces and compilers are among the most formidable. The ongoing costs for support and maintenance of two architectures are equally important considerations. 68000-compatible products developed by Edge Computer let OEMs and System Integrators move ahead with a high-end compatible 68000 architecture to eliminate substantial software porting expenditures while still maintaining architectural compatibility.

EDGE COMPUTER FORMS SWISS SUBSIDIARY

Edge Computer Corporation has formed a European subsidiary in Lausanne, Switzerland. The new company was established to capitalize on the rapidly growing European demand by OEMs, System Integrators and Value-Added Resellers for compatible high-end Motorola 68000-based products. The subsidiary will be headed by Heiner Krapp, vice president of international operations.

EDGE COMPUTER

Compatible With Your Future

For more information, contact Pamela Mayer, Edge Computer Corporation, 7273 E. Butherus Drive, Scottsdale, AZ 85260, 602/951-2020. European Sales Office contact Heiner Krapp, 5, Avenue des Jordils CH 1000 Lausanne 6 Switzerland, 41-21-275315.

68000 and VME are trademarks of Motorola Corporation

Circle 51 on reader service card

VLSI Part No.	Organization	Functions	Access Times
VT7C122	256 x 4	Separate I/O	15 ns
VT20C18	2K x 8	APD; 10 ns OE	20 ns
VT20C19	2K x 8	12 ns CE; 10 ns OE	20 ns
VT20C50	1K x 4	Separate I/O; FC	15 ns
VT20C68	4K x 4	APD	20 ns
VT20C69	4K x 4	12 ns CS	20 ns
VT20C71	4K x 4	Separate I/O; OT	20 ns
VT20C72	4K x 4	Separate I/O; HZ	20 ns
VT20C78	4K x 4	APD; 10 ns OE	20 ns
VT20C79	4K x 4	12 ns CS; 10 ns OE	20 ns
VT20C98*	8K x 8	APD	25 ns
VT20C99*	8K x 8	Fast CE	25 ns
VT62KS4*	16K x 4	15 ns CS	25 ns
VT63KS4*	16K x 4	15 ns CS; OE	25 ns
VT64KS4*	16K x 4	APD	25 ns
VT65KS4*	16K x 4	APD; OE	25 ns

APD = Auto Power Down; CE = Chip Enable; OE = Output Enable; CS = Chip Select; FC = Flash Clear; OT = Outputs Track Inputs During Write; HZ = High-Impedance Outputs During Write *Samples Available 4th Quarter, 1987

So long, Cypress. Sayonara, Toshiba. That goes for you, too, IDT. And Motorola. And all you other CMOS SRAM makers.

Now VLSI has some of the fastest CMOS SRAMs around.

We're not talking about just one part here. And one part there.

But a whole family of SRAMs that blow the doors off anything from the competition.

Our SRAMs make it easy to

For a free poster of this ad call 800-8-SAMPLE.

boost performance in your existing designs because each and every one is pin-compatible with industry-standard chips.

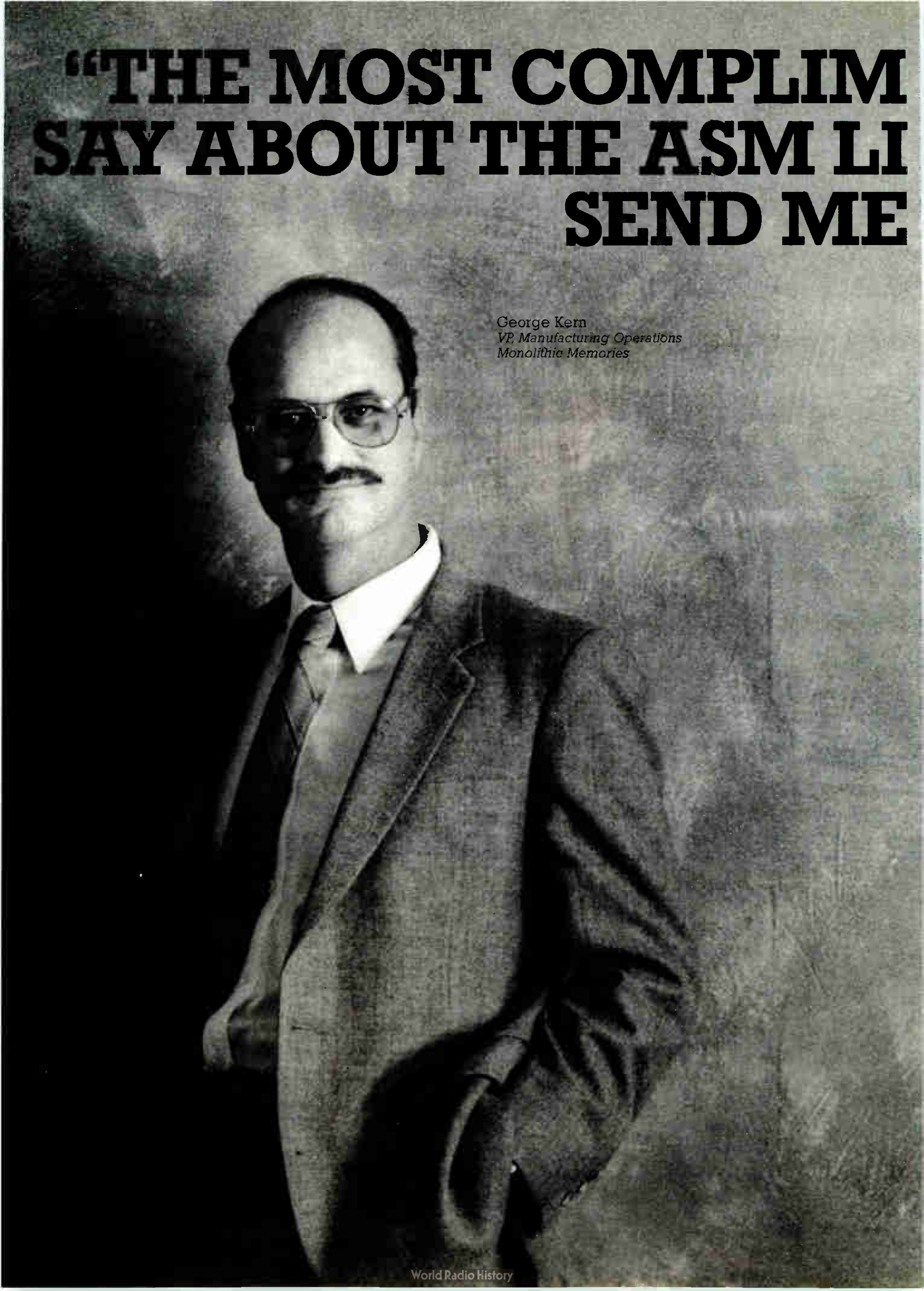
And we're developing tools to make them available for ASIC designs.

So phone VLSI Technology at 800-8-SAMPLE for more information and samples. Or write to us at 1109 McKay Dr., San Jose, CA 95131.

And see how you can blow the doors off your competition.

VLSI TECHNOLOGY, INC.

Circle 53 on reader service card



"THE MOST COMPLIM
SAY ABOUT THE ASM LI
SEND ME
George Kern
VP, Manufacturing Operations
Monolithic Memories

ENTARY THING I CAN THOGRAPHY STEPPER? FOUR MORE!"

Monolithic Memories, the premier manufacturer of PAL® devices and a large variety of memory products, did what few others could during the semiconductor industry slump. They prospered.

Not only did MMI offer the products the market wanted, they knew how to manufacture them efficiently. The recent purchase of steppers from ASM Lithography helps MMI continue fine-tuning their fabrication process.

According to Mr. Kern, *"ASML's specifications created high expectations for our first units. We certainly weren't disappointed. Performance has been so good, in fact, we've increased throughput by more than a third.*

High production of revenue-generating devices is determined by many factors. Among the most important are increased utilization and throughput. Areas where ASML steppers stand out.

They're fast, completely automatic, need no tedious baseline adjustments and achieve exceptional overlay in global-only mode. So you get more wafer passes a month.

"Overlay accuracy and yields both exceeded our previous steppers' by half," says Mr. Kern. *"As important, to my mind though, was uptime – over 90%. These things are reliable. They're a terrific addition to our high-speed production lines."*

A purchase of another four ASML steppers will help MMI continue extending their product offerings. The new steppers will be used in both their CMOS and Bipolar areas.

"You can believe we'll keep our latest ASML steppers just as busy," he adds.

We invite you to find out more about ASM Lithography steppers. For application notes, case histories, and our informative 20-page brochure, "The New Standard in Wafer Stepper Technology," contact us at any ASML address. You'll see, ASML steppers speak for themselves.

ASM Lithography, Inc.
2315 W. Fairmont Drive
Tempe, AZ 85282
USA
602-438-0559

ASM Lithography, B.V.
Meierijweg 15
5503 HN Veldhoven
The Netherlands
40-580800

ASM Asia
6 / F Watson Center
16 Kung Yip st. Kwai Chung
Hong Kong
(0)297961

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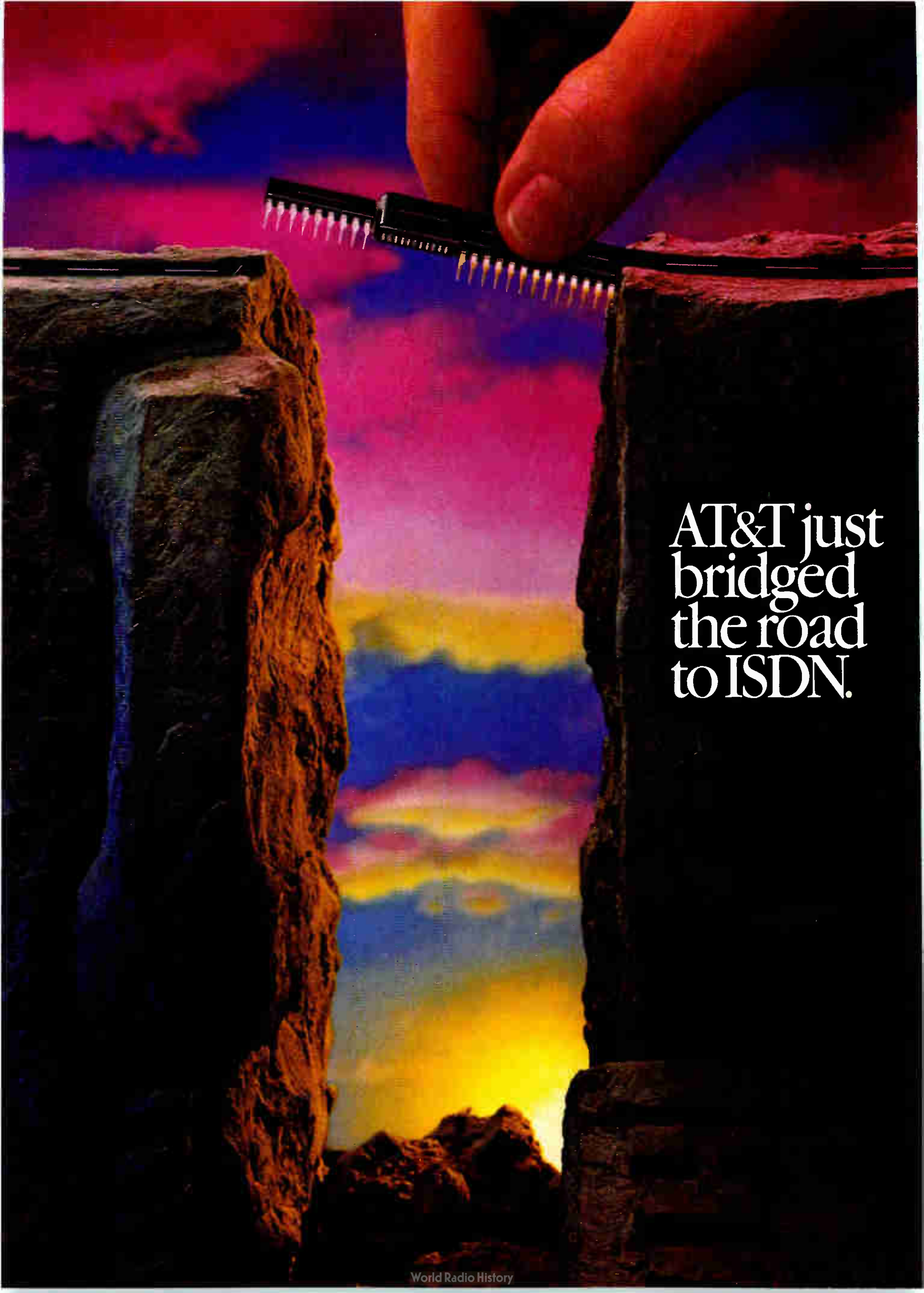
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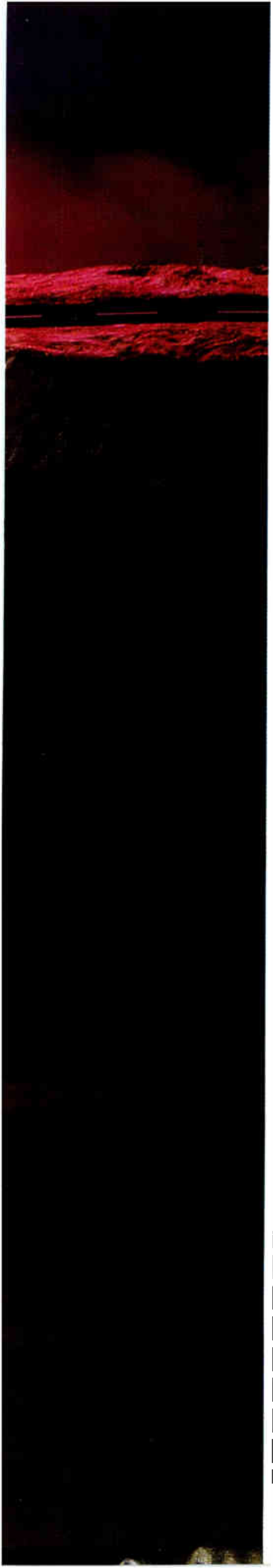

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Circle 57 on reader service card

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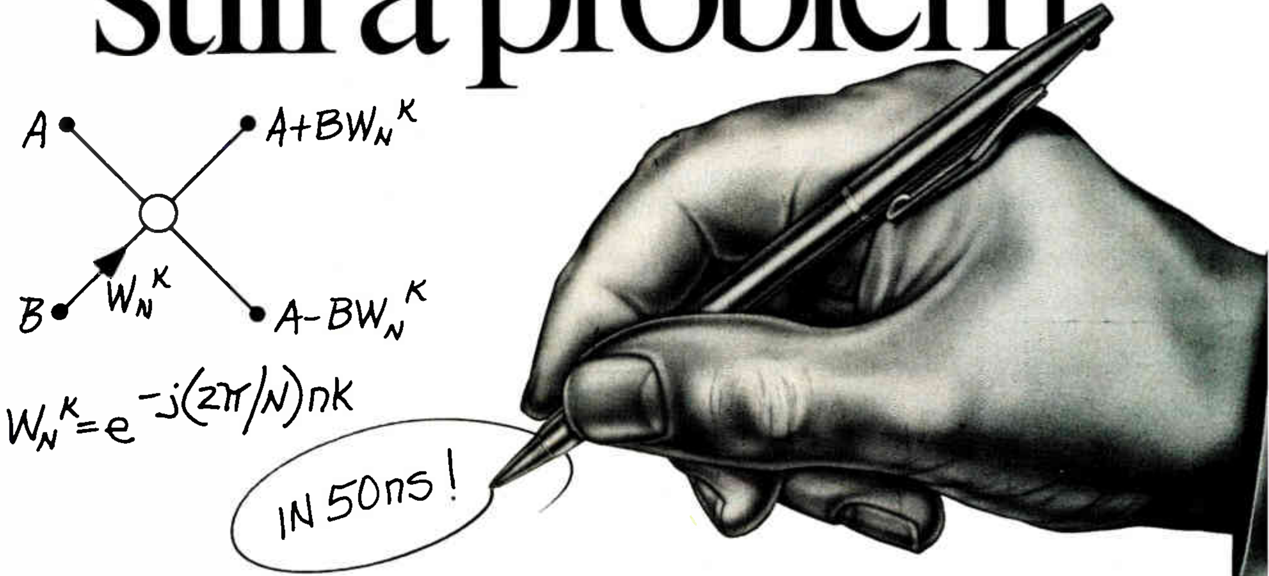

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THE FRANTIC SEARCH FOR MORE SPEED

Impatient with the rate of improvement in the speeds of standard microprocessors, computer designers switch to RISC chips, try new kinds of CISC, or go it alone with their own designs

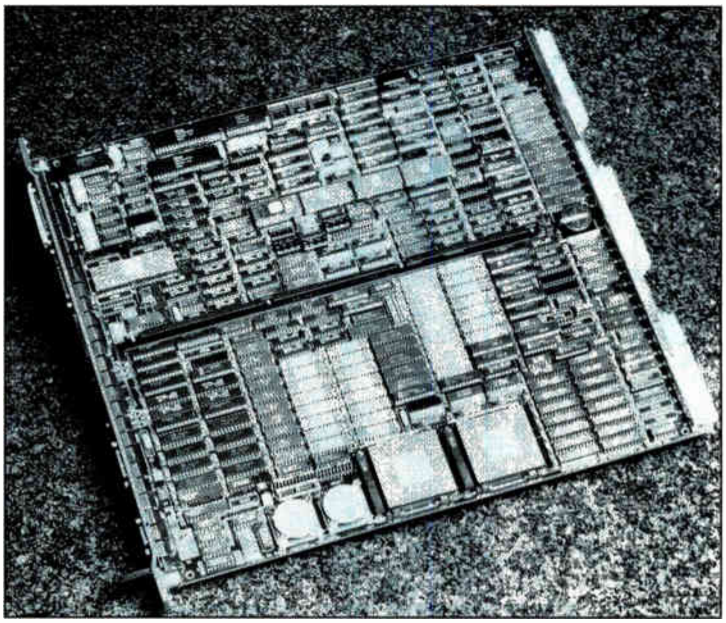
by Tom Manuel

Standard microprocessors may be running out of steam. Computer makers accustomed to building their products around them are now demanding such increases in performance that these needs are outstripping what chip makers can deliver with their standard microprocessors. In the frantic search for more performance, a growing number of computer designers are abandoning off-the-shelf microprocessors and heading off in three different directions.

Some are designing their systems around one of the burgeoning number of reduced-instruction-set computer (RISC) chips and others are reimplementing a standard complex-instruction (CISC) set with design techniques borrowed from RISC and mainframe features to get a RISC-like performance. A small band of designers are striking out on their own with proprietary designs, while a diehard group is still using standard microprocessors, hoping they will catch up in this accelerating performance race.

European computer companies, like their U. S. counterparts, are embroiled in a similar search for performance and are embracing the same alternatives. However, the Europeans are jumping more quickly into a commitment to open systems using industry standards, such as the Unix operating system (see p. 62).

There are important tradeoffs for each of the four approaches. For example, many proponents of RISC accept it as a savior, but its critics dismiss it as a passing fad. Bill Joy, vice president of research and development for computer and work-station maker Sun Microsystems Inc., believes the debate between RISC and complex instruction set computers is over and that RISC has won (see p. 64). In contrast, Phillips W. Smith, chairman and chief executive officer of Scottsdale, Ariz., supermicrocomputer maker Edge Computer Corp. says that RISC versus CISC is not the issue (see p. 65) and that processor designers can achieve the high performance of RISC with a CISC instruction set. What's more, his company has done it (see p. 66) with the design



1. BIG RISC. The Sun 4/260 computer's central processor board carries a new RISC architecture processor chip that delivers a whopping 10 mips.

WHAT DETERMINES CPU PERFORMANCE?

T = N•I•C

T = TIME TO EXECUTE PROGRAM
N = NUMBER OF INSTRUCTIONS IN PROGRAM— A FUNCTION OF ARCHITECTURE AND COMPILERS
I = AVERAGE NUMBER OF CLOCKS PER INSTRUCTION— A FUNCTION OF ARCHITECTURE AND IMPLEMENTATION
C = BASIC CLOCK CYCLE TIME— A FUNCTION OF CIRCUIT TECHNOLOGY

of the Edge 2000 central processing unit.

Joy argues that RISC and software compatibility can both be achieved if a standard operating system such as Unix is used. Joy's proof is that his Mountain View, Calif., company did it with a RISC processor for the central processing unit in its recently introduced Sun 4/260 computer (see p. 72). Sun can point to a RISC CPU board rated at 10 million instructions/s (see fig. 1).

Some companies, such as Ridge Computer Corp., have been using RISC architecture long enough to have developed next-generation processors. The Santa Clara, Calif., company is readying a superminicomputer that will use a third-generation, VLSI version of its RISC CPU (see p. 70). But not every company is embracing RISC for high performance: an upstart startup, Davin Computer Inc. of Irvine, Calif., is planning to build a powerhouse machine using a very complex set of instructions—and a 64-bit word size (see p. 73).

RISC machines tend to do better than popular standard microprocessors when measured by a simple formula for processor performance (see chart, left), in which the time to execute a program is a product of three parameters: the number of instructions in a program, the average number of clock cycles per instruction, and the clock cycle time. The resulting execution time is raw processor performance, with no systems considerations—waiting for data from memory or for a peripheral to respond, for example, or stopping for interruptions from other processors—factored in. Extensive benchmarking of systems is required to complete the performance picture.

One method of comparing performance comes from a plot of the average number of cycles per instruction and clock speed (see chart, below). It shows that a flood of new processors, both RISC and CISC, are crowding down to the lower levels of cycles per instruction. And some also are pushing to much higher clock speeds. The number of offerings that outstrip standard microprocessors and future microprocessors that will move into RISC territory give system designers a lot to choose from.

However, the choice is not an easy one. The four paths to performance have various advantages and disadvantages—enough of each so that no one emerges as clearly the best.

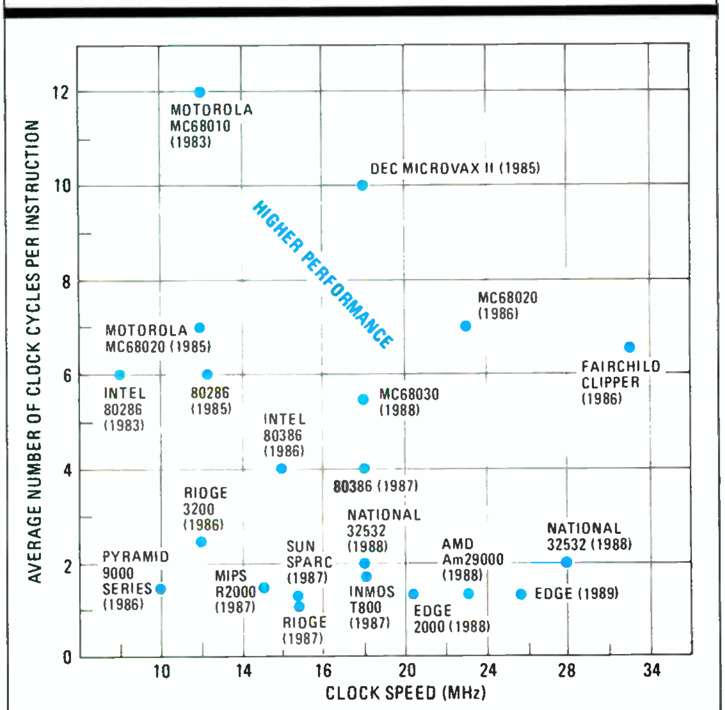
A reduced-instruction design will give a company an advantage over the standard microprocessors now available—if the RISC processor is ready on schedule. The risk of being late with a product—getting to market after competitors or missing a product cycle completely—carries a high penalty. Also, if the computer vendor has not been using a standard operating system, getting proprietary software to run on the RISC machine could cause such a delay.

On the other hand, once the architecture and the software are checked out, a RISC processor is easier and quicker to implement in a hotter technology than a CISC design. Its inherent simplicity gives it the edge here.

The second approach, implementing a standard microprocessor instruction set with high-density, high-speed, VLSI application-specific integrated circuits, can also leapfrog standard chips. This direction poses few software risks since compatibilty is automatic when the standard instruction set and operating system that the vendor has been using all along is incorporated. Like the RISC approach, this is a semicustom approach, so problems could arise if the designers or the design tools are not up to the task. Also, such a processor will probably cost more than standard microprocessors because the chip volume for ASICs is much lower than that for standard chips. Yet the performance advantage could be worth it.

The safest approach for system vendors is to

THE QUEST FOR SPEED LEADS TO A CROWDED FIELD



stay with their chosen microprocessor supplier and ride his price/performance curve. There is no need to worry about software compatability as long as the chip supplier remains committed to its instruction set. The danger here is too low a level of performance to satisfy every customer's demands. Also, product introduction schedules may be at the mercy of the chip supplier's delivery performance.

The fourth approach is the most daring of all. Here a company leaves a well-trodden path of the standard microprocessor and blazes a new trail—in some cases with a new CISC or super CISC architecture, in others with a very long instruction-word machine, in still others with some radically different design.

The possible advantages are extraordinary performance, a price/performance breakthrough, creation of a distinctive product for a niche market, or enabling a whole new market to emerge. Disadvantages include the danger that the high performance might only be applicable to certain types of applications. Niche markets can prove to be too small. Projects could be too ambitious and either take too long or be abandoned because they don't work.

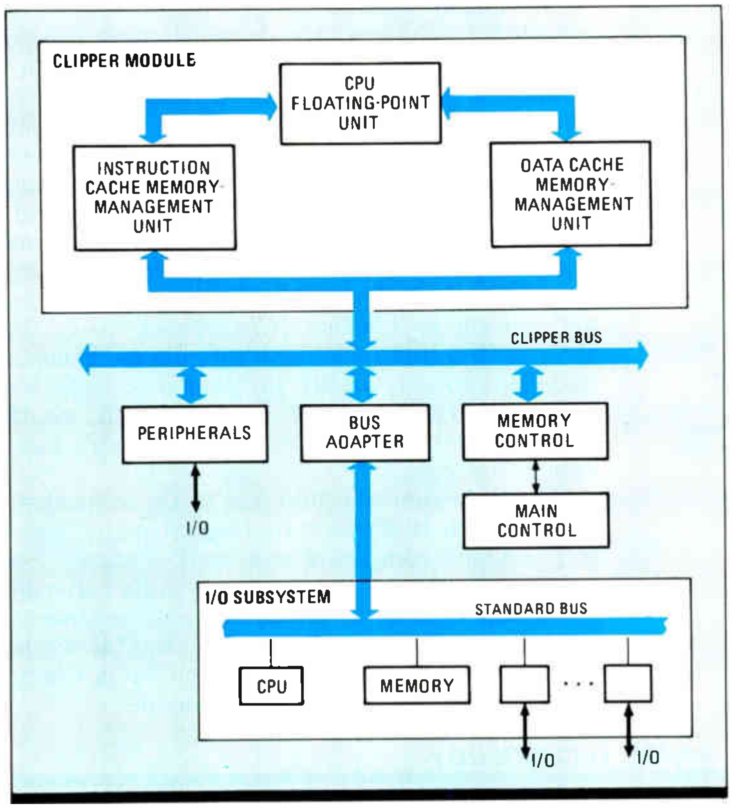
Taking the first approach—a RISC architecture—are Sun, Ridge, and several other companies. Celerity Computing Inc. is boldly taking RISC where it has never gone before—to high-speed bipolar circuits. The San Diego superminicomputer maker will up the clock speed of its new RISC processor by using the emitter-coupled logic VLSI technology from Bipolar Integrated Technology Inc. in Beaverton, Ore. [*Electronics*, April 7, 1986, p. 35].

At least one company is so confident about RISC technology that it has made it its line of business. MIPS Computer Systems Inc. offers its RISC technology as chips, boards, and systems. The Sunnyvale, Calif., company has recently introduced a chip set, consisting of RISC processor and floating-point unit, that is rated at 10 mips [*Electronics*, Aug. 20, 1987, p. 83].

One RISC pioneer, Pyramid Technologies Inc., is striving to keep up. Pyramid, which has been shipping RISC products since March 1984, is busy implementing its processor in faster VLSI technology. The Mountain View, Calif., company also has been moving gradually to multiple RISC engines in its computers. The latest model is a four-processor system.

A example of specialized RISC is the implementation of the military 1750A instruction set on a RISC chip by United Technologies Corp. Microelectronics in Colorado Springs [*Electronics*, March 19, 1987, p. 97]. The UT150AR operates in a 1750A emulation mode and a native RISC mode, delivering up to 6 mips in the latter.

The second approach is using standard microprocessors, which are not all that standard these days. Chips like the enhanced RISC microprocessor being built by Advanced Micro Devices Inc.



2. MIPS DENSITY. The small 3-chip module of cache and two processing units in the Fairchild Clipper compute engine steams up to five mips.

for delivery early next year, for example, combine RISC and big computer features [*Electronics*, March 19, 1987, p. 61]. The Sunnyvale, Calif., company's Am29000 will achieve an impressive average number of cycles per instruction of 1.4.

National Semiconductor Corp. is getting into the architectural enhancement act, too. The Santa Clara, Calif., company is using classic mainframe computer techniques to pare the number of cycles per instruction to 2 in its new 32532 processor. The National designers have embraced the RISC attribute of a large register set—the 532 has an on-chip data cache that doubles as an equivalent to a large register set of 640 data registers.

Mainframe and supercomputer features in a small module make the Clipper three-chip processor by Fairchild Semiconductor Corp. stand out. The big-computer architectural features include separate instruction and data caches, each with its memory management unit and a bus adapter for independent input/output subsystems (see fig. 2). A CPU plus a floating-point unit and a complete cache system, all in a small module, deliver up to 5 mips of performance.

While the Clipper's average of 6.7 clocks/instruction is not down to the RISC range, its fast 33-MHz clock speed makes up for that. Also, "the Clipper can be improved by taking clock cycles out of instructions, and we will be doing this," says Gary Baum, strategic marketing manager for Clipper products at the Palo Alto, Calif., company.

The microprocessor market leaders Motorola Inc. and Intel Corp. are doing all they can to help their customers keep performance up. Motorola's newest 68000 family member, the 68030 due out late this year (see p. 87), is targeted for higher-performance products by most of the vendors currently using the 68020, including Sun. And Force Computers Inc. has designed an advanced VMEbus interface chip, and a processor card using it, around a 68020 now and is ready for a 68030 from Motorola's Semiconductor Products Group in Phoenix [*Electronics*, Aug. 20, 1987, p. 66]. However, industry rumors indicate that Motorola is about to go public with its MC78000 RISC processor design, which would have interesting implications for Motorola's marketing strategy.

Having beaten the Motorola 68030 to market, Intel's 80386 is already running in many high-end personal computers and work stations. Sequent Computers, for one, uses it in its high-end Symmetry series of multiprocessor computers [*Electronics*, May 28, 1987, p. 76]. Intel is working on a follow-on product, but the Santa Clara, Calif., company declines to give details.

When it comes to proprietary processors, the Davin BAT 6420 may be the latest one to be revealed, but it is not alone. The Inmos Ltd. T800 transputer is another: RISC with a twist [*Electronics*, Nov. 27, 1986, p. 51]. It has a very powerful floating-point unit, four high-speed communications links, and memory on chip. Both Multiflow Computer Inc. and Transcept Systems Inc. have chosen a very long instruction-word architecture for their Trace supercomputer and TAAC-1 application accelerator, respectively.

The big advantage of a very long instruction word is the degree of low-level parallelism at the instruction level. The Multiflow and Transcept machines have many processing elements and high-bandwidth data and instruction paths. Each wide instruction word contains multiple operations. Very long instruction-word architectures hold out the promise of high processing efficiency since each instruction directs the performance of many operations in parallel. Each long instruction completes execution during one machine cycle. For users of the Multiflow Trace machines and the Transcept TACC-1, lightning performance is a reality. □

INSIDE TECHNOLOGY

EUROPE BETS ON STANDARDS TO GET MORE PEFORMANCE

Most major computer vendors are abandoning proprietary systems and moving to off-the-shelf microprocessors and Unix; a consensus emerges for RISC

by John Gosch

In its drive for more performance, Europe has largely abandoned proprietary designs for its small and medium-size computers. It is turning elsewhere, chiefly to the U. S., for the most advanced technology it can get, sticking to the microprocessors, buses, operating systems, and other hardware and software that are de facto standards.

At the same time, most of the European companies are taking the standard commercial elements of their systems and shaping them into different architectures. As they do so, the Europeans find themselves embroiled in issues now under debate in the U. S. Chief among these is the debate over reduced-instruction-set vs. complex-instruction-set architectures, where a consensus seems to be emerging in favor of RISC to boost performance on the high end.

While the Europeans are divided over some issues, they are working together on other projects. Their efforts have culminated in the X/Open group [*Electronics*, July 10, 1986, p. 121], in which most of the major European computer vendors are working to establish standards based on the Unix operating system.

The support for standards among the leading European suppliers begins with the strategy of building systems around the newest standard microprocessor families rather than proprietary hardware and architecture. West Germany's Siemens AG, for example, made a radical shift in early 1982 away from proprietary bus systems and processors made in-house "to a standard microprocessor, a standard bus, and a standard operating system," says Hans W. Strack-Zimmermann, a senior director at the company's Data Systems Division in Munich. Reflecting

Strack-Zimmermann's standards credo is Siemens' family of midrange microcomputers and supermicros designed around 16- and 32-bit microprocessors from National Semiconductor Corp., the Multibus I (and eventually Multibus II), and Unix. The latest members of the family are part of the new the MX500 series. It includes the MX500-20, with 4 to 8 Mbytes of main memory, which serves up to 16 work stations; the MX500-40, 8 to 16 Mbytes, which handles 24 work stations; and the MX500-60, 10 to 16 Mbytes, which accommodates 32 work stations.

As it developed its standards strategy, Siemens avoided RISC systems. Strack-Zimmermann is not convinced that RISC pays off. "The performance increase that RISC provides is not enough to justify the enormous expense needed to convert development and production to incorporate RISC technology," he says.

Although virtually all of the European companies resemble Siemens in the use of standard parts and commitment to Unix, most of them disagree with Strack-Zimmermann's opinion of RISC. For example, West Germany's other leading computer company, Nixdorf Computer AG, fields Targon, a line of computers similar to Siemens' systems in that both use Motorola's 68000 microprocessors and Unix. But at the high end, the line diverges sharply, depending on RISC processors for more performance.

Targon ranges from professional work stations to fault-tolerant multicomputer systems. The line includes the Targon/31, which uses a 32-bit architecture based on Motorola's 68000; the Targon/32, a multicomputer system with up to eight computers coupled via high-performance buses; and the Targon/35, running at 6.5 mips, which uses RISC CPUs from Pyramid Technology Corp. in Mountain View, Calif.

Wolfgang Raum, head of Nixdorf's Decentralized Systems Division, for one, says that standard microprocessors are fine for systems supporting up to 32 work stations, but they won't work well for systems that must accommodate from, say, 40 to 200. Here, fast RISC processors must be used for more performance, he says.

Similarly, the Italian computer maker Ing. C. Olivetti & Co. builds personal computers based on Intel Corp.'s 80386 and minicomputers based on Motorola's 68020, says Elserino Piol, executive vice president for strategy and development. But it also makes a personal computer, the Archimedes, based on a proprietary RISC architecture developed by Acorn Computers in the UK. In operating systems, the company's main thrust is Unix.

In France, Bull has been using RISC architecture for several years in its SPS9 minicomputer. Bull's RISC architecture was designed by Ridge Computers Inc. in Santa Clara, Calif. (see p. 70).

Across the Channel in London, Whitechapel Workstations, the leading European vendor of high-performance graphics work stations, also embraces both industry standards and RISC. Based on the RISC chip set from MIPS Computer Systems Inc. in Sunnyvale, Calif., the Whitechapel systems support Unix, X Windows, and other standard protocols and software.

Philips of the Netherlands is also committed to standard processors and, with the introduction of its P9000 family, to Unix. Designed around Motorola's 68020, the P9000 family consists of minicomputers functioning as the integrated-system servers or departmental processors. It has two implementations: the P9X00 and P9070.

The P9X00 is a departmental minicomputer system combining the advantages of monitoring and control features such as are available on a mainframe. The P9X00 has an MPX operating system, which is a multiprocessor version of Unix.

The P9070 is a high-performance system with a full implemetation of the standard VMEbus architecture. The CPU includes a 16-Kbyte cache memory and a floating-point coprocessor. Up to 16 Mbytes of random-access memory and a variety of intelligent disk, tape and communications controllers are supported.

The P9000 family "is a Unix system following the specifications for portability defined by the X/Open group," says Gerd Bindels, senior managing director of the Philips Telecommunication and Data Systems Division.

STANDARDIZING. Siemens uses National Semiconductor processors and the Unix operating system for its midrange MX500.

X/Open embodies the European commitment to standards. Its 11 members have defined a standard software environment built on interfaces to Unix. Their aim is to provide portability, particularly for applications software, allowing users to mix and match both hardware and software from different suppliers.

X/Open now numbers four American companies among its membership—AT&T, Digital Equipment Corp., Hewlett-Packard, and Unisys—along with seven European companies. They are Bull, Sweden's Ericsson, Great Britain's ICL, Nixdorf, Olivetti, Philips, and Siemens. Industry watchers expect more companies to join soon.

OPINION

IT'S NO CONTEST: RISC HAS WON

BILL JOY

As vice president of research and development for Sun Microsystems Inc., Joy, 33, guides the company's technology thrust, especially in software. Before cofounding Sun, he was the senior architect of the Berkeley Unix operating system at the University of California at Berkeley. There he designed and implemented the 4.1bsd version of Unix. He is also responsible for the virtual memory and networking enhancements in that version of Unix.

The CISC vs. RISC debate is over in the microprocessor world. You do complex-instruction-set single-chip computers only if you have to.

There are two major categories of potential RISC users. Vendors who use the AT&T Unix operating system enjoy portable software, so they can go to reduced-instruction-set computers easily. And vendors with proprietary architectures and a lot of code written in low-level and machine-dependent ways must look to using RISC ideas to make their machines run faster. But such systems will be more expensive and/or slower than pure RISCs implemented in the same time frame.

A good example of a Unix-based system is Sun's scalable processor architecture (Sparc), a RISC design with three implementations (see p. 72). All these implementations are fully compatible and run the range of software available on Sun's CISC 680X0-based work stations. Other vendors who wish to implement systems using this processor family can license operating-system software and compilers from the silicon vendors and additional software from Sun and its value-added software suppliers. This is all available today. So much for any software problem.

Sparc's performance range of 10 to 50 million instructions per second is achievable today only with RISC microprocessor technology. We expect it can be extended further by using more aggressive technologies, perhaps with a GaAs microprocessor. Nonmicroprocessor implementations that achieve the same performance will not be cost-competitive with microprocessors. For the moment, this performance is achievable in the technologies used in the three Sparc implementations only with a simplified architecture: more complicated CISC architectures simply wouldn't fit in any usable area of silicon.

A key point here is that we are in the age of the microprocessor, so the debate over RISC versus CISC in micros is a debate over the future of computing. At the dawn of the microprocessor age, early microprocessors made personal computers possible. The 32-bit processors made work stations possible, bringing the performance of superminicomputers to the desktop. Now, with pipelined microprocessors and RISC architecture, extremely fast personal systems are possible. Work stations as fast as 100 mips will appear in the office in the next five years as the era of super work stations arrives: machines with very fast processors and powerful graphics.

So in the struggle to keep up with RISC, many vendors are improving existing CISC implementations by adopting features promoted by all RISC implementations: single-cycle execution, hard-wired control, and so on. By focusing on predecoding instructions into instruction caches, they can achieve a measure of simplicity that RISC implementations achieve by using fixed-length instructions and a load/store architecture.

But the CISCs remain more complex than the RISCs. Especially in the next few years, the best technologies will have limitations on the complexity they allow to be implemented in a single chip. So CISC chips will trail RISC chips in performance. For CISC to achieve the same performance as RISC often will require a board, rather than a chip, for the processor.

In the future, CISC microprocessors will become more possible in advanced technologies, such as very dense CMOS—but at the same time RISC will have additional silicon area that can be put to productive use. It's important to remember that, just as there are a range of techniques that can be applied to CISC machines to make them run faster, there are things that can be done in RISC implementations to run even faster. So by the time there are CISC microprocessors running with 1.5 cycles per instruction, there will be RISC microprocessors running two instructions every 1.5 cycles.

We think RISC is ahead to stay, at least until something better than either CISC or RISC comes along.

OPINION

CISC CAN STILL DELIVER THE GOODS

PHILLIPS W. SMITH

Brought in as Edge Computer Corp.'s chairman and chief executive officer in August 1986, Smith, 48, has extensive experience managing growth operations. He was CEO and president of CAE Systems Inc., both before and after its sale to Tektronix Inc. Before that, Smith was the vice president of marketing at Computervision, where he was responsible for worldwide marketing activities. Earlier, he spent four years with Bausch & Lomb and nine years at Lear Siegler.

Being a slave to fashion is an epithet usually associated with the salons of Paris instead of the executive suites of Silicon Valley. But the current excitement over reduced-instruction-set technology could result in some companies rushing to this latest status symbol without doing a "reality check" to determine if it really is going to fit their needs.

Like any fashion trend, systems based on RISC architecture are going to be right for some people but wrong for a lot of others. And by adopting some of the RISC characteristics, complex-instruction-set computers can achieve RISC performance levels.

I think that that most of the original-equipment manufacturers debating the RISC versus CISC issue these days seem to overlook or downplay what is, to me, an absolutely key issue. OEMs with CISC architectures that try to add to the high end by going to a RISC machine create enormous—and unnecessary—problems, especially when it comes to adapting software. This approach results not only in two incompatible architectures that have to be supported and maintained; it also creates two separate lines for which operating systems, diagnostics, compilers, high-level languages, and third-party applications need to be developed and supported.

The ongoing maintenance cost for two separate sets of systems software is extremely expensive. It's very similar to an airline company buying both DC-10s and L-1011s for its fleet. The airline will have to stock two sets of parts, train mechanics in two different maintenance routines, and so on.

Clearly, the aspect of RISC that has generated so much interest is the promised leap in performance. On the surface, RISC truly offers that, although there definitely are penalties in this approach. Some of the penalties are short-term and transitory, such as the lack of software and software-development tools, and of system-level architecture to harness high-density computing. But the cost and strain of maintaining two different architectures are not problems that will go away with time.

This gives rise to the question of whether there is a way to achieve both objectives. Is it possible to deliver RISC-like efficiency using a CISC instruction set? Edge's answer is yes. Through appropriate design, it is indeed possible to attain performance in the RISC category without having to abandon the architecture used in the existing machines of a company's product line.

Part of the confusion, I believe, is that of the four tenets usually cited as characterizing RISC architectures—only two of which are actually architectural issues. The four are fixed instruction length, a load/store architecture, single-cycle execution, and hardwired control. These characteristics are cited as the unique way in which the RISC approach is able to reduce average instruction time.

Actually, only fixed instruction length and load/store architecture relate to the architecture of RISC. Single-cycle execution and hardwired control are descriptions not of the architecture, but of the way the architecture is implemented. And they can be accomplished in a CISC design as well as in RISC.

This isn't theory. It's proven, as our new Edge 2000 system attests (see p. 66). That machine achieves single-cycle execution and uses hardwired control. In addition, it achieves performance levels that previously have been accomplished only through RISC architecture in a superminicomputer. More important, it permits preservation of a company's investment in its software base.

The real issue, it turns out, isn't RISC vs. CISC, but the attainment of a high-performance engine without having to abandon existing software and without needing to support two different machine architectures. It can be done.

GETTING MAINFRAME POWER OUT OF A CISC SUPERMICRO

Edge Computer more than doubles the performance of fastest RISC designs with its complex instruction-set architecture; running 68030 code three times faster

by Tom Manuel

Edge Computer Corp. is about to jump way ahead of the competition in the big push for more computer performance from microprocessors. The Scottsdale, Ariz., company has designed a supermicrocomputer system that wrings faster performance out of a conventional complex instruction set than others are claiming for the reduced-instruction-set architectures that are being touted often these days as the performance leaders.

The Edge 2000 implements the instruction set of the Motorola 680X0 series of microprocessors, but it delivers up to seven times the throughput of other systems built with the same microprocessors. It also boasts double the performance of the fastest RISC processors.

The biggest advantage Edge's design has over RISC processors is that its superior performance can be used to run existing 680X0 programs without change. That means the machine offers builders of 680X0-based systems a painless, cost-effective way to add to the top end of their product lines.

Edge is a four-year-old maker of high-performance Unix systems based on the 680X0 series instruction set (see p. 69). It plans to produce a family of products based on the Edge 2000 architecture, ranging from board-level products to complete computer systems. Company spokesmen say the products will be aimed primarily at original-equipment manufacturers.

The Edge design team plans a high-end machine that will use four processors and deliver up to 112 million instructions/s at peak; 69 mips sustained; and up to 1 gigabyte of physical memory. This maxisystem will not be available until 1989. The first product, a single-processor system called the Edge 2112, rated at 12 mips of sustained performance with a peak performance of 16.7 mips, will be available for beta test sites in early 1988. By the second quarter of 1988, production units with one, two, and four processors will be ready, with the most likely applications being large multiuser systems and as the processing engine in new super work stations. The Edge production machines will range in performance from 16 to 89.6 mips. The processors will have a clock cycle of 45 ns. Systems scheduled for early 1989 will have processors implemented in faster circuitry with a clock cycle of 35 ns.

This breakthrough in performance promises to deliver mainframe levels of performance at the size, power requirements, and cost levels of supermicrocomputers. Edge is promising price/performance of $1,000 per mips by early 1989. The current price/performance leaders among microprocessor-based multiprocessor systems are pushing as low as $8,000/mips; run-of-the mill systems rank at about $14,000/mips. Superminicomputers cost closer to $100,000/mips; mainframes, about $130,000 to $170,000/mips.

The keys to the Edge systems' performance are advances in processor architecture and advanced CMOS gate-array technology for the processor. The high-performance central processing unit is based on two of the four basic tenets of reduced-instruction-set computers: single-cycle instructions and hardwired control. It also incorporates several mainframe features, such as pipelining, three kinds of cache, and separation of instruction fetching from execution. The design team also chose a system structure that uses a proprietary high-bandwidth system bus and very large main memory to accommodate large applications, hundreds of simultaneous users, and multiple processors.

To design balanced-performance systems, designers must make sure that no one area be-

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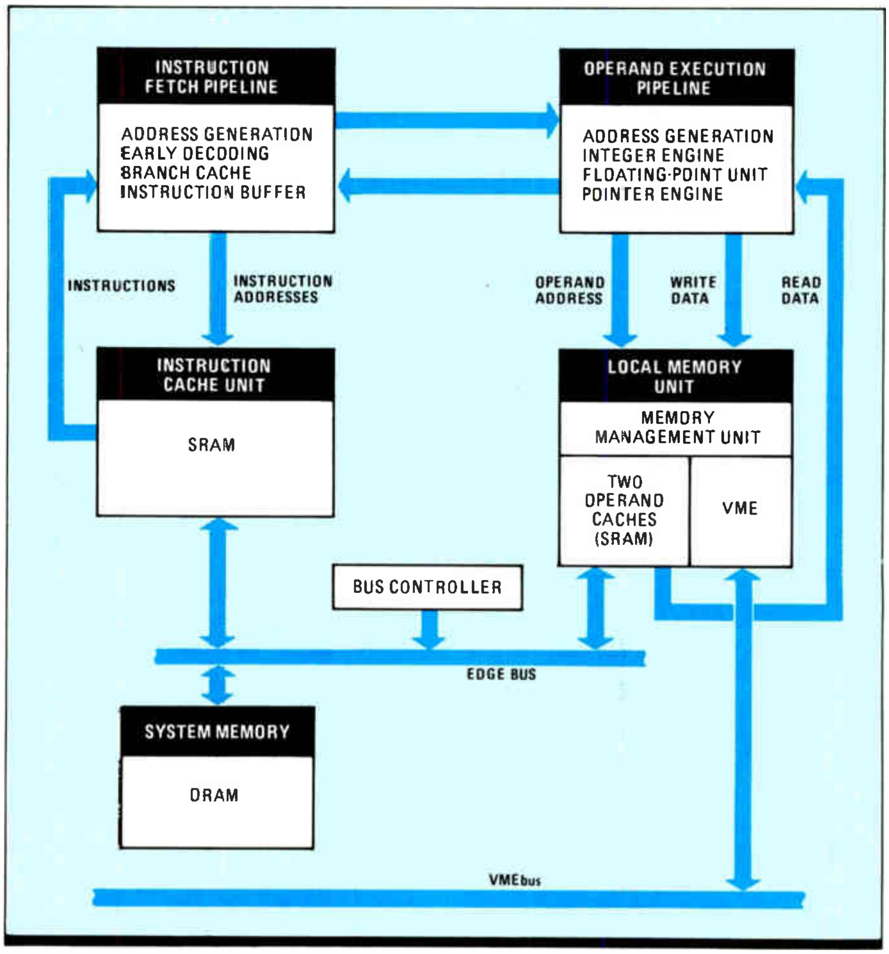
TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

comes a bottleneck. Common operations—fetching and decoding instructions from memory and delivering them to the CPU, getting the right operands from memory to the CPU, doing integer calculations, executing floating-point calculations, and transferring data to and from the peripheral input/output devices—can slow the machine.

To break these bottlenecks, the Edge CPU (see fig. 1) has two pipelines—an instruction-fetch pipeline and an operand-execution pipeline, each with its own cache subsystem. It also provided an I/O controller that works as a bus translator, so industry-standard I/O buses such as the VMEbus can be used for peripherals. The architecture achieves an average instruction time of 1.4 cycles/instruction—a ratio matching some and surpassing other RISC architectures, which strive for 1 cycle/instruction.

Edge also used another of the basic techniques of RISC, hardwired control rather than microcoded instructions. Borrowing the idea of hardwired control and the low ratio of cycles to instructions from RISC are major contributors to the design's achievement of RISC-level performance with a complex instruction set. The other architectural features, such as the two pipelines and the three caches, also contribute their share.



1. SYSTEM MAP. The Edge 2000 gets high performance from two pipelines, an instruction cache, a memory unit for operands, and a large system memory.

The instruction-fetch pipeline (see fig. 2) fetches program instructions and does some early decoding of them to set up optimum instruction streams for the execution module. The early-decode feature in the pipeline dynamically recodes the instructions before sending them off to the operand-execution pipeline. This recoding tells the execution pipeline the same things about the instructions that a RISC processor is told, such as detected changes in the instruction flow, contributing to efficient hardwired control of the execution pipeline. Branch and return information about the instruction path is kept in the branch cache and return stack within the instruction-fetch pipeline.

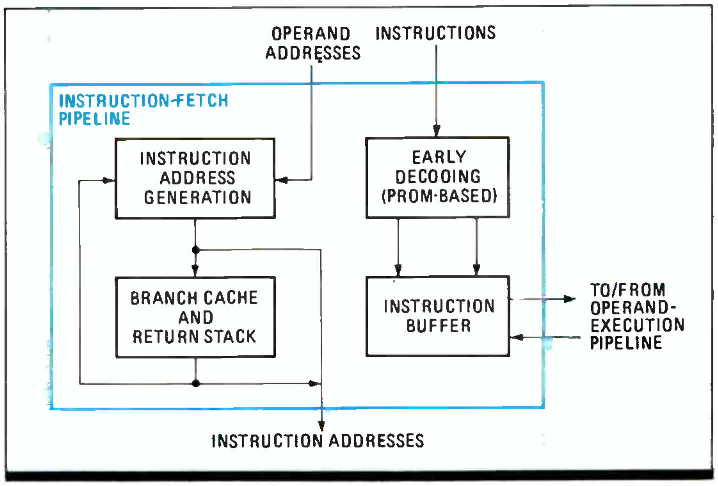
The instruction cache is 32 Kbytes with a two-set associative organization. It is a virtual cache with a 16-byte line. Separate supervisor and user valid bits are maintained for each set and the user entries are cleared on every context switch—the supervisor entries are left valid.

The operand-execution pipeline (see fig. 3) first generates operand addresses and fetches operands from its dual-cache local memory unit. The subsequent execution functions are divided among an integer engine, a fast, low-power emitter-coupled-logic floating-point engine, and a separate engine for handling pointers. The local memory unit contains the CPU's memory management unit, a VMEbus interface, and the two caches.

The pipeline's control logic governs the 64-bit interface with the instruction pipeline. The operand-address generator produces the addresses of the operands required by the decoded instructions. The generator supports all the addressing modes of the 680X0 instruction set, generating any address in one cycle. Operand addresses go to the local memory unit to be used to fetch the operands for the two execution engines from one of the two caches, the main memory, or the register stack located within the operand address generator.

The local memory unit, which provides the important function of getting operands to and from the execution engines quickly, fetches operands or stores results to and from either of its two caches. The two caches serving the operand execution pipeline are a 64-Kbyte four-set associative cache and a 448-Kbyte direct cache. Both use a copy-back strategy that reduces traffic on the main system bus.

The associative cache stores data from the



2. INSTRUCTIVE. The instruction pipeline generates and stores addresses and fetches and starts decoding instructions.

global memory's physical addresses between 448 Kbytes to 1 gigabyte. The copy-back management scheme uses four types of tags for complete coherency control: invalid, read-shared, read-exclusive, and written-exclusive. The copy-back protocol is totally hardware controlled. It is fast enough to monitor the system bus and keep all the caches coherent in a system that can have up to four CPUs—each with three caches—and four I/O controllers.

The direct cache maps the first 448 Kbyte locations (addresses 0 to 447 Kbytes) of the global memory's address space directly and singularly. This cache is also managed with a copy-back cache-control mechanism with the same tag types as the associative cache.

The designers intended that the direct cache provide programs with a large, fast static random-access memory for storing stacks. The 680X0 instruction set is based on heavy use of stacks—the Edge engineers measured many 680X0 programs and found that 30% to 50% of all memory accesses are to and from stacks. Since programs can direct the machine to move whole stacks into the cache, this feature speeds up program execution significantly.

Another key part contributing to high performance is the pointer-execution engine. It consists of tracking logic for register values, which can allow an instruction that modifies pointers and registers to move to the front of the pipeline without incurring a break in the pipeline flow.

Some of the newest and fastest circuit technology is being tapped by the Edge designers to implement all of the 68010 instructions and the most common additional 68020 instructions. For building most of the CPU, they selected 1.5-μm CMOS gate arrays with 30,000 to 50,000 gates from LSI Logic Inc. One Edge 2000 CPU uses five gate arrays in four designs. The engineers anticipate that in future systems they will go to 1.0-μm CMOS, which may be standard cells instead of gate arrays.

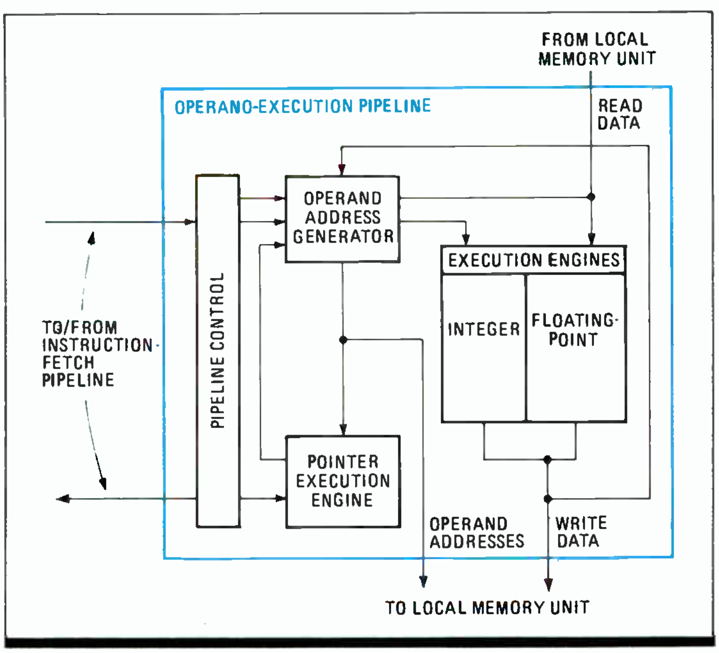
FAST FLOATING-POINT ENGINE

The fast integer execution engine is implemented as part of one of the system's CMOS gate arrays. For the floating-point execution engine the designers chose a very fast ECL floating-point unit made by Bipolar Integrated Technology Inc. [*Electronics*, Feb. 19, 1987, p. 88]. The floating-point chip set from BIT is implemented in the Beaverton, Ore., company's low-power, high-density ECL process and is rated by BIT at 60 million floating-point operations/s in raw performance.

The balanced Edge 2000 system with its 128-MHz system bus is designed to run with a very large global memory, which is needed for large numbers of users and big programs. The first system to be released will accommodate up to 64 Mbytes using 256-Kbit chips on four cards. With a move to 1-Mbit chips each card will hold 64 Mbytes and the system will go up to 256 Mbytes. With the availability of 4-Mbit chips, a system global memory of 1 gigabyte will be possible on just four memory cards—matching the Edge design's 1 gigabyte of physical memory address space.

The I/O controllers provide dual channels out to a secondary bus to keep that part of the total system in balance. Each I/O controller has a memory management unit and a direct-memory-access controller to map to the system's virtual memory and to handle direct memory access in hardware. So the Edge 2000 system looks like a 680X0 system to the disk drives and their controllers, as well as to user software. The I/O controller acts as a bus translator so that OEM customers can retain a proprietary or standard bus structure and preserve their investment in I/O subsystems. □

For more information, circle 480 on the reader service card.



3. BALANCING. In the execution pipeline, operands are fetched and instructions executed, while three execution engines help balance performance.

RACING TO FILL 'THE 15-TO-60-MIPS GAP'

A tiny company in the Arizona desert is getting ready to challenge the leaders in the superminicomputer and mainframe segments of the worldwide computer market. Edge Computer Corp. in Scottsdale sees a gap in the computer market, and it's racing to fill it.

Edge's management defines the gap as a need for systems akin to supermicrocomputers in size, power requirements, and cost, but with performance in the range of 15 million to 60 million instructions per second—performance that the most powerful superminicomputers are just starting to deliver and that mainframes have only recently attained.

Edge plans to deliver on its price/performance promise using industry standards. Its current Edge 1000 series and the new 2000 series (see p. 66) are compatible with the popular Motorola 68000 series of microprocessors—they use the same instruction set—and run the latest version of AT&T Co.'s Unix System V with Berkeley enhancements and extensions for multiple processors.

This grand strategy is a far cry from Edge's modest beginnings. In late 1983, when company president Alex B. Cimochowski and 10 engineers got together to start the company, their goal was to build a graphics work station. That machine was not a success—Edge is no longer selling it—but the company realized it had a high-performance processor on its hands and built a computer around it. The firm introduced the Edge 1 (now called the Edge 1000) in March 1986.

Ronald Bernal, director of advanced development and a company founder, heads the Edge 2000 team. The designers have worked together since they began creating the Edge 1 in early 1984; they then designed the dual-processor Edge 1200. They began work on the Edge 2000 in September 1986.

Now that the design is completed and board-level products and systems are being built, marketing takes center stage. Phillips W. Smith, who came to the company in August 1986 as chairman and chief executive officer, says, "Edge is sitting on a $1 billion opportunity." He arrives at that number in a simple but convincing way.

RON BERNAL. He is the guiding light in the development of the Edge 2000 architecture.

Smith first looks at what Motorola is selling. He estimates that Motorola will sell about 1 million 68020s this year. If those go into systems that sell for an average price of $10,000, that is a $10 billion market. Assuming that a conservative 10% of that market will move up into the high-performance gap above the 68020 and 68030, a $1 billion market opportunity emerges.

The marketing strategy put together by Smith, Cimochowski, and John Sims, vice president of marketing and sales, is to go after most if not all of that billion dollar market, focusing on very specific target accounts. "The profile of our target accounts is very simple, really; they are the original-equipment manufacturers currently using 68000s that are running out of performance," says Smith.

ALEX CIMOCHOWSKI. With 10 engineers, he founded the company in 1983.

The Edge marketing strategy is not limited to OEMs, but they are the most important first target. "Systems integrators are a significant opportunity long-range, as are value-added resellers," says Sims. But right now Sims is hiring salesmen to get to assigned 68000 system accounts through three contact points: engineering, marketing, and executive management. "It's pretty clear who we ought to be calling on," Sims says.

Edge is also negotiating a number of important large OEM agreements for the 2000, notably with several major European computer firms, says Smith. But he says that none of them can be announced yet and he will not say who the companies are. However, Ing. C. Olivetti & Co. of Ivrea, Italy, has indicated that it will make a significant announcement in November of a product based on 32-bit technology from Edge.

Olivetti is also one of the major investors in Edge. Beside the initial capital funding when the company was founded, venture capital funding has come in three rounds—$10 million in March 1984, $6.5 million in May 1985, and $17.5 million in October 1986. The company is still privately held, but current plans are to look toward an initial public offering in about the fourth quarter of 1988, market conditions permitting.

Smith's revenue and profit/loss projections call for nearly $10 million in revenue with a $5 million loss this year. He expects the company to turn profitable next year on $30 million in revenue, with revenues and profits rising to $120 million and $18 million respectively in 1990. *–Tom Manuel*

RISC TO HELP RIDGE MOVE UP INTO SUPERMINI CAMP

The company that led the way in the move to reduced-instruction-set computer architecture three years ago is pinning its hopes on a new RISC model to move back up to the front of the line. The 128-user superminicomputer is coming in the third quarter from Ridge Computers Inc., which has lately seen its product line getting squeezed by superminis on one side and high-powered work stations on the other.

The computer, as yet unnamed, will provide up to three times the power of Ridge's existing 64-user Ridge 3200 Model 9 system, and will cost $100,000—some $700,000 less than a comparable machine, Digital Equipment Corp.'s VAX 11/785 minicomputer. The jump into the supermini camp marks not only a technological leap forward but also a major restructuring of the Santa Clara, Calif., company's product positioning. It is scheduled to be introduced late this month.

"We were caught in what I would characterize as a positioning no man's land, somewhere between work stations and superminis," says Lawrence Lunetta Jr., vice president of marketing. It was clear, he says, that Ridge had to go one way or the other, and "we felt we were closer to a complete solution for the supermini market than we were for the work-station market."

To make a splash in this market, "we wanted a solid two-to-three-times performance improvement over the Ridge 3200, which is a 5-million-instructions/s machine," says Hugh Martin, vice president of engineering. So the company squeezed the 3200's four-board central processing unit down to a single printed-circuit board, increased the clock rate, and redesigned the processor to handle more operations in parallel.

At the heart of the design are two new CMOS chips: a main RISC integer processor and a floating-point chip. Both are implemented in a 1.5-μm CMOS gate array from Fujitsu and run at 16 MHz. The integer processor has its own general-purpose registers and load-and-store unit (see fig. 1). "Increasing the clock rate to 16 MHz, by using 1.5-μm VLSI instead of 2.0 μm, provided a 25% performance boost above the 12 MHz of the existing system," says Martin. To further up the ante, Ridge relied on parallelism, which "in effect reduces the number of clock cycles per instruction from about 2.5 to 1.3, including floating-point operations," Martin explains.

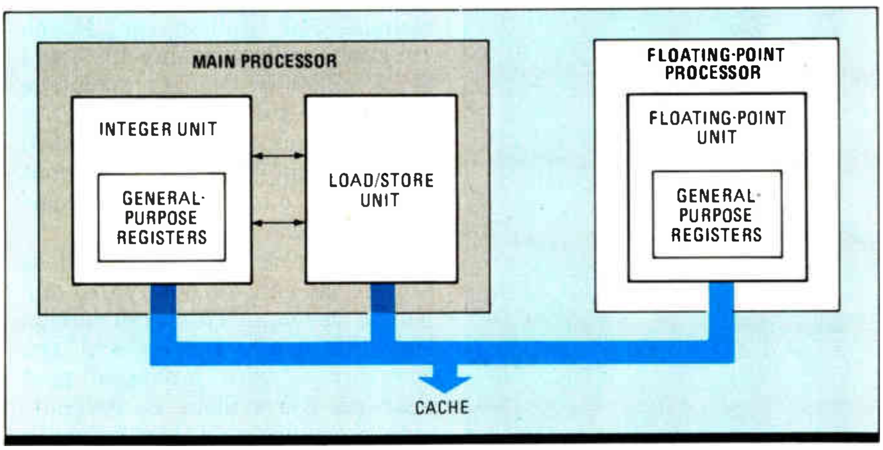
"That [parallelism] gets us almost the factor of two in performance," he says. Coupled with the 25% increase in clock speed, "it puts us in the area of a 2½ times performance increase. Then we also made some improvement in the compilers." The result is a product "just about three times faster" than the previous system.

The design achieves its parallelism by giving each chip its own set of general-purpose registers. A program sequence of five instructions—floating-point multiply, load, add, store, and increment—shows how the registers achieve this parallelism. A program must be arranged so that instructions in a given sequence do not use the same registers; if this condition is met, the instructions can be executed virtually simultaneously, rather than sequentially.

"If none of the registers conflict, it would take us only five clocks to do the five instructions—one clock per instruction," says Martin. This is where Ridge's changes to its C, Fortran, and Pascal compilers become important. "We modified the resequencer of the compilers to minimize the register conflicts between successive instructions," Martin says.

The results of the parallel registers and the reduction in register conflicts are dramatically illustrated by a short program sequence with five instructions (see chart, opposite). The total number of clock cycles for this sequence is reduced to half of what it would be with sequential operation.

Ridge is betting that this new computer will catapult it back into the forefront of the RISC world, where it was comfortably ensconced just three years ago. By



1. PARALLELISM. The new RISC computer on its way from Ridge runs its integer and floating point units in parallel; each of the processors has its own set of general purpose registers.

PARALLELISM CUTS CLOCK CYCLES		
Instruction	Sequential	Parallel
Floating-point multiply	5	1
Load	2	1
Add	1	1
Store	2	1
Increment	1	1
Total number of clocks for five instructions	11	5

(The clocks for the parallel case assume there are no register conflicts)

the end of 1984, its first systems were selling well in the U. S. work-station market to users who needed high-performance computation with a low price tag: $75,000 to $100,000. In addition, the Paris-based computer company Compagnie des Machines Bull, which owns just under 20% of Ridge, was selling Ridge systems in Europe, and the volume was beginning to swell.

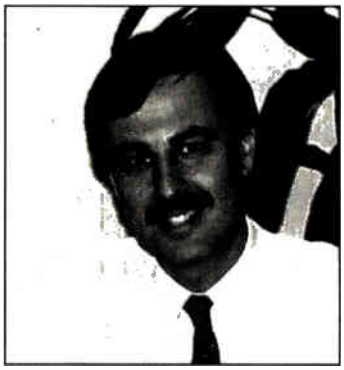
But in 1985, the company was stopped short by two events that threw its marketing plan into disarray. The first was DEC's introduction of the MicroVAX II, and the second was the advent of work stations based on the Motorola 68020 microprocessor, primarily from Sun Microsystems Inc. and Apollo Computer Inc. The MicroVAX brought high-power computing way down in price, eating into Ridge's market from the top. At the other end, the 68020 gave work stations enough power to rival the Ridge 32 Turbo/RX—especially since Ridge lacked a good user interface with high-powered graphics and the networking capability of the new stations.

ENHANCEMENT WITHOUT A DIFFERENCE

The Turbo RX, says Lunetta, was "an enhanced version" of the original Ridge 32, but it "did not have the performance differential required to really distance itself in the marketplace." The 64-user 3200, which the company announced in 1986, would have been the appropriate corporate response, but it was late and not distinctive enough to lure buyers away from the competition.

In addition, the market was beginning to split between work stations and superminis. Ridge products had the hardware characteristics of superminis, but like work stations they were multitasking, single-user machines—and that confused buyers. "By early 1986, we were experiencing fewer sales than in 1985, and the company was clearly at a crossroads," Lunetta says. And so last summer, Ridge cast its lot with the superminis—"a major repositioning."

To be competitive in this market, Ridge had to offer the standard Unix operating system. The



LUNETTA: "The company was clearly at a crossroads."

MARTIN: "We wanted two to three times the performance."

company was able to quickly pick up the Unix System 5 adaptation that Bull was offering on Ridge machines in Europe, and it added the Unix System 4.2 Berkeley extensions. "The availability of Unix on the system gave us a true multiuser time-sharing system, which we lacked before with the Ridge proprietary ROS operating system," Lunetta explains.

Now instead of competing with work stations, the Ridge computers will be working with them as servers in networks. For example, through a joint marketing agreement with Apollo, Ridge machines will be supported on Apollo's Domain network.

At the same time it was changing its product positioning, Ridge was also restructuring its senior management team. The restructuring was sparked by Robert Evans, a general partner in Hambrecht & Quist, the San Francisco-based high-technology venture-capital company that is the major backer of Ridge. In May 1986, Evans was sent by Hambrecht & Quist to evaluate the company. Evans subsequently joined the company in July 1986 as chairman and chief executive officer. The 59-year-old executive had spent 33 years at IBM Corp. and was corporate vice president of engineering, programming, and technology when he left for Hambrecht & Quist.

The company then recruited N. D'Arcy Roche as president and chief operating officer in October 1986. The 48-year-old Roche had worked at IBM for 25 years, then was president and chief executive officer at Soft Switch, a software company in King of Prussia, Pa.

In March, Hambrecht & Quist, Arthur Rock, and Groupe Bull brought in a $12 million round of financing, raising the company's total capitalization to $31,000,000. The two major investors in Ridge now own more than 80% of the company—Hambrecht & Quist 62%, with $12.3 million invested, and Bull at 19.5%, with a $7.2 million stake.

While Hambrecht & Quist has helped with management, Bull is helping Ridge with development. "Bull has over 40 people doing Ridge-related research and development," Lunetta says. "Already they have contributed some of the I/O controllers for our system. And they're doing a new disk controller that we'll incorporate." *–Jonah McLeod*

WHY SUN DESIGNED ITS OWN RISC CHIP

SPEED

Why did Sun Microsystems Inc. adopt a proprietary reduced-instruction-set microprocessor for its new high-end machines instead of sticking with the 68020 that fueled its rise to the top of the work-station market? The answer is simple, according to Sun. The work-station superstar believes that complex-instruction-set processors such as the 68000 family can't keep up with the fast-rising demands for more performance in work stations.

Executives at the Mountain View, Calif., company privately came to that conclusion about four years ago. They saw a need for a midrange work station family in the $20,000 to $100,000 class that would offer speeds of 8 mips in 1987, 16 mips by 1988, 32 mips by 1989, and 64 mips by 1990. For that rate of change, CISC microprocessors just couldn't be upgraded quickly enough, they concluded. A number of RISC microprocessors are now available from several vendors, but Sun designers feel these chips are too slow, as well as too limited in their ability to handle artificial intelligence, which they expect will be added to a wide variety of work station tasks. So the company ended up developing its own RISC chip for the new Sun 4/260 10-million-instruction-per-second work station.

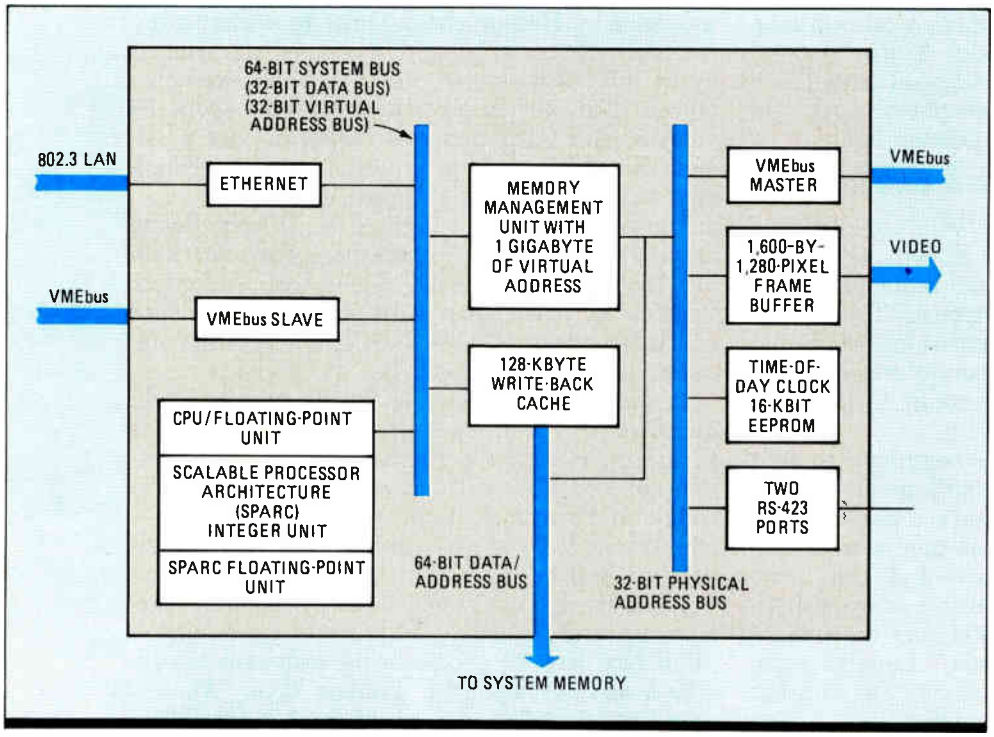
"The new work station does not replace our 68000-based family, which we will continue to develop. It extends the high end," says Wayne Rosing, Sun's vice president of high-end engineering. And users wishing to upgrade to the 4/260 won't have to give up their old software, for the new system is software-compatible with existing Sun products.

The central design concept for Sun's new RISC chip is its scalable processor architecture (Sparc), designed to be easily scaled down. "A CISC architecture does not scale as well as a RISC architecture does," Rosing maintains.

The current Sparc chip, which delivers 10-mips performance, is an off-the-shelf CMOS gate array from Fujitsu Microelectronics Inc. of Santa Clara, Calif. Fujitsu also will be selling the Sparc chip to other vendors. Next year, the architecture will be implemented as a full-custom design in 0.8-μm dual-layer-metal CMOS from Cypress Semiconductor Corp. of San Jose, Calif. This version will offer 20-mips performance. A third Sparc version will be a full-custom ECL chip from Bipolar Integrated Technology of Beaverton, Ore. When this becomes available in 1989, it will afford performance in excess of 40 mips—in fact, BIT claims the chip will offer 50 mips. Sun expects the succeeding generation of ECL to produce a Sparc chip capable of 64-mips performance.

In addition to the Sparc CPU, the 4/260 system (see figure) boasts a floating point unit that can hit 1 million floating-point instructions/s. Another performance enhancement is the 128-Kbyte write-back cache. This allows a CPU to write into, as well as extract data and instructions, at the high access speed of the cache instead of that of much slower dynamic RAM.

Sun began looking for an alternative to CISC processors as early as 1983, when it became apparent that Motorola would need two or three years to upgrade the 68000 family from 1 mips to 4 mips. "We drew a technology



FULL HOUSE. Sun's 4/260 uses a RISC chip for an integer CPU and boasts a floating-point unit, a 128-Kbyte write-back cache, a 1-gigabyte memory management unit, and other enhancements.

trend line and saw that, realistically, by 1990 the 68000 family of chips would be running at 10 to 12 mips—not fast enough for many work-station applications," explains Rosing.

As an example of the sluggish pace of CISC upgrades, Rosing points to the five-year effort required to design a VLSI version of VAX—the MicroVAX II—which was originally implemented in discrete TTL. Upgrading becomes time-consuming when dealing with an architecture as complex as that of VAX, which has over 300 instructions with a large number of instruction formats, he explains. "That translates into lots of complex control logic and microcode. You need two to six times as much logic to perform a function with a CISC architecture as you do you to perform the same function in RISC."

Besides avoiding the pitfalls inherent in CISC, the Sun chip has two main advantages over the prime commercially available RISC chip, the Clipper from Fairchild Semiconductor Inc. in Palo Alto, Calif. The first advantage is speed. The Clipper runs at only 5 mips—half the speed of the Sun chip. Rosing believes that this moderate increase in processor speed would not be enough to lure most technical users away from 4-mips 68020-based work stations that can run all the industry-standard 68000 software not available to a Clipper-based system.

ROSING: 68000s will be too slow for many work-station applications.

A second advantage the Sun chip has over other RISC-based microprocessors is that it can better implement standard high-level languages (particularly C and Fortran) and the AI languages Smalltalk and Lisp. "We feel that AI is an up-and-coming technology we need to address with high-performance computing," Rosing says.

To implement Lisp and Smalltalk on its Sparc chip, Sun is using design techniques that emerged from a University of California at Berkeley research project called SOAR (Smalltalk on a RISC). These techniques allow Lisp and Smalltalk programs to run significantly faster on a RISC processor, Rosing says. □

For more information, circle 481 on the reader service card.

TECHNOLOGY TO WATCH

METHVIN'S CISC BLOWOUT: A 64-BIT-WORD SUPERMINI!

With everyone's eyes focused on reduced-instruction-set computers, it's refreshing to find a machine with an architectural counterview. And the BAT 6420, carved out by two-year-old Davin Computer Corp. in Irvine, Calif., is just that: a general-purpose, 64-bit superminicomputer design that relies on complexity to answer the never-ending cry for more performance.

The $15,000 machine, which will be ready to go on sale to original-equipment manufacturers later this year, may be the first 64-bit computer that isn't a mainframe. It boasts 2 Mbytes of memory, runs under the Unix operating system, and comes down squarely in the camp of CISC, or complex instruction-set computers. "The Davin architecture is about as philosophically far from RISC as one can get," says the company's founder, David Methvin, a minicomputer veteran whose Computer Automation Inc. brought him success a decade ago.

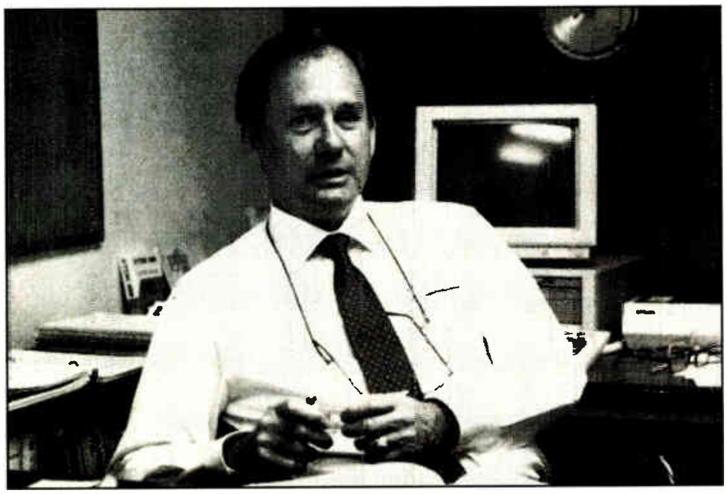
"RISC flies in the face of what we've been doing for 40 years in the computer business," he says—namely, moving toward more and more complex instructions. In Methvin's view, the RISC crowd has gone down the wrong track by "working under a false premise: that faster execution speeds are attained through simplifying the operation of the central processor, and that this, in turn, permits shrunk-down instructions."

RISC gains much of its speed in dedicated tasks by fetching instructions contained in a cache memory built with 20-to-30-ns static random-access memories. But it cannot match conventional machines in a general-purpose environment, because its programs are many times larger and many instructions must be executed to do such fundamental tasks as a single procedure call, Methvin says.

Proponents of RISC admit their architecture lags the ideal for input/output and communications-heavy uses. But Methvin is more emphatic. "For task switching, with lots of I/O going on, it just dies," he says flatly.

In designing the 6420, which is to be the first in a family of 64-bit machines, Methvin compiled mountains of comparative data on RISC vs. CISC. For example, one study shows the BAT 6420 taking 1.75 to 2.25 μs for interrupt context switching, compared with 9 to 18 μs for a RISC machine. In another test running comparable programs, the 6420 required 20,000 bytes of program and a RISC computer 170,000 bytes. In practical terms, this means the BAT approach needs only 2,500 memory operations, while the RISC requires 42,500.

The Davin machine boasts 317 basic instruc-



DAVID METHVIN: "The Davin architecture is about as philosophically far from RISC as one can get."

tions, with four data sizes and six data types; RISC machines generally stay below 100 instructions, and data size is limited. Most of these 317 instructions occupy three bytes or less, with a few going to 11 bytes. The advantage of such a scheme is that programs can be shorter than those written with repetitive RISC statements.

With its 64-bit word width and the register-intensive organization of its central processing unit, the 6420 breaks other new architectural ground. The wide word width attacks the instruction-fetch overhead problem that consumes a major part of run time in most other comput-

Davin, his new firm, breaks new ground with a register-intensive design as well as a 64-bit word, cutting instruction-fetch overhead that eats up so much run-time on other computers

ers, with their narrower word width, Methvin says. The new supermini can fetch up to four or more instructions in one memory cycle, compared with just one in most other machines, so this cuts the number of fetches-per-instruction that must be executed to perform a task. Besides these improvements in word width, an instruction pipeline and three cache memories boost throughput and further facilitate fetching.

One of the most significant features of the 6420 is Methvin's multiple register stacks, which drastically cut the time required to execute procedure calls, or jumps, to and from subroutines. Instead of the conventional single-register stack, the BAT's CPU has four 256-register stacks. These, says Methvin, are "organized in overlapped 'windows' of 32 registers each," with each stack containing 15 windows.

These overlapped, or "sliding," windows are crucial to reducing the overhead of procedure calls. In other computers, each call and return must be saved in main memory and then restored in the register. Each save and restore requires a memory reference, which eats up computing time. The Davin computer eliminates this burden, says Methvin, by saving procedure calls in a four-register window section, which he calls a "shadow stack." The window slides down 16 registers to overlap the two parts of the procedure (calling and called). This process requires only three CPU cycles, while standard memory saves can take up to 20 instructions and as many as 400 CPU cycles, Methvin says.

The concept of the overlapped register stack first surfaced about 1980, in research done at the University of California at Berkeley by a pioneering RISC group. "That's the only good thing to come out of that bunch," Methvin says.

"By most of the economic and technological standards of judging the fundamentals of significant ideas, RISC doesn't make any sense," says Methvin, who admits that his strongly negative stance has carried little weight in the industry. "I've been shouting into the wind for years."

He concedes that a small instruction set can zip through simple instructions, a quality that makes RISC a good bet for specific, computationally intensive jobs, such as serving as the graphics engine in work stations. But any speed advantage gained in dedicated tasks does not apply to general-purpose computing, where a number of heavyweight RISC backers—most notably, Hewlett-Packard Co.—are trying to make a mark.

As Methvin explains it, most commercial and industrial applications are dominated by byte-oriented data; handling this data along with the communications among large numbers of terminals, lines, or high-speed disks consumes most of the computing time. And it requires "a super-fast, expensive memory—not to mention expensive I/O subsystems," says Methvin.

In software, too, he says, the costs of RISC are high: "To get the benefits of RISC, an optimizing compiler is an absolute requirement. It is the only way to grab hold of the features and control their operation. The reason is that RISC architecture has eliminated the engine for interpreting machine microcode, so even the simplest instructions have to be placed into both hard-wired processor logic and the compiler. This is an enormously complex and sophisticated job." With a conventional computer, by contrast, a simple assembler or microcode engine can do the trick.

Then, too, Methvin argues, the compilers generally have to be written by the RISC machine manufacturer, the only source for the detailed information required to create the compiler microcode. This all but eliminates the possibility for third-party houses to offer their own versions, and in Methvin's view it results in higher costs for users. *–Larry Waller*

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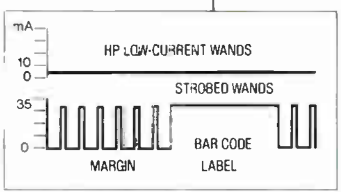

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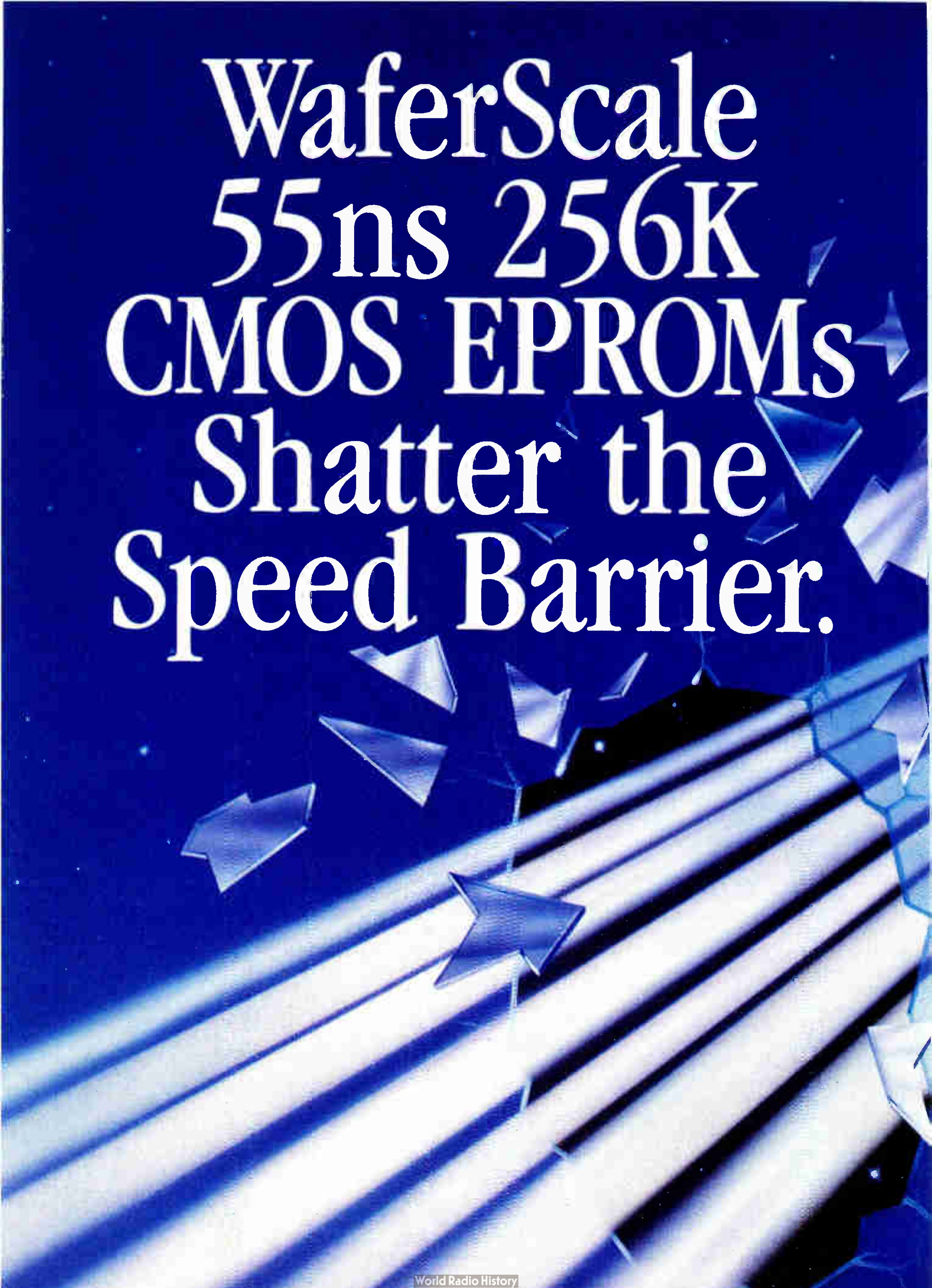
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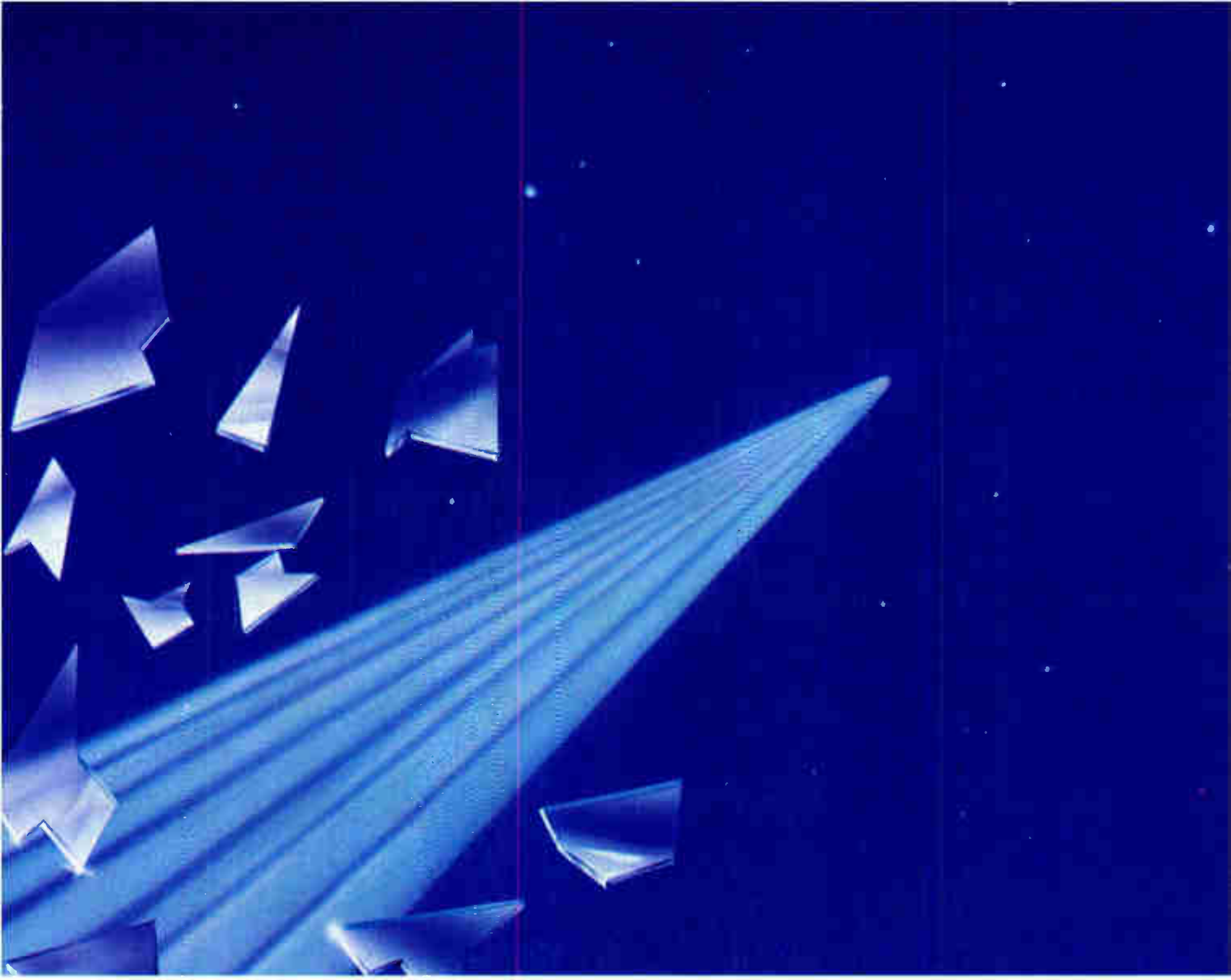

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WS57C49	55 ns	70 ns	8K x 8 CMOS EPROM
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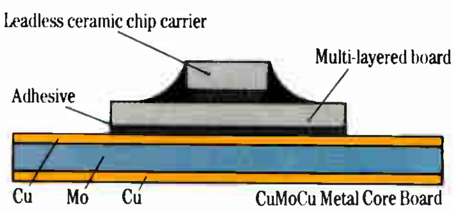
Copper-Clad Invar

High density surface mounting of leadless ceramic chip carriers has created new thermal and mechanical problems for those working on high reliability electronic projects.

More and more companies are addressing these problems by incorporating metal cores as thermal mounting platforms in their printed circuit board assemblies. The choice of metal laminate comes down to two: Copper-Clad Molybdenum or Copper-Clad Invar. Both do an equally good job of solving the problem of the coefficient of thermal expansion (CTE) mismatch between chip carrier and substrate. But, that's where the similarity ends.



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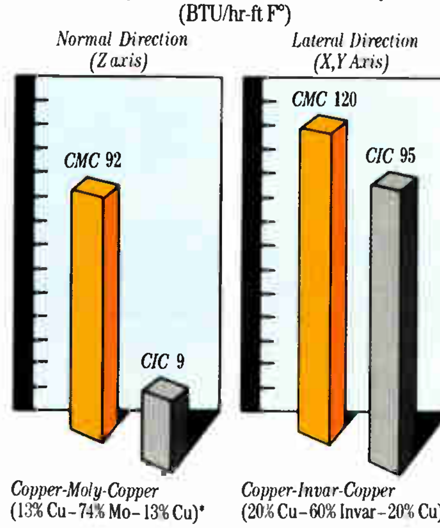
Comparison of Thermal Conductivity (BTU/hr-ft F°)



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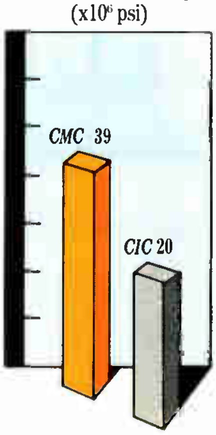
Comparison of Modulus of Elasticity ($x10^6$ psi)



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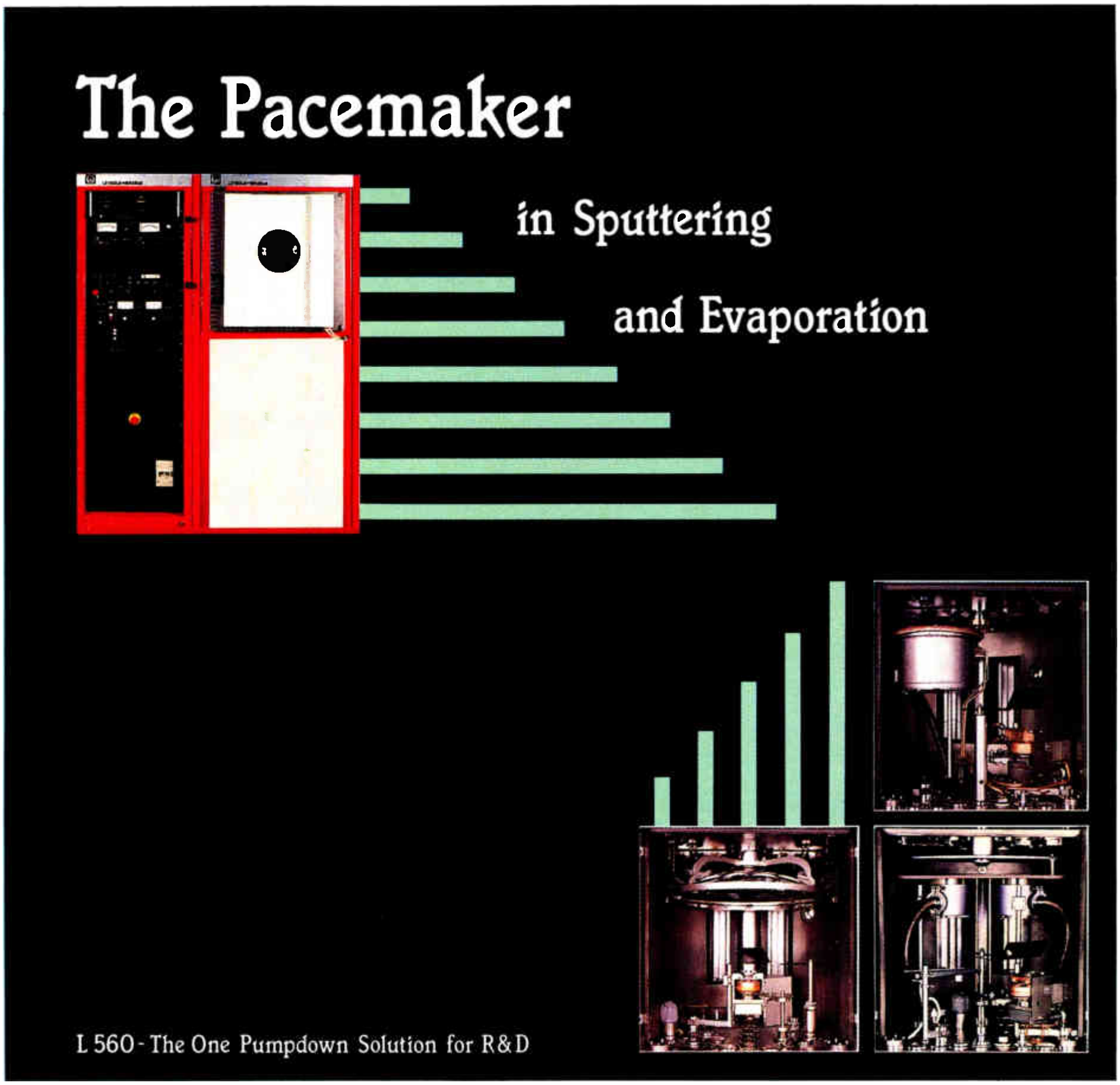

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HP FINDS A WAY TO PROBE DEEP INTO OPTICAL LINES

A major problem for communications engineers should evaporate now that Hewlett-Packard Co. is bringing data correlation to optical time-domain reflectometers. Engineers will be able to look miles deeper into a glass fiber to spot a fault, as well as to make measurements faster than with any conventional instrument.

The HP 8145A (see fig. 1) is the answer to a knotty problem: as repeater distance gets longer because of more powerful lasers, lower-loss fibers, and more sensitive receivers, it is becoming increasingly difficult to characterize performance or find faults in optical transmission cables. The 8145 addresses this problem by increasing the distance over which reflectometers operate by up to 56%, depending on the wavelength and fiber type. It marks the Palo Alto, Calif., company's entry into this business.

Short measuring time is as important as distance. A typical transcontinental cable carries up to 30,000 phone channels on a single fiber. So a fault in the line can be costly, with losses of revenue to the operating company amounting to as much as $100,000 an hour. With its better than hundred-fold improvement in measuring time, the 8145 will help cut such losses considerably, the company says.

Although maintenance on fiber links will account for up to 70% of the instrument's applications, the 8145 will find many other uses, says Peter Aue, research and development section manager at HP's Instruments Division in Böblingen, West Germany. Examples are localizing discontinuities, such as air bubbles and cracks in fibers during manufacture, and verifying performance during installation. Still other applications involve quality control at cable makers and incoming inspection at operating companies. In the research sector, the 8145 can check out splices and connectors in test links and determine dynamic range.

The data-correlation technique was worked out at HP Laboratories in Palo Alto. The 8145 that implements it was developed in Böblingen.

Like other optical time-domain reflectometers, the 8145 uses signal-reflection principles similar to those employed in radar to find out the distance to an object. It sends bursts of laser light into a fiber, determines parameters such as signal loss, and calculates the distance to a faulty splice, break, or other discontinuity in the line.

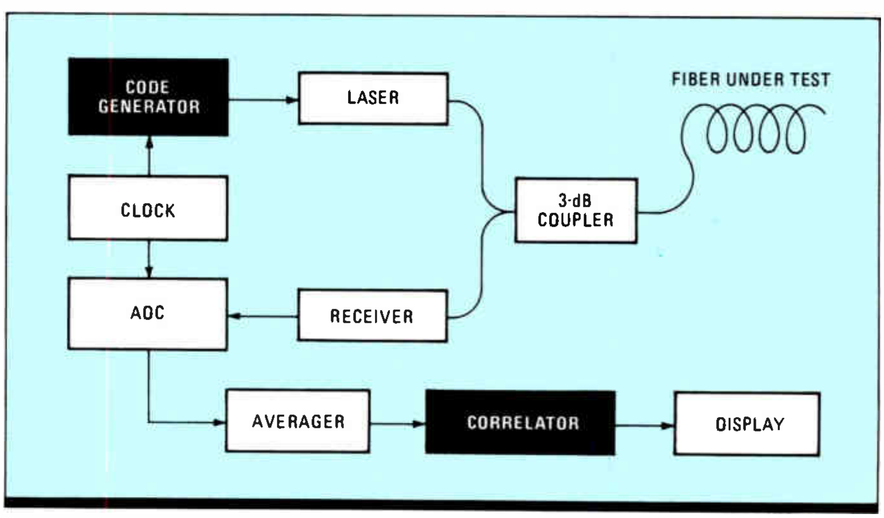
The new instrument's dynamic range is 28 dB for 1,300-nm single-mode fiber and 26 dB for 1,540-nm fiber. Present reflectometers have dynamic ranges between 18 and 22 dB for 1,300-nm single-mode fiber and between 16 and 20 dB for 1,540-nm fiber, says Franz Sischka, the head of the 8145 hardware design team in Böblingen. Consequently, the HP instrument probes much deeper into a line: 70 to 130 km (43 to 81 miles), depending on wavelength and fiber type, compared with between 45 and 100 km (28 to 62 miles) for present units. This range is large enough for even the longest repeater distances in today's networks, and it "leaves much headroom for future networks, too," Sischka says.

Also impressive is the speed with which the 8145 takes measurements. When the designers coupled their reflectometer to a 60-km, 1,300-nm fiber, they had results in 8 seconds. It took competitive instruments hooked to the same fiber 15 minutes to do the job, the company says.

The accuracy with which the 8145 locates faults is better than ±3 meters, with a readout resolution of better than ±0.5 meters. Typical accuracy in today's reflectometers is around ±5 meters. However, accuracy figures are highly variable, depending as they do on the characteristics of the cable being measured.

For all of its benefits and performance characteristics, the 8145 is not "essentially more expensive than competitive units," says Aue. Available now, it is priced at $24,000 to $35,000, depending on whether the user needs to test a 1,300-nm fiber, a 1,540-nm fiber, or both. Most competitive units cost between $27,000 and $31,000.

Responsible for the high measuring speed, long range, and high accuracy "are a new correlation technique and careful design of the analog parts," Sischka explains. In an optical time-domain reflectometer the highest possible back-



1. PENETRATING FIBERS. Correlation lets the HP 8145A OTDR look deep into fiber-optic cables.

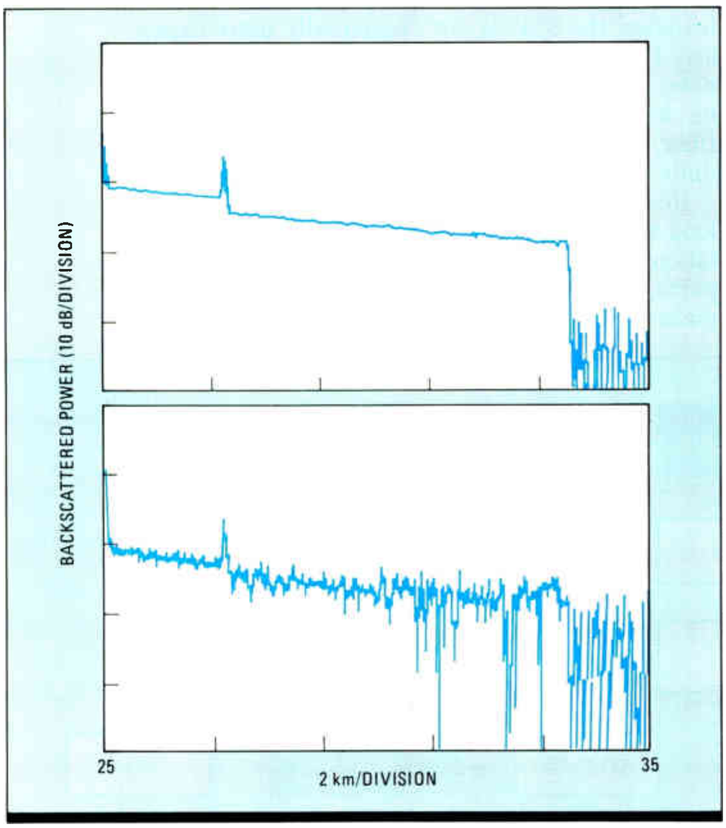
scatter signal level must get to the receiver diode. To meet that goal, the Böblingen team used high-power semiconductor lasers and driver circuits with extremely low noise in the 8145.

However, peak laser power and pulse width, which together determine the energy in the fiber, impose limits beyond which the laser output cannot be raised. Peak power is limited because any increase beyond the level specified by the laser manufacturer rapidly decreases laser lifetime. And pulse width is limited because as it is made longer, the resolution drops.

To overcome these limitations, HP went to its new correlation technique for the 8145. Where conventional units use a single-pulse architecture in which one pulse is launched and the return signal sampled in each cycle, the 8145 sends out pulse trains coded with a proprietary variable code.

The correlation technique concentrates the information distributed in a train of coded pulses into a single pulse, one with an amplitude up to 500 times higher than that of other reflectometer lasers. This, in effect, means the fiber is probed with 500 times more light than conventional reflectometers put out. That, in turn, translates into increases in both dynamic range and measuring speed.

The sampled return signal is correlated in a fast custom-built 32-bit signal processor in real time. To make correlation work in a reflectometer, the signal-processing hardware must be linear to within 0.1% over as large a dynamic range as possible—and that includes such inherently nonlinear devices as semiconductor lasers. HP achieved this linearity by design-centering techniques that hold down the receiver's sensitivity to device tolerances and to distortions caused by the signal-processing circuitry, while optimizing signal sensitivity. The laser diode is made part of a feedback loop to prevent degradation effects. These design measures are another reason for the 8145's large dynamic range.



2. SPEEDIER RESULTS. The HP 8145A (top) measures up to 100 times faster and exhibits less noise than do other OTDRs (bottom).

LOWERING NOISE

Getting high linearity was not the only challenge facing the HP designers. Fast recovery from saturation caused by Fresnel reflections and extremely low noise were other goals. Clamping techniques achieve the fast recovery and to reduce noise, the designers went to boxcar averaging in which the line is repetitively sampled and the results added. That increases the usable signals by the number of samples. The noise, however, increases only by the square root of the number of samples. With averaging, the receiver's noise level is –105 dB at a 3-MHz bandwidth (see fig. 2).

But boxcar averaging takes time. In single-pulse reflectometers, it generally takes 1 second to achieve a 10-dB improvement in one-way dynamic range; after 100 seconds, the improvement is 15 dB; and it would take a prohibitive 10,000 seconds, or more than 160 minutes, to get a 20-dB improvement. In the 8145, however, the averaging, and hence the measuring, time is drastically reduced by using codes. That means that for a given dynamic range the averaging time is cut by the same factor by which the laser power is increased. Expressed differently, coding leads to a higher dynamic range for a given averaging time.

Probing with variable code lengths, good correlation techniques, and well-designed analog hardware are essential for a high-performance reflectometer. But also needed is sophisticated software to select the proper codes for a fiber under test, to suppress nonlinearities, and to combine the results of partial measurements into a final result with an error of less than 0.01 dB. The Böblingen Instruments Software Group wrote this software for the 8145.

The software experts also came up with soft keys to avoid a large number of hardwired keys, yet retain flexibility. The 8145 is the first reflectometer on the market to employ such a user-friendly man-machine interface, Sischka says. User-specific soft keys, defined by customer, make it possible even for the unskilled in the field to handle the instrument. What's more, the software group incorporated new features into the 8145—a recall and compare mode, easy access to an extra mass memory module, store and recall of instrument settings, and user-selectable display modes. *–John Gosch*

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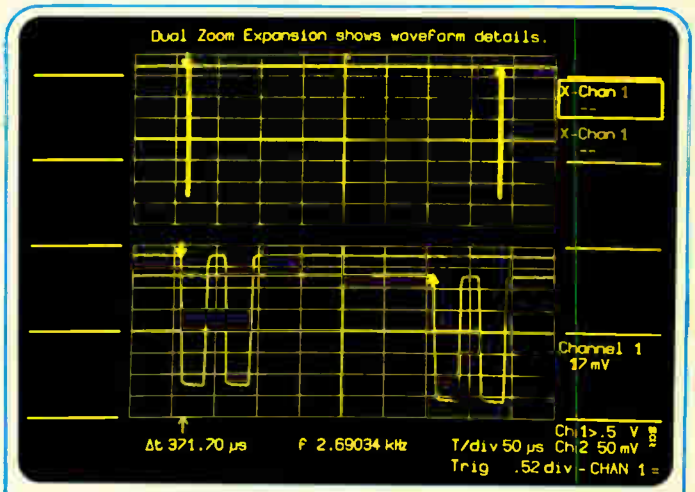

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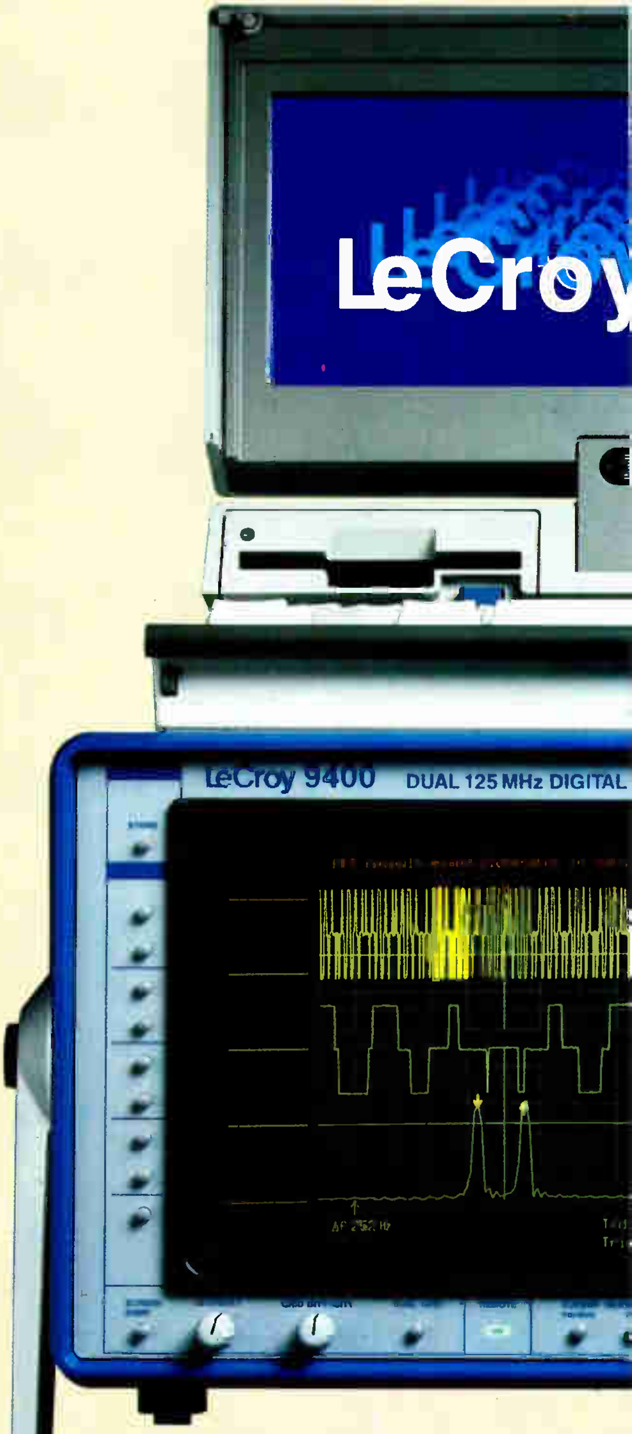

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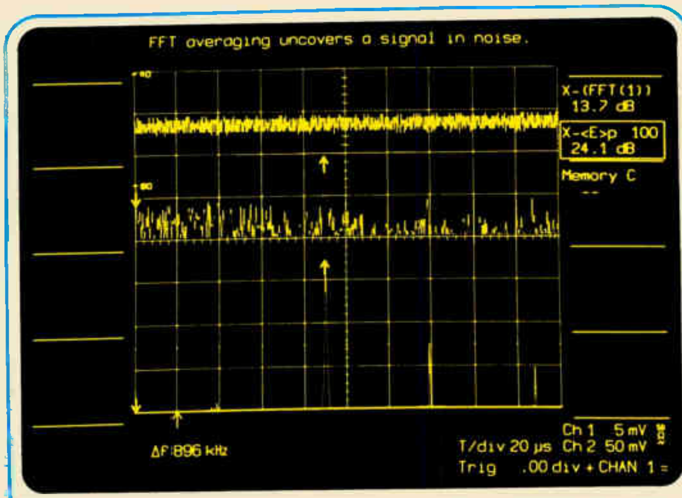

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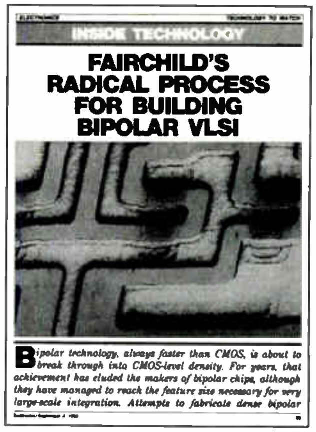
UPDATE: ASPECT IS ON SCHEDULE AT FAIRCHILD

Fairchild Semiconductor Corp.'s Aspect emitter-coupled-logic technology is moving to production on schedule, says Thomas Miller, director of strategic marketing for custom circuits. Following introduction of the 2-μm version of the bipolar process a year ago [*Electronics*, Sept. 4, 1986, p. 55], the Cupertino, Calif., company quickly transferred a scaled 1.5-μm version to its production line.

And in March, Fairchild introduced its first commercial product: the Aspect 12k, a 12,269 equivalent-gate ECL array. In the low-power mode, it features a gate-switching current of 150 mA and a gate delay of 200 ps. In the high-power mode, gate delay drops to 120 ps with a switching current of 300 mA.

The second 1.5-μm Aspect product is a 16-by-16-bit multiplier introduced in June [*Electronics*, June 25, 1987, p. 74]. With a standard-cell methodology built around the Aspect process, the 240-by-260-mil multiplier has a guaranteed fall-through time of 4 ns and a power dissipation of only 6.5 W. The company is offering samples to interested customers, Miller says.

Aspect is also being used in the fabrication of a family of ECL standard-cell-based data-path elements with densities of up to 20,000 gates. In the works are a series of multipliers, a 32-bit arithmetic logic unit, a 32-bit barrel shifter, and a three-port register file. Designed for use in minicomputers and superminis, the supercells should enter Fairchild's cell library in early 1988. They may be fabricated as standard parts as well, says Miller.



Also, he says, Fairchild is working with several companies on designs based on the Aspect 12k array. A number of additions to the gate-array family, including a variety of lower-density versions with TTL interface, are under development and expected to move into production by the end of the year.

Other products being planned in the Aspect bipolar process include a variety of analog circuits, including a 400-MHz digital-to-analog converter, a video shift register for graphics applications, and fusible-link bipolar programmable logic devices. *–Bernard C. Cole*

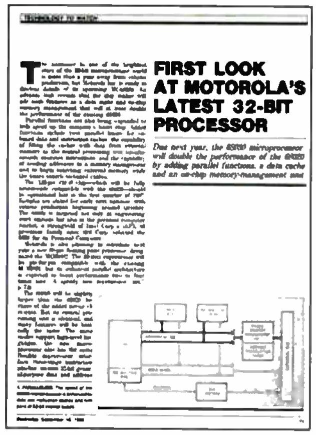
UPDATE: MOTOROLA'S 68030 GOES TO MARKET

In the year since Motorola Inc. first disclosed details about its new 32-bit microprocessor, announcements about the competing Intel Corp. chip seem to have pushed the Motorola 68030 into the shadows.

But executives at the Motorola Microprocessor Products Group in Austin, Texas, are decidedly upbeat as they prepare to market the 68030 microprocessor on time [*Electronics*, Sept. 18, 1986, p. 71]. Their aim is to meet archrival Intel head-on in the competitive personal-computer arena, where Intel's 80386 is making waves as the microprocessor of choice in IBM Corp.'s Personal System/2 and is eagerly sought after by the inevitable host of clone makers. Moreover, they have two significant design wins to report.

Production of this "superchip," as Motorola calls it, is on schedule: it will be available this month in sample quantities and volume production will start in the fourth quarter, says Jeff Nutt, technical marketing manager for the 68000 family. Over the summer, the company exercised prototypes in preparation for initial shipments of 16.7- and 20-MHz parts. Nutt says minor adjustments have been made to the 1.2-μm CMOS process to improve yields in the higher-speed range.

The Motorola team took competitive delight in the glitches that hampered Intel's 80386 early on. They also believe the personal-computer market may have been thrown into a state of confusion by the lack of software for the new IBM machines. So now is a good time for their own vigorous countercharge in marketing the 68030, they say. It executes software twice as fast as the three-year-old, 32-bit 68020 and is compatible with the nine years' worth of programs written for the entire 68000 family.



"We see a place in two markets," says Nutt, citing Motorola's traditional strength in work stations and the larger but more elusive business-PC area. Importantly, both Apple Computer Inc. and NCR Corp., which have been using the 68020, have now committed to the 68030, he says.

The chip's cost will be disclosed soon. Motorola says pricing will resemble the 68020's pattern: that chip debuted at $187 and now sells at $135 in 100-piece quantities. *–J. Robert Lineback*

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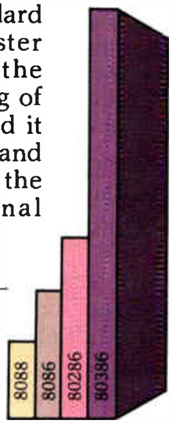

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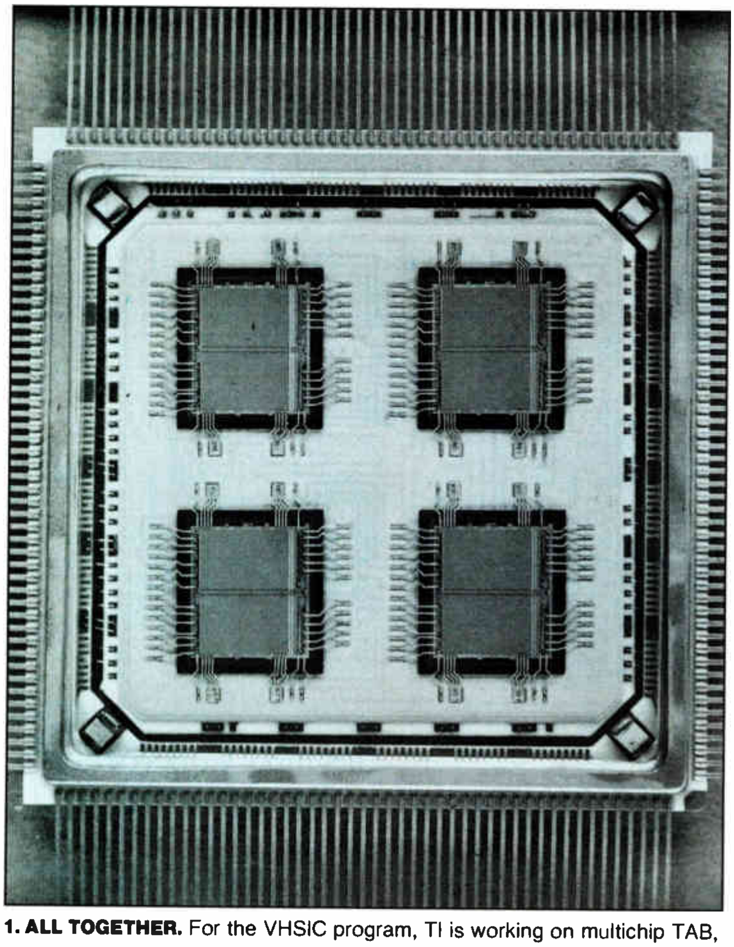
WHAT'S NEW IN PACKAGING?

TAPE-AUTOMATED BONDING PUSHES IN NEW DIRECTIONS

Support grows for setting standards and a new generation of technology begins to emerge—evidence that TAB is no longer the orphan of the packaging world

by Marce Eleccion



1. ALL TOGETHER. For the VHSIC program, TI is working on multichip TAB, such as this module that holds four 100-MHz 32-Kbit-by-9-bit static RAMs.

Tape-automated bonding is picking up speed in its drive to make a mark in IC packaging technology in the 1990s. Among the signs of TAB's new strength are a standards-setting campaign and second-generation technology—notably multichip and area TAB.

TAB proponents recognize that the technology must leap the barrier of nonuniformity, so a recently formed group is working out standards. Engineers are pushing beyond superchip packaging to develop multichip TAB, modules that pack several densely leaded chips into a small area. They are also beginning to develop procedures for area TAB chips with interconnect pads in their interiors as well as along their peripheries.

Interest in TAB started picking up when engineers realized it would be a good package for high-speed, very large-scale integrated circuits with hundreds of external leads. It offers a highly productive, low-cost, and reliable alternative to wire-bonding integrated circuits to lead frames and ceramic substrates. It is based on polyimide reeled tape ranging in width from 35 to 105 mm and with etched copper conduction paths. ICs are bonded onto the tape and then packaged: both processes are highly automated.

Although it was pioneered by the General Electric Co. in 1972, TAB was an orphan technology in the U.S. for many years. It did find a home in Japan [*Electronics*, Nov. 11, 1985, p. 26], where electronics manufacturers saw its potential for providing relatively small, multileaded packages with interconnects that can be handled by automated bonding procedures. And now TAB is finding its place in U.S. electronics.

TAB still has a minuscule share of the market, but by 1990, it could garner anywhere from 5% to 20% of the total chip interconnection market, says Bob Applewhite, manager of 3M Co.'s Microinterconnect Systems Division in St. Paul, Minn.

To give TAB a push in the marketplace, a group of eight companies is supporting a Jedec standard proposal. It addresses such issues as the maximum number of outer leads (from 60 to 804) for a given package size, their pitch (10, 15, and 20 mils), test pad location and size, and dimensions of the sprocket holes (to assure accurate positioning in test sockets and handlers). All dimensions and tolerances allow the use of two- or three-layer tape, as well as any future multilayer tape configurations. The eight companies are Amp, Apple Computer, Boeing Electronics, Ford Aerospace, IBM, Indy Electronics, Mesa Technology, and Rockwell International.

With its multilead capability, TAB is a natural for modules like the ones Texas Instruments Inc. is working on for the U. S. Army Electronics Technology and Devices Laboratory, Ft. Monmouth, N. J. The Dallas company has already produced two surface-mount modules designed to hold TAB-connected VHSIC chips running at up to 100-MHz frequencies. The chips are mounted directly to a multilayer cofired ceramic substrate, with each module having electrical characteristics matching those of the VHSIC chips (see fig. 1). The modules use chips developed by TI, with ceramic packaging from Interamics, San Diego, Calif., and TAB equipment and tape from TAB pioneer International Micro Industries, Cherry Hill, N. J [*Electronics*, Feb. 17, 1986, p. 38].

In the commercial market, Du Pont Electronics' Connector Systems Division in New Cumberland, Pa., offers a multichip memory module (see fig. 2) for floppy-disk backup and other applications. The credit-card-size module [*Electronics*, Dec. 18, 1986, p. 142] contains 16 memory chips and measures 1/8 in. thick; two smaller sizes are available. Made by NEC Corp. using IMI equipment and processing technology, they are available in three random-access and read-only versions ranging from 32 Kbits to 1 Mbit.

MULTICHIP CONNECTIONS

One development that's helping speed the spread of multichip TAB is IMI's Multitab, which permits the connection of many chips in the same plane or substrate. Multitab uses two single-level tapes in a cantilevered configuration that eliminates the need for a polyimide support ring while allowing each chip to be tested prior to commitment to a final package. The system is presently being used by an IMI subsidiary, Smart Card Systems Inc., to fabricate two military access systems, and it may be used to make the next generation of Du Pont memory cassettes.

As lead counts begin to increase, it is inevitable that I/O pads in the center of the die will supplement those on the periphery. And TAB technologists are already devising a scheme to accommodate this move. Called area TAB, the process uses tape containing multilevel conducting planes of copper (see fig. 3).

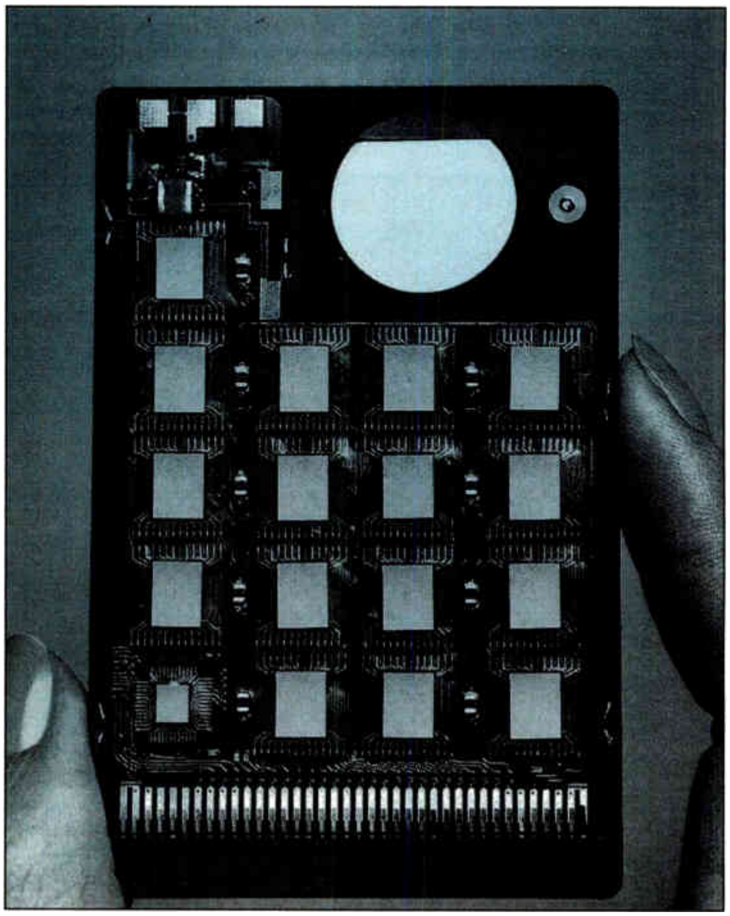
Area TAB may cause problems in the way processing is carried out, however. Since the upper level of TAB leads must be brought down to the plane of the die surface, methods must be devised to open up a path through the lower level of leads without causing shorting and to apply the bonding tool through the path. This almost eliminates the use of gang bonders, which are more suited to single-level planar bonding.

Area bonding also may cause the polyimide film that supports the leads to delaminate due to overheating and expansion. One way of solving this problem is to employ single-point bonders that attach one lead at a time, a method that Hughes Aircraft Co., Carlsbad, Calif., uses in its dual TAB and wire bonder. Hughes also employs single-frame TAB carriers instead of reel-to-reel film sprocket drives.

Hughes is betting that its system is ideal for large-area ICs, says Gary Smith, Hughes TAB marketing manager. But IMI's Holt believes that area TAB will not take off until a reliable way of forming fast, consistent interconnections is developed—and that could take until the end of the decade, he says. A way must also be found to prevent the tape film from outgassing when heated, says Holt, since both moisture and process chemicals can contaminate the chip environment. Another problem with area bonding is the inaccessibility of inner die bonds for inspection, and that makes it unacceptable for most military standards, says 3M's Applewhite.

Most of the larger IC makers and users are jumping on the TAB bandwagon. For example, TI is TAB-bonding a 394-mil^2 chip with 224 leads into ceramic chip carriers for its MegaChip Lisp processor. To handle such big chips, IMI is developing TAB with several levels of interconnections for ICs almost 3 in. on a side and with over 2,000 leads.

Another development that's generating a lot



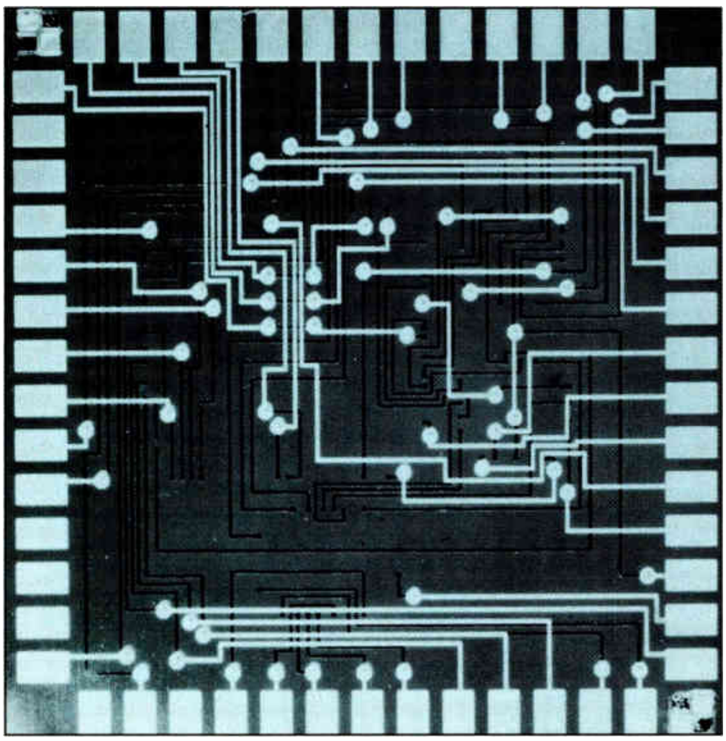
2. MEMORY PACK. Du Pont is offering three multichip TAB modules to hold RAMs or ROMs; this credit-card-size module holds 16 memory ICs.

of interest is the TapePak process for leaded TAB plastic chip carriers from National Semiconductor Corp., Santa Clara, Calif. TapePak uses a single-layer tape with no polyimide and with double-thickness pure copper for better thermal performance. Also, it provides on the tape the "bumps"—built-up input/output pads needed for bonding. That means the bumps needn't be added to the chip—and that requirement for special processing of the ICs has been a major roadblock to the spread of TAB.

Two recent TapePak converts are Motorola Inc.'s Semiconductor Products Group, Phoenix, Ariz.—second largest IC producer in the U. S.—and the Delco Products Division of General Motors Corp., Kokomo, Ind. [*Electronics,* April 16, 1987, p. 24]. Motorola will turn out VLSI packages with 20-mil centers; Delco won't say what it's using TapePak for. National itself has implemented an assembly line called Odyssey that incorporates both TapePak and wire bonding to produce an array of device styles in a variety of packages [*Electronics,* Aug. 21, 1986, p. 74].

Next to go commercial could be area TAB with multilevel conductors to accommodate interconnection pads in the chip interior as well as around the periphery

And IBM Corp. is getting into the act. Although it is using a flip-chip solder-mount technology called the C4 process in its new Personal System/2, industry sources say the computer giant has begun to develop its own TAB technology. However, Intel Corp. will stick with C4, says Jeff Katz, director of marketing. Intel has an IBM license for the technology, which divides die tabs into three to four rows on the periphery of the chip to obtain closer pitch spacing.



3. MULTILEVEL TAB. Area array TAB on this 3M setup uses tape with multiple connection levels to provide a path to inner I/O pads on a chip.

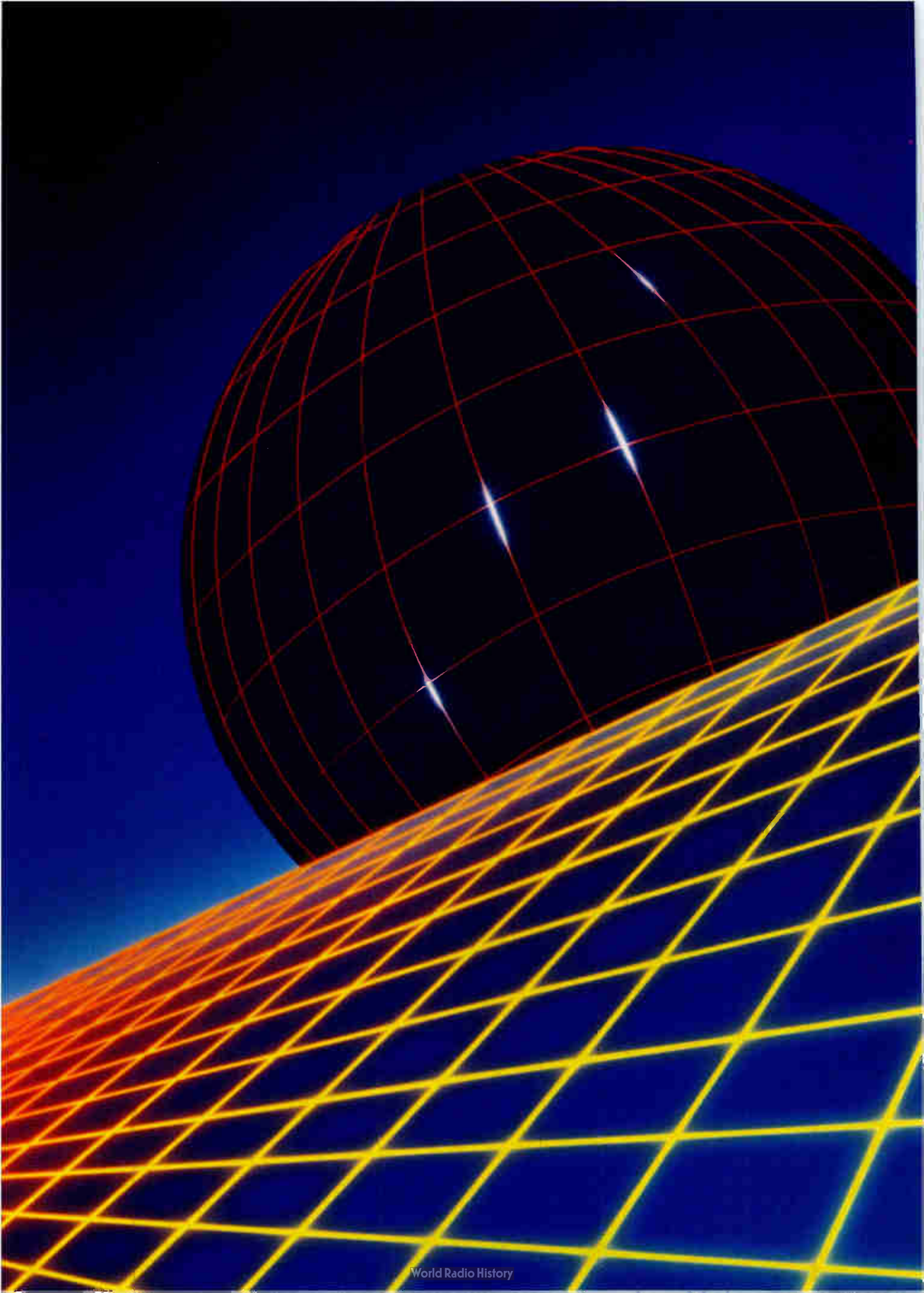
It doesn't take a super-salesman to tout the advantages of TAB technology. As line densities rise to meet the demands of higher-speed circuits, the surface area of VLSI circuits gets smaller. The mechanical restrictions of wire bonding, however, require that each die pad be no smaller than about 4 by 4 mils, with no less than 2 mils spacing between pads. With lead counts of some devices now surpassing 300, this means that a chip would have to be almost 500 mils on a side to accommodate wire-bond pads at its edges. Such sizes are beyond the capabilities of most semiconductor processes, which can't go beyond 394 mils on a side.

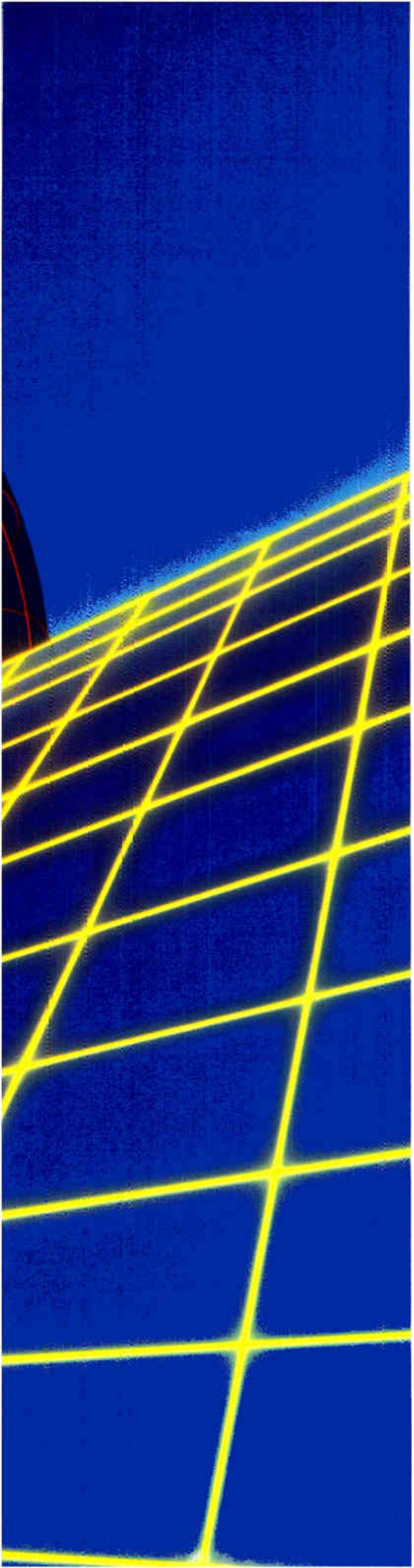
That's where TAB comes to the rescue. It permits bonding pads to be reduced to 2 by 2 mils by doing away with the vertical leads necessary in popular conventional packages. And Fairchild Semiconductor Corp., Palo Alto, Calif., recently reached 1 by 1 mils per pad with 1-mil spacing for an inner lead pitch of 2 mils [*Electronics,* Aug. 20, 1987, p. 32]. With this version of TAB, chip sizes can be reduced by almost 90%, restricted only by the number of components on the die.

And TAB has additional advantages. For one, because bonded inner leads are brought out to wider pitches that are more accessible to probing, circuits on the die can be more easily tested and even burned-in before being packaged. That will save the expense of unknowingly bonding defective chips to a substrate. Since the chip itself does not have to be directly touched by surface probes, there's less likelihood of damage occurring during chip handling.

TAB leads also perform better at high speeds, primarily because of the rectangular paths that they offer. Above about 50 MHz, the round wires associated with chip-and-wire methods begin to introduce large lead inductances, whereas rectangular cross sections do not. Because of the lead shape, TAB also provides improved heat dissipation over wire bonding—Fairchild claims a 60% improvement. The improved heat dissipation and the considerably higher bond strengths of TAB dramatically improve the reliability of the chip. And, since the manufacturer specifies the design configuration of TAB leads, there is more control over interconnection impedance.

One of the primary advantages of TAB is that inner leads can be attached to the die and outer leads attached to the package in a single gang-bonding process. As lead counts increase, wire-bonding of conventional packages becomes extremely labor-intensive, adding to the cost of assembly as well as increasing the chances of device malfunction through faulty connections. □





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HOW TO HIKE PRODUCTIVITY IN MILITARY SOFTWARE

Contractors building U.S. military aerospace systems are fighting a crisis in software productivity, and their tactics may point the way for civilian companies that are facing the same problems. Their solutions are networks of highly sophisticated tools. Two of these contractors, GMHE/Hughes Aircraft Co. and Boeing Corp., are in the forefront in developing complex networked systems that integrate the different packages required for a software-writing job and then manage each of those jobs.

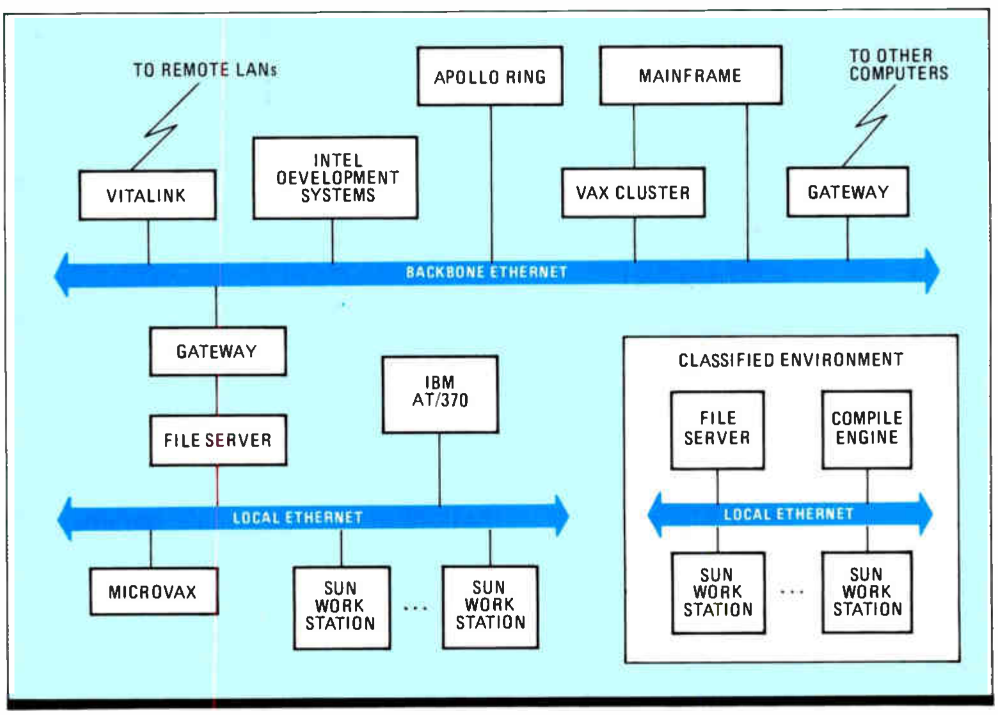
The contractors' problems stem from the mushrooming need to define, write, and maintain military software, which can account for nearly 70% of a system's cost. For example, the Advanced Tactical Fighter, which will be built in the early 1990s, will need 1 million lines of computer code to run its processors, plus 10 million more for ground-support equipment. By comparison, the current workhorse fighter, the F-16, needs only 256,000 lines of computer code for its processors. And productivity isn't keeping pace: one Air Force study concludes that the use of software in military programs is growing 12% a year, but software-writing efficiency is improving only 5% a year.

That's why Hughes and Boeing are pouring time and money into software-development networks. Hughes's Software Engineering Environment, or SE², and the Boeing Automated Software Engineering network, BASE, give individual users at work stations access to an assortment of computers and an extensive array of software tools. These are a mix of commercial packages and tools devised internally for defining and writing application programs.

The significance of the networks lies with "their integration, bringing many tools together," says Kenneth E. Nidiffer. Now a consultant at the Software Productivity Consortium in Reston, Va., Nidiffer is a retired Air Force officer who was a leader in the drive for better management of software engineering when he was at the Air Force Systems Command. "It has not been well recognized that integration [of software development tools] is not only a discipline in itself, but a barrier we are tripping over," he says. That is why the initial success of the Hughes and Boeing approaches has Nidiffer optimistic that these networks could become the "software factories" that help resolve the military crisis.

Hughes and Boeing say their new development networks are already proving their worth. Software productivity is notoriously hard to quantify, but managers at both companies say that comparing the projected costs of software in recent bids on military projects with similar bids in the past is encouraging. "We have reduced [the cost of software in] our bids up to 40%," says Paul A. Mauro, who manages the program in the Software Engineering Division at Hughes's Ground Systems Group in Fullerton, Calif. "SE² has really had positive effects on productivity." Lloyd Osborn, directer of automation and productivity at Boeing Aerospace Co. in Seattle, says much the same about BASE. "Our goal of 100% productivity improvement from 1984 to 1990 is on track and attainable," he says.

Both systems are still expanding. Hughes now operates some 150 work stations (see fig. 1), mostly Sun Microsystem units, connected to a central cluster of 16 Digital Equipment Corp. VAX minicomputers. Boeing won't say how many computers and work stations are involved with BASE (see fig. 2), but will say that it has a dozen projects under way, with each project using



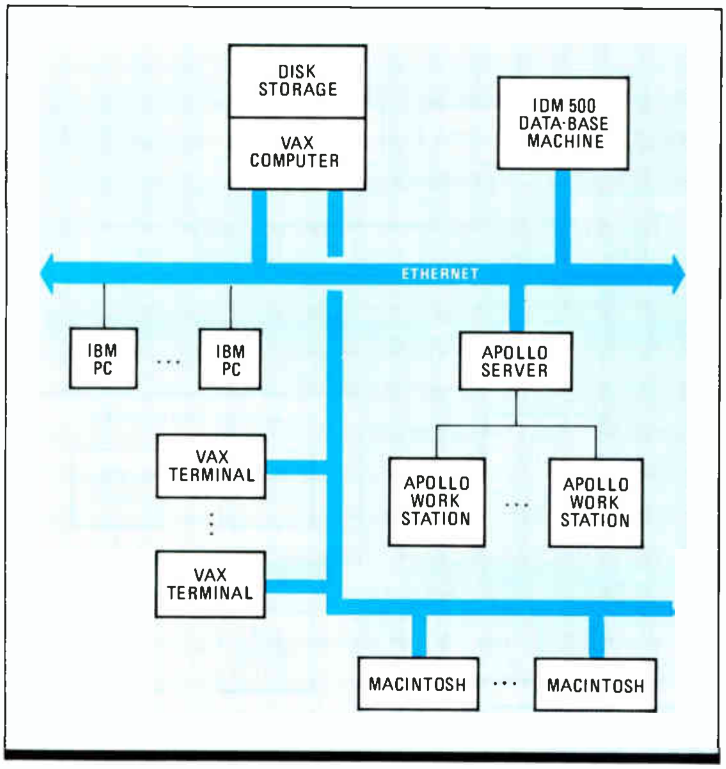
1. EVER GROWING. Hughes's Software Engineering Environment, or SE², now contains 40 software-development products with more being added. It incorporates 150 work stations linked to 16 VAX computers.

about 20 work stations and two VAX 8700s.

Hughes already has employed SE² to develop software for AAS776, an air-defense system for Egypt, as well as for large sonar, communications, and radar-control projects. Boeing's BASE has played a pivotal role in developing software for the Peace Shield air-defense system for Saudi Arabia, the SRAM 2 missile, and for control systems for small intercontinental ballistic missiles.

Furthermore, the networks are being spun off into nonmilitary applications. Hughes is using SE² in its bid for the new Federal Aviation Administration air-traffic-control system, which requires 1.5 million lines of Ada computer code. Boeing's BASE has a role in design of the company's next generation of passenger jets.

Of course, writing military software has an extra dimension of difficulty because the requirements go far beyond defining the system and writing the programs. For one thing, the formats for maintaining and changing the programs have to be provided for life cycles of at least 15 years. Also, Nidiffer says, it has been clear for years that "software-intensive defense systems are beset with a myriad of symptomatic problems" that run the gamut from faulty initial software design to poor performance caused by unskilled operating personnel and lack of system-management expertise. Recognition of these pitfalls paved the way for the integrated software engineering networks. The way to deal with these pitfalls, he says, is by coordinating the definition and production of software, and



2. BROAD BASE. The Boeing Automated Software Engineering Program is being used on a dozen projects, each of which requires about 20 work stations.

"by bringing the good ideas in software engineering, technology, and management techniques directly to bear on the weapons-system acquisition environment."

Both Hughes and Boeing began grappling with the software productivity dilemma a decade ago. By the early 1980s, they had come up with interactive development techniques. Then, starting around 1984, both companies set about putting together sets of standardized software engineering tools embedded in networks that primarily serve users at work stations.

Hughes was an early user of the R1000, a superminicomputer from Rational, Mountain View, Calif., with software optimized for executing Ada code. The system [*Electronics*, July 8, 1985, p. 36] can do incremental compilation, a major timesaver in debugging. It also manages software, decomposing large programs into manageable subsystems and tracking the interfaces between those subsystems.

EXPANDING TOOL KITS

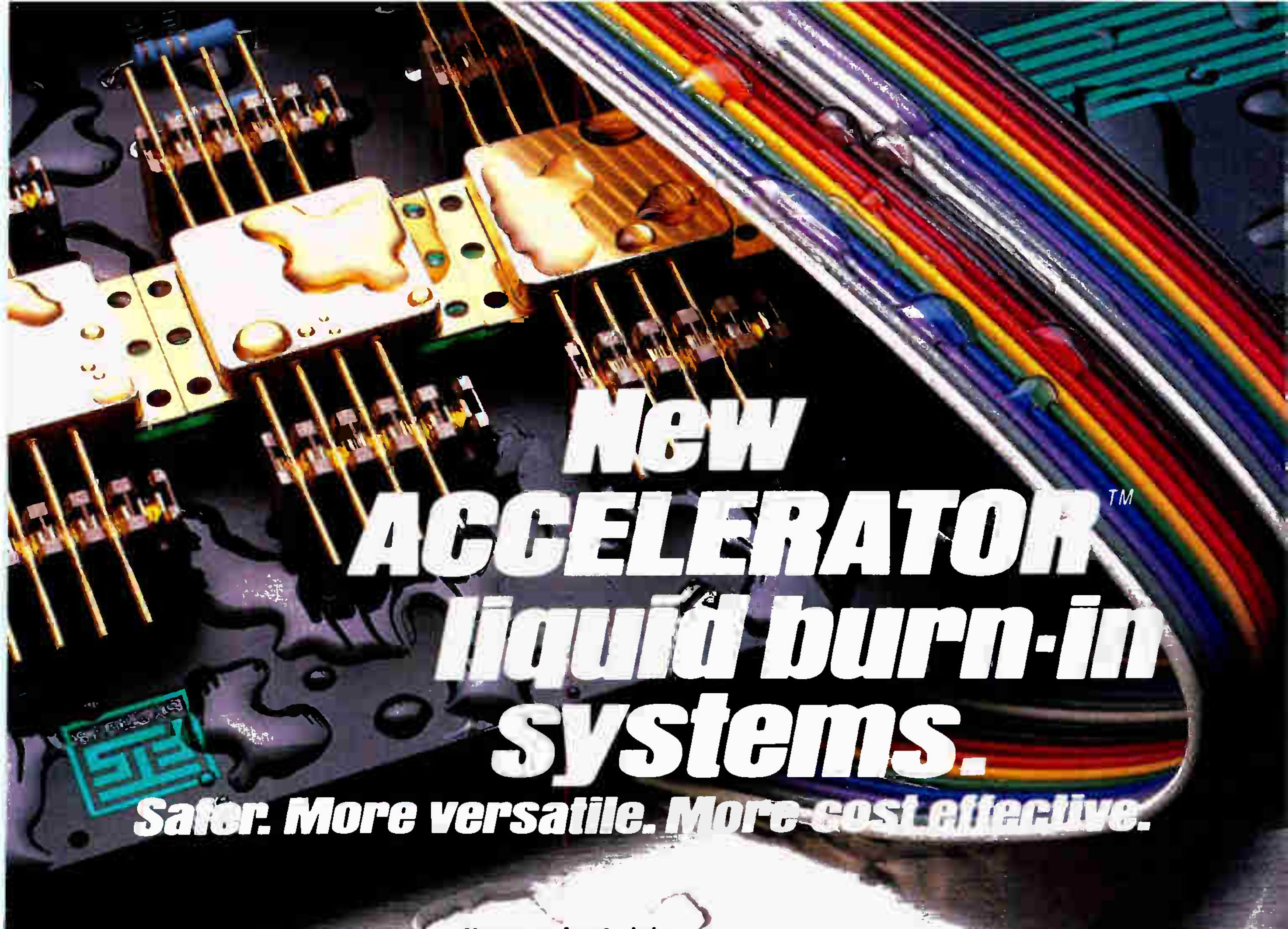
Both Hughes and Boeing are working feverishly to devise development tools that support productivity improvements throughout the entire software engineering cycle. Hughes's system contains 40 software-development products—and the number keeps growing—and Boeing's network has an equivalent number. Both companies have added several tools that have been recently developed, both in house and by outside vendors, into their systems.

Hughes's latest tool is the Design Recovery System, essentially a reverse-engineering package for existing software. It takes source code from a program and charts its structure in order to examine and analyze how it was written. The code then can be converted easily to a structure compatible with SE².

At Boeing, several products developed internally are in heavy use. One is a package called Grace, for Generic Reusable Ada Components for Engineering. It is an 18-function library created to recycle about 240 lines of Ada source code. Another is a structured analysis and design system that uses graphics to speed the early part of the development process.

Development tools are only the beginning for successful networks: just as important are the integrating software and data bases to connect the tools. For example, Boeing's BASE automatically transfers graphics and text between the different tools and converts information into formats required by various military end users.

Hughes and Boeing have financed the new software systems themselves, to the tune of about $20 million for hardware alone. They won't disclose the cost of the software. And that's not the end of it. Nidiffer points out that to incorporate the improvements already in sight will cost far more, upwards of $50 million total, "but the result will be worth it." *–Larry Waller*



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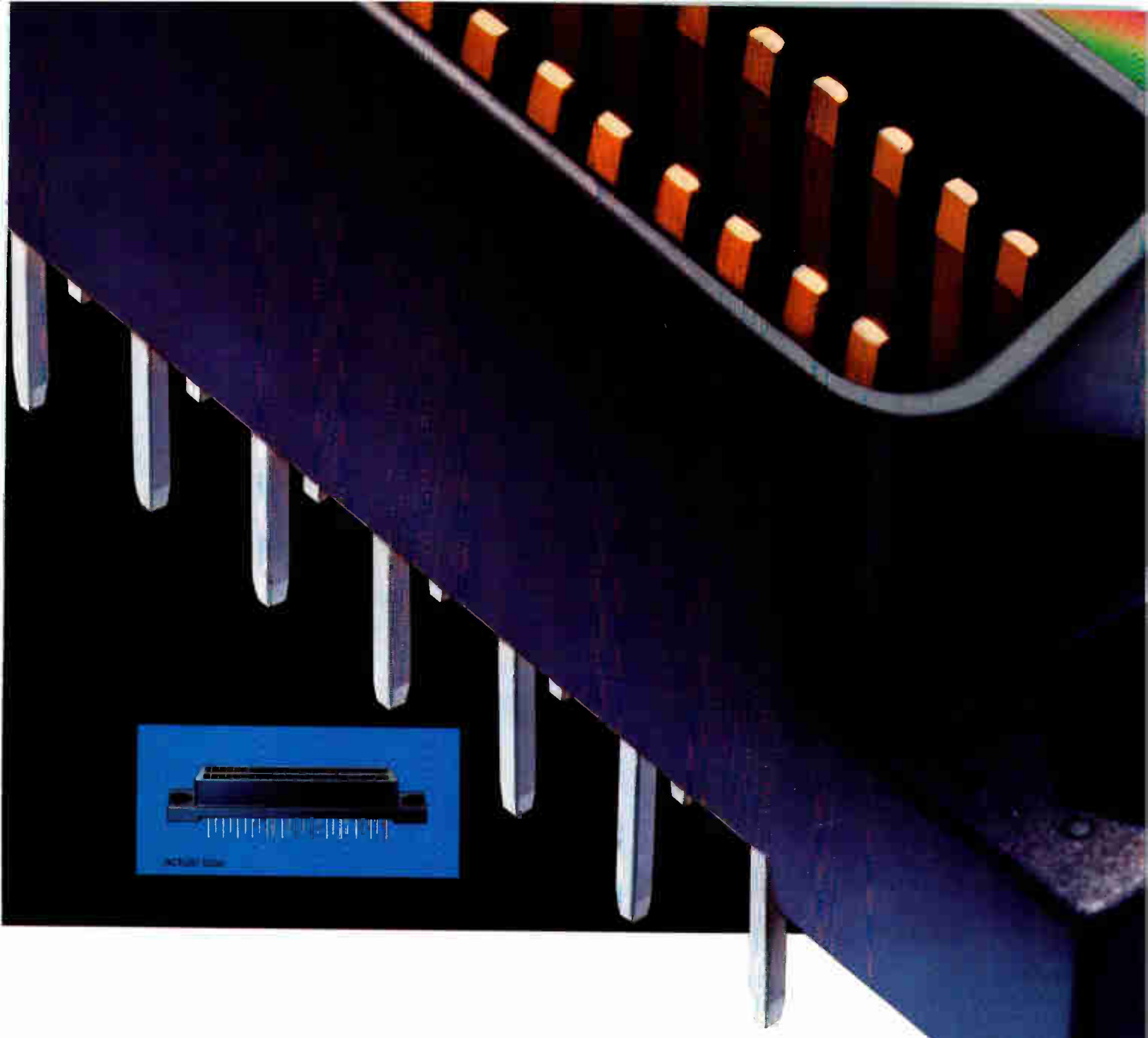
Circle 99 on reader service card



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MILITARY/AEROSPACE NEWSLETTER

THE PENTAGON WANTS TO FUND PRODUCTION R&D ON IR ARRAYS

Aiming to give a badly needed shot-in-the-arm to passive infrared technology, the Defense Department is seeking $45.1 million in the fiscal 1988 budget for the IR Focal Plane Array Producibility Initiative. Passive IR systems will be essential to the development of such advanced military systems as the Space-Based Kinetic Kill Vehicle, a key component in the Strategic Defense Initiative, as well as less-exotic weapons systems, such as the M-1 tank and TOW 3 missiles. The Defense Department says the manufacturing technology for making focal-plane arrays is lagging behind the development of materials and architectures, and could threaten to delay future programs. Yields for focal-plane arrays hover around 1%—far too low for economical production. The producibility initiative aims to tackle the manufacturing problem in much the same way as the Very High Speed Integrated Circuits Program has addressed submicron geometries for advanced ICs: by putting the work in the hands of experienced manufacturers. Like the VHSIC program, the new initiative will be funded out of the office of the Secretary of Defense, and it will require that results be in the public domain. GM/Hughes Electronics, Northrop, and Texas Instruments are the most likely participants—and beneficiaries—of the program. □

SEMATECH WILL MISS ITS DEADLINES

Sematech will not meet its self-imposed Sept. 30 deadline for choosing a headquarters location, and it now appears that its search for top management talent is also falling behind schedule. But organizers of the cooperative research group say the delays will not affect plans to set up shop by Christmas and to begin producing wafers by mid-1988. They attribute the site-selection delay to the surprisingly high number of applicants. The group received 58 proposals for 100 sites in 36 states, and has apparently narrowed that figure down to 14 finalists. Sematech's Site Selection Committee heard pitches from those 14 in late July, but a spokesman says no decisions on any proposal have been made. In the search for a pair of top executives, meanwhile, "at least 40 candidates" are vying for two posts—chief executive and chief operating officer. Sematech's founders had hoped to have a site and executives in place by late September, but no word is now expected until October or later. Some things are running on schedule, however—the organization will announce in mid-September its 12 to 14 still-unnamed founding companies. That should be about the time Congress decides just how much government funding the project will get. □

THE HEAT BUILDS ON THE MX MISSILE

The Air Force and Northrop Corp.'s Electronics Division are feeling the heat after an investigation by the House Armed Services Committee concluded that the company had mismanaged a contract to produce the inertial measurement unit for the MX missile. The report says the Hawthorne, Calif., contractor "used fictitious companies [and] extraordinary practices that led to the acquisition of uncertified parts and false certification of test results." The 126-lb. inertial measurement unit determines the missile's position as it relates to its programmed course. The report adds that the affair "has severely undermined confidence in the Air Force's ability to manage and oversee important strategic modernization efforts." Only 5 of the 17 MX test flights actually used the Northrop IMU that is installed in the nine operational MXs currently deployed. Of those five, the report asserts, two fell far out of range, apparently as a result of failures in the IMU. The device contains three gyroscopes, three sensors to measure acceleration, and other electronic components. Northrop and the Air Force deny any wrongdoing. □

MILITARY/AEROSPACE NEWSLETTER

ARMY MOVES AHEAD ON MIDRANGE BATTLEFIELD COMPUTERS...

The Army's Combat Service Support Control System is slowly moving from conception to procurement. The Army plans to deploy almost 1,200 systems by 1992 for use in such areas as intelligence, fire support, air defense, and battle planning. Specific capabilities and equipment options have not yet been set for the five-year, $153.1 million program, nor has an architecture or software environment been chosen. But preliminary architecture and concept-definition work should be done by summer's end at the Information Engineering Command at Ft. Belvoir, Va. A more thorough development effort is set to begin there this fall. One thing that's clear about the CSSCS system, however, is that it will be compatible with other Army equipment. The program is part of the Army's Command and Control System, an attempt to end the proliferation of unlike computers within Army ranks by specifying a single common hardware family. That family hasn't yet been set, but a request for proposals went out in May and responses are due this month. □

...AS ITS MOBILE MAINFRAMES GET SMALLER AND CHEAPER

Another part of the Army's move to automate its battlefield management systems—the Corps and Theater Automatic Data Processing Service Center, known as CTASC—is set for a facelift. The program is moving into its second phase, with the CTASC-1 machines—12 mobile, rugged commercial mainframes that cost $3 million each—being replaced by as many as 100 or more next-generation models. The CTASC-2 systems are smaller, more powerful, and, at under $1 million, cheaper than their predecessors. They will fit into just two trailers, instead of the three required for the CTASC-1s, and will have twice the memory. An initial order of 64 machines, with an option for 40 or more at a later date, will go to a small or minority-owned supplier this winter. The first machines are due out by late 1989. □

GRUMMAN, MARTIN MARIETTA DEVELOP TELE-OPERATED ROBOTS

Tele-operated robots for reconnaissance and anti-armor infantry support could be roaming the battlefields of tomorrow if prototype systems now being developed by Grumman Corp. and Martin Marietta Corp. prove successful. Sandia National Laboratories is managing the development effort for the Army Missile Command at Red Stone Arsenal, Ala., and it awarded development contracts to both companies this summer. The robotic vehicles will be controlled by a fiber-optic cable trailing back to a portable control pack as far as 5 km behind. The cable will carry control data and a video signal showing what's in the vehicle's path. □

E-SYSTEMS WILL DEVELOP JOINT-SERVICES RECONNAISSANCE SYSTEM

Development of a highly classified reconnaissance image-collection and processing system for U. S. battle group commands is now in the hands of Dallas-based E-Systems Inc., which this summer beat out General Dynamics Corp. and Lockheed Corp. for the joint-services contact. Coordinated by the Electronic Systems Division of the Air Force Systems Command, the deal is so hush-hush that even the value of the pact was not disclosed—the first time in memory that a program was announced without a dollar value, says one veteran command official. The Joint Service Image Processing System will process images from a wide range of reconnaissance systems, including satellites, aircraft, and ground-based equipment, and then forward them to battle group commands. Loral Corp.'s System Group in Phoenix, Ariz., and General Electric Co.'s Automated Systems Division in Burlington, Mass., are subcontractors for the program. □


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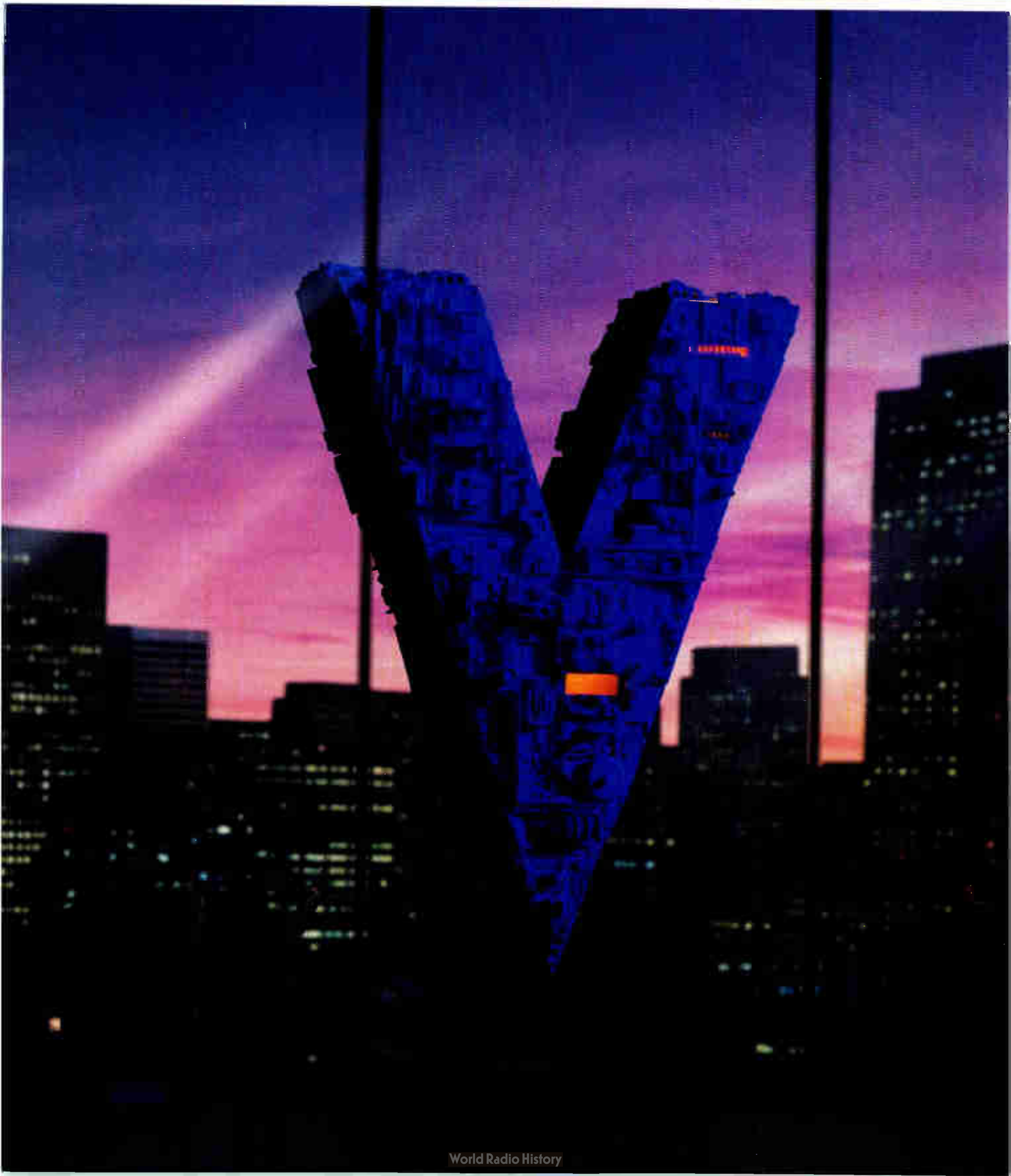
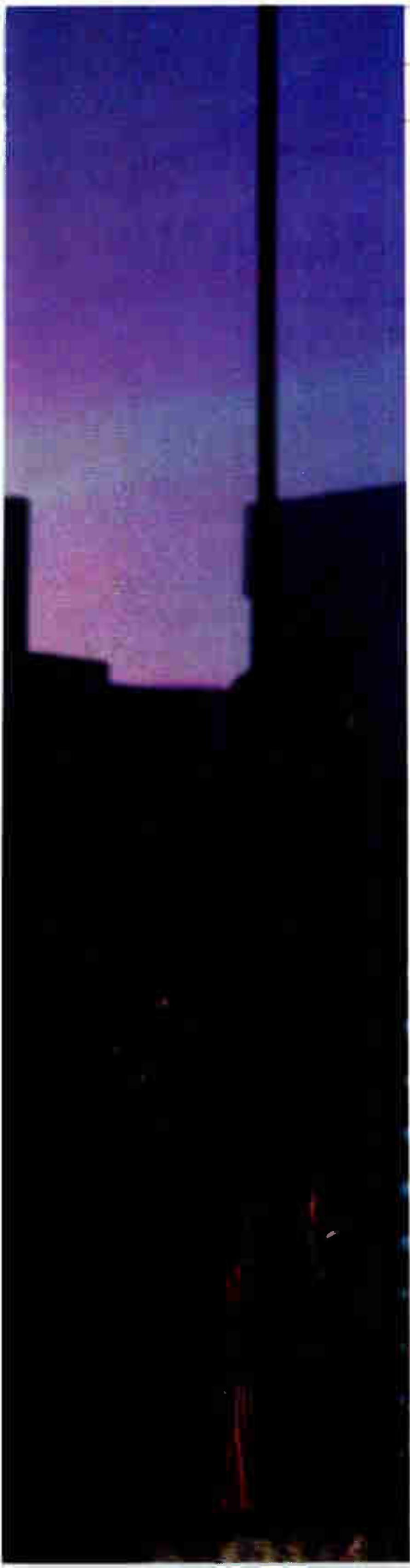
JAPAN

Electronics SPECIAL ADVERTISING SECTION

Your window of opportunity



C&C
Computers and Communications



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SPECIAL ADVERTISING SECTION

JAPAN

HIGH TECHNOLOGY IN JAPAN: AN UP-TO-DATE REPORT

After years of unimpeded growth, Japan's high-technology industry has temporarily stumbled. A confluence of factors have caused some segments of the industry to come to a screeching halt while other segments actually declined. Two world oil shortages, a saturated domestic market, and the rising value of the yen have all had a negative impact on the various segments. But the hard-hit Japanese companies are taking agressive steps to reverse their recent setbacks as this year's report indicates.

The hardest hit were the semiconductor makers, but the next generation of ICs should make the market bounce back. Telecommunications holds a lot of promise now that the laws have been liberalized. Decentralization continues to be the trend in computers. When the pattern recognition technology gets more refined, look for such items as a Japanese language word processor. The picture in the test and measurement business brightened somewhat in the first half of 1987. Optical disk consumption is on the rise thanks to a strong world-wide demand. And component makers find overseas production the answer to an ever rising yen.

This year's report was prepared by the Nomura Research Institute in Kanagawa, Japan, under the direction of Shigeaki Kaneyori, who also wrote the components update. The Semiconductor report was written by Junichi Inoue and the Telecommunications section by Shinji Yamane. Yasuhiko Arai prepared the Computers & Peripherals update while Juro Toda wrote the Pattern Recognition Technology section. Hiroshi Fukui wrote the Test & Measurement report, while the Optical Disk section was prepared by Shin Kusunoki.

Cover photo compliments of Graphtec Corp.

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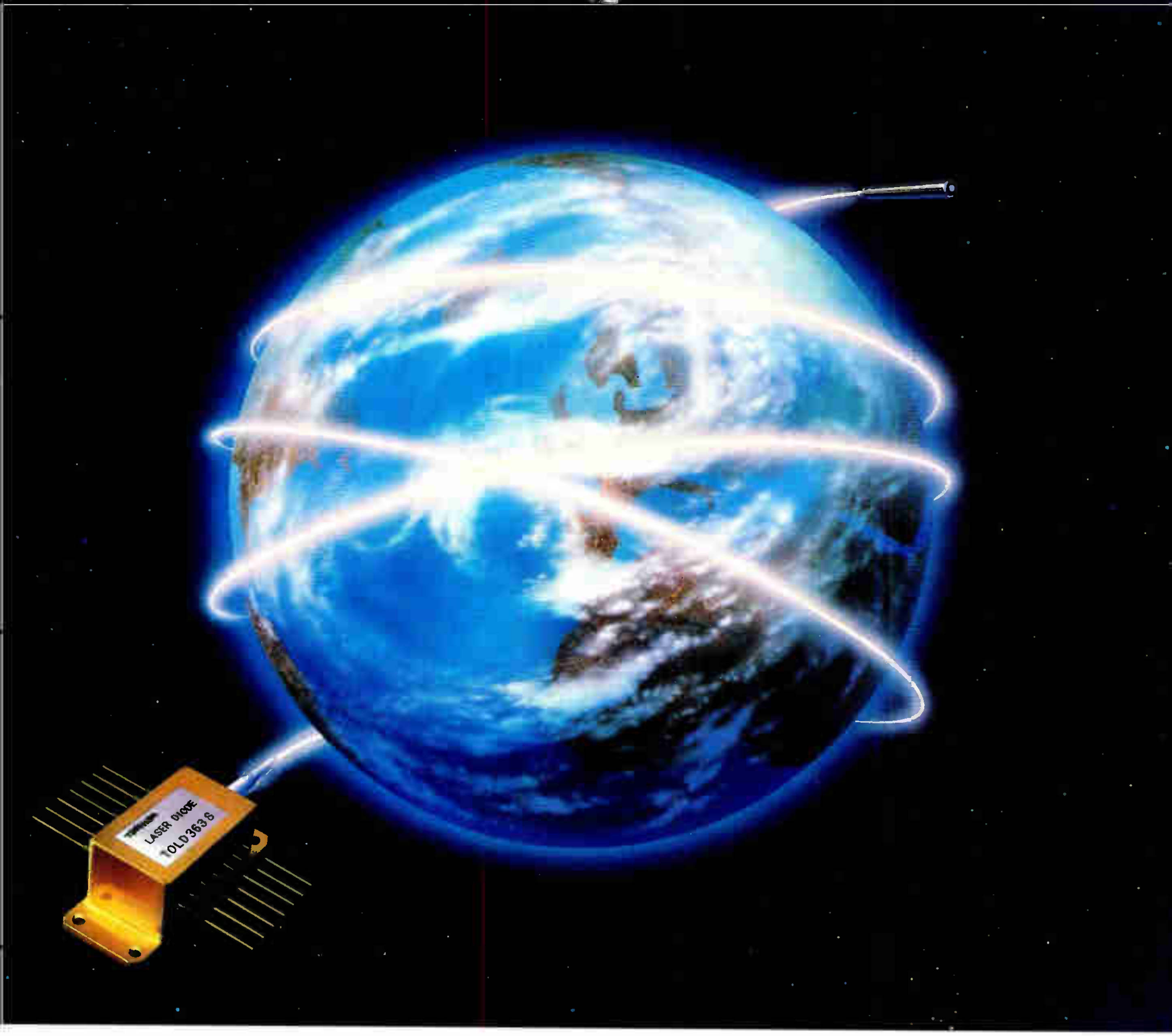

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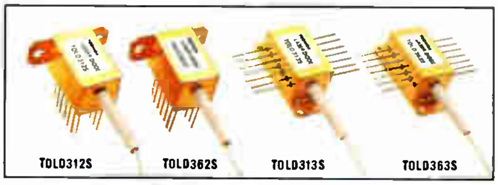

PACKAGE	1.3μm DFB	1.55μm DFB
CHIPCARRIER	TOLD300S	TOLD350S
DIL	TOLD312S	TOLD362S
BUTTERFLY	TOLD313S	TOLD363S

TOSHIBA

TOSHIBA CORPORATION TOKYO, JAPAN

SEMICONDUCTORS

Chip makers continue to introduce products despite a harsh economy

Over the last two to three years, Japan's semiconductor industry has gradually found itself in an exceedingly harsh environment—an unprecedented situation. Surplus plant and equipment investments and the cooling off of the market around 1984 are the chief villans. The situation was further compounded by the rapid deterioration of the trade climate last year.

While it is difficult to say just what the decisive blow was, the fact remains that the industry actually declined for the three years following 1984—something hard to believe for an industry that had enjoyed a steady healthy growth rate until then. What's more, the industry has been unable to find any positive signs to give an encouraging answer to the question of the hour: "When will it get back on the growth track?"

Making progress

Nevertheless, efforts made by various manufacturers since the start of 1987 appear to be having some effect, at least as far as the market environment is concerned. Specifically, production for fiscal year 1987 is forecast to reach 2.7 trillion yen from 2.3 trillion yen in 1986, an increase of 17%. If so, it would represent the first increase in the last three years.

At the same time, the pressure put on earnings with the decline of 256-Kbit dynamic random-access memory prices to about 200 yen is being alleviated as the price recovers to about 350 yen. However, these developments appear to derive more from production adjustments than to any full-fledged recovery in the marketplace.

Even in these straits, all manufacturers are busily taking steps to improve the trade climate. These basically include establishing new production plants overseas, improving existing ones, and setting up partnerships with foreign manufacturers for cooperative efforts involving technology or production. Virtually all of the big domestic manufacturers announced some measures of this sort over the past year.

NEC, for example, is reinforcing its production of logic integrated circuits and memories at its Roseville, Ca., facility, while Toshiba is embarking on full-fledged production of 1-Mbit dynamic RAMs in West Germany, and Mitsubishi Electric has decided to produce 256-Kbit static RAMs at its plant in North Carolina. More extensive global relationships are also taking shape.

Toshiba already has partnerships with Motorola, Zilog, and Intel. NEC is tied up with Intel, American Microsystems Inc., Standard Microsystems Corp., and Zilog, while Sony has links with Advanced Micro Devices Inc., for production of 256 Kbit static RAMs and other circuits.

Naturally, part of the motivation on the Japanese companies' part is to minimize the effects of the rapid increase in the value of the yen. It cannot be denied, however, that companies are gradually laying the foundation for more extensive international partnerships invoving technology, manufacturing, and sales. This kind of activity is likely to increase, especially given the desire of the manufacturers in other industries to enter this field.

The past year saw no downturn in the pace of technological development or marketing of new products aimed at capitalizing on the market's great potential and building a great demand. Notable in this reagard is the application-specific IC (ASIC), which has become a matter of priority with all manufacturers.

This is an interesting development, in light of the fact that Japan's semiconductor industry has in the past leaned heavily toward the dynamic RAM and engaged in low-run, highly diverse product lines. The trend is surfacing in a host of fields. ICs for displays is a prime example; the display manufacturers Hitachi, Toshiba, Matsushita, and Sharp are attempting to use their dominance to build up an assortment of products. There is also NEC and ASCII Corp's development of a 256-Kbit image-processing memory for personal computers, Hitachi's development of a 1-Mbit frame memory to improve the picture quality and expand the functions of the video cassette recorder. And lastly, Sony finished developing its dual-ported RAM and announced its entry into the 1-Mbit memory field.

4-Mbit ROMs

In addition, all entrants are vigorously pursuing development of processors and graphic controllers for image processing with their eyes on the bright prospects for growth in that field. Meanwhile, they are bracing for mass production of 4-Mbit masked ROMs. These will store character fonts for use in Japanese-language word processors and printers, which are now in demand.

In terms of new types of products, a major trend is the response to mass production of the 1-Mbit dynamic RAM, which emerged on a full-scale beginning last last year. The big semiconductor manufacturers are preparing to increase this production later this year from a monthly volume of a few hundred thousands of units to roughly two million chips. NEC, Fujitsu, Hitachi, Toshiba, Matsushita, Mitsubishi, and Oki have all announced products or are delivering them, all offering their own distinctive features.

There has also been a stream of other types of new memory devices. NEC and Mitsubishi, for example, have each unveiled 256-Kbit static RAM devices boasting a 35-ns access time; the 256-Kbit electrically erasable programmable read-only memory announced by Sanyo features a read time of 50 ns.

Besides such devices, there has also been a succession of announcements of elements that are to form the focus of corporate efforts in the future. At the International Solid-State Circuit Conference held this February, Toshiba stated that it was taking aim at a 4-Mbit erasable PROM, and Hitachi and Sony made similar statements concerning the 1-Mbit static RAM. In addition, at this conference five companies—Toshiba, Hitachi, Fujitsu, Mitsubishi, and Matsushita—announced the development of 4-Mbit dynamic RAMs or circuit technology following those made by NEC and Toshiba last year.

Moreover, this year's announcements are much closer to being viable products than were previous ones. In each case, the

Focus on Oki Electronic Devices Group

Systems technology is having a significant impact on the way in which large-scale integrated circuits are designed and used. Semiconductors have become extremely complex, especially with today's CMOS ASIC technology, and are much more than mere components; they are systems in and of themselves.

To succeed in today's world market for ICs, manufacturers must adopt the mentality and methods of systems makers. Semiconductor companies must be ready and able to enter into a working partnership with their customers so that solutions can be found for the unique problems faced by systems manufacturers.

Gone are the days when an IC producer could simply manufacture a variety of commodity products and expect to sell them in high volume. Today, there is a need to understand the design problems and end-use environment of systems. The IC manufacturer must offer systems technology for customer solutions.

The systems market is constantly changing, and semiconductor manufacturers must change with it, providing an ever-widening variety of extremely complex devices tailored to specific systems applications.

A systems orientation would require organizational and procedural changes for most semiconductor manufacturers, but Oki has been designing and manufacturing systems since the company was founded over 100 years ago and is intimately familiar with the problems that systems companies face.

Because Oki has gained extensive experience as a designer and producer of system products, the company has the unique ability to design building blocks that improve the designs of its customers. Oki brings its systems experience to bear on its silicon offerings in the world marketplace.

To help with the implementation of new systems, Oki offers a variety of chip mounting techniques on its high-speed, high-capacity automated assembly lines. A large percentage of the company's revenues are reinvested into specific areas of research and development for the benefit of future systems. At the company's new research and development laboratories in Hachioji, for example, Oki is refining its 0.8-μm CMOS technology and has begun pilot production of its 4-Mbit dynamic random-access memories.

Oki has long experience with the problems faced by systems manufacturers. The company has a tradition of developing close, intense working relationships with increasingly sophisticated systems manufacturers and providing them with the best, most advanced system technology solutions.

Masao Nogami, president

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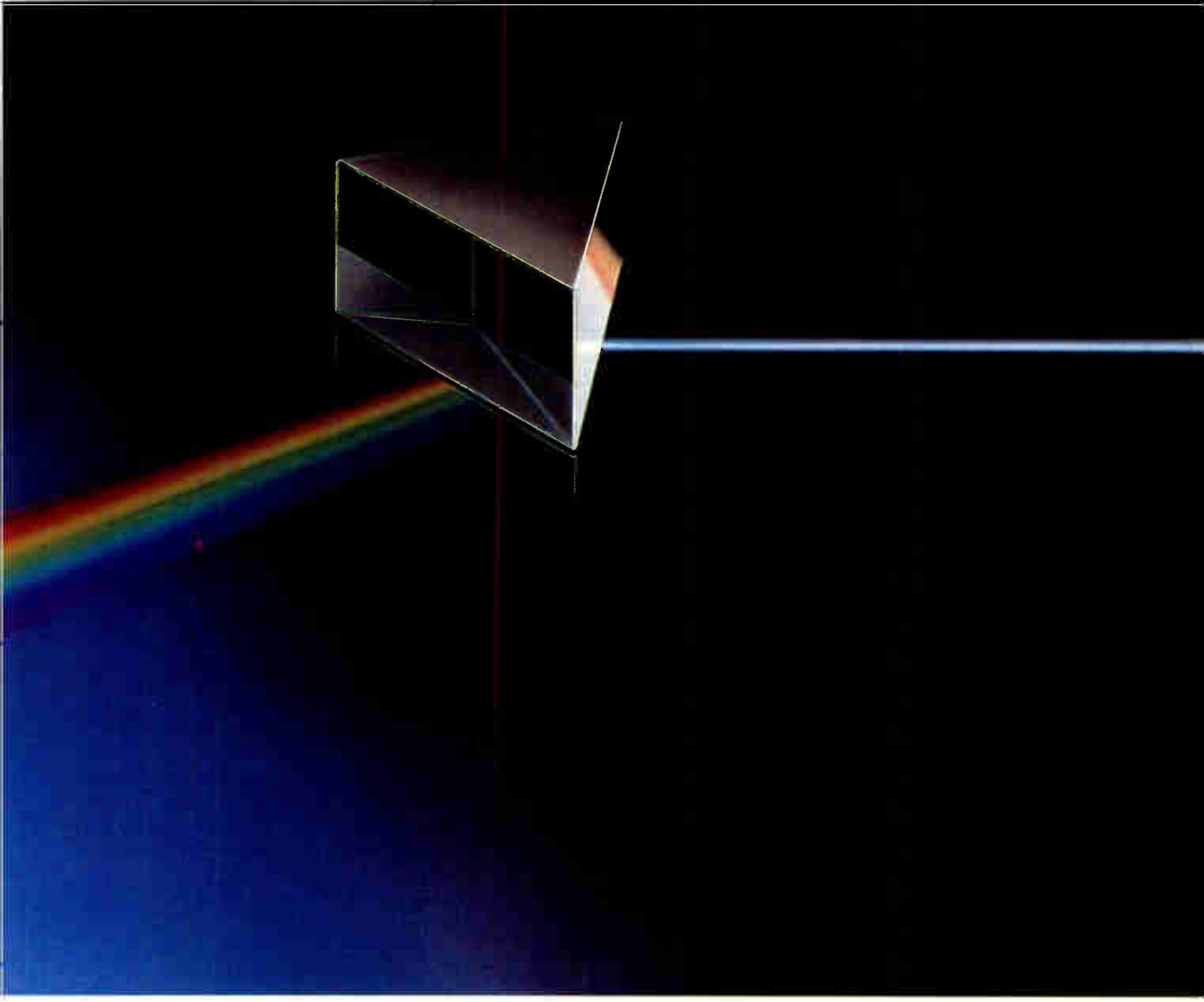

Response

DRAM

Product No.		Organization	Access Time Maximum(ns) tRAC	Access Time Maximum(ns) tCAC	Cycle Time Minimum(ns)	Mode
256K	AAA2800 SERIES	256KX1	60/70/80	11/12/13	121/136/151	Static column decode, Page Nibble Clocked Serial
1M	AAA1M100 SERIES	1MX1	100/120	20/25	190/220	Static column decode, Page
	AAA1M104 SERIES	256KX4	100/120	20/25	190/220	Static column decode, Page
1M	*AAA1M200 SERIES	1MX1	60/80	15/20	100/130	Static column decode, Page Nibble
	*AAA1M204 SERIES	256KX4	60/80	15/20	100/130	Static column decode, Page

(Products marked * are currently under development.)

SRAM

Product No.		Organization	Access Time Maximum(ns)
16K	AAA16K4	4KX4	35
64K	AAA64K1	64KX1	35/45

DRAM MODULE

Product No.	Organization	Access Time(ns)
MM2800 SERIES	256KX8/9	70/80/100

VIDEO RAM MODULE

Product No.	Organization	Access Time(ns)	Function
AAA3081K	256KX16	13/15/20	** Serial Port
AAA3082K	256KX8X2	25/30/40	** Dual Port
AAA3083K	512KX8	70/80/90	** Random Access

(**Customized Option Available)

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NMB SEMICONDUCTOR

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devices have submicron design rules and various elaborations, such as countermeasures for soft errors from alpha rays on the ever shrinking cell area. There is also a diversity in memory cell structure, including trench and laminated types. Sample shipments could begin next year.

Another topic is the progress being made on the chip that is part of The Real-Time Operating System Nuclear (TRON) project, with a 32-bit processor set to debut on the market this December (see Computers and Peripherals). The main participants in the project are Hitachi, Fujitsu, Mitsubishi, Toshiba, and Matsushita. It is gaining momentum faster than initially expected, and its future efforts in the areas of personal computers and office automation equipment will be closely monitored.

There were several significant announcements concerning development of semiconductor device technology this year as well, one being the research in the area of 16-Mbit devices. The approximately 0.5-μm design rules in this class are inevitably difficult to accommodate through the existing processes and elemental technology or even improved versions along the same lines.

Solid State Conference

At the International Solid-State Circuits Conference, Nippon Telegraph & Telephone announced that it had developed a 16-Mbit dynamic RAM by employing element fabrication technology with a design rule of 0.7 μm. A high-performance on-chip error correction circuit termed an error correction code was incorporated as an alpha-ray countermeasure, and a new trench type capacitor was employed as part of the technology to shrink the memory cell area.

Although several problems must be resolved before commercialization can take place, this is the first such development in the world and must be considered important. Oki Electric also announced that it had developed a 4-Mbit pseudo static RAM by adding a refresh function to a 4-Mbit dynamic RAM.

This movement toward greater scales of integration and higher speeds for silicon devices is being paralleled by that to raise devices employing compounds for substrates to the level of practical usage. Development here has thus far reached the 4-Kbit static RAM level. A higher scale of integration and expanded range of applications are anticipated with an improvement in the quality of the materials for substrates and for other elements.

A notable item is the blue light-emitting diode developed by a research group of the Tokyo Institute of Technology this March. Its luminance shows a remarkable improvement over models announced previously. The core technology is epitaxial growth through metal organic chemical vapor deposition with a semiconductor of the Group II-VI elements (zinc selenium, zinc sulphur) on a gallium arsenide substrate of the Group III-V elements. The results have brought a blue LED one step closer to practical use and could therefore pave the way for the incorporation of three-colored LEDs into full-color displays.

This LED research is also expected to quicken the tempo of research on blue laser diodes. Practical use here would have a great impact on optical recording, optical printers, and various other fields.

Manufacturing

There is also news on the semiconductor manufacturing equipment front. Obviously, this industry has been placed in a difficult position with the restraints on investment by its customers in the semiconductor industry over the last three years. However, it is attempting to turn the mass production of new devices and the improving market climate into new growth.

In particular, the industry harbors great expectations for the investment that is becoming necessary as production of devices in the 1-Mbit dynamic RAM class begins to emerge on a full scale. The related manufacturing equipment may be exemplified by steppers enabling precise pattern formation through the use of low-pressure chemical vapor deposition systems needed for formation of quality thin-film for demanding stepper coverage, and ion and dry etching equipment.

The industry is also making a push in such fields as film fabrication equipment related to the rapidly expanding fields of optical disks and to liquid-crystal displays, which have good potential for future growth with practical use of the active matrix, as well as inspection equipment. Users are making increasing investments in these fields. Altogether, several dozen corporations are active in the field of optical disks alone, whether ROM, write-once read-many (WORM), or erasable direct read after write (EDRAW).

Investments on facilities from these corporations make this a promising field for the semiconductor manufacturing equipment industry, at least over the short term. As for liquid-crystal display devices, the demand is anticipated to steadily expand as application broadens from pocket TVs to office automation, factory automation, and automotive fields in the years ahead.

There are also extensive programs concerning equipment designed for the development or support of innovative semiconductor devices. In the lithography field, X-ray and laser sources are coming to the fore as replacements for the current ultraviolet light sources. X-ray lithography research has thus far been centered in the big semiconductor manufacturers and NTT, but the results are being translated into commercial products by Nippon Kogaku and Canon. Late last year, Matsushita announced technology for pattern formation using an excimer laser (krypton-flourine) as the stepper light source. And Canon is working on X-ray sources and lasers.

In short, development in the semiconductor industry is generating a succession of new technology that is gradually being placed on commercial footing. This, in turn, is spawning new equipment for mass production or developmental support in the semiconductor manufacturing equipment industry, which consequently appears to be on the verge of a new expansion, provided the right opportunities can be found and exploited.

TELECOMMUNICATIONS

Future growth areas are mobile phones, facsimile

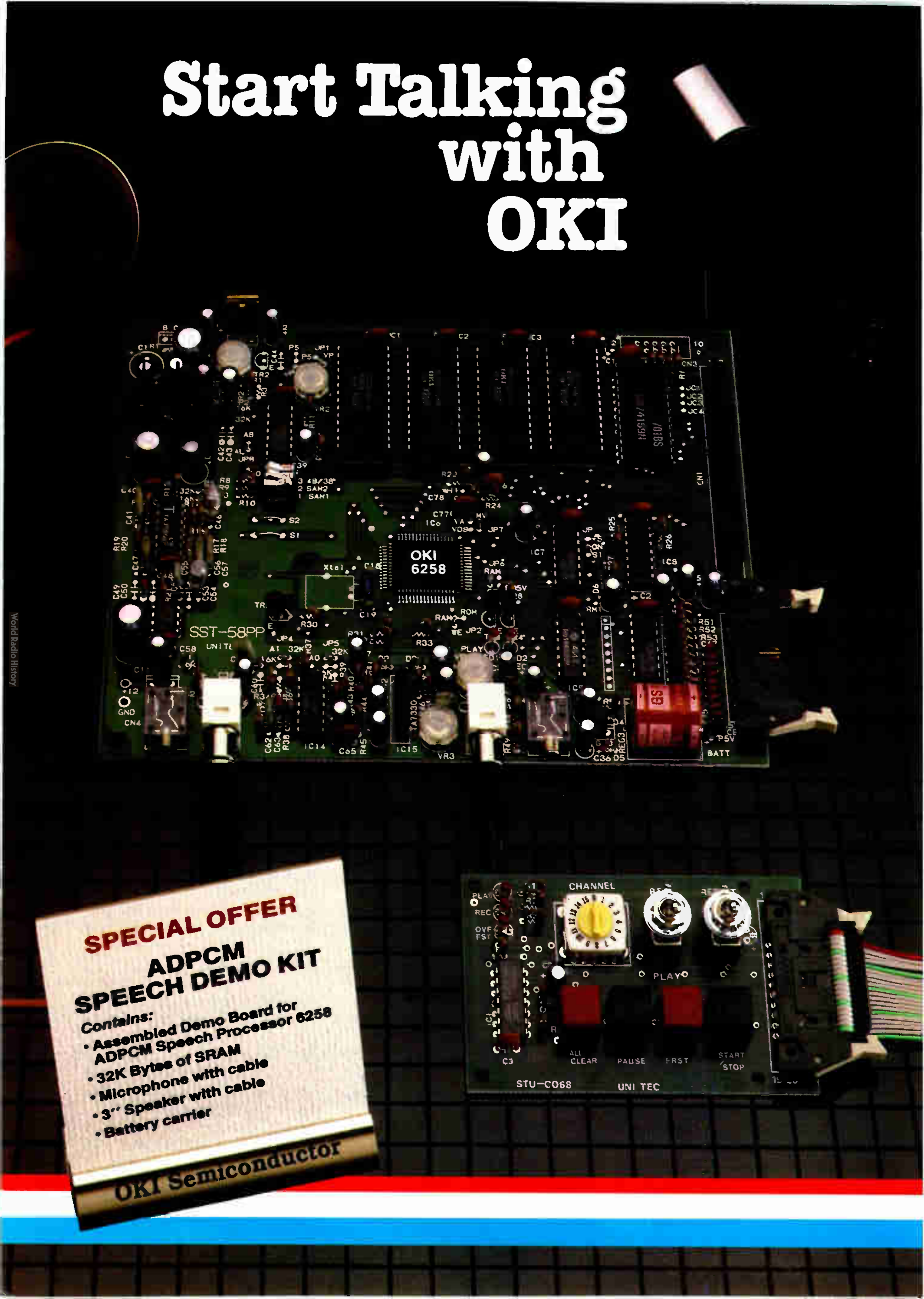
Japan's communications equipment industry has been rapidly developing over the past five years, but since the latter half of 1985, the business climate has become quite unfavorable, due to the rapid rise of the yen compared with the dollar. This makes exporting unprofitable. Another factor is the intensified competition from the newly industrialized countries.

And in general, the growth rate projected for the next five years (see table) is quite low, despite some new developments expected in the domestic market.

Although unfavorable export conditions and increasing overseas production will affect Japan's production of communication equipment, the domestic telephone equipment market is expected to stay strong thanks to the liberalized telecommunications laws. And the facsimile market is also expected to grow, as personal facsimile systems come on the market.

According to the Ministry of Post and Telecommunications, a wave of new products is expected to flood the market in the next five years.

- Marinet telephones are radio communication telephones for use within ports by small ships that don't have large, sophisticated radio systems. These are expected to come on the scene in April, 1988.
- Convenience radio phones are simplified mobile telephone systems that do not require a base station. This service will be available to customers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PROJECTED GROWTH RATE OF TELECOMMUNICATIONS INDUSTRY			
Product	1985	1990	Compound Growth Rate 1985–1990
Telephone equipment	369 (In Billion Yen)	420 (In Billion Yen)	2.6%
Facsimile	308	391	4.9
New media equipment	16	24	8.4
PBXs	89	133	8.4
Other exchanges	214	267	4.5
Transmission equipment	346	463	6.0
Radio communication equipment	353	476	6.2
Total	1,695	2,174	5.1
Source: Computer Industries Association of Japan			

sometime next spring.

- Closed-circuit radio station, which uses micro power radio transmission (below 0.01 W) for communication within a factory site or a building for telemeter/telecontrol systems, low-speed data transmission, and inside-premise paging.
- High definition TV based on the broadcast satellite BS-3 will start in 1990 when the satellite is launched. The standard Japan is proposing is the Multiple Sub-Nyquist Sampling Encoding (MUSE) system, developed at Nippon Hoso Kyokai (NHK), Japan's Public Broadcasting Organization, jointly with the US.
- Extended-definition TV, unlike high-definition TV, is compatible with the conventional TV standards and will be commercialized in 1989.
- Facsimile broadcast, which is a system superimposing such images as photographs on TV broadcasting signals, is being studied. A report is to be issued by the end of 1988.
- FM multiple broadcasting, in which text and images are broadcast on audio subcarrier signals, will start after the necessary legal procedures are completed in 1988.
- AM stereo broadcasting is expected to begin shortly after technical problems are resolved.
- High fidelity digital audio broadcasting is being studied, with a report expected in 1988 and commercialization to begin in 1991.
- Pulse code modulation audio broadcasting will be conducted full scale once the BS-3 satellite is launched. Since 1984 it has been conducted by NHK within the framework of direct broadcast satellite service.

The Shinkansen bullet train is also scheduled to implement new communication services such as personal computer communication and personal facsimile service taking advantage of leakage coaxial cables (LCX) to be installed by 1989.

In addition, two types of television telephone systems (picture phones) using ordinary telephone lines that send and receive still images and voice transmissions have been developed by Nippon Telegraph & Telephone and Sony and by Mitsubishi Electric.

The system by NTT and Sony, which costs 49,800 Yen is a 4-inch CRT and video camera that attaches to a telephone. Transmission of video signals takes 9 s, during which voice communication is suppressed.

On the other hand, Mitsubishi Electric's system, which costs 198,000 Yen is a 3-inch CRT, video camera, and telephone in which transmission of the video image takes just 5.5 s.

Another area of expected growth is in cable TV. Cable TV, two-way cable TV, and satellite distribution of broadcast programs are all establishing footholds in large cities. In 1985 there were 550 cable facilities but by 1991 it is estimated that there will be 1,150. Currently, there are virtually no two-way cable systems, but by 1991 they will make up 17% of the total number of cable systems. The number of earth stations for satellite communications is expected to grow from 96 in 1985 to 13,000 in 1991.

Two-way cable equipment such as amplifiers are provided by Yagi Antenna, Maspro, DX Antenna, and others; Fujitsu developed a cable system based on optical digital communication.

New common carriers

In addition, new common carriers started service in 1986 and their long-distance telephone service to compete with NTT is scheduled to start later this year. In 1988, common carriers will start service using satellite communication technology.

Mobile communication is one of the important segments for future growth, specifically, portable pagers and mobile phones. On the other hand, joint research and development of space communication technology has begun. A stationary space platform will house large antennas, solid-state power amplifiers, millimeter radio wave transceivers, and satellite exchangers. The participants in this project include NTT, Kokusai Denshin Denwa, NHK Engineering Services, Toshiba, Mitsubishi, Hitachi, Fujitsu, NEC, Tokyo Electric Power, and Toyota Motor.

Decentralized processing is the name of the game in computing

For the last few years, the prevailing trend in the computer industry has been the decentralization of processing. It has been given further impetus by the inroads made by Digital Equipment Corp. and the introduction of International Business Machines Corp.'s Systems Applications Architecture (SAA) to counter it.

The trend even holds true in general-purpose computers, where announcements of small systems have come to the fore. Two stellar examples include DEC's VAX and the IBM 9370. The major Japanese representatives in this market are Fujitsu's M730 and NEC's ACOS 3300.

Small general-purpose systems are aiming for a position in between large, general-purpose computers and office computers, to form the nucleus of decentralized processing. Such models are compatible with both the high- and low-end models, and provide a connection with personal computers and work stations. In general, there is a shift away from pyramids topped by large, general-purpose computers and toward peer-to-peer networking.

Office processors

There have been no major new developments in the area of large, general-purpose computers, with the exception of Fujitsu's development of a new series. IBM continues to hold sway over this market, which is basically awaiting the announcement of Summit (IBM's next mainframe for the world market), barring any major change in the 3090 series.

However, there has been a great deal of activity aimed at the marketing of what are termed office processors as node computers linking general-purpose machines and work stations or personal computers; these office processors also serve as host computers for small offices. These can be regarded as alternatives to IBM's 38/36 series and DEC's VAX series. Systems are growing smaller in size and offering higher performance as a result of the increasing capacity of semiconductor memories, the shrinking diameters and higher densities of magnetic disks, and the penetration of 32-bit microprocessors.

In addition to turnkey business software, such systems offer an abundance of capabilities on a par with those of general-purpose machines, such as Open Systems Interface communications, multihost functions, decentralized relational database functions, and micro-to-mainframe links, as well as functions for fourth-generation language and electronic file functions. In these applications, Unix is the most widely used operating system.

The main products are Fujitsu's K and R series, Hitachi's L-70/80, NEC's System 3100, and Univac Japan's U family.

Minicomputers are generally not found in Japanese offices, and the need for office processors as nodes of decentralized processing is only expected to increase. This, in turn, is raising expectations for enhanced communications capabilities. Closely watched in this regard is the orientation of IBM's Silver Lake, the successor to its System/38 and /36 lines.

The spread of the 80386, 68020, and other 32-bit microprocessors is becoming evident in the appearance of new 32-bit work stations and personal computers. An increase in the processing capabilities of such personal machines is bound to spur greater system decentralization.

The list of Japanese manufacturers announcing 32-bit work stations and personal computers includes Fujitsu, Mitsubishi, NEC, IBM Japan, and Hitachi. IBM Japan's product, called the PS/55, is positioned as an SAA model, and is likely to have a great impact on products of other companies, both in the US and Japan.

At the same time, attention is being focused at Fujitsu's work station, the G Series, for its accommodation of System Integration Architecture (SIA), which is one of the approaches of the System Development Architecture and Support facility (SDAS) announced by Fujitsu in response to SAA. It is equivalent to IBM's PS/2 or PS/55.

Unix

Unix is generally preferred as the operating system for 32-bit work stations. It is supplied with Fujitsu's G Series and NEC's N5300AD, for example. Things could change, however, with wide-scale acceptance of OS/2 and MS-DOS Version 5.0.

IBM's SAA announcement also caused quite a stir among Japanese mainframe manufacturers. Fujitsu was the first to respond (with its SDAS and its SIA), and other mainframe and office computer manufacturers are expected to follow suit with similar announcements.

In addition to the growing usage of 32-bit microprocessors, a new trend in the area of personal computers is the addition of audio-visual functions in popularly-priced models. The AV touches of Apple's Macintosh II and IBM's PS/2 led to arrangements for richer display colors, fm sound, and other multimedia features as exemplified by Sharp's X68000, NEC's PC88 Series, and Fujitsu's FM77 AV40. This trend is likely to accelerate with the acceptance of CD-ROMs, CD-visual, and CD-interactive disks.

Minicomputers are in widespread use in turnkey systems for engineering and factory automation applications, particularly computer-aided design and manufacturing. A recent development is the increasing popularity of DEC's VAX for such purposes. Machines built with reduced instruction set (RISC) architecture (Yokogawa Hewlett-Packard and Yokogawa Electric) are also on the rise.

Application of engineering work stations for engineering purposes and software development is also going into full swing in Japan. American manufacturers such as Apollo, Sun, DEC, and YHP hold a big share of this market, while Sumitomo Electric Industries (Ustation), Sony, Toshiba, Hitachi, and NEC are attempting to build up theirs.

Particularly extensive inroads are being made by Sony's NEWS product, which boasts an extemely good price performance ratio. It is built around two 68020 microprocessors and costs under one million yen. It can also be used as a VAX terminal, a feature that is helping it get adopted in research and development laboratories.

The other manufacturers, and NEC in particular, are also making vigorous efforts in this area. Fujitsu as well has, for the first time, announced an engineering work station as the high-end model for its G Series.

Sigma and TRON

The Japanese computer industry is bound to be greatly affected by two projects now going on: Sigma and TRON. The former is being promoted by the Ministry of International Trade and Industry, and the latter on the private level, headed by Professor Sakamura of the University of Tokyo.

The Sigma project is aimed at improving software productivity as a means of meeting the software crisis. The main elements are determining a common operating system (based on Unix System V), preparing a Sigma work station, and instituting a Sigma center to serve as a database tool available to all participants. The scale of the project swelled with the entry of IBM Japan as a participant last year.

Sigma work stations have been announced by Sumitomo Electric Industries, Omron Tateishi Electronics, Ricoh, DEC, and other major computer manufacturers. A Sigma in-circuit emulator has already been announced for debugging and testing in the microcomputer field.

The Sigma center is being equipped with four mainframes from Nippon Telegraph & Telephone, Hitachi, Fujitsu, and NEC. Testing is to begin at the center this October.

The objective of the TRON (The Real Time Operating System Nuclear) project is the creation of a system of computers with a man-machine interface so sophisticated that compatibility ceases to be a concern. The system would consolidate everything from microprocessors, work stations, robot controllers, general-purpose computers, and network controllers to communications equipment in the public domain in a single architecture.

A real-time operating system (Industrial TRON or ITRON) has already been marketed for controlling robots. Development of a 32-bit microprocessor is also moving ahead; shipments of the processor developed jointly by Fujitsu, Hitahci, and Mitsubishi are set to begin late this year. Toshiba and Matsushita are also developing microprocessors.

NTT is leading the development of Central or Communication TRON (CTRON) as an operating system for switching and communications control equipment in the public domain. An announcement is expected in conjunction with the inauguration of the Integrated Services Digital Network.

For the project's work station and personal computer (Business TRON or BTRON), Matsushita is developing the test machines and the related operating system (BTRON-OS) in a network type of file structure.

Desktop publishing is also catching on in Japan. The problem is, however, that the volume of data per document in Japan is more than fifty times as great as it is for the West, and the characters themselves are far more difficult to handle. For this reason, full-fledged desktop publishing is not possible without powerful equipment like high-speed 32-bit machines. These same factors complicate software development.

Software development

It is also true, however, that NEC, Canon, Fuji-Xerox, and numerous other corporations are making great strides in software development in this field. Sony intends to expand desktop publishing by forming a Desktop Publishing League with a group of 42 software houses and other companies based on the use of NEWS, its engineering work station.

Development and application of a Japanese-language postscript is also on the agenda of the TRON project. The desktop publishing market may be expected to expand further with this technology.

The most notable developments concerning peripherals are in the printer market. The mainstream printer for office use is currently the 24-pin dot matric impact serial printer. The dominant products are those from NEC, Epson, Tokyo Electric, and Oki Electric. Along with the spread of word processors, however, the market for thermal transfer printers has begun to soar, and other non-impact printers such as the electrophotographic (which uses a laser light source), and ink-jet printers are also becoming more popular.

Japan is the biggest supplier of laser printer engines, with an overwhelming share of the world market. Up to now, the chief vendors have been Ricoh and Canon, but their position is being challenged by a host of companies that have entered the market since last year.

Among them are Tokyo Electric, NEC, Kyocera, and Casio, as well as copy machine manufacturers and manufacturers of conventional information processing equipment. The level of production technology is rising and the price of controllers is falling, which means that the thousand-dollar laser printer is on the horizon.

Ink-jet printers are steadily growing more reliable. Epson's product has found wide acceptance where noise is a major concern. A new type called a melting-jet printer is also expected shortly.

Color printers

There has also been a stream of new full-color printers employing thermal transfer, ink-jet, electrophotographic, and silver chloride photographic formats.

An up-and-coming model is the culmination of thermal transfer printer technology. It was developed jointly by Dainippon Printing and Fuji-Xerox. And several other companies including Hitachi are coming out with their own versions. The main feature is the rich tonal expression, but the printer needs to acquire greater precision and the capability of printing on a larger scale.

There are also many other types of thermal transfer printers, manufactured by such companies as Seiko Electroinc, Shinko Electric, and Epson. Epson's product is a resistive film type with the potential for high-resolution image printing.

Many manufacturers have also come out with ink-jet printers, the most unique of which comes from Canon—the bubble jet printer. In operation, the printer forms bubbles in the nozzle to force out any ink that accumulates. Its main selling points are its high speed and quality printing.

Canon is also manufacturing a full-color printer using laser technology that is capable of high speeds yet costs little to operate. From Fuji Photo Film come silver chloride photographic printers, which use LED exposure and thermal development and transfer technology to produce outputs with the quality of photographs.

In the area of storage devices, the notable trend is the adoption of optical disks. This is being spurred by the emerging use of CD-ROMs along with audio-visual peripherals in personal computers and by IBM's decision to use a write-once optical disk as external memory for its new PS/2.

Although CD-ROMs were traditionally supplied by such vendors as Sony, Matsushita, and Sanyo, the entry of the big personal computer makers into the CD-ROM market has raised the possibility of wide-scale acceptance of the CD-ROM as a peripheral for a personal computer. Extended capabilities and wider usage is expected with the availability of CD-V, CD-I, and digital video interactive disks.

IBM's adoption of an optical disk for its PS/2 looms large and will presumably lead to a string of products from several manufacturers. Nevertheless, many are of the opinion that extensive penetration of optical disks will have to await the development of a viable erase-and-rewrite type. Sharp, Sony, and Nippon Kogaku bear watching here.

Image input devices are also making increasing inroads, mainly as options for portable word processors. Along with the growth of desktop publishing and the rise in the resolution and number of colors of displays, usage of scanners is likely to broaden from personal computers to a variety of high-end machines.

PATTERN RECOGNITION TECHNOLOGY

Enhanced capabilities will stir up the market

Pattern recognition technology is a generic term describing equipment used to recognize audio, characters, and images. In Japan, commercialization is in its infancy in all three of these market segments; sizeable markets have yet to be developed.

Nevertheless, an immense demand is expected to emerge for such products as a means of significantly improving the man-machine interface—a crucial item in the information equipment industry's agenda.

By comparison with impressive assortment of other information processing equipment available, there is little variety among pattern recognition technology devices with a data input function. Information processing and memory devices offer a wide diversity in functions and prices and also command great markets. It can also be noted that the level of sophistication of pattern recognition technology has not been entirely satisfactory in the eyes of users.

A major expansion in the range of pattern recognition products is anticipated in the coming years. The market could expand substantially if an improvement occurs in recognition technology itself as well as in product concept, design, and capabilities.

Basically, further advances in the product and technological aspects of patten recognition depend on the degree of commitment on the part of suppliers, who can look forward to healthy expansion in this field. Trends are begining to emerge in commercialization of audio, character, and image recognition technology.

Voice Recognition

In the U.S., audio recognition devices, that is, those that recognize human voices, have been marketed as extensions of equipment for the handicapped. In Japan, however, voice recognition has been targeted for use in office equipment as an alternative to entering information with a keyboard and in factory automation systems for sorting and control functions.

Shipments of all suppliers are still on a limited basis and the size of the market does not exceed 1 billion yen.

On the technical front, the development of speaker independent recognition devices, that is those that can recognize anyone's speech, is still in the experimental stage. The products that are either being delivered in sample quantities or are in full production are speaker dependent, that is the device needs to be trained to recognize the voice patterns of only certain people, and with a limited vocabulary at that. Models that recognize particularly small vocabularies are supplied as either chips or boards.

The list of Japanese corporations active in voice recognition include such names as NEC, Hitachi, Fujitsu Ltd., Kyosan Electric Manufacturing, Matsushita Electric Industry Group, Sanyo Electric, and Ricoh. NEC, Sanyo, and Matsushita also supply voice recognition chips, which are used in low-performance products such as games and high-tech toys such as robots. Kyosan and NEC are offering voice recognition boards mainly as enhancements for personal computers and for factory automation systems.

Character Recognition

Commercialization in this segment is being pursued most energetically by NEC, which is marketing a DP200 model and a high-end DP300 model. Recently Ricoh has garnered attention for its high-performance voice recognition device based on fuzzy logic.

There are two basic types of character recognition technology devices: optical character readers and online character readers. The former type can be divided into three categories: (1) high-end models capable of recognizing even handwritten Kanji characters; (2) intermediate models capable of recognizing typed Kanji characters; and (3) low-end models that can only recognize typed alphanumeric characters.

As the ultimate OCR target in Japan, the high-end models are still in the research laboratories. Intermediate models now under development will be aimed at applications in text input; commercialization remains in its infancy, with users awaiting products with satisfactory performance and price. Low-end products are becoming widely used as input devices for data from accounting slips or notes among financial institutions, distributors, and public institutions.

The market is currently estimated at 15 to 20 billion yen. Dominating this market are Nippon Telegraph & Telephone, Toshiba, NEC, Fujitsu, Hitachi, and Sanyo.

All are deeply involved in researching and developing the high-end models. At the same time, the enormous latent demand in their business has made intermediate models a focus of the big computer manufacturers such as NEC, Hitachi, and Toshiba. NTT recently has come out with a high-performance device that boasts high-speed generation while maintaining the recognition level of conventional intermediate models.

In the area of low-end models, there is a rising demand from professional users who are fully aware of the limits of OCR functions. Low-end devices are being manufactured by NEC, Toshiba, Hitachi, and Sanyo. Although models equipped to recognize typed Kanji characters are making their way into this market, the performance level is low and the mainstream application continues to be alphanumeric data input.

Online character recognition technology is in the initial stages of commercialization, with the market on the order of 400 to 500 hundred million yen. Participants include Oki Electric, Tateishi Electric, NEC, and Matsushita.

Image recognition devices command a market on the order of 10 billion yen, mainly in the field of factory automation. There is a wider range of products as compared with voice and character recognition devices, with many products arriving from Western Europe and the U.S.

In addition to devices offering a high-precision recognition for use in the integrated circuit and printed-circuit board industries, the factory automation market segment is also seeing inspection-oriented devices for food products, pharmaceuticals, and springs or other components designed to replace the human eye in such work.

Nevertheless, application of robot vision has not occurred on a wide scale in processing and assembly applications because mechanical means and one-dimensional sensors

Focus on Fujitsu Ltd.

Fujitsu's first data-storage product was a magnetic drum, first introduced back in 1959. From this beginning, the company expanded its capability to where it now offers the broadest line of storage systems, including magnetic tape devices, magnetic disk drives, optical disk drives, mass storage systems, as well as the broadest line of hard-copy output devices including band printers, serial printers, and laser printers.

Fujitsu's policies for development are:

1. To be a total supplier who can provide peripherals for the complete needs of large super computer systems to the smallest personal computers.
2. Always challenge the state-of-the-art technology and strive to have unique advantages based on advanced technologies.
3. Close cooperation and integration of research, engineering development, and manufacturing in order to insure high quality and manufacturability.

As an example, in order to improve reliability, Fujitsu adopted a new sealed disk enclosure that avoided the contamination problems of previous systems. This led the company to adopt a unique 10½-inch disk diameter to reduce the heat generated compared with 14-inch models.

This new 10½-inch disk enclosure, the Eagle series, helped to establish a new industry standard for high-reliability disk drives. Also, the company was the first to adopt an 8-inch disk in its Swallow disk series, which offers both a compact design and higher performance.

Developing and manufacturing magnetic disk drives requires a large investment and expertise in a variety of disciplines, including mechanical design, precision machining, fluid dynamics, materials science (including chemical, metrology, lubrication materials), and electronics.

To be specific, high-density recording requires thin film media and low flying read-write head technology. High-speed data transfer requires thin film head and read-write head circuit technology. Also, high-speed data access and high track-density recording require precision, high-speed read-write head access mechanisms along with control technology.

Tokio Tatsuta, director

However, one of the very interesting technologies for the future is vertical recording. Fujitsu started research and development in this area about 10 years ago. Recently, it has made significant progress. Fujitsu believes that this technology will be used in actual products in the near future.

Fujitsu envisions future products being developed for two different applications, such as high-performance disk drive systems or high-capacity, space-saving disk drive systems with low cost-per-bit. In either case, look for the size of the disks to get smaller and smaller.

In the area of optical disks, the market will expand significantly when the easily erasable optical disk is available; currently available disks are either write-once versions that can't be reused or reusable models that require and erase cycle and a rewrite cycle.

Fujitsu plans to continue to provide various kinds of highly-reliable, high-performance data-storage products to its worldwide customer base and to provide good service to its customers.

are already established as production technology for positioning and other operations. In addition, image recognition devices are liable to lengthen the tact time, the time it takes for them to sense, considering the slow speeds at which they currently operate.

In the IC area, image recognition devices are finding use in inspection equipment for photomasks and patterning wafers. The major domestic manufacturer in this area is Laser Tech; the Hitachi Group and Toshiba are also offering products, but mainly on a captive basis.

The image recognition devices marketed for the production of printed-circuit boards are surface inspection systems. Such products are manufactured by Hitachi, Fujitsu, and other Japanese manufacturers. The rest of the market is dominated by imports. The printed-circuit board industry is flooded with small- and medium-sized manufacturers, whose needs for low prices create barrier to the domestic image recognition device manufacturers.

Fuji Electric is vigorously developing products for other types of factory automation systems. It has, for example, developed products that even encompass the construction of production lines in cooperation with the product technology departments of food and pharmaceutical manufacturers. While domestic venture corporations are pushing their recognition software, the keys to Fuji Electric's success are its accumulated store of hardware and other commercialized technology as well as its attention to customers after sales to insure that the production line is operating smoothly.

Other companies in this market are DAK Engineering and Creative Systems, both of which possess sophisticated recognition software, and NHK Spring, which has been developing spring inspectors for its own inhouse needs and now is now selling its system in the open market.

Unfulfilled demand

As can be seen, there is a huge latent demand for pattern recogntion technology products, which has thus far not been satisfied due to the fact that the current state of product technology does not meet user needs. It can be said that what has slowed commercialization has been expectations that pattern recognition devices could function as well as humans.

Obviously, it would be difficult for pattern recognition technology to surpass human levels of aural and visual perception. This does not alter the fact, however, that recognition through such devices is on a fairly sophisticated level. Aside from better performance, development should probably be weighted toward the design of new product features in existing fields, i.e., OCRs, which are now in wide use but restricted in function, factory automation systems supplemented by recognition functions with hardware technology, and high-tech toys, for which a primitive voice recognition is sufficient.

Although the market for pattern recognition products is expected to grow, the size of the market for each type of product will not be great due to the concurrent diversification, resulting in a micro-mass structure. This outlook is keeping the big electronic and electrical machinery manufacturers from entering the market. Instead, such a situation favors venture corporations or other companies outside those industries attempting to diversify their operations. It can also be observed that there are numerous business opportunities dormant in the pattern recognition industry, given the infancy of the market. Depending on the level of its commitment, a corporation could cultivate a great market.

TEST & MEASURMENT

After a sizeable decline, the market looks bright for the long term

Electrical test and measurement equipment is closely bound up with advances in, most importantly, the semiconductor industry, as well as in new media equipment, computers, information and communications, new materials, and the aerospace field. It is indispensible for improving the quality and productivity of manufacturing and helping to generate new technologies in these fields.

Over the ten-year period beginning in 1975, when the market actually declined in the wake of the first oil crisis, and ending in 1985, the market for test and measurement equipment grew at an annual rate averaging nearly 20%. However, 1986 production amounted to roughly 243 billion yen, representing a sizeable 28% decline from the previous year (see table). This may be attributed to a drop in demand as investment on plants and equipment in the private sector contracted with the semiconductor slump.

The picture brightened somewhat in 1987 as surpluses were shown by the business results of large US semiconductor manufacturers (one of the major yardsticks applied in the

PRODUCTION OF TEST AND MEASUREMENT EQUIPMENT	1983	1984	1985	1986
Electrical Measurement Equipment Total (In Million Yen)	**211,867**	**289,453**	**338,695**	**243,051**
Digital measurement equipment (Voltage, current, and power)	6,156	8,642	9,124	7,627
Oscilloscopes	22,285	26,028	27,723	19,522
FFT analyzers	N.A.	N.A.	1,857	1,700
Distortion measurement equipment	2,939	4,652	3,759	4,117
Logic analyzers	N.A.	N.A.	5,294	4,159
Microprocessor development equipment	N.A.	N.A.	9,454	9,566
IC and LSI test and measurement	43,608	79,086	103,293	50,817
Measurement systems for specific equipment	8,529	8,511	9,995	10,218
Optical measurement equipment (including equipment for construction)	N.A.	21,348	25,741	31,460

Source: Ministry of International Trade and Industry and Optoelectronics Industry and Technology Development Association

negotiations involving the adjustment of the yen and semiconductor trade friction). In addition, the Japanese semiconductor manufacturers readied for an increase in investment for new product development. The expectation is that last year's stagnation will therefore prove to be temporary and that the 1987 market will show a moderate recovery. The forecast is for a steady growth over the medium and long terms.

As one of the tools supporting technological development, the standing requirements for test and measurement equipment are the highest performance possible and the most advanced technology. The forerunning position of the US for innovative technology, particularly in the field of microelectronics, is reflected in the high share of the Japanese market occupied by products of such joint ventures as Sony-Tektronics and Yokogawa-Hewlett-Packard.

At the same time, the level of technology available from domestic manufacturers is rising along with increased productivity and quality. As a result, certain domestically produced equipment is already competitively equal to or even greater than the US counterpart on the world market. Competition in this market is intensifying with the influx of numerous corporations attracted by its potential for growth. Nevertheless, the demand appears to be clustering around those corporations with all-around technological capabilities as products grow larger in scale and are formed into systems.

One of the latest trends in test and measurement technology is the shift to intelligent systems that apply digital signal-processing technology. These are equipped with analog-to-digital converters, microprocessors, or memory chips for the storage, processing, or analysis of the test and measurement data of the main unit. In addition to enhancing test and measurement technology, these devices also contribute to size and weight reduction as well as improved operation and reliability.

Another major trend is building systems through the standardization of interfaces. Confronted with increasingly complicated subjects and swelling data loads, corporations are rapidly turning to Hewlett-Packard's General-Purpose Interface Bus (GPIB), which is a single standard interface for connecting equipment with peripherals or other test and measurement equipment. It has made possible the construction of various kinds of systems, including the connection of equipment from different manufacturers. Coupled with advances in the main processing unit, this is resulting in a consolidated operation from measurement to recording, ushering in automation, labor reduction, and a large cut in the time required for testing and measuring. As shown in the table, the following three fields have steadily registered growth even during periods of overall decline:

- Microprocessor Development Support Systems
- Measuring Systems for Data Acquisition
- Optical Measuring Devices

The development of equipment built around increasingly high-speed, sophisticated microprocessors requires software development on ever larger scales and with more efficient defect diagnostics. Some of the devices being supplied for this need are general

10 years ago you asked us for flat-panel displays, and we delivered.

"Great!" you said, "But can you make them...

development support units, logic analyzers, and in-circuit emulators. Such equipment is not used alone, but is designed for expansion into a system with computer-aided engineering or design systems and engineering work stations to create a broadly-based environment applicable for concept design, hardware design and development, and software development.

The 1986 production of microprocessor development support systems was more than double that of 1985 on a volume basis, indicating a surging demand, but stayed almost flat on a monetary basis, amounting to roughly 9.6 billion yen. The background of this situation was the exacerbation of competition as the handful of big manufacturers in this industry found themselves joined by roughly 40 others as well as the drop in the price of the equipment itself. The penetration of the 32-bit microprocessor is expected to stimulate a large demand.

Data acquisition measuring systems are dedicated systems for effective measurement of the performance of electroinc equipment and systems, with a wide-ranging use in the related research and development, manufacturing, and maintenance fields. The types include general measurement devices for communications and for audio-video equipment. The main representatives are network analyzers and protocol analyzers.

In 1986, the production of such systems topped the 10-billion yen mark. The main domestic manufacturers are Ando Electric, Anritsu, Matsushita Communication, and Shibasoku. The demand for these systems will presumably expand further with the inauguration of new communications businesses such as the Integrated Services Digital Network (ISDN) and automotive telephones and with the penetration of equipment for satellite broadcasting, high-definition television, and other new media.

The demand for optical measurement devices is steadily building along with the growth of the optical industry driven by optic communications and optical disk memories. Demand is growing for equipment for the installation and maintenance of systems applying optics and for the related mechanical and material research.

The production record for fiscal year 1986 is anticipated to show an amount in excess of 30 billion yen. The mainstays are optical loss measurement devices and optical time domain reflectometers, both of which are used for measuring the properties of optical power meters and optical fiber, as well as optical spectrum analyzers.

Reflecting the high level of Japanese optical technology, a sizeable share of the world market for this equipment is held by the domestic manufacturers Anritsu and Ando Electric, which were some of the first measurement device manufacturers to venture into this field. The market can be expected to register even stronger growth with the wider installation of optical local-area networks for intelligent buildings and the penetration of optical memory cards, laser printers, and laser sensors. This prospect has lead Advantest, Iwatsu Electric, Shimazu Seisakusho, Japan Radio and a number of others to enter the market.

In addition to the three areas outlined above, strong growth is also anticipated for digital multimeters, oscilloscopes, Fast Fourier Transform analyzers, and distortion measurement equipment, all of which would be endowed with high-performance capabilities through application of digital signal processing technology. Integrated circuit testers, which currently account for roughly 20% of the total test and measurement production total, are being developed to accommodate the high-speed, multipin LSI packages that house 32-bit microprocessors and application-specific ICs. Demand in this segment is consequently expected to expand also.

One of the crucial points for steady growth in today's industry is an accurate reading and analysis of substantive information to generate quality products. As such, the needs for test and measurement equipment offering more sophisticated performance and functions to support this effort are likely to only grow stronger in the years ahead.

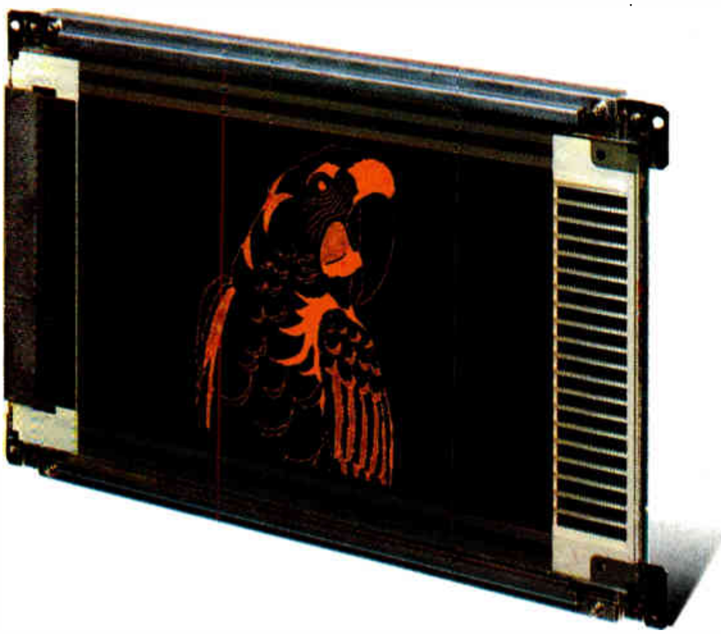
OPTICAL DISKS

Disk makers search for standardization

According to the Optoelectronics Industry and Technology Development Association, Japan's optoelectronics industry topped one trillion yen in 1986 (in terms of domestic production). One of the greatest forces behind this expansion was optical disk products such as compact disks (CD) and laser vision disks (LVD). As the market grows, standardization is becoming an issue.

The prospects for tremendous growth in the optical disk market have attracted numerous corportations to enter the market, creating a harsh, competitive business environment. The world's largest CD manufacturer, Sony, has plants in both Japan (CBS-Sony) and in the US (DADC in Indiana). Together these two plants turn out some 80 to 90 million CDs annually.

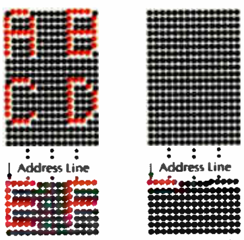
Sony is followed by PDO, the West German optical disk manufacturer established jointly by Philips and DuPont. The other major Japanese CD manufacturers include JVC, Sanyo



“We’re so glad you asked!”

Fujitsu presents the future of flat-panel displays.

In the beginning, all you had to do to make a good flat-panel display was to make it flat. Not any more. Today’s flat-panel displays are bigger, thinner, lighter, brighter. With higher resolution – and higher reliability.



New Fujitsu memory-type display All addressed lines light up simultaneously.

Conventional refresh-type display Only one line lights up at a time.

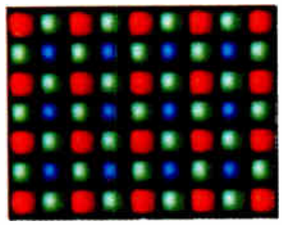
The brightest ideas in flat-panel technology, gas plasma discharge displays like Fujitsu’s FPF8050HFUG, give system designers some important extras, like high-contrast, flicker-free screens, with wide viewing angles.

Today Fujitsu’s plasma flat-panel displays can go almost anywhere a CRT can go. And do a lot a CRT can’t do. Which makes Fujitsu plasma displays the right choice for all kinds of applications: portable computers, electronic instruments, CNC control panels, automatic teller machines, just about any kind of information display.

They’re rugged, reliable, require very little space or power. And, unlike LCD displays, they come in lots of sizes, including extra large. In any size, Fujitsu plasma displays are easy to read under all kinds of lighting conditions.

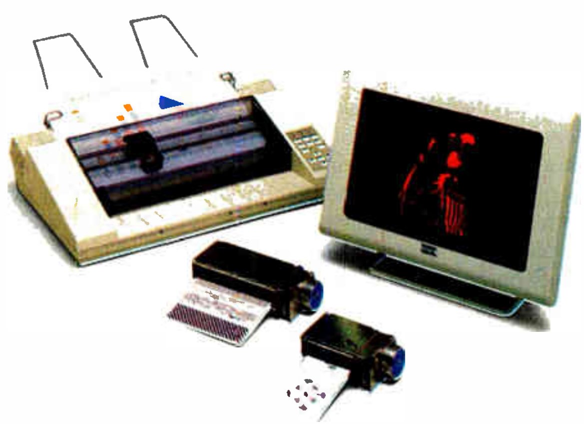
In fact, today’s plasma displays are so good, there’s really only one thing left to do to make them better.

And Fujitsu’s doing it. Naturally.



Our flat-panel display designers are leading the way in color plasma display engineering. Using new AC surface discharge technology and low power IC drivers, we’re on our way to color plasma displays that will give you the same high contrast, flicker-free viewing you can find today in our monochrome plasma displays.

R&D in new flat-panel display technologies is just one of the ways we’re working to give you the newest, highest quality components for your systems. From hybrid ICs to thermal printers and color plotters, from keyboards and displays to switches, relays, connectors, magnetic bubble memories and more, Fujitsu has the high quality components you need.



And if you don’t see what you need, just ask. Chances are it’s on its way.

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FUJITSU

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Electric, and Denon, in that order. Japanese manufacturers currently account for approximately 40% of the world CD production.

It is estimated that some 50% of Japan's 1986 CD production was exported overseas, implying a total production volume of roughly 100 million disks. While the hot topic up to 1986 was the stream of newcomers embarking on CD manufacturing even in Japan, this year the focus has shifted entirely to gaining production facilities overseas.

Strong yen

The reason, of course, is that the strength of the yen has made it increasingly difficult to supply CDs on an original-equipment manufacturer basis from Japan in the face of the burgeoning production in the US and Western Europe. Since the saturation point of the Japanese market for musical CDs is estimated at roughly 10 million disks, no substantial increase in production facilities and new market entrants can be expected in Japan. Acceptance of this fact is stimulating interest in the CD-ROM market.

While opportunities are drying up for prospective newcomers, those now in the CD manufacturing business are suffering from an erosion of profits due to the deterioration of exports as a result of the strong yen. The purchase of the manufacturing facilities of such corporations would provide a means for major corporations to enter this business.

The LVD has finally secured a position in Japan's audio-visual market, largely due to the efforts of Pioneer. The long-standing contest between the video high-density disk (VHD) and video disk formats appears to have been decided with the LVD's increasingly dominant position.

The position of optical LVDs is expected to be made even more secure with the emergence of the CD-visual (CD-V) models announced by Philips and Sony as single-type LVDs. Pioneer is also directing its attention to the CD-V, and has already come out with a player capable of handling all three types (LVD, CD-V, and CD-digital audio disk [DAD]).

Notable here are the activities of Matsushita Electric Industry, the parent of JVC, which developed the VHD. Matsushita continues to produce and sell the VHDs developed by JVC, but has announced its intention of pursuing the CD-V, with its introduction of optical video disk players a certainty. The dominance of the LVD would be absolutely assured if Matsushita decided to produce it.

Pioneer's LVD production of 12 million disks annually accounts for virtually the entire world total. Mitsubishi Plastics and Kuraray have also begun producing the LVD on an OEM basis, and Sony and Hitachi also have a limited LVD production capability.

The video disk market is confined almost totally to Japan; there have been virtually no sales to the US or Europe. Primarily two factors have attributed to the early take-off of this market in Japan.

Popularity of "karaoke." It would be impossible to overlook the influence of karaoke in the penetration of video disks in Japan. Meaning literarlly "empty orchestra," karaoke systems play a source (tape, CD, video disk, etc.) on which only the accompaniment of popular songs is recorded (not the vocal tracks) for customers to buy and sing along with. These systems can be found in about half of all drinking establishments in Japan. Use of video disks began in connection with karaoke, which still accounts for a considerabe percentage of the total.

The second factor is the undeveloped video tape rental business. Japanese VCR owners use their systems almost exclusively for time-shift recording; playing of purchased prerecorded video tapes is far less common than in other countries. As such, the video rental business is undeveloped compared to the US, for example.

While more rental shops have been springing up lately, the industry still harbors many illegitimate operations renting mainly pornographic video tapes and impeding the growth of the legitimate market. Given the lack of quality rental shops, the Japanese consumer is more likely to purchase than rent video tapes.

Contrary to expectations, the domestic video disk market failed to expand greatly last year. A full-fledged expansion of the business is likely to require a greater variety of CD-Vs and the establishment of the long-awaited video disk rental business.

The first product to apply write-once optical disks (WORM) was Toshiba's document storage system, which was unveiled in 1983. This product records document data on optical disks in the form of images. A 130-millimeter product has now joined the 300-mm disks.

Computer peripherals

Yet another market for write-once optical disks is as external memory for computers. The external memory of IBM's new PS/2 computer, for example, employs a 130-mm write-once optical disk, supplied by Matsushita on an OEM basis. The product represents the first adoption of the optical disk as a peripheral by a major computer supplier.

IBM's move has had a great impact on the industry, and has caused particular commotion in the International Standards Organization's (ISO) SC23 committee deliberating standardization of the 130-mm optical disk. This encompasses standardization of 130-mm WORM and erasable disks, but agreement on a single format for each is anticipated to require considerable time (especially for the former) due to the great number of companies involved in their development and the conflict of interests among them.

With marketing of products incorporating optical disks having already begun by various companies, most importantly IBM, the committee is afraid that the issue will be decided in the market before it can reach an agreement.

Five main types of WORM recording formats (and roughly ten types altogether) are already represented on the market. Differences in recording materials have ruled out compatibility among them. The products also differ in regard to medium life and the sensitivity of the recording layer.

The recording material with the most extensive record of use for optical disks is the terbium alloy used in the pit-forming format manufactured by Toshiba and Hitachi (with no physical compatibility between the two at this point). It is used for the optical disk document storage system, which debuted in 1983, and therefore has a record of roughly four years use.

According to Toshiba, there has not been a single case of user data being destroyed as a result of a failure of the recording medium. As others have pointed out, however, oxidation beginning from the exposed surface is a real danger, since the terbium alloy is exposed to the air after the formation of the pit.

Alloy formation

As far as medium life is concerned, the most effective recording format is the alloy formation-type medium manufactured by Sony. The recording layer actually consists of four thin-film layers. When irradiated by the laser, the layers fuse into an alloy. Sony claims a life of 20 years for this medium, as compared with the ten years for the media of other leading manufacturers.

Other media on the market include a type using the phase change of terbium alloys (Matsushita), a pit-forming type employing organic dye (Ricoh, Pioneer, and TDK), and a type using the change in the reflection factor corresponding with the change in recording layer shape (Plasmon and Kuraray).

Recording layer differences translate into different reflection factors, resulting in a loss of physical compatibility between media with different recording layers. The SC23 committee has consequently adopted a system by which optical disk cartridges are equipped with indentification holes enabling the drive to automatically detect the type of recording layer. Theorectically, it would be possible to manufacture a drive capable of reading all types of disks with this system. The actual results are being closely monitored.

Another major focus of the standardization committee is the question of the tracking method. The candidates are a sample servo method and a continuous servo method; the

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two are mutually incompatible. The former entails the use of a disk on which sample signals have been written in advance and perform the tracking while following the sample signals.

In the latter, the tracking is carried out through the course of the head in the groove. The selection also has repercussions for disk manufacturing processes and other aspects. The direction in standardization here is likely to become clearer sometime this autumn.

Compared with the WORM, with its plethora of recording formats, standardization of erasable disks is expected to proceed more smoothly. The magneto-optical disk form is in the mainstream.

The committee has already opened deliberations on the optical disk, and an agreement could be reached here even before WORM standardization is settled.

The pace of optical disk development has run its course for the time being, with sample shipments scheduled to begin later this year. The first are expected to come from Sony and Sharp.

The products from both companies employ the optical modulation format, in which the head must pass over the pit a total of three times in order to erase tracks on which data has already been written. In short, three phases are required: erase, write, and verify.

Writing therefore entails an extremely long latency time, a disadvantage in the competition with hard disks. In contrast to the 1-Mbyte/s for the 5.25-inch hard disk, the transfer rate for the 130-mm erasble optical disk is roughly 500 Kbytes/s during read and drops as low as half that rate during write operations.

For this reason, one of the higher priorities in optical disk development is an overwrite capability. Overwrite calls for either adoption of a magnetic field modulation format or use of a dual-layer disk, such as that recently announced by Nippon Kogaku. The

Focus on Nippon Electric Glass Co.

In the autumn of 1944, while Junichi Nagasaki was working at the Nippon Electric Company's research laboratory, NEC decided to produce glass for radio vacuum tubes. In 1949, the glass factory was spun off from NEC as an independent company under the corporate name of Nippon Electric Glass Co. Ltd. This new company began with 90 employees, who worked by using closed pots to melt the glass and hand-blowing to form it.

Junichi Nagasaki, director

In 1951, the company developed the Danner machine process to form glass tubing for fluorescent lamps, though closed pots were still used for melting the glass. Around that time, two competitors entered the market with more cost-efficient technologies imported from the US. The only way to compete was to enter into a technolgy exchange program with a superior glass maker. Therefore, discussions were immediately begun with Owens-Illinois and in 1958 an agreement was reached in the field of glass tubing, followed by an agreement in the field of cathode-ray-tube glass bulbs in 1965.

After concluding Nippon Electric Glass Co.'s first agreement with Owens-Illinois, the company had no investment money left to import the necessary equipment. Therefore, the company decided to design and produce all the equipment itself. This was the beginning of a company policy that is still in effect. An example of this is the press machine designed and built to produce the 43-inch color TV faceplates.

Another company policy is to avoid business segments in which others are already operating profitably. To create products, Nippon Electric Glass develops original technologies and applies them to commercial products, however small or unprofitable the business may look at first.

Glass ceramics is one field in which the company has concentrated its efforts for many years. Neoparies, the glass ceramics developed for building materials, has properties far superior to those of natural stone and has been used for exterior and interior walls and for columns. Glass ceramics for surgical and dental prostheses is another field that Nippon Electric Glass has given priority for development.

In addition to the glass tubing, TV glass bulbs, and glass ceramics, major Nippon Electric Glass products include glass fibers, a variety of glasses, including powdered glasses for integrated-circuit packages and other electronic applications, thin sheets for liquid-crystal displays, heat-resistant glass ceramics for microwave ovens, radiation shielding glass, and other blown and pressed glass products.

In short, Nippon Electric Glass will continue to develop glass products that meet the wide range of modern needs, while maintaining its established management policies.

magnetic field modulation format is being developed by KDD and Hitachi, among others. It appears to be comparatively conducive to development, since it affords room for the application of technology developed for rigid disks.

The format being developed by Nippon Kogaku, on the other hand, enables overwrite by optic modulation through the use of two recording layers with different curie points.

Erasure of previously recorded data is performed by an advance head made of a permanent magnet. Many problems still need to be solved here as well, such as a stable manufacturing of the dual-layer film and the question of countermeasures in the event the permanent magnet is demagnetized.

As far as these manufacturers are concerned, the optical disk technology acquired through the CD is an indispensable tool for entry into the field of industrial equipment, and especially computer peripherals; they are determined to solidify their position in the peripherals market this way.

Behind this activity lies the sudden downshift from steep to moderate growth in the home electrical/electronic industry as a whole and the continuing healthy performance of the computer industry backed by a strong domestic demand.

COMPONENTS

Companies move shops overseas

Due to the yen's recent rise against other currencies, Japan's electronics components industry has been forced to move production overseas, particularly to Southeast Asia. No other sector of the electronics industry has more experience with overseas production than the components sector. The components sector makes up 52% of Japan's electronics industry's total direct worldwide overseas investment. And Southeast Asia accounts for 64% of the component sector's total direct overseas investment from 1974 to 1984.

According to recent consolidated revenue and production figures of major Japanese electronics components manufacturers, 25% of all revenue is derived from overseas production. And 94% of overseas production is done in Southeast Asia. Taiwan and Korea account for 53% and 29%, respectively.

Overseas production is expected to accelerate in the coming years, not just to Southeast Asia, but to the US and Western Europe. Witness:

- TDK will produce ceramic capacitors in the US.
- The US will also be home to Taiyo Yuden, which will make

BREAKDOWN BY MARKET OF DOMESTIC COMPONENT SHIPMENTS			
Markets	**April–Sept 1984**	**April–Sept 1985**	**April–Sept 1986**
Consumer	64.9%	64.2%	63.1%
VCRs	21.3	21.9	20.0
Audio	19.1	17.2	17.5
TVs	15.4	16.3	14.2
Home appliances, etc.	9.2	9.8	11.3
Industrial	23.4	23.5	24.2
Computers and peripherals	7.7	8.5	8.2
Communication equipment	8.1	7.5	8.4
Office equipment	5.4	5.4	5.5
Test and measurement	2.2	2.1	2.1
Automotive	3.6	2.5	3.5
Industrial machinery, etc.	8.9	9.4	9.2

Source: Electronic Industries Association of Japan

chip capacitors.

- SMK will add mice to the list of products made in the US.
- Alps will expand US production of components and computers.
- Mitsumi will produce components for TVs and video cassette recorders in the US.
- Matsushita Electric Corp. will make power supplies for photocopiers in West Germany.
- Tabuchi will produce transformers and coils in Mexico.
- Murata will make thermistors and variable resistors in Brazil.

The markets for Japanese electronic components is steadily shifting from consumer electronics to information processing systems (such as computers, communication equipment, and office equipment). The proportion of the domestic shipments to major market segments for Japan's electronics components industry is shown in the table.

Chip components and surface-mount technology were originally developed for ease-of-use in automated assembly operations. But now, however, the technology is serving a different role: to produce densly packed printed-circuit boards. Various types of components are becoming available in chip form and usage of hybrid circuits is increasing.

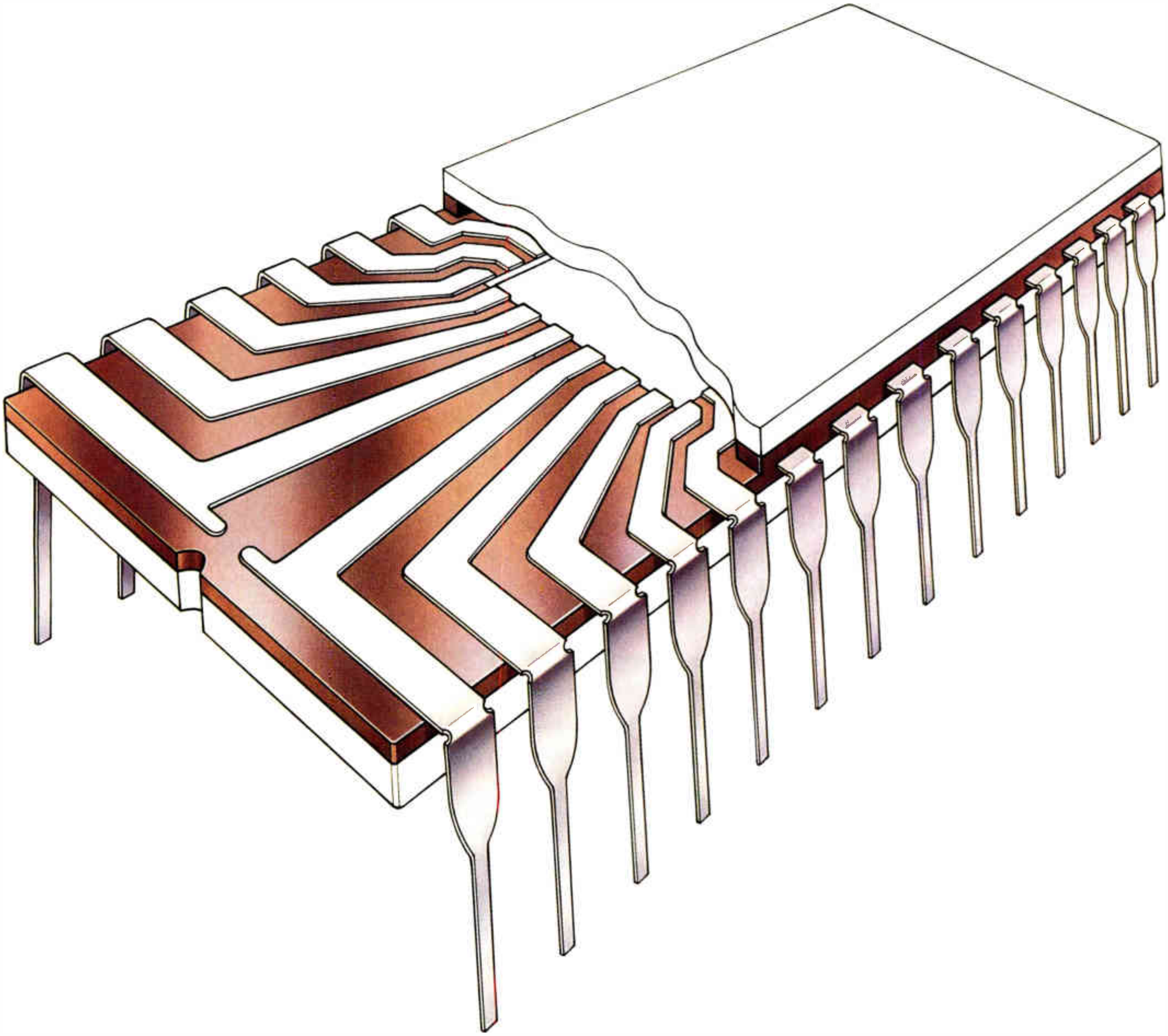
Fixed capacitors and resistors have been the traditional items to be put in surface-mountable devices, but now semi-variable capacitors and resistors, coils, transformers, filters, and quartz crystal oscillators are all produced in surface-mountable devices in addition to the conventional packages. And mechanical components such as switches, connectors, and relays are also becoming available in surface-mountable packages. Furthermore, chip components with multiple functions (such as capacitors and varistors) have been developed.

It has been difficult to house quartz crystal oscillators in surface-mountable packages since they are very sensitive to the environment, such as humidity and dust. The chip has to be kept airtight and its oscillating section has to be kept suspended in midair. Kinseki has developed surface mountable quartz oscillators using ceramic packages and sealing it with glass frit and polyimide-based conductive adhesive to meet the stringint requirements.

Surface-mountable relays have also been difficult to develop because their operating characteristics are affected by the heat stress of the soldering process. Omron has developed surface-mountable relays by adopting a new type of structure and new heat-resistant materials. Omron's development is also based on the finite element method applied to the relationship between stress and distortion within the temperature range of relay usage.

Optical devices are the next items that will be housed in surface-mountable packages. Matsushita Electronics (a subsidiary of Matsushita Electric) plans to produce photo interrupters, photo sensors, and enhanced versions of light-emitting diodes in the latter half of this year.

Development and standardization of surface-mountable devices has been vigorous. Already, 35% of capacitors, 25% of resistors, and 5% of fixed coils used today are surface-mountable versions. It is reported that surface-mountable devices presently account for 5% of the components used in Japanese assembly establishments (7% in industrial equipment and 3% in consumer equipment) and in five years the proportion will be skyrocket to about 40% (44% in industrial equipment and 35% in consumer equipment). ■



LS-2010 Composite Sealing Glass

Passes 270°C solder dipping test without preheating

Whether you're dealing with millions of ICs a month or just a few hundred, when it comes to sealing ceramic packages, the two most important numbers are the sealing temperature and flexural strength of the sealing glass: 430°C and 720kg/cm² would be excellent.

Where can you find numbers like these? At Nippon Electric Glass, the world's largest supplier of sealing glasses and manufacturer of LS-2010 composite sealing glass.

LS-2010 also provides higher hermeticity even after solder dipping at a temperature of 270°C, and does so without preheating.

More numbers to think about...a short, 10-minute sealing time...a low thermal expansion coefficient of 65 and a low dielectric constant of 12.5. Together they add up to more consistent quality from lot to lot, higher packaging yields, and superior dependability and performance.

Contact NEG today. We'll show you how our numbers can help improve your numbers—the ones regarding package reliability.

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Chicago Representative Office: 3158 Des Plaines Avenue, Suite 227, Des Plaines, Ilinois 60018. Phone: 312-297-7020 Fax: 312-390-0583

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NEW PRODUCTS

ONE-CHIP WAVEFORM GENERATOR CUTS PURCHASE PRICE IN HALF

HP ELIMINATES FREQUENCY DRIFT BY SWITCHING FROM ANALOG TO DIGITAL

By shunning analog-component technology and integrating waveform-synthesis functions onto a single chip, Hewlett-Packard Co. has cut the cost of arbitrary waveform generation in half and has immunized its new instrument to frequency drift arising from temperature and humidity changes.

The HP8904A Multifunction Synthesizer tests FM-radio receivers, touch-tone telephones, and a diverse assortment of other electronics gear by mixing digitally created waveforms. Unlike analog-component-based arbitrary waveform analyzers that require the user to calculate the waveform and store it in the instrument's memory, the 8904A generates its functions instantaneously. Modifications can be made on the fly.

SYNTHESIS. The HP8904A dynamically combines four standard waveforms plus dc and noise to create complex signals on the fly.

Implementing the instrument on a 100,000-transistor, 1.2-μm n-MOS digital-signal-processor chip eliminates the need for compensation circuits that prevent frequency drift in analog instruments. That saving, along with reduced costs for components and assembly, means the 8904A costs about half the price of analog signal generators with comparable capability.

SIGNAL BUILDER. The DSP orchestrates waveform generation through a programmable-logic-array state machine that controls the operation of a 24-bit counter and a 12-bit-wide read-only memory. The ROM contains pulse-code-modulated data needed to construct a sine wave. Driven by a master clock, the counter counts up to some value, overflows, and begins again. Each value in the counter addresses a location in the ROM. By reading the values from the register and applying them to a digital-to-analog converter, the PLA produces a sine wave. The output waveform's frequency is varied by changing the step size of the counter, which changes how fast the counter counts up.

By reading different values from the counter, the PLA can create different waveforms from the sine-wave data. To produce a triangular wave, for example, the PLA reads the counter value when it has counted one fourth of the way to completion, again at the halfway point, and again at the three-fourths point.

The instrument has up to four channels, each of which can generate four different waveforms—sine wave, square wave, triangle, and ramp. Noise and dc can also be generated; a separate ROM is used for the noise signal. Since all the standard signals are created from the same ROM, their relative phases are easily controlled relative to one another.

"The power of the new synthesizer is that it can vary the frequency, phase, and amplitude of every one of these four signals with digital precision," says Kenneth Thompson, product marketing manager at Hewlett-Packard.

"No other instrument has this flexibility. An analog instrument providing this same capability costs twice as much. Moreover, the instrument, because it is digital, does not drift, nor change with temperature," says Thompson.

The 8904A produces sine waves up to 600 KHz and triangle and square waves up to 20 KHz with less than –72 dB distortion. It has a frequency resolution of 0.1 Hz. In addition, the PLA can sum the outputs of all four channels together to produce a composite signal. Furthermore, three of the channels can be used to modulate the primary channel.

Modulation capability is useful in testing FM stereo receivers, for example, because the signal has four components: the 38-KHz subcarrier, a 19-KHz pilot tone, the sum of 38 KHz and the left plus right signal (that is, the monaural signal) and the sum of 38 KHz plus the left minus right channel (the stereo information).

All of these signals are summed, and the result is used to modulate the rf carrier signal. When the receiver demodulates all four of these signals, any phase or level errors occurring in the process result in a loss of channel separation—that is, one channel's signal leaks into another.

An instrument that generates a test signal to measure a receiver's ability to demodulate a stereo signal must have flatness beyond 53 KHz—the sum of the 38-KHz subcarrier and 15 KHz—the maximum audio signal used to modulate the subcarrier. It also must have no phase shift.

The 8904A has more than 65 dB of stereo separation, and the signals generated by the synthesizer exhibit a flatness of ±0.009 dB up to 100 KHz. Most special-purpose dedicated stereo composite generators have 55 dB of stereo separation from 500 Hz to 5 KHz, but the separation varies outside that band due to frequency drift. These testers have a signal flatness on the order of ±0.3 dB.

EASY TO USE. The user interface to the instrument is friendly thanks to an on-board Motorola Inc. 6809 microprocessor. Displaying prompting messages on a liquid-crystal display on the instrument control panel, the microprocessor leads a user through the setup procedure for creating a waveform. This contrasts with conventional methods of programming a separate computer to drive an arbitrary-waveform generator.

The basic HP8904A costs $2,600 and comes with one synthesizer, which produces a single output that is composed of the four basic waveforms, dc, and noise. It has all four synthesizers, but firmware for only one channel.

Option 1 costs $1,500 and provides the firmware for the remaining three synthesizers. Option 1 can also generate sequences of signals. This capability is useful in testing communications signalling circuits found in phone pagers. Option 1 can also be used to generate sequences of signals for testing equipment such as touch tone telephones.

Option 2 costs $1,200 and provides a second synthesizer and a second output: a digital-to-analog converter, an output amplifier, attenuator, and filters. With it, the 8904A can precisely vary the phase angle of each waveform from two channels—a useful capability when measuring differential amplifiers and servo systems. The instrument is available now. *–Jonah McLeod*

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Blvd., Palo Alto, Calif. 94303. [Circle 380]

FAULT SIMULATOR SPEEDS TEST DEVELOPMENT BY 70%

Developing fault-test programs for printed-circuit boards can be speeded up by 50% to 70% with a fault simulator from Computer Automation that tests multiple nodes concurrently, instead of by the conventional node-by-node approach.

The Sprint 3.0 simulator also can save customers as much as $400,000 over other systems and their associated hardware, claims the Irvine, Calif., company. This is because it was developed specifically for the test industry and does not include functions the test designers do not need. The company says tailoring a simulator to the test function allows it to be simpler, to create test programs faster, and to be less expensive.

Most simulators for developing printed-circuit-board test programs have not been updated since the 1970s and are really either design simulators with fault-simulation capability added, or fault simulators with design-simulation capability added. In either case, the test engineer has purchased more capability than he needs.

Sprint 3.0 boosts performance primarily with its concurrent algorithm. Previous-generation fault simulators introduced a single fault at one node in a model of the printed-circuit board and applied a test pattern at the input pins of the board. If an error pattern were detected at the output pins, the pattern would be saved; otherwise, it would be discarded. The process is repeated with the simulator introducing a fault at every node on the board and until a test pattern is found for every possible fault on the board.

POWERFUL. Sprint 3.0 handles 1,000 gates, 8,000 signals, and 32,000 faults.

A concurrent fault simulator, on the other hand, divides the model of the board into smaller sections. Then it introduces multiple faults into each section and applies patterns to the input pins. The Sprint 3.0 simulator introduces 600 faults at a time. By finding patterns that detect more than one fault and by performing the simulation on several nodes at once, the simulation time is decreased and the size of board that can be handled is increased.

Another strategy in reducing processing time is to simulate only activity that is meaningful for the fault being simulated. Sprint 3.0 ignores so-called "don't care" states in the logic of a circuit for a given test pattern.

TIME SAVER. Using Computer Automation's dedicated test simulator in combination with its test programming languages can reduce test development time as much as 50% to 70% over the time required by other simulators, says the company.

Sprint 3.0 and its predecessor product—Sprint—are the only state-of-the-art concurrent simulators available exclusively for the test market, claims the company.

Sprint 3.0 can handle 4,000 elements (four elements make a gate), 8,000 signals, 1,000 I/O pins, and 32,000 faults. That's a fourfold improvement over Sprint, which could handle only 1,000 elements, 2,000 signals, 250 I/O pins, and 8,000 faults.

While the original Sprint was written in assembly language, Sprint 3.0 has been completely rewritten in C and executes in the Unix operating system environment.

The new software is compatible with the older systems. One version of the Sprint 3.0—the Model I-200—costs $82,000. It comprises the simulator software and the Mighty Frame multiuser computer system from Convergent Technologies Inc. of Santa Clara, Calif.

A smaller version of the simulator, the Model I-210, costs $30,000. It comes with a Model I-100 Unix Workstation—a 32-bit Convergent computer based on Motorola Inc.'s 68010 microprocessor.

Besides the simulator software, the system comes with high-level compilers, the Majic Plus Programming language, and text editors.

Also included are device-modeling languages, such as ICDL (Integrated Circuit Description Language), and various library programs that allow storage and modfication of test programs. All products are available now.

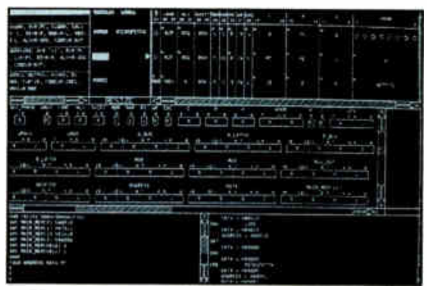
–Jonah McLeod

Computer Automation Inc., 2181 Du Pont Dr., Irvine, Calif. 92715.
Phone (714) 833-8830 [Circle 381]

MICROCODE SOFTWARE SPEEDS DEVELOPMENT

Trimeter Technologies Corp.'s Microcode Assistant speeds microcode development by unifying the coding, assembly, and verification functions into a single software package.

Unlike other microcode tools that represent code as strings of ASCII characters, Microcode Assistant uses a graphical interface on Apollo Computer Co. work stations.



Users create formats corresponding to the target system's architecture and give data fields symbolic names so they can easily be called to the screen, edited, and manipulated.

The software automatically creates object code while source code is being written, and object code can also be imported from other applications. The microcode program can be tested through a register-level hardware-simulation model.

Microcode Assistant is available now and costs $16,100.

Trimeter Technologies Corp., 200 Hightower Blvd., Pittsburgh, Pa. 15205.
Phone (412) 787-8630 [Circle 385]

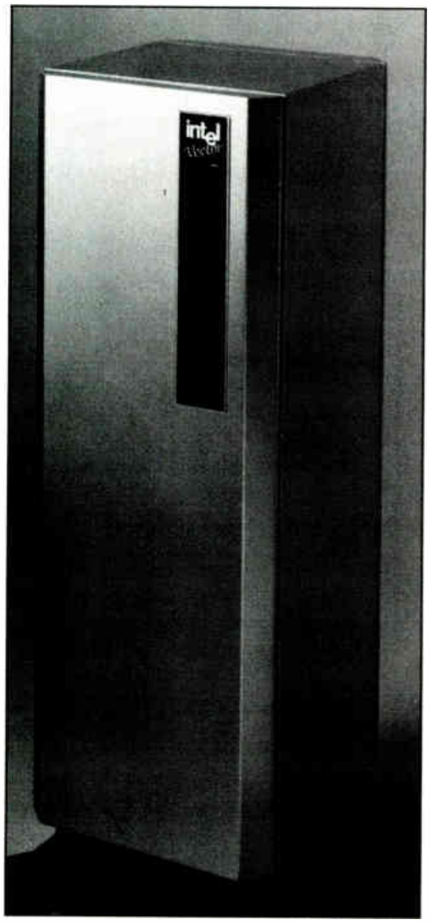
INTEL BOOSTS HYPERCUBE PERFORMANCE 10-FOLD

DIRECT ROUTING BETWEEN NODES CUTS DELAYS WHILE 80386 AND 80387 SPEED PROCESSING

The second generation of hypercube concurrent supercomputers from Intel Scientific Computers runs up to 10 times faster than its predecessors. The iPSC/2 boosts the power of the machine's node-based architecture by teaming Intel Corp. 80386 and 80387 processors with a new direct-connect message-routing technology.

Each node in the iPSC/2 has an 80386, an 80387 math coprocessor, and 1, 4, 8, or 16 Mbytes of 1-Mbit dynamic random access memory—plus a direct-connect router and a static RAM cache module, both of which are built in CMOS gate-array logic. Standard systems can have 32 to 128 nodes and a maximum memory of 1 gigabyte.

In systems configured for vector processing, a vector coprocessor is added to each node. The system can have from 16 to 64 such nodes. In its maximum configuration, the vector version can perform up to 1 billion floating point operations/s.



FAST. The iPSC/2 runs artificial intelligence programs four times faster than a Cray 1S.

Direct-connect routing plays an important role in improving performance. It reduces message delays by a factor of four and increases message speeds by a factor of 10.

In the hypercube interconnect scheme used in the first-generation iPSC machine, many messages had to pass through and be handled by a varying number of nodes, depending on how far across the cube the message was being sent. In the direct-connect routing scheme, messages are quickly and efficiently handled by the direct-connect router in each node and the interconnection system as if each node were directly connected to all other nodes.

The new routing and processors achieve a high measure of performance improvement in the iPSC/2. For example, a two-dimensional fast Fourier transform—one of the most difficult problems for hypercubes—is performed at a rate of 154 megaflops by a 32-node iPSC/2 VX (the vector version), which is 10 times faster than a first-generation iPSC-VX system. For artificial-intelligence applications, the standard Gabriel Triangle benchmark runs four times faster on the iPSC/2 than on a Cray 1S. This makes the iPSC/2 the fastest Lisp computer available.

UNIX-BASED. A version of AT&T Co.'s Unix forms the base operating software. The addition of a debugging program provides users with a software-development environment. A vectorizing compiler is available for the vector processors.

To speed the system's migration from research uses in academic institutions into engineering applications, the Beaverton, Ore., company has developed the Concurrent Workbench, a programming environment that gives multiple programmers access to the system simultaneously from a work-station network.

"The iPSC has come of age for real applications," says Justin Ratner, director of technology. "We have found that there is a market for cost-effective supercomputing. The biggest market is for speeding up simulation and modeling." The most common installation of the Intel Scientific Computers hypercube is as a computational server in a network of work stations and other computers.

Because of its relatively low cost, the machine can put Cray-class simulation resources into the hands of small engineering teams, according to the company. There are now 70 iPSC sites worldwide, spread among universities, government and defense establishments, industry, and application software companies. Simulation and modeling are the prevalent uses.

The new systems are software- and hardware-compatible with the old. Existing customers can upgrade the iPSC to the iPSC/2 and during a 90-day period will receive full credit for their original system purchase. The iPSC/2 systems will ship to beta-site customers at the end of October. Volume shipments will begin in January. The iPSC/2 systems are priced from $200,000 to $2,000,000.

–Tom Manuel

Intel Scientific Computers, Customer Response Dept., 15201 N. W. Greenbrier Pkwy., Beaverton, Ore. 97006.
Phone (503) 629-7629 [Circle 340]

PRINTER DOES HI-FI COLOR, 300 DOTS/IN.

The 4793D color printer from Tektronix Inc.'s Information Display Group combines 300-dots/in. resolution, a four-pass printing system, and sophisticated software to deliver color-matching performance in hard copy that captures the fidelity of high-end graphics computer systems.

Using a thermal-wax image process, the 4639D makes a separate pass for each of the three primary colors and a fourth pass for black to produce true blacks and deeper color saturation than other color printing techniques, according to the Wilsonville, Ore., company. The 4693D also has two monochrome printing modes, one for 256 shades of gray and one in black and white only.

To take full advantage of a palette of 16 million colors, Tektronix engineers developed a new dithering algorithm for mixing the colors to truly match the display colors on paper and transparencies. The company has applied for a patent on this algorithm.

To speed overall system performance, Tektronix engineers added a built-in im-

FAST REPEATER. The 4693D prints one copy in 90 s and subsequent copies in 60 s.

age processor to handle image preparation and relieve the work station of that task.

Throughput is enhanced by integrating a built-in frame buffer for images. The printer can be configured with one to three 4-Mbyte frame buffers so that the computer can send from one to three complete images to the printer in six seconds per image and then go about its other business—leaving the printer to process and print those images. The printer can process and print the first copy of an image in 90 s. Subsequent copies take just 60 s.

FOUR-WAY LINK. The image-processing and color conversions from display colors to printing colors are handled by a Motorola Corp. 68020 microprocessor. In addition to the buffer memory and processor, the system is equipped with a four-channel multiplexer so that up to four terminals, work stations, host computers, or persoanl computers can be connected to the printer simultaneously.

"The 4693D's high resolution and true color representation make it an excellent tool for designers, engineers, scientists, and other professionals in a broad range of applications such as mapping, medical imaging, technical data analysis, CAD/CAM and graphic arts," says Rick Lada, the product manager.

The 4693D can be driven by all Tektronix graphics terminals and work stations. Device drivers are also available for Sun Microsystems Inc. work stations and IBM Corp. Personal Computers AT and compatible PCs

In a standard configuration with one 4-Mbyte frame buffer and an 8-bit parallel port, the 4693D costs $7,995. It is available now. – *Tom Manuel*

Tektronix Inc., P.O. Box 1000, MS-63-447, Wilsonville, Ore. 97070.
Phone (800) 225-5434 [Circle 341]

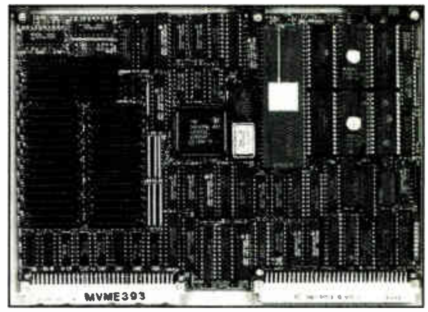
GRAPHICS BOARD CAN HANDLE 8 TERMINALS

A dual-processor VMEbus graphics controller board from Motorola Inc.'s Microcomputer Division handles high-resolution, bit-mapped displays for up to eight color monitors at a cost of $850 per channel.

The MVME393 uses Motorola's 68010 32-bit microprocessor for multitasking and windowing functions and Texas Instrument Inc.'s TMS34010 32-bit graphics processor for high-speed bit-mapped display functions.

The board offers a palette of 4,096 colors. It can draw 48 million pixels/s and render 64,000 vectors/s.

With the addition of the plug-in MVME794-2 eight-channel transition module, eight bit-mapped color displays can be driven at a resolution of 1,024 by 256 pixels by 4 bit planes.



The board supports GKS/CGI software from Nova Graphics Inc., Austin, Texas. The software is downloaded from the host to on-board memory.

Available in the third quarter, the board costs $3,295. The eight-channel transition module costs $3,195.

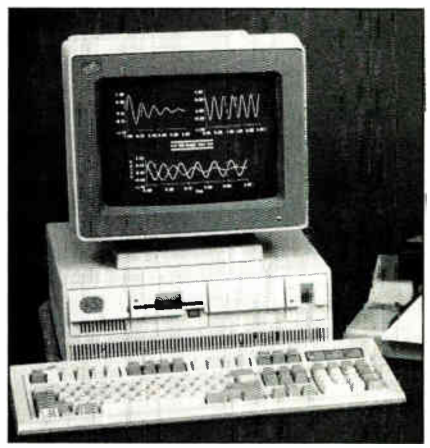
Motorola Microcomputer Division, Marcom Dept.-DW284, 2900 S. Diablo Way, Tempe, Ariz. 85282.
Phone (800) 556-1234 [Circle 345]

PROGRAM TURNS DATA INTO PS/2 GRAPHICS

Engineering data created in a variety of environments can be transferred to IBM Corp.'s Personal System/2 environment for graphical representation with the CEC-Graph software package from Capital Equipment Corp.

CEC-Graph converts virtually any data format to a PS/2-compatible format. A single command either displays the graph on IBM's Video Graphics Adapter or sends it to a plotter.

In addition to handling data files created on non-IBM computer systems, the software also supports conversion from



RS-232-C serial inputs and data acquisition from Hewlett-Packard Co.'s GP-IB instrument-bus format.

A window command lets more than one graph be displayed. Other features include automatic scaling and labeling and support for programs written in Basic, Pascal, C, and Fortran. Available now, CEC-Graph costs $95.

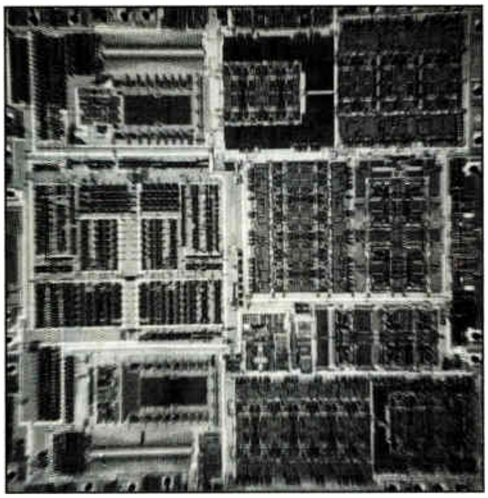
Capital Equipment Corp., 99 S. Bedford St., Suite 107, Burlington, Mass. 01803.
Phone (617) 273-1818 [Circle 346]

DSP INTERFACE CHIP CUTS COSTS IN HALF

TI'S 32040 REPLACES 6 TO 10 DISCRETE PARTS AND PERMITS ON-THE-FLY FEATURE PROGRAMMING

An analog-interface chip for digital signal processors cuts DSP interface implementation costs by about 50%, compared with board-level solutions using high-resolution converters, filters, and other discrete components.

Texas Instruments Inc.'s new TLC32040 interface chip replaces 6 to 10 parts. Just as important to DSP system designers, the chip also offers a wealth of programmable features not found in the integrated circuits that were originally developed for telecommunications applications but have been adapted to DSP systems as front-end and back-end peripherals.



STABLE. The 32040's converter has a 14-bit dynamic range and linearity over any 10-bit range.

QUICK CHANGE. On-chip control logic can be programmed on the fly to change sampling rates, filtering characteristics, or gain. In an asynchronous mode, the chip is able to run analog-to-digital and digital-to-analog conversions independent of each other.

Sampling rates can be programmed to handle 7.2, 8, 9.6, 14.4, and 19.2 KHz. The chip's converter has a 14-bit dynamic range and 10-bit ADC or DAC linearity over any 10-bit range.

The chip's bandpass switched-capacitor anti-aliasing input filter comprises seventh-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filtering and a fourth-order equalizer. The filter may be switched out of the signal path when filtering is not needed. The low-pass output filter is a seventh-order CC-type. The 67,000-mil^2 chip has four microprocessor-compatible modes for its serial port.

The 32040 can also synchronize on an incoming signal by incrementally adjusting analog-to-digital and digital-to-analog conversions. This is a useful feature in high-speed modems, which often must slow transmissions to compensate for poor-quality phone lines, says Mark Stropoli, strategic marketing engineer for linear IC products.

FAMILY LEADER. Fabricated in TI's 3-μm CMOS silicon-gate advanced LinCMOS technology, the 28-pin 32040 is the first in a family of DSP interface peripherals [*Electronics*, June 11, p. 23]. It is expected to be used primarily with TI's TMS320 signal processors in smart, high-speed modem systems and synthetic-speech applications. "About 5% of the 32040s are expected to serve other DSP applications in instrumentation and industrial control," says Stropoli.

In addition to conventional codec-filter combos, the 32040 will compete with AT&T Co.'s 7520 analog-interface peripheral chip. TI linear officials in Dallas say the 32040 contains more programmable features than AT&T's 7520, which is focused on voice-processing markets.

The 32040 interfaces directly to several TI TMS320 DSP hosts. With two external serial-to-parallel shift-register chips, the peripheral can be used with other DSP chips or first-in, first-out circuitry. It operates with a ±5-V analog power supply and a separate 5-V digital supply. Maximum power dissipation is 250 mW.

Commercial-grade parts, which operate over 0° to 70°C, cost $26 each in 100-piece quantities. Industrial-grade chips, which operate over –40° to 85° C, cost $27 each. *–J. Robert Lineback*

Texas Instruments Inc., Semiconductor Group, P. O. Box 809066, Dallas, Texas 75380-9066.
Phone (800) 232-3200, ext. 700 [Circle 360]

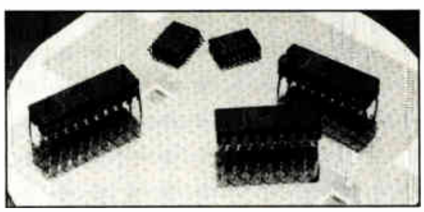
45-MHz FIFO MEMORIES USE 80% LESS POWER

Integrated Device Technology Inc.'s newest additions to its CMOS first-in, first-out memory family boast speeds of up to 45 MHz and power savings of up to 80% over comparable bipolar chips.

The IDT72401 and 72402 are pin- and function-compatible with the MMI67401 and 67402 bipolar parts from Monolithic Memories Inc., Santa Clara, Calif. The IDT72403 and 72404 are pin- and function-compatible with the same MMI parts but offer an additional output-enable pin.

The 72401 and 72403 are organized as 64 words by 4 bits, and the 72402 and 72404 as 64 words by 5 bits. All four parts come in 10-, 15-, 25-, 35-, and 45-MHz versions and have typical power consumptions of 200 mW.

Available now, the 72401 and 72403 cost $15 each, packaged in plastic DIPs and purchased in 100-unit quantities. The 72402 and 72404 in the same packages cost $23 each in lots of 100. Other packages are also available.



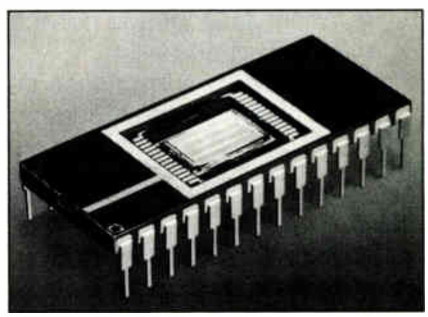
Integrated Device Technology, 3236 Scott Blvd., Santa Clara, Calif. 95052.
Phone (408) 727-6116 [Circle 365]

MILITARY SRAMS HAVE 100-ns ACCESS TIME

A 256-Kbit CMOS static random-access memory chip from GE/RCA Solid State Division targeting military uses offers a 120-ns maximum access time at 125° C.

The CDM62256C has a 100-ns access time at 25°C. Organized as 32,000 8-bit words, it also features a low-power standby mode that consumes 350 μA. Maximum operating current is 90 mA.

Designed for high-reliability tactical military hardware that requires dense memory systems capable of high speed, the device is specified across the full military temperature range of –55 to +125°C and operates from a single 4.5- to 5.5-V source. It conforms to the MIL-STD 833 Class B specification.



Available now packaged in a 28-pin heremetically sealed ceramic package, the chip costs $137.70 each in 1,000-unit quantities.

GE/RCA Solid State, P. O. Box 2900, Somerville, N.J. 08876. Phone (201) 685-6132

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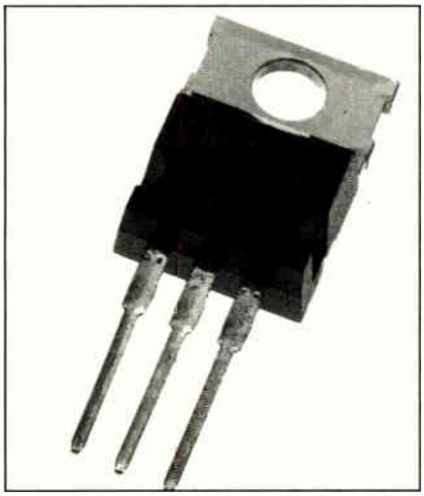
Fairchild Semiconductor Corp.'s FRP Series reverse-recovery rectifiers cover an operating range of 400 to 600 V and boast a maximum reverse recovery current of 5 A.

The 5-A rating is a key feature in reducing electromagnetic interference and voltage transients. Offering a maximum reverse recovery time of 75 ns, the rectifiers target applications in high-voltage switching power supplies, uninterruptible power supplies, inverters, and motor controls.



Two versions are offered. The 8A FRP-860 is encapsulated in a TO-220AC package. In the 16A FRP-1660CC version, two 8A dice are combined in a TO-220AB package. Both versions are available now. The 8A version costs $1.80 each in 1,000-unit purchases, and the 16A version is $2.50 each.

Fairchild Semiconductor Corp., 313 Fairchild Dr., Mountain View, Calif. 94039.
Phone (800) 554-4443 [Circle 367]

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A pair of high-speed sample-and-hold amplifiers from Datel Inc. have data-acquisition times as low as 8 ns and sampling frequencies up to 35 MHz.

Both bipolar parts are intended for use primarily with analog-to-digital converters. The SHM-361 offers 8-ns, 35-MHz operation and consumes 680 mW. The SHM-360 offers 14-ns, 18-MHz operation and consumes 420 mW.

The chips come in 24-in. DIP packages and target applications such as TV video encoding, radar pulse analysis, infrared imaging, and high-speed data acquisition.

Available now, the SHM-361 costs $26.80 in single-unit purchases; the SHM-360 is $18 each.

Datel Inc., 11 Cabot Blvd., Mansfield, Mass. 02048.
Phone (617) 339-9341 [Circle 368]

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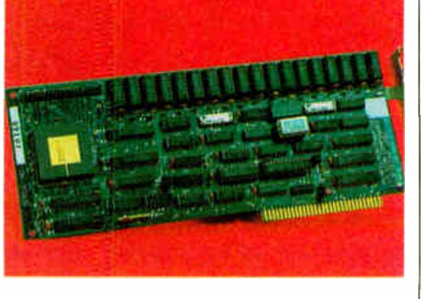

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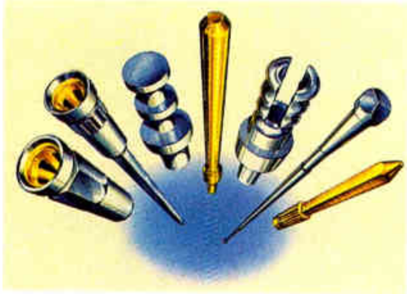

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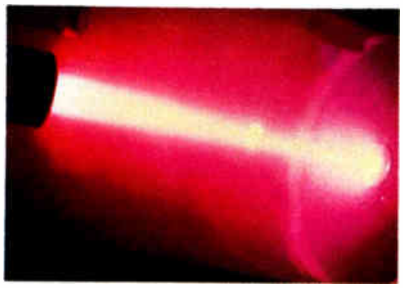

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ELECTRONICS WEEK

FLOPPY-DISK SALES: MORE FOR LESS

Consumers in the U.S. are buying more floppy disks, but they're spending a lot less for them. The International Tape/Disc Association says U.S. sales slipped 10% in 1986, from $476.8 million in 1985 to $427 million—even though unit shipments rose 41% during the same period. Leading the decline was the 5¼-in. market, which saw unit sales rise 40% while revenue slipped by 16% to $330 million from 1985's $392 million. Unit sales of 3½-in. disks, meanwhile, grew a whopping 140%, reaching 43.4 million units in 1986 from only 18.1 million a year earlier. Dollar volume, however, rose only 73%, because the average price of a 3½-in. floppy fell from $1.96 in 1985 to $1.42 in 1986.

FIRST-HALF PARTS SHIPMENTS UP 5%

Factory shipments of electronics equipment, components, and related products in the U.S. rose from $102.7 billion in the first half of 1986 to $107.9 billion during the same period in 1987—a gain of 5%, says the Electronic Industries Association. The greatest gains were made by components at 6.5%, and consumer electronics at 9.6%, while communications gear posted only a 4.5% rise. The Santa Clara, Calif.-based group reports that domestic sales of electronics products and services totaled $116.1 billion in the first half of 1987, a 4.5% increase over the $111.2 billion recorded last year. Orders were also up: $118.1 billion, compared with $113.7 billion a year ago.

MANAGEMENT BUYS MOTOROLA UNIT

In a leveraged buyout, the management of Motorola Display Systems has acquired that subsidiary of Motorola Inc. The new company thus formed, DisplayTEK, is the largest U.S supplier of CRT displays selling exclusively to original-equipment manufacturers. It inherits the staff and resources of the Motorola unit but will soon move company headquarters from Schaumburg, Ill., to Elgin, Ill. Manufacturing operations will continue at its Joplin, Mo., facility.

TEAM TO BUILD SMART 3½-in. DRIVE

Western Digital Corp. and Tandon Corp. are about to jointly manufacture and market 3½-in. intelligent Winchester disk drives. The new drives incorporate an interface controller into the drive, instead of having the controller that interfaces the drive and the central processing unit reside on a separate board in the computer. The drives will be incorporated into Tandon's personal computers and Western Digital's storage products.

SURPRISE—IBM IS A LOW-COST SUPPLIER

The Sierra Group, a Tempe, Ariz., research firm, has prepared a report on the real costs of computer systems, and it turns out that IBM Corp. doesn't make the most expensive systems in town. Sierra's second annual cost-of-ownership survey finds that IBM's long-term costs are lower than many of its competitors. The report is available from the Sierra Group for $225.

US WEST EXPORTS U.S. TECHNOLOGY

US West, one of the seven regional Bell operating companies, is expanding its Project Export program, which began in agricultural Nebraska, to the high-tech area in and around Portland, Ore. The program is aimed at identifying products, such as electronic components, subsystems, and software, that are produced in the target area and are ripe for export to Europe and the Far East. US West International will help the smaller U.S. firms with marketing, distribution, and even sales negotiations.

386-BASED SYSTEMS CAN DO X WINDOWS

Software that creates device-independent user interfaces for most major work stations will now be available for 386-based personal computers too. Apollo Computer Inc. has signed a joint development agreement with Graphic Software Systems Inc., a supplier of graphics for IBM DOS and OS/2 systems, in which GSS will adapt the Chelmsford, Mass., company's Open Dialogue software to 386-based PCs running Xenix. Based on the industry-standard X Windows, Open Dialogue currently runs on Apollo, Digital Equipment, and Sun systems.

HP, SONY TO BUILD DAT STORAGE UNITS

Hewlett-Packard Co. and Sony Corp. will jointly develop a range of computer data-storage products using digital audio tape. The two companies plan to develop cost-effective format-compatible products having fast transfer rates and a storage capacity of 1.2 gigabytes. The fast-search capability of DAT allows on-line inquiry with an average access time of only 20 seconds, and the small size of the tape cassettes makes them attractive for backup and archival use in computer systems.

INDUSTRY TRADE DEFICIT EASES

The trade deficit for the U.S. electronics industry eased greatly, with improvements showing up in computers, consumer, components, and instrumentation segments, reports the American Electronics Association, Santa Clara, Calif. Only in the communications segment did deficits grow in the first half of 1987 over the same period in 1986, spiraling from $900 million to $1.1 billion. In computers, a positive balance grew to $1.5 billion compared with $1.3 billion in 1986. The deficit in consumer products dropped to $4.8 billion from $5.3 billion in first-half 1986, and in components from $2.1 billion in 1986 to $1.9 billion this year. Instruments made slight gains, as the positive trade balance hit $1 billion this half, up from $900 million last year.

3COM SIGNS NEW TOKEN-RING PACT

Willemijn Holding BV has granted a full license to 3Com Corp. to use token-ring technology, expanding the terms of a two-year-old limited license. Now 3Com can produce, market, and distribute products based on the IEEE 802.5 token-ring standard without restriction. IBM Corp. also licenses the technology; it is limited to using token rings on its own machines. 3Com sells its token-ring products worldwide through dealers, value-added resellers, and computer manufacturers; the new deal permits dealers and customers to use 3Com products in both IBM and non-IBM environments.

NEW TANDEM WORK STATIONS DEBUT

A new family of seven MS-DOS work stations has been introduced by Tandem Computers Inc., Cupertino, Calif. The PSX/300 and PSX/200 series machines can function as stand-alone units or as fully integrated terminals for Tandem NonStop and LNX systems. They range from a high-performance Intel 80386-based work station with a 70-Mbyte hard disk to a low-cost, diskless work station based on the 80286 that is connected to a local-area network. The machines' common chassis measures 15 in. wide, 16 in. deep, and 6 in. tall. Prices range from $1,195 to $5,695.

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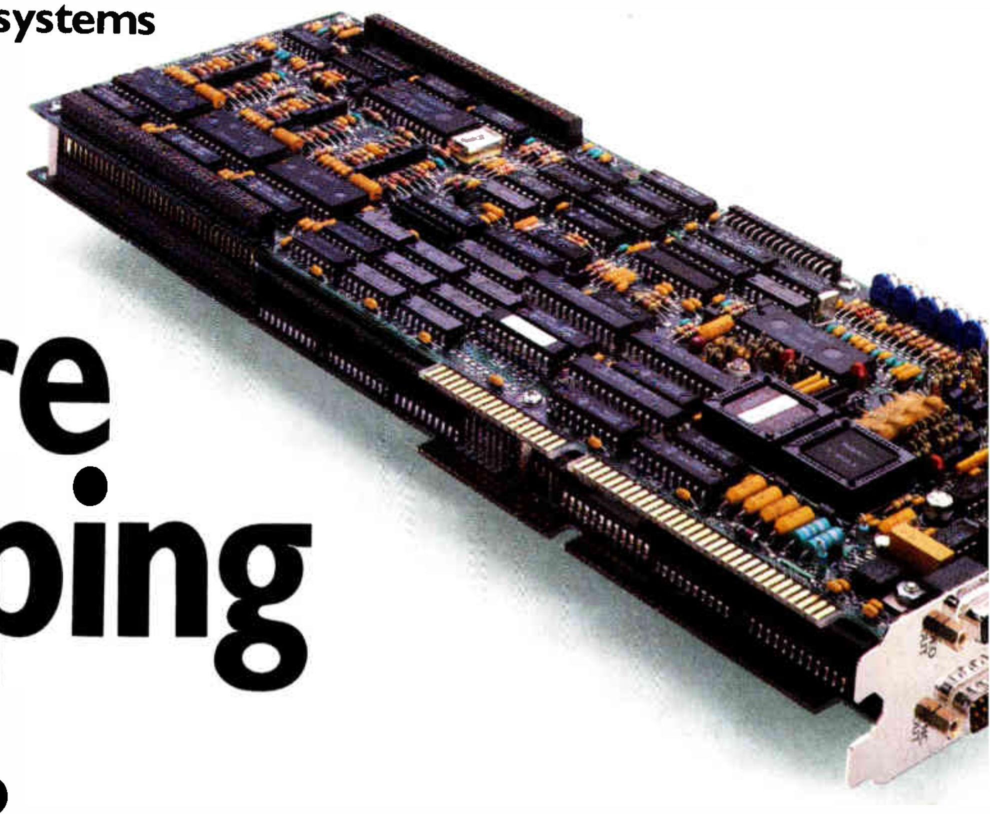

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