SPECIAL REPORT: THE MOVE TO ONE-CHIP LINEAR SYSTEMS/70

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A McGRAW-HILL PUBLICATION SIX DOLLARS MAY 28, 1987

Electronics

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While others talked "industry standard" only Mentor Graphics became one.

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EL 5/28/87

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We'd also like to suggest comparing us to the competition. But there doesn't seem to be any.

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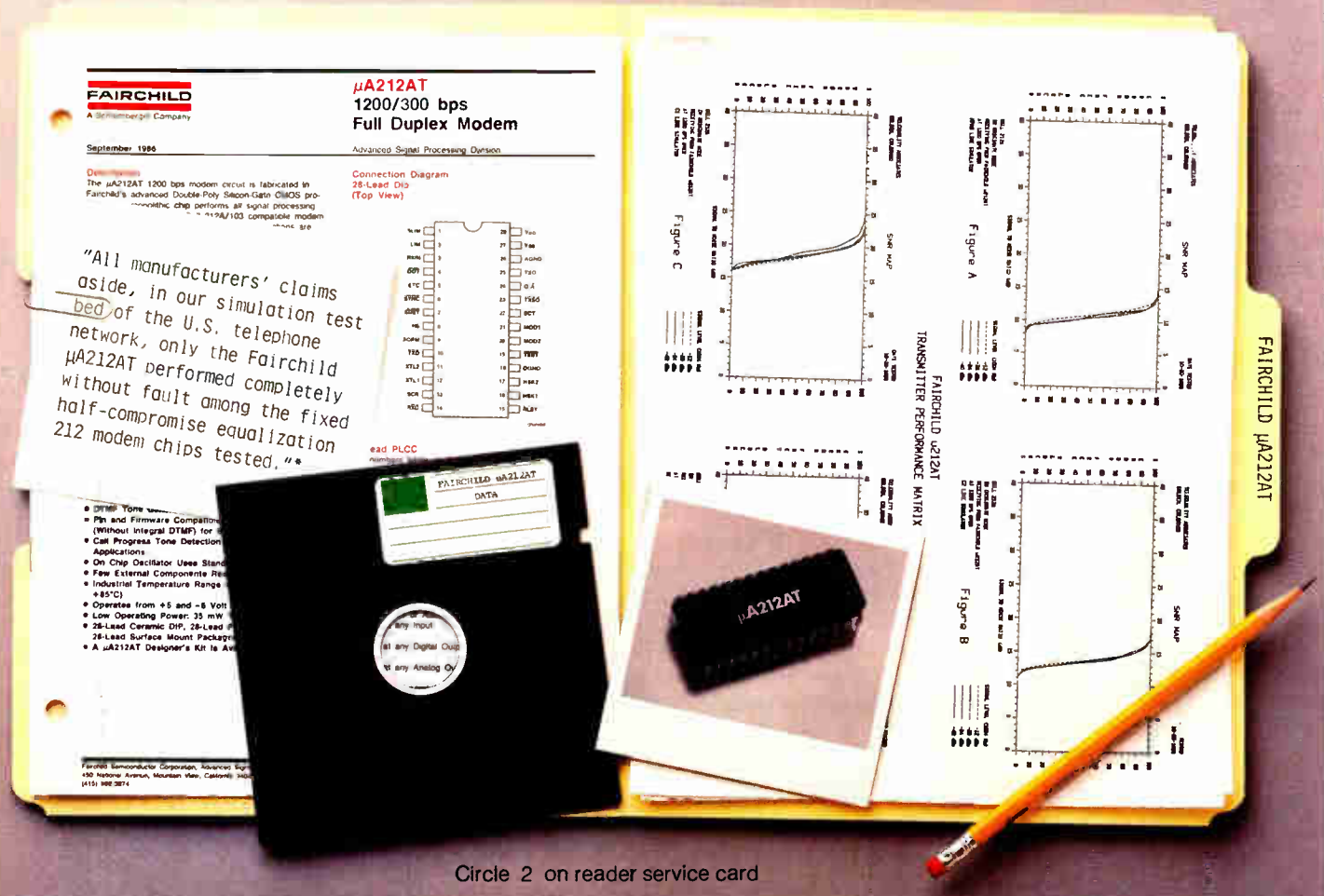

Circle 2 on reader service card

Electronics

PUBLISHER'S LETTER

To stay on top in our highly competitive business, *Electronics*' department editors not only have to keep up with the latest technological developments, but they must know which companies are working on them. Then their job is to track the work and, when the time is ripe, talk with the companies to develop articles describing it.

MANUEL: Keeping in touch and doing thorough groundwork.

Compared with the way we turn around on a dime to cover major, late-breaking news stories—we described in the last issue how we do that in mere days—that watch-and-wait process with which we originate the feature articles that appear in the center of the magazine is downright leisurely. That, of course, is a plus: with our international circulation, we are constantly reminded that our decisions about important developments carry a great deal of weight. We don't want to force our editors to make split-second judgments of the significance of technologies that still may be in the lab. Also, often a series of related developments lends itself to a broad look at what's new.

In this issue, the cover roundup on flat-panel displays is a case in point. The four-story package, shepherded into print by associate managing editor Tom Manuel, who also wrote the overview on p. 55, got its start last September.

"Last September, we saw a demonstration of Planar Systems Inc.'s two-color electroluminescent display," recalls Tom, "and found it quite impressive. "But the company told us it was working on a three-color version, so we decided to wait until that was ready." The wait was fruitful; the story on the three-color EL display is on p. 63.

But that wasn't all. "A couple of months later, along came Tektronix with a prototype of its liquid-crystal display, one with high contrast and a wide viewing angle. It looked so good that it didn't look like an LCD," says Tom. "We knew immediately that we had a good one and that we wanted to keep track of how Tek was doing so that we could run an article when the display was out of the prototype stage." The article on that development is on p. 61.

Then, early in the year, we learned that Cherry was going to culminate a three-year design effort by introducing its EL display—but one that uses thick rather than thin film (p. 58). Says Tom, "That was the key to our timing: with the Society for Information Display conference coming up in New Orleans in the middle of May, we had a natural package of articles about flat panels. In this case, it was the Cherry development that was the charm. And that's particularly true, because it has all the elements that make for good technical journalism: it describes something new, useful, and timely."

The lesson to be learned here is, as Tom puts it, "When you keep in touch, as *Electronics* does, and prepare the groundwork well in advance of the projected publication date, packages like the one in this issue just seem to fall into place." It's all a question of knowing just what to wait for and how long to wait, and we have as much experience doing that as we have in turning around fast on breaking stories.

Laurence Altman

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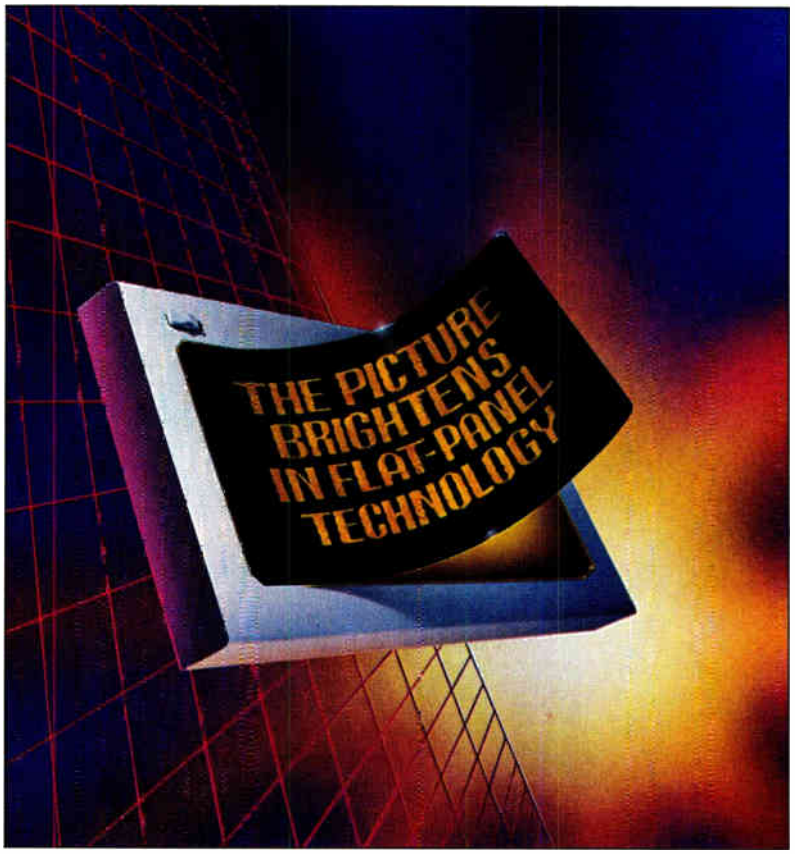

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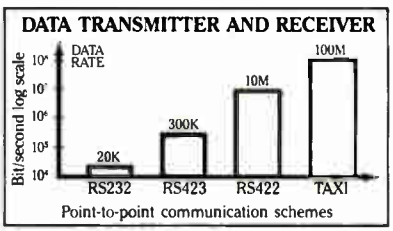

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Circle 7 on reader service card

FYI

Admits one chip maker: 'I don't know if I'll send my best production engineers to Sematech . . . I also don't know if I'll share my proprietary advances with it'

We still have many of the worries about the semiconductor manufacturing consortium that we had in January [*Electronics*, Jan. 22, 1987, p. 8], but now it looks like the co-op has a better chance of making it (see p. 33). To our surprise, U.S. chip makers sat down and cooperated: industry leaders bit the bullet, reached a consensus, and put a complex package together. We were impressed by months of hard work. Chip makers have also decided just what the co-op is going to do, what companies can join, what products it will make, and how many to make. So far, it's been mostly the big producers that have been making these decisions. What they did wasn't easy, but the next part is even harder: they've got to get the small semiconductor makers to join and pay 1% of their sales, as well as get equipment makers behind the consortium.

The chip makers also have to make sure the consortium will do what it's supposed to do: transfer technology. Success depends on chip-making technology being handed off to commercial houses by their best engineers, who will have to go to work at Sematech. But, admits one senior executive at a big chip maker: "I don't know if I'll send my best production engineers. I also don't know if I'll share with it the proprietary advances in manufacturing we've achieved at our company."

The federal connection still worries people, but progress is being made. "I think Congress now recognizes the hazards of tying strings to any money appropriated to Sematech, and it's trying to set up something to get around that problem," says Regis McKenna, a Silicon Valley consultant who has briefed Congress on the subject. "One way might be for Congress to set up an advisory board to oversee and direct Sematech."

Washington is still going to be a hard sell, especially since chip makers want Uncle Sam to kick in $125 million annually to save their industry. Best estimates now are that the co-op will get no more than $50 million from the government in the first year. *The New York Times* also is cool to the industry's pitch: "The lesson here is caution. . . panic over Japanese successes is not a reasonable basis for public policy. Congress should turn a skeptical ear to pleas for direct subsidies." As usual, the *Times* showed little understanding of chip makers' problems, or how not setting up Sematech would affect the nation's future. As Harris Semiconductor's Jon Cornell puts it: "Sematech may have its problems, but our only choice as an industry is to try it, or die."

ROBERT W. HENKEL

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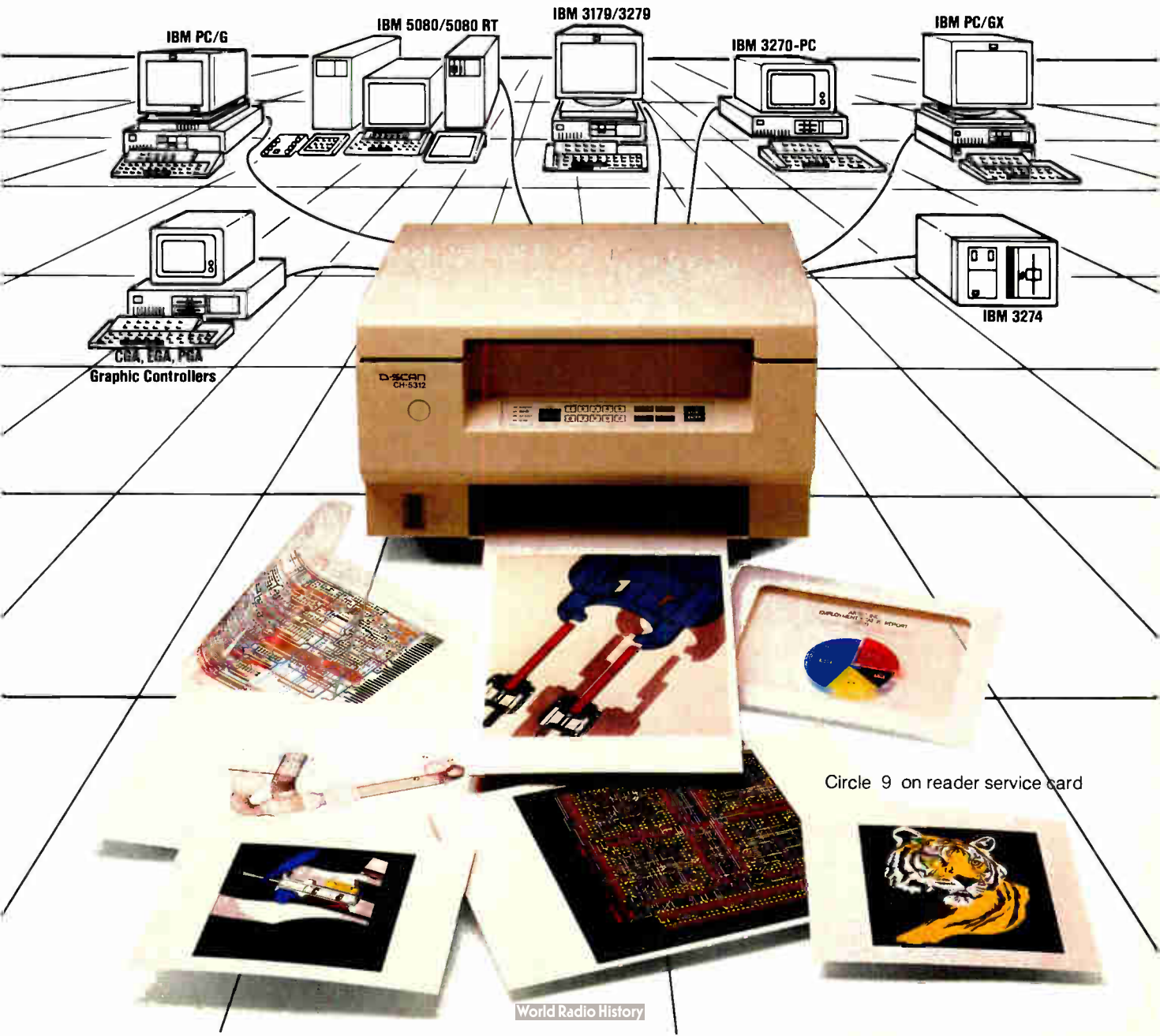

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Max. Clock Freq. (typ) J/K F-F (C_L = 15pF)	60MHz	45MHz	20MHz	2MHz
Quiescent Power Diss. (typ) (GATE)	0.01 μW	8mW	0.01 μW	0.01 μW
Noise Margin $V_{IH(min)}/V_{IL(max)}$	3.5V/1.5V	2.0V/0.8V	4.0V/1.0V	3.5V/1.5V
Output Current I_{OH}I(min)/I_{OL} (min)	4mA/4mA	0.4mA/4mA	0.36mA/ 0.8mA	0.12mA/ 0.36mA
Op. Volt. Range	2-6V	4.75-5.25V	2-8V	3-18V
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LETTERS

Exception to the rule

To the editor: I am writing to you in regard to the excellent article in your semiconductor special issue [*Electronics*, April 2, 1987, p. 62].

We take exception, though, to being listed as a standard integrated-circuit maker instead of as a vertically integrated company. Your note at the bottom of the charts explains that where a company fits in more than one category, it is placed under the heading of its most important business.

In the case of Motorola, our largest business is the communications sector (FM two-way radios, pagers, and other electronic communications systems). Our Semiconductor Products Sector is our second largest organization, accounting for 31% of our 1986 sales. Several other businesses (automotive and industrial electronics, computer systems, cellular radiotelephones, government electronics, and data communications) make up another one third of the company.

Charles A. Sengstock Jr.
Director, Corporate Public Relations
Motorola Inc.
Schaumberg, Ill.

First and foremost??

To the editor: The recent news item in which Toshiba proclaimed itself the first company to apply biCMOS technology to 74-type logic [*Electronics*, March 19, 1987, p. 53] is mistaken.

Texas Instruments announced its own biCMOS family in October 1986 and has been offering actual devices in sample quantities since that time. This family is specification-compatible with the 74F logic family, except that it consumes less than 5 mA of current when disabled and one third the power of the 74F counterparts in the enable mode.

These devices are perfect for interfacing with high-drive (IOL=64 mA) backplanes such as the PC-Bus, Multibus II, and VMEbus. We have offered sample quantities of some members of the 29800 series to date. The '245 octal transceiver will be offered in sample quantities in April. The balance of the family will be offered as samples by July, with production by September.

Robert L. Bailey
Logic Strategic Marketing Manager
Texas Instruments Inc.
Dallas, Texas

Shifting sites

Correction: *A story on Lasarray Corp. [Electronics, April 2, 1987, p. 72] said the company is building a new facility in Scotts Valley, Calif. Lasarray is actually moving to new headquarters in Irvine, Calif.*

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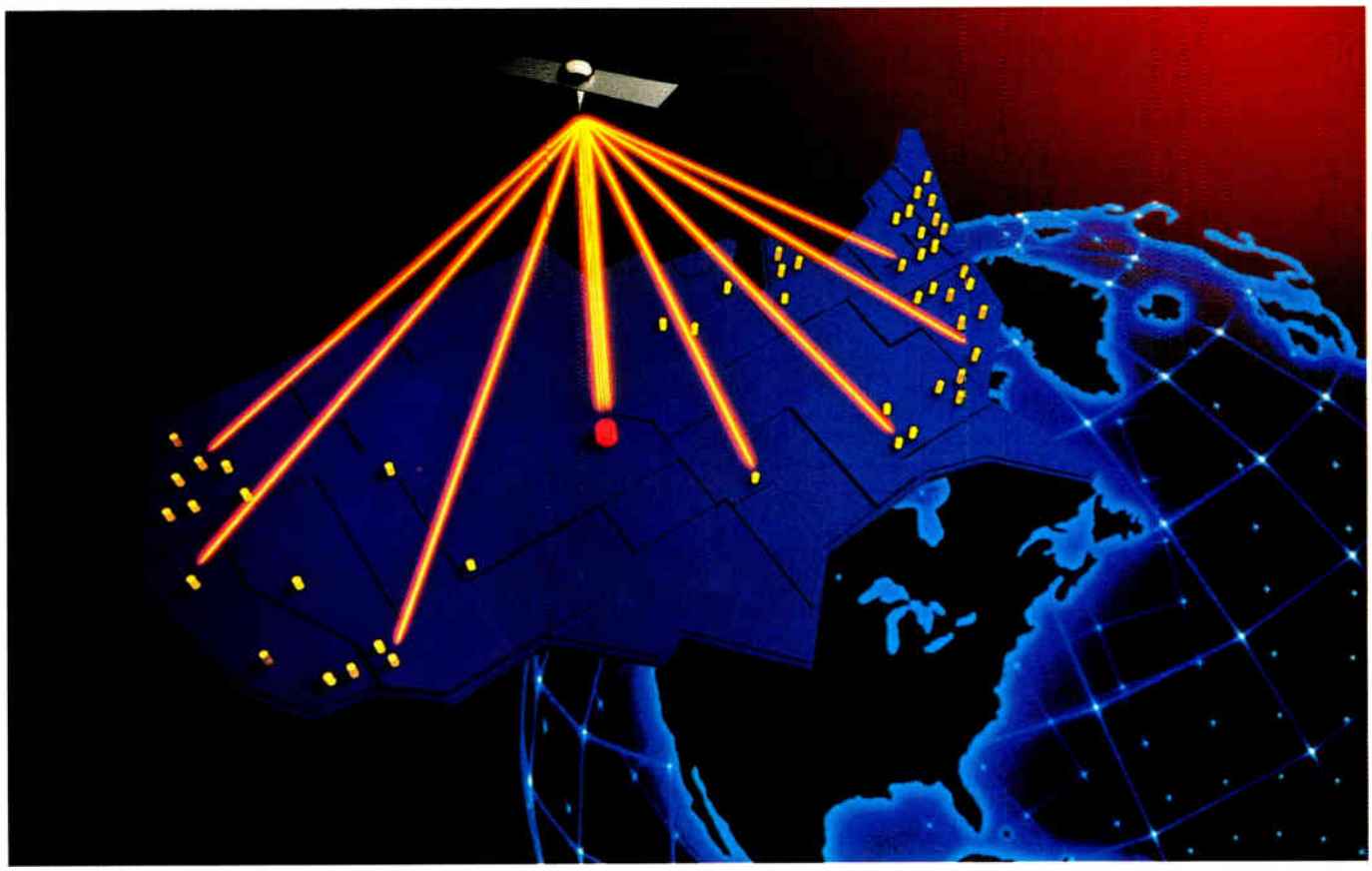

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Our advanced mini earth station networking system "NEXTAR" offers unprecedented flexibility for transaction-oriented businesses typically using POS, ECR and ATM systems.

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The mini earth station, a 1.2 or 1.8m antenna with an integral RF package and compact indoor unit, takes less than a workday to install. Site selection and licensing are also simplified with the Ku-band. The central hub station with comprehensive monitoring, control and diagnostic capabilities can be located adjacent to a data center or at a shared site.

The NEXTAR network can be custom-tailored to a user's exacting needs—data rates from 75bps to 56Kbps plus voice and video capability. It eliminates the wasted transmission capacity and high cost of traditional alternatives.

C&C
Computers and Communications

NUMBER 137

1.3-MICRON OEICs FOR GIGA-BIT LINKS.

Scientists at the NEC Optoelectronics Research Laboratory have successfully tested the world's first optoelectronic ICs to operate in the 1.3μm band at data rates of 1.2Gbps.

The optical transmitter and receiver chip pair set records of a 12-km communication at 1.2Gbps with a 7.7dB margin, and 22-km transmission at 565Mbps with a 9.9dB margin in the experiment using a single-mode fiber.

The new light-emitting chip incorporates a 1.3μm DC-PBH (double-channel planar buried heterostructure) laser diode and three InGaAsP/InP hetero-junction bipolar transistors on the same InP substrate. Modulation up to 2Gbps is possible in NRZ mode. A peak output of 20mW was marked at 1Gbps.

The optical receiver integrates a PIN photo diode and three low-noise InGaAsP junction FETs on a single chip for sensitivity of -14dBm at 1.2Gbps.

NEC's new OEIC pair will be the ideal workhorse in medium- or short-distance ultra-high speed links including LANs, local subscriber loops and interconnections of computers and peripherals because it promises much lower cost and smaller size than prevalent discrete devices.

These OEIC devices will reach the market within a few years.

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Today there are NEAX61 switches in service at 1,002 exchanges in 37 nations—more than 5 million equivalent subscriber lines in all. With recent orders from New Zealand (400,000 lines), Hong Kong (600,000 lines) and Venezuela (330,000 lines) the aggregate orders received now exceeds 10 million equivalent subscriber lines.

NEC OPTICAL REPEATERS GO TRANSPACIFIC AND SUBMARINE.

The trend in transoceanic submarine cable systems is undeniably "optical". The use of fiber optic transmission technology increases capacity, extends repeater span and ensures compatibility with land-based digital networks.

Under a contract awarded by KDD, Japan's leading international telecommunications network, NEC is manufacturing optical submersible repeaters and optical terminal equipment for the third Trans-Pacific Cable (TPC-3) which will link Hawaii and Japan with a branch to Guam.

The TPC-3, to be completed in 1988 and owned by 22 telephone operating companies in 10 countries, will have two 280Mbps systems, offering a total capacity equivalent to 7,560 telephone channels—a dramatic increase from 138 channels with TPC-1 and 845 channels with TPC-2.

Incorporating our 1.3μm DC-PBH (double-channel planar buried heterostructure) laser diodes and newly-developed high-speed monolithic ICs the optical repeaters are designed to maintain high reliability on the ocean floor at a depth up to 8,000 meters.

NEC

HOW CATRAMBONE AIMS TO WIN IN POWER HYBRIDS

LEOMINSTER, MASS.

John Catrambone maintains that few people in the electronics business fully understand the world of power-hybrid devices. They may grasp the intricacies of designing and manufacturing power hybrids for power-management and supply functions in military and industrial applications. But not many are good at packaging, and even fewer understand that one of the key ingredients that flunks aspiring suppliers of power hybrids is customer service.

Catrambone, 46, is president and cofounder of Omnirel Corp., a young Leominster, Mass., company that provides power hybrids operating at a few amperes at anywhere from 5 W to hundreds of watts. A major goal at Omnirel is to provide customers what they ask for on schedule, which Catrambone agrees is pretty much like being in favor of motherhood. "But that's one of the biggest needs today—servicing the customer," he says.

"Customers keep telling us they try to buy power devices, but nobody can deliver. Packaging is a big part of the failures, but for various reasons, the customer doesn't get the parts. The ability to do what you say you'll do is critical. I think the electronics industry has lost sight of that fact."

LESSONS. Catrambone and his partner, Terrence Heng, learned the needs of power hybrid users well, mainly at Unitrode Corp., the Lexington, Mass., manufacturer of power semiconductors. Catrambone most recently was vice president for marketing and sales at Unitrode; Heng was director of research, development, and engineering.

The motivation to start Omnirel came from Catrambone's realization over the years of the special needs of power-hybrid users. "We continued to see needs for sophisticated, high-frequency devices that could handle power—needs that weren't being met. "Our customers' needs stem from the continual push for more functions in less space in all applications, including power," Catrambone says.

Catrambone maintains that Omnirel "understands the customers' power requirements, has a facility designed for power [meeting MIL STD 1772, which covers facility cleanliness and documentation], and the technical expertise to design power—including packaging, which is critical." In fact, Omnirel is working closely with a packaging house (Catrambone won't say which one) to develop innovative, hermetically sealed packages that are also cost-effective.

"We're also working closely with semiconductor manufacturers to help design and then second-source them in power devices so that we have access to the latest devices at favorable prices, can second-source each other's products, and can identify potential device needs," Catrambone says. Omnirel has such a deal with "a major MOS FET manufacturer based in northern California," Catrambone says. Siliconix Inc. fits the description, although Catrambone just smiles at mention of the name.

The company, which will be two years old in June, has received orders worth "hundreds of thousands" of dollars for power-management devices from an impressive list of military systems suppliers that includes Honeywell, Litton, Northrop, and the U.S. Navy's Weapons Center at China Lake, Calif. Catrambone expects 70% of Omnirel's business to come from military contractors; the remainder will result from sales to industrial power users in medical electronics, portable instruments, industrial control systems, and portable data-processing and peripheral equipment.

Omnirel will have revenues "in the multiple millions" in this, its first fiscal year of full operation, he says. The business plan calls for revenues of $35 million in the fourth year, or calendar year 1990. That may seem an overly ambitious objective. But Catrambone disagrees: because of early customer acceptance of Omnirel's products, he says that he is confident of meeting the goals of that plan. *–Larry Curran*

CATRAMBONE: "The ability to do what you say you'll do is critical."

TEXAS INSTRUMENTS REPORTS ON

GRAPHICS

IN THE ERA OF

MegaChip TECHNOLOGIES

Graphics in the Era of MegaChip Technologies:

New Texas Instruments lets you program circles

plus filled polygons, spline curves, antialiased lines,

From PC displays to laser printers, the flexibility of TI's TMS34010 processor delivers the leading-edge performance you need today and to stay out in front tomorrow.

In TI's TMS34010 Graphics System Processor, you have a new and better graphics-design approach: The first high-performance, 32-bit CMOS microprocessor optimized for graphics applications.

The 34010 can execute all functions needed by graphics operating environments; hard-wired coprocessors can only execute a small part.

32-bit graphics processor around competition...

text, and more.

"Because the 34010 is programmable, it is in a league all its own."
Jim Richards, president of VMI, is talking graphics performance. You can program the 34010 processor to perform any graphics function you want, unlike hard-wired coprocessors. This means you can readily customize your system to outperform your competition.

But there's an even more important aspect to consider. The 34010 will help keep your system ahead of competition because it is compatible with existing graphics hardware standards — CGA,™ EGA,™ and PGC™ — and supports graphics software standards such as CGI, DGIS,™ and MS-Windows.™

Standards like Windows and DGIS run faster on TI's TMS34010

The 34010 is also among the fastest microprocessors available. It handles six million instructions per second with a "draw" rate of up to an amazing 50 million pixels per second. Thus, it can boost total system performance.

Because of the support of MS-Windows and DGIS alone, many major applications software packages can already run on 34010-based systems.

TI's MegaChip Technologies

Our emphasis on high-density memories is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip™ Technologies, and they are the means by which we can help you and your company get to market faster with better products.

workstations, terminals, plotters, FAX, image processing, digital copiers, mass storage, robot vision, and communications.

TI's total systems solution

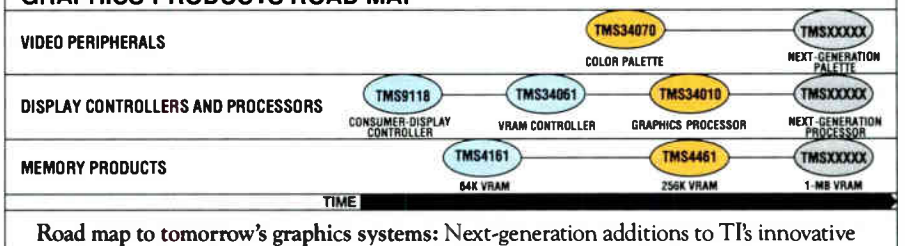
In implementing your design, you'll want to consider other building blocks TI has developed. Included are the single-chip TMS34070 66-MHz Color Palette that supports simultaneous display of 16 out of 4,096 colors and the TMS70C42 Microcontroller that handles all serial interface duties.

Also included are high-speed video random-access memories (TMS4161 and TMS4461), plus linear small and large-area CCD image sensors.

To provide the host bus interface and any other customized functions you may require, TI offers quick design and production turnaround through its Application-Specific Integrated Circuits (ASICs) capabilities.

Development tools are available now for applying the 34010. Turn the page for details. ▶

GRAPHICS-PRODUCTS ROAD MAP



Road map to tomorrow's graphics systems: Next-generation additions to TI's innovative graphics-products family will allow you to build on your present designs to develop even higher-performance systems.

"You would think TI designed the 34010 with our technology in mind."

Luis Villalobos, Conographic president, refers to the power of the 34010 to process font outlines for desk-top publishing. Resolution up to 64K × 64K means no hardware limits for laser printers and other hard-copy devices.

Host independence and the flexibility of a device programmable in "C" language make TI's 34010 the cost/performance leader for PC displays, laser printers, desk-top publishing,

"Texas Instruments had ready the full set of development tools we needed."

As William Frentz, executive vice president at Number Nine Computer, points out, TI has ready the hardware, software, and documentation you will need to make designing in the 34010 as fast and as easy as possible.

TI's 34010 software includes a full Kernighan and Ritchie "C" compiler with extensions and an assembler package for both MS-DOS™ and VAX™ operating environments.

A graphics/math library provides source code for more than 100 functions, whereas a typical controller chip offers only 15 to 20. A special font library contains more than 100 type fonts to expedite development of desktop publishing applications.

The TMS34010 XDS/22 Emulator is a flexible, realtime, in-circuit emulator. It can be used in a stand-alone mode through a standard terminal or through a host computer with a powerful debugger interface.

To see immediately what TI's new graphics processor can do for you, just plug the TMS34010 Software Development Board into an IBM® PC-compatible or TI Professional computer. The board is populated with TI's 34010 Graphics Processor, Color Palette, and VRAMs. It provides an ideal environment for developing your own high-performance graphics applications.

For more information on TI's total graphics-system solutions, including details on TI's Graphics Design Kit and design training courses, complete and return the coupon today. Or write Texas Instruments Incorporated, P.O. Box 809066, Dallas, Texas 75380-9066.

FOR FREE ON-LINE INFORMATION, dial 1-800-345-7335 with any 80-column ASCII terminal or PC and a 300 or 1200 baud modem (EVEN or IGNORE parity, 7 data bits, 1 stop bit). At "Enter Response Code," type TIGRAFX. In Conn. dial (203) 852-9201.

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26-4537

To speed the design of your graphics system, TI's range of development tools includes a comprehensive design kit *(left rear)*, a realtime emulator, and a plug-in software development board. On floppy and magnetic disks: "C" compiler, assembler package, and function and font libraries. User's guides, development books, product bulletins and data sheets, and TI's newsletter, *Pixel Perspectives*, are all readily available.

Hundreds of designers must be right. Hundreds of hardware and software designers are making TI's 34010 the new graphics standard. Among them are leading board-development houses and major software vendors.

In fact, the wide range of graphics standards and application software already written for TI's 34010 makes it the easiest-to-use new graphics chip ever introduced. Here's just a sampling of the software that will run on top of Graphic Software Systems DGIS* 34010:

Software Products	Company
AutoCad™	AutoDesk
GSS*CGI™†	GSS
Master Series™	Ashton-Tate
Freelance Plus™	Lotus GPG
Graphics Development Toolkit™†	IBM
Harvard Presentation Graphics™	Software Publishing Corp.
ProDesign II™	American Small Business Computers
VersaCad™	VersaCad Corp.
Windows™†	Microsoft
Symphony™,1-2-3™	Lotus Development
P-CAD™	Personal CAD Systems

™Trademarks are as noted.

†More than 100 graphics applications are currently available for these operating environments.

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YES, please send me information on TI's Total Graphics-System Solutions.

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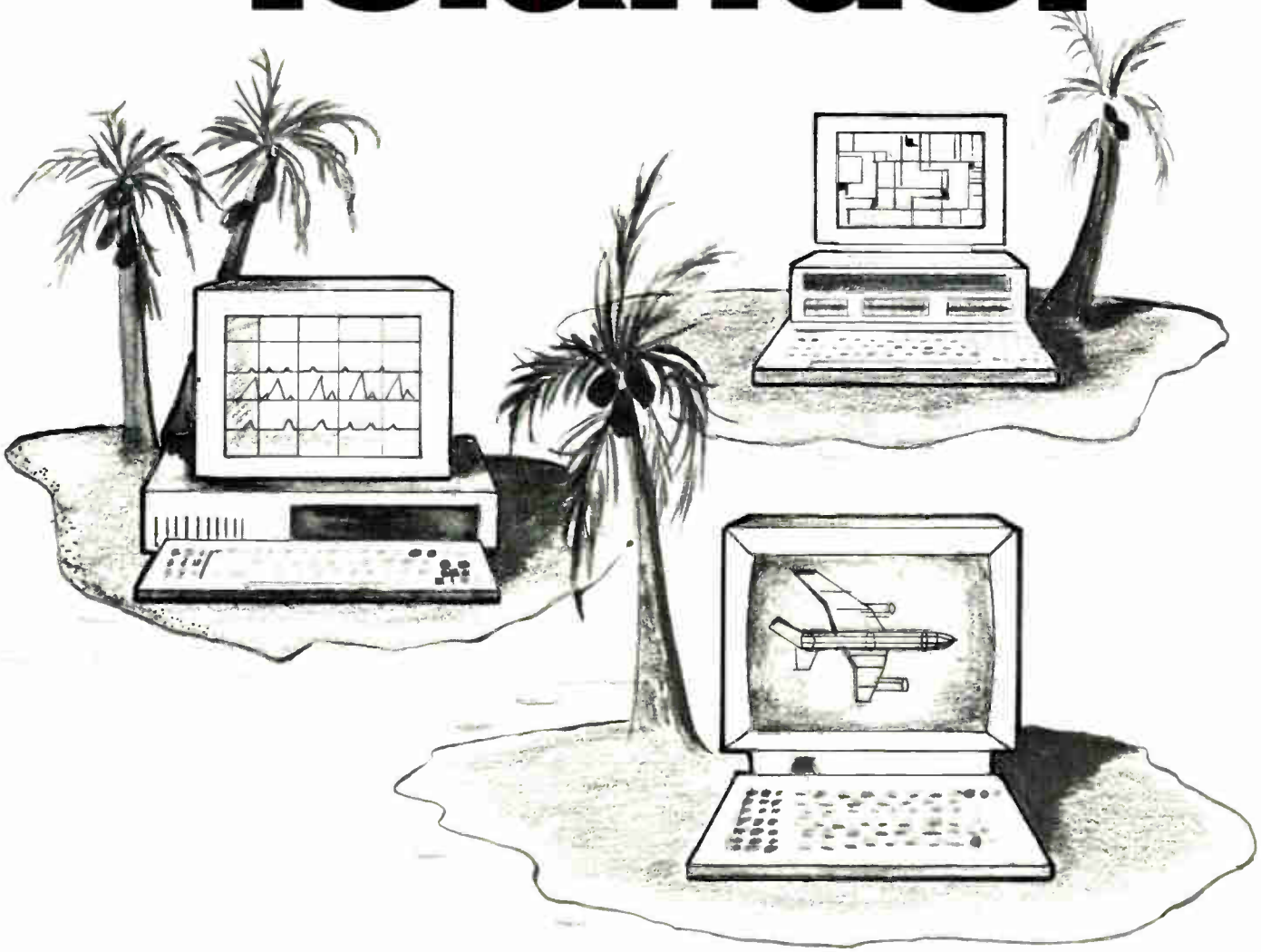
TEXAS INSTRUMENTS

Topical Islands.



In the June 25th issue of *Electronics* magazine, we will explore one of the hottest topics facing engineering managers today—design automation.

We'll discuss if, indeed, we are islands of automation. Or, if true design automation is becoming a reality. And who is responsible for bridging the gap.

It's a special issue. Focusing on the 24th ACM/IEEE Design Automation Conference being held in Miami Beach, June 28-July 1.

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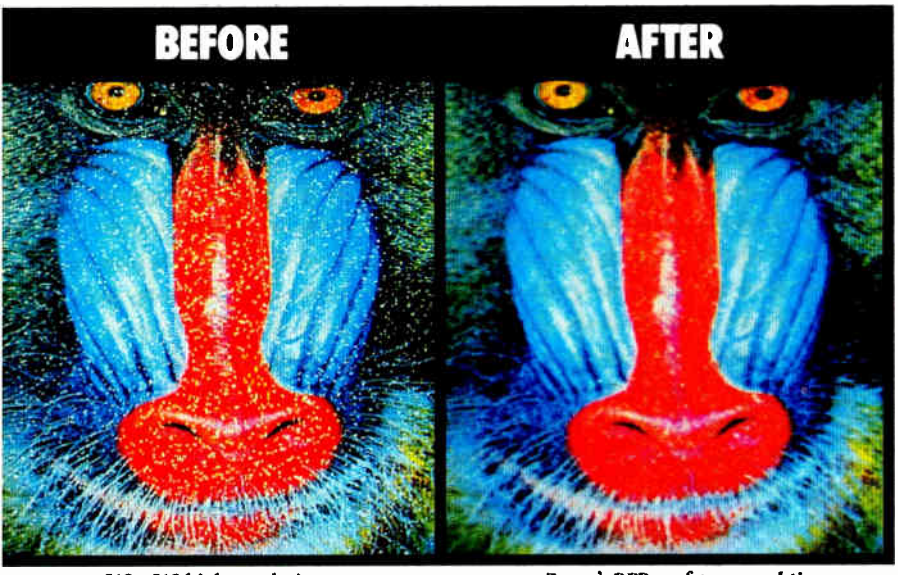
Electronics

Circle 20 on reader service card

REAL-TIME DIGITAL FILTERING NEVER LOOKED BETTER.

When it comes to high-speed digital filtering or correlation, Zoran's Digital Filter Processor (DFP) family makes it look better than ever.

Using system processors that deliver the high performance of building blocks. But with the high integration of a single device.



512 x 512 high-resolution image with randomly distributed noise.

Zoran's DFP performs *real-time* low-pass filtering to remove noise using a 7x7 convolution.

Each DFP is configured as a unique parallel-processing system capable of performing 320 million operations per second. At a blazing 20MHz throughput.

What's more, you can parallel multiple devices to reach throughput rates in excess of 120MHz.

And you'll do it in far less space, thanks to our highly integrated, proprietary architecture.

Which lets you design your system in a lot less time. At a lower cost. And with greater ease and flexibility than you ever thought possible.

The DFP is so flexible you can use a single device to easily implement a 32-tap decimate-by-four FIR filter.

The DFP makes all your applications look good. Take inspection, for example. You can execute complete 3 x 3 real-time imaging convolutions or correlations with a single DFP.

In high-speed satellite communications, digital radios, or radar, you can cascade multiple DFPs to achieve a higher sample rate and longer filter length, eliminating analog filters.

High-resolution video is easy with the 9-bit ZR33891, which delivers the longer word length and extended precision you need for studio broadcast applications.

You'll like the look of our tools and support. The shorter your development cycle, the better it looks. Which is why our VAX™ and PC-based tools provide you with everything you need for fast and easy implementation.

Including software for filter design and coefficient selection. And plug-in boards for real-time filter evaluation.

All of which explains why Zoran's DFP and Vector Signal Processor (VSP)™ product families provide the fastest, easiest solutions for computation-intensive applications.

Best of all, we're shipping products now. Instead of simply announcing them. Which means you don't have to wait to get the jump on your competition.

Take a look at our *free* databook. Call 1-800-556-1234, ext. 99 (outside CA), or 1-800-441-2345, ext. 99 (in CA). Or write Zoran Corporation, Dept. MC-1, 3450 Central Expressway, Santa Clara, CA 95051, 408/720-0444, ext. 3523. We'll make you look good in a hurry.

THE LAST WORD IN DSP. ZORAN

ELECTRONICS NEWSLETTER

IS THERE A CLOUD OVER MOSTEK IN THE SGS-THOMSON MERGER?

The pending merger of Thomson Semiconducteurs SA of France and Italy's SGS-Microelettronica SpA [*Electronics*, May 14, 1987, p. 60] leaves a lot of questions about the two companies' U. S. businesses up in the air. Pasquale Pistorio, who will be chairman of the new company, says 1,500 manufacturing and administrative jobs worldwide must be cut to make the firm more competitive. That makes some people wonder how Thomson Components-Mostek Corp.'s Carrollton, Texas, plant will survive the deal. "I think we have too many plants in the combine," Pistorio says, adding that the new SGS facility in Phoenix, Ariz., will be "the most advanced facility in the world—it's a super facility for the 1990s," since it will be capable of submicron work. As for the Carrollton facility, he says, "Mostek was good for the '80s, fantastic down to 1.2 μm, but Phoenix is for the future." Pistorio's decision should come by autumn, when he is expected to propose a five-year plan for the company. □

KEEPING UP WITH THE JONESES: NCR IS SET TO UNVEIL ITS NEW PCs

NCR Corp. isn't about to be left behind in the personal computer race. The Dayton, Ohio, company is expected to unveil its new personal-computer lineup this week, including a high-end 80386-based model that, while not fully compatible, will compete against IBM's new Personal System/2 Model 80. Other entries include two PC/AT-compatible machines based on the Intel 80286 microprocessor, a communications work station, and a Token Ring local-area network. NCR is pushing a flexible-architecture strategy that it says will let users choose between 3.5-in. or 5.25-in. floppy-disk drives, and upgrade from an 80286 processor to an 80386 by replacing a single board. The PC 916, scheduled for fourth-quarter delivery, is expected to cost between $6,350 and $8,650; the AT-compatibles, models 710 and 810, will be available in September for $2,000 to $6,000. □

SYMBOLICS COMES OUT WITH A MONOLITHIC SYMBOLIC PROCESSOR

Symbolics Inc., a leading maker of specialty symbolic processors, hopes to gain an edge over its competition with a highly integrated single-chip symbolic processor. Included on the chip are memory management for a full 32-bit address and 8-bit tag memory system, instruction and stack caches, and the instruction microcode. Called Ivory, the 400,000-transistor CMOS VLSI circuit was designed both as a commercial part and for use in the Cambridge, Mass., company's own machines. Symbolics will use it in its system products by the second half of 1988. Symbolics is targeting three groups of customers with chip and board products: defense contractors, who may use it as an embedded delivery platform; commercial vendors who want to add a symbolic coprocessor to their offerings; and original-equipment manufacturers. □

GENRAD'S NEW IC TESTER PUSHES STATE OF THE ART IN ACCURACY

Automatic test-equipment architectures once could test multiple pins with a single tester, but higher-density integrated circuits have forced ATE designers to go to a tester-per-pin strategy, where every pin is tested by an individual instrument. With the change, however, has come a sacrifice in accuracy, and now GenRad Inc., the Concord, Mass., ATE maker, is working on a solution. GenRad is developing the GR300 tester, a new system that promises a per-pin timing accuracy of 150 ps—compared with 250 ps for today's best systems. Scheduled to ship in late 1988 or early 1989, the GR300 will be able to handle chips with as many as 512 pins, double that of today's best offerings. □

ELECTRONICS NEWSLETTER

IBM WILL MAKE WAVES AS A COMMERCIAL SYSTEMS INTEGRATOR

IBM Corp. is starting a major push to become a dominant player in the growing commercial market for integrated systems. "We have the broadest range of products in the industry," says Dennis Sigloh, director of Systems Integration at IBM's Information Systems Group, "but there will still be times when customers' requirements go beyond our product line." IBM's new strategy is to help find the needed equipment and work with other vendors and systems integrators to put together a total solution. But as new as the strategy is to IBM's commercial sector, systems integration has been a major part of its Federal Systems Division for 30 years. IBM Information Services will head up the commercial integration effort, drawing on the experience and help of FSD, which works as both a prime contractor and subcontractor in developing military and government systems. □

WHAT HAS THREE ARMS, NO LEGS, AND JUST ONE CONTROLLER?

Researchers at the Westinghouse Research & Development Center, Pittsburgh, have demonstrated what's believed to be the first system that allows multiple robot arms to work together under a common control program. The approach greatly simplifies the programming task, Westinghouse says, compared with techniques relying on stand-alone controllers for each arm that report to a common supervisor or communicate in a rudimentary fashion. The Westinghouse Troikabot uses three Puma 560 robot arms that operate in the same work envelope, using intelligent electrical grippers, force-feedback sensors, and an integrated vision sensor. The control program used is a modification of a real-time control system developed at the National Bureau of Standards, and could be extended for use with more than three arms. □

THE AEA BLAMES CHIP AGREEMENT FOR DOMESTIC SALES SLUMP

Domestic electronics sales slumped in the first quarter, and the American Electronics Association blames it primarily on the slow implementation of the U. S.-Japan semiconductor trade agreement. The reason, the AEA says, is that the deal spawned a Far Eastern gray market for semiconductor products that tempted U. S. manufacturers to move production off U. S. shores. Cheaper parts overseas improved their sales and profits, without increasing domestic production, according AEA president Richard J. Iversen. Citing Commerce Department figures for domestic electronics sales—including the value added in the U. S. to products made offshore—the AEA says sales were $56.1 billion for the March quarter, down almost 10% over the fourth quarter of last year. Employment in the domestic industry dropped 60,000, to 2.47 million, between last August, when the pact took effect, and February 1987, the AEA says. The Semiconductor Industry Association, which lobbied hard for the trade agreement, disagrees, however. The SIA says the real reason for the shift offshore is low labor costs. □

HERE COMES A NEW WAY TO TEST HIGH-SPEED GaAs ICs

What's holding back the next generation of high-speed gallium arsenide integrated circuits? Simple: today's test equipment just isn't fast enough to keep up with their 100-GHz cycle times. Lightwave Electronics Corp., a Mountain View, Calif., startup, is hoping to get things rolling, though, with a new laser-based testing scheme. Using a technique developed at Stanford University and AT&T Co.'s Bell Laboratories, Lightwave built a prototype for the U. S. Air Force's Rome Air Development Center. The system applies laser pulses, 5 ps in duration, onto the chip. The frequency—or speed—of the chip can then be determined by the intensity of the reflected beam. □

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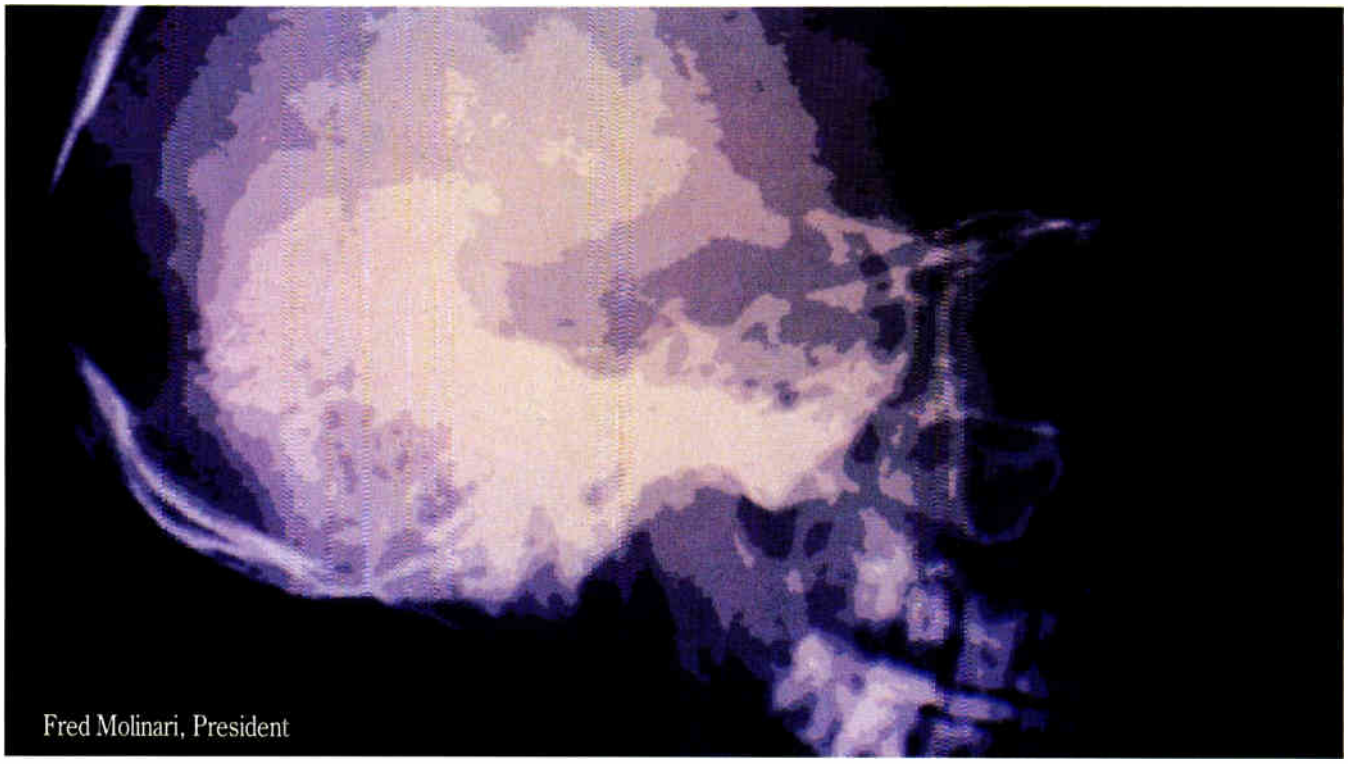
Thinking about Image Processing on the VMEbus? Think Data Translation.



Are we out of our skull? Data Translation's Image Processing boards and software for the VMEbus are priced below the competition's. Yet Data Translation squeezes more functions on a board.

Since Fred Molinari sets prices, we had his head examined. As you can see, Fred and his skull are doing quite well.

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- Full-functionality-on-one board (thanks to custom CMOS chips and surface mount technology!)
- Real-time ALU processing on the frame grabber
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Simply put, Data Translation has the best values on Image Processing boards and software for the VMEbus.

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Image Processing Board	Spatial Resolution	Gray Levels	RS-170, NTSC, RS-330, CCIR, PAL Compatible	VCR Compatible	Slow-Scan Compatible	Number of Video Inputs	Real-Time Frame Grab	Input and Output LUTs	Memory-Mapped Frame-Store Memory	Real-Time Processing N-by-N Conv., Math, Logic, Histograms, Zoom, Pan, Scroll	Price
DT1451 High Resolution Frame Grabber and DT1458 Auxiliary Frame Processor	512x 512	256	✓	✓	✓	4	✓	✓	2 Buffers 512x512x8 (512 KB) and 1 Buffer 512x512x16 (512 KB)	✓	✓	DT1451 $2995 DT1458 $1895

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Circle 26 on reader service card

PRODUCTS NEWSLETTER

SOFTWARE PACKAGE DOES MICROSOFT WINDOWS 10 TIMES FASTER

A new software package from Graphics Software Systems Inc. speeds execution of Microsoft Corp.'s Windows by a factor of up to 10 on systems that use Texas Instruments Inc.'s TMS34010 graphics chip. Based on source code written by TI engineers in Houston, the accelerator is firmware that offloads Windows chores to TI's graphics chip. It requires about 15 Kbytes of host memory and another 60 Kbytes in the 34010. It will be available from the Beaverton, Ore., company in June for $15,000, which includes a redistribution license for 3,000 units. A demonstration disk for IBM Corp. PC ATs and compatibles with TI's Software Development board costs $2,495. □

NCR BOOSTS SCSI INTERFACE CHIP PERFORMANCE 33%...

The newest entry in the race to offer the most advanced Small Computer System Interface single-chip controller comes from NCR Corp.'s Microelectronics Division. The NCR 53C90 aims to snatch performance honors from market leader Western Digital Corp.'s WD33C93 SCSI controller by boosting the asynchronous transfer rate from 2.5 Mbytes/s to 3 Mbytes/s. The chip minimizes protocol delays by using dedicated sequential logic instead of on-chip general processing that has to be interrupted for multitasking commands, according to the company. It was developed with Emulex Corp., Costa Mesa, Calif., and will be jointly marketed. The NCR 53C90 will be available in August, priced at $21.99 in quantities of 1,000. □

...AND ELIMINATES 200 DEVICES IN COMPUTER-PERIPHERAL LINKS

Interfacing as many as four 8-bit peripheral controllers to the new generation of 32-bit microprocessors has gotten a lot simpler for systems designers, thanks to a CMOS chip from NCR Corp.'s Microelectronics Division that replaces up to 200 devices. The NCR 8232 has an internal 32-bit buffer to handle direct-memory-access requests from the processor. On the peripheral side, its internal 32-bit shift register exchanges data 8 bits at a time with up to four peripheral chips. The Colorado Springs, Colo., division targets production deliveries in the third quarter priced at $55 each in 1,000-unit quantities. □

WAFERSCALE 256-KBIT EPROMS ARE UP TO FOUR TIMES FASTER THAN RIVALS

A pair of 55-ns, 256-Kbit erasable programmable read-only memories from WaferScale Integration Inc. boasts access speeds three to four times faster than comparably sized nonvolatile memory devices from other semiconductor houses, say company officials. The byte-wide 32-Kbit-by-8-bit WS57C256F and word-wide 16-Kbit-by-16-bit WS57C257 are fabricated with the Fremont, Calif., company's patented self-aligned split-gate EPROM technology. The memories can run in 32-bit systems without wait states and consume 300 mW each. Available within the next 30 to 60 days, both devices cost $94 each in quantities of 100. □

MONITOR HIKES MAC II RESOLUTION TO 1,600 BY 1,280 PIXELS

Cornerstone Technology's monochrome monitor for Apple Computer Inc.'s Macintosh II features 1,600-by-1,280-pixel resolution, 67-Hz noninterlaced refresh rate, and a 200-MHz video bandwidth, strengthening the Mac II's bid for computer-aided-engineering and design applications. The San Jose, Calif., company claims its Vista 1600 19-in. monitor offers the highest resolution available for the Mac II. Available now, the Mac II version retails for $2,195. A version for IBM Corp. PCs and compatibles and Intel Corp. 80386-based computers costs $2,395. □

PRODUCTS NEWSLETTER

VLSI TECHNOLOGY'S CHIP SET CUTS IC COUNT 70% FOR PC/AT CLONES

Look for a new chip set from VLSI Technology Inc. to drive down the cost of building an IBM Corp. Personal Computer AT compatible by cutting IC counts on the clone's motherboard from 130 to 36. That translates to up to a 20% savings over competing motherboard-silicon costs, claims the Phoenix, Ariz., company. The five-chip set also promises easier customization. Since it was designed with a megacell technology, designers using VLSI's Chip Compiler tools can recombine elements to suit applications in hours instead of months. Samples of the 12-MHz VL82C100 peripheral controller, VL82C101 system controller, VL82C102 memory controller, VL82C103 address buffer, and VL82C104 data buffer will be available in June, and production parts in the third quarter priced at $68.85 per set in 10,000-set quantities. □

MATSUSHITA COMES UP WITH MONSTER ROMS THAT ARE STILL FAST

Memory engineers at Matsushita Electric Industrial Co. in Osaka, Japan, have developed 8- and 16-Mbit mask-programmable CMOS read-only memories that boast a speedy 200-ns access time—equal to 4-Mbit speeds. Fabricated in the company's 1-μm shallow-trench technology, the devices consume 300 mW in active mode and break new ground in capacity. The 16-Mbit MN2316000 can store 28,000 characters in a 24-by-24-dot format required for Japanese-character generation in word-processor dictionaries; the 8-Mbit MN238000 stores 14,000 characters. Other applications include waveform storage for electronic musical instruments. Samples are available, with delivery two months after order. The MN2316000 costs $71 each in Japan, and the MN238000 is $36. The mask charge is $5,700. □

TRW ACCELERATOR SPEEDS 1750A MATH CALCULATIONS BY NEARLY 50 TIMES

Designers of next-generation avionics gear working with the Air Force's Airborne Computer Standard 1750A chip architecture will soon be able to get their hands on a 32-bit accelerator integrated circuit that boosts the speed of floating-point add/subtract computations by a factor of nearly 50. The TMC3202 floating-point processor chip from TRW Inc.'s LSI Products Division races through add/substract operations in 125 ns, compared with the 3.1 μs of representative 1750A chips, according to the La Jolla, Calif., company. Fabricated in 1-μm CMOS technology, the accelerator boasts a top data-throughput rate of 8 million floating-point operations per second. It will also speed up the yet-to-arrive 1750A sets being developed by contractors in the Very High Speed Integrated Circuits Phase 1 program. Samples will be ready in the fourth quarter of this year, at a price of $400 each in 1,000-piece quantities. □

TELEVIDEO'S 386-BASED WORK STATION RUNS FASTER AND COSTS LESS

Televideo Systems Inc.'s family of Telestar 386 work stations based on Intel Corp.'s 80386 microprocessor executes 2.2 million instructions per second on a 16-MHz clock—50% better performance than a low-end Sun Microsystems Inc. work station for about 80% the cost. The Televideo machines are also the first 386-based work stations on the market, claims the Sunnyvale, Calif., firm. An operating environment called DOS Merge-386 lets users run AT&T's Unix and MS-DOS applications concurrently. Televideo also provides an Ethernet and TCP/IP interfaces and supports the Windows networking standard. Available now, the low-end Model 15M, with 4 Mbytes of memory, a 15-in. monochrome monitor, an Intel 80287 floating point coprocessor and a 40-Mbyte hard disk, sells for $3,995 to original-equipment manufacturers. A fully configured top-of-the-line Model FS costs $15,995. □

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NEC

Electronics

IT'S CRUNCH TIME AS SEMATECH RACES TO GET ORGANIZED

NEEDED ASAP: SITE, BOSS, AND MONEY—FROM BOTH THE U.S. AND IC MAKERS

CUPERTINO, CALIF.

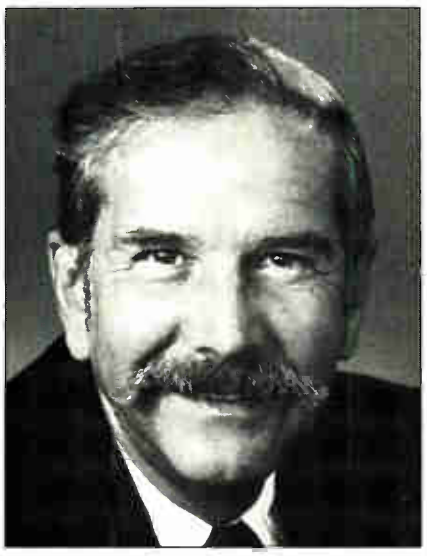
The selling of Sematech has begun. Organizers of the Semiconductor Industry Association's landmark chip-manufacturing technology consortium are going to have a frenetic summer as they race to complete an overflow list of critical jobs. The must-do list includes:

- Have most membership commitments in hand by the end of June. Backers hope to enlist at least 25 to 30 major chip makers as members and to have their annual funding pledges pinned down by September.
- Line up support in Congress to get the $125 million in annual federal aid the SIA is aiming for.
- Select a manufacturing site by September with the goal of making the first chips in the last half of 1988, and hire a chief executive officer, president, and chief operating officer by September.
- Persuade U.S.-based semiconductor-manufacturing equipment makers and materials suppliers to participate and pay dues.

Proponents argue that the project must go ahead because without it, U.S. leadership in advanced integrated circuits will be lost. "It is the most ambitious project of its kind ever contemplated," states Jon Cornell, senior vice president at Harris Corp., who is a director of SIA and one of the creators of Sematech. "We're late doing this—we've denied the problem of competing [with Japanese manufacturing technology] for some time. The reality is that the U.S. semiconductor industry will die if we don't do something like this."

The first key indicator will come at the end of June, when the SIA expects to tally up the Sematech commitments from among its 41 member companies. The SIA's aggressive target is to collect a total of $125 million a year from 25 to 30 members and raise a matching amount from the federal government. Each member would pay 1% of the value of its chip shipments, including captive use.

The membership task is complicated, because the SIA expects many firms to make their commitments contingent upon how much the government contributes, or on the percentage of SIA membership involvement. But because of the slow-moving political process, congressional authorization and exact funding levels are not likely to be final until late this year, says Alan Wolff, the SIA counsel in Washington, D.C., who is working to clear legal hurdles.



SPORCK: Sematech chips will be used up—or even destroyed—but they won't be sold.

Crawling through the congressional mill is a critical piece of legislation—the House-approved trade bill earmarking $100 million a year for Sematech through 1992. The Senate's defense authorization bill includes $100 million, but only for the next two years. Additionally, Sematech funds are being sought from the Defense Department, which could get the money from defense authorization bills.

RESTRICTIONS. Membership will be restricted to chip-making firms primarily owned by U.S. citizens and having a domestic manufacturing base. This provision will bar subsidiaries of foreign-based firms—such as Fairchild, Inmos, Mostek, Signetics, and several Japanese-owned operations—as well as the wave of startups and niche silicon houses dependent on offshore foundries, says the SIA.

Also yet to be chosen is a home for the consortium. Stanford L. Kane, the IBM Corp. vice president who heads the site-selection panel, has mailed letters to civic leaders who might be interested in luring Sematech, which will eventually employ 700 to 800 people.

Kane says Sematech wants a site with an existing 100,000-to-200,000-ft² building that can house a clean room and can be occupied by year's end. It also prefers 30 to 35 acres of adjoining land for a future facility, to be built by the end of 1989.

Another issue yet to be hammered out is the role of U.S.-based makers of semiconductor manufacturing equipment and materials. They are being asked to participate in Sematech via a specially created SIA chapter: the U.S.-based members of the Semiconductor Equipment and Materials Institute Inc.—about 750 out of the total of 1,150—will be invited to join for about $5,000 for large companies and less for smaller ones, says William H. Reed, executive director of SEMI. It is anticipated that SEMI members would form small vertical consortiums to bid on Sematech proposals.

Despite the formidable path ahead, officials estimate that Sematech could begin research as early as this fall. Production of its first technology-driving chips—most likely static random-access memories—is to start in the second half of 1988. World-class simulated volume manufacturing is to begin by 1990.

An early sticking point—what to do with the chips produced—has since been smoothed out. Charles E. Sporck, president of National Semiconductor Corp. and chairman of the SIA's Sematech steering committee, promises that none will go to market. Instead, they will be used in testing or in process characterization—or simply destroyed. Volume production runs will be simulated by storing wafers at various points along the fabrication line and then "stressing" equipment and processes on a 24-hour basis. This should keep excess chips to a minimum. Other decisions, on the exact technology definitions and on production techniques, will be made this fall.

—J. Robert Lineback, with bureau reports

A CES LOVE-IN FOR COMPACT-DISK VIDEO

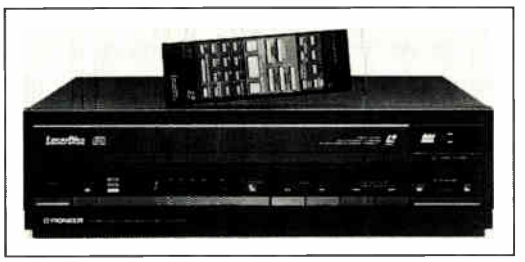
CHICAGO

Consumer electronics hardware and software vendors are beginning to act like a fickle married couple who argue and then get into bed. The two of them are vehemently divided over the issue of next-generation digital audio tape (DAT) technology. But everything's coming up roses when the topic turns to Compact Disc Video (CD-V), the latest format to hit the industry.

More than 30 peddlers of consumer hardware and video and audio software are in Chicago this week for a flashy, Hollywood-style launch of the video "singles" format. The stage is the Summer Consumer Electronics Show. And in the 6,000 ft² CD-V booth, hardware and software suppliers will put aside their differences that have postponed mass introduction of DAT to the U.S. market [*Electronics*, Jan. 22, 1987, p. 30].

Unlike DAT, a record/play medium that has the recording industry concerned over copyright issues, CD-V relies on play-only optical disks that can't be used to make copies. The 5-in. disk format packs five minutes of video with audio, as well as an additional 20 minutes of sound only. Costing about $7 each, the CD-V disks will be 30% to 50% cheaper than conventional audio-only CDs, which play up to 70 minutes.

Combination players for around $750 will hit the stores this summer. They will handle not only the CD-V and CD formats, but also conventional 8- and 12-in. video platters. In addition, the industry plans to offer 5-in.-format-only players for roughly $600.



IN CHICAGO: Pioneer will show this all-purpose player for CD, CD-V, and 8-in. and 12-in. video disks.

The record industry sees CD-V as a way to sell the video promotion clips that are an important part of album sales and artist promotions. "Before, we just gave it to the TV companies for promotion," says Guenter Hensler, president of Polygram CD-Video, a unit of Polygram Records Inc. in New York.

BACK AGAIN. For the movie industry, CD-V is another try at video disks. Despite superior playback quality, video disks never caught on with U.S. consumers, who instead have flocked to lower-priced play/record videocassette recorders [*Electronics*, July 12, 1984, p. 92]. With CD-V, "we're hoping to give video disk its best shot," states a spokesman at Warner Home Video Inc. in Burbank, Calif.

In all, John Messerschmitt, vice president at North American Philips in New York, expects that 200 to 300 CD-V titles, slated to start showing up this summer, will be announced at the show. Likewise, about 50 8-in. titles will be unveiled, along with 12-in. titles.

Despite industry enthusiasm, some observers remain skeptical. "This is obviously an attempt to revive the video disk. It's a good medium, but it bombed the first time around," observes David Lachenbruch, editorial director for the trade publication *Television Digest* in New York. The key to CD-V success, he believes, hinges on having "large amounts of programming" on hand.

Lachenbruch gives the format an outside chance of catching on big with consumers. But he points out that 40 million VCRs are already in the hands of U.S. consumers, compared with only 250,000 video disk players. "You can't sell software unless there's some way to play it," Lachenbruch comments. "It's a big chicken-and-egg situation." And VCR was there first. –*Wesley R. Iversen*

EAST MEETS WEST IN IBM PCs

TOKYO

Japanese politicians and business executives never seem to tire of explaining how different their country is from the rest of the world. But now IBM is challenging that belief, at least as far as Personal Computers are concerned, by making its U.S. and Japanese PC products compatible. That will enable software publishers to sell original versions of their wares in Japan and will enable IBM to reap the benefits of producing hardware and software for Japan in different countries, and vice versa, as it always has with products sold in the rest of the world. Until now, IBM PCs made in Japan for sale in Japan could use only recompiled software, because the basic input/output system and hardware are different. IBM PCs made in the U.S. were sold in Japan only through selected dealers at a high price.

The first inkling that things were going to change came when IBM introduced its Personal System/2 in Japan hours after the U.S. announcement [*Electronics*, April 16, 1987, p. 46] and said that it would support the products in the Japanese market at competitive prices. The company also said that its Systems Applications Architecture would support both American and Japanese PC products.

This was followed in short order by a new line of IBM Personal System/55 PCs for Japan (all machines made for Japan have the "55" prefix) that includes the 5570, a Personal System/2 model 80 variant that is being built in IBM Japan's Fujisawa plant. It uses the same powerful 80386 processor and the same 3½-in. disks as its American cousin. But the Japanese version of the new multitasking OS/2 will be more powerful initially than that for the U.S. because it will provide native support of 3270 terminal emulation.

Also new are the 5530, 5550, and 5560, made for IBM by Matsushita Electric Industrial Co. The 5530, like the System/2 model 30, uses 3½-in. disks and an 8086 processor. The 5530, last year's 5540, and 5550 also have small system units that fit under the monitor rather than the large units that fit alongside it that their predecessors have. Use of IBM 1-Mb memory chips for the main board and expansion memory, as well as extensive use of surface-mount technology, help keep down the size.

The fact that the new 5550 and 5560 as well as the 5540 use 5¼-in. disks points to a system in transition. The floppy drives for the three products in the middle of the range are not compatible with those for the bottom and top-of-the-line products. Their 80286 processor—running at 10 MHz in the new models—could well remain in next year's systems, though. Chances are good that there will be new systems with 3½-in. disks next year, because models have changed every year since 1983, when IBM introduced its multistation 5550 in Japan. –*Charles L. Cohen*

DESIGN TOOLS

A MAJOR HARRIS THRUST LINKS FORTH WITH RISC

MELBOURNE, FLA.

The first fruits of a program to develop a family of real-time microprocessors, support macrocells, and hardware and software tools that integrate the Forth programming language with reduced-instruction-set computer architecture will be available late this year from Harris Corp.'s Semiconductor sector.

The CMOS family, called Force (Forth-optimized RISC computing engine) Toolbox, will be built around a 16-bit microprocessor. It will have macrocells, standard cells that include 7400-series logic and 8086/8088 peripheral chips, and hardware and software design tools for standard ICs that combine Forth and RISC. Harris plans to offer both standard and semicustom chips, starting with a real-time control processor and a local-area-network controller.

Forth is especially suitable for real-time military and industrial applications involving control and digital signal processing, such as vision systems, robotics, communications controllers, signal processing, and input/output controllers. The combination of CMOS processing and RISC architecture gives power and performance benefits not possible with bipolar processors, says Michael Graff, vice president for marketing at the Melbourne, Fla., company.

For example, a tenfold reduction in power consumption is possible compared with bipolar processors, and speed might be increased by the same factor—to a sustained 10 million to 15 million instructions per second for the core microprocessor, and 30 mips peak. Harris licensed the microprocessor architecture from Novix Inc. of Cupertino, Calif., and CAD software from SDA Systems Inc. of Santa Clara, Calif.

The key to the architecture, says John Peers, Novix chairman and chief executive officer, is simplicity. "There is no microcode, and there are no wait states," he points out. The entire processor is implemented in fewer than 16,000 transistors and directly implements in silicon the primitives described in the Forth language, he says.

Semicustom devices are expected to become available early next year, after the standard parts begin to flow. Graff says it will take three to five years for the Force technology to be designed in. He looks for the family to account for "substantial business" at Harris within three years. *–Larry Curran*

COMPONENTS

A NEW WAY TO 'SPEC' DSP PERFORMANCE

AUSTIN, TEXAS

A trend-setting technique is riding in from Texas that will make it a whole lot easier to build digital-signal-processor systems. Crystal Semiconductor Corp. of Austin has come up with a new way to look at the dynamic error sources that impede DSP performance with harmonic noise and distortion, and is rolling out analog-to-digital converter ICs that were made using the technique.

The 2½-year-old analog IC house has created test software, based on a fast Fourier transform, that exercises and measures fast data-conversion performance in the frequency domain rather than in the more traditional linear area. This enables it to predict and guarantee the resulting chip's performance in DSP applications. Crystal Semiconductor officials are betting that the new family of what they call S-to-Z domain converters will give the Austin company an early foothold in the emerging market for analog-to-digital DSP front-end circuits, which are nearly half the high-performance converters sold today.

ANALYSIS. The FFT test algorithms turn standard chip testers into DSPs, which then analyze the S-to-Z (S for continuous time, Z for sampled time) converter's dynamic performance in terms of the spectral content of the digitized signal. The FFT programs run the converters through a set of test conditions representing real-world signals.

During the testing, a pure sine wave is applied to the sampling ADC chips. A time record of 1,024 samples is logged in memory and processed by the FFT testing software. The program sorts through the spectral content of the digital waveform, distributing its energy into 512 "frequency bins." Energy falling outside those bins is characterized as errors, which are then included in the new Z-domain specs.

"The bottom line is that engineers working on DSP systems have had to go through a lot of design effort and characterization of parts trying to respecify the ADCs," says John R. Croteau, product manager for Crystal's data-acquisition products. "Being the first in the industry with monolithic sampling converters, we thought it was appropriate to lead the industry into frequency-domain specifications."

Industry analyst Will Strauss of Forward Concepts Inc. in Tempe, Ariz., says the attempt to create a method of grading Z-domain performance in ADCs is a significant move, and he believes Crystal could be starting a trend. "There are no such specs today. The traditional specs now tell you about the linearity of parts, but there is a certain set of assumptions buried in all of that, and you hope it will work for DSP applications," he says. He calls the FFT-testing software "an interesting way of doing it, and the testing of ICs can certainly enhance their value."

Forward Concepts estimates $235 million will be spent on ADCs in DSP applications. That represents nearly a fourth of worldwide component sales in DSP markets. Strauss says the DSP front-end segment is groing 32% a year.

Crystal is introducing the new frequency-domain specifications by announcing three FFT-tested versions of traditionally tested 12-, 14-, and 16-bit

WORLDWIDE DSP MARKET

	1986	1987	1988	1989	1990	1991
Analog to digital	168	235	306	397	517	672
Digital to analog	50	79	123	172	223	290
Total*	706	1,006	1,396	1,916	2,600	3,500
In millions of dollars						

*Includes one-chip DSPs, general-purpose microprocessor units used in signal processing, building-block components, and data-conversion circuits.

SOURCE: GNOSTIC CONCEPTS INC

sampling ADCs it brought out earlier this year. The block functions are identical, and only processing tweaks are being made in selected portions of the dielectrics of the 3-μm CMOS chips. These process changes have been found to improve the performance rating of the converters being measured with the new FFT-test software. For many non-DSP applications, Crystal continues to offer the original converters, characterized with traditional linearity specs.

The S-to-Z family contains three devices that perform conversion with successive-approximation algorithms, plus one device that uses delta-sigma techniques. Pricing on the 16-bit converters starts at $69 each in 100-piece quantities. The 14-bit chips start at $58 each and the 12-bit converters at $34 each, also in 100-piece orders. Total harmonic-distortion ratings are as low as 0.002%, and signal-sampling rates can be as high as 63 KHz. *–J. Robert Lineback*

MATERIALS

A TEST THAT COULD BOOST GaAs YIELDS

MUNICH

If gallium arsenide is ever going to be a mainline semiconductor material, developers will have to do a better job of solving processing problems and find a way to produce higher yields. Now help may come from a new test technique for GaAs material. If it works as billed, yields may dramatically improve, thus pushing device costs down and sales up.

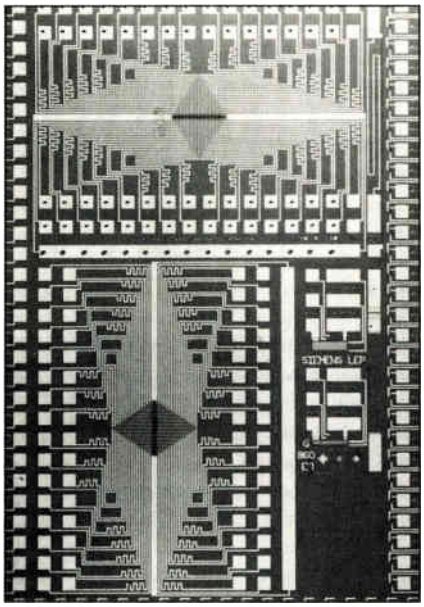
The idea is to examine GaAs ingots and reliably classify their quality before they are processed. This would enable device makers to determine whether a specific ingot is pure enough for complex ICs with critical fabrication steps or whether it can be used only for simple discrete components.

Testing takes place on a microscopic scale: with a 10-μm spatial resolution, or over distances as small as 10 μm. The technique was developed at West Germany's Siemens AG and France's Laboratoires d'Electronique et de Physique Appliquée, a member of the Netherlands-based Philips Research Organization.

The test is performed by ion-implanting into the wafer metal-semiconductor FETs in a dense-row pattern and measuring their threshold voltage. The variations of the voltage values give a clue to crystal impurities and dislocations in the material, and hence to its quality. The variations also hint at such electrical characteristics as electron mobility, isolation behavior, and charge-carrier profiles.

It is difficult to say just how much the Siemens/LEP method raises yield, because not only material quality but also processes, equipment, and design come into play. Also, the technique is too new to provide reliable yield figures, although the French and German developers are now using it routinely.

But one thing can be said: "By systematically classifying and selecting GaAs ingots, one can almost be certain that it is not the material's fault if a circuit fails," says Gerhard Packeiser, who heads the GaAs Substrate and Layers Group at Siemens's Central Laboratories in Munich. "We expect yield to improve considerably, because with state-of-the-art GaAs substrates, material-related circuit failures will now account for less than 20% of total failures."



FOR TEST. Siemens test structure's dense-row transistors are in the diamond patterns.

Until now, Packeiser explains, device makers could not determine for sure whether the substrate material's influence on circuits is the same everywhere across the wafer. The only material-quality check used so far is a macroscopic one, a method that puts several discrete and widely spaced transistors on the wafer and then compares their performance against each other.

The Siemens/LEP technique, by contrast, for the first time checks out a GaAs wafer microscopically, which means that test structures with typical IC dimensions are involved. That accounts for the method's reliability. The technique employs MES FETs because of their excellent high-frequency behavior and comparatively easy process technology.

MATCHING. Basic to the test philosophy are findings that the quality of only one or two wafers cut from the ends of a GaAs ingot (typically 15 cm long) is the same as that of the entire ingot. Other experiments have shown that the local defect density in the material is correlated to the threshold voltage of the MES FETs on the wafer.

For quantifying the material, the researchers implant about a hundred 2-mm-by-4-mm test structures (see photo) on a wafer, which may be 2 or 3 in. in diameter. Each structure has at its center a dense-row pattern of 30 FETs over 300 μm long spaced 5 μm apart. That makes the transistor-to-transistor distance 10 μm, which is the spatial resolution.

Using such a test structure, it is possible to measure the variations of the transistors' threshold voltage—which is typically around 25 mV—with computer-controlled test equipment. This finally gives clues on a microscopic scale to the effects of impurities and crystal dislocations on transistor parameters and tells whether GaAs devices can be made from a particular ingot with the required yield. *–John Gosch*

NAVIGATION

NAVIGATING BY SATELLITE STARTS GETTING CHEAPER

SUNNYVALE, CALIF.

For more than a decade now, engineers have sung a siren song of low-cost positioning by satellite. For the military, that would mean everyone from a soldier in a Jeep to a pilot flying across the Pacific could read the output from a black box to instantly learn his location to within 1 m. And once the equipment price dropped in volume production, this navigation tool could be used in a host of nonmilitary applications. For one, it could even be installed in the family car.

This ambitious program hasn't moved nearly as fast as its developers had promised, mainly because of the delay in launching the constellation of orbiting Global Positioning Satellites (GPS) need-

ed for the triangulation. And the lack of the shuttle to launch GPS also slowed development of ground receivers, keeping their volume down and costs up.

But a glimpse of the future will be given in mid-June at the Paris Air Show. There, Valentine L. Denninger, vice president of Trimble Navigation, will be walking around with a battery-powered receiver in his briefcase that will track his position to within 15 m and immediately report it out. Weighing only 2.53 lbs, including its separate antenna, the receiver is about the size of a Kleenex box, measuring 9.5 by 5 by 2 in. Trimble calls it "the Brick." In contrast, the company's first-generation satellite-positioning system weighs 57 lbs, measures 25 by 21.5 by 10 in., and has an antenna weighing another 15 lbs.

The new Trimble receiver is priced at slightly under $13,000, or under $5,000 in 1,000-unit volume. That's half the price of systems built only last year, Hyler says. And only volume production, he says, is needed to bring receiver cost down to $200, which would make it suitable for autos. Trimble tested the Brick in a car around its Sunnyvale, Calif., headquarters, and it produced output that, when used to drive a plotter, laid a dotted line right down the middle of highways drawn on a standard U. S. Geological Survey 7.5-minute map, says Ralph Eschenbach, vice president for engineering.

NEW GATE ARRAY. The new system, based on a Trimble-designed gate array that carries less than 10,000 gates, has all the digital signal processing for two-channel reception, including phase-locked-loop circuitry, a correlator, timing, and analog-to-digital conversion. There are 24 Kbytes of on-chip random-access memory and 40 Kbytes of read-only memory, the latter to decode the satellite signals and compute coordinates. Phase shifts in the arriving signal are used to calculate position. The Brick delivers digital positioning information, either as latitude, longitude, and altitude, or as three-dimensional Cartesian coordinates from an origin at the center of the earth, plus velocity.

Trimble, a seven-year-old firm, thinks that huge new markets will open when the satellite transmitters are in place. Beyond the obvious navigation systems, more exotic applications are possible for static measurements in which the satellite-based system is used with a reference receiver and data is integrated over time, making possible positioning with centimeter accuracy.

One major construction firm, for example, has invested in the technology, hoping it will make it possible to control the blade angle on earth-moving equipment so as to dig out absolutely level grades. Another application would be to measure minute changes in the position of a dam or building to detect structural weakness or earthquake damage.

Such applications make Trimble think it may be sitting on a bonanza. It won't find out for a while, however, because of the lack of launch power. Only seven of the Rockwell-built satellites were operational when the Challenger shuttle exploded early last year, and 18 are needed for 24-hour coverage. Next launch of a 2,700-lb. satellite, this time on a Delta rocket, isn't scheduled until October 1988. Complete global coverage won't be available until 1990.

Nevertheless, Trimble has plowed ahead. "Some of the bigger firms had to cut back their efforts because they couldn't afford the overhead of large staffs and no market," says marketing vice president F. H. Hyler. "However, to us a $10 million market looks fine." Trimble had sales last year of $7.5 million and expects to reach $12 million in 1987. It competes with large companies such as Rockwell's Collins division, Magnavox, Motorola, and Litton.

Litton's Aero Products Division in Moorpark, Calif., has a $55,000 receiver that measures 12.75 by 7.5 by 7.5 in. and weighs 20 lbs. A next-generation system may also be demonstrated at Paris.

Complicating development of positioning systems is the fact that the satellite signal is controlled by the Department of Defense. Once the entire transmission network is in orbit, the DOD says, it will change the signal on the channel that is accessible for civilian use so as to degrade system accuracy to 100 m for navigation. The purpose is to deny accurate data to a potential foe.

Even at 100 m, says Eschenbach, the accuracy would be better than current inertial navigation systems. An inertial system accurate to 1 mph would be off by six miles after only six hours, Eschenbach points out. A satellite system, however, is time-insensitive and keeps on updating its position. *–Clifford Barney*

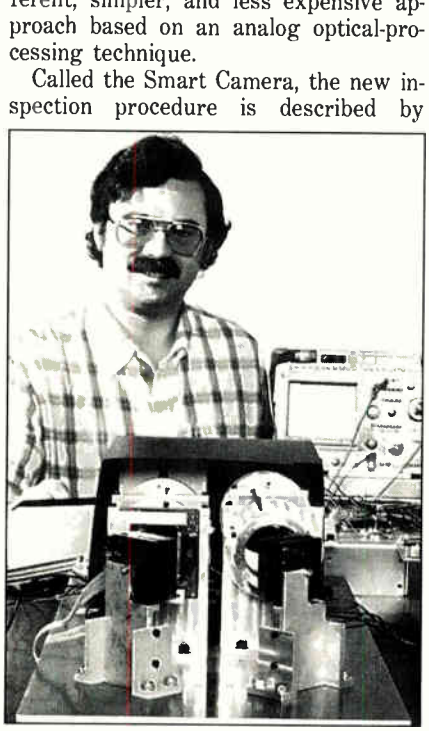
OPTICAL PROCESSING

A LOW-COST APPROACH TO SIMPLER MACHINE VISION

FAIRFIELD, IOWA

High-speed machine inspection requires heavy doses of parallelism to handle the massive pixel-processing requirements. Now a fledgling Fairfield, Iowa, firm called Global Holonetics Corp. has come up with a radically different, simpler, and less expensive approach based on an analog optical-processing technique.

Called the Smart Camera, the new inspection procedure is described by James Belilove, chief operating officer, as "the only commercial two-dimensional optical signal processor for machine vision or any other application." It relies on a technique known as optical Fourier feature extraction, which capitalizes on the ability inherent in coherent optical systems to process massive amounts of data spontaneously and in parallel, limited only by the speed of light.



CAMERA. Global Holonetics president David Clark and the company's optical processor.

Though well understood, the technique has been too expensive for commercial applications. But Global Holonetics says that clever engineering and the use of low-cost, conventional optical components have brought the price down.

In its initial configuration, the Smart Camera will handle certain types of high-speed inspection jobs at up to 900 objects per minute in a system costing around $10,000, the company says. On a turnkey basis, that's about one fourth to one third the price of conventional high-speed digital machine-vision systems, says Global Holonetics founder and president David Clark. Prototype shipments are expected to start by about midyear.

At least one expert sees promise in the Global Holonetics approach. "The kind of things these people are doing are going to be important," says H. John Caulfield, director of the Center for Applied Optics at the University of Alabama in Huntsville and chief technical adviser for the Strategic Defense

Initiative's optical-computing program. Optical Fourier techniques have to date been employed in only a few military applications, such as in aerial-photography analysis, Caulfield says. But "everybody in the world, including us, the Japanese, and the Soviets, is working on it," he says.

'Everybody in the world, including Japan and the USSR, is working on it'

Two-dimensional Fourier feature extraction works when a coherent laser is directed through a transmissive, programmable 2-d plane known as a spatial light modulator, on which an image is represented. The image information is encoded on the beam, which then spontaneously generates a 2-d Fourier transform that occurs at a point on the beam known as the Fourier plane. The transform is a spatial representation of the frequency content of the image created by the diffraction of the light around the contours, edges, and other features of the image.

Global Holonetics uses about 65,000 liquid-crystal elements in the Smart Camera to create the spatial light modulator. These are addressed electronically, taking input from a video camera at a 15-Hz rate. The laser shines through the image plane and appropriate lenses, and then a set of photodetectors positioned at the Fourier plane picks off the transform information. This creates a Fourier "feature signature" that can be compared to a known good signature.

To hold down the cost, the transform data is sampled strategically. It can be robustly characterized by only 32 data points (which amounts to a 2,000-to-1 compression factor, compared with the 65,000 pixels on the original image plane), Belilove says.

But the real key to the Smart Camera's cost is Global Holonetics' use of conventional liquid-crystal technology to form the image plane. Until now, spatial-light modulators have been made using exotic liquid-crystal light-valve or magneto-optic technologies, Belilove says, at a cost for the image plane alone of $10,000 to $25,000, he notes. Meanwhile, conventional liquid-crystal technology has been considered inadequate for the job, because of poor contrast, lack of shift invariance, poor light efficiency, low resolution, and slow response. *–Wesley R. Iversen*

SOFTWARE

NEW DATA BASES TRY TO MOVE INTO NETWORKS

NEW YORK

Data-base software providers are trying to keep up with the steady migration of networks and distributed-processing systems into the realm of personal computers, work stations, and superminicomputers. It's not easy. The software must be powerful yet easy to use, handling multiple simultaneous updating and query operations at high peak volumes while offering the same fast response, broad capabilities, and flexibility available in single-user data bases. And, of course, absolute data integrity is a must.

But now two systems that address those challenges are on the market. Ansa Software of Belmont, Calif., is unveiling an advanced version of its Paradox data base for personal computers. And Sybase Inc. of Berkeley, Calif., has taken the wraps off a two-part relational data-base system designed for use on Sun work stations and Digital Equipment Corp. superminicomputers.

Ansa bills its Paradox 2.0 as the first personal-computer data-base system to offer full support for multiuser applications, permitting an unlimited number of users unlimited simultaneous access. Ron Posner, Ansa's president, says that other data bases claiming to be multiuser "have shortcomings that Paradox 2.0 doesn't, such as limited concurrent access, inadequate data protection, and slow performance."

Sybase, meanwhile, says its software is the first Sequel-based relational system to provide everything needed for on-line applications for work stations and superminis. It combines the performance of transaction-based file systems and the ease of use, flexibility, and maintainability of SQL-based relational data-base management systems. The NonStop SQL from Tandem Computers Inc., Cupertino, Calif., does the same on its transaction processing system.

Sybase's system divides the work into two parts, dubbed the DataServer and the DataToolset. The DataServer handles data management separately from the applications functions, which are controlled by the DataToolset. Both can run concurrently on a single computer or independently on different machines. For maximum performance, the DataServer runs as a single process under the operating system.

–Tom Manuel

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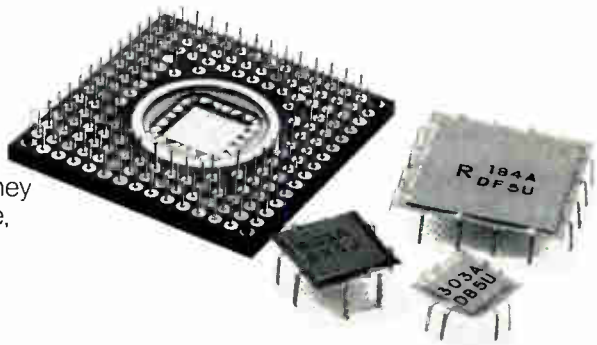

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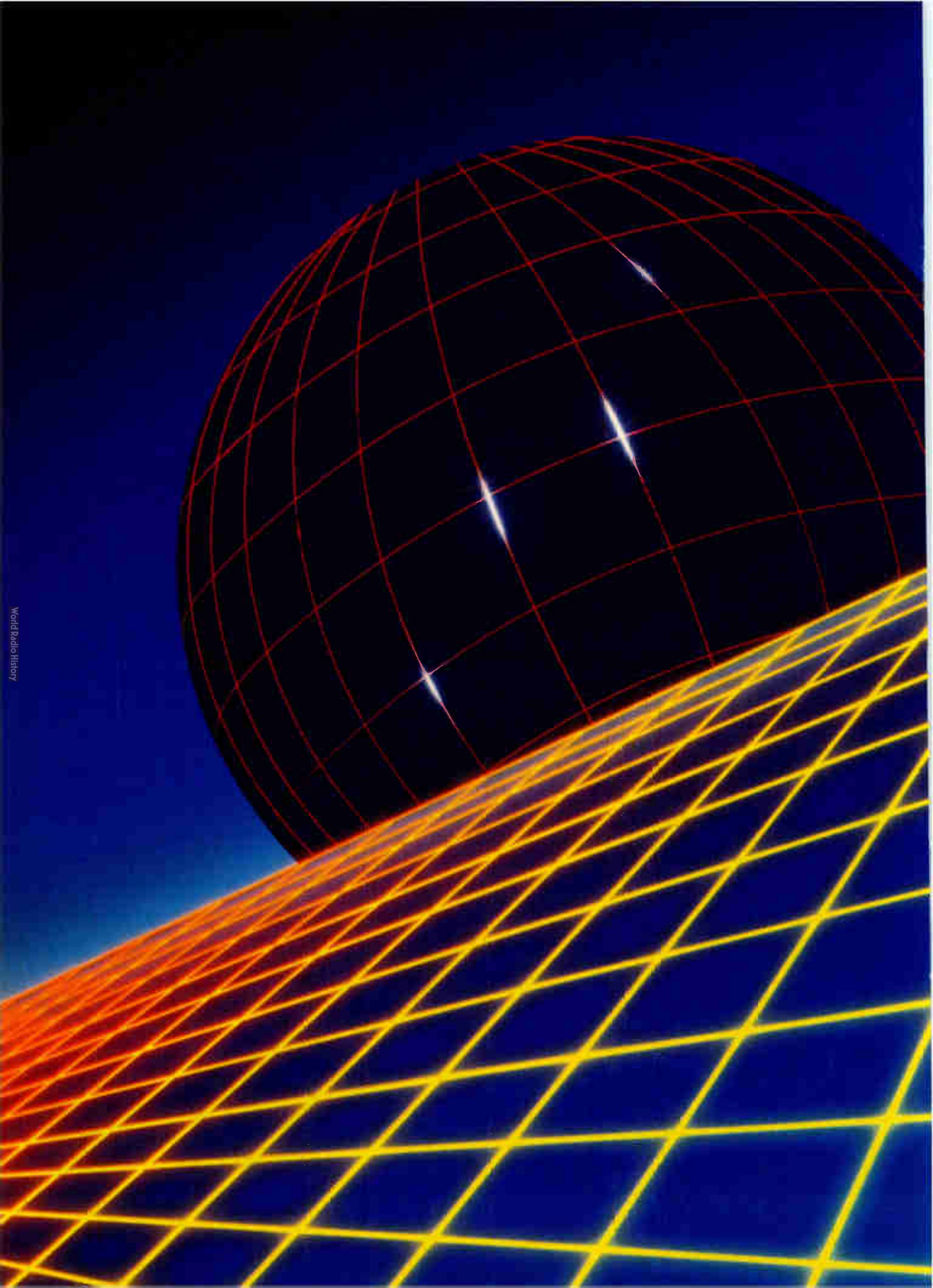

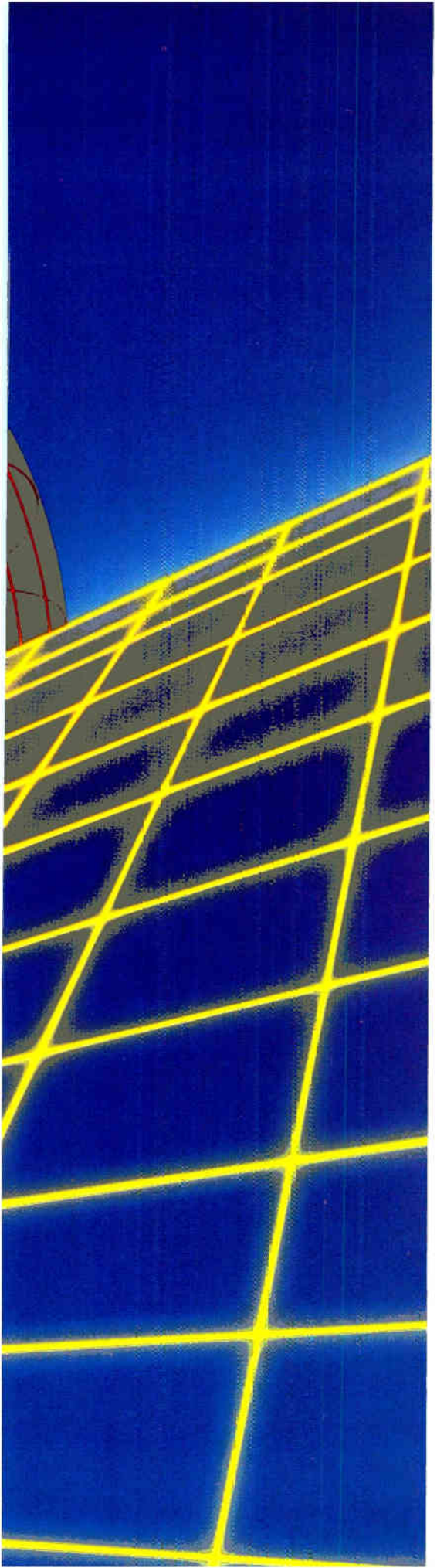

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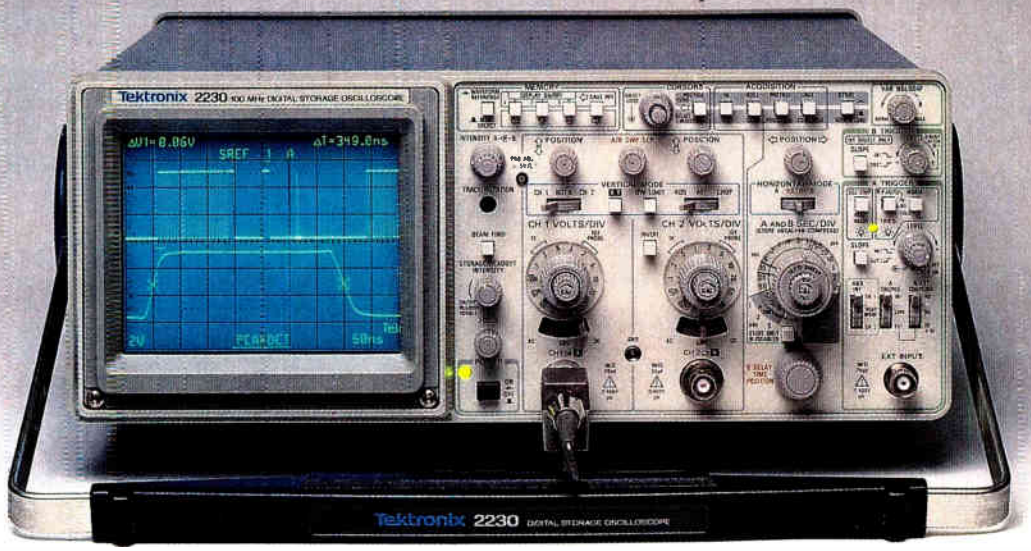

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Features	2230	2220
Analog/Digital Storage BW	100 MHz	60 MHz
Max. Sampling Speed	20 MS/s	20 MS/s
Record Length	4K/1K (selectable)	4K
Save Reference Memory	One, 4K Three, 1K	One, 4K
Vertical Resolution	8 bits 10 bits (AVG mode) 12 bits (AVG mode over bus)	8 bits
CRT Readout	Yes	No
Cursor Measurements	Yes (storage mode)	No
GPIB/RS-232-C Options	Yes ($850)	Yes ($550)
Battery-Backed Memory (save 26 waveform sets)	Yes (inc. with 2230 communications options)	No
Price	$5150	$4150

Both scopes offer optional GPIB or RS-232-C interfaces. With either option the 2230 also includes battery-backed memory that provides 26K of keep-alive CMOS memory—for storing up to 26 waveform sets.

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PROBING THE NEWS

HOW APOLLO EXPECTS TO KEEP ITS LEAD IN WORK STATIONS

IT STICKS TO ORIGINAL PLAN, BUT MOVES TO ALLIANCES, OPEN NETWORKS

Viewed alone, this month's introduction of a new work station by Apollo Computer Inc. is a logical step in capturing the market for networked engineering work stations. To fully appreciate Apollo's strategy, though, the unveiling should be viewed against a backdrop of several other recent developments at the Chelmsford, Mass., company. Taken together, these moves show that Apollo's management is continuing to follow a game plan that has been largely successful ever since the company was founded in 1980.

The mission, as chairman, president, and chief executive officer Thomas A. Vanderslice sees it, is "to continue as the premier vendor of leading-edge, network-based work-station solutions for technical professionals and work groups." In short, Apollo plans to hone its competitive edge through innovation, strong backing of industry standards like Unix, and forming strategic alliances with other leading companies.

HAMMERLOCK. Industry analysts indicate that Apollo is succeeding. In fact, Mark D. Stahlman, a research analyst at Sanford C. Bernstein & Co., New York, maintains that Apollo and Sun Microsystems Inc., Mountain View, Calif., "have a hammerlock" on the work-station business. "If they continue to execute well," Stahlman says, "both companies will pass the 100,000 mark next year in work stations installed."

For his part, John Hime, director of product marketing at Sun, respects his rival and appreciates its pioneering the technical work-station market that has allowed Sun to prosper. "They created the market," Hime attests, "and they got some of the important OEMs and software vendors, such as Mentor Graphics, on their platforms. Mentor has strong electronic CAD software, and it's available only on Apollo platforms." He suggests, however, that such exclusive arrangements are both an asset and a liability. "Newer software vendors don't want to be locked into any one platform or proprietary operating system, preferring an open system."

Apollo understands the problems created by its proprietary software and is taking steps to integrate its Domain network with such standards as Unix and Ethernet. Just last month, it announced a version of Domain that is network-independent and can run directly on Ethernet. And in February, Apollo took the wraps off the Network Computing System [*Electronics*, March 5, 1987, p. 32], which makes it possible to write application programs that run in distributed fashion on multivendor computer networks.

LEADER. President Vanderslice carries on after being recruited by Apollo founder Poduska.

And Apollo is working toward bringing Unix aboard its systems as a native operating system. About 18 months ago, the company hired Roland Pampel from AT&T Co. as its senior vice president of technology, marketing, and manufacturing, and he's played a big part in pushing Apollo toward AT&T's Unix operating system. Many company resources have been redirected toward a Unix program, which, he notes, is "under way and fundamental to our strategy."

MESHING. The goal of that program is to modify Domain's kernel so that it meshes with the AT&T and Berkeley incarnations of Unix without compromising its own functioning. "Unix will fully arrive a couple of years from now," states Pampel. But some pieces of the Unix puzzle must still fall into place, such as strong graphics standards, a windowing system such as X Windows—which Apollo already supports [*Electronics*, Jan. 22, 1987, p. 58]—and standard support for database operations and communications.

"It will save Apollo a lot of trouble to get Unix strongly integrated into the Domain system" by the time all those missing features are in place, Pampel points out. Domain features not integrated into Unix will be kept on a superset mode, he adds.

Such long-term strategies would be worthless without a solid business picture. The company lost money in 1985, but Vanderslice has been able to turn it around and 1986 saw Apollo return to profitability on sales of $391.6 million.

Vanderslice was recruited by Apollo founder J. William Poduska, who left in 1985 to form a company now called Stellar Computer Inc., Newton, Mass. Vanderslice credits Poduska with having the vision to start a network-based work-station company before the terms "work station" and "work group" came into use. "But Bill will tell you that he's not a day-to-day manager," says Vanderslice, who moved to Apollo from GTE Corp., where he was president and CEO. He also spent 23 years at General Electric Co. in senior management positions.

David L. Nelson, vice president and chief technical officer, recognizes Vanderslice as the creator of a management infrastructure that has moved the firm "well beyond the transition [from an entrepreneurship] to a professionally managed company."

That management brought the company back to the black after its only loss in 1985. That year revenues were posted at $295.5 million with a net loss of $1.5 million. In contrast, net income for 1986 was $9.3 million on revenues of $391.6 million. For the first quarter of this year, revenues were up 50% over the same period in 1986—from $82 million to $123.4 million. And net income jumped more than tenfold—from $539,000 to $6.4 million.

Vanderslice attributes the recovery to several factors. The 1985 results reflected a sluggish market, which has now come back to life. The positive trend of the past 18 months stems, in part, from the fact that Apollo delivered almost

half of its installed base of more than 38,000 work stations during that period.

Also contributing to the company's strong showing is a broadening of the customer base. When Vanderslice arrived, 70% of revenues came from just three customers. Today, the customer count totals almost 1,900, and no customer last year accounted for more than 15% of the revenues.

NCS is another reason Vanderslice and Nelson are smiling these days. Nelson notes that NCS is the first approach to computing that can distribute portions of a single applications program to whichever specialized computer on the network—regardless of its vendor—is best suited for the task, such as an artificial-intelligence engine, automatic test equipment, a design simulator, or a supercomputer.

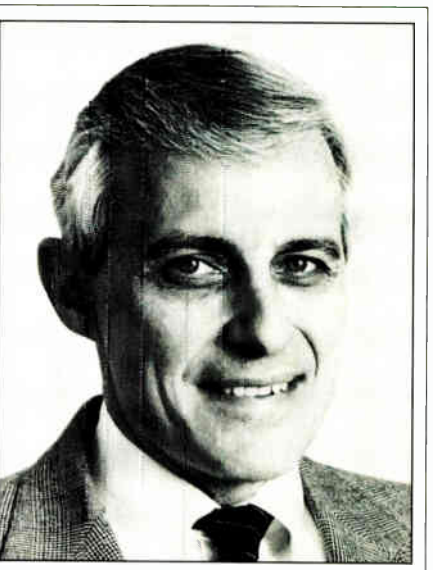
Three NCS components hit the streets in February. They are a Remote Procedure Call run-time environment, Network Interface Definition Compiler, and a package dubbed the Location Broker.

The run-time environment is transparent to applications programs. It handles the packaging, transmitting, and receiving of data and error corrections between the client and server subroutines—those parts of the application on the user's work station and on the computers delivering remote services.

NIDC converts programs written in Apollo's Network Interface Definition Language into portable C source code that can be compiled to run on both the client and server sides of the connection. The Location Broker lets applications programs determine at run time those networked machines that can supply services to the operator.

Apollo isn't alone in advocating a multivendor standard. Sun Microsystems lobbied for it before Apollo did, and Digital Equipment Corp. may launch its edition before long. Apollo's Paul Levine, a senior consulting engineer, counters that it isn't critical that NCS be universally adopted. "We think this is the best solution for now," he argues, "but it's more important that such a standard be adopted, not that we have the only solution."

In addition to a broadened customer base and advanced technologies, new markets are a mainstay of Apollo's game plan. Here again, the drive to make Domain network-independent and to offer full Ethernet support is essential. The Ethernet link allows users of Domain work stations to integrate more easily with computers, like the DEC VAX, that work with Ethernet.



OPENING UP. Pampel is helping to push Apollo toward the open-system world of Unix.

As part of the search for new territories, Vanderslice is constantly on the lookout for strategic alliances such as the three that were formalized last year. Under one of those, Apollo will collaborate with AT&T on versions of Unix, helping to define it as a standard for professional work-station systems.

The other 1986 alliances were made with Wang Laboratories Inc. and Texas Instruments Inc. Apollo has undertaken a cooperative sales effort to offer an open-office computing environment that joins Wang's technical office-automation products with the Domain system. The alliance with Texas Instruments weds Domain with TI's Explorer Lisp engine for AI applications.

NEW MARKETS. Beyond such affiliations, part of Pampel's job is to make sure Apollo is plotting new market opportunities. He's tracking the federal government and computer-integrated-manufacturing, having established formalized business units in those sectors. He expects substantial business to result—beginning this year—from more than $1 billion in government proposals outstanding. The CIM effort won't begin to produce revenue until 1989.

Nelson is quick to point out that although new markets are important, "we can't overlook the markets we now dominate—electronic design automation and mechanical CAD. A lot of new-product development is focused on these," with the latest embodied in the DN590.

He adds that much of the senior management team has remained with Apollo since its founding, "and we've been stable since Roland Pampel's arrival 18 months ago. We're a well-oiled machine now, all of us working with the same game plan." *–Larry Curran*

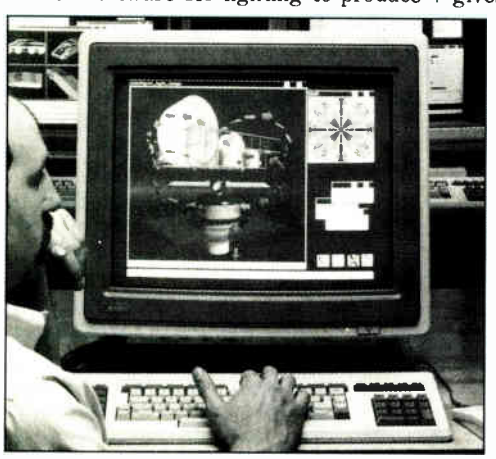
TRIMMING THE COST OF HIGH-END GRAPHICS

Apollo Computer Inc.'s newest work station, the DN590, catapults the company into the rarified atmosphere of very high-speed rendering of three-dimensional shaded solid objects in millions of colors and intensities with complex lighting. This capability, heretofore only available from a few expensive graphics processors and super work stations, is offered at a lower price and comes as part of the popular Apollo Domain network system.

The Apollo product developers have melded the computational performance of the company's top 68020/68881-based work station—the DN580—with two specialized graphics processors and advanced software for lighting to produce the DN590 Turbo color graphics work station. Aimed at the most demanding graphics applications—the modeling of 3-d solid objects for applications such as visual simulation, product styling, mechanical computer-aided engineering, molecular modeling, fluid dynamics, and animation—the cost-effective DN590 broadens Apollo's market scope. Software improvements boost both drawing and numerical calculation speeds.

A typical DN590 selling at $69,900 matches or betters work stations costing $100,000 or more, company spokesmen say. The work station comes with a 6-Mbyte array memory with 24 bit planes (the DN580 has only 8), which gives it the ability to display 16.7 million colors and intensities. The screen display size is 1,280 by 1,024 pixels, but the DN590's array memory measures 1,280 by 2,048. The extra memory is used for a 16-bit Z buffer for 3-d depth information.

The DN590 also boasts new lighting software for manipulation of light sources within a graphics image. Called the advanced lighting model, it supports up to 16 colored lights, spotlights, and specularity. The model is driven by microcoded subroutines. *–Tom Manuel*



COLOR-RICH. Apollo's DN590 models 3-d solids in millions of colors.

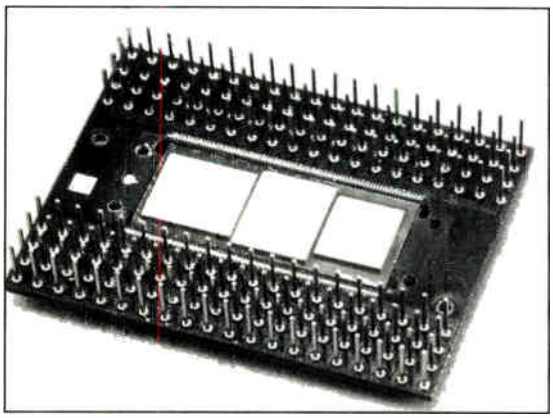
SILICON-ON-SILICON HYBRIDS ARE COMING INTO THEIR OWN

MULTILAYER PC BOARDS, CERAMIC SUBSTRATES CAN'T KEEP UP WITH VLSI

by Jerry Lyman

NEW YORK

Originally seen as a stepping stone to monolithic wafer-scale integration, the silicon-on-silicon hybrid is headed for a life of its own. Composed of chips bonded to a silicon substrate, this mix of integrated- and hybrid-circuit technologies is being worked on by Mosaic Systems, AT&T Bell Laboratories, and Hitachi. Moreover, an ongoing research and development program on silicon hybrids is being sponsored by the Semiconductor Research Corp. at Auburn University, Auburn, Ala.



1. FASTER. Bell Labs boosted the speed of the three-chip 32100 processor with a silicon substrate in a pin-grid array.

Giving silicon hybrids a big boost is the growing need to provide large numbers of high-speed interconnects, as well as greater packaging densities, to VLSI circuits. At the rate that VLSI technology is growing, packaging schemes based on multilayer printed-circuit boards and ceramic hybrid-circuit substrates simply can't keep pace with the interconnect demands. The fine-line geometries associated with the pc boards carrying the next generation of chips will be even tighter, says Maurice Sage, managing director of BPA Ltd., Dorking, Surrey, UK. "There is growing evidence," he says, "that pc-board technology will not be able to meet these developing requirements."

SPACE SAVER. The silicon substrate, which carries interconnects fabricated with well-established IC-processing techniques, can easily have 10-to-25-μm conductors, compared with the 3-mil conductors of the most advanced pc boards or ceramic hybrids. That helps reduce the area of a circuit to as little as 1/10 of what it would be on standard boards or hybrids.

With its short wiring runs, the silicon substrate also cuts parasitic inductance and capacitance by a factor of at least five. Those reductions account for the low propagation delays and high performance of typical circuits on multichip silicon substrates. Also, passive elements like bypass capacitors and termination resistors can be fabricated right on the substrate.

Another advantage of the substrate is that its thermal coefficient of expansion exactly matches that of the IC, eliminating the silicon-to-alumina mismatch in a ceramic hybrid. Further, metal or silicon carbide heat sinks can be glued to the substrate for efficient heat transfer.

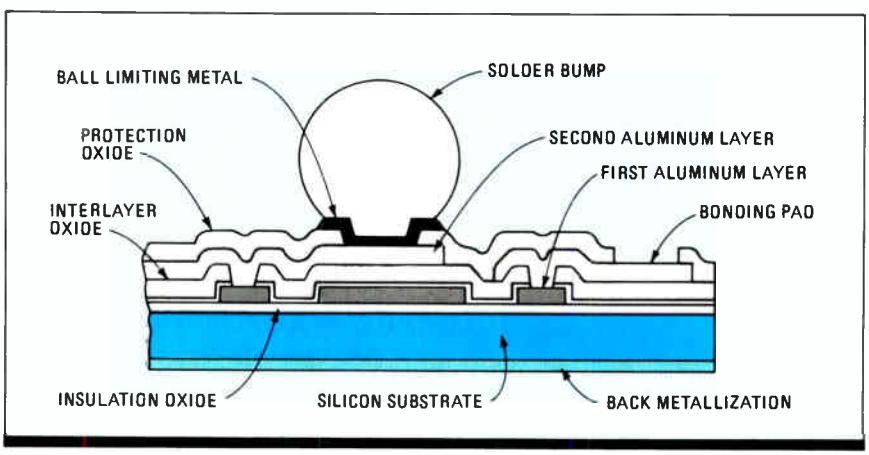
The substrate does has disadvantages. Four to nine chips can dissipate up to 15 W in about 1 in.^{2}, so special attention must be paid to cooling. And if more than four chips are bonded to the substrate, pretested ICs are needed to ensure a cost-effective yield.

Of all the firms engaged in silicon-on-silicon work, Mosaic appears to be the furthest along. It produces an off-the-shelf silicon substrate with a built-in grid of metal lines and amorphous-silicon vias that can be electrically programmed for connecting chips wirebonded to the substrate [*Electronics*, Nov. 27, 1986, p. 38]. Mosaic's product line is called Unipro SCB (for universally programmable silicon circuit board). It comes in two sizes—a 4-in. wafer and a 1-by-1-in. segment. The latter can carry up to eight memory chips; several of the substrates can be tiled together and connected with bonded wire. These tiled substrates fit in quad-width flat packs.

Mosaic's Unipro SCBs can save a significant amount of time. Fabricating, assembling, testing, and repairing a typical design with a ceramic hybrid substrate can eat up roughly five months. The same process with an SCB takes four to seven weeks. Design changes for a ceramic substrate can take 25 to 45 days. Because SCBs are layered before a design is programmed, changes are made in two hours by reprogramming.

Providing some help here is FutureNet, Canoga Park, Calif., a unit of Data I/O Corp., which recently revealed new computer-aided engineering tools. Based on an IBM Corp. PC AT, the tools were developed specifically for the Unipro SCB substrates. The Futurenet software is used to lay out and edit a design. Other software modules and a programming module then program the specified connections and reroute unsuccessfully linked connections.

Though Mosaic wirebonds chips to its substrates, two of the other silicon-hybrid entries, AT&T Bell Laboratories in



2. NO WIRE BONDS. Hitachi bump-bonds flipped chips to a silicon substrate, which carries two layers of metal interconnections and has a thermally conductive backing.

Murray Hill, N.J., and Hitachi Ltd. of Tokyo, base their multichip boards on reflow-soldered bumped chips. In both cases, the flip-chip connection was chosen for its low-inductance path between chip and substrate.

AT&T works with a two-layer structure consisting of polyimide insulation layers, copper conductors, and copper ground and power planes [*Electronics*, March 5, 1987, p. 34]. It departs from other silicon substrates, which use silicon dioxide insulation and aluminum conductors; it also features monolithic bypass capacitors. The overall structure is designed to achieve a 50-Ω characteristic impedance.

Interconnects take 1/10 the space with silicon substrates

Bell Laboratories has already built a 1.3-by-3.0-in. substrate for Western Electric's three-chip WE32100 32-bit microprocessor. This substrate, which has 160 input/output connections, is wire-bonded to a pc-board pin-grid array (see fig. 1). That approach raised the operating frequency by a factor of 3 and cut board area to 1/7 that required by conventionally packaging the same chip set.

Hitachi recently reported on its substrate—a 7-ns, 128-Kbit, multichip, emitter-coupled-logic random-access-memory module with on-board logic. The 14.2-by-25-mm module was developed to overcome the large interconnection delays between ECL RAMs and their peripheral chips. In the Hitachi module, eight RAMs and one logic chip are flip-chip bonded face down on a double-layer-metallized silicon substrate (see fig. 2). The substrate is then attached to a piece of high-thermal-conductivity silicon-carbide ceramic. The module is placed in a 96-lead flat pack; its logic is on a 700-gate array with 0.2-ns-per-gate delays. The ECL array is fitted with built-in termination resistors for a matched interface with the RAM.

Another variation on the silicon-on-silicon theme is being pursued at Auburn University's Microelectronics Science and Technology Center. Researchers at the university mount pretested ICs in holes etched in 3-in. silicon wafers and then connect them via a standard two-level aluminum metallization process. The group started out using polyimide as the interlayer dielectric, but an organic dielectric is now being evaluated.

Normally, the finished silicon substrate would be wire-bonded to the next level of interconnection (either a package or pc board), but the Auburn researchers are also investigating optical communications links. □

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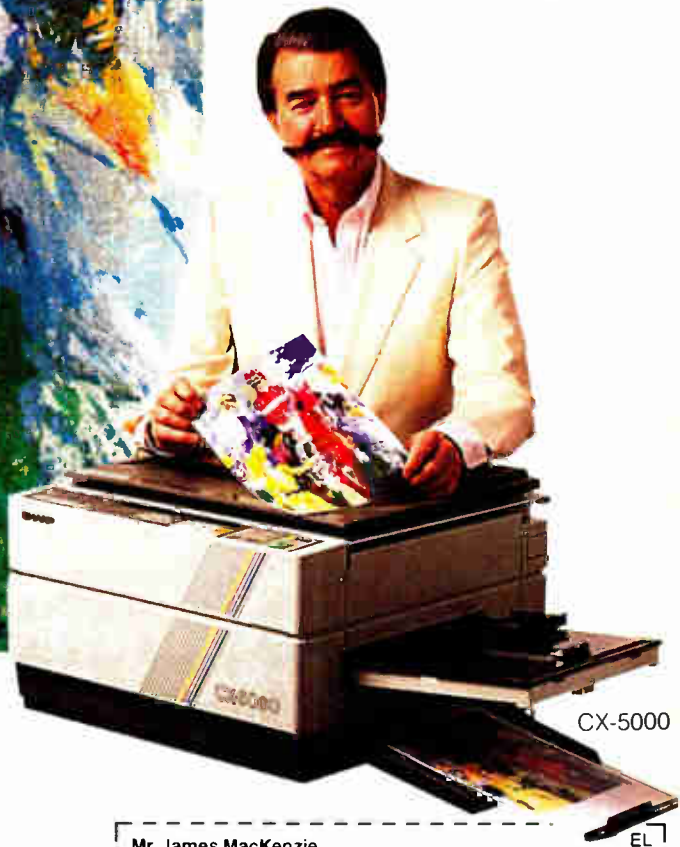

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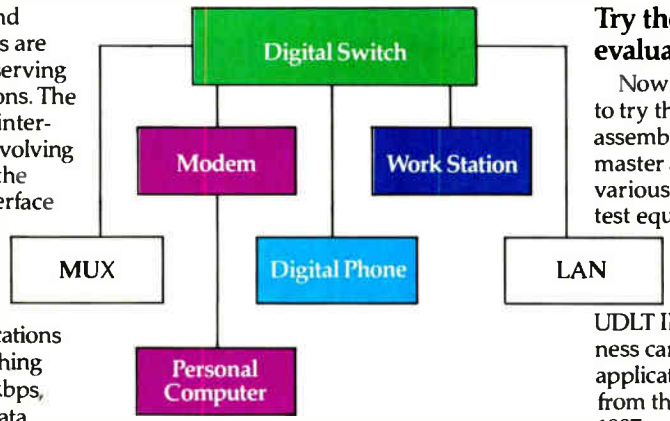

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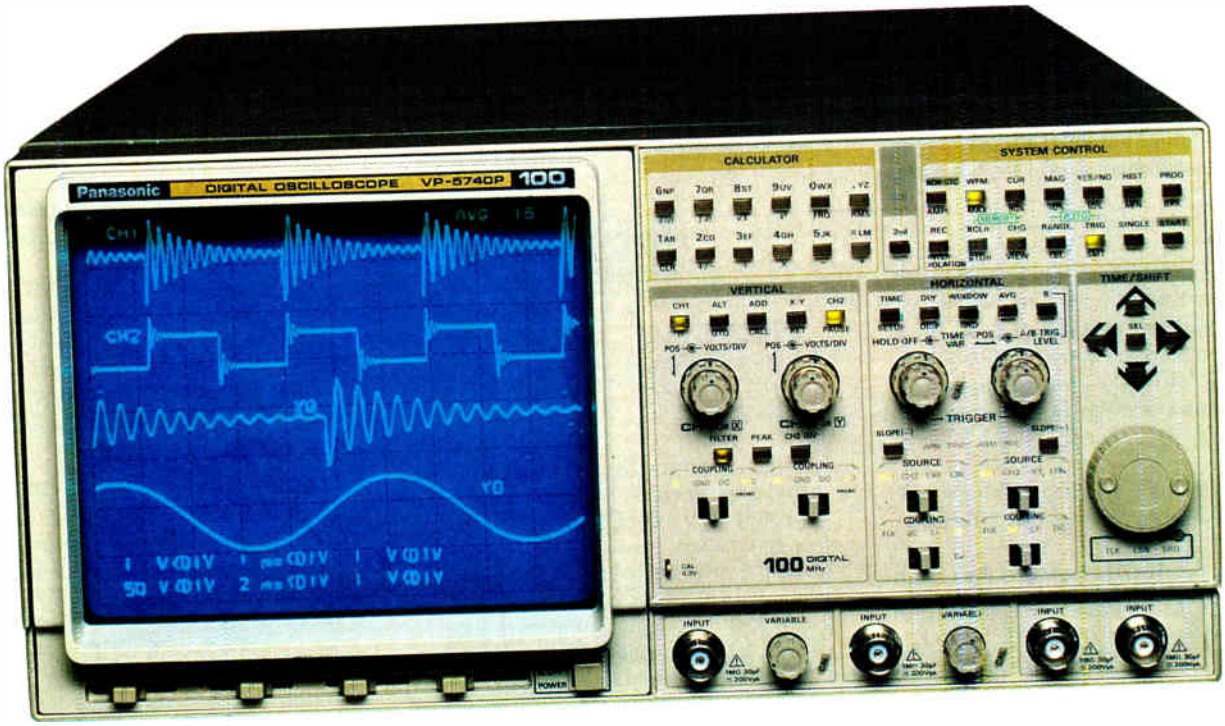

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INTERNATIONAL NEWSLETTER

THE JAPANESE TEAM TO DEVELOP TRON KEEPS GROWING

Add Mitsubishi Electric Corp. to the team of Japanese companies cooperating on the development of 32-bit microprocessors based on The Real-time Operating-system Nucleus (TRON). The Tokyo company joins Hitachi Ltd. and Fujitsu Ltd., the original TRON developers [*Electronics*, Nov. 13, 1986, p. 48], in a pact that will allow each to build the microprocessor it was working on before the agreement. Development of processor-independent peripherals will be divided among the group. Each company will be able to second-source the others' products, which will be suitable for Unix applications. Hitachi will be the first to announce a product—a microprocessor rated at 6 million to 10 million instructions per second for engineering work stations. It should be available late this year. Mitsubishi, meanwhile, expects to produce a 4.5-to-6-mips microprocessor for use in personal computers and application-specific controllers by early 1989, and Fujitsu plans to put a 12-to-20-mips chip for work stations and minicomputer applications into systems designers' hands by mid-1989. □

NOW IT'S NEC THAT'S SHIFTING COMPUTER PRODUCTION TO U.S....

Responding to the steady rise in the yen and to the trade sanctions imposed by the Reagan administration, NEC Corp. plans to shift some of its computer production to the U. S. NEC will begin assembling two personal-computer models in the U. S. by June, officials in Tokyo say. NEC Information Systems, its Boxborough, Mass., subsidiary, will build its 16-bit APC IVs to the tune of 16,000 units a month. NEC Home Electronics U. S. A., another subsidiary in Atlanta, Ga., will build NEC's Multispeed product, a 16-bit laptop machine, at a rate of "several thousand" units per month. The APC IV and the Multispeed made their debuts in the U. S. market last year. □

...AS MITSUBISHI WILL BE THE FIRST JAPANESE FIRM TO BUILD ASICS IN THE U.S.

Mitsubishi Electric Corp. will be the first Japanese chip maker to start manufacturing application-specific integrated circuits in the U. S. if a plan for a new plant in Durham, N. C., comes through. The company wants to build a wafer fab for ASICs there and hopes to start operations within the next year, but it has not yet decided how large the facility should be or how much to spend on it. Currently Mitsubishi Semiconductor America, a Durham subsidiary of the Tokyo conglomerate, limits its work to assembly, packaging 256-Kbit dynamic random-access memories at a rate of 1.6 million units/month and 64-Kbit DRAMs at 400,000 units/month. □

MOTOROLA MAY GET A PIECE OF TOKYO'S MOBILE-PHONE MARKET AFTER ALL

Motorola Inc. may get a share of Tokyo's lucrative cellular-phone market after all. The Ministry of Posts and Telecommunications will consider a request in June from Nippon Keitai Denwa KK, a new joint-venture company, to allow it to offer portable phone services on Motorola equipment in Tokyo's 23 wards. Another company, Teleway Japan Corp., recently won approval for its plan to compete with Nippon Telegraph and Telephone Corp. in Tokyo and other major cities. Teleway, which will start service at the end of next year, will use equipment developed by NTT. Motorola's phones are smaller and lighter than NTT's. And unlike the NTT equipment, they can be used from underground locations or within buildings, according to Nippon Keitai Denwa, which is owned jointly by Orient Finance Co., Japan's second-largest consumer financier, and Electronic Industrial Enterprises Inc., an electronic-parts trading firm, both of Tokyo. The new venture could start service by October 1988, and it hopes to have 35,000 subscribers by 1995. □

INTERNATIONAL NEWSLETTER

SEIKO READIES THE BIGGEST COLOR LCD TV YET

Seiko Epson Corp. of Suwa, Japan, will start selling a 3.3-in. pocket color TV in Japan on June 23. The compact TV will feature the company's new metal-insulator-metal active-matrix liquid-crystal display [*Electronics*, May 14, 1987, p. 32]. With 70,400 dots, the TV is the largest color LCD TV to be announced by any manufacturer. The new model weighs about 380 grams, 15% more than Seiko Epson's latest model, a 2.6-in. MIM panel with 56,320 dots that went on sale in February. The company expects to sell about 12,000 units a month in Japan at around $385 each—26% more than the 2.6-in. model. Plans to market the new TV in the U. S. or Europe have not yet been set, Seiko Epson officials say. □

BRITISH AI COMPUTER OUTSPEEDS FASTEST JAPANESE MACHINES

British Aerospace plc has developed an artificial-intelligence computer more than twice as fast as the fastest Japanese AI engines. The Declarative Language Machine, built by BA's Naval and Electronic Systems Division in Bracknell, UK, can execute 620-k logical inferences per second. The two-year-old High-Performance Sequential Inference Machine, developed by the Institute for New Generation Computer Technology in Tokyo and built by NEC Corp., can muster just 280 klips. ICOT says it has since developed a faster version of its High-Performance Machine, but the institute refused to disclose its speed. BA says initial applications for its computer include image cognition and recognition for television and infrared tracking systems for missile and gunfire-control systems. Such military controls would be used for target detection, target recognition, and other applications, such as classification and prioritization programs. □

THE DUTCH WILL OPEN UP THEIR TELECOM BUSINESS

The Dutch are now preparing to join the U. S., Japan, and the UK, and open up their telecommunications business to private competition. The Dutch parliament has already approved the move in principle. Various ministries are now working out the details of the plan, which will be presented to the cabinet later this year for final approval. It could be implemented by Jan. 1, 1989. Under the plan, two major changes are expected to increase competition in the Dutch equipment market, now valued at about $1 billion a year. First, a private company called NV PTT will be set up as the exclusive concessionaire for the telephone, data communications, and telex infrastructure. The second change will put an end to the government's monopoly on terminal equipment, such as private branch exchanges. This market will now be open to foreigners. □

HITACHI DEVELOPS A PHOTOSENSITIVE SUPERCONDUCTING DEVICE

Researchers at Hitachi Ltd. say they have developed the world's first optically driven superconducting switch. The device, which operates in temperatures up to 88 K, or −188°C, consists of two thin-film electrodes separated by a trench in which the superconductive film coating is thinner than elsewhere. Cooled in liquid nitrogen, the trench becomes superconductive, and electrons called "Cooper pairs" can tunnel through the area without resistance. Exposing the trench to light, however, restricts the free flow of excited electrons. That means that light—either from a laser or a light-emitting diode—can be used to switch the device between "on" and "off" states. Moreover, the device's light sensitivity can be increased more than 10 times by covering the trench with a photoconducting material, according to Hitachi researchers. □

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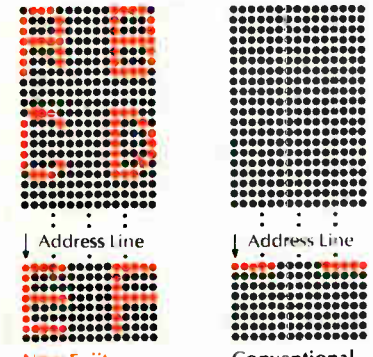

New Fujitsu memory-type display
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FUJITSU

INTERNATIONAL WEEK

CHINA LAUNCH FOR SATELLITES EYED

Bundespost, the agency that runs West Germany's public communications lines, is considering contracting with China to launch its TV broadcast and communications satellites into orbit if failures and setbacks of European-made launchers such as the Ariane continue their delays. Chinese aerospace authorities have assured Bundespost officials that they can ready their "Long March" rockets to launch West Germany's TV-SAT 2 broadcast satellite by 1990. The German officials visited China in April. They say they are convinced of the reliability of the launchers, which cost about one third less to use than comparable launchers from the U.S. or Europe.

JAPAN OKs MORE PHONE PRODUCTS

The Japan Approvals Institute for Telecommunications Equipment, an agency of the Ministry of Posts and Telecommunications, has approved 1,716 telecommunication terminal products, including foreign-developed products, for the year, a 50% increase over the 1,051 for 1985. These terminals are approved for connection to public and private telephone circuits in Japan.

UK ROBOT MARKET DECLINES SHARPLY

The robot market in the UK is declining sharply, according to the British Robot Association. Only 475 robots, worth $20.6 million, were installed in 1986, compared with 585 in 1985, a drop of 20%. The 1985 figure was 27% below 1984's 870. John Collins, president of the association, believes the market will flatten out this year and 400 to 500 robots will be installed in the UK this year. The number of robots imported from the U.S. has reduced to a trickle—11 in 1986, compared with 114 in 1985.

SUPERCONDUCTOR WORKS AT –185°C

Plessey Research and Technology Ltd. has developed a superconductor that will work at –185°C, 88 degrees above absolute zero. The material used is a new type of ferroelectric ceramic developed by the Caswell, UK, company that is normally an electrical insulator but which superconducts at low temperatures. Plessey will use the material to build a SQUID, or Superconducting Quantum Interference Device.

HP SINGAPORE TO OPEN WAFER FAB

Hewlett-Packard Singapore will pour an additional $42.5 million into a wafer diffusion plant and research and development. Work has begun on the $23.6 million wafer-diffusion facility, which will start producing gallium-arsenide chips next April and gallium-phosphide wafers in 1990. It will also double its engineering force to 200 over the next five years.

MITSUI SEES NEW USE FOR BAR CODE

Mitsui and Co. is asking for help from telecommunications-equipment manufacturers, printing companies, and other related businesses to develop equipment for a new bar code market niche: printers that can print bar codes onto business cards or into private telephone directories and sets equipped with a bar code scanner for automatic dialing. Mitsui is targeting Japan's new operating companies, Teleway Japan Corp., Daini Denden Inc., and Japan Telecom Co. They plan to start long-distance phone services this fall between Tokyo and Osaka, charging 20% to 30% less than Nippon Telegram and Telephone Corp. But because subscribers will have to dial four more digits than the 9 or 10 digits used by NTT, Mitsui planners have the idea of using bar code scanners for automatic dialing. The telecom manufacturers would be creating a new market, and Mitsui would receive royalties.

TI OFFERING BiCMOS LOGIC IN JAPAN

The BiCMOS bus interface logic ICs recently developed by Texas Instruments will soon be available in the Japanese market. The ICs, SN74BCT and SN74ABCT series, will initially be available as 8-, 9-, and 10-bit products, including latches, buffers, and transceivers. TI Japan Ltd., Tokyo, will import and begin to supply samples of 46 devices in the two series in June, and production quantities will be available late in the third quarter. Both center-pin and end-pin ground configurations will be available for 300 to 400 yen.

UK BOOK TO BILL DECLINES SLIGHTLY

The UK book-to-bill ratio is still above parity, even though the provisional figure for April dropped from March, says the Electronic Component Industry Federation. Though the provisional 1.15 for April is down from the revised 1.29 for March, it still represents the fifth month in a row that the ratio has been above one.

SIEMENS RECORDS 18% SALES GAIN

Siemens AG, West Germany's No. 1 electronics/electrical producer, registered a whopping sales gain of 18% during the first half of fiscal 1987, which ends Sept. 30. Worldwide gross sales for the six-month period jumped to 26 billion deutschmarks, or $14.5 billion, up from 22 billion DM, or $12.3 billion, during the same six-month period in 1986. The Munich company attributed the increase primarily to the expansion of its domestic markets.

TOKYO POLICE RAID SOFTWARE HOUSE

Tokyo Metropolitan police raided eight offices of Ma's Marketing Co. to investigate allegations that the Tokyo company was copying and selling 3,000 types of personal-computer software programs owned by IBM Corp. and several major Japanese software houses. The firm, which was established in 1982, has been accused of selling copied software for IBM's PC series for about 20% of the price set by IBM. The search followed a complaint filed in March by IBM claiming that a large quantity of pirated IBM software was being sold in Japan at low prices.

PHILIPS FACTORY FOR PC BOARDS

Philips has gone on stream with a factory for multilayer printed-circuit boards that the Dutch company believes to be Europe's most advanced facility. The development and manufacturing facility, in Brussels, turns out double-sided and multilayer pc boards for through-hole and surface-mount technologies. It can also produce in full volume boards with buried and blind holes.

W. EUROPE'S PC MARKET UP SLIGHTLY

The Western European personal-computer market grew 2.5% during 1986 after a 0.5% decline in 1985, according to International Data Corp. of London. In 1986, 5.27 million units were installed, compared with 5.13 million in 1985. The strongest growth was in the business and professional sector, with a 33% increase from 1.41 million to 1.88 million in 1986.

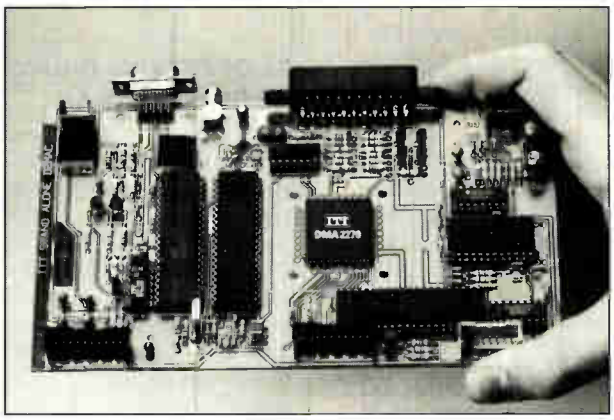
INTERNATIONAL PRODUCTS

CHIP FOR TV SET CAN DECODE DIRECT SATELLITE BROADCASTS

IC FROM ITT'S INTERMETALL UNIT HANDLES PROPOSED D2-MAC STANDARD

An integrated circuit from Intermetall GmbH uses 1.5-μm CMOS technology to provide a compact, 7.2-by-7.1-mm package that can do complete decoding of television signals broadcast directly from satellites. With the DMA2270, television designers can begin to build that capability into their receivers well in advance of Europe's first broadcast-satellite launch, which is scheduled for early next year.

Intermetall—a division of the Freiburg, West Germany-based ITT Semiconductors Group—claims the DMA2270 is the first decoder to be marketed for the complex D2-MAC signals. D2-MAC is based on a time-division-multiplexed transmission of video signals called Multiplexed Analog Components—MAC, for short. The D2 stands for digitally encoded sound and data signals, organized in packets and coded in duobinary form.



DIGITAL TV. Intermetall's DMA2270 signal decoder can accommodate digital television simply by adding a few standard ICs.

NEW STANDARD. The French-proposed D2-MAC standard is favored by most European countries because it provides better receiver performance than current color transmission standards, such as NTSC, PAL, and Secam. The improvements include the elimination of cross-color and cross-luminance, better chrominance-noise performance, and an ability to transmit digital sound as well as data services such as teletex and pay-TV.

Intermetall's 2270 decoder fits easily into the digital TV concept, Digit 2000, promoted by ITT Semiconductors [*Electronics*, April 5, 1984, p. 89]. But by adding a few standard ICs, such as analog-to-digital and digital-to-analog converters and clocks, the decoder can be designed into other digital or analog chassis as well, says Hermann Zibold, leader of the 2270 design team. The 2270 can expand existing digital TV systems into multistandard systems capable of handling the NTSC, PAL, Secam, and D2-MAC signals.

In a TV receiver, the 2270 performs three basic functions: video processing, clock and data recovery, and sound/data processing. For these tasks, the device functions as a real-time signal processor whose array of circuits amounts to a powerhouse of processing stages.

Besides a code converter and a duobinary decoder, the 2270 incorporates clamping circuits, the chroma and luma stores for MAC signal expansion, and chroma and luma interpolating filters. There is also a contrast multiplier with a limiter for the luminance signal.

The device also contains a color saturation multiplier with a multiplexer, a synchronization circuit, a descrambler, and a de-interleaver. Other circuits include a packet linker and a packet buffer, a sound decoder and sound multiplexer, and an IM (for Intermetall) bus-interface circuit, which provides communication with the receiver's central control unit.

Technologically, "what enabled us to pack so much on a chip only 52 mm² in size is a 1.5-μm CMOS process," Zibold says. "That's the only way to do it." The 2270, a programmable VLSI circuit, packs 150,000 transistors on the 7.2-by-7.1 mm chip.

Housed in a 68-pin plastic leaded chip carrier, the device consumes 300 mW of power. It operates on a 5-V supply and is designed for an ambient operating temperature range from 0° to 65° C. The device weighs about 4.5 grams.

Samples of the DMA2270 are now available. As soon as volume production gets started at the end of June or early July, the device will be available in large quantities from stock. Large-order unit pricing ranges from $20 to $25, depending on volume. *–John Gosch*

Intermetall GmbH, P.O. Box 840, D-7800 Freiburg, West Germany.
Phone 49-761-5170 [Circle 500]

CODEC SHRINKS VIDEO IMAGES TO CUT COSTS

Vistacom Industries Inc.'s Video Codec 64 compresses motion-and-color television images by a ratio of 1,500:1 for economical transmission between videophones over 64-Kbit/s telephone lines.

Compressing the information means telephone costs can be significantly reduced. Designed for use in the company's Vistacom videophone system, the codecs consume 50 W of power, compared with up to 1,000 W for competitors. They weigh 12 kg and measure 47×15×47 cm.—approximately a third smaller than competitive equipment. A 56-Kbit/s codec is available for the U. S. market. Pricing is not yet available.

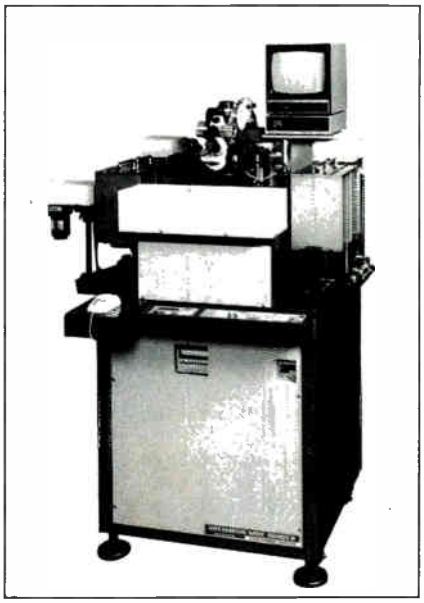
Vistacom Industries Inc., Oy, Kipparinkatu 2, SF-02320 Espoo, Finland.
Phone 358-0-802-5011 [Circle 701]

WIRE BONDER OFFERS PULL-TESTER OPTION

A fully automatic wire-bonding system for heavy aluminum wire has been designed by Hakuto Co. Ltd. to handle a wide range of production needs.

The UWB-301-FA can be configured with a pull-tester directly linked to the bonder to provide nondestructive testing

of the product. A special unit for forming loops is also available. Other features include a computer-based control system, a monitor, a pattern recognition



system, and a large work table. Price depends on the importing country.
Hakuto Co. Ltd., 1-1-13 Shinjuku, Shinjuku-ku, Tokyo 160, Japan.
Phone 81-3-341-2611 [Circle 702]

ADC RUNS FAST AT UP TO 16-BIT RESOLUTION

The SYS68K/AD-10/11 series of analog-to-digital converter boards from Force Computers GmbH features conversion rates down to 4 μs and resolutions up to 16 bits. The AD-10 board has 32 single-ended or 16 differential analog input channels with 12-to-16-bit resolution. In order to provide full analog-output control functions, the AD-11 board can incorporate two additional analog output channels.

The capabilities of the AD-10/11 boards may be expanded by an optional expansion interface. This interface provides channel and control information, available via a 25-way connector on the front panel of each board. The expansion bus expands the number of input channels to 256.

Available from stock, the boards have a two- to four-week delivery time. Price ranges from 5,000 to 7,000 DM, depending on resolution and conversion time.
Force Computers GmbH, Daimlerstr. 9, D-8012 Ottobrunn, West Germany.
Phone 49-89-600910 [Circle 703]

PHOTORESISTS TARGET SUBMICRON DEVICES

Designed for dry-etching techniques in VLSI fabrication, Dage Ltd.'s CMS series of negative photoresists yields accurate line spacing as small as 0.8 μm.

The CMS-EX products are targeted at master-mask fabrication and direct writing on wafers using electron-beam lithography. The CMS-DU products handle printing of extremely fine mask patterns on silicon using deep-ultraviolet lithography.

The EX and DU product lines can be used in the fabrication of devices following 1.5-μm and 1-μm design rules, respectively. Metal-ion content is less than 0.01 parts per million, and shelf life exceeds one year. Available now, the products cost approximately £1,100 per liter, but price depends on importing country and volume purchased.
Dage Ltd., Intersem Div., Rabans La., Aylesbury, Bucks HP19 3RG, UK.
Phone 44-296-393200 [Circle 704]

COLOR CRT ADJUSTS TO INPUT VOLTAGE

The power supplies in Electrohome Ltd.'s ECM 1300 Vari-Scan series of color monitors automatically adjust to any input voltage between 90 and 240 V to relieve end users, distributors, and dealers in importing countries from the responsibility of making the adjustment for their particular country.

The ECM 1310 and 1311 also automatically sense and lock in on frequency inputs from 15 to 34 KHz.

A tinted cathode-ray tube provides up to 10% more light transmission than previous models, which makes the screen brighter and easier to read in high ambient light. Available now, the monitors cost U. S. $1,198.
Electrohome Ltd., 809 Wellington St. N., Kitchener, Ontario, Canada.
Phone 519-744-7111 [Circle 705]

REPAIR PHOTOMASKS IN HALF THE TIME

A one-step photomask-repair system from NEC Corp. uses an ultraviolet laser beam within a chemical-vapor-deposition chamber to repair defects in less than half the time required by competitive pyrolytic-CVD or focused-ion-beam systems.

The YL454A generates a repair patch of chrome film less than 0.2 μm thick without requiring a chrome seed. The patch remains intact under normal photomask-process conditions.

The system repairs masks for 1×, 5×, and 10× wafer steppers. It uses a single-wavelength laser to repair both clear and opaque defects, a technique that both improves placement accuracy and decreases maintenance costs.

The system is available one month after order and costs 124 million yen.
NEC Corp., 5-33-1 Shiba, Minato-ku, Tokyo 108, Japan.
Phone 81-3-454-1111 [Circle 706]

PC COMPATIBLE RUNS 10 TIMES FASTER

Applied Microsystems Technology Ltd.'s AMT 286xii microcomputer runs at 6-, 8-, and 12-MHz clock speeds and offers 1 Mbyte of RAM. Although compatible with IBM Corp.'s Personal Computer, it runs as much as 10 times faster.

Based on an Intel Corp. 80286 microprocessor backed up with CMOS VLSI technology on the motherboard to enhance performance and reduce power consumption, the system offers as standard equipment a 1.2-Mbyte floppy disk, a 20-Mbyte hard disk, and both serial and parallel interfaces.

The basic model comes with a 14-in. high-resolution monitor and supports Hercules, CGA, EGA, and PGA graphics. Available now, it costs £1,999. Equipped with an optional 40-Mbyte hard disk, the system costs £2,449; and with an 80-

Mbyte hard disk it sells for £2,899.
Applied Microsystems Technology Ltd., 249 Cricklewood Broadway, London NW2 6NX, UK.
Phone 44-1-450-3222 [Circle 707]

REED SWITCHES RUN 1 BILLION OPERATIONS

A new series of reed switches from Philips Elcoma offers a combination of high reliability and long life. Their contact resistance of 70 mΩ varies insignificantly over a billion switching operations.

Packaged in a compact 2.54-mm-diameter by 15-mm-long gas-filled glass capsule, the RI-25 switches have a switching range from 300 mW to 25 W. They are single-pole, single-throw types with normally open contacts and two magnetically activated reeds.

The products target applications in computer keyboards, telephones, test equipment, and automotive systems.

The 25AAA has a maximum switching capacity of 8 W; the 25AA, 15 W; the 25B and 25C, 25 W. Maximum voltage is 200 V dc or 140 V ac, and maximum current is 1 A. Samples are available

WHATEVER THE CHALLENGE

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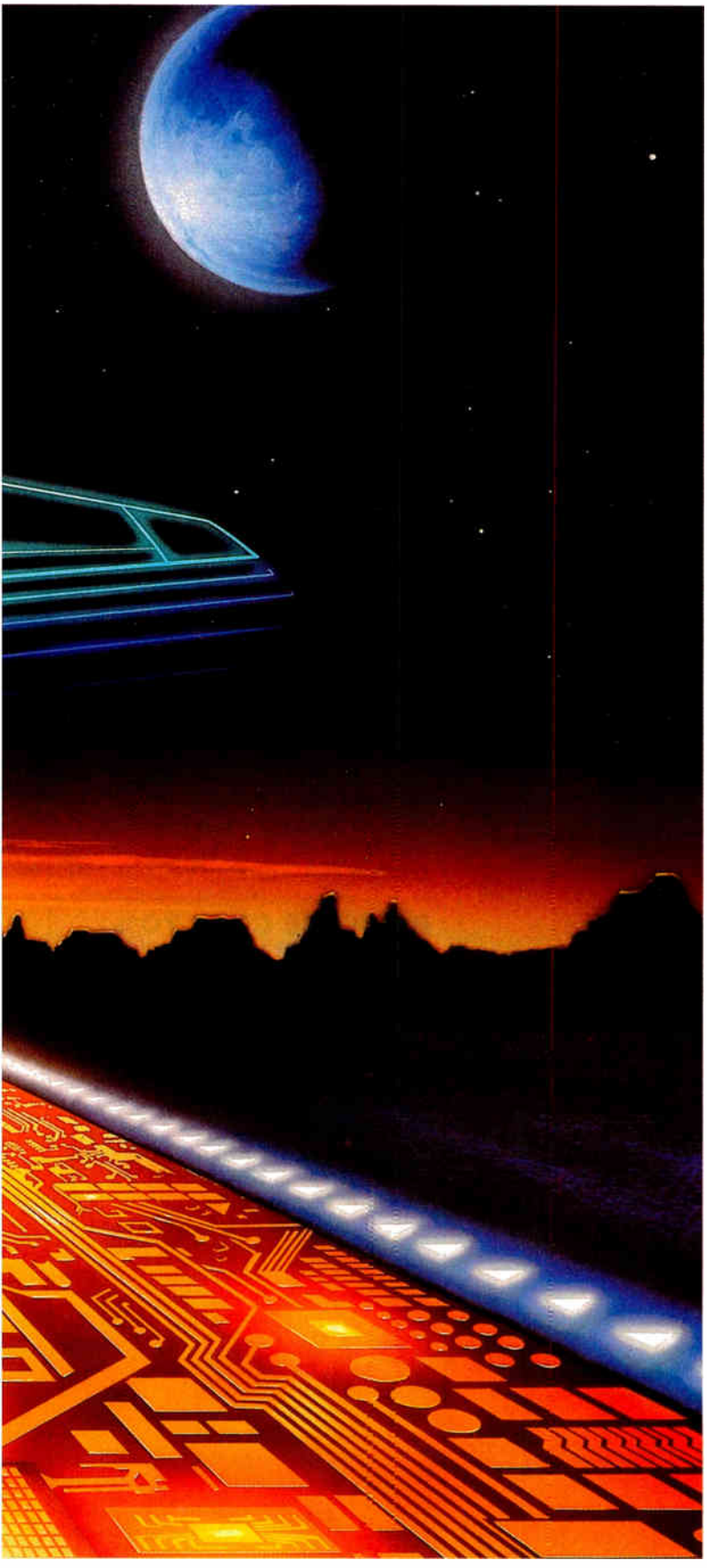

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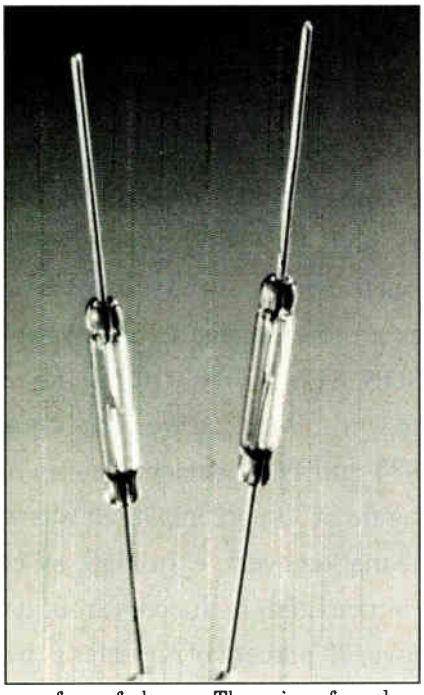


now free of charge. The price of production purchases depends on the importing country, but a typical quote in the Netherlands for 100 of the 25AAA parts is 50 Dutch guilders.

Philips Elcoma, P. O. Box 523, 5600 AM Eindhoven, The Netherlands.
Phone 31-30-757005 [Circle 709]

PORTABLE RS-232-C TESTER COSTS £75

Compucorp Ltd.'s portable, in-line communications tester for RS-232-C serial interfaces offers tristate monitoring on all signal pins and two-level open-circuit voltage testing capability for just £75.

Designed for use by service personnel, computer engineers, and peripherals suppliers, the Computext Comtest requires no batteries. A guide to CCITT and EIA abbreviations, including identification of originating signals, pin numbers. and descriptions, is included on the back panel.

Compucorp Ltd., Cunningham House, Westfield Lane, Kenton, Middlesex HA3 9ED, UK.
Phone 44-1-583-5112 [Circle 708]

SOLDERER WORKS ON MOST SURFACE MOUNTS

A modular soldering system from Tamura Corp. can handle a variety of surface-mounted devices, including plastic leadless chip carriers, dual in-line packages, and small-outline integrated circuits.

The Model SC30-80SPF can be configured to accommodate specific manufacturing processes by adding or deleting modules. The system consists of six independent units, each handling one of the system's major operations: loading, precleaning, soldering, rinsing, drying, and unloading.

Other features include fully automatic loading and unloading modules and a solder unit that can be adapted for either wave or dip soldering technology. The system can be laid out in either C or L configurations.

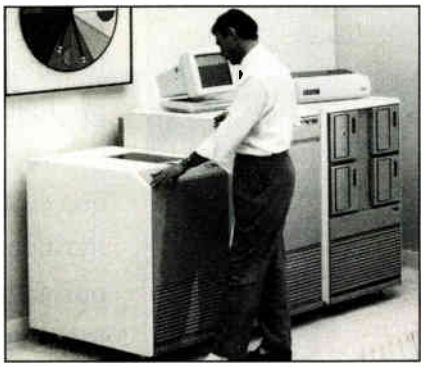
Available now, the system costs 45 million yen. Delivery takes three months after order.

Tamura Corp., 1-25-1 Nishi Shinjuku, Shinjuku-ku, Tokyo, Japan.
Phone 81-3-354-0781 [Circle 710]

HONEYWELL COMPUTERS CAN LINK 1,000 USERS

Honeywell Bull Ltd.'s DPS 7000 series of five departmental computers supports transaction-processing capability ranging from 8,500 to 51,500 transactions/hr and connections to up to 1,000 work stations. They continue compatibility with the company's GCOS 7 operating system.

Models 10, 20, 30, and 40 are all upgradable through the line to the high-performance Model 50, which can handle



up to 300 user stations simultaneously.

A twofold performance increase over the company's previous system is achieved by incorporating 64 Mbytes of cache memory, a 27-Mbyte/s bus capable of handling 130-bit words, and 25-Mbyte/s input/output channels.

The machines will be available in the third quarter. Price depends on model and options. Typical system prices are £119,000 for an entry-level system and £423,000 for a top-of-the-line model.

Honeywell Bull Ltd., Honeywell House, Great West Road, Brentford, Middlesex, TW8 9DH, UK.
Phone 44-568-9191 [Circle 712]

FUNCTION GENERATOR HANDLES WIDE RANGE

The AFGU function generator from Rohde & Schwarz handles signal-generator requirements for a wide range of applications: analog and digital technology, electroacoustics, vibration measurements, materials testing, automatic control, and biomedicine. Over a frequency range from 1 μHz to 20 MHz, the AFGU produces sine-wave, triangle, square, trapezoid, and pulse signals of synthesizer quality. User-specific waveforms can be generated as desired, using the "arbitrary" functions module.

A 4-Kbit parameter memory with a resolution of 10 bits is available. Start and stop addresses can be set to produce either curve segments or whole

curves. The wide output voltage range for all signal waveforms extends from 0 up to 30 V. The dc offset voltage of the output signal can be adjusted by up to ±15 V.

The AFGU features a wide variety of modulation modes: internal and external frequency-shift keying and pulse modulation; external amplitude-modulation; frequency modulation; and voltage-controlled oscillation. The sweep mode is particularly convenient, allowing start-and-stop frequencies, sweep time, time between two sweeps, and as many as four marker frequencies.

Delivery time for the AFGU function generator is two to three months after receipt of order. Its price in West Germany is 18,500 DM.

Rohde & Schwarz, Muehldorfstr. 15, D-8000 Munich 80, West Germany.
Phone 49-89-41292625 [Circle 711].

PACKAGE CUTS 70% OF SOFTWARE COSTS

Axion, a software-maintenance package from British Telecom plc, provides users a means of automatically documenting software development projects. It can save up to 70% of the cost of developing and managing a large, complex software project.

The savings are realized by allowing programmers of real-time control systems to concentrate their time on software specification and design instead of documentation chores.

The first products in the package are: Kindra, a program suite for producing design diagrams and coding them into C, Pascal, Coral, and PL/M; Asym, a control tool for common software problems; and Kalix, which facilitates graphical programming without special graphics terminals and plotters.

Available now, the tools run on most standard computers and cost £300 to £2,000 per user, depending on computer.

British Telecom plc, Martlesham Heath, Ipswich IP5 7RE, UK.
Phone 44-345-959111 [Circle 713]

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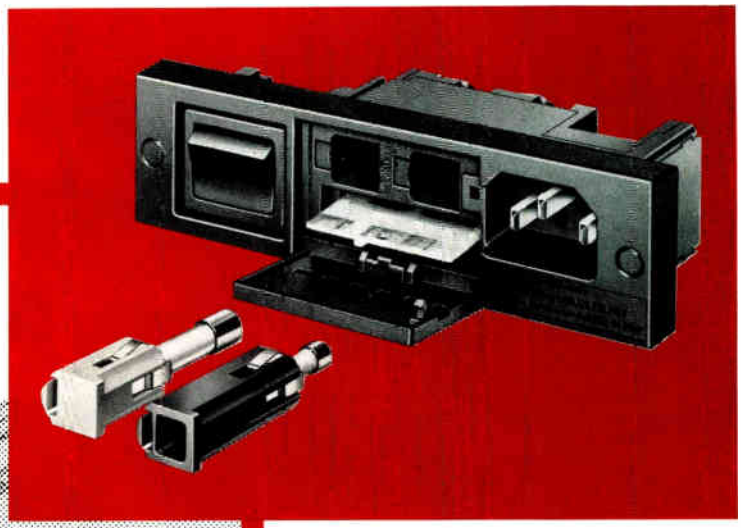
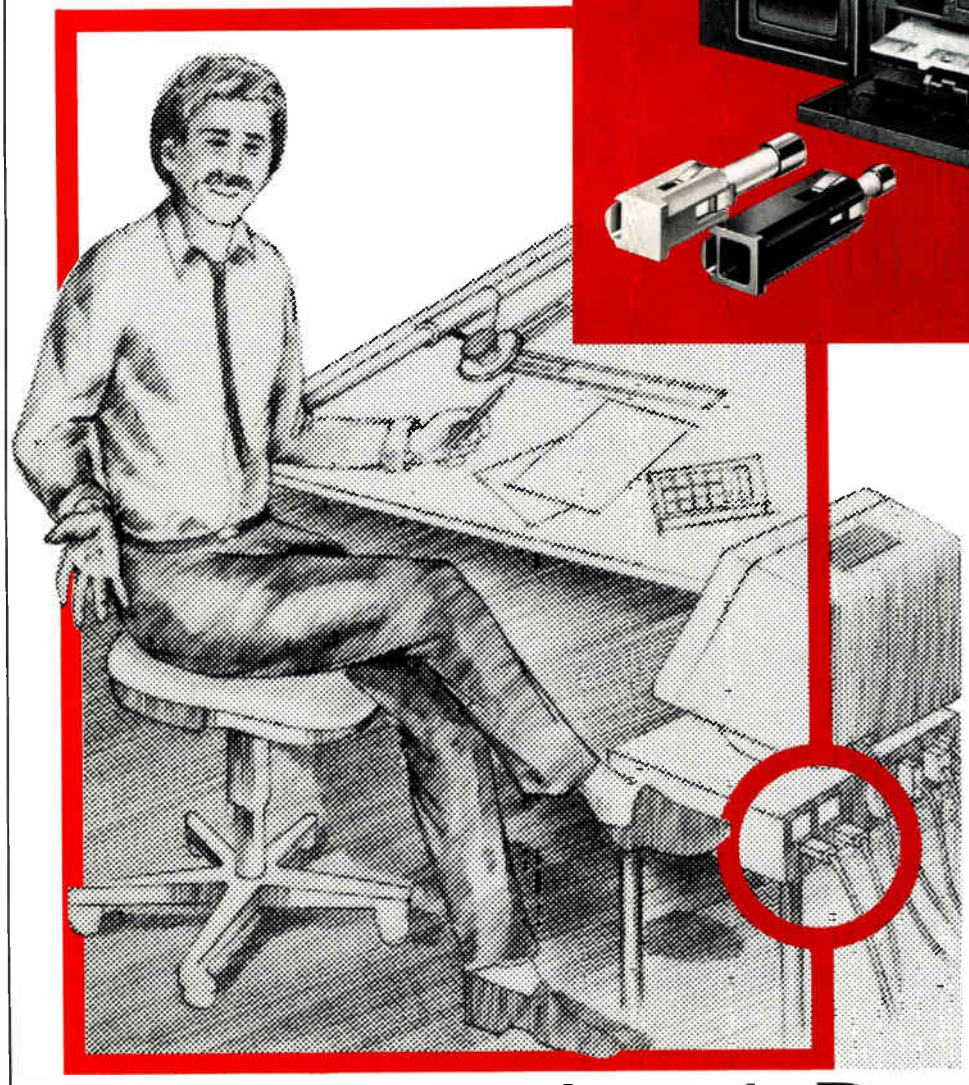
Power Module





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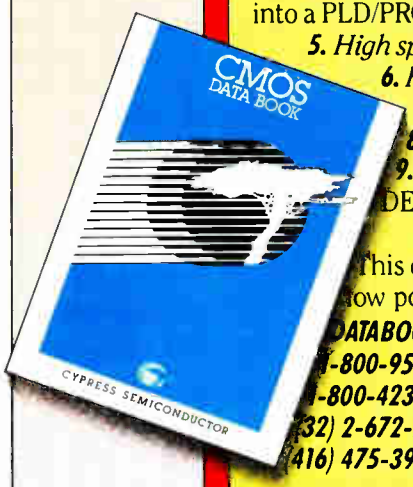

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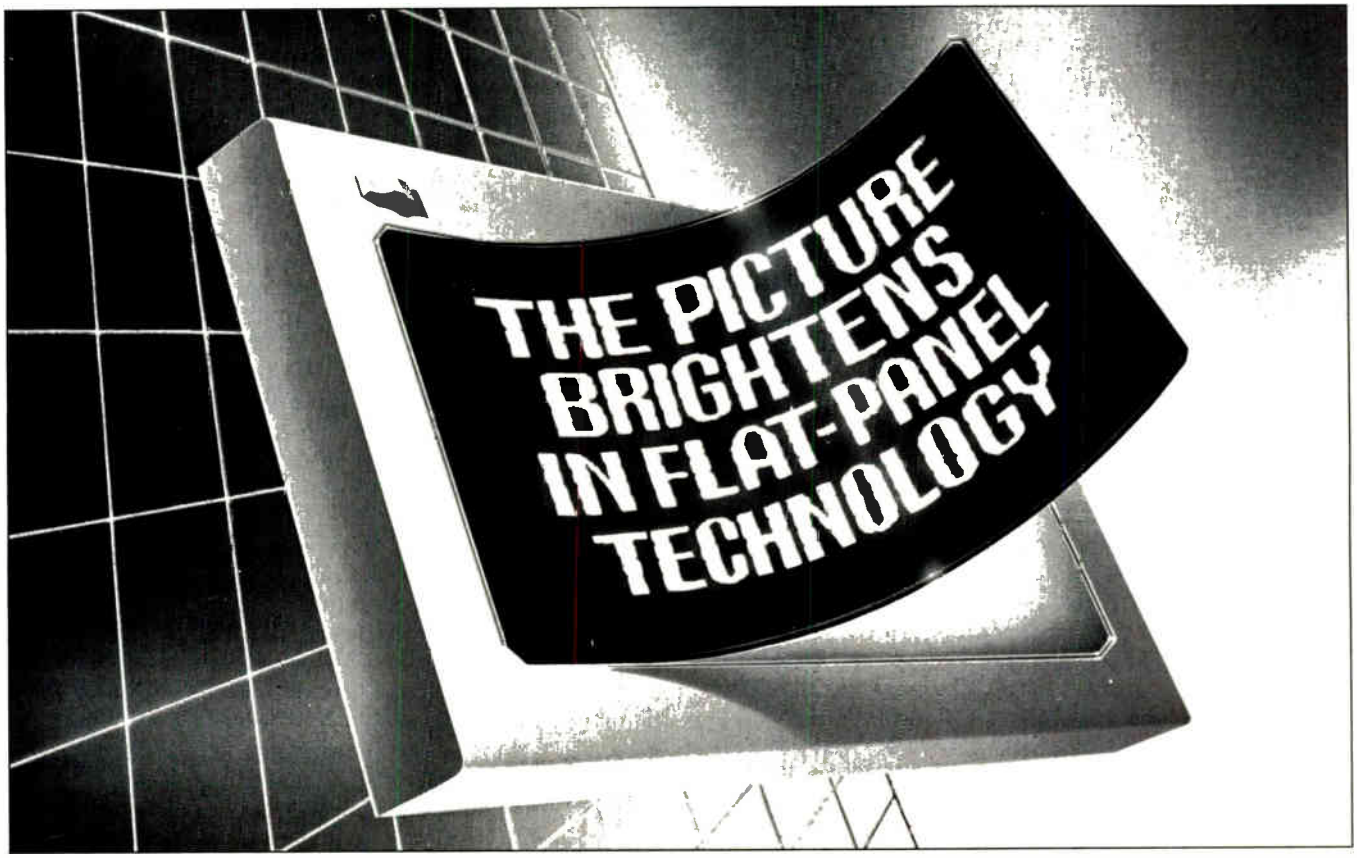


by Tom Manuel

For a decade and more, system engineers have wanted to design-in flat-panel displays that were bright and crisp, but still affordable. Most designers are still waiting, but what they seek is getting closer. And several of the niche flat-panel technologies are beginning to move into the mainstream.

Until recently, these flat displays have had more than their share of drawbacks. They often were monochromatic, came with a smaller display size, and offered lower contrast and resolution. They also cost a lot more than cathode-ray-tube displays. And none of the flat-panel technologies—electroluminescent, liquid-crystal, or plasma—offered one single approach that could be applied to a wide range of display applications. Flat panels are now used where their thin profile—and in some cases low power and ruggedness—outweigh relatively high costs.

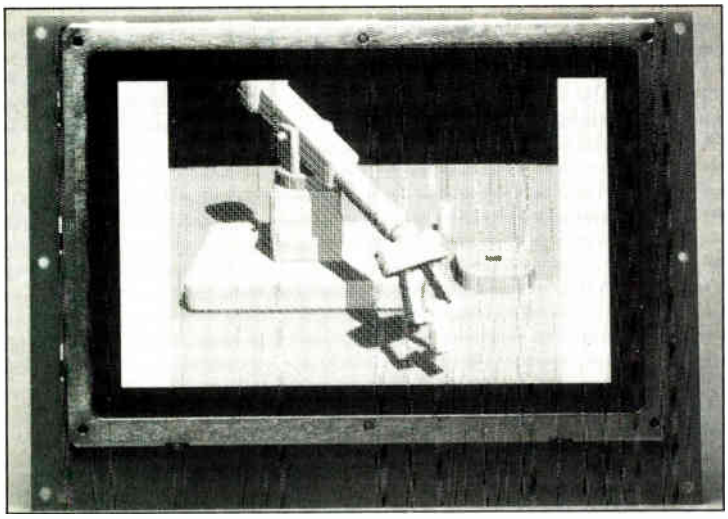
Flat-panel developers had long aimed at practical panels with high resolution and contrast that could be viewed over the same wide angle as a printed page, panels that could be seen equally well in both dim and bright light, and that could render the full-color visible spectrum with a nearly infinite gray scale. CRTs more-or-less competed in all but thinness, but they also shared serious drawbacks for some applications: they were bulky, fragile, and power-hungry. The CRT simply could not be used in such applications as portable computers or in such harsh environments as the factory and in space.

Meanwhile, flat-panel technologies were improving and finding niche markets where particular characteristics were important. Now two significant developments are likely to help push electroluminescent displays out of their niche markets into some mainstream applications. Cherry Corp. is introducing a thick-film, direct-current EL technology (see p. 58) that promises much lower costs than state-of-the-art thin-film EL displays.

Full color seems to be in the offing now for thin-film EL displays. Two-color TFEL prototypes have been produced at Planar Systems Inc., and successful experiments conducted on full-color versions. Planar is forging ahead to deliver a three-color prototype by the end of the year (see p. 63), but affordable commercial versions still appear to be a couple of years away.

Liquid-crystal technology is moving ahead at a rapid clip, too—even in the U.S., which gave up an early lead to Japan. Tektronix Inc. is unveiling bright LCDs with high contrast and a wide viewing angle. Its Hypertwist LCD modules come from work done at its imaging research lab in making the optical effect known as supertwisted birefringence a commercial reality (see p. 60).

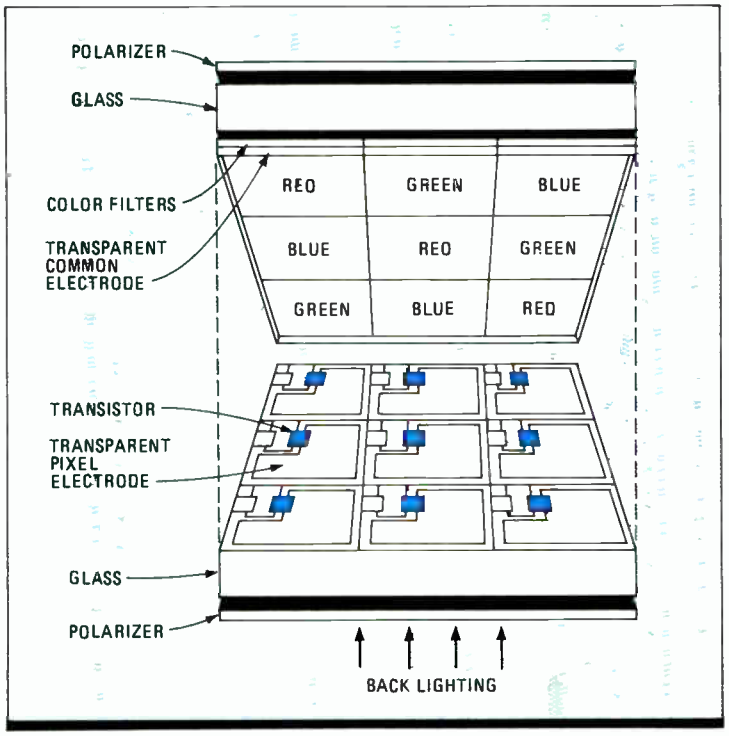
And coming soon are more flat-panel displays that



1. CRT QUALITY. EL displays such as this one made by Planar show high-resolution images of CRT quality or better.

will match or surpass the display quality of high-resolution color CRTs. They will find a ready market in applications where CRTs are impossible or very difficult to use. In addition, if the price is right, the more convenient flat panels will replace CRTs in many traditional applications such as desktop work stations and TV.

Advances in the three most important flat-panel display technologies—EL, liquid crystal, and gas plasma—are legion. They hold out the promise for spectacular and exciting products just over the horizon, such as full-color, high-resolution flat-panel displays as small or as large as needed that have low power requirements.



2. COLOR LCD. Filters of the three primary colors are matched to the pixels in this proposed structure for a full-color thin-film-transistor LCD module.

Monochrome flat-panel displays also have important roles to play in the market. The monochrome versions of the important flat-panel technologies are advancing on several fronts—getting larger, brighter, more reliable, easier to make, and less expensive to buy.

EL displays are light-emitting and deliver bright images with high resolution (see fig. 1). Rugged and reliable, they are available in very thin packages. With these features, EL displays appear to be ideal choices for many applications. Unfortunately, they have been too costly or too power-hungry for many uses.

Several significant developments in EL technology have occurred in the past year, with more expected over the next few years. Color is a major development. The most significant trends in monochrome are continued cost and power reductions. Components, especially integrated circuits, are getting less expensive; manufacturing processes are improving; economies of scale are beginning to take effect; and the development of a thick-film technology promises to significantly lower the overall manufacturing cost.

For the first thick-film EL display, Cherry Electrical Products Corp. of Waukegan, Ill., and Siliconix Inc. of Santa Clara, Calif., teamed up to develop both the thick-film direct-current EL technology and new driver electronics. The manufacturing process promises to significantly drop the price of EL displays. The result is a commercial version of a very bright dc EL display system that requires low voltage, is free of catastrophic failures, and is economical to produce.

Four proprietary ICs for constant-current drive electronics were jointly designed by Cherry and Siliconix engineers and are being fabricated by Siliconix. These drive chips provide a fast frame rate of 240 Hz and a current-limited drive, which produces high brightness without excessive heat buildup that could damage the phosphor. The circuits make it possible to exploit the low cost of thick-film dc EL display technology by providing drivers that give the display the long life and brightness it needs to compete with other EL technologies.

Exciting progress is also being made by U. S. and Japanese manufacturers in bringing color to EL displays. In the U. S., Planar is building its full-color thin-film EL display with a patterned red-green-blue phosphor for the U. S. Army. The Beaverton, Ore., company plans to demonstrate a product within the next 12 months. It has successfully built two-color stacked-phosphor displays and is well on its way to perfecting the three-color technique.

Several other projects for color EL displays were reported at the 1987 conference of the Society for Information Display in New Orleans in mid-May. For example, the NTT Electrical Communications Laboratories in Ibaraki, Japan, have developed a prototype of a two-color patterned-phosphor color EL display and proposes extending it to three col-

ors. The NTT researchers have successfully fabricated a two-color device to demonstrate the feasibility of color EL displays. The laboratories' approach to full-color, like Planar's, is with patterned phosphors. NTT engineers are planning to use active-matrix addressing for their color display.

In another research project in Japan, the electronics department of Tottori University is developing a full-color EL display with a two-color stacked phosphor and embedded filters to add the third primary color for the full-color spectrum. The two stacked phosphors will emit blue-green and red light, respectively. The researchers are putting pass filters with short and long wavelengths side by side over the blue-green phosphor to produce the blue and green primary colors. On top of this they will place a transparent red-emitting phosphor. To produce all colors, they will mix blue with green spatially, and then, as needed, add red to these colors coincidently.

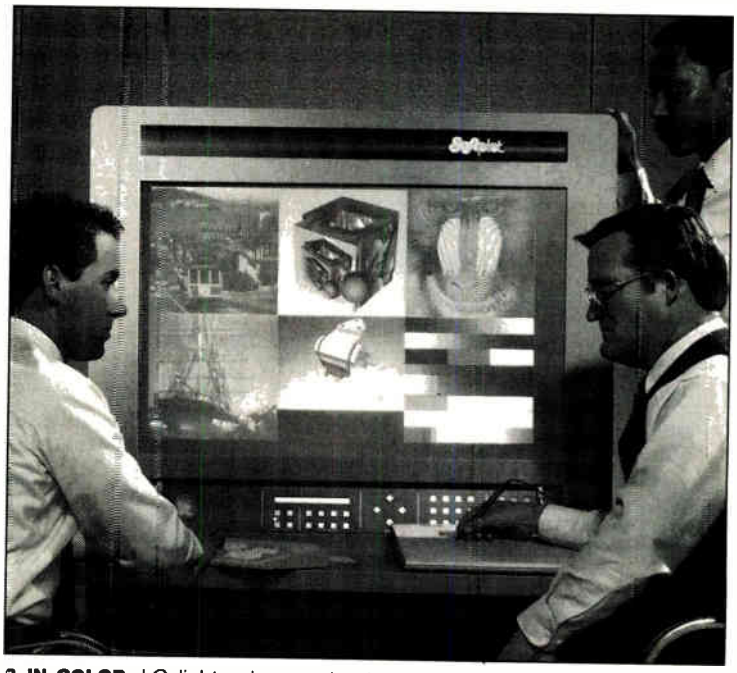
Several more papers at the conference were on improvements to monochrome EL displays. They focused on efficiency improvements and experiments with colors other than the common red-orange of phosphors made from zinc sulfide doped with manganese, such as a bright green terbium-fluoride-doped ZnS phosphor.

Flat-panel display innovations are not limited to EL technology. LCDs are getting their fair share of research and development. Tektronix is working with the supertwisted birefringence effect, and larger SBE panels are on the way. Standard twisted-nematic and the newer supertwisted-nematic LCD technologies are not standing still. Enhancements continue to be made, and, for certain applications, these technologies will be useful for possibly another decade.

The Tektronix HyperTwist SBE is a very bright, crisp LCD display. Engineers developed HyperTwist by imparting an optimum 270° twist to the liquid-crystal structure and adding just the right amount of birefringence—light refracted into two slightly different directions—to obtain high contrast and a wide viewing angle. Tektronix is the first to produce SBE displays commercially, with two products offered. Although these displays are small—128 by 128 pixels and 128 by 256 pixels—Tektronix has plans to offer larger panels.

A UK company is achieving similar results in resolution and viewing angle. STC Technology Ltd. is using a smectic-A liquid-crystal technology. The Harlow company has developed a material that it says can lead to LCDs with unlimited resolution, on-screen memory, and a viewing angle as wide as anyone can read [*Electronics*, April 30, 1987, p. 39]. Samples of the material, based on smectic-A cyano-biphenyls, are available.

One of the most interesting and lively fields of LCD R&D is the active matrix or active substrate, where active circuit elements such as diodes and transistors are built into the LC layers as part of each pixel during the display fabrication process. This process allows much higher resolutions and larger area displays; and because the pixels can be smaller, active-matrix LCD technology holds the promise for high-resolution, full-color displays.



3. IN COLOR. LC light valves and a laser show engineering drawings on a Greyhawk paperless plotter.

Terry Scheffer, principal engineer and scientist at Tektronix, has suggested a way to build a color LCD with a thin-film transistor matrix (see fig. 2). The method incorporates mosaic filters of the three primary colors that are precisely registered to the pixel electrodes on the lower substrate. The filters are placed inside the liquid-crystal cell to eliminate parallax. Thin-film transistors are fabricated for each pixel.

Many of the TFT color LCD developments are in Japan. Seiko Instruments Inc. for example, reported success in developing a 14-in.-diagonal active-matrix three-color display with a resolution of 640 by 440 pixels. It is driven by new TFTs—which the Chiba company's engineers call V²-TFT for very simple and very thin thin-film transistor—that can be fabricated in three photolithographic steps.

The engineers at Seiko have also developed an active diode-matrix LCD that is 9.8 in. diagonally with 640 by 400 pixels. It can be fabricated with only two masks—holding the promise of very low-cost production.

Elsewhere, Seiko Epson Corp. in Nagano, Japan, has designed a diode active-matrix full-color LCD, using a metal-insulator-metal diode comprising tantalum, tantalum oxide, and chromium [*Electronics*, May 14, 1987, p. 32]. The largest display with this technology measures 6.7-in. diagonally with 440 by 640 pixels. Seiko has used the technology to make portable color TVs.

An Exton, Pa., company, LC Systems Division of Eagle Picher Industries Inc., has developed a

FLAT-PANEL DISPLAY MAKERS ARE DISTRIBUTED ACROSS THREE MAJOR TECHNOLOGIES

Electroluminescent		Liquid crystal		Plasma	
Cherry	(U.S.)	Epson	(Japan)	Fujitsu	(Japan)
Fujitsu	(Japan)	LC Systems	(U.S.)	Hitachi	(Japan)
Lohja	(U.S.)	Matsushita	(Japan)	IBM	(U.S.)
NEC	(Japan)	Mesa State Technology	(U.S.)	Lucitron	(U.S.)
NTT	(Japan)	Sanyo	(Japan)	Magnavox Electronic Systems	(U.S.)
Planar Systems	(U.S.)	Seiko Instruments	(Japan)	Matsushita	(Japan)
Sharp	(Japan)	Sharp	(Japan)	NEC	(Japan)
Sigmatron Nova	(U.S.)	STC Technology	(UK)	Photonics Technology	(U.S.)
		Tektronix	(U.S.)	Plasma Graphics	(U.S.)
		Toshiba	(Japan)		

640-by-200-pixel MIM active-matrix display with a 10:1 contrast ratio and a wide 90° viewing cone [*Electronics*, Sept. 18, 1986, p. 104].

Liquid-crystal structures are used for more display products than just direct-view displays of the liquid crystal itself. They are used as shutters to produce color from very high-resolution monochrome displays as in the paperless plotter products made by Greyhawk Systems Inc. (see fig. 3). Seiko Epson has developed a high-resolution full-color video projector using active-matrix liquid-crystal light valves [*Electronics*, May 14, 1987, p. 33]. Three twisted nematic liquid-crystal light valves with very small polysilicon TFT transistor drivers each deliver 440 by 480 pixels in one primary color. The optical characteristics of the LC material are set individually for optimum contrast for the red, green, and blue light valves. This device projects a full-color video image with 350 TV lines, a 50:1 contrast ratio, and a linear gray scale.

Kodak is using liquid-crystal technology for two of its most recent products, a projection pad for a transmissive overhead projector and a computer-data projector. Both come with set-up software and allow monochromatic projection of screens from IBM PC and compatible machines. Two other companies are also offering LCD-based computer display panels for overhead projectors: Sharp Electronic Corp. and N-View Inc.

Also in the realm of large displays, AEG has developed LCDs for sign boards, such as those in airports, railway stations, and stock exchanges. AEG's billboard LCD uses a dichroic technology in which a highly concentrated dye is mixed with the liquid-crystal material. Only one polarizer is used to minimize the bleed-through in the transmissive mode. These LCDs deliver very bright characters with a 50:1 contrast ratio and no viewing-angle problems.

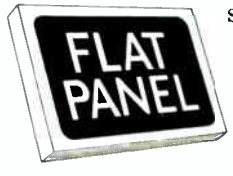
Plasma or gas-discharge displays do not have to project an image to get a large display area. Photonics Technology Inc. and Magnavox Electronic Systems Co. have teamed up to build a giant ac plasma display—the biggest ever at 1.5 meters diagonal [*Electronics*, April 30, 1987, p. 22].

Magnavox has also developed a full-color plasma display. The ultimate goal of the company's work is to produce a meter-square (1.5 m diagonal) color plasma display with the same resolution of the 1.5-m monochromatic display. So far, Magnavox engineers have fabricated and tested 6-in., 256-by 256-pixel full-color plasma displays.

The flat-panel display industry has many players, with most of the important ones evenly distributed among the three major technologies (see table), mainly in the U. S. and Japan. Two Japanese firms, Oki Electric Industry Co. and Dixy Corp., which are not shown in the table, are major vendors of plasma displays. Oki is also a leading LCD manufacturer. With all these participants in the market and many other organizations conducting research, the electronics industry can expect many more important developments in the technology of flat-panel displays.

TECHNOLOGY TO WATCH

CHERRY FINDS THE WAY TO BUILD THICK-FILM EL PANELS



A three-year effort has paid off for Cherry Electrical Products Corp. with a long-lasting, low-cost panel display made with a technology that has eluded commercialization for more than 50 years. This technology, dc thick-film electroluminescence, had long been relegated to relative obscurity in the display world, because no one could overcome the four main stumbling blocks afflicting them, says Walter Cherry, founder and chairman of the Waukegan, Ill., company.

Instead, companies were forced to use ac thin-film EL panels, which last longer but have other drawbacks. Producing thin-film EL panels requires many delicate thin-film sputtering steps, is hazardous to workers, and is prone to low yields, resulting in a costly product susceptible to catastrophic failures.

By contrast, the Cherry process uses only one spray coating and one noncritical aluminum

evaporation, permitting high yields at lower costs with no potential for catastrophic failure. Cherry engineers also discovered that a special driver circuitry was the key to squeezing optimized performance and longevity from the panel. The Cherry Display Products division in El Paso, Texas, called on Siliconix Inc. of Santa Clara, Calif., which designed and fabricated a specialized driver chip set. The partnership has resulted in a 128,000-pixel display panel with a starting luminance of 25 foot-lamberts and a maximum of 30% degradation after 10,000 hours. Cherry expects to begin production of the panel by the end of this year.

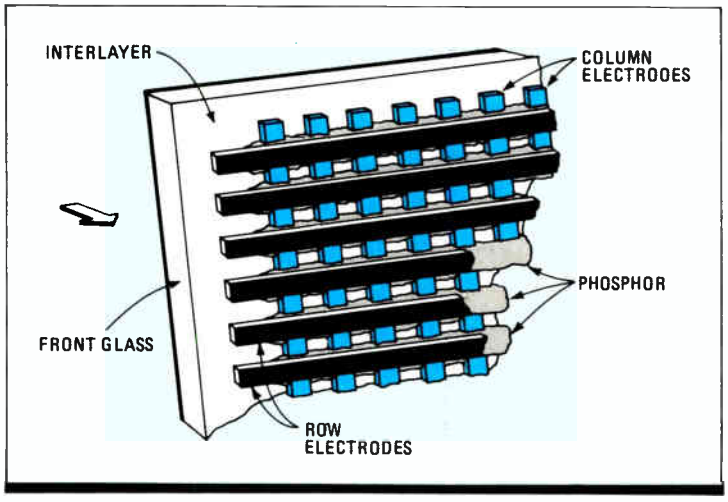
The design of Cherry's dc EL panel differs significantly in other ways from an ac panel. An ac panel is capacitive. Its brightness is limited by capacitance, drive voltage, and pulse-repetition frequency. It requires a relatively high voltage, on the order of 400 V.

The dc panel is resistive. And because its brightness is proportional to its constant drive current, the panel is limited by temperature rise and the pulse-repetition frequency. Dynamic resistance in the dc panel is low, in the order of 100 Ω. To prevent excessive currents that can damage the phosphor, Cherry uses the Siliconix SI 9559 D/CMOS, an adjustable constant-current column driver. Its dc panel produces most of its visible light after the termination of the drive pulse. Cherry found that a 17.5-μs pulse at 240-Hz repetition frequency provided high brightness without excessive thermal buildup.

The dc EL panel (see fig. 1) comprises a glass substrate on which 640 column electrodes of tin oxide are etched. An interlayer of aluminum oxide on the order of 100 Å is deposited over these electrodes. A phosphor comprising crystals of copper-coated zinc sulfide, nominally 2 μm wide, doped with manganese and copper, is next sprayed onto the substrate to a thickness of 25 μm. A 1-μm aluminum back layer that later forms the row electrodes is then evaporated over this phosphor layer. The substrate is trimmed and the row electrodes mechanically scribed. Bridging links connect the row electrodes to the row contact fingers.

Next, the panel undergoes forming, during which dc current is passed through the device. The current causes the discrete 2 μm-crystals to produce a light-emitting film. Process temperature is critical—temperatures above 120°C will lower luminous efficiency and produce dark-centered pixels. The brightness of the fully formed panel (see fig. 2) slightly decreases over time.

Cherry's new dc EL panel substantially overcomes the four main failure mechanisms of previous thick-film devices. The first is further forming, in which moisture, certain organic contaminents, and excessive heat cause the threshold voltage to keep increasing until the drive circuitry can no longer draw sufficient current at its maximum voltage. Vacuum baking and the current-limited drive prevent further forming.



1. THICK-FILM EL. Cherry's panel has a glass substrate with 640 etched column electrodes of thick-film tin oxide.

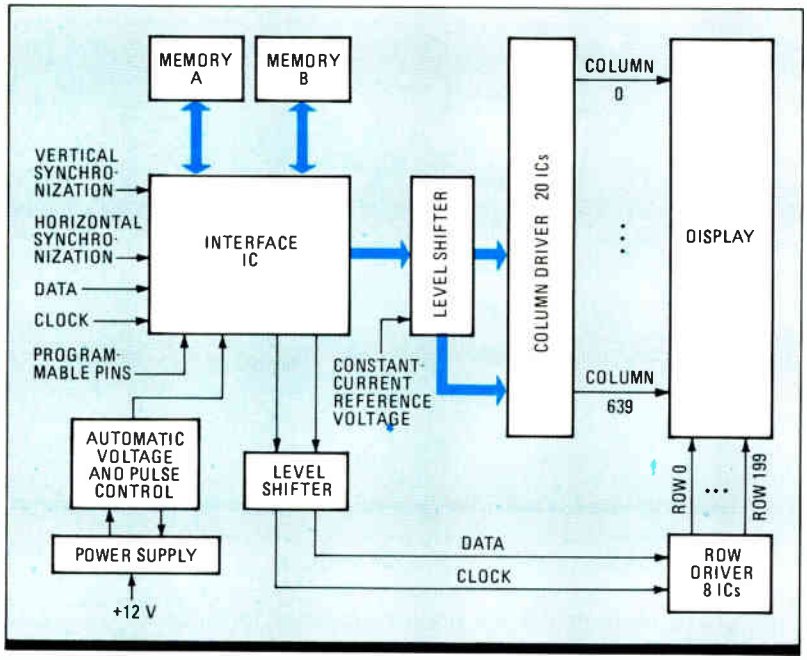
The second, loadline flattening, occurs when the resistance of the copper-coated back layer progressively increases, limiting the current that can be passed, and therefore the brightness. A small amount of silver added to the phosphor coating substantially eliminates the problem.

The third problem, softening, means the threshold voltage of the device degrades, producing background light. The efficiency of the phosphor also degrades. Silver added to the phosphor's copper coating stops softening.

The fourth problem, light rise time, means the time it takes for the panel to reach the proper brightness lags behind the applied current. Traps or defect centers in the phosphor cause the lag. Adding sulphur to the binder maintains the rise time.

The main function of the panel's electronics is to drive the panel at a 240-Hz frame rate with a current-limited signal to maintain high brightness without excessive thermal buildup at a high efficiency. In a 240-Hz frame-rate system, the time available for illuminating a pixel in each

2. LIGHT OUTPUT VS. TIME. The EL panel's brightness is a linear function of current, but brightness degrades slightly over time.



3. PANEL DRIVE. The system provides a 240-Hz frame rate current-limited drive for high brightness.

frame is only 12.5 μs. During this period, the drive system must overcome the interelectrode capacitance in the panel and avoid overdriving the display. When a pixel is addressed, the current is supplied by the column drive in two steps. The first precharges the pixel with a short-duration, high-current pulse that charges the column capacitance to the pixel voltage, about 70 V dc. When the pixel voltage exceeds the threshold of 70 to 90 V, the dc EL pixel conducts current resulting in light emission. Then the column drive supplies a constant current to the pixel.

The drive system consists of an interface integrated circuit, a level shifter, constant-current column drivers, a high-current row driver, and an automatic voltage and pulse-control circuit (see fig. 3). The interface IC stores video data at a 60-Hz frame rate in a dynamic random-access memory and then retrieves this data at a 240-Hz frame rate and supplies it to the column driver ICs. The interface IC provides row and column-timing pulses and has a programmable pulse width.

The level-shift IC does two tasks: converts the 5-V CMOS logic-level outputs of the interface IC to 12-V signal levels needed for the column drivers, and converts a 0 to 12-V analog reference to a constant current capable of driving 20 column drivers. The column driver, a Siliconix SI 9559 D/CMOS IC, comprises a 32-bit shift register, a 32-bit latch, and 32 NAND gates and output drivers. This IC is able to source more than 15 mA in a precharge mode and sink more than 15 mA in a pull-down mode. The output drivers operate at 90 V with low quiescent power. The outputs also source a constant current with a programmable range from 100 μA to 1 mA.

The row driver, a TI SN65557, sinks a minimum of 300 mA in the on state and blocks 100 V in its

TEAMWORK BETWEEN COMPANIES MADE IT HAPPEN

Walter Cherry, the 70-year-old founder and chairman of Cherry Electrical Products Corp., says that his company succeeded where others failed in the quest for a commercial thick-film electroluminescent display panel because of the partnership it forged with other companies. For example, he says, "as good as the new display panel is, it wouldn't meet the established performance specifications without the special integrated circuit developed by Siliconix."

The IC is part of the critical drive circuitry used in the new panel, the development of which was split between the Cherry Display Products division in El Paso, Texas, and Siliconix Inc. of Santa Clara, Calif. In addition to the Siliconix contribution, thick-film technology acquired from Phosphor Products Co., a British company, was refined, improved, and modified to make a producible panel.

In El Paso, chief scientist David Glaser and general manager George Kupsky concentrated on the processing and manufacturing of the dc thick-film EL panel. Glaser, who holds more than 50 patents in display technology, was responsible for the revised chemistry and physics used during processing. Kupsky, with more than 25 years in display technology and 80 patents, worked on the physical development of the display component and set up the production facility.


KUPSKY


GLASER


WILLIAMS


CONCKLIN

At no point did anyone working on the project come up with a dramatic breakthrough that made the rest easy, Glaser says. Rather, a series of developments paved the way: overcoming the four failure modes of the older thick-film technology, increasing frame timing to 240 Hz for better thermal efficiency, and increasing the luminous intensity by modifying the chemistry needed for the panel.

An important part of the task of creating the electronic drive system for the panel fell on the shoulders of Barry Concklin and Richard Williams at Siliconix. Concklin was responsible for the circuitry design, and Williams handled process development for the display devices.

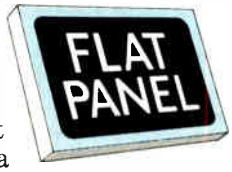
off state. The automatic voltage and pulse control electronically adjusts the voltage and pulse-width setting of the drive circuitry to allow the panel to be driven to a predetermined operating point.

Cherry will produce two types of dc EL panels. The EL1C-G000 will have a pixel aspect ratio similar to most liquid-crystal displays and will be in a 10.74-by-5.9-by-0.6-in. package that includes integral electronics. The EL1C-I000 will have a larger pixel height, comparable to an emissive (plasma) display, and this unit and its electronics will be in a 10.5-by-7.8-by-0.6-in. package. Prototypes will be available in August; production models by the end of this year. Volume pricing should be $250 per panel. *–Jerry Lyman*

For more information, circle 480 on the reader service card.

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

TECHNOLOGY TO WATCH



TEKTRONIX BUILDS A BRIGHTER, CRISPER LCD

Liquid-crystal display technology is taking on a crisp new look. Tektronix Inc. is now producing LCD modules that offer far higher contrast and a much greater viewing angle than has heretofore been available. The Beaverton, Ore., company's HyperTwist panel modules rely on an electro-optical effect called the supertwisted birefringence effect, or SBE, to attain their superior display characteristics. They are the first SBE products to come out of the laboratory and onto the market.

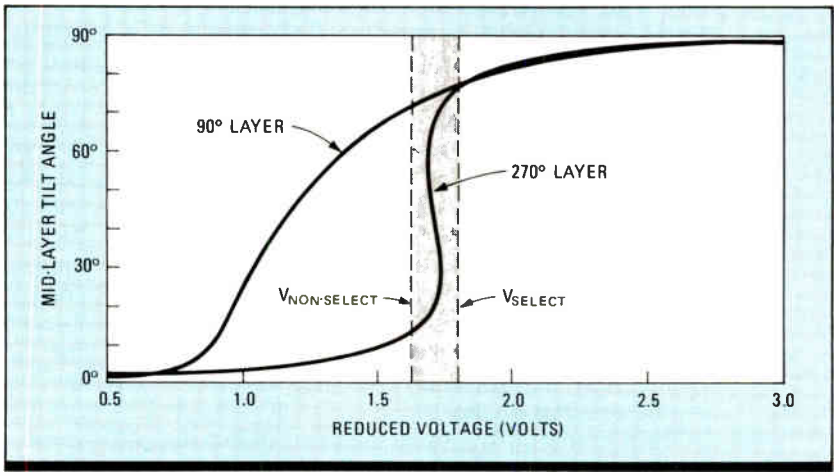
The HyperTwist modules are nematic LCDs. Nematic LCDs have gradually been improved—from twisted-nematic displays, which twist only the liquid crystal molecules through an angle of 90°; to supertwisted-nematic panels, which twist the entire molecular structure 180°; and now to supertwisted birefringence, which uses an optimal twist of 270°. The high supertwist angle, when combined with a high pretilt angle at the panel's alignment layer, yields an LCD with a wide viewing cone. With the supertwisted LCD's polarizers set up for birefringence, the resulting display also exhibits exceptionally high contrast.

The HyperTwist display panel is built as a multilayer transparent sandwich. The panels can be made to operate in either of two modes: black on yellow, or dark blue on white. These high-contrast displays are well suited to a number of applications, including laptop computers, computer projection displays, and instrumentation. As an option, the panels can be backlit for nighttime visibility. Since the HyperTwist displays use the same type of row and column driver electronics as conventional twisted-nematic LCDs, they substitute easily for these.

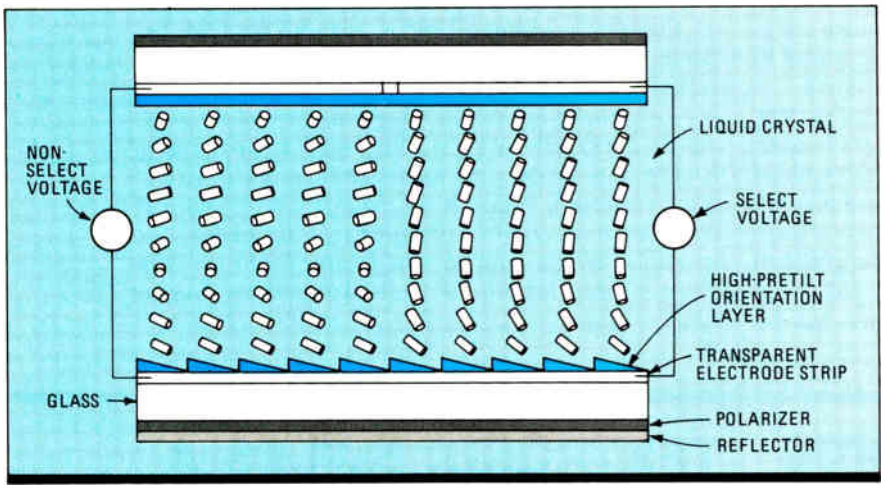
So far, the HyperTwist panels come in two sizes: 128×128 pixels and 128×256 pixels, which will be available within the next three months. Custom-designed HyperTwist displays are also available. A full-size 640-by-200-pixel HyperTwist display will be available in January 1988. No prices have been set.

HyperTwist technology relies on three important factors: 270° supertwisted nematic liquid crystals, a high pretilt angle of 28° to 31°, and the birefringence effect. Researchers have found that the supertwist angle of 270° is optimal: it produces the potential to achieve the highest contrast and the widest viewing angle. However, this 270° twist must be accompanied by a high pretilt angle. These two conditions are sufficient to achieve a wide viewing angle. A high contrast ratio is achieved by adding a final ingredient: birefringence, or the refraction of light in two slightly different directions to form two rays.

In conventional twisted-nematic displays, the molecules in the liquid crystal twist through an angle of 90° from one electrode plane to the other. A high twist angle, or supertwist, is achieved by imparting a twist to the entire nematic liquid-crystal structure. This results in a steeper distortion-vs.-voltage curve than in twisted-nematic structures (see fig. 1). The distortion curve measures the change in mid-plane tilt angle within



1. THE TWIST. The distortion curve of a 270° supertwisted liquid crystal is far steeper and thus spans a greater mid-plane tilt angle than a 90° twisted crystal.



2. CLEAR SANDWICH. The Tektronix HyperTwist LCD is a multilayer transparent structure in which the active layer is a supertwisted chiral-nematic liquid crystal.

the liquid-crystal matrix with respect to changes in voltage across the liquid-crystal plane. A steep slope in the distortion curve at the SBE threshold voltage is a necessary condition for high contrast and a wide viewing angle in a high-resolution display, because the sharp threshold allows more pixels to be addressed without losing contrast or reducing the viewing angle.

In a supertwisted-nematic liquid crystal, the distortion curve increases in steepness with increasing supertwist angles until at a certain critical twist angle—the optimal 270° angle—a portion of the curve attains an infinite slope at the SBE threshold voltage. At this angle the voltage threshold spans a large change—from nearly 0° to nearly 90°—in the mid-layer tilt angle. This helps improve resolution, contrast ratio, and viewing angle. To achieve the optimal twist angle of 270°, Tektronix engineers doped nematic liquid-crystal material with optically active, or chiral, molecules. This doped material is called a supertwisted chiral-nematic liquid crystal.

In addition to supertwisting, a high pretilt angle is required. "The only known method to obtain true SBE operation is to increase the pretilt angle," says Terry J. Scheffer, Tektronix's principal scientist. In a twisted-nematic LCD, the nematic liquid crystal is uniformly oriented along well-defined directions at the surfaces of the substrate plates by means of alignment layers. These alignment layers, or nematic directors, are produced by coating a thin film of polyimide on the substrate and rubbing it with a nylon brush with precisely controlled pressure and speed. This produces a surface layer where the nematic director actually points out of the surface by a few degrees, called the pretilt angle. For this reason, the alignment layer is also known as the pretilt orientation layer.

Until recently, the only reliable method to get a high pretilt angle—that is, 20° or more—was to lay a material such as silicon oxide on the substrate at an oblique angle through vacuum deposition. Pretilt angles of 20° to 30° have been attained this way, but the method is not cost-effective for volume manufacturing. The 31° pretilt in the HyperTwist SBE module's pretilt orientation layer is produced with a proprietary rubbing process.

But although the high supertwist angle and the high pretilt angle provide a wide viewing cone, "in order to obtain a high contrast ratio with the 270° configuration, the [HyperTwist panel] is operated in a birefringence mode," says Scheffer. The SBE display, like conventional twisted-nematic LCDs, uses two polarizers. To achieve the correct degree of birefringence, the front and rear polarizers are offset approximately 30° and 60°, respectively, from the on-axis position, and the thickness and birefringence of the liquid-crystal layer are set to satisfy a specific optical relationship.

The HyperTwist display consists of a multilayer transparent sandwich structure (see fig. 2). The reflector layer is optional; if it is removed, the display will operate in a transmissive mode—that is, for backlighting and projection.

The transparent electrode strips run at right angles to each other on the two inner glass surfaces and define the pixel areas. With the select voltage applied, the orientation of the cylinders (the liquid crystals) is such that light is transmitted through the sandwich. When the non-select voltage is applied, the orientation of the cylinders changes the direction of the local optical axis through the pixel area of the liquid-crystal layer in such a way as to cause the sandwich to block the transmission of light. A 270° SBE display built this way appears bright yellow when the non-select voltage is applied and black when the select voltage is applied; this mode of operation is called the yellow mode. Rotating either of the two polarizers by 90° produces a complementary mode called the blue mode, which has a bright, colorless appearance in the select state and a dark purplish-blue in the non-select state.

"The SBE display is not suitable for applications that require gray scale, full-color capability, and video response times," says Scheffer. However, he is quick to point out that "in contrast to twisted-nematic displays, the SBE display technology does seem to be ideally suited for applications where large-area displays of high complexity, high contast, wide viewing cone, and low power consumption are required—such as, for example, in portable laptop computers." In addition, SBE display technology opens up opportunities for high-quality computer projection displays, either as front or rear projection systems or as an add-on to overhead projectors, and for various types of instrumentation. *–Tom Manuel*

For more information, circle 481 on the reader service card.

COMING SOON FROM PLANAR: A FULL-COLOR EL DISPLAY

Planar Systems Inc., which earlier this year delivered its first two-color thin-film electroluminescent display to the U.S. Army, is working hard now to build on this technology and develop a three-color EL display. That should happen shortly: Planar engineers have come up with a new technology to produce what they expect to be the industry's first full-color thin-film EL display. The Beaverton, Ore., company expects to deliver the first prototype of its full-color EL flat-panel to the Army late this year.

Planar's challenge is to build a single-layer, full-color display panel with red, green, and blue EL phosphors that is bright enough, large enough, and low enough in cost to be a commercially viable product. While military needs will probably generate some business initially for the full color display, it will probably take the company another two years to bring down costs sufficiently to bring out the display as a commercial product.

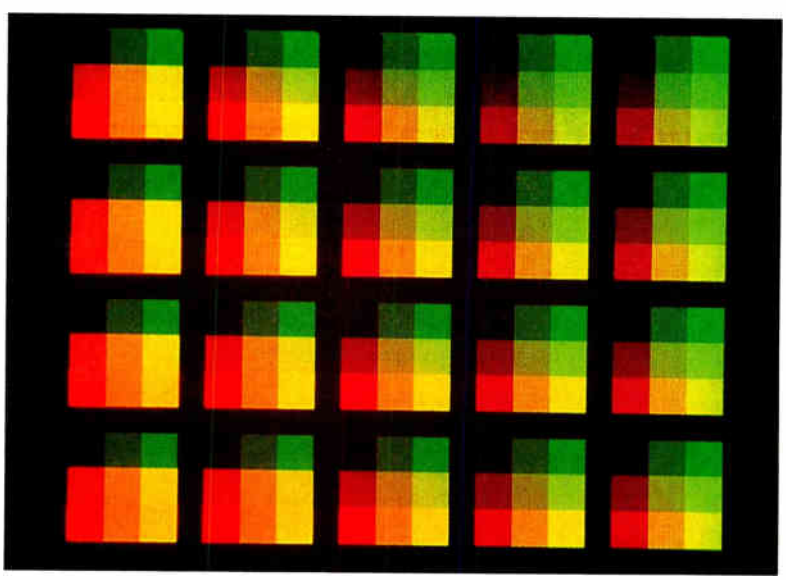
The company's most recent development, the two-color thin-film EL display, was developed with a stacked twin-phosphor, red and green structure (see fig. 1). Standard one-color TFEL displays are made by a meticulously controlled process, in which a thin film of EL phosphor and patterns of thin-film electrodes are laid down on glass panels. When two layers of phosphors emitting two primary colors—red and green, for example—are used, then a limited color display can be made. Planar's new full-color process involves a single EL active layer with a pattern of three stripes of red, green, and blue phosphors and the appropriate pattern of electrodes with corresponding drivers and electronics. A self-healing burn-in procedure will be used in the manufacturing process.

TFEL display technology is based upon a thin uniform layer of EL material, such as zinc sulfide doped with manganese, that emits light when an electric field above the threshold voltage is applied across it. Pixels are produced when the electric field is applied selectively to small squares. The field is applied by a layer of thin stripes of conducting material on one side of the EL active layer and another layer of conducting stripes facing the opposite way on the other side. The pixels are selectively turned on or off to produce displays of text and graphics.

For the light to reach the viewer, the conducting electrode stripes on the side facing the glass front of the panel must be made with transparent conducting material—in most cases, indium tin oxide. The electrode stripes behind the active layer are usually made by depositing a thin layer of aluminum. The row and column electrodes are insulated from the active layer by layers of thin-film dielectric.

Planar has perfected a continuous manufacturing process for TFEL display panels using photoprocessing, thin-film deposition, and metallization performed in a Class 10 clean room—a process similar to integrated-circuit manufacturing. Planar is now using this manufacturing facility in Beaverton to make a large volume of affordable, bright, high-resolution monochrome TFEL panels for a wide variety of electronic products.

To achieve limited color capability, multicolor TFEL displays are made from a two-layer stacked active substrate—one thin-film EL layer for each color. Rare-earth fluorides are used as activators to produce colors other than the yellow-orange emission of Mn doped ZnS—terbium fluoride for green light, samarium fluoride for red, and thulium fluoride for blue, for example. However, the brightness of the ZnS-TmF_3 blue phosphor is too dim to be used, and some way to brighten it or a brighter blue phosphor must be found. Planar engineers decided against using the stacked substrate to develop a full-color EL display because it is only workable for two colors—any more and the resolution is too poor—and is too thick, heavy, and costly to make. So the development team settled on a patterned phosphor structure, says Steve Hix, Planar's vice president of the marketing and sales group. The structure is a single-substrate EL layer with stripes of alternating color phosphors. Three primary-color (RGB) stripes placed close together represent one pixel. Full-color display is achieved much as it is in a color CRT with its RGB dots, because different



1. LIMITED COLOR. Planar's two-color, thin-film EL display stacks red and green phosphors to produce a variety of colors in the green-yellow-red region.

stripes are turned on or off in combination to achieve the desired colors.

The challenges in turning this technology into a viable product include increasing the effective brightness of each stripe to obtain a pixel brightness equal to the brightness of a single-color pixel. Because each stripe is a third the size of a monochrome TFEL pixel, it should be at least three times as bright. Planar engineers claim that they know how to make the phosphors brighter, although they are not ready to describe exactly how their method works.

Planar expects to deliver a prototype three-color TFEL panel late this year; it hopes to get the cost down in two years so it can offer a commercially viable product

The patterned phosphor structure also provides the minimum size and weight and requires much less packaging complexity than a stacked substrate. But the main disadvantage of this structure is that to produce a display with an effective resolution of a given number of pixels per inch, the panel must be produced with subpixels at three times that number per inch.

The pattern could be deposited in many ways: the films could be patterned directly by depositing them through a shadow mask, the pattern could be made by a photoresist liftoff process, or it could be defined by wet or dry etching through a photoresist or metal mask. The Planar team plans to evaluate all these approaches and then develop a process for the most promising.

The addressing electronics for a three-color display are more complex. The three stripes, or subpixels, of each pixel must be addressed and driven independently to achieve the full-color spectrum, producing three times as many row and column drivers and driver electronics as in a monochrome display with the same resolution. Each color will have its own set of drivers and drive electronics. A common controller will determine what pixels to turn on, what color each is to be, and what subpixels to turn on to achieve that color.

Color gray-scale capability needs to be added for a realistic display, but Planar has not yet fully developed the gray-scale drivers to vary the intensity of the colors. Gray scale can be controlled by varying the frequency for the three subpixels, because the average luminance of the phosphors increases as the frequency of the ac voltage increases.

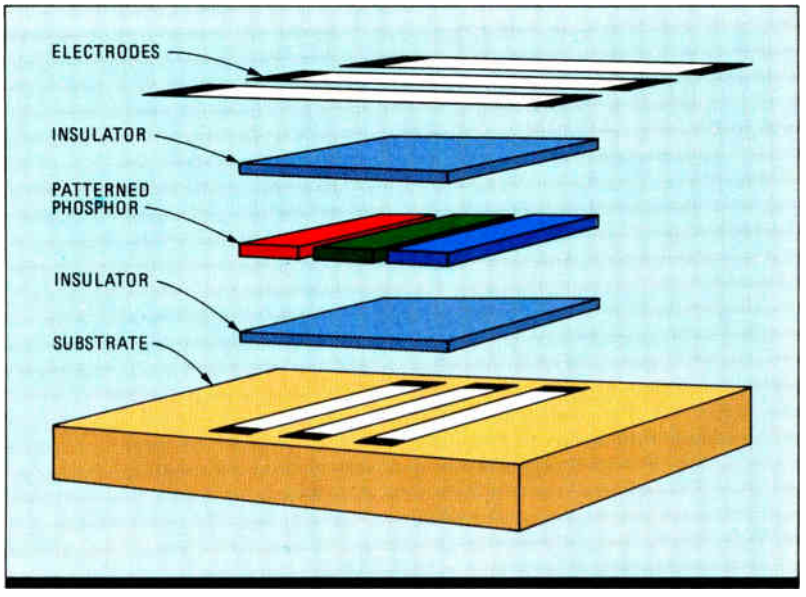
The company has already demonstrated multicolor TFEL display technology with high resolution and a large active area. A reliable two-color structure has been built, fully addressed, tested, and delivered under a two-year development contract with the U. S. Army Laboratory Command in Fort Monmouth, N. J. However, because this display has no blue, it can only produce colors in the green-yellow-red region of the spectrum. It also costs too much to be a viable commercial product.

However, Planar's manufacturing technology for monochromatic yellow-phosphor TFEL display is already cost-effective for high-volume commercial production. The display panels are manufactured in a continuous process with equipment designed by the company. Planar's process is the only continuous process developed so far for high-volume TFEL production, the company claims.

Depositing a multilayer stack of different thin films to form a solid-state device on a glass substrate takes place in a Class 10 clean room. The vacuum equipment in the continuous-process clean room minimizes defects while maximizing throughputs and yields.

However, "even with our leading-edge manufacturing technology, each of the large area TFEL devices contains microscopic flaws," says Eric Dickey, a process engineer at Planar. If these flaws are left untreated, the instantaneous high voltage applied when the device is first fired up would cause arcing that would burn out pixels or whole rows of pixels, ruining the panel.

Therefore, Planar developed a self-healing burn-in procedure as part of the manufacturing process. Panels are installed on a rack of special burn-in circuit boards that limit the current flow to each pixel. Voltage ramp rate, pulse width, and frequency are computer controlled. This controlled burn-in heals the flaws, yielding a display panel that can outlast the electronics supporting it—Planar reports lifetimes in excess of 30,000 hours. Average lifetimes of CRT displays are 10,000 hours. *–Tom Manuel*



2. FULL COLOR. Planar engineers are developing a patterned red-green-blue phosphor structure to produce TFEL display panels that will show all the colors of the spectrum.

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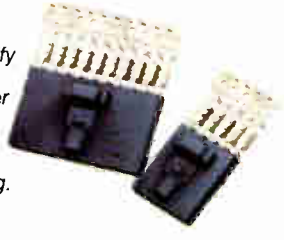

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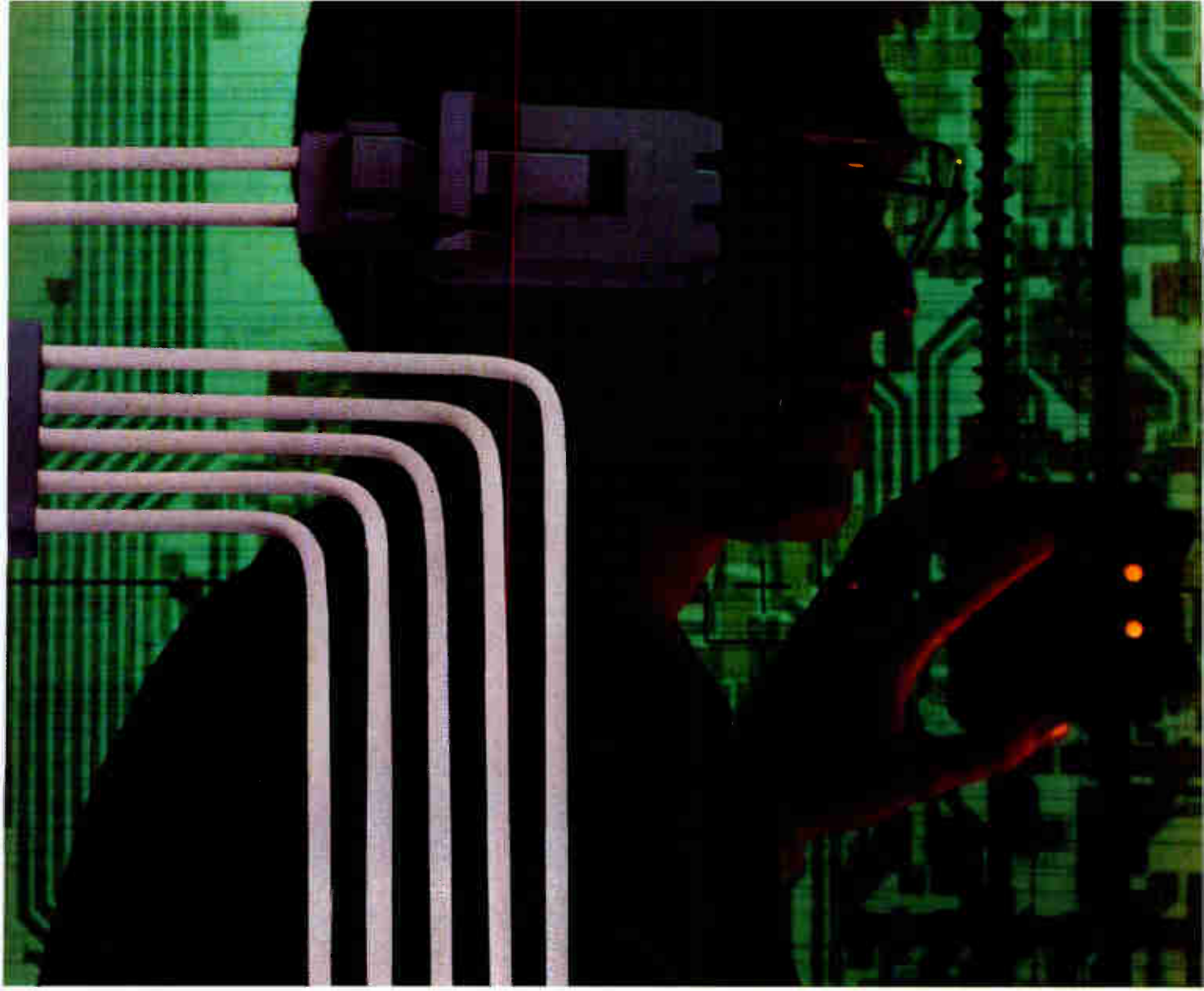

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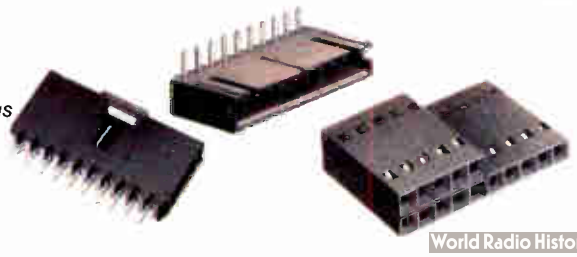

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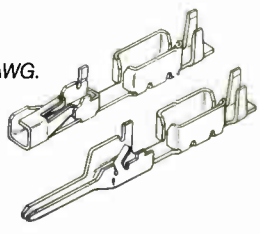

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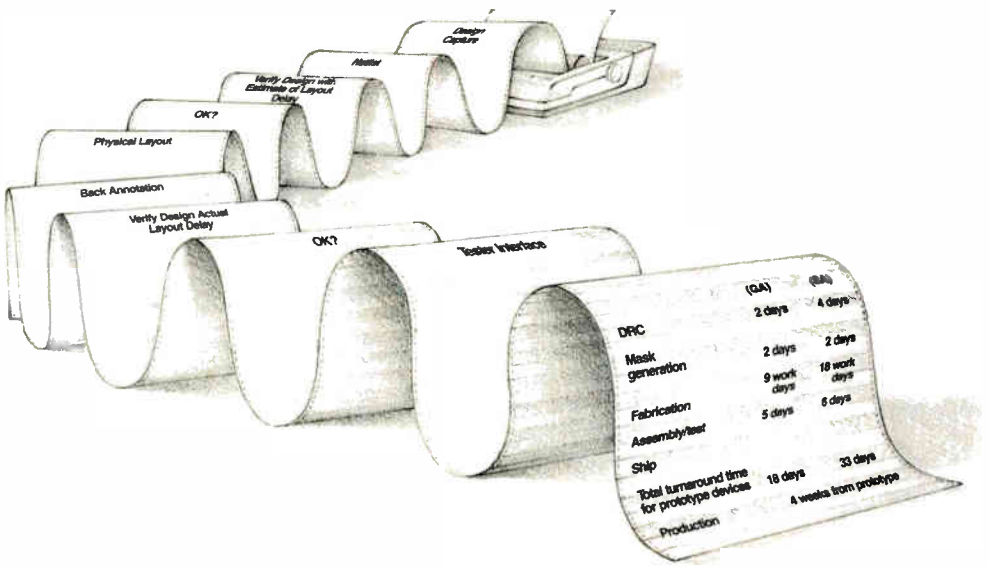
02000	2128	76	12	28, 40, 48 (C/P)	68, 84 (C/P)	44, 51, 68 (C/P) 84 (C)
03000	3264	96	12		68, 84, 100 (C/P)	68, 84 (C/P) 100 (C)
04000	4256	108	12		68, 84, 100, 120 (C/P)	68, 84 (C/P) 100, 124 (C)
06000	5880	132	12		68, 84, 100, 120 (C/P) 144 (C)	68, 84 (C/P) 100, 124 (C)
08000	7872	168	16		84, 100, 120 (C/P) 144, 180 (C)	84 (C/P) 100, 124 (C)
10000	9776	192	16		84, 100, 120 (C/P) 144, 180, 208 (C)	84 (C/P) 100, 124 (C)

C = ceramic, P = plastic



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SPECIAL REPORT: THE MOVE TO ONE-CHIP LINEAR SYSTEMS

Linear chip makers increasingly are developing complex products that provide application-specific-circuit or user-programmable solutions

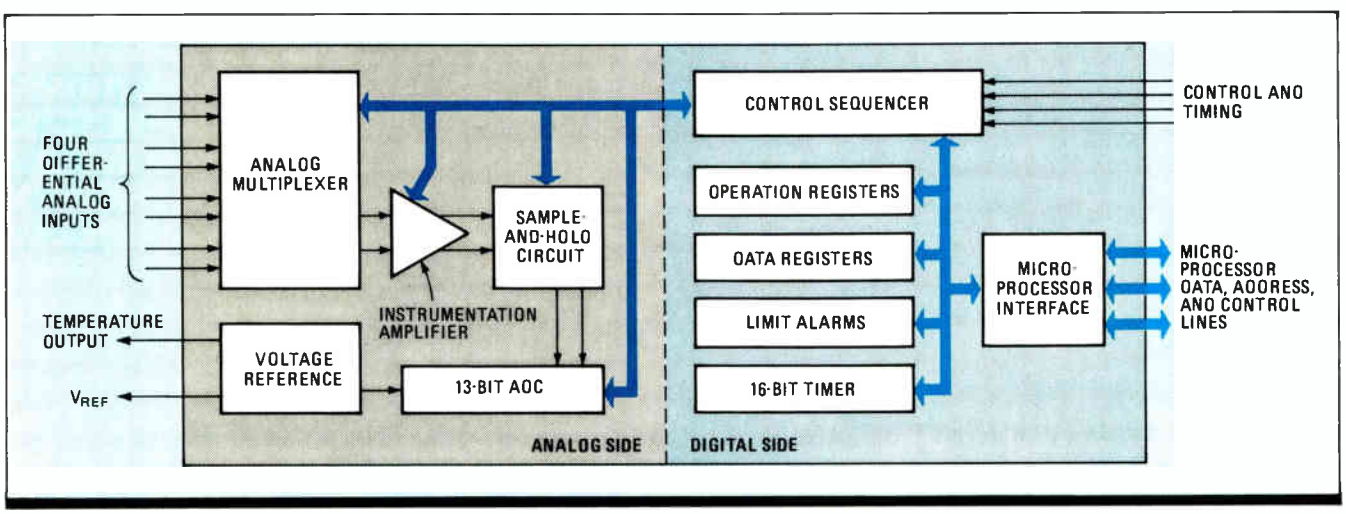
by Bernard C. Cole

Slowly but surely, the analog chip business is going the way of its digital sibling. Analog is moving away from commodity-type building-block circuits designed to work in a variety of designs to one-chip subsystems that provide user-programmable or application-specific solutions.

Commodity building-block circuits are still the mainstay of many chip makers that build linear circuits, but a concerted effort by all of them is under way to strike a better balance in this increasingly competitive segment of the business. Manufacturers are exploring niche markets, seeking areas where there are fewer competitors and therefore higher profits. They can wring more profit from a custom or semicustom application-specific circuit that offers users increased functionality, reduced component count, and lower cost.

Other manufacturers are working hard to develop the analog equivalent of the microprocessor. They're trying to build general-purpose building blocks that can be programmed by the user to meet his needs, within the constraints of the architecture of the device.

Some of the factors that motivate the shift to user-programmable analog subsystems are similar to those on the digital side: increased competition and rising demand for more specific solutions to users' problems, along with smaller geometries and higher levels of integration, which reduce component count and system cost. Other factors fueling the trend are unique to the linear business: most young engineers are well-trained in digital design techniques; relatively few understand how to design with linear circuits, so manufacturers need to build linear parts that



1. ANALOG SUBSYSTEM. Micro Linear's ML2200 is a flexible, programmable, self-calibrating data-acquisition peripheral on a single chip.

can work with digital devices without extensive linear design work. The basic incompatibility between dense digital VLSI and high-performance linear needs also plays a part, placing extra value on chips that combine the two, successfully dealing with the incompatibilities.

Densities in both bipolar and CMOS linear technologies have been reduced from the 8-to-10-μm range over the past decade to about 3 to 5 μm today, says Surinder Krishna, manager of advanced technology at Fairchild Semiconductor Corp., Cupertino, Calif. A few companies, such as GE/Intersil, Cupertino, have pushed linear geometries down to 1.5 μm without substantially compromising performance. With such improvements, says Norman Wheelock, director of marketing at GE/Intersil, designers are looking beyond simple linear blocks to more sophisticated subsystems on a chip as a way to differentiate their products from competitive devices.

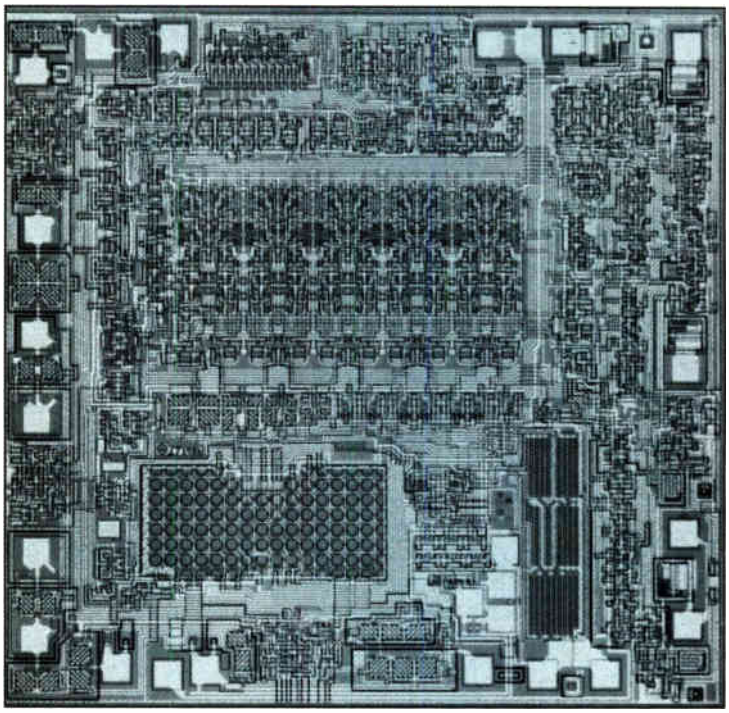
And such differentiation is becoming more important with increased competition. Traditionally, the linear market has been dominated by a half dozen or so U. S. companies, including Analog Devices, Burr-Brown, Exar, Honeywell, Ferranti Interdesign, GE/Intersil, GE/RCA, Motorola, National Semiconductor, Precision Monolithics, TRW, Signetics, and Texas Instruments. They have now been joined by such companies as Advanced Linear Devices, Brooktree, Crystal Semiconductor, Inmos, Integrated Device Technology, Linear Technology, Maxim Integrated Devices, Micro Linear, and NCR. And activity overseas, especially in Japan, is growing: At the International Solid State Circuits Conference held in New York last February, for example, eight out of the 24 papers on analog and linear circuits were from Japanese companies.

The increased competition is driving linear houses to diversify into building single-chip linear subsystems that solve specific application needs. "The problem is identifying a sufficiently large user base to justify building such a circuit," says Thomas Redfern, CMOS design manager at Linear Technology Corp., Milpitas, Calif. "The attraction is that if you can identify such a market, and do so before the competition, you can build products with profit margins much greater than you could ever get in the commodity business. The tradeoff is risk."

Many other companies, like Crystal Semiconductor, Linear Technology, and Micro Linear, are looking for a place where a general-purpose microprogrammable analog subsystem solution can be applied to as broad a base of systems as possible. One such place is at the interface between the microprocessor and the surrounding analog and sensor circuitry needed to communicate with the outside world. Digitally oriented system designers often lack experience in building such circuitry.

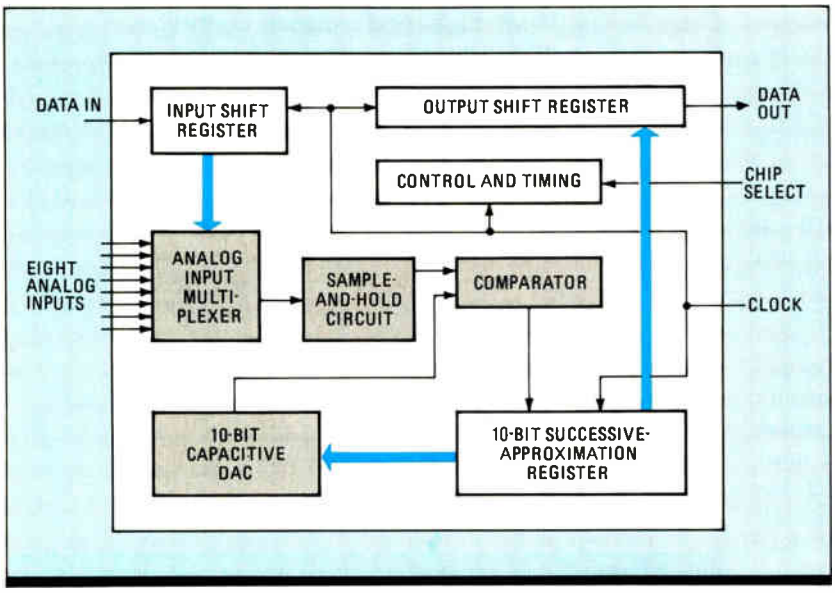
An approach to solving this interface problem, taken by vendors like National Semiconductor Corp. in its 16-bit high performance controller and 4- and 8- bit COPs microcontroller families, is to incorporate the data-conversion circuitry onto the same chip as the central processing unit. When the data-conversion circuitry moves on chip, valuable microprocessor pins are not taken up by the necessary converter interface, says Dan Shockey, strategic marketing manager for National's analog division. In the case of an analog-to-digital converter, only two pins—analog input and reference voltage—need be added. In some cases the reference can be eliminated.

But Linear Technology's Redfern says there are two problems with this approach. First, very few systems have only one analog input. To expand inputs, an analog multiplexer must be added. If it is integrated onto the same chip as the processor, a pin must be added for each analog channel. Second, there are a number of manufacturing reasons why integrating the microprocessor on the same chip as the data conversion circuitry is not advisable. "The processing requirements for data-conversion devices are in some cases opposed to those for a microprocessor," Redfern says. "For instance, the microprocessor needs small feature size for the best possible speed and density. The ADC, on the other hand, needs very precise matching at relatively large geometries."



2. FLAGSHIP. Linear Technology has designed the first of a family of one-chip data-acquisition systems, the 10-bit LTC1090.

An alternative solution, pioneered by companies such as Analog Devices, Burr-Brown, and National Semiconductor, is to add a parallel interface to the data-conversion chip. This reduces the chip count at the interface between the data-conversion chip and the microprocessor, but it



3. SERIAL I/O. The LTC1090 data-acquisition chip has serial digital I/O that can be configured to operate in full- or half-duplex modes.

brings with it some problems. Even when directly compatible with the microprocessor's control and data buses, the parallel interface has the disadvantage of adding many more pins and complexity to the ADC. It also consumes microprocessor memory and I/O space, says Redfern, which might be better used elsewhere.

To overcome these problems, companies such as Crystal Semiconductor and Micro Linear have developed single-chip programmable analog subsystems that are fabricated with processes optimized for linear functions but which are dense enough to incorporate a lot of digital circuitry. The circuitry can turn an ADC into a complete data-acquisition peripheral that ties directly to the microprocessor bus, minimizing use of the processor's own memory and I/O space.

Micro Linear's first effort in this direction is the ML2200, a self-calibrating 13-bit data-acquisition peripheral (see fig. 1). Fabricated using a 3-μm double-polysilicon CMOS process, the chip contains 25,000 transistors on a 160-by-160-mil die. Key design aims for the part were flexibility and programmability, says Charles Gopen, vice president of marketing at the company. To achieve them, the device incorporates a digital block that contains an 8-bit microcontroller and sequencer, data and operation registers based on static random-access memory, limit alarms, a 16-bit timer, and a microprocessor interface. Even without the sophisticated microprocessor-like digital block, the analog portion of the circuit incorporates an impressive level of functionality, including a four-channel differential-input multiplexer, a combination sample-and-hold and instrumentation amplifier, a 13-bit ADC, and a 2.5-V bandgap reference that also provides an analog output proportional to the ambient temperature.

Gopen says the data-acquisition peripheral's on-chip control sequencer is programmed by the user in the same way as a CPU, using the operation registers. Among the programmable functions are degree of accuracy (8 or 13 bits); gain selection (1, 2, 4, or 8); the use of an internal or external reference; and a variety of synchronization and data-transfer options.

Converted data is stored in a double-buffered data register that holds the results of up to eight conversions before the ML2200 notifies the CPU, through an interrupt or direct memory access request, that the buffer is full. This double-buffered approach, says Gopen, allows eight more conversions to be made while the previous series of conversions are being read. To achieve the impressive 13-bit accuracy, the ML2200 incorporates a self-calibration technique that makes use of the on-board intelligence of the control sequencer to monitor the operation of the converter and correct errors on the fly.

The only other company besides Micro Linear that is pursuing the analog subsystem approach using a parallel interface is Crystal Semiconductor Inc. of Dallas [*Electronics*, Dec. 18, 1986, p. 67]. Its CS5000 series of 12-, 14-, and 16-bit converters has sampling rates of 63, 50, and 50 kHz, respectively. By comparison, the Micro Linear device features sampling rates of 40 kHz at 13 bits and 50 kHz at 8 bits. The first in a family of such data-acquisition peripheral chips that will include one version with eight single-ended input channels, the core of the device has also been incorporated by Micro Linear into a cell family.

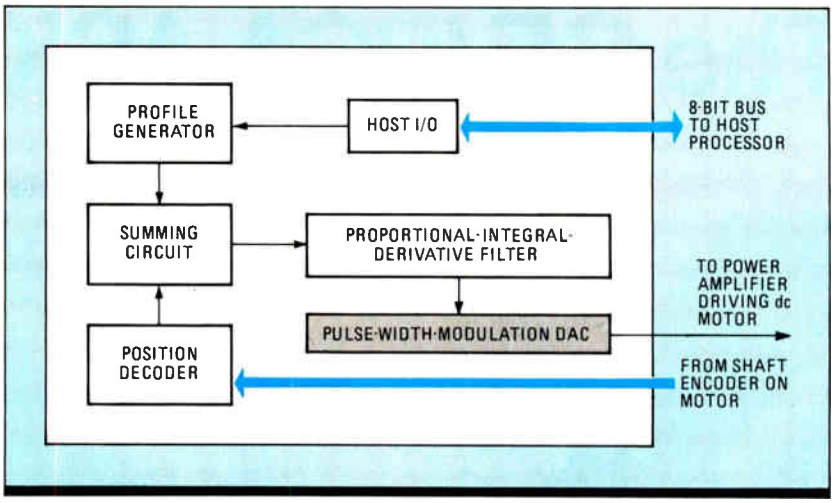
As an alternative to the parallel approach, a number of companies have adopted the serial interface. The advantage of this approach, says Redfern, is that it keeps the data-conversion and microprocessor functions completely separate, while consuming a minimum number of pins on both.

Two types of serial protocols have been developed for use on data-conversion devices, the full- and half-duplex schemes. Both of them are synchronous and require a clock. The half-duplex is used in such devices as the ADC-0831, -0832, -0834, and -0838, a series of 8-bit ADCs made by both Texas Instruments and National Semiconductor. It separates the address and data portions of the interface into two time increments, in which the ADC is either listening or talking, but never both at the same time.

In the full-duplex system, the ADC talks and listens at the same time. It is less straightforward than the half-duplex scheme but has the advantage of taking only half as long to transmit address and data words because the transmission occurs simultaneously. Full-duplex interfaces are used on the TLC540, MC14540, and ADC0811, 8-bit ADCs from TI, Motorola, and National Semi-

conductor, respectively.

Taking this concept to its logical conclusion, Linear Technology has developed the first in a family of what it calls single-chip data-acquisition systems. The flagship of the family is the LTC1090 (see fig. 2), a 10-bit ADC with a full-duplex serial I/O that can be reconfigured to operate in the half-duplex mode also. Fabricated using a 4-μm CMOS process, the LTC1090 integrates a 10-bit digital-to-analog converter, a 10-bit shift register, a sample-and-hold circuit, a comparator, a 10-bit successive-approximation register, an eight-channel multiplexer, and control and timing logic (see fig. 3). The device can be programmed to operate in either single-ended-bipolar or differential-unipolar configurations. The multiplexer can be configured as eight single-ended channels, four differential channels, or any combination totaling eight pins. Output words may be programmed to be either 8, 10, 12, or 16 bits long.



4. MOTOR CONTROLLER. System-level linear IC solutions are appearing for motor control, such as the LM628 from National Semiconductor.

Also in the works are at least three other products in the family: the half-duplex LTC1091, a 10-bit ADC with a two-channel on-chip multiplexer; the full-duplex LTC1540 with an 11-channel multiplexer; and the full-duplex LTC1092 with a two-channel multiplexer.

But finding niches for such general-purpose programmable subsystems on a chip is difficult, says Tom Odell, vice president of analog and military divisions at National Semiconductor. "A more cost-effective approach is to define niche markets where the users would find a more highly integrated, higher performance solution valuable enough to be willing to pay more for it," he says.

One such subsystem is the video DAC, which has a market now estimated by Dataquest Inc. at about $50 million. This could grow to as much as $100 million by 1990, predicts the San Jose market analyst. About a dozen semiconductor houses are pursuing various segments, among them Advanced Micro Devices, Brooktree, Honeywell, Inmos, NCR, Signetics, and TI. A newcomer to the market is GE/Intersil, with its IM2110, a 50-MHz device with three on-chip 4-bit DACs, an on-chip voltage reference, and 256 by 12 bits of SRAM for storage of color lookup tables (see p. 84).

Another market segment that is attracting a number of intriguing system-level linear IC solutions is motor control, with offerings from a diverse range of companies including: Galil Motion Control, Hewlett-Packard, Ixys, Motorola, and National Semiconductor. One of the more ambitious efforts is the LM628 from National Semiconductor, a monolithic controller for dc servo motors fabricated with a 3-μm n-channel MOS process (see fig. 4). Incorporating a profile generator, a position decoder, a microprocessor interface, a proportional-integral-derivative filter, and a pulse-width-modulation 8-bit DAC, it can be configured for either 8- or 12-bit outputs, with commands entered into the chip via an 8-bit parallel I/O bus. The sampling rate is under software control, settable by the user between 250 Hz and 4 kHz.

Defining such market opportunities and then serving them in a cost-effective way is difficult and many companies have opted for a custom or semicustom approach. In its Custom Linear ASIC group, Fairchild Semiconductor has developed an analog cell library for use by its designers that includes over ten types of internal operational amplifiers; a variety of analog buffers; voltage and current references; standard and auto-zeroed comparators; and both capacitor- and resistor-string-based DACs with accuracies up to 10 bits and up to 14 bits of resolution.

A similar approach is used at National Semiconductor. National still plans to remain a major competitor in the commodity building-block linear business, says Odell, but all such designs are incorporated into the company's cell library for use by its engineers in designing custom ICs. Also targeting this market is Honeywell Inc. with its programmable data-acquisition effort, in which it produces customized data-conversion circuits built around cell-based "analog engines" including bandgap references, comparators, low-noise op amps, switched-capacitor integrators, RC filters, oscillators and logic elements.

Whatever the approach, says Odell, analog subsystems incorporating more of the linear building blocks on a single chip are going to proliferate in the future. "The users, as a result of their experience on the digital side, are more sophisticated in what they want and are more demanding on the analog side," he says. "The question is identifying where it makes the most sense, and which form—the general-purpose programmable, the application-specific standard, or the custom or semicustom—is the most viable, economically." □

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HOW SEQUENT'S NEW MODEL OUTRUNS MOST MAINFRAMES

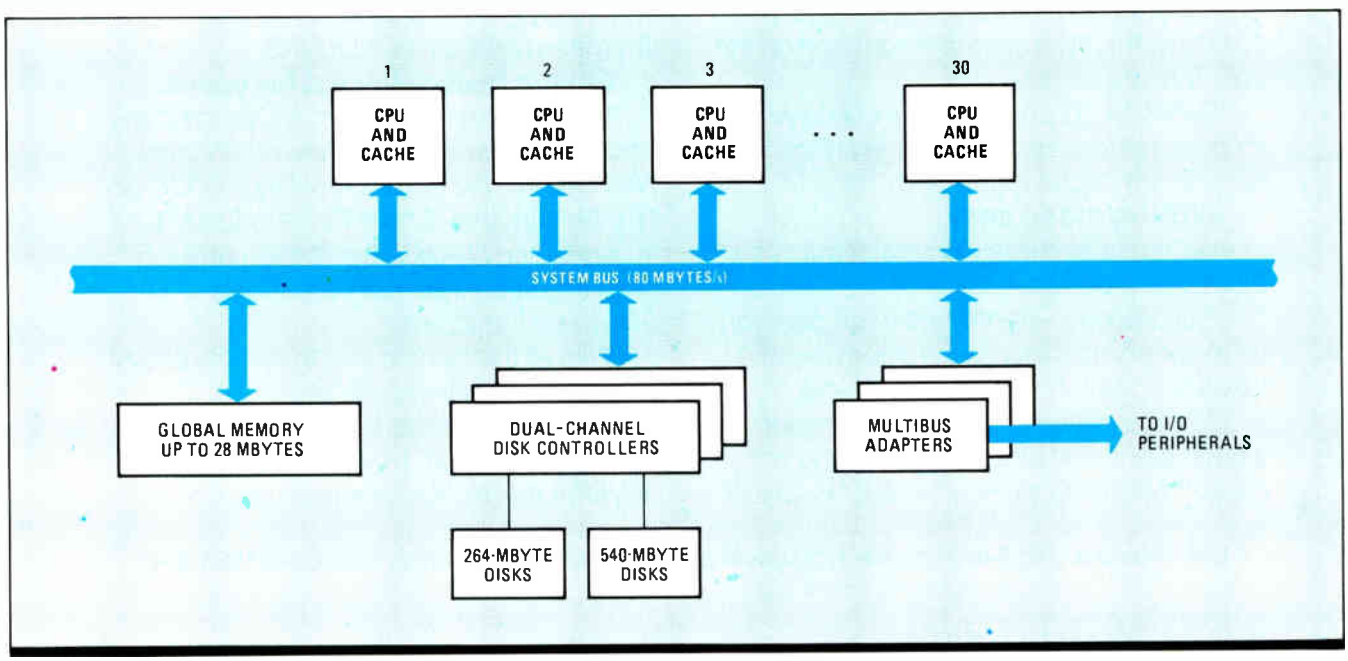
The company's latest parallel processor peaks at an awesome 81 mips; not only can it outperform most other mainframe computers, but it also costs just $788,000—20% as much

by Tom Manuel

A new line of parallel computer systems redefines the meaning of price-performance for midrange and mainframe computing. The Symmetry series from Sequent Computer Systems Inc. ties together as many as thirty 32-bit Intel 80386 microprocessors and takes advantage of 1-Mbit dynamic random-access memories, several custom VLSI chips, and a particularly effective caching scheme to hit a peak performance of 81 million instructions per second for the top-of-the-mark S81—at a cost of only $788,000 [*Electronics*, May 14, 1987, p. 21]. That translates into the processing wallop of the biggest mainframes, which cost from $4 million to $6 million. That kind of bang for the buck makes the Symmetry series suitable—and attractive—for use in two markets: business data processing and technical computing.

Because of the way the machine is designed, adding processors results in an almost linear rise in power. Moreover, little speed is sacrificed through contention for shared resources. And one of the chief concerns with multiprocessor systems—processors bogged down with too many calls to main memory—is overcome by assigning a local cache memory to each 386. A related problem, tying up a system bus by shifting data in and out of the cache, is solved by a clever memory-management scheme that makes certain that when two processors simultaneously try to access the same address in main memory, they get the correct data. The bus itself does a first-rate juggling act—keeping data and requests moving smoothly. Finally, a system of synchronizing mechanisms sets up global memory-based locks used by the operating system and applications programs.

Parallel computers built from potent but low-cost microprocessors ushered in a new era in computing about three years ago. Today, these machines deliver mainframe punch at minicomputer prices. Tomorrow, multiprocessor machines could replace both mainframes and minis. Sequent has been at the forefront of this movement since 1984, the year it introduced its Bal-



1. MICROMAINFRAME. Sequent linked multiple 386-based central processing units, memory modules, and I/O with a high-speed bus.

ance series of parallel computers (see story, p. 79).

The Symmetry series makes its entrance at 6 mips, climbing up to the peak of 81 mips. The system architecture nods in the direction of the original Sequent Balance, which was based on National Semiconductor's 32-bit microprocessors.

Broken down into its parts, the Symmetry system consists of central processing unit boards, global memory, dual-channel disk controllers, and Multibus adapter boards, all tied together by the system bus (see fig. 1). Each CPU is made up of an 80386, an 80387 floating-point unit, a two-way set-associative cache, and full bus-interface logic. To step things along even faster, a floating-point accelerator can be added.

Intel's 80386 is the powerhouse that drives the Symmetry series. Running at 16 MHz, each processor delivers three mips and operates with zero wait states when the data it needs is in the cache memory—a cache hit. A simulation indicates that in average programs hits are likely to occur 95% of the time. Packing two complete CPUs onto a card 12.5 by 14 in. is no mean feat (see fig. 2). To accomplish it, the engineers had to think dense. They chose three custom VLSI devices to complement the microprocessor and floating-point chips. Also, an 8-layer-printed circuit board filled the bill nicely. Thanks to its paired 386s, each CPU board stands ready and able to plug its six mips into the system.

Enough memory can be kept on tap to serve from 2 to 30 processors. Each memory-controller board is loaded with 8 or 16 Mbytes of memory, and each can be accompanied by a 24-Mbyte expansion board. A full-blown setup contains six controllers, for a total of 240 Mbytes of storage. The controller cards were designed with 4-Mbit chips in mind, so that when they become available, system memory will close in on the gigabyte mark. They also carry the necessary circuitry for correcting and scrubbing errors, initializing automatically, and interleaving between memory controllers.

To remain cost-effective, multiple processors must be kept busy. A potential problem in bus-based shared-memory systems is the congestion that can develop on the bus as data is moved between the memory and the processors.

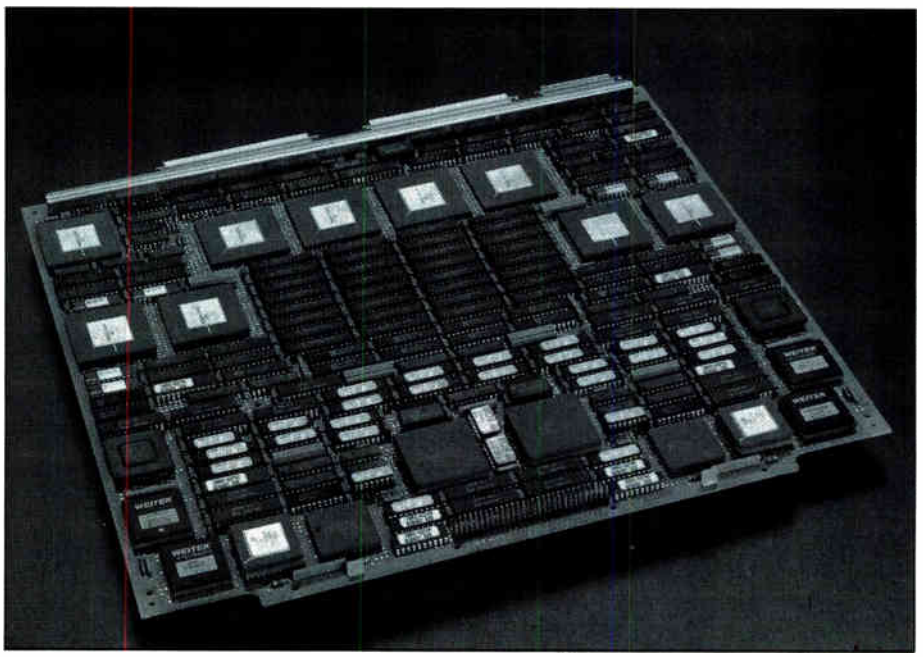
One way over that hurdle is to go with a very fast bus and high-speed memory, both of which can be expensive. The design team at Sequent took a more frugal route, enhancing the efficient, low-cost bus created for the Balance series. That accomplished, the team devoted itself to designing a cache subsystem that would hold down traffic and make the most of bus bandwidth.

The designers first built a 64-Kbyte cache into each processor. They then devised a cache-management scheme incorporating a copy-back algorithm. The algorithm guarantees that each cache remains current, or coherent, while not requiring that all writes to a cache be passed along to main memory.

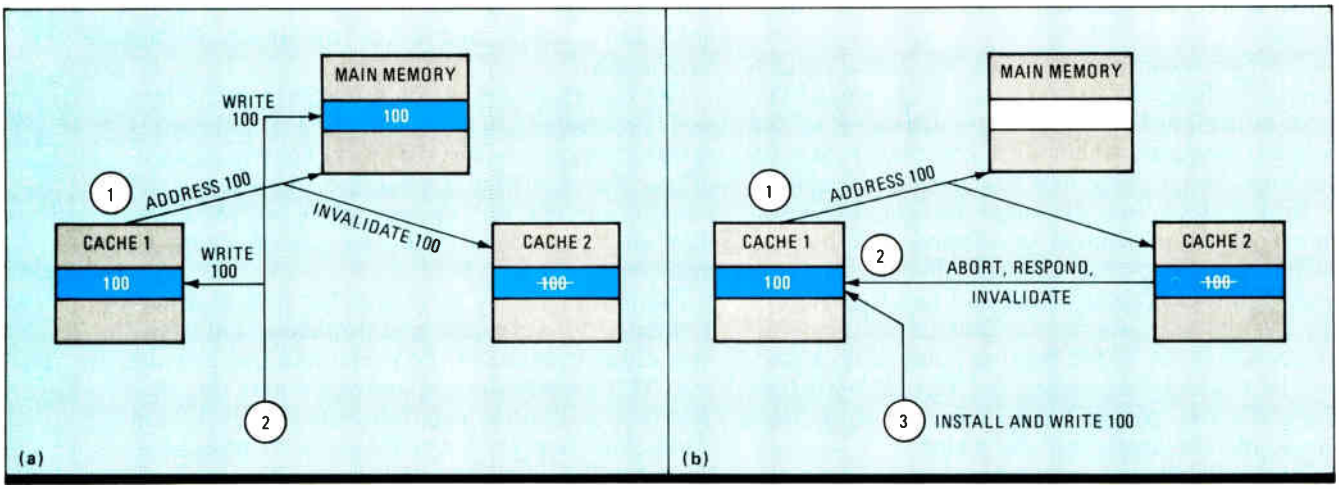
The design team's work was far from finished: it went into a huddle and brainstormed three VLSI chips to manage the cache and oversee the bus. The cache-memory controller and the bus-interface controller are fabricated with 1.2-μm CMOS gate arrays from Thomson Components-Mostek. The bus data-path controller is made with 1.2-μm CMOS standard cells.

The next item on the agenda was the crucial cache-management scheme. Key to keeping a shared-memory multiprocessor system up to snuff, the policy for handling data in the caches and passing it between them and main memory must hold down traffic on the bus. At the same time, it must react correctly when more than one processor simultaneously tries to write to the same memory location. It will neither allow a processor unrestrained access to main memory nor let every processor alter data in its cache without reflecting those changes back to main memory.

Most schemes for multiprocessor cache management employ the write-through technique: They guarantee coherence by propagating every write to a cache location back to the corresponding main memory location via the system bus. Bus-watching logic then signals each processor to invalidate the contents of that location if it is in the cache (see fig. 3a). Although the scheme



2. PACKED. One 8-layer board holds two complete CPUs—processors, caches, and control chips.



3. DATA SHUTTLE. A write-through cache (a) will write to memory whenever data in a cache is written upon by a processor. The copy-back cache scheme (b) will very often not write back to memory when a processor updates a value in its cache, thus cutting bus traffic.

ensures coherence, it does boost bus traffic.

The copy-back cache scheme does not force writes back through the bus to main memory, wasting valuable bus cycles. On the average it cuts bus traffic by 50% or more.

In Sequent's management scheme, blocks of data in a cache are tagged "private," "modified," "shared," or "invalid." When a processor requests data not in its cache—a read miss—it is read from memory. If no other copies of it exist, it is tagged as private. If that processor then wants to write over the private data, it writes to its cache without copying back to memory and tags the new data as modified. Hence the write occurs without tying up the system bus.

At this point the data in main memory is stale, and one cache contains the current value. Now the situation gets trickier. The other processors need to know that the data in main memory is no longer current. There is no problem, however, if the processor that owns the data wants to write over it again—write hits to blocks tagged as modified also proceed without bus traffic. When another processor requests modified data, the logic of the cache owning the modified block recognizes that the correct data is not in main memory but in its cache. Consequently, the valid data is copied to the requesting processor and is then tagged as shared in both caches. Since the bus is used for this transfer, the main memory is also updated on the fly. Thus shared blocks in the cache are also current in memory.

If one processor wants to write over shared data, then all other caches holding the shared data are told to tag it invalid. The requesting processor now owns the data, writes over it, and tags its copy as modified (see fig. 3b).

When a processor wants to write over data that is not in its cache but is current in memory, the write is turned into a read, saving cycles because the bus protocol is much more efficient at reading than at writing. In this instance, the data is read from main memory, stored in the cache, written over, and tagged as modified.

The data highway that ties all of the system's functional elements together is a 10-MHz synchronous bus with a 64-bit data path and a 32-bit address path. The latter is multiplexed with the data on the lower 32 lines of the 64-line bus. The speed, width, and cycle-optimizing design yield a sustainable bandwidth of 53.2 Mbytes/s out of a theoretical maximum of 80 Mbytes/s.

The bus wrings work out of every cycle. Requests to and responses from memory and input/output devices are handled asynchronously even though the bus is synchronous. Also, multiple requests to the memory and peripherals are queued and handled on a first-in, first-out basis. These FIFO queues hold up to three requests for reads from memory, two write requests to memory, and one I/O request. All initiators—CPUs, for example—can sense the state of the queues and will not transmit a request across the bus if the queue is full. Thus bus cycles are not wasted transmitting a request and a negative acknowledgement. Packet sizes for memory requests can be 1, 2, 3, 4, 8, or 16 bytes, with future expansion to 32-byte transfers planned. The most commonly used 16-byte packet matches the cache block size for efficient handling of traffic between the caches and main memory.

In multiprocessor systems with a number of shared resources, access to these resources by the processors and communication among processors must be controlled and synchronized. The Symmetry series makes good use of the test and set operations of the 386, establishing global memory-based locks used both by the operating system and by applications programs. Every memory location can be locked, and a block can be set or checked in less than a microsecond. Further, any processor that's spinning its wheels, waiting for a lock to open, executes its waiting loop entirely within its own cache, thereby freeing the system bus. *–Tom Manuel*

For more information, circle 483 on the reader service card.

SEQUENT TAKES ITS ACT ON THE ROAD

Sequent Computer Systems is taking a big step away from its competitors in parallel computing to push its already high growth rate even higher. The company is going full tilt for the huge business-automation market. Such competitors as Aliant Computer Systems and Convex Computer have instead targeted numerically intensive tasks for scientific and engineering markets.

Sequent started by aiming for the technical and engineering market. More than half of Sequent's sales since the first product was delivered in December 1984 have been to that marketplace. But Sequent has changed its marketing focus. "To achieve significant sales growth we must increase our penetration of commercial markets," says Casey Powell, president, chief executive officer, and one of Sequent's founders. In January 1983, Powell and 17 other executives left Intel Corp. to found Sequent.

Price performance is Sequent's No. 1 weapon. It just introduced its second-generation system, called Symmetry (see p. 76), which delivers 10 times more power per dollar than the leading superminicomputers and mainframes. Symmetry computers sell for $8,000 to $14,000 per million instructions per second, compared to $90,000 to $100,000 per mips for Digital Equipment Corp. VAX computers and $130,000 to $170,000 for IBM 3090 mainframe systems, according to data from Sequent.

Three years ago, the Beaverton, Ore., company was an unknown hawking an unfamiliar and untried technology. But Sequent was able to break into a sluggish market with the Balance B8 and B21.

Sequent's revenue has risen from $4.3 million in 1985 to $20 million in 1987. In its two most recent quarters, Sequent's net income was $546,000 and $825,000 (ending April 4, 1987). Sequent recently went public at $17 in an oversubscribed offering; the stock is currently selling in the mid

SEQUENT FOUNDERS. Powell (left) and Gibson pioneered in parallel processing.

$20s. By April, Sequent had sold 164 systems to 115 customers and employed 212 people, 69 of them in product development.

It was the technical, engineering, and research customers, often the early adopters of new technology, that got Sequent rolling. "These customers were the right target when the company started," says cofounder C. Scott Gibson, executive vice president and chief operating officer.

However, now that the company and its multiprocessing technology have a good track record, sales are broadening to commercial customers. "We didn't know we would end up selling in commercial markets when we started," says Gibson.

Sequent now has six major original-equipment-manufacturer contracts, including a $50 million pact

DEVELOPERS. Johnstone (left) and Gifford led the teams that developed Symmetry.

with Siemens AG of West Germany. In 1986 Siemens accounted for 19% of Sequent's net product sales. The others are Amperif, ClinCom, CLSI, MAI Basic Four, and Teradyne. Teradyne Inc. uses Sequent computers for logic and fault simulation, but the others are in business automation.

The business-automation segment of the commercial market is large and growing fast. It comprises systems that automate the highly interactive parts of a business, such as making reservations and keeping tabs on inventory.

Since most such tasks are critical in nature—reservations, for example, are the airlines' bread and butter—they are well served by the new Symmetry. The multiprocessor system maintains rapid response times as the number of users grows. It expands economically and without disruption.

However, Sequent has no intention of abandoning the technical arena in favor of business users. Thus the challenge in designing the Symmetry was to build a system that served both worlds, maintaining compatibility with the Balance series. Sequent succeeded: the same software and input/output peripherals run with both systems. "The biggest restriction was not being able to change the bus," recalls Paul Gifford, manager of central systems for Sequent. The hardware designers doubled the capacity of the bus by doubling the word size, without sacrificing compatibility. Together, the hardware engineers and the software experts, led by Ian Johnstone, manager of operating systems development, hatched a cache-memory scheme that held down traffic.

Selecting the right microprocessor was also a lot of work. The team evaluated reduced-instruction-set-computer chips as well as 32-bit processors. They settled on the 386 because it had high enough performance and allowed them to get Symmetry to market the fastest. *–Tom Manuel*

HP'S LATEST RISC SYSTEMS RUN FAST AND COST LESS

Hewlett-Packard Co.'s latest product releases in its Spectrum line are aimed at the technical and engineering marketplace. Their main claim to fame is a big jump on the price-performance curve, a move that the company says pushes it ahead of its chief competitor, Digital Equipment Corp. of Maynard, Mass. The Palo Alto, Calif., company's low-end model 825S work station is priced at $13,700 per million instructions per second, while its high-end 850S superminicomputer costs $27,800 per mips. The price for comparable VAX products from DEC, HP calculates, is $54,100 per mips and $99,000 per mips.

The Precision Architecture, HP's implementation of the reduced-instruction-set computer [*Electronics*, March 3, 1986, p. 39] used on these systems, is the key to the improved cost and performance. The architecture cuts costs and increases performance by simplifying the instruction set: each instruction can be executed in one clock cycle, because each instruction has a fixed length and a fixed format. This speeds and simplifies decoding, saving time and money.

By reducing the number of accesses to memory, the architecture also reduces cost and improves performance. Branch instructions, which typically waste a memory fetch when a branch is taken, save that memory access in the new architecture—boosting performance 10% to 20%. The architecture also uses a 32-bit register file to contain intermediate variables that otherwise would have to be put into the memory for temporary storage.

And by integrating more of the hardware onto a single chip, the architecture lowers cost and improves performance. Additional performance comes from HP's latest n-MOS III, a proprietary silicon process offering a 1.2-μm gate-width feature size. Such integration of the Precision Architecture on-chip helps the model 825S—the low-end of the three systems—rack up performance of 3.1 mips in multiuser applications (see fig. 1). The performance benchmarks that HP carried out measure system throughput as well as raw computing power of the central-processing unit. The system's principal competition, DEC's VAX 8250, achieved only 1.2 mips in the HP benchmark. HP's 850S achieved a higher 7.2 mips in the test, while its rival, the VAX 8700, mustered only 6.3 mips.

The company has also upgraded and renamed its model 840 system to the 840S, which recorded 4.5 mips in the benchmark test. By comparison, the competitive VAX 8350 system managed only 2.3 mips in the same test.

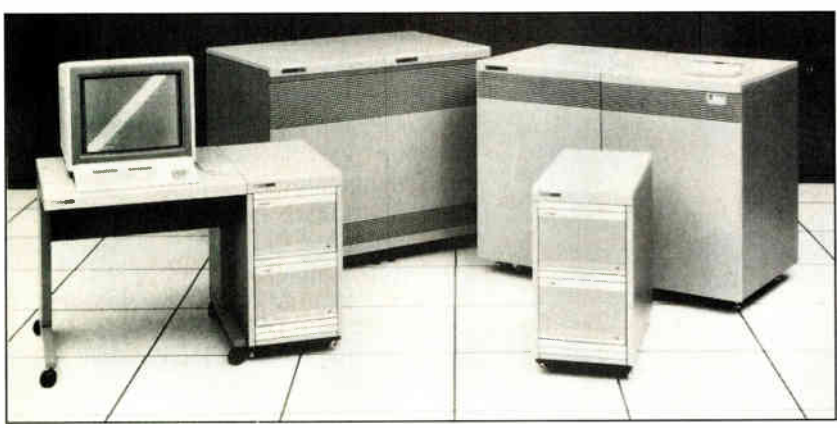
Another version of the 825, called the 825SRX, is a single-user work station. This model achieved a high 8.5 mips performance in a separate benchmark that measures only raw computing power and not system throughput.

But sheer performance is not the only edge that the HP systems have over DEC. The 825S sells for $121,700 for a system that will support 16 users, compared with $170,900 for a comparably equipped DEC system. Likewise, the price of the basic HP 850S system-processor unit is $200,000; the VAX 8700 is $502,000. The 840S, which is equipped to handle 32 users, costs $304,000, and the comparable VAX 8530 system sells for $525,000. All three of HP's systems execute HP-UX, HP's compatible version of the Unix System V operating system.

The Precision Architecture improves performance and lowers cost by allowing the processor to execute one instruction every clock cycle. Because the instructions are a fixed length, each fetch reads one instruction into the computer for execution. The instruction unit pulls an instruction out of memory every clock cycle.

The drawback of a system with conventional architecture is that it can have variable length instruction of 16 to more than 128 bits. An application performing a large number of long instructions requires a larger cache than an application performing mostly shorter instructions. Fetching 32 bits at a time, the computer can take from one to four memory accesses to fetch one instruction.

Moreover, the logic to decode the instruction is more complex on systems with a conventional architecture. The instruction unit in these systems must assemble and decode a variable-length instruction word. The decode logic must handle instructions in which the location of operation code, operand addresses, and conditional operators can vary



1. FAST FAMILY. The Precision Architecture family of computers from Hewlett-Packard now ranges in performance from 3.1 mips to 8.5 mips on the super work station (left).

with different instructions. In contrast, the fixed length and format of the Precision Architecture mean that the instruction operation code is in a specific part of the instruction, the relevant operand addresses in another prescribed location, and conditional operators in another fixed location. The simpler decode logic also reduces hardware cost.

The instruction set can be divided into three different groups. The first group, the basic arithmetic instructions—such as addition and subtraction—are very simple to execute. These instructions read data into the registers, produce a result, and place the result in a register. The second group of instructions, the load and store types that interface with the memory, takes a variable into a register or moves the variable from a register to the memory. The third type, the branch instructions, changes the program register value, which changes the location of the next instruction to execute. "Between 10% and 20% of a typical computer program can be branches," says David Fotland, the engineering project manager of HP's Information Technology Group in Cupertino, Calif.

Because all computer architectures fetch the next instruction as another is executed, a conditional branch that causes a branch wastes the memory access occurring during the execution of the branch instruction. HP's architecture contains a technique called delayed branch, which eliminates this wasted access without adding hardware cost.

"By not wasting one memory-fetch operation, the Precision Architecture actually runs 10% to 20% faster than a conventional architecture computer," says Fotland. "On some computers, to overcome the effect of wasting a memory access, the architecture prefetches down both forks of a conditional branch instruction."

The problem with this approach is that it adds cost to the system by requiring a larger prefetch cache. "With delayed branch, the computer executes the next instruction in line before the branch is actually executed," says Fotland. "So the branch takes effect one instruction after it occurs in a program sequence."

Besides saving time during a memory access, the precision architecture also reduces the overall number of memory accesses. Thirty-two general-purpose registers in the system contain intermediate variables locally, rather than storing them temporarily in memory. An add instruction in the computer produces a sum, likely to be used by another instruction later in the program, that is stored in one of the 32 registers. So rather than store the sum during one memory access and then read it back from a second memory access some microseconds later, the computer stores the result in a register.

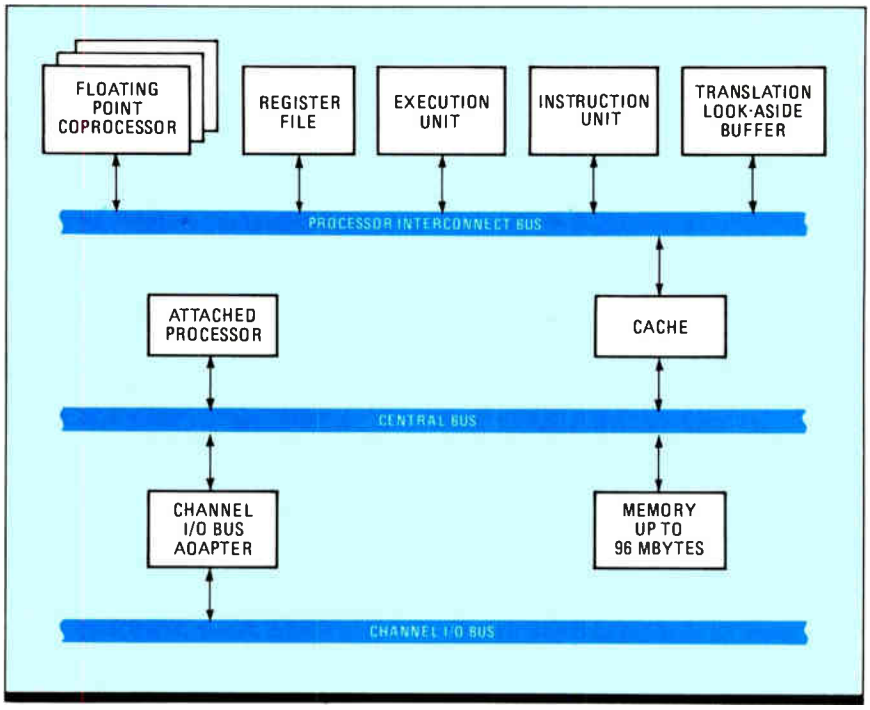
Programs are made up of loops; the same data is repeatedly operated upon. When a variable is found in the register file, the computer saves two accesses. HP researchers, in studying typical programs, determined that between 25 and 30 registers are needed to contain variables used in the course of executing a program. "We chose 32 to provide extra registers that can be used for stack pointers," says Fotland.

Using the Precision Architecture, these newer systems have integrated much of the discrete TTL logic used in the earlier generations of HP computers onto three n-MOS chips that use the latest version of the company's n-MOS III process. In this implementation (see fig. 2), a single CPU contains the instruction unit, the execution unit, and the register file. A second chip is the cache control unit, and the third is the translation lookaside-buffer control unit.

Both the buffer and the cache are in parallel. Each of them has associated random-access memory chips. In addition, a fourth chip forms the storage interface unit, and a fifth implements a math interface unit. Overall, the result is a much simpler configuration. "The model 825S has two boards that implement the CPU and floating point coprocessor," says Daniel Vivoli, product manager of HP's Fort Collins, Colo., Systems Division. "The earlier model 840 that is also based on the Precision Architecture requires seven boards to implement the same function."

–Jonah McLeod

For more information, circle 484 on the reader service card.



2. TRIPLE BUSES. HP's new architecture relies on three buses to connect the RISC-like central processor and floating point coprocessors with memory and I/O devices.

POWER SUPPLY NOISE CUT 70 dB BY MOTOROLA CODEC

A new family of codec chips from Motorola Inc. is raising the standard for power-supply noise rejection. To do this, the chips process the analog signal in a fully differential mode. The Monocircuit II codecs, which digitize and reconstruct analog voice inputs for pulse-code-modulated systems, use on-board filters and differential analog circuitry to cut power-supply noise by a factor of 3,000, or 70 dB. By contrast, competing codec chips typically exhibit a power-supply noise-rejection factor of no more than 40 dB, say developers at Motorola's MOS telecommunications chip operation in Austin, Texas.

Motorola's first new PCM codec-filters in five years balance out noise generated by power supplies by mirroring the true analog signals against inverted signals. Both signals are then passed through a fully differential path of filters and conversion circuitry.

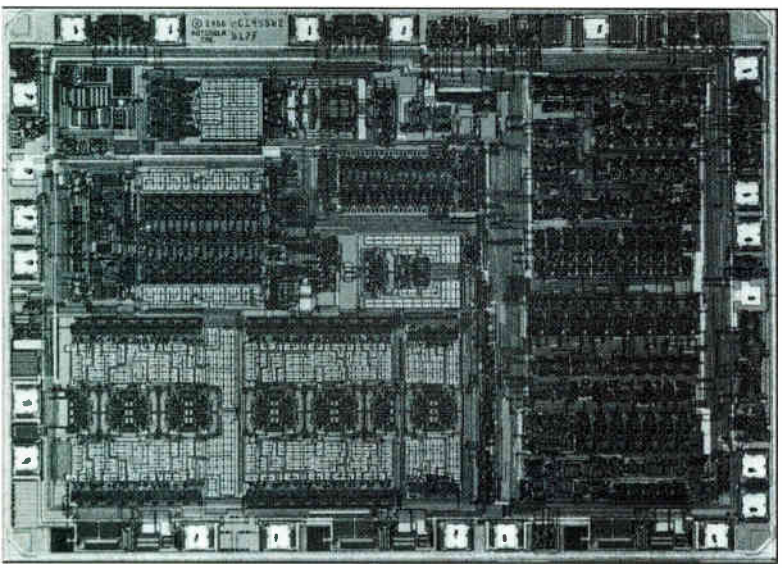
The new MC145500 family of chips is being fabricated in Motorola's 3.5-μm CMOS technology. The die size of the five Monocircuit II chips is significantly smaller than their Monocircuit 14400 predecessors [*Electronics*, Jan. 27, 1982, p. 146], and the new chips are less than half the price. Moreover, output remains a standard single-ended signal, and the new codec-filters are functionally equivalent, pin-compatible replacements for their forerunners. Applications for the five new 145500 chips include small office-telephone systems (5 to 100 lines), private-branch-exchange systems, central-office switches, transmission-channel banks, digital telephones, digital delay lines, and analog-to-digital and digital-to analog converters.

Only differential signals are processed through the analog circuitry of the CMOS chips, eliminating the common-mode inputs of power-supply-induced noise that might crop up on both true and inverted signals as a result of the way a system is designed.

Inside the 145500 codec-filters, the analog signals are placed into a differential mode in two places of the design. Incoming analog voice signals, which are to be digitized for PCM transmission, are converted into bolstered differential voltages at the output of a three-terminal operational amplifier located just before the high- and low-bandpass filters. In addition, reconstructed analog voice signals coming from PCM networks are placed into the differential mode in the chip's DAC block. The differential signals then run through a 3-kHz low-pass filter, and just before leaving the analog output the bolstered signals are converted to a single-ended mode and attenuated down to a usable signal.

By treating analog signals in a differential mode, the new MC145500 codec-filter design doubles the amplitude of voice signals processed internally, increasing the likelihood that equipment designers will be able to use the PCM codec-filters with a single +5-V power supply with an external 1.5-V reference. Historically, codec-filter chips in PCM systems have been powered by burdensome split supplies of +5 V and −5 V, which are usually more costly than a single +5-V supply.

The new 145500 family is being made in 3.5-μm double-polysilicon CMOS, versus the 5-μm single-poly process of the 14400 parts. Consequently, the die size of the 145500 codec-filter (see fig. 1) is only 28,000 mil², compared with 36,000 mil² for the older, less complex design. The finer geometries and double-poly layers of the 3.5-μm silicon-gate CMOS process also enable Motorola to double the circuits in the chip's analog path so that differential signals can be processed. Circuits mirror the low-pass and high-pass filters, as well as the chip's analog-to-digital and digital-to-analog converter block (see fig. 2).



1. **BALANCE.** The analog portion of Motorola's new codec-filter chip contains symmetrical circuits to process signals in a fully differential mode.

"Our No. 1 goal was the cost issue, especially with foreign competition coming into the markets," says Al Mouton, Motorola MOS telecommunications marketing manager. "Looking at where the industry was going [in terms of average selling price], we knew we could not achieve it with the previous design."

Motorola's 14400 monocircuits have been selling for an average price of $10. Mouton expects to see the new codec-filter chips selling closer to $4. A 16-pin MC145503 general-purpose part, designed for both synchronous and asynchronous applications, is

now available for $3.90 each in 10,000-piece quantities. The 22-pin 145502—fully loaded will all the current monocircuit options—costs $4.51 in 10,000-piece quantities. In addition, customized 145500 chips are planned, says Mouton.

While refitting the codec-filter for a lower-cost process, Motorola also aimed for higher performance, believing that power-supply noise rejection is fast becoming a key system issue. "More and more digital telephone systems are going to inherently noisier switching power supplies, and smaller line cards are becoming packed [with ICs, large buses, and telephone channels]," says Mouton, who notes that board sizes are down to 8 in. from 12 in. and now contain as many as 16 codecs, versus four in 1980. Noise from power supplies causes constant hissing sounds, or white noise, on telephone lines. This problem could require equipment houses to use expensive power supplies or add components in front of the codec-filter chips to reduce noise in order to get products to comply with telephony standards.

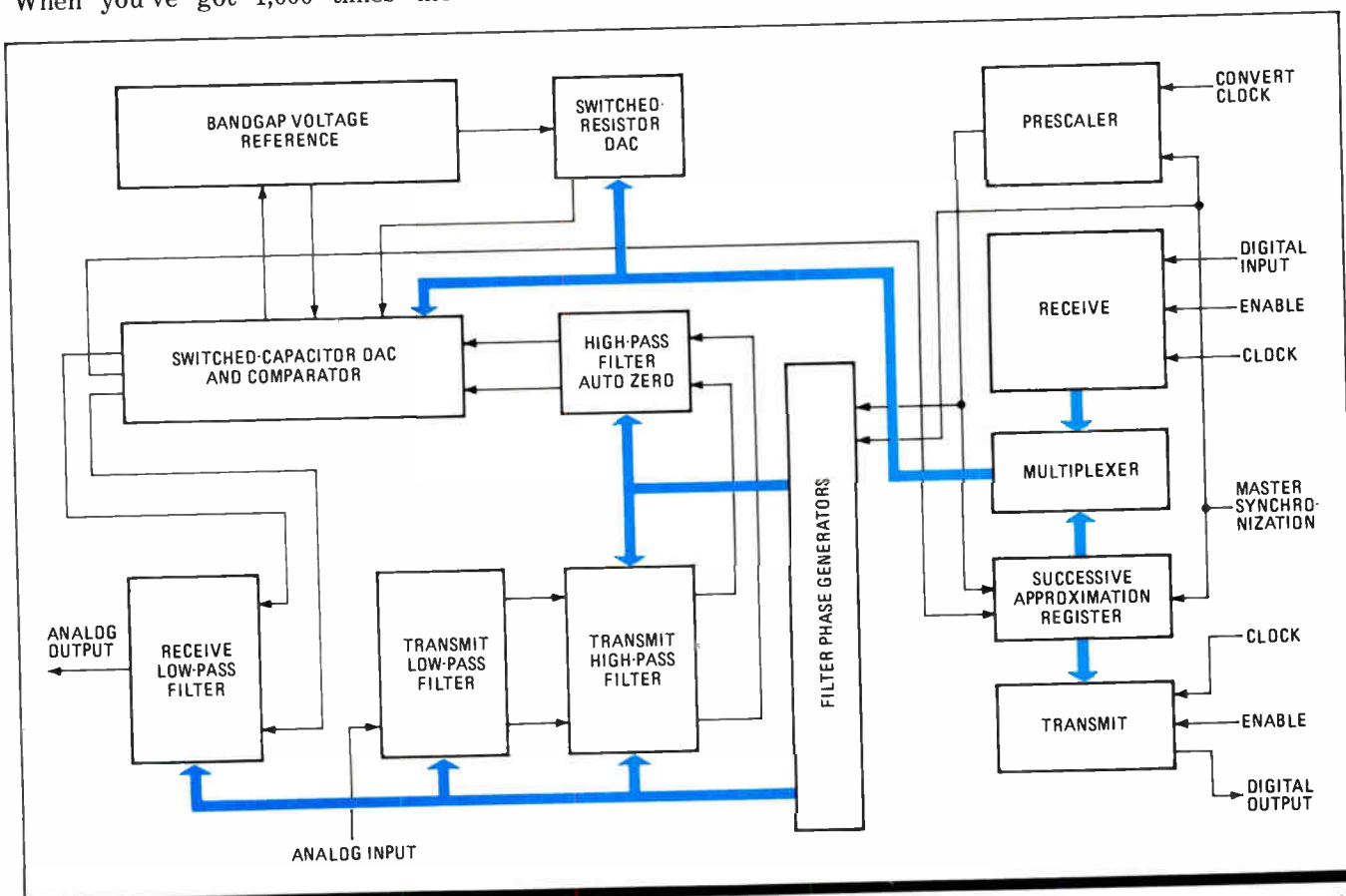
"We are talking about potentially millivolts of noise from power supplies, while the amount of noise you want to be measuring in the analog signal path is down in the microvolt range. Telephone systems are able to tolerate on the order of 300-350 μV of maximum noise," notes Motorola telecommunications engineer Mike Floyd. "When you've got 1,000 times the maximum noise on the power supplies, you need to have [a rejection ratio] on the order of 60 dB. With that power-supply rejection ratio, noise that comes through is attenuated to an insignificant factor.

"All of the differential circuitry on the chip is as symmetrical as possible," he continues. "In that environment, all of the parasitics and noise that might come in through the power supply appear as a common mode [on both true and inverted signals]. In the differential design, the only signal that actually gets processed is the differential signal. Common-mode signals are not, and they go through transparently."

The chips have a precision bandgap voltage reference, allowing single or split power supplies of 7 to 12 V or ±3.5 to ±6 V. The single +5-V operation can be achieved with an external 1.5-V reference. Typical power dissipation of the parts is 50 mW active and 0.1 mW in the power-down mode.

The differential design technique used in the 145500 reduces the margin between the absolute voltage required for the analog signal and the power supply. The circuit designs require only 1 V of headroom, or margin, meaning that a chip running off a single +5-V power supply will have a peak-to-peak operating range of 3 V. Because the differential circuit doubles the amplitude, the actual internal peak-to-peak range is 6 V for processing signals. *–J. Robert Lineback*

For more information, circle 486 on the reader service card.



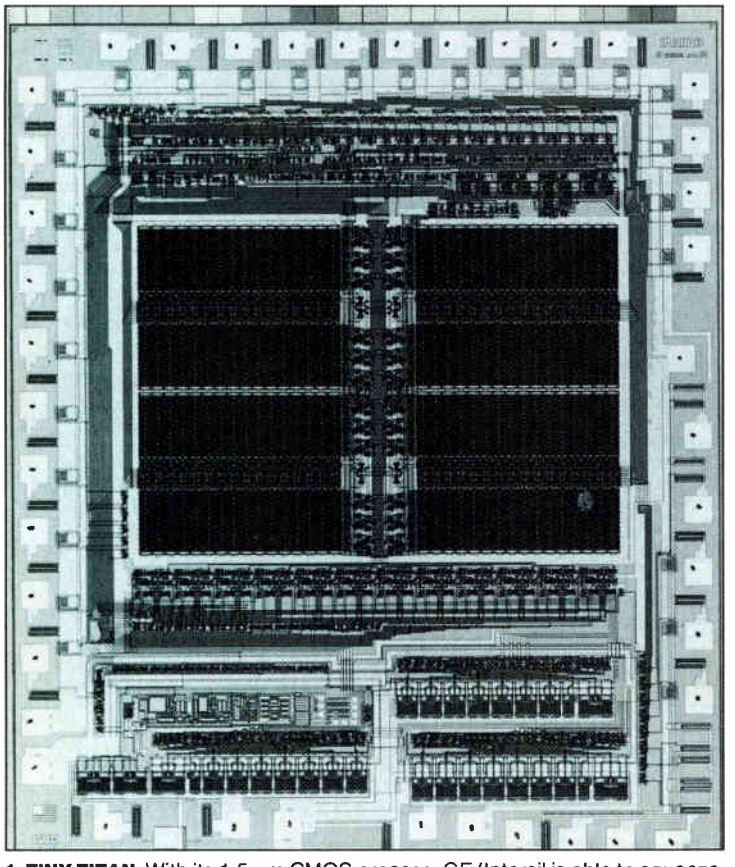
2. DOUBLING UP. The 145500 architecture has functional blocks identical to those in Motorola's first-generation codec-filters, but differentia processing of analog signals provides greater immunity to noise from switching power supplies.

GE/INTERSIL BRINGS VLSI TO THE ANALOG WORLD

With the introduction of its new color video digital-to-analog converter, GE/Intersil has brought true VLSI to the analog world. The IM2110, which uses 1.5-μm design rules, is the first commercially available analog CMOS circuit to break the 2-μm barrier. The 25-MHz chip is aimed at the midrange of price and performance: high-end personal computers and low-end work stations.

With the IM2110's 1.5-μm process, GE/Intersil has been able to cram about 25,000 transistors onto a die that measures only 169 by 192 mils (see fig. 1). That's 25% to 30% smaller than most currently available color video DACs, says senior design engineer Chris Patterson. And despite this smaller size, the chip packs a great deal more functionality than competing color-video DAC chips, he notes.

The IM2110, like most color-video DAC chips, includes three 4-bit DACs and a dual-ported color palette random-access memory of 256 by 12 bits, plus associated synchronization and control logic. The internal color palette RAM uses a two-level pipeline structure to cut delay time between input and output by 50%, from a non-pipelined chip's 80 ns down to just 40 ns at 25 MHz.



1. TINY TITAN. With its 1.5-μm CMOS process, GE/Intersil is able to squeeze 25,000 transistors onto a die that is 25% smaller than other video DACs.

The chip also has its own general-purpose microprocessor interface and an on-chip temperature-compensated band-gap reference, simplifying system design and reducing chip count. And in addition to the chip's registers for storing color-table values, there are also three on-board overlay registers that allow grids, cursors, and text to be displayed on top of the graphics (see fig. 2).

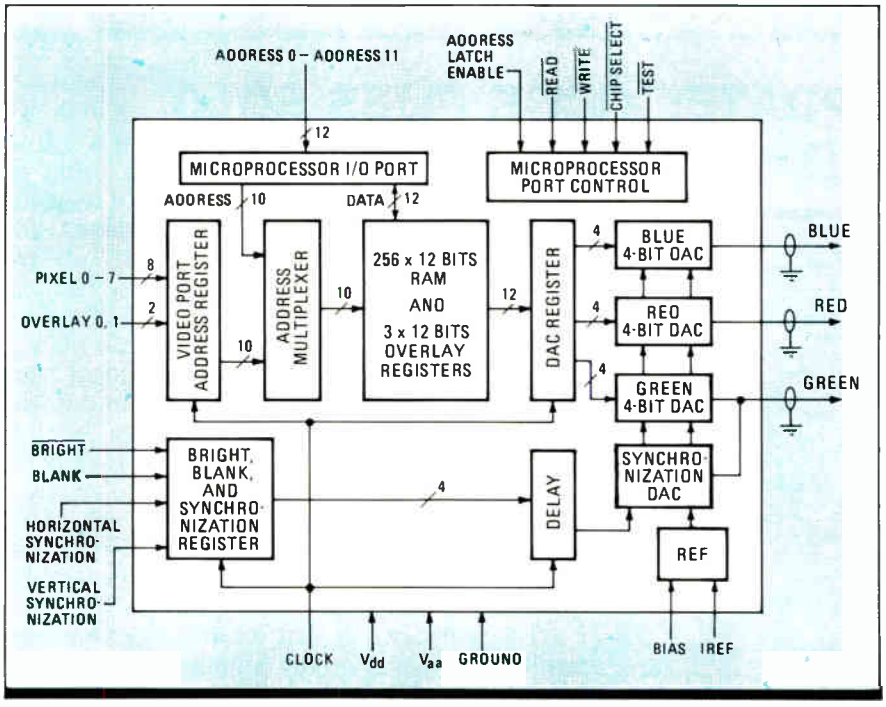
The device can simultaneously display 256 out of 4,096 colors in a 640-by-680-pixel noninterlaced display. It generates RS-343-A-compatible red, green, and blue analog signals and is capable of directly driving doubly terminated 75-Ω coaxial cables. The overlay can be displayed in any three colors out of the 4,096 available.

To break the 2-μm analog VLSI barrier, GE/Intersil engineers used as their starting point a high-performance p-well bulk CMOS process that uses a retrograde implant to improve latchup, two levels of aluminum interconnect, and two levels of polysilicon. To this they added a special set of steps that optimize the process for analog functions. These include the use of a nitride dielectric to improve interlevel isolation, an additional metal layer, and the use of molybdenum to form sub-2-μm resistor strings with resistivity values and electron-migration characteristics that match many less-dense analog CMOS processes.

Of four possible capacitor structures that can be fabricated with GE/Intersil's analog VLSI process, three have electrical properties equivalent to LSI and MSI CMOS processes (see fig. 3). "These three capacitors—formed, respectively, from the two levels of metal, the two levels of polysilicon, and the first metal and an additional metal layer—all feature 15-V breakdown voltage, less than 4 A/cm^2 of leakage, and temperature coefficients in the range of 50 to 55 parts per million per degree C," says design engineering manager Everett L. Bird. "The two metal-to-metal capacitor structures have voltage coefficients in the 10 to 40 ppm/V range."

Most competitive devices use an external voltage reference, usually a bipolar device and several passive components. The IM2110, though, uses the parasitic npn bipolar transistor inherent in the CMOS process as a bandgap reference, thereby incorporating the voltage-reference function onto the chip, says Patterson. Extensive use has also been made of the inherent npn structures throughout the chip as emitter-follower drivers in many of the linear blocks, he adds.

The IM2110 also incorporates circuitry to reduce the so-called glitch-energy problem that plagues many DACs. "The problem with a lot of parts is that when the converter changes codes in midrange, an intermittent voltage spike is produced," says Patterson. "In a video system, this



2. LOADED. The IM2110 has overlay registers, voltage reference, and a microprocessor interface.

usually shows up in the form of snow or visible white bands between adjacent colors." The problem occurs in traditional DAC designs that use binary-weighted current sources, where bits are manipulated in large 2-, 4-, and 8-bit combinations; this produces large glitch-energy sources when the output goes positive. This is solved in the IM2110 by using a segment-weighted approach, in which each current source is manipulated separately. When a code transition occurs, the resulting energy does not exceed 1 least significant bit.

On the digital side, the designers added several features to enhance performance. For example, most video DACs do text overlays through the use of external circuitry, but the IM2110 has three overlay registers on-chip, in addition to the color palette memory. "By incorporating the overlay registers on-chip, not only is component count reduced, but throughput is increased by as much as 50%, depending on system configuration," says Patterson.

Performance is also improved by the two-level pipeline architecture in the internal SRAM-based color-lookup table. Throughput time is cut in half by adding registers on the input and output of the RAM, allowing the RAM to be addressed, video data to be acquired, and precharging to be performed in a single clock cycle.

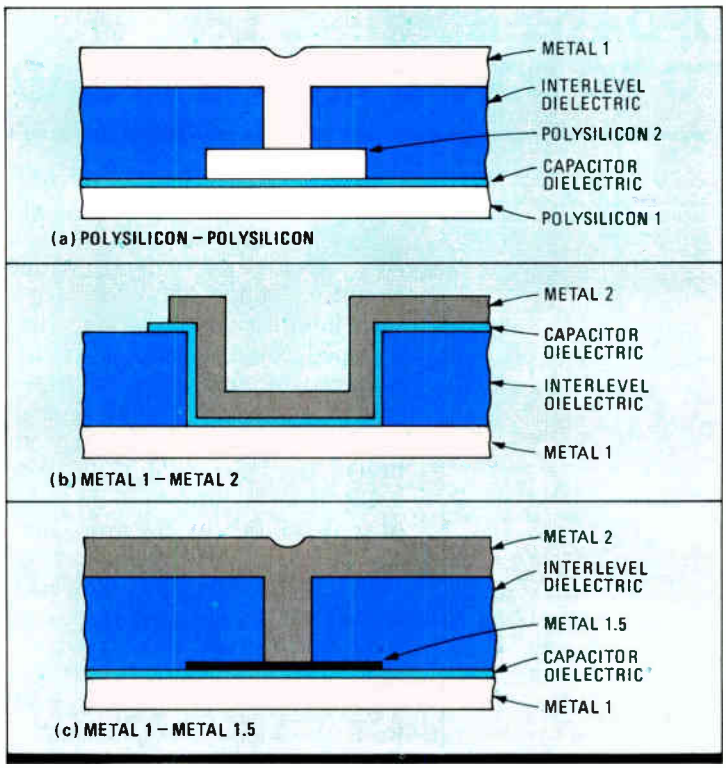
Finally, the IM2110 incorporates a 12-bit microprocessor interface to external CPUs. This interface allows the IM2110 to operate asynchronously, unlike other video DACs, since the microprocessor can write into or read from the converter's on-chip RAM at the same time as RAM data is being transferred to the video outputs via the normal 8-bit video interface.

The IM2110 is built with the same process that GE/Intersil uses to build its digital signal processing parts, says Norman Wheelock, director of marketing for digital products. "What our success in making this part tells us is that not only are there a number of different ways to go in the video DAC market—higher performance, higher functionality, as well as higher accuracy—but a number of ways to combine high-density ADC and DAC functions with the DSP blocks as well," he says. "Rather than separating the conversion to and from the analog world from the signal processing, this process will allow us to combine both functions on a single chip."

Unlike most color video DACs, which are aimed at applications in excess of 50 MHz, the 25-MHz IM2110 is being aimed at high-end personal computers and low-end work stations. It incorporates all of the interface logic necessary for the next generation of Personal Computer Graphics cards, including IBM Corp.'s Professional Graphics Adapter standard. Wheelock says that the IM2110 is also being aimed at such medium-range applications as heads-up displays for military vehicles and tactical displays for radar and sonar systems.

–Bernard C. Cole

For more information, circle 487 on the reader service card.



3. CHOICES. GE/Intersil's 1.5-μm analog VLSI process allows fabrication of three types of capacitor structures that perform as well as LSI and MSI CMOS structures.

UPDATE: XICOR FLIES SOLO WITH THICK-OXIDE EEPROM


THICK OXIDE BEATS THIN FILM IN BUILDING BIG EEPROMS

XICOR USES IT TO SOLVE 3-D SCALING PROBLEMS IN 256-K CHIPS

Since the introduction of its 256-Kbit electrically erasable programmable read-only memory last year, Xicor Inc. has had some good news and some bad news. The good news is that after the introduction of the X28256, the company moved quickly into volume production. It is now averaging a run rate in excess of 10,000 units per month, and production is going up.

The bad news is that Xicor is still the industry's only supplier and manufacturer of EEPROMs that are fabricated using a thick-oxide triple-polysilicon approach [*Electronics*, May 12, 1986, p. 30]. A joint technology-development agreement with Intel Corp. was called off in April. Intel is discontinuing its work with thick-oxide triple-poly, according to a company spokeswoman, in favor of other alternatives to achieving high density EEPROMs.

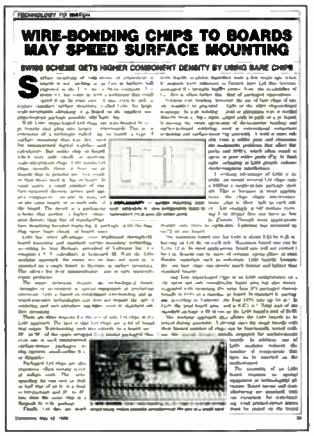
Intel's departure has not deterred Xicor, though. The company is completing development of a CMOS version of the chip, the X28C256, and a 1-Mbit version, as yet unnamed. It has successfully completed qualification to MIL-STD-883C class B for all versions of the X28256 in a 28-pin CERDIP package and in a 32-pad leadless chip carrier package.

Xicor's original goal was to push EEPROMs to 256 Kbits, past the 64-Kbit barrier where conventional EEPROMs stopped. The key to leaping that hurdle was the way most EEPROMs are fabricated—with a thin-oxide, double-poly technology derived from ultraviolet erasable PROMs. Although relatively easy to manufacture at 2-μm geometries, thin-oxide devices cannot easily be scaled down to achieve higher densities without introducing significant reliability problems.

The problem is that besides pushing horizontal geometries down to 1 to 1.5 μm, vertical geometries must be reduced proportionately. That is difficult to do in thin-oxide devices that are already pushing the limits of reliability at a thickness of 80 to 100 Å. But by using the thick-oxide, triple-poly process, Xicor engineers achieved much higher densities in the 256-Kbit EEPROM, while only scaling down from 3 μm to 2 μm horizontally and from 600 Å down to 400 Å vertically.

–Bernard C. Cole

UPDATE: BONDING LSI TO PC BOARD MOVES AHEAD


WIRE-BONDING CHIPS TO BOARDS MAY SPEED SURFACE MOUNTING

SWISS SCHEME GETS HIGHER COMPONENT DENSITY BY USING BARE CHIPS

A year ago, Valtronic SA reported that it had come up with a new method of surface mounting called LSIS, for large-scale-integration shrinking, that it hoped could speed up the acceptance of surface mounting—and in some cases replace conventional surface mounting entirely [*Electronics*, May 12, 1986, p. 33]. It looks now as if the company is on its way toward reaching at least the first goal.

The Swiss company is already marketing a smart-modem module in Europe and is in the process of getting approval from the Federal Communications Commission to sell it in the U. S. It also has used its technique to build a new video random-access memory module and a static RAM module. In another area, it has won two contracts to assemble smart cards. One contract, with a Swiss customer, is for a medical card that stores a patient's medical history. The second is with a French company that prefers to keep its application secret.

Valtronic's approach to surface mounting is a variation of chip-on-board technology. It is a method of wirebonding multiple bare integrated-circuit chips to small printed-circuit boards. Unlike other chip-on-board methods, however, which use small- or medium-scale-integration chips, the Valtronics approach bonds LSI chips to a pc board. The approach permits a higher component density than does conventional surface mounting, because replacing IC packages with bare chips saves a large amount of board area.

Valtronic's next move is to consolidate its position in the U. S., says George Rochat, a director of the company. An office and a laboratory were established in Cleveland early this year. Within the next few months, the lab will handle all prototypes for the U. S. By the end of 1987, a pilot line should be running there. In the first quarter of next year, the company says, full production operations will begin at a new facility, the location of which has not yet been chosen.

Meanwhile, Valtronic is evaluating wafer bumping as a first step toward tape-automated bonding. The company thinks TAB may be a way to make its next logical move—bonding VLSI rather than LSI chips.

–Jerry Lyman

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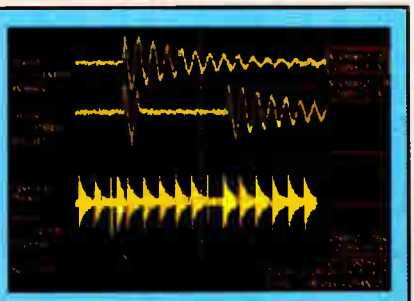
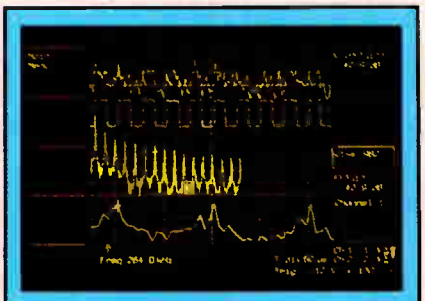


Switching transients recorded in segmented memories show contact bounce in segment number 3. Cursors can measure bounce-time-interval precisely.



Noisy R.E. Transmission Signal is averaged in time domain. Spectral content of cleaned-up signal is analyzed by FFT.

Inverted photo-diode signal is normalized then integrated for energy measurement (area under curve =11.44 nVs). Differential dC/dt is shown as well.

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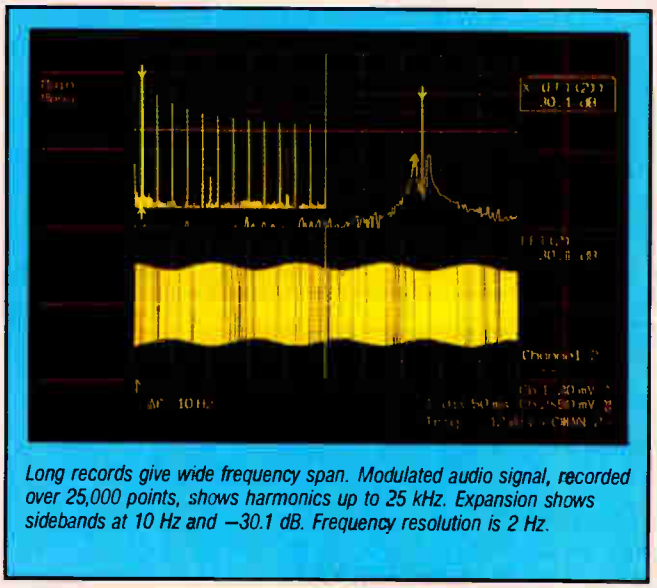

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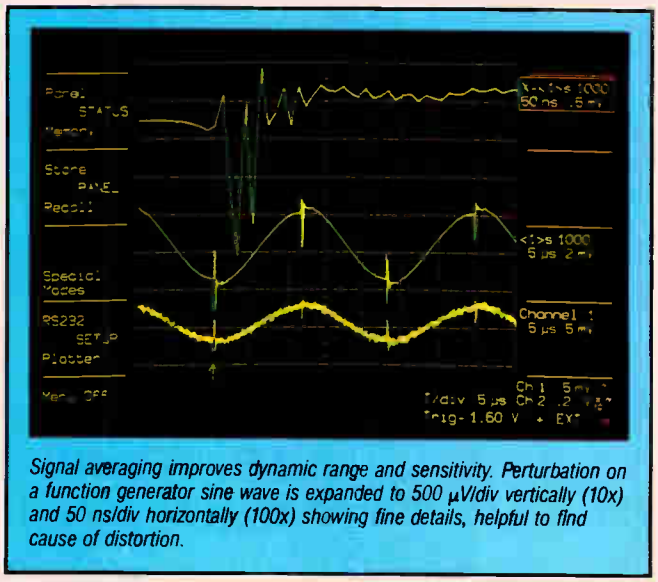

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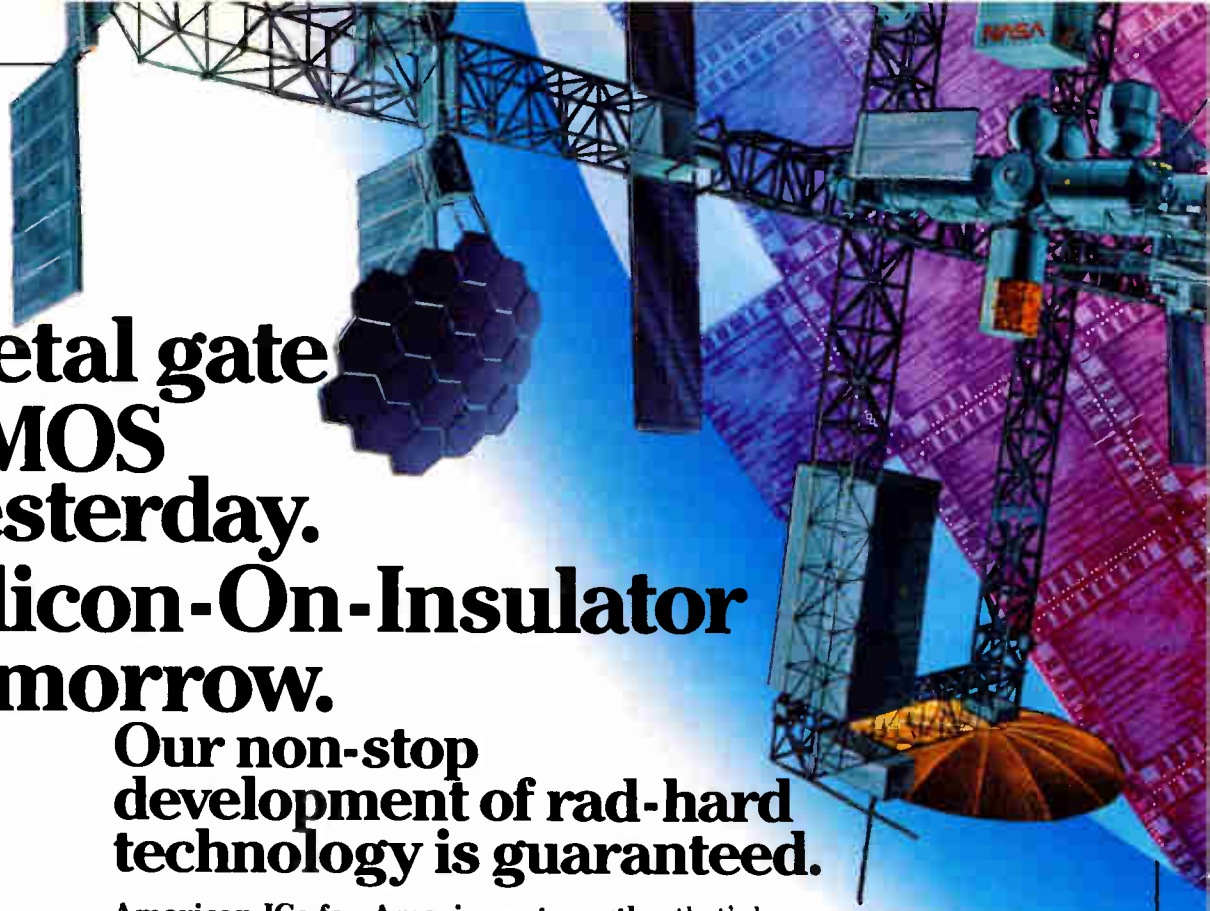

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MILITARY/AEROSPACE NEWSLETTER

DOD'S FIRST GATE ARRAY STANDARDS SHOULD BOOST MARKET GROWTH

Pentagon procurement officials have made it easier for vendors to specify gate arrays in their system designs. The use of gate arrays should grow even faster now that military equipment developers will no longer be required to use source control drawings to get around the lengthy procedure of qualifying each of their designs [*Electronics*, Oct. 16, 1986, p. 31]. Already, a 60% jump in gate-array usage in military systems has been charted over the past six months by the Defense Electronics Supply Center. And a study by Integrated Circuit Engineering Corp., Scottsdale, Ariz., shows gate arrays will make up 67% of the $548 million U. S. military ASIC market in 1991. DESC has notified industry companies and military agencies that it has approved the long-awaited specifications for bipolar and CMOS gate arrays. Standard MIL-M-38510/600 covers bipolar devices, and MIL-M-38510/605 relates to CMOS products. An additional six "slash sheets" will be released by DESC over the next six to eight months, covering packaging combinations and other technical specifications. DESC officials say 17 device manufacturers have expressed interest in qualifying CMOS gate arrays under the new standard. In recent weeks, DESC has mailed some 1,200 copies of the specs to military hardware makers and DOD agencies. □

REPORT CARDS FOR SOFTWARE VENDORS TO HELP DOD PICK CONTRACTORS

The Defense Department's Software Engineering Institute earlier this month sent out for review copies of an assessment guide designed to appraise the software-engineering capabilities of Pentagon software suppliers. Copies were mailed to 120 companies with which the SEI has signed an information exchange agreement, as well as military agencies. The guide asks 160 "yes" or "no" questions aimed at determining an organization's software capabilities. The questions cover four areas: organization, software engineering process and management, process tools, and technology. William Sweet, manager of the project, says the guide was also designed to be used by companies and DOD agencies as an internal tool—essentially to grade themselves. Workshops will be scheduled in the fall to train vendor and government teams in how to use the document. The SEI began work on the assessment guide when the Air Force asked for help in recognizing good software engineering capabilities in potential contractors. The guide will be published in September for general trial use by all Pentagon software vendors. □

DEC TO HELP DEVELOP GATEWAYS BETWEEN DOD AND OPEN-SYSTEMS PROTOCOLS

Digital Equipment Corp. will join a cooperative effort between the Defense Communications Agency, the National Bureau of Standards, and Network Research Corp. to develop design specifications and prototypes for gateways between the Pentagon's communications protocols and Open Systems Interconnection networking protocols. When completed, these specs and testing procedures will be available to computer and communications vendors and test service organizations for use in developing gateway products that link DOD and OSI networking protocols. Gateways between DOD and OSI protocols will enable the DOD and other federal agencies to begin migrating to international standards, according to an OSI procurement specification being prepared for government use. Specifications are being developed for two gateways: One will link the DOD electronic mail protocol; the other will connect the military's file-transfer protocol and OSI's file-transfer, access, and management protocol. DEC is contributing consulting services and the use of its OSI-compatible networking software to the project. Network Research, Oxnard, Calif., is also providing networking software and consulting engineers to the effort. □

MILITARY/AEROSPACE NEWSLETTER

THE PINOUT BATTLE IN IC LOGIC HITS THE MILITARY MARKET

The industry battle over proposed pinout changes for the new generation of CMOS glue logic has marched right into the military chip market. Military component managers at Texas Instruments Inc. expect the Defense Electronics Supply Center in Dayton, Ohio, to soon issue a second DESC source-drawing for advanced CMOS logic with the TI-backed changes in standard pinouts. TI is pushing to move ground and power pins from the corners of dual in-line packages to the centers. The switch—along with additional power and ground pins on some functions—is aimed at reducing lead inductance, which can cause system noise spikes as multiple outputs are switched in the speedy CMOS parts. DESC will also have a drawing for the traditional pinout, which is backed by Fairchild Semiconductor Corp. and General Electric/RCA. Ironically, a key victory in the new military-pinout skirmish could be decided by General Electric Co. in Pittsfield, Mass., which has already begun characterizing electrical performance (including noise spike potentials) and assessing overall quality of RCA, Fairchild, and TI parts as part of a new two-year contract from the Air Force's Rome Air Development Center in Rome, N.Y. Preliminary results are expected in two to three months. The Rome center hopes the study will help it decide which pinout to use in future defense systems. □

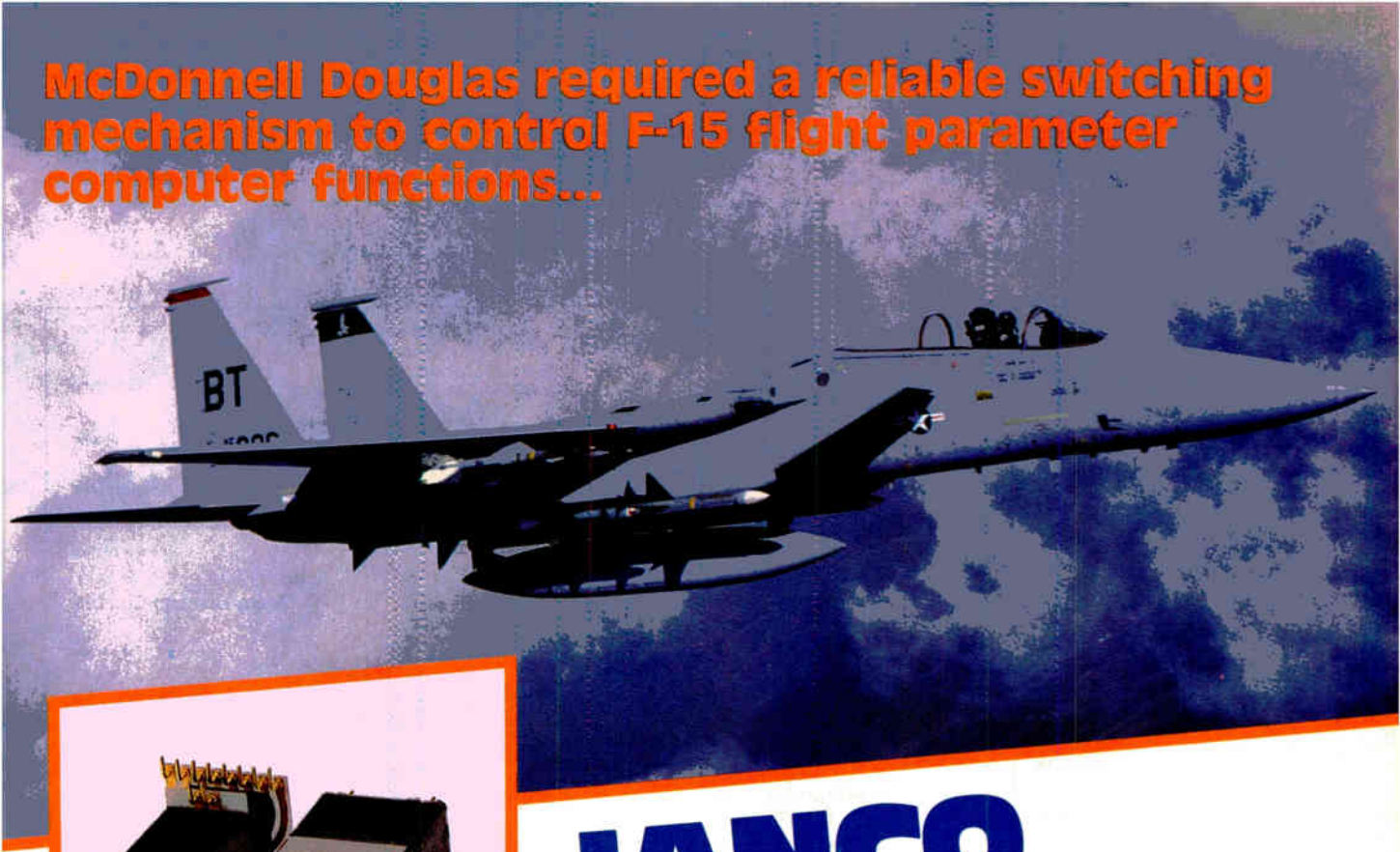
NEW DOD GUIDELINES FOR SECURE NETWORKS COULD SEE COMMERCIAL USE

New guidelines for secured computer networks won't be published by the National Computer Security Center until August. But the document is already generating enough interest to indicate that the guidelines may be adopted—wholly or in part—for commercial use. "We have received queries from many companies, but mainly financial institutions, about the new guidelines," says an official of the Ft. George G. Meade, Md., agency. Called the Brown Book when the Pentagon security center began work on it in late 1983, the final version will be based on interpretations of the agency's Trusted Computer Systems Evaluation Criteria, the so-called Orange Book, which describes the Pentagon's criteria for securing computer hardware and software [*Electronics*, March 5, 1987, p. 87]. It will be called Trusted Network Interpretations. Besides addressing what's in the Orange Book, the guidelines will cover integrity and denial of access in local- and wide-area networks. □

STAR WARS R&D MAY ALSO IMPROVE CONVENTIONAL DEFENSES

Star Wars research and development work may end up transferring technology to conventional defense systems as well. The Pentagon has just sent Congress a report detailing possible spinoffs for conventional defense. The study from the Strategic Defense Initiative Organization suggests that its R&D can help develop better near-term ballistic-missile defenses as well as provide technology to protect the nation's communications, navigation, and satellite networks. SDI officials provided more details in recent meetings with industry executives. They included the preliminary design of an x-band phased-array terminal imaging radar capable of producing high-resolution images of distant targets. This technology, which can identify warheads high in the atmosphere, will reach the experimental test stage within the next two years, according to SDI. The Star Wars agency also is claiming significant progress in new ultra-short-wavelength laboratory lasers for lithography and X-ray laser studies; optical switches for applications in sixth-generation optical computers; new mathematical techniques and numerical algorithms for faster and more accurate target determination, tracking, and discrimination; and composite materials that can withstand high temperatures for extended periods of time. □

McDonnell Douglas required a reliable switching mechanism to control F-15 flight parameter computer functions...



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Circle 93 on reader service card

HOW SALOMON BROTHERS' M&A HELPS ADVANCE TECHNOLOGY.

October 7, 1986 **Aeronca, Inc.** has been acquired by **Fleet Aerospace Corporation**	January 28, 1986 **Applied Data Research, Inc.** has been acquired by **American Information Technologies Corporation**	October 1, 1986 **The Chase Manhattan Corporation** has sold its indirect wholly-owned subsidiary **Computer Power Inc.** in a leveraged buyout transaction to **CPI Acquisition, Inc.** a new corporation formed by members of the management of Computer Power Inc.	July, 1986 **Citicorp** has acquired **Quotron Systems, Inc.**
June 11, 1986 **Mitel Corporation** has sold 51% of its common shares to **British Telecommunications plc**	November 13, 1986 **M/A-COM, Inc.** has sold **M/A-COM Information Systems, Inc.** to **Centel Corporation**	October 14, 1986 **M/A-COM, Inc.** has sold its wholly-owned subsidiary **Cable/Home Communication Corp.** to **General Instrument Corporation**	December 24, 1986 **Osaka Titanium Co., Ltd.** has acquired **U.S. Semiconductor Corporation**
July 29, 1986 **Power Conversion, Inc.** has been acquired by **Hawker Siddeley Group** **Public Limited Company**	November 21, 1986 **Teknekron Financial Systems, Inc.** a majority-owned subsidiary of **Teknekron Industries, Inc.** has been acquired by **TRW Inc.**	March 18, 1986 **Textron Inc.** has sold its **Dalmo Victor Division** to **The Singer Company**	October 30, 1986 **TRW Inc.** has sold its **Aviation Product Support Division** to **Aviation Product Support, Inc.** a subsidiary of **Kleco Corporation**
October 30, 1986 **TRW Inc.** has sold **TRW Turbine Overhaul Services Private Limited** to **Kleco Corporation**	October 30, 1986 **TRW Inc.** has sold its **Turbine Airfoils Division** to **Chromalloy American Corporation**	October 30, 1986 **TRW Inc.** has sold its **Power Accessories Division** to **Argo-Tech Corporation**	October 30, 1986 **TRW Inc.** has sold its **Compressor Components Division** to **Ex-Cell-O Corporation**
October 30, 1986 **TRW Inc.** has sold its **Castings Division** to **PCC Airfoils, Inc.** a subsidiary of **Precision Castparts Corp.**	July 29, 1986 **U S WEST Information Systems, Inc.** a wholly-owned subsidiary of **U S WEST, Inc.** has acquired **Applied Communications, Inc.**	May 6, 1986 **Western Union Corporation** has sold the assets of its **Government Systems Division** to **American Satellite Company** a subsidiary of **Contel Corporation**	November 13, 1986 **Xertex Corporation** has sold substantially all its assets to **Emerson Electric Co.**

Helping technology companies meet their M&A objectives is a specialty of Salomon Brothers. So much so, in fact, that during 1986, we completed more M&A transactions involving technology companies than any other investment bank.

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NEW PRODUCTS

TWO-CHIP MODEM DELIVERS FULL-FEATURED PERFORMANCE

EXAR'S 2,400-BAUD SET WORKS WITH MOST MICROCONTROLLERS

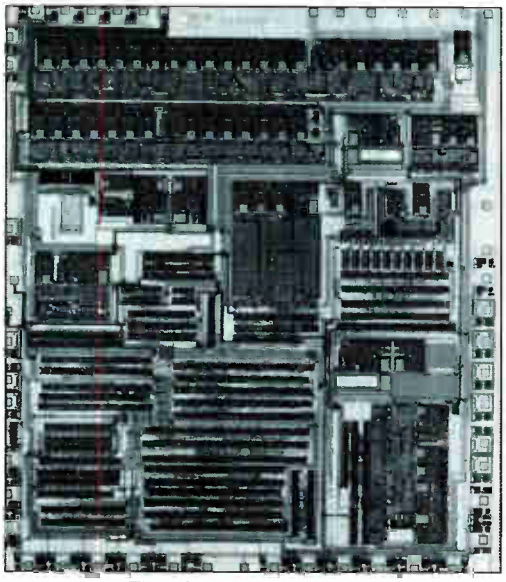
Aiming to provide high functionality but still make life easier for designers, Exar Corp. has employed digital signal processing technology to develop a two-chip 2,400-bit/s modem that provides all of the functions required for operation under the Bell 212A or CCITT V.22bis standards. The chip set can be used with most commercially available microcontrollers.

Jim Lange, applications engineering manager at Exar, says the two-chip XR-2400 modem is unique because it uses digital signal processing exclusively to perform all the modulator/demodulator functions. Competitive devices, he says, either use a totally analog processing approach or divide operations into separate digital and analog functions. "While such approaches are adequate for operations at 300 and 1,200 bits/s, at 2,400 bits/s a totally digital-signal-processing approach is necessary," he says.

3 SPEEDS. Designed to operate at 300, 1,200, and 2,400 bits/s, the chip set consists of the XR-2401 DSP modem signal processor and the XR-2402 DSP interface. The 40-pin XR-2401 incorporates the modulation/demodulation circuitry, as well as such functions as carrier detection, automatic gain control, timing recovery, adaptive equalization, carrier recovery, and tone generation.

The 48-pin XR-2402 chip interfaces the XR-2401 with the telephone line and the microcontroller needed to run handshaking protocols and dialing control. "Unlike other competitive devices, which are designed to work with a specific type of microcontroller such as the Intel Corp. 8051 or 8096, the XR-2402 incorporates a general-purpose microprocessor interface that allows it to be used with virtually any commercially available microcontroller," says Lange. However, because of its wide use in the industry, the company recommends using the 8051 microprocessor, he says.

The XR-2402 also carries an analog-to-digital converter, a digital-to-analog converter, a band-splitting filter, a programmable-gain amplifier, asynchronous-to-synchronous and synchronous-to-asynchronous converters, and a guard-tone generator.



INTERFACE. The XR-2402 links the modem chip with the telephone line and microcontroller.

The modem chip set features advanced functions, including automatic dialing, which allows the modem to work without a telephone or to perform unattended dialing, and call-progress monitoring, which instructs the modem to ring back after a few minutes if it gets a busy signal.

Also incorporated in the two chips is circuitry that performs a variety of self-test functions through the use of a loop-back feature. The XR-2400 set can perform analog loop-back and digital loop-back for transmit-and-receive testing, and remote digital loop-back for long-distance testing, says Lange.

Fabricated in a silicon-gate CMOS process, the XR-2401 operates off a single +5-V supply, whereas the XR-2402 uses +5-V supplies. Combined power dissipation is 1 W. Under development for the European market is an 18-pin device that will allow the chip set to satisfy the CCITT 300-bit/s V.21 standard, Lange says.

The chips are available now in both plastic and ceramic packages. The XR-2401 costs $18 each and the XR-2402 is $12 each in 10,000-unit quantities.

–Bernard C. Cole

Exar Corp. 750 Palomar Ave., Sunnyvale, Calif. 94086.
Phone (408) 732-7970 [Circle 440]

VIDEOPHONE ADD-ON PUTS IMAGES IN DISK STORAGE

Still-frame pictures snapped by a proprietary videophone-camera can now be stored in a digital database for remote retrieval and display on other videophones. Image Data Corp.'s PhotoLink system does the trick by harnessing a proprietary compression algorithm to a personal-computer file server and transmitting the images over standard telephone lines.

The system is a major addition to the San Antonio, Texas, company's Photophone product line [*Electronics*, Aug. 19, 1985, p. 34). Based on an Intel Corp. 80186 microprocessor, PhotoLink is an image-processing module that interfaces the file server—an IBM Corp. PC AT or compatible—with the Photophone network. Networking software and a database applications program called PhotoFile round out the system, which targets a wide range of black-and-white video teletransmission applications.

PhotoLink employs the same proprietary video-compression algorithm as the two-year-old Photophone desktop units. Compressing the images reduces storage requirements by a factor of 10 and reduces telephone costs. Users connect PhotoLink directly into standard telephone wall jacks and into a networking card in the expansion slot of a PC AT or compatible.

The digitized images can be stored on

the computer's hard disks or attached video-storage peripherals for display on Photophone screens. A typical Photophone image of 592×440 pixels (128 gray levels) requires about 20 Kbytes of disk storage.

The PhotoLink chassis holds up to five telephone-line interface cards, and the PC must have a PhotoLink network card and communications software. Networking software and a picture-data-base program called PhotoFile—the first of a number of applications programs to run on top of PhotoLink's core software—complete the system.

SOFTWARE. Image Data is working with software companies to develop retrieval packages that classify, index, and sort the images.

Possible uses include nationwide real estate listings or conference calls by doctors reviewing medical images. Programmers can also create their own end-user applications packages using the software shell.

PhotoLink starter kits are now available for applications developers and will be retailed at the end of the year for $9,600. The kit includes the chassis, software, and computer- and phone-interface cards. Extra phone interfaces cost $1,800. A basic Photophone system costs $8,500.

–J. Robert Lineback

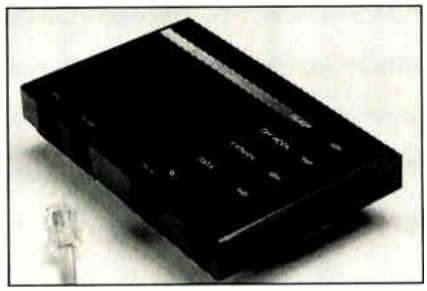
Image Data Corp., 7986 Mainland Dr., San Antonio, Texas 78250.
Phone (512) 680-2727 [Circle 441]

COMPACT 1,200-BAUD MODEM COSTS $119

Novation Inc.'s Parrot 1200 modem is about the size and weight of an audio cassette. The new 300-to-1,200-baud AT Hayes-compatible modem measures 4¼ by 2¾ by ⅝ in. and weighs 3 oz. Its suggested retail price of $119 is about one-fifth the cost of the Hayes Smartmodem 1200.

A microprocessor-controlled power-management system enables the Parrot 1200 to function reliably using only the power available from the host computer's RS-232-C serial interface. Neither batteries nor external ac power are required. It is available now.

Novation Inc., 21345 Lassen St., Chatsworth, Calif. 91311.
Phone (818) 998-5060 [Circle 446]



ENCRYPTION KEYS LAN SECURITY

A data security system for local-area networks and telephone-line transmissions encrypts data by using a 16-bit key and a scrambling algorithm that complies with the National Bureau of Standards encryption standard.

Intelicom Corp.'s Microcipher handles the problems normally created by passing encrypted data through computer systems with a Safe-Talk mode, which

guards against unwanted control characters that the computer would recognize and act upon.

The system is installed between the user terminal and modem via an RS-232-C serial interface. It self-checks its operational functions each time it is powered up. An automatic key-distribution function eliminates the security problems inherent in sending keys through the mail.

Available now, Microcipher costs $399.

Intelicom Corp., 9259 Eton Ave., Chatsworth, Calif. 91311.
Phone (818) 882-3745 [Circle 447]

TWO-CHIP MODEM SET INCLUDES CONTROLLER

A 2,400-baud modem chip set from Sierra Semiconductor Corp. minimizes chip counts for designers by integrating all modem functions—including a microcontroller—on two chips.

Sierra's solution lets designers use a modem chip—the SC11006—to implement all modem functions except the adaptive equalizer, and then to choose either of two controller chips—the SC11009 or SC11010—for control and adaptive equalization.

The SC11009 is used with parallel-bus applications such as IBM Corp.'s PC AT; the SC11010 is for serial applications.

The modem chip handles dual-tone multifrequency generation, call-progress monitoring, and remote loop-back diagnostics, and it has a programmable audio output port. Its transmission sections include a scrambler, a data encoder, a pulse sharpener, and a quadrature modulator. The receiver sections include low- and high-band filters, a Hilbert transformer, and an 8-bit analog-to-digital converter.

Available in June, samples of the SC11006 cost $49 each, and samples of the controllers cost $40 each.

Sierra Semiconductor Corp., 2075 N. Capitol Ave., San Jose, Calif. 95132.
Phone (408) 263-9300 [Circle 445]

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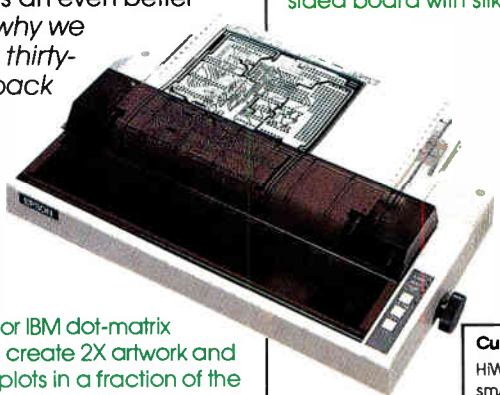

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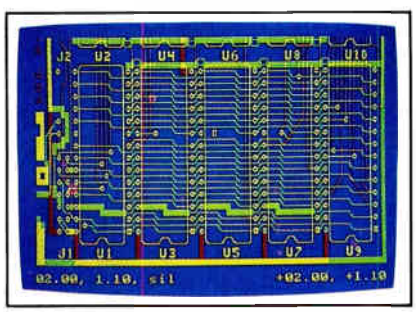

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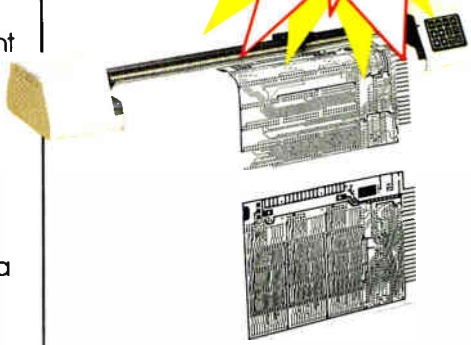

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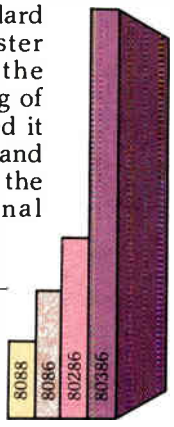

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SONY'S 2-IN. FLOPPY PACKS NEARLY A MEGABYTE

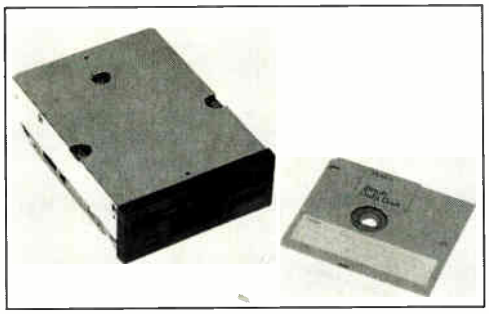
AIMED AT LAPTOP COMPUTERS, ITS 7-OZ DRIVE TRANSFERS DATA AT 14.3 MBITS/S

The trend toward small memory devices with top-drawer performance has taken a quantum leap in Sony Corp.'s 2-in. flexible magnetic disk and companion drive system, which together reach a blazing 14.3-Mbit/s data-transfer rate and pack 0.819 Mbytes of formatted information on a single side.

Sony's PDM-1 data disk is dimensionally identical with designs standardized by 43 companies for electronic still cameras. More important to the computer and communications industries, it conforms to the standard data-disk format that the same companies promulgated in 1986 and is suitable for a wide range of storage applications, including laptop computers.

MORE CLEARANCE. The system owes its speed in part to more internal clearance between disk and liners than larger-format disks. This means the disk can be rotated at 3,600 rpm for shorter latency time and higher data rate.

Engineers achieved the 0.819-Mbyte capacity (1-Mbyte unformatted) with high-density tracks and a 1,300-Oersted metal-powder recording medium. By comparison, 1-Mbyte 3½-in. disks use a 625-Oersted medium.



COMPACT. Sony's new 2-in. disk drive weighs 7 oz and is 2.6 in. wide, 1 in. high, and 3.8 in. deep.

The disk's 50 tracks are packed at 254 tracks/in. and reach a maximum recording density of 51.2 Kbits/in. along the innermost track. These specifications almost double the 135 tracks/in. of the 3½-in. disk and more than triple the disk's 16.5 Kbits/in. density.

Each track has four 4,096-byte physical sectors, which can be used as 256-, 512-, or 4,096-logical-byte sectors. Data in the sectors is broken up into 44-byte frames, each of which consists of a 4-byte header, 32 bytes of information, and two 4-byte blocks of redundancy code. These codes are used in a cross-interleaved, double-encoded Reed-Solomon code to provide error detection and correction of both random and burst errors. Error-free reading is possible, even if the error rate falls to 10^{-3}.

The disks weigh 8.7 g and incorporate a sophisticated error-correction code similar to that used on digital audio compact disks, to protect against loss of data from accidental damage. Copy protection is provided.

NEW DRIVE. Sony's companion PDD-100 2-in. drive weighs about 7 oz and is 2.6 in. wide, 1 in. high, and 3.8 in. deep. The drive's CXD-1103AQ controller chip is implemented with 10,000 gates in 2-μm CMOS technology to hold power consumption at a low 1 W during read or write. Besides its use in laptops, the drive is well suited for electronic musical instruments, synthesizers, facsimile terminals, and multifunctional telephones.

Sample price for the PDM-1 data disks in Japan is $7.50 each. The PDD-100 drive and CXD-1103AQ controller chip together cost $271.43. Sample quantities will be available in Japan in June.

–Charles L. Cohen

Sony Corp., Components Marketing Group, Data Transfer and Image Devices Department, 4-10-18 Takanawa, Minato-ku, Tokyo 108, Japan.
Phone 81-3-448-3217 [Circle 340]

GIVING IBM'S PS/2 A 1,280-BY-960 DISPLAY

Moniterm Corp.'s graphics-controller board links its 19-in. high-resolution monochrome monitor to IBM Corp.'s Personal System/2 computers, to deliver high-performance graphics while maintaining compatibility with IBM's new 640-by-480 video-graphics-array standard.

The Viking 2 controller implements 1,280-by-960-pixel resolution in a flicker-free, noninterlaced display on the Personal System/2 Models 50, 60, and 80. It combines VGA compatibility with much higher resolution than the VGA standard by performing a 4-to-1 pixel replication while refreshing the image at a rate of 66 Hz.

HIGH END. A new controller gives the Viking 19-in. monitor 1,280-by-960 resolution.

Moniterm claims it is the first third-party company to have a graphics controller board linking Personal System/2 systems to high-resolution monitors.

SMALLER SLOT. The board has 2 Mbits of video memory, but its key technology is a set of three CMOS 1,800-gate-array chips designed to accommodate the smaller slot size—the Personal System/2 boards are about 40% smaller than PC AT boards—and a power-consumption restriction of 1.6 A per connector in the Personal System/2.

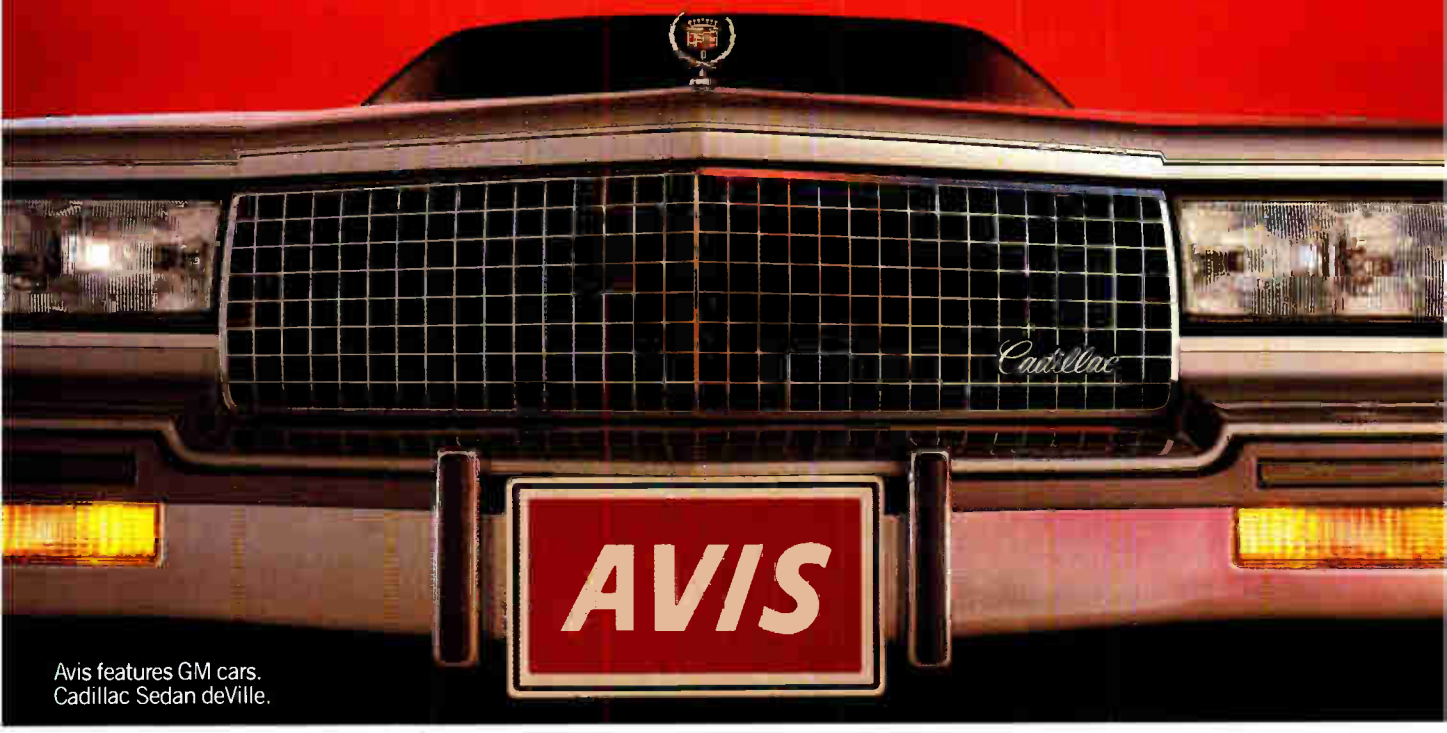
"We're taking our earlier controller board (for IBM's PC family) and interfacing it to a Micro Channel for all intents and purposes," says Henry Neils, Moniterm's marketing director. The three gate-array chips will replace about 50 of the 88 chips on the original PC graphics board, he says.

Shipments are scheduled for September. Moniterm credits its prompt entry into the Personal System/2 market to early access to specifications on IBM's Micro Channel architecture.

Despite the general unavailability of technical information for the new IBM machines, Neils says the Minnetonka, Minn., company was given the specifications within a week after the Personal System/2 announcement [*Electronics*, April 16, p. 46). "We feel we have a 45- to 60-day jump," says Ward Johnson, Moniterm president. "Other people are out there reverse-engineering the bus, and we're sitting here with marked-up documentation [from IBM]."

The Moniterm graphics board will measure about 2.9 by 11 in. and will fit into a 136-connector slot in the Personal System/2 motherboard, says Thomas C. Lohse, the company's vice president of engineering. The card features a 10-MHz version of Hitachi Semiconductor Inc.'s HD63484 advanced CRT controller

CADILLAC COMFORT AT A COZY PRICE.



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Circle 101 on reader service card

chip for high-speed graphics coprocessing. This version provides a 44% advantage over the 6.9-MHz clock speed of the Hitachi chip used on Moniterm's IBM PC, XT, and AT graphics card.

The new Moniterm offering is aimed at computer-aided design and manufacturing, desktop publishing, financial modeling, and other applications requiring high-resolution, large format, flicker-free viewing. Moniterm plans to offer the board separately or as part of a bundled package with the Viking 2 monochrome monitor.

OEM PRICES. Board pricing has not yet been set. The monitor/board package, however, will carry a suggested retail price of $2,395 and will be sold to original-equipment manufacturers for $1,413 in 100-unit quantities, Johnson says.

Moniterm is upgrading its current Viking 1 software drivers for the PC, XT, and AT to be compatible with the Personal System/2 and will provide the upgraded drivers with the new board. These include drivers for Microsoft Windows, GEM, Ventura Publisher, Lotus 1-2-3, AutoCAD, and VersaCAD.

–Wesley R. Iversen

Moniterm Corp., 5740 Green Circle Dr., Minnetonka, Minn. 55343.
Phone (612) 935-4151 [Circle 341]

ALTOS 386 MACHINE HANDLES 64 USERS

Altos Computer Systems has combined multitasking Unix-based software with one of the first multiuser computers based on Intel Corp.'s 80386 32-bit microprocessor. The result is a system that supports up to 64 users.

The San Jose, Calif., company has also beefed up memory and disk storage in its Series 2000 and incorporated several recent microprocessor-based enhancements, including built-in communications and peripheral interfaces and powerful software support.

THREE MODELS. The new series is available in three configurations. The model 2408S, accommodating 20 users, offers 4 Mbytes of random-access memory and a 65-Mbyte (formatted) Enhanced Small Disk Interface drive. The model 2417M handles 64 users and has 4 Mbytes of RAM, a 142-Mbyte hard disk, and a multidrop cabling-and-transmission system that connects up to 128 serial devices on RS-422 cabling. The model 2817M is similiar to the 2417M but has 8 Mbytes of RAM.

Altos also provides IBM Corp. 3270 and 3780 connections, CCITT X.25 and asynchronous network links, the Small Computer Systems Interface for intelligent peripheral control, and the compa-

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ny's own Worknet local-area network. Altos says it will develop an Ethernet/TCP/IP interface by the fourth quarter of this year.

Software includes an integrated office-automation package, word processing, spreadsheets, graphics, and data bases. The operating system is an enhanced version of Microsoft's Xenix System V, comparable to AT&T's Unix Sys-

The Series 2000 offers built-in links to several networking schemes

tem V.2 and conforming with AT&T's System V Interface Definition.

Although the Series 2000 more than doubles memory and offers two to three times the performance of the company's previous top-of-the-line, 30-user, 80286-based Model 3086, it will actually cost less than similarly configured 286-based equipment, says product marketing vice president Jeff Bork.

The Series 2000 is fully compatible with older system software, and hardware upgrades will cost from $5,000 to $9,000, Bork says.

Altos describes the System 2000 as a departmental or branch computer for original-equipment manufacturers and value-added resellers.

Exact prices are not available because Altos has recently adopted a policy of quoting each sale separately, but the general range is from $25,000 to $30,000. They are available now.

Altos Computer Systems, 2641 Orchard Pkwy., San Jose, Calif. 95134.
Phone (408) 946-6700 [Circle 342]

HARDCARD GIVES IBM PS/2 40 MBYTES

Plus Development Corp.'s new memory-expansion hard-disk board for IBM Corp. Personal Computers and compatibles offers 40-Mbyte capacity—double its predecessor, the Hardcard 20—and plugs into a single expansion slot. It is also compatible with the IBM Personal System/2.

The Hardcard 40's memory resides in two 3½-in. thin-film disks. A rotary-coil actuator provides average seek times of 35 ms. The product can withstand a 100-G shock and has a mean-time-between-failure rating of 40,000 hours. It comes with software that allows users to alter the standard configuration of two 21-Mbyte volumes. Both the size and number of volumes can be changed.

Available now, the Hardcard 40 costs $1,195 in single-unit purchases.

Plus Development Corp., 1778 McCarthy Blvd., Milpitas, Calif. 95035.
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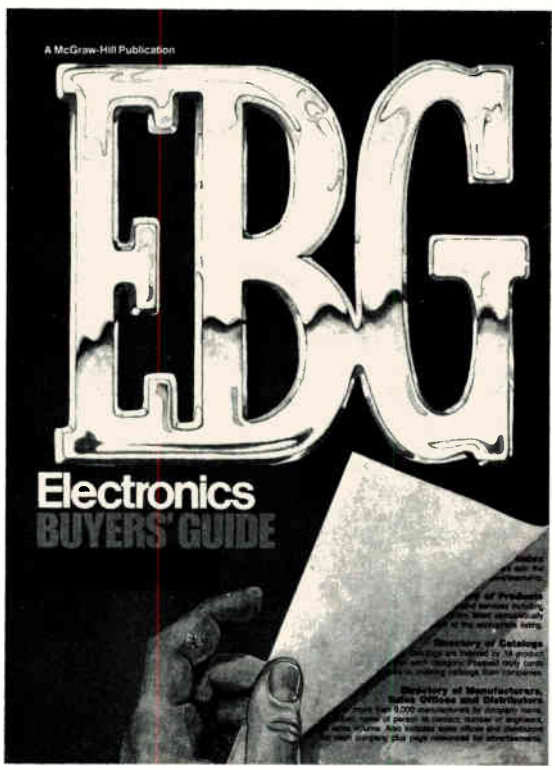

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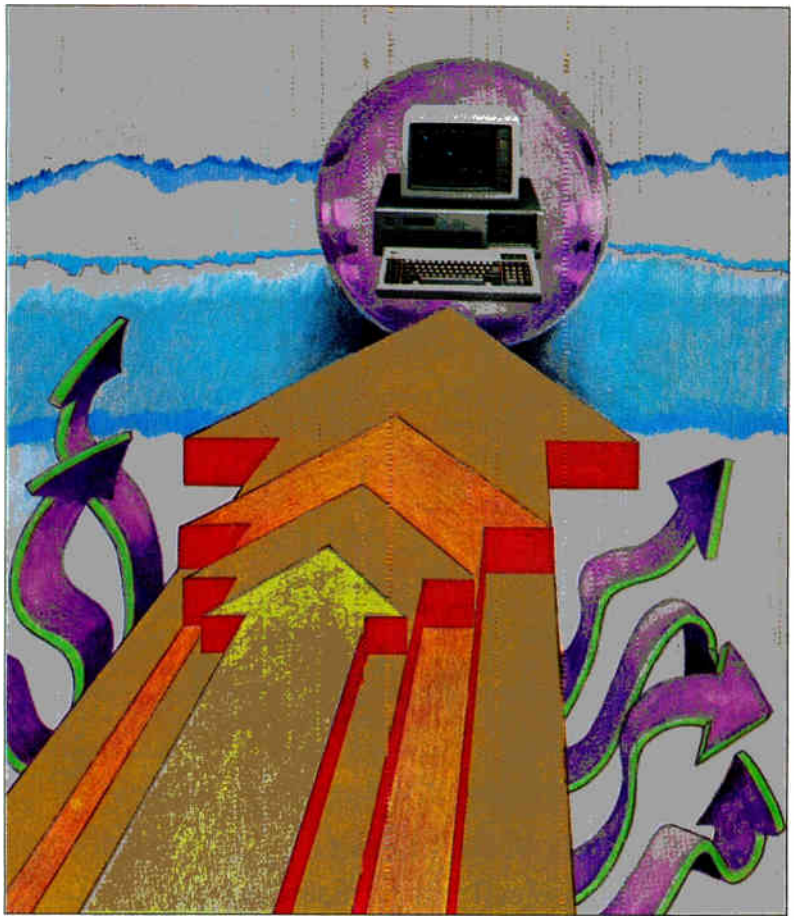

Windowing systems such as X Windows allow users to work with multiple applications simultaneously and to move files and data back and forth among them.

Vendors push MIT's standard, promising support and products.

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Excerpted from an exclusive article in the January 22, 1987 issue.

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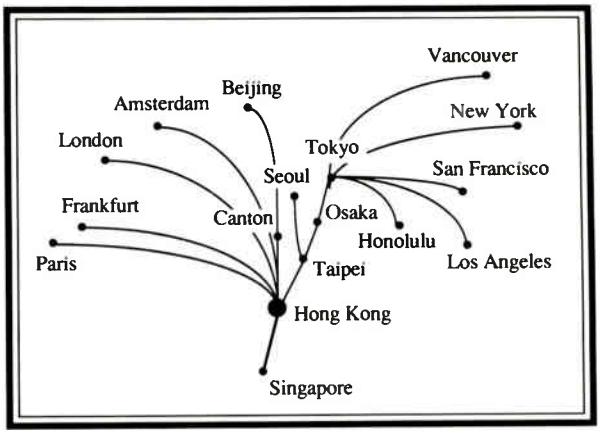

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ELECTRONICS WEEK

DEC WANTS MAP BOTH WAYS...

While vowing continued support for the Manufacturing Automation Protocol, Digital Equipment Corp. is raising hackles in the MAP community by continuing to insist that the IEEE 802.3 standard, on which the DEC-backed Ethernet scheme is based, should be made a part of the MAP factory networking specification. The current specification, which ties MAP to the IEEE 802.4 token-passing standard, is "like requiring that the only way to get to Pittsburgh is by bus," declared DEC vice president William R. Johnson in a keynote address before the MAP/TOP (Technical Office Protocol) Users Group meeting in Pittsburgh in May.

...BUT SOME RESIST DOUBLE STANDARD

Johnson's remarks in Pittsburgh prompted Michael Kaminski, head of MAP activities at General Motors Corp., to respond that "GM still believes that 802.4 is the proper media technology for use in manufacturing." Kaminski did allow that the auto giant will agree to user-community testing of the carrier-sense multiple access/collision detection-based 802.3 approach for possible MAP inclusion. But DEC's two-standard position drew fire from many MAP vendors and users in Pittsburgh for confusing the issue in an already sluggish MAP market.

FLUORIDE OPTICAL FIBER IS IMPROVED

GTE Laboratories Inc. has developed a process that increases tenfold the purity of zirconium fluoride, the key ingredient in fluoride optical fiber. Fluoride optical fiber can transmit light 20 times farther than silicon-based fiber, reducing the number of repeaters needed in long-distance applications. The company uses a single-cycle chemical-vapor process to achieve a purity level of 99.99999%. Several more hurdles exist, though, before a high-purity commercial fluoride fiber is available. The Waltham, Mass., company is now working on purifying other ingredients of fluoride glass. "No one is going to throw away their silicon fiber tomorrow, but this looks promising," says Richard Klein, manager of optical technology at GTE Laboratories.

SIMTEK GETS JAPANESE BACKING

Simtek Corp., an EEPROM startup formed by two former Inmos Corp. executives in Colorado Springs [*Electronics*, Sept. 4, 1986, p. 168], is getting an undisclosed sum of initial equity capital from the world's largest steel maker, Japan's Nippon Steel Corp., which now owns 20% of Simtek. Simtek plans to enter the market with an ultra-large-scale-integrated nonvolatile memory. The company will use EEPROM cells to make a range of customer-configurable circuits that can be mass-produced. Simtek will likely select a U.S. plant site in three months, have a manufacturing staff ready for production in 12 to 18 months, and employ 500 to 1,000 workers within three to five years.

INTERGRAPH HOOKS INTO VAX BUS

Intergraph Corp., Huntsville, Ala., can now interface specialized hardware to the 13.3-Mbyte/s VAXBI bus, the main input/output bus of Digital Equipment Corp.'s VAX 8000 series computers, under a recent license agreement. Extending an ongoing relationship, the Marlboro, Mass., computer maker has given Intergraph the green light to link its work stations to the VAXBI bus via the Alabama company's own communications processor, and to connect the Interbus File Processor, a high-speed data scanning device, to the bus. Both of the add-ons offload the central processor and provide better multiuser and multitasking performance in a graphics environment.

ADVANTEST TO ASSEMBLE IN U.S.

Advantest Corp., Tokyo, a leading IC test-system manufacturer, will begin assembling its VLSI test systems in July at its U.S. subsidiary, Advantest America Inc., in Chicago. The Japanese company sold 26 billion yen worth of IC test systems in fiscal year 1986, ended March 31, 1987, and about 25% of those sales were to the U.S. market.

HP TO MAKE AND USE WEITEK CHIPS

Hewlett-Packard Co. will not only manufacture chips for Weitek Corp., which has no fabrication facilities of its own, but will also incorporate the Weitek 2264/65 floating-point chip set in its new Precision Architecture series of reduced-instruction-set computers—thereby giving tacit support to the theory that RISC processors don't perform floating-point operations very well. The Weitek chip set executes at 40 megaflops and has enjoyed wide success in the industry. In addition to manufacturing to meet its own requirement, HP will supply packaged chips to Weitek, of Sunnyvale, Calif. The chips will be made in HP's 1.2-μm CMOS technology by its Corvallis, Ore., Circuit Technology Group.

SUN MOVING INTO FINANCIAL MARKET

Sun Microsystems Inc. in Mountain View, Calif., is moving aggressively into the financial services market, signing a deal to provide work stations for stock-market data and making a cooperative marketing agreement with a firm that makes fault-tolerant servers. The stock-market deal is with Quotron Systems Inc., Los Angeles, which will resell Sun-3 work stations to display and manipulate data from a number of market-information sources. Sun also linked up with Stratus Computer Inc., Marlboro, Mass., to market networked work stations and a fault-tolerant Stratus server. Sun, which sells mainly to engineers and scientists, expects to do $15 million in sales to financial markets this year.

BROADCASTERS PUSH FMX STEREO

The National Association of Broadcasters, Washington, D.C., has started up NAB Technologies Inc., a for-profit subsidiary whose first project will be to participate in the final development and marketing of the FMX stereo system [*Electronics*, April 16, 1987, p. 39]. FMX is circuitry that improves distant reception of FM stereo signals. NAB Technologies expects to become involved in other technology licensing agreements in the future.

FUJITSU TAKES ON INTEGRATED CAE

Fujitsu America is launching an Information Systems division in San Jose, Calif., with a lofty goal: to integrate all design and engineering functions into a set of software packages. The initial product, scheduled for release in the second quarter of this year, will be a PC-based civil and mechanical engineering package. Future products include computer-aided design and drafting, technical publishing, engineering data bases, and product simulation. Fujitsu's model of computer-aided manufacturing, which has streamlined the operations of many of Japan's largest companies, is the takeoff point for what the company dubs "computer-integrated engineering."

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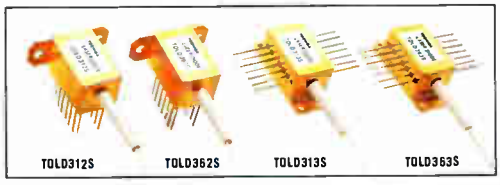

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