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Electronics

A NEW TOOL DRAMATICALLY CUTS VLSI DEBUGGING TIME

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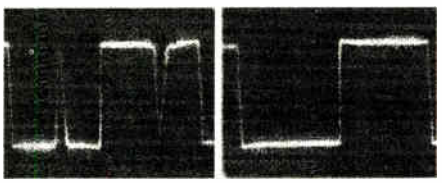

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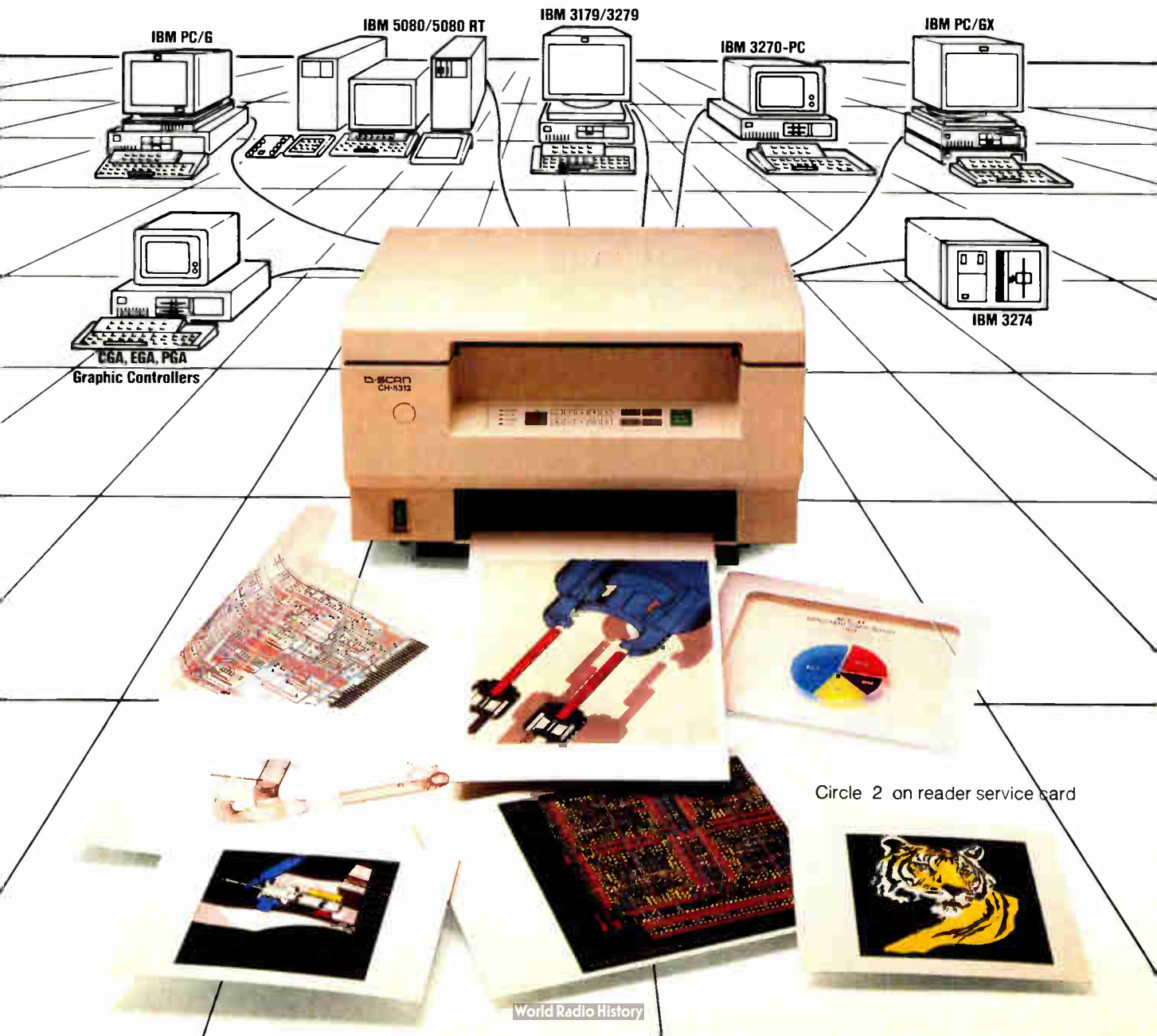

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If you want to get a fix on just how times have changed in the electronics industry, think back to a decade ago and try to remember how many articles about software appeared in any issue of *Electronics*. The answer is: not very many.

Now take a look at the contents page of this issue. There are no less than three Technologies to Watch and a Special Report based on software developments that will greatly improve the design and testing of integrated circuits. They bear out that adage about the industry: the only constant is change, particularly when it comes to software taking over jobs once performed by hand. The times are truly changing—and no magazine is doing a better job of changing with them than *Electronics*.

McLEOD: Now the engineers can stick to engineering.

The four articles come from CAD/CAE editor Jonah McLeod. He observes that their common thread, and the dominating trend in the entire field of IC design, is that the mundane, clerical-type work now is handled by the work station.

"The software is taking over a lot of the routine functions that the designer of hardware used to have to do manually. Before, you had the designer working on Mylar plots of an IC with strips of rubylith to create masks—that is, to produce the chip. This work literally required months, and in some cases years for a complex chip," says Jonah.

"But the funny thing is that none of that stuff had anything to do with engineering; it was drafting. Now all of those jobs are done automatically, and the engineer can do engineering. He's back to doing the things that he really enjoys, the things that led him into engineering in the first place."

Then there's the other half of the chip-design story in which software has wrought such massive change: the test function. Says Jonah, "On the test side, the story is equally interesting. Say you produce a chip and it doesn't work. Back in the old days—which were really just a few years ago—it meant pulling out the paper versions of those good old Mylar plots and laboriously looking for points on the plot.

"I recall seeing it many times when I visited companies and was being taken through the design and test labs. There would be this poor engineer with a microscope tediously and laboriously staring at a chip that was perhaps 100 mils on a side, and behind him on the floor would be a 6-ft exploded view on paper of that chip.

"All he wanted to do was find a polygon in that morass to pinpoint the error," says Jonah. "But he was forced to spend hours and days bent over the chip and searching the paper plot looking for his clues.

"Then along came the Sentry machine [described in this issue's cover story]. Now all the designer has to do is tell the computer where he wants to probe on the chip, and the system does the rest."

Where is all this leading? In Jonah's view, "We're really just starting out in this area of design software. There's a lot more still to be done, which in my view makes it one of the most exciting frontiers in electronics."

Laurence Altman

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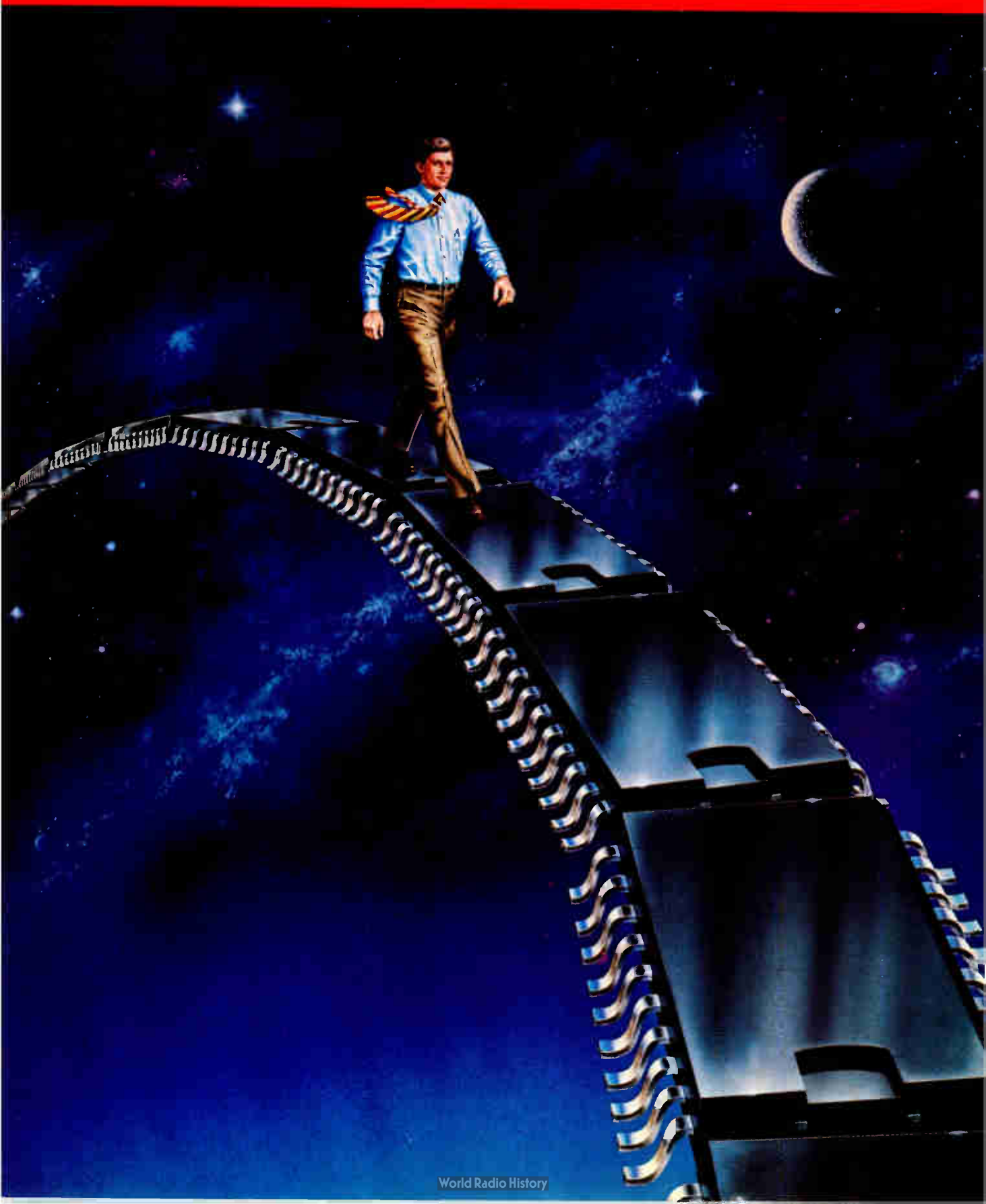

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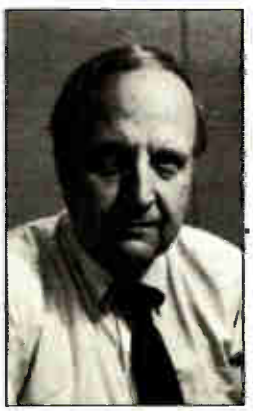
- Built-in op amps for excellent linearity.
- Op-amp buffered demodulated output.
- A pin which indicates lock detect.
- 2 phase comparators to choose from.
- Applications: FM Modulation/Demodulation, Frequency Synthesis, Frequency Multiplexing, Voltage to Frequency/Frequency to Voltage Conversion, Servo Control Systems, Data Synchronization, Manchester Coding/Decoding.

RCA

FYI

Americans usually don't have a good understanding of the way the Japanese do business; partly because of this, only 1 in 25 U.S.-Japanese negotiations ever succeeds



As the one-world electronics industry gets closer and making it depends on a company picking the right strategic alliance or partner, more and more U.S. managers will have to deal with their Japanese counterparts. Yet most Americans are often at a distinct disadvantage in negotiating such deals. While the Japanese have been "U.S.-watching" for decades, Americans usually don't have a good understanding of the Japanese way of doing business. In fact, Eugene L. Mendonsa, senior vice president at Red Bluff, Calif.'s, International & Domestic Negotiating Institute, estimates only 1 in 25 American-Japanese negotiations ever succeeds. Even though the Japanese may like a business proposition, they won't sign if they don't like the way the U.S. negotiator talks or behaves. Certain core values rule Japanese perception, thought, and behavior, Mendonsa says, and four key concepts form the foundation of their manners and ethics in business:

1. Amae (pronounced ah-my) means "indulgent love" and is most important. All relationships are based on it; concern for another pervades most Japanese relationships: one should do nothing to cause the other to lose face. This makes negotiating difficult for the Japanese, and a U.S. businessman should do everything he can to establish a personal, trusting relationship. Without Amae, the Japanese will not feel comfortable or "right" and will move more slowly than usual.

2. Shinyo (sheen-yoe) is "gut level" trust, a necessary faith that the other person won't cause any harm. The Japanese are hesitant to enter into any relationship without this trust. In the early stages of any negotiation, the U.S. executive should try to convey shinyo. The Japanese will be far more impressed by the good feeling than by sterling logic and data.

3. Enryo (in-ree-oh) is a feeling of distrust leading to interpersonal distancing. When the Japanese don't feel close to another person, they practice enryo to avoid conflict. Conveying a good feeling is all the more important for foreigners because the Japanese automatically practice enryo with them.

4. Giseisha (ghee-say-e-sha) means "victim syndrome;" the Japanese seem easily insulted. When they are thwarted from having their way, they take it as a personal insult and take revenge. Even an inadvertent insult can damage a long-term business relationship. And it can go beyond that. An insulted Japanese manager could even blacklist an American and make it difficult for him to do business in Japan. **ROBERT W. HENKEL**

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WHY DG's MILLER WENT TO MIPS COMPUTER

BOSTON

A senior vice president at Data General Corp. who also has 15 years of experience at IBM Corp. under his belt is the kind of quarry that computer-industry headhunters love to bag. Little wonder, then, that Robert C. Miller, who fits that description, had several "career opportunities" dangled before him during his six years at the Westboro, Mass., computer maker. But only one seemed worth taking—the chance to become president, chief executive officer, and chairman of MIPS Computer Systems Inc. of Sunnyvale, Calif.

"It's always been a dream of mine to run my own company," says the 43-year-old Miller. He headed Data General's Information Systems Group, which accounted for revenues of $1.2 billion in 1986, until he signed on with MIPS in mid-April. "To find one that played to my interests like MIPS is truly a rare opportunity."

MIPS, a private company formed in 1984, was the first firm to specialize in reduced-instruction-set-computer technology [*Electronics*, April 29, 1985, p. 36]. It remains as perhaps the only company dedicated to a pure RISC approach. Its product line includes commercial versions of a RISC chip originally developed at Stanford University, plus board-level products, a component kit, optimizing compilers, and a development system built around that chip.

The RISC technology was one reason Miller accepted the MIPS offer. The company's location, in Palo Alto, Calif., also played a role, as did the opportunity to head "a team that has real class." He also likes MIPS' use of Unix.

'DONE RIGHT.' Miller earned a master's degree in thermodynamics from Stanford, which is in Palo Alto. "When I left there 20 years ago, I promised myself I'd go back. And when the people at MIPS took me through the architecture of the RISC processor, I could see that these fellows had done it right. They've moved the state of the art quite a bit forward," he contends. "These fellows" include John Hennessey, who pioneered in RISC when he designed the experimental chip at Stanford that MIPS is now selling. He remains at MIPS as chief scientist and now heads a Stanford research project aimed at developing an advanced version of the chip for the Defense Advanced Research Projects Agency.

Miller declines to discuss that effort until he's more familiar with it, but he's quite vocal about Unix and RISC. He's convinced that RISC processors will be the dominant Unix platform for the 1990s. "Forecasts for the Unix market in the next decade are in the billions of dollars, and I believe this processor [and Unix] will be to the '90s what PC/DOS is to the '80s," Miller predicts.

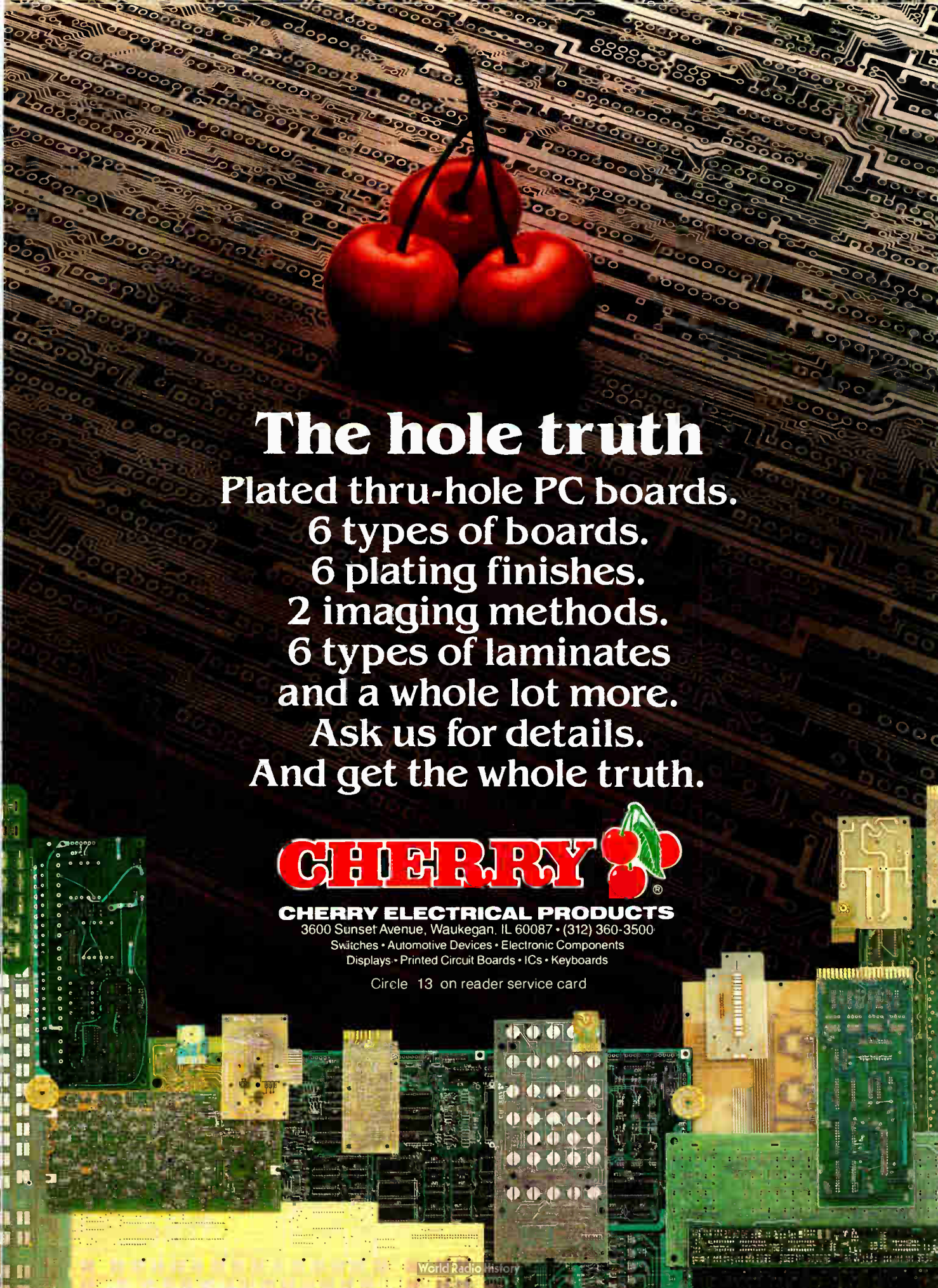
MILLER. MIPS gave him an opportunity he says he simply couldn't overlook.

"I was convinced a few years ago that Unix was going to be an exciting part of the business," he continues. "To think about a processor board that runs at 8 mips at no cost premium versus a 68020-based board is especially exciting. We'll need to keep driving the performance up to realize high-function work stations and servers."

For now, Miller sees MIPS' current CMOS as the most cost-effective implementation for RISC architectures. But he anticipates opportunities for emitter-coupled logic in applications where users will pay a premium for speed.

Miller is joining a company that acting chairman Donald Muller says is aimed at becoming the dominant supplier of RISC-based products. MIPS has backing from some of Silicon Valley's top venture firms, including the Mayfield Fund and Kleiner Perkins Caufield and Byers, San Francisco. The company has already sold Unix-based RISC platforms to several original-equipment manufacturers, including Prime Computer, Silicon Graphics Computer Systems, and Racal-Redac. All in all, Miller concludes, "I couldn't overlook this opportunity."

–Lawrence Curran



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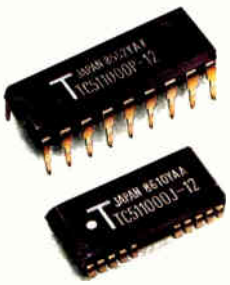

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TC511001 - 10	1 Mb x 1	CMOS	100 ns	Nibble	18 pin
TC511001 - 12	1 Mb x 1	CMOS	120 ns	Nibble	18 pin
TC511002 - 10	1 Mb x 1	CMOS	100 ns	Static Column	18 pin
TC511002 - 12	1 Mb x 1	CMOS	120 ns	Static Column	18 pin
TC514256 - 10	256K x 4	CMOS	100 ns	Fast Page	20 pin
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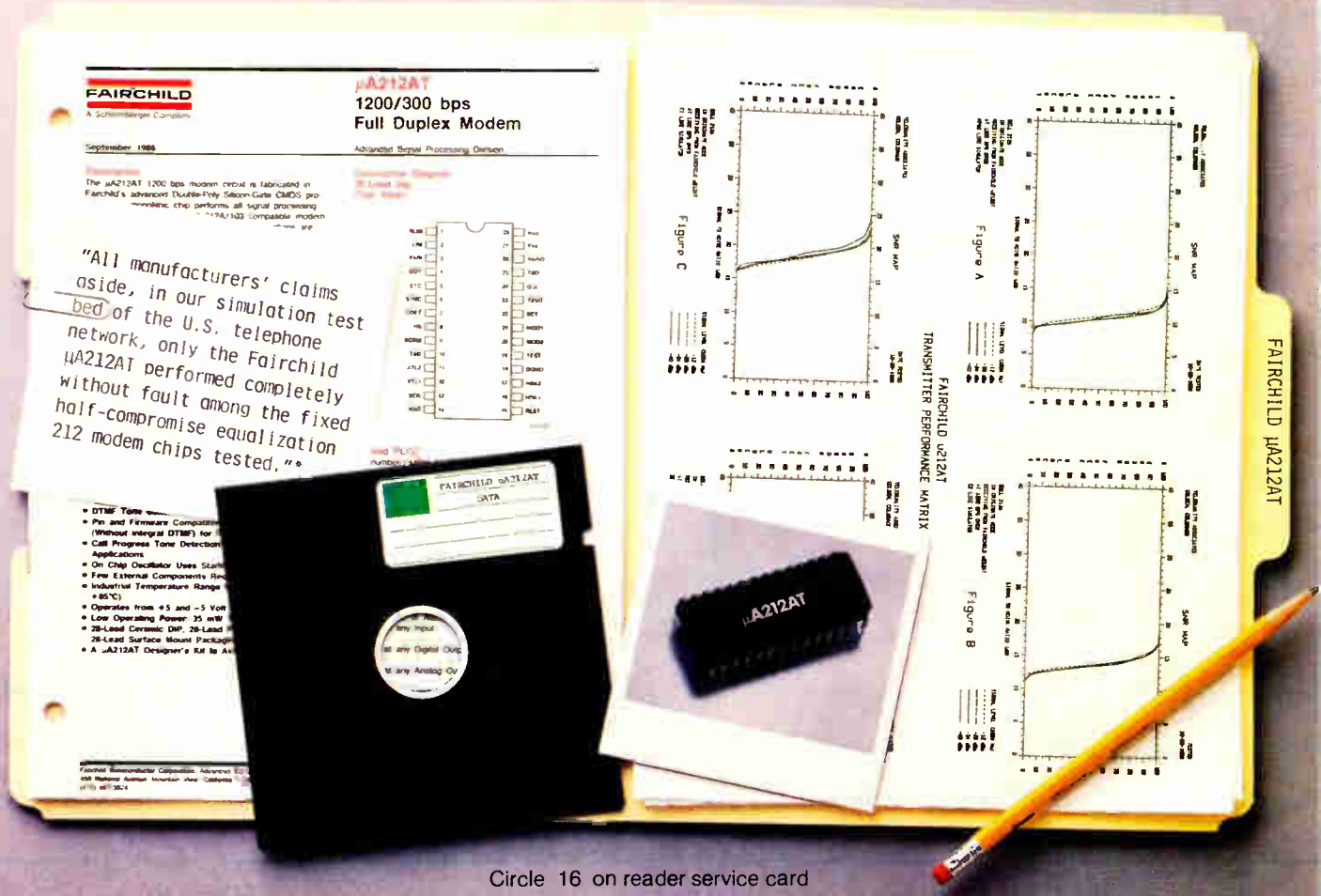

Circle 16 on reader service card

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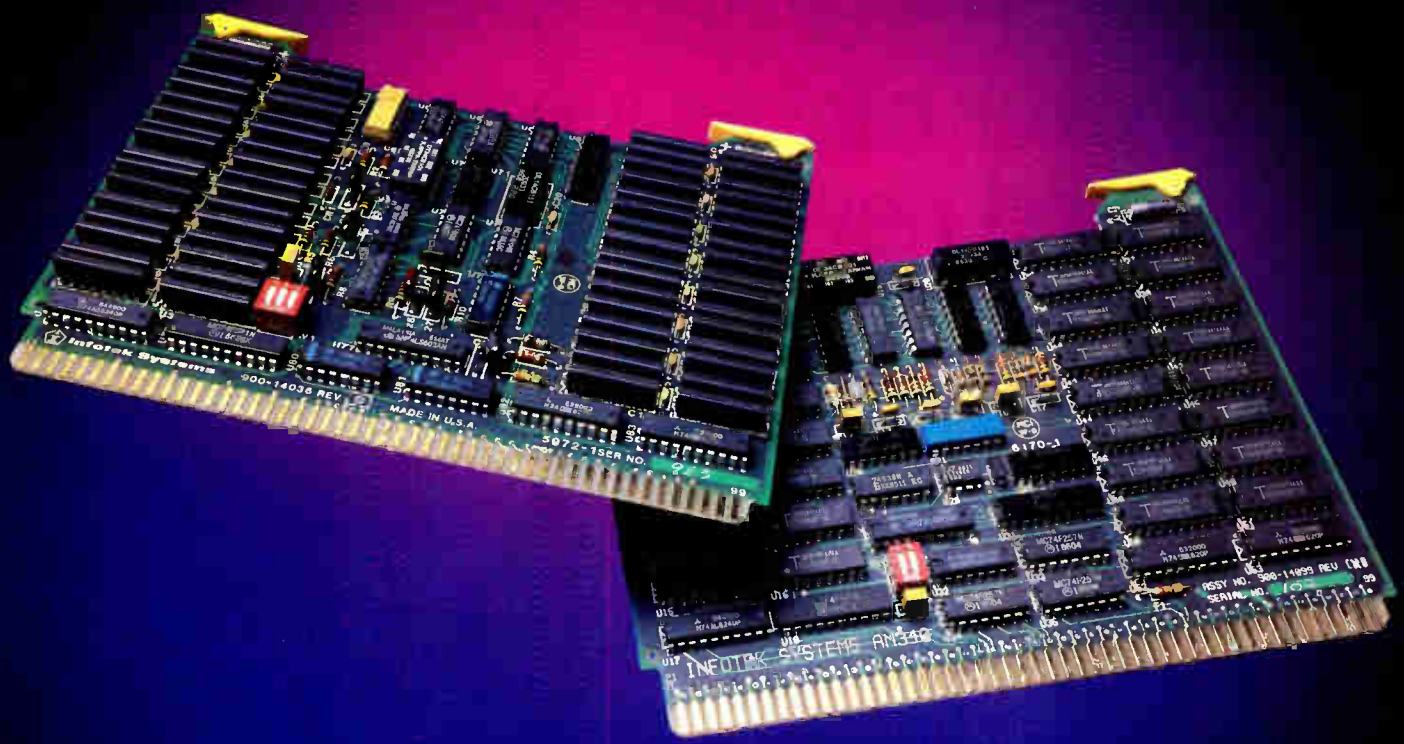

Now, get all the memory you need for the most complex programs—CAD, CAE—all on a single, compact card. And, at the same time, get the lowest cost per megabyte of memory on the market.

Infotek's new AM380 is the first 8 megabyte single-card memory available for HP 200/300 computers. It allows you to take advantage of the full storage capacity of your HP workstation without wasting valuable backplane space. ZIP packaging of 1 MByte monolithic DRAMs makes the low cost per byte possible.

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ELECTRONICS NEWSLETTER

TRADE-WAR FEARS AND COMPUTER-MARKET RECOVERY BOOST CHIP SALES

A burst of panicky buying spurred by fears of a trade war between the U. S. and Japan added a fillip to the chip business, but that's not the only reason behind the rise in March semiconductor bookings. Analysts say solid improvement in the computer market—as much as 9% growth—could lead to a double-digit rise for the semiconductor industry for 1987. The Reagan Administration imposed 100% punitive tariffs April 17 on some Japanese instruments, color TVs, and laptop computers, maintaining the Japanese had failed to live up to last summer's semiconductor trade accord. Industry insiders had worried that the move would prompt quick retaliation—and possible chip shortages—from Japan, but so far the Japanese have been slow to react. In the U. S., the strong yen and fears of price hikes for memory parts has fueled a chip-industry comeback, according to Integrated Circuit Engineering Corp., of Scottsdale, Ariz. With the Semiconductor Industry Association reporting March billings of $912.1 million and bookings of more than $1 billion, ICE now says its 1987 forecast for 9% growth might be on the low side, and Jack Beedle, the traditionally bearish analyst at In-Stat Corp., has boosted his 1987 sales estimates by about 6%, to 15%. □

GE/RCA IS ABOUT TO JUMP INTO DIGITAL SIGNAL PROCESSORS

Seeking to cash in on the rapidly expanding market for digital signal processors, the GE/RCA Solid State Division is making a late but significant entry. GE/RCA, of Somerville, N. J., has not previously marketed DSP chips, but the company hopes to make a splash this summer when it offers samples of a trio of commercial DSPs that will become part of GE/RCA's Advanced CMOS Logic family. Military versions will follow later this year, and the devices will also be added to the company's standard-cell library for application-specific integrated circuits. The new products include a 20-MHz programmable digital finite-impulse-response filter, a least-mean-square adaptive FIR filter, and a programmable-length first-in, first-out circuit. □

NATIONAL SLICES TURNAROUND TO TWO WEEKS FOR PROTOTYPE ROMs

National Semiconductor Corp. has found a way to program read-only memories after the final metallization layer has been deposited, cutting turnaround time for new designs to as little as two weeks for prototypes and four weeks for production parts. Normal turnaround time is generally three to four times longer. National found that implanting the chip with phosphorus ions at high energy could change the dopant of a buried layer to turn an enhancement device, which is always off, into a depletion device, which is always on. National has applied the process first to relatively slow devices, called stacked ROMs, in its high-volume COP 400 4-bit microcontroller line and may use it in high-speed ROMs or even programmable logic in the future. □

TELESOFT AND READY SYSTEMS WILL PRODUCE A RUN-TIME VERSION OF ADA

Seeking a way to produce a runtime version of Ada fast enough to operate in time-critical embedded avionics systems, Telesoft of San Diego is trying to mate its validated compiler with VRTX, a real-time operating system from Ready Systems of Palo Alto. The result should be a run-time Ada capable of context switching in as little as 125 μs, versus 600 to 900 μs for current Ada compilers. Avionics systems need fast context switching to check through a battery of sensors in a given cycle. Ready Systems expects to have an interim product out by midsummer, called AVX, that will provide an alternate tasking mechanism for Ada systems. □

ELECTRONICS NEWSLETTER

PHOTONICS' 5-FT GAS-DISCHARGE FLAT PANEL IS THE BIGGEST EVER

The largest-ever gas-discharge dot-matrix flat-panel display, measuring 59 in. diagonally, will be shown for the first time at the Society of Information Display conference in New Orleans in May. The ac display developed by Photonics Technology Inc., Northwood, Ohio, and Magnavox Electronics Systems Co., Fort Wayne, Ind., features 2,048-by-2,048-pixel monochrome resolution. It packs more than 4 million pixels into a 12.5-ft² viewing area. Photonics has shipped six of the 4-in.-thick, wall-size units, which have a refresh rate of 30 frames/s, to military contractors for command and control applications. Complete with a power supply, electromagnetic interference protection, software, and 68020-based electronics, a military version sells for about $400,000; the commercial version costs about $200,000. □

BELL LABS BUILDS WORLD'S FASTEST LASER

AT&T Co.'s Bell Laboratories has set a new standard for the world's fastest laser, shattering a record thought to be unbreakable just six months ago. Bell Lab researchers have built a device capable of emitting pulses every 6 fs, 25% faster than the previous high, and they are already using the laser experimentally. Chuck Shank, director of AT&T's Electronics Research Laboratory in Holmdel, N. J., says he once believed 8 fs was the technological limit, because the two optical gradings the laser relied on distorted results at higher repetition rates. But by bringing a pair of prisms into the picture, researchers in his group discovered that they could counteract the distortion by distorting the signal in an equal, but opposite, manner. The laser "gives us the ability to track an electron through a solid [object], step by step," Shank says. "We're witnessing the fundamental processes of how carriers act inside a material." □

NOW PCs CAN ACT AS WORK STATIONS ON SUPERCOMPUTER NETWORKS

Linking popular personal computers to a supercomputer is becoming a lot easier, thanks to software packages developed at the National Center for Supercomputing Applications at the University of Illinois. The center is distributing a communications package called NCSA Telnet, which allows an Apple Macintosh or an IBM PC to serve as a front-end work station to Cray X-MP or other scientific and engineering computers. Designed for the TCP/IP (for Transmission Control Protocol/Internet Protocol) environment used on Arpanet and the National Science Foundation's NSFnet, NCSA Telnet is the first package to allow multiple simultaneous communications between a Mac or PC and a Cray XM/P on a network. Both versions include VT 100 emulation for file editing, and the Mac version incorporates Tektronix 4010 terminal emulation for line-drawing graphics. □

DG BLAMES $9.6 MILLION OPERATING LOSS ON AGING 16-BIT COMPUTER LINE

Data General Corp. posted a $42.6 million loss, including an operating loss of $9.6 million, for its second quarter, which ended March 28, and DG president Edson de Castro is blaming the poor showing on "the rapid deterioration in sales of our older 16-bit product line." Sales of the company's MV line of 32-bit computers are increasing, but not enough to make up the difference. "We don't know when revenues will improve," a spokesman says. "We can't predict the rest of the year." The total quarterly loss was augmented by a one-time charge of $18.2 million the Westboro, Mass., company took for the early redemption of $150 million worth of debentures due in 2015, and a $14.8 million write-down from readjustments in market value for an unconsolidated affilliate, Dama Telecommunications Corp. of Rockville, Md. □

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Model	FFT* 1024 Point Real	FFT* 1024 Point Complex	FFT* 256x256 Image	Software	Price
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DT2811	✔	✔	12-bit	20kHz	✔	$199-$745

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Circle 24 on reader service card

PRODUCTS NEWSLETTER

TELEBIT DESIGNS A 2,400-BAUD MODEM FROM OFF-THE-SHELF PARTS

Telebit Corp., which threw a fastball at the dial-up modem market with its 18-Kbaud Trailblazer modem two years ago, is now following up with a curve: a design for a 2,400-baud modem that can be built from off-the-shelf, second-sourced parts. At the modem's heart is the Texas Instruments Inc. 320CM10 digital signal processor, programmed in read-only memory with basic modem functions from Telebit's Trailblazer architecture. The modem supports CCITT V.22bis, 2,400-baud transmission as well as Bell 212A and Bell 103 (1,200- and 300-baud) operation. The other two chips are an Intel Corp. 80C51 microcontroller with source code for mask programming and an Oki Semiconductor 6950B analog front end. Together the three chips cost about $27, says the Cupertino, Calif., company. The Telebit licensing fee is either a $200,000 one-time payment, which includes engineering support; or a $25,000 technology-transfer fee plus a $5/unit royalty. □

SMC CONTROLLER CUTS CHIP COUNT ON INTERFACE BOARDS FOR IBM MINIS

Chip counts on boards that link IBM Corp. System/3X minicomputers with terminals, peripherals, and networks can be reduced from as many as 100 to just 12 using Standard Microsystems Corp.'s single-chip controller to implement IBM's 5250 Standard. The COM52C50 is fabricated in 3-μm CMOS standard cells from the company's application-specific integrated-circuit library. All its high-speed-related functions are concentrated on-chip, so board designers can substitute a $2 chip for a high-speed input-output processor costing 10 times as much, says the Hauppauge, N. Y., company. Samples are available now. In 100-unit quantities, the device costs $19.50 in plastic dual in-line packages. □

SOFTWARE CUTS TEST-DEVELOPMENT TIME FOR PROCESSOR BOARDS BY 80%

A new high-level language, combined with utilities that automate fault-isolation programming, promises to trim the time it takes to develop test and trouble-shooting programs for typical microprocessor boards from the usual 20 to 30 man-weeks down to four to six man-weeks. The software comes with John Fluke Mfg. Co.'s new 9100 series of low-cost digital testers. The testers also handle functional testing up to 10 MHz and guided fault isolation up to 40 MHz. To reduce manual probing during fault isolation, up to 160 10-MHz lines can be employed with dual-in-line-package clips to stimulate and check circuit nodes automatically. Prices range from $21,500 for a stand-alone system with a programmer's work station to $9,000 for a test station, says the Everett, Wash., company. □

DEC BOOSTS SPEED AND RESOLUTION ON ITS VAX TERMINALS

Besides offering five times the speed and twice the resolution of older DEC terminals, the newest monochrome and color VAX terminals from Digital Equipment Corp. can manage and display two computing sessions simultaneously. What's more, they're priced substantially below their predecessors. The new text-and-graphics terminals are the monochrome VT330 and the full-color VT340. A proprietary VAX layered software utility, called SSU and priced at $200, allows dual sessions on a single wire with a VAX and an IBM Corp. mainframe, for example—a capability DEC claims is unique. The new terminals, which are completely compatible with all earlier DEC hardware and software, offer either six screens of text memory or two screens of graphics memory to offload the host computer. The VT330 sells for $1,895, which is $300 less than its predecessor, the VT240. At $2,795, the VT340 is $400 less than the older VT241. Both will be available in volume in May. □

PRODUCTS NEWSLETTER

PRIME SUPERMICRO RUNS UNIX AND MS-DOS SIMULTANEOUSLY

Prime Computer Inc. has tapped into the Unix environment with a supermicrocomputer that can run character-mode MS-DOS and Unix applications at the same time. The EXL 316 turns the trick with Merge 386, a software package from Locus Computing Corp., Santa Monica, Calif. Based on Intel Corp.'s 80386 microprocessor, the EXL 316 also has an Intel 80186 in its asynchronous controller, which means the 80386's 4 million-instructions-per-second performance at 16 MHz is degraded only slightly—to 3.2 mips—in executing Prime's implementation of AT&T Co.'s Unix V.3. With prices starting at $23,900, the EXL 316 is price-competitive with other multiuser supermicros, but none of them can run MS-DOS and Unix programs simultaneously, says the Natick, Mass., company. The EXL 316 will be available in June. Merge 386 software is separately priced at $1,800. Prime's other computers—with the exception of a recently introduced Unix-based graphics work station—use the company's Primos operating system. □

AMIABLE 100-Mbyte WINCHESTER FROM CONNER GETS ALONG WITH ANY PC

By interfacing a custom gate array with drive logic, Conner Peripherals has built a 100-Mbyte (formatted) 3½-in. Winchester disk drive that can be tailored to a specific host bus interface. The CP3100 normally uses the Small Computer Systems Interface and is fully compatible with the SCSI Common Command Set. It is also available with the IBM Corp. PC/AT interface, which means the AT needs no interface card. Other interfaces can be designed with the custom gate array. The San Jose, Calif., company's new drive is voice-coil actuated and employs 2,7 run-length-limited encoding. The half-height drive has a 25-ms access time and weighs 2 lb. Priced at $995 in OEM quantities ($1,595 for single units), evaluation units are available now. Volume shipments begin in the fourth quarter. □

CHOICES: $595 PER NODE FOR A NETBIOS 1-MBIT/S LAN...

Telegence Corp.'s Tokenstar 3301 plug-in card turns IBM Corp. Personal Computers or compatibles into networked work stations on Telegence's 1-Mbit/s Tokenstar local-area network using the IBM Netbios industry-standard interface. For $595 per node, users can chain together PCs with 3301s by interconnecting them with standard twisted-pair telephone cables with modular plugs. Or, they can plug the PCs into a Tokenstar network installed on a building's telephone wiring. The network transmits data over phone lines without interfering with voice calls [*Electronics*, Jan. 8, 1987, p. 31]. The 3301 boards are available now from the Westlake Village, Calif., company. □

...OR A NONSTANDARD COAXIAL NETWORK THAT'S 3.6 TIMES FASTER

A 3.6-Mbit/s local-area network called Grapevine connects IBM Corp. Personal Computers or compatibles for $595 per node—compared with $1,600 to $2,600 per node for competing systems that share 11- to 16-disk dedicated file servers. The LAN, from Computer Pathways Inc., eliminates file servers. Data resident in the PCs is shared instead by means of a proprietary real-time multitasking system. The total system—which consists of an adapter board, software, and coaxial cable—provides extensive user functions for electronic mailboxes, peripheral assignments, and file transfers. Although up to 50 PCs can be linked with the system, the Bothell, Wash., company says Grapevine is best suited for small, eight-member work groups—the majority of network users. Ethernet and IBM Token Ring gateways to larger systems can be purchased if needed. Grapevine's range is 4,000 ft using 14¢/ft RG-59 television coaxial cable. The product is available now. □

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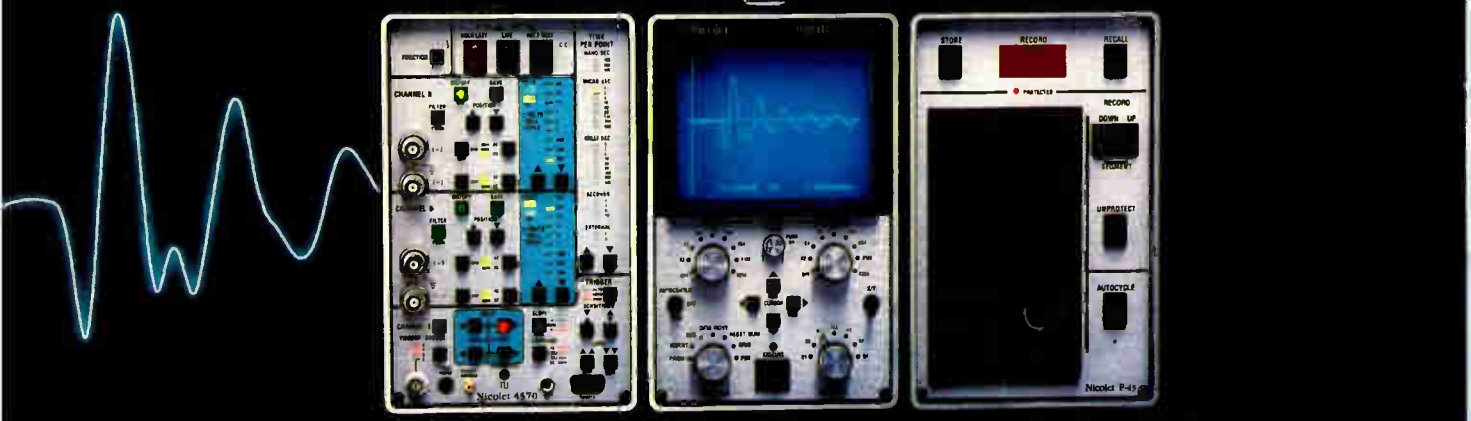

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Electronics

SRAM MAKERS CROWD INTO THE CACHE-TAG MEMORY NICHE

THE BIG QUESTION: CHIP SETS OR ONE-CHIP SOLUTIONS?

DALLAS

The cache-tag chip race has suddenly picked up speed. With nearly 20 manufacturers competing hard in static random-access-memories, most of them are looking for profitable niches. Right now, cache-tag is the most popular one: at least 10 of them have chips or are planning them.

"Cache is just now coming into its own," says Robert Bailey of Texas Instruments Inc., which originated cache-tag integrated circuits in 1980. "With microprocessor speeds increasing, memory is becoming the major bottleneck," says Bailey, U. S. logic strategy manager for standard logic circuits at the Dallas company. That is the design problem TI set out to overcome when it combined a static memory array and the logic of a comparator in the first cache-tag circuit.

Now the company is launching a new series of 1-μm CMOS cache-tag chips (see p. 81) as part of a VLSI logic portfolio. Others are hot on TI's heels, with a significant portion of chip sales at stake: cache storage represents about a third of fast-SRAM shipments.

"We knew this thing was too good to last," says Bailey, reflecting on TI's fast-vanishing position as the sole producer of cache-tag ICs. TI must fend off not only the onslaught of new competitors, but also the advent of highly integrated cache controllers, which incorporate address-matching functions with tightly coupled interfaces to specific 32-bit microprocessors.

The cache-tag function acts as a self-initiating directory of what data is being held in SRAM-based cache storage. It automatically checks incoming addresses from host processors against the data copied in cache from slower dynamic random-access main memory. These specialized address-matching memories can boost system throughput by offloading overhead from a busy host.

Silicon integrators now must decide how much, and how quickly, cache circuitry should be squeezed onto a single IC. Products planned for later this year run the gamut of possibilities, as chip merchants anticipate cache's move into high-volume personal computers, thanks to 32-bit microprocessors that rev at more than 20 MHz.

The result is a strategic jumble. Solutions range from relatively simple cache-tag devices to chip sets and highly integrated cache controllers. Some companies favor what TI's Bailey terms "generic" chips, those not tightly tied to a microprocessor or system-bus architecture. Others are designing around Intel Corp.'s popular 32-bit 80386 microprocessor.

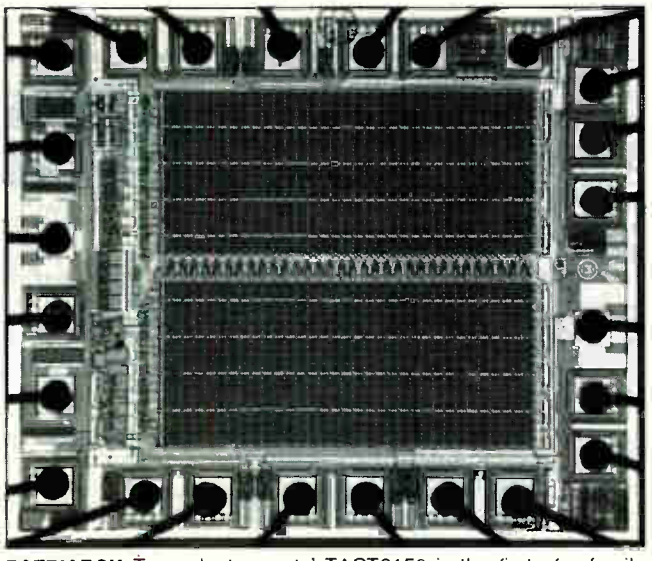
These diverse system-cache architectures are making it difficult for chip makers to clearly identify high-volume configurations, notes Curt Wyman, Motorola Inc.'s SRAM marketing manager. "We are expecting a shakeout in the features area, and standards will evolve," he says.

GETTING FASTER. So chip makers are hustling to get a leg up. For example, TI is redoing its widely used n-channel cache-tag design (512 by 9 bits) in 1-μm CMOS, speeding up the part to 20 ns from 35 ns. The result is the TACT2150, priced at $16.20 each in 10,000-piece orders. Bailey expects to see 15-ns speeds by year's end.

By June, TI will also offer samples of new 1-Kbit-by-12-bit and 2-Kbit-by-9-bit CMOS cache-tag chips. Like other companies, TI is planning system-specific cache controllers, and it is likely to place cache-tag functions into its 1-μm CMOS standard-cell library.

At Motorola in Austin, Texas, MOS-memory managers are planning a new line of cache-tag SRAMs by the beginning of next year, one matching the 22-pin MK41H68 4-Kbit-by-4-bit design introduced by Thomson Components-Mostek Corp. [*Electronics*, Jan. 22, 1987, p. 102]. Motorola's 24-pin design will contain a bit-set/bit-clear write feature that will allow individual bit manipulation without the need for a complete read-modify-write operation.

But other companies are not willing to wait patiently. They are hoping to get a head start, especially in playing off the popularity of the Intel 80386 processor. Intel itself plans to ship in the second half of the year a high-performance 32-bit cache controller tightly coupled to its microprocessor. The 132-pin 82385 contains not only the cache-tag function but a "posted write-through" feature that uses on-board buffers to make information immediately available to an 80386 system bus.



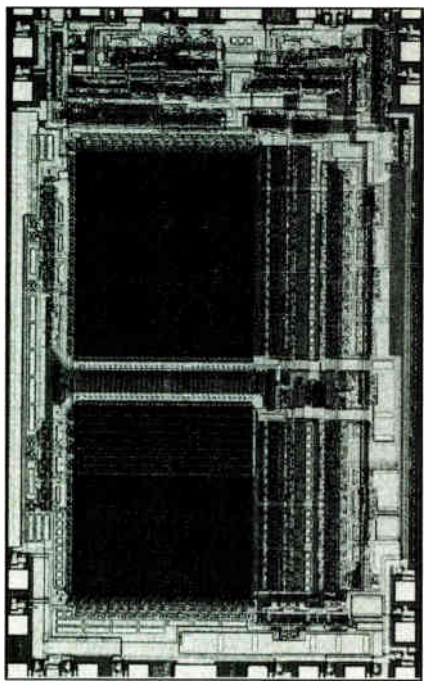
PATRIARCH. Texas Instruments' TACT2150 is the first of a family fabricated in its 1-μm CMOS technology.

Intel's plans have led Inmos Corp. to tightly couple the 80386 to a cache-storage chip set now in the works. "We were working on a cache chip set before Intel made its plans known," says Don Carrigan, director of memory marketing at Inmos, Colorado Springs. "Intel's move certainly influenced us in the area of whether or not to go generic, or [to design] one for the Motorola 68020 or the Intel 80386." Inmos plans to roll out early next year a 68-pin controller that will have an 8-bit-wide cache-tag function on-chip and support for a four-way associative organization.

The firm is also designing a cache-oriented data RAM that will have extra interface logic to

work quickly with the Inmos controller or others, such as the Intel chip. Carrigan expects the company's next step will be integration of data array onto the controller for a monolithic cache chip.

Cypress Semiconductor Corp. in San Jose, Calif., plans to support a number of microprocessor families and large cache configurations with a set to be introduced later this year. Dane Elliot, applications manager. believes the best approach to cache architectures will be "a building-block approach for a long time. The company that tries to get it down to one chip is going to lose flexibility."



TTL COMPETITOR. Advanced Micro Devices is entering the fray with its Am93469.

The wave of new cache-tag chips is not confined to the CMOS world. Advanced Micro Devices Inc. of Sunnyvale, Calif., plans to start volume deliveries of emitter-coupled-logic 512-by-9-bit cache-tag buffers in June. Robert Sykes, marketing manager for bipolar RAMs, says AMD's IMOX-III process will be used to make 20-ns parts with TTL-compatible input-ouput buffers, which he says is "the correct speed to be used for many of the 32-bit microprocessors and many new telecom networking applications." Two ECL-compatible parts—the Am10469 and 100469—will be even faster at 9.5 ns.

Meanwhile, the companies that already have cache-tag chips on the market are finding prices under siege. For example, Integrated Device Technology introduced in December the IDT7174 8-Kbit-by-8-bit cache tag at a price of $51.75 each in lots of 100. It's now selling for $25.80. Industry watchers expect pricing pressures to increase as the competition grows. *–J. Robert Lineback*

CAREERS

INFLATION CONTINUES TO CUT INTO EE PAY GAINS

NEW YORK

Engineering salaries have risen 280% since 1972, but the news isn't all that good. According to a new report on salaries and fringe benefits by the Institute of Electrical and Electronics Engineers, inflation has taken its toll. The $53,900 earned by the average IEEE member today is worth a scant 2% more than the $19,200 he was paid in 1972.

The 1987 IEEE Salary and Fringe Benefit Survey is the eighth edition of the study that the institute has been conducting every two years, except for a three-year break between the first two. The statistical data were analyzed by Number Crunchers Inc. of Takoma Park, Md. The numbers came from questionnaires that were returned by 12,669 engineers—roughly 8% of the IEEE's membership.

The report also sheds light on a number of other salary-related issues. The data show that women, minorities, and government employees earn significantly less than the typical IEEE member—a white male between age 30 and 49 employed in the private sector. Top-paid government engineers can expect at least 25% less than what they could earn in the private sector.

Self-employed engineers earn more than full-time salaried workers. And with the rise in double-income households, fewer people are taking advantage of health and other benefits available to them, probably because their spouse's employer offers a more attractive benefit program.

The report closely analyzes the factors that contribute to how much an engineer earns, including gender, education, experience, and the size company he works for. What it found, says Victoria Albright, vice president of Number Crunchers, is that women earn, on the average, $2,300 less than similarly qualified men doing the same job. It also found that whites—whether male or female—earn roughly $1,300 more than minorities with identical backgrounds, educations, or work histories, and that veterans of the armed forces earn almost $1,000 less than nonveterans. Government employees earn less than those working in industry by as much as $12,000.

THE RIGHT BOSS. The engineers making the most money are self-employed, Albright says. Their annual income can range up to $300,000, with the median income being $63,500. That's much higher than the $50,000 median for those in full-time jobs. But those figures can be misleading, because self-employed individuals must pay for their own benefits. Also, more than 70% of them claim that they work more than six hours of overtime a week—11% say they work 16 to 20 overtime hours weekly.

Regardless, Albright says many more engineers are likely to consider self-employment, especially as more and more companies offer lucrative incentives for early retirement. These engineers can then go out and cash in on their experience, Albright says, pointing out that there are now more than 3,500 "technically retired engineers who are working full time," and half of them are younger than 62. *–Tobias Naegele*

MANUFACTURING

CHEMICAL DEPOSITION GETS AN EXPLOSIVE NEW ENTRY

SANTA CLARA, CALIF.

Take a market that was worth $200 million last year, is expected to reach $560 million worldwide by 1991, and has no clear leader. Add a manufacturer that is determined to seize control with an innovative entry. The result could be explosive.

The market is the one for chemical-vapor-deposition equipment used to make integrated circuits. The manufacturer is Applied Materials Inc., whose vice president, James Bagley, predicts that the Santa Clara, Calif., company will grab the better part of that market with its Precision 5000 CVD system.

Bagley says that Applied Materials already has commitments to buy the $750,000 machine from 10 companies in the U. S., Japan, and Europe. What is causing the 5000's popularity is its ability to handle both low-temperature oxides and plasma nitride, something no other machine can do. These two applications, which dominate today's CVD market, should account for 60% of this business in five years.

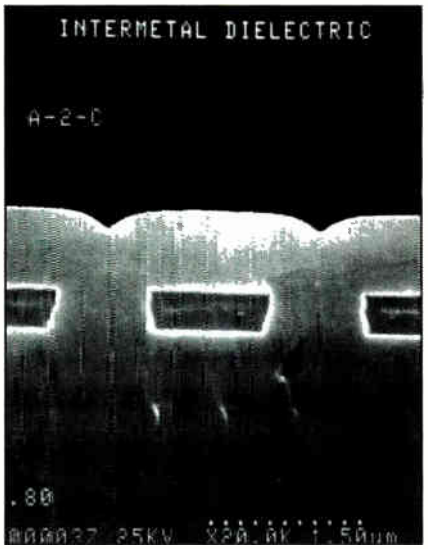
The new machine will be even more versatile next year. Bagley says the company is working on a modification

that will enable the system to do refactory CVD, which will account for another 25% of the market in 1991.

Also, the 5000 shines where conventional CVD systems fall short: in controlling particulates, uniformity, and conformality in such operations as passivation, doped interlevel dielectrics, and conformal films, says David Wang, the company's vice president of marketing and technology.

And he emphasizes that in the vital area of intermetal dielectrics, one of the cornerstones of the next generation of multimetal-level devices, today's vapor-deposition systems create a critical bottleneck with as many as seven steps spread over multiple machines. The 5000 unclogs the process and eliminates all the difficulties associated with low-temperature dielectrics and does it with an elegant single-wafer, multichamber approach. Particulates are taken care of by a self-cleaning system in each chamber.

The heart of the new CVD system is its loadlock chamber. There, a robot arm and storage elevator take incoming wafers from cassettes and route the wafers to two (expandable to four) completely independent process chambers where different steps may be completed without pumping down the loadlock chamber, a time-consuming operation. For example, two- or three-step jobs can be performed within the chambers: 1-μm spaces can be filled without leaving any voids, conformal film can be deposited without cusping, and topography and profile of the deposited film can be controlled with *in situ* etchback.



FILLED. The 5000 fills 1-μm spaces without voids, providing a favorable topography.

Extreme care is taken to minimize particulate generation. Every wafer is cleaned automatically by a plasma process in each chamber that takes about a minute. A loadlock protects the chambers from atmospheric contamination, while a surface-controlled reaction minimizes process-generated particles.

AUTOMATED. The system is completely automated, with all wafer-handling and control systems incorporated into a centralized mainframe. Push-button operator commands are limited to Go, Stop, Load, and Unload. Programming is done on a control screen with a light pen or directly from a host computer.

Another striking feature of the 5000, one that promises to increase productivity, is its self-cleaning capability. This should limit down time for maintenance to about 10%; present-day CVDs must be turned off for cleaning about 40% of the time. Also, Applied Materials has made a major effort to increase reliability by designing each module for a system mean time between failure of 500 hours.–*Jerry Lyman*

COMMUNICATIONS

JETLINERS TO GET SATELLITE ANTENNAS

LONDON

By early next year, the International Maritime Satellite Organization expects to be doing for planes flying over oceans what it has long been doing for ships sailing on them: offer satellite channels in the L and C bands for voice and data communications. And to make sure all the crucial technology will be there to get the service on the air, London-based Inmarsat has funneled some $3.2 million in development money to three antenna makers and an avionics-package supplier. The aim is to ensure that airlines will have antennas that will get the messages through without creating drag that will slow down the planes.

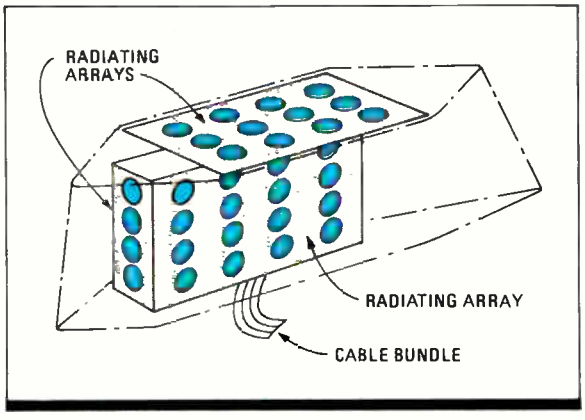
Inmarsat has two companies working on electronically steered phased-array antennas: Racal Antennas Ltd. of Southhampton, UK, and Ball Corp.'s Aerospace Systems Division in Boulder, Colo. And for anyone who wants a more shipshape solution with a mechanically steered platform, the agency is backing a development at E-Systems Inc., Greenville, Texas. Rockwell International's Commercial Electronics Division, Dallas, is developing the associated avionics gear.

Racal figures that a small fin atop the fuselage would be the slickest way to retrofit an antenna to an airliner. "It's the most flexible and reliable arrangement," maintains Derek Henderson, the firm's commercial director. "You don't need keyhole antennas to get coverage ahead and to the rear."

To achieve the required coverage, Racal puts five independent dipole arrays inside its fin, which measures 30 in. long, 8 in. wide, and 15 in. high (see figure). Gain over 85% of the coverage zone is 12 dB, and 9 dB for 95% coverage; there are no blind spots.

Racal plans to have prototypes on two British Airways Boeing 747s by the end of the year. For these two, part of an experimental transatlantic passenger telephone service that the airline will operate with British Telecom International, the receiving and transmitting antennas will be mounted in separate fins. The single-fin version will be installed aboard a third 747 in April 1988.

Foregoing fins, Ball packaged its 16-element antenna arrays into two curved panels mounted on opposite sides of the fuselage at a 45° elevation. The panels, only ¼ in. thick, measure 32 in. long by 16 in. wide. Driving the arrays are p-i-n diode phase shifters that are mounted just inside the aircraft skin to hold down transmission losses between the drivers and the dipoles themselves.



TAKE FIVE. Racal's satcom antenna for aircraft has five phased arrays tucked inside an aerodynamic fin.

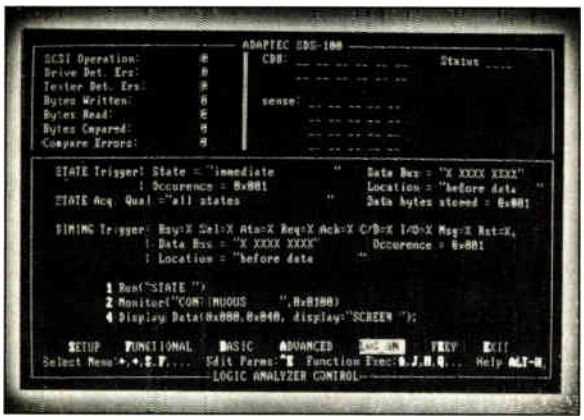
Ball successfully tested a prototype low-gain array in 1985 and expects to have its first high-gain antennas installed in a commercial airliner this year.

As for E-Systems, its engineers are convinced that mechanically steered antennas outperform electronically steered phase arrays. "We can get 13.5-dB gain over the full 360° range at elevation –30 to +90," says Donald E. Schrader, the firm's director of nonmilitary programs. "You can't get that with electronic steering," he maintains. –*Arthur L. Erikson*

NOW IT'S EASY TO DEBUG SCSI SYSTEMS

MILPITAS, CALIF.

Four out of five microcomputer and minicomputer manufacturers either use or plan to use the Small Computer System Interface, but until recently computer makers have had no easy way of determining whether host adapters, controllers, and peripherals are mutually compatible. Now Adaptec Inc. has come up with a way to make sure that intelligent peripherals conforming to the SCSI standard will operate reliably when they're all connected to a host.



SETUP. The Adaptec SDS-2's menu for setting up special logic-analysis tests through the SDS-100 tester.

SCSI enables a microprocessor to operate with low overhead by commanding intelligent peripherals to handle such operations as transferring and copying data files among themselves. However, system-design teams that have tried it with different types of peripherals have spent up to five man-years devising and running tests to verify that the peripherals can work reliably, says William A. Horton. director of the Milpitas, Calif., company's development systems operation. He is also a member of the American National Standards Institute committee ANSI X3.131 that is responsible for the standard.

SCSI PIONEER. Horton says the new Adaptec development system, the SDS-2, integrates design and test tools that the company initially developed for its own use. The company has been something of a SCSI pioneer. Two founders—Laurence B. Boucher, chairman and chief executive officer, and Bernard G. Nieman, systems vice president—headed development of the original SCSI design in 1979 at defunct Shugart Associates. Adaptec also helped launch the interface in 1981 by producing some of the first peripheral-control chips and boards, though it still gets most of its revenues ($51.5 million last year) from other products.

Although the interface has been standardized since then, a new system design needs from 1,000 to 10,000 trial runs because of the interface's flexibility and the way peripheral manufacturers have used the leeway, Horton says. For instance, some 90% of all disk-drive commands come from a common command set for random-access devices, but drive manufacturers can choose different command combinations, implement the standard commands differently, and add vendor-unique commands.

The SDS-2 automates those trial runs as it performs both the logic functions, called the initiator and target functions, that are needed to emulate the whole system. It follows the year-old SDS-1, Adaptec's first SCSI development system, which can perform only the initiator function. The functions handle transactions among host adapters and peripheral-control units. Moreover, says Horton, the SDS-2 "provides for hostile device emulation. Hostile 1's create parity errors once in a while, or move through bus phases in an unexpected order, or put out impossible but legal sequences. If you are emulating a target, for instance, you don't want to be a nice target—you want to try to mess up the host."

The system also automates debugging and verification tests and serves as a standardized interface system. With these capabilities, system designers can either develop and debug complete interface systems, or verify that off-the-shelf adapters, controllers, and peripherals are compatible with each other, as well as with the standard, Horton says.

Adaptec will also introduce on May 4 a low-cost test system and a logic analyzer that works with the SDS-2 as well as the SDS-1 or the SDS-100 tester. The systems, which operate at data rates to 1.8 megabytes per second, are based on the IBM Corp. PC/XT computer.

With the SDS-2, which costs $19,500 including the PC/XT, designers can start with a programmable adapter and a menu-driven library of more than 250 test functions. It has an interactive mode for initial debugging sessions and a programmatic mode for setting up lengthy, design-verification tests. "For instance, one of our verification tests runs all night, prints out results of each test, and ends with a pass/fail statement," Horton says. There are also two target-emulation modes, one in which the system designer controls test environments and another for testing whether the system can properly execute such commands as the standard SCSI copy command.

LOW-COST TESTER. Tests programmed with the SDS-2 can also be executed on the SDS-100, which also can be used as a low-cost, programmable tester for incoming inspection of peripherals and for other manufacturing and maintenance tests. Horton says a typical disk drive can be inspected with only four tests: write, read, and compare 1,000 data blocks; random write, read, and compare; arbitration test; and parity error-detection test.

The operator makes only one keystroke to start a test, and then the tester displays transactions and displays or prints results. The $5,500 price includes an adapter board and a software package, but not the PC AT. Also menu-driven. the package includes a library of more than 50 preprogrammed test functions. *–George Sideris*

LOOK OUT YANKS! HERE COME THE BRITISH

LONDON

The British are coming, and this time their objective is U. S. power-supply makers. One attacker is especially well-armed: the Dowty Group plc is one of the UK's largest suppliers of electronic systems. It is going after American companies on their home ground: the $1.84 billion U. S. power-supply market. On another front, tiny Pascall Electronics Ltd. wants to shove the Yanks out of a British niche they have long dominated: the $84 million defense power-supply market.

Dowty is an $800 million company, with almost half of its sales in the U. S. But it only recently entered the U. S. power-supply market, through a subsidiary, Dowty Power Supplies Vermont. Now it has combined its four European power-supply divisions and the Vermont operation to form a new company,

RETAIL GaAs.

The success of Vitesse's venture into off-the-shelf LSI GaAs parts depends in large part on its proprietary silicon-like fabrication process.

Vitesse goes commercial with GaAs LSI bit-slice family.

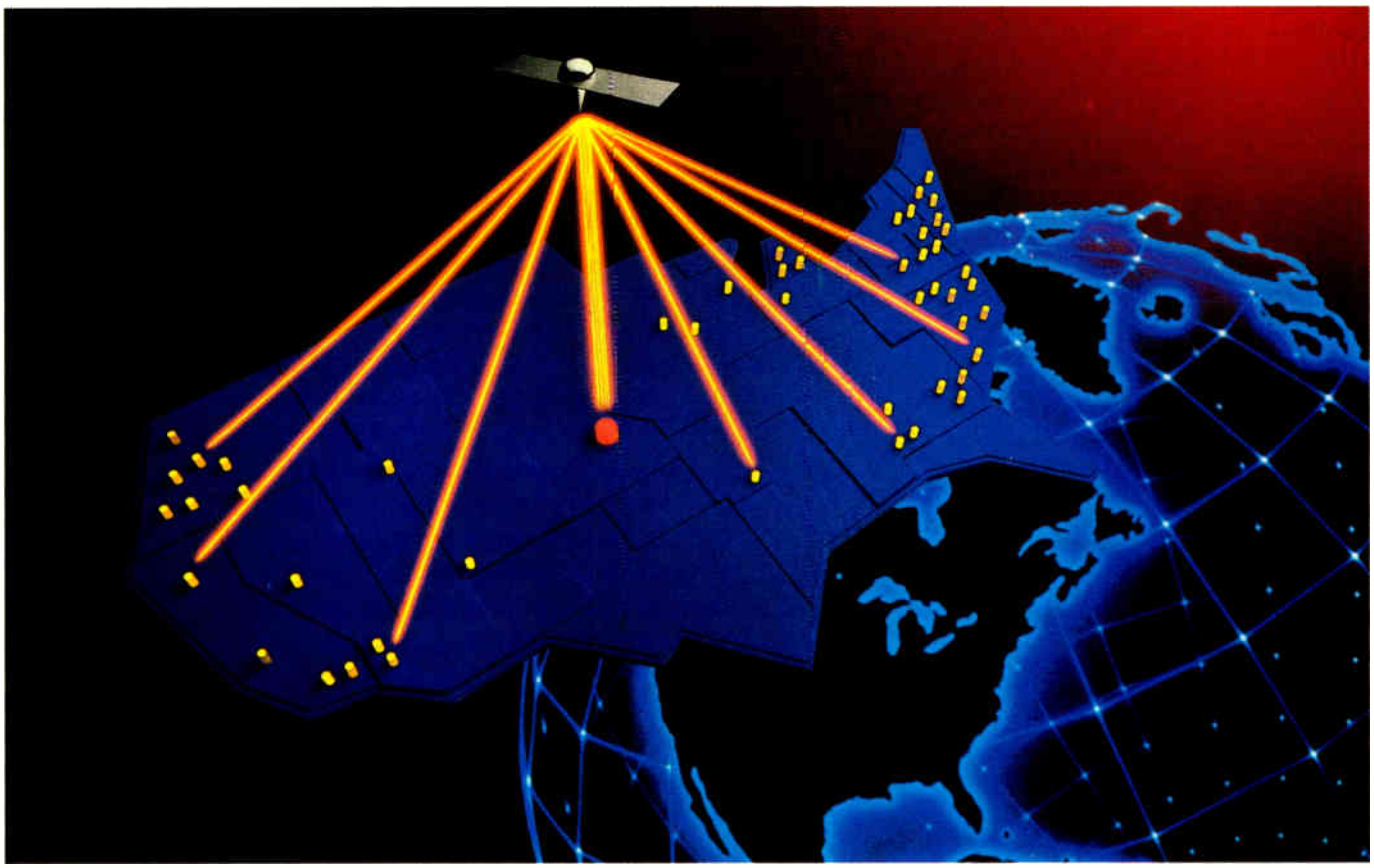
"The era of off-the-shelf LSI gallium arsenide chips is coming, and engineers will not have to wait long to begin designing these parts into systems. Vitesse Electronics Corp. is launching GaAs versions of three Advanced Micro Devices parts, plus a novel 1-K-by-4-bit static RAM.

Vitesse's announcement constitutes the first commercial availability of LSI logic in gallium arsenide. Further, if the company lives up to its announced delivery schedule, it may also be the first U.S. company to begin volume production of GaAs LSI logic, commercial or otherwise. However, other companies are also planning GaAs parts, and next year should see a flood of similar LSI products..."

Excerpted from an exclusive article in the September 18, 1986 issue.

Electronics

THE LEADER IN NEW TECHNOLOGY COVERAGE



"NEXTAR" MINI EARTH STATION NETWORK.

Private Ku-band satellite communications networks using mini earth stations on customer premises are poised to take off in the US.

Our advanced mini earth station networking system "NEXTAR" offers unprecedented flexibility for transaction-oriented businesses typically using POS, ECR and ATM systems.

The NEXTAR provides interactive data communications between a central hub and many widely-dispersed remote mini earth stations in a "star" network topology. Our exclusive Adaptive Assignment TDMA system automatically assigns the best pathway for each data message to minimize response time for short interactive messages and increase throughput during long batch transmission. NEXTAR transparently interconnects existing remote terminals and the host's front-end processor thanks to its intelligent network features.

The mini earth station, a 1.2 or 1.8m antenna with an integral RF package and compact indoor unit, takes less than a workday to install. Site selection and licensing are also simplified with the Ku-band. The central hub station with comprehensive monitoring, control and diagnostic capabilities can be located adjacent to a data center or at a shared site.

The NEXTAR network can be custom-tailored to a user's exacting needs—data rates from 75bps to 56Kbps plus voice and video capability. It eliminates the wasted transmission capacity and high cost of traditional alternatives.

C&C
Computers and Communications

NUMBER 137

1.3-MICRON OEICs FOR GIGA-BIT LINKS.

Scientists at the NEC Optoelectronics Research Laboratory have successfully tested the world's first optoelectronic ICs to operate in the 1.3μm band at data rates of 1.2Gbps.

The optical transmitter and receiver chip pair set records of a 12-km communication at 1.2Gbps with a 7.7dB margin, and 22-km transmission at 565Mbps with a 9.9dB margin in the experiment using a single-mode fiber.

The new light-emitting chip incorporates a 1.3μm DC-PBH (double-channel planar buried heterostructure) laser diode and three InGaAsP/InP hetero-junction bipolar transistors on the same InP substrate. Modulation up to 2Gbps is possible in NRZ mode. A peak output of 20mW was marked at 1Gbps.

The optical receiver integrates a PIN photo diode and three low-noise InGaAsP junction FETs on a single chip for sensitivity of −14dBm at 1.2Gbps.

NEC's new OEIC pair will be the ideal workhorse in medium- or short-distance ultra-high speed links including LANs, local subscriber loops and interconnections of computers and peripherals because it promises much lower cost and smaller size than prevalent discrete devices.

These OEIC devices will reach the market within a few years.

NEAX61 NOW IN SERVICE AT 1,002 EXCHANGES.

Our NEAX61 digital switching system continues to play a key role in the phenomenal expansion of digital networks around the world.

Since its implementation in 1979 the NEAX61 has captured the attention of telecommunications administrators globewide for its sophisticated modular hardware and software, advanced service features, and full operation and maintenance support.

Today there are NEAX61 switches in service at 1,002 exchanges in 37 nations—more than 5 million equivalent subscriber lines in all. With recent orders from New Zealand (400,000 lines), Hong Kong (600,000 lines) and Venezuela (330,000 lines) the aggregate orders received now exceeds 10 million equivalent subscriber lines.

NEC OPTICAL REPEATERS GO TRANSPACIFIC AND SUBMARINE.

The trend in transoceanic submarine cable systems is undeniably "optical". The use of fiber optic transmission technology increases capacity, extends repeater span and ensures compatibility with land-based digital networks.

Under a contract awarded by KDD, Japan's leading international telecommunications network, NEC is manufacturing optical submersible repeaters and optical terminal equipment for the third Trans-Pacific Cable (TPC-3) which will link Hawaii and Japan with a branch to Guam.

The TPC-3, to be completed in 1988 and owned by 22 telephone operating companies in 10 countries, will have two 280Mbps systems, offering a total capacity equivalent to 7,560 telephone channels—a dramatic increase from 138 channels with TPC-1 and 845 channels with TPC-2.

Incorporating our 1.3μm DC-PBH (double-channel planar buried heterostructure) laser diodes and newly-developed high-speed monolithic ICs, the optical repeaters are designed to maintain high reliability on the ocean floor at a depth up to 8,000 meters.

Dowty Power Supply Conversion Ltd. And it is shopping for a U.S. power-supply manufacturer. "When each division was operating on its own, they were finding it difficult to fund substantial development projects and support the export market. The group company can now shoulder the cost of the overseas sales effort," says Nigel Mattinson, managing director and chief executive of the new company, in Salisbury.

To bolster its product line, Dowty is looking for a U.S. maker of avionic power supplies, he says. "We already do make some that are used by other Dowty companies, but we have no significant presence."

Meanwhile, Dowty has been selling power supplies in the U.S. for 18 months and reports some success. The company grossed $38 million in power supplies last year, $2.5 million of that in the U.S. It will soon start delivering 10,000 high-voltage supplies a month to a "major U.S. high-technology company" that Mattinson won't name. He says, "We are now beginning to be known [in the U.S.] as a supplier of custom power supplies." He adds that he expects U.S. sales to reach $35 million within two years.

One of the company's biggest customers is IBM Corp., for which it makes the power supplies for the Personal Computer model sold in the UK. "We don't want to become totally reliant on IBM, so we are sticking to their UK sales," Mattinson says.

MATTINSON: Dowty's power-supply sales in the U.S. will reach $35 million in two years.

While Dowty is attacking U.S. manufacturers on their own soil, Pascall, a $3 million components maker on the Isle of Wight, is trying to kick the U.S. out of the UK defense market. With no UK company able to produce supplies that are small enough and reliable enough at a wide range of temperatures to satisfy military specifications, most of the 30- and 50-W dc-to-dc converters in UK military electronics systems come from the U.S.

HOT AND COLD. Pascall's supplies are designed to work in the high temperatures next to an airplane engine as well as the freezing cold of the plane's extremities. Called Powermite, the converters operate at 30 and 50 W between −55°C and +100°C. The firm has shrunk the devices by using newer ferrite materials, smaller coils, and, most importantly, surface-mount technology. They cost $650 to $1,100, compared with about $1,600 for the U.S. products.

The converters are also the smallest available from a UK supplier. A company spokesman points out that although some of the U.S. supplies are smaller to begin with, components added to meet the military radio-frequency-interference specifications make them bigger.

Pascall will start selling in Europe early next year. If it is successful, the U.S. is next. Unfavorable exchange rates could make it difficult to compete on price in the U.S. But because the size of orders in the U.S. tend to be larger, Pascall will probably be able to reduce the price enough to be competitive, the spokesman says. *–Steve Rogerson*

SPEECH PROCESSING

COMING: A SYSTEM FOR REAL-TIME DIALOG

MUNICH

For computer makers, the ultimate talk show would be a machine that could listen to its user, "understand" the query, and then answer right back. No one yet has made such a machine, of course, but a Dutch-German group has started to move in that direction. It has put together an experimental dialog system—Spicos 1—that gives spoken answers to questions and instructions put to it in continuous human speech.

Spicos 1, to be sure, has its limits. It has a limited vocabulary, roughly 1,000 words. Questions put to it must match the patterns of some 200 characteristic sentences. The system is speaker-dependent—that is, it must be "trained" to recognize the voices of specific operators. Above all, it is slow, taking five minutes to analyze each word in a query, go through its files, and formulate answers. But a system that works in close to real time isn't far off.

TALKATIVE. The Spicos dialog system understands fluent, continuous speech and replies to the speaker.

Even so, Spicos 1 goes well beyond the capabilities of commercial speech-recognition equipment now on the market or close to it. Some of this gear offers vocabularies as high as 20,000 words, but the words must in most cases be uttered one at a time; the systems can't recognize them as sentences. The Dutch-German system, by contrast, swallows whole sentences, a considerably more difficult task—so much so that commercial versions of Spicos won't be in sight until the 1990s.

Spicos 1 is the fruit of a three-year, $8 million effort by Siemens AG in Munich, Philips GmbH in Hamburg, and the Institute for Perception Research, or IPO, in Eindhoven, the Netherlands ("Spicos" stands for Siemens/Philips/IPO Continuous Speech). Demonstration models have been built at Munich, Hamburg, and Eindhoven.

The models are programmed to recognize and interpret German words commonly heard in engineering and office environments. In theory, the system can cope with up to 1.5 trillion different questions and replies, says Manfred Lang, senior director and head of the Signal Processing Department at Siemens's Central Research Laboratories in Munich. That is the estimated number of combinations possible with the 1,000 words stored in a data bank and the characteristic sentence structures the system understands (for example, sentences starting with what, when, where, or how, and preferably having no complex clauses).

INTERPRETER. Spicos has enough linguistic talent not only to understand the literal meaning of words but also to interpret ambiguous words and sentences. For example, from the context of a sentence, it can determine the correct different meaning for, say, "paper"—

whether it's a noun denoting a piece of paper, a dissertation, a newspaper, or a verb meaning to "paper" over.

Spicos first acoustically analyzes, word for word, a question spoken to it through a microphone. It then feeds each word to a syntax module that recognizes whether the word is a verb, noun, preposition, or another part of speech. Supporting the word-recognition process are a German pronunciation dictionary and a language model that represents the structure of the 200-odd characteristic sentences in the form of a network.

Next, the system compares the acoustic characteristics of the spoken words with reference patterns. Then, using statistical methods, a semantics module generates word-and-sentence hypotheses, which are fed to a linguistic-analysis module. That module generates grammatically correct sentence structures. These are transformed into semantic trees to determine the meaning of a sentence.

MATHSPEAK. A dialog module determines what type of sentence is involved and formulates an answer in mathematical form. The answer is transformed into an understandable sentence, which can be displayed on a screen or fed to a speech-synthesis module and played on a loudspeaker.

The Spicos 1 demonstration model uses a VAX 11-780 computer from Digital Equipment Corp. Together with Siemens and Philips peripherals, it controls all processes involved in speech analysis, data-bank search, and speech digitization and synthesis. The various modules are implemented in software.

Future work by the Philips/Siemens/IPO team of physicists, linguists, and computer scientists is aimed at a system that understands English, can ask counter-questions, and can understand anyone who speaks to it, not just the people whose voices it recognizes. The effort is sponsored by the Dutch Economics Ministry and West Germany's Ministry for Research and Technology.

Another goal is real-time dialog. A big step, Lang says, will come from high-speed signal processors that are expected to come on the market soon.

–John Gosch

DISPLAYS

HOW STC IS BOOSTING LCD RESOLUTION

HARLOW, ENGLAND

A British company, STC Technology Ltd., has developed a liquid-crystal material that it says will yield displays offering exceptional sharpness, higher resolution, and a viewing angle of virtually 180°. The key to the sharpness and the high resolution is that the material is stable in both the transparent and opaque states. And the wide viewing angle—some 20° better than the best reported up to now—is the result of achieving contrast through scattering rather than through polarization.

The stability of the new material, which is in the LC family classified as smectic A, means it does not need refreshing after every 200 or so lines as is common with conventional, unstable, LCDs, a requirement that makes it impractical to have a large number of lines. But with the STC material, there is theoretically no limit to the number of lines. This permits a choice between a large screen or a smaller one with the same number of lines closer together to improve resolution. Initial plans are for the latter: screens with more than 1,000 closely spaced lines, says STC.

At least one expert who has seen a demonstration of the panel reports that the quality of the picture is uncommonly high. "It's more like looking at a piece of paper than at a display," says Peter Batchelor, who is principal engineer at the British Department of Trade and Industry.

The displays will be aimed at the high-end market for use in such systems as projectors for business conferencing, desktop publishing, and educational work stations. STC is particularly high on one application: in an overhead projector that would be driven by a computer. The company has not yet set a price for completed panels, but says that they will compete with standard monochrome cathode-ray-tube displays.

Samples of the material, based on cyano-biphenyls, are available from STC in Harlow. But production units will come from a joint-venture company, Image Displays Ltd., when its factory in Cambridge is completed next year [*Electronics*, April 16, 1987, p. 53]. STC formed the joint venture with Alcatel NV of Holland and venture capitalists.

Other LC materials change states by polarizing the molecules. But with STC's material, the job is done by aligning or scrambling them with the application of a high or low frequency to each pixel. A high of about 2 kHz aligns the crystals and makes the screen transparent, and a low of about 100 Hz scatters them and makes the screen opaque.

Dopants and redox agents are added to the cyano-biphenyl material to facilitate dynamic scattering. The liquid crystal must also be doped with an ionic material whose mobility along the direction of the smectic layers is greater than its mobility through them. The result, as in nematic dynamic scattering, is that scattering becomes increasingly difficult as the frequency of the applied field goes up. Above about 1 kHz, scattering stops.

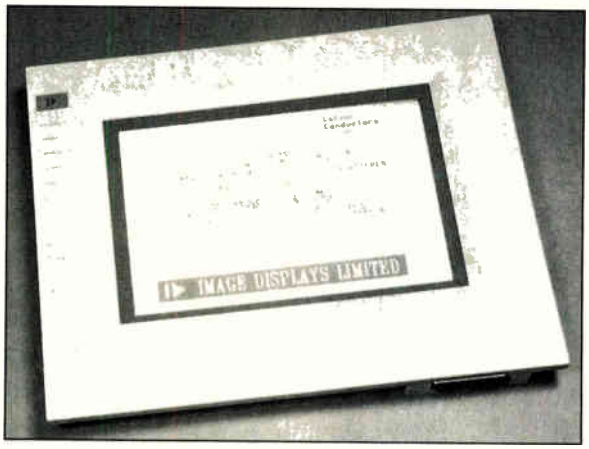
The cyano-biphenyl material needs no refresh current because below a certain temperature that is well above room temperature, the material is in its stable scattered state—unless voltage is applied. This state can be induced by short-duration monopolar or bipolar pulses, according to the company.

SCREEN BLANKING. The screen is first blanked by scattering the crystals in all the pixels. Information is then scanned onto the screen a layer at a time. When a scan is finished, the row and column voltages fall to zero, since no voltage is needed to maintain the information.

Blanking not only can be done on the whole screen but also on any number of individual rows. It takes about 40 ms for a full blanking. The scanning voltage is applied to the rows and a different voltage is applied to the columns. These voltages are in a square waveform. If the row voltage is out of phase with the column voltage, the pixel will be cleared; if they are in phase the pixel will be scattered.

The display needs no special lighting. However, two methods—straight rear illumination and front illumination with a reflective Fresnel backing—are particularly suited to overhead or slide projection.

–Steve Rogerson



WIDE SCREEN. New liquid-crystal display from STC has on-screen memory and a viewing angle of virtually 180°.

Cadnetix
the standard C

Finally, full-function CAE for your standard IBM PC.

For a long time, full-function CAE and a standard IBM PC couldn't be mentioned together in the same breath. The Cadnetix PC System has changed all that.

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The super-computer power of Cadnetix Engines, directly available to your PC's.

With Cadnetix, your IBM PC becomes much more than a normal entry-level CAE workstation. For fast analysis of your largest designs, Cadnetix gives you direct access from your PC to our full line of CAE Engines.

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- Physical Modeling Engine: This engine simulates

introduces AE workstation.

VLSI chips at vector rates of up to 16 MHz and accommodates devices with up to 364 inputs and 384 outputs. Vector storage of 512K x 91 bits provides for longer simulations and simultaneous analysis of up to 30 devices.

Powerful Cadnetix engines complement PC capabilities, achieving top efficiency in compute-intensive design tasks while supporting lowest-cost per engineer for routine access.

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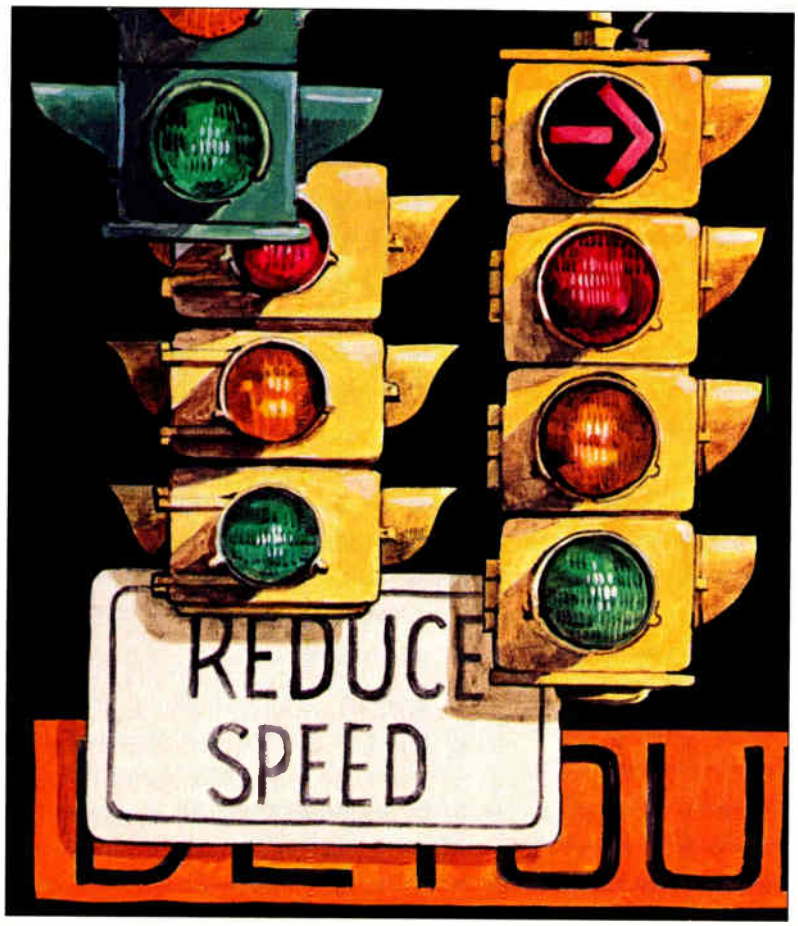
Circle 41 on reader service card

SPEEDS I/O TRAFFIC.



A system with independent processors and 35-MHz bus, capable of moving 200 megabytes/s, takes over data-transfer chores from central processing units.

How Aptec plans to break the input/output bottleneck.

"Input/output is the neglected stepchild of computer systems. Little has been done to make I/O pathways fast enough to keep up with central processors and memories. But now, I/O bottlenecks are getting more attention from specialized vendors as well as some designers of high-performance computer systems.

One way of cracking the bottleneck is by giving all of a system's I/O tasks to a separate computer equipped with its own high-speed processing units and wide-bandwidth data bus. Following this approach, Aptec Computer Systems Inc. has come up with the fastest central processing units and peripherals available today—reaching peak data rates of 200 megabytes/s..."

Excerpted from an exclusive article in the November 13, 1986 issue.

Electronics

THE LEADER IN NEW TECHNOLOGY COVERAGE

PROBING THE NEWS

INTELLECTUAL PROPERTY TURNS INTO HIGH-PRICED REAL ESTATE

CHIP MAKERS GET AGGRESSIVE IN RAISING THE RETURN ON THEIR PATENTS

by Clifford Barney

SAN MATEO, CALIF.

A wave of legal cases has swept the semiconductor industry as chip makers have become far more aggressive in standing up for the rights to their intellectual property, in the form of technology patents and copyrights. A tightening of practices on the second-sourcing of major chip products can also be seen, as companies who have invested heavily in developing, for example, 32-bit microprocessors, attempt to wring as much return as possible—in the form of dollars or exchanged technology—from their R&D investment.

Avoiding second-source pacts and prosecuting any company that steps on copyright or patent rights while attempting to build similar chips are both ways to prevent direct competition for a new product from appearing quickly to drive prices and profits down. Enforcing intellectual property rights is growing more important because the industry, particularly the Japanese segment, has become very adept at getting competing products to market quickly.

But chip companies are also pursuing such rights more vigorously than ever simply because recent changes of the law and court decisions have made it far easier to do so. Copyright law has been changed to cover both software and chip designs, and the Intel-NEC court case appears to be setting a precedent in favor of the originator of microcode, as well. In addition, a new appeals court that hears only patent cases has made the patent laws easier to enforce.

With new legal tools making it easier to protect intellectual-property rights, established chip companies with fat patent portfolios are moving to captialize on their past work. Collecting substantial license fees has grown very attractive, and Texas Instruments Inc.'s latest quarterly report shows how big this can pay off. After suing several Japanese makers of dynamic random-access memories, the Dallas company has succeeded in collecting large royalty fees, thanks to its patents on DRAM technology.

Both Intel Corp. and Motorola Inc. are showing great reluctance to let other vendors make versions of their 32-bit processors; second sources have helped drive down the prices of microprocessors in the recent past, cutting into the profits of the original developer. At the very least, Motorola and Intel expect to get something very significant in return for the rights to second-source their 32-bit processors—such as the rights to manufacture parts having what they see as equal value. "Semiconductor companies have stopped giving technology away for a song," says industry analyst Dan Klesken of Montgomery Securities Corp., San Francisco.

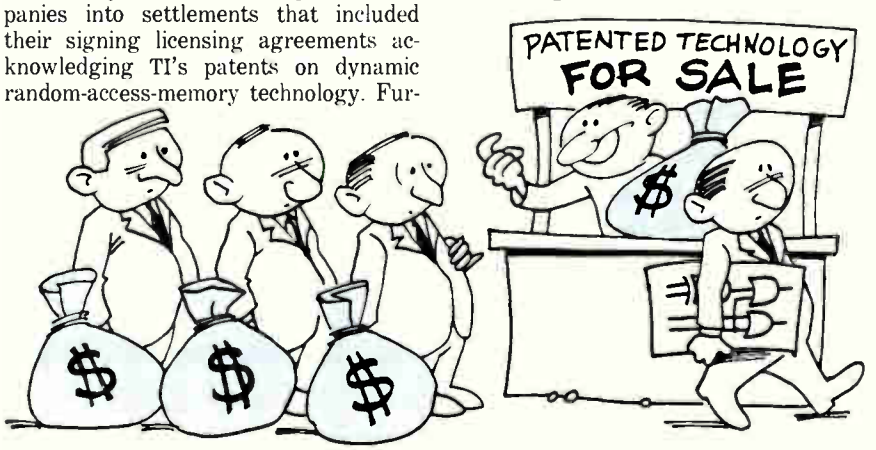
Not everyone likes the idea of aggressive protection for intellectual property. Chip makers that don't have a great many patents aren't happy with it, for obvious reasons. More disinterested observers wonder whether the march of progress will slow down considerably if a handful of large companies decline to share their technology and designs.

The latest example of a chip maker successfully reaping rewards in an intellectual-property battle is the extraordinary $108 million item listed on the TI balance sheet for the first quarter of fiscal 1987, released just before its annual meeting April 16. The money represents three years of royalty payments the Dallas-based company won from the six Japanese chip makers. A series of lawsuits by TI forced the Japanese companies into settlements that included their signing licensing agreements acknowledging TI's patents on dynamic random-access-memory technology. Further royalties will accrue on a per-unit basis until 1990. And the clear message from TI's top executives is, "You ain't seen nothin' yet."

TI president Jerry Junkins told stockholders at the annual meeting that he expects to see an era of much greater protection of patents in the industry. After the meeting, he said that TI is actively exploring its patent portfolio and the company might go after companies in areas besides DRAMs, although he would not be specific. Privately, TI executives say they expect the company to sue some U.S. companies as well as foreign-based manufacturers that are violating patents. One even admits that "you can probably expect us to be the target of some lawsuits as well."

Gordon Moore, chairman of Intel, Santa Clara, Calif., also predicts that semiconductor companies will henceforth become much more aggressive over their intellectual property rights [*Electronics*, April 2, 1987, p. 65]. Intel itself certainly intends to: it has hired a top patent lawyer to guard its interests.

He is Carl Silverman, one-time chief patent counsel for Schlumberger Ltd. and before that for the General Electric Co., and now Intel's chief counsel for intellectual property. He lays out Intel's position in forthright terms. "We are now action-oriented," Silverman says. "Intel has a significant portfolio, and we are willing to take action based on it.



Some companies are still living in 1973 or 1980. But this is a new day." Intel's suit against NEC is one sign of its aggressiveness. Another is the wrangling between Intel and its Silicon Valley neighbor, Advanced Micro Devices Inc., Sunnyvale, Calif., over rights to second-source members of the iAPX microprocessor family. AMD has been second-sourcing chips in that family, but now, because of a disagreement over a seven-year-old math coprocessor, the 8087, Intel and AMD are heading for binding arbitration. Intel has used the occasion to cancel the second-source agreement for any new members of the family, five years into what was to have been a 10-year pact.

In other action, Monolithic Memories Inc. of Santa Clara has nailed down many basic rights to programmable-array-logic technology and is suing anyone who won't acknowledge them. A suit against Altera Corp., also of Santa Clara, ended with a settlement in which Altera fell into line with MMI's demands. MMI's litigation against Lattice Semiconductor Corp., Beaverton, Ore., continues.

Motorola's Semiconductor Products Sector is reportedly seriously considering enforcement of a patented dynamic-bus-sizing concept. Several popular 32-bit microprocessors can self-configure for 8-, 16-, or 32-bit data paths, and their makers may be asked to pay license fees, Motorola managers say.

Motorola is also holding out for a major transfer of technology in return for second-source rights to its 32-bit 68020 microprocessor. "We are not in the business of selling technology," says Jeff Nutt, technical marketing manager for the 68000 family. "We want to exchange technology for equal technology."

Only Thomson CSF has the rights to manufacture the 68020, and only in France—and Motorola is reportedly dragging its feet about transferring the technology to Thomson. Meanwhile, it has rebuffed several determined efforts from Signetics Corp., which has so far struck out with offers of three complex 68000-family peripherals. On the other hand, Motorola managers in Austin, Texas, hint that the 68020, and the future 68030, may become one of the chips made by Motorola's joint venture with Toshiba Ltd. in Japan.

Intel appears to want to go completely without second sources for the 80386, the 32-bit microprocessor that is everyone's bet to take over the office workstation market. AMD made a commodity item out of the 16-bit 80286, which Intel had spent millions to develop, and the Santa Clara firm is not about to let that happen again with its $100 million 80386.

Cutting back on second sourcing worries systems houses, though. "If customers like us had a choice, we'd prefer two sources," says chief executive officer Michael Dell of PC's Limited in Austin, makers of an IBM Personal Computer clone. Dell notes that AMD both kept the price of the 80286 processor down and kept Intel honest by driving its speed higher.

PATENT MAN. Changes in the legal system have made patents more valuable, says Intel's Silverman.

One reason for increased attention to intellectual-property issues is that a growing number of companies have no real assets except their intellectual property. For example, Brooktree Corp., a San Diego startup that markets chips for graphics work stations, is one of the new breed of design-only chip houses that relies on foundries for all its manufacturing. It takes patents so seriously that it has a patent attorney on its board of directors. Designs, says President James A. Bixby, are "all we have—the basis of the company."

A new patent court is making it easier to fight patent cases—and win

But many have taken to heart the lesson of TI's success in collecting from Japanese licensees. The two biggest DRAM makers, NEC and Hitachi, and Samsung of Korea, resist negotiating a settlement, but the six companies that have settled noticeably improved TI's bottom line. What TI has done, others can do—particularly in light of today's more favorable climate for intellectual-property protection.

Experts point to the restructuring of the court process and strengthening of copyright and patent law as key factors contributing to the increasing power of intellectual-property rights. Before 1982, patent cases could be appealed to any federal circuit court. In that year, a new appeals court was formed specifically for patent cases. This court "made life more uniform" for patent lawyers, says Intel's Silverman. In some circles, it is seen as a pro-patent court.

Derek Lidow, senior vice president of International Rectifier Corp., El Segundo, Calif., agrees with Silverman on the importance of the new court. International Rectifier holds basic patents on MOS field-effect transistors. However, working with the circuit courts, it could collect on only half of its cases. "Who wants to stake a birthright on the flip of a coin?" asks Lidow. In the new court, he says, patent holders are winning 80% of the time.

Coupled with the new patent court are changes in copyright laws that are now being used as the basis for legal rulings. Last September's decision that Intel's 8086-family microcode is protected by copyrights was based on a 1980 amendment bringing software under the protection of the Copyright Act, and the 1984 Semiconductor Chip Protection Act, which covers chip designs. How close a copy can be without infringing on a copyright remains to be determined.

Copyright standards tend to be broad and not rigorous, says analyst Michael Boss of Dataquest Inc., San Jose, Calif. The second part of the Intel-NEC decision from District Judge William Ingram will serve to "calibrate" the copyright protection, Boss adds.

The increased emphasis on protection of intellectual property is not universally welcomed. Raymond P. Capece, executive vice president and general manager of Lattice Semiconductor Corp., Beaverton, Ore., warns that excessively strict controls on licensing and patents can hinder technology development. "The ability to apply new technology to older and widely used concepts is what leads to new inventions and better products," Capece says. "Patent rights can be leveraged to prevent new developments from reaching the market."

In general, says MMI marketing vice president Tim Propeck, it's going to be tougher for companies to ignore the patent laws. "They may not be excluded, but they will have to pay for access to the technology." Cross-licensing will occur between established companies that already have patent portfolios, he adds.

And the movement to the use of standard cells could also come to bear on intellectual-property issues. Many standard chips have been incorporated into cells that are used to build application-specific ICs. The result: "We're going to see a lot of positioning in alliances for standard-cell libraries," Boss says. "The window of opportunity is limited."

Additional reporting by J. Robert Lineback and Larry Waller

CUSTOM IC CONFERENCE LOOKS LIKE A REAL WINNER

A WIDE RANGE OF DENSER, SPEEDIER ARRAYS; FASTER TURNAROUND

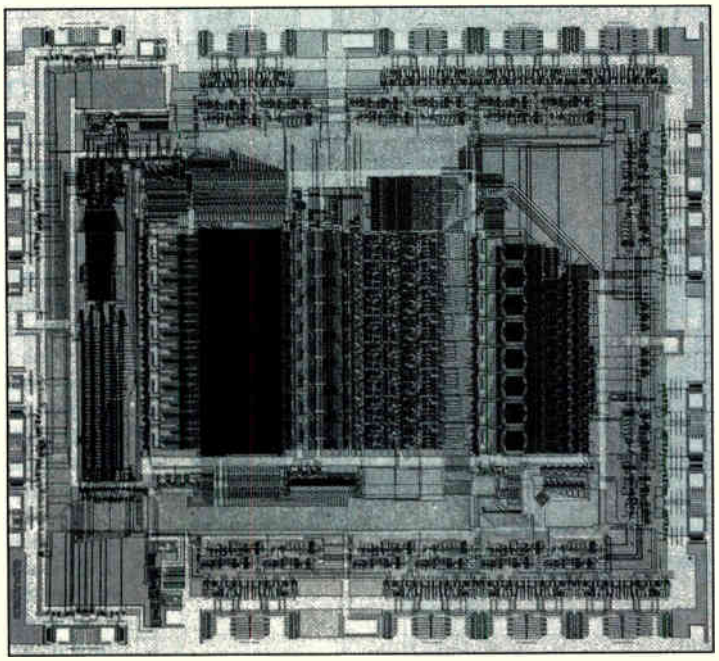
by Bernard C. Cole

The Custom Integrated Circuits Conference is where the designers of custom and semicustom circuits shine. At technology shows like the International Electron Devices Meeting, their achievements are often overshadowed by the work of device physicists and designers of standard circuits. This year's CICC in Portland, Ore., will be no exception: the custom and semicustom crowd will put on one heck of a show.

Papers to be given at the on May 4-7 CICC indicate that a variety of techniques are rapidly pushing field-programmable logic devices to higher density levels. For semicustom logic devices that are not electrically programmable, designers are working on methods to produce fast-turnaround chips using direct writing with laser and electron beams. The perennial push of gate arrays and standard-cell parts to higher speeds and densities also continues apace.

Users of custom and semicustom chips are always on the lookout for better design tools, and papers at the CICC will introduce, most notably, tools for developing linear and analog circuits. And a bevy of leading-edge custom designs will be described, including special-application memories; the meeting will also feature a session on somewhat less-radical custom products and services that are available right now.

In the regular sessions, one of the hottest topics will be semicustom approaches that add the density and functionality of gate arrays to fast-turnaround field-programmable logic. From Intel Corp.'s Folsom, Calif., operation comes the first in a family of application-specific electrically programmable logic devices: a three-port transceiver (see photograph) with embedded logic macrocells based on erasable programmable read-only-memory, as well as crosspoint signal routing that allows the user to implement a wide variety of bus-interface alternatives. From Xilinx Corp., San Jose, Calif., will come a description of its second-generation family of programmable gate arrays based on static random-access memory, arrays that will allow densities far in excess of the 1,500 to 3,000 gates on currently available EPLDs. Also showing promise of extending the density levels of EPLDs is a new architecture from Amtel Corp. of San Jose, Calif., and Western Digital Corp. of Irvine, Calif. Where current EPLDs combine nonvolatile elements with AND/OR logic arrays, this new entry combines an uncommitted gate array with a front end containing 128 logic primitives. Each of these logic primitives is capable of performing the functions of 4 to 16 gates.



FLEXIBLE. Intel's three-port transceiver is an EPLD with embedded logic macrocells and crosspoint signal routing for bus-interface flexibility.

In another area, several companies aiming at quick turnaround will describe direct-write techniques using laser and electron beams. From Laserpath Corp., Sunnyvale, Calif., comes a new family of laser-programmable-gate two-level CMOS arrays with densities as high as 5,000 gates and a turnaround time of 24 hours. Hitachi Ltd. of Japan is pushing the densities of fast-turnaround devices even higher with a direct-write E-beam technique that achieves densities as high as 24,000 gates using a 1.3-μm twin-tub CMOS process with two levels of metal and tungsten silicide gates. And from VLSI Technology Inc. of San Jose and Elron Electronic Industries Ltd. of Haifa, Israel, comes an experimental laser-programming methodology. Still under development, the technique promises densities as high as 25,000 gates and a turnaround time of no more than a few hours.

Traditional standard cells and gate arrays are also continuing to make progress, as manufacturers aggressively push speeds and densities. Aiming for high density is a 150,000-gate 0.5-μm CMOS channelless gate array from Motorola Semiconductor's Research and Development Laboratory in Phoenix. The Motorola array uses trench isolation, 150-Å gate oxides, self-aligned platinum silicides, and three levels of metal. In addition, to shorten the turnaround time, four layers—trench, contact, gate, and first metal—are patterned by direct writing on the wafer with an E-beam.

Aiming for higher gate-utilization levels than are currently available in channelless arrays, researchers from Hughes Aircraft Co., Newport Beach, Calif., will describe a triple-level-metal 2-μm CMOS process. It achieves gate-utilization rates as high as 87% and at the same time improves speeds as much as 15% over double-level-metal implementations.

Still fighting it out for king of the high-speed mountain are silicon bipolar and gallium arsenide gate arrays. From Tektronix Inc., Beaverton, Ore., comes a novel triple-diffused, self-aligned bipolar process optimized for gate arrays, which uses local oxidation and gold-based metalization. Featuring gate propagation delays as low as 480 ps and a power consumption of 1 mW per gate, the process avoids the epitaxial collectors and

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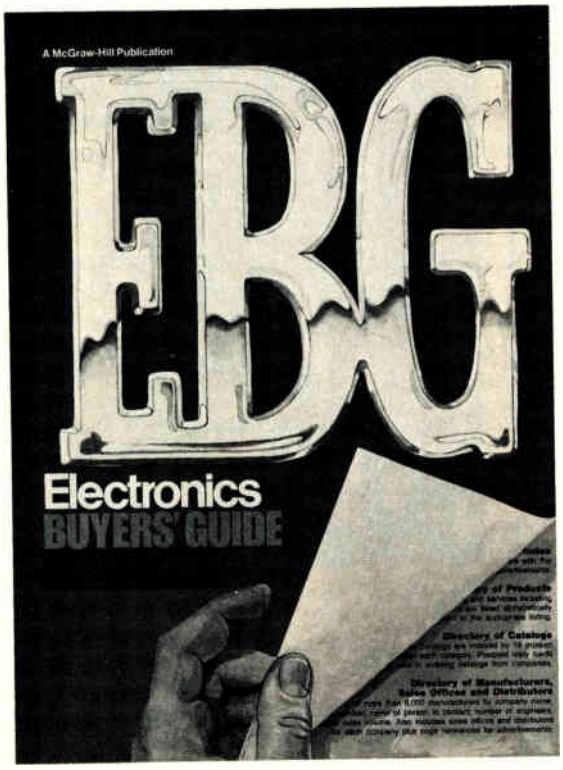

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INTERNATIONAL NEWSLETTER

WILL U.S. TARIFFS PROMPT JAPAN TO FLOOD EUROPEAN MARKETS?

The European Community is worried that Japan may redirect its electronic-equipment exports to Europe now that the U. S. has slapped stiff tariffs on some Japanese common electronic products (see story, p. 21). Officials at EC headquarters in Brussels say the community is considering protective measures in case the Japanese try to increase marketing efforts in Europe as a result of the Reagan Administration's sanctions. The fear is that Japan may divert products such as calculators, precision measuring equipment, TV sets, and tape recorders that were originally bound for U. S. stores and ship them instead to European markets. Europe's trade deficit with Japan is growing quickly—the deficit for January and February, projected for a full 12 months, indicates a year-end deficit of $21 billion, up from $18 billion in 1986 and only $12 billion in 1985. □

THE EC IS INVESTIGATING CHARGES THAT JAPAN IS DUMPING EPROMS

The Europeans are investigating charges that the Japanese are dumping chips at below-market prices by investigating Japanese chip makers that sell erasable programmable read-only memories in Europe. The European Commission, the executive body of the European Communities, is responding to complaints by European components makers. Between 1984 and 1986, Japanese EPROM makers more than tripled their unit sales in Europe, to 29 million chips by the end of last year, bringing their share of the European EPROM market to nearly 80%, according to EC officials. □

S-VHS—LATEST ENTRY IN VCR WARS—HITS JAPANESE MARKET...

The latest in high-resolution video-cassette recorders, which conform to an improved VHS standard that nearly doubles resolution to better than 400 lines, are hitting Japanese streets now, and the first should reach the U. S. by late May. In a shotgun series of April announcements, the Victor Co. of Japan, Hitachi Ltd., Mitsubishi Electric Corp., Matsushita Electric Industrial Co., and Sharp Corp. said they would begin marketing S-VHS players domestically by June. The machines, which feature 420- to 430-line resolution [*Electronics* Jan. 22, 1987, p. 45], will cost much more than most VHS systems. Prices should range from $1,500 to $2,000 for S-VHS machines. However, they will offer extra functionality. One of the two models Hitachi will launch, for example, will come equipped with a 256-Kbit video random-access memory that allows it to show as many as 12 pictures on a single screen, superimpose pictures, display digital art, and freeze individual frames. The five companies anticipate that the new S-VHS format will account for about 10% of Japan's VHS sales by year's end. The new machines will play standard VHS cartridges. □

...AS PHILIPS DEALS TO BUILD VHS VCRs IN CZECHOSLOVAKIA

The Dutch electronics giant Philips is forging its first joint venture in Eastern Europe to make VHS video-cassette recorders in Czechoslovakia. The bulk of the machines, which will be manufactured in a new facility in Bratislava, will be sold in the Eastern Bloc, but part of the deal also stipulates that Philips will market some machines in the West. The company, called Avex, is scheduled to begin production next year. It will be owned 70% by Tesla, the Czech electronics combine, 20% by Philips, and 10% by Transakta, a Czech marketing outfit. Philips will contribute its VCR manufacturing know-how and production equipment and initially will supply Avex with subassemblies and components, but by the early 1990s those parts will be manufactured in Eastern Europe. Annual output will begin at around 100,000 units, rising to more than 500,000 in 1993. □

INTERNATIONAL NEWSLETTER

SURPRISE! ERICSSON BEATS OUT SIEMENS AND AT&T IN BATTLE FOR CGCT

In the year-long battle to gain control of France's state-owned telephone-equipment maker Compagnie Générale de Constructions Téléphoniques, Sweden's LM Ericsson AB and a consortium of French firms and banks have emerged as the surprise winners. The consortium, which includes France's Matra SA, made an $82.5 million offer. New York-based AT&T Co., in partnership with Philips of the Netherlands, and West Germany's Siemens AG, in conjunction with Jeumont-Schneider of France, had been the leading contenders [*Electronics*, April 2, 1987, p. 56]. But insiders say the French were afraid of upsetting political forces in Bonn and Washington by choosing one over the other. Stockholm-based Ericsson, long considered an outsider in the competition, came to be seen as a logical "safe" choice. With control of CGCT, Ericsson will gain access to 16% of the French market for public switches. □

LASER REPEATER SUCCESSFULLY TESTED IN UK FOR OPTICAL-FIBER NET

British Telecom has successfully field-tested a laser repeater in a 120-km optical-fiber link between Colchester and Ipswich in the UK. The device, which is still in an experimental phase, is designed for long-distance fiber-optic communications links and is potentially less expensive to produce, maintain, and operate than current repeaters. These must convert optical pulses into electronic signals, amplify the results, and then reconvert them to light. The new device, however, amplifies the signal optically. It consists of a modified laser onto which a steady voltage is superimposed. This creates an electric field across the cavity between the laser's upper and lower surfaces, so when a pulse of light enters the laser's receptor, it stimulates the production of extra photons, which are used to amplify the original signal. Laboratory tests indicate the technology can also amplify multiple light frequencies and pulses traveling in opposite directions. □

SCOTTISH FIRM BUILDS AN ULTRA-THIN LED SWITCHING PANEL

Enco Industries Ltd. of Renfrewshire, Scotland, will produce an illuminated-membrane switching keypad that is one seventh the thickness of current panels. Developed in just six months, the keypad is only 2 mm thick, compared with the 14-mm thickness of the panels it aims to replace. It is a self-contained unit that requires no external support from a printed-circuit board or other source. The Enco panels use surface-mounted light-emitting diodes to light the switches, compact integral power sources, and special adhesives, and they are aimed mainly at instrumentation in hostile environments. IBM Corp. may be the first to use the panels, in point-of-sale terminals for bars and restaurants. The extra-small LEDs measure 1.6 by 1 by 2 mm. By using batteries less than 2 mm thick, Enco keeps its keypad compact and cheap. □

JUST-PC ISN'T JUST ANOTHER BRIGHT IDEA ANYMORE—IT'S CATCHING ON

JUST-PC, the Japanese Unified Standards for Telecommunications for Personal Computers, is suddenly taking off in Japan. NTT and Meiji Milk Products Co., Japan's second-largest dairy, have set up competing subsidiary companies to offer computer network services using the JUST-PC communications adapter promoted by the Ministry of Posts and Telecommunications [*Electronics*, Oct. 16, 1986, p. 113]. Masternet Inc., a wholly owned subsidiary of Meiji formed in December, will start to provide commercial services next month, including electronic mail, bulletin boards, conferencing, and other information services. Already, NTTPC Communications Inc., which is a subsidiary of NTT, is using the JUST-PC protocol to provide electronic-mail service over telephone circuits between Japan and North America and Europe. □

INSIDE TECHNOLOGY

A NEW TOOL DRAMATICALLY CUTS VLSI DEBUGGING TIME

Sentry Schlumberger's IDS 5000 integrates E-beam probing with CAD/CAE tools; it marries netlists, layout, and scope with a 'live' microscopic image of the chip

by Jonah McLeod

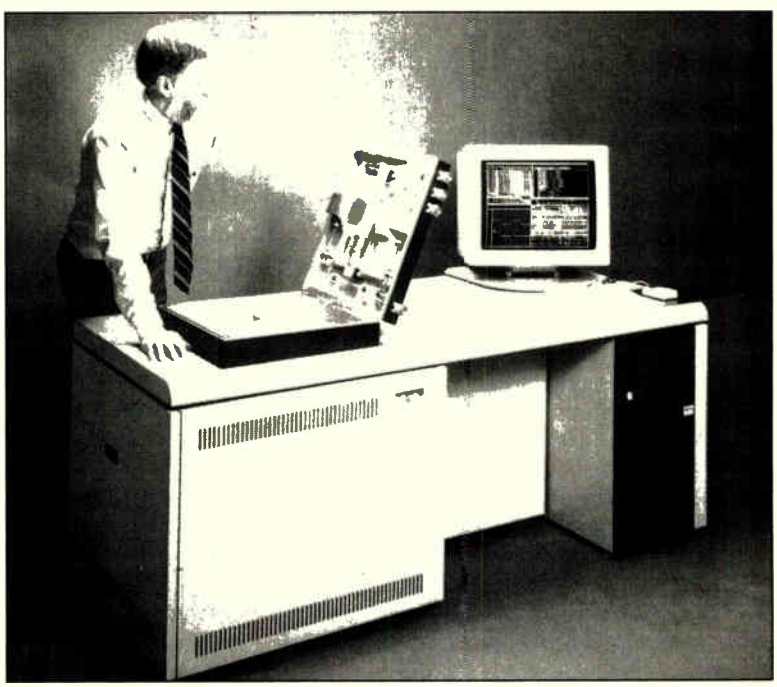
A new diagnostic tool promises to cut weeks off the time required to debug prototype VLSI devices that have submicron feature sizes. The Integrated Diagnosis System 5000 from Sentry Schlumberger Inc. of San Jose, Calif., uses an electron-beam probe and combines data from a complex VLSI chip's CAD netlist with an actual microscope image of the chip. The IDS 5000's Unix operating system allows the designer to use four closely linked diagnostic tools that appear in windows on a display screen: a netlist tool, a layout tool, a scanning-electron-microscope tool, and an oscilloscope.

The IDS 5000 is the first debugging system to integrate front-end design data—netlists and connectivity—with back-end layout data—the physical chip layout. In addition, these two data files are correlated with the actual image of the chip as seen by the scanning electron microscope. The designer can instantly correlate nets on the schematic with points on the chip, and vice versa. Also, he can probe with the on-line digital oscilloscope to display waveforms from nets on the chip.

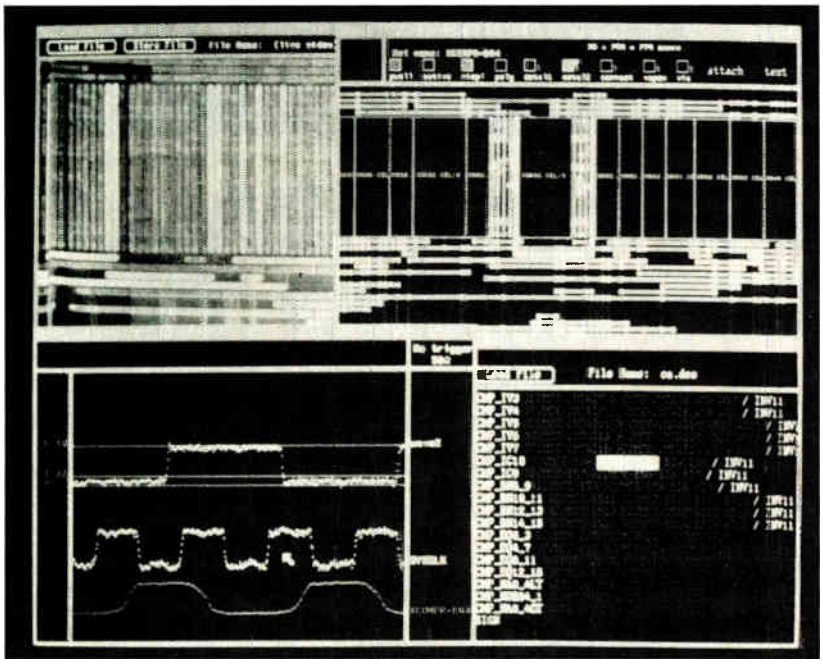
In addition, this system for the first time makes scanning-electron-microscope technology available to designers in an engineering lab. Before, these bulky and expensive microscopes, meant for scientific analysis of a wide variety of specimens, had to be modified to handle E-beam probing. The new Sentry system contains a scanning electron microscope designed and built for diagnosing VLSI chips and wafers. The company has applied for more than 50 patents on the design of the electron-optics system. The E-beam is easy to use and is smaller than conventional scanning electron microscopes, fitting into a 2-ft-square cabinet.

The IDS 5000 (see fig. 1) consists of a conventional work station from Sun Microsystems Inc. of Mountain View, Calif.; a tester providing stimulus to, and acquiring responses from, the chip under test; the microscope; and control electronics for integrating the microscope and the work station. The system will sell for around $500,000, and orders will be taken in June.

The diagnostic system is easy to use. The designer sees a display screen containing familiar diagnostic tools (see fig. 2). In one window is a live image of the chip as it appears to the microscope. In another window is the CAD layout of the chip, and in another a netlist of the schematic of the chip. In a fourth window is an oscilloscope. All four windows are correlated, and software locks the microscope display tool with the layout display tool so that each one tracks the other on-screen. "The system had to be completely interactive so that the designer gets immediate re-



1. HOOKED IN. The IDS 5000 accesses CAD/CAE data via an Ethernet interface.



2. THE VIEW. Four windows display the diagnostic tools: a netlist, a chip layout, a live image of the device under test, and a digital oscilloscope.

sponse as he moves from one window to another," explains Stefano Concina, software engineering manager.

When the designer analyzing the schematic to search for a fault finds a suspect net, he can point to the net in the netlist window, and the corresponding point appears in the CAD layout window. Using the oscilloscope icon, he can point the probe at the appropriate spot in the microscope window, and the waveform or level on the net will be displayed in the scope window. If, in observing the surface of the chip, the designer sees a broken line, he can point to it in the layout window; the netlist window will then display the corresponding line, which the designer can then locate on his schematic.

SELECTIVELY DISPLAYS LAYERS

To be able to correlate the layout data and the netlist, Sentry provides an Ethernet port for accessing the design data bases contained in the front-end CAE sytems and the back-end CAD work stations. "Most CAD systems are on Ethernet or DECnet, and most all permit file transfers using the TCP/IP protocol," says Neil Richardson, director of advanced products at Sentry-Schlumberger's VHSIC Test System Division. "The system can read layout files and netlists from these design work stations over the network."

The layout tool can accept input in Calma GDS II Streams format, in Applicon Apple 860 or CIF (Caltech Intermediate Format) CAD file formats, and in all other popular CAD file formats. The netlist tool accepts most standard netlist file formats, including Spice and Tegas. Sentry also plans to support the Electronic Design Interchange Format (EDIF) when it becomes available.

In order to view hidden nets on screen, the designer can selectively display or remove the poly layer, the diffusion layer, and so forth from the layout window. The tool can highlight nets, such as the power distribution or master clock nets, using the netlist tool.

The microscope tool displays a live video image of the chip inside its window. The tool contains all the functions needed to control the microscope, including auto-alignment. The designer can zoom, pan, or track across the netlist or CAD layout diagram of the chip, and the microscope moves in lockstep if the designer configures the system to do so.

The scope tool receives data from a special I/O processor located in the E-beam subsystem, consisting of a time-base board built with high-speed ECL and a trigger board that performs much the same function as an oscilloscope trigger circuit. "We built into the boards sophisticated signal averaging, which improves signal-to-noise ratio and ensures high-integrity waveforms," says Christopher Talbot, staff marketing engineer and the man who designed the two-board I/O processor. One function the time-base board provides is a highly accurate time delay. "We need to be able to trigger and then sample precisely at some microseconds or milliseconds later," says Talbot. The board has an edge-placement accuracy of 50 ps over a 5-ms period of time.

The scope tool performs all the functions of a digitizing oscilloscope and displays a live waveform on the screen 15 times a second. Specifications for the scope function include a maximum input voltage range of ±10 V, minimum sample-pulse duration of 100 ps, and a maximum trigger frequency of 250 MHz. In addition, the designer can define cursors, store a number of waveforms, produce a hard copy, and perform operations on the store waveforms.

The advantage in using an E-beam to probe a net on a chip under power is that it is a completely nonintrusive measurement device that cannot damage the circuit under test. "The beam adds no capacitance to the circuit that is being tested," says Richardson. "It provides a perfectly infinite impedance with no capacitance to the net being probed, and it can be focused to a submicron spot." In addition, the E-beam probe provides two capabilities not possible with any other probe. "You can see through dielectric and passivation layers in the chip," Richardson explains. "That means you can probe nets not accessible with conventional mechanical probing devices."

Probing with an E-beam uses the concept of voltage-contrast measurement. The microscope directs a fairly low-energy beam of primary electrons at the net being probed on the chip sur-

face. The system uses a beam energy of about 800 electron-volts; a conventional electron microscope typically operates at 20,000 electron-volts. "We use the low energy level so as not to generate X-rays, which can affect the operation of the circuit being tested," Richardson explains.

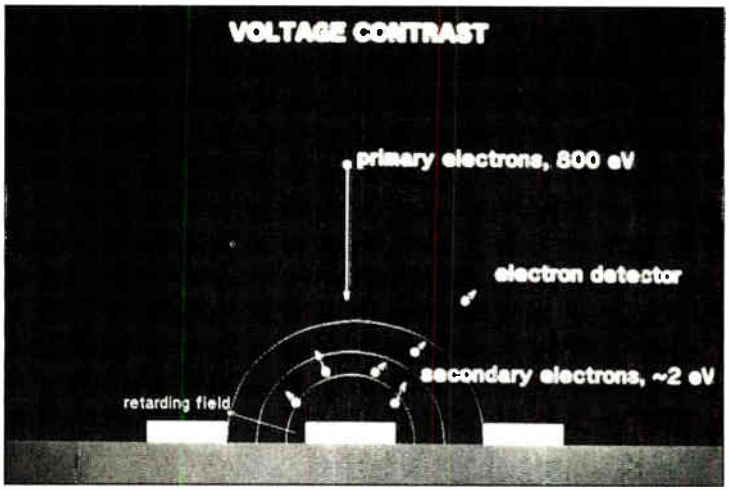
Sentry developed a special two-lens E-beam column to minimize chromatic aberration—that is, to keep the beam from blurring—to allow operation at low energy levels. At lower energy levels, electrons in the beam, which has a tungstem electron source, travel at different speeds and hence tend to spread apart before hitting the target. But in diagnosing chips, lower energy is needed so as not to damage the device.

Richardson says that his team developed a special two-lens configuration that keeps the beam focused at the lower energy level. "The beam penetrates only a few hundred angstroms, so it does not impact any of the active layers of the chip," he says (see fig. 3). "If the net being probed has a +5-V potential, there is a positive retarding field around the net that tends to reduce the amount of secondary electrons emitted when the beam impacts the net on the chip." It is the amount of secondary electrons emitted by the net on the chip and sensed by the detector—a built-in energy spectrometer—that measures the amount of voltage on the net.

One obstacle to detecting the amount of secondary electrons emitted is the local field-effect interference from surrounding nets. The lens system that Richardson's team developed also collimates the secondary electron emission very efficiently and thereby minimizes the surrounding local field effect. In addition, the new lens design reduces the number of lenses from the three found in a typical SEM to two in the Sentry system.

One other function designed into the electron-optics hardware is a built-in beam blanker for the high-speed voltage and signal-sampling operations provided by the microscope tool. In measuring a high-frequency signal occurring on a net, the system switches the beam on and off at a 100-ps sample time to digitize the waveform of the signal on the net. Because conventional electron microscopes scan a sample continuously, this capability formerly had to be added externally. In designing the electron optics of the IDS 5000 from scratch, Sentry was able to tailor the design to the special needs of chip and wafer diagnosis. □

For more information, circle 480 on the reader service card.



3. CONTACTLESS PROBE. The impact of the E-beam produces secondary electron emission for sensing voltage at a node.

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RICHARDSON IS THE DRIVING FORCE

As director of advanced products at Sentry Schlumberger's VHSIC Test Systems Division, Neil Richardson, 32, has been the driving force behind Sentry Schlumberger's diagnostic work station, the Integrated Diagnosis System 5000. He joined Fairchild's Palo Alto research center in 1982, bringing expertise in electron-beam testing. "Over a period of 18 months, I put together and operated an extensive electron-beam lab," he says. "Fairchild was having problems—stubborn bugs in VLSI designs at first silicon—that were burning up money and resources; using E-beam technology I demonstrated that I could solve these problems." He was building special E-beam test fixtures, but he knew that designers needed something more than just laboratory tools.

In 1984 Richardson moved from the Fairchild research center to the Schlumberger Computer-Aided Systems Division Labs and began work on what was to become the IDS 5000. The staff he assembled for the project includes Stefano Concina, 26, software engineering manager; Christopher Talbot, 28, staff marketing engineer; and Son Trinh, 34, senior mechanical engineer.

NEIL RICHARDSON

Concina wrote the system's software. Starting with a Sun Microsystems Inc. work station, he wrote new software to interact directly with the work station to improve performance while retaining the Sun windowing system.

Talbot built the high-speed board used to acquire high-frequency waveforms from the device under test. "There are two boards in the subsystem," he says. "I not only had to design the time-base board, but I had to program its integral on-board microprocessor as well."

Trinh's job was to build a compact scanning electron microscope. "Our application did not require the 50-Å resolution provided by a conventional scanning electron microscope," he says. "The system needed only 200 Å at most. As a result, we were able to use a much lower-power E-beam source, and we were able to reduce the number of lenses from three to two. The result was a much shorter column that easily fit into the IDS 5000."

Steven Harari, 30, marketing manager, joined the team in 1986. He expects Sentry Schlumberger will sell some $500 million worth of the IDS 5000 systems over the next five years.

SPECIAL REPORT: AI BOOSTS IQ OF SILICON COMPILERS

Thanks to artificial intelligence techniques, silicon compilers are about to deliver the long-promised goal of full automation of most of the chip-design process

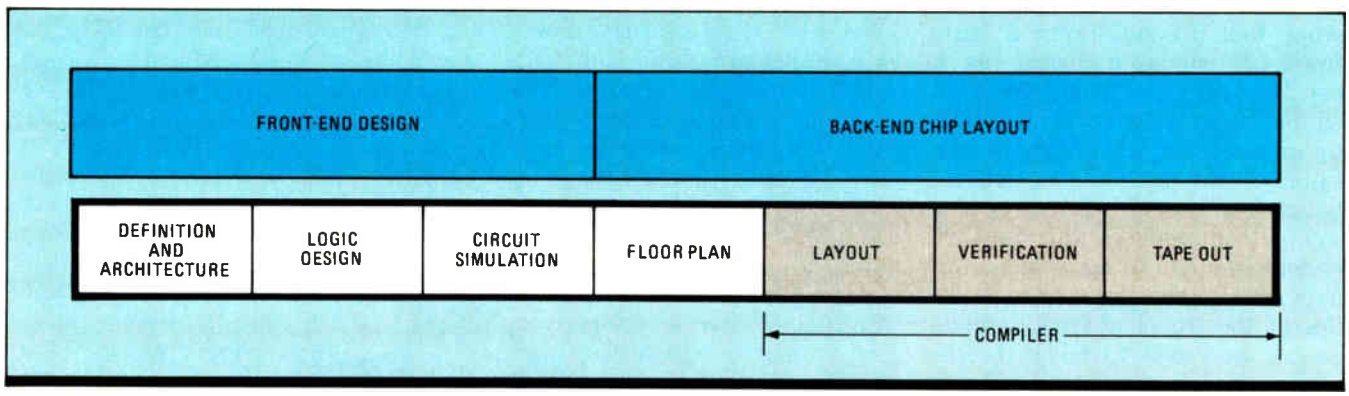
by Jonah McLeod

Silicon compilers are on the verge of delivering on their long-promised goal: full automation of a significant portion of the integrated-circuit design process. The introduction of artificial-intelligence techniques is yielding compilation software that can "learn" how to improve initial circuit designs and so offer productivity gains that go beyond schematic capture and simulation. Another important boost is coming from greatly improved circuit-optimization techniques. And one task that has resisted automation—placement of macro cells and standard cells—is making major progress, with a wide range of new automation software being introduced for this job.

One giant step toward full automation is the promise of intelligent compilation from San Jose, Calif.-based Silicon Compilers Inc., which is now called Silicon Compilers Systems Corp. after its merger with Silicon Design Labs of Liberty Corner, N. J. Advances in circuit optimization came with the advent of the Socrates system from the General Electric Microelectronics Center and a commercially available state-machine compiler from VLSI Technology Inc. Both of these systems are aimed at optimizing a single variable—speed, gate count, or area—at a time. Silicon Compilers Systems' intelligent compilation technique promises to go one step further, toward simultaneous optimizing of multiple variables.

Among the software automating the placement of macro cells and standard cells is a new chip-compiler product from VLSI Technology and a floor planner tool from LSI Logic Inc., both of San Jose, Calif. Seattle Silicon Corp. of Bellevue, Wash., and SDA Systems Inc. of Santa Clara, Calif., have introduced new place-and-route tools that also help automate placement.

Most design automation focuses on one stage of the front end of the design process, where a



1. FRONT TO BACK. Most design tools focus on one stage of the front end of the design process, while back-end tools such as compilers can only deal with the design as handed off to them. New AI-based compilers, however, will be able to make improvements that affect both front and back end.

systems designer uses CAE tools to enter his schematic and performs logical simulation to debug his design. At that point, the designer passes the debugged design to the silicon compiler (see fig. 1). With help from the designer, the compiler generates the major blocks and places them. Then it routes interconnections between the blocks, optimizing the interconnections for speed, area, or some other variable.

The compiler, in turn, passes a back-annotated netlist containing the timing of the circuit back to the designer so that he can resimulate the design to see if it meets his goals. It is possible that the circuit layout will have altered the timing of a smaller network within the larger design so that it no longer functions as specified. After the designer resimulates, he adjusts the layout or replaces components in a critical path to achieve the desired performance.

Until now, back-end tools could only optimize the design based on the initial debugged circuit. But Silicon Compilers Systems says that in the next six months it will introduce an intelligent compilation system that uses artificial intelligence techniques to learn how to make improvements in a circuit design that affect the entire design process, front end as well as back end.

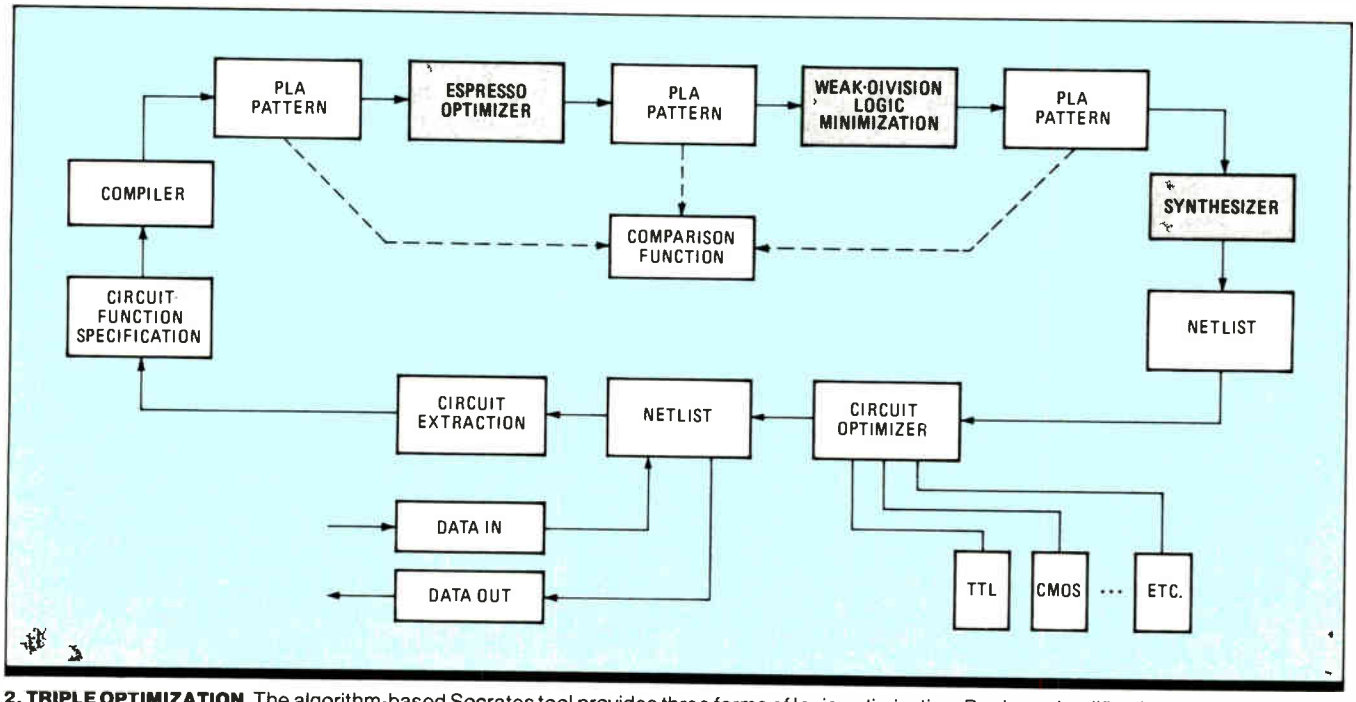
"Logic optimization is a series of rules," says David Johannsen, cofounder and vice president of Silicon Compilers Systems. The designer selects the rules the optimizer must use for a particular design, Johannsen says: "He could choose to concentrate on putting the design in the least amount of area, or he can attempt to optimize the speed of the design." Such optimizers are called heuristic schemes; that is, they are based on the trial-and-error knowledge engineers accumulate by optimizing circuits by hand.

Today, using a set of rules, most logic optimizers examine a circuit design to determine if it can be replaced with another, functionally equivalent but more efficient circuit. When a software engineer creates a logic optimizer, he is developing a table of rules. If he has a clever method for designing a circuit that is superior to other equivalent circuits, he enters the rules of the circuit into the table.

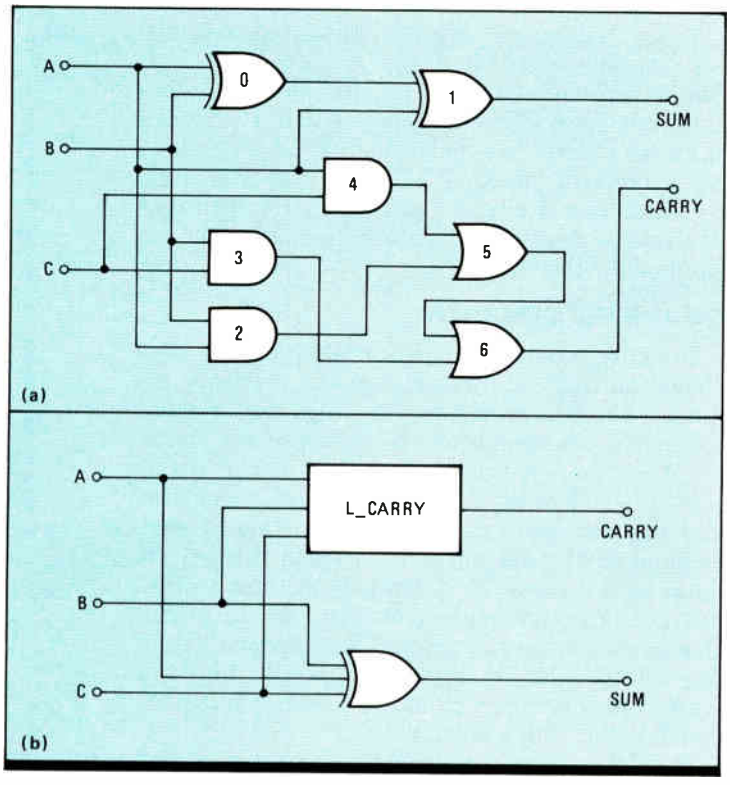
SWAPPING CIRCUITS

In many cases, there are circuits that are very similar but not equivalent, and the software engineer has to specify in the rules under what conditions one circuit can be swapped for another. With the new Silicon Compilers AI-based system, the designer enters his circuit schematic, and the program examines the function of each element of the design. It then looks through its data base to see if it contains a circuit that provides a better implementation. "If the circuit that the designer has entered is superior to all of the circuits already in the data base, the software remembers the circuit and uses it in future evaluations," says Johannsen.

Besides heuristic optimizers, there are a number of algorithmic techniques that perform efficient optimization. One of the newest is the Socrates tool developed at the General Electric Microelectronics Center in Research Triangle Park, N. C. "It builds a netlist using a gate array or standard-cell library," says Aart de Geus, acting president of Optimal Solutions Inc., also of Research Triangle Park, a spin-off of the Microelectronics Center that GE is helping to finance. Optimal Solutions will release a commercial version



2. TRIPLE OPTIMIZATION. The algorithm-based Socrates tool provides three forms of logic optimization: Boolean simplification (the Espresso PLA optimizer), redundant-gate elimination (the weak-division tool), and expert-system circuit optimization (the synthesize tool).



3. GATES TO CIRCUITS. To optimize the function of an adder, the designer might specify the circuit in terms of logic gates (a), and the system turns the logic into an optimized circuit (b).

of Socrates this summer.

"Socrates' final layout is comparable in area and speed to optimized hand layout," says de Geus. He points out that until the Socrates software was developed, optimizers could deal as well as a human designer can with area or speed, but not both. Socrates performs three types of optimization when making a netlist (see fig. 2). "First, it uses a PLA optimizer called Espresso," says de Geus. Espresso, which was developed at the University of California at Berkeley, uses algebraic methods to automatically synthesize and optimize combinatorial circuits. It is the equivalent of simplifying a Boolean equation.

Socrates then uses a form of logic minimization called weak division to create a multilevel network. In weak division, an algorithm examines the Boolean expressions in a design and eliminates redundancies. The synthesize tool then transforms the Boolean expressions into gates, and uses a rule base—an expert-system gate-level circuit optimizer—to get the most efficient netlist.

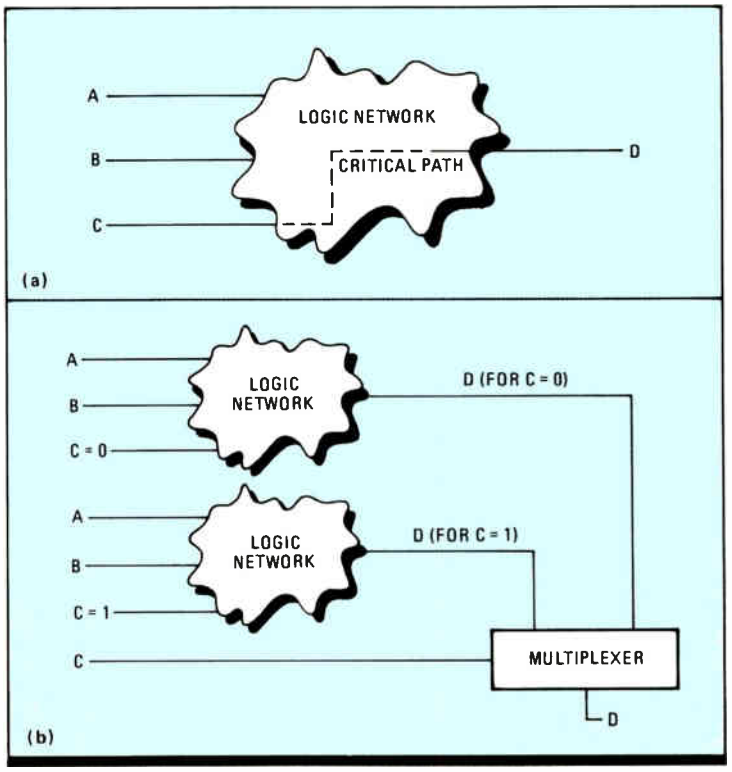
Another tool that uses an expert-systems approach to silicon compiling is the Logic Array Design System, from S-MOS Systems Inc., in San Jose. "This tool checks the electrical and schematic syntax of the design," says John Conover, director of engineering at S-MOS. "It examines the context in which a gate is used in a given design and determines if the gate has been used properly. If not, it generates an error message."

In contrast to present-day algorithmic techniques, Silicon Compilers' heuristic intelligent compiler promises to provide more complete and automatic optimization of multiple variables than has heretofore been possible. "Software tools such as Socrates allow the designer to select two variable design goals—speed and area—and tell the optimizer that, for example, speed is more important than area, but try to keep the area down to a minimum, too," says Philip Kaufman, chairman and chief executive officer of Silicon Compilers Systems. But, notes Johannsen, "Intelligent compilation will optimize the design for functional, performance, and physical layout constraints set by the designer." To optimize the function of an adder, for example, the designer can specify the circuit in terms of logic gates (see fig. 3a) or a higher-level macro cell. In either event, the system produces an optimized circuit (see fig. 3b).

For physical optimization, the compilation system places transistors and interconnections to attain the area or aspect ratio specified by the designer. In physical optimization, cells on a critical path will tend to be spaced closer together and cells not on a critical path will tend to be spaced farther apart. The physical optimizer minimizes the size of noncritical transistors. If a transistor is not on the critical path, there is no need to make it large or powerful.

Performance optimization is based on critical-path analysis. The compiler determines the actual circuit values: the resistance, capacitance, and size of transistors. Then it alters components to best meet the speed constraints but have minimal impact on area and power consumption. "For example, there may be 10 cells on a critical path," says Johannsen. "To speed up the path, you could change the size of the transistors in any of the cells, but some of those might be constraining the height of the block, so the compiler might change the size of other cells in the path to affect the performance." The compiler also knows how much capacitance and loading are required in interconnections.

Another tool the performance optimizer uses is a procrastination algorithm. An example involving a logic network with three inputs, A, B, and C (see fig. 4a), shows how the procrastination algorithm works. Of the three inputs, C is an input to a critical path through the network to an output D. To increase the signal speed through the critical path, the algorithm replicates the logic network and computes the outputs when the C input to one network is a 1, and when it is a 0 in the duplicate network, for any input values of A and B (see fig. 4b). Thus the algorithm predicts the output of the network for both possible states of C before C actually occurs. When it does, it is applied to a multiplexer that chooses the correct result from the two that



4. ENDING DELAYS. The procrastination algorithm predicts the two possible states of C before C occurs. This information can be used to speed up the critical path C takes within the logic network.

were computed. This eliminates the delays that C would encounter if it traversed the large number of gates within the logic network, and the critical path is speeded accordingly. The result is that C experiences only one gate delay: through the multiplexer.

Besides tools that automatically optimize a design's function, performance, and physical size, there are new tools that add more automation to the placement and routing of compiled designs. Typical of the new generation of place-and-route tools is the ChipCompiler from VLSI Technology Inc. (See p. 61).

The VLSI Technology compiler is an automatic chip-assembly tool that, interacting with the designer, places and automatically routes standard cells and multiple arbitrary macro cells. Unlike most other block-routing systems, the chip compiler places few constraints on macro cell blocks.

Block connectors can be on any side of the block—other tools restrict which sides of a block can contain I/O connections. With the VLSI Technology tool, these can be on any layer of the block and do not have to be on any fixed routing pitch layer. Finally, there are no restrictions on block connector widths, since nets may be routed with different widths.

"A major advance of the ChipCompiler is that it is the first tool that allows the designer to give it routing guidance," says Daniel Skilken, software product manager at VLSI Technology. "When dealing with power and clock signals, for example, the designer can guide the tool as to where generally on the chip these lines should be routed, how wide to make the power lines, how short to make signal lines, etc."

Another type of input is an instruction to group certain sets of standard cells because of timing considerations or some other functional criterion. Normally, the tool treats standard cells as individually movable and attempts to place them in the layout to facilitate routing.

PLACING BLOCKS OF ARBITRARY SIZE

Though most purveyors of place-and-route tools call the tools automatic, no one has devised a good solution for placing blocks of arbitrary sizes. The Place and Route product with Macrocell option from SDA Systems Inc. of San Jose, Calif., is one of the few with some automatic placement capability for such blocks. The software uses four algorithms to determine the placement of blocks.

First, a program using force-directed techniques places the blocks relative to one another, based on the amount of interconnect and the length of the nets running between the two. Force direction refers to the method that determines block placement. For example, a large number of pins would imply a large force. Fewer connections would indicate much less force. The algorithm looks at the forces between blocks and determines how to place the blocks and route the connections between them.

A second program spreads the blocks apart to accommodate routing. A third orients the blocks—rotates or mirrors individual blocks—to improve connectivity, and a fourth moves the blocks in the circuit plane, maximizing connectivity.

Another competitor entering the place-and-route tool market is Calma Co. The Milpitas, Calif., company's Block Interconnect System (BIS) provides users of GDS II (Graphics Design System) with a feature for automatically connecting IC structures while maintaining full user interaction for critical placement and routing. Unlike other routing systems that require data translation, the BIS router uses information directly from the GDS II data base.

With BIS, the designer uses another Calma tool called CustomPlus to build blocks, place them, and perform any special routing, such as defining and placing power and bus lines. In addition, blocks may be any arbitrary closed rectilinear shape with terminals at any point. Once critical paths are routed, the designer initiates the BIS tool, which actually routes the blocks.

Place-and-route tools in turnkey silicon-compiler systems differ from those just described in that they do not perform combined standard-cell and macro-cell placement. Rather, the tool places and routes larger macro cells alone. The glue logic typically contained in standard cells is collected into a larger macro cell. □

THE FIRST GaAs COMPILER IS ALREADY PRODUCING CHIPS

Seattle Silicon and Gigabit Logic team up to produce a compiler that can handle different logic types and can migrate to smaller-geometry processes in the future

by Jonah McLeod

Designing complex gallium arsenide integrated circuits is bound to get easier now that Seattle Silicon Corp. and Gigabit Logic Inc. have teamed up to develop the first GaAs logic compiler. The new tool is likely to boost acceptance of GaAs among the designers of application-specific ICs.

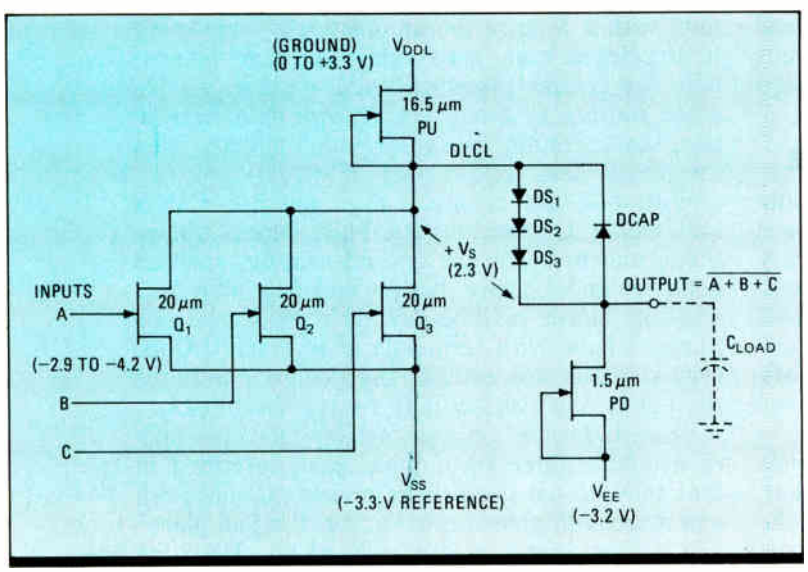
The GaAs Compiler meets the special needs of CDFL (capacitive diode FET logic), the form of transistor logic used with Gigabit Logic's GaAs process. But it can be easily converted from CDFL to whatever new logic becomes available, such as high-electron-mobility transistors. In addition, the compiler can migrate to smaller-geometry GaAs processes as they become available. Seattle Silicon and Gigabit Logic have demonstrated the compiler's capabilities by designing a high-speed 4-bit arithmetic logic unit.

The compiler was a natural pooling of resources: Seattle Silicon of Bellevue, Wash., is a fast-growing player in the silicon-compiler arena; Gigabit Logic of Newbury Park, Calif., is a foundry specializing in GaAs circuits. Gigabit Logic's GaAs process uses CDFL transistor technology (see fig. 1).

CDFL circuits comprise Schottky diodes and depletion-mode metal-semiconductor field-effect transistors (D-MES FETs). The dc characteristics of GaAs Schottky diodes (DS_1, DS_2, and DS_3 in Fig. 1) are similar to those of silicon p-n diodes, with typical forward voltage drops of about 0.8 V at typical current densities, but their useable frequency range extends beyond 500 GHz. The single-gate MES FET (Q_1, Q_2, and Q_3 in fig. 1) is a Schottky depletion-mode n-channel junction FET with a nominal pinchoff voltage equal to –1 V and dc characteristics similar to a silicon n-channel JFET.

Each CDFL circuit also employs n+ implant resistors and gateless MES FETs, referred to as saturation resistors (PU and PD of fig. 1), for current limiting. Reverse-biased large diodes (DCAP in fig. 1) acting as capacitors are used to handle the charging and discharging of circuit loading and for power-supply decoupling.

"CDFL offers the best speed-power point for GaAs," says Michael Pawlik, director of application-specific IC products at Gigabit Logic in Newbury Park, Calif. But fashion-



1. LOGIC OF CHOICE. Gigabit Logic's GaAs process works with capacitive diode FET logic, which uses reverse-biased Schottky diode capacitors.

ing a compiler that handles CDFL takes considerable attention to the heuristics, which is the art of incorporating the knowledge that skilled GaAs IC designers have accumulated by trial and error. "A GaAs compiler requires special heuristics to handle the layout of CDFL circuits to preserve this speed-power performance point," Pawlik says.

One example of heuristic knowledge in the GaAs Compiler is the way it handles the GaAs characteristic of different dc levels for the output and input, says Richard Oettel, chief scientist at Seattle Silicon. "So the compiler performing the layout has to insert, between the output of one gate and input to the next, a level-shifting network [in fig. 1, the diode series, DS_1, DS_2, and DS_3, and reverse-biased Schottky diode DCAP] and a pull-down transistor [PD in fig. 1] going to V_{ee}."

In designing this network, "the compiler not only has to determine how many inputs to each gate, but what size of Schottky diode to use, and how much fanout there is," says Oettel. The current capacity and breakdown voltage of the Schottky diode must be precisely established to preserve the speed characteristic of CDFL logic. "GaAs has entirely different loading and fanout requirements than CMOS or other process technology," Oettel says. The GaAs Compiler determines such parameters as the size of the Schottky diode, where to place the diode shifting network, where to place the actual gates, and where to route power, ground, and V_{ee}. "In designing the compiler, Dick [Oettel] added the heuristics needed to handle these layout requirements," Pawlik explains.

HEMT COMPILER COMING

Another design goal for the GaAs Compiler was accommodation of the rapidly evolving GaAs technology. The current compiler has built-in heuristics to handle the particular layout requirements for depletion-mode MES FETs. Future versions of the compiler will contain the heuristics for HEMTs and other transistor logic that may emerge.

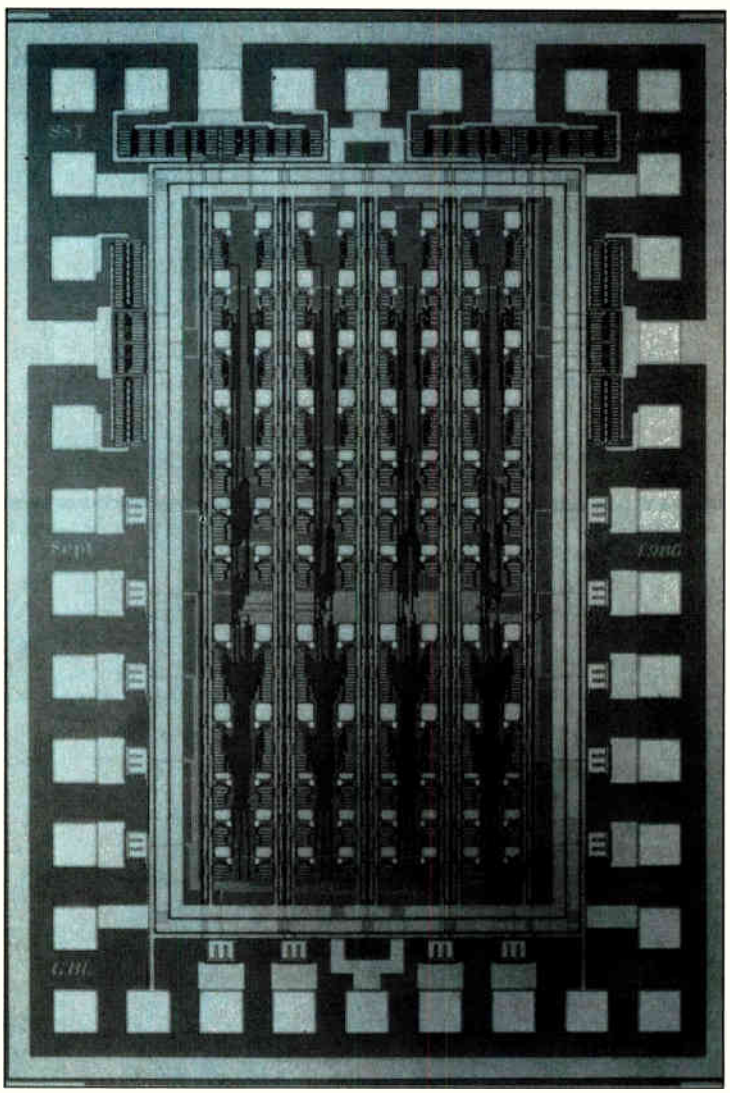
To accommodate different process technologies and different foundry requirements, the GaAs Compiler is organized in two files, a technology file and a design-rule file.

The technology file specifies what the compiler must provide to generate the various levels of a given process. CMOS, for example, has a rather homogeneous set of process rules; hence one file can contain the rules for building the mask layers of most commercially available CMOS processes. GaAs, on the other hand, is not homogeneous, and there are different process rules for building GaAs. So each different set of GaAs process rules is in a separate file in the GaAs Compiler.

"Our compiler is unique in that it uses the actual design rules for a process technology in performing its layout," says Oettel. There is a different design rule file for every foundry since each has its own set based on its requirements. For example, some foundries use the same polysilicon width as a minimum line width for the gate. Other foundries may require a larger polysilicon width for the minimum line width of the gate than for the minimum line width of the interconnect. The compiler applies the rule appropriate to the process it is compiling.

"The GaAs Compiler is reading the same specification data that a process engineer in the silicon foundry is reading," says Oettel. Having all the foundry's design rules means that the compiler is producing the optimum layout for each process. These rules are also used by yet another part of the compiler to compact the layout when the process rules shift to smaller geometries. Successively smaller line widths do not scale downward linearly, but Seattle Silicon has developed a method called dynamic compaction to account for this. The dynamic compaction method of adjusting the layout to match individual process rules differs from the way other silicon compiler manufacturers do so.

The conventional approach defines each com-



2. SPEEDY ALU. To demonstrate their GaAs Compiler, Seattle Silicon and Gigabit Logic created a 4-bit ALU that operates at 1.3 GHz.

ponent for a given process as a leaf cell, which are the basic elements a compiler uses to lay out a circuit. The conventional compiler performs a linear shrink of the individual leaf cells. Then it examines the cell and the process rules to determine where in the cell it can make additional nonlinear shrinks to achieve a more compact cell area. Not only does this take longer to adapt the process than does dynamic compaction, it also fails to give the optimum shrink of the cell. In addition, for each foundry the compiler has a file containing all the leaf cells for a given process. Each leaf cell would have been linearly shrunk and then optimized by a compiler program.

A high-speed 4-bit ALU created with the GaAs Compiler boasts a layout that is as good as one done by hand and 50% more area-efficient than possible in a gate array

When the GaAs Compiler lays out a circuit using dynamic compaction, it builds the circuit on a grid that it can change. "In our system there are a set of landmarks," says Oettel. "The distances between landmarks are set by design rules. In this methodology, the compiler, using the schematic of the circuit to be built, lays out the circuit in the most efficient way possible. When the compiler completes the initial layout, it lines it up with the grid." The grid lines are labels, X_0, X_1, ... X_n on the X axis and likewise Y_0, Y_1, ... Y_n in the Y axis. Because the compiler uses a dynamically changeable grid, it can space a design according to a mathematical formula: "$X_2 = X_1$ + (loading rule)." The area surrounding X_2 may be adjusted by the amount of the loading rule. The compiler accepts the loading rule and adjusts the size to accommodate the rule for the process in which it is operating.

To demonstrate their new GaAs Compiler, Seattle Silicon and Gigabit Logic created a high-speed 4-bit ALU (see fig. 2). "The resulting layout of the 4-bit ALU is comparable [in terms of area efficiency] to hand layout and is approximately 50% better than if the design were implemented as a gate array," Oettel says. The compiled design is also four times faster than the GaAs gate-array version and consumes 30% less power.

The GaAs ALU that the compiler produced for Gigabit Logic will be introduced April 30 as a member of the company's PicoLogic family of standard products. The 10G181, as it will be called, will operate at 1.3 GHz, three times faster than the equivalent 10K or 100K ECL version of the part, but will require only two thirds the power.

The number of items in the GaAs Compiler's library is small, with a transistor being the most complex item yet defined. But this is adequate to handle typical GaAs designs, which average around 1,000 gates, maintains Oettel. In contrast, a typical silicon compiler might have 25 categories of components and include complex items such as multipliers, adders, data paths, etc. Of course, the number and complexity of elements in the GaAs Compiler's library will increase over time as new elements are added.

With the advent of a GaAs compiler, designers who were fearful of undertaking a GaAs design now have a computer program that masks the complexity of the process. Moreover, they can be assured that the resulting layout will be in transistor logic appropriate for the foundry to be used. In addition, the layout will be as efficient as a circuit laid out by hand. Finally, the GaAs compiler is designed to be adapted to future GaAs process technology or design technology. □

For more information, circle 481 on the reader service card.

COOPERATION PAYS OFF FOR SEATTLE SILICON AND GIGABIT LOGIC

The first GaAs compiler took shape in an experiment that Seattle Silicon Corp. and Gigabit Logic Inc. carried out at the Washington Technology Center in Seattle—and both companies think that their cooperation paid off handsomely.

"Our GaAs compiler is the first instance of compiler methods applied to GaAs material," says Richard Oettel, who is the chief scientist at Seattle Silicon in Bellevue, Wash. "We started it to see whether compiler techniques made sense for GaAs materials, devices, and circuits. The fact that we built the compiler says something about our ability to make tools for processes other than CMOS and n-MOS."

Gigabit Logic is also pleased with the outcome. "The fact that there is a GaAs compiler means that now designers interested in Gigabit's technology can create designs that are correct without requiring the engineering support we previously had to provide," says Michael Pawlik, director of ASIC products at Gigabit Logic in Newbury Park, Calif. As Oettel explains it, "Gigabit doesn't have to do with every customer what they did with me—describe the technology and all the functions a designer can and cannot do. All of that explanation has already been built into the compiler."

PROUD FATHERS. Gigabit Logic's Michael Pawlik (left) and Seattle Silicon's Richard Oettel created the first GaAs compiler.

The Washington Technology Center was the fertile ground where these two companies came together to develop the compiler. Gordon Kuenster, a founder of Seattle Silicon, is also a founder of the center, which is at the University of Washington. It is a creation of the Washington legislature intended to promote technology development in the state.

NOW DESIGNERS CAN SKIP FLOOR-PLANNING DETAILS

One task in the back end of integrated circuit design that has resisted full automation is the placement and routing, or floor planning, of macro cells and standard cells. With existing floor planners, the designer must do many details that he could more efficiently leave for a computer to handle. He has to partition standard cells into clusters and convert each cluster into a macro cell, which the floor planner then places with other macro cells in the design.

If the designer wants to improve the timing of a critical path, for example, he must add weights to the line representing that path, forcing the place-and-route tool to give it priority in routing. He must hand-route power and ground lines in order to maintain control of their routing. Finally, to add the pad ring—the connections between the die and the leads in the package—the designer must call up a ring from a library and ensure it has the appropriate pads for the chip.

Now, however, a new floor-planning tool from VLSI Technology Inc. of San Jose, Calif., relieves the designer of these chores. The tool, called ChipCompiler, can handle both a macro-cell block for a full-custom layout and a standard-cell netlist implementation.

In addition, the designer can give guidance about the layout, and the ChipCompiler automatically does the rest. In terms of placement, for example, the designer can indicate areas that are to contain standard cells—without converting a cluster of cells into a macro cell of a particular aspect ratio to fit into the area. With this feature, a designer can completely change a floor plan in a matter of minutes or hours.

The designer can also give the tool guidance on routing. He can draw a set of lines on the layout, roughly outlining where power and ground should go, and the tool automatically and correctly routes the design to fit the guideline.

THREE-LEVEL DESIGN HIERARCHY

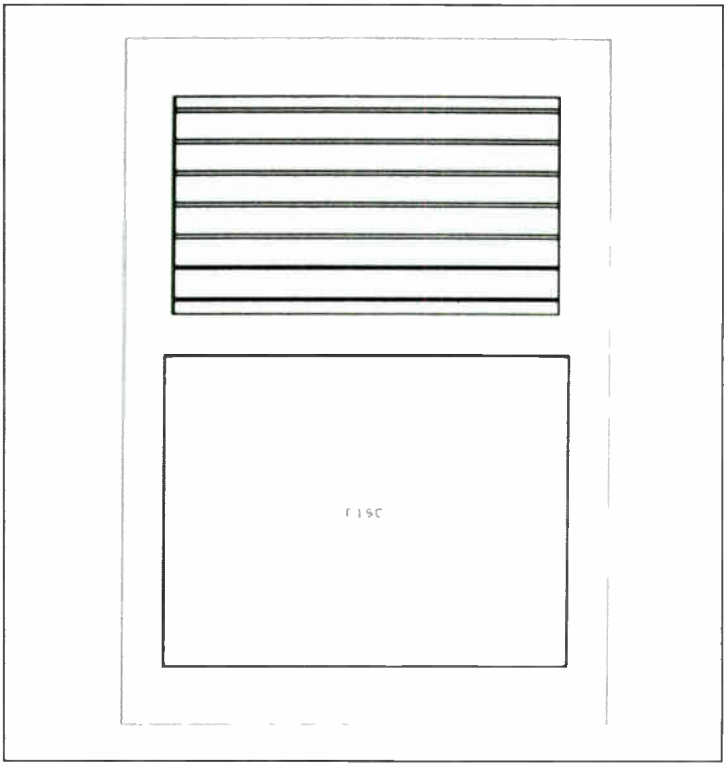
The capability for placing and routing individual standard cells and macro cells derives from the tool's ability to comprehend three levels of design hierarchy. At the lowest level are standard cells, represented as a netlist. At the next level, the software tool sees macro cells and standard cells clustered together as macro cells. At the highest level, the tool treats all macro cells as a single block surrounded by a pad ring.

An example involving a 16-bit microcontroller chip helps to illustrate the power of the ChipCompiler. This microcontroller includes a compiled datapath and a state machine for controlling datapath operation. Both were created with the company's newest compiler tools [*Electronics*, Feb. 5, 1987, p. 62]. Both could have been implemented as full-custom macro cells, but the designer chose to implement the state machine as a collection of standard cells and the datapath as a full-custom macro cell.

In this example, the layout the ChipCompiler produces is a rectangular chip (see fig. 1). The designer wishes to change the layout in order to achieve a smaller die size—a typical task at the floor-planning stage of designing an integrated circuit, as reducing the die size increases yields and cuts costs. One way to reduce the die size is to convert the large block of standard cells into smaller, rectangular-shaped cells surrounding the larger custom macro cell on three sides.

With other place-and-route tools, to change the one large block of standard cells would require returning to the schematic-capture tool, partitioning the standard cells into three separate blocks, creating a macro cell out of each block, and then returning to the floor-planning tool. Depending on the number of cells involved, the iterations could take hours or days to complete.

With the new tool, the designer changes the layout simply by drawing three rectangular blocks in place of the one large block originally created: two vertical areas and the original horizontal area (see fig. 2). "The designer creates these areas without having to know if they are



1. FLOOR PLAN REDUCTION. By giving the floor planner guidance on how it should route the power net, a designer can significantly reduce die size.

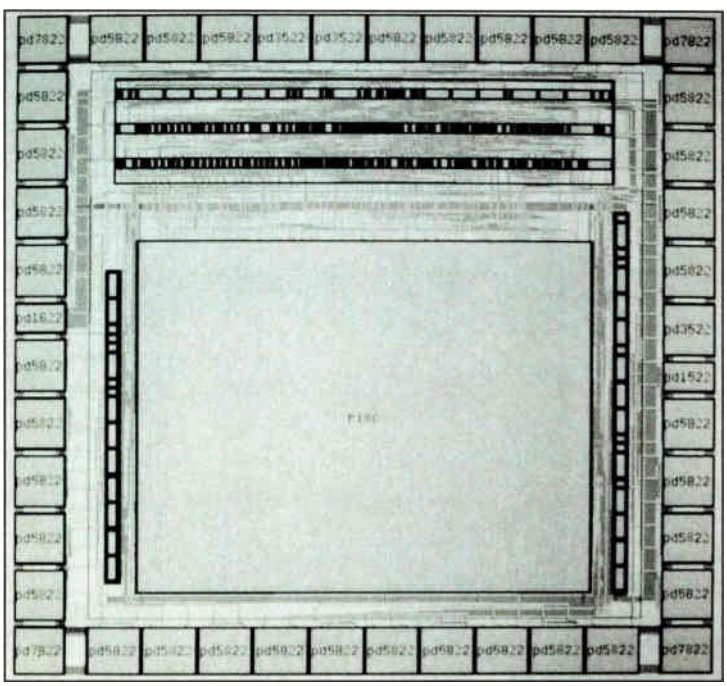
the right size or not," says Mark Hartoog, manager of physical design software at the company. "In addition, the designer can freeze the two newly created vertical standard-cell areas, indicating to the software that he wants the two to be the same height as the compiled macro cell," Hartoog continues. Establishing the height of a standard-cell row is another example of guid-

VLSI Technology's ChipCompiler can do all the tasks needed to turn one large circuit block into three: all the designer need do is draw three rectangles in place of the one

ance. The floor planner automatically adjusts the unfrozen areas to be the right size after it determines how many standard cells can fit into the two frozen areas. It adjusts all three areas to match the total size needed to contain all the standard cells in the design.

In breaking up the single block into three smaller ones, the designer need not specify to the software which standard cells are assigned to each block. However, he can make seed placement in any given area to improve timing in a critical network or to achieve other design goals. The floor planner knows what cells are contained in the netlist and the amount of area required to place and route the standard cells in each of the three areas assigned. It places standard cells into each designated area in such a way as to minimize total wiring between blocks.

Once the designer is content with the placement, he directs the tool to route the standard cells inside the individual blocks. The floor planner is now working at the lowest level in the design hierarchy, placing and routing standard cells. When the software completes this routing, the designer is ready to route the larger macro cells at the second level.



2. DIVIDE AND CONQUER. ChipCompiler quickly divides a large macro cell containing standard cells into smaller blocks of standard cells.

Before routing the larger block, the floor planner's analysis tools show the designer any routing congestion within the current floor plan. He sees a "rat's nest" view of the wiring between blocks. At this point, he can rotate or move blocks around to improve the routing.

Once satisfied with the block placement, the designer can route the blocks with default power routing. In wiring the blocks, the ChipCompiler first shows the designer the channel structure of the arbitrary blocks and in which order it will route them. The floor planner starts routing the innermost channels and works outward so that it can move blocks apart to accommodate routing.

"After each channel is routed, the floor planner adjusts the block positions to keep from wasting space or causing routing failures caused by too many wires trying to run through too narrow a routing channel," says Hartoog. "Routing channels are not required to be rectangular. They can be any rectilinear shape. After the router finishes wiring, it compacts the channel wherever possible by removing extraneous bends, jogs, and vias."

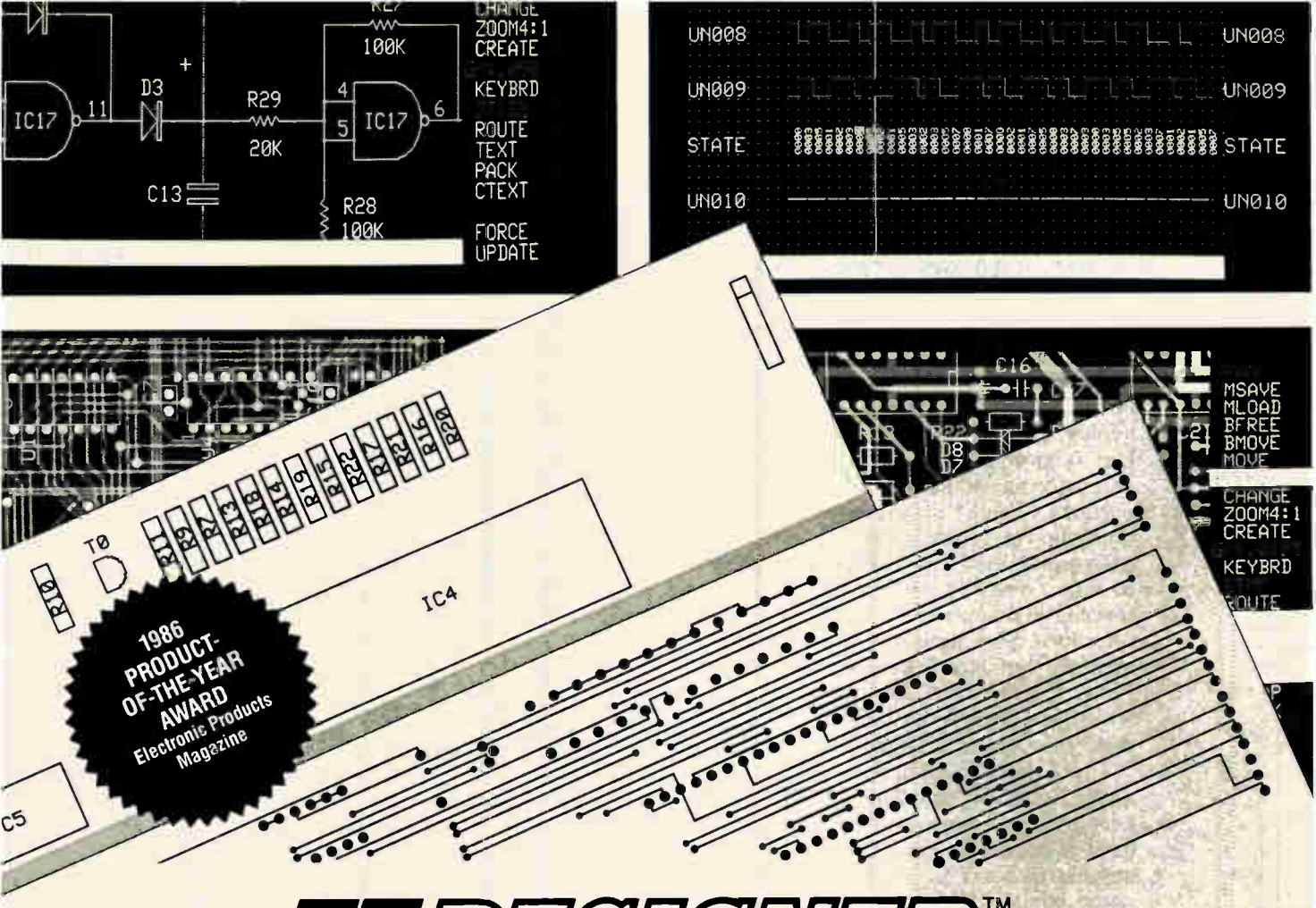
On this first layout iteration, the ChipCompiler floor planner produces a chip measuring 179 by 178 mils. To reduce die size even further, the designer reroutes the design and gives the floor planner guidance on power and ground routing. To do so, he first selects the positive supply voltage, or V_{dd}, net; the system highlights all the V_{dd} connectors on each block in the layout.

The standard-cell areas generally have V_{dd} connectors at both ends of the standard-cell rows. "The designer may choose to connect V_{dd} at only one end of the row of standard cells, to prevent the supply voltage from circulating around the pad ring," says Daniel Skilken, software product manager. Routing power through the pad ring has the effect of increasing die size.

To guide the routing of the power net, the designer draws lines between power connectors on the various blocks to indicate the general area for the power lines. "The segments do not need to be connected directly to the V_{dd} connectors; the designer merely indicates the vicinity of the connector, and the system creates the exact wiring for him," says Hartoog. "He can also specify the width of the power bus."

The new layout produces a chip measuring 169 by 168 mils—a reduction of 10 mils off each side of the original chip layout for a total savings of 100 mil^2. "This reduction would significantly reduce the price of the chip," says Skilken. "It could also make a difference in the kind of package the designer can use. Certain die sizes require larger cavities." *–Jonah McLeod*

For more information, circle 482 on the reader service card.



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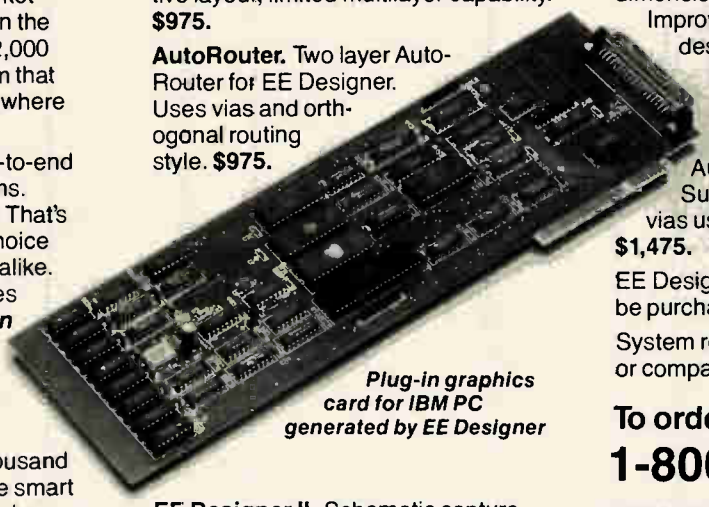

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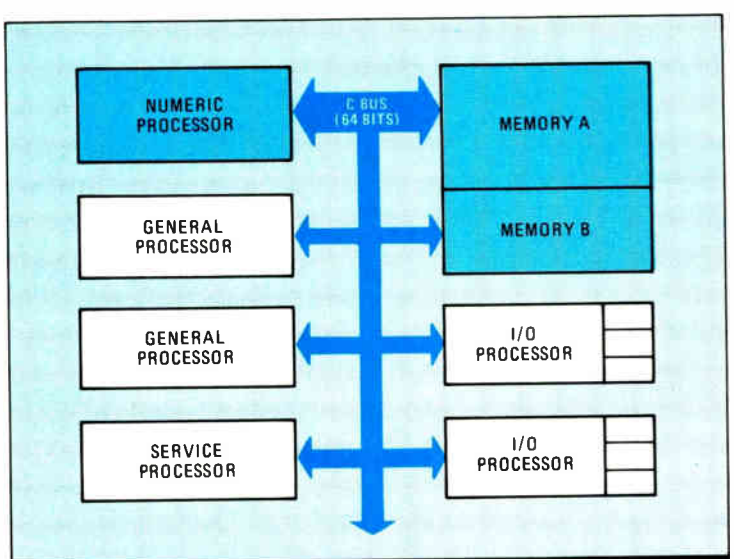
THIS NEW DESIGN OUTRUNS VECTORIZING MINISUPERS

Vector-processing minisupercomputers face a challenge from a new kid on the block who has a different method of crunching numbers. Cydrome Inc. claims that its modified data-flow architecture avoids the major roadblock for vector processing: some code can never be vectorized. So overall performance, as a result, is degraded because portions of most programs must be executed at much-slower scalar speeds.

Cydrome says that its Cydra 5 achieves three to four times the sustained performance of vectorizing minisupers that have the same peak performance. The figures are based on tests with an early version of the machine running 24 Lawrence Livermore Laboratory Loops kernels, which are regarded as giving the best measurement of performance across an entire workload.

The Cydrome designers took what is good about data-flow parallel-computer architecture—keeping all processing resources busy as long as data is available and thus doing a maximum amount of work in parallel. But they also eliminated what is bad—the overhead that the data-flow machine generates in sensing when data is available for operations—by moving the complex scheduling to a very intelligent compiler instead of building it into the hardware.

To make the Cydra 5 a fast mathematical processor as well as a good general-purpose machine, the engineers designed a special numeric processor and built in a provision for multiple processors (see figure). Since the most efficient use of all processors in this design requires that data be shifted among the processors, the designers built a wide and fast system bus—64 bits wide and rated at 100 Mbytes/s.



DUAL MEMORIES. The Cydra 5 is designed with dual memories, one serving a numeric processor and the other serving general-purpose processors

The Cydrome engineers opted for two kinds of system memory for balanced performance. One of the memories is set up for rapid parallel access to deliver numbers to the numeric processors in high volume, while a second memory, structured for serial access, serves the general-purpose processors.

Cydrome will demonstrate the Cydra 5 at the Second International Conference on Supercomputing May 3 to 8 in Santa Clara, Calif. When the machine is introduced this summer, it is expected to have a price tag of from $600,000 to $900,000 for a fully configured system. Cydrome will market the machine itself and through an OEM arrangement with Prime Computer Inc., which has a 10% stake in the Milpitas, Calif. startup.

MORE HORSEPOWER

The Cydra 5 is intended to serve users who now have a general-purpose processor, such as a Digital Equipment Corp. VAX, but who want more horsepower for structural analysis, simulation, computer-aided engineering and design, and other computationally intensive tasks. Because it does not require code to be vectorized, it may run sequential algorithms essentially unchanged, merely recompiled.

By contrast, says B. Ramakrishna Rau, Cydrome's chief technical officer and the designer of the Cydra 5, vectorizing superminis are best for would-be supercomputer users who want to run existing supercomputer code without paying supercomputer prices. Other users, he adds, will require an 8-to-10-fold performance improvement to justify the cost of vectorizing.

Data-flow architecture takes advantage of inherent parallelism in a program—independent operations that can be done at the same time—explains Rau. An operation may be performed whenever all inputs are available and a processor is available. Thus a data-flow processor can tolerate nonlinear recurrences, where the result of one operation is fed back into another—which can derail a vector machine by forcing every iteration in a matrix operation to wait for the recurrent value to be calculated.

Cydrome calls its architecture "data-flow-like." A pure data-flow machine can quickly bog down in overhead, Rau explains. True data-flow hardware must sense when inputs to an operator are available. That requires tagging each input with an index number, and then performing two associative searches for every operation.

The Cydra machine makes these decisions in advance, at compile time instead of run time. The compiler will schedule operations so that data will automatically be assigned to an avail-

able operator. Such scheduling entails calculating an initiation interval for each instruction and then setting up a timing schedule so that the many iterations of the instruction can be interleaved. "Scheduling requires modification of code, but the change is not nearly so great as for vectorizing," Rau says.

Floating-point operations in the Cydra 5 are handled by a special numeric processor, designed from standard emitter-coupled-logic chips and some Motorola gate arrays. Where most vectorizing minisupers use floating-point processors to offload number crunching from master central processing units, the Cydra treats the numeric processor and one or more general processors as equal citizens. Up to a dozen processors, in any mix, can be plugged into the system bus. Initially, the Cydra will have only one numeric processor, but it is designed for multiple units.

Programs run on the numeric processors generate requests to the general processor, a 16-MHz Motorola 68020, for input/output operations and other operating system services. Tasks are assigned via a "ready-to-run" queue in the general processor, through which the processors self-schedule.

Except for a direct memory-access path for the numeric processor, all internal communication in the Cydra 5 is handled by a 64-bit bus built from standard TTL chips and rated at a theoretical peak of 100 Mbytes/s. (Typical actual performance is 50 Mbytes/s, says Rau. The maximum actually achieved has been 80 Mbytes/s.)

System memory, a service processor (a Motorola 68000 that controls the system console), and an I/O processor also communicate via this bus. The I/O processor in turn can control up to three VMEbus interfaces, and all peripherals and outside communications links are controlled via the VMEbuses. "We picked VMEbus because it is the fastest standard industry bus," Rau says.

System memory is organized as two types; physically, they are the same kind of n-MOS 1-Mbit dynamic random-access memories, but are accessed differently by the different processors. Each memory can hold both instructions and data. Memory A is interleaved so that it can be accessed in parallel by the numeric processor over a 200-Mbyte/s bus; it is optimized for short access time, Rau says. Memory B is accessed serially over the system bus by the general processor, which can sustain longer access times but needs a larger bandwidth. This processor can also access Memory A over the system bus. The Cydra supports up to 256 Mbytes of Memory A, added in 16-Mbyte increments, and either 8, 16, or 32 Mbytes of Memory B.

The numeric processor includes a 32-Kbyte instruction cache, but no data cache. Rau says that the data cachese—which are commonly thought to be valuable because they hold in fast static random-access memory the small subset of data that a program will commonly require at a given time—can actually degrade performance. A nu-

HOW CYDROME'S DATA-FLOW ARCHITECTURE DOES IT

A good example of how data-flow architecture can outrun a vector-processing machine is Fortran Do loops, which are the most compute-intensive portions of floating-point operations. The figure implements the instruction

DO 10 I = 1,1000

for the expressions

G(I) = (A(I) + B(I)) * (C(I) + D(I))

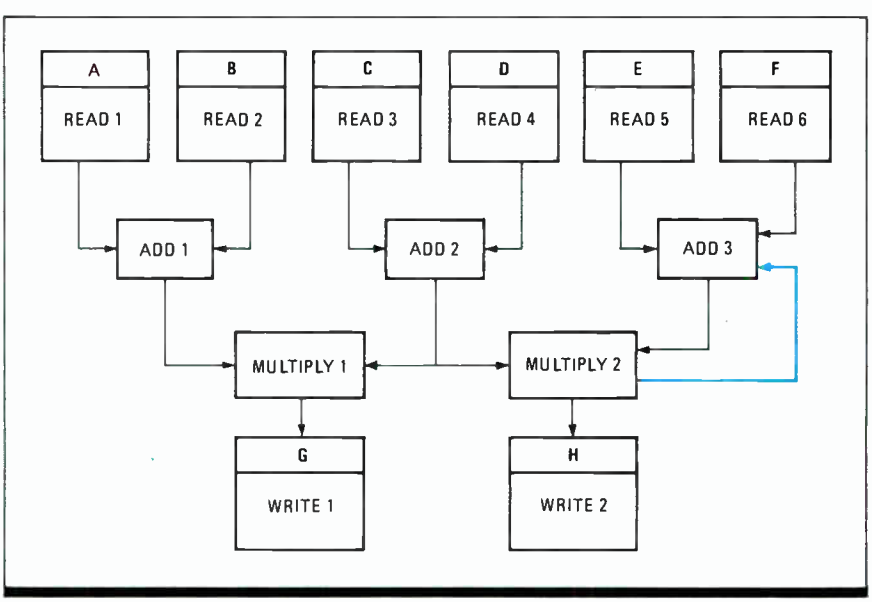
H(I) = (C(I) + D(I)) * (E(I) + F(I))

where

F(I) = H(I-1)

A data-flow machine can perform as many of these adds and multiplys in parallel as it has hardware for, as soon as the data representing the inputs is present. By contrast, a vectorizing processor would first read in all the data and then perform all iterations of the Add1, all of the Add2, all of the Add3, and so on. Therefore, because this expression has a recursion, with the results of Multiply2 becoming an input to Multiply3, it cannot be vectorized. Each iteration of Read6 will have to be calculated separately.

A simple data-flow machine might typically offer a 3 : 1 improvement in performance over a serial execution of this expression, says Cydrome chief technical officer B. R. Rau. A serial machine, such as a vector unit, will have to perform 6 reads, 3 adds, 2 multiplies, and 2 writes per iteration. For reads taking 5 cycles, writes 1 cycle, adds 2 cycles, and multiplies 3 cycles, each iteration will require 44 cycles. Even if the data-flow machine can only handle one memory access, one add, and one multiply per cycle, it can perform this iteration in 16 cycles.



TWO WAYS. A data-flow machine does these operations in parallel; a vector processor works serially.

merical processor works on large arrays of data, Rau notes. If the cache is one word too small, so that the first word of each iteration keeps getting pushed back into main memory, the cache can come up with a zero hit rate. The problem is even worse, Rau says, in multiprogramming environments when the cache may be looking at every fourth word; in such cases it has to switch four times as much memory in and out of the cache.

The 200-Mbyte/s memory bus is the price Cydrome paid for leaving out the data cache, Rau says. With no data being kept immediately accessible to it, the numeric processor needed a fast path and a fast access time to Memory A.

–Clifford Barney

For more information, circle 483 on the reader service card.

TECHNOLOGY TO WATCH

FAST CONTROL STORES CAN NOW USE EEPROMs

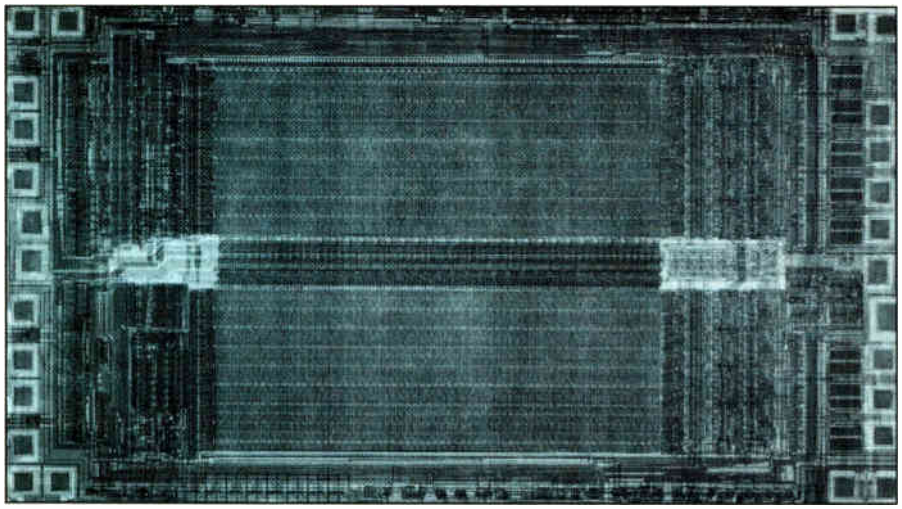
The race to fill the need for high-speed writable control memories traditionally has been run neck-and-neck between bipolar programmable read-only memories and CMOS static random-access memories combined with ultraviolet-erasable CMOS PROMs. But a new entry from Seeq Technology Inc. should cause these competitors to look over their shoulders. Coming up fast is Seeq's set of superfast but CMOS 16- and 32-Kbit electrically erasable PROMs with access times of 25 to 35 ns.

These access times for the 2-Kbit-by-8-bit 36C16 and the 4-Kbit-by-8-bit 36C32 (see fig. 1), which are 5-V, byte-writable, low-power CMOS EEPROMs, are equivalent to those times available with bipolar PROMs and faster than those available on current EPROMs and EEPROMs. The unprecedented high speed of these EEPROMs is achieved without sacrificing reliability and endurance, according to Radu Vancu, senior staff design engineer at the San Jose, Calif., company. What makes that possible is the use of a higher-performance scaled 1.25-μm n-well CMOS process and a variation of its traditional Q-cell in which a pair of EEPROM transistors is read out through separate sense amplifiers. Called the differential Q-cell, it incorporates a differential sense-amplification scheme and address-detection techniques borrowed from high-speed static RAMs.

Because of their combination of in-system reprogrammability and high speed, the two devices will open up new applications, says Gary Rauh, Seeq's strategic marketing manager. "For one thing, in high-speed nonvolatile memory systems requiring infrequent RAM rewrites, this 35-ns EEPROM can replace the combination of a high-speed static RAM and slower EEPROM at substantial savings. System design is also simplified, because the need for loading and unloading a large number of SRAMs is eliminated."

In addition, applications traditionally performed by bipolar PROM will gain more flexibility with these high-speed, nonvolatile alternatives, says Rauh. "Code conversion, for example, can now incorporate user-defined codes, and high-speed character generators can be customized to meet the specific requirements of the user's applications."

Until now, the only commonly available nonvolatile memories with access times of 35 ns or less have been bipolar fusible-link programmable ROMs such as those available from Advanced Micro Devices [*Electronics*, Feb. 10, 1986, p. 35]. Although they offer high speed, bipolar PROMs have limitations, most important of which is that they consume much more power than MOS devices, especially when compared with the many high-speed CMOS SRAM and EPROM circuits available. High-speed CMOS EPROMs with access times of 45 to 60 ns are pushing toward 35 ns.



1. FAST EEPROM. Seeq's 36C16 CMOS EEPROM has an access time of 25 to 35 ns.

Before the development of Seeq's high-speed differential Q-cell, the best available EEPROMs had access times of 50 to 55 ns, limiting them to relatively slow microprocessor applications or forcing the introduction of wait states into what would otherwise be faster systems. As a result, EEPROMs were ruled out for use as high-speed control store in such applications as control systems, graphics displays, array processing, and digital signal processing. Users who need high speed, nonvolatility, low power, and in-circuit reprogrammability have had to settle for a battery-backed 25- to 35-ns SRAM or a combination of

high-speed SRAM and somewhat slower 50- to 100-ns EEPROMs. In the latter approach, fast SRAMs are used for program execution, loaded from slower EEPROMs after power-on.

Seeq aims to eliminate this dilemma with the first two devices in its family of EEPROMs in the Jedec standard byte-wide 24-pin packages with the output drive characteristics of commonly available bipolar PROMs. Available in 300- and 600-mil dual inline packages, they are programmed with voltage programming pulse applied to one of the chip select inputs, because there is no enable input pin on this pinout. Individual bytes and the entire chip are reprogrammable at a rate of 5 ms/byte.

In addition to a 35-ns access time, the devices feature a chip-enable output time of 20 ns. The devices have external read and write cycles identical to most commonly available SRAMs, with high-speed address and data input latches incorporated to permit microprocessor-compatible write signals. These cycles make it easier for systems designers to incorporate the device into existing systems.

The most important factor in boosting the speed of the EEPROMs to the sub-35-ns range has been the shift to sense-and-detection circuit techniques more commonly associated with static RAMs. "Most EEPROMs use two transistors per bit—one to store data and one as a select transistor—and single-ended sensing, yielding high density memories," says Vancu. "But the down side is that access times are in the 200-ns range." Attempts have been made to use the technique in higher-speed designs by increasing the bit-cell current and reducing the word-line delay. "By using a large bit-cell transistor and additional decoding circuitry, EEPROMs with access times around 70 to 90 ns have emerged."

However, the basic limitation of such designs is the relatively poor performance of the single-ended amplification technique in noisy high-speed environments, because common-mode noise is not rejected. For these reasons, says Vancu, Seeq decided to use a differential bit-cell and sense-amplifier techniques borrowed from SRAM designs. Called the DQ cell, Seeq's differential bit cell (see fig. 2) is a variation of its proprietary Q-cell in which a pair of EEPROM transistors is read out through separate sense amplifiers, which are in turn combined into a NOR gate. The effect of this arrangement is that correct information will be read out as long as at least one of the two transistors is not defective. The only difference between the Q and DQ cells is that in the latter each half of the EEPROM pair contains the complement of the other half.

In a configuration similar to SRAM designs, a differential sense amplifier is shared by each half of the cell, one for the select transistor and one for the floating gate transistor, allowing rapid bit-cell-state detection at a low-input differential voltage. "Moreover, it is done in the presence of common mode noise on the bit lines as well as on the ground and supply voltage inputs."

To further improve bit-sensing time, input-edge-detection circuitry similar to that used in SRAMs was incorporated to generate internal voltage-equalization pulses, says Vancu. At 350 mW, the 36C16 and 36C32 consume less than half the power that a bipolar PROM of the same density needs, he says, which means they may be designed with smaller power supplies and less sophisticated cooling systems. Because they run cooler, they are also more reliable over the long run.

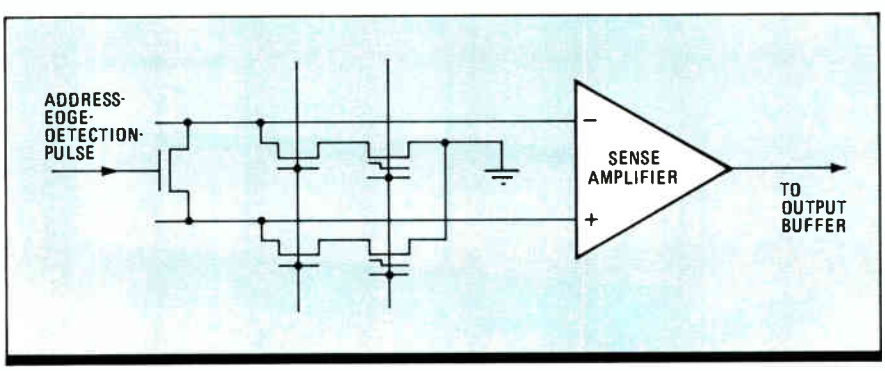
Seeq's 1.25-micron n-well CMOS process keeps power consumption at reasonable levels while squeezing as much speed as possible out of the new EEPROMs

In contrast to bipolar PROMs, Rauh says, the two devices can be completely tested before shipment because of their electrically erasable cells. The 36C16 and 36C32 also have the advantage of in-system reprogrammability. "Unlike bipolar PROMS, which must be scrapped and replaced with new devices when code changes are necessary, an EEPROM does not have to be replaced," Rauh says. "It is simply updated and reused."

To keep power consumption at reasonable levels while squeezing as much speed as possible out of the devices, a 1.25-μm n-well CMOS has been used. "However, this represented a considerable circuit-design challenge," Vancu says, "since an EEPROM requires a high voltage, 18 to 21 V, to write, and also must operate at high speed." To reconcile these two requirements, a substrate bias generator was incorporated: to keep the substrate at about –2 V, decreasing the bit-line capacitance and reducing signal delay; to enhance the characteristics of high voltage devices; and to improve latchup immunity.

–Bernard C. Cole

For more information, circle 484 on the reader service card.



2. RAPID DETECTION. A sense amplifier detects bit-cell states fast at low input voltage.

PYRAMID ADDS RISC TO PARALLEL PROCESSING

Pyramid Technology has taken a giant step forward on the performance curve by putting fast reduced-instruction-set processors into a tightly coupled, shared-memory multiprocessor architecture. Its two new systems, the 9830 and the 9840, extend the performance and improve the price/performance of the 9800 series—two models, the 9810 and 9820, were introduced in November. The Mountain View, Calif., company now sees this family of computers as its ticket into a commercial data-processing marketplace dominated by the likes of IBM Corp., broadening its current market base of technically oriented customers.

The new models offer mainframe power at minicomputer prices. As a result, they pack a price/performance wallop that will make them attractive platforms for large data base, transaction processing, and software-development applications in the commercial data-processing arena. "Users can go all the way from the classical upper end of the minicomputer marketplace well into the traditional mainframe marketplace with the 9830 at $424,000 and the 9840 at $514,000, which is half to a quarter of what they've traditionally paid for that performance, " says Dick Lussier, Pyramid's president and chief executive officer.

Pyramid engineers combined three performance-enhancing ideas—RISC, a floating-point coprocessor, and parallel processing—into one computer architecture. Then, by adding high-speed input/output capability with separate I/O controllers on the 40-Mbyte/s Xtend system bus, they kept the system in balance. In another balancing act, the designers made sure disk-file storage was more than adequate and set it up to be used as virtual disks. A built-in diagnostic and service processor ensures that all this capability can run smoothly without great expense.

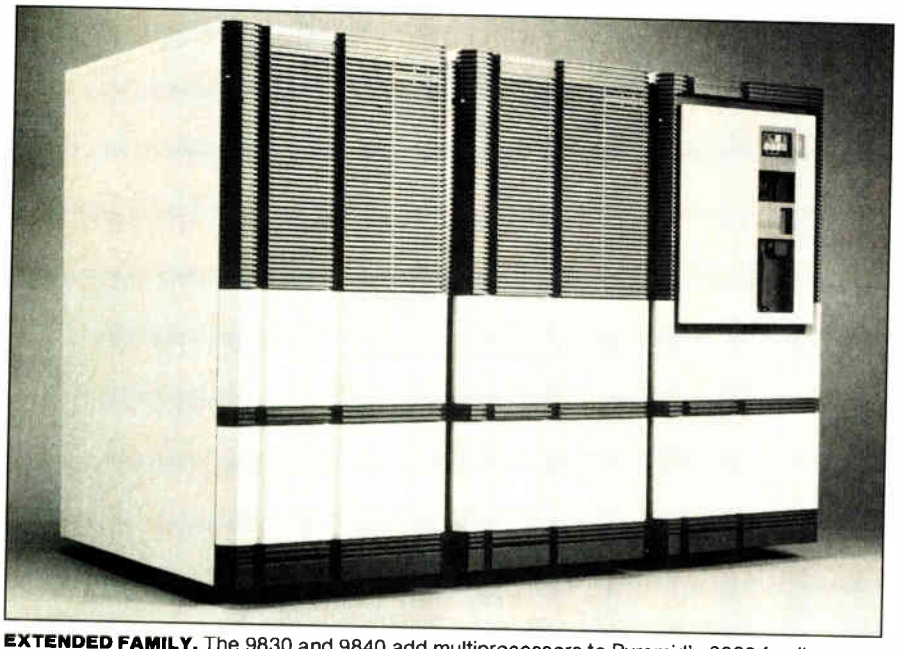
Performance specifications indicate the machines have power to spare. Equipped with four RISC central processing units tied together in a shared global-memory configuration, the 9840 can execute some 25 million instructions per second—better than twice the performance of a Digital Equipment Corp. 8800, according to Pyramid. The three-CPU configuration of the 9830 offers 19-mips computing.

The 32-bit RISC CPU at the heart of these systems features an instruction pipeline to allow most instructions to execute in a single 100-ns clock cycle. The CPU also features an unusually large number of registers—528. "We tried to make our processor do what computers do best, namely, use lots of register operations as well as minimize the bottleneck between processor and memory," says cofounder Robert Ragan-Kelley, Pyramid's director of advanced software development. "So our design is a hybrid between a register machine and a stack machine—it's easy to program, but it has all of the implementation advantages of registers."

Unlike many single-chip VLSI RISC implementations, Pyramid has included a 16-Kbyte instruction cache, a 64-Kbyte data cache, memory-management system, and floating-point coprocessor, all of which are so critical for system performance, onto each CPU board. For its successor computer systems due out in late 1988 or early 1989, Pyramid is developing a CMOS VLSI version of this RISC CPU, Lussier says.

The RISC CPUs communicate with main memory and with the system's I/O processors over Pyramid's proprietary Xtend bus design. A 32-bit bus, Xtend can transfer data at up to 40 Mbytes/s. Because the 9830 and 9840 use separate controllers to handle external input and output, the Xtend bus transfers only short messages between the CPUs and the controllers. This message-based design helps reduce bus activity and prevent I/O bottlenecks.

For communication with peripheral devices and the outside world, the 9830 and 9840 feature a high-capacity intelligent I/O subsystem. This subsystem combines a 5-mips AMD 29116 processor and 14 paral-



EXTENDED FAMILY. The 9830 and 9840 add multiprocessors to Pyramid's 9000 family.

lel direct-memory-access channels to provide a total throughput of 11 Mbytes/s. The I/O processor's disk controller can transfer data to and from disks at rates of up to 2.5 Mbytes/s. A separate tape/printer/Ethernet controller subsystem provides a high-speed tape interface, a printer interface, and an Ethernet controller. The 9830 and 9840 can also support a variety of other I/O controllers via its Multibus adaptor.

To handle storage requirements, the 9840 is equipped with 128 Mbytes of main memory and up to 29 gigabytes of disk space. All memory comes with error-correcting logic that corrects single-bit memory errors and detects double-bit errors. Virtual memory is byte-addressable and allows each processor to use up to 4 gigabytes of virtual address space. Also included is a virtual disk facility, a feature that helps manage the immense quantities of data that might be associated with large database applications. Where such databases are too big to store on a single physical disk, the virtual-disk facility allows several physical disk drives to be grouped together as a single logical disk.

To ensure smooth recovery from faults, each machine contains an internal diagnostic and service processor called the system support processor. This processor performs diagnostic and test functions, downloads microcode for the central and I/O processors, and handles the interface to the system operator through the system console. Most important, it hooks into a modem that allows service personnel to diagnose problems over the phone for quick repair.

–Alexander Wolfe

For more information, circle 485 on the reader service card.

TECHNOLOGY TO WATCH

PC AT-BASED TESTER CUTS COST OF MILITARY ATE

Summation Inc. had the hardware and TYX Corp. had the software needed to develop personal-computer-based test systems for military applications. So they got together and designed a new tester based on the IBM Personal Computer AT that, they say, meets all military requirements for automatic test equipment, including programming, documentation, and operation. The partners expect their Summation Atlas Test System to lower significantly the cost of such applications as testing power supplies and microprocessor boards at military repair depots.

"The new system can easily take the place of power-supply testers costing more than $700,000 per test stand. The replacement would cost about $110,000, including software, instruments, test stand, and computer," says John M. Thompson, ATE marketing manager of TYX. Software redevelopment costs would be modest, he adds, because the system can quickly recompile programs written in Atlas, the standard military ATE language.

Summation, of Kirkland, Wash., introduced its SigmaSeries family of PC-based test and management systems in 1985 for industrial applications; it now claims more than 100 customers (see p. 71). To build test stations, users plug instrument-on-a-card and signal-switching modules into an intelligent test frame that operates as a benchtop analog, digital or hybrid tester. In March, Summation upgraded the system with high-speed digital modules for testing complex components and board assemblies, both of which are used extensively in military equipment.

TYX, of Reston, Va., produces the Personal Atlas Work Station, or PAWS, a software development, documentation, and execution system that runs on PCs and minicomputers. PAWS is used in more than 30 major military ATE programs, TYX says. In the new system, PAWS is integrated with drivers and a switching data base for Summation's hardware so that it can compile and execute Atlas programs for the test stations. Options include an expert system designed to help programmers develop test strategies.

Each Atlas test system station (see fig. 1) contains a Motorola Inc. 68000 16-bit microprocessor system and a VMEbus for instrument-on-a-card modules, a configuration becoming popular in military ATE systems [*Electronics*, April 16, 1987, p. 57]. The 68000 executes programs and commands sent to it over an IEEE-488 bus by a PC AT. The PC can also operate conventional instruments via the same bus. As in conventional ATE systems, several modules and conventional instruments can operate on the bus; the optimum number depends on the complexity of the tests being run.

Up to 12 microprocessor-controllable instrument-on-a-card and switching modules plug into a station's test frame and up to 11 more modules plug into an expansion chassis. The modules are

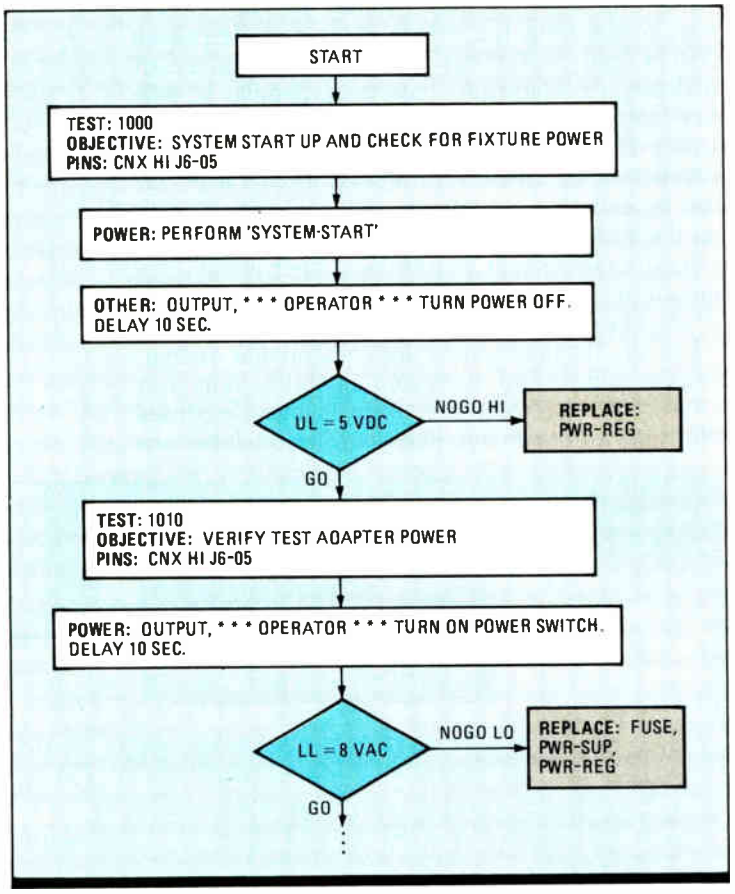
1. SMART TEST STATION. A microprocessor in the test station (left) executes test programs downloaded by a personal computer (right).

synchronized by a trigger bus and share a front panel with software-defined control keys and an 80-character electrofluorescent display. The station also has foot-control, bar-code-reader, printer, and RS-232-C ports.

Analog signals to 200 MHz can be switched into the modules, says Brian T. Laine, Summation's project manager, and signals to about 100 MHz can be transferred on buses in the test frame. For high-accuracy measurement of electrical parameters at frequencies to about 1 MHz, there are shielded analog buses with an offset of less than 1 μV.

Summation's new DSR10 digital stimulus and response module provides for high-speed functional testing of microprocessor boards and other complex components. It operates at test-data rates to 20 MHz with 100-MHz strobes and 10-ns timing resolution and can expand to hundreds of pins at that performance.

The DSR10 is partitioned into a controller module and memory modules. Each memory module provides 16 outputs, 16 inputs, and 16-kiloword input and output memories, using 16-bit words. A test station with an expansion chassis can have as many as 336 inputs and 336 outputs. Test patterns stored in the output memories can be varied with stored strobe-signal transitions and repeated a specified number of times (up to 65,536 times), or repeated indefinitely.



2. TEST DOCUMENTATION. Optional software translates Atlas programs into flow charts and other documentation and prints them out on a laser printer.

The PC version of PAWS runs under Venix System 5, a Unix-based, real-time operating system from Venturecom Inc., Cambridge, Mass. A menu-controlled system with more than 1.2 million lines of code written in the C language, PAWS evolved from an Atlas software system developed for the Air Force MATE (modular ATE) program in the 1970s by RLG Associates, a TYX predecessor.

"Atlas compilers are slow, and ours is no exception," Thompson says. However, he says, recent enhancements and Venix's speed enable a standard IBM PC AT to compile at a respectable work-station rate—592 lines per minute, compared with 600 lines per minute for Digital Equipment Corp.'s MicroVAX II, 662 lines for a Hewlett-Packard Co. HP 9000/500, and more than 1,000 lines for a VAX minicomputer.

FOUR KINDS OF CODE

The basic system compiles and edits programs written in the IEEE-716 C/Atlas subset, with other subsets optional. Besides generating object code in the Atlas intermediate language for test stations, the compiler can also generate code for conventional instruments in CIIL (Control Intermediate Interface Language, the MATE standard), instrument native code (ASCII strings), or HP's special routines.

Among the development tools is a windowing editor for development of test-program sets (TPSs). With it, test engineers can "cut and paste" existing programs to build TPSs. Up to six programs 65,000 lines long can be scrolled through six display windows and up to eight programs can be manipulated at one time. To speed debugging, a review editor displays programs and diagnostic messages in two windows and jumps from messages to the erroneous Atlas source code with a single keystroke.

The run-time system does double duty as an on-line development tool for executing code on the target test station during final debugging and as the software package that runs the tests. TYX's optional documentation packages translate Atlas programs into laser-printed test-requirements documents, or TRDs, flow charts, and other documentation in printing formats that meet military specifications. The first of these packages, called the TRD/Atlas generator, also translates existing TRDs into Atlas programs. PAWS also has a host of optional Atlas subsets and utilities.

Another aid to development is an expert system supplied by Automated Reasoning Corp., New York, that runs on the Apple Macintosh. For instance, it will analyze a microprocessor-board schematic and such data as part costs and failure probabilities, then recommend test and fault-isolation procedures. When the user is satisfied with the test strategy, he develops the test program with PAWS. *–George Sideris*

For more information, circle 486 on the reader service card.

SUMMATION BETS ON PC-BASED TESTERS

Fledgling Summation Inc. is laying all its money on just one horse: the volume market for low-cost test systems based on IBM Corp.'s Personal Computer AT. To help it run faster, the Kirkland, Wash., company is pursuing a "customer-driven" strategy—customers specify system capabilities they want, and Summation supplies them in a system that users can program and customize themselves. The strategy is starting to pay off.

Summation, which announced its first product, the SigmaSeries, in October 1985 and began shipping systems in January 1986, claims more than 100 users, including Ford, General Electric, General Motors, and IBM. Average system price is about $35,000. First-year sales were several million dollars, says Jimmie E. Bloomer, Summation's president, declining to be more specific. Second-year sales will probably be twice as large.

ADDING IT UP. Cofounders Bullis and Seres and president Bloomer (from left) built Summation on the idea of PC-based ATE.

Summation's move now into the military market (see p. 69) can be attributed in part to sheer luck. Last fall, Bloomer demonstrated the SigmaSeries at E-Systems Inc.'s Melpar Division, Falls Church, Va., a leading producer of electronic-warfare equipment. Lindsay Coffman, Melpar's test systems manager, thought the system would be useful in future applications if it could be programmed in Atlas, the standard military test-system language. So, after Bloomer left, Coffman called John M. Thompson, ATE marketing manager at TYX Corp. in nearby Reston, Va., which supplies Melpar with Atlas development software. Coffman gave him Bloomer's phone number and said something like, "Why don't you two get together?" They did that evening, and the end result was the Summation Atlas test system.

Summation also had a bit of luck with the main SigmaSeries software package. The company was founded just as Microsoft Corp. of Redmond, Wash., was developing its Windows software for PCs. Summation became an alpha test site for the software and became the first company to ship a Windows-based software system. Called TestWindows, the package allows tests to be programmed and controlled through a simplified graphics interface.

Cofounders David A. Seres, 40, vice president of engineering, and David C. Bullis, 34, vice president of sales, started planning the series a full year before the official startup in May 1984. Both had been research supervisors at Du Pont Co.'s Engineering R&D Division. Seres recalls that Du Pont was spending $100,000 to $200,000 per system to build automatic test equipment with conventional instruments and controllers. He and Bullis realized that the opposite approach, a modular system with a tightly coupled software package, would be inexpensive and do the job.

Now the three-year-old company is going for the military market

That idea didn't quite jell, though, until the IBM PC came along. The realization that the PC could be used as a controller was the catalyst that prompted them to quit Du Pont and draft a business plan for Summation in 1983.

Seres and Bullis recruited Bloomer, 43, who was formerly general manager of John Fluke Manufacturing Co.'s Instrumentation Division. Seven leading venture capital firms invested a total of $16 million, and Summation was in business.

To start things off, the company's executives identified 65 major commercial and military/aerospace manufacturers on the West Coast as potential customers. After the company started business they spent the first 100 days canvassing and visiting those companies, says Bloomer. After shipments began, the company beefed up its customer-support staff with engineers to be sure of getting correct feedback on new requirements.

The basic system was designed for both analog and digital applications but, says Bloomer, "we didn't have the resources to develop both at once. We started with analog instruments that solved the majority of problems for those 65 companies." He adds, "We didn't know at the time exactly what digital capabilities would be needed. We selected a 20-MHz test rate because 10 MHz covers about 90% of requirements and 20 MHz about 95%."

However, he concludes, "We would never have been able to bring our product out in 13 months without giving our employees a sense of ownership." So every employee receives stock, in addition to normal wages, and extra stock for merit after periodic evaluations, and, Bloomer says, "That philosophy gives us the ability to move very rapidly into the marketplace."

–George Sideris

UPDATE: TANDEM'S VLX RACKS UP NONSTOP SALES


TANDEM MAKES A GOOD THING BETTER

ITS FIRST MAINFRAME RUNS TWICE AS FAST

Since Tandem Computers Inc. introduced its first mainframe-class of fault-tolerant computers, the NonStop VLX, a year ago, sales of the new system have soared. Now the company is getting ready to introduce new configurations of the VLX that it hopes will get the same reception as the original, which accounted for 75% to 80% of the company's growth in the past year, says Terence Retford, manager of systems products at Tandem.

The Cupertino, Calif., company began shipping the VLX in small quantities prior to its formal introduction [*Electronics*, April 14, 1986, p. 34]. Volume production began almost immediately thereafter. Customer reaction was instantaneous, and sales have consistently exceeded forecasts.

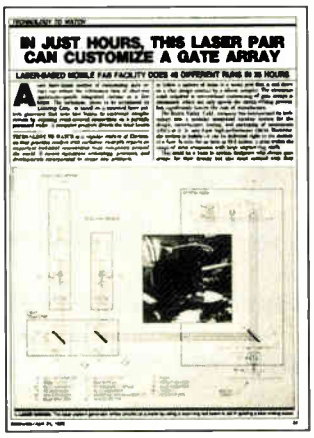
The new configurations, coming in May, will extend the system's capabilities at both the high end and the low end. They will be based on the same bipolar gate array used in the VLX, the MCA2800, which Tandem developed with Motorola Inc. One of the main challenges for the team working on the upgrade was keeping pace with technology. Al McBride, director of technology at Tandem, says that the number of transistors on bipolar gate arrays once was doubling every year; now it's tripling.

Despite the advances that the VLX systems represent, they don't seem to compete with the older Tandem NonStop TXP system. "The TXP systems are selling at the same rate after the VLX announcement as before," says McBride. Apparently, established Tandem customers have chosen to expand their existing TXP systems rather than buy into the newer VLX product. That means that VLX is appealing largely to new customers, although existing customers can buy the new VLX and tie the new and old system together with a fiber-optics link called FOX.

What characterizes the new customers is their demand for the sheer power of the VLX—twice the transactions per second of the old TXP systems, delivered by a modular system that can contain up to 16 processors, all operating on a high-speed processor bus. To get more power, customers simply add more processor cards.

That seems to indicate that the new customers come at the expense of the company Tandem has always regarded as it prime competitor—IBM Corp. "Before, there was only one supplier of high-end transaction processing systems," says Retford, "and that was IBM. VLX for the first time gave customers an alternative, which not only offered more functionality but also came at a better price-performance." *–Jonah McLeod*

UPDATE: NOW LASARRAY IS READY FOR A BRISK YEAR


IN JUST HOURS, THIS LASER PAIR CAN CUSTOMIZE A GATE ARRAY

Lasarray Corp. got off to a slow start after the introduction last year of its laser-based method of customizing gate arrays [*Electronics*, April 21, 1986, p. 51]. The company's management has spent much of its time reorganizing its operations in Europe and setting up a U.S. sales and marketing staff. With those tasks accomplished, Lasarray is now gearing up for a brisk year in 1987.

A round of financing by private investors in Europe—where Lasarray was founded as an operation within Switzerland's FELA group—has given the company some $15 million to work with. And commitments are in hand for the purchase of at least five of Lasarray's turnkey mobile fabrication facilities, costing $3 million to $4 million apiece. First delivery of a system is scheduled for May, says vice president George Krautner.

Based on a laser pattern generator, the system uses two beams to customize circuits by exposing resist-covered connections on a partially processed wafer. A computer program directs the beams along a pattern of holes in a metal grid that is laid down on a chip design created by a silicon compiler. The technique eliminates the chromium mask required in conventional gate-array customization, making circuit-writing faster and manufacturing less expensive.

The turnkey systems include equipment for design, testing and packaging of the resulting CMOS arrays. With it, a finished prototype takes only a few hours from the completion of a design simulation.

So far, orders for the system have all come from European companies, Krautner says. But he expects an enthusiastic reception in the U.S. once a demonstration facility now being built at the company's headquarters in Scotts Valley, Calif., is completed. *–Bernard C. Cole*

SMART SENSORS WILL HELP CUT WIRING THAT CLOGS SYSTEMS

Micro Switch's application-specific sensors can interface with any bus protocol; they will help reduce the fast-growing maze of wiring in cars, buildings, and aircraft

by Jerry Lyman

A new breed of smart sensors from the Micro Switch division of Honeywell Inc. promises to get rid of most of the increasingly complex wiring that is snaking through automobiles, buildings, factories, and aircraft. As microprocessors take over the control of more and more mechanical functions, from windshield wipers to jetliner landing gear, the need is growing for the flow of data to and from the equipment being controlled.

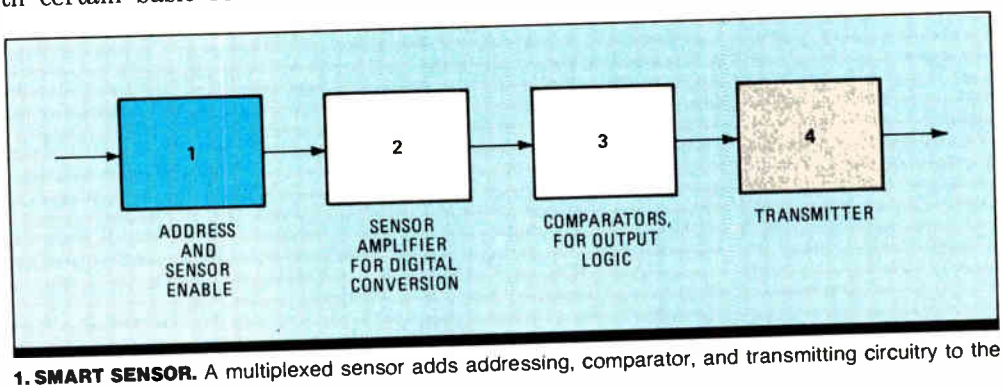
The solution seems obvious: data multiplexing—the simultaneous transmission of multiple messages on a single wire—can keep wiring requirements to a minimum. But for a data-multiplexing system to operate effectively, the devices providing the inputs to the multiplexed bus should also be "smart," or capable of performing their own logic functions. Because a majority of inputs to the data system are sensors, the place to begin multiplexing is with the sensors themselves.

That's exactly what Micro Switch did. Engineers at the Freeport, Ill., company developed smart-sensor integrated circuits that combine sensing, amplification, digital logic, and data communications functions on one chip. The sensors are not only capable of being multiplexed, but they also can be easily customized to interface with any bus protocol. Moreover, the sensors can be tailored to work in different kinds of systems—they are, in effect, application-specific.

Such adaptability is particularly important in the first application that the smart sensors are likely to be used for, automotive systems, where standards for multiplexed wiring are still in flux. Mona AbdelRahman, the director of technology for Micro Switch, says that this adaptability probably also will come in handy in the other areas where the sensors are likely to be used: building automation, industrial and process control, and avionics.

To cover the range of applications, the Micro Switch engineers started with certain basic requirements. The smart sensor they needed would have to have various characteristics such as amplification and internal environmental compensation, integral data conversion and digital processing, bus and microprocessor interface capability, built-in self-diagnostics, and transient protection.

However, the current generation of smart sen-



1. SMART SENSOR. A multiplexed sensor adds addressing, comparator, and transmitting circuitry to the circuitry of the standard sensor.

sors are general-purpose devices. Using them could result in overkill, bringing to bear more intelligence than is needed for an application and making the devices more expensive than they need to be. The solution is the application-specific sensors, which will not only lower the cost but will make the sensors themselves more efficient.

With that concept in mind, Micro Switch developed a strategy for implementing application-specific sensors, beginning with those to be used in automobiles and later extending to the other applications. The starting point was certain generic characteristics that are expected from any "smart" sensor. Micro Switch sees these characteristics as separate functional sensor requirements that can be represented in a simple single-path, four-block flow chart (see fig. 1).

The problem: general-purpose sensors with more intelligence than they need drive up costs. The solution: cheaper and more efficient application-specific sensors

Block 1, which contains address and enable functions and transient protection, has to do with the sensor's ability to identify itself as a separate element and realize that it has been addressed by the system. Once this happens, the enable function turns on the next component, Block 2. This block does actual sensing of the required parameter, such as temperature, pressure, position, acceleration; amplifies the signal if necessary; compensates for environmental drifts; and converts the signal to a digital form.

Block 3, composed of logic and comparator circuitry, notifies Block 4 of the status, pass or fail, of the information from the sensor block and also may produce diagnostic data or even send a signal to Block 2 to switch in a redundant sensor in a critical application. Block 4's function is to format the digitized sensor data of Block 2 to the protocol required by the bus. Block 4 is then able to "talk" back to the bus or the microprocessor.

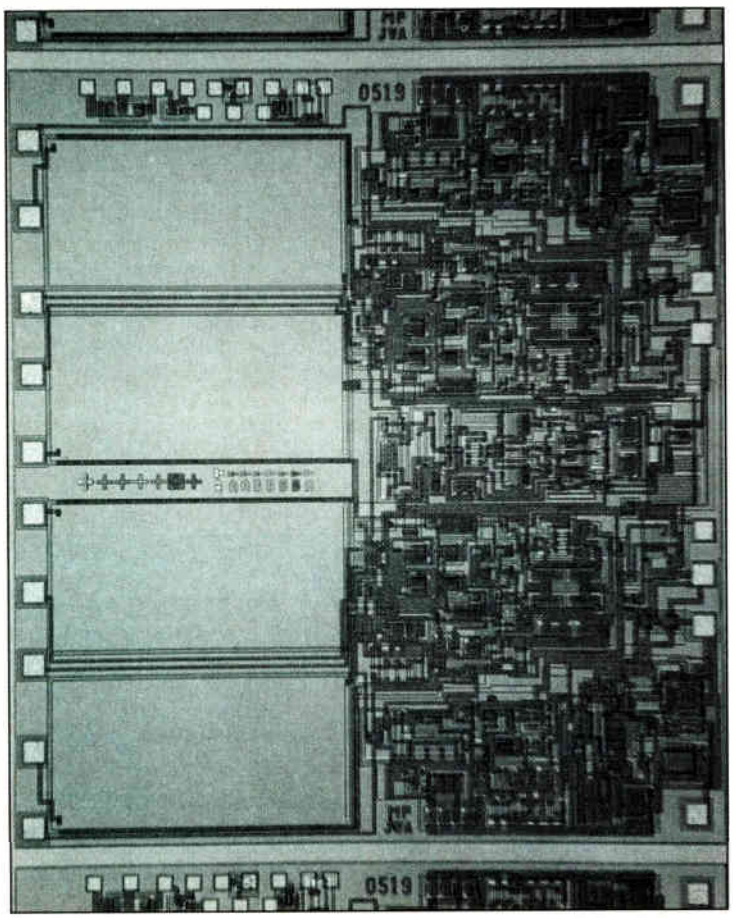
The key to the new smart sensors lies in Block 1 and Block 4, which are the only elements that would need to interface with a multiplexed system. Therefore, they are the only elements of the sensor that would have to conform to any specific protocol. The complexity of Blocks 1 and 4 is determined by whether the sensor is interfacing with the microprocessor or the bus. If it is interfacing with the bus, complexity is further determined by the protocol, the number of sensors talking to the bus, and the data rate.

The complexity of Block 2, the actual sensing portion of the smart sensor, is based on what is being sensed, the required degree of accuracy, the environment within which the sensor is operating, and the type of output required.

Block 3 could have two levels of complexity. The simplest would deal with just reporting the status of the parameter being sensed. This would be enhanced by a second level of internal self-diagnostics that checks the output signal to evaluate potential sensor failure.

An example of the type of IC that Micro Switch will use in its future smart sensors is a multiplexable optical encoder chip (see fig. 2) produced for Honeywell by its Optoelectronic Division in Richardson, Texas. This chip combines sensors and analog and digital circuitry on a single chip. The on-chip sensors can determine direction or rotation, rotational velocity and angular position.

This 60-by-80-mil chip, manufactured with a high-speed bipolar process, uses the four-block approach. For this chip, Block 1's function is as a sensor address and enabling, specifically for multiplexing, which would be application specific and custom-designed. Block 2 has four sets of photodetectors that form two channels. These channels are configured to be 90° out of phase. The output of these detectors is fed into Block 3 where a decision on rotation direction, rotation velocity, or angular position is made. Block 3's output is then sent to the transmitter stage of Block 4, where there is the option of digital out-



2. ON ONE CHIP. The multiplexed optical encoder combines four optical sensors with digital and analog circuitry.

put for interfacing to a microprocessor or analog output for the next drive stage.

This four-block functional approach to the development of customized smart sensors will eliminate waiting for a protocol to be established for multiplexed automotive systems—an important consideration, since the major auto manufacturers so far have not settled on a standard bus protocol for multiplexed wiring, although they have formed committees to address various multiplexing options.

Micro Switch has worked around the automakers to develop smart multiplexable sensors compatible with any bus protocol they might adopt. Their protocol will deal only with data communication, so only those blocks interacting with the system would have to conform to it. The protocol will dictate the proper choice of digital logic to communicate with the bus.

The crucial matter is the ability of the sensor to accurately perform its function and communicate the data that it gathers. Various technologies to do this in different applications are now under development or are being refined at Micro Switch.

In automotive applications, multiplexing can be applied in both control and communication applications. Control is further divided into two categories, low speed and real time. Both control types of multiplexing are heavily dependent on sensors to do their tasks.

Control multiplexing deals with the operation of relatively static functions such as lights, power locks, horns, and windshield wipers. This type of low-speed multiplexing, together with data communication, will be the first to be addressed by the automotive manufacturers. High-speed control, which deals with real-time control of antilock brakes, active suspension systems, and the like, is more difficult and will take longer to develop.

Micro Switch worked with major U. S. automotive suppliers to develop its automotive sensors. Qualification and reliability testing are under way, and production-level manufacturing is expected to begin in 1988. Automobiles with multiplexed sensor systems might be available as early as the 1988-1989 model year.

The future holds a host of applications for smart sensors: building-automation and industrial-control systems will depend on multiplexed sensors to cut miles of wiring

Beyond automobiles, other applications beckon. For example, in today's building automation control systems—an area in which Honeywell is particularly strong—smoke and fire detectors, thermostats and air conditioning, and building security systems all depend on sensors. They also are all linked to a master minicomputer by miles of wiring. Multiplexing sensors can, as in automotive applications, substantially cut the amount of wiring.

In industrial control, sensors may be used for diagnosing problems. For example, a machine tool on a factory floor might be monitored for vibration and temperature to prevent possible failures. Process control and aviation instruments are also heavily based on multiple sensors and eventually should be candidates for multiplexed smart sensors. □

For more information, circle 487 on the reader service card.

FOR MICRO SWITCH, SMART SENSORS ARE A TEAM EFFORT

Micro Switch's game plan to become the No. 1 sensor supplier to the automotive industry called for it to first assemble the best team in the league. The Freeport, Ill., division of Honeywell Inc. chose some talented specialists from Micro Switch and other Honeywell divisions with Mona AbdelRahman, director of technology at Micro Switch, as the quarterback.

AbdelRahman, the coordinator of the development effort for smart sensors, oversees team assignments in areas ranging from sensors to data communication, important elements in defining sensor requirements for multiplexed automotive systems. Multiplexed sensors for any application, she says, must be considered in terms of performance, diagnostics, data-communication capabilities, protocol boundaries, and cost.

Expertise in these areas was gathered from various Honeywell organizations. For example, teams from Honeywell's Solid State Electronic Division, the Optoelectronic Division, and the Physical Science Center contributed experience in silicon-based technology and a range of processing capabilities. Input on communication issues came from the Corporate Systems Development Division, and Honeywell Systems Research contributed system-design information.

QUARTERBACK. Mona AbdelRahman leads the sensor-development team.

As head of the team, AbdelRahman brought a wealth of expertise to the project. She earned an undergraduate degree in electrical engineering from Cairo Institute in 1966, and a master's and a doctorate in solid-state physics from the University of Minnesota. She joined Honeywell's Solid State Electronics Division in 1973 and spent 12 years working on silicon sensor and integrated-circuit technology. She later worked at the Physical Science Center on smart-sensor development for building automation, factory automation, and the medical industry, then joined Micro Switch as manager of technology in 1984.

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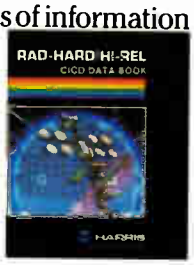

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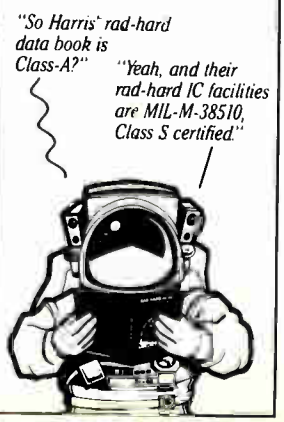

MILITARY/AEROSPACE NEWSLETTER

AVIONICS WORK FOR FIGHTER TO COST $900 MILLION OVER FIVE YEARS

The Air Force will spend at least $900 million over the next five years on avionics development for its Advanced Tactical Fighter. "There may be some things in the initial phase of the program that we can't afford, but we'll get to them," says Brig. Gen. John A. Corder, director of the Air Force's electronic combat programs. Most of the ATF program's avionics development budget will go for systems integration and software. Meanwhile, the development phase of the program is already under way. A team composed of Lockheed, General Dynamics, and Boeing Military Airplane will compete with the team of Northrop and McDonnell Douglas to design the ATF. Early this month, Boeing awarded a contract to design the active-element phased-array radar demonstration/validation system for the ATF to a development team made up of Westinghouse Electric Development and Operations Divisions and Texas Instruments Defense System & Electronics Group. The first prototypes are scheduled to fly in 1989. The Navy also will ask the two contracting teams for concept studies of a Navy version of the ATF. □

GTE NOW WANTS TO SELL ITS ARIZONA SEMICONDUCTOR FACILITY

GTE Corp. is trying to sell the 176,000-ft² semiconductor facility built in 1984 in Tempe, Ariz., for its government systems and laboratories subsidiaries. The facility employs 55 engineers and support staff from GTE Government Systems and 19 from GTE Laboratories Support Group. The operation is a 1.2-μm facility with a capacity of 6,000 wafer starts a week, according to Paul Stein, vice president for business and venture development, GTE Product & Systems Group, Stamford, Conn. Stein would not disclose GTE's asking price. The facility was used primarily to develop and produce advanced semiconductors to meet government contracts. The military work is over, and there are few prospects for more government work, Stein says. He adds that joint GTE ventures with Siemens and Fujitsu mean developing commercial products at the Tempe operation is no longer necessary. □

PENTAGON JUMPS ON SUPERCONDUCTOR BANDWAGON

Superconductors, materials capable of carrying electric current without power loss in the form of heat, have caught the eye—and the imagination—of the Pentagon. The Defense Advanced Research Projects Agency, or Darpa, will soon become very active in superconductive materials research, according to Darpa Director Robert C. Duncan. The Navy, meanwhile, has started its own in-house superconductive materials-research program. "Superconductors will revolutionize your industry; keep a close watch on them," Chief of Naval Research Rear Admiral J. B. Mooney Jr. told a group of industry executives at a mid-April conference on military research in Alexandria, Va. The Army Material Command has identified advanced materials as one of its R&D priorities and will seek industry input over the next several months on potential applications for superconductive materials. □

DOD SEEKS NEW COMPONENTS SUPPLIERS

The market for military components should become more competitive now that the Defense Electronics Supply Center in Dayton, Ohio, the Pentagon's principal procurement center for electronic spare parts, intends to open up competitive bidding for parts—such as semiconductors, resistors, capacitors, and relays—that it currently buys from single sources. DESC expects representatives from more than 500 companies to show up May 7 to compete for contracts in 200 components categories that together account for more than $30 million in procurements by DESC each year. □

MILITARY/AEROSPACE NEWSLETTER

A NEW PENTAGON GROUP WILL COORDINATE AVIONICS R&D

The Pentagon is forming a Joint Integrated Avionics Working Group comprised mainly of military technical officers to coordinate the avionics research and development efforts of the Air Force and Navy. Contractors and standards groups, such as the Institute of Electrical and Electronics Engineers and the Society of Automotive Engineers, will be asked to participate as advisors. Both the Air Force and Navy are emphasizing the upgrading of avionics. Each has major programs to integrate advanced avionics systems and cockpit displays in future aircraft, and to make these subsystems more reliable and easier to maintain. The Air Force has budgeted $53.3 million in 1988 for advanced avionics technology development; the Navy, $3.8 million. In separate programs, the Air Force plans to upgrade the avionics of most of its current fighter aircraft. The Air Force has also asked for $41.2 million in 1988 for advanced development work in 380 electronic combat-technology programs. □

AIR FORCE MAY SET UP RECON SQUADRONS, OPENING NEW MARKETS

The Air Force is considering setting up squadrons around the world that are dedicated solely to reconnaissance missions. Because most of the Air Force's aircraft are assigned to combat-ready roles, they often are either unavailable or ill-equipped for recon tasks. There's no word out of the Pentagon yet about new procurements for recon hardware and software, but the Air Force's Programs & Resources Office is pushing for specially equipped aircraft and specially trained crews to perform virtually all of the Air Force's recon tasks. The Air Force believes that by dedicating aircraft solely to reconnaissance, it will be in a better position to maintain and integrate new technologies as they're developed. □

MILITARY SIMULATOR/TRAINER MARKET AVERAGING $3.4B A YEAR

The complexity of modern military weapons has created a market averaging $3.4 billion a year for simulators and trainers, according to a market study by Frost & Sullivan Inc. of New York. Nearly $18 billion will be spent between 1987 and 1991 on this equipment, the report says. The Navy is the biggest spender, averaging close to $1.3 billion a year. The largest portion is devoted to aviation trainers and simulators. The Air Force is putting half of its spending for this technology, which will average about $1.2 billion a year up to 1991, into flight simulators. The Air Force believes fighter simulator training is "severely limited by lack of visual scene detail and complexity and by limited display brightness and resolution," Frost & Sullivan reports. The Air Force also has determined that it needs more on-board training systems in its fighter aircraft to create simulated combat conditions, and it is developing plans to fill the requirement. □

HOLOGRAPHY, COLOR LCD, VOICE-ACTUATED CONTROLS TO GO INTO NAVY JET

The Navy hasn't said anything new about its Advanced Tactical Aircraft program since October, when it confirmed that two teams are competing for the ATA contract—Grumman, Northrop, and Vought Corp. and General Dynamics and McDonnell Douglas. However, military officials left little doubt about just how advanced the aircraft will be when they disclosed some of the proposed features of the ATA's cockpit at a recent industry meeting: a holographic head-up display, LCD color instrumentation, and voice-actuated controls. But there is another telling factor in its secrecy—it's the only program office listed in the Naval Air Systems Command directory with no room number. □

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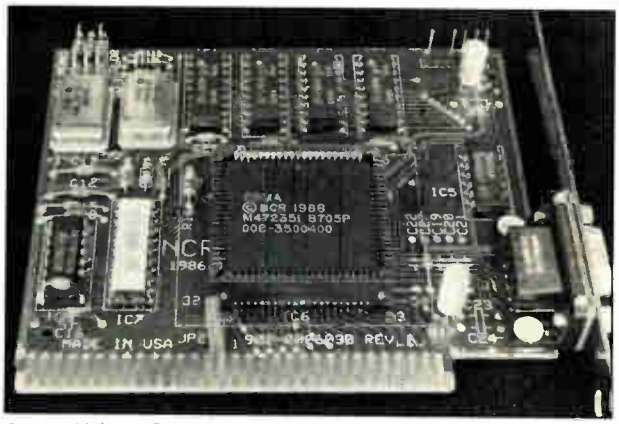
NEW PRODUCTS

A SINGLE NCR CHIP SUPPORTS THREE IBM PC GRAPHICS FORMATS

THE 7280 ALSO INTEGRATES A CRT CONTROLLER

Graphics-board designers can now use a single display-adapter chip to implement three of the most commonly used IBM Corp. Personal Computer graphics formats: MDA (Monochrome Display Adapter), HGA (Hercules Graphics Adapter), and CGA (Color Graphics Adapter). NCR Corp.'s CMOS 7280 Color Graphics Monochrome Adapter chip also features a 6845 cathode-ray-tube controller and a high-definition CGA mode that doubles the number of scan lines for sharper graphics and higher-quality text while maintaining CGA compatibility.



CHIPS. Using NCR's 7280, a three-mode graphics board requires only a frame-buffer memory and clock circuitry.

The 7280 was developed by NCR's Microelectronics Division. Brian Herbert, the division's graphics and PC support product manager, says the 7280 is the first chip of its kind. At least one other vendor offers a circuit that provides MDA, HGA, and CGA compatibility on the same device and also conforms to a fourth standard, Plantronics Plus. But that chip—the Spectrum, from Genoa Systems Corp., San Jose, Calif.—requires a separate 6845 CRT controller.

AFFORDABLE COLOR. The 7280 is aimed at low- to medium-priced graphics applications. NCR expects to see continuing demand for the chip, despite the likely emergence of a new high-end graphics standard based on the VGA (Video Graphics Array) format used in IBM's Personal System/2 [*Electronics*, April 16, 1987, p. 46].

VGA's 640-by-480-pixel resolution will require a $600 monitor, says Herbert. Monochrome monitors that can handle MDA or HGA sell for $100 or less, while CGA-compatible monitor prices average around $340. Monitors that support EGA (Enhanced Graphics Adapter), IBM's previous high-end format, also cost more, Herbert says—$435 to $550. "Right now, CGA is the most affordable way to get into color," he says.

EGA is superior to standard CGA when used in text mode, but the 7280's high-definition CGA mode gives performance comparable to EGA. Compared with standard CGA's 8-by-8-pixel text character cells, the 7280's high-definition mode uses an 8-by-14 cell, producing text quality equal to EGA, Herbert says. Since the NCR high-definition mode doubles the number of scan lines, the 7280 produces two additional inter-row spacing lines not found in EGA, he notes. In graphics mode, the scan doubling produces 640-by-400-pixel resolution, compared with EGA's 640-by-350 graphics.

The 7280 features direct interfacing to the PC bus, display monitor, and frame buffer, eliminating the need for glue logic. A 16-bit-wide interface to the frame buffer allows for interleaved memory access, since the 7280 can read 2 bytes per cycle from the frame buffer, compared with a 1-byte read with standard CGA. This interleaved approach provides for "flashless updates" without the snow seen on standard CGA displays, Herbert says. "We read a word twice as wide as normal, so this gives us an extra cycle in which we can write data to the memory without having a conflict between writing to the memory and refreshing the screen," he explains.

NCR expects the 7280 to be used with four 64-Kbit-by-4-bit dynamic random-access memories acting as the frame buffer to provide the 16-bit-wide interface. For a full-blown system, two additional clock oscillators are also required. A 16.257-MHz clock is needed for the monochrome MDA and HGA formats. The high-definition CGA format requires a 20-MHz clock. (The 14.318-MHz signal needed for standard CGA is available on the PC bus.)

Built with NCR's 3-μm CMOS standard-cell technology, the 7280 provides 35-mA power dissipation, typical, and less than 100-mA maximum. Available now in an 84-pin plastic leaded chip carrier, the chip costs $28.50 each in 1,000-unit quantities and $23.50 in 10,000-unit quantities. During the second half of this year NCR plans to convert production on the device to a 2-μm CMOS process and reduce 10,000-unit pricing to $17.85 per chip.

–Wesley R. Iversen

NCR Microelectronics Division, 1635 Aeroplaza Dr., Colorado Springs, Colo. 80916. Phone (303) 596-5612 [Circle 360]

5-V OP AMPS SPAN MILITARY TEMPERATURE RANGE

GE/RCA Solid State Division's upgraded line of BiMOS operational amplifiers have guaranteed specifications for 5-V power supplies over the full military temperature range of −55° to +125° C. The new CA5000 line includes three single op amps—the 5420, 5130, and 5160—and the 5422, a dual op amp introduced earlier this year.

What makes the devices special is that the company is able to guarantee performance under specific operating conditions, says Carmine Salerno, product manager for op amps at Solid State headquarters in Somerville, N.J. "If you're looking at op amps and you're using 5-V characteristics, you'd choose these," he says. "I haven't seen other op

amps out there that have guaranteed 5-V specifications."

LEAKPROOF. The 5420 and 5422 chips feature circuitry that helps keep input levels low. Under normal operation, conventional MOS op amps fall victim to rising current leakage, which can force designers to raise input levels. Current leakage rises with the temperature, doubling every time the operating temperature goes up 10° C, in most devices. But a guard-banding circuit built into the 5420 and 5422 chips compensates for that, Salerno says. "These internal guard-banding terminals allow input current to be kept constant all the way up to 85° C," he says. The guard-banding circuit accomplishes this by nulling the input currents at either or both input terminals. Above 85° C, leakage is kept below 1 nA.

Capable of operating with a supply as small as 2 V, the 5420 output stage—an output transconductance amplifier—provides high output swings from 0.12 V to 4.9 V. The 5130 and 5160 are intended for use with high-speed CMOS logic and microprocessors, Salerno says. The two are almost identical, but the 5160 features built-in frequency compensation and slightly lower bandwidth and slew-rate specifications. The 5160 has a unity-gain frequency of 4 MHz and a slewing rate of 10 V/μs; the 5130 is rated at 15 MHz and 30 V/μs.

Intended for low-power applications such as 5-V microprocessor-based systems, the op amps draw very low bias current—less than 2 pA at 25° C. As a result, they maintain high impedance for the driving circuits. The chips have a wide input-voltage range and high gain. "They can sink and source at least 1 mA," says Salerno.

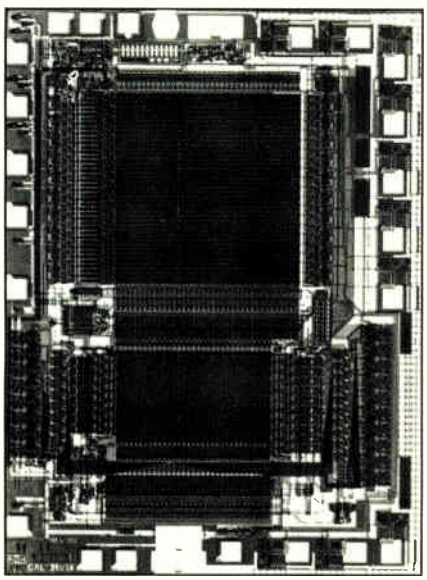
All parts are available in regular and enhanced versions, called A versions, that offer improved performance characteristics. They can be purchased in either 8-pin metal TO-5 packages or in 8-pin plastic dual in-line packages. In plastic packages, 1,000-piece pricing for the 5420 is $1.30 each, the 5130 is 79¢ each, and the 5160 is 72¢ each. Pricing for the enhanced versions is $2.38 for the 5420, $1.13 for the 5430, and $1.08 for the 5460. – *Tobias Naegele*

GE/RCA Solid State Division, P. O. Box 2900, Somerville, N.J. 08876.
Phone (201) 685-6652

CMOS LOGIC ARRAYS OFFER HIGH DENSITY

Lattice Semiconductor Corp.'s GAL39-V18 programmable logic array offers 75 inputs and outputs on its AND-gate array and 64 inputs and 36 outputs on its OR-gate array. This is two to four times the density of earlier PLDs, Lattice says. The 39V18 allows designers to create computer interfaces and bus controllers with the same functionality as full-custom devices but costing less.

Based on a field-programmable architecture and fabricated in the company's E²CMOS technology, the 24-pin device features 30-ns delays from input to output and 15-ns delays from clock to output.



CMOS technology halves the device's power consumption compared with competitive bipolar logic arrays. Typical input current is 80 mA with a maximum of 120 mA. Samples are available in 300-mil plastic dual in-line packages for $20 each in 100-unit purchases.

Lattice Semiconductor Corp., 15400 N. W. Greenbriar Pkwy., Beaverton, Ore. 97006.
Phone (503) 629-2131 [Circle 365]

CACHE-TAG MEMORIES BOAST 20-ns ACCESS

Texas Instruments Inc. is reducing the fastest access time on its cache-tag memories from 35 ns to 20 ns by shifting to a 1-μm CMOS process technology. The first chip to use the new technology is the popular n-MOS 512-by-8-bit part.

The TACT2150 chip is the first in a family of fast CMOS cache-tag memories. TI expects to trim access time down to 15 ns by year's end. Applications will include 32-bit desktop computers, where a 20-ns cache-tag chip is fast enough to keep a 25-MHz system bus busy, says the company.

In 10,000-piece quantities, the 2150 with 20-ns access time sells for $16.20 each in quantities of 10,000. A 30-ns version of the part costs $12.96 each.

Samples of similar cache-tag memories designed in 1-Kbit-by-12-bit and 2-Kbit-by-8-bit configurations will be introduced later in the year, but prices for these devices are not available.

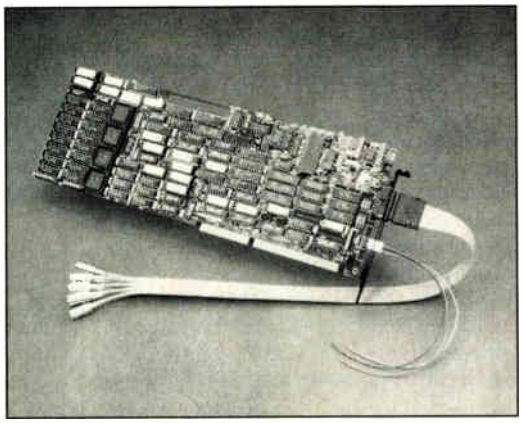
Texas Instruments Inc., 13500 N. Central Expressway, Dallas, Texas 75265.
Phone (214) 995-2011 [Circle 366]

PC/AT VIDEO BOARD GRABS 30 FRAMES/S FOR $1,600

DATA TRANSLATION'S 2853 LACKS SOME FEATURES OF THE HIGH-END 2851, BUT IT COSTS $1,400 LESS

Data Translation Inc.'s DT2853 frame grabber—a low-cost version of its full-featured DT2851—lets IBM Corp. PC/AT users acquire, store, display, and process images at 30 frames/s for less than $1,600.

The price brings it into the market $1,400 below the full-featured board and $200 to $400 under competing low-cost frame grabbers, some of which have fewer onboard functions, says John Molinari, product marketing manager for imaging products.



SINGLE SLOT. The DT2853 runs Data Translation's Iris software and uses a single slot of an IBM PC/AT.

The DT2853 runs the company's DT Iris software and plugs into a single slot of a PC/AT. It digitizes a 512-by-512-by-8-bit image from a video signal, stores the image in one of two on-board buffers, and displays it in RGB false color or monochrome at 30 frames/s.

The DT2853 is compatible with monochrome or color video cameras and with VCRs. It includes an 8-bit flash converter that produces pixels in 256 gray levels. Two external triggers are available for applications such as machine vision inspection that usually require frame grabbing to occur in synchronization with one or more external events.

The DT2853's ability to process images is a bonus that Molinari says isn't usually found in a low-cost unit. Processing includes the ability to add images or subtract them from one another, multiplication or division by a constant to adjust contrast, image averaging, and image-of-interest processing.

What the DT2853 does not include are slow-scan and a direct connection to a companion frame processor—a dedicated array processor. Slow-scan allows image acquisition from sensors that are slower than TV cameras or VCRs, such as CAT scanners or scanning electron microscopes. These features are found in the $2,995 DT2851.

SQUARE DISPLAY. A square-pixel version of the DT2853 is available for an additional $400 for applications such as graphics, robotics, or feature measurement, which require a perfectly square display (1 : 1 aspect ratio). This feature eliminates the geometric distortions inherent in standard rectangular displays (4 : 3 aspect ratio), such as TV screens. The DT-Iris software library contains image-processing algorithms that make full use of the real-time features of the DT2853 and are callable from Pascal, C, and Fortran.

Both the DT2853 and DT-Iris are available immediately; DT-Iris sells for $695. *–Lawrence Curran*

Data Translation Inc., 100 Locke Dr., Marlboro, Mass. 01752.
Phone (617) 481-3700 [Circle 340]

TANDEM ON-LINE UNITS TARGET LOW END

Tandem Computers Inc. has invaded the low end of the market for on-line transaction processing with two new systems, one a Motorola Corp. 68020-based computer running AT&T's Unix V.2 and the other supporting Tandem's proprietary Guardian operating system. Both are intended to extend transaction processing to distributed environments and support multiple communications protocols. Tandem also announced a desktop eight-page/min. laser printer, the Laser-LX.

PIONEER. The LXN computer is Tandem's first venture into the Unix operating system environment, where the company hopes to gain access to a burgeoning number of applications in banking, retail sales, manufacturing, telecommunications, and transportation—all markets served by Tandem's larger minicomputer line. In keeping with Tandem's traditional emphasis on high reliability, the LXN provides disk mirroring and power automatic restart.

The LXN is being supplied to Tandem by the original-equipment manufacturer Altos Computer Systems Corp., San Jose, Calif. It represents the first of several steps Tandem will take to integrate Unix into on-line transaction processing, a Tandem spokeswoman said.

The Motorola processor on which the LXN is based runs 2.3 million instructions per second. The machine can access Tandem's own systems via the company's SNAX communications software, or it can communicate with IBM Corp. mainframes via SNA or with other Unix systems using the CCITT X.25 packet-mode network.

COMPATIBLE. The LXN networks with IBM Corp. mainframes and AT&T Unix systems.

The system using Guardian, the NonStop CLX, is intended for use in departmental and branch offices and is built around the CMOS gate-array implementation of Tandem's proprietary central processing unit. Although it is the first Tandem computer to be offered with a single processor, up to six processors may be configured in a single system.

System performance ranges from 2.5 to 15 data-base transactions per second, depending on the number of CPUs. The system supports SNA, Open Systems Interconnect, and X.25 networking, as well as connections to several commercial local-area networks.

The new laser printer is compatible with Hewlett-Packard Co.'s LaserJet Plus, giving users access to hundreds of Unix and MS/DOS applications. It is intended for desktop-publishing applications averaging 4,000 pages a month.

Available now, the Unix-based LXN costs $18,012 each for 25 to 39 systems. Although the $39,500 single-processor

CLX 610 will not be available until 1988, the two-processor CLX 620 version will be released in the fourth quarter of 1987 at $59,500 in lots of 25 to 39. The LaserLX printer will cost $2,595 when it becomes available in the third quarter of 1987.

Tandem Computers Inc., 19191 Vallco Pkwy., Cupertino, Calif. 95014.
Phone (408) 725-600 [Circle 341]

WANG DESKTOP SYSTEM COMBINES TEXT, GRAPHICS

Office automation projects and systems that have stumbled over the formidable task of efficiently handling information in different formats are getting a powerful new tool in Wang Laboratories Inc.'s Integrated Image Systems, which can integrate images with text on a single desktop work station.

With the system, an order-processing clerk, for example, can call up an image of a purchase order, check the accounts receivable data base for a credit profile and approval, and enter the order into the system through an order-entry data base. A confirmation letter can be written for the customer, and an image of the purchase order and cover message can be sent to the shipping office over the company's Wang Office electronic mail.

MINI-BASED. Built around the VS superminicomputer line and PACE, the company's application-development and relational-data-base manager, the system targets applications in financial services, insurance companies, the legal profession, and health care. An entry-level System I—consisting of a VS processor, an Image work station, a stand-alone optical disk drive, a scanner, a standard VS work station, and Wang Integrated Image Systems environment software—will sell for approximately $100,000.

The first page of a document can be retrieved from a dedicated optical drive in 10 s; the second page takes 3 s. Retrieval times from optical jukeboxes are 20 s and 3 s for the first and second pages, respectively; from a microfilm storage-and-retrieval unit, the times are 30 s and 5 s.

Sophisticated systems capable of supporting as many as 20 users will also be available. This System III class will incorporate a VS 7000-series processor, plus 16 Mbytes of main memory, printers, and optical, magnetic, and film storage devices. These machines will be priced from $750,000 to more than $1 million.

Current users of certain VS 5 or VS 6 processors can convert them into Integrated Image systems by adding an imaging work station, an optical scanner, an optical disk drive, and the Integrated Image software for an incremental cost beginning at $60,000.

In between an entry-level System I and the high-end System III, various configurations will be available that can include any or all of the following, based on a VS 65 processor and Integrated Image software: a 16-mm document camera to convert up to 500 pages/hr to microfilm for low-volume jobs; a high-volume microfilm camera system; an image-transfer controller to manage image transfers between the VS and mass-storage devices; cabinet-mounted optical drives that house up to five drives; an optical jukebox that can store as many as 3.8 million pages; and a robotic film-storage and -retrieval device.

INTEGRATED. Hardware includes a processor, terminal, optical disk, and scanner.

First shipments of entry-level systems are scheduled for the third quarter of this year. Early installations of high-end systems will begin in the fourth quarter; volume shipments are scheduled to begin in the first quarter of 1988.

–Lawrence Curran

Wang Laboratories Inc., One Industrial Ave., Lowell, Mass. 01851.
Phone (617) 459-5000 [Circle 342]

SUPERCOMPUTER RUNS UNMODIFIED FORTRAN

Multiflow Computer Inc.'s Trace family of 64-bit supercomputers uses two new technologies to bring supercomputer-level parallel-processing performance to existing, unmodified applications programs written in Fortran and C.

These new technologies are a very-long-instruction-word machine architecture and an optimizing-compiler software architecture called trace scheduling [*Electronics*, Sept. 18, 1986, p. 89]. They combine to give the Trace 7/200 a peak performance of 53 million instructions per second and 30 million floating-point operations per second (single-precision). The Trace 28/200 model peaks at 215 mips and 120 megaflops.

Very long instruction words pack many basic operations into single instructions. The trace-scheduling compiler packs as many operations as possible into each long instruction, using whatever elements are available. The Trace 200 models have more computational elements and therefore longer instruction words.

The Trace 7/200 is available now. A basic configuration costs $300,000. The company's 14/200 and 28/200 models will be available in the fourth quarter with prices ranging as high as $1 million.

Multiflow Computer Inc., 175 N. Main St., Branford, Conn. 06405.
Phone (203) 488-6090 [Circle 345]

EGA BOARD OFFERS 3 RESOLUTION LEVELS

Vutek Systems Inc.'s Enhanced Graphics Adapter board supports display resolutions of 752 by 410, 640 by 480, and 896 by 350 pixels, as well as all features of IBM Corp.'s EGA, Color Graphics Adapter (CGA), and Monochrome Display Adapter standards.

Vutek's model EGA also provides keyboard switching when changing from EGA to CGA modes and works with all popular software programs, such as Lotus Development Corp.'s Lotus 1-2-3.

Other features include a random-access-memory-based loadable character generator, 256 Kbits of on-board video memory, and an optional printer port.

Available now, the EGA board costs $559.

Vutek Systems Inc., 10855 Sorrento Valley Rd., San Diego, Calif. 92121.
Phone (619) 587-2800 [Circle 347]

HAND-HELD DIGITIZER CAN SCAN 150 FONTS

Saba Technology's Handscan digitizer allows users to enter alphanumeric information printed in more than 150 font styles from most common typewriters and computer printers directly into IBM Corp. Personal Computers and compatibles in approximately half the time needed to type it in.

Since the information is formatted for the computer's printer buffer, it can be used without modification by most popular spreadsheet software, including Lotus Development Corp.'s Lotus 1-2-3.

Handscan's character-recognition software offers an error rate of less than one mistake for each 1,300 characters read. Since the information appears on the computer's screen immediately, er-

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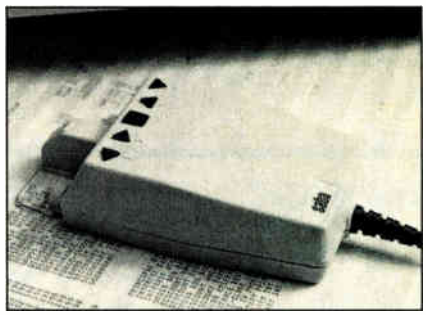

rors can be detected and corrected either by rescanning the data or by changing it through the PC's keyboard.

The Handscan is available now. It costs $650 in single-unit purchases.

Saba Technologies Inc., 9300 S.W. Gemini Dr., Beaverton, Ore. 97005.
Phone (503) 626-7050 [Circle 346]

SOFTWARE LINKS IBM PS/2 TO MINIS

Grafpoint's TGRAF software permits users to run minicomputer and mainframe graphics software using their IBM Corp. Personal System/2 computer as a terminal. Tektronix Inc. color graphics terminals are among those that the software emulates.

Grafpoint products are available for both serial and local-area-network communications environments.

The versions for standard graphics display with 640-by-480 resolution and 16 colors are available immediately at prices ranging from $495 to $1,995. The high-resolution versions with 1,024-by-768 resolution and 256 colors will be available in June; prices have not been set.

Grafpoint, 4340 Stevens Creek Blvd., San Jose, Calif. 95129.
Phone (408) 249-7951 [Circle 347]

PRINTER RUNS AT 2,100 LINES/MIN

Storage Technology Corp.'s 5000 Series Model 21 single-hammerbank impact printer provides high print quality and runs as fast as 2,100 lines/min.

It has 132, 150, and 168-character-width print positions and a replaceable stainless steel print band containing 576 characters. Characters are etched onto the band to provide high definition and long life.

The Model 21 is compatible with IBM Corp. 370, 3000, 4300, and 9300 systems and compatible processors and emulates IBM 3211, 4245, and 4248 impact printers. With the addition of a second hammerbank and dedicated electronics, it is field-upgradable to Storage Technology's dual-hammerbank Models 28 and 50. Available now, the free-standing printer costs $35,000.

Storage Technology Corp., 2270 S. 88th St., Louisville, Colo. 80028.
Phone (303) 673-5151 [Circle 348]

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ELECTRONICS WEEK

TWO FAIRCHILD FABS GO ON THE BLOCK

Schlumberger Ltd. is slimming its Fairchild Semiconductor Corp. subsidiary to an appropriate size for a management-led buyout. Its two most modern plants, submicron fab lines in Nagasaki, Japan, and Wasserburg, West Germany, are for sale. Fairchild president Donald W. Brooks says the fabs have yet to produce any revenue and as nonproductive assets are a drag on the sale of the company. Fairchild will rely on foundry agreements with Fujitsu and Seiko of Japan and Samsung of Korea and will continue to do its own assembly in Japan and Europe. Schlumberger recently abandoned its attempt to sell 80% of Fairchild to Fujitsu [*Electronics*, April 2, 1987, p. 31].

NORWAY GETS HUGE FIBER-OPTIC NET

FiberCom Inc. of Roanoke, Va., has landed a $3.5 million contract to supply Computer Connection A/S of Mjoendalen, Norway, with some 6,000 transceivers for what it claims will be the world's largest fiber-optic data-communications network. The Norwegian company will install FiberCom's WhisperNet, a fiber-optic extended-distance Ethernet local-area network, in about 125 of Norway's largest banking cooperatives. Some 850 bank branches will use the network, which will link self-service terminals based on NCR work stations to an NCR Tower multiuser computer.

APOLLO TAKES ON AI SOFTWARE

Apollo Computer Inc., of Chelmsford, Mass., and Inference Corp., Los Angeles, will jointly market the California-based company's expert-systems software on Apollo's family of 32-bit work stations. The alliance represents another shift of AI technology away from specialized AI machines and toward general-purpose work stations. Inference's software, the Automated Reasoning Tool, is a tool kit for developing expert systems that help executives make complex business decisions. Apollo's network-based work stations can run both AI and a range of general applications.

TI UNVEILS ITS INDUSTRY OUTLOOK

The worldwide semiconductor markets will grow 14% in 1987 to $30 billion, according to an annual industry outlook issued by Texas Instruments Inc. The Dallas company expects the U. S. chip market to grow 15%, reaching $10 billion, assuming that capital spending will strengthen in the second half of 1987. The outlook also assumes that end-equipment markets will see moderate growth and that inventories of chips will not surge as semiconductor purchases stay in line with system shipments. TI also expects Japanese chip markets to rise 10% in U. S. dollar volume. The company foresees 12% growth in Europe this year, while chip shipments in the Asia-Pacific region outside of Japan—still a small market segment—are expected to jump 35%.

ARETE AND PLEXUS READY TO MERGE

The prospective merger of privately held Arete Systems Corp. and Plexus Computers Inc., both of San Jose, Calif., will result in a maker of departmental computing systems based on Unix with sales of about $65 million a year. Both companies build systems that are based on the Motorola 68020 microprocessor and support Unix V.2. Arete supplies the high end of the market with a multiprocessor architecture capable of supporting up to 256 users. Plexus focuses on end users and value-added resellers. Plexus Computers will be the surviving company, and its president, Paul Klein, will be president and chief executive officer of the merged companies.

SUN BRINGS X WINDOWS ABOARD

Sun Microsystems Inc. is joining the many computer-system and work-station vendors that are backing Massachussetts Institite of Technology's X Windows user interface as an industry standard [*Electronics*, Jan. 22, 1987, p. 58]. Sun is merging X Windows with its own NeWS window system to provide a unified window system for its customers. Many companies also license Sun's NeWS, making it a potential competitor as an industry-standard window system. Now, with Sun backing X Windows and merging it into NeWS, companies can rally around a more broadly established standard.

E-SYSTEMS GROWTH SPURS HIRING

Defense electronics supplier E-Systems Inc. is going on a major hiring spree. The Dallas firm, which has set its sights toward nearly doubling its sales to $2 billion by 1990, expects to add about 5,000 jobs to its current 15,000-worker payroll over the next three years. About 1,000 of the new hires will be made in 1987, with nearly half of them being engineering and scientific positions.

SOFTWARE-TOOLS ALLIANCE FORMED

Northwest Instrument Systems Inc. of Beaverton, Ore., and Microtek International of Taiwan may bring about the end of the era of stand-alone tools for microprocessor software development. The two companies have formed a strategic alliance in which Northwest will market Microtek's in-circuit emulators in the U. S. The two companies also intend to develop interfaces that will enable Microtek's in-circuit emulators and Northwest's work stations for software analysis, as well as compilers from other suppliers, to be integrated into a package that handles the complete process of computer-aided software engineering. The first such systems should be available by early 1988 and will support a variety of microprocessors, including the two best-selling 32-bit engines: Motorola's 68020 and Intel Corp.'s 80386.

INDUSTRY MERGERS ON THE RISE

Acquisitions and mergers in the computer, software, services, and information industries totaled 342 in 1986, up 18% from 290 a year before, reports the Cerberus Group Inc. of Frenchtown, N. J. The company attributes this record increase to tax-reform legislation. The total value of all U. S. acquisition and merger transactions in 1986 was $4.66 billion, down 6.8% from the record $5.0 billion in 1985. Acquisition of publicly traded sellers numbered 78, down 18% from 95 in 1985. Privately owned sellers numbered 184, up 3% from 135 the year before.

CDC LOWERS CYBERPLUS PRICES

Control Data Corp. is bowing to competitive pressure in the increasingly crowded parallel-processing business by slashing prices up to 44% on its Cyberplus parallel processor. Pricing on a single full-blown Cyberplus processor equipped with 512-K 64-bit words of memory and 32/64-bit floating-point capacity is now set at $765,000, compared with the previous $1.365 million list price. "We've already been discounting [the Cyberplus] by about 25%, so effectively we've decided to get the list price more in line with the street price," a Control Data spokesman explains.

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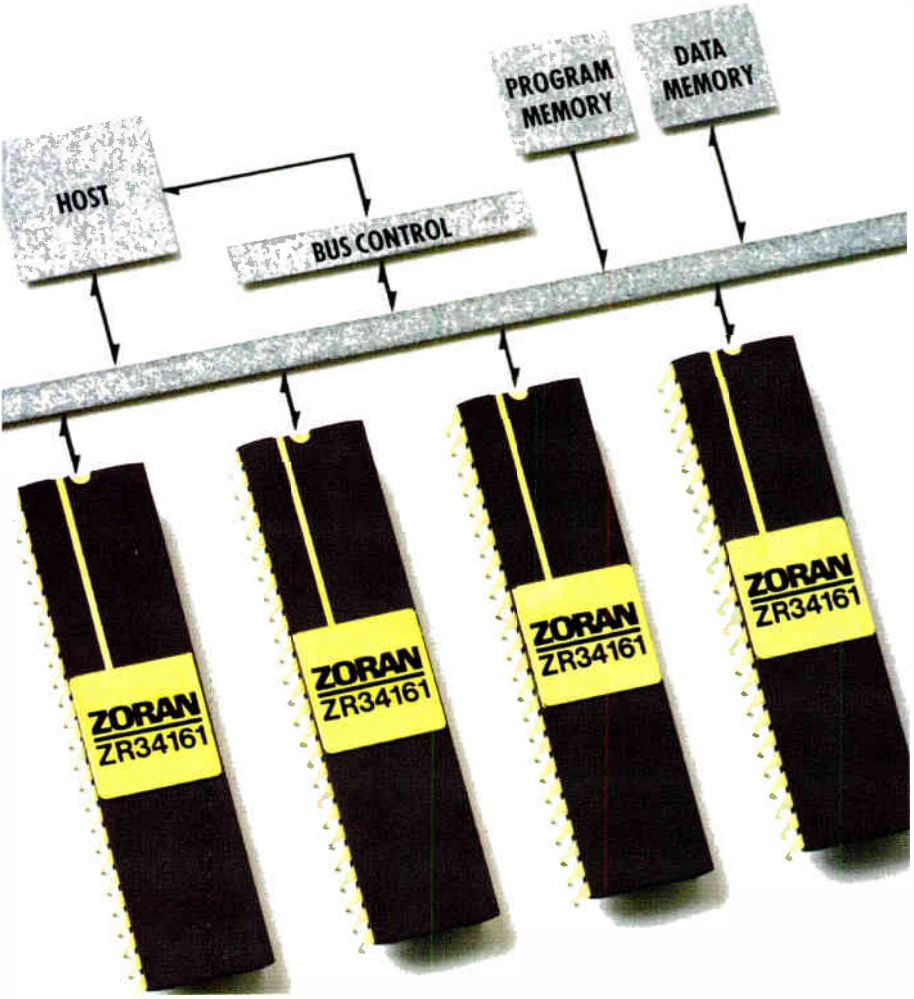

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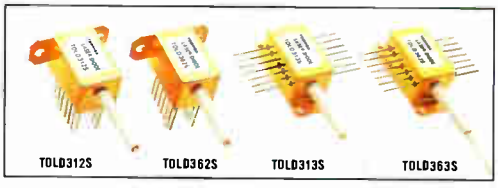

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