SMART MEMORIES START EATING INTO JELLY BEAN MARKET/65

TI CROSSBAR IC CUTS THE COST OF PARALLEL PROCESSING/72

A McGRAW-HILL PUBLICATION SIX DOLLARS FEBRUARY 5, 1987

Electronics

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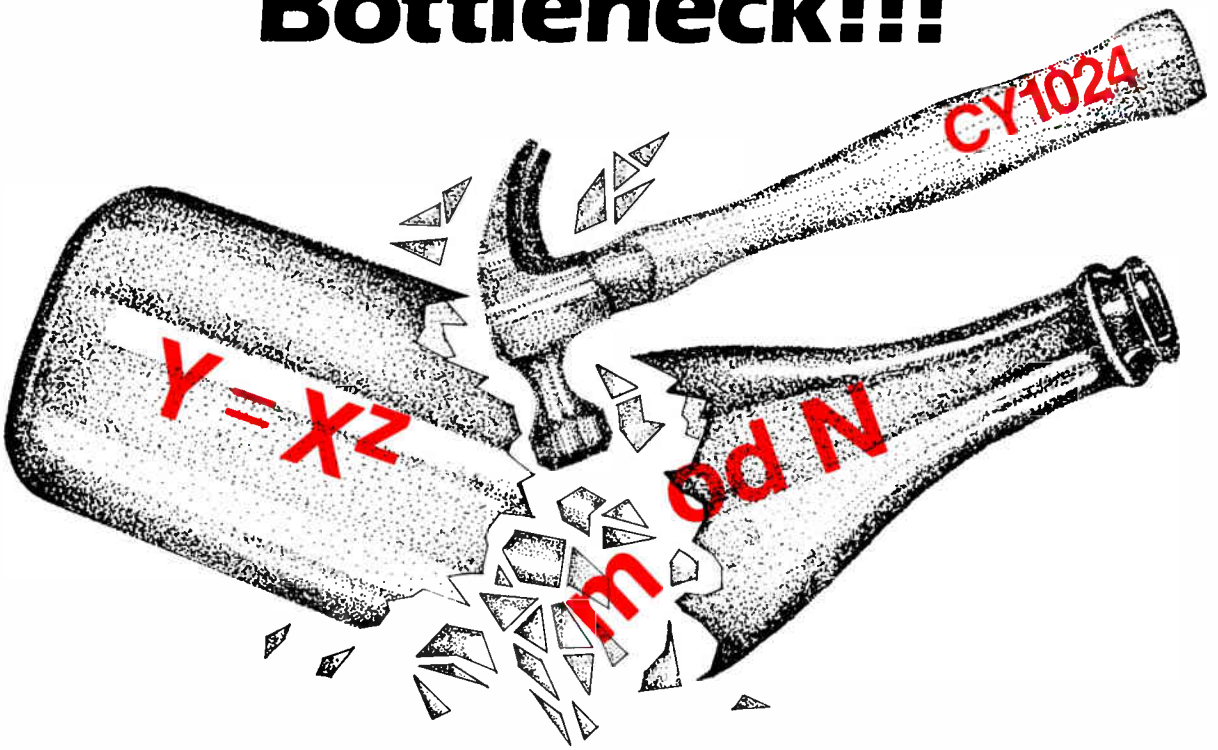
HERE COME THE TOOLS TO DESIGN 50,000-GATE ASICs

PAGE 55

CYLINK Breaks the Key Management Bottleneck!!!



Computing this function rapidly has been a major bottleneck in implementing public-key cryptographic algorithms such as CYLINK's SEEK™, Diffie-Hellman, and RSA. CYLINK has changed all that with its low power key-management processor chip, the CY1024. A single CY1024 chip can perform a modular exponentiation using 1028-bit integers in less than one second!

TRY THAT ON WHATEVER PROCESSOR YOU HAVE!!!

Unless you happen to have a CRAY or something comparable, it will take you hundreds or thousands of times longer. And just in case 1028 bits isn't enough for your needs, you can stack up to sixteen CY1024 chips together to perform exponentiations up to 16,448 bits long.

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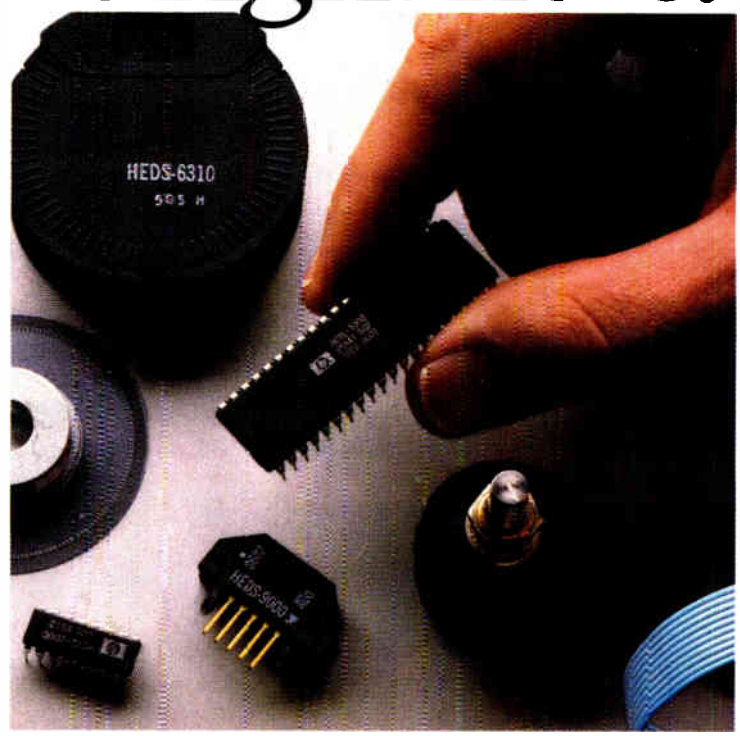

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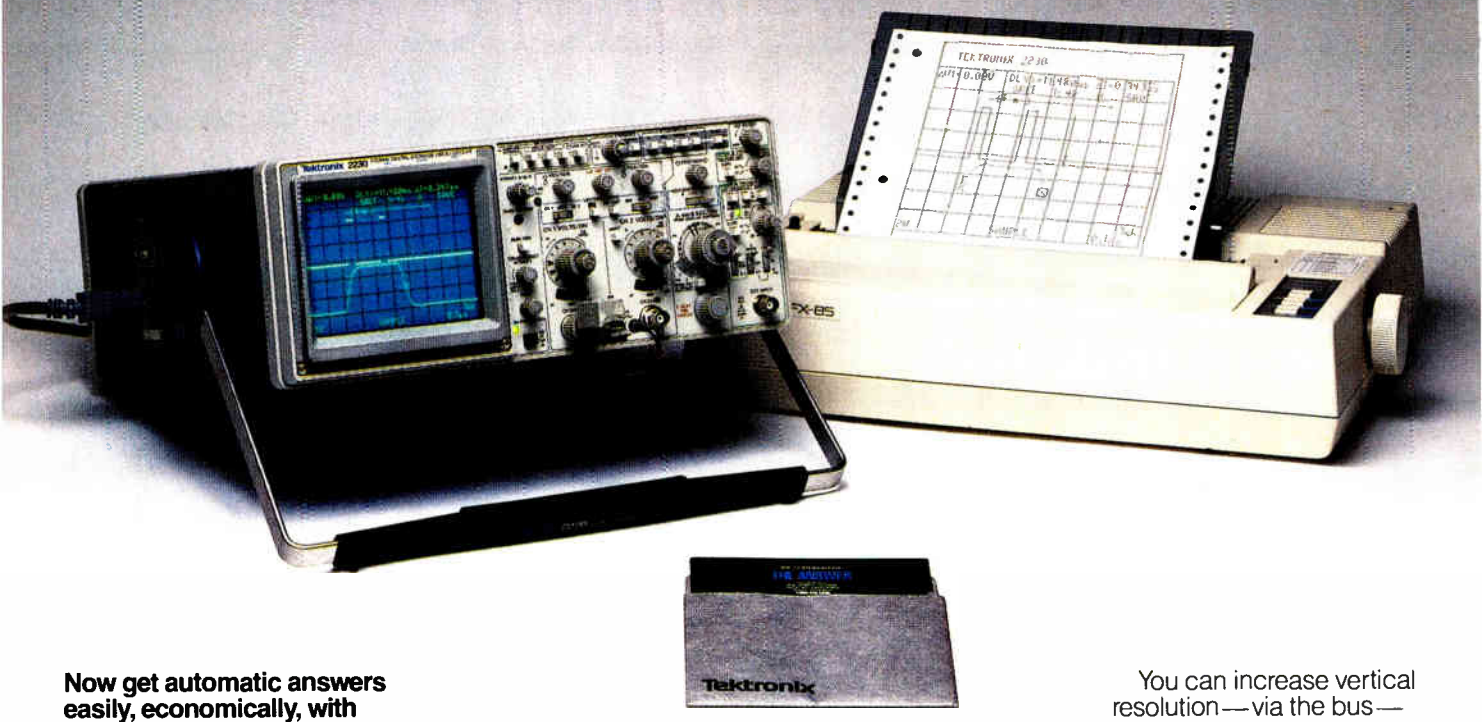

Now get automatic answers easily, economically, with immediate hard copy output. The 100 MHz Tek 2230 or 60 MHz 2220 are high-performance, high-value digital storage oscilloscopes. Equip either with an optional GPIB or RS-232-C interface and digitized data can be ported to your PC, sent over phone lines, or directed to your printer or plotter for hard copies.

With either option the 2230 includes battery-backed memory that provides 26K of keep-alive CMOS memory—for storing up to 26 waveform sets.

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Features	2230	2220
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Max. Sampling Speed	20 MS/s	20 MS/s
Record Length	4K/1K (selectable)	4K
Save Reference Memory	One, 4K Three, 1K	One, 4K
Vertical Resolution	8 bits 10 bits (AVG mode) 12 bits (AVG mode over bus)	8 bits
CRT Readout	Yes	No
Cursor Measurements	Yes (storage mode)	No
GPIB/RS-232-C Options	Yes ($850)	Yes ($550)
Battery-Backed Memory (save 26 waveform sets)	Yes (inc. with 2230 communications options)	No
Price	$5150	$4150

You can increase vertical resolution—via the bus—from 8 to 12 bits with signal averaging. And Tek software is available to help you get the most from your systems configurations.

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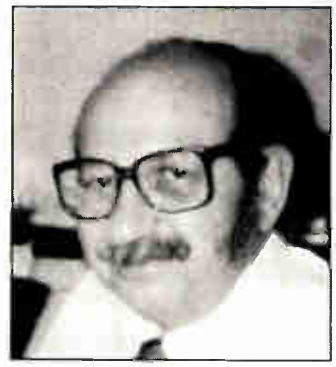
Electronics

PUBLISHER'S LETTER

What's new in laboratory instruments? We have the up-to-the-minute answer on p. 89 in the first of a new series of product special reports that will combine in-depth looks at the state of the art and the state of the industry in different sectors of electronics. These "What's new in . . ." features will cover the markets, the players, and the trends in technology.



SIDERIS: Providing an inside look at the lab-instrument industry.

These product special reports illustrate one of *Electronics'* great strengths. We have the unique know-how and the people to look at technology from the standpoint of business and from the standpoint of technology. That is an important and valuable plus for the reader, particularly in these days when the two are so closely meshed that it is difficult to understand one without also understanding the other.

We are also proud of our pioneering approach, in which we schedule such reports as regular events. That displays another strength of the magazine: our editors have the background and knowledge to take both the macro and micro views when they lift the covers off a subject and peek into all the corners. We are able to do this routinely; other magazines and newspapers that cover the electronics industry try to do it a few times a year.

This inaugural report was written by test instruments editor George Sideris in San Mateo and edited in New York by new products editor Jack Shandle and associate managing editor Ben Mason. The industry survey that led to the report was started last fall by Jonah McLeod, also based in San Mateo, who now specializes in coverage of computer-aided design and engineering. George, who took over the instruments slot from Jonah in December, worked his way through Jonah's 5-ft. shelf of material on instrument developments and economic trends through the Christmas and New Year's holidays to get up to speed, and then began talking to instrument makers to complete the report.

He found that while the instruments sector of the electronics industry appears to be parked on a low-growth plateau, there's still plenty of growth at the leading edge. High-performance digital-storage oscilloscopes and other new instruments are coming on strong and bumping older instruments off the bench, he reports, because engineers now developing advanced electronic products need tools that are faster and smarter than conventional lab instruments. "I focused the report on this new generation of instruments because I'm convinced that they'll dominate the lab-instrument market in the future," George says.

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FEBRUARY 5, 1987

Electronics

NEWS

INSIDE TECHNOLOGY

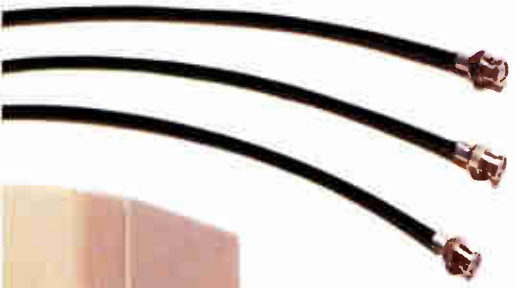
COVER: NAVA BENJAMINI

PAGE 55

NEW PRODUCTS

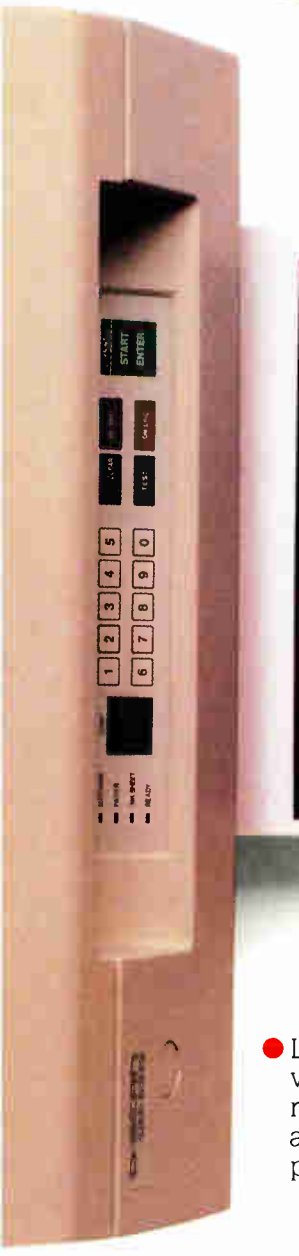
DEPARTMENTS

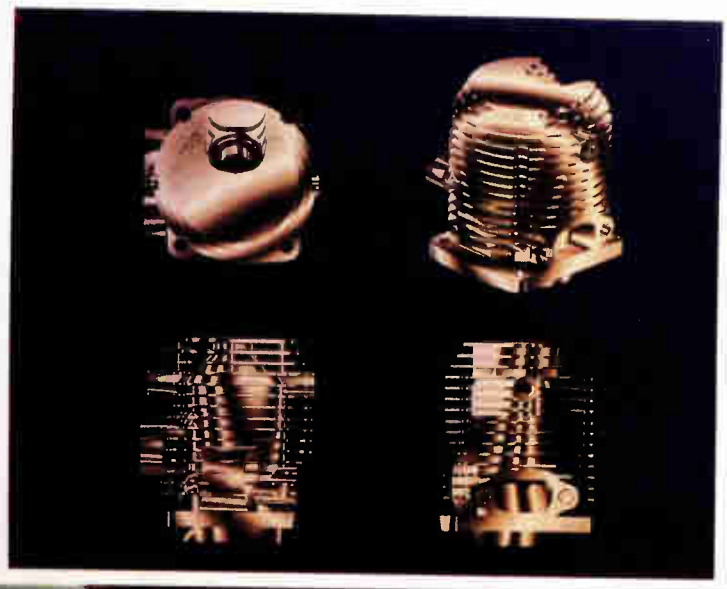
- Both parallel and RS-232 interfaces are supported by a wide selection of software.

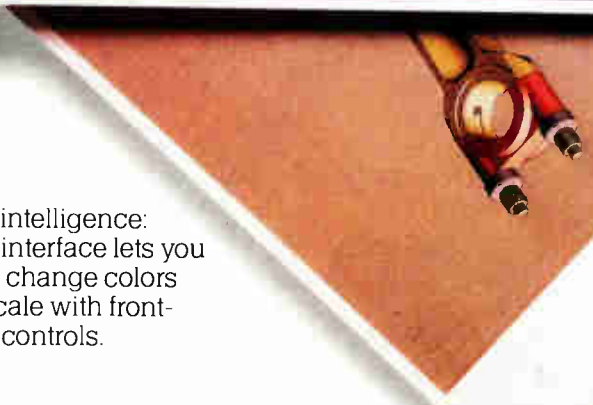


- Easy video interfacing—over 150 interfaces are supported. No need to write software.

- Accurate shading for realistic, detailed solids; work with 4,912 colors.







- Local intelligence: video interface lets you rotate, change colors and scale with front-panel controls.

- Crisp, clean lines for highly detailed drawings.

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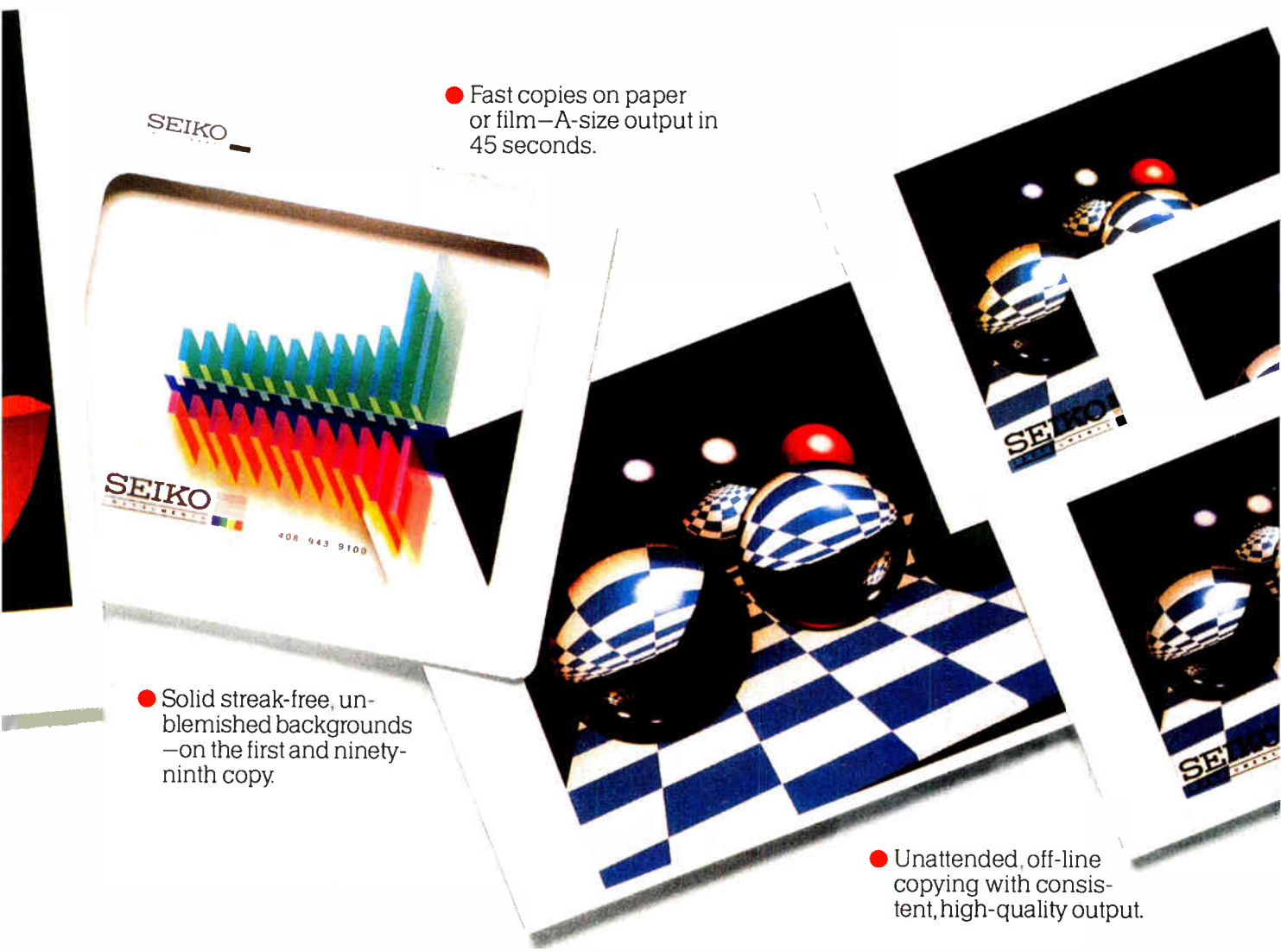
SEIKO INSTRUMENTS



- Fast copies on paper or film—A-size output in 45 seconds.
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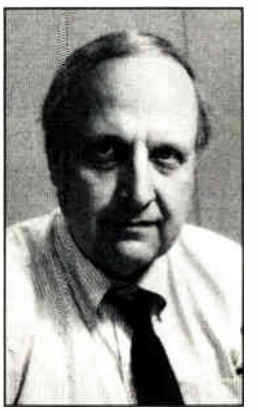
The days of the automated monster plant, the kind the Japanese built to grab market share, may be numbered, and U.S. chip makers have a chance to catch up



If some leading consultants are right in their latest observations, the outlook for U. S. chip makers may not be as bleak as some people predicted. It now appears to the experts that the days of the highly automated monster plant—the expensive kind that the Japanese built by the dozens to grab market share from American chip makers in the early 1980s—are numbered. This should be good news for the U. S. companies since they never did build any wafer fabs that size. "For the first time in 10 years, the U. S. has a chance to catch up," declares consultant Jerry D. Hutcheson, founder and CEO of VLSI Research Inc.

The Japanese have now concluded, he says, that the economies of scale for going to 8-in. wafers (see p. 29), as well as for profitably utilizing their many existing monster plants, are just not there. In fact, Hutcheson maintains the Japanese are now beginning to shut down these $150 million monster plants that run 7,000 to 10,000 6-in. wafers a week. And, he adds, they built 40 of them! While they aren't talking now, Hutcheson says that the Japanese learned a lesson, and they won't build the large monster lines again—even when the market turns up.

While these big plants clobbered the smaller U. S. factories in the high-volume markets of the booming early 1980s, when the downturn came they proved to be too costly to operate at less than capacity. Running a monster plant at 2,500 wafers per week, or just 25% of capacity, turns out to be "enormously unprofitable," Hutcheson says. Now the Japanese are turning back to the 2,500 wafers-per-week plants.

Automation just isn't cutting it now for semiconductor manufacturing. The Japanese found that their monster plants were highly inflexible and could not easily be adapted to turning out smaller-lot sizes of more variable product types. In contrast, U. S. makers have relied on smaller, more flexible plants, Hutcheson notes, that run up to 5,000 wafers a week. Hutcheson's VLSI Research will not recommend a single computer integrated manufacturing approach today to the semiconductor industry. "A practical system has yet to be designed," he insists. He points out that there are many areas that automation is failing to address, including machine uptime and machine mean-time-between failure.

ROBERT W. HENKEL

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Motorola BiMOS provides semicustom solutions that other technologies often can't.

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- **Input translator/buffer delays (typ)**—
  TTL—2.0 ns, ECL—3.3 ns
- **Internal gate delays, 2-input NAND**—
  F.O.=1, 0 mm metal—0.8 ns
  F.O.=5, 2 mm metal—1.2 ns
- **Delay deg. per unit load**—275 ps/pF
- **Output translator/buffer delays (typ)**—
  TTL 8 mA @ 50 pF load—5.5 ns
  ECL 50 ohm @ 50 pF load—1.25 ns
- **D-type flip flop toggle freq.**—200 MHz
- **Power dissipation (typ) per active gate**—
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- **Maximum output sink, TTL**—
  8 mA, 24 mA (single cell)
  48 mA, 64 mA, 72 mA (multiple cell)
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LETTERS

Don't stop production!

To the editor: In your story "Motorola to Drop Some Discretes" [*Electronics*, Jan. 8, p. 129], you state that Motorola's Discrete Semiconductor Group had asked customers "to stock up on a large number of small-signal discrete devices before it shuts down production lines" Some of your readers have interpreted this to mean that Motorola is stopping production of small-signal devices. This is not only inaccurate, but also totally opposite to Motorola's strategy.

Motorola has a worldwide total of nearly 60,000 device types, an unwieldy number to deal with and still meet market demand for short lead times and on-time delivery. Approximately 10,000 device types will be pruned from the Discrete Group's portfolio. Some will have direct replacements with tighter tolerances; some can be replaced by better device types from the same generic family; others may be available for lifetime buys, since the die process and/or the package may be discontinued. Motorola will assure all customers that they will either be offered a viable replacement device or given the opportunity to place a lifetime buy.

Danny L. Schnell
Motorola Discrete and Special Group
Phoenix, Ariz.

Mask repairing by laser

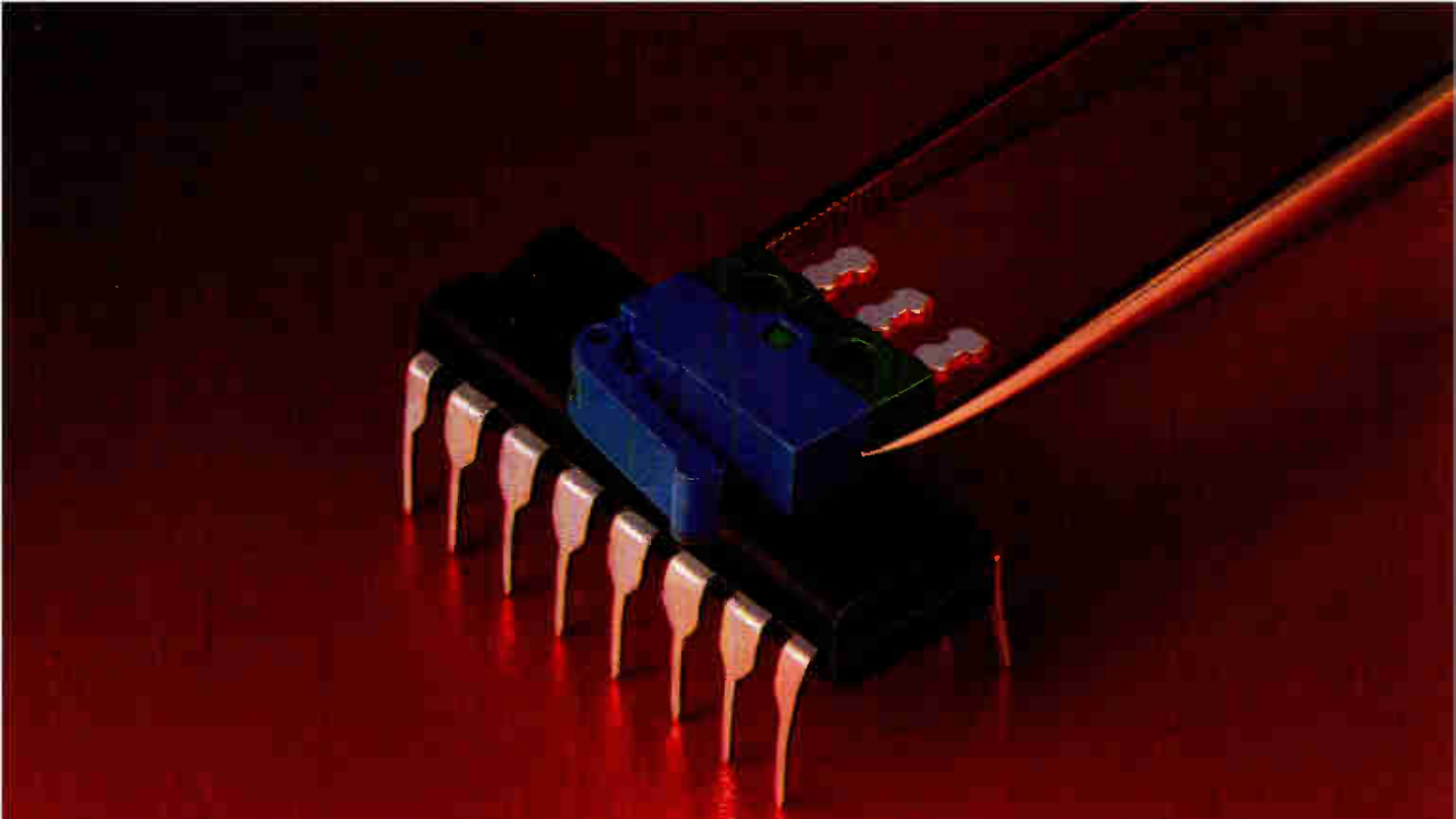
To the editor: Your Jan. 8 issue of *Electronics* [p. 96] comments on a growing segment of the semiconductor equipment market, focused ion-beam mask-repair systems. An even faster-growing segment of the mask-repair equipment business is based on laser technology.

In May 1985, Quantronix and Micrion announced their versions of mask-repair systems designed to meet the requirements for repair of clear defects and improved repair resolution. During the next 18 months, mask makers have chosen laser-based repair systems over focused ion beam by more than 3-to-1. Quantronix has delivered more than 25 laser-based DRS II Mask Repair Systems, including multiple installations at several locations.

William I. Kern
Vice President Marketing
Quantronix Corp.
Smithtown, N. Y.

Credit where credit is due

Correction: *The single-board 1750A computer described in "RCA crams three boards' circuitry onto one"* [Electronics, *Nov. 27, 1986, p. 19*] *was developed by the RCA Missile and Surface Radar Division, not the Government Systems Division. Lutz Engineering Corp. also contributed to the project.*



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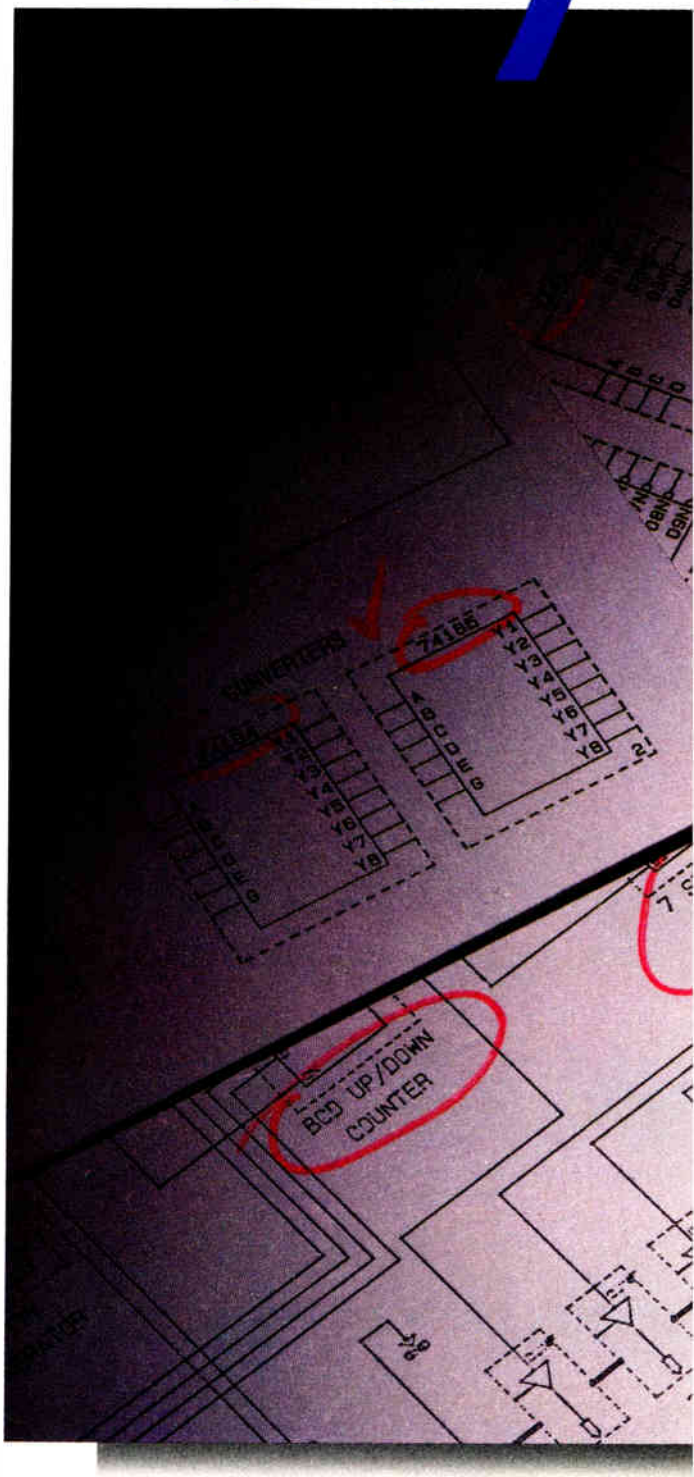
What's more, you won't get stuck with custom leadtimes and high inventory costs because our EPLDs are standard, off-the-shelf products.

Note, too, that the EP1800 is ideal for military (especially if you're still in the bidding process), instrumentation and telecommunications applications. You get high density, low power, TTL speed, fast prototyping (even prototyping for gate arrays) and no upfront development charges.

So call today to learn more. Because if you talk TTL, you can now talk affordable VLSI. With the easiest terms in the business.



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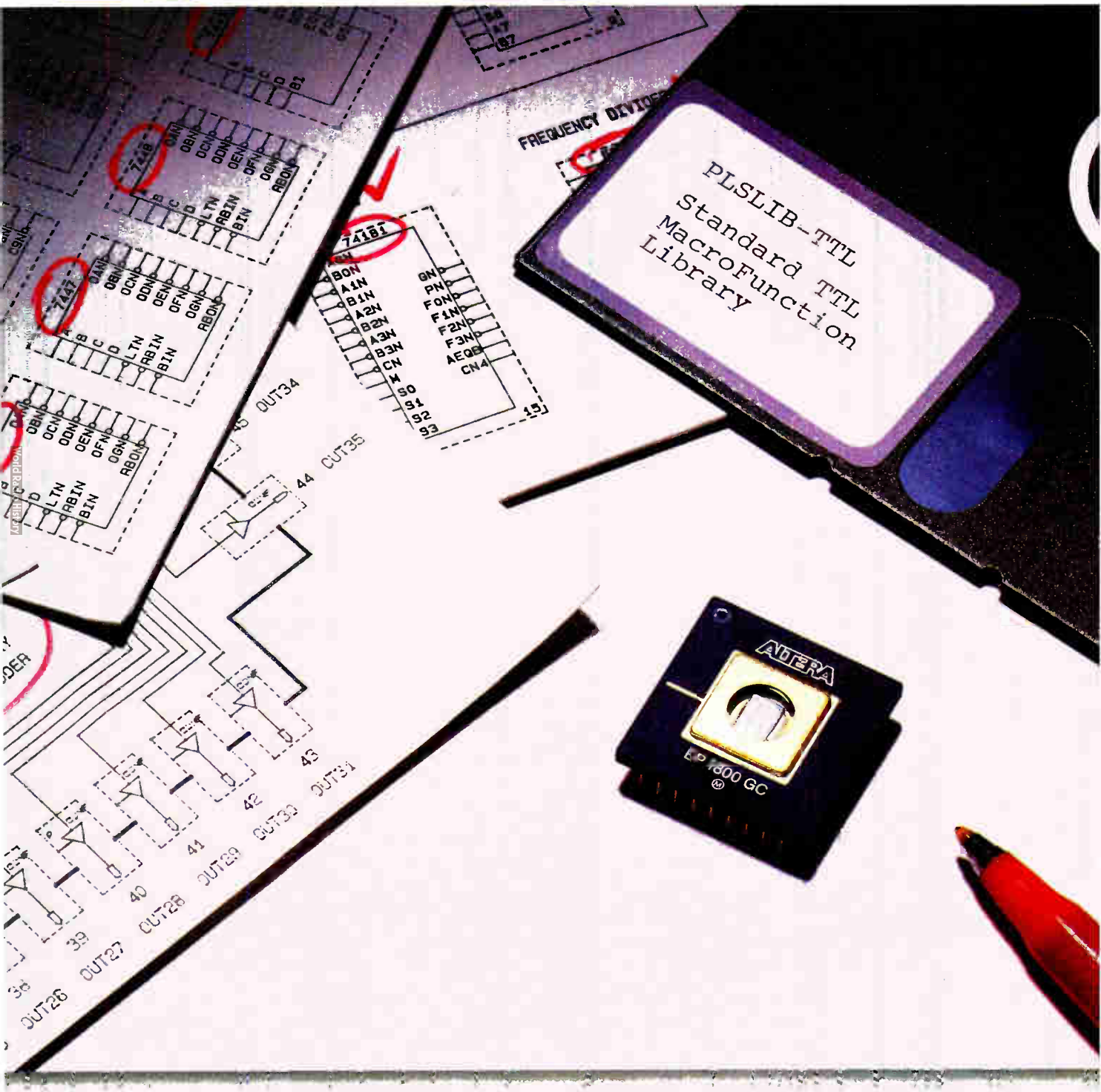

Circle 15 on reader service card

A WORD ABOUT COMPATIBILITY

Some things work together. Some things don't.

Introducing the 3100 Performance Test System from Support Technologies. A new functional automatic test system that lets you standardize testing across the board—from the design engineer's workbench, to the manufacturing floor, to service repair centers.

The 3000 Portable Test System

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SUPPORTECHNOLOGIES

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ELECTRONICS NEWSLETTER

IBM SHIFTS 1-Mb DRAM PRODUCTION TO 8-in. WAFERS...

Even as many chip makers reconsider their expensive moves from 3-in. and 5-in. silicon wafers to 6-in. fab lines (see p. 29), IBM Corp. is forging ahead and gearing up the first production line for 8-in. wafers. IBM already has a small line running at its fab in Essex Junction, Vt., and the company plans to gradually shift all production of its newest 1-Mb dynamic random-access memory, a high-speed device developed for its Sierra line of mainframe computers (see p. 45), onto a full-production 8-in. line. The wafers can hold three times as many devices as the 5-in. wafers IBM generally uses. Each wafer will contain 440 of the n-MOS DRAMs, which use 1-μm geometries more extensively than IBM's previous megabit DRAM. The new chip also uses silicon-gate technology instead of the metal-gate process used in the earlier chip and is nearly twice as fast—maximum access time is 80 ns. □

..AND JOINS NEC IN THE RUSH TO BUILD 4-Mb DRAMs

Just as suppliers are beginning to mass-produce 1-Mb dynamic random access memories, IBM Corp. and NEC Corp. are positioning themselves as leaders in the next-generation 4-Mb technology. IBM researchers are scheduled to describe their success in a paper at the International Solid State Circuits Conference later this month in New York. NEC, meanwhile, is incorporating trench capacitors in its 1-Mb devices because it believes the technology will be essential in 4-Mb DRAMs. By using trench capacitors now, NEC gets a head start on the technology without adding significantly to its production costs, the company says. NEC now produces about 200,000 1-Mb DRAMs per month, and it hopes to become the leading Japanese supplier by year end, with monthly production reaching 2 million chips. □

WILL THE SIA FOLLOW UP DEC'S STUDY ON PREGNANT CHIP WORKERS?

The semiconductor industry continues to see fallout from the Digital Equipment Corp. report released late last year that reported that women at one of DEC's plants face significantly higher chances of miscarriage than other women [*Electronics*, Jan. 8, 1987, p. 24]. Now the Semiconductor Industry Association is apparently considering an industrywide study of the health of chip-production workers, according to a well-placed SIA source. An SIA task force got a special briefing in late January from researchers at the University of Massachusetts School of Public Health, which conducted the DEC study, and will report back to the SIA board of directors in March. At that time, the source says, the SIA board will most likely discuss a proposal for a wider study covering as many as 2,000 pregnancies at several plants. The DEC study covered only 35 pregnancies at one plant. The SIA study would have to be done by an independent agency, and could take two years and cost up to $4 million to complete. The SIA now monitors only acute medical problems of workers, and an independent study of the effectiveness of that system by the University of California, Davis, is due in April or May. □

INFATUATION WITH HIGH-PURITY MATERIALS MAY BE POINTLESS

The industry quest for ever-higher levels of purity in gases, chemicals, and solid materials is approaching "witch-hunt" proportions, says Daniel J. Rose, president of Rose Associates in Los Altos, Calif. He says demand has pushed analytical measurement technology to the limits. Chip makers may well be seeking higher purity materials than they really need, Rose says. Although purity levels of better than one part per billion are required for many solid materials, in some cases customers are seeking purity levels as much as 10 to 100 times greater. □

ELECTRONICS NEWSLETTER

STORM BREWS OVER STANDARDS FOR 5¼-in. WRITABLE DISKS

A storm is brewing over standards for 5¼-in. writable optical disks, as the backers of continuous-servo and sampled-servo methods each try to persuade Asian, U. S., and European standards committees to see it their way. A Japanese standards body avoided the issue by backing both [*Electronics*, Jan. 8, 1987, p. 48], but the American National Standards Institute's X3B11 committee will try to come up with a single format at a special meeting Feb. 17 in San Jose, Calif. "It's a sensitive issue, because a lot of money is riding on the outcome," says committee chairman Joseph Zajaczkowski of Cherokee Data Systems, Boulder, Colo. "But the committee has decided to work for a single set of parameters." A major point of controversy is the potential for reference-clock problems in the sampled-servo method. However, the continuous-servo approach also has a drawback: it suffers from self-clocking errors. Some 16 companies, including Hewlett-Packard and Maxtor in the U. S. and Fujitsu, Matsushita, Mitsubishi, and NEC in Japan, support the continuous-servo approach. A smaller but equally powerful group, led by Japan's Sony Corp. and Philips International NV of the Netherlands, favors the sampled-servo method. Hitachi Ltd. has product groups for both methods, and the European International Standards Organization has discussed the issue but has made no move to support either format. □

TEKTRONIX IS EXPANDING INTO THE HIGH-END PC-BOARD BUSINESS

Tektronix is taking aim at the high end of the $2 billion printed-circuit-board market. Tek PCB, a new division in Forest Grove, Ore., is already supplying about 50 customers with fine-line multilayer boards. The division's fully automated facility can produce up to 1.6 million ft² of pc boards annually, and it boasts a 98% on-time delivery rating, one of the best in the industry. Although Tektronix is its largest customer, accounting for 80% of sales, Tek PCB plans to boost external business to 50% by 1991. □

TI CREATING FIFTH IC FOCUS AIMED AT ADVANCED LINEAR CHIPS

Texas Instruments Inc. will soon disclose that it has designated advanced linear integrated circuits as its fifth IC-product focus area. The advanced linear thrust will include digital signal processors, network devices, interface chips, and high-performance operational amplifiers. It joins four other strategic focus programs aimed at concentrating more of TI's semiconductor investments into more profitable, high-growth markets by 1990. In a move to help revive the Dallas-based firm, president Jerry R. Junkins last year launched the focus program with a goal of having 50% of the company's chip business in four areas: application-specific ICs; application processors and microcontrollers; military circuits; and very large-scale integrated logic, both bipolar and CMOS. The addition of advanced linear ICs will increase that figure by a still unidentified amount. □

APPLE LAYS THE GROUNDWORK FOR ITS OPEN-MAC STRATEGY

Apple Computer Inc. separated fact from fiction last week with the first in an expected flurry of new products that will culminate in the debut of new open Macintosh hardware this spring [*Electronics*, Jan. 8, 1987, p. 98]. The products are aimed at making the Mac more competitive in the business market, dominated by IBM Corp. AppleShare, an $800 software communications package, allows the Mac to act as a network file server, enabling it to share data with IBM-compatible personal computers. The $400 AppleTalk PC plug-in card allows IBM machines to print documents on Apple's laser printer. □

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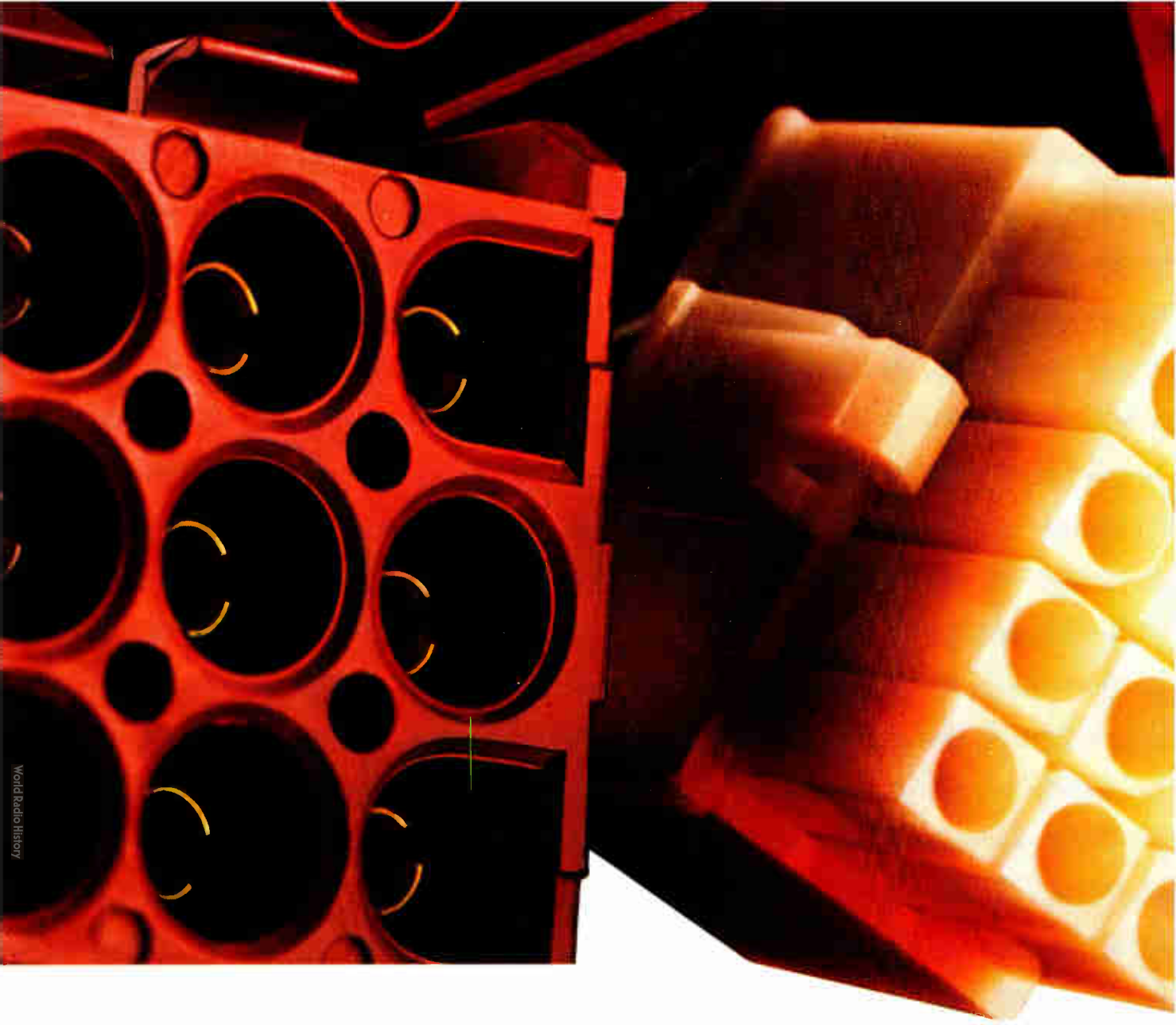

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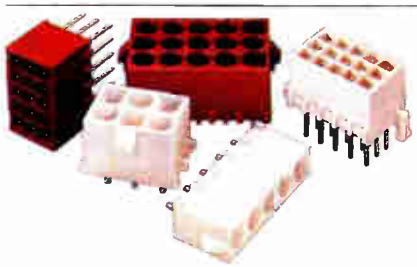
AMP Interconnecting ideas



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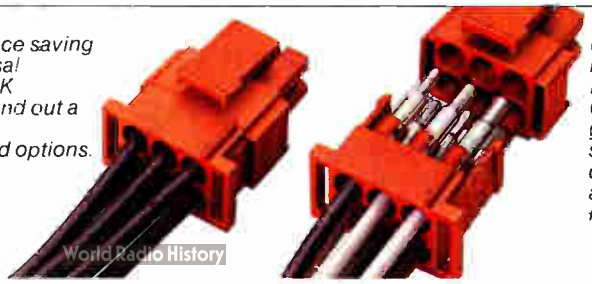

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PRODUCTS NEWSLETTER

NETWORK PROCESSOR GEARED TO EVOLVING OPEN NETWORK ARCHITECTURE

Avanti Communications Corp. is making its play to dominate the market for equipment meeting the Federal Communications Commission's unrestricted telecommunications service standard—Open Network Architecture—with a network processor that supports just about all existing and proposed telecommunications standards. The company's Open Network Exchange for 1.544 Mb/s-digital-line networks, or T1 lines, targets large, information-intensive organizations. Besides being able to network with gear using technologies such as pulse-code modulation and adaptive differential-pulse-code modulation, Avanti's Open Network Exchange has a three-dimensional cross-connect unit to handle subrate data multiplexing for transmission channels carrying as little as 2.4-K baud. Preliminary standards for the integrated services digital network are also supported. Prices will depend on configurations. A low-end version will sell for about $35,000 when deliveries start in May, estimates George Kushin, senior vice president of sales and marketing. □

INTEL'S ERASABLE LOGIC PUTS THE ELBOW ON PALs

In a move that could challenge the dominance of Monolithic Memories Inc.'s programmable array logic architecture, Intel Corp. this week introduced an erasable programmable logic device. Designed to implement bus-interface functions, the 5CBIC allows designers to replace as many as four small- or medium-scale-integration standard components and two 20-pin PALs. Fabricated using Intel's advanced CHMOSII-E process, the chip is the first proprietary EPLD product Intel has developed since the Santa Clara, Calif., company acquired the CMOS-based technology from Altera Corp. a year ago. Besides eight programmable macrocells, the chip has user-programmable logic supporting synchronous and/or asynchronous real-time data transfer. The 44-pin chip is available now in plastic leaded chip-carrier packaging and is priced at $18.50 each in 100-unit sample quantities. □

KONTRON'S LOGIC ANALYZER DOUBLES AS PC AT

The tables have turned on personal computers that have been invading the test instrumentation market configured with add-ons that make them bench instruments. Kontron Electronics Inc.'s PLA 286 Personal Logic Analyzer can serve as the host computer of an instrumentation system or as a portable personal computer. Built around a ruggedized, 10-MHz version of the IBM Corp. Personal Computer AT, the Mountain View, Calif., company's basic analyzer costs $7,400 with forty-eight 20-MHz state-and-timing channels, a flexible-disk drive, and 1 megabyte of random-access memory. Prices range up to $15,900 for a fully expanded system with ninety-six 20-MHz channels, sixteen 100-MHz timing-analysis channels, a 20-megabyte hard-disk drive, a fold-out keyboard, and MicroSoft Corp.'s MS-DOS operating system. □

NEW SUPERMINI FROM PRIME OFFERS MORE BANG FOR THE BOX

Prime Computer Inc.'s latest 50 Series superminicomputer will pack up to 35% more computing power than its predecessors with no increase in cabinet size. The 32-bit 2755, which is smaller than a standard four-drawer file cabinet, supports up to 128 terminals directly connected to the host and 63 remote terminals. When used as a platform for computer-aided design and engineering, the 2755 supports up to six work stations. In its basic configuration, it includes 16 Mb of main memory, 64-K of cache memory, and 4.2 gigabytes of on-line disk storage. The Natick, Mass., company says the new computer will execute 1.6 million instructions/s. Available now, the 2755 is compatible with previous 50 Series models. It costs $95,050 to $133,200. □

PRODUCTS NEWSLETTER

SOFTWARE MAKES IT EASIER TO TEST FOR COMPLIANCE TO MAP STANDARDS

Designers of equipment using the Manufacturing Automation Protocol factory-communications standard now can pretest for MAP compliance with a software package. As expected [*Electronics*, March 31, 1986, p. 15], the Industrial Technology Institute, Ann Arbor, Mich., is making its MAP test software available for work stations from Sun Microsystems Inc. The package, which tests nine protocols used in the upper five layers of MAP version 2.1, is compatible with the 4.2bsd version of AT&T Co.'s Unix. Available now, a single-site license sells for $12,000 to members of the Corporation for Open Systems, which funded development. Non-members pay $20,000. □

MICRO LINEAR 3-CHIP SET MAKES UP CLOSED-LOOP SERVO FOR WINCHESTERS

Micro Linear Corp.'s three integrated circuits for high-performance 5¼-in. Winchester disk drives implement a closed-loop servo system and replace custom-designed discrete circuits that ate up precious board real estate. The ML401 servo demodulator decodes read/write-head position data; the ML402 provides drive signals for the voice coil actuator; and the ML403 holds the read/write head on track and accelerates it to the desired track position during a seek operation. Samples of the ML401 and ML402 are available now. The ML403 will be ready in March. In 1,000-unit orders, the ML401 costs $9 apiece; the ML402, $5.70; and the ML403, $8.10. □

TEKTRONIX LOGIC ANALYZER OFFERS HIGH-END FEATURES AT LOW-END PRICES

Tektronix Inc. has upgraded low-cost logic analyzers with instruments that offer as many as 12 modes of interactive triggering, plus state analysis on 48 channels operating at 25 MHz or on 12 channels operating at 100 MHz. These features were formerly found only in instruments costing about $12,000, says the Beaverton, Ore., company. Tektronix's Model 1225 is priced at $5,295 and its Model 1220 sells for $3,995. The 1225 can analyze an 8-bit microprocessor on 32 channels and simultaneously perform timing analysis on its remaining 16 channels. Model 1220 offers the same capability for a total of 32 channels. Both models are available four weeks after order.□

BURR-BROWN'S FIBER-OPTIC MODEM EXTENDS RS-232-C LINKS TO 3.5 km

Burr-Brown Inc.'s high-speed fiber-optic modem outdistances the 50-ft limit of conventional metal cable for RS-232-C connections by a factor of about 300. The LDM80 supports 3.5-km connections and transmission rates up to 19.2-K baud. It can be used with most fiber-optic cable sizes and is completely powered by the host computer's RS-232-C port signals, eliminating the need for a separate power supply. Maximum connection length is achieved by using glass cable having a 100-μm core and an attenuation of 4 dB/km. The 3.5-by-1.7-by-0.8-in. modem is small enough to mount on the back of a video display terminal. Available now, the LDM80 costs $98. □

HP'S ASIC VERIFIER SPEEDS DEVELOPMENT CYCLE

An application-specific integrated-circuit verifier from Hewlett-Packard Co. speeds the turnaround time from prototype chip to production with high-speed processing and real-time response. The HP81810S IC Design Verification System boasts a maximum data-transfer rate of 50 MHz and a 16-K vector memory that allows real-time comparison of actual versus expected response. It handles devices with as many as 256 pins and has 100-ps resolution of clock pulse and delay time. The HP81810S costs between $40,000 and $250,000, depending on configuration, and is available now.□

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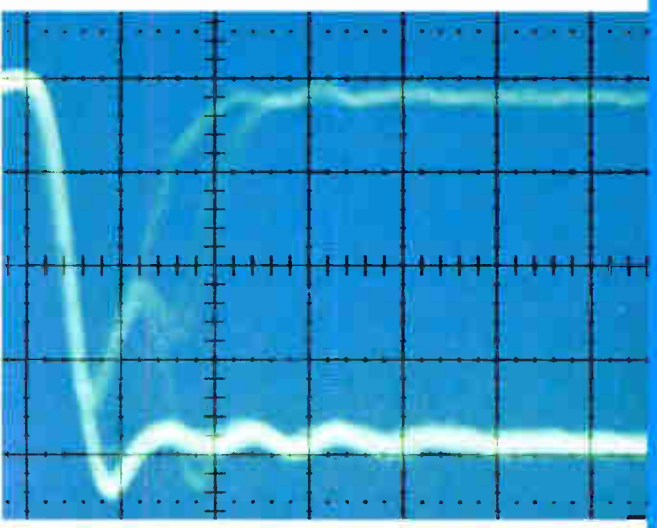

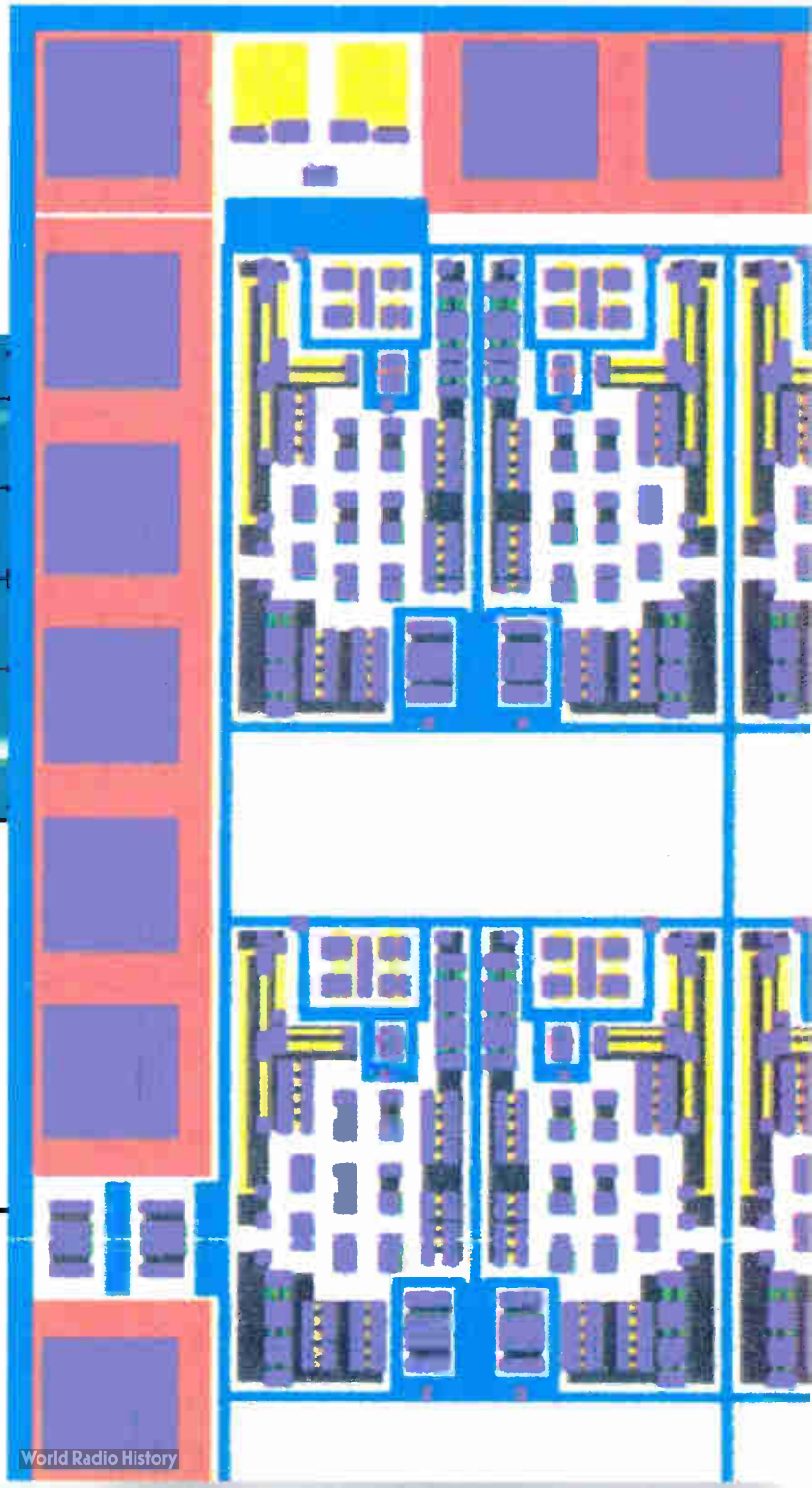

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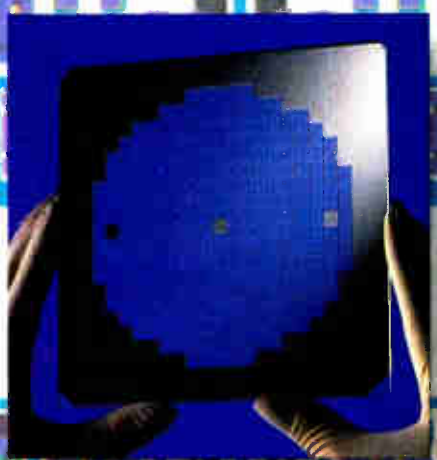

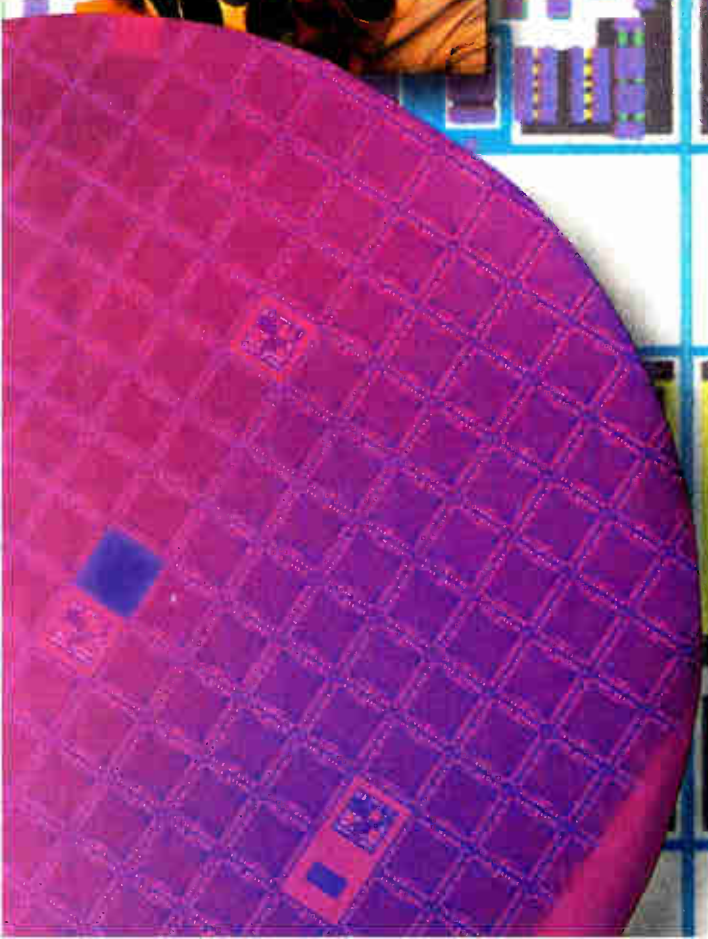

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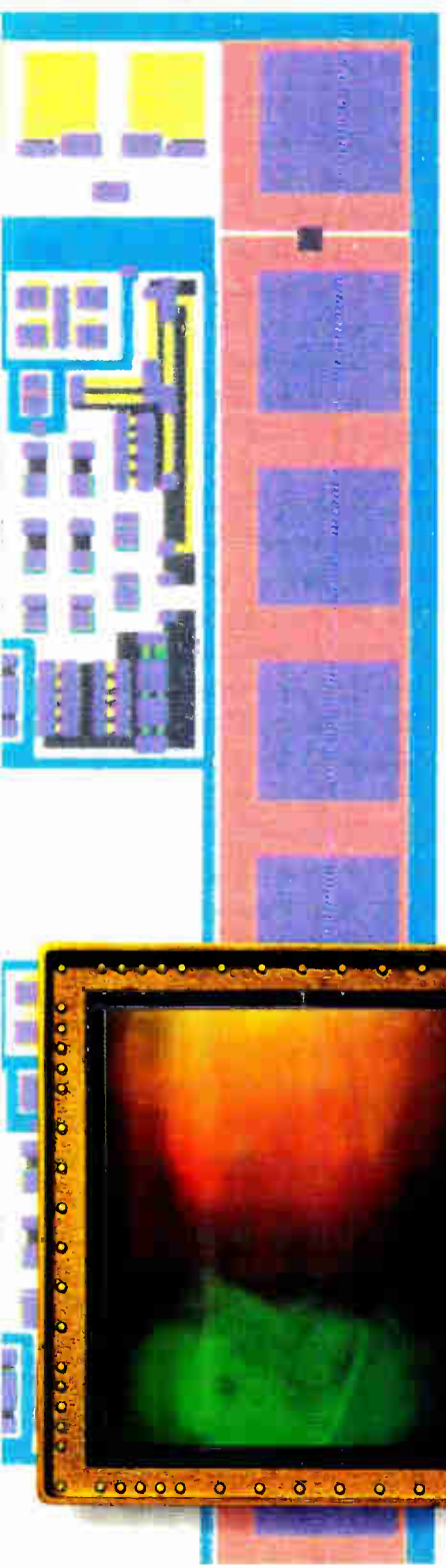

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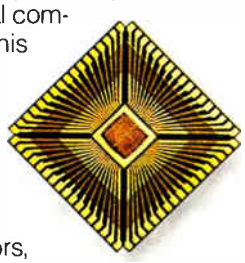

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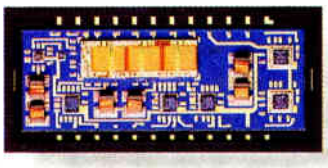

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Electronics

AUTOMATED 'MONSTER' IC PLANTS MAY BE AN EXPENSIVE MISTAKE

JAPANESE CLOSE SOME 6-IN. PLANTS, PULL BACK FROM 8-IN. WAFERS

LOS ANGELES

Led by the Japanese, the rush by the world semiconductor industry to highly automated, 6-in. wafer "monster" plants is now being called an expensive mistake by leading industry consultants. And the next step, to 8-in. wafer lines, has hit an economic and technical stone wall. The result, they say, has been a growing number of Japanese plant closings, cancelled construction plans—and maybe a golden opportunity for U.S. chip makers to catch up.

These dramatic views were first aired in late January by Jerry D. Hutcheson, founder and CEO of VLSI Research Inc. in San Jose, Calif., an expert on semiconductor production equipment. He is challenging what has been regarded as a bedrock truth: economies of scale are the key to prosperity. The reasoning has been that the bigger the wafer and the more automation, the more good dice at a lower cost. Such attitudes had led to the huge automated 6-in. wafer fabs that can crank out up to 10,000 wafer starts per week. These plants cost upwards of $150 million each, and the Japanese alone have committed to build about 40 since 1984.

TIMES CHANGE. But today's lagging markets are not the same as the markets of five years ago, when the Japanese were taking market share with high-volume production of dynamic random-access memories and could afford to build the huge plants. "They are finding the plants don't work profitably today," Hutcheson says—so startups have been delayed, and plants have either been closed or downsized.

The question now is, what effect will all this have on U.S. plans to compete against the Japanese, their monster plants, and their supposed economies of scale? Being discussed now are two similar proposals: a Pentagon-supported U.S. manufacturing consortium and an industrial plan to set up a manufacturing cooperative (Sematech). As far as Hutcheson is concerned, there is a role for such a cooperative. "I'm still for it," he says, but adds that the key to making a U.S. manufacturing cooperative work is plant flexibility.

The monster plant problems have gone unnoticed, says Hutcheson, because Japanese semiconductor executives do not discuss the issue candidly. "They're still saying, 'Everything looks great,' when asked about how the 6-in. wafer plants are doing," says Hutcheson, who regularly visits Japan. Those same attitudes prevailed in late January when an *Electronics* editor queried Japanese chip makers. NEC maintained it has three 6-in. lines operating. Hitachi said it has two, and neither would admit that it has overbuilt. In addition, Toshiba insisted that its next new line will handle 6-in. wafers.

Hutcheson's conclusions are seconded by other experts, such as semiconductor analyst Daniel J. Rose, who track the business. For example, recent data from Integrated Circuit Engineering Corp. of Scottsdale, Ariz., shows that some Japanese companies are indeed backing off from 6-in. production (see table).

The problem, says Hutcheson, is sluggish growth leading to overcapacity. On top of that, Hutcheson says, the automated equipment is designed to perform at top rates for peak efficiencies and cannot easily be scaled back to lesser volume: "The plants are inflexible because these systems are essentially bolted together," he says.

So when demand is flat or lower, production is cut, and expenses climb to the point that operations "can be enormously unprofitable," says Hutcheson. Also, the mix of semiconductor type has changed from high-volume commodities to ASICs. The implications for the U.S. chip industry could be profound, he thinks. "Americans [merchant market suppliers] never built the monster plants, but that can work to our benefit. For the first time in 10 years, the U.S. has a chance to catch up." U.S. makers rely on smaller, more flexible plants, he says. Since these plants are now being upgraded to improved processes, U.S. suppliers are better attuned to today's demand for short-run ASICs.

ASIANS DELAY SOME 6-IN.-WAFER PRODUCTION

Company	Facility location	Installed capacity (wafers/month)
Fujitsu	Iwate	22,000
	Mie	10,000
	Wakamatsu	10,000
Hitachi	Kofu	15,000
	Mobara	15,000
	Naka	Closed
	Ohme	Delayed indefinitely
	Hokkaido	Opens 2nd quarter 1987
Hyundai	Inchon	Opened 4th quarter 1986
Matsushita	Arai	Delayed indefinitely
	Uozu	Opened 4th quarter 1986
Mitsubishi	Kumamoto	Delayed indefinitely
	Saijo	Delayed indefinitely
	Kochi	Opens 1st quarter 1987
NEC	Kumamoto	25,000
	Yamaguchi	20,000
	Livingston, Scotland	Opens 1st quarter 1987
Oki	Miyazaki	Opened 4th quarter 1986
Ricoh	Osaka	10,000
Sony	Niigata	Delayed indefinitely
Sharp	Fukuyama	Opened 3rd quarter 1986
Toshiba	Oh-Ita	20,000
	Iwate	Opened 4th quarter 1986
Total	–	147,000

SOURCE INTEGRATED CIRCUIT ENGINEERING CORP

The changes could turn back the clock, says marketing consultant Matt Crugnale of Crugnale & Associates, Mountain View, Calif. "The chip business could look like it did before the DRAM push," before the Japanese commodity dominance, he says. "Flexibility [in manufacturing] is the key word, since it means closer ties between suppliers and big users."

Attaining true flexibility in chip manufacturing is a task that causes headaches for U.S. companies too, says Theodore Malanczuk, vice president of manufacturing at National Semiconductor Corp., Santa Clara, Calif. The software for controlling automated process lines is so much different for ASICs that "generating this software is a monumental task," he says. "Japan has generated

software for commodity items; they will have to go back and regenerate for custom. That is something the U. S. is struggling with now."

As for 8-in. wafers, Hutcheson says, "the trend is slowing, possibly disappearing." The Japanese think there's no need for the bigger wafers and believe that they are technologically beyond the state of the art. Keeping to a ±5% tolerance across 8 inches is the main bottleneck. So IBM Corp. and Texas Instruments Inc. are the bellwethers of the 8-in. world, with perhaps eight plants between them on-line or planned, Hutcheson says. IBM, in fact, announced last week that the megabit chips in its new 3090 processors were fabricated on 8-in. wafers (see p. 17).

–Larry Waller

BIPOLAR

14,000-GATE HONEYWELL IC LEADS NEXT BIPOLAR WAVE

COLORADO SPRINGS, COLO.

Honeywell Inc. has redefined the word "big," at least for fast commercial bipolar gate-array designs. A new semicustom logic array called the HE12,000, from Honeywell Digital Product Center, raises the gate-count ante for bipolar parts well over the 10,000 mark while offering 150-ps propagation delays and typical power dissipation of 9 W and worst-case dissipation of 15 W.

The new chip is part of the next wave of bigger, faster commercial bipolar arrays aimed at keeping powerful computers percolating on data and programs without the need for expensive liquid-cooling systems. Close on Honeywell's heels are the likes of Fairchild, Motorola, and Texas Instruments, which are expected to announce arrays made from new emitter-coupled logic processes.

POWER STINGY. But Honeywell is making its bid with the same 1.25-μm triple-level-metal bipolar technology it used a year ago to launch the 8,000-gate HE8000. The process—a cousin of the 1.25-μm technology Honeywell used for its Phase I work in the military's Very High Speed Integrated Circuits Program—produces a speedy but power-stingy array of current-mode logic gates surrounded by ECL input-output circuits. CML cells are similar to ECL circuits minus the emitter follower. Without emitter followers, CML cells dissipate less power and have increased density, says David Wick, bipolar product manager.

"The drive capability of CML is inherently less [than ECL], but we have found through our computer design experience that we don't need super-high drive in all of the macrocells of the array," says Wick. "We have an emitter-follower macrocell that a customer can use when he needs to drive a clock line or clock network inside the array."

Although the majority of computer applications will continue the migration toward high-density CMOS semicustom ICs, a small but determined group of mainframe and supermini manufacturers will continue to ask for faster and bigger bipolar chips. That's the view of Dean Winkelmann, who tracks application-specific logic ICs at Integrated Circuit Engineering Corp. of Scottsdale, Ariz.

BIPOLAR: STILL A GOOD NICHE

	1986	1991
Worldwide market ($ billions)	1.285	3.35
CMOS	66%	76%
ECL	21%	14%
Bipolar	13%	8%
GaAs	–	2%

SOURCE: INTEGRATED CIRCUIT ENGINEERING CORP.

"The majority of applications do not require the speed and will not pay the price premium for ECL," he says. However, "there will always be manufacturers that want fast bipolar chips. The only thing is, this group will continually get smaller. Therefore, commercial demand will be generally satisfied—for quite a while—by these products being introduced this year." He estimates ECL and bipolar parts will shrink from a combined 34% share of $1.29 billion gate-array sales in 1986 to only 22% of $3.35 billion by 1991 (see table).

Even though the market is getting smaller, others have no intention of leaving it all to Honeywell. For example, Motorola is expected to introduce soon a high-density ECL gate array based on an extension of its Mosaic II process using a new structure called a polyelectrode transistor. Fairchild, likewise, is expected to apply its latest bipolar process, called Aspect [*Electronics*, Sept. 4, 1986, p. 55], to high-performance bipolar arrays. And England's Ferranti Electronics Ltd. announced last fall a fast, low-power 10,000-gate bipolar array using a new third generation of its collector-diffused isolation process [*Electronics*, Oct. 2, 1986, p. 68].

In Colorado Springs, Honeywell has already quietly begun manufacturing master slices in preparation for second-quarter shipments of its first HE12,000 gate arrays. In making the jump from the HE8000 to the HE12,000—which actually has 14,000 usable gates—Honeywell simply made a die as large as it could with its current wafer-stepper equipment. The die measures roughly 400 mils on a side. The count of 256 input/output pins was selected after customers were polled.

The chip is packaged in a cavity-down 319-pin grid array. Scan macros have been designed into the HE12,000. Designers can also use Honeywell's proprietary scan technique for testability checking, called native fault testing. The array comes with three power-supply modes, available for ECL 10-K and 100-K system compatibility of –5.2 V, –4.5 V, and –3.3 V. A nonrecurring engineering charge has been set at $80,000 to $110,000, depending on the number of designs bought. *–J. Robert Lineback*

SEMICONDUCTORS

WITH FINGERS CROSSED, CHIP MAKERS EYE UPTURN

SAN MATEO, CALIF.

While no one was watching, the semiconductor pot has quietly begun to simmer. At least a few U. S. chip makers are well into a modest recovery that may not be a turnaround, but that looks more solidly based than the inventory bubble that raised hopes a year ago. This time the improvement appears to be fueled in large part by an equally welcome upturn in at least some data processing sectors, which overall account for nearly a third of the semiconductor marketplace.

"Having been deluded by the false start last spring, I am cautious about announcing an upturn, but the momentum has definitely shifted to favorable," chairman Jerry Sanders told workers at Advanced Micro Devices Inc. in announcing the Sunnyvale, Calif., company's improved results for the quarter that ended in December and the outlook for the spring. "Our most important market sector, computers, is recovering, led by strong demand for personal computers," Sanders added.

AMD's Silicon Valley neighbor, Intel Corp., Santa Clara, has been given an even bigger boost by renewed demand for microprocessors, microcontrollers, and related circuits. Intel reportedly enjoyed four straight months of $100 million-plus orders, beginning in Septem-

ber, with December bookings approaching $140 million. January kept up the pace, insiders say. "They are smoking," comments analyst Adam Cuhney of Kidder Peabody & Co. in San Francisco, who recommended Intel as a buy despite the company's just-announced quarterly loss of $16 million.

Intel marketing director Larry Hootnick says, "We have been increasing in revenue 5% to 10% a quarter, and it's not because of good pricing, so something must be going on. It's clearly the best sign we've had." Still, he wants to see more evidence. "We're trying to assess whether or not it is the start of a broad upturn. It's premature to say that it is."

GETTING BUSY. Modest recovery, spending cycle, or real turnaround: whatever it is, the upturn means more fab work.

Makers of application-specific integrated circuits, such as LSI Logic Inc. and VLSI Technology Inc., and programmable logic maker Monolithic Memories Inc. are also sharing in the boomlet, as personal computer makers adapt their boards to replace the glue chips used in earlier generations.

Another encouraging trend, Hootnick notes, is that Intel's customers' sales are also increasing. In fact, although the data-processing recovery is just as tentative as the semiconductor industry's, a number of computer companies and makers of computer-related equipment have also shown signs of improvement.

Sun Microsystems Inc. was up 42% in sales over a year ago in its most recent quarter. Improvement was also reported by Tandem Computers, up 40%; Kaypro, up 113%; Amdahl, up 30%; and Apple Computer, up 24%. Digital Equipment Corp., the first of the computer makers to show signs of life last year, and Zenith Data Systems, which expects its personal-computer business to expand 50% this year, from last year's $352 million, also contributed to the resurgence.

The spectacular performance of disk-drive makers Seagate Technology and Maxtor Corp., both of which more than doubled sales and earnings in the fourth quarter, pointed to the role of the personal computer in pacing the recovery. Further confirmation came from software supplier Microsoft Inc., up 62% in sales to $81 million.

Some marketers are still cautious about the prospects for a recovery now. Motorola Inc.'s Semiconductor Products Center reported a business upswing, but world marketing director Charles Thompson says he has no idea whether it will continue. Texas Instruments Inc. reported gradual growth in ASICs and microprocessors, as well as some memory products. Orders were balanced between distributors and original equipment manufacturers, says Bruno Pagliuca, TI's director of world marketing, but he also says he suspects that the increase was due in large part to inventory restocking.

Moreover, not all the news has been good. IBM's much-publicized earnings slide, as its revenues for the fourth-quarter slipped 1.2% and rose only 2.4% for the year, and the sluggishness of the mainframe market in general have kept enthusiasm within bounds. "We don't sense any big recovery," says Richard D. Skinner of Integrated Circuit Engineering Corp., a semiconductor research firm in Scottsdale, Ariz. "IBM is still the biggest buyer. Inventories are still being reduced, and just-in-time manufacturing is keeping them down." ICE expects only a 4% growth in the U.S. semiconductor market in 1987, with most of the improvement coming in the fourth quarter.

And semiconductor materials consultant Daniel J. Rose foresees a carbon copy of last year—that is, "a business bubble through February, then a big thump." Rose credits rock-bottom inventories and seasonal capital spending, when companies place orders for computers, for the current upturn. "The long-term outlook continues grim," he warns.

European and Japanese companies also doubt that a full-scale recovery is in progress. Semiconductor trade-agreement pricing and the mainframe slump are keeping Japanese memory sales down. And the falling value of the dollar has left foreign markets vulnerable to U.S. penetration. In Europe, semiconductor executives point out that general economic forecasts for 1987 have been revised downward recently. "So I have my doubts about the slight upswing leading to a substantial recovery," says Rudolf Schwenger, marketing director for ICs at Siemens AG's Components Group in Munich.

RAISED FORECAST. But after waiting two years, no one wants to miss the recovery when it does appear. Market consultant Jack Beedle of In-Stat Inc., Scottsdale, predicts higher bookings through February and is preparing to raise his U.S. gain forecast for this year from a 5.1% increase to 8% to 12%.

And the Semiconductor Industry Association, whose closely watched book-to-bill ratio surprised everyone by rising 0.9 in December to 1.08, won't knock its own numbers, even if it can't entirely explain them. "We know there is a recovery out there," says SIA statistician Douglas Ardrey, "but we don't know where it is." *–Clifford Barney*

SOFTWARE

MICROSOFT AND AT&T FACE OFF IN UNIX WARS

WASHINGTON, D.C.

A tangled web of alliances is shaping up as AT&T Co. and Microsoft Corp. battle to dominate the Unix marketplace. Both have enlisted Intel Corp.'s powerful 32-bit 80386 microprocessor, and each made major announcements at the recent UniForum conference in Washington. Microsoft initiated a bold bid to make its Xenix the Unix version of choice on microcomputers, while AT&T lent its muscle to an industry-wide effort aimed at standardizing the operating system it invented.

Both moves come as the imminent debut of a raft of 80386-based microcomputers promises to rock the Unix marketplace. "Everybody's looking at the 386 as the platform to get Unix spread over a much wider market," says Betty M. Niimi, vice president of Interactive Systems Corp., Santa Monica, Calif.

This is a market that Microsoft of Bellevue, Wash., intends to capture. It has forged an agreement with Interactive Systems to develop a version of Xenix expressly for the 80386. The software is expected late this year.

In the meantime, users seeking to run multiple applications under Unix and MS-DOS—Microsoft's other well-known operating system—can use Interactive's new VP/ix [*Electronics*, Jan. 22, 1987, p. 22] with MS-DOS, which Microsoft has

just licensed Interactive to distribute. Also Xenix's codeveloper, The Santa Cruz Operation Inc., Santa Cruz, Calif., assumes from Microsoft the distribution and support of Xenix for use with Compaq Computer Corp.'s 80286- and new 80386-based microcomputers.

To date, microcomputers have generated only minimal Unix software sales—about $19 million in 1986, according to estimates by the market researchers Dataquest Inc. That was before machines like Compaq's new Deskpro 386 came along. Based on the 80386, it has ample power to provide an ideal showcase for Unix. As a result, Dataquest believes microcomputer Unix revenues will burgeon to $62 million in 1987 and $158 million in 1990.

As Compaq's computer is joined by competitors' hardware, software developers are demanding standards to ensure their Unix packages will run on disparate machines. Providing such assurances is in AT&T's interest, because the company receives a licensing fee each time a software maker develops a product on its Unix System V.

That may be the reason AT&T has joined X/Open, the international group striving to define a standard for a common Unix applications environment. AT&T announced in Washington that it has become the 11th member of the London-based group, joining Bull, Digital Equipment, Ericsson, Hewlett-Packard, ICL, Nixdorf, Olivetti, Philips, Siemens, and Unisys.

INDEPENDENCE. But more than 230 software suppliers are seeking independence from AT&T licensing fees. They have joined the Posix (Portable Operating Standard for Computer Environments) committee, an effort sponsored by the Institute of Electrical and Electronics Engineers to develop, in effect, a generic Unix systems standard. Posix is expected to become the Unix standard for government computing, though its commercial effect is less clear.

Equally unclear is just how AT&T intends to fend off Microsoft's Xenix attack. Indeed, there has been speculation that AT&T may give up the 386 market and license to Microsoft the sole rights to offer Unix for 80386-based machines.

Yet that could not have been AT&T's plan one year ago, when it licensed Interactive Systems and Intel, of Santa Clara, Calif., to transfer AT&T Unix System V to the 80386. The result, Unix System V/386 Release 3.0, is now being tested at 50 beta sites and is expected to come to market early this year, says Intel, ahead of Microsoft's 386 package.

Yet even on the 386, Unix remains best suited for running multiuser applications. So Microsoft is hanging on to its MS-DOS card and is hard at work developing a version of MS-DOS especially for the 80386 [*Electronics*, Sept. 18, 1986, p. 91]. *-Alexander Wolfe*

COMPUTER-AIDED DESIGN

PLESSEY PUTS ITS CHIPS ON SOFTWARE

CASWELL, ENGLAND

Unable to find the software that it needs for computer-aided integrated-circuit design, Plessey Research Ltd. is turning the problem into an opportunity. It has embarked on a two-year research project aimed at putting it in the forefront of CAD chip-design software.

The vehicle is Plessey's Megacell system. It can design CMOS chips with up to 80,000 gates and bipolar parts with up to 30,000 gates, and can do the job at up to 500 gates per man-week. The company puts the speed of most existing systems at 300 gates a week. But the Caswell, UK, company wants more than just more speed: it plans to increase Megacell's design capacity to 250,000 gates for CMOS and 40,000 for bipolar. And it hasn't been able to find the necessary software and systems on the market.

"There is not enough software for capture and algorithm defining," says Derek Boardman, manager of the company's CAD and computer facilities. "We can't use Daisy, Mentor, and other systems except for defining structures and physical design. A lot of time is needed at the higher level."

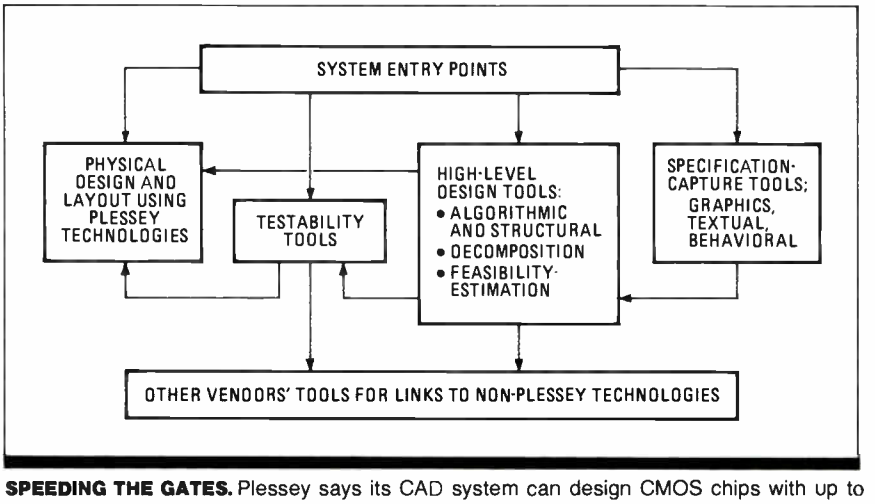
Enter the software project. With some help from the Alvey fifth-generation computer project, which provides research funds to industry and universities, Plessey aims by 1989 to have a system running on a Digital Equipment Corp. MicroVax that will be able to handle designs of up to 1 million transistors at a rate of 10,000 gates per man-week.

"Our system will be equal to or better than the rest of the world's in two years' time," says Boardman. "It will still be able to be used by system designers, but the expert designers will be able to push the limits of technology." Boardman shrugs off possible competition. He says he sees little in the marketplace that suggests competitors will be able to solve the problems that the Plessey system will be able to handle.

Plessey will invest $3.75 million to $4.5 million a year over the next two years in the project. Another $750,000 will come from an Alvey CAD project that has a total of $9 million to spread among Plessey, General Electric Co., Racal, Ferranti, STC, ICL, the Royal Signals and Radar Establishment, and a few universities.

On the marketing side, Plessey is taking a new approach. Its existing Megacell software is tied into Plessey silicon; Plessey sells it to customers at a low price, knowing that the profits will come when the customer wants the chips made. The new software, however, will be sold in its own right in the marketplace at a realistic price, and users will be able to use software tools from other companies to design in non-Plessey technologies.

Megacell itself is engendering some 60 new Plessey products this year, which will run on its 2-μm fab line in Roborough. The 1.5-μm prototype line at Caswell will be transferred to Roborough for full production this year; the plan is to scale it down to 1.2-μm in mid-1988. Meanwhile, work is under way to prepare for the next stage: below 1 μm and, ultimately, 0.5 μm.*-Steve Rogerson*



SPEEDING THE GATES. Plessey says its CAD system can design CMOS chips with up to 80,000 gates at 500 gates per man-week. An upgrade to 250,000 gates is planned.

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ELECTROCHROMICS ARE SET TO DO IT WITH MIRRORS

ZEELAND, MICH.

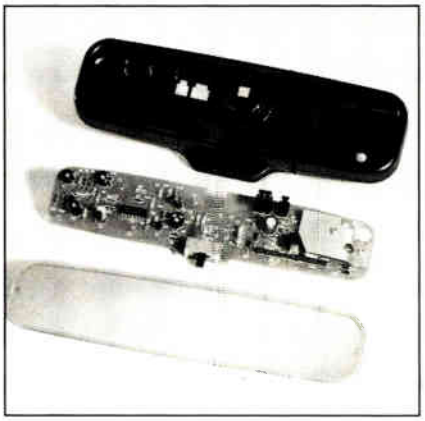
Electrochromics never made it as an automotive dashboard-display technology because of slow transition time. But now a pair of small Michigan companies think they've found a way to pop open the automotive market for this technology. They're going to do it with mirrors.

The idea is to replace conventional silvered-glass rearview mirrors with electrochromic mirrors that can automatically adjust for glare. Sensors on the front and back of each mirror will read light conditions, providing input for built-in electronics that will make the adjustments. Though details of the deal are sketchy, the first mirrors will show up in model-year 1988 or 1989 cars from Ford Motor Co. The mirrors will be supplied by Gentex Corp. of Zeeland, Mich., which is tooling up to begin manufacturing this summer.

The reward is a niche market for electrochromic inside and outside mirror systems that Gentex chairman Frederick T. Bauer says could reach about $300 million within five years. Gentex is one of two Michigan firms planning to supply electrochromic mirrors. The other is Donnelly Corp., in Holland, Mich., which will ship its first prototype mirrors to automakers late this month. Donnelly executives will unveil their design at the Society of Automotive Engineers' International Congress and Exposition, Feb. 23-27 in Detroit.

Also in the competition are two Japanese companies that are developing similar mirrors based on liquid-crystal technology. Executives from two firms—Nippondenso Co. and Tokai Rika Co.—will be at the Detroit conference to discuss their approach. But Bauer contends that electrochromics have inherent advantages over liquid crystal (see "Why electrochromics won out in Detroit," below). And, he says, electrochromics could be suited for a much larger automotive market for variable-light sunroofs, rear hatches, and windshields.

In the U.S. auto market, at least, Gentex appears to have the early lead. Some 100 prototype Gentex mirrors have been under test by automakers since the fall of 1985. And last April, the



EYE EASE. Gentex will start making its electrochromic mirrors for 1988 or 1989 Fords.

WHY ELECTROCHROMICS WON OUT IN DETROIT

The benefits of electrochromic versus liquid-crystal technology in the design of automatic antiglare rear-view mirrors in cars will likely get a full hearing Feb. 23-27 at the International Congress and Exposition in Detroit, where Japanese suppliers will lay out the benefits of their liquid-crystal units. But in the U.S., at least, suppliers believe that electrochromic technology holds a clear advantage over liquid crystal. And the automakers seem to agree.

For one thing, electrochromics offer a broader range of reflectivity, observers say. As with liquid crystals, the reflectance level of electrochromic-based mirrors is changed by applying a variable voltage across the mirror surface, using conductively coated glass electrodes. At about 1 V, the mirror becomes darker, and 4% to 6% of the light is reflected; at 0 V, it's 80%.

That's close to the 85%-to-4% reflectance range of conventional antiglare glass mirrors, which must be moved mechanically. Liquid crystal's low-end reflectivity is equal, but it can't match electrochromics at the high end, contends William P. Lantz, market-development manager at Donnelly Corp. in Holland, Mich. "We're not aware of any liquid-crystal mirror that does better than 50% [reflectivity at maximum brightness]," he says.

An additional electrochromic advantage is one that worked against the technology for displays: slow transition time. With rear-view mirrors, an abrupt transition could be disconcerting to a driver, says Frederick T. Bauer, chairman at Gentex Corp. of Zeeland, Mich. The electrochromic mirrors that Gentex plans to sell to Ford Motor Co. starting this summer will require 3 s to go from light to dark, and 7 s going the other way, Bauer says. *–W. R. I.*

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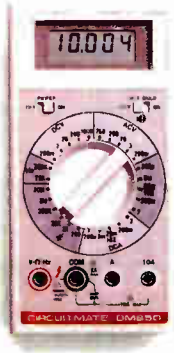
- DMM: Input Impedance—10 Megohms DCA/ACA-5 ranges (200μA to 2A)
- Ohms-8 ranges (200 ohms to 2000 Megohms)
- Continuity beeper

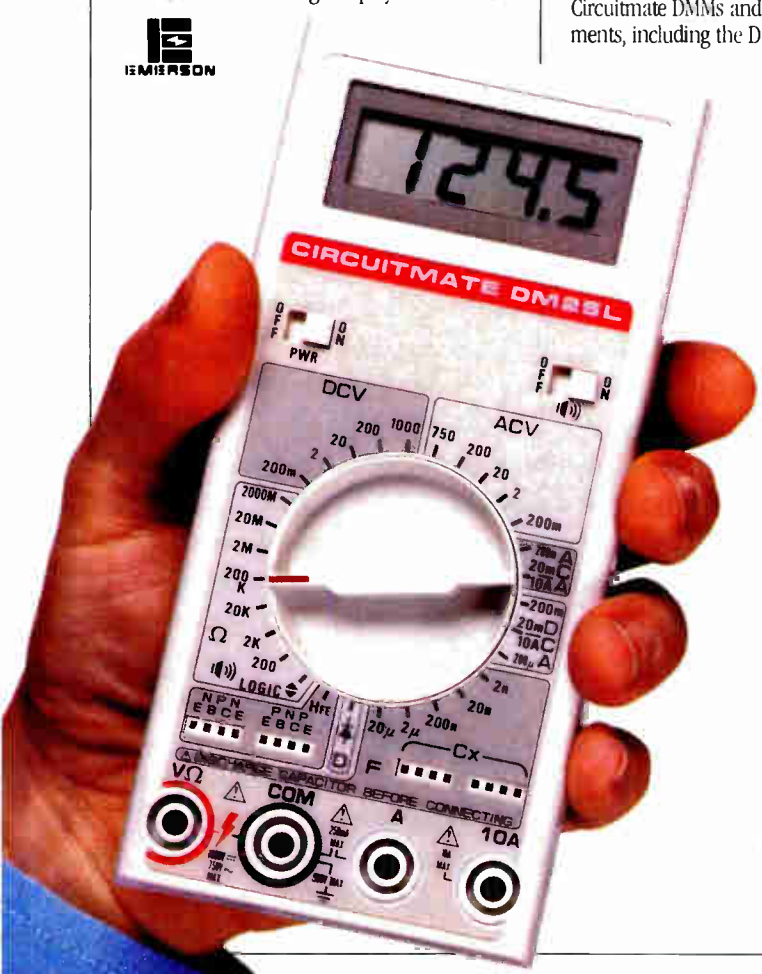
DM850 True RMS

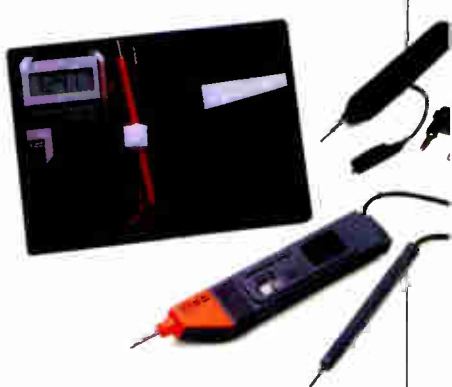
- 4½ digits. DCV accuracy is .05% +3 digits
- True RMS
- Frequency counter to 200KHz
- Data Hold display capability
- Continuity beeper
- Built-in bail
- Anti-skid pads
- Price: DM850 (True RMS). . . .$219.95* DM800 (Average) $169.95*



DM25L Capacitance, Logic, hFE $89.95*

- TTL Logic Probe: 20MHz Hi/lo/off indications Detects 25nS pulse widths
- Capacitance: 5 ranges (2nF to 20μF)
- hFE (NPN or PNP): 1 range (1000)
- Continuity beeper
- Built-in bail
- Anti-skid pads





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Circle 37 on reader service card

company was the first to demonstrate a system with the left outside mirror working as a slave to the sensor-equipped inside mirror.

What's more, Gentex says it has come up with a technique based on a proprietary electrochromic chemical that can be injected between two glass plates. Conventional techniques require multiple layers of electrochromic materials, such as tungsten oxide and strontium titanate, to be sputtered on glass. The Gentex approach will cut manufacturing costs dramatically, perhaps by as much as half, Bauer says. But at Donnelly, which will rely on a multiple-sputtered-layer process, market development manager Willam P. Lantz says his firm has developed some proprietary materials and manufacturing techniques that will likewise hold costs down.

Electrochromic models cost considerably more than today's mirrors. Lantz says that Donnelly's interior mirror will be sold to automakers for $30 to $50 apiece, depending on features, compared to $2 to $2.50 for conventional mirrors. The Gentex mirror is expected to fall in the same range. Nevertheless, both Gentex and Donnelly believe that the benefits, at least for buyers of luxury cars, will justify the cost.

EYE ON NEW YORK. Though its initial order from Gentex is for interior mirrors only, Ford, for one, is planning to show a 1990s concept vehicle at the New York Auto Show, April 18-26, that will be equipped with both interior and exterior mirrors by Gentex. And at General Motors Corp., a spokesman for the Cadillac Motor Car Division in Detroit says its engineers prefer electrochromic mirrors to the liquid-crystal units so far tested. Cadillac expects to use electrochromics, the spokesman says, but not until a full interior/exterior mirror system is available, probably by model year 1990. *–Wesley R. Iversen*

STATIC MEMORY

PHILIPS' SRAM GOES AFTER LOW-POWER APPLICATIONS

EINDHOVEN, THE NETHERLANDS

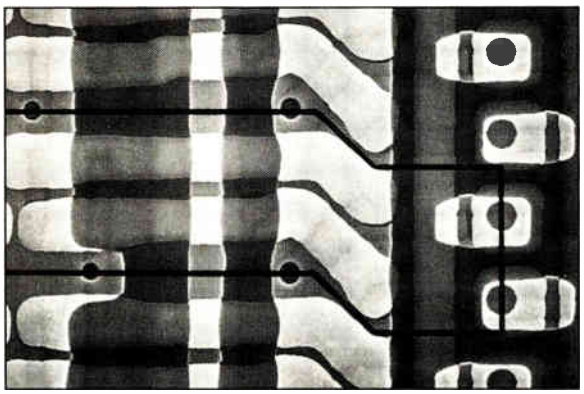
In the go-go world of static random-access memories, speed is king. But the engineers at the Philips Research Laboratories in Eindhoven have taken a deep bow to another feature, one they believe will open applications in portable consumer products and battery-operated office equipment: low power. They are developing a 256-K CMOS SRAM that not only is a speedy power miser, but has so much capacity that it should be a natural for video cassette recorders and portable computers.

The SRAM [*Electronics*, Dec. 18, 1986, p. 50] consumes less than 1 mW in standby and 75 mW at 10 MHz—versus up to 200 mW for competing SRAMS. Its developers also credit it with greater reliability and more freedom from transient noise and temperature variations than most other SRAMs. And with all that, they have not neglected speed: with a 100-pF load, the memory accesses in 40 ns, which is not bad given the low power consumption.

The Philips team has combined well-known techniques and some novel methods to cut the chip's power demands. Fabrication is with what Joseph Bastiaens, CMOS process integration manager, considers a relatively simple technology: a complementary-doped, single-polysilicon, CMOS process that uses double-metal, twin-well design on an epitaxial substrate. Fabrication requires 14 masks. The minimum 1.3-μm features and buried contacts push the six-transistor cell down to an area of 8 by 25 μm, says Bastiaens.

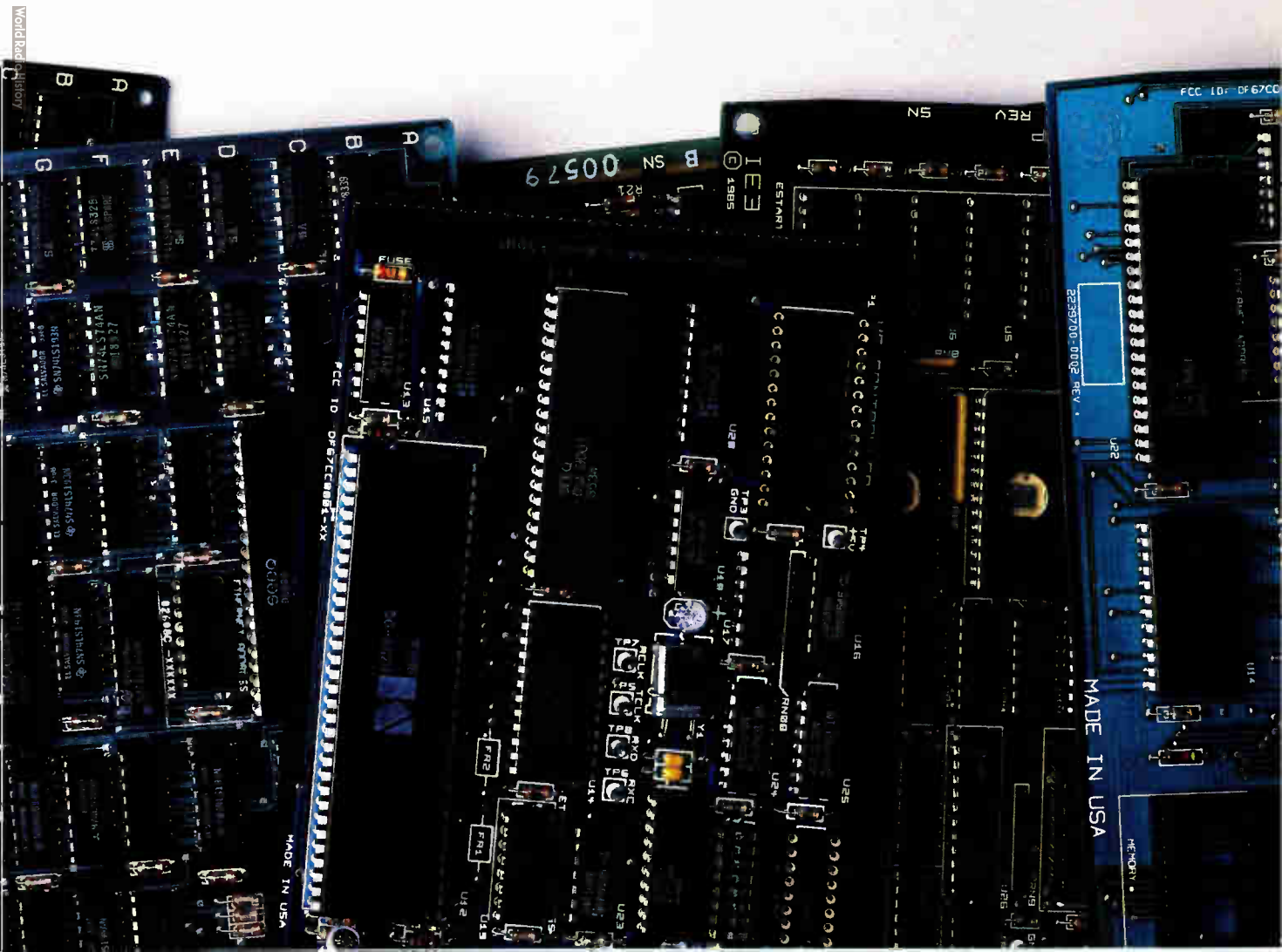
Because the polysilicon gates of the two p-channel and four n-channel transistors are p- and n-doped, parasitic lateral poly/poly diodes are formed in the cell. But as Will Gubbels, the memory's chief designer, points out, measurements have shown that the noise-margin loss due to these diodes is minimal.

The Philips cell uses a double-cross-connection scheme, so the gates of the two p-channel transistors connect with the drains of two n-channel transistors. That means



BUILDING UP MEMORY. Memory cell of the Philips low-power 256-K static RAM after the first metal layer.

HOW TO AVOID GOING OVERBOARD.



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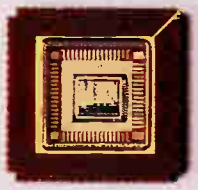

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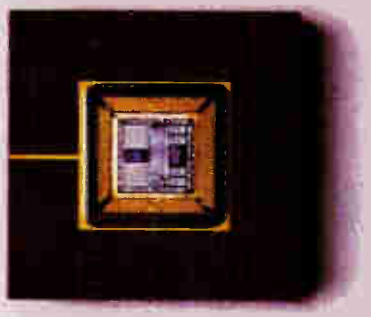
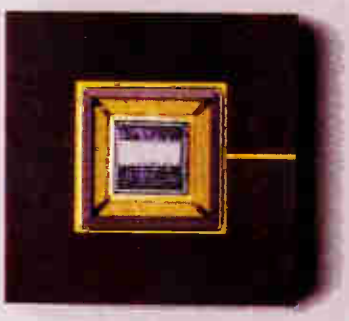
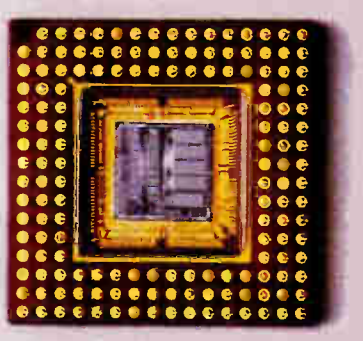


High Performance cell-based 1750 CPU combines logic, ROM and processors.



Structured Arrays combine high-density memories with up to 41,000 logic gates.



Channel-free Compacted Arrays combine logic and memory functions with up to 129,000 available (up to 70,000 utilized) gates.

that one p-channel transistor is always completely off, dissipating little power.

The data-path circuits also help to keep the power demands down. An address-transition detector circuit generates asynchronous pulses, such as automatic power-up pulses, as well as pulses to equalize the bit lines, the section data-read lines, and the internal nodes of the sense amplifiers. These pulses, generated at the beginning of a read operation, deactivate the word lines and sense amplifiers to reduce active power dissipation during long read cycles.

In a long write cycle, a so-called data-transition detection circuit—which Gubbels says is a first for SRAMs—retriggers the power-up pulse after a delayed data change. The bit lines operate close to the power-supply level to maximize stability and noise immunity of the cell during read operations.

A compact tristate driver, switched to the high-impedance state during the equalize and amplification phases, does its part by seeing to it that only valid data is put onto the global read bus. An output latch maintains the valid data when the sense amplifier and the tristate driver are disabled. A new output

One p-channel transistor is always off, saving power

buffer design minimizes the effects of the package lead inductance on the output buffer delay and supply-line noise. A special inverter, with a voltage-dependent capacitor and a p-channel MOS diode as key elements, drives the gates of two push-pull transistors. When switched on, the buffer current increases linearly with time.

The chip uses a six-transistor cell structure compared with the conventional four-transistor resistance-load cell. Also, by using 1.3-μm design rules, the Dutch researchers have squeezed the cell down to about the same size—200 mm^2—as the less robust four-transistor cell. In addition, "we are considering putting the memory into a surface-mounted-device package," says Jan Lohstroh, head of the research lab's Advanced Memory Design Center.

To improve production yield, two spare rows and 32 spare columns are incorporated on the memory chip. These can be programmed by laser fuses. To reduce chip dimensions and increase speed, the Philips designers are now working to shrink the device linearly by a factor of 0.8. This, they say, will be relatively easy, since CMOS memory cells depend only on transistor ratios for their operation and therefore remain stable when shrunk. *–John Gosch*

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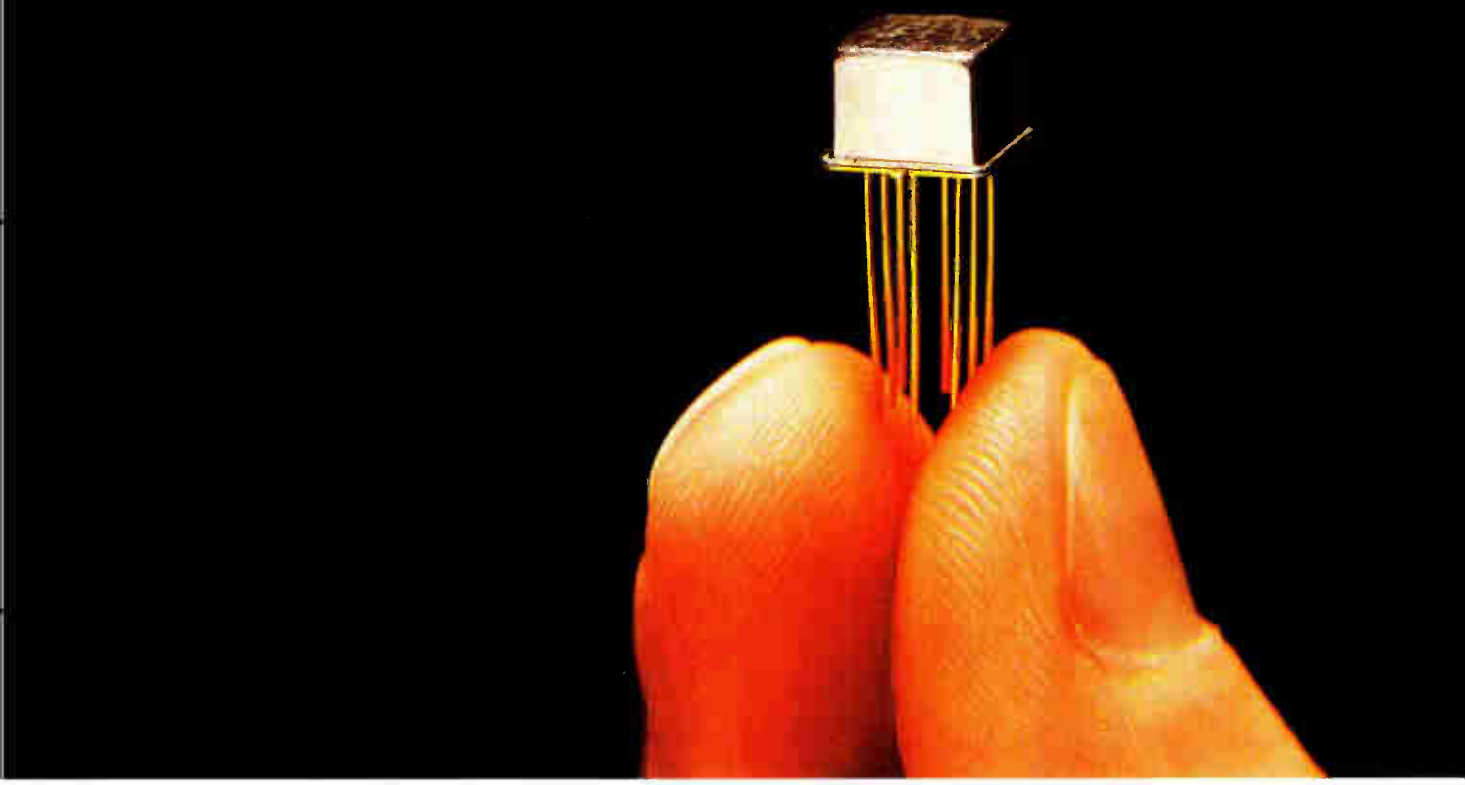

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COMPUTERS

IBM TRIES TO CHANGE ITS LUCK

NEW YORK

Looking for a way to spark some first-quarter sales action, IBM Corp. is making major changes to its high-end 3090 mainframes—introducing two new models, cutting prices on two existing models, and upgrading performance across the entire line.

The move came just days after the Armonk, N.Y., giant disclosed that earnings declined a startling 27% in 1986, and 48% in the year's fourth quarter. IBM is banking on its new model 600E—its most powerful computer ever—to help spur sales. The key to the increased performance is a new version of the company's 1-Mb dynamic random-access-memory chip that is twice as fast and one third the size of the megabit DRAM that IBM has been using until now (see p. 17).

Though not unexpected, IBM's announcement appears to be designed to boost lagging first-quarter sales. The company will begin selling the enhanced models immediately, but customers should not expect to see any performance improvement over the current line until May. That's when IBM says it will start modifying those processors, on location, by adding the hardware upgrades. Delivery of the fully configured enhanced models will also begin in May.

"I think they were getting anxious to produce some good news," says Kenneth Bosomworth, president of International Resource Development Inc., a Norwalk, Conn., consultant. "This must have been the best thing they could come up with now." Bosomworth says the new lineup should help fight off the less expensive IBM-compatible mainframes by Amdahl Corp. and the National Advanced Systems Division of National Semiconductor Corp.

SIX PROCESSORS. The queen bee of the new lineup is the 600E, a six-processor machine priced at $11.5 million. The 600E offers a 50% to 60% performance increase over IBM's previous leading-edge machine, the 400, which cost about $8.5 million. The other new machine, the 300E, costs $6.1 million and is IBM's first three-processor design. It is 60% to 70% more powerful than the 200, which can be upgraded to a 300E for about $1.75 million.

The heart of any upgrade will be the 1-Mb chips and the 4-Mb memory cards holding them. The dense cards will allow IBM to double the memory capacity of the 400E and the 600E from 128 Mb to 256 Mb. *–Tobias Naegele*

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INTERNATIONAL NEWSLETTER

DOUBLE-DOPED LASER IS THREE TIMES MORE EFFICIENT THAN YAG LASERS...

Researchers at the University of Hamburg in West Germany have developed a double-doped laser with an efficiency rating of 7%—three times better than conventional neodymium-YAG lasers. The researchers replaced the yttrium and aluminum garnet used in neodymium-YAG lasers with a new material, GSGG—gadolinium, scandium, and gallium garnet—and doped it with both chromium and neodymium. According to Klaus Petermann, head of the research team at the university's Institute for Applied Physics, the two dopants give the laser improved absorption characteristics, making for better use of the pump energy. There is one drawback, however: the neodymium-GSGG laser, at least in its current experimental form, achieves its high efficiency only at medium pumping power, up to 50 W. Beyond that point, thermal lensing causes efficiency to drop. The Hamburg group hopes to overcome the problem by improving and adjusting the laser's resonator geometries. □

...BUT SONY'S SEMICONDUCTOR LASERS ARE AN EVEN BETTER BET

Sony Corp. has developed a high-energy semiconductor laser that offers an efficient but expensive alternative to argon and neodymium-YAG lasers. Fabricated in Sony's metal-organic chemical-vapor-deposition process, the new devices are capable of producing outputs up to 1 W—approaching the range of argon and YAG lasers. Sony's lasers, which operate at wavelengths between 770 nm and 840 nm, boast efficiency in the range of 17%, compared to efficiencies below 3% for most argon and YAG lasers. But the new lasers won't come cheap: prices range up to about $13,000 per unit.□

BRITISH TELECOM PLANS FIELD TRIALS FOR OPTICAL CARDS

British Telecom is planning a major thrust into the optical memory card business that could position the company as a leader in the fledgling European market. BT will launch at least two trials later this year, using cards produced by Drexler Technology Corp., Mountain View, Calif. If all goes well, full-scale operations could begin by 1990. The credit-card-sized medium can store up to 2 megabytes of data and can be read with a laser, much like a compact audio disk [*Electronics*, Dec. 16, 1986, p. 58]. There are four areas in which BT wants to use the cards: the health care industry, for storing medical records; in electronics, for software distribution; in financial services, for credit and debit applications; and in security applications. BT plans to buy more than 10,000 cards from Drexler this year, and it is studying reader/writers from at least six Japanese companies. If it meets its goal, BT will be the first British company to use the technology on a large scale, which should open the door for other potential users and vendors in the UK. □

MICROPROCESSOR DEVELOPMENT TOOLS FROM INTEL JAPAN RUN ON NEC PCs

Intel Corp. isn't letting its microcode copyright battle with NEC Corp. stand in the way of making money in Japan. Intel Japan is now offering a line of microprocessor development systems that can use the NEC PC-9800-series personal computers as hosts. The systems are designed for a range of Intel microprocessors, from the 16-bit 80286 to the 8-bit 8051, and Intel is betting that when they're offered on the best-selling PC-9800, its microprocessor sales in Japan will pick up. Individual software kits are priced at $1,300 each, while in-circuit emulators add from $15,700 for the 8086 to $22,300 for the 10-MHz 80286. Intel is expected to start selling development systems for its 32-bit microprocessors in Japan by the fourth quarter, but earlier in the U. S. The Japanese version will use the PC-9800 as host; in the U. S. the systems will be supported by IBM Corp.'s PC/XT and PC AT. □

INTERNATIONAL NEWSLETTER

SIEMENS AND ERICSSON TO DEVELOP ISDN-COMPATIBLE MOBILE PHONE

In a bid to set an all-European standard for mobile radiotelephone systems, West Germany's Siemens AG and Sweden's LM Ericsson AB will jointly develop a digital system that is at once compatible with international integrated services digital networks standards and economical enough to be used in remote locations. Called D-net, the Siemens-Ericsson system should be ready for introduction in 1990 or 1991, by which time the European Communications Committee is expected to have worked out standards for a pan-European mobile radiotelephone system. Sources say the committee already has received proposals from Philips International NV of the Netherlands and West Germany's Robert Bosch GmbH, among others. The Swedish/German consortium is banking on high-end features, such as highly efficient narrow-band operation and border-crossing functionality, to win approval for its entry. But another key will be low-cost handsets. The pair believe these will help them to open the radiotelephone to a wider base of potential customers. □

NEC DEVELOPS WORLD'S FIRST LONG-LASTING VISIBLE-LIGHT LASER DIODES

The world's first commercial visible-light laser diodes should hit the market in less than a year, according to NEC Corp. engineers. Experimental devices oscillating at the red wavelength of 678 nm have shown no signs of deterioration after 3,000 hours of operation, and the Tokyo company says accelerated life tests give it confidence that the new laser diodes will have a much longer life than the 10,000 hours at which helium-neon lasers are rated. The 678-nm lasers could improve laser printers, as the sensitivity of the amorphous silicon drums incorporated in those printers is four times higher at 678 nm than at the 780-nm wavelength of the laser diodes now used in popular-price printers. The new devices are fabricated using a double-heterojunction structure consisting of a gallium indium phosphide active layer sandwiched between two aluminum gallium indium phosphide layers. □

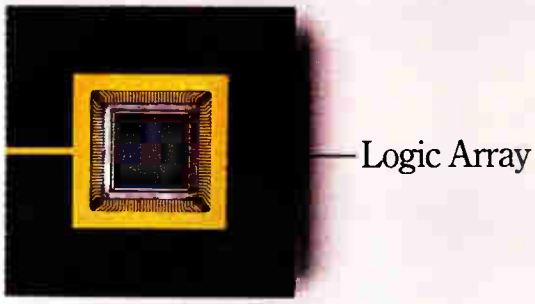
NEC MAY ESCALATE ITS DRIVE ON THE U.S. SWITCH MARKET

NEC Corp., Tokyo, is angling for a slice of the U. S. digital switch market, now dominated by AT&T Co. and Northern Telecom. Industry sources in Japan believe NEC may increase its engineering staff in Dallas from just 40 to as many as 200 or 300 people in the next two years, primarily because the company fears that restrictive trade regulations might force it from the market if it is considered a foreign, offshore operation. NEC now claims a 10% share of the U. S. market for digital private branch exchanges, but has thus far failed in its efforts to sell central office switches. □

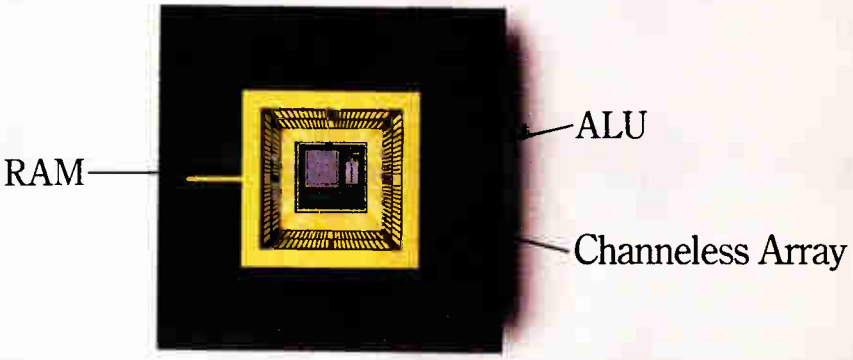
RHÔNE-POULENC IS LOOKING FOR GOLD IN PRODUCING GALLIUM

At least one metals company is hoping to cash in on the growing demand for gallium—a rare-earth metal that is increasingly used in high-speed semiconductors. Rhône-Poulenc Minérale Fine of France is planning to expand its 20-ton annual production capacity with the addition of two new plants by the end of 1988. The company is building one in Freeport, Texas, and the other at an Aluminum Co. of America refinery in Pinjarra, Western Australia, where it will extract gallium from the sodium aluminate obtained in refining bauxite. Since purity is measured in decimal-place percentages, the Australian product—99.99% straight gallium—will be considered crude, while the U. S product, at 99.9999% and 99.99999%, will be considered highly pure. One industry source says that when the two plants are open, the company's output will exceed the total worldwide demand for the metal—now about 50 tons a year. □

A BREAKTHROUGH THAT DEFIES ALL CURRENT LOGIC.



Current Logic



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Circle 54 on reader service card

INSIDE TECHNOLOGY

by Jonah McLeod

The market for computer-aided-engineering software continues to run strong despite the slow overall growth in the electronics industry. High-density semiconductor technology is driving the demand for better chip-design tools. The increasing

THE U.S. MARKET GROWS BRISKLY FOR ASIC TOOLS

Tool type	($ millions)		
	1985	1986	1987
Standard-cell design	10	14	20
Gate-array design	10	15	20
Full-custom design	30	28	25
Silicon compilers	15	35	60
Physical layout	56	72	73
Simulation programs	12	15	18
Total	133	179	216

availability of process technology for building chips with design rules of 1.25 μm and less has made available a generation of digital chips that integrate a daunting number of circuit functions.

The ability to produce application-specific integrated circuits—gate arrays, standard-cell parts, and full-custom types—with 50,000 gates and more is of no use without tools that can make the design of such ASICs manageable. Without such tools, the design of these complex chips takes so long—500 to 1,000 man-years, by some estimates—that a given application market would most likely be captured by competing fast-turnaround board-level implementations before the big ASICs can be readied.

Design software is being improved to deal with these levels of chip complexity at both the front end—the tools used for design entry and debugging—and the back end—the programs that use the design data to generate the physical

Speed is the key: complex ASICs will lose applications to faster-turnaround, board-level implementations without a complete tool kit to rush them to market

chip layouts, standard-cell floor plans, or gate-array routings. A high degree of automation is needed at both the front end and the back end to reduce the time it takes to get chips to market.

At the front end, new design-capture tools are available that allow a designer to enter high-level functions with large numbers of gates in a single stroke, instead of entering tens of thousands of gates one by one. These high-level functions can be compiled for full-custom chips, or they can be called from a library for either standard-cell or gate-array implementation. Various types of user interfaces, from icon-based graphics to special design languages, have been developed to suit the preferences of individual designers for particular tasks. The new tools display the captured logic in simplified forms that allow the designer to conceptualize the design without being overwhelmed by detail.

In addition, to support various levels of chip volume, the tools working at the back end of the design process must be flexible: designers should be able to choose whether to implement their designs as gate arrays for relatively low-volume production, standard cells for better silicon efficiency in somewhat higher volumes, or as full-custom chips for the highest-volume markets. The engineer should not have to rework his design to move from one type of implementation to the other. This kind of flexibility is now becoming available from such companies as LSI Logic Inc. and VLSI Technology Inc., both of San Jose, Calif. (see pp. 59 and 62, respectively).

Such new-generation tools can lay out macrocells—large blocks of logic, such as an arithmetic logic unit or a full central processing unit—for any type of ASIC implementation with a high degree of automation. Whereas the process once required a layout specialist to make the placement of circuit elements, especially the large ones, or to correct a rough placement made by the system, placement today is automatic. Routing the interconnections among those elements requires less and less manual intervention as well, and the heavy computing burden this work places on design systems is being reduced by the use of more efficient algorithms.

The market for advanced ASIC-design tools is driven by the demand for application-specific chips, even as the tools themselves help drive the ASIC market. ASIC sales are predicted to more than double in the next few years.

Sales of CAE tools reflect a trend toward gate-array and standard-cell designs and away from full-custom design. Full-custom chip design is appropriate for standard parts, but it suits ASICs only in the relatively rare cases where demand for very substantial volumes can be established. The market for both gate-array and standard-cell tools is expected to grow more than 40% this year (see table).

Simulation and verification tools will experience more modest growth, but still more than 20%. The fledgling market for silicon compilers will nearly double its growth as user confidence in them builds. The more mature market for physical-layout tools—place-and-route and floor-planning software—will grow nearly 20% this year.

"Gate arrays will experience twice the growth of commercial ICs, and standard cells and macrocells will see a five-to-ten-times growth," says Joseph Costello, vice president of marketing at SDA Systems Inc. in San Jose, Calif. "Even with this large growth, standard cells will not catch up to gate arrays in the next few years."

"Today a systems company spends 1% of its yearly revenue on CAE hardware and software," says Costello. "By 1990 this figure will grow to 2%, with purchases of hardware and software being equal." Design centers and foundries inside large companies will be one source of demand. But a bigger factor will be systems designers in these companies who will have their

own design systems. Rob Walker, vice president and chief engineering officer at LSI Logic, says 40% of ASIC designs are done on individual work stations, not on shared mainframe systems. This percentage will rise as more systems engineers get their own work stations. "The productivity gains of the first few systems purchased in an engineering group have been demonstrated, and now more members of the group are getting their own system and software tools," says Thomas Bruggere, president and chief executive officer of Mentor Graphics Inc., Portland, Ore.

To make sure these productivity gains continue, new front-end design tools are aimed at minimizing the complexity of a 50,000-gate design. New design-entry systems make greater use of the familiar schematic entry, but with higher-level functions, where functional blocks and single lines replace complex multiple-wire schematics.

Typical of the new schematic-capture systems is one from Silicon Compilers Inc., San Jose, Calif. When Silicon Compilers adapted its Genesil silicon-compiler software to the work-station family from Daisy Systems Inc., Mountain View, Calif., they added a new user interface. "Instead of filling out forms, as is done with the existing Genesil user interface, the designer selects icons of circuit elements—an ALU, for example—to enter his schematic," says Dennis Sabo, vice president of marketing at Silicon Compilers.

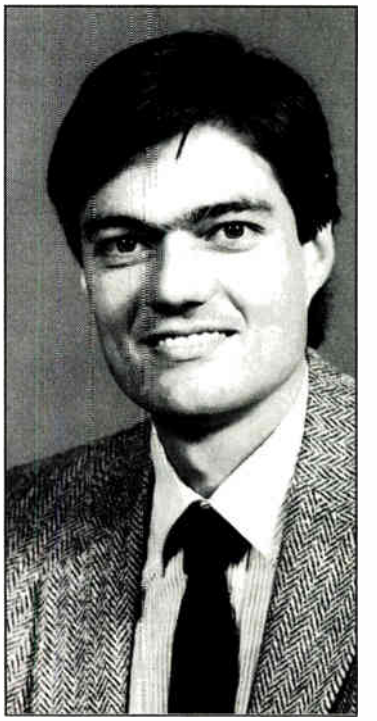
"The designer selects from a Macintosh-like screen display the icon for the ALU," Sabo explains. "The system then queries the designer on the number of inputs to the ALU. After he answers, the system continues with further queries on other characteristics."

Newly introduced tool kits from rivals LSI Logic and VLSI Technology are employing similar high-level graphics symbols for schematic capture. Tools from the two companies allow the designer to mix compiled circuit blocks with standard cells and macrocells, which are library circuits that have been previously laid out.

"Unlike most schematic-entry systems, which require the designer to master hundreds of commands, our new schematic-entry system requires only 15 commands to manipulate schematic symbols, edit the design network, and change waveform data," says LSI Logic's Walker.

VLSI Technology provides two different user interfaces for their new data-path and state-machine silicon compilers. The data-path compiler produces circuits with replicated logic elements interconnected in a regular pattern. The state-machine compiler produces logic blocks whose input and internal state determine their output.

"The user enters the data-path specification by drawing a free-form schematic to describe the interconnection of elements within the data path," says James Rowson, the company's manager of advanced development. The schematic represents complex elements as single blocks—register files, ALUs, counters, and so on—and buses as single lines to minimize confusing details.



ASIC WATCHER: SDA Sytems' Costello predicts a fast-growing market for gate-array and standard-cell design tools that run on work stations.

For entering data to the state-machine compiler, the designer writes commands in a high-level state-machine specification language. "State machines are typically specified in the form of a bubble diagram, but we chose language-statement input because it allows much larger designs to be specified," says Christopher Kingsley, software engineer and creator of the compiler at VLSI Technology. "Bubble diagrams tend to become confusing with more than four states described, and with our compiler we expect the designer to build large state machines."

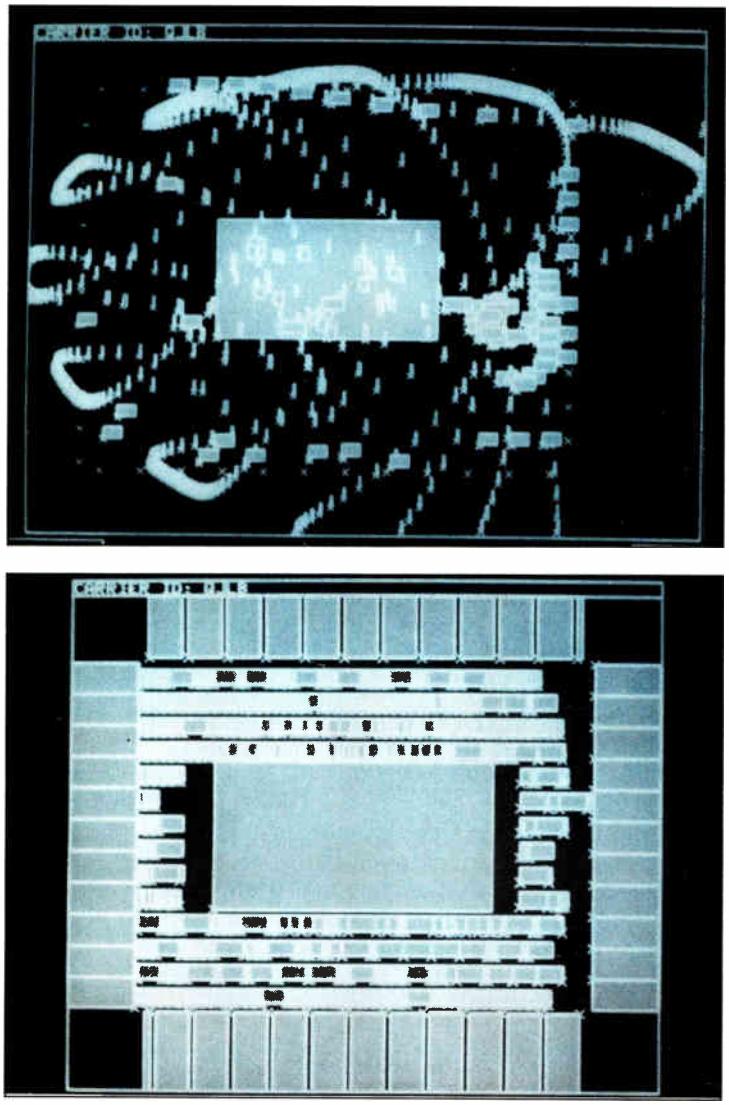
No one interface is the ultimate for all designers and all forms of data entry. "CAE system interfaces are a matter of personal preference," says Silicon Compilers' Sabo. "Some prefer graphics, others like computer languages. And CAE system interfaces will have to accommodate these preferences. Future CAE systems will allow designers to choose the interface they prefer."

'Today a systems company spends 1% of its yearly revenues on CAE hardware and software; by 1990 this figure will grow to 2%'

There is also a big payoff in design time saved to be found in improvements in back-end chip-design software. This back-end software now includes silicon compilers as well as more traditional place-and-route systems.

A large ASIC chip typically will contain one or more large logic blocks, such as a megacell or a compiled data path, and some read-only and random-access memory. Around these larger blocks are found small amounts of logic needed to tie the blocks together and to interface with external logic. The place-and-route tool places these blocks where they will go on the silicon die and makes the interconnections among them.

Most place-and-route tools already offer the ability to place and route standard cells automatically, but most require the designer to interactively fix the location of macrocells. The tool



1. FAST SHUFFLE. Merlyn S from Tektronics CAE Systems is a place-and-route tool set for standard-cell designs. Its quadratic algorithm moves cells around (at top) to achieve optimal placement (at bottom) without iterations, saving computer time.

would then automatically place the surrounding standard cells and route the chip. The next step in the development of this type of tool is to provide automatic placement and routing of both macrocells and standard cells.

Advanced Technology Laboratories at RCA Aerospace and Defense in Moorestown, N. J., has a tool called Happi, a place-and-route tool for chips with up to 500,000 transistors, says Rathin Putatunda, senior member of engineering. The tool requires two metal layers for routing and a third layer of polysilicon that may be used for short distances to resolve routing conflicts. The third layer helps ensure 100% automatic routing but is not always needed.

A physical design system called Vanguard, from IBM Corp.'s Thomas J. Watson Research Center in Yorktown Heights, N. Y., offers similar capability. The system partitions a chip into subchips that define macrocell boundaries, according to Peter Hauge, a research staff member at the center. The subchip contains the macrocell circuit and inter-macrocell connections. It also contains portions of connections that are part of the final chip design but lie within the region of the subchip.

Subchips, which are designed individually, are abutted to assemble the chip. A floor-planning program determines the location of each subchip to meet the criteria of short interconnections, low and balanced wiring congestion, and minimum area. "Vanguard has been used to design a 32-bit microprocessor containing 13 macros, including a large register array," says Hauge.

To minimize chip area and to place and route the chip with a minimum of processing time, each tool supplier has his own algorithm. For example, the CAE System Division of Tektronix Inc. in Austin, Tex., offers two place-and-route tools—the Merlyn-G Gate Array Physical Design System and the Merlyn-S Standard Cell Physical Design System—that use what the company calls the quadratic placement algorithm (see fig. 1). The technique is described as an alternative to placement based on the simulated annealing algorithm, an algorithm that emulates how metals expand slightly to realign their molecules before they can further contract during the cooling cycle of the annealing process. The simulated annealing algorithm is used in RCA's Happi, as well as in a place-and-route tool called TimberWolf, being developed as an ongoing project at the University of California at Berkeley, to progressively expand and contract layouts to achieve maximum compaction.

According to John Blanks, senior software engineer at Tektronix, the Tektronix algorithm requires much less computer time than simulated annealing to perform a placement. In a benchmark Blanks carried out using a small, 2,600-gate array, his technique took 20 minutes to run, while placement using the simulated annealing algorithm took nearly six hours on a Digital Equipment Corp. VAX-11/780 computer. The tool can handle chips with more than 10,000 gates.

Place-and-route tools such as those from RCA and Tektronix are intended for cells that have already been laid out and stored in a library. Other fully automatic place-and-route tools are built to function with silicon compilers for handling cells that have just been compiled. In addition, some of these tools, from Silicon Compilers, LSI Logic, and VLSI Technology, can also mix compiled cells with standard cells and macrocells.

SDA Systems was an early supplier of place-and-route tools. Its MacroEdge product offers the designer automatic assisted macrocell placement and automatic placement and routing of standard cells. The tool makes a rough placement of the larger cells, and the designer then moves the cells for a more optimum placement. A future version of the tool will offer automatic placement of macrocells, the company says. □

LSI LOGIC'S BIG BAG OF ASIC DESIGN TOOLS

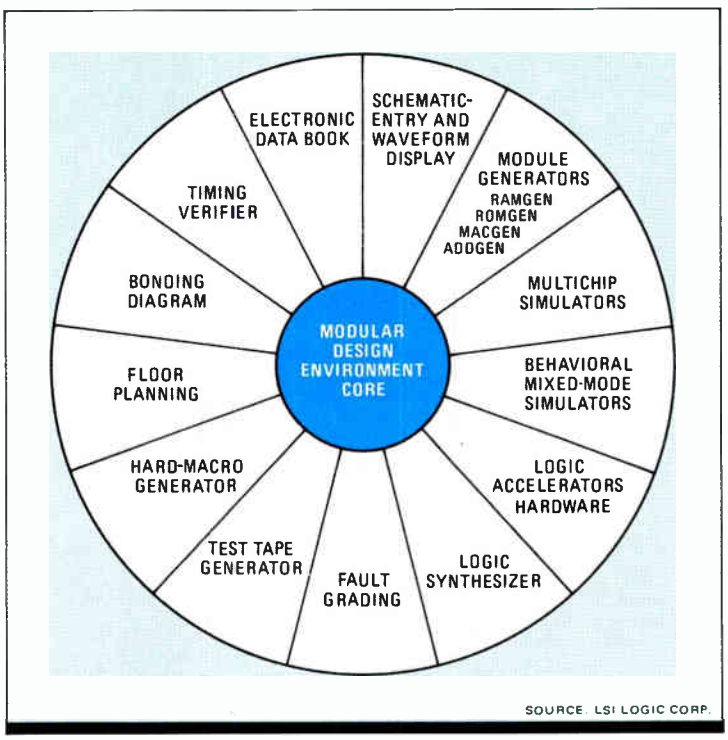
This new tool kit, consisting of a software core, several supporting software modules, and logic accelerators, speeds design of big semicustom chips

LSI Logic Inc. boasts a bulging new tool kit for designing application-specific integrated circuits. The Milpitas, Calif., ASIC vendor now has a computer-aided engineering system that allows designers to quickly create complex chip designs using either gate arrays or standard cells. And designers can simulate a chip within a multichip system having more than 250,000 gates, with gate delays as low as 200 ps. The tool set, called the Modular Design Environment, consists of a software core, 12 software modules, and a logic simulation accelerator (see fig. 1).

Because the Modular Design Environment is designed specifically for today's higher levels of integration, it overcomes many of the limitations associated with previous tools. This latest edition of LSI Logic's tool kit contains new features, such as silicon-compiler module generators, and updated versions of existing tools. It captures large logic blocks quickly and uses schematic entry to provide input and output circuits to the blocks. And it allows simulation of a design's behavior in silicon.

The software core, to which the modules can be added, comprises a logic simulator, a design verifier, a data-base-management system, and associated libraries. Several of the modules, including four silicon compilers (module generators), a logic synthesizer, and a hard-macro generator, reduce entry time to a matter of hours. The module generators compile large or complex functional blocks such as read-only memory, random-access memory, multiplier-accumulators, and adders. The logic synthesizer module—a state-machine compiler—enables existing programmable logic arrays to be entered into a new chip design, saving the time it takes to create and debug a fresh design. A new schematic editor, the schematic-entry and waveform-display module, is used to enter the surrounding circuits to interconnect these logic blocks.

Finally, to help the designer anticipate the behavior of a circuit in silicon and plan the layout accordingly, the tool kit has a bonding-diagram module and a floor-planning module. The former allows the designer to specify the input and output of his chip early in the design; the latter allows him to arrange the placement of the large blocks of his design so as to minimize signal



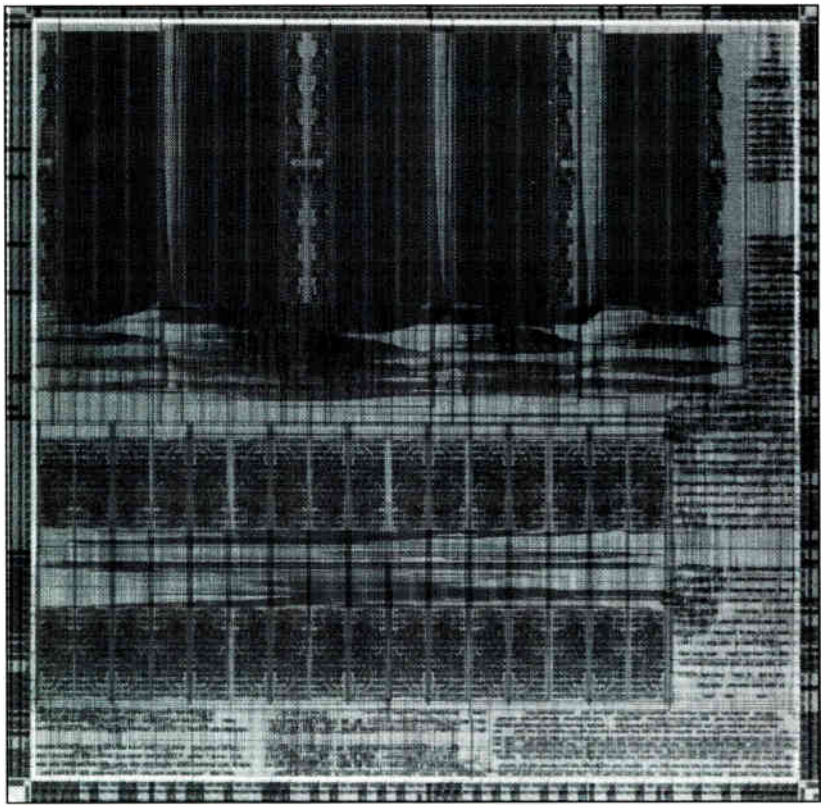
1. TOOL KIT. Supporting the core of the Modular Design Environment are 12 software modules and modified Zycad logic accelerator hardware.

delays in critical paths. The floor-planning module allows him to change the aspect ratio of a block to achieve an optimal layout.

One of the fastest methods for creating large amounts of logic is by using the silicon compilers, or module generators, which generate physical designs from high-level descriptions. The four module generators available now are for RAM; metal-programmable ROM; multipliers and multiplier/accumulators using Booth's algorithm; and fast adders. These compilers differ from others in that they produce large, regular structures as building blocks known as megacells. These megacells are used to implement complete ASICs. The circuits can be implemented in gate arrays or with standard cells.

If the circuit is implemented as a gate array, the compiler produces a netlist that a foundry can use with its place-and-route tools to create the compiled circuit. If the circuit is implemented as a standard cell, the compiler produces a layout that the foundry can use to create the mask layers to build the circuit. In addition, the compilers impose no penalty in performance or silicon area by their use. In some cases the performance is superior to that obtainable, in a finite amount of time, with layouts done by hand.

Another tool in the kit that makes the designer more productive is the logic-synthesizer module. It can combine several PLAs into a single ASIC. Since a typical PLA uses only about 300 gates, many PLAs can be integrated into one chip—keeping costs low, saving board area, and yielding greater reliability. The module's program minimizes the logic and produces a compatible macrocell network that is optimized for both gate count and speed, and is ready for simulation and physical implementation. The logic-synthesizer module accepts inputs in finite-state-machine format (Mealy or Moore models), Boolean equations, truth tables, or PLA format. The tool kit's schematic-entry module, in turn, enables these large compiled blocks and the logic-synthesizer-generated blocks to be connected together automatically.



2. THE RESULTS. This ASIC, built on LSI Logic's Compacted Array, has two RAM blocks compiled by a module generator and 32 medium-size blocks built by a macro generator.

SIMULATION SOLUTION

Once the logic synthesizer and compilers create the logic blocks and connect them, the designer must verify that the design will perform to specification. To do this, the tool kit has a logic simulator called LSIM in the core, plus a behavioral mixed-mode simulation module called BSIM. LSIM, an event-driven logic simulator, can accurately simulate more than 250,000 gates at speeds two to three times faster than similar simulators.

The BSIM module allows functions to be modeled algorithmically at the behavioral level and later simulated at the gate level with LSIM. Simulation time is significantly reduced, and functions are described in a more straightforward manner than at the physical level. Later, behavioral models can be replaced by gate-level models for logic simulation.

After the logic and behavioral simulators ensure that a chip has been designed correctly, the designer can use the multichip simulator module to verify that the chip will work in the final system.

ICs that are to be simulated together—either ASICs or standard products—are described in BSIM or LSIM format. Test vectors are applied to the entire system and its operation verified. After a simulation, design changes are recompiled only if the IC is actually altered. As the printed-circuit board that will contain the final system is designed, actual interchip loading becomes known, and delays may be refined. Individual ASIC test vectors may be extracted for production testing of the ICs, and the system input and output vectors may be extracted and used for production pc-board testing.

The tool kit uses a hardware accelerator built by Zycad Corp. of Minneapolis, Minn., and equipped with a simulation algorithm that is optimized for use with the LSI Logic models. This accelerator provides a more conservative glitch-modeling algorithm than the standard Zycad accelerator. The Zycad accelerator is fully compatible with the LSIM software simulator and supports the multichip simulation feature.

Besides simulating multichip operation, the designer can also plan the layout of each chip in the larger system and establish the location of the input/output pins of each early in the design process. The bonding-diagram module allows the designer to generate an outline diagram of his final chip. The program leads a designer through the steps necessary to generate a manufacturable device, considering such design elements as number and location of power pins, cavity size, and angle and length of wire bonds. It also allows a designer to specify input, output, and bidirectional pin locations.

The tool kit's floor-planning module provides delay control, feasibility checking, and graphical interaction with the designer. The designer can control the effects of layout on the design without time-consuming trial layouts. The program provides the designer with two color-coded displays of the design. The first shows the hierarchy of the design in the form of a tree. The designer can zoom and pan through the tree to observe detail. The second screen shows a color-coded chip plan. Regions on the plan are shown in the same color as the corresponding blocks on the hierarchy tree.

The program automatically provides an initial chip plan that minimizes chip area while maintaining the hierarchy. Along with this plan, the designer receives an evaluation of the "feasibility with confidence level" of laying out the design in the specified chip size. This minimum-area plan, however, does not consider the delay requirements.

With this array of design and chip-layout tools, a designer can now create much more complex chips in a much shorter time, greatly reducing that all-important time to market for new products. For example, in the time it takes to design a 10,000-gate ASIC with conventional tools, the designer can develop a chip design using five times that number of gates. Figure 2 shows a metal-mask-programmable ASIC called a Compacted Array designed with the module generators and macrogenerators. The base array contains more than 400,000 transistors, of which 168,000 are used in this design. The two large blocks are RAMs, compiled using a module generator, and the 32 medium blocks were generated with a macro generator. Using the extensive simulation capabilities available, the designer can ensure that the chip will operate to specification not only individually, but in the total system environment. Finally, the tool set lets the designer lay out a chip interactively to achieve the best use of silicon and the highest performance. □

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

TWO DECADES OF EXPERIENCE WENT INTO DEVELOPING THIS ASIC TOOL KIT

As the old saying goes, the more things change, the more they stay the same. Nowhere is that more true than in the semiconductor business. In the late 1960s there were two programs at Fairchild Semiconductor Inc. in Palo Alto, Calif., called Micromatrix and Micromosaic. The former was to develop one of the first semicustom gate-array products; the latter, one of the first standard-cell products. Rob Walker, James Koford, and Edward Jones were involved in the programs at Fairchild, and more than 20 years later these three are still in the same game, producing similar products at LSI Logic Inc. in San Jose, Calif.

"At Fairchild, we developed most of today's ASIC tools: schematic capture, logic simulation, automatic place-and-route, and automatic test generation," says Walker, LSI Logic's vice president and chief engineering officer. In putting together LSI Logic's new Modular Design Environment, Walker and Koford, vice president of computer design engineering, wanted to create tools to handle gate arrays and standard cells that are much larger than were dreamed possible in the late 1960s.

"Accuracy is very important to us, since we guarantee that the silicon will be correct," says Koford. "If the models or algorithms have a bug, we have to redo the circuit at no cost to the customer. So we have to go out of our way to make sure the tools produce a design right the first time."

Producing the tool kit was a job divided between Jones, LSI Logic's director of topological systems, and Douglas Boyle, the company's director of logic design systems. Boyle joined LSI Logic shortly after it was founded in 1981. He handled the front-end schematic-capture and simulation tools, and Jones did the back-end tools—the floor planner and most of the layout tools.

TOOL KIT TEAM. From left: Boyle, Walker, Jones, and Koford built the Modular Design Environment.

"When we started to develop the tools four years ago, we decided on a strategy of using standard hardware and software," says Boyle. "We selected the Unix operating system and the C programming language as our development environment. They would allow us to port the tool kit to a number of standard hardware platforms."

"When we started the company, we built a tool kit that so far has completed over 3,000 ASIC standard-cell and gate-array designs," says Walker. "In this new tool kit we have continued to improve old tools, and we have added new ones to meet the needs of the next generation of process technology." Boyle adds, "what we did in this new software is to provide much more automated tools for creating ASIC chips."

A COMPILER FOR SEMICUSTOM SOLUTIONS

VLSI Technology's new data-path and state-machine compilers can generate gate-array and standard-cell netlists, as well as full-custom layout formats

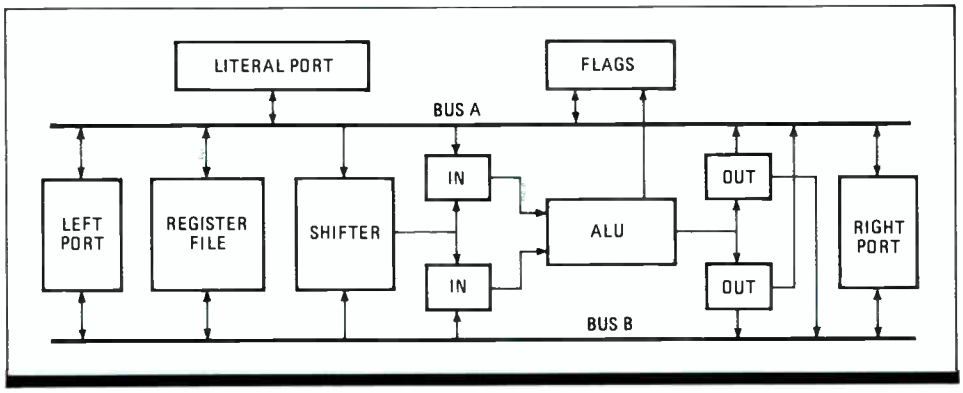
A pair of versatile compilers from VLSI Technology Inc. extends compiler technology into the realm of gate-array and standard-cell implementations. The San Jose, Calif., silicon foundry now offers a data-path compiler and a state-machine compiler that give designers a choice of gate-array, standard-cell, or full-custom implementation of chips with 50,000 gates or more. What's more, the choice of implementation technology can be made after the initial design has been made.

"Both compilers can create full-custom layout, standard-cell layout, or a high-density gate array from a high-level input description," says James Rowson, manager of advanced development at VLSI Technologies. "Now, the designer can choose the implementation medium that best suits his design problem: gate arrays for the fastest turnaround, standard cells for better silicon area efficiency, or full custom for best silicon area efficiency."

The compilers are distinguished by their flexibility. The data-path compiler not only allows the designer to specify any number of general-purpose buses, but also provides a versatile way to wire between bits within the data path. In addition, the state-machine compiler lets the designer specify the speed of the state-machine clock and get a tight layout specifically for that clock speed. And both compilers produce netlists for gate-array and standard-cell implementations.

Until now, the quick turnaround offered by commercially available silicon compilers came with a number of limitations. First, they allowed only full-custom solutions. Second, the number of buses available was only four, which constrained the placement and interconnection of blocks. And third, no commercially available state-machine compilers could produce logic designs optimized for the specific size and performance characteristics of a given circuit.

Previously, for a designer to enter the description of the circuit he wished to compile required that he fill out



1. FLEXIBILITY. VLSI Technology's data-path compiler can overcome the limitations of compilers that restrict the number of buses in this design to four. The new compiler will provide as many buses as needed.

forms appearing on the compiler work station screen. For example, the designer might need an arithmetic logic unit, a register file, a shifter, and other elements of a typical data path (see fig. 1). The compiler would place blocks in the data path in the order in which these forms were entered on the screen.

Other data-path compilers also restrict the bus architecture for a design to two global buses—the two buses running the width of the data path in fig. 1—and two nearest-neighbor buses in the data path, that is, the buses running between blocks in the data path. The former are used for signals common to all blocks; the latter for signals that move between two blocks. A designer must specify the order of blocks to ensure that blocks requiring access to neighboring blocks are adjacent; otherwise, the global bus will have to be used for signals that are specific to only two blocks.

With VLSI Technology's new data-path compiler, the designer can specify nine general-purpose buses without incurring an area penalty. "With so many buses, the designer is no longer restricted in how to place blocks inside the data path," says Rowson. "That means he can build structures not possible before."

For even more flexibility in designing a data path, there is a general facility for wiring between bits in the data path, a function called a swizzle. This allows the designer to reverse the order of bits at any point in the data path.

"To illustrate the power of the new compiler," says Rowson, "we designed a simple circuit (see fig. 2) that generates the timing signals for a high-performance bit-mapped display, up to 2-K by 2-K." The design is fully programmable, Rowson adds, allowing the designer to control the number of bytes of visible data (nvis), the number of scan lines (nlines), and the length of blank (nblank) and retrace (nretrace) lines. The schematic describes a simple data path containing two adder-subtractors, which in this application function as counters. The top one counts visible bytes and blanking lines; the lower one counts scan lines and retrace lines. Inputs to each adder-subtractor are routed through a multiplexer and a D flip-flop.

The designer specifies the width, n, of each of the D flip-flops making up nvis, nlines, nblank, and nretrace. The n refers to the bit width of each element in the data path. The designer is also able to select a fast or slow speed for each portion of the circuit.

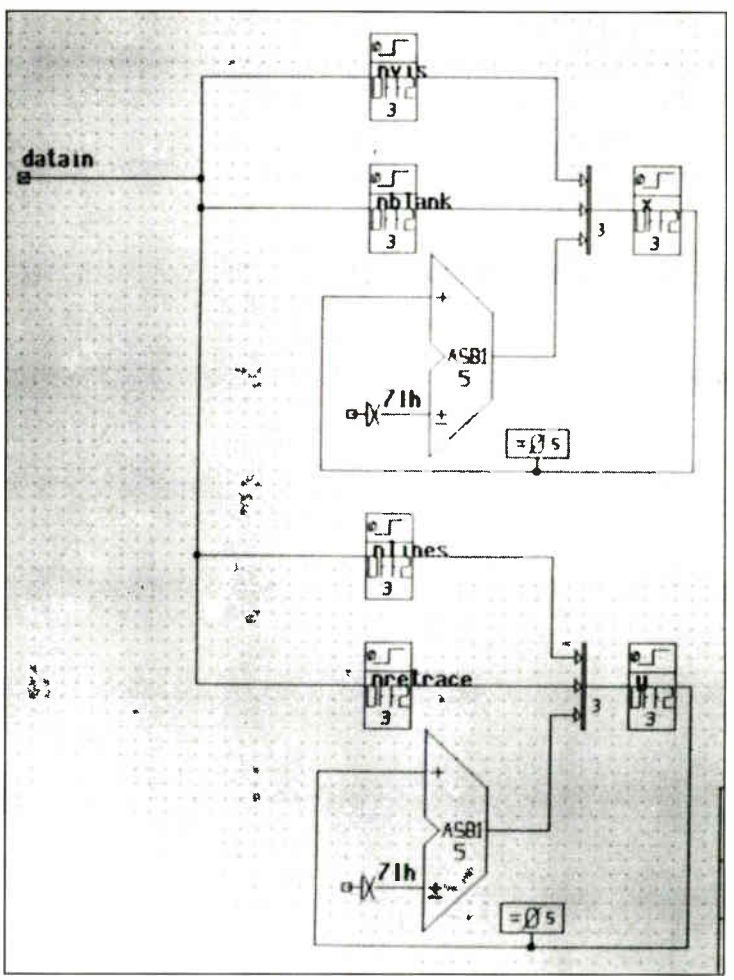
Another feature of the data-path compiler is that the designer can vary the width of the data path from one section to another. "One of the features we observed when creating the compiler was that designers had different numbers of bits in different parts of their data path—for example, a 16-bit adder, an 8-bit register, and a 4-bit register all intermingled," says Rowson.

On other data path compilers, the paths would have to be the same size. In other words, a 4-bit register would be 16 bits long, but only 4 bits would be used. In the VLSI Technology approach, the compiler leaves out unused parts of functional units. If one part of a design calls for a 4-bit register in a gate-array implementation, there will be four pieces of layout—a set of transistors connected to form a register stage—and four unused areas. In the gate-array version, there will be only four flip-flops in the register.

With this feature, if a designer opts for a gate array, he will not have to wire up unused gates. And if he chooses a standard cell, he won't necessarily save the unused space, but he will conserve power.

BUILDING A STATE MACHINE

To direct the operation of the data path requires combinational logic, which VLSI Technology's new state-machine compiler produces. State machines are blocks of logic whose outputs depend not only on their inputs but also on their internal state. The designer uses a simple hardware-description language to specify a design. These statements are converted into Boolean expressions, which in turn are transformed into the final logic function.



2. PROGRAMMABLE. In this circuit, for a bit-map graphics timing generator, the designer is able to control graphics parameters, path widths, and speeds.

"We considered using bubble diagrams to enter the design, which is the way engineers think of state machines," says Christopher Kingsley, software engineer and creator of the compilers. "But bubble diagrams are only easy to use for up to about four states. With larger designs, the diagram becomes a rat's nest of lines too complex to be easily comprehended."

A small number of compiler statements implement the state machine for the bit-map graphics timing generator. VLSI Technology's state-machine compiler differs from other state-machine compilers available up to now in that it allows the designer to specify how fast the state-machine clock is to run. In the new compiler, performance requirements are specified by using defaults, or by providing the loads the outputs must drive, the drive capability on the inputs, and the required maximum delays from inputs or storage elements. The inputs and outputs can be latched, and outputs can have JK flip-flops.

"In compiling a design, the compiler makes a first transformation of the combinational logic," says Kingsley. "If the transformation does not meet the timing requirements, the compiler performs another transformation and continues until the timing specification is met. Once a transformation achieves the desired speed, the compiler attempts to reduce the area of the design to a minimum." The compiler produces a circuit that is nearly the same size as one designed by hand, Kingsley says.

The new compilers allow the designer to delay the decision on chip implementation technology until the final stages of the design process. Other compilers produce a file suitable only for a full-custom layout. To prepare the state-machine and data-path compilers for producing a layout, the designer first draws a top-level schematic that joins the data-path schematic and the state-machine program; then, he completes a parameter cell, which specifies where to find the schematic, whether to perform automatic or manual placement, and what kind of layout to produce.

The designer can request a CIF (Caltech Interface Format) layout format for a custom chip, or a netlist for a gate-array or standard-cell implementation. The system can generate a CIF output in 5 minutes or a netlist in 1 minute. The netlist can be used for either gate-array or standard-cell implementation, because the designer uses the same library of functions that he used when he originally designed the data path and the state machine. VLSI Technology's library is a common set of small-, medium-, and large-scale-integration functions that the company guarantees to work with standard cells or gate arrays in all of its new 2-μm and 1½-μm CMOS technologies. □

FRIENDS AT ROCKWELL HELPED VLSI TECHNOLOGY BUILD NEW COMPILERS

James Rowson, manager of advanced development at VLSI Technology Inc., and his staff got a lot of help in building a new pair of compilers from friends at Rockwell International Corp. in Newport Beach, Calif. "About a year and a half ago, we began planning a new generation of data-path compilers," says Rowson. At the same time, some designers at Rockwell who have a close working relationship with the San Jose, Calif. foundry approached him with the idea of doing a general-purpose data-path compiler.

Rowson and his team set out to build a compiler that would allow designers to choose gate-array, standard-cell, or full-custom implementation after the initial design had been made. Soon after, the decision to build a similar state-machine compiler was made. Rowson gives Rockwell designers lots of credit for features now in the tool. "It was Rockwell's idea that the input to the compiler should be a schematic," he says.

The job of writing the data-path compiler program initially fell to Rowson and William Walker, a senior design engineer in VLSI Technology's silicon applications group. "Jim did the software, and I did the hardware," says Walker, whose job was to build the register cells the compiler would use to lay out a circuit.

JIM ROWSON

BILL WALKER

SURESH DHOLAKIA

CHRIS KINGSLEY

"About a third of the way through the design," Walker recounts, "Jim and I realized we needed to build into the cells the ability to support the 'swizzle' capability [the ability to wire between bits in the data path], as well as to allow blanks in the layout—there had to be a way to leave out cells in an 8-bit register inside a 16-bit data path."

Soon, Rowson brought in software engineer Suresh Dholakia to take over the programming effort. "One addition I made was to write software that allowed a megacell—a previously laid-out circuit—to be merged into compiled layout," Dholakia says. "I made the change after our collaborators at Rockwell, who had been using an early version of the data path, asked how they could perform the function themselves."

The state-machine compiler was the work of software engineer Christopher Kingsley. "We had been considering building a state-machine compiler," says Rowson, "and as a first step we formulated all we felt should make up the tool. Chris took this input, selected the algorithms to use, performed benchmarks to test the compiler's effectiveness, and came up with a product."

SMART MEMORIES ARE EATING INTO THE JELLY-BEAN MARKET

These special-purpose chips, combining logic with memory, could prove to be a potent weapon for U. S. makers in their battle for market share with the Japanese

by Bernard C. Cole

A new breed of memory chip is beginning to take over special-purpose storage tasks from the high-volume jelly-bean chips. Although no one can agree on just what to name this new class of special-purpose parts, they are often called smart memories because they also incorporate the support logic required for control functions and system interfacing.

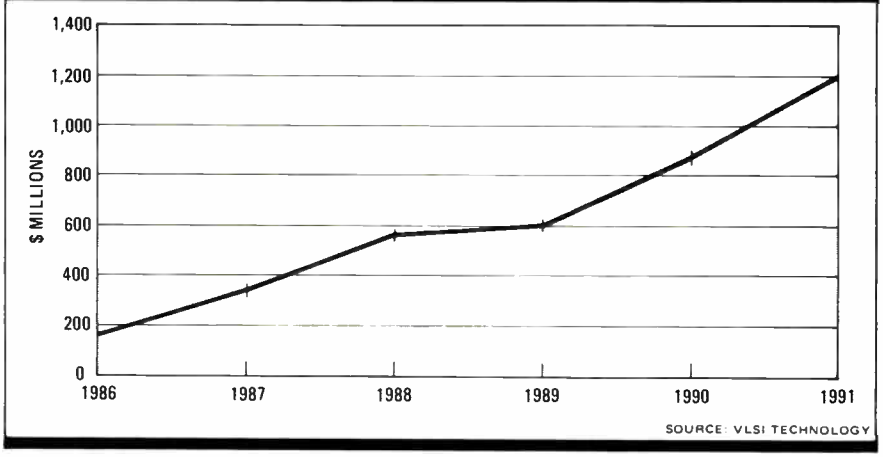
Early entries are random-access memories for the most part, but chip makers are now starting to turn out other special-application types. And not too far down the road are the application-specific memories, in which the user will be able to specify the RAM organization as well as other special features. Another design approach is to put memory on logic chips, and makers are beginning to offer this as metal-mask options on gate arrays and as handcrafted or compiled supercells in standard cells.

A major reason for the emergence now of this type of logic-memory chip—a part that is also known as specialty memory or logic that remembers—is that it relieves the system designer of the job of fashioning such combinations, thereby reducing system cost and time to market. Another cost cutter is the reduced chip count achieved by combining logic and memory on one chip. It boosts performance by eliminating the delay time of an off-chip connection.

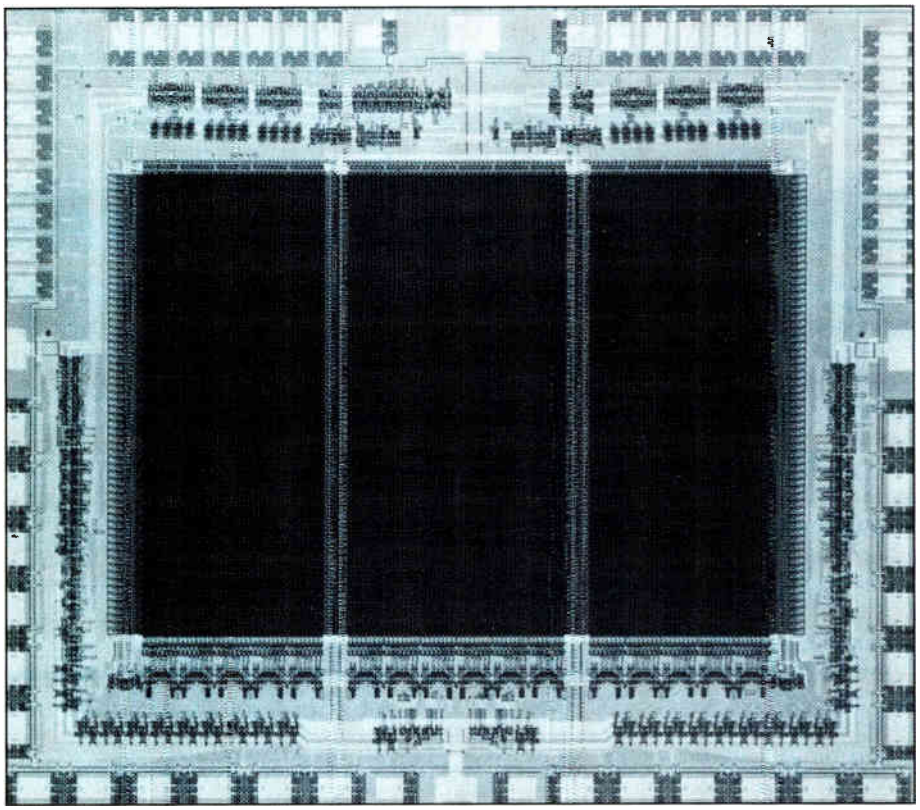
The timing on these specialized memory chips couldn't be better, as far as some U. S. chip makers are concerned. They could prove to be a potent weapon for American manufacturers in their ongoing battle for market share with Japanese semiconductor memory producers, according to Victor DeDios, senior industry analyst with Dataquest Inc., a San Jose market research firm.

A combination of geographical proximity to potential customers, mainly computer manufacturers; a greater degree of systems expertise, particularly in startup memory companies; and more experience in computer-aided design favors U. S. manufacturers in these new niche markets, declares DeDios. The ad-

BOOM FORECAST IN THE U.S. FOR SPECIAL-APPLICATION MEMORIES



SOURCE: VLSI TECHNOLOGY



1. DUAL PORTS. A new breed of SRAM, the VT16AM8 from VLSI Technology, sports dual I/O ports, one 8 bits wide, the second 16 bits wide.

vantage could be short-lived, however, if a special-purpose memory turns into a high-volume market. This is already the case with video RAMs. In such cases, the Japanese, with their track record in producing low-cost, high-volume circuits, will ultimately dominate, says another observer, Thomas Goodman of Vitelic Corp., in San Jose.

Perhaps the most common of these special-purpose parts are a variety of CMOS RAMS, including new multiport video dynamic RAMS, multiport static RAMs, semaphore RAMs, and SRAM-based first-in, first-out buffers. Also falling into this category are even more specialized devices, which include content-addressable memories, cache-tag RAMs, and cache-data RAMs. Semicustom-logic vendors also seek to satisfy the special memory requirements of many systems designers with circuits that use reconfigurable memory blocks in their gate-array and standard-cell-based products. These blocks hold up to 32-K of SRAM and 512-K of read-only memory. Vendors are also considering SRAM-based designs as the best way to achieve gate-array-like densities in CMOS-based programmable logic devices.

Even makers of CMOS electrically erasable programmable read-only memories and EPROMs are incorporating additional logic into their standard architectures to serve niche markets such as data encryption and enhanced error correction. Also, makers of charge-coupled-device memories are modifying their devices, adding the logic to optimize them for digital TV, image enhancement, and data reduction.

The fastest-growing portion of this emerging memory market is the special-application RAM. U. S. sales will grow from slightly less than $200 million last year to $300 million this year and to $900 million by 1990 (see chart, p. 65), predicts one San Jose maker, VLSI Technology Inc. A more conservative estimate comes from Dataquest, which estimates this market will grow to about $700 million by 1990.

Barely two years old, the video RAM, a multiport DRAM used in graphics systems, is the most mature segment of the special-application RAM business. This business, which ran about $10 million in the U. S. last year, will double this year, says David Handorf, general manager of application-specific memory products at VLSI Technology. Video DRAMs support the high-capacity requirements of frame buffers and display memory found in graphics terminals and systems by providing two input-output ports, one for random access and another for serial access. The random-access port is driven by the graphics processor. It is the entry port used for building the screens of data that are to be displayed. The serial port sequentially accesses the memory and performs the various serialization tasks that are necessary to drive a cathode-ray tube or other serial data device. The relative independence of the two ports helps unburden the random-access port, which increases the available bandwidth and makes it easy to change screens quickly, without burdening the central processor.

In early 1985, Texas Instruments Inc. set the standard for video RAMs, combining a 64-K-by-1 DRAM on the same chip as a 256-bit serial-access shift register. Last year TI introduced a CMOS 64-K-by-4 video RAM. It has been quickly joined by a variety of 256-K video RAMs from other makers. Now meetings are being held to consider conflicting standards proposed for the megabit generation of video RAMs. Some designers believe they can use a straightforward extension of the current 64-K-by-4 design, organized into a 256-K-by-4 array with 512-by-4 serial registers. Others believe the 4-bit-wide data port, with four times as much memory behind each data pin, constrains bandwidth for the performance they need. These designers are pushing for a 128-K-by-8 part with 256-by-8 serial registers. Both will probably be made available, says James Koo, vice president of engineering at Vitelic.

The dual-port SRAM marketplace is growing

as rapidly as video RAMs. VLSI Technology's Handorf estimates that these sales will double this year from last year's $5 million to $10 million. In fact, sales are expected to double each year until at least 1990, he says. Current participants in the market include AMD, Cypress Semiconductor, Integrated Device Technology, Performance Semiconductor, TI, VLSI Technology, and Vitelic. Intel and Fairchild Semiconductor are considering a move into this market.

Dual-port SRAMs ranging in density up to 16 K are becoming widely used because they give two independent devices simultaneous read and write access to one memory, says Thomas Goodman, director of applications engineering at Vitelic. "This allows the two devices to communicate with each other by passing data through the common memory. These devices might be a CPU and a disk controller, or two CPUs working on different but related tasks." The dual-port SRAM approach is useful, says Goodman, because it allows the same memory to be used for working storage and communication by both devices, and it eliminates the need for any special data-communication hardware between them.

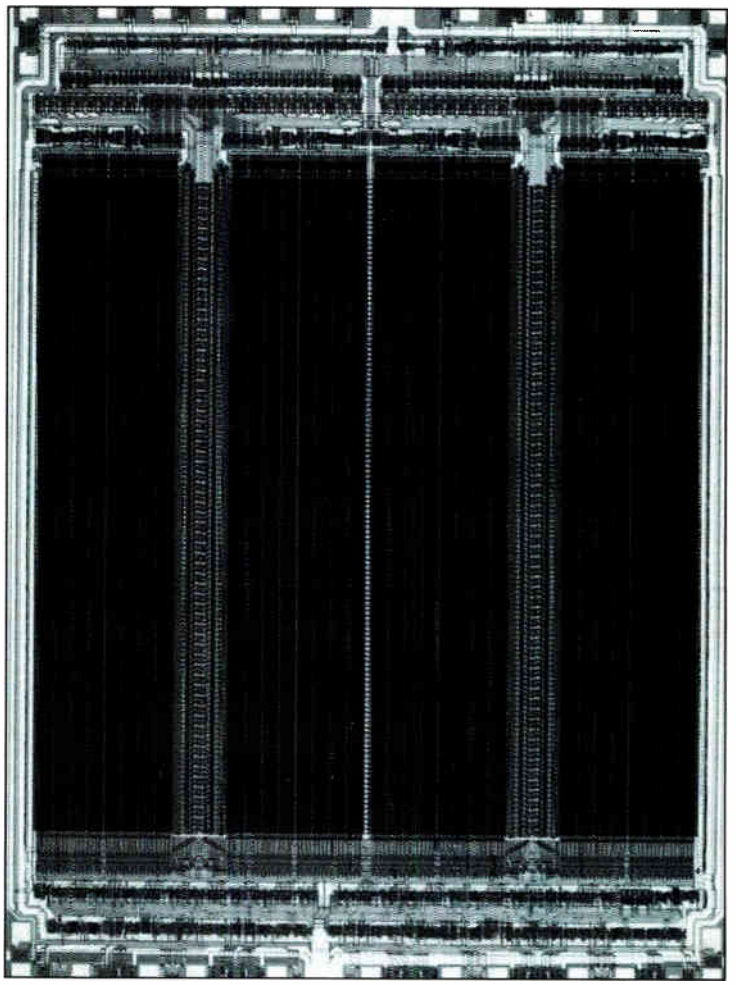
ONE RAM: TWO PORT SIZES

At least one dual-port SRAM comes with different sized ports. VLSI Technology's VT16AM8 aims at solving the problem of data transfers between systems with dissimilar word sizes (see fig. 1). It has a left port organized for 1,024 16-bit words and a right port for 2,048 8-bit words.

Two CMOS approaches are now used to build dual-port SRAMs, says Vitelic's Koo. One approach is to build dual-port memories with special memory cells that add extra transistors so that each memory cell can be written and read independently from two sources. This produces sub-50-ns speeds in 16-K devices, but the approach is density-limited because a 6- or 8-transistor cell is needed. The second approach, used in designs where the emphasis is on lower cost and higher density, retains the standard 4- or 6-transistor cell. However, the entire memory array is switched between two ports using additional multiplexer and arbitration logic so that dual-port operation is simulated. Although this results in smaller dice and lower cost as well as higher density, it doubles the access time.

One of the original special-application memories—the FIFO part—is getting a new lease on life. Unlike earlier shift-register-based designs, the new FIFOs from companies such as AMD, Integrated Device Technology, and Vitelic are SRAM-based. They incorporate separate read and write pointers for addressing the RAM array, so data inserted into the device is available immediately without any of the "fall-through" time associated with shift-register-based FIFOs.

Another advantage, says Vitelic's Koo, is higher density. "Shift-register-based FIFOs now range in size from about 1-K words in depth and from 4 to 9 bits in width," he says. "Shifting to SRAM-type architectures allows much higher density FIFOs. SRAM-based configurations ranging from 512 bits to 32-K deep and 9 bits wide are possible, all with sub-50-ns performance."

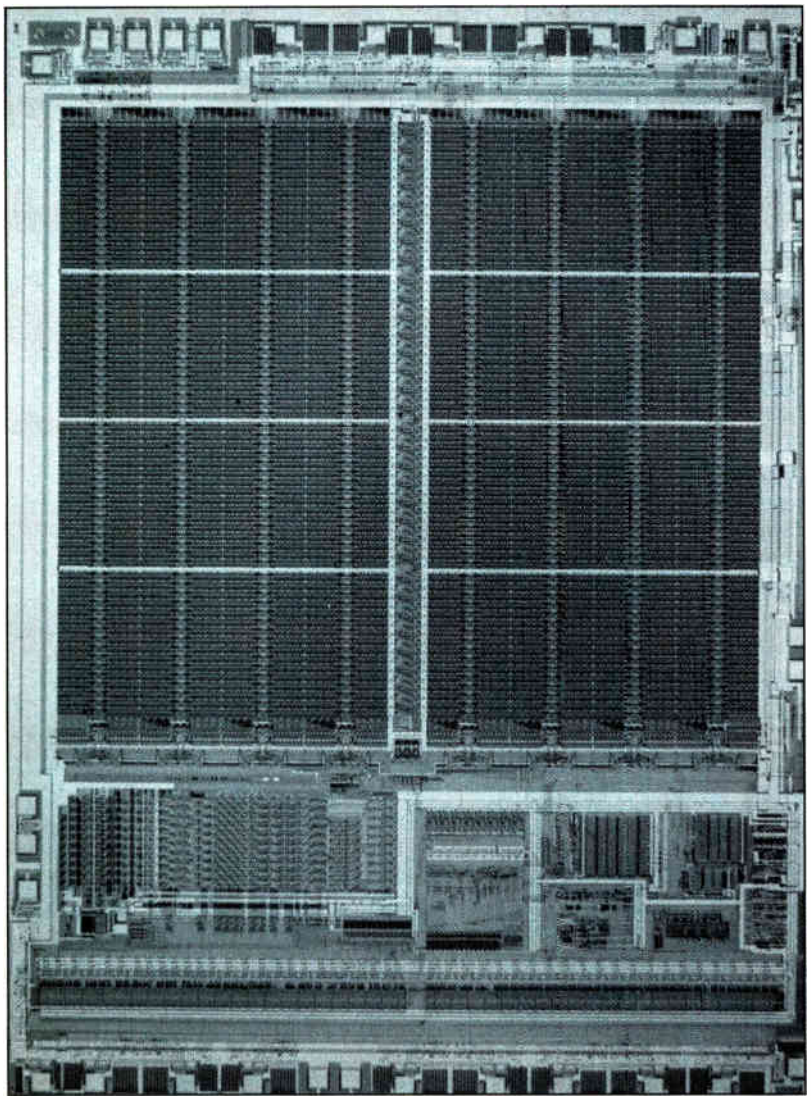


2. PLAYING TAG. IDT's 7174 cache-tag RAM increases speed with a copy of the most frequently used main-memory data.

SRAM-based FIFOs also offer greater flexibility in matching data rates, he says. "In addition to the standard serial in, serial out, you can have serial in, parallel out; parallel in, serial out; or parallel in, parallel out."

Another feature of SRAM-based FIFOs that's exciting system designers is that their storage capacity does not necessarily affect package design, says Goodman of Vitelic. "It is theoretically possible to make a FIFO of arbitrarily large size that will fit into the same package as a much smaller device with the same data width and features," he says. "FIFOs do not need addresses from outside but supply them internally," and therefore do not need external address pins that would increase package size. With this in mind, some companies are developing very-high-density FIFOs up to 256-K built around DRAMs rather than SRAM arrays.

Another emerging special-application memory is the cache-tag RAM (see fig. 2) ranging in size



3. DATA SORTING. AMD's 95C85 content-addressable data manager finds files 500 times faster than software-implemented algorithms.

up to 64 K and available from AMD, Integrated Device Technology, and Motorola. Fairchild Semiconductor and TI may enter this market. Designed to support cache designs by providing the tag comparison on chip, such devices usually incorporate a SRAM array and an 8-bit comparator that performs the address tag comparison. Cache-tag RAMs fit in between the CPU and the slower main memory and increase the effective speed of the main memory by responding quickly with a copy of the most frequently used main-memory data. The first generation of these CMOS devices have direct-mapped architectures: each memory address maps into the cache at only one memory location.

Other cache-memory devices under development will support what are called fully associative and set-associative configurations. In the former, any block from main memory can be stored to any memory location in cache. The latter extends the direct mapping approach but increases the number of locations into which a memory address can be mapped.

An old idea receiving new interest as a special-applications memory is the content-addressable memory, says Steve Dines, CAM product manager at AMD Inc. in Sunnyvale, Calif. It will be mainly used in applications such as artificial intelligence, machine vision, communications control, and various sorting applications.

Although data is written into an addressed location, as it is in a RAM, the CAM operates differently during the read operation. In the read operation in a standard SRAM, an address is asserted on the address pins, and the data stored in the associated locations is recovered from the data-out lines. When a CAM performs an analogous function, the data request is asserted on some input pin and the CAM responds with the addresses, if any, where the data was written.

AMD is currently the only company with a product, the Am95C85 content-addressable data manager, a 1-K-by-8-bit device (see fig. 3). It can manipulate data files up to 500 times faster than a software-sorting routine. Likely to join AMD are Fairchild Semiconductor, Integrated Device Technology, and Vitelic.

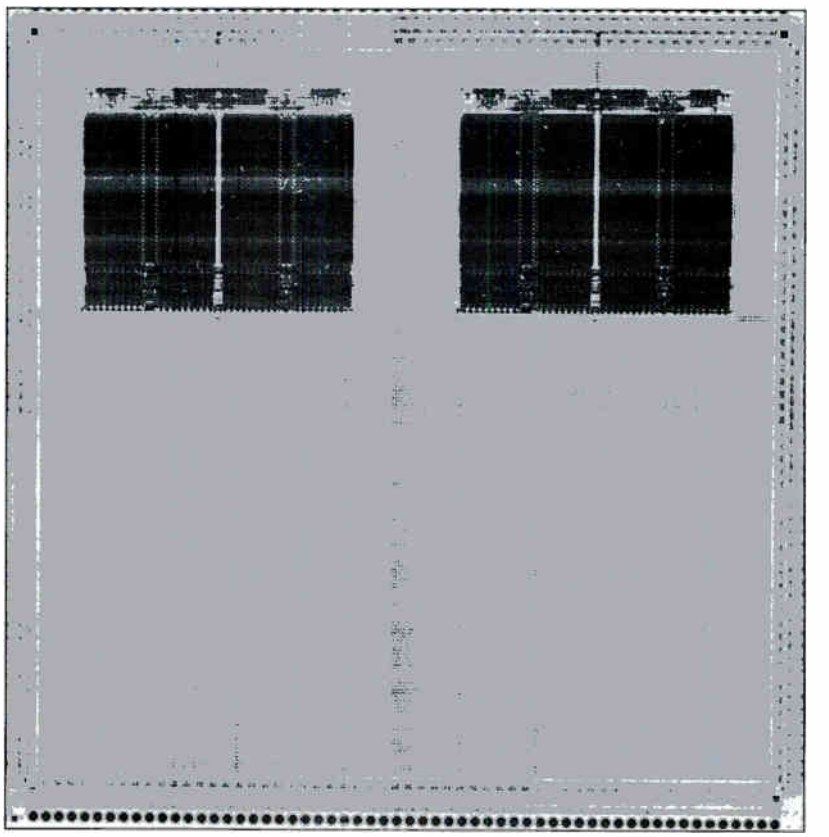
Further differentiation in the special-application memory market is continuing, with new architectures emerging to meet specific system needs. Several companies, for example, are developing semaphore SRAMs to resolve the contention problems faced in the current generation of dual-port SRAMs without sacrificing cost, speed, or density. In this approach, contention between the ports is arbitrated, and status messages are passed using on-board semaphore registers, which are addressed rather than the normal SRAM core when such situations occur. In other variations, vendors are combining disparate special-application memory devices on the same chip to reach a broader market and thus reduce chip costs as volume increases. For example, Hitachi Semiconductor Inc. of San Jose now has available the HD63310, which can be configured as either a 1-K-by-8 SRAM or as two FIFO shift registers of up to 1 K-byte long. It can operate in both the multiplexed and nonmultiplexed mode and has eight semaphore and 32 programmable registers.

Special-application memories with much more on-board intelligence are ready to burst on the scene. For example, Vitelic is developing a counting RAM that combines a simple arithmetic logic unit—whose sole function is to increment or decrement 1 bit of data—and a 64-K dual-port SRAM core. Aimed at applications such as histogram collection, the chip can be configured as either an 8-K-by-8 SRAM, or as a collection of 8,192 8-bit individual binary counters, 4,096 16-bit counters,

or 2,048 32-bit counters. Taking the concept of on-chip ALUs a step further is Hitachi's HM53462, which combines a 64-K-by-4-bit SRAM with several registers and an 8-bit ALU that executes a multiple-step loop without going off-chip. After it is given an address and the operation to be performed, it puts the result back into the memory, shortening the time to do certain logic operations such as graphics and signal-processing tasks.

As fast as the market for special-application memories is growing, application-specific memories could end up leaving them in the dust. Many observers, such as VLSI Technology's Handorf, see an emerging trend toward application-specific chips. Cell-based custom memories will offer the user the same short turnaround and application specificity that ASIC companies now provide for logic designs. And the driving force for this development, says Vitelic's Goodman, are the same powerful computer-aided-design tools that are now starting to transform the way designers implement logic designs [*Electronics*, June 23, 1986, p. 34].

"Virtually every major memory circuit now in production or in development has been designed with the help of these sophisticated CAD tools," says Vitelic's Koo. "And although most vendors' CAD systems are not yet to the point where all the internal pieces of a memory design are components in a standard-cell library, the trend is in that direction." Eventually, a customer will be able to specify an unusual RAM organization and a set of features, and the vendor will be able to quickly assemble the required components into a floor plan, do some manual hookup and tweaking, and generate custom memories in the megabit density range, he says.



4. LOGIC PLUS MEMORY. LSI Logic's LSA1500 series combines up to 37,000 gates and up to 36K bits of SRAM for up to five ports.

FOLLOWING THE ASIC ROAD

An ASIC memory chip may be down the road a bit, but already ASIC logic chips are beginning to offer memory options. ASIC manufacturers are attempting to address the individual memory requirements of systems designers by incorporating large memory blocks into prefabricated gate arrays and incorporating increasingly larger memory blocks into their standard-cell libraries.

Typical of the approach being considered by many gate-array manufacturers is the LSA1500 series from LSI Logic Corp., a family of structured arrays that combines up to 37,000 available gates with up to 36 K of on-chip SRAM and up to five ports with cycle times less than 20 ns (fig. 4). The Milpitas, Calif., company has also just introduced the LSC15 structured-cell library that includes SRAMs up to 38-K, multiport memories, FIFOs, content-addressable memories, and a variety of other types.

Another company applying the concept to cell-based methodology is Unicorn Microelectronics of San Jose with its Compile library of memories. These memories include single- and dual-port SRAMs which are configurable for word width and depth and can support synchronous or asynchronous operation. SRAM-based core FIFOs of any word width and depth can be compiled.

Many other memory and logic suppliers are looking at SRAM-based technologies to extend the reach of CMOS-based programmable logic devices into gate-array densities. A family of logic cell arrays from Xilinx Corp. of San Jose comprises "sea-of-memory" devices with configurable logic and I/O blocks as well as configurable interconnect resources [*Electronics*, Jan. 27, 1986, p. 25]. Currently available in densities up to 1,800 gates, the technology offers the promise of being capable of extension up to the 10,000- to 20,000-gate level, says VLSI Technology's Handorf. To take advantage of this capability, a number of other companies, including Intel Corp., Monolithic Memories Inc. of Santa Clara, Calif., and VLSI Technology are considering entering the market with similar devices.

"However, from whatever direction you come," says Vitelic's Goodman, "the final result in the very near future will in all probability be the same—an integrated memory-logic device that fills a specific application at the lowest possible cost and highest practical utility." □

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Device	Available Speed (MHz)	Description	Alternate Source
8-BIT			
EF 6802	1, 1.5, 2	MPU with Clock and RAM	MC 6802 (A,B)
EF 6803	1, 1.5, 2	8-Bit ROMless Microcontroller	MC 6803 (A,B)
EF 6803U4	1, 1.25, 1.5	8-Bit ROMless Microcontroller	MC 6803U4 (−1,A)
EF 6809	1, 1.5, 2	High-performance 8-Bit MPU	MC 6809 (A,B)
EF 6809E	1, 1.5, 2	High-performance	MC 6809E (A,B)
16-BIT			
MK 68000	8	16-Bit Microprocessor	MC 68000-8
TS 68000	10, 12.5, 16	16-Bit Microprocessor	MC 68000-10, 12
TS 68008	8, 10, 12.5	16-Bit Microprocessor	MC 68008-8, 10, 12
MK 68200	4, 6	16-Bit ROMless Microcontroller	

PERIPHERALS

Device	Available Speed (MHz)	Description	Alternate Source
8-BIT			
EF 6821	1, 1.5, 2	Parallel I/O (PIA)	MC 6821 (A,B)
EF 6840	1, 1.5, 2	Programmable Timer (PTM)	MC 6840 (A,B)
EF 6850	1, 1.5, 2	Serial I/O (ACIA)	MC 6850 (A,B)
EF 6854	1, 1.5, 2	ADLC Controller	MC 6854 (A,B)
16-BIT			
MK 68230	8, 10	Parallel I/O and Timer	MC 68230-8, 10
MK 68564	4, 5	Serial I/O	
MK 68901	4, 5	Multi-Function Peripheral	MC 68901-4
MK 68451	8, 10	MMU	MC 68451-8, 10
TS 68HC901	4, 5, 8	HCMOS Version of 68901	

CRT CONTROLLERS

Device	Description
EF 9345	Alphanumeric — Semi-graphic CRT
EF 9367	Graphic 512 x 1024 Pixels
EF 9369	Palette Circuit 16 x 4096
EF 9370	Palette Circuit 16 x 4096
TS 68483	Graphic — Drawing Processor
TS 68493	Enhanced 68483
TS 68494	Palette 256 x 4096

DSP/DATA COMMUNICATION

Device	Description
TS 68930	High-performance Digital Signal Processor
TS 68931	ROMless version of 68930
TS 68950/1/2	Modem Analog Front End Chip Set
MK 68590	Ethernet Controller (LANCE™)
MK 68591/92	Serial Interface for Ethernet

Local Area Network Controller for Ethernet (LANCE) is a trademark of Thomson Components-Mostek Corp.

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Circle 71 on reader service card

CROSSBAR IC CUTS COST OF PARALLEL PROCESSING

Designers at Texas Instruments Inc., borrowing a page from telecommunications switching architecture, have applied the concept of the nonblocking telephone-circuit switch to digital integrated-circuit design. The resulting new chip will bring low-cost crossbar switching to parallel computing systems.

Until the introduction of TI's AS8840 IC crossbar switch (see fig. 1), only a few large, expensive mainframe computers could use a crossbar switch network for parallel computing. The AS8840 16-port crossbar IC, acting as the nonblocking interconnecting network in a parallel computing system, is dynamically reconfigurable. This provides a flexible wideband path, because a multiplicity of devices connected to the chip can be operated simultaneously. Engineering samples of the crossbar in a 156-pin grid-array package are currently available.

Multiple microprocessors—or other processors such as multipliers, accumulators, and array processors—can now work simultaneously in small systems with memories and peripherals and in small systems with full bidirectionality.

A split architecture enables each of the chip's 16 input/output ports to be independently controlled. The AS8840 allows any two processing elements to interchange data and instructions without interfering with other communications paths (see fig. 2). Splitting also has advantages in self-testing, error checking, and throughput.

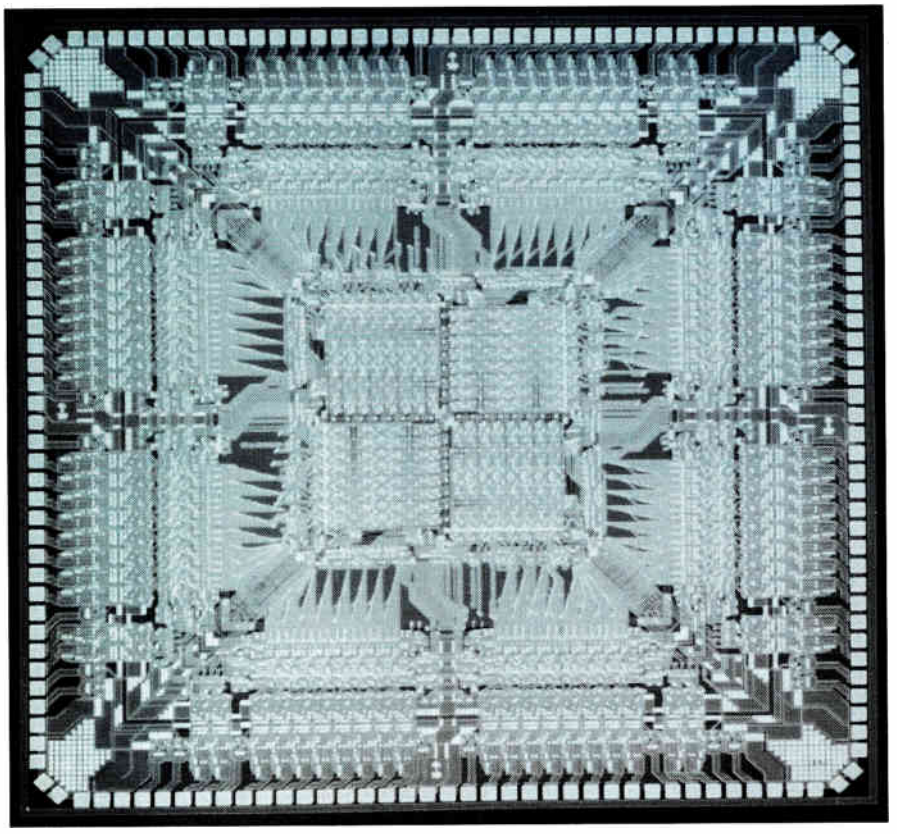
The 16 I/O ports of the 8840 each handle a nibble—4 bits of data—bidirectionally. Each independently controllable port of the 8840 can be set for input or output modes. Therefore, sixteen 4-bit, eight 8-bit, four 16-bit, or two 32-bit processors or other devices can work together on one switch. And connecting their control units in parallel allows several 8840s to operate together.

The circuit is divided into two parts around a 16-by-4-bit data bus, with eight ports in each part. When the control signals are high, data entering the 8840 passes directly to an internal 64-bit bus through a one-of-two selector circuit. When the control signals are low, the data can enter either or both parts of a two-part memory that consists of two groups of eight 4-bit register latches.

Each of the two clock inputs serves the memories of one of the eight ports. Each ports handles 1/16th of the throughput, or one nibble. Users can direct control signals from a master supervisory source or from the processor data flow. Data can travel asynchronously between ports, or it can be buffered in the data-register latches for a store-and-forward operation.

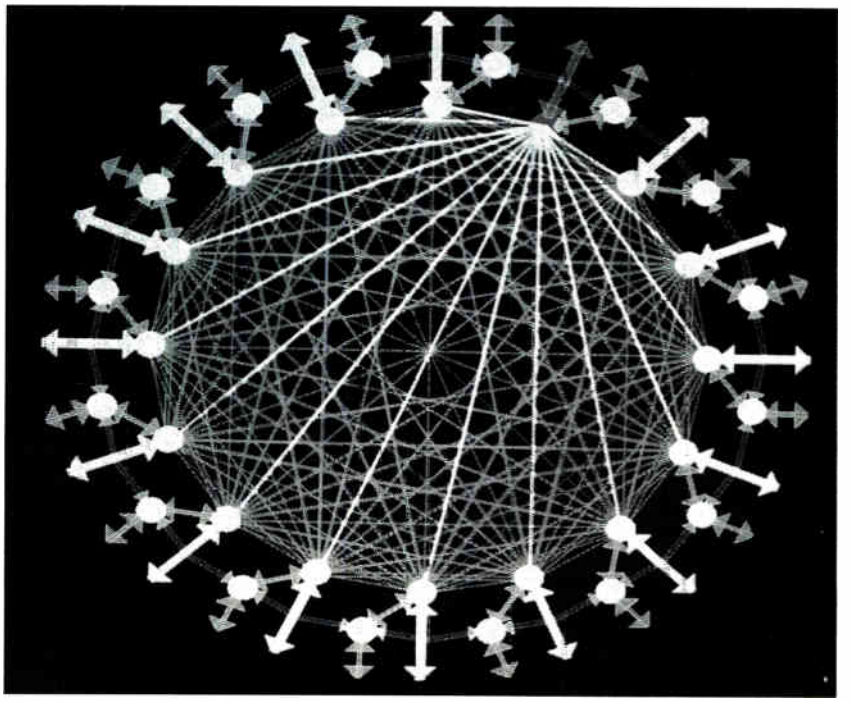
Splitting the 8840 architecture into two separately controlled parts has several advantages. For example, a 32-bit processor sending out data could become a receiver of that data to ensure it passed without error through the network. This is an important feature for fault detection and repair, or even for data rerouting. An automatic rerouting system would allow the design of a truly fault-tolerant computing system.

Also, because the split-architecture arrangement can store two different data sets and select between them under external control, the 8840 is especially useful when the same data must undergo two different permutations a number of times, as in fast Fourier transforms. That procedure can be performed by splitting the switch without repeatedly having to reload the data. Additionally, the two-part register-latch memory allows loop-back functions, such as those that are



1. CROSS CONNECTION. TI's 16-port nonblocking crossbar IC is packaged in a 156-pin grid array for parallel computing.

2. CONNECTIVITY PLUS. Any 4-bit data transfer between two ports is independent of all other simultaneous transfers—thanks to an internal 64-bit data bus.



encountered in sorting operations. Data can enter or bypass the registers and loop back to the input.

The design also provides a flexible approach to handling control signals. Nibbles can be loaded into the control registers from an external source via the control-register nibble input ports or the data buses, and the control signals can be returned via the control register output ports. But four clock cycles are needed for such an entry from the control input ports, as opposed to one clock cycle using the data ports.

The full set of logic-control inputs that are provided with the 8840 crossbar IC permits data paths to be configured to suit such diverse applications as phone networks, radar image processing, FFT calculations, artificial-intelligence applications, and robotics. For example, two 8840 crossbars can handle the switching in a ring topology. One switch, or ring, connects a series of processors to a shared bank of memories. The other switch is ringed with several printers, terminals, disk storage, and memory units. Two I/O circuits and a direct expansion line join the two rings.

Since each line to and from the crossbar switches represents a nibble, the connection between rings carries 12 bits. Larger buses could be accommodated with several AS8840s in a parallel arrangement.

This multiprocessor system is totally nonblocking, because all devices can communicate with all other ones without waiting for a bus to become available. An exception, however, is that no device may be simultaneously addressed by two or more other devices. □

TECHNOLOGY TO WATCH

PARALLEL PROCESSING GETS REAL-TIME DISPLAY

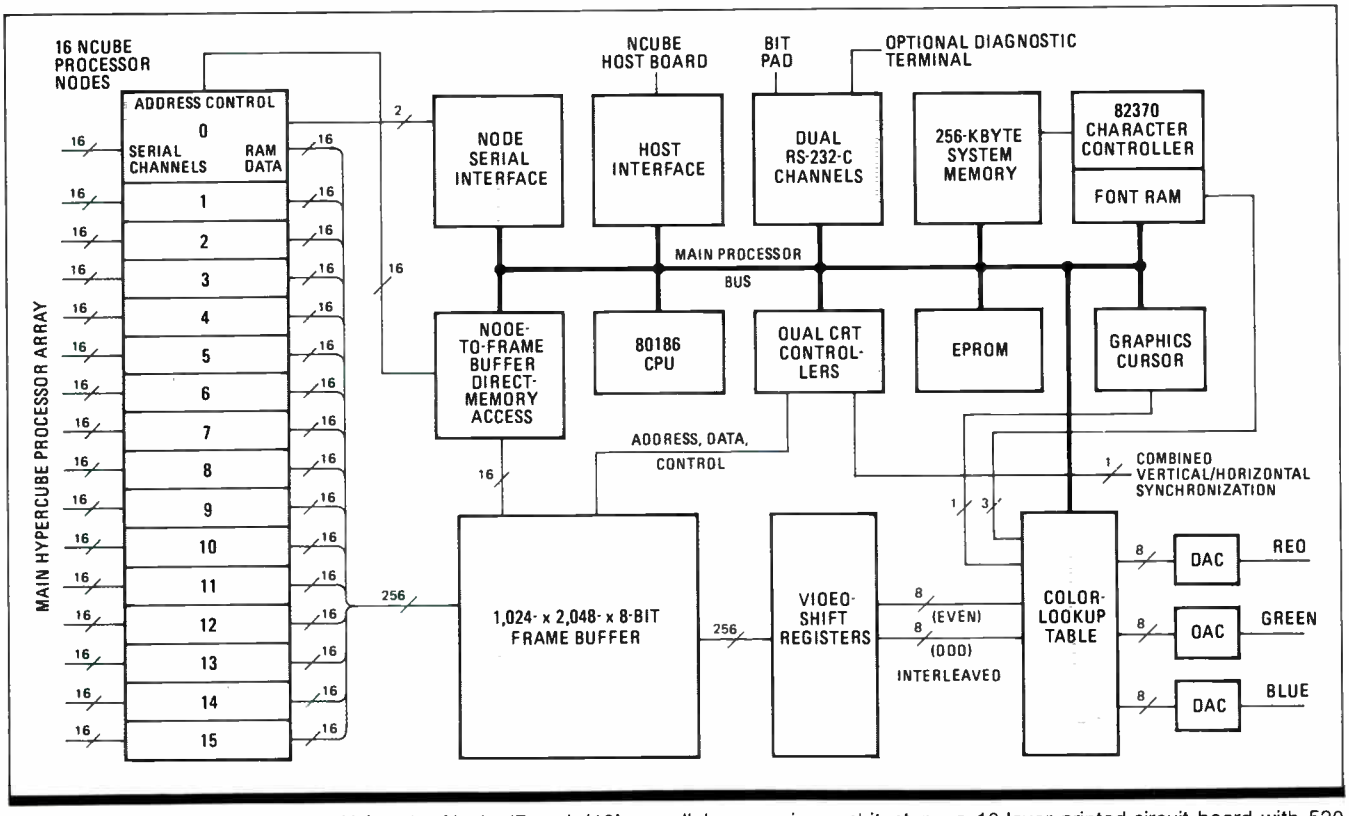
Real-time graphics are coming to the supercomputing world with new hardware and software from Ncube Corp. The Graphics System HP converts the Beaverton, Ore., company's Ncube/7 or Ncube/10 parallel processor from a laboratory-based giant to a personal supercomputer.

The Ncube/7 and /10 provide up to 500 megaflops of computing power. But, as with most parallel processors, it takes extra muscle to extract the output of applications software executing on the machines. A dedicated front-end processor, such as a minicomputer, can be programmed to do the job, but now Ncube users can turn to the $50,000 Graphics System HP add-in board. "The Graphics System HP makes an Ncube machine into a product that has the interactivity of a work station but with an awful lot more muscle behind it," says John Gustafson, staff scientist.

Real-time display of results is desirable because of the complexity of supercomputing applications. "You can solve scientific simulations where you're actually watching the progress of the computation," explains Gustafson. "If you're doing fluid flow, for example, you're trying to see how waves propagate around an object. With the Graphics System HP, you would be able to see the updates on the screen as quickly and as completely as the computer can calculate them."

Similar applications will be important to seismic researchers. Oil companies are currently the largest users of supercomputers and parallel processors, running seismic analysis software to locate petroleum reserves. Other potential applications of a Graphics System HP-equipped Ncube processor are circuit simulation, computer-aided engineering, animation, and photorealistic graphics effects.

Ncube machines each contain 1 to 1,024 nodes. A single node comprises a processor and a communications handler. With 1,500 nodes at 36 customer sites, Ncube claims the largest dollar volume and number of installed nodes of any manufacturer of Hypercube-architecture parallel processors. At the heart of its Graphics System



INSTANT GRAPHICS. Using the Ncube/7 and /10's parallel-processing architecture, a 10-layer printed-circuit board with 530 integrated circuits, the Graphics System HP provides real-time graphics display for supercomputer applications.

HP is a 10-layer printed-circuit board fitted with 530 integrated circuits (see figure). The board plugs into backplane expansion slots in the chassis of the Ncube/7 and Ncube/10 machines and handles three modes.

In the first mode, straight graphics, the board can produce 50 frames/s of graphics at a screen resolution of 1,024 by 768 pixels. Each pixel is described by an 8-bit word, allowing the simultaneous use of 256 colors selected by the user from a palette of 16 million colors. Three graphics boards can be grouped together to provide 16 million simultaneous colors.

The second mode, for drawing, allows users to command the board to draw a variety of shapes, including arcs, circles, rectangles, polygons. An additional feature is a high-quality, high-resolution text mode.

Crucial to the design of the graphics board is its interconnections to the many processors in an Ncube system. The board connects to the Ncube system board via a 128-line bidirectional bus with a 1-megabyte/s data-transfer capacity. On the graphics-board side of the bus, 16 processors act as communications channels to manage the data output by the Ncube system board across that bus.

The 16 processors are tied by a 16-bit data bus to a 2-megabyte frame buffer. The processors are synchronized so that they load a 256-bit word at 50 megabytes/s. Those 256 bits contain 16 bits of information, or 2 bytes, from each of the 16 processors. Since each of the pixels in the 1,024-by-768 screen uses an 8-bit data word, the 256 bits contain information on 32 pixels.

The frame buffer alternately reads data from the communications processors and writes it out to the board's dual advanced CRT controllers. A timing chain on the CRT controllers determines when to deliver a set of pixels to the screen. Using internal registers that store pan and scroll commands, the controller computes an address for the starting pixel and sends that address, along with the appropriate control signals, to the frame buffer.

Multiple banks in the frame buffer send 256 bits, representing a row of 32 screen pixels, to the board's video shift registers. The shift registers then push data to the color-lookup table at 60 MHz. Two sets of shift registers, each representing alternate pixels, are interleaved for higher speed.

Character-generator and graphics-cursor signals are now added to the picture. Finally, digital-to-analog conversion sends appropriate levels of red, green, and blue output to the CRT.

To ease the task of writing programs that use the board's graphics features, Ncube is offering a library of Fortran and C routines. Because the graphics board looks like a device file under Unix, the routines can treat it as if it were a disk drive or similar device. Using the routines, end-users can use high-level-language commands to paint regions of the screen. □

NATIONAL'S CMOS PROCESS TAILORED FOR ANALOG ICs

A new CMOS process from National Semiconductor Corp. that's optimized for analog circuits provides breakdown voltages of 60 V, improved speed, and lower noise and charge injection. Not only are charge injection voltages 10 times lower than current metal- and silicon-gate processes, but gate delays in an inverter fabricated with the new LMCMOS process are only 1 ns, which is one half to one quarter the delay of other available devices. The Santa Clara, Calif., company is using the 3-μm process to produce a wide range of analog circuits.

Key features of LMCMOS are the channel stops and lightly doped drain extensions used to increase breakdown voltage to more than 60 V, without compromising speed. The process is flexible enough to accommodate a wide variety of breakdown voltages and device densities, says Kerry Lacanette, National's manager of analog MOS applications. LMCMOS allows portions of the chip that do not need high speed, such as the digital logic-control circuitry, to be packed more densely by dispensing with the extensions and channel stops and by operating at lower voltages, he says.

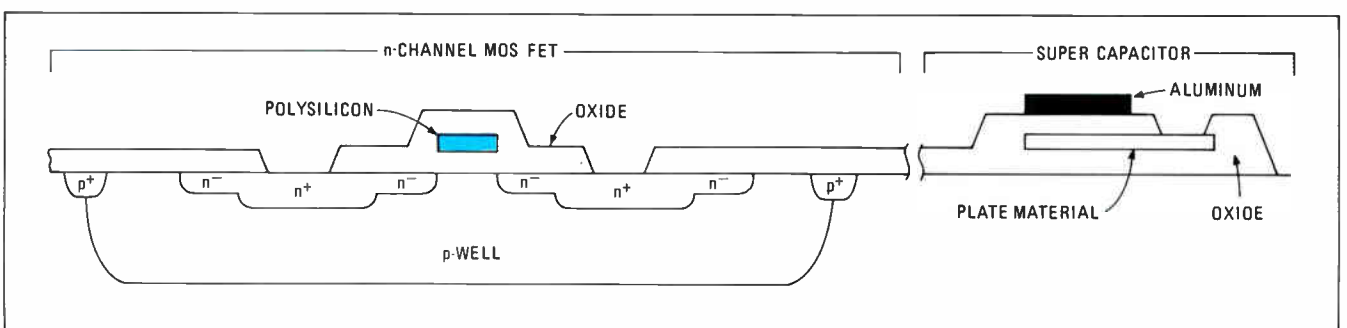
Another important feature of LMCMOS is a self-aligning silicon-gate structure that eliminates misalignment overlap and lateral spreading, both of which contribute to an increased injected charge. "Traditionally, the parasitic capacitance between a transistor's gate and its drain or source causes a charge to be injected into the associated circuitry every time the gate voltage is abruptly changed," says Lacanette. This injected charge produces excess voltage on the internal capacitors in a switched-capacitor filter, which in turn can result in high offset voltages for the overall filter.

Parasitic capacitance is a serious problem in metal-gate CMOS; the gate metal significantly overlaps the source and drain diffusions, because of misalignment and lateral spreading of the source and drain. The inherent self-alignment characteristics eliminate the overlap caused by misalignment in many of the first generation of high-voltage, silicon-gate CMOS processes, according to Lacanette, but the problem of lateral spreading remains. Not only is misalignment overlap eliminated in National's 2-μm self-aligned LMCMOS process, but excess capacitance caused by lateral spreading is reduced with shallow source and drain extensions. In LMCMOS, the overlap caused by lateral spreading is no more than a tenth of a micron, versus 1 μm in standard silicon-gate CMOS and 3 μm for metal-gate. "An additional benefit of LMCMOS is that since the lateral spreading is roughly equal to the vertical junction depth, the shallow extensions further reduce overlap capacitance by keeping the spreading distance small," says Lacanette.

Yet another important feature of LMCMOS is the option of laying down a special refractory metal—using a proprietary process—when a design requires high-quality "supercapacitors." In typical MOS capacitors, a diffusion serves as one plate of the capacitor, says Lacanette. But since the depletion region of the capacitor is modulated by a voltage across the capacitor, its plates move apart as the applied voltage increases. This limits linearity in data-acquisition circuits to about 12 bits at 5 V.

In addition, leakage current between the diffusion and substrate also limits the use of this type of capacitor. Using one of the polysilicon layers as a plate—a common technique in many silicon-gate CMOS processes—eliminates leakage current in the capacitor but will still develop a depletion region.

To reduce to a minimum the resulting voltage coefficient—100 to 150 ppm/V—the LMCMOS process includes an optional supercapacitor that uses the refractory metal as one of the plates. The plate material behaves like a metal, because it has no depletion regions. The plate material's interface with the dielectric is much better than can be achieved with other materials, however, and results in supercapacitor stability of better



INCREASED SPEED. A new process by National Semiconductor Corp., LMCMOS, uses extensions to increase breakdown voltage and speed. Supercapacitors have very low voltage coefficients for high-linearity sampled data circuits.

than 10 ppm over a ±20-V range, with no leakage current.

Some of the first new circuits to use LMCMOS are two quad analog switches, the LMC13421 and LMC13422, which can handle rail-to-rail voltages up to ±20 V. With on resistances of no more than 50 Ω, the result is an improvement in linearity into a given load impedance—0.01% for a 3-V rms signal and a 10,000-Ω load—than is possible with other analog switches, according to Lacanette.

A particularly significant feature of the switches is that they accept TTL-level signals regardless of the supply voltage, he says. "Normally, one would expect a loss in switching speed because of the additional level-translation circuitry and the larger device geometries necessary for high voltage and low on-resistance." Since LMCMOS allows high-speed operation even at high voltage, the switches turn on and off in less than 100 ns, which is about two to five times faster than comparable competitive circuits. "Thus, operation is always break-before-make," says Lacanette, "which ensures that signal sources will not have their outputs shorted together."

The new analog CMOS process is also being used in a series of switched-capacitor filters that operate on supply voltages up to 15 V. In the LMF100, the new process results in dc offset voltages that are an order of magnitude lower than the earlier MF10 universal switched-capacitor filter. This improvement is significant because of the lower charge injection of the new process, says Lacanette, since the high offset voltages—typically around 200 mV—common to the earlier filters previously restricted those filters to ac-only applications. "In addition to improved dc performance, the ac performance is better than it is with metal gate or with other high-voltage silicon-gate processes," he says. "In the LMF100, for example, the center frequency is well over 50 kHz, roughly two and a half times the 20 kHz on other versions of the filter." □

TECHNOLOGY TO WATCH

A WAY TO REWRITE DATA ON MAGNETO-OPTIC DISKS

Researchers at Carnegie Mellon University have discovered a simple method for direct erasing and rewriting on magneto-optic recording media that makes possible the same high-speed direct read, write, erase, and rewrite capabilities as magnetic recording while retaining the very high density of magneto-optics. Until now, the absence of direct overwrite has kept magneto-optic disk drives from competing with magnetic drives, even though they can hold 25 times the bit density of the best magnetic disks.

Magneto-optic recording technology uses a combination of magnetism and laser optics to write a bit and pure optics to read it. That method of writing and rewriting, however, does not permit direct writing—changing a bit on the fly. The Pittsburgh university's team has discovered that the inherent demagnetizing field in the disks' magnetic media can be used to perform erasing and direct writing. The team successfully altered the media formulation to raise the compensation temperature and developed a read-before-write scheme. The technique looks very promising for commercial application.

Magnetic-disk recording changes bits directly with low-flying read/write heads. Until now, no one had discovered how to write directly with magneto-optic technology, because optical recording does not achieve its high density with flying read/write heads. Instead, magneto-optic recording is done with a laser beam on a vertically magnetized medium, which allows for much narrower recording tracks. At the compensation temperature, where the coercivity of the medium is extremely high, the magnetization direction in the medium cannot be changed with an applied external magnetic field, which is used for writing, because that magnetic field is small in comparison with the coercivity.

However, when a spot on the medium is heated by a laser beam to above the compensation temperature, the coercivity of the media spot under the beam drops rapidly. The writing magnetic field will also change the magnetization direction in the domain under the laser beam, a process called nucleating the domain.

The compensation temperature of magneto-optic media is typically close to room temperature—where the drives are used. A beam of polarized laser light reads the magnetic-optic disk, and the light reflected off the nucleated, or reversed, magnetic domains switches polarity, so a bit can be detected.

The current method of erasing data on thermomagneto-optic media reverses the applied magnetic field and reheats the spot, thus reversing the magnetization that created the bit. This method does not provide for simultaneously overwriting new data, however. Usually, whole blocks are first erased, then the new data is written on a second pass.

The CMU researchers discovered that the demagnetizing field in magneto-optic thin-film materials is strong enough to erase a bit. They found that this method worked best in materials with compensation temperatures a few tens of degrees higher than the ambient temperatures.

The technique uses the demagnetizing field in the medium instead of applying an external mag-

netic field to change a bit. This eliminates the difficulties in applying a rapidly changing external magnetic field close to the disk.

Although it has long been common knowledge that the demagnetizing field can be used to write a bit, no one thought it could be used to erase a bit. But the nucleated domain—the region of reversed magnetism—is large enough in relation to the thickness of the medium for its demagnetizing field to do so. The demagnetized field has the strength within the inner regions of the nucleated domain to override the opposite demagnetizing field in the surrounding material, which means it is strong enough to erase the domain.

When the material of the nucleated domain is heated with a laser beam with a Gaussian heat distribution—that is, hottest in the center—the demagnetizing field in the domain's center has more influence than the opposite demagnetizing field in the material surrounding the domain. The heating and the demagnetizing fields create a smaller reversed domain in the center of the nucleated domain.

This yields two sets of domain walls that move together and collapse, leaving the entire domain with magnetization in the same direction as the surrounding material (see figure). In other words, the nucleated domain is gone—the bit is erased. The laser pulse for erasing must be shorter than the pulse used for writing, otherwise the domain would renucleate instead of being erased.

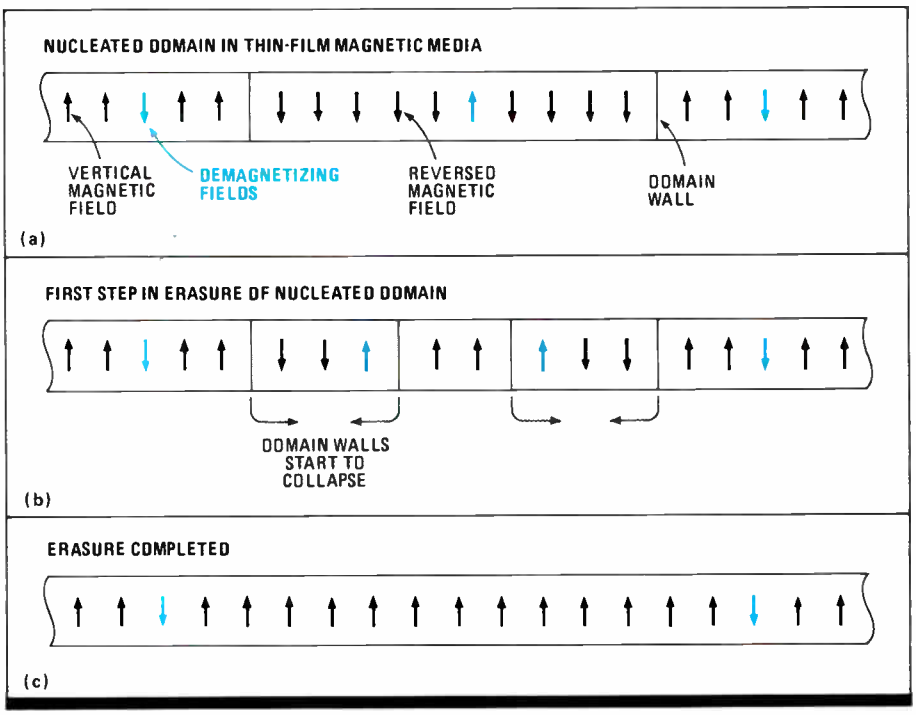
This process is a simple idea, and the researchers have proven that it works. Yet, like many simple ideas, no one thought of it before CMU graduate student Han-Ping D. Shieh presented the idea to Mark Kryder, professor of electrical and computer engineering and director of the university's Magnetics Technology Center. "At first, I was skeptical," Kryder says. "But then I told him to check it out." Together, Shieh and Kryder proved the theory.

The basic theoretical physics does not require that the compensation temperature, T_c, be above the ambient temperature. However, the researchers found empirically that the compensation temperature should be a few tens of degrees higher, in the range of 60° to 80° C, Kryder says, because the coercivity has a steeper fall just above T_c. Raising it means that T_c is closer to the temperature of the erasing laser beam, and the coercivity drops faster. This seems to be crucial for erasure without renucleating the domain. To raise T_c requires only a small change in the composition of the recording medium, which can be done by altering the ratio of the rare earths used in the formulation of the medium. This new medium is no more difficult to make than current media.

A read-before-write scheme was chosen for the direct-writing process. Two laser beams or one split beam can be used. The first beam reads the data on the disk, and a circuit compares this data stream with the incoming write data. The second beam, the changing beam, either erases or writes the bits needed.

This technology is not yet being used commercially. The research was done under contract with General Electric Co., which holds the patent. The technology is being evaluated by a number of companies in the magneto-optic disk-drive business, says Kryder, and it appears that commercial applications are very feasible. The technique works well at high data rates. And in the materials made and tested so far, the researchers have been able to pulse the laser at 10 MHz. Using NRZI coding, they produced a bit rate of 10 Mb/s. With 2-7 run-length-limited coding, they raised the bit rate to 15 Mb/s. Kryder believes that up to 20 Mb/s is possible. These rates compare favorably with current magnetic disk drives.

Computer systems makers and users have been waiting for erasable read-write optical disk drives ever since optical disks were invented. Several schemes for these drives—magneto-optic, phase change, and dye polymer—are under investigation [*Electronics*, May 19, 1986, p. 30]. The CMU discovery may be the development that puts magneto-optics ahead in the race. The technology that gets to market first is likely to survive the longest. Magnetic recording may at last have an optical challenger to its supremacy. □



HEAT TREATMENT. Heating the nucleated domain with a laser creates a reversed domain within the nucleated domain. The domain walls collapse, changing the magnetization and erasing a bit.

WEST GERMANY GRABS THE LEAD IN X-RAY LITHOGRAPHY

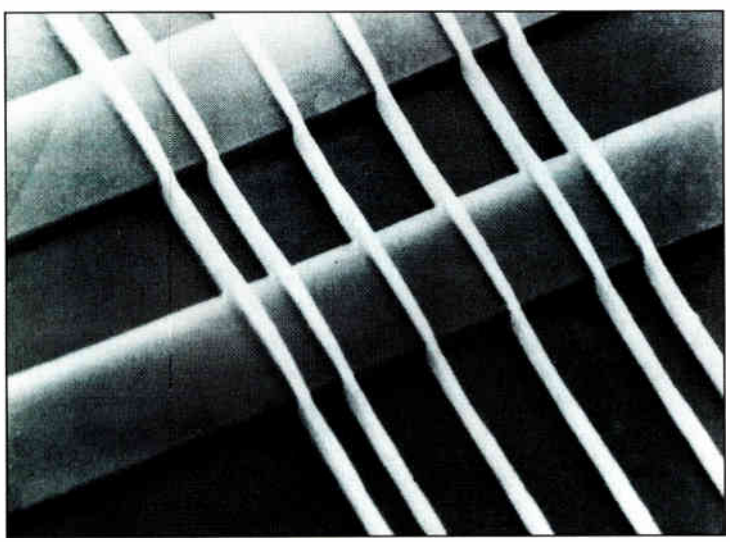
Researchers now produce submicron devices, moving ahead of the U.S. and Japan

by John Gosch

In the international race to make X-ray lithography an important submicron semiconductor technology of the 1990s, West Germany is running well ahead of the pack. Working together under a government-sponsored project, chip makers and systems producers are developing new techniques and equipment—and they've used them to fabricate the first devices made with X-ray lithography.

Although only a year ago it looked like a close three-way race between Germany, Japan, and the U. S. [*Electronics*, March 17, 1986, p. 46], the Germans' reported progress since then indicates that they have pulled into the lead. The West Germans claim they are now one to two years ahead of the rest of the world.

X-ray lithography's strength is high image resolution, down to 0.1 μm (see fig. 1), which makes possible new generations of denser integrated circuits. The technology could become vital to progress in the semiconductor industry in the early 1990s, when 16-Mb dynamic random-access memories hit the market. The chips made by teams from leading West German semiconductor makers do not yet demonstrate X-ray lithography's full potential, but the teams are already on their way to producing devices that can be used in practical applications.



1. VERY FINE. X-ray lithography can achieve 0.1-μm resolution. These narrow lines, crossing 1-μm-high silicon dioxide stripes, are only 0.2 μm wide.

The Germans have also developed the first version of the special wafer stepper needed for X-ray lithography and are working on a second stepper for production environments. A vertical stepper is required, because X-rays emerge from a synchrotron horizontally, and there is no workable way to redirect them. And to deal with the tiny device geometries involved, the stepper must have an automatic alignment system far more precise than existing equipment.

The key to the West Germans' lead over researchers in the U. S. and Japan was their early access to a research synchrotron suitable for X-ray lithography [*Electronics*, March 17, 1986, p. 46]. Another factor is the drive and energy of Anton Heuberger, the leader of the X-ray lithography project and director of the Fraunhofer Institute for Microstructure Technology in West Berlin, which coordinates the national effort.

WORKABLE DEVICES BY 1988?

The chips developed by Heuberger's group were fabricated by teams from two leading West German chip makers, Telefunken electronic GmbH and Siemens AG. Telefunken produced high-frequency MOS field-effect transistors with 1-μm gate lengths; Siemens built metal-semiconductor FETs with 0.35-μm geometries for test purposes. Apparently, they are the first devices ever made with a synchrotron-based X-ray stepper. The project's next phase, which is already under way, envisages high-frequency silicon MOS FETs and bipolar transistors with 0.5-μm features and gallium arsenide MES FETs with 0.3-μm lines. These could be ready as workable devices by 1988.

The next stage after that aims at sub-0.5-μm 4-Mb DRAMs, although commercial 4-Mb chips will probably be built with optical lithography—the last generation of optical-lithography chips before X-ray lithography becomes an important alternative. The introduction of 16-Mb DRAMs and other devices with 0.3-μm geometries, in the early 1990s, should signal the emergence of X-ray lithography.

The X-ray source that has been crucial to the project is the Berlin Electron Storage Ring for Synchrotron Radiation, or Bessy for short. Built during the late 1970s for basic research and tapped by various West Berlin research facilities, Bessy has since been modified to accommodate microelectronics R&D. Of Bessy's 30 or so radiation ports, the Institute for Microstructure Technology—situated in an adjacent building—

rents about one fourth for the X-ray lithography project.

In Bessy, X-rays are produced by electrons racing around a storage ring 20 meters in diameter at the speed of light. The radiation is delivered in nearly parallel rays at a power of more than 100 mW/cm². That much power is needed for the high-throughput step-and-repeat equipment, Heuberger says. The level is adjustable for different sets of masks and resists.

HEUBERGER. The head of West Germany's X-ray lithography project sees a payoff in the 1990s.

A radiation source of the size and cost of Bessy is, of course, impractical for use in semiconductor production at a company's premises. So, for production-line applications, a compact synchrotron storage ring, called Cosy, is now in development at the West Berlin institute. It will be built and marketed by Cosy Microtec GmbH of West Berlin [*Electronics*, May 26, 1986, p. 15].

An even less-expensive alternative is the plasma X-ray source under development at Karl Suss KG, of Munich. However, Suss's LSX 10 is only for laboratory R&D work and small-scale device production. Its exposure time will be on the order of minutes rather than seconds, and the depth of focus will be much smaller than that obtainable with Cosy. A prototype of the LSX 10 will be ready during the first half of this year.

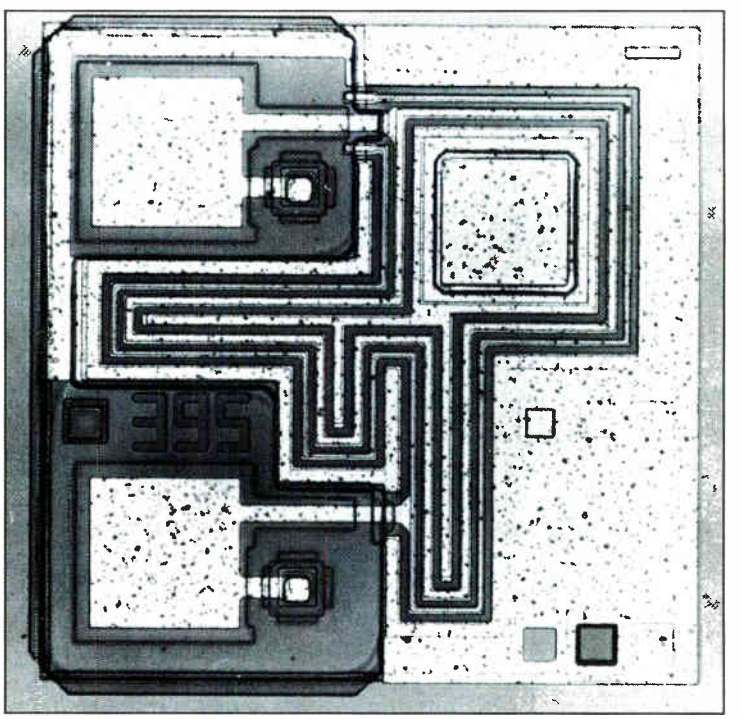
Even without low-cost X-ray sources, the West Germans have passed the pure-research stage: components built with X-ray lithography at the Institute can already be used in practical applications. The 1-μm-gate MOS FETs made by a team from Telefunken in Heilbronn are n-channel dual-gate devices on a 0.5-by-0.5-mm chip (see fig. 2). Although the 10,000-odd devices that Telefunken fabricated last year are mainly for tests and evaluation, the company is offering them for use in, for example, tuners, mixers, and amplifiers for radios and television sets. The working chips arrived about a year ahead of schedule—"a result of shifting our priorities and doubling the manpower assigned to the development effort," says Gerhard K. Lässing, manager for process engineering of discrete devices at Telefunken.

In these devices, X-ray techniques are applied to only one of the 10 or more masking steps—the most critical one, opening the gate stripes. All other steps rely on conventional photolithography. "Using the still-costly X-ray processes for noncritical steps for which the less-expensive standard methods will do is not economical," Lässing declares. However, the 0.5-μm MOS FETs Telefunken will have ready by the end of this year will have two X-ray masking steps, and future bipolar devices and high-density memories will have five and more.

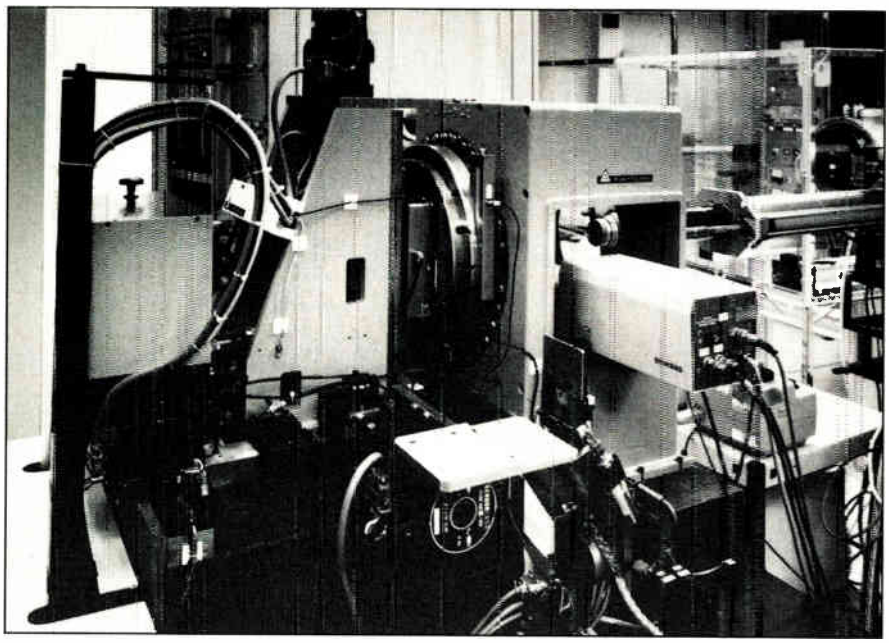
At gate lengths of 1 μm, Telefunken's chips could be made with photolithography. But in making them, Telefunken's goal was not to push fine-line geometries toward their limit, but to compare the effects of optical and X-ray techniques on the devices and to see whether X-rays caused any radiation damage to the devices. They did not, Lässing says.

The parts that Siemens, of Munich, made were fabricated using X-ray-exposed lift-off resist profiles with 0.35-μm features. These profiles, to be used for gate metalization of MES FETs, are test vehicles employed for measuring parameters, determining yields and optimum exposure conditions, and investigating defects. "We are now developing and optimizing test devices with 0.3-μm gate lengths," says Karl-Heinz Müller, a laboratory manager heading the Siemens team at the Institute. Besides device fabrication, Siemens will supply the superconducting magnets for the Cosy compact synchrotron.

An important part of the X-ray lithography project is work on X-ray resists and mask technology. Masks for X-ray work are hard to make, because no known material is transparent to X-rays in relatively thick dimensions, as glass is to light. Researchers are also looking for materials that block X-rays despite very thin dimensions. Telefunken, the Institute, and the AEG Research Laboratories in Ulm have jointly developed a boron- and germanium-doped silicon membrane



2. UNDAMAGED. Telefunken has built about 10,000 n-channel dual-gate MOS FET chips using one X-ray lithography step to check for radiation damage.



3. FIRST STEPPER. Karl Suss KG built the Max I vertical wafer stepper for X-ray lithography work, and Siemens developed its high-precision alignment system.

that carries a gold X-ray absorber pattern.

Meanwhile, the Telefunken affiliate Eurosil GmbH in Munich is trying out a membrane consisting of silicon nitride and is investigating gold and tungsten absorbers. The Philips subsidiary Valvo GmbH, Hamburg, is looking at silicon carbide for membranes and gold and tungsten as absorbers. The Institute will evaluate these membrane and absorber materials.

Besides access to Bessy, another important boost to the West German efforts was the availability, starting in 1984, of an X-ray stepper developed by Karl Suss, which both Siemens and Telefunken used to fabricate their devices (see fig. 3). The Suss machine was the first stepper designed to work with a synchrotron radiation source, according to Elmar Cullmann, senior scientist for R&D at the Munich-based company, although IBM has since built a similar machine.

Designated Max I, the stepper uses a step-and-repeat approach, which Cullmann says is necessary to obtain the mask-to-mask overlay accuracy—better than 0.1 μm—required for submicron design rules. All coarse motions of the wafer relative to the mask (in rotation and in the x and y directions in the wafer plane) are on air bearings and are induced by the step motor in 0.4-μm increments. Fine alignment is done with an x-y piezoelectric stage that moves in 10-nm increments. A second piezoelectric stage rotates the mask. Wafer exposure takes about two seconds and can be done in a conventional air environment—no sealed chamber is necessary, as it is with optical lithography.

Although Max I was developed primarily for experimental work, Suss is now building another model that is intended for volume production work. With its cassette-handling capability for wafers up to 8 in. in diameter, the XRS-200 stepper, when used with Cosy as the X-ray source, will have a throughput of twenty 6-in. wafers per hour for 25-by-25-mm step-and-repeat fields.

The XRS-200 is now undergoing tests. The first system will be installed in the Institute's pilot line by May. The machine will be employed for research on 4-Mb DRAMs with 0.5-μm features and "could pave the way for 16-Mb DRAM production," Cullmann says.

Suss will start taking orders for the XRS-200 in 1987 and hopes to deliver the first systems toward the end of the year. At a cost of $800,000 to $1 million, the XRS-200 alone will sell for less than an optical stepper, Cullmann says. The Cosy synchrotron storage ring is expected to sell for around $6 million. The stepper's price, plus the cost of a share in a Cosy ring, comes to less than $2 million when the maximum of eight steppers are operated on one ring.

Crucial to the stepper's ability to transfer submicron features is its alignment system. To handle such structures, the system must operate automatically with an adjustment tolerance of 0.1 μm. And it must be able to cope with the problems of nonuniform mask-to-wafer distances, varying X-ray-resist thicknesses, and the differing optical contrasts of alignment patterns.

To help solve these problems and to meet the stringent accuracy requirements, Siemens developed an automatic alignment system with an accuracy of around 20 nm, which the company believes is the best such a system has ever done under working conditions. The aligner on the Max I stepper reaches the 20-nm accuracy in about 5 s. Siemens is working on a version for the XRS-200 that can reach the same accuracy in just 500 ms.

The Siemens system implements a light-optical alignment technique based on image processing and pattern recognition, rather than on the interferometric approach commonly used in alignment systems. Instead of evaluating diffraction patterns, the Siemens system processes an optical image in grey-scale levels.

The symmetrical multiple-alignment patterns on mask and wafer consist of crossed lines that form an array of nine squares. The aligner is a real-time pattern-recognition subsystem for detecting the position of the alignment patterns on mask and wafer, and a high-precision positioning unit. Micro-objective lenses project the alignment patterns onto the targets of charge-coupled-device cameras. The outputs of the subsystem control the piezoelectric-driven stage that positions the mask. □

UPDATE: PHILIPS BELATEDLY BEGINS BUILDING IMAGER

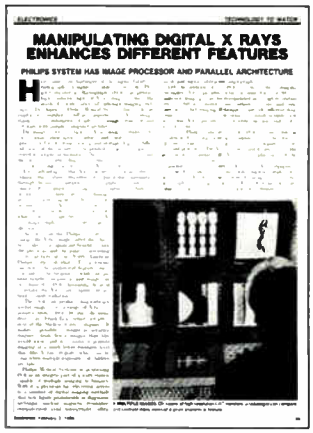
A year ago, Philips Medical Systems Inc. was touting its PCR (for Philips Computerized Radiography system) as the state of the art in medical imaging, but a funny thing happened on the way to market. The Shelton, Conn., company found that the user base for the $600,000 system was more sophisticated than had been anticipated, and advances Philips originally thought could wait for at least six months were needed immediately.

Used in conjunction with conventional X-ray equipment, the PCR digitizes X-ray images and records them on optical disk for storage. The images can then be called up for display on a high-resolution monitor or printed out on hard copy, and images can be transmitted to similarly equipped diagnostic centers around the world [*Electronics*, Feb. 3, 1986, p. 39].

"We had assumed that there would be a gradual movement from hard-copy film [X-rays] to soft-copy displays," says Anthony Lando, marketing manager for computed radiography and imaging physics. "But in reality, we found that the market is driving us toward soft copy and away from film at a much faster rate than we figured on."

With roughly 90% of the orders requesting systems that could be connected directly to a high-resolution CRT rather than a hard-copy printer, Philips had to develop a video-output controller and a local-area-network connection that complemented the system.

The PCR ran into some other problems on its way to market. With a weaker U. S. dollar, Japanese components became more expensive, and Philips had to raise the price of its new machine 9% over the original $550,000 price quote. Also, delivery of the first system to the Oschner Clinic in New Orleans, La., was delayed until late September—about four months behind schedule. The delays were caused by timing difficulties in the system's high-speed processor and problems with the software that ran the system controller board. A task force eventually made hardware and software modifications, such as boosting the clock rate on the processor board, necessary to make the system run. Only now is Philips finally ready to rev into full-scale production, Lando says.


MANIPULATING DIGITAL X RAYS ENHANCES DIFFERENT FEATURES

PHILIPS SYSTEM HAS IMAGE PROCESSOR AND PARALLEL ARCHITECTURE

H

Despite the delays, however, Lando says sales have been right on target. "We sold about 12 to 15 systems into some very prestigious universities in the U. S., and another four to six overseas," Lando explains. "We think we can sell 22 to 30 systems next year." *–Tobias Naegele*

UPDATE: IBM ADDS SUPPORT FOR ITS VECTOR PROCESSOR

The first vector-processing option for an IBM 3090 was delivered on schedule just about a year ago, arriving at Exxon Corp. in Houston on Feb. 28. Since then, use of the option has spread to customers for all models of IBM Corp.'s biggest mainframe—the dual-processor Model 200 that Exxon uses; the two single-processor models, the 150 and 180; and the four-processor Model 400. The first Vector Facility on a 180 went to Shawmut Corp. in Boston on March 17, the first on a 150 to Lockheed Aircraft Service Corp. on June 9, and the first Model 400 with a Vector Facility—an upgrade from a Model 200—was delivered to A. C. Neilsen Inc. on Aug. 22.

Acceptance came readily for the Vector Facility in part because IBM designed it as a natural extension of the 3090, basing it on the System 370 architecture used for the mainframe. That design work was made simpler by IBM's earlier decision to build the 3090 so a vector-processing option could easily be added to it [*Electronics*, Feb. 3, 1986, p. 35]. And, it turned out, IBM's customers were a lot more eager to get a vector processor than the company thought.

The early design decisions are paying off now, says Edward H. Robbins, director of scientific and technical computing for IBM's Information Systems Group. All components of the Vector Facility—hardware, software, and how the vector processor works with the 3090's central-processing units and with MVS and VM, the two operating systems available for it—have lived up to the company's expectations, he says.


HOW THE SIERRA MAINFRAME GOT ITS NUMBER-CRUNCHING PUNCH

IBM 3090 NOW COMBINES PARALLEL, VECTOR, AND SCALAR PROCESSING

W

What IBM found that needed more work, Robbins says, was the way the facility was presented to customers: "We learned that we had to explain to customers how to use the vector facility." Since introducing the Vector Fa-

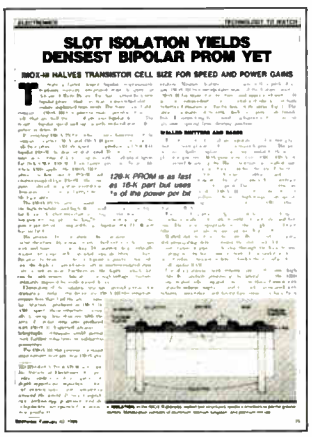
cility, IBM has increased its efforts to help customers transfer engineering and scientific applications programs from other computers to the 3090 and also to optimize their performance.

The company has also been increasing its software support. Additional software introduced during the past year includes an execution analyzer, which identifies parts of programs that can benefit most from optimization efforts, and a vector simulator, which helps users develop and debug vector programs before their vector facility is installed.

The support IBM is giving the vector facility, in fact, has grown into a larger effort to expand its offerings for scientific and engineering computing generally—an area that IBM is setting its sights on as a high-growth market. "This application area is growing much more rapidly than other [computer] fields," says Robbins. "Although we are pleased with the acceptance of the vector facility, we see an opportunity to do better than we thought possible a year ago—there is more demand than you can see with foresight," he says. *–Tom Manuel*

TECHNOLOGY TO WATCH

UPDATE: AMD MOVES INTO PRODUCTION WITH ION ETCH


SLOT ISOLATION YIELDS DENSEST BIPOLAR PROM YET

IMOX-III HALVES TRANSISTOR CELL SIZE FOR SPEED AND POWER GAINS

A year after introducing its IMOX III-Slot bipolar process, Advanced Micro Devices Inc. has transferred the process from its pilot line in Santa Clara, Calif., to its 6-in.-wafer production facility in San Antonio, Texas, and is ramping up for high-volume fabrication of the bipolar programmable read-only memories, random-access memories, and programmable array logic that will be fabricated using the next-generation VLSI process. The process uses reactive ion etching to form slots to isolate implanted transistors, reducing their size by half [*Electronics*, Feb. 10, 1986, p. 35].

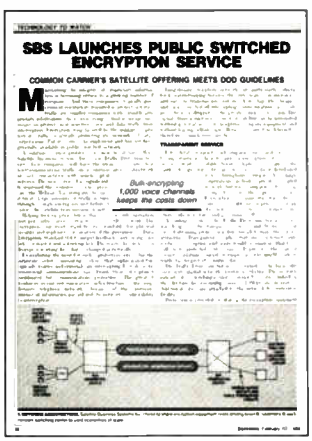
The first product into production is the 27S51, a 35-ns 128-K PROM, which is now being offered in sample quantities, says John Bourgoin, managing director of bipolar PROMs and PALs. Also being offered as samples is the Am100474, a 1-K-by-4-ECL SRAM featuring access times in the 10- to-25-ns range and power dissipation ranging from 1.15 to 1 W, respectively. Scheduled for sampling later this quarter is the Am100480, a 16-K-by-1-ECL SRAM.

The first IMOX III-Slot logic product is the 24-pin AmPAL10H20EV8/10020EV8, a 6- to 8-ns, 125-MHz ECL programmable-array-logic part. Scheduled for introduction in sample quantities later this quarter, it features up to 20 inputs and 8 outputs, says Bourgoin, along with eight user-programmable output-logic macrocells for registered or combinatorial operation.

This will be followed by a 20-pin series of bipolar PALs featuring speeds in the 15- to 40-ns range. Also, the company has seen silicon on 17% linear shrinks of the SRAMs with a 10% to 15% performance improvement over current IMOX III-Slot devices. *–Bernard C. Cole*

TECHNOLOGY TO WATCH

UPDATE: PUBLIC SWITCHED ENCRYPTION GOES PRIVATE


SBS LAUNCHES PUBLIC SWITCHED ENCRYPTION SERVICE

COMMON CARRIER'S SATELLITE OFFERING MEETS DOD GUIDELINES

Secure telephone conversations, a service avidly sought by both business and government agencies—especially the secretive ones—were promised a year ago by Satellite Business Systems Inc. when it announced its Traffic Protection Service. By bulk-encrypting 1,000 voice channels, SBS said, it could offer for the first time a low-cost, public-switched encryption service. To initiate the service, SBS installed at least one bulk encryption unit on each of the 25 earth stations in its Skyline nationwide digital network to be able to offer transparent encryption service on up to 1,000 lines simultaneously [*Electronics*, Feb. 10, 1986, p. 38].

Since then, MCI Communications Corp. has acquired SBS from IBM Corp. and Equitable Life Insurance Co., and in the wake of the acquisition, the status of the encryption service is unclear. MCI refuses to comment on the use of encryption, citing the sensitive nature of the business as the reason.

An MCI spokesman says that MCI does not want to say any more about the service because of the company's close relationship with the National Security Agency. If the bulk encryption units are still installed and working, many telephone conversations among government agencies and between them and their contractors may be protected by encryption without the speakers being aware of it. *–Tom Manuel*

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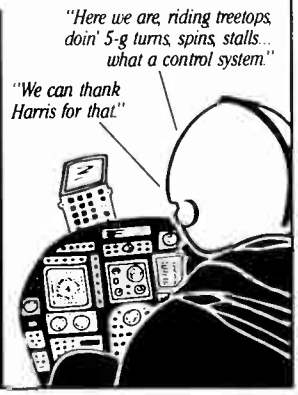

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MILITARY/AEROSPACE NEWSLETTER

NSA PROJECT TO DEVELOP OFF-THE-SHELF SECURITY DEVICES IS RUNNING LATE

Project Overtake—a partnership formed almost two years ago between the National Security Agency and 11 electronics companies to develop a series of standard embedded communications security, or Comsec, devices—is nearly a year behind schedule. At the program's inception, the NSA had estimated that upwards of 85% of all future telecommunications security needs would be met by these devices. However, Phase I of the program is scheduled to end in March with few, if any, products in sight—and spokesmen for several of the companies say no products will appear before late 1987. Windster, the project's proposed line of embeddable modules for encryption of digitized voice and low-speed data signals, is still in the design cycle. Under consideration is the development of the Mini Windster, a cut-down version of Windster. Another product line, called Foresee, intended to provide high-speed digital data streams at all classifications levels, has been downgraded from a government-classified program to commercial-version status and renamed Brushstroke. The main reason product development is moving so slowly, according to several companies participating in Project Overtake, is that the communications and computer security market remains unclear and difficult to define. A recent market study by the Electronic Industries Association's Government Division [*Electronics*, Jan. 22, 1987, p. 95] indicates there's another problem: resistance within the Defense Department to embedded security products, primarily because of concern about how they will fit into currently installed systems. The NSA is expected to ask the 11 companies in March for a memorandum of understanding on yet another new product—Indictor, a secure hand-held radio. □

WESTINGHOUSE LEADS TEAM DEVELOPING FASTER WAY TO MAKE GaAs WAFERS

Westinghouse Electric Co. will head a three-company team to develop technology that will attempt a 20-fold productivity increase in gallium arsenide wafer production over the next two and a half years. Armed with a $1.3 million contract from the Aeronautical Systems Divisions at Wright-Patterson Air Force Base, Ohio, Westinghouse will be joined by Emcore, a New Jersey-based manufacturer of advanced epitaxy systems, and Stauffer Chemical Co., of Westport, Conn. The team hopes to increase the production rate and lower the cost of coated GaAs wafer preparation, which involves coating sliced crystals of the semiconductor with an electronically active layer so that both crystal and coatings are precisely aligned. The work will be carried out using the metal-organic chemical-vapor-deposition process at a new laboratory at the Westinghouse Research and Development Center in Churchill, Pa. Emcore will help equip the laboratory; Stauffer will provide the chemicals. □

NASA REJECTS UTC's BID TO BUILD UNMANNED PAYLOAD CARRIER

The National Aeronautics and Space Administration has shot down an unsolicited proposal for an unmanned payload carrier that could be used as a supplemental space-shuttle launch vehicle. United Technologies Corp.'s Defense and Space Systems Group, Hartford, Conn., submitted the proposal last November. There is no request in NASA's fiscal 1988 budget for expendable or unmanned spacecraft [*Electronics*, Jan. 22, 1987, p. 96]. NASA's Marshall Space Flight Center in Huntsville, Ala., told United Technologies that even if the space agency were interested in the proposal, it would require independent development of specifications and competitive bidding. United Technologies' plan was for an unmanned space vehicle initially capable of achieving a low-earth orbit with a 115,000-lb payload. The vehicle was to use existing shuttle hardware and software. The company said the spacecraft could have been operational within three years of approval. □

MILITARY/AEROSPACE NEWSLETTER

20-IN. COLOR LCD IS TARGETED INITIALLY AT MILITARY

The military most likely will be the first customer for a flat-panel, 20-in. color television system that uses fiber-optics and liquid-crystal-display technologies, according to its developer, Tru-Lyte Systems, Beaver, Pa., a fiber-optic research company. Eventually, larger versions of the system with at least 50-in. screens will be marketed as point-of-sale displays in shopping malls, for use in sports stadiums, and possibly as home TV sets. However, the Naval Ocean Systems Command in San Diego is currently using a prototype of the system, on which patents are pending. The display uses colored liquid-crystal cells that are illuminated by fiber-optic strands, operating off a single light source similar to a light bulb. Tru-Lyte executives report ongoing discussions with other Defense Department agencies interested in using its new display system, primarily as a status board for critical information. □

SDI RESEARCH MOMENTUM BUILDING, ACCORDING TO STUDY

The Pentagon's position that a space-based defense system could be deployed by the early 1990s has gained support from The Heritage Foundation, a conservative Washington, D. C., think tank. "The momentum of SDI [Strategic Defense Initiative] research is greater than originally anticipated, and what once seemed probable now seems certain," says Kim R. Holmes, deputy director of defense policy studies. Holmes cites such advances as the ability to intercept ballistic missiles both inside and outside the atmosphere. With improvements of existing technology, he adds, SDI could soon provide a terminal defense against short- and long-range ballistic-missile warheads. Holmes believes the best candidate so far for a strategic defense against missile warheads is the Army's Exoatmospheric Reentry Vehicle Interceptor System. Using current technology, for example, "limited discrimination techniques" could be developed that would separate decoys from real warheads in space, Holmes says; a "perfect system" solution to the discrimination problem isn't necessary. □

REPORT CALLS FOR UPDATE OF EXPORT CONTROLS

Although national-security export controls are "a necessary and appropriate mechanism" for impeding Soviet-bloc efforts to acquire militarily sensitive commercial technology, U. S. export controls cover too many products and technologies to be administered effectively, according to an 18-month study by the National Academy of Sciences. The study takes the government to task for not justifying ongoing control of some classes of memory chips traded outside the Communist bloc, "technologies that may be of marginal military significance." The study panel requested, but did not receive, information from the Pentagon on the military significance of these so-called low-level technologies. But the panel says it determined on its own, through two fact-finding missions, that many products restricted by the U. S. are available in other countries with little or no restriction. □

TRW CENTRALIZES MILITARY R&D

TRW Inc. has centralized its military research and development activities with the formation of an Office of Technology within its Defense Systems Group, Redondo Beach, Calif. Crawford W. Scott will direct the new operation. Barry W. Boehm, as chief scientist, will be responsible for the group's Ada office, technology education program, and software development. The office will be responsible for development of strategic technology plans, including TRW's Strategic Defense Initiative projects, its independent research and development programs, and other technological efforts. □

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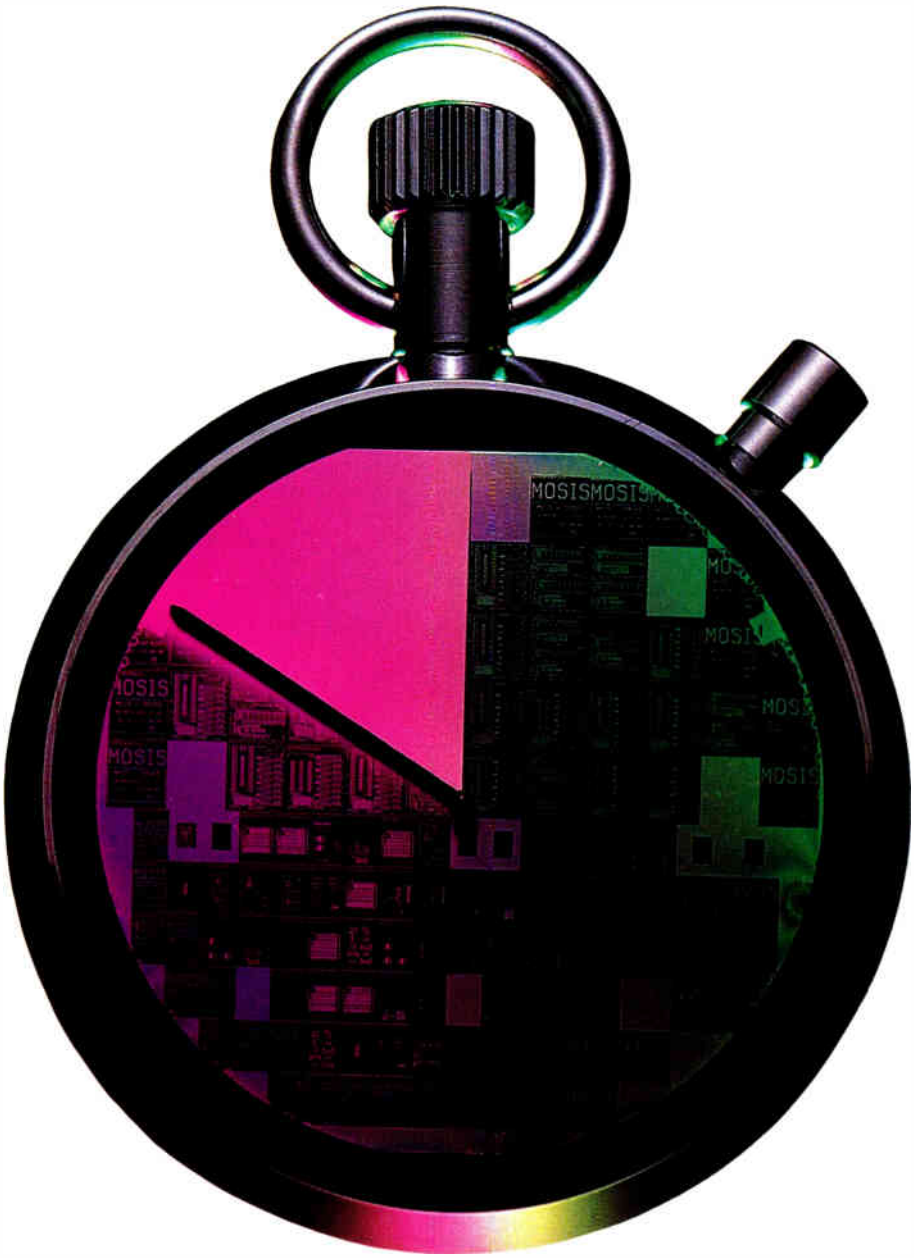

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WHAT'S NEW IN LABORATORY INSTRUMENTS

TRADITIONAL PRODUCTS GET SQUEEZED BY NEWER GEAR

Faster and smarter products are keeping up with new testing requirements—and crowding traditional lab instruments in a market where growth is slowing

by George Sideris

Time was when the test and measurement needs of almost every engineer could be satisfied by an analog oscilloscope, a handful of meters, some signal sources, and the like. These laboratory instruments still do yeoman's duty on many a designer's bench and in the field, but newer gear such as logic analyzers, digitizing scopes, and arbitrary waveform generators are crowding them. Now many more types of lab instruments are competing in a market where growth is slowing.

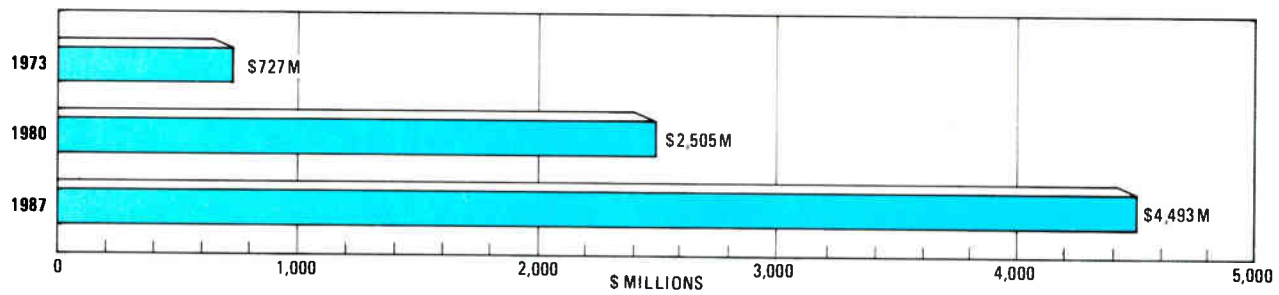
While the slack user demand that pervades the electronics industry is a contributor to the slowdown, the driving force is new technology that demands new kinds of T&M equipment. As users invest more and more money in computer-aided design and engineering systems, automated test equipment and other development and test systems, lab instruments have been left in the lurch. These developments will continue to shrink the traditional lab instruments' share of the overall T&M market. Moreover, increases in future spending on all forms of conventional T&M equipment—including the newer gear such as digital analysis systems—will be small compared with spending on factory automation networks and other new forms of T&M systems.

In other words, lab instruments are being squeezed into a smaller share of the overall market and are beginning to experience relatively low growth rates. Yet, some of the old-line instruments are bouncing back, rejuvenated by new technology: the oscilloscope is the prime example.

In the billion-dollar scope sector, two strong growth paths have emerged, both reflecting technological advancements. The first includes instruments with bandwidths well above 100 MHz, which is the performance needed to keep up with continuing increases in semiconductor-chip performance. The second is in digitizing oscilloscopes. Digitizers—also known as digital-storage scopes—are better suited for advanced development work because they store waveform data and can process, recall, and

1. MULTIPURPOSE TESTER. Digital analysis systems such as Tektronix' DAS 9200 can replace cascades of logic analyzers for ASIC verification and multiprocessor debugging.

THE U.S. GROWTH RATE SLOWS FOR LAB INSTRUMENTS



SOURCE: *ELECTRONICS* MARKET REPORTS

compare this waveform data. For instance, some new models contain fast-Fourier-transform processors to operate in a spectrum-analyzer mode.

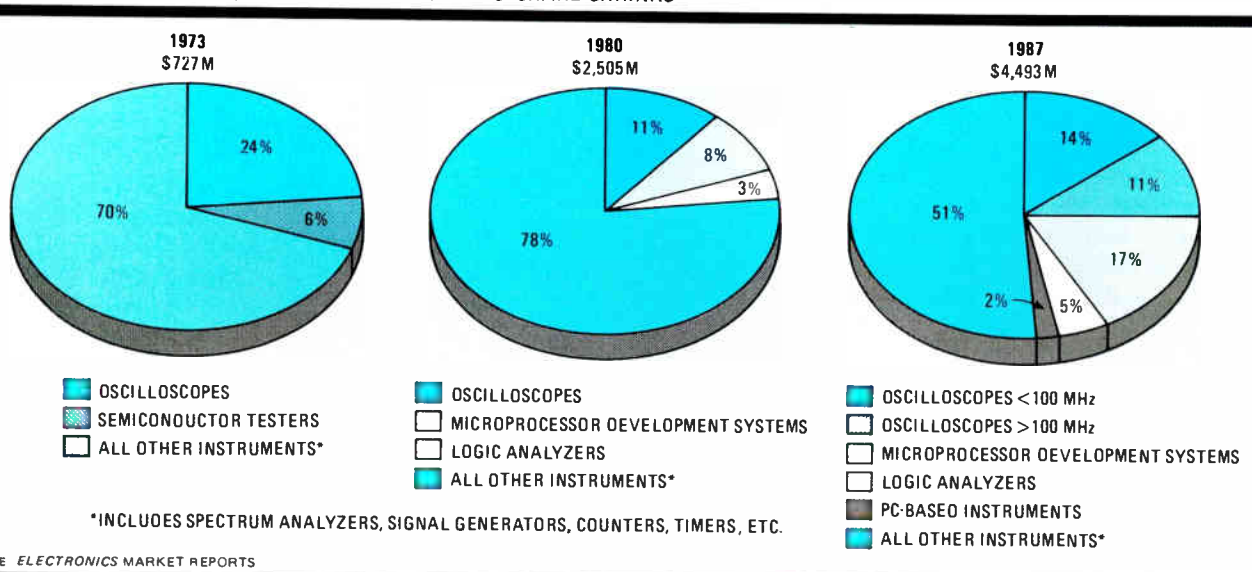
For scopes under 100 MHz, the focus of the competition is price, and low-cost models are moving into the market in force. Much the same kind of price competition is shaking the market for logic analyzers, the other instrument widely used to debug microprocessor systems. There has been little incentive to push analyzer performance above 100 MHz, a speed that suits most microprocessor system development. However, several companies have pushed beyond 100 MHz to meet the requirements of systems being built with today's very fast emitter-coupled-logic chips and the parts emerging from the Pentagon's Very High-Speed Integrated Circuits program.

Lab instruments also are evolving into multifunction units that are in themselves small T&M systems. Another important force for change is the application-specific IC. ASIC designers have been using logic analyzers and other conventional instruments to verify the functionality and performance of prototype chips. But since that's cumbersome and time-consuming, high-end logic analyzers are evolving into larger, smarter digital analysis systems for developing ASICs and multiprocessor systems (see fig. 1). And the need for software commonality from the lab, through factory and field testing, is being addressed by a variety of test systems, as well as by instruments based on the personal computer.

The market for lab instruments continues to grow, but the rate of increase is dropping (see bar graphs, above). Data drawn from *Electronics'* U.S. market reports show how the size and shape of the market has changed since the advent of the microprocessor. In 1973, bench instruments and similar instruments for rack-and-stack test systems had almost the entire T&M equipment market (see pie charts, below). Since then, microprocessor development systems, logic analyzers and personal-computer-based instruments have grown to a projected 24% of the U. S. market in 1987.

The market for instruments, IEEE-488 bus controllers, and other T&M products that more or less meet the original definition of lab instruments, is expected to grow this year about 10%, to $3.4 billion, compared with 11% and $3.1 billion last year [*Electronics*, January 8, 1987, p. 62]. Some of these instruments will still grow

NEW INSTRUMENTS DO WELL, BUT OLDER INSTRUMENTS' SHARE SHRINKS



*INCLUDES SPECTRUM ANALYZERS, SIGNAL GENERATORS, COUNTERS, TIMERS, ETC.

SOURCE *ELECTRONICS* MARKET REPORTS

significantly where their makers incorporate new technology. For example, universal counter-timers that can perform 1-ns measurements will grow 26% this year, and scopes will grow 10%. Among the new breed of lab instruments, PC-based equipment will jump 15% this year—but it is stealing sales from microprocessor development systems, which will drop 17%. Moreover, automated test equipment, which grew out of T&M, is supplanting rack-and-stack gear in component and board testing. ATE will grow 12% in 1987 to $2.2 billion, equal to about half the total lab instrument market.

In fact, the John Fluke Manufacturing Co. predicts that users will rapidly shrink the share of their capital equipment budget spent on traditional T&M equipment and will turn to novel T&M functions, including networked intelligence and T&M functions implanted in fabrication equipment by their manufacturers. The Everett, Wash., company estimates capital spending by all T&M buyers on traditional T&M was $2.5 billion in 1980, will hit $5 billion this year, and then rise to some $7.5 billion in 1990. But Fluke estimates that capital spending for novel T&M was $4.5 billion in 1980, will be some $12 billion this year, and will grow to $20 billion in 1990.

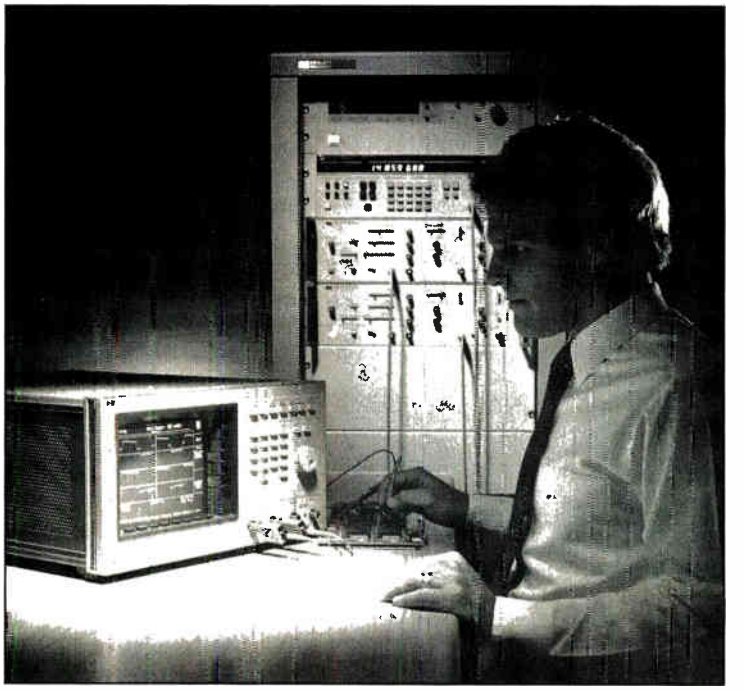
The need for better instruments to develop and test computer equipment has been the driving force behind instrument technology and growth. That this process is still going on is evident in the oscilloscope sector. The scope market has been close to saturation, but a new generation of products is expected to turn it over again.

Sales of scopes with bandwidths to 100 MHz were flat last year but are expected to rise about 5% to $646 million this year, according to the *Electronics* 1987 market report. In contrast, sales of higher-performance scopes grew about 12% last year and are slated for a 17% rise, to $494 million, this year. One reason: up to 100 MHz was the favorite bandwidth in the TTL era, but wider bandwidths are now needed to see transients in systems built with today's faster ICs.

GOING BEYOND 100 MHz

Last fall, Hewlett-Packard Co. reached a single-shot bandwidth of 250 MHz in a new digitizing scope series, the HP54111 (see fig. 2). Other scope makers will be hard put to keep up, because the Palo Alto, Calif., company developed bipolar flash converters that digitize at 1 megasample/s, gallium arsenide track-and-hold circuits, and a 1-GHz surface-acoustic-wave oscillator.

Another lab-instrument powerhouse, Tektronix Inc., of Beaverton, Ore., pushed its proprietary charge-coupled-device technology into the multi-gigasample-a-second range. CCDs can capture faster single-shot transients than conventional digitizers. However, they do introduce a readout time delay where flash converters do not. Tektronix uses CCDs in the digital models in its 11000 family of 1-GHz scopes, which also includes



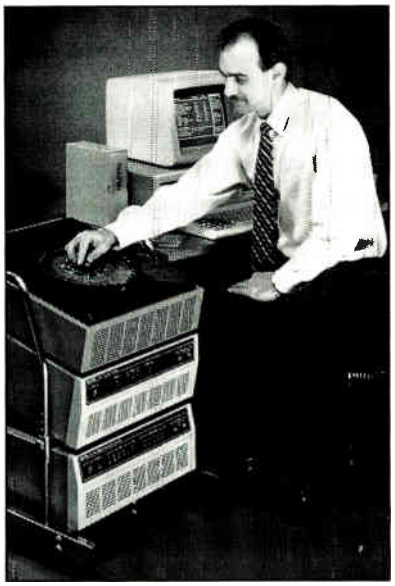
2. QUICK SCOPE. The HP54111D digitizer runs at bandwidths from 250 MHz, single-shot, to 500 MHz with repetitive inputs.

analog units. These scopes expand to 12 channels, with 8 selectively displayed—twice as many as previous scopes. David White, the Tektronix marketing manager for lab instruments, says such instruments have a bright future in ASIC development work because they can be used to tune CAE simulation models by feeding back high-resolution parametric and pin-to-pin skew measurements to computers.

Added functionality is also winning converts to digital storage scopes. Recently, Prime Data, a San Jose, Calif., market researcher, looked at the competition between analog and digital scopes. It found that, while analog scopes still outsell digitizers 2:1, their annual growth rate has dwindled to about 2%, compared with 26% for digitizers. Analog scopes have higher real-time bandwidth at any price/performance level, and they save the cost of flash converters, recording memories, and other high-speed digital circuits. But because digitizers store waveform data, their users can look at waveforms before trigger events, as well as after, and can compare stored waveforms and process the stored data.

Digitizers are capable of bumping other instruments, such as spectrum analyzers, off the test engineer's bench. A new portable unit, the 4094, from Nicolet Instrument Corp., Madison, Wis., uses plug-in modules to run at bandwidths from 100 KHz with 12-bit resolution on up to an equivalent bandwidth (with repetitive-input sampling) of 500 MHz at 8 bits. It does spectrum analysis and math processing at 5 MHz and has disks for data collection and postprocessing analysis software.

Another digitizer that competes with spectrum



3. DOUBLE DUTY. Hilevel Technology's Topaz ASIC verifier uses simulation software downloaded from the design system.

analyzers is the 9400 from LeCroy Corp., Spring Valley, N. Y. This multichannel portable has a built-in FFT processor that displays time- and frequency-domain spectrums simultaneously. FFT resolution is 1 mHz at 50 MHz and, with repetitive inputs, equivalent bandwidth is 125 MHz.

One sign of the times is that HP's new catalog contains no analog oscilloscopes whatsoever. It declared its analog models obsolete last year and replaced them with competitively priced mid-range digitizers.

Both HP and Tektronix have gone to new user interfaces with uncluttered front panels, many automated functions, and menus that pop up on the screen. HP's models can make and display many complex measurements automatically, and HP says its color-coordinated displays save the time users would generally spend sorting out waveforms and measurement data. Tektronix offers an infrared touch screen on the 11000 series: point a finger at a waveform and parameters are displayed automatically; tweak a knob, and that part of the waveform zooms up in size.

But with the bulk of the scope market still under 100 MHz, major producers are also striving to drive prices down on these products. Philips Test & Measuring Instruments Inc., the Mahwah, N. J., subsidiary of Philips International NV, last year challenged Tektronix in the low-priced analog scope market with 50-MHz smart analog scopes designed for mass production. The PM3050 costs $1,245 and the PM3055, with a dual time base, costs $1,345. Philips claims its prices undercut those of Tektronix' 2200 series by as much as $150. And the no-frills scopes made by Kikusui Electronics Corp. of Japan cost still less: the 60-MHz COS5060 lists at $1,185.

That kind of value engineering is also going on in the logic-analyzer market, where growth of only 2% to $207 million is expected this year, compared with 9% and $202 million last year. For example, David Blakemore, vice president at Arium Corp., says his seven-year-old Anaheim, Calif., company has come up fast to rank among the top five in market share because its NL4100 series provides 90% of the functions needed in logic analyzers at prices ranging from $2,995 to $5,850: half to a third the price of analyzers with all the bells and whistles.

Moreover, today's low-cost models often give the same 100-MHz performance on timing-analysis channels as most of the more expensive models do. So to compete in the lab market, the leading companies have made their high-end logic analyzers smarter. Among other new features,

JAPAN LEADS THE WAY IN OPTOELECTRONIC T&M GEAR

Optoelectronic test and measurement equipment is increasingly a Japanese affair, and that's because Japan is pushing optoelectronic technology in many areas. Japan's drive began in earnest in 1979, when the Ministry of International Trade and Industry targeted optoelectronics as a growth industry and spurred a nation-wide research and development effort.

That project and similar support from Nippon Telegraph and Telephone Corp. helped Japanese firms grow rapidly in optoelectronic components, measurement and control systems, and fiber-optics communications. It wound down last year while another, headed by the Japan Key Technology Center in Tokyo, began. The new one, to last 10 years, is focused on optoelectronic integrated circuits for computers and communications equipment.

Today, the optoelectronic instrument market is dominated by optical reflectometers and other instruments used to test fiber-optic transmission lines in communications networks. Those are made in several countries, but Japanese firms lead the world in optical spectrum analyzers, which are general-purpose instruments used for component and system development and testing.

In Japan, as in the west, the market is still dominated by fiber-optic test equipment. And two companies—Ando Electric Co. and Anritsu Corp.—claim 90% of the $65 million Japanese domestic and export markets. Industry sources say that's because NTT limits its purchases for optoelectronic test gear to Anritsu and Ando.

Nevertheless, others are trying to get a piece of the pie. Advantest Corp., a leading Japanese maker of automated test equipment, recently fielded a line of optical time-domain reflectometers and spectrum analyzers, but admits it has made little headway. Instrument maker Iwatsu Ltd. is also an erstwhile player, but is even further behind. Neither have made sales to large users.

Meanwhile, Anritsu and Ando are in a neck-and-neck race for market share. Anritsu is slightly ahead, according to Michiro Ono, Anritsu's Manager, Second Section, Sales Promotion Department, Measuring Instruments Division. At Ando, Kenichiro Yamano, Manager, First Engineering Department, Measuring Instruments Division, contends the split may depend on which company has most recently started shipping a major new piece of equipment.

Both agree that optical time-domain reflectometers are the largest single category. Sporting prices as high as $20,000, these instruments are also the most expensive product. The latest models are compact and portable.

Ono pegs the total market at 50% reflectometers, 10% power meters, 10% light sources, 10% spectrum analyzers, 10% attenuators, and 10% other equipment. Yamano has a somewhat different breakdown: 40% reflectometers, 30% power meters and light sources, 15% spectrum analyzers, and 15% other equipment. *–Charles L. Cohen*

HP and Tektronix now offer system performance analysis, a system-optimization aid. Also, HP's 200-MHz HP1631 series has two digitizing-scope channels to measure electrical parameters and process the data. And some units from Gould Inc.'s Design & Test System Division analyze noise margins and compare tolerances. The Cupertino, Calif., division also has a 500-MHz unit, the K500, with a built-in analog channel that is aimed at supercomputers.

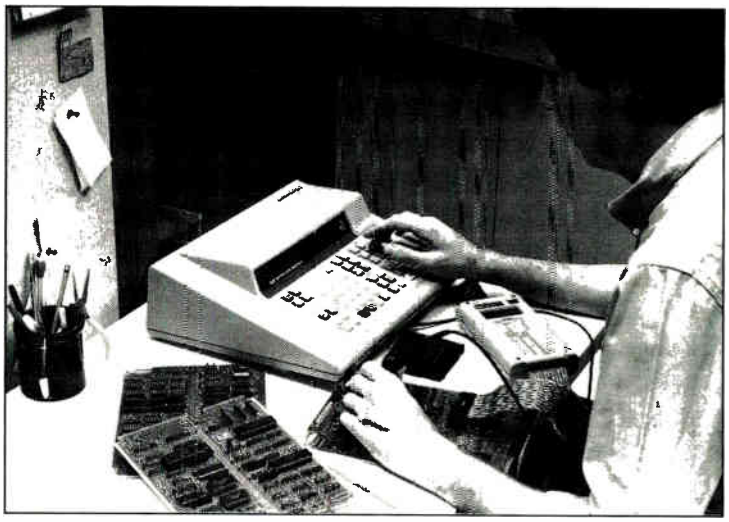
Moreover, lab-quality logic analyzers have reached the performance that advanced semiconductor devices demand. Both Tektronix and Outlook Technology, Campbell, Calif., have 2-GHz machines—high enough for timing analysis of 500-MHz chips. With input sampling similar to that in digitizing oscilloscopes, Outlook reaches 100-ps resolution in its T-100 scope.

One reason sales of conventional instruments have been flattening out is that today's new multifunction instruments, such as universal counters, make it less necessary to build rack-and-stack systems for bench work. In these new boxes, microprocessors coordinate functions that used to take a rack of instruments and an IEEE-488 bus controller. The new breed of arbitrary waveform generator, for one, is smart enough to replace noise generators, function generators, sweep generators, and the like, at frequencies from dc into the rf range.

Stimulus and analysis instruments will be integrated, too. John Battin, president of Wavetek Corp., San Diego, Calif., sees instruments that operate as frequency generators and spectrum analyzers replacing the usual combination of sweep generator and network analyzer. But don't discount conventional spectrum analyzers yet. Sales are forecast to grow another 12%, to $280 million, this year, according to the *Electronics* 1987 U. S. market report.

Lab-instrument makers also are responding to the verification requirements of ASICs and multiprocessor systems. To test these, high-end logic analyzers are evolving into digital analysis systems with large numbers of stimulus and analysis channels. The Atlas system from Dolch Logic Instruments Inc., San Jose, Calif., expands to 192 channels, and as many as 64 channels can analyze at 300 MHz. And Tektronix' newest DAS 9200 runs at rates from 20 MHz on 540 channels to 2 GHz on 160 channels, and it can have as many as 1,008 stimulus channels.

Recently, too, several new small ATE systems dedicated to ASIC verification have borrowed technology from logic analyzers. Although ATE-like ASIC verifiers are too big to fit on a bench, they are designed to be used by the same engineers who develop ASICs and to test prototype chips with the same test patterns and vectors as the engineers' CAE systems. For instance, Hilevel Technology Inc., Irvine, Calif., builds an ASIC verifier around a logic analyzer and a high-speed bit-slice bipolar processor (see fig. 3). The Topaz



4. TINY BOARD TESTER. Fluke's 9010 compact board tester is going into labs as a debugging tool's compact tester.

series has 288 pins, and its test channels multiplex from 25 to 100 MHz. A new file-conversion package allows test software to be shared by CAE, ASIC verifier, and large IC testers.

In another development, sparked by the need for software commonality, board testers once seen only on the factory floor are going into labs and out into field-service depots. For example, Fluke recently introduced the 9010, a programmable tester that's smaller than most logic analyzers (see fig. 4). The 9010 operates with in-circuit emulators or miniature bed-of-nails test heads and was designed for troubleshooting boards rejected by large board testers, says Hugo Draye, manager of Fluke's manufacturing and R&D marketing group. But, he adds, it is also being used in labs, where board designers can program it to run debugging tests, then pass the programs on to troubleshooting technicians in the factory and in the field.

A key development is the evolution of lab instruments into multifunction units that are themselves small T&M systems capable of replacing an entire rack

Another fast-developing trend that's changing the face of the lab-instrument world is the personal computer. The IBM Personal Computer and the flood of new instruments that interface with it let users take advantage of both the extra processing power of the PC family and all the engineering and test software developed for it. Recognizing a fait accompli, the Institute of Electronics and Electrical Engineers has set up committees to standardize the PC bus, the PC-AT bus, and BIOS, the basic input/output system for computers using Intel Corp.'s 80286 16-bit and 80386 32-bit microprocessors. □

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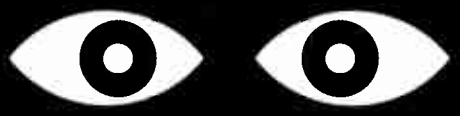

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NEW PRODUCTS

$29,000 IMAGE PROCESSOR CUTS HIGH-RESOLUTION GRAPHICS COST

IMAGING TECHNOLOGY'S SERIES 200 RUNS ON MICROVAX, OTHER DEC MODELS

Imaging Technology Inc.'s new multiboard Series 200 system substantially lowers the cost of high-performance imaging systems, cutting the price to roughly half that of competitive systems.

The Series 200 costs less than $29,000 and can be teamed with Digital Equipment Corp.'s MicroVax II and other computers compatible with DEC's Q bus. A MicroVax II/Series 200 system costs about $50,000. Previously, the least expensive comparable high-end imaging systems cost up to $100,000, says Imaging Technology.

The Series 200 executes logical operations and linear and nonlinear point transformations in real time at rates corresponding to 0.033 s for a 512-by-512-pixel RS-170 frame. Convolutions for a 3-by-3 kernel applied to a 512-by-512 image are executed in 0.33 s.

Interpolated zooming and rotation on 512-by-512 images take 1.05 and 0.44 s, respectively. Imaging Technology says the system executes fast Fourier transformations in 11 s.

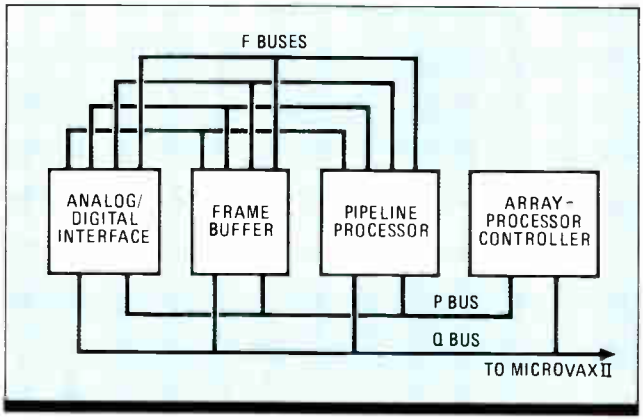
The basic Series 200 system includes four printed-circuit boards that interface the host computer through a repeater compatible with the Q bus. The modules are an analog/digital interface; a frame buffer; a pipeline processor with maximum speed of 50 million operations/s; and a high-speed array processor.

The Series 200 owes its performance to its architecture and custom gate arrays. The most important is a programmable video-bus network that can be dynamically reconfigured for optimal execution of a given operation.

BUSES. The bus network includes four bidirectional, 10-Hz frame buses known as F buses, which carry scanned image data between the analog-digital interface, the frame buffer, and the pipeline processor. Also in the bus network is an 8-MHz processor bus (P bus), which is used by the system's array processor to access other modules.

The F buses are used for pipelined operations on live video or stored images. Software control allows these buses to form any combination of interconnections between the modules, while custom gate arrays implement the reconfigurable data paths.

The system's frame buffer also helps boost performance. Built around custom gate arrays, it allows access to the buffer through two ports.



PIPELINED. Frame buses (F buses) carry image data between processing modules; the P bus connects them to the array processor.

Bob Birenbaum, director of marketing, emphasizes that both of the ports on the Series 200 frame buffer can operate at 10 MHz. "So it essentially has two scan ports," says Birenbaum. Thus the second port can perform three functions. It can communicate with the system's array processor at 8 MHz; it can be assigned as a second 10-MHz scan port; or it can communicate with the host processor at much slower rates.

Another important contributor to system performance is the symmetrical architecture of the system's array processor, the HSP-200. This closely coupled single chip can handle transfers to and from the frame buffer while simultaneously performing algorithmic computations. In addition, the HSP-200 can control operation of other system modules in real time over the P bus. DEC's MicroVMS operating system alone cannot do this, because it is not a real-time operating system.

Included with all Series 200 systems is a library of image-processing routines and an interactive development environment. The ITEX200 library is written in C and microcode. The system's interpreter calls ITEX routines from an interactive terminal and supports special functions such as If-tests and Do-loops. All software is compatible with the MicroVMS operating system. Additional tools allow users to develop microcoded algorithms for the system.

The entry-level price for the Series 200 is $28,895, including the Q bus repeater for communication with the DEC system, the chassis with power supply, the ITEX 200 subroutine library, and software. Additional frame buffers each cost $4,995. All are available 60 to 90 days after order. *–Craig Rose*

[Circle 340]

32-BIT VMEBUS MODULE FITS INTO TIGHT SPOTS

The 32-bit VMEbus microcomputer module from Pep Modular Computers GmbH features a small format especially suited for designing compact industrial systems.

Built around Motorola Inc.'s 68020 microprocessor, the single-height, Eurocard-format VMPM68KC module is half the size of the double-height format that competing 32-bit VMEbus modules use, according to Norbert Hauser, the marketing director for the West German company.

The 100-by-160-mm module allows equipment makers to build compact and rugged computing systems for industrial environments where tight spaces, shock, and vibration are common, says

Hauser. The VMPM68KC is designed for applications where lots of computing power with fast 32-bit operations is needed, such as factory and robot control and process automation. Hauser says the module can handle about 2.5 million instructions/s.

Pep, a leading producer of VMEbus and intelligent input/output channel modules in low-cost Eurocard format, has based its latest system on a processor and a memory board, which together form a tight package. It marries the high performance of the 32-bit 68020 processor and a 68881 floating-point coprocessor to 1 megabyte of static random-access memory and up to 512-K of read-only memory.

For fast throughput, the 68020 and 68881 are closely coupled to the local RAM and ROM via a high-speed 32-bit address and data bus. The module is supported by a debugging monitor in firmware and a real-time multitasking, multiuser operating system, OS-9/68020.

The VMPM68KC comes in two versions: one with a 12.5-MHz data-transfer speed and the other with a 16.7-MHz speed. The SRAM offers zero-wait states, and the dual-port RAM architecture facilitates high throughput between memory and the CPU, as well as between memory and the VMEbus.

Two serial I/O ports, which can be configured individually with piggybacks, provide maximum flexibility for communications, Hauser says. For example, the memory board can be upgraded with memory piggybacks. Four 32-pin sockets, which can also accept 28-pin integrated circuits, allow for up to 512-K bytes of 32-bit-wide ROM, which makes the module suitable for industrial-control applications with ROM operating systems such as the OS-9.

The module's functions are implemented almost entirely with CMOS circuits. This helps keep power consumption to a low level, about 12 W.

The VMPM68KC costs $2,600 each for the 12.5-MHz version in 100-unit lots, $3,500 for the 16.7-MHz version, also in 100-unit lots. Both versions will be available in March.

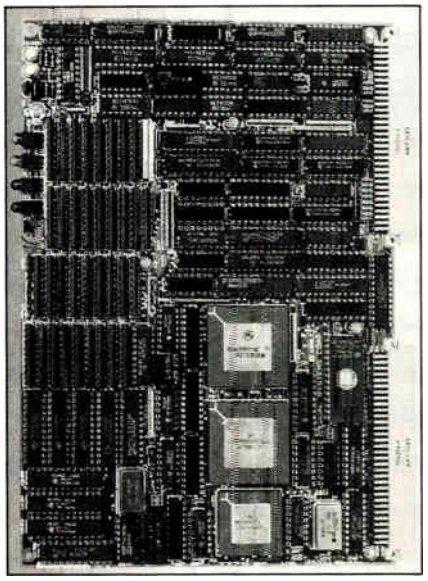
–John Gosch

[Circle 341]

BOARD COMPUTER RUNS AT 25 MHz

Dual Systems Corp.'s single-board computer runs at 25 MHz and uses a 2-K byte data-cache memory to ensure no-wait-state operation for 70% to 90% of its bus cycles.

Based on Motorola Corp.'s 68020 processor, the VMPU-4M also features 4 megabytes of on-board memory. Its cache memory can be expanded to 8-K bytes.



An on-board Motorola MC68851 memory-management unit controls access to the dual-ported memory, which has an access time of 115 ns and a cycle time of 200 ns.

The board can be used with VMEbus-compatible computers that run AT&T Co.'s Unix operating system. By adding an input/output processor board and storage controller, it can be configured to support multiuser applications. The VMPU-4M costs $12,000 in single-unit purchases and is available now.

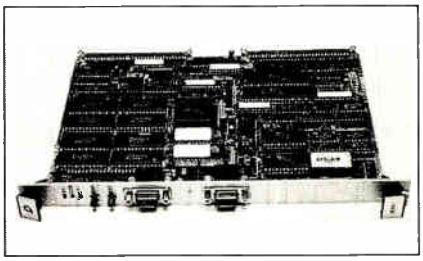
Dual Systems Corp., 2530 San Pablo Ave., Berkeley, Calif. 94702.
Phone (415) 549-3854 [Circle 345]

ALL-CMOS CPU BOARD RUNS ON 30 mA

An all-CMOS central-processing-unit board from Dynatem Inc. consumes only 300 mA in normal operation and runs at 12.5 MHz. The DCPU1 has 128 K bytes of programmable read-only memory and can be built with either of two Motorola Corp. processors, the 68000 or 68010.

VMEbus compatible, it includes an on-board rechargeable battery to maintain clock and memory. Other features include no-wait memory, extensive input/output, two serial ports, three 16-bit timers, 40 programmable parallel lines, and a real-time clock/calendar.

Programming can be prepared on IBM Corp. Personal Computers XT and AT and compatibles and downloaded to



the module. The 64-K-byte random-access memory board costs $975, and the 512-K-byte RAM version costs $1,675. Both boards are available now.

Dynatem Inc., 19 Thomas, Irvine, Calif. 92718. Phone (714) 855-3235 [Circle 346]

MULTIUSER SYSTEM PUTS XENIX ON PC/AT

A plug-in module from Corollary Inc. runs on Microsoft Corp.'s Xenix operating system and provides enough processing power to support 8 to 32 additional users on a host IBM Corp. Personal Computer AT system. The company's ATtain 286 subsystem has an Intel Corp. 80286 processor, 1 megabyte of dual-port RAM, and two serial ports. Up to four ATtain subsystems can be piggybacked on a single PC/AT or compatible. The processor is aimed at original-equipment manufacturers and value-added retailers. Available in March, the ATtain 286 costs $1,950 in single-unit purchases.

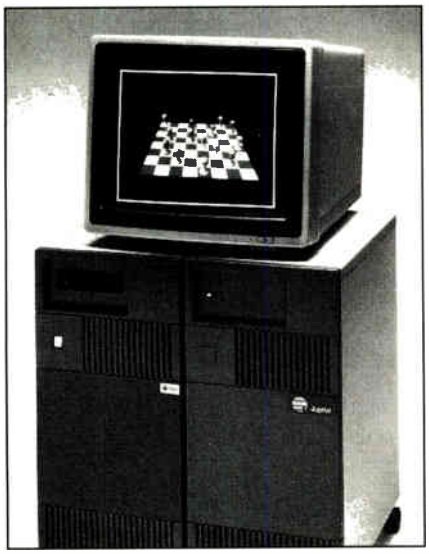
Corollary Inc., 18011 E. Skypark Circle, Irvine, Calif. 92714.
Phone (714) 250-4040 [Circle 347]

GRAPHICS SYSTEM HAS 5 COLOR MODES

A high-performance, high-resolution color graphics display system from Jupiter Systems Inc. features extensive imaging capabilities, programmable video formats, and up to five independent color display modes.

Designed to be configured with Sun Microsystems Corp. work stations, Jupiter's Satellite line is based on a high-speed bit-slice processor that has been custom-designed for graphics tasks. The processor can execute program loops at more than 6 million iterations/s.

The Satellite's imaging capabilities include panning with single-pixel resolution, zoom factors of 1 to 16, magnification, and pixel block-transfer operations. Each of the system's four bitplanes of memory have separate pan and zoom controls so that images can be zoomed to different levels and panned relative to each other.



Besides the standard 1,280-by-1,024 pixel format, the system can accommodate any display format up to a maximum pixel rate of 110 MHz. American, European, and the new High-Definition Television formats are supported. Users can also customize their own formats.

Additional flexibility is provided by the Satellite's five display modes. The system provides both 4-bit and 8-bit color-look-up table modes as well as 12-bit and 24-bit red-green-blue modes. Another display mode known as HUES16 provided 128 shades of 16 basic hues. Its color pallete supports 16 million colors.

The company offers 16-in. and 19-in. high-resolution monitors with the system. They have scan rates of 65 KHz and a 110-MHz bandwidth.

The Satellite can be used with any Sun work station. Available now, prices range from $15,000 to $30,000 depending on configuration.

Jupiter Systems, Inc., 1100 Marina Village Pkwy, Alameda, Calif. 94501.
Phone (415) 523-9000 [Circle 348]

CASCADED GRAPHICS CHIPS DRAW 3.3 MILLION PIXELS/S

AMD'S CONTROLLER INTEGRATES TEXT, GRAPHICS; 64-CHIP CASCADE HANDLES 256 BIT-MAPPED MEMORY PLANES

Aimed at high-performance graphics applications, a new controller chip from Advanced Micro Devices Inc. handles up to 256 bit-mapped memory planes when cascaded with other units, and it draws vectors at the rate of 3.3 million pixels/ns.

Using 4-K-by-4-K memory planes, the Am95C60 also features the integration of text and graphics in the same bit map with a bit-block-transfer algorithm.

AMD expects the chip to be used in engineering work stations, computer-aided design and manufacturing equipment, graphic arts, and desktop publishing. It is one more example of the move by semiconductor companies to incorporate more graphics control at the chip level to accommodate ever more sophisticated graphics applications.

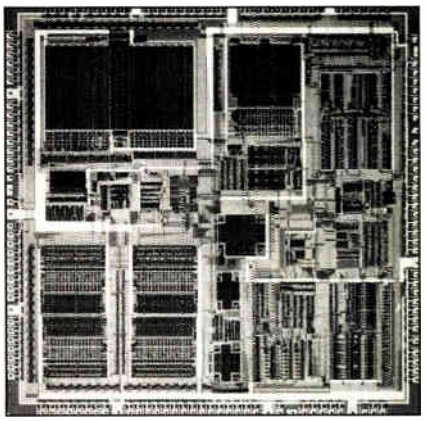
256 PLANES. AMD calls the device a quad pixel dataflow manager, because each chip manages and updates four bit-mapped memory planes from a single control channel. As many as 64 chips can be cascaded to create 256 memory planes without performance degradation, says the company.

The 95C60 supports screen displays up to 2-K by 2-K pixels and can update a 1-K-by-1-K-pixel screen—the most common high-resolution screen on the market—in 0.2 s at its 20-MHz clock speed.

AMD speeded bit-mapping in the 95C60 by using both graphic and raster primitives to update each bit map. Graphics are drawn with line and arc vectors at a speed of 3.3 million pixels/s. Polygon-fill operations are accomplished at a rate of 50 ns/pixel.

The 95C60 efficiently mixes text and graphics. A bit-block-transfer primitive replaces the usual alphanumeric control for characters, which means that text is treated as a special form of graphics. The command, called BITBLT, can transfer blocks of data at up to 20 Mb/s. A single 13-bit character-address instruction can access up to 8,192 characters—enough to support any character set, including oriental Kanji characters. Fonts are stored in the bit map.

The chip's performance results in part from extensive parallelism in its architecture. Fetch, execute, and display cycles overlap. All chip cycles are decoupled from system bus cycles. The chip can fetch its own instructions via the display memory bus, off-loading this task from the central processor. Arbitration between refresh cycles, update cycles, and external-memory-refresh cycles is performed on-chip.



CONCURRENCY. AMD's graphics controller chip overlaps cycles for higher performance.

The instruction set supports windowing in both hardware and, via BITBLT, software. Scroll, pan, and zoom may be performed on the screen itself and on any window on the screen. Anti-aliasing is used to eliminate jagged "steps" in diagonal lines.

A 16-MHz version of the chip costs $250 in lots of 100. It has been offered in sample lots since January and will be available in quantity next month. The 20-MHz version of the chip will also be available next month for $287.57 each in lots of 100.

[Circle 360]

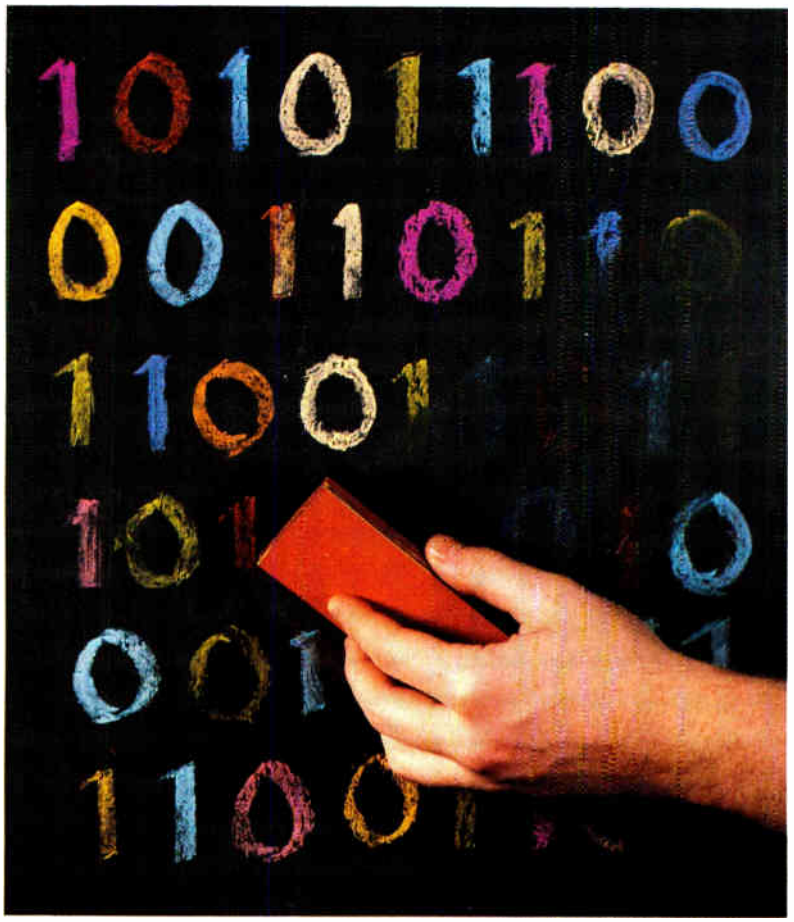
CHIP CUTS COST AND SPACE NEEDS

Adaptec's AIC-610 peripheral controller chip replaces 10 logic components formerly implemented in discrete form on most controllers, including a programmable storage buffer, a dual-port buffer controller, and buffer addressing logic.

By integrating more components on-chip, Adaptec achieved a 60% to 70% space reduction over controllers now on the market, says the company. Consequently, logic-hardware costs will be reduced by 40% and power requirements by 30%.

Offering a maximum 15-MHz data-transfer speed and a maximum bus transfer rate of 1.5 megabytes/s, the chip is compatible with any standard interface used by Winchester-disk, floppy-disk, and tape drives.

ERASES IN A FLASH.



Combining the fast programming techniques of EPROMs with the erasure mechanism of EEPROMs results in a high-density device with the best of each

How Seeq is pushing EEPROMs to 1-Mb densities.

"The 1-Mb electrically erasable read-only memory has come a step closer, now that Seeq Technology Inc. is going into production with its version of a flash EEPROM. This device, so named because the contents of all the array's memory cells are erased simultaneously by a single field emission of electrons, combines the advantages of ultraviolet-erasable EPROMs and floating-gate EEPROMs.

It unites the high density, small cell size, low cost, and hot-electron write capability of an EPROM and the easy erasability, on-board reprogrammability, high endurance, and cold-electron tunneling erasure of floating-gate EEPROMs. In doing so, Seeq's single transistor 16-K-by-8-bit memory paves the way for high-density EEPROMs..."

Excerpted from an exclusive article in the August 21, 1986 issue.

Electronics

THE LEADER IN NEW TECHNOLOGY COVERAGE

The company's 10-MHz version of the AIC-610 costs $23 each in 1,000-unit lots. A 15-MHz version, the AIC-610-15, costs $34.50 in 1,000-unit orders. Both will be available in June.
Adaptec Inc., 580 Cottonwood Dr., Milpitas, Calif. 95035.
Phone (408) 432-8600 [Circle 365]

GaAs FANOUT BUFFER CLOCKS AT 1.8 GHz

A gallium arsenide dual-clock-driver/fanout buffer from Harris Microwave Semiconductor Corp. features a 1.8-GHz clock speed and a typical propagation delay of 800 ps.

The HMD-11188-2 is fully compatible with emitter-coupled logic and operates at processing speeds up to four times faster than those of ECL devices, the company claims.

It has a four-output fanout capability into 50-Ω terminated transmission lines, with an output skew mismatch of less than 50 ps.

The chip's dual-driver design allows three operational modes as a clock fanout buffer: with matching inputs and outputs; with inverted outputs; and with the outputs at a high state when the data-enable is fixed low.

The device is fully compatible with other Harris GaAs integrated circuits and is available in a 16-pin hermetic flat pack. It costs $155 in 100-unit quantities. Delivery is within six weeks of order.
Harris Corp., Microwave Semiconductor Div., 1530 McCarthy Blvd., Milpitas, Calif. 95035.
Phone (408) 262-2222 [Circle 356]

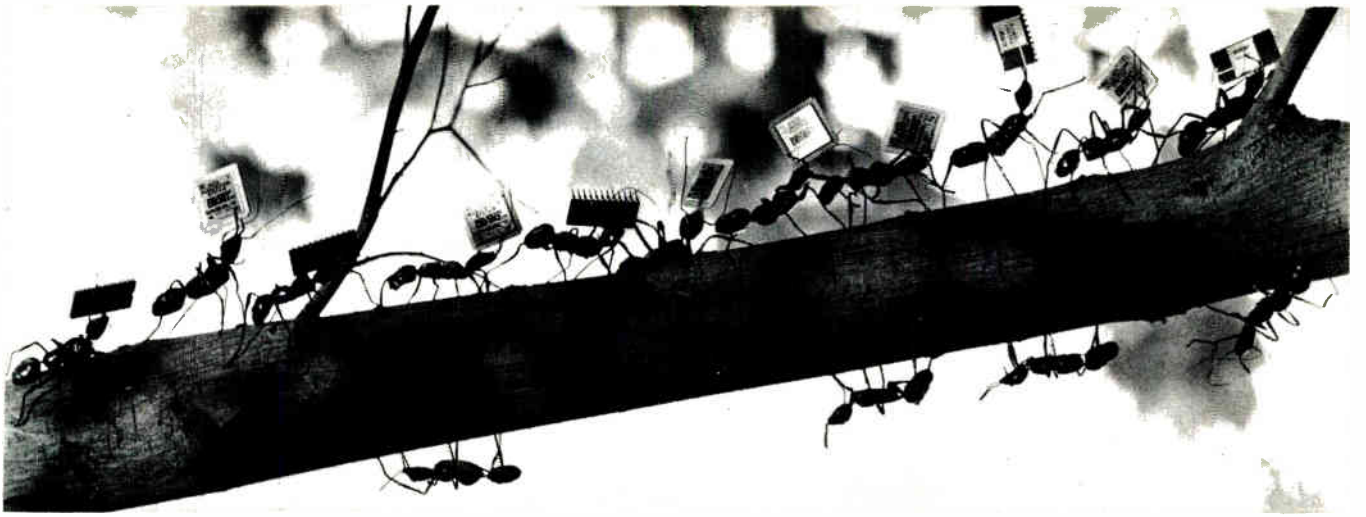
CHIP COMBINES MATH FUNCTIONS

An arithmetic logic unit from Analog Devices Inc. combines an array multiplier, dual 40-bit accumulators, shift-register logic, and block floating-point circuitry on a single chip to achieve a device that performs complex integer operations without external logic.

The ADSP-1101 offers throughputs comparable to multiplier/accumulators, says the company. It can compute a 1,024-point complex fast Fourier transformation in 2.2 ms, a speed equal to processors costing hundreds of dollars.

The 1.5-μm CMOS device offers cycle times of 70 ns and maximum power dissipation of 450 mW. It has two 16-bit input ports and a 20-bit output port. As many as six 16-bit words can be transferred through the chip's three data ports in a single cycle.

The devices cost $88 each and will be available in the third quarter of 1987.
Analog Devices Inc., 70 Shawmut Rd., Canton, Mass. 02021.
Phone (617) 461-3672 [Circle 367]



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NEPCON PREVIEW

AUTOMATED LEAD TINNING REDUCES REJECTION RATES

CORFIN TECHNOLOGY'S SYSTEM USES VACUUM TRANSPORT AND HOT-AIR CUTTER TO PUT ON EVEN SOLDER COAT

Corfin Technology Inc.'s automated tinning system for surface-mounted components cuts product-rejection rates and labor costs when compared with the batch-soldering process now in use, the company says.

To be introduced at Nepcon West, the VTS-350 offers innovative solutions to a number of problems that have plagued surface-mount technology. Until now, pretinning the leads of surface-mountable integrated-circuit packages has required a labor-intensive batch-soldering process. Devices are loaded onto pallets, and then these devices are transported through flux, solder, and cleaning stages.

FEWER PROBLEMS. Batch pretinning results in an uneven application of solder, however, and has been difficult to automate. The process also requires extensive downtime for machine service.

To control solder thickness, Corfin developed a method based on a vacuum-based device-transport system and a solder-profiling device, which together consistently maintain solder planarity to within ±0.5 mil.

The combination cuts rejection rates from 30% to practically zero, says the company. Moreover, the automated system significantly reduces labor costs.

The transport system grips each IC with a vacuum suction nozzle. The ICs are dipped in the solder rather than transported through it.

The profiler is located immediately after the soldering unit. It controls thickness by precisely directing a stream of hot air across the leads, thereby cutting off excess solder.

Other features of the VTS-350 are a flat-wave fluxing unit and a flat-wave soldering unit. The fluxing unit, which can be equipped with a flux-density controller, is fully adjustable and is designed for easy removal for cleaning and filling.

The flat-wave soldering unit provides a highly stable wave to ensure an even, high-quality coating of solder. Strategically located heating elements in this unit ensure an even, controlled heating of the solder.

To further enhance product integrity, the surface-mountable components are successively cleaned, dried, fluxed, preheated, soldered, cleaned a second time, and then they are dried before being unloaded.

The VTS-350 can tin several thousand components an hour. Prices vary from $75,000 to 150,000, depending on the de-

NEPCON WEST '87

Nepcon West '87 once again promises a glimpse of the leading edge in packaging technology. Surface mounting has provided a big impetus for innovation in device-handling technology, and factory automation is proving to be a growing segment of the show, but the 980 exhibitors have also fielded plenty of traditional equipment for the expected 38,000 attendees to inspect.

gree of sophistication and automation of loading and unloading. Estimated delivery is 16 weeks.

This machine can tin typical surface-mount IC packages such as the SOIC, leaded chip carriers, and the quad flat pack. Corfin is also developing a machine for tinning tiny chip resistors, capacitors, and SOT-23 packages, which are also heavily used in surface-mounted boards. *–Jerry Lyman*

[Circle 420]

SYSTEM SOLDERS 360 PC BOARDS/HR

A hot-air solder system for printed circuit boards uses a new placement technique and separate pre- and post-treatment lines to achieve a throughput of up to 360 pc boards/hr.

The fixing system uses two pins to quickly place the boards in position and level them before they enter the solder pot. Other features of the Quicksilver include a heavy-duty solder pump, a self-cleaning overflow system, and precisely controlled heat exchangers.

The solder pump circulates solder around the sump to ensure even solder temperature and a dross-free dripping zone. Available now with a delivery time of six weeks, Quicksilver's price will be released at Nepcon.

Circuit Engineering Co. Ltd., Kiln Lane, Buriton, Petersfield, Hampshire GU31 5SJ, UK.

Phone 44-730-66026 [Circle 427]

FIBER LINK STOPS RF INTERFERENCE

By using nonconductive fiber-optic cable and a metal housing, Thomas Betts Corp. eliminates electromagnetic interference in its fiber-optic RS-232-C Data Channel interface for computer-integrated manufacturing applications.

The devices are available in plastic- and glass-fiber versions. Both create a barrier against ground-loop hazards, voltage spikes, switching transients, and line tapping.

The plastic-fiber device handles up to 20-K bytes/s of non-return-to-zero duplex asynchronous data at distances up to 130 m. The glass-fiber version can carry 20-K bytes/s as far as 4 km. The systems are available in 25-pin-connector configurations for DTE-type and DCE-type RS-232-C equipment. Available now, they cost $132 in unit purchases and $115 each in 50-unit purchases.

Thomas Betts Corp., 920 Route 202, Raritan, N. J. 08869.

Phone (201) 469-4000 [Circle 426]

POLYMERS YIELD STRONG IC PACKAGES

The Xydar RC-210 series of reinforced liquid-crystal polymers from Dartco Technology Center features high mechanical strength for a wide range of injection-molded electronics component packages.

The resin has a heat-deflection temperature of 650° F (343° C), a flexural strength greater than 10,000 lb/in.^{2} at 510° F (266° C), and a flexural modulus of 1.35 million lb/in.^{2} at 575° F. A 0.125-in. layer of Xydar RC-210 will resist a 2,000° F torch for 15 minutes without burn-through. It is resistant to high-temperature deformation, and its mechanical strength increases at subzero temperatures.

The product can be injection-molded on conventional machinery at up to 50% faster cycles than polyphenylene sulfide and up to 75% faster than polyetherimide. It can be used to fill very thin wall sections at low injection pressures.

The resin costs $7.35 to $9.75 per pound for orders of 10,000 lbs. Delivery takes five to seven days for off-the-shelf RC-210 series products.

Dartco Technology Center, P.O. Box 5867, Augusta, Ga. 30906

Phone (404) 790-3100 [Circle 425]

Electronics 1987 Recruitment Editorial Calendar

Issue Date	Feature	Closing Date
January 8	U.S. Market Forecast	December 22
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March 5	Online Transaction Systems ISSCC Wrap-Up	February 16
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June 25	Industrial Electronics Design Automation Conference	June 8
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November 26	Military Electronics Parallel Processing ISDN IEDM Preview	November 9
December 17	Year-End Double Issue Executive Outlook ISSCC Preview GaAs Technology	November 30

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EXPERTS IN ART.

By making it easier to develop programs, the new C-language version of the ART development tool could accelerate the move of expert systems into the mainstream.

A new strategy speeds up expert systems into the mainstream.

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Excerpted from an exclusive article in the August 7, 1986 issue.

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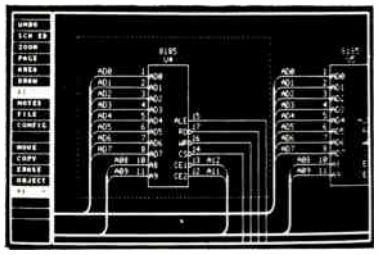

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San Jose, Calif. 95131
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(408) 559-7778

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Advertising Sales Staff

Atlanta, Ga. 30319: Joseph Milroy
4170 Ashford-Dunwoody Road N.E.
[404] 252-0626
Boston, Mass. 02116:
M. E. "Casey" McKibben, Jr.
575 Boylston St.
[617] 262-1160
633-0155 Mobil Phone
Chicago, Ill. 60611: William J. Walker
[312] 751-3738
645 North Michigan Avenue
Cleveland, Ohio 44113:
[216] 496-3800
Costa Mesa, Calif. 92626: Fran Cowen
3001 Red Hill Ave. Bldg. #1 Suite 222
[714] 557-6292

Dallas, Texas 75240: Harry B. Doyle, Jr.
5151 Belt Line Road, Suite 907
[214] 458-2400
Englewood, Co. 80112: Harry B. Doyle, Jr.
7400 South Alton Court Suite 111
[303] 740-4633
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[713] 462-0757
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3333 Wilshire Blvd.
[213] 480-5210
New York, N.Y. 10020
Matthew T. Reseska [212] 512-3617
John Gallie [212] 512-4420
1221 Avenue of the Americas
Stamford, Ct. 06902
Albert J. Liedel
777 Long Ridge Road. Bldg. A
[203] 968-7115
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Larry Goldstein, Jeffrey C. Hoopes, Paul Mazzacano
3rd Floor
951 Mariner's Island Blvd.
[415] 349-4100
Philadelphia, Pa. 19102: Joseph Milroy
Three Parkway, [215] 496-3800
Pittsburgh, Pa. 15222: Joseph Milroy
Suite 215, 6 Gateway Center, [215] 496-3800
Southfield, Michigan 48075:
4000 Town Center, Suite 770, Tower 2
[313] 352-9760
San Francisco, Calif. 94111:
Larry Goldstein, Jeffrey C. Hoopes, Paul Mazzacano
425 Battery Street
[415] 362-4600

Frankfurt/Main: Fritz Krusebecker, Dieter Rothenbach
19 Liebigstrasse, Germany
Tel: 72-01-81
Milan: Manuela Capuano
1 via Baracchini, Italy
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Paris: Jean - Christian Acis, Alain Faure
128 Faubourg Saint Honore, 75008 Paris, France
Tel: [1] 42-89-0381
Scandinavia: Andrew Karnig
Finnbodavagen
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Sweden
Tel. 46-8-440005
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Tokyo: Hirokazu Morita
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Kasumigaseki Building 3-2-5, chome,
Kasumigaseki, Chiyoda-Ku, Tokyo, 100 Japan
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United Kingdom: Art Scheffer
34 Dover Street, London W1
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Business Department

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[212] 512-2627
Daniel McLaughlin
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DISTRIBUTION WEEK

COMPETITION, SLACK MARKETS STRETCH DISTRIBUTORS' LONG WAIT FOR PAYMENT

Unless business conditions pick up unexpectedly in 1987, electronics distributors will have to keep living with stretched-out accounts receivables.

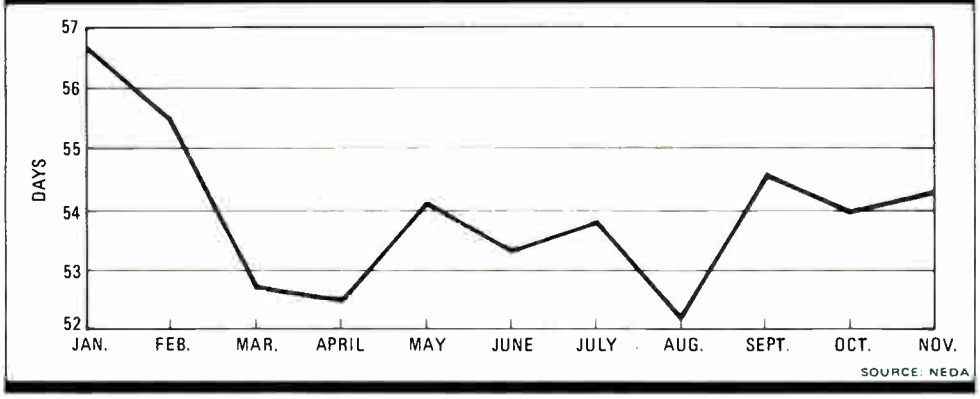
Figures published by the National Electronic Distributors Association in Chicago show that the number of days in which payments were outstanding held steady at around 54 during the last few months of 1986. "It's kind of stabilized at an unhealthy high level," says Toby Mack, NEDA's executive vice president. "Forty-five to 50 days would really be more healthy."

The numbers reflect the buyer's market conditions that plagued the business in 1986, a state of affairs that forced distributors to compete on the basis of credit terms as well as on price.

Mack sees only gradually improving conditions for distributors this year. "To get receivables down, it's going to take a slightly less competitive market," he says. And at best, NEDA expects growth at 3% to 4% in the first quarter and at 12% for the year.

In the meantime, "It puts the distributor in the position of being a banker," Mack says. Of course, he adds, "that is one of the functions of distributors. There are a lot of small original-equipment manufacturers out there who wouldn't be able to get off the ground unless their distributors were issuing them credit." *–Wesley R. Iversen*

DISTRIBUTORS' ACCOUNTS-RECEIVABLE LAG TIME: JANUARY TO NOVEMBER 1986



GRAY MARKETEERS FEELING HEAT

Although U. S. distributors of Japanese parts are still losing business to gray-market operations in countries outside Japan and the U. S., there are signs that the gray market is beginning to feel the effects of the semiconductor trade agreement.

"Some of our suppliers have indicated that the gray-market dealers are selling chips back into the resale market at approximately their own cost," says Bernard T. Marren, vice president of Western Micro Technology Inc., Cupertino, Calif.

What has the gray marketeers jittery is not the law itself, but the impact of memory chips from Texas Instruments Inc. and Nippon Electric Corp. that are manufactured in the U. S., and, therefore, are not covered by the semiconductor pricing regulations. These chips could undercut the gray-market prices.

Chip distributors in the U. S. are still not getting their fair share of the business, however, because of buyer uncertainty, says Marren. "People don't know what the price will be, so they tend not to buy, or to buy on the spot market."

GESPAC ADDS SWISS BOARDS

Gespac Inc., a Mesa, Ariz., manufacturer of single-board computers, will distribute Swiss board-maker MPL AG's G-64 product line in the U. S. and Canada. Under the agreement, Gespac will perform functions such as promotion, stocking, technical support, and maintenance for MPL boards. MPL, of Zurich, has been in the G-64 bus business for six years and designs boards that complement Gespac's products.

SCHWEBER TO SELL MIZAR BOARDS

Mizar Inc., a St. Paul, Minn., maker of board-level products, has signed a nationwide distribution contract with Schweber Electronics Inc., Westbury, N. Y. Mizar says it expects to forge a similar pact with Schweber's Long Island neighbor and competitor, Arrow Electronics Inc. of Melville, N. Y., in coming weeks.

The distributors will be the first for Mizar, which makes VME- and STD-bus boards and systems aimed at engineering applications. But the three companies are not strangers. When Mizar purchased the Hamilton Standard Digital Systems division of Mostek Corp. last summer, it inherited that company's contracts with the two Long Island distributors.

Schweber is a subsidiary of Lex Electronics Inc., Stamford, Conn., the nation's second-largest distributor of electronic equipment. Last year, Lex tallied $520 million in sales.

CUBIC INKS UK RADIO CONTRACT

Cubic Communications, San Diego, Calif., has signed an exclusive distribution agreement with Codan UK Ltd. to provide paramilitary high-frequency communications gear to several countries in Africa and the Middle East. Included in the three-year pact are rights to Cubic's line of receivers, transceivers, and related accessories.

Codan, a communications marketing company, will perform marketing, installation, service, and warranty functions from its headquarters in Hampshire, England.

U. S. DATA SIGNED TO BOOST UNIX USE

To accelerate use of AT&T Co.'s Unix operating systems in the office, Uniplex Integration Systems Inc. has awarded United States Data Corp. exclusive rights to distribute Uniplex-II Plus software in the Western Hemisphere.

Both Dallas-area companies see the agreement as a means of increasing support to end users. Uniplex-II Plus integrates user interface, word processing, spreadsheet, and data-base capabilities. Prices start at $1,000 for a single-user work station.

Uniplex Integration Systems says it will continue to market the software directly to computer makers and to value-added resellers.

ELECTRONICS WEEK

ENMASSE CUTS STAFF TO SIX

On the verge of announcing its newest on-line transaction processing system, Enmasse Computer has instead halted all sales and cut its staff to six employees. The Acton, Mass., company has not filed for Chapter 11, but rather hopes to sell off its technology and assets. Enmasse sold about 20 of its multiprocessor systems since its founding in 1983, and was planning to announce a new Unix-based multiprocessor system at Uniforum, a Unix show held last month in Washington, D.C.

LOANS TO EASE FLEXIBLE'S CRUNCH

Flexible Computer Corp. has received $1.3 million of a $3.9 million loan package designed to end a severe cash shortage it reported last year. The Dallas firm had reduced reported 1985 and 1986 revenues [*Electronics*, Jan. 22, 1987, p. 108]. The loan package, from Swiss and U.S. investment groups, is designed to relieve Flexible's cash shortage. The firm also earlier received loans totaling $455,000 from a major stockholder. Flexible president Nicholas Matelan says additional financing this spring is being contemplated by European investors.

MICROWAVE OVENS TOP THE CHARTS

More microwave ovens were shipped to the U.S. market last year than any other major appliance in history, accounting in units for more than 25% of all appliances sold, says the Association of Home Appliance Manufacturers in Chicago. Driven by a trend toward smaller models with more electronic features, microwave oven shipments last year totaled 12.4 million units. That's up 14.3% over 1985, helping to push the appliance industry to its third consecutive record year, the association says. Microwave ovens are now in about 60% of all U.S. households.

U.S. ELECTRONICS EMPLOYMENT DIPS

Employment in the U.S. electronics industry fell 0.8% during the first nine months of 1986, says the American Electronics Association. The Palo Alto, Calif., trade group reports that jobs in the computer segment dropped 3%—more than 16,000 positions—while semiconductors picked up 900 jobs for a 0.3% gain, and software/programming climbed 5.2% with 10,000 new jobs. The total number of jobs in the industry fell from 2.54 million in January to 2.52 million in September.

AT&T SIGNS TWO FOUNDRY DEALS

AT&T Co. will be providing foundry services for Western Digital Corp. under the terms of two deals that could be worth as much as $50 million or more over the next three years. Under the first deal, which covers application-specific integrated circuits and could be worth between $8 million and $20 million, Western Digital, Irvine, Calif., will purchase a guaranteed minimum volume of chips built by AT&T at its Orlando, Fla. fabrication line. A second deal, worth $30 million, calls for AT&T to manufacture Western Digital's line of standard silicon products and will help Western Digital speed its migration to 1.25-μm geometries.

ZENITH BUCKS OFFSHORE TIDE

In contrast to the trend toward offshore manufacturing by U.S. electronics suppliers, Zenith Electronics Corp. says it plans to add up to 600 new jobs at its color picture tube plant in Melrose Park, Ill. The new workers will join some 2,100 already employed at the plant, and are needed to begin production of cathode-ray-tube displays based on Zenith's flat tension-mask technology unveiled last year [*Electronics*, May 12, 1986, p. 76]. Zenith says the domestic expansion is made possible in part by some $725,000 in job training funds pledged by state and local officials and by contract concessions negotiated by Zenith with the International Brotherhood of Electrical Workers.

GE, FANUC FORM JOINT VENTURE

General Electric Co., Fairfield, Conn., and Fanuc Ltd. of Oshino-mura, Japan, have combined their factory automation businesses into GE Fanuc Automation Corp., a $200 million multinational joint venture. Headquartered in Charlottesville, Va., the 50-50 venture will sell software, controllers, industrial computers, and data networks, but it will not sell robots. Robert Collins, president and chief executive of GE Fanuc Automation North America, says GE Fanuc will act as a systems integrator on the factory floor. The company, which will also have operating units in Japan and Europe, anticipates sales of about $250 million in 1987.

APOLLO BOUNCES BACK STRONGLY

Apollo Computer Inc.'s shift to standards may be paying off. In the past year the Chelmsford, Mass., company has responded to critics by offering two versions of Unix, plus links from its proprietary network to industry standards—and now it reports a 71% jump in sales to more than $70 million for the fourth quarter, ended Jan. 3. Contributing to the rise is the success of its low-end work station, the Domain Series 3000, which at a base price of under $10,000 sold 7,000 systems from March through December of 1986.

3COM BUYS MAC SOFTWARE FIRM

The beachhead established by the Macintosh computer in the office marketplace has prompted 3Com Corp. to acquire a software firm that specializes in Mac software and to tailor its own software to fit more Macintosh products. The Santa Clara, Calif., network specialist has signed a letter of intent to acquire Berkeley-based Centram Systems West, designer of the TOPS file server, for an undisclosed sum. 3Com has also tailored its 3+ network operating system for the Macintosh and announced support for the AppleTalk work-station/server filing protocol.

ROBOT SYSTEM LOADS DATA TAPES

A robotic storage and retrieval system for 3480-type data tape cartridges, announced last week by Storage Technology Corp., can hold up to 6,000 cartridges in a single library module, for about 1 terabyte of data that can be accessed relatively quickly. The Louisville, Colo., company says the 4400 Nearline system takes an average of 11 seconds to mount a tape in a drive, and 15 s worst-case. Shipments are due to start in the fourth quarter, and cost is said to be less than 50¢ per megabyte.

DEC BEEFS UP REAL-TIME LINEUP

Digital Equipment Corp. will continue efforts to strengthen its real-time product line later this year by offering real-time capability for multiple processors on the VAX BI Bus. The Maynard, Mass., computer giant also promises that the recently introduced KA620, a 32-bit single-board computer with a modified Microvax II CPU optimized for real-time environments, will be used as a building block for future application-specific system offerings.

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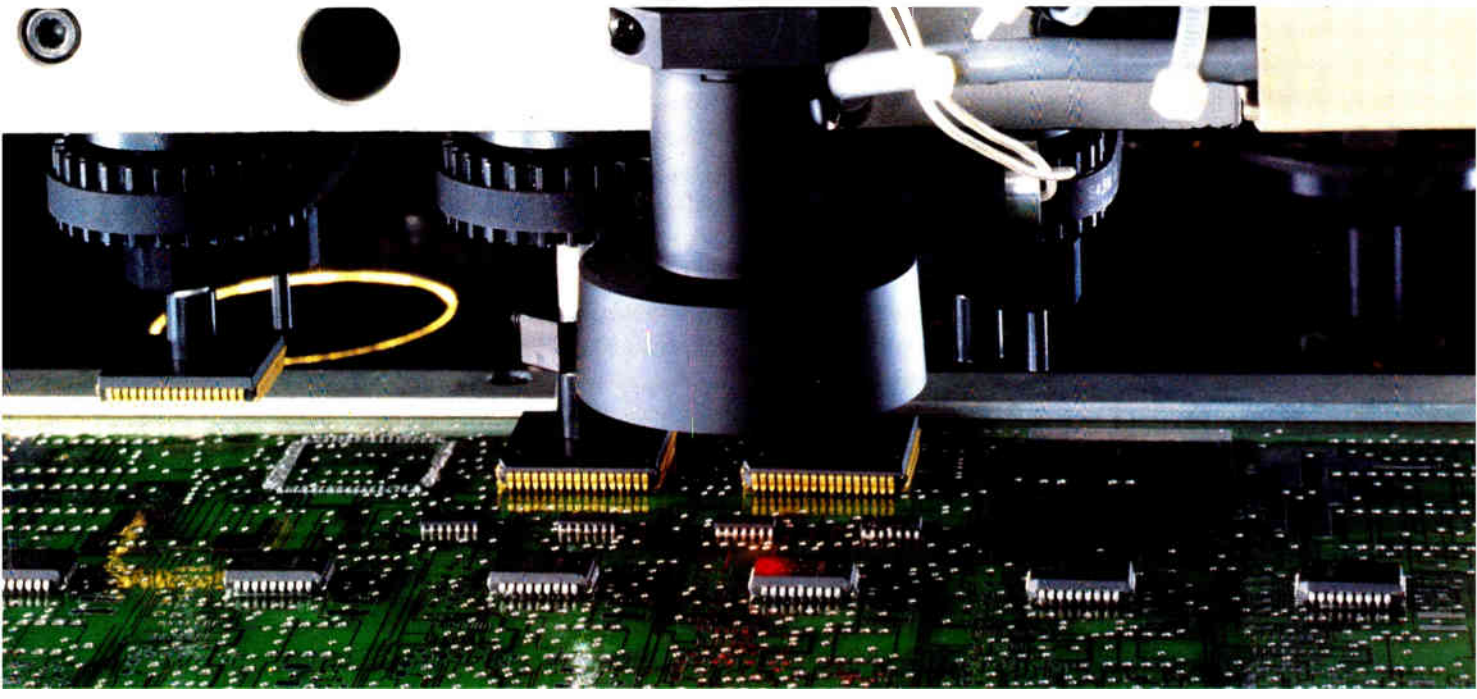

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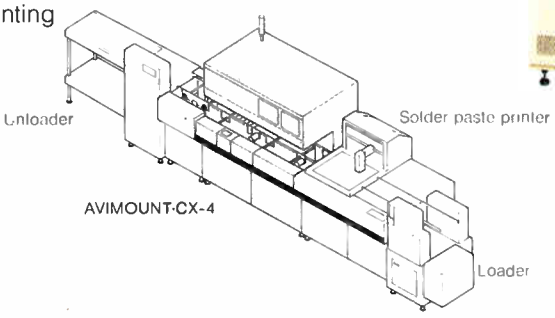

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