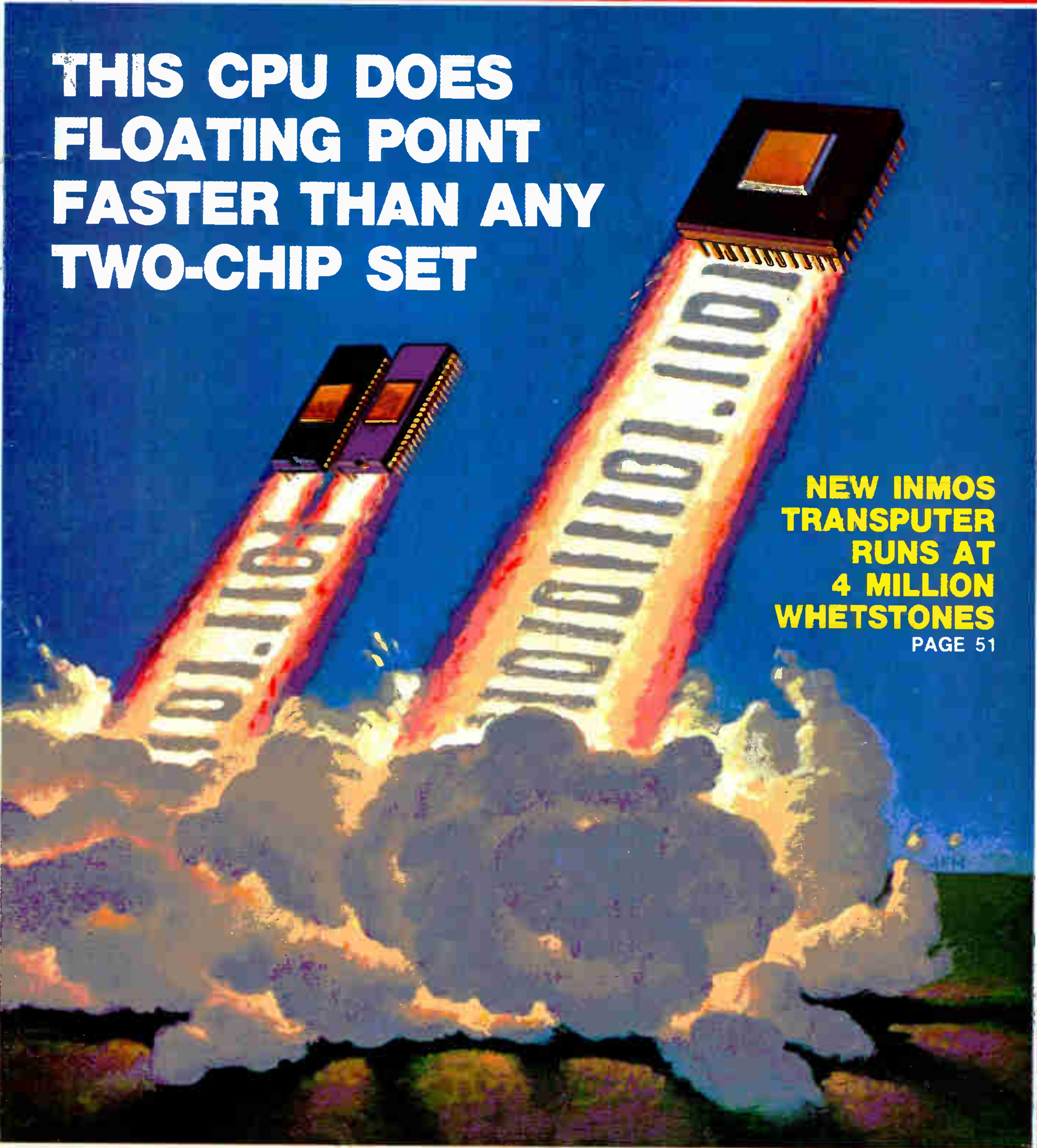
WHAT THE HOT TRENDS WILL BE AT IEDM/66

CONTACTLESS ARRAYS SHRINK EPROM SIZE AND COST/70

A McGRAW-HILL PUBLICATION SIX DOLLARS NOVEMBER 27, 1986

# Electronics



## THIS CPU DOES FLOATING POINT FASTER THAN ANY TWO-CHIP SET

**NEW INMOS TRANSPUTER RUNS AT 4 MILLION WHETSTONES**

PAGE 51

# HiWIRE™ Starts the Job that smARTWORK® Finishes

### Introducing HiWIRE™

Wintek's smARTWORK® is used by thousands of engineers to design printed-circuit boards. Now Wintek introduces HiWIRE, an electronic-schematic program that is easy to learn and use.

With a click of the mouse button, you can extract symbols from our library of over 700 common components and connect them with wires and buses. You can also easily modify the library's symbols or create your own by combining labels, lines, and arcs.

### HiWIRE Advantages

- ☐ Easy-to-learn mouse/menu-driven operation
- ☐ Complete documentation and tutorial
- ☐ Extensive TTL, CMOS, microprocessor, and discrete-component libraries
- ☐ Rubberbanding
- ☐ Moving, copying, mirroring, and rotating of symbols
- ☐ Text-string searching
- ☐ Multiple display windows
- ☐ High-quality schematics from printers and plotters
- ☐ Hierarchical-design support; netlist and bill-of-materials utilities
- ☐ Schematic/layout cross checking
- ☐ 800 number for free technical support

### System Requirements

- ☐ IBM Personal Computer, PC XT, or PC AT with 320K RAM, parallel printer port, 2 disk drives, and DOS V2.0 or later
- ☐ IBM Color/Graphics Adapter or EGA with RGB color monitor
- ☐ Microsoft Mouse
- ☐ IBM Graphics Printer or Epson FX/MX/RX-series dot-matrix printer, and/or:
- ☐ Houston Instrument DMP-40, 41, 42, 51, 52 or Hewlett-Packard 7470, 7475, 7550, 7580, 7585, 7586 plotter

### High Performance at Low Cost

At $895, HiWIRE delivers quality schematics quickly and easily. You don't need to guess whether or not HiWIRE is right for you. Our money-back guarantee lets you try it for 30 days at absolutely no risk. Call (800) 742-6809 toll free today and put HiWIRE to work tomorrow.

**Wintek Corporation**
1801 South Street
Lafayette, IN 47904-2993
Telephone: (800) 742-6809
or in Indiana (317) 742-8428
Telex: 70-9079 WINTEK CORP UD

"HiWIRE" is a trademark, and "smARTWORK", "Wintek", and the Wintek logo are registered trademarks of Wintek Corporation.

Europe: RIVA Terminals Ltd., England, Phone: 04862-71001, Telex: 859502/Australia: Entertainment Audio Pty. Ltd., Phone: (08) 363-0454/Brazil: Comicro Informatica E Tecnologia Ltda., Phone: (041) 224-5616

Circle [illegible] on reader service card

MITEL SEMICONDUCTOR

# ISDN COMPONENT NEWS

Vol. 3

# Bypass Your Competition With T1/CEPT Access Components To ISDN By Mitel

Demand for T1/CEPT communications facilities is opening unprecedented opportunities for your MUX, LAN, Data Switch, PBX or other communications product.

T1/CEPT Interfaces belonging to the Mitel *ST-BUS*™ family of ISDN-compatible components can provide the competitive edge you need with:

- The smallest size and lowest cost per function in the industry.
- Redundant links at the same price as our competitors' single link interfaces.
- DMI and CPI compatibility.
- Software-controlled diagnostic and maintenance functions.
- Drop and insert capabilities.
- Signaling selection options for simultaneous voice, data and video transmission over a single T1/CEPT link.

The following devices offer a variety of functional and packaging choices that will minimize the cost, time and complexity of your design-in:

- **MT8974/75 –** T1 Interface ICs with extensive interface support functions.
- **MH89740/50 –** T1 Interface Module with Clock extraction and line equalization.
- **MH89756 –** T1 Interface Module with line coupling transformers, microprocessor control port, time slot switching, clock sources and PLL synchronization.
- **MH89780/785 –** CEPT family of 2.048 Mbit/s interface components that functionally are compatible with our T1 Interfaces.

Don't let the opportunity bypass you – pick up the phone now and talk with us about worldwide Primary Rate Access.

MITEL® SEMICONDUCTOR

**UNITED STATES** – San Diego, California. Telephone: (619) 276-3421. San Jose, California. Telephone: (408) 249-2111. Oakbrook, Illinois. Telephone: (312) 655-3930. Boca Raton, Florida. Telephone: (305) 994-8500. **CANADA** – Kanata, Ontario. Telephone: (613) 592-5630. **UNITED KINGDOM** – Portskewett, Newport, Gwent, South Wales NP6 4YR. Telephone: +44 291-423355. **ASIA** – Tsuen Wan, Hong Kong. Telephone: +852 0-463641. **EUROPE** – Denmark. Telephone: +45 1-612566. Milan, Italy. Telephone: +39 2-6245222/8245177. West Germany. Telephone: +49 711-7701522.

Circle 2 on reader service card

No other publication covering the electronics industry can match the coverage of technology news overseas from our full-time bureaus in Tokyo, Frankfurt, Paris, and London. The extent of our circulation in Europe and Japan is evidence of the breadth of our reportage.

The only way we can maintain that level of quality is to maintain the quality of the people who report and interpret the news, and the debut this week (see p. 32) of Steve Rogerson, our new man in London, is a case in point. Steve, who as a child lived in Pennsylvania for 18 months, is a native of Oldham near Manchester, and studied physics at Lancaster University. "There, I became heavily involved in the university radio station and newspaper, which is where I first fell in love with writing." He then went to work in 1979 for the Institution of Electrical Engineers, the British organization that is the equivalent of the U. S.-based Institute of Electrical and Electronics Engineers.

**ROGERSON:** His education and experience prepared him well for *Electronics*.

"For the first year I was an assistant editor on *IEE Proceedings* and then moved on to be a reporter on two other *IEE* publications: *IEE News* and *Electronics & Power*," says Steve. While he was with the trade group, he studied periodical journalism at the London College of Printing.

Early in 1981, Steve found a job as a technical writer on a weekly newspaper for electrical contractors. "I stayed there until August 1983, when I joined Morgan Grampian as a reporter on *Electronics Times*, the UK's top electronics newspaper. A year later I was promoted to features editor. I stayed there until I joined *Electronics*," says Steve.

"The reasons I joined *Electronics* are many. But most important, I wanted a new challenge, and being a foreign correspondent for an American magazine offered such a challenge. I had always read *Electronics* and considered it the most professional in the field; now that I am on the staff of the magazine I can see that my initial reactions were right and that I have made the right choice."

Steve gave up soccer, a favorite pastime, a few years ago because of injury. Since then, he's filled his spare hours by collecting comics, beer mats, and matchboxes. He also has a serious side: he is a member of Camra (Campaign for Real Ale) and the Society for Preservation of Beers from the Wood.

Our next issue will be dated Dec. 18, and it promises to be a winner. The issue will contain *Electronics'* annual year-end survey of how executives and technology managers around the world perceive the major issues and problems facing the industry. Included will be their predictions of the star technologies of 1987.

*November 27, 1986 Volume 59, Number 36*
*144,538 copies of this issue printed*

Electronics (ISSN 0883-4989). Published biweekly by McGraw-Hill Inc. Founder: James H. McGraw 1860-1948. Publication office: 1221 Avenue of the Americas, N. Y., N. Y. 10020, second class postage paid at New York, New York and additional mailing offices. Postage paid at Montreal, P. Q. Registration Number 9034.

Executive, editorial, circulation, and advertising addresses: Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N. Y. 10020. Telephone (212) 512-2000. Teletype 12-7960 TWX 710-581-4879. Cable address: M C G R A W H I L L N E W Y O R K.

Subscriptions limited to professional persons with active responsibility in electronics technology. No subscriptions accepted without complete identification of subscriber name, title or job function, company or organization, and product manufactured or services performed. Based on information supplied, the publisher reserves the right to reject nonqualified requests. Subscription rates: the United States and possessions $32 one year, $55 two years, $76 three years; company addresses and company libraries $40 one year, $67 two years, $93 three years; Canada and Mexico $34 one year, $57 two years, $78 three years; Europe $50 one year, $85 two years, $125 three years; Japan, Israel, and Brazil $85 one year, $140 two years, $200 three years; Australia and New Zealand $95 one year, $170 two years, $240 three years, including air freight; all other countries $50 one year, $85 two years, $125 three years. Limited quota of subscriptions available at higher-than-basic rate for persons allied to field served. Check with publisher for these rates. Single copies: $6.00. Please allow four to eight weeks for shipment.

Officers of McGraw-Hill Information Systems Company: President: Richard B. Miller; Executive Vice Presidents: Frederick P. Janrot, Construction Information Group; Russell C. White, Computers and Communications Information Group; J. Thomas Ryan, Marketing and International. Senior Vice President: Francis A. Shinal, Controller. Senior Vice Presidents-Publishers: Laurence Altman, Electronics; Harry L. Brown, BYTE; David J.McGrath, Engineering News-Record. Group Vice President: Peter B. McCuen, Communications.

Vice Presidents: Fred O. Jensen, Planning and Development; Michael J. Koeller, Human Resources; Talat M. Sadig, Systems Planning and Technology. Vice President-Publisher: Paul B. Beatty, Architectural Record and Building Economics.

Officers of McGraw-Hill Inc.: Harold W. McGraw Jr., Chairman; Joseph L. Dionne, President and Chief Executive Officer; Robert N. Landes, Executive Vice President and Secretary; Walter D. Serwatka, Executive Vice President and Chief Financial Officer; Shel F. Asen, Senior Vice President, Manufacturing; Robert J. Bahash, Senior Vice President, Finance and Manufacturing; Ralph R. Schulz, Senior Vice President, Editorial; George R. Elsinger, Vice President, Circulation; Ralph J. Webb, Vice President and Treasurer.



Subscribers: The publisher, upon written request to our New York office from any subscriber, agrees to refund that part of the subscription price applying to copies not yet mailed. Please send change-of-address notices or complaints to Fulfillment Manager; subscription orders to Circulation Manager, Electronics, at address below. Change-of-address notices should provide old as well as new address, including zip codes. Attach address label from recent issue. Allow one month for change to become effective. Subscriber Service: call (201) 981-1064, 9 a.m. to 4 p.m. EST. Postmaster: Please send address changes to Electronics, att. Fulfillment Manager, CN 808, Martinsville, N. J. 08836.

**Editorial department phones:** Administration (212) 512-2645, News and New Products (212) 512-2685, Technology (212) 512-2666. Bureaus: Boston (617) 262-1160, Chicago (312) 751-3811, Dallas (214) 458-2400, Los Angeles (213) 480-5234, New York (212) 512-3322, San Francisco/San Mateo (415) 349-4100, Washington (202) 463-1650, Frankfurt 72-5566, London 493-1451, Paris 42-89-03-80, Tokyo 581-9816.
**Business departments:** (212) 512-6435 (Business departments follow the Advertisers' Index).

Electronics

## NEWS



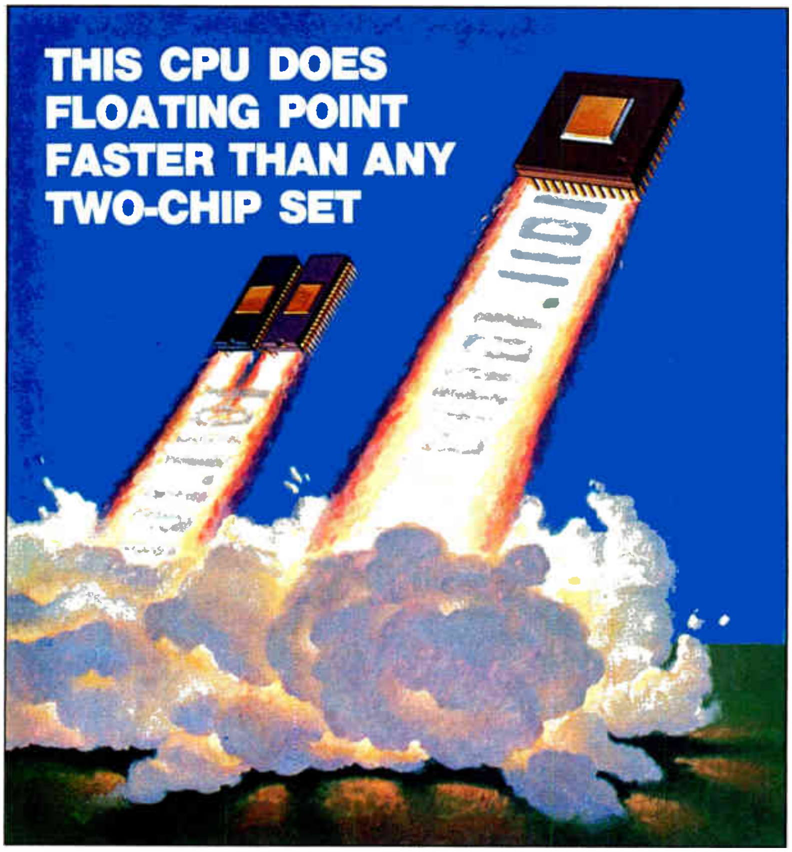
## INSIDE TECHNOLOGY



## PROBING THE NEWS

VOLUME 59, NO. 36

COVER: JOEL NAPRSTEK



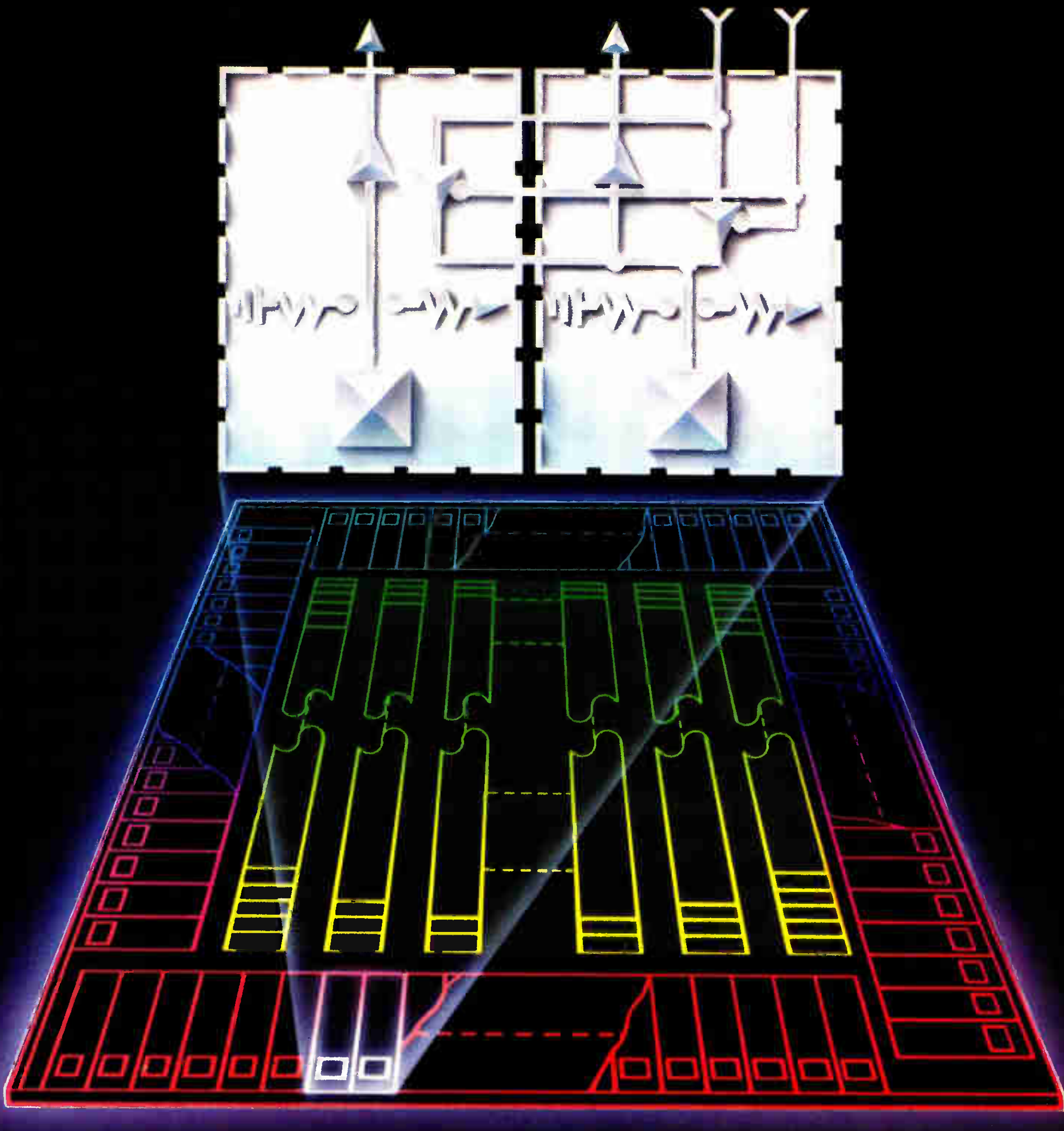

PAGE 51

## NEW PRODUCTS



## DEPARTMENTS

MOTOROLA



# The only CMOS arrays you need.

## Our '62A00 Series with advanced universal I/O offers densities to 8,500 gates.

Look again if you think there's little or no difference among available CMOS arrays.

Motorola's new 2-micron silicon-gate CMOS HCA62A00 Series provides advanced features that spell real simplicity in semicustom design solutions for both commercial and military applications.

### Advanced 2-Micron HCA62A Series HCMOS Macrocell Arrays

| Array Type | Gate Equivalent | Primary Cells | Available I/O Pads | Available Packages (# Pins) |
|---|---|---|---|---|
| HCA62A06 | 648 | 216 | 44 | 16-44 |
| HCA62A10 | 957 | 319 | 52 | 24-52 |
| HCA62A17 | 1638 | 546 | 68 | 28-68 |
| HCA62A25 | 2448 | 816 | 84 | 40-84 |
| HCA62A36 | 3600 | 1200 | 100 | 40-100 |
| HCA62A50 | 4968 | 1656 | 124 | 40-120 |
| HCA62A85 | 8568 | 2856 | 168 | 68-168 |

### Universal I/O buffers take you from schematic to semicustom chip. Fast.

Our advanced HCA62A Series lets you move from concept to finished silicon with ease and speed, letting you put the signal and power pins anywhere you want them. For high output drive, you can parallel up to six output cells on a chip for 24 mA through a single pin. If that isn't unique enough, the same cells you paralleled to obtain the higher drive can still be used as array inputs. You can have your cake and eat it too: high output drive without reduced pin utilization. That's a Motorola exclusive.

Still another creative feature of the HCA62A Series is integral oscillator macros. Adjacent input buffers can form on-chip oscillators, with frequencies controllable from 1.0 to 60 MHz, for clocking internal cells. Frequencies are adjusted simply, with an external RC and crystal network.

### Replace conventional gates to 10K.

Thanks to 100% utilization and routability, Motorola's HCA62A Series will replace conventional gate arrays of up to 10,000-gate density. They're also the industry's most flexible devices, with availability in practically every packaging and pin configuration from 16-pin dual in-line to 168-pin PGA, in plastic and ceramic. The series also provides high latch-up immunity and 3 kV ESD protection. Licensed alternate sourcing is available, too.

### Complete, easy-to-use CAD development.

Perhaps as important, our high-speed, low-power HCA62A Series Macrocell arrays are supported by a complete CAD development system to quickly translate your design into working silicon. All you need to design using Motorola's CAD system is an ASCII-type terminal and a modem. Or, you can use your own engineering workstation such as Daisy, Mentor, P-CAD™ or FutureNet supported by terrific software.

Interface is that easy.

Motorola also provides a comprehensive, efficient hardware library which includes an oscillator with clock buffer. Functions are being added almost daily to make putting '62A Series performance into new or old designs even easier.

With HCA62A Series macros you can easily grow into standard cells which offer identical functions in both 3- and 2-micron technologies.

Add up these advantages of relying on Motorola for your semicustom array. Remember as well that we carry through and maintain direct control over the entire manufacturing cycle, with Motorola attention to detail and quality.

Give your designs the simplicity, flexibility, performance and quality of Motorola semicustom arrays. Give them the edge.

### One-on-one design-in help.

Get an engineer-to-engineer update on Motorola Macrocell array design-in.

**1-800-521-6274**

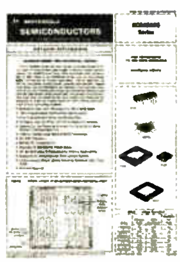
Call toll-free any weekday between 8:00 a.m. and 4:30 p.m., MST, from anywhere in the U.S. or Canada. If the call can't answer your needs, we'll have a local ASIC specialist contact you.

For published data on the HCA62A00 Series, send the completed coupon or write to Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

We're on your design-in team.

MOTOROLA

P-CAD is a trademark of Personal CAD Systems, Inc.



To: Motorola Semiconductor Products, Inc.
P.O. Box 20912, Phoenix, AZ 85036

**Please send me data on your HCA62A00 Series Macrocell arrays.**

305ELEX112786

Name ____________________

Title ____________________

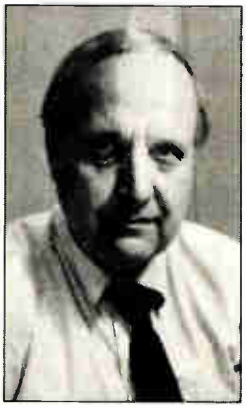
Company ____________________

Address ____________________

City ____________ State ________ Zip ________

Call me (______) ____________________

## *Comparing two big fall shows: a changing Comdex displays plenty of microcomputer pizazz, while a quiet, mature Wescon reflects a soft components market*



It may not be quite fair, but after walking the miles of exhibits at Comdex and Wescon on successive weeks, you can't help but compare the two giant shows. While Comdex/Fall turned out to be a confusing bunch of exhibits spread around Las Vegas, and a show in transition from a personal-computer dealer affair to more of an OEM event, its vitality was obvious. You got this feeling from more than just 1,200 exhibitions and 70,000 or so showgoers; you got it from the flood of exciting new products and the way that people felt in general about their business prospects. For the first time in more than two years, they felt good. Personal-computer sales are going up smartly.

The mood was far different at Wescon/'86 in Anaheim. While attendance was supposed to hit 60,000 or so for an exhibit only a bit smaller than the last Orange County Wescon in 1984, the big meeting reflected the soft components business as well as Wescon's own maturity. The show had far less pizazz than Comdex.

Getting the most attention in the flood of Comdex new products were those based on Intel's 13-month-old 32-bit microprocessor. The chip maker went all out to promote the 80386 chip, and it succeeded handsomely. More than 400 attendees at a Comdex conference heard International Data Corp. market researcher Will Zachmann proclaim the arrival of the second generation of computers, based on the 386 and its 32-bit competitors, that will radically change the basic structure of the entire computer industry. He says the new generation of computers will look more like consumer products than conventional computers and "will accelerate the rate of effective innovation and the decline in prices." It will also extend the microprocessor into those markets now dominated by the minicomputer and the mainframe system.

After that rousing prediction, Intel vice president Dave House listed 18 customers who had new products at Comdex based on Intel's 386 and/or 82786 graphics processor (see p. 85). He forecast that "Intel would sell more 32-bit microprocessors in 1987 than any other manufacturer." House seems to be off to a good start: More than 200 companies have committed themselves to the 386, he says, and Intel is racking up 50 design wins per quarter. Many of those, no doubt, will show up at next year's Fall Comdex, making it even more exciting than the 1986 edition. **ROBERT W. HENKEL**

# Don't miss the details!


## Let LeCroy help you make sure you capture all the detail of every signal every time with WAVEFORM-CATALYST PC-Based Multichannel Oscilloscope

- **The Fastest Sampling ... to 200 megasamples/sec**
- **Into The Longest Memories ... 8K to 2M samples**
- **On The Most Channels ... from 1 to over 100**

LeCroy's WAVEFORM-CATALYST Multichannel Digital Oscilloscopes make sure you capture all the detail of every signal every time. Analog bandwidth to 100 MHz and fast sampling provide fidelity and high resolution. Long memories insure total signal capture even at high sampling rates.

Plug-in modular design allows you to configure exactly what you need today, yet expand to meet tomorrow's requirements. One hundred or more input channels with independent time bases, triggering and memory lengths can operate side-by-side for optimum views of the same or different signals.

And the IBM PC™ provides simple operation, comprehensive displays, and flexible disk archiving. Waveform measurements can be made with versatile cursors or optional post-processing and user-designed automation.

™IBM PC is a registered trademark of International Business Machines Corporation.

**LeCroy**

700 S. Main St., Spring Valley, NY 10977, (914) 578-6038; Geneva, Switzerland, (022) 82 33 55; Heidelberg, West Germany, (06221) 49162; Les Ulis, France, (6) 907.38.97; Rome, Italy, (06) 320-0646; Botley, Oxford, England, (0865) 72 72 75.
Representatives throughout the world.

Circle 9 For Information

Circle 102 For Demonstration


MORRISON
CLOSED

# YEARS FROM NOW, WILL YOUR MILITARY SUPPLIER BE JUST A BAD MEMORY?

It's no secret—there's a lot of uncertainty in the marketplace. You never know if the company you're dealing with today will still be around to service you tomorrow. And that's a chance you can't take—especially in the military market.

With INMOS, you're not taking any chances. We have a seven-year history of supporting all major military defense programs with static and dynamic RAMs. Our fabrication facilities are fully compliant with MIL-STD-883C; with military burn-in, performance testing and quality assurance conducted in Colorado Springs.

We have your future in mind with our new CMOS military SRAMs (with performance to 35ns over the full military temperature range) and military low power battery backup CMOS SRAM products. We're the only company in the world to produce 64K and 256K DRAMs with RAS access times down to 80ns, and we're going to keep on producing and servicing innovative military products year after year.

For military products you can depend on, count on INMOS—the beginning of a very good memory.

| 16K SRAMs | | |
|---|---|---|
| Device | Process | Access Times |
| IMS1400M (x1) | NMOS | 45, 55, 70ns |
| IMS1420M (x4) | NMOS | 45, 55, 70ns |
| IMS1403M (x1)* | CMOS | 35, 45, 55ns |
| IMS1423M (x4) | CMOS | 35, 45, 55ns |

| 64K CMOS SRAMs | |
|---|---|
| Device | Access Times |
| IMS1600M (x1)* | 45, 55, 70ns |
| IMS1620M (x4)* | 45, 55, 70ns |
| IMS1624M (OE, x4)* | 45, 55, 70ns |
| IMS1630M (x8)* | 45, 55, 70ns |

| MILITARY DRAMs | | |
|---|---|---|
| Device | Process | RAS Access Times |
| IMS2600M (64Kx1) | NMOS | 100, 120, 150ns |
| IMS2800M (256Kx1) | CMOS | 80, 100, 120, 150ns |
| IMS2801M (256Kx1) | CMOS | 80, 100, 120, 150ns |

*Also available as Low Power Battery Backup CMOS SRAMs with Idr of 10µA (typical Icc at 2V at 25° centigrade).

inmos, and IMS are trademarks of the INMOS Group of Companies.

## MIL-STD-883C RAMs

inmos

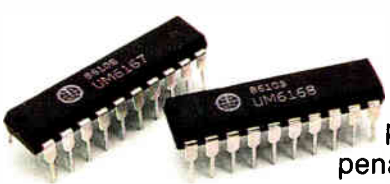
INMOS, Colorado Springs, Colorado, Tel. (303) 630-4000;
Bristol, England, Tel. (0454) 616616;
Paris, France, Tel. (1) 46.87.22.01;
Munich, Germany, Tel. (089) 319 10 28;
Tokyo, Japan, Tel. 03-505-2840.

Circle 11 on reader service card

# Score A Winning Touchdown with UMC


With backing from UNITED MICROELECTRONICS CORPORATION, one of our customers scored a winning touchdown with a voice control IC last year. He netted a profit of 2.5 million dollars on just one product. This is one of the many examples of how UMC helps its customers score financial goals.

UMC scored its first touchdown by becoming profitable 6 months after it went into operation and has been making a profit and registering phenomenal sales growth annually since then. Last year, 4 quarters of penalties left most companies sitting on the bench and several others were ejected from the game. UMC, however, still romped to a sales growth rate of 24.4%, which was the fourth best in the world and outscored 92% of the IC industry.




If you want to be on a winning team, go with a proven winner......UMC.

UMC **UNITED MICROELECTRONICS CORPORATION**

**CORPORATE HEADQUARTERS:** NO. 3, INDUSTRIAL EAST THIRD ROAD SCIENCE BASED INDUSTRIAL PARK, HSINCHU CITY, TAIWAN, REPUBLIC OF CHINA
**SALES OFFICE:** 9TH FLOOR, NO. 201-26, TUNHUA NORTH ROAD TAIPEI, TAIWAN, REPUBLIC OF CHINA TEL: (02)7152455 TLX: 28560 UMCTPE FAX: (02) 7166291
**U.S.A. HEADQUARTERS:** NMC CORPORATION 3054 SCOTT BLVD. SANTA CLARA, CA 95054 U.S.A. TEL: 408-7279239 TLX: 172730 NMC SNTA FAX: 408-9700548

## Pretty close to the mark

**To the editor:** I feel obliged to respond to statements by Robert N. Castellano in the Electronics Newsletter [*Electronics*, Oct. 30, 1986, p. 20]. In October 1983, Mackintosh International completed a study called "Gigabit Memories and Logic" that focused on technologies suitable for producing integrated circuits capable of operating at clock rates exceeding 1 GHz. Needless to say, the main thrust of the study was on GaAs digital ICs.

Our study was not one of those that "missed the mark badly." In fact, we said in 1983 that "before GaAs ICs can establish themselves securely in the marketplace, several technological objectives must be achieved." One of the key objectives was improving yields, and we wrote that "before a significant market emerges from GaAs ICs, the problem of low yields . . . must be solved so that devices of at least [large-scale integration] complexities can be made."

To quote further from our study: "Mackintosh International does not believe that GaAs will become a replacement for silicon in the foreseeable future. Predictions that GaAs ICs will form 50% of the world IC market in five years are wildy optimistic."

*George I. Stojsavljevic*
*Mackintosh Consultants Inc.*
*Natick, Mass.*

## Hitachi disputes report

**To the editor:** An International Newsletter item [*Electronics*, Oct. 30, 1986, p. 48] contains factual errors regarding Hitachi Ltd.'s semiconductor operations. The item says Hitachi "has cut production of all chips by 20%," and virtually shut down production of dynamic random-access memories. Hitachi, in fact, has not cut production quantity by 20%, and is continuing to produce a considerable amount of DRAMs. The item also incorrectly said Hitachi is "switching from memory- to logic-chip assembly at its U. S. plants." We have a plan to introduce wafer processes for logic chips at a plant now under construction in Dallas, Texas, and have scheduled to start operations at the end of next year. The existing plant at Dallas will continue to assemble memory chips.

*Manabu Kuwae, Public Relations Mgr.*
*Hitachi Ltd., Tokyo*

☐ *While Hitachi won't quantify its production cutbacks, sources maintain that the 20% figure is accurate.*

## Multiply that by 10, please

**Correction:** The correct price of the Convex XE computer [*Electronics*, Nov. 13, 1986, p. 22] is $190,000—not $19,000 as originally reported.


## NEW 32-BIT CMOS MICROPROCESSORS.

The two new members of NEC's CMOS microprocessor V-Series bring unprecedented density and performance in the 32-bit realm. The V60 and V70 supermicros are the first to integrate a Memory Management Unit and basic floating-point processing functions on a single chip.

The V60 has a 16-bit external data bus for an easy, affordable path into 32-bit products while the V70 is a full 32-bit engine designed to power leading-edge systems.

The super-fast V60 and V70 offer a clock speed of 16MHz, and execute 3.5 MIPS and 6 MIPS respectively. A six-stage pipelined CPU enables concurrent execution of up to 4 instructions. With 32 on-board 32-bit general-purpose registers, there is no need to access slow off-chip memory.

The V60/V70 feature an on-chip memory management unit with 4 gigabytes of demand-paged virtual memory space, and 4 levels of memory protection for multi-tasking and multi-user environments.

The V60/V70 instruction set is ideal for high-level languages and OS support (UNIX™ V and proprietary realtime OS). There are 21 addressing modes, 273 instructions, and an emulation mode for 16-bit V20/V30 software.

*UNIX: trademark of AT&T Bell Laboratories.*

**C&C**
Computers and Communications

# NUMBER 136

## COMING SOON: 1.3/1.55$\mu$ DFB LASER DIODES.

Dispersion has always been a major obstacle in long-distance, high-speed lightwave communications. With conventional laser diodes emitting multiple spectrums, pulses deteriorate by dispersion after long travel through the fiber. This in turn limits repeater span to 20–30km and capacity to 400–560Mbps for the prevalent 1.3$\mu$ fiber optic systems.

NEC has overcome this obstacle with newly-developed distributed feedback (DFB) laser diodes for 1.3$\mu$ and 1.55$\mu$ fiber optic transmission systems. They feature a stable single longitudinal mode operation, high efficiency and high output power. The new DFB laser diodes are expected to expand repeater span to 80–100km for 1.3$\mu$ system or 100–200km for 1.55$\mu$ system.

NEC's new DFB laser diodes inherit the renowned double channel planar-buried heterostructure (DC-PBH) and have a diffraction grating in the optical guide region to produce a single wavelength. Output powers are rated 8mw for the 1.3$\mu$ NDL5600 and 5mw for the 1.55$\mu$ NDL5650. They come in the TO-5 package with an integral monitor photo diode or chip-on-carrier configurations.

As matching light-receiving devices, NEC has planar type InGaAs avalanche photo diodes. They have a selective guard ring construction to achieve high sensitivity and excellent reliability.

## NEW INTELLIGENT BUILDING COMPLEX AT VANCOUVER.

The intelligent building is an idea whose time has come. As the perfect nestling for office workers in the Information Age, it centers on an advanced information management system which provides simultaneous voice, data and image services to tenants at less cost while it controls the entire building environment efficiently.

The World Trade Centre/Pan-Pacific Vancouver Hotel recently opened is just such an installation. NEC's NEAX 2400 Information Management System (IMS) allows tenants to utilize enhanced telephone/facsimile services including least-cost routing, message center and voice mail services, and computer terminal connection via a multifunction digital telephone set. The NEAX 2400 IMS also offers sophisticated services to hotel guests.

NEC's Intelligent Building Systems, based on our unique C&C (integrated computer and communications) technology, are the most advanced and comprehensive available today. As the core of this system, the modular NEAX 2400 IMS can expand to 255 tenant partitions. It supports more than a hundred advanced features including a protocol converter to allow communication with most popular host computers.

NEC also supplies comprehensive component equipment including multifunction digital telephones, information display pagers, high-speed facsimiles, business and personal computers, teleconferencing and CATV equipment and local distribution microwave links.

NEC's comprehensive systems breathe new life into the smart building concept, bringing costly services like teleconferencing within the reach of every business.

## NEW HIGH-CAPACITY 64QAM DMR SERIES.

NEC's newest 800 Series high-capacity digital microwave radio (DMR) systems transmit two or three DS3 signals per RF carrier, utilizing 64-state quadrature amplitude modulation (64QAM) for effective use of radio spectrum.

Three systems meeting FCC standards are available: a 4GHz 90M-bit system providing 1,344 voice channels, and 6GHz and 11GHz 135M-bit systems for 2,016 voice channels.

The new systems incorporate the latest LSIs, hybrid and microwave ICs throughout to achieve compact design, lower power consumption and improved system reliability. Housed in a standard 19-inch rack, they require minimal cabling work for installation.

The advanced 800 Series is fully compatible with Bell's facility maintenance and administration system.

**NEC**

# DREW IS UNRUFFLED BY CLOSE VOTE IN IEEE RACE

**NEW YORK**

After all the dust had settled, and all 52,334 votes cast in the race for the presidency of the Institute of Electrical and Electronics Engineers were counted earlier this month, Russell Drew's margin of victory was just 242 votes. Drew, the president of a Sterling, Va., instrument-maker, edged his nearest competition by less than 0.5% of the vote.

Drew's narrow margin may even have been something of a moral victory for runner-up Irwin Feerst, the outspoken IEEE critic who for years has maintained that the Institute does not serve the needs of the professional engineer. Feerst is contesting the results before the IEEE Credentials Committee. The committee is not empowered to overturn the results, however, so if Feerst's plea is upheld, a new election will follow.

None of this seems to worry Drew, who spent most of a 20-year Navy career in Washington as a principal staffer in the Science and Technology Policy Office, a part of the executive branch. His experiences first as a naval aviator, and later as a White House science and technology adviser (he worked for Presidents Johnson, Nixon, Ford, and Carter), apparently taught him to stay calm in tight elections.

**DREW:** The opposition's ideas are still very much a minority view.

Drew's work is cut out for him, though. One of two candidates nominated by the IEEE's board of directors, he handily slipped by Merlin Smith, the board's other nominee, who garnered 30.2% of the vote compared with Drew's 35.1% share. Outpolling Feerst, who wound up with 34.6%, was not so easy.

Feerst dismisses the idea of a moral victory, saying that "I didn't win, I didn't make a point." Drew admits, though, that the close finish lends credence to some of Feerst's points, especially issues of fair pay and fair treatment for working engineers. The 55-year-old Drew says these will be his primary concerns during his apprenticeship as president-elect. (Under IEEE bylaws, the winner serves one year each as president-elect, president, and past president.)

"If you look at the two board candidates, we kind of outpolled Feerst by almost a 2 : 1 ratio," says Drew. He isn't worried by the surprising support for Feerst, who promised to clean house at IEEE headquarters. Feerst's ideas are the minority view, Drew says, but he adds that such support should trigger concern.

"I'm not really sure why people voted for Irwin, but we'll look into that," Drew says. "Some of the things he's concerned about are things the institute is concerned about—like unemployment and employment practices that might ultimately be detrimental. I respect that kind of message."

Drew himself is not a typical IEEE candidate. It is almost ironic that Feerst, that attacker of the institute's status quo, lost to a man who himself is a relative newcomer to the IEEE.

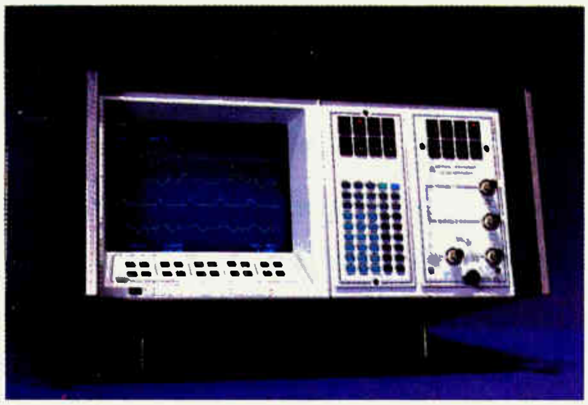
Drew didn't join the institute—or the commercial world—until 1978, when he retired from the Navy to join Systems Control Inc., Palo Alto, Calif., as vice president for Washington operations. In 1983, Drew helped found Viking Instruments Corp. with technology that was originally developed for the Viking space program. The company makes mass spectrometers, specializing in portable but highly sensitive instruments that are used in space research and other fields to determine the nature of organic substances.

Drew says his experience working in government agencies such as the Science and Technology Policy Office and the National Science Foundation will help him in his leadership role at the IEEE.

"If you look at the role of the president of the IEEE, one thing he's responsible for is to interact with leaders in the scientific community, in government, and in industry," Drew says. "To do that, the experiences I've had—particularly in the White House—can be a great asset. I can talk to a number of these leaders on a familiar basis."

Moreover, he says, being part of Viking's 12-person team has attuned Drew to the concerns of entrepreneurs and working engineers.

"I'm very sympathetic to entrepreneurial spirit, because I'm part of that movement," he says. "I'm not just a manager. I'm also in the lab. I'm very much a working engineer." *–Tobias Naegele*



*DATA 6000 Waveform Analyzer*

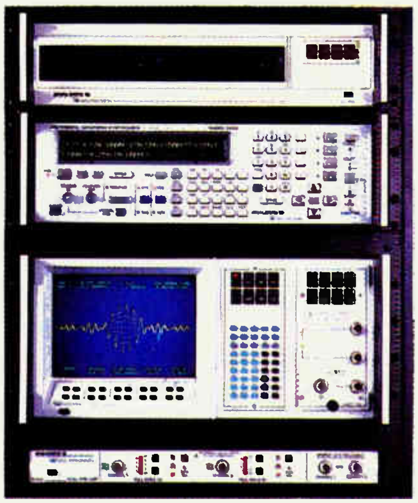
*DATA 2020 Waveform Generator*

# Rule the Waves

## Coming...

The DATA 6000 Universal Waveform Analyzer offers the ultimate in signal acquisition and on-board waveform analysis in one unit—without programming. Front panel commands are available for complex waveform operations, such as FFT and Correlation as well as scalar parameters such as Max., Min., Width, Rise, or PK-PK, using the display cursor and crosshair. For specialized measurements, the 6000 can also store analytical routines internally.

- Digitizing Plug-Ins from millihertz to 100MHz sample rates.
- An ultra-high dynamic range digitizing plug-in: 1MHz at 16 bits.
- Simultaneous multi-channel sampling with pre- and post-trigger transient capture.
- FFT (Magnitude and Phase), Convolution, Correlation, Waveform Average, Amplitude Histogram, etc.
- Direct plotter drive for HP-GL compatible plotters.
- Companion Model 681 Flexible Disk Drive for waveform and program storage.
- Full Programmability for ATE via IEEE-488 or RS-232 interface.



Combining the DATA 2020 and DATA 6000 yields an unbeatable system for signal acquisition, analysis *and regeneration.* Capture actual signals with the DATA 6000. They can then be modified or combined with other waveforms and down-loaded into the 2020 for regeneration. What was transient can become repetitive, available on call. Shown above, from top to bottom, are the 681 Flexible Disk, the DATA 2020, DATA 6000 and D-1000 Pre-Amplifier: products which give you the power to rule the waves both coming *and* going.

## or Going.

The DATA 2020 Polynomial Waveform Synthesizer* provides an unprecedented ability to emulate real world signals, creating desired waveforms from mathematical definitions. Modify the ideal waveforms to add distortion, noise or glitches. Simulate degraded rise times, phase shifts . . . test the limits. Your systems and products must live in the real world. Emulate it with the 2020.

- Direct front panel or remote entry of mathematical equations of the form Y = f(t).
- High-speed waveform generation—up to 25 megapoints per second at 12 bits (100 megapoints at 12 bits, optional).
- Large waveform output memory—up to 512K points, combined with non-volatile storage of hundreds of waveform equations.
- Standard Functions—sine, square, triangle with variable symmetry, plus white noise which can be summed with any signal.
- Arbitrary Mode including point entry, scope draw, and down-loading of the waveform memory.
- Full Programmability for ATE via IEEE-488 or RS-232 interface.

*Patents pending

ANALOGIC®

DATA PRECISION®

**HEADQUARTERS: DATA PRECISION,** Division of Analogic Corporation, Electronics Avenue, Danvers, MA 01923. Tel: 617-246-1600. Telex: 6817144.
**ANALOGIC Ltd.,** The Center, Weybridge, Surrey, England KT138BN. Tel: 0932-56011. Telex: 928030 ANALOG G.
**ANALOGIC GmbH,** Daimlerring 2, 6200 Wiesbaden-Nordenstadt, W. Germany. Tel: 06122-4071. Telex: 4182587 ANA D.

Circle 17 For Demonstration    Circle 103 For Additional Information

# EVERY BUSINESS NEEDS AN IBM-PC
## WHO WANTS TO PAY IBM PRICES?
## WE HAVE A SOLUTION!!!

FACTORY DIRECT
$799.
STANDARD MODEL

100% Compatible PC-XT
BASE PRICE $950.00 LEASE $39/MO
With 20 MEG Hard Disk $1399.00 LEASE $56/MO

CALL

Upon Approved Credit

5 YEAR WARRANTY AVAILABLE

Our **PC-XT SUPER TURBO COMPUTER** runs all the popular Business Programs, like Lotus 1, 2, 3, Word Perfect, Wordstar, dBase III, Homebase, Sidekick, and Flight Simulator. In addition to running the programs at the standard IBM clock speed of 4.77 Mhz, it also runs at 8 Mhz — **almost twice as fast as IBM**.

ACS has developed the fastest, most powerful XT and AT computers available today. We have also researched the numerous software programs available to automate your office. If you are considering buying a computer, call ACS. We can recommend the software and hardware system that will best solve your business needs.

### HERE'S WHAT YOU GET
**ACS-Turbo** Mother Board 4.77/8.0 Mhz
640K of RAM
Two 360K Floppy Drives
Heavy Duty 135 Watt Power Supply
Keyboard New "AT" Type with Large Enter Key
Parallel Printer Port
Monochrome Graphics Display Card
High Resolution Mono Monitor
with Swivel Base and Anti-Glare Screen

### OPTIONS

| | |
|---|---|
| 20 MEG Hard Disk | $449.00 |
| 20 MEG Tape Back-Up | $595.00 |
| Clock/Calendar | $ 59.00 |
| Internal Modem 300/1200 BAUD | $199.00 |
| Okidata 192 Printer | $399.00 |

### PROGRAMS INCLUDED
Included in the purchase price is MS-DOS, the standard IBM operating system. With our Hard Disk Computer, you also get HOMEBASE, a general purpose multi-function program to perform word processing, electronic filing, and data base management. HOMEBASE has a built-in calendar, with monthly, weekly, and daily scheduling. The Homebase Calculator lets you perform calculations on the monitor and the ability to print a paper tape if desired. HOMEBASE also includes a communication program with autodialer for communication with other computers (requires a modem).

### GUARANTEE & WARRANTY
We guarantee you will be delighted with our **ACS-Turbo Computer** or return it within 30 days for a refund (less shipping charges). We warranty our Turbo Computer 100% Parts & Labor for 1 year. We believe our computer is even more reliable than IBM — that's why we're offering a five-year extended warranty for only $30.00 a year. Order early for the holidays — delivery may take over 30 days.

### HOW TO ORDER
Call us at (818) 889-1092. We have experienced salespeople to advise you with your computer requirements. Ask for our experts — ask for Department FD.

You can charge our **ACS-Turbo Computer** with a VISA or MasterCard. We also have a lease plan available for qualified businesses, with payments from 36 months to 60 months.

*IBM is a registered trademark of International Business Machines.

DEALERS WANTED

**ACS**

5311 Derry Avenue, Suite A, Agoura Hills, CA 91301
Phone: 818/889-1092 Fax: 818/889-5605 Telex: 299 353 POST UR
EASY LINK Mailbox: 62941735 Telex: 5106018224 ACS AGRA HILLS UQ

# ELECTRONICS NEWSLETTER

## GE MAY SELL ITS MERCHANT-CHIP OPERATION PIECE BY PIECE

General Electric Co. is mum over the sale of its merchant semiconductor business, but a new scenario is making the rounds: GE, unable to find anyone willing to buy the entire operation, will sell the parts. The power MOS FET business in particular, built by RCA Corp.'s Solid State Division into a member of the top tier of manufacturers, would attract companies seeking either a foothold in a fast-growing segment or a way to improve market share. Motorola Inc.'s Semiconductor Products Sector, a major MOS FET player itself, is a potential bidder, according to some sources. Motorola is not a likely suitor for the entire GE operation, however, since parts of it duplicate current lines. Others in the industry are convinced that GE is trying to sell the operation to a single buyer [*Electronics*, Nov. 13, 1986, p 30]. □

## WESTINGHOUSE RACES TO MARKET FIBER-OPTIC MAP NETWORK

At least one method to hook up Manufacturing Automation Protocol networks using fiber-optic media will be available next year if Westinghouse Electric Corp. meets its schedule. Westinghouse executives said at this month's Autofact show in Detroit that they hope to be the first to market, with a fiber-optic local area network set for introduction in mid-1987. The active-star system will be designed so it can be used to develop new MAP nets or to hook up critical segments of broadband cable-based MAP networks. One key to the Westinghouse network will be the use of redundant active elements in the hub, which the company says should overcome the objections of passive-star proponents that a single failure within an active-star system could bring down an entire network. AT&T Co. and General Motors Corp. are planning to test fiber-optic MAP nets using a passive-star approach late this year, and an IEEE 802.4 subcommittee is expected to develop a proposed fiber-optic MAP specification by January [*Electronics*, Oct. 2, 1986, p. 36]. □

## VITALINK OFFERS A WIDE-AREA LINK FOR LOCAL NETS

Wide-area networks are going to be the next big market in data communications—at least Vitalink Communications Corp. thinks so. That's why the Mountain View, Calif., company is shifting its emphasis from satellite communications products to wide-area nets. Vitalink plans to link local-area networks over a variety of distances and communications media. Vitalink's concept, 802 WAN, is an expansion of its current product, TransLAN, a high-speed bridge that transparently connects two or more IEEE 802.3 Ethernet LANs. The 802 WAN operates at the data-link layer of the seven-layer open-systems interconnection reference model of the International Organization for Standardization. One 802 WAN link can simultaneously carry traffic using different high-level protocols. □

## RCA CRAMS THREE BOARDS' CIRCUITRY ONTO ONE

Engineers at RCA Corp. have crammed the circuitry of three printed-circuit boards into one double-sided board of the same size. They combined Multiwire having 100 interconnections per square inch with leadless ceramic chip carriers, which allow for a high component density, in a thermally compensated board. Developed at RCA's Government Systems Division in Cherry Hill, N. J., the technique was described at the International Electronics Packaging Conference last week in San Diego. For the Navy's Aegis radar system's signal processor, the surface-mounted board carries both leadless chip carriers and flatpacks. It uses polyimide outer layers, copper-Invar-copper thermal compensating ground and power planes, and four signal layers of Multiwire. □

# ELECTRONICS NEWSLETTER

## NEW TOKEN-RING PROTOCOL IC TO SPAN BRIDGE CONTROVERSY

Texas Instruments Inc. figures it has both sides covered in the controversy brewing over internetwork bridging techniques. A decisive rift separates many suppliers of local-area networks from a contingent led by IBM Corp., which is proposing a source-routing scheme for token rings that is different from the IEEE 802.1 spec (see p. 29). Now, look for TI to add to its TMS380 token-ring chip set a bridge-oriented protocol-handler device that with the appropriate software can support either IBM's source-routing bridge or the 802.1 transparent bridge. The new TMS38021 will contain all of the features in today's 38020 protocol-handler chip. The 38021 gives designers access to two test pins, not made available on the 38020. These pins can be used in a high-speed network-bridge node, performing an external address-checker function that automatically recognizes token-ring source-routing frames. ☐

## FLATTENING DEFENSE BUSINESS MAY NOT AFFECT ELECTRONICS INDUSTRY

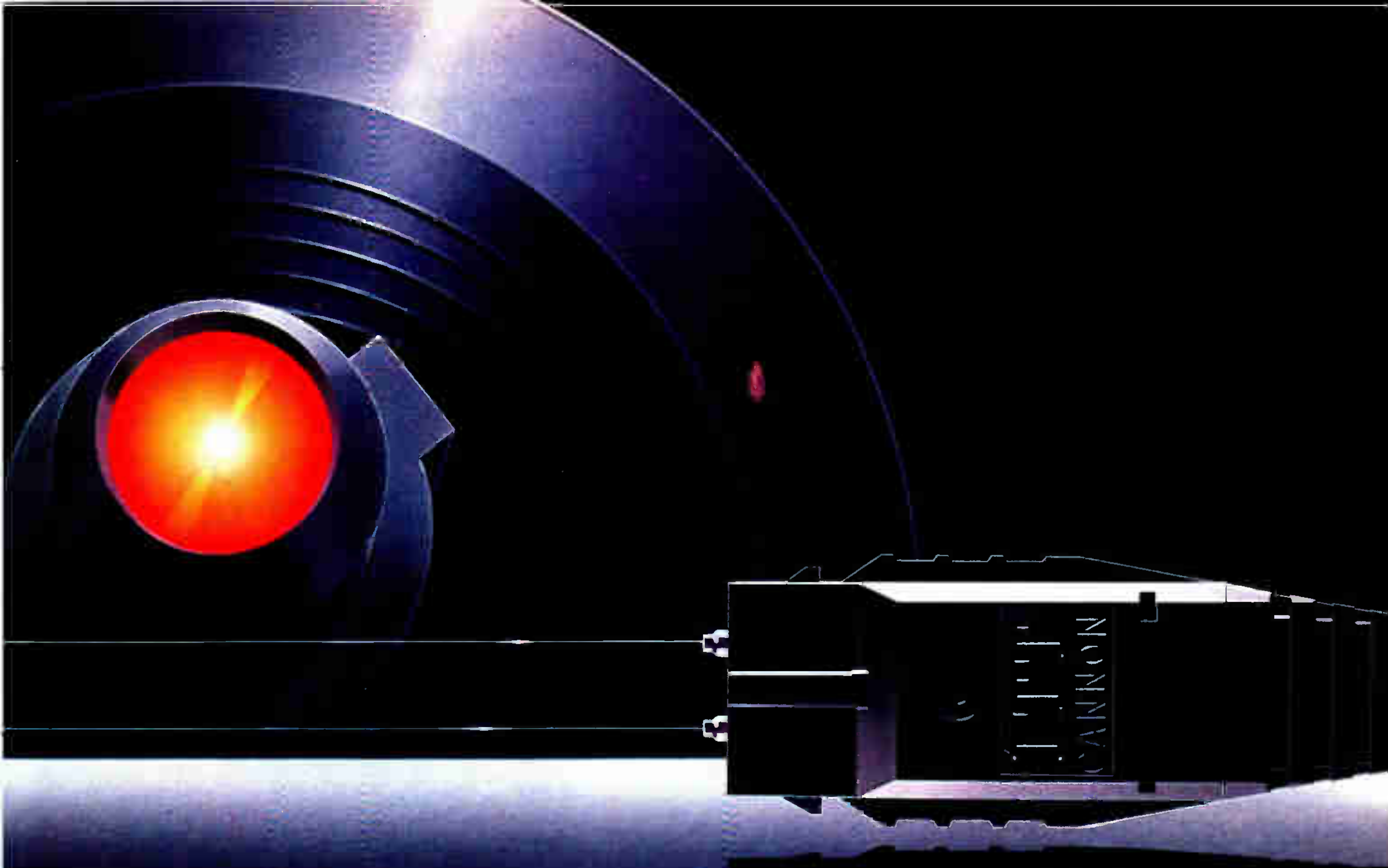
Tightening defense markets during the second half of the 1980s won't affect the electronics industry, concludes a study by Prudential-Bache Securities. The armed services are relying more on electronics to improve their effectiveness, and so the report expects growth in command, control, and communications and intelligence-gathering systems, as well as upgrades to electronic-warfare systems. The report also predicts a move toward large, fully integrated airborne-electronic-countermeasures systems; opportunities in the Strategic Defense Initiative; electronics packages for remotely piloted and robotic vehicles; smart munitions; and the continuing need to counter improvements in adversaries' capabilities. ☐

## MOTOROLA IS OFF AND RUNNING IN FACTORY CONTROLLERS

Motorola Inc. is getting into the cell-controller business for factory automation with a new company called Computer X Inc. The operation was actually formed three years ago as part of Motorola's New Enterprises program, but it was disclosed only this month at the Autofact show with word that Honeywell Inc. will be its first customer. Honeywell officials announced the selection of Computer X to supply hardware and systems software for future Honeywell factory-cell controllers. The new cell-controller platform features the Motorola M68000 microprocessor family, a VMEbus architecture, and a Computer X real-time operating system known as cXOS, Motorola says. Computer X plans to later add a real-time Unix operating environment. The company is in Schaumburg, Ill. ☐

## TI CMOS EPROM IS FAST ENOUGH TO RIVAL BIPOLAR PROM

A revised cell layout is being mixed in with an existing CMOS process to make a speedy 16-K erasable programmable read-only memory at Texas Instruments Inc. The 2-K-by-8-bit EPROM is so fast that the Dallas company will soon offer the chip as a CMOS alternative to one-time programmable bipolar PROMs. The first in a family of fast EPROMs, the TMS27C292 will have access times as low as 35 ns and will dissipate 394 mW. The 27C292 and its relatives will have half the bit-line capacitance of conventional designs and will employ a stretched differential X-cell that needs only half the bit-line swing for sense margin. The chips also feature a word-line path that is optimized with short channels and improved coupling of coefficients between control gates and floating gates. The chip's 2-$\mu$m design is considered a halfway step between some of TI's more recently announced EPROMs and its forthcoming memories that will use an advanced contactless EPROM technology (see p. 70). ☐




# Pinpoint Success

These pin points of light have the same success story.

Efficient transmission with minimum light loss. Time after time.

They belong to the fiber optic connector family of ITT Cannon: the Fiber Optic Single Channel (FOSC), Twin Channel (FOTC), Multi-Channel (FOMC) connector series and interchangeable optical contacts for standard electrical connectors.

From tactical field communication systems to LAN's to the emerging medical and transportation markets, Cannon offers an extensive line of fiber optic products for both commercial and military applications. We also have the experience and technical expertise to custom design connector systems to fit special applications anywhere in the world.

Standard product and custom-design capabilities. Part of Cannon's total commitment to the fiber optics industry and to the development of tomorrow's reliable, cost effective interconnects.

Contact our Fiber Optic Products Group, 10550 Talbert Ave., Fountain Valley, CA 92708. Or call 714/964-7400.


**ITT CANNON**
*MicroTech Division*

Circle 21 on reader service card

# PRODUCTS NEWSLETTER

## ON-RESISTANCE OF MOTOROLA MOS FET IS ONLY 0.15 OHM

The first power MOS FET fabricated in Motorola Inc.'s proprietary, TMOS IV process boasts a density of 1 million cells/in². That lowers on-resistance to a maximum 0.15 Ω and offers lower capacitance per unit area. At the heart of the device is a source-drain diode designed as a cellular anode zener able to withstand high energy in the avalanche and commutation modes. A 90-ns recovery time is suitable for bridge circuits, says Motorola's Phoenix-based Semiconductor Products Sector. The MTP3055E, a 60-V, 12-A, n-channel device, is available now and sells for 57 cents in 100-unit quantities. □

## BOARD TRANSFORMS IBM PC INTO WORK STATION FOR MINIS AND MAINFRAMES

IBM Corp. Personal Computers and compatibles become work stations for mainframes, minicomputers, and other file servers with a hardware-software combination from Ungermann-Bass Inc. The Santa Clara, Calif., company's Net/One NIUpc board introduced at last week's LocalNet show in San Francisco permits asynchronous access to Digital Equipment Corp. VAXs, Hewlett-Packard HP 3000s, and other minicomputers. Network software enables users to communicate with host applications while running other applications on minicomputers or networked PCs. Another board—the Net/One NIU 3270pc—accesses up to four IBM hosts via a network. And graphics software puts 3279 mainframe graphics at the service of the PC. The NUIpc is priced at $1,095 and the 3270pc at $1,495. All items are available now. □

## LSI LOGIC MOVES INTO STANDARD CELLS

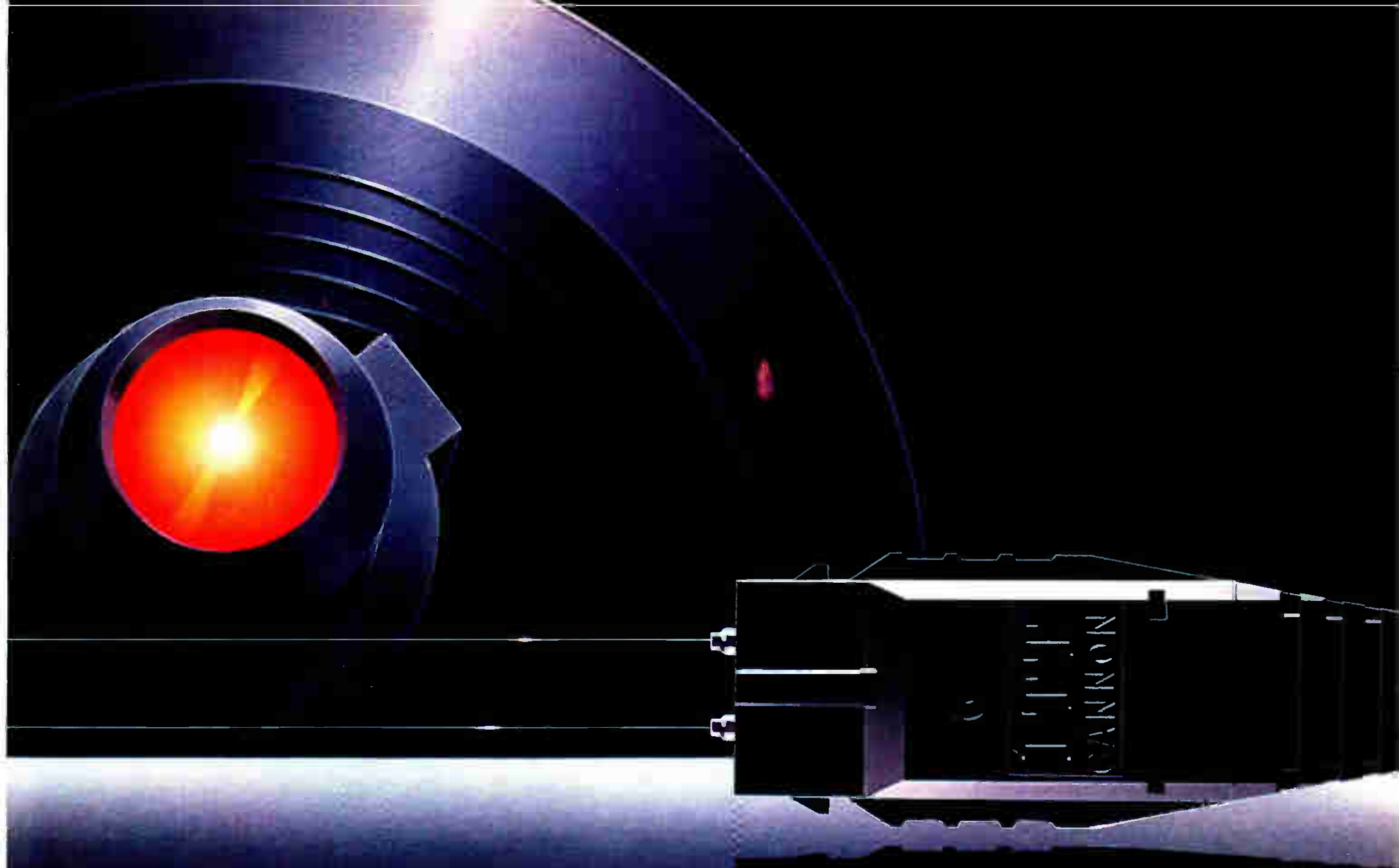
LSI Logic Inc.'s first foray out of gate arrays into standard cells—the LSC15 structured cell family—gives designers a library that includes nearly 100 large-scale-integration megacell types as well as 700 medium- and small-scale-integration cell types. Circuits containing up to 60,000 gates, with 36-K of static RAM or 512-K of ROM, are possible with the library. The circuits use the Milpitas, Calif., company's 1.5-μm, dual-layer metal CMOS process to achieve 650-ps gate delays. LSI uses the process in its LCA10000 compacted gate-array family. □

## MOSEL DELIVERS 256-K SRAMs WITH 55-NS ACCESS TIMES

Mosel, a Sunnyvale, Calif., newcomer to the growing ranks of static RAM suppliers, is trying to leapfrog to the head of the class with the announcement of a 32-K-by-8-bit device with a 55-ns access time—one of the first 256-K SRAMs to market. The chip, the MS62256, draws less than 1 μA in standby mode and typically operates at 60 mA. It's the sixth product from the three-year-old company, which plans to offer a full line of SRAMs and specialty memories, such as dual-port, first-in/first-out, and application-specific devices. The MS62256 is priced at $45 to $95 in lots of 100, depending on speed, and will be available in 12 to 18 weeks. □

## TI OFFERS PROGRAMMABLE ARRAY LOGIC WITH MACROCELL OUTPUTS

Two bipolar, programmable-array-logic devices from Texas Instruments Inc. are functionally equivalent to the sole-sourced AmPAL22V10 chips from Advanced Micro Devices Inc. The parts contain a programmable macrocell that lets users implement more complex output functions than they can with standard programmable arrays. In 1,000-piece quantities, the speed-sorted 25-ns 22V10A device is priced at $15.84 each in plastic DIPs. The 35-ns 22V10 costs $10.08 each. Programming firmware is due in January. □



# Pinpoint Success

These pin points of light have the same success story.

Efficient transmission with minimum light loss. Time after time.

They belong to the fiber optic connector family of ITT Cannon: the Fiber Optic Single Channel (FOSC), Twin Channel (FOTC), Multi-Channel (FOMC) connector series and interchangeable optical contacts for standard electrical connectors.

From tactical field communication systems to LAN's to the emerging medical and transportation markets, Cannon offers an extensive line of fiber optic products for both commercial and military applications. We also have the experience and technical expertise to custom design connector systems to fit special applications anywhere in the world.

Standard product and custom-design capabilities. Part of Cannon's total commitment to the fiber optics industry and to the development of tomorrow's reliable, cost effective interconnects.

Contact our Fiber Optic Products Group, 10550 Talbert Ave., Fountain Valley, CA 92708. Or call 714/964-7400.

Fiber Optic
Products

**ITT CANNON**
*MicroTech Division*

Circle 21 on reader service card

# Finally, a championship lineup to tackle remote measurement and control.

Center, Fred Molinari, President


Here's an unbeatable team.

IBM. Intel. And Data Translation.

Three leaders in their fields. A new standard in industrial automation for remote measurement and control.

By combining an IBM PC™ as master controller, Intel's BITBUS,™ and boards and modules from Data Translation,™ you can create a factory automation network.

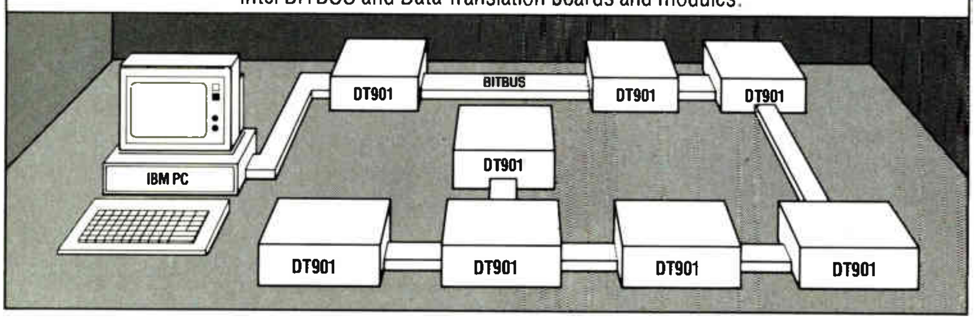
The system's modular approach lets you buy just what you need, in any configuration. And by using industry standard hardware and software, no other system is easier to implement.

You can turn your IBM PC™ into a process controller handling up to 3000 I/O points with Loopworks, a menu-driven process monitoring and control software package.

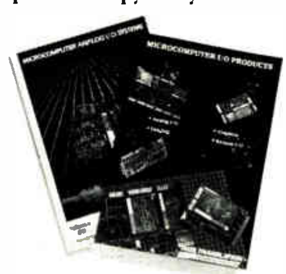
Remotely controlling your factory with such flexibility and at such low cost has been a tough goal to cross. Now there's a team to help you make the big score. Led by Data Translation.

## Call (617) 481-3700

Remote measurement and control using the IBM PC, Intel BITBUS and Data Translation boards and modules.




**See our new 646 pg. catalog handbook or see us in Gold Book 1986. Or call for your personal copy today.**



# DATA TRANSLATION


**World Headquarters:** Data Translation, Inc., 100 Locke Dr., Marlboro, MA 01752 (617) 481-3700 Tlx 951 646
**European Headquarters:** Data Translation, Ltd., 13 The Business Centre, Molly Millars Lane, Wokingham Berks, RG112QZ, England Tlx 851849862 (#D)
**International Sales Offices:** Australia (61) 2-6635289; Belgium (32) 2-7352135; Canada (416) 625-1907; Chile (2) 2-253689; China (408) 727-8222, (86) 87214017; Denmark (02) 187188; England (44) 0734-793838; Finland (358) 0-372-144; France (33) 146306839; Greece (30) 031-527039, (30) 13-614300, (30) 95-14944; Hong Kong (852) 3-324563; India (91) 2-231040; Israel (972) 3-324298; Italy (39) 2349751; Japan (81) 3-502-5550, (81) 3-348-8301, (81) 3-355-1111; Korea (82) 753-3101; Malaysia (60) 3-36299; Morocco (21) 9-30-6949; Netherlands (31) 70996360; New Zealand (61) 2-663-5289; Norway (47) (02) 559050; Peru (51) (14) 31-8060; Philippines 818-0103; Portugal (351) 1545313; Singapore (65) 271-3163; South Africa (27) 12469221; Spain (34) 14558112; Sweden (46) 87617820; Switzerland (41) 17231410, (41) 22360830; Taiwan (86) 2-721-7864, (86) 2-531 2434; West Germany (49) 89809020.


Circle 22 on reader service card

# PRODUCTS NEWSLETTER

## PHILIPS DECIDES TO TRY THE U. S.-JAPANESE-DOMINATED EEPROM MARKET

Philips International NV is plunging into the market for electrically erasable programmable read-only memories, which is now dominated by American and Japanese companies. The Dutch electronics giant's first offering will be a 256-by-8-bit CMOS device designed in a floating-gate technology. The PCF8582 EEPROM targets data-processing, automotive, and battery-powered consumer-product applications. It comes in an 8-pin DIP, needs one 5-V supply, and has a maximum standby current of 110 mA. Samples are being distributed now. Prices will be set by the local Philips organizations in importing countries. □

## RATIONAL HOPES TO BOOSTS ADA WITH ITS NEW DEVELOPMENT SYSTEMS

Rational expects to boost interest in the Defense Department's Ada programming language by cutting the cost of developing large-scale Ada software. The Mountain View, Calif., company cut a high profile at Ada Expo '86 in Charleston, W. Va., last week, where it unveiled three second-generation systems that speed development times. The Rational R1000 Development System Series 200 models 10, 20, and 40 feature incremental compilation [*ElectronicsWeek,* July 8, 1985, p. 36] and can support from six to more than 30 users, depending on configuration. To be available in January, the entry-level Model 10 is priced at $295,000; the top-of-the-line Model 40, at $795,000. Rational also announced three cross-development software packages that allow R1000 users to develop Ada applications that will run on Digital Equipment Corp. VAX/VMS, Motorola Corp. MC68000, and the Defense Department's MIL-STD-1750A-based computers. □

## PYRAMID IMPROVES PIPELINING IN ITS NEW SUPERMINIS

A pair of superminicomputers with improved pipelining and reduced-instruction-set processors are on the way from Pyramid Technology Corp., Mountain View, Calif. And larger, multiprocessor versions are in the wings, the company hints. The 9810 is a single-processor system that performs at the level of a Digital Equipment Corp. VAX 8700 for scalar applications, Pyramid says. The 9820 system is a tightly coupled dual processor that delivers about 1.7 times the performance of the 9810. Pyramid is adding a third pipeline stage that permits the new series to execute one instruction during each 100-ns clock cycle. The machines run under Pyramid's implementations of Berkeley 4.2 and AT&T System V Unix, which allow users to switch from one operating system to the other. Main memory ranges from 16 to 128 megabytes, with a 16-K-byte instruction cache and a 64-K-byte data cache. With 16 megabytes of memory, an Ethernet local-area network, 32 RS-232-C ports, a 470-megabyte disk drive, and a Unix license, the 9810 costs nearly $200,000; the 9820 package is less than $300,000. Both products are set to ship in the first quarter of 1987. □

## BENCH INSTRUMENT COMBINES FEATURES OF OSCILLOSCOPE AND A PC

The measurement capabilities of oscilloscopes and waveform digitizers are combined with the power and versatility of a personal computer by Sequence Inc. to create an instrument providing a scope's waveform measurement, and the processing and display of a personal computer. Model 3000 offers a 1 ns real-time sample interval and 10-bit amplitude resolution in single-shot sampling, according to the San Jose, Calif., company. The 3000 has a 1,024-word acquisition memory with pre- and post-triggering capability. Its single-shot input bandwidth is dc to 350 MHz. Available now, the 3000 costs $28,500. □

# PRODUCTS NEWSLETTER

## ON-RESISTANCE OF MOTOROLA MOS FET IS ONLY 0.15 OHM

The first power MOS FET fabricated in Motorola Inc.'s proprietary, TMOS IV process boasts a density of 1 million cells/in². That lowers on-resistance to a maximum 0.15 Ω and offers lower capacitance per unit area. At the heart of the device is a source-drain diode designed as a cellular anode zener able to withstand high energy in the avalanche and commutation modes. A 90-ns recovery time is suitable for bridge circuits, says Motorola's Phoenix-based Semiconductor Products Sector. The MTP3055E, a 60-V, 12-A, n-channel device, is available now and sells for 57 cents in 100-unit quantities. □

## BOARD TRANSFORMS IBM PC INTO WORK STATION FOR MINIS AND MAINFRAMES

IBM Corp. Personal Computers and compatibles become work stations for mainframes, minicomputers, and other file servers with a hardware-software combination from Ungermann-Bass Inc. The Santa Clara, Calif., company's Net/One NIUpc board introduced at last week's LocalNet show in San Francisco permits asynchronous access to Digital Equipment Corp. VAXs, Hewlett-Packard HP 3000s, and other minicomputers. Network software enables users to communicate with host applications while running other applications on minicomputers or networked PCs. Another board—the Net/One NIU 3270pc—accesses up to four IBM hosts via a network. And graphics software puts 3279 mainframe graphics at the service of the PC. The NUIpc is priced at $1,095 and the 3270pc at $1,495. All items are available now. □

## LSI LOGIC MOVES INTO STANDARD CELLS

LSI Logic Inc.'s first foray out of gate arrays into standard cells—the LSC15 structured cell family—gives designers a library that includes nearly 100 large-scale-integration megacell types as well as 700 medium- and small-scale-integration cell types. Circuits containing up to 60,000 gates, with 36-K of static RAM or 512-K of ROM, are possible with the library. The circuits use the Milpitas, Calif., company's 1.5-μm, dual-layer metal CMOS process to achieve 650-ps gate delays. LSI uses the process in its LCA10000 compacted gate-array family. □

## MOSEL DELIVERS 256-K SRAMs WITH 55-NS ACCESS TIMES

Mosel, a Sunnyvale, Calif., newcomer to the growing ranks of static RAM suppliers, is trying to leapfrog to the head of the class with the announcement of a 32-K-by-8-bit device with a 55-ns access time—one of the first 256-K SRAMs to market. The chip, the MS62256, draws less than 1 μA in standby mode and typically operates at 60 mA. It's the sixth product from the three-year-old company, which plans to offer a full line of SRAMs and specialty memories, such as dual-port, first-in/first-out, and application-specific devices. The MS62256 is priced at $45 to $95 in lots of 100, depending on speed, and will be available in 12 to 18 weeks. □

## TI OFFERS PROGRAMMABLE ARRAY LOGIC WITH MACROCELL OUTPUTS

Two bipolar, programmable-array-logic devices from Texas Instruments Inc. are functionally equivalent to the sole-sourced AmPAL22V10 chips from Advanced Micro Devices Inc. The parts contain a programmable macrocell that lets users implement more complex output functions than they can with standard programmable arrays. In 1,000-piece quantities, the speed-sorted 25-ns 22V10A device is priced at $15.84 each in plastic DIPs. The 35-ns 22V10 costs $10.08 each. Programming firmware is due in January. □

# ALL OTHERS PALE BEFORE US.

No other color graphics terminal can compare to the GR-1105. In fact, you'd have to spend an extra five or ten thousand dollars to get something even close.

The GR-1105's screen is brighter than anything else in its price class. It's also sharper. With three times the resolution of similarly priced terminals. And sixty times more addressable points (32K x 32K).

Plus the GR-1105 is perfect for people who hate to wait. It's twice as fast as its price competitors. And updates over one and a half times more data.

So look into the GR-1105. You'll see it's the one terminal that makes all others look pale.

**Call Martin Nelson at (408) 943-9100 today.**

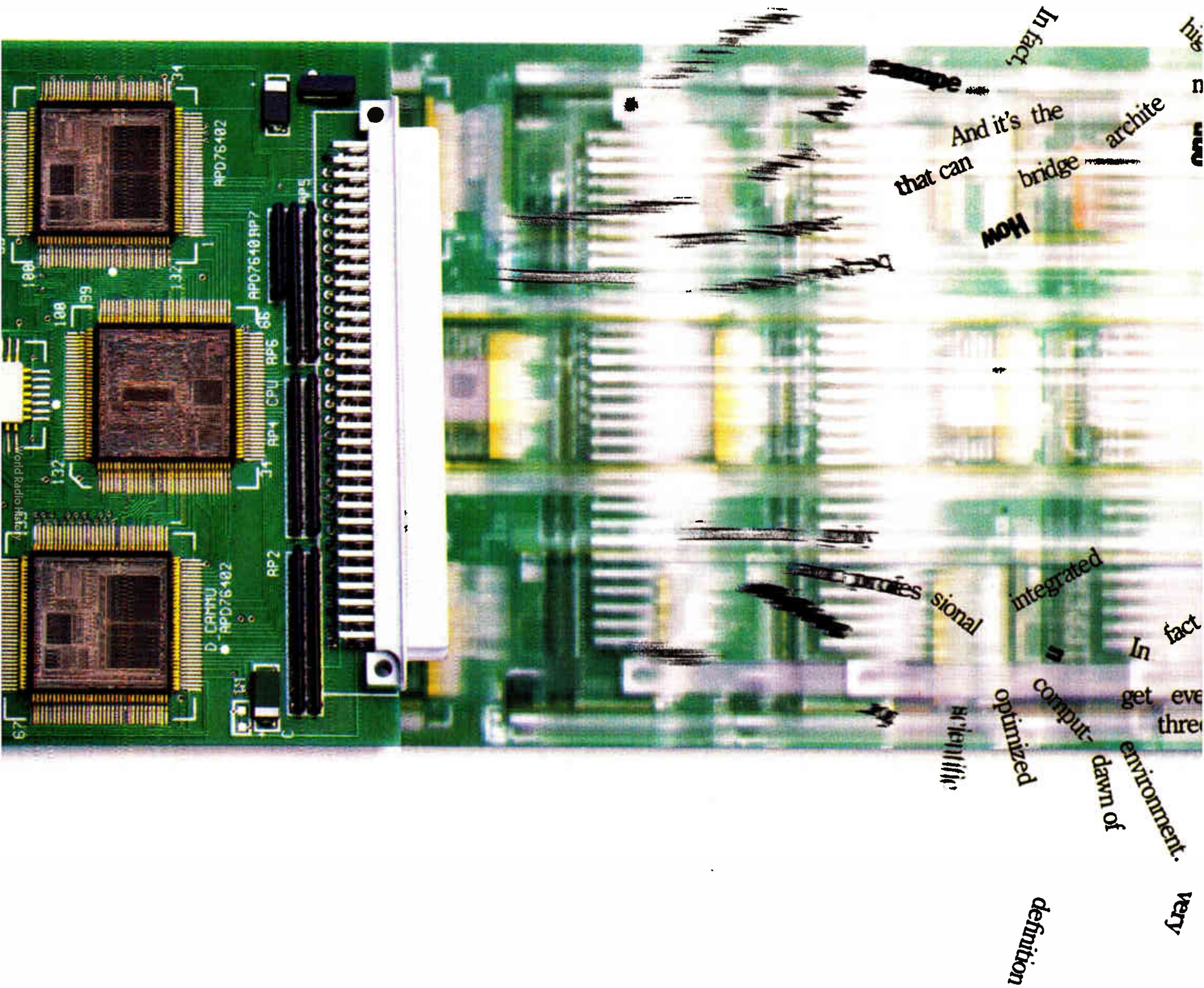
SEIKO INSTRUMENTS



Circle 25 on reader service card

You're looking at an image on the GR-1105's 14," 1024 x 780, 60Hz non-interlaced monitor. Image produced with Vectart Software from Prosperity Systems.

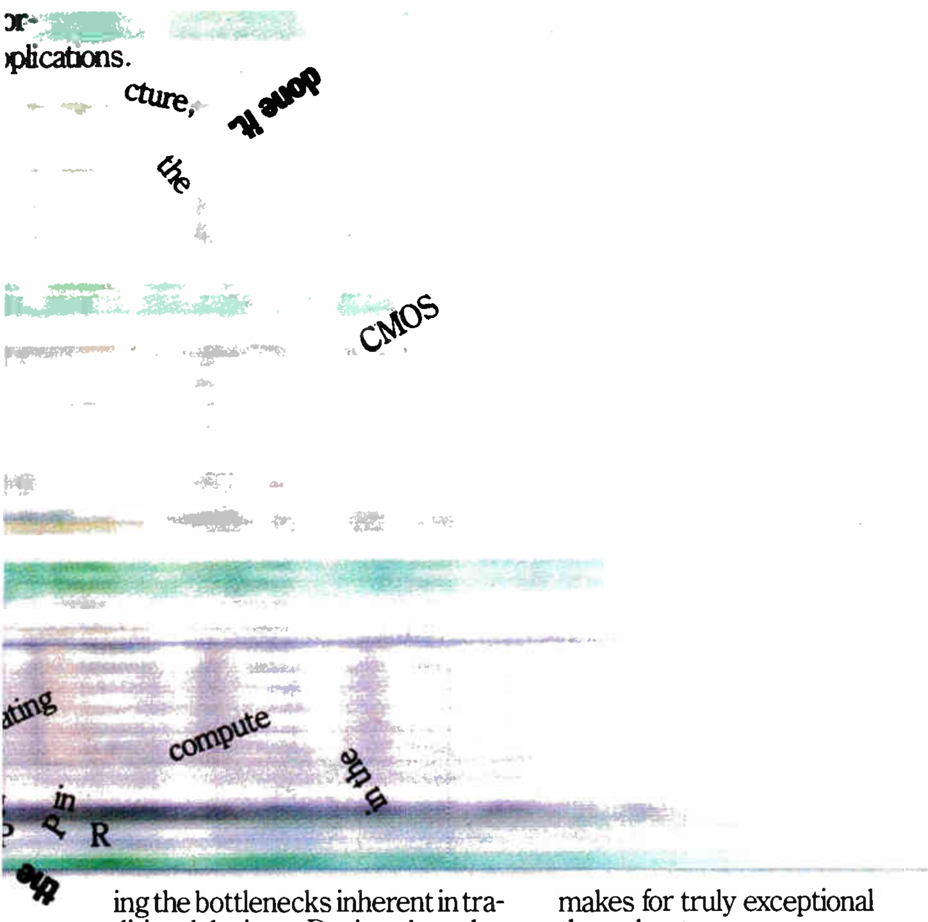
# Take a look at the fastest 32-bit microprocessor available.



# Well, it was here a second ago.

The ultimate goal of any computer system is performance. Whether it's for a high-performance workstation, a high-speed LAN, a telecommunications system, or any other advanced system.

That kind of high performance can only be achieved by eliminat-




ing the bottlenecks inherent in traditional designs. Designs based on outmoded architectures.

Today's designs need a microprocessor built from the ground up with brand new architecture. For today's brand new high-performance systems.

Which is where Fairchild's CLIPPER™ microprocessor comes in.

**CLIPPER means performance.**

CLIPPER is optimized for throughput. It provides system performance greater than a VAX™ 8600 – over five times that of a VAX 11/780 running VMS.™

CLIPPER features copy-back caching, which delivers a 15%-20% system performance improvement over other caching schemes. And a streamlined instruction set that combines the simplicity and performance of a hardwired CPU with a set of high-level instructions.

CLIPPER features highly pipelined processing. Which makes for truly exceptional throughput.

Its dual-bus architecture delivers up to 133M bytes/second to the CPU – roughly five times the bandwidth of traditional single-bus implementations.

An IEEE-standard Floating Point Unit is integrated onto the CPU to reduce communication overhead, and two mainframe-style 4K-byte caches provide memory access time as fast as one clock cycle.

**Good things really do come in small packages.**

CLIPPER's speed and performance weren't enough, however. We made it the most highly integrated solution in existence. And put it into a package that addresses the needs of today's designer like nothing else can.

On a small 3.0 x 4.5-inch module, we've combined a CPU, an on-chip FPU, two Memory Management Units, and a complete cache memory subsystem. And using just 8K bytes of cache memory, CLIPPER delivers performance that competitive designs need 128K bytes of cache to equal. Allowing CLIPPER to outperform board-level implementations that use over five *times* the board space.

**CLIPPER. It fits in practically anywhere.**

Because CLIPPER packs so much performance into such a small package, it can fit into places and applications other systems can't – on a desktop, in a portable package, you name it.

And it comes with all the support you need to make your product happen. Including a CLIPPER port based on the UNIX® System V operating system. Optimizing FORTRAN, C and Pascal compilers. Plus an assembler. Or you can choose a VAX cross-support package.

You'll also enjoy ongoing, expert advice from our applications engineers and systems designers, in every sales office and FAIRTECH™ Design Center.

For more information, call The Fairchild Customer Information Center, 1-800-554-4443.

**CLIPPER**

CLIPPER from Fairchild. It's fast becoming your only real choice.



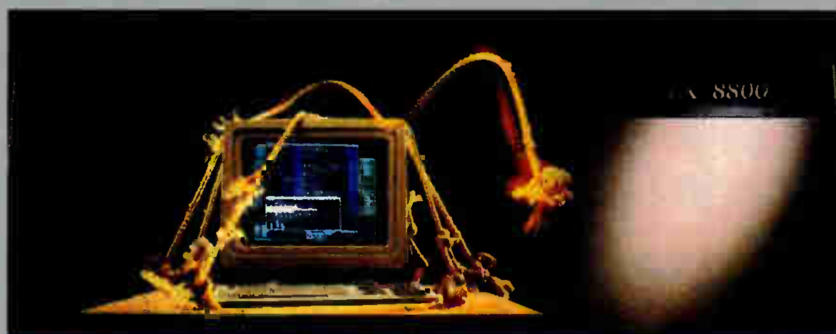
**We're taking the high ground.**

**FAIRCHILD**

A Schlumberger Company

Circle 27 on reader service card

# Digital has it now.



## The power to free up workstations from compute intensive tasks.

As every electronic engineer knows, there are some tasks no technical workstation can adequately handle. Design steps like logic simulation and design file verification are incredibly compute-intensive. Put them on a workstation and instead of working, you wind up waiting.

Now there's the VAX 8800™ system with mainframe power. It runs the same operating system, networking software and applications as our workstations. So a VAX 8800 can do all the time-consuming, number-crunching tasks, while the workstations concentrate on doing what they do best – delivering exceptional graphics at tremendous speeds.

For more information on the VAX 8800 system, write: Digital Equipment Corporation, 200 Baker Avenue, West Concord, Massachusetts 01742. Or call your local sales office.

digital™



Circle 28 on reader service card

Electronics

# IBM BRIDGING SCHEME ROILS THE LOCAL NET COMMUNITY

## IS BIG BLUE TRYING TO ISOLATE ITS TOKEN RING FROM OTHER LANs?

**DALLAS**

Bridges have suddenly become a burning issue for the local-area network industry. A fiery debate is raging over a controversial internetwork bridging scheme proposed by IBM Corp. Officials guiding the IEEE's 802 network committee are asking voting members to remain cool long enough to sort out the technical issues.

Angry opponents to IBM's proposal accuse the computer giant of trying to isolate its token-ring networks from Ethernet and token-bus LANs. They say the proposal introduces a source-routing scheme that's incompatible with bridging specifications that have already been set by the IEEE 802.1 internetworking subcommittee. Adding to their irritation is the belief that IBM may be trying to circumvent the 802.1 panel by adding source routing to the 802.5 token-ring specification.

Some Ethernet supporters have objected to letting the 802.5 subcommittee address the bridge issue, because they believe it is heavily under the influence of IBM. The 802 executive committee is attempting to set up an administrative structure—some support a special task force—to deal with IBM's proposal.

IBM executives in the Communication Products Division in Research Triangle Park, N. C., deny that the company is trying to undermine the 802.1 panel's work. Daniel Pitt, the designated standards-project authority for networks for IBM, says the company's proposal is based on technical considerations.

Pitt claims that token-ring systems are under severe time constraints when it comes to setting bits in address frames. He does not think that routing bits, which are needed to send data across multiple networks, can be set fast enough by a bridge that must determine addresses without help from the sending node. These route-setting nodes are called transparent bridges in the 802.1 specification.

Transparent bridges between LANs must make routing decisions and attach addresses to data crossing between nets. They generally store downloaded address tables, although some can learn addresses dynamically. Either way, IBM says the address-lookup times and associated costs of transparent bridges cause trouble for rings—troubles that will worsen in future 16-Mb/s rings.

At the heart of the bridge debate is where internetworking overhead will be located: in each attached computer, or in the bridge nodes tying LANs together. IBM has built its token-ring bridging system atop the connection-oriented data-link layer of the International Organization for Standardization reference networking model. IBM proposes to use Type-2 logical-link control, which performs some higher-level LAN services usually reserved for the network and transport layers of the ISO model.

Older standards for other LANs have been built on a simpler Type-1 logical link control without those higher-level services. Opponents to IBM's proposal complain that most of those networks would have to be modified to use source routing.

Networks based on collision-sensing multiple-access technology with collision detection, such as Ethernet, allow transparent bridges 60 μs or more to attach addresses, estimates Robert Donnan, a retired IBM staff member and chairman of the 802.5 subcommittee. "If you buffer incoming transmissions, you can increase the average time with CSMA/CD," he notes. "The transparent bridge appears the best for CSMA/CD."

But, he adds, bridges attached to 4-Mb/s token rings would slow the network if they have to set the most-significant bits of the source address, which is used as a frame-routing indicator. On a 16-Mb/s ring, a transparent bridge would have only 7 μs to set the bit.

The Type-2 logical link control and source routing enable IBM to maintain a LAN environment compatible with its Systems Network Architecture mainframe environment. "Like it or not, SNA is here and will probably stay for a long time. It will be necessary to do these

## SIGN UP HERE FOR TOKEN-RING RIGHTS

**Local-area network** vendors may be annoyed by royalty negotiations with the originator of the token-ring concept, but they're signing up nevertheless. Token-ring inventor Olof Soderblom, who settled a key license pact with IBM Corp. in 1980 and received a U. S. patent one year later, says about 17 agreements have been reached with LAN suppliers. Another 10 are nearing settlement, and Soderblom says his agents are now in contact with another 20 companies, which have either announced products or indicated interest in using token-ring technology.

But Soderblom says he has decided not to legally pursue the makers of token-ring chip sets. "It is impractical to license the token ring at the chip level," he says. That should come as good news to product managers for the TMS380 token-ring chip at Texas Instruments Inc. in Houston, who have been under the impression that TI was still negotiating with Soderblom. Still, TI's customers are faced with the royalty entanglement, adds Robert M. Metcalfe, chairman of 3Com Corp. The Mountain View, Calif., company is itself caught in the awkward position of shipping TMS380-based token-ring products without a license agreement.

OLOF SODERBLOM

"A lot of people are paying what seem to be extraordinary royalties," says Metcalfe, who believes the IEEE 802 committee should have insisted on public access to token-ring patents before making the IBM Token Ring a standard. "The IEEE knuckled under to IBM. Having threatening legal letters sent out [from Soderblom] to anyone who breathes a word of interest in token rings has got to be chilling." *–J. Robert Lineback*

# A LOW-COST, HIGH-SPEED VISION SYSTEM

**HORSHAM, UK**

A 10-year-old university research project has evolved into an affordable high-speed vision system that is attracting interest in many quarters, from industrial users to police departments to the U. S. Department of Defense. Called Clip, for cellular-logic image processor, the system uses a fine-grained parallel architecture that will process images up to 2,000 times faster than conventional, serial processors, according to its maker, Stonefield Systems plc.

Equally important, an extensive library of software has been developed for the machine. Clip comes with software for applications as diverse as fingerprint analysis, X-ray sorting, and aircraft identification. This is significant because only a handful of similar parallel image-processing systems have been built, and very little software for such machines exists.

Work on Clip dates back to 1976, when Michael Duff, now a professor at University College, London, started developing a large-scale parallel array processor. Seven years ago, his project culminated in a 96-by-96 array of 1-bit processors. "We believe this was the first one built in the world," says Bill Considine, Stonefield's managing director. Then Duff developed the system's software to the point where it has become viable as a commercial product, Stonefield believes. The Horsham company has licensed the Clip design from Duff and his university backers.

A 64-by-64-processor system can find one dropped stitch in a piece of textile in 0.1 s, a task that takes a DEC PDP-11/64 a full minute. When Clips with bigger processor arrays are built, they will do the job even faster, Stonefield says.

Few commercial parallel-processing engines have capabilities comparable to Clip's for the price. The Pixar Image Computer from Pixar, San Rafael, Calif., for example, has only four processors, so it is not a fine-grained, one-processor-per-pixel system like Clip. The Connection Machine from Thinking Machines Corp., Cambridge, Mass., could approximate Clip's capabilities—it contains 65,535 1-bit processors—but it is a $3 million general-purpose computer. Clip not only is designed for image processing, but is far less expensive. Stonefield expects most of its sales will consist of 32-by-32-processor systems, priced at about $142,000 each.

The processor array comprises a number of cards, each carrying processors for an array of 32 by 4 pixels. Usually, 32 bits or less of local image memory are associated with each processor. Extra image-store cards can extend this to up to 2,048 image planes.

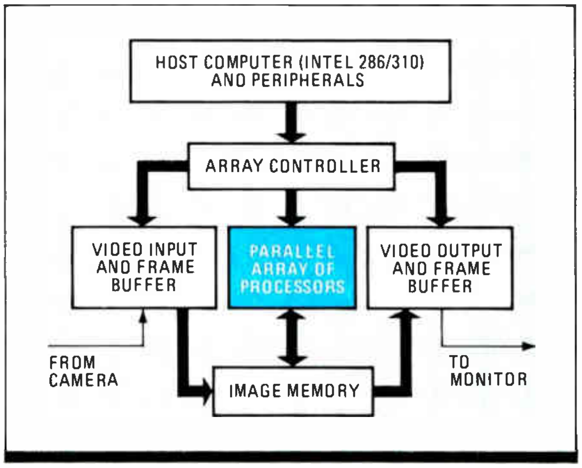



**IMAGE ENGINE.** Large arrays of 1-bit processors—32 by 32 and up—are the heart of Stonefield image-processing systems.

The system's video-input boards can take standard images from television-signal sources, charge-coupled-device or line-scan cameras, and satellite picture-data files. Video-output boards display the processed image on a monitor. The host computer is based on an Intel 286/310 system and runs under Xenix.

Clip's software lets it take small sections of a large, high-resolution picture and analyze it by sections. For example, a 32-by-32-processor Clip could analyze a 256-by-256-pixel picture in 64 sections.

A library of subroutines callable from the user's C-language program contains some 100 image-processing functions, including image enhancement using high-speed thresholding; feature enhancement and noise reduction; measurement of area, perimeter, and angles; and object recognition. Applications include pattern recognition, component inspection, surface inspection, target analysis, surveillance, seismological surveys, and X-ray classification.

From Stonefield's point of view, the most important applications will be industrial. The 13-year-old company specializes in industrial-control systems. "Machine vision has become a hot subject. People are building systems controlled entirely by robots," says Considine. "But there is little or no automation in the inspection systems," which is where Clip could be brought to bear.

Stonefield's beta-site applications include surface inspection of aerospace material, textile inspection, and checking of electronic components. The first production model, a 32-by-32-processor array, was delivered at the end of September to the U. S. Defense Department. The DOD has also ordered a 128-by-128-processor version. The Pentagon is believed to be experimenting with using Clip in aircraft-recognition systems.

*–Steve Rogerson*

GRAPHICS

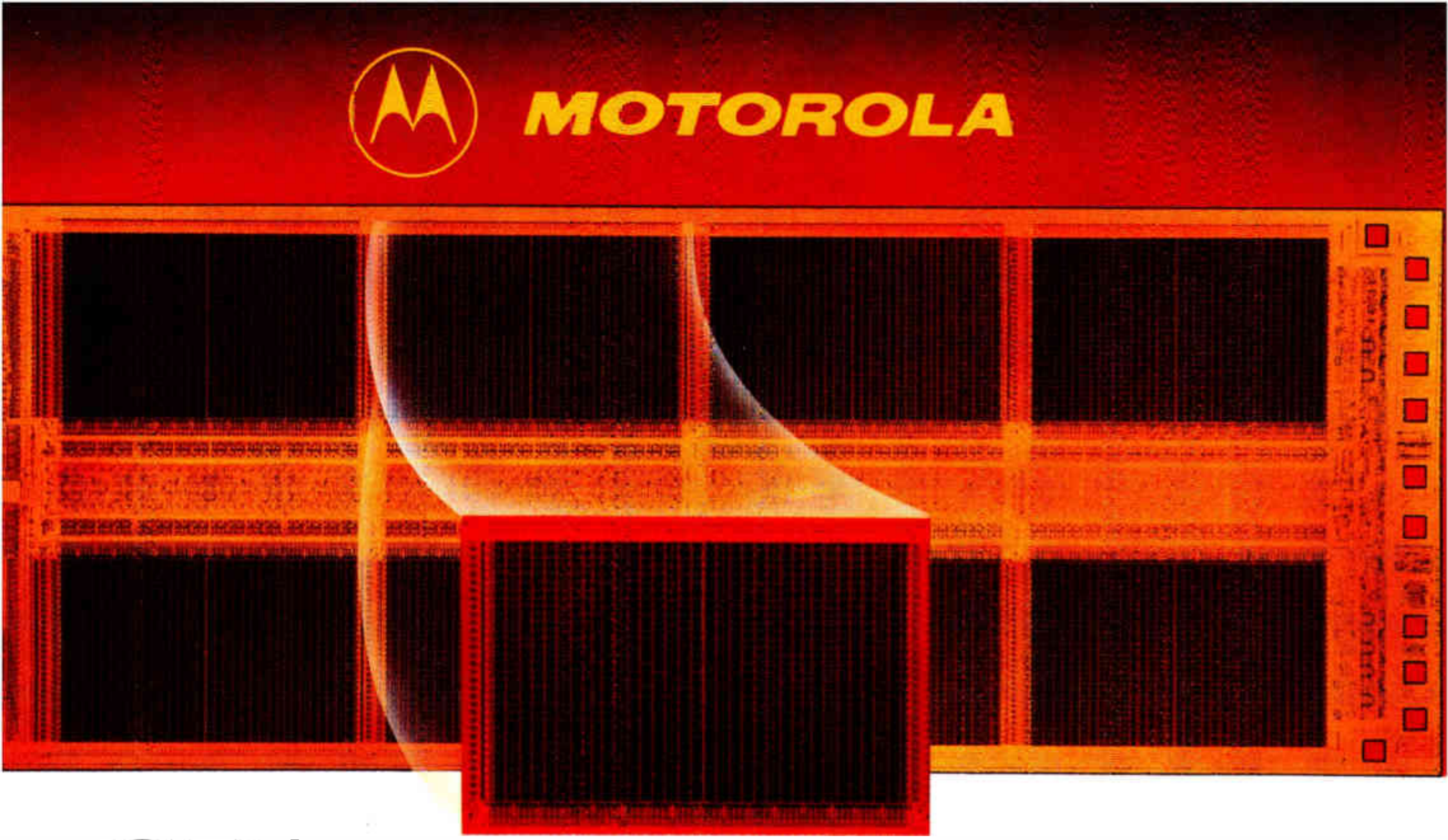
# IC ADDS HIGH-END GRAPHICS TO PERSONAL COMPUTERS

**SAN DIEGO**

The sophisticated color graphics that have helped make high-end work stations indispensable engineering tools are on the verge of spilling over into personal computers. The road to high-performance color graphics—which require video-data rates above 100 MHz and precise control of high-resolution bit-mapped displays—is being paved in large part by a single-chip back-end subsystem called a Ramdac.

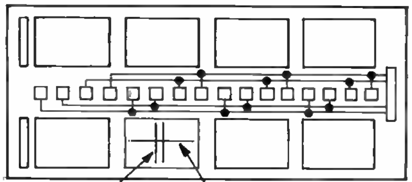
The Ramdac—a proprietary design of Brooktree Corp. that combines random-access memory with digital-to-analog converters—vastly simplifies the design of the analog and digital circuits that stand between a graphics system's frame-buffer memory and the color monitor. This has been the toughest part of a graphics system for digital-oriented engineers to design. Now, the appearance of a low-cost Ramdac will likely hasten the penetration of personal computers into desktop publishing and other markets driven by high-resolution graphics.

The 454's introduction signals an important new phase for graphics, says market consultant William I. Strauss of Forward Concepts Inc. in Tempe, Ariz. "It's the first round of sophisticated chips for personal-computer color graphics. Within six months, we'll see a lot more." The boom in desktop publishing is inspiring users to apply graphics in




# CMOS 64K SRAMs hit 25 ns.

## New Static family achieves faster speed and lower power with innovative architecture, proven process.




Unique design features provide both lower power and 25 ns speed for a new family of 64K and 16K CMOS Static RAMs available now from Motorola.

The MCM6287 is a 64K×1, the MCM6288 is a 16K×4 and the MCM6268 is organized in 4K×4.

### Rows vs. columns.

A reversal of the traditional Row-Column architecture runs the bit lines across the short dimension of arrays separated into 8K blocks.

The resultant bit lines are one-fourth the traditional length, significantly reducing resistance and capacitance for a tremendous speed increase. And, only one-eighth of the chip is powered up at a time, so power consumption is held to the absolute minimum.

### Patented power down boosts speed.

Another speed boost is achieved by a patented circuit which allows power down without any speed penalty. The result is that access from Chip Select is the same as from Address Valid—25 ns.

### Proven, volume technology.

Although these SRAMs are among the first to utilize double metal, they are fabricated in standard double poly, 1.5 micron CMOS. So it's a case of SRAM performance achieved through innovative design, produced in a proven process that's years along the experience curve.

### Motorola's newest fast Static RAMs

| Device | Organization | Speed (ns) | $I_{CCA}$ (mA) | Production |
|---|---|---|---|---|
| MCM6287 | 64K×1 | 25, 35 | 70, 60 | Now |
| MCM6288 | 16K×4 | 25, 35 | 90, 70 | Now |
| MCM6268 | 4K×4 | 25, 35 | 90, 70 | Now |
| MCM6164 | 8K×8 | 45, 55 | 90, 80 | Now |
| MCM6168 | 4K×4 | 45, 55 | 80 | Now |
| MCM2018 | 2K×8 | 35, 45 | 150 | Now |

### One-on-one design-in help.

Get an engineer-to-engineer update on designing-in these great Motorola SRAMs.

**1-800-521-6274**

Call toll-free any weekday, 8:00 a.m. to 4:30 p.m., MST, from anywhere in the U.S. or Canada. If the call can't cover your needs, we'll have a local engineer contact you.

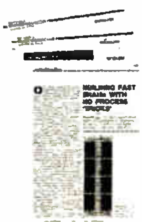
For information, send the coupon or write to Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

We're on your design-in team.

MOTOROLA

To: Motorola Semiconductor Products, Inc. P.O. Box 20912, Phoenix, AZ 85036
**Please send me more Motorola fast Static RAM information.**

302ELEX112786



Name ____________________

Title ____________________

Company ____________________

Address ____________________

City __________ State __________ Zip __________

Call me (______) ____________________

# More options for every design. Every mode. Everybody's need for practical solutions.

*AMP offers the widest range of cable assemblies, cables and products from board level to network level implementation.*

Circle 35 on reader service card

AMP and OPTIMATE are trademarks of AMP Incorporated

Now AMP makes it easier to design with fiber optics. And to bring fiber optics into practical application. With the broadest selection of single-mode and multimode interconnect products available anywhere.

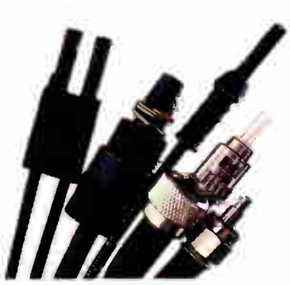
The newest? Our 2.5mm threaded or bayonet styles which offer high performance and intermate with current single-mode connectors.

Cable and cable assemblies. Connectors and splices. Active device mounts. Transmitters, receivers and transceivers. And the technology you need—board level to network level—to create and maintain your entire system.

And—as you might expect from AMP—all our interconnect products and application tooling are designed for simplicity, precision and speed. Just the practical help you need to put bright ideas to work.

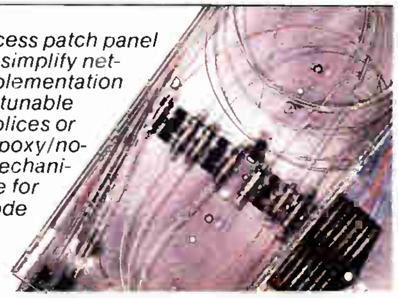
**Call (717) 780-4400 and ask for the AMP OPTIMATE Information Desk. Or write AMP Incorporated, Harrisburg, PA 17105-3608.**

**AMP Interconnecting ideas**



*Transmitters and receivers offer logic level compatibility at data rates from 25 Mb/s to 220 Mb/s. Available in either short or long wavelengths. Transceiver plugs into a standard RS-232 port for instant fiber optic capability.*

*Easy-access patch panel systems simplify network implementation with our tunable spring splices or our no-epoxy/no-polish mechanical splice for multi-mode use.*



ways they never thought of before, says Strauss.

Brooktree, of San Diego, introduced the first Ramdac last year. Called the Bt451, it is a monolithic CMOS device that operates at up to 125 MHz and replaces 20 to 30 parts, mostly expensive and power-hungry emitter-coupled-logic chips for multiplexing, interface logic, and control circuitry. The 451 has been snapped up by makers of high-resolution graphics gear, a large percentage of whom use it in their latest-generation hardware. But the 451's tab of about $100 per chip remains far too costly for personal-computer makers and suppliers of add-on graphics boards.

However, these vendors badly want sophisticated color graphics. Brooktree is accommodating them with a CMOS Ramdac that at 110 MHz runs almost as fast but costs only $40. The new Bt454, now being produced in sample quantities, supports fewer simultaneous colors, 17 from a palette of 4,096 colors, compared with 259 from a palette of the same size for the 451. But otherwise it retains most of the important features of the 451, notes Jeffrey R. Teza, director of product marketing.

Brooktree had been reluctant to develop a chip for the personal-computer market, preferring instead to devote more design energy to higher-performance Ramdacs. But potential users would not give up. "They pried it out of us," says Teza. "It's truly a market-driven part." The attraction, besides the price and functionality, is its architecture, which is pin-compatible with the 451.

A Ramdac provides circuitry for the fastest part of graphics: controlling the color monitor and refreshing the screen at the same time that the system's frame buffer is updated. The 454 chip carries a 16-by-12-bit bank of RAM used as a color palette, or color-lookup table, and three 4-bit DACs.

**DUAL-PORT RAM.** The Ramdac architecture supports a display of 1,280 by 1,024 pixels, with up to 4 bits of image data per pixel, plus another bit for overlay data. A special 1-by-12-bit overlay palette simplifies designing in cursor and screen-grid functions, solving what is said to have been a ticklish problem for graphics designers. Another of the 454's major advantages is that it has a dual-port color-palette RAM: there are separate paths for pixel and microprocessor data, so screen refreshing can continue while new palette selections are entered into the RAM.

The frame buffer interfaces with the 454 at up to 28 MHz through four TTL-compatible pixel-data input ports. Internal multiplexing of the pixel data allows the Ramdac to maintain the 110-MHz video-data rates that Teza says are needed for sophisticated color graphics.

Brooktree knows it could be poised to have its first chip to find a volume market, Teza says. The firm's other products address markets with volumes in the tens of thousands, far less than the potential of the personal-computer business. In addition to makers of graphics systems, several add-on personal-computer graphics-board suppliers are discussing buys of 50,000 devices and up. *–Larry Waller*

# SMART SCANNER READS ROUGH DRAWINGS

**MUNICH**

Coupling artificial-intelligence techniques with a scanning camera yields Siemens AG a setup that can enter even rough drawings into a computer-aided-design system. What's more, the high speed of the operation means that graphics can be entered in as little as 10% to 20% of the time required by conventional graphics-input techniques. The Siemens technique—so far unnamed—also considerably reduces the chances of human error during the input process, says Eckart Hundt, a laboratory manager at the West German company's Corporate Research Center in Munich.

The experimental setup developed by Hundt's team can take a rough sketch of a circuit diagram, drawn by hand without attention to detail, and reduce it to its symbolic elements. The lines don't have to be straight and precisely terminated, nor do the circuit symbols need to be drawn or oriented exactly in the diagram. Accompanying text, such as component designations and specifications, can be handwritten as well.

Siemens is demonstrating the technique for recognizing circuit diagrams, but the company says it is easy to load the system with symbols for other types of graphics, such as flow diagrams, construction drawings, or maps. The technique could replace keyboards, mice, and digitizing pads as input devices for computer graphics in such applications, Siemens says.

Conventional graphics-input methods rely on commands from a keyboard or a mouse. Entering them takes time, and so does the method in which a stylus is used to pick off the coordinate points of lines on a drawing placed on a tablet or pad. Not only are these methods slow, they are also subject to human error.

With the Siemens technique, human intervention is kept to a minimum. First, a charge-coupled-device camera scans the rough sketch—typically, a page measuring about 8½ by 11 in. The camera outputs a digital signal that is fed line by line to a computer and stored as a bit map in the computer's random-access memory.

The program that Hundt and his associate Gerd Maderlechner have devised runs on a Digital Equipment Corp. VAX computer. Using pattern-recognition methods, the computer separates the text from the graphics. If the text is machine-readable, such as hand-printed block letters and figures (but not script), the computer identifies each character in the text by means of optical character recognition, converts the characters into ASCII code, and stores the code in the same bank of RAM as the drawing data.

**HUNDT:** Cameras and AI software may replace conventional ways of entering drawings into CAD systems.

This memory has a typical capacity of 2,000 by 3,000 bits or pixels—sufficient for the amount of graphics and text that can fit on a letter-size sheet.

The program's main task is to transform the raster image into a symbolic description. It does this by breaking down the graphics into individual line elements and determining the coordinates of their ends.

Defining a line with just two coordinates results in a big reduction in data, which, Maderlechner points out, "significantly raises the technique's processing speed." The system also specifies the points at which lines branch off or join each other.

Next, the software determines whether the line elements repre-

## Burr-Brown came to Livingston for the workforce.

For Burr-Brown, the requirements for their European location were relatively straightforward.

A clean environment, modern facilities and direct transport and communication links with continental Europe.

They found all this in Livingston, Scotland.

A town purpose-built for new industries situated at the heart of one of the greatest concentrations of electronic companies in Europe.

And they found much more.

They found investment grants of up to 35%, rent-free periods plus European Community assistance. They found Kirkton Campus, a high-technology park ready-made to receive them.

And they found us.

A Development Corporation that could help them develop at every turn and a workforce that was both skilful and conscientious.

In Burr-Brown's words, one whose productivity was 'second to none in the world'.

A 20 minute drive down the M8 motorway and they're in Edinburgh. Scotland's capital city and a distinguished I.T. community that's home to no less than four Technology Transfer units.

Including Wolfson Micro electronics Limited and the Centre for Applications Software Technology.

Today, Burr-Brown is one of a long list of blue chip Livingston residents with firm plans for expansion.

A list that we can offer you every incentive to join.

To: C. Anne Robins, PO Box 345, Old Greenwich, CT 06870. Tel: (203) 629 3496.
Prove that Livingston is Europe's most logical location for my company. BLOCK LETTERS PLEASE.

Name ______________________

Position ______________________

Company ______________________

Address ______________________

______________________

______________________

Zip Code ______________________

Telephone ______________________

E11

**MAKE IT IN LIVINGSTON**

Europe's most logical location.

Circle 37 on reader service card

sent straight or curved lines. Through the use of AI concepts, the elements are compared with models stored in a symbol library, and the computer checks to see whether these elements represent simple lines or an arrangement of straight and curved lines that make up symbols for, say, resistors, diodes, or transistors.

**LOGICAL TEXT.** While this classification process takes place, the program determines where the connections should go—for example, from the emitter of one transistor to the base of another. After the graphics are completely resolved and diagnosed, the text portions of the page are inserted at the appropriate locations. For instance, a transistor designation and its value are placed next to the transistor to which they logically pertain.

After the Siemens software has analyzed a drawing, it generates a file that can be processed in the CAD system. The CAD system can then be used to print out a clean drawing, complete with symbols and all interconnection lines. It can also be used for making up, say, a components parts list and for numerical simulations of the circuit.

Of course, it is possible in some cases for a person to do a better job of reading and interpreting a relatively sloppy drawing than the machine can. If text overwrites a graphic symbol, for instance, the software will be foiled.

Hundt concedes that Siemens is not alone in pursuing this kind of work. Several Japanese companies, he says, have reported similar activities at technical meetings. But none of those schemes, he believes, are flexible enough to cope with rough sketches the way the Siemens technique can. *–John Gosch*

***PACKAGING***

# HYBRID INDUSTRY GETS A 'UNIVERSAL' SUBSTRATE

**TROY, MICH.**

Amorphous silicon is the basis of a radical departure in hybrid circuits: what amounts to a universal substrate with interconnections that can be programmed to suit the user's application. The new substrate comes from Mosaic Systems Inc., the Troy company that has been laboring for four years to produce wafer-scale circuitry.

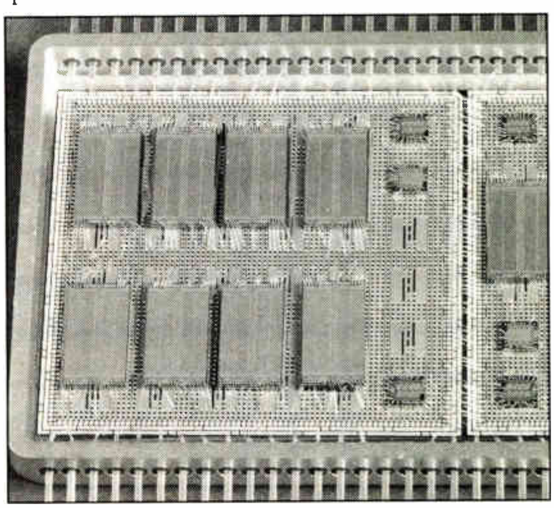
The new product line, called Unipro SCB for universally programmable silicon circuit board, does make use of wafer-scale techniques in the programmable interconnections. The company says Unipro SCB can dramatically shorten hybrid development cycles because users can simply adapt the programmable substrate rather than having to come up with an application-specific board to hold diced chips and other components.

Mosaic proposes to replace conventional fixed-connection, multilayer, ceramic hybrid boards with an off-the-shelf silicon substrate incorporating a built-in grid of metal lines and amorphous-silicon vias that can be programmed electrically for connecting surface-mounted, wire-bonded chips. Power and ground layers are included on the substrate.

The Unipro substrate eliminates the substrate-surface wiring used in conventional fixed-wire hybrids, while cutting hybrid development cycles down to three weeks from five months or more for complex multilayer ceramic circuits, Mosaic says. The method also allows chips to be packed up to 10 times denser than they are on conventional hybrids, the company says.

Mosaic is targeting both commercial and military markets with Unipro SCB. It has already made deliveries to Westinghouse Electric Corp. and is negotiating an order with General Electric Co.

One hybrid user impressed with the technology is Ted Bates, an avionics design specialist at Boeing Military Airplane Co., Wichita, Kan., who says he's always "looking for the point where technologies jump in a revolutionary way." Mosaic's method, he says, "looks like it could be one of those."



**DENSE.** One 1-in.-by-1-in. tile of this two-tile Mosaic Unipro hybrid carries eight memory chips.

Mosaic started up in 1982 with the goal of developing a true wafer-scale-integration technology. The company intended to use its programmable interconnection technology to overcome the complex discretionary-wiring problems associated with linking functional undiced chips on a wafer [*Electronics-Week*, Apr. 8, 1985, p. 25].

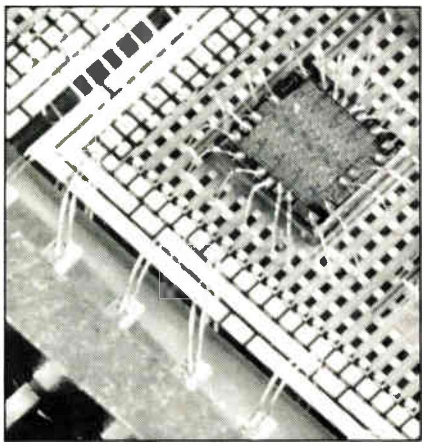
But the Unipro product line, at least initially, is aimed at the less ambitious hybrid approach. Mosaic is offering the line in two substrate sizes—one a 4-in. wafer, the other a downsized 1-in.-by-1-in. segment that can be tiled with other segments to build up larger substrates.

Mosaic will offer Unipro wafers and segments three ways. They will be available programmed to a customer's specifications or as completely assembled and tested hybrids. The company will also sell Unipro raw substrates that can be programmed and then tested by an end user or a hybrid manufacturer using modified programmable read-only-memory equipment. Mosaic is working with Data I/O Corp. of Redmond, Wash., to develop an interface board for IBM PC AT-based control of that process, says Albert A. Bogdan, Mosaic's director of marketing.

**VIA LINES TO GRID.** Each Unipro substrate incorporates a grid of metal lines, composed of layers of parallel lines. The layers are insulated from each other by a layer of amorphous, or noncrystalline, silicon. The substrates are programmed by applying a voltage at the appropriate paths, causing the insulating amorphous material where two lines cross to crystallize and become a conductive via. A large number of such vias connect the metal lines in a pattern that links the chips into one circuit.

The 1-in.-by-1-in. Unipro segments provide 101,061 programmable via points organized into 36 cells. Each cell can accommodate one small-scale integrated circuit. Larger chips cover more cells.

The greatest interest in the line so far is among defense contractors. The Wes-



**BONDED.** Connections to chips mounted on substrate are made with bonded wires.

# Du Pont delivers high-tech cable assemblies

## No one makes it easier than Du Pont to meet your high-performance cable assembly needs.

High-technology cable assemblies should deliver high signal speeds with low cross talk and excellent control of EMI, RFI, and ESD. They should not present quality, delivery, or performance problems.

That's why you should connect with Du Pont. And get computer-designed assemblies fabricated fast and backed fully.

You'll avoid the headaches of in-house designing, specifying components, receiving, managing inventories, assembling, and testing. And you'll have one source responsible for the entire project.

**Complete design flexibility.**

Du Pont's engineers use CAD and computer simulation programs plus cable and connector development facilities and model shops to create the designs you need. Or, we may be able to combine or adapt existing components that will be compatible with your needs. And, as an integral part of Du Pont Electronics, we can help solve material and other electronic technology problems.

**Responsiveness and responsibility.**

With 36 years of experience in terminals, moldings, plating, and connector assemblies, we have the know-how to deliver your prototypes in weeks, not months.

We manage every step from internal manufac-

**Berg Electronics is now**

# without high-tech headaches.

turing through outside purchases to maintain total quality and delivery control.

Du Pont responsiveness includes the economy of just-in-time deliveries or ship-to-stock programs.

**Total testing and economy.**

Every Du Pont cable assembly must pass many rigid inspections during fabrication plus a final performance test. Every one will perform to specs. And that's a promise.

Because we fabricate in volume for many OEM s, we can deliver high-performance cable assemblies at competitive prices—probably less than the cost of doing it yourself when you consider design and coordination time, supplies, fabricating equipment, and assembly.

**See our capabilities on videotape.**

If you have a current or future need for high-performance cable assemblies and you'd like to learn more about our capabilities, ask for a copy of our new videotape. Write on your company's letterhead to Du Pont Connector Systems, 515 Fishing Creek Road, New Cumberland, PA 17070, Attention: Systems and Assemblies Division. Or make the Du Pont Connection and call 800 233-1173 (in Pa., call 800 222-2194). See for yourself how to get high-tech cable assemblies without high-tech headaches.

**DU PONT CONNECTOR SYSTEMS**

DU PONT
REG. U.S. PAT. & TM. OFF.

Circle 41 on reader service card

tinghouse Defense and Electronics Center in Baltimore, for example, is testing assembled units supplied by Mosaic that pack 1.1 Mb of static random-access memory, using 24 chips on a 1-by-2-in. (two-segment) tiled substrate.

GE, likewise, is planning to use the Mosaic technology in a classified Strategic Defense Initiative application that requires high chip density and low mass, says Jules Ehland, a technical staff engineer at the firm's Space Systems Division in King of Prussia, Pa.

In 1,000-unit quantities, the unprogrammed segments will be offered at about $50 to $55 each, says Bogdan. The 4-in., wafer-sized substrates will carry 240 cells programmable through a total of 1,606,800 vias and will sell for $1,200 when preprogrammed by Mosaic.

Mosaic has licensed VLSI Technology Inc. of San Jose, Calif., as a second source of the wafers and the packages that use them. It also plans to sign up hybrid makers to do programming and assembly. *–Wesley R. Iversen*

# A SIMPLER WAY TO MOUNT HIGH-PIN-COUNT MODULES

**ROGERS, CONN.**

Making the connection between the several hundred pins of a multichip module or a pin-grid array package and a printed-circuit motherboard usually requires a very complex and costly socket or zero-insertion-force connector. An approach developed by Rogers Corp., though, offers an alternative: a much simpler and less expensive pinless grid array consisting of Z-shaped conductors that are inserted into a foam elastomer sheet, which in turn is compressed between the chip module and the motherboard.

The company, based in Rogers, Conn., says that its area-array connector provides not only a controlled contact force, but also contact wiping during compression. The resulting connections maintain low contact resistance, even when exposed to a wide range of environmental conditions, including vibration, relatively high temperatures, and humidity.

Rogers declines to make specific estimates of the cost savings provided by the area-array connector. But it points out that in addition to replacing a more expensive type of connector, the new scheme makes the motherboard itself less complex and less costly to make. No plated through-holes are required, nor is any connector soldering needed.

The new connector provides independent wiping action for each of its contact points, as well as low overall resistance. And nearly all of its design parameters can be varied independently, providing a wide range of solutions for connector design problems. For example, denser arrays are possible than the ones on 100-mil centers that Rogers has run through environmental tests. Arrays have been produced using 50-mil centers, and techniques are being developed for making higher densities.

Rogers has made connection sheets from both cellular urethane foam and silicone. The sheets are compressed between a board and a module—each having arrays of contact pads—to make positive contacts.

A foam-matrix elastomer was chosen over a solid one, because the foam does not displace the conductors when the matrix is compressed. The foam has a fine cell structure, which supports each conductor evenly, and a low level of relaxation under stress, which provides a low contact resistance that remains stable over time.

To develop a high-performance, high-reliability system, Rogers engineers had to select a conductor material with high conductivity, low contact resistance when mated to gold contact pads, and high corrosion resistance. They found that either gold- or nickel-clad copper wire with a rectangular cross section of 10 by 40 mils worked well. Lengths of the wire are formed into a Z shape and inserted into the elastomer sheets.

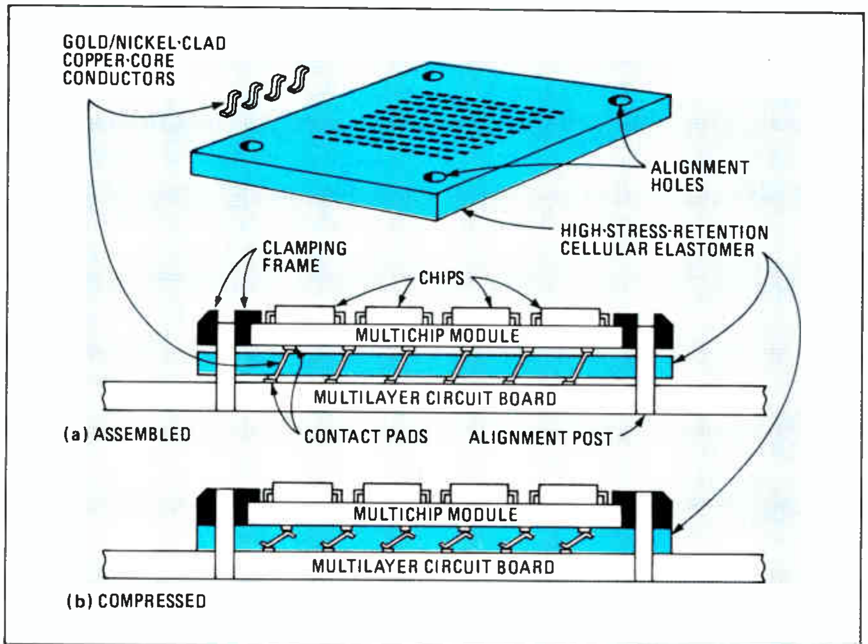
A prototype 400-pad connector with connectors on 100-mil centers has been built, and a 16-pad test unit has passed a battery of environmental tests, according to Scott Simpson, development supervisor at Rogers. After 20 days at 85°C and 100% relative humidity, contact resistance rose negligibly—from 3.3 to 3.7 mΩ—for a urethane-based connector. A similar silicone-based connector survived the same conditions for 40 days with no measurable degradation in contact resistance.

**CLAMPED TOGETHER.** The connectors can be used to mount a multichip module of ceramic, glass-epoxy, or other construction. An array of gold pads on the module's bottom side mate with the contacts in the elastomeric matrix, which in turn mates with the mother board. A clamping frame holds the assembly together.

Before assembly, alignment posts are mounted on the motherboard. The conductor-filled elastomeric sheet is placed on the circuit board, and the module is positioned atop that. Then the clamping mechanism compresses the sheet.

As the multichip module contacts the conductor surfaces, the conductors are rotated about their centers in the foam sheet. This rotation compresses the foam under the ends of each conductor to generate a contact force, while it also scrapes oxide layers from pads and conductors with wiping action—but the pressure is not sufficient to deform the conductors. The final position of the module on top precisely determines the amount of force generated at each contact; this directly corresponds to a known contact resistance.

Rogers can supply prototypes of the area array now. The company is initially aiming at arrays the size of current pin-grid arrays, or 144 pads. *–Jerry Lyman*




**SQUEEZE.** Rogers' elastomeric sheets are compressed to connect modules to pc boards.

# A complete list of things to know about 2400 bps modems.


Now that you've memorized that, here's a partial list of why a Hayes® Smartmodem 2400™ is best for you.

1. The Hayes Smartmodem 2400 allows you to communicate with the vast installed-base of 300, 1200 and 2400 bps "Hayes-compatible" modems. The Hayes Standard "AT" Command Set allows you to use Smartcom II® and other software that communicates.

2. Through synchronous/asynchronous technologies, the Smartmodem 2400 permits your PC to access mainframes, minis, and on-line services previously inaccessible through asynchronous-only modems.

3. The Hayes Smartmodem 2400 is efficient...it pays for itself in just 4 hours of annual use over long distance.

4. The technology of the Smartmodem 2400 allows you to transfer volumes of files with confidence across the city or across the ocean using Bell and CCITT standards.


5. The new Smartmodem 2400B™—a plug-in board for the IBM PC and compatibles—allows synchronous and asynchronous communication through the same Com port.

6. You will also get the Hayes standard 2-year limited warranty and the opportunity to extend the warranty to 4 years.

Best of all...you get Hayes. And that's all you ever really have to know!

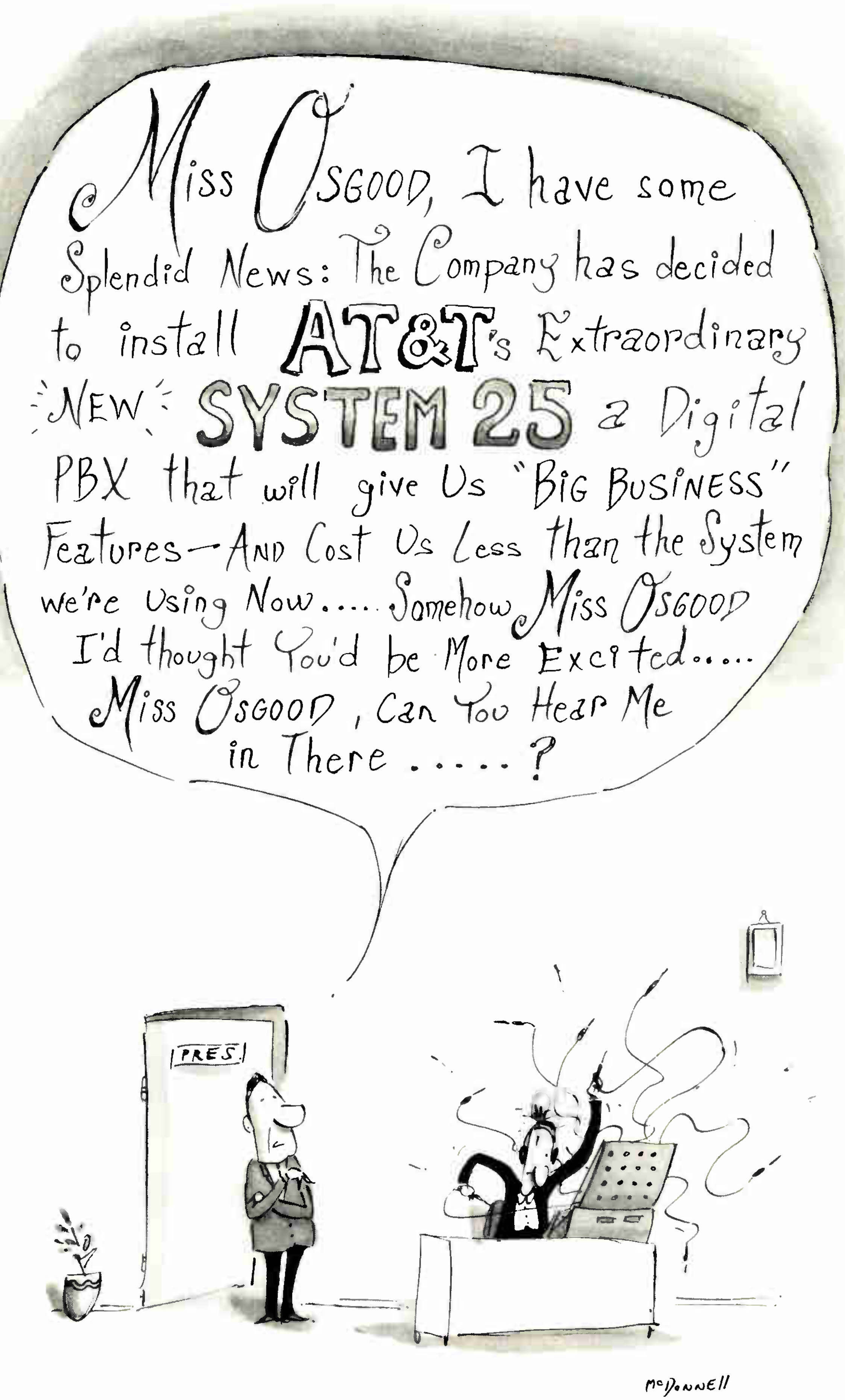
For more information or technical specs, contact your authorized Hayes dealer. Or Hayes directly at (404) 441-1617.

Hayes Microcomputer Products, Inc., P.O. Box 105203, Atlanta, Georgia 30348.

Hayes

Say yes to the future with Hayes.

Circle 43 on reader service card



Miss Osgood, I have some Splendid News: The Company has decided to install AT&T's Extraordinary NEW SYSTEM 25 a Digital PBX that will give Us "Big Business" Features—And Cost Us Less than the System we're Using Now..... Somehow Miss Osgood I'd thought You'd be More Excited..... Miss Osgood, Can You Hear Me in There .....?
PRES
McDONNELL

## Introducing AT&T's System 25, a state-of-the-art small PBX that can help the state of your business.

Not to mention the state of Miss Osgood.

System 25—from AT&T's Small Business Connection—is an instant solution to outmoded, over-the-hill equipment. It can give any company with 20-150 telephones the kind of special features once found only on "big business" systems. For instance, callers can reach everyone in your business without going through the receptionist. Its unique Personal Dial Code allows your calls to follow you around from office to office. And you can activate the code from any location on your route.

System 25's digital technology lets voice and data travel the same telephone lines. So you can add computers or other data equipment now or whenever the need arises.

What's more, it doesn't require special telephones. You can probably use the traditional telephones you have now. That makes System 25 perhaps the most cost-effective way to upgrade your phone system.

And it's cost-effective *after* you upgrade. For instance, System 25 sends all long-distance calls over the least expensive route. And keeps detailed records of those long-distance calls so you can charge clients or track expenses. But most important, you know your telephone investment is protected, because System 25 is from AT&T.

Plus, with System 25, Miss Osgood will have less work on her hands and a permanent smile on her face.

For more information about System 25, call 1 800 247-7000.

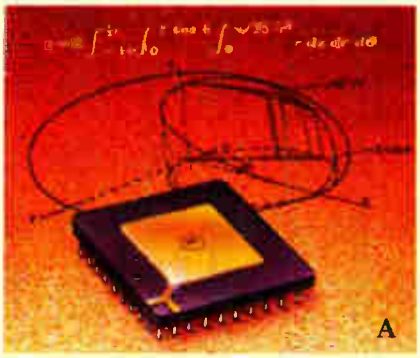
**AT&T's Small Business Connection / 1 800 247-7000**

This toll-free number connects you to the office in your area. In Hawaii call 1 808-946-2509.

**AT&T**

The right choice.

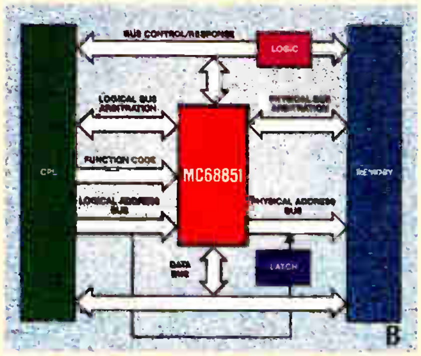
# Motorola M68000




## Floating point coprocessor has it all.

The MC68881 Floating Point Coprocessor serves M68000 Family and non-Motorola processors with a blend of complete conformance to the IEEE binary floating point standard (754), the four basic arithmetic functions, plus over 40 transcendental and non-transcendental functions including root values, trig functions, logs, exponentials and hyperbolics.

All functions are worked to 80 bits of precision in hardware, and it can break the million Whetstone performance mark.



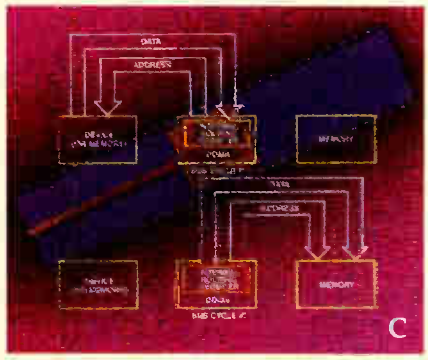

## Memory management support for virtual memory environments.

Memory management for M68000 Family processors is performed by the MC68851 Paged Memory Management Unit and MC68451 MMU.

The MC68851 supports a demand-paged virtual memory environment with the high-performance 32-bit MC68020 MPU.

On-chip address translation minimizes translation delays and maximizes system performance.

The MC68451 provides address translation, write protection and task access protection for MC68010-based systems.



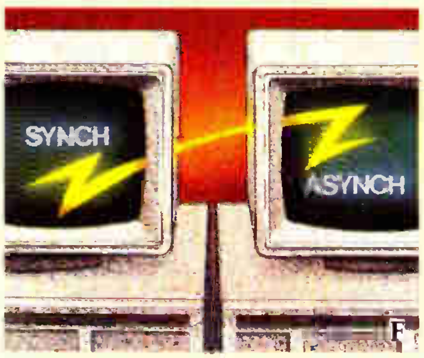

## DMA moves and manipulates data on multiple channels.

Three DMA Controllers of varied functionality serve the M68000 Family.

The MC68450 performs high-speed data movement and sophisticated data manipulation in complex systems. It's pin compatible with the MC68440 and '442.

The MC68440 moves blocks of data quickly and efficiently on two independent DMA channels. Channel switching and set up is also very fast.

The MC68442, with extra addressing for 32-bit MPUs, is an expanded version of the '68440.




## Versatile answers for the need to communicate data.

The MC68661 is a universal synchronous/asynchronous communications controller for M68000 and most other 8- and 16-bit MPUs. Receiver and transmitter are double-buffered for efficient full- and half-duplex operation. No system clock is used.

It can simultaneously convert parallel data from the MPU data bus to transmit-serial data and receive-serial data to parallel characters for MPU input.

The MC68652 is a single-channel serial data device that recognizes byte-control and bit-oriented protocols. It can operate at 2 Mbit/sec.


## General Purpose I/O interface supreme, with DUART, Multifunction Peripheral and Interface/Timer circuits.

The MC68681 DUART has two independent full-duplex synchronous receiver/transmitter channels for direct M68000 MPU bus interface.

Receiver data registers are quadruple buffered, and transmitter data registers are double buffered to assure minimum MPU intervention. Power for complex data communications is from multi-function 6-bit input and 8-bit output ports, a 16-bit programmable counter/timer, interrupt handling ability and a one-megabyte/sec. maximum transfer rate.

Our MC2681 is otherwise identical, but is without the M68000 bus interface.

The MC68901 multifunction circuit serves microcomputer requirements, via M68000 bus interface, with a single-channel UART for data communications. It has an 8-source interrupt controller, four 8-bit timers and eight parallel I/O lines.

The MC68230 is a programmable interface/timer with versatile double-buffered, unidirectional or bidirectional, parallel interfaces and an M68000 system timer. It also has the full M68000 bus interface.

# Peripherals Today


## $98 kit demonstrates the performance and versatility of the M68000 Family.

We put together the MC68000KIT and gave it the irresistibly low price of only $98 to make it easy and inexpensive for you to experience the performance and flexibility of the M68000 Family.

It has just what you need to create three basic M68000-based systems.

You get: Three MPUs • MC68000, the general-purpose standard for performance-intensive applications • MC68010 high-performance virtual memory MPU • MC68008, a cost effective 8-bit MPU with the 32-bit architecture of the '68000.

Six peripherals • for DMA control, the MC68440 provides two independent DMA channels • the MC68230 handles system timing and parallel I/O requirements • the MC68681, MC68661 and MC68652 are varied universal protocol circuits for communications designs • the jack-of-all-trades MC68901.

The kit also contains the documentation you'll want for converting the nine high-performance M68000 Family devices into superior basic systems of your own design.

The MC68000KIT is available only from authorized Motorola distributors, so contact the distributor of your choice and take advantage of this outstanding $98 value today.


## X.25 Protocol Controller.

Motorola's MC68605 implements level 2 of the 1984 CCITT X.25 Recommendation Link Access Procedure Balanced LAPB.

It independently supports full-duplex point-to-point serial communications up to 10 Mbps generating link level commands and responses. In transparent operation (monitor mode), frames are user-generated with the MC68605 providing HDLC framing and CRC checking/generation.

## One-on-one design-in help.

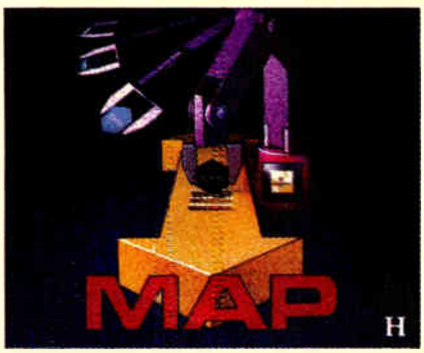
Get an engineer-to-engineer update on designing in Motorola's M68000 Family.

## 1-800-521-6274

Call toll-free any weekday, 8:00 a.m. to 4:30 p.m., MST. If the call can't cover your needs, we'll have a local applications engineer contact you.

We're on your design-in team.

MOTOROLA




## Chips for MAP Communications.

Motorola's MC68824 is the only single-chip implementation of the IEEE 802.4 Media Access Control sublayer of the ISO Data Link Layer specified by MAP, the GM Manufacturing Automation Protocol.

It supports serial data rates of 1, 5 and 10 Mbps, and relieves the host processor of frame-formatting and token-management functions.

The MC68184 Broadband Interface Controller completely implements the digital functions necessary for an IEEE 802.4 broadband modem as specified in MAP.


## Special literature packs supply product and application facts.

M68000 Family product literature has been assembled into three special assortments including brochures, technical summaries and data sheets, benchmark reports, application notes, technical articles, etc.

The M68KPAK is an M68000 Family overview, from chips and software to board- and system-level products.

The M32BITPAK focuses on our 32-bit products featuring the MC68020, with material specific to the subject.

The M68KCOMPAK is oriented to communications, including MAP, X.25, Bisynch, Asynch, etc.

**To: Motorola Semiconductor Products, Inc.**
**P.O. Box 20912, Phoenix, AZ 85036**

Please send me the following information on the M68000 Family.

- A ☐ Floating Point Coprocessor
- B ☐ Memory Management
- C ☐ DMA Control
- D ☐ Kit Brochure. Kits available from authorized Motorola distributors only. Contact yours.
- E ☐ X.25 Protocol Control
- F ☐ Communications Peripherals
- G ☐ General Purpose I/O
- H ☐ Manufacturing Automation Protocol (MAP)
- J Literature packs (one only) ☐ M68KPAK ☐ M32BITPAK ☐ M68KCOMPAK

Name ______________________

Title ______________________

Company ______________________

Address ______________________

City ____________ State ______ Zip ______

Call me (______) ______________________

303ELECS112786

# INTERNATIONAL NEWSLETTER

## SIEMENS AND BASF JOIN FORCES TO FIGHT IBM DOMINANCE IN EUROPE

West Germany's Siemens AG and BASF AG are teaming up to try to undermine IBM Corp.'s dominance in Europe, by forming a company that will sell Japanese-made IBM-compatible mainframes and peripherals. If the company achieves its sales goal of more than $500 million in the first year, with half of that outside West Germany, it would become Europe's largest vendor of IBM compatibles. Europe's installed base of medium- and large-size mainframes—those costing $250,000 and up—is $15 billion, with $8 billion of that representing IBM systems. Siemens, of Munich, brings to the venture its experience in large mainframes, made for it by Japan's Fujitsu Ltd. BASF, a Ludwigshafen company whose main business is chemical production, brings to the venture medium-size computers, made by Hitachi Ltd. of Japan, and peripherals from makers in the U. S. and elsewhere. The as-yet-unnamed company, to be based in Mannheim, will open Jan. 1. □

## TI, PHILIPS, AND EUROPEAN SILICON STRUCTURES SET ASIC EFFORT

European Silicon Structures is setting its sights on the high end of the continent's application-specific integrated-circuit market and is about to announce an agreement to develop standard cells with two heavyweights: Texas Instruments Ltd. of England and Philips International NV of the Netherlands. The year-old pan-European semiconductor company, based in Munich, is expected to announce details of the deal early next month. It will involve setting up a design house and a low-volume production house. TI and Philips already have a second-sourcing agreement dating from early 1985 on the firms' twin-well 3-$\mu$m CMOS processes; it was extended earlier this year to include 2-$\mu$m standard-cell technology. The ASIC business is one of the few European semiconductor markets not dominated by the U. S. or Japan. □

## ASCII CORP. WILL BE A VALUE-ADDED DISTRIBUTOR FOR TI CHIPS

Ascii Corp. has cut a deal that makes the Tokyo software house a value-added distributor of various products from Dallas-based Texas Instruments Inc.—among them, graphics-system processors, digital signal processors, and token-ring local-area-network chip sets using IBM protocols. Ascii expects to sell about $6 million to $9 million worth of TI products during the first year of the agreement, which will also permit the company to work closely with TI's design center to develop software for future devices; TI will then offer that software overseas. The deal is the latest in what has become a busy year for Ascii. So far, the company has ended a relationship with Microsoft Corp. of Bellevue, Wash., [*Electronics,* April 7, 1986, p. 11], and has agreed to form a chip-design partnership with Chips & Technologies Inc. of Milpitas, Calif. [*Electronics,* Sept. 4, 1986, p. 50]. □

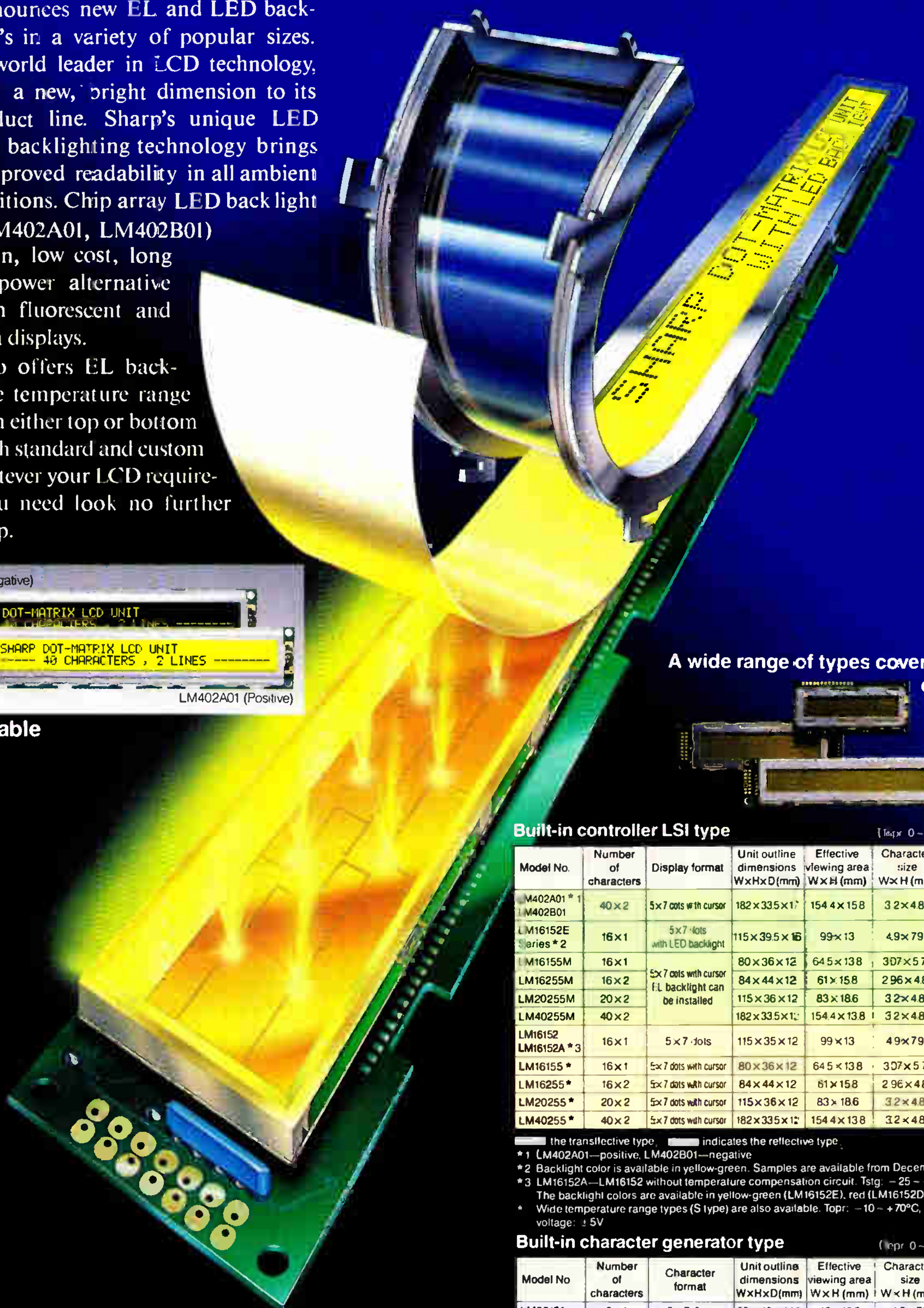
## NEW EUROPEAN SATELLITE WILL CATER TO BUSINESS SERVICES

The European Space Agency's Olympus satellite due to be launched in 1988 will feature high-data-rate business services—and teleconferencing over the $K_a$-band (30/20 GHz) will be one of the first. On behalf of the British National Space Centre, England's ESA representative, the Royal Signals and Radar Establishment has placed a $1.5 million order for an advanced $K_a$-band earth station to communicate with Olympus. The station, ordered from Marconi Defence Systems Ltd., will have a solid-state 20-GHz receiver using gallium arsenide high-electron-mobility transistors, a solid-state 30-GHz intermediate power amplifier, fully automatic computer-controlled remote-control facilities, and advanced digital modems with adaptive bit rates for fade countermeasures. The ESA will be the sales agency for Olympus services. □

# The new LCD from Sharp shows up

Sharp announces new EL and LED back-light LCD's in a variety of popular sizes. Sharp, a world leader in LCD technology, has added a new, bright dimension to its LCD product line. Sharp's unique LED chip array backlighting technology brings greatly improved readability in all ambient light conditions. Chip array LED back light LCD's (LM402A01, LM402B01) offer a thin, low cost, long life, low power alternative to vacuum fluorescent and gas plasma displays.

Sharp also offers EL back-light, wide temperature range LCD's with either top or bottom view in both standard and custom sizes. Whatever your LCD requirements, you need look no further than Sharp.




**Now available**

**A wide range of types covers a wide range of applications.**

## Built-in controller LSI type

(Topr 0 ~ +50°C, Tstg −25 ~ +70°C)

| Model No. | Number of characters | Display format | Unit outline dimensions WxHxD(mm) | Effective viewing area WxH (mm) | Character size WxH (mm) | Dot size WxH (mm) | Supply voltage (V) |
|---|---|---|---|---|---|---|---|
| LM402A01 *1 LM402B01 | 40×2 | 5x7 dots with cursor | 182×33.5×1? | 154.4×15.8 | 3.2×4.85 | 0.6×0.65 | −5, +12 |
| LM16152E Series *2 | 16×1 | 5x7 dots with LED backlight | 115×39.5×16 | 99×13 | 4.9×795 | 0.9×105 | +5 |
| LM16155M | 16×1 | 5x7 dots with cursor EL backlight can be installed | 80×36×12 | 64.5×13.8 | 307×575 | 0.55×0.75 | +5 |
| LM16255M | 16×2 | | 84×44×12 | 61×15.8 | 2.96×4.86 | 0.56×0.66 | +5 |
| LM20255M | 20×2 | | 115×36×12 | 83×18.6 | 3.2×4.85 | 0.6×0.65 | +5 |
| LM40255M | 40×2 | | 182×33.5×1? | 154.4×13.8 | 3.2×4.85 | 0.6×0.65 | +5 |
| LM16152 LM16152A *3 | 16×1 | 5×7 dots | 115×35×12 | 99×13 | 4.9×795 | 0.9×1.05 | +5 |
| LM16155 * | 16×1 | 5x7 dots with cursor | 80×36×12 | 64.5×13.8 | 307×5.73 | 0.55×0.75 | +5 |
| LM16255 * | 16×2 | 5x7 dots with cursor | 84×44×12 | 61×15.8 | 2.96×4.86 | 0.58×0.66 | +5 |
| LM20255 * | 20×2 | 5x7 dots with cursor | 115×36×12 | 83×18.6 | 3.2×4.85 | 0.6×0.65 | +5 |
| LM40255 * | 40×2 | 5x7 dots with cursor | 182×33.5×1? | 154.4×13.8 | 3.2×4.85 | 0.6×0.65 | +5 |

▭ the transflective type, ▬ indicates the reflective type.

*1 LM402A01—positive, LM402B01—negative

*2 Backlight color is available in yellow-green. Samples are available from December 1986.

*3 LM16152A—LM16152 without temperature compensation circuit. Tstg: −25 ~ +55°C
The backlight colors are available in yellow-green (LM16152E), red (LM16152D), and yellow (LM16152H).

* Wide temperature range types (S type) are also available. Topr: −10 ~ +70°C, Tstg: −40 ~ +80°C, Supply voltage: ±5V

## Built-in character generator type

(Topr 0 ~ +50°C, Tstg −25 ~ +55°C)

| Model No | Number of characters | Character format | Unit outline dimensions WxHxD(mm) | Effective viewing area WxH (mm) | Character size WxH (mm) | Dot size WxH (mm) | Supply voltage (V) |
|---|---|---|---|---|---|---|---|
| LM06151 | 6×1 | 5×7 dots | 60×40×14.5 | 45×13.5 | 4.8×75 | 0.8×09 | +5 |
| LM14151 | 14×1 | 5x7 dots with cursor | 93×47×13.5 | 53×11.2 | 2.65×3.75 | 0.45×0.45 | +5 |
| LM24151 | 24×1 | 5x7 dots with cursor | 174×51×13.5 | 115×11.2 | 3.3×5.05 | 0.5×0.55 | +5 |
| LM40151 | 40×1 | 5x7 dots with cursor | 177×46×13.5 | 120×9.6 | 2.32×3.28 | 0.4×0.4 | +5 |

## 7-Segment type

(Topr 0 ~ +50°C, Tstg −25 ~ +55°C)

| Model No. | Number of characters | Character format | Unit outline dimensions WxHxD(mm) | Effective viewing area WxH (mm) | Character size WxH (mm) | Supply voltage (V) | Power consumption (mW) |
|---|---|---|---|---|---|---|---|
| LM1610S2 | 16×1 | 7 segment | 80×36×15 | 61.6×11.6 | 2.7×5.5 | +5 | 3 |
| LM1610SE Series *1 | 16×1 | 7 segment with LED backlight | 80×36×17 | 61.6×11.6 | 2.7×5.5 | +5 | *2 |

*1 The backlight colors are available in yellow-green (LM1610SE), red (LM1610SD) and yellow (LM1610SH).

*2 3mW with backlight OFF, 503mW with backlight ON (LM1610SE, LM1610SD), 303mW with backlight ON (LM1610SH)

**SHARP**

**SHARP CORPORATION, JAPAN**

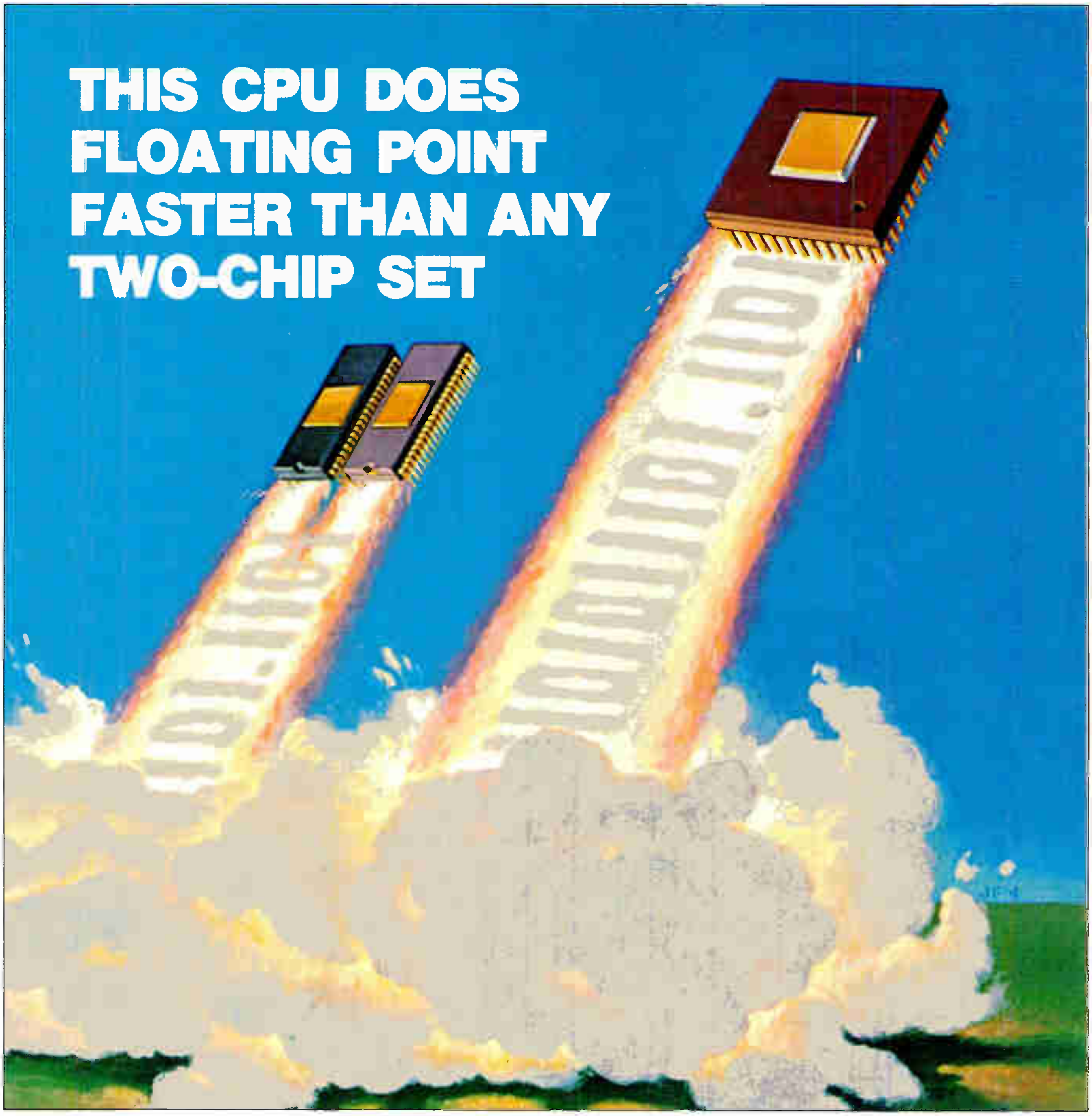
**SHARP CORPORATION** Electronic Components Group International Sales Dept.
22-22, Nagaike-cho, Abeno-ku, Osaka 545, JAPAN
Tel:(06)621-1221 Cable.LABOMET OSAKA Telex J63428 Attn.OSKPA(LABOMET A B)

**U.S.A.:SHARP ELECTRONICS CORPORATION** Electronic Components Division.
Sharp Plaza, Mahwah, New Jersey 07430-2135 U.S.A. Tel 201-529 8757 Telex 426903(SHARPAM PARA)

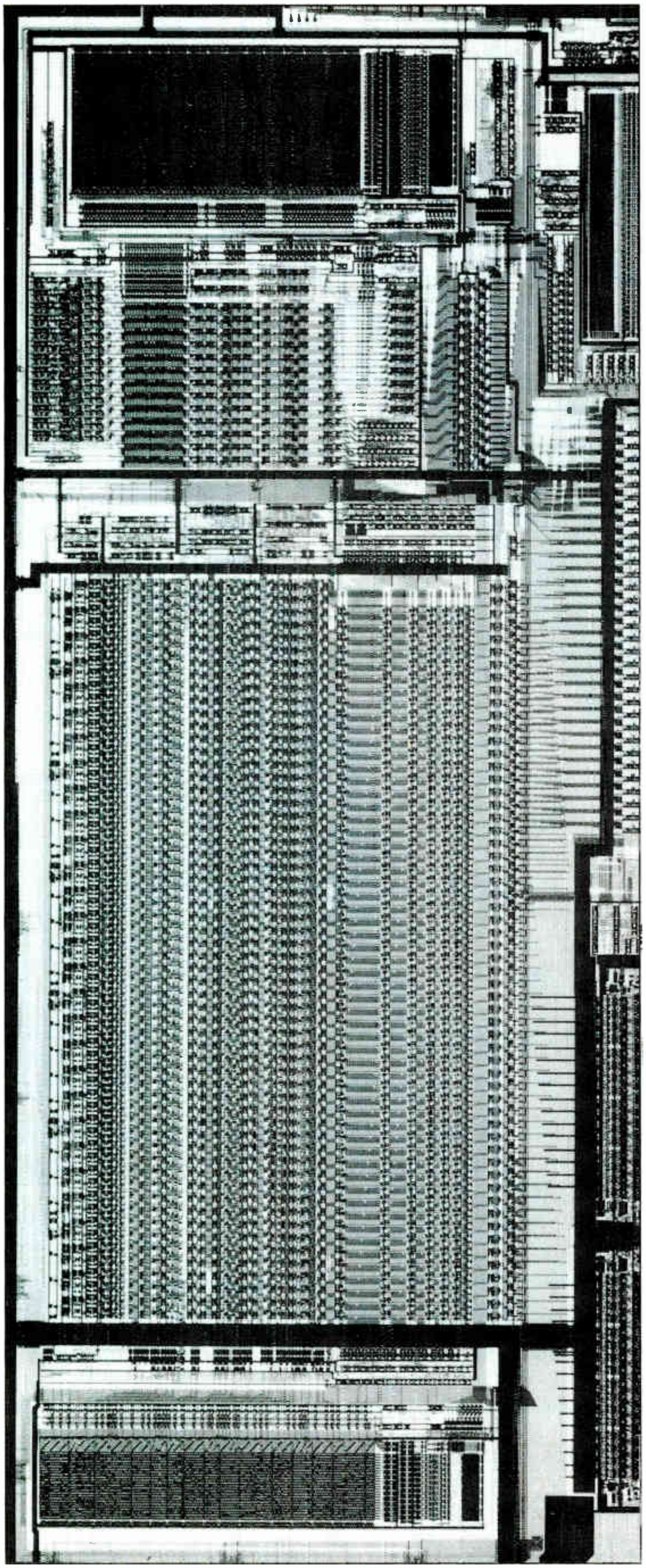
**EUROPE:SHARP ELECTRONICS(EUROPE)GmbH** Electronic Components Dept.
Sonninstraße 3,2000 Hamburg 1, F.R. Germany Tel (040)23/75 0 Telex 2161867(HEEG D)

Circle 50 on reader service card

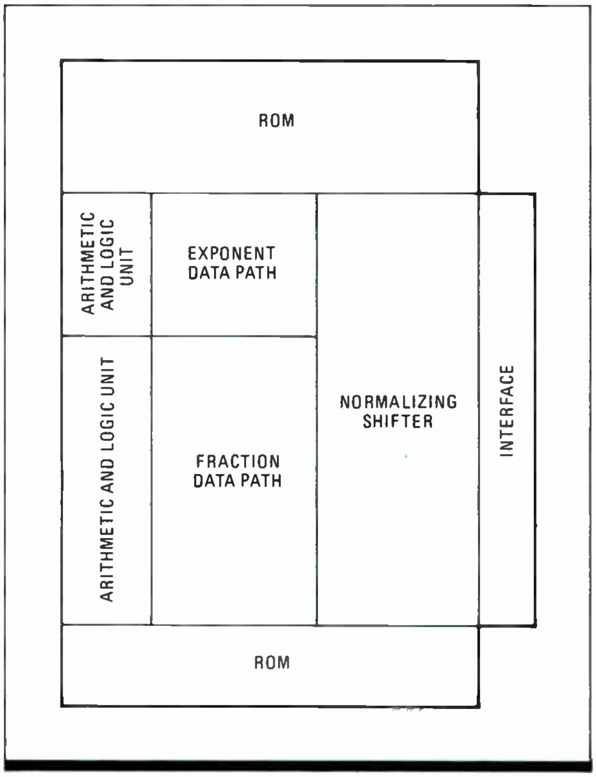
# INSIDE TECHNOLOGY




*Four million single-precision Whetstone instructions per second—that's the awesome speed of the new T800 floating-point version of Inmos Corp.'s single-chip transputer. Inmos took its 32-bit T414 microprocessor and incorporated onto it a*



**1. COMPACT FPU.** Inmos uses a 1.4-$\mu$m CMOS process and splits the ROM into two blocks to fit a floating-point unit onto the 9-by-1[illegible]-mil T800 transputer.




**2. FRESH APPROACH.** Inmos rethought the architecture of the FPU and squeezed it into 25% of the T800's area.

floating-point unit to achieve speeds never before reached by a single chip. Three key elements make the T800 possible, says David May, transputer design manager for the Bristol, UK company. They are a 1.4-$\mu$m CMOS process, an FPU with a multiplier and shift mechanism tailored for single-chip integration, and a three-bus architecture designed to let the FPU operate concurrently with the central processing unit.

Such speeds are 4 to 12 times faster than current combinations of 32-bit central processing units and their floating-point coprocessors, says May. The chip's blinding speed, he says, is equaled only by special multichip implementations incorporating combinations of a stand-alone floating-point processor and a multiplier. Most other implementations that are capable of such speeds, he adds, must include either a specially designed interface chip or miscellaneous interface logic in addition to the multiplier and the floating-point processor. And multichip solutions require external memory, with consequent interchip delays—while the T800 has 4-K of static random-access memory on board.

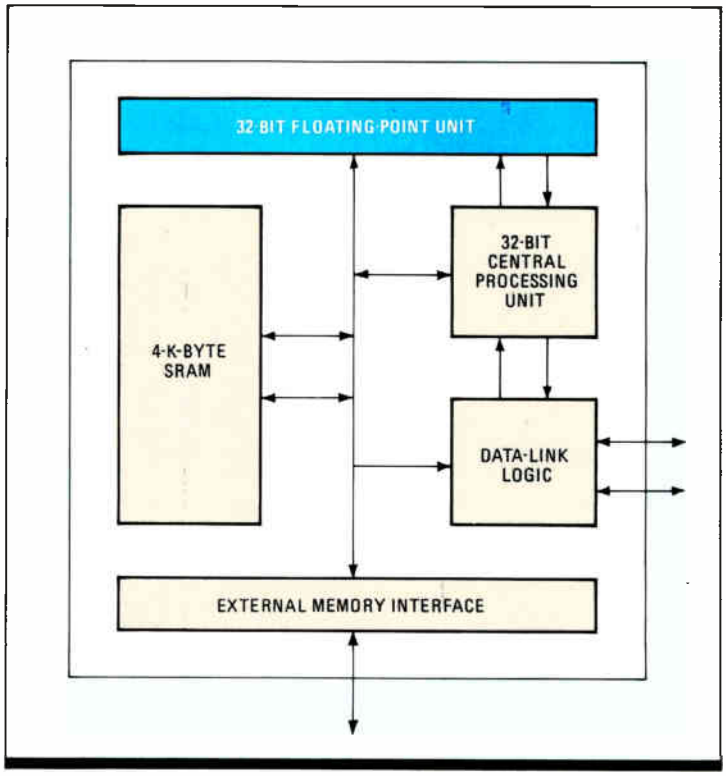
Measured at 4 million Whetstones/s, the T800, May says, is more than 12 times faster than an Intel 80386 and its coprocessor, the 80287, and has six times the performance of a Motorola 68020/68881 combination. It's also got four times the speed of a National Semiconductor 32032 and its 32100 floating-point coprocessor and about twice the speed of the next-generation Motorola 68030 and its coprocessor, the 68882. According to May, the only combination of chips that can compare in floating-point throughput are four-chip combinations of industry-standard 32-bit CPUs, a special customized interface chip, and the Weitek two-chip floating-point chip set, the 1164 and 1165.

The T800 is being developed as part of the European Esprit parallel-computer-architecture project. It is intended as part of a proposed supercomputer constructed from a reconfigurable collection of transputer elements. May also is enthusiastic about the potential of the new chip in the marketplace against the various multichip solutions. In fact, Meiko Ltd., a Bristol company founded by several former Inmos employees, announced a T800-based supercomputer called the Computing Surface at the same time as Inmos announced its new chip (see p. 56).

"Virtually every significant application for 32-bit CPUs also requires some degree of floating-point processing capability—mostly more, not less," says May. "It is much like the demand for memory; as the cost per bit dropped, users' demands became voracious." A similar situation will occur in floating-point processing, May adds, as semiconductor vendors find ways to increase the number of floating-point operations per second for each square centimeter of chip surface. "Virtually the only way to condense essentially megaflops of performance into a few square centimeters will be with the T800," he says. He believes that the T800 will be the chip that finally breaks the transputer out of the pack, pushing it into a leading position, competitive with the more mainstream 32-bit processors.

Set for early 1987 release, the new 84-pin, 300,000-transistor dual FPU/CPU processor uses a 1.4-$\mu$m single-level polysilicon CMOS process (0.8 $\mu$m effective channel length) to achieve the dizzying speeds in a chip that is only 25% larger than the T414. Into the 11-by-9-mil chip area of the T800, Inmos designers have incorporated not only the complete CPU structure of the T414 [*Electronics*, Nov. 17, 1983, p. 109], but also the full-function floating-point processor (Fig. 1) and multiply and divide logic. In addition to the standard instructions available on the T414, the new floating-point transputer also incorporates instructions for such standard floating-point operations as addition, subtraction, multiplication, and division, plus new ones for loading, operating on, and storing from floating-point register stacks. It also includes instructions for color graphics, pattern recognition, and error-correcting codes.

May and his design team took a fresh approach to the structure of the FPU (Fig. 2) and how it would be incorporated onto the chip with the CPU. "The basic drawback to many of the present floating-point coprocessors and chip sets is that they are monolithic versions of circuit solutions developed when the technology was still at the small- and medium-scale-integration levels," says May. "What is required is a good look at floating-point calculations and how the silicon can be optimized, through clever circuit design, to perform the functions critical to fast and accurate operation."

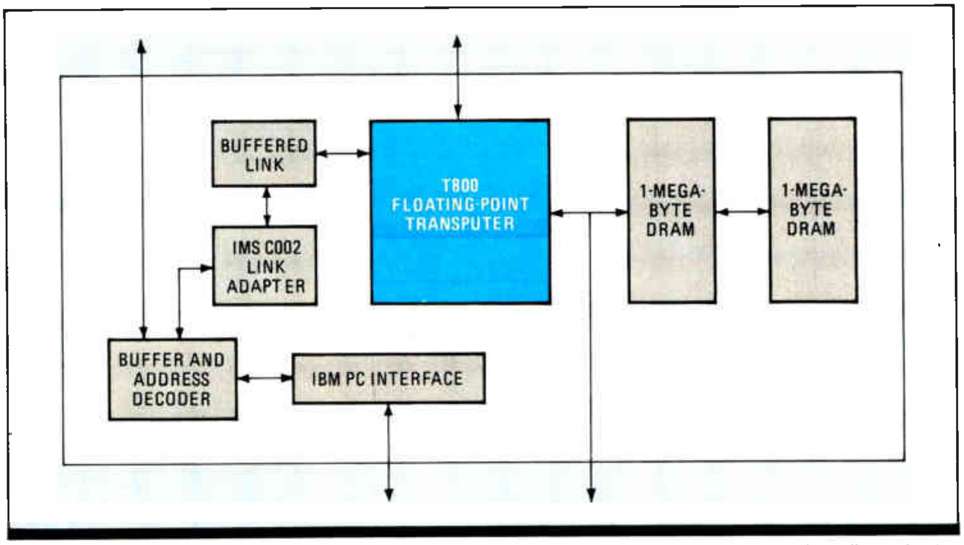



**3. CONCURRENT DESIGN.** The T800's floating-point and central-processing units are tightly coupled for concurrent operation.

After months of detailed analysis, says May, it became clear that some of the traditional building blocks of floating-point system design—particularly flash, or parallel, multipliers and barrel and funnel shifters—were inadequate. "In most traditional designs it is a matter of either overkill, or missing the mark altogether," he says.

*Inmos is betting that most users of 32-bit microprocessors are going to demand floating-point capability, and that they'll welcome the T800 single-chip implementation*

For example, while incorporating a flash multiplier on chip would result in a significant improvement in performance, it would result in a die area about twice that of a complete microprocessor CPU. "As it turns out, a flash multiplier operates much more quickly than is necessary for most floating-point calculations," May notes. "This is because useful floating-point calculation involves more operand accesses than operations." In a typical floating-point benchmark, it might be necessary to load three operands, perform two operations, and store the results. "If it takes half a microsecond to access an operand,




**4. TRY IT OUT.** An evaluation board for the IBM PC combines the T800 with a link adapter and dynamic RAM to allow users to see for themselves the speed of the new chip.

the calculation will still take at least 2 μs, even if the operations take no time at all," he reasons.

So, instead of an extremely large parallel multiplier, Inmos designers have opted for a slower but less silicon- and power-hungry serial pipelined logic structure dedicated to multiplication and division. While inherently slower than a flash multiplier, this approach, says May, has the advantage of being sufficiently small enough to be incorporated onto the chip, thus eliminating the multichip solution's chip-to-chip delay, which slows down the rate at which operands can be transferred to and from the FPU.

Just as important a consideration as the multiplier, May says, is the implementation of the shift function of the floating-point processor.

*The 1.4-μm CMOS process was part of the designers' campaign to shrink the size of the FPU; they also rethought the structure of the multiplier, the shifter, and the ROM*

"When implementing IEEE arithmetic, it is often necessary to perform long shifts on every floating-point operation. Unless a fast shifter can be incorporated into the floating-point unit, the maximum operation time can become very long."

So, rather than incorporating a traditional barrel or funnel shifter, Inmos engineers have come up with a proprietary shifter design that is optimized for normalization—one of the most critical and time-consuming aspects of a floating-point calculation. Normalization is used as a means of referencing a number to a fixed-radix point. Commonly used in fixed-to-floating-point conversion and division, normalization is usually provided for in microcode. Incorporating this function into the chip logic results in an extremely fast shifter that can perform a shift in a single 20-MHz clock cycle and a normalization in no more than two cycles. That's an order of magnitude quicker than traditional implementations.

Additional speed improvement is obtained by slightly modifying the basic structure to incorporate a 2-bit shift algorithm into the FPU data path, rather than the traditional 1-bit implementation. In this approach, two numbers are presented serially to the circuit. The partial product is evaluated for every bit of the multiplier, and a serial addition is performed, with the partial additions being stored in a register. The 1-bit shift required for each partial product is performed automatically. Incorporating 2-bit shift elements, says May, does not increase chip area substantially. In exchange, there is almost a twofold improvement in performance, with a single-precision divide time of 950 ns and 1.7 μs for double precision.

The register and shift logic necessary for arithmetic operations such as multiply and divide are incorporated into a two-level data path. The fraction mantissa data path is 58 bits wide, and the exponent data path is 13 bits wide. The normalizing shifter interfaces both the fraction data path and the exponent data path. As a result, data to be shifted comes from the first, while the magnitude of the shift is associated with values located in the exponent data path.

To squeeze the FPU block into as little silicon as possible, the read-only memory containing the floating-point instruction microcode was split into two parts. "Although physically split into two arrays, each is part of the same logical ROM," says May. "This configuration has two benefits. First, control signals do not have to be bused through the data paths, which reduces interconnect length and thus overall delay time. Second, the FPU area is reduced, since the ultimate size of the block is not dependent on the size of one large array, but on the geometries associated with two smaller ones."

The T800 uses a slight modification of the T414's bus structure (Fig. 3) to permit the FPU to operate concurrently with the CPU. A common bidirectional 32-bit address and data bus is used to allow both the CPU and FPU to access internal and external memory. This main bus is also used by the FPU on the few occasions it must access the CPU and for sending the results of its calculations through the data link to the outside world. A separate unidirectional bus is used by the CPU to access the data link. A third bus is used by the CPU to send control instructions to the FPU and receive status information in return.

This concurrent architecture means that the FPU and CPU operate essentially independent of each other; address calculations can be performed in the CPU at the same time the FPU is doing a floating-point calculation. "This can lead to significant improvements in applications that access arrays heavily, such as in array processors used in supercomputers, signal processing, image processing, and many graphics tasks in high-end scientific and engineering work stations," says May.

Critical to the concurrent operation of the T800's CPU and FPU is the depth of the register stacks in each block. May notes that floating-point expressions commonly have embedded address calculations, as the operands of floating-point operators are often elements of one- or two-dimensional arrays. "The CPU stack has been designed to be deep enough to allow most integer operations and address calculations to be performed in it," he says. "Similarly, the depth of the FPU stack allows most floating-point expressions to be evaluated within it, employing the CPU stack to form addresses for the operands."

In terms of raw speed and throughput, the T800 compares well with many multichip solutions. For example, the T800's operation time on standard single-precision IEEE 754 floating-point numbers is typically in the submicrosecond range: 350 ns for an add or a subtract, 850 ns for a multiply, and 950 ns for a divide—comparable to many multichip implementations.

In a T800-based evaluation board designed for use in an IBM Personal Computer or compatible machine (Fig. 4), typical floating-point benchmark programs required only 2 to 3 seconds, versus 28 to 30 seconds on a similar board using the T414 transputer and 135 seconds using an Intel 80287 floating-point coprocessor.

However, says May, it is by the traditional floating-point benchmark—the Whetstone—that the power of the T800 is most apparent. The Whetstone benchmark reflects a typical scientific or engineering program because it includes procedure calls, array indexing, and transcendental operations, as well as a good mix of floating-point operations. And a chip that can do 4 million single-precision Whetstone instructions per second is a good candidate for scientific and engineering tasks. □

---

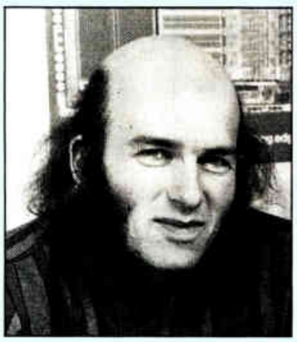
TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

## 'THE FLOATING-POINT NICHE IS NOW THE MAINSTREAM,' SAYS MAY

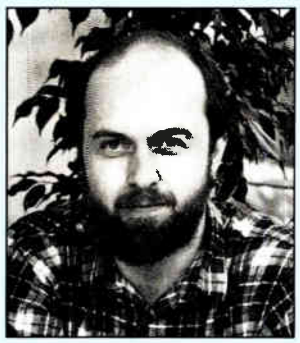
**Floating-point operations** are becoming commonplace tasks for microprocessors, says David May, manager of product architecture at Inmos Ltd. And that's why he thinks the T800 floating-point transputer is going to get a rousing reception. May, 35, sees a growing convergence of general-purpose central-processor-unit architectures and such special-purpose applications as floating-point processing. "The niche is now the mainstream," he says.

"Initially, many microprocessor manufacturers considered floating-point as ancillary to the main thrust of their 32-bit product line," May says. "And while it was important to offer such features in the form of a coprocessor, the market was not [thought to be] significant enough to support the development of a processor that combines both capabilities into a single chip."

It is now increasingly clear to many, he says, that virtually every significant market for general-purpose 32-bit CPUs will also require a high degree of floating-point processing capability. For Inmos, he says, this realization came soon after the introduction of its original 32-bit transputer, the T414. While primitive in comparison to the T800, the T414 incorporated enough floating-point capability to perform at a rate of 647,000 single-precision Whetstone operations per second, he says.



DAVID MAY



TONY FUGE

Response to that performance was such that the Bristol, UK, company began work two years ago on the T800. For the first year, says May, most of the effort was an informal exchange of ideas between himself, 32-year-old transputer design manager Tony Fuge, and others on the team.

Once the rough outline of the T800 was defined, Fuge, May and a 10-person design team set to work and turned out a final design in less than 12 months. The result, says May, is a combined CPU/FPU architecture that he believes will be the prototype of similar offerings from other manufacturers.

A 1972 Cambridge University graduate with degrees in mathematics and computer science, May was involved in basic research in artificial intelligence and concurrent programming at Warwick University, Warwick, UK, before joining Inmos in 1979 to begin development on Inmos' original T414 transputer.

Fuge graduated in 1974 from Bristol Polytechnical Institute. He then joined Fairchild Camera and Instrument Company Ltd.—also in Bristol—where he was involved in development of the company's IsoCMOS and CMOS Macrologic and bipolar FAST product lines. Fuge started work at Inmos in 1980 as a MOS design engineer. He was named manager of the transputer design effort in 1984.

# HOW MEIKO IS GETTING AN INSTANT SUPERCOMPUTER

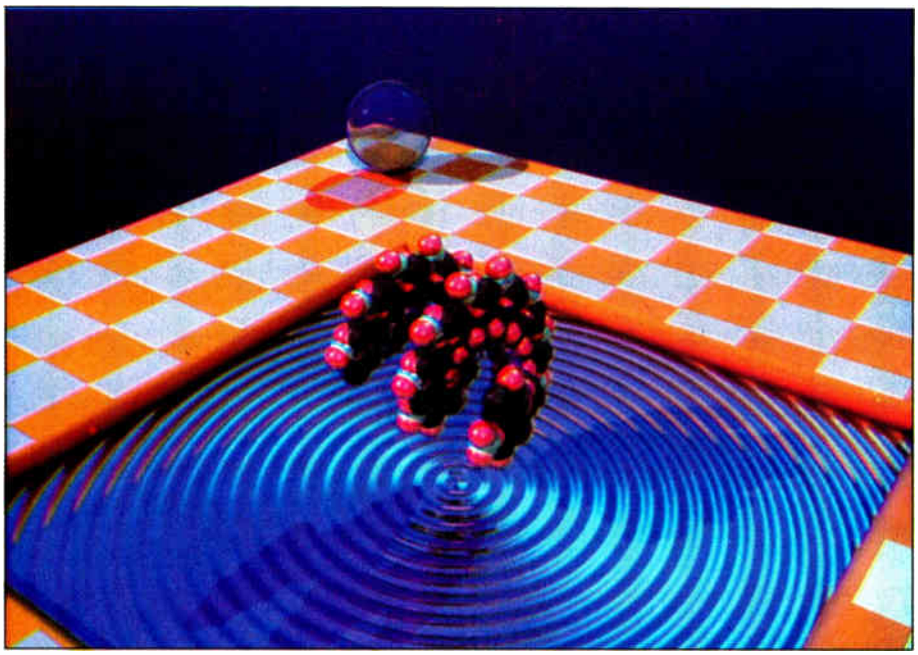
*The British company will use 311 of the new Inmos T800 transputer chips to boost the speed of its Computing Surface parallel computer to 360 megaflops*

The blistering speed of Inmos Ltd.'s new T800 floating-point transputer is already making its mark in real-world computing. Meiko Ltd., founded by a group of Inmos employees who had worked on the original T414 transputer, is ready to plug the T800 (see p. 51) into its T414-based Computing Surface to make this high-performance parallel computer into a 360-megaflops supercomputer. Meiko says its T800-based Computing Surface, while a general-purpose machine, is well suited to image processing: it can create a frame in an animation sequence in one minute, rather than the T414-based machine's seven minutes.

Meiko is well positioned to exploit the new floating-point version of the transputer, says cofounder David Alden. Both companies are in Bristol, UK, and Meiko was founded by Inmos employees who were itching to make the most of the transputer in a systems context. As a result, Meiko was ready with its first Computing Surface [*Electronics*, Oct. 7, 1985, p. 43] when the original T414 was introduced, and it has staged an encore with the T800-based machine.

The Computing Surface's parallel architecture exploits the parallel features built into the transputer. Yet the user can continue to compile sequential Fortran programs with floating-point unit code. A sea-of-processors concept called the Fortran Farm, which consists of operating software above the Fortran code, distributes the tasks among the parallel floating-point engines.

In August, the company demonstrated a 3-billion-instruction/s Computing Surface running with 311 of the T414 transputers at the Siggraph conference [*Electronics,* Aug. 21, 1986, p. 21]. The same configuration with 311 T800s will become a 360-megaflops supercomputer, up to 10 times faster than the earlier machine. "The performance esti-



**FAST FRAMES.** Ray-tracing on the Computing Surface draws a frame for a DNA-molecule animation in less than a minute.

mate of 360 megaflops for a machine with 311 processors is sustainable floating-point performance, rather than a raw megaflops figure simply derived from the basic add and multiply times," says Alden.

This new addition to the ranks of supercomputers is particularly good at producing high-resolution pictures for computer-generated animation. A ray-tracing algorithm for generating images can be run on the Computing Surface's multiple processors, which can work on calculating either one image frame or several frames simultaneously. For the animation of a DNA molecule, each frame required between 8 and 16 million rays, depending on the degree of anti-aliasing required.

A typical frame (figure) required 120,000 CPU seconds to calculate—the whole job taking less than seven minutes—on the 311-processor T414 Meiko Computing Surface. Meiko estimates that plugging in the T800 processors will reduce the elapsed time to less than a minute.

Meiko's engineers at first envisioned a T414-based machine that would accommodate a floating-point coprocessor. But when they learned of the forthcoming T800 and, most importantly, that it would be plug-compatible with the T414, they decided not to implement a coprocessor but rather to wait for the new chip and use the microcoded floating-point software for the T414 in the interim. Existing Fortran 77 programs for the Computing Surface need only to be recompiled with Meiko's compiler to use the T800s.

Because of the T800's tightly coupled parallelism between the floating-point unit and the central processor, standard Fortran 77 achieves efficient use of the floating-point hardware without the complexity of vectorization. By eliminating vectorization, the new Meiko system raises the level at which parallelism needs to be considered up to that of the processing unit. In existing supercomputers, parallelism needs to be considered at the relatively low level of the pipelined vector unit.

In addition to eliminating vectorization, the Meiko Fortran lets programmers use parallel processing without resorting to a special language.

For a wealth of existing Fortran programs, Meiko has addressed the problem of transparently exploiting parallelism with the Fortran Farm. In the Farm concept, several independent sequential Fortran tasks are distributed among an array of processing elements.

With the Fortran Farm, the massive parallelism of the Computing Surface machine is tapped semiautomatically to produce an increase in throughput that is directly proportional to the number of processors. If a job is broken into separate sequential tasks or an existing program needs to be repeated many times with different data, existing Fortran programs, once set up, will be distributed by the operating software of the Farm among all the available processors in the Computing Surface for parallel execution.

Examples of applications that map well onto this combination of architecture and the Fortran Farm concept are Monte Carlo simulations and off-line animation production, where many frames can be processed concurrently.

By working closely with a microprocessor developer, a systems company like Meiko can bring enhanced versions of its products to market very quickly. The Computing Surface shows the advantages of designing a computer system to use a forthcoming microprocessor as a simple plug-in replacement for the original processor. □

## A LEAP FROM CHIP DESIGN TO SYSTEMS DESIGN

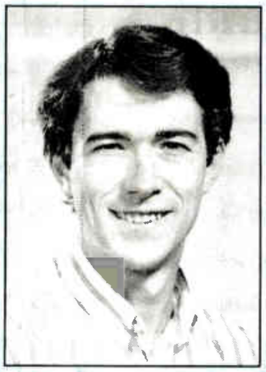
**It's not often** that a microprocessor designer gets a chance to apply the chip he worked on to systems design. But that's what Moray McLaren is doing with his move from Inmos Ltd. to Meiko Ltd. He joined Meiko in Bristol, UK, last summer after completing design work on the floating-point unit that Inmos is adding to the T414 transputer to create the T800. The 25-year-old honors graduate in microelectronic design from Edinburgh University had worked on the design of the T414 as well during his nearly three-year stint at Inmos in Bristol.

"Inmos was great," McLaren says. "I got a lot of good experience there. But Meiko presents an opportunity to work on more things, to do more of a whole job rather than a piece of a chip, working in smaller teams and with shorter design cycles."

He calls the T800 "a really elegant design. It has all the advantages of a coprocessor, with parallelism between the floating-point unit and the main processor—but because the floating-point unit is right there on the same piece of silicon, there are none of the problems associated with getting operands and instructions in and out."

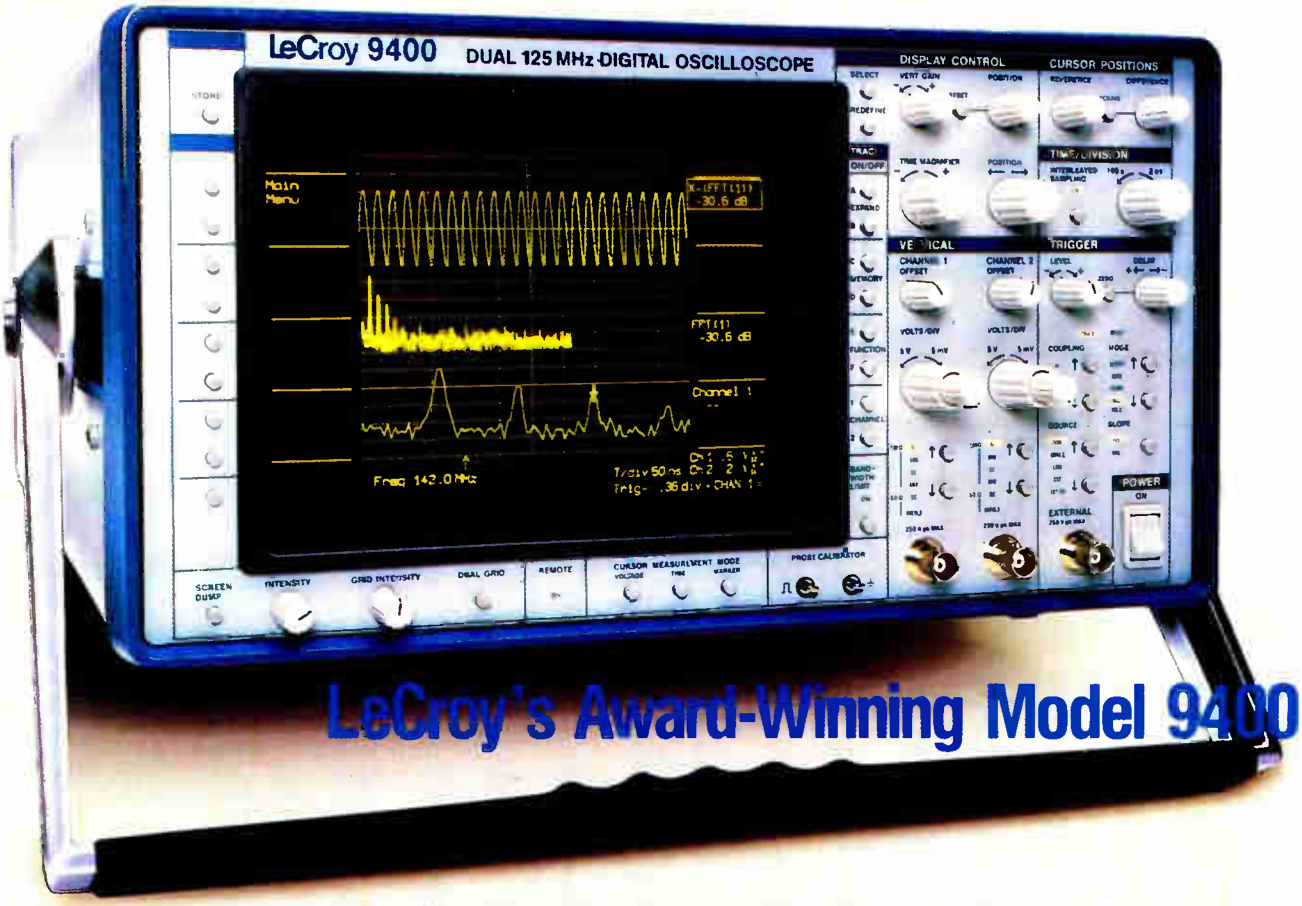
McLaren designed an efficient high-performance FPU that fits into a small area of the microprocessor chip—7 by 1.5 mm. He chose to emphasize performance in the primitive core operations, such as floating-point addition and multiplication. As a result, overall floating-point performance is high because the usual coprocessor hangups are avoided by the tight coupling of the FPU and the main processor.

"All the housekeeping to do with synchronizing the two units and saving the additional state of the floating-point unit on interrupts is implemented efficiently in hardware and microcode and is invisible to the programmer," says McLaren. "No other implementation—either single-chip or multichip—comes close for floating-point performance for a given board area."

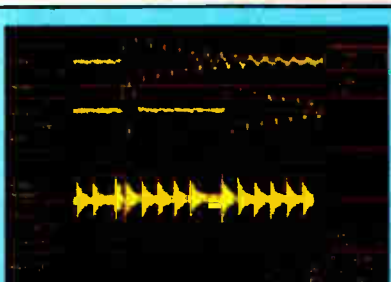

**MORAY McLAREN**

At Meiko, McLaren is working on integrated circuits for extending the functions of the company's computer products. Meiko is not ready to reveal any details of these features, but in general, McLaren will be designing integrated circuits to add more functions to the processor board for Meiko's Computing Surface computer—functions that go beyond those supplied by the transputer architecture.

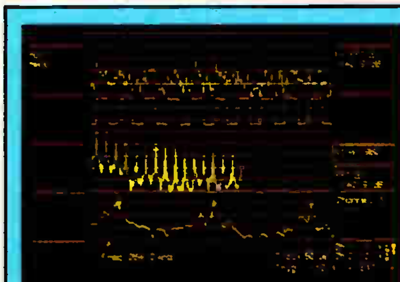
# Now for the First Time in a Digital Oscilloscope...



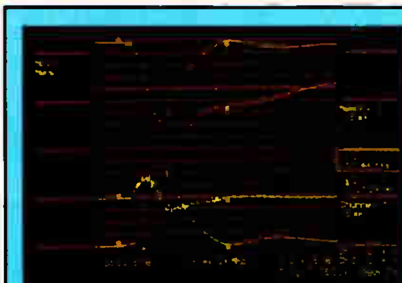

- Bandwidth in Excess of 125 MHz. 100 MS/S Digitizing Rate. 5 GS/S Random Interleaved Sampling Rate.
- ±1% DC Accuracy. Autocalibration.
- 32K Segmentable Acquisition Memories, Each Channel. Up to 192K Total Memory.
- Fast Fourier Transforms 50-25,000 Points.
- FFT Frequency Resolution; 1 milliHertz to 50 MHz.
- Signal Averaging in Time and Frequency Domains to 1,000,000 Sweeps.
- Digital Filtering and Extrema Mode.
- Fully Programmable Via GPIB and RS-232.
- Waveform Processing Mathematics: Integration, Differentiation, Arithmetics.



*Switching transients recorded in segmented memories show contact bounce in segment number 3. Cursors measure bounce-time-interval precisely.*



*Noisy H.F. Transmission Signal is averaged in time domain. Spectral content of cleaned-up signal is analyzed by FFT.*



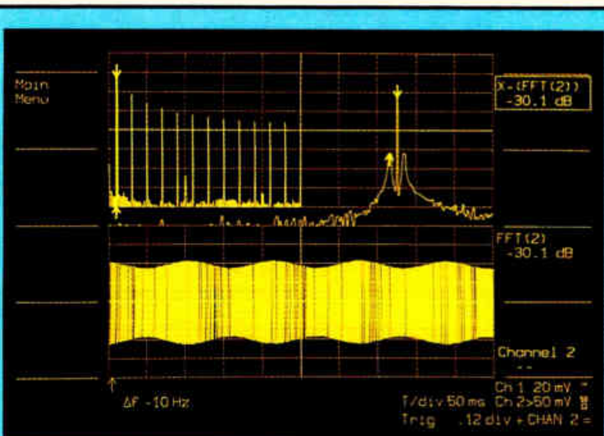
*Inverted photo-diode signal is normalized then integrated for energy measurement (area under curve >11.44 nVs). Differential dC/dt is shown as well.*

# ...Signal Processing in Both the Time and Frequency Domains!

## UNPRECEDENTED PERFORMANCE IN A GENERAL PURPOSE DIGITAL OSCILLOSCOPE!

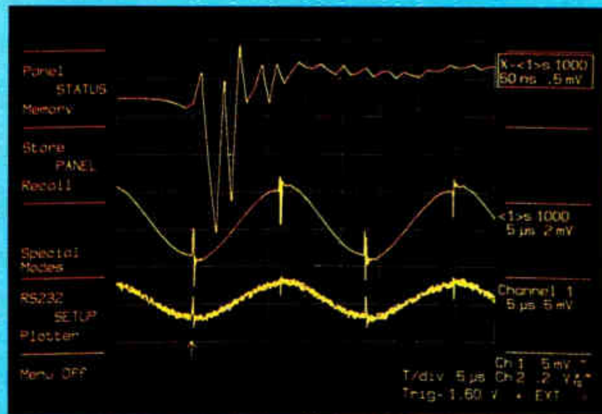
**LeCroy's Model 9400 Digital Oscilloscope offers you more waveform measurement capability, more signal analysis power, longer memories and higher precision than any other digital scope. Here's how:**

**Start with wideband, dual-channel, simultaneous signal acquisition at 100 MS/S and a 5 GS/S random interleaved sampling rate with unmatched DC accuracy of ±1%.** Add a full complement of waveform processing mathematics and then offer more memory capacity than any other scope, like 192K! Memory that can be segmented into smaller sections allowing you, for example, to store up to 250 waveforms per channel for individual analysis and comparison.




*Long records give wide frequency span. Modulated audio signal, recorded over 25,000 points, shows harmonics up to 25 kHz. Expansion shows siebands at 10 Hz and −30.1 dB. Frequency resolution is 2 Hz.*

**And now, with Fourier Processing,** you can examine the frequency constituents of your processed time-domain data over a **WIDER** range and with **MORE** resolution than has ever been possible before with any other **portable digital scope!** The 50-25,000 point FFT variable transform size provides unequalled resolution from 1 milliHertz to 50 MHz. Large transform size FFT's yield better and faster signal-to-noise improvement than signal averaging and enable you to separate closely-spaced frequency components for detailed analysis without an external computer. Multiple, menu-selectable display options present your spectra in familiar formats, such as power spectrum, power spectral density (PSD), real and imaginary, or magnitude and phase. And, with this versatile scope, you can instantly change displays or look at the same data in different formats **without changing setups.**




*Signal averaging improves dynamic range and sensitivity. Perturbation on a function generator sine wave is expanded to 500 μV/div vertically (10x) and 50 ns/div horizontally (100x) showing fine details, helpful to find cause of distortion.*

**And the 9400 has many more outstanding features!** Unique features such as **summation** averaging up to 1,000,000 signals with offset dithering to increase the effective resolution by several bits. And, **continuous** (exponential) averaging with multiple weighting factors so you can quickly and easily minimize the effects of noise on your measurements. Do you have a time or amplitude drift problem? In its unique **EXTREMA** mode, the 9400 precisely tracks and records all extreme positive and negative values including glitches and spikes as short as 10 ns. And with its comprehensive waveform processing, the 9400 offers many powerful routines for performing signal characterization, mathematical analysis and post-processing of waveform data.

**All this in a scope!** And yet, with all of its **unprecedented capability,** LeCroy's Model 9400 remains as easy to use as your familiar analog scope. Let our field engineers show you how easy it is to put the power of the 9400 literally at your fingertips.

**LeCroy . . . the Innovator in Instrumentation is Raising the Standards for Digital Oscilloscopes . . . Again!**

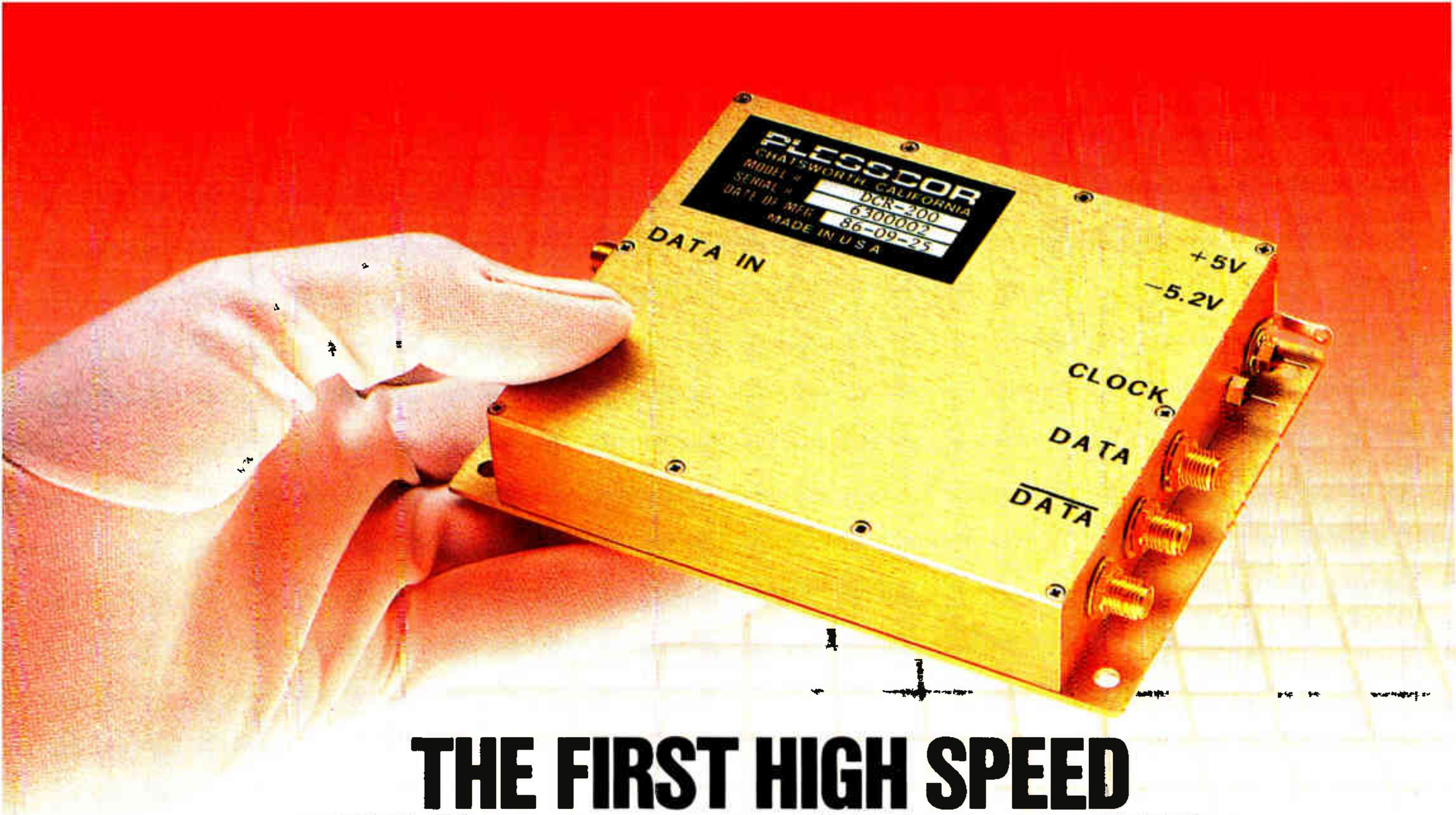

To receive your free literature package or, for a demonstration, simply circle the reader service card or call (914) 578-6038.

LeCroy

**700 South Main Street, Spring Valley, NY 10977, U.S.A., (914) 578-6097**
**Geneva, Switzerland, (022) 82 33 55 Sales and Service throughout the world.**

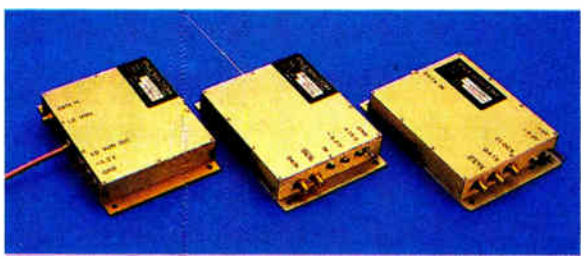
Circle 107 For Information

Circle 59 For Demonstration




# THE FIRST HIGH SPEED TRANSMITTER AND RECEIVER DESIGNED TO WORK AROUND THE CLOCK.

## From 0-878 Mb/s, PlessCor's Transmitter, Receiver and Clock Recovery Modules Take Data Transmission To An All Time High.



Bringing your high speed communications system up to speed doesn't begin and end with the transmitter and receiver. It also takes a clock recovery module to keep up with the data stream and make sense of the megabits.

At PlessCor, we're doing our bit to help solve your optical transmission problems where they begin. In the design stage. We're doing it with a complete "turnkey" system composed of laser diode transmitters, optical PINFET receivers and SAW clock recovery modules available in either standard or custom operating speeds, all the way up to 878 Mb/s.

We're doing it with the most advanced components and circuitry available. Like InGaAsP buried heterostructure laser transmitters featuring high optical power output and unrestricted data input. We're doing it with InGaAs PINFET receivers for long wavelength and high detection sensitivity. We're doing it with a clock recovery module that offers full signal regeneration capability.

Why have we worked around the clock to develop a complete modular transmission package for the commercial marketplace? For just one reason. To help you make the quickest recovery in communications history.

For more information on these as well as our full line of other optical transmitter, receiver and data link products, contact us at 818/700-0841.

MADE IN THE USA.

**PLESSCOR**

PlessCor Optronics Inc., 20200 Sunburst Street, Chatsworth, CA 91311
Tel: 818/700-1233. Telex: 650-239-8651. Fax: 818/700-9047.

# NEXT STEP FOR FIBER OPTICS: THE LOCAL LOOP

*With growth flattening for long-haul networks, the makers of fiber-optic gear must now adapt their products for use in short-haul communications links*

**By Robert Rosenberg**

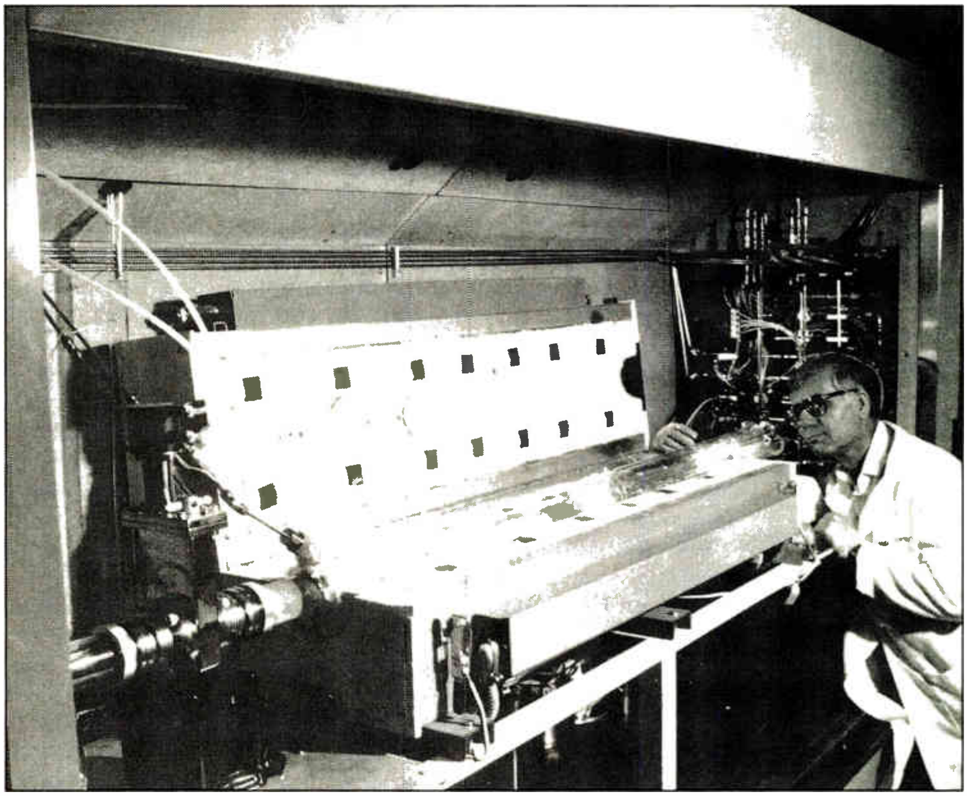
Fiber-optic communications equipment makers are turning their attention to the local loop in an attempt to get growth back on track. They are working to bring down the cost of their gear—an obstacle that must be overcome before the regional Bell operating companies will begin to install fiber-optic gear for short-haul communications.

Growth of the fiber-optics industry has already begun to slow because saturation nears in the long-haul network business. The fibers, sources, detectors, and logic circuits that have made fiber-optic transmission the long-haul carrier of choice must now be applied to local, short-haul communications.

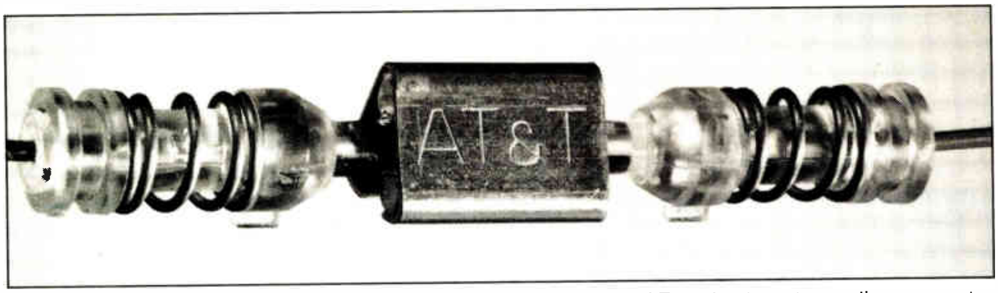
Besides cost, the makers of fiber-optic equipment are working on easier connection techniques. These are important since the cabling used in short-haul communications systems will be installed in a variety of environments, from crowded conduits in modern buildings to decades-old telephone pipes at the bottom of city manholes. New technology is simplifying the construction of fiber-optic networks under such conditions.

In long-haul networks, the fiber-optic industry's primary concern is cranking up the standard long-haul transmission rate, currently 565 Mb/s, to 1 Gb/s and beyond. New lasers, such as the distributed feedback laser, and families of gallium-arsenide circuitry will make the move to 1 Gb/s feasible.

The bulk of the long-haul networks have now been converted to fiber optics, however. The industry's growth has slowed accordingly, leaving insiders disappointed and frustrated. The total value of installed fiber-



**1. MORE DETECTORS.** Mass production of the longer-wavelength photodetectors is possible with Epitaxx's vapor-phase epitaxy.




**2. CONNECTOR.** To splice fiber-optic ribbon cable, AT&T devised a rotary-splice connector that mates single- and multimode fibers quickly without special procedures.

optic equipment (excluding the cable itself) was $750 million last year, according to the New York investment bank L. F. Rothschild, Unterberg, Tobin Inc. Some projections from the early 1980s forecast that the industry would have reached the $1 billion level by now. "Things are not as good as we expected," says J. E. (Jack) Andrews, department chief of lightguide development engineering at the AT&T Co.'s Network Systems Division facility in Atlanta. "We expected continuous growth, but we've had layoffs. So have Corning and the others."

To get back on track, the industry must penetrate local markets. It must push fiber into the gap between central telephone switching offices and customers' premises. Fiber optics also must become the backbone of local networks. Then the installed-equipment non-cable value could climb to $1.7 billion by 1990, projects Rothschild, Unterberg, Tobin. The growth rate could jump form the present 20% to as high as 30%, predicts Rothschild research associate Cindy M. Schmidt. In the early 1980s, it was as high as 40%, she estimates.

## TARGETING COST

A number of companies are already working on fiber-optic networks, equipment, and components for use in local communications. Their primary goal, in most cases, is to make their costs competitive with copper's.

American Photonics Inc., for example, is coupling various grades of multimode and single-mode fibers to a line of fiber-optic data communications modems and a lightwave 4:1 multiplexer. "We are taking short-wavelength [800-nm] sources being used in video disks," says James A. Walyus, chief executive officer of the Brookfield, Conn., company. "We use them as drivers. We are not spending the $1,500 apiece that it costs for a 1,300-nm laser with a cooler."

The equipment cannot take full advantage of the 565-Mb/s data rates possible over single-mode fibers, but that's not a problem, says Walyus. On the local level, users need the more modest T1 (1.544-Mb/s) and T2 (6.312-Mb/s) rates that still are more than an order of magnitude higher than the rates possible with copper technology.

Albert D. Bender, the president of FiberCom Inc. in Roanoke, Va., shares Walyus's opinion. FiberCom produces Ethernet-compatible fiber-optic networks, and it too is shying away from the costly telecommunications components. "We are at the low end of the fiber business, where it is very price-sensitive," says Bender. "Our optical sources are 850-nm LEDs, typically surface emitters, that we can buy for under $10 apiece in quantities. We couple to a 50-μm fiber at under –20 dBm, which is not very exciting. Our detectors are p-i-n diodes with modest performance characteristics, but we get them for under $10, too."

Eventually, the vendors of short-haul systems must move from the 850-nm range to 1,300 nm, where the dispersion characteristics that plague multimode fibers are minimal. Dispersion ultimately determines how much bandwidth is available. At the same time, they must maintain their relatively low costs.

Improvements in process technology used to manufacture the longer-wavelength components will go a long way toward dropping the cost of 1,300-nm systems, making them inexpensive enough for widespread deployment. For example, Epitaxx Inc., Princeton, N. J., has devised a vapor-phase epitaxy process for manufacturing 1,300-nm and 1,500-nm Indium GaAs p-i-n photodetectors (Fig. 1). Plans are under way to launch a complementary line of LEDs.

Vapor-phase epitaxy is the best technology for producing the InGaAs parts, says Epitaxx president Gregory H. Olsen, because it has already proved itself for more than 20 years in silicon production. "Most manufacturers use a liquid-phase epitaxy process. Solid films are deposited from a cooled, saturated melt," Olsen says. "But you lose the ability to mass-produce, because the bath can be used for only one or two substrates a day. Vapor-phase epitaxy has the advantage of greater uniformity across the wafer and yields of 10 to 15 wafers a day."

Materials such as germanium and InGaAs are being used because silicon detectors—which work well at 850 nm—become transparent to wavelengths above 1,000 nm. Germanium was the material of choice for some time, but has recently been supplanted by InGaAs. As transmission moves to longer wavelengths, detectors with narrower bandgaps will be needed—and it's easier to alter the bandgap of InGaAs than it is of germanium.

Besides the attempts to drive down the cost of local fiber-optic systems, work is being done to make them easier to hook up. "Much of our development effort is in new connection systems," says J. A. Jefferies, manager of engineering for lightguide fiber and cable at AT&T Networks Systems in Atlanta. AT&T is trying to build connectors that can be coupled quickly—even in big-city manholes. For example, AT&T Network Systems enhanced its rotary splice technique (Fig. 2) used to mate the 125-μm cladding for single- and multimode fibers. The big advantage of the rotary splice is that the fibers can be mated quickly, without specialized test sets or a local injection of light. By adding two flanges to the mated glass plugs installed on each end of a fiber, a visual alignment can be made when the fibers are joined in the triangular mating sleeve. To decrease signal loss, a gel with an index of refraction matching the fiber is spread at the joint.

The rotary splice is proving itself in use with AT&T's flat ribbon cable, which consists of 12 strands of single-mode fiber. The strands are floated onto a sandwich of two adhesive-faced polyester tapes to form a 0.14-in. ribbon that can be stacked. But connecting each strand is a laborious process, so AT&T came up with an array splice connnector for the single-mode fibers. The array connector is made of two grooved silicon clamps on either side of the ribbon that restrain the fibers in it. The connector is a speedy way to get in and out of manholes, but it does take extensive training to make a good splice, Jefferies says.

Cost and connections are not the main concern at the high end of the fiber-optic industry, where most vendors are working to increase the long-haul data rate. Such technological improvement historically has been first priority of the industry, ever since the first commercial fiber-optic transmission system operating over multimode fibers went into service in 1977.

Those early commercial fiber-optic systems were made up of multimode fibers consisting of high-refractive-index 50-mm core and 125-mm cladding, which could easily be coupled to 0.8-mm light sources based on gallium aluminum arsenide semiconductors.

However, launching short wavelengths of light into the comparatively wide cores dispersed the light, producing signal interference that kept performance down to about 90 Mb/s, roughly the same as copper-cable networks. Today's single-mode fibers, consisting of 5- to 8-mm cores coupled to longer-wavelength (1.3-mm) InGaAsP semiconductors, have steadily increased transmission rates.

"Currently, 565 Mb/s is the established long-haul standard. But it is being expanded to 1 Gb/s—there is a worldwide push on," says Neven Karlovac, director of engineering in the Lightwave Systems Division of Rockwell International Corp., Dallas. And there is no indication that the industry plans to stop at 1 Gb/s.

AT&T Bell Laboratories has gone well beyond the 1-Gb/s threshold in the laboratory and in field experiments. The labs recently demonstrated an experimental 8-Gb/s direct-detection fiber-optic link over 68 km and has field-tested a 1.7-Gb/s system over 23.1 km of single-mode fiber between two sites in Pennsylvania, says Tingye Li, head of the Lightwave Systems Research Dept. at Bell Labs. The field test used a high-speed InGaAsP/InP laser with a channeled-substrate buried heterostructure that was externally modulated.

Also in the race for higher speeds and longer-transmission links is Japan's NTT Corp. It recently demonstrated an experimental 1.6-Gb/s transmission over a 75-mile link, a transmission rate that represents a fourfold improvement over the 400-Mb/s technology now in use in Japanese long-haul communications. The key to that improvement is the single-longitudinal-mode, distributed-feedback laser diode, which NTT coupled with InGaAs avalanche photodiode detectors (Fig. 3).

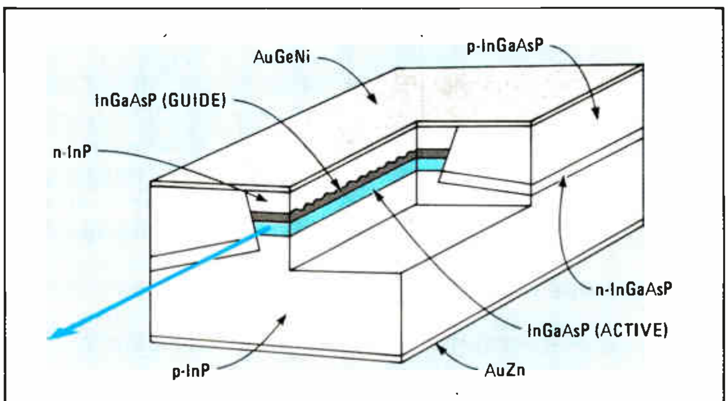
"If there is one key technological development

*The industry has pushed transmission rates for long-haul fiber-optic networks to 565 Mb/s; now experimental systems are reaching rates of 1.6 Gb/s and beyond*

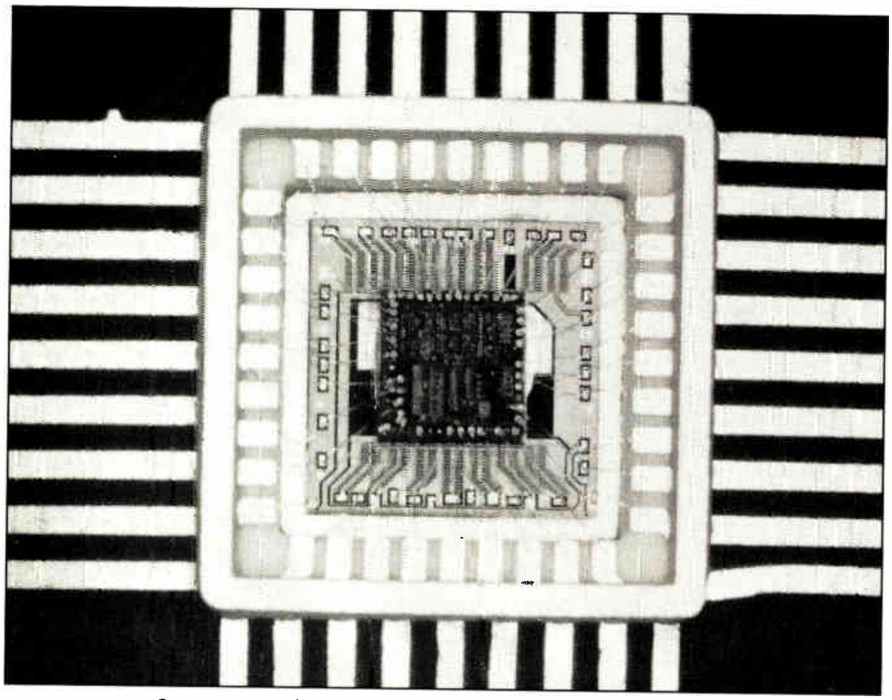
recently, it is the development of the single-frequency distributed feedback laser," Rockwell's Karlovac says. "The advantage of the single-frequency feedback laser comes down to overcoming the dispersion characteristics of the fiber and maximizing the distance between repeaters." The laser provides high optical power and narrow spectrum bandwidth. Conventional diode lasers also produce high optical output but tend to have a wider spectrum, producing unwanted modes. The distributed-feedback laser feeds back the output, producing a true single-mode output.

The laser design has already been commercialized. It has been available in the U. S. for the past two or three months from the Microwave and Optoelectronic Division of Fujitsu Microelectronics Inc., Santa Clara, Calif., among others.

NTT externally modulated the laser sources us-




**3. KEY COMPONENT.** To get to a 1.6-Gb/s transmission rate, NTT is using a single-longitudinal-mode distributed-feedback laser.



**4. GaAs ENTRY.** Gigabit Logic's 8 : 1/1 : 8 time division multiplexer and demultiplexer are fabricated in 1-$\mu$m geometries and contain about 1,000 gates per chip.

ing familiar silicon modulation circuitry, rather than the more exotic GaAs circuitry, because of silicon's higher reliability, says Nobuaki Ieda, senior researcher at NTT's Atsugi Electrical Communications Laboratory. "The field trial used high-speed bipolar technology in all SSI and MSI logic. We have more experience with silicon; it is well established." So far, Ieda says, silicon designers have been able keep pace with the improved system performance. But he concedes that someday NTT will have to switch to GaAs logic circuity.

The higher electron mobility and lower parasitic capacitance of GaAs give it the ultimate edge over silicon in high-performance systems. "If an application is in the performance range of silicon, that technology is more effective. But the performance limit of bipolar ECL is at 565 Mb/s, and achieving that kind of performance usually means going to custom gate arrays, which are expensive," says Stewart Sando, director of product marketing for Gigabit Logic Inc. GaAs ICs are typically an order of magnitude faster than silicon. "Look at bipolar ECL. The measure of its rise and fall times is in nanoseconds. Our products are typically about 150 ps," Sando says.

The Newbury Park, Calif., company is producing a line of digital GaAs circuits with the commonly used depletion-mode metal-semiconductor FET process. Gigabit has introduced an 8 : 1/1 : 8 time-division multiplexer and demultiplexer (Fig. 4) with full ECL input-output compatibility. And Sando expects big performance improvements in 1987. The 1-$\mu$m parts now being shipped contain about 1,000 gates per chip. The density should double next year, he says. "We are getting the improvements from better process control and lower defects. There is nothing magic about it, just plain, hard work."

TriQuint Semiconductor Inc., a Tektronix Inc. subsidiary in Beaverton, Ore., is also targeting GaAs, with depletion-mode parts built around its Q-Logic standard-cell library. Engineers can use Q-logic to design feature additions into high-speed parts without giving up high data rates, says Don Larson, design engineer for the Q-Logic family.

Now available are a 3-GHz, 4-bit ripple counter and a 1-GHz, 4-bit synchronous up/down counter. In January, the company will introduce a 2-GHz 4 : 1 and 1 : 4 multiplexer-demultiplexer pair and a programmable 16 : 1 and 1 : 16 mux-demux pair which can be made to operate as two 8 : 1 parts.

"These parts were all done with standard cells, and there wasn't a lot of tweaking involved," Larson says. "If the next step in system speeds is going to go to 2.2 to 2.3 GHz, then our goal would be to raise our performance to the range of 2.5 GHz. And we think we can do that."

Additional improvements in performance will come with higher integration in GaAs, which is beginning to occur. In early October, Microwave Semiconductor Corp., a subsidiary of West Germany's Siemens AG, introduced five highly integrated GaAs circuits: a transimpedance receiver circuit, a transimpedance amplifier, a laser diode current modulator, and a time division multiplexer and demultiplexer.

## A 2-GHz RECEIVER

The 72-by-46-mil transimpedance receiver, dubbed TIRC 1500, has a speed of 2 GHz, says Saul R. Lederhandler, president of the Somerset, N. J., company. The monolithic circuit not only converts p-i-n or avalanche diode currents to voltage, but also amplifies the voltage and outputs it into a clocked digital format. To decrease the possibility of the amplifier being saturated with high currents from a p-i-n diode, an automatic gain control is implemented.

All of the advances that are pushing long-haul fiber-optic communications to higher speed and greater capacity, though, must eventually be reconciled with the need for low-cost, easily connected systems for local use. The various vendors working at both the low end and the high end each must play a part. The former need to reach the speed and capacity that will match the capability of the long-haul networks, and the latter need to lower costs and simplify connections for short-haul applications. □

# AT IEDM, NEW WAYS TO BOOST CHIP SPEED AND DENSITY

*International Electron Devices Meeting will showcase advanced structures and new processes paving the way to everything from 4-Mb dynamic RAMs to bipolar VLSI*

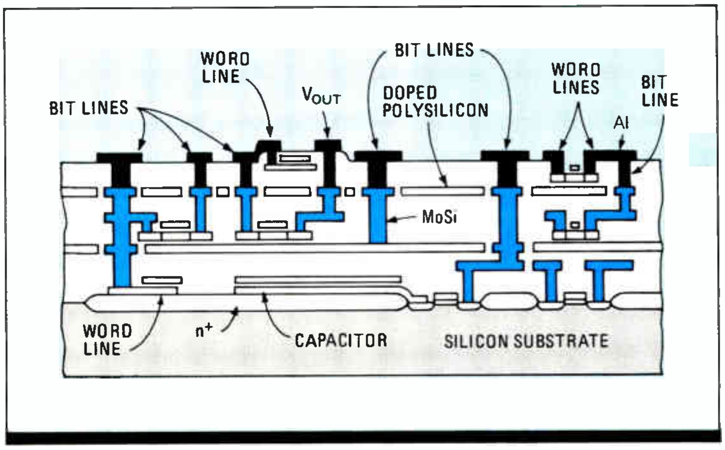
Device and process engineers are making big gains as they step up their quest for new ways to increase integrated-circuit density and speed, now that ICs' shortest dimensions are shrinking below 1 μm. At the annual International Electron Devices Meeting next month, they will report on advances in silicon-on-insulator technology and new departures in cell structures for both dynamic and static random-access memories. The goals in both Japan and the U. S. are to move 4-Mb DRAMs toward the market and to boost SRAMs' role as a technology driver. Researchers also will chart similar advances in erasable programmable read-only memories.

In bipolar technology, the new process twists and new structures that will star include an improved bipolar-CMOS process and progress toward very large-scale integration. In power discrete devices, work on next-generation high-voltage, high-current devices will take the spotlight at the IEDM meeting Dec. 7-10 at the Westin Bonaventure Hotel in Los Angeles.

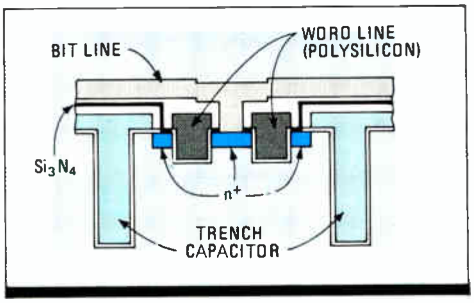
In DRAMs, one of the most advanced structures is a triple-layered silicon-on-insulator arrangement (Fig. 1) from Sharp Corp.'s Central Research Laboratories at Nara, Japan. Making use of three recrystallized SOI layers, Sharp has fabricated a standard planar memory cell in which the capacitor and switching gate can be laid out in the same layer or in two neighboring layers. This arrangement has the effect of increasing density and reducing lateral chip area.

Researchers at NEC Corp. in Kanagawa, Japan, are taking a much more conservative approach than Sharp's. They are looking to squeeze as much density and performance out of standard bulk silicon with a variation on the trench capacitor scheme they call a trench transistor cell. This structure uses the trench transistor as a transfer gate and self-aligns the bit-line contacts to the word lines (Fig. 2). It also is compatible with conventional two-level polysilicon CMOS processes. Sharp's researchers have fabricated devices with cell areas of only 9 $\mu m^2$ that are only 0.5 μm deep—more than enough to allow them to achieve 4-Mb densities and beyond.

Using another variation of the trench capacitor cell, Fujitsu Ltd.'s Semiconductor Devices Laboratory in Atsugi, Japan, has achieved 4-Mb




**1. SOI.** Sharp's silicon-on-insulator technology is a three-level design.




**2. TRENCH.** NEC sees its trench transistor cell as a key to the 4-Mb DRAM.

densities. Fujitsu calls its variation the dielectrically encapsulated trench-capacitor cell. In this 12.72-$\mu m^2$ configuration, a polysilicon-to-polysilicon storage capacitor is placed in a 5-$\mu$m-deep trench, into which the storage electrode is placed and then surrounded by a counter-electrode that blocks the expansion of the electric field to adjacent cells. Both elements are then placed in a silicon dioxide capsule to prevent diffusion of doped impurities in the counter-electrode. A MOS FET fabricated with 1-$\mu$m design rules is the transfer gate.

The path to 4-Mb density at Mitsubishi Electric Corp. of Itami, Japan, is a chip that incorporates a capacitor cell with a folded bit-line in its unusual adaptive sidewall isolation technique. The 10.92 $\mu m^2$ cell, 2 $\mu$m deep, has an isolated capacitor built onto the walls. This conserves space and prevents expansion of the electric field into adjacent cells. The transfer gates, fabricated using standard local-oxidation CMOS processing, are placed atop this trench.

## BOOSTING SRAM DENSITY

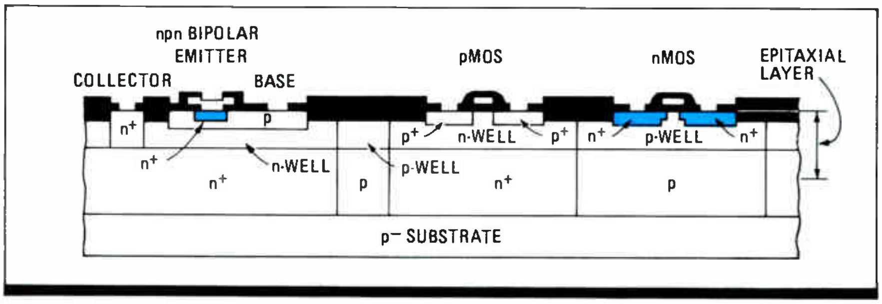
With SRAMs emerging as an important technology driver, researchers at Matsushita Electric Industrial Co. are using SOI techniques as a vehicle to reach megabit densities. They are stacking memory cells in layers in an experimental 8-K CMOS SRAM. In the Osaka, Japan, company's 120-ns chip, each of the three layers has a silicon island array embedded in silicon dioxide by laser-beam recrystallization. In the second layer, SRAM cells are fabricated on 10-by-63-$\mu$m SOI islands, with longer 2-mm islands used for diffused interconnections. In the top layer, a tungsten/tungsten silicide/polysilicon metal scheme is used to make an interconnect structure linking the SRAM cell islands. The SRAM cells and surrounding circuits such as input/output, decoders, and sense amplifiers are built in the top layer, but the second layer contains only SRAM cells.

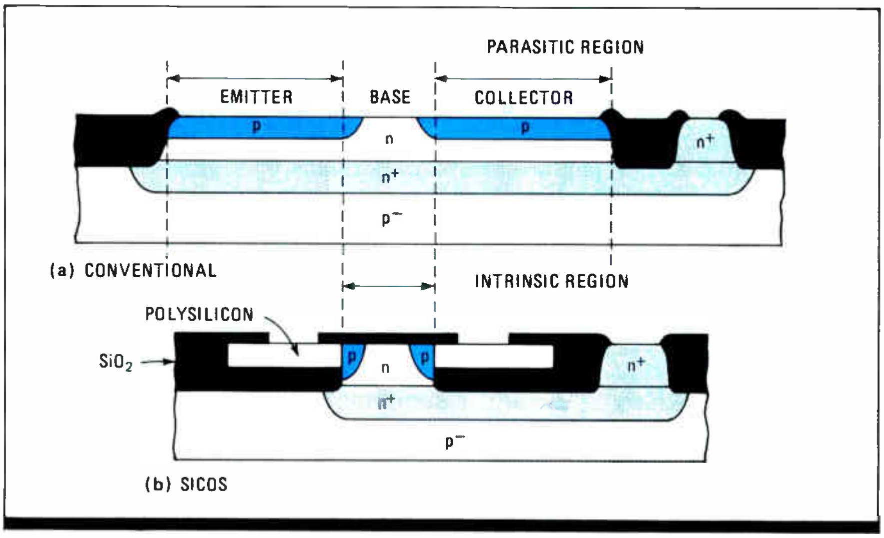
To get the extremely fast access times needed in megabit-level SRAMs, Motorola Inc. engineers in Austin, Texas, have developed a selectively pumped p-well memory-array technology. They have reached speeds as high as 22 ns in a 256-K double-polysilicon CMOS SRAM using 1.2-$\mu$m double-level metal. To achieve this speed, Motorola raised the threshold voltage of the n-MOS devices in the array by selectively pumping the p-well containing the array with an on-chip bias generator. This reduces the subthreshold current by three orders of magnitude, which in turn reduces the standby current by a similar amount. In the periphery, low-threshold n-MOS transistors raise device performance. In addition, precharge operation is speeded with a reduction in the bit-line junction capacitance. To avoid latchup, a novel p-channel pump circuit was designed to eliminate forward biasing of junctions.

In four-transistor SRAMs that use resistive loads, one critical problem is developing submicron resistors with sufficiently high values. Without these submicron resistors, it won't be possible to achieve high densities without sacrificing performance. For researchers at Hitachi Ltd. in Ibaraki, Japan, the solution is an oxygen-implantation technique for undoped polysilicon films. Combined with film thinning and arsenic doping, this technique allows the fabrication of 0.8-to-1-$\mu$m resistors with little or no loss in impedance.

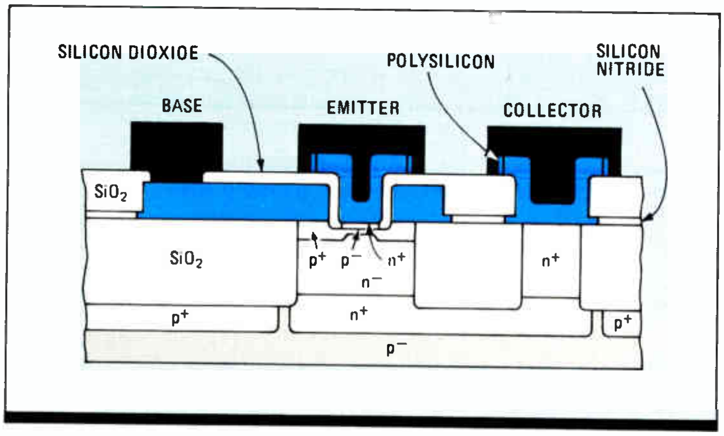
Using a 1-$\mu$m CMOS process optimized for the fabrication of highly stable tera-ohm polysilicon resistive loads, Sony Corp. researchers in Atsugi, Japan, have fabricated 1-Mb SRAMs. But first Sony had to surmount two major technical barriers. Researchers reduced the bird's beak—caused by residual silicon—without increasing

**3. SMALLER AND FASTER.** Hitachi has improved its mixed bipolar-CMOS logic, reducing geometries from 2.0 to 1.3 $\mu$m and gate delay from 700 to 500 ps.




**4. MATCHMAKING.** Hitachi replaces uncomplementary npn-pnp structures (a) with a sidewall approach (b) that minimizes parasitic effects.




**5. BOUND FOR VLSI.** Matsushita aims at bipolar VLSI by using self-aligned double-diffusion polysilicon to fabricate base electrodes.

stress on the necessary nitride film by inserting a buffer film between the nitride and the thin oxide used to reduce the beak. Then, they achieved high resistance—ranging from 0.5 to 2 TΩ—with short polysilicon loads by placing the loads between two nitride film layers to eliminate hydrogen diffusion into the polysilicon, and by keeping the processing temperature below 900°C.

Less dramatic than DRAMs and SRAMs in terms of density or cell size, nonvolatile memories make up for that with innovative design. For example, work at the University of California at Berkeley has netted a source-side injection EPROM configuration with an order-of-magnitude improvement in programming speed—5 μs—and a low drain voltage of 5 V. Researchers achieved this by using an asymmetrical n-channel stacked-

*Bipolar advances include a Bi-CMOS process with 30% better gate delays and a sidewall structure for pnp devices that reach the 3-GHz speed of npn devices*

gate MOS FET with a short, weak gate-control channel introduced close to the source.

Aiming for high speed, engineers at Silicon Microsystems Inc. in San Jose, Calif., use a 1.5-μm n-well double-polysilicon CMOS process to build a high-performance three-transistor EPROM cell. In a 64-K chip, the 138-$\mu m^2$ cell results in a read-access time of 25 ns, twice the speed of current designs.

Aiming for high density rather than high speed, Texas Instruments Inc. researchers will describe a contactless self-aligned EPROM technology that results in a cell area of only 13.5 $\mu m^2$, which at 1.5-μm design rules is one third smaller than the conventional 20-to-25-$\mu m^2$ cell (see p. 70). Used to fabricate a fully functional 64-K EPROM, the technology will lead to cells that can be scaled to below 10 $\mu m^2$. That cell size will give megabit densities, the researchers believe.

In bipolar-CMOS logic, Hitachi will report further improvements in its Hi-BiCMOS process (Fig. 3). It is using a well structure with self-aligned $n^+$ and $p^-$ buried layers to create bipolar npn devices with polysilicon emitters and n-MOS and p-MOS transistors. The structure is fabricated with a standard double-polysilicon process to which three mask steps have been added for the bipolar devices. The Hitachi team will report that reducing critical device geometries from 2.0 to 1.3 μm gives an almost 30% improvement in gate-delay time, from about 700 to 500 ps.

Hitachi researchers also will describe a step toward the goal of truly complementary bipolar npn-pnp structures. In many bipolar circuits, pnp transistors are used in combination with npn devices. However, where npn devices typically operate at cutoff frequencies in the gigahertz range, pnp types are hard pressed to edge up beyond half a gigahertz. To solve this, Hitachi uses an advanced version of its sidewall-base contact structure, or SICOS (Fig. 4), incorporating polysilicon electrodes on silicon dioxide to minimize parasitic effects. This requires no additional fabrication steps to produce 3-GHz lateral pnp devices compatible with vertical npn transistors.

Shooting for bipolar VLSI densities, process engineers at Matsushita have developed a new self-aligned double-diffusion polysilicon technology permitting shallow emitter-base junctions. They then combined the technology with a new method for fabricating self-aligned base electrodes and got extremely small submicron transistors with 0.4- to 0.6-μm emitters that have gate propagation delays of no more than 75 ns and a cutoff frequency of 11 GHz (Fig. 5).

Reducing gate delays even further, engineers at Hitachi have developed an advanced version of their bipolar process with the base contacts in the sidewall. The new version has polysilicon bases, shallow emitter profiles, and a very shallow graft base to reduce parasitic capacitances, as well as polysilicon resistors. The result is ECL-type gate delays of no more than 63 ps—which Hitachi says is the fastest ever reported—at about 3 mW per gate.

Also of interest at the meeting will be technologies that handle high voltages and currents needed for the next generation of power transistors. For example, engineers from Siemens AG in Munich will describe a very fast-switching 1,000-V, 50-A bipolar power transistor. The speed is achieved through the use of a small-geometry structure it calls the Siemens Ring Emitter transistor, which features 5-μm emitter geometries and a 3-μm base width. In three-stage Darlington configurations, the transistor boasts a storage time of less than 2 μs and a MOS FET-like fall time of 30 ns, even when switching a 50-A inductive load. It is ideal for power-converter and chopper applications in motor drives. □

# CONTACTLESS ARRAYS FOR EPROMs ARRIVE JUST IN TIME

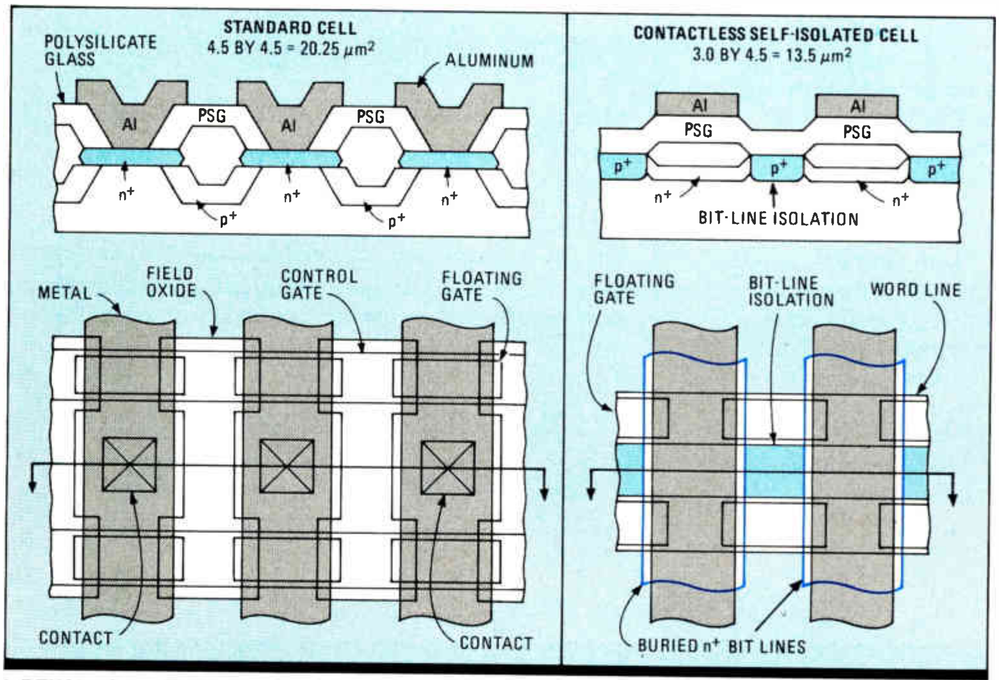
*With conventional EPROMs getting increasingly difficult to make as densities increase, TI's new crosspoint structure promises lower-cost, denser arrays*

Lower-cost, denser arrays for erasable programmable read-only memories are on the way from Texas Instruments Inc. What TI calls the array contactless EPROM, or ACE structure, is designed to eliminate metal contacts and thereby overcome manufacturing difficulties associated with conventional technologies. The structure makes it possible to build EPROM arrays with a third less area than arrays made with conventional techniques. This new structure has already yielded 64-K EPROMs that operate just as fast as conventional memories and show the reliability necessary for commercial use.

The new EPROM structure couldn't come at a better time. It has become more and more difficult to manufacture EPROMs as they have gotten denser and as existing structures have been scaled down to their limits. As the feature sizes of conventional arrays have gotten smaller, it has become harder to make contact with the self-isolated cells. In a typical memory made with 1.5-μm design rules, making contact with a cell involves depositing metal down to the bottom of a hole some 2.5 μm deep but only 1.5 μm on a side.

In order to improve contact with the individual cells, the ACE process aims at eliminating metal. By making the manufacturing easier, it holds out the prospect of increasing yields and therefore lowering costs. As a result, the process promises to help EPROMs maintain their position as the predominant nonvolatile memory device. It will help them remain competitive even as the more flexible electrically erasable PROMs drop in price, thanks to the new flash technology in which the whole memory is erased with a single impulse.

The new technology developed at the Dallas company employs a crosspoint configuration that is defined between a series of buried $n^+$ bit lines and an orthogonal set of polycide word lines. In contrast to conventional self-isolated cells, the new configuration's individual self-aligned cells are accessed through the bit and word




**1. DENSER CELL.** The area of a conventional EPROM cell drops by a third with the contactless self-isolated cell.

lines, with no need for a direct connection to each memory element. Memories made using the new process are planar and, in principle, have no need for metal contacts—which allows their increased density.

In the crosspoint array of the new memory, each memory cell is accessed through its $n^-$ buried bit line and its polycide word line (Fig. 1). The polycide control gates that serve as word lines are low-resistivity, two-layer stacked structures consisting of a layer of polysilicon covered by a layer of tungsten silicide. Isolation between the bit lines and the word lines is provided by a layer of thick oxide grown over the buried $n^-$ layer. Isolation from one bit line to the next is achieved by ion implantation.

A conventional EPROM cell made with 1.5-$\mu$m design rules typically measures 4.5 by 4.5 $\mu$m, yielding a cell area of 20.25 $\mu m^2$. The cells in the 64-K demonstration vehicle, which was also made with 1.5-$\mu$m rules, measure 4.5 by 3.0 $\mu$m, for a cell area of just 13.5 $\mu m^2$.

## SOME METAL USED

Although in principle the ACE process requires no metalization, some metal was used in the 64-K demonstration vehicle in order to reduce bit-line resistance. The metal lines run parallel to the buried bit lines and contact them every 16th cell, instead of every cell, as is required in conventional structures. As superior buried-layer materials—silicides, for example—are developed, the metal will be able to contact the buried layer at fewer and fewer points, until finally these contacts will be eliminated altogether.

Other than its use of buried $n^+$ bit lines under the floating gate and control gate, the ACE process isn't all that different from the standard FAMOS (floating-gate avalanche MOS) processes used for all EPROM fabrication, say TI engineers. The new process is a self-aligned, twin-well, high-voltage CMOS process with conventional parameters (Table).

After the buried $n^+$ module defines the active FAMOS area, the first gate oxide is grown, the first layer of polysilicon is deposited, and the floating gates are formed in the polysilicon. Then the interlevel dielectric and n- and p-channel transistors are created, and the control gates that serve as the word lines are formed in the two-layer polysilicon/tungsten-silicide structure. The self-aligned source/drain, contact, and metalization scheme is similar to that employed in conventional CMOS technologies.

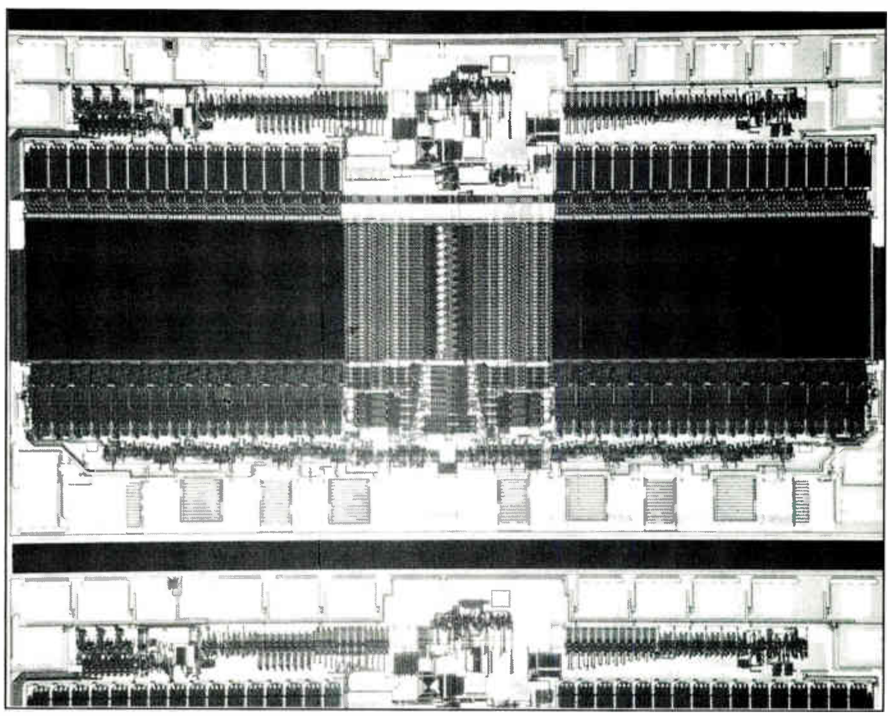
The buried $n^-$ FAMOS structure has programming characteristics similar to those of conventional

*ACE PROCESS PARAMETERS*

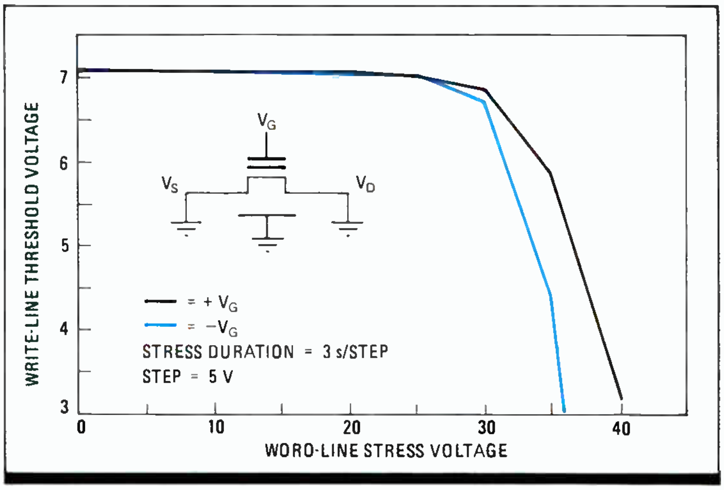
| | |
|---|---|
| Technology | Twin-well, double-poly, single-metal CMOS |
| Minimum feature size | 1.5 $\mu$m |
| $n^+$ resistivity | 30 $\Omega$/square |
| FAMOS oxide thickness | 350 Å |
| CMOS oxide thickness | 400 Å |
| Interlevel dielectric material | Oxide-nitride-oxide |
| Interlevel dielectric thickness | 375 Å |
| Metal pitch | 4.5 $\mu$m |
| Control-gate resistivity | 3 $\Omega$/square |
| Contact size | 1.5 by 1.5 $\mu$m |

EPROMs. As the drain voltage rises, the drain current rises with it, until avalanching takes place near the drain junction. At that point, hot electrons tunnel into the floating gate, charging it and reducing the conductivity of the transistor channel. As more and more charge gets trapped on the floating gate, the current keeps decreasing, the threshold voltage $V_T$ moves to a much higher level, and the transistor turns off. After this happens, the only way to remove the charge from the floating gate and return the conductivity of the transistor to normal is to expose the chip to intense ultraviolet light.

To demonstrate the viability of the ACE structure, TI built a fully addressable 64-K memory (Fig. 2). The demonstration vehicle employed nominal FAMOS process parameters, as well as variations on them—varying lengths, widths, and bit-line contact densities. The continuous buried $n^-$ structure, like the X-cell array used in



**2. PROVING GROUND.** This test vehicle, a 64-K EPROM, demonstrated the validity of the ACE concept. The column-address access time of this fully functional memory is 60 to 70 ns.

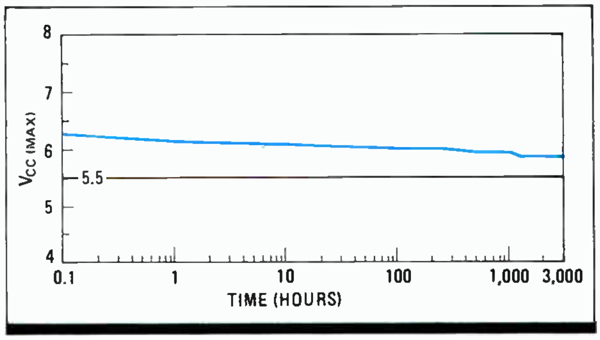



**3. NO STRESS.** In an n+ FAMOS cell, the threshold voltage of the interlevel dielectric withstands word-line stress voltages to 25 V.

TI's standard EPROM designs, requires that both sources and drains be addressable. It provides flexibility of source bias to the array to improve manufacturability margins, especially at the shorter FAMOS channel lengths.

Fully functional memories were fabricated using this technology. Cell drive—that is, cell sense current—was typically 100 μA, yielding a column-address access time of 60 to 70 ns. Allowing for another 60 to 70 ns to get overall address-access time, it becomes clear that the performance of the new process is comparable to that of conventional EPROMs. So the new ACE process yields parts that perform at least as well as conventional EPROMs.

The question then remains: how reliable are the ACE memories? In particular, how good are they at retaining data? To answer these and




**4. DATA INTEGRITY.** The contactless-array prototype EPROMs show excellent data retention for up to 3,000 hours at 200°C.

other questions, a comprehensive test program was undertaken.

Key aspects of floating-gate memory reliability—namely, thermally and electrically accelerated charge loss from the floating gate, and the impact of this charge loss on the performance of the chip—were evaluated by studying discrete floating gates as well as fully functional 64-K memories. TI scientists also studied the effects of electrical stress on the interlevel dielectrics—stress caused by the high voltages applied to the word lines during programming. A plot of threshold voltage versus word-line stress voltage (Fig. 3) shows that the oxide-nitride-oxide interlevel dielectric of the new ACE structure has good resistance to word-line stress for programming potentials up to 25 V.

TI also measured thermally accelerated charge loss for the prototype 64-K memories. Data retention was excellent for up to 3,000 hours at 200°C (Fig. 4). These and the other reliability data obtained have proved the viability of the ACE technique. □

## TI's CONTACTLESS EPROM PROVED TRICKY TO GET INTO SILICON

**There were times** when the designers of Texas Instruments Inc.'s new contactless-array erasable programmable read-only memories weren't sure they could come up with the goods. The new chips are a more economical, but much trickier, approach to EPROMs.

"One could see right off the bat that the new cell concept was attractive," says Pradeep Shah, product manager for EPROMs and static memories. "But we went through times where it looked as if it was just not feasible for large-scale integration. We were concerned over whether using a continuous buried n+ bit line would provide reliable programming." The TI engineers persevered, however, and proved they could implement the new design in an LSI chip.

**PRADEEP SHAH**

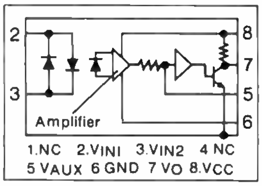
Shah gives credit to Texas Instrument development teams based in Dallas and Houston, including the VLSI Laboratory in Dallas headed by Jim Paterson, and in Houston a design team headed by Tim Coffman and a technology group under Manzur Gill. The basic cell technology goes back to a concept patented in 1979 by David McElroy, a scientist in Shah's group.

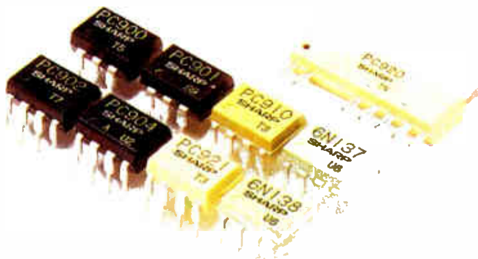
Shah believes the new cell and technology will have a dramatic impact on the share EPROMs will claim in nonvolatile-memory market share. He says the new cell promises to dramatically lower the size of circuits and the overall cost of EPROMs, reducing chip area by a third compared with conventional designs. "It also makes the EPROM more manufacturable, because we have taken the contacts out," Shah adds. He believes the development of the new structure, called ACE for array contactless EPROM, will help propel the market for ultraviolet-erasable memories past the billion-dollar mark.

Shah, who holds a BSEE with honors from the Indian Institute of Technology and a PhD in electrical engineering from Rice University, joined TI in 1973 as a member of the technical staff in the Semiconductor Research and Development Lab. Before transferring to MOS memory development, he was responsible for such diverse developments as TI's linear CMOS (LinCMOS), 74HC CMOS, and double-level-metal twin-well CMOS technologies

**For application-specific, specify Sharp OPIC.**

Sharp's unique opto-electronics technology and IC technology have been integrated to create the OPIC photocoupler with its own built-in circuitry.
Sharp developed this application-specific OPIC to better respond to rapidly diversifying needs.
The applications are ample and diverse, including high-speed digital transmission, programmable controllers, inverter air conditioners, switching power supplies, etc.
This leading-edge technology gives you enhanced performance, reduced product cost and compact/light-weight design.
Now you have an ally to help you to beat the competition.





# Choose your photocoupler as wisely as you choose your club.

● OPIC photocouplers/general purpose photocouplers

| Series | Model | Features | Applications |
|---|---|---|---|
| PC900 series | PC900 | Digital switching. Normal-off operation | Computers Programmable controllers. Measuring equipment. Numerical control machines |
| | PC901 | Digital switching. Normal-on operation | Computers. Programmable controllers. Measuring equipment. Numerical control machines |
| | PC902 | AC input. Built-in integration circuit | Programmable controllers. Telephones. Copiers |
| | PC904 | Built-in voltage deviation detection circuit | Switching power supplies |
| | PC910 | Ultra high speed(10Mb/s) | Computers. Programmable controllers. Copiers |
| | PC920 | For inverter control. Single-in-line package | Inverter air conditioners |
| | PC921 | For inverter control. Dual-in-line package | Inverter air conditioners |
| 6N series | 6N135 | High speed(1Mb/s) | Computers. Telephones. Measuring equipment. Numerical control machines |
| | 6N136 | High speed(1Mb/s) | Computers. Telephones. Measuring equipment. Numerical control machines |
| | 6N137 | Ultra high speed(10Mb/s) | Computers. Telephones |
| | 6N138 | Low input current. High sensitivity(CTR:300 % min.) | Computers. Telephones |
| | 6N139 | High sensitivity (CTR:500 % min.) | Computers. Telephones. Measuring equipment. Numerical control machines |


## OPIC PHOTOCOUPLERS

▶ OPIC is a registered trademark of Sharp and stands for Optical IC.

## SHARP

SHARP CORPORATION, JAPAN

**SHARP CORPORATION** Electronic Components Group. International Sales Dept.
22-22, Nagaike-cho, Abeno-ku, Osaka 545, JAPAN
Tel:(06)621-1221 Cable:LABOMET OSAKA Telex:J63428 Attn:OSKPA(LABOMET A-B)
**U.S.A.:SHARP ELECTRONICS CORPORATION** Electronic Components Division
Sharp Plaza, Mahwah, New Jersey 07430-2135, USA Tel:201-529-8757 Telex:426903(SHARPAM PARA)
**EUROPE:SHARP ELECTRONICS(EUROPE)GmbH** Electronic Components Dept.
Sonninstraße 3,2000 Hamburg 1, F.R. Germany Tel:(040)23775-0 Telex:2161867(HEEG D)

Circle 73 on reader service card

# How COMPAQ® advanced personal

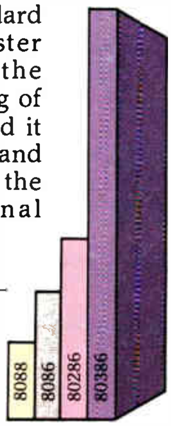

COMPAQ announces its biggest improvement yet to the industry standard—the new COMPAQ DESKPRO 386.™ It reaches far higher levels of speed, compatibility, performance and expandability than have ever been possible in personal computers. At the heart of this breakthrough is the new high-speed, 32-bit, 16-MHz Intel® 80386 microprocessor

## Introducing the new COMPAQ DESKPRO 386™

## The most advanced personal

# advanced-technology computers

that runs industry-standard software 2-3 times faster than ever before. But the chip is just the beginning of this story. We surrounded it with dozens of features and enhancements to create the most advanced personal computer in the world.




*The Intel 80386 microprocessor is faster and more powerful than its predecessors.*

## Each component the very best

Every component has been optimized to take advantage of the increased speed and power of the 80386. We offer, for instance, more storage, up to 130 Megabytes, with access times 50 to 150 percent faster than most computers. Plus you get the flexibility of up to four storage devices. But that's just the beginning.

We give you more memory. Enhanced color graphics. Even a built-in expanded memory manager that breaks the 640K barrier of current operating systems. We improved the keyboard, quadrupled the capacity of the internal fixed disk drive backup to 40 Megabytes and made it twice as fast as before, then went on to add a host of other features. Combined, they make this the first PC to offer a true minicomputer level of performance in a versatile, industry-standard desktop computer.

## The winning numbers

The new COMPAQ DESKPRO 386 features advanced 32-bit architecture that processes twice as much information as 16-bit computers in the same amount of time. Coupled with its impressive 16-MHz processing speed, it radically improves the responsiveness of spreadsheets, databases and networks as well as the ease of multi-tasking.

It runs thousands of business programs as well as all the popular engineering software, achieving an unparalleled level of performance, and making it a replacement for expensive dedicated engineering and scientific workstations.

And because it's so compatible, there's no other personal computer more connectable. As a result, you can use industry-standard expansion boards to network, communicate with mainframes and minicomputers, or even support several terminals.

## History in the making

The COMPAQ DESKPRO 386 combines superior technology with COMPAQ innovation to let you do things once thought impossible or impractical with PCs. There may be companies that copy one or two of its features, but it will be years before they can copy them all. It's clearly the computer of choice for today's *and* tomorrow's most demanding users. From the company with the highest user satisfaction ratings in the industry. For the Authorized Dealer nearest you, or to obtain a brochure, call 1-800-231-0900 and ask for Operator 27. In Canada, call 416-449-8741, Operator 27.


*Industry-standard software now performs 2-3 times faster than ever before.*

It simply works better.

# computer in the world

COMPAQ
DESKPRO 386™

# Master of Possibilities: John E. Hulse

Vice Chairman & CFO
Pacific Telesis Group

## Long distance or local, Pacific Telesis gets great reception with the MasterCard BusinessCard.

Pacific Telesis chose the new MasterCard BusinessCard™ because it is consistent with the company's philosophy . . . progress, intelligently planned. It's a philosophy Pacific Telesis is bringing to life in many ways–from providing quality phone service in California to operating a paging company in Thailand. And, it's a philosophy that warrants the best corporate card program possible.

Whether it's a technician in California or an executive in New York, the BusinessCard makes every employee's work easier. It's welcome in four times more places than any other corporate card and offers cash access at 110,000 locations.

The BusinessCard program enables Pacific Telesis to control business expenses with virtually no administrative effort. It offers individual credit limits and monitoring for each of the 12,000 cardholding employees at Pacific Telesis.

Finally, the BusinessCard offers unparalleled flexibility. The program was tailored for Pacific Telesis by its bank so the company chose services that were right for its business. In addition, each card carries the Pacific Telesis logo.

The distinctive silver BusinessCard is an investment in progress for Pacific Telesis. The program is helping the company live up to its corporate philosophy by keeping it in touch with all the possibilities.

For more information call 1-800-821-7700. Ext. 706


## Master The Business Possibilities™

# WIDEBAND GaAs OP AMPs PUSH ONTO SILICON'S TURF

Analog gallium arsenide integrated circuits from Anadigics Inc. are reaching into new territory for GaAs: wideband monolithic operational amplifiers. In fact, the two-year-old Warren, N. J., company is producing wideband GaAs op amps that almost match their silicon competitors.

Anadigics' latest product, the AOP3510, boasts a 350-MHz unity-gain bandwidth, a 70-MHz full-power bandwidth, a slew rate as high as 1,500 V/μs, and a 20-ns settling time. The leading performers among silicon monolithic and hybrid op amps exhibit unity-gain bandwidths of up to 400 MHz, full-power bandwidths of about 50 MHz, a slew rate of 1,000 V/μs in monolithic units and up to 3,000 V/μs in hybrid units, and settling times of 12 to 15 ns.

## TOPPING THE FASTEST

The internally compensated AOP3510 (figure) is based on a 1-μm depletion-mode metal-semiconductor FET technology with a 12-GHz frequency cutoff, $F_T$. It tops Anadigics' previous AOP1510, a 150-MHz chip that has been the fastest available GaAs op amp. It also has double the slew rate and full-power bandwidth of the 1510. In addition, its 20-mA output-current capability is three times greater, its 100-mV initial offset voltage is half as much, and its 30-μV/°C offset temperature coefficient is a third as great.

Anadigics is using the same process for the 3510 as it does for the 1510. To get the new level of performance, it improved the layout, redesigned the feedback compensation circuitry, incorporated larger output devices, used closer-matching FETs, and redesigned the temperature-compensation networks.

The new 350-MHz op amp is packaged in a 16-pin ceramic dual in-line package. It is intended for applications such as pre- and postamplifiers for analog-to-digital and digital-to-analog converters, fiber-optic local-area networks, driver preamps for cathode-ray tubes, radar and intermediate-fre-quency pulse converters, and high-speed sample-and-hold circuitry.

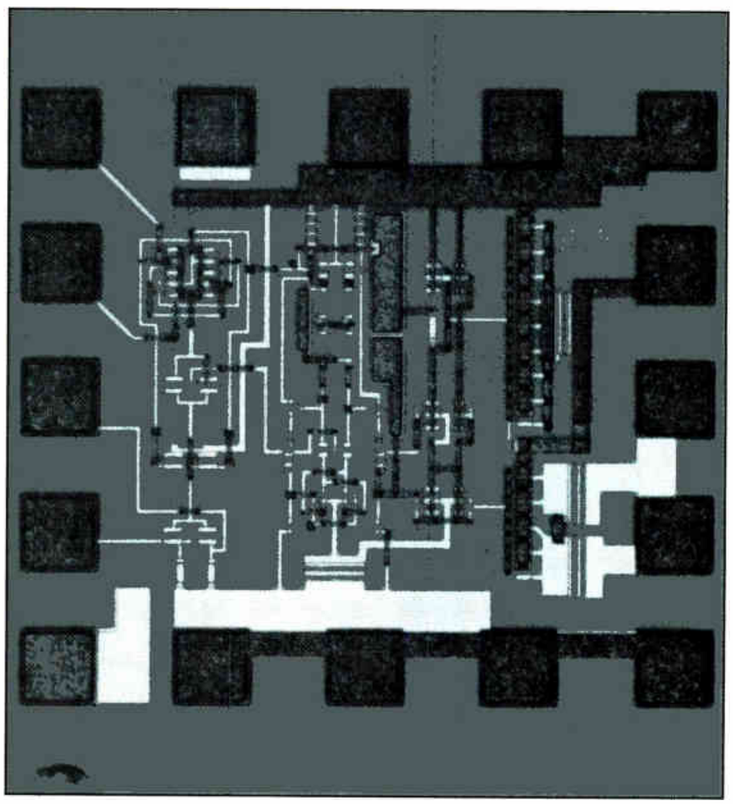
Anadigics has taken a very conservative approach in designing its new wideband op amp, says Michael Gagnon, director of sales and marketing. Even though the company has a GaAs process with 0.5-μm gate lengths that is capable of producing devices with a 24-GHz $F_T$, it decided to use its well-established 1-μm FET technology for its initial products. "As a matter of fact, the older process, with its 12-GHz frequency cutoff limit, still has plenty of growth potential for even wider bandwidth analog circuitry," Gagnon says. "Silicon wideband op amps, on the other hand, are based on transistors with frequency cutoffs of only 5 to 6 GHz, which severely limits any further bandwith expansion."

Anadigics surveyed the users of its earlier 150-MHz op amp and found that they were looking for design improvements such as increased bandwidth, more current drive, and better voltage-offset matching in any second-generation GaAs op amp. The findings of the survey tailored the design of the AOP3510.

Anadigics increased unity-gain bandwidth in two ways. First, it improved the layout in order to maximize bandwidth. The new layout minimizes lead lengths to cut parasitic inductances and capacitances—factors that limit the real bandwidth.

The company also reduced the internal frequency-compen-sation capacitor, which shapes the amplifier's open-loop response for optimum closed-loop stability. An analysis of the 150-MHz op-amp design showed it was overcompensated, and a smaller capacitor in the new AOP3510 would open up bandwidth further and still maintain an adequate stability margin.

The new GaAs op amp can put out 20 mA, compared with about 7 mA for the predecessor unit, because the size of the output transistors was increased. Boosting the size of the transis-



**SUPER AMP.** Anadigics's new GaAs op amp IC has a unity-gain bandwidth of 350 MHz—200 MHz more than its predecessor.

tors is an important step toward upping the full-power bandwidth. Gagnon notes, however, that this is an interim step toward Anadigics' goal of a 50-mA output-current capability.

Customer requests for reduced voltage offset were met by better matching of the input differential pair of FETs, resulting in a reduction in voltage offset from 200 mV to 100 mV. Anadigics has already installed active laser-trimming equipment, and its third-generation unity-gain op amp will incorporate trimmable thin-film resistors, reducing offset voltage even more.

At the same time, Anadigics designed an improved level-shifting current-mirror circuitry of the original amplifier. The new circuitry results in a reduced temperature coefficient of 30 μV/°C for the new unit, compared with about 90 μV/°C for the older amplifier.

Anadigics doesn't intend to stop here. Future op-amp designs with even greater unity-gain bandwidth based on the 0.5-μm process, greater drive capability, and lower offset voltages are in the works. These monolithic high-bandwidth op amps will use a more advanced ceramic flatpack rather than the current ceramic dual in-line package to allow full-rated performance from the new GaAs circuitry. Anadigics also has plans to build other types of GaAs chips that support data acquisition, such as comparators and sample-and-hold circuits. □

*TECHNOLOGY TO WATCH*

# A CRUCIAL STEP TOWARD ULTRA-FAST DATA PATHS

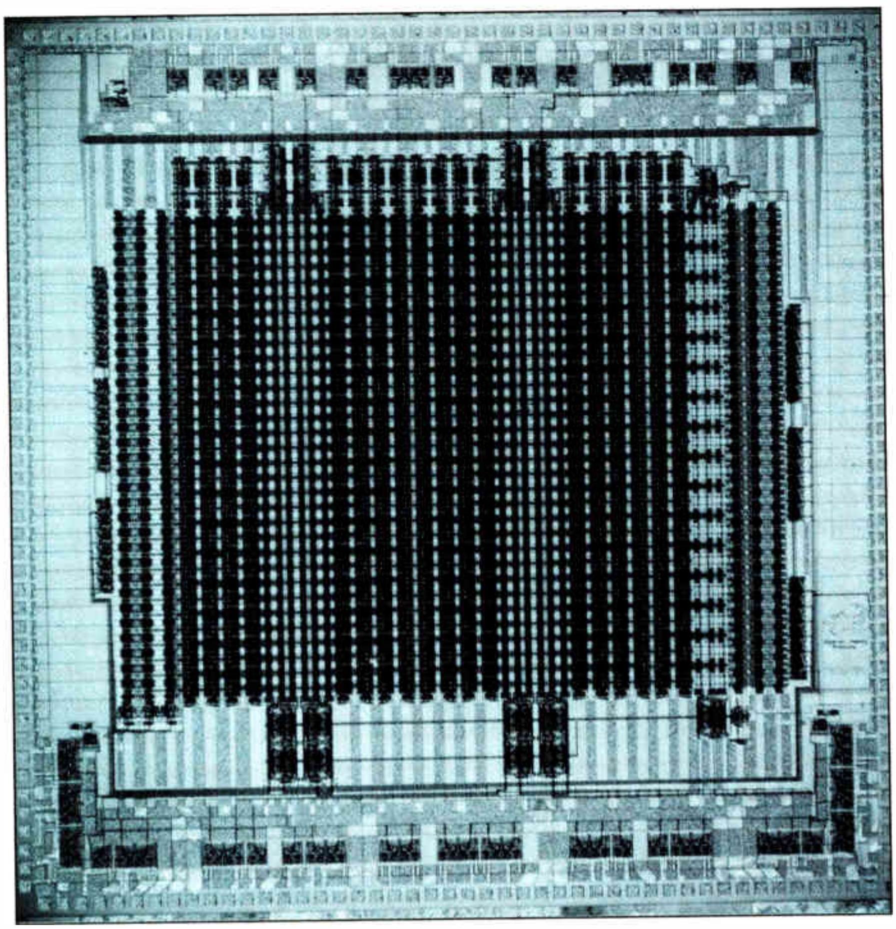
The crucial link in Bipolar Integrated Technology Inc.'s family of ultra-fast data-path elements is now in the sample stage. The new B3210 chip (figure) is a 1-K register file with a typical read-cycle time of only 6 ns. For faster swapping of the data in and out, it has five ports, one of which can be used for either input or output, and a set of six internal buses, three for writing and three for reading.

The 1-K register file is the critical element in the family, says company vice president Les Soltesz. "In most of the high-speed applications at which we are aiming this chip set—signal processing, graphics, and high-performance data processing—the choke point as it were, the element upon which the throughput of the entire system is dependent, is usually the register file and its ability to swap data in and out quickly."

The B3210, an emitter-coupled chip, has a power dissipation of 3.9 W and supports throughput rates as high as 100 MHz. Worst-case read-cycle time is 10 ns. A slightly slower version of the chip, the 15-ns B2210, is designed for applications requiring TTL compatibility and features a power dissipation of only 3 W.

Both parts are the most recent members in the Beaverton, Ore., company's family of ECL and TTL bipolar very large-scale integrated data-path elements that includes several 16-by-16-bit and 32-by-32-bit multipliers and multiplier accumulators introduced earlier this year [*Electronics*, April 7, 1986, p. 35]. The family also includes a powerful 32-bit IEEE-compatible 32-bit floating-point processor. All devices in the family are fabricated in the company's 2-μm BIT1 bipolar VLSI process featuring 14-μm$^2$ minimum transistor sizes and a cutoff frequency of 5 GHz.

No matter how fast the multipliers, accumulators, and arithmetic logic units in the system work, if



**QUICK CHIP.** The B3210 register file from Bipolar Integrated Technology has two input and two output ports and one input/output port.

data cannot be transferred in and out of memory at a fast enough rate, system throughput is reduced considerably. "Ideally, the best solution is a multiport memory; the more ports the better," says design engineer Bruce W. Rose. "However, because of pinout and power-dissipation limitations, choices are much more circumscribed."

The company's solution is a five-port register file, packaged in a 168-pin grid array, that under certain conditions looks to the system as if it were a six-port device. The B3210 incorporates a bidirectional read/write port, in addition to two read and two write ports. "Not only does this solve somewhat the pinout limitation, it also allows the device to more accurately match system requirements," says Soltesz. "Data-transfer requirements are seldom symmetrical, with exactly two streams of data coming in and two going out. The third bidirectional port is a backup, acting as an input or output port, depending on system requirements."

Each independently addressable port has separate read and write clocks to permit asynchronous concurrent access to the memory array. To support the simultaneous reading and writing of different address locations, the register file incorporates three independent write-address and data buses and three independent read-address and data buses.

Designed with a choice of transparent latches or edge-triggered registers for storing read addresses and data, the B3210 allows data to be written to and read from the same word in the same cycle. It feeds the result back to the inputs for additional processing. "Individual write and output enables on each port allow multiple registers to be cascaded to form deeper memory buffers," Soltesz says.

To support double-word operand accesses in floating-point calculations, an additional least-significant-bit address pin can be ORed with the LSB of the read, write, and read/write ports. According to Rose, this configuration is especially useful in transferring double-precision operands when the most and least significant words are at contiguous memory locations. Also, to reduce address- and data-setup time, the B3210 register file generates a write-enable pulse after data and address updates are clocked into the write-input registers.

The core cell of only 24 transistors is a major factor in producing the low power and small size of the B3210—43,000 transistors in a 290-by-290-mil die. The cell serves as the write-data multiplexer and read-data multiplexer, as well as the memory latch. It also allows newly written data to be written from an address location during the same clock cycle in which it was written. □

*TECHNOLOGY TO WATCH*

# A SPEEDY BOARD LAMINATE SUITS SURFACE MOUNTING

High-speed printed-circuit boards will get a charge out of a new polytetrafluoroethylene/ceramic laminate, Rogers Corp. says. The RO-2800, now being developed by the Rogers, Conn., company, not only will boost electrical performance for extremely high-speed multilayer pc-board applications, but the new laminate also is better suited to surface-mount applications than conventional pc-board materials, the company says.

The need for such laminates will grow as emitter-coupled logic and gallium-arsenide integrated circuits become more prevalent in high speed-computers, says David Arthur, Rogers' technical manager. He notes that with the high operating frequencies and short rise times of the new digital ICs, the electrical and physical properties of the pc-board substrate are even more critical.

Rogers' RO-2800 is a result of its High Speed Interconnections program [*Electronics*, Aug. 12, 1985, p. 46]. The material's low dielectric constant of 2.8 and low dissipation factor of 0.002 combine to greatly improve electrical performance over competitive laminates (table). It is these two characteristics that determine electrical performance. For example, signal-propagation delay decreases proportionately to the square root of the decrease in effective dielectric constant.

In addition, the RO-2800's low thermal coefficient of expansion and its compliance, which depends on its tensile modulus, make the laminate suitable for surface-mount assembly, a technique used in high-speed circuitry. Rogers engineers estimate that the cost of a finished RO-2800 board will be two to three times more than the same board fabricated in epoxy/glass.

The most frequently used pc-board materials for digitial applications are made of woven-glass-reinforced epoxy and polyimide materials. They have nominal dielectric constants of 4.8 and 4.5, respectively. Microfiberglass-reinforced PTFE laminates are typically used for microwave-circuit applications because they have dielectric constants of about 2.2. However, none of these materials is suitable for surface mounting of large ceramic leadless chip carriers because of their thermal mismatch with the alumina used for the carriers.

So substrate manufacturers have developed woven quartz- and Kevlar-reinforced polyimide laminates with TCEs low enough to suit many surface-mount applications. These materials also have low dielectric constants of 3.35 and 3.6, respectively.

With Rogers' RO-2800, however, a dielectric constant of 2.8 reduces propagation delays by as

SELECTED PROPERTIES OF PC-BOARD MATERIALS

| PCB material | Dielectric constant[1] | Dissipation factor[1] | TCE[2] (ppm/°C) | | Tensile modulus[1] (pounds/in.$^2$ x $10^6$) |
|---|---|---|---|---|---|
| | | | x-y axis | z axis | |
| PTFE* | 2.1[4] | 0.0004[4] | 224 | 224 | 0.05 |
| PTFE/microfiberglass | 2.2[4] | 0.0008[4] | 24 | 261 | 0.14 |
| RO-2800 | 2.8[4] | 0.002[4] | 19 | 24 | 0.06 |
| Polyimide/quartz | 3.35[3] | 0.005[3] | 6–8 | 34 | – |
| Polyimide/Kevlar | 3.6[3] | 0.008[3] | 3.4–6.7 | 83 | 4.0 |
| Polyimide/glass | 4.5[3] | 0.010[3] | 11.7–14.2 | 60 | 2.8 |
| Epoxy/glass | 4.8[3] | 0.022[3] | 12.8–16 | 189 | 2.5 |

*Polytetrafluoroethylene [1]measured at room temperature [2]measured from 0 to +125°C [3]measured at 1 MHz [4]measured at 10 GHz

much as 30%, compared with woven-glass-reinforced epoxy and polyimide materials, and by as much as 10% over the newer polyimide laminates reinforced with quartz or Kevlar fabric.

Another benefit of the RO-2800's low dielectric constant is a reduction in crosstalk. For instance, when the material is applied in a dual stripline configuration with a characteristic impedance of 50 Ω and 5-mil spacing, backward crosstalk with the RO-2800 is 2.7%, which compares with 4% in polyimide/quartz; 5% in polyimide/Kevlar, 6.6% in polyimide/glass, and 7.4% in epoxy/glass.

Unlike its competitors, the RO-2800 laminate maintains a low dissipation factor even up to 10 GHz. The result is a significant reduction in rise-time degradation: 40% less than polyimide/glass and 55% less than epoxy/glass. In general, the the RO-2800 performs significantly better at high frequency than any of its competitors, primarily because the dielectric constant and dissipation factors of these competitive materials (both single and composite) are much higher.

With its combination of a low tensile modulus and a low *x-y*-axis TCE, an RO-2800 board achieves the same solder-joint reliability as do thermally compensated boards that have copper-invar-copper cores, polyimide/Kevlar, or polyimide/quartz. That's one reason why RO-2800 boards work well with leadless ceramic chip carriers.

In addition, the TCE of the Rogers material along the *z*-axis is a third better than polyimide/quartz and about 3½ times better than polyimide/Kevlar. That translates into fewer strains on plated through-holes, which cuts down the potential for microcracks in the copper barrel of the holes. In fact, the TCE of the polytetrafluoroethylene/ceramic RO-2800 material is an order of magnitude better than that of straight PTFE and the microfiberglass-PTFE.

Layer-to-layer registration is a critical issue for makers of multilayer boards because it can affect yield. Sample multilayer boards with up to 12 layers fabricated from RO-2800 have proven more dimensionally stable than materials composed of woven reinforcement. For example, with conventional laminates, the effects of processing can cause impedance variations of as much as ±10%. With RO-2800, this variation can be almost halved, and the yield will improve.

Rogers has been working with several large electronics companies to evaluate boards made of its material. It has just delivered to one large company pairs of identical eight-layer evaluation test boards that will be loaded with leadless carriers and placed on both sides of a metal core. These units will then undergo thermal shock testing of their solder joints. □

TECHNOLOGY TO WATCH

# HOW IKOS MAKES IT EASIER TO SIMULATE ASIC DESIGNS

Validating the design of a complex application-specific integrated circuit can require a mind-boggling 100 million test vectors to simulate less than a second of operation. Because it takes so long to generate and to run these vectors, ASIC designs rarely are exercised as thoroughly as they should be. That's where the Ikos 800 from Ikos Systems Inc. comes in: it speeds up the creation of the vectors and then accelerates the simulation.

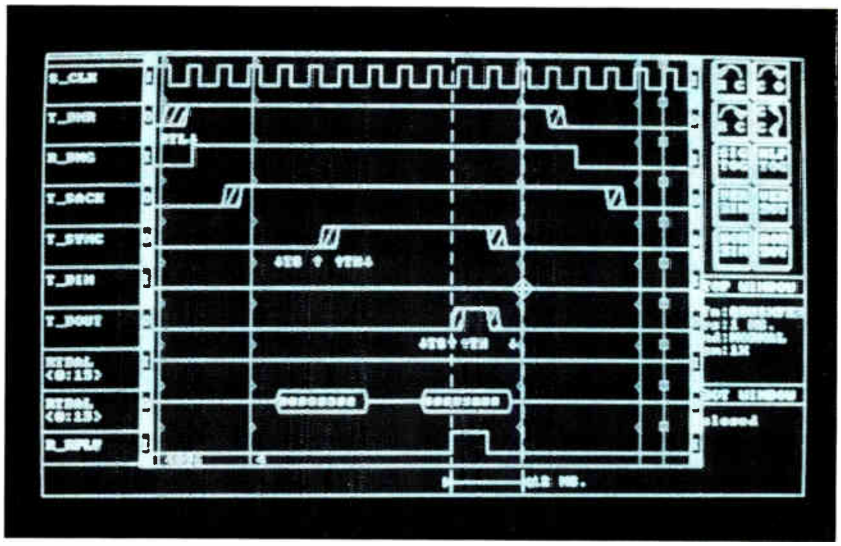
The Ikos 800 stimulus-processing hardware accelerator [*Electronics*, June 23, 1986, p. 68] uses an IBM Corp. Personal Computer AT, PC/XT, or most work stations as a front-end processor. The designer uses Ikos's Program Development Environment software and a graphics interface to enter a program that will generate enough test vectors to simulate seconds or even minutes of real-time operation. Writing such a program will take only minutes, as opposed to hours or even days in other simulation approaches. The $40,000 Ikos 800 is now in production.

Applying 100,000 test vectors to the software model of an application-specific IC operating at 20 MHz can simulate a mere 5 ms of real-time operation. Increasing the number of vectors by an order of magnitude only extends the simulation to 50 ms. "Ideally, the designer would like to simulate at least a few seconds of real-time chip operation," says William Loesch, Ikos president. "But to simulate one second of ASIC operation requires generating and processing 10 million to 100 million test vectors."

To speed the creation of up to 100 million test vectors, Ikos has developed the timing template, a stimulus-programming facility that lets the designer enter information graphically. Rather than writing test vectors one at a time, the designer creates a program by drawing a template consisting of representative timing diagrams (Figure). The Ikos stimulus processor then converts the waveforms into a test program. In this way, a small program can produce thousands of vectors.

In addition, the company has designed an accelerator that generates the test vectors on the fly as the simulation is running. "So there are two accelerators in the product: one that greatly speeds stimulus processing and a second that accelerates the execution of the simulation," says Loesch.

To create the program that the stimulus processor uses to generate the individual stimulus vectors, Ikos offers waveform capture, a screen-oriented, mouse-driven technique similar to schematic capture. With this technique, the ASIC designer graphically specifies timing relationships between signals by creating a timing template.



**STIMULUS SOURCE.** To create a test program, the ASIC designer creates a template on which he can specify the desired input and output waveforms.

The Ikos Program Development Environment software converts the resulting waveforms into a set of high-level commands that tell the accelerator how to generate a set of test vectors.

A critical requirement for generating large numbers of test vectors is the ability to separate stimulus timing from data. Timing relationships between control and data signals typically repeat in a hierarchical manner, as is easily seen when these relationships are analyzed without regard to data content.

In the Ikos 800, hierarchical timing relationships may be represented by an event stream entering a simulated ASIC if the data content is specified separately from timing signals. The data in the address field for the simulation can be generated by a hardware counter in the hardware accelerator, which is loaded to a preset value and incremented at a specified rate.

The data in the data field can be created by a random-number generator in the accelerator. To create a file containing values for each of these two fields, the designer can write a Pascal or C language program that generates up to 16-K words of address and data for the transfer. The accelerator hardware compiles these programs and inserts the resulting values in the appropriate place in the final stimulus pattern.

The Ikos 800 accelerator compares the simulation data with the expected data. The stimulus processor processes the timing template, interpreting the event stream as a program and allowing data substitution, loop control, subroutine calls, and other options.

The timing template for a disk controller's 16-K-word block transfer can be captured in less than 30 min. Within the inner loop are 86 events repeated four times for a total of 344 events per outer loop. The bus request/release cycle adds another six events, for a total of 350. The outer loop is repeated 4,096 times for the block transfer, which requires that 1,433,600 I/O events be processed for the simple DMA block transfer.

Assuming that the logic network stimulated by this stream contains 8,000 gates and that an average of 5% of these gates must be evaluated for each stimulus event, then the simulation of this network would necessarily result in 573,440,000 evaluations. However, this large number still represents less than 50 ms of real time. Moreover, this simulation has only checked the transfer of data from disk to computer.

## TIME CONSUMING

Another problem in simulating such a block transfer with the typical hardware accelerator is the amount of time it takes: more than an hour, compared with a few minutes with the Ikos 800. Each new address range would require another hour of simulation.

Moreover, Ikos recognizes that logic validation does not require detailed timing information. "Functional simulation can be accelerated to 10 million gate evaluations/s for about one-tenth the cost of accelerating detailed timing simulation to the same performance level," Loesch says.

This level of acceleration comes from using a pipeline in the Ikos 800. At the front of the pipeline is an event-queue manager, which works in two modes. In the timing mode, run time is equivalent to real-time operation of the final circuit. Event-queue management in this mode requires multiple memory cycles.

In the unit-delay mode, run time is not related to real-time operation. The algorithm is simple, and a single memory cycle is required. Because event-queue management is a separate stage, the mode can be easily switched from timing to unit-delay to perform logic validation. □

# Find out how good Business Class can be.

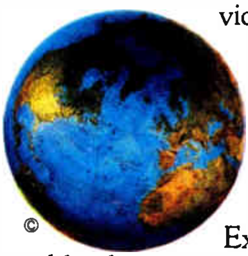
TWA


**TWA AND AMERICAN EXPRESS MEAN BUSINESS.** Discover the peace of mind that comes with TWA's Airport Express® service. TWA recommends you reserve and pay for your tickets ahead of time with the American Express® Card, and get your boarding passes even before you get to the airport.

Plus, Business Class travelers enjoy many other special services like priority luggage drop-off and pick-up.

**YOUR COMFORT IS OUR BUSINESS.** TWA goes to great lengths and widths to ensure your comfort with extra leg and shoulder room. And on our 747s, Business Class travelers can find themselves sitting in the lap of luxury in our spacious Business Lounger℠—the widest seat in the sky. And all of this special Business Class comfort is available not only across the Atlantic, but also on all TWA widebodies across America.

**AMERICAN EXPRESS INTRODUCES GLOBAL ASSIST.℠** Wherever business takes you, American Express' new Global Assist service provides worldwide emergency referrals. With one call, toll free, 24 hours a day, American Express will help Cardmembers find a lawyer, doctor, dentist, pharmacist, interpreter—or even suggest which visas or inoculations are needed for specific trips. And American Express has Travel Service Offices worldwide to help you with any changes in your travel plans.



©

**THE BEST TRAVEL AWARDS FOR FREQUENT FLYERS.** Only TWA offers frequent flyers the opportunity to earn a free trip for two, First Class, around the world, as well as free travel to a variety of exciting, exotic places. And members of TWA's Frequent Flight Bonus® program who travel Business Class will earn 25% bonus miles on every flight.

**THE IDEAL TRAVEL PARTNERS: TWA AND AMERICAN EXPRESS.** There's a new spirit and vitality at TWA and we're determined to make sure your Business Class travel goes as smoothly and conveniently as possible. To ensure this ease, TWA gladly accepts the American Express Card with its instant acceptance at TWA counters worldwide. Don't leave home without it.®

American Express Cards

**TODAY'S TWA. FIND OUT HOW GOOD WE REALLY ARE.**

PROBING THE NEWS

# THE ISSCC'S MENU RANGES FROM 4-Mb DRAMs TO GaAs MEMORIES

## WILL CONFEREES' PLATES OVERFLOW AT THE 1987 SOLID-STATE PARLEY?

*by Bernard Conrad Cole*

Down through the years at the International Solid State Circuits Conference, show-goers have learned that just one type of circuit will capture the attention of the industry at any given show. But engineers and designers will face a different situation when they gather in New York from Feb. 25 to 27 for the 1987 ISSCC. This time, their plates will be filled with a wide variety of technological morsels—a large number of them from Japan.

The buffet will range from 4-Mb dynamic random-access memories, megabit-level static RAMs, and a 4-Mb erasable programmable read-only memory to 32-bit central processing units using reduced-instruction-set principles, a host of other processor designs, almost two dozen analog designs, and gallium-arsenide memories as large as 16-K.

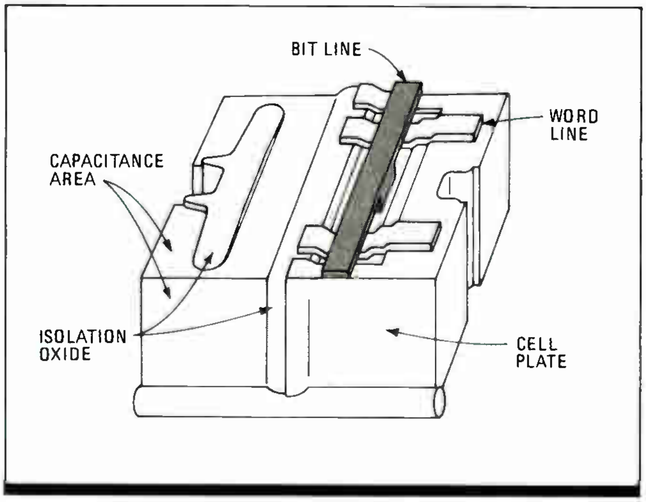
And, for researchers from the U.S., next year's ISSCC will serve up a good-sized portion of humble pie. Regardless of how firmly they believe in their continued technological leadership, they are going to be reminded once again that the Japanese are close to snatching that crown, at least insofar as participation in professional conferences such as the ISSCC is concerned.

According to Lewis Winner, the man who has been organizing the conference since the first one in 1958, a total of 104 papers were accepted, up from 85 in 1986. A significant number of those papers are Japanese—40 papers for 1987, up from 35 for 1986. There will be 48 U.S. papers.

Also, for the first time there will be four parallel sessions instead of the usual three. And in almost every session except those relating to analog circuitry and microprocessors, Japanese papers dominate in terms of quality.

In DRAMs, for example, three out of the four papers accepted to date on 4-Mb RAMs are from Japanese companies. Even in SRAMs, which U.S. firms have staked out as their own domain, the balance also favors the Japanese, who have contributed 9 of the 12 papers on this topic.

American companies are still holding firm in a few areas. Prime among them are microprocessors and digital signal processors. All the major papers on 32-bit general-purpose CPUs come from the U.S., and a total of only 6 out of the 20 papers on microprocessors and DSPs originate in Japan. U.S. companies are also holding their own in analog circuits, where only 5 out of 21 papers come from Japan.




**ISOLATED CAPACITANCE** Mistsubishi's 4-Mb 72.3-mm² DRAM uses an isolated capacitive cell with a folded bit line and adaptive sidewall.

**TOWARD MEGABITS.** Aside from the Japanese presence, the big news will be the growing trend in all memory types toward megabit densities. Leading the pack are DRAMs with a trio of 4-Mb circuits, including a 65-ns offering from Hitachi Ltd. of Tokyo; a 25-ns 1-Mb-by-4-bit device from IBM Corp.'s General Technology Division in Essex Junction, Vt.; and a 90-ns part from Mitsubishi Electric Corp. of Itami, Japan, that incorporates bonding options for either a 4-Mb-by-1-bit or 1-Mb-by-4-bit organization. It is based on an isolated capacitive cell with a folded bit line and adaptive sidewall structure. The cell (see figure) will be discussed at next month's International Electron Devices Meeting.

Also joining the megabit-memory club will be several SRAM and EPROM models, including:

- A 4-Mb SRAM from Oki Electric Industry Co.
- Two 1-Mb CMOS SRAMs—a 35-ns, 128-K-by-8-bit device from Sony Corp. in Kanagawa, Japan; and a 42-ns 128-K-by-8-bit SRAM from Hitachi.
- A 4-Mb CMOS EPROM from Toshiba Corp. in Kawasaki, Japan, with 120-ns access times and a programming rate of 10 µs per byte.

A plethora of advanced 32-bit microprocessor designs will also be featured—indeed, this ISSCC may well be remembered as the place where reduced-instruction-set computing came of age. Virtually every paper on 32-bit CPU design is devoted to the subject.

For example, AT&T Bell Laboratories at Murray Hill, N. J., has managed to cram 13-K of SRAM on a microprocessor. With about 172,000 transistors, the chip is fabricated using 1.5-µm CMOS and contains caches for a pre-fetch buffer, decoded instructions, and register stacks linked in three pipeline stages. And engineers from Digital Equipment Corp., Maynard, Mass., will describe a 180,000-transistor design that uses a 2-µm CMOS process. The processor incorporates a 32-bit RISC-type CPU onto the same 9.7-by-9.4-mm chip as 1 K of instruction and data cache and a 28-entry translation buffer.

From Hewlett-Packard Co.—whose Spectrum project is probably the best-known RISC development effort—will come two new 32-bit RISC offerings. Its Fort Collins, Colo., operation will report on a 15-million-instructions-per-second CPU using 2-µm n-MOS that has a direct hardware-instruction decode scheme and a three-stage pipelined execution architecture. Not to be outdone, the Palo Alto, Calif., facility of HP uses a 1.6-µm CMOS process to get 8 mips out of a 32-bit CPU with a 256-byte instruction cache and a 64-entry translation look-ahead buffer.

Stanford University researchers were more conservative; they used a 2-µm CMOS process with two layers of metal. Their RISC-based design features a five-stage pipeline that operates at 12 mips.

**MORE DIGITAL DELIGHTS.** Also on the digital side, among the highlights are:

- Two CMOS 32-bit Lisp processors. One, an 80,000-transistor device, is from the NTT Electrical Communications Laboratory in Tokyo; the other, a 553,000-transistor part, is from Texas Instruments Inc. in Dallas and features 114-K of on-chip SRAM.
- A massively parallel two-chip processor fabricated with 2-µm CMOS. This processor comes from DEC's Hudson, Mass., facility and uses 32 computing elements to achieve 320 million 4-bit operations per second.
- A 2-µm CMOS associative parallel processor with 256 computing elements on a single chip. This device, which is capable of executing 262 million 8-bit additions per second, is the result of research at Brunel University in Uxbridge, UK.
- Two 50-ns CMOS single-chip programmable digital signal processors. They are from AT&T Bell Laboratories of Holmdel, N. J., and Hitachi.
- A CMOS associative memory chip that is based on neural networks. This chip also comes from the AT&T Bell Laboratories in Holmdel.
- A 32-bit programmable arithmetic processor. From IBM France's Component Development Center in Corbeil-Essonnes, it is fabricated with 0.5-µm CMOS. The processor sports a 30-ns instruction-execution time and a 200-ps gate delay.

*Among the GaAs ICs are a 15-ns 16-K SRAM and a 6,000-gate array*

Among the standouts in the analog area are an eight-channel analog-to-digital interface processor from Microlinear Corp. of San Jose, Calif., whose unique feature is that it is algorithm-based. The processor is also self-calibrating and has 13-bit resolution.

Also eye-catching are two oversampling analog-to-digital converters. One is a 14-bit design from NEC Corp.; the other, a 16-bit chip from NTT. There is also a 350-MHz 8-bit flash ADC from Sony that consumes only 1.5 W. Linear Technology Corp. of Milpitas, Calif., will describe a switched-capacitor voltage converter that is made with a bipolar rather than a CMOS process, and Columbia University has an analog CMOS filter with full digital programmability.

Also vying for attention will be a number of major GaAs circuit introductions. Among the digital circuits is a 1-ns 4-K SRAM from Hitachi that dissipates 1.6 W and a 2-ns, 1-K SRAM with 210-mW active power consumption from Laboratoires d'Electronique et de Physique Appliquée in Limeil-Brévannes, France. Also described is a 16-K SRAM from Mitsubishi with a 15-ns access time and a 6,000-gate array from Toshiba, featuring a propagation delay of 284 ps per gate, that dissipates 1 mW per gate.

Among the analog GaAs circuits that will be described is a very-high-frequency/high-frequency GaAs monolithic front end from Laboratoires d'Electronique et de Physique Appliquée. It includes an automatic gain-control amplifier, two mixers, a voltage-controlled oscillator, a pair of amplifiers, and an active combiner.

Also described is a family of 5- to 300-MHz GaAs switched-capacitor circuits for video signal processing from Hughes Research Laboratories in Malibu, Calif., and the University of California, Los Angeles, and an 8-ns GaAs sample-and-hold amplifier from Anadigics Inc. in Warren, N. J. □

## THE KEY TOPICS AND PLAYERS AT ISSCC

### ANALOG CIRCUITS
- Anadigics
- Analog Devices
- AT&T Bell Laboratories
- Columbia University
- Laboratoires d'Electronique et de Physique Appliquée
- Hewlett-Packard Laboratories
- Hitachi
- Hughes Research Laboratories
- Linear Technology
- Microlinear
- Motorola

### DYNAMIC RAMs
- Hitachi
- IBM General Technology Division
- Mitsubishi Electric
- Oki Electric Industry
- Siemens

### GENERAL-PURPOSE CPUs AND PERIPHERALS
- AT&T Bell Laboratories
- Digital Equipment
- General Electric
- Hewlett-Packard
- Hitachi
- IBM Laboratories
- Mitsubishi
- NEC
- NTT Electrical Communications Laboratory
- Stanford University

### HIGH-SPEED LOGIC
- Fujitsu
- Hitachi
- IBM France
- National Semiconductor
- Toshiba

### NONVOLATILE MEMORY
- Fujitsu
- Seeq Technology
- Texas Instruments
- Toshiba

### SEMICUSTOM LOGIC AND GATE ARRAYS
- Fujitsu
- Mitsubishi
- Motorola
- NEC
- Toshiba

### SIGNAL PROCESSING
- AT&T Bell Laboratories
- General Electric
- Hitachi
- NEC
- Siemens
- Syracuse University
- Toshiba

### SPECIAL-PURPOSE CPUs
- Brunel University
- Digital Equipment
- General Electric
- Hitachi
- MIT Lincoln Laboratory
- NEC
- NTT
- Philips Research Laboratories
- Ruhr University
- Sony
- Texas Instruments
- University of California, Berkeley
- University of California, Los Angeles

### STATIC RAMs
- AT&T Bell Laboratories
- Laboratoires d'Electronique et de Physique Appliquée
- Fujitsu
- Hitachi
- IBM General Technology Division
- Mitsubishi
- Motorola
- Sony

# HOW COMPUTER MAKERS ARE MAKING THE MOST OF THE 80386

## THE KEY IS TO COMBINE IT WITH OTHER LEADING-EDGE PRODUCTS

*by Jonah McLeod*

**LAS VEGAS**

The onrush of computers based on Intel Corp.'s powerful new 80386 microprocessor is turning into a tidal wave—but it's due to more than the 32-bit chip. Computer makers are combining it with leading-edge graphics boards and software to create platforms for the long-awaited desktop work station.

It's no surprise that the 386-based machines were coming, because many observers see them answering the needs of what are called power users, those people who run out of processing speed, or disk space, or need better display resolution on existing personal-computer systems. What did surprise showgoers at the fall Comdex earlier this month in Las Vegas was the number of these machines that were introduced.

On display were the first of the 386-based machines soon to be flooding the market from well-known suppliers such as Compaq Computer Corp. and Convergent Technologies Inc. To those platforms, the original-equipment manufacturer can add graphics boards and monitors that provide resolution comparable to that of high-resolution graphics work stations. However, operating systems that fully exploit the chip are still needed. But already, "control programs," software that makes full use of the 80386 architecture, are becoming available. They will permit the power user to exploit such 80386 functionality as running multiple operating systems.

The Deskpro 386 from Compaq of Houston—the first to ship an 80386-based computer [*Electronics*, Sept. 18, 1986, p. 66]—is the archetype of many of the systems on display at Comdex. Most come with a 16-MHz 386 chip and 4 megabytes of random-access memory. All claim that 16 megabytes of RAM and 40 megabytes of Winchester disk storage will be available in the next three months, and most promise an 80-megabyte drive.

Some had brought versions of their products that contained high-speed static RAM to show the system at optimum performance. But these manufacturers admitted that the version they ship will use slower dynamic RAM instead of the faster—and costlier—SRAM. "Static RAM adds a couple thousand dollars to the cost of a system," says Richard Swingle, product manager at Compaq. "And in such a highly competitive marketplace, the cost penalty will put a competitor at a severe disadvantage."

To get the most out of their DRAM-based systems, manufacturers are using the faster static-column version with an average access time of 70 ns—still only half as fast as SRAMs. They also are using an instruction cache, so their systems run, on average, with less than one wait state.

Performance is critical not only for competitive reasons but because 386-based systems are going into computationally intensive applications. "There are five categories of applications for the 386-based systems," says Swingle. "They are: spreadsheets and data bases, computer-aided engineering and design, an inexpensive platform for developing artificial-intelligence applications, software development, and network file server."

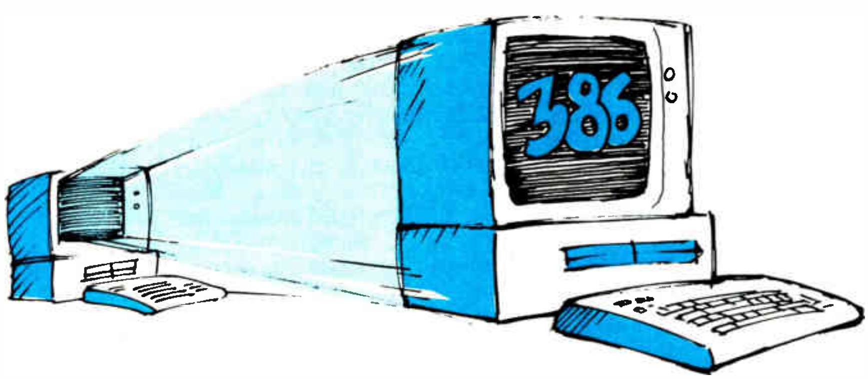
Each competitor is trying to distance itself from the others with particular technical features. PC Ltd. of Austin, Texas, calls attention to its basic board design, claiming a total of just 28 integrated circuits as opposed to the 170 chips on Compaq's. The key is that many of the 28 are application-specific ICs. The company also offers two package sizes, one comparable to the IBM PC AT and a second, smaller one about the size of the ITT Xtra. Another offering the same package sizes is MAD Intelligent Systems Inc. of San Jose, Calif., on its D3000.

For its part, Compaq points to its 5¼-in. Winchesters, which use the ESDI (extended small device interface) standard to achieve a data-transfer rate of 10 Mb/s. Zenith Data Systems Corp. of Glenview, Ill., highlights a backplane in its Z-386 PC that contains card slots for add-in cards built for the IBM PC, other slots for cards built for the PC AT, and even slots for cards built to the 32-bit-wide data bus of the 80386.

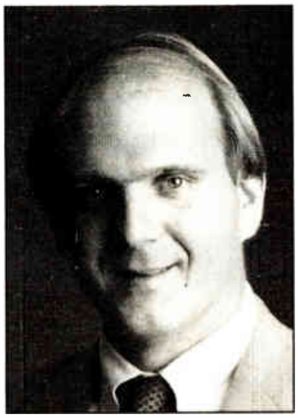
**GOING FOR GRAPHICS.** The board that seems most likely to find its way into the backplane of all these computers is a graphics-controller card tied to a higher-resolution monitor, for desktop publishing and CAE and CAD. Typical of the solutions offered is the Laserview Display Adapter from Sigma Designs Inc. of Fremont, Calif. The graphics controller card is used with the LM-15, a monochrome monitor offering 1,664-by-1,200-dot resolution from Princeton Graphics Systems Inc. of Princeton, N. J.

"This combination of higher-resolution graphics display and high-performance graphics controller offers the user a 150-dot/in. resolution. That's nearly twice the resolution of the IBM Extended Graphics Adapter (EGA) board and monitor," says Brad Fuller, manager of software development at Sigma Designs. That kind of resolution would have cost $4,000 to $5,000 a year ago. Now it can be had for $1,900 to $2,400 on a 15- or 19-in. monitor, respectively.

For twice the resolution available with the IBM EGA board, Sigma Designs has to write its own software drivers to various application programs such as AutoCAD, the popular design-automation software package from Autodesk Inc. of Sausalito, Calif. Fuller believes that the



386 chip will cure one big headache for application-program suppliers such as Autodesk: writing their software to use a standard user interface package such as MS Windows from Microsoft Corp. or GEM from Digital Research Inc.



**BALLMER:** Software vendors have "two absolute crying needs" in an operating system.

Up to now, application developers have shunned standard interfaces because even with the computing power of the 80286 CPU and graphics controllers, such packages made their software appear lethargic and unresponsive. With the more powerful 386, a standard user interface won't slow the system down appreciably.

Abetting that trend is the emergence of special graphics controller chips, especially the 82786 from Intel. "The chip does all the processing for any graphics operation, leaving the main CPU free to do other processing," says Mark Olson, product line manager for Intel's Microcomputer Group in Santa Clara, Calif.

Most graphics boards without a dedicated graphics controller are large dedicated RAMs serving as frame buffers. A graphics image to be displayed is moved into the frame buffer; any changes—for example, one window overlaying another—require that the main CPU overwrite the portion of the graphic that has changed with new data. With the 82786 and a large frame buffer, the processor can maintain several windows at a time. When the user merely switches between windows, the chip points to the section of the buffer containing the new window rather than writing a new image over the top of the old.

The Intel controller chip gives a big jump in graphics-processing speed. "A system containing an 80386 main CPU and 82786 coprocessor will run 4½ times faster than an 80286 with an EGA board," says Olson. "An 82786 in combination with the 80286 will run two times faster than a 286 with EGA board."

The Intel 80386-82786 combination at Comdex was a demonstration system not for sale. However, Pepper Plus, from Number Nine Computer Corp. of Cambridge, Mass., an 82786-based graphics controller card that can work with the 80386, will be ready in January.

Nevertheless, even with a powerful CPU and high-resolution graphics, one piece of the picture of a powerful work station is still missing: an operating system that matches this high-performance machine. No one is more conscious of the demand for more functionality than Microsoft, progenitor of DOS for the personal computer.

"We see two absolute crying needs from independent software vendors," says Steve Ballmer, vice president of system software for the Bellevue, Wash, company. "First, they want to see the DOS platform expand to enable individual applications and systems of applications to use more memory [beyond the current 640-K limit of DOS]. Second, they would like to see the platform expanded to be multitasking." In addition, any new version of DOS must be compatible with the current version.

Ballmer won't say what Microsoft has planned to meet these demands. But Therese Meyers, president of Quarterdeck Office Systems in Santa Monica, Calif., has her own solution.

"Don't forget DOS 3.2, since it is all we have to work with at present," she says. "There have been enhancements to 3.2 that have extended the capability of DOS to deal with the problems at hand. One is expanded memory that has come via the LIM (Lotus-Intel-Microsoft expanded memory specification) spec," which boosts the DOS memory limit to 8 megabytes. Intel says there are 150 programs using expanded memory.

**COLVIN:** Control software opens the door to a host of 386 operating-system add-ons.

"The second enhancement was enhanced expanded memory, which allows the software developer to run multiple programs," says Meyers. "The third enhancement is the 386 virtual-machine architecture, so you can have control programs that cross the memory boundary. As we wait for DOS 5.0 or other operating systems that will give us the long-awaited multitasking and expanded memory for real, these three enhancements will do in the meantime."

Another way of adding functionality to operating systems for 386-based machines is control software. It commands the hardware to alter its configuration—for example, from a segmented to a linear address-space architecture. "Developers are looking at everything from emulating the LIM standard on the linear address space, to doing hot-key switching between multiple resident programs in memory, to doing full virtual-machine environments of multiple operating systems running side by side simultaneously in the machine with multiple tasks running under each of the operating systems," says Neil Colvin, president of Phoenix Technologies Ltd. of Norwood, Mass.

One of the first to use control software to implement full virtual-machine environments of multiple operating systems is Convergent Technologies on its Ngen work station [*Electronics*, Nov. 13, 1986, p. 63]. The Santa Clara, Calif., company demonstrated at Comdex a 386-based system running its own CTOS operating system, MS DOS, and Unix on the same work station simultaneously. Moreover, the user can switch between each of the three environments with a single keystroke.

Quarterdeck Office Systems is using control software to switch between multiple resident programs in memory. "We have a program called DesqView Version 1.3 that runs on the Compaq Deskpro 386 that allows the user to run multiple DOS sessions, each executing an application program such as Lotus 1-2-3 or Wordstar," says Meyers. "To be able to run on various machines besides the Compaq, we have our own expanded memory-management software."

The opportunity for control software is also attracting The Software Link Inc. of Atlanta. "Our approach in the PC MOS 386 software product is to provide multiple sessions of DOS in which one re-entrant operating system controls multiple-user sessions simultaneously," says Gary Robertson, director of sales and marketing for the company. "The sessions can be local to one user [multitasking], or they can be assigned to inexpensive ASCII terminals so you have a multiuser operating system running concurrently."

All this synergy flowing from the 386 is causing an explosive new market to develop around the new microprocessor. In fact, Andrew Seybold, president of the Seybold Group in Torrance, Calif., says that it is too bad the 386 is overwhelming the 80286 market before it has had a chance to fully develop.

But his sadness isn't shared by Intel. David House, the company's vice president and general manager of the Microcomputer Group, says there is an installed base of 2 million 286-based systems from more than 50 companies, and he expects another 5 million to 6 million will be shipped in the next 12 months. Add to that the way the 386 is coming on so fast and gaining such quick acceptance, and the picture is one of the people at Intel worrying about the 286 all the way to the bank. □

# NEW PRODUCTS

# AMD'S PERIPHERAL CONTROLLER EXPANDS, SQUEEZES IMAGE DATA

## CHIP ADDRESSES STORAGE AND HIGH-SPEED TRANSMISSION PROBLEMS

Advanced Micro Devices Inc. has adopted a technique from facsimile technology to create a peripheral controller chip that can compress bit-mapped data for storage and transmission or, at the same time, expand data for display and printing.

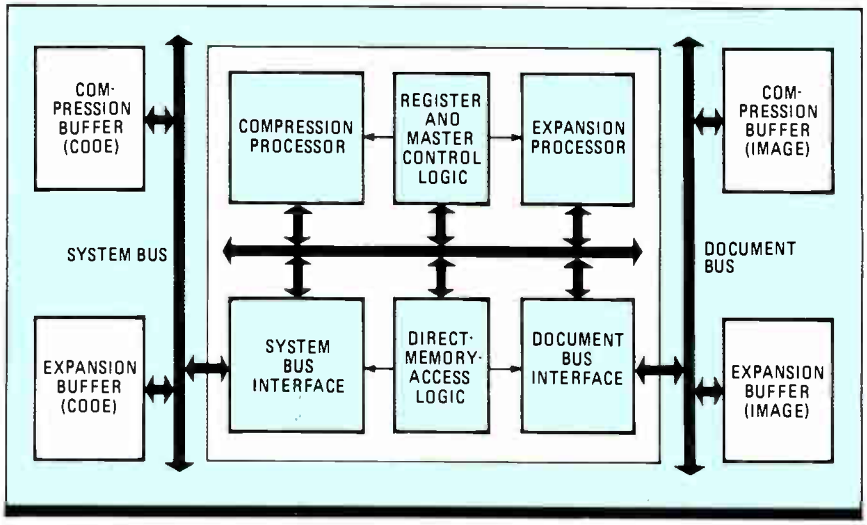
In creating the Am7971, AMD addressed the immense demands that high-density digitization places on system storage and transmission channels. At a scanner resolution of 300 dots/in., for example, an 80-in.$^2$ image would require 7.2 Mb of disk storage and a high-speed network to make transmission practical.

**FAX PROTOCOLS.** AMD adopted the standard Group III and IV facsimile protocols developed by the International Consultative Committee on Telegraphy and Telephony, says Steven Dines, strategic marketing manager for logic products. Group III standards are used in most current facsimile systems; Group IV is intended for next-generation digital systems. Both employ modified Huffman run-length encoding, in which a string of similar picture elements can be described by the length of a run. In such protocols, Dines says, the compression ratio is quite data-dependent. AMD claims compression ranging from 5:1 to 50:1 for the 7971.

The chip can be part of an optical file server or an intelligent copier. It interfaces between document memory or an input scanner and the rest of the system. "It's like back-to-back direct-memory-access chips with compression and expansion in between," Dines says.

Two-dimensional encoding can be done by comparing each line of a scan with a reference line, with new reference lines determined at programmable intervals. The 2-D coding gives a greater compression ratio, but it sacrifices encoding speed and is more prone to error.

The chip recognizes boundaries on a single picture element when it is used for displaying data on a video screen. A video display may not have the same resolution as the original image, but the compression algorithm loses none of the original information, and the image may be printed out at the original resolution.




**FULL DUPLEX.** Data may be simultaneously compressed and expanded for storage and display.

Document page width is programmable up to 16,000 pixels, AMD says, so that even at 400 dots/in., the 7971 can process documents 3.4 ft. wide.

Page-width checks are part of the chip's error-detection system, since illegal line widths and negative run lengths indicate incorrect data. Error recovery is possible with minimal intervention by the central processor, AMD says. The chip has 44 user-programmable registers and a dual-bus architecture that permits independent access by system components over the system bus and document access over a document-store bus. Full-duplex operation is possible, with compression and expansion of data taking place simultaneously in different directions. Future chips will address filtering problems inherent when peripherals vary widely in resolution.

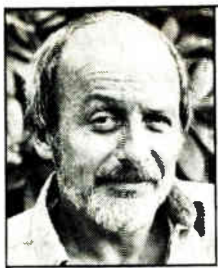
The chip is fabricated with AMD's n-MOS process. It is packaged in 68-pin leaded chip carriers or pin-grid arrays. In 100-lot quantities, the leaded-chip-carrier version costs $142.86 each; the pin-grid-array package costs $166.67. Both are scheduled for full production Dec. 1.

Advanced Micro Devices Inc., 901 Thompson Place, Sunnyvale, Calif. 94088.
Phone (408) 732-2400 [Circle 361]

# MOSTEK ADDS A CLOCK TO ITS ZEROPOWER SRAM

Thomson Components Mostek Corp. has added a real-time clock circuit to its CMOS 2-K-by-8-bit Zeropower nonvolatile SRAM chip. Besides storing backup data during system power interrupts, the chip now keeps track of elapsed time. When power is restored, the MK48T02 Zeropower Timekeeper can tell the computer the precise time when processing ceased.

Besides tracking elapsed hours, minutes, and seconds, the device also records year, month, and day data. This information is held in what Mostek calls Timekeeper registers, which are constructed from dual-port SRAM cells. Control circuits dump the time-related data from clock counters into the register. Since the on-chip clock is read in the same manner that byte-wide SRAMs are


E.L. DOCTOROW


NANCY MILFORD


HERMAN WOUK


THEODORE H. WHITE

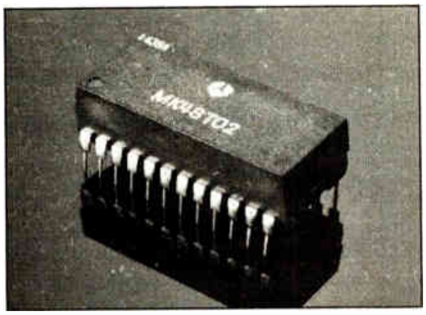


accessed, Mostek utilizes the dual-ported SRAMs to keep the once-a-second update from impeding access to the chip's 2-K-by-8-bit memory.

The Zeropower Timekeeper also features software-controlled calibration that periodically corrects the clock counter by adding or deleting pulses to the timing chain. Calibration may be set by comparing the clock's time with a known reference or by measuring the frequency of the circuit's clock chain.

A lithium battery cell housed inside the Timekeeper's 24-pin dual in-line package automatically powers the quartz oscillator-controlled clock and maintains the backup data stored in the memory array.

The clock will maintain accuracy within one minute over a month at 25° C




**SAFETY NET.** Mostek's SRAM chip keeps track of time during power outages.

without calibration. The predicted typical life of the lithium carbon monofluoride battery cell is 38 years at 25° C. The clock will typically operate 31,500 hours in the battery-backup mode at that temperature, according to Mostek product representatives.

The Timekeeper's quartz oscillator runs at a nominal frequency of 32.768 MHz. The 48T02's crystal, like the lithium carbon monofluoride battery cell, is contained in the top hat of the DIP, which conforms to the Jedec pinout for memories that output data 8 bits at a time.

**SAFETY RANGE.** The chip's power-failure-detection circuit tracks supply voltage and switches the memory and clock to battery backup whenever input power deviates from an acceptable range. Normal operating voltage is 5 V. The 48T02 will switch on the battery power whenever the system power supply falls within a range of 4.75 to 4.50 V. A variant of the chip—the 48T12—has a trigger range of 4.5 to 4.2 V.

Active maximum power dissipation of the part is 80 mA. With the clock running, the chip has a maximum standby current of 1.4 μA. The clock may be turned off with a stop bit, cutting power dissipation to 300 nA at 70° C. The Timekeeper resides on a die measuring 183 by 254 mils. Its ambient operating temperature range is 0°C to 70°C.

In 100-piece quantities, the 48T02 Zeropower Timekeeper with 120-ns access time sells for $25.83 each, or with 150-ns speeds for $19.86 each. The price with 200-ns speeds is $15.87 each, and with 250-ns speed the chips cost $16.29 each. The devices are available now.

*– J. Robert Lineback*

Thomson Components Mostek Corp., 1310 Electronics Dr., Carrollton, Texas 75006. Phone (214) 466-6000 [Circle 360]

## CMOS LOGIC FAMILY OFFERS 5-ns DELAYS

A family of high-speed CMOS logic parts from Integrated Device Technology Inc. offers the fastest TTL-compatible logic available, the company claims. An 8-bit buffer in the FCT-A family boasts a propagation delay of 4.3 ns in a circuit running on a 10-MHz clock; the average delay for the family is 5 ns.

In comparison, the 8-bit buffer in Fairchild Semiconductor Inc.'s FAST bipolar logic family offers a 6.3-ns propagation delay under similar conditions.

The FCT-A family comprises 17 logic circuits, including dual decoders, one-of-eight decoders, sychronous binary counters, 8-bit comparators, and 8-bit shift registers. IDC expects to add five more parts before year end.

Typical power consumption for the parts is 10 mW per device—significantly lower than that of bipolar devices.

Fabricated in IDT's proprietary 1.2-μm CEMOS technology, the chips are well-suited for high-performance applications such as high-speed graphics, instrumentation, and test equipment, the company says. IDT offers industry-standard 5400/7400 logic-family I/O electrical specifications and pinouts, including hermetic 16-, 20-, and 24-pin DIPs and plastic 16- and 20-pin small-outline ICs.

The chips are available now. Prices begin at $2.65 for the IDT74CT374A 8-bit register in lots of 100 or more plastic DIPs.

Integrated Device Technology Inc., 3236 Scott Blvd., Santa Clara, Calif. 95054. Phone (408) 727-6116 [Circle 365]

## XILINX HIKES DENSITY OF ITS GATE ARRAYS

A user-programmable gate array from Xilinx Inc. contains the equivalent of 1,800 two-input NAND gates—50% greater density than its 1,200-gate devices released last year. They have three user-programmable elements: input/output blocks, configurable logic blocks, and interconnections.

The I/O blocks can support two independent 32-bit buses and can be defined on a pin-by-pin basis as output, input, bidirectional, or three-state. Users inter-

# Canon presents your personal print shop.


### Here's the laser beam printer from the company that pioneered desktop laser beam printing.

From the shortest memo to the longest report, the Canon LBP-8 A1 makes everything you print look hot off the presses. Your output will look so professional you'll think it came from a print shop.

The LBP-8 A1 is incredibly fast, producing copy at a rate of 8 pages per minute, and because it's non-impact, it prints so quietly that you'll hardly know it's working.

This versatile printer lets you use a wide range of plug-in fonts. And Canon's replaceable cartridge system makes it virtually maintenance-free.

To set up your own personal print shop, get the Canon LBP-8 A1, or the LBP-8 A2 with full graphics capability. You're sure to make a favorable impression with everything you print. To learn more about Canon's advanced laser beam printers as well as the complete line of wire dot matrix and bubble-jet printers, call 1-800-453-3307. (In Utah, 1-800-662-2500.)

**Canon®**
**PRINTERS**
**Printouts that stand out.**

Canon U.S.A., Inc., Printer Division, P.O. Box 619865, Dallas/Fort Worth Airport, Texas 75261. © 1986 Canon U.S.A., Inc. Printility is a product of Metro Software Inc.

Circle 89 on reader service card

connect the configurable logic blocks to build higher-level logic functions.

Routing of internal signals and the configuration of I/O logic blocks is controlled by a configuration program stored in an internal CMOS SRAM. During power-up, the program is loaded into the chip from a storage device such as an EPROM, or under microprocessor control from a disk. Xilinx fabricates its XC 2018 Logic Cell Array using a 1.5-$\mu$m, two-layer-metal CMOS process.

Xilinx also enhanced its development software. The company claims its XACT development system, a complete personal-computer-based gate-array system, will enable engineers to bring their products to market in less than half the time required for conventional gate arrays. In production volumes, prices on the XC 2018 start at $15 each. The XACT system costs $3,600, and hardware and software are now available.

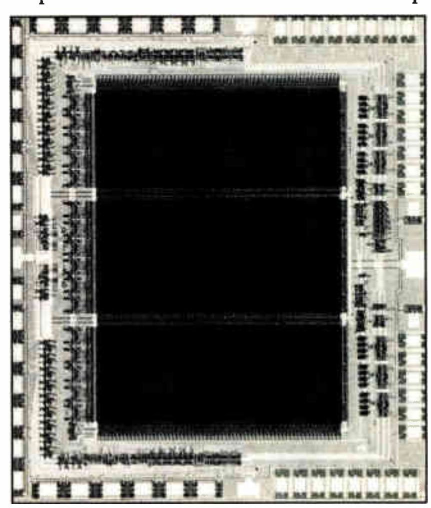
Xilinx Inc., 2069 Hamilton Ave., San Jose, Calif. 95125.
Phone (408) 559-7778 [Circle 366]

## SRAM CAN HANDLE 8- OR 16-BIT WORDS

A dual-port static RAM chip by VLSI Technology Inc.'s Application-Specific Memory Products Division could make communication problems between systems with different word sizes a thing of the past.

The device is intended for use in applications in which a multiplexed address/data bus is used. The VT16AM8 1-K-by-16-bit, 2-K-by-8-bit dual-port RAM has its left port organized as 1,024 16-bit words and its right port organized as 2,048 8-bit words. This scheme enables simultaneous, independent access by both 8-bit and 16-bit microprocessors.

The VT16AM8 also provides a single-chip solution for such applications as interfacing a 16-bit host with 8-bit peripherals, a task that has required a system designer to either design a custom chip or else add on an extra multi-chip



board. VLSI Technology is marketing the new chip in the first quarter of 1987 for $55.10 each in OEM quantities.

VLSI Technology Inc., Application-Specific Memory Products Division, 1100 McKay Dr., San Jose, Calif. 95131.
Phone (408) 434-3000 [Circle 367]

## SELF-CALIBRATING ADC SAMPLES AT 50 KHz

Crystal Semiconductor Corp.'s 14-bit CMOS self-calibrating data converter targets high-resolution analog-to-digital conversion for such applications as robotics, process control, and signal processing. Incorporating a conversion and calibration microcontroller, clock, comparator, control I/O, and self-calibration circuitry on a single chip, the CS5014 provides 14-bit digital representation of a bipolar or unipolar analog signal at sampling rates up to 50 KHz. Self-calibration is performed using a binary weighted-capacitor array, with each capacitor consisting of a subarray of capacitors that can be configured to adjust a particular bit weight. This process achieves a maximum nonlinearity of ½ least-significant bit and no missing


codes at 14 bits. Additional features include 16-ms conversion and 150 mW power dissipation. Samples of the CS5014 are available this month at a cost of $45 each in quantities of 100.

Crystal Semiconductor Corp., P.O. Box 17847, Austin, Texas 78760.
Phone (512) 445-7222 [Circle 368]

## CYPRESS TO OFFER DIAGNOSTIC PROMS

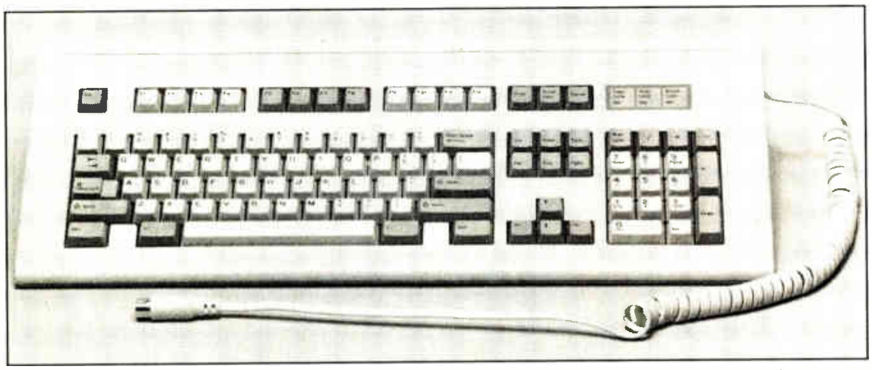
Cypress Semiconductor Corp.'s CY7C268 and CY7C269 are 8-K-by-8-bit diagnostic PROMs fabricated in CMOS technology that offer low power consumption and high density.

The 32-pin CY7C269 has two independent clocks, enabling it to perform diagnostics simultaneously with operation. The 28-pin CY7C268 has only one clock. Applications include military electronics, telecommunications, and instrumentation. Both chips are now in production and available in OEM quantities with a 10- to 12-week lead time. Prices vary with the address setup time, which can be 40, 50, or 60 ns.

Cypress Semiconductor Corp., 3901 N. First St., San Jose, Calif. 95134.
Phone (408) 943-2600 [Circle 369]

# EASY-TO-USE KEYBOARD FOR PCs WORKS SILENTLY

## MICROWITCH'S REARRANGED KEYS DUPLICATE THE NEWEST IBM OFFERING WHILE PROVIDING TACTILE FEEDBACK



**VERSATILE.** Keyboard connects to PCs or mainframes by changing the interface plug.

Honeywell Inc.'s Micro Switch Division has rearranged key placements and used light-emitting diodes to make its plug-compatible replacement keyboard for the IBM Personal Computer XT and AT easier to use.

The 101ST13-14E duplicates the key layout of IBM Corp.'s most recent 101-key products. But it also employs Micro Switch's capacitive-membrane technology to make the keys work silently while providing tactile feedback to the operator, according to Mark Tiddens, Micro Switch's keyboard products manager.

**SENSITIVITY.** Tactile feedback lets operators know when they have completed an entry, and since high-speed typists can depress three keys within 9 ms, feedback can increase productivity substantially. Independent studies indicate that operators generally prefer silent operation to the metallic click that is characteristic of many tactile-feedback keyboards, says Tiddens, particularly in applications such as data entry where many operators are working in close proximity. Micro Switch also offers a noise generator as an option.

In the revised keyboard layout, the cursor is controlled by four single-purpose keys in an inverted-T configuration at the lower right side of the board, which allows quicker, less ambiguous access to the keys. Many competing keyboards arrange the cursor-control keypads within an array of function or numeric keys, which can lead to a neighboring key being actuated in error.

LEDs situated in the upper-right portion of the board give users a clear signal of the status of the "caps lock," "num lock" and "scroll lock" keys. The number of function keys has been increased from 10 on the old keyboard to 12, and the keys have been moved to form a single line across the top of the panel to improve operator recognition. The additional keys' shift mode can be used to duplicate the functionality of a 122-key board.

Micro Switch also followed IBM's lead by fabricating the keyboard so its functional unit is distinct from the housing. This means it can be used either with PCs or as a terminal on a host computer simply by changing the interface plug, says Tiddens.

An interface cable and two-year warranty are included in the package, and an IBM interface is offered as an option. The keyboard housing is a high-strength, injection-molded enclosure with a matte white finish and a two-position height adjustment. The 101ST13-14E conforms to European ergonomic standards. It will become available in January for $180 in single-unit sales and for less than $70 in orders of 1,000. *–Jack Shandle*

Micro Switch Division, Honeywell Inc., 11 W. Spring St., Freeport, Ill. 61032.
Phone (815) 235-6600 [Circle 400]

## PC BOARD SUITS VMEBUS, MULTIBUS II

Mupac Corp.'s four-layer, wire-wrap pc board is designed to meet the growing need for circuit boards that conform to the Eurocard 96-pin DIN/IEC standard that is implemented in VMEbus and Multibus II. The HVU Hybrid is engineered to accommodate 0.3-in devices in the holes parallel to its height and 0.6-in. devices in the holes parallel to its width. It holds up to 132 of the 0.3-in. devices and 49 of the 0.6-in. devices.

It is available for Mupac's Metric bus applications as well as for Multibus II and VMEbus. The HVU Hybrid is Schottky-compatible.

The construction of the 233.35-mm-by-160-mm pc board promotes current flow by decreasing resistance across the surface of any of the four layers by 60%, which results in a corresponding increase in current-carrying capacity. Plated through-holes are placed every 0.200 in. to provide capacitive decoupling.

The board also features rows of low-insertion-force pins on 0.100-in. centers for pin-grid-array devices, as well as vertical rows of socket terminals alternating on 0.100-in. and 0.300-in. centers for high-density packaging of devices. Horizontal rows on 0.100-in. and 0.600-in. centers also aid in packaging density. Custom power provisions are offered for most 96-pin DIN connectors.

Mupac's HVU Hybrid is available now; prices start at $572.

Mupac Corp., 10 Mupac Dr., P.O. Box 3099, Brockton, Mass. 02410.
Phone (617) 588-6110 [Circle 406]

## LEAD BATTERIES ARE MAINTENANCE-FREE

Gates Energy Products Inc. has applied its starved-electrolyte, gas-recombination technology to a line of maintenance-free flat-plate batteries. The SBS family of sealed lead-acid batteries targets such applications as telecommunications, uninterruptible power supplies, and cable TV systems.

The family includes four configurations: the SBS 30, with a capacity of 26

Ah; the SBS 40, with 35 Ah; the SBS 110, with 100 Ah; and the SBS 300, with 300 Ah. Traditionally, batteries in this range have been flooded lead-acid or nickel-cadmium energy cells, which require maintenance—and which, because of their corrosive electrolyte, necessitate special mounting and handling.

Gates' patented sealed-recombination-battery technology has been used in the past decade to make batteries smaller. Now, by adapting the technology to a new flat-plate design, Gates is now able to manufacture larger batteries in industry-standard configurations.

Models 110 and 300 will cost $140 and

# Count on OKI to expand your CMOS CSIC options.

# Gate Arrays

| 1.5-micron 70V000 Series VERY HIGH SPEED # Gates | # I/Os | & 2-micron 70H000 Series HIGH SPEED # Gates | # I/Os | 3-micron 70000 Series # Gates | # I/Os |
|---|---|---|---|---|---|
| 700 | 66 | 3289 | 86 | 387 | 44 |
| 1000 | 66 | 4290 | 104 | 720 | 62 |
| 1500 | 66 | 6000 | 130 | 1445 | 88 |
| 2000 | 80 | 8024 | 148 | 2000 | 106 |
| 2500 | 80 | 10008 | 172 | 4205 | 120 |

Gate Arrays
OKI CMOS

**NOW:** Expanded Gate Array options from OKI, supported by world-class CSIC capabilities.

**Expanded** product families and packaging. For more cost-effective, more flexible single-chip logic integration, OKI supplies more pre-designed Gate Array options—in the most advanced package types: plastic or ceramic through-hole DIPs or pin grid arrays; or plastic surface-mount PLCC or flatpack.

**Expanded** services, plus world-leading production automation. OKI CSIC* design expertise is accessible at any development stage. And OKI's CSIC manufacturing/testing facilities—among the world's most highly automated—assure high quality, high volume fabrication.

*Customer-Specific Integrated Circuit

For RFQ or technical data, complete form below and return to: CSIC Marketing, OKI Semiconductor, 650 N. Mary Ave., Sunnyvale, CA 94086. (408) 720-1900.

## RFQ
Request for Quote

## OKI CMOS Gate Arrays

For prompt response to your Request for Quote (returned with complete technical data), please fill out these brief specifications.

**OKI**
SEMICONDUCTOR

**My application requires:**

1. Gate count: ______
2. Pin count: ______
3. **CMOS process:**
   ( ) 1.5 micron
   ( ) 2 micron
   ( ) 3 micron
4. **Packaging preferred:**
   Surface-mount
   ( ) PLCC
   ( ) Flatpack
   Through-hole
   ( ) Pin Grid Array
   ( ) DIP
5. **Anticipated volume:**
   ______ pieces/month

☐ Please call me for immediate consultation.

**Request for Data**

☐ Please rush complete technical input on:
( ) CMOS Gate Arrays
( ) CMOS Standard Cells
( ) CMOS Custom VLSI Logic


Name/Title ______ Company ______ Tel: (___) ______
Address ______ City ______ State ______ Zip ______

EL 11/27/86

will be available in December; prices and availability for the SBS 30 and SBS 40 have not yet been determined.

Gates Energy Products Inc., 1050 S. Broadway, P.O. Box 5887, Denver, Colo. 80217.
Phone (303) 744-4806 [Circle 405]

## SMART LEDs ARE USER-PROGRAMMABLE

A family of 8-by-8-dot-matrix LED displays from Siemens Components Inc. incorporate built-in RAM to make them user-programmable.

Users can employ the same interface techniques they use for microprocessor peripherals. Progamming is accomplished through a direct correlation between each bit of an 8-bit word in the program code and a specific LED in a row or column. ASCII codes and low-resolution graphics can be implemented, including Japanese, Chinese, and other characters.

The PD-1165 red-orange LEDs and the PD-1167 green LEDs offer 1.2-in.-high characters and a 75° viewing angle. The LEDs can be read from 35 ft. away, suiting them for industrial applications.

Available now, an 1165 array costs $20.65 in 100-unit lots; the 1167 costs $22.10 in similar quantities.

Siemens Components Inc., Optoelectronic Division, 19000 Homestead Rd., Cupertino, Calif. 95014.
Phone (408) 752-3548 [Circle 407]

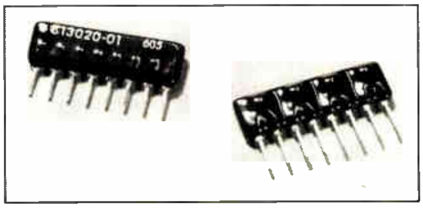
## SEMICUSTOM ARRAYS CUT CAPACITOR COSTS

Capacitor networks based on semicustom designs by Kyocera Northwest Inc. eliminate pattern costs and the need for substrate tooling for custom arrays. They can be available in production quantities within eight weeks.

The networks can be configured with 4 to 14 devices and feature three standard dielectrics: Z5U, X7R, and NPO. Operating voltages of 50 V and 100 V are standard, but the company offers a range of other values and tolerances. Kyocera will also build full-custom networks to meet special requirements.

The typical cost for an 8-pin, 50-V 470-pF semicustom network of four capacitors in an NPO dielectric is 55¢ in lots of 10,000.

Kyocera Northwest Inc., 11425 Sorrento Valley Rd., San Diego, Calif. 92121.
Phone (619) 454-1800 [Circle 408]



# SOLID-INK PRINTER OFFERS LETTER-QUALITY OUTPUT

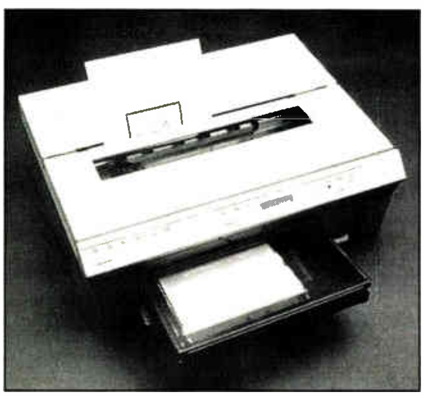
## DATAPRODUCTS' SI 480 BOASTS A CLOG-PROOF PRINTHEAD AND RESOLUTIONS AS HIGH AS 480 DOTS/IN.

A printer from Dataproducts Corp. with an innovative solid-ink technology achieves letter-quality output while eliminating two of the problems that have long plagued ink-jet printers—clogged pinheads and an inability to print on all paper types.

The $2,795 SI 480 [*Electronics*, Nov. 13, 1986, p. 25] uses solid ink in pellet form and an innovative printhead that can achieve letter-quality printing at both 200 and 400 characters/s. Horizontal resolution at 200 characters/s is 480 dots/in.; at 400 characters/s, it is 240 dots/in. Print quality is better than daisywheel or laser-printer output, the company claims, and the SI 480 runs two to four times faster than a daisywheel printer. "This is the most significant product Dataproducts has introduced since the initial letter printer on which the company was founded in the early 1960s," says John W. Leggat III, senior vice president of marketing.

The SI 480's primary application, says Leggat, will be as an upgrade for office systems. While it produces high-quality text and graphics at high speed, it also runs quietly—the noise level at top speed is less than 55 d, says Leggat. The SI 480 can be used with a wide variety of cut-sheet and pin-fed papers, as well as with transparencies, Leggat says. He estimates the company will sell about 6,000 SI 480 printers next year in an overall market of approximately 60,000 units.

The printing process involves melting the pellets and firing the liquified ink through tiny nozzles. Black is the only color available. Ink solidifies on the print media as a very fine, dark dot. The printer produces crisp output on all office papers, as well as on transparencies and labels. Since nozzle clogging due to evaporation is eliminated, printhead reliability is high—averaging 24 months between failures at a 25% duty cycle. Another factor in keeping the nozzle clear and functioning is a "drop on demand" scheme that feeds ink to the printhead only when it is needed.



**CRISP TYPE.** Character resolution on the SI 480 can be up to 480 dots per inch. The package includes two font styles and two

The printhead has 32 holes. Although horizontal resolution varies according to printing speed, vertical resolution is a constant 240 dots/in.

**FONT LIBRARY.** Two font styles are available with the standard unit, and an additional font library is optional. The SI 480 supports both RS-232-C and Centronics parallel-interface protocols. The basic unit, which includes a sheet feeder, tractors for continuous sheet feed, two font styles, and two interfaces, costs $2,795. It will be available in the first quarter of 1987.

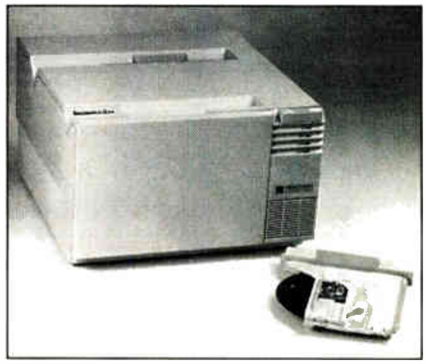
*–Ellie Aguilar*

Dataproducts Corp., 6200 Canoga Ave., P.O. Box 746, Woodland Hills, Calif. 91365.
Phone (818) 887-8000 [Circle 340]

## SLIDE-MAKING SYSTEM DELIVERS COST BREAK

Presentation Technology Inc.'s IBM Personal-Computer-based slide maker offers resolution equal to 35-mm slides made at service bureaus, but at a tenth the cost. Designed for use by nontechnical personnel, the ImageMaker desktop system delivers color slides with 8,000-line resolution in about a minute at an average cost of 50¢ per slide.

The ImageMaker departs from the conventional in-house method because it uses typesetting and plotter technology to reproduce the screen image. The conventional method is to take a photograph of the personal computer's screen, and the quality of these slides is limited by the resolution of the display screen. ImageMaker uses interchangeable font cartridges with industry-standard typefaces that can be reproduced directly on Eastman Kodak Co. Ektachrome or Polaroid Corp. Polachrome film. The device operates with most computers and requires an RS-232-C serial interface. System random-access-memory requirements vary, depending on the application software.



The system's IBM PC-compatible menu-oriented graphics program, ImageMate, provides a selection of four typefaces, eight graph charts, 16 foreground colors, and six fill patterns. It supports the Lotus 1-2-3 spreadsheet and Hewlett-Packard Co. plotters and permits on-screen previewing of slides. Available now, ImageMaker costs $4,995, and ImageMate, $295.

Presentation Technologies Inc., 743 N. Pastoria Ave., Sunnyvale, Calif. 94086.
Phone (408) 749-1959 [Circle 345]

## CUSTOM CLOCK KEYS TRIPLE REDUNDANCY

August Systems Inc. relies on custom-designed clock to synchronize triple-redundant Motorola Corp. 68020 processors, I/Os, and power supplies in its fault-tolerant CS3000 computer. Triple redundancy usually implemented by software has been implanted in proprietary logic to make fault tolerance transparent to the user.

This system implements a voting scheme aimed at eliminating transient errors, intermittent faults, and hardware-initiated errors. The result is a faster, more reliable computer having applications in aerospace, defense, and communications, claims the company.

A three-to-one voter system compares data and parity on all processors during each microprocessor read operation. If an error occurs, self-diagnostics are initiated on the faulty processor while the other two continue.

In order to match the fault-tolerant requirements of specific applications, CS3000s may be configured as single-, dual- or triple-redundant devices. This, in turn, minimizes cost and compatibility problems.

Compatible with industry standards, the system can be used with the Unix operating system, which supports Motorola's 68020 processor. The computer's I/O architecture supports two buses: VMEbus and the CS3000 fault-tolerant I/O. The CS3000 costs $75,000, and shipments will begin in March 1987.

August Systems Inc., 18277 S.W. Boones Ferry Rd., Tigard, Ore. 97224.
Phone (503) 684-3550 [Circle 347]

# Electronics
## CAREER OPPORTUNITIES
### Fall 1986 Planning Guide

| Issue | | Closing |
|---|---|---|
| November 13 | **Wescon Preview**<br>Bonus Distribution at Wescon<br>**Instruments Technology**<br>Automatic Test Equipment | October 27 |
| November 27 | **Communications Technology**<br>Fiber Optics<br>Special Communication Career Section | November 10 |
| December 11 | **Year-End Double Issue**<br>Executive Outlook<br>**Semiconductor Technology**<br>Linear ICs<br>ISSCC<br>**Military Technology**<br>Special Section: Military Electronics | November 24 |

**For more information, contact Susan Barnes-Ronga, National Recruitment Sales Representative, at (212) 512-2787**

## DESIGN ENGINEER

Provide engineering design & calculations for contract requirements relating to elevator systems (electrical/electronic/hydraulic) to ensure they meet safety regulations, pertinent codes & conform to functional specifications & customers requirements. Analyze drafting and related proposals to determine feasibility of project & material engineering requirements in connection with new products and/or determine appropriate products modifications. Change operations on relay based systems. Requires an Associate Degree in Electrical Engineering with an emphasis on Electrical Control Systems plus three years direct experience. Salary $32,400 Per Year, 40 Hours P.W., 8:30 A.M. to 5 P.M., M-F. Send resume to Illinois Job Service, 910 South Michigan Avenue, Room 333, Chicago, IL 60605, Att: L. Denegan, Ref. #: 6304-L. An Employer Paid Ad.

# THE CHALLENGE

## A Career as a
## SECURITY ENGINEER
## in the
## UNITED STATES FOREIGN SERVICE

An extraordinary opportunity for service in electronic surveillance countermeasures, security systems, computer security, and technical administration. Locations include the Washington, D.C. area and embassies and consulates throughout the world. Starting salary range $20,142 - $40,834.

*Further information and applications may be obtained by writing to:*

**Professional Policies and Programs**
**Bureau of Diplomatic Security**
**DS/PLD/PRP, Room 2426**
**U.S. Department of State**
**Washington, D.C. 20520**

or

**CALL COLLECT:**

**(202) 647-4819**

**An Equal Opportunity Employer**

# Engineers:

## Pan Am World Services, Inc. provides exactly the range that brilliant careers require.

### One range is geographical

World Services is prime contractor to the U.S. Air Force for the planning, engineering and operation of the Eastern Test Range. It stretches 10,000 miles from Cape Canaveral to Pretoria, South Africa, and includes some 1,800 ship and land based tracking units.

### Another is professional

We have long been involved with the entire space program. Missiles. Satellites. Space Shuttle. You name it. Depending on orientation, you'll be seeing, and contributing to, the last word in radar, optical instrumentation, telemetry, communications, data handling, $C^2$, statistical data reduction, meteorology, timing/firing, frequency control, shipboard instrumentation . . . and related technologies.

### The third range is choice

Following is a diverse array of engineering opportunities. Each requires an appropriate degree and at least 5 years relevant experience.

**TELEMETRY SYSTEMS ENGINEER**
Will accomplish design, acquisition, installation and evaluation of antennas, preamplifiers, mixers, down-converters, filters, demodulators, decommutators and computer interfaces for large aperture S-band telemetry antenna systems. Must perform hardware design and system analysis.

**DATA SYSTEMS ENGINEER**
Will accomplish design, acquisition, installation and evaluation of data acquisition, transmission, processing and display systems for distributed instrumentation complexes. Must have substantial experience in system/subsystem design, test and evaluation.

**RADAR SYSTEMS ENGINEER**
Will perform design, acquisition, installation and evaluation of high power transmitters, solid-state receivers, and digital range machines, and preparation of specifications for new land and shipboard radar used in tracking and signature data collection. Must be experienced in system/subsystem design, test and evaluation.

**OPTICAL SYSTEMS ENGINEER**
Will perform system design, installation, modification and evaluation of manned and unmanned optical tracker and camera systems.

**COMMUNICATIONS SYSTEMS ENGINEER**
Will accomplish design, acquisition, installation and evaluation of subsystem equipment and systems to support communications and timing requirements. ETR Communications Systems include analog and digital communications systems, red and black switching systems, long and short haul data transmission over HF, Microwave, Satellite and Cable (copper and fiber optics) Systems and Electronic Security Systems. Timing includes state-of-the-art PTTI systems.

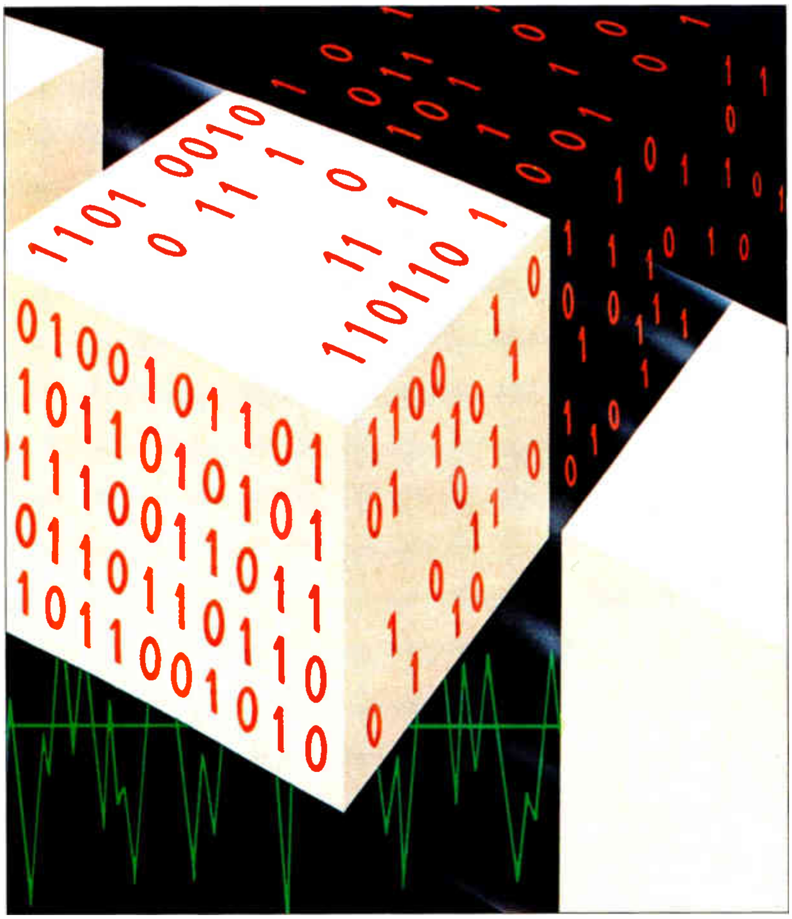
### Other attractions

Florida at its best . . . specifically, the Cocoa Beach area, excellent salaries, extensive benefits, stimulating associates, excellent career prospects, and eligibility for 75% discount travel on Pan Am for yourself and each eligible family member. Learn more. Contact Don Mosby at (305) 494-7322, or send your resume indicating position of interest to him at Pan Am World Services, Inc., Ref. 87-16, P.O. Box 4608, Building 423, MU 100, Patrick Air Force Base, Florida 32925.

**Pan Am World Services, Inc.**

An Equal Opportunity Employer • U.S. Citizenship Required

# DATA GRABBER.



*Zoran's vector digital-signal-processing chip with 70,000 transistors requires only three instructions to do a 1,024-point fast Fourier transform in 2.4 ms.*

"A speedy new single-chip contender is getting set to make a splash in digital signal processing. Zoran Corp.'s ZR34161 uses vector-handling techniques to gulp down blocks of data, rather than picking off a single data input at a time as scalar processors do. Vector processing alone is a big speed booster, and Zoran enhances it with embedded signal-processing algorithms that radically pare down system overhead.

The Santa Clara, Calif., company's 16-bit CMOS VSP is the first monolithic signal processor to utilize the powerful vector-handling techniques employed for scientific data processing in large vector computers and minicomputer array processors..."

*Excerpted from an exclusive article in the July 24, 1986 issue.*

McGraw-Hill **Electronics**

**THE LEADER IN NEW TECHNOLOGY COVERAGE**

## MEETINGS

**Microcomputer Graphics Show and Conference,** Expoconsul International Inc. (3 Independence Way, Princeton, N. J. 08540), Jacob Javits Convention Center, New York, Dec. 17-19.

**ATE West '87:** Automatic Test Equipment Exhibit and Conference, MG Expositions Group (1050 Commonwealth Ave., Boston, Mass. 02215) Anaheim Convention Center, Anaheim, Calif., Jan. 5-8.

**International Winter Consumer Electronics Show,** EIA Consumer Electronics Group (2001 Eye St., N.W., Washington, D.C. 20006), Las Vegas Convention Center, Las Vegas, Nev., Jan. 8-11.

**Macworld Exposition,** Mitch Hall Associates (P.O. Box 155, Westwood, Mass. 02090), Moscone Center, San Francisco, Calif., Jan. 8-10.

**O-E/LASE '87:** Symposium on Optoelectronics and Laser Applications, International Society for Optical Engineering (P.O. Box 10, Bellingham, Wash. 98227), Marriott Hotel and Airport Hilton Hotel, Los Angeles, Calif., Jan. 11-16.

**SMART III:** Surface Mounting and Reflow Technology, EIA, *et al.* (2001 Eye St., N. W., Washington, D. C. 20006), New Orleans Hyatt Regency, New Orleans, La., Jan. 12-15.

**Picosecond Electronics and Optoelectronics,** IEEE Lasers and Electro-Optics Society, *et al.* (Optical Society of America, 1816 Jefferson Place, N. W., Washington, D. C. 20036), Hyatt Lake Tahoe Hotel, Incline Village, Nev., Jan. 14-16.

**Computer Graphics '87,** Frost & Sullivan Inc. (106 Fulton St., New York, N.Y. 10038), Wesgate Hotel, San Diego, Calif., Jan. 14-16.

**Instrument Asia '87,** Instrument and Control Society (Kallman Associates, 5 Maple Ct., Ridgewood, N. J. 07450), Singapore, Jan. 14-17.

**OFC/IOOC '87:** Optical Fiber Communication Conference/International Conference on Integrated Optics and Optical Fiber Communication, IEEE Lasers and Electro-Optics Society, *et al.* (Optical Society of America, 1816 Jefferson Pl., N. W., Washington, D. C. 20036), Reno-Sparks Convention Center, Reno, Nev., Jan. 19-22.

**SYSCON:** OEM Computer Peripherals Subsystems Conference & Exposition, Multidynamics Inc. (17100 Norwalk Blvd., Suite 116, Cerritos, Calif. 90701), Los Angeles Airport Hilton Hotel, Los Angeles, Calif., Jan. 20-21.

**Uniforum Conference and Trade Show,** USR/group (4655 Old Ironsides Dr., Suite 200, Santa Clara, Calif. 95054), Washington Convention Center, Washington, D. C., Jan. 20-23.

**Winter 1987 Usenix Technical Conference,** Usenix Association (P.O. Box 385, Sunset Beach, Calif. 90742) Omni Shoreham, Washington, D. C., Jan. 21-23.

**Southern Manufacturing Technology Show,** National Machine Tool Builders Association (7901 Westpark Dr., McLean, Va. 22102), Charlotte Convention Center, Charlotte, N. C., Jan. 26-29.

**Advanced Semiconductor Equipment Exposition & Conference,** Cartlidge & Associates Inc. (1101 S. Winchester Blvd., Suite M259, San Jose, Calif. 95128) Santa Clara Convention Center, Santa Clara, Calif., Jan. 27-29.

**Wincon '87,** Aerospace and Electronic Systems Society (P. O. Box 6876, Burbank, Calif. 91510), South Coast Plaza Hotel, Costa Mesa, Calif., Jan. 27-29.

**1987 Annual Reliability and Maintainability Symposium,** IEEE, *et al.*, (Gen Pettee, Lockheed Missiles and Space Co., P. O. Box 1269, Cocoa Beach, Fla. 32931), Dunfey City Line Hotel, Philadelphia, Pa., Jan. 27-29.

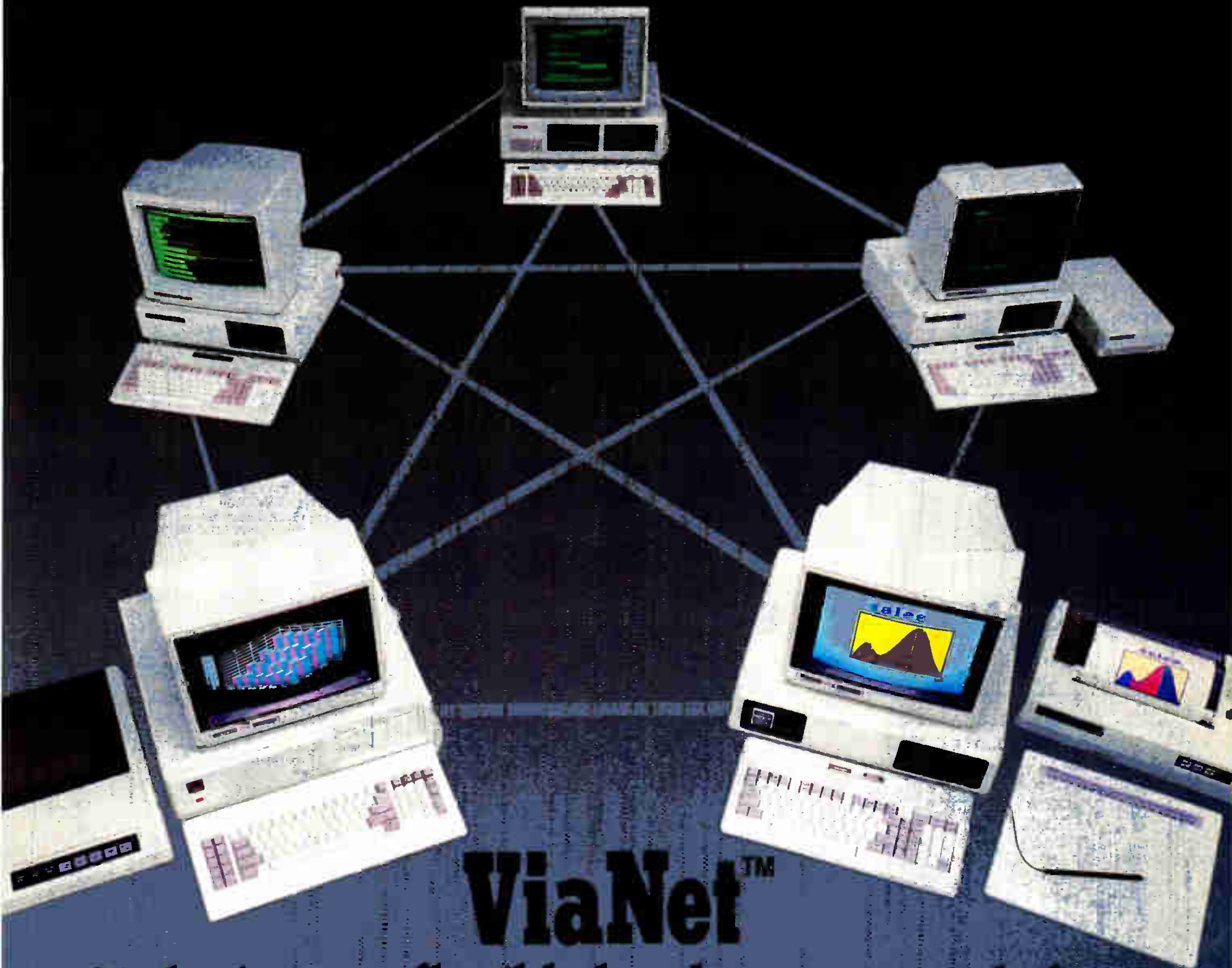
**Measurement Science Conference,** MSC (John Van de Houten, program chairman, TRW S/937, One Space Park, Redondo Beach, Calif. 90278), Irvine Marriott, Irvine, Calif., Jan. 29-30.

**International Symposium on Pattern Recognition and Accoustical Imaging,** International Society for Optical Engineering (P. O. Box 10, Bellingham, Wash. 98227), Newport Beach, Calif., Feb. 1-6.

**International Conference on Data Engineering,** IEEE Computer Society (1730 Massachusetts Ave., N.W., Washington, D. C. 20036), Pacifica Hotel, Los Angeles, Calif., Feb. 2-6.

**Manufacturing Productivity Conference & Exposition,** Society of Manufacturing Engineers (One SME Dr., P. O. Box 930, Dearborn, Mich. 48121), Expo Centre, Orlando, Fla. Feb. 3-5.

**Aerospace Applications Conference,** IEEE South Bay Harbor Section (Fausto Pasqualucci, Hughes Aircraft, 3100 Fujita St., Torrance, Calif. 90509), Vail, Colo., Feb. 8-13.



# PROFESSIONAL SERVICES

**Call**

**212-512-2556**

## PATENT SERVICES

Patentability Searches, Applications & Prosecutions • Marketing • Technology Transfer • Over a decade of service to the inventor.

*CALL FOR FREE INFORMATION*

**AMERICAN INVENTORS CORPORATION**

***(800) 338-5656*** ***In MA (413) 568-3753***

## POSITIONS VACANT

**Engineers—Discreet, Personal, Reputable.** National-fee paid. Murkett Assoc., Box 527, Montgomery, AL 36101.

## SPECIAL SERVICES

**Custom Switching Power Supply Design** — From concept to production model. High quality design, fast and reliable service, competitive rates. PETA, 833 The Queensway, Toronto, Ont., M8Z 5Z1, (416) 252-1581.

## POSITIONS WANTED

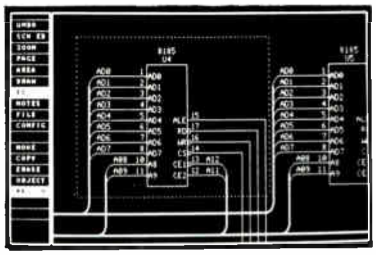
**Electronic Engr, for hire. Microprocessor** based designs, controls, telecom. Contact or per diem. Mr. Barry Masel. 718-476-1516.

## EMPLOYMENT SERVICES

**Overseas — 75 Countries — Interviewing** now. All Fields — for Conn. interview. Send resume: Global Services, (O) Clinton, CT 06413. Transportation not paid to Connecticut.

# COMPUTER SOFTWARE

## FREE DEMO DISK



**SCHEMA** is a complete, integrated schematic drawing software package for IBM Personal Computers. Use **SCHEMA** with your PC to draw schematics and automatically generate design documentation such as Wire and Net Lists, Bills of Materials, Design Rule Checks, etc. **SCHEMA** is $495 and supports most common PC hardware configurations. Call or write today for a free demo disk and brochure.

**OMATION, INC.**
1701 N. Greenville Ave., Suite 809
Richardson, TX 75081
(214) 231-5167

OMATION

**THE BEST Schematic Capture IS ONLY $495**

- Runs on IBM PC/XT/AT or compatible, supporting most common graphic boards, printers and plotters
- Over 2000 unique library parts
- Part rotation & mirroring
- Rubberbanding of wires & buses when objects are moved
- Supports A through E size sheets
- True unlimited level hierarchy
- Visible grids, 5 zoom levels
- Color & monochrome graphics
- Draws non-orthogonal wires & buses
- Step & repeat with auto increment/decrement of labels
- Powerful keyboard macros & auto panning
- Net/wire list, BOM, design check & library creation utilities

OrCAD gives you so many features, nothing else even comes close. Why settle for anything less? At only **$495** you will discover that **OrCAD/SDT** is the most powerful and cost effective schematic design tool available. . . at any price!

Call today for your Free Demo Disk and brochure. All orders are shipped from stock for immediate delivery!

OrCAD Systems Corporation
1049 S.W. Baseline St., Suite 500
Hillsboro, OR 97123
(503) 640-5007

**RELIABILITY PREDICTION SOFTWARE**

***ARE YOUR PRODUCTS RELIABLE?***

RelCalc 2 automates MIL-HDBK-217D on your IBM PC!
Very easy to use. Demo package $25.

**T-CUBED SYSTEMS** **(818) 991-0057** **31220 La Baya Drive, #110** **Westlake Village, CA 91362**

*SPICE* up your *PC*

Z/SPICE professional circuit simulation
Full version $300 Student version $79

**ZTEC** box 737, college place, wa 99324 (509)-529-7025

## Advertising Sales Staff

**Atlanta, Ga. 30319:** Joseph Milroy
4170 Ashford-Dunwoody Road N.E.
[404] 252-0626
**Boston, Mass. 02116:**
M. E. "Casey" McKibben, Jr.
575 Boylston St.
[617] 262-1160
633-0155 Mobil Phone
**Chicago, Ill. 60611:** William J. Walker
[312] 751-3738
645 North Michigan Avenue
**Cleveland, Ohio 44113:**
[216] 496-3800
**Costa Mesa, Calif. 92626:** Fran Cowen
3001 Red Hill Ave. Bldg. #1 Suite 222
[714] 557-6292

**Dallas, Texas 75240:** Harry B. Doyle, Jr.
5151 Belt Line Road, Suite 907
[214] 458-2400
**Englewood, Co. 80112:** Harry B. Doyle, Jr.
7400 South Alton Court Suite 111
[303] 740-4633
**Houston, Texas 77040:** Harry B. Doyle, Jr.
7600 West Tidwell, Suite 500
[713] 462-0757
**Los Angeles, Calif. 90010:** Chuck Crowe
3333 Wilshire Blvd.
[213] 480-5210
**New York, N.Y. 10020**
Matthew T. Reseska [212] 512-3617
John Gallie [212] 512-4420
1221 Avenue of the Americas
**Stamford, Ct. 06902**
Albert J. Liedel
777 Long Ridge Road. Bldg. A
[203] 968-7115
**San Mateo, Ca 94404:**
Larry Goldstein, Jeffrey C. Hoopes, Paul Mazzacano
3rd Floor
951 Mariner's Island Blvd.
[415] 349-4100
**Philadelphia, Pa. 19102:** Joseph Milroy
Three Parkway, [215] 496-3800
**Pittsburgh, Pa. 15222:** Joseph Milroy
Suite 215, 6 Gateway Center, [215] 496-3800
**Southfield, Michigan 48075:**
4000 Town Center, Suite 770, Tower 2
[313] 352-9760
**San Francisco, Calif. 94111:**
Larry Goldstein, Jeffrey C. Hoopes, Paul Mazzacano
425 Battery Street
[415] 362-4600

**Frankfurt/Main:** Fritz Krusebecker, Dieter Rothenbach
19 Liebigstrasse, Germany
Tel: 72-01-81
**Milan:** Manuela Capuano
1 via Baracchini, Italy
Tel: 86-90-656
**Paris:** Jean - Christian Acis, Alain Faure
128 Faubourg Saint Honore, 75008 Paris, France
Tel: [1] 42-89-0381
**Scandinavia:** Andrew Karnig
Finnbodavagen
S-131 31 Nacka
Sweden
Tel. 46-8-440005
Telex: 17951 AKA S
**Tokyo:** Hirokazu Morita
McGraw-Hill Publications Overseas Corporation,
Kasumigaseki Building 2-5, 3-chome,
Kasumigaseki, Chiyoda-Ku, Tokyo, Japan
[581] 9811

**United Kingdom:** Art Scheffer
34 Dover Street, London W1
Tel: 01-493-1451

## Business Department

**Thomas E. Vachon**
Director of Operations
[212] 512-2627
**Leon Irgang**
Circulation Director
[609] 426-5542
**Roseann Lehmann**
Office Administrator
[212] 512-3469
Customer Service
[212] 512-6643
**Frances M. Vallone**
Mgr./Marketing Adm.
[212] 512-6058
**Patricia Parks**
Billing Specialist
[212] 512-2589
**Thomas M. Egan**
Production Director
[212] 512-3140
**Carol Gallagher**
Production Manager
[212] 512-2045
**Evelyn Dillon**
Production Manager Related Products
[212] 512-2044

## Classified Advertising

[212] 512-2556

## Recruitment Advertising

**Susan Barnes-Ronga**
[212] 512-2787
[212] 512-2788

# Advertisers Index



## Classified and employment advertising



■ For more information of complete product line see advertisement in the latest Electronics Buyers Guide
* Advertisers in Electronics International
‡ Advertisers in Electronics domestic edition

# ELECTRONICS WEEK

## BOOK-TO-BILL RATIO UP IN OCTOBER

The U. S. semiconductor industry posted modest gains during October. The Semiconductor Industry Association's book-to-bill ratio edged up slightly to 0.98 from 0.92 in September. The National Electronics Distributors Association, meanwhile, reported a stronger book-to-bill ratio for the fourth straight month, rising in October to 1.06 from 1.0 in September.

The SIA's book-to-bill had been slipping steadily since April, but preliminary figures for October show it reached its highest level since June, when the ratio was 1.07. The SIA says that for the three-month period ending Oct. 31, bookings totaled $700.4 million, while sales for the same period were $650.1 million.

## HP ACQUIRES MCC MEMBERSHIP

Hewlett-Packard Co. is buying into the Microelectronics and Computer Technology Corp., an industry research consortium, by purchasing the membership of BMC Industries Inc., St. Paul, Minn. The move makes HP one of 11 companies sponsoring the consortium's semiconductor packaging and interconnection program, and keeps the total of MCC shareholders at 21. BMC announced late last year that it was selling the MCC membership as well as its Interconics Division as part of a restructuring program geared to divest itself of electronics businesses.

## SPERRY-BURROUGHS BECOMES UNISYS...

Unisys Corp. is the new name for the world's second largest computer maker, the massive new company formed when Burroughs Corp. paid $4.8 billion for Sperry Corp. in September. The name change is just one milestone in a major shakeup, however. Unisys is still trying to sell off $1.5 billion in assets not directly tied to the company's core information-processing businesses.

## ...AND SELLS GROUP TO HONEYWELL

Unisys Corp. has agreed to sell the former Sperry Aerospace Group for $1.03 billion to Honeywell Inc. Based in Phoenix, Ariz., the aerospace operation makes flight instrumentation, advanced avionics equipment, and spaceborne computer systems, and had sales of $700 million in fiscal 1986. Observers say the group will fit well with Honeywell's Aerospace and Defense Business, which is based in Minneapolis, Minn., and had 1985 sales of $1.9 billion. Honeywell makes navigation systems that are based on ring-laser gyroscopes, radar altimeters, and flight controls.

## TOSHIBA HAS YEN TO BUY AMERICAN

Toshiba Corp. will take advantage of the strong Japanese yen by increasing purchases from U. S. companies. The Japanese electronics giant has opened a procurement office in Burlington, Mass.—the second such office in the U. S.—to buy U. S. electronic equipment, components, and materials. Toshiba has also established a Semiconductor Evaluation Support Center in Tokyo to evaluate foreign semiconductors for Toshiba divisions. The company says it will double electronics imports next year, which totaled $420 million in 1985—including $300 million from the U.S.

## 50,000 JOBS IN ELECTRONICS CUT

The U. S. electronics industry lost 50,000 jobs in 1985, mostly in California, Massachusetts, and Illinois, says the American Electronics Association. California, the nation's leading electronics employer with 23% of the industry's 2.54 million jobs, lost 20,000 jobs last year, and Massachusetts and Illinois each lost 12,000. Two newcomers to electronics, Maryland and Michigan, helped pick up the slack, however, with 5,000 new jobs each. North Carolina chipped in with 3,000 new positions.

## ZILOG CUTS BACK SYSTEMS DIVISION

Zilog Inc., a subsidiary of Exxon Corp., is trimming some of its non-semiconductor operations. The Cupertino, Calif., chipmaker will continue to sell 16- and 32-bit Unix-based computer systems, but it has sold off the customer services operation of its Systems Division and is now negotiating to transfer all manufacturing to Gold Star Ltd. in Seoul, South Korea. Zilog also has sold its spare parts, maintenance equipment, and service contracts to the customer services division of Honeywell Inc. A spokesman says that, stripped of manufacturing and service operations, the Systems Division will now operate at a profit.

## 7.5% GROWTH SEEN IN EUROPE'S MARKET

The Western European electronics market will grow by 7.5% in 1987, predicts Benn Electronics Publications Ltd. in this year's edition of its "Mackintosh" data book. Benn expects the European market for electronic equipment and components to grow to $113 billion in 1987 from $105 billion this year, with the bulk of the growth taking place in data processing. Benn says Western Europe's appetite for data-processing equipment will grow at an 11.2% annual rate through 1990.

West Europe's semiconductor market is set for even bigger growth, according to Motorola Inc., which says the booming automotive market will help drive the chip industry in Western Europe to 13% growth.

## XEROX SETS UP UK COMPUTER LAB

Rank Xerox Ltd. and Xerox Corp. are setting up a research laboratory in Cambridge, UK, called EuroParc (after Xerox's Palo Alto Research Center in Silicon Valley). About 12 to 15 senior researchers and a support staff will initially concentrate on speech recognition, eventually branching out to study other man/machine interfaces for business computers as well. The companies are spending about $320,000 to equip the laboratory, which should be operational by February. Its annual budget will be about $1.4 million.

## FOUR FIRMS BLESS 5¼-in. OPTICAL DISK

An international quartet of electronics companies have joined to support a new standard for 5¼-in. optical disk drives and media. Alcatel Thomson Gigadisc of France, Optical Storage International of the U. S., and Japan's Sony Corp. have joined with the Philips and Dupont Optical Co. of the Netherlands to back a data format that will allow a minimum of 300 megabytes storage capacity on each side of the disk.

## KODAK UNVEILS 14-in. DRIVE

Eastman Kodak Co. unveiled its own 14-in. optical-disk technology at Fall Comdex in Las Vegas less than a week after it announced an agreement with the Philips and Dupont Optical Co. to develop a standard 14-in. optical memory system. The WORM (for write-once, read-many times) system provides 6.8 gigabytes of random-access storage. Samples will ship this winter, and volume quantities will be available in late 1987.

# Electronics Reader Service

If the card below has already been used, you may obtain the needed information by writing directly to the manufacturer, or by sending your name and address, plus the Reader Service card number and issue date, to Electronics Reader Service Department, P.O. Box 2713, Clinton, Iowa 52735.

## Electronics

November 27, 1986 This Reader Service Card expires February 27, 1987

Name ______________________ Title ______________________

Phone ______________________ Company ______________________

Street address (company [ ] or home [ ] check one) ______________________

City ______________________ State ______________________ Zip ______________________

Signature ______________________ Date ______________________

Was this magazine personally addressed to you? [ ] Yes [ ] No

5 Source of Inquiry-Domestic

**Industry classification** (check one)

**A.** ☐ Computers Computer Systems and Equipment
**B.** ☐ Communications Communications Systems and Equipment
**C.** ☐ Military Space Systems and Equipment
**D.** ☐ Industrial Systems Controls and Equipment
**E.** ☐ Electronics Subassemblies Components and Materials
**F.** ☐ Test and Measurement Equipment
**G.** ☐ Consumer Products
**H.** ☐ Medical Systems and Equipment
**I.** ☐ Software
**J.** ☐ Research & Development
**K.** ☐ Educational 2-4 Year College University
**L.** ☐ Other ______________________ Please specify

**Your principal job responsibility** (check one)

**A.** ☐ Corporate/Operating and General Management
**B.** ☐ Design & Development Engineering
**C.** ☐ Engineering Services
**D.** ☐ Basic Research
**E.** ☐ Manufacturing & Production
**F.** ☐ Other ______________________

**Estimate number of employees** (at this location): **1.** ☐ under 20 **2.** ☐ 20-99 **3.** ☐ 100-999 **4.** ☐ over 1000

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 16 31 46 | 61 76 91 106 | 121 136 151 166 | 181 196 211 226 | 241 256 271 348 | 363 378 393 408 | 423 438 453 468 | 483 498 703 718 |
| 2 17 32 47 | 62 77 92 107 | 122 137 152 167 | 182 197 212 227 | 242 257 272 349 | 364 379 394 409 | 424 439 454 469 | 484 499 704 719 |
| 3 18 33 48 | 63 78 93 108 | 123 138 153 168 | 183 198 213 228 | 243 258 273 350 | 365 380 395 410 | 425 440 455 470 | 485 500 705 720 |
| 4 19 34 49 | 64 79 94 109 | 124 139 154 169 | 184 199 214 229 | 244 259 274 351 | 366 381 396 411 | 426 441 456 471 | 486 501 706 900 |
| 5 20 35 50 | 65 80 95 110 | 125 140 155 170 | 185 200 215 230 | 245 260 275 352 | 367 382 397 412 | 427 442 457 472 | 487 502 707 901 |
| 6 21 36 51 | 66 81 96 111 | 126 141 156 171 | 186 201 216 231 | 246 261 338 353 | 368 383 398 413 | 428 443 458 473 | 488 503 708 902 |
| 7 22 37 52 | 67 82 97 112 | 127 142 157 172 | 187 202 217 232 | 247 262 339 354 | 369 384 399 414 | 429 444 459 474 | 489 504 709 951 |
| 8 23 38 53 | 68 83 98 113 | 128 143 158 173 | 188 203 218 233 | 248 263 340 355 | 370 385 400 415 | 430 445 460 475 | 490 505 710 952 |
| 9 24 39 54 | 69 84 99 114 | 129 144 159 174 | 189 204 219 234 | 249 264 341 356 | 371 386 401 416 | 431 446 461 476 | 491 506 711 953 |
| 10 25 40 55 | 70 85 100 115 | 130 145 160 175 | 190 205 220 235 | 250 265 342 357 | 372 387 402 417 | 432 447 462 477 | 492 507 712 954 |
| 11 26 41 56 | 71 86 101 116 | 131 146 161 176 | 191 206 221 236 | 251 266 343 358 | 373 388 403 418 | 433 448 463 478 | 493 508 713 956 |
| 12 27 42 57 | 72 87 102 117 | 132 147 162 177 | 192 207 222 237 | 252 267 344 359 | 374 389 404 419 | 434 449 464 479 | 494 509 714 957 |
| 13 28 43 58 | 73 88 103 118 | 133 148 163 178 | 193 208 223 238 | 253 268 345 360 | 375 390 405 420 | 435 450 465 480 | 495 510 715 958 |
| 14 29 44 59 | 74 89 104 119 | 134 149 164 179 | 194 209 224 239 | 254 269 346 361 | 376 391 406 421 | 436 451 466 481 | 496 701 716 959 |
| 15 30 45 60 | 75 90 105 120 | 135 150 165 180 | 195 210 225 240 | 255 270 347 362 | 377 392 407 422 | 437 452 467 482 | 497 702 717 960 |

## YES, *please enter my subscription to Electronics for the term checked below:* Subscription Card

Name ______________________

Title ______________________

Company ______________________

Div. or Dept. ______________________

Co. address ______________________

City ______________________ State ______________________ Zip ______________________

☐ **Check here if you wish publication to be sent to home address:**

Street ______________________

City ______________________ State ______________________ Zip ______________________

Signature ______________________

Those not qualifying may pay higher than basic price.

| | US | CANADA | MEXICO |
|---|---|---|---|
| ☐ One Year: | $32 | $ 51 CDN | 17,850 Pesos |
| ☐ Two Years: | $55 | $ 86 CDN | 29,925 Pesos |
| ☐ Three Years: | $76 | $117 CDN | 40,950 Pesos |

☐ **Payment enclosed** ☐ **Bill me**

Charge my subscription to: ☐ AMEX ☐ DC ☐ VISA

☐ MC-Bank# ______________________

Acct# ______________________ Exp. ______________________

Signature ______________________

Subscriptions are normally entered within 2 weeks, but please allow 4 weeks for shipment.

**Please check which best describes your company's business at your location:**
☐ Manufacturing ☐ Distribution ☐ Retailing ☐ Other ______________________

☐ **Indicate the primary product manufactured or services performed at your plant. (place applicable letter in box)**

A. Computers, data processing and peripheral equipment, office and business machines
B. Communications, data communications, telecommunications systems and equipment
C. Navigation and guidance, aircraft and missile systems or equipment (oceanography)
D. Test and measurement equipment
E. Consumer products (TV, radio, hi-fi, recorders, home computers, appliances)
F. Medical, industrial controls, systems or equipment
G. Semiconductor production equipment (component insertion, coil winding, etc.)
H. Electronic sub-assemblies, components and materials (passive, active components, IC's, discretes, hybrids, power supplies)
I. Other manufacturers using electronics equipment as part of their product (machine tools, chemicals, metals, plastics, pharmaceuticals, etc.)
J. Government and military
K. Independent research and development laboratory or consultant
L. Research and development organizations which are part of an educational institution
M. Independent software developers
N. Operators of communications equipment (utilities, railroads, police and airlines, broadcasting, etc.)
O. Educational 2-4 year college, university
P. Other ______________________

☐ **Indicate your principal job function, occupation and/or title (place applicable letter in box. If letters O, P, or Q are used, fill in name of college or university).**

A. Corporate Management (Owners, Partners, Presidents, V.P.'s, etc.)
B. Operating Management (General Managers, Group Managers, Division Heads, etc.)
C. Engineering Management (Project Manager, Chief Engineer, Section Heads, V.P. Engineering, V.P. Research and Development, V.P. Quality Control, etc.)
D. Software Engineering
E. Systems Engineering/Integration
F. Quality Control Engineering (Reliability and Standards)
G. Design Engineering
H. Engineering Support (Lab Assistants, etc.)
I. Test Engineering (Materials, Test, Evaluation)
J. Field Service Enginering
K. Research and Development (Scientists, Chemists, Physicists)
L. Manufacturing and Production
M. Purchasing and Procurement
N. Marketing and Sales
O. Professor/Instructor at ______________________
P. Senior Student at ______________________
Q. Graduate Student at ______________________

☐ **Indicate your principal job responsibility. (place the appropriate number in box)**
1. Management 2. Engineering Management 3. Engineering

**Estimated number of employees at this location. (check one)**
☐ 1 to 49 ☐ 50 to 249 ☐ 250 to 999 ☐ over 1,000

Date ______________________ Signature ______________________

**All information is required for reentry of subscription**

55K2

# Electronics

# Reader Service

**For additional information on products advertised, new products or new literature, use these business reply cards.**

Complete entire card.

Please print or type.

Circle the number on the Reader Service postcard that corresponds to the number at the bottom of the advertisement, new product item, or new literature in which you are interested.

To aid the manufacturer in filling your request, please answer the three questions.

All inquiries from outside the U.S. that cannot reach Electronics before the expiration date noted on the Reader Service postcard must be mailed directly to the manufacturer. The manufacturer assumes all responsibilities for responding to inquiries.

## Subscriptions & Renewals

Fill in the subscription card adjoining this card. Electronics will bill you at the address indicated on the card.

AFFIX POSTAGE STAMP HERE

**Electronics**

**P.O. BOX NO. 2713**
**CLINTON, IOWA 52735**

NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

**BUSINESS REPLY MAIL**

FIRST CLASS PERMIT NO. 55 MARTINSVILLE, NJ

Postage will be paid by Addressee

**Electronics**

**CN 807**
**MARTINSVILLE, NJ 08836**