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THE APPLE II: HOW AN OLD DOG LEARNED NEW TRICKS/92

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Electronics®

INTEL'S ISDN ENTRY ACCELERATES A MAJOR PUSH INTO MICROCOMMUNICATIONS

PAGE 59

ISDN CHIP SETS:

USERS FACE A RISKY CHOICE

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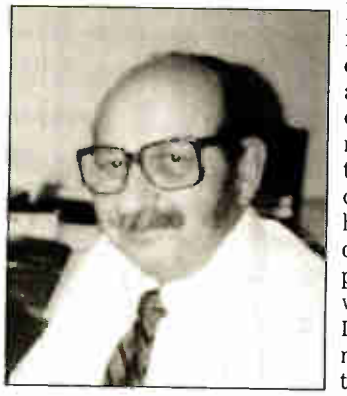
Electronics

PUBLISHER'S LETTER

George Sideris, a veteran *Electronics* editor, is back on our masthead as special-projects editor. He'll work out of our San Mateo, Calif., office on special reports and series that are designed to expand our coverage of the major trends and issues in the industry.



SIDERIS. Back to *Electronics* as our special projects editor.

One of the best known and most respected journalists in Silicon Valley, George has worked with us in one way or another for a good part of the past 30 years. He first signed on in 1957 as a business news editor in New York, after graduating from the University of Chicago in 1949 with a BA degree, taking a year of journalism courses at Rutgers University, and working five years as a newspaper reporter.

During the next 10 years George held a variety of news and technical editing positions, before leaving to work as a free-lance writer with many of the larger companies in the Valley. He rejoined us as San Francisco bureau manager in 1972, went back to free-lancing and then to Regis McKenna Inc., a high-tech public relations company in Palo Alto, Calif. He joined us again in 1982 as a department editor based in Palo Alto.

Then George decided to bite the bullet and do what many of us in this business say we'll do some day—write a novel. "I spent most of 1983 and 1984 working on the book, which is now in second draft. Last year, I began to freelance again—speeches first, then technical articles. Those first articles took me twice as much time to write as they should have because I had fallen behind. While I was developing my characters and plot, the industry was developing ASIC, CAE, ISDN, AI, DSP, and many other important technologies.

"I was very impressed by the intensity and skill with which *Electronics* has been reporting this tidal wave of developments. That work certainly has helped me to catch up, and I have no doubt that it has also greatly helped our other readers to stay on the learning curve. It's easy to become blasé about technical journalism, but that experience of staying away for a few years opened my eyes. It was one of the reasons I decided to return to *Electronics*."

George says he is looking forward to his new post. "Working on special projects will be far more challenging and interesting than free-lancing, because most free-lance jobs are about a single development. I welcome the opportunity to report on some of the sea changes and cross-currents occurring in the industry today."

And he has even armed himself with a fully loaded AT&T personal computer. But George is welcome back even without the computer.

Laurence Altman

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FYI

The Peat Marwick-McKenna alliance is one more indicator that no publication is better positioned than ours to meet the information needs of industry managers

Not a few industry managers were bemused by last week's announcement of a "strategic affiliation" between Peat Marwick and Regis McKenna Inc. Many of them were having a hard time figuring out exactly what the Big Eight accounting firm, which serves some 1,500 high-tech clients, wanted with RMI, the Silicon Valley agency that provides strategic marketing and communications services to some 100 high-tech companies. A giant press kit didn't help much: "The alliance will provide the breadth and depth of expertise that high-tech companies need to address strategic business, marketing, and communications issues." So what does it all mean?

For one thing, it will mean exactly what the two companies want it to mean. As Regis McKenna puts it: "There is no model now for service companies when they want to form strategic alliances." There are few observers of the high-tech marketing scene more canny than McKenna. Early on he recognized that industry leaders, whether they were product planners, designers, or marketers, were having an increasingly difficult time creating markets and positioning and differentiating products in a global environment of diversity and proliferation.

As McKenna points out, the industry environment has changed radically. Ten years ago, there were far fewer companies, products, or technologies. Now it has exploded into dozens of narrow vertical niches, while major segments have become intensely competitive. In 1985, for example, over 150 companies supplied IBM PC clones, 240 firms marketed personal computers, and 60 offered 5¼-in. disk drives.

That environment, which always shapes the industry's products as McKenna is fond of saying, also drives this magazine. Whether it's time-sensitive, value-added information packaged by *Electronics* in a highly readable form for technically trained managers, or whether it's the expertise that the Peat Marwick-RMI combo says it can provide, hard-pressed managers will need far more of this help in the future if they and their companies are to survive. For McKenna, his strategic alliance "is a highly exciting prospect that will break new ground." For us, his move is one more indicator that no publication is better positioned than ours to meet the pressing information needs of industry managers.

ROBERT W. HENKEL

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LETTERS

Another one rides the bus

To the editor: I read with interest Tobias Naegele's article, "The Next Big Auto Market: The Multiplexed Data Bus" [*Electronics*, Aug. 21, P.81]. I was especially interested in the summary of European sources of multiplexed systems, particularly when it became obvious that my company, Salplex Ltd., was not mentioned—even though the example on a control family is very similar to drawings in our advertising material.

Salplex is probably the only company that has been set up solely to develop and market multiplexed wiring systems. The conclusion we reached is that the prime requirement is for an SAE Class 'A' system [basic controls] that is cost-competitive with conventional wiring.

We believe that our competitors' approach of designing Class B systems [instruments, engine controllers, and trip computers], which then encompasses Class A almost as an afterthought, does not meet this requirement, and as such we have designed a system that is essentially Class A and encompasses some of Class B applications.

J.A. Hodgkiss
Engineering Manager, Salplex Ltd.
Rugeley, UK

□Electronics *based its drawing on one supplied by Integrated Power Semiconductors Ltd., Livingston, Scotland.*

An alternative to Lisp

To the editor: When writing software for an expert system, it is not necessary to avoid artificial intelligence programming languages in favor of conventional high-level languages, as implied in "What's Holding Back Expert Systems?" [*Electronics*, Aug. 7, 1986, p. 59]

C and Lisp are not the only alternatives. IF/Prolog is a real AI programming language (executing at 100,000 logical inferences per second) especially aimed at expert-systems applications. It also runs on a large number of computers, such as the Digital Equipment Corp. VAX, and others that run Unix or VMS/Ultrix operating systems and use Motorola's 680XX processors. Using Prolog, a given inference component can be implemented on conventional computer architectures.

Karin Höss
Interface Computer GmbH
Munich, W. Germany

Aion isn't switching to C

Correction: *In "What's Holding Back Expert Systems?"* [Electronics, *Aug. 7, 1986, p. 59] the programming language used by Aion Corp. for its expert systems was incorrectly identified. Aion's products are all written in Pascal.*

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HOW ZAININGER BUILT A U.S. LAB FOR SIEMENS

PRINCETON, N. J.

When Siemens AG decided to set up a research center for its growing American business six years ago, the West German electronics giant turned to Karl Zaininger, a native of Munich who has studied and worked in the U. S. since the early 1950s. It was the perfect fit—Zaininger had the experience to build a successful research program along with the German roots needed to fit seamlessly into the Siemens picture.

Building Siemens' Research and Technology Laboratories into a $40-million-a-year research institution was a challenging task, Zaininger says, and his success has not gone unrewarded. Last month he earned the added title of president, Siemens Corporate Research and Support Corp., which includes the lab and several administrative and strategic support facilities. But it is the Princeton, N. J., laboratory—Zaininger calls it his "baby"—that makes him most proud. "You've got to be an American to build an American laboratory," says Zaininger, a naturalized U. S. citizen. But he adds that his German background didn't hurt when it came to getting what he needed from the Siemens bureaucracy.

The biggest difference between an American and a European lab, Zaininger explains, is the outlook of the researchers who work there. In Munich, he says, getting a job with Siemens is just like joining Ma Bell in the days before divestiture: employment for life.

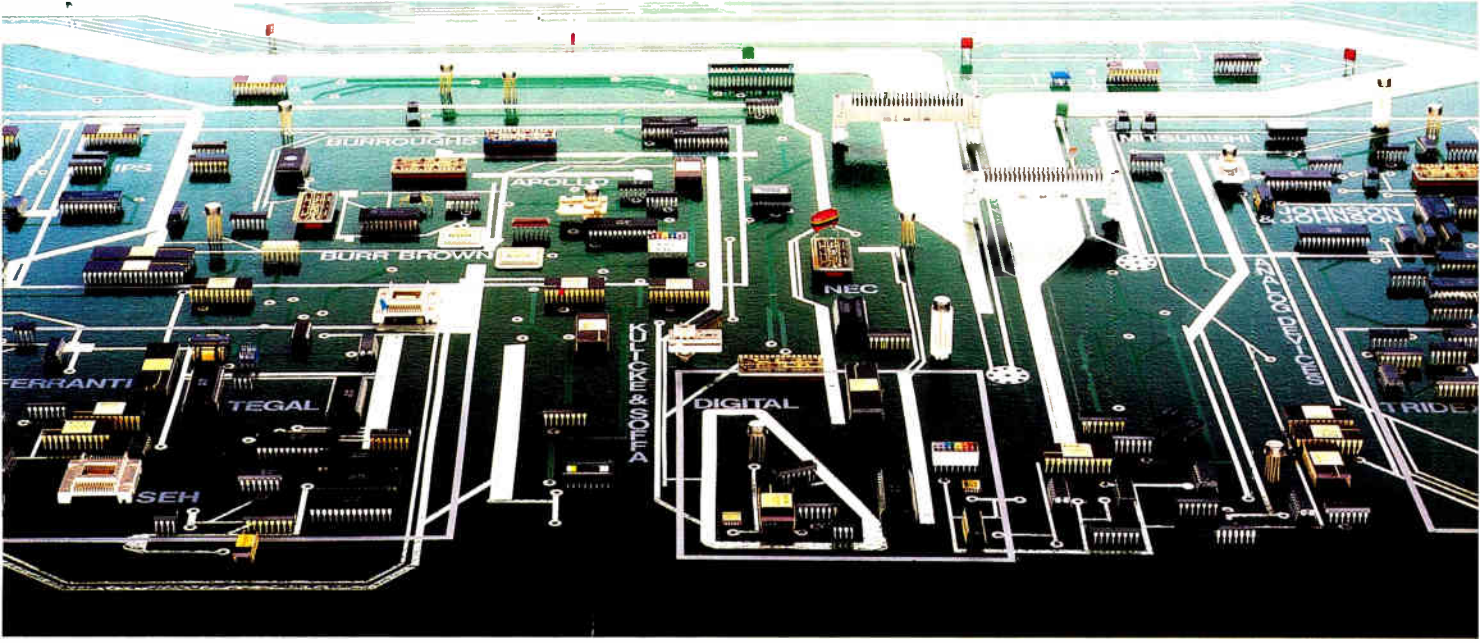
"But in the U. S. the kids want to stay competitive," he says. "They want to be able to take other jobs in the outside world, or to go seek venture capital." So at the Research and Technology Labs he encourages employees to use the Princeton University facilities, he lets them travel to technical meetings, and he has made German classes available for employees interested in temporary transfers overseas.

Location is also important to American engineers, he says. After graduating from Princeton University with master's and doctoral degrees in solid-state physics, Zaininger chose to stay in the Princeton area at RCA Corp.'s David Sarnoff Research Center. His reasons ranged from the area's proximity to New York and the New Jersey shore to the high concentration of quality laboratory facilities run by other firms, notably those of AT&T Co. When it came time to set up the research facility, Zaininger pressed Siemens to let him remain here.

STAYING FLEXIBLE. With about 120 researchers working on such diverse projects as molecular-beam epitaxy and robotics control, Zaininger says the organization is now half-grown. He wants to double the group's size by 1990, he says, but that will be it. "With 250 people it will be the ideal size. Once you get bigger than that you lose the flexibility of a small lab."

An adventurous youth, Zaininger came to the U. S. in pursuit of the woman who would eventually become his wife—a Ukrainian refugee who had stopped in Munich before moving on to the U. S. Drafted during the Korean conflict, he served two years in the Army and then enrolled at Princeton. Upon graduating, he was snapped up by

ZAININGER: "With 250 people [it] will be the ideal size. Once you get bigger you lose the flexibility of a small lab."



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Nor are Burroughs the only company to manufacture a successful product that's been both designed and developed entirely in Livingston. This particular new product (the S40 desk-top document processing machine) is also designed to be marketed worldwide from Livingston.

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For the design, manufacture and marketing of the S40, Burroughs, along with every other company who are 'making it in Livingston', have a wealth of local resources to call upon.

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Semiconductor suppliers such as L.T.I.S. Matra, Alphasem, Tegal and Kulicke & Soffa.

Packaging suppliers. Component engineering companies such as

Livingston Precision. (Coincidentally, one of only a handful of companies, worldwide, who have been awarded the coveted Burroughs Supplier Excellence Award.)

And, of course, a plentiful, highly skilled and motivated workforce with a proven record of outstanding productivity.

A description fully endorsed by a recent survey carried out amongst US-owned companies operating in Scotland.

Of the workforce, it concluded that attitudes to work and responsiveness to training were well pleasing, quality of output was consistently above corporate standards and high flexibility was a common feature of the plants visited.

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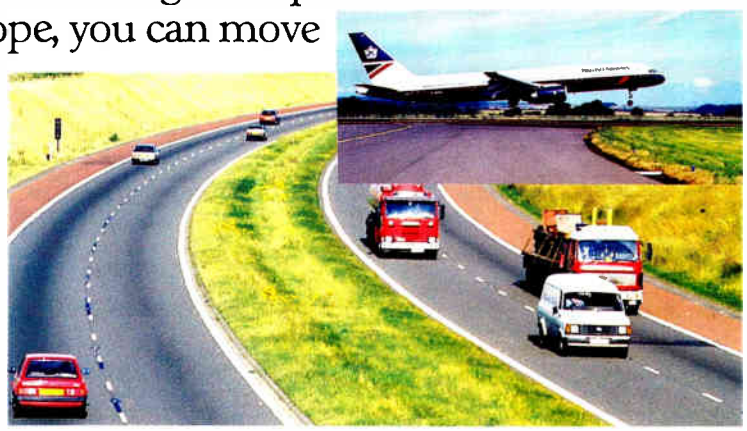

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RCA, where he stayed 19 years. By the time he left—"it was the result of a midlife crisis, of course"—he had risen to be the center's manager of solid-state technology. An eight-month stint at the Department of Energy's Solar Energy Research Institute in Golden, Colo., followed, and then Zaininger was named director of the Army's Microelectronics Division at Ft. Monmouth Laboratories in New Jersey in 1978. During that three-year stretch he helped set up the Defense Department's Very High Speed Integrated Circuit (VHSIC) program there before Siemens gave him a chance to build his own lab from scratch.

"This is the best job for me," Zaininger says of Siemens. "It lets me live in my two favorite cities in the world—Munich and Princeton."–*Tobias Naegele*

WHY PRIME'S LEDBETTER IS BULLISH ON MINISUPERS

NATICK, MASS.

A lot of people are busy worrying about how long the computer industry doldrums will last, but Carl S. Ledbetter Jr. is busy preparing for a boom. Ledbetter may have developed his penchant for optimism during his stint as chief earthquake emergency planner for California, an office he held five years ago, before taking on the newly created position of vice president for scientific programs at Prime Computer Inc.

In any case, it's his job to oversee Prime's entry into the minisupercomputer market. He believes that market is poised for a surge, and that Prime will be a major player. "We'll be in the business before 1987 is out," says Ledbetter, adding, "1987 is the watershed year."

LEDBETTER: 1987 will be the watershed year for minisupers.

Minisupercomputers fill the performance gap between current superminis and Cray-class supercomputers. More specifically, Ledbetter says the successful minisupercomputers will be those that are capable of sustaining an execution rate of 2 million to 6 million floating-point operations per second.

His optimism about this market is founded on evidence that the engineering and scientific—that is, the numerically intensive—computer markets have grown while the rest of the computer industry slumped. He predicts this sector will continue to outperform the industry as a whole by a factor of two or three for the next decade.

The growing demand for high-power computing has dramatized the gap in performance and attracted vendors. Some, such as Alliant Computers, are already selling machines. Many others are, like Prime, developing products as fast as they can.

Quite a few of the latter are building machines with exotic architectures, intended for narrow applications. But Ledbetter argues that the big winner will be the company that markets a general-purpose minisupercomputer, one with extremely stable performance characteristics for a broad range of applications.

Of particular importance to Prime is that a significant portion—40% by Ledbetter's accounting —of the instructions executed by supercomputers is for simulation and modeling in computer-assisted design and engineering. Prime has become an important player in that business in recent years. "The link between modeling, or CAD/CAM, and supercomputing is the key link," says Ledbetter. "The trick for us is to integrate with that environment."

Ledbetter, 37, earned his bachelor's degree from the University of Redlands in California, his master's degree from Brandeis University, and a doctorate in mathematics from Clark University. He has been a professor of mathematics at Wellesley College in Massachusetts and at Sonoma State University in California.

From December 1980 to August 1981, Ledbetter was director of the California Earthquake Preparedness Agency in the administration of former Gov. Jerry Brown. He then spent five years at IBM Corp. before joining Prime. Beginning at IBM as a senior research consultant, Ledbetter most recently oversaw the engineering, production, and marketing of IBM's vector-processing option for the 3090 mainframe.

At Prime, the effort to develop a minisupercomputer has reached the point where hardware may soon be moving out to beta sites, says Ledbetter. "I think we'll have a market opportunity of 12 to 18 months. Although others claim the ground, they're well below the performance of big mainframes in scientific work, so there's nobody ahead of us," he says. –*Craig D. Rose*

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IMS2800-10	Decode	53ns	100ns	176ns

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IMS2801-60*	Enhanced Page Mode	32ns	11ns	35ns
IMS2801-80		43ns	13ns	46ns
IMS2801-10		53ns	16ns	56ns

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ELECTRONICS NEWSLETTER

ARE THE JAPANESE VIOLATING THE NEW CHIP TRADE AGREEMENT?

Evidence that some Japanese memory chips were sold for prices below the foreign market values set by a new U. S.-Japan trade agreement is being evaluated by the U. S. Commerce Dept., according to the Semiconductor Industry Association. This is the first allegation of a violation of the pact, which was signed only Sept. 4. The chips involved are said to be erasable programmable read-only memories. One industry source says a U. S. user blew the whistle on a Japanese company after being offered cheap EPROMS in Hong Kong on Sept. 9. □

TI TO SELL TESTERS TO ITS IC CUSTOMERS

Texas Instruments Inc. is changing its policy of keeping internally developed manufacturing and test equipment closely guarded secrets. Not only will TI sell to its own IC customers a new high-speed integrated circuit tester it's developed, but managers hint the Dallas company is weighing a major push into the tester business. TI promises the new tester, called Impact-1, will cost less than existing systems, but has not yet announced a price. Impact-1 can perform both ac and dc parameter tests in a single pass on fast logic chips and is controlled by a 32-bit central processing unit. □

INTEL POISED FOR ENTRANCE INTO THE ASIC MARKET

Intel Corp. is about to announce its plans for marketing application-specific integrated circuits, industry sources say. The Santa Clara, Calif., company's announcement is expected this month—more than a year after Intel first said it would start selling ASICs. Sources say Intel will focus on standard cells, based on its rich array of proprietary products, and that Intel would license design tools from IBM Corp., since its own tools, built for semiconductor experts, aren't that user-friendly. Other sources say, however, that IBM's tools are no friendlier and that a licensing deal—which would be IBM's first—would probably be only for Intel's internal use. Intel won't comment. □

INMAN TO HEAD NEW HOLDING COMPANY IN THE DEFENSE INDUSTRY

An ambitious new holding company for defense and aerospace manufacturing is taking shape in Texas. It will be headed by B. R. (Bobby) Inman, the departing leader of the electronics research consortium, Microelectronics and Computer Technology Corp. He will become chairman and chief executive officer of Westmark Systems Inc., which will acquire promising defense companies with combined revenues of about $1 billion. It may also start operations aimed at new defense markets. When Inman quit at MCC, he said that he wanted to move from developing technology to applying it [*Electronics*, Sept. 18, 1986, p. 33]. Westmark will try to do just that. □

OPTIMISTIC SIA FORECASTS A 20% RISE IN 1987 SEMICONDUCTOR SALES

The Semiconductor Industry Association, known for its optimistic sales forecasts, lives up to its reputation with its latest prediction: sales worldwide will increase 20% next year. The figure comes from predictions by executives from U. S., Japanese, and European semiconductor firms. These annual forecasts have been consistently far higher than actual industry performance—the increase for 1986 was pegged at 25%; the actual number was a more modest 7%. The 1987 forecast is based on a slow increase in equipment markets and an end to price wars. The SIA says that sales this year will reach $26.5 billion, excluding captive markets, and it predicts $31.9 billion in revenues for next year. □

ELECTRONICS NEWSLETTER

CONSOLIDATION CONTINUES IN THE MAINFRAME BUSINESS

A foreshadowing of the next major consolidation in the mainframe computer industry came last week with word that Honeywell Inc. plans to negotiate a combination of its computer business with that of NEC Corp. of Japan and France's Bull SA. The Minneapolis company says it does plan to continue in the computer business. The Honeywell move, plus the merger between Burroughs Corp. and Sperry Corp. [*Electronics*, May 12, 1986, p. 76], indicates a major restructuring in the mainframe business as vendors struggle to compete against giant IBM Corp. Honeywell has had ties with NEC and Bull for a number of years. Only last July it announced plans to market NEC-built supercomputers in the U. S. and Canada. □

TI ASKS TO DELAY DELIVERY DATE ON COMPACT LISP MACHINE

Texas Instruments Inc., citing production gremlins, is asking for a new deadline to deliver its Compact Lisp Machine. Currently, the Defense Advanced Research Projects Agency must receive it by Nov. 30. The unit's 32-bit Lisp microprocessor is not yet fully functional, a TI spokesman says, after an initial fabrication pass this summer. But the 264-pin IC is operating well enough to conform to the letter of the August 1984 contract. With an extension into 1987, TI promises it will make the unit fully functional, plus deliver much more artificial intelligence software. The trouble, TI says, is mainly in the first-pass metal masks of the huge Lisp chip, fabricated in 1.2-μm CMOS and measuring 1 cm on a side. The chip contains an execution unit, a state microengine, 2.5 kilowords of 18-bit-wide dispatch memory, 1,000 32-bit words of scratchpad storage, and another 1,000 words of push-down list memory. [*Electronics,* March 31, 1986, p. 17]. □

HONEYWELL AND TI DEVELOP 10,000-GATE ARRAYS TO SPEED USE OF VHSIC

To help defense contractors overcome the long wait for some critical components in the Department of Defense's Very High-Speed Integrated Circuits program, both Honeywell Inc. and Texas Instruments Inc. are developing a 10,000-gate bipolar logic array. The two 1.25-μm arrays, each of which is to be introduced next year, are likely to be among the first of several semicustom products intended to speed up the VHSIC program. Honeywell's Digital Product Center in Colorado Springs is preparing what will be its largest bipolar array, the HMV 10000. It will be made with three-layer metal and will feature on-chip native pulse testing, Honeywell's version of scan testing. The bipolar array is being designed for military systems needing 180 to 200 input/output pins. In Midland, Texas, TI is planning to introduce a similar 10,000-gate VHSIC array in the first quarter of 1987. □

INTEL SAYS DECISION IN NEC TRIAL SETS MAJOR PRECEDENT

Intel Corp. expects its initial victory in a microcode copyright suit against NEC Corp. of Japan to protect not only its microprocessors but also peripheral devices, application-specific integrated circuits with silicon software, and other types of chips. Copyright protection was extended to microprograms stored on IC chips by a decision last week in the U. S. District Court in San Francisco. Still to be decided is whether NEC's V series microprocessors actually infringe on Intel's copyright and, if so, what damages NEC must pay. However, says F. Thomas Dunlap, Intel's general counsel, the Court's decision "sets a major precedent for the entire microprocessor industry." In Japan, NEC senior vice president Tomihiro Matsumura says, "This ruling is only a judgment on a part of the points in contention in this trial, and there is absolutely no finding that our firm has infringed on Intel's copyright." □

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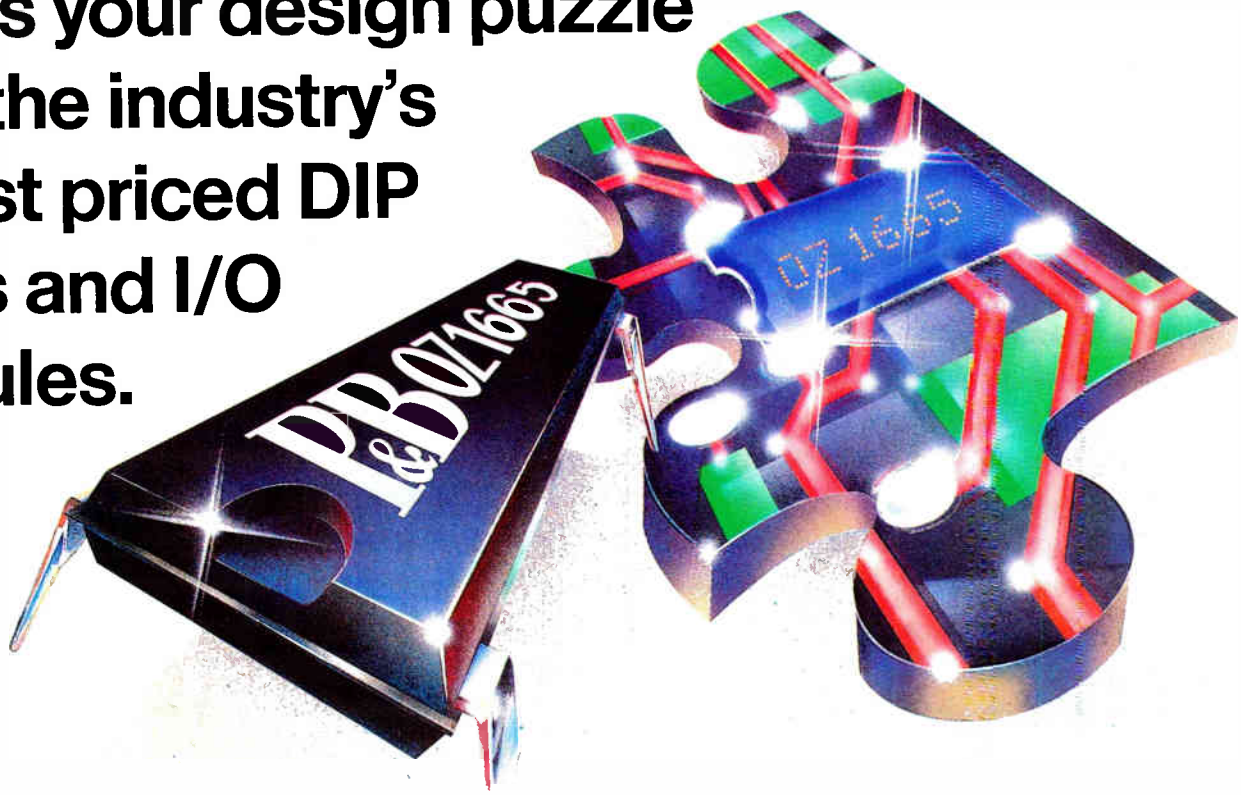

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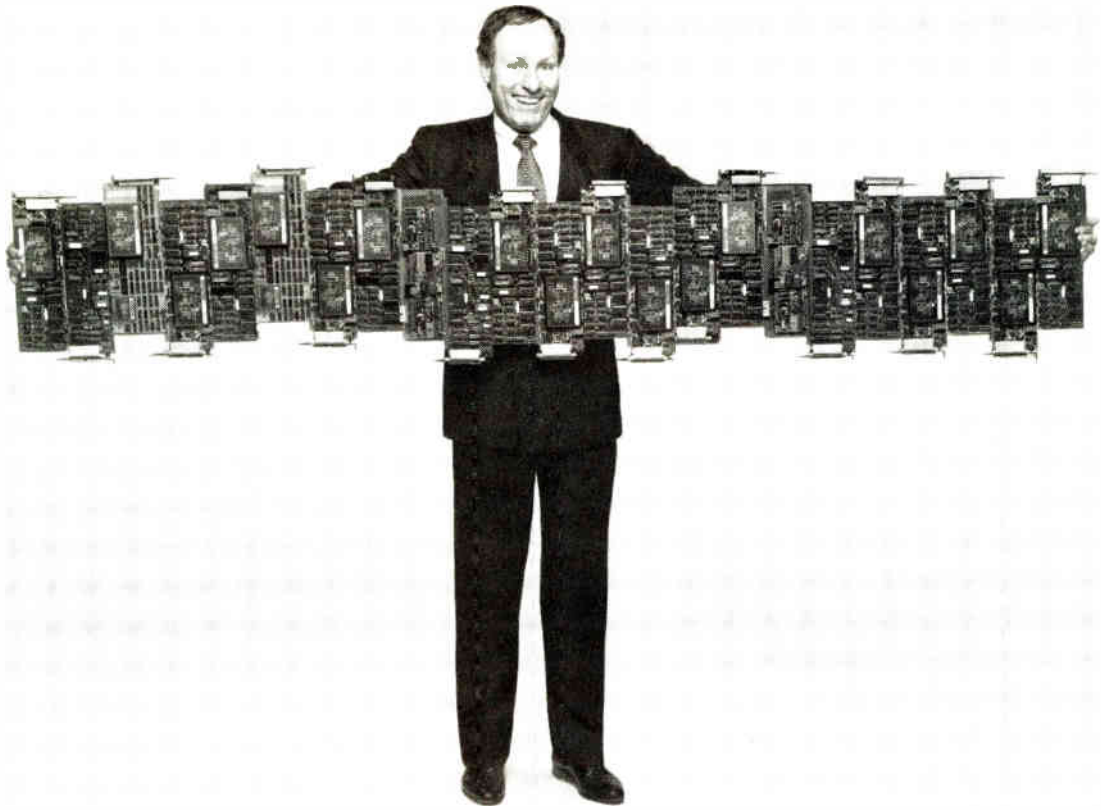

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	General Purpose DT2808	495	16	10	3 3	2	8	16	Yes	DT707
	Low Cost DT2814	395	16	12	25	–	–	–	Yes	DT757
	Low Cost DT2815	499		–		8	12	–	–	DT757
	Low Cost DT2817	199	–		–		–	32	–	DT758
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PRODUCTS NEWSLETTER

NEC CLAIMS FIRST MONOLITHIC DUAL-PORT FIFO MEMORY

NEC Corp. has developed what it claims is a ground-breaking first-in first-out memory—it has dual ports. Up until now, equipment manufacturers have had to implement equivalent functions as boards. Intended for use in communications and computer systems, the CMOS 32-K-by-8-bit μPD4532C can take data in or out asynchronously from either port with a cycle time of 100 ns. If necessary, chips can be connected in cascade for larger memory capacity. Shigeki Matsue, general manager of NEC's Memory Products Division, says the chip will require 95% less area and cost 20% to 33% less than boards. The chip's DRAM portion uses the same 1.3-μm n-MOS process and memory cells as the standard memory product but has a different layout. Logic, control, and data buffer circuits use the 1.2-μm CMOS process developed for the firm's 256-K SRAM. Because of the complex peripheral circuits required, the chip measures 7 by 8 mm, compared with the 4-by-7-mm size of standard 256-K DRAM. It comes in a standard 600-mil 40-pin plastic package. Samples will cost $65 in Japan when shipments start this month. □

SYSTEM STORES ENGINEERING DOCUMENTS IN OPTICAL MEMORY

Optical memory so far has been limited mostly to business systems, but now 3M Co., St. Paul, Minn., and FileNet Corp., Costa Mesa, Calif., are taking aim at a new area: engineering. The two are jointly developing an engineering-document management system based on write-once optical technology. The system will record, store, and automatically route drawings and other data throughout an organization. 3M will sell and support the system, with a variety of peripherals to fit individual requirements, worldwide. Price is yet to be determined, but the system should be ready by mid-1987, the cooperating companies say. □

CONVERGENT LURES OFFICE OEMs WITH MULTIUSER UNIX SYSTEMS

Hoping to attract a new class of original-equipment manufacturers and value-added resellers, Convergent Technologies Inc. is introducing a family of six Unix-based office systems. The San Jose, Calif., firm's S/Series Workgroup Servers can serve from 5 to 128 users. All use Motorola Inc.'s 68000 series of microprocessors; one, the S/640, uses the 25-MHz version of the 68020. The top-of-the-line S/1280 can be configured with up to four 68020s and one Intel Corp. 80186 microprocessor. There are two midrange computers, the 12-user S/120 and the 32-user S/220, and a new S/50 version of the personal computer that Convergent builds for AT&T Co., once its main customer. Prices range from $6,000 to $350,000. Four of the models are available immediately (the S/220 has been available in Europe since June); the midrange S/120 and the S/640 will ship in volume by the first quarter of 1987. Convergent has also introduced software packages supporting a variety of office automation and networking functions. □

CAD ACCELERATOR SPEEDS ROUTING ON PC BOARDS BY UP TO SEVEN TIMES

A new computer-aided-design accelerator that speeds automatic routing in printed-circuit-board design by as much as seven times is being unveiled this week at the Automated Design and Engineering for Electronics East Conference in Boston. The RPR-7 Autorouting Accelerator, from Calay Systems Inc., Irvine, Calif., is built with reduced-instruction-set-computer architecture as a single HCMOS chip that performs a single-cycle instruction in only 125 ns. On board the chip is a 2-megabyte two-port memory, which can be extended to 16 megabytes. The RPR-7 costs $19,500 and can be delivered in 30 days. □

PRODUCTS NEWSLETTER

$39,000 FAULT SIMULATOR HITS 2 MILLION EVENTS PER SECOND

The competition is heating up in low-end hardware accelerators for logic and fault simulation. The latest entry comes from Xcelerated Computer Aided Technology Inc., Minneapolis, Minn. The MXT-25, priced at $39,000, offers simulation speeds of 2 million events/s on as many as 16,000 modeling elements, and can serve as either a dedicated work-station accelerator or a network resource on systems based on Apollo computers, Digital Equipment VAX machines, or IBM Personal Computers. The new Xcelerated engine is a downward extension of the MX/MXT line that the 18-month-old firm brought out last June [*Electronics*, June 16, 1986, p. 21]. It comes on the heels of the debut of a new low-end system priced at $38,000 from industry leader Zycad Corp., St. Paul, Minn. [*Electronics*, Sept. 18, 1986, p. 27]. The earlier Xcelerated machines, priced at $49,000 to $295,000, offer the same 2-million-event/s performance as the MXT-25, but can handle up to 250,000 modeling elements. The MXT-25 is scheduled for first deliveries in November. □

HITACHI'S MEMORY CAN STORE TWO FULL LINES OF NTSC SIGNAL

Hitachi Ltd. has kicked off its fall season by announcing its HM63021P two-horizontal-line (2H) memory for video processing systems. The 2,048-by-8-bit line memory is fabricated using 1.3-μm CMOS technology and features five separate access modes: conversion to double scan frequency (for noninterlaced scan); alternate delay of 1 H and 2 H (for comb filters); time-base contraction or expansion (for picture-in-a-picture or multiplexed analog components); time-base correction mode (for video cassette recorders); and delay line mode. The chip's memory capacity is sufficient to store two full lines of NTSC signal. It can also store the display portion of two lines of a PAL signal, but not a retrace of the signal when sampled at four times the color subcarrier frequency. Input and output pins for the two horizontal lines are multiplexed to enable the device to fit in a 28-pin 300-mil DIP. Hitachi has not settled on prices for the memory chip. □

BOARD CONVERTS 8-BIT COMPUTERS TO 16-BIT SYSTEMS

A new single-board computer allows 8-bit systems built around the 6500 microprocessor family—used in a wide variety of personal computers, notably the Apple II and the Commodore 64—to be upgraded to 16-bit performance. The RMX65-1600 module, offered by Dynatem Inc., Irvine, Calif., is based on the 65C816 central processing unit and can act as the base for a new system by using existing RM65 modules to perform system functions—or it can replace the 8-bit system entirely. It has 128-K of on-board memory and can address up to 16 megabytes of external memory. Delivered from stock and without memory, the board costs $399. □

BACKLIT LCD SCREEN BRIGHTENS FUTURE OF ZENITH'S PORTABLE PC

Zenith Data Systems Inc., which turned into a leading contender in the portable computer market when it captured a 15,000-unit Internal Revenue Service order [*Electronics*, March 3, 1986, p. 16], wants to keep its momentum going by upgrading the computer's liquid-crystal display to an easier-to-read version similar to Data General Corp.'s latest portable LCD screen. Zenith's Z-181, which is equipped with a twisted-nematic backlit display, can be read easily in daylight or dimly lit rooms, something that couldn't be done with previous models. The new 25-line, 80-character screen, a backlit liquid-crystal display with adjustable brightness and contrast, is one-third larger than its predecessor screen and can be tilted to adapt to changing ambient lighting. Available now, the Z-181 costs $2,399. □

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SEIKO INSTRUMENTS

Circle 29 on reader service card

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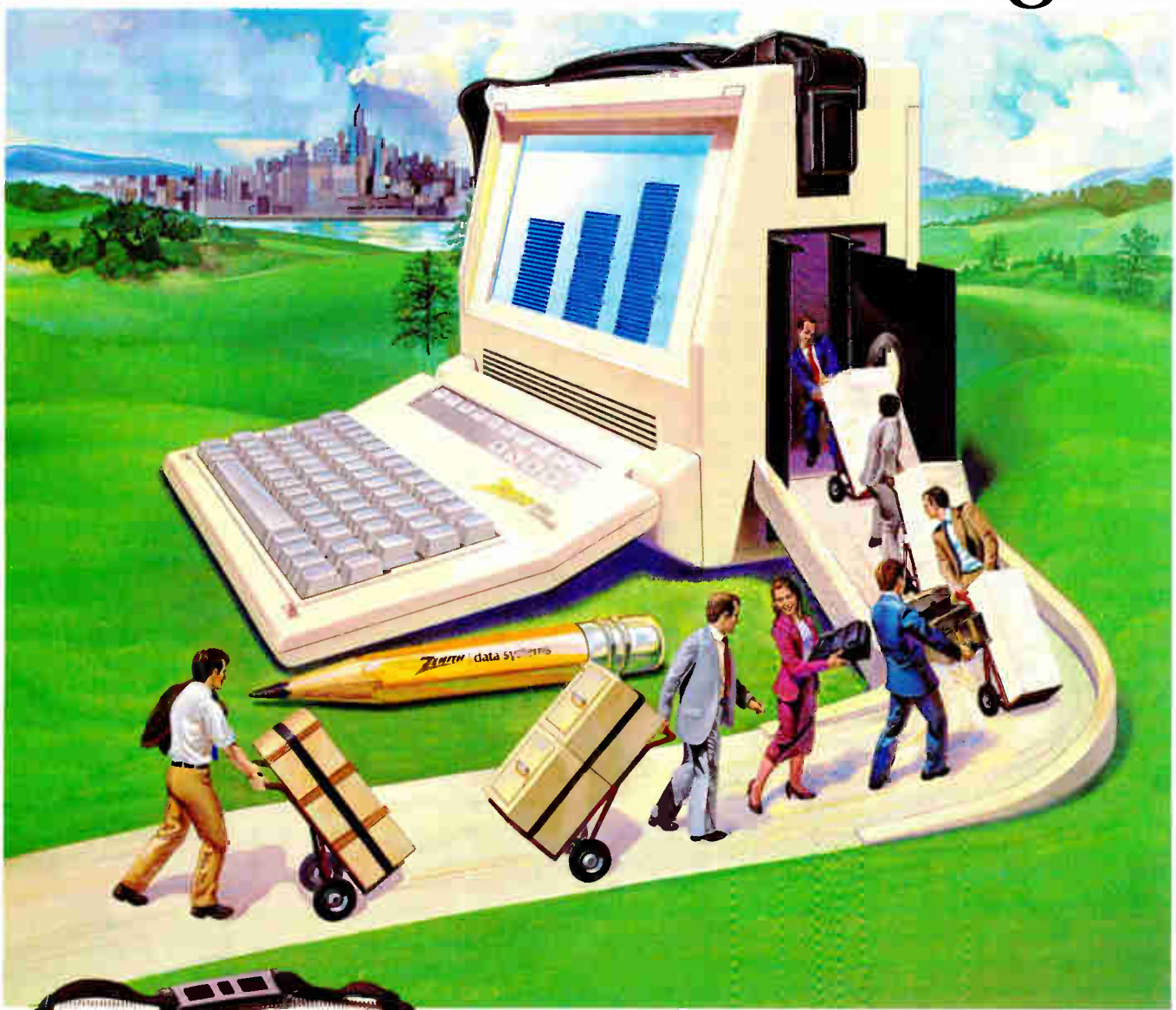

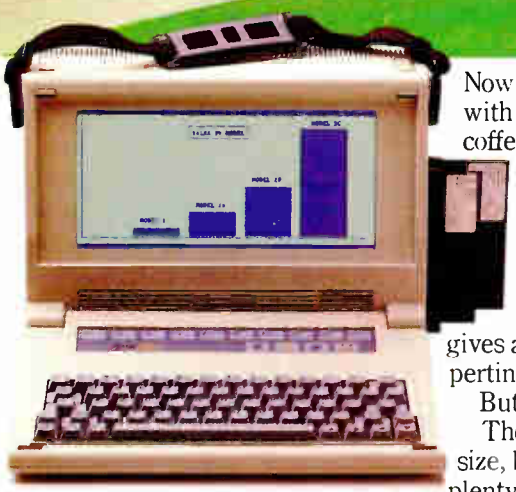

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Electronics

MICROWAVE AND DIGITAL CIRCUITS ARE COMBINED ON ONE GaAs CHIP

ROCKWELL IC GIVES RECEIVER HIGH SENSITIVITY AND CUTOFF FREQUENCY

NEWBURY PARK, CALIF.

Chalk up another milestone for gallium arsenide: a monolithic microwave-digital combo. Intended for military needs, the chip from Rockwell International Corp. will become a key component in L-band receivers using signals from the Air Force's Global Positioning Satellite (GPS).

Combining the digital and microwave functions on one GaAs chip is significant because of the improvements in frequency, sensitivity, and power consumption that doing so makes possible. In a conventional design, the microwave and digital tasks would be done on separate silicon chips, then packaged in a hybrid assembly. GaAs offers a particularly high cutoff frequency, about 26 to 30 GHz, compared with silicon's 4 to 8 GHz, according to Rockwell scientists.

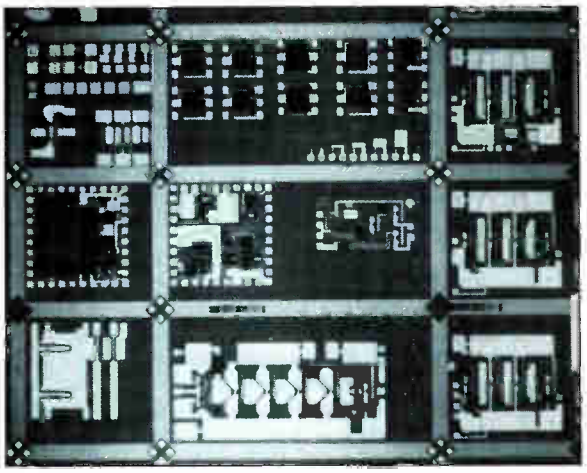
This makes the GaAs chip ideal, they say, for the GPS receiver and for the integrated avionics systems that use data from the GPS. The receiver detects phase-modulated signals at 1,575.2 and 1,227.6 MHz, and the avionics systems receive signals from 30 to 2,000 MHz. Rockwell's amplifiers are matched to achieve gains of 40 dB at 200 MHz and 25 dB at 1.66 GHz.

PAYOFF. One significant payoff of a monolithic microwave-digital chip, sources say, is improved receiver sensitivity. This results from reduced capacitance in the integrated circuit: devices can be much closer together on the chip than they are on a hybrid.

To build the monolithic device, Rockwell used enhancement/depletion-mode metal-semiconductor field-effect transistor technology. All functions were implemented using a single mask set.

One of the challenges in developing the device was finding a way to tune the microwave and digital circuits independently. Rockwell uses a combination of features to pull this off. Among these are self-aligned MES FET gates, implanted resistors, and a range of implantation conditions.

The self-aligned digital section of the chip includes both enhancement-mode and depletion-mode transistors with 0.8-μm gate lengths. The microwave portion uses depletion-mode transistors with gate lengths of 0.6 μm. In tests, power-supply requirements ranged from 2 to 5 V, and the circuits operated at frequencies from 10 MHz to 2.2 GHz.



COMBINATION CHIP. Rockwell has built digital MES FETs and microwave MES FETs (at upper left) on a single GaAs chip.

Fabricating the chip is considered an important step ahead for GaAs. "It's certainly of interest, since it's in a real-world application," says Lou Tomasetta, president of the Integrated Circuit Division of Vitesse Electronics Corp., the first company to bring a line of GaAs chips to market [*Electronics*, Sept. 18, 1986, p. 61]. Although a microwave-digital chip might be implemented in silicon, "it would be touch-and-go, and the frequency would not be as high," he says.

Consultant William I. Strauss, of Forward Concepts Inc., Tempe, Ariz., is intrigued with the idea of GaAs ICs moving into a visible military role. The L-band application, he says, gives promise of the "very next step," which would be a similar application of GaAs in a receiver for commercial direct-broadcast satellites and earth stations. "It's the same kind of thing, although not in the microwave frequencies," Strauss notes.

The monolithic chip was developed at Rockwell International Corp.'s GaAs pilot line at its Microelectronics Research and Development Center in Newbury Park. The part is being built for a sister Rockwell operation, the Avionics Group, Microwave Technology, Cedar Rapids, Iowa. The Avionics Group has a contract for GPS gear.

The chip is one of the first to roll off Rockwell's GaAs line, one of three funded by the Defense Advanced Research Projects Agency as a source for military GaAs ICs. Opened late last year, the pilot line is revving up to meet a 100-wafer-per-week goal by next April, and is now at the 40-wafer mark, says Conilee G. Kirkpatrick, director of the Microelectronics R&D Center. Producing at this level already "gives us more GaAs fabrication experience than anyone else," she claims. *–Larry Waller*

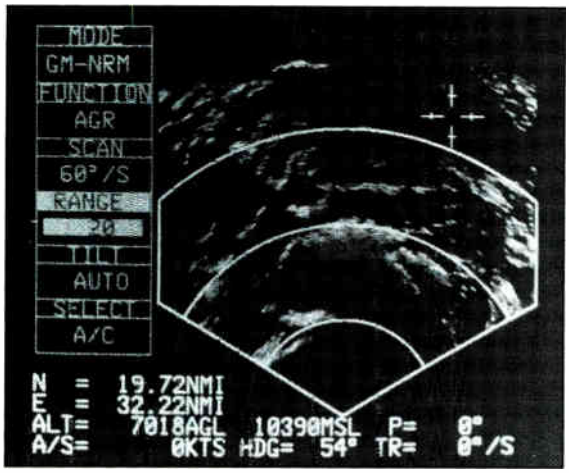
MILITARY

EXPERT SYSTEMS GIVE PILOTS A HELPING HAND

DALLAS

Combat pilots may have more of a fighting chance in future battles, thanks to new computer simulation tools and expert systems. Software developed by Merit Technology Inc. will now let them rehearse the missions and evaluate their flight plans.

Dallas-based Merit is merging the power of color graphics and expert systems into simulation software that runs on a variety of systems. The Battle Area Tactical System (BATS) previews missions with displays of out-the-window views, three-dimensional maps, landmass radar screens, and instrument



LOOKS REAL. Merit's system mimics a landmass radar—or other types—and is much cheaper than hard-wired systems.

readings—all working from digital terrain data from the U.S. Defense Mapping Agency. Merit has also developed some multiprocessing hardware for the project that it feels has applications in testing algorithms developed for the Strategic Defense Initiative.

BATS is an outgrowth of Merit's avionics engineering software [*Electronics*, Dec. 16, 1985, p. 28]. It is targeted at the pilot and mission planner.

FUEL AND FOES. Part of the package applies expert systems to grading the fuel efficiency of various flight paths. Another portion checks exposure to known enemy threats. Other software modules include one with terrain-following algorithms and others for threat avoidance, route planning, and trajectory generation. An altitude-generation expert system enables BATS to calculate optimum flight altitudes for avoiding enemy detectors without crashing.

Merit's software can also generate preflight reports. Done by hand, these reports can take pilots hours to complete. Hard copies of flight maps, which pilots take on missions, can be produced by plotters in a few minutes.

Along with the mission-planning software, Merit has some new hardware that, among other things, runs a radar generator used in the radar simulation part of BATS. The generator, which can have up to a dozen 68020 microprocessors and 40 megabytes of memory, is based on standard VMEbus modules and a System 1000 chassis from Motorola Inc. It mimics the displays of landmass radars that pilots watch during flight, using input from the digital terrain data base.

The VMEbus hardware is targeted at a wide range of "multiprocessor, rapid-reaction, brassboarding applications," says George L. Bair, director of systems engineering. Merit modified the System 1000 backplane to accommodate 20 VMEbus modules and is using it to build a 10-processor navigation system for a large defense airframe maker.

Most of Merit's changes to Motorola's standard VMEbus product have been made in the VersaDOS operating system, extending utilities to support concurrent processing. For radar simulation, the hardware performs three different forms of multiprocessing simultaneously. On the fly, Merit's software reconfigures the 68020-based boards to perform tasks using combinations of parallel-processing, pipelining, and distributed-computing techniques.

The use of multiple VMEbus computer modules results in a programmable radar simulator at about 20% of the cost of hardwired versions, which can cost up to $5 million, says Bair. Merit anticipates that the system could be used to train student pilots, who do not usually see modern radars in operation until they get time in an expensive flight simulator. The VMEbus system can simulate a wide range of multiple-mode radars found in modern jet fighters.

Merit engineers are also working on multiprocessing concepts that would aim the VMEbus hardware at benchmarking the complex algorithms being developed for SDI. "Conceptually, we have designed a system with 220 processors [each a 68020-based computer board] by hooking 22 VMEbus systems together with a high-speed local-area network," says Bair. *–J. Robert Lineback*

SEMICONDUCTORS

JAPANESE HEMT ICs RUN AT ROOM TEMPERATURE

TOKYO

Logic and memory chips made with high-electron-mobility transistors turn off many system designers even before they start to use them, because they generally require refrigeration to liquid-nitrogen temperatures—77 K—for high performance. Now, however, several groups in Japan are working on device configurations or materials that promise to make the transistors useful at room temperature.

At Oki Electric Industry Co.'s Research Lab in Hachioji, near Tokyo, a group is working on an inverted HEMT structure that reduces source resistance—one of the central problems in getting HEMTs to work at room temperature. Source resistance is especially degrading to device gain because it is common to both the input and output circuits, and therefore introduces negative feedback.

Sony Corp.'s Research Center in Yokohama, also near Tokyo, is using a more conventional device structure while emphasizing improved metallurgy to cut source resistance and obtain higher electron mobility.

At Oki, senior researcher Seiji Nishi says the company appears to be the only Japanese firm that has published the results of work on inverted HEMTs. Other groups have rejected the configuration because it increases the difficulty of growing the HEMT structure with the high-mobility two-dimensional electron gas required for high-performance devices. But Nishi says his group has solved the problem.

The most advanced HEMTs fabricated so far at Oki have an aluminum gate 0.5 μm long. At room temperature, logic gates have a propagation delay of 19.7 ps and use 0.212 mW each.

More representative of production technology is a 6-by-6-bit multiplier made on a 1,024-gate array fabricated with 0.8-μm gate length and 10-μm gate width. The device achieves a multiplication time of 6 ns. Of the devices fabricated on the same wafer as the multiplier, the highest-performance individual HEMTs have transconductances of 400 millisiemens per millimeter of gate width at room temperature and 550 mS/mm at 77 K. Source resistances are as low as 0.7 Ω-mm at room temperature and 0.54 Ω-mm at 77 K.

NO HETEROJUNCTION. Oki has succeeded where others have failed in growing high-quality GaAs crystals on top of aluminum gallium arsenide and thus achieving high mobility in the 2-d electron gas of an inverted HEMT structure. In Oki's inverted configuration, the doped AlGaAs layer that induces the electron-gas layer in the undoped GaAs layer is located below rather than above the GaAs (see diagram). This configuration lowers source resistance because it eliminates the heterojunction at the source contact.

In conventional HEMTs, the heterojunction between the overlying AlGaAs layer and the GaAs layer makes it necessary to alloy the contacts down to the 2-d electron gas. However, the gas has about five times the sheet resistance of the Oki device's n^+ GaAs layer, which acts as an extension of the metallic ohmic source contact located 2 μm to

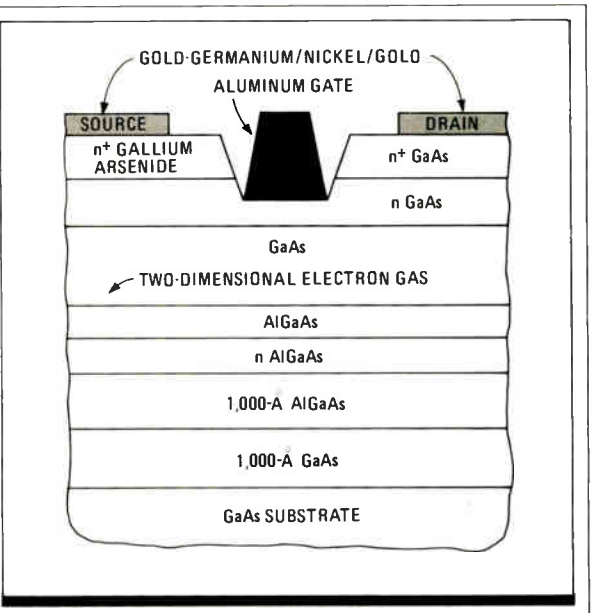
one side of the gate. The device's source resistance is therefore considerably lower than a conventional HEMT's.

Source resistance is much less of a problem in conventional HEMTs used as high-frequency amplifiers, because the single transistors or microwave integrated circuits can be fabricated with smaller source-contact-to-gate spacing by electron-beam lithography. But logic and memory devices with thousands or tens of thousands of devices must be fabricated with optical lithography having larger minimum dimensions.

SONY DEPOSITS. Sony, for its part, is using a conventional HEMT structure but is working with different materials. The company's researchers are using n-doped aluminum indium arsenide and undoped gallium indium arsenide because of their high 2-d electron-gas mobility and a high discontinuity at the band edge. They also fabricate devices with a metal-organic chemical-vapor deposition process they think is more suitable for production than the molecular-beam epitaxial process used by others.

Senior researcher Mikio Kamada says his group is the first to grow devices on semi-insulating indium phosphide by metal-organic chemical-vapor deposition. He further notes that Sony is using the deposition process for production of commercial 12-GHz HEMT transistors for direct-broadcast-satellite TV receivers.

UPSIDE DOWN. In its room-temperature HEMT, Oki has put the AlGaAs layer that induces the electron gas below rather than above the GaAs layer where the gas resides.



Despite the conventional device structure that Sony is using, Kamada says the HEMT devices have very low source-contact resistivity—0.3 Ω-mm at room temperature with a source-to-gate spacing of 1.4 μm. This was achieved because the higher mobility and band-edge discontinuity of AlInAs/GaInAs allow the 2-d electron gas to retain high mobility at high electron concentrations, to give about 10% the sheet resistance of devices fabricated with GaAs/AlGaAs. Transconductance at room temperature is a respectable 302 mS/mm, even though the HEMTs have a fairly long gate: 1.5 μm. This should translate into good performance—particularly as gates are shortened—but Sony has not yet measured it. *–Charles L. Cohen*

NETWORKING

TI PARES CHIP SET FOR IBM TOKEN RING

HOUSTON

Texas Instruments Inc. isn't resting on its laurels with its chip set that integrates protocols and processing functions for IBM Corp.'s token-ring local-area network. It is pushing development of a two-chip set, code-named Eagle, that will replace the five members of TI's current TMS320 family of token-ring adapter chips [*Electronics*, Oct. 21, 1985, p. 56]. Prototypes of the second-generation chip set will become available no sooner than next spring.

LAN product managers in Houston say TI is readying a 1-μm CMOS circuit that integrates three of its five current-generation TMS380 token-ring adapter chips onto a single 132-pin device. The new chip, under development at TI's facility in Bedford, UK, will incorporate the functions of the 38010 communications processor, the 38020 protocol handler, and the 38030 system interface chip. It will be housed in a surface-mountable flat pack.

TI is also combining the functions of its two bipolar ring-interface devices onto a single 44-pin bipolar integrated circuit, the second member of the two-chip set. Other additions planned for its ring-LAN family include software for developing application-specific interface ICs to go with the chip sets, and firmware for handling higher-level protocols.

The new CMOS chip will incorporate a series of throughput-boosting enhancements in the communications processor core of TI's adapter architecture. For starters, the processor's memory address space is being expanded from the current 96-K bytes to 2 megabytes. This will make it easier for the adapter chip set to handle higher levels of networking protocols than are currently embedded in the five-chip set.

TI is also making a number of minor tweaks to the data-path architecture of the communications core unit. Register-file caches have been added to the communications processor block, and the processor will execute some new instructions. The changes will add up to a two- to threefold performance boost, says John Hughes, LAN product manager in Houston. "We have done a lot of performance analysis and identified some bottlenecks in the ways the current chip set does things," he says.

Two new ICs will replace five current ring-adapter chips

Hughes asserts that TI's two-chip adapter will be just as compatible with IBM's token ring as the five-chip set, which resulted from IBM-TI joint development. Compatibility is being tested against a body of test cases developed jointly. Hughes also hints that the two companies are maintaining a relationship to keep future LAN-adapter products on a compatible path. "There are ongoing programs that I cannot discuss. Some are carryovers from the original development project," he says.

$25 IN 1990. TI aims to drive down the cost of an adapter chip set from about $125 today to about $25 for the two-chip set in volume quantities by 1990. This past summer, TI announced it was cutting the 1987 price of the current five-chip set to $88 in quantities of 25,000.

The Eagle chips will not hit the market before TI makes three other product introductions to its current TMS380 offering. It will soon announce the 38021 protocol handler, which will support internetworking, such as for gateway adapters to other LANs, or bridges to multiple token-ring networks. The 38021 will replace the current 48-pin 38020 protocol handler; its functions will be included in the Eagle chip.

Later this year TI will introduce a software tool kit that will help automate the design of ASIC interfaces between the TMS380 adapters, the system backplane, and LAN-card expansion memory. Once a customer completes a design on

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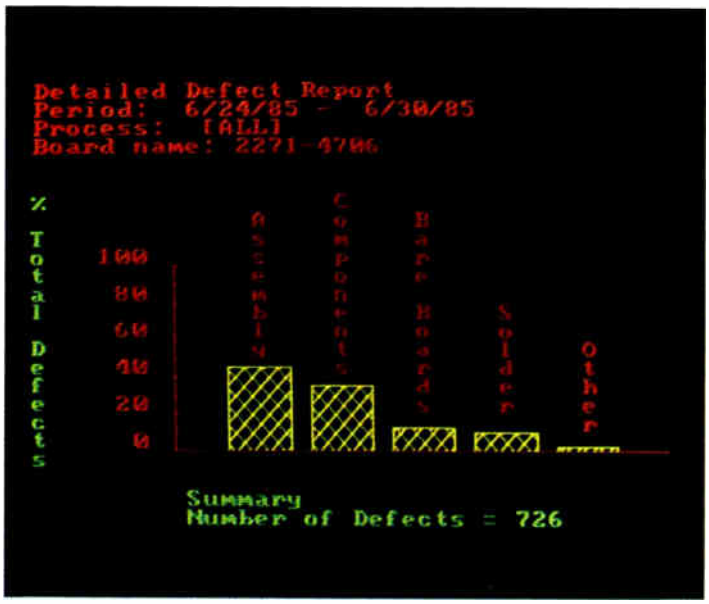

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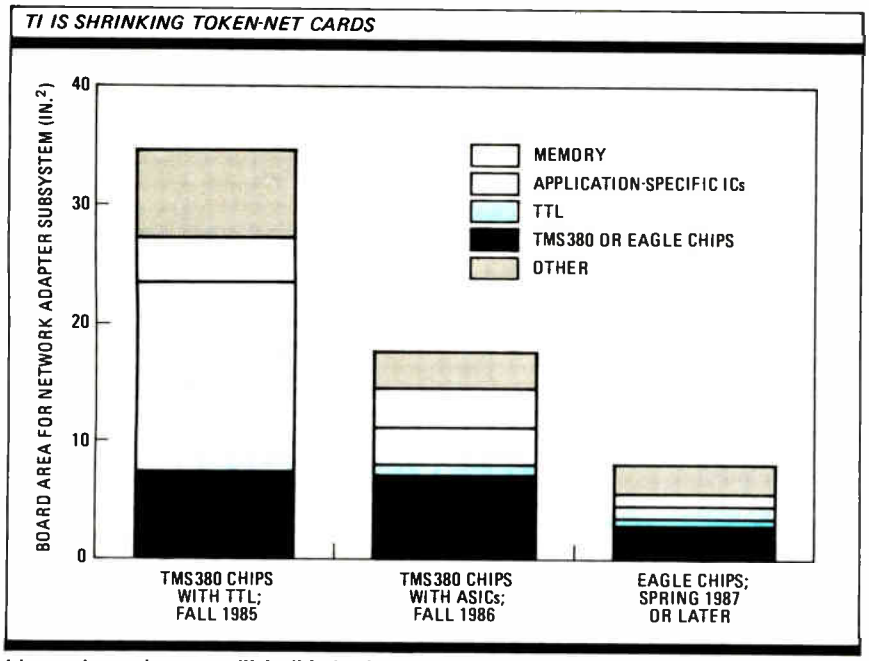


his work station, TI will build the interface IC using its 2-μm CMOS standard-cell library.

The ASIC tool kit should help reduce adapter board-size requirements by nearly half (see chart). When available, the two Eagle chips will further reduce board space to less than 8 in^2.

And by the end of the first quarter of 1987, TI is planning to move its TMS380 support up one more step on the token-ring protocol ladder with the introduction of firmware for IBM-compatible (and IEEE 802.2-compatible) logic-link control. Firmware for the physical layer and the medium-access control level protocols already resides in the 38020 protocol handler. *–J. Robert Lineback*

CARD IS INTERIM SOLUTION FOR MODEM IN MAP NETS

ANN ARBOR, MICH.

Factory networkers are still waiting for chipmakers to fully integrate the front-end analog and digital circuitry of carrier-band modems that work in networks based on the Manufacturing Automation Protocol. So Allen-Bradley Co. and Industrial Networking Inc. are racing to get a partial solution on the market. Their plan: integrate only the digital portions of a modem, using a gate array.

A number of manufacturers, including Motorola Inc. and Siemens AG, already have full-blown MAP carrier-band chips in the works to do both analog and digital integration [*Electronics*, Sept. 4, 1986, p. 32]. But Motorola's single-chip MC68194 won't be available in production quantities until the first quarter of next year at the earliest. Siemens declines to say when its product will arrive, but industry sources think it won't be until the second quarter of 1987.

By contrast, Allen-Bradley's Communication Division in Ann Arbor says that by December it will offer a card-level product built around a CMOS gate-array chip from Fujitsu. The device won't include the amplifier, clock-recovery circuitry, and other analog devices that will be on the fully integrated chips. But it will replace about 20 digital devices. As a result, boards using it will cost half as much as current board-level MAP carrier-band products, says Michael T. Klein, engineering supervisor for the division's LAN component technology group. The boards will also cut power consumption and size by 50%.

Allen-Bradley plans to use the gate array in its own line of industrial-automation products and has no plans to market the chip. But there is one change in Allen-Bradley's strategy since it was acquired by Rockwell International Co. in February 1985: the company now plans to sell a board-level product based on the chip to original-equipment manufacturers.

OEM DEALS. At last month's MAP/TOP Users Group meeting in Ann Arbor, the company unveiled a series of MAP product agreements, including an OEM deal with Data General Corp., at the same time that it announced the new carrier-band product. Several more OEM deals are in the works, Klein says.

The carrier-band card is based on a single-height VME board. Initially, it will go for about $600, says Kevin Hughes, manager of MAP product marketing at Allen-Bradley's Communication Division. The card will implement the IEEE 802.4 carrier-band standard for the physical layer of the MAP specification. A second token-bus controller board will be required to implement the remaining layers, 2 through 7, of the MAP protocol, adding $2,000 to $3,000 to the price per node.

Price per node for the just-emerging MAP carrier-band market will hover between $2,500 and $5,000 from various vendors next year, Hughes predicts. As volume ramps up and full-blown single-chip modems become available, that is expected to drop as low as $500.

Industrial Networking Inc., Santa Clara, Calif., has developed a similar product, also unveiled at the MAP/TOP meeting. Using a CMOS gate array, to be supplied by Toshiba Ltd., the device likewise integrates only digital portions of the modem. The company has as yet set no timetable for delivery of products using the chip. "We're just announcing that we've reached a significant milestone," says Davis S. Fields, product marketing manager. He declines to speculate on when a product might appear. *–Wesley R. Iversen*

THE NEXT STEP FOR MAP: FIBER-OPTIC NETWORKS

ANN ARBOR, MICH.

Now that the Manufacturing Automation Protocol is nearing reality for factory networks based on coaxial cable, MAP proponents are beginning to look more seriously at MAP nets based on fiber-optic media. Both AT&T Co. and General Motors Corp. plan to launch experimental fiber-optic MAP networks before the end of the year. And at last month's MAP/TOP (Technical Office Protocol) Users Group meeting in Ann Arbor, officials announced the formation of a MAP special-interest group chartered to identify standards from which a MAP fiber-optic specification can be written.

The advantages of fiber-based MAP networks include immunity to electromagnetic interference in noisy factory environments, higher bandwidth, and improved security compared with nets

using coaxial cable. So far, though, the lack of fiber-optic standards has impeded development. Another obstacle has been disagreement over the best topography for a fiber-optic network.

Nevertheless, AT&T plans, in the next few months, to bring up an experimental fiber-optic MAP network in one of its factories, according to Louis W. Weigle, manager of industrial information systems planning and management for AT&T in Berkeley Heights, N.J. Which factory it will be has not been disclosed.

WEIGLE: AT&T may soon be using fiber MAP nets.

The company will use MAP board- and box-level products supplied by Concord Communications Inc., Marlboro, Mass., which will be modified by AT&T for use with fiber. "We've already got a lot of fiber in our factories, and our objective is to determine whether and where we can use MAP," Weigle says. Unanswered questions include the cost of a fiber-based MAP system, the number of devices that can be connected, and whether adequate MAP performance can be achieved with fiber.

Weigle declines to speculate on the answers to those questions. But if the effort pans out, he says, AT&T could be using fiber-based MAP production networks in its factories by early 1988.

GM is also about to test a fiber-optic MAP network, in an Oshawa, Ont., plant beginning in November. The network will initially link up about 10 robots in a net, says a GM manager. The company plans to evaluate by mid-1987 the technology's potential for use on an Oshawa assembly line, linking some 500 robots.

More manufacturers may join AT&T and GM soon, as the obstacles to fiber optics are overcome. A working group of the IEEE 802.4 token-bus subcommittee known as 802.4H is nearing completion of a proposed standard for 10- and 20-Mb/s fiber-based token-bus local-area networks. "My hope is that we'll have something we can take to the 802.4 subcommittee for a vote by about January of 1987," says Robert S. Crowder, 802.4H chairman. If that schedule is met, a final standard could be approved before the end of 1987, says Crowder, the president of Ship Star Associates Inc., a Newark, Del., MAP/TOP consulting firm.

However, Crowder says the 802.4H group is divided on the question of topology. One camp favors a passive-star topology, and the other is backing an active-star approach.

A passive star uses no active elements in the hub, but depends on a fused-fiber cluster that optically divides an incoming signal and passes it to all other nodes. An active star, on the other hand, transmits optical signals from a node to a central unit that contains a transmitter/receiver pair for each node on the net. There, the signals are amplified and retransmitted to all other nodes.

COMPARING STARS. Passive-star backers contend that the passive approach will be more reliable than an active star, since a power-supply failure or some other glitch in an active star's hub could bring down the whole net. Active-star backers say their approach can be significantly cheaper, since it gets by with less powerful and thus less expensive transmitters. Furthermore, an active star can be more easily extended to support large networks, since messages are amplified in the central hub, and signal loss is not dependent on the number of nodes.

Both AT&T and GM are testing passive-star nets. Crowder says the final 802.4H draft standard will likely call for some combination of active and passive approaches. *–Wesley R. Iversen*

IC TESTING

FAULT IMAGING MOVES FROM LAB TO FAB

SANTA CLARA, CALIF.

One of the best ways to spot flaws in circuit design or fabrication processes of logic integrated circuits is to catch logic errors on the fly, as the chip is running. And several chip makers have been catching them in the laboratory for the past five years or so using a scanning electron microscope.

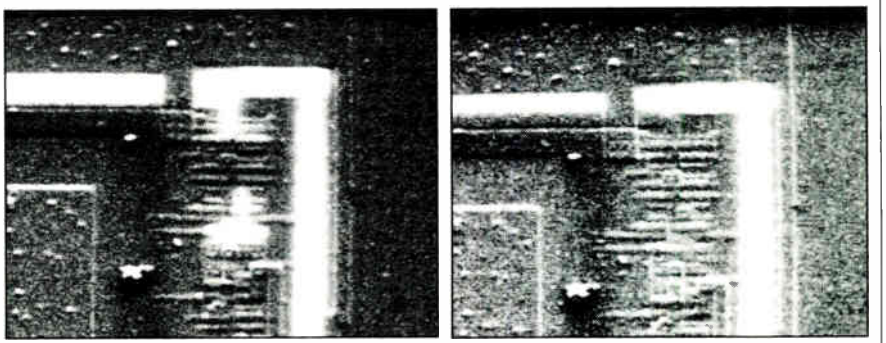
For Intel Corp., dynamic fault imaging by SEM has worked so well in the laboratory that the Santa Clara company has turned the technique into a test bed for production devices. The imaging systems, including SEM equipment from several vendors, wide-bore optics, and a Digital Equipment Corp. MicroVAX work station, are already operational in two plants, with three more installations planned, says Jack Salvador, manager of quality and reliability at Intel's Microcomputer Group.

The dynamic fault imaging systems display logic levels as light and dark spots on an SEM image of the chip. Successive images of the chip show internal error paths. Errors show up at once, therefore, rather than after they have propagated internally until they reach an output pin.

The process is similar to the kind of transistor-level failure analysis previously available only for memory chips, the regularity of which permits them to be raster-scanned. Logic chips change states in such an irregular fashion, though, that raster scanning is not feasible, and systems that probe a single logic node have too narrow a field of view to permit analysis of a complex chip.

The Intel system uses a strobed SEM beam, synchronized to the system clock, to record a sequence of images representing successive logic states. Errors can be detected by image processing, in which frames from tested devices are compared with similar frames from devices known to be good. Intel's home-designed optics permit its system to see lines as small as 2 μm over an entire 1-cm-square chip in a single scan.

A "NICE PICTURE." Other firms are working with SEM equipment for fault tracing as well. "It's an ideal machine for that kind of application," says Harry Wachob of Failure Analysis Corp., in Palo Alto, Calif. "When you use an electron beam to generate an image of a circuit with a voltage applied to it, you



BAD AND GOOD. The small upside-down white "T" near the middle of the image on the left pinpoints faulty logic, when the image is compared with that of a known good chip (right).

MC68020 vs. 80386.

How to run apples-to-apples vs. apples-to-oranges benchmarks on these archrival 32-bit MPUs.

Choosing the world's highest-performance 32-bit microprocessor should be as easy as making an apples-to-apples comparison with such industry-standard benchmarks as Whetstone and Dhrystone performance.

How to tell apples from oranges.

When pulling an apples-to-apples comparison, anyone, anywhere, should be able to easily duplicate the comparison factors and results. Repeatably.

Attempt no. 1.

So, when comparing the MC68020 and 80386, the first task is to find one of each.

Motorola expects to ship over a quarter of a million MC68020s this year, so finding one of them shouldn't be too difficult. Get the fastest available—a 25 MHz—and a 20 MHz Motorola floating-point coprocessor, the MC68881.

Next (things get harder), try to get your hands on a fully functional, bug free 80386 MPU and 80387 floating point.

And now you know why it's so hard to make an apples-to-apples comparison: you can get the Motorola devices, but "comparable" '386 and '387s? No way. You have to settle for the slower '386 and the promise of silicon yet to come on the '387.

Attempt no. 2.

All right, if you can't find the chips, go for readily-available 32-bit systems and compare real, live, '020- and '386-based systems from the commercial market.

Exasperating, isn't it? There are hundreds of choices of commercially-available, '020-based systems. But, finding comparable '386-based systems...?

Attempt no. 3.

Running real benchmarks on real products is the best comparison. We've looked at two questionable comparison attempts. Now it's time to try some industry-standard approaches, such as Whetstone and Dhrystone benchmarking. That should allow an apples-to-apples comparison, shouldn't it? If not, at least it should be apples-to-apples on paper.

Here are currently-available Whetstone and Dhrystone procedures for the MC68020 and the 80386 32-bit processors. To use industry-standard methods of comparison, you'll have to—must—rerun the Whetstones and Dhrystones for the '386 along the same universally-accepted lines as for the '020.

And discover which has the greater potential for being a keystone and which for being a millstone in your new design. The MC68020 is *still* the highest-performance microprocessor no matter how you slice it!

WHETSTONE PERFORMANCE

The Whetstone is a standard double-precision, floating-point benchmark written in FORTRAN.

MC68020/68881

- Execution of standard Whetstone benchmark written in FORTRAN: recognized and run by all leading systems manufacturers (Cray, DEC, IBM, etc.).
- Double-precision floating point: specified by standard Whetstone for high accuracy.
- Complete, 10-loop-count execution: 1 million Whetstone instructions.
- Unary instructions executed: specified by standard Whetstone; single-operand operations.
- Entire Whetstone benchmark procedure was not modified from the original standard: no tricks or tweaks to hype performance.

Result: 1.24 million Whetstones/second with commercially-available silicon (68020, 68881).

80386/80387

- Execution of vendor-modified Whetstone benchmark written in C: nobody else in the industry uses this particular procedure.
- Single-precision floating point: non-standard Whetstone sacrifices accuracy for "performance."
- Incomplete, 2-loop-count execution: only 200,000 Whetstone instructions.
- No unary instructions executed: intentional '386-vendor modifications to Whetstone spec avoids single-operand operations.
- Altered Whetstone benchmark procedure allowed '386 vendor more favorable results: avoided branch control overhead.

Result: Claims that have no apples-to-apples comparison to reality.

DHRYSTONE PERFORMANCE

The Dhrystone Benchmark measures CPU performance on a typical mix of high-level language statements.

MC68020

- Dhrystone results measured on commercially-available system: Sun Microsystems 3/200 workstation.
- Commercially-available operating system (UNIX®).
- Commercially-available UNIX® C compiler (cc).
- Real-world memory architecture: Dhrystone WRITE operations must pass through to main-memory DRAM.

Result: 6362 Dhrystones with commercially-available, real-world systems.

80386

- Dhrystone results measured on specially-modified "hot box" built by '386 vendor: '386 "starter kit" version not commercially available.
- No operating system used: '386 vendor used own modified debug monitor.
- '386 Vendor used own internal "beta" version of C compiler: not commercially available.
- Utopian memory architecture: zero-wait-state WRITE operations to unlimited cache SRAM —no write through to main memory.

Result: Claims that have no apples-to-apples comparison to reality.

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can paint a very nice picture of where the charges and voltages are."

Siemens in Europe, and IBM and some instrumentation firms in the U. S., are also investigating SEM techniques, according to Giorgio Riga of Riga Analytical Laboratories in Santa Clara; but, he says, "Intel is among the most advanced users of the technique."

In the production environment, Salvador says, Intel hopes to use dynamic fault imaging as a test bed for automated test systems, analogous to the "bed of nails" used to test printed circuit boards. The setup won't be simple, though. To test one of Intel's 80386 microprocessors at full clock rating will require running 132 high-performance coaxial lines through a vacuum wall.

When a fault is detected, the test vector is set to loop where the fault begins, and the propagation paths can then be traced. Signals that get onto a bus can propagate anywhere on the chip, Salvador notes. They may remain on the chip for dozens of logic states before showing up at a pin. "When we were designing quad gates, there were 12 pins for four gates, or three pins per logic node," Salvador says. "Now we may have 70,000 nodes and only 96 pins—more than 700 nodes per pin."

On the production line, Salvador says, dynamic fault imaging can contribute to yield enhancement. "If you can double the rate at which you come down the learning curve, you get increased volumes and can drop prices sooner," he notes. He concedes, though, that the technique is still in its infancy.

EARLY SUCCESS. The technique has had successes already, however. One Intel chip was redesigned after the imaging system tracked errors to metal that had been eroded during life testing. Further investigation turned up a violation of design rules, which had caused the metal lines to be laid down improperly.

"We haven't quantified savings on dynamic fault imaging," Salvador says. "That would be difficult, because we are looking at a failure mode that historically we haven't been able to find at all."

Systems already are operational at Intel's Santa Clara and Aloha, Ore., fabrication plants. By the end of the year, systems will be installed at fabs in Folsom, Calif., and Chandler, Ariz. A fifth system will go into Panang, Malaysia, in 1987, Salavador adds. *–Clifford Barney*

TELEVISION

SIEMENS FITS DIGITAL TV INTO 2-Mb/s DATA STREAM

MUNICH

In their search for an efficient data-reduction method to help digital television transmission get off the ground, researchers at Siemens AG have developed a technique that sends moving TV pictures at a rate of just 2 Mb/s without any discernible loss of picture quality.

This cut in data rate from the 140 Mb/s needed now will come in handy, especially in the upcoming integrated services digital networks. These nets carry data at 64 kb/s or multiples of that rate up to 2 Mb/s, which is expected to become the standard—probably toward the end of the decade. The enormous rate reduction will help communications authorities make better use of available cable capacity.

Experts at Siemens' Corporate Research Center in Munich are now implementing their scheme, based on a mathematical technique called discrete cosine transformation, in hardware. The discrete cosine transformation (DCT) is a special Fourier transform taking into account only a signal's cosine function.

The equipment, says laboratory manager Eckart Hundt, will be ready for use in public networks when the 2-Mb/s rate becomes standard. It could be used before then in local and private networks where no standards exist.

Still not satisfied, Hundt and his associates are now working out the basics for reducing the data rate even further—to 384 kb/s, and eventually to 64 kb/s. At 64 kb/s, the Siemens technique, simulated with a computer, already produces pictures of acceptable grade. Hundt says more work should result in high-quality pictures even at this comparatively low rate.

Normally, in a series of TV images flashed onto the screen at 30 frames/s (25 frames/s in Europe), only a small portion of the picture content varies from one image to the next. So the most obvious scheme for achieving data reduction would be to transmit only the picture variations. But that would reduce the data by only a factor of 5 or 10, which is a long way from getting a 140-Mb/s data rate down to 2 Mb/s, let alone 64 kb/s.

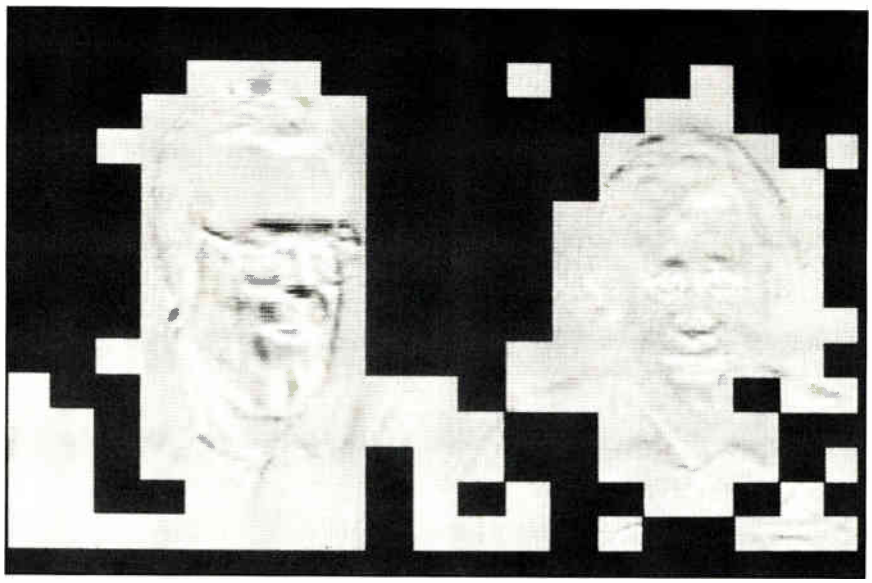
The DCT provides for a substantially larger reduction. In the DCT method that Siemens, like other firms around the world, is pursuing, the TV picture is first divided into blocks, each block containing, say, 16 by 16 picture elements.

EFFICIENT COEFFICIENTS. Assigned to each block are coefficients that exactly describe the picture content of that block. Each coefficient, a real number, characterizes a certain signal frequency. Because of their probability distribution, these coefficients lend themselves to data reduction much better than, for example, the intensities of individual pixels.

DCT then checks whether the assigned coefficients vary from picture to picture, and determines the magnitude of any variation. If the differences are minor, all variations are transmitted.

If, however, the differences are substantial, as with abrupt movements in a TV scene, only the most significant variations are transmitted. The minor variations and details are sent in subsequent pictures. The casual observer hardly notices the image buildup and manipulation. Only when the viewer closely scrutinizes the picture is a slight and temporary loss of sharpness discernible during abrupt movements on the screen.

Good as the basic DCT method may



PARTIAL IMAGE. Siemens sends only an image's moving parts (light areas) to cut data rates.

be, Hundt and his team believe it can be improved upon to provide much better pictures. Toward that end, the Siemens experts have come up with a special coding technique based not only on normal DCT and difference pulse-code modulation but also on the detection of groups of coefficients in the transform domain, on adaptive Huffman coding, and on postbuffer control.

As researcher Walter Tengler explains it, in this improved technique the energy of each coefficient is measured, and the coefficients to be transmitted are defined. They are classified in three groups, one containing coefficients representing sharp movements, the other with coefficients standing for less pronounced movements, and the third containing weak-movement coefficients. A Huffman coder determines which coeffients occur frequently and which do not. Frequently occurring coefficients are assigned shorter codes.

DESCRIBING DETAILS. This classification and code-assignment scheme, Tengler says, significantly reduces the amount of data needed to characterize movements and, consequently, picture variations. And as less data is needed, more space is made available for coefficients that describe picture details.

The Huffman-coded coefficients are written into a buffer whose output is a constant 2-Mb/s data stream. By controlling the quantization process, as well as the process of differentiating between various degrees of movement via a feedback loop, the output buffer ensures that picture quality is maintained.

At 2 Mb/s, the Siemens technique makes for excellent TV images, even when picture details change rapidly. The ultimate goal is high picture quality even at 64 kb/s. At this low rate, however, the pictures cannot be sent at full resolution. Instead of the normal resolution of 540 by 575 pixels, the resolution at 64 kb/s is only one-third that value, or 360 by 288 pixels. And only 8.33 frames are transmitted each second.

To avoid having the movements in such pictures appear jerky, as in early silent movies, the missing pictures are generated with the help of a small computer. It performs an interpolation of available images and inserts the missing images into the stream. First investigations of this scheme have produced good results. *–John Gosch*

SPEECH TECHNOLOGY

SCORING 98.6% IN SPEECH RECOGNITION

CAMBRIDGE, MASS.

One small step for a young Cambridge company may point the way to a giant leap forward in speech recognition. Voice Processing Corp. is reporting the highest accuracy yet for a speaker-independent continuous-speech recognition system with an 11-word vocabulary. Moreover, the company says its work indicates its algorithms may be applied to large vocabularies without a crushing level of complexity.

The accuracy reported by Voice Processing—98.6%—is the highest yet claimed for a system of its type, which differs from speaker-dependent and isolated-word systems. The four-year-old company takes an approach to speech recognition that relies more heavily on linguistic knowledge and feature extraction than others working in the field.

The company's prototype system now requires a Symbolics 3600 minicomputer and executes about 35 times more slowly than it should to qualify as a real-time system. However, the algorithm used will allow the company to implement a faster version of the system using microprocessor-based hardware within a year, says David Shipman, vice president of research and development.

BENCHMARKED. Voice Processing has tested its system on a benchmark called the Connected Digit Database, developed by Texas Instruments Inc. and distributed by the National Bureau of Standards. This data base comprises more than 75 utterances, averaging three to four words in length, from each of 220 adult speakers.

The roots of the Voice Processing system can be traced back to Victor Zue, a professor at Massachusetts Institute of Technology who is an expert at reading voice spectragrams and who is a consultant to the company.

SHIPMAN: Voice Processing's spoken-digit recognizer could run on a microprocessor.

Although linguistic knowledge plays a large role, the system does not try to mimic someone who is an expert spectragram reader, says Shipman, because "that is too cumbersome computationally." And it is not an expert system, at least in the narrow sense of software depending primarily on an elaborate series of yes-no questions. "We have yes-no [rules], but also a lot of algorithms where a definite set of procedures leads to something else," says Philip Kromer, vice president of engineering.

In a demonstration, an average speaker's recitation of a Zip Code is followed by the display of a spectragram. Then the system segments the spectragram into phonemes based on spectral discontinuity and phonetic duration. It creates phonetic hypotheses for each segment on the basis of spectral patterns, phonetic context, and phonological rules.

Kromer emphasizes that feature extraction taking place at this point covers a very broad spectrum. "Anything goes," he says. "A feature can be anything from something simple, such as a duration, to something pretty complex requiring a complex algorithm to do it, such as trying to localize a 'k' burst, usually concentrated around 1,800 Hz."

Finally, the system selects from among the hypotheses it has generated. Elapsed time from speech to numerical display is about 35 s for a Zip Code.

Several outside speech-recognition experts say that even though it is in developmental form, the work is significant. They question, though, how easy it will be to extend a knowledge- or rule-based system to larger vocabularies.

John Makhoul, manager of speech signal processing at Bolt Beranek and Newman Laboratories, Cambridge, for one, calls the Voice Processing results good. However, he says his experience has been that acoustic/phonetic knowledge-based systems do not generalize to larger vocabularies. The problem, he notes, is that as vocabulary size increases, the number of rules required quickly grows unmanageable. For this reason, he and others believe the long-term solution will combine a knowledge-based approach with statistical modeling.

William Meisel, president of Speech Systems Inc. in Tarzana, Calif., says Voice Processing's results are the best he's heard of for digits. But he adds that the value of such work is extremely limited. The utterance of digits represents something between isolated-word and continuous-speech modes, he argues. In addition, "you're looking at less that one half the phonemes when you

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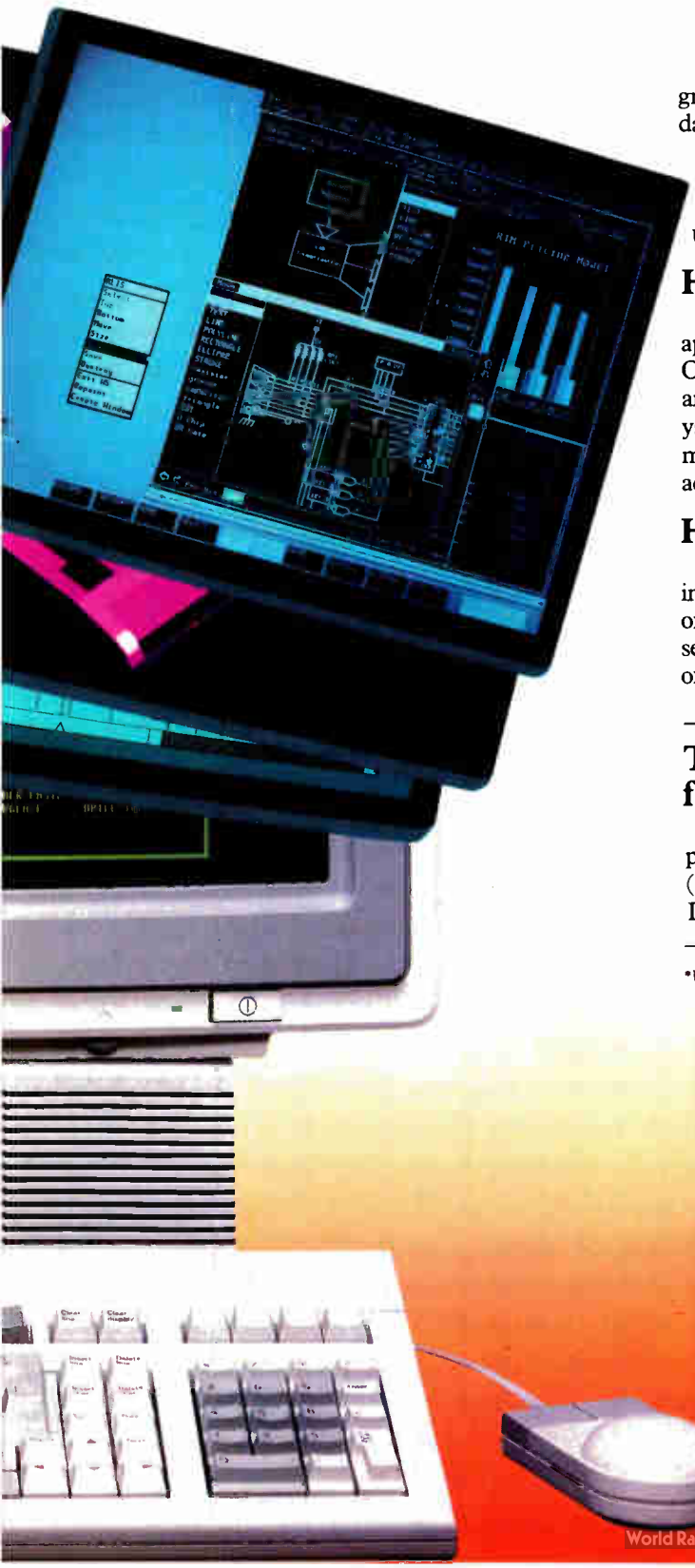

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look at digits... I don't think that gives you perspective on continuous speech."

Shipman maintains that the utterance of digits is a form of continuous speech. But he agrees with Makhoul that both knowledge-based and statistical approaches will be required for large-vocabulary systems. "You're a fool if you ignore statistics," he says. The emphasis at this point, he argues, should be on knowledge-based systems extracting information from the bottom up, starting at the sample level.

In the meantime, Voice Processing is optimistic about the potential for applying its system to larger vocabularies. Kromer acknowledges that the work with digits involves only about 20 phonemes, about half of those in the language. But he says the code used for digit recognition has been tried with minimal modification on other words and has worked well.

"It would be wrong to say it won't require more work to extend to a large context," he says. "But it seems to be very robust and extensible to large vocabularies." The growth in the number of rules with vocabulary, he adds, appears to be linear or somewhat faster, but remains manageable in its computational demands. *–Craig D. Rose*

GRAPHICS

GRAPHICS TABLET TRIES TO COMPETE WITH MOUSE

FAIRFIELD, CONN.

The mouse may be the king of the low-end market for graphics input devices, but Summagraphics Corp., a leading maker of both mice and electronic tablets, is in the midst of setting what may turn out to be a mousetrap: a new type of tablet that can be produced for less than half the cost of conventional tablets. The company is already showing pre-production units to customers.

By using a charge-ratio, or capacitive, technique to determine the x-y coordinates of an electronic pen-point, Summagraphics was able to strip out much of the electronic circuitry required for conventional tablets, which rely on electromagnetic technology.

OFF THE BOARD. Although the company's higher-end—and higher-priced—electromagnetic tablets need 14 multiplexing chips to run the x-y grid, the capacitive approach uses none of these chips at all. Other circuitry was also eliminated, making it possible for all control hardware to be moved off the main board. Similarly, the complicated grid system used in electromagnetic tablets—one double-sided printed circuit board to determine the x and y coordinates, plus a second board to aid in focusing—has been replaced by a single, one-sided board.

Furthermore, charge-ratio tablets require considerably less power for operation. The new tablet runs on a 5-V supply, as opposed to the 12-V supply required by electromagnetic ones.

The added simplicity does not come free. Resolution is 200 lines/in., one-fifth that of the company's Microgrid II tablets, and accuracy is down to about 50 mils, as opposed to the 10 mils Summagraphics quotes for its top-of-the-line product.

Still, such high levels of resolution and accuracy are not needed on the low end, where price has made mice the preferred input device for most applications, according to chief technical officer Paul Smith. A mouse typically costs under $200, much less than tablets, which cost about $600 and up, but the tablet, he says, is the faster and more accurate input method "because you don't have to run from corner to corner like a mouse—you can hop.

"With the charge-ratio technology, we will trim the price of tablets to a point where they can start cutting in on some of the mouse applications—like data entry, paint programs, and business graphics," Smith says.

At least one competitor, however, thinks Summagraphics is off-base in its analysis of the market. "I don't think the mouse and tablet are competitive technologies," says Philip Schlosser, vice president for research and development at Scriptel Corp., Columbus, Ohio. "The people who do computer-aided design simply won't use a mouse, and you don't need a tablet for most non-CAD applications. Besides, the tablet takes up about four to five times the area of a mouse—it needs too much space."

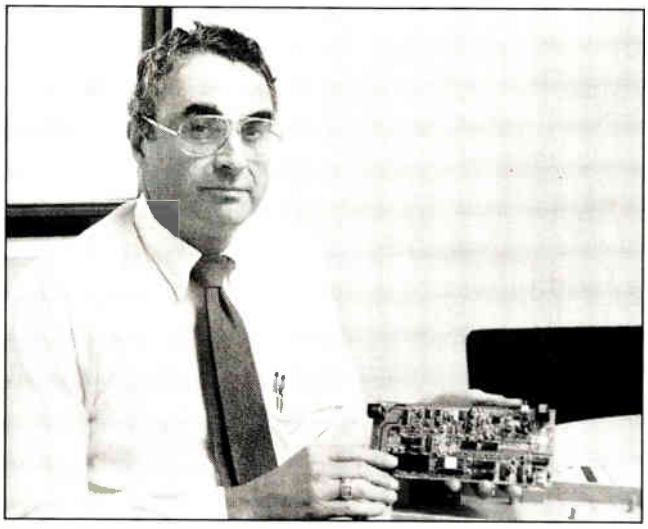
But Smith says many users will move up to the higher accuracy of the tablet, given a competitive price. "We expect this technology to open up brand-new applications for people who never thought of using tablets before." To further cut production costs, Summagraphics is talking with chip makers about reducing the controller-board components to just two or three very large-scale integrated circuits—a move that could cut the manufacturing cost of a tablet to as little as $50. Once that happens, Smith says, Summagraphics will really "begin attacking the mouse."

DIFFERENCES. The main difference between charge-ratio technology and electromagnetic technology, Smith explains, is what drives them. Electromagnetic tablets are current-driven, establishing a pair of crisscrossing electromagnetic fields that can be used to determine a sensor's position. Charge-ratio tablets are charge-driven and use a capacitive effect. The system has three electrodes—one each for the x and y coordinates, and a third that "fills in the remaining area" around the coordinates and helps to fine-tune accuracy. By measuring the charge levels at each electrode, one can determine location, since the three relate to one another such that the sum of their values will always be the same.

Another difference between the two tablet approaches is the main pc board. Although it appears to be made up of a series of parallel contacts, the charge-ratio board is actually coated with an interlocking array of wedge-shaped strips that are wider on the left than on the right, and a series of bars, with thinner bars at the top and thicker ones toward the bottom. The wedges drive the x coordinates; the bars drive the y coordinates.

The charge-ratio technology is similar to the charge-division scheme developed earlier by Scriptel. Schlosser says Scriptel "abandoned that technology because it was susceptible to noise in many environments." Smith claims no such problem affects the Summagraphics tablets.

–Tobias Naegele



MOUSETRAP. Low cost could make charge-ratio tablets competitive with mice in low-end graphics jobs, says Summagraphics' Smith.

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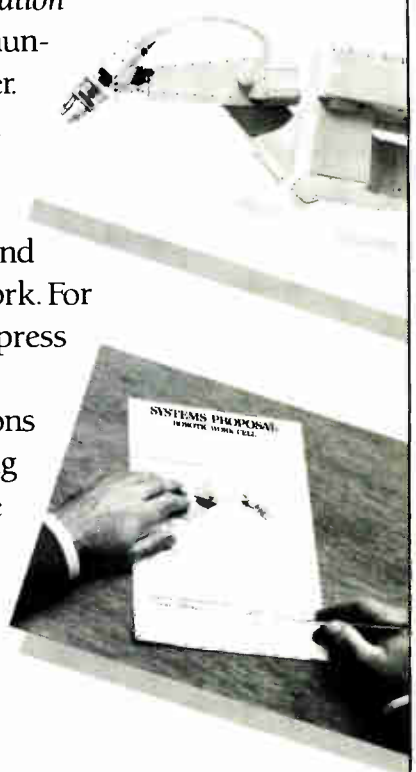

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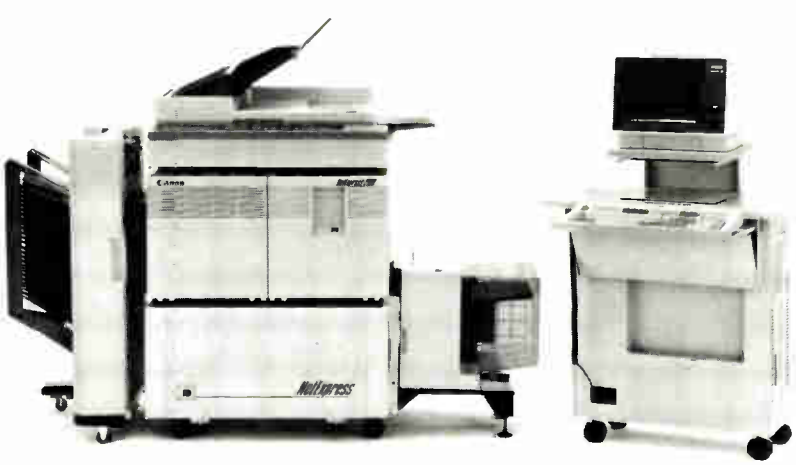

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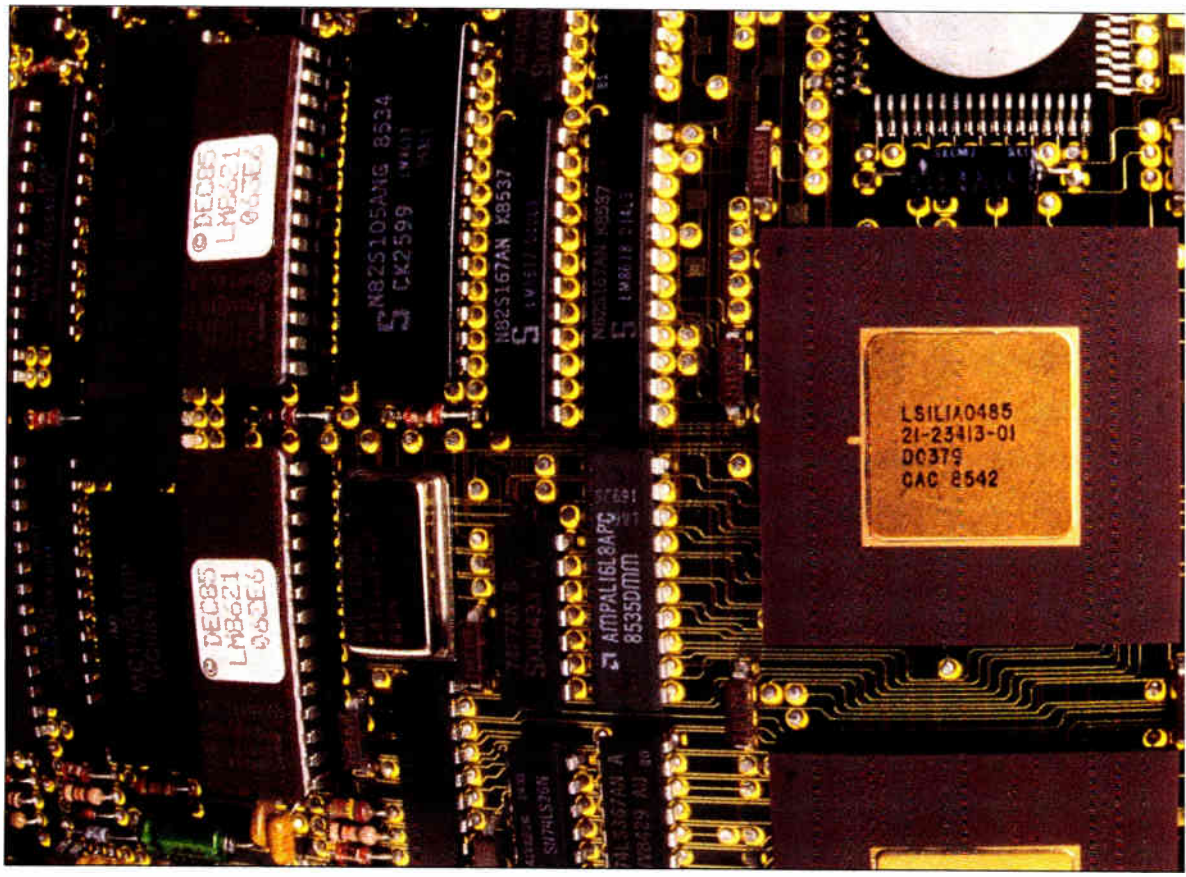
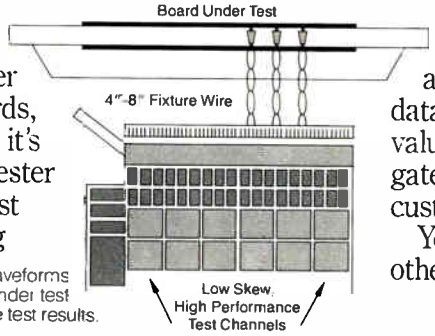


Introducing Teradyne's L210i. The only true VLSI in-circuit tester.

There are a lot of other in-circuit testers out there. But on VLSI boards, all they test is your patience.

Now there's the L210i VLSI In-Circuit Tester from Teradyne. It has over 3,000 bidirectional test pins. With digital, analog, and memory testing on every pin. And 10 MHz pattern rates.

Most importantly, the L210i delivers 95% or greater fault coverage on VLSI boards, in just 1–2 months. Because it's the first and only in-circuit tester that handles the three biggest problems in in-circuit testing today.



The L210i delivers waveforms accurately at the board under test for repeatable test results.

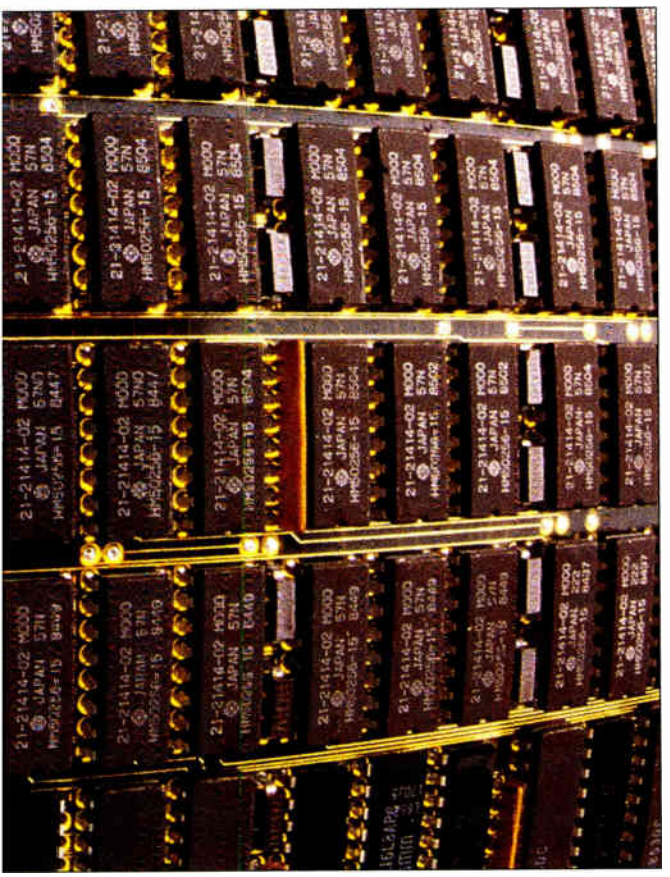
Test ASIC's ASAP.

One of the biggest problems for in-circuit testers today is ASIC's. If they detect ASIC faults at all, it's only because you've spent weeks and weeks programming them.

Not so with the L210i. It has a unique VLSI device tester architecture. So you can use patterns from device design and test databases. The L210i's translators convert patterns quickly.

Plus, the L210i stores and processes lengthy test data efficiently. So you save valuable time in testing gate arrays and other semi-custom devices.

You won't find that in any other in-circuit tester.



Repeatability. Repeatability. Repeatability.

With the L210i, you won't be plagued by unreliable tests of your high performance logic. False clocking. Or shifting signal timing.

Because the L210i features short, low inductance fixture wiring. Superb driver electronics. And powerful debug tools. So everything you test gets tested repeatedly. Including high speed ECL and FAST.* Even Advanced Schottky and CMOS, with their tricky overdrive impedances.

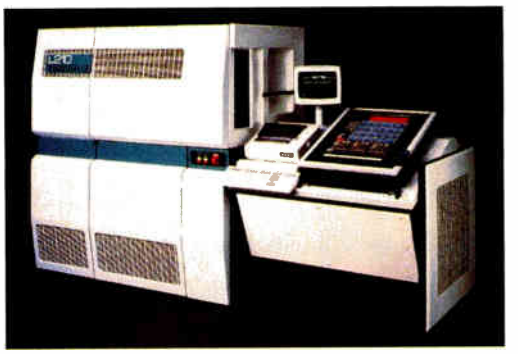
The L210i fears no logic.

The only in-circuit tester with an escape hatch.

The L210i is the only in-circuit tester that's flexible enough to test today's SMT clusters. Memory arrays. Or hard-to-isolate devices.

With its MultiMode capability, you can easily partition the board into functional clusters, making the most of the L210i's functional test and diagnostic techniques.

That means you'll never be trapped by in-circuit testability problems again.



The L210i is Teradyne's first board tester for VLSI in-circuit testing, and in-circuit tester budgets.

No-fault insurance.

Teradyne's L200 family has set the standard for VLSI board testing in this decade, driving test quality up to bring costs down.

Now the L210i offers the first practical VLSI in-circuit test solution. It's the system you need to boost board yields at system test. And make your in-circuit test strategy successful.

If you can't afford a tester that misses VLSI faults, you'd better find out more about the L210i. Write Teradyne, 321 Harrison Avenue, Boston, MA 02118. Or call Daryl Layzer, L200 Product Group, 617/482-2700, ext. 2808.

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INTERNATIONAL NEWSLETTER

NEW EXCISE TAX IS BAD NEWS TO JAPANESE MAKERS

Japanese consumer electronics manufacturers, still reeling from an increase of more than 60% in the value of the yen against the dollar, are preparing to absorb another blow. In order to maintain demand, they believe they will have to hold prices steady while absorbing additional excise taxes. Starting Oct. 1, video cameras, camcorders, video-disk players, compact-disk players, prerecorded video tapes, video disks, and compact disks were added to the list of consumer products on which excise taxes must be paid. The levy starts at 5% of factory price, rising to 10% after one year and 15% after two years, except for tapes and disks; their rate will remain at 5%. Manufacturers say they will try to make up for the new tax by reducing production and distribution costs. □

PHILIPS WILL UNVEIL A CCD CHIP WITH 2 MILLION DEVICES

Now in development by Philips International NV's Electronic Components & Materials (Elcoma) Division at Nijmegen in the Netherlands is an 835-Kb charge-coupled-device memory that packs the equivalent of 2 million transistors on a 27-mm² chip. The chip uses a 1.3-μm modified CMOS process, with one metal and two polysilicon layers. The memory, a store for video signals, will go to market in late 1987 or early 1988. Scheduled for introduction later on is a CCD chip using submicron technology and boasting three times the density of the 835-Kb version. Elcoma's predecessor CCD chip is a 300-Kb version that packs 700,000 transistor equivalents on a 24-mm² chip. □

JAPAN SEEKS A ROLE IN SETTING STANDARDS FOR OPEN SYSTEMS

Japan's Ministry of International Trade and Industry is resisting overtures from the Corporation for Open Systems, which began a drive to enlist Japanese companies as members with a seminar at Tokyo's prestigious Imperial Hotel. A MITI official says that the U. S. group should meet with its Japanese counterpart, the Promoting Conference for Open Systems Interconnection, and its European counterpart, the Standards Promotion and Application Group, to develop protocols and certification procedures for subsets of standards set by the International Standards Organization. MITI wants Japan to have an equal voice with the U. S. and Europe in setting standards. On the other hand, COS president Lincoln D. Faurer says that his organization will share information with the Japanese and European groups, but that its decisions will be made only by its members. If the Japanese want a vote, they'll have to join up. □

IBM RELEASES MORE OPEN-SYSTEMS SOFTWARE ONLY FOR EUROPE

IBM Corp. once again has released a software package for Open Systems Interconnection that is available only in Europe. Like the first one, this package is for System/370 computers; it will help applications written for its Systems Network Architecture work with applications written for systems conforming to the OSI model. The new package, called the General Teleprocessing Monitor for Open Systems Interconnection, "extends OSI communications into the heart of the SNA world," says Henri J. Vidil, manager of the OSI marketing center at IBM's La Gaude research laboratory in southern France. The new package provides programming tools to make it easier to write OSI levels 6 and 7 protocol-conversion routines so that OSI and SNA applications can talk with each other. The earlier software, Open Systems Transport and Session Support, implements the protocols in the fourth (transport) and fifth (session) layers of the OSI Model. IBM won't say when either will be available in the U. S. □

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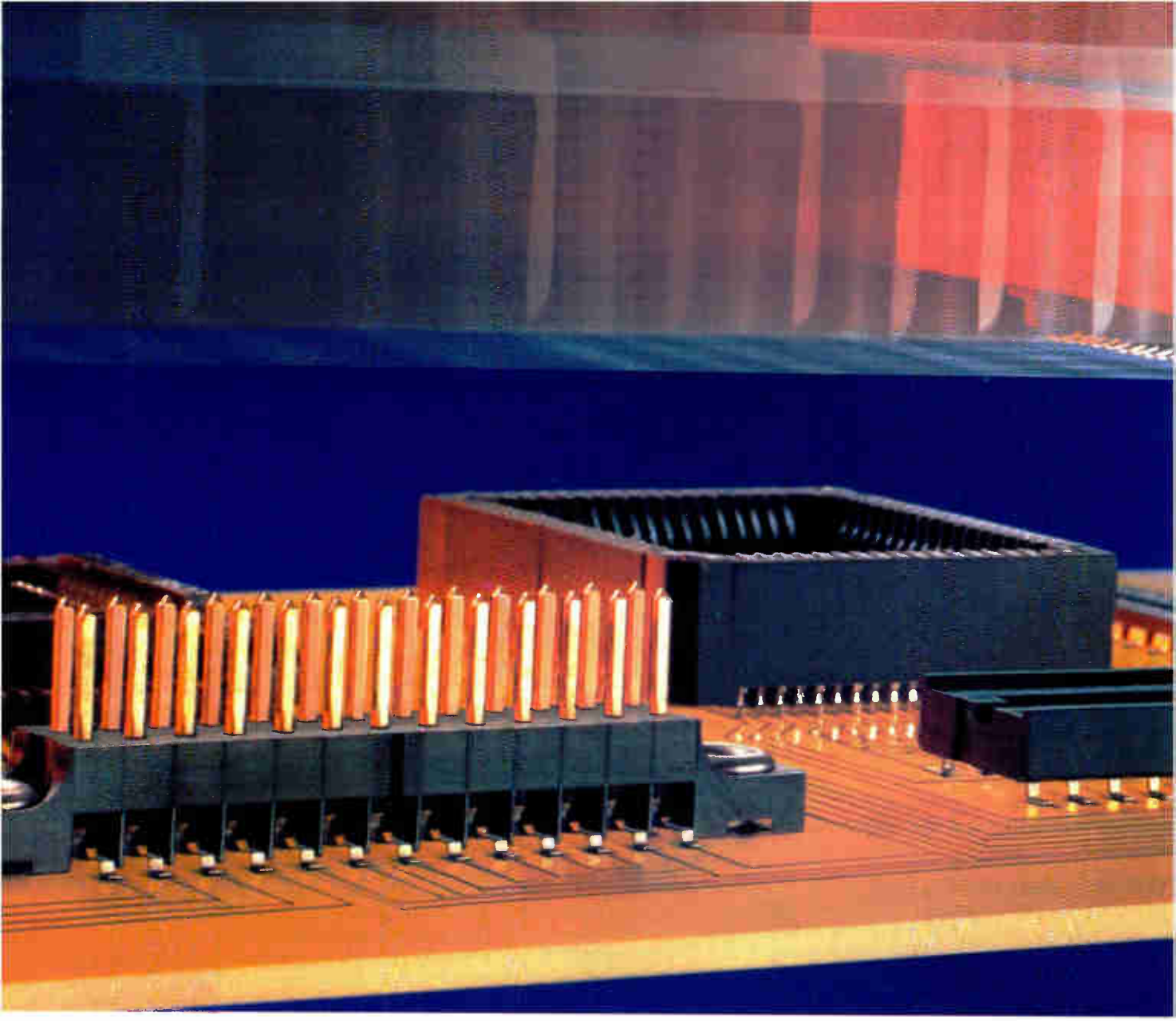


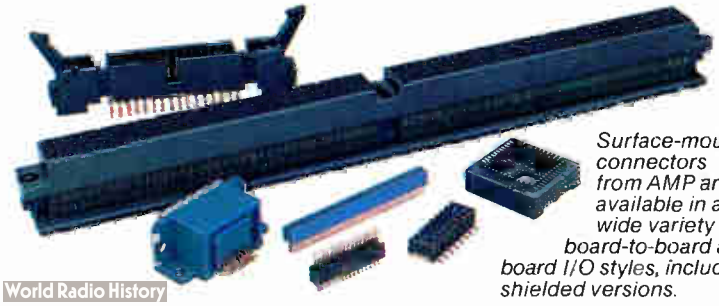
How AMP adds depth to

Technologies expand—and pay off—when they get in-depth support.

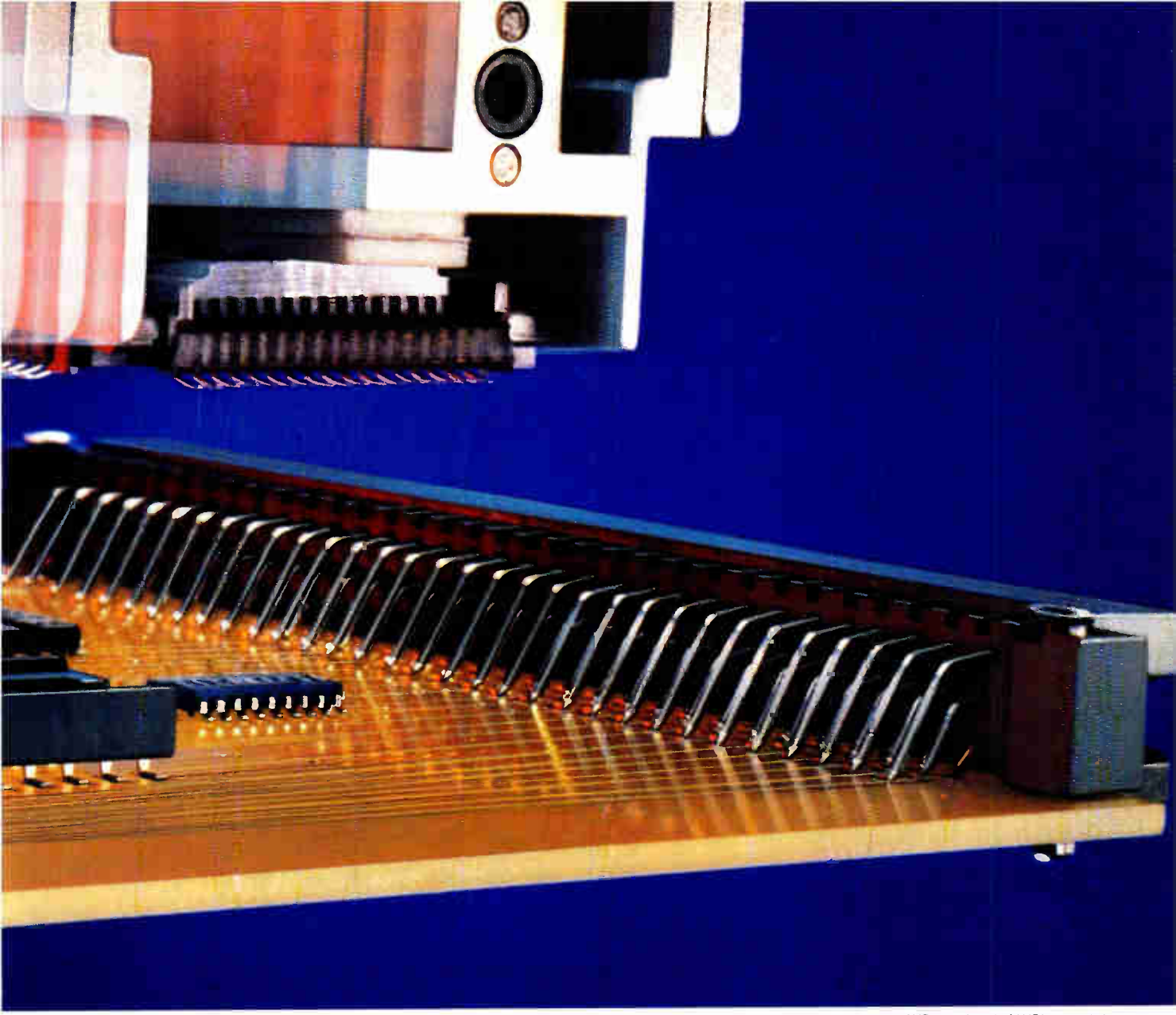
Many popular AMP connectors and sockets are already available in surface-mount styles. With more being developed every day. The depth? In the design, and in the usual for us—the technological backing to make a product both practical and affordable.

For instance, many of our surface-mount products are designed for flexible automation. Robotic systems offer fast production changeover via programming control. And we offer what you need to make it work: feeder and positioning equipment, and a variety of compatible packages, from tape and single tubes to stacking, multi-track trays.

All our SMT products are in tested materials, naturally—plastics and platings developed to withstand the process conditions of surface mounting. Because the technology is developing,



Surface-mount connectors from AMP are available in a wide variety of board-to-board and board I/O styles, including shielded versions.



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a surfacing technology.

some areas of product specification are still flexible. For example, solder leg design and specific platings are finalized in conjunction with the paste thickness you use, or time in reflow.

In fact, our "confidential early involvement" programs are a key measure of the support we offer. And especially important when the technology is itself new.

Chances are AMP can contribute a great deal. Dedicated staff and facilities for development of surface-mount products mean we're already involved in most industries where they're now being used, or considered.

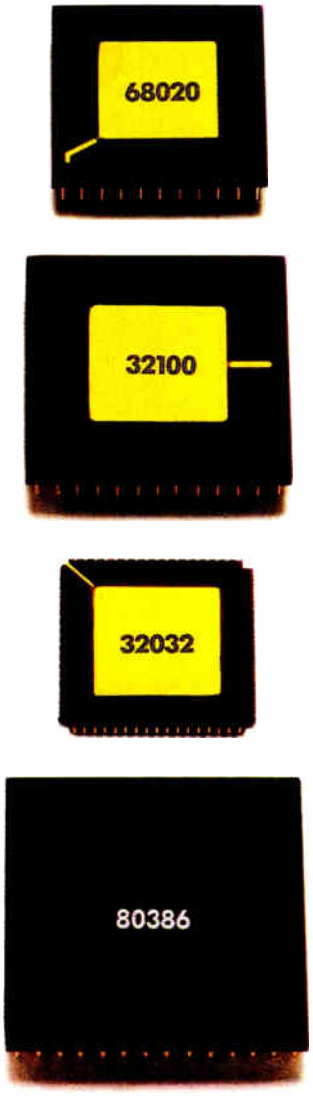
Write AMP Incorporated, Harrisburg, PA 17105-3608 and ask for our Surface Mount Products Guide and Robotic Application Tooling brochure. Or call (717) 780-4400 and ask for the SMT Information desk.

SMT products, advanced packaging, and feeder and positioning systems provide in-depth support for robotics-based flexible automation systems.

Circle 51 on reader service card

AMP **Interconnecting ideas**

State-of-the-past.



State-of-the-art.

CLIPPER™ from Fairchild. The most significant advance in microprocessors since microprocessors themselves.

Unlike the others, its performance isn't limited by an architecture designed back at the dawn of the microprocessor era. It's built from the ground up with a brand *new* architecture, for today's high-performance applications. And it's the only microprocessor that can bridge the architectural gap to true supercomputer performance.

CLIPPER. The new definition of state-of-the-art.

How the competition wishes they'd done it.

In a highly integrated three-chip set, you get an architecturally advanced, very high performance, CMOS 32-bit compute engine, optimized for scientific and professional computing applications in the UNIX® operating system environment. In fact, you get everything in the three CLIPPER chips that it takes the competition's entire CPU board to give you.

Designed for high bandwidth and true concurrent execution of instructions, CLIPPER runs at 33 MHz. Which, until we proved otherwise, was considered impossible. CLIPPER achieves a peak execution rate of 33 MIPS, with average performance greater than a VAX™ 8600 – twice as fast as any other microprocessor in existence, five *times* as fast as a VAX 11/780. And floating-point performance exceeds 2 MFLOPS, while simple instructions execute in a scant 30 ns.

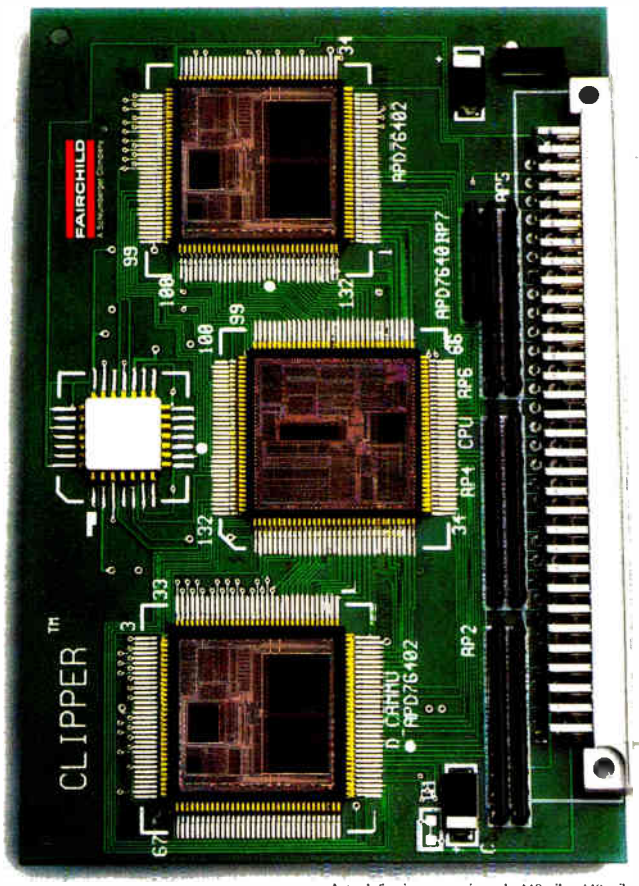
Supercomputer technology on a chip.

Unlike any other microprocessor architecture, CLIPPER uses proven supercomputer and mainframe architectural concepts.

Such as extensive pipelining. An on-chip floating point unit processing in parallel to a three-stage, pipelined integer execution unit. Two 32-bit buses, one for instructions, one for data, delivering up to 133M bytes per second to the CPU, eliminating bandwidth as a performance bottleneck.

Two large 4K-byte cache/memory management units (CAMMUs) provide mainframe-style, copyback caching concurrent with virtual address translation.

Then there's our Streamlined Instruction Set. With 101 instructions hardwired instead of microcoded for performance. There's also a macro-instruction unit, providing 67 high-level instructions and system functions. For all the advantages of RISC and the robustness of a CISC.



Actual die size approximately 440mil. x 440 mil.

What got into CLIPPER.

Residing on a 3.0 x 4.5-inch printed circuit card, the CLIPPER three-chip module includes a pipelined CPU with an on-chip, IEEE-standard FPU, and two 4K-byte cache/memory-management units. A clock generator completes the package, adding up to a staggering total of 846,000 transistors.

How CLIPPER backs you up.

CLIPPER is supported by a powerful software environment. Including a port based on the UNIX System V operating system. Optimized FORTRAN, C and Pascal compilers. Plus numerous utilities.

Or you can choose a complete VAX cross-support package.

And you're further supported by our application engineers and system designers. Each of them experts on CLIPPER.

For more information on the most advanced microprocessor since the advent of microprocessors themselves, just give us a call. You'll find us at The Fairchild Customer Information Center, 1-800-554-4443.

CLIPPER from Fairchild. All of a sudden, it's *the* state-of-the-art microprocessor on the market.

CLIPPER

We're taking the high ground.

FAIRCHILD

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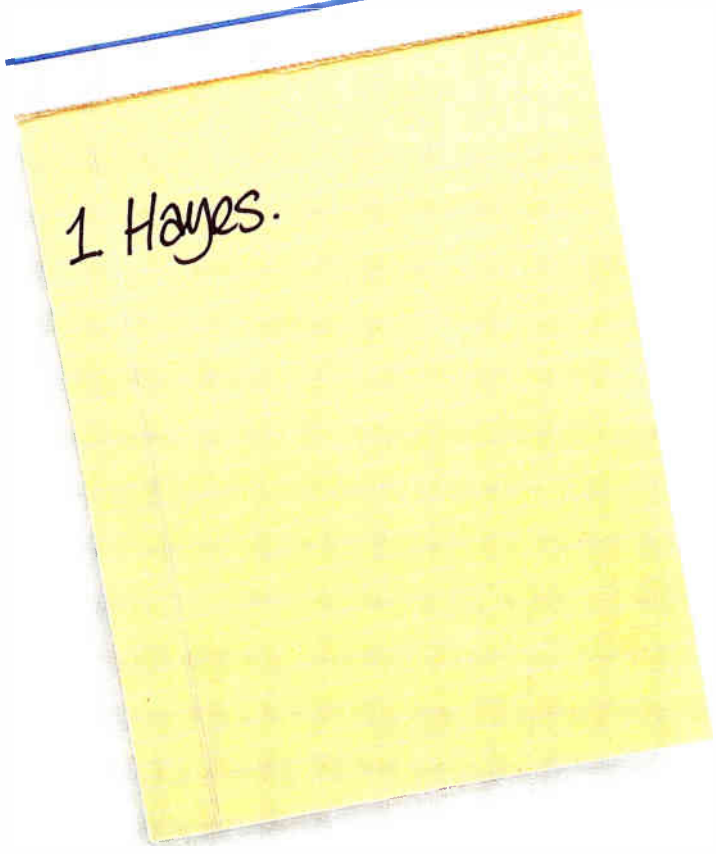
Circle 53 on reader service card

A complete list of things to know about 2400 bps modems.



Now that you've memorized that, here's a partial list of why a Hayes® Smartmodem 2400™ is best for you.

1. The Hayes Smartmodem 2400 allows you to communicate with the vast installed-base of 300,1200 and 2400 bps "Hayes-compatible" modems. The Hayes Standard "AT" Command Set allows you to use Smartcom II® and other software that communicates.

2. Through synchronous/asynchronous technologies, the Smartmodem 2400 permits your PC to access mainframes, minis, and on-line services previously inaccessible through asynchronous-only modems.

3. The Hayes Smartmodem 2400 is efficient...it pays for itself in just 4 hours of annual use over long distance.

4. The technology of the Smartmodem 2400 allows you to transfer volumes of files with confidence across the city or across the ocean using Bell and CCITT standards.

5. The new Smartmodem 2400B™—a plug-in board for the IBM PC and compatibles—allows synchronous and asynchronous communication through the same Com port.

6. You will also get the Hayes standard 2-year limited warranty and the opportunity to extend the warranty to 4 years.

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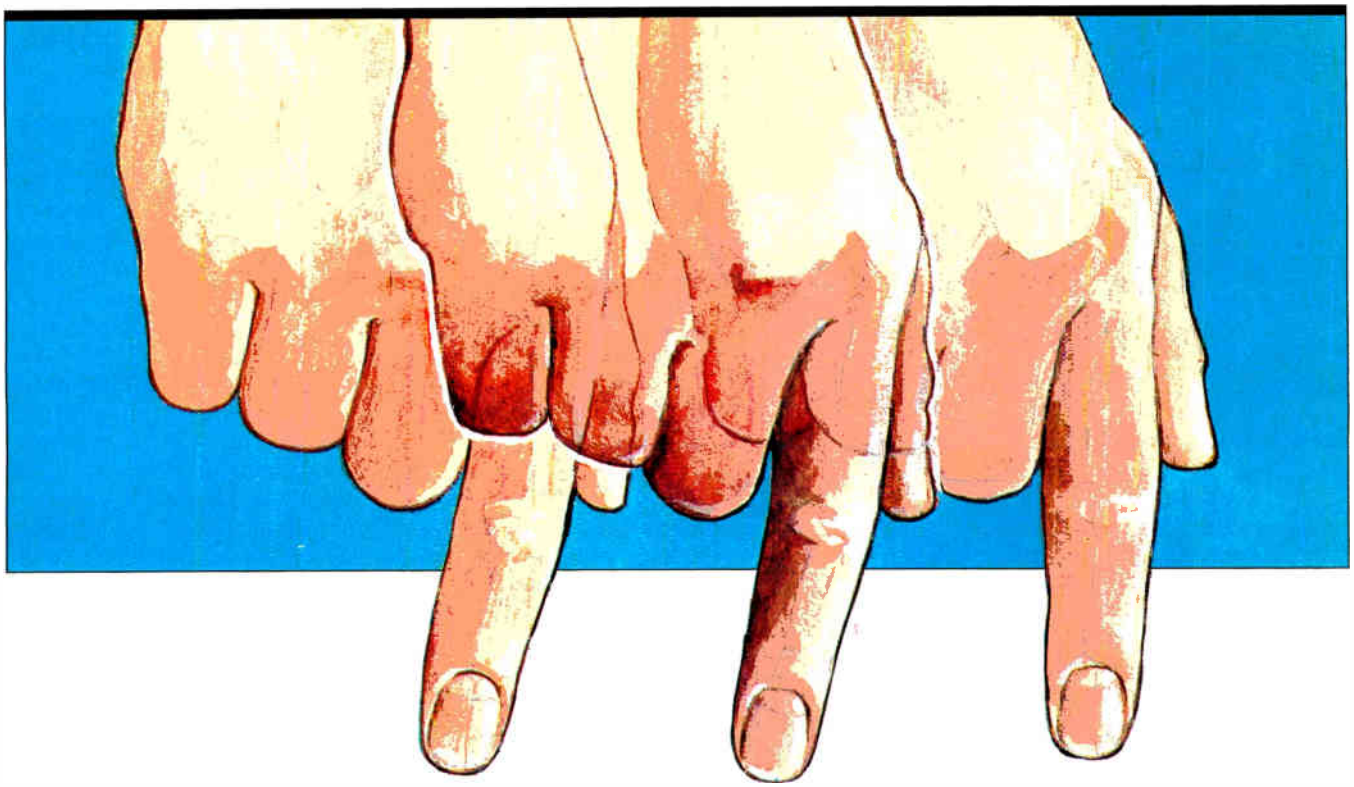
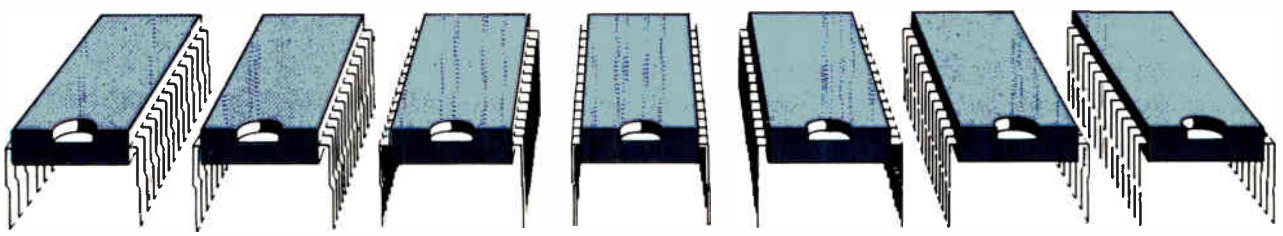
Circle 54 on reader service card

INSIDE TECHNOLOGY



ISDN CHIP SETS: USERS FACE A RISKY CHOICE



by Robert Rosenberg

Before integrated voice-data terminals can take over in the office from modems and analog telephones, terminal makers and system houses must make critical choices. They have to pick from a bewildering variety of chips—all billed as "standard"—available to implement the integrated services

HOW ISDN IS MOVING TOWARD IMPLEMENTATION	
1976	Common Channel Signaling No. 7 to handle signals across network (CCS 7) proposed First ISDN discussions at CCITT meeting
1981	First implementation of end-office digital switches
1983	ISDN standards committee begins work
1984	Basic and primary grades of ISDN service defined by CCITT First ISDN demonstration at International Switching Symposium
1985	Bellcore publishes basic- and primary-grade specifications Regional Bell operating companies express interest in ISDN field trials Bellcore requests proposals for ISDN hardware from terminal vendors
1986	Basic-grade access implemented by Illinois Bell, Pacific Northwest Bell, and Mountain Bell
1987	Nynex primary-grade access field trial Mountain Bell primary-grade demonstration ISDN demonstration of central-office switches from five vendors at International Switching Symposium
1988	Central office switching interconnection using CCS 7
1989	First implementation of interexchange (between different carriers) access
1990	First broadband ISDN implementation

digital network, or ISDN. The penalty for making the wrong choice is severe. Not only will designs be more difficult, but there is the risk of losing markets because of a late start. As Ronald R. Ruebusch, marketing manager of the Information Products Division at Advanced Micro Devices Inc. in Austin, Texas, points out: "The timing of a decision on when ... to have an ISDN product" is vital.

The threat of design complications looms large in the selection process, says Jim Garrett, telecommunications manager at Thomson Components-Mostek Corp. in Carrollton, Texas. One of the most important design considerations is "how easy it will be to interface these chip architectures back to their system buses," he says.

The whole selection process is further complicated by the fact that work on ISDN itself is far from finished. Although ISDN could be available for commercial use by the late 1980s (see chart, above), the International Telegraph and Telephone Consultative Committee, called CCITT for its initials in French, is still working on definitions of the standard interfaces and the signaling protocols that are needed to make the connection between a customer's equipment and the new network. Meanwhile, the chip makers are turning out parts that are needed for equipment within the customers' premises, with Intel Corp. the latest to introduce ISDN products (see p. 59).

All the current ISDN chip sets conform to whatever standards CCITT has set so far, on the network side. On the customer side, much of the CCITT's work is finished and the standards are set—but the rules leave ample room for variations. And there certainly are variations among the chips offered by the 10 or so companies selling their wares in the U. S. The differences among them occur chiefly in how the ISDN functions are partitioned on the chips.

Still to be heard from are the Japanese, who are expected to launch a major thrust into what is predicted to be the next big commodity market. By 1999, ISDN chips could be worth hundreds of millions of dollars for semiconductor manufacturers, says Ed Means, program director for telecommunications at SRI International in Menlo Park, Calif. The Japanese are not going to ignore a market that large, although they will probably wait for the differences to be sorted out before plunging in. With lower development costs to bear, they should drive down the chips' prices.

As things stand now, though, the price of ISDN chips is less important than the widespread differences among the circuits. Too much diversity is making potential purchasers reluctant to commit their system designs to one chip set or another.

The makers of private branch exchanges would appear to be the logical candidates to lead the way out of the ISDN maze. After all, the argument goes, they have plenty of telecommunications expertise and can readily evaluate the different chip offerings. But it turns out that PBX makers are reluctant—they fear rising costs for chips and a loss of revenues from their proprietary voice and data terminals, which more or less lock in their customer bases.

Typical is InteCom Inc. of Allen, Texas. "We are talking to the big players in the chip business who are spending big bucks, but right now our observation is that we are still a few years away from making any choice," says Ron Mills, director of hardware engineering. Mills says the new Wang laboratory unit has its own digital voice-data chip sets (which are not ISDN-compatible) and none of the proposed ISDN circuits is affordable yet.

AWAITING A STANDARD

John Wakerly, director of system architecture, David Systems, Inc.—a Sunnyvale, Calif., firm making a voice-data add-on to a PBX or Centrex system—says "as far as twisted-pair interfaces in the office, there will still be some shakeout. Our position at David is that when ISDN has a standard customer-premise interface, we will be compatible with it; but we are not taking the lead in that."

The prospect of lower revenues from the lucrative aftersale market is not to be dismissed lightly. That wouldn't have been the case five years ago, when PBX makers sold only switches. But the advent of digital voice-data gave them a rare opportunity: they could sell their own digital phone sets and office-automation software by

using proprietary interfaces and architectures. The PBX houses have since developed a tidy add-on business in proprietary equipment.

Deciding whether to surrender that steady income from proprietary equipment in order to adopt a standard ISDN architecture is only part of the broader quandary for the PBX people. They must also choose between a defensive or an offensive ISDN strategy, says AMD's Ruebusch. They can "take a defensive strategy by denying that ISDN exists, and claim that their proprietary approaches are as good as or better than the standard. Or they can adopt an offensive strategy by believing in their capability to produce switches at competitive costs, and in their software engineering organization to provide better features than the competition."

In the end, PBX vendors will adapt to ISDN. They won't have much choice; at some point, those who haven't adapted won't have a market. The issue is how quickly. Ruebusch suggests that those who don't take the offensive soon could find themselves behind foreign merchants.

DESIGN OR DEFER

Makers of end-user equipment with little telecom experience have a choice, too. They can select a chip set and begin the design themselves, or they can elect to use an interface developed by one of several telecom switch manufacturers that adhere to the ISDN rules. "The complexity of either solution is the same, and the risk is the same," says Russ Aldrich, manager of communications products and networking at Altos Computer Systems in San Jose, Calif.

Altos's dilemma is typical of the smaller systems house without in-house telecommunications expertise. Altos, which makes 8-, 16-, and 32-bit microcomputers, has already installed 70,000 systems worldwide. So it can either join an existing telecom company and design an interface specific to that company's product line, or throw in with a chip manufacturer and buy into an architectural approach.

Choosing to go it alone—the architectural approach—probably provides a much more flexible solution, Aldrich says, but the question remains, "What do you make with all these parts?"

For larger system houses with plenty of in-house communications expertise—companies like Convergent Technologies in San Jose, Calif., or NCR Comten Inc. in St. Paul, Minn.—the make-or-buy decision is less traumatic.

"We assume that the chip-set supplier will only have an impact on the interface board, not on the system," says Bobby Johnson, director of communications and networking at Convergent. Johnson is still researching and planning how ISDN chips will be folded into the Convergent product line, but he doesn't anticipate substantial modifications. "We could be wrong [about the ISDN]; but in the past, the choice of Ethernet did not affect our system architecture," Johnson explains.

Officials at NCR Comten say they are evaluating ISDN chips just like any other logic. "We face the same problem we've faced before," says Patrick Phillips, principal product manager in St. Paul. "We've had suppliers make changes in specific TTL that required a change in our product. Picking ISDN components should not be any more difficult."

One of the main advantages the larger system houses gain from their in-house expertise is the ability to make a functional comparison of the offerings and follow though with an evaluation of the partitioning of the functions. How the chips are partitioned illuminates how difficult it will be to implement the chip vendor's architectural approach.

The question of partitioning is probably the main sticking point for system houses, vendors of local area networks, and others planning to use ISDN circuits. Some chip vendors are ganging several protocol requirements on a single chip; others are dividing the requirements among several ICs. Also, users must evaluate the merits of the different local bus interface schemes being promoted by manufacturers. For example, several claim their particular interface

RUEBUSCH. AMD marketer says the choice is between defense, "denying that ISDN exists," and offense, believing in one's capability to produce competitive switches with better features.

bus simplifies connection requirements, though such benefits accrue only when using that same manufacturer's peripheral chips.

Chip vendors are approaching the functional partitioning differently. Some are shooting for higher levels of integration on a single chip. AT&T Technologies and Intel each have made one package out of their S interface (the point at which the user's equipment interfaces with the physical termination of the network) and their LAP D (for link access protocol) formatter (see figure, below). In Austin, Texas, Advanced Micro Devices Inc. goes further, including in its S interface a transceiver, an integrated codec and filters, and a LAP D formatter.

ALDRICH. Altos manager says the risk is the same whether the user designs a switch or decides to use one from a switch maker.

Other manufacturers say separating layer 1 transceiver functions and layer 2 data formatting is the way to go. West Germany's Siemens AG is distributing samples of its 2080 S interface transceiver and a separate layer 2 link access communication controller. Mitel Inc. in Kanata, Ont., Canada, which promises to have about 30 products supporting ISDN by the end of the month, has an HDLC protocol controller and will ship samples of an S interface in September.

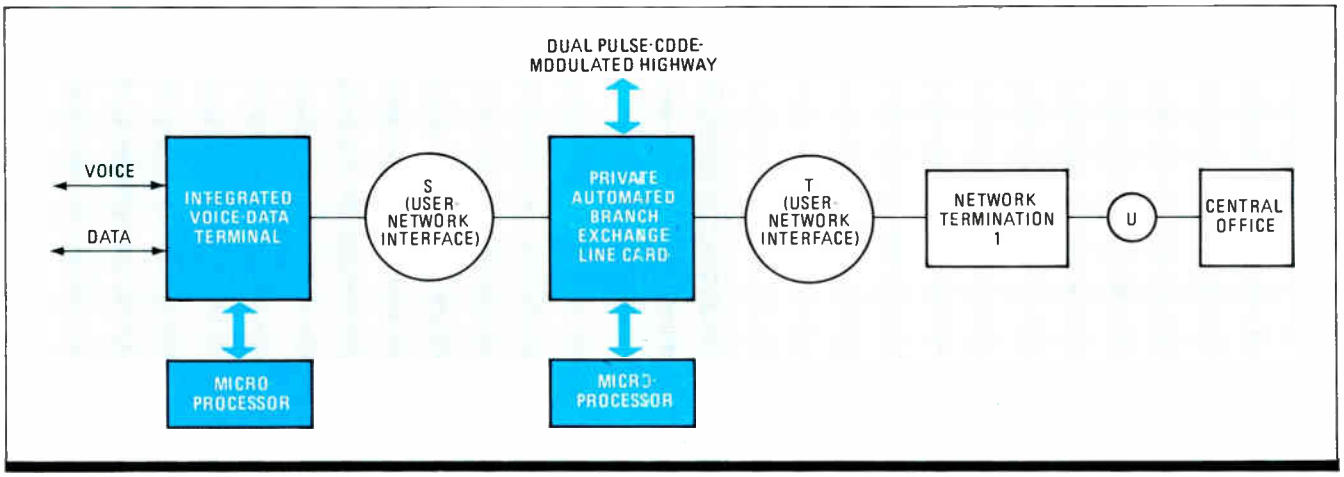
Thomson Components-Mostek will join its parent company—Thomson CSF of France—early next year in offering a level 1 S interface transceiver and a seperate level 2 interface with an integrated LAP D controller. National Semiconductor Corp. of Santa Clara, Calif., which offers an S interface, is taking the modular approach and separating layer 1 from the higher levels. Motorola Inc.'s Semiconductor Products Sector in Phoenix, Ariz., also plans to go modular; the thinking is that designers will have more flexibility at less cost with a variety of chips, rather than using one big, expensive chip for any given application.

Another area of confusion involves the local bus interface, where chip makers go off in a number of different directions. Intel's SLD (subscriber line device), Mitel's STbus, Motorola's IDL (interchip digital link), and Siemens's IOM (ISDN-oriented modular architecture) all have different interface schemes. "In many cases, the local bus interface has to have a set of associated peripheral chips to make a clean interface," says Lynn Ditty, the product marketing manager for communications devices at AT&T Technologies in Allentown, Pa.

One expense that ISDN chip users will avoid is the investment in software development. "In a microprocessor selection, you must buy into the software and instruction sets," says Ditty. But much of the software that will work with ISDN equipment is, in effect, already decided: it is being set by international standards.

Users deciding to develop a homegrown interface probably will not encounter insurmountable obstacles. "I don't think you can say the selection of one silicon implementation locks you into one vendor. You can actually interchange these things, although it will require extra glue logic," notes Al Mouton, Motorola's MOS telecommunications marketing manager. "That's not as bad as a microprocessor selection. With that decision, you had to invest in a lot of software. ISDN chips are simply a hardware interface." □

Also contributing to this report were Clifford Barney in San Mateo, John Gosch in Frankfurt, and J. Robert Lineback in Dallas



FINDING ITS PLACE. The S interface links the user's terminal and PBX, while the T interface joins at the network termination.

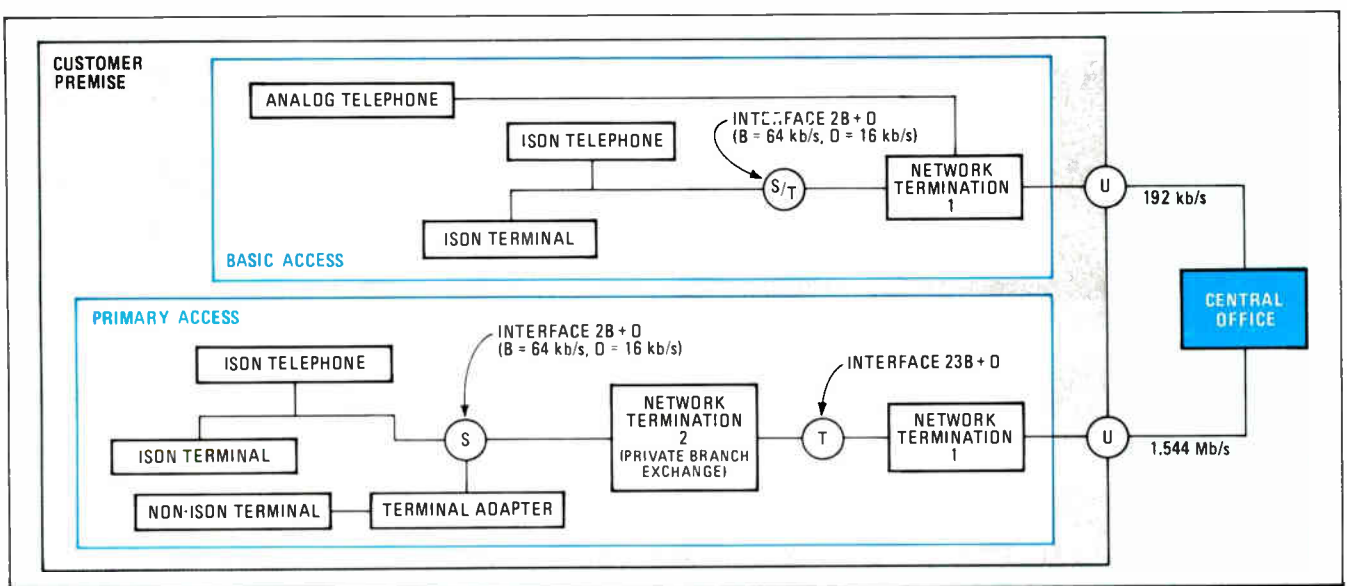
BULLISH ON ISDN, INTEL LAUNCHES ITS CHIP SET

An S interface IC, a line-card controller, and a codec-filter combo pave the way to the all-digital network, as well as easing the transition from the analog net

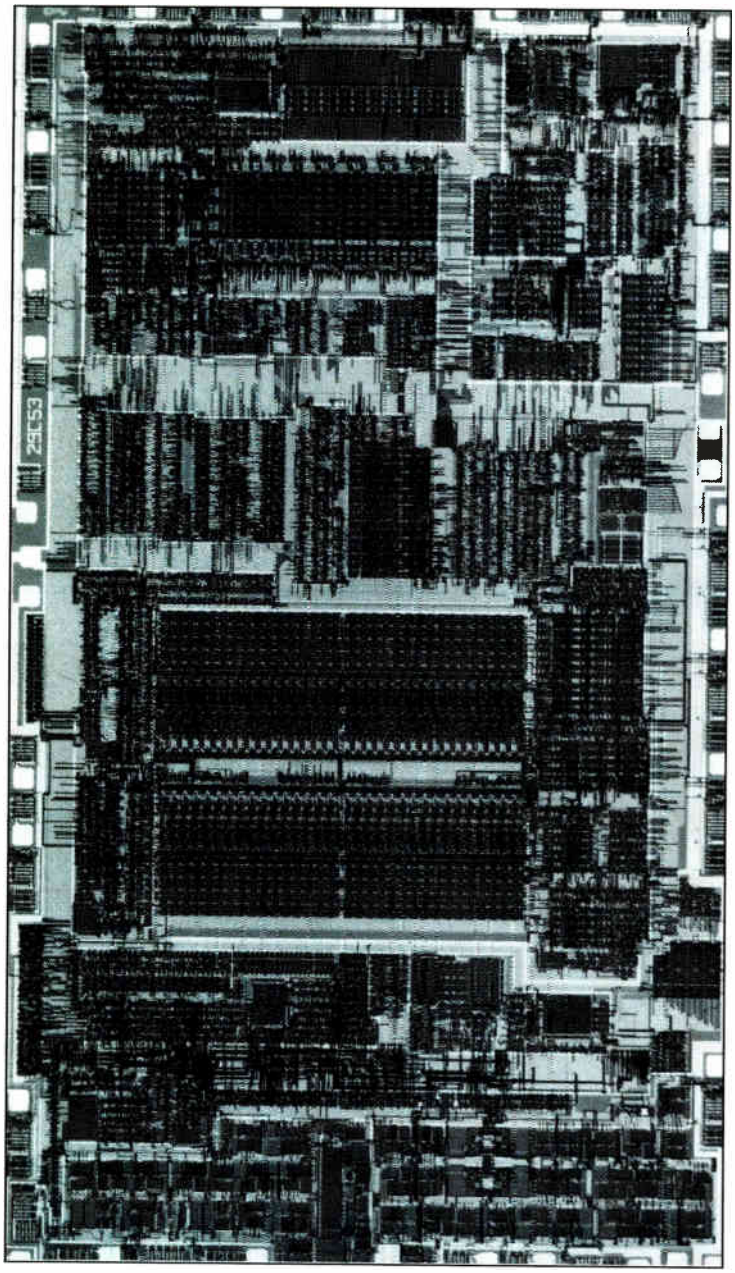
Intel Corp. is very bullish on the integrated services digital network, the all-digital scheme for replacing the worldwide analog telephone net. To compete in this embryonic market, the Santa Clara, Calif., IC maker is now moving into full production on its first chip set—and it expects sales of these sets to start showing up on its books next year. By then, standards for ISDN equipment to be used on customer premises should be solid enough for PBX and terminal vendors to begin designing that equipment, predicts Graham Alcott, telecom operations manager at Intel's Phoenix, Ariz., facility.

Intel is not the first with ISDN circuitry, of course. More than 10 other chip makers have already jumped into the market. But Intel believes that it has a big edge in its installed microprocessor base. And it is betting that terminal makers and others already using its microprocessors will adopt its approach to ISDN circuits—especially since Intel is making it simple to link the local microprocessor bus to its new ISDN interface circuits. It expects the first customers to be builders of ISDN voice-and-data terminals, telephones, and private branch exchanges.

Intel's first ISDN chips will be a basic-rate four-wire S interface transceiver, an input/output controller for PBX line cards, and a codec and



1. ISDN CALLING. Standards for the S interface—the link between the termination of ISDN and customers' equipment—are already set.



2. S INTERFACE. Intel's version of the four-wire S interface is the 29C53 digital loop controller. It meets the CCITT requirements for 144-kb/s basic-rate transmission.

filter combo. These new telecommunications chips, added to its microprocessors and local-area network circuits, will give the company a broad product line for the entire microcommunications market—a business that it intends to pursue aggressively (see p. 63). Intel is also working on a microcontroller that will link two of these pivotal product areas: local-area networks and ISDN.

This network conversion will not happen overnight, of course. Field tests of ISDN in the U. S. are underway, but full deployment will take years. Analog and digital technologies, as a result, will coexist for a decade or more. And Intel is designing its chips to provide a bridge between the old analog and the new digital services. "Our entire architecture is aimed at providing interfaces that can change from analog to ISDN with just an adjustment to a subscriber card; this should be wholly transparent to the user," Alcott says.

The new circuits are the latest products that Intel has developed in collaboration with the French chip maker Matra-Harris SA. The line-card controller is coming from Intel, while Matra-Harris is designing both the S interface and the codec and filter combo, working from Intel specifications. Both companies will produce and sell the chip sets.

The circuits represent a certain leap of faith on Intel's part. Strictly speaking, ISDN does not exist yet (see p. 55). Although the CCITT has already defined the grades of service that ISDN will provide and outlined how they will be implemented, many of the details are not yet settled. But Alcott says the industry knows enough about the specifications now to forge ahead. He points out that standards for the S interface—the connection between the physical termination of the network and equipment on the customers' premises—are already set (Fig. 1). "The S interface is clearly defined by the CCITT," he says. "Though there are spare bits in the specification that are reserved for as-yet-undefined applications, a few bytes of code could process whatever functions are required of those spare bits."

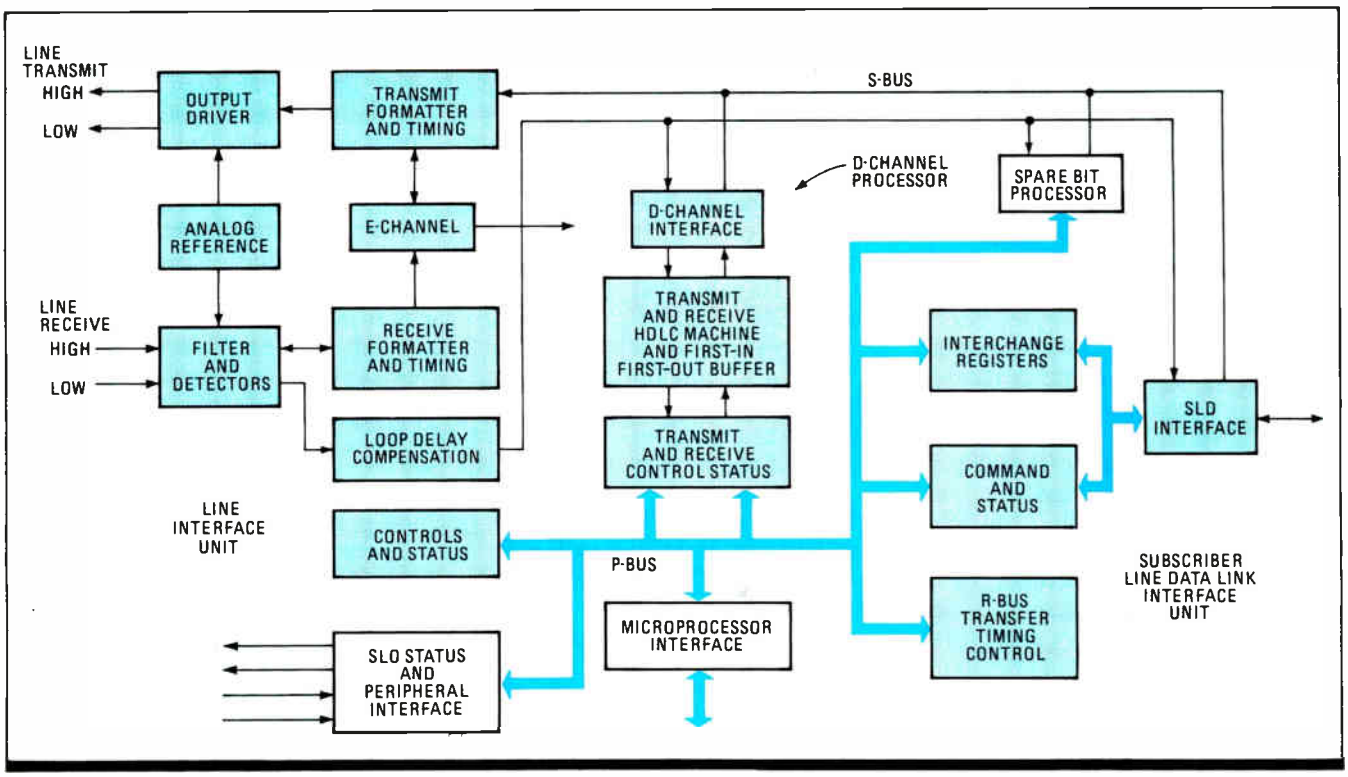
THE S INTERFACE

The 29C53 digital loop controller is Intel's basic-grade four-wire S interface transceiver (Fig. 2). Samples have been produced; full production is expected early next year. The chip meets the CCITT requirements for basic-grade service, which is established as 192 kb/s, divided into three channels. Two are 64-kb/s data- or voice-carrying channels, designated B channels. The third is a 16-kb/s signaling channel, designated the D channel. This allocation is commonly referred to as 2B+D and gives an effective channel capacity of 144 kb/s. The remaining 48 kb/s handles framing and other overhead signals.

Intel's chip provides all the internal drivers for transformer coupling to a standard twisted-pair telephone cable and establishes a data connection across a telephone link by implementing many lower-level HDLC protocols, or layer 2 of the International Organization for Standardization's Open Systems Interconnection model.

The chip provides four interface points. One is a subscriber-line data (SLD) link, which is based on the three-wire bus architecture that Harris Corp., Intel, Matra-Harris, Philips International NV, Siemens AG, and SGS Semiconductor Corp. support as the answer to serial transmissions on the line card. The second is a parallel peripheral interface; the third, a parallel microprocessor interface; and the fourth, a four-wire CCITT-compatible S interface.

These four interface points are controlled by



3. TWO BUSES. The 29C53 digital loop controller's line-interface, D-channel processor, and SLD functional elements are connected by a parallel bus (P-bus), which handles D-channel data, and a serial bus (S-bus), which transfers B-channel data.

three functional elements: the line-interface unit; the D-channel processor, or packetizer; and the SLD unit (Fig. 3). These elements connect through two buses. The parallel bus handles D-channel data, general status, and control information. The serial bus transfers B-channel data and the unprocessed D-channel data between the line-interface unit and SLD interface unit.

The SLD interface acts as a buffer during serial transfers, but its main job is to manage the 512-kb half-duplex communications link to other SLD devices. Half of the 256 kb/s in each direction is used by the two B channels. The other 128 kb/s handle D-channel packet data and control and status information. The D-channel processor performs some of the lower-level packet-formatting functions as specified by the OSI link-access protocol, version D. The line-interface unit contains the line drivers and receivers for the S interface. Line voltages are adjusted for the four-wire requirements. Formatting, timing, and synchronization are maintained across the four-wire loop.

"The requirements for the S interface came to us predefined by the CCITT, so this was an obvious necessity," says George Hayak, staff design engineer for the Intel team that developed the chips. "The SLD interface, on the other hand, is the most convenient way we have to link together devices with low bandwidth requirements. The parallel peripheral interface was needed to control the basic I/O functions. The parallel microprocessor interface works with any standard microprocessor or microcontroller."

The interface package gives the designer several options, Hayak says. PBX manufacturers, for example, must implement either local or centralized processing of D-channel (network-control) information. Those who want to upgrade older switch architectures can process D-channel information by linking the S interface to the line-card microprocessor. The processor can be programmed to take over link-level processing. In the newer switch architectures, which are designed with ISDN in mind, D-channel information processing is usually centralized; the SLD interface provides an easy way to route data for packet processing.

PEACEFUL COEXISTENCE

Both the 2952 line-card controller and the 29C48 codec and filter combo will help the chips' users coexist with both analog and digital lines. The 2952 is a special-purpose I/O controller; the 29C48 codec-filter links older, analog telephones and line cards to a digital PBX serving ISDN.

The 2952 controller chip, which is already in full production, controls the switching and control information passed between the individual devices and the backplane of the PBX, using the HDLC format. "On one side, it has provisions for up to eight SLD serial interfaces," Hayak says. "On the other, it is the interface to the TDM highway," the time-division-multiplexing scheme across the backplane of the PBX.

Of the various control functions it performs,

the 2952's primary job is managing the synchronous interface between the TDM signaling path of the host system and the subscriber interface. But it also manages the asynchronous signaling and control messages between a central D-channel control processor or the local line-card microprocessor, if one is used. "In a switch with centralized processing of D-channel information, the line-card controller handles its own processing. It need not call on the local microprocessor for processing D-channel information," Hayak says.

The 29C48 codec-filter combo provides the analog-to-digital and digital-to-analog transmit-and-receive functions needed to interface an analog telephone to the 64-kb/s pulse-code-modulated signaling scheme used in digital PBXs. Samples are available; the chip will be in full production early next year.

Functionally, the chip resides between the Borscht functions of the analog line card and the line-card controller circuitry of the digital PBX. Besides supporting traditional Borscht functions—battery feed, overvoltage correction, ring generation, supervision, codec, hybrid impedance balancing, and testing—the chip adds some new functions that help make analog sets work with ISDN. It has a secondary line-input channel, programmable gain adjustment, a custom hybrid balancing network selection, and either A- or μ-Law programming capability.

The secondary analog input channel can be used for remote-loop testing and control. The gain adjustment can be changed on the line card to accommodate differences in loop losses. Up to three external balancing networks can be applied to the chip to accommodate varying subscriber loop characteristics.

Besides the three ISDN interface chips, Intel says it will also be coming out with the 83C152, a microcontroller that will implement many of the protocols for ISDN B-channel communications—or, at any rate, the protocols Intel is anticipating the CCITT will select. The chip also will feature several popular LAN protocols. Samples are available now, but the company is tight-lipped about an introduction date, saying only that it will be "a 1987 product." The chip probably will be offered as the heart of a communications board for personal computers that will handle both local and long-haul communications chores.

The serial microcontroller operates in either full- or half-duplex modes and has automatic frame-check sequence generation to ensure error-free transmissions. It supports a variety of protocols, including synchronous data-link control and carrier-sense multiple-access/collision-detection protocols, the 1-Mb/s Starlan, and subsets of the HDLC. The company says it will also operate on user-definable protocols.

With its three chips and the controller, Intel is preparing the ground for ISDN's arrival. They add the features and signaling intelligence needed to give ISDN capability to terminals and telephones, so that users can take advantage of the coming all-digital network. □

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HELLO, PARIS? THIS IS PHOENIX CALLING

International collaboration—which is the essence of ISDN—played a big part in the design of the new S interface circuit being introducted by Intel Corp. The cooperation needed to set standards for an all-digital telephone network by the member countries of the CCITT found a counterpart in the joint chip-development efforts undertaken by Intel Corp., Phoenix, Ariz., and Matra-Harris at the Cimatel facility the two companies own near St. Quentin en Yvelines in the suburbs of Paris.

Ironically, though, the international team bent on creating the new communications circuit found it had to contend with some very old communications links. Intel's 28-year-old communications circuit designer, George Hayak, says, "From our end, we had to rely on the standard communications of today. We could depend on a traditional telephone conversation for some of our communications, but the computer links we had between here and there were very primitive."

To augment the low bandwidth links available for communications, Intel engineers moved computer tapes and prototype chips between the French and American facilities. "We were like carrier pigeons carrying tapes and chips," recalls Hayak.

COLLABORATORS. Martin Mueller (l.) and George Hayak had to use some old communications technology as they worked on new ISDN chips.

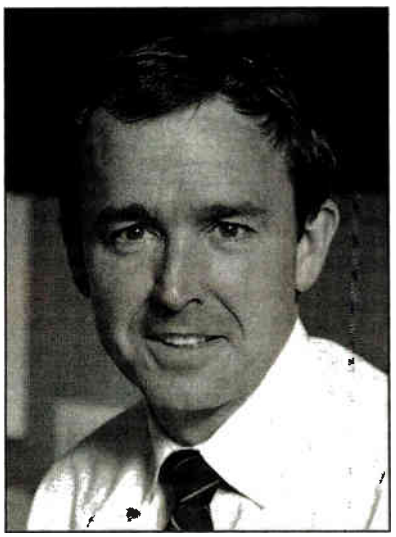
"We tried to make those exchanges every two months," says Martin Mueller, head of the telecom-circuits group at the Cimatel facility, but he admits that the arrangement was less than ideal. "Sometimes we suffered from the difficulty of the information exchange."

Cimatel is installing a Digital Equiment Corp. DECnet local-area network, Mueller says, which will give the French facility compatibility with Intel's internal network. Low-data-rate communications over the international network will be easier once the installation is complete, but true high-bandwidth data exchange will have to wait for completion of ISDN; Mueller says it could be five years away.

INTEL AIMS AT MICROCOMMUNICATIONS

Adding telecommunications chips to its product line puts Intel Corp. in position for a broad assault on the entire communications market. With its strong microprocessor line and wide array of local-area network chips bolstered by the new telecom circuits (see p. 59), Intel now figures it has what it needs to be a complete supplier of everything from components to complete networks—a broad area that it calls microcommunications: microchip-based digital-communications products.

"By 1990, suppliers will not be able to market a microcomputer without an integrated communications function," says Ron Whittier, Intel's vice president of marketing. He estimates the total communications market at $1.3 billion in 1989, 80% of it in data communications over small, local, and global networks and the rest in telecommunications.



WHITTIER: "Any place you put in a computer, there is a need for a communications system," says Intel marketer.

Intel wants to participate in that market by providing communications capabilities for the installed base of personal computers, which it estimates now stands at some 16 million units. Its next step will be to use that know-how to build entire systems linked by Intel-supplied buses, telecom products, and networks. In fact, Intel has already started acquiring the communications experience it will need.

Its microprocessors and LAN chips are at the heart of a system it has sold to the Army Electronics Command at Fort Huachuca, Ariz. The system consists of an Intel 310 microcomputer, based on the 80286 microprocessor, acting as file server for some 1,200 nodes. It uses Open Systems Interconnection communications with Intel Ethernet chips and proprietary software developed by Intel, IBM Corp., and Microsoft Corp. for the upper communications level.

Personal computers and peripherals on a local area network can be connected to an IBM or IBM-compatible mainframe via an Intel product called Fast Path, which provides up to six connections into the 3-megabyte/s IBM input/output channel. Fast Path replaces the 3270 emulation mode, which operates at 56 Kb/s, and also makes possible linkups with minicomputer hosts.

Besides working on total communications systems, Intel is taking an active role in LAN markets. It has acquired token bus products for use in Manufacturing Automation Protocol networks, through a technology exchange agreement with Industrial Networking Inc. of Santa Clara, Calif., itself an affiliate of LAN-vendor Ungermann-Bass Inc. Under the terms of the agreement, Intel will be able to sell Industrial Networking's token bus chip set and board; Industrial Networking gets the rights to market an Intel Multibus board that uses the chip set.

At this point, Whittier says, most MAP sales are at the board and system level, as users evaluate products. "People aren't designing in components at this point," he adds. "They want a next-generation chip—which will come along at the end of next year."

Intel already has products supporting the networks Ethernet and Starlan. "We'll also support [the IEEE 802.4] token ring," Whittier says, although he declines to give details. In addition, Intel offers a low-speed serial architecture called Bitbus for tying together components in a factory-automation system.

The Integrated Services Digital Network chips introduced this month provide the telecommunications component necessary for Intel's overall communications strategy. They support wide-area networks at the component level.

The entire array leaves Intel with a mix of products that are standard where standard protocols exist, such as in ISDN and 802.3, and proprietary where standard protocols have yet to be developed, such as in the upper OSI layers and on the factory floor. In the standardized markets, for instance, Intel's Open Net must compete with Xerox Corp.'s XNS and Sun Microsystems Inc.'s Network File System. Among proprietary systems, Bitbus occupies ground challenged by several other systems and by the carrier band extension to the 802.4 token bus protocol.

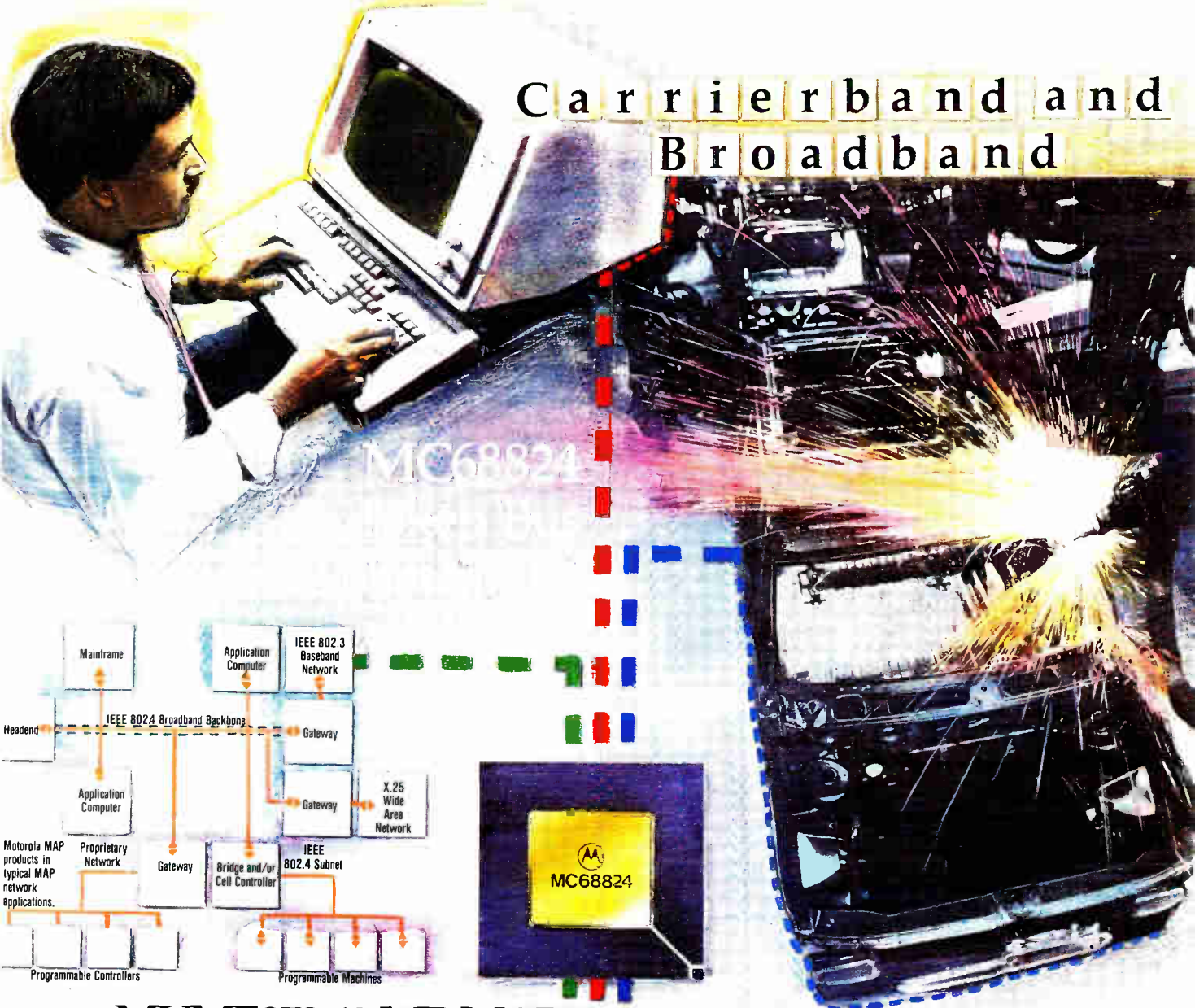
The market by 1989 will be $1.3 billion, and 'by 1990, suppliers will not be able to market a microcomputer without an integrated communications function'

Nevertheless, Whittier emphasizes that Intel intends to mount an attack in the market any place it can. "Any place you put in a computer, there is a need for a communications system," he says.

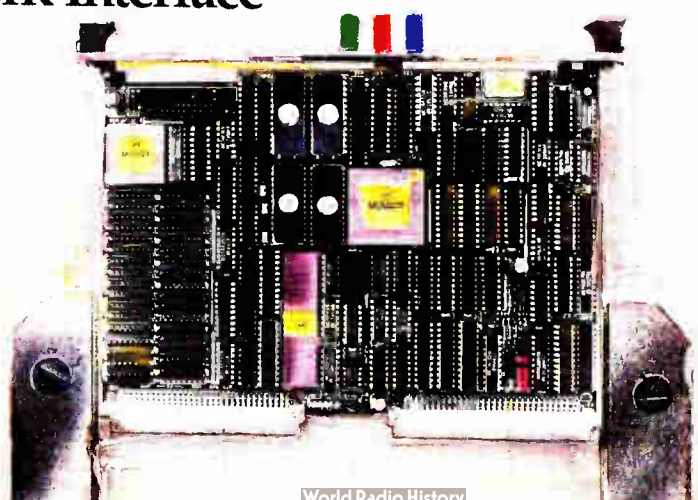
–Clifford Barney

MOTOROLA

Carrierband and Broadband



MVME372 10 MB MAP Network Interface



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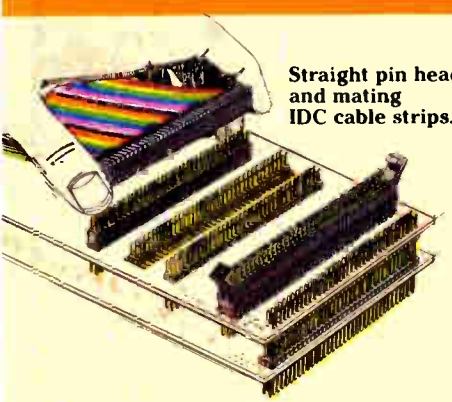
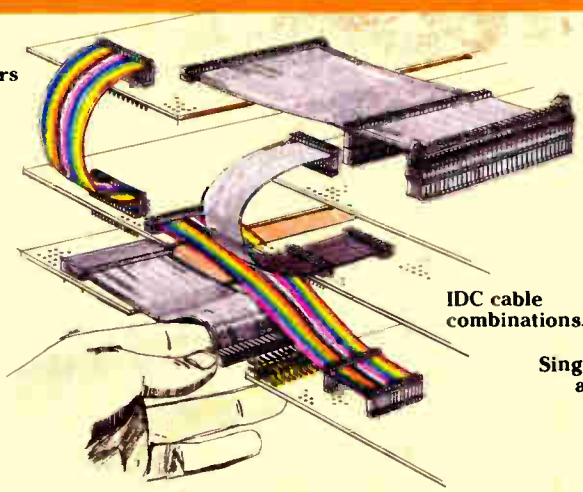
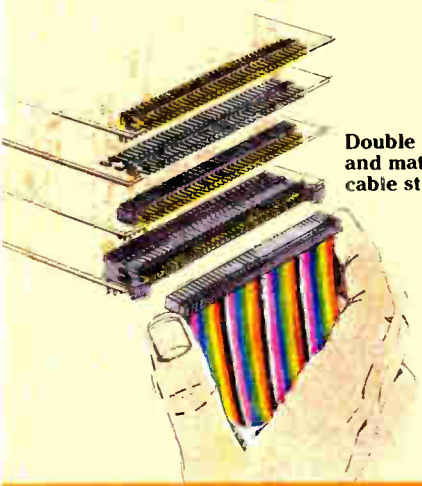


Straight pin headers and mating IDC cable strips.

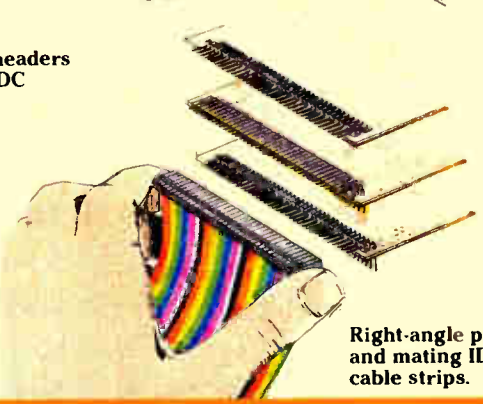


IDC cable combinations.

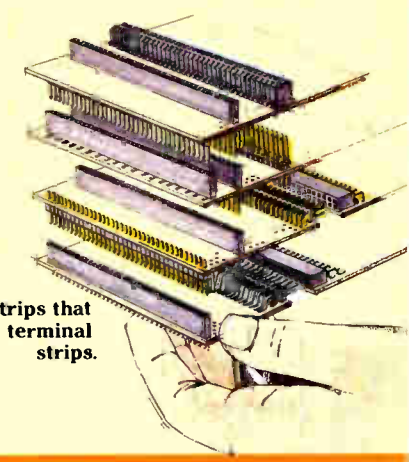
Single row headers and mating IDC cable strips.



Double row headers and mating IDC cable strips.



Right-angle pin headers and mating IDC cable strips.



Socket strips that mate with terminal strips.

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A BIPOLAR GATE ARRAY THAT RUNS FAST ON LOW POWER

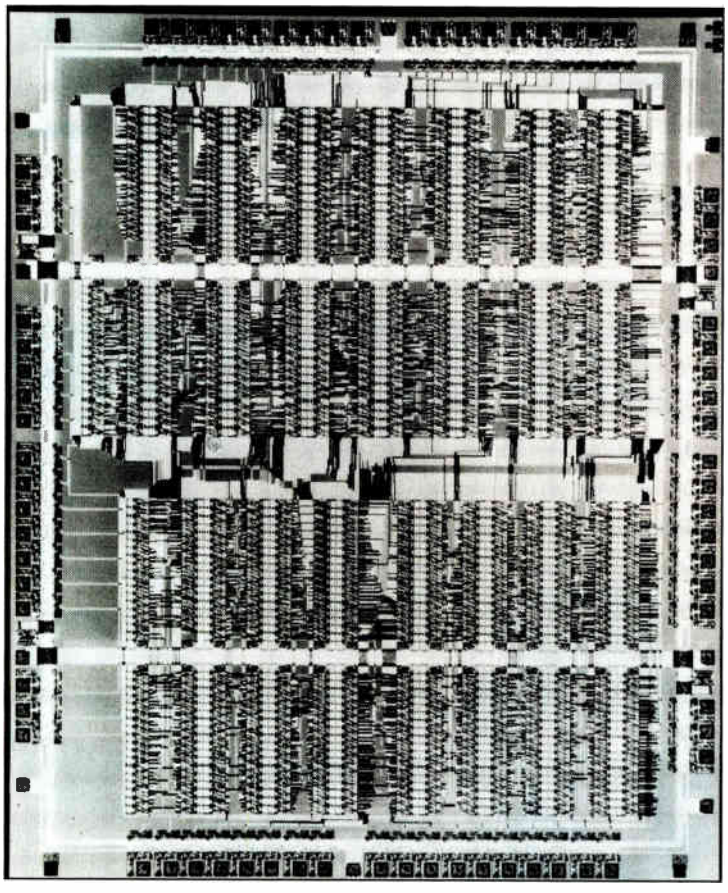
Ferranti puts a new twist on an old process to yield gate arrays with 1-ns gate delays and 100-MHz system speeds—with power dissipation ratings that rival CMOS

The combination of a workhorse bipolar technology and a logic scheme called differential logic is spawning a new generation of Ferranti Electronics Ltd. high-density gate arrays that run at speeds competitive with the fastest bipolar VLSI circuits. What's more, the combination of collector-diffusion isolation and differential logic yields devices that achieve power dissipation ratings in the CMOS class.

Capable of gate delays in the 1-ns range, clock frequencies up to 250 MHz, and system speeds as high as 100 MHz, the British company's new FAB3 devices are able to achieve power dissipation ratings ranging between 55 and 750 μW. In addition, this third-generation, 1.5-μm version of Ferranti's decade-old collector-diffused-isolation (CDI) process requires only six to eight masking steps, compared with the 12 to 15 steps required for competitive bipolar and CMOS VLSI processes.

Differential logic involves steering current through a logic tree by means of differential pairs of transistors stacked across the supply rail. This stacking technique achieves flip-flop delays that are only marginally greater than a single gate delay. Used in Ferranti's new DS series of ULAs, the CDI/differential logic combination has yielded chip densities as high as 10,000 gates (Fig. 1). David L. Grundy, technical director at Ferranti's Microelectronics Center, Hollinwood, Oldham, England, predicts that future versions of the technology will lead to arrays with densities up to 100,000 gates.

The CDI process starts in the same way as the standard bipolar TTL, ECL, or CML processes by diffusing low-resistivity collector regions into a p-type substrate. The CDI process diverges by laying down p-type epitaxy, to serve as both the isolation and base regions. Two n-type diffusions are then laid: a deep diffusion in a rectangular frame that encloses a p-type base region, followed by a shallow diffusion into the base. The deep diffusion connects the surface to the buried collector, and the shallow one forms the emitter. The transistor structure thus formed (Fig. 2) is surrounded by the p-type epitaxy and is isolated from adjacent components.



1. 10,000 GATES. To achieve 10,000-gate density, Ferranti combines differential logic with collector diffused isolation.

Jeffrey A. Bruchez, manager of microcircuit development for Ferranti, points out that CDI allows the fabrication of multiple-emitter structures that can operate efficiently in the inverse mode. CDI is still an epitaxial process, but, unlike most other bipolar processes, it does not involve an n-type epitaxial layer on the surface of the p-type substrate. Instead, a p-type epitaxial layer is laid down, which will constitute the final transistor base regions, with an n+ diffusion into this epitaxial layer finally forming the collector and isolation regions.

The collector is a heavily doped n-type region, unlike the lightly doped collectors of TTL fabrication, which provide good inverse-mode transistor operation necessary for the current sources, but at the expense of diffusion times of electrons across the base region. The CDI process uses thin epitaxial layers—typically 2 μm—and shallow diffusion depths, typically 1 μm, yielding a very narrow base width and a good operating speed.

Bruchez notes that the basic CDI process has a topography well suited to optical lithography, even when device geometries are scaled down to the submicron level. Unlike a typical CMOS VLSI structure, he says, CDI requires no plasma etching or low-pressure chemical vapor deposition, does not involve implantation or complex metallization procedures, and uses standard projection lithography. All process stages are conventional bulk-silicon techniques, with a flat surface topography at all stages.

The basic process requires only five masking operations, with multilayer metallization adding two further masks. A selective p+ mask may also be used if high voltage or minimization of edge capacitance is required. Submicron versions of the process use self-alignment techniques to increase packing density without sacrificing this simplicity.

HOW DIFFERENTIAL LOGIC HELPS

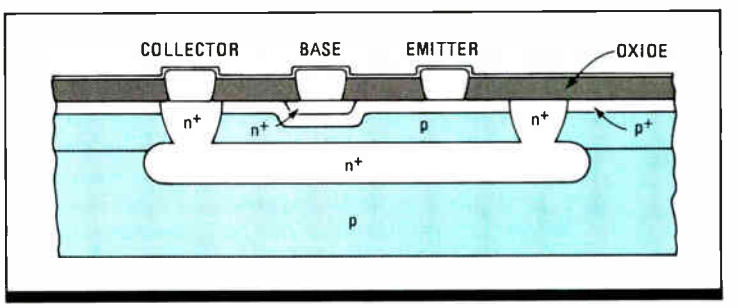
To take full advantage of the CDI process, says Grundy, Ferranti designers developed a differential logic technique that allows vast improvement in the power-delay product by ensuring that system power levels are kept to a minimum, achieving a twofold to fourfold increase in speed. Another advantage is that the flip-flop clock-to-output delay is less than two equivalent gate delays. Many complex logic functions can be implemented with the technique.

Differential logic is unique in bipolar technology. Unlike ECL, it eliminates the need to generate and distribute accurate temperature-compensated voltage references. Its inherent common-mode rejection removes problems associated with noise, crosstalk, supply-voltage distribution drops, and variations in temperature. In addition, differential pairs also have an extremely linear and sharp transfer characteristic, enabling the differential gates to operate with logic swings as low as 100 mV while retaining the same discrimination between logic levels as do single-ended circuits, which have logic swings of 400 mV or greater. Since power dissipation is directly proportional to logic swing, a 75% power savings is achieved with no compromise in speed.

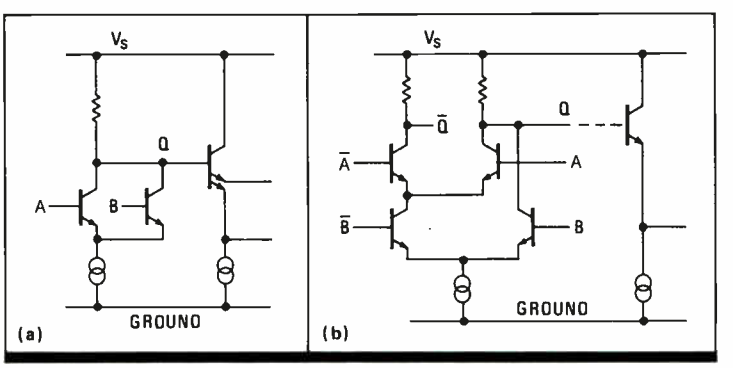
A conventional single-ended emitter-coupled-logic or current-mode-logic gate with an added emitter-follower buffered output (Fig. 3a) has the advantage of operating as a nonsaturating gate at a reduced supply voltage and logic swing, and the added benefit of a wire OR facility. A differential logic gate (Fig. 3b), on the other hand, is based on long-tailed pairs of transistors. The advantage of a long-tailed pair is that it has a linear transfer characteristic that does not soften near signal extremes, so it can operate within the common-mode range without problems associated with supply voltage, power distribution drops, temperature variations, noise, and crosstalk. Good radiation hardness is an additional benefit.

Maximizing these advantages enables differential gates to operate with logic swings as low as 100 mV, half that of conventional single-ended gates. Comparison with high-speed ECL gate structures of similar circuit complexity shows that not only is the logic swing significantly reduced—by almost an order of magnitude—but also the need for voltage-reference distribution around the chip is eliminated.

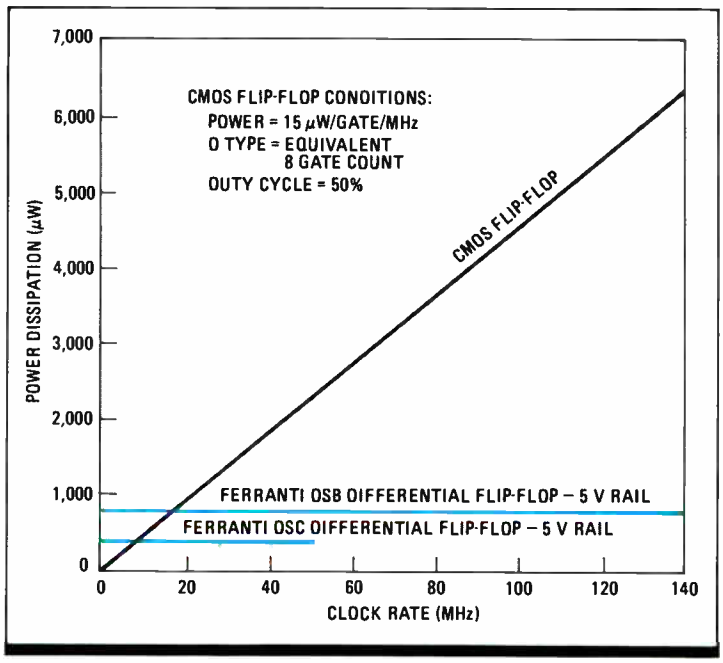
The long-tailed transistor pairs are stacked in order to implement flip-flop and complex logic functions. Up to four levels can be accommodated with a supply voltage of 5 V. The combination of reduced logic swings and increased functional



2. DEEP AND SHALLOW. Ferranti builds CDI devices with a deep diffusion to the buried collector and a shallow one to form the emitter.



3. TWO APPROACHES. Unlike the single-ended ECL gate (a), differential logic gate (b) uses long-tailed pairs of transistors.



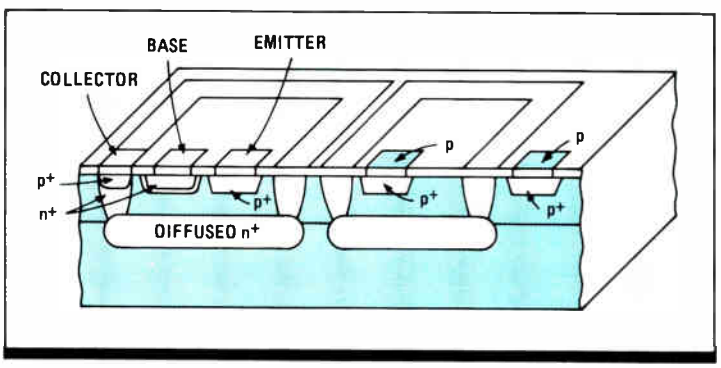
4. LOW POWER. Unlike CMOS, bipolar differential logic flip-flop shows no increase in power dissipation at higher clock rates.

complexity has resulted in significant improvements in power-delay performance compared with single-ended logic gates. Since the gates have complementary outputs, the need for inverters has been removed, resulting in gate savings of about 15%.

10,000-GATE ARRAYS

Ferranti has combined the new differential logic technique with FAB3 to achieve densities of 10,000 gates and system speeds up to 100 MHz in the new DS series of uncommitted logic arrays, marketed by Ferranti Interdesign Inc., Scotts Valley, Calif. A scaled-down, 1.5-μm version of the original CDI process, FAB3 also features double-layer-metal interconnect with a 6-μm grid pitch on both layers.

Several characteristics of the DS series contribute to the high system speed, says Grundy. Among them are flip-flop toggle rates approaching 250 MHz, and gate propagation delays in the 200- to 500-ps range, which are maintained virtually independent of increased fanout. Using differential logic techniques, circuits fabricated with FAB3 compare well to equivalent CMOS functions, both in terms of power dissipation and clock rate (Fig. 4).



5. GOING DOWN. Ferranti is refining a self-aligned, collector-diffused oxide-isolated process to scale down CDI.

For example, a D-type flip-flop implemented in one array type, the DSA series, is capable of a clock-to-output delay of 1.5 ns and a 250-MHz toggle rate. Power dissipation at this frequency is 750 μW at 5 V and 300 μW at 2 V, with no loss of speed. In the 140-MHz DSB series, clock-to-output delay is 2.7 ns, with power dissipation ratings of 380 μW at 5 V and 152 μW at 2 V. With the 50-MHz DSC series, clock-to-output delays are no more than 7.5 ns, with power dissipation of 137 μW at 5 V and 55 μW at 3 V.

This performance under high load conditions is further enhanced by the clock driver gate, which directly drives the high fan-outs experienced on clock lines, while avoiding partitioning into tree structures and the associated clock skew problems. The effect of loading within I/O buffers is also minimized.

Differential logic also accounts for two other significant advantages involving the two-level D-type flip-flops used in the DS series. First, only two current sources are required to support the basic master-slave flip-flop function, compared with six for a D-type flip-flop based on conventional gates. Second, the propagation delay from the active clock edge to both outputs is only marginally greater than for a single gate, compared with a delay equivalent to two or three gates for conventional D-types.

The use of differential logic also eliminates the need for inverters by automatically providing the true and inverse of every input and output. So an AND gate can become an OR, NOR, or NAND simply by changing the order in which the connections are made. Not only does the removal of inverters enable an increase in overall system speed for a given gate delay, it also yields a gate savings of about 15%.

Each ULA in the DS series contains high-performance I/O cells designed to allow the integration of special digital and linear functions for versatility in interfacing. Each cell has a 48-mA high-output drive capability.

Impressive as it is in the fabrication of gate arrays, the multilevel differential-logic/CDI combination is at its best when applied to high-speed regular architectures—such as systolic arrays—on a full-custom basis. For example, integrating the Winograd Fourier transform algorithm using a bit-level systolic array architecture with three-level differential logic yields a chip area savings of more than 50% and a sixfold power-delay improvement compared with the same implementation in a conventional 5,000-gate CML/ECL-based design.

Using the current 1.5-μm FAB3 process, Ferranti has fabricated a 16-bit multiplier with a multiply time of 25 ns and a power dissipation of

1 W, in which the full adder function was implemented in four-level differential logic using a single current source, and in which the fast path is selectively powered up. Using conventional CML/ECL-based circuit techniques, a worst-case gate delay of 200 ps would have been required; using four-level differential logic gave an eightfold power-delay advantage.

THE NEXT STEP

To achieve circuit densities of 100,000 logic gates per square centimeter in gate-array form using optical lithography will require submicron feature sizes with alignment tolerances of 0.25 μm or better, depending on the process layer characteristics, says Bruchez. He also says it will be necessary to have a multilevel metallization system with a 3-μm grid pitch (2μm track, 1μm gap), with all process conditions scaled to suit this pitch (Fig. 5). To achieve this within the CDI structure, two further degrees of self-alignment are introduced into the process at the 1.0-μm and 0.8-μm levels.

In the 1.0-μm process, all contacts and emitters are self-aligned using a photoresist barrier technique in conjunction with implantation, thus removing key alignment tolerances without further masking operations. At the 0.8-μm level and beyond, the base region is implanted through the self-aligned contacts, thus achieving a selective base structure, with attendant voltage and capacitance benefits—again, without the need for an additional mask. Bruchez reports that the performance characteristics of CDI transistors have been studied down to the submicron level, where they exhibit extremely good gain and can hold it over four decades of current, down to the nanoampere level.

"As geometries are scaled toward the submicron level, minimum transistor sizes are compromised by parasitic effects and the intrinsic component speed requirements," says Grundy. "Significantly, the interconnection requirements pose fundamental limitations, not only on component size, but also on system speed and packing density."

To address this problem, Ferranti designers have decided to use an oxide-isolated structure for the next-generation 1.0- and 0.8-μm processes. Their approach will bypass many of the disadvantages of current oxide-isolation schemes, such as increased process complexities, surface irregularities, defect generation, lateral encroachments, and disturbance of vertical bipolar structure. The oxide-isolated structure requires only six basic masking steps. □

THEY KEPT IT SIMPLE, AND THEY FOUND 'A WINNER'

With FAB3, the current third-generation 1.5-μm version of the CDI process, Jeffrey A. Bruchez and David L. Grundy believe they have hit it big, moving into the mainstream with a viable bipolar VLSI process. "In terms of process simplicity, we are where many other bipolar and CMOS vendors started many years ago—and now find they must return to in order to produce VLSI circuits that are reliable, cost-effective, and fast," says Grundy, who is technical director of the company's Microelectronics Center at Hollinwood, Oldham, England. "Where other processes with each succeeding generation have become more and more complex, requiring additional processing steps, we have managed to keep it simple with CDI."

Grundy believes that FAB3, which combines CDI with the company's differential logic circuit technique, will yield ICs that match ECL- and CML-based circuits in terms of speed, but at power dissipation levels equaled only by CMOS. "In short," he says, "I think we've got a winner."

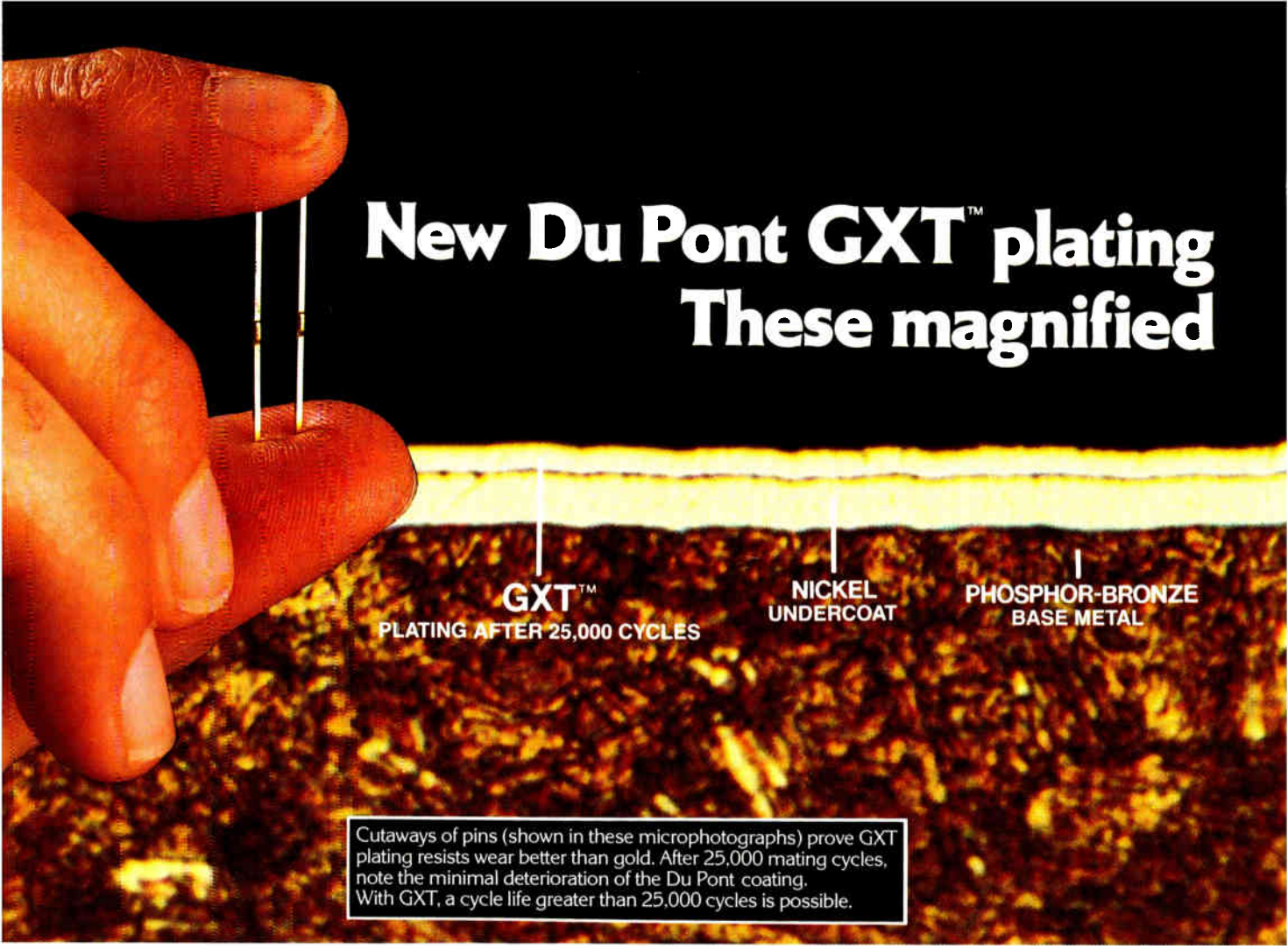
Both men are old-timers at Ferranti Electronics Ltd. on at least three counts. Both have been with the company since they graduated as engineers; both have been in the semiconductor business since the late 1950s and early 1960s; and both have been in on the development of the company's collector-diffused-isolation process and differential-logic technology from the beginning.

Educated at Oldham Technical College and Salford College of Advanced Technology, the 51-year-old Grundy joined Ferranti in 1955, shortly after graduation. After working on semiconductor rectifiers, photoelectric devices, and early integrated circuits—such as fast diode-transistor logic and operational amplifiers—he became manager of IC engineering in 1968 and was responsible for the development and introduction of the company's original uncommitted logic arrays in 1971. Grundy, who holds more than a dozen patents, and Bruchez coauthored several papers on earlier versions of CDI and differential logic.

EXPERIENCE PAYS: Grundy (left) and Bruchez have been working with Ferranti's CDI concept since its start.

Bruchez, 41, joined Ferranti directly after graduation from Liverpool University in 1967 with a bachelor's degree in engineering with honors in electronics. As semiconductor process development engineer from 1967 to 1969, he took a concept originally introduced by IBM as a starting point from which to develop Ferranti's original CDI process. Granted two patents for his work, he became group leader for bipolar process technology in 1969 and led development of CDI into large-scale integration. He also introduced positive photoresist and chrome-plate technology to the production line in advance of its acceptance by the industry in general.

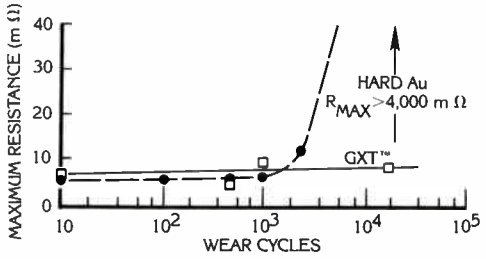
As head of bipolar LSI process technology from 1971 to 1973, Bruchez was co-originator and developer of Ferranti's uncommitted logic array technology using the CDI process. Before taking his current post as manager of microcircuit development in 1969, he served as the project manager in the development and establishment of the Microelectronics Center R&D facilities in Hollinwood.



Tests also show the GXT plating system is better than gold in solderability, porosity, bend ductility, and corrosion resistance. Yet GXT can reduce costs as much as 20%.

Independent testing laboratories have proved that the Du Pont GXT plating system is *superior to gold* in wear resistance, solderability, porosity, environmental corrosion resistance and bend ductility. And is as *good as gold* in contact resistance and wire-wrapping performance.

Moreover, connectors protected by this remarkable new coating system frequently cost considerably less than comparable parts plated with gold. For example, savings of up to 20% are possible on pins plated with GXT. (Savings depend on the price of gold and upon the amount of gold being replaced.)



GXT assures minimum contact resistance after wear and exposure to H_2S

By 25,000 cycles, gold shows contact resistance increases to 4,000 milliohms or higher. In contrast, GXT shows excellent electrical performance even after 25,000 cycles.

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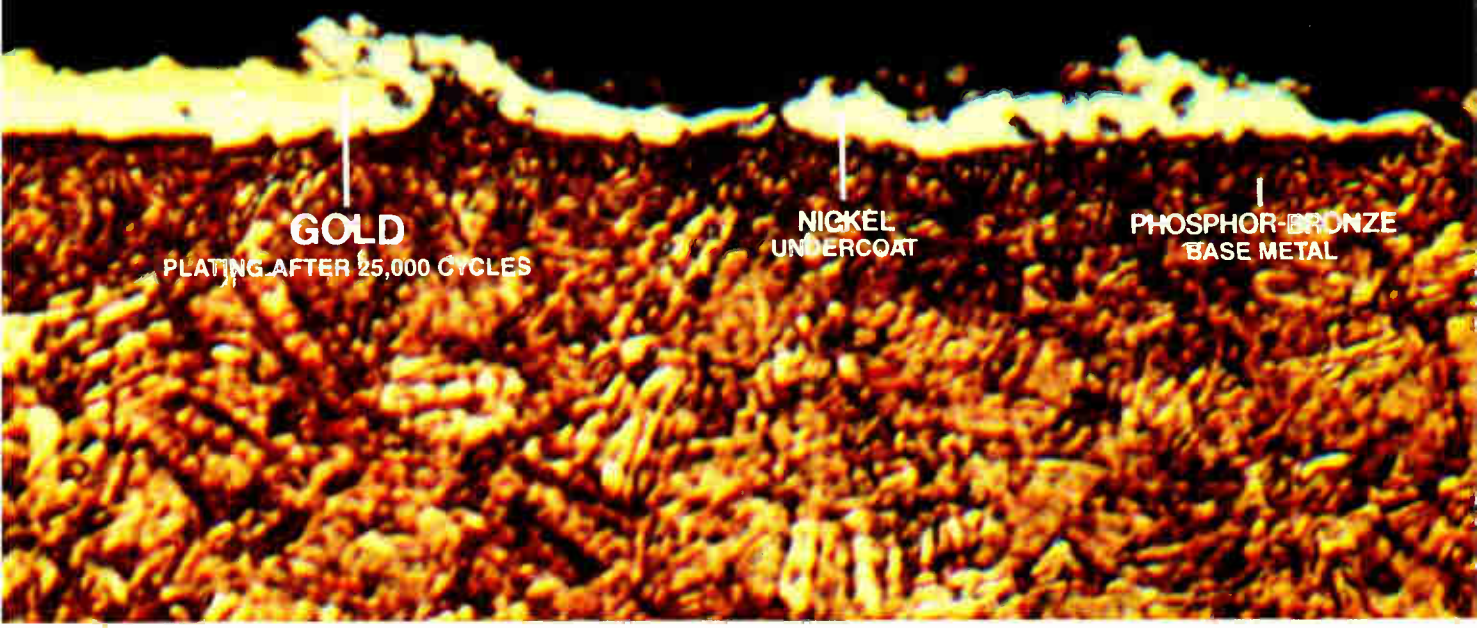

In these tests, other gold substitutes didn't measure up to GXT, either. In porosity, solderability, intermetallic growth, bend ductility, internal stress, and manufacturing process stability, the GXT plating system clearly outperformed all other gold alternatives including other palladium-nickel and pure palladium coatings.

In fact, in no test did any gold substitute—or gold itself—outperform GXT.

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CIM STARTS TO CHANGE THE FACTORY LANDSCAPE

Computer-integrated manufacturing is already a hit in giant automotive and aerospace firms, and now the electronics industry is beginning to get on board

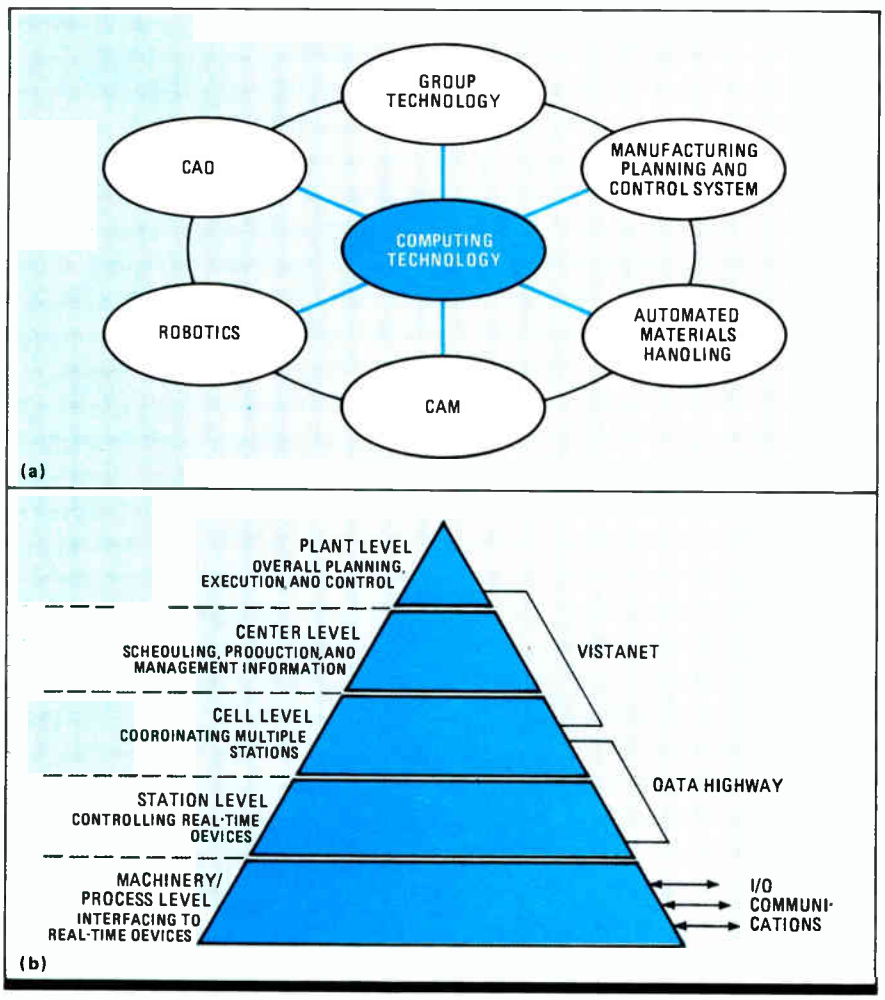
by Jerry Lyman

The U. S. industrial landscape is on the verge of a radical change as computer-integrated manufacturing starts to take hold. The computerized linking and control of the many activities needed to turn out an industrial product promises to reduce manufacturing costs and increase competitiveness. The automotive, aerospace, and heavy industries already are converting to CIM; some companies are even integrating expert systems into their CIM-controlled lines.

The electronics industry, however, has been holding back. Only such giants as AT&T, Hewlett-Packard, IBM, and Tektronix have put CIM fully into practice, though many electronics manufacturers already have many of CIM's major ingredients, such as mechanically linked islands of automation, robotics, automated equipment handling, and computer-aided design, engineering, and manufacturing. As in many industries, the roadblock is the high cost of integrating any complex production process.

Nonetheless, CIM is beginning to be used in integrated-circuit manufacturing, where yield and productivity are critical. It will also have a big impact on electronics manufacturers, in terms of the proliferation of equipment being built for the Manufacturing Automation Protocol and the market that MAP will create for electronics systems and components.

CIM provides extremely precise control over complex manufacturing processes, coupled with a strong flow of management information. As a result, it allows a substantial reduction in inventory with corresponding reductions in space requirements, overhead, and financing costs. In addition, it can cut direct and indirect labor costs, lower



1. CIM MODELS. Models of computer-integrated manufacturing include Arthur D. Little's (a) and Allen-Bradley's (b).

energy and raw materials consumption, reduce scrap and rework as a result of zero-defect production, increase uptime on the production line, raise production rates, yield products of higher quality, speed product introductions, and optimize information flow.

The CIM concept has many models. Among the most basic is Arthur D. Little Inc.'s simple, wheel-like representation (Fig. 1a) of CAD, group technology, planning and control systems, automatic materials handling, computer-aided manufacturing, and robotics activities. All of these activities are linked by a distributed network to a central computer.

Allen-Bradley Co. favors a pyramid concept (Fig. 1b) topped by the plant, which is responsible for overall planning, execution, and control. Then comes a center level for scheduling production and management information. Beneath the center level is the cell, which coordinates multiple stations. Next comes the station, which performs the logic functions needed to convert input from lower levels to output commands. The pyramid's base is the machinery that is linked to equipment on the plant floor.

Hewlett-Packard Co.'s generic CIM model is a layered configuration topped by a host computer. The next layer is plant and factory control. Then comes a layer of cell controllers, which manage dedicated equipment controllers arranged in clusters or cells. These programmable controllers make up the bottom layer.

CIM STATUS

Brian Moore, general manager of HP's Manufacturing Systems Group, notes that in all CIM models, integrating a manufacturing activity has two parts: hard automation, or mechanization, and systemization, or computer integration. HP recently conducted a survey to find out what manufacturers want most in future plants and how they would split the investment between mechanization and systemization (table).

In the aerospace industry, customized manufacturing resource planning, documentation links, and data collection are high on the wish list—not surprising given the government's need for vast amounts of documentation. In the electronics industry, provision for just-in-time manufacturing is on top. In the automotive field, the most wanted CIM features are order entry, purchasing, efficient scheduling, and inventory control. In addition, electronics, instrumentation, and automotible manufacturers all want CIM plans to facilitate strict quality control as well as to include process control.

HP also checked on how far along customers and potential customers were in implementing CIM, splitting them into three classifications. Stage one companies are considering or just moving into automation. Stage two companies have set up islands of automation and are trying to tie together these islands as well as develop a hierarchical link between the CAD/CAE/CAM information and planning activities. Stage three consists of the giant companies that already are working from a full-CIM plan.

Though the overwhelming number of respondents in the survey—75,000—are in stage one, the 100 to 150 companies in stage three have the lion's share of the market's dollar value at 50% (Fig. 2). In the U. S., stage three CIM companies include Chrysler, Ford, and GM, all of which have fully integrated, automated lines for automobile assembly. In addition, Ford and GM are using CIM in electronic assembly.

BUILDING IN EFFICIENCY

Another industrial giant, General Electric Co., is using CIM in a wide range of operations—for example, in a dishwasher plant, a locomotive plant, and a steam turbine plant.

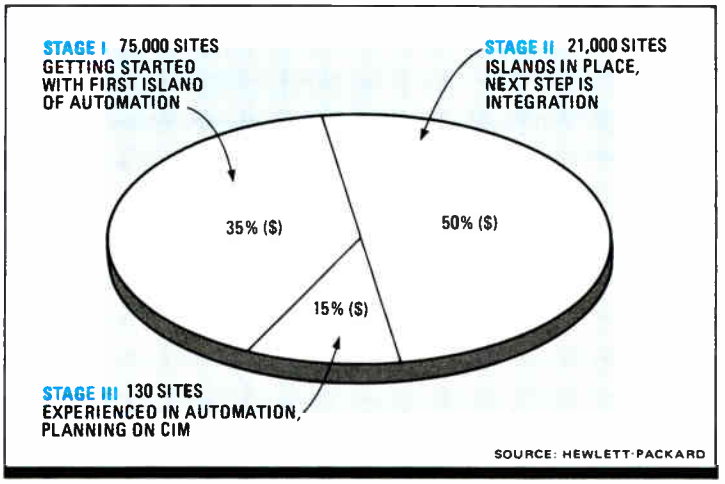
Most recently, GE has implemented CIM in a refrigerator compressor plant, where operations include machining, fabrication, and assembly. Because the production rate differs for each manufacturing cell, silos located between the cells store parts until a machine is ready to use them. A continuous conveyor connects the lines, cells, and silos. A robotic loader places each part on a machine for processing and removes it afterward. Based on the number of parts in the silos, the CIM system programs production; the machines go idle automatically when no parts are forthcoming.

This state-of-the art plant marries its manufacturing control system with its plantwide information system—one of CIM's foundations. The data-

WHAT MANUFACTURERS WANT FROM CIM

Aerospace	Electrical machinery; electronics	Instruments	Automotive
Customized manufacturing resource planning	Just in time (JIT)	JIT	Order entry
Real-time scheduling	Material handling	Material handling	Purchasing
Documentation links	Incoming inspection	Documentation links	Scheduling optimization
Data collection	Quality management	Data collection	Simulation
Cell control	Process control	Quality management	Inventory control
		Process control	Documentation links
			Quality management
			Process/cell control
Mechanization/systemization			
40/60	85/15	70/30	80/20

SOURCE: HEWLETT-PACKARD



2. STARTING CIM. About 130 U. S. companies have implemented CIM fully, but most manufacturers have only islands of automation or are still planning to start CIM.

acquisition system communicates directly with programmable controllers to collect real-time production data and status information.

Another industry where CIM has taken hold is aerospace. Companies such as Lockheed, McDonnell Douglas, and Rockwell International have both the resources and the government backing to have ongoing CIM programs.

Lockheed-Georgia Co., Marietta, Ga., has many facets of full CIM and is aiming for a fully integrated factory, which it labels the Factory 2000. For this factory's office portion, Lockheed has developed what it calls computer-assisted generative process planning. Genplan, which develops by computer step-by-step instructions for fabricating and assembling parts, has already cut process planning time by more than 60%.

The U. S. aerospace industry is using CIM to improve numerical-control milling, to automate design and stress analysis, and to place and solder parts on pc boards

On the factory floor, a joint Air Force and Lockheed Technology Modernization project (TechMod) takes over. This system consists of a computer network that links more than 40 numerical-control and computer-numerical-control metal milling machines. It has eliminated the need for n/c tapes and tape readers, increased machine usage, cut maintenance downtime through automated diagnostics, and reduced errors and scrap. Lockheed also has implemented CIM in a new sheet-metal center, an automated paint center, and a multifunction robotic work cell for routing extruded aluminum parts.

McDonnell Douglas Corp. has CIM programs for part design, stress analysis, and n/c programming. In addition, the Air Force has funded the $9 million Integrated Composites Center at the St. Louis company. This fully automated complex will manufacture advanced composite parts. Computers will share data to coordinate all phases of production, and the company says that printed work orders will be eliminated.

In August, Rockwell International Corp.'s Defense Electronics Operations, Anaheim, Calif., demonstrated completely automated manufacturing and materials handling facilities that should increase production efficiency enough to save millions of dollars on the Air Force's intercontinental ballistic missile programs over the next decade. The program was jointly funded by Rockwell and the Air Force. Both facilities, the automated manufacturing cell and the automated materials system, are controlled by a Tandem Computers Inc. NonStop fault-tolerant computer, which communicates with the Rockwell host computer over land lines.

The automated manufacturing cell is a computer-integrated robot-based manufacturing system that places and solders surface-mounted components on printed-circuit boards. It has a component preparation and kitting work station, two pick-and-place machines for robotic assembly, and vapor-phase reflow-soldering and automated cleaning systems.

The precision made possible though the facility's automation and process control will minimize scrap and rework, Rockwell says. This in turn will minimize subassembly costs and maximize subassembly quality.

The automated materials system was designed as a computer-aided materials processing and handling warehouse for receiving, receiving inspection, and warehousing under stringent government program requirements. Conveyors move parts from one station to the next, which eliminates the labor-intensive task of lifting and moving material.

The facility makes extensive use of cathode ray tubes, bar codes, and laser scanners. It can handle three times the current volume of materials flowing through the warehouse with no increase in manpower.

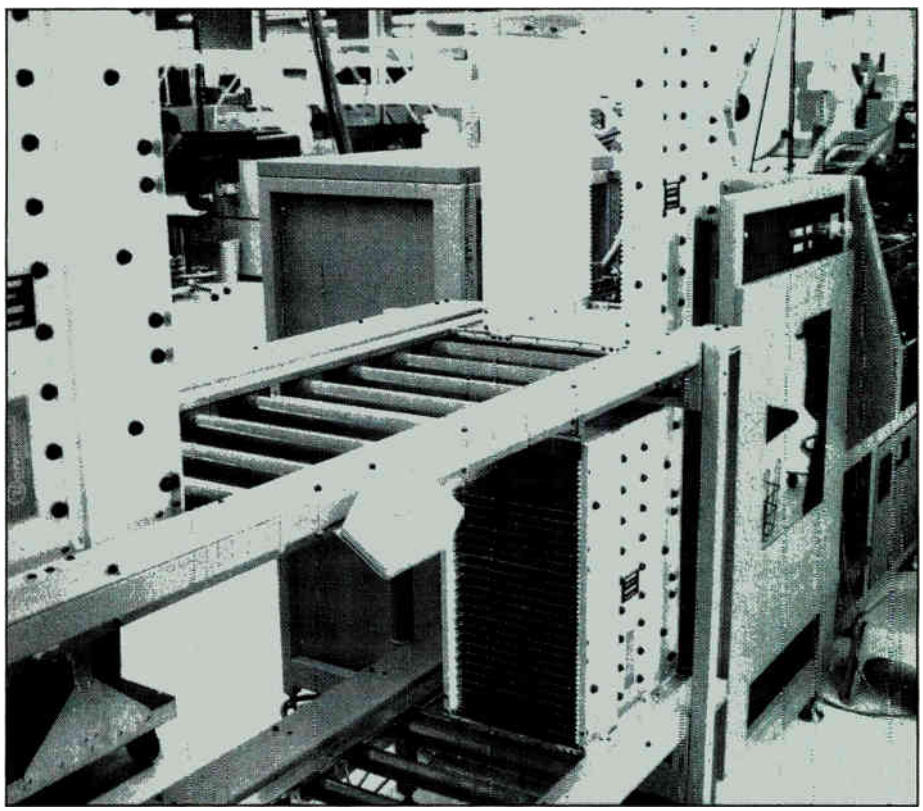
Most electronics manufacturers—with the exception of several industry giants such as AT&T, HP, IBM, and Tektronix that have CIM capabilities—are thinking of tying their islands of automation into a distributed computer network. For example, Racal-Milgo, Sunrise, Fla., has installed a flexible automated line (Fig. 3) in a Miami plant for assembling components on its customized pc boards for communications equipment.

The line, built for about $2.5 million in 1985, includes robotics, soldering, aqueous cleaning, and automated material handling. Real-time data collection provides the information to monitor and control the automated process, increasing output and reducing defects related to pc-board handling and manufacturing. Since its installation, the line has increased board output per

person by 50% and reduced workmanship defects to less than 5% of those found during circuit testing.

Engineers at the company's CAD facility create new board designs on VAX computers from Digital Equipment Corp., Maynard, Mass. This information is transmitted to Miami for manual programming into the computer there. Universal Instruments Corp., Binghamton, N. Y., makes the assembly line's automated insertion equipment as well as a proprietary operating system to network commands from two PDP-11/23 computers that control the on-line processes. These same minicomputers receive information on product quality and machine performance from each insertion machine.

For management reporting, the Racal-Milgo line uses Genrad Inc.'s Test and Repair, Analysis/Control System. The TRAC system gathers process data in the automated-line area, correlates it with data gathered at the test stations, which are not part of the line, and provides management with the real-time information they need to control quality and productivity. The Concord, Mass., company's system communicates with its own proprietary local-area network, GRnet. An emulation bridge enables the system to communicate with DEC computers.



3. MORE BOARDS. Racal-Milgo's flexible automated assembly line has increased board output by 50% and worker productivity by 80%.

Because the aerospace, automotive, and heavy-equipment industries now accept MAP, electronics manufacturers, especially in the programmable-controller field, are now busy supplying equipment either for implementing this protocol or for interfacing to it. For example, GE's Factory Automation Products Group already has demonstrated its MAP-compliant GEnet factory LAN. This 10-Mb/s broadband token-bus net provides high-speed communication among GE automation products and other MAP devices.

Allen-Bradley has its VistaMAP, a high-speed LAN that meets MAP standards for communications among incompatible computers, peripherals, and data networks. It operates at 10 Mb/s.

Texas Instruments Inc., Dallas, provides a gateway device called Tiway II to connect any MAP network and TI's industrial LAN, Tiway I.

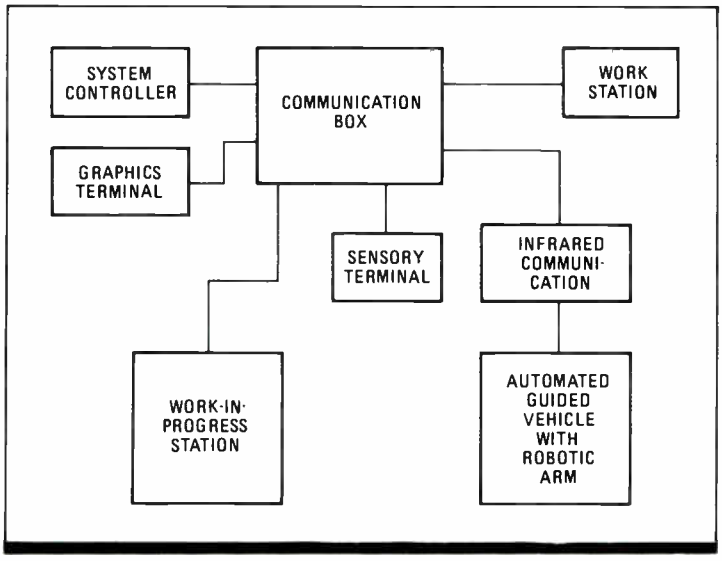
Outside the LAN field, Automatix Inc., Billerica, Mass., has a MAP-compatible controller, called Microspec, that inspects pc boards for the presence, location, and proper orientation of surface-mounted devices. Microspec checks SMD chip capacitors and resistors as well as active devices. It consists of a vision system, a specially designed set of lights and optics, and a material-handling system. The MAP interface has been done in software in its controller because "there presently are simply too many hardware options for a company of our size to sort out," says Mike Schuh, vice president of marketing at Automatix.

IC processing—with its demands of high productivity, quality, yield, extreme cleanliness, and, in the age of application-specific ICs, flexibility—cries out for integrated manufacturing. The depressed state of the IC industry almost guarantees that no overall conversion to CIM will take place for a while in the U. S. Such companies as IBM and TI do have CIM-controlled processes, such as TI's DMOS IV line in Dallas, but full CIM is still rare in the industry.

LIMITING CONTAMINATION

What is appearing are systems that tie together many IC processing modules, usually with the aid of robotics techniques. The aim of this type of system is not only to increase productivity but to limit contamination of wafers. An example is Flexible Manufacturing Systems Inc.'s CIM system for material handling in IC processing, which is based on a guided vehicle with a robotic arm.

In this system (Fig. 4), the system controller combines the function of a control computer and all its communications hardware. It feeds the communications system, which routes messages to the various components. In case of equipment



4. TOUCH AND GO. Flexible Manufacturing's system for IC processing includes automatic guided vehicles with robotic arms.

failure, intelligent work-in-progress stations, located throughout the manufacturing area, store the wafers until processing can continue.

At each station, operator interfaces allow inquiry and limited routing of lots of material. For operational interfaces, a supervisory terminal accesses the system controller, displaying text information on the location of material. Various software modules monitor material location, production, machine status, and the CIM system. The modules also report continuously to the system controller.

Also in IC processing, Veeco Integrated Automation Inc., Austin, Texas, recently sold a complete automated wafer-fabrication system to Sandia National Laboratories, Albuquerque, N. M. This system also is based on an automated guided vehicle with a robotic arm but adds distributed computing and communication. Its system control software operates on a DEC MicroVAX and the Veeco VIAlan communications network. Several local work-in-progress stations provide distributed inventory management for material that is handled by a V3000 series automated guided vehicle. This equipment will be used to load and unload process equipment on the Sandia CMOS fab line.

The next big step in CIM is the use of artificial intelligence; already some manufacturing systems blend in AI, but these are just the tip of the iceberg

A recent development is the appearance of CIM system integrators for IC fabrication, such as equipment from Thesis Group Inc., Dallas, and Qronos Technology Inc., Cupertino, Calif. Thesis has designed and developed a number of automated manufacturing systems for major electronics companies, including a prototype cell for an automated photolithography bay for Northern Telecom Electronics Inc., San Diego.

The cell combines a car-on-track monorail system, a three-axis clean-room robot, elevators, and a clean tunnel to automate the movement of cassettes of wafers through the lithography process's various steps, such as coating, alignment, development, inspection, and stripping.

A custom control system developed for the photo bay uses an unusual set of features. The cell controller is an industry-standard 32-bit minicomputer with a virtual-memory operating system. A hardware data-base processor attached to the controller's bus provides relational data-base functions. An advanced query language simplifies data-base access for personnel unfamiliar with data-processing techniques. The cell controller supports a variety of control methods within the bay, including SEMI Equipment Communications Standard II, SECS II emulations, RS-232-C, and proprietary message protocols.

Initial operational results show the cycle times in the new photo bay are only 14% of those for the equivalent manual photo area. Though no yield or rework improvement figures are available as yet, initial indications are promising. The cleanliness of the wafer areas was monitored using an aerosol-type laser particle counter. At the 0.5-μm level, an average of about two counts per day were observed. At the 0.3 μm level, the counts were too low to be significant.

While CIM is just beginning in IC fabrication, AI is being built into CIM systems on the factory floor. For example, the automation group at TI's Trinity Mills facility in Carrollton, Texas, is using an Explorer Lisp work station with AI software to create a control system that will automatically perform all scheduling and dispatching operations, eliminating people from the loop. The system will control this plant's flexible manufacturing system, which consists of five multiple-pallet four-axis milling machines, plus automatic guided vehicles and robots.

McDonnell Douglas is also heavily involved with blending AI into its integrated manufacturing. For instance, it has developed an expert system based on the Lisp language for determining a cutter selection program for n/c machining. This system captures the accumulated knowledge of experienced machinists and enables machinists with less experience to take advantage of this expertise. McDonnell Douglas is developing another AI package for the maintenance of n/c tools.

These two examples are probably just the tip of the AI iceberg in computer-integrated manufacturing. The coming years should see more examples of expert systems being designed into CIM loops for all types of manufacturing, including electronic assembly and IC processing. □

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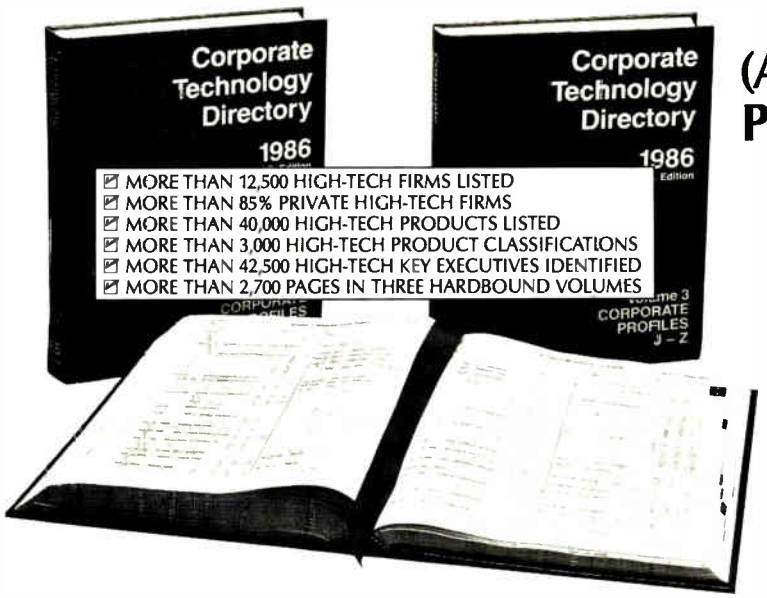

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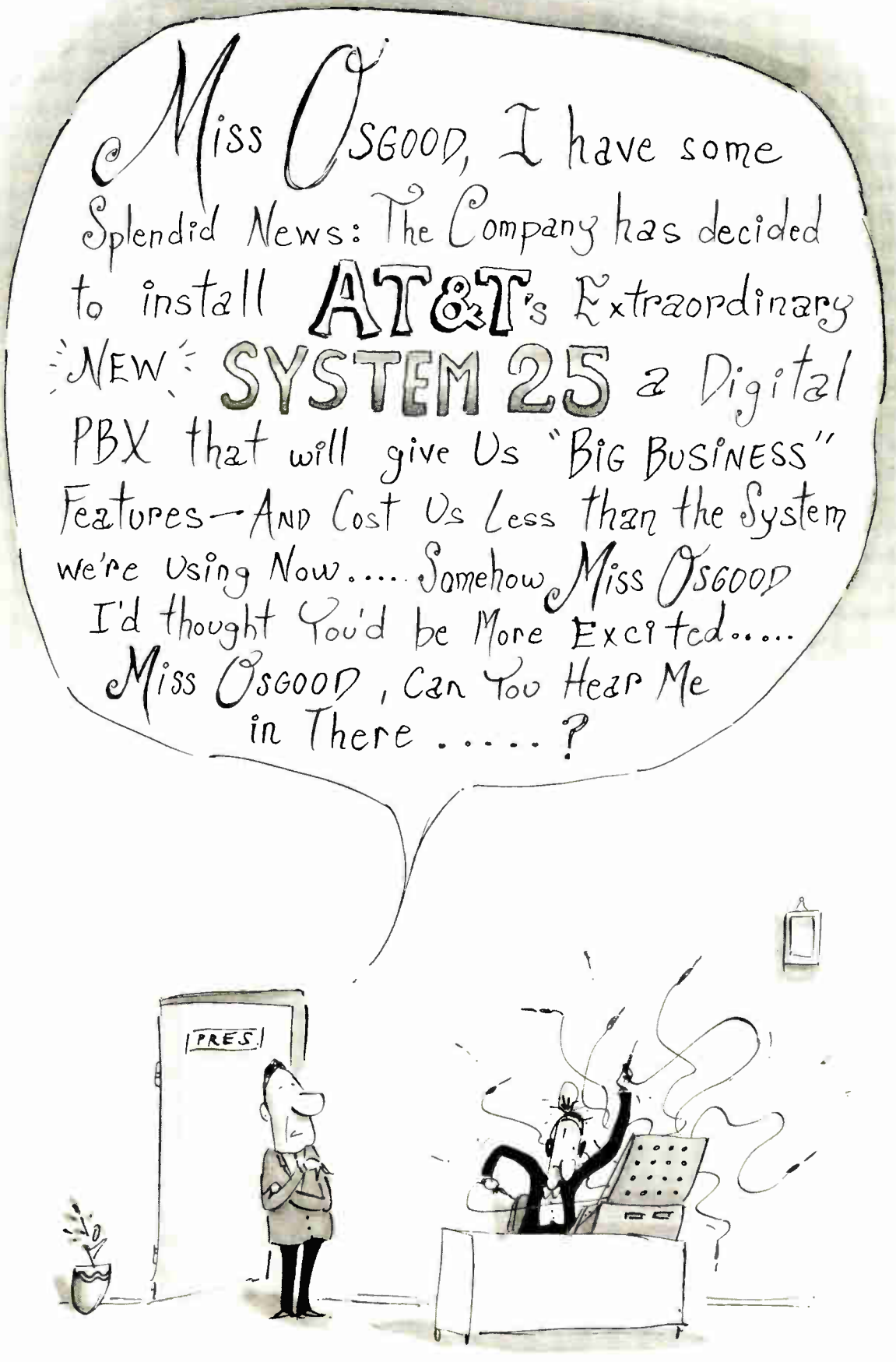

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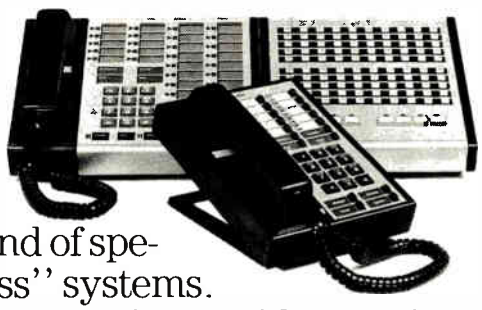

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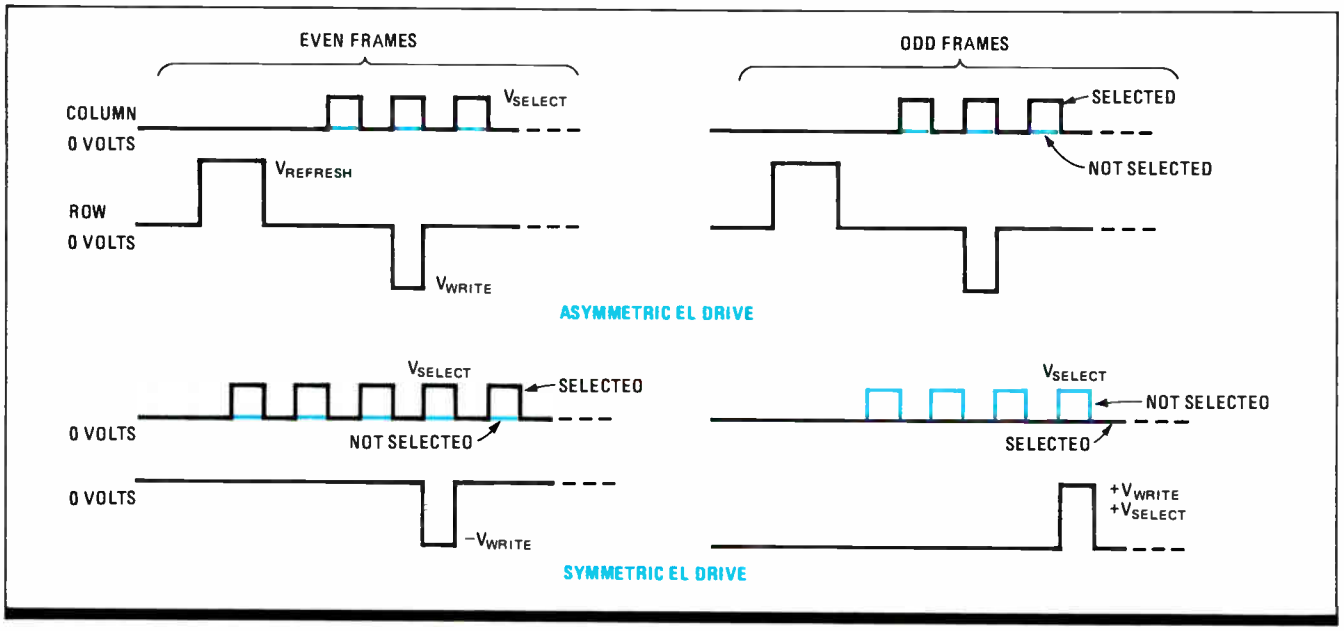
PROLONGING THE LIFE OF THIN-FILM EL FLAT PANELS

A process enhanced for high voltages produces symmmetric row drivers that overcome the latent-image problem in thin-film electroluminescent displays

Flat-panel display screens based on thin-film electroluminescent (TFEL) technology are making a bid to capture many of the applications now held by ac plasma panels, particularly in military equipment, where flat-panel demands are strongest. While TFEL displays lag behind plasma in development, designers find their ruggedness and lower power consumption attractive. And now their appeal will strengthen as a new approach to driving the displays eliminates one of the glitches that has plagued TFEL operation—what's called the differential-aging effect.

The new approach, from Texas Instruments Inc., begins with an enhancement to the Dallas company's Bidfet process, which combines bipolar and MOS transistors on a single chip. The enhancements double the output voltage of Bidfet devices from 120 V to 225 V, suiting them for use in symmetric row drivers that eliminate the differential aging problem.

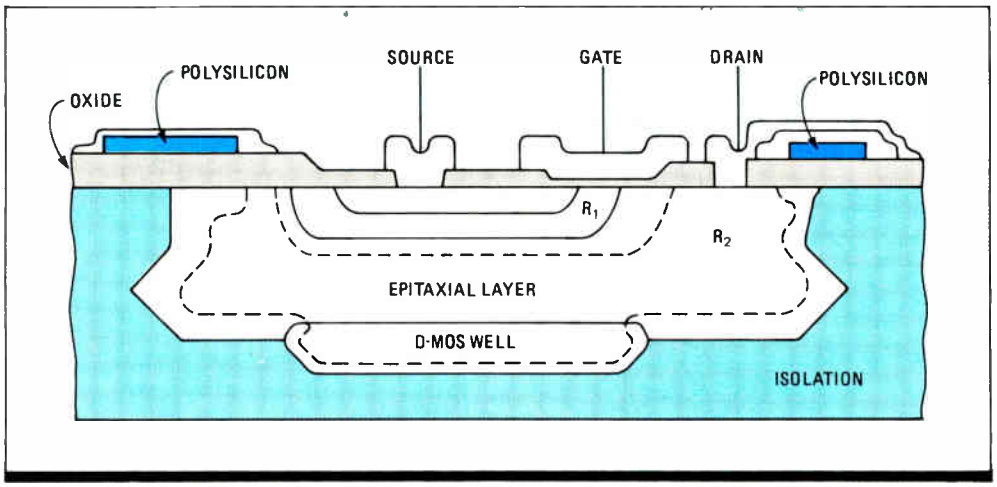
Differential aging is related to a panel's electrical characteristics and to the manner in which the panel is driven. For example, under conventional, asymmetrical drive, the screen tends to retain any continuously displayed pattern as a dim image that is not erasable. This could be a problem in such instances as a log-on menu that is displayed any time a computer is not in use. Known as a latent image, the pattern remains brighter than the background luminescence—unlike a similar effect that occurs on cathode-ray



1. GOODBYE LATENT IMAGE. Conventional thin-film electroluminescent display-driving chips use asymmetric waveforms. To prevent the latent-image phenomenon resulting from differential aging of the pixels, a new type of IC using symmetric drive has been developed for future displays.

tubes, where the retained image is dimmer than the background. Differential-aging effects that become too pronounced will severely shorten a TFEL panel's life in display monitor applications.

Early studies by TFEL-display manufacturers indicated that latent images were likely related more to the method of driving the panel than to its fabrication and materials. Further investigations concluded that the key to minimizing differential aging lay in compensating for or eliminating asymmetries in the driving waveforms applied to a panel.



2. DOUBLING UP. The enhanced Bidfet. process more than doubles the voltage-breakdown capability to 250 V. Adding polysilicon field plates helps overcome breakdown mechanisms.

To solve the problem, the panel manufacturers have turned to semiconductor houses, which have been supplying the asymmetrical driver chips. TI, a major producer of display-driver integrated circuits, has responded to the call with a design effort that is adding a new wrinkle to its well-established Bidfet process—which puts bipolar, double-diffused MOS (DMOS), and n- and p-channel MOS logic transistors on the same chip. The company's designers have converted the standard asymmetrical 225-V open-drain DMOS row-driver chip into a 225-V totem-pole Bidfet row driver that provides symmetric drive.

This is no minor processing change; it requires that the voltage-breakdown capability of the standard Bidfet driver configuration (120 V) be doubled. However, Bidfet is an ideal starting point for fabricating high-voltage, symmetric row drivers, because its only limitation is the maximum output voltage of the DMOS driver device.

TI designers also have succeeded in integrating into a single package the 225-V sink and source transistors needed to drive each row of a display. Other chip makers supply two devices—one with p-channel source transistors, the other with n-channel sink transistors—to drive each row of a display. So the single-chip enhanced-Bidfet drivers use fewer interconnections, less printed-circuit-board mounting space, and fewer interfacing signals, thereby offering a more cost-effective solution to TFEL-display driving than conventional devices. TI believes that, because of their many advantages over asymmetric drive, symmetric row drivers could become the industry-standard method of driving a new generation of TFEL displays.

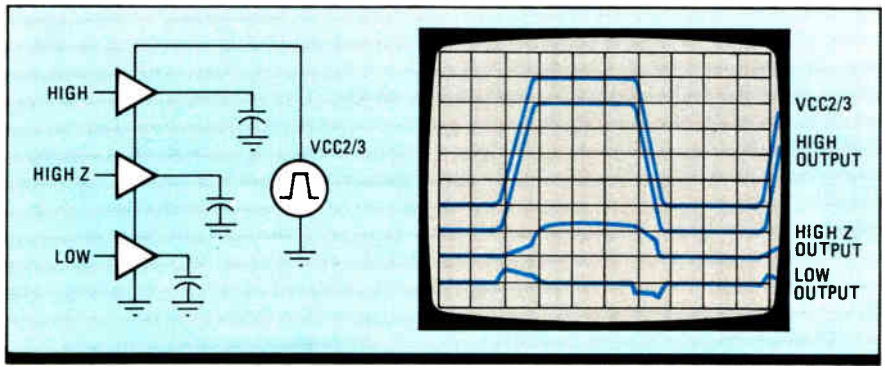
In what's now the industry-standard method, TFEL displays are driven by an asymmetric waveform that charges pixels with pulses of alternating polarity called write and refresh (Fig. 1, top). The two pulses differ in amplitude—+190 V and −210 V—and in duration, with the net effect of a dc charge on the pixels. This dc charge can cause "burned" pixels, which remain partially on when not selected. This is what causes the latent-image phenomenon associated with TFEL displays.

Also because of the unequal pulses used to address the pixels and the resulting unequal retention of charge, differential aging is greater at the top of the display screen than at the bottom. But when pulse amplitudes are made equal, as they are in symmetric drive, the differential-aging effects are equalized at the top and bottom of the screen.

A better approach is to drive each pixel with write pulses of alternating polarity in a symmetric manner (Fig. 1, bottom). There are important advantages to this approach. First, the pixels are driven with equal levels of positive and negative voltage—an ac signal, in effect—so no net dc charging occurs. As a result, the burned-pixel phenomenon is eliminated. Second, the absence of a high-current refresh pulse significantly improves a display's contrast ratio and lowers system power consumption. "Symmetric drive is seldom found in TFEL display systems, because until now, few row-driver chips have had this capability," says Bob Sheer, design engineer in TI's Display Circuits Group.

Symmetric write pulses eliminate 'burned pixels' so there is no latent-image effect; they also provide a higher display contrast ratio and lower system power consumption

To provide symmetric drive to TFEL panels, TI will offer a family of monolithic Bidfet row drivers—the SN65563, 65564, 75563, and 75564. The SN65563 and 75563 devices differ from the



3. THREE STATES. Waveshapes from high-voltage output sink and source transistors show that enhanced Bidfet structures withstand 250 V before breakdown.

SN65564 and 75564 only in the connection of drive signals to package pins. Two different pin configurations are provided to simplify pc-board layouts.

In all four chips, the positive write input signal controls the state of the display-driving output transistors. When that line is high, the Q outputs act as open-source drivers and output data is not inverted with respect to input data. Data inversion occurs when the positive write input is low. Serial data enters the on-chip shift register on the high-to-low transition of the clock input. A high on the enable input allows outputs with a high in their associated registers to be turned on. This causes the corresponding row to be connected to either the high-voltage Vcc_2 supply when the positive write input is high or to ground when it is low. A serial out line permits the cascading of additional row drivers.

When TI designers decided to develop a high-voltage symmetrical row-driver chip, they opted for the Bidfet process for three reasons. First, Bidfet provided all the components necessary for a symmetrical driver. Second, the process of-

CAD modeling software helped TI revise the standard Bidfet process to overcome the voltage breakdown problems that restricted device outputs to 120 V

fered an established reliability track record in TFEL applications. Finally, Bidfet is a proven high-volume, cost-effective process.

On the other side of the ledger is a negative: a TFEL row driver must combine low-voltage CMOS logic circuitry with 225-V three-state-output devices. And this is a problem with the standard process, because DMOS devices connected in a source-follower configuration have a breakdown voltage of only 120 V. TI designers identified three breakdown mechanisms in the standard process that had to be overcome to produce a high-voltage symmetrical driver.

The first problem occurs at the p-n junctions between the isolation and epitaxial tank in which the DMOS transistor is formed. Electrical breakdown takes place in this junction at or near the silicon surface due to electric-field intensification and curvature caused by an overlying high-voltage lead. The second mechanism involves the radius of curvature and the doping level of the DMOS backgate diffusion. These parameters in the standard process permit breakdown at less than the desired voltage. The third limitation of the standard process is that breakdown occurs in the bulk silicon between the DMOS backgate diffusion and the n+ buried layer. Each problem requires its own innovative solution.

To help them find those solutions, TI designers relied on two sophisticated computer-aided-design software packages: Supra, a two-dimensional semiconductor-process model, and Gemini, a two-dimensional electric-field analysis program. Inputs to Supra produce a junction profile and impurity concentration based on the processing steps. That is, if the program knows the length of time used in each process, its equations calculate junction profile and impurity concentration using a finite-difference method.

Supra's output serves as a Gemini input. The latter program allows designers to apply potentials to the junctions and silicon surface of a hypothetical device. It responds with parameters such as electric-field strength. Knowing the strength and location of electric fields allows designers to identify regions on a chip where avalanching—which represents voltage breakdown—can occur.

Revising the Bidfet process with the help of Supra and Gemini makes possible high-voltage devices (Fig. 2). To develop the new process, TI designers tackled each of the three limitations of the standard process in turn.

The first problem, breakdown at the junction of the epitaxial and isolation layers, involves electric-field intensification and curvature caused by overlying metal leads. A possible solution is to place a field plate over the oxide above the junction and then run the metal leads over the field plate. This shields the junction from the leads. The field plate can be biased if necessary.

To determine the suitability of this structure, TI designers created a Supra model. Gemini evaluated the model's behavior with bias applied to the field plate. It also evaluated other parameters, such as field-plate overlap of the junction and oxide thickness. These analyses confirmed that the epi-to-isolation structure the designers had come up with would satisfy the breakdown requirements.

Field plates also play a role in solving the second mechanism, the one caused by radius of

curvature breakdown between the epi and D-well. In this case, the radius of the electric field's curvature is more important than that of the diffusions. The designers believed a field plate overlapping the edge of a diffusion could modify the field distribution of the junction below. A Supra model was fed into Gemini to evaluate its performance under various amounts of field-plate bias. The results indicated the proposed structure would indeed be able to withstand the maximum drain-to-source voltage required in a symmetrical drive application.

To form the field plates that would solve two problems at once, the TI team added to the standard Bidfet process a polysilicon layer, as well as a deposited oxide to prevent shorting to the overlying metal. Both additions were incorporated with as little disturbance as possible to the standard process.

The third problem, breakdown in the bulk material of the semiconductor, turned out to be the easiest to solve. The team needed only to find a new optimum thickness and resistivity of the epitaxial layer. As expected, the new epi layer had to be thicker than the old because of the higher voltages involved.

But the added thickness created a new problem: the standard isolation process would not penetrate the thicker epi layer without excessively long drive times. Therefore, the team added a p-type buried layer to the substrate before deposition of the epitaxial layer. This gave the driver chip a process component that diffuses up from beneath the epi layer, in addition to the usual down-diffusing component introduced on top of the epi layer.

Each row of a TFEL display requires a sink/source driving circuit capable of withstanding 225 V, and the high-voltage Bidfet process turns out just that: a three-state, DMOS-based row-driver device capable of sustaining 250 V. Low-voltage logic signals from the CMOS circuitry independently control the output sink and source transistors. That independent control allows the output transistors to be set to any of three states: high-voltage, low-voltage, or high-impedance, in which both output transistors are turned off. The source transistor can deliver 80 mA and is supported by a built-in depletion-mode n-MOS transistor connected between its gate and source to ensure turn-off when the source transistor is not selected. Level-shift circuitry is simply a current-limited pnp transistor with a DMOS drive switch. The lower-stage DMOS output transistor is capable of sinking more than 100 mA.

Oscilloscope waveshapes demonstrate the doubled voltage-breakdown capability of the new Bidfet process. Each of the traces of the circuit's output-switching waveforms (Fig. 3) is offset by one division on the scope display for clarity. The waveform in the high-voltage state tracks the TFEL display-energizing voltage (Vcc_2) perfectly. In the low-voltage state, the output voltage is less than 1 V from ground. And in the high-impedance state, the output voltage is, as expected, undetermined—it drifts anywhere between Vcc_2 and ground. The important fact is that both the upper- and lower-stage transistors of the totem-pole output can withstand the full supply voltage, which is 250 V in this case.

That ability gives the enhanced Bidfet technology potential far beyond its initial use in single-chip synchronous TFEL row drivers. Integrating multiple components on a chip that is capable of withstanding high voltages opens the door to low-cost banks of smart power in a variety of applications. □

CAD TOOLS CAN'T SUBSTITUTE FOR EXPERIENCE

Although modeling software is necessary to quantify parameter values in a project such as the development of Texas Instruments Inc.'s enhanced Bidfet process, it cannot substitute for engineering experience or knowledge of a semiconductor process. "We knew about epi-to-isolation-surface breakdown by analyzing our 100-V Bidfet parts, and we knew from the literature that this type of problem did exist," says Steve Sutton, display circuits engineering manager at TI in Dallas.

Sutton, Dan Mosher, process development engineer in TI's Process Development Group, and Bob Sheer, a design engineer in the Display Circuits Group, had a solution in mind. And computer modeling did come to their aid, thanks to work at Stanford University, Technology Modeling Associates of Palo Alto, Calif., and TI's own Design Automation Group. Two computer-aided-design programs from Stanford—Supra and Gemini—were able to provide the specifics the designers needed to modify the Bidfet process.

CAD software came in handy again to calculate the new thickness of the epitaxial layer and to figure how much the buried layer would up-diffuse. Designers understand the nature of the problem, but, as Mosher puts it, "rather than try 10 different variations in silicon and wait two months for an answer, we ran the programs overnight on our IBM 4341 and got our answer the next day." Therein lies one of the great advantages of modeling software: it permits designers to experiment with a process-development program away from the wafer-fabrication line.


SHEER


MOSHER


SUTTON

While Sutton and Mosher acknowledge the importance of Supra and Gemini, they point out that semiconductor modeling programs are still evolving and are far from perfect. In fact, they are most useful in situations in which chip designers have sound theoretical knowledge, and where the process variables can be tightly controlled. In the case of the Bidfet modifications, the designers understood all three breakdown mechanisms that limited voltage and how to model them. The software's role was to perform many iterations in a very short time while eliminating costly wafer runs on the production line.

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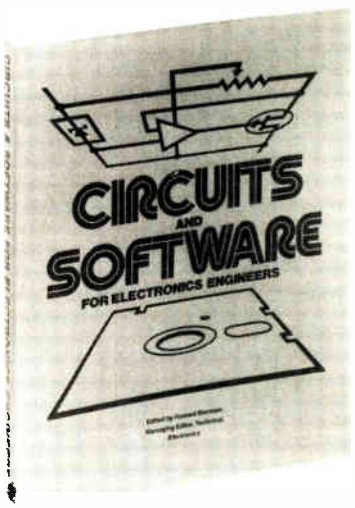

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THIS SMART POWER CHIP BREAKS THE 100-V BARRIER

Until now, smart power MOS FETs have stalled at the 100-V mark—but Ixys' approach has yielded first silicon of a chip that can run at 500 V

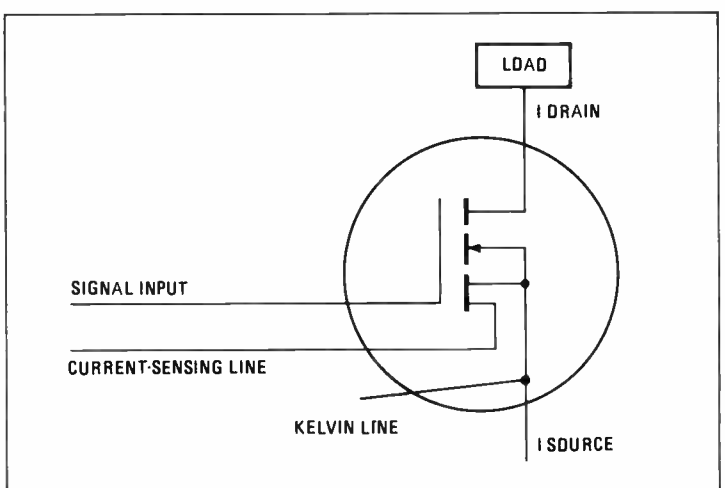
The tantalizing promise of smart power technology—the combining of low-power digital logic devices and high-power output devices on the same chip substrate—is to reduce manufacturing costs and the complexity of control applications. By putting low-power control logic and a high-voltage power device on a single chip, much of the processing that would otherwise have to be done by an external microprocessor can be offloaded onto the chip. So far, however, there has been a troublesome threshold that has prevented designers from coming up with smart power chips that can reliably handle more than about 100 V. The problem: isolating the sensitive control circuitry from the high voltages in the power circuit.

Crossing the threshold offers great rewards. That end of the power device business is exploding. Production of power devices rated at more than 400 V is growing three times faster than the power market as a whole. This opens up a huge potential market for smart power chips in process control, switching power supplies, automotive applications, and appliances—if any company can make them work. Of the $155 million in power MOS devices shipped in 1985, those with over 400-V output constituted 20%, according to Dataquest Inc., a San Jose, Calif., research company. The 1986 projection pegs those figures at 25% of a $215 million market, and Dataquest expects the market to reach $700 million by 1990.

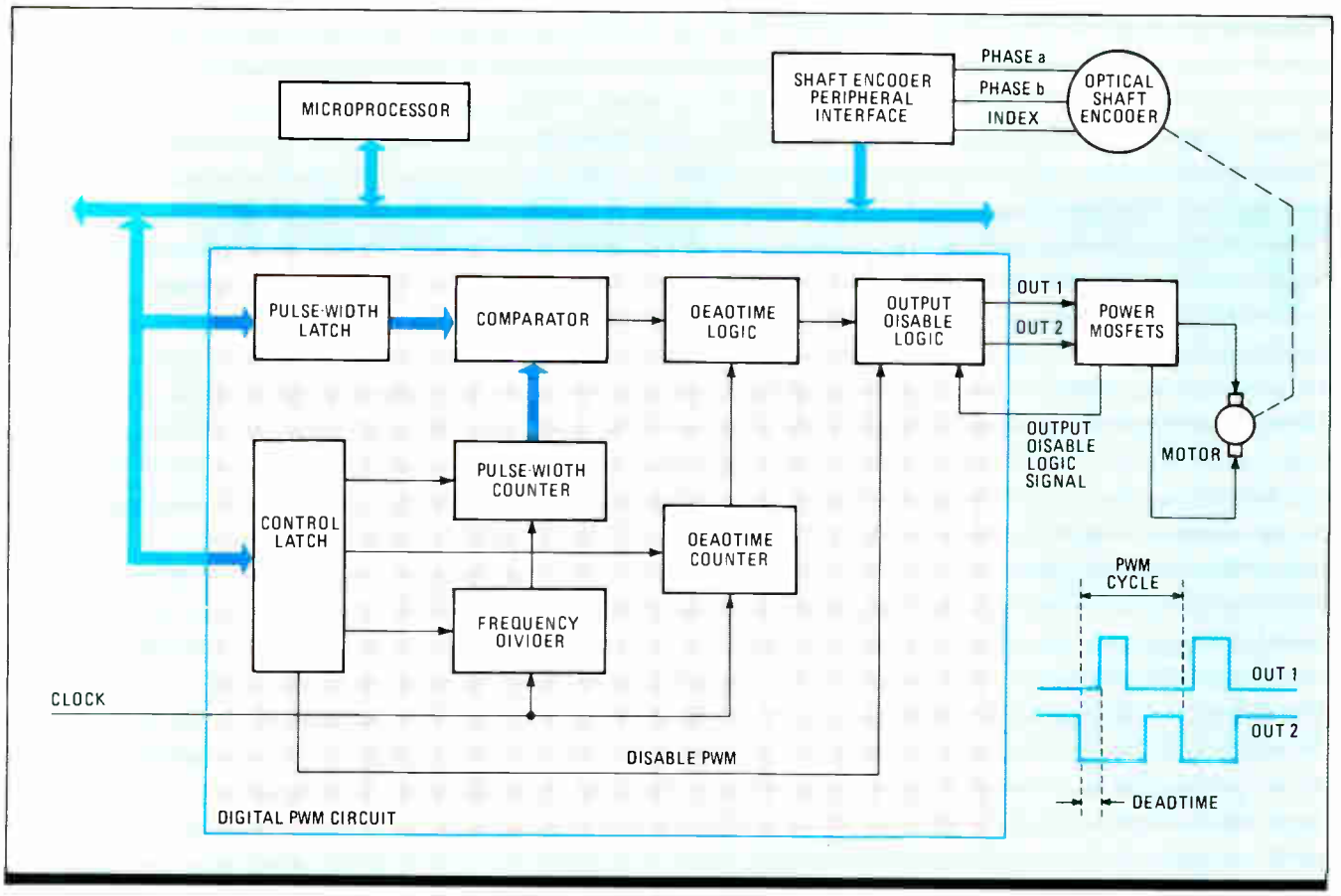
Ixys Corp. is betting that it can produce a smart power chip that will help it grab a piece of that market. Using a new approach that combines low-power CMOS control logic with a proprietary high-performance double-density MOS (HDMOS) power chip, the San Jose, Calif., company has achieved first silicon of a chip that operates at 500 V and 25 A. Its goal is 1,000 V at 10 A. And it expects to bring high-voltage smart power products to market by early 1987. "So far, no smart power device operating at more than 100 V has appeared," says Dan Schwob, vice president of marketing at Ixys.

This is the way it will play: first, Ixys will release three products this fall—the MirrorFET, which is a power device with a built-in sensor that can report to a remote microprocessor the current flowing through the device, and two pulse-width-modulation control chips, one analog and one digital. By early 1987, a small amount of logic will be placed on a production FET, and by the end of 1987 the analog and digital pwm circuits will appear on smart power chips.

Ixys chose to implement its logic circuitry in CMOS for a variety of reasons. One of the most



1. BUILT-IN SENSORS. Ixys's MirrorFET has a current-sense lead that picks up 1/1,000th of the drain current. A Kelvin circuit monitors stray impedance so that an external differential amplifier can factor out source inductance.



2. DIRECT CONTROL. Taking digital control information directly from the microprocessor, the IXDP610 circuit varies the pulse width of the square wave applied to the power MOS FETs that drive the motor. In 1987 the circuit will share a chip with the MirrorFET device.

important of these is that CMOS can accommodate variations in the power supply voltage without being affected. As a result, the designer does not require a highly regulated Vcc. In addition, the CMOS output voltage can swing from ground potential all the way to maximum Vcc, the level required to turn on the MOS FET.

In addition, CMOS can operate at 15 to 20 V. Power MOS devices need a 10-V or larger input pulse in order to switch on, and it is far easier to implement a CMOS device on a chip for switching these power devices than it is to use an alternative technology, such as n-MOS. To top it all off, CMOS devices also draw very little power.

Also, "CMOS has the advantage that there are more readily available building blocks than in other technologies," declares Nathan Zommer, executive vice president and chief technical officer of Ixys. "Voltage references, operational amplifiers, comparators, etc., are implemented much better in CMOS than in n-MOS."

Another important reason for choosing CMOS is its process similarities to the company's HDMOS technology. CMOS has so much in common with HDMOS that Ixys believed it could integrate the two into a single, economically viable manufacturing process.

Ixys is approaching the evolution of its smart power chips in two stages. For the time being, the company is keeping the CMOS and MOS functions separate, while it solves the problems of integrating the two into a single chip. "We are developing smart power one step at a time," says Schwob. "As we build more powerful MOS FETs, we are creating separate low-power CMOS analog and digital circuits. Eventually, we will merge all or a portion of the low-power CMOS control circuits onto our power devices."

STEP BY STEP

This month, the company will introduce the MirrorFET, so called because it "reflects" to an external control circuit how much source current is flowing through it. As a first step toward smart power, it incorporates sensing capability into a high-power MOS FET device. In October, Ixys will introduce a digital pwm control chip, the IXDP610. Then, in November, the company will bring out its IXMS150 analog current-mode pwm controller.

In building the MirrorFET (Fig. 1), the company incorporated the minimum amount of sensing capability needed to control the power device from an external control circuit. Two sensors are used to determine the current flow through the power device: a current-sensing line and a Kelvin line. The current-sensing line—bonded to one of a thousand miniature FETs that make up the

power device—carries 1/1000th of the drain current of the device, which therefore can be monitored. Because inductance in the source-current lead can render the current-sensing reading incorrect, the stray impedance in the lead is monitored by the Kelvin line; an external differential amplifier factors out the error.

Ixys' digital pwm circuit (Fig. 2) will be used with the MirrorFET in motor-control applications. It accepts an 8-bit pulse-width command from an external microprocessor and produces two modulated pulse streams. The pulse width of the output streams can vary from 0 to 100%. The Ixys pwm chip will connect directly to a microprocessor bus and will be able to generate the modulated pulse streams without requiring a digital-to-analog conversion of the microprocessor output.

In this closed-loop system, the microprocessor modulates the pulse width using a feedback signal from an optical shaft encoder and a shaft-encoder peripheral interface chip. The microprocessor enters a hexadecimal value into the pulse-width latch to compensate for errors detected by the interface chip. The comparator derives the pwm output waveform by comparing the output of the pulse-width counter and the pulse-width value stored in the pulse-width latch. The result of the comparison determines which power MOS FETs to turn on and for how long.

Programmable dead time—the time between the leading edge of Out1 in Fig. 2 and the leading edge of Out2—is incorporated into the waveform by the dead-time logic. The dead-time counter counts the number of input clock cycles to determine the dead-time period. The dead time is the amount of time needed to turn one set of power transistors driving the motor off and turn the other set on. How many clock cycles to count is specified by the control logic and is a value that is preset during initialization of the circuit.

The IXMS150 analog pwm circuit is designed for controlling stepper motors and for switching power supplies. For stepper-motor control, the circuit promises to deliver better smoothness and accuracy at a lower cost than can a board-level controller or a closed-loop dc servo. It can improve the accuracy of a 200-step/revolution stepper motor to equal that of a 20,000-step/revolution unit.

Making these products work with CMOS circuits on the same substrate with power transistors is no easy task. The noisy environment on the high-power transistor substrate creates a high parasitic capacitance that causes the CMOS devices to latch up. In addition, a high-power MOS FET operates at extremely high temperatures, often 150°C and higher, whereas low-power CMOS digital logic devices typically operate at no more than 80°C. Elevated temperatures increase the conduction of parasitic currents, thereby increasing the likelihood of latchup.

Ixys is developing new technology to overcome these problems in its smart power chips. The company is making changes to the topology, the layout of cells in the low-power CMOS section of the chip, the CMOS process used for the control functions, and the vertical structure of the cell on the substrate. With these changes, Ixys expects to place low-power CMOS control logic on power MOS devices that can handle up to 1,000 V at 10 A.

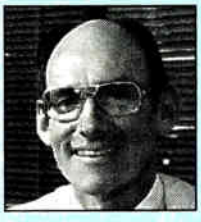
In order to control costs and maximize yield, Ixys will keep the number of mask steps used to fabricate the smart power chips to a minimum. Conventional CMOS typically requires 12 or 13 mask steps; power MOS devices typically require seven or eight steps. "We plan to produce the smart power device using only 11 or 12 steps," says Mark Barron, vice president of engineering and operations. The secret: the process similarities of CMOS and Ixys' HDMOS power FET technology, which allows the two circuits to be fabricated side by side. □

THE FAST TRACK TO 500-V SMART POWER

Nathan Zommer is wasting no time in the race to bring high-voltage smart power chips to market. "To arrive at smart power, we will begin by incorporating medium-scale integrated circuits with the power MOS circuit," the president of Ixys Corp. says. "The first silicon examples of our initial smart power chip designs are functional and require only minor refinement to achieve the full rated 500-V output."

ZOMMER

The San Jose, Calif., company is preparing building blocks that can go together quickly. "We've developed our existing products in such a manner that we will ultimately end up with a smart power line," says Dan Schwob, vice president of marketing and sales. "In creating a low-power CMOS line, we've developed the expertise to build efficient CMOS control circuits. In refining our line of power devices, we developed a high-power process that can easily accommodate CMOS logic or analog circuits on-board."



BARRON

SCHWOB

Since Ixys has no fab line of its own, the company has become technical partners with Samsung Semiconductor & Telecommunications Co., Seoul, Korea. Pilot production will begin at Samsung's Santa Clara, Calif., wafer fab facility, but full-scale runs will be done in Korea. "Samsung is a fine choice to manufacture our products," says Mark Barron, vice president of engineering and operations. "The company has the latest in process equipment.... Not only do we get a low cost of manufacture, we also get the latest in processing equipment."

All three Ixys founders are former General Electric Corp. engineers. Zommer came to GE via Intersil, where he had developed a power MOS line; Barron had been senior vice president of research and development at GE Calma Company, Milpitas, Calif.; and Schwob had been product marketing manager for bipolar and MOS power circuits at GE.

THE APPLE II: TEACHING AN OLD DOG NEW TRICKS

A 2.8-MHz microprocessor more than doubles its speed; high-resolution modes sharpen the graphics; and a 32-oscillator synthesizer makes the machine talk

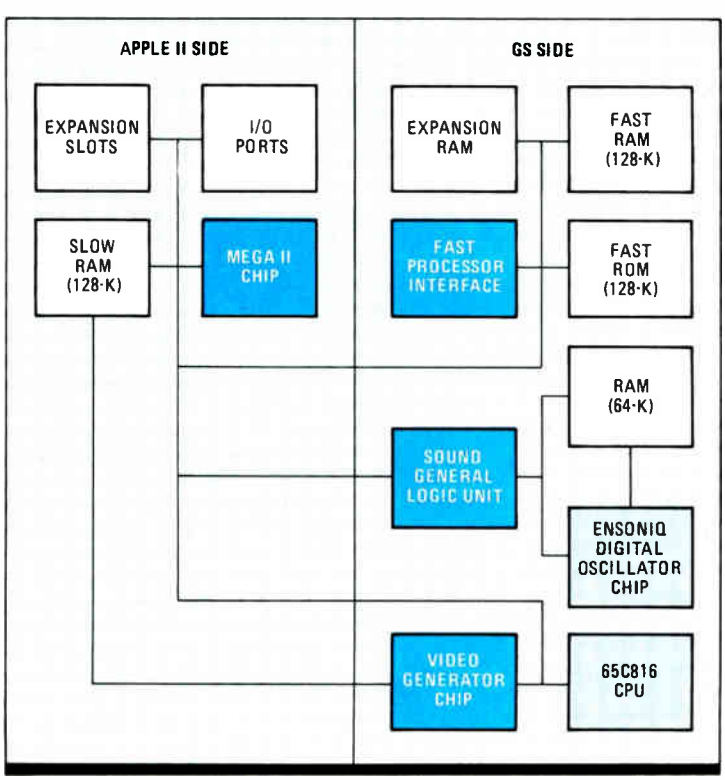
Designers at Apple Computer Inc. have taken the Apple II and made it once again a personal computer to contend with. The Apple IIGS not only has a more powerful microprocessor that still can execute most Apple II programs. It also boasts new display features such as two super-high-resolution graphic modes that don't sacrifice crispness for color and a sound-generating system based on a synthesizer chip that has 15 independent voices. In fact, the GS in the new computer's name stands for graphics and sound. Other innovations include up to eight megabytes of memory expansion and software features geared to help programmers develop applications.

Essentially, the new machine has two sides (Fig. 1)—a II side and a GS side, both with features that ensure compatibility with older Apple IIs. On the Apple II side, it has slow RAM, expansion slots, ports, and the Mega II, a single-chip version of all Apple II circuits except the CPU and RAM. On the GS side, it has such new features as a Western Digital 65C816 microprocessor, the Apple II graphics support in the video generator chip, and a sound-generating system consisting of a digital oscillator chip, sound-storage RAM, and a logic chip.

The Apple IIGS's 65C816 central processing unit is a 2.8-MHz 16-bit CMOS design based on the 6502 used in the earlier Apple IIs. The 65C816 has 16-bit data registers and a 24-bit internal address bus that enables the machine's 256-K-byte memory to be expanded by 8 megabytes [*Electronics*, Sept. 18, 1986, p. 23]. It has 11 new addressing modes and 36 new instructions beyond the 6502.

Despite the new CPU's increased power, it can still emulate the 6502 and 65C02, meaning that it can execute 6502 instructions either at the standard Apple II clock rate of 1 MHz or at the faster Apple IIGS speed of about 2.5 MHz.

The Apple IIGS will run at the slower speed for one of three reasons: when a program selects the slow speed because it is executing an instruction that uses the slow memory; when a timing-dependent routine is executing—probably an operation of a disk interface card; or when



1. DOUBLE DUTY. The Apple IIGS has its own complement of chips plus a set that makes it compatible with Apple II models.

the user selects the slower speed by means of the control panel, a program that is used to set a number of the machine's operating parameters.

The graphics and text display features for the Apple IIGS (Fig. 2) include all five Apple II display modes—40- and 80-column text; low-, high-, and double high-resolution color (40 by 4, 260 by 192, and 560 by 192 pixels). It also has two new super high-resolution modes—a 320-by-200-pixel mode that displays 16 colors out of a palette of 4,096 and a 640-by-200-pixel mode that displays 4 colors out of 4,096. A custom video graphics controller chip supports the five resolution modes.

All four high-resolution graphics modes drive the Apple IIGS's new red-green-blue video output. Unlike standard and double high-resolution modes, the super high-resolution modes do not sacrifice resolution to get color.

The designers of the Apple IIGS included a one-two punch for realism by enhancing sound as well as graphics. The means: Ensoniq's 32-oscillator synthesizer, which generates sounds from digital samples stored in 64-K bytes of dedicated random-access memory and is used in music synthesizers. "Most chips could give you beeps and boops," says hardware engineer Brian Moore. "This one plays Beethoven's Fifth." The team designed another custom chip, the general logic unit, to interface the Ensoniq chip and its RAM asynchronously to the Apple II side containing the Mega II chip and the input/output ports.

DESIGNING IN COMPATIBILITY

One of the early hangups was in making existing Apple II software run faster on the Apple IIGS. The software engineers wanted a clean memory map for new programs, but existing software is designed to enter memory at location 00000. Working from an idea of Apple cofounder Steve Wozniak, Moore designed a fast processor interface chip that altered I/O points.

Revamping ROM for the new IIGS could have made it difficult to ensure total compatibility with existing Apple II software. Nevertheless, the team bent over backwards to accommodate existing programs. "In designing the new ROM, we found that some of the most popular software wouldn't work," says Dan Hillman, chief hardware designer. "We put them on a logic analyzer and saw that some of it was due to copy protection and some was due to use of the wrong entry points."

Adds Bachman, "If it was at all possible, we accommodated them. We listed them as new published entry points. Now that they're published, we'll be more hard-nosed."

The IIGS's memory banks run at two speeds. The minimum high-speed memory in the Apple IIGS is 256-K bytes, of which programs can use up to about 176-K bytes. The slow-speed memory is 128-K bytes to match the maximum memory of the Apple II. The Apple IIGS also has a special card slot for RAM expansion of up to 8 megabytes. All the RAM on a memory card is available for Apple IIGS application programs if they call the memory manager—memory-management code residing in read-only memory.

When the Apple IIGS is running an Apple II application, the memory available for that application is the same as in an Apple IIc or a 128-K-byte Apple IIe. The first two 64-K-byte banks work like the main and auxiliary banks, complete with language-card spaces, display buffers, and I/O space at location $C000.

BUILT-IN PROGRAM ROUTINES

In addition to all the compatibility features, the Apple IIGS has several new software features that are important for application program developers. First of all, there is the toolbox, a collection of built-in program routines that can be called by applications. Then there is the program development environment, called the Apple IIGS Programmer's Workshop. It includes the language compilers.

The languages available on the Apple IIGS include assembly, C, and Pascal. Thanks to the standard object file format, a new feature available for the first time on an Apple II, the Apple IIGS linker and loader can handle program segments created in any of the languages.

The primary high-level language that is used in the Apple IIGS Programmer's Workshop is C. Programs written in C can easily include sections written in assembly language and in Pascal. Apple IIGS Workshop C comes with a standard C library and a Apple IIGS interface library.

2. RIVALING REMBRANDT. The high-resolution graphics modes of the Apple IIGS combine crispness with color in their pictures.

Apple IIGS Pascal is similar to Macintosh Pascal and to Apple II Instant Pascal. Apple IIGS Pascal works with ProDOS 16, the 16-bit version of ProDOS created for the Apple IIGS.

The assembler is a full-featured macro assembler that supports the instruction sets for the 6502, the 65C02, and the 65SC816.

PROGRAMMING AIDS

To provide a consistent working environment, the Programmer's Workshop incorporates a set of programs that makes it easier to develop applications for the IIGS. They include the operating shell for controlling the language compilers, along with a program editor, a debugger, the linker/loader, and utility programs.

Among other new features, the Apple IIGS desktop bus is a simple I/O port that supports the detached keyboard and built-in mouse interface. The bus also provides an inexpensive way to connect additional input devices such as hand controls, graphics tablets, and numeric keypads.

The Apple IIGS also has a built-in disk I/O port similar to the one on the Apple IIc. It can handle both 5¼-in. (UniDisk or DuoDisk) and 3½-in. (UniDisk 3.5 or Apple IIGS 3.5) disk drives, connected in a daisy chain of as many as four drives. Its seven expansion slots are almost identical to the slots in an Apple IIe and can accept most Apple II peripheral cards.

The Apple IIGS has a built-in real-time clock, powered by a long-life battery. The user sets the clock by means of the new control panel program. The control panel is a ROM-resident utility program that enables the user to set machine parameters such as CPU operating speed, video display, I/O port assignments, and slot allocation.

The ROM monitor has been enhanced with several new features, including the ability to handle the long addresses required for the expanded memory, and a mini-assembler and disassembler for the 65816 microprocessor.

The AppleTalk LAN interface is built into the Apple IIGS, unlike the Apple IIe and Apple IIc, which need an optional peripheral for AppleTalk.

This new flagship of the Apple II line provides an easier and faster way to run the 10,000 or so programs created for Apple II computers. In addition, it provides a platform for promising new programs that will fully use the enhanced color and sound, large memory, and the graphical and mouse user interface. □

HERE'S ONE DESIGN TEAM THAT KNEW JUST WHAT THE USER WANTED

The designers of the new Apple IIGS had a head start on achieving their goal of creating a 16-bit successor to the phenomenally popular Apple II: they knew from experience what had to be done.

"Everybody who worked on this project is a user," says hardware engineer Rob Moore, an Apple hobbyist long before he joined the company in August 1984. "We all had a feel for what the Apple II user wanted—a faster machine with more memory, graphics, and better disk drives."

Nevertheless, the team had to overcome some severe obstacles, one of which was Apple's indecision over what kind of computer to make. Earlier projects included a 16-bit II X, abandoned because the processor wasn't perfected, and the Mega II, a single-chip version of the Apple II, later adapted for use in the new machine.

An October 1984 sales meeting, at which Apple II projects took a back seat to the upcoming Macintosh, spurred strong protests from Apple cofounder Steve Wozniak. The result: a decision to proceed with a redesigned Apple II, code-named Cortland. "It was supposed to be an educational computer," says Dan Hillman, the IIGS's chief hardware designer. "But we all knew it would be more than that. This is a box that can be useful to anyone."

The project took off in December 1984 with a small team that eventually grew to 5 hardware specialists and about 20 software engineers. Among the leaders:

- Hillman, 39, the only team member with any experience in integrated-circuit design. In eight years at RCA and four at Zilog, he designed microprocessors and peripherals until, he says, "I got tired of ICs and wanted to get on the other side." Working on the Apple IIGS project, however, put Hillman right back in the IC world: the new machine includes six Apple-designed chips.
- Harvey Lehtman, 40, software engineering manager, a 12-year veteran of the original pre-personal-computer NLS project under Douglas Engelbart at SRI International. NLS was a pioneering multiuser version of the interactive format that has become common with personal computers.
- Moore, 37, a hardware designer at A. B. Dick Co. before joining Apple in August 1984 during a company reorganization. After several weeks of doing nothing, he says, "I went to Dan and told him 'I'm going to work for you.'" He eventually succeeded Hillman as chief hardware designer on the Cortland.
- Fern Bachman, designer of the software architecture and the mouse and AppleTalk cards for the Apple IIGS. A five-year Apple veteran, he came to the company from Measurex, where he worked on process control software.
- Eagle I. Berns, 45, a software engineer who taught computer science for 16 years at Stanford University and came to Apple last November after a brief stint at Atari. Berns has written graphics software for the Macintosh and games for the Apple II.

APPLE OF THEIR EYE. The Apple Computer Inc. team that spiffed up the Apple II for its next round includes, from left, Rob Moore, Eagle I. Berns, Dan Hillman, Fern Bachman, and Harvey Lehtman.

PROBING THE NEWS

CAN THE U.S. CONTINUE AS NO. 1 IN SPACE COMMUNICATIONS?

BUDGET CUTS SLOW SATELLITE AS EUROPEANS, JAPANESE GAIN

by Wesley R. Iversen

CLEVELAND

The Reagan Administration's decision to build a fourth space shuttle casts a shadow over another National Aeronautics and Space Administration program: the Advanced Communication Technology Satellite. As NASA reviews its budget to find $2.8 billion for the shuttle, a likely candidate for cutbacks is the nine-year-old space-communications program. And with Europe and Japan readying their own satellites for 1991-92 launching, further cuts in ACTS could imperil U.S. preeminence in space communications.

The $350-million ACTS project would launch several advanced technologies that have never been tested in space before. These include an on-board baseband processor for circuit switching in the sky and a scanning multibeam antenna system that could provide up to 10 times better frequency utilization than today's commercial satellites. An optical laser-communications experiment would also be the first space test of its kind; it holds high interest for military as well as commercial concerns.

"We really want to get it up there and test out these technologies prior to the Europeans and Japanese," says William T. Kondik, NASA's ACTS program manager in Washington.

Caught in the debate over the roles of government and the private sector in stimulating new space communications technology, ACTS has had a rocky history. Since its inception in 1977, it has been axed more than once by the Office of Management and Budget, only to be restored by Congress. "The ACTS program has led a *Perils of Pauline* existence, and there's really no reason to think that's going to change," says John Logsdon, director of the Science Policy Program at George Washington University in Washington. "Even though Congress keeps putting it back, it's highly likely that the OMB and the White House will keep trying to take it out."

Optimistic ACTS officials, though, believe the program will weather the latest storm. "We're feeling fairly comfortable that we're going to go," says William H. Hawersaat, deputy ACTS program manager at the NASA Lewis Research Center in Cleveland. The question now isn't whether ACTS will be funded, but at what rate. "We have already sunk about $165 million into the program, and we're at the top of the [funding] curve," says Kondik.

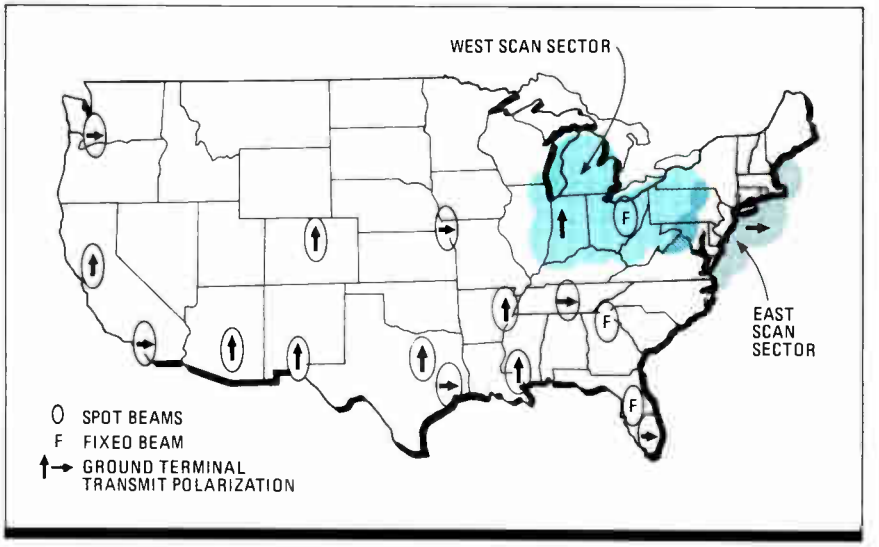
Recent congressional-committee action indicates that fiscal 1987 funding could come in "between $77 million and $95 million," says Richard T. Gedney, chief of the ACTS project office at NASA Lewis. That's less than the $119 million NASA requested to keep the program moving toward its scheduled launch date of September 1989. But the $95 million would be enough to ensure a May 1990 launch, Gedney says.

The timing could be critical. Both the European Space Agency and the Japanese are breathing down NASA's neck, warns Robert R. Lovell, communications division director at the agency's headquarters in Washington. "The Europeans will fly an experimental satellite that has all the capabilities of ACTS by midyear to the third quarter of 1991," Lovell says. And the Japanese are not far behind: they plan an ACTS-type satellite in 1992, NASA officials say.

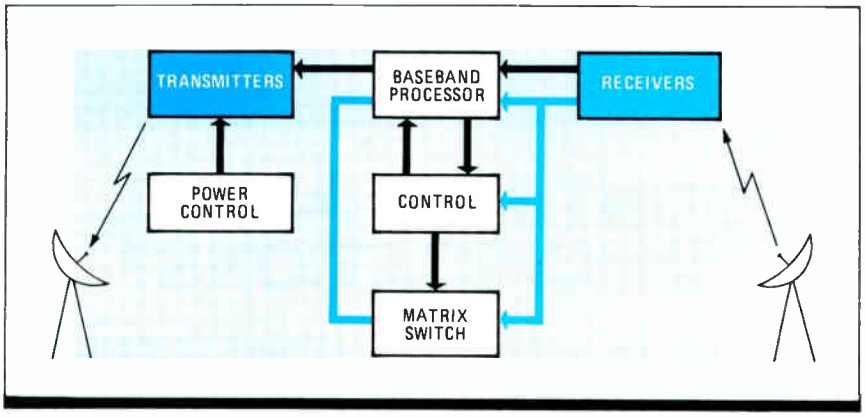
ACTS began as an experiment to test high-frequency K_a-band satellite communications technologies. NASA was looking toward the day when currently used lower-frequency C-band and K_u-band geostationary orbital slots will be saturated [*Electronics*, July 14, 1983, p. 97]. It sold the program on the grounds that it was too risky and costly an undertaking for any one company to attempt alone, a position strongly supported by industry.

INDUSTRY BACKERS. But ACTS opponents contend new technology development is the role of industry, not the government. Critics note, too, that since ACTS was conceived, growth in the satellite communications market has been eroded by the rapid expansion of terrestrial fiber-optic systems, raising questions about the near-term need for K_a-band satellites.

As now conceived, ACTS will provide the vehicle by which NASA—as well as potential carriers, users, and communications-equipment suppliers—can test the technologies for future satellite systems. Commercial users will perform their own experiments at their own ex-



TWO BEAM TYPES. Unlike fixed-beam satellites, ACTS will have movable and fixed beams.



HEAVY-DUTY SWITCHING. Space-based baseband processor will handle volumes of data.

pense—for example, testing K_a-band network schemes, modulation techniques, or ways to overcome the rain-fade problems expected on the higher-frequency 30/20-GHz K_a band. NASA has received about 100 responses to a notice sent out last year to assess interest, the agency's Gedney says. A meeting for potential participants will be held in Washington next week.

The program has also picked up increased military interest over the past year with the addition of an optical-laser-communications experiment to be performed under joint NASA-Air Force sponsorship. With Air Force funding, the Massachusetts Institute of Technology's Lincoln Laboratory is developing an optical pointing and tracking system and heterodyne transmitter to be flown on ACTS. At the same time, NASA's Goddard Space Flight Center in Greenbelt, Md., is developing a direct-detection receiver and transmitter that will also be aboard.

The laser experiment will test technology for future high-data-rate intersatellite links. Today's satellites talk to each other via microwave, typically at 30 to 85 Mb/s. But NASA studies show that future laser-based systems could support intersatellite links at speeds of 2 to 4 Gb/s, says Michael Fitzmaurice, head of the instrument electro-optics branch at Goddard. Because the pencil-thin laser beams are difficult to intercept, the technology offers the potential for highly secure links that could be used in military programs such as the Strategic Defense Initiative.

Unlike today's commercial satellites, which cover the continental U.S. or a portion of the country with a single, fixed microwave beam, the ACTS payload will feature a multiple microwave-spot-beam antenna system. The antenna and transponder package is being supplied by TRW Inc.'s Space Communications Division at Redondo Beach, Calif., for prime contractor RCA Astro-Electronics, a Princeton, N.J., division of RCA Corp. RCA is handling the ACTS bus and spacecraft system design and payload integration. Communications Satellite Corp. (Comsat), of Washington, will supply the ground equipment.

Operating at 30-GHz uplink and 20-GHz downlink, the TRW antenna system will include three fixed beams (see map, p. 95). These beams will be focused on Cleveland, where the ACTS master-control ground station will be located, and on Tampa, Fla., and Atlanta. Two additional scanning or hopping beams will provide contiguous-scanning coverage of a section of the northeastern U.S. and the Midwest, while also hopping to isolated spots in the South and West as traffic dictates. For contiguous-scan operation, the two beams will provide 0.3° spots that will dwell for 10 to 100 μs on areas 120 miles wide before being switched at a rate of 0.5 μs. To enhance isolation, adjacent beams on the ACTS will transmit and receive at different polarizations.

GEDNEY. ACTS could provide the equivalent of 5 to 10 times the channels available today.

By allowing frequency reuse on each beam, the ACTS multibeam system will provide the equivalent of 5 to 10 times the number of channels possible on today's satellites with their single, fixed beam, says NASA's Gedney. And more complex multibeam craft of the future based on ACTS technology could go well beyond that. Because of the improved frequency use, next-generation multibeam satellites could lower communications costs. And because the focused antenna beams concentrate energy in a spot, they will also make possible use of low-cost small-diameter earth terminals that can be located on customer sites. NASA recently issued a request for proposals for the development of experimental ACTS ground terminals with a range of capabilities, including a low-end dish that could be sold to ACTS experimenters for less than $50,000 each. The agency expects to award 6 to 10 contracts for that work by mid-1987.

CHANCY SWITCH. Although the multibeam antenna system will be far more complex than anything ever flown in space, the ACTS baseband processor is an even higher-risk technology, Gedney says. Literally a "switchboard in the sky," it will do what now can be accomplished only on the ground.

To be supplied by Motorola Inc.'s Government Electronics Group in Scottsdale, Ariz., the baseband processor will be "one fantastic piece of equipment if it does what it's supposed to do," observes T. J. (Jim) McKnight, who manages the spacecraft portion of ACTS for RCA Astro-Electronics. "It has got to handle one hell of a lot of data in a very short period of time, and the timing and synchronization have got to be exquisite," he says.

The baseband processor will feature numerous Motorola-designed custom logic circuits fabricated in emitter-coupled logic, current-mode logic, and CMOS at densities up to about 30,000 transistors, as well as 2-K-by-8-bit CMOS silicon-on-sapphire memory chips. The processor will be housed in three modules—modem, input/output memory, and central processor—and weigh 119 lb. It will convert incoming transmissions at intermediate frequency to baseband for temporary storage in what's called an input ping-pong memory. During the next frame, the messages will be processed and routed to an output ping-pong memory according to destination, and modulated back to IF before being sent to an upconverter prior to transmission.

On-board switching will allow low-cost small-aperture ground terminals to be used in "single hop" mode at customer sites, says Gedney. By contrast, today's VSAT (for very small-aperture terminal) ground stations require a double hop: data transmitted to a satellite must be transmitted back to a ground hub for switching, then retransmitted to the satellite for forwarding to the appropriate terrestrial destination.

The double-hop technique limits small-aperture ground terminals to data services only, because the 0.5-s delay

built into the double hop is unacceptable for voice or video traffic, Gedney explains. The ACTS technology, on the other hand, promises full-blown voice, video, and data communications using a single, inexpensive dish.

The dish is the 1.8-m Micro 1 terminal, which is easily mounted on a rooftop. It will handle up to 24 voice channels and at under $50,000 will be 5 to 10 times cheaper than the 5- to 7-m dish terminals required for single-hop operations today, he notes. Other ACTS experimental terminals will use larger dishes, which could cost up to $1 million apiece, for higher volume and faster data rates.

The ACTS baseband processor will handle transmissions in what NASA calls the low-burst-rate mode, at either 27.5 or 110 Mb/s. The slower speed will be used for adaptive fade compensation using a forward error-correcting code when receiving from or transmitting to a ground terminal that is being rained on, a condition the ACTS system will detect automatically. High-frequency

ACTS is designed to be launched by any vehicle that's assigned

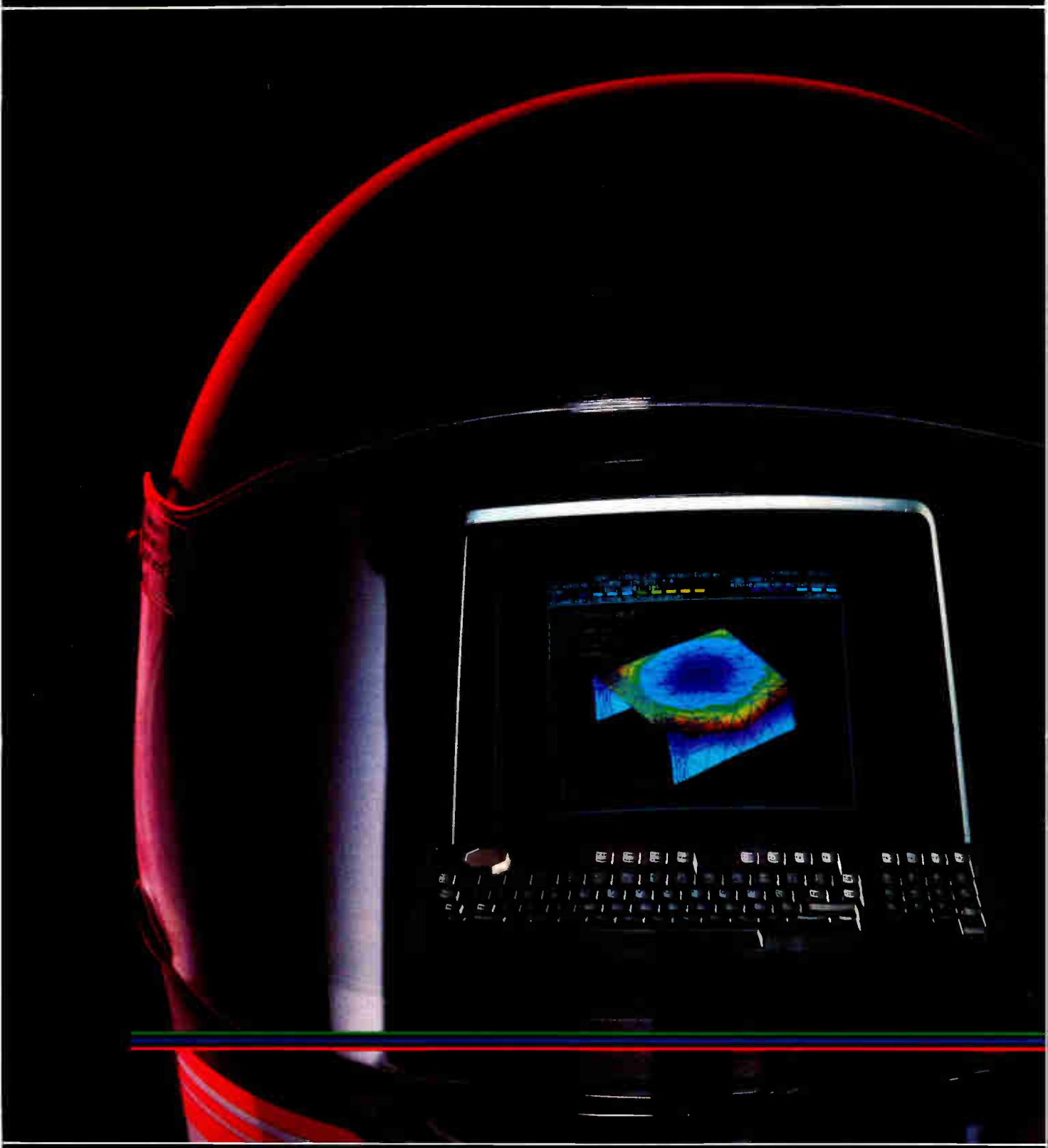
K_a-band satellite transmissions are expected to be much more susceptible to outages caused by rain than currently used 6-GHz/4-GHz C-band and 14-GHz/12-GHz K_u-band uplink- and downlink-frequency systems.

EYE ON 1990. Despite the uncertainties, ACTS contractors are steaming ahead with the project with an eye now toward a spring 1990 launch, says RCA's McKnight. Since the contract was signed in August 1984 for development of the ACTS flight experiment system, RCA and TRW have done significant hardware breadboard work and plan to begin developing the actual flight hardware next year.

The payload package is scheduled for delivery in mid-1988, McKnight says. Comsat is in the early design stages of the ground-control system and, depending on funding, will deliver hardware to RCA in 1989 or 1990.

McKnight notes that the loss of the space shuttle Challenger has meant a more complex design for the ACTS spacecraft, which was originally scheduled to be launched via shuttle. That decision is now on hold.

"The structure design [for ACTS] has got to be compatible with whatever launch vehicle we end up with," McKnight explains. "We're OK for now, but we'll have to know soon. We have asked for a resolution [of the launch-vehicle question] by the end of the year." □



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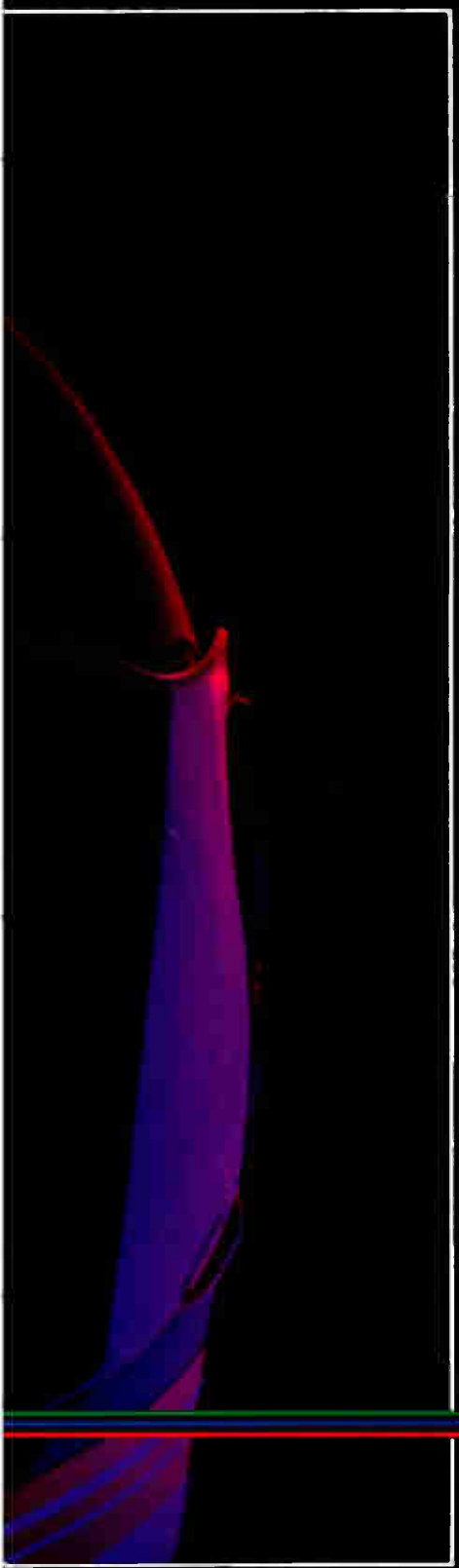

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NEW PRODUCTS

DSP IC STORES ROUTINES IN RAM TO ACCELERATE DEVELOPMENT

MOTOROLA'S 24-BIT SIGNAL-PROCESSOR VARIANT ALSO LOWERS COSTS

by J. Robert Lineback

A new 24-bit digital signal processor that runs from routines stored in random-access memory is on its way from Motorola Inc. The 56001 will slip onto the market in the first quarter of 1987, just ahead of a previously announced DSP chip using routines frozen in read-only memory, the 56000 [*Electronics*, March 10, 1986, p. 30]. The RAM-based part is useful for system development, and for getting users onboard rapidly, avoiding the time and expense incurred in getting ROM-based versions in production.

The 56001 contains a 512-by-24-bit array of random-access memory for DSP programs, which may be downloaded quickly from off-chip storage. "As we've coded up more applications, it has become quite clear that 512 words of program RAM for most DSP applications is efficient," notes Bryant Wilder, manager of Motorola's Digital Signal Processor Operation in Austin, Texas.

The 512-word program RAM resides in essentially the same die area as the 2-K by 24 bits of masked ROM found on the 56000. With the exception of some added DSP algorithms and logic for writing programs into the RAM, the 56001 and 56000 are similar, according to Wilder.

EASIER ENTRY. The 56001 processor is being brought to market first in hopes of getting customers to use Motorola's signal-processor offering quickly—without facing the hurdles normally associated with masked ROM. Usually, ROM-based processors involve longer development times because programs must be set in silicon. Customers buying ROM-based parts also incur a mask charge, which averages about $5,000.

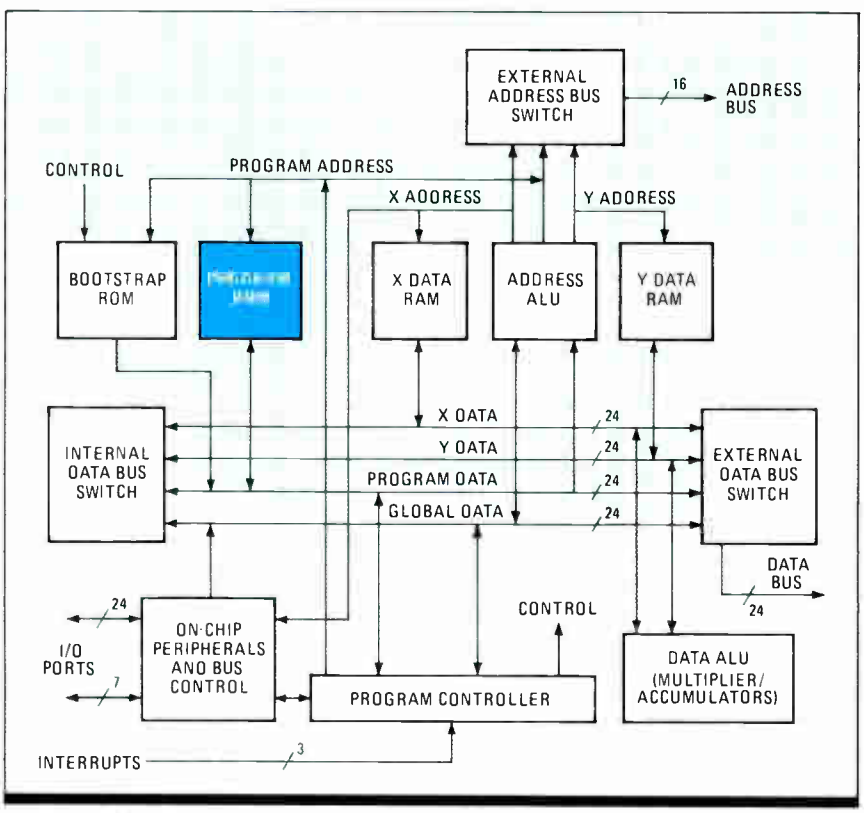
But DSP programs do not have to be fixed into the 56001, and product managers believe the RAM-based DSP will be better suited for system prototyping, small-volume purchases, and distributor-sales channels.

The 56001 can use software overlays so that a system can swap new program code into the RAM quickly. The programs stored on the chip can be totally replaced in 1.5 ms. The chip can also selectively overlay one word of new code into RAM. The overlay feature is aimed at applications needing programs of more than 512 words or jobs that make it necessary to change out sections of program on the fly.

TWO WRITING MODES. The program RAM may be written to in two modes. In the first, programs can be downloaded by another processor using the chip's host interface. In the second, code from byte-wide PROMs may be sent to the RAM via the 56001's data-bus port.

Like the 56000, the 56001 will perform 10.25 million instructions/s at a maximum clock rate of 20.5 MHz. Both general-purpose DSPs have identical processing cores, consisting of three parallel-processing execution units. The arithmetic-logic unit for data, the address ALU, and the program controller can all operate concurrently within their own independent memory spaces.

The 56001 is fitted with two independent 256-by-24-bit data-RAM spaces, like the 56000. But the 56001 will contain preprogrammed coefficients in data ROM. In one block of 256 data-ROM words, Motorola is loading positive A-law and μ-law values, which are applicable in many telecommunications applications as expansion tables. In a second chunk of 256 data-ROM words, the chip carries a sine-wave table, which can be used in waveform generation for fast Fourier transforms. Another 32-word block of ROM holds the chip's bootstrap program, which the 56001 uses when downloading programs into its RAM.



DEVELOPMENT VEHICLE. The first member of Motorola's 56000 DSP family will be the 56001, whose program RAM makes it suitable for development work and small-volume purchases.

The 56001, like the 56000, will be housed in an 88-pin grid array. Both are going to be built with the same CMOS process, which will have minimum features between 1.25 and 1.5 μm.

The 56001, samples of which will be available in the first quarter of 1987, "will be the first part in silicon," says Wilder, referring to Motorola's emerging family of general-purpose DSP chips. "Customers have been telling us they first want RAM-based [DSPs] more than ROM or EPROM."

Motorola's DSP software, which the company is shipping to customers for 56000 development, can be used to develop 56001-based systems. The recently released Version 1.1 of the development package [*Electronics*, Aug. 21, 1986, p. 26] has a mode for developing 56001-based systems. Development software that runs on IBM Personal Computers and compatibles costs $295; for engineering work stations and multiuser minicomputers, $3,000.

In sample quantities, the 56001 will cost $500 each. Volume deliveries are slated to commence in the second half of 1987.

Motorola Inc., Digital Signal Processor Operation, 6501 William Cannon West, Austin, Texas 78735. Phone (512) 440-2030 [Circle reader service number 360]

NOW AN AT SYSTEM BOARD FITS ON A PLUG-IN CARD

Chips and Technologies Inc. has completed its transmutation of the IBM PC AT with the introduction of a peripherals controller chip that integrates most of the logic missed in the firm's initial five-chip set. That set replaced 63 of the AT's 93 components; the new 82C206 replaces all the remaining controllers but the keyboard controller.

The new chip allows a 27-chip implementation of the AT system board, small enough to fit on a plug-in card. Two 8237A direct-memory-access controllers, two 8259A interrupt controllers, an 8254 timer/counter, a 74LS612 memory mapper, and a 146818 real-time clock, plus six small- and medium-scale integration chips, are included in the new peripheral controller. The company says its chip set extends the role of the AT into industrial applications and transaction processing, where it can be a single component of a system. A board-level AT will dissipate only 15 W, it says, one-third the power of the AT motherboard.

The new chip gives the company VLSI products in logic (the original five-piece CS8220), graphics display (an IBM Extended Graphics Adapter chip), local-area networks (a StarLAN chipset), and controllers (the 82C206). The original chip set has been used in PCs built by Tandy, Nippon Electric, PCs Limited, and Apricot Computer; but Chips and Technologies expects the new chip to open new markets.

A board-level AT could control any kind of automation process, and at the same time manage mass storage and interface with add-on cards and standard software packages. Chips and Technologies will now focus on buses, operating systems, languages, linkers, and loaders, says product marketing director Sikander Naqvi.

To support this market, the company also supplies a development kit, the DK8220, which includes the six AT chips and 512-K bytes of memory. The board provides 26 test points and light-emitting-diode diagnostic readouts.

The CMOS 82C206 chip is the first developed with Chips and Technologies' own computer-aided engineering tools. Based on an Amdahl 470 mainframe and run from AT-based workstations, the tools resulted in a chip area less than 290 mm², versus 420 mm² in designs made with standard CAE tools.

The controller operates at 10 MHz, with 8 MHz DMA, compared with 8 and 5 MHz, respectively, for a standard AT; the chip is priced at $49 in quantities of 100. The accompanying 5-chip CS8220 is also $51 in hundreds. A single development board costs $1,495. Both chip and board will be sampled this month, with volume production slated for the first quarter of next year.

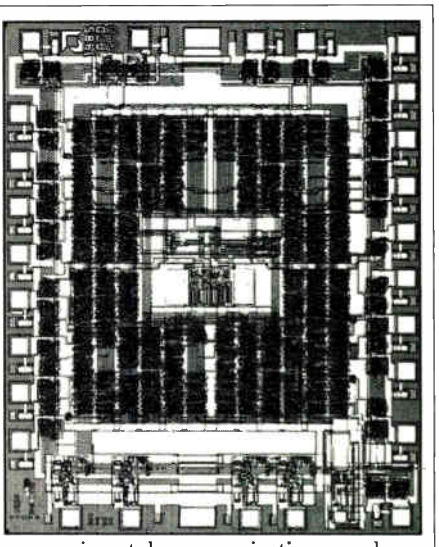
Chips and Technologies Inc., 521 Cottonwood Drive, Milpitas, Calif. 95035. Phone (408) 434-0600 [Circle 361]

BOUNDS CHECKER BOOSTS THROUGHPUT

By helping to set task priorities, comparing data against available memory space and checking for potential overflows, a 16-bit bipolar bounds checker enhances throughput for systems built with Advanced Micro Devices' 16- and 32-bit Am29300-family microprocessors.

Besides its limit registers, the Am29337 also integrates two 8-bit comparators to enhance power and propagation characteristics. It supports 80-ns system cycles when used with other members of the Am29300 family.

The Am29337 has applications in superminicomputers, graphics, digital signal processing, telecommunications, and peripheral controllers.



Available now in a 28-pin ceramic DIP, the device is priced at $22 each in 100-unit quantities. It is also available in plastic leaded chip carriers and leadless chip carriers.

Advanced Micro Devices Inc., 901 Thompson Place, P. O. Box 3453, Sunnyvale, Calif. 94088. Phone (408) 732-2400 [Circle 366]

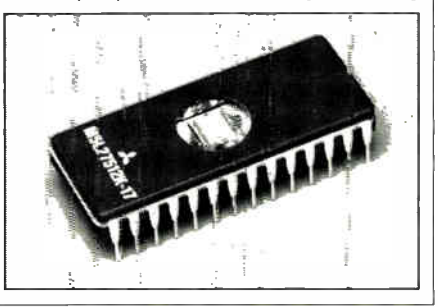
FAST PROGRAMMING FOR A 512-K EPROM

Easy upgrading and fast programming are featured in a 64-K-by-8-bit addition to Mitsubishi's n-MOS EPROM line. The 512-K MSL27512K comes in 170-, 200-, and 250-ns versions and has a power-down feature that cuts operating current from 100 mA to 40 mA in standby.

All Mitsubishi n-MOS EPROM products conform to JEDEC 28-pin standards, making it easy to upgrade from 64-K to 512-K as memory requirements increase. Fabricated with double-polysilicon floating-gate technology, the MSL27512K also features a fast programming algorithm and a programming voltage of 12.5 V. All inputs and outputs are TTL-compatible in read and program modes.

Available now in sample lots, the 250-ns version is priced at $29 each in 100-piece quantities.

Mitsubishi Electronics America Inc., 1050 East Arques Ave., Sunnyvale, Calif. 94086. Phone (408) 730-5900 [Circle 367]



SOFTWARE PROTECTOR FINGERPRINTS DISKS

EVERLOCK USES PATTERN OF SPURIOUS BITS BETWEEN TRACKS TO THWART UNAUTHORIZED COPYING

Software developers can protect programs from unauthorized copying with Everlock, a new package from Az-Tech Software Inc. that uses spurious bits on product disks to create identifying "fingerprints."

Everlock also addresses other common complaints about copy-protector packages, such as the need for passwords, the inability to create adequate backup copies, and the nonportability of protected application programs to machines that are software-compatible, says president Bill J. Lewis.

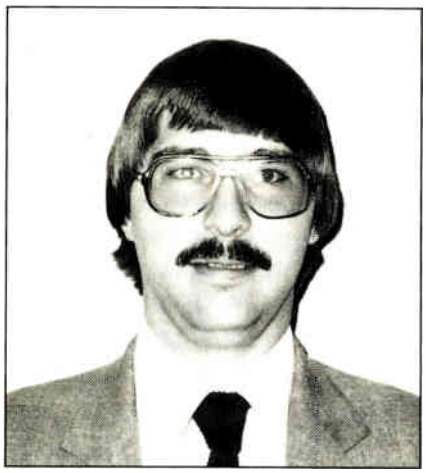
The system supports application programs written to run under PC-DOS Versions 2 through 3.2 and the corresponding MS-DOS operating systems. Except for about a 1- or 2-s longer disk loading time, Everlock is completely transparent to the software end user, Lewis says.

Everlock works at the machine-code level, breaking down machine-readable modules in a program, inserting Everlock code, and then reassembling the modules into a DOS-readable format.

Lewis contends that Everlock cannot be foiled by the current generation of bit-copier programs designed to beat copy-protection schemes. Bit copiers work by simply copying ones and zeros on a disk, even if they are encrypted or intentionally formatted improperly by a copy-protection system. Everlock frustrates that tactic by using the random and spurious bits between the disk's tracks and sectors to create a unique "fingerprint" for each individual disk. Though some bit copiers can read these random bits, none can reproduce them reliably, Lewis says.

In its protection mode, Everlock signals the floppy-disk head to check for signature bits between the tracks and sectors on product disks. If these bits don't match the original, the system knows the disk is an unauthorized copy and acts according to options specified by the software developer. The developer might choose, for example, to have the system display an explanatory message on the user's screen and then return to DOS. But in no case does Everlock enable the developer to specify that data be destroyed in the end user's computer system, as some controversial copy-protection systems have done in the past, Lewis says.

Because Everlock does not use an encrypted master, developers write application programs unencumbered by copy protection concerns. Protection is applied to the finished products using an IBM Personal Computer or compatible.



LOCKSMITH. Everlock copy protection is transparent to the end user, says Lewis.

The developer loads Everlock from its 5¼- or 3½-in. floppy disk. Unprotected product disks are inserted one or two at a time. The system requires 10 to 50 seconds per disk or pair of disks to apply the protection code. Everlock allows the developer to specify as many as 99 backup copies before the protective code is invoked.

Priced at $495, Everlock can be used an unlimited number of times. "For $500, most of our competitors would limit you to protecting about 50 to 75" disks, Lewis says.

Unlike most other copy protectors, Everlock is designed for both network and stand-alone systems and can also protect multitasking software applications. It works with hard disks as well as floppy disks.

Everlock can dynamically configure itself to talk directly to the floppy-disk controller in the appropriate protocol used by the user's host machine. This feature helps do away with compatibility problems when a user upgrades a machine or goes to a different model. By contrast, most competing copy-protection schemes rely on device-dependent code for various clones and even different models of IBM machines, Lewis says.

ENCRYPTED. Despite the advantages, Lewis concedes that Everlock, like any other copy-protection scheme, could be broken by a sophisticated computer user intent on branching around the protection checks. "Any software system is susceptible to a patch approach," says Lewis. "But we've gone to some unbelievable measures to protect against that. We've encrypted the program, so people are going to get garbled code. And if someone goes in with Debug or a similar tool, he's going to be foiled by various traps."

Lewis says experience shows that the lifetime of a copy-protection program is typically about three to four months, and concedes Everlock will likely be no exception. "The thing we sell is that we're going to be able to protect you from a very high percentage of illegal copying, maybe 95%," he says.

Az-Tek plans to release upgrades of Everlock about every three months, Lewis says. These versions will not differ in the system's reliance on unique "fingerprint" data from each individual product disk. But they will employ differing techniques to foil a patch approach. Buyers of the $495 Everlock system will get six months' worth of free upgrades. Another $45 puts a user's name on the upgrade list for three more months. *–Wesley R. Iversen*

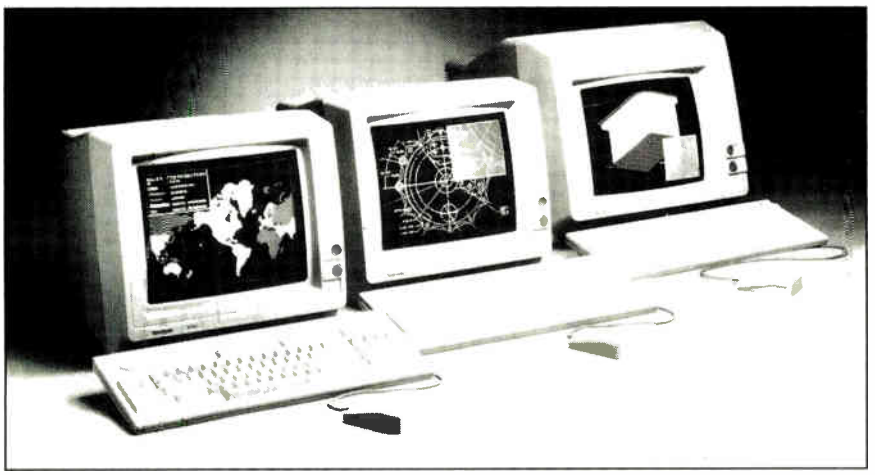
Az-Tech Software Inc., 426 Grandview, Richmond, Mo. 64085.
Phone (816) 776-8153 [Circle 340]

TEK GRAPHICS TERMINALS DO MORE FOR MUCH LESS

A 40% to 65% drop in price combined with an increase in functionality marks Tektronix's replacement of several members of its 4100-series intelligent color graphics terminals with the new generation of the 4200 series. Through the application of higher levels of integration and other cost reductions, market leader Tektronix has moved to head off several vendors of Tektronix look-alike terminals.

The closest comparison between members of the old and the new lines, says Tektronix program manager Donald Hershiser, is between the 4107 and the 4207. Similar in display resolution and feature set, they differ in single-quantity price by $3,000—the 4107 was priced at $6,995, and the 4207 goes for $3,995.

This price differential, along with the



CLONE-STOPPER. New series of Tektronix graphics terminals shows striking price reductions.

company's commitment to compatibility with earlier terminals, make the new terminals very attractive to users of software written for the 4100-series hardware. But Tektronix has also been able to add features.

For example, the 4205, 4207, and 4208 offer a copy-spooling feature that eliminates the waiting time that users of the last-generation models had to put up with while an image was being printed. There is now an optional mouse, which a beta-site user who is producing systems for architectural design and facilities management singles out as the line's most important new feature.

Furthermore, the terminals' capabilities in an IBM 3270 environment have been enhanced, bringing them in line with IBM's Distributed Function Terminal features. These capabilities make it possible to carry on more than one terminal-to-host session simultaneously and to provide alphanumeric emulation of IBM's 3179 terminals. In addition, the 4200-series terminals, already capable of emulating Digital Equipment Corp. VT-100 terminals, will be made optionally capable of VT-220 emulation by May of next year.

"I believe the Tektronix strategy was to strike out at the Tek clones," says Barry Lewine, a software engineer at Sierra Geophysics Inc., Seattle, who has been involved in beta testing the new terminals. The 4200-series products are smaller, lighter, and ergonomically superior to their predecessors, he says, but "the biggest thing was the price reduction. All of a sudden the Tek series is very attractively priced."

"Tek aims to build its lead to 25% of the market or better," says Hershiser. The new entry-level terminal is the 4205, which at a quantity-one price of $2,495 offers a resolution of 480 by 360 pixels. It has 128-K bytes of local memory and can display 16 colors from a palette of 64 on a 13-in. screen refreshed at 60 Hz, noninterlaced.

The 4207 has a 640-by-480-pixel resolution and 256-K bytes of memory. The 4208, at $4,995, has the same resolution but pushes memory to 512-K bytes and offers a red-green-blue video output for driving an auxiliary monitor useful in, for example, classroom situations. The 4207 and 4208 also support the use of a Hewlett-Packard LaserJet printer for graphic output.

Application-specific integrated circuits played a large part in the price reduction. "We took about 75 ICs and put them in three [1.5-μm CMOS] gate arrays," says Hershiser. Three printed-circuit boards in the 4107 were reduced to a single board in the 4207, and the company was able to consolidate to a single power supply. Total component count was about 700 for the 4107, says Hershiser; it is less than 400 in the 4207.

The terminals will be used in typical scientific and engineering applications such as computer-aided design, drafting, and data analysis. Hershiser also expects them to see increasing use on factory floors, where their pan and zoom capabilities will allow shop personnel to scan the details of technical drawings.

The 4208 is available now. The 4205 and 4207 will be available Nov. 15.

–Jeremy Young

Tektronix Inc., Information Display Group, P. O. Box 1000, Wilsonville, Ore. 97070. Phone (800) 547-1512 [Circle 341]

5¼-IN. DRIVE STORES A FULL 765 MEGABYTES

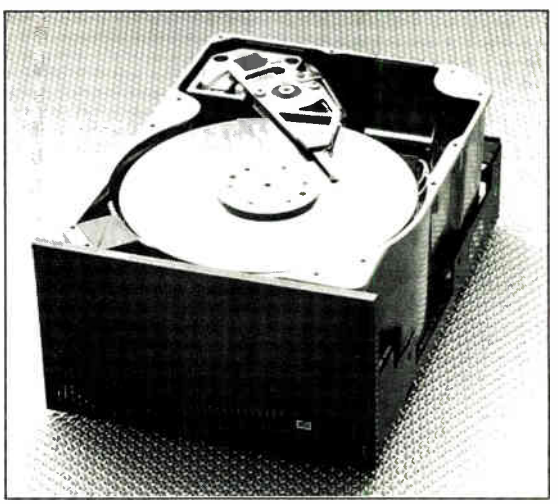
Offering up to 765 megabytes of unformatted storage, Maxtor's EXT-8000 family of Winchester disk drives are the highest-capacity 5¼-in. units yet—a bad omen for larger Winchesters. In addition, the drives set a new performance standard for 5¼-in. drives.

The lower-capacity, 408-megabyte EXT8000 models have a 16-ms average access time, compared with the previous 25-ms pacesetter. High-capacity units offer 18 ms, equaling the performance of 10-in. Eagle Winchesters from Fujitsu America Inc., San Jose, Calif., and 14-in. 3380 Winchesters from the San Jose, Calif. division of IBM Corp.

To achieve a low average access time and high track density, Maxtor uses an innovative microprocessor-controlled adaptive track-positioning system that changes the acceleration and deceleration profiles for each change in track position. In addition, a balanced actuator keeps the mass that must be moved to a minimum.

Maxtor offers the extended small device interface (ESDI), on the initial release of the product, with the small computer system interface (SCSI) version to come later. With either interface, the smaller unit competes with larger drives' data-transfer rates. Until now, 5¼-in. drives offered top rates of 7.5 Mb/s. Larger drives such as Fujitsu's offered transfer rates of up to 24 Mb/s using a modified version of the industry-standard storage module drive (SMD) interface.

Using ESDI or SCSI, Maxtor now offers a 15-Mb/s rate, which makes it cost-effective competition against the big drives for work-station and minicomputer applications. Moreover, the smaller drives have an extra advantage, be-



LITTLE BIG DRIVE. Maxtor's latest 5¼-in. drive stores 51 megabytes on each of 15 surfaces and accesses in 18 ms.

cause ESDI and SCSI interfaces are less expensive to implement than the SMD interface.

Since the spindle motors of several drives can be synchronized, customers are exploring the possibility of using drives in parallel, according to drive-family marketing manager John Klonick. By treating eight units as a single, byte-wide memory, it is possible to store 6 gigabytes of data and achieve a transfer rate of 15 megabytes/s, all for a price under $50,000.

To double storage capacity per surface, Klonick says the company increased track density to 1,632 from 1,224—a 33% increase. Bit density was also pushed up 41%, from 14,873 to 20,953 b/in.

Both the 408-megabyte XT-8380E and the 765-megabyte XT-8760E will sell for between $4 and $5 per megabyte, the company says. The drives will be demonstrated at the Comdex Show in November in Las Vegas, Nev. Evaluation units are available immediately, and production units will be available in the first quarter of 1987. *–Jonah McLeod*

Maxtor Corp., 150 River Oaks Parkway, San Jose, Calif. 95134.
Phone (408) 942-1700 [Circle 342]

VISUAL PACKAGE SPEEDS PROGRAMMING

Cortex Corp.'s graphical programming package lets software developers working in the Digital Equipment Corp. VAX/VMS environment cut development time by using picture-based programming instead of conventional techniques. CorVision's graphical mode extends such user-friendly devices as mouse capability, pop-up menu windows, and icons right through implementation and maintenance.

On any work station compatible with the IBM Corp. Personal Computer AT, a designer can diagram a complete application, including fields in the data dictionary, file structures, menus, screens, and reports. An action diagrammer and very high-level language are used to customize logic for each application.

The package also offers an intelligent guidance system that recommends the next logical step in the design process and keeps track of incomplete specifications.

After the design phase, CorVision generates the complete production-ready application for the VAX, which executes in optimized machine code.

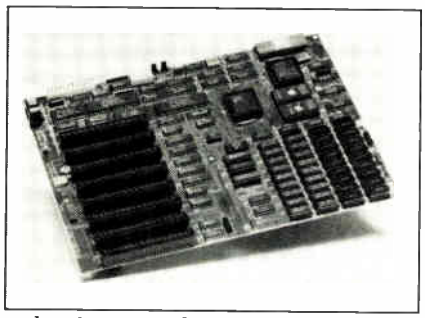
CorVision will be available in the first quarter of 1987 for $50,000 to $175,000, depending on the VAX model.

Cortex Corp., 128 Technology Center, 128 Roberts Rd., Waltham, Mass. 02254.
Phone (617) 894-7000 [Circle 345]

XT-COMPATIBLE CARD RUNS AT 12.5 MHz

By eliminating the normal wait states that slow up IBM Corp. PC/XTs, an upgraded version of a popular motherboard runs standard software up to 15.3 times faster than the IBM original.

The Bullet-286ii reaches higher speeds by avoiding the need to slow down to achieve compatibility between the hardware and software. It does this by emulating the 8088 chip in both hardware



and software and by synchronizing the 80286 chip's high-speed clock with the standard clock of the PC/XT's expansion bus.

Available with clock speeds of 8, 10, or 12.5 MHz, Bullet-286ii is aimed at builders of new systems for graphics, CAD/CAM, networks, file servers, and multiuser applications.

Virtually all IBM PC/XT add-in cards and software run on the board. Available now, the boards cost as little as $300 each in volume.

Wavemate Inc., 2341 205th St., Torrance, Calif. 90501.
Phone (213) 533-8190 [Circle 346]

DEC-COMPATIBLE TERMINAL UPGRADED

Additional function keys, double-high characters, and a keyboard layout compatible with the Digital Equipment Corp. DEC VT-220 terminal are among the offerings in Advanced Digital Systems Inc.'s model 3220 terminal.

By combining the styling of its ADDS

2020 terminal with the functionality of its initial entry in the DEC-compatible market, the Viewpoint/122, ADDS engineered in better ergonomics. It also added six more function keys than DEC offers—for a total of 22. They're programmable from keyboard or host and functional in the DEC 220, 100, and 52 modes and when using the ANSI X3.64 command set.

Priced at $695 and available now, the ADDS 3220 has a 14-in. flat-face CRT available in green, amber, or white and a 70-Hz refresh rate to eliminate flicker.

ADDS Display Products Division, 100 Marcus Blvd., Hauppauge, N. Y. 11788.
Phone (516) 231-5400 [Circle 351]

OPAL GRAPHICS BOOSTS RESOLUTION

Ultrahigh-resolution monochrome graphics has been added to Europel Systems Ltd.'s Opal series of VMEbus graphics controllers. With the new map-one option, displays can be configured to virtually any resolution up to 4,096 by 2,048 pixels at video signal rates in excess of 160 MHz.

A software-programmable anti-aliasing circuit reduces the bandwidth requirement of display monitors to between 40 and 80 MHz to provide a flicker-free, noninterlaced, 60-Hz display at 1,800 by 1,400 pixels without using a long-persistence phosphor.

Packaged on a single standard-depth, double-height VMEbus Eurocard, the SS180 board has the map-one option available in three memory sizes: 128-K bytes, 512-K bytes, and 2 megabytes. Available now, the option is priced at £3,400 in the 2-megabyte board.

Europel Systems (Electronics) Ltd., Craven House, Craven Road, Newbury, Berkshire RG14 5NE, England.
Phone 44 635 31047 [Circle 349]

NEW WORK STATION OFFERS 1-s REPAINT

Capable of repainting an AutoCAD screen in less than 1 s, a new entry in the work-station market offers 1,280-by-1,024-pixel resolution as well. The MicroDirect 286/CAE is fully compatible with software for the IBM Corp. Personal Computer PC AT and has been independently tested for its ability to run several popular software packages.

The work-station package, priced at $10,886, includes 1 megabyte of high-speed RAM on board; a 30-megabyte self-parking voice-coil hard-disk drive; 1.2-megabyte floppy disk; Pixelworks Clipper graphics card; Hitachi CM2073A color monitor; and one-year warranty.

MicroDirect Inc., 180 Bent St., Cambridge, Mass. 02141.
Phone (617) 345-5800 [Circle 347]

ATE SYSTEM TESTS AT FULL CLOCK SPEED

FUNCTIONAL TESTING AT FULL SPEED ELIMINATES A SECOND SERIES OF SYSTEM TESTS

Besides costing $300,000 or more, functional board-test systems have another drawback: by testing nodes at less than full clock speed, they cannot catch timing problems, and that means another series of system tests must be run later.

A new in-circuit functional tester, Support Technologies Inc. model 3100, not only cuts purchase cost by a factor of almost 10, but also enables functional testing at the board's full speed. It tests microprocessor-based printed circuit cards with a software-selectable emulation-system technique. But instead of using the common method of replacing the microprocessor with an emulator, the tester probe is inserted in place of the EPROM, ROM, or PROM. By replacing the program memory, the tester gains control over the microprocessor.

The test-system software contains a control program that downloads target routines that stimulate certain parts of the printed-circuit board's normal operation. For example, it might load a routine that causes data to be transmitted and received via the board's on-board RS-232-C or Small Computer Systems Interface input/output port. The tester would then check the circuit's operation. If a fault occurred, it could then be isolated, leaving it to the human operator to probe backward from the faulty node to find the trouble. Or a programmer could program the trouble diagnostic "walkback" process into the tester for production-line use where operators are less experienced. A future version with upgraded software will tell the technician where to probe.

TRIPLE THREAT. The tester contains three modules: an emulator system, a measurement system, and a pin system. Each is contained on circuit modules that slide into one of up to 10 slots in the tester mainframe. The first unit emulates the microprocessor via the ROM sockets. There can be several emulator modules inside the mainframe at once. Each can concurrently emulate up to two microprocessors with 16-bit-wide data paths. If the board under test has more than two microprocessors, the system can be configured with a second or third emulator module to test all the microprocessors simultaneously. This capability is useful in boards where two or more slave processors control I/O operations under direction of a master, because processor coordination is necessary for system testing.

The measurement module provides the system's instrumentation in two 100-MHz variable-threshold input channels. Each can handle voltage swings between ±20 V. The two can be configured three ways. Both can operate to measure asynchronously occurring events. The two can be strung together as a single channel with two thresholds to measure the characteristics of a single waveform, such as rise and fall times and noise. Finally, both channels can operate synchronously, with one used for clock and the second for input data. The former can serve as a qualifier for the latter to look at data moving on a bus over a serial input link, for example.

FLEXIBLE. Model 3100 in-circuit tester uses a software-selectable emulation technique and costs only $35,000.

The measurement system provides 100-MHz sampling that can measure asynchronous events occurring at a 40-MHz clock rate. That rate can measure even high-frequency clock pulses used to time microprocessor-based systems.

Instead of continuously filling the capture memory with the most recently occurring events in the circuit being monitored, the measurement system's logic analyzer can selectively sample the circuit and only record when activity occurs in the circuit. If the system is measuring the activity of an RS-232-C I/O port, the logic analyzer will record only when data is on the line, not when the line is idle and waiting for data to be received. Besides the logic analyzer, the measurement system also contains a frequency counter, period counter, and digital voltmeter. These can be used to measure signal levels coming into the measurement unit.

The third module in the tester is the pin-system module, which controls the operation of a bed-of-nails test fixture. Most testers with bed-of-nails probes are intended to probe every node in a printed circuit board being tested. By contrast, the bed-of-nails system in the 3100 probes only those pins that connect to a bus on-board the pc board or to pins that go to a bus off the board. The pin system in the bed-of-nails has comparators across all the pins. The comparators selectively switch on the fly to check every output from the bus. The pin system can imitate the bus protocol using the pin drivers and check for proper response using the pin comparators.

The Model 3100 Performance Test System is priced at $35,000 with the bed-of-nails fixture. Emulator modules for 8-bit microprocessors sell for $300; those for 16-bit units sell for $500, and for 32-bit processors $700. *–Jonah McLeod*

Support Technologies Inc., 7405 S.W. Tech Center Dr., Portland, Ore. 97223. Phone (503) 620-3554 [Circle 380]

ASIC TOOL CAN HANDLE MACROS, STANDARD CELLS

One goal of silicon compilation is to enable a system engineer inexperienced in application-specific integrated circuit design to enter a schematic into a work station and have the system take over—automatically compile the macro blocks (counters, registers, and so on), and place and route the compiled blocks among the standard cells used to connect the larger blocks. Until now, none of the ASIC layout tools could automatically place macro blocks and standard cells, though many could make a suggested placement, which the designer would often have to change. Moreover, router tools could route no more than 10

COMPAQ® creates the with a business

The new COMPAQ DESKPRO 386™ is the first *complete* high-performance PC CAD/CAE solution that single-handedly runs all the popular engineering *and* business software. It offers versatility without compromise. Each and every component far surpasses the limits of previous "advanced technology" PCs. From its superior microprocessor to its exceptional memory capacity to its greater storage to its monitor all the way to its faster disk drives, it is the most advanced personal computer in the world.

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The COMPAQ DESKPRO 386 sports the fastest 40-, 70- and 130-Megabyte internal fixed disk drives in the industry so you can access data two times faster than other advanced-technology PCs.

Watch the performance on the new COMPAQ Color Monitor for enhanced text and graphics resolution. Displaying 16 colors at once from a palette of 64, it comes with the COMPAQ Enhanced Color Graphics Board.

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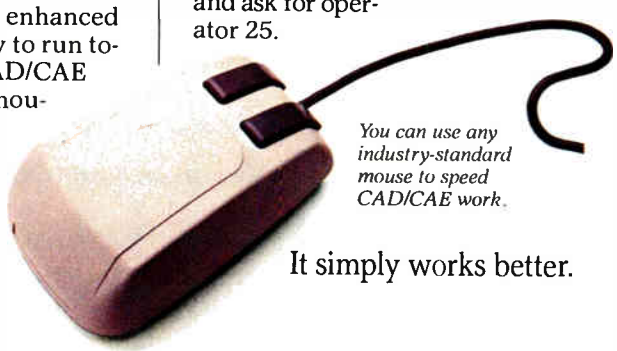

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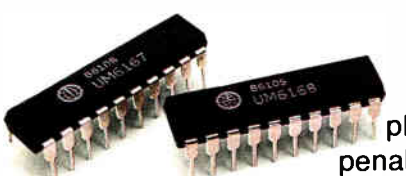
COMPAQ DESKPRO 386™

Score A Winning Touchdown with UMC

With backing from UNITED MICROELECTRONICS CORPORATION, one of our customers scored a winning touchdown with a voice control IC last year. He netted a profit of 2.5 million dollars on just one product. This is one of the many examples of how UMC helps its customers score financial goals.



UMC scored its first touchdown by becoming profitable 6 months after it went into operation and has been making a profit and registering phenomenal sales growth annually since then. Last year, 4 quarters of penalties left most companies sitting on the bench and several others were ejected from the game. UMC, however, still romped to a sales growth rate of 24.4%, which was the fourth best in the world and outscored 92% of the IC industry.

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to 20 macro blocks among a larger number of standard cells.

That situation has changed with the release of Version 4.0 of the Concorde Silicon Compilation Tools package. Significant revisions in this release include a new version of the Concorde placement tool that automatically places large numbers of macro blocks and standard cells. The only limitation to the number of macro blocks possible is the amount of computer memory and processing power. Seattle Silicon Technologies Inc. has successfully placed and routed 50 macro blocks on a standard-cell array.

In addition, the company has improved the router tool to handle two-layer metal, improving density over the previous version of the software. The router is guaranteed to provide a 100% route of any ASIC design.

OVERRIDE OPTION. The placement chosen by the system is most often the best arrangement possible. But the designer can override the unit and reposition blocks to reduce wire lengths or to evaluate other alternatives in a "what-if" analysis. "In the next few years, the placement algorithm will get so much better than manual placement that even the most experienced layout designer will not be able to improve on it," says Warren Snapp, vice president of engineering at Seattle Silicon. For small chips, the place-and-route tool executes in a few minutes.

Besides the placement algorithm, the router has been optimized for dual-layer-metal semiconductor processing. One improvement was to enable the placement tool to handle the cell routing. Previously, one metal layer was used entirely to wire circuits within a standard cell or macro block, while the second layer was used to wire between these elements via routing channels.

With the new software, instead of wiring a cell into a routing channel and into another cell, a connection can be run "over a cell" from one cell to another in the layer previously used to wire within the cells. With this "over-the-cell" routing, there is less need to have dedicated routing channels.

The routing algorithm has been changed to reduce the spacing between blocks. The company estimates that this compaction improves layout density by 20% over the previous generation of software. Plans are under way to change the router again to handle three-layer metal, which should improve density over the two-layer-metal technique but will fall short of the 20% gain that two-layer metal routing achieves over single-layer designs.

Besides the improved place-and-route tools, The Concorde software now provides power, circuit-size, and performance-data feedback to the designer at different stages in the process of design, schematic capture, and simulation. This allows the designer to explore at a high level how much power and space a given design will require and how much performance it can provide.

In addition, the tools have been enhanced to allow foreign modules—cells from a cell library—to be entered into a design containing compiled macro blocks and standard cells. Once the foreign module has been entered, it can be manipulated like any other block or cell.

Beta-site shipments of Version 4.0 of the Concorde Silicon Compilation Tools have begun. Full release is scheduled for Dec. 30. *–Jonah McLeod*

Seattle Silicon Technologies Inc., 12356 Northup Way, Bellevue, Wash. 98005.
Phone (206) 883-2176 [Circle 381]

SOFTWARE TURNS PC INTO DIGITAL SCOPE

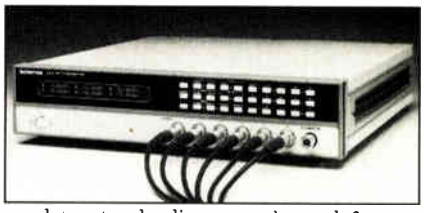
The Snapshot Storage Scope software package turns an IBM Personal Computer into a digital storage oscilloscope. Collecting data that has already been converted from analog to digital by one of the company's DT2801 data-acquisition boards, the package displays the information on the computer's monitor much as an oscilloscope would.

Data can be collected from up to four input channels, and all functions on the menu-driven program are executed with a single keystroke. The data collected and stored by the program is compatible with a variety of spreadsheet packages, such as DADiSP, Lotus 1-2-3, and Symphony. The $495 program is available immediately and delivery is from stock.
Data Translation Inc., 100 Locke Dr., Marlboro, Mass. 01752.
Phone (617) 481-3700 [Circle 389]

POWER METER CAN SUPPORT SIX INPUTS

The 4300 Multichannel Power Meter supports up to six fully independent input channels and can simultaneously monitor, display, manipulate, and put out measurements between –70 and +70 dBm.

The system uses coaxial sensors with dynamic ranges of up to 90 dB that cover frequencies between 100 kHz and 26.5 GHz. Also available are waveguide sensors with 70-dB dynamic ranges going from 18 to 110 GHz. A programmable 30-MHz internal calibrator can be



used to standardize any channel for accuracy better than ±1%.

The 4300 is ideal for swept measurements, the company claims, because data can be synchronized from channel to channel when the meter is in sample trigger mode. In that mode, the meter can produce measurements of all channels within a 20-ms timeframe. A four-channel configuration without sensors is priced at $6,325 and takes eight weeks for delivery.

Boonton Electronics Corp., 791 Rt. 10, Randolph, N. J. 07869.
Phone (201) 584-1077 [Circle 385]

PC SOFTWARE SPEEDS OSCILLATOR TESTING

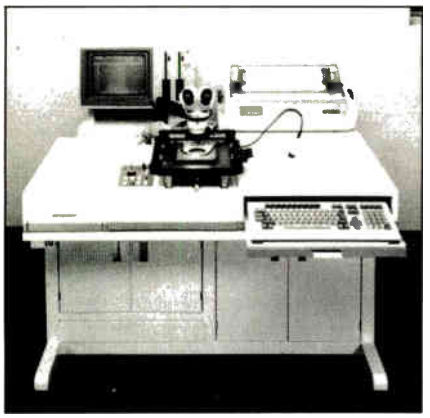
Easy-On software can cut oscillator testing time in half, its manufacturer says. Application-specific for settling time, post-tuning drift, hysteresis, and linearity, Easy-On is written around Basic and Compiled Basic for use with IBM Personal Computers and compatibles. It was designed for use with the company's 585 automatic pulse counter.

Requiring little or no computer knowledge on the part of the operator, the software includes a data-collection function that provides a plotted output of results to dot-matrix printers. The $250 package is available now.

EIP Microwave Inc., 2731 N. First St., San Jose, Calif. 95134.
Phone (408) 946-5700 [Circle 386]

PROBE-CARD TESTER IS FULLY AUTOMATIC

Probe cards with up to 512 pins can be checked for resistance, trace leakage, and shorts using the Micronics 760C Computerized Probe Card Tester. The self-programming 760C automatically recognizes probes and displays data. It has a maintenance menu and can be used for probe-point planarization and



alignment. A light pen can be used to interact with the display, which graphically shows contact at 1, 2, 3, or more microns, pin alignment, color-coded resistance values for each pin, connector-to-pin resistance, and other data. The $60,000 machine takes eight weeks for delivery.

Marubeni International Electronics Corp., 3285 Scott Blvd., Santa Clara, Calif. 95054.
Phone (408) 727-8447 [Circle 387]

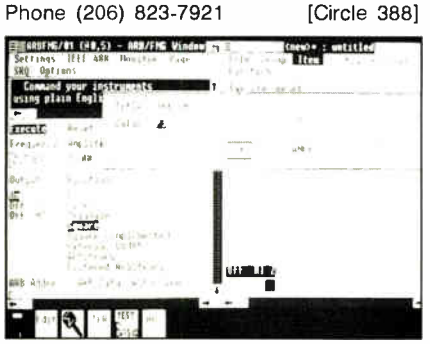
SOFTWARE LETS PC CONTROL INSTRUMENTS

An IBM Personal Computer AT or compatible is converted into an instrument controller with TestWindows Version 2.0, a program that lets the PC control any IEEE-488 programmable instrument. The new version includes facilities for guided-probe graphics and subroutine libraries.

TestWindow's key feature is Summation's IEEE-488 Window Generator, which simplifies programming and reduces development time for board-, subassembly-, and system-level automatic testing. The user interface is simple: users select icons and commands with a mouse. There are two modes of operation—immediate and programming.

The company supplies windows designed for control of a variety of instruments, and users can create additional windows using an application program called Window Editor. Unit-priced at $1,950, TestWindows requires six weeks for delivery.

Summation Inc., 11335 N. E. 122nd Way, Kirkland, Wash. 98034.
Phone (206) 823-7921 [Circle 388]



ONE-CHIP BELL 202 MODEM SELLS FOR UNDER $10

1,200-BAUD CHIP CUTS COSTS IN APPLICATIONS WHERE FAST TRANSMISSION IS NEEDED IN ONE DIRECTION

A one-chip asynchronous modem from Texas Instruments Inc. gives designers a price-performance advantage, with a price less than $10 in high volumes. In full-duplex mode, the frequency-shift-keying TCM3105 modem can transmit at 1,200 baud and receive at 150 baud—or vice versa—over two wires for such Bell 202 or CCITT V.23 applications as point-of-sale terminals, automatic teller machines, videotex systems, and remote data loggers.

The chip can also operate at 1,200 baud for both transmitting and receiving in the half-duplex mode. Other modem ICs that satisfy Bell 212 standards can run at 1,200 baud in full-duplex mode. But these chips must use more-complex phase-shift keying and for the most part sell for about $20 more than the TCM3105, according to TI.

The chip shines in applications where the vast majority of data flows in one direction and where low data rates in the other direction are acceptable. For example, a host computer that collects data from outside systems will likely receive far more data than it transmits.

The slower half of the conversation can be made invisible to the user, says TI, so that there is no perceived drop in performance relative to the Bell 212 approach. A videotex system that receives at 1,200 baud can therefore be built for a cost close to that of one based on the 300-baud Bell 103 standard.

Fabricated with TI's silicon-gate LinCMOS technology and incorporating switched-capacitor filters, the TCM3105 typically consumes only 5.5 mA from a single 5-V supply, which suits it for use in portable, battery-powered equipment. It is housed in a 16-pin ceramic DIP.

The modem is available now for 0°-to-70°C operation at $9.94 in lots of 1,000. A version for the industrial temperature range, –40° to 85°C, is $15.83.

Texas Instruments Inc., Semiconductor Group, P. O. Box 809066, Dallas, Texas 75380. Phone (800) 232-3200 [Circle 440]

PROCESSOR TIES TERMINALS TO T1 LINE

With an eye toward chopping the cost of remote 3270-networking while significantly improving terminal response times, Lee Data Corp. will start shipments next month on its model 525 T1 communications processor.

Unlike most other remote 3270 networking solutions, the 525 does not require the use of an IBM-class 3705/3725 front-end processor at the host. Instead, the 525 attaches to a host through a channel while interconnecting via T1 transmission lines to remote Systems Network Architecture controllers made by Lee Data.

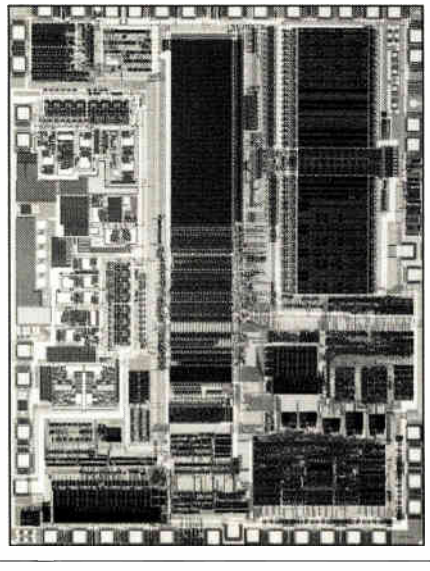
The Model 525 cannot provide the network-control functions of a full-fledged front-end communications processor, but it does provide remote 3270/host communications at full 1.544-Mb/s T1 rates. This compares to maximum 64-kb/s rates provided by IBM and others, Lee Data says.

Compared with the $70,000 to $200,000 price of a front-end processor, the 525 sells for $19,185 in single-unit quantities. It supports up to four remote Lee Data controllers simultaneously. Each controller can support up to 32 displays. A model 550 interface expander priced at $1,500 is required to attach more than one controller to a single T1 line.

Lee Data Corp., 7075 Flying Cloud Dr., Minneapolis, Minn. 55344.
Phone (612) 828-0300 [Circle 444]

1,200-BAUD MODEM IC CARRIES ITS OWN UART

Advanced Micro Devices Inc. believes its Am79C12 to be the first one-chip, 1,200-baud, full-duplex Bell 212A modem to incorporate an on-chip universal asynchronous receiver/transmitter. The UART provides such functions as parallel data transfer, parity generation and checking, and overrun and framing-error detection, making possible direct connection of the modem IC to a microprocessor bus.



The Am79C12 lets the user choose parallel or serial data transmission through software control, making the device useful for applications ranging from integrated personal-computer modems to box modem designs. The CMOS chip does modulation, demodulation, filtering, analog-to-digital and digital-to-analog conversion, and other tasks. Thus only control circuits and a simple protective phone-line interface are needed to implement a complete modem.

The chip supports automatic dialing with dual-tone multifrequency generation, pulse dial-through support, progress tone detection, and answer-back tone detection. Digital signal-processing techniques implemented on chip ensure stability over time and temperature, and reduce noise and voltage sensitivity.

Available now in production quantities, the Am79C12 sells for $48 in lots of 100, housed in a 40-pin plastic dual in-line package.

Advanced Micro Devices Inc., 901 Thompson Pl., P. O. Box 3453, Sunnyvale, Calif. 94088. Phone (408) 732-2400 [Circle 445]

GaAs FET STICKS TO POWER BUDGET

The HMF-0330 gallium arsenide field-effect transistor delivers high amplifier-stage gain and hews to limited power-consumption budgets in microwave applications in the 2- to 20-GHz range. Typical maximum gain is 13.5 dB at 8 GHz with a 4-V drain-to-source bias and drawing only 20 mA.

Under similar conditions, maximum gain is 11 dB at 12 GHz and 8 dB at 18 GHz. The linear power capability of the FET associated with maximum-gain tuning is typically 14 dBm at 18 GHz, making it suitable for multiple successive gain blocks, including initial driver stages. The transistor's gate measures 300 by 0.5 μm.

Under low noise bias, the typical noise figure is 1.3 dB at 8 GHz, with an associated gain of 10.5 dB. The drain current at zero gate voltage (I_{DSS}) stays within a guaranteed range of 20 to 60 mA.

The manufacturer performs radio-frequency and reliability qualification of each wafer. A titanium-platinum-gold metalization system and dielectric scratch and short-circuit protection also add to the FET's reliability. It is available from stock at $12.75 in lots of 1,000.

Harris Microwave Semiconductor, 1530 McCarthy Blvd., Milpitas, Calif. 95035. Phone (408) 262-2222 [Circle 446]

CONVERTERS LINK ASCII GEAR TO HOST

Four protocol converters from May-Craft Information Systems Inc. offer a range of capabilities in interfacing personal computers, ASCII terminals, and printers with IBM Corp. host systems.

The 74R comes with 3, 5, 7, or 9 ports and supports access to two hosts. It emulates 3274 or 3276 control units and allows asynchronous terminals to emulate 3278 terminals.

The May-Craft 3780 is a bisynchronous unit that emulates IBM 3780, 2780, 2770, and 3741 behavior, allowing users to move data at 19.2 kb/s.

A third product, the 87P, interfaces standard ASCII printers to an IBM 3274, 3276, or 4701 control unit via the IBM Type A device adapter.

Finally, the 78T protocol converter links ASCII terminals and personal computers to IBM 3274 and 3276 controllers so they can emulate 3278-2 terminals. It operates at 19.2 kb/s on an RS-232-C interface and may be configured for dedicated or dial-up applications.

All the converters are available now. The 74R sells for $3,000 to $6,000, depending on configuration. The May-Craft 3780, 87P, and 78T are priced at $1,445, $1,495, and $995, respectively.

May-Craft Information Systems Inc., 4312 Beltwood Parkway South, Dallas, Texas 75244. Phone (800) 527-7456 [Circle 447]

CMOS TONE RECEIVERS ARE POWER MISERS

Three dual-tone multifrequency receiver integrated circuits from Crystal Semiconductor are said to offer superior dial-tone rejection performance and to require less power than alternative products. The CSC202, 203, and 204 all provide 22 dB of dial-tone rejection and run on a typical 22.5 mW.

The receivers recognize and decode dual-tone multifrequency signals and transmit digital signals that identify the received tone pair. They meet all central-office specifications.

Used for access and control, data entry, and phone switching applications, the CSC203 provides early detection of tone bursts for voice-messaging and private-branch-exchange applications. The CSC204 is designed for subscriber equipment such as telephone answering machines.

Built in 3-μm CMOS, the chips have tone sensitivity from −2 to −32 dBm.

In quantities of 1,000, the CSC202 is priced at less than $4.50, the 203 at less than $6, and the 204 at less than $3.25. Samples are available now.

Crystal Semiconductor Corp., 2024 E. Saint Elmo Rd., P. O. Box 17847, Austin, Texas 78760. Phone (512) 445-7222 [Circle 448]

COMPUTER SOFTWARE

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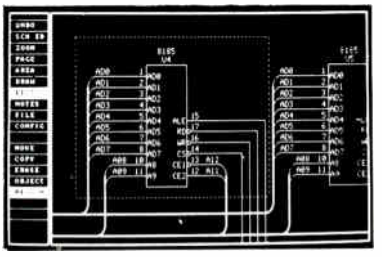

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MEETINGS

Semicon/Southwest '86, Semiconductor Equipment and Materials Institute (805 East Middlefield Rd., Mountain View, Calif. 94043), Infomart, Dallas, Oct. 15-16.

Scan-Tech '86, Automatic Identification Manufacturers Inc. (1326 Freeport Rd., Pittsburgh, Pa. 15238), Moscone Convention Center, San Francisco, Oct. 15-17.

International Conference on Semiconductor and Integrated Circuit Technology, University of California-Berkeley, (Continued Education in Engineering, University Extension, Univ. of California, 2223 Fulton St., Berkeley, Calif. 94720), Beijing, People's Republic of China, Oct. 19-22.

Intelec '86: International Telecommunications Energy Conference, IEEE (Don Reid, Bell Northern Research, P. O. Box 3511, Station C, Ottawa, Ont. K1Y 4H7 Canada), Royal York Hotel, Toronto, Oct. 19-22.

Convergence '86: International Congress on Transportation Electronics, Society of Automotive Engineers (Suite 602, 3001 W. Big Beaver, Troy, Mich. 48084), Hyatt Regency, Dearborn, Mich., Oct. 20-22.

International Symposium for Testing and Failure Analysis—1986, American Society for Metals (Metals Park, Ohio 44073), Los Angeles Airport Hilton, Los Angeles, Oct. 20-24.

Ergodesign 86, Ergodesign (P. O. Box 122, CH-1820, Montreux, Switzerland), Montreux Congress Centre, Montreux, Switzerland, Oct. 21-24.

Asia-Electronics, Singapore Manufacturers' Association, *et al.* (Interfama Exhibitions PTE LTD, 1 Marine Parade Central, Parkway Builders' Centre, #10-03/06, Singapore 1544), World Trade Centre, Singapore, Oct. 21-25.

1986 Joint Power Generation Conference, IEEE (G. R. Meloy, U. S. Army Corps of Engineers, P. O. Box 2870, Portland, Ore. 97208), Portland Hilton Hotel, Portland, Ore., Oct. 22-24.

Fifth Annual Pacific Northwest Computer Graphics Conference, University of Oregon (University of Oregon Continuation Center, 1553 Moss St., Eugene, Ore. 97403), Eugene Conference Center and Hult Center for the Performing Arts, Eugene, Ore., Oct. 27-28.

IEEE Holm Conference on Electrical Contacts, IEEE (Fern Katronetsky, IEEE Headquarters, 345 East 47th St., New York, N. Y. 10017), Copley Plaza Hotel, Boston, Oct. 27-29.

Interface International in Europe Conference and Exposition, The Interface Group Inc. (300 First Ave., Needham, Mass. 02194), Parc des Expositions/Porte de Versailles, Paris, Oct. 27-29.

ATE Silicon Valley Conference and Exposition, MG Expositions Group (1050 Commonwealth Ave., Boston, Mass. 02215), Santa Clara Convention Center, Santa Clara, Calif., Oct. 27-30.

Defense and Government Computer Graphics '86, World Computer Graphics Association (P. O. Box N, Wayland, Mass. 01778), Washington Convention Center, Washington, Oct. 27-30.

1986 IEEE GaAs IC Symposium, IEEE, *et al.* (Robert Markunas, Research Triangle Institute, P. O. Box 12194, Research Triangle Park, N. C. 27709), Grenelefe Resort and Conference Center, Grenelefe, Fla., Oct. 28-30.

Fall Joint Computer Conference, IEEE Computer Society, *et al.* (1950 Stemmons Freeway, Suite 6038, Dallas, Texas, 75207), Infomart, Dallas, Nov. 2-6.

AM '86, Automated Manufacturing Exhibition and Conference, The Consortium for Automated Manufacturing (P. O. Box 5616, Greenville, S. C. 29606-5616), Greenville Technical College, Greenville, S. C., Nov. 3-6.

Space Simulation Conference, Institute of Environmental Sciences, *et al.* (940 East Northwest Highway, Mount Prospect, Ill. 60056), Sheraton Inner Harbor Hotel, Baltimore, Nov. 3-6.

Lasers '86, Society for Optical & Quantum Electronics (P. O. Box 245, McLean, Va. 22101), Peabody Hotel, Orlando, Fla., Nov. 3-7.

International Electronic Imaging Exposition & Conference, Morgan-Grampian Expositions Group, *et al.* (Ed Martin, Sales Manager, 1050 Commonwealth Ave., Boston, Mass. 02115), Sheraton-Boston Hotel, Boston, Nov. 4-6.

International Workshop on Symbolic Layout and Compaction, Microelectronics Center of North Carolina (Franc Brglez, MCNC/BNR, 3021 Cornwallis Rd., Research Triangle Park, N. C. 27709), Hotel Europa, Chapel Hill, N. C., Nov. 5-6.

Electronica '86 and 12th International Microelectronics Conference, Munich Fair and Expositions GmbH, *et al.* (Postfach 12 1009, D-8000 Munchen 12), Munich Trade Fair Center, Munich, West Germany, Nov. 11-15.

Electronics CAREER OPPORTUNITIES

Fall 1986 Planning Guide

Issue		Closing
October 2	**Computer Technology** CAD/CAM/CAE	September 15
October 16	**Technology Outlook Special Issue** ■ Semiconductors ■ Communications ■ CAD/CAM/CAE ■ Packaging & Production ■ Test & Measurement ■ Industrial Electronics ■ Consumer Electronics ■ Computers ■ Software **Military Technology** Military Career Section *Postcom Readership Survey*	September 29
October 30	**Software Technology** Artificial Intelligence	October 10
November 13	**Wescon Preview** Bonus Distribution at Wescon **Instruments Technology** Automatic Test Equipment	October 27
November 27	**Communications Technology** Fiber Optics Special Communication Career Section	November 10
December 11	**Semiconductor Technology** Linear ICs IEDM Preview **Military Technology** Special Section: Military Electronics *Postcom Readership Survey*	November 24
December 25	**Computer Technology** PC Boards Peripheral Boards	December 8

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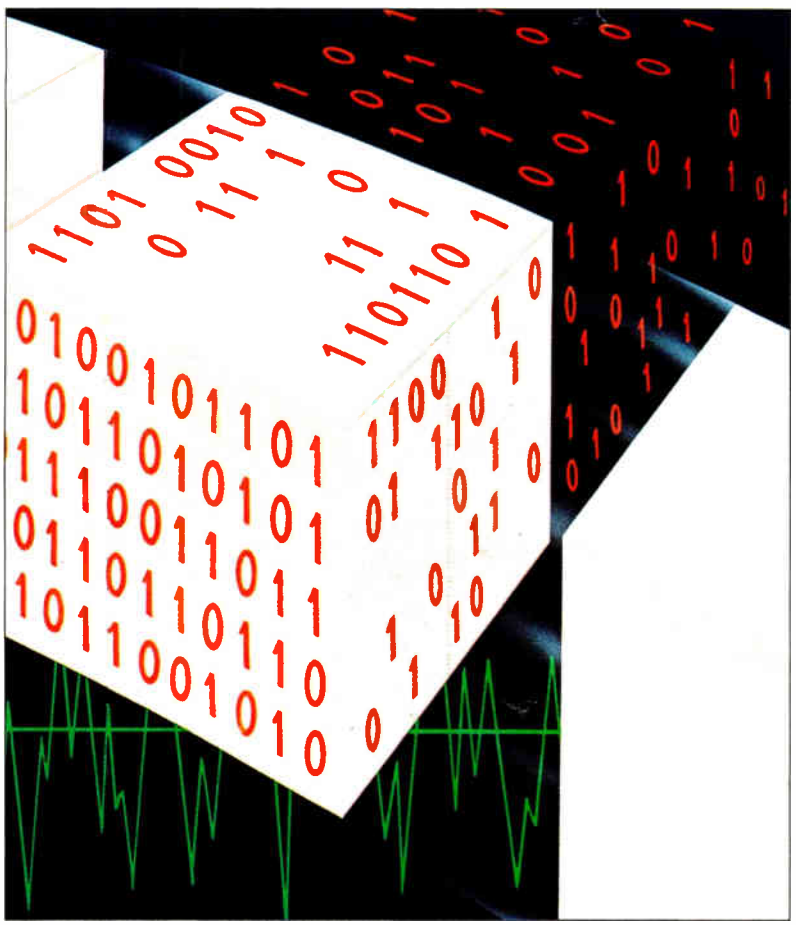

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Excerpted from an exclusive article in the July 24, 1986 issue.

Electronics

THE LEADER IN NEW TECHNOLOGY COVERAGE

ELECTRONICS WEEK

IBM CUTS PRICES, ENHANCES RT PC

Less than a month after IBM Corp. delivered the first models of its RT Personal Computer, Big Blue is already offering enhancements to the basic product—and cutting prices, too. The RT is a high-powered reduced-instruction-set machine [*Electronics*, Jan. 27, 1986, p. 14] aimed at the high end of the engineering market.

Among the changes: a two-fold increase in internal memory capacity; a floating-point accelerator card that can triple the speed of floating-point calculations; a facility to double the number of system users to 16; and price cuts of 20% to 32%, depending on the model. Even with the price cut, though, the machines don't come cheap: the least expensive RT PC will go for at least $7,000.

TI PLANS MOVE INTO BiCMOS

Texas Instruments is marrying bipolar and CMOS technology in a new family of three-state bus interface circuits. Joining a growing BiCMOS trend, TI will announce the series later this year under the name ABCT, for advanced bipolar CMOS with TTL-compatible input-output signals. The devices will be made using a variation on TI's bipolar Impact technology, to which masks for CMOS transistors will be added. TI is also working on Impact-CS, an enhanced 1.5-μm version it says will improve performance in the CMOS portion of the devices. Next year, TI will roll out another BiCMOS mixture, based on CMOS technology and aimed at very large-scale integrated logic and 1-μm random-access memories.

NEC DEVELOPS LOW-NOISE VCR

Not only is its DX1000U VHS video cassette recorder the first consumer model to use digital noise reduction techniques, says NEC Consumer Electronics, but the new machine outperforms four-head VCRs—even though it uses the more conventional two-head technology. NEC claims the $699 VCR offers a 9-dB improvement in the signal-to-noise ratio. The noise reduction system works only in the playback mode and is based on the summing of two consecutive video fields. Picture information is effectively doubled, while random noise increases minimally.

OLIVETTI BUYS TRIUMPH-ADLER

Ing. C. Olivetti & Co. has completed its takeover of the West German office equipment maker Triumph-Adler AG from Volkswagenwerk AG. VW relinquished 98.4% of its shares in Triumph-Adler to the Italian company, and in return the West German car maker has acquired 5% of Olivetti—worth a total of $300 million. Olivetti wasted no time installing a new man to head Triumph-Adler's operations in Nuremberg: Francesco Tato has already taken over.

ATARI READIES PUBLIC OFFERING

Warner Communications Inc. will finally get something out of its relationship with Atari Corp. when the Sunnyvale, Calif., computer maker goes public this fall. Atari will offer 4.5 million shares of stock at between $11.50 and $13.50 a share; it will use part of the proceeds to pay off the $36.1 million still owed Warner as part of the deal under which Atari chairman Jack Tramiel took control of the struggling company in 1984. Warner now owns 7.1 million shares in Atari, representing about 25% of the stock that will be outstanding after the offer. Tramiel will own 45%. Atari earned about $8.5 million on sales of $105.6 million in the first half of 1986—which is not much when compared with the $750 million Warner reportedly has lost since it bought Atari in 1976.

SIEMENS SIGNS SOVIET CONTRACT

The Soviet Union has awarded Siemens AG a $10 million contract to automate what it claims to be the world's biggest blast furnace, a facility at the iron works in Tscherepowetz, about 300 miles north of Moscow. The contract encompasses a process computing system with peripherals, user software, and instrumentation. Munich-based Siemens will also train the Soviet personnel and furnish documentation.

IBM WILL TRY TO TRIM ITS RANKS

Add IBM Corp. to the growing list of companies trying to trim down their ranks. IBM is offering a voluntary retirement incentive aimed at helping the computer giant cut more than 8,000 jobs in 1987—more than twice the number that will disappear this year as a result of normal attrition and limited hiring. IBM is seeking to reduce its overall U.S. staff to about 230,000 or less; it had 242,241 employees at the conclusion of 1985.

ZYMOS SEARCHES FOR A NEW CEO

Zymos Corp., the Sunnyvale, Calif., maker of ASICs that has lost more than $35 million over the past three years, is looking for a new chief executive officer following the resignation of founder W. Bert Braddock. Vice president Haller M. Moyers has been named interim chief operating officer. Meanwhile, Daewoo Corp., the Korean conglomerate that bought control of Zymos in August, named its chairman, W. C. Kim, to chair the Zymos board of directors, a post that had been vacant since February.

ASHTON-TATE TO ACQUIRE DRI

Ashton-Tate Inc. plans to acquire Decision Resources Inc., an independent supplier of business graphics software for microcomputers. With about $13 million in annual sales and more than 100 employees, the Westport, Conn., company will get $12.9 million in the deal, which should be completed by Oct. 1.

TELEVIDEO MERGING WITH ALPHA MICRO

Televideo Systems Inc. will combine its line of terminals and work stations with Alpha Micro multiuser computers—if Televideo's takeover offer is successful. The Sunnyvale, Calif., firm offered $25 million in cash and $25 million in stock in a friendly $8-per-share offer for Alpha Micro, Santa Ana, Calif., which was accepted by the Alpha Micro board to thwart a $6-per-share bid from Point 4 Data Systems, Inc. Point 4, of Tustin, Calif., said it does not intend to make a counteroffer.

NATIONAL, MMI TO CUT PLANT HOURS

Continued poor semiconductor sales are forcing Monolithic Memories, Inc., and National Semiconductor Corp. to plan temporary plant closings during the balance of 1986. MMI will close its manufacturing operations for 19 days between Sept. 29 and Jan. 1. Nonmanufacturing personnel will shift to four-day work weeks from now through Nov. 23, when the company will shut down for three weeks. A second three-week shutdown is planned around Christmastime. National will shut its plants for 14 days, not counting seven paid holidays. Combined, the closings will affect more than 12,000 employees.

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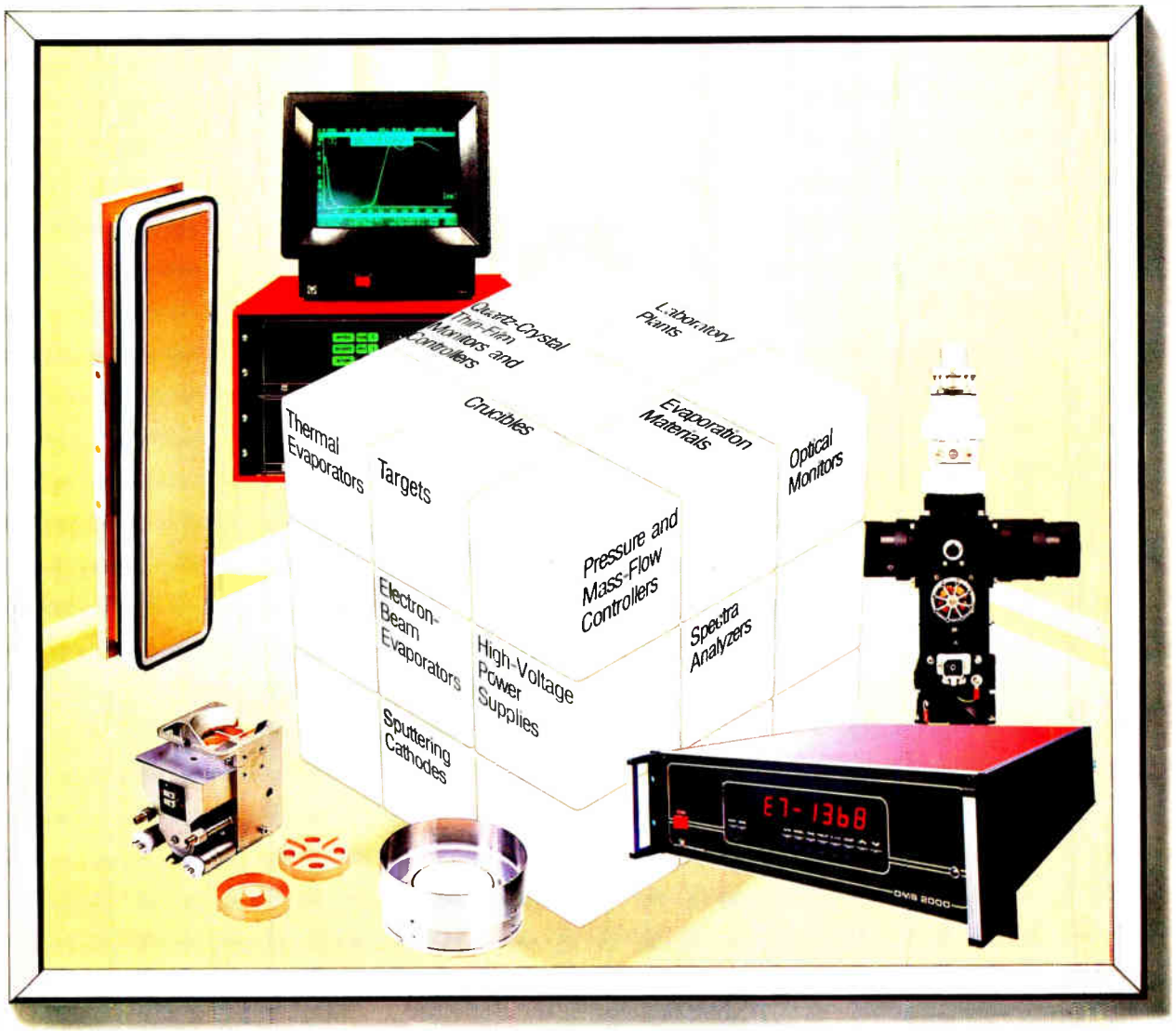

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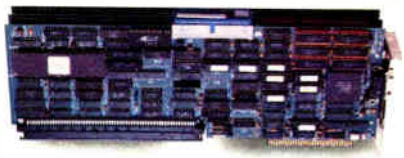

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