WHAT MAKES COMPAQ'S 386-BASED PC SO IMPORTANT/66

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A McGRAW-HILL PUBLICATION SIX DOLLARS SEPTEMBER 18, 1986

Electronics

GaAs LSI GOES COMMERCIAL

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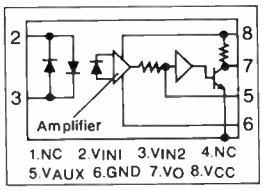

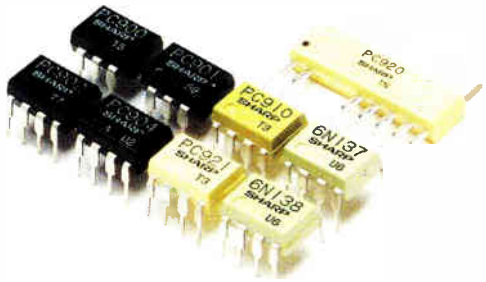

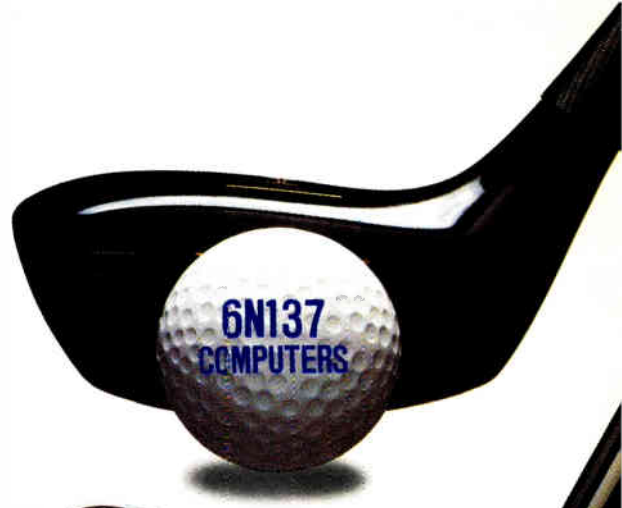

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	PC904	Built-in voltage deviation detection circuit	Switching power supplies
	PC910	Ultra high speed(10Mb/s)	Computers. Programmable controllers. Copiers
	PC920	For inverter control. Single-in-line package	Inverter air conditioners
	PC921	For inverter control. Dual-in-line package	Inverter air conditioners
6N series	6N135	High speed (1Mb/s)	Computers. Telephones. Measuring equipment. Numerical control machines
	6N136	High speed (1Mb/s)	Computers. Telephones. Measuring equipment. Numerical control machines
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	6N138	Low input current. High sensitivity (CTR:300 % min.)	Computers. Telephones
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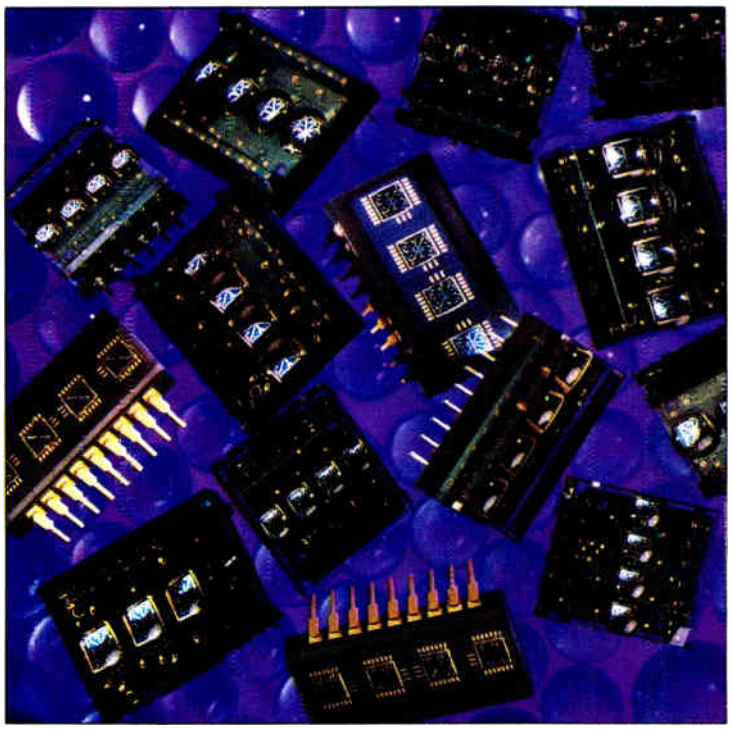

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PUBLISHER'S LETTER

A strong sense of curiosity honed by five years in market research prompted Ayako Hayashihara to start a new career in journalism: Ayako is editorial assistant to bureau manager Charlie Cohen in *Electronics'* Tokyo office. Her new spot watching Japan's lively electronics industry fulfills her wish to stay abreast of the rapidly changing Japanese business scene.

HAYASHIHARA. She can handle dBase II as well as the viola.

Starting her third job only five years after graduating from college might set Ayako apart in a country where people don't switch employers frequently. However, she left her former positions only when her employers in both cases decided to de-emphasize market research.

The initial two years of Ayako's first job—at the Tokyo office of Travenol Ltd., the Japanese pharmaceutical- and medical-equipment manufacturing subsidiary of Baxter Travenol Laboratories Inc.—were not so far removed from journalism. She reported and wrote on various activities at the company's plant for the company newspaper. Later, as part of a hospital-management service project, she helped write a dBase II program for the NEC Corp. 9801 personal computer. Ayako made her exit from that job when the firm decided that the market research arm of its business was not viable.

Her next job was at the Tokyo Consulting Group Inc., where she assisted Japanese and American executives in a management consulting business. Clients included Japanese firms as well as overseas companies planning to market products or enter into agreements or joint ventures with Japanese businesses. She did text searches in Japanese data banks and used Microsoft Corp.'s Multitool-File to maintain a data base on an IBM Corp. 5550 multistation. Fortunately for *Electronics*, the company switched its emphasis to mergers and acquisitions, and its need for the type of research Ayako had been doing decreased. She joined the magazine's staff last month.

In her spare time Ayako practices the viola to be ready for Sunday rehearsals of the classical string orchestra of which she is a member.

After growing up in Onomichi in Hiroshima Prefecture, Ayako enrolled at the prestigious Tokyo Woman's Christian University. There she studied English literature and earned licenses to teach English in junior high and high school.

She has lived in Tokyo for the last nine years and now is in a position to observe at close range one of the most remarkable industrial flowerings in her nation's history—the evolution of the Japanese electronics industry.

Laurence Altman

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WEEK 48

It's about time someone met the needs of the stingy. And AMD did it. With our new Am29C841 High-Performance CMOS 10-Bit Latch. Another member of AMD's Bus Interface Family.

The Am29C841 gives you speed comparable to a bipolar latch—with a propagation delay of only 11ns. But it only uses 80 microAmps at stand-by. That should warm any power-pincher's heart.

Am29C841

A latch for the stingy.

In addition to saving power, the Am29C841 is 10-bits wide. That extra data width is just what you need for wider address/data paths or buses carrying parity.

Use the Am29C841 instead of a bipolar latch when you need only moderate drive capability. The CMOS Am29C841 provides 24mA drive. Its MOS/TTL compatible inputs and outputs mean you can use it with both bipolar and MOS systems.

You don't necessarily have to be stingy to want a low-powered, high-performance latch like the Am29C841. You just have to be wise, far-sighted and exceptionally bright.

WEEK 49

Nothing travels faster than a good rumor except the data in AMD's new Am9580A Hard Disk Controller. A single chip that can make data approach the Speed of Gossip.

Am9580A

Only rumors travel faster.

To achieve this feat, we designed the Am9580A with on-board sector buffers. These make data easier to find so it's easier to pull up when it's needed. We also designed in Direct Memory Access (DMA). DMA retrieves data and transfers it directly to the main memory. And that takes a burden off the CPU.

But what really makes us a challenger to the coffee room is our Zero Sector Interleave. A user can pull up random data as much as six times faster than other hard disk controllers.

The Am9580A supports the ST 506 ANSI standard interface and the ESDI interface (which the coffee machine doesn't). And it's flexible. Handle any combination of up to four hard or floppy disk drives.

Get in and out of storage faster than ever with the Am9580A Hard Disk Controller. And, in case you were wondering, we got all this information from a very reliable source: AMD. Pass it on.

WEEK 50

You can't be everywhere at once. Then, how can you make sure your data goes where you want it? Easy. With the first 16-Bit Bounds Checker, the Am29337, the newest member of AMD's powerful 29300 family. It's designed to put data where it belongs: In memory.

Am29337

Border patrol

The Am29337 can compare addresses with stored upper and lower limits and tell your system if those limits are exceeded. And in which direction. It can compare with signed and unsigned numbers, too.

The Am29337 can compare available data intended for memory with available memory space and alert your system to potential overflows. (And never miss a bit.) Use it with the family or as a stand-alone. Also, the Am29337 is cascadable in 16-bit increments.

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WEEK 51

AMD's extraordinarily powerful, high-performance Am29300 Family welcomes its first CMOS member: The Am29C323 32-Bit Parallel Multiplier. It's easy to operate. And for such adult high-performance, it's hard to believe it has such a child-sized interest in power. When it's operating at 8MHz (125ns cycle time) it consumes less than one Watt.

Am29C323

Announcing a new addition: Multiplication

The Am29C323 will produce a 64-bit multiply from two 32-bit inputs. It supports multiprecision multiply. And dual input registers on both the X and Y buses increase the efficiency of the Am29C323.

With an internal 3-bus, 32-bit architecture, a 67-bit accumulator, shift register and temporary output register, it's guaranteed to give incredible performance and speed.

The Am29C323 isn't temperamental. It supports 2's-compliment, unsigned numbers and mixed numbers.

We also built in data integrity. The Am29C323 supports fault tolerant operation by running on master/slave mode. Parity is checked on input, and the Am29C323 generates parity on output.

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After building a comfortable lead with a new product a week, every week—on the shelf, in volume—we called in the heavy hitters:

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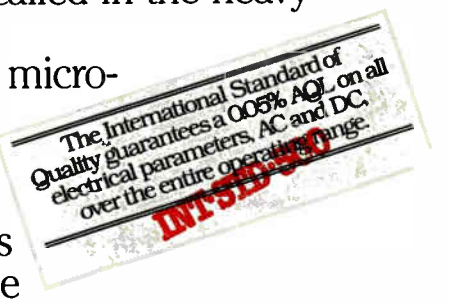

No one who follows the game closely is the least bit surprised. This team puts more dollars into R&D, as a percent of sales, than anyone else in the business.

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Advanced Micro Devices

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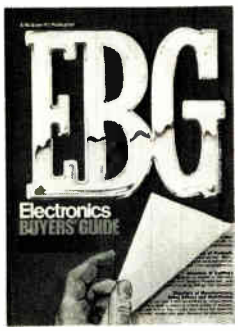

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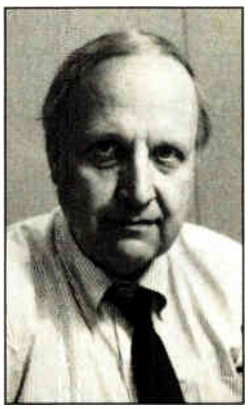
20-year-old words that still ring true: 'The FAA is as far from coping with the midair collision threat as it was on the day it was founded'



The Aug. 31 midair collision over Cerritos, Calif. between an Aeromexico DC-9 jetliner and a Piper Archer triggered a sad sense of *deja vu* in us. The tragic crash once again reminded us that, after decades of effort, the U. S. still hasn't solved its air traffic control problems. Despite a long technology parade of potential solutions, the Federal Aviation Administration has not seen fit to install collision avoidance systems or ground-based gear that conflicted with its ideas. The agency decided long ago what such a system should look like, and it has never seriously considered other solutions, no matter how promising.

The FAA's not-invented-here attitude goes back decades. Indeed, for us it goes back as far as 1963 or 1964 when, not 10 miles from the Cerritos crash site, Hughes Aircraft Co. gave us a demonstration of a prototype three-dimensional CRT that it had developed with its own money. Instead of showing the crowded Los Angeles skies as many merging blips on a conventional, hard-to-read 2-D scope, Hughes' 3-D display showed the aircraft as easy-to-spot targets that looked as if they were flying over one another and separated by as much as 12 inches of depth. It took a special pair of glasses to help create this illusion, but such a display most likely would have helped a busy controller sort out aircraft in Los Angeles on Aug. 31, 1986. The FAA, however, never showed any interest in the Hughes prototype.

Over the years, this magazine has covered a wide variety of such technologies aimed at solving the ATC problems. In fact, as far back as July 24, 1967, we concluded: "The FAA has little to show for 16 years of effort in the field of air traffic control. Moreover, its record for availing itself of practical technology isn't inspiring."

And we stated in an editorial: "Of all the thousands of Government agencies, it would seem almost impossible to rate one as the worst. Yet technical men who have studied the air traffic control problems are willing to give that malodorous distinction to the FAA. The agency has turned out to be weak, ineffectual, unimaginative, and apathetic. The threat of midair collision hanging over the U. S. when the FAA was formed is still with us—only worse than ever. And the FAA is as far from coping with this threat as it was on the day it was founded." Those words ring just as true today.

ROBERT W. HENKEL

World Radio History

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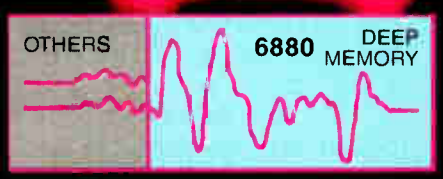

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Circle 110 for Demonstration

NEW 32-BIT CMOS MICROPROCESSORS.

The two new members of NEC's CMOS microprocessor V-Series bring unprecedented density and performance in the 32-bit realm. The V60 and V70 supermicros are the first to integrate a Memory Management Unit and basic floating-point processing functions on a single chip.

The V60 has a 16-bit external data bus for an easy, affordable path into 32-bit products while the V70 is a full 32-bit engine designed to power leading-edge systems.

The super-fast V60 and V70 offer a clock speed of 16MHz, and execute 3.5 MIPS and 6 MIPS respectively. A six-stage pipelined CPU enables concurrent execution of up to 4 instructions. With 32 on-board 32-bit general-purpose registers, there is no need to access slow off-chip memory.

The V60/V70 feature an on-chip memory management unit with 4 gigabytes of demand-paged virtual memory space, and 4 levels of memory protection for multi-tasking and multi-user environments.

The V60/V70 instruction set is ideal for high-level languages and OS support (UNIX™ V and proprietary realtime OS). There are 21 addressing modes, 273 instructions, and an emulation mode for 16-bit V20/V30 software.

UNIX: trademark of AT&T Bell Laboratories.

World Radio History

NUMBER 136

COMING SOON: 1.3/1.55μ DFB LASER DIODES.

Dispersion has always been a major obstacle in long-distance, high-speed light-wave communications. With conventional laser diodes emitting multiple spectrums, pulses deteriorate by dispersion after long travel through the fiber. This in turn limits repeater span to 20—30km and capacity to 400—560Mbps for the prevalent 1.3μ fiber optic systems.

NEC has overcome this obstacle with newly-developed distributed feedback (DFB) laser diodes for 1.3μ and 1.55μ fiber optic transmission systems. They feature a stable single longitudinal mode operation, high efficiency and high output power. The new DFB laser diodes are expected to expand repeater span to 80—100km for 1.3μ system or 100—200km for 1.55μ system.

NEC's new DFB laser diodes inherit the renowned double channel planar-buried heterostructure (DC-PBH) and have a diffraction grating in the optical guide region to produce a single wavelength. Output powers are rated 8mw for the 1.3μ NDL5600 and 5mw for the 1.55μ NDL5650. They come in the TO-5 package with an integral monitor photo diode or chip-on-carrier configurations.

As matching light-receiving devices, NEC has planar type InGaAs avalanche photo diodes. They have a selective guard ring construction to achieve high sensitivity and excellent reliability.

NEW INTELLIGENT BUILDING COMPLEX AT VANCOUVER.

The intelligent building is an idea whose time has come. As the perfect nestling for office workers in the Information Age, it centers on an advanced information management system which provides simultaneous voice, data and image services to tenants at less cost while it controls the entire building environment efficiently.

The World Trade Centre/ Pan-Pacific Vancouver Hotel recently opened is just such an installation. NEC's NEAX 2400 Information Management System (IMS) allows tenants to utilize enhanced telephone/facsimile services including least-cost routing, message center and voice mail services, and computer terminal connection via a multifunction digital telephone set. The NEAX 2400 IMS also offers sophisticated services to hotel guests.

NEC's Intelligent Building Systems, based on our unique C&C (integrated computer and communications) technology, are the most advanced and comprehensive available today. As the core of this system, the modular NEAX 2400 IMS can expand to 255 tenant partitions. It supports more than a hundred advanced features including a protocol converter to allow communication with most popular host computers. NEC also supplies comprehensive component equipment including multifunction digital telephones, information display pagers, high-speed facsimiles, business and personal computers, teleconferencing and CATV equipment and local distribution microwave links.

NEC's comprehensive systems breathe new life into the smart building concept, bringing costly services like teleconferencing within the reach of every business.

NEW HIGH-CAPACITY 64QAM DMR SERIES.

NEC's newest 800 Series high-capacity digital microwave radio (DMR) systems transmit two or three DS3 signals per RF carrier, utilizing 64-state quadrature amplitude modulation (64QAM) for effective use of radio spectrum.

Three systems meeting FCC standards are available: a 4GHz 90M-bit system providing 1,344 voice channels, and 6GHz and 11GHz 135M-bit systems for 2,016 voice channels.

The new systems incorporate the latest LSIs, hybrid and microwave ICs throughout to achieve compact design, lower power consumption and improved system reliability. Housed in a standard 19-inch rack, they require minimal cabling work for installation.

The advanced 800 Series is fully compatible with Bell's facility maintenance and administration system.

NEC

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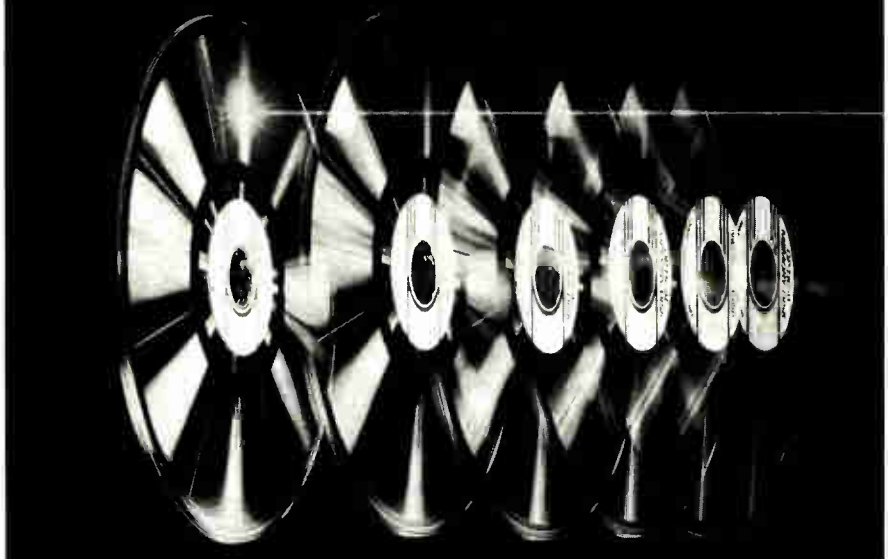
MASS PRODUCTION / 5¼"(130mm) WORM DISK



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"Chemitronics" combines advanced chemical and electronic technology. Our unique chemitronic technology produces optical recording disks with high reliability and low cost volume production, and is used at our ultramodern Harima plant to manufacture the optical recording disk (WORM).

These laser-road large-capacity storage disks have many information storage applications ranging from external memory for computers to office automation to video recording and herald a new stage in the information revolution.

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LETTERS

'Quantum leap' falls short

To the editor: The "new breed of photovoltaic cell" described in the article "A better way to build efficient solar cells" [*Electronics*, Aug. 7, 1986, p. 38] represents neither a "quantum leap in conversion efficiency" nor a savings in cost. While the Erlangen inversion layer cell is an interesting laboratory device, it has no clear advantage over existing technology already in large-scale use. Indeed, inversion layer devices have a reputation for poor stability under environmental stress, and are notoriously difficult to reproduce with reasonable yields on large-area substrates.

At Solarex, our "conventional" technology uses inexpensive continuous processes, which eliminate batch metallization evaporations and expensive chemical vapor deposition operations.

Stephen P. Shea
Manager, Cell Technology
Solarex Corp.
Rockville, Md.

Ask if ye will learn

To the editor: You surely touched on some key points in your cover story, "What's holding back expert systems," [*Electronics*, Aug. 7, 1986, p. 59], but I think you missed one: The vendors don't appear to be exerting enough effort to find out what customers need.

I've been approached often by vendors who are very cognizant of the strengths of their own products and the weaknesses of the competition's but who never once ask me what I could use. You might consider a survey of artificial intelligence developers in business and industry, and ask us what we need in AI hardware, development software, communications, etc. Maybe if *Electronics* says it, the manufacturers will listen.

Hannah Blank, Vice President
Advanced Product Research Division
The Chase Manhattan Bank, N.A.
New York

Standby, not maximum

Correction: *The standby current rating of Altera Corp.'s EP320 was incorrectly reported in "Erasable PLD draws only 10 mA"* [Electronics, *Aug. 21, 1986, p. 84*]. *The correct standby figure is 10 μA; the maximum current rating, 10 mA.*

Smaller than you think

Correction: *The drawn gate length of Performance Semiconductor Corp.'s static RAMs was misstated in the chart "Who's doing what in fast static RAMs"* [Electronics, *Aug. 7, 1986, p. 122*]. *Performance Semiconductor uses a 0.8-μm technology.*

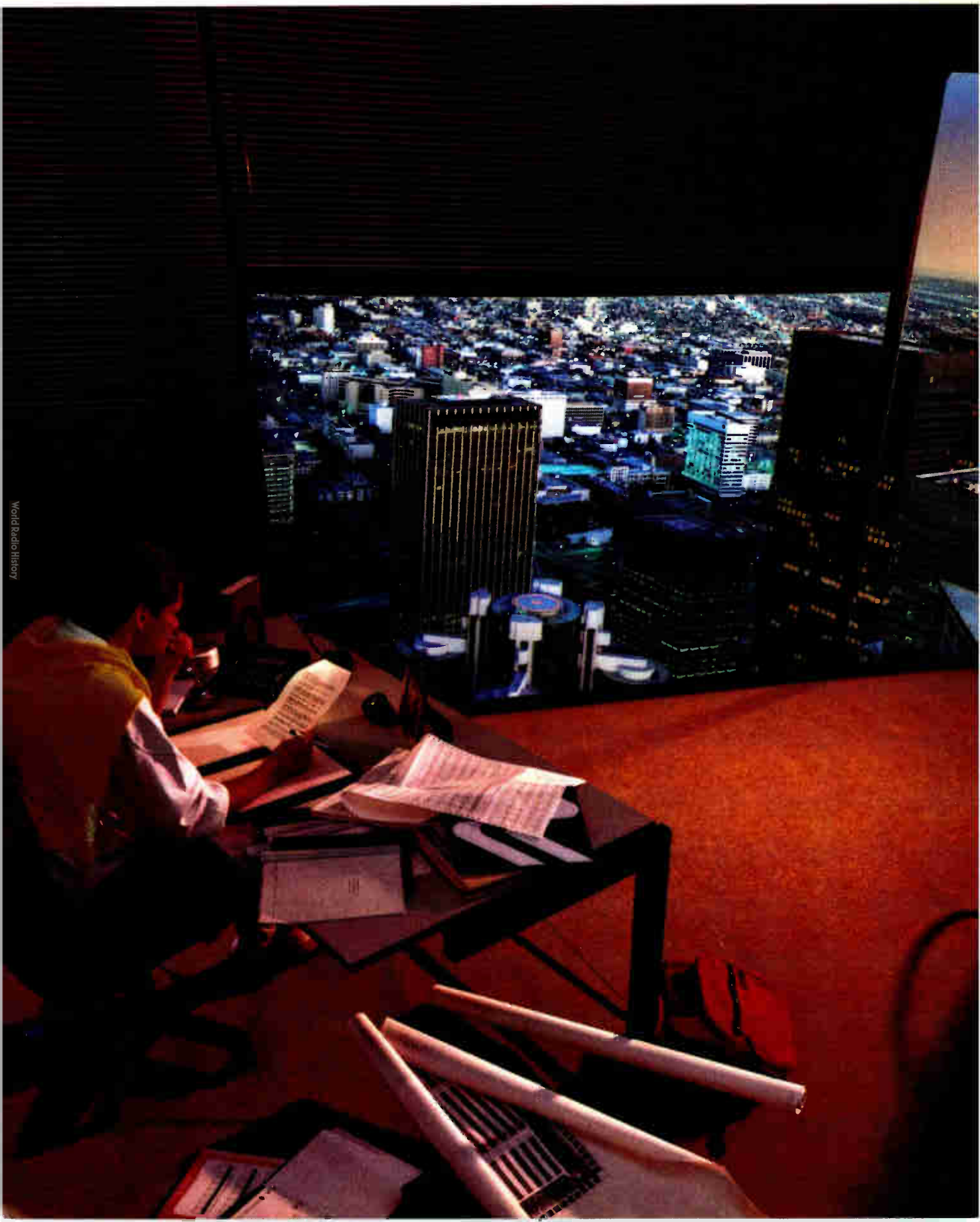
World Radio History

Long hours.
Late nights.
Lost weekends.

Nobody said choosing an ASIC company was going to be easy.

World Radio History

National Semiconductor



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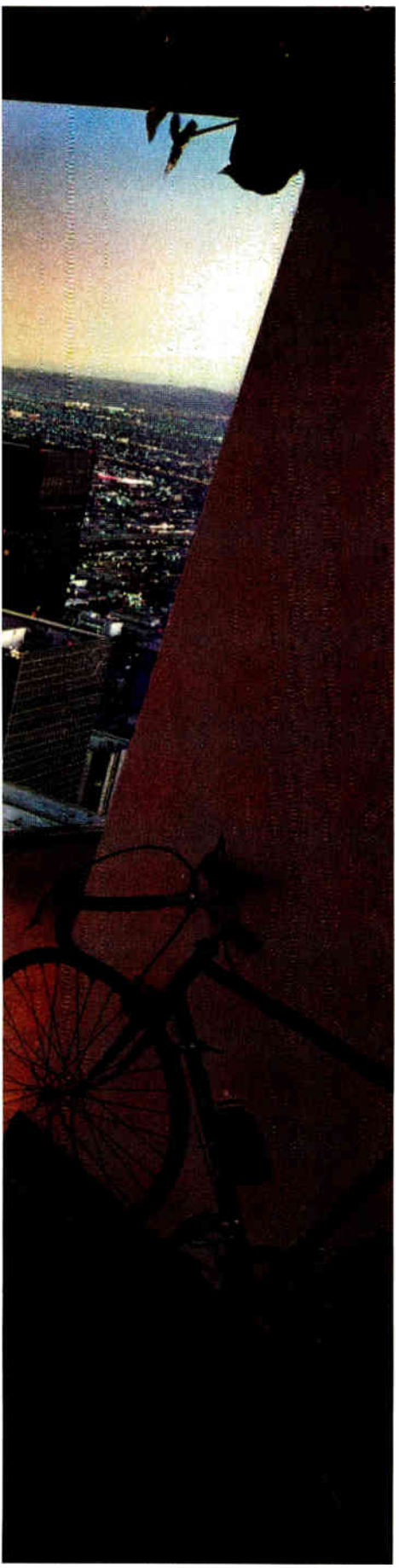

Xerox spent a year examining the same ASIC companies you're looking at now.

Only one made it to the top.

Long hours. Late nights. Lost weekends. Nobody said it was going to be easy.

But choosing the right ASIC manufacturer is critical to your product's success — and perhaps your company's.

So when Xerox anticipated their long-term needs for CMOS gate arrays and standard cells, they constructed a comprehensive list of criteria and launched a world-wide search.

That search took more than a year and involved over 30 companies. In the end, only one had the right combination of sophisticated design tools, extensive cell libraries, dedicated engineering and support staffs, well-established manufacturing strength, the flexibility to meet customer needs, and a demonstrated long-term commitment to ASIC technology.

Because Xerox knew they needed more than just an ASIC supplier... they needed an ASIC technology *alliance.*

That's why Xerox chose National Semiconductor.

If you want to learn what Xerox learned about National, just write:

National Semiconductor Corp.
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National Semiconductor

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Preci-sely what you need

A comprehensive range of IC Sockets, manufactured to the highest standard at a competitive price.

Precicontact, a pioneer of the two-piece screw machined socket terminal, are one of a few companies offering fully gold plated contact clips.

Our range of versatile, competitively priced sockets covers turned-pin and stamped contact versions with solder or wire-wrap tails for all applications; patented snap-a-part and carrier sockets; socket adaptors and custom models.

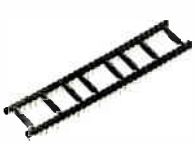
Seventeen years of high precision manufacture has resulted in MIL spec approval and regular use by the world's top aerospace, telecom and computer producers.

USO Series

- open insulator, 6 to 64 ways
- stackable end-to-end/side-to-side
- machined outer sleeve with precision inner contact, plated all over
- contact features closed end construction

SO Series

- closed insulator, 6 to 40 ways
- stackable end-to-end/side-to-side
- machined outer sleeve with precision inner contact, plated all over
- contact features closed end construction



DSO Series

- DIL socket, breakable into any required length
- reduced inventory space
- contacts remain perpendicular to the board when bridges are taken away after soldering
- can be used as a SIL socket

SSO Series

- SIL socket, breakable into any required length
- ease the preparation of prototypes
- precision contact

CSO Series

- brass carrier, 60 to 40 ways
- direct visibility for soldering inspection and repair
- allows maximum air circulation under IC's

SOM Series

- MIL S/83734C approved
- stackable end-to-end/side-to-side
- machined outer sleeve with precision inner contact, plated all over
- contact features closed end construction

UH Series

- open insulator, 6 to 40 ways
- meets most severe environmental operating conditions
- operating temperature −65° C to +250° C
- machined outer sleeve with special Beryllium alloy 4 leaf contact, plated all over
- contact features closed end construction

LED Series

- LED sockets, 6 to 40 ways
- stackable end-to-end
- machined outer sleeve with 4 leaf inner contact, plated all over

LSO Series

- 6 to 40 ways
- contact material phosphorous bronze pre tinned
- stamped and formed dual beamed contact
- available also with BeCu contact material
- stackable end-to-end/side-to-side

USA/USB Series

- adaptor with precision contacts
- open insulator, 6 to 64 ways
- stackable end-to-end/side-to-side
- contact features closed end construction

USC Series

- adaptor with precision contact
- open insulator, 60 to 64 ways
- stackable end-to-end/side-to-side
- contact features closed end construction

USD Series

- adaptor with precision contacts
- open insulator, 6 to 64 ways
- stackable end-to-end/side-to-side
- contact features closed end construction

UX Series

- large variety of configurations
- solder or wire wrap tail contact
- machined outer sleeve with precision inner contact, plated all over
- contact features closed end construction

So when you require sockets of quality at a price that's competitive we have preci-sely what you need.

For full information and price list, contact Precicontact.

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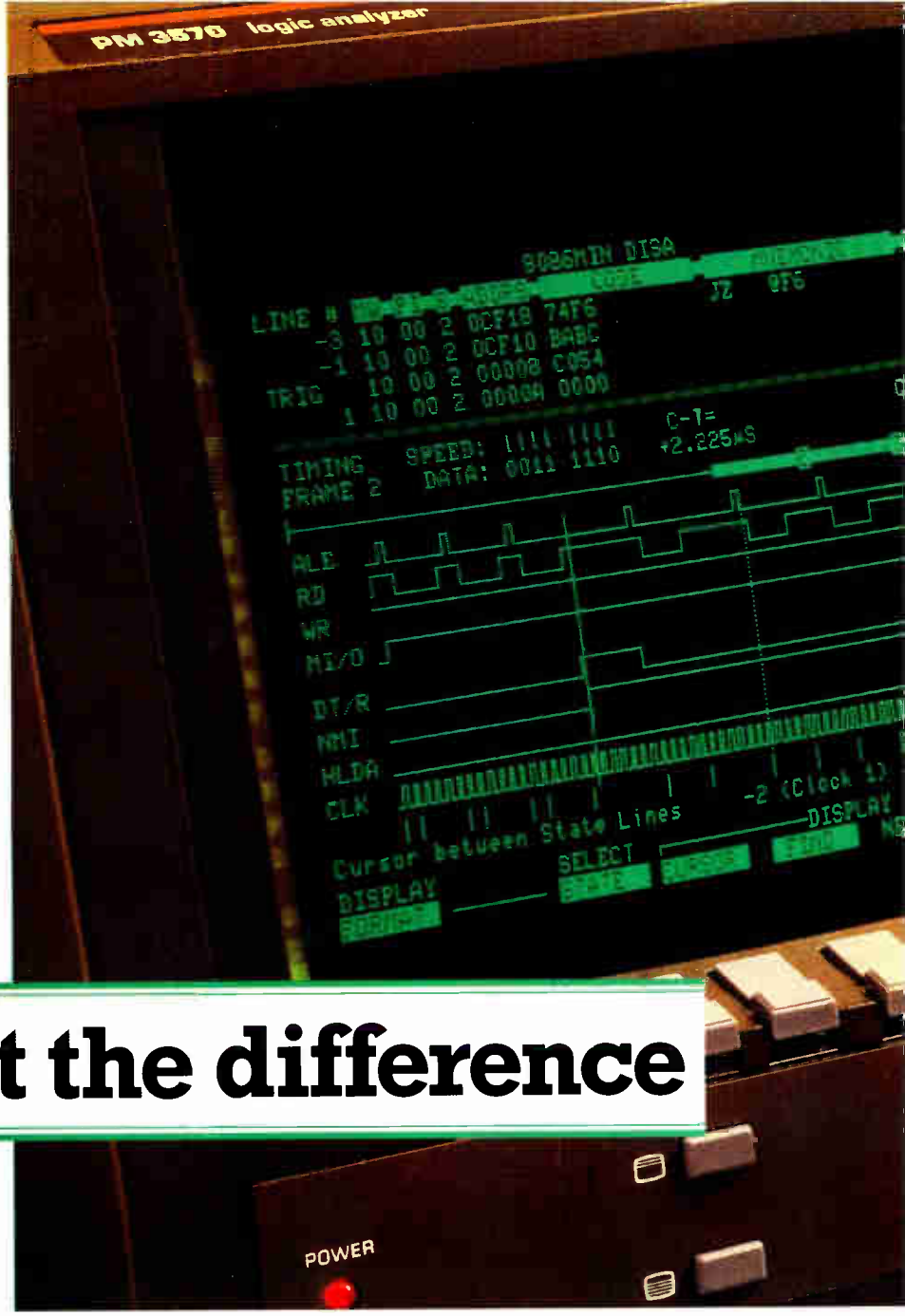
Double your logic analysis capability!

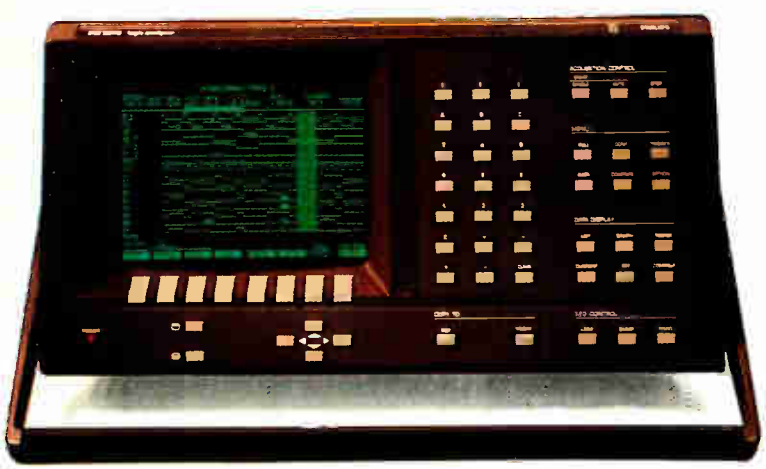


The new PM 3570 Logic Analyzer featuring the dual-screen mode allows you to perform time-correlated state and timing analysis with no less than 115 channels simultaneously. Built-in performance analysis permits system optimization. Other special features include:

- 83 state and 32 transitional timing channels for simultaneous, time-correlated acquisition at speeds up to 400 MHz! Or you can combine them for an unprecedented 115 channels of state acquisition.
- Microprocessor support for 8, 16 and 32 bit analysis plus a wide range of adaptors including: 40-, 48- and 64-pin dual-in-line (DIL) as well as 68- and 114-pin grid array and 68-pin leadless chip carrier (LCC) versions.
- Softkey operational simplicity for step-by-step entry, and non-volatile memory for storage of instrument set-ups and measurement data.
- Product credibility in technology, technique, quality and service because the PM 3570 is backed by the vast corporate resources of one of the world's largest electronics companies.

Test the difference

A simpler configuration, the PM 3565, handles up to 75 channels including 59 state and 16 transitional timing channels with speeds up to 300 MHz.



Test the difference and you'll also agree that Philips wins on price and performance!

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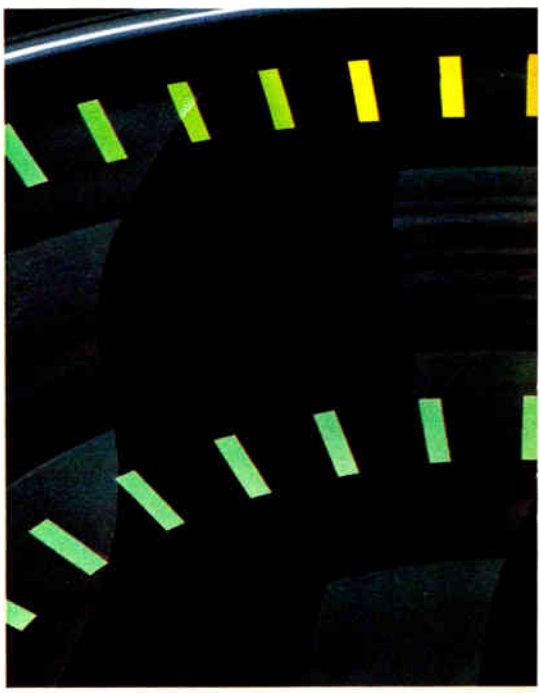
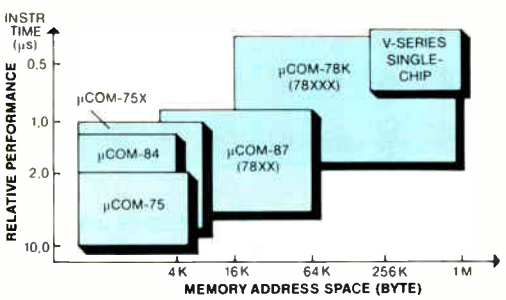


If real-time control applications are your business, there's now an easy way to get ahead: NEC's new high-performance 8-bit CMOS single-chip microcomputer with 16-bit speed and power.

The μPD78312 has all the features to turn your designs into uncompromising solutions—on time and within budget.



A single-chip device with a cycle time of 0.5 μs, it bridges the gap between NEC's 8-bit μCOM-87 products and the V25 microcomputer. Memory capacity on-chip is 8 Kbyte ROM and 256 byte RAM, with 64 Kbyte of external memory possible.

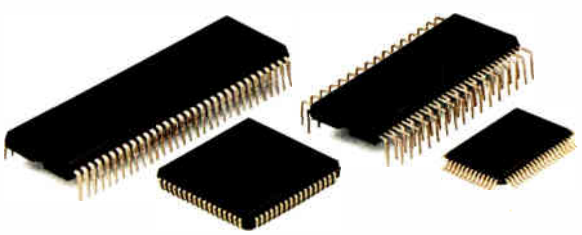
The μPD78312 features a true 16-bit CPU and bus architecture, plus dedicated hardware blocks for streamlining real-time control applications. Enhanced interrupt capabilities include interrupt service handling, context switching, and a macro service facility. Specially designed for

World Radio History

ad start

Real Time omputer

control applications, the instruction set is ideal for high-speed arithmetic and logic operations. The μPD78312 is easily integrated into office and industrial automation systems, as well as automotive systems. Packaging options ensure flexibility in device mounting, while CMOS technology keeps power consumption to a minimum. In short, if you're after state of the art silicon, backed up by one of the world's leading electronics innovators, NEC's μPD78312 may well be exactly what you are looking for.



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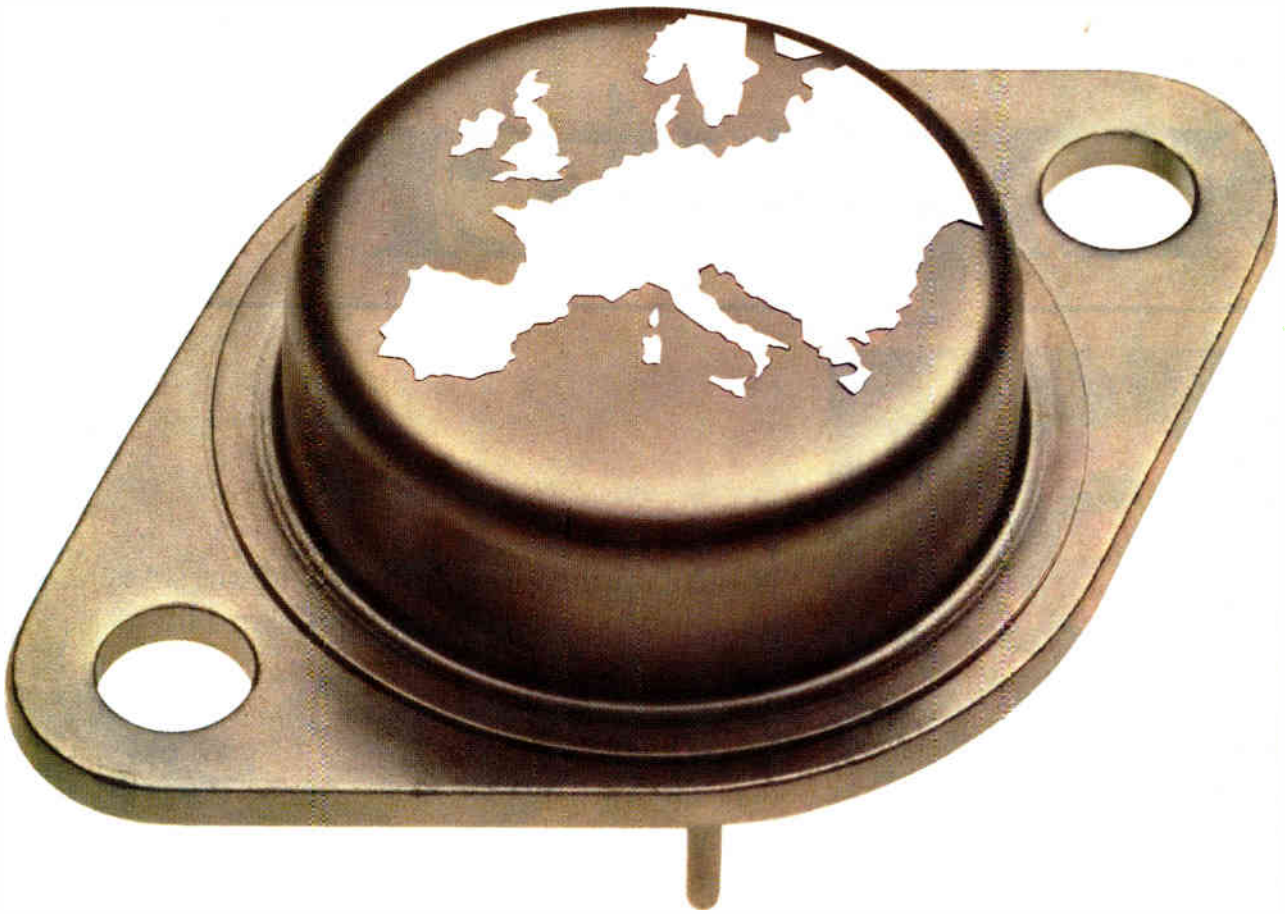
For The Best In Power Transistors Call The European World Power



Now the European world power is becoming even more powerful. An extensive 4 year investment program in power transistor production, backed by an expanded pan-European commercial network, has won SGS a major slice of the European power transistor market. And an aggressive product expansion program now aims to put the European power at the very forefront of the world's markets.

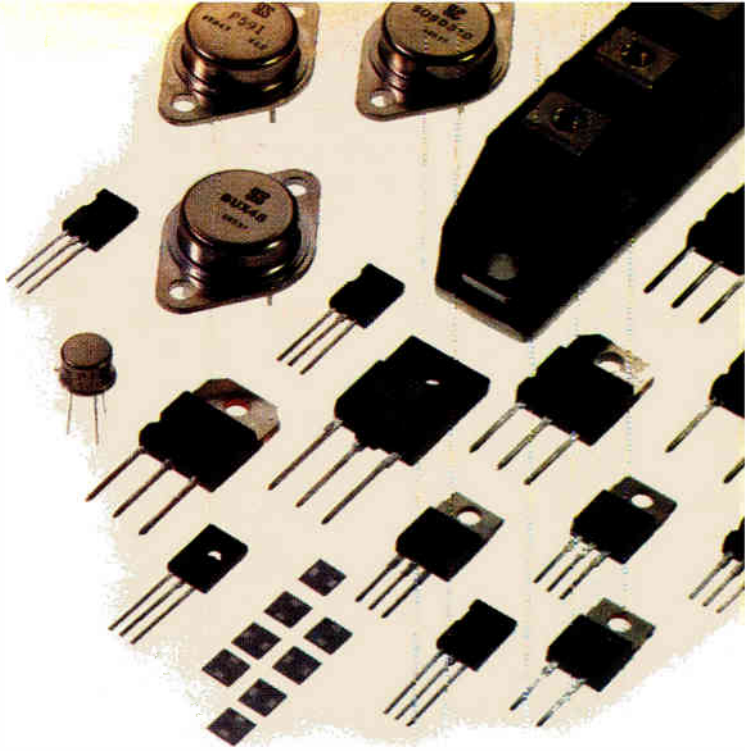
World Radio History

POWERFUL PRODUCT RANGE

Breaking the "1000 type" barrier in 1984, the SGS Power Transistor range is growing at more than 3 new types a week to cover all aspects of power technology.

DMOS transistors for ultrafast switching applications, proprietary FASTSWITCH bipolar devices for 50W to 500W off-line switching power supplies and the SGS TRANSPACK 35kVA power modules are just some of the powerful solutions developed and made for you in Europe - and there's more.

SGS, with its ISOWATT218 isolated package, aims to be the first western manufacturer to offer "user friendly" replacements of the TO-218/SOT-93 or TO-3P medium power devices. And a new range of fast epitaxial diodes up to 1200V breakdown and 50A rms. complement the faster switching power transistors now being designed-in.



Over 1000 devices with a wide range of packages offers the optimum trade-off between economy and performance for all your applications.

COST EFFECTIVE

Price, Performance, Quality and Service are the four main elements of truly cost effective power transistors. SGS is the European supplier with the most significant presence on worldwide markets to give the levels of production volume that translate into lower costs, and we've enhanced this with investments in advanced 5" diffusion facilities for power transistors. SGS' advanced silicon and packaging technologies guarantee you the best in power transistor performance, while with 100% in house epitaxial growth,

100% in-house epitaxial growth gives SGS complete quality and process control from the very start of production.

the key to all modern power transistors, SGS has complete quality and process control from the very start of production.

And Service?

RIGHT HERE IN EUROPE

SGS is right here in Europe with full production and a pan-European marketing organisation. What's more, SGS has a dedicated team of more than 100 engineers and technicians working on R&D in the power transistor field. This expertise too is right here in Europe working on your future needs in power technology. A concrete example of the teams' success is the reachable cost and ready availability of the FASTSWITCH series of 1000V ultrafast switching transistors. Compare these to the 500V power MOS offered by our American competition and you'll see why the European power means technology and service.

The European World Power.

SGS Technology ® and Service

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Circle 122 on reader service card

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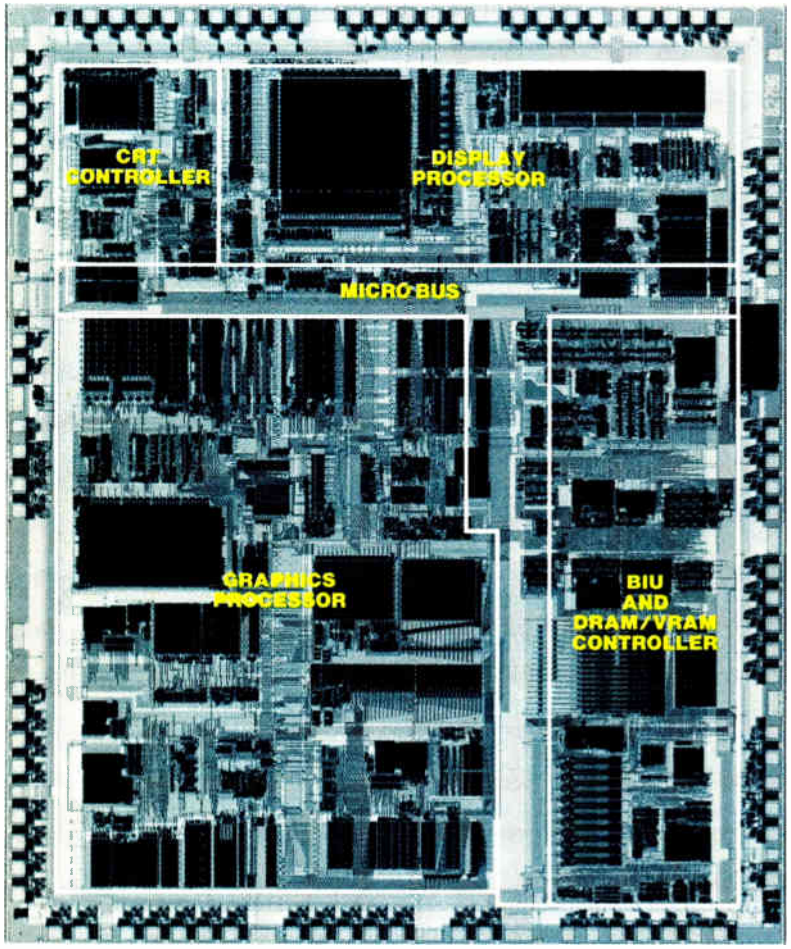
DOES WINDOWS.



Intel's 82786 graphics coprocessor supports its family of 16- and 32-bit central processing units.

"Two completely different kinds of end customers seem to be fueling the embryonic graphics chip market: the personal computer user in business, and the designer on a work station. Intel Corp., long reported to be developing a graphics-oriented microprocessor, is finally announcing its 82786 graphics coprocessor for both applications.

Demand for multiple-windowing capability is on the rise, especially for multitasking chores in the office environment. The 82786 implements this capability in hardware. Each application can have its text and graphics drawn into separate regions of memory, which are then combined within windows of the same display. Large amounts of overhead associated with graphics tasks can be offloaded from the main system CPU by storing more text and graphics information in memory than is shown in the display..."

Excerpted from an exclusive article in the May 19, 1986 issue.

McGraw-Hill Electronics

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KALOV GOES FOR SINGLES, NOT JUST HOME RUNS

CHICAGO

As a kid growing up in government-subsidized housing in Chicago during the 1940s, Jerry Kalov used to play baseball in the tough inner-city leagues. One thing he learned was that to win consistently, you can't always swing for the fences.

And when Kalov, now 50, took over as president of Chicago-based Dynascan Corp. in April 1985, one of the first things he did was to apply that bit of wisdom to the consumer electronics business. By doing so, he's gotten impressive results for Dynascan, marketer of the well-known Cobra brand of imported products that include citizen's band radios, cordless and corded telephones, phone-answering machines, and radar detectors.

Dynascan has seen a dramatic turnaround since Kalov transformed it from a company that focused on home runs to one he says will concentrate on singles. That means Dynascan will broaden its business by aiming for multiple niche markets that can contribute $5 million to $10 million each in annual profits. "You can capitalize on the occasional home run when it comes," Kalov says. "But the trick is that you don't let it dominate the company."

The numbers in Kalov's 16 months as president tell the story. Gross profit margins have climbed from 16.2% in the first quarter last year to 27.3% in the three months ended June 30, 1986. Dynascan turned in $1.8 million in profits on sales of $63.6 million during the first six months this year, and has made money in every full quarter since Kalov arrived a year and a half ago. That's not bad for a company that in late 1984 was in the worst slump of its 31-year history, when sales dipped by 28%, to $125.2 million for the year, and the firm recorded its first loss ever, dropping $16 million. Last month, Dynascan's board of directors elected Kalov to the additional post of chief executive officer on the same day the firm reported its sixth straight improved quarter.

His niche strategy is turning Dynascan around

Kalov's style contrasts starkly with the company's previous strategy. Dynascan got into trouble because it relied too heavily on 1983's hot market in cordless phones, only to see the bottom drop out in 1984. When that happened, on the heels of a similar but less devastating drop in CB radio sales, Dynascan's co-founder, board chairman, and then-CEO, Carl Korn, recruited Kalov to help stop the up-and-down trend.

KALOV. Profits have climbed in the 16 months since he took over as president.

In Kalov, Korn got exactly the kind of executive he was looking for. A 28-year veteran of the consumer electronics industry, the high-school-educated Kalov has seen the business from a number of perspectives. Since his first job as a sales representive for a small Chicago electronics manufacturer, Kalov has done everything from running his own retail chain to managing the day-to-day operations of electronics concerns larger than Dynascan. He formed his own Los Angeles-based venture-capital and consulting firm in 1983. Before that, he served as president and CEO of loudspeaker manufacturer JBL Inc., and as senior officer of International Jensen Inc. At the latter, he was credited with turning a lackluster, $8 million business into a company with annual sales of more than $100 million in 10 years.

Kalov stresses that the changes at Dynascan grow out of his close working relationship with Korn, who is now board chairman. Those changes are far-reaching. Dynascan now emphasizes diversification rather than volume. Where once cordless phones and CB radios dominated sales, the company now sells a broad range of higher-quality better-positioned products. No single category accounts for more than 25% of sales.

At June's Summer Consumer Electronics Show in Chicago, Dynascan un-

Thorton F. Bradshaw, Chairman, RCA

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WHERE THE FUTURE IS AN OPEN BOOK

veiled plans for a fourth-quarter entry into a new market: high-frequency radio scanners. And Kalov promises forays into other new niches will come.

Dynascan may not be able to avoid financial downturns of the kind that have plagued it in the past, when business in a hot consumer category suddenly turns sour, says Richard Singer, a limited partner with Mesirow & Co., a Chicago-based investment house. But by spreading the risk among many product categories, Kalov has ensured that "when a business [category] goes down, it won't hurt Dynascan as in the past. What Jerry Kalov has done," says Singer, "is change the company from one that used to just grab the tail of a tiger and hang on to one that is much more disciplined today." *–Wesley R. Iversen*

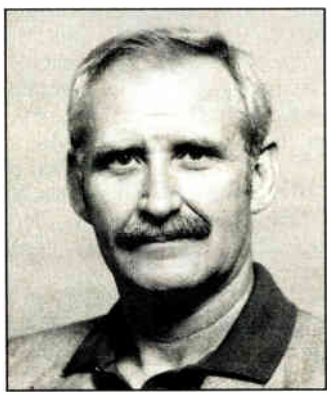
WHY LATTIN LEFT INTEL FOR LOGIC AUTOMATION

PORTLAND, ORE.

Take the excitement of new technology, add the challenge of running a startup company, leaven the mix with the good life in Oregon, and you have the blend that lured William W. Lattin to Logic Automation Inc.

As the new president of the Portland company, the 46-year-old Lattin will run a startup that produces simulation models for system designers. He brings to the job two decades of experience in VLSI design and production, computer-aided design, and engineering management at Intel Corp. and Motorola Inc.

"The 32-bit microcomputer is going to stimulate the growth in the simulation market," says Lattin, explaining his move to this technology. "The availability of that much computing power on a desktop is going to encourage much more circuit simulation than is currently being done. This means that there will be increasing need for software models of VLSI devices."



LATTIN: "The 32-bit microcomputer will encourage simulation."

Besides Logic Automation's burgeoning technology, the company's Oregon location sealed his decision, says Lattin, who moved to the state while working for Intel. "In the time since I've been in Oregon, a number of opportunities have come my way," he says. "In the last couple of months I got more interested in making a change.

"I knew my job at Intel really required that I be down [at company headquarters] in Santa Clara if I was to do it the way I felt it should be done. But at this point in my life I wanted to stay in Oregon," says the native of Callaway, Neb. "Of the several different opportunities that I looked at, Logic Automation was the most attractive."

The two-year-old company's healthy growth—it expects sales of $1 million to $2 million this year, up from $400,000 last year—helped make it attractive. But just as important to Lattin is the company's mix of the talents needed to do software models successfully, he says. "There are a number of ex-chip designers, some personal computer designers, and some software people—what you need to make this kind of product fly." He also sees a chance to renew some old acquaintances: "There are a number of ex-Intel people at the company whom I look forward to working with again."

Lattin served Intel in a number of key posts. He arrived there in 1975 from Motorola Semiconductor Products in Phoenix, where he started in 1969 after getting his BSEE and MSEE from the University of California at Berkeley and his PhD from Arizona State University. When he left Motorola he was MOS engineering manager, responsible for microprocessors, memories, CMOS, CAD, and quality engineering.

On joining Intel, he started the company's component CAD program. The next move was to Oregon as program manager for the Advanced Microcomputer System; that finished, he was named general manager for the OEM Microcomputer Systems Division.

Lattin ran that division for three years. In 1983, he became vice president and general manager of the Systems Group, including operations in Phoenix, Texas, Puerto Rico, and Singapore.

At Logic Automation, Lattin can build the kind of company he wants. Says James Morris, chairman, the company founder and the president until Lattin was hired: "When you have a startup, an essential ingredient is a president with that kind of experience. We knew we had to build a strong management team. Bill is the man who now makes this effort complete." *–Jonah McLeod*

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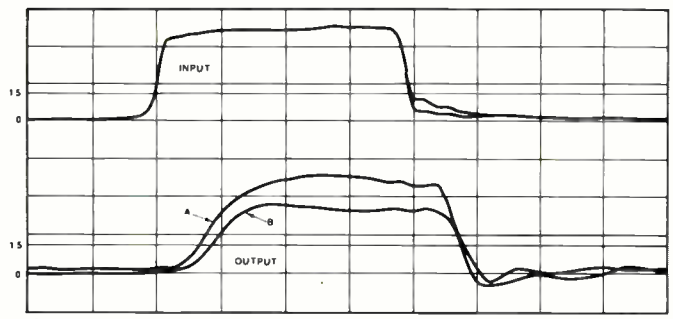
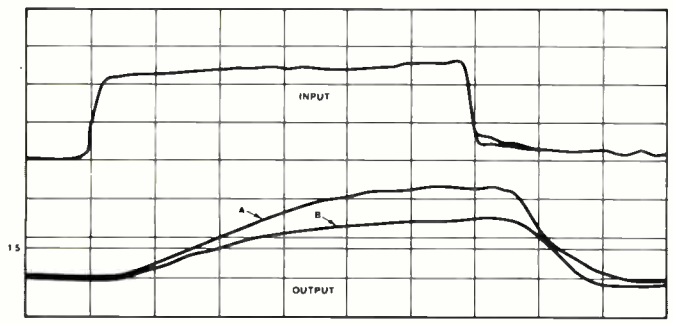


A = Performance's CMOS octal transceivers B = Advanced Schottky TTL bipolar



Performance's CMOS octal transceivers out-pace advanced Schottky TTL bipolar devices while driving a 50 picofarad load (top) and a 300 picofarad load (bottom). That's Performance!

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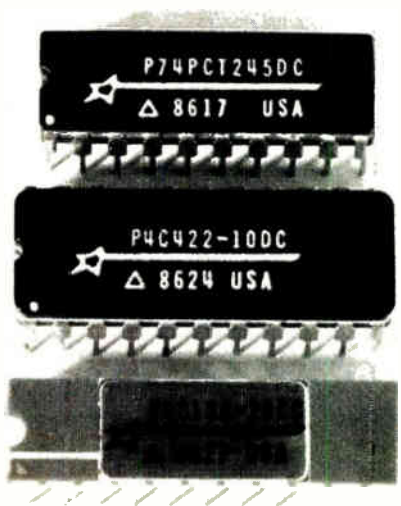

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ELECTRONICS NEWSLETTER

LATTICE DENIES INFRINGING ON MONOLITHIC MEMORIES' PAL PATENTS

Lattice Semiconductor Corp. promises a vigorous response to the patent infringement suit brought against it and Altera Corp. by Monolithic Memories Inc. MMI claims that its basic programmable-array-logic patent covers the programmable-logic devices the other two make. Not so, says Lattice; it alleges that MMI is using the suit to try to overcome Lattice's lead in CMOS arrays. Lattice says it will countersue, claiming market interference and seeking damages. MMI invented PAL architecture and is the acknowledged market leader, with 40% of a $300 million market. The Santa Clara, Calif., firm says it won a ruling from the U. S. Patent and Trademark Office last month that 13 of the 21 claims in its 1978 PAL patent were valid. Lattice, of Portland, Ore., and Altera, of Santa Clara, are young companies just beginning to make a dent in the market. However, Altera—which declines to comment on the case—has a technology-exchange agreement with Intel Corp. that covers its arrays. An MMI spokesman says his company is aware of the Intel connection but is not suing Intel at this time. □

VENDOR GROUP TO HELP CERTIFY PRODUCTS FOR DOD NETWORK

A vendors' group called the Coalition for Working Systems is forming to work with the Defense Communications Agency on a process for certifying products that implement the Transmission Control Protocol/Internet Protocol, a requirement in most Defense Department computer systems. The agency has declined to certify products itself, but wants some way to ensure that they meet military standards. The new group will probably find a home on a university campus and will use the Internet Protocol to test products, says Daniel C. Lynch. An Arpanet veteran, Lynch was picked at last month's TCP/IP conference in Monterey, Calif., to organize the coalition. Its work will in some ways parallel that of the Corporation for Open Systems, a well-heeled industry group that wants to hasten use of the International Organization for Standardization's Open-Systems Interconnection reference model. □

SOUPED-UP APPLE II RUNS THREE TIMES FASTER

Apple Computer Inc. will take to the streets to introduce its new 16-bit Apple II GS, the souped-up version of the Apple II it is to introduce this week. Apple teams will descend on shopping malls across the country for six straight weekends beginning Sept. 26, demonstrating the new machine and offering free software as an inducement to buy one. The GS runs 90% of all Apple II software, the Cupertino, Calif., company says, but is three times faster than the IIe and supports 8 megabytes of memory, all directly addressable. A basic version, with keyboard and mouse but no display, will sell for $999; with an RGB monitor and a 3.5-in. 800-megabyte floppy disk drive, it will cost $1,898. Apple will offer IIe upgrades for $498. □

COMMERCIALIZING AI PROVIDES 16,000 JOBS IN U. S.

Critics charge that artificial-intelligence companies have lagged in turning research into usable products, but apparently it's not for lack of trying—and the efforts have created a lot of jobs, says DM Data Inc. About 16,000 people are now working in the U. S. to commercialize AI technologies, according to figures compiled by the Scottsdale, Ariz., research and consulting firm. The total includes those inside large companies and those with small AI firms, but excludes anyone in the academic community, research organizations, or noncommercial projects. The largest number of workers is involved in machine vision, the most labor-intensive of AI segments, followed by expert systems, where small startup companies are proliferating. □

World Radio History

ELECTRONICS NEWSLETTER

MOTOROLA GOES AFTER SECURE-PHONE MARKET

Motorola Inc. is convinced that large businesses, particularly petroleum and industrial firms, are looking for secure communication. So the company's Communications Sector in Schaumburg, Ill., is bringing out a telephone digital voice-encryption box that it says can tie into two-way radio networks for secure end-to-end communications. The $5,000 telephone unit, the SVX-1000, relies on the National Bureau of Standard's Digital Encryption Standard, with optional use of a proprietary Motorola encryption algorithm. First shipments are scheduled for November. □

MULTIPROCESSOR PROMISES SUPER POWER AT LOWER PRICE

Looking for a for a more affordable way for scientific institutions to get their hands on supercomputing power, researchers at the Fermi National Accelerator Laboratory in Batavia, Ill., have developed a powerful parallel multiprocessor. It delivers supercomputer-class performance at a fraction of the cost of a general-purpose supercomputer—$350,000 versus $10 million or so. The multiprocessor was designed to to solve high-energy physics problems, but Fermi is working with Omnibyte Corp., a West Chicago board manufacturer, to apply the technology to other scientific uses, while driving down the cost. Already running is a system based on a multiple-instruction/multiple-data-stream architecture that uses 74 Fermi-designed single-board 32-bit computers. Over the next two months, Fermi plans to add 66 more nodes. Each of the processors is about equal in performance to a VAX 11/780, says Thomas Nash, head of Fermi's Advanced Computer Program. □

MODEM WITH ON-BOARD UART COMPLETES AMD PRODUCT BLITZ

The one-a-week product introductions launching 52 "liberty chips" is ending at Advanced Micro Devices Inc. The company hoped the year-long announcement blitz would help it break out of the doldrums surrounding the industry. The effort wasn't entirely successful; last month AMD departed from its no-layoff policy and furloughed 200 workers [*Electronics,* Aug. 21, 1986, p. 31]. The liberty program will wind up in the last half of September with this week's introduction of a CMOS 32-bit parallel multiplier and next week's debut of a full-duplex modem chip rated at 1,200 bits/s. The 168-pin Am29C323 32-bit multiplier will sell for $245 each in 100-piece quantities. Next week, the CMOS Am79C12 modem, with on-board UART, will be introduced at a price of $48 each in plastic dual in-line packages. With the final two introductions, AMD's liberty chip fleet consists of 18 microprogrammable controllers and processors; 11 graphics and peripheral circuits; five networking, logic, and interface components; six fixed-instruction processors; two nonvolatile memories; four static random-access memories; one dynamic RAM; two telecom chips; one programmable array logic; one bipolar custom product; and a bipolar programmable read-only memory. □

THE SAG IN THE SEMICONDUCTOR BOOK-TO-BILL RATIO IS NO SURPRISE

Don't get too upset over the latest book-to-bill report from the Semiconductor Industry Association. The three-month average declined in August for the fourth straight time but "the third quarter is normally down—this is not totally unexpected," says James Feldhan, vice president at market researcher In-Stat Inc., Scottsdale, Ariz. For the June through August period, the book-to-bill ratio stood at 0.92, down from 0.96 in the previous report. Feldhan is not worried, however. "We're forecasting fourth quarter sales growth [over the current period] of about 7%, so we really need to see some booking increases in the next several months." □

World Radio History

The INMOS 256K CMOS DRAM. Feel the exhilaration of unparalleled speed.

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IMS2800-80		43ns	80ns	146ns
IMS2800-10		53ns	100ns	176ns

Part Number	Function	Column Access Time (Max.)	$\overline{CAS}$ Access Time (Max.)	Page Mode Cycle Time (Min.)
IMS2801-60*	Enhanced Page Mode	32ns	11ns	35ns
IMS2801-80		43ns	13ns	46ns
IMS2801-10		53ns	16ns	56ns

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PRODUCTS NEWSLETTER

VLSI TESTER WITH 512 PINS RUNS AT 200-MHz RATE

Advantest America Inc. figures to establish new high ground in pin count and speed for very-large-scale integration testers with the prototype of a system it will have at its stand in early December at the Semicon Japan '86 show in Tokyo. The Lincolnshire, Ill., company's T3381 VLSI Test System can apply stimulus patterns to ICs undergoing tests through 512 pins at a rate of 100 MHz, and double that rate by multiplexing. Most competitive VLSI testers run at rates below 100 MHz and have no more than 300 test pins. Advantest announced the tester at last week's International Test Conference in Washington, D. C. The company said prices would run between $2 million and $6 million, with deliveries scheduled to start in the second quarter of 1987. □

HITACHI'S U. S.-BUILT CD-ROM DRIVES SELL FOR LESS THAN $1,000

Watch for compact-disk read-only-memories to become a high-profile product in personal computer markets soon. Hitachi Sales Corp. of America, Compton, Calif., now has both stand-alone and built-in versions of a 552-megabyte CD-ROM drive in production for PC data-storage applications. The drives employ technology similar to audio CD players, so Hitachi can achieve economies of scale by producing both products in the same production facilities at Compton. The stand-alone CDR 1502S sells for $1,000 and the built-in CDR 2500 for $940. Both are available now and come with an interface board for connection to the IBM Personal Computer, a connector cable, and a demonstration disk. □

ZYCAD FIGHTS BACK BY OFFERING UNDER-$40,000 LOGIC SIMULATOR

Zycad Corp., a front-runner in hardware accelerators for logic and fault simulation, plans to fight back against a growing cadre of competitors by shifting to a new architecture for a line of low-priced end-user systems. The five-year-old St. Paul, Minn., company designed its Magnum line of accelerators from the ground up to work directly on integrated circuits created using popular packages such as Cadat, from HHB Systems, Mahwah, N.J. As a result, there is no need for users to write special interfaces or to have Zycad's proprietary Zilos front-end computer-aided-design and interface software to run the simulation. Hosts can range from engineering workstations through Digital Equipment Corp. VAX minicomputers and up to IBM mainframes. Zycad's current line of end-user products ranges from about $95,000 up to $2.5 million, but prices for the new line will run much lower: from $38,000 to about $100,000 for logic and fault simulation performance equivalent to 25 million to 100 million instructions/s on up to 64,000 gates. The Magnum is scheduled to be unveiled at the Automated Design and Engineering for Electronics Show in Boston late this month. □

MOTOROLA "CORE" MODULE PACKS AN 8-USER 32-BIT MICROCOMPUTER

Original-equipment manufacturers who want to build systems around a 32-bit microcomputer can turn to Motorola Inc. for a fast start. The firm's Semiconductor Products Sector in Phoenix can deliver now a $19,945 "core" module—an 8-user VMEbus system that combines a 16.67-MHz MC68020 processor, an MC68881 floating-point coprocessor, 16-K bytes of instruction-/data cache memory, System V/68 software, 2 megabytes of dual-ported DRAM, and an intelligent serial communications controller. Mass storage is provided by a 70-megabyte Winchester disk, a 655-K-byte floppy disk, and a backup streaming-tape unit. Supplied in a 19-in. rack-mountable chassis, the SYS1131UY341 has 12 card slots and a 400-W power supply. Available for U. S. delivery only; quantity discounts apply for OEM buyers. □

World Radio History

PRODUCTS NEWSLETTER

SENTRY'S RAM TESTER CAN RUN 32 CHIPS AT 50 MHz

Watch for the temperature to rise in the random-access-memory test market, now that the Sentry Test Systems Division of Schlumberger Ltd. has added to its line a tester that can run through 32 dynamic RAM CMOS chips at a time, working at a full 50-MHz test rate; previously, 16 chips was the maximum for testing in parallel. The new S90 is aimed at devices fabricated with submicron geometries, such as the 256-K static RAM and 1-Mbit dynamic RAM. There are four test heads, each of which can probe eight DRAMs or four SRAMs. Systems start at $250,000, going up to some $600,000 for one that can test 32 chips in parallel. "The price tag is very reasonable, considering that it costs only $19,375 per test site," said Bob Evans, marketing manager for the line, at its introduction last week at the International Test Conference in Washington, D.C. The San Jose, Calif., company plans to start shipments in the first quarter of 1987. □

VISION PROCESSOR ON-A-BOARD GOES FOR $10,000

Cognex Corp. has packaged a complete low-cost vision processor on a 13-by-15-in. board and expects it to catch on with original-equipment manufacturers and systems integrators. The Needham, Mass., company claims that the 2000/VP offers all the hardware and software functions of packaged systems, although it sells for as little as one-fourth the price of competing systems—less than $10,000 per board in quantities of 50 or more. The 2000/VP is also sold as part of the company's latest vision system, the $40,000 Cognex 2000, which includes a development system for customizing applications with the 2000/VP, a floppy-disk drive, solid state camera, 13-in. monitor, incremental C compiler, and vision and communications software. The Cognex 2000 features 2 megabytes of dynamic RAM and a resolution of 516 by 448 pixels. □

TI'S CMOS DIGITAL SIGNAL PROCESSOR RUNS AT 6.4 MIPS

A total of 6.4 million instructions per second can be executed by a new high-speed version of the TMS320C10 digital signal processor that Texas Instruments Inc. will introduce this week. The CMOS part operates with a maximum clock rate of 25.6 MHz and is fully compatible with the standard 32010 n-channel part, whose top speed is 25% slower. Despite its speed advantages, the CMOS chip has a typical current drain of 35 mA, about one-fifth the power dissipation of the 32010. In 100-piece quantities, the 320C10-25 sells for $60 each, housed in a 40-pin plastic dual in-line package. At the same time, the Dallas firm will expand its linear CMOS line with two new timers and two new differential comparators. Both operate off a single power supply as low as 1 V. □

TEKELEC USES 68010 PROCESSOR TO DRIVE ISDN DEVELOPMENT SYSTEM

Tekelec Inc. will unveil next week a third-generation protocol test-and-development system based on Motorola's 68010 microprocessor. Aimed at designers of integrated services digital network systems who need to simulate operating environments and to test responses, the Chameleon 32 interfaces with telecommunications channels running at the primary ISDN rates of 1.544 megabits/s and 2.048 megabits/s. The system includes a high-resolution color CRT from Sony Corp. that can display up to 15 screens simultaneously, and it runs on M-TOS, a real-time multitasking operating system. The 40-lb, transportable Chameleon 32 costs between $22,000 and $30,000 and is aimed primarily at research labs, but the Calabasas, Calif., company expects it to sell in the communications network market as well. □

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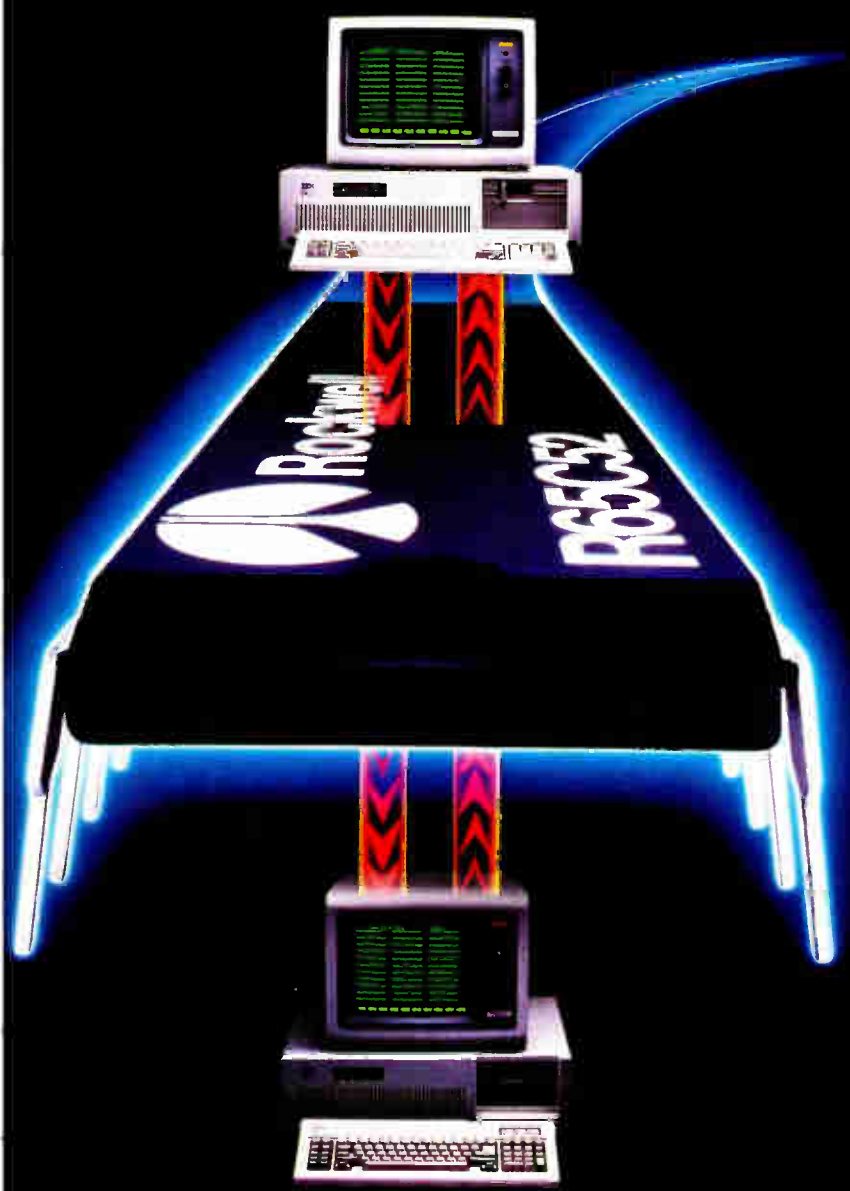

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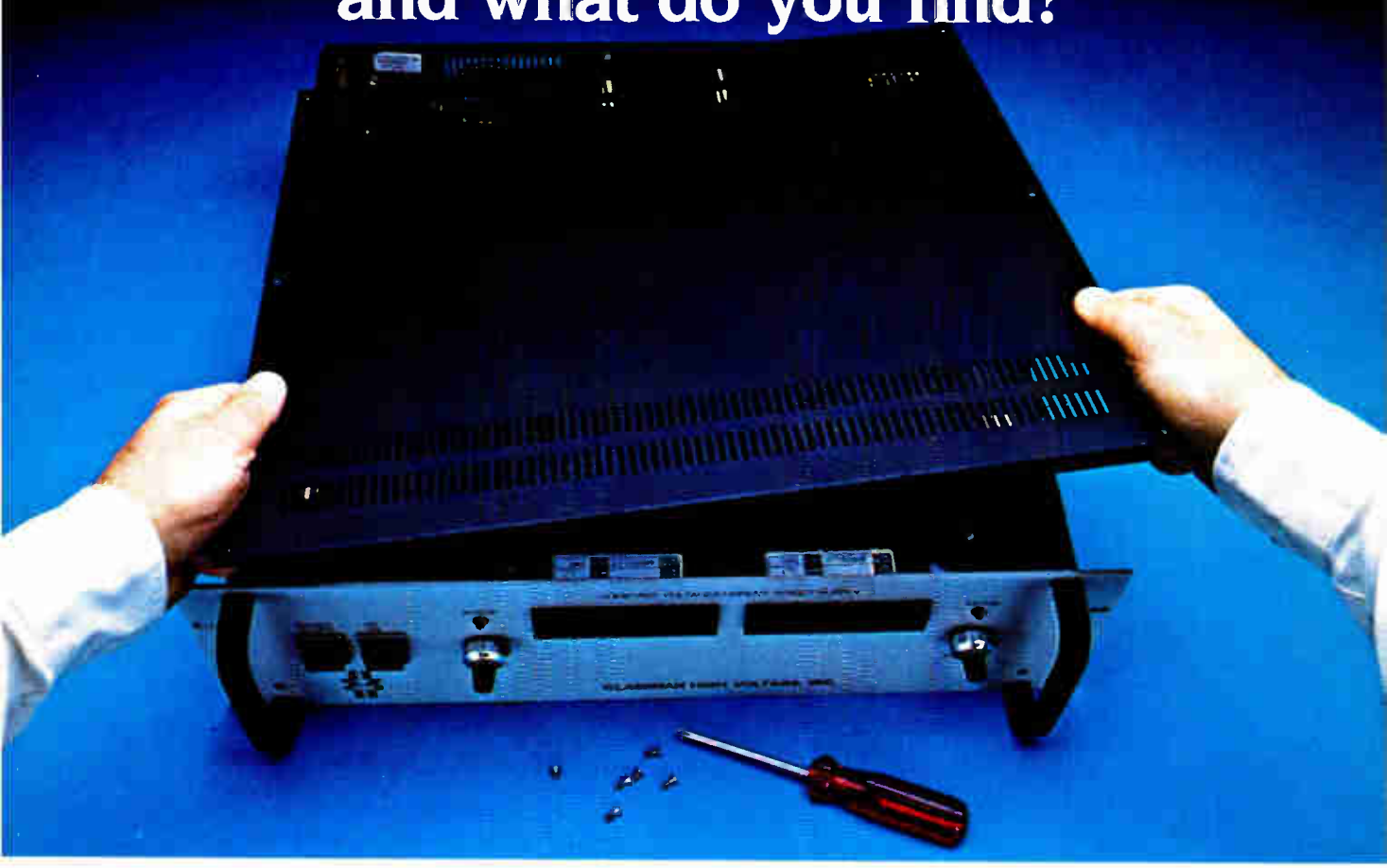

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Electronics

TI BUILDS 1-K STATIC RAM IN GaAs-ON-SILICON

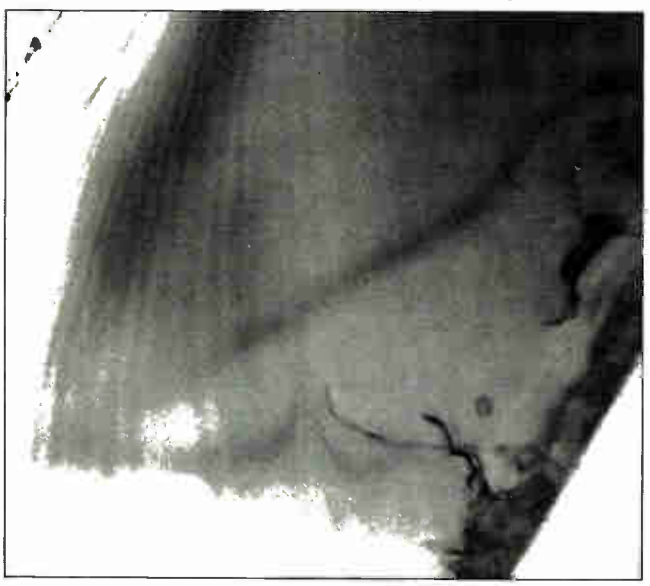
PROMISING MARRIAGE OF MATERIALS PROVES ITSELF AT LSI LEVEL

DALLAS

The promising but ticklish marriage of gallium arsenide and silicon on a single semiconductor chip appears to be passing the test of large-scale integration. Fully functional 1-K static random-access memories with address-access times as short as 6 ns have been fabricated on GaAs-on-silicon wafers in the research labs of Texas Instruments Inc., Dallas.

TI's experimental GaAs-on-silicon circuits are believed to be the most complex working integrated circuits ever made from the combination of the materials. The 1-K SRAM has more than 7,500 transistors, compared with no more than 50 transistors in previously reported ring oscillators made with GaAs-on-silicon wafers at other research facilities over the past year.

Several key developments have been combined by TI materials scientists to keep crystalline defects, which result from the mismatched lattices of silicon substrates and the grown GaAs, away from the critical wafer-surface region. These include the molecular-beam epitaxy equipment used to make the GaAs-on-silicon wafers and a combination of high- and low-temperature processing. In addition, the wafers were made to withstand the rigors of normal LSI processing.



CONFINED. Lattice dislocations in the GaAs layer TI has grown on silicon are confined to a layer (lower right) just above the silicon.

The GaAs-on-silicon chips represent a major step toward moving the technology out of the lab and to the fabrication line. TI will report on the chips at the International Symposium on GaAs and Related Compounds, which begins Sept. 28 in Las Vegas.

To measure the feasibility of manufacturing the chips, TI researchers have made the GaAs-on-silicon memories with the same processing steps and circuit designs that the company is now using to prototype bulk-GaAs 1-K SRAMs under a separate development contract with the U. S. Air Force. Preliminary pattern testing indicates that all 1,024 bits on the devices are working. Access times are 6 to 14 ns, compared with the 4 to 12 ns of identical SRAM circuits made on conventional bulk semi-insulating GaAs wafers, says Hisashi Shichijo, senior technical staff member in TI's GaAs logic and memory branch of the System Components Laboratory. Power dissipation for bulk GaAs and the new GaAs-on-silicon SRAMs are about the same, at 500 mW.

"Unless you can show that this material can be used in actual devices, the excitement will not grow," says Shichijo. "Now we are getting very good results, and the 1-K SRAM will encourage a lot of people to apply other devices."

Growth of device-quality GaAs-on-silicon opens up many avenues in device fabrication. One aim is to merge the high electron mobility of GaAs with the high-level integration capabilities of silicon. Long-term hopes include a new breed of ICs combining silicon-based digital circuits with GaAs optoelectronics used for light-based interconnections.

In the near term, the research is likely to help pave the way to lower-cost, less-brittle GaAs wafers. Growing GaAs on silicon substrates strengthens it, reducing breakage in processing. As many as half of the brittle bulk-GaAs wafers break in most processing lines, according to TI researchers. GaAs devices would also benefit from the higher thermal conductivity of a silicon substrate.

With the backing of silicon substrates, GaAs wafers may also one day reach the size of today's silicon wafers, 5 to 8 in. in diameter. Today's bulk GaAs wafers are available with diameters of only 2 to 3 in.

TI has been growing experimental GaAs-on-silicon substrates for about two years and has been making rapid advances in lowering defect-dislocation densities. Transistor performance in the GaAs-on-silicon material is now about 80% to 90% that of similar devices built on bulk GaAs. That compares with about 70% earlier this year.

TI, like other research organizations, is tilting the silicon wafer 3° to 4° before layering GaAs on top. This tilting helps compensate for misalignment of Ga and As atoms resulting from Si substrates that are not smooth at the atomic level. Abutting Ga and As atoms create unwanted antiphase boundaries that are electrically active with localized fields. Tilting also seems to help compensate for a mismatch of atom spacings in GaAs and silicon crystal lattices. In GaAs, 25 atoms are packed into the space taken by 24 atoms in silicon. The one missing plane of atoms in every 25 planes can cause a dislocation in the GaAs crystal.

Not all of the dislocations can be eliminated by the tilt, however. Therefore, TI researchers are combining low and high processing temperatures to confine any dislocations that appear to a narrow buffer layer at the interface of the GaAs and silicon (see photo).

Other researchers have attempted to reduce the strain of lattice mismatches with superlattice layers, but TI did not do this on the wafers it used for its

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SRAMs. Instead, the mixed-temperature process redirects dislocation lines so that they will not reach the surface of the GaAs layer, where active devices will be fabricated. Many of the dislocations are diverted to run parallel with the silicon-GaAs interface inside the 0.2-to-0.3-μm buffer layer, says Jhang W. Lee, developer of the technique and a member of the technical staff in TI's Materials Science Laboratory.

Lee also developed a process that greatly reduces warping of the outer GaAs surface. The surface of TI's 2-in. GaAs-on-silicon wafers varies only 1 to 5 μm from the edge to the center, compared with as much as 55 μm in other processes, adds Lee. The surface region of the grown GaAs, which is about ½ μm thick, has a dislocation density of $10^6/cm^2$ to $10^5/cm^2$. Bulk GaAs has a rating of between $10^4/cm^2$ and $10^5/cm^2$.

In industry and university labs, other researchers are also putting GaAs-on-silicon through test fabrication runs. At GTE Laboratories Inc. in Waltham, Mass., for example, researchers are gearing up to make small gate arrays, ring oscillators, and other simple metal-semiconductor FETs using GaAs grown on silicon by metal-organic vapor-phase epitaxy, which has certain advantages over molecular-beam epitaxy.

"While there has been work in MBE, we take the position that metal-organic vapor-phase epitaxy will be the way to scale up manufacturing, because this technique doesn't have the high vacuums, purity requirements, and low throughput of MBE," notes Leslie A. Riseberg, director of the Electronics and Photonics Laboratory at the GTE center. Under an Air Force contract, the lab has already made MES FETs and test structures.

Similar work is also being done at Oki Electric, Fujitsu, NEC, and NTT in Japan. In the U. S., research is underway at Bell Laboratories, Ford Microelectronics, Xerox, Hewlett-Packard, Honeywell, and startup Kopin Corp., Taunton, Mass. *–J. Robert Lineback*

TRADE

SYSTEM HOUSES OUTRAGED BY TRADE PACT'S EFFECTS

PALO ALTO, CALIF.

The brand-new semiconductor trade agreement between the United States and Japan is under fire before the ink has dried. On the attack are U. S. computer and systems makers who have been stung by the immediate results of the pact: price rises of as much as 600% and the outright disappearance of some vital Japanese memory chips.

At a meeting hastily arranged here early this month by the American Electronics Association, some 60 angry manufacturers told aides from the U. S. Department of Commerce and the U. S. Trade Representative's office that the agreement the latter had struck with Japan was ruinous to U. S. systems houses and, adding insult to injury, provided a bonanza for Japanese semiconductor makers that could fuel further Japanese advances in technology.

Unappeased by reassurances from the government, the computer executives pressed for, and got, further high-level meetings last week with Commerce Secretary Malcolm Baldrige and deputy U. S. Trade Representative Michael Smith. This time, they got a more detailed briefing on how the pact is to be implemented, a hint that price fluctuations would smooth out when new prices are set for Japanese dynamic random access memory imports Oct. 15, and a promise that they would be consulted before any new actions were taken.

ENFORCEMENT. To provide that consultation, the AEA will organize a task force that will have access to Department of Commerce data on how prices are calculated and how the agreement is being enforced in third countries. The latter is a sore point with U. S. firms, which claim that cheap Japanese memories are still available abroad.

"We were given some information about certain activities under way that would ameliorate the most serious impacts of the aftermath of the agreement," says AEA vice president Ralph Thompson, one of those who met with Baldrige. While declining to go into detail, Thompson says the industry found "a very clear awareness" on the part of Commerce and the trade office of the agreement's impact on users.

Relief from the initial turbulence is a matter of weeks away, Thompson says. It can't come too soon for the computer executives, who have been howling with rage since their suppliers told them in mid-August that not only were prices going through the roof, but that there would be a month-long DRAM drought

IS IT A PC/XT OR IS IT A PC AT? ONLY IBM KNOWS FOR SURE

The murky waters of the Personal Computer market are even murkier now that IBM Corp. has unveiled a new PC/XT. Analysts greeted the new XT-286 with befuddlement—the main result of IBM's action seems to be further blurring of the hazy boundaries between the company's midrange PC/XT and its high-end PC AT.

Just what makes this machine an XT is anyone's guess. An IBM spokesman alludes to the enclosure: "It's an XT because its basic characteristics are more of an XT than an AT when you look at it." But inside the XT-286 beats the heart of an AT—the same Intel Corp. 80286 microprocessor that gave the AT its "Advanced Technology" name in the first place.

The XT-286 runs at 6 MHz—faster than the 4.77-MHz XT and the same speed as the original AT. The current AT runs at 8 MHz. Also, IBM has equipped the XT-286 with five 16-bit expansion slots, one less than the AT has, and with three 8-bit expansion slots, one more than the AT. The basic PC/XT comes with eight 8-bit expansion slots.

IBM will sell the new machine for $3,995 (the same price as the original base-model AT) configured with 640-K bytes of main memory and a 20-megabyte hard disk, the same as the $2,895 XT. The basic AT now costs $5,295 and comes with 512-K bytes of main memory and a 30-megabyte hard disk.

The overlapping specifications don't help distinguish the new XT-286 from its siblings. "I think it's a baffling product," says IBM watcher George Colony, president of Forrester Research Inc., Cambridge, Mass. "IBM is introducing a 6-MHz AT at a time when virtually every clone out there is running at 8 MHz."

Moreover, the XT-286 will cut into sales of the PC AT in the short term, says Joe Cross of Future Computing Inc., Dallas. "It's basically a low-end AT-compatible. This is a new twist on how to update your product line—sort of like detergent: 'new and improved,'" he maintains.

Further confusing matters, Compaq Computer Corp. and Sperry Corp. immediately followed IBM, announcing new configurations for low-end AT-compatibles. As one analyst puts it, the PC-compatible market has become "hyper-responsive."

Compaq brought out the Deskpro 286-20, a model nearly identical to the XT-286 but with a 1.2-megabyte floppy-disk drive. Sperry introduced the PC/microIT, a machine like the XT-286, but with more options available. Moving upstream, Compaq also just introduced a machine based on the 32-bit Intel 80386 microprocessor (see p. 66.) *–Tobias Naegele*

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while they got used to the idea.

Some firms say only abrupt changes in the way the agreement is being implemented can prevent a mass exodus of systems manufacturing from the U. S. to Japan. "The planes are figuratively warming up on the runway," Thompson said after the Palo Alto meeting.

The moratorium on DRAM shipments was ordered by the Japanese Ministry of International Trade and Industry in order to prevent the U. S. from being flooded with cheap DRAMs before the agreement took effect. DRAM volume was voluntarily kept the same as it was in the April-June period. That was reached Aug. 15—and shipments dried up. MITI was to turn on the tap again Sept. 15.

COST-BASED. The agreement, formally signed on Sept. 2, provides for Commerce to set "foreign market values," on Japanese DRAMs and erasable programmable read-only memories, based on cost data supplied by the Japanese vendors. The Japanese firms are not supposed to sell below these prices anywhere in the world outside of Japan.

And George Scalise, government relations liaison for the Semiconductor Industry Association, says that even low-cost pricing in Japan, although not covered in the trade agreement, would still be considered a violation of the spirit of the pact and would result in the resumption of anti-dumping penalties against Japanese shippers.

The intent of the trade agreement is to shield U. S. chip makers from Japanese dumping, or selling their chips below cost in overseas markets. The pact has had no effect on the EPROM market, where U. S. firms dominate. In any case, EPROMs are a relatively low-volume part. But the DRAM market, where only one significant U. S. supplier remains active (aside from a Japanese subsidiary), has gone haywire.

The price of 256-K DRAMs has jumped from around $2 to $5 or more, depending on the supplier, and the cutoff of shipments has resulted in a frantic scrambling for parts. Some users complain that Micron Technology Inc., of Boise, Idaho, the U. S. DRAM supplier, had broken contracts and raised prices in order to cash in on the drought. (Micron denies violating contracts; it won't comment on pricing.)

Meanwhile, the price of a 1-Mb DRAM shot from $25 to between $120 and $170, and users didn't know what hit them. "We knew the agreement was crazy, but we couldn't believe what happened," says Robert J. Paluck, president of Convex Computer Corp., Dallas. "One of the most incredible results is it that it guarantees Japanese companies a dramatically bigger profit, which they will funnel into development. Our government is price-fixing for the Japanese."

Andrew Kay, chairman of Kaypro Computer Corp., San Diego, says that the price increases have boosted Kaypro's costs by $300,000 a month. Kaypro is faced, he says, with a decision to reduce the amount of memory in its computers, to increase its prices, or to move production offshore.

Joseph Parkinson, president of Micron, says the users are partly to blame for their current woes. Systems houses that find themselves hurting "should have thought about that when they were canceling orders with Mostek and Motorola and placing them with Japanese suppliers," Parkinson says.

Motorola has left the DRAM business (though it recently re-entered through the back door, by buying wafers from Japan's Toshiba Inc.). Mostek collapsed under the pressure.

The plight of the systems houses, Parkinson says, "is part of a continuing American tragedy. They think they are being rolled over now; they don't know what being rolled over is until they feel the onslaught of below-cost prices from Japan. And their turn is next; the Japanese are moving into systems products."

But some of the systems executives think that the semiconductor houses are grasping at straws if they believe the trade pact will help them. L. William Krause, president of 3Com Corp., Mountain View, Calif., says that after talking with Commerce and the trade office he is convinced that the trade agreement cannot work.

"It's a Band-Aid on a patient who is hemorrhaging from an artery," Krause says. "We have a fundamental problem: the Japanese have put together a cohesive industrial policy and we have not." Krause thinks Japanese producers really are more efficient than U. S. manufacturers because they have been able to invest in automated production equipment. He plans to form another AEA task force to study the influences on the cost of capital, and to use the results as the basis for suggesting a national industrial policy. *–Clifford Barney*

PEOPLE

WHY BOBBY INMAN IS RESIGNING AS MCC HEAD

AUSTIN, TEXAS

A new purpose has taken hold of B. R. (Bobby) Inman: he wants to help American business actually use new technologies, not just help develop the technology in the first place. Such a role is increasingly important, he feels, because the gap between newly available technology and the technology in day-to-day use continues to widen.

Inman's latest ambition has led him to resign as head of research consortium Microelectronics and Computer Technology Corp. He intends to accept a private-sector position in the next few weeks. However, he hasn't decided which one, and will serve out his 1986 term as MCC chairman, president, and chief executive officer.

NEW AIMS. MCC's Inman wants to move from research to the application of new technologies.

Inman has held the reins at MCC since the consortium began formal operations in January 1983. His decision to leave has raised worries about the impact his departure will have on the consortium. But Inman says the organization, which now has 21 members, has been structured for his departure from the start: "I came here to build it, not to operate it. It is the right time to turn it over."

Inman is weighing a variety of job offers, ranging from positions in giant U. S. corporations to investment banking opportunities that "would involve assembling a series of companies into a larger package to address some of these problems" of applying technology.

Inman says he will not take a post in government. The retired U. S. admiral was director of the National Security Agency for four years and deputy director of the Central Intelligence Agency from 1981 to mid-1982.

The 55-year-old Texan decided to leave MCC in early September, after its 1987 budget was set at $75 million, compared with a total in 1986 of $65 million. Although there were rumors of rifts between him and some MCC shareholders, Inman says his decision not to renew his contract was based on the completion of MCC's building phase.

"My sense is that [MCC's] growth has crested with the 1987 plans. It will grow with inflation or with unique opportunities, and along the way they will start additional programs—but essentially the

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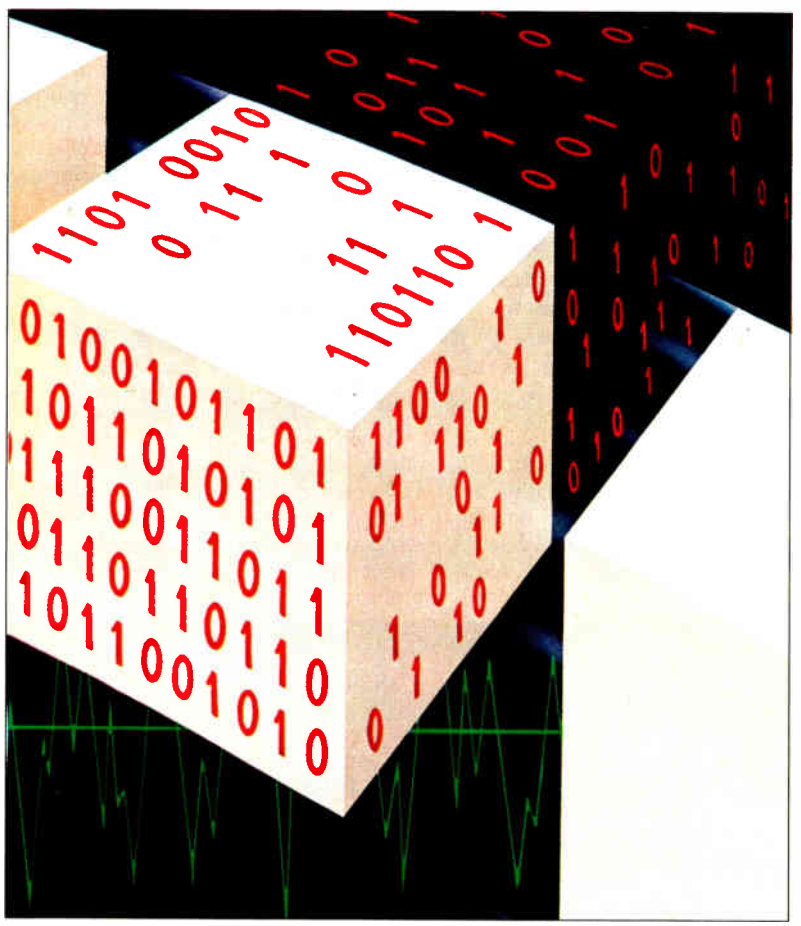
DATA GRABBER.



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Excerpted from an exclusive article in the July 24, 1986 issue.

Electronics

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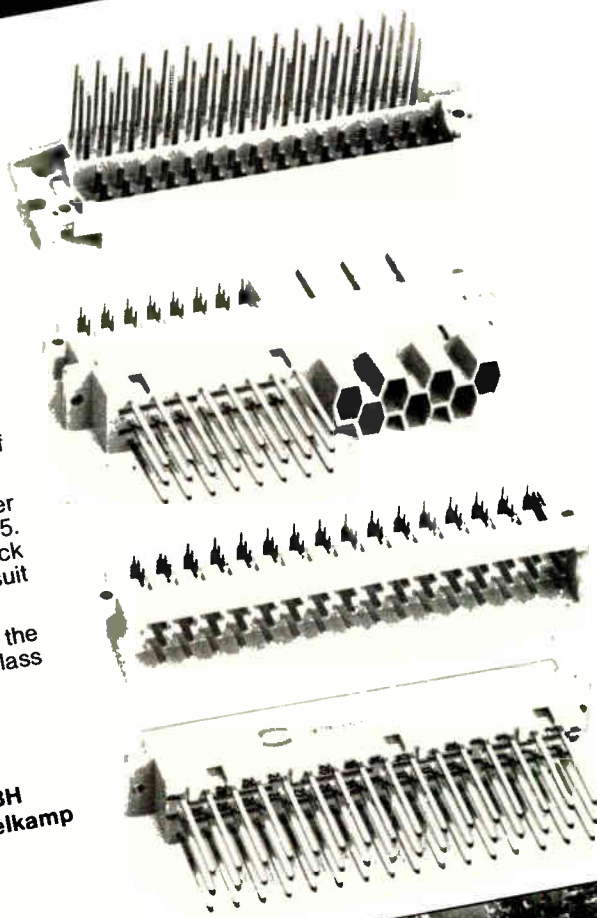

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Circle 127 on reader service card

World Radio History

building job is done," he says, adding that the staff has "awesome talent."

Inman says his interest began shifting in March 1984, when he first began to feel comfortable with MCC's staffing. "The part that has become increasingly worrisome to me is that we keep creating technology faster, and I don't see comparable changes in grappling with moving technology into products faster," Inman says.

He believes a system of quick and efficient application of new technology —similar to what he witnessed while guiding high-priority military projects— is possible in industry. Japanese manufacturers adapt quickly, he points out, and he worries about the advantages this gives Japanese companies over their U. S. counterparts. "These are the things that I have gotten interested in. Just where all that fits into what I do next is something I have yet to decide," he says. *–J. Robert Lineback*

AUTOMOTIVE

WOULD YOU BELIEVE LED BRAKE LIGHTS?

DETROIT

Automotive brake lights may soon be taking on a richer red glow. And the makers of a new breed of high-intensity light-emitting diodes may be taking on a new glow of their own if a potentially huge market for LED automotive taillights takes off.

The emergence of red LEDs that can produce light up to 10 times as intense as that emitted by conventional LEDs is making the automotive industry take a look at the devices as a replacement for the incandescent bulbs now used in brake lights, taillights, and turn signals. Significant cost barriers still remain. But recent advances in LED outputs have made the idea feasible, automakers say.

NEXT YEAR? Japanese automakers may be first to bring the technology to market. Toyota, for one, demonstrated an LED taillight on its SFXB experimental car at the Tokyo Auto Show last year. Some U. S. observers believe the first Japanese production cars to employ the technology could show up as early as the 1987 model year.

The LEDs probably will first be used in the center high-mounted brake lights that were required for the U. S. market starting with the 1986 model year. They represent an easy first target because federal standards dictate lower minimum outputs than for bumper-level stop lights and turn signals. General Motors Corp. is field-testing a center high-mounted stop lamp based on LEDs for possible use in a special-edition 1988 Corvette.

The brighter LEDs are made from aluminum gallium arsenide. Compared with the 1.5-to-2-lumens/A output of traditional red LEDs made of gallium arsenide phosphide on a gallium phosphide substrate, some AlGaAs devices can hit 15 to 20 lm/A, says Stanley R. Gage, research and development manager for Hewlett-Packard Co.'s Optoelectronics Division in San Jose, Calif.

The potential advantages of LED-based automotive stop lights are several. LEDs have a lifetime exceeding that of the average automobile, meaning that they would rarely have to be replaced. Because of their small size—typically only about 0.010 in. square and 0.003 in. deep—LEDs would also afford automotive designers much more flexibility. And the AlGaAs devices produce a monochromatic 660-to-680-nm wavelength light that is a deeper, more distinctive shade of red that some think is more aesthetically pleasing than the color produced by incandescent units.

LED-based stop lamps represent potential big business for vendors of the devices and subassemblies. Depending on the application, anywhere from 50 to 100 or more individual LEDs might be required for each automobile. By one vendor's estimate, that could eventually add up to a worldwide market approaching $1 billion annually—about equal to the worldwide market for all visible LEDs today—a prospect that is drawing a flock of would-be competitors.

In the U. S., Hewlett-Packard is pursuing the technology, though the company is not yet selling production AlGaAs LEDs. Most of the likely players are Japanese. Stanley Electric Co., a Tokyo automotive lighting supplier, appears to have an early lead in the technology, automakers say. But other suppliers, including Matsushita, Mitsubishi, and Toshiba, are also in the game.

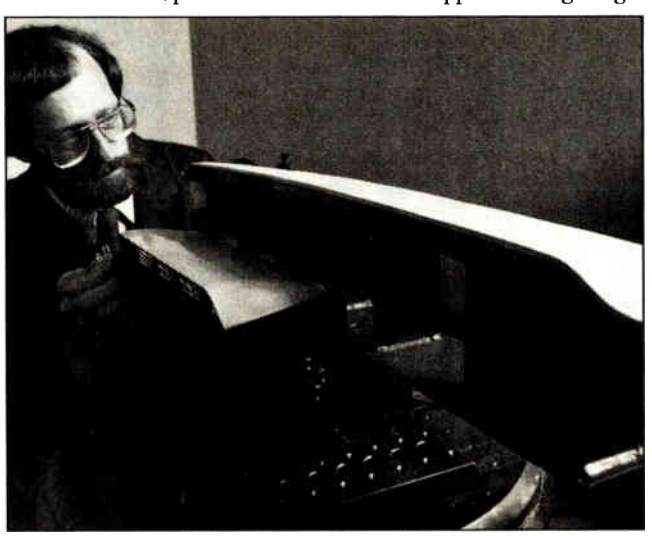
Despite the potential advantages, LED vendors must still overcome a cost hurdle if the devices are to find widespread use on cars. At current price levels, LED-based stop lamps are 2½ to 3 times more expensive than incandescent assemblies, says Gene P. Wright, the staff project engineer who heads up LED development at GM's Fisher Guide Division in Anderson, Ind.

But "as volume goes up, pricing will come down," Wright predicts. Executives at Matsushita Electric Industrial Co. agree. The Osaka firm is already selling AlGaAs LEDs made with a liquid-phase epitaxy process. Matsushita won't disclose its pricing, but executives say that as volume rises, they will be able to cut pricing to about one-fifth its present level within two or three years.

COST IS CRUCIAL. Others, however, aren't so sure about the cost picture. "In order to really penetrate the market with an LED solution, you're going to have to approach the same cost as an incandescent unit, and that's a technological challenge that I don't think has been solved yet," says HP's Gage.

The key to cutting LED-lamp pricing lies in optically focusing the LED output so as to hold down the number of devices required to meet photometric output standards, says Gage. HP is investigating "nonstandard optical approaches," he says, as well as "methods by which we could manufacture in extremely high volume at low cost."

There are indications that a market of some size will emerge soon. In response to an inquiry from Stanley Electric, the National Highway Traffic Safety Administration has approved the use of LED high center-mounted stop lamps that meet the photometric-output and other federal requirements. Furthermore, the Society of Automotive Engineers recently formed a task force to look at LED characteristics with an eye toward developing an SAE specification for LED exterior-lamp assemblies. *–Wesley R. Iversen*



LONG LAMP. General Motors Corp. is testing 27-in.-long contoured brake lights using LEDs as replacements for incandescent lamps.

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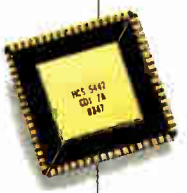

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PtSi: A NEW CONTENDER FOR IR SENSORS

LOS ANGELES

High-resolution infrared sensors, which will serve as the eyes of the next-generation of smart U. S. military gear, continue to get top research attention from a select—and competitive—circle of suppliers. Choosing the best material is a critical matter, and so far mercury cadmium telluride and indium antimonide have garnered the lion's share of funding. But now GM/Hughes Electronics Corp. is moving to promote a third material, platinum silicide.

The emergence of PtSi is marked by its use in the focal-plane array sensor of the IR seeker element of the Army's proposed Fiber Optic Guided Missile. The new sensor-array prototype, said to be not only the first such device packaged as a tactical missile seeker but also the first flight-quality imaging IR seeker received for testing by the Army, is the work of GM/Hughes Electronics Missile Systems Group, Canoga Park, Calif. It is a very large-scale integrated circuit with 65,536 IR detectors in a 256-by-256 mosaic arrangement. The Army's Missile Command will flight-test the seeker on FOG missile at Redstone Arsenal, Huntsville, Ala.

VOLUME LEADER. If this tactical missile reaches production as a mainstay antiarmor weapon, the Army will need many thousands of the sensors, making PtSi a clear volume leader over other materials. As recently as midyear, most IR-imager suppliers regarded PtSi as an also-ran material with little potential [*Electronics*, June 9, 1986, p. 40]. However, PtSi could offer lower sensor costs than the other materials. And production yields are better, because, as a close relative of pure silicon, PtSi enjoys the benefits of the wealth of fabrication techniques developed for silicon. PtSi detectors can be built in quantity on 4-in. wafers; HgCdTe, for instance, is currently limited to 2-in. wafers.

Another advantage is that the PtSi sensors can be packaged as a hybrid with a signal-multiplexing chip, because the IR light passes unhindered through the silicon substrate on which the sensor is built. The bottom of the detector chip faces outward toward the seeker's lens, and the active side of the chip can be bump-bonded to a second chip.

The technique is similar to one long used by IBM Corp. for mounting memory chips on ceramic substrates, but in this case, two active chips are bonded. Indium bumps are formed on pads on the detector chip, and the multiplexer chip is made with a matching bump pattern. The two chips are sandwiched together, and heat is applied so that the indium bumps melt and bond.

MISSILE EYE. Hughes has delivered IR seekers with PtSi sensors to the Army for tests.

"This allows us to simplify the signal-processing electronics, which means fewer parts and therefore lower costs," says Robert A. Aguilera, Hughes sensor program manager. He notes that seeker cost is particularly important to FOG-M because each sensor is mounted on the missile and is thus expendable.

Defense Department research money so far has heavily backed HgCdTe because it works in all three of the sensing-wavelength windows (1 to 3 μm, 3 to 5 μm, and 8 to 14 μm) in which the Strategic Defense Initiative has requirements.

But Freeman Shepherd, PtSi's developer and its strongest proponent, thinks that even though his material is starting late, its conversion efficiencies for tactical sensing tasks in the 3-to-5-μm range are now as good as the others. Bump-bonding techniques and semiconductor processing advances have helped make PtSi fully as sensitive as its competition, says Shepherd, chief of the Electronic Devices Technology Division at the Air Force's Rome Air Development Center, Hanscom Air Force Base, Mass. He estimates that PtSi sensors could be cheaper by a "factor of 20" than other materials in production quantities.

SHORTCOMINGS. Companies firmly committed to the other materials do not agree. "I doubt its usefulness in the tactical environment," where smoke and haze require more sensing performance than PtSi has exhibited, says George Hopper, a senior fellow at Texas Instruments Inc. of Dallas. As for cost, Hopper points out that because chips account for such a small percentage of the total expense, "there's not much substance to the cost argument."

The competing IR materials will get a thorough test in another Army development project announced in late August, the Advanced Antitank Weapon System Missile. Hughes, Ford Aerospace Corp., and TI won $30 million contracts to demonstrate technology on this portable missile for infantrymen. TI's seeker will employ HgCdTe and Hughes's PtSi; Ford has not announced its approach.

–Larry Waller

SATELLITE SYSTEM TO CUT MARINE TELECOM COSTS

LONDON

The cost of marine satellite-communications systems should drop to about one-sixth of its current level within two years. A new system—Standard C, designed by the London-based International Maritime Satellite Organization—slashes the size, weight, and price of such systems by reducing the types of services handled.

The low-speed, data-only marine earth station could cost as little as $5,000, estimates Inmarsat, a 46-country cooperative that provides communications facilities for maritime and other mobile applications through three geostationary satellites. The Standard A marine earth stations now in use, which can handle voice, Telex, facsimile, high-speed data, and even television signals, require a stabilized parabolic antenna 1 m in diameter, weigh several hundred kilograms, and cost an average of $30,000.

Standard C offers access to such text-based services as Telex, Teletex, electronic mail, and packet-switched data networks; it can support any alphabet used in the world. Furthermore, users may also be able to take advantage of a number of proposed navigational and positioning services, says Inmarsat. "Standard C represents an advance in

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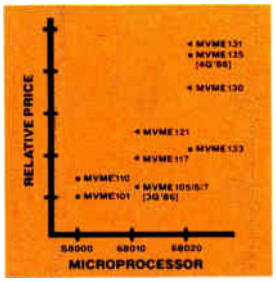

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The evidence is in, and it's incontrovertible. When it comes to light, Anritsu runs second to the sun.

True, Anritsu's little laser diodes *are* powerful enough to raise more than a few eyebrows.

And Anritsu optical attenuators can cut *almost* any light source down to size.

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As of October 1, 1985, Anritsu Electric Co., Ltd. became Anritsu Corporation.

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LIGHTWEIGHT. Inmarsat's prototype of a complete data-only marine earth station weighs only 13 lb. Production units should sell for about $5,000 and mount on the ship's superstructure.

marine communications as significant as the replacement of signal flags by radio. It will for the first time bring the benefits of satellite communications within the grasp of every class of vessel that goes to sea," says J. Christopher Bell, Inmarsat's Standard C project leader.

There are some 5,000 Standard A installations on commercial ships. But the world's commercial fleet comprises some 175,000 vessels, according to Inmarsat. In addition to those potential Standard C users, the organization feels that a large number of pleasure-boat owners will want Standard C, particularly those who venture onto the high seas or into remote areas. Standard C may also find uses in mobile terrestrial applications in areas where few people live.

IMMUNE. Seagoing vessels generally carry high-frequency marine radios, but bad weather can make hf communications unreliable. Satellite communications systems are relatively immune to interference, Inmarsat points out.

Inmarsat engineers have built a prototype Standard C earth station, and they expect to finalize system specifications by the end of the year. A number of manufacturers have shown interest in producing the earth stations commercially. Service using the same three satellites that support the Standard A stations should begin as soon as the manufacturers can bring their products to market, which should be in late 1987 or early 1988, says Inmarsat. Field trials of the equipment are scheduled for the second half of 1987.

Inmarsat will not reveal which manufacturers are working on Standard C equipment. Makers of receivers for a one-way shore-to-ship Inmarsat service called the Enhanced Group Call System seem to be likely candidates, however. Among them are Thrane & Thrane A/S of Copenhagen, Denmark; Sat-Text Ltd., Falmouth, UK; and Racal-Decca Marine Navigation Ltd., New Malvern, UK.

In addition, several component manufacturers have parts under development that will be useful in Standard C stations and should have them on the market within a year, Inmarsat says. Among them are integrated front-end chips and decoder chips implementing the Viterbi algorithm.

To compensate for the fact that the tiny earth station has less power than most satellite data systems, Standard C designers developed a highly redundant data-transfer scheme to ensure reliability. The 600-b/s digital microwave terminal transmits in the 1.53- to 1.545-GHz band and receives a downlink of between 1.6315 and 1.6455 GHz.

The prototype is housed in a box that measures 12 by 8.5 by 5 in. and weighs 13 lb, but production models are expected to be packaged so that they can be mounted entirely on a vessel's mast or superstructure. In the box are a front end for signal reception and transmission, a demodulator and decoder for received messages, a modulator and encoder for outgoing messages, an access-control and message-handling processor—a Motorola 68000 in the case of the prototype—and a user interface.

Signals are coded in a 1,200-symbol/s Viterbi-algorithm format, which provides full bit-for-bit redundancy at the 600-b/s system rate. Data is interleaved to make correction possible should the signal fade during reception.

The antenna used is a nonstabilized omnidirectional type with a minimum gain-to-noise-temperature figure of −24 dB/K. After the signal is decoded into a standard ASCII message, it is held in a buffer memory at least 32-K bytes in size. It can then be sent to a data terminal through an RS-232-C link. Inmarsat chose to use a laptop computer as the data terminal in its prototype, but other equipment can be used.

Outgoing messages are composed on the terminal. Pressing the transmit button initiates an interleaving, coding, and modulating process. A 20-W amplifier boosts the signal as it goes to the antenna. A synthesizer tunes the station automatically in 5-kHz increments for both transmission and reception.

Coastal earth stations will act as store-and-forward switches between Standard C users and land-based telecommunications systems, and they will need to be fitted with additional equipment to enable them to handle this new class of data. The amount of such equipment needed depends on the number of channels the shore station expects to support.

PLESSEY CHIPS WILL RUN WRISTWATCH PAGER

SWINDON, UK

In itself, building front-end receiver chips for radio communications gear is no big problem for Plessey Semiconductors Ltd., which has been a leader in this bread-and-butter business for years. But the company's newest task calls for something out of the ordinary: fabricating two chips that will do all frequency-modulation receiving and signal-conversion tasks for a wristwatch paging terminal—and fitting the chips into a 0.25-by-0.25-by-0.08-in. space.

The Swindon-based Plessey unit has been tapped by AT&E Corp., San Francisco, to supply the two devices, a front-end direct-conversion receiver and a synthesizer for its Receptor product. Now in the latter stages of development, Receptor seeks to integrate into a wristwatch package a radio receiver operating in the FM broadcast band, a microprocessor, and timekeeping integrated circuits.

The wristwatch terminal is key to a planned wireless communications network that will enable a person wearing the watch to receive short messages on its digital display. The message can tell the receiving person to dial a known

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Lyon, Oct 10
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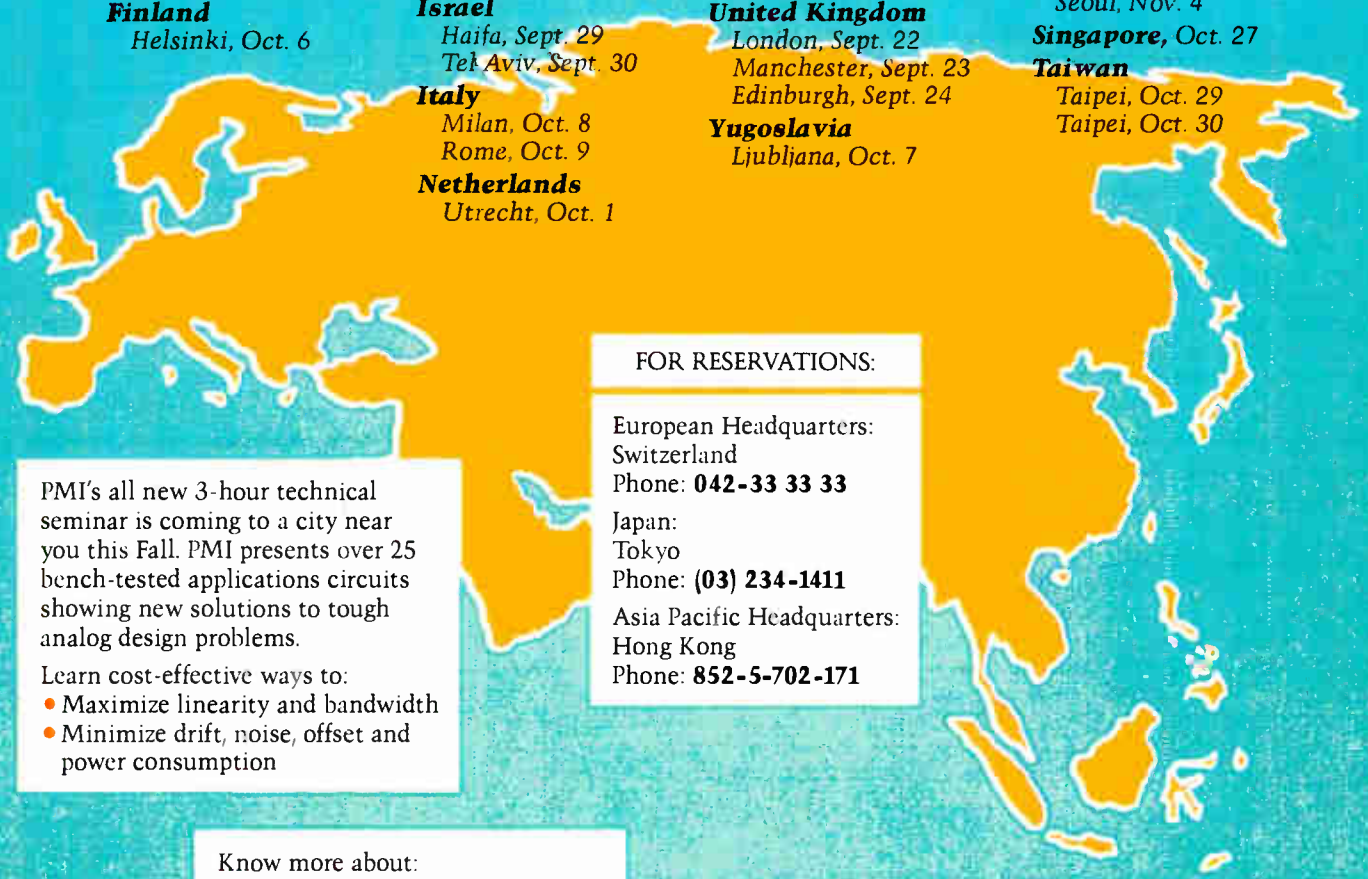
Munich, Sept. 26
Dusseldorf, Oct. 9
Israel
Haifa, Sept. 29
Tel Aviv, Sept. 30
Italy
Milan, Oct. 8
Rome, Oct. 9
Netherlands
Utrecht, Oct. 1

Norway
Oslo, Oct. 8
Spain
Barcelona, Oct. 10
Sweden
Stockholm, Oct. 7
United Kingdom
London, Sept. 22
Manchester, Sept. 23
Edinburgh, Sept. 24
Yugoslavia
Ljubljana, Oct. 7

Japan
Tokyo, Nov. 5
Tokyo, Nov. 6
Osaka, Nov. 7
Korea
Seoul, Nov. 3
Seoul, Nov. 4
Singapore, *Oct. 27*
Taiwan
Taipei, Oct. 29
Taipei, Oct. 30



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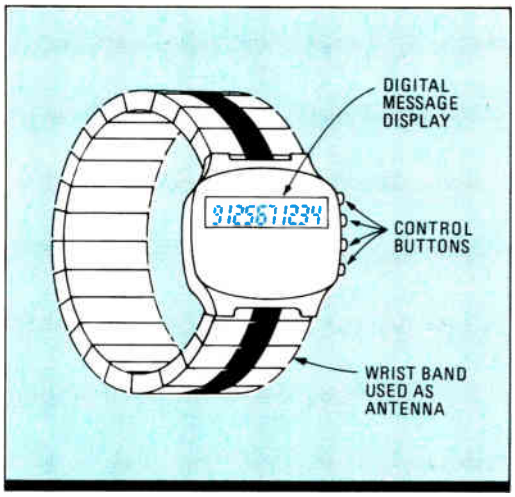

WRIST PAGER. AT&E Corp. is developing a messaging pager that fits inside a case the size of a wristwatch.

number (such as "call home" or "call office" requests), or the message sender can enter a new number for the Receptor wearer to call.

When AT&E completes its international network, persons wishing to send a message to a Receptor wearer will be able to do so via the telephone network. The message will be relayed to an FM broadcast station, where it is converted into a subchannel signal and transmitted superimposed on the signal carrying the station's normal program material.

Plessey officials do not play down the difficulty of their assignment—fabricating and delivering working silicon prototypes during the first quarter of 1987—but they point out that concept and basic design approaches were nailed down during the fulfillment of several joint-research contracts over the past year. "It is a very tough requirement, providing a receiver of that sensitivity, size, and power level," says Brian Hyde, product manager for Plessey. "It means taking integration to the highest levels, which provides the architecture for a Rolls-Royce solution to a very difficult task."

There are tight specifications on receiver signal-to-noise ratio (–92 dB) and dynamic range (40 to 60 dB). They're necessary because of the way the Receptor will be used, says Joseph F. Stiley, president of the AT&E research subsidiary, AT&E Laboratories in Beaverton, Ore. "Wearing it inside cars and buildings would yield a subpar performance otherwise," he says.

The receiver chip will be fabricated in a bipolar process technology, says Hyde, to operate off a 0.9-V supply, which is lower than commercial pagers now on the market. The Receptor will use a standard 50-to-60-mA watch battery, which should last for about a year—the chips draw power only when commanded, under a synchronous time protocol, as paging signals are transmitted.

One of the chip's sophisticated features is a gyrator filter built with a number of small-value capacitors. The filter produces a sharp response curve, which helps in maintaining the receiver's dynamic range.

The CMOS synthesizer chip has a frequency-agile feature that gives it the capability to step in 50-kHz intervals over the entire FM broadcast band. AT&E expects to use FM broadcast stations anywhere in the band, and Receptor must work without retuning in all locations, notes Stiley. The chip also has a filter designed to extract the subchannel FM signal, which has a transmission rate of 19 kb/s.

AT&E intends to subcontract Receptor manufacture, including signing a major watch firm. Officials will not say when that might occur, but the firm expects to have the wrist terminals ready late next year. *–Larry Waller*

AT&T DOUBLES MICROWAVE DATA RATE

NORTH ANDOVER, MASS.

An upgrade by AT&T Co. of its microwave radio network will soon allow the communications giant to move data at 90 Mb/s—twice the current rate—anywhere in the country. The upgrade means a substantial number of the 3,100 stations in the network will be enhanced with a new digital-signal transmission system.

AT&T began implementation of the new system in April, but the company was close-mouthed about details until the European Microwave Conference in Dublin, Ireland, last week, where it presented papers on the upgrade. The new digital system, called the TD-90, modifies and augments existing microwave equipment, using 64 quadrature-amplitude-modulation to raise the data rate. The 64 refers to the number of modulation levels being used in quadrature-amplitude-modulation transmission, a standard technique that combines phase and amplitude modulation.

INTERFERENCE BLOCKED. The new equipment is also notable for other features, however. It automatically varies transmission-power levels to suit conditions, for example. An extra-robust error-correction scheme is being used, along with a new system for canceling interference among microwave signals.

Economy was an important consideration in the upgrade development. Radio bays can be field-converted for TD-90 digital transmission by adding one shelf of equipment and making other, minor modifications, says Frank Witt, head of the microwave radio systems department at Bell Laboratories in North Andover. TD-90 also uses existing station antennas, towers, waveguide, and channel-separation networks.

To overcome signal-fading problems, Bell Labs developed an automatic transmitter-power controller for digital microwave transmission, says William Barnett, head of the digital transport performance planning department at Bell Labs in Holmdel, N. J. In normal operation, the controller allows transmission at relatively low levels to help avoid interference with other signals.

But if the signal starts to fade, the controller increases transmitter power in response to a tone generated at the receiving end and sent back to the transmitting side of the link. The frequency of the tone is proportional to power received.

As an added benefit, using the controller helps to eliminate the need for signal regeneration at each hop in the network. The lower transmission levels used make it possible to get by on amplification alone between most stations, so that regeneration is only required at every fourth hop. This results in a substantial hardware savings and improves system reliability, says Witt.

WITT: AT&T's digital microwave facilities will be upgraded without scrapping existing equipment.

By adding redundant bits to data streams, TD-90 can reduce background error rates of, say, 1 in 10^8 to the virtually error-free level of 1 error in 10^{13} bits. Higher error rates would still yield effective results; an error rate of 1 in 10^4 can be corrected to 1 in 10^6. Barnett asserts that the TD-90 system will typically run error-free.

Bell engineers designed an FM interference canceling system to address problems that

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crop up at the microwave stations, which might have up to five transmitters or receivers operating cheek by jowl. Their approach uses a sample signal to cancel interference through dynamic amplitude and phase optimization. "We can get 15 to 20 dB of cancelation," Barnett reports.

The TD-90 took two years to develop. The first implementation was a 10-switch installation covering a route running 750 miles, from White Plains, N. Y., to Cleveland.

AT&T will manufacture the TD-90 systems in North Andover and in Winston-Salem, N. C. The company says most of the work on the upgrade should be finished by the end of 1987.–*Craig D. Rose*

PACKAGING

AMP'S NEW VLSI PACKAGE SQUEEZES IN 320 LEADS

HARRISBURG, PA.

Very large-scale integrated circuits, especially those designed for the Defense Department's Very High Speed Integrated Circuits program, are pushing hard on chip-package and socket technologies. There's a need for much higher interconnection density and far faster operating speeds.

Amp Inc., Harrisburg, is trying to meet these requirements with a new 320-terminal ceramic chip carrier and the carrier's surface-mount socket. The package, which has input/output pads on 10-mil centers running around its edge, will be described at the International Electronic Manufacturing Technology Symposium in San Francisco this week.

Competing solutions, such as the dual in-line package and the pin-grid array, have leads on 100-mil centers. Most leaded and leadless chip carriers have either leads or pads on 50-mil centers; special chip carriers are becoming available with leads on 25- or 20-mil centers.

Typically, these packages are made using either co-fired ceramic technology, with its high dielectric constant and high conductor resistivity, or expensive thin-film technology. Some companies have gone to thick-film technology, which results in somewhat lower resistance but offers more limited resolution.

Amp's product, by contrast, has low-resistivity traces and short conductor lengths that contribute to its speed capabilities, says Martin G. Freedman, manager of micrologic packaging at Amp. To create the low-resistivity conductors, the ceramic leadless package is made using a very precise lithographic patterning technique that makes for a fine-line, high-purity, plated-copper pattern with a nominal 1-mil thickness.

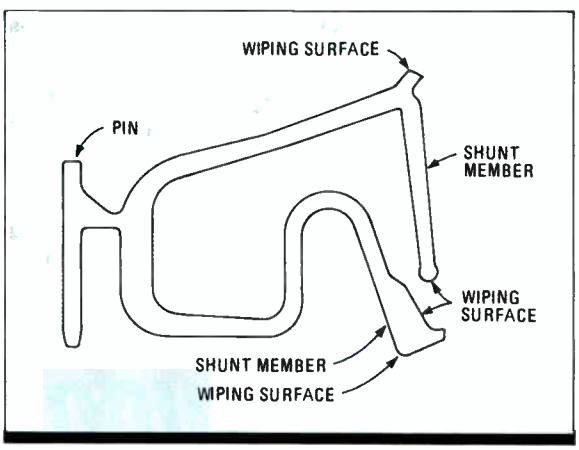
SHORT CONDUCTORS. A proprietary conductor design keeps conductors short on the carrier's substrate by completely encircling the die-attach area with both voltage and ground buses, providing direct access for all the chip's ground and power-supply circuits. In addition, the pattern contains a built-in decoupling structure.

And to achieve interconnection density, the fine-pitch Amp socket exploits a clever mechanical and electrical design, and the carrier uses a new fabrication method.

The socket has up to 320 contacts on 10-mil centers and is designed to accommodate a standard square substrate measuring 0.950 in. on a side. The key to the socket's high performance is its elegant contact design (see diagram). The single vertical pin shape at the left side of the contact assembly is driven into the plastic socket housing and serves as the anchor for the contact.

When the carrier is mounted, the contact is compressed. Then it rotates so that full wiping action occurs at three important interfaces: the one between the package and the contact, the contact to the printed-circuit board, and the interface between the two shunt members. The shunt members are the key ingredients that let the socket carry very high-speed signals.

For example, the vertical shunt bypass member



CONTACT. The contact design in Amp Inc.'s 10-mil-pitch socket provides a very short electrical path to the pc board.

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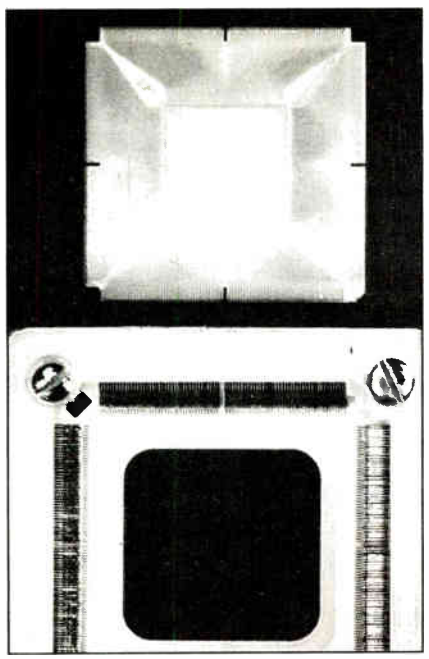

VLSI DENSITY. The chip carrier and socket combination can support 320 I/O lines.

provides the lowest inductance and shortest signal path possible. The only limit to signal-path shortness is the thickness of the package or cover. Initial theoretical calculations indicate an inductance of less than 1.5 mH and adjacent-contact capacitance of about 0.5 pF. This contact design separates the spring-force member from the signal-carrying member, which makes the desired electrical performance possible.

SOLDER ELIMINATED. The force (150 grams per contact) needed to compress 320 contacts requires the use of top and bottom aluminum plates to clamp the carrier/socket assembly to the pads of a pc board. The elimination of solder from this surface-mount socket makes ready replacement possible. The metal-to-metal contact between socket and board greatly contributes to long-term contact reliability.

Precise alignment of the socket with its finely patterned contacts required a special mechanical design. The features of a standard Jedec chip carrier, consisting of three corner notches and one corner chamfer, were inadequate for a package with contacts on 10-mil centers.

Amp developed a new alignment system based on features in the middle of each side of the package—slots in the carrier and mating posts on the socket. Accurate lithography and precise laser machining made this system possible.

Using a socket avoids the problem of handling fragile socket leads on 10-mil centers, while providing the required mechanical compliance. This permits the board substrate to be selected on the basis of its electrical properties alone.

–Jerry Lyman

TAKE THE 32-BIT TEST:

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The key to digital communication systems

Circle 112 on reader service card

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INTERNATIONAL NEWSLETTER

FUJITSU ADDS MINISUPER-CLASS COMPUTER

Fujitsu Ltd., by extending its supercomputer line at the low end with a stand-alone model that doubles as a mainframe, has in effect entered the minisupercomputer market. The Kawasaki, Japan, company was able to keep the new VP-30's price low by lowering scalar performance, a reduction that tends to make the machine more a minisuper than a supercomputer. At the same time, though, Fujitsu maintained most of the vector performance: more than 110 megaflops for the VP-30, compared with 140 for the former bottom-of-the-line VP-50. That's a reduction of only 20%, while the price—$485,000 to $515,000 in Japan—and the scalar performance are both 35% lower. Other major changes include simpler control systems and a scalar buffer reduced from 64- to 32-K bytes. Still, the computer can be upgraded in the field all the way to a top-of-the-line VP-200. Fujitsu expects to sell about 170 supercomputers by the end of fiscal 1989, and predicts 70 or so will be VP-30s. The company already has sold 30 VP-family machines in Japan, and 14 throughout the rest of the world; most of the latter were sold by Amdahl Corp., Sunnyvale, Calif., and most of those outside the U. S. □

PHILIPS GAINS MUSCLE IN OFFICE MARKET

Look for Philips International NV of Eindhoven, the Netherlands, to make a bigger dent in the European office market. The Dutch giant will be able to connect its products to networks supporting IBM Corp.'s ubiquitous System Network Architecture, now that it has agreed to integrate software from The Orion Group Inc. into the Philips product line. As part of the deal, Philips and Orion, of Berkeley, Calif., will develop a software package that combines support for earlier versions of SNA with more recent enhancements. □

VICTOR THREATENS 8-MM MARKET WITH LIGHTWEIGHT VHS CAMCORDER...

Victor Co. of Japan has thrown another roadblock in the path of 8-mm camcorders and VCRs in the battle for market supremacy. It has reduced the weight of its GR-C9 record-only camcorder, which uses half-inch tape in the VHS-C format, to only 1.5 lb, which is three-fourths the weight of the smallest available 8-mm camcorder, made by Sony. Earlier this year—February in Japan and May overseas—Victor introduced its 2.9-lb GR-C7 full-feature VHS-C camcorders, beating Sony's 8-mm product by more than 2 lb. At that time, industry experts said that Victor pushed Sony's 8-mm marketing program back by at least a year. The new GR-C9 has only a fixed-focal-length lens (rather than a zoom lens; Sony's lightest product has a similar fixed-focal-length lens) and can only record, but its low price—$955 in Japan—lightness, and compactness make it an excellent take-along system for the more than 100 million consumers worldwide who have VHS VCRs at home on which to play back the tapes. □

....AS NIKON JOINS RIVAL CAMERA MAKERS IN THE 8-MM RACE

Add Nihon Kogaku (Nikon) to the list of Japanese firms, mainly camera manufacturers, jockeying for position in the emerging U. S. 8-mm camcorder market. Nikon is expected to lock horns with Minolta, spilling their battle for leadership in the automatic-focus 35-mm single-lens-reflex camera market over into the new arena. This time Nikon hopes that its lighter, 2.9-lb camcorder made by Matsushita should put it one up over Minolta with a 3.1-lb unit from Hitachi, even though Matsushita supplies a similar product to Olympus, while Asahi Pentax and Kyocera (Yashica) sell private-label models made by Hitachi [*Electronics,* Sept. 4, 1986, p. 50]. Canon offers a 4.4-lb camcorder it makes itself. □

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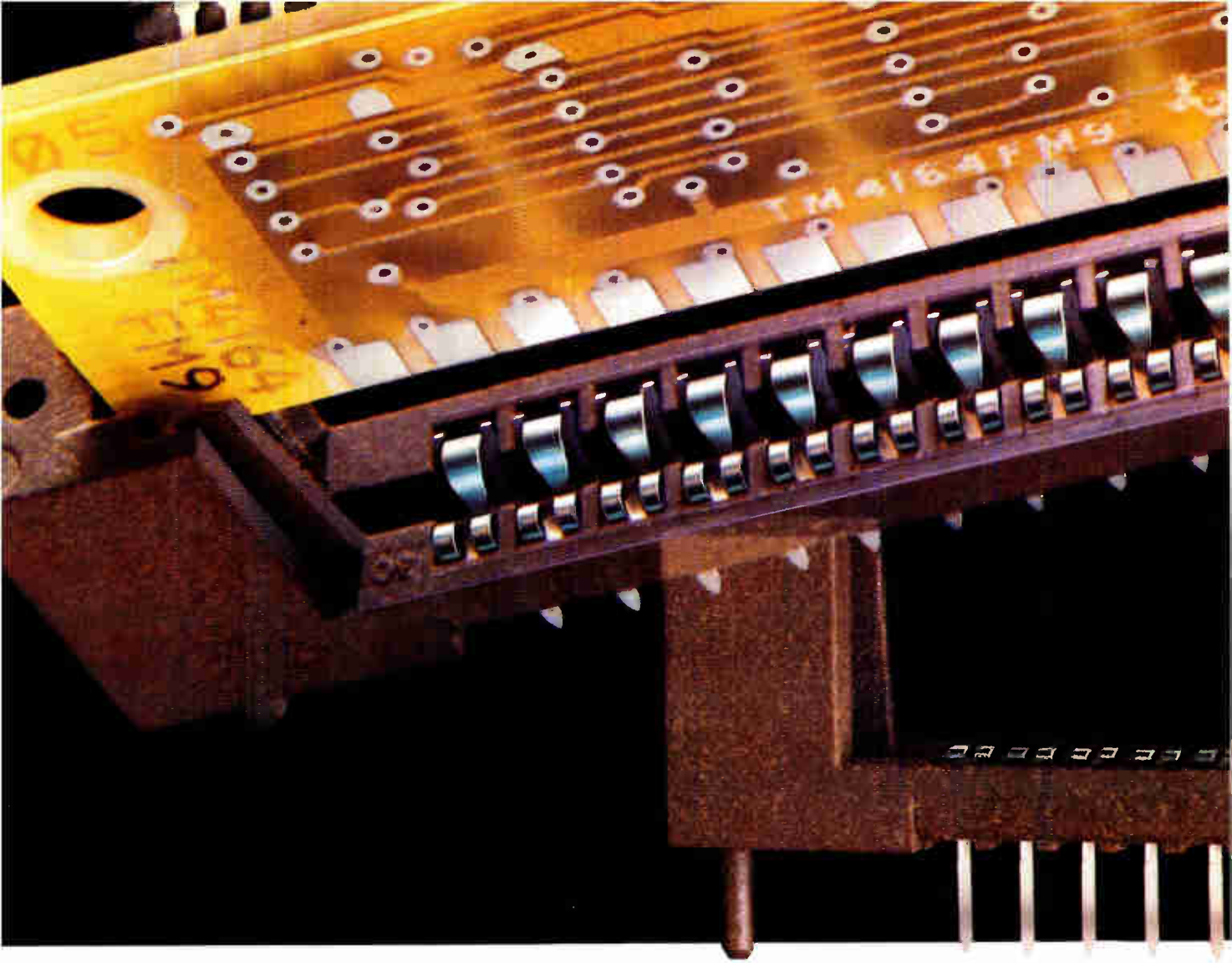

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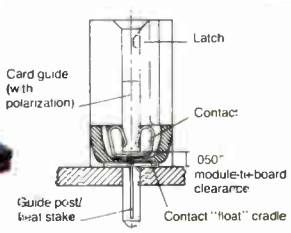

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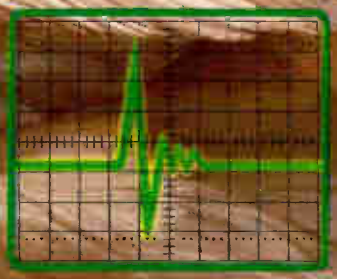

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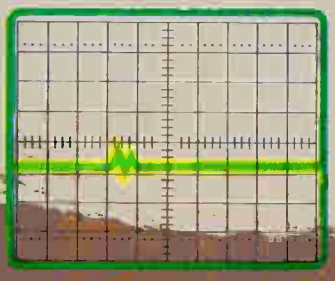
TO FEATHERS



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Circle 53 on reader service card

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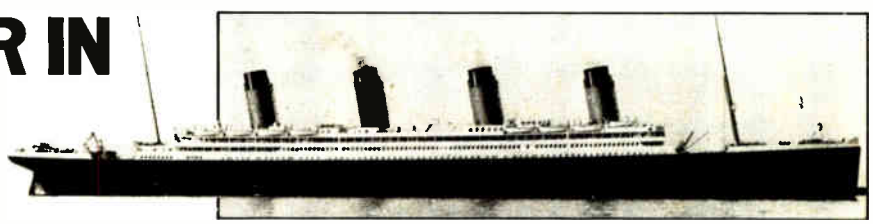

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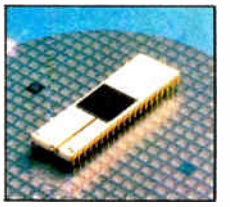

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INSIDE TECHNOLOGY

GaAs LSI GOES COMMERCIAL

by Bernard Conrad Cole

With the handling and fabrication of complex gallium arsenide chips becoming less of a headache, GaAs LSI *is emerging into the real world as a material that can compete with silicon in some major application areas. GaAs has long tantalized system designers with its promise of speed, even as it has frustrated them with its fragility, but years of work on processing—the learning curve so familar in*

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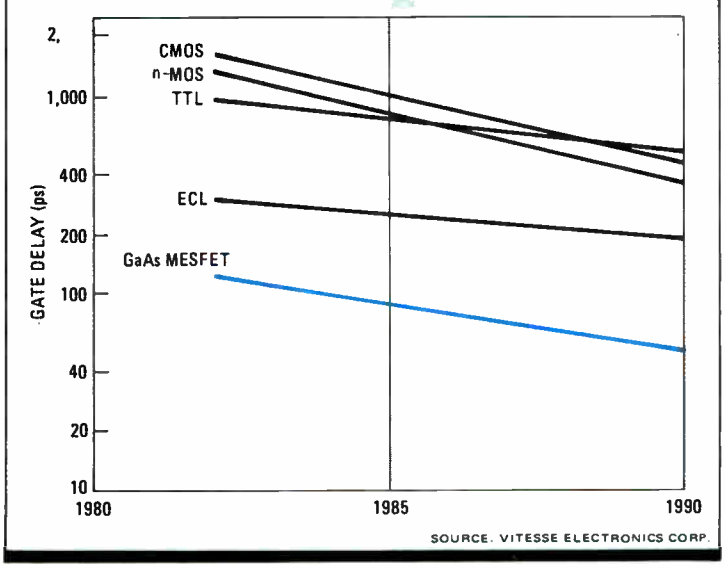
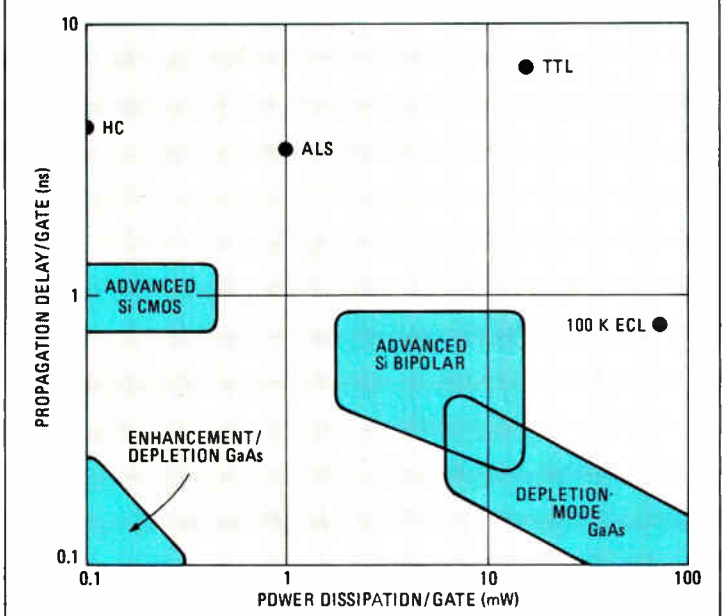
GaAs MAINTAINS SPEED EDGE



GaAs CAN COMPETE WITH BIPOLAR, MOS



electronics technology—is beginning to pay off with commercial digital GaAs integrated circuits.

The key is complexity. Now that affordable LSI GaAs circuits are coming out of the labs, the technology can be expected to climb out of niche military applications and into a widening circle of uses: high-speed controllers in disk subsystems, process automation, simulation, and high-performance graphics systems, to name a few. And GaAs memory components will find their way into computer cache memory; computer register files, such as those supporting fast reduced-instruction-set architectures; and real-time signal processing in array processors, for example.

In most of these applications the GaAs parts will be selected solely for speed. But in some applications their radiation hardness—GaAs can absorb up to 10,000 times as much radiation as silicon without ill effects—or temperature tolerance will make the sale.

The first GaAs LSI digital logic parts to move into commercial production is the family of 29G00 bit-slice components from Vitesse Electronics Corp. (see story, p. 61). But if the increasing number of product introductions and technical papers is any indication, Vitesse will not be alone for long. At least two other manufacturers—Rockwell International Corp. and McDonnell Douglas Corp.—plan volume production in 1987 of GaAs LSI 4-bit-slice components, and three other companies have announced LSI-level gate arrays.

Further evidence of momentum will be seen next month when the Gallium Arsenide Integrated Circuit Symposium convenes at Grenelefe, Fla. Of the 39 papers scheduled for presentation at the Oct. 28-30 meeting, half are devoted to digital circuits. And more than three quarters of these describe a variety of LSI circuits, ranging from gate arrays to static RAMs and a variety of custom and standard circuits.

These developments, however, come at a moment of resurgence for silicon bipolar technology [*Electronics*, April 7, 1986, p. 24]. Bipolar's subnanosecond speeds are approaching those of GaAs, and VLSI densities are 10 to 30 times those of current GaAs digital circuits. Some manufacturers, including Fairchild Semiconductor Corp., believe silicon will remain the technology of choice (see "Fairchild relegates GaAs to niche status," p. 60). Others—like Lou Tomasetta, the president of Vitesse's Integrated Circuits Division in Camarillo, Calif.—say the ball game is still in its early innings and that GaAs will emerge the winner.

The first hint that GaAs was emerging as a force in the market was the unveiling of circuits last winter by Fujitsu Ltd., NEC Corp., and Texas Instruments Inc.

From TI in Dallas came a 4,000-gate bipolar GaAs array, fabricated using 5-μm rules with molecular-beam epitaxy. The key to its density is a variation of the heterojunction inverted-transistor integrated-logic technique. At 0.2 mW per gate, propagation delay is 1.25 ns with a fanout of four. At 1 mW per gate, the delay is improved threefold, to 400 ps.

Fujitsu, of Atsugi, Japan—which like TI and NEC made its announcement at the International Solid State Circuits Conference [*Electronics*, Feb. 17, 1986, p. 23]—described the largest high-electron-mobility transistor-based logic circuit, an array with 1,500 gates and 6,650 transistors. Its 1.2-μm enhancement/depletion type direct-coupled FET logic process has also been used to build 1-K, 4-K, and 16-K static random-access memories. Now in development is a 3,000-gate HEMT-type array, featuring gate delays of 85 ns

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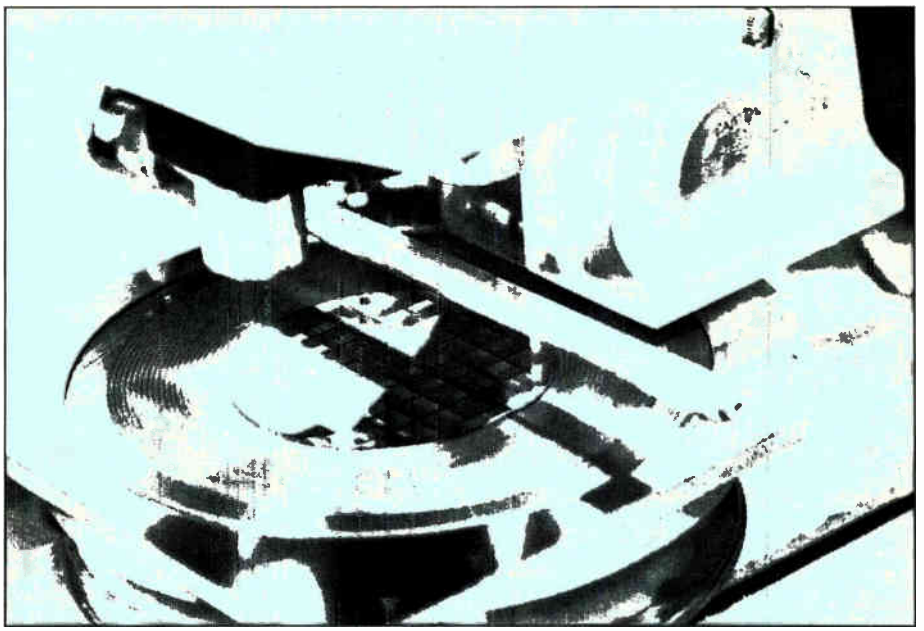
for a three-input NOR gate.

In Kawasaki, Japan, NEC is developing a bipolar silicon GaAs array that is compatible with current-mode logic. It houses 3,000 gates, and boasts gate delays in the 200-ps range and data rates up to 1.32 gigabytes/s.

Perhaps the most impressive item to be unveiled at the upcoming Florida symposium is a 6,000-gate array from Honeywell Inc. The Minneapolis company designed, fabricated, and tested the device as part of the Defense Advanced Research Project Agency's GaAs pilot-line program. With a gate delay of about 1 ns, the array has been used to fabricate a 19,000-transistor 12-by-12-bit asynchronous multiplier and its associated test circuitry.



EASIER TO GET ALONG WITH. Gallium arsenide wafers are inherently fragile, although recent work has led to improved materials and higher yields.

Looking for compatibility with silicon emitter-coupled logic, CMOS, and TTL, TriQuint Semiconductor Inc. of Beaverton, Ore., has developed an enhancement/depletion GaAs array with 3,000 gates and configurable cells. It has 64 input/output lines, each of which can handle data rates up to 700 MHz. With it, a 4-bit 10181 silicon bipolar ECL arithmetic logic unit has been emulated using only 9% of the total array. The unit has 2- to 4-ns propagation delays and dissipates 430 mW. Consisting of 1,020 compound logic cells, the array has an intercell delay of 55 ps/mm of interconnect, making possible a 2:1 speed advantage for long critical paths. Flip-flop macrocells have typical toggle rates of 1 GHz. NOR-gate macro delays are typically 120 ps unloaded and 285 ps loaded.

Ford Microelectronics Inc., meanwhile, is aiming at the eventual introduction of an ECL-compatible GaAs array with 3,000 to 6,000 gates. The Colorado Springs company has developed a self-aligned n+ enhancement/depletion MES FET process with refactory metal-silicide gates that can be fabricated at low temperatures. Using 1.4 μm design rules, arrays with an internal gate delay of 225 ps and dissipating 1.5 mW have been achieved.

FASTER STATIC RAMs

On the static RAM front, researchers will report that they have substantially sped up the devices since the 1985 gathering. Pushing the limit to its extreme is a 1-K HEMT-based design from Rockwell International Corp. in Thousand Oaks, Calif., that dissipates 450 mW and accesses addresses as quickly as 600 ps. The combination of high speed and low power is achieved through the use of complementary push-pull drivers and enhancement/depletion source followers in places where long line driving is required. By using depletion-mode pull-up FETs to connect the bit lines to the pull-up voltage, the bit lines are precharged, reducing the voltage swing on the bit lines and speeding up the access time.

Mitsubishi Electric Corp. in Itami, Japan, has developed a 2.5 ns, 4-K SRAM made with an enhancement/depletion mode GaAs process, which the company has also used to fabricate 1-ns 1-K and 5-ns 4-K SRAMs. The 4-K model dissipates only 200 mW, one-fifth that of the earlier devices. Manufactured with a 2-μm self-aligned process with refactory metal gates, double-level metal interconnects, and shallow channels, the circuit derives its low power demand by using OR-gate structured address predecoders to reduce the power dissipation of the address buffers and predecoders to 10%.

Matching it in low-power operation without sacrificing much in speed is a 256-by-4-bit SRAM from Honeywell's Physical Sciences Center in Bloomington. Minn. It features access in 3 ns and dissipates only 150 mW. The device is fabricated with 1-μm enhancement/depletion MES FET technology with two levels of metal interconnect and tungsten silicide gates.

Another memory chip sacrifices some speed and power for ECL compatibility. The 256-by-4 SRAM from Gigabit Logic Corp. of Newbury Park, Calif., has read and write cycle times of 2 ns at 4 W, and 2.5 ns at 2.5 W. That is a sixfold improvement over the 12 ns that current bipolar ECL RAM systems need to cycle, and it is achieved with a proprietary self-timed architecture and the use of capacitor diode FET logic at the gate level. Internal measurements indicate a delay of 600 ps for internal clock generation and 1.45 ns from the internal clock to the input of the output register.

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Several papers will describe initial efforts aiming at the next goal: VLSI densities. This work to step up integration a notch seeks to build circuits using GaAs/aluminum GaAs heterojunction superlattice structures [*Electronics*, April 28, 1986, p. 37].

Under investigation at Raytheon Corp. in Lexington, Mass., are both non-self-aligned and self-aligned molecular-beam epitaxial structures that are more than 100 times smaller than current GaAs transistors. They will be used to fabricate a number of memory test circuits. Even more aggressive is Japan's Nippon Telegraph & Telephone Corp. in Kanagawa, which will report on complementary MIS FET circuits using such structures. In a 15-stage ring oscillator, researchers were able to achieve minimum gate delays of about 94 ps with power dissipation of no more than 580 μW/gate, with a 1.5-V supply.

GaAs backers say development of the technology is still in its infancy and will soon outdistance silicon, which is approaching its physical limits

All these new GaAs products will be going head-to-head with vastly faster silicon digital circuits (see top chart, p. 58). But, says Vitesse's Tomasetta, the technologists working with silicon are approaching the physical limits of their material. By contrast, digital GaAs technology is still in its infancy. It should improve by leaps and bounds, and limits on its speed are nowhere in sight. Therefore, he concludes, the comparisons between silicon and GaAs should begin to diverge sharply over the next several years.

In addition, he says, GaAs's lower power dissipation—and therefore less complex chips—gives it an even stronger edge over ECL now and, in the long term, over silicon CMOS. Enhancement/depletion GaAs digital circuits in particular, with power-dissipation ratings at the gate level on the order of 0.1 mW to 0.25 mW per gate, are no higher than 1-to-2μm silicon CMOS circuits of equivalent density, but are 3 to 10 times faster, he says (see bottom chart, p. 58).

Also backing GaAs is Bob Gisburne, GaAs custom products manager at Ford Microelectronics Inc. Gisburne believes LSI digital GaAs ICs will continue to increase their performance edge over the fastest silicon-based ICs as advances are made in lithography and materials. "Even first-generation GaAs ICs will maintain their 2½- to 5-times lead over equivalent-geometry silicon devices, and that lead will be extended when second- and third-generation devices, now in development, emerge into production," he says. □

FAIRCHILD RELEGATES GaAs TO NICHE STATUS

Despite the optimistic projections of gallium arsenide digital circuits vendors, traditional silicon bipolar and CMOS manufacturers such as Fairchild Semiconductor Corp. feel confident in their ability to retain a dominant share of the high-performance end of the integrated-circuit business.

The reasons are simple, says Hemraj K. Hingarh, design engineering manager for Fairchild's memory and high-speed logic division in Puyallup, Wash.: GaAs circuits do not offer many advantages over conventional processes, and they are a great deal more expensive. Aside from high radiation tolerance and the ability to operate over a wider temperature range, he says, digital GaAs offers little competition to silicon bipolar and CMOS technology.

As far as raw speed is concerned, he says, advanced bipolar processes can yield gate delays that match those of GaAs. At the same time, silicon bipolar can drive high-capacitance loads. "Digital GaAs circuits, especially of the enhancement/depletion type, are similar to silicon CMOS in their poor loaded-drive capabilities," he says. As a result, system throughput is compromised because of on-chip interconnect delays and off-chip voltage translation.

Hingarh says that the story is essentially the same regarding power dissipation: GaAs digital LSI, especially of the enhancement/depletion type, compares favorably with advanced VLSI CMOS at the gate level, but it is quite a different story at the chip level, especially at high densities. That is because the thermal conductivity of GaAs is only about half that of silicon. Moreover, he argues, even when compared with silicon bipolar ECL, GaAs digital logic requires a great deal more power at frequencies above 100 MHz.

"Another factor that must be considered in the use of GaAs digital logic is that noise margins are not as good as in silicon," Hingarh notes. This means that "area has to be traded for higher reliability."

In terms of density, silicon technology comes out ahead on at least two counts, according to Hingarh. First of all, he says, GaAs digital logic is at least two generations behind silicon, both CMOS and bipolar. "GaAs is just now nudging into the LSI level, with gate densities ranging from 3,000 to 6,000 just now being considered. By comparison, CMOS gate densities that are now going into production range from 25,000 to 125,000. Bipolar digital logic is now at the 8,000-to-10,000-gate level, and it's moving toward 100,000 gates."

Even with equivalent design rules, Hingarh says, GaAs digital logic lags behind silicon, because of its higher density of wafer dislocations, lower noise margins, gate interconnection limitations, and lower drive capability. For example, he notes, at 1 μm, GaAs is limited to 10,000 to 15,000 gates, whereas bipolar is in the 50,000-to-80,000-gate range, and CMOS stands at the 200,000-to-300,000-gate level.

Still other factors limit GaAs to certain niche applications, Hingarh adds. "For one thing, wafer costs are extremely high compared to silicon, greater by a factor of 5 to 10," he says. "Second, there is the issue of input/output compatibility—or more precisely, incompatibility." In order for GaAs to be useful to the designer in real-world applications, "the raw gate speed of GaAs must be sacrificed to make such circuits compatible with existing silicon logic families." *–B.C.C.*

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BIT-SLICE ICs KICK OFF ERA OF COMMERCIAL GaAs LSI

Vitesse's 29G00 bit-slice family members are functionally compatible with their AMD equivalents, but system throughput will be two to three times faster

The era of off-the-shelf large-scale-integrated gallium arsenide chips is coming, and engineers will not have to wait long to begin designing these parts into systems. Vitesse Electronics Corp. is launching GaAs versions of Advanced Micro Devices Inc.'s Am2901 4-bit microprocessor, Am2902 carry-lookahead generator, and Am2910A microcontroller, plus a novel 1-K-by-4-bit static random-access memory. And it expects to begin shipping samples next month; all four chips should be available by the first quarter of 1987.

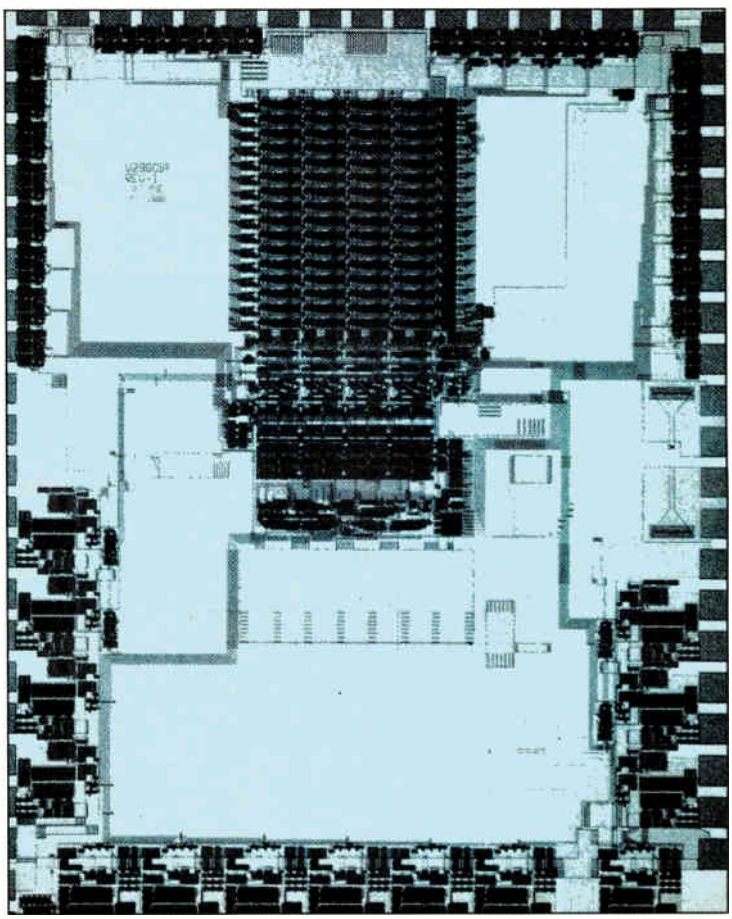
Vitesse has set out to make GaAs parts that are functionally compatible with their AMD equivalents. However, every member of Vitesse's VE29G00 family is input/output compatible with 100K emitter-coupled logic, giving designers a familiar set of I/O specifications and chips to work with. The RAM has a 3.5-ns minimum cycle time, and the other devices exhibit speeds three to four times higher than those of the high-speed ECL devices after which they are modeled.

To demonstrate the speed that can be achieved using its new GaAs components, the Camarillo, Calif., company compared two 16-bit processors made of 4-bit slices. The two configurations are identical in function; one uses Vitesse GaAs parts, plus one 100K ECL glue chip, and the other uses bipolar ECL 2900 parts. In some operations, the GaAs processor is as much as four times faster than the silicon version. For example, the minimum control loop cycle time is 22 ns for the VE29G00 parts and 98 ns for the bipolar ECL 2900C parts. For the data loop, cycle time drops from 97 ns to 29 ns.

Engineering samples of the VE29G02 carry-lookahead generator will be available for shipment within 30 days. The VE29G01 processor slice (Fig. 1) and VE29G10 microcontroller can be ordered now for delivery in the first quarter of 1987. The VE12G474 static RAM is scheduled for shipment by December.

Samples cost $435 each for the VE29G01 processor, $225 for the 29G02 carry-lookahead generator, $475 for the 29G10 microcontroller, and $595 for the 12G474 SRAM. If yields materialize as planned, volume pricing for the 29G01 and 29G02 will break the $100 barrier by the end of 1987 and the $50 barrier by the end of 1988. Similarly, production-quantity pricing on both the 29G10 and 12G474 SRAM should be below $150 by the end of 1987 and around $50 by the end of 1988.

Vitesse's announcement constitutes the first



1. SPEEDY SLICE. At 14 ns, the VE29G01 4-bit-slice ALU is four times faster than bipolar implementations of the 2900 part.

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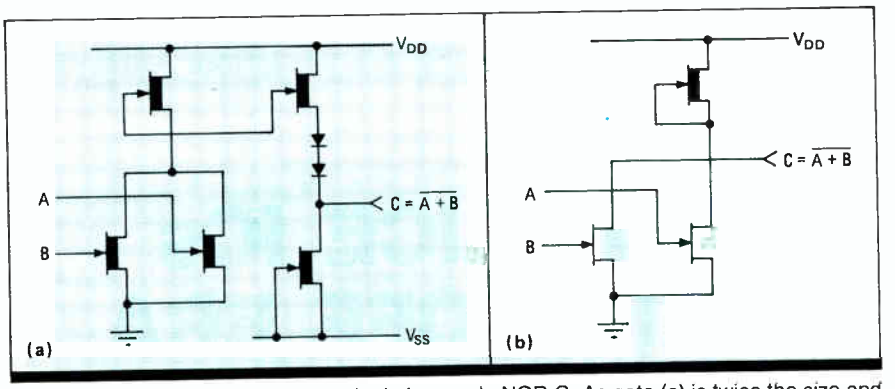


2. LSI GaAs GATES. A depletion-mode NOR GaAs gate (a) is twice the size and uses 10 times the power of an enhancement/depletion GaAs gate (b).

commercial availability of LSI logic in gallium arsenide. Further, if the company lives up to its announced delivery schedule, it may also be the first U. S. company to begin volume production of GaAs LSI logic, commercial or otherwise. However, other companies are also planning GaAs parts (see p. 57), and next year should see a flood of similar LSI products.

The success of Vitesse's venture into off-the-shelf LSI GaAs parts depends in large part on its proprietary silicon-like fabrication process, based on enhancement/depletion-mode metal-semiconductor FET technology. The process uses nine mask levels, including two aluminum layers for global metalization. "The equipment we use is the same that one would use for silicon IC fabrication, although we use it slightly differently and process smaller wafers than in contemporary silicon production," says Jim Mikkelson, vice president of operations.

"Our objective from the beginning was to adapt proven silicon IC processes, rather than put Band-Aids on an R&D process. And this gives us an added advantage: as better equipment or better methods are developed for silicon IC manufacturing, we should be able to incorporate many of those improvements into our processing."

Vitesse is using conservative 1.25-μm feature sizes, with a 4-μm pitch for the metal features. However, both the process and the equipment are capable of working below 1-μm geometries.

The Vitesse design mixes enhancement-mode switches and depletion-mode loads, much like silicon n-MOS, and uses self-aligning refractory metal gates. In addition, gate metal can be routed for local interconnects, much like polysilicon in MOS processes.

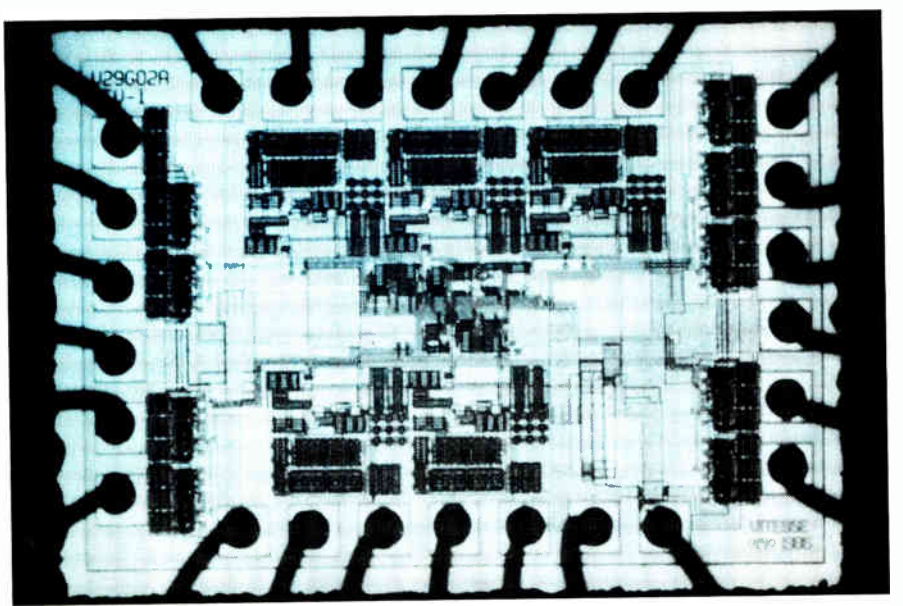
In contrast to digital GaAs ICs based on depletion-mode technology, typical enhancement/depletion GaAs chips use very little power—as little as 0.1 mW per gate, compared with 5 mW for depletion-mode. They run at about the same speed, and they have less than half the number of components. Implementing a simple two-input NOR gate requires seven components in depletion-mode technology and only three in enhancement/depletion technology (Fig. 2).

Vitesse's process can produce as many as 5,000 gates per chip. Continuing refinement is expected to bring that capability up to 6,000 gates by 1988, and to 10,000 gates per chip by 1990.

Vitesse selected the 2900 family for its first LSI products because it is widely used in applications where computing horsepower is critical, such as real-time signal processing. The market for the devices has continued to grow, if only because for the past 10 years bit-slice architecture has offered the fastest computational engine on a chip. A five-year technology exchange agreement signed in late 1985 with AMD guarantees that the GaAs slice parts are microcode-compatible with the 2900 family.

In keeping with Vitesse's emphasis on practicality, its first parts are not laboratory curiosities, but are for use in real-world applications. There are enough pieces in the set, says Lou Tomasetta, president of Vitesse's Integrated Circuits Division, to make up useful subsystems on the order of 16- or 32-bit microprocessors or controllers. Designers can use the familiar 100K ECL I/O specifications and code that is compatible with existing applications.

By making its GaAs products logically compatible with the AMD family, Vitesse is ensuring that its customers can take advantage of existing software, application designs, documentation and development systems, and even the familiarity of



3. CARRYING ON. The VE29G02 carry-lookahead generator can work across four groups of binary ALUs and across 16- or 32-bit word lengths.

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working designers with the AMD chips. The new chips do depart from the AMD parts in certain physical and electrical characteristics.

Functionally, the GaAs parts behave just like their silicon counterparts. The VE29G01 is a 4-bit microprocessor slice intended for use in central processing units, peripheral controllers, programmable microprocessors, video graphics engines, and other applications where speed is a primary requirement. Like the Am2901, the device consists of a high-speed arithmetic logic unit with an eight-function repertoire and a 16-word-by-4-bit two-port RAM, along with associated shifting, decoding, and multiplexing circuitry.

AMD's high-speed version of the 2901, the Am2901C, is specified to perform a 4-bit add in 40 ns; even with Vitesse's conservative design rules, the VE29G01 does it in 13 ns. The respective maximum clock rates are 25 MHz and 77 MHz.

The VE29G02 (Fig. 3) is a high-speed carry-lookahead generator that accepts up to four pairs of carry propagate and generate signals as well as a carry input signal. It can provide carry lookahead across four groups of binary ALUs and across 16- or 32-bit word lengths.

The third member of Vitesse's new family is the VE29G10A microcontroller, an address sequencer for controlling the sequence of execution of microinstructions stored in microprogram memory. Its internal elements are 12 bits wide, so it can address up to 4,096 words. In addition to supporting sequential access, it also permits conditional branching to any instruction.

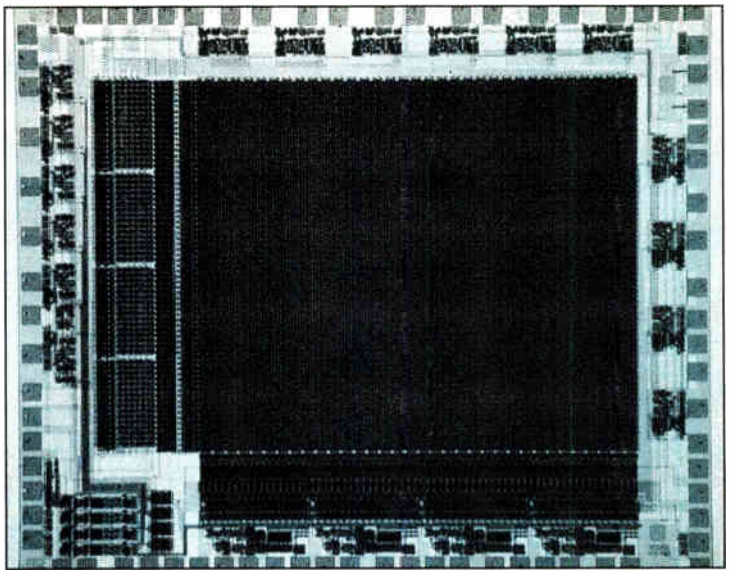
EXTRAS ON THE RAM

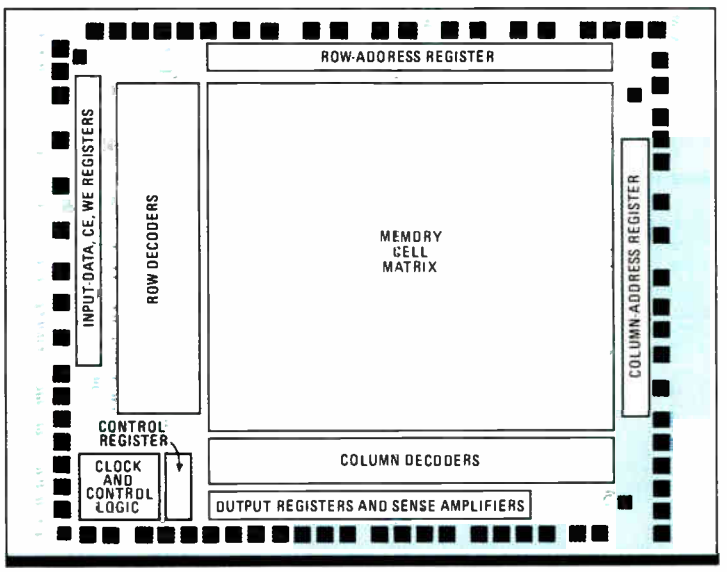
The most unusual of the products is the VE12G474 SRAM (Fig. 4). It incorporates more than its 1-K-by-4-bit memory matrix; it also boasts I/O registers, a self-timing mechanism, and output buffers capable of driving up to 25 Ω. The SRAM is functionally equivalent to a six-chip set of 100K RAMs but cycles in 3.5 ns versus 7.8 ns for the ECL parts. It is designed to relieve several significant problems for the design engineer moving up to GaAs speeds.

For instance, the added I/O registers assure synchronization. Given the high internal speed of GaAs chips, the time for signals to move between chips becomes significant, and it is possible in some designs for some address bits, for example, to reach the RAM before others. The registers nullify this problem.

However, the high speed of the RAM can present its own kind of design problems. For example, a conventional memory architecture would require the off-chip generation of write pulses, a procedure that works acceptably well for slower memories. Given the 3.5-ns cycle time of the VE12G474, those write pulses would have to be held to 1.0 ns, a difficult design exercise requiring another handful of support chips.

In addition, since skew times can be of the same magnitude as the pulse being generated, the designer might face a substantial challenge in designing this circuitry. So the VE12G474 uses an on-chip clock module and a portion of the clock pulse doubles as the write pulse, obviating the need for an off-chip pulse generator.





4. FAST SRAM. The 3.5-ns cycle time of the 4-K VE12G474 GaAs SRAM is 2½ times faster than that of the 100K ECL equivalents.

Despite opting for functional and microcode compatibililty with the 2900 family, Vitesse chose not to make the VE29G00 parts physically or electrically identical to the AMD parts. "The high-speed characteristics of GaAs put different requirements on things like the I/O logic and even the packaging," explains Ira Deyhimy, vice president of engineering. "To start, you need to minimize the chip-to-chip connection lengths in order to realize the full speed potential of the part. It makes little sense to use a 3- or 4-ns part and then consume another 5, 6, or even 10 ns getting the signal to it. In silicon, you wouldn't worry about that as much. In GaAs, you absolutely must. Even the package must be considered sep-

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arately. It must have the smallest inherent delays possible to maintain the highest system performance possible, as well as to minimize ringing caused by loading effects, and crosstalk and power-supply interference."

For these reasons, a custom ceramic leadless chip carrier was designed. A square cavity, only slightly larger than the die, reduces the length of the wire bond, thereby decreasing the inductance of signal lines. The chip carrier offers a lower impedance ground path than other packages and occupies less board space—which, again, allows for packing the parts closer together to minimize signal line lengths.

Operating speeds demanded that I/O characteristics be changed as well. The original 2900 family used TTL-level I/O interface circuitry. Today, 100K ECL is the fastest interface available, and the VE29G00 family has been designed to use 100K I/O and voltage levels.

The benefit to the user of an ECL interface outweighs the sacrifice of GaAs's maximum speed and such drawbacks as increased power use and a second power supply, –4.5 V, that enhancement/depletion GaAs doesn't need, Deyhimy maintains. From the interface standpoint, a VE29G00 family member looks just like a 100K ECL device, yet has significantly lower internal propagation delays. And designers will be able to choose from a wealth of existing glue chips to complement the VEG2901 microprocessor.

"Striving for every drop of performance we could wring out of gallium arsenide would have led us to lower-power designs using specialized I/O," says Tomasetta. "But that wasn't the purpose. Then the parts would indeed have been ultrafast laboratory curiosities. Instead, these are real parts designed to double or triple the critical-path speeds in real applications. And to make them legitimately useful, they have to be compatible with other merchant hardware."

However, the new 100K-compatible parts are not drop-in replacements for 2900 parts. To capitalize on the extra processing power, the designer must optimize off-chip path lengths, clock skew, and other speed-related parameters. So making the parts plug-in replacements would not be desirable, according to Vitesse. The microcode- and 100K ECL-compatibility are there to cut what would have been a monumental system design task down to a reasonably small and quickly dispatched one. □

WOULD HENRY FORD HAVE DONE IT THIS WAY?

Lou Tomasetta, a founder of Vitesse Electronics and president of its IC Division, would like to become the Henry Ford of gallium arsenide digital integrated circuits—which is like saying that he has gone into business to mass-produce Ferraris.

To achieve this ambitious goal, Tomasetta began in mid-1984 to gather together some of the country's top materials research scientists, who at that time had the best understanding of gallium arsenide, and some of the best talents from the commercial semiconductor community, who had the most experience at translating laboratory knowledge into IC manufacturing know-how.

The group was challenged to develop a technology for producing digital LSI GaAs ICs on a production basis rather than the laboratory-specimen basis on which LSI GaAs was then being attempted. Two years and more than $15 million and 50 people later, they have pulled it off.

Three who were there from the start, having been founders of the company, are Tomasetta, Ira Deyhimy, vice president in charge of engineering, and Jim Mikkelson, vice president in charge of operations. Tomasetta and Deyhimy each have more than 15 years experience in GaAs research and development, at Rockwell International Corp.'s Microelectronics R&D Center.

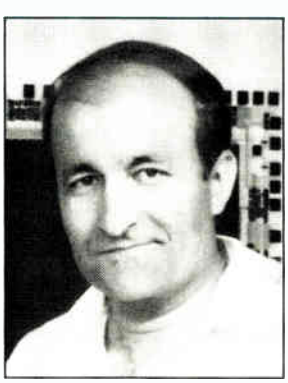
Mikkelson's strength is in the fabrication of high-density, high-complexity silicon ICs. He was responsible for developing the 1-μm NMOS III process used by Hewlett-Packard Co. for its HP9000 32-bit microprocessor chip. Mikkelson and Tomasetta were classmates at the Massachusetts Institute of Technology.

Oddly enough, Mikkelson, rather than one of the GaAs technologists, came up with the outline of a process. His goal, he says, was to make it look as much as possible like n-MOS rather than like the process then in favor for depletion-mode GaAs ICs. "I just didn't let myself get confused by what the others were doing. There were some things we had to do to make GaAs look more like silicon, and a few of those are things we have to patent, so we can't talk about them yet," he says.

After what the developers describe as a "mountain of calculations," the process was proved and refined on paper, and Mikkelson was given the go-ahead to construct his fabrication line. Real verification in the form of functioning circuits from the facility didn't come until 21 months later—at eight in the evening on April 29, when the first VE29G02 carry-lookahead generators were produced from the first product wafer run.

Deyhimy says the products are already going into their second design generation. "When fully qualified parts are available, which should be early next year, they'll be even better," he says.

TOMASETTA



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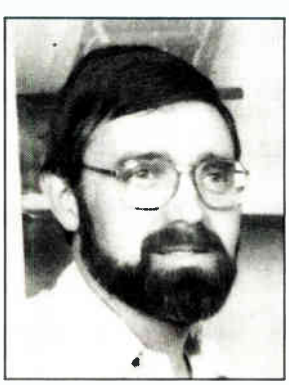

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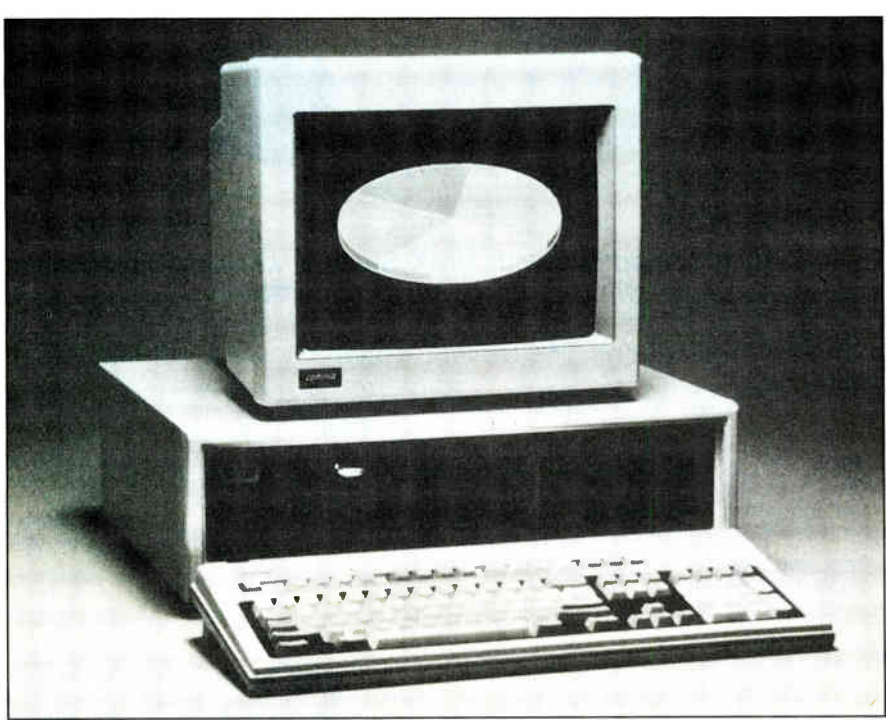
WHAT MAKES COMPAQ'S NEW PC SO IMPORTANT

Based on Intel's 32-bit microprocessor, with its 16-MHz clock rate, the new Deskpro 386 can reach speeds that outstrip any other personal computer

Using Intel's powerful new 32-bit 80386 microprocessor, Compaq Computer Corp. has built a machine that it claims is "the most advanced personal computer in the industry." Key reason: "The single most perceptible characteristic of the product is its blinding speed," says Rod Canion, Compaq's president and chief executive officer.

The speed of the 80386, running at a 16-MHz clock frequency, ensures that the Compaq Deskpro 386 will outperform existing personal computers, including the IBM Personal Computer AT, by a healthy margin [*Electronics*, Sept. 4, 1986, p. 21]. Compaq says that the Deskpro 386 will run most popular microcomputer software packages—such as Lotus 1-2-3, and Ashton-Tate's dBase III and Framework II—two to three times faster than the PC AT. The Deskpro 386's maximum execution rate hits a peak of about 4 million instructions per second. Running code written for a 16-bit 80286-based machine, the Deskpro 386 runs at between 1.5 and 2 mips. An optional Intel 80287 math coprocessor chip boosts performance on floating-point calculations.



1. SPEEDY. The Compaq Deskpro 386 runs most popular applications up to three times faster than an IBM PC AT.

The new Deskpro, however, is not simply a much faster version of older Compaq equipment. "The only thing that hasn't changed is the outside case," says Gary Stimac, vice president of engineering for the Houston computer maker. Besides high speed, the Deskpro offers a number of new features, including larger disk-drive subsystems, a tape cartridge backup, and an optional enhanced graphics card and optional color monitor.

The Deskpro not only represents a technological advance for Compaq, but also something of a corporate declaration of independence. With the introduction of the new machine, Compaq is saying that it is no longer simply a

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manufacturer of IBM PC clones (see p. 69).

The base Deskpro 386 Model 40 will sell for about $6,500; the Model 130 for about $8,800. By comparison, the PC AT is priced at about $5,000. Both Compaq units are available now through the company's network of dealers.

The Deskpro 386 is equipped with one megabyte of random-access memory, which can be expanded to 14 megabytes of internal memory. Powerful 256-K and 1-megabit RAM chips are configured in static column memory, a design that allows the RAM to keep up with the high speed of the 80386 chip.

Two new hard disk drives, one with 40 megabytes of storage capacity, the second with 130 megabytes, were developed expressly for the Deskpro 386. The Model 40 comes equipped with the 40-megabyte drive; the Model 130 with the 130-megabyte drive. Both also have a 1.2-megabyte floppy disk drive. A 40-megabyte tape cartridge drive for hard disk backup is available as an option.

8- AND 16-BIT SOFTWARE, TOO

The Deskpro 386 supports MS-DOS, along with built-in support for the new Lotus/Intel/Microsoft Expanded Memory Specification, which extends memory past the 640-K-byte limits imposed by standard MS-DOS. Also featured is a 32-bit data bus structure that allows much existing software written for 16-bit and 8-bit personal computers to run unchanged.

The concern with compatibility began, in fact, before the microprocessor at the heart of the computer rolled off Intel's production lines. "We worked with Intel in [the] development of the chip," says Stimac. Compaq wanted to make sure that an 80386-based machine would be able to run existing microcomputer software packages written for machines using earlier members of Intel's microprocessor family: the 8088, 8086, and 80286.

Compatibility of another sort was the issue in designing the Deskpro 386's memory subsystem. The fast 80386 requires a speedy memory. If the chip and memory aren't on an equal footing, the 80386 will sit idle, waiting for the instructions and data it needs. Finding a memory subsystem worthy of the 80386 was perhaps the toughest challenge Compaq engineers faced.

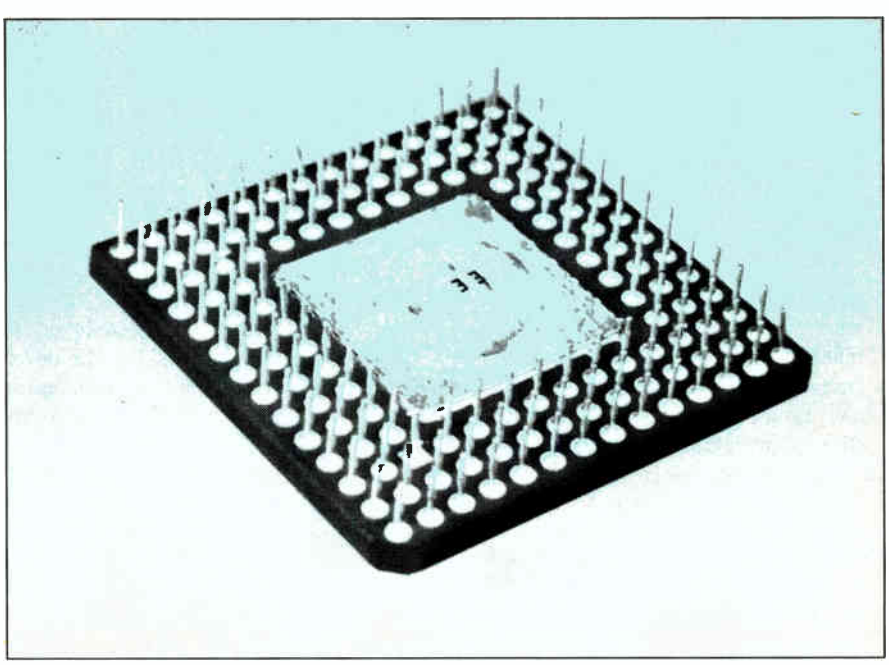
Pure static memory designs offered the best performance, but faster static chips were too expensive to use in the actual product. Compaq engineers investigated cache memory, bank-switched page memory, static column memory, and pure DRAM before finally settling on a static column memory design for the Deskpro 386.

Static column memory is the most recent technique devised to increase the bandwidth of conventional dynamic RAMs. Static column decode systems allow the individual memory chips to operate like static RAMs during the column address portion of the memory-access cycle, resulting in faster access times.

"We found that the most economical solution was using the static column memories. They seemed to complement the [80386] CPU quite a bit," says Stimac. "What also drove us to static column memory was the knowledge that 1-megabit static column chips are going to be standard in the industry. As time goes on, 1-megabit chips will be more cost-effective than 256-K chips, and we'd like to be able to carry through the architecture that way."

The main system memory board uses 256-K-by-1-bit static column memories with 100-ns access time. With the base Deskpro 386, the main system board comes equipped with one megabyte of memory, expandable to two megabytes by plugging additional chips into the board. Plugging in "piggyback" boards on top of the main system board can add as much as 10 more megabytes. Two piggyback boards are offered: a 1-to-2-megabyte board using 256-K-by-1-bit chips, or a 4-to-8-megabyte capacity board using 1-megabyte memories. Another four megabytes can be added by plugging a board into one of the four system expansion slots inside the machine's chassis.

Compaq also expanded the Deskpro's data storage capacities, which were built with an eye to the future. "We're getting prepared for the movement of the industry to higher and higher densities," says Stimac. In the Deskpro 386, that movement is heralded by two completely new



2. LEADER. Compaq says the Intel 80386 chip makes the Deskpro 386 the most advanced microcomputer in the industry.

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half-height hard disk drives: A 40-megabyte ST506-type Winchester drive and a 130-megabyte ESDI (Enhanced Small Device Interface) drive.

The Winchester drive packs 17 sectors on a track, boasts an average access time of less than 30 ms—"state-of-the-art performance," Stimac says—and transfers data at 5 megabits/s. The 130-megabyte ESDI disk drive can seek and find data in less then 25 ms, on average. It transfers data at a rate of 10 megabits/s and stores it at a density of 34 sectors on a track. The controller boards are combined with the drives themselves in integral units. Previously, controllers have been mounted separately. But using surface-mounted devices saved enough space to squeeze the controller board beneath the drive, which not only increases reliability, but also saves a controller-board chassis slot.

The Deskpro runs a version of MS-DOS enhanced to support a memory extension that surmounts the 640-K-byte memory barrier of today's personal computers

For preserving hard disk data, a 40-megabyte tape backup unit is available as an option. The drive packs 40 megabytes onto a single 3M DC2000 cartridge. The storage subsystem transfers data at a rate of 500 kilobytes/s.

While the Deskpro 386 has a full 32-bit data bus, the machine also sports data-bus conversion circuitry, allowing expansion products (such as local-area-network or video cards) that were designed for 8- and 16-bit systems to use that 32-bit bus. The cards, sold by third-party vendors, can plug into the six expansion slots available on the Model 40 or the five slots on the Model 130.

High-quality color graphics are another feature of Compaq's new machine. The Deskpro 386 implements the IBM Extended Graphics Interface (EGA), using a chip set supplied to Compaq from Chips & Technology Inc., Milpitas, Calif. Using Compaq's optional enhanced color graphics board and optional color monitor, 16 colors from a 64-color palette can be simultaneously displayed at a resolution of 640 by 350 pixels.

To control the execution power of the machine, the Deskpro 386 can run version 3, release 3.1 of the MS-DOS operating system from Microsoft Corp., Redmond, Wash. Compaq, with Microsoft's help, has enhanced standard 3.1 MS-DOS with built-in support for the Lotus/Intel/Microsoft Extended Memory Specification. The extension breaks the 640-K-byte memory barrier of today's personal computers. With LIM, applications software can use up to eight megabytes of RAM. "This extension is how Lotus 1-2-3, Framework, Symphony, and Autocad expand the amount of data storage that a program can have," says Stimac. "When you power up, we provide 912-K bytes for Lotus 1-2-3 to be expanded [in the 2-megabyte Deskpro 386]. In the 1-megabyte Deskpro 386, users get approximately 256-K bytes of space for Lotus 1-2-3 and Framework."

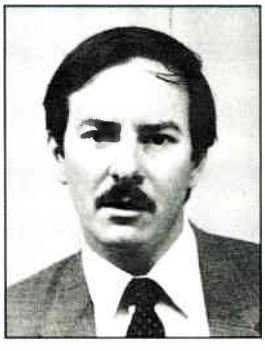
MS-DOS 5.0, an operating system that will support the 80386 chip and can access up to 16 megabytes of RAM without LIM extensions, is said to be currently under development at Microsoft. Compaq executives will not comment on MS-DOS 5.0, but that system is a big part of the software activity surrounding the 80386 (p. 91).

Another operating system now under development at Microsoft, the Unix-like Xenix System V/386, will be available in the first half of 1987. That will be the first operating system to take full advantage of the 80386's 32-bit architecture, with virtual memory mode, larger address space, and memory paging features. Xenix System V/286, which is currently available, and applications written for it can run on the Deskpro 386 without modifications. □

COMPAQ'S STIMAC GOT VERY CLOSE TO INTEL

One thing Gary Stimac has learned since he joined Compaq Computer Corp. in 1982 is how fast microprocessor technology moves. In the past four years, Stimac, Compaq's vice president of engineering, has worked on computers based on four different Intel microprocessors. Compaq's first machine featured the 8088. The original Deskpro, introduced in 1984, used an 8086 chip. Last year's Deskpro 286 was built around Intel's 80286 microprocessor. And, for his latest act, Stimac led the design of the Deskpro 386, which uses the 32-bit 80386.

The 80386 is far more powerful than any of its predecessors, but working on those earlier machines was valuable training for the Deskpro 386 project, Stimac says. "The only way we could have developed the Deskpro 386 to be as compatible as it is," he says, "is to have lived through developing an 8086 machine, a 286 machine, and then worked with the 386."



GARY STIMAC

This time around, Compaq not only designed the computer, but got deeply involved in the design of the chip itself. "I had weekly conversations with Gene Hill, who ran Intel's 386 program development," Stimac says. "When different problems came up we worked with the architect of the 386, John Crawford. The normal barriers between two companies were completely broken down, and we worked on issues and problems like we were friends and neighbors."

Stimac first joined Compaq's software group, where he helped to develop Basic and DOS systems software. In 1984, he was tapped to manage the development of the 8086-based Deskpro computer. He went on to lead the Deskpro 286 development project and then, in early 1985, the Deskpro 386 project.

Stimac, 35, holds a BSEE from the Milwaukee School of Engineering. Before joining Compaq, he spent nine years at Texas Instruments Inc. as an engineer and program manager.

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COMPAQ DECLARES ITS INDEPENDENCE

Compaq Computer Corp. sees its new Deskpro 386 32-bit personal computer as the vehicle that is going to move the company out of the long shadow of IBM Corp., helping it to shed the label of "clone maker" as it goes. Compaq executives believe, in fact, that the new machine will redirect the entire personal computer industry beyond IBM's standards and toward Intel Corp.'s 80386, the 32-bit microprocessor that is the heart of the 386.

The 80386 will give the personal computer the power of a minicomputer, says Compaq president Rod Canion. He thinks machines built around it will have the punch to open new vistas for personal computer users, ranging from desktop expert systems to scientific computing. Such machines mean that Intel, not IBM, will be setting the standard for the next generation of personal computers, he believes.

For Compaq, the blindingly fast 386 represents the boldest bid yet to whittle away at IBM's dominance in personal computers. Canion believes that the 386 has the power to enable the company to blaze its own trail, after 4½ years of adapting to the standards set by two generations of IBM PCs. "The Deskpro 386 could change the whole nature of this company and the way we are viewed by the outside world," Canion says. "It could move us to a new phase of growth."

OTHER PRODUCTS COMING

Canion cautions that Compaq won't neglect the rest of its product line, its portable and Deskpro 286 machines. "You will see other portables and other kinds of computers coming from Compaq," says Canion. In fact, last week, reacting to IBM's announcement of an 80286-based Personal Computer XT Model 286, Compaq came out with a new model of its Deskpro 286 and cut some prices. Still, Canion says the 386 "may very well be the most important product we have ever done, including the first," which was introduced after Canion founded the Houston company in February 1982 with two colleagues from Texas Instruments Inc. That first IBM-compatible portable started the company toward the No. 2 spot in sales of microcomputers to business buyers.

Compaq got to be No. 2, however, by shadowing No. 1—IBM. The introduction of the Deskpro 386, coming well in advance of any 80386-based desktop that IBM might produce, amounts to a declaration of independence for personal computers running the standard MS-DOS operating systems from Microsoft Corp. in Redmond, Wash. "It is a strategic move, and very likely a shrewd move," says Seymour Merrin, vice president and personal computer analyst at the Gartner Group, in Stamford, Conn. He does not expect an equivalent machine from IBM before late 1987.

Canion maintains his company is not attempting to set a standard for 32-bit desktop machines. Intel has already done that, he says. "The processor itself is fixed. The 80386 is the natural evolution of the Intel family. It is going to be the next generation, even if IBM has a diabolical plot to change their own version of the 80386. [If so,] that would not be an Intel 80386."

Canion believes IBM is planning future PC products—including a new operating system for the 80286 models—that would depart from the current MS-DOS standard. "I believe IBM will try very hard to move [its PCs] in a proprietary direction, but I believe it is not Compaq versus IBM but rather the whole industry versus IBM," he says. "My point is, even though the Deskpro 386 is a major move for us, we believe we understand very thoroughly what it means and if there are risks or not. We are very convinced that there are few, if any, risks."

Intel has set the 32-bit standard, says Compaq's Rod Canion. The 80386 is 'going to be the next generation even if IBM has a plot to change its own version'

Even if there are risks for Compaq, many analysts believe the move is relatively safe for the company, simply because it has grown large enough to recover from what only a few years ago might have been fatal errors in market judgment. In its first full year of operation in 1983, Compaq posted $111.2 million in revenue on the strength of a single IBM PC-compatible portable using the Intel 8088 microprocessor. In this fiscal year's second quarter, which ended June 30, Compaq netted income of $9.6 million and sales of $147.1 million—increases of 70% and 24%, respectively, compared with the same period a year ago.

In 1983, Compaq sold 47,000 units; market research firm Future Computing Inc. predicts that the company will sell 316,000 computers this year (table). In contrast, IBM sold 538,000 PCs in 1983

PERSONAL COMPUTER SALES TO END USERS (WORLDWIDE)

	Units in thousands			
	1983	1984	1985	1986 Projected
Compaq	47	142	244	316
IBM	538	1,375	1,793	2,270 (includes RT PC)

SOURCE FUTURE COMPUTING

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CANION: "The Deskpro 386 could change [Compaq] and the way we are viewed. It could move us to a new phase of growth."

and is expected to sell some 2,270,000 of the various PC models this year. Canion declines to estimate how many Deskpro 386s will be shipped.

Until now, the biggest risk the company has taken was the introduction, in 1984, of an 8086-based desktop computer, the original Deskpro [*Electronics*, June 28, 1984, p. 56]. Six weeks after that machine was unveiled, IBM launched its 80286-based PC AT, causing Compaq to rush the AT-compatible Deskpro 286 to market in early 1985.

Whatever risks Compaq is taking with its latest Deskpro, it will not be taking them alone—some 20 to 30 other 386-based machines are expected this year. Moreover, the company's continued record growth has given it impressive status in the eyes of recession-weary computer industry executives, and some of them have become Compaq's allies. For example, on the day the Deskpro 386 made its debut, there were testimonials from the presidents of software vendors Ashton-Tate and Lotus.

Compaq will maintain its dealers-only policy for the distribution of the Deskpro 386, believing they are 'the only effective means of selling these types of products'

Edward M. Esber Jr., president and chief executive officer of Ashton-Tate, in Torrance, Calif., says the new Deskpro will run software two to three times faster than the average IBM AT. And James P. Manzi, president of Lotus Development Corp. in Cambridge, Mass., says he believes Compaq is setting the stage for advances that "will allow us as a company to do whole new applications that we cannot envision today."

INTEL, MICROSOFT HELPED

Intel and Microsoft—prime contributors to IBM's early lead in the personal computer contest—worked behind the scenes with Compaq during the development of the 32-bit Deskpro. Intel provided early prototypes of the 32-bit 80386 to Compaq designers. In return, Compaq gave the initial 80386 chips a test run to determine their compatibility with MS-DOS.

"The way I view the 386, it was a three-way joint development to ensure compatibility," says Gary Stimac, Compaq's vice president of engineering. Some bugs were found and fixed by Intel, he says. Microsoft wrote part of the Deskpro 386's extended memory manager, breaking the 640-kilobyte barrier of today's MS-DOS-based personal computers. Microsoft and Compaq started talking about 32-bit personal computers two years ago, according to William H. Gates, Microsoft's chairman.

Compaq also has an ally in its network of dealers. The company, believing its dealers are mature enough for 32-bit computing, plans to continue its dealer-only distribution strategy with the Deskpro 386. "At the right price-performance [ratio], the dealer channel of distribution is the only effective means of selling these types of products," says Michael Swavely, Compaq's vice president of marketing. In an effort to build strong dealer loyalties, Compaq has elected not to sell units directly to large corporations or value-added resellers. Instead, the company has maintained a "dealer's associate program," which channels VAR sales through the dealers.

For example, Gold Hill Computers Inc. of Cambridge, Mass., a supplier of artificial-intelligence software, has placed a large order for Deskpro 386 computers through Businessland in Boston and plans to use them as a delivery system for a future product. Compaq says it has some 300 dealer associate programs in the U. S., giving it a dealer channel into specialized hardware and software markets.

"The dealer channels have been evolving significantly toward the value-added type of applications for personal computers," says Swavely. About 50% of Compaq's dealers are selling systems for computer-aided design and computer-aided engineering, and about 25% for multiuser environments. Swavely believes that as personal computers get more powerful, the dealers will quickly accommodate them. "Five years from now we will be deciding whether we can sell mainframe power through these dealer channels," he predicts. *–J. Robert Lineback*

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FIRST LOOK AT MOTOROLA'S LATEST 32-BIT PROCESSOR

Due next year, the 68030 microprocessor will double the performance of the 68020 by adding parallel functions, a data cache and an on-chip memory-management unit

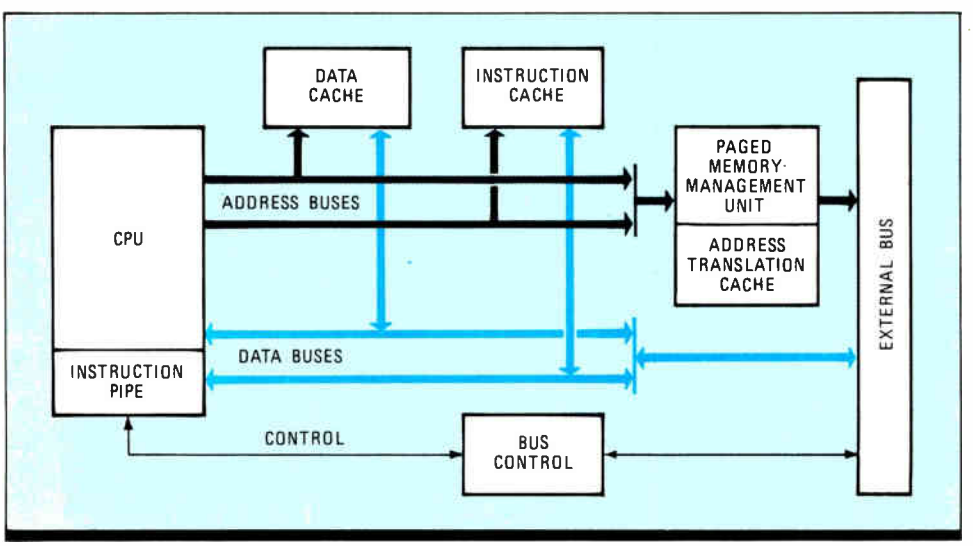
The successor to one of the brightest stars of the 32-bit microprocessor world is more than a year away from volume production, but Motorola Inc. is ready to disclose details of its upcoming MC68030. An advance look reveals that the chip maker will add such features as a data cache and on-chip memory management that will at least double the performance of the existing 68020.

Parallel functions are also being expanded to help speed up the company's latest chip. Added functions include twin parallel buses for on-board data and instruction caches, the capability of filling the caches with data from external memory as the central processing unit simultaneously executes instructions, and the capability of sending addresses to a memory-management unit to begin searching external memory while the buses search on-board caches.

The 128-pin CMOS chip—which will be fully source-code compatible with the 68020—should be operational late in the first quarter of 1987. Samples are slated for early next summer, with volume production beginning around October. The 68030 is targeted not only at engineering work stations but also at the personal computer market, a stronghold of Intel Corp.'s iAPX 86 processor family since IBM Corp. selected the 8088 for its Personal Computer.

Motorola is also planning to introduce next year a new 68-pin floating-point processor, designated the MC68882. The 20-MHz coprocessor will be pin-for-pin compatible with the existing MC68881, but its enhanced parallel architecture is expected to boost performance two to four times (see "A speedy new coprocessor, too," p. 72).

The 68030 will be slightly larger than the 68020 because of the added circuit elements. But its central processing unit is identical, and many features will be basically the same. The same modes support high-level languages; the new microprocessor also has the same flexible coprocessor interface, three-stage instruction pipeline, sixteen 32-bit general-purpose data and address



1. PARALLELISM. The speed of the 68030 microprocessor is enhanced by data and instruction caches and twin pairs of 32-bit internal buses.

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registers, two 32-bit supervisor stack pointers, a 32-bit program counter, 18 addressing modes, memory-mapped input/output ports, and a dynamic bus-sizing mechanism. Dynamic bus sizing allows the processor to transfer operands to and from external devices while automatically determining the port size of those chips on a cycle-by-cycle basis.

Like the 68020, the 68030 will be object-code compatible with the 68008, 68000, 68010, and 68012 microprocessors. The execution unit contains one arithmetic logic unit and two arithmetic unit blocks, also like the 68020.

The 68030 is based on 1.2-μm design rules optimized to yield minimum clock speeds of 20 MHz, though Motorola will also have versions that run at 16.7 MHz. By contrast, the 68020 began with design rules optimized to yield clock speeds of 16.7 MHz. The 68020 recently topped out at 25 MHz through process shrinks and fabrication tweaks. Judging by the 68020's history, the 68030 should reach speeds of at least 30 MHz, although Motorola refuses to commit itself to a maximum speed.

Target clock speed for the first version of the 68030 is 20 MHz, but after process shrinks and fabrication tweaks, it might eventually hit a top of 30 MHz

Three important changes stand out among the enhancements made to the 68030. All of them implement, in one way or another, the parallelism built into the new device. A 256-byte data cache and a paged memory-management unit have been added, and the bus controller has been enhanced for parallel operation with a burst mode that can feed bytes to the data and the instruction cache while the execution unit is performing computations that will be used by the CPU.

The data cache can send 32 bits to the execution unit in a single clock cycle. The 68020, by contrast, has a two-clock instruction cache but no data cache. Because data has to come from an external cache or main memory over the system bus, getting an instruction ready to execute takes a minimum of three or four clock cycles.

"Bringing memory management on board has enabled us to put the data cache on the chip, and that was one of the biggest motivations in the design," says Jack W. Browne Jr., marketing manager for the 68000 family. Teaming the data cache with the instruction cache will allow the 68030 to execute more cycles without accessing the external system bus. The system bus is then free for other system processors and controllers to use, notes Russell Stanphill, advanced product engineer with the 68030 project.

The 68030's instruction cache is the same size as the the 68020's, but it is better organized and faster—the CPU can access one full instruction in the instruction cache in one clock cycle. These improvements increase the hit ratio, the percentage of the time the cache holds the data the CPU wants. To help deliver information from the caches to the CPU more quickly, the Motorola designers added parallel pairs of 32-bit data and address buses (Fig. 1), which run at 80 megabytes/s; the external bus transfer rate is 40 megabytes/s. "The two separate 32-bit data and address buses allow simultaneous access to both caches, while allowing us to fetch an instruction and an operand at the same time," says Stanphill.

To improve the likelihood of cache hits, Motorola is also reorganizing the 256-byte instruction cache into 16 entries of four long words each with four bytes per word. The 68020 instruction cache consists of 64 entries each of one long word. The new data cache on the 68030 is organized the same way as the new instruction cache (Fig. 2). The reorganized instruction cache, along with the new burst-mode addressing methods, should double the cache-hit ratio and reduce the number of times the 68030 must access the system bus.

"By having the on-chip caches and having them operate more effectively with higher hit ratios, we can readily support more complex system architectures," says Stanphill. "We expect the external bus accesses of this part to be significantly fewer than in the 68020." In fact, he adds, "You could take away the external bus and this chip would keep executing internally until it misses a hit in on-chip cache. This is a complete processing core."

If neither cache contains the

A SPEEDY NEW COPROCESSOR, TOO

Additional bus interface logic and dual-port registers will add new parallelism to the architecture of a future floating-point coprocessor from Motorola Inc. The second-generation MC68882 coprocessor will be a direct plug-in replacement to the existing 68881, but the new 20-MHz chip will outperform the existing unit by two to four times, according to Motorola.

The 68-pin 68882, which is expected to be operational by year's end, will fetch operands and perform in parallel the necessary data conversions for floating-point math in the bus interface portion of the die. The 68881 uses its execution unit to convert incoming data into the required internal format. Dual-port floating-point registers in the new 1.4-μm CMOS chip will support concurrent loading, storing, and computation of the data.

These features involve "a relatively simple and minor change to the die, but it allows much higher parallelism in the part, which can directly double the performance of 68881 code," says Russell Stanphill, an advanced product engineer. By coding the software to take advantage of the 68882's pipelined operations, Stanphill says it will be possible to get four times the performance.

The 68882 may be used with either the 68020 or the 68030 32-bit microprocessors. Volume production is expected to begin next summer.

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wanted information, the 68030 can execute a performance-boosting flank maneuver. While the parallel buses are accessing the caches, addresses are forwarded simultaneously to the on-board paged memory-management unit. The paged MMU translates and holds these addresses in its translation cache. "If you do not have a hit in cache, the translated address is available at the external pads of the 68030," says Stanphill. "All you have to do is an enable to the external system bus, and you are already a big portion of the way to fetching the information from an off-chip source."

The result is that, in the event of a cache miss, the 68030 can access the system bus with a physical address in just two clock cycles. The 68020 takes three clocks to produce a logical address for a peripheral MMU. "Accessing the data cache while simultaneously translating addresses in case the data is not in cache is a technique employed in some computer architectures for a number of years, but as far as I know no one has done it on an integrated circuit," says Stanphill.

Putting a paged MMU on the 68030 marks a reversal of Motorola's practice with the 68020. The company believed that the CMOS technology of 1984 could not support both on-chip MMU and the other features it wanted to include on the chip. The 1.2-μm CMOS technology used on the 68030 makes it feasible to put the main subset of the paged MMU on the new processor, saving real estate, lowering power consumption, and, Browne estimates, cutting component costs by about 20%.

When it designed the 68020, Motorola also figured that different system houses had different ways to manage memory, and that it should leave the choice open for them. Some 68020 customers implemented their own memory management. Others used Motorola's peripheral MMU chips, such as the early 68461 logic-array-based chip and later the 68851, a more-powerful paged MMU.

For those customers, the 68030's paged MMU is a code-compatible register subset of the

NO SECOND SOURCE FOR THE 68030?

What a difference five years and an early market lead can make. Motorola Inc., once the aggressive wooer of alternate-sourcing pacts for its 68000 microprocessor family, is going to play very hard to get when it comes to sharing the manufacturing rights to the 68030.

Product managers in Austin, Texas, now believe the industry may at last be ready for sole-sourced 32-bit microprocessors. In return, Motorola pledges much closer cooperation between the chip vendor and buyer.

"Our position is you don't have to have a second source to be successful. We can give the customers what they want and guarantee delivery as well as an aggressive pricing schedule," maintains Jack W. Browne Jr., manager of marketing and applications engineering for the 68000 family. "We are not finding it as difficult to share advanced information [with customers]. Both sides are finding it easier to talk without requiring the other side to commit itself to something."

Some Motorola managers want to go it alone

Motorola is working with about 14 customers to establish just-in-time delivery services, says Browne. Recently installed process controls and testing systems at the company's microprocessor plant in southwest Austin are an important step in establishing JIT service, he says.

And as its investment grows, Motorola's asking price for the sourcing rights to the 68030 is also going up. "We are not interested in handing over microprocessors to companies that have not had the overhead it takes to create a market for the chips. We are firmly committed, as we have been [on the 68020], that we want equal value from a second source," Browne says.

The general manager of the Microprocessor Products Group, senior vice president Murray A. Goldman, will say only that a decision on whether to seek a second source for the 68030 has not been made. "I cannot talk about second sourcing on a product that has not been introduced yet," he says. "We've got our blinders on and want to get that product out.... If we were working closely with anyone else, it would hinder us." But Motorola executives are greatly encouraged by the firm's ability to meet the demand for the 32-bit 68020 alone during the past two years.

At the time of initial disclosure in 1982, the 68020 became a key attraction for most of the five 68000 second sources recruited by Motorola in the early 1980s. Motorola, attempting to overcome Intel Corp.'s lead in 16-bit chips, had signed pacts with Hitachi, Mostek, Rockwell International, Signetics, and Thomson-CSF. Motorola was willing to swap the designs for central processors, coprocessors, and memory-management chips for a wide variety of much needed peripherals. High-volume microprocessor buyers also insisted on having more than one source for 16-bit and future 32-bit chips.

But after the 68020 introduction in mid-1984, Motorola's push for partners cooled as the industry fell into its worst recession. Encouraged by its jump on archrival Intel in the 32-bit race and by new fabrication lines in Austin, Motorola toughened its trading demands. Bids were repeatedly turn down from Hitachi, Mostek (then a subsidiary of United Technology Corp.), and Signetics. Only Thomson had a provision in its 68000 contract giving it a right to make the 68020. Still, Motorola and Thomson (now owner of Mostek) have not come to terms over the transfer of 68020 mask and production technology. By default, then, Motorola is the only source for the 68020.

"We have not had any problems from any customers over being a sole source for the 68020," notes Browne. In fact, Motorola plans to keep 68020 buyers happy in the future by driving the price so low that it will be thought of as a commodity chip. Last June, the cost of a 12.5-MHz 68020 was reduced to $174 each in 100-piece quantities. The 1984 introductory price was $487. Prices on the 68030 have not yet been set, but Motorola is planning to drive costs down quicker on that chip.

"We are going to be extremely aggressive, and we think the volumes will turn on for this new product faster than they did for the 68020," says Browne. The full impact of Motorola's manufacturing learning curve is expected to greatly cut the price tag of the 68030 about 18 months after next year's introduction.

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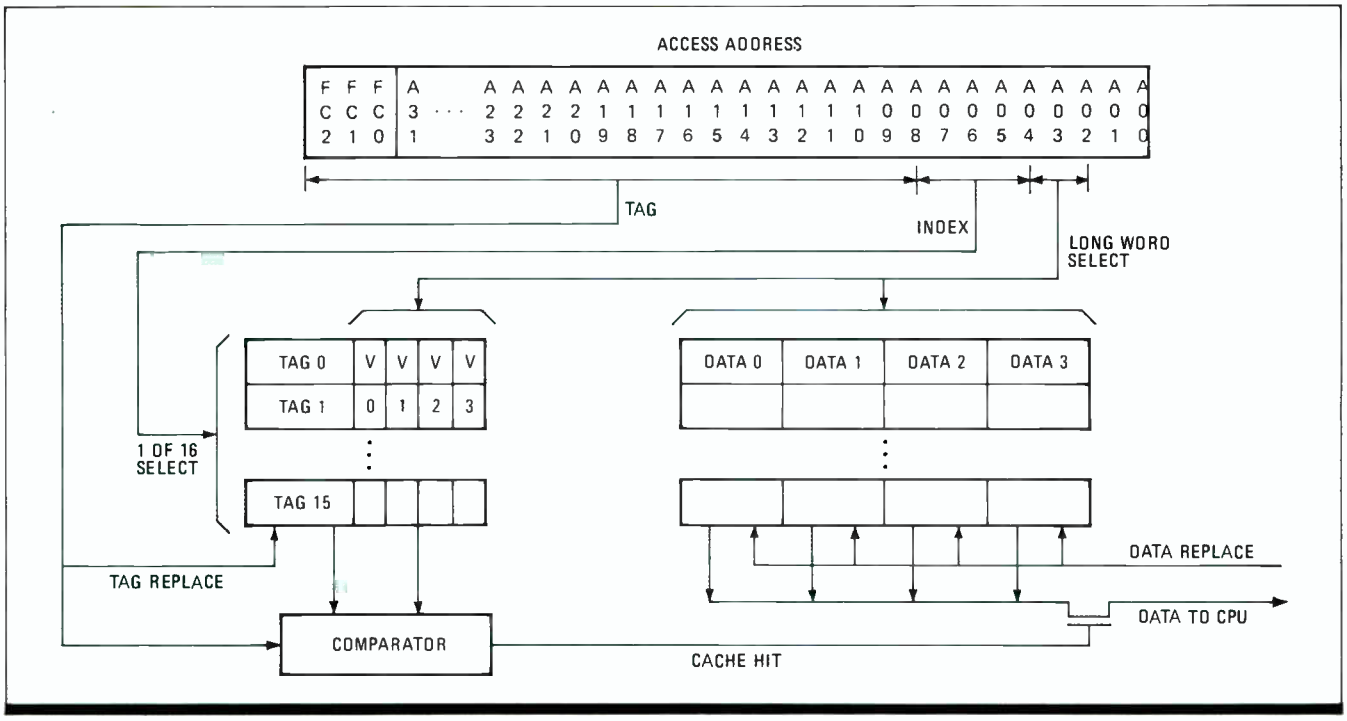

2. DATA CACHE. The on-chip data cache is structured as four-word blocks, each 4 bytes long. It holds 16 such blocks for a total of 256 bytes. The 68030's instruction cache is organized the same way, a setup that improves the likelihood of cache hits.

68851. It supports all the descriptors from the 68851, omitting only a few of the peripheral's infrequently used features—test and diagnostic support for off-chip functions, for example. It will, however, address the full 4-gigabyte address space available to the 68020 and 68851. The 68030 will also support the same 256-byte to 32-K-byte page sizes. However, any Motorola customers who want to implement their own memory-management techniques can still do so. Motorola has designed the on-chip MMU so that it can be disabled by software or external hardware.

One example of 68030 parallelism is the enhanced bus controller, which frees the CPU from the task of filling the data and instruction caches from external memory

The third major addition to the 68020 is an enhanced bus controller, which supports a burst mode that, in effect, anticipates the needs of the CPU and independently fills the data and instruction caches with bytes from off-chip memory. While the 68030's execution unit is performing computations, the bus-interface unit simultaneously interrogates the cache, checking it against the accesses being made by the CPU. Modulo 4 arithmetic is used to determine whether the cache's content is likely to be needed by the execution unit.

The same Modulo 4 addressing mechanism is contained in many of today's dynamic random-access memories that feature ripple-burst modes of nibble, page, or static-column decode, says Stanphill. This look-ahead cache-filling mode will enable customers to use low-cost DRAMs instead of static memories. The burst-mode memories automatically generate the second, third, and fourth accesses according to the Modulo 4 addressing scheme, sending bits back to the processor on every subsequent clock edge. "That means the burst mode will supply data on every clock edge, driving the transfer rate to about 64 megabytes per second," adds Stanphill.

For more conventional external memory subsystems, the 68030 can work in a new synchronous bus-control mode. In this mode, only two clock signals are needed to access external cache. In contrast, the 68020 uses three clock phases to access external cache over an asynchronous system bus, with the extra clock phase serving to pass incoming bytes through the synchronizing logic.

Because incoming synchronous data need not pass through a synchronizing logic circuit, the 68030 has an extra half-clock phase added to its memory-access window. The result is faster transfers with a wider window for slower and often lower-cost SRAMs, says Stanphill.

68030 control pins will be able to switch the bus-control interface between synchronous and asynchronous modes on the fly. The three-clock asynchronous mode would still be needed to communicate with such processors as peripheral controllers.

In addition, new pins have been added to the 68030's bus-interface unit for system development support. For example, a system designer

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can disable the on-chip caches and MMU, freezing their content, and then use two of the new pins to interrogate the conditions and follow the flow of instructions with emulators or analyzers during system development or debugging. A new refill pin also tells designers when the part's internal instruction pipe has been flushed and if all the instructions have been used.

Motorola executives in Austin promise the 68030 will be well worth the wait. "New CMOS technology, greater chip integration, the increased parallelism, and the processor's ability to run fast with inexpensive DRAMs by using the burst mode all add up to 68030-based systems costing about half the price of current computers using the 68020," says Browne.

Besides cutting down on system costs by its integration of features on the 68030, Motorola plans to drive down the cost of the chip itself with volume manufacturing. The manufacturing muscle for the 68030 is being exercised on a new 25-ns 64-K SRAM, which has become Motorola's latest process driver for advanced silicon-gate CMOS [*Electronics*, Aug. 7, 1986, p. 81]. When the 68030 goes into production next year, its 1.2-μm silicon-gate version of CMOS technology will result in fully packed 16.7- and 20 MHz microprocessors that dissipate less than 2 W. Faster parts should appear after 1987.

Initially, the 68030 will be available in a ceramic pin grid array. Motorola expects the low power dissipation resulting from the 1.2-μm process will allow the company to place the 32-bit microprocessor in low-cost plastic packages.

"We feel very comfortable saying you will be able to take this product and use it as the basis of a $2,000 system. That system would deliver a minimum of four MIPS—most likely, it will be around six to eight," says Browne.

In Motorola's view, system designers too often conclude that they can't afford the processing power that 32-bit microprocessors provide, and end up using 16-bit microprocessors instead. "Today, everyone perceives the 16-bit microprocessor as a commodity," Browne says. "We are now ready to turn the 32-bit market into a commodity market rather than one that trades dollars off for MIPS. There is no reason why it should be a market of tradeoffs."

"We want to get the 68030 into the office-automation marketplace, where the 68020 is just now emerging with our lower prices," says Jeff Nutt, technical marketing manager for the 68000 family, referring to a recent 48% price reduction on the 12.5-MHz 68020. "The 68020 will continue to be used in some applications, like controllers, where customers might want to stay with their own memory-management techniques or in areas where there's not a need for a data cache. But I believe most people will move over to the 68030, just as customers have migrated from the 16-bit 68000 to the 68020."

To make that movement easier, Motorola maintained the same instruction sets and programmer models used on the 68020 and 68851 memory-management peripherals. The 68030's cache-controlling registers accept the same instructions as those for the 68020 and 688521 chip set. "No instructions were added to the chip for the control of the on-board data cache. We just expanded the existing registers. So the same instructions manipulate more bits within the chip's paged MMU," says Stanphill. "We are doing everything we can to make sure this is an easy migration from the 68020 world." □

KEEPING A STEP AHEAD OF THE COMPETITION

The job of topping the 32-bit 68020 at Motorola Inc. is being carried out on three fronts with a staff of about 30 circuit engineers, system architects, and chip-layout experts. The task blends the familiar—the 68020's central processing unit—with the new—namely, a highly parallel architecture and a new 1.2-μm CMOS process.

And for the man heading Motorola's MOS microprocessors over the past eight years, the 68030 is a critical bid to stay ahead of the competition in 32-bit chips. "We introduce a lot of products out of our different organizations," notes Murray A. Goldman, senior vice president and general manager of the Microprocessor Products Group in Austin, Texas. In addition to CPUs, the group handles microcontrollers, digital signal processors, and peripherals.

"Sometimes they are singles. Sometimes they are nothing, and sometimes they're home runs. The 68020 was a grand slam, and obviously we want to maintain the momentum," says Goldman, a 17-year veteran of Motorola who joined the company's semiconductor sector in Phoenix after working six years at Bell Laboratories and earning a PhD in electrical engineering from New York University in 1969. Seven years later, Goldman joined Motorola's small but growing microprocessor operation in product engineering. In 1978, he was named operations manager.

GOLDMAN

"I've been in the same job since, but the job has gotten bigger," he adds, referring to the operation's growth into full-group status with its own plant site on the southwest side of Austin. Planning for the 68030 began several years ago with Goldman's strategist selecting 1987 as the window for a second-generation product introduction. "We decided to have a 1987 offering that was on the order of seven to eight VAX-system MIPS in order to maintain our goal of 300% to 400% performance advantage over the competition," says the 48-year-old executive.

The system-design team—accounting for about a third of the total 68030 effort—set its aim on a high-performance parallel architecture. Circuit designers and chip-layout teams targeted a process that would eventually achieve a low-cost 32-bit chip for systems priced below $5,000 after 1987.

The 68030 team has also borrowed from Motorola's earlier efforts on the 68020, implementing the 32-bit chip with breadboards of TTL to prove out concepts born on a vast supply of computer-aided design stations. "We don't do that with every project, but some projects are so important we'll do it," adds Goldman confidently.

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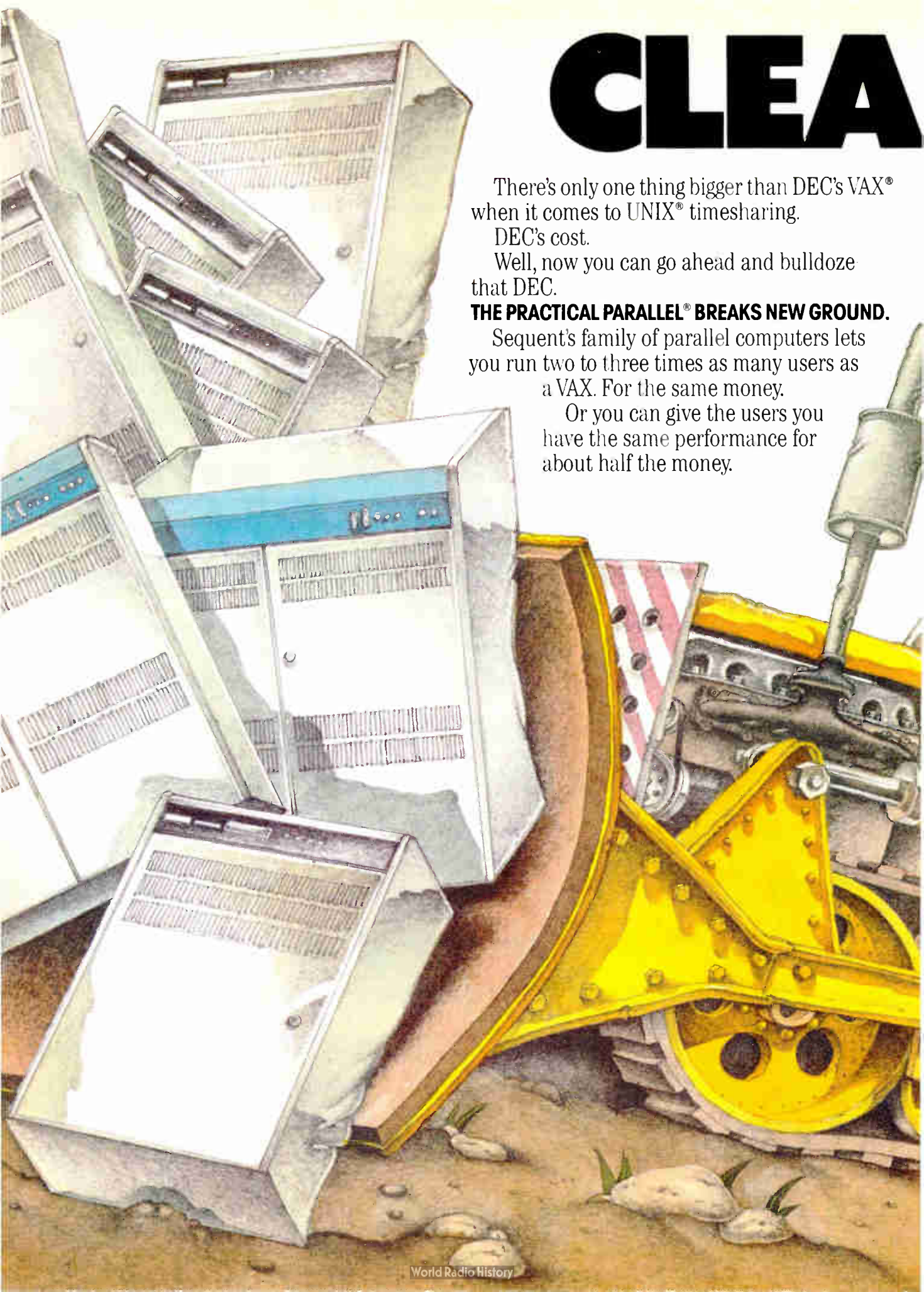

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TI'S BLAZING-FAST CMOS LOGIC TAKES ON SCHOTTKY BIPOLAR

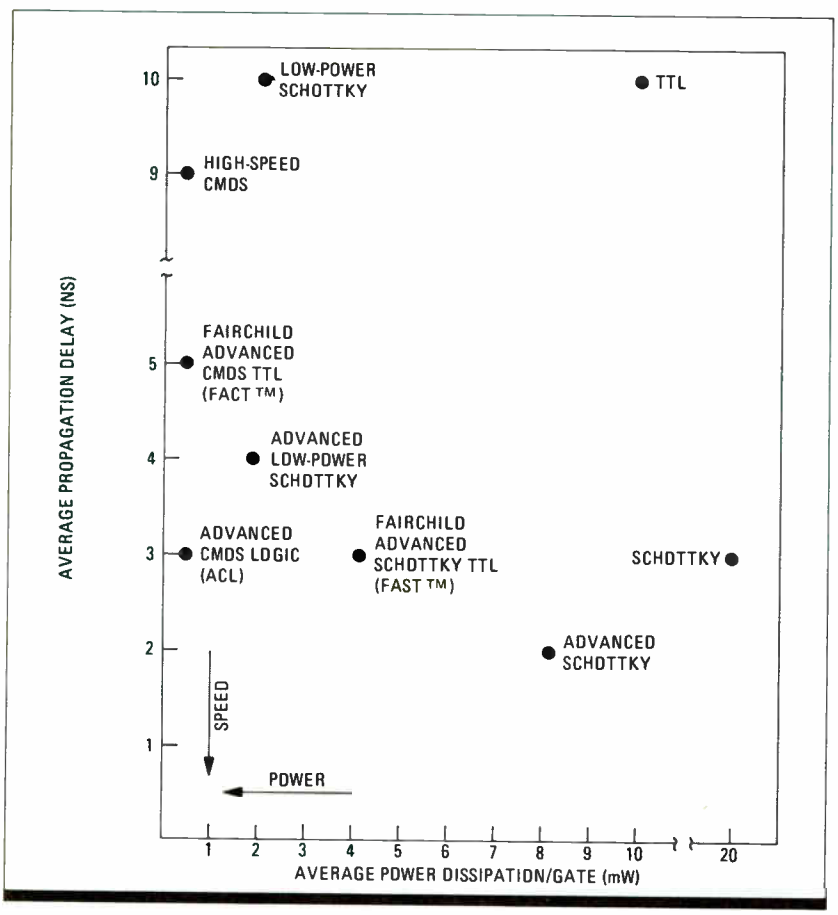
An innovative twin-well process, a novel pinout, and close attention to latchup and to electrostatic discharge help boost the performance into bipolar territory

A new contender in the race to put CMOS logic parts on an even footing with Schottky TTL is coming from Texas Instruments Inc. The Dallas company's advanced CMOS logic parts switch data at an average propagation delay of 3 ns, matching the time of Fairchild Semiconductor Corp.'s FAST TTL family. The impressive specs of TI's ACL parts include a 24-mA drive-current capability and an upper frequency limit of 200 MHz.

That combination means many systems previously implemented with bipolar logic can be built more cost-effectively in CMOS. Sharing the credit for the performance of the TI ACL parts are an innovative twin-well process that builds 1-μm-long gates and a novel pinout. Also important for performance is the close attention TI gave to fighting off latchup and electrostatic discharge.

The cost-effectiveness of ACL begins with its power/delay product, which is a considerable improvement on TI's older HCT (high-speed CMOS with TTL levels) and HC (high-speed CMOS) technology. As measured by the standard power/delay figures of merit for logic device performance, both families consume about the same power, but ACL's 3-ns propagation delay is three times better than HC's time (Fig. 1). In fact, ACL families lead all logic families in terms of speed/power performance. Advanced Schottky (AS) is faster but consumes far more power.

In addition, ACL is unique among CMOS families in its high drive-power capability. In the high switching-speed environment of modern digital systems, logic chips often must drive 50-Ω transmission lines at frequencies in the tens of megahertz. Until now, current-operated bipolar chips were better suited to such conditions than were voltage-operated CMOS parts. The 24-mA drive capability of TI's ACL series, however, is more than adequate to drive 50-Ω lines



1. FRONT-RUNNER. Power-delay product is the best overall indicator of a logic family's efficiency. Advanced CMOS logic (ACL) offers the highest power-delay product of any current digital ICs.

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at frequencies greater than 200 MHz.

Besides its speed and drive features, TI's ACL retains the operating characteristics that made its CMOS predecessors a desirable alternative to bipolar technology. These include high noise immunity, a wide supply-voltage range of 3 to 5.5 V dc, and operation over –40°C to 85°C for industrial versions and –55°C to 125°C for military parts. Like all CMOS logic, ACL parts dissipate power at microwatt levels when in standby mode. The new family is fully compatible with both TTL and CMOS input levels.

To support ACL system designs, TI's opening salvo will feature a wide range of general-purpose parts to interface microprocessors, memories, and other very large-scale integrated circuits. The first spate of offerings will include 16 gates and Schmitt triggers, 21 multiplexer/demultiplexers and flip-flops, 23 line drivers and receivers, 24 latches and shift registers, 14 counters, and 7 arithmetic support chips. All will be available in military and commercial grades by the first half of 1987. Commercial parts will come in plastic dual in-line packages as well as small-outline surface-mount packages.

As ACL moves into the general-purpose-logic stage, it faces stiff resistance from established TTL types—FAST, for example. Moreover, there is always an operating frequency at which TTL and CMOS parts consume the same power, a point called the crossover frequency (Fig. 2).

In comparing dissipation of an ACL gate and a FAST gate, the crossover frequency is 30 MHz when both operate at the same temperature, load, and supply voltage. To conserve power, therefore, a designer is better off using ACL chips in circuits that switch at average frequencies below 30 MHz. The higher the crossover frequency, the greater the impact of a given CMOS technology on the design.

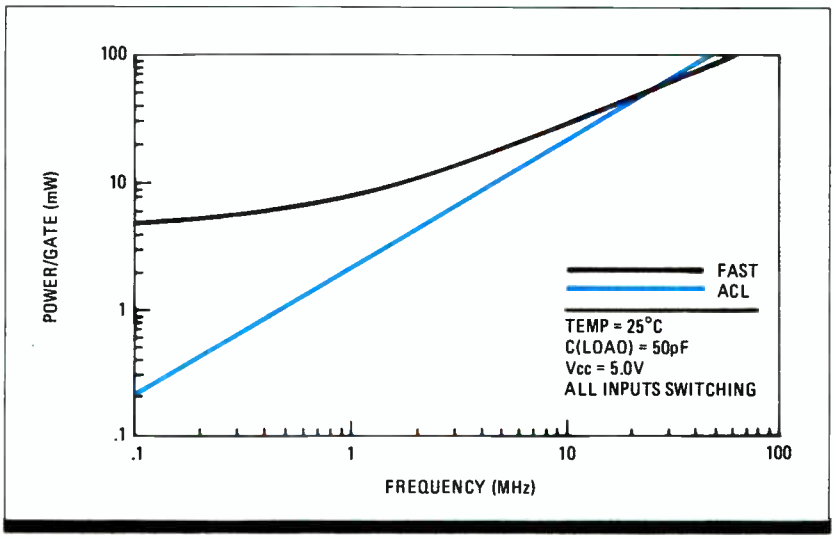
Power, however, is often oversimplified when discussing CMOS devices. In many instances, only the static dissipation of a CMOS logic function is compared to its TTL counterpart. This makes CMOS look highly favorable, but power considerations in system design are actually far more complex. A system's total power consumption takes in three factors: static power, measured when a device has steady-state voltages on its inputs; switching power, when it is active; and load power, which is the amount dissipated in the output capacitance plus any power dissipated in other loading elements at the chip's output—resistors, for example.

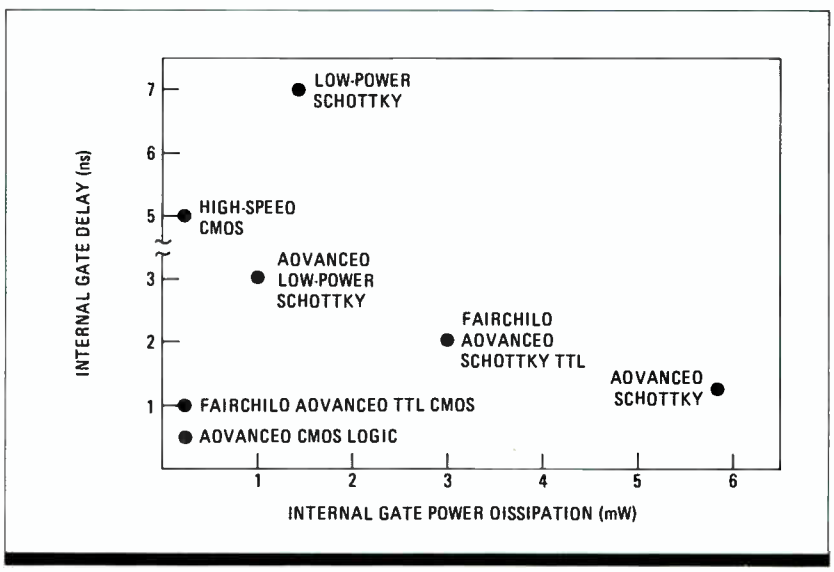
Of the three, only static power is frequency-independent. Static power is simple to calculate from data-sheet parameters of power-supply current, but in most cases it can be assumed to be on the order of a few microwatts per gate. By contrast, static dissipation is much greater in a bipolar part, typically ranging from 1 to 20 mW per gate.

Switching power depends on the power-dissipation capacitance (Cpd) of the specific device. Cpd is specified on the data sheets of ACL chips, allowing the switching power to be computed fairly easily.

This is not the case for a TTL chip. At low frequency, the switching power is swamped out by the high static dissipation of the bipolar device. At higher frequencies, it becomes a factor in overall dissipation and must be determined.

2. POWER STRUGGLE. ACL consumes more power than FAST above 30 MHz, but few logic devices are required to operate at such lofty levels.





3. BETTER THAN BIPOLAR. TI's EPIC CMOS process enables the ACL logic family to achieve less internal delay and power dissipation than even the advanced bipolar families do.

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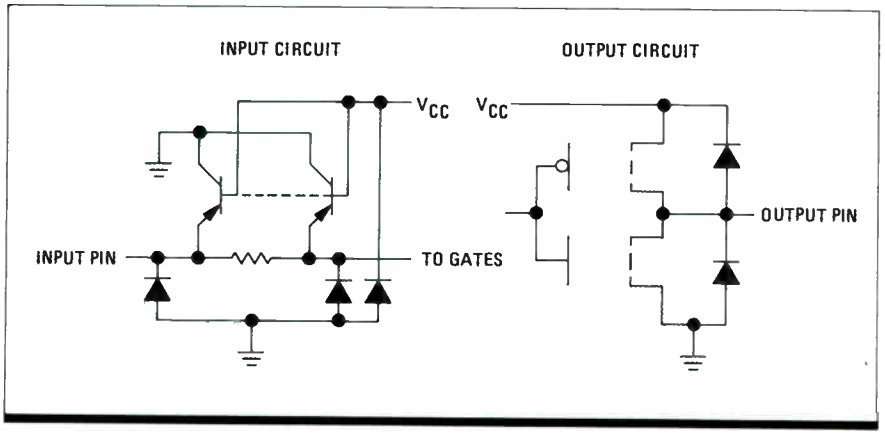

4. PROTECTION. TI's ACL family members contain protection circuitry on each of the input and output pins to withstand electrostatic discharges up to 6 kV.

But the calculation of power becomes difficult at the system level because logic elements operate at widely varying frequencies and duty cycles.

Load power is a function of the load capacitance and output voltage of an ACL part. Like switching power, it requires consideration of the various operating frequencies and duty cycles of the devices involved. In a CMOS system, the load is generally almost purely capacitive since the driven devices have negligible input currents. Such is not the case for a bipolar system because its TTL devices draw appreciable input current.

The bottom line is that an ACL system consumes far less power than an equivalent TTL system, regardless of the operating frequency. While individual ACL devices may consume more power than equivalent TTL types above certain frequencies, the distribution of switching frequencies and duty cycles gives the CMOS version the edge. This is because the vast majority of devices switch at a rate far below that of the system clock.

The best way to defeat noise is to move the Vcc and ground pins from the ends of the package and to center the Vcc pins on one side, and the ground on the other

Inherent in CMOS technology is the need to provide a greater number of internal gates per circuit function than is required of the equivalent bipolar function. Therefore, to achieve the equivalent external speed (propagation delay) of the same bipolar function, the internal gates of a CMOS device must switch at a rate three to four times faster than those of the bipolar device. TI's EPIC (enhanced performance implanted CMOS) process gives ACL gates the ability to meet or exceed the switching times of even the advanced bipolar technologies (Fig. 3).

EPIC is based on a twin-well structure that permits transistors to be packed at the densities required for 1- and 4-megabyte dynamic random-access memories. And, in fact, TI developed the process to support the company's 1-megabyte DRAMs. EPIC's 1-μm gate length holds on-chip propagation delays in the subnanosecond region.

TI has developed a proprietary process for forming the gate and source and drain regions of a CMOS transistor from silicide. This is key to the process because it reduces internal interconnection resistance. In CMOS chips, internal resistance and capacitance are the chief limiters of switching speed. To minimize the contributions of speed-robbing parasitic capacitance, sidewell oxidation is used between the gate-source and drain-source nodes.

While the speed of ACL is a boon to designers of high-performance systems, it also can create problems in performance. In the case of TI's ACL, the 2- to 4-ns rise and fall times of high-switching-speed pulse edges can adversely affect circuit operation. When multiple outputs of an ACL chip switch simultaneously, a number of problems can crop up: output glitching, loss of stored data, speed degradation, and plain old system noise.

Fast-switching bipolar devices suffer the same problems. But the amplitude of a bipolar part's voltage swing is lower—a maximum of about 3.5 V. So the noise problem is not as severe as in CMOS devices, where the rail-to-rail voltage is from 0 to 5 V.

One of the culprits in CMOS is inductance, both in the package leads and in the printed circuit's traces. Inductance produces a dV/dt effect that the output of an ACL device can propagate through the system in the form of noise. And maximum inductance in an IC package is at the ends—exactly where the V_{cc} and ground pins are located.

One way to solve the noise problem is to change the traditional placement of the V_{cc} and ground pins. Rather than placing V_{cc} and ground at the ends of the package, TI and Signetics Corp. center them on opposite sides of the package [*Electronics*, Aug. 7, 1986, p. 29]. In the new configuration, inputs surround the V_{cc} pins on one side of the package and outputs surround the ground pin on the other side. Experiments with this arrangement indicate that glitching, ringing, and bounce can be reduced significantly.

Because the centered V_{cc} and ground pins mark a departure from the traditional end-pin layout that dates back to the early days of TTL, there may be some reluctance to change (see p. 82). However, two points must be considered.

First, the present 1-μm ACL chips are just the first of a line whose ultimate geometry may well

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reach down to submicron levels. Speed increases as geometry shrinks, so today's noise problems may be insignificant compared with those of a higher-speed technology. It is therefore inevitable that some type of revised packaging for logic devices will have to be addressed in the future. TI and Signetics have chosen to address the problem now so that future generations of high-speed logic are packaged in a form to minimize system problems and maximize performance.

Second, the centered pin placement has proven effective in reducing noise levels caused by simultaneous switching. System noise immunity is improved, speed is not degraded, and the design's overall reliability is enhanced.

RELIABILITY MATTERS

But as most designers are painfully aware, any MOS transistor is subject to failure from the twin killers of latchup and electrostatic discharge. These two failure modes represent the most serious assaults on the reliability of CMOS logic.

Latchup is difficult to eliminate completely, but the current necessary to trigger it can be raised to values that are unlikely to occur in operation. TI's solution is to use guard-ring structures that shunt potential latchup currents to ground before they appear as base current in the parasitic silicon controlled rectifier. A guard ring raises the SCR's trigger point to a current level much higher than that supplied by typical signals.

In addition, TI combines a high-resistance epitaxial layer with a low-resistance p+ substrate to produce a material that resists the formation of parasitic elements. The result is that it typically takes 650 mA at worst case to cause latchup at 25°C and 500 mA at 125°C. These levels are about 100 mA greater than those of earlier versions of high-speed CMOS logic.

TI provides ESD protection by incorporating networks across the package's input and output pins. On the input side, a p+ diode and a diffused pnp transistor across a resistor clamp ESD spikes. The output pins are protected by the p+ and n+ drain diodes of the output transistors. An additional p+ diode can be connected between the power supply terminal (V_{cc}) and the output pin (Fig. 4). TI tests the ESD protection circuitry according to MIL STD 883, Method 3015. Using this method, ACL devices typically provide protection to ±6 kV. □

WHY MOORE AND HEFNER CHOSE A NEW PINOUT

When Texas Instruments shifted the responsibility for all CMOS logic engineering to its Sherman, Texas, facility, Rich Moore and Charles Hefner got the job—but neither knew it would lead to an industry controversy. Because they have extensive backgrounds in general-purpose logic products such as high-speed CMOS (HC), advanced Schottky TTL (AS), and advanced CMOS logic (ACL), they were prepared to go to a new pinout for TI's ACL family.

The new pinout was to solve the problem of switching spikes, something they had faced before. "We've known about simultaneous switching problems in high-speed logic parts for years," says Moore, new-product engineering manager for TI's HC, AS, 74F, and ACL logic products. "When we began specifying these advanced CMOS logic parts, customer input was overwhelmingly focused on this problem of parasitic package inductance in the newer families of high-speed CMOS."

Moore points out that the problems of simultaneous switching of multiple outputs in parts in these CMOS families used to occur only in isolated devices. "We have seen a migration in these components from causing an occasional system problem to the point when it exists throughout currently available ACL families," Moore says. "Rather than have a family of parts that did not meet customer needs, we decided to solve a family problem with an overall solution."

SPIKE FIGHTERS: Rich Moore (left) and Charles Hefner push new CMOS logic pinouts.

Hefner, application engineering section manager for the Advanced Schottky group in Sherman, says the pinout change has received high marks from customers. "I've been on the road talking with customers, and almost every one has confirmed our solution. After all, this isn't the kind of thing you do in a vacuum."

Currently, Moore and Hefner are working on these new center-pin ground and V_{cc} pinout designs to provide parts to the market by mid 1987. "We feel that enough customers realize the problem to make this change warranted, and once more engineers gain experience designing with high-speed logic, they'll also understand the importance of the pinout change in a system," Hefner says.

Moore has a BS in electrical engineering from Purdue University, West Lafayette, Ind., and an MS in engineering management from Southern Methodist University, Dallas. Hefner received BS degrees in both engineering physics and mathematics from Southeast Missouri State University, Cape Girardeau.

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OPINION

IT'S TIME FOR A NEW LOGIC PINOUT

JAMES F. WATSON
As vice president of U. S. marketing for Texas Instruments Inc.'s Semiconductor Group, Watson's responsibilities include the supervision and administration of marketing for the U. S. regional technology centers and U. S. marketing communications, and two logic product departments. He has held numerous positions over the course of his 26 years with the Dallas company, including division manager of digital circuits and military products.

It's tough to break tradition. But when breaking tradition provides a solution for the industry and for all future high-speed logic families, the choice becomes clear. The decision by Philips International NV, its subsidiary Signetics, and Texas Instruments to abandon the standard ground and V_{cc} end-pin configurations in the 1-μm advanced CMOS logic line was not frivolous, but based on tests, customer input, and consideration of real-world systems.

Functional tests on available ACL parts and on preliminary system designs aroused real concern at TI and Philips/Signetics that these parts could not drive other logic devices in a system without sending false information. These findings echoed customer complaints about the performance of high-speed CMOS logic in system designs.

The three companies moved to solve an industry problem that others have chosen not to address at the chip level. The companies decided that, while vendor resistance to changing the standard pinout would be great, this truly was a case where the ends justified the means.

A look at the history behind the old logic pinouts shows that they may no longer be valid in today's environment. Back when TI began designing the TTL family, printed-circuit boards were single-level, and so were logic chips. Power and ground pins were located at the ends of the package to minimize noise at the board level. This setup maximized system performance, since power lines were run to the outside of the board. In addition, designs for inputs and outputs were configured with the aim of easing fabrication, not system design.

Other than familiarity, there is no reason to retain these pinouts. Today's parts are made with double-level metal, and pc boards provide numerous levels for routing data and power. Also, smaller device geometries and double-level-metal fabrication have made chip layout independent of old design rules and thereby more easily modified.

The problems of noise encountered in the simultaneous switching of multiple outputs is found to some degree in all logic families, including Fairchild Semiconductor Corp.'s AS, ALS, and FAST series, as well as in all currently available ACL families. The phenomenon can jeopardize performance, and the end-pin ground and V_{cc} are a primary cause.

The problem lies in the unacceptable level of package inductance when high-speed CMOS logic families use such a pinout. In tests conducted in our laboratories using a variety of high-speed logic parts—both CMOS and bipolar—we found that many of the parts were running on the borderline of acceptable functionality in a system with multiple-output switching. CMOS parts especially tended to generate high voltage spikes on an octal device with seven outputs switching and one output quiescent.

Some critics of the new pinout have suggested that designers avoid switching multiple outputs at once or that they use damping resistors on the outputs to handle the voltage spikes. Others have suggested altering system timing to plan ahead for ringing on the outputs. All these "solutions" will work, but besides requiring extensive engineering, they slow the parts to HCMOS levels. And what design engineer needs an octal device if he can't use all the outputs?

Using a center-pin ground and V_{cc} design, designers can minimize simultaneous switching noise and maximize design efficiency without sacrificing the speed inherent in these new logic families. Changing the pinouts will require some board-level design changes. However, these changes can be offset by the convenience of the new flow-through architecture. At most, the new designs add only four pins to any configuration.

The bottom line in this so-called controversy is resistance to change. TI and Philips/Signetics understand that. But we think that in this case, the problems are significant enough to justify changing an industry standard. And we're betting that a lot of designers will think so, too. □

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OPINION

DON'T CHANGE LOGIC PINOUT STANDARDS

KIRK POND
The executive vice president and general manager of Fairchild Semiconductor Corp.'s Digital Unit is a veteran of Timex Corp., where he was senior vice president of consumer electronics. Prior to that, he spent 14 years with Texas Instruments Inc. as vice president and general manager of the Calculator and Educational Products Division and in various semiconductor management positions. Pond holds both an MBA and a BSEE.

With the recent introduction of alternate advanced CMOS logic (ACL) families, there may develop a misconception that the accepted pinout standards and the needs of high-performance systems are incompatible. Nonstandard package pinouts for ACL are simply not necessary to overcome such problems as noise. Fortunately, systems designers have long managed crosstalk, ground bounce, reflections, skew, and other modes of spurious noise at the board level.

Before ACL, the last successful generation of industry-standard small- and medium-scale integrated logic was introduced in 1979. Fairchild advanced Schottky TTL (FAST) quickly was accepted as the standard replacement for Schottky TTL and Advanced Schottky in mainframes and minicomputers. The reasons: its speed, ease of use, reliability, and pin-compatibility.

Systems designers also quickly understood that outside of ECL implementations, the FAST family pushed system clock rates to the limits of conventional TTL board design. With its high speed and high drive capability, it gave rise to transmission-line termination techniques and system-timing expertise.

However, new system needs emerged as FAST migrated downward in the systems hierarchy to popular desktop machines. Existing low-power Schottky and advanced low-power Schottky families consumed too much power, while the newer high-speed CMOS (HC) family lacked speed and drive. Emerging to meet those needs was Fairchild advanced CMOS technology, or FACT. This first ACL family brought an opportunity to reduce the cost of equivalent LS and ALS functions and to usher in a new generation of portable equipment.

Systems designers, having been exposed to performance enhancements made feasible by FAST logic, are now using high-performance design techniques in systems based on FACT logic. Today there are about 1,000 FACT customers using these techniques and experiencing reliable operation at this enhanced price/performance level. This broad level of acceptance could only have been established by adhering to traditional pinout standards and complementing this steadfastness with technical information regarding the design of high-performance systems.

Demands for better performance are driving system design in new directions. For example, putting traditional standard logic families into small-outline integrated-circuit packages permits closer physical spacing, reduced backplane noise, and reduced pin inductance, creating the potential for tighter system timing. With them, systems makers are experiencing concomitant lower manufacturing costs. With over 85 members of the FAST and FACT families available in SOICs, this is a clear opportunity for higher speed at lower densities.

Beyond standard CMOS logic, CMOS gate arrays, standard cells, and emitter-coupled logic will all follow the designers' demand for higher system performance. Hence, semiconductor vendors are committing valuable resources to developing the right process technologies and support tools. Included are such tools as system-level simulators, automatic test-vector generators, and computer-aided-engineering packages. These will help systems designers develop innovative architectures based on the unfolding generations of VLSI circuitry.

Packaging technology, too, needs a boost in the high-pin-count high-density areas where the next generation is heading. These are the necessary targets of innovation.

Yes, standards are important. Because we have been dealing with fast edge rates in both FAST and ECL for a long time, we understand the tradeoffs customers want, and we have met their needs in terms of proper speed and ease of use. We believe CMOS systems will migrate toward custom very large-scale ICs, rather than to new nonstandard logic families. □

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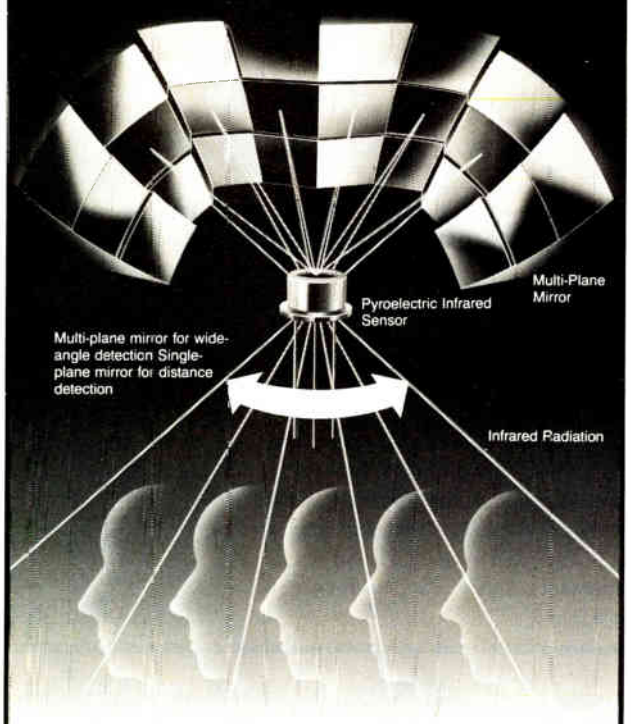

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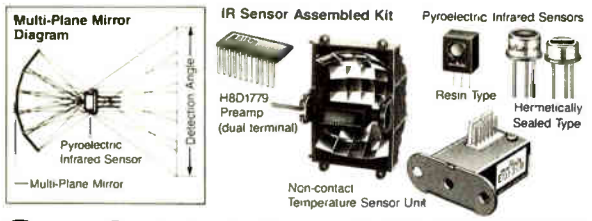

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PARALLEL PROCESSING: THE PACE QUICKENS

Work is accelerating on the two big remaining obstacles: the lack of good benchmarks and the need for software that uses parallelism efficiently

by Tom Manuel

Parallel processing is trying hard to move into the mainstream. The number of parallel computer products now on the market is climbing, and more are expected shortly. Work is accelerating on the remaining problems that stand in the way of widespread implementation of parallel processing. Two of the biggest are the lack of good benchmark programs based on real jobs and job mixes and the need for application software that uses the multiple processors efficiently.

Parallel processors are such a radical departure in computing architectures that they don't fit into any of the conventional classifications of computers; new ones have had to be devised. One classification used frequently distinguishes on the basis of tightly coupled or loosely coupled architectures. Tightly coupled processors have their operation tied closely together through the sharing of one main memory and often one copy of the operating system. Loosely coupled processors each have their own main memory and may have their own input/output peripherals as well. These processors usually run their own copies of the operating system.

But not all parallel computers fall neatly into these two classes. Some have both local and shared memory, and the interconnection schemes among processors and memories vary greatly, as do the control schemes. And breaking down the architectures into the way individual processors are connected—through a bus, a hypercube, or a switching network—would also show tremendous differences in price and performance.

A more useful way to classify architectures is

COMMERCIAL PARALLEL-PROCESSING COMPUTERS BY ARCHITECTURE

System starting price	Bus-connected, shared memory, few big processors	Bus-connected, shared memory, moderate to large number of medium-sized processors	Hypercube interconnection, local memory, moderate number to many processors	Networked computers and work stations, local memory, small to potentially very large numbers of computers	Others: such as, data-flow, switched-connected processors and transputer-based machines
$10,000 to $100,000	Concurrent Computer	Masscomp 5700 5800 Sequent Balance 8000 Balance 21000	Ametek System 14	Apollo DW Series Sun SUN-3 Series	BBN Butterfly Loral Data Flo LDF-100
$100,000 to $1 million	Alliant FX/B Culler Culler 7 Digital Equipment VAX 8300 VAX 8800 VAX Clusters Elxsi 6400	Encore Multimax Flexible Flex-32 Teradata DBC/10/2	Intel Scientific Computers iPSC iPSC-VX Ncube Ncube/ten	Digital Equipment Networked VAXes and MicroVAXes	Floating-Point Systems T Series Meiko Computing Surface Multiflow (Unamed)
$1 million to $10 million	Cray Research XMP Cray-2 Cray-3 Control Data Cyber Plus IBM 3090 Model 400	None available now	None available now	None available now	Thinking Machines The Connection Machine Myrias Research (Unamed)

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offered by Justin R. Rattner, program manager at Intel Corp.'s Scientific Computers group in Beaverton, Ore. It is a two-dimensional matrix with the basic architectural styles on one axis and system price ranges on the other. For the table, opposite, based on this matrix, *Electronics* selected three price ranges and four architectural styles.

The three price ranges—$10,000 to $100,000, $100,000 to $1 million, and $1 million to $10 million—represent approximate starting prices for small configurations. All the computers shown can be incrementally expanded to very large systems.

The first class of architectures includes systems in which a few (2, 4, 8, 12, or so) powerful processors share a single large memory and link through a bus or a hierarchy of buses. The second class differs only in the type and number of processors: a moderate number—ten to hundreds and possibly a few thousand—of medium-sized processors.

Class three designs can range from a moderate number of small to medium processors to a great many—tens of thousands—of these processors. Each processor has local memory and connects to others through a hypercube network. The hypercube is an interconnection scheme using an n-dimensional cube where n represents the number of directly connected computers (called nodes) that establish the cube's dimension. A 32-node cube, for example, is a 5-d system with each node connected to its five nearest neighbors. A 6-d cube holds 64 nodes, a 7-d cube 128.

NOT FOR PURISTS

A fourth class describes systems that some purists would say are not parallel. Included are systems in which the same, similar, or completely different computer types are loosely coupled through communications networks—local-area, wide-area, or combinations. The systems range from relatively few to very many processors, each having its own memory and operating system. But in being able to share a file system or pass messages to others, they can work concurrently on the same problem.

For example, Digital Equipment Corp.'s dual-processor VAX 8800s and 8300s can coexist in clusters that are linked by LANs. These, in turn, are interconnected through wide-area networks. This represents four types of multiprocessing, says Robert Burley, engineering product manager for advanced VAX computer development: over wide-area networks, over LANS, within the computer room (VAX clusters), and within tightly coupled central processing units. DEC has such a setup for internal use.

The world's biggest computer company hasn't developed any parallel machines for sale other than its biggest mainframe, the 3090 Model 400, which has a pair of dyadic CPUs, but it is exploring the technology. IBM Corp. is convinced that parallel processing is strategically important to itself and the computer industry, says Tilak Agerwala, director of symbolic and numeric processing at the Thomas J. Watson Research Laboratory in Yorktown Heights, N. Y. "At the very highest level, there are two generic categories: specialized processors and multipurpose machines," Agerwala says. IBM Research has built one specialized machine, the Yorktown Simulation Engine, and is working on another. This machine simulates new circuits for high-end computers, and is in daily use, says Agerwala.

IBM also is building the RP3, for research parallel-processing prototype. With this computer, researchers will attempt to sort out the incredibly complicated taxonomies for parallel-processing architectures and tackle the many problems in programming and benchmarking parallel computers.

The RP3 (Fig. 1) will use the same basic reduced-instruction-set microprocessor that powers IBM's RT Personal Computer. However, this highly parallel, multiple-instruction, multiple-data research machine will necessarily implement a

MICROPARALLELISM. The T Series computer from Floating Point Systems uses Inmos's Transputer microprocessor.

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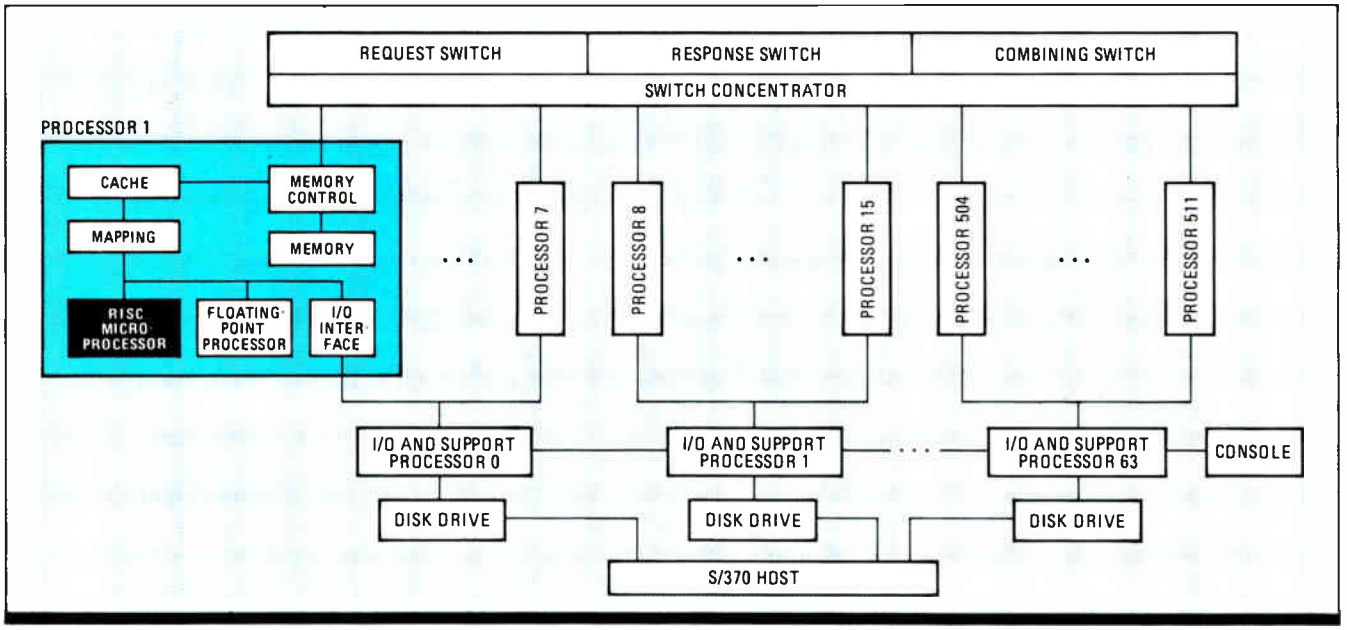

1. AT THE LABS. IBM Corp.'s Thomas J. Watson Research Laboratory is building the RP3 flexible-architecture parallel processor with 512 RISC microprocessors. It will be used for experiments and study projects, including benchmarking.

quite different approach to memory management. It will also employ a very powerful, flexible, and intelligent switch to handle interprocessor control and memory access [*Electronics*, Aug. 26, 1985, p. 16]. The RP3 really has two networks: the low-latency, high-bandwidth, self-routing Omega for interprocessor connection, and a net to combine the messages from several processors for information from the same memory module.

The novel memory-mapping mechanism developed for the RP3 allows any combination of global and local memory and lets users vary the mix at run time. The switch allows variable configurations of processors.

The first RP3, which IBM expects to have operational late next year, will have 64 processors. It will ultimately have 512 processors and will perform 1 billion instructions/s, says Agerwala.

THE CLASSLESS KIND

Other parallel-computer designs fall outside the first four classes of architecture. These include data-flow computers and machines built using Inmos Corp.'s transputer, such as the T Series of supercomputers from Floating Point Systems Inc., Beaverton, Ore., shown in the photograph on p. 87. Others include the Computing Surface from Meiko, Bristol, England; the wide-word-instruction machine from Multiflow Computer Inc., Branford, Conn.; and the Connection Machine from Thinking Machines Inc., Cambridge, Mass. [*Electronics*, June 23, 1986, p. 45].

Also in this category is the Myrias Parallel Computing System, a design using thousands of microprocessors that is now under development by Myrias Research Corp., Edmonton, Alberta, Canada. The Myrias computer is being designed as an infinitely scalable machine that is also programmable in languages minimally different from current standard languages such as Fortran and C. One goal is to execute all iterations of program loops at once simply by inserting a parallel-loop command in appropriate places in both existing and new programs.

Another member of the miscellaneous category is BB&N Advanced Computers Inc.'s Butterfly, for which the Cambridge, Mass., company claims the largest installed base of any parallel computer. The Butterfly has up to 256 MC68020 processors, each with its own memory and connected by the patented Butterfly switch (Fig. 2). Although the memory is physically attached to the individual processors, it is used as a shared memory pool, tightly coupling the processors. As the number of processors grows, so does the size of the shared memory.

Sorting out and classifying parallel-computer architectures is only half the battle. The other half is evaluating their suitability for a specific job mix. The best way to do that is to assemble a set of representative benchmarks.

Once a benchmark set is assembled, it should be run on a system configured with the minimum number of processors and then run again on at least one other configuration with the largest number of processors available. This will measure the linearity of performance increase as the system grows, as well as the overall system throughput on an anticipated job mix.

Sequent Computer Inc. has worked out a series of benchmark programs for measuring throughput of multiuser, multiprocessor systems. "The best way we could think of to do an honest job [of benchmarking] was to figure out an average load; in other words, what Sequent

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users are doing," says president Casey Powell. The Beaverton, Ore., company compiled jobs from its customers to create a typical load. Then, with that job load running, the evaluators run several benchmarks on Sequent machines with two processors and on up. They also run the same combination of load and benchmarks on other makes of machines.

Help is available for the prospective customer who cannot assemble a set of benchmarks and run it on a variety of parallel-computing systems. Several groups, including parallel-computer vendors, are developing sets of standard benchmarks [*Electronics*, April 7, 1986, p. 16].

A few researchers, such as Jack D. Dongarra, scientific director of the Advanced Computer Research Facility at Argonne National Laboratory, Argonne, Ill., run their benchmarks on a wide variety of computers and publish the results. Dongarra's Linpak floating-point calculation codes are a package of about 400 Fortran subroutines. They measure performance for only a particular class of problems and were not developed with parallel processing in mind.

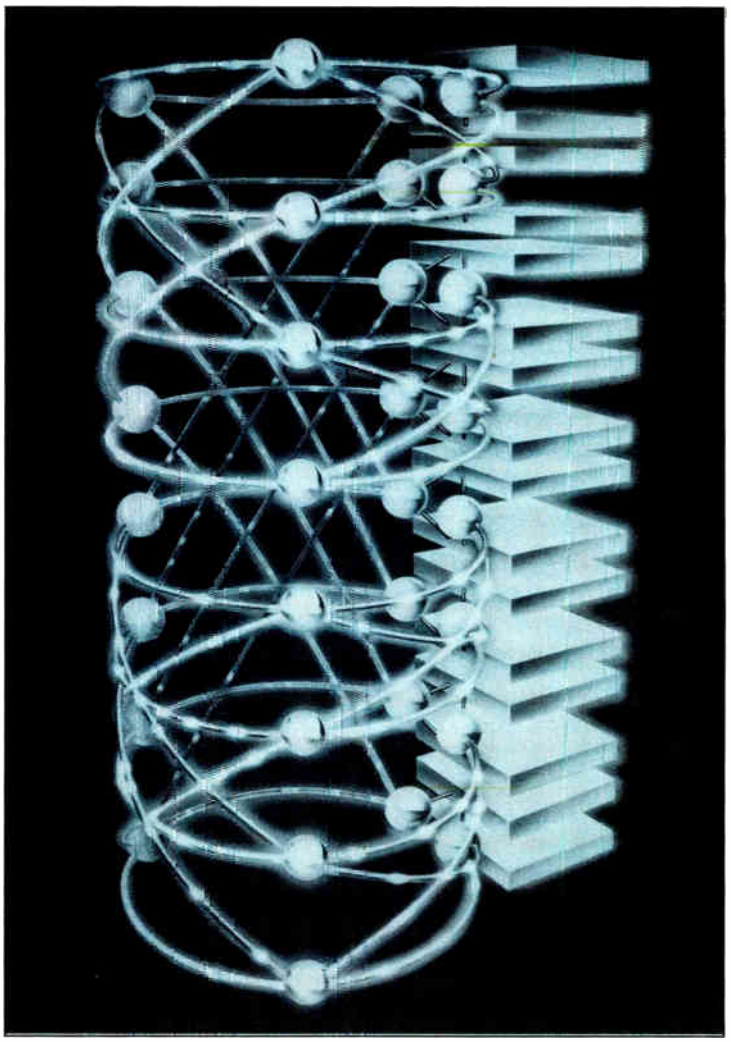
The National Bureau of Standards is also working on parallel-computing benchmarks. It has collected 12 sets of benchmarks in Fortran and C and is distributing them through Arpanet. Use of these is picking up—there have been about 290 transactions, according to an NBS spokesman, who cautions that delivery of one benchmark sometimes takes several transactions.

AIMING FOR THE HEART

The biggest challenge in parallel computing is in the software: finding and exploiting parallelism in a given job. Several attempts are under way to automate the discovery of parallelism and the creation of code to exploit it.

At Multiflow Computer, for example, executive vice president Joseph A. Fisher and his team are working on hardware and software that will automatically find and use parallelism in all parts of an application. Current attempts to parallelize code focus on what Fisher calls the program's mathematical heart. The rest of the code, some 80% to 90% in scientific and engineering applications, does not benefit from the parallelization efforts, he says. Multiflow's design aims to take care of this junk code, as it is sometimes called, by using a machine with a very wide instruction word and a very smart compiler that will understand how a given program works. The compiler will pick operations that can be done together and assemble one big instruction comprising many small operations such as loads, stores, multiplies, address fetches, and tests.

The parallelism in such an architecture is extremely fine-grained. The Multiflow machine will not be a true multiprocessor with many complete processors. Instead, it will have plenty of computational elements that the smart compiler can select to use in each big instruction.



2. BUTTERFLY. The BB&N Advanced Computers Inc. Butterfly computer uses a proprietary packet-switched network (left) to efficiently interconnect many processors (right).

In looking ahead in the program to find little operations to pack into each big instruction, the smart compiler runs into one barrier. When programs or human programmers, looking for parallelism, run into a conditional jump, they must either stop looking or guess where the program will jump next. Fisher claims his development team has broken the barrier with trace scheduling. This scheme gambles on a way to go when it encounters a conditional jump and intelligently recovers if it makes the wrong choice.

At DEC, Burley reports some significant results from manual decomposition of programs. If a programmer or software engineer looks closely at a program to find where parts of it can be run in parallel and figures out how to reorganize it accordingly, worthwhile speedups are often achieved. For example, one engineer took the popular circuit-simulation program Spice and got a 70% performance improvement on a dual-processor VAX 8800 by rewriting only about 10% of the 18,000 lines of code. □

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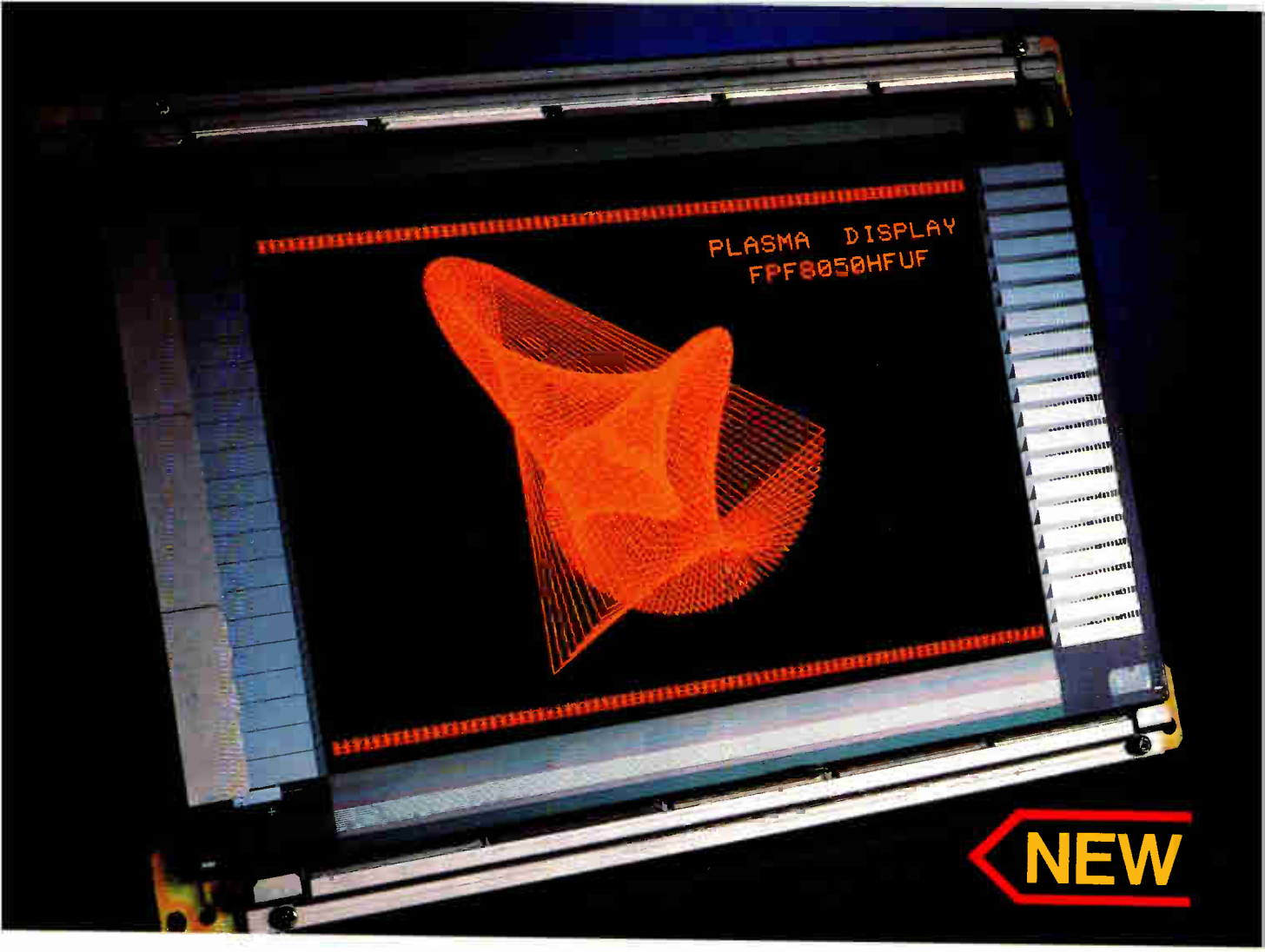

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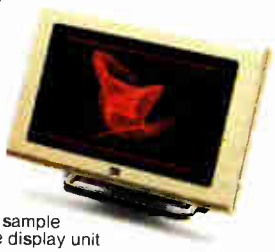

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- 640 x 400 dot matrix high-resolution display
- Easy-to-use CRT-compatible interface
- Multi-drive LSI that makes the unit compact, thin, and lets it consume little power
- Highly reliable AC memory panel

Specifications

Model	FPF 8050 HFUF
Display resolution	640 x 400 dot matrix (256,000 dots)
Effective display size	210.87 mm (W) x 131.67 mm (H)
Dot spacing	3 dots/mm (dot pitch: 0.33 mm)
Brightness	150 cd/m^2
Contrast ratio	20 : 1
Display color	Neon orange
Field of view	120° min.
Exterior dimensions	300 mm (W) x 200 mm (H) x 35 mm (D)
Weight	Approx. 1.7 kg

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PROBING THE NEWS

WHOSE OPERATING SYSTEM WILL RUN THE 386-BASED PCs?

MICROSOFT'S NEW MS-DOS IS LATE, AND IBM MAY GO ITS OWN WAY

by Alexander Wolfe

NEW YORK

The biggest guessing game in the personal computer world today is what kind of operating system IBM Corp. and Microsoft Corp. will come up with to run machines based on Intel Corp.'s powerful 32-bit microprocessor, the 80386. The industry is buzzing with reports that Microsoft is running late in announcing its new version of the current Personal Computer standard, MS-DOS, and IBM is thought to be working on its own proprietary operating system in a strong bid to fend off clone makers that have increasingly been cutting into its PC business.

The speculation grew more intense last week as the first microcomputer from a major manufacturer to use the 80386 chip, Compaq Computer Corp.'s Deskpro 386, was announced (see p. 66). The leader in a parade of 20 to 30 more 80386-based machines expected before the end of the year, the Compaq machine has a control program written by Microsoft.

At the same time, Microsoft dispelled some of the uncertainity, offering a hint about the future of MS-DOS. Joining Compaq's big bash for the new Deskpro at New York's trendy Palladium nightclub, Microsoft chairman William H. Gates III said, "Future DOSes are being developed that will take full advantage of the 386."

Meanwhile, the Redmond, Wash., company announced the first of its commercially available 386 operating systems: the Unix-like Xenix System V/386. Microsoft and Compaq have already developed a DOS-based system for the Deskpro 386 together, but it is available only with the new machine.

THE SCRAMBLE BEGINS. Dozens of lesser-known companies are also scrambling to get on the 80386 bandwagon. Among the companies said to have operating-system software in the works are Interactive Systems, Locus Computing, Phoenix Technologies, Pick Systems, Softguard Systems, and Software Link. Their hopes rest on beating Microsoft to market, as well as offering specialized operating-system capabilities geared to applications for niche markets.

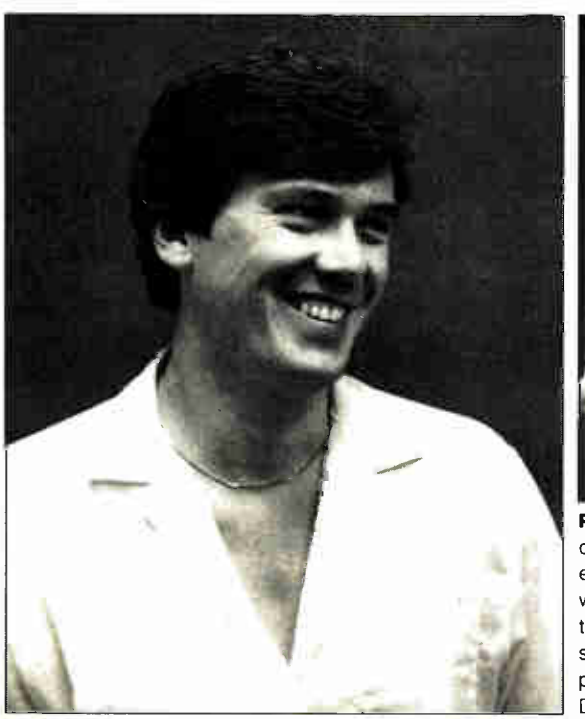
Industry insiders say that Microsoft's MS-DOS strategy for the 80386 will emerge in a three-step progression. First is the system offered with the Deskpro 386, which combines the existing 3.1 version of MS-DOS with the Lotus/Intel/Microsoft Extended Memory Specification code, or LIM/EMS. LIM/EMS breaks the 640-K barrier of standard personal computers, allowing machines to take advantage of the larger addressing capacity of a 32-bit chip. Besides staking a claim as the first 32-bit operating system, the Deskpro 386's control program is the first to implement multitasking features.

Next, in December or early next year, analysts say, will come the long-awaited MS-DOS 5.0. That system, built to support Intel's older 80286 chip, will also handle the 80386, treating it essentially as a fast version of the 80286. MS-DOS 5.0 will be the first of the Microsoft lineup to implement full multitasking.

Finally, beyond MS-DOS 5.0, Microsoft is believed to be working on a successor designed expressly around the 80386 chip. Sometimes called MS-DOS 6.0, its true numerical designation is unknown. Industry watchers expect it to be available late in 1987 or early in 1988.

PUSHED. But which DOS? Though Microsoft will not officially verify its existence, MS-DOS 5.0 has been expected for some time, and Adrian King, director of operating systems and systems software, admits the company is feeling growing pressure to release it. Surprisingly, end users are not the ones pushing hardest for the new system. "The pressure we get is from software developers, who in the last year have hit the limits of the 8086 in terms of the performance, in terms of the 640-K address space, in the protection aspects," says King.

To push past those limits, King believes, software developers will look next to the 80286, not the new 80386.



PRESSURE. Microsoft president Gates, above, acknowledges that the company is working on 386 operating systems. And executive King, left, says the company is feeling pressure to release its MS-DOS 5.0 package.

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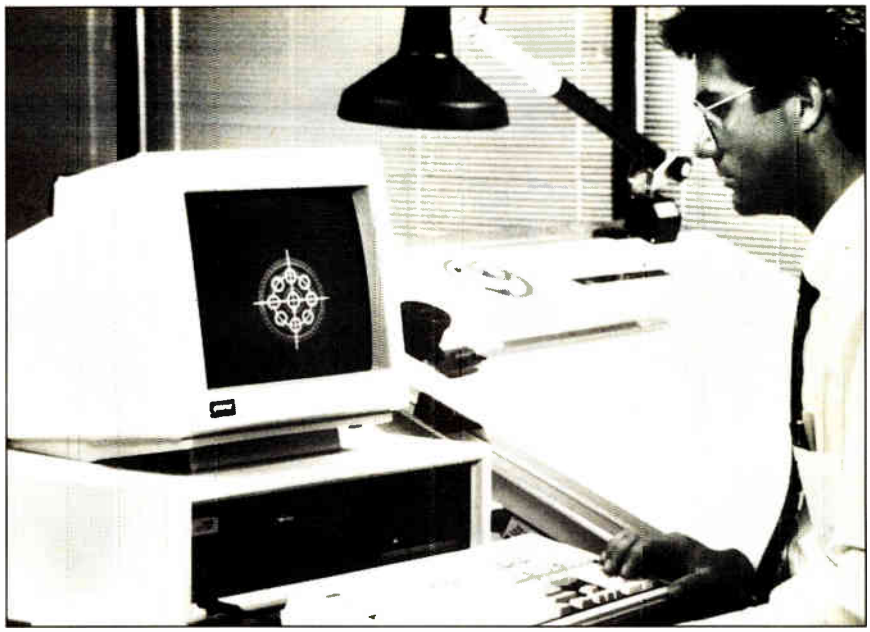
"One of the misconceptions that people have is that the 286 is suddenly going to wither and die as a result of the fact that the 386 is now in production," he says. "The 286-based [personal computer] is going to be the standard for at least two more years, and probably longer, before the 386 begins to assert itself in the marketplace in terms of the number of machines that are actually sold." (See p. 33.)

MS-DOS 5.0 will run on 80386 machines, but it is strategically aimed at those 80286-based computers. "We intend to evolve [MS-DOS] in line with the way the market is working. That means that full support of the 286 is very important now, and 386 will become so later," says King. In software terms, the popularity of the 286 today will speed that transition to the 386, King argues.

The reason is the similarity between them, combined with the incompatibility between the 8086 chip and the 80286 operating in its protect mode. Programs designed for the 8086 will not run in the 80286. Software developers will therefore have to begin rewriting their applications programs to take full advantage of the 286's power.

But the next step up—from the 80286 to the 80386—will be easy. Anything that runs on protected mode on the 286 can also run unmodified on a 386. That is why Microsoft says it's in no rush to release a package specifically designed around the 386.

Meanwhile, The Software Link Inc. is attempting to beat MS-DOS 5.0 to the punch. The Atlanta, Ga., company is developing an MS-DOS-like multiuser, multitasking operating system for the 80386, dubbed PC-MOS/386. Gary Robertson, director of sales and marketing, says the package was created on an 80286-based machine and is currently being converted on an 80386-based computer. Shipments are expected to begin by February, he says.



RACE BEGINNING. Software writers are lining up in the competition to beat Microsoft to market with an operating system for computers built around Intel's new 80386 microprocessor.

Will IBM trade compatibility for enhancements?

IBM, for its part, may not depend on evolution. Instead, some industry insiders believe Big Blue will create its own proprietary 80386-based machine, in a move perhaps inspired by the steadily increasing price competition from the PC-clone makers. IBM would simply remove itself from the cut-rate market and concentrate on adding value for a price.

"IBM has said that the compatible makers will have to step lively to keep up with them—I think that points to some sort of closing off of the architecture," says Tom Roberts, an analyst with International Data Corp. in Framingham, Mass.

Such a proprietary architecture might include hardware to facilitate networking and multitasking. As an operating system, AT&T's Unix or a proprietary large-systems program modeled after IBM's Virtual Machine operating system, or both, may be included.

The rationale, says Roberts, is that the added features would "give large corporations a reason to buy your box—they're worried about connectivity to larger systems and communications with larger systems." Such a strategy is akin to what Digital Equipment Corp. has done with its new VAXmate [*Electronics*, Sept. 4, 1986, p. 25], a PC-compatible desktop machine that incorporates a controller for networking.

At least one highly placed industry observer agrees that IBM will end up going to a proprietary operating-system. "It's really what they have to do," says the source. "They want to own the *Fortune* 500 market for computing at all levels, and that includes personal computers. The clone makers will head toward 80286 compatibility in their 80386 operating systems, but IBM is likely to build a 386 desktop work station for the corporate world that looks more like a mainframe."

"The real win with the 80386 is to take advantage of the large physical memory, virtual-machine, and demand-paging features. An 80386 PC with a proprietary IBM operating system for the business world would be more successful than Unix on a PC," he adds.

But another respected source says that IBM's die has not yet been cast, and he argues against a proprietary route. "The debate hasn't ended inside IBM. But if they take the proprietary route, [I believe] it's a big mistake." Customers do not want compatibility to diminish, even for the sake of enhanced features, this source believes.

A debate is also taking place between proponents of MS-DOS and those who favor Unix-like operating systems for 80386-based machines. For business users, Unix may be the best choice.

"We know from looking at people who use Xenix that primarily what they're after is simple, terminal-oriented applications that interface primarily with a data base," says King of Microsoft. "That is very different from what MS-DOS services, which is a desktop environment with a mouse, probably with a bit-mapped screen, with applications that drive those devices."

As a result, according to one industry insider, "It is my opinion that Microsoft will push Xenix/386 as being a better solution [than MS-DOS] for 386-based machines in the future." Microsoft has announced that its Xenix System V/386 will ship in January.

Many software manufacturers are developing programs called "hypervisors" that will allow Unix and MS-DOS to reside simultaneously on an 80386-based machine. One type runs DOS as an application under the top-level control of Unix. Simultaneity is possible because of the 80386's virtual-machine feature; with the right control software, it can act like several 8086 machines running within the same chip at the same time.

Among such programs is one being developed by Phoenix Technologies Inc. of Norwood, Mass. According to analyst Roberts, the Phoenix hypervisor is "targeted at the work-station market—peo-

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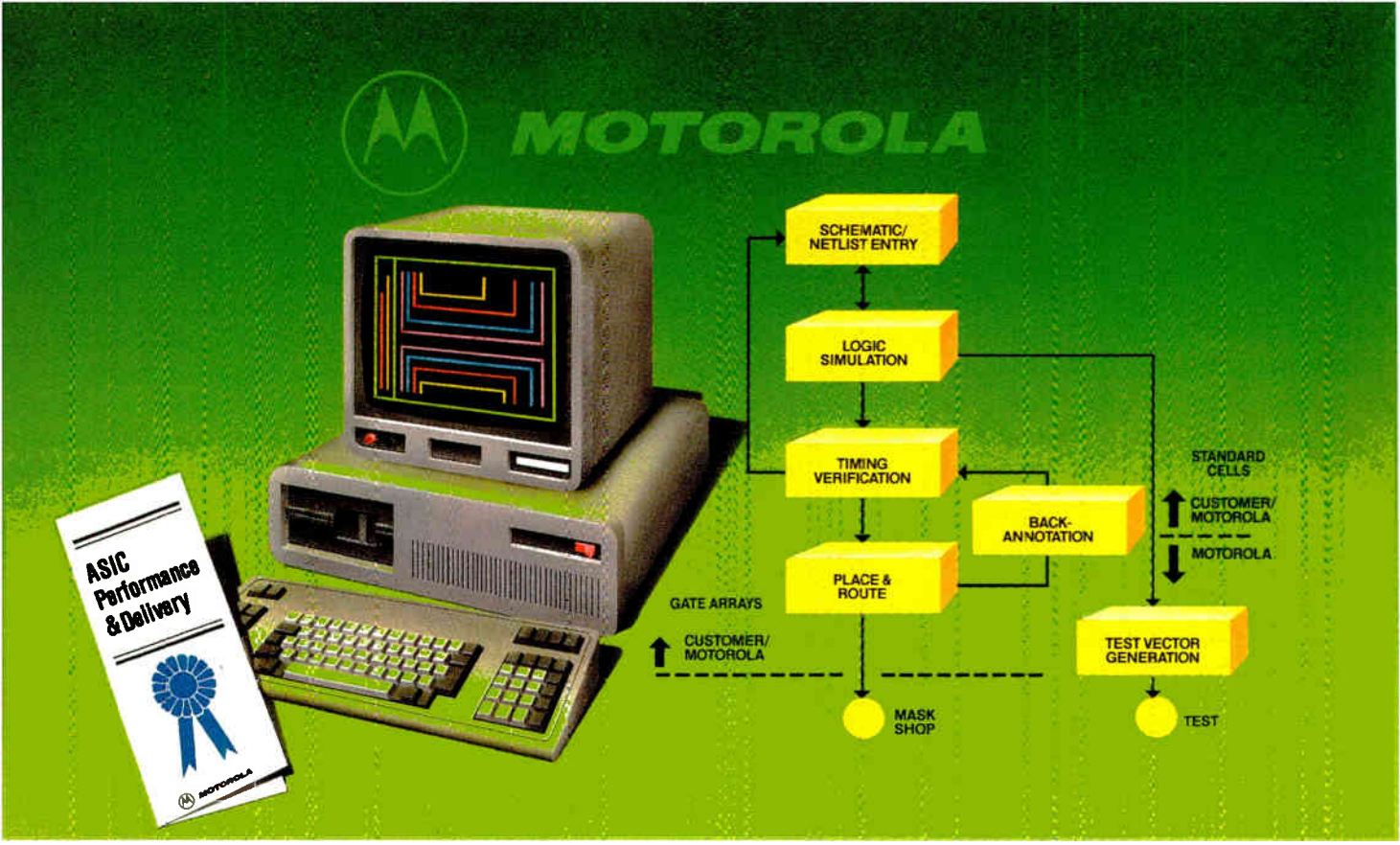

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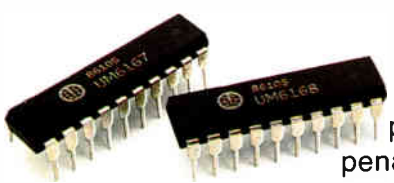

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ple who are primarily going to use Unix and then want to use some DOS applications every once in a while." Phoenix is developing the system with Interactive Systems Corp. of Santa Monica, Calif.

Another hypervisor—this one under development at Softguard Systems Inc. of Santa Clara, Calif.—will function as a multitasking controller, allowing several DOS applications, or several DOS applications and Unix, to run side by side. And Locus Computing Corp. of Santa Monica, Calif., is working on an 80386 version of its Multisystem Merge, a DOS monitor that allows Unix and DOS to run simultaneously.

Many of these software developers are rushing to get the jump on Microsoft's Xenix, and Microsoft acknowledges that some of them may ship before it does. But, says Microsoft's King, "in terms of the overall quality of the product—they're not going to beat us."

The operating system from Pick Systems Inc. falls into neither the DOS nor the Unix camps. Aimed at business users, it will generate some $1.3 billion in sales in 1986, says Dick Pick, head of the Irvine, Calif., company, which has just readied its operating system for the

Other developers may beat Microsoft's Xenix to the market

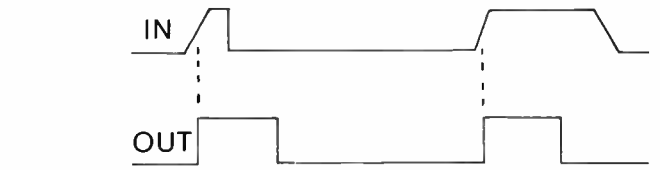
80386. "The day you can buy a Compaq [Deskpro 386], you can buy a version of the Pick operating system that will run on it," he says.

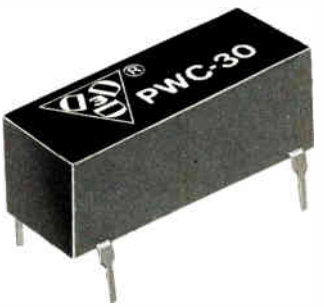
Pick claims his system will be better geared to the 80386 than Microsoft's. "MS-DOS is written in 286 assembly language, and [Microsoft has] probably taken a lot of advantages of the 286 operating system," says Pick. His company's system, he says, "is written in a pseudo-language or a universal assembly language. That's how we've achieved our portability—we've written the entire [Pick operating] system in this assembly language for almost a hypothetical or a generalized computer.

"Then, on the various [target] machines, we set up tables that define the characteristics of the machines, and we just reassemble the system and generate object code for the target machine." So rewriting the Pick operating system for new target machines was easy, Pick says: "The 386 for us is a slam-dunk."

This initial 386 version does not make full use of the 386's 32-bit data bus. But, vows Pick, "Once we get a machine in here for a week, then we'll be taking full advantage of the 386." □

Additional reporting by Clifford Barney and J. Robert Lineback.





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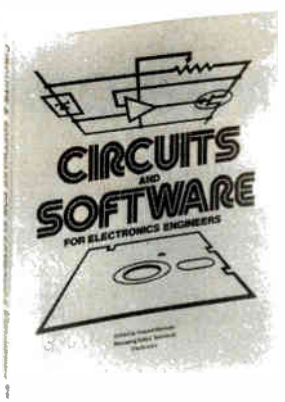

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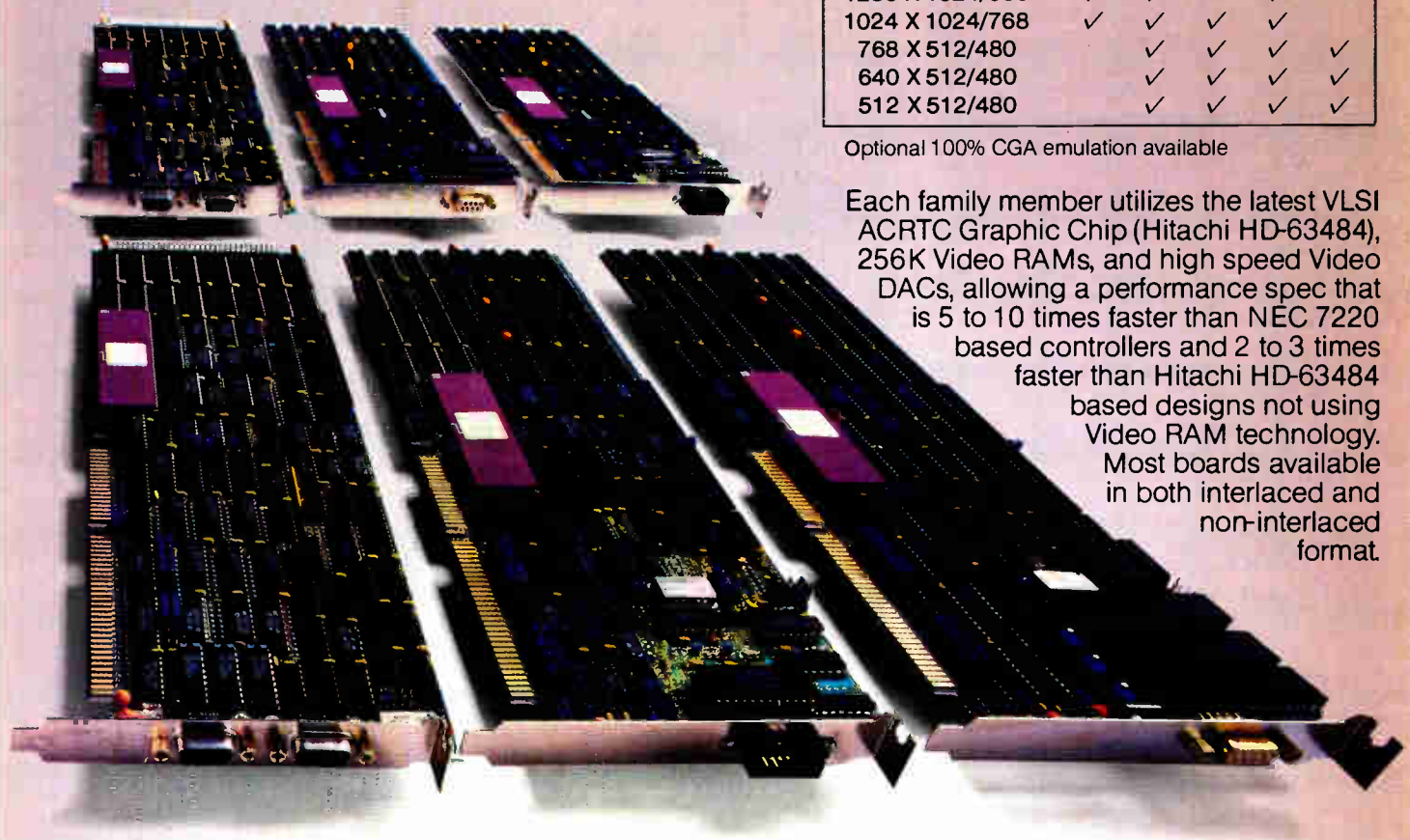

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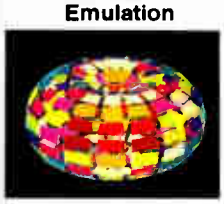

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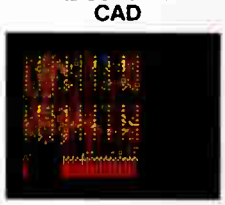

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NEW PRODUCTS

INDUSTRY-STANDARD ADC NOW COMES IN A MONOLITHIC VERSION

HONEYWELL USES BIPOLAR-ENHANCED CMOS TO KEEP POWER LOW

by Bernard Conrad Cole

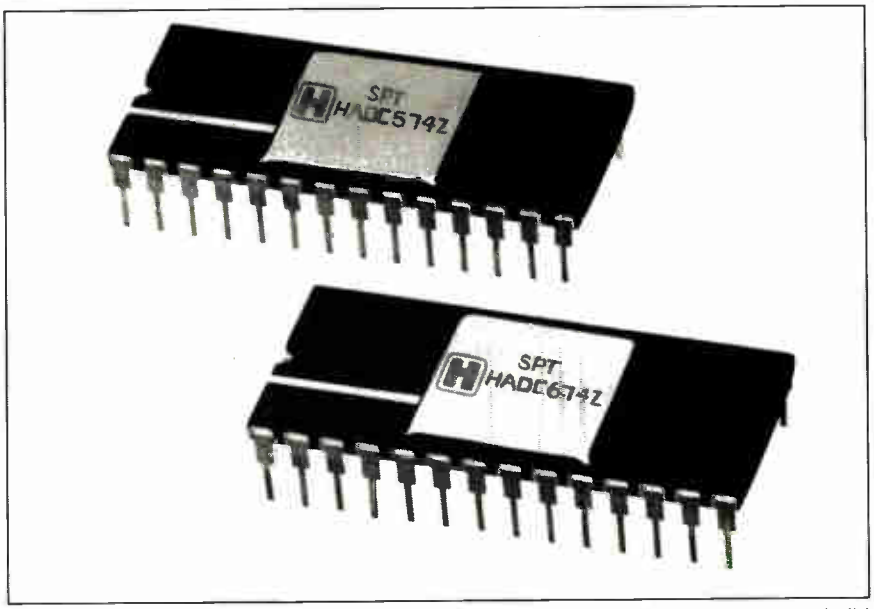
To mark its entry into the mixed bipolar/CMOS arena, Honeywell Inc. has introduced a pair of higher-speed, lower-power, functionally enhanced, single-chip versions of the industry-standard 574A/674A 12-bit analog to digital converters.

Designed and manufactured by Honeywell's Signal Processing Technologies Center in Colorado Springs, the HADC574Z and HADC674Z are the first monolithic versions of the industry-standard devices. Compatible both in pinout and function with the industry standards, they incorporate a 12-bit ADC with a reference and a clock. They also offer a variety of features not available on similar standard devices, including a sample-and-hold circuit and an on-chip three-state buffer. The buffer simplifies the interfacing of the ADC to 8-bit, 12-bit, and 16-bit microprocessor-based systems.

Power dissipation is 150 mW, which Honeywell maintains is five times better than that of comparable devices now on the market. The credit for reaching that level belongs to Honeywell's Bipolar Enhanced CMOS (BEMOS) process, which combines CMOS logic and fast bipolar npn transistors to yield high-performance digital and analog functions on the same die.

CUTS GROUND NOISE. Besides decreasing power consumption, the company says, the combination of monolithic construction and BEMOS processing also reduces ground noise and minimizes parasitics. In addition, a thin-film option on this process gives Honeywell the opportunity to actively adjust converter and comparator offset, linearity, and gain errors.

Conversion time on 10-V or 20-V input signals is 25 microseconds maximum and 15 μs minimum for the HADC574Z on a 12-bit cycle. On an 8-bit cycle, maximum conversion time is 17 μs and minimum is 10 μs. For the HADC674Z, maximum conversion times are 15 μs on a 12-bit cycle and 10 μs on an 8-bit cycle. Minimum conversion times are 9 μs and 6 μs, respectively.



DOUBLE-TEAMED. Honeywell employed its Bipolar Enhanced CMOS technology to build monolithic versions of the industry-standard 574A/674A analog-digital converters.

Both devices feature standard bipolar and unipolar input ranges of 10 and 20 V. These ranges are controlled by a bipolar offset pin and are laser-trimmed for specified linearity, gain, and offset accuracy.

Operational over the full bipolar input range, the two converters run with supply voltages of +5V, +12V, and +15V. There is an internally generated negative supply, so an external negative supply is not required.

Other key specifications of the devices include a linearity error of ±1/2 least significant bit (LSB), a unipolar offset of ±2 LSB, a bipolar offset of ±4 LSB, and a calibration error of 0.3% of full scale.

Offered in 28-pin dual-in-line packages with industry-standard pinouts, the two converters are being offered in commercial plastic, industrial ceramic, and military side-brazed packages.

The plastic-packaged versions are available now in sample quantities; the HADC574Z is priced at $26.90 apiece and the HADC674Z at $36.40, in 100-unit quantities. Production quantities are scheduled for the first quarter of 1987. At that time, samples of the industrial and military versions will also be available, for which Honeywell has not yet set prices.

Marketing Communications Department, Signal Processing Technologies, Honeywell Inc., 1150 E. Cheyenne Mountain Blvd., Colorado Springs, Colo., 80906 Phone (303) 577-1000 [Circle 364]

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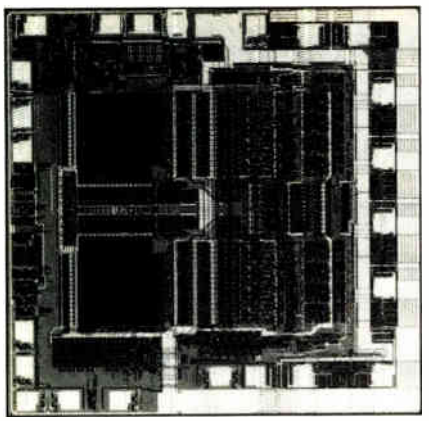


ny's GAL 16V8. the new chip has four extra pins that allow reprogramming and diagnostics to be performed remotely. It has a maximum access time of 25 ns, and maximum power consumption is rated at 90 mA. Available in sample quantities in October, the chips come in either 24-pin plastic DIPs or 28-pin plastic-leaded chip carriers. Production quantities, available in early 1987, will cost $20.95 each in 100-piece quantities.
Lattice Semiconductor Corp., 15400 N. W. Greenbrier Pkwy., Beaverton, Ore. 97006. Phone (503) 629-2131 [Circle 365]

HYBRID DAC HAS 32-COLOR TABLE

An advanced hybrid digital-to-analog converter boasts both a 32-color lookup-table memory and a complete 4-bit 3-color composite video subsystem—in a single 24-pin DIP. Accepting data rates up to 20 MHz, the AH8304 video DAC can generate RS170, RS330, or RS343 composite video signals for direct connection to a color monitor. Typical power dissipation is 1.5 W, and the maximum is 2 W.

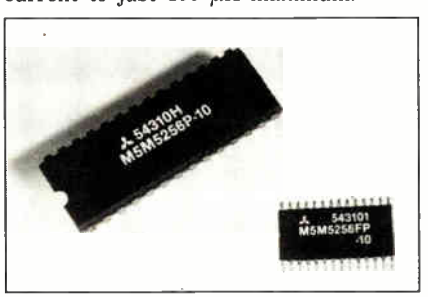
During the display cycle, data fed into the converter is latched simultaneously into the input registers of three DACs to generate the appropriate voltages on the red, green, and blue channels. Reliability is enhanced by a 24-hour burn-in at 125°C. The hybrid is available from stock now. Price is $76 each in 100-unit quantities.
Analogic Corp., 8 Centennial Dr., Centennial Industrial Park, Peabody, Mass. 01961. Phone (617) 246-0300 [Circle 367]

10-BIT-WIDE LATCH USES 80% LESS POWER

This 10-bit-wide bus interface latch reduces power consumption by more than 80% over its bipolar cousin, thanks to CMOS technology, says the company that makes both parts. The Am29C841's wide data path makes it well-suited for parity-based applications as well as for 16-, 32-, and 64-bit systems. With a 24-mA drive, the chip can be used for mid-board applications or systems with moderate drive requirements, the company says. A higher-performance version has an 11-mA drive. Already in production, the parts are available in 24-pin plastic and ceramic DIPs, and by the fourth quarter will also be available in plastic-leaded chip carriers. Prices begin at $2.20 each for 100-unit orders.
Advanced Micro Devices Inc., 901 Thompson Place, P. O. Box 3453, Sunnyvale, Calif. 94088.
Phone (408) 732-2400 [Circle 370]

256-K STATIC RAMS ARE FAST, LOW-POWER

A new family of 256-K static RAMs organized as 32-K by 8 is fully TTL-compatible. The CMOS parts are available now with 100-, 120-, and 150-ns access times; 70- and 85-ns versions will be available later this year. All parts have a typical current draw of 35 mA; maximum standby current is 2 mA, but a low-power option can reduce standby current to just 100 μA maximum.



Running on 5-V power supplies, the M5M5256 parts are well-suited for battery backup applications because they feature 3-V data retention. Available in small-outline packages as well as 28-pin DIPs, prices begin at $38.50 each for orders of 100 or more of the 150-ns parts.
Mitsubishi Electronics America Inc., 1050 E. Arques Ave., Sunnyvale, Calif. 94086. Phone (408) 730-5900 [Circle 366]

12-BIT DAC HOOKS TO 4- AND 8-BIT MICROS

Double-buffered input architecture allows this monolithic 12-bit digital-to-analog converter to interface directly with 4- and 8-bit microprocessors. All data-loading and transfer operations are accomplished through four control pins, and a clear pin can reset the 12-bit DAC register to all zeros. Current output settling time is 2 μs. The device has four-quadrant multiplying capability and operates from a single 5-V supply. CMOS technology keeps power consumption to a maximum 10 mW.

Pin-for-pin compatible with the Analog Devices Inc. AD7542 series, the HS7542 series is available from stock in plastic or ceramic DIPs. Pricing, in quantities of 100 or more, begins at $13.95 each. Military versions are available from $42.10.
Hybrid Systems Corp., 22 Linnell Circle, Suburban Industrial Park, Billerica, Mass. 01821. Phone (617) 667-8700 [Circle 369]

CCD SENSORS OPERATE TO 10 MHz

Nine new charge-coupled devices—both linear and area—are available for use in such applications as optical character recognition, bar-code scanners, optical measuring equipment, and video cameras. The CCDs offer high resolution and operating frequencies up to 10 MHz.

The seven linear CCDs, all of which operate from single 12-V supplies, have from 128 to 5,000 elements each. The two area CCD sensors have element arrays of 40 by 14 and 488 by 376, and operate from single 8-V and 15-V power supplies, respectively. Deliverable within 8 to 10 weeks of order, the devices come in hermetically sealed packages and cost $25 to $285 each in 100-piece quantities.
Toshiba America Inc., ECBS, Semiconductor Products Division, 2692 Dow Ave., Tustin, Calif. 92680.
Phone (714) 832-6300 [Circle 368]

GaAs FET PUTS OUT 25-dB LINEAR POWER

A high-gain gallium arsenide FET for narrowband and broadband amplifiers operates between 8 and 20 GHz. Designers of narrowband and broadband hybrid solid-state power amplifiers working in that range will find the HMF-1210 a useful building block in balanced designs requiring individual device linear-output power of 150 to 250 mW.

The FET provides typical linear power (power at 1-dB gain compression) of 25 dB at 18 GHz, with an associated gain of 4 dB. Under maximum gain tuning conditions, the HMF-1210 achieves typical gains of 6 dB at 18 GHz, 9 dB at 12 GHz, and 12 dB at 8 GHz. Associated linear power with such tuning is 22 dBm, 23 dBm, and 24 dBm, respectively.

Available from stock, the MHF-1210 is priced at $45 each in lots of 100.
Harris Corp., Microwave Semiconductor Division, 1530 McCarthy Blvd., Milpitas, Calif. 95035. Phone (408) 262-2222 [Circle 372]

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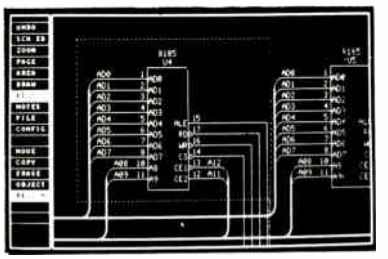

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TYPE AND NUMBER OF STUDENTS SOUGHT: **Electronics** **Avionics**

Electrical Computer Mechanical Computer Science Other(Draftsman, etc.)

Note: Last date coupons can be accepted for this year's summer job listings is November 19, 1986

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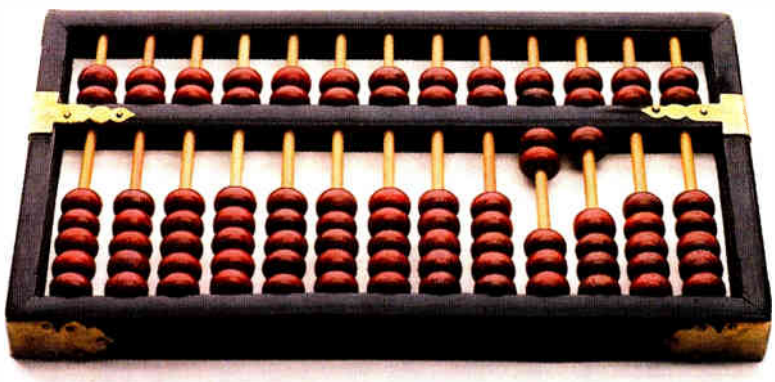

DIGITAL BY ANALOGY.

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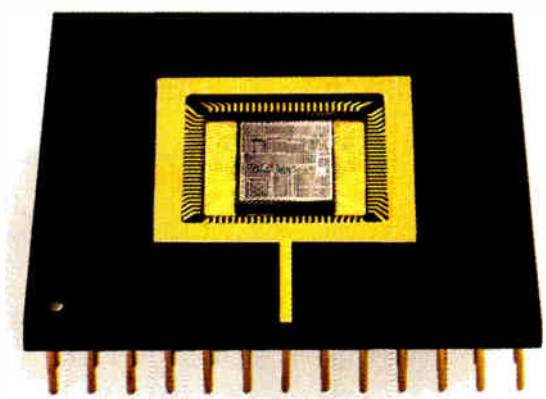

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For more information, call your nearest Analog Devices, Inc. sales office. Analog Devices, Inc.: Austria (222) 885504; Belgium (3) 237 1672; Denmark (2) 845800; France (1) 4687-34-11; Holland (1620) 81500; Israel (052) 28995; Italy (2) 6883831 (2) 6883832 (3) 6883833; Japan (3) 263-6826; Sweden (8) 282740; Switzerland (22) 31 57 60; United Kingdom (01) 9410-466; West Germany (89) 570050.

ANALOG DEVICES

World Radio History

VAPOR DEPOSITION SYSTEM SUITS ASIC PRODUCERS

REACTOR TAKES UP ONLY 15 FT² OF FLOOR SPACE BUT HANDLES VARIETY OF PROCESSES AND WAFERS

Application-specific integrated circuits most often are produced in short runs, making large, expensive, high-volume production equipment uneconomical. To meet the needs of space- and budget-conscious ASIC makers, ASM America has designed a plasma-enhanced chemical vapor deposition system that takes up only some 15 ft² of factory floor space, yet can handle short runs for a variety of fabrication processes involving wafers from 3 in. to 8 in. in diameter. Available now, the system has a base price of less than $200,000—compared with about $450,000 for conventional systems.

ASM says its SF50 system is one of the first pieces of semiconductor equipment designed specifically for ASIC production. Its small size stems in large part from a cantilevered boat loader that is integral to the system. Wafer-carrying boats extend outside the system only when a process tube is unloaded. And the Phoenix manufacturer maintains that the SF50 is the first self-cleaning deposition system. A proprietary technique developed by the firm cleans the system continuously as part of the process, reducing the particulate count and the need for maintenance requirements.

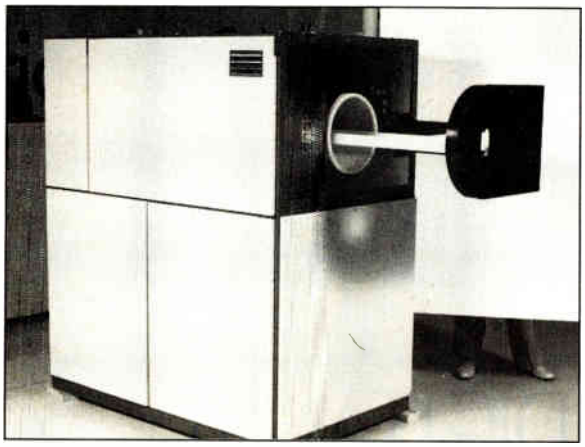
BEHIND A BULKHEAD. Because its footprint is about one-third that of conventional deposition gear, the SF50 can easily be tucked into existing clean rooms. In fact, the unit can be mounted on a bulkhead so that only its front panel projects into the clean room.

Despite its size, the SF50 is fully compatible with ASM's current deposition reactors. So processes and prototypes developed on this system can be transferred to volume production without changing parameters.

The new reactor uses a gas distribution system that achieves very high gas-purity standards. The system incorporates tubes of several sizes having independent processing systems that can operate different processes, wafer sizes, and loads. Two sequential controllers provide precise, repeatable process control.

Based on 1-sigma calculations, normal nitride, oxide, and oxynitride uniformities will vary less than 3% from wafer to wafer and from run to run. Point-to-point variation will be less than 4%.

All active gas lines are furnished with 0.02-μm filters and tested to verify leak-free operation to 4×10^{-9} cc/s of helium.



BOATLOAD. Cantilevered loading arm swings closed after wafer-carrying boats are loaded into process tube.

Point-of-use submicron filters are also provided. New disk-type graphite boats may be pyrolitic-graphite-coated or uncoated. Boats are designed for easy loading and manual or automatic removal.

ASM America Inc., 4302 Broadway, Phoenix, Ariz. 85040. Phone (602) 437-1405 [Circle 420]

SYSTEM CONTROLS PLATING BATHS

A computer-based chemical-control system provides a quantitative picture of individual elements during the printed-wiring-board plating process. The CCS 2100 Chemical Control System and electrolytic plating additives work together to allow board makers to control bath performance in precise statistical terms.

The bath is monitored continuously, and the system computer compares the data from the bath with preset standards and then determines what replenishment is necessary to maintain those standards. The system is available by lease only, and pricing is available on request.

ETD Technology Inc., 605 West County Rd. E., Shoreview, Minn. 55126. Phone (612) 482-7760 [Circle 431]

DEPOSITION GEAR IS LESS THAN $100,000

Producing gallium arsenide wafers is neither easy nor cheap, and when it comes to metal-organic vapor deposition equipment, there isn't much to be had for less than $200,000. The Model 422 Spartan vapor deposition system, however, is designed for applications, such as research, in which a big budget may not exist. Complete with gas and exhaust handling systems, a reaction chamber, a programmable controller, and several safety features, the Spartan costs $99,900.

The gas system boasts six sources, each using mass-flow controllers and a proprietary manifold for very thin layers and abrupt interfaces. The system, which can be used to grow GaAs, GaAlAs, and GaInP, among other materials, requires 20 weeks for delivery.

Crystal Specialties Inc., Systems Division, 16535 S. W. 72nd St., Portland, Ore. 97224. Phone (503) 684-0470 [Circle 425]

X-RAY IMAGING DEVICE HELPS FIND DEFECTS

The Micro Focus Fluoroscope, an X-ray imaging device, can magnify images up to 27 times, allowing easy visual inspection of solder joints, ribbon cable, and other products where defects are difficult to spot.

Boards can be tested during assembly, the company says, so problems can be fixed before defective boards are produced. In addition, the instrument can be used to measure the spacing of a ribbon cable, a process that otherwise requires the cable to be cut open for visual inspection. The 18-lb fluoroscope can be run off a 12-V, 2-A battery pack when used in a portable configuration, and is available in three versions: 30-kV, 50-kV, and 70-kV. The higher-voltage models are more capable of penetrating dense materials, such as solder.

Pricing ranges from $45,000 to $50,000, depending on the model; delivery takes four to six weeks.

Lixi Inc., 1438 Brook Dr., Downers Grove, Ill. 60515. Phone (312) 620-4646 [Circle 427]

World Radio History

PRINTER LABELS ICs AND PC BOARDS

The electronics industry has some special needs when it comes to labeling products, and the Bradywriter II Printer aims to address them. Designed to make labels and markers for ICs and other components, as well as pc boards, wire, cable, and terminal blocks, this portable dot-matrix printer incorporates a computer that allows hundreds of label messages to be stored for later recall.

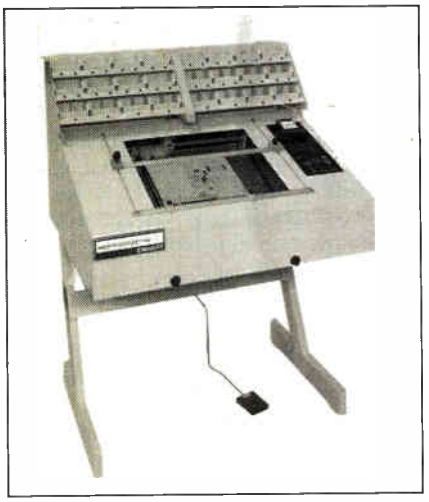
With a print speed of 120 c/s, the Bradywriter II has a detachable keyboard and display that can be taken to the factory floor for on-site label entry. Labels can later be printed out when the

unit is returned to the printer. Markers and labels can be serialized numerically, alphabetically, or both.

The Bradywriter II costs $2,795 and requires about three weeks for delivery.
W. H. Brady Co., Industrial Products Division, 2221 W. Camden Rd., P. O. Box 2131, Milwaukee, Wis. 53201.
Phone (414) 351-6630 [Circle 430]

MANUAL INSERTER CAN CUT AND CLINCH LEADS

A manual insertion machine for connecting leaded circuits to pc boards, the MCPA, can cut and clinch leads just as more expensive and automatic systems do. The system, which can handle board sizes up to 14 by 16 in., has a large programmable center distance of 2.25 in. and can be easily interfaced to the Data



Management System, from the same company.

The $17,000 machine takes four to six weeks for delivery.
Dynapert Division, Emhart Corp., 181 Elliott St., Beverly, Mass. 01915.
Phone (617) 927-4200 [Circle 429]

VISION SYSTEM CHECKS ASSEMBLED BOARDS

Simultaneous inspection of assembled pc boards for compliance with a broad range of guidelines is possible with a new vision system. Before the board is soldered, the IntelleVue DR 2000 checks to see that critical specifications—such as the length of leads, the clinch angle, and the wipe angle—are met. According to the manufacturer, the vision system also makes sure that neighboring leads are not so close that a short circuit could occur, while examining components to determine polarity.

Using up to 10 cameras, the DR 2000 can check devices mounted on both the top and bottom sides of pc boards. It can inspect leaded, surface mount, and hybrid devices, the manufacturer says, and can also inspect for a combination of clinched and straight leads.

The DR 2000 performs inspection inside an isolated chamber, allowing for complete lighting control. Unpredictable and changing ambient light does not allow the control required for operations like determining the proximity of two components' leads in order to predict potential solder bridges.

Prices for systems configured to do single-sided inspection start at about $110,000. Delivery takes 120 days.
Intelledex Inc., 4575 S. W. Research Way, Corvallis, Ore. 97333.
Phone (503) 758-4700 [Circle 432]

LASER TRIMS, DRILLS, MARKS, AND SCRIBES

The MEL-40 yttrium aluminum garnet laser can trim, drill, mark, and scribe a variety of hybrid microelectronic devices, packages, and substrates. The versatile system saves floor space by combining these four laser processing techniques. An additional advantage is that wafers stay cleaner, since the extra steps of moving substrates from one machine to the next are eliminated—all processes are housed in the same machine.

The MEL-40 trims both active and passive thin- and thick-film circuits. The drilling operations, are controlled by an IBM Corp. Personal Computer.

Prices for the MEL-40 start at $85,000; it can be delivered in 60 days.
Florod Corp., 17360 S. Gramercy Pl., Gardena, Calif. 90247.
Phone (213) 532-2700 [Circle 433]

THE COMPLETE SOLUTION FOR MICROCODED PROCESSORS.

Analog Devices' ADSP-1401 and ADSP-1410 offer you the highest speed and the greatest functionality for key tasks in microcoded systems – microprogram sequencing and data address generation.

The ADSP-1401 MicroProgram Sequencer is the industry's most advanced IC for generating microcode addresses. It supplies 16-bit addresses with a clock-to-address delay of just 25ns. The chip supports 10 maskable, prioritized interrupts, as well as traps. A 64-word internal RAM is user-configurable for subroutine stack, register stack, and parameter storage. Four event counters streamline nested loops.

The ADSP-1410 is the industry's only IC dedicated to flexible, high-speed data address generation. It provides 16-bit pointers to data memory 30ns after the clock edge. Its thirty registers hold address pointers, offsets, comparison values, and initialization values. With its powerful zero-overhead looping structure, the device can – in a single cycle – output an address, modify it, and conditionally branch to an initialization address.

Both Word-Slice™ components offer low-power CMOS technology (≤ 375 mW) in a 48-pin ceramic or plastic DIP. And, microcode system development tools and support are available from many third parties, including Hewlett-Packard, Step Engineering, and HiLevel Technology.

For more details, call your nearest Analog Devices, Inc. Sales Office.

ANALOG DEVICES

Circle 114 on reader service card

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POWER MOS FETS FEATURE LOW ON-RESISTANCE

UPGRADED 50-V P-CHANNEL DEVICES SHOW 100% IMPROVEMENT OVER 100-V VERSIONS

Improved on-resistance is the hallmark of a new family of 50-V p-channel power MOS FETs from International Rectifier Corp. The improvement over the company's 100-V devices tops 100%.

In the Hex 1 size (0.069-by-0.091-in. die), for example, the IRFD9010 has maximum on-resistance of 0.55 Ω, compared with 1.2 Ω for the 100-V p-channel devices. Other sizes in this latest addition to the El Segundo, Calif., firm's Hexfet line of power devices show improvements of a similar magnitude: in the Hex 2 size (0.087-by-0.137-in. die), the IRFD9020 has 0.28-Ω maximum on-resistance; the Hex 3 (0.115-by-0.175-in. die) IRF9Z30, 0.14-Ω.

Development of the low on-resistance p-channel family has a major advantage for users, says Allan Tregidga, executive director of IR's Electronic Business Group: p-channel MOS FETs are more economical than n-channel devices at modest current ratings. The new family, he notes, raises the crossover point where p-channel devices are the best value up to 12.5 A; previously it was 4.5 A. The family is particularly suited for motor-control circuits over 2 A.

For the Hex 1 IRFD9010, parameters include: continuous drain current, –1.0 A at 25°C, –0.65 A at 100°C; power dissipation of 1 W; on-state drain current minimum of –1.0 A; input capacitance, 240 pf typical, 360 pf maximum; output capacitance, 260 pf typical, 390 pf maximum; and reverse transfer capacitance, 30 pf typical, 45 pf maximum.

Already introduced are versions in the HexDIP and the TO-220 package. The surface-mounted product, in a D-Pak, will be available in the fourth quarter. Representative prices, in quantities of 1,000, are $1.20 for the Hex 1 size and $2.25 for the Hex 2. Samples are available now. *–Larry Waller*

International Rectifier Corp., Semiconductor Division, 233 Kansas St., El Segundo, Calif. 90245. Phone (213) 772-2000 [Circle 400]

ACTIVE-MATRIX LCD HAS 90° VIEWING CONE

Metal-insulator-metal technology is used in the Model 1001 active-matrix liquid-crystal display panel. Its 640-by-200-pixel array allows it to display a full 25 lines of 80 characters each. The active-matrix technology endows it with a very high contrast (10 : 1) and a wide, 90° viewing cone.

The display boasts a rise time of less than 50 ms and power requirements of 100 mW maximum. It works with IBM Corp. Personal Computers and compatible machines.

The 1001 is offered as a reflective display or a transmissive unit with an electroluminescent panel behind it. A number of polarizer options allow the designer to choose the two colors seen by the user.

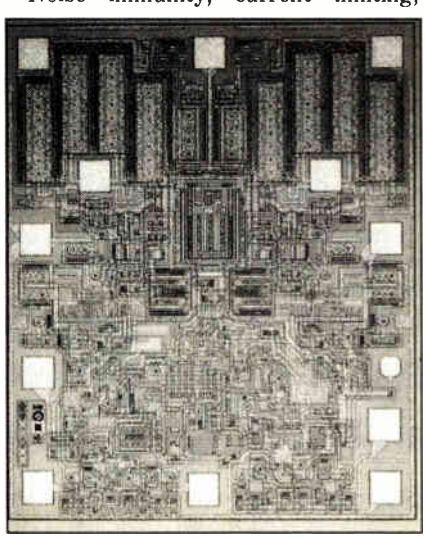
The basic display sells for less than $300 each in quantities of 10,000. Prototypes can be delivered during the fourth quarter, and production quantities will be available next year.

LC Systems Division of Eagle Picher Industries Inc., 210 Welsh Pool Rd., Exton, Pa. 19341.
Phone (215) 524-9944 [Circle 406]

DRIVERS REPLACE A HANDFUL OF PARTS

Two dual relay drivers cut costs by eliminating a number of components: each replaces a dual comparator, dual op amp, two power Darlingtons, two zeners, a voltage reference, and a few passive components. Designed to drive relays, dc motors, lamps, and other loads, the L9305 and L9306 each contain two separate drivers. Each driver consists of a comparator with hysteresis circuit, an open-collector output stage, a clamping zener, and a current limiter.

Noise immunity, current limiting, automatic thermal shutdown, and other protective features suit the parts to automotive and industrial applications, the manufacturer says.



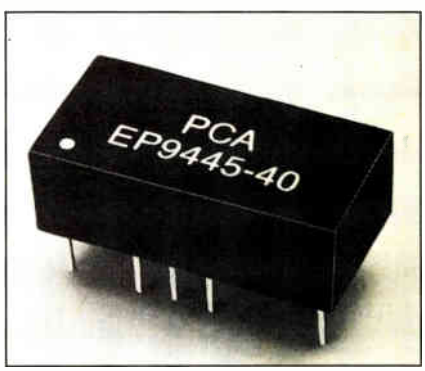
The L9305 is housed in the company's Powerdip 8+8 package, a copper-frame plastic DIP with eight pins on one side used to dissipate heat. It delivers 1.0 A per channel and dissipates 2.2 W in an 85°C ambient. It sells for $1.15 in lots of 1,000.

The L9306 comes in a miniDIP package and puts out 600 mA per channel. It sells for 90¢ in quantities of 1,000 and, like the L9305, requires a single supply of 3.5 to 18 V. Samples of both devices are available now.

SGS Semiconductor Corp., 1000 E. Bell Rd., Phoenix, Ariz. 85022.
Phone (602) 867-6100 [Circle 409]

DELAY LINES ARE ECL-COMPATIBLE

A series of 22 five-tap transfer-molded delay lines that are compatible with 10K emitter-coupled logic is aimed at high-speed applications requiring high delay stability, fast rise time, and no jitter,



such as memory boards, hard-disk-drive controllers, and signal processing. A noninverting ECL gate buffers the input to each EP9445-series delay line and each device's five output taps.

The parts are housed in 16-pin DIPs and offer total delays ranging from 6 to 1,000 ns. Each provides five equally spaced delays with rise times dependent on the total delay. For example, the EP9445-40 has taps at 8±1.0, 16±1.5, 24±2.0, 32±2.0, and 40±2.0 ns with a rise time of 5 ns maximum.

The delay lines require a single –5.2-V supply. Outputs are terminated externally with a 100-Ω resistor tied to –2.0 V. Pulse width is given as three times the total delay and pulse spacing as five times the total delay.

Standard EP9445 delay lines sell for $4.20 in lots of 1,000 and can be delivered in six weeks. Units with custom buffering and delay times are also available.

PCA Electronics Inc., 16799 Schoenborn St., Sepulveda, Calif. 91343. Phone (818) 892-0761 [Circle 410]

World Radio History

TRACK-AND-HOLD AMP UNRUFFLED BY SPEED

A high-speed hybrid track-and-hold amplifier, the CLC940 Flash-Track, provides very fast switching capabilities without losing supporting specifications, such as that for harmonic distortion. It is conservatively specified to provide a quick, reliable design solution in analog-to-digital conversion for communications, instrumentation, radar, and electronic imaging applications.

Among its key specifications are a hold-to-track acquisition time of 10 ns (to 1.0%) or 16 ns (to 0.1%); a track-to-hold settling time of 12 ns (to 1 mV); aperture jitter of 1.3 ps maximum; –3-dB small-signal bandwidth of 150 MHz; a slew rate of 470 V/μs; and gain nonlinearity of only 0.02%. Despite high-speed operation, harmonic distortion is held to –65 dB (below carrier signal), and the droop rate is only 20 μV/μs.

Packaged in a 24-pin DIP, the commercial version of the CLC940 sells for $196 in lots of 100. It is available now.

Complinear Corp., 4800 Wheaton Dr., Ft. Collins, Colo. 80525.
Phone (303) 226-0500 [Circle 407]

POWER MOS FETs MEET MILITARY STANDARD

A line of four power MOS FETs, rated from 100 V to 500 V and qualified to MIL-S-19500/542, is intended for high-speed applications such as switching power supplies, motor controls, and relay and solenoid drivers. The parts are listed under QPL-19500 for JAN, JANTX, and JANTXV reliability levels.

The military FETs are industry-standard 2N67XX types. The 2N6756 version is rated at 14 A, 100 V, and 0.18 Ω on-state resistance. Similarly, the 2N6758 is specified at 9 A, 200 V, and 0.4 Ω; the 2N6760 at 5.5 A, 400 V, and 1.0 Ω; and the 2N6762 at 4.5 A, 500 V, and 1.5 Ω.

The power FETs are housed in TO-204AA metal packages and operate over a range of –55° to 150°C. Total power dissipation at 25°C is 75 W. They are available now for $4 to $20.

Fairchild Semiconductor Corp., 313 Fairchild Dr., Mountain View, Calif. 94042.
Phone (415) 962-4046 [Circle 408]

BREAKOVER DIODES SAVE TELECOM GEAR

Glass-passivated breakover diodes provide reliable, fast-acting protection from transient overvoltage for digital telephone, modem, facsimile, Telex, and answering-machine equipment, as well as remote instrumentation monitoring lines.

The diodes are designed to operate in the range between 100 and 280 V.

The BR210 series comprises single bidirectional diodes in two-terminal TO-220AC-outline packages. The BR220-series breakover diodes are monolithic double diodes in a TO-220AB-outline package with three terminals, one of which is common. The BR220's monolithic construction ensures that the diodes are evenly matched and stable in operation.

The diodes go into action within 5 ns of the occurrence of a voltage transient that comes within ±12% of their nominal rating. They have a holding current of more than 150 mA and can cope with transients of up to 40 A.

Based on a proprietary four-layer pnpn thyristor technology, the diodes can replace voltage-dependent resistors in many applications. They are available now. Pricing varies, depending on the importing country.

Philips Elcoma Division, P. O. Box 523, 56 AM, Eindhoven, The Netherlands
[Circle 401]

In the U. S.—Amperex Electronic Corp., George Washington Highway, Smithfield, R. I. 02917. Phone (401) 232-0500
[Circle 411]

RECTIFIERS' PACKAGES CUT COST, SAVE SPACE

An entire family of Schottky and ultrafast (designated UES) rectifiers for switching power supplies is now available in plastic TO-247 power packages. Built in single- and dual-chip configurations, the rectifiers cover the range from 30 V to 200 V and 16 A to 45 A.

The TO-247 packages lower costs, save board space, and reduce assembly time. They are compatible with spring clips for mounting and heat sinking, and can eliminate the need for a heat sink when plastic TO-220-housed devices are being replaced.

The rectifiers offer very low forward voltages and high surge-current capabilities; reverse recovery times are less than 50 ns for UES types and essentially zero for Schottky types, which have guard-ring reverse protection.

Prices range from $2.13 to $5.39 each in quantities of 100.

Unitrode, 5 Forbes Rd., Lexington, Mass. 02173. Phone (617) 861-6540 [Circle 412]

FLOATING-POINT CHIP SET WITHOUT COMPROMISE.

Analog Devices' ADSP-3210/3220 floating-point multiplier and ALU are the industry's best available solution for fast IEEE arithmetic. This chip set provides blazing throughput and low latency – without compromise.

The chips execute an extensive set of operations on 32- and 64-bit IEEE floating-point and 32-bit fixed point. So, systems using them have the flexibility to support all standard data formats.

Circuit innovations and a fast 1.5μm process allow each chip to achieve 10 MFLOPS for most operations. And with CMOS, there are no power or reliability penalties.

What's more, number-crunching speed doesn't come from cumbersome pipelining. Because it has just one internal pipeline stage, the ADSP-3210/3220 is the industry's lowest-latency double precision chip set in production. And, with this architecture, microcode development is simple.

For more details, call your nearest Analog Devices, Inc. Sales Office.

ANALOG DEVICES

Circle 115 on reader service card

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HAND-HELD TEST UNIT PROBES DATA LINES

NONVOLATILE MEMORY STORES SETUP PARAMETERS AND TEST RESULTS FOR UP TO THREE YEARS

A "go anywhere" communications-line analyzer crams the features of a data-line monitor and a digital test set into a hand-held 18-ounce unit having 512-K of lithium-battery-backed nonvolatile static random-access memory. The battery-backed memory is able to store programmed test parameters and captured bits from data lines for up to three years.

The Analyst 2 from the Data Controls Division of AirBorn Electronics Corp. can handle a variety of widely used data-communications tests, with up to 448-K of the on-board nonvolatile RAM serving to capture data for review and analysis by users at a later time.

Based on a Z8 microcomputer, the system scrolls through a circular program menu in response to commands fed in plain English through an eight-key pad. The menus that show how to set up the system and the buffered data picked off transmission lines are read out on an electroluminescent back-lit liquid crystal display having two lines of 16 characters each.

WIDE RANGE OF TESTS. The Analyst 2 can be used in asynchronous, monosynchronous, bisynchronous, and synchronous data-link control (SDLC) and high-level data-link control (HDLC) environments. It also supports multiplexer operations. The tests include bit-error-rate test, block-error-rate test, character-error-rate test, single-error-rate test, errored-seconds test, time-delay test, and three kinds of distortion—isochronous, gross, and mark-space bias. The character error-rate test mode uses a pseudo-random pattern of 63, 511 (the standard set by the International Consultative Committee on Telegraph and Telephone), 1023, 2047, 4096, and the quick-brown-fox message. The unit has complete character sets conforming to ASCII standards and EBCDIC (IBM Corp.'s extended binary coded decimal interchange code).

ON THE LINE. Handheld unit combines a data-line monitor and a digital test set.

Data Controls has applied for rigorous Class B certification of the unit under the Federal Communications Commission's five-year-old guidelines for radio-frequency interface from home and business computers. William L. Payne II, president of the Data Controls Division in Addison, Texas, says the company is attempting to establish Class B certification as the de facto standard in portable test systems.

The FCC currently exempts test equipment from its RFI guidelines. Class B standards apply tighter controls on consumer computers and video systems compared with Class A guidelines for business systems. Payne anticipates FCC requirements to be eventually applied to test equipment as well, and he figures his test set will have an edge if the commission mandates the tougher standards.

The 8.25-by-4.25-by-1.25-in. portable unit attaches to RS-232-C data-communication lines via a standard 25-pin DB25 connector. Sixteen transmission rates, ranging from 50 bits per second to 19.2-Kb/s, are supported. An audio alarm may be set to beep whenever tests are completed, carrier or synchronization are lost, errors occur, self-test is completed, or if wrong entries are made via the keypad. The test-set unit also has a bank of eight tricolor light-emitting diodes indicating signals for data, clock, and control on the RS-232 lines.

In quantities up to nine, the Analyst 2 costs $2,495. A manual that reviews digital communications techniques is included. *–J. Robert Lineback*

Data Controls Division, AirBorn Electronics Corp., P. O. Box 670, Addison, Texas 75001-0670.
Phone (214) 248-9658. [Circle 380]

$495 BUYS PC-BOARD DESIGN SOFTWARE

A low-cost software package for IBM Corp. Personal Computers carries multilayer printed-circuit-board design from concept to camera-ready artwork. The program, which runs on the IBM PC, PC/XT, and PC AT, as well as compatible computers, is being offered for only $495 by Accel Technologies Inc.

"This is the first full-function IBM PC-based pc-board design package to break the $500 barrier," claims Raymond Schnoor, vice president of marketing for Accel. "Typically, an engineer's savings in time and money from laying out his own pc board pays for the software on the very first board."

Nor is Tango-PCB, as Accel calls the package, a stripped-down economy version. "The package offers features normally found only on expensive work-station-based design systems," according to Schnorr.

Tango-PCB will produce artwork on a plotter that can be taken to a board manufacturer for immediate turnaround to hardware. Rapid prototyping is available to anyone with a desktop computer.

The software designs boards as large as 32 by 19 in. Zooming in on the layout view makes possible precise component placement and track laying. Five zoom levels are available, from a view of an area measuring 1.6 by 0.95 in. to the full 32 by 19 in.

Users can select from nine grid spacings with grid lines 1, 5, 10, 25, 50, 100, 125, 156, and 200 mils apart. The finer grids let users place components such as DB-25 connectors and edge connectors with odd spacings. Tango-PCB is the only product in its class to offer 1-mil resolution, the company says.

The package can handle circuit boards with up to eight layers, including power and ground planes. The software also stores two "layers" that carry documentation text and a component-overlay image. Provisions for four track widths, seven pad sizes, four edge-connector pad sizes, and two DIP pad sizes help the system cover a wide range of uses.

An extensive library of common components comes with the system. Users can also create entries for specialized components.

A feature called track stacking makes it possible to repeat a complex sequence of tracks, which is useful for designing boards with many memory chips. Side-by-side, step-and-repeat plots are possible with an adjustable plot-starting

World Radio History

point, using the computer's cursor control keys.

Tango-PCB also provides a rubberbanding feature, which lets users move and rotate components while maintaining track connections. To facilitate layout revisions and design changes, the software allows designers to delete entire tracks or individual track sections, to break a track section into two parts, and to stretch track sections from their original end points.

Design flexibility is further enhanced through block operation, the marking of a particular block in a circuit and transferring of the block to another part of the layout. Block operations also include writing and reading blocks to and from disk files.

Multicolor checkplots may be produced quickly for complete verification of electrical connectivity and component placement. The software will also produce a bill-of-materials listing to aid in component purchasing and in board production.

The software supports 16 colors on systems with IBM's Enhanced Graphics Adapter in the 640-by-350-pixel mode. For computers with the IBM Color Graphics Adapter, it supports four colors in the 320-by-200-pixel mode.

Tango-PCB is available now. A demonstration kit—a full-function package with a clear, jargon-free tutorial—goes $10. *–Ellie Aguilar*

Accel Technologies Inc., 7358 Trade St., San Diego, Calif. 92121. Phone (619) 695-2000 [Circle 381]

TEST GENERATOR TRACES OUTPUTS BACK TO INPUTS

In Greek mythology, Theseus worked his way through a complex labyrinth to slay the fearsome Minotaur, and then retraced his steps to escape the maze. That feat is just about on a par with generating tests for new integrated circuit designs, according to Ralph Marlett, director of automatic test generation at HHB Systems, Mahwah, N.J. He says chip complexity has reached the point where seeking out logic faults is like fighting through a maze.

Marlett's group spent nearly two years developing its own Theseus, an automatic test generation program HHB unveiled last week at the International Test Conference in Washington.

Marlett says one of the difficulties of automatic test generation arises because circuits are sequential—the performance of each component affects almost every other component as well. "You can't just apply a stimulus to a component and make a measurement," he says. "You've got to apply a sequence of stimuli."

Keeping that in mind, Theseus takes after its mythical namesake by working its way backward through an IC design. Starting at the output pins, the program winds through the chip's architecture to the inputs, detecting possible fault locations as it goes.

Marlett says 80% of the designs Theseus has been tried on so far have "achieved fault coverage in the mid- to high-90% range" on the first run-through. Using the optional Knowledge-Based Compiler, which allows designers to tell Theseus about a particular device's eccentricities, can further improve the test generator's performance.

Marlett's group also took a new approach toward the primitive elements the program uses to simulate the chip under test. Most test-generation programs use simple gate-level primitives, such as NAND or NOR gates. Theseus, on the other hand, adds what are called complex primitives, such as counters and flip-flops, to that standard group. These primitives save tremendous amounts of computer power, Marlett says, because they require smaller chunks of code than would be required to simulate identical components gate by gate. An optional Library Development System allows designers to create their own additional primitives.

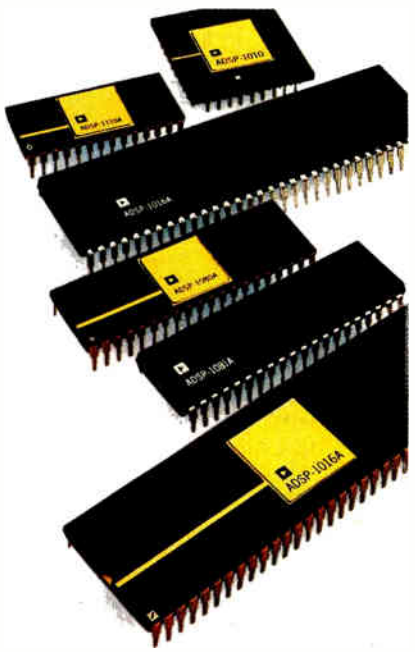
Theseus can run on a Digital Equipment Corp. VAX 780 or other high-performance minicomputer, as well as on Sun Microsystems Inc. Sun 3 workstations. An Interactive Testability Analyzer, which can recommend layout adjustments that make testing easier, is also available. Theseus is available now for about $200,000. The three optional packages are $15,000 each. *–Tobias Naegele*

HHB Systems, 1000 Wycoff Ave., Mahwah, N.J. 07430. Phone (201) 848-8000 [Circle 386]

UPGRADED SIMULATOR GAINS IN ACCURACY

Version 5.1 of Dash-Cadat Plus logic-simulation software supports minimum-maximum timing analysis, a technique that considers all the timing variations of the components being simulated. The number of simulation states has jumped from 12 to 21, increasing accuracy.

Release 5.1 now features a method called interval mathematics and a new



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These DSP components – fabricated in our 1.5μm CMOS process – are offered in multiple packages, including pin-grid arrays, ceramic DIPs, and low-cost plastic DIPs. Ceramic parts are available processed to MIL-STD 883B, Rev. C, on Analog's MIL-M-38510-certified lines.

For more details, call your nearest Analog Devices, Inc. Sales Office.

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Ad Council Coalition for Literacy

MOS analysis algorithm. The software also handles reconvergent fanout, a condition that causes trouble for most other timing simulators.

Based on the Cadat simulator from HHB Systems of Mahwah, N.J., Dash-Cadat Plus lets engineers use a "software breadboard" to analyze and debug designs, eliminating the time and expense of prototyping. Running on a National Semiconductor Corp. 32000-series coprocessor under AT&T Co.'s Unix System V, it integrates logic, timing, and fault simulation.

The software now runs on the 532 Personal Mainframe from Opus Systems, Cupertino, Calif., an expansion board for the IBM Corp. Personal Computer. This coprocessor uses a 10-MHz 32032 with up to 4 megabytes of memory. The board and Version 5.1's software improve performance by 200% to 300% compared with the previous version of the product. The $13,000 package is available immediately.

FutureNet Division of Data I/O Corp., 10525 Willows Rd. N. E., Redmond, Wash. 98073. Phone (206) 881-6444 [Circle 389]

HPIB SWITCH SYSTEM SIMPLIFIES SETUP

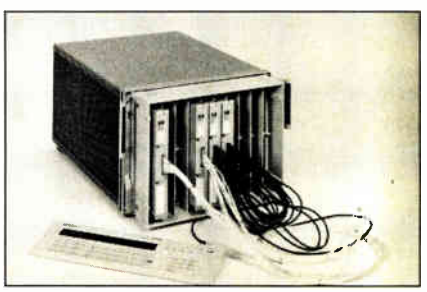
The HP 3235A switch/test unit reduces test-development time for HPIB-based production-test systems by providing high-performance off-the-shelf switching and interfacing to a wide variety of devices under test. It routes signals between them and test equipment such as digital multimeters and counters.

The 3235A is a 10-slot card cage whose mainframe can handle Basic programming commands, perform foreground and background tasks, and make pass-fail decisions. Up to seven 3235E extenders can be slaved for a maximum of 2,560 two-wire points.

Seven switch modules cover the range from low-level dc to 1 GHz. The unit also has a digital multimeter, digital I/O, and breadboard modules. A control panel can be added.

The HP 3235A mainframe is priced at $4,400, the 3235E extender at $3,700. The control panel costs $550, and modules range from $1,100 to $2,550. Deliveries take four weeks.

Hewlett-Packard Co., 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [Circle 390]



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MEETINGS

IECON '86, IEEE (Richard Born, Rexnord Inc., 5101 W. Beloit Rd., Milwaukee, Wis. 53214), Hyatt Regency Hotel, Milwaukee, Sept. 28-Oct. 3.

1986 Applied Superconductivity Conference, IEEE (Lahni Blohm, Code 6630C, Naval Research Laboratory, Washington, D. C. 20375), Hyatt Regency on the Harbor, Baltimore, Sept. 28-Oct. 3.

Satech '86, Intertec Communications Inc. (Sam Davis, 2472 Eastman Ave., Bldg. 34, Ventura, Calif. 93003), Indiana Convention Center Indianapolis, Sept. 29-Oct. 3.

Automated Design and Engineering for Electronics East, Cahners Exposition Group (1350 E. Touhy Ave., P. O. Box 5060, Des Plaines, Ill. 60017), World Trade Center, Boston, Sept. 30-Oct. 2.

Montech '86, Montreal IEEE (7063 St-Michel Blvd., Montreal, QC, H2A 2Z6, Canada), Convention Center, Montreal, Sept. 30-Oct. 2.

AFSM World Conference, Association of Field Service Managers (3475 Presidential Court, Suite B, Ft. Myers, Fla. 33907), Tropicana Hotel, Las Vegas, Oct. 5-8.

MILCOM '86, IEEE Military Communications Conference, *et al.* (Kenneth L. Rose, Ford Aerospace and Communications Corp., 3939 Fabian Way, Palo Alto, Calif. 94303), Monterey, Calif., Oct. 5-9.

TMS Fall Meeting, The Metallurgical Society Electronic Device Materials Committee (Meetings Department, 420 Commonwealth Dr., Warrendale, Penn. 15086), Marriott's World Center, Orlando, Fla., Oct. 5-9.

Fiber Optic Communications and Local Area Networks Exposition, Information Gatekeepers Inc. (Joan Barry, 214 Harvard Ave., Boston, Mass. 02134), Orange County Civic Center, Orlando, Fla., Oct. 6-10.

IEEE International Conference on Computer Design, IEEE Computer Society, *et al.* (1730 Massachusetts Ave., N. W., Washington, D. C. 20036), Rye Town Hilton, Rye Brook, N. Y., Oct. 6-9.

Small Computer System Interface Forum, Technology Forums, *et al.* (3425 Pomona Blvd., Suite F, Pomona, Calif. 91768), Hilton At Colonial, Wakefield, Mass. Oct. 7-9.

PC Expo Chicago, PC Expo (Steven Gross, 333 Sylvan Ave., Englewood Cliffs, N. J. 07632), McCormick Place II, Chicago, Ill., Oct. 7-9.

18th National Sampe Technical Conference, The Society for the Advancement of Material and Process Engineering (J. C. Johnson, Mail Stop 87-63, Organization 2-3621, Boeing Aerospace Co., P. O. Box 3999, Seattle, Wash. 98124), Red Lion Inn, Seattle, Oct. 7-9.

Connector & Interconnection Technology Symposium, Electronic Connector Study Group Inc. (P. O. Box 167, Fort Washington, Pa. 19034), Disneyland Hotel, Anaheim, Calif., Oct. 7-9.

Fall EIA Conference, Electronic Industries Association (2001 Eye St., N. W., Washington, D. C. 20036), Hotel del Coronado, San Diego, Calif., Oct. 7-10.

1986 Canadian Conference on Communications & Energy, IEEE (IEEE Canadian Region Office, 7061 Yonge St., Thornhill, Ontario, L3T 2A6, Canada), Queen Elizabeth Hotel, Montreal, Oct. 8-10.

ISA/86 International Conference and Exhibit, Instrument Society of America (67 Alexander Dr., Research Triangle Park, N. C. 27709), Houston Astrohall, Houston, Tex., Oct. 12-16.

CAM-I's 15th Annual Meeting & Technical Conference, Computer Aided Manufacturing-International Inc. (Suite 1107, 611 Ryan Plaza Dr., Arlington, Tex. 76011), Hilton Palacio del Rio Hotel, San Antonio, Tex., Oct. 14-15.

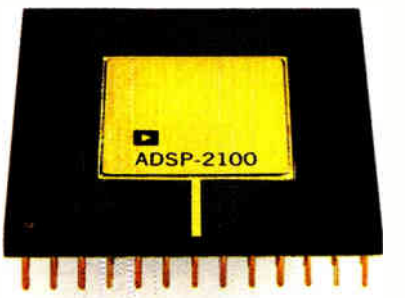
10th IEEE International Semiconductor Laser Conference, IEEE (Prof. Y. Suematsu, General Chairman, LD CONF'86, Dept. of Physical Electronics, Tokyo Institute of Technology, 2-12-1, O-okayama, Meguro-ku, Tokyo 152, Japan), Kanazawa, Japan, Oct. 14-17.

SEMICON/Southwest '86, Semiconductor Equipment and Materials Institute (805 East Middlefield Rd., Mountain View, Calif. 94043), The Infomart, Dallas, Oct. 15-16.

SCAN-TECH '86, Automatic Identification Manufacturers Inc. (1326 Freeport Rd., Pittsburgh, Pa. 15238), Moscone Convention Center, San Francisco, Oct. 15-17.

UNIX EXPO, National Expositions Co., (49 W. 38th St., Suite 12A, New York, N. Y. 10018), Jacob Javits Convention Center, New York, Oct. 20-22.

1986 IEEE GaAs IC Symposium, IEEE, *et al.* (Robert Markunas, Research Triangle Institute, P.O. Box 12194, Research Triangle Park, N.C. 27709) Grenelefe Resort and Conference Center, Grenelefe, Fla., Oct. 28-30.



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Electronics CAREER OPPORTUNITIES

Fall 1986 Planning Guide

Issue		Closing
October 2	**Computer Technology** CAD/CAM/CAE	September 15
October 16	**Technology Outlook Special Issue** ■ Semiconductors ■ Communications ■ CAD/CAM/CAE ■ Packaging & Production ■ Test & Measurement ■ Industrial Electronics ■ Consumer Electronics ■ Computers ■ Software **Military Technology** Military Career Section *Postcom Readership Survey*	September 29
October 30	**Software Technology** Artificial Intelligence	October 10
November 13	**Wescon Preview** Bonus Distribution at Wescon **Instruments Technology** Automatic Test Equipment	October 27
November 27	**Communications Technology** Fiber Optics Special Communication Career Section	November 10
December 11	**Semiconductor Technology** Linear ICs IEDM Preview **Military Technology** Special Section: Military Electronics *Postcom Readership Survey*	November 24
December 25	**Computer Technology** PC Boards Peripheral Boards	December 8

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Helicopter Avionics

Avionics System Engineer

In this position you should have a BSEE with three or more year's experience on military avionics programs. You should also have experience with designs using Mil-Std-1553 interface and the associated software/hardware background design requirements. Experience in working with the man-machine interface and familiarity with structured analysis/design methodologies is desired.

Software Engineer

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Flight Control Systems

Flight Controls Engineer

These positions require a BSEE degree and two or more year's experience associated with the design of microprocessor-based systems including I/O, data transmission, bus architecture, signal conversion and analog/digital circuit design. Applications include: Flight management development, wide band analog and high speed digital circuit design, flight control system development, software development and simulation/algorithm development.

RF Engineer

To qualify for this position you should have a BSEE degree with four or more year's experience in transponder development. Specific experience with spread spectrum operation of L-Band transponders and antenna pattern testing is desired.

Tactical and Reference Systems

Product Engineer

To qualify for this position you will need a BSEE degree with a minimum of two year's experience. In this position you will be working in support of momentum programs associated with digital and/or analog military avionics. You will be responsible for solving engineering design problems on the production line and for coordinating customer required changes into production hardware. Some direct customer interface also included.

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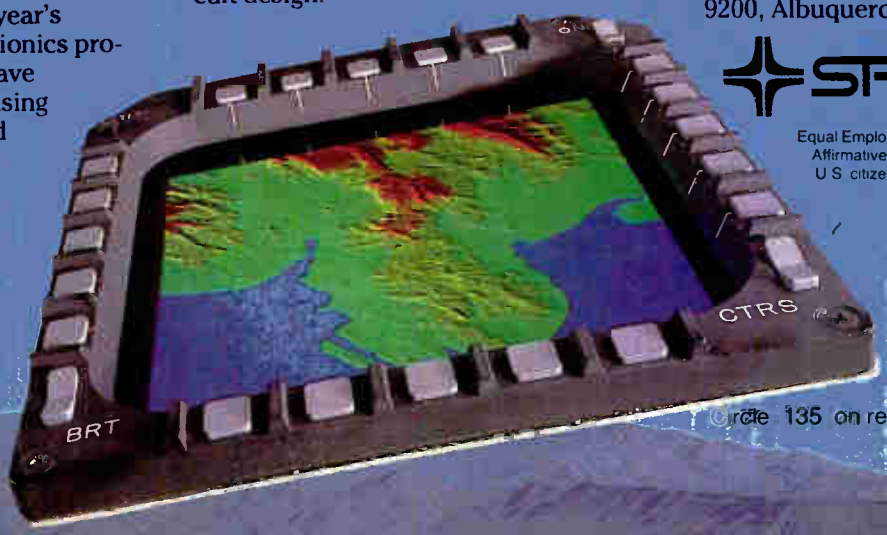

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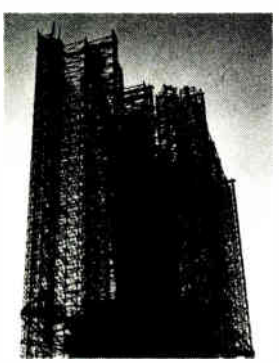

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ELECTRONICS WEEK

MOTOROLA TO MAKE FAIRCHILD'S FACT

Fairchild Semiconductor Corp. will name Motorola Inc. its first U.S. alternate source for Fairchild Advanced CMOS Technology (FACT) logic. The contract, similar to one recently signed by Hitachi Ltd. [*Electronics*, July 10, 1986, p. 20], may take a couple of months to complete. Motorola's alignment behind FACT and existing pinouts for the new CMOS logic is a victory for Fairchild over archrival Texas Instruments Inc. TI has sought Motorola's support for its plan to change standard pinouts [see p. 83].

MITSUBISHI BUYS U.S. WAFER MAKER

Siltec Corp., a silicon wafer manufacturer that put itself up for sale last spring after six money-losing quarters, found a taker in Mitsubishi Metal Corp. of Tokyo. Mitsubishi will pay about $30 million for the Menlo Park, Calif., company, which lost $14.3 million on sales of $40.5 million in fiscal 1985, and $4.3 million on $14 million in sales for the first half of 1986.

SANYO WILL MAKE CDS IN INDIANA

The rush of Japanese electronics companies toward offshore production continues. Sanyo Electric Co. is building a plant in Richmond, Ind., to manufacture optical and compact disks. Sanyo Laser Products Corp. will start producing at a rate of 5 million disks/year next June. Sanyo joins Sony, Japan Victor (JVC), and Nippon Columbia Co. in establishing CD manufacturing plants in the U.S.

GAIN SIGNS TO USE NTT TECHNOLOGY

The gallium arsenide startup Gain Electronics Corp. is hoping to "leapfrog the competition in the U.S." with a license from Nippon Telephone and Telegraph. Pending Japanese government approval, Gain will be the first U.S. company to use NTT's Enhancement Depletion Mode MES FET technology, which is considered more advanced than the SDHT (for selectively doped hetero-transistor) technology Gain is licensing from AT&T Co. The Somerville, N.J., firm plans to use the MES FET technology for memory and related devices and SDHT for other advanced integrated circuits.

STORAGE TECH EXPECTS REBOUND

Creditors of Storage Technology Corp. will vote next month on a new reorganization plan that suggests the firm may reach $1 billion in revenue before 1990. Storage Technology filed the plan earlier this month in Denver bankruptcy court in a move to emerge from Chapter 11 by early 1987. The Louisville, Colo., computer-peripherals maker plunged into the industry's largest bankruptcy case in October 1984 after revenue peaked at $1.08 billion in 1982. Last year, the company took in $673 million and returned to profitability [*Electronics*, June 16, p. 56], but it is not out of the woods yet. The company must still settle a dispute with the Internal Revenue Service over outstanding taxes and fines that could total more than $300 million.

SALES OF U.S.-MADE ELECTRONICS SLIP

Domestically produced electronics sales and services fell 3.4% to $109.4 billion in the first half of 1986, according to the American Electronics Association. But the AEA had one bright spot to report: June orders were $21.8 billion, the highest in 15 months. Derived from preliminary Commerce Department figures, the estimates differ slightly from those of the Electronics Industries Association, which reported that first-half shipments were down 1.8% [*Electronics*, Sept. 4, 1986, p. 168].

PROJECT VICTORIA PASSES FIRST TESTS

Pacific Bell says its Project Victoria technology, a method of multiplexing seven voice and data transmissions onto a single standard telephone line, performed better than expected in an initial test of 200 Danville, Calif. residents [*Electronics*, Aug. 21, 1986, p. 57]. PacBell found Victoria could transmit reliably up to 22,000 ft from the central switching office; it had expected an 18,000-ft reach. There were no major outages and the bit-error rate was better than predicted, the company says.

TWO SENSOR FIRMS AGREE TO MERGE

Two Silicon Valley sensor firms—IC Sensors Inc. of Milpitas and Transensory Devices Inc. of Fremont—are combining operations. IC Sensors is a volume maker of solid-state pressure sensors, while Transensory has been a research and development firm specializing in microsensors and micromachinery. The merged company will call itself IC Sensors but will also market equipment under the Transensory trademark.

HP, AMD OPPOSE TOXICS INITIATIVE

Hewlett-Packard Co. and Advanced Micro Devices Inc. are asking other California electronics firms to contribute toward a $600,000 war chest to defeat a toxics initiative on the November state ballot. "We agree with the intent of the initiative," an HP spokesman says. "But there are too many exemptions; the primary sources of toxics would not be affected." The initiative specifies that consumers and workers be warned about chemicals that have been found to cause cancer or birth defects.

KODAK PRINTER USES LED ARRAY

Eastman Kodak Co. is using an LED-array print-head built by Sanyo Corp. in its latest office publishing machine—a high-speed nonimpact printer that can produce 92 pages/min. Kodak designed custom circuitry and software to regulate the brightness of the LEDs in the 300-dots/in. print-head. The printer will be sold as part of Kodak's Keeps office publishing system as well as to original-equipment manufacurers for data processing applications.

IC PRODUCTION FALLS IN JAPAN

Japan's production of integrated circuits fell 16.2% in the first six months of 1986, and the Ministry of International Trade and Industry, while predicting a rise in the second six months, still expects a 7% decline for the year. Monthly production did top 1 billion units in June, for the first time ever; and in July, IC exports to the U.S. rose 12.1% over June's total—still 14.9% behind 1985.

DAINICHI KIKO ASKS COURT PROTECTION

Dainichi Kiko Co.—two years ago the fastest-growing robotics maker in the world [*Electronics*, Feb. 11, 1985, p. 45]—may go under. Late last month the Japanese firm sought court protection from creditors to whom it owed an estimated 5.5 billion yen, about $36 million at current exchange rates. Its primary backer, the insurance giant Daiichi Seimei Co., took over operations in late 1985 [*Electronics*, June 2, 1986, p. 49], but a sluggish and competitive robot market and delays in new-product development apparently were insurmountable obstacles.

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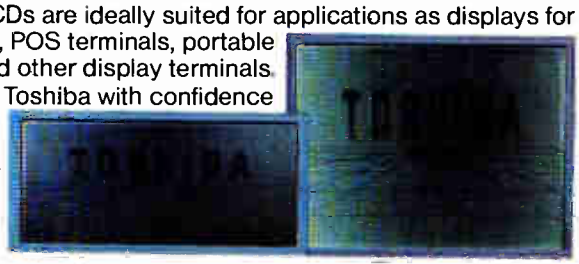
These versatile LCDs are ideally suited for applications as displays for personal computers, POS terminals, portable word processors and other display terminals. You can also look to Toshiba with confidence for a wide range of sizes and display capacity to suit your LCD requirements.



TLC-363 *TLC-402*

Specifications

		TLC-402	TLC-363B
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W × H × D)		274.8×240.6×17.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		−20° – 70° C	−20° – 70° C
Operating Temperature		0° – 50° C	0° – 50° C
Supply Voltage	V_{DD}	7 V	7 V
	$V_{DD} - V_{EE}$	20 V	20 V
Input Voltage		$0 \leq V_{IN} \leq V_{DD}$	$V_{SS} \leq V_{IN} \leq V_{DD}$
Recommended Operating Conditions			
Supply Voltage	V_{DD}	5±0.25V	5±0.25V
	V_{EE}	−11±3V Var.	−11±3V Var.
Input Voltage	High	V_{DD} − 0.5V min.	V_{DD} − 0.5V min.
	Low	0.5V max.	0.5V max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		3	3
Viewing Angle		15 – 35 degrees	15 – 35 degrees

Design and specifications are subject to change without notice.

TOSHIBA

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