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Electronics®

WHAT'S HOLDING BACK EXPERT SYSTEMS?

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INFERENCE'S STRATEGY TO SPEED THINGS UP

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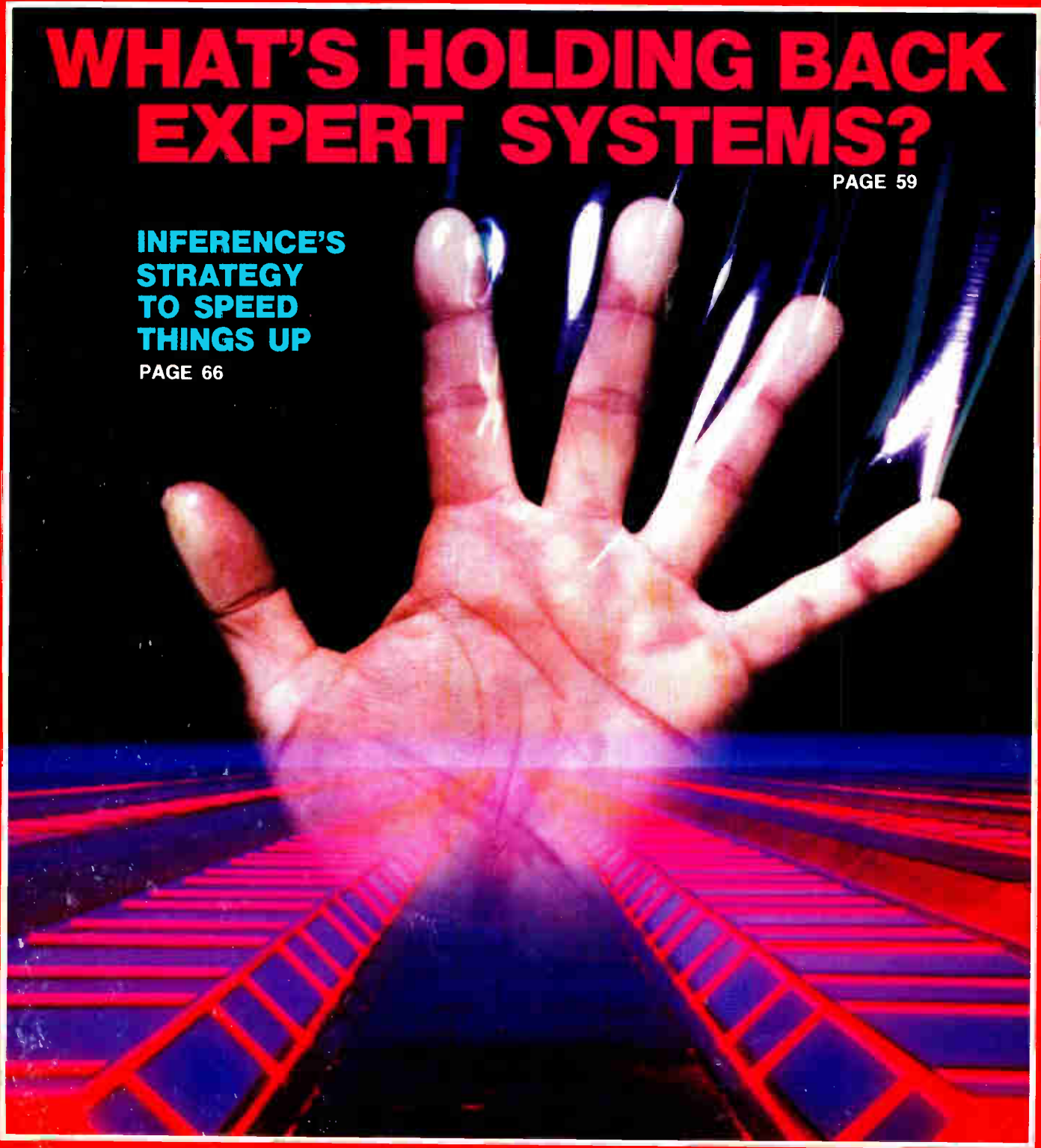

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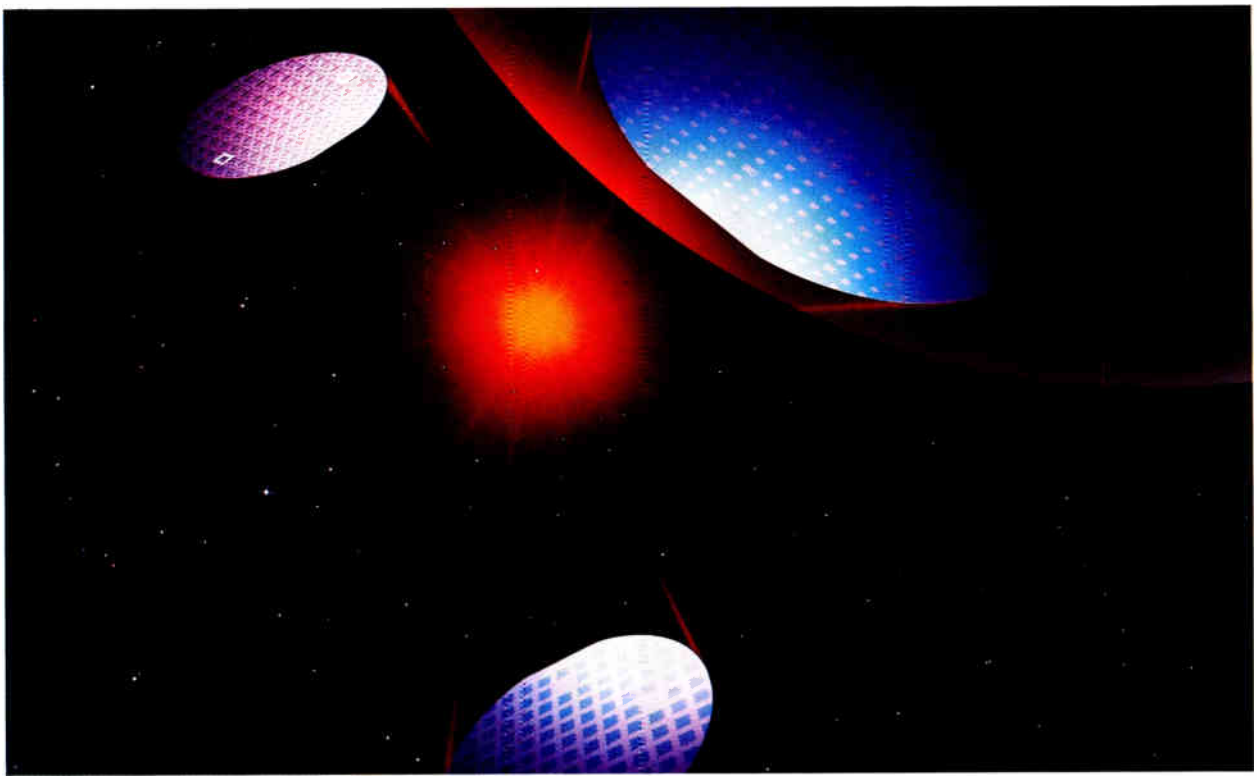

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MITEL SEMICONDUCTOR

ISDN COMPONENT NEWS

Vol. 2

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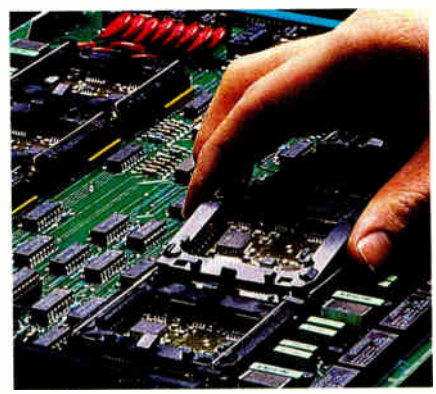

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PUBLISHER'S LETTER

It's been a year since *Electronics* last took an in-depth look at expert systems, and what has transpired in the meantime wasn't quite what was expected then.

Last year, just before the mid-August Ninth International Joint Conference on Artificial Intelligence in Los Angeles, it looked as if expert systems were poised to enter the computing mainstream. Taking stock of the technology's status this summer, Tom Manuel, our computer editor, says the technology seems to have stalled.

MANUEL. He's kept watch on AI activities for seven years.

Tom has been keeping tabs on AI for seven years, ever since it began to emerge from university labs. "Large-scale commercialization of expert systems and natural languages has been 'right around the corner' for several years now," he says. "Expert systems have a promising future if they can just get their sea legs."

Tom decided that a package of articles—rather than a single long piece—would be the best way to examine the problems that are currently holding up the development of expert systems and to analyze some of their possible solutions for our readers.

The centerpiece of the package we put together is the Special Report by Tom that begins on p. 59. It covers the main issues that seem to be slowing the progress of commercial expert systems. The report tells what many industry leaders say is being done and what further steps could be taken now to remove the roadblocks.

One of the major holdups, it turns out, is the Lisp language, which dominates among expert-system development tools and the technology in general. It has been difficult for non-AI and non-Lisp computer people to embrace this new and different language readily.

Because there are opposing opinions about Lisp and the role the popular AI language should or should not play, we decided to give each side a chance to speak its piece. So we invited two AI industry leaders to write their opinions on the role and importance of Lisp. On p. 64, Alex Jacobson of Inference Corp. argues the need for a non-Lisp approach to expert systems. On p. 65, Dick Gabriel of Lucid Inc. explains why he's convinced Lisp should be the language of choice for expert systems.

To complete the package, we asked software editor Alex Wolfe to take a detailed look at a new version of a popular expert-system development-tool package that has been translated from Lisp to the C language. That's the subject of the Technology to Watch beginning on p. 66, a detailed description and analysis of the C version 3.0 of Inference's ART package.

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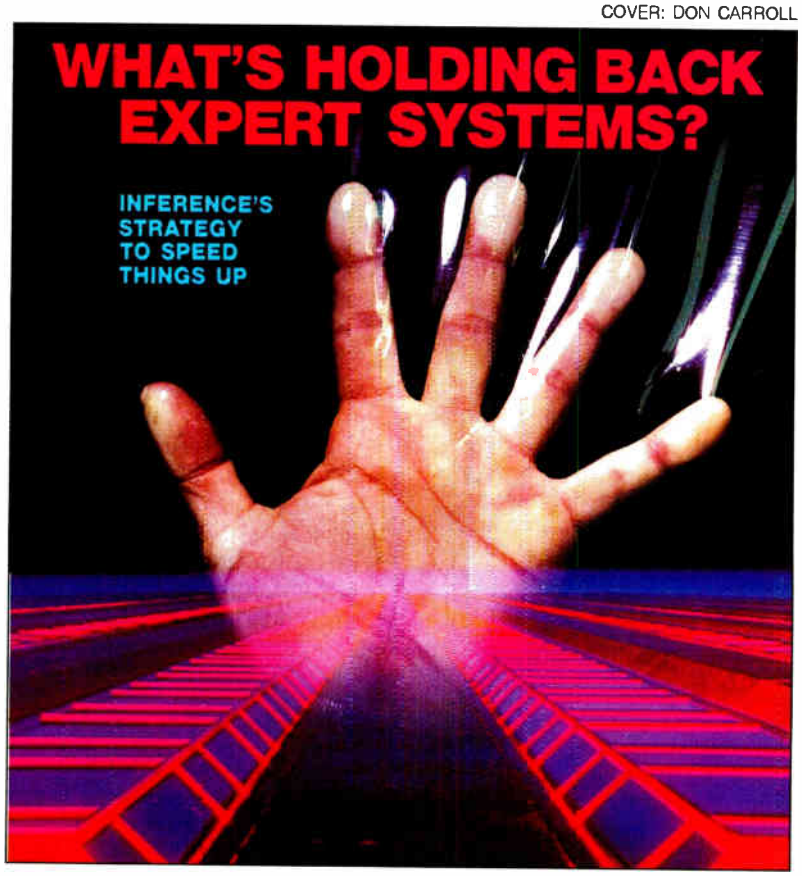

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WEEK 42

AMD not only lets you beat the clock. It lets you program it your way. From delay lines to system timing. All with one very timely device: AMD's new Am2971 Programmable Event Generator.

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WEEK 43

Don't get us wrong. TRW's bipolar 12 X 12-Bit Multiplier Accumulator is a very serviceable product.

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WEEK 44

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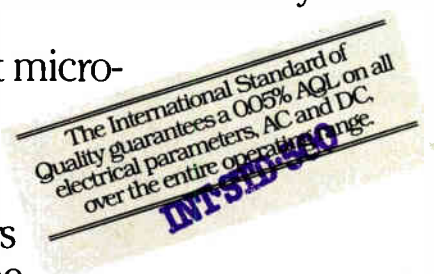

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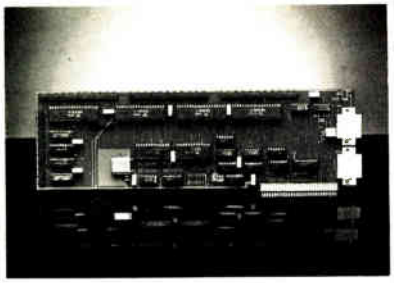

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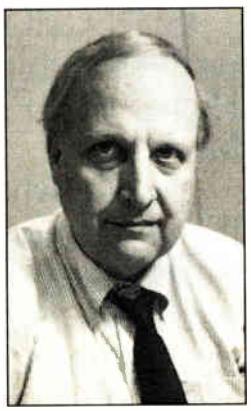
Half of our readers say they don't bother to read the other six major industry publications; they count on us to keep them up to date on new technology



For some readers, the arguments, carried of late in two of our industry's biweekly magazines, over how and when to cover new products are beginning to sound downright shrill. With all their expressed outrage and name calling, these editorials might even sound to the casual reader like the future of the industry itself was at stake. Relax. This intramural snarl between chief editors would be of little concern to most electronics industry executives.

But their arguments do make it easier for us to demonstrate how we cover new technology better than anyone. In fact, more than half of our readers now say they don't even bother to read either of those two magazines, or any of the six major industry publications, for that matter. They count on *Electronics* to keep them up to date on new technology and technology trends.

One of the feuding chief editors, whose magazine writes about products only when they already exist, sees "far too much science fiction" in the technical press. These articles often fall under a heading of "exclusive," he says, indicating the publication in which it appears is delivering something no other publication can. "After deceiving their readers, they have the audacity of boasting of having the most exclusive up-to-date coverage." Only 21% of his readers, he claims, want information on a product more than 90 days before it is available. But with new-product lead times getting longer and longer, designers need to know what's likely to be available six months or even a year out.

"Hogwash, rubbish, and balderdash" was the way the other chief editor answered the science-fiction charge. She claims her magazine puts great stock in product exclusives. So does *Electronics*, but we don't label every article in our publication as an exclusive. That's high-school journalism. Our readers expect to read about new technology in *Electronics* just as soon as information is available, and they don't want to wait to hear about a product until it's on the shelf. They also don't want just a recitation of the specs written for readers largely familiar with the technology.

Our readers want us to put new technology into perspective, assess its significance and impact in the marketplace, and tell how it could affect other companies and products. In short, they want us to add value, which is the prime directive at *Electronics*.

ROBERT W. HENKEL

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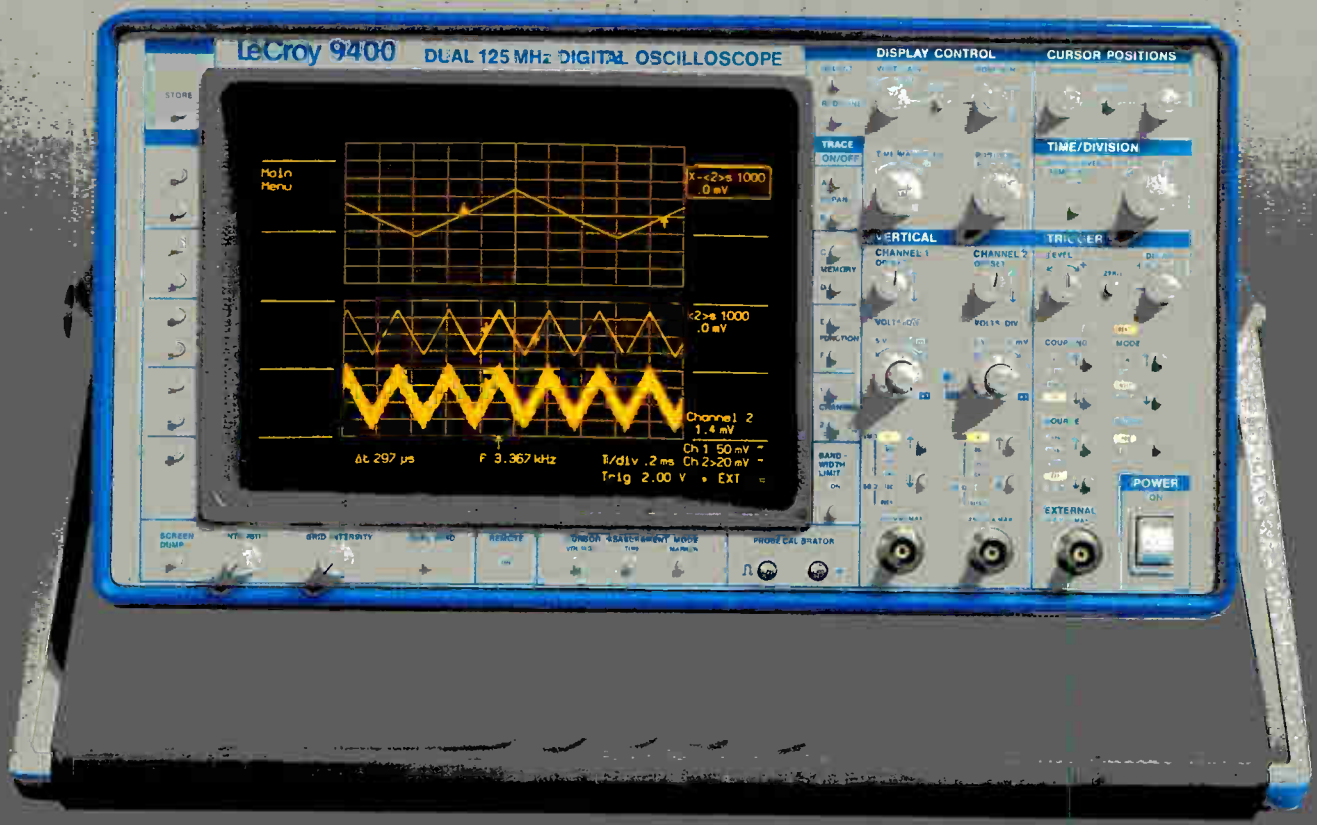

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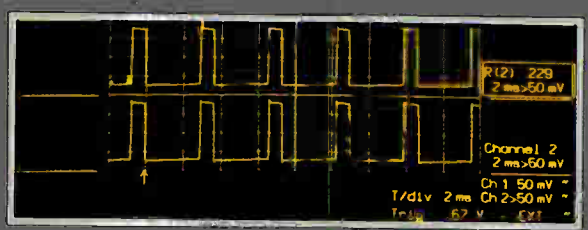

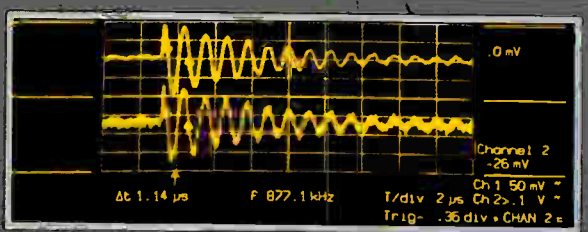

Top: Summation averaging over 1,000 waveforms, expansion and high resolution frequency measurement all shown in one display.

Middle: Extrema Mode shows glitches in digital circuitry, logged over 229 acquired waveforms.

Below: Digital filtering with a 9-point filter smooth noisy transient.

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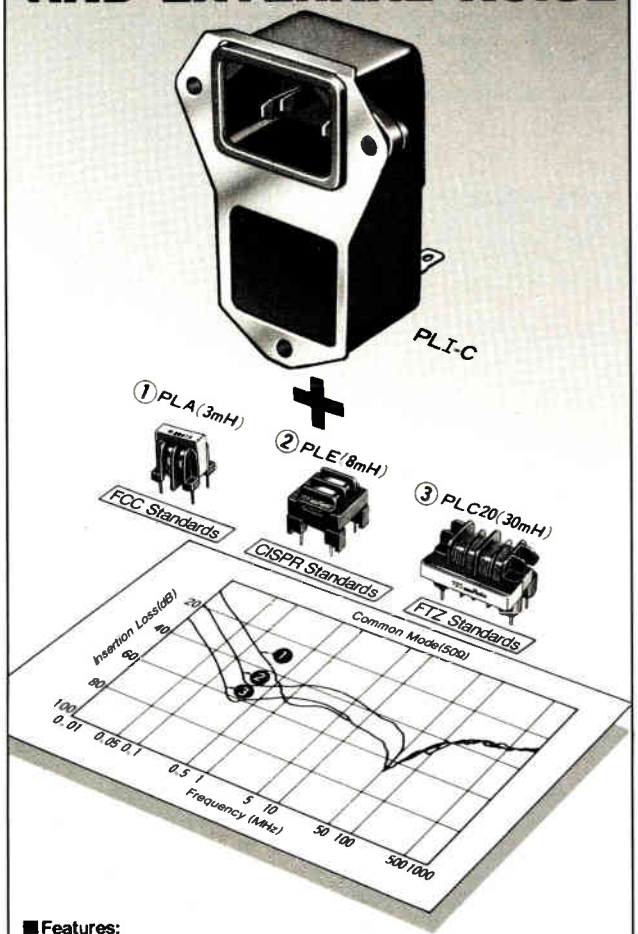

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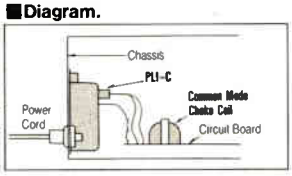
■ **Diagram.**



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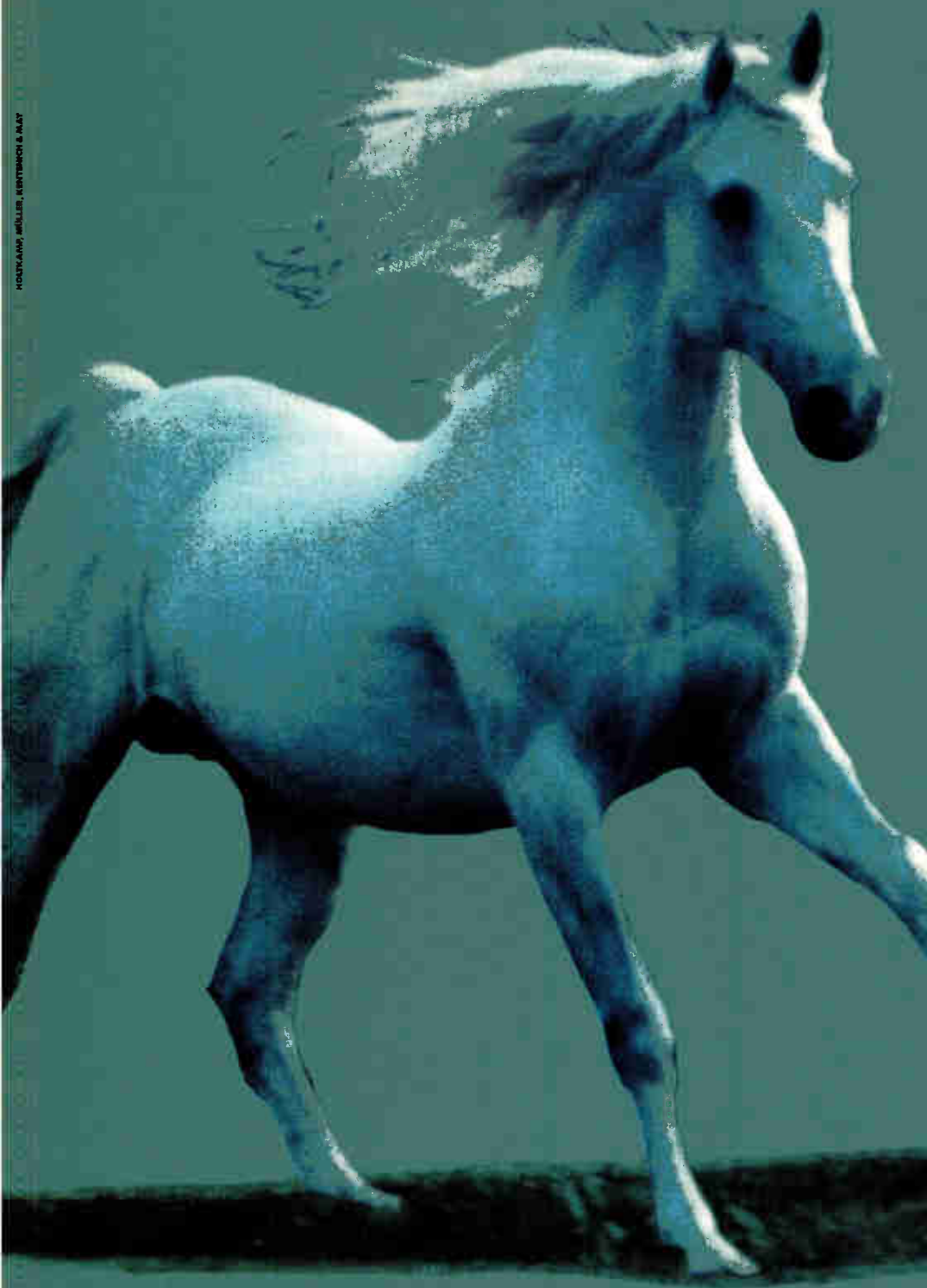

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LEE TAKES A BIG LEAP: BELLCORE TO A STARTUP

LEE. His job switch involves a new workday outlook—marketing for a small company rather than doing research for a giant one—and a new material, GaAs rather than silicon.

BRANCHBURG, N. J.

Charles Lee is on the move again, and it means big changes for the former Bell Labs researcher. In the two decades since he left Taiwan to become a chip designer in the U. S., Lee picked up two postgraduate degrees and set up shop in some of the biggest silicon houses in the country. Now he's jumping to Branchburg's tiny Gain Electronics Corp. to head a four-man team forging new ground in gallium arsenide chip design.

Lee is shifting from a research position at Bell Communications Research (Bellcore), Morristown, N. J., to be director of circuit design at Gain, one of a slew of new GaAs companies popping up in central New Jersey [*Electronics*, Jan. 13, 1986, p. 62].

Moreover, the 45-year-old Chinese native is also making the transition from silicon to GaAs technology. Most of Lee's experience has been with silicon CMOS design, the technology he used to help design AT&T Co.'s WE32000 32-bit chip set. And research that grew out of that project led Lee to invent a new and faster Zipper CMOS while he was with Bellcore [*Electronics*, April 28, 1986, p. 20].

Lee got his BS in electrical engineering at the National Taiwan University. He began his U. S. career in 1968 as a chip designer at Texas Instruments Inc., Dallas, after earning his master's degree in electrical engineering at the University of Cincinnati. He left TI to chase down a doctorate at the University of Michigan and, after he earned it in 1973, joined Bell Laboratories as a member of the technical staff.

At Gain, Lee will be using the talents that he applied in silicon research to develop high-speed GaAs integrated circuits. But to do so he must swap the mind-set of a researcher, who is concerned with technical feasibility, for that of a pragmatic businessman, who is more worried about manufacturability and a ready market. Lee says that he must get used to the fact that "obviously, research will be very low on my list of priorities."

SMALL DIFFERENCE. But Lee doesn't think it will be hard to adjust. "During the past five years, I was involved in the design of the Bell Mac 3200 chip set," he says, "and my responsibility was not only to design the chips but also to transfer those technologies to the production lines." And to hear Lee tell it, it won't make much difference if those production lines are for silicon or GaAs.

Many people think chip design for the two materials is vastly different. But Lee, who has worked with both, disagrees. "There's some general misconception that GaAs's defect density is awfully high, and hence that will make larger-scale integration difficult," he explains. "But the random defect doesn't hurt as much as people thought it would." Lee says the selectively doped heterojunction-transistor technology Gain is licensing from AT&T gives better immunity against defects and has a better speed/power product than other GaAs technologies.

Lee says part of the impetus for his move to Gain was the changes caused by the Bell System breakup. "I didn't think I'd ever leave AT&T," Lee recalls, but once the breakup was completed in 1984, his feelings changed.

Lee found himself a part of Bellcore, the research arm of the seven regional Bell operating companies. And while Bellcore wasn't a bad place to work,

World Radio History

the fierce loyalty common to most Bell Labs researchers had been worn thin. When Ray Dingle, Gain's founder and another Bell Labs veteran, recruited him, Lee knew the chance was too good to pass up.

Lee's new duties include product planning and development, but as happens in a small company, they overflow into many other areas as well. What excites him most is the opportunity to assemble what he promises will become the best design team in the entire GaAs industry. "Building a top-notch design team in the area is a very challenging task, but it's rewarding in a spiritual sense as well," says Lee, who describes himself as "an average scientist who got caught up in this divestiture chaos."

"How many opportunities of this kind exist in this industry?" he asks. "Not many." Lee says he now works 50% more than he did at Bellcore, and that travel has gobbled up about half of his first month at Gain. But although his absence may bother his family a bit—he is married and the father of three children—Lee is invigorated by all the new responsibility.

"This is time-scale pressure," Lee explains. "There isn't all the bureaucracy here. All the decisions have to be made quickly. Everything has to be done faster." *–Tobias Naegele*

DEPEYROT IS ON TRACK WITH HIS DESIGN CENTER

MEYLAN, FRANCE

It has been just a year since Michel Depeyrot launched a design center in Meylan for very large-scale integrated circuits. But he's already talking about "our major innovation"—a set of CMOS custom-chip design rules that adapt readily to any silicon foundry's process.

Depeyrot left his job as vice president in charge of design at Thomson Semiconducteurs in neighboring Grenoble to strike out on his own in a business that is still in its infancy in Europe, particularly in France. But by any measure, things at Dolphin Integration SA are on the right track.

By September, the staff will already have tripled from the original five (including Depeyrot), which should stabilize at around 25 next year. A Digital Equipment Corp. MicroVAX II should arrive soon. It will take over most of the graphics work, leaving the company's VAX-11/750 more time for simulation and verification. And by the end of the year, Depeyrot expects to break even.

In addition, he has secured as customers both his former employer and Matra Harris Semiconducteurs, which is the other French national integrated-circuit manufacturer. He expects to expand his customer base in the next couple of months with his first foreign client and systems house.

PRIDE IN TECHNOLOGY. Depeyrot's real pride is his company's set of portable design rules for CMOS 2-μm, two-metal-layer technology. "When you analyze the layers in a given IC producer's technology, you realize that even though there are 12 or 15, as many as half of them are not essential to the technology structure—they're added to the process to increase yields," he says.

"What we've done is to develop design rules based on seven abstract layers that correspond to the actual structure," he says. "When the design is finished, we can then generate a tape [for the mask set] automatically, depending on the foundry that is going to produce the chip." This, he argues, gives his customers a lot more flexibility in working with custom designs.

DEPEYROT. He has based his business on a portable set of CMOS design rules.

Depeyrot, 46, is a graduate of France's prestigious Ecole Supérieure d'Electricité, and he holds a doctorate in electrical engineering from Stanford University. Before working for Thomson he spent six years at DEC, where he led the team that put the PDP-11 minicomputer on a single chip.

Depeyrot's plans for Dolphin are ambitious. He says the company will enlarge its catalog of portable design rules to other technologies. It also will tackle the problems of mixed-power and VLSI technologies.

In addition, the company is beginning development of a couple of standard chips to fill market niches. About these Depeyrot will say no more than that they are tools for image and signal processing. *–Robert T. Gallagher*

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ELECTRONICS NEWSLETTER

U.S. AND JAPAN SIGN LAST-MINUTE SEMICONDUCTOR TRADE AGREEMENT

American chip makers could find their markets in Japan climbing an additional $1.5 billion above the current $600 million level, say White House officials. That optimistic estimate stems from the five-year semiconductor trade agreement reached last week in Washington by the two countries just before the deadline imposed by the Reagan administration. The pact calls for the Japanese government to set up an organization to help U. S. chip manufacturers sell into the Japanese market, to stop dumping by Japanese companies in the U. S. market, to monitor costs and prices on some semiconductor products exported to the U. S. and to guard against dumping in countries where Japanese and U. S. firms compete. In return, the U. S. agreed not to impose dumping-penalty duties on electrically programmable read-only memories and 256-K dynamic random-access memories, and to drop charges of unfair trade practices against Japanese firms that had been made under Section 301 of the U. S. Trade Act. □

1987 SEMICONDUCTOR OUTLOOK TOO CLOUDY TO CALL, SAYS IN-STAT...

Calling the trends in semiconductor markets, always a perilous task, has become more uncertain than ever. The outlook right now is so cloudy, says Jack Beedle of market research firm In-Stat Inc., that he cannot for the moment predict next year's trends. Beedle notes in his midyear report, released in late July, that "1987 remains a big question mark as we all wait for the final results of the upcoming tax changes." The only good news the Scottsdale, Ariz., seer projects is a fourth-quarter recovery of 7.7% in device sales, offsetting a 6.8% decline in the present quarter. Full 1986 results then would be a disappointing 2.9% increase over 1985. □

...BUT 1986 FIRST-HALF RANKINGS CLEARLY SHOW JAPAN'S ONRUSH

A doubly disappointing year is in sight for U. S. chip makers. In addition to a sluggish home market, they could well wind up second to Japan-based semiconductor houses in crucial market categories, according to a midyear report that Integrated Circuit Engineering Corp. will release later this month. The Scottsdale, Ariz., consultants say that during the first half of 1986, Japanese companies shipped $10.2 billion in integrated circuits, compared with $9.9 billion for their U. S. counterparts. What's more, the U. S. market for ICs was estimated at $7 billion, compared with $8 billion in Japan in the first six months. ICE also figures that Japanese firms hold the top three slots among first-half IC sales leaders—NEC, with $2.865 billion; Hitachi, $2.270 billion; and Toshiba, $1.975 billion. □

AT&T MAY SIGN ON INTEL AS PARTNER IN ISDN ALLIANCE

Another high-impact strategic alliance between a chip maker and a telecommunications-gear manufacturer now looks likely. Hard on AT&T Co.'s late-July announcement of an interface chip for integrated services digital networks, industry watchers surmised that AT&T would sign on Intel Corp. as a partner to develop a range of ISDN chips. A formal announcement of such a pact could come as early as September, although an Intel spokesman insists, "There ain't no deal yet." Presumably, the pair are teaming up to counter an ISDN alliance between Motorola Inc. and Northern Telecom Inc., signed in late May. Still unanswered is the question of how IBM Corp., a minority shareholder in Intel and a potential head-to-head competitor to AT&T in telecommunications, would react. Telecommunications consultant Spencer R. Rice, of S&R Consultants, Madison N. J., rates AT&T and Intel a stronger pair than Motorola-Northern. □

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ELECTRONICS NEWSLETTER

AMD'S OPTIONAL PINOUT QUELLS NOISE WITH DIE ROTATION

Advanced Micro Devices Inc. has yet to take sides in the roiling controversy over changing the pinout of advanced CMOS logic chips (see story, p. 29). But the Sunnyvale, Calif., chip maker has quietly made an optional quick fix to solve the noise problem that led Texas Instruments Inc. to make its change. In the fourth quarter, AMD will offer its Am29800 bus-interface circuits with the ground and power pins at the center of a 24-pin dual-in-line package. Achieved by rotating the die 90° inside the DIP, the move shortens the leads to the pins, lowering the inductance that can produce noise-voltage spikes in fast logic. The pinout move was requested by customer Honeywell Inc.'s minicomputer operation. "We find it is the cleanest way of bringing down the noise levels," says AMD's Roy Selinger, product marketing manager for logic and interfaces. Power and ground leads will remain on the corners of the DIPs in the standard 29800 products. □

TAPE-AUTOMATED BONDING MOVES TOWARD SUPERCHIPS

Tape-automated bonding has bounded into the realm of superchips. One of these chips packaged using the technique is Texas Instruments Inc.'s MegaChip Lisp processor. TI first attaches its large, square chip—394 mils on a side—to a 224-lead pattern on 70-mm tape from International Micro Industries, Cherry Hill, N. J. The tape-bonded chips in turn are bonded into custom ceramic chip carriers. Other companies are picking up on TAB for much larger chips. To meet their needs, IMI is developing a multilayered TAB interconnect for extremely large chips having over 2,000 leads. Such devices need TAB for its pretesting capabilities and for a minimum-length high-speed interconnection. □

SEEQ PINS ITS FUTURE ON EEPROMS

Seeq Technology Inc. is making a strong bet that its new flash electrically erasable programmable read-only memory technology can make conventional ultraviolet EPROMs obsolete. The San Jose, Calif., company last week abandoned the commercial EPROM business, laying off 150 of its 425 workers as it dropped out. Seeq has targeted its QPROM, a single-transistor flash EEPROM, as a high-density replacement for the EPROM [*Electronics*, June 16, 1986, p. 17]. EPROMs accounted for two thirds of Seeq's unit shipments but for only one third of its revenues. □

BROOKTREE CASTS ITS EYE ON ATE TEST-HEAD MARKET

Brooktree Corp. has spotted a promising semiconductor-market niche—blazing-fast very large-scale ICs that carry the many circuits required in leading-edge automated-test equipment. And the San Diego company plans to fill the niche fast, with first products due by the end of the year, says president James A. Bixby. Each new generation of ATE gear must run faster than the parts being tested, posing device-design challenges that cause the test head alone to account for 30% of an ATE system's cost. Total ATE market value of some $100 million this year makes this "a real opening for a company like us to go after," says Bixby. Brooktree's intentions for the ATE business have to be taken seriously: the privately held firm already has pulled off a similar feat with its first line of products. It makes specialized, very fast digital-to-analog converter chips that bundle many of the back-end processing jobs in computer-graphics displays. The firm, second-sourced by 5% owner Fairchild Semiconductor Corp., has won a major share of business in forthcoming work-station and computer lines. Brooktree designs and tests its products but uses outside foundries to fabricate them. □

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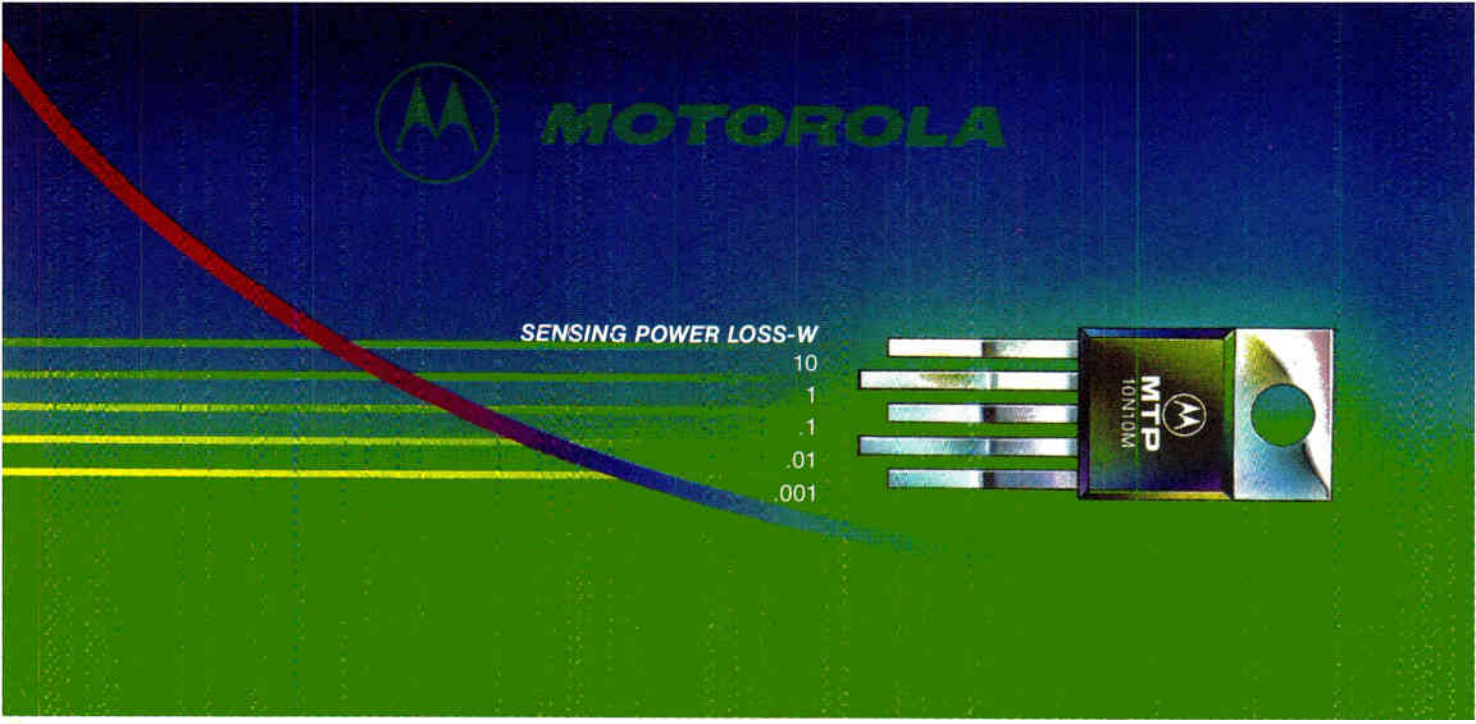

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Comparison of Current Sensing Techniques

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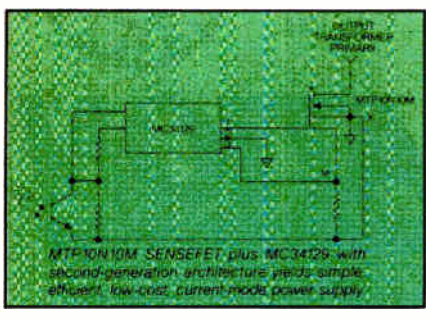

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PRODUCTS NEWSLETTER

TI TRIMS PRICE OF IBM TOKEN-RING CHIP SET BY 60%

Texas Instruments Inc. says greater sales volumes and manufacturing efficiencies have enabled it to cut 60% from the price of its adapter chip set for the IBM Corp. token-ring local-area network. The five-chip TMS380 has been reduced from $385 each to $150 in 100-piece quantities. The Dallas company is also quoting $88 prices for 1987 deliveries in lots of 25,000. □

AMD ADDS TWO 8-BIT CMOS SINGLE-CHIP COMPUTERS

Two new single-chip 8-bit microcomputers are coming from Advanced Micro Devices Inc. early this month. This week, the Sunnyvale, Calif., company rolls out its CMOS version of Intel Corp.'s 80C31. The chip has an active power dissipation of 120 mW. It contains 128 bytes of RAM, 32 programmable I/O lines, two 16-bit timers, and a full-duplex serial port. It sells for $10.25 each in a 40-pin plastic DIP. A similar 8-bit microcomputer with 8 K of ROM will be introduced next week. The 12-MHz 8053AH will cost $5 each in lots of 1,000 plus a $2,500 mask charge. □

DEC CONTINUES TO ROLL OUT NEW VAX COMPUTERS USING THE BI BUS

Digital Equipment Corp. continues to introduce new products at a steady clip. This week's expected announcements are of two new VAX machines using the VAX BI Bus. The VAX 8700 is said to offer performance in the range of 6 million to 7 million instructions/s. A second new computer reportedly will pack dual processors and execute at about six times the speed of a VAX 780. Pricing was unavailable. □

INTEL ANNOUNCES AI PROGRAMMING LANGUAGES FOR 32-BIT 80386

Intel Corp. is teaming with four software firms to offer versions of the artificial-intelligence programming languages Lisp and Prolog for the Santa Clara, Calif., company's 32-bit 80386 microprocessor. In doing so, Intel hopes to boost the chip's prospects as the engine of choice for AI applications, making it an attractive alternative to specialized Lisp machines. Intel's 80386 partners are Arity Corp., Concord, Mass., offering the Unix-based Arity/Prolog programming environment; Franz Inc., Alameda, Calif., with its Extended Common Lisp programming environment running under the Unix operating system; Gold Hill Computers, Cambridge, Mass., with the Gold Hill Common Lisp environment under both Unix and PC-DOS; and Lucid Inc., Menlo Park, Calif., offering the Common Lisp development environment, also under Unix. Pricing has not been set yet because the products won't be available until the fourth quarter (for Franz's Lisp) and the first quarter of next year (for the other three). Other products are in the works for the 80386 at two Palo Alto, Calif., companies: a Prolog package from Quintus Computer Systems Inc. and an expert-system tool kit from Teknowledge Inc. □

ON-LINE SERVICE KEEPS CHIP USERS MORE UP TO DATE THAN DATA BOOKS

Designers can throw away their printed data books and instead turn to an on-line data-base service that provides complete information on integrated circuits and discrete components. To be updated weekly, the DesignLine service from Engineering Information Services, Cupertino, Calif., is more current than data books, which are issued yearly. DesignLine differs from its competitors in that it will make available three analysis services: logic simulation, behavioral modeling, and physical modeling. The service provides both text and graphic information—such as a part's pinouts—and charges $60/h; it is delivered over phone lines to a customer's personal computer. □

World Radio History

PRODUCTS NEWSLETTER

AI GEAR GOES TO MARKET IN JAPAN, SALES IN U. S. TO FOLLOW

Mitsubishi Electric Corp. has turned some of the first hardware developed for Japan's Fifth Generation Computer Systems Project into a powerful work station for artificial-intelligence research. The Tokyo firm now offers—for $125,000—a commercial version of the personal sequential inference (PSI) machine developed by the Institute for New Generation Computer Technology [*ElectronicsWeek*, Dec. 3, 1984, p. 57]. Mitsubishi's PSI, which has 20 megabytes of dynamic RAM, uses an extended version of the Prolog AI language. In addition to the main memory, which can be extended to 80 megabytes, the work station has 40-K bytes of cache memory, two 1-megabyte floppy disks, a 200-megabyte hard disk, a 17-in. monochrome display, and a printer. Mitsubishi expects to start exporting the work station to the U. S. by the end of next year. □

DISTRIBUTED-FEEDBACK LASER BOOSTS FIBER-OPTIC TRANSMISSION DISTANCE

NEC Corp. will start production in September of single-mode distributed-feedback laser diodes for the 1.55- and 1.3-μm bands. The devices are suitable for high-capacity single-mode optical-fiber circuits operating at 1.6 gigabits/s. They will transmit data over distances of 100 to 200 km at a 1.55-μm wavelength and 80 to 100 km at 1.3 μm without repeaters. The 1.55-μm NDL5650 has a power output of 5 mW and will sell for $3,526, while the 1.3-μm NDL5600 is rated at 8 mW and will sell for $2,885. Production will start at 500 to 1,000 pieces a month, rising to 2,000 a month next year. □

EMCORE TO UNVEIL PRODUCTION VERSION OF ITS DEPOSITION SYSTEM

Come this fall, Emcore Inc. will have the first truly automated production version of its GS 8000 metal-organic chemical-vapor-deposition system. The South Plainfield, N. J., maker of processing systems for growing layers on gallium arsenide wafers says the new model will feature cassette-to-cassette wafer handling, doubling the 40-wafer-per-day throughput of Emcore's laboratory systems [*Electronics*, Aug. 5, 1985, p. 53]. The unveiling is slated for Semicon East next month in Boston, and the system will cost about $200,000 for a low-end model to nearly $1 million, depending on user requirements. □

TRW FLASH CONVERTER SUITED TO HIGH-RESOLUTION RADAR

A monolithic 9-bit flash analog-to-digital converter from TRW Inc. operates with linearity errors of less than 0.2% (adjustable to 0.1%) over the full −55°C to +125°C military operating range. The TDC1049's low error rate and 30 megasamples/s sampling rate suit it for high-resolution radar, infrared processing, and video-data conversion. The chip, which is available now from TRW's LSI Products Division in La Jolla, Calif., has 57-dB signal-to-noise ratio. The TDC1049J3A military-grade version is priced at $560 per chip. □

SOFTWARE PACKAGE KEEPS TABS ON IEEE-488 BUS ACTIVITY

A troubleshooting software tool from Interface Technology for the widely used IEEE-488 interface bus can substantially reduce system integration time. The Bus Analysis System works with the Glendora, Calif., company's model 488 Bus Analyzer and an IBM Corp. Personal Computer or compatible machine to provide complete monitoring, control, and analysis functions. The system has two levels of control to exercise an interface under test. It can simulate any condition or sequence, and no matter how complex the system, the monitor can quickly show bus activity, including the control lines. The software package is priced at $225 and will be available in 6 to 8 weeks. □

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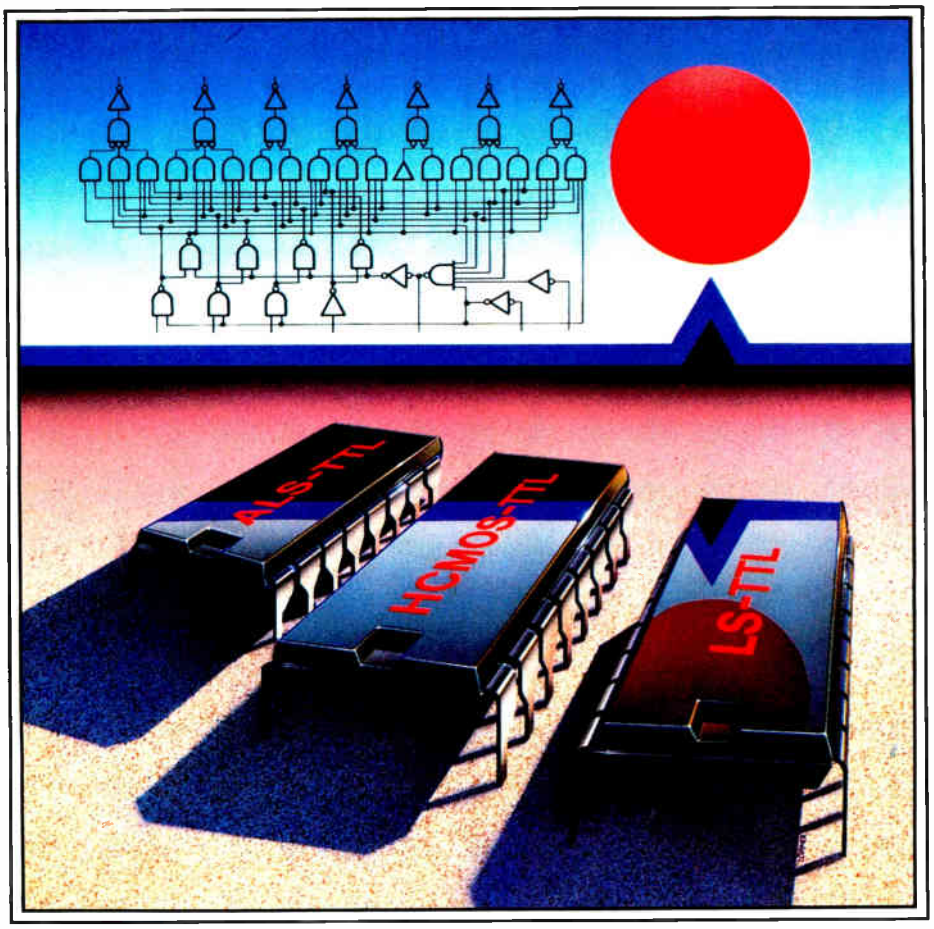

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Electronics

IT'S AN ALL-OUT FIGHT OVER PINOUTS FOR FAST CMOS LOGIC

MOST AGREE THERE IS A NOISE PROBLEM, BUT IS TI'S FIX TOO DRASTIC?

DALLAS

A controversial bid to break from two decades of packaging standards has landed the new generation of CMOS glue logic in what is expected to be the pinout battle of the decade.

Commodity glue-logic parts generally use package pinouts that are standard across chip families. Suddenly, however, Texas Instruments Inc. and its second-sourcing partners are changing the rules, casting a cloud over the next wave of fast CMOS logic.

TI, along with Philips and the Dutch giant's U. S. subsidiary, Signetics Corp., are moving the ground and Vcc (power) pins on future advanced CMOS logic from the corner to the center of dual in-line packages [*Electronics*, July 24, 1986, p. 21]. The move is aimed at reducing the inductance of long leads and quelling system noise—voltage spikes that commonly occur on unswitched pins when multiple outputs are switched simultaneously in fast logic chips.

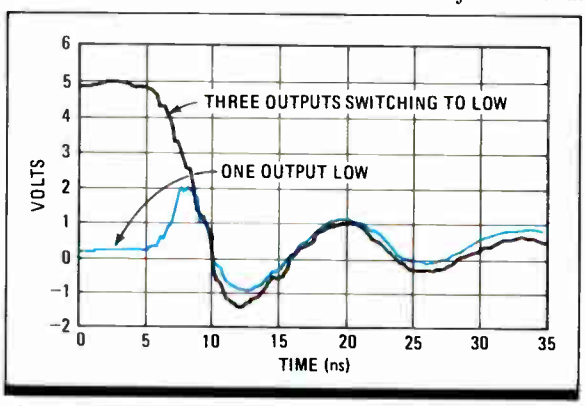
But the decision has stirred a storm of protest from early suppliers and future vendors of advanced CMOS logic. Adamantly opposed are Fairchild Semiconductor, Hitachi, Integrated Device Technology, RCA, and VTC. Motorola and National Semiconductor, which launched the first generation of silicon-gate CMOS logic five years ago, remain undecided as they consider entries into the unfolding market.

At stake are fortunes in advanced CMOS logic markets, the next generation of fast computers and work stations, and the life span of the through-hole DIP, which emits more noise from pins than do the short-leaded surface-mount packages.

OPPOSITION. Opponents charge TI, Philips, and Signetics with making a calculated marketing maneuver aimed at slowing the use of advanced CMOS logic until their own products are available late this year. TI and Signetics counter that the noise problem is polluting new board designs. They plan to submit to Jedec's 40.2 logic committee their plan to change the pinout and in some cases increase the number of ground leads to four and Vcc leads to two on chips with more than three outputs. The committee will meet Aug. 13-15.

The new pinouts increase the length of the 300-mil-wide DIPs for a given function. Most existing logic parts housed in 14-pin DIPs would go to 16 pins. The 16-pin chips would grow to 20, and the 20-pin parts to 24; TI is developing a 28-pin 300-mil DIP for current 24-pin functions. To help offset the size increase and ease board layout, Signetics and TI are also proposing a new flow-through architecture that places most inputs on the right side of the package and outputs on the left.

Many Jedec members question efforts to alter all logic functions, because the larger multiple-output components—such as octal bus drivers—are the center of most noise concerns. Fairchild, Integrated Device Technology, RCA, and other companies believe the bulk of the system-design hurdles can be reduced or eliminated either by new output-driver circuits, more prudent board layouts, or, in the long run, by greater use of surface-mount packaging.



THE PROBLEM. A scope trace shows how one output of a TI AC00 part bounces when three other outputs are switched.

But TI's Delbert A. Whitaker, senior vice president in the Semiconductor Group in Dallas, says the only way other suppliers can keep the speeds and existing pinouts without data loss is "to repeal the laws of physics." Whitaker says he was the last top TI manager to be convinced by internal technical arguments favoring a break with the existing standard—which was, ironically, set by TI in the mid-1960s with the introduction of 74-series TTL.

While logic merchants draw their battle lines, system-hardware designers are faced with trying to distinguish between technical truth and strategic jockeying. As in all pinout wars, major casualties are nearly certain among both chip makers and chip users.

"We are going to be more cautious and wait for more functions to become available—second sources and more pricing information—before committing ourselves to any of these new CMOS logic families," says Andy Bechtolsheim, technology vice president of Sun Microsystems Inc., Mountain View, Calif. "Ultimately, the new pinout is the right move. It is just that they should have done it 10 years ago." He calls the move "a very painful thing, because you cannot upgrade or retrofit the new CMOS logic into designs."

Even with the changed pinout, systems makers will have to struggle with noise at the board level, says Bruce Imsand of work-station maker Intergraph Corp. "No one is going to have a good time pushing 1.5-ns edges around on a 100-in.^{2} board," says Imsand, vice president of systems development at the Huntsville, Ala., company. "That's why I have to chuckle a little when I hear [semiconductor] people getting heated up about what almost seems to be an issue in an academic vacuum, compared to overall board design.

"I think TI is right—if the technical issues were the only issues." But he worries that a new pinout leaves no fallback to existing bipolar parts if problems crop up. Intergraph has chosen advanced CMOS logic from Fairchild, which uses the standard pinout.

Other chip customers who favor the status quo mostly want drop-in replacement of older chips to speed up or cut the power use of existing boards, says Ray Becker, Fairchild's technology manager

World Radio History

BEFORE THE PINOUT BOMBSHELL: A CHRONOLOGY

Here's how the industry stepped into the controversy over pinouts for advanced CMOS logic (ACL):

- **1985.** First half. Early ACL parts appear with bipolar speeds and compatible pinouts from such companies as Integrated Device Technology Inc. and VTC Inc. Another, Zytrex Corp., after splashing "Bipolar bites the dust" across billboards, files for protection under Chapter 11.
- May. Fairchild Semiconductor Corp. discloses it will be aiming an ACL family at Texas Instruments Inc.'s advanced low-power Schottky line. TI lays plans to counter with ACL of its own.
- October. Fairchild unveils its FACT (Fairchild Advanced CMOS Technology) family.
- Fall. TI and Signetics Corp. start alternate-sourcing talks for ACL. The two bipolar-logic competitors also discuss common problems with noise produced by the simultaneous switching of multiple outputs in TI's ALS/AS and FAST products sold by Signetics. Engineers start looking for a way to cut noise.
- **1986.** January. Fairchild begins volume shipments of its first FACT parts.
- February. TI, along with Philips and its Signetics subsidiary, announces intentions to develop ACL parts, indicating that they will be pin-compatible with existing bipolar-logic families. About the same time, TI sees working silicon on its first three 1-μm parts. Several weeks later, marketing managers yield to technical arguments: the decision is made to move power and ground pins to the center of the package, causing a three-month delay in product introductions.
- March. RCA Corp. unveils a line of standard-pinout ACL.
- May. TI and Signetics begin briefing prime customers and some competitors on plans to move pins on ACL in hopes of getting industry opinion behind a proposal they plan to make before the August Jedec meeting.
- Early July. Hitachi Ltd. announces it will second-source Fairchild's FACT line.
- Mid-July. Fairchild, armed with copies of the pinout proposal from TI and Signetics, takes the initiative, campaigning publicly for no change in the location of ground and power pins. Fairchild claims the TI ACL speeds have been set too fast by mistake. Hitachi, Integrated Device Technology, RCA, VTC, and others plan to fight the pinout change.
- Late July. Jedec 40.2 chairman Richard Funk says his panel does not plan to take up the TI-Signetics proposals. Integrated Device Technology Inc. plans a counterproposal for the August Jedec meeting that would have the 40.2 committee support the current pinout and call for circuit design to ease noise problems. *–J. R. L.*

for marketing and sales in New England. The year-old FACT (for Fairchild Advanced CMOS Technology) family, which uses the standard pinouts, now has 35 part types, and Fairchild plans to have 100 in production by year end. The company claims more than 250 design wins. Widespread adoption of a new pinout would scrub those early market victories, and it would take about three months per part type to alter FACT layouts to bring ground and Vcc pins to the middle of the package.

"One major computer company told me they are concerned about the cost of a change because their computer-aided-design system is set up for the standard pinouts," says Becker.

TI contends that customers with little experience with fast bipolar logic are the most apprehensive. "The people that have designed with Advanced Schottky, Advanced Low-power Schottky, and Fairchild's FAST bipolar chips understand the noise issue, and when you show them the magnitude of the problem caused by CMOS's rail-to-rail switching, they agree this [change] is the solution," says Dwain Chaffin, TI vice president in charge of standard logic.

Signetics' Frank Schneider, vice president and general manager of the Standard Products Division, says the noise issue was initially raised by customers using FAST, which Signetics second-sources. "There have been customers beating the heck out of us over FAST once they tried to switch six outputs and hold two steady. Ground bounced all over the place," he says. "TI was finding the same response with AS and ALS. The good, solid technical systems guy is going to say, 'You guys finally listened to us.' "

Charles Hunt, senior principal engineer at Compugraphic Corp., Wilmington, Mass., agrees. "I've gone through all the pitches, and the only one that has responded to the noise issue is the TI proposal. Until TI comes on line, I don't consider advanced CMOS logic viable for Compugraphic."

At Prime Computer Inc. in Natick, Mass., Steve Albino, section manager in component engineering, believes the trouble of dealing with a new pinout is worth the price for speed and easier debugging of board layouts. But Fairchild says that of 1,000 customers receiving FACT parts, none has encountered a noise problem serious enough to curb use of the devices.

The TI-Signetics proposal is likely to get a chilly reception at the Jedec 40.2 committee. For one thing, RCA Corp.'s Richard Funk, manager of standard IC applications in Somerville, N.J., is chairman of the committee. He believes the pinout change is a result of a design flaw in TI and Signetics parts, a charge TI and Signetics deny. Funk says RCA has redesigned its octal parts to cut dv/dt levels at the corner pins.

Integrated Device Technology Inc., Santa Clara, Calif., is ready to make a counterproposal to the pinout change before the upcoming Jedec meeting, says Tom Kadlec, product marketing manager for logic. "We want to see everyone support the standard pinout and solve the noise problem with better designs and output structures," he states. *–J. Robert Lineback*

ENCRYPTION

CYPHER CHIP MAKES KEY DISTRIBUTION A SNAP

SUNNYVALE, CALIF.

A method of exchanging private encryption keys over public networks is moving into silicon. Cylink Inc., a Sunnyvale maker of encryption equipment, says the process makes key distribution far more secure than the data the keys unlock, and the chip makes the process much faster.

Cylink's chip supports two major algorithms for public key encryption—its own and the RSA algorithm marketed by RSA Data Security Inc. Both algorithms derive keys from the exponentiation of large prime numbers.

Public algorithms such as the Data Encryption Standard make it possible for independent parties to send and receive encrypted data. But before doing so, they have to agree on a key to decipher it. The classic method has been to send the key by courier, which is expensive, slow, and vulnerable to the classic countermove: bribing the courier. Moreover, the method is impractical in systems where keys are changed frequently.

Public key systems, in which a secret key is matched with a publicly distributed key, solve these problems. Users wishing to receive encrypted data distribute a public key related mathematically to a privately held key used in

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decrypting. This makes high-security key-transfer processes unnecessary.

RSA Data Security, Redwood City, Calif., marketed the first public key algorithm, developed by the company's founders at the Massachusetts Institute of Technology. It uses two large prime numbers to derive a modulus in which public and private keys are related. The algorithm's creators, Ronald Rivest, Adi Shamir, and Leonard Adleman, founded RSA to lease commercial rights from MIT. Stymied in a 1983 attempt to implement the RSA algorithm in 3-μm CMOS (the company it licensed failed), RSA turned to software this time. The firm's Mailsafe and Comsafe packages, introduced this spring, run under MS-DOS.

Cylink, however, has handcrafted a 1,024-cell, 150,000-transistor key-distribution processor in 2-μm CMOS. Its most immediate use will be in the company's own data-encryption boxes. However, any company making DES equipment may have a use for key management.

The hardware speeds up execution of both the RSA algorithm and Cylink's SEEK (for secure electronic exchange of keys) algorithm. The chip, Cylink says, can also encrypt entire messages at 6,500 b/s. As a key manager, it reduces handshaking time to less than a minute from the many minutes required by software-only systems.

Cylink's SEEK algorithm differs in some fundamental respects from RSA's. For example, where RSA uses two large primes, Cylink uses a function of one prime. But the two are enough alike that the bit-slice structure of the Cylink chip, the CY1024, allows it to be used with either algorithm. The companies are negotiating ways to offer an RSA license with Cylink's chip.

Like RSA, SEEK is essentially a method of doubly encrypting a message, once in a public key and once in a private key, by a method that is commutative—that is, it does not matter which key is applied first. SEEK's public key is derived by raising a known constant to a power equal to the secret key. The public key is equal to this exponential value in the modulus of a known 500-digit prime supplied by Cylink.

TOUGH NUT. Cracking the private key therefore entails finding the discrete logarithm of the secret encryption exponent, a process Cylink founder Jim Omura says is "several orders of magnitude" harder than cracking a message coded in the 512-bit DES algorithm. The RSA method results in a key that would take between 10 years and several million years of brute-force calculation on a supercomputer to decipher, adds RSA marketing vice president James Bidzos.

Introduction of the key-management chip comes as end-to-end data encryption is beginning to break into the mainstream of data communications. Most encryption is now performed between major nodes in a network, with security being a matter of physical locks and keys. But with the proliferation of networks and personal computers, individual keys become necessary for each user, says Omura.

OMURA: Cylink's founder has embedded his SEEK algorithm in silicon.

SEEK is already under license to several large users, including a telecommunications utility, an aerospace firm, and a federal agency. This week, RSA will announce an agreement with Lotus Development Corp. to include its technology in future Lotus products.

"The real applications of key management are not in security. They are in office automation," says Bidzos. He's referring to the RSA algorithm's ability not only to encrypt data, but to append a digital signature that verifies the source and integrity of the data. Frequently, Bidzos says, users are less concerned with someone seeing their data than with making sure it's authentic.

Secure as they may appear, the RSA and SEEK algorithms will still have to win user acceptance, says consultant Donn Parker of SRI International, Menlo Park, Calif. Any private system will have to win the same kind of acceptance that the National Bureau of Standards has obtained for the DES.

"The purchaser has to get the feeling that the company providing the algorithm is legitimate, and that there is no Trojan horse in it," Parker says. "DES became so popular because IBM and the NSA put 17 man-years into trying to break it, and couldn't. So confidence in DES has built up."

Omura says the Cylink chip, fabricated at VLSI Technology Inc., will be shipping by September. No price is set, but it will eventually sell for about $100 in volume. *–Clifford Barney*

TELECOMMUNICATIONS

FCC STALLS SATELLITE MOBILE RADIO SERVICE

WASHINGTON

It's back to square one for the 12 companies competing for the right to operate a potentially lucrative land Mobile Satellite Service, now that the Federal Communications Commission has decided against allotting to the MSS any of the heavily used 800-MHz ultrahigh-frequency band. The FCC assigned the service instead to the less-desirable L band and allotted the available uhf frequencies to metropolitan public-safety agencies, which have lobbied strongly for them.

The decision bitterly disappointed the 12 potential MSS operators. It lays the groundwork for "a horrendous political battle," says Michael L. Exner, president of Skylink Corp., one of the contenders. "It will undoubtedly delay the implementation of an MSS satellite." The FCC move also will raise international hackles, especially since the commission upset its own 1982 agreement with Canada to establish the MSS in the 800-MHz band.

An MSS would provide communications capability for public-safety and private customers operating outside metropolitan areas served by ground-based two-way and cellular radio services. It could eventually represent a $1 billion annual market for the system operator. There is also money to be made by vendors that will sell equipment to support the service.

In its controversial July 24 decision, the FCC voted three to two to earmark 6 MHz of the uhf band in question for terrestrial two-way radios for public safety agencies—police and fire departments and ambulance services. MSS was kicked up into a section of the less-crowded L band, which had already been allocated internationally for use by Aeronautical Mobile Satellite Service.

The FCC decision represents a victory for public-safety forces led by Associated Public-Safety Communications Officers Inc. (APCO), New Smyrna Beach, Fla. With support from Motorola Inc., the world's largest manufacturer of two-way radios, the group had lobbied to get 800-MHz frequencies adjacent to

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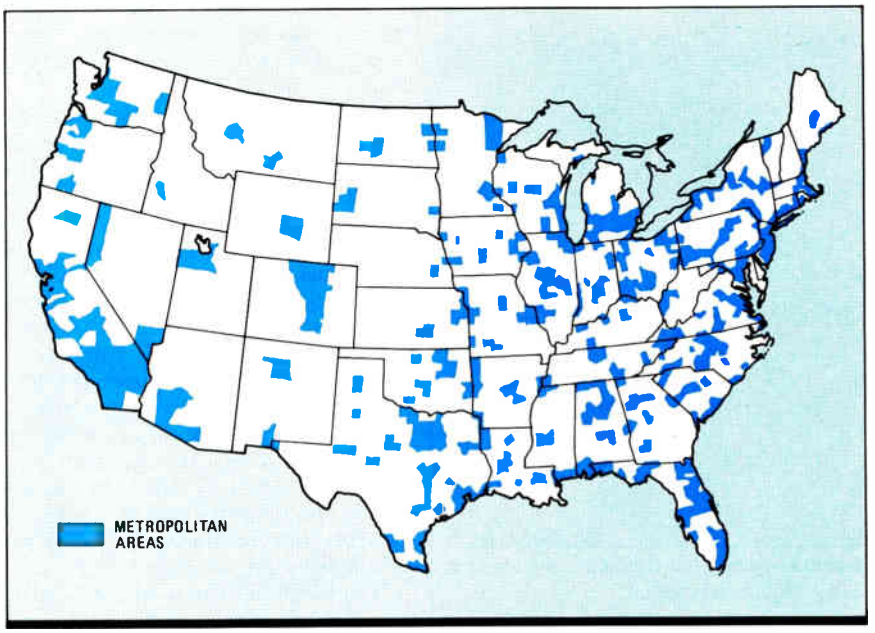

RURAL SERVICE. An FCC decision will delay satellite mobile-radio services for the 25% of the U. S. population outside metropolitan areas, which already have other services available.

existing public-safety channels.

"We are currently out of 800-MHz frequency in 11 major metropolitan areas," says APCO executive director Robert E. Tall. Public-safety agencies need the adjacent bands to add channels without buying new radio gear, he says.

For the MSS applicants, however, the implications of the FCC ruling are mixed. The positive side is that, although the 800-MHz band went to terrestrial public-safety uses, the FCC did find slots totaling 27 MHz for MSS in the L band. But the decision has a negative note for MSS, too: it is likely to raise the cost of providing MSS services and delay their launch further until international issues are resolved.

Only one of the 12 applicants had proposed operating exclusively in the L band. Most had proposed operating at both L and uhf bands.

The FCC decision will be costly, says Skylink's Exner. The Boulder, Colo., company had proposed combined uhf and L band service. "We estimate that $50 million has been spent in the U. S. and Canada in developing the plans and technology for this service in uhf."

DISMAY UP NORTH. The decision also makes officials unhappy in Canada, which wants to launch a uhf/L-band MSS service. This would be in line with agreements reached at the 1979 World Administrative Radio Conference, under which portions of the 800-MHz band can be used for MSS at the negotiated discretion of cooperating governments.

Although the FCC has no authority over Canada, the country needs U. S. cooperation to avoid interference, points out Glyn Berry, first secretary of the Canadian Embassy in Washington. Furthermore, if both countries put MSS in the 800-MHz band, Berry says, each country's system operator could use the other's satellite for a backup, eliminating the need for a costly spare.

In 1982, the U. S. and Canada agreed to coordinate MSS establishment in the 800-MHz band. The proposal for rulemaking that the FCC issued in January 1985 proposed to set aside 8 MHz near 800 MHz. Last month's FCC decision was an about-face. But "out of comity to Canada," the commission did place 4 MHz in reserve pending the outcome of negotiations set to begin soon with Canada. The Canadians are expected to press for 8 MHz for MSS, 4 MHz for each country.

The FCC decision also raises other issues because the International Telecommunications Union has pegged those L-band frequencies for the Aeronautical Mobile Satellite Service. The FCC now says that of the 28 MHz available in the L band, AMSS and MSS will share 18 MHz on a coprimary basis, meaning the two operators must work out equitable sharing. In another 9 MHz, AMSS operation will be primary and MSS secondary. The remaining 1 MHz will be for AMSS only. The idea may allow AMSS and MSS to share the same satellite, says Julius P. Knapp, chief of the FCC's frequency-allocation branch.

But efforts to promote L-band frequency sharing between AMSS and MSS face tough opposition. The international avionics community believes that by 2010, it will need all of the 28 MHz now allocated and probably more, says Siegbert B. Poritzky, director of systems studies and cooperative programs at the Federal Aviation Administration.

Consequently, the International Civil Aviation Organization, a standards-setting body, is firmly opposed to sharing L-band frequencies with MSS, Poritzky says. The U. S. could pursue the matter of AMSS/MSS frequency sharing at a World Administrative Radio Conference scheduled for 1987, says the FCC's Knapp. Or the U. S. could authorize use of the L band for MSS "in derogation of the [international spectrum-assignment] tables"—but only if Canada agrees to the move. *–Wesley R. Iversen*

IMAGING

OPTICS OPEN UP ROLES FOR ASSOCIATIVE MEMORY

LOS ANGELES

Enter just a fragment of an image into a new associative memory from GM/Hughes Electronics Corp., and it can return the complete image as its output. That's the most dramatic proof of associative memory's potential for a practical payoff, being brought to life by an all-optical approach eliminating any need for complex digital circuitry.

As an intriguing prospect in parallel processing, the associative-memory approach has for years attracted some research attention with few practical results. But associative memory based on emerging neural-network theory aimed at replicating the human brain's workings, might operate with less-than-precise instructions, opening up new possibilities in computer techniques—the memory processes data as well as storing it.

Besides optical memory's roles in pattern recognition, image manipulation, and robotic vision, it could be used in a "hetero-associative" memory, which would employ neural-networking techniques and would have the capacity for learning.

The new setup uses a holographically stored image as the data base, as did some earlier experiments, but adds what are called phase-conjugate mirrors. These devices go on each side of the hologram to form a resonator cavity that provides a nonlinear interaction with the stored images, producing feedback, a thresholding function, and gain. The memory thus obtains properties it needs to become—with further work—a stable processing mechanism.

A bevy of research teams has been racing to build a working prototype of

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Printing speed	80 characters/sec.	
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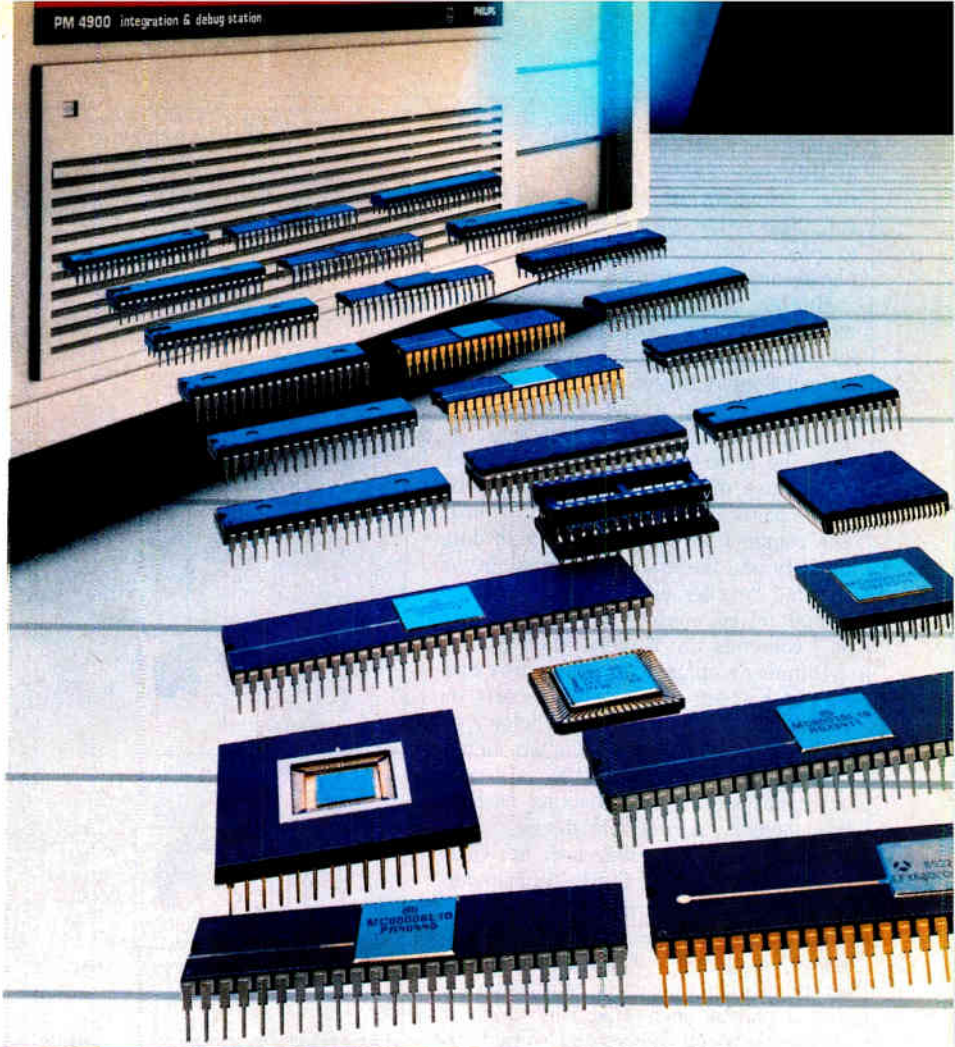

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such a memory, but the first to reveal findings, earlier this year, was a group at Hughes's Malibu Research Laboratories. Scientists at the GM subsidiary call their prototype an associative holographic memory with feedback using phase-conjugate mirrors.

Hughes technical staff member Gilmore J. Dunning says of the new develoment, "It's a big plus. You do not need an exact input to get an exact output."

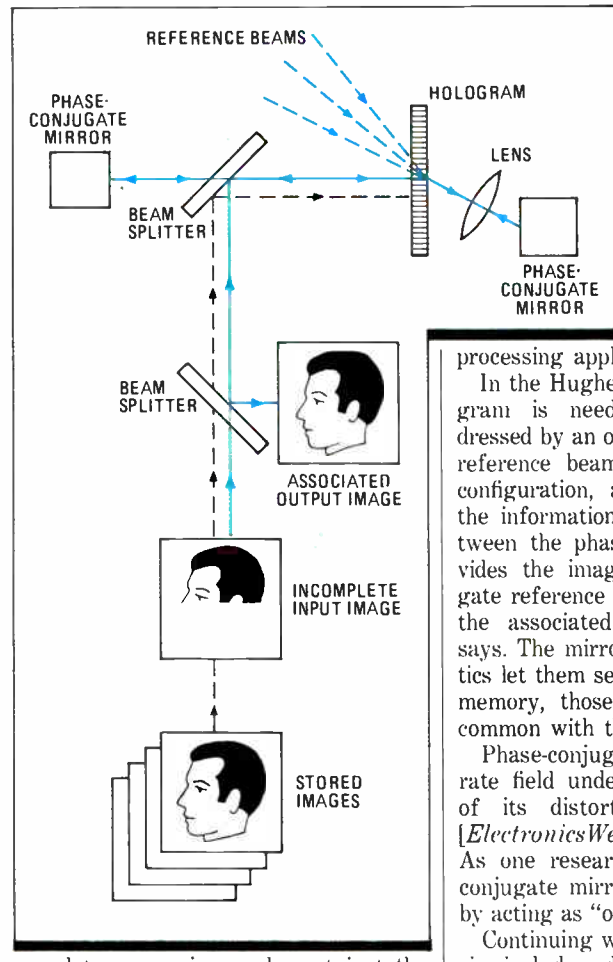
The prototype works by identifying data through general associations, as does the brain. Moreover, the approach makes use of massive parallelism—the entire picture field is processed at once. The combination of that very high data capacity and the associative capability is creating "excitement in the [optical and computer] community for what it can do," contends the Hughes scientist.

Dunning's opinions are shared by Sze-Keung Kwong, a scientist formerly on a California Institute of Technology team that demonstrated a similar memory. "Using phase conjugation is a very important step toward making associative memory a practical device," says Kwong, now a researcher at Ortel Corp., an Alhambra, Calif., semiconductor laser manufacturer.

Caltech is a center for advanced research on optical and neural networking techniques, as well as on silicon devices that replicate such functions. John J. Hopfield's widely recognized work there on neural-network modeling, though noted more for applying biocomputing techniques to silicon circuits, also provides the conceptual underpinnings for optical associative memory.

Observers point out, however, that calling the prototype a memory is overly limiting, and something of a misnomer. Its operation actually encompasses a complete processing cycle, not just the fetching of stored data.

The Hughes associative memory project, under way for nearly two years and supported largely by internal funding, draws heavily on Hopfield's findings of the early 1980s. His models, which employ globally distributed and interconnected memory elements, have self-organizing properties that lend themselves well to optical processing applications, Dunning says.



FROM FRAGMENT. Given a partial image as input, associative optical memory from GM/Hughes Malibu Research Laboratories uses a feedback process to retrieve a complete image from those it has stored holographically.

In the Hughes memory, only one hologram is needed, simultaneously addressed by an object beam and conjugate reference beam (see diagram). In this configuration, a fixed hologram stores the information, and the interaction between the phase-conjugate mirrors provides the image feedback. "The conjugate reference beam is key to unlocking the associated information," Dunning says. The mirrors' threshold characteristics let them select, from features in the memory, those that have the most in common with the input image.

Phase-conjugate optics is itself a separate field under intense study because of its distortion-correcting potential [*ElectronicsWeek*, Feb. 18, 1985, p. 33]. As one researcher puts it, the phase-conjugate mirrors derive their features by acting as "optical analog computers."

Continuing work on the optical memories includes adding more storage capacity for such tasks as handling three-dimensional objects and finding ways to gain a greater degree of control so real-time recording can be achieved by modification of the stored image. These improvements would make it possible to demonstrate a host of optical applications, says Dunning. *–Larry Waller*

TELEPHONY

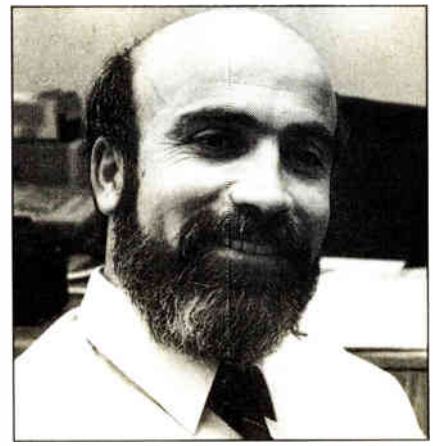
QUALITY SPEECH RIDES 8-KB/S CHANNEL

WALTHAM, MASS.

GTE Laboratories has found a way to cram more high-quality speech into a standard telephone channel than anyone else so far. Researchers at the Waltham labs have developed a system for multichannel communications that provides real-time voice compression using only about 8 kb/s of bandwidth.

In a simpler configuration, the system transmits toll-call-quality speech at 16 kb/s. The work, GTE Corp. says, holds the potential to code and compress four or more voice channels into the space of a single channel without significant degradation and at low cost.

At the Institute of Electrical and Electronics Engineers' Montech conference in Montreal next month, GTE will report that by combining a coding algorithm based on an adaptive subband excited transform (ASET) and time-domain harmonic scaling (TDHS), it achieved high-quality speech compression at 8.5 kb/s. The work builds on results announced in April using the ASET algorithm alone. With it, GTE obtained speech quality in a 16-kb/s compression comparable to that of the 32-kb/s algorithm accepted two years ago as the international standard.



SMALL TALK. GTE's Baruch Mazor foresees VLSI chip sets for speech compression.

Acknowledging that the world of speech compression has been crowded with claims of high quality despite disappointing performance, GTE emphasizes that the quality of its system has been verified by formal testing.

The fundamental obstacle to develop-

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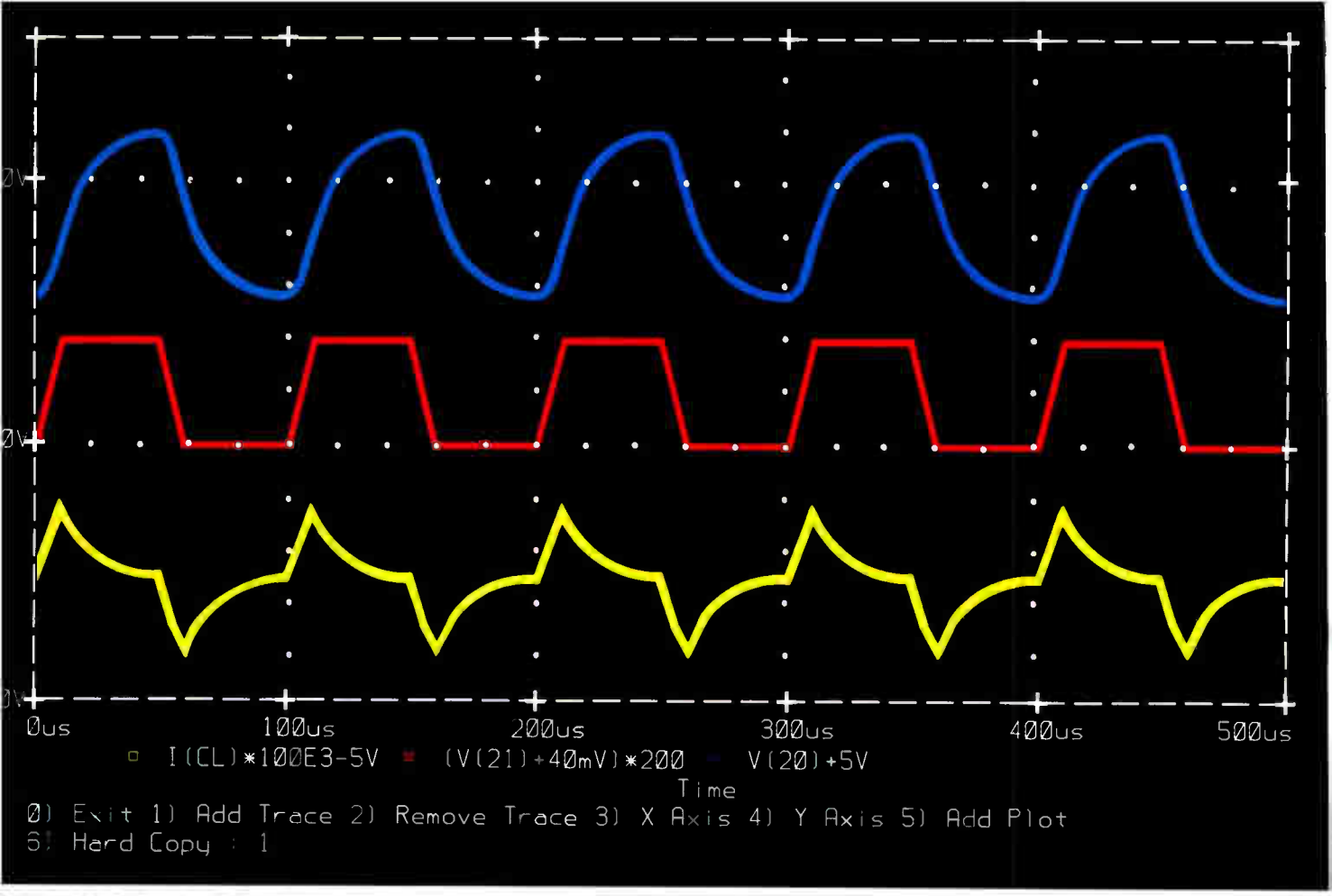

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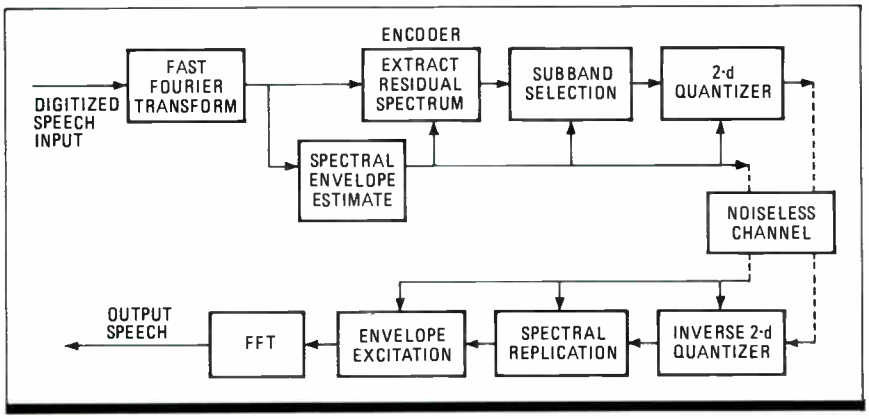

WORD CRUNCHER. GTE Laboratories is using its adaptive subbands excited-transform coding algorithm to push high-quality speech compression down near the 8-kb/s level.

ment of a high-quality ASET algorithm was finding a satisfactory way to reduce framing noise, or discontinuity along the edges of the coded speech samples. Earlier approaches have concentrated on improved coding within each frame to minimize this noise. "But that brings the rate up and increases the complexity," says Baruch Mazor, a principal member of GTE's technical staff who worked with fellow staffer Dale Veeneman on the two-year project.

Instead, GTE used a coding approach that "is not the finest possible," Mazor says, and focused efforts on smoothing the transition between coding frames in the transform-based coder. The smoothing involved one conventional technique—the overlap of neighboring frames. Here, GTE used trapezoidal rather than square windows.

GTE developed a post-coding speech-enhancement feature. Mazor explains that this feature, for which GTE is pursuing a patent, exploits redundancy in speech as well as how and when noise is produced. GTE also developed hardware tailored to the new algorithm.

For the 8.5-kb/s compression work, GTE used the ASET algorithm and added pre- and postprocessing TDHS (see figure). Optimizing the perceived quality of speech with TDHS is heavily dependent on the choices of periodicity detection, says Mazor. GTE settled on an average-magnitude-difference function because it was found to be superior in reducing reverberance.

PIPELINED. The basic hardware for the systems is a multichannel codec partitioned into six blocks. A dedicated processor is assigned to each function. Each processor has a computational unit and a memory unit. They are connected in pipelines to form a distributed processing system with each processor having access to two fully independent data bases. Maximum delay is about 45 ms, with an average of 22.5 ms.

"The algorithm is such that someone could implement it on a set of very large-scale integrated circuits," Mazor says. Short of VLSI, GTE estimates that the use of commercial digital signal-processing chips would lower the system's per-channel cost below $50.

To get as objective as possible a reading on quality, the lab administered a formal phonetically balanced test to 66 people. The average score for standard 64-kb/s speech was 4.36. The result obtained for GTE's 16-kb/s compression algorithm was 3.9, comparable to results obtained elsewhere for the 32-kb/s standard. GTE's combined ASET-TDHS method for 8.5 kb/s scored about 2.9.

Similar laboratory results have been reported by others in the past, according to both Paul Mermelstein, manager of man-machine communications at Bell Northern Research Ltd., Montreal, and David Wong, director of signal processing at Digital Sound Corp., Santa Barbara, Calif. Such high-quality performance has not been demonstrated outside the laboratory, however.

Mazor emphasizes that GTE's testing has been rigorous, its results have been reported on fully encoded speech, and compromises for implementation have already been made. Furthermore, Mazor says, "we consider the complexity of our algorithms to be medium to low." Field tests are to begin later this year.

Questions of quality aside, Wong feels GTE could make an important contribution to the technology's economics. GTE could bring costs down "because if they do it, they would do it in large volume." *–Craig D. Rose*

PHOTOVOLTAICS

A BETTER WAY TO BUILD EFFICIENT SOLAR CELLS

ERLANGEN, WEST GERMANY

A new breed of photovoltaic cell makes a quantum leap in conversion efficiency and promises a drastic improvement in price-per-watt performance. Using inexpensive polycrystalline silicon as its base material, the cell is about 14% efficient—some 4% better than conventional polysilicon solar cells.

Solar cells are available with even higher efficiencies—some exceeding 20%—but they cost more to make than the one developed at the University of Erlangen-Nürnberg. Using gallium arsenide or other costly materials, competitive cells generally require elaborate fabrication processes or employ expensive collectors that track the sun.

The Erlangen device, by contrast, not only uses cheaper materials, but relies on inexpensive fabrication techniques. Its fabrication foregoes high-temperature processing and uses "simple, not to say primitive, production methods," says professor Rudolf Hezel, head of the cell development team at the university's Institute for Materials Research.

The cell consists of a 1.5-nm layer of silicon dioxide grown onto a p-doped silicon substrate, onto which a grid of aluminum contacts is deposited. An aluminum back contact covers the cell's entire bottom. The key step is the plasma chemical-vapor deposition of an 80-nm-thick silicon nitride film. A mechanical mask, rather than an expensive photolithographic mask, is used to create the metal contacts, which at just 8 μm wide permit current densities as high as 35 mA/cm^2.

KEEPING COOL. In ordinary solar cells, temperatures of more than 800°C are required for a diffusion process that takes over an hour to make the p-n junction. Moreover, if ion implantation is used with a conventional cell, a high-temperature step is again required—this time to activate the dopants and to anneal damage that ion bombardment causes to the crystal lattice. These processes ultimately have a negative effect on the cell's efficiency.

Thanks to its silicon nitride film, the new cell requires no such steps. For operation, the film must have a high concentration of positive charges at its bottom—the side facing the substrate. These charges set up a depletion region in the substrate as well as a region with a high electron concentration near the substrate surface.

To achieve the high concentration of positive charges, the researchers dip the cell into a solution containing cesium. The region with the high electron concentration, about 10 to 50 nm thick,

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forms an induced p-n junction.

This region changes, or inverts, the cell's type of conduction—say, from hole to electron conduction—hence it is called the inversion layer. The positive cesium ions greatly increase electron density in the inversion layer, thereby enhancing the layer's conductivity.

The nitride film also protects the delicate silicon surface and the metal contacts from corrosion, contamination, and scratches. Moreover, the film retards reflection, ensuring that as much light as possible reaches the silicon. A textured pyramid surface collects scattered light and further cuts down reflection.

Light penetrating the cell between the contacts produces hole-electron pairs, which are separated by the depletion region's electric field. The holes diffuse toward the back contact while the electrons travel through the high-conductivity inversion layer to the contacts above. Current then flows through the external circuit, its strength depending on the light's intensity.

Continuing development work on the silicon-nitride inversion-layer cell could lead to polysilicon versions with efficiencies up to 17% and single-crystalline types with 19% efficiencies. But squeezing such performance out of the devices "will be an arduous job, one that may take another three years or so," Hezel says. His group has already achieved roughly 16% efficiency out of the more expensive single-crystalline silicon. The maximum efficiency of a silicon-based solar cell that does not use a focusing scheme that tracks the sun, he says, is about 25% at air-mass 1 conditions, that is, when the sun is directly overhead.

With the Erlangen device not yet in production, Hezel cannot say just what the price/watt performance will be. But he thinks the cell's cost will eventually be half that of conventional devices.

The silicon nitride inversion-layer cell is a result of years of semiconductor materials research. Since 1979, Hezel has applied the expertise he gained as an integrated circuit researcher in U. S. and West German laboratories to the project. But it has only been in the past year or so that Hezel and his team of 12 students and doctoral candidates have made significant breakthroughs.

Although their performance can still be improved, present cells are advanced enough to go into volume production, he says, and at least two native companies are interested in fabricating them. The first pilot production line could go into service as early as 1987. *–John Gosch*

AVIONICS

COMPUTERS SAVE WEIGHT IN FLY-BY-WIRE AIRLINER

VILLACOUBLAY, FRANCE

One of France's principal manufacturers of avionics equipment has begun deliveries of an advanced flight-computer system for what's said to be the first commercial airliner in production that relies on a fly-by-wire system. In such a system, electronic signals replace the mechanical components by which a pilot usually manipulates a plane's rudder, ailerons, and other control surfaces.

The computer system is for the Airbus Industrie A320, Europe's newest entry in the airliner market, which is scheduled to make its first test flights next March. The computer system has been developed by a consortium of avionics manufacturers led by Sfena (the Société Française d'Equipement pour la Navigation Aérienne) in Villacoublay. Despite the added functions it has taken on, the system will have just half the volume and weight of computers developed for earlier Airbus models.

Sfena will supply the plane's flight-management guidance system in addition to two flight-augmentation computers, three spoiler and elevator computers, a computer and four accelerometers for wing-load distribution, and a centralized fault-display system. Other computer systems will be supplied by Sperry Corp. and France's Thomson-CSF.

NO YOKE. The control yoke pilots use in mechanically flown planes will be missing in the fly-by-wire cockpit of the French plane. It will be replaced by small joystick controllers placed to the left and right of the pilot's and copilot's respective seats.

Like the fly-by-wire system, the A320's flight-management guidance system boasts increased processing power that has added features. The system integrates a centralized fault-display interface unit that lets analytical programs

U. S. PLANE MAKERS EDGE CAUTIOUSLY TOWARD FLY-BY-WIRE SYSTEMS

While Europeans are taking a bold step in commercial aviation by going to a comprehensive fly-by-wire system on the A320 airliner from Airbus Industrie, their competitors on the other side of the Atlantic are calmly sticking to their own schedules. Boeing Co. and the Douglas Aircraft Co., subsidiary of McDonnell Douglas Corp., say fly-by-wire is the next step for commercial aviation, but neither plans to launch a plane with fly-by-wire systems as extensive as the A320's before 1990.

The two companies are quick to point out, though, that fly-by-wire technology is being used for some isolated functions in commercial and military planes. The Boeing 757 has electronic fuel controls, for example. More functions will be turned over to the technology as new planes come out.

"We are studying fly-by-wire systems coupled with a backup fiber-optic cable system for the 7J7," a Boeing commercial jet that's due for production starting in 1992, says a spokesman for the Seattle company. "No final decisions have been made, but we expect that the 7J7 will be virtually a fly-by-wire plane, with a much more extensive system than the A320."

Douglas Aircraft's name for its fly-by-wire technology is full-authority digital electronic control, or Fadec. Douglas is using Fadec for engine control on the MD-11, a wide-cabin plane the Long Beach, Calif., company plans to have out by late 1989, says Elaine Bendel, manager for commercial programs. "It would not be cost-effective for our company to use full fly-by-wire on the MD-11 because the plane is built on the success of the DC-10's mechanical design. When we start designing a plane from scratch, fly-by-wire will be considered."

Douglas uses some fly-by-wire functions for such projects as the KC-10 military tanker, but not for commercial aircraft. "In commercial aviation, reliability is most important. An airline can't afford to keep a plane on the ground," says Bendel. For this reason, Douglas is interested in developing a fly-by-wire system with a mechanical backup system, something the A320 does not have.

One potentially troublesome detail of the full fly-by-wire system Airbus has designed, believes Douglas's Bendel, is the joystick that replaces the standard yoke steering control in the cockpit. He questions whether pilots will accept the joystick: "The yoke is universally accepted as the standard, and eventually you must cater to the comfort of the pilot in the cockpit."

Boeing's Wheeler also questions the acceptability of fly-by-wire joystick controls—but not of fly-by-wire systems for the rest of the plane's functions. "When Boeing does switch to fly-by-wire, we will probably stay with the yoke control," he says. "Industry pilots just don't like using a stick, but they do like fly-by-wire technology for the rest of the plane." *–David Rubinger*

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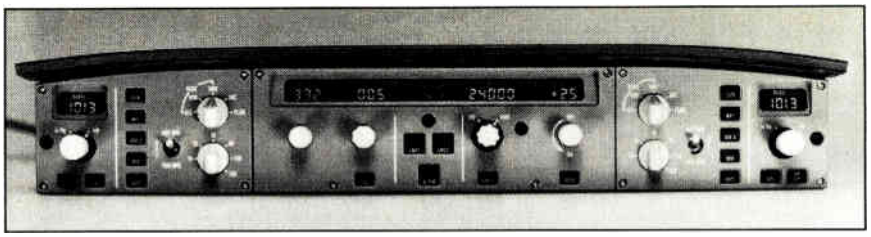
isolate faults and specify which unit must be replaced. Toulouse-based Airbus Industrie will, in future models, extend this feature to all of the plane's subsystems.

In its work for the A310 Airbus, Sfena was one of the first to supply a fully digital flight computer and, with work begun in 1979, was among the first to develop one based on 16-bit microprocessors.

The dramatic increase in the computer system's functionality and the simultaneous decrease in its weight and volume are a result of the spare processing power available when using new-generation components to do the jobs computers were assigned in the A310, says Daniel Gruaz, Sfena's manager for A320 flight systems. The systems for the earlier plane were based on Intel Corp.'s 8086 microprocessor, whereas the A320's computers rely on the Intel 80286 and 80287 floating-point coprocessor.



CONTROL. Airbus A320 pilots will interact with the plane's computers via a digital panel.

The weight and volume savings are particularly important for the A320, a 150-passenger plane designed to compete with the aging Boeing 727 and 737 and the McDonnell Douglas DC-9. Gruaz reckons that between the weight savings in the computers themselves and the elimination of cables and hydraulic servos, the A320 will be able to add "several passengers" to its payload.

To add flexibility, Sfena has developed an exchangeable cassette-like memory module featuring erasable programmable read-only memories. Software is being written with the aid of two tools produced in-house: Palas, a software-configuration control program that permits software to be developed and modified in a high-security environment, and Gala, a system for automatic management of code based on control laws expressed in graphic form to speed debugging. *–Robert T. Gallagher*

IC PRODUCTION

JAPAN KICKS OFF X-RAY FAB PROJECT

TOKYO

Just as the University of Wisconsin ring promised to even the international race to develop practical high-energy synchrotron-based X-ray lithography for very large-scale integrated circuits, Japan has tilted the odds again. A government-sponsored joint-venture company, K. K. Sortec, was set up in early June to build a synchrotron center for use by 13 member companies from the nation's electronics industry.

In designing and building its ring, Sortec will use all technology available in Japan, including that of the Ministry of International Trade and Industry's Electrotechnical Lab. But unlike MITI's lab, which is developing compact rings suited to production use, Sortec aims to build a larger ring quickly so its members can acquire expertise in the use of synchrotron radiation technology. Sortec's ring will be similar in size to those found in other research facilities but not so big as the Wisconsin ring, which is about 90 meters in circumference [*Electronics*, June 23, 1986, p. 19]

PROTEIN ANALYSIS. VLSI lithography technology and device fabrication will be a major part of the effort, but the Sortec ring will also be used for protein-structure analysis and other, unspecified applications. One possible area of study is the enzyme proteins needed to fabricate biochips.

The government will provide about 70% of Sortec's capitalization. The rest will come from the member firms—Canon, Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC, Nikon, Oki Electric, Sanyo, Sharp, Sony, Sumitomo, and Toshiba. The equity participation of the companies will be unequal; for example, Canon and Nikon will contribute somewhat less than the semiconductor manufacturers.

The joint venture will buy land for the center near Japan's science city, Tsukuba. That location was selected because it's near Tokyo—about 70 km northeast—yet far enough away that land is affordable. Moreover, those involved believe environmental-impact approval will be easier to obtain there than elsewhere—Tsukuba already plays host to one synchrotron, and others are scheduled to be installed [*Electronics*, March 17, 1986, p. 46]. At other locations, public concern about the possibility of exposure to ionizing radiation could provoke delays.

Thirteen companies join government in X-ray lithography effort

The government will support Sortec for no more than 10 years. But long before that, the members should get results that will help them make plans for the future, because Sortec expects to have its ring in operation in three or four years. The companies need not return money invested by the government, but the agency that sponsors Sortec will get a 70% share of any patent royalties and trade-secret payments.

The initial idea of founding Sortec came from MITI. Actual planning for its establishment was done by a foundation set up for the purpose, the Research & Development Association for Future Electron Devices [*Electronics*, Sept. 8, 1983, p. 94].

Sortec now has a staff of 10, including president Tsunero Ushio, executive vice president of Mitsubishi Electric Corp. But the company is actually run by vice president Goro Tamura, former head of the Fukuoka Bureau of International Trade & Industry—one of eight regional bureaus that duplicate on a local level many of MITI's functions.

The government funds Sortec through the Japan Key Technology Center, which was founded in October 1985 to promote private-sector research and fundamental technologies needed for the 21st Century. Japan Key-TEC, as it is called, is in turn financed by dividends and investments from the government's shares in NTT, Japan Tobacco, Japan Development Bank, other government financial institutions, and private-sector investments. It can provide up to 70% of the capital of a company's research project, as well as loans; it can also make arrangements for joint research and execute contract research.

Japan Key-TEC's budget for the current fiscal year, which started April 1, is $132 million, of which $81 million is for investment, $37 million for loans, and the remainder for the fund. Last year's budget included about $1 million for Sortec, 70% of the firm's total capitalization of almost $1.4 million. This year Japan Key-TEC is contemplating once again contributing 70% of Sortec's total budget, which will have reached $4.5 million to $5 million. *–Charles L. Cohen*

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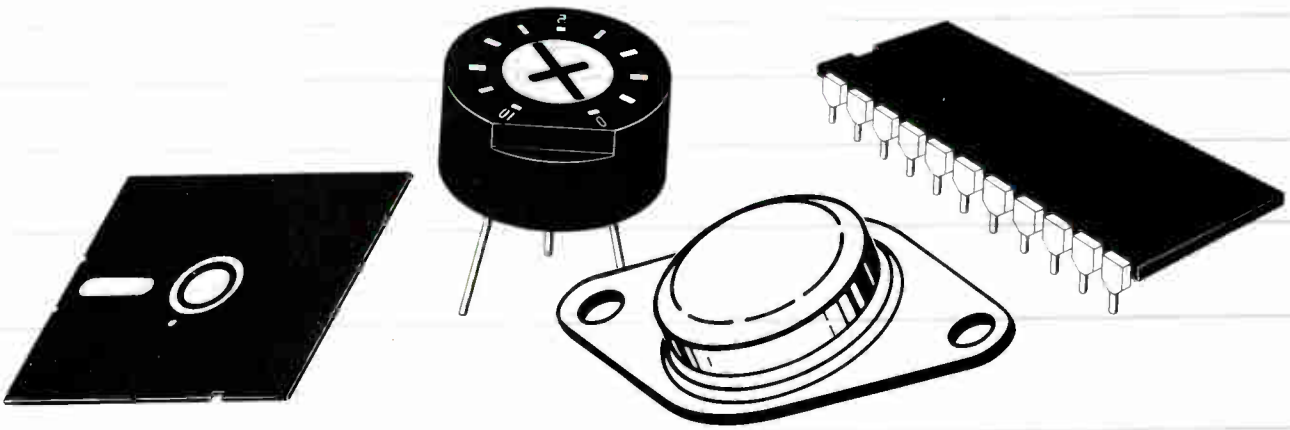

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Robots get Smart in Japan
ITT Invests in European Units Crack U.S.

February

Europe's Esprit Finally Sets Sail
LSI Logic Counts on Sandfort to make its Mark in Europe
Upstart Vendor Makes Waves in Japan's Robot Market
NEC Fashions New Fab Process
Olivetti's Viti Directs ET Designs that Marry Bus & Art
German Startup's Success Surprises Europeans
Britons Seek Tolerant Chips
OBI Rains on IBM's Parade
Mega's Friedrich Aims to Cut Asian Lead in Memories

March

British GaAs Chips Go to Market
NEC's CPU Leapfrogs IBM
Hitachi CPU Challenges IBM
France's Lansat Rival Set for Fall Launch
Olivetti Stakes Claim in Video Typewriters
Italian VLSI Chip has the Right Accent
Koreans Try for VCR Replay
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UK Beats a Path for Europe's Race

April

German System Meets New ICAO Standard
West Germans Squabble Over Choice of IFF
Britain Promotes Open Architecture
US Makes Progress in Japan Telecom Talks
Japan's Lead in Optical Disks: It's Part of the System
Daisenberger Guides US Firms through Red Tape
Asia: It's No Longer Just Japan That Threatens US Markets
Malaysia: Top Shipper of Discretes
Indonesia: Domestic Sales are the Lure

May

Thomson's VCR System Clears Up Doubts
ICL Banks on Networks and Japanese Chips
Min Blazes Bright Path for Korea's Gold Star
Asia: The Four Dragons Rush to Play Catch-up Game
Singapore Casts Lot with Software
Philips' Eurom Chip Finally Debuts
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June

Plessey Switches Off Flash ADC, Saves Power
Sony Campaigns Hard for BMM Camcorders
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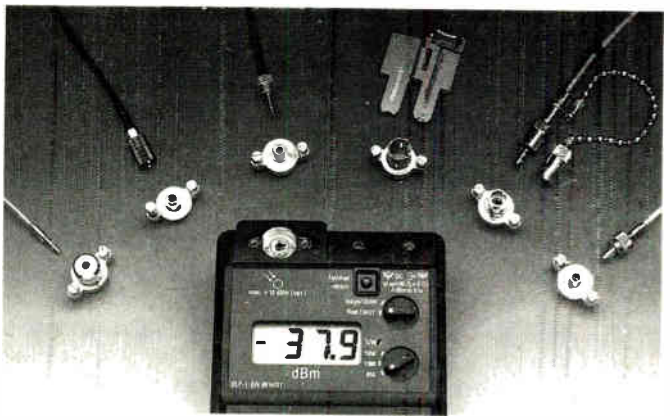

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INTERNATIONAL NEWSLETTER

FUJITSU EYES TV PRODUCTION IN CHINA

Battered by the soaring yen, Japan's Fujitsu General Ltd. is eyeing the People's Republic of China and its plentiful supply of cheap labor as a manufacturing base for consumer electronics and appliances to be exported to the U. S. and the Middle East. China is already manufacturing color TV sets and refrigerators for sale locally under license from the Fujitsu Ltd. subsidiary. Fujitsu General is negotiating with Chinese authorities to produce refrigerators for export by the end of the year, and it may try to strike a similar deal for color TVs. It is also poised to set up a production center in Hong Kong that will supply components to the Chinese plants. The consumer electrical and electronics company is controlled by Fujitsu Ltd., Tokyo, which two years ago bought a 21% stake, making it the largest shareholder, and changed the name from General Corp. in a bid to bolster its own small consumer electronics business. □

SIEMENS, THOMSON, AND ICL SET JOINT EFFORT IN VLSI CAD TOOLS

Three European equipment makers that usually compete with one another will work together to develop computer-aided-design tools for very large-scale integrated circuits having more than 1 million transistors. The three—West Germany's Siemens AG, France's Thomson Group, and International Computers Ltd. of the UK—have launched their $34 million, four-year Advanced Integrated-Circuit Design Aids (AIDA) project within the framework of Esprit, the European Strategic Program for Research in Information Technology. Siemens will be project leader and will develop layout and testing tools; Thomson will be responsible for developing silicon compilers and user interfaces; and ICL will coordinate system specifications and data-management tools for CAD gear. □

BUNDESPOST INSTALLS A FIBER-OPTIC ISDN TEST NET

West Germany's communications authority, the Bundespost, is planning to set up a 140-Mb/s broadband integrated-services digital network, even though the initial links of its first ISDN, a nationwide narrowband 64-kb/s net, won't be operating for at least another two years. As a step toward the broadband ISDN, the agency is installing a fiber-optic network in West Berlin to test various communication services on high-speed terminals at up to 40 private and public subscribers. The Berkom (the German acronym for Berlin Communication System) will cost around $45 million. Of that amount, $9 million is slated to support development of terminals at communications-equipment houses, which will match the Bundespost's funds. □

THOMSON AND FRENCH LAB TEAM FOR CCD DEVELOPMENT

Thomson-CSF has signed on a leading French government laboratory to strengthen its market position in charge-coupled devices. Working with the Atomic Energy Commissariat's Laboratoire d'Electronique et de Technologie de l'Informatique (LETI) in Grenoble, Thomson intends to shrink its current 2.5-μm n-MOS buried-channel technology to 1.5 μm within two years and to submicron line widths by 1990. LETI has substantial experience in fine-line lithography and is already cooperating with Thomson in development of advanced MOS ICs. Thomson is aiming for CCDs with higher resolution, better sensitivity, and faster signal-processing capabilities than its existing range. It expects to have the first fruits of its collaboration with LETI on the market in about 18 months. The French electronics heavyweight figures it can winnow out a 10% share at the high-end of the CCD business by 1990, when the world market should be running close to $1 billion. □

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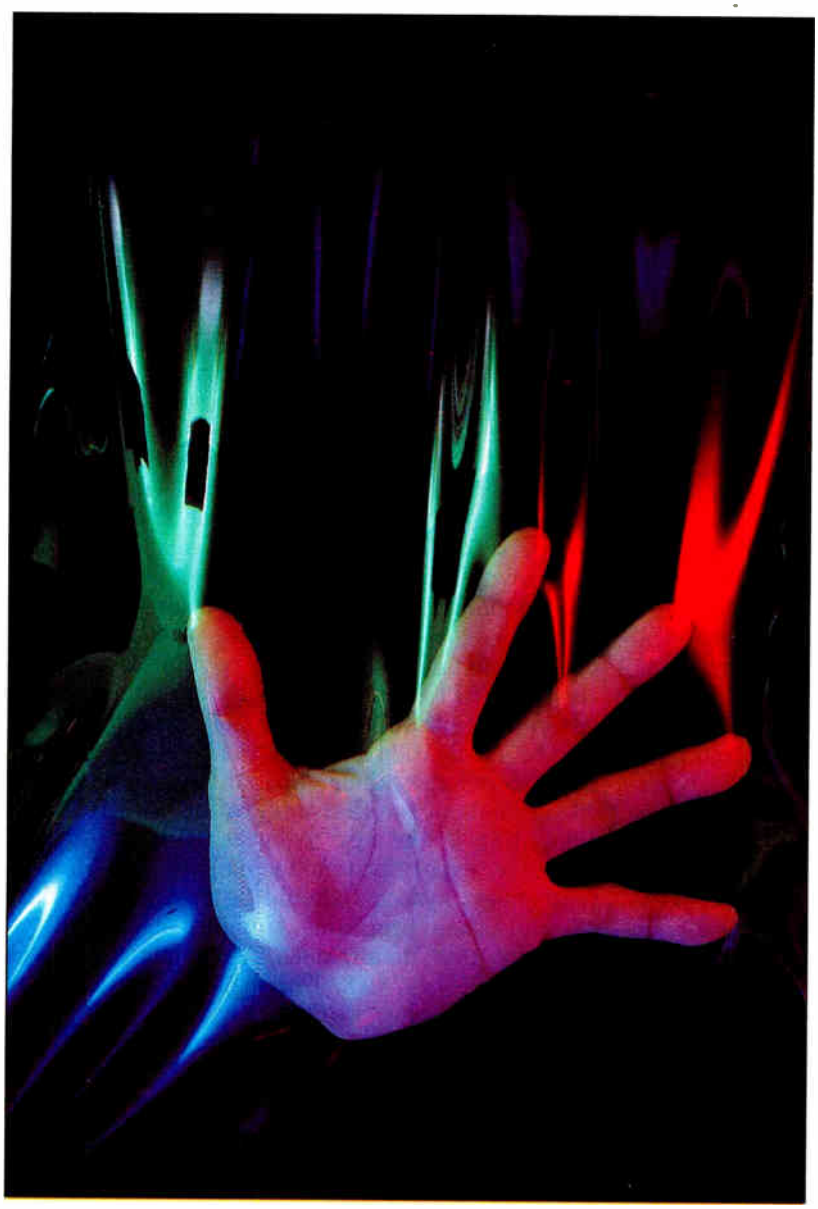
INSIDE TECHNOLOGY

WHAT'S HOLDING BACK EXPERT SYSTEMS?

by Tom Manuel



Expert systems should have started taking hold in the mainstream of computing by now—if they had lived up to the expectations voiced by many people a year or two ago. But the technology is not yet making its impact felt. It is not making any significant difference in the way that the bulk of commercial computing and data processing is done. The question is: why not?

Many proponents and vendors of expert-system technology

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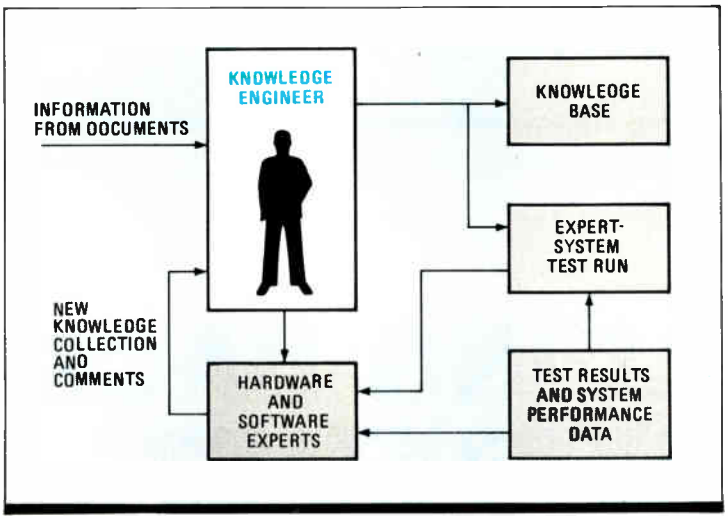

1. BUILDUP. A knowledge base is built by adding facts, testing the expert system, then adding more knowledge if necessary.

believe it is ready and waiting to hit the big time, but its entry into the mainstream is still just a trickle. Now, however, there are signs that the current is beginning to quicken.

It may have been naive last year to expect that expert systems would have started hitting the big time by now [*Electronics*, July 1, 1985, p. 54]. After all, the expert-system industry is in its infancy, and it is a new and very different technology that is somewhat difficult to grasp when first encountered. Expert-system technology has been held back primarily because it has, until now, required programmers and knowledge engineers with some experience in artificial intelligence and Lisp programming coupled with computers designed to run the popular AI language efficiently. To get expert systems moving, the technology must be made more accessible to mainstream computers and users.

Several companies concentrating on AI and commercial expert systems, as well as most of the major computer companies, are working on this problem. The expert-system startups see the need to assimilate their technology into the mainstream to become successful businesses. The computer companies, on the other hand, see expert-system technology eventually becoming a neccessary part of most, if not all, applications.

One important sign of the quickening pace is the migration of expert-system tools away from the Lisp AI language and Lisp machines.This shift is just beginning and heralds an acceleration of expert-system applications, especially in traditional management-information systems, according to many industry experts.

Expert systems are the focus of the many efforts to commercialize AI technology for the computing mainstream, which primarily means MIS computing. Commercial work in other AI subfields is progressing, especially in language recognition and understanding, also referred to as natural-language processing. But expert systems constitute by far the bulk of activity in the commercialization of AI.

The Gartner Group Inc. breaks down the 1986 market for expert-system tools and applications as $45 million and $12 million, respectively. The Stamford, Conn., market researcher forecasts that, by 1990, the market will jump to $275 million for tools and $350 million for expert systems.

But the promise of expert-system technology goes far beyond the market figures. Such systems are computer programs that solve problems the way a human expert in the field would solve them. Potentially, this is a very valuable function, since it is a way to capture, codify, and preserve the knowledge and skill of someone who is very good at a specific task.

An expert-system program uses a knowledge base—a large store of facts specific to the expertise—and a set of rules. Both are supplied by the human expert the system is being programmed to mimic (Fig. 1).

Once the expertise is secured in an expert system, another benefit is that it can be copied, distributed, and used in far-flung locations—a difficult feat to achieve with a human expert. Other benefits are that the computerized expert or adviser is always alert, is never under the weather or temperamental, can work 24 hours a day, seven days a week, and cannot accept a better offer from a business competitor.

PRODUCTIVITY WILL DRIVE AI

Best of all, expert systems promise to improve productivity significantly, says Joel Magid, senior product manager of Digital Equipment Corp.'s AI Technology Center in Hudson, Mass. "In the future perhaps, applications will have 30% AI content and 70% conventional MIS." The major computer companies don't want to rely entirely on third parties to provide the AI part of products that they sell, so they are developing their own AI capability.

To popularize expert systems, most of the development-tool vendors believe the technology must be available in today's popular languages, such as C, PL/1, and Cobol. By running on computers other than Lisp machines, expert systems can be easily tied to new and existing applications to enhance their capabilities.

All hands agree that integration with mainline computing is the key to successful applications based on expert-system technology. This means that expert systems should be easily made part of application programs running on computers such as IBM mainframes, superminicomputers such as the DEC VAX, Unix-based midrange systems, engineering work stations, and the high-performance personal computers that will soon show up.

Many proponents of expert systems and vendors of development tools, such as Alexander D. Jacobson, president of Inference Corp., and Lee Hecht, chairman, president, and chief executive

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officer of Teknowledge Inc., agree that expert-system and AI technologies can and must move away from Lisp (see p. 64). But others, such as Lucid Inc. president Richard P. Gabriel and IntelliCorp chairman and CEO Thomas P. Kehler, disagree and present valid arguments for continuing to use Lisp (see p. 65).

Both sides agree that most applications must run on the non-Lisp machines that mainstream MIS computing employs. Yet, in many instances, a good case can be made for employing a Lisp machine, either for software development, or as an embedded or attached symbolic-processing engine.

NON-LISP TOOLS NEEDED

Inference Corp. believes non-Lisp versions of expert-system development tools will be needed to drive the technology firmly into the mainstream computing world. To put its money where its mouth is, the Los Angeles company has just completed a C-language version of the ART (Automated Reasoning Tool) system, an integrated set of tools for developing large expert systems (see p. 66). The C version will debut next week at the National Conference on AI in Philadelphia.

Inference has been marketing automated reasoning for nearly two years now with its original version of ART for Lisp machines. Just last month, the company announced the third release of Lisp-ART, with enhanced features, as well as versions for conventional computers such as VAX superminicomputers and Sun Microsystems Inc. work stations [*Electronics*, July 24, 1986, p. 25].

The expert-system tool kit has matured very quickly. "Inference went on a functionality splurge in a very short, fast release cycle [with ART]—three versions released in less than 1½ years," says Jacobson. The first release was a packaging of the basic expert-system building technology developed by Inference into a commercially usable form.

The second release, ART 2.0, was designed to make it easier for expert-system makers to employ the technology. Inference also added tools to the integrated package. Now ART 3.0 introduces features to ease the deployment of production expert systems—an engineering release, as Jacobson calls it.

Another prominent expert-system tool company, Teknowledge of Palo Alto, also has made its development products, S.1 and M.1, available in C. Teknowledge's Hecht believes the maturing of building tools, along with their availability in C on many different computers, will speed up adoption of the technology. "This is the wave of the present. It's not going to take five years or more. Today's customers can apply our mainstream tools today to solve specific, real problems," he says.

Meanwhile, The Carnegie Group Inc. has announced that it is readying C versions of Knowledge Craft and Language Craft. "We are going both ways, as a hedge," says president Larry Geisel. He notes that although Lisp machines have made some inroads into the computer market, there is a much larger population of 32-bit work stations. So to broaden its market substantially, the Pittsburgh company will offer C-based versions of its tools, at least for the delivery of expert systems.

HECHT: In offering C-language versions of its expert-system building tools, Teknowledge Inc. is following "the wave of the present," says its chairman and chief executive.

Expert-system builders, and therefore the vendors of their tools, have two choices with respect to expert systems on work stations, Geisel says. "They can use Lisp-based tools and Common Lisp, which will be okay in the long run when these Lisps can really perform, or they can use C-based delivery vehicles.

"We are not writing off users of Lisp—some users will like Lisp and some will like C," Geisel says. Lisp-based tools may be desirable and probably see heavy use in prototyping and developing expert systems, but C-based delivery systems may hold the key to widespread deployment of completed production systems, he says.

One reason Lisp is not a good commercial tool is that it suffers performance problems at run time because of the overhead it generates, Inference's Jacobson says. "For expert systems to become commercial, they must be economical at run time." Because the C version of ART is a translation of ART-Lisp, Inference customers will be able to develop and deploy knowledge-based applications on both Lisp machines and conventional computers. Or they can develop expert systems on Lisp machines and deploy them on conventional machines, and then tie them into MIS applications and have them run with the same efficiencies as conventional software does, Jacobson says.

A broad expert-systems market won't appear until the applications can run on the non-Lisp machines that are familar to computer users, say most vendors

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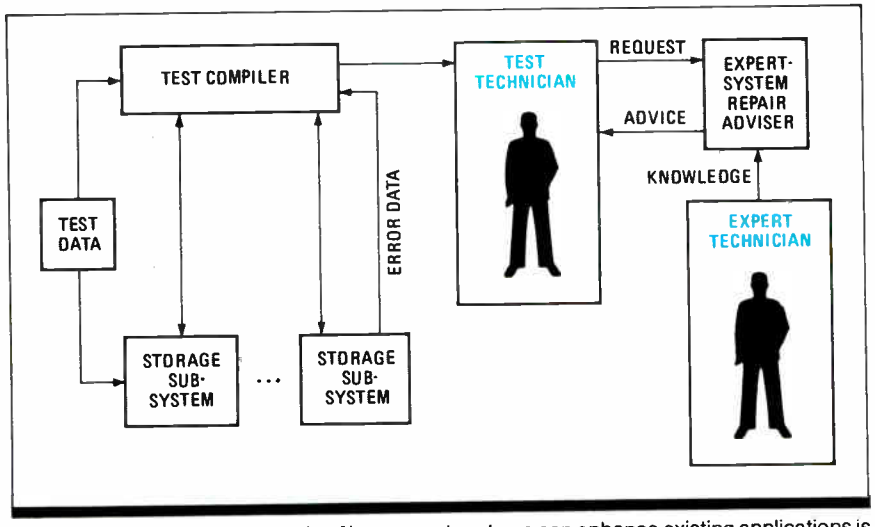

2. TIE-IN. An example of how expert systems can enhance existing applications is this repair adviser, which IBM has linked up to a storage-system test setup.

Whatever the attraction of C, Inference is not abandoning Lisp and its aficionados. "Lisp is an excellent development environment with its great power and flexibility," Jacobson is quick to say. However, that power and flexibility generates the overhead that slows performance at run time. "To commercialize AI, that overhead needs to be put behind us," says Jacobson. One way to do that, once development is done, is to port the application to a more efficient language for deployment. "That's what the C version of ART is all about," he adds.

The C version of ART is available now on work stations. The next step, Jacobson says, is to put it on mainframes. "There is a lot of interest in doing that; at Inference, IBM, and among MIS people, for example. It's time to get expert-system technology into the hands of corporate MIS," he says.

Seconding the motion, The Carnegie Group's Geisel says C is absolutely essential for production delivery because application users also want the attributes of real production operating systems to apply to their expert systems. Such attributes as security, data and system integrity, and automatic backup of transactions are not yet available on Lisp machines.

Supporters say there's no reason to shift from using Lisp in development tools because the user can write additional functions in conventional languages

Other expert-system development-tool companies are also starting to make their products available in C. Notable among them are Aion, Radian, and Software Architecture & Engineering.

Lisp-machine operating systems do lack some of the robustness that seasoned commercial systems have developed over the years, acknowledge the language's proponents. But they are quick to point out that there are many very good versions of Lisp and Common Lisp available for a variety of mainframes, superminicomputers, and work stations. They also note that Lisp compilers are getting more efficient and that hardware speed is growing so fast that the run-time performance issues are diminishing to a point where the arguments over it will soon become moot.

IntelliCorp sees no need to offer its Knowledge Engineering Environment (KEE) package in C or any other language besides the original Lisp. The Mountain View, Calif., company has shipped more than 867 copies, maintaining a 60% to 70% market share, according to industry analysts. "The big question in knowledge-based systems is, 'Can the customer develop the applications he needs to realize more efficient operation of his business?' " says Tom Kehler.

If the customer can develop knowledge-based systems and tie in procedural parts of the application that are written in conventional languages such as C, then it doesn't matter what language the development tool is in, Kehler says. "We have no motivation to shift from Lisp. We believe in [Lisp] compilers. They allow working in a high-level language appropriate to the class of problems we need to solve and at the same time answer the need for rapid prototyping and quick-turnaround repair and maintenance."

But is there a need for expert systems that can run on non-Lisp computers and work stations? Kehler answers a resounding yes. IntelliCorp is concentrating on providing KEE on a variety of hardware platforms. The system already has the hooks to tie in C-language procedures, and IntelliCorp was one of the first major expert-system tool vendors to ship its product on Sun work stations. It also has a joint marketing agreement with Hewlett-Packard Co., Palo Alto, to sell KEE on an HP platform soon. And a complete version for full development on VAX work stations will be available soon.

IntelliCorp has just started shipping version 3.0 of KEE. One of the key new features is called common windows. This feature standardizes the KEE expert system's graphics and user interface parts so that, once written, they can be ported from one machine to another in a matter of hours or minutes. Adding common windows was another step, along with the complete rewriting of KEE in Common Lisp, designed to allow expert-system applications to be easily adapted to a variety of hardware platforms.

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Another strong supporter of Lisp for expert-system development and deployment is Dick Gabriel of Lucid, Menlo Park, Calif. "The performance of Common Lisp is rapidly improving. So is its integration into the commercial computing environment," he says.

Many people are working to implement commercial-quality Common Lisp systems on the full range of conventional computers. "It now runs well on mainframes, minicomputers, work stations, and personal computers," says Gabriel. And the speed with which Common Lisp runs on some of these machines is quite adequate, he believes. "Already, today's scientific work stations are nearly as powerful at running expert systems as the specialized Lisp machines."

GEISEL: Carnegie Group's president thinks C tools will tap the 32-bit work station market.

With activity growing in expert systems, it's not surprising that IBM Corp. is in the fold. Besides the third-party vendor packages that are available for the Personal Computer and the RT PC work station, the company offers a couple of AI languages and an expert-system development environment for its System/370 mainframe family of computers.

IBM executives have indicated that the company does not plan to produce dedicated Lisp machines or AI work stations. The company considers the RT machine its AI work station, said Herbert Schorr, group director for products and technology at IBM, speaking at a recent Gartner Group seminar on AI. "The performance numbers look quite good in relation to AI work stations," said Schorr, referring to timing tests done at Carnegie Mellon University.

The roster of expert-system tools for IBM computers includes the Expert System Consultation and Development Environments for both the VM and MVS S/370 operating systems, VM/Prolog, and Lisp/VM. Microprolog and Golden Common Lisp, plus several vendor's expert-system shells, are available for the PC family. Three of the major expert-system development tools, KEE, ART, and S.1, are available for the RT PC or soon will be, along with Quintus Prolog. And Lucid's Common Lisp has just joined the roster of AI languages for the RT PC.

As well as IBM, other major computer companies are becoming big developers and users of expert systems for enhancing their own productivity. Companies such as Apollo Computer, Data General, DEC, HP, Sperry, and TI have many projects. IBM now has 70 expert systems in various stages of development and deployment and is adding more all the time.

KEHLER: IntelliCorp's chairman sees no reason to offer non-Lisp versions of KEE.

Computer makers are finding out from their own experiences that expert systems must be integrated into other applications. They know that when they sell expert-system applications and tools to their customers, this same requirement will be paramount. One internal IBM expert system, for example, is a repair adviser integrated into a storage-system test setup (Fig. 2).

DEC's thrust into expert systems consists of providing the common AI languages—Lisp, OPS5, and Prolog, for example. For expert-system development tools, DEC now relies on the major ones such as KEE, ART, and KnowledgeCraft, which are offered by their developers on VAX computers.

DEC does not plan to build specialized AI hardware or to create any tools beyond the languages, says Magid. "However, we are likely to offer some things in the next generation of tools—what comes after KEE, ART, S.1, and KnowledgeCraft. We will be also looking at products that integrate these tools into data bases and other [non-AI] tools." Magid also predicts that in the 1990s DEC, IBM, and other major computer companies will probably offer symbolic processors as part of their systems architecture.

In support of AI and expert-system development, Texas Instruments Inc. offers customers both hardware and software. The hardware is in the form of its Explorer Lisp machine. The Dallas company's main software offering for expert-systems development is the Personal Consultant Series, a newly announced expansion of its Lisp-based tool into a compatible family of products for the TI personal computer line and the Explorer.

There's no doubt that it's getting easier to build expert systems and to tie them into other applications. And with so many computer heavyweights making sizable commitments to the technology, expert systems are not likely to be held back too much longer. □

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OPINION

LISP IS NOT NEEDED FOR EXPERT SYSTEMS

ALEXANDER D. JACOBSON

The president, chief executive officer, and chairman of the board of Inference Corp. is a veteran manager of high-technology programs. Before he helped found the Los Angeles company in 1979, Jacobson served as a consultant to Control Data Corp. on its Plato computer-aided education system. Prior to that, he managed corporate research and operating division programs for Hughes Aircraft Co.

The commercialization of expert systems requires that the technology be delivered in traditional procedural languages. The importance of languages other than Lisp for delivery of expert systems stems from a number of sources, one of which is the fact that these systems will run more efficiently (require less memory and run faster) in these languages than they will in Lisp when installed on mainstream computers.

Run-time efficiency is fundamental to the economic deployment of computer applications. It is advantageous, for this reason alone, to provide expert-system technology in traditional languages as one of the primary steps towards commercialization.

Expert-system technology is packaged and used in the form of software tools, such as Inference's Automated Reasoning Tool (ART), that are designed to support the interactive process of knowledge engineering and to provide the inferencing capability at the heart of successful expert systems. Most of these tools have been, and continue to be, written in Lisp—and rightfully so, since Lisp is the language of choice for artificial-intelligence research and development.

However, those who use these tools to build expert systems are developing applications, not performing AI R&D. For these people, the language of choice is the particular tool that they use to build their application. These tools are not tied to Lisp; their underlying AI technology can be delivered in traditional languages without loss of functionality, robustness, or power.

No one has yet created a version of Lisp that has its full range of benefits as a development language without suffering significantly degraded efficiency at run time. Because the power and flexibility of Lisp for exploratory development is not needed when using expert-system development tools, its cost in run-time efficiency can therefore be avoided by not using Lisp.

Moreover, garbage collection, which is so valuable in exploratory development, can be particularly burdensome at run time for a practical application. Batch garbage collection leads to randomly occurring, oftentimes lengthy pauses in the operation of an application at run time. The alternative, incremental garbage collection, avoids many of these pauses but leads to a general reduction in run-time efficiency.

Traditional languages, on the other hand, have less of the power and flexibility of Lisp for development, but are optimized to run software efficiently. Moreover, most existing software applications are written in traditional programming languages. Therefore, it is easier and more efficient to interface expert systems written in non-Lisp languages to existing applications software.

Finally, there are situations in which it may not be permissible to deliver an expert system in Lisp. The most obvious examples are defense installations that require Ada.

The conversion of a tool like ART to a traditional language can be done without loss of AI functionality and will neither destabilize the product nor bar its users from programming the procedural part of their expert system in Lisp if they choose to do so, because all major versions of Lisp now or soon will support calling to and from other procedural languages. The advantages of run-time efficiency, interfaceability, programming-language doctrine, and conventional acceptability dictate that such tools be deliverable in non-Lisp languages to take advantage of such important benefits. Given these considerable advantages of delivering expert systems in non-Lisp languages, there is no compelling reason not to do so.

All of the foregoing delineates the reasoning behind Inference's decision to support non-Lisp versions of its product. Put simply, it reduces to this: non-Lisp language implementation delivers full-power expert-system technology in the traditional commercial form that business and industry have come to expect. □

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OPINION

LISP EXPERT SYSTEMS ARE MORE USEFUL

RICHARD P. GABRIEL
The originator of Common Lisp, Gabriel was the manager of the S-1 Lisp Project at the Lawrence Livermore Laboratory and a senior research associate in the Computer Science Department at Stanford University before joining Lucid Inc. as president and chief technical officer. He has a great deal of experience in optimizing Lisp compilers. He also did extensive work on MacLisp at both the University of Illinois and Stanford.

Lisp continues to be the language of choice for artificial-intelligence research. But the question is, should Lisp programs be translated into conventional languages for the commercial world?

The answer is simple: no. The path from the laboratory to the field is smoothest when both worlds use the same programming language.

Lisp has unique features that are not only difficult to develop and use in other languages, but that are fundamental to writing expert systems. Expert systems in Lisp can be more functional, flexible, and useful than what can be achieved using other languages.

A Lisp system can extend itself by writing, compiling, and dynamically linking code. Another feature is that functions (programs) can be created, passed as arguments, and returned as values. A third feature, dynamic storage allocation, means the programmer need not directly manage memory allocation and deallocation and he is not limited to stack-like allocation schemes.

Because of these features, a Lisp-based expert system can be flexible and respond to the situation in the field, even reconfiguring itself to meet changing needs. Translating an AI application from Lisp to another language for delivery to a targeted market cannot be justified if the Lisp version is fast enough, integrated with the commercial environment, and small enough to fit on the computers that are to be used.

One misperception of Lisp is that it is inherently slow because it is simply an interpreted language. But in fact, all Lisp systems in serious use since 1959 have had compilers.

Another misperception is that Lisp must do type checking at run time. Again, for several years, Lisp systems have had declaration facilities that enable a programmer to direct the compiler to avoid run-time type checking.

Yet another notion clouding Lisp's reputation is that garbage collection must be done during the execution of any application program. This is not necessarily so. Explicit memory-management techniques can be and frequently are used.

C is occasionally mentioned as an alternative to Lisp for expert-system delivery, and its performance is cited as a major attraction. But Lisp is not necessarily slower than C. Lisp and C have similar performances on problems for which both languages are appropriate. Benchmarks for three such problems rated Lisp from 20% slower than C to 30% faster. These benchmarks do not represent a wide range of applications.

Expert systems must also integrate with commercial computing. Current Common Lisp systems interact with other systems by invoking non-Lisp code. In many systems, the foreign code can also call Lisp code as if it were a subroutine. Protocols for foreign function calls have minimally adequate functionality at present but are certain to improve rapidly.

Size is another major factor in the delivery of expert systems. Lisp-based expert systems have many megabytes of code and data, with a significant proportion being the underlying Lisp system. Expert systems delivered on run-time Lisp systems that include just those functions needed for deployment are often small enough.

Before very long, even personal computers will be large enough and powerful enough to run today's complex expert systems easily. And then, better expert systems—ones using the full power of the Lisp development environment—can be delivered on personal computers.

AI is a field whose fruits can make a significant contribution to the efficiency and usefulness of computers in the business and commercial world. As with any scientific field that has practical applications, a continuous flow of techniques from the research laboratories into the commercial world is critical to the health of both the scientific field and the commercial enterprises that can benefit from the techniques.

There is simply no good reason to deliver AI in anything but its natural language—Lisp. □

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INFERENCE'S STRATEGY TO SPEED THINGS UP

By making it easier to develop programs, the new C-language version of the ART development tool could accelerate the move of expert systems into the mainstream

A long-time leader in expert-system tools is answering the call for easier-to-use development aids. Inference Corp. is extending the reach of its ART automated reasoning tool beyond the Lisp programming language. Its ART non-Lisp 3.0 will make expert-system programming accessible to program developers familar with the C language. Such development tools could speed up the move of expert systems into mainstream computing (see p. 59).

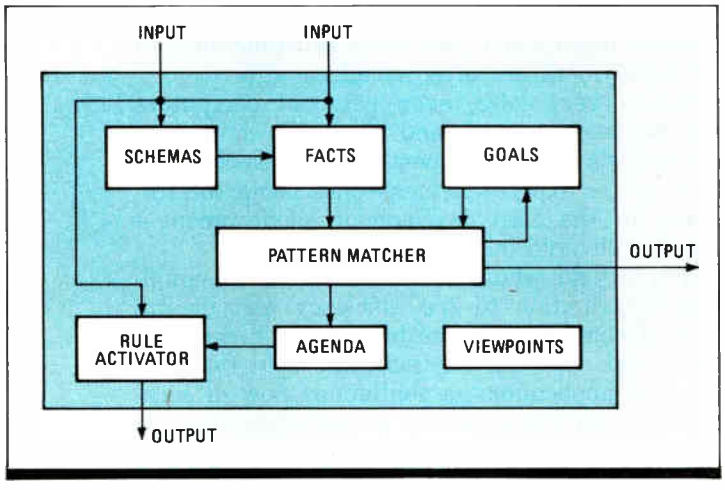
The Los Angeles company is also introducing ART Lisp 3.0 [*Electronics*, July 24, 1986, p. 25]. Both ART non-Lisp 3.0 and ART Lisp 3.0 incorporate a host of powerful enhancements that make them easier to use and improve their performance over ART 2.0. These enhancements should also speed up the spread of expert systems.

ART non-Lisp 3.0, written in C, brings Inference's AI technology to mainstream computing hardware—the VAX minicomputers and Sun-3 work stations, with forthcoming release planned for the IBM RT Personal Computer and Apollo hardware. ART Lisp 3.0 brings Inference's enhancements to developers working on standard Lisp hardware—the Symbolics 3600 series, Texas Instruments Explorer, and LMI Lambda Lisp machines, as well as on VAX and Sun-3 equipment.

The push toward the computing mainstream led by ART non-Lisp 3.0 offers expert-systems developers some powerful advantages. "We're going to gain considerable performance on traditional mainstream computer equipment, as opposed to the specialized Lisp hardware we've used in the past," says executive vice president and chief technical officer Chuck Williams.

"The second issue is interfaceability—ART non-Lisp 3.0 is going to make it easier to fit an expert system into an existing environment. Expert systems are typically developed to be deployed into an existing hardware-software environment. That tends to be easier if you've got a common language foundation, because items like subroutine linkages and naming conventions are the same." That flexibility includes the ability to network ART-based systems.

"The third reason is that we have not simply recoded ART into C—we felt it would be impracti-



1. DIFFERENT DATA BASES. Inference's ART 3.0 represents data in a base composed of schemas, facts, and goals, and includes a viewpoints feature. A pattern matcher, an agenda, and a rule activator round out the system.

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

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cal to maintain two versions as complex as ART in multiple source-code forms and ensure their compatibility and consistency," Williams says. "Instead, we've devised a scheme of automatically translating Lisp-based source code into C. That means we now have the flexibility to deliver ART in multiple languages without compromising our ability to develop and maintain the product. That same scheme can be generalized for translation into other languages—we are under contract to NASA to build an Ada-based version of ART."

The chief improvements in both new versions of ART are reduced garbage collection, for improved efficiency and performance; pattern-matcher enhancements, notably the introduction of joins from the right; a new procedural attachment capability; and graphics enhancements to the user-interface tools.

NO MORE GARBAGE

The modified garbage collection yields perhaps the biggest run-time performance improvements, Williams says. Conventional Lisp-based garbage collection figures out when memory is no longer needed and returns it to a free pool so it can be used by other parts of the program. Lisp can detect underutilization of a memory block and can dump its contents—the origin of the term "garbage collection." In most other programming languages, programmers must explicitly allocate storage when it's needed and later deallocate it, returning it to the free pool.

There is, however, a tradeoff. "What you lose [with garbage collection] is run-time performance," explains Williams. So Inference has streamlined its collection procedures. "What we're doing in C is simply not generating garbage. ART non-Lisp 3.0 deallocates storage when it's done with it—there's no garbage collection because there's no garbage," says Williams. ART Lisp 3.0 also has significantly curtailed its collection duties, so much so that Inference bills it as "99% garbage-free."

In constructing an expert system, a developer will use ART to build a base comprising facts and two other data types—schemas (structured frameworks) and goals (Fig. 1). "The schema system allows you to lay out a taxonomy of different kinds of objects that your system knows about and to classify new objects by relating them to existing, more general concepts," explains Williams.

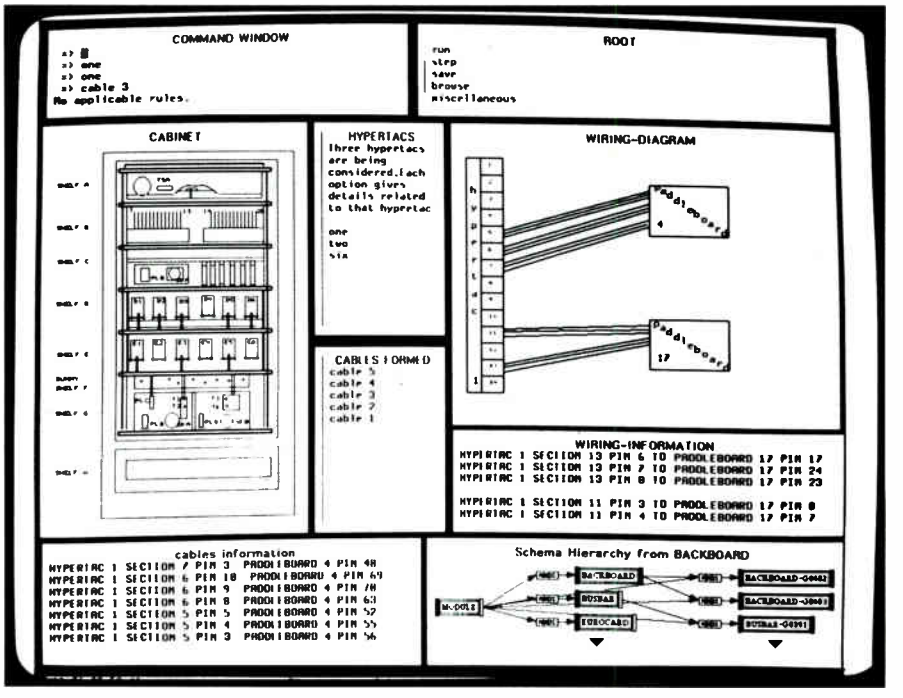
In schema data bases, inheritance is an important concept. If, for example, an IBM Corp. Personal Computer were added to a schema data base of computers and defined as an instance of "microcomputer," then all the data-base information on microcomputers would be applied to the PC. "You can know a whole lot about a new concept just by classifying it as an instance of general concepts that you already know about," adds Williams.

Goals are patterns, representing facts or schema relationships, that an expert system would like to know about. For example, the goal of an expert system for fault diagnosis might be to determine a particular logic gate's output. "The way we do goals is to represent patterns that show the kinds of facts we would like to derive. A goal says the system would like to know a fact that matches this pattern," says Williams. The pattern matcher automatically generates goals by noticing what facts would allow rules to draw useful conclusions.

Like most other expert systems, those developed with ART execute a series of if-then rules to reach their conclusions. A typical rule looks for conditions on the facts, schemas, and goals, using that information to reach its conclusion. More precisely, the conclusion reached by executing the system's rules uses information gleaned from the actions of ART's pattern matcher.

A key component of ART, the pattern matcher finds the significant relationships among the elements of the schema, goal, and fact data bases. "The rules say, 'When you notice a pattern of this kind among the elements of the various data bases, then take this corresponding action on that data,' " says Williams.

"For example, the pattern matcher might look for a property of the IBM PC schema, a relationship it exists in, and a goal about it that all occur in one pattern. So you're looking for a relation-



2. LEFT-RIGHT. Joins from the right speed up problem solving in expert systems. An application called Cables uses it to help select the minimum number of cables for a wiring harness.

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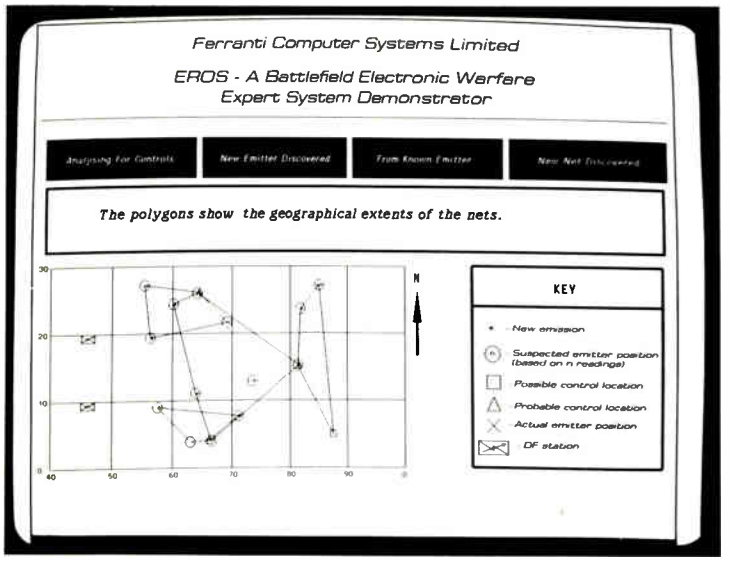

3. HELPER. Using the ART Studio, expert-systems developers can add charts and graphs to their ART-based applications.

ship among these different data elements. Whenever you see a relationship, you take an action—that's the way ART programs work." This strategy is known as data-directed computation.

In performing data-directed computation, ART uses pattern-match compilation, which means the pattern matcher's chief function is to track changes in the data bases. The data bases contain all the declarative information the system knows and representations of what it would like to know. The agenda, another ART component, holds the set of all possible rule matches against the current data. The pattern matcher's responsibility is to update and maintain the agenda as the data bases change, which will occur as the expert system executes its rules.

"The trick of pattern matching is to do it as efficiently as possible," says Williams. With the

ART supports data-directed programming, which can more easily adapt a set of rules to different expert-system problems than can more familiar procedural programming

matching scheme implemented in ART Lisp 3.0, Inference believes it has done just that. It has improved the pattern matcher's structure by adding enhancements to the join net, one of the matcher's two principal components along with the pattern net.

The pattern net classifies each new or altered fact, schema, or goal by making a series of tests on it, identifying which pattern it's an instance of, and maintaining a memory of all such instances. The join net is responsible for noting relationships on multiple patterns. These relationships in essence define a rule antecedent and lead to an activation. (An activation occurs when a rule and a set of data both match a pattern—a "hit.")

The pattern matcher performs AND and NOT joins. In ART 2.0, the AND joins operation "ands" two patterns and then the NOT joins looks for all the other patterns that do not match some other condition. "In ART 2.0, the joins were sequential—every join has a left input and a right input. The right input was always a single pattern, always one of these top-level nodes, whereas the left input could either be a pattern or a previous join," explains Williams.

"ART 3.0 has fundamentally generalized the topology of the join net to support an arbitrary binary tree of joins rather than sequential joins." The new concept has been dubbed "joins from the right" (Fig. 2). It is so flexible that it allows the user to structure the tree any way he likes. To take advantage of this concept, the ART 3.0 user does not have to change his program. ART 3.0's rule compiler will automatically pick the most efficient joins-net topology.

THE DATA IS IN CHARGE

Joins from the right lead to big efficiency improvements in the pattern matcher. "Typically, programs that do pattern matching on schema data get the biggest impact. Speedups from 4 : 1 to 50 : 1 are typical," Williams says.

The functions performed by the pattern matcher make it possible for ART to implement the concept of data-directed computation. "In procedural programming, the procedure decides what to do next—there are explicit branch points in the procedure," Williams says. "In data-directed programming, that's not the case. The data base contains the entire state of the program. A change to the data base selects the set of rules that are applicable. A rule executes, and all it can do is modify the data bases—it can't select the next rule, it can't call the next rule by name.

"What that means is the system has a lot more flexibility to organize and adapt all the rules at its disposal to each particular problem. The benefit that leads to is the ability to incrementally evolve your system."

The procedural-attachment capability is another ART 3.0 highlight. It involves two forms of procedural attachment—active values, and methods and message passing.

The active-values procedure lets ART invoke a subroutine whenever an attribute of an individual schema is referenced, modified, or accessed. "A typical example is attaching a graphical depiction to a schema attribute," Williams explains. "For instance, you might have something in your data base that models a gate during circuit simulation, and whenever the value of one of the inputs changes, you want to update the picture on the screen. You could attach a procedure to the output port of that gate, and whenever it changed, that procedure would be invoked and it

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would update the graphical display."

Methods and message passing, also new to ART 3.0, allows the user to define operations—Print or New Job, for example—on objects. To invoke the operation on a schema, a message is sent to it telling it to go ahead.

The two procedural attachments seem similar but are distinct. With the active values approach, a procedure responds to a change in the schema data. In the methods approach, the program specifically calls for a procedure, somewhat analogous to invoking a subroutine.

The viewpoints feature, though not new to ART 3.0, is generally regarded as a significant feature of ART. The schema, fact, and goal data bases represent a model of a situation, but a viewpoint is a data base that represents a hypothetical situation. The viewpoints feature allows the system to maintain a whole network of models that represent either different possibilities the system might be considering or the state of the world at different points in time.

The viewpoint data base is built dynamically by the execution of rules when the expert system is running. The pattern matcher uses it to see under what hypothetical scenarios or at what points in time patterns match.

The viewpoint data base constitutes another form of declarative data and is very tightly integrated with the schema, fact, and goal data bases. "You can think of it as being a whole network of related data bases—you might have hundreds or thousands of data bases to represent different possibilities," Williams explains. "The representation of viewpoints is extremely efficient, so you represent each possibility only by how it differs from other possibilities."

Systems developers using Inference's new tools will communicate with ART through ART Studio (Fig. 3). An interactive window running on top of the ART system, ART Studio provides graphical displays of the application's knowledge base. Tracing and browsing commands let users stop and examine their programs, as well as graphically displaying internal knowledge structures.

ART Studio provides structured access to the run-time environment and the ability to add incremental updates and modifications. Inference also provides Integrated Editor, which lets the user modify source code and update it interactively and incrementally.

Inference enhanced its Artist interface tool with an interactive drawing system that allows the user to draw and store a bit-mapped graphical image using icons

Inference also has enhanced Artist, the ART interface synthesis tool. The enhancements for the 3.0 versions include an interactive drawing graphics system. Working with either icons or an electronic "brush," users can draw bit-mapped images and store them using Artist's "image" icon type. Previously created images can be recalled and modified. In addition, multiple window displays can be saved in a single file. Artist also features a run-time screen-management package. □

ART 3.0 DEVELOPERS MADE A TRANSITION TO THE COMMERCIAL WORLD

Expert systems have made the transition from the lab to the commercial world, says Inference Corp., and so has its executive vice president and chief technical officer. In the late 1970s, Chuck Williams was researching basic artificial-intelligence technology at Information Sciences Institute, Marina Del Rey, Calif.

"That's where I got interested in AI tools. We were working on an application for which existing tools were clearly inadequate—we developed one called Hearsay 3. But I really wanted to get into an area where results and work were evaluated on practical results. That's why I decided to make the transition into the commercial world."

PAUL HALEY

So in 1979, Williams helped found Inference. Originally, the firm had planned to focus on natural language. "But we started out developing AI tools technology. Around 1983, it became clear that expert systems had a more promising commercial near-term outlook than natural language did, so we made the transition." Williams, 28, was responsible for overall management for the ART 3.0 project. He holds a BS from the University of Southern California and an MS from the University of California at Irvine.

Paul V. Haley, executive director of AI tools technology, joined Inference in 1983 after stints as a consultant for Digital Equipment Corp. and The Carnegie Group. He managed the ART 3.0 project's technical end and was "hands-on responsible for much of the garbage collection and the 'joins from the right.'"

Haley has impressive expert-systems credentials. He was a codeveloper of the Intelligent Scheduling Assistant, a system now used throughout DEC, and he led development of the Intelligent Manufacturing and Control System. From 1981 to 1984, Haley worked with John McDermott at Carnegie-Mellon University, where he developed manufacturing-management expert systems.

"At the time I was at Carnegie-Mellon, OPS5 was the only viable tool for expert-system development, but its ability to develop complex systems was limited," he recalls. "So I saw a phenomenal opportunity to get into the tools business."

Haley, 29, earned a BS in physics and astronomy from the University of Virginia in 1979 and got an MS in computer science from the University of Washington in 1981.

CHUCK WILLIAMS

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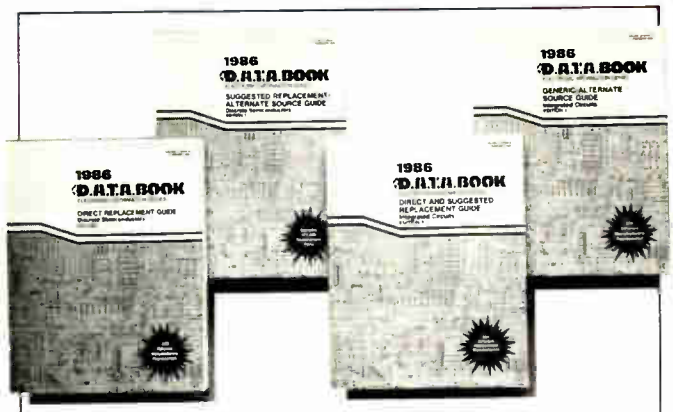

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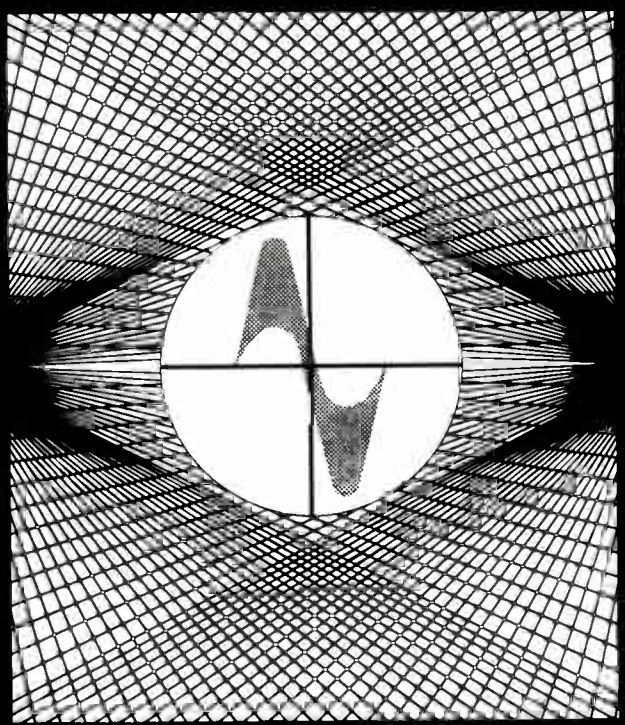

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A NEW WAY TO SPEED UP CIRCUIT SIMULATION

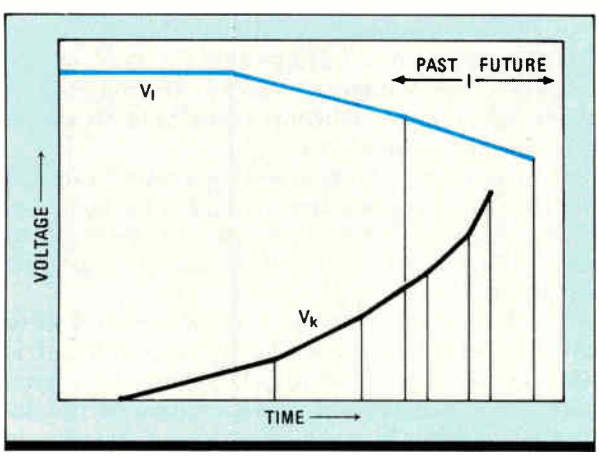
By tailoring analysis to a range of voltages, rather than to the universe of possible values, the Cinnamon algorithm outruns the Spice2 circuit simulator by 100 to 1

More efficient software has taken a back seat in recent years to faster hardware as a way of boosting computer performance. Moreover, most software speed gains have come from better compilers, often called optimizing compilers, rather than from new algorithms that can boost program performance. But computationally intensive work such as circuit simulation is ripe for revised algorithms, and computer researchers are beginning to create them.

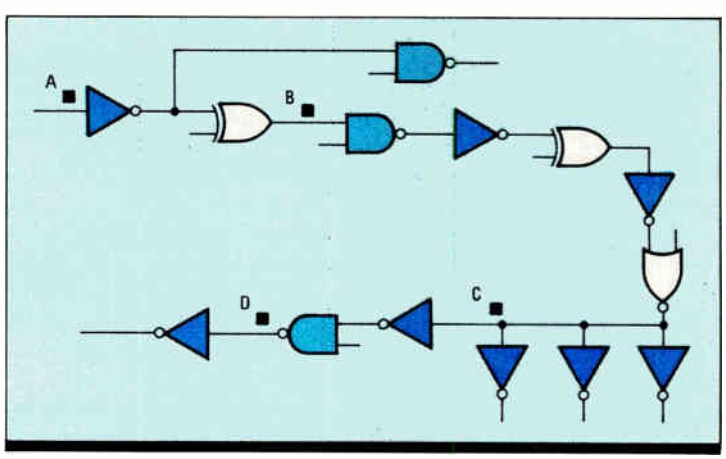
An excellent example of performance improvement gained from work on algorithms is the Cinnamon project at Carnegie Mellon University. The CMU researchers have developed a new approach, including a new algorithm, for simulating circuits with a computer that in many cases does the job about 100 times faster (that is, uses 1/100th the computer time) than the current most used circuit simulator, Spice2.

The Pittsburgh team, headed by Stephen W. Director and including L. M. Vidigal and S. R. Nassif, has developed a simulation algorithm using an event-driven methodology. It specifies a set of voltage changes and analyzes how each such change (event) would affect the circuit being simulated. Traditional integration schemes for circuit simulation compute all circuit variables for a continuous voltage swing for specified points in time.

The overall effect of the Cinnamon (for coupled integration and nodal analysis of MOS net-



1. OUT OF THE PAST. The approximation for node I can be obtained from the past and future scheduling for the node.



2. CRITICALITY. For comparison with Spice simulations, Cinnamon was tested against the critical path of a MOS design, represented by the schematic above.

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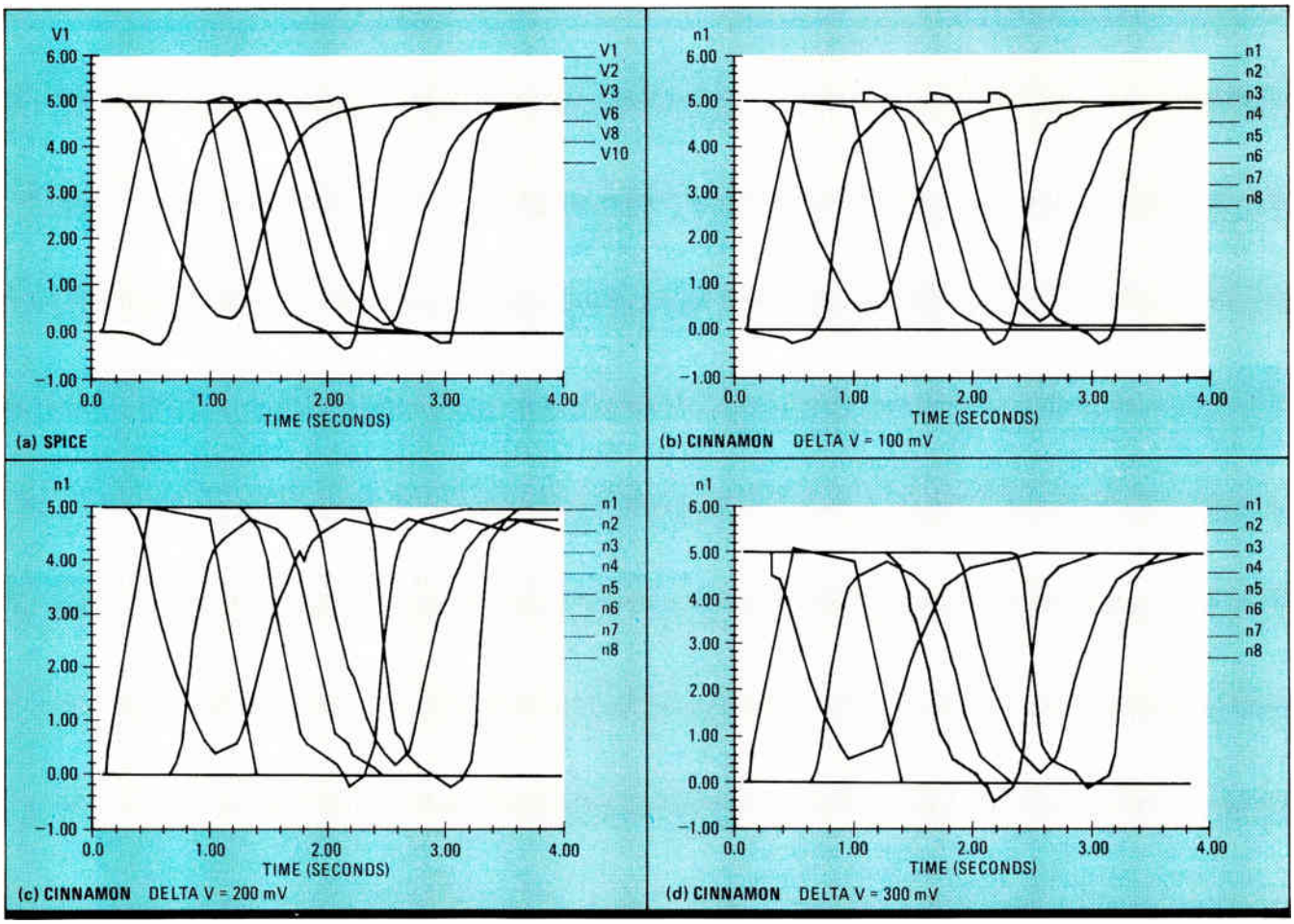

3. MAKING WAVES. Waveforms of the critical-path simulation for Spice (a) and Cinnamon at 100 (b), 200 (c), and 300 mV (d).

works) algorithm is a significantly reduced amount of computation required to accurately simulate a circuit. The basic method could be generalized for any circuit type, but the scope of this work, supported in part by Semiconductor Research Corp. and the Army Research Office, is limited to simulating MOS integrated circuits.

For simulation, a MOS circuit can be regarded as a nonlinear time-invariant network consisting of linear resistors, nonlinear capacitors, nonlinear controlled current sources, and independent voltage sources. Sets of equations that characterize this type of network are well established. The general form of the equation is

$$C(v)\frac{dv}{dt} + f(v) = 0 \qquad (A)$$

where v is a vector representing the node voltages, $C(v)$ is a matrix whose elements represent the nonlinear capacitors, and $f(v)$ is a vector that represents the currents through all other circuit elements. (A) represents a set of first-order nonlinear differential equations.

To solve this set of equations in order to simulate a MOS circuit, most techniques first assume an initial solution. They then use difference methods to subdivide the interval over which the solution is to be evaluated. The smaller intervals correspond to time steps. Unfortunately, these explicit methods tend to be unstable if the time step is large compared with the smallest time constant in the circuit.

Therefore, to eliminate the need for lots of small time steps, which increases computation requirements, most circuit simulators use implicit methods. Here, the values of C and f are assumed to be some function of $v(t_{k-1})$. The new voltage values, $v(t_{k+1})$, can be evaluated by solving a set of nonlinear equations. This is done in most cases by some variation of Newton's method, where the nonlinear elements are replaced at every iteration by a linear approximation evaluated for the estimate of $v(t_{k+1})$.

In summary, conventional circuit-simulation methods first replace the derivative by some estimate and only then linearize the network to solve the resulting set of nonlinear algebraic equations.

The Cinnamon research team observed that to solve the equations for a nonlinear circuit, it is natural to control the step size by the region over which a linearized approximation of the device's behavior is valid. For MOS networks in particular, the device's behavior over large voltage ranges is quasilinear. Hence, if the elements

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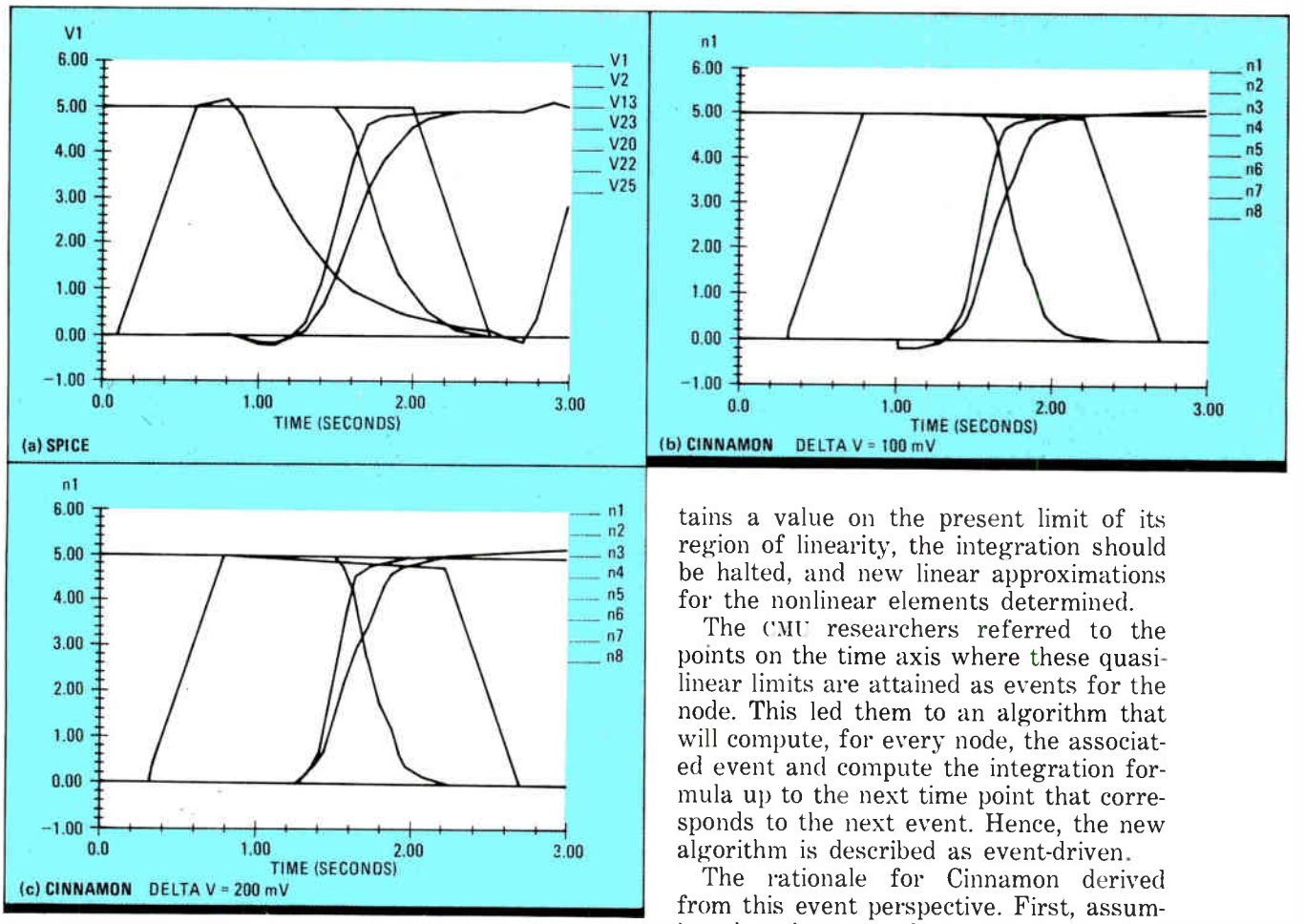

4. TWO-BIT SOLUTION. Spice simulated waveforms for a 2-bit comparator in 1,100 s (a). Cinnamon took 12.5 s at 100 mV (b), 8.1 s at 200 mV (c).

in the network are linearized, the circuit's dynamic behavior can be represented by a system of linear differential equations of the form

$$C\frac{dv}{dt} + Gv = i \qquad (B)$$

where C and G are n-by-n matrices (n stands for the number of nodes in the network) and v and i are vectors of size n. For a MOS circuit, C is a symmetric, nonsingular matrix and in most cases diagonally dominant. Though diagonal dominance is not essential to the Cinnamon algorithm, it can be used to speed the solution of this set of equations. While this is a first-order differential equation that could, in principle, be solved by any of the well-established integration methods, such methods are computationally intensive.

The analytical solution can be formulated easily as a function of a matrix e^{At}, where $A = C^{-1}G$. Although this matrix is in general hard to compute, if the order of the matrix is small, it is easy to obtain an explicit and exact solution for v, the different values of the node voltage.

The differential equation, (B), will be valid only for those values of v where the linear model in use is valid. Whenever a node voltage attains a value on the present limit of its region of linearity, the integration should be halted, and new linear approximations for the nonlinear elements determined.

The CMU researchers referred to the points on the time axis where these quasi-linear limits are attained as events for the node. This led them to an algorithm that will compute, for every node, the associated event and compute the integration formula up to the next time point that corresponds to the next event. Hence, the new algorithm is described as event-driven.

The rationale for Cinnamon derived from this event perspective. First, assuming that the network under consideration is initially stable, the algorithm applies a perturbation to node i. This forces the voltage at this node to reach a discrete value immediately below or above the current value, and a new event will be scheduled for node i. All other nodes in the network will not notice this voltage change simultaneously as there are intrinsic delays associated with any RC network. In other words, the change in voltage v_i will initially affect only the adjacent nodes—those that are connected to node i, through a capacitor, resistor, or transistor.

These node voltages can be computed by solving the respective node equations. The method can then be applied sequentially until the network stabilizes. For example, the equation for node k is:

$$C_k\frac{dv_k}{dt} + G_k v_k - \sum_{j\epsilon J} C_{kj}\frac{dv_k}{dt} - \sum_{j\epsilon J} G_{kj}v_j = \sum_m i_m \qquad (C)$$

where v_k is the voltage at node k and v_j the voltage at node j. J represents a set, usually small, of indices to the node voltages that will contribute to the equation at node k. C_k is the sum of capacitances connected between nodes k and j. The coefficients G_k, G_{kj}, and i_m result from

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the linearization of $f(v)$ in the first equation.

Obviously, the above equation should not be solved independently of the other n-1 equations in linear differential set (B). However, if the exact solutions for the v_j, $j \epsilon J$ were known, the solution for v_k could be exactly determined from the linear differential equations (B).

If an approximation is kept for every voltage waveform, a new approximation of v_k can be obtained by solving a convolution integral. Generically, e^{At} represents a sum of exponential terms. If the voltage steps for the node voltages are small, these exponential terms can be approximated by straight lines obtained from the previous known and next estimated event associated with the node (Fig. 1).

IMPLEMENTING CINNAMON

A straightforward way to implement the Cinnamon algorithm is to assume that the voltage axis can be broken into discrete points such that all voltage values are multiples of ΔV. The interval ΔV ultimately defines the simulation's accuracy. At every step, the integration algorithm's objective is to find, for each circuit node whose voltage is changing, the point in time where the node voltage attains the next discrete value (an event).

The algorithm is clearly explicit, thereby avoiding costly iterations at each time step. But because the method automatically maintains bounds for the voltage values, it does not suffer from stability problems that occur in conventional explicit techniques caused by wild voltage variations when the step size is not kept small.

Also important is the data's structure and organization. This approach tries to solve only a few equations when an event is scheduled, namely those that are directly influenced by the node voltage corresponding to the event.

Evaluating the coefficients for these equations is the algorithm's single most time-consuming task, so it must be done as efficiently as possible. To avoid searching through one long list of nodes and elements, the algorithm organizes each node's data in two linked lists. One is for adjacent nodes, whose functions must be evaluated whenever the node is scheduled. This list is used to decide how many equations are to be solved for every event. The other list consists of components connected to the node. It is used to derive the coefficients of the nodal equations.

The execution time of a simulation using the Cinnamon algorithm does not depend on the number of nodes in a network but rather on the level of activity during the simulation. In addition, the algorithm shows good stability and execution times very much smaller than Spice2. Many simulations have been run by the CMU team with both Spice2 and Cinnamon. The engine used for these tests is a Digital Equipment Corp. VAX-11/785 running Berkeley Unix 4.2.

A FEW EXAMPLES

One test simulation used to compare Spice and Cinnamon was a critical path found in a MOS design (Fig. 2). The corresponding waveforms obtained with Spice and Cinnamon were compared for different values of the voltage step (Fig. 3). The simulation of this circuit required 752.9 s with Spice. The run times for Cinnamon were 24.7 s for a ΔV of 100 mV, 14.7 s for a ΔV of 200 mV, and 10.4 s for a ΔV of 300 mV. Note that for even large values of ΔV good accuracy is achieved.

In another test, Spice simulated a 2-bit comparator (Fig. 4) in 1,100 s. Cinnamon required only 12.5, 8.1, and 6.8 s for ΔVs of 100 mV, 200 mV, and 300 mV, respectively. This truly impressive performance illustrates the significant opportunity for improvement to be gained through algorithmic development. □

A THREE-MAN TEAM DESIGNED CINNAMON

The Cinnamon simulator grew out of the ongoing research work of Steve Director and his associates at the Center for Excellence in Computer Aided Design. Based at Pittsburgh's Carnegie Mellon University, the center's primary goal is research into design methodologies for very large-scale integration. The center is one of two Semiconductor Research Corp. centers devoted to research in computer aided-design, the other being at the University of California at Berkeley. (SRC also sponsors a microstructure research center at Cornell University in Ithaca, N. Y.)

Director, who is Whitaker Professor of Electrical and Computer Engineering as well as head of that department at CMU, is the center's director. His teammates on the Cinnamon project were Sani Richard Nassif and Luis Manuel Vidigal. Nassif, until this spring one of Director's graduate students, is now at Bell Laboratories in Allentown, Pa.

SPICE BUSTERS. CMU's Nassif and Director (from left) developed Cinnamon with help from visiting professor Vidigal.

Vidigal, an associate professor at Instituto Superior Tecnico, Lisbon, Portugal, graduated from CMU in 1980. He was a visiting associate professor of electrical and computer engineering at CMU last year.

The Cinnamon project was a team effort that extended from June to December 1985—the period that Vidigal was visiting professor. First, the Cinnamon algorithm was designed during a series of meetings of the triumvirate, then Nassif and Vidigal did most of the coding and testing.

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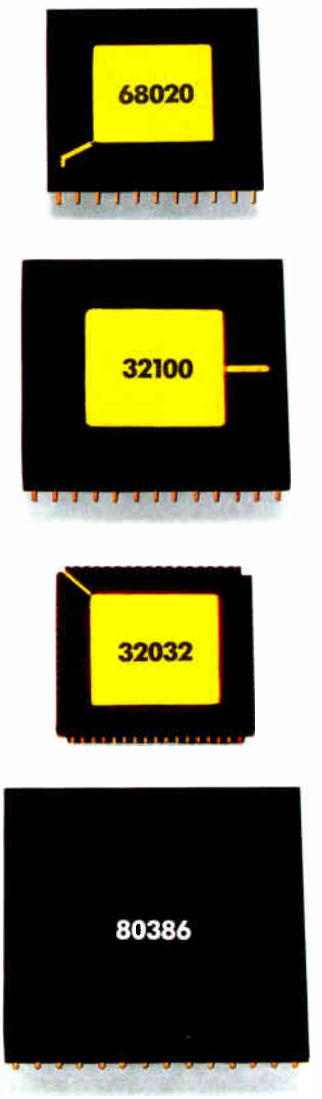
If they had it to do all over again,



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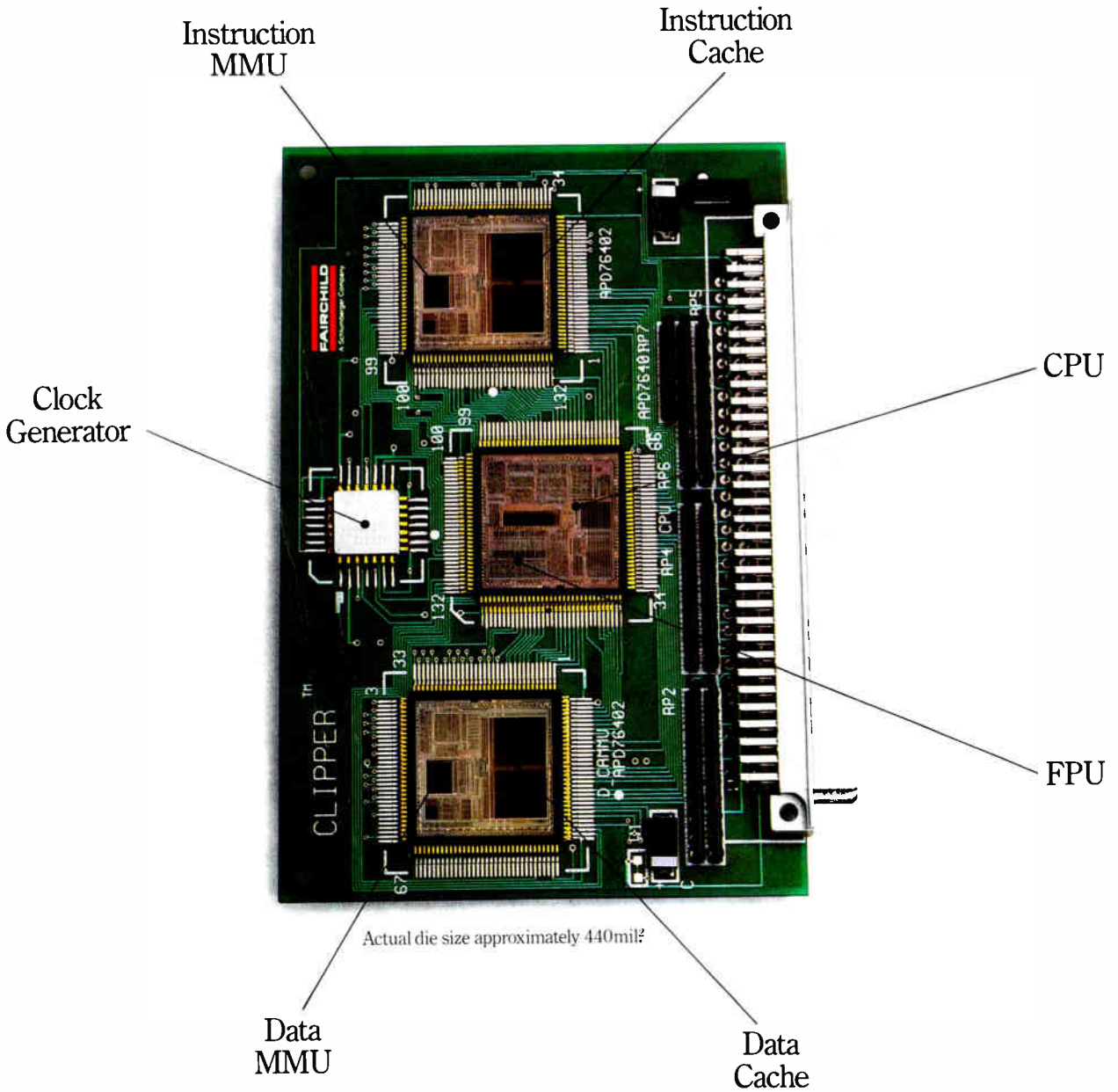
this is how they'd do it.



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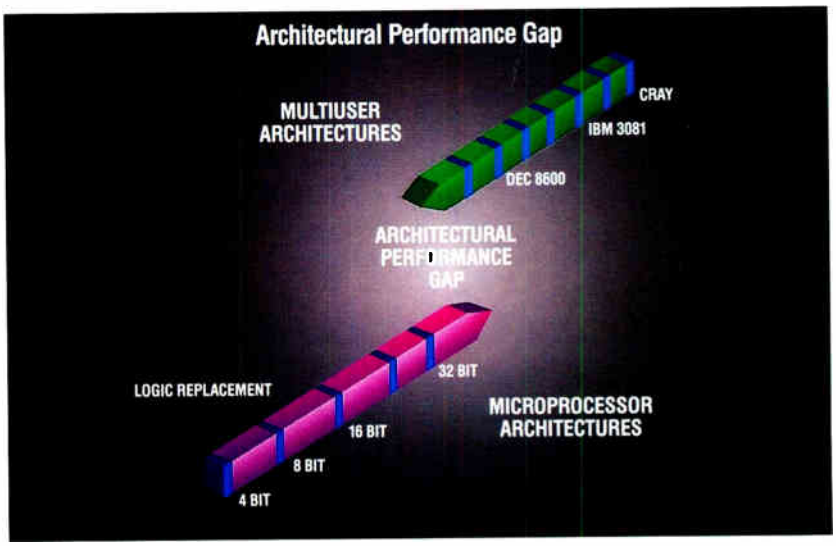

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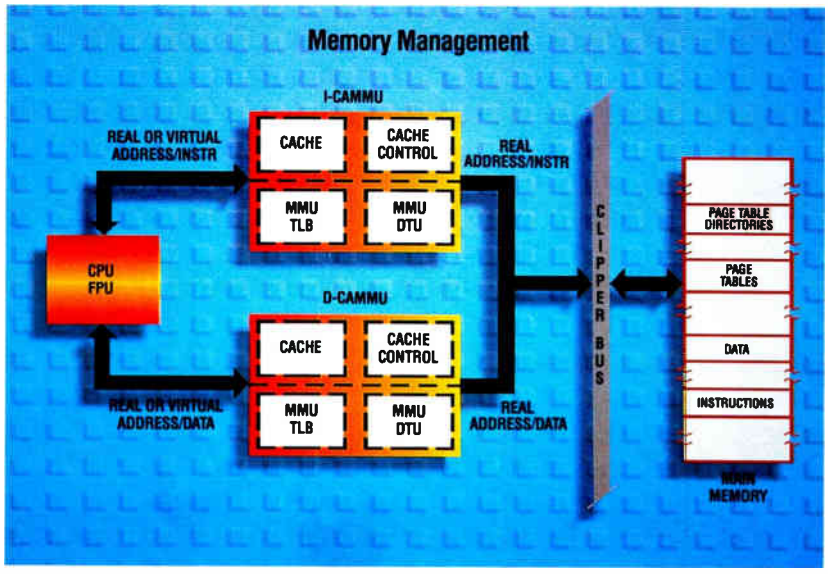

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We also included mainframe-style caching. The two large 4K-byte caches, combined with mainframe-style set associativity and 16-byte line size, reduce memory access times and significantly improve hit ratios. When it comes to bus bandwidth, the CLIPPER CPU features two 32-bit buses to cache memory. Bus bandwidth to the CPU is 133M bytes per second, far greater than ordinary, single-bus architectures. We enhanced bus bandwidth even further by using an additional 32-bit CLIPPER synchronous bus that provides quad-word updating of the caches, in addition to its flexible byte, half-word and word transfers.

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Lastly, you'll find switching speeds up to the rest of the fast CLIPPER standards. Like Fairchild's FACT logic family and other advanced products, CLIPPER is fabricated with a high-speed, double-metal advanced CMOS process that achieves transistor switching at speeds of up to 500 ps.

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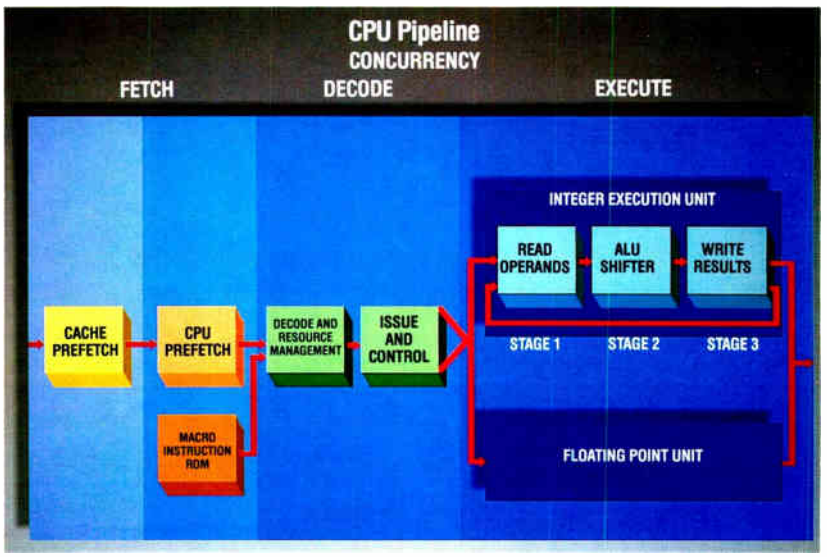

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BUILDING FAST SRAMs WITH NO PROCESS 'TRICKS'

Motorola goes for circuit improvements, rather than exotic process refinements, to develop a pair of 64-K static RAMs that boast speeds better than 35 ns

One company moving into the new market for high-speed CMOS static random-access memories is bucking the trend toward process complexity. Motorola Inc. has devised a series of circuit innovations that create truly asynchronous SRAMs capable of speeds as fast as 25 ns.

Its competitors are using a variety of processing techniques—1.0- and 1.25-μm geometries, three levels of interconnection, silicides and salicides to reduce resistance and increase speed, and bipolar/CMOS combinations—to push speeds to less than 50 ns on 64-K SRAMs. The upshot is a wealth of new products in a market traditionally dominated by bipolar technology (see p. 121).

Motorola is coming to market with a pair of high-speed 64-K SRAMs [*Electronics*, July 24, 1986, p. 151] that use a conventional double-level-metal, double-polysilicon-gate, 1.5-μm CMOS process. Without resorting to any special processing tricks or techniques, the Austin, Texas, company has produced the 64-K-by-1-bit MCM6287 and 16-K-by-4-bit MCM6288, capable of typical speeds as fast as 35 ns and maximum speeds of 25 ns over the full commercial temperature range. At room temperature, the speed of the devices pushes below 15 ns.

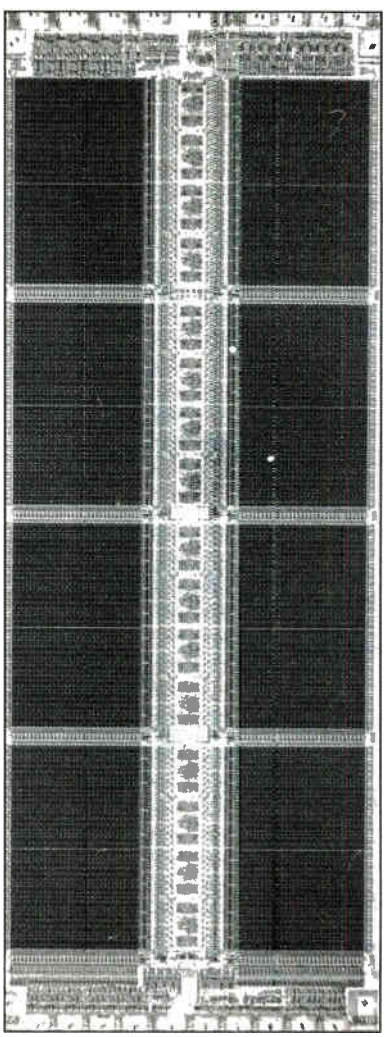
Motorola is also introducing a 4-K-by-4-bit SRAM fabricated using the same process and circuit techniques. It will have an access time of less than 10 ns over the whole temperature range and will approach 1 ns at room temperature.

Motorola's two new SRAMs achieve their high speeds with a remarkably low active power, 250 mW ac and 100 mW dc, using a 40-MHz clock rate. Equally impressive is the ability of the new SRAMs to operate as fully asynchronous devices, says Steve Flannagan, manager of the fast SRAM design project. The truly asynchronous operation and immunity from skews derive from a proprietary circuit technique. Unlike present designs, it distinguishes between address transition detection and address stability detection.

The key to the SRAM's high speed is not process improvements or scaling, but rather 13 proprietary circuit improvements, says Roger I. Kung, manager of MOS memory design at Motorola's MOS Memory Products Group.

Significant among these is a new SRAM architecture (Fig. 1) that allows extremely short bit lines (with only 64 cells per bit line) for high-speed signal development during read operations and ensures increased data integrity during write operations.

The way Motorola implemented bit lines in the architecture makes a particular contribution to



1. NEW DESIGN. In designing its 25-ns 64-K-by-1-bit (16-by-4) CMOS SRAM, Motorola used innovative circuit, not process, improvements to boost speed.

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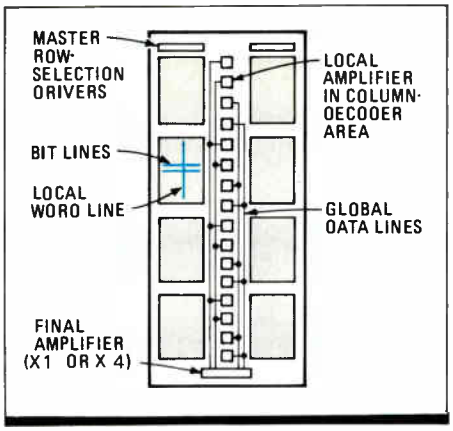


2. SUBDIVIDED. So it can achieve high speed while using low power, Motorola's 64-K SRAM is divided into eight blocks with only 64 cells per bit-line.

chip speed (Fig. 2). In most other designs, the bit lines extend the length of the memory device and are very long and vertical, which decreases speed and increases bit-line capacitance, resistance, and delay time.

This design uses local word lines, which ensure low power because only one eighth of the memory is activated at a time. But the design combines them with horizontal bit lines that contain only 64 cells each instead of 256 or more; this provides high-speed signal development.

Contributing substantially to the higher performance of this design are the high gain margin and high stability of the basic four-transistor cell (Fig. 3), which occupies only 189 μm^2. Motorola achieved them "by increasing the size ratio of the cross-coupled pull-down transistor to the transfer transistor—from a simple 1 : 1 correspondence to over 3 : 1," says Flannagan. This increases the cell's immunity to process variations and, more important, its immunity to noise.

The higher size ratio required one modification to the plain vanilla 1.5-μm CMOS process Motorola is using: the addition of a second level of metal interconnection. Bit lines are in first-level metal, the resistor is in second-level polysilicon, and two second-level metal lines cross the memory cell. These cells are organized into a 128-row-by-512-column array divided into eight blocks.

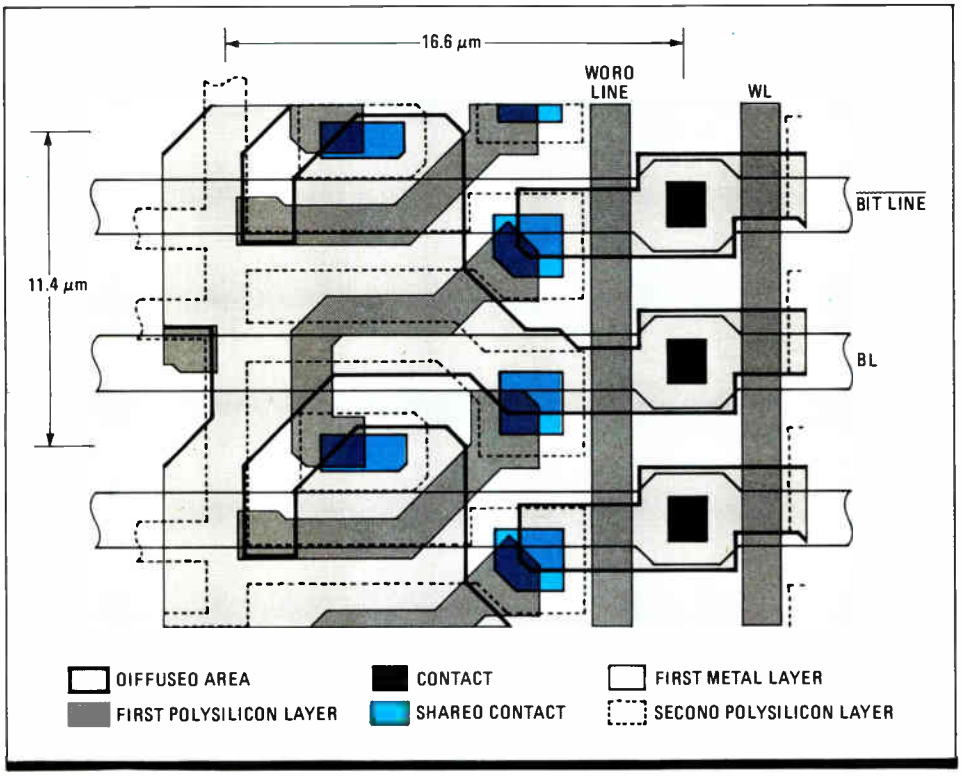
A further aid to high speed is a proprietary circuit that allows power-down without any speed penalty. "Ordinarily, the chip deselect signal produces a false address-transition-detection signal, which causes the cycle to start over again, resulting in a chip-select penalty the equivalent of a complete cycle," Flannagan says. To eliminate this delay, a chip-select speedup function implemented on the chip sends out an ATD-inhibit signal at power-down, masking out the false ATD pulse. The new architecture results in greatly improved data sensing. It takes only one or two nanoseconds to develop a reliable signal, versus 45 ns for other approaches.

AN ASYNCHRONOUS RETURN

The Motorola chip design's asynchronous capabilities constitute a major contribution to the state of the art, according to Flannagan. "Historically, the original static RAM designs were conceived as asynchronous devices. But as the industry moved toward higher complexity and speed, many designers opted for synchronous designs," he says. A synchronous SRAM recognizes transitions only at predetermined points in a clock cycle, whereas an asynchronous SRAM allows and recognizes address changes or transitions at any time.

In recent years, there has been a move back to asynchronous designs in SRAMs based on ATD, a self-clocking technique that uses the address transition signal, or edge, as a reference and performs a summation, synchronizing all operations on the chip to that signal. The ATD approach does not sacrifice speed, but "the problem is that it assumes all the addresses occur at the same time," says Flannagan. "In real life this seldom occurs, with the various address edges occurring in any timing relationship to one another. For example, addresses may go through a transition and change back again at any time whatever."

Motorola's SRAMs share certain characteristics with ATD designs: when a summation address transition is detected, the array is equal-



3. HIGH-GAIN CELL. The key to stability and performance is the high-gain four-transistor cell with double-polysilicon gates and double-level metal in only 189 μm^2.

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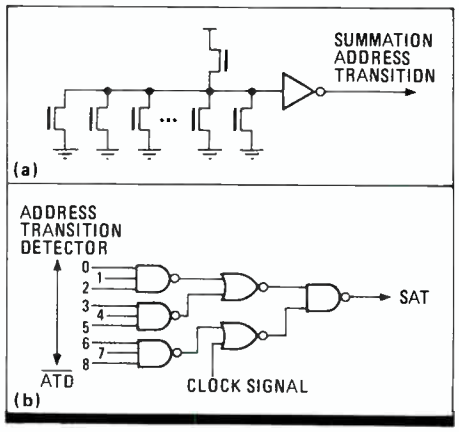
ized—that is, the bit lines are precharged and the word lines are set to their appropriate values. In addition, the sense amps are turned off, and the output buffer is placed in a hold state.

So to make their SRAMs fully asynchronous, the Motorola designers have taken the ATD approach one step further: they distinguish between address transition detection and address stability detection. Unlike present ATD approaches, address summation is not timed from the first edge; rather, it is postponed until address stability has been detected.

"With receipt of the second edge, the memory recognizes that enough time has passed for the address transition signal to stabilize," says Flannagan. The second edge then begins the access cycle, turning on the new word line, turning on the amplifiers, and controlling the output buffer. A predetermined time later, the cycle-end signal turns everything off except the output buffer.

For this approach to work, Motorola had to replace the traditional address summation circuit (Fig. 4a), consisting of a wide, shallow NOR gate with a big, hard-wired, high-capacitance metal line running from the top to the bottom of the memory array. "In the particular architecture we chose, this common metal line has a very large fan-out, with as many as 16 addresses at one time, slowing it down considerably," says Flannagan.

Also, the wide, shallow NOR-gate circuit requires a reset pulse; the result of such a pulse is that the first edge, the address transition signal, does not track the second edge, the address stability signal—they are not in sync. "For true address stability detection, it is necessary that the second edge be controlled by the natural propagation delay through the circuit," he says.



4. ASYNCHRONOUS. For asynchronous operation, Motorola's 64-K SRAM replaces NOR gates (a) with treelike summation circuits (b).

In the Motorola SRAM, this common NOR gate is replaced by separate summation address transition (SAT) generators for the rows and for the columns. With the elimination of the common SAT generator—which requires a specified ratio between the driver and the load devices—the local SAT devices can be built using a ratioless, treelike logic structure (Fig. 4b) in which the load devices are gated by clock signals, and transmission of logic signals from one gate to another is similarly gated.

The chief advantage of this structure is that, being ratioless, it is inherently synchronous, with signal propagation through the gates paced only by the system clock, says Flannagan; this design minimizes timing problems considerably. In addition, such ratioless logic has lower power dissipation, because there is no direct discharge path from the power supply lead to ground, and because the use of minimum geometry devices reduces the die-area requirements. □

DEVELOPING CMOS SRAMS: THE CHANCE OF A LIFETIME

To Stephen Flannagan and Paul Reed, their assignment to develop Motorola Inc.'s new family of high-speed CMOS 64-K static random-access memories was the chance of a lifetime, a chance to show that aggressive circuit design could accomplish as much as aggressive process development.

"In a general sense, part of our charter was not just to develop the fastest or the lowest-power or even the most cost-effective CMOS SRAM, but the best combination of all of these," says Flannagan, fast SRAM design manager. The company also wanted a part that would serve as a vehicle to move to higher-density 256-K and 1-Mb SRAMs as process improvements allow.

With these parameters, the first decision he and Reed, design engineer and project leader, had to make was relatively easy. "If cost was to be a factor, it was clear that pushing the process to the limits was not the answer," Flannagan says. "The emphasis had to be on circuit design. Not that process development is not important, but in this case it had to serve the needs of the circuit designer, rather than vice versa, as is often the case." Once that decision was made, the second—who was going to direct the design of the 16-K-by-4-bit configuration and who the design of the 64-K-by-1-bit configuration—was also easy, he says. "Paul had the most experience with by-4 memory designs, and I had the most experience with by-1 designs."

NEXT STEP. With their 64-K SRAMs in production, Paul Reed, left, and Stephen Flannagan are working on their 256-K SRAM.

Reed, who graduated from the University of Missouri in 1977 with a BSEE, received most of his experience in memory design at Texas Instruments Inc. Since 1983, he has been involved in SRAM design at Motorola's MOS Memory Design Group in Austin, Texas.

Flannagan received his BSEE from the University of Cincinnati in 1977 and a MSEE from Oregon State University while working at Intel Corp. from 1977 to 1983. Since 1983 he has been at Motorola, where he's responsible for the 256-K SRAM development.

As the 64-K SRAMs go into production, the team has seen first silicon on 256-K SRAM prototypes using 1.25-μm design rules; 1-Mb SRAMs using 1-μm geometries are in design. Both use the same double-level-metal, double-polysilicon-gate CMOS used on the 64-K types.

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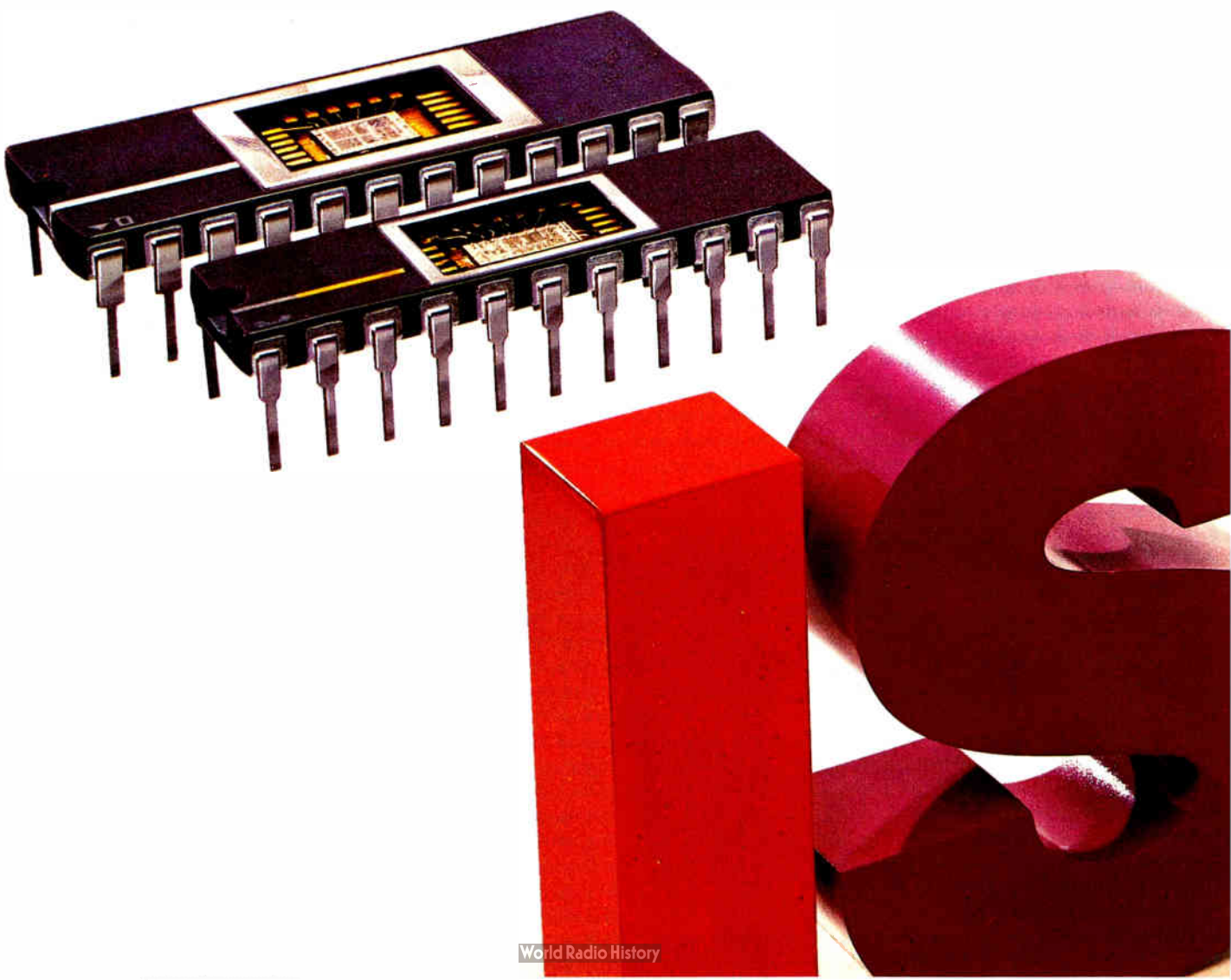

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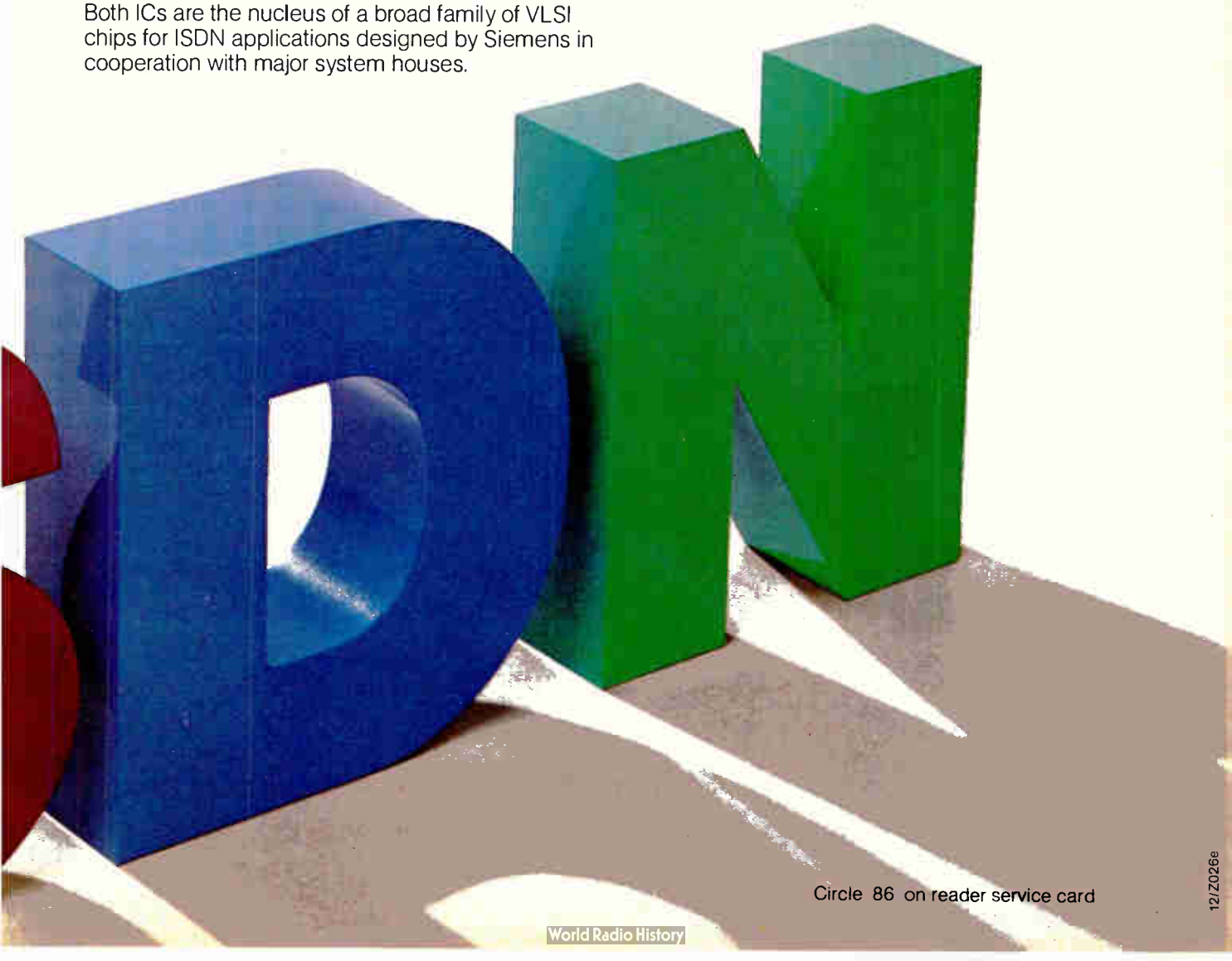

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THICK AND THIN FILMS BATTLE FOR GROWING HYBRID MARKET

Thick-film hybrids still dominate the market, but thin films are coming on fast. And a new competitor emerges—electroplating copper on ceramic

by Jerry Lyman

Despite the current industry malaise, the market for hybrid microelectronics continues to grow at a good clip. Both thick- and thin-film hybrids are being driven by the needs of the growing military and aerospace markets and their increasing demands for dense, high-speed, high-powered circuitry in the smallest possible area and volume. The total U. S. hybrid market (65% captive and 35% independent) amounted to about $1 billion in 1976 and has now reached about $4 billion, according to estimates from Tektronix Inc. About 40% of current sales are for military applications.

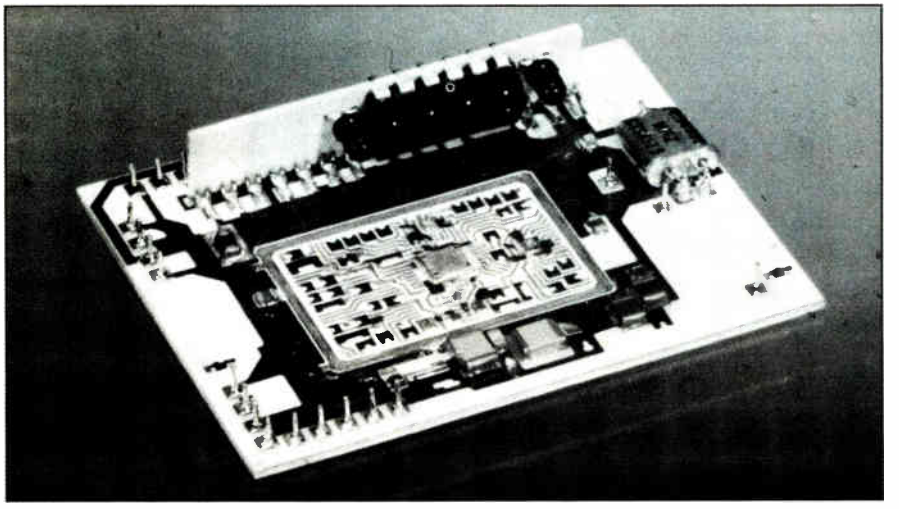
While thick-film hybrids are maintaining their preeminence, three trends have started to reshape this industry:

- The use of thin-film technology, both by itself and combined with thick-film technology, is increasing; at the same time, a rival—electroplating fine lines directly on ceramic—has appeared.
- Power hybrid applications are increasing.
- Electronics and aerospace manufacturers with in-house hybrid facilities are actively soliciting custom work from outside customers.

Thick-film hybrids, used in 75% of all applications, dominate the world of hybrid microelectronics (Fig. 1). The thick-film process is based on sequentially screening and firing multiple layers of conductive, resistive, and insulating thick-film pastes onto a ceramic substrate. For low-level circuitry, the usual substrate is a material called 96% alumina. Beryllia is the material of choice for applications dissipating a lot of power.

Typical conductor materials are gold (for wire-bonding and multilayering), platinum gold (for reflow soldering), and palladium silver (the lowest-cost material). Resistive pastes are mostly based on ruthenium oxides and cover a resistance range of 3 Ω to 10 MΩ per square, with temperature coefficients from 50 to 100 parts per million/C°. Today, most hybrid manufacturers have standardized on 10-mil lines and spaces for their thick-film conductor patterns, but the limit for thick-film hybrids is actually about 5 mils. Thick-film hybrids can be multilayered, and most companies now routinely do four to six layers.

Currently, thick-film hybrids are being assembled either with the chip-and-wire technique, based on die- and wire-bonding bare chips to screened-on pads, or with surface mounting where packaged leaded



1. LED LIT. A thick-film hybrid from Aeroflex has a light-emitting-diode display on a small substrate reflowed to a large substrate containing the display's drive and control electronics.

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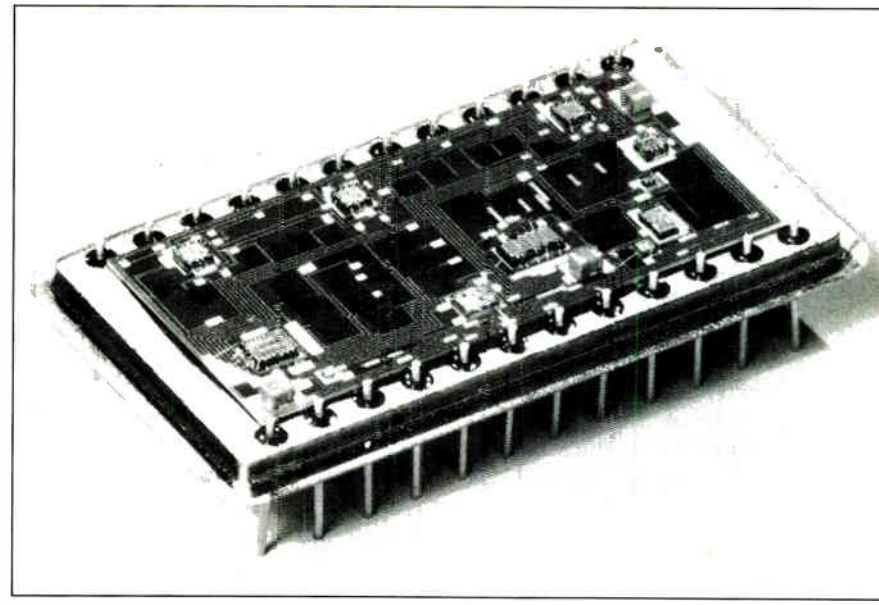
or unleaded components are reflow-soldered to the pads of a substrate. In general, most military hybrids use the chip-and-wire technique. However, some military contractors such as RCA Corp.'s Government Systems Division, Moorestown, N.J., sacrifice the acknowledged density advantage of chip-and-wire packaged thick-film hybrids by building military thick-film hybrids with chips in leadless ceramic chip carriers. RCA's engineers feel that the testability of the packaged chips in this militarized surface-mounting application results in higher assembly yields and better long-term reliability.

While RCA produces no complete chip-and-wire hybrids, it does produce small hybrids consisting of three to four medium-scale-integration chips wire-bonded inside a ceramic leadless chip carrier, which, in turn, is reflow-soldered to a motherboard ceramic substrate housing an array of single large-scale and very large-scale-integration chips in their carriers. The multichip submodule can be tested and burned in before final assembly. Saab Microelectronics in Sweden uses the same technique on its large-scale avionics ceramic modules.



2. THIN-FILM DAC. The fine-line conductors possible with thin-film technology allow all the circuitry of ILC Data Device's 12-bit DAC to be combined in one layer.

MANY ASSEMBLY CHOICES

In the commercial world, there are other forms of thick-film assemblies. For example, many telecommunication companies have surface-mounted assemblies based on leaded plastic packages, such as plastic-leaded chip carriers, small-outline integrated-circuit packages, small-outline transistors, and even plastic quad flatpacks reflow-soldered onto the ceramic substrate. This last type is particularly popular in memory packages.

In automotive applications, hybrids make up 5% to 10% of a typical car's electronics; for example, they can be used in voltage regulators, ignitions, and sensors. Delco Electronics, Kokomo, Ind., which manufactures the electronics for General Motors Corp. cars, has a large thick-film facility that uses neither chip-and-wire nor conventional surface mounting. Instead, Delco uses flip chips (solder-bumped chips designed for face-down mounting) that are reflow-soldered to the ceramic. Hybrid modules for 1987 car models will employ thick-film hybrids with a mix of flip chips and chips in single-layer ceramic, or SLAM, leadless carriers. The SLAMs are capable of higher input/output counts than the flip chips. For the future, Delco is looking into applying extremely high-lead-count tape-automated bonded chips to its hybrid substrates.

Bare TAB bonding (with the chip and its tape beams excised from the tape) approaches wire bonding in packaging density and allows testing and burn-in of chips on tape.

Hybrids with TAB chips are already being used in large computer mainframes [*Electronics*, March 10, 1986, p. 44] mainly as multichip, multilayered ceramic chip assemblies in the U.S., Japan, and France. But the cost of this technique is still too high for the small runs of custom military and commercial hybrids most U.S. companies handle.

Thick film's rival is thin-film technology, which uses the techniques of IC processing—optical lithography, sputtering, and etching—in a subtractive lithographic process to produce much finer lines than can the thick-film process.

Thin-film substrates are typically a 99.6% alumina ceramic, but glass, silicon, and fused silica can also be used. The conductor material normally used with thin-film processing is gold, and the minimum line width, limited by current film photoresists, is now at about 1 mil. Most thin-film facilities for production runs actually have 2- to 5-mil design rules.

Thin-film processing produces much finer lines than thick-film processing can; 2- to 5-mil-thick gold conductors are routine on most production facilities

In the resistor area, the deposited thin-film resistors (nichrome or tantalum) are superior, in terms of temperature coefficient and resistive tolerance, to their thick-film counterparts. This accounts for the use of thin-film networks as a component in many thick-film applications.

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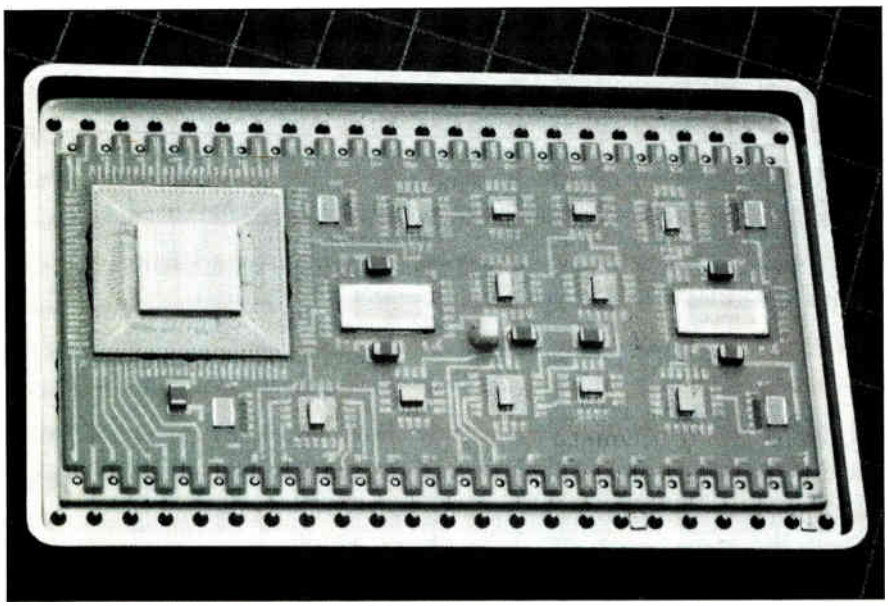
Thin-film hybrids are primarily used in high-frequency applications. With care, thick films can be pushed to the 2-GHz vicinity, but thin films are more effective at higher frequencies. The thin film's smaller conductor geometry and more precise definition of conductor edges minimize lead inductance. Thin films are suitable for operation up to 60 GHz.

The thin-film technique is also valuable in complex analog or analog/digital applications where space is at a premium. Current noise for thin-film resistors is more than 10 dB lower than the lowest value for thick-film resistors.

Thin-film technology is now crossing over into some of the lower-frequency applications usually done with thick-film processing. For example, companies such as ILC Data Device Corp., Bohemia, N. Y., have done complete data-conversion hybrids on one layer of a thin-film substrate (Fig. 2). The same unit in thick film would have required a multilayered approach. The increased interconnection density of the finer-line thin-film hybrid makes multilayering unnecessary.



3. THICK AND THIN. The VLSI portion of Circuit Technology Inc.'s thick-film MIL-STD-1553B microprocessor interface is mounted on a small thin-film substrate.

The advent of VLSI chips and those from the Pentagon's Very High Speed Integrated Circuits program with over 68 I/O pads has caused several hybrid manufacturers to mix thick- and thin-film techniques to get the interconnection densities required. For example, Natel Engineering Co., Simi Valley, Calif., which makes military data-conversion modules, has developed an assembly method it calls a subhybrid/hybrid routine.

In this method, multiple small thin-film substrates are fabricated on a large (3-by-3-in.) substrate. The key chips of an overall hybrid circuit, such as a VLSI chip and a gate array, are wire-bonded to the small substrates (½-in. square), which have 3-mil conductors and spaces and deposited thin-film resistors. These subassemblies are tested and then scribed apart.

The smaller thin-film substrate is then mounted and wire-bonded onto a larger, multilayered thick-film substrate, which contains mainly passive components and an interconnection pattern. In essence, the subhybrid is the most difficult part of the overall hybrid. This mixed technique allows a manufacturer to integrate the best features of thick films (multilayering) and thin films (fine lines) into his hybrids.

Circuit Technology Inc., Farmingdale, N. Y., uses a similar approach in a special hybrid implementing a MIL-STD-1553B function. A custom VLSI chip designed by CTI is die- and wire-bonded to its own small, thin-film substrate, a sort of thin-film chip carrier, and this in turn is wire-bonded to a larger thick-film substrate that contains the rest of the circuit's active and passive elements (Fig. 3).

Thin-film hybrids have certain disadvantages. First, they are more expensive to make. Second, until recently, multilayer thin films weren't attainable because there was no sputterable dielectric material. However, over the past three to four years, Honeywell Inc., IBM Corp., and several Japanese firms have made experimental thin-film multilayered substrates with polyimide insulating layers.

This technique is now diffusing down to thin-film hybrid processing firms. Tektronix, for example, is already offering two-layer thin-film hybrids based on polyimide insulating layers and is actively working to extend this technique. Lockheed Electronics Co., Plainfield, N. J., has made experimental thin-film substrates with three conductive layers. This technique, which was first used in IC processing, bears further watching because it could allow thin-film hybrids to make even further inroads into the thick-film-hybrid market.

While thin-film technology looks to snare some of thick film's market, a competitive technique—semiadditive electroplating of fine copper patterns—has arisen and is looking to cut into thin-film applications.

COPPER-PLATED CERAMIC

The process is called Ceraclad and is now going into production. It was developed by the PCK Technology Division of Kollmorgen Corp., Melville, N. Y. The Ceraclad process can put down 2-mil-wide pure copper traces (Fig. 4) on ceramic materials such as alumina, beryllia, aluminum nitride, and silicon carbide at a lower cost than that of a thin-film process. In addition, the process can produce 3- to 5-mil-diameter plated

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through-holes, allowing the equivalent of a two-sided thin-film hybrid.

The electroplated copper results in excellent thermal conductivity, necessary for good bonding or soldering, and a high electrical conductivity (low resistance). The pure metal surface gives a bonding strength equal to that of thin films and much higher than that of thick films. The process results in smooth vertical side walls on conductors, resulting in better signal propagation at high frequencies. Finally, the pure copper trace is extremely smooth and glass-free, which makes it a suitable low-loss conductor for microwave applications.

PCK uses a semiadditive plating process for patterning a Ceraclad substrate. First, the alumina substrate is activated with a special seeding material, and then a 0.1-mil flash pattern of electroless copper is put on. Next, a film photoresist is laminated onto the substrate, and the resist is imaged and developed. The exposed areas are then electroplated up, and the unwanted resist and copper flash are etched away.

Don Freed, general manager of the Ceramic Technology Group of PCK Technology, already sees the impact of Ceraclad in three areas. One is as a direct replacement for thin-film hybrids; the second is in chip carriers, particularly those requiring very fine line pitches; and the third is in microwave ICs. PCK has already licensed this process to six companies in Europe, Japan, and Australia, and is delivering products to 15 U. S. firms. One of the companies is RCA's Government Systems Division, which is evaluating the technique for a fine-line hybrid that has circuitry on both sides of a substrate interconnected with plated through-holes.

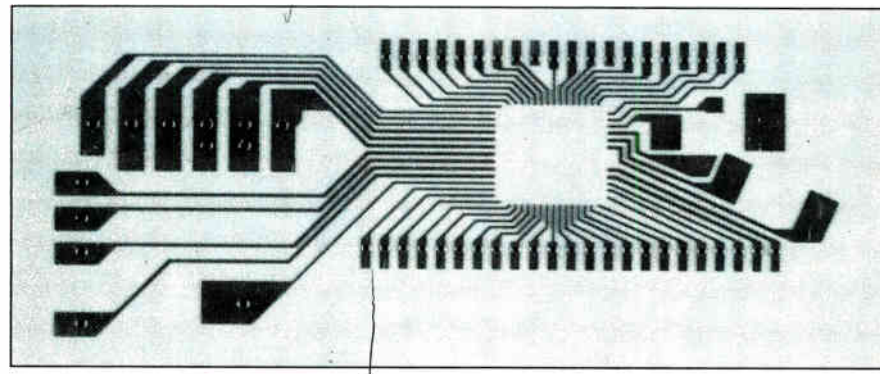
POWERED UP

Along with the surge in thin-film hybrids, the thick-film power hybrid area is also expanding. For example, Mel Spitz, vice president of marketing at Circuit Technology, estimates that 10% of his company's thick-film hybrids are now power hybrids. At ILC Data Device, a separate department with its own thick-film line has been set up for power hybrids. In fact, most hybrid firms are either investigating or starting to manufacture power hybrids.

The demand for power hybrids has been brought on mainly by two factors. The first is the military's push for miniaturization, which dictates that power amplifiers, voltage regulators, and all types of high-power analog circuitry be compressed into tiny packages. A second factor is that today's VHSIC and VLSI chips dissipate from 1 to 5 W apiece, and when many of these chips are jammed into a small substrate, a power hybrid results. A conventional hybrid might dissipate up to 5 W, while a power hybrid can dissipate more than 100 W. But the real difference between a power hybrid and a standard hybrid, according to Haim Taraseiskey, engineering manager for power hybrids at ILC Data Device, is the nonconventional assembly techniques needed to get good thermal conductivity out of the power hybrid.

HANDLING THE HEAT

For example, power hybrids usually have beryllia rather than alumina substrates because of beryllia's better thermal conductivity. Power hybrid packages must provide an efficient thermal transfer from the heat-generating semiconductors (typically power transistors, FETs, diodes, silicon controlled rectifiers, and so forth) to the system heat sink. Three packages are in general use: solid copper machined packages with soldered-in terminals; a Kovar ring frame with matched glass-to-metal sealed leads brazed to a molybdenum bed; and the second package with a beryllia substrate instead of the molybdenum bottom.



4. CERACLAD. In PCK Technology's Ceraclad process, extremely smooth 2-mil copper traces are semiadditively plated to a ceramic substrate.

Special high-temperature solders are needed for attaching dice to the beryllia substrate and the substrate to the case. And to handle the large currents passing through a power hybrid, up to 25-mil wire must be bonded (requiring special bonders) rather than the 1- or 2-mil wire of a standard hybrid.

Power hybrid assembly requires special beryllia oxide substrates, solid copper machined packages, 25-mil wire bonding, and special high-temperature solders

Power hybrids run the gamut from the very simple—such as four power MOS FETs (Fig. 5) in a bridge for a motor driver—to the complex—such as a unit for a three-phase brushless motor controller with a multilayer alumina substrate carrying the low-level circuitry plus three separate beryllium substrates for the power electron-

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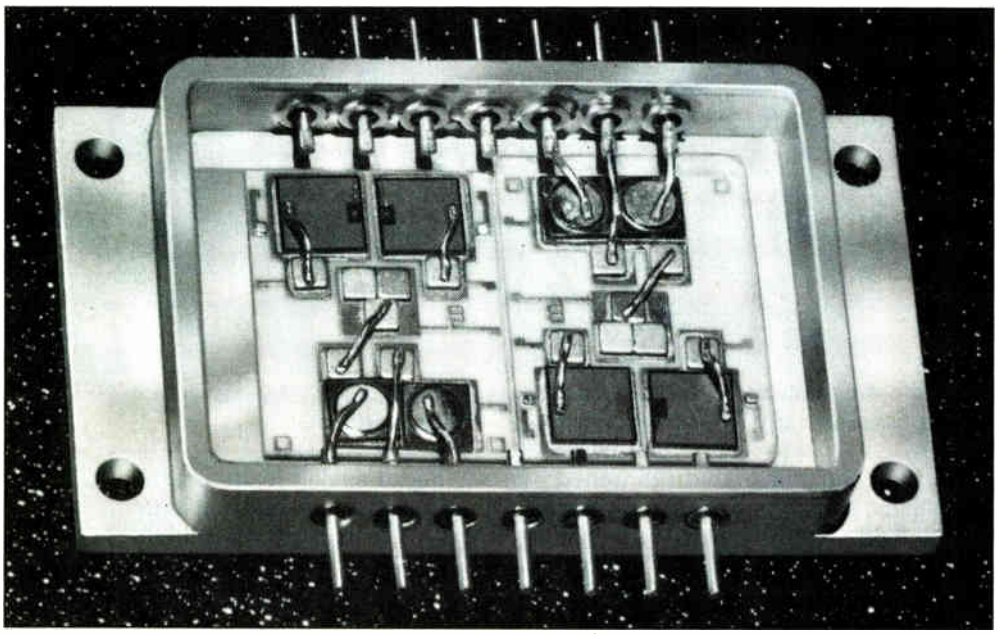
ics, each composed of a power MOS FET and a power Darlington. In the commercial field, cars and solid-state relays are full of power hybrids.

While some companies have been installing in-house hybrid facilities, other firms with well established in-house expertise in hybrid fabrication decided to venture into the independent custom hybrid market. Among these were Tektronix, Lockheed Electronics, and Gordos at its Rogers, Ark., facility.

HYBRID KNOW-HOW FOR SALE

In 1984, Tektronix decided to go into the custom hybrid business, applying its many years of in-house experience on the many types of hybrids that had been designed and built for its oscilloscopes, instruments, and automatic test equipment. The Beaverton, Ore., company had a set of hybrid capabilities—an ability to manufacture thick films, thin films, and high-frequency and power hybrids. In addition, the company has a large CAD/CAE base that can both lay out a hybrid design and analyze its thermal parameters.



5. POWERED UP. ILC Data Device Corp.'s power hybrid has four power MOS FETs that dissipate a total of 150 W, and they are soldered to a beryllia substrate brazed to a copper case.

At first, Tektronix wanted to concentrate on commercial custom hybrids, but it could not ignore the large military market. The company is now doing some military work and is seeking Pentagon qualification for the latest military standard for hybrids—MIL-STD-1772. So far, only ILC Data Device and Teledyne Microelectronics have been certified.

In May 1986, Tektronix opened a multilayer cofired ceramic facility. A cofired substrate consists of sheets of green ceramic with circuit patterns screened on, formed into a monolithic block, and fired. This plant will produce cofired ceramic substrates for hybrid and IC packages. Tektronix is already producing a 264-lead chip carrier with a 20-mil pitch and a characteristic impedance of 50 Ω using a cofired substrate for a VHSIC subcontract.

Through its instrument design, Tektronix has made many electro-optical hybrids (those with electro-optical components such as light-emitting diodes, lasers, fiber-optic components, and so on) and is now pursuing this field to the point of setting up a separate organization for it. In fact, the company's hybrid operation plans to make commercial-standard electro-optical products.

Lockheed Electronics, like Tektronix, has both a thick- and thin-film capability and a CAE facility based on an Applicon system, but its output is almost 100% military. Currently, 70% of its work is for Lockheed divisions, and 30% is for such outside firms as General Dynamics, Harris, and Raytheon. "Our aim is to get this ratio to 50 : 50," says Joseph Iervolino, director of hybrid microelectronics. Like other companies serious about military hybrids, Lockheed is waiting to be certified for MIL-STD-1772.

Lockheed Electronics does both chip-and-wire and surface-mounted thick-film hybrids and has done many thin-film microwave circuits. An example of Lockheed's design capability is a recent thick-film design for use aboard a military spacecraft. This hybrid successfully completed a test at –95°C. Special selection of thick-film materials and IC chips made this difficult task possible.

Back in the earthbound world, Lockheed Electronics recently reduced one customer's circuitry for an Intel Corp. bubble-memory board from a 5-by-9-in. pc board to a 1-by-1-in. thick-film hybrid.

Not only the industry giants are following this trend. In June, Gordos Corp., a medium-size producer of relays, solid-state relays, and power I/O modules, decided to market its power hybrid capability because of the several-hundred-million-dollar potential of this particular hybrid market segment. Gordos has accumulated six years of experience on commercial/industrial thick-film solid-state relays and has recently hybridized its electromechanical power I/O modules used in industrial automation and control.

Because many other companies either already have extensive in-house thick- and thin-film facilities or are installing them for such specialized circuitry as the pin electronics of VLSI automatic test equipment, the ranks of custom hybrid suppliers should grow. □

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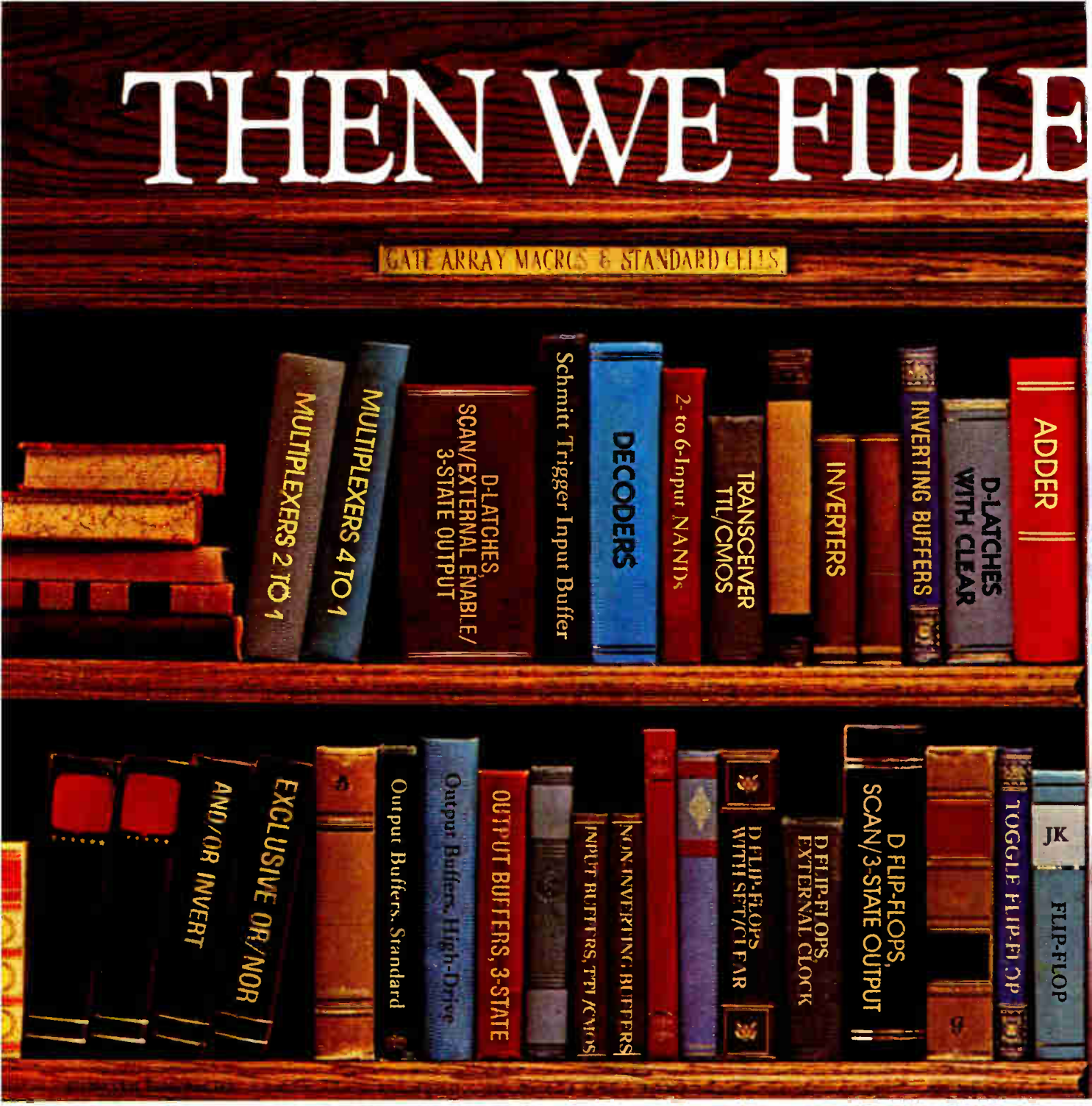

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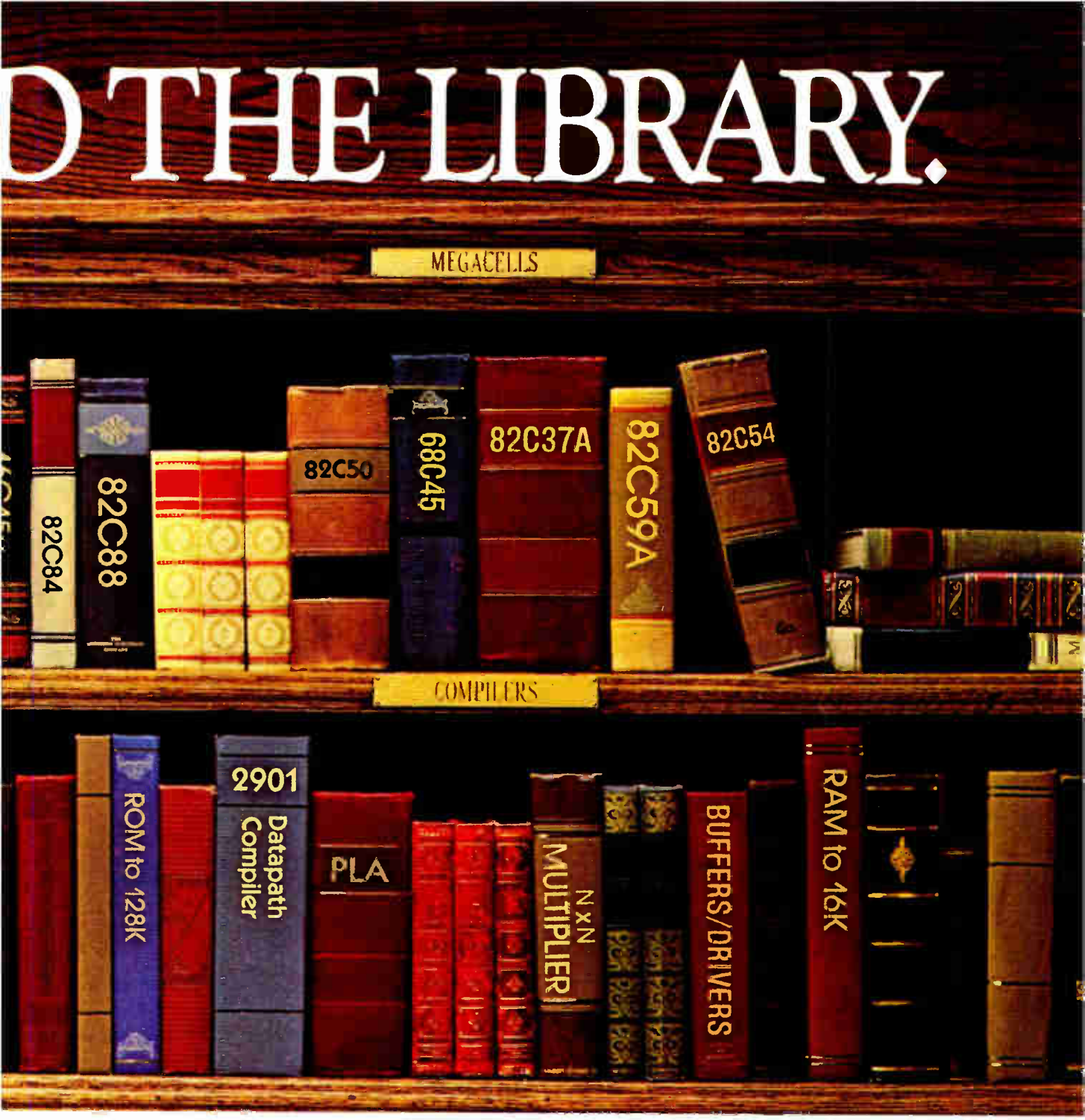

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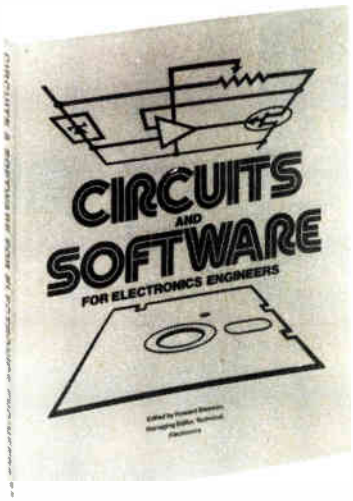

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NOW 3-D CAD IMAGES CAN BE MOVED IN REAL TIME

At the heart of a new HP work station is a chip set that can compute realistic 3-d color images fast enough to manipulate them in less than a second

Work-station vendors have an ambitious goal: a solids-modeling capability that lets designers zoom, pan, and rotate a color three-dimensional image with complete shading and illumination around all its axes in real time. One work station that comes closer to realizing this ambition than anything so far is Hewlett-Packard Co.'s new HP320SRX. HP's Fort Collins (Colo.) Systems Division designed a set of very large-scale integrated circuits that compute realistic 3-d images fast enough for the operator to manipulate them and see the results in less than a second.

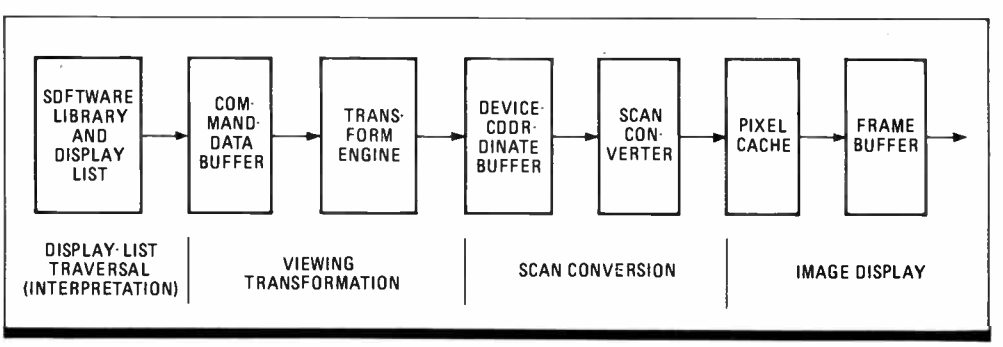
Up to now, a graphics work station could not move such an image in real time. It could only move a wire-frame 3-d image in real time and then turn this skeleton into a shaded, colored 3-d image. Rendering the final image could take upwards of 60 seconds on some systems.

HP's 320SRX is a bundled work-station system that includes a general-purpose 16-MHz MC68020 32-bit central processing unit with an input/output expander, a 16-K-byte high-speed cache, a 16-MHz 68881 floating-point coprocessor, 4 megabytes of RAM, a high-speed IEEE-488 bus, direct-memory addressing, a local-area network, and a display with a 1,280-by-1,024-pixel monitor.

The new HP work station includes eight planes of frame-buffer memory and four overlay planes. Another 16, 24, or 32 planes of graphics memory can be added. It comes with the HP-UX operating system and associated graphics libraries.

To create a 3-d image on a cathode-ray tube, a designer uses a large set of graphics primitives. In drawing a car, for example, the designer uses a set of circles to draw a wheel and a hexagon to draw a lug nut. When he creates a graphics construct of a lug nut, he specifies that it is to be drawn five times at five different locations on the wheel. Likewise, he specifies that the completed image of the wheel is to appear four times in the larger image of the car.

There are many of these lower-level graphics primitives in the larger image of the car. Associated with each of these constructs is a transformation matrix. It contains 16 real numbers arranged in an array of four entries by four entries. These entries store the information re-



1. UPSCALE. HP has enhanced each stage in the graphics pipeline of the HP320SRX work station to handle 3-d graphics processing.

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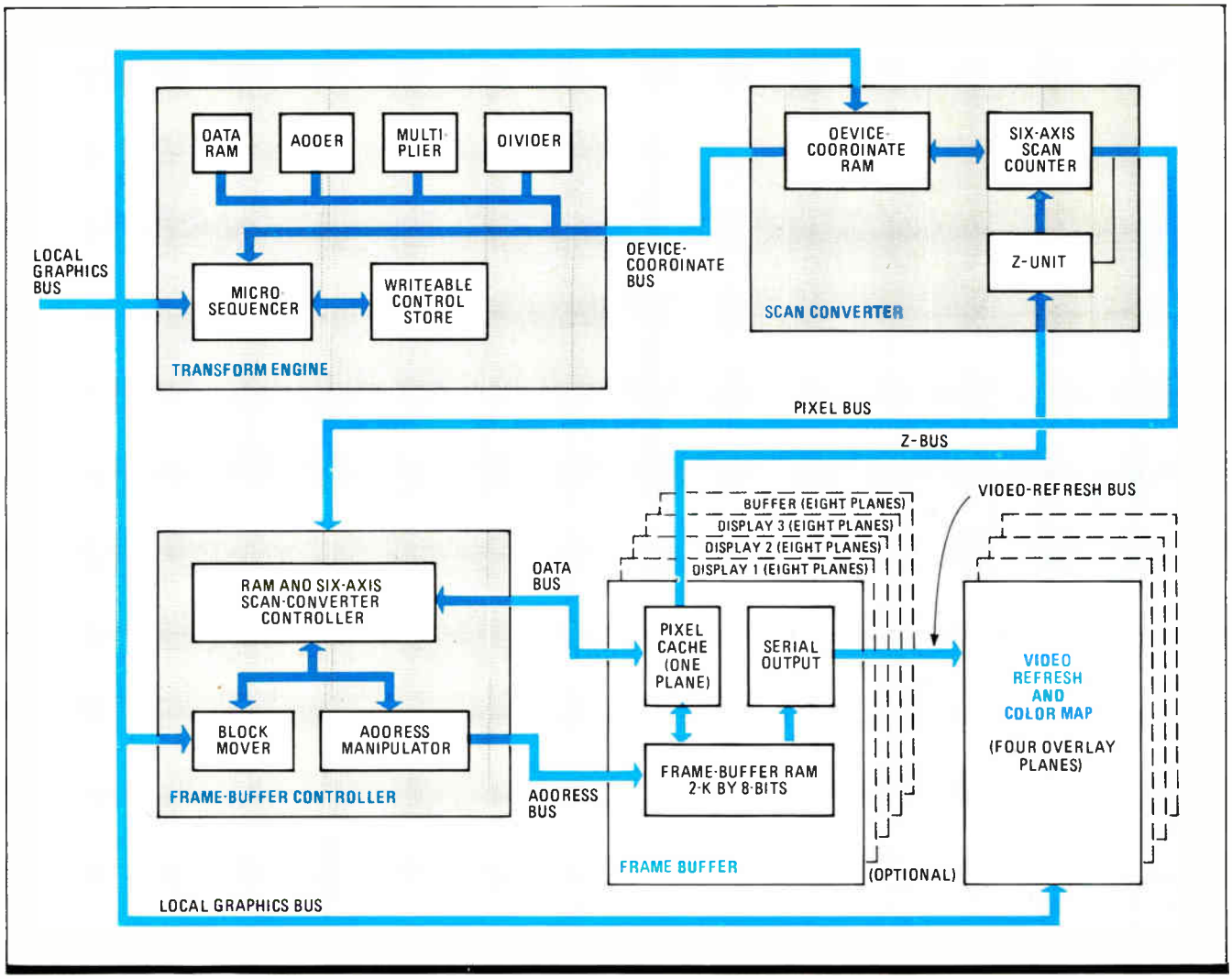

2. FILLING IN. HP designed six VLSI chips to take care of most of the tasks required to create and manipulate a color 3-d CRT drawing. The six are the scan converter, the adder, the multiplier, the divider, the pixel cache, and the video-refresh shift register.

quired to scale, rotate, translate, shear, and apply perspective to the individual graphics constructs. Any time the image is drawn or redrawn, each of these four-by-four matrices are transformed, and millions of mathematical calculations are required for each image displayed on the work station's CRT. In rotating the image of an automobile, for example, each step in the rotation represents a complete frame of data that must be calculated.

To display the image on the screen, the transform engine translates the display list, the collection of graphics constructs that define the image to be displayed, from the modeling coordinate system to the device coordinate system of the CRT. The transformation matrix for each graphics construct is scaled, rotated, and clipped to fit into the device coordinate system. Each graphics construct, such as a lug nut and a wheel, must be created and placed correctly relative to one another in the larger image.

HP's 320SRX work station is built on a traditional pipelined graphics architecture (Fig. 1). The four stages of this architecture—display-list traversal (interpretation), viewing transformation, scan conversion, and image display—are separated by dual-port memory, through which commands and data are passed. The dual-port memory allows each stage of the pipeline to operate independently to optimize performance.

HP's six custom VLSI chips are used in three of the four stages of the pipelined graphics architecture (Fig. 2). The most important of the new ICs is the scan converter, which can do the many high-speed calculations necessary to depict a solid image. The transformation engine has three custom ICs that speed through the arithmetic operations necessary to transform an image. The other custom chips are the pixel cache, which is part of the frame buffer, and a high-speed shift register.

"A key part of the new HP work station is a new custom n-MOS IC for scan conversion," says Warren Pratt, research and development manager of HP's Technical Work Station operation. "It provides high-speed conversion by solving simultaneous Bresenham algorithms on six axes. Conventional hardware implementations of the algo-

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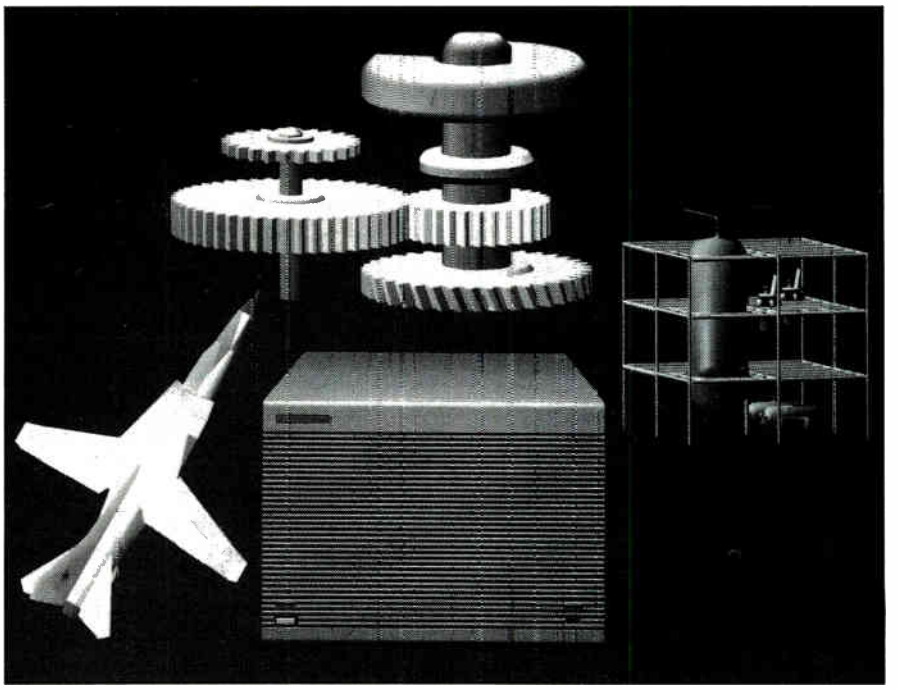
rithm deal with only two or three axes at the most, X, Y, and Z."

Named after IBM scientist J. E. Bresenham, the simple, line-drawing algorithm takes the two end-point values of a line and interpolates to find every pixel in between that must be lit to draw the line. It is well suited to hardware implementation because it avoids division or multiplication in interpolating between points on a line.

The scan converter must work with the output of the transform engine, which is an image defined entirely by end points. If one surface of an image being drawn resembles a quadrangle, say, the scan converter gets four end points defining its four vertices. It then connects the four points together. To shade the surface, the scan converter draws a set of closely spaced lines between end points of the surface. The process is analogous to the way that a pen plotter fills an area.



3. SMOOTHIE. The HP320SRX manipulates 3-d color images as smoothly as other work stations manipulate wire-frame images.

"In the HP implementation, the Bresenham algorithm has been extended," Pratt explains. "The scan converter accepts line and polygon information and not only interpolates the X-Y-Z coordinates for each pixel but also calculates the red, green, and blue values for each pixel. Computations on all six axes are done in parallel to allow the work station to produce smoothly shaded polygons with Z data for hidden-surface removal at a data rate up to 16 million pixels per second. Convex or concave polygons with up to 255 sides (including holes) can be rendered by the VLSI scan converter."

When the six axes are active, the scan converter performs over 300 million additions per second. To achieve such performance, it is implemented in HP's proprietary n-MOS III 1-μm technology. "The chip provides a 15-times performance improvement over a discrete implementation and orders-of-magnitude performance improvement over a general-purpose processor," Pratt says.

Also part of scan conversion, the Z unit uses a Z-buffer algorithm to remove hidden surfaces. It examines the Z-axis value—the depth of a 3-d image—and compares it with the value of adjacent pixels. If the new value is greater than the adjacent values—indicating the current pixel is located behind the adjacent pixels, the hardware does not compute the value but rather discards the pixel—that is, it removes a hidden surface.

Hardware Z buffers offer several advantages. First, polygons can be rendered in any order, eliminating the need for time-consuming depth sorts that arrange pixels in order of their depth on the CRT screen. In addition, "there is a no restriction on the complexity of a scene, as the depth comparison is done in the coordinate system of the CRT screen," says Pratt. "Complex or intersecting polygons are handled no differently than other objects. Finally, performance is kept at a maximum even as the number of objects in the scene increases." The computation associated with Z-buffer hidden-surface removal increases linearly in the worst case because the size of the image space—the number of pixels that can be displayed on the CRT—is fixed.

In the transform engine, a set of three custom ICs performs addition and subtraction, multiplication, and division. The chip set provides substantially lower cost than commercially available alternatives. The 1-μm n-MOS parts include the divide function, which only now is becoming available on other chip sets. The HP chips can perform a variety of 32-bit IEEE floating-point and fixed-point operations at a rate up to 9 million floating-point operations per second.

The scan-converter IC produces RGB values plus X-Y-Z coordinates for each pixel. It's 15 times faster than discretes that handle only the X-Y-Z axes

"Rendering features are implemented in microcode" in the transform engine's chip set, says Pratt. "They include enhancements for the smooth Gouraud shading to add multiple light sources, and Phong lighting models to provide specular highlighting. Ambient, positional, and

World Radio History

infinite light sources may be defined either as white or colored lights. Up to seven positional sources of light may be defined. Light calculations include ambient illumination, diffuse reflections, and positional sources with distance and spotlight effects."

Adding light-source information to the end-point data produced by the transform engine is a matter of calculating the intensity of color for a given end point—assuming a light source placed at some point around the object. When light sources are added to the image, the image initially contained in the display list in the modeling coordinate system is transformed into the world coordinate system.

CONVERTING COORDINATES

Converting to the world coordinate system entails fixing a point relative to the image at which a light source can be located: five feet above the object, for instance, or a foot below. In this way, the transform engine's lighting algorithm can calculate the intensity of each pixel relative to that light source. These end points with light-intensity data embedded are then passed to the scan converter, which interpolates intermediate pixels and resulting color using the light-intensity data.

Another function of the transform engine is back-facing polygon culling. It examines an object, such as a cube that has three faces showing and the others hidden. The unseen faces are culled or discarded and their associated end-point data is not sent to the scan converter. "By quickly eliminating many of the completely hidden polygons in a scene, this back-face cull improves throughput of the pipeline," Pratt explains.

Another chip built for the work station is a semicustom CMOS IC called the pixel cache, part of the image-display stage of the pipelined architecture. Implemented in HP's 1.6-μm CMOS technology, the chip is the primary data manipulator for the work station's frame buffer. A pixel cache functions in the same way that a memory cache does in traditional computers. In the HP320SRX, it balances the bandwidth between the high-speed scan converter and the slower frame buffer. "Data leaving the scan converter accesses the pixel cache at a 16-ns access rate," says Pratt. "By contrast, the frame buffer has a much longer 360-ns access rate."

A feature of the frame buffer is double buffering, which enables the designer to produce realistic animation sequences. Applications may display one portion of the frame buffer while the other portion is being updated. When the updating is completed, the buffers' roles are reversed. The picture appears to be updated instantaneously.

The final custom chip is a 108-MHz video shift register, also fabricated in the HP 1.6-μm CMOS technology. It serializes incoming pixel data from the frame buffer and produces a video bit stream for the color map subsystem.

Taken together, these chips raise the performance standard for solids-modeling applications. They also help keep the cost of the HP 320SRX work station down to the level of systems that can manipulate only wire-frame 3-d images. □

HOW CUSTOM ICs GOT HP INTO HIGH-PERFORMANCE GRAPHICS

When Hewlett Packard Co. formed a design team to investigate work-station architectures in 1984, it was looking for a route it could take to enter the high-performance graphics business. "The team's goal was to push HP into the forefront of the marketplace," says Warren Pratt, research and development manager of HP's Technical Work Station operation in Fort Collins, Colo.

The team, under Pratt's direction, soon decided that the most glaring deficiency in current work stations was their inability to move solid 3-d models in real time. Most of HP's competitors were using floating-point data-path chips to do the image creation and manipulation, and they weren't fast enough for real-time work. Others were developing custom chips, but they were not achieving significant speed hikes.

HP decided to build its own set of integrated circuits that would speed up the pipeline in the graphics work-station architecture. The chip set would give the new HP work station a speed advantage over work stations using off-the-shelf components. In addition, HP could compete against work-station makers with their own chips by coming out with a next-generation set of ICs.

Of the six chips that provide the work station with its high performance, the multiplier, divider, adder, and scan converter were fabricated in the company 1-μm n-MOS process. "We expect to convert this to a CMOS process in time," Pratt says. The other two chips, a pixel cache and video shift register, were implemented in 1.6-μm CMOS.

HP did the work station design in 17 months. "The product definition was refined over time, but the schedule didn't change," says Pratt. "What contributed to the rapid product development was the use of HP's own CAE DesignCenter tools in building the six proprietary chips and pc boards for the system.

"There were 60 people associated with getting this product to market on time," he says. "It's an HP tradition that when we develop new products, we try to make a contribution to the technology. In this product, with its large improvement in performance over what currently exists, we think we have kept faith with this tradition."

WARREN C. PRATT

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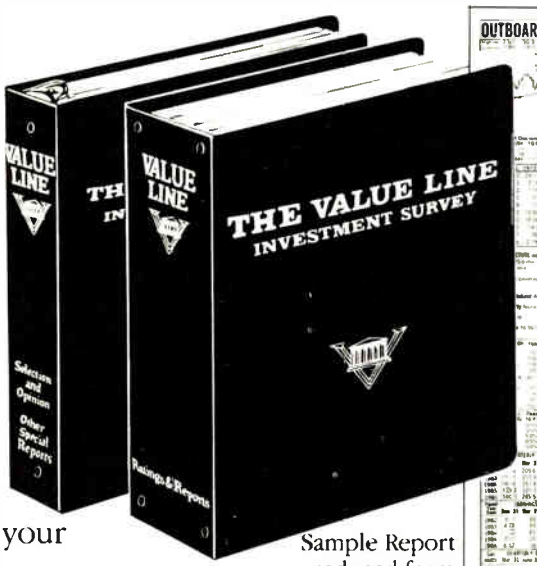

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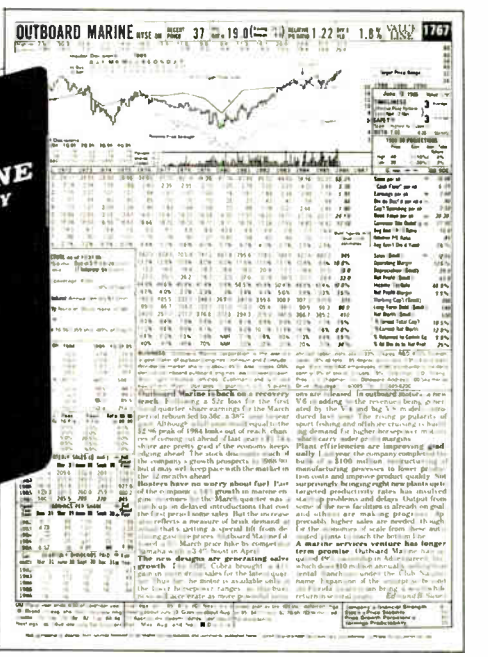

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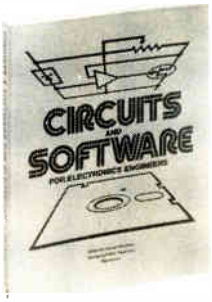

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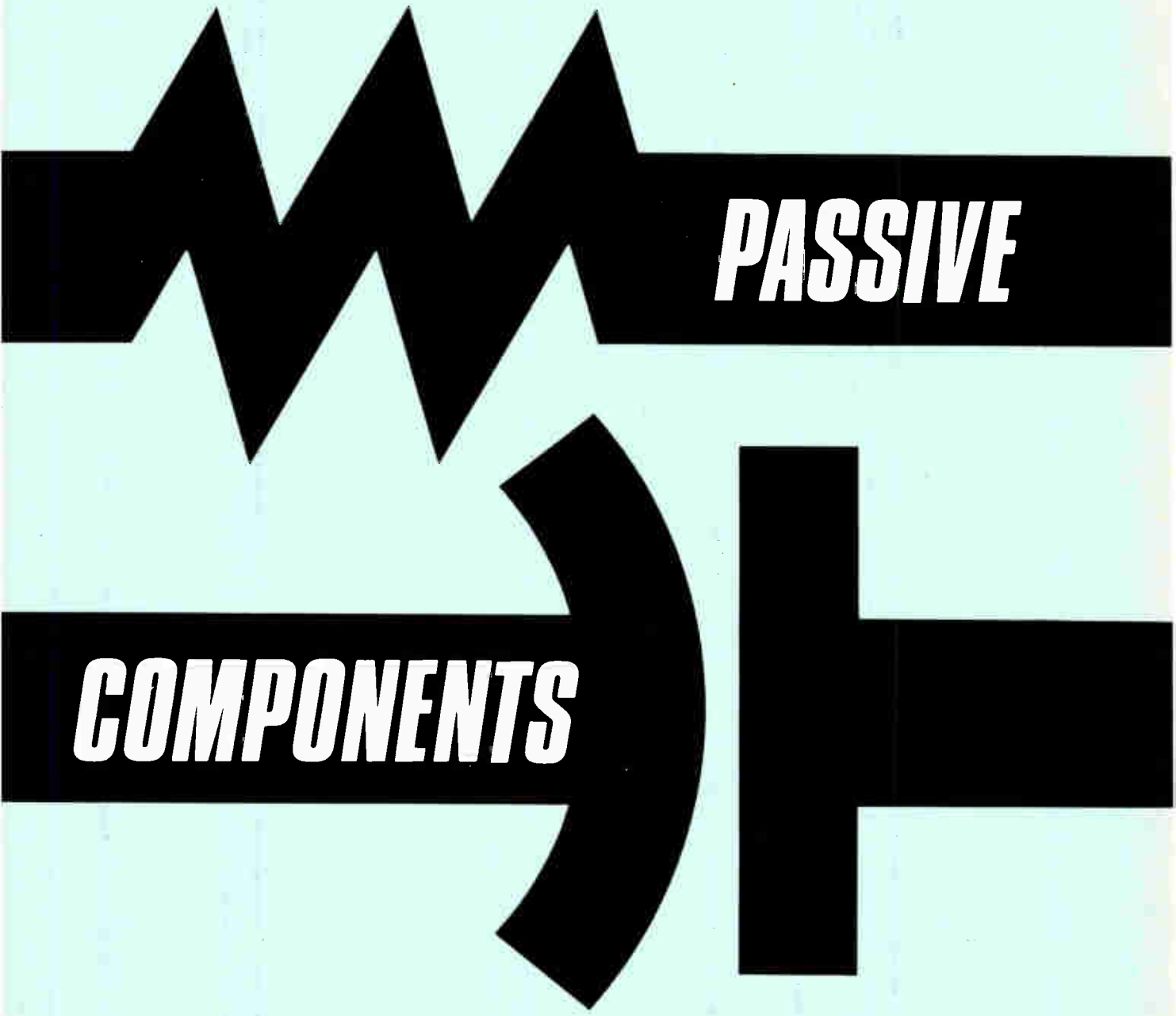

Electronics SPECIAL ADVERTISING SECTION

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Surface mounting makes gains in a so-so market

By the second half of the year, U. S. consumption of passive components should be on the upswing once again. The 26% jump in consumption of passives in 1984 was not the start of a trend. In 1985, the sector took a nosedive as equipment manufacturers worked off swollen inventories, and the year ended with a meager 2% growth.

Through the rest of this year, however, the market should come alive as customer orders start coming in. At the same time, prices should rise as lead times for deliveries stretch out and systems makers clamor for parts.

Mostly good news

Sales of relays, switches, connectors and integrated-circuit sockets, capacitors, and resistors all will increase this year over 1985, according to market researcher Gnostic Concepts Inc., San Mateo, Calif. Connectors and IC sockets along with capacitors are the best bets for growth in the category this year and next. Overall, passive electromechanical components, including printed-circuit boards, will climb from $11.6 billion in 1985 to $12.3 billion this year and will move up to $13.4 billion in 1987. Pc boards will come in at almost $4.3 billion this year, says Gnostic Concepts.

One of the real bright spots is surface-mounted devices. Market projections by Electronic Trends, a Cupertino, Calif., market researcher, indicate that more than 41% of all passive components will be in the form of SMDs by 1990. An Electronic Trends study also projects that by 1990 more

Yugoslavia's Iskra introduces two families of metalized capacitors

Iskra Electronics Inc., a Yugoslavian electronics manufacturer whose U. S. headquarters is in Farmingdale, N. Y., has added two new families of capacitors to its product line—metalized polyester-foil capacitors and metalized radio-interference capacitors.

The radial-type metalized polyester-foil capacitors come in a wide range of sizes with lead spacing down to 5 mm. The KEU 1943, a capacitor with 5-mm spacing, is designed for manual or automatic insertion. It comes in a capacitance range of 0.001 μF to 1 μF, 50 V, 63 V, 100 V dc, or 30 V, 40 V, or 63 V ac. Its temperature range is −55°C to +100°C, and its case material is self-extinguishing, in accordance with UL 94 U-O.

Iskra's metalized radio-interference capacitors—KNB 1530, 1531, 1532, and 1533—have a dielectric of metalized polypropylene foil with self-healing properties at puncture. For protection against climatic and mechanical influences, the very low-inductance capacitor winding is enclosed in a self-extinguishing thermoplastic case that is sealed with an artificial resin.

The devices recently were approved for UL 1283 filter applications. UL 1414 approval is pending. They comply with VDE 565-1 for Class X2 suppression capacitors. The capacitors are available with different lead lengths and types of connecting terminals for printed-circuit boards and other applications. Typical targets for these capacitors include switched-mode power supplies, clock generators, thyristors, commutator motors, and various electronic ignition systems.

Iskra, a $2 billion concern with 13 divisions and over 80 plant locations in Ecuador, Switzerland, Turkey, and Yugoslavia, maintains a warehouse in Farmingdale and a branch office in Santa Clara, Calif. It produces a wide range of products, including resistors (metal- and carbon-film resistors, chips, precision resistors, networks, trimmerpots), rectifier diodes, bridges, and custom-designed microelectronics. Five of its production facilities manufacture capacitors. The company also produces telecommunication, computer, electro-optic, electromechanical, and test equipment as well as consumer products.

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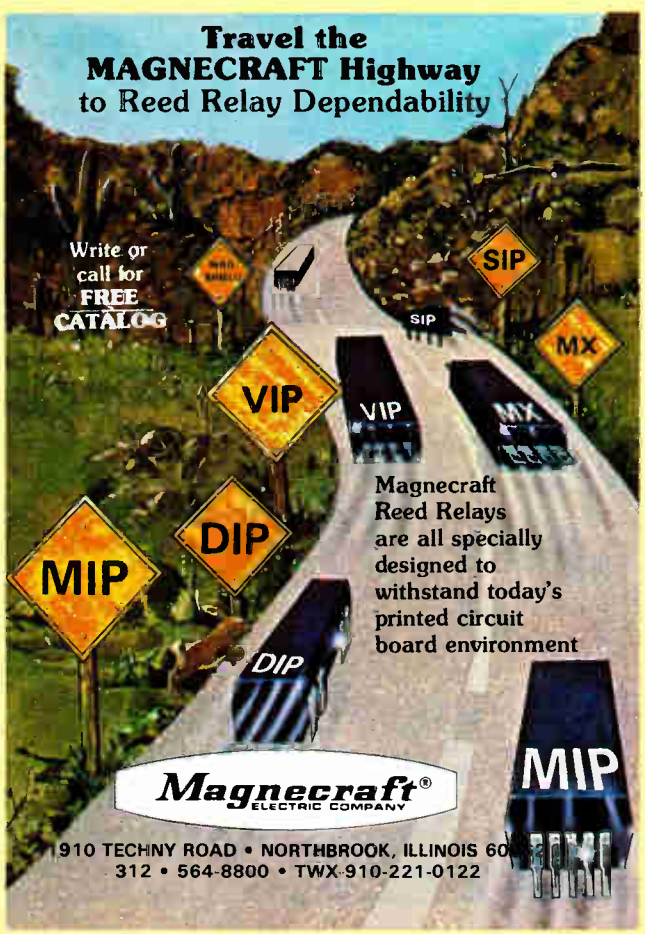

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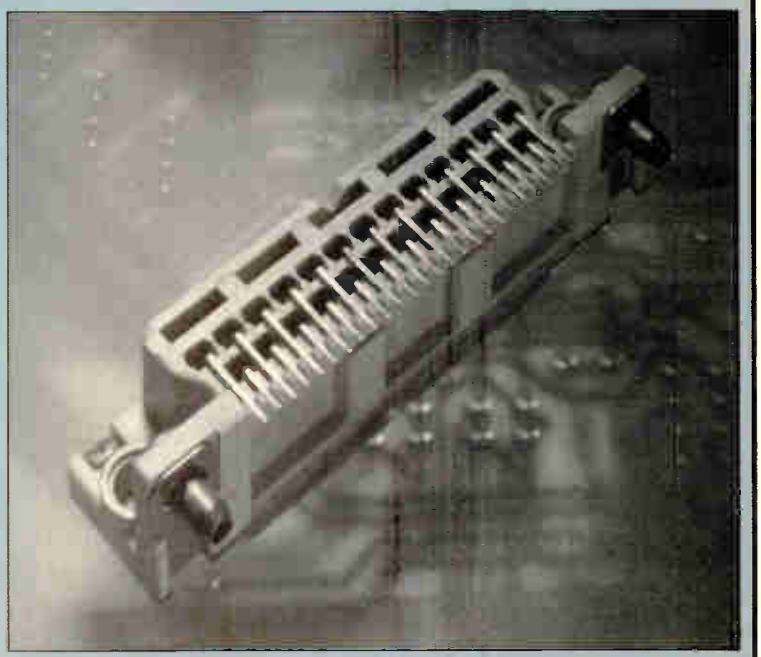
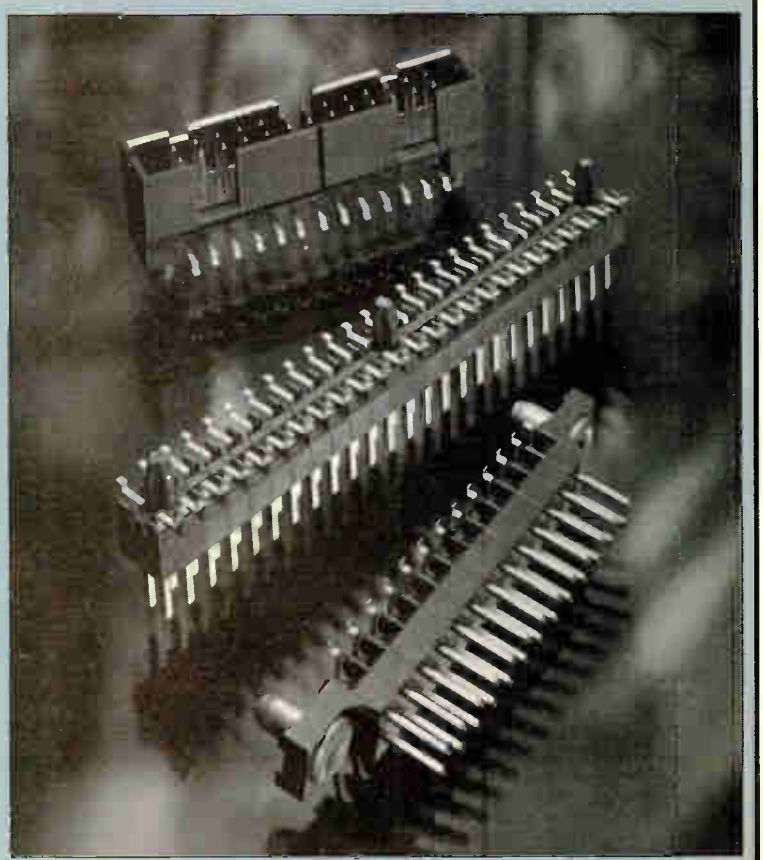
than half the pc-board assemblies for electronic equipment will contain SMDs, both passive and active. Indeed, while other sectors were struggling, surface-mounted components have been making quarter-to-quarter sales gains of 10% to 20%. One reason for these increases is that more companies, especially large ones, are getting involved in the technology and are working hard to develop products. The

Amp packages surface-mounted connectors for robotic handling





While some component market segments have been slow to grow, surface-mounted connectors continue to gain in sales—encouraging news for manufacturers such as Amp Inc. The Harrisburg, Pa., company, which has been researching surface-mount technology for several years, recently developed new connector and packaging techniques for use with robotic and other advanced handling systems. In fact, each of its 17 operating divisions has an active surface-mount program supported by Amp's Technology Division.

Beneath the company's efforts is the belief that robotics is one of the keys to cost-effective surface mounting. Thus its surface-mount devices have locating and orienting features along with features to ensure proper gripper manipulation and integration with other components and subsystems. They are packaged and shipped in reels, trays, or tubes designed to properly feed robotic work stations. Indeed, Amp's stress on the importance of robotic packaging goes further: it has many products that are not surface-mountable yet are designed for robotic application.

Among Amp's newest surface-mountable products designed and packaged for robotic handling are its Amplimite subminiature D connectors. Available with tin-plated steel shells in sizes 1 through 4 with 9, 15, 25, or 37 contacts, these right-angle plugs and receptacle connectors have mechanical hold-down features to accurately secure the temperature-resistant housing in place; the tin-plated leads solder to the printed-circuit-board pads in a single row for easy visual inspection.

Amplimite connectors are suitable for front-to-back, side, or top gripping. They come in single tubes, multitrack tubes, and multitrack trays or on tape. Amp also has robot feeders and grippers.

In addition, the company is offering Ampmodu double-row headers for surface mounting in board-to-board and wire-to-board applications. These connectors have locating features for robotic handling. They are compatible with standard dual-row, 0.025-in.^{2} post connectors on 0.100-in. centerlines and range in size up to 60 contact positions. Because the structure is compliant, it can withstand stress at the solder joint.

Both the shrouded and unshrouded versions of the headers have mechanical hold-down features to secure the connector in position before solder reflow. All materials are compatible with infrared and vapor-phase reflow soldering, according to the company.

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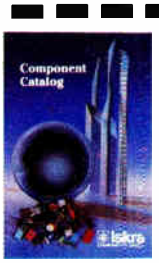

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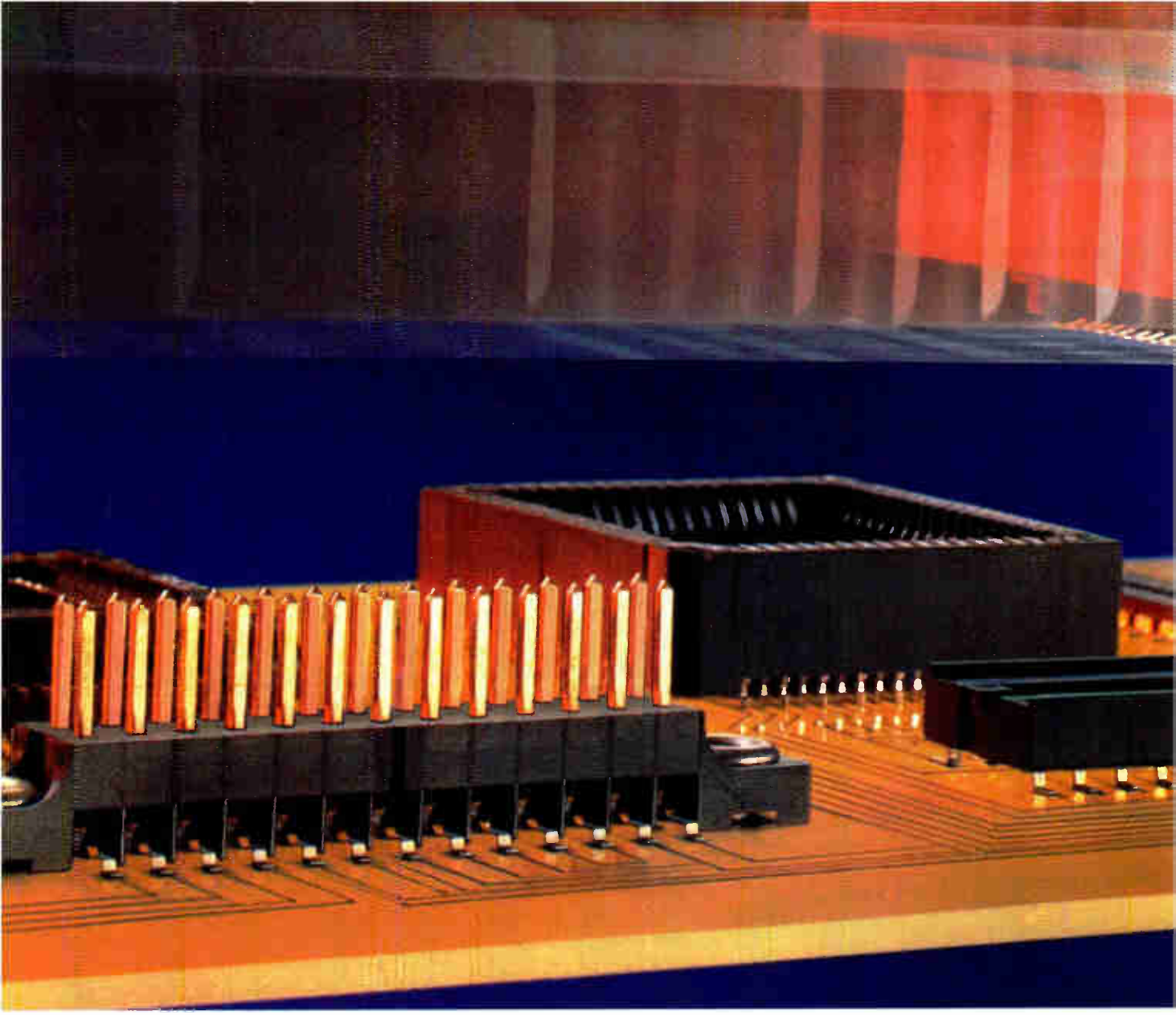

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Technologies expand—and pay off—when they get in-depth support.

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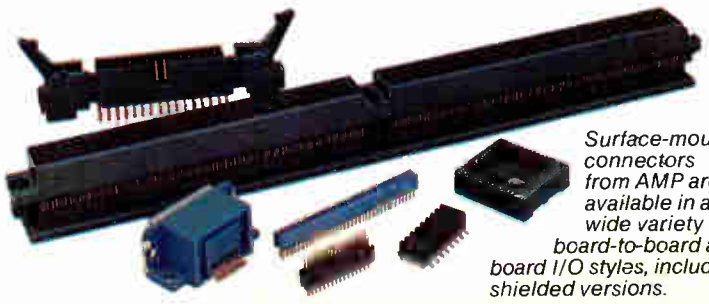
For instance, many of our SURMOUNT products are designed for flexible automation. Robotic systems offer fast production changeover via programming control. And we offer what you need to make it work: feeder and positioning equipment, and a variety of compatible packages, from tape and single tubes to stacking, multi-track trays.

All SURMOUNT products are in tested materials, naturally. Plastics and platings developed to withstand the process conditions of surface mounting. Because the technology is developing,



Surface-mount connectors from AMP are available in a wide variety of board-to-board and board I/O styles, including shielded versions.

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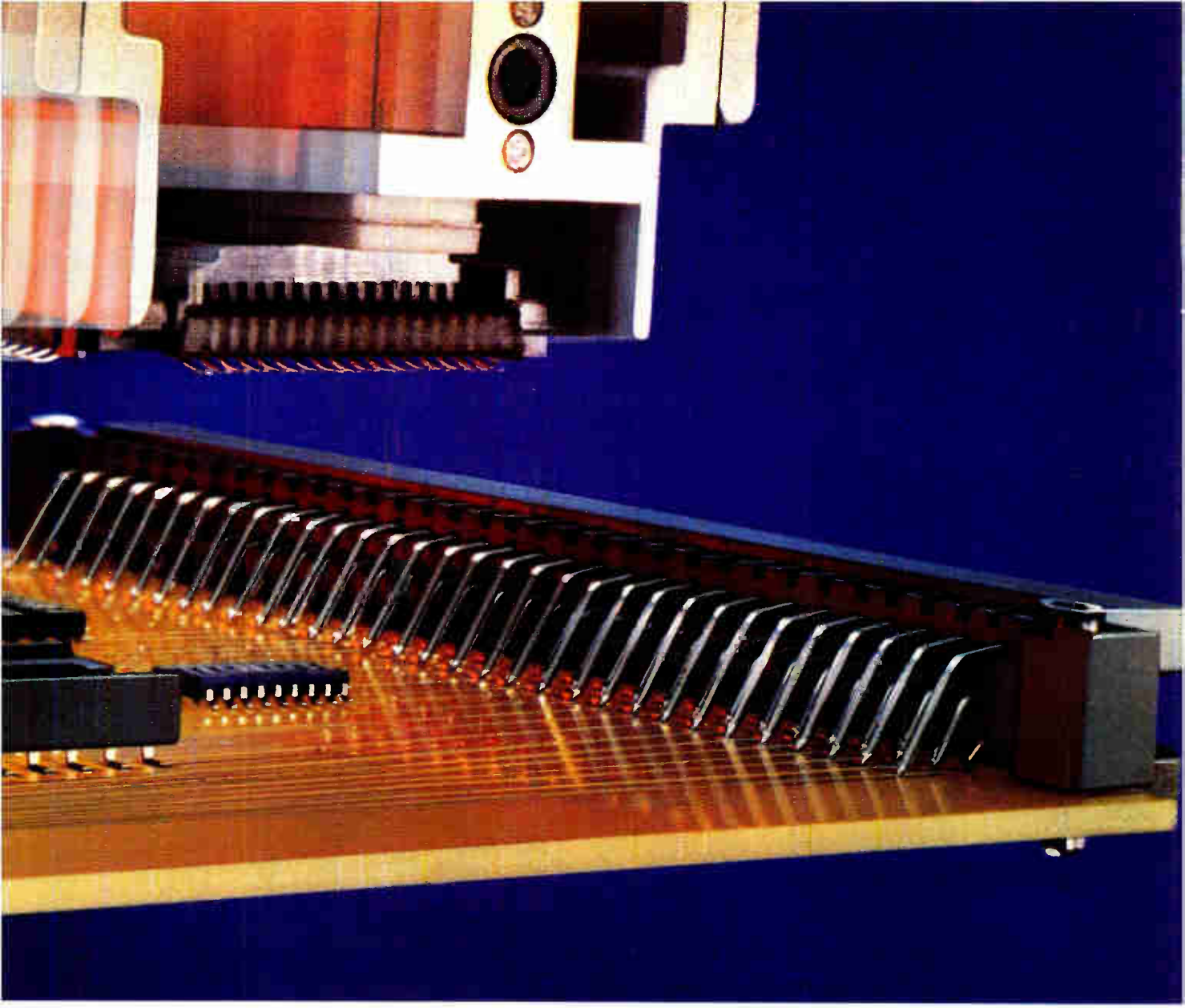

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some areas of product specification are still flexible. For example, solder leg design and specific platings are finalized in conjunction with the paste thickness you use, or time in reflow.

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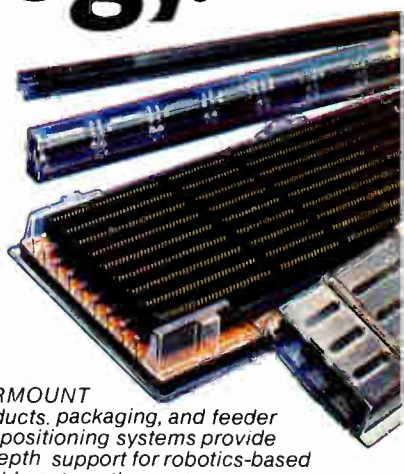

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AMP **Interconnecting ideas**

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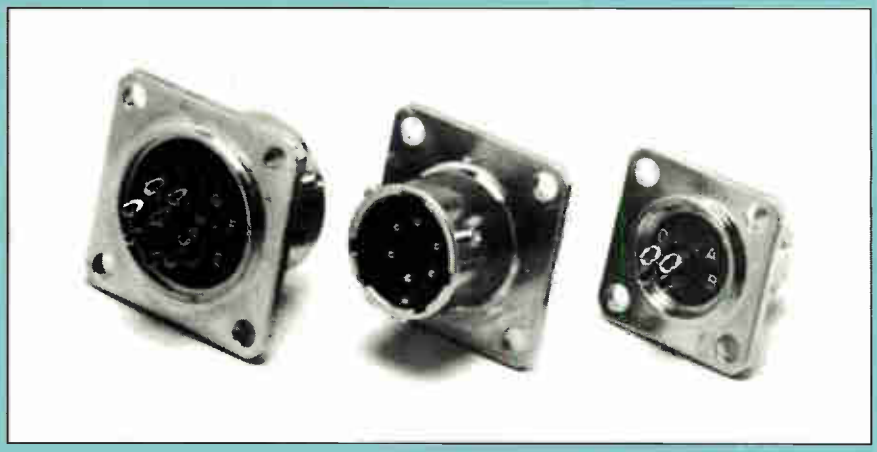
impetus: the ongoing trend toward denser packaging of electronic systems, which requires that components be soldered directly onto board surfaces. This trend has encouraged the miniaturization of components. And surface mounting also offers improved reliability, greater device integration, and better compatibility with automatic placement equipment—mainly robotic.

Along with all its merits, surface mounting has several unresolved problems, including the lack of test methods for SMDs and the questionable reliability of multicontact connectors. Standardization is another issue: the lack of standards for surface-mount resistors and other parts could slow the development of the technology. But efforts are under way to get surface-mounting standards in force, led by the Electronic Industries Association and the Institute for Interconnecting & Packaging Electronic Circuits, which recently cosponsored a

Detoronics brings out glass-sealed connectors

Detoronics Corp.'s new DTIH series of integral glass-sealed hermetic miniature connectors was designed originally for military applications, because the hermetic seal created by glass to metal forges a bond with a high sealing integrity that will maintain rated electrical characteristics through continuous exposure to thermal and mechanical shock. Now the devices, which come in several insert arrangements, are finding uses in other areas, says Richard Baroda, president of the South El Monte, Calif., company.



"The connectors are designed for applications requiring a vacuum, inert gas, or controlled pressure to eliminate adverse effects created by atmospheric changes," such as in instrumentation, missile control, and aircraft, he explains. Baroda says the company is aggressively marketing the glass-sealed connectors for industrial and medical applications, in which they are likely to be exposed to chemicals and other harsh environmental conditions.

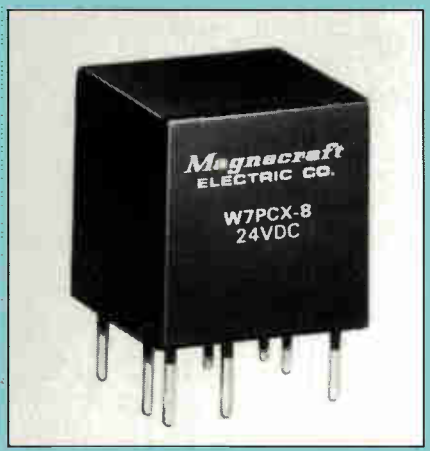
One new application is robotics, where the devices' ability to withstand both vibration and thermal shock makes them particularly useful. In addition, Detoronics is developing a single-pin version of the connector for use in the high-heat areas of automobiles.

Magnecraft adds to miniature and microminiature relay lines

Magnecraft Electric Co.'s lines of miniature and microminiature power relays are getting bigger. New are a Class 7 microminiature industrial-grade and a redesigned Class 65 low-profile pc-board power relay that can be cleaned by immersion.

The Class 7 device, which is the Northbrook, Ill., company's smallest two-pole microminiature high-reliability relay, has a mechanical life expectancy of over 100 million operations. It is rated for low-level to 2-A switching. Because it requires only 0.155 in.^{2} of space on the circuit board, a mounting density of more than six relays per square inch is possible.

The Class 65 miniature relay handles standard control voltages of 5, 6, 12, 23, and 48 V dc. It has low coil power for high-current switching



and is available in both horizontal and vertical styles. It also has 0.1 grid terminals. Typical applications for this relay are heating systems, automotive and consumer electronics, process control, communications, and data processing.

Also new from the company is a Class 236 voltage-sensing relay, which has received UL recognition at 481 V ac without transformers. The unit has independent adjustments for pull in and hysteresis, with pickup adjustable from 75% to 115% of nominal voltage and hysteresis adjustable from 75% to 98% of pickup. This range enables the relay to be used as either an overvoltage or undervoltage sensor.

World Radio History

of total capacitor sales in the U. S. in 1984, but they could reach 35% by 1989. Gnostic Concepts says that four major equipment producers—Delco, Northern Telecom, Motorola, and AT&T Technologies—consumed close to 800 million chip capacitors last year, and their needs could top 1.5 billion this year. The military market for capacitors also remains strong.

Consumption up

For connectors, U. S. production was down by 3% last year, but *Electronics*' 1986 market survey found that consumption was up close to 8%. The fact that many major users relied on their inventories last year cut significantly into connector manufacturers' sales.

Now that inventories are down, production this year is expected to grow at a reasonably healthy 13%, with much of that growth coming from sales to government/military customers. In fact, this year the government should become the largest consumer of connectors, edging out the computer industry for the first time.

Military and government sales also have given switches a much-needed boost and helped switch pricing remain fairly stable. *Electronics*, in its market survey earlier this year, projected growth of U. S. consumption at only 2% this year over 1985, partly because of heavy competition from Japanese manufacturers.

In an effort to get costs down, several switch makers have moved more of their production offshore and automated much of what's left of their domestic capacity. They have also targeted specific markets with improved designs.

Also starting to move offshore are keyboard makers looking to keep their prices in line with foreign competitors. Others are diversifying into different types of input devices. The keyboard market that was spectacular in 1983 and '84 declined in 1985 by at least 10%, according to some sources. Fortunately for passive components as a category, most of 1986's news is good, with surface mounting having been instrumental in boosting what could have been a flat market. And now the technology is creating a new generation of passive components. ■

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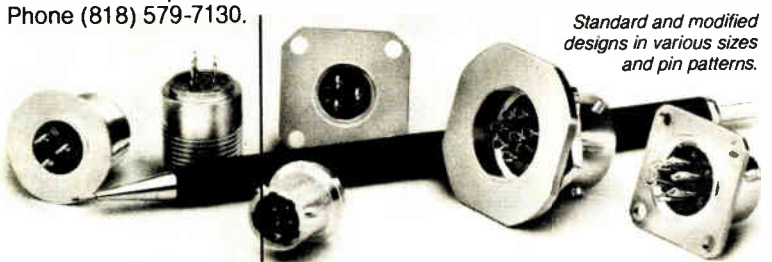

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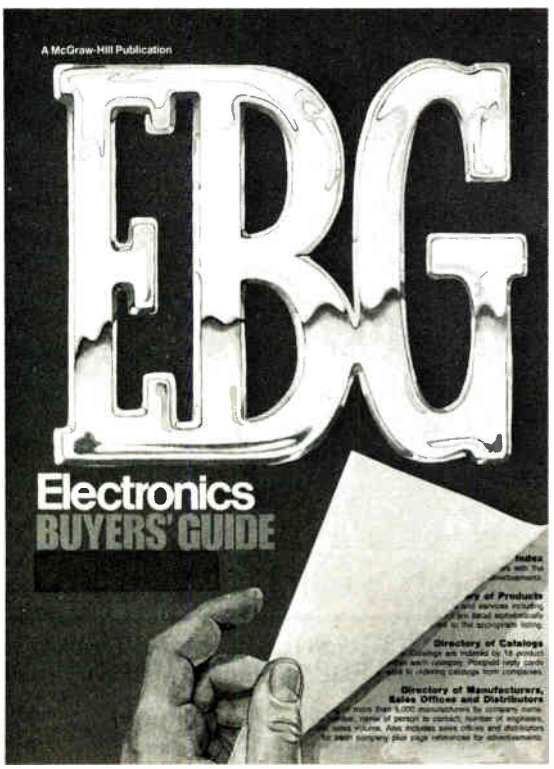

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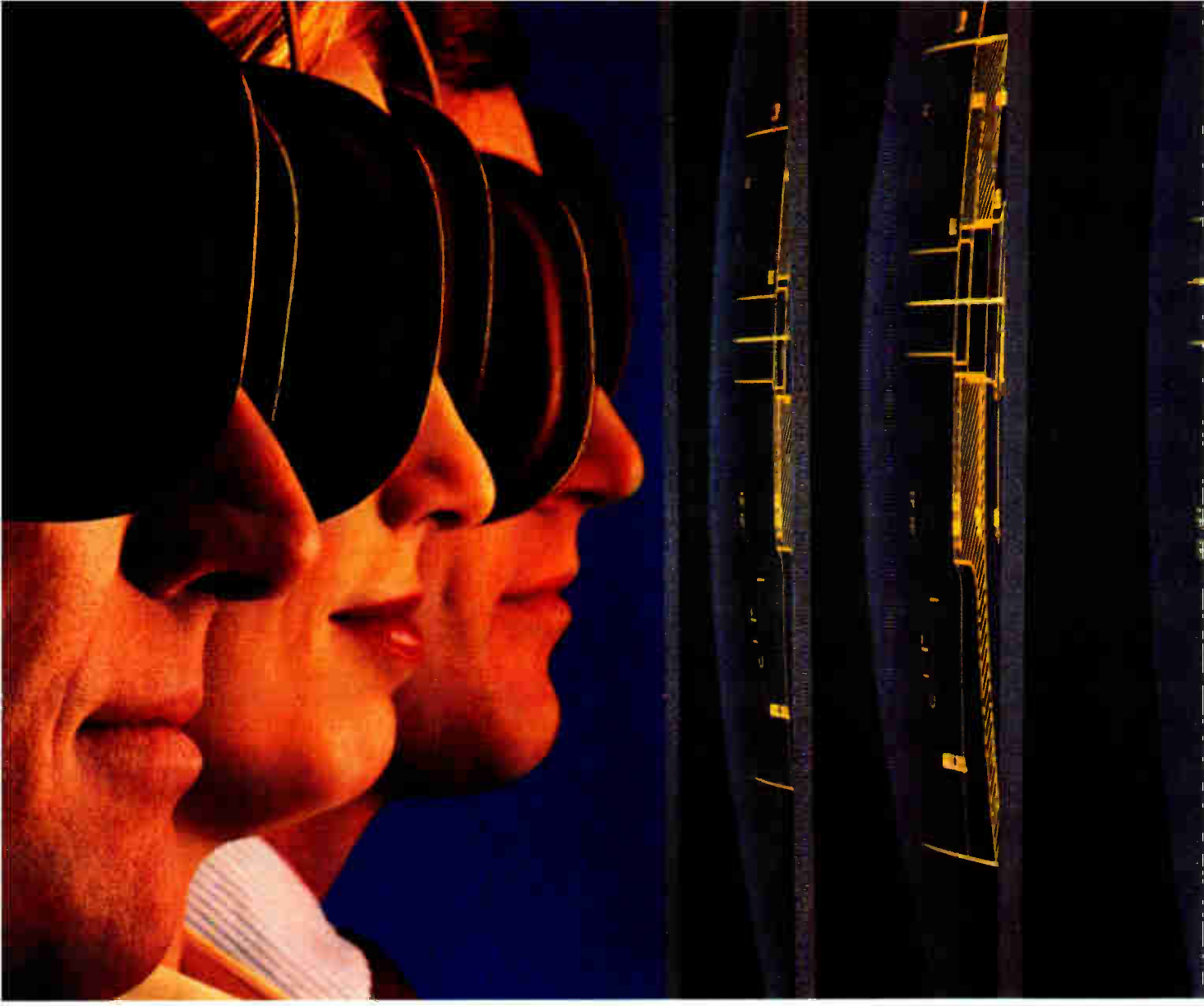

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PROBING THE NEWS

THE FAST STATIC RAM MOVES INTO THE MAINSTREAM

MORE IC MAKERS PICK IT AS TECHNOLOGY DRIVER FOR ADVANCED CMOS

by J. Robert Lineback

All of a sudden, chip makers around the world are paying heightened attention to fast static CMOS random-access memories, not long ago considered a minor niche in the memory market. Some 20 producers of integrated circuits now have moved into fast SRAMs and the pace of new-product introductions is picking up.

The players are lured in part by the relative stability of prices in high-performance memory chips, which so far have escaped the devastating price wars of the dynamic-RAM business. But even more important for the long term, the SRAM has become the chip of choice for many IC houses to drive advanced CMOS technology.

Along with its initial advantage of stingy power consumption, CMOS has become lightning-fast and threatens to displace entrenched technologies such as n-MOS and bipolar almost across the board as densities increase. Speed and application-specific features now figure as crucial elements for survival in SRAM markets, where prices for slower parts have started to slide and overpopulation almost surely will force a painful price war.

"We are all using SRAMs as a logical place for product differentiation," says Bob Johnson, vice president of National Semiconductor Corp.'s MOS Memory Group, Salt Lake City, Utah. "In this case, speed is the differentiation."

PAYOFF FOR SPEED. Indeed, each new step up in access speeds is likely to be profitable for early suppliers, says analyst Susan Scibetta of Dataquest Inc., the San Jose, Calif., market researcher. "The driver of this market is how fast you can access the data. So the price premium will belong to the company with products in the 25- or 15-ns range, while other [products] are slower."

Already, fast 64-K CMOS SRAMs are nipping at the heels of bipolar SRAMs. New chips from such makers as Advanced Micro Devices, Motorola, and Hitachi as well as from such smaller houses as Lattice Semiconductor and Performance Semiconductor (see chart, p. 122) have pushed maximum access times well below the 30-ns mark. Some designs will outdo 20 ns with further submicron process enhancements in the coming year. What's more, early prototypes of 256-K chips are already clocking in at 25 ns and 35 ns.

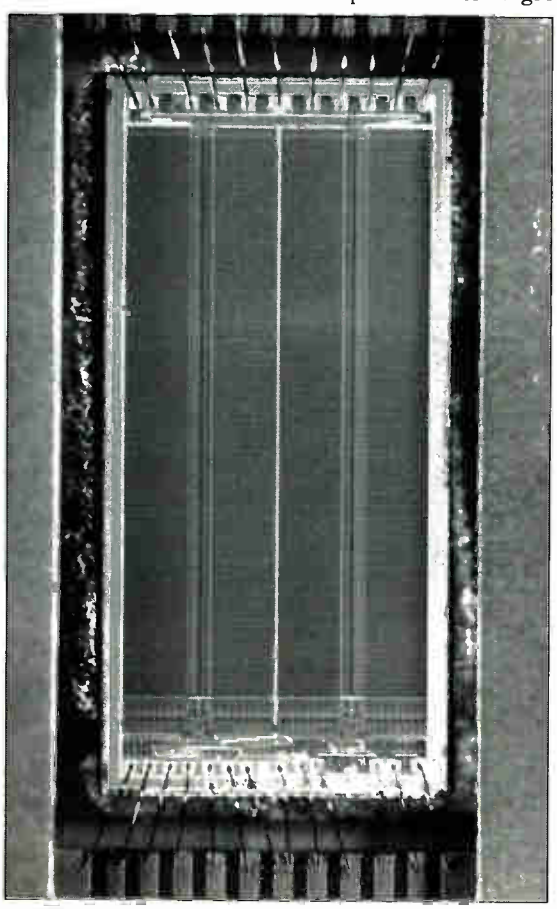
And a few CMOS proponents now believe the technology can eventually match the 5-ns access speeds of today's emitter-coupled logic. Many more predict the marriage of advanced CMOS with bipolar to achieve fast Bi-MOS megabit SRAMs.

The market for such devices, though still small, appears to be expanding. Dataquest says that fast SRAMs—those sporting access times of 70 ns or less—occupy a niche that's been growing while other MOS memory segments have not. In recession-vexed 1985, the company says, shipments of fast SRAMs rose 3%, to $365 million, compared with a plunge of 39% for all MOS memories, whose shipments totaled $1.8 billion. Dataquest says sales of fast SRAMs will grow to $400 million in 1986, while slow static memories will continue their slide, dipping another 5% this year, to $515 million.

The new emphasis on fast CMOS statics is partly a reaction to the tribulations in dynamic-RAM markets that resulted from overcapacity in the early 1980s. Until the recent industry downturn, DRAMs were solidly seated as the IC process driver at many leading chip houses. But promotion of SRAMs to the top of the technology pecking order may also have inherent technical advantages.

CMOS SRAMs, made with either four- or six-transistor storage cells, entail double-level metal processes and therefore are a natural learning vehicle for future CMOS technologies, which are becoming necessary for high-performance microprocessors. In addition, some SRAM proponents contend, DRAMs appear headed outside the technology mainstream, since they need special structures—such as trenched storage capacitors—to reach beyond megabit chip densities.

"Let's hope there is a good demand for all these fast statics," cautions Johnson at National Semiconductor. National is gearing up to join the quickening race for fast CMOS SRAMs with a new 35-ns 64-K chip design. It scrubbed a 150-ns



GETTING BETTER. Lattice Semiconductor is upgrading its 64-K chip to speed its access time from 35 to 25 ns.

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part last year because of falling prices for slower parts.

"Obviously, a lot of people are migrating to statics now to get away from DRAMs," Johnson says. "Everyone had hoped there wouldn't be that many competitors. I'm not sure it is turning out that way."

The ongoing push to raise the speed of SRAMs is opening up new markets, moreover. Anticipating much lower prices, some major personal computer makers, such as IBM Corp., plan to use high-density SRAMs in their upcoming machines instead of cheaper but slower DRAMs. Fast CMOS SRAMs are also speeding their way into new sockets inside engineering work stations, parallel-processing scientific computers, and high-resolution graphics subsystems.

NEW ARCHITECTURE. The new market potentials and process spinoffs of fast CMOS SRAMs have drawn Motorola Inc. into the fray. Motorola is introducing a series of fast CMOS statics using a new block-oriented architecture with short bit lines and local operational amplifiers (see p. 81).

"We took some risks in playing the technology leapfrog game," admits Curt Wyman, Motorola's marketing manager for CMOS SRAMs in Austin, Texas. In addition to the new block architecture, Motorola developed a double-level metal CMOS process featuring transistors with 1.5-μm drawn channel lengths. The result is 25-ns access times in its 64-K parts scheduled to go into production this month, and likely the same speeds at the 256-K density. "The message there is that at the 64-K level you don't just shrink the geometries to get 25 ns," says Wyman.

The speed battle is pushing many SRAM makers toward the marriage of fast bipolar with CMOS. Many suppliers believe the trend could make SRAMs the process driver for BiMOS or BiCMOS hybrid technologies.

"We believe that CMOS, by itself, will be limited in the next two to three years in achieving the speeds and densities," says Raj Patel, product marketing manager for Integrated Device Technology Inc., Santa Clara, Calif. "The combination of bipolar and CMOS is certainly a possibility." IDT is now shipping 25-ns 64-K SRAMs using four transistor cells and, like many competing parts, made from a mixture of n-channel arrays with CMOS peripheral circuits.

Another company shipping in volume is Hitachi Ltd., whose 25-ns 64-K-by-1-bit SRAMs are made from its 2-μm Hi-BiCMOS process. The Tokyo company is also offering samples of a 16-K-by-4-bit Hi-BiCMOS chip.

Fujitsu Ltd., Tokyo, says it plans to introduce a new 64-K-by-1-bit BiMOS part that will achieve 15- to 20-ns speeds. In Cupertino, Calif., a startup called Saratoga Semiconductor Corp. recently announced 10-ns 4-K chips; they are ECL SRAMs made with full CMOS six-transistor cells. The 2-μm process—called SABiC, for self-aligned bipolar CMOS—will be used to produce 15- to 20-ns 16-K SRAMs as well.

But some competitors warn that schemes to marry bipolar and CMOS may be a little premature. Among them is Thomas A. Longo, whose Performance Semiconductor Corp., Sunnyvale, Calif., upped the speed ante in the 64-K race to 20 ns using a full CMOS technology. "I think BiMOS is interesting, but I would prefer to do whatever I can in full CMOS, because it gives you the low-

WHO'S DOING WHAT IN FAST STATIC RAMs

Company	Part	Technology[1]	Cell[2]	Speed (ns)	Power[3] (mW)	Current status
Advanced Micro Devices	64-K	CMOS, n-MOS/1.2/double	4	25	715, 110	Shipping
	256-K	10% shrink, but same gate size	4	35	NA	3Q introduction
Cypress Semiconductor	64-K	CMOS, n-MOS/0.8/single	4	25	550, 220	3Q introduction
	256-K	Considering same	4	25	NA	1987 introduction
Fairchild	64-K	CMOS, n-MOS/1.5/single	4	45	385, 55	Shipping
Fujitsu	64-K	CMOS, n-MOS/1.5/single	4	45	660, 83	Shipping
	64-K	CMOS, n-MOS/1.3/single	4	35	459, 83	Samples
	256-K	CMOS, n-MOS/1.3/single	4	55	550, 55	Samples
Integrated Device Technology	64-K	CMOS, n-MOS/1.2/single	4	25	550, 236	Shipping
	256-K	CMOS, n-MOS/NA/single	4	45	NA	Samples 4Q
Inmos	64-K	CMOS, n-MOS/1.5/single	4	35	440, 140	Shipping
	64-K	CMOS, n-MOS/1.0/double (upgrade)	4	25	NA	Late 1986 introduction
	256-K	CMOS, n-MOS/1.0/double	4	25	NA	Late 1986 introduction
Intel	16-K	Full CMOS/1.5/double	6	25	440, 55	Shipping
Harris	64-K	Full CMOS/2.0/single (military)	6	150	110, 55	3Q introduction
	64-K	Full CMOS/1.2/double (military: upgrade)	6	70	NA	Pilot production
Hitachi	64-K	CMOS, n-MOS/2.0/single	4	45	550, 165	Shipping
	64-K	CMOS, n-MOS/1.3/double	4	35	550, 165	Samples 3Q
	64-K	BiCMOS/2.0/double	4	25	550, 220	Samples
	256-K	NA	4	NA	NA	1987 introduction
Lattice Semiconductor	64-K	CMOS, n-MOS/1.5/single	4	35	550, 75	Shipping
	64-K	CMOS, n-MOS/1.0/single (upgrade, scaled)	4	25	450, 75	Samples 4Q
	64-K	CMOS, n-MOS/1.0/double	4	20	450, 75	Second half 1987
	256-K	CMOS, n-MOS/1.0/double	4	35	450, 75	Samples late 1986
Mostek	16-K	Full CMOS/1.2/double	6	20	605, 55	Shipping
	16-K[4]	Same technology (with mask change)	6	25	303, 33	Shipping
Motorola	64-K	CMOS, n-MOS/1.5/double	4	25	110, 28	Production 8/86
	256-K	NA	4	25	NA	Early 1987 introduction
National	64-K	CMOS, n-MOS/1.6/single	4	35	358,110	Samples 3Q
	256-K	Basically as above	4	55	NA	1987 introduction
NEC	64-K	CMOS, n-MOS/1.5/double	4	40	660, 11	Shipping
Performance Semiconductor	64-K	Full CMOS/1.2/double	6	20	550, 193	Production 9/86
	256-K	NA	NA	NA	NA	1987 introduction
RCA	64-K	Full CMOS/2.0/single	6	150	500, 225	Shipping
	16-K	Full CMOS/3.0/single	6	55	50, 100	Samples 9/86
	256-K	Full CMOS/1.2/single	6	100	500, 325	Samples 9/86
Texas Instruments	16-K	Full CMOS/1.0/single	6	<30	NA	1987 introduction
	64-K	Same as 16-K				
	256-K	Full CMOS/NA/NA	6	<30	NA	1987 introduction
Toshiba	64-K	CMOS, n-MOS/1.5/double	4	45	550, 55	Shipping
	64-K	CMOS, n-MOS/1.2/double	4	35	550, 55	In design
	256-K	CMOS, n-MOS/1.0/double	4	35	495, 110	In design
Visic	64-K	Full CMOS/1.2/double	6	20–25	NA	Early 1987 introduction
	256-K	NA	6	25–35	NA	1987 introduction
Vitelic	64-K	CMOS, n-MOS/1.5/double	4	45	660, 138	Shipping
	256-K	Two versions/1.2/double	4, 6	25	NA	1Q introduction

[1] Peripheral circuits, memory array/drawn gate length (μm)/metalization
[2] Number of transistors per cell
[3] Active, standby (on 5.5 V power supply with TTL inputs)
[4] Operates at 3.3 V
NA = Not available

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PROBING THE NEWS

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MORE IC MAKERS PICK IT AS TECHNOLOGY DRIVER FOR ADVANCED CMOS

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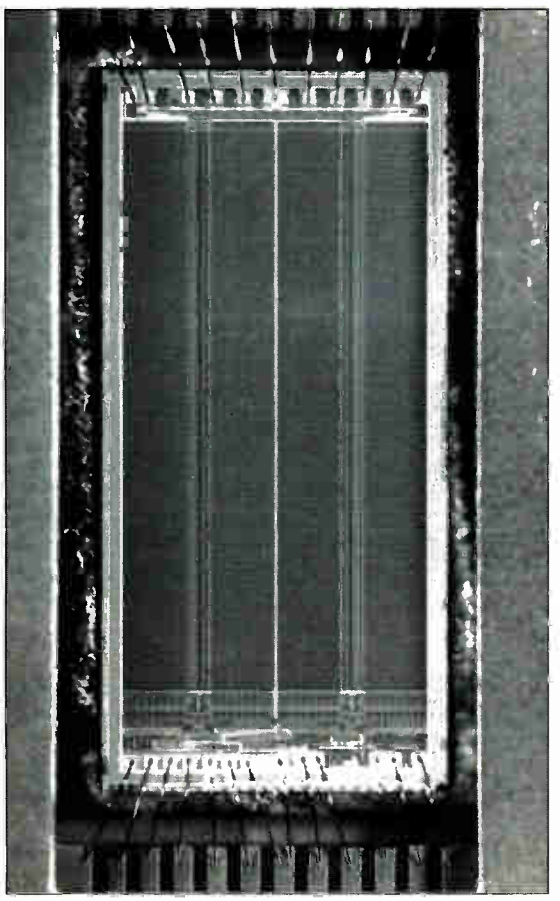
CMOS SRAMs, made with either four- or six-transistor storage cells, entail double-level metal processes and therefore are a natural learning vehicle for future CMOS technologies, which are becoming necessary for high-performance microprocessors. In addition, some SRAM proponents contend, DRAMs appear headed outside the technology mainstream, since they need special structures—such as trenched storage capacitors—to reach beyond megabit chip densities.

"Let's hope there is a good demand for all these fast statics," cautions Johnson at National Semiconductor. National is gearing up to join the quickening race for fast CMOS SRAMs with a new 35-ns 64-K chip design. It scrubbed a 150-ns



GETTING BETTER. Lattice Semiconductor is upgrading its 64-K chip to speed its access time from 35 to 25 ns.

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part last year because of falling prices for slower parts.

"Obviously, a lot of people are migrating to statics now to get away from DRAMs," Johnson says. "Everyone had hoped there wouldn't be that many competitors. I'm not sure it is turning out that way."

The ongoing push to raise the speed of SRAMs is opening up new markets, moreover. Anticipating much lower prices, some major personal computer makers, such as IBM Corp., plan to use high-density SRAMs in their upcoming machines instead of cheaper but slower DRAMs. Fast CMOS SRAMs are also speeding their way into new sockets inside engineering work stations, parallel-processing scientific computers, and high-resolution graphics subsystems.

NEW ARCHITECTURE. The new market potentials and process spinoffs of fast CMOS SRAMs have drawn Motorola Inc. into the fray. Motorola is introducing a series of fast CMOS statics using a new block-oriented architecture with short bit lines and local operational amplifiers (see p. 81).

"We took some risks in playing the technology leapfrog game," admits Curt Wyman, Motorola's marketing manager for CMOS SRAMs in Austin, Texas. In addition to the new block architecture, Motorola developed a double-level metal CMOS process featuring transistors with 1.5-μm drawn channel lengths. The result is 25-ns access times in its 64-K parts scheduled to go into production this month, and likely the same speeds at the 256-K density. "The message there is that at the 64-K level you don't just shrink the geometries to get 25 ns," says Wyman.

The speed battle is pushing many SRAM makers toward the marriage of fast bipolar with CMOS. Many suppliers believe the trend could make SRAMs the process driver for BiMOS or BiCMOS hybrid technologies.

"We believe that CMOS, by itself, will be limited in the next two to three years in achieving the speeds and densities," says Raj Patel, product marketing manager for Integrated Device Technology Inc., Santa Clara, Calif. "The combination of bipolar and CMOS is certainly a possibility." IDT is now shipping 25-ns 64-K SRAMs using four transistor cells and, like many competing parts, made from a mixture of n-channel arrays with CMOS peripheral circuits.

Another company shipping in volume is Hitachi Ltd., whose 25-ns 64-K-by-1-bit SRAMs are made from its 2-μm Hi-BiCMOS process. The Tokyo company is also offering samples of a 16-K-by-4-bit Hi-BiCMOS chip.

Fujitsu Ltd., Tokyo, says it plans to introduce a new 64-K-by-1-bit BiMOS part that will achieve 15- to 20-ns speeds. In Cupertino, Calif., a startup called Saratoga Semiconductor Corp. recently announced 10-ns 4-K chips; they are ECL SRAMs made with full CMOS six-transistor cells. The 2-μm process—called SABiC, for self-aligned bipolar CMOS—will be used to produce 15- to 20-ns 16-K SRAMs as well.

But some competitors warn that schemes to marry bipolar and CMOS may be a little premature. Among them is Thomas A. Longo, whose Performance Semiconductor Corp., Sunnyvale, Calif., upped the speed ante in the 64-K race to 20 ns using a full CMOS technology. "I think BiMOS is interesting, but I would prefer to do whatever I can in full CMOS, because it gives you the low-

WHO'S DOING WHAT IN FAST STATIC RAMs

Company	Part	Technology[1]	Cell[2]	Speed (ns)	Power[3] (mW)	Current status
Advanced Micro Devices	64-K 256-K	CMOS, n-MOS/1.2/double 10% shrink, but same gate size	4 4	25 35	715, 110 NA	Shipping 3Q introduction
Cypress Semiconductor	64-K 256-K	CMOS, n-MOS/0.8/single Considering same	4 4	25 25	550, 220 NA	3Q introduction 1987 introduction
Fairchild	64-K	CMOS, n-MOS/1.5/single	4	45	385, 55	Shipping
Fujitsu	64-K 64-K 256-K	CMOS, n-MOS/1.5/single CMOS, n-MOS/1.3/single CMOS, n-MOS/1.3/single	4 4 4	45 35 55	660, 83 459, 83 550, 55	Shipping Samples Samples
Integrated Device Technology	64-K 256-K	CMOS, n-MOS/1.2/single CMOS, n-MOS/NA/single	4 4	25 45	550, 236 NA	Shipping Samples 4Q
Inmos	64-K 64-K 256-K	CMOS, n-MOS/1.5/single CMOS, n-MOS/1.0/double (upgrade) CMOS, n-MOS/1.0/double	4 4 4	35 25 25	440, 140 NA NA	Shipping Late 1986 introduction Late 1986 introduction
Intel	16-K	Full CMOS/1.5/double	6	25	440, 55	Shipping
Harris	64-K 64-K	Full CMOS/2.0/single (military) Full CMOS/1.2/double (military: upgrade)	6 6	150 70	110, 55 NA	3Q introduction Pilot production
Hitachi	64-K 64-K 64-K 256-K	CMOS, n-MOS/2.0/single CMOS, n-MOS/1.3/double BiCMOS/2.0/double NA	4 4 4 4	45 35 25 NA	550, 165 550, 165 550, 220 NA	Shipping Samples 3Q Samples 1987 introduction
Lattice Semiconductor	64-K 64-K 64-K 256-K	CMOS, n-MOS/1.5/single CMOS, n-MOS/1.0/single (upgrade, scaled) CMOS, n-MOS/1.0/double CMOS, n-MOS/1.0/double	4 4 4 4	35 25 20 35	550, 75 450, 75 450, 75 450, 75	Shipping Samples 4Q Second half 1987 Samples late 1986
Mostek	16-K 16-K[4]	Full CMOS/1.2/double Same technology (with mask change)	6 6	20 25	605, 55 303, 33	Shipping Shipping
Motorola	64-K 256-K	CMOS, n-MOS/1.5/double NA	4 4	25 25	110, 28 NA	Production 8/86 Early 1987 introduction
National	64-K 256-K	CMOS, n-MOS/1.6/single Basically as above	4 4	35 55	358,110 NA	Samples 3Q 1987 introduction
NEC	64-K	CMOS, n-MOS/1.5/double	4	40	660, 11	Shipping
Performance Semiconductor	64-K 256-K	Full CMOS/1.2/double NA	6 NA	20 NA	550, 193 NA	Production 9/86 1987 introduction
RCA	64-K 16-K 256-K	Full CMOS/2.0/single Full CMOS/3.0/single Full CMOS/1.2 single	6 6 6	150 55 100	500. 225 50. 100 500, 325	Shipping Samples 9/86 Samples 9/86
Texas Instruments	16-K 64-K 256-K	Full CMOS/1.0/single Same as 16-K Full CMOS/NA/NA	6 6	<30 <30	NA NA	1987 introduction 1987 introduction
Toshiba	64-K 64-K 256-K	CMOS, n-MOS/1.5/double CMOS, n-MOS/1.2/double CMOS, n-MOS/1.0/double	4 4 4	45 35 35	550, 55 550, 55 495, 110	Shipping In design In design
Visic	64-K 256-K	Full CMOS/1.2/double NA	6 6	20–25 25–35	NA NA	Early 1987 introduction 1987 introduction
Vitelic	64-K 256-K	CMOS, n-MOS/1.5/double Two versions/1.2/double	4 4, 6	45 25	660, 138 NA	Shipping 1Q introduction

[1] Peripheral circuits, memory array/drawn gate length (μm)/metalization
[2] Number of transistors per cell
[3] Active, standby (on 5.5 V power supply with TTL inputs)
[4] Operates at 3.3 V
NA = Not available

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est power and the most cost-competitive product," says Longo, who is company president.

"As soon as you get into things like BiMOS, everything changes, and things start to look more like ECL.... I think people are tending to overuse BiMOS right now because it is the only way they know to get the speeds." Longo boldly believes CMOS can potentially reach 5-ns access times through process refinements such as finer geometries and lower sheet resistance for gates.

AMD'S APPROACH. Advanced Micro Devices Inc. is exploring both BiMOS and some new ways of thinking about CMOS when it comes to future SRAMs, says Marshall Wilder, managing director of MOS RAMs in Sunnyvale, Calif. "We now have a very serious effort under way to marry the two together into a BiMOS technology. That should produce sub-10-ns large SRAMs, primarily directed toward the ECL speed levels."

Wilder is convinced that CMOS speeds could be stepped up considerably if power constraints were eased. "Tell your clever CMOS circuit designers not to worry about burning a watt or two," he says.

Lattice Semiconductor Corp., Beaverton, Ore., is pursuing the architectural path to higher speeds with more emphasis on application-specific memories, says Scott McMorrow, application manager for memories. Unlike Longo, he believes that pure-CMOS 64-K RAMs will stall at 20-ns access times. "At 20 ns, you are within 0.7- or 0.8-μm effective channel lengths, which is where you get into the hot-electron effects," he says. "That's why we are looking very carefully at application-specific memories [such as video RAMs] to increase the overall system performance without pushing the technology so hard."

The growing demand for fast CMOS SRAMs has spawned upgrades of early-to-market memories, as well as a plethora of new products. Refined designs of 64-K and 256-K chips, pushing times to as low as 25 ns, are coming from nearly all major SRAM vendors.

For example, Inmos Corp., which in its heyday as a startup nearly had the entire fast-SRAM market to itself, is preparing a rebid for speed leadership with a new double-level metal 1-μm process. After moving its volume production from Colorado Springs to Newport, Wales, the company will install a new class 10 clean-room pilot line in its U. S. plant for the fabrication of a new 25-ns 64-K-by-4-bit SRAM.

The company has already begun evaluating a future technology—"Process 88"—for an eventual pass at fast 1-Mb CMOS SRAMs. "We were in a leadership process. People caught up. I think we are going to get ahead again," says Dee Hockaday, product marketing manager for SRAMs.

"Right now we've got some parts running at 20 ns. What's to keep us from getting faster? The chip testers on the market only go that fast, but by the start of 1987, systems are expecting to test parts 10 ns or faster."

New entries into the market are also under way at several large chip suppliers, including Mostek (now a subsidiary of Thomson-CSF), RCA, and TI.

Thomson Components-Mostek Corp., Carrollton, Texas, is the first supplier to introduce a family of fast 16-K SRAMs that operate off 3.3-V power supplies. (Jedec has standardized the 3.3-V power supply in response to chip makers' concerns that current 5-V supplies may be too high for submicron circuit geometries.) The 3.3-V option is set by a metal mask, which changes the output drivers. Mostek's 3.3-V parts achieve 25-ns access times; its standard 5-V versions are rated at 20 ns.

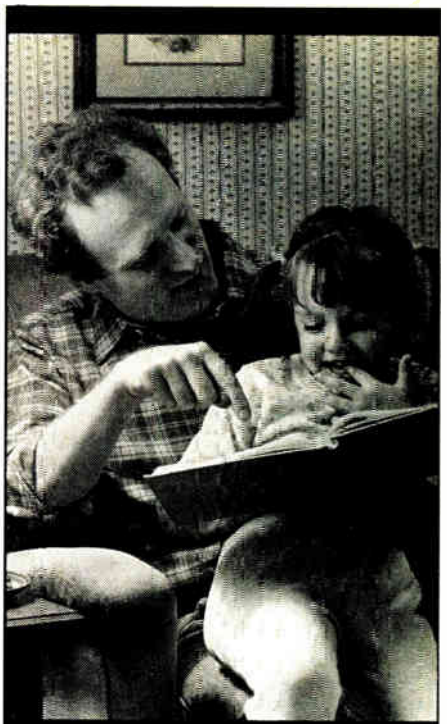
"As far as we can tell we are the first ones [with 3.3-V parts]. It is a little early and it will take a while for things to take off. But you have to start somewhere, and we are getting some interest in the parts already," says Tom Tyson, marketing manager for Mostek memory products. Most other SRAM suppliers remain reluctant to offer 3.3-V parts because similarly powered logic chips are not yet available.

One chip maker says CMOS can achieve 5-ns access times

MILITARY BUSINESS. Texas Instruments Inc.—a staunch proponent of DRAM-driven process strategies—will be courting the military system houses next year with a fast SRAM that will use a technology spun off the Dallas company's 1-μm megabit DRAM process. TI's DRAM process uses titanium silicide to lower the gate and junction sheet resistance. When the titanium is annealed in a nitrogen ambient, it forms a connecting strap of titanium nitride wherever the material is not in contact with silicon.

The strap, which is usually etched away, can be used to form a space-saving n+-to-p+ gate connection. Full CMOS six-transistor cells turn out to be roughly the same size as less reliable four-transistor cells. TI believes six-transistor cells are needed in fast 1-μm SRAMs to ensure immunity from soft errors and transient noise. □

Additional reporting came from Charles L. Cohen in Tokyo and Tobias Naegele in New York.



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CAN DISTRIBUTORS STAKE OUT A CLAIM IN THE ASIC BUSINESS?

THE PLUNGERS SAY YES; OTHERS BALK AT THE RISKY INVESTMENT

by Larry Waller

LOS ANGELES

The fast rise of the application-specific integrated circuit is already causing fundamental changes in the IC industry. But perhaps nowhere are these semicustom chips creating more pressure for change than in the distribution business.

Distributors have had to make bedrock decisions and make them fast. Should it be business as usual—with the distributor serving merely as a marketer for the silicon houses? Or should the distributor immerse itself in design details, becoming a technology broker between ASIC users and silicon fabricators? Whichever way they go, the risks are great: the conservative approach can mean being left behind; the bold one involves investing large sums of money in a business so new that its direction is still difficult to read.

Some executives concluded early on that they had no choice in the matter. "[ASIC sales] will be half of all IC sales sometime in the 1990s. How can we [distributors] not be involved in that?" asks Charles M. Clough, president of Wyle Laboratories and the man cited by industry watchers as the earliest and most enthusiastic proponent of the go-for-it approach. As then head of the Irvine, Calif., company's Electronic Marketing Group, Clough in late 1984 led Wyle to its first ASIC design win, months before any of its competitors nabbed a contract.

Though not quite so bullish on the market as Clough, In-Stat Inc., the Scottsdale, Ariz., market analyst, predicts a significant hike. ASICs' share of IC sales worldwide will rise from 12.8% in 1986 to 22.3% in 1990, In-Stat says. In fact, In-Stat predicts ASIC sales will still climb even when the IC industry enters its next downturn (see table, p. 125).

Clough thinks that earlybird Wyle—plus the nationwide distribution behemoth Hamilton/Avnet Corp., Culver City, Calif., and perhaps a few others—will manage to capture and keep the lion's share of the market, as all but a few late starters will find it difficult to catch up. William I. Strauss of Forward Concepts in Tempe, Ariz., a market and process consultant who has advised distributors on this matter, agrees. "Those who did the planning and got started will lead the pack," he says.

And with substantial ASIC revenues in sight, nagging doubts about profitability are being dispelled too. Wyle, in fact, is edging into the black sooner than chart watchers expected. At midyear, sales were running at an annual rate of $5 million.

'VULNERABILITIES.' Nevertheless, some distributors are in no big hurry to join the game. "A distributor does not need the vulnerabilities of ASIC as it exists today," says Howard Franklin, president of Electronic Marketing in Sunnyvale, Calif., the nationwide distribution arm of Bell Industries Inc. His view sums up the skepticism of many distributors, who are wary of the financial risks involved. Indeed, the timing for the early entrants was difficult: not only did they have to hire a technical design staff and invest in computer-aided-design equipment, but they were doing so during a semiconductor recession, with no guarantee of a return for years.

But despite such qualms, the number of pro-ASIC houses is growing. Besides front-runner Wyle and Hamilton/Avnet, they include such regional distributors as Hall-Mark Electronics in Dallas, which started its effort 18 months ago and now has three design centers in operation, with a fourth scheduled to start up at year-end. Among the second wave are national distributors Schweber Electronics Corp., Westbury, N. Y., representing LSI Logic Corp.; and Arrow Electronics Inc., Melville, N. Y., which is forging an ASIC agreement with Texas Instruments Inc. These companies and a handful of others are making solid commitments to ASIC-selling programs.

"These guys have to be considered gutsy," says Strauss of Forward Concepts, even though small customers who need only a few thousand ASICs do add up to an important opportunity for distributors. He notes that aside from the potential financing and marketing headaches, working with ASIC designs is far different, and more complex, than anything distributors have ever done before. Indeed, the new role vastly alters what in the past was simply sales.

"It's really a new industry," says financial analyst Andrew J. Neff of Mont-

SNUGGLING UP. To place testing facilities as close as possible to the customer, TI has installed Impact Centers at distributor sites. This first is in Santa Clara, Calif.

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gomery Securities, San Francisco. "It's not the chip business as they knew it, that's for sure," echoes William J. O'Meara, vice president for marketing and sales at LSI Logic, the Milpitas, Calif., chip maker that is the leading supplier of gate-array ASICs to Wyle and others. And, says Strauss, "some distributors are scared to death of technology."

Not Wyle. The company set up its first design center in the summer of 1984 and signed up its first customers in the fourth quarter of that year. Shipments started in early 1985, well ahead of competitors. Industry observers say the early start was crucial and is the main reason Wyle has racked up an impressive 165 ASIC design wins—"as many as everyone else put together," says Rick Timmins, Wyle's vice president for semicustom ICs. Nearly all of them are CMOS arrays from LSI Logic, which means that some 10% of its ASIC orders now come from distributors and the share is fast increasing.

Hamilton/Avnet won't divulge its total ASIC design wins, but analysts see the company as a strong contender because of its size—it boasts 52 locations and billion-dollar annual total sales. "Wyle has the higher profile, but Avnet is the biggest guy and solidly in the ball game," notes analyst Neff.

Wyle sells in 13 Western states through six strategically located CAD-equipped regional design centers. Customers come largely from its roster of smaller companies that traditionally buy from distributors rather than direct from a semiconductor factory. Hamilton/Avnet, with ASIC operations at Sunnyvale, also has six design centers, but its approach is to work whenever possible at the customer's site. "Customers prefer their own premises," says Robert Gardner, Hamilton/Avnet's vice president for ASICs. Gardner credits the field approach for the company's "80% hit rate" in getting design jobs.

DESIGN IS THE KEY. Equipment and approaches aside, no successful ASIC effort can be mounted without a design staff at least as skilled as those of the ASIC manufacturers themselves. "That's the key—being very technically competent," says Wyle's Clough. Not only are highly qualified people critical to getting business, but they mean fewer failed designs and fewer customers whose projects run into trouble. Because of the single-source nature of ASICs, "our responsibility to customers is far greater," says Clough.

Wyle's design staff counts 12 BSEEs who have taken courses offered by suppliers. Other distributors have followed suit, says LSI Logic's O'Meara: "Most everybody else is taking a page out of Wyle's primer."

ASICs TO GAIN WORLDWIDE MARKET SHARE

	Total IC sales ($ billion)	Total ASIC sales ($ billion)	ASIC share
1986	17.15	2.16	12.6
1987	21.34	2.98	14.0
1988	24.55	3.88	15.8
1989	23.20	4.20	18.1
1990	22.53	5.03	22.3

SOURCE IN STAT INC

Hamilton/Avnet has 14 design engineers and soon will add six more. And next year it will add field-application people as part of what ASIC vice president Gardner calls "a strong engineering value-added program." He sees "pool groups of engineers" being more effective with customers in the field than "single engineers, who get very lonely out there."

Not only must distributors beef up their technical expertise, but there are other departures from traditional distribution strategy as well, says Clough. The most obvious casualty is the salesman's classic emphasis on offering a customer the widest possible choices among competing products. Given the complexity of the devices and the extent of training needed to design them, "specialization is the need," he says.

Wyle therefore limits itself to one supplier for each ASIC category. Besides LSI Logic, it sells standard cells from TI; erasable programmable logic circuits from Altera Corp., Santa Clara, Calif.; and programmable logic devices from TI and several noncompeting makers. All designs are done on Daisy Systems Corp. work stations, either at the design centers or on systems sold or leased to customers. (Hamilton/Avnet, on the other hand, believes diversity is an advantage, even with ASIC. It lists a half dozen large and small semiconductor houses with competing products.)

The ASIC investment includes a design team, as well as CAD gear

Among suppliers, TI also prefers to keep distributor agreements to a minimum, for reasons similar to Clough's. "Our feeling-out period with Wyle lasted for months, since we spent so much time on how to support [the new setup]. This is a very service-oriented business," notes William Bolin, marketing manager at TI's ASIC marketing division, Dallas. TI will soon announce that Arrow Electronics Inc. is the next distributor to handle its ASIC lines.

TI probably markets its ASICs through distributors more aggressively than any of its rivals. This is true with standard cells, but the company is also making a major commitment to what it calls Impact Centers at distributor locations for testing programmable logic devices and programmable read-only memories.

The first center was set up in May at the Santa Clara site of regional distributor Marshall Industries; the second went into Wyle's Irvine site in July. "The Impact Centers came from customers telling us they wanted them," says Philip Coup, vice president of TI's VLSI Logic Products Group. The advantage is proximity to the customer; the alternative is having a third party do the testing at considerable loss of time, he says.

STILL UNCONVINCED. Despite this flurry of activity, some distributors remain holdouts, pointing to potential booby traps. Among them, says Howard Franklin of Electronic Marketing, is one key problem area—the price-protection and return provisions that cover off-the-shelf components but that cannot apply to one-of-a-kind ASICs. "Once you [the distributor] order a special device, you own it," he says. Still, Franklin says his company is taking a wait-and-see stance and keeping its options open.

Price protection and returns also concern Neff of Montgomery Securities. "Who bears the risk" for foul-ups, he wonders, when a customer suddenly decides not to take as many parts as originally ordered. Order changes are almost inevitable as new ASIC designs continually move into production and as market conditions change. Wyle's Timmins says that so far, his experience shows another problem is more common: "canceling a project after the design is completed." This has happened to Wyle, he says, and the liabilities are still being sorted out.

One potential pitfall is almost as old as distribution itself: who should serve a choice components customer. This could cause even more tension in the ASIC field than it has in the past, when both manufacturer and distributor have a design center near the customer. Surprisingly, it is the suppliers who vow to keep it from happening. "Early on, we are front-loading it for the distributor," says LSI Logic's O'Meara.

TI too says the dividing line is clear: large buyers to the factory and small ones to the distributor, with any conflict resolved on the side of distribution. "We need distributors to be successful, to help us reach the mass market," says TI's Bolin, echoing O'Meara's view.

Distributors have demonstrated they can sell ASICs. The biggest remaining questions now concern how fast the market can grow for them and how many strong contenders will emerge. □

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NEW PRODUCTS

MODELING VHSIC CHIPS SPEEDS UP SYSTEM SIMULATION

LOGIC AUTOMATION'S SOFTWARE REPLACES HARDWARE PROTOTYPES

Software simulation models from Logic Automation Inc. aim to solve the nagging system-simulation problems that are popping up as very high-speed ICs—such as IBM Corp.'s complex multiplier accumulator (CMAC)—emerge from the labs and move into production. Called SmartModels, Logic Automation's products are for the IBM chip and four new VHSIC components from TRW Inc.: the TVC341 four-port memory, TVC372 multiplier accumulator, TVC831 fast Fourier transform arithmetic unit, and TVC981 FFT control unit.

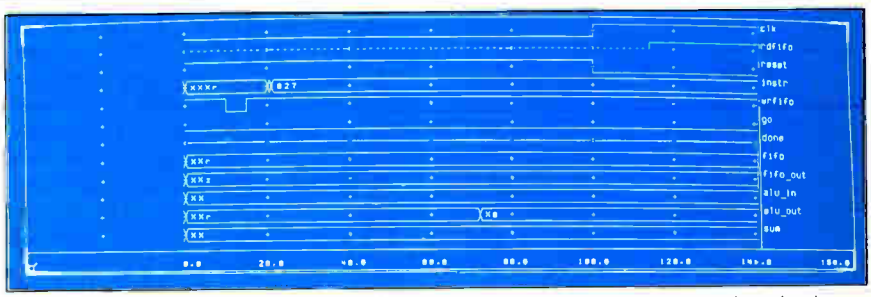
IBM's CMAC and the TRW chips were built to meet the specifications of Phase 1 of the Defense Department's VHSIC program. They will be used in a wide range of DOD applications for real-time electronic warfare, communications, and radar.

The cutting-edge features of VHSIC chips such as the CMAC—high pin count and high operating speed, for example—make them difficult for an engineer to design into a pc board. Moreover, even if a breadboard could be built, debugging the circuit using a conventional logic analyzer would be impractical.

TOO MUCH, TOO FAST. "It is unreasonable to hook up a logic analyzer to several 200-pin ICs and expect to make a lot of sense out of the reading," says Logic Automation's marketing vice president Robert Hunter. The IBM CMAC has 210 pins, and a typical implementation will use several CMACs. The amount of data to collect will exceed a logic analyzer's memory. The speed at which the data is passing through the chip's pins (25 MHz and above) is too much for the analyzer to handle—and Phase 2 VHSIC chips will run between 50 and 100 MHz.

The Logic Automation software models solve the major problems confronting the designer. They provide a way to handle the large amount of data that must be analyzed to validate the chip's operation. And they validate a design at full speed without having to run a hardware prototype at a slower speed to imitate full-speed operation.

For example, a designer running a simulation of the CMAC in a typical implementation must simulate the surrounding circuits as well. The system and group controllers controlling the CMAC download initialization data, in the form of 40-bit-wide words, into the chip.



CLOCKING. Logic Automation's SmartModels, which are software packages that simulate a number of VHSIC chips, detect clock edges even at rates above 25 MHz.

"To simulate this operation, the SmartModel downloads equivalent data from a file at initialization time in the simulation run," says Robert Hunter. "Thereafter, the model watches all the clock edges at all times, and if it sees a violation, it reports it immediately." At 25 MHz, even a hardware model using an actual chip cannot accurately simulate the real-time operating speeds possible with SmartModel.

SPEC CHECKS. A number of tests within each model check that all parameters are set according to the chip's data sheet. For example, to verify that the complex protocols are correct between the CMAC and its surrounding chips, the model examines the order and procedures of the protocols; violations are reported to the user.

A feature called symbolic hardware debugging provides error messages to the designer when timing or other usage rules are violated. Just as a logic analyzer would, the model's error messages pinpoint the exact location, time, and nature of the fault condition.

Finally, the SmartModel simulates a malfunction in a chip. This capability is important for the CMAC chip, which has built-in redundancy. The CMAC SmartModel can simulate a failure and the resulting repair made by the self-correcting circuit.

SmartModels for the IBM and TRW chips run on popular work stations. The model for the IBM chip is available now, and models of the TRW devices will be made available between September and November. Models are priced at $4,900 each. *–Jonah McLeod*

Logic Automation Inc., 19545 N. W. Von Neumann Drive, Beaverton, Ore. 97006. Phone (503) 690-6900 [Circle reader service number 380]

EPLD DESIGN SOFTWARE COMES IN UNDER $1,000

A schematic-capture software package designed for Altera Corp.'s development system for erasable programmable logic devices breaks the $1,000 price barrier for such software. Logicaps replaces general-purpose schematic-capture packages that range from $5,000 to $10,000. With it, the user can create interactively an EPLD schematic, using familiar logic symbols on the screen of a work station based on an IBM Corp. Personal Computer.

The software, which Altera is introducing this week, eliminates the need for EPLD users to apply Boolean algebra design techniques to develop logic

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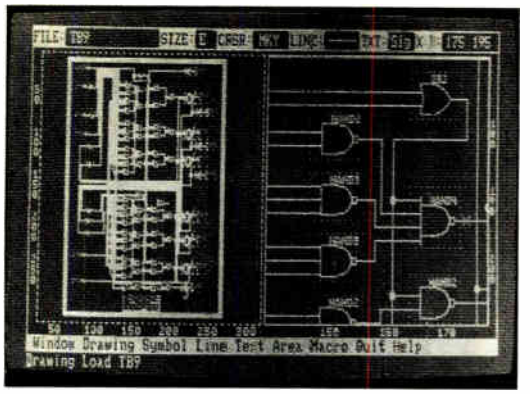

NO MATH. Altera Corp.'s Logicaps lets users program erasable PLDs without using Boolean algebra.

functions, says David Laws, vice president of marketing. And it significantly reduces the time it takes to design with high-density 1,000- to 2,000-gate EPLDs.

"Although Boolean design methods are adequate for devices with low equivalent gate complexities, it is inefficient to try to write equations for today's high-density CMOS EPLDs, such as our 2,000-gate EP1800," says Laws. "While some of the popular PC-based schematic-capture packages from Futurenet and P-CAD have been adapted by Altera and others for use with such high-density EPLDs, the pricing structure of these products has limited their use."

Along with Altera's newly revised A+Plus EPLD development software, Laws says Logicaps will let engineers create EPLD designs by combining macros from a TTL behavioral library consisting of many 7400-series CMOS logic functions. The software also contains a redundant-gate eliminator, or macro-muncher, which frees unused components in a macro for use in other logic functions.

The user simply presses a single key, and Logicaps automatically generates a netlist file, Laws says. And because Logicaps automatically generates design files, he says, it eliminates the intermediate translation steps necessary with other schematic packages.

TWO WINDOWS. "Coupled with Altera's A+Plus software, Logicaps provides an efficient, totally integrated working environment for EPLD designers," Laws says. Key features include area etching, orthogonal rubber-banding, two windows for editing, a rapid screen redraw rate, multilevel zooming, and direct output to the A+Plus software.

With the area-editing feature, the user can define an area of the schematic for manipulation, then move, copy, or delete components within it. With orthogonal rubber-banding, component symbols that have wires connected to them may be stretched in both vertical and horizontal directions, causing the attached signals to move with the component. As components are rubber-banded, signal routing remains orthogonal, which means wire segments remain at continuous right angles to each other. Without such a feature, says Laws, moving components causes a "rat's nest" of signals requiring manual clean-up by the designer.

Logicaps also provides real-time graphic feedback when components are moved or copied. If the user places the cursor within the component-recognition area and presses the mouse button, says Laws, the component is highlighted and remains so as it is dragged from point to point within the schematic.

Logicaps costs $950 and comes on a 5¼-in. floppy disk for use on PC/XT and PC AT work stations. A complete development system, designated the PLCAD4 and including Logicaps, A+Plus, and a software-controlled programming module, is available for $3,250.

Logicaps can also be used with Intel Corp.'s iPLD development system, which is built under license from Altera. The company also offers a free demonstration disk. *-Bernard C. Cole*

Altera Corp., 3525 Monroe St., Santa Clara, Calif. 95051.
Phone (408) 984-2800 [Circle 381]

SMART-POWER TESTER IS ONLY $55,000

Axiom Technology Corp. is making it easier and less expensive to test smart power chips. Its Smart Power subsystem ties to its AT100 work station to exercise high-power portions of a chip and digital logic simultaneously.

At $55,000, a basic configuration is half the price of testers that must be reconfigured each time a different part type is tested, Axiom says. "So far, the competition can only test smart power devices on a part-by-part basis by adding appendages," says James Seaton, business development manager.

The configurable subsystem's high-power instrumentation includes five current-source options and two high-voltage sources, along with an 80-pin high-voltage matrix and an 80-channel high-voltage logic detector. For high-current needs, Smart Power users can choose one or two floating 400-W four-quadrant voltage/current sources. The choices range from ±20 V at ±20 A to ±100 V at ±4 A. The sources use standard interfaces and can be connected independently, in series, or in parallel.

Users can select up to two high-voltage sources, including 325 V at 800 mA and ±500 V at ±80 mA. These can be used either as voltage sources for leakage measurements or as current sources for breakdown-voltage testing; for example, they can be used to make parallel leakage measurements. For faster leakage testing, Smart Power boasts four output channels with current meters where competing equipment has only one channel and meter.

The high-voltage matrix makes possible high-throughput parallel measurement and can switch four high-voltage measurement lines or four standard 2-A sources among 80 output pins. Mercury relays and Teflon insulation provide isolation to more than 700 V and current rating of 2 A per pin. Smart Power's logic detector operates at up to 500 V to offer greater speed in testing devices with high pin counts.

ADAPTABLE. The Smart Power subsystem tests logic and power circuitry together.

Digital instrumentation allows users to program test patterns using loops, branches, and subroutines. Digital signals are fully synchronous with other system instrumentation so that the multiple tests the system performs interact properly.

The system has six independent timing channels, which generate accurate edge placement for clocking a device, for fully programmable edges with 2-ns resolution at data rates as high as 4 MHz. The control memory is 32-K per pin, with waveform memory operating at 64-K per pin. The Smart Power system is available now. *-Debra Michals*

Axiom Technology Corp., 375 Elliot St., Newton, Mass. 02164.
Phone (617) 965-8010 [Circle 382]

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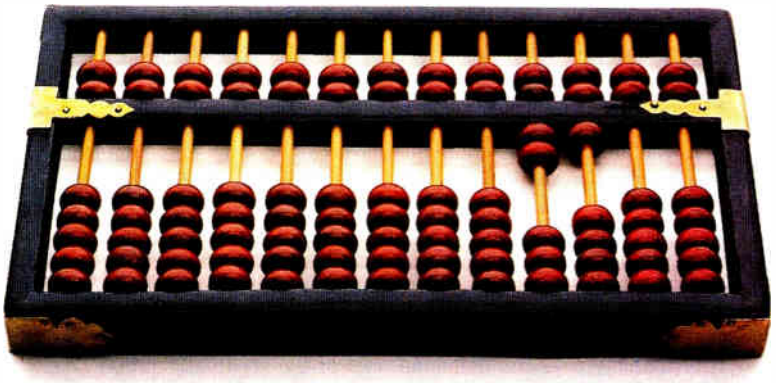

DIGITAL BY ANALOGY.

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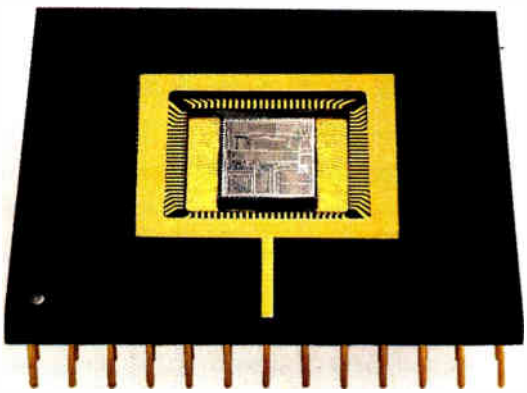

DIGITAL BY ANALOG.

For DSP and numeric processing, your best source of digital is Analog, the industry's leading supplier of signal processing ICs.

Our number crunchers include a superior, high speed floating-point chip set. Along with the broadest line of fixed point multipliers and multiplier/accumulators.

For microprogram sequencing and data address generation, Analog offers innovative Word-Slice™ devices – fast, functional and compact.

For a single-chip solution, we have the industry's highest-performance DSP processor. A powerful 8 MIPS machine, supported with first-class development tools.

Analog Devices – the pioneer of high-speed CMOS in DSP – manufactures these VLSI components in a 1.5 µm CMOS process. So they're fast, cool, and reliable. And they are available now, with full support of MIL-STD 883B, Rev. C.

For more information, call your nearest Analog Devices, Inc. sales office. Analog Devices, Inc.: Austria (222) 885504; Belgium (3) 237 1672; Denmark (2) 845800; France (1) 4687-34-11; Holland (1620) 81500; Israel (052) 28995; Italy (2) 6883831 (2) 6883832 (3) 6883833; Japan (3) 263-6826; Sweden (8) 282740; Switzerland (22) 31 57 60; United Kingdom (01) 9410-466; West Germany (89) 570050.

ANALOG DEVICES

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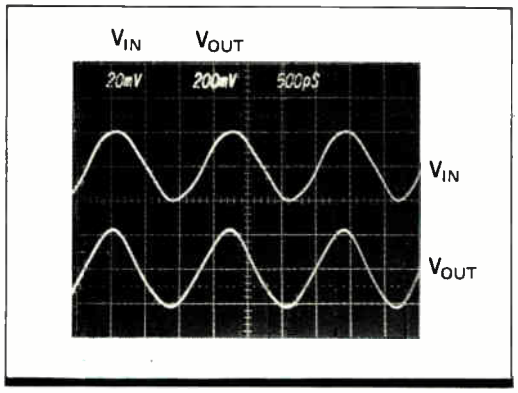
COMPARATOR IC TACKLES HIGH-SPEED SIGNALS

ECL CHIP IS FAST ENOUGH TO COMPETE WITH DISCRETE AND HYBRID COMPARATORS FOR SIGNAL-CONDITIONING TASKS

Systems requiring high-speed linear signal processing will now be easier to design, thanks to a new family of extremely fast comparators and other monolithic components from VTC Inc. First in the new line is the VC7695, which the company bills as an ultrahigh-speed comparator on a chip.

The VC7695 features guaranteed propagation delays of 1.9 ns across the 0°C-to-75°C commercial temperature range and 2.0 ns on parts built for the military range, –55°C to 125°C. VTC specifies typical delays as 1.4 ns.



NO TRADEOFFS. Users of the VC7695 comparator don't have to give up precision for increased speed.

At those speeds, the VC7695 significantly outstrips competitors such as Analog Devices' AD9685, which offers 2.2-ns typical delays at 25°C. "Our guaranteed propagation delays are faster than the typical delays specified for competitors' parts," boasts Jerry Thimsen, VTC's product line manager for linear signal-processing products.

ADC CONDITIONING. The VC7695's performance will pay particular dividends in such applications as signal conditioning for the current generation of fast flash analog-to-digital converters and in high-speed fiber-optic telecommunications tasks. Such jobs typically require the use of hybrid or discrete implementations, Thimsen says, but the VC7695 offers the necessary speed in a monolithic, off-the-shelf part.

When used as a telecommunications line receiver, the VC7695 comparator can handle speeds of 600 MHz to 1 GHz. That compares with maximums of about 400 MHz for competitive standard parts, Thimsen says. Moreover, where other monolithic comparators can handle signal conditioning for ADCs that run between 50 and 100 MHz, the VC7695 can support flash devices specified at 100 to 300 MHz, he says.

VC7695 users can take advantage of the part's superior speed without giving up the precision found on slower comparators, says Thimsen. The part's maximum input offset voltage of ±5 mV and input offset current of 5 μA maximum equals that of competitive parts.

The VC7695 owes its speed to a 2-μm double-layer-metal ECL process that jacks up the transistor transition frequency (f_T) to 6 GHz. "Right now, there's only one other company in the marketplace offering that type of process, and that's Tektronix," says Thimsen. "They're offering it on their semicustom type of product, but they're not doing any standard products."

VTC plans to team its ECL technology with another 2-μm process it calls complementary bipolar to bring out a complete family of standard, high-speed linear signal-processing parts over the next two years, Thimsen says. The complementary bipolar process has already been used on the company's VA705 and VA706 high-speed precision operational amplifiers introduced last December. Follow-on products will include additional comparators, op amps, and flash ADCs and DACs, Thimsen says.

Other VC7695 specifications also match up well against pin-compatible parts such as the 9685, as well as devices such as Plessey's SP9685 and Advanced Micro Devices' AMD9685, Thimsen claims. VTC will offer the new part in several types of 16-pin packages. Depending upon market demand, the company may also offer the VC7695 in a 14-pin package to match Fairchild's UA6685, with which the VC7695 is functionally compatible, Thimsen adds.

The VC7695 is available now, VTC says. In 100-unit quantities, it is priced at $10.25 per part housed in a plastic DIP, $10.75 in a small-outline IC package, $11.35 in a Cerdip, and $21.60 in a 10-pin metal can. The 35-by-40-mil dice will be sold unpackaged at $7.50 in 100-unit quantities. *–Wesley R. Iversen*

VTC Inc., 2401 E. 86th St., Bloomington, Minn. 55420.
Phone (612) 851-5000 [Circle 360]

MILITARY IC HANDLES BUS-CONTROL TASKS

The UT1553B supports both MIL-STD-1553B bus-controller and remote-terminal functions. The chip, which is designed for the military and aerospace industry, also provides specialized memory management and direct-memory-access operations.

The chip automatically polls and executes message transactions, provides programmable interrupts, and generates status information. It contains two Manchester decoders for redundancy, a Manchester encoder, serial-to-parallel and parallel-to-serial conversion registers, a programmable interrupt controller, timers, and a programmable memory-management unit.

The design also gives users the flexibility to implement a pseudotransparent dual-port RAM configuration. Available now, the UT1553B sells for $895 each in lots of 100 pieces.

United Technologies Microelectronics Center, 1575 Garden of the Gods Rd., Colorado Springs, Colo. 80907.
Phone (800) 645-8862 [Circle 365]

CMOS GATE ARRAY BOASTS 1-NS DELAYS

Propagation delays as low as 1 ns mark the SLA 7000 series of six gate arrays that range in size from 2,232 to 9,250 cells. The silicon-gate CMOS arrays are fabricated using 1.5-μm design rules and two-layer metalization.

The manufacturer targets the series at applications where high speed and low power consumption are required. The SLA series comes in a variety of packages including chip carriers, DIPs, surface-mountable packages, flatpacks, and pin-grid arrays.

Typical design time is five to seven weeks from completion of logic simulation to delivery of prototypes. Engineering charges start at $15,000.

S-MOS Systems, 50 W. Brokaw Rd., Building 7, San Jose, Calif. 95110.
Phone (408) 993-1212 [Circle 366]

CMOS PROCESSOR CUTS POWER USE BY 75%

Users of Advanced Micro Devices Inc.'s bipolar Am29117 32-bit microprocessor can cut power consumption in their designs 75% by replacing it with the CMOS version, the Am29C117. The chip reduces power consumption to less than 1 W. At 120-ns system cycle time, the Am29C117 is just 5 ns slower than the bipolar version.

The microprogrammable Am29C117 has a flow-through architecture with dedicated ports that enhance system throughput by eliminating I/O-bus turn-

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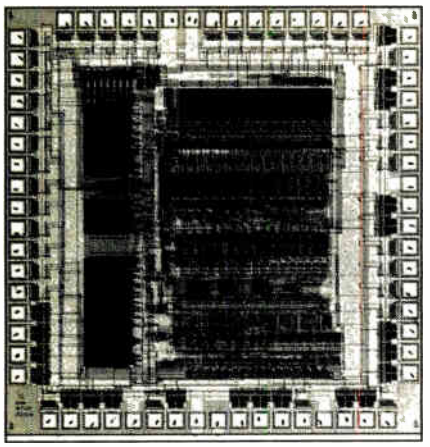


around delays. This improves system design by reducing both the parts count and the design time needed.

A three-input arithmetic logic unit operates on two data operands, and the third input allows two-operand instructions with masking. A 16-bit barrel shifter can shift or rotate a word up to 15 bits long in a single instruction. Available now, the chip sells for $95 each in lots of 100 pieces.

Advanced Micro Devices Inc., 901 Thompson Pl., P. O. Box 3453, Sunnyvale, Calif. 94088. Phone (408) 732-2400 [Circle 367]

CMOS COMPARATOR DRIVES 60 mA

The ALD 2301, a silicon-gate CMOS dual comparator, features a high-drive current of 60 mA but a quiescent-state current drain of only 55 μA for each comparator. This setup allows fanouts of 45 low-power Schottky TTL loads and very high resistive load-driving capability for LEDs and relays.

The ALD 2301 boasts a high input impedance of 10^{12} Ω and a 10-pA input offset current. The two eliminate not only any loading of the signal source, but dependence on signal-source resistance, the company claims.

Typical response time is 650 ns. The chip operates from 3 to 12 V and comes in four offset voltage grades: 2 mV for the 2301A, 5 mV for the 2301B, 10 mV for the 2301, and 20 mV for the 2301C. Available from stock, the 2301 in a plastic DIP costs $1.26 each in lots of 100.

Advanced Linear Devices Inc., 1030 W. Maude Ave., Suite 501, Sunnyvale, Calif. 94086. Phone (408) 720-8737 [Circle 368]

DUAL-PORT RAMS USE MASTER/SLAVE SETUP

A set of four dual-port static RAMs features access times of 55 ns over the full commercial temperature range. The 1-K-by-8-bit IDT7130 and the 2-K-by-8-bit IDT7132 are the set's master SRAMs, containing arbitration logic to detect simultaneous access of a memory location from both of the memory's ports.

The corresponding slave parts, the IDT7140 and IDT7142, have the same capacities and organizations, interfacing with the masters without any external logic. Data-bus width can be expanded easily to 16 or more bits.

Both pairs feature two fully independent address and data ports with separate control lines that facilitate simultaneous read and write operations to separate locations in the memory. Each port also has its own chip-enable and power-down line so that power can be reduced if one port is not needed.

Typical power consumption is 325 mW. Prices begin at $13.38 in lots of 100 for the IDT7130 and IDT7140 and $20 for the IDT7132 and IDT7142. Military-grade versions are also available.

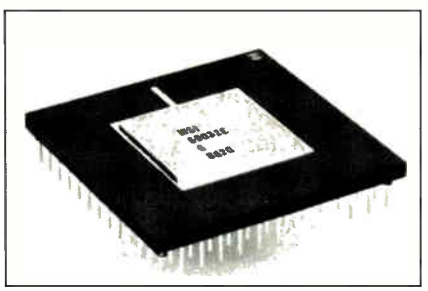
Integrated Device Technology Inc., 3236 Scott Blvd., Santa Clara, Calif. 95054. Phone (408) 727-6116 [Circle 369]

BIT-SLICE CMOS IC RUNS AT 20 MHz

The WS59032E 32-bit bit-slice microprocessor is faster than bipolar parts and consumes less power. Using a 20-MHz clock, the CMOS chip provides a read-modify-write cycle of only 52 ns.

This cycle is 56% faster than a bipolar ECL 32-bit processor built using Advanced Micro Devices Inc.'s 2901s and 48% faster than the company's earlier version, the WS59032D. Power consumption is 350 mW, less than 4% of the power requirement of bipolar parts.

The microprogrammable chip has the



flexibility to emulate almost any digital computing machine. It is suitable for such applications as radar array processors, digital signal processors, graphics work stations, superminicomputers, and military electronics.

The WS59032E is fabricated in the company's proprietary 1.2-μm CMOS technology. It integrates the functions of eight 2901s and three 2902s and includes 32 on-board registers that enhance throughput by eliminating many external memory fetches. In lots of 100 pieces, the chip is $93 each in 101-pin ceramic grid arrays. Military grade versions are also available.

Waferscale Integration Inc., 47280 Kato Rd., Fremont, Calif. 94538. Phone (415) 656-5400 [Circle 370]

THE COMPLETE SOLUTION FOR MICROCODED PROCESSORS.

Analog Devices' ADSP-1401 and ADSP-1410 offer you the highest speed and the greatest functionality for key tasks in microcoded systems – microprogram sequencing and data address generation.

The ADSP-1401 MicroProgram Sequencer is the industry's most advanced IC for generating microcode addresses. It supplies 16-bit addresses with a clock-to-address delay of just 25ns. The chip supports 10 maskable, prioritized interrupts, as well as traps. A 64-word internal RAM is user-configurable for subroutine stack, register stack, and parameter storage. Four event counters streamline nested loops.

The ADSP-1410 is the industry's only IC dedicated to flexible, high-speed data address generation. It provides 16-bit pointers to data memory 30ns after the clock edge. Its thirty registers hold address pointers, offsets, comparison values, and initialization values. With its powerful zero-overhead looping structure, the device can – in a single cycle – output an address, modify it, and conditionally branch to an initialization address.

Both Word-Slice™ components offer low-power CMOS technology (≤ 375 mW) in a 48-pin ceramic or plastic DIP. And, microcode system development tools and support are available from many third parties, including Hewlett-Packard, Step Engineering, and HiLevel Technology.

For more details, call your nearest Analog Devices, Inc. Sales Office.

ANALOG DEVICES

Circle 144 on reader service card

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LOW-COST GEAR BOOSTS ARCNET PERFORMANCE

STANDARD MICROSYSTEMS MAKES LAN-BUILDING EASY WITH ITS CONTROLLER, DUAL-PORT HUB, AND STARTER KIT

Standard Microsystems Corp. is applying its Arcnet expertise to a flurry of products that boost the local-area network's performance, lower per-node costs, and make the LAN more flexible. The new products include the first LAN card to employ surface-mount technology, a dual-port hub that lets users add eight nodes but occupies only one port in the main hub, and a starter kit that lets users set up small Arcnets at low cost.

Arcnet, which was developed by Datapoint Corp., is a high-performance network using a token-passing protocol in a logical bus topology. It uses active repeaters called hubs to isolate nodes and provide signal regeneration; with the hub, users can build networks with free-form tree topologies.

The logical bus provides more flexibility in adding and deleting nodes than do such physical ring networks as the IBM Corp. Token Ring Network. With ring networks, the net has to be interrupted, the ring opened, and the system software reconfigured to add nodes. With the logical bus, nodes can be added without interrupting service. The network reconfigures itself, a process in which each node announces to the rest of the nodes that it is on the net.

SMC's expertise with the network stems from the fact that it is the sole producer of both the Arcnet controller chip, the COM9026, and the Arcnet transceiver chip, the COM9032. It has also devised a high-impedance transceiver driver, called the Hit module, that doubles the maximum possible distance between nodes from 2,000 to 4,000 ft.

The new network card, the PC110, is functionally identical to Standard Microsystems' PC100. But the earlier product occupies a full-size card in an IBM Corp. Personal Computer, whereas the PC110 fits into a half-height slot, thanks to surface mounting. The board will sell for $545 when available in September.

The controller on the PC110 provides a simplified interface between the IBM PC and the Arcnet. The card incorporates surface-mount versions of the 9026 network controller and the 9032 transceiver chip to provide complete Arcnet protocol handling. A 2-K-byte on-board data-packet buffer provides four pages of packet storage. The user may dynamically define this memory to buffer both transmit and receive functions.

ETHERNET TOO. The controller may be polled or driven by interrupts. An on-board 8-K PROM socket means the user can install an automatic-booting PROM so that less expensive diskless personal computers can access the network. Although the 2.5-Mb/s Arcnet was designed for baseband coaxial cable transmission, SMC's cards support other media, including Ethernet cable and broadband types.

The second new product, a dual-port active hub called the Active Link, revolves around the company's Hit driver module and its PC200 controller card, which was devised to daisy-chain together up to eight nodes while occupying only one port in the hub. Without the PC200, users who wanted to go beyond the eight-node limit of the hub would have to connect two hubs together. The PC200 is functionally identical to the PC100 and PC110.

The Active Link is an inexpensive way to add ports, which in the eight-port hub cost about $100 apiece. By adding nodes and taking up only one port, the cost can drop eightfold. The Active Link also adds flexibility in the way users can build nets. It connects two daisy-chained strings of nodes that use the PC200.

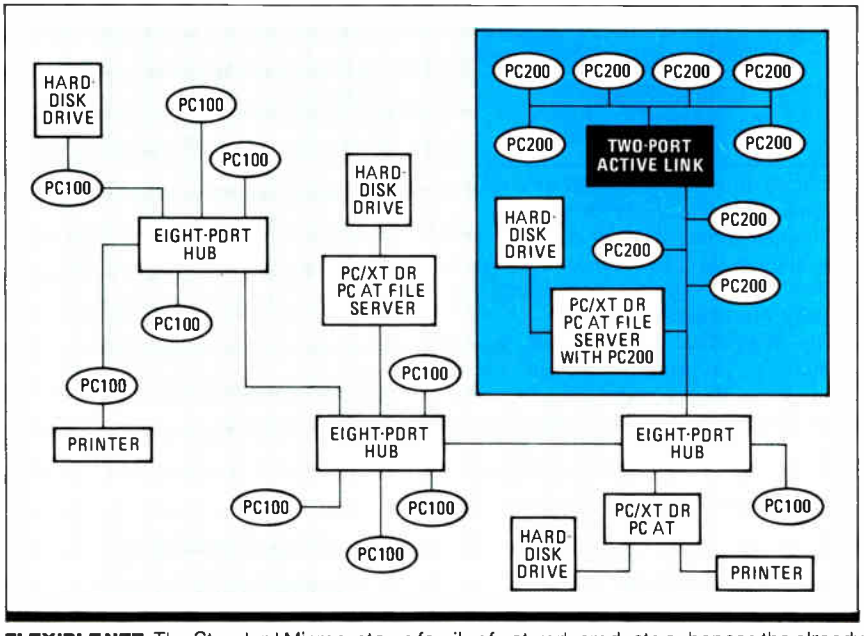
The Active Link provides proper termination for the RG-62/U cable and signal regeneration (through the Hit driver module) to maintain data integrity. Unlike signal-repeating devices in other networks, the Active Link is easy to install and does not decrease the speed of the network bus. In addition, it allows for system cabling flexibility and ease of expansion.

The Active Link sells for $375, with delivery of production quantities in early September. Samples are available now.

The third product, a starter kit, creates virtually instant Arcnets. Each kit contains two network controller boards— either the PC100, PC200, or the fiber-optic version, the PC300—a network software package, and 20 ft of cable. The software is either ViaNetix' ViaNet or Novell's Advanced NetWare, and the cable may be RG-62/U or fiber-optic cable.

Pricing for the Arcnet starter kit with PC100s and the Advanced NetWare software is $2,195. For starter kits with PC100s and the ViaNet software, pricing is $1,298. Both kits are available now. *–Steve Zollo*

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, N. Y. 11788.
Phone (516) 273-3100 [Circle 440]



FLEXIBLE NET. The Standard Microsystems family of network products enhances the already flexible Arcnet. For example, the Active Link connects strings of daisy-chained nodes.

VOICE DIAL PHONE COSTS ONLY $249

To help those too harried to dial or punch numbers, Innovative Devices has come up with a telephone with a voice-activated dialer that will sell for $249. This is considerably less than other voice-activated phone systems.

The sleek-looking telephone claims 99% accuracy on spoken commands using a robust voice-recognition technol-

World Radio History

ogy under the control of a 6502 processor. Using a variant of template-matching voice-recognition technology, a speaker first trains the recognizer by repeating up to 100 names. These are digitized, analyzed, and stored as a template in 64-K bytes of RAM.

With the template established, both home and office phone numbers are entered through the keypad and mapped to a template. To place a call after the recognizer is trained, users pick up the handset and repeat the name.

A match is performed between the stored template and the spectral parameters of the spoken name. A synthesizer repeats the match, then generates either pulse or tone dialing of the number stored in the directory.

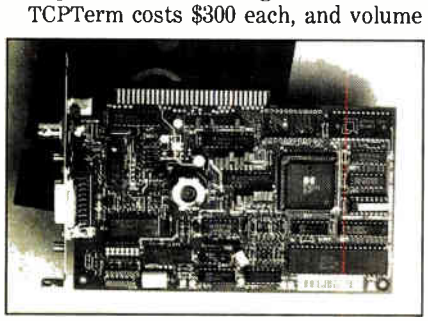
Innovative Devices, 1333 Lawrence Expressway, Suite 257, Santa Clara, Calif. 95051. Phone (408) 984-1616 [Circle 452]

PROGRAM LETS PCs RUN ON ETHERNET LAN

IBM Corp. Personal Computers can be tied into local-area networks that run the high-level Transmission Control Protocol/Interconnect Protocol by using TCPTerm. It is the first software package to fully integrate PCs into Ethernet LANs, its maker claims.

The program enables PCs to emulate VT100 terminals and transfer files through asynchronous ports, 3270 Systems Network Architecture sessions, and hosts including Digital Equipment Corp. VAX minicomputers and Sun Microsystems Inc. work stations. The package supports the standard TCP/IP set developed by the Defense Department and used in many computer-aided engineering systems. It supports coaxial and fiber-optic Ethernet cabling schemes.

TCPTerm costs $300 each, and volume



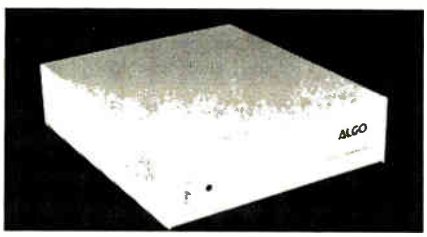
discounts are available. Delivery takes 30 days.

Bridge Communications Inc., 2081 Stierlin Rd., Mountain View, Calif. 94043. Phone (415) 969-4400 [Circle 447]

MULTIPLEXER BUILDS 500-NODE NETWORKS

Not limited to point-to-point communications, the ALGO MC610 statistical multiplexer also works with multiple composite data channels. It thereby allows users to build networks with up to 500 nodes while keeping telephone costs down.

The unit's port-switching features allow any terminal or computer with an RS-232-C interface to connect to any oth-



er local or remote RS-232-compatible unit. That means microcomputer clusters can pass files back and forth with other clusters, computers, or printers on the network.

Original-equipment manufacturer discounts are available now for the MC610, which lists for $1,495 each.

Algo Inc., 9198C Red Branch Rd., Columbia, Md. 21045. Phone (800) 252-2546 [Circle 446]

SOFTWARE SIMULATOR TESTS LOCAL NETS

The Smart LPT program lets users compare competing local-area networks in a simulated environment, the manufacturer says. Smart LPT, for LAN Performance Test, measures the network's throughput and productivity by simulating applications and testing the last, or nth, network node.

The program is built around its maker's Smart Software system, which includes data-base-management, spreadsheet, graphics, word-processing, and communications packages and an application programming language. The system runs on IBM Corp. Netbios and DOS CALL 3.1-compatible LAN operating systems.

The menu-driven program can print results in either spreadsheet or bar-chart form, and it can be used either to compare different networks or different configurations of the same network. Available now, the package lists for $49.95.

Innovative Software, 9875 Widmer Rd., Lenexa, Kan. 66215. Phone (913) 492-3800 [Circle 445]

FLOATING-POINT CHIP SET WITHOUT COMPROMISE.

Analog Devices' ADSP-3210/3220 floating-point multiplier and ALU are the industry's best available solution for fast IEEE arithmetic. This chip set provides blazing throughput and low latency – without compromise.

The chips execute an extensive set of operations on 32- and 64-bit IEEE floating-point and 32-bit fixed point. So, systems using them have the flexibility to support all standard data formats.

Circuit innovations and a fast 1.5μm process allow each chip to achieve 10 MFLOPS for most operations. And with CMOS, there are no power or reliability penalties.

What's more, number-crunching speed doesn't come from cumbersome pipelining. Because it has just one internal pipeline stage, the ADSP-3210/3220 is the industry's lowest-latency double precision chip set in production. And, with this architecture, microcode development is simple.

For more details, call your nearest Analog Devices, Inc. Sales Office.

ANALOG DEVICES

Circle 145 on reader service card

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PRODUCTION EQUIPMENT

RECYCLING UNIT CUTS ACID CONSUMPTION BY 95%

DISTILLATION REMOVES CONTAMINANTS SO THAT CHEMICALS CAN BE REUSED IN WAFER-CLEANSING BATHS

Cleanliness is next to godliness" for chip makers, so they must keep replacing the chemical baths used to clean wafers. That's an expense that Athens Corp. aims to pare with a distillation and extraction unit that it calls the Micro Chemical Reprocessor. The new Athens unit removes the contaminants that the acids pick up as they clean wafers. The acids can be reused a number of times, and chip makers can cut acid consumption by up to 95%, the company claims.

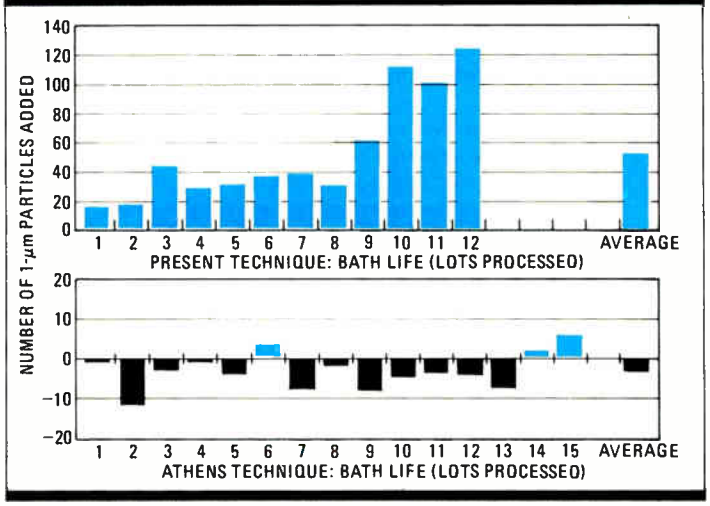
Wafers are often cleaned 25 to 50 times during processing, and the particles that they leave behind in the chemical baths can contaminate all subsequent wafers. Moreover, the likelihood of these particles causing a fatal chip defect increases as the design rules for very large-scale integration shrink toward 1-μm and below.

Frequent disposal of high-cost VLSI-grade chemicals, such as sulfuric acid, has been necessary to maintain chemical purity. But frequent disposal is costly, jeopardizes worker safety, and can damage the environment.

The Micro Chemical Reprocessor from the 11-month-old Oceanside, Calif., company attaches to wafer-cleaning equipment already used in circuit fabrication facilities. Under microprocessor control, the system recycles the acids to return them to their original strength and purity. It provides a continuous flow of fresh chemicals to clean each lot of wafers, reducing both particulate and trace-impurity contamination of the wafers and the amount of chemicals that must be discarded, says Athens president Scot Clark.

Until now, IC manufacturers have had to replace contaminated acid cleaning baths every few hours—and typically it costs as much to dispose of the chemicals as it does to buy them. But the Micro Chemical Reprocessor cuts acid consumption by 95%. This means users need to purchase and dispose of only 90 gallons of acid a month for a static bath rather than 1,800 gallons currently used. So the system pays back its $350,000 price in about 10 months, the company claims.

WAFER-LOT DEFECTS AFTER EACH BATH



Athens' reprocessor reduces particles by as much as 10,000 per milliliter. The point-of-use system also analyzes particle counts and trace impurities on line and in real time, increasing process control. All processing parameters are measured continuously, providing real-time information on the status of the chemicals, the company says.

All static baths need an oxidant, such as hydrogen peroxide. In the standard wafer-cleaning setup, this chemical must be refreshed by adding more hydrogen peroxide periodically—and that adds even more impurities. Athens' reprocessor solves this problem by generating oxidants directly from the sulfuric acid as needed.

The resulting oxidant is much more pure than hydrogen peroxide, and the resulting bath is of extremely high purity. In addition, the power of the oxidizing agent is constant and controlled, rather than diminishing over time.

The Micro Chemical Reprocessor interfaces with a host computer through the Semiconductor Equipment Communications Standard I and II protocols. It attaches to existing wafer-cleaning equipment and is installed in the chase or service area.

The microprocessor supervising its operation also monitors the instruments for out-of-control conditions. The flush-mount wall unit has a 3-by-5-foot footprint and no moving parts.

The Micro Chemical Reprocessor is available four months after receipt of an order. The first unit has been delivered to Fairchild Semiconductor Corp., the company says —*Jerry Lyman*

Athens Corp., 602 Airport Rd., Oceanside, Calif. 92054.
Phone (619) 757-4370 [Circle 420]

NOW SMALL FIRMS CAN DO SMT SOLDERING

Soldering techniques that dispense solder paste for the automated assembly of surface-mounted components on pc boards are a popular alternative to selectively screening pastes—and now they are within reach of smaller companies. Creative Automation Co. is bringing out a smaller, less expensive version of its solder-paste machine, which has sold well to manufacturers with high-volume production lines.

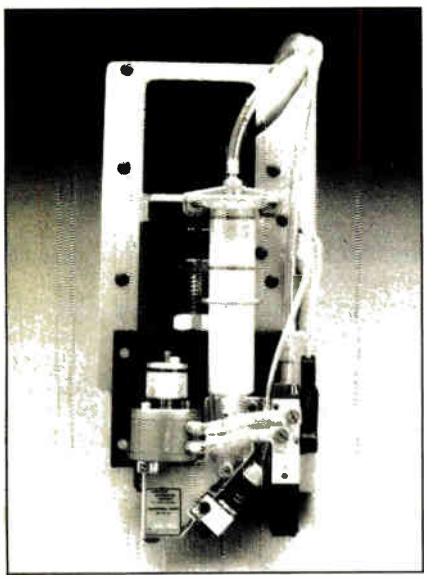
The new ADM 1412 three-axis programmable solder-paste system provides an 8.8-in./s dispensing speed over a 14-by-12-in.-board surface area. The larger, existing model, ADM 2220, is slightly faster, dispensing at 11 in./s over a 22-by-20-in. surface area.

The ADM 1412's base price, including computer and software, is $22,719, compared with the ADM 2220's price of $39,450. The ADM 1412 is a tabletop model, with fewer options than the larger ADM 2220, notes Jerry Asher, sales manager for Creative Automation. "It's built as an economy model, for smaller shops."

The system, controlled by any personal computer, works by positioning a head over a pc board and precisely placing tiny solder-paste dots—as small as 0.018 in. in diameter on 0.025-in. centers. When the board is removed, a component is placed on the surface so the contact points on that device are aligned with the solder dots. Finally, the entire assembly is put through a reflow oven, which heats the solder and completes the electrical/mechanical connection of the circuit device to the board.

"Manufacturers have discovered that higher yields are possible with precision

World Radio History



TOGETHER. The ADM 1412's high-pressure piston pump keeps mixtures from separating.

placement of solder paste," he adds. "The 99.96% repeatability and the versatility of changing placement through simple programming make dispensing the method of choice for more surface-mount technology applications."

The ADM 1412 is designed to dispense with a resolution to within 0.0001 in. along both the X and Y axes. The programmable Z-axis resolution, the vertical placement resolution of the solder tip, is 0.0005 in.

NO SEPARATION. At the heart of the 1412 is a patented solder-paste dispensing pump that produces an output of 4 dots/s. The company's pump solves a critical problem in dispensing paste, the separation of the mixture of binder, solvent, and flux, by using a "positive displacement" method. The piston stroke pump works by applying high pressure (between 5,000 and 10,000 lb/in.^{2}) on only a minute volume deposited in the pumping chamber, thus eliminating the possibility of separation.

Systems are available now. The system is also available with an optional touch-screen controller, which offers menu-driven operation. *–Ellie Aguilar*

Creative Automation Co., 11641 Pendleton St., Sun Valley, Calif. 91352.
Phone (818) 767-6220 [Circle 421]

COUNTER INVENTORIES PARTS ON TAPE REELS

The Kwikcount model B530 automatic counter takes fast and accurate inventory of tape-mounted components. The portable system, which runs on rechargable batteries or on an ac line, can keep track of up to 100,000 parts at a time.

The model B530 counts axial parts and, with a turret-head adapter, can count multilegged radial components. The system uses an LED and photodetector sensor. As each part passes between the LED and sensor, interrupting the latter's reception of light, the counter is incremented or decremented. A ½-in. LCD displays the parts count at all times.

The B530 not only simplifies inventory taking but lets users count out only the number of parts needed for an assembly project. The unit counts backwards also, so if too many parts are run out, they can be reeled back.

Available now, the Kwikcount B530 is priced at $595.

Heller Industries Inc., 4 Vreeland Rd., Florham Park, N. J. 07932.
Phone (201) 370-6800 [Circle 427]

SCREEN PRINTER SHIFTS AMONG FOUR CYCLES

A program in an on-board EPROM permits the Accu-Coat model 3200 semiautomatic screen printer to shift rapidly among any one of four basic printing cycles: flood/print, print/flood, single bidirectional, or double bidirectional.

Squeegee motions are controlled by magnetic reed switches on the travel bar of the yoke. The model 3200 will screen substrates up to 4 by 6 in., with a registration to within 0.0003 in. It can be programmed to do 2,000 cycles/h.

Priced at $7,970, the model 3200 is available now.

Aremco Products Inc., P. O. Box 429, Ossining, N. Y. 10562.
Phone (914) 762-0685 [Circle 430]

SURFACE-MOUNT SETUP COSTS ONLY $35,000

A turnkey system called System 842 allows companies to rapidly acquire surface mount technology at a lower cost than previous SMT systems. The System 842 includes the SPS-812 high-reliability stencil printer, the SMT-4090 robotic pick-and-place machine, and the VP-200 vapor-phase reflow solderer. Available now, it costs under $35,000, whereas other systems cost $100,000 and up.

The vacuum-frame stencil printer works on boards as large as 8 by 12 in. Precision adjustments along the X, Y, and Z axes ensure perfect registration of paste on the smallest of solder dots. The heart of the system is the pick-and-place machine, which handles chips supplied in bulk, on waffles, in sticks, or on tape. Fully outfitted, the system can place as many as 50 different parts.

The vapor-phase reflow solderer displays vapor and cooling-water temperatures on digital readouts.

Henry Mann Inc., Manix Division, Marketing Dept., Mann Road, Huntingdon Valley, Pa. 19006. Phone (215) 355-7200 [Circle 425]

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For more details, call your nearest Analog Devices, Inc. Sales Office.

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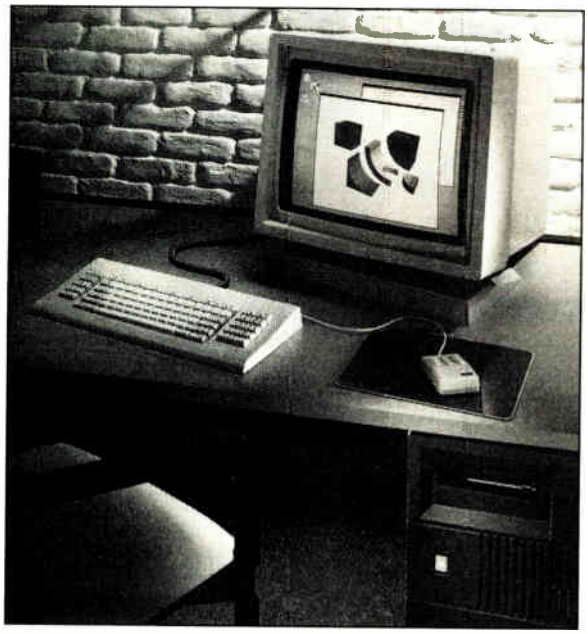
GRAPHICS BOARDS MAKE SUN STATIONS 80% FASTER

THE GRAPHICS PROCESSOR AND GRAPHICS BUFFER PROVIDE QUICKER RESPONSE FOR CAE AND SOLIDS MODELING



FASTER STILL. Sun's two graphics boards will work in the Sun 3/160 and a new work station based on the 20-MHz 68020.

Users of Sun Microsystems Inc.'s work stations can now add options that will speed up their graphics processing capability by 80%. Called Graphics Acceleration Options, the two-board set comprises the GP+ graphics processor and the GB graphics buffer.

The two boards afford faster response for two-dimensional applications, such as computer-aided engineering, and for 3-d applications, such as mechanical computer-aided design and solids modeling. The options can boost the graphics performance of the Sun 3/160 work station family and that of a family the company will unveil next month at the Siggraph show in Dallas. The new work stations will be built around the new 20-MHz version of Motorola's 68020 32-bit microprocessor.

QUICK DRAW. The drawing speed of the GP+ graphics processor is 20% faster than the previous-generation board. It has a vector drawing rate of 1.75 million pixels/s, as compared with 1.5 million pixel/s. It can transform, clip, and scale a 3-d image at a rate of 45,000 vectors/s as compared with the older board's 25.000 vectors/s.

The GP+ graphics processor architecture is based on two pipeline stages, the viewing processor and the painting processor. Each is implemented with a high-speed 29116 bipolar bit-slice processor from Advanced Micro Devices Inc. of Sunnyvale, Calif. The viewing processor also uses the 1232 and 1233 floating-point data-path chip set from Weitek Corp., Sunnyvale, to perform all transformation and clipping operations in floating-point coordinates, with no loss of performance. The chips are CMOS versions of previous-generation bipolar chips, the 1032 and 1033. They give the viewing process a speed 2½ times that of the previous version of the processor.

Sun expects even more performance once it adds Weitek's next generation of the data-path chips, called the 3132. On one chip, the multiply and add operations will work in parallel so that a multiply-and-accumulate operation can occur in 50 ns, half the time now required. In addition, the same chip also contains a divide capability and a lookup table. The chip is said to be the first to combine all three functions.

In performing a transformation, the GP+ viewing processor converts the image stored as a display list in the modeling-coordinate system into the device-coordinate system of the work-station CRT. The clipping operation removes any part of the image that is outside the viewing area of the CRT screen after the designer has zoomed in. The viewing processor passes its transformed image to the painting processor.

DOT TO DOT. At this point, the drawing consists of a set of end points that resembles a connect-the-dots drawing. The painting processor not only connects the dots but colors in the spaces between. In addition, it performs hidden-surface removal at the same time.

The painting processor also performs Gouraud shading, the minimum shading required for solids modeling. Also known as smooth shading, Gouraud shading is a computationally intense technique used to render 3-d objects by interpolating the color and intensity of each pixel based on the end points of the polygons that make up an image being displayed on the work station's screen. The result is a smooth transition of color change over the surface of the object.

The GB memory speeds hidden-surface removal in 3-d images. It functions as a 16-bit-per-pixel memory array for Z-buffer depth-sorting algorithms in 3-d applications. This helps boost the Gouraud shading rate, says Sun, because the hardware algorithm allows Z-buffer read operations to overlap with other functions.

The GP+ sells for $6,900, and the GB sells for $4,000. Both graphics boards can be delivered 60 days after receipt of order. *–Jonah McLeod*

Sun Microsystems Inc., 2550 Garcia Ave., Mountain View, Calif. 94043.
Phone (415) 960-1300 [Circle 341]

SILICON GRAPHICS ADDS NETWORK SUPPORT

New support for one popular engineering network and enhanced support for another will help Silicon Graphics Inc.'s work stations communicate with the variety of mainframes, minicomputers, and work stations its customers use. Now the Iris 3000 [*Electronics*, Feb. 10, 1986, p. 57] and Iris 2400 color graphics work stations can use the Network File System (NFS) from Sun Microsystems Inc. They also will be able to make wider use of the Defense Department's Transmission Control Protocol/Internet Protocol.

NFS, which operates independently of machine type or operating system, enables a work station to access a file on a remote work station as if it were a local file. The sharing of data in a heterogeneous network facilitates teamwork among engineers and cuts the amount of system administration by eliminating the need to keep redundant copies of files.

THREE-WAY TRANSFERS. TCP/IP makes it possible to transfer files among the Mountain View, Calif., company's work stations operating under AT&T Co.'s Unix operating system and Digital Equipment Corp. VAX and MicroVAX computers running under the VMS operating system, or IBM Corp. mainframe computers operating under the MVS environment. The new TCP/IP implemen-

World Radio History

POWER LINK. Options let Silicon Graphics' work stations link to powerful computers.

tation allows multiple sessions to execute simultaneously.

Silicon Graphics puts the program code for the TCP/IP transfer protocol in its Unix kernel, not in the Ethernet controller board. Locating the code in the kernel allows Silicon Graphics to fully support and control the TCP/IP capability. The VMS operating system can use the TCP/IP to access the Silicon Graphics Remote Graphics Library. The Silicon Graphics Unix TCP/IP communications support runs concurrently with Decnet, DEC's version of Ethernet.

For the Silicon Graphics TCP/IP software to function properly, the TCP/IP implementation on a DEC computer must be DEC's own or the one from the Wollongong Group of Palo Alto. Similarly, the TCP/IP on an IBM mainframe must be provided by IBM or the Wollongong Group. With the IBM MVS interface, Silicon Graphics provides 3270 communications and file-transfer capability.

The TCP/IP software sells for $1,200, and NFS sells for $2,000; the IBM MVS host link will be no more than $5,000. The Graphics Library Software for DEC will sell for $1,200. The new capabilities will be announced later this month, at the Aug. 18-22 Siggraph conference being held in Dallas. All products will be available in November. *-Jonah McLeod*

Silicon Graphics Inc., 2011 Stierlin Rd., Mountain View, Calif. 94043.
Phone (415) 960-1980 [Circle 340]

ROM BIOS SOFTWARE BOWS FOR 80386

Designers who want to bring to market an Intel 80386-based computer that maintains compatibility with the IBM Corp. Personal Computer family can use the new ROM Bios from Phoenix Technologies Ltd. The Phoenix Bios supports the new features designed into the 80386, including extended CPU diagnostics, full 32-bit memory testing, support for the 80387 numeric coprocessor, and support for processing speeds of up to 20 MHz.

It also takes advantage of the 386 architecture to enhance the performance of the Bios-related function of switching between real and protected modes, used for such tasks as virtual-disk or overlay management. Unlike the company's previous Bios firmware, the 386 Bios is not an emulation of a new IBM hardware environment, but it has been written expressly for the 80386 while maintaining compatibility with the PC AT.

The ROM Bios is available now. The company won't divulge a specific price but has a flexible licensing fee plus a royalty pricing schedule.

Phoenix Technologies Ltd., 320 Norwood Park S., Norwood, Mass. 02062.
Phone (617) 769-7020 [Circle 345]

68020-BASED SYSTEM SUPPORTS 64 USERS

Cromemco's latest 68020-based supermicrocomputer supports up to 64 users. The CS420 system, which runs under the Unix 5.2 operating system, also boasts a 68881 math coprocessor and up to 16 megabytes of error-correcting memory. The system has been benchmarked at 1.05 million Whetstones, owing its high throughput to a triple-cache architecture.

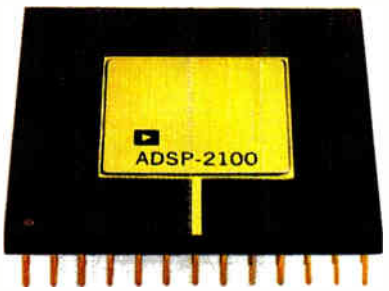
High-speed cache memory is used to speed CPU performance, disk I/O operations, and CRT terminal I/O activity. The 16-K-byte CPU cache uses a two-set associative architecture to provide no-wait-state performance. A four-track cache is provided for each disk drive, and a 2,000-character screen cache is used for each CRT terminal.

The CS420 with 2 megabytes of RAM and a 140-megabyte hard-disk drive sells for $27,995. Systems are available now.

Cromemco Inc., 280 Bernardo Ave., Mountain View, Calif. 94043.
Phone (415) 964-7400 [Circle 347]

GRAPHICS CARD HAS LIGHT-PEN INTERFACE

A light-pen interface is standard with the EGAds enhanced graphics adapter card. The $269 card supports both color and monochrome displays in a variety of modes and comes with versions for the



BREAKTHROUGH PERFORMANCE FROM A DSP MICROPROCESSOR.

Analog Devices' ADSP-2100 is the first single-chip DSP microprocessor to break the bit-slice performance barrier. Now, for the first time, high-performance and ease-of-design are combined in a single CMOS DSP solution.

For calculation-intensive algorithms, the 2100 features three independent computational units: a 16-bit ALU, a 16 x 16 multiplier with a 40-bit accumulator and a robust barrel shifter. To keep the numbers coming, the 8 MIPS processor has unmatched program sequencing and data address generation capabilities.

The ADSP-2100's architecture allows two operands to be fetched from off-chip in parallel with on-chip computation. With this efficient use of external memory (up to 48K) you'll avoid the I/O bottlenecks typical of other processors.

Extensive ADSP-2100 support streamlines your development schedule. The processor is programmed in a high-level algebraic assembly language. Development tools include extensive software support and a full-speed emulator.

Whether your application is modems, speech, imaging, graphics, radar, sonar, or control, the ADSP-2100 gives you outstanding performance, while speeding your project to completion.

For more details, call your nearest Analog Devices, Inc. Sales Office.

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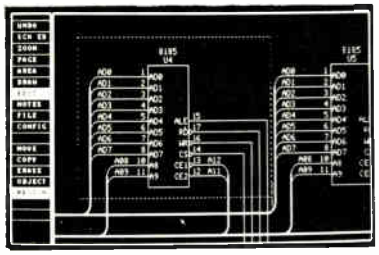

SCHEMA is a complete, integrated schematic drawing software package for IBM Personal Computers. Use SCHEMA with your PC to draw schematics and automatically generate design documentation such as Wire and Net Lists, Bills of Materials, Design Rule Checks, etc. SCHEMA is $495 and supports most common PC hardware configurations. Call or write today for a free demo disk and brochure.

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Inventions, ideas, new products wanted! Industry presentation / national exposition. Call 1-800-528-6050. Canada, 1-800-528-6060. X831.

IBM Personal Computer and the PC/XT and for the PC AT. It features a 256-K bit-mapped graphics buffer and a loadable RAM-based character generator.

The EGAds card supports a 640-by-350-pixel resolution in monochrome mode. In color mode, resolutions are 320 by 200 and 640 by 200 pixels, both supporting 16 displayable colors. It can also support 640-by-350-pixel color. The card handles smooth panning and scrolling and split-screen displays, and it has multiple modes for writing to display memory. It is available now.

PC's Limited, 1611 Headway Circle, Building 3, Austin, Texas 98754.
Phone (512) 339-6800 [Circle 353]

$195 CARD ADDS GRAPHICS TO APPLE II

An inexpensive card adds monochrome graphics capabilities to the Apple II and IIe computers. The Grafex card supports a display resolution of 640 by 400 pixels and draws at 500,000 pixels/s.

The basic card comes with 32-K bytes of memory. If the memory is increased to 128-K bytes, screen resolution increases to 640 by 1,600 pixels.

To aid in software development, the company provides Dimensions, an assembly-language driver that can be called from Applesoft and provides plotting, character generation with multiple fonts, and screen dumps.

The Grafex card sells for $195, and the Dimensions software is an additional $45. Both are available now.

Ray Dahlby Electronics, Department 225, Box C 34069, Seattle, Wash. 98124
[Circle 354]

COLOR PRINTER MAKES COPIES IN 2.5 MINUTES

The model 4696 color ink-jet printer, a desktop personal printer, turns out graphics hard copies on paper or transparency media in 2.5 min. When combined with the 4510A color graphics rasterizer, the result is a system that features 120-dots/in. resolution, a palette of 130,000 colors, and image-queueing and multiple-copy capabilities.

The system is host-based. As a shared plotting resource for ASCII-based computers, the combination of printer and rasterizer is priced at $6,995. A system for use with an IBM Corp. EBCDIC-based 3270 host costs $8,995.

The printer alone, including start-up supplies and interface cable, costs $1,795. The 4696 will be sold as a companion printer to the maker's line of display terminals and color-graphics work stations.

Tektronix Inc., P. O. Box 1700, Beaverton, Ore. 97075.
Phone (503) 644-0161 [Circle 346]

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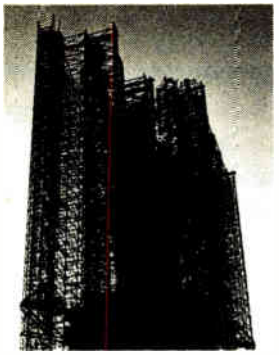

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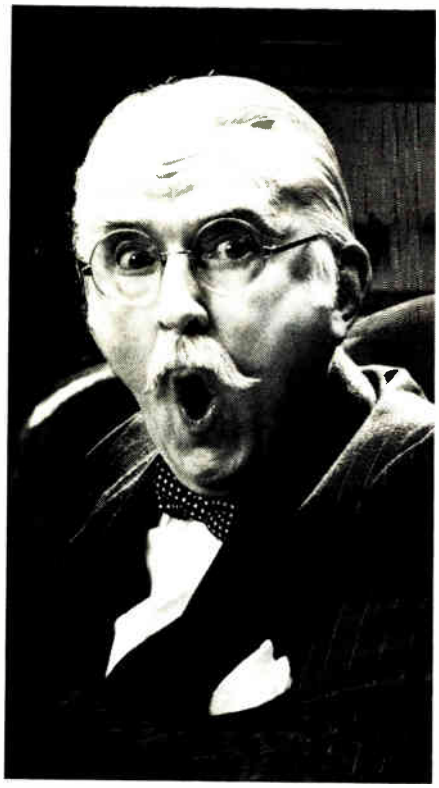
Did You Know That Last Year's U.S. Savings Bonds Average Rate Exceeded 9%?



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MEETINGS

IFIP Congress '86, International Federation for Information Processing (Philip H. Dorn, Dorn Computer Consultants Inc., 25 E. 86th St., New York, N.Y. 10028), Trinity College, Dublin, Sept. 1-5.

Comdex/Australia, The Interface Group Inc. (300 First Ave., Needham, Mass. 02194), RAS Showground, Sydney, Australia, Sept. 2-4.

International Test Conference 1986, IEEE Computer Society (P. O. Box 264, Mt. Freedom, N.J. 07970), Sheraton Washington, Washington, Sept. 8-12.

Midcon '86, IEEE *et al.* (Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045), Dallas Convention Center, Dallas, Sept. 9-11.

Satellite Communications Users Conference, Satellite Communications (Kathy Kriner, 6530 S. Yosemite St., Englewood, Colo. 80111), Bally's Grand, Las Vegas, Sept. 9-11.

European Simulation Congress, Society for Computer Simulation (Ghislain C. Vansteenkiste, University of Ghent, Coupure Links 653, B-9000 Ghent, Belgium), Antwerp, Belgium, Sept. 9-12.

Electronic Materials Management Conference, Electronic Materials Report (111 Main St., Los Altos, Calif. 94022), Hyatt, Palo Alto, Sept. 10-12.

1986 Bipolar Circuits and Technology Meeting, IEEE (John Shier, VTC Inc., 2800 E. Old Shakopee Rd., Bloomington, Minn. 55420), Hyatt Regency Hotel, Minneapolis, Sept. 11-12.

Intelevent '86, E. F. Hutton & Co. *et al.* (Marianne Berrigan, Executive Director, 1120 Connecticut Ave. N.W., Suite 1144, Washington, D.C. 20036), Hotel Bayerischer Hof, Munich, West Germany, Sept. 14-17.

Fiber LASE '86, Society of Photo-Optical Instrumentation Engineers (P. O. Box 10, Bellingham, Wash. 98227), Hyatt Regency, Cambridge, Mass., Sept. 14-26.

Intercomm '86: International Communications Exposition and Conference for Science & Technology, Cahners Exposition Group (P. O. Box 70007, Washington, D.C. 20088), Exposition Center, Beijing, China, Sept. 15-20.

1986 IEEE International Electronic Manufacturing Technology Symposium, Components, Hybrids, & Manufacturing Technology Society of the IEEE (IEEE Council Office, 701 Welch Rd., Suite 2205, Palo Alto, Calif. 94304), San Francisco Hilton & Tower, San Francisco, Sept. 15-17.

International Videotex Industry Exposition and Conference, Videotex Industry Association (1901 N. Fort Myer Dr., Suite 200, Rosslyn, Va. 22209), Marriott Marquis Hotel, New York, Sept. 15-17.

Independent Power Generation Conference and Exhibition, Fuel and Metallurgical Journals Ltd. (2 Queensway, Redhill, Surrey RH1 1QS, England), Excelsior Hotel, London, Sept. 16-17.

IEEE International Symposium on Electromagnetic Compatibility, IEEE (George Ufen, GRU Associates, 1105 E. Commonwealth Ave., Fullerton, Calif. 92631), Town and Country Hotel, San Diego, Sept. 16-18.

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IECON '86, International Industrial Electronics Conference, IEEE (Dr. Richard C. Born, Rexnord Inc., 5101 W. Beloit Rd., Milwaukee, Wis. 53214), Hyatt Regency Hotel, Milwaukee, Sept. 28-Oct. 3.

1986 Applied Superconductivity Conference, IEEE (Ms. Lahni N. Blohm, Executive Administrator, ASC86, Code 6630C, Naval Research Laboratory, Washington, D.C. 20375), Hyatt Regency On the Harbor, Baltimore, Sept. 28-Oct. 3.

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ELECTRONICS WEEK

EUROPE'S APPETITE FOR CHIPS GROWS

Western Europe's chip market will grow by 18% a year for the next decade—faster than that of any other region, according to Dataquest UK Ltd. Between 1975 and 1985, the Western European semiconductor market nearly tripled—from $1.6 billion to about $4.6 billion—and it now accounts for about 17% of the global chip market. Looking into the next decade, Dataquest expects the market to hit the $25 billion mark by 1996.

SIEMENS, GTE START JOINT VENTURE

Siemens AG and GTE Corp. have finally agreed to set up a telecommunications-equipment joint venture after nearly a year of negotiations [*Electronics*, Jan. 27, 1986, p. 80]. Munich-based Siemens will own an 80% stake in the still-unnamed venture, which will probably be headquartered in the U.S. The new company will market GTE's transmission systems internationally and will sell both parents' switching equipment—EWSDs from Siemens and GTD-5s from its Stamford, Conn., partner—to markets outside the U.S. In the U.S., Siemens and GTE will continue to sell their switching gear independently.

DEC EARNINGS JUMP BY 38%

While giant IBM Corp. is mired in the general economic slowdown, the nation's second-largest computer maker, Digital Equipment Corp., is rushing along without any signs of difficulty. Profits for the Maynard, Mass., company jumped 38% to $617 million for the year ended June 28, as revenues rose 14% to nearly $7.6 billion. Fourth-quarter profits leaped 138% to $238 million and revenues rose 17%. DEC's networking ability and revamped product line are at the heart of the strong showing, analysts say. DEC is expected to continue to roll out new products at its present fast pace, with new low-end computers slated for introduction later this year.

U.S. ELECTRONICS JOBS HOLD STEADY

Employment in the U.S. electronics industry held steady through the first quarter of 1986, according to the American Electronics Association. But employment is still down 1.6% from first-quarter 1985 levels. The software, programming, and components businesses accounted for about half of the industry's 12,000 new jobs, but those gains were offset by an equal number of layoffs by semiconductor and computer makers.

MESSERSCHMITT SIGNS ASIC DEAL

The leading aerospace company in West Germany, Messerschmitt-Bölkow-Blohm GmbH, is getting its toes wet in application-specific integrated circuits. MBB is set to announce a three-year, $5 million deal with two San Jose, Calif., ASIC houses—International Microelectronic Products and the Micro Linear Corp. The former makes bipolar linear devices and the latter digital CMOS chips. The deal is the first sizable venture into ASICs for MBB, the largest European NATO contractor.

DRI PICKS OBUCH TO RUN OPERATIONS

Digital Research, Inc., an ailing Monterey, Calif., developer of microcomputer software, is shuffling its executives in an attempt to strengthen its operations. Robert Obuch, a Multimate International executive who left when that company was bought by Ashton-Tate last year, joins DRI as chief operating officer, and senior vice president John Hiles is switching his responsibilities from engineering to business development. The moves free president John Rowley for a strategic role after a hands-on stint as his own director of marketing.

ITALTEL MAY MERGE WITH TELETTRA

Merger mania continues to flutter throughout the European telecommunications industry. Italy's once-troubled equipment supplier, Italtel SpA, is pursuing a joint venture to further increase its domestic sales potential. The company is exploring a partial or total merger with Milan neighbor Telettra SpA to strengthen itself in the competitive and overcrowded telecommunications market.

APPLE'S YOCUM GETS NO. 2 SPOT

For the first time since founder and former chairman Steven Jobs left Apple Computer Corp., the company has a computer veteran running its operations. President John Sculley, a marketing whiz with background in the soft drink business, promoted Del Yocum to chief operating officer, a new post. Yocum had been general manager of the Cupertino, Calif., company's Apple II group.

DATA GENERAL RAISES PRICES

Data General Corp. is boosting prices on about 40% of its product line. The Westboro, Mass., company has increased by 6% the cost of products announced before February 1986—including the top-selling MV/10,000 superminicomputer. Data General says the hikes "will bring profit margins on older products in line with margins on newer products." George Colony, an analyst at Forrester Research, Cambridge, Mass., says the move is aimed at steering customers to the company's newer products, which are not selling as well as expected.

TANDY LOWERS ANTE FOR PCS

Tandy Corp. last week fired a twin salvo in the personal computer war. A scant three months after IBM Corp. cut its wholesale prices by as much as 18%, the Fort Worth, Texas, consumer electronics giant has introduced five new models—all of them cheaper than competing IBM products—and says it will pursue the office market with a new 1,500-member sales force. So far, Tandy has sold its machines only through its nationwide chain of Radio Shack stores.

IBM DELIVERS FIRST VHSIC CHIPS

IBM Corp. is delivering the first packaged test chips built under Phase II of the Defense Department's Very High Speed Integrated Circuits program. Using 0.5-μm geometries, the chips contain memory and a multiplier, and will be used at the U.S. Army Lab Command, Fort Monmouth, N.J., to evaluate the new technology. They are housed in 40-pin DIPs.

TI HAS FIRST PROFIT SINCE '85

Texas Instruments Inc. declared its first profitable quarter since the first quarter of 1985. TI earned $12.3 million on sales of $1.2 billion in the second quarter ended June 30, ending the longest financial drought in its history. Last year, TI reported a $3.9 million loss on nearly identical revenue. Company president Jerry R. Junkins says TI's semiconductor business is nearing the break-even point and its computer equipment group has turned around to register a profit. Now TI plans to lift an eight-month-old wage freeze.

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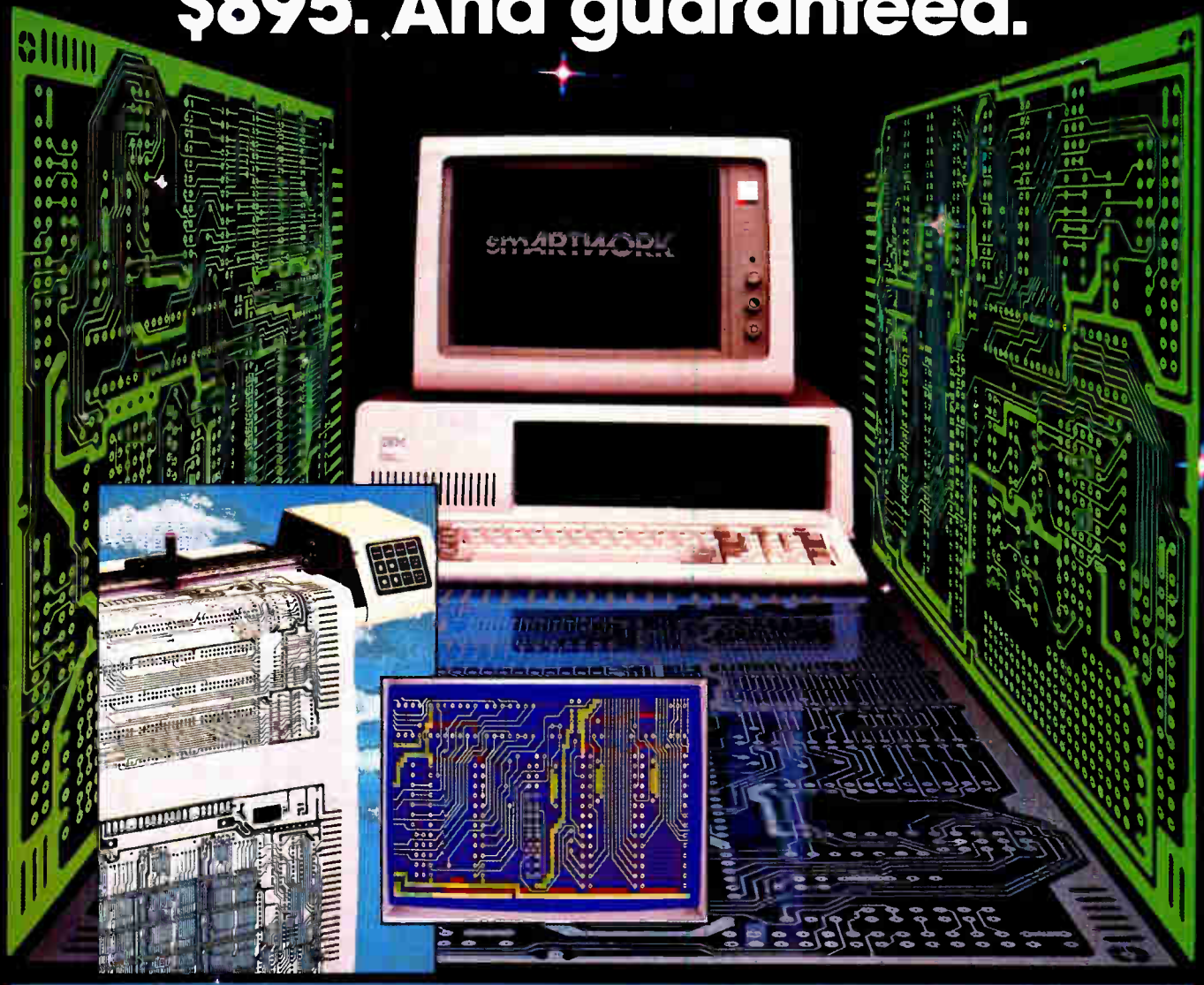

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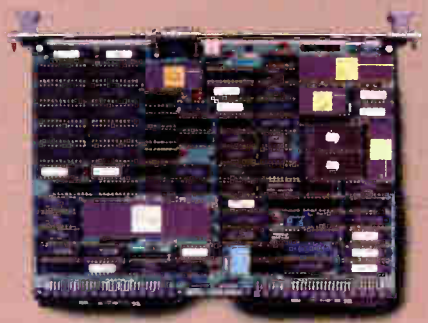

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