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THREE DOLLARS

Electronics

THE WORLDWIDE TECHNOLOGY WEEKLY

MAY 5, 1986

RISC: IS IT A GOOD IDEA OR JUST ANOTHER HYPE?

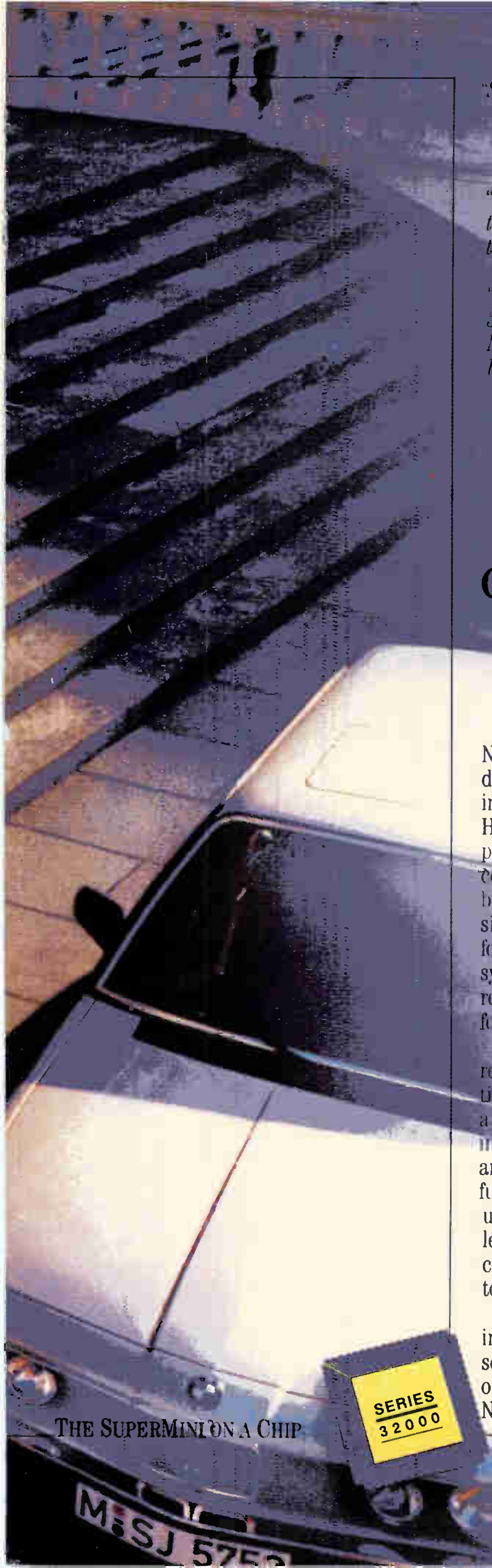
DESPITE THE FLAP, IT'S BEGINNING TO CHANGE COMPUTER DESIGN

PAGE 28

HOW IBM DESIGNED ITS RISC-TECHNOLOGY PC/34

A NEW TOOL LAYS OUT COMPLEX ASIC DESIGNS FAST/37


SIEMENS



"Success! Another order."

"Systems with our kind of power and upgrade potential are difficult to resist."

"Certainly, we've covered all their needs today, and well into the future."

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Type No.	LM64014W	LM64016W
Dot pitch ratio	1:1.4	1:2
Type	Reflective Type	Reflective Type
Contrast	7.0(TYP.)	7.0(TYP.)
Viewing angle	−10~+45°(Co≥2,TYP.)	−10~+45°(Co≥2,TYP.)
Unit outline dimensions W×H×D(mm)	256×128×13.3	256×164×13.3
Display format(W×H)	640×200	640×200

* Compared with earlier Sharp models.

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LM64016W

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Circle 2 on reader service card

MAY 5, 1986 VOLUME 59, NO. 18

Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

COVER

NEW PRODUCTS

DEPARTMENTS

THE ONLY QUICK–TURN GUARANTEE.

Feature Size: 2μ CMOS

	N-Channel	P-Channel
VTEO	0.5–1.0$_V$	0.5–1.0$_V$
BVDSS	>10$_V$	>10$_V$
$K^1 = \frac{\mu c}{2}$ linear region	21–25	6.5—8.5
B_E(Long Channel)	0.8–1.2$_V^{1/2}$	0.4—0.6$_V^{1/2}$
Cap. Gate 10^4 PF/cm^2	8–10	8–10
Cap. Poly to Sub 10^4 PF/cm^2	0.55–0.65	0.55–0.65
Cap. Metal to Sub 10^4 PF/cm^2	0.27–0.32	0.27–0.32
Junction Depth	0.4μ–0.6μ	0.2μ–0.4μ
P-Well Junction	2.5μ–3.5μ	
Poly P_S	15–30Ω/□	15–30Ω/□
Diffusion P_S	20–40Ω/□	60–100Ω/□
VTF Poly	>10$_V$	>10$_V$
ΔW	—1.0μ	—1.2μ
LEFF	1.0μ–1.4μ	1.3μ–1.7μ
Substrate Resistivity	2.5KΩ/□	1.2Ω/cm

Feature Size: 3μ CMOS

	N-Channel	P-Channel
VTEO	0.5-1.0$_V$	0.5–1.0$_V$
BVDSS	>10$_V$	>10$_V$
$K^1 = \frac{\mu c}{2}$ linear region	18–21	6–8
B_E(Long Channel)	0.8–1.4$_V^{1/2}$	0.4—0.6$_V^{1/2}$
Cap. Gate 10^4 PF/cm^2	5.9–7.0	5.9– 7.0
Cap. Poly to Sub 10^4 PF/cm^2	0.45–0.55	0.45–0.55
Cap. Metal to Sub 10^4 PF/cm^2	0.2–0.25	0.2–0.25
Junction Depth	0.6μ–1.0μ	0.4μ–0.8μ
P-Well Junction	3.5μ–4.5μ	
Poly P_S	15–30Ω/□	15–30Ω/□
Diffusion P_S	10–30Ω/□	30–70Ω/□
VTF Poly	>10$_V$	>10$_V$
ΔW	—1.0μ	—1.0μ
LEFF	1.4μ–2.0μ	1.8μ–2.4μ
Substrate Resistivity	2.5K Ω/□	1.0–1.5Ω/cm

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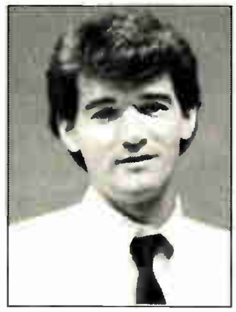
What others promise, we STILL guarantee.

Washington correspondent" brings to mind a reporter dashing through federal agencies and chasing down stories in Washington, D.C. But for George Leopold, our man in the nation's capital, the beat he gets to cover is that and a lot more.

In addition to covering the federal agencies that concern the electronics industry, George's territory takes in all of the Southeast and includes such major industry centers as Research Triangle Park, N. C.; Atlanta; and Florida.

George's contributions to this issue of *Electronics* are particularly apt examples of the breadth of his coverage. A Probing the News starting on p. 44 covers one program of the National Aeronautics and Space Administration—materials manufacturing in space—that is sailing along unscathed even as the space agency itself is getting a black eye. George traveled to Huntsville, Ala., to report on the story on Intergraph Corp. beginning on p. 48. That fast-growing company is challenging IBM for the lead in the computer-aided design and manufacturing market.

"The idea of covering a wide geographical area is one part of my job that is particularly attractive," says George. "As a matter of fact, I feel sorry for the journalists who rarely get out of Washington to cover a story. They are in danger of succumbing to the Beltway syndrome, a malady that causes one's mind to close itself to anything that happens beyond the highway that encircles the city and its adjacent suburbs. I think it's necessary to get a regular breath of the real world to keep from losing perspective. And the federal government beat is really a treat for a reporter, particularly when he works for *Electronics*. That's because, even though they are all part of the federal bureaucracy, the agencies actually offer a great variety of subject matter. I cover the Pentagon, NASA, the Federal Communications Commission, and any other agency that pops up in the news, which they all do from time to time."



LEOPOLD: He heeds the call of the road.

George's experience on the magazine has been varied, even though he has been with *Electronics* just two years—since he received his master's degree from the Columbia University Graduate School of Journalism. Before moving to suburban Maryland with his artist wife, he wrote about new products and covered the New York metropolitan area. And before coming to New York to go to Columbia, the Appleton, Wis., native graduated from the University of Wisconsin.

"I'm a small-town boy at heart—actually, I was brought up in dairy-farm country—and Washington is really a small town at heart," George observes. "New York is an exciting place to live and work, but the pace can be a killer. All in all, I would say that I am pretty fortunate to be living where I am, working the beat I have."

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WEEK 28

Every new IC claims reduced boardspace. But this baby delivers. The Am29C101 is a CMOS 16-Bit Slice, and the newest member of our 2900 family gone CMOS. It is equivalent to four 2901s. Plus one 2902.

The pin count went from 172 to 64. And package count from 5 to 1.

Power's part of the reducing program. You'll need only 0.7W. (Equivalent bipolar parts typically require 5.8W.)

Am29C101

Lose ugly fat. Fast.

How much performance did we have to sacrifice? None. The speed of the Am29C101 is equivalent to 2901C-based systems.

The Am29C101 is software compatible, so the only thing you'll need to modify is your PC board layout.

It's expandable for longer word lengths (16-, 32-, 48-bit systems, etc.). And it's available in 64-pin plastic or ceramic DIP, 68-pin PLCC, or ceramic LCC.

Ask for the Am29C101 and cut the fat out of your next system.

Design and application seminars are available for this product. Write or call for information.

Circle 151 on reader service card

WEEK 29

Announcing the Am29C827/28 high-performance CMOS Bus Buffers, the first members of AMD's hot new Am29C800 series—9 and 10-bit buffers, latches, registers and transceivers in CMOS. They're bipolar fast, CMOS cool.

Am29C827/28

Hot is cool.

Requiring only 80 microAmps of stand-by current, both parts have 8ns propagation delays for truly high-performance systems. With 24mA of drive, they can be used in place of or along with their Am29800 bipolar counterparts to match your drive and power requirements.

Additionally, both devices have MOS/TTL compatible inputs and outputs. (The Am29C828 has inverted outputs, the Am29C827 is non-inverting.) Board space is conserved because both have wide data widths. And their flow-through structure means simpler, more compact interfaces.

If you're looking for bus interface chips that keep their cool under the pressure of high performance, look no further.

Circle 152 on reader service card

WEEK 30

Introducing the Am29C01 4-Bit CMOS Microprocessor Slice. The latest CMOS part of AMD's 2900 family. Advanced Micro Devices created the 2900 phenomenon in the first place. So you can count on the Am29C01 being a product of elegant engineering.

Because the Am29C01 is in CMOS, it uses a mere 25% of the power used by the bipolar version. But it doesn't ask you to give up anything in performance. Anything.

Am29C01

The arrival of the fittest.

And this new breed is the quick, cool, multi-talented, plug-in replacement for our industry standard Am2901. It comes in PLCC and LCC packages. And a military version will soon be available.

The Am29C01, Am29C10 and the Am29C101 are here now. Soon you'll be able to get the Am29C116/117 and the Am29C516/517. All so you can create the next generation of high performance, cooler boards.

So keep up with evolution. Give AMD a call.

Design and application seminars are available for this product. Write or call for information.

Circle 153 on reader service card

WEEK 31

Introducing the Am29331—the fastest 16-Bit Interruptible Microprogram Sequencer anywhere. It's the second member of AMD's remarkably fast, ingeniously-designed Am29300 family.

Am29331

Real time needs unreal speed.

The Am29331 has Real Time Interrupt. By building in Test Generation Logic (which no one else does), we cut down on chips and allow for faster system cycle time. Without having to wait for the additional cycle you usually need to accommodate an interrupt, you get faster throughput.

More reasons why the speed stays white hot: Errors can't get too far in the Am29331. They're detected at the source, not at the memory level. It's transparently interruptible at any microinstruction boundary, and Built-in Trap Handling insures speedy re-execution.

While the Am29331 16-Bit Interruptible Microprogram Sequencer is just one of AMD's 29300 family. Other members of the family are the Am28332 32-Bit ALU and the Am29334 Four Part Dual Access Register File.

You can use the Am29331 with non-family members if you must. Just make sure the microprocessor you choose can keep up with it.

Design and application seminars are available for this product. Write or call for information.

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FOILING THE SYSTEM BREAKERS: COMPUTER SECURITY AND ACCESS CONTROL

Jerome Lobel
McGraw-Hill Book Co.
$34.95/292pp

Anyone who still believes computer-system security is a minor issue will likely change his mind after reading Jerome Lobel's book. Unauthorized access to data banks by insiders as well as outsiders is a major headache to corporations and government agencies, and is exacerbated by the growth in user-friendly software, which is particularly vulnerable to penetration. The book is aimed at system managers, who must determine who should have access, establish a consistent access policy, evaluate the system, choose the right combination of security products, and monitor access security during the system's lifetime.

Types of systems examined include closed and limited-access networks, office-automation systems, network-connected personal computers, and home computers. Lobel, who is manager of computer security for Honeywell Information Systems, pegs successful security systems to the development of strong, consistent guidelines, which in turn will drive security technology.

STRATEGIC DEFENSE INITIATIVE MARKET DIRECTORY

IMA Inc.
$480/200pp

This guide to the SDI market is designed to be used by marketing managers and planners. It contains budget projections for individual research programs, a directory of over 200 SDI managers in the armed forces and government agencies, names of over 300 companies that are already working on SDI contracts, descriptions of about 100 major contracts for SDI-related research, and applicable contracting procedures and policies. IMA Inc., a management consulting firm, issues updates at quarterly intervals. Contact the company at 1800 K St., N. W., Washington, D. C., or phone (202) 296-4615.

REAL-TIME MICROPROCESSOR SYSTEMS

Stephen Savitzky
Van Nostrand Reinhold
$47.50/338pp

Engineers and programmers who are unfamiliar with real-time systems will find this book useful. Savitzky, a staff engineer at Zilog Inc. and designer of the ZRTS operating system, sticks to a goal-oriented approach that should appeal to managers of large projects.

Following a general introduction, Savitzky moves into specifics of design and implementation. He divides these into milestones or events, beginning with the requirements document and ending with production and follow-up maintenance. The book closes with detailed studies of uniprocessing, multitasking, and multiprocessor systems. Finite-state machines are described under "special techniques." Hardware engineers probably will not learn programming from the brief examples, but programmers may come away with increased respect for the constraints imposed on design by the hardware.

AI TRENDS '86

DM Data Inc.
$195/175pp

This is the fourth annual report on artificial intelligence to appear from DM Data, a high-technology consulting company. Since the last report was published, the company says, more than 60 companies have entered the market, many products have been introduced, and investment in AI by Fortune 500 companies has been heavy.

AI Trends '86 contains updates on startups, major investments and contracts, and shifts in the marketplace. Each chapter of the report contains definitions, reviews of the current technology, present and future applications, and information on developers and suppliers. DM Data is located at 6900 E. Camelback Rd., Suite 1000, Scottsdale, Ariz. 85251; phone (602) 945-9620.

ELECTRICAL OVERSTRESS PROTECTION FOR ELECTRONIC DEVICES

Robert J. Antinone *et al.*
Noyes Publications
$48/462pp

This is an extremely detailed investigation, for the specialist engineer, of electrical overstress (EOS) protection for microelectronic devices. The authors evaluate benefits versus performance and cost penalties for submicron and very large-scale-integration devices and review physical mechanisms that cause EOS failure in semiconductors.

Though the studies were prepared for military purposes, they also have commercial applications in equipment reliability. The format—photo-offset reproduction of typescript—keeps the price of such a not-very-accessible collection of documents within reasonable bounds. As a result, however, halftone reproductions in the sections on device characterization and testing have been degraded and the text has been scaled down to borderline readability in all program printouts and some tables.

TECHNOLOGY NEWSLETTER

SUBSTRATE CHANNELS TAKE THE HEAT FROM BIG CHIPS

Researchers at Nippon Telegraph & Telephone Corp.'s Electrical Communications Laboratories in Musashino, Japan, have found an indirect way to cool very large-scale integrated circuits mounted on ceramic substrates that is just as effective as direct immersion cooling and at the same time permits the stacking of boards to achieve dense modules. The researchers improve indirect cooling tenfold by means of microminiature cooling channels in multilayered alumina-cofired substrates. In an experimental package, the lab mounted a five-by-five array of 8-by-8-mm chips on an 85-by-105-mm substrate. The substrate had 29 coolant channels (800 μm wide by 400 μm high), six conductive layers, and 900 input/output pins. An allowable heat dissipation greater than 400 W per package was realized at a flow rate of 1 liter of coolant per minute. NTT researchers will describe the work at this week's Electronic Components Conference in Seattle. ☐

SPEECH SYSTEM RECOGNIZES 67,000 WORDS

Vocabularies of real-time speech-recognition systems could bound as high as 67,000 words by year end—triple the word power currently possible. Speech Recognition Systems Inc., Rochester, N.Y., has in the works an experimental large-vocabulary system based on phoneme recognition. The system organizes acoustic and phonetic information from real-time speech into a string of phonemes, which is then processed by a dictionary, or lexical processor, to match up with 200,000 possible word pronunciations. Company president Robert Houde says the processing algorithm now achieves 90% phoneme accuracy and 99% word-recognition accuracy with the 67,000-word system running about five times slower than real time on a Sun Microsystems Inc. computer. Houde expects real-time processing when custom hardware is completed by the end of the year. Houde described the system last week at Speech Tech '86. ☐

HITACHI BRIGHTENS FUTURE FOR FLAT-PANEL TV SCREENS

Hitachi researchers believe flat-panel color TVs could be only a few years away, now that they have developed an 8-in. prototype using a Townsend effect gas-discharge panel. The prototype generates strong ultraviolet rays in individual pixel cells to excite red, green, and blue phosphors to high brightness at low power consumption. The experimental display has only 6,400 pixels, each composed of three discharge cells—one red, one green, and one blue. But by going to a size of 40 in., the pixel count will provide practical resolution for TV viewing. The panel will be described at this week's International Symposium of the Society for Information Display. ☐

A NONOPTICAL SENSOR FEELS THE SHAPE OF COMPLEX OBJECTS

A small, 11-month-old company in West Berlin says it is on the way to solving a major problem in industrial automation: how to make a nonoptical sensor that, just like a blind person, can feel the shape of complex objects so they can be optimally gripped. The tactile sensor, now in development at Robot GmbH, senses the object's shape and feeds data to a microprocessor. From that data, the processor generates signals for the gripping system of a robot arm. Except to say that the sensor is based on principles worked out at the Institute for Electromechanical Constructions at the Technical University at Darmstadt, the company will not reveal details. A gripping system that will pick up and place small objects weighing up to 100 grams will go to market next year. It should cost less than present camera-based models that rely on the contrast between objects and their surroundings. ☐

ELECTRONICS NEWSLETTER

FORTUNES START TO RISE FOR CHIP SUPPLIERS

Fortunes of U. S. semiconductor suppliers at last are showing some improvement, paced by better-than-expected bookings and sales in the first quarter. Sales for the three-month period showed an upswing for the first time since 1984, growing 5.7% over the final quarter of 1985, reports consultant Jack Beedle of In-Stat Inc., Scottsdale, Ariz. Beedle, who closely tracks the initial "flash" data from the Semiconductor Industry Association, has even better news: new orders, up a whopping 23.9%, should support a 9% sales increase in this quarter. For the entire year, however, Beedle is sticking with his previous 3.5% gain prediction for U. S. semiconductors, somewhat below the consensus of other forecasters who look for an increase of 6% to 10% for the year. Beedle is widely credited with predicting the recent semiconductor recession earlier and more accurately than other seers. □

NEC ATTACKS U. S. MARKET WITH PC AT CLONE

NEC Information Systems Inc. is taking aim at the weaker players in the U. S. personal computer market with its powerful APC IV Advanced Personal Computer. Frank Girard, vice president of systems marketing for the Boxboro, Mass., marketing arm of the Japanese computer giant, says his company is shooting for a $100 million share of the U. S. personal computer business by the end of this year and twice that in 1987. That translates to about an 8% share of this year's $1.25 billion market. The new machine, which is fully compatible with IBM Corp.'s Personal Computer AT, comes with a 5¼-in. floppy-disk drive, a 40-megabyte hard-disk drive, and a high-resolution color monitor and will sell for about $6,100. Girard says NEC is aiming at the high end of the personal computer market because the demand for engineering and other work-station products is booming. "The future of the personal computer is gravitating toward computer-aided design, -manufacturing, and desktop publishing, and no one else has targeted that niche," he says. At Comdex/Spring in Atlanta last week, Girard said, "We've got a sleeping giant here, with the resources to stay in this market—and win in it."□

U. S. AND CHINESE PLANNING COOPERATIVE TRADE EFFORTS

The U. S. electronics industry is giving heavy support to an attempt to open up markets in the People's Republic of China. A delegation of Chinese electronics officials, headed by chief electronics minister Li Tieying, is in Washington this week to try to persuade the departments of defense and commerce to relax their export controls on the technology China needs. As part of a visit sponsored by the American Electronics Association and Stanford University, Tieying told a dinner meeting in Palo Alto last week that Chinese electronics technology is now at the level of the U. S. in the 1970s. China, which imported just $200 million in electronics from the U. S. last year, wants to reach the 1980s level of the U. S. by the end of the five-year plan just begun. The AEA and the Chinese delegation agreed to set up a direct communications link to facilitate trade negotiations, and announced that the joint private-sector meetings would be repeated regularly. The next one will be held in Beijing. In a day-long meeting with some 40 U. S. electronics executives, the Chinese urged U. S. companies to explore Chinese markets, warning that Japanese competition is already on the scene. In return, among other issues, the U. S. executives asked for Chinese compliance with software copyrights. Meanwhile, a delegation of U. S. executives from nine software and four semiconductor companies is in China on a two-week mission led by George T. DeBakey, deputy assistant secretary of commerce for science and electronics. DeBakey led a group of telecommunications officials on a similar trip last December. □

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	DT3382	12-bit A/D, up to 32DI/64SE throughput up to 250kHz, m to n channel scans, and programmable gain	MicroVMSLIB
Digital I/O	DT2751	Two 12-bit D/As designed for waveform generation and point-plotting	MicroVMSLIB
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PRODUCTS NEWSLETTER

NCR ADDS EEPROM TO ITS LIBRARY

Nonvolatile memory can be designed into application-specific ICs now that NCR Corp.'s Microelectronics Division has added an EEPROM supercell to its standard-cell library. Designers need only select a density, which can range from 32 to 256 bits, and a word width in 1-bit increments to add the EEPROM to chip designs. Programming voltage for the Dayton, Ohio, company's supercell is 15 V, versus 21 V for other EEPROMs. Sierra Semiconductor Corp. was the first to add EEPROM to its library [*Electronics,* March 10, 1986, p. 14], which allows users to create reprogrammable ASICs. □

HITACHI IS ABOUT TO TAKE THE LEAD IN PSEUDOSTATIC-RAM RACE

Hitachi Ltd. is about to offer a 1-Mb pseudostatic RAM, a move that will give it the capacity lead for this type of part. But the competition is close on its heels. Both NEC Corp., which already has a 256-K model, and Toshiba Corp., which calls its version virtually static RAM, have 1-Mb parts in development. Samples of Hitachi's 1-Mb HM658128P will be available in July for $82; Toshiba promises to start delivery of its part next spring. A pseudostatic RAM has the same memory-cell structure as a dynamic RAM but can be used like a static RAM. This gives equipment designers the advantages of SRAM's ease of use combined with DRAM's larger capacity and lower cost per bit. Hitachi's pseudostatic RAM is organized as 128-K by 8 bits and has a maximum access time of 120 ns. Maximum operating current is 85 mA. The HM658128P is the Tokyo company's second pseudostatic RAM, following the 256-K part introduced last July. □

DICONIX UNVEILS A 4-LB PORTABLE INKJET PRINTER

Eastman Kodak Co.'s Diconix Inc. subsidiary unveiled at Comdex in Atlanta last week a battery-powered inkjet printer small enough to be carried around with laptop and other portable computers. It weighs only 4 lb and measures 2 by 6.5 by 10.8 in. The Diconix 150 connects to a computer's parallel port and will sell for $479 when available in the fall from the Dayton, Ohio, company. It can print up to 150 characters/s in 12 type fonts on either single sheets or continuous-form paper. The printer uses a $9.95 replaceable cartridge that contains both the printhead and a 500-page ink supply. □

FUJITSU'S GaAs MICROWAVE AMPLIFIER HAS LOW NOISE INDEX

Fujitsu Ltd. is shipping samples of a low-noise GaAs microwave signal amplifier that can amplify a 1-μW signal to 10 μW in the K band. The use of high-electron-mobility transistors reduces the noise index to only 1.8 dB. This will greatly improve the signal resolution of radio telescopes. The Tokyo company's FHRO1FH is priced at $890 to $1,190, depending on frequency range. □

TEKNOWLEDGE EXPANDS EXPERT-SYSTEM TOOL LINE

A development toolkit that runs on the IBM Corp. Personal Computer, PC/XT, and PC AT led the list of new products announced by Teknowledge Inc. at last week's AI '86 convention in Long Beach, Calif. The Quick Start package from the Los Altos, Calif., artificial-intelligence software house sells for $7,500. In addition, Teknowledge said that its high-performance S.1 applications delivery software will be shipped late this summer in a PC AT version for $3,000. The company also announced that all its offerings, originally written in Prolog, have been rewritten in C. Teknowledge says this makes the S.1 package, for example, run 50 times faster. □

Electronics

BOOTLEGGING ON SATELLITES TURNS OUT TO BE REAL PROBLEM

'CAPTAIN MIDNIGHT' ONLY MAKES PUBLIC A YEARS-OLD PRACTICE

SANTA CLARA, CALIF.

The satellite pirate who commandeered a Home Box Office transponder late last month to protest the scrambling of pay-TV movies relayed by satellite vividly made public a practice that has been going on in the background for several years. Even Pentagon communications satellites reportedly have been co-opted by unauthorized sources.

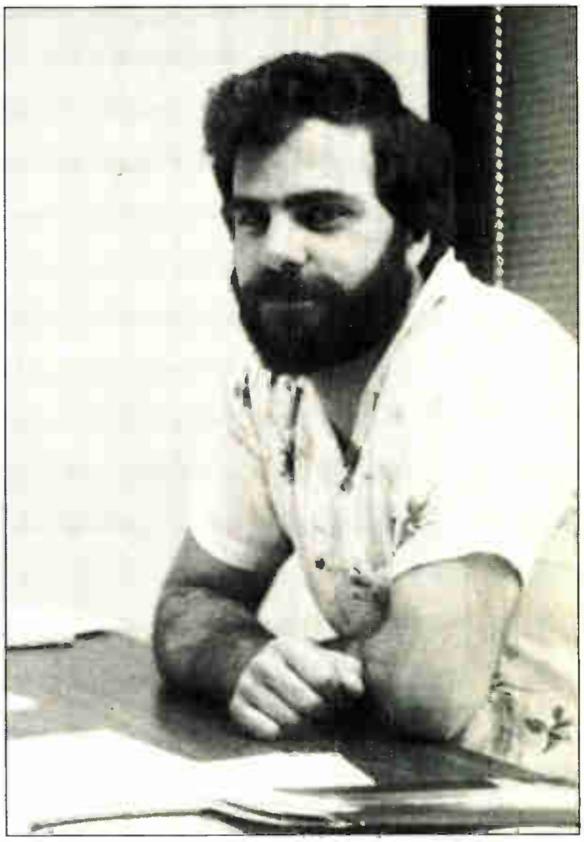
"Captain Midnight," the HBO intruder, deliberately invited the attention of cable viewers by overriding the signal with his protest. Most satellite pirates, however, take pains not to be noticed. They tag along on the skirts of video waveforms and modulate low-power signals at the edges of the 36-MHz transponder bandwidth, which affects the legitimate user's transmission only slightly. C-band video, however, will present an ever more tempting target.

"Lots of people love to scan satellites," says Steve Wozniak, designer of the Apple II computer and a one-time expert on the "blue boxes" that are used to pirate long-distance telephone calls. "Now that the signals are scrambled, they are going to fight back." The HBO episode did not surprise Wozniak, who has made satellite piracy the theme of a film treatment. Bootlegging in the audio spectrum has been going on for five years, he says; shifting to video will be easy, "but very, very risky."

The Defense Communications Agency, which monitors its communications meticulously, has detected a number of spurious signals on the Defense Satellite Communications System's satellites 2 and 3, says an official at a company that makes signal-analysis gear.

The DCA reportedly has found some unexpected carriers at nominally low-power bandwidths, either encrypted or modulated in a nonstandard way, on the satellites that carry most of the Defense Department's long-haul communications. A satellite specialist at the DCA refused to confirm or deny this.

But commercial users commonly check only their own signals and may not even be aware of the extra activity, says Timothy M. Shroyer, director of communications and information systems at Stanford Telecommunications Inc., Santa Clara. It makes monitoring gear—waveform analyzers and digital signal processors—that the DCA uses to tune its satellites for efficient operation and to check for jamming.



FIND THEM. The only good response to satellite piracy is to find the pirates, says Stanford Telecommunications' Shroyer.

Until now, commercial users have balked at the $200,000 to $300,000 price of monitoring equipment, Shroyer says—though his company does have one commercial customer for its analyzers, GTE Spacenet. But satellite pirates are hard both to elude and to find, and Shroyer thinks the Captain Midnight episode may give commercial satellite operators second thoughts. "We believe there are lots of people up there," he says. "They just haven't been malicious, to date."

A company representative of the Hughes Aircraft Space and Communications Group, operator of the Galaxy I satellite that Captain Midnight jammed, says Hughes does analyze Galaxy signals continuously, though he won't say how.

WOR-TV of Secaucus, N. J., reported to the Federal Communications Commission last October that its signals had been interfered with for three days. Charles Magin, satellite specialist at the FCC's Field Operations Bureau, Laurel, Md., says the source of the interference was an unmodulated carrier on a frequency common to two transponders. Magin says the investigation found no indication that it was intentional, and the interference probably was caused by "sloppy operation."

Nevertheless, Magin acknowledges that interference with satellite communications is becoming a widespread problem. Following the WOR investigation, he says, the FCC published a general notice emphasizing that the penalty for interference with satellite TV signals can include a $10,000 fine and a one-year prison sentence.

Sarah Lawrence of the FCC's Office of Congressional and Public Affairs in Washington says an investigation of the Captain Midnight incident is under way and the matter has also been referred to the Federal Bureau of Investigation and the Justice Department. "We view it as very serious," she says.

The Defense Department can protect itself against jamming with on-board signal processing that keeps changing the receive frequencies, as Lockheed Corp. does with its Milstar satellite, or by requiring an identifier on the uplink signal, says Shroyer of Stanford Telecommunications. These are expensive solutions. Desensitizing the receiver in the satellite is another possible defense, but a pirate would need only more transmission power to overcome it and transmit his own signal.

For commercial users, though, "there aren't any real solutions, except to find the pirates," Shroyer says.

His company is working on a system that will do that by analyzing the phase shift in uplink signals. Communications satellites traverse a small figure-eight path in their geostationary orbits, and when the phase shift of a transponder signal is compared with a calculated satellite ephemeris, the ground source can be located to within the range of line-of-sight tracking equipment. The company expects to offer the tracking system within six to nine months.

Satellite Business Systems Inc. of McLean, Va., for one, thinks it has less of a problem because it transmits digital data in the K_u band, which it considers a more difficult target for pirates than the Galaxy satellites' C-band video. For SBS, spurious signals show up as bit errors, and the company says that so far it has been able to attribute them to operational errors. *–Clifford Barney*

MAGNETIC MEDIA

IBM LIGHTS A FIRE UNDER THE 3½-IN. DISK

ATLANTA

Makers of 3½-in. floppy disks are a whole lot happier these days; they figure the smaller, semirigid cousin to the dominant 5¼-in. floppy disk is bound to become the next product standard. Retail prices should firm and sales should boom, they say, now that IBM Corp. has put its stamp of approval on the smaller drive by installing it in its Personal Computer Convertible. The good news can't come too fast for the beleaguered magnetic-media makers, who have watched disk prices tumble recently as more and more competitors flocked to the emerging market.

Media makers say the Convertible is just IBM's opening salvo. By fitting the new portable with 3½-in. disk drives, IBM is committing itself to making a wide body of software available on the smaller disks. And industry observers agree that Big Blue wouldn't be taking on such a task if it planned to limit 3½-in. disk drives to its portable machines. The dominant sentiment among media makers at the Comdex/Spring show in Atlanta last week was that IBM must be preparing to make broader use of 3½-in. technology—and soon.

Maxell Corp. of America, one of the leading suppliers of 3½-in. floppy disks and a subsidiary of Tokyo's Hitachi Ltd., says tumbling prices have shaved its profit margins to the bone, prompting the company to try renegotiating its long-term manufacturing and materials-supply agreements. Maxell's wholesale price for a single-sided high-density 3½-in. disk with a half megabyte of unformatted capacity has dropped from about $2.60 a year ago to about $1.50 today. Other makers have been hit harder by the crunch because of yield problems in production, which have forced them to seek out competing suppliers to help them meet production needs.

BLUE BLESSING. Welland sees IBM's use of 3½-in. disks as a major endorsement.

"This is an endorsement of tremendous magnitude," says Mark Welland, national sales manager for computer products at Maxell. "It's one thing for a niche machine like Apple's Macintosh to use the format, but it's another for IBM to use it."

Others agree. They point to the kinds of machines that are taking advantage of the format, which uses smaller drives and offers higher storage density than its 5¼-in. cousin. The Macintosh, the Commodore Amiga, and now the Convertible are all leading-edge machines, says David Sewall, development manager for commercial markets at 3M Co.'s Magnetic Media Division, St. Paul, Minn. "Although the Convertible market is small, people will now be looking for 3½-in. capability in other machines."

Sewall believes that within the next 12 months IBM will unveil a new version of the popular PC AT that will have one 5¼-in. drive and one 3½-in. drive. Though such a machine did not appear at this show, IBM representatives said a PC/XT with just such a drive configuration was displayed last fall at the Comdex show in Las Vegas.

NEW PC STANDARD. Others speculate that by the end of the summer, IBM will finally release the long-awaited second coming of the standard PC—a reconfigured, modernized machine that could feature at least one 3½-in. disk drive. IBM is said to be waiting for the availability of sufficiently reliable drives for the 2-megabyte 3½-in. disks that are starting to show up on the market.

Maxell and Sony Corp., the market leaders, now offer 2-megabyte disks in production quantities, as does Verbatim, a division of Eastman Kodak Co. Others, such as 3M and TDK Electronics Corp., say they plan to offer the higher-density products soon. But availability of drives for the denser media is still limited, and as yet no manufacturer has incorporated a 2-megabyte 3½-in. floppy-disk drive into a computer product.

3M's Sewall points out that "the market is hardware-driven," and maintains that drives are not yet available. But Michael Korizno, national sales manager for floppy disks at Sony's Magnetic Products Co., Park Ridge, N.J., says Sony has offered a drive for more than a year, and Welland of Maxell says Hitachi, Mitsubishi, and Toshiba are also making drives. One well-founded rumor floating about the Comdex show floor had IBM already placing a major production order for the 2-megabyte media for short-term delivery. *–Tobias Naegele*

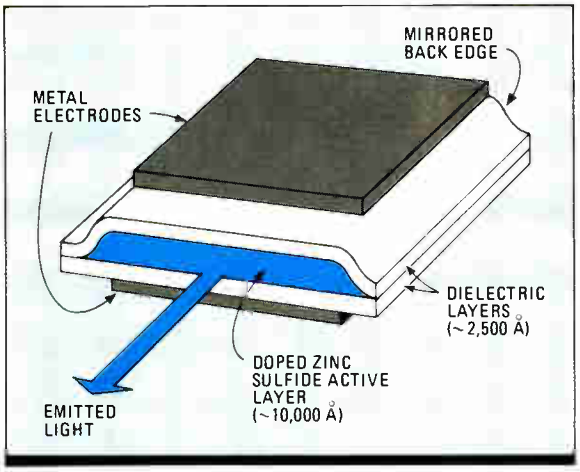
PRINTERS

EDGE-EMITTING EL DEVICES COULD CUT PRINTER COST

PITTSBURGH

By turning an electroluminescent thin film on its side and taking the light from the edge instead of from the face of the film, Westinghouse Electric Corp. hopes to light the way to a new low-cost nonimpact printer technology.

Westinghouse researchers have demonstrated that with a manganese-doped zinc sulfide thin film of the kind typically used in EL flat-panel displays, light from the edge of the film can be 100 times brighter than that from the face. Westinghouse plans to use the technique to develop printer image bars for use in electrophotographic printing sys-



BRIGHTER. Westinghouse gets 100 times more light from the edge of an EL element than can be had from its top.

tems, but they are at least two years away from commercial introduction.

In such systems, a light source is directed onto a charged photoconductive drum to selectively discharge areas on the drum, preventing adherence of oppositely charged inks or toners used for the printing. Westinghouse says image bars based on thin-film devices could replace today's mirror-scanned laser light sources, which are relatively expensive, bulky, and fragile. The technique will also compete with image bars based on light-emitting diodes.

Westinghouse has been working on the image-bar application for about two years and received a patent for the idea last August. Project leader Zoltan Kun, coinventor of the thin-film technique, will make the first technical disclosure of the method at a session on electrophotographic printing at this week's International Symposium on Information Display in San Diego.

'STEP FORWARD.' The Westinghouse development is "a step forward in technology," says Thomas J. Werner, operations manager at 3M Co.'s Software and Electronics Resource Center in St. Paul, Minn., who will chair the session on electrophotographic printing. But he cautions, "the printing head is just one facet of the entire system." Werner points out that cost savings or other benefits from a new image-bar technology must be weighed against total system considerations.

But Kun believes the technology will have a significant impact on the systems. His team at the Westinghouse Research and Development Center in Pittsburgh has built experimental 3½-in.-long linear arrays of edge-emitter devices that have achieved a resolution of 20 lines/in.

Fabrication of the array starts with a quartz substrate. Using electron-beam evaporation, a common electrode composed of palladium is put down on the substrate. An yttrium oxide dielectric is deposited on the palladium electrode, followed by the ZnS thin film and another dielectric layer. An aluminum electrode on top completes the sandwich.

When these arrays are excited with 5-kHz square or sine waves at 150 to 260 V, one edge emits a broadband yellow-orange light with a wavelength that peaks in the visible range at around 580 nm. Westinghouse has measured brightness levels of 500 mW/cm² using devices that rely on ZnS thin films that are 1.2 μm thick, Kun says. That compares with about 5 mW/cm² for flat-panel EL displays based on conventional face-emitting thin-film devices.

IN DEEP. The high light output per unit is "mainly due to the fact that the light comes from much deeper in the device," Kun explains. Though the emitting edges of the Westinghouse devices are only 1 to 1.5 μm—about 10,000 Å—thick and 0.75 mm wide, the devices are about 3 mm deep. "Luminescence is a volume phenomenon," Kun explains. The Westinghouse device not only generates light, but also acts as its own waveguide.

Brightness levels of 500 mW/cm² have been seen

Kun's team has shown that the quality of the dielectric layers and the thickness and quality of the ZnS thin film are critical to the edge-emitting devices' performance. The dielectric layers act as current limiters in the device, and thus must be uniform and free of pinhole defects. Because the dielectric layers have a smaller refractive index than the ZnS, they reflect photons in the active ZnS layer, exciting a number of propagation modes in the film.

The film's thickness is critical because the number of modes propagated is governed by the thickness of the ZnS layer. A thicker film can support more propagation modes, allowing higher light radiation. But more modes also means more angular dispersion of the light at the emitting edge. Kun's team is working to find the ZnS layer thickness at which the optimum amount of edge-emitted light is concentrated in a forward direction. This could help cut costs and alleviate problems by eliminating the need for concentrating lenses in an edge-emitting-array assembly, he says.

The amount of light output also depends on attenuation factors within the ZnS layer, Kun notes. Work has shown that thin-film lossiness is related to the quality and crystal structure of the thin film, which in turn is a function of the heat-treatment techniques used during fabrication, he says.

By fine-tuning the fabrication methods, Kun believes he can increase the intrinsic output of the edge-emitting devices even more. And he points out that devices to date have been built without an antireflective coating on the emitting edge. Such a coating, he says, would increase the device's output by 2.4 times. Kun expects to have devices equipped with an antireflective coating by the second half of the year. And within about a year, he hopes to demonstrate linear arrays up to 9 in. long with the 400 lines/in. resolution needed for high-quality printing; 12-in.-long arrays with 200- to 300-lines/in. resolution are also planned. *–Wesley R. Iversen*

COMPUTERS

A 1-BIPS SYSTEM TAKES NEW TACK IN PARALLELISM

CAMBRIDGE, MASS.

Mips worshipers have a new god. Thinking Machines Corp.'s Connection Machine, a massively parallel computer that made its commercial debut last week, goes beyond millions of instructions per second and ushers in the era of bips with its ability to execute 1 billion instructions/s.

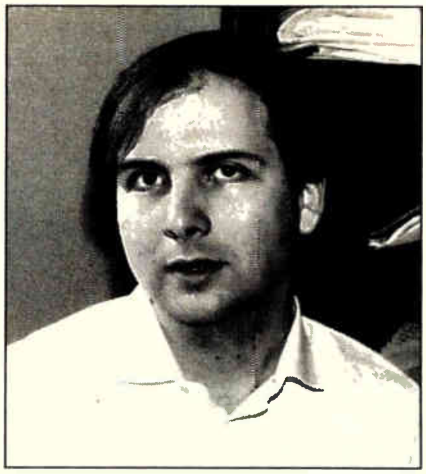
Other numbers describing the Cambridge company's machine are likewise grand in scale. In its largest configuration, the computer has 65,536 processors and 32 megabytes of memory. Processors can communicate with each other at 3,000 Mb/s and the computer's input/output channel can handle 500 Mb/s. The air-cooled computer, housed in a cluster of eight translucent black cubes clustered one on one in four stacks with dozens of blinking red lights, needs a hefty front-end machine, either a Digital Equipment Corp. VAX or Symbolics Inc. computer.

More important than the raw numbers, however, is that the computer takes a new approach to parallelism. The Connection Machine uses data-level parallelism by reducing tasks to data elements and assigning a single processor to each element, says W. Daniel Hillis, founding scientist at Thinking Machines. This makes it particularly useful for applications involving huge amounts of data, as opposed to heavy computing on a few data elements.

As an example, Hillis describes an attempt to determine which of 50,000 news articles relates to a particular clipping. In the Connection Machine, he explains, each article would be assigned to and examined by a single processor. The processors would then compare their data elements with the reference clipping stored in the front-end computer.

ALL AT ONCE. "The most rational way to execute a lot of operations is to work all the data at once," says Hillis. This fine-grain parallel-computing method also avoids the primary bugaboo of so-called coarse-grain processors (those with fewer, larger elements), which require subdivision of the application problem, he adds. "We don't partition, and that avoids a big set of problems."

The Connection Machine's cornerstone is a custom chip that holds 16 processors and 4-K of memory. If an application takes only some processors, the system temporarily switches off unused chips. If there are more data elements than processors, the computer's hardware operates in virtual-processor mode by subdividing memory and simulating additional multiple processors, each with a smaller memory. The Connection Machine can support up to a million virtual processors. The machine's breakthrough concept was eliminating the separation of processors and memory and instead mixing them together along with high-speed communication elements, says president Sheryl Handler.



HILLIS. The Connection Machine devotes a processor to each data element in a problem.

The Connection Machine runs under conventional operating systems, including AT&T Co.'s Unix, DEC's VMS, and Symbolics's Lisp environment. Its languages are extended versions of Lisp and C. Throughout development, says Handler, the development team concentrated on applications. At the large conference announcing availability of the machine, demonstration areas included document processing, contour mapping, chip design, and fluid dynamics.

The company also announced that several machines had already been sold, in addition to one delivered last fall to the Defense Advanced Research Projects Agency, which partly funded development of the computer and has placed an order for another machine. Other early customers are Perkin-Elmer Corp., the Massachusetts Institute of Technology, and Yale University.

Perkin-Elmer's 16,000-processor unit will be used at MRJ Inc., Oakton, Va., to search text, process images, and do research, says Edward McMahon, a member of the Perkin-Elmer division's technical staff. Referring to the difficulty of programming other multiprocessors, McMahon says, "The creativity in using the Connection Machine is in formulating algorithms, rather than the programming part."

Price for the computer with 65,536 processors and 32 megabytes of memory is $3 million. A unit with 16,384 processors and 8 megabytes of memory sells for $1 million. This compares favorably with large mainframes, claims vice president Richard Clayton. He calculates the Connection Machine's cost at $3,000 per mips or less, whereas mainframes cost up to $150,000/mips. To keep costs down, he explains, the company placed a priority on using simple building blocks and conservative manufacturing technology. *–Craig D. Rose*

SUPERCOMPUTING GOES DESKTOP

Culler couples its vector processor to Sun work station

SANTA BARBARA, CALIF.

It was bound to happen: somebody would move supercomputing to the desktop. Just a couple of years ago, a new class of machines called minisupercomputers arrived, moving high-performance 64-bit vector supercomputing out of the realm of giant multimillion-dollar number crunchers in big computer centers and into the size, environment, and cost worlds of the minicomputer.

But now, before minisupercomputers really have had a chance to catch on anywhere, Culler Scientific Systems Corp. has developed a machine that fits neatly beside or under a desk and pulls supercomputing into the office. The Santa Barbara company will pull the wraps off its PSC computer at the National Computer Graphics Association conference next week in Anaheim, Calif.

CLOSE TO CRAY. The minisupercomputers available from several companies now claim to deliver computational performance that's getting close to that of Cray Research Inc.'s Cray-1 supercomputer, but at prices as low as 10% of a Cray. They also present power and space requirements no greater than those of a superminicomputer.

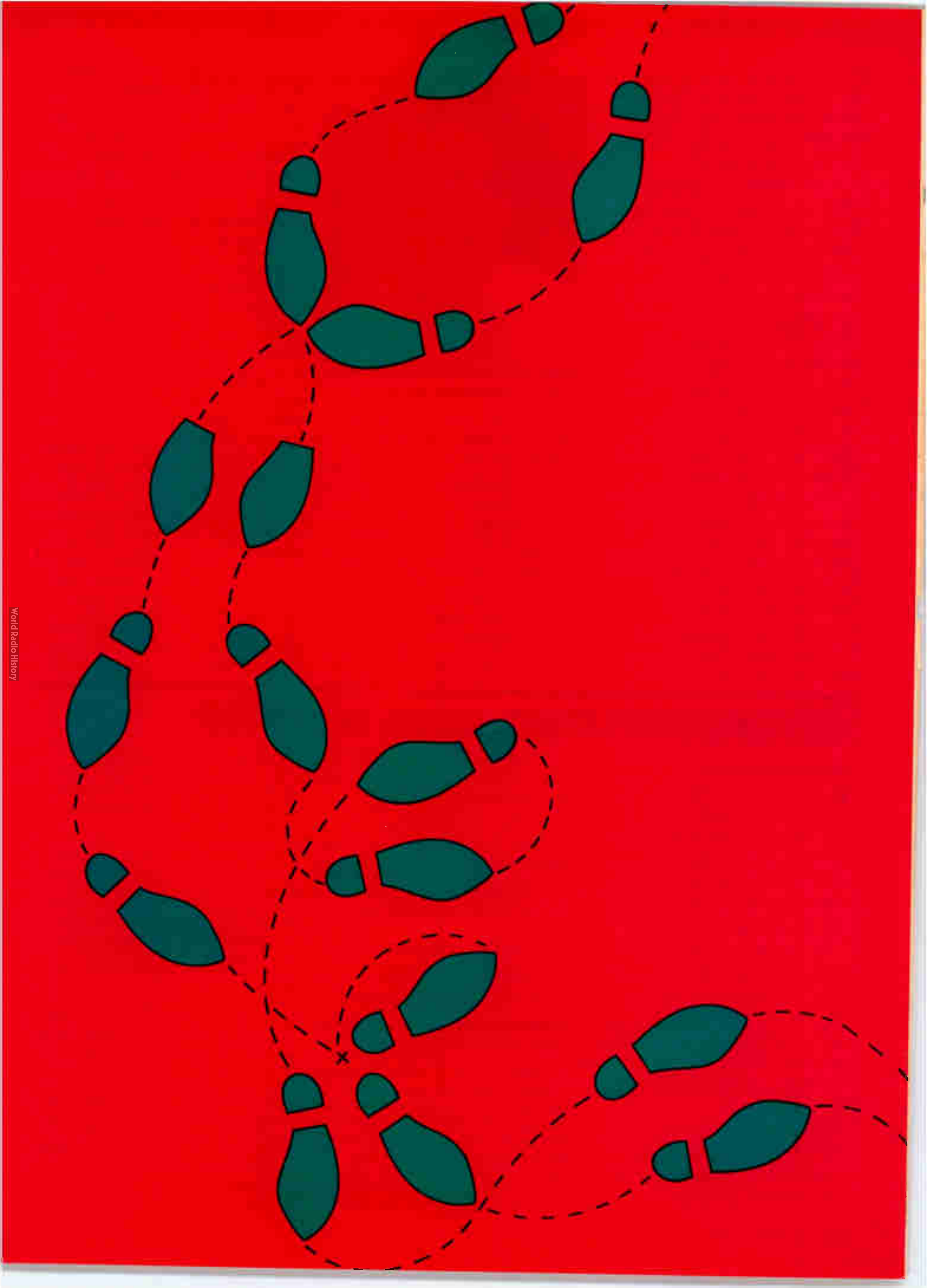
The most successful company to date offering this class of computer, Convex Computer Corp. of Richardson, Texas, spotted this market niche about two years ago. Convex predicted a demand for computation-intensive machines to fill a gap between the fastest superminicomputers and the big supercomputers.

Since Convex opened the market, other companies such as Alliant Computer Systems Corp. [*Electronics*, July 29, 1985, pp. 26 and 56], Scientific Computer Systems Corp. [*Electronics*, March 10, 1986, p. 69], and Culler have brought minisupercomputers to this very new market. Culler introduced its full-fledged line of minisupercomputers, called the Culler 7 Series, late last year [*Electronics*, Nov. 25, 1985, p. 43].

Now Culler is betting that there is another niche below the minisupercomputer market, and it is attempting to adapt the low end of its line to the office environment at less than $100,000. The new PSC (for Personal Super Computer) is designed as a computation engine to add muscle to engineering and scientific work stations. The designers created this new type of computer by linking the user processor of its Culler 7 system with work stations made by Sun Microsystems Inc., Mountain View, Calif.

The PSC is a scaled-down Culler 7 without the kernel processor, a 68020-based front end. The processor, in a package that measures only 27 by 16 by 36 in., requires less than 1,600 W from a 115-V power source and fits nicely in an office environment. Anyone with a reasonably-sized Sun work station already installed that needs more powerful computation can add it by buying the little PSC box (photo, p. 20).

Though it does not replace supercomputers or even minisupers—Culler



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Transputers are high performance microprocessors optimized for high level language use, and incorporate special features for multi-tasking and multiprocessor support. The IMS T414—the first in the family—is a 32-bit machine, integrating a high performance processor, 2 kilobytes of fast RAM, four full-duplex interprocessor communications links (with an eight channel DMA engine to service them), and a 32-bit memory interface which includes a DRAM controller: all on a single CMOS chip, dissipating under a watt. And the best part—it's available now.

With its special design, the processor offers execution rates up to 10 MIPs. It combines direct support for multitasking, floating point and block transfer with submicrosecond procedure call and task switching.

The links are used to connect any number of Transputers to form systems for a wide range of applications, including numerical computation, AI, robotics, distributed systems, real-time control and digital signal processing.

Development tools for the T414 are available now to support programming both single and multiprocessor systems. Versions of the development system exist for use with IBM PC XT and AT machines, VAX/VMS and Stride 440.

The Transputer family includes 32 and 16-bit Transputers, peripheral controllers, link adaptors, evaluation boards and development tools to support OCCAM, C, Fortran and Pascal.

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May 7	Portland	(503) 620-1931
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May 9	St. Louis	(314) 521-6683
May 12	Dallas	(214) 234-8438
May 12	San Jose	(408) 988-6300
May 13	*San Jose	(408) 988-6300
May 14	Austin	(512) 346-9186
May 14	+Los Angeles	(818) 704-1655
May 15	*Los Angeles	(818) 704-1655
May 16	Houston	(713) 531-4144
May 16	Orange County	(714) 261-2123
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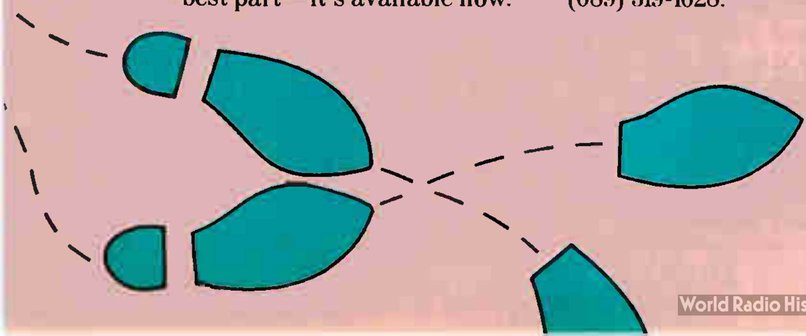


Circle 19 on reader service card

is still offering the Culler 7 line—work-station users can now add computational servers or array processors to their networks when the computational requirements of their application programs outstrip the capabilities of the work-station processors. The $98,500 PSC will give engineers who already have a Sun work station a way to add high-speed vector computation to their networks.

NEW PACKAGING. The PSC is rated by Culler at 18 million instructions per second and 8 million floating-point operations per second. The company's designers achieved the small size and low price by throwing out the 27-slot backplane and the kernel processor of the low-end Culler 7 and repackaging the user processor and memory board set in a 12-slot backplane and small cabinet. Because the PSC can work as a server in a Sun work-station network and as a stand-alone unit when paired with a single Sun station, it offers a way for small work-station networks to add a vector-processing server at a much lower cost than the current crop of minisupercomputers—$100,000, versus $250,000 to $750,000.

The user processor of the PSC has some parallel computing features. The processing functions are divided between two machines (the XY and A processors) that operate in parallel. Even within the proprietary XY machine there is some parallelism. It contains a parallel floating-point arithmetic logic unit and a separate floating-point multiplier. The A machine relieves the XY math processor from dealing with memory operations and program-sequence changes.

The marketing strategists at Culler may have hit on a new market niche,

COMPACT. The PSC fits neatly beside a desk and pulls supercomputing into the office.

and their technical team has come up with a product quickly. If indeed a sizable market exists, Culler's success will depend not only on how well it services that market but on how quickly its competitors can jump in—if Culler's engineers could turn it around quickly, then others probably can. too, although other minisupers might not split in half so readily. But if the idea catches on, work stations other than the Sun could use such an attachment. *–Tom Manuel*

MILITARY

IR DETECTOR ARRAY 'SEES' BETTER AND FARTHER

ANAHEIM, CALIF.

Infrared detectors, which give guidance systems the "eyes" to spot targets at night or in bad weather, have greatly improved the accuracy of weapons delivery in recent years. But a new generation of weapons—smart missiles, advanced aircraft, and the like—need even better detector performance, which means sharper images at much longer ranges than the several miles or so now possible.

Now a new round of detector research seems to be close to satisfying that need. All players are working to mass more detector elements on one chip in what is called a focal-plane array. Among the achievements of the last few months is the successful fabrication of 128-by-128-element single-chip detector arrays.

The latest 16,384-element array to surface comes from Northrop Corp., which scored against competitors by demonstrating the array late last year in a target-recognition test. "Our focal-plane array obtained clear images at distances beyond 10 nautical miles," claims W. Dean Baker, vice president of engineering at Northrop's Electro-Mechanical Division in Anaheim.

Northrop claims that achieving imaging at this distance is a first, and that it is important because "that's a tactically useful range," says Baker.

But Northrop is by no means alone at the 16,384-element level. Hughes Aircraft Co.'s Santa Barbara Center, for example, says it delivered an array of this size to an unspecified U. S. Navy customer last year without fanfare.

The Hughes array was fabricated in the workhorse detector material, mercury cadmium telluride, the only material that works in the most useful IR sensing window—the 8- to 12-μm region. But Hughes' 16,384-element HgCdTe array is in fact tuned to operate in what is known as the midrange sensing window—3 to 5 μm. This is the region the Northrop offering uses, but Northrop makes its array with easier-to-handle indium antimonide (InSb).

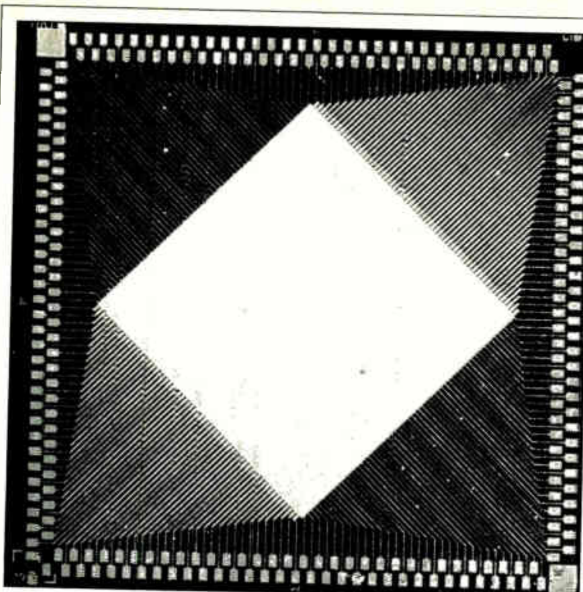
The first 128-by-128 IR array was made by General Electric Co.'s Electronics Laboratory, Syracuse, N. Y., of InSb. Its fabrication was announced more than a year ago, but further developments have not been made public. Texas Instruments Inc., another major player, says it will have a 128-by-128-element HgCdTe array ready early next year.

FERTILE FIELD. Sorting through all these initial claims is a tough proposition without enough data, observes Samuel Lambert, chief scientist of the Air Force Weapons Laboratory, Eglin AFB, Fla. "But it shows how much is going on now in this field," adds the veteran IR researcher. Northrop's array chip "could be a coup for them," he says, even though it is made of InSb, which is inherently limited to midrange IR operation. The reason is that Northrop has proved it can fabricate the devices "in more than just ones and twos." It also has taken the chip to the demonstration phase and is now packaging it for several specific tasks.

The relative usefulness of the mid- and top-range IR detection windows is debatable. The top-range "8- to 12-μm band has a definite advantage," according to Lambert. Generally, this advantage stems from the fact that devices operating in this wider window can collect more thermal energy radiated from targets.

But Northrop's Baker points out that the midrange 3- to 5-μm window is suitable for certain tactical military sensing applications—in air-to-air and ground-to-air weapons. For example, he says the narrowness of the window is an advantage because it is harder for enemy electronic-warfare gear to neutralize a sensor operating within it.

Baker says Northrop researchers chose InSb because it was much easier to work with than HgCdTe and because silicon production gear could be altered to handle it. The company skipped the 64-by-64-element level when its studies based on a 32-by-32 chip showed the move to 16,384 detectors was feasible. Each detector element is slightly less



IR EYE. Northrop's 128-by-128-element infrared detector array produces clear images of objects 10 or more miles away.

than 1 mil wide, and the chip is about ⅛ in. on each side. It is mounted in a hybrid package with eight CMOS addressing chips and four preamplifier devices. At present, the hybrid measures about 1.5 in. on each side, but researchers are aiming to reduce that figure by half.

POD SIZE. Northrop has initially earmarked its array to offer a night-vision edge for two existing tactical programs: the TV sensor system on the Navy's F-14 Tomcat fighter, and the tracking gear on the Hawk antiaircraft missile used by the Army and the Marines. The array package, even with the cryogenics that conventional IR detectors require, fits into a small pod on the F-14 because it is much smaller than previous IR sensors, according to the company. The array extends the pilot's unaided sight by a factor of 10, Northrop says.

Though detector suppliers are progressing, Air Force scientist Lambert warns that there are yield and uniformity problems with advanced high-density arrays. Some yields are as low as 1%, which raise costs sky high, and the history of detectors is that uniformity is hard to achieve. When sensitivity "varies all over the place, as is typical, it's like eyeballs receiving different signals," says Lambert.

Another barrier is the challenge of processing the sensors' massive data stream. Doing this task well has often been a problem for companies that make detectors, says Lambert, although upcoming digital signal-processing chips from suppliers in the military's Very High Speed Integrated Circuits program should help.

Baker confirms that computing the sensed data in the new focal-plane arrays is a ticklish job because gain and offset have to be continually corrected "on a pixel-to-pixel basis."

This is one improvement Northrop is pursuing as polishes its array into a product. Sometime next year, the company expects to conduct a full flight test on the F-14. Already, however, the working 16,384-element array is stirring interest among military users who had not been seriously considering such devices for systems on the drawing board. Says Baker, "It provides data to give them confidence to go forward." *–Larry Waller*

ARTIFICIAL INTELLIGENCE

EXPERT SYSTEMS MOVE FAST IN MEDICAL ANALYSIS

AVIGNON, FRANCE

Expert systems are penetrating medical analysis in Europe faster than any other single application, if a recent conference on artificial intelligence is any gauge.

One of the principal European conferences on artificial intelligence—expert systems and their applications—was held in Avignon last week, and nine papers were devoted to medical diagnostic expert systems already completed or in advanced stages of development. That's more than double the number in any other field.

"In some ways, medicine is the ideal field for expert systems in their current state of development," asserts Luc d'Arras, the founder of Delphia SA, a Grenoble, France, company that specializes in artificial-intelligence tools, particularly those based on the French-developed Prolog language.

"The reason is that in medicine there are many well-defined areas where our understanding of the analytical problems is very complete, and we can include everything that is known within the limits of the program," he explains. D'Arras' own company is developing two medical expert systems for future commercialization.

A consensus of the conference was that there are still few "major" expert systems in operation, where a major system is defined as one dealing with a large number of complex rules and capable of using its experience to evolve its knowledge base. Financial portfolio management and high-level accounting work would fall into this category.

Gerald Barber, president of Gold Hill Computers in Cambridge, Mass., estimates there are fewer than 10 major systems in the entire U. S. "It seems obvious, but people tend to forget that developing an expert system requires an expert who can express his knowledge of his field clearly," he declares. Another problem, Barber says, is that any criteria that are actually abstract feelings can't be integrated into a knowledge base—so, for example, people have tried in vain to develop expert systems to choose stock market winners.

SPECIALIZING. Integrating feelings wasn't a requirement in the medical applications presented at the Avignon conference, most of which are aimed at freeing doctors from time-consuming work or giving generalists access to highly specialized knowledge, rather than at taking over essential diagnostic functions. Two systems, for example—one developed at the University of Nancy and the other at the University of Marseilles—are devoted to the treatment of certain diabetic conditions.

The former, designed for use by nurses or patients, uses Apple Computer Inc.'s IIe personal computer to calculate a patient's dose of insulin as a function of blood analysis and environment. The program can also teach the patient to calculate the dose independently.

The Marseilles system, by contrast, is aimed at more difficult aspects of diabetes and tries to bring specialists' knowledge to general practitioners. For more than 90% of the cases in a verification study, it delivered diagnoses and prescriptions that agreed with those of two specialists for the identical cases. In addition, it scored far better than a group of general practitioners used as a control group for measuring reliability.

The program is now available to a group of some 40 doctors in the Marseilles region. It runs on a Digital Equipment Corp. VAX computer at the university, and the local doctors access it using a teletext interface and the French low-cost Minitel terminal.

Also presented at the Avignon conference was an orthodontics scheme for fitting braces, from the University of Toronto. And the most general medical application aired at the meeting was a diagnostic system for use by nurses and pharmacists in third-world countries. Developed by Medicins Sans Frontières, a French nonprofit organization, the system runs on a battery-powered laptop computer for maximum portability.

But if the medical possibilities of expert systems were much in evidence, so were the limitations. A presentation from the Pitié-Salpêtrière Hospital in Paris concerned a system for the diagnosis of thyroid conditions. A participant asked Christine Pineau, who delivered the paper, why pregnancy, which can have a significant effect on thyroid conditions, was not included in the system's decision criteria. Pineau answered that including it would "simply add too many variables to make the diagnosis of an expert system reliable. The [medically] difficult cases are best left to the specialists." *–Robert T. Gallagher*

TELECOMMUNICATIONS

PRODUCTION DEFICIENCIES MAY SLOW EAST GERMANS

LEIPZIG, EAST GERMANY

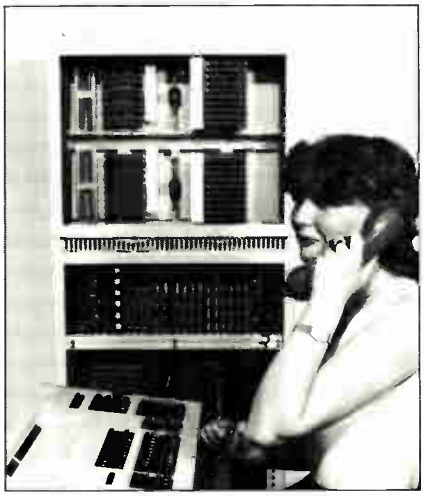
East Germany has embarked on an ambitious course to modernize its industry with advanced microelectronics-based equipment. But what could slow the drive, some Western observers say, are deficiencies in components production technology.

Big changes are projected for the communications sector, in which East Germany is considered to have particular expertise and where a speedup in the rate of product development is planned. The plans include switching to digital technology and beginning the integration of services such as speech, data, text, and video communications into a single system.

The country's latest five-year plan also calls for huge increases in the use of computer work stations and robots by 1990, as well as big jumps in the production of office equipment and personal computers (see "East Germany's 5-year plan makes big demands").

Western observers give high ratings to East Germany's efforts in communications and are convinced it will reach its targets in technology for the integrated services digital network (ISDN). One West German analyst who keeps tabs on the Soviet Bloc points to the advances the country has made in fiber-optic communications. East Germany has been active in this field since the mid-1960s and is said to be closely cooperating with the Soviet Union to replace outdated communications links in that country with fiber networks.

But production shortcomings may stall the latest communications efforts. Says one analyst at a U.S. semiconductor maker in West Germany, "In the lab, the East Germans, like the Russians, are making excellent devices, given the high level of sophistication of research equipment." But for volume fabrication, they lack the production systems to turn out components of high reproducibility, quality, and reliability, he says.



AUTO. VEB's NZ400D PBX allows manual and automatic buildup of connections.

But many industry watchers believe the Eastern Bloc, and East Germany in particular, eventually will iron out these problems—"not least because inaccessibility of Western markets forces them to," according to one source. He rates the Bloc's military communications links on a par with Western civilian networks.

Handling East Germany's activities in communications is VEB Kombinat Nachrichtenelektronik, Leipzig, a state-owned combine of 17 manufacturing facilities and one research center, the Institute for Telecommunications in East Berlin. The combine employs some 39,000 people, including 5,000 scientists and engineers. Its annual output is estimated at more than $1 billion. More than half of that is exported, mostly to the Soviet Union.

Perhaps the combine's best example of its switching technology is the NZ-400D microprocessor-controlled digital private branch exchange. Developed at the combine's manufacturing facility, Fernmeldewerk Neustadt-Glewe, and using information-processing technology from the Dresden computer combine VEB Robotron, the system is modular in both hardware and software, is ISDN-compatible, and is designed to handle from 16 to 384 subscriber lines.

Its features include manual and automatic buildup of connections, call-charge recording and registration, automatic transfer of calls, abbreviated dialing, conference calls for up to six subscribers, push-button dialing, dial repetition, and automatic ring-back. A receive-only teletypewriter or a printer can be connected for putting out protocols relating to system operation and service.

The NZ400D is controlled by an 8-bit multiprocessor system consisting of a central control processor and two decentralized processors, all coupled by parallel interfaces. The information flow within the exchange is over a PCM-30 bus system. Programmable one-channel codecs are used for speech-path switching. Storing the programs and the rele-

EAST GERMANY'S 5-YEAR PLAN MAKES BIG DEMANDS

East Germany's new efforts in microelectronics are part of its latest five-year plan, revealed at the country's 11th Communist Party Congress in East Berlin in late April.

Erich Honecker, East Germany's president and the party's general secretary, exhorted the delegates to help speed up the use of the latest advances in industrial equipment and urged the industry to meet the "higher demands" that trading partners and domestic consumers are putting on product quality.

The country aims to make its economy grow by 24% to 26% from 1986 to 1990. Industrial production is to rise 22% to 24%, while net wages are to go up at least 22% in the next five years.

These figures are the same as or higher than those set for the previous five years and will help East Germany maintain its standard of living as the second highest in Eastern Europe, behind Hungary. Last year, the East German economy, which Western observers rate as Eastern Europe's most efficient, spurted ahead 4.8%, the biggest jump among socialist countries.

To hasten growth, use of computers in the country's VEBs (the initials for the German words meaning people-owned enterprise) will be pushed more than planned in the first draft of the five-year plan made several months ago.

Instead of the 28,000 computer-based work stations envisaged for 1986 to 1990, the plan now calls for the installation of up to 90,000 such stations. During the next year alone, about 17,000 office and personal computers are to be produced, 10,000 more than originally planned.

By 1990, East German factories are to double the 65,000 robots—which are mainly industrial manipulators—now in operation. Production of microelectronic components is to rise nearly 40% in value and more in units. *–J. G.*

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vant system data are dynamic random-access memories. The system's key components are 8-bit U880 microprocessors from VEB Kombinat Mikroelektronik, in Erfurt.

For communications between the system and the operator, a control console works as a processor-controlled peripheral unit of the central processor. It has a keyboard, a 16-digit display, and a light-emitting-diode display area.

The system consumes about 2 W per subscriber line and requires only 0.2 hours of service per line per year. A system for 128 lines uses about 0.15 m^2 of floor space. *–John Gosch*

BUSINESS ABROAD

SCOTS, IRISH NO LONGER COURT JUST ANY FIRM

LOS ANGELES

Not surprisingly, the sharp business downturn that dealt so harshly with the U. S. electronics industry last year also hit those countries that rely heavily on American companies for plant expansion.

The slowdown virtually eliminated 1985 expansion activity in Scotland and Ireland, two highly successful practitioners of industrial recruiting. Officials from the two countries, keen but gentlemanly competitors, used the slow period to rethink their strategies and already are putting new ideas to work, they say.

HANNA. Ireland offers excellent support for process-control firms.

The new approaches depend on choosing the companies to be courted on a more selective and more systematic basis. The choices are rooted in more quantitative advanced planning, planning that can spell out benefits in detail. "Now we're narrowing in, being more precise," explains David P. Hanna, West Coast director for Ireland's Industrial Development Authority. "In the good old days [before 1985], we would have gone after everything."

A similar plan emerged from rethink sessions at the Scottish Development Agency late last year, says North American director Donald Harrison. As a result, "we now can go into a corporate headquarters [of a U. S. company] with a solid strategy for it."

Hanna and Harrison say the more focused development efforts would likely have evolved in due course, but the recession brought them about several years earlier than steady progress would have. A stark fact underlying the new strategies—and emphasized by slow 1985 business—is that most of the major companies in the U. S. and elsewhere have already made such commitments. "The larger companies have been pretty well trolled over," Hanna says.

A key part of the new pitches coming from Scotland and Ireland stresses more heavily the advantages of technology and engineering infrastructures. These infrastructures are composed of services available from companies that have already grown to support industry.

In Scotland, equipment and services for semiconductor and computer manufacturers are supplied by an especially strong group, says Harrison, because about 15% of Europe's chip production takes place there, and an IBM Corp. plant that makes equipment sold in Europe is there as well. Ireland stresses its engineering services for process-control companies, which it claims have reached world-class quality.

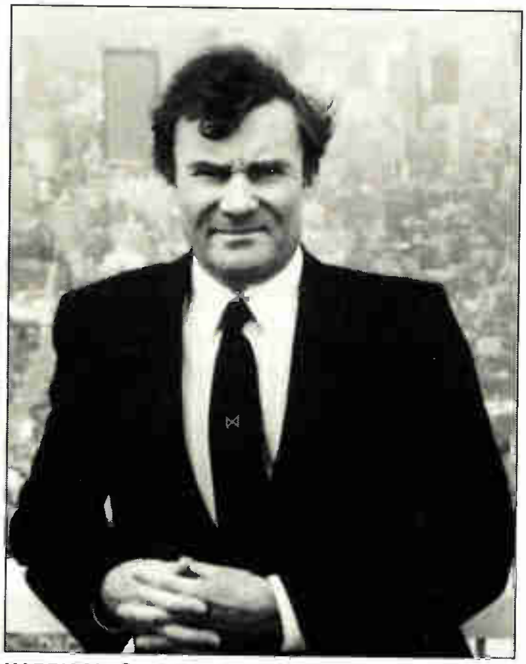
The two countries therefore differ greatly in which companies they go after. Scotland's sights are on volume production operations—printed-circuit-board stuffing and assembly, for example, of the type usually slotted for the Far East. Scottish development officials have prepared cost comparisons that show an advantage over Oriental plants for boards aimed at European markets. "We are actively marketing that," says Harrison, who notes that a local board manufacturer now supplies an Apple Computer Inc. plant in Singapore.

On the other hand, Ireland is stressing the high margin benefits of its quality engineering force in adding value for such products as scientific instrumentation. This pitch has been a factor in snagging its newest addition, a plant for scientific instrument maker EG&G Inc., Wellesley, Mass., which will eventually provide some 500 jobs.

SMALLER TARGETS. The narrower focus has points in its favor, but it is clear that many more smaller companies must be bagged for a gain in jobs equal to that achieved by bringing in one of the larger species of quarry sought in years past. "We now have to bring in three or four companies instead of one," notes Hanna. The size of the U. S. companies courted will likely be in the $20 million to $30 million sales class; even smaller companies from elsewhere will be on Ireland's lists.

Scotland and Ireland were both affected by the worldwide electronics slowdown, but Harrison and Hanna say the result was largely one of no growth. They were not hit by the disastrous slide in sales that occurred elsewhere.

Scotland has lured nearly $2 billion in investments since the 1970s and this year expects electronics exports to surpass Scotch whiskey in value. Ireland has garnered about 100 electronics companies during the past decade. "We were used to onwards and upwards," admits Hanna.



HARRISON. Scotland has built a strong infrastructure to back producers of semiconductors and computers.

As measured by employment, the Scottish electronics industry held a 45,000-plus level for 1985, while the Irish industry stabilized at about 26,000 workers. Both countries experienced plant closings, however. General Instrument Inc. shut down its operations in Scotland, and Ireland lost facilities run by Mostek Corp. and Storage Technology Co.

The two development officials believe that weathering the recession as well as their countries did proves that foreign-based expansion plants are not the first to be cut when chilling business winds blow hardest, as some critics had predicted. "The fact we did not suffer wholesale slaughter shows we have the right type of companies," Harrison says. *–Larry Waller*

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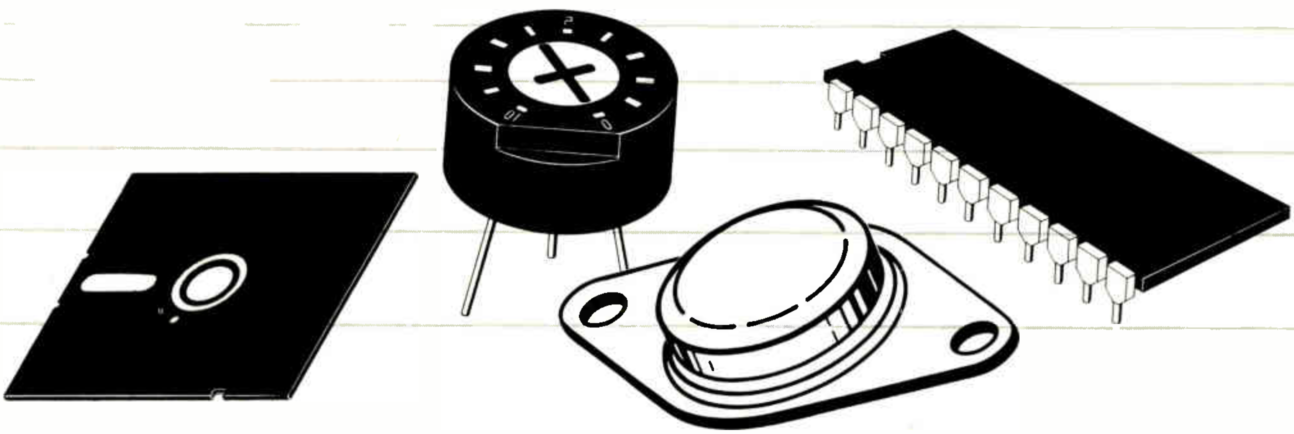

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RISC: IS IT A GOOD IDEA OR JUST ANOTHER HYPE?

DESPITE THE FLAP, IT'S BEGINNING TO CHANGE COMPUTER DESIGN

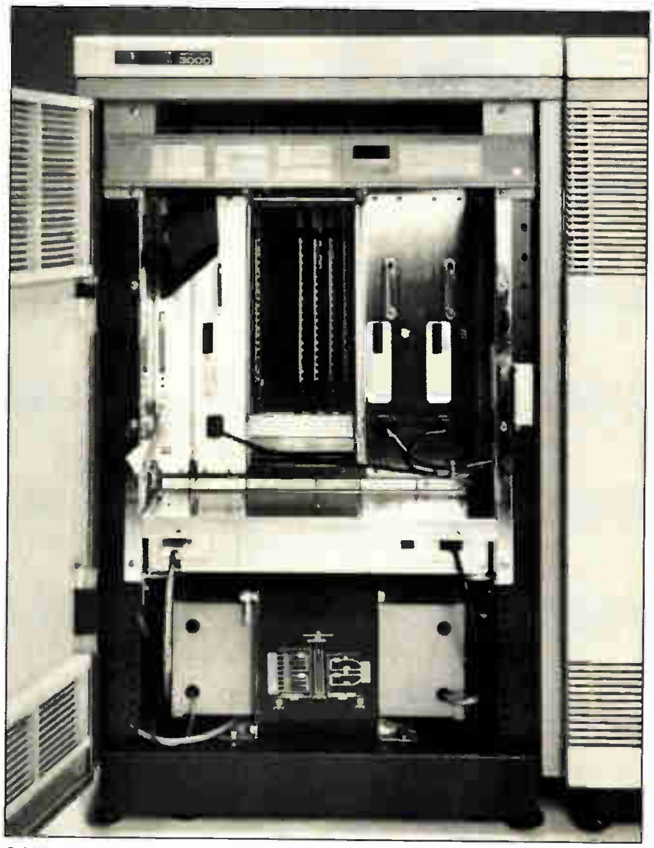
by Clifford Barney and Tom Manuel

There's so much noise being generated now about the reduced-instruction-set computer and whether such designs are a big step forward that it tends to obscure what's really happening in computer architecture. The RISC concept is gaining increasing credibility as it starts showing up in major commercial designs. New products from Hewlett-Packard Co. and IBM Corp., for example, are helping a lot to move RISC out of the realm of debate and speculation and into the real world.

Yet the debate still rages on whether the RISC concept that was born a decade ago in the rarefied atmosphere of academia can be successfully applied to the design of commercial machines. Complicating things further is that computer scientists cannot even agree on just exactly what a RISC machine is.

The RISC concept emerged in 1975 at IBM's Thomas J. Watson Research Center in Yorktown Heights, N. Y. (see "How it all began," p. 29), when John Cocke, an IBM Fellow, came up with the idea. Cocke is considered the father of RISC, although the term was first used at the University of California at Berkeley, where graduate students under David A. Patterson designed a microprocessor they called RISC I. Other early RISC research was done at Stanford University in Palo Alto. As interest in the concept mounted, commercial RISC or RISC-like computers were produced by Acorn Computers, Celerity, Harris Computers, Pyramid Computer, Ridge Computers, Shiva Multisystems, and France's Thomson. Most recently, Mips Computer Systems, Sunnyvale, Calif., has introduced a blazingly fast "pure RISC" system based on the chip developed by John Hennessey at Stanford (see story, p. 56).

Now IBM and HP have minted two of the newest designs applying basic RISC principles. One is the IBM RT Personal Computer (see story, p. 34), and the other is HP's Precision Architecture [*Electronics*, March 3, 1986, p. 39], which is being used first in the new HP 3000 series 930 minicomputer. They both apply such principles as a small set of simple, regular instructions that execute in one cycle, only load and store instructions can access memory, other instructions operate only upon registers, hardwired control is used instead of microcode, and complex compilers provide complex functions and generate the optimal code for the machine.



COMMERCIAL RISC. The HP 3000 series 930 is the first product from Hewlett-Packard built with its new RISC-based architecture.

As interest has grown in the RISC concept, so has debate over it. The arguments swirl around the closely related questions of applying the university-nurtured technology to commercial machines and how to define RISC. In fact, the acronym has turned into such a buzzword that an argument over RISC versus complex-instruction-set computers practically drained all other sessions at Compcon in San Francisco in March.

Looking back on that debate—a panel discussion entitled "The Great RISC vs. CISC Debate"—G. Glenn Henry distinguishes between work done on RISC at universities and in industry. "The RISC chips done at UCB and Stanford really are the classical RISCs," says the IBM Fellow, who is also manager of hardware and software system development for the IBM RT PC at the company's Engineering Systems Products independent business unit in Austin, Texas [*Electronics*, April 28, 1986, p. 54]. "But RISC is a misnomer for the work being done in industry—for example, here at IBM in Austin and at HP.

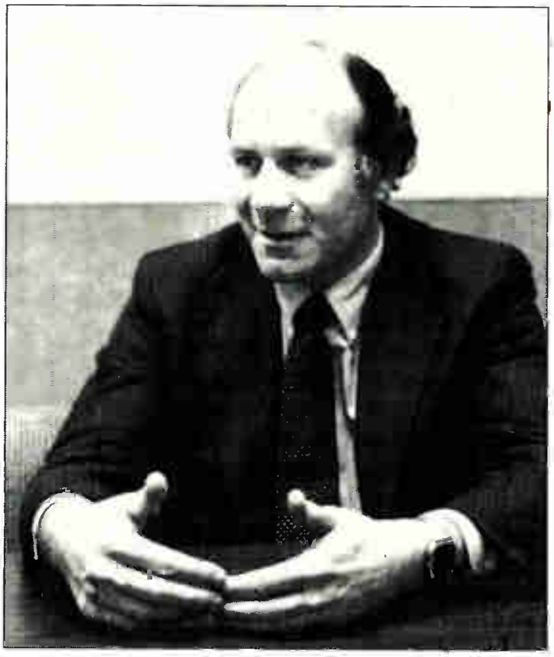
"The commercial systems have some complex instructions where they are needed," he continues. "The classical RISC chips out of the universities are very simple—just chips, not complete systems. Therefore, it is rather unrealistic to compare performances of these to the performances of commercial systems."

Performance measurements cited for the RT PC were made using real applications running under AT&T Bell Laboratories' Unix operating system with virtual memory and error correction turned on and fully operating. They were not done with simple benchmarks on a stripped-down microprocessor, Henry notes. "But wait," he quickly adds, "I'm not putting the universities' work down. They did good work. They learned things that we all could put to use."

Another IBMer rejects that notion. Nick Tredennick, a researcher at IBM's Watson Research Center, led an attack on RISC at Compcon. "RISC is a poor idea for commercial microprocessors," he said. "Commercial microprocessors are bandwidth-limited at the pins already, and reducing the instruction set makes the problem worse."

One argument against RISC is certainly that with fewer instructions, doing a particular task takes more instruction execution, concede Henry and Joel Birnbaum, an HP vice president and head of the Palo Alto company's RISC-like Spectrum project. That would mean that more memory bandwidth would be needed to deliver those instructions to the processor. "But," says Henry, "Tredennick works on putting a 370 on a chip, and for that task he can't use the classical university RISC. That's probably what he is talking about when he says that RISC is a poor idea for commercial microprocessors." Henry has proved that a commercial computer system can be designed using RISC principles while still solving the memory bandwidth problem.

HP's Birnbaum says that "Tredennick is right, in one sense, to say that RISC won't work in a commercial microprocessor. But what's RISC? If you are talking about the Berkeley chip, as opposed to a set of design principles upon which you can build, that's such a trivial and obvious argument it isn't worth making. It's like arguing about how many angels can dance on the head of a pin."



A BETTER MOUSETRAP. HP's Joel Birnbaum believes RISC principles, rigidly applied, lead to better computers.

David Patterson, the Berkeley computer scientist who helped start the debate four years ago, agrees that by now the argument is irrelevant. "In 1981 and 1982, it was heretical to suggest that you could improve performance by transferring hardware functions to software," Patterson says. "It was supposed to go the other way. In 1986, rather than argue, let's see what people have built. The professional designers and the computer buyers will be the judges."

Even these judges, Birnbaum contends, won't be intent on classifying computers as RISC or non-RISC machines. "I don't know whether Spectrum is an architecture that proves that RISC is viable or that it is not," Birnbaum says. "The reason is that there is no 'RISC architecture.' There is a set of principles which can be applied in a particular architecture to solve a design goal."

These principles—such as single-cycle execution and absence of microcode—cannot be applied blindly to a commercial computer, Birnbaum adds. "We have some multicycle instruc-

HOW IT ALL BEGAN

It all began in 1975 when IBM Fellow John Cocke had an idea. Cocke, then a researcher at IBM's Thomas J. Watson Research Center in Yorktown Heights, N. Y., decided that a computer with a simple architecture, using a simple instruction set, could have certain advantages over the trend toward computers with increasing architectures and more complex instruction sets. In the late 1970s, graduate students at the University of California at Berkeley gave it the label it goes by today—reduced-instruction-set computer (RISC).

Cocke and his small team of researchers at first tested the idea's feasibility with a research prototype—the 801 computer (named after the number of the building where the team worked). The original project, however, did not have a new computer architecture as its objective. "We were studying what would be needed to make very large telephone switching systems, and a very fast controller was one of these needs," says Cocke, a 30-year IBM veteran. "After the switching project was abandoned, we started to consider the controller as a machine in itself." The result of the redirected effort was the 801 minicomputer prototype, which was built in 1979.

The research team experimented along many avenues to reach their objective of an efficient new architecture. It was not just slashing away at the instruction set. "In fact," says Cocke, "while it's true that we reduced the number of instructions, that is more a result than a cause. We didn't believe we should put complicated instructions into a machine when they can be built up from simpler ones without sacrificing performance."

JOHN COCKE: The inventor of RISC.

Cocke and his researchers also took advantage of advances in compiler technology. The new compilers were getting smarter at automatic programming and code optimization. The compiler technology made simple machine instructions feasible because if a complex instruction were needed, the compiler could string together simple instructions.

The 801 designers also put to use large, very fast memories. "Since the memory hierarchy of the 801 minimized problems of storing and retrieving information and we had designed the instructions to all be the same size and execute in one cycle," Cocke says, "we were able to build in a lot of overlapping—pipelining—of the execution of instructions." The 801 and other RISC machines pipeline nicely because of their simple organization and instructions. *—Tom Manuel* tions. So if you want to say we are not RISC, that's OK. On the other hand, most of the Spectrum instructions execute in one cycle. We have some microcode, to help with input/output. So we have RISC architecture, but it goes far beyond RISC."

Yale Patt, the Berkeley professor who chaired the Compcon session, calls RISC a "useless label," because "people can't agree on what it means." He suggests a new microprocessor category, "RISC-but," into which HP's Spectrum fits neatly.

In Glenn Henry's idea of RISC, "the key is to get the processor speed as fast as you can on the smallest amount of silicon and, at the same time, separate the processor from the bottlenecks of memory and I/O." This is necessary, he says, because in recent years very large-scale integration has produced processors that are much faster than memory and I/O circuitry. The goal is to make a single processor chip run as fast as possible, independent of memory and I/O speeds.

ADVOCATE. David A. Patterson of UC Berkeley was the first promoter of RISC principles for computer design.

Henry says a computer architecture must incorporate three design concepts in order to be a true RISC. First, it must overlap processing with memory accesses. Second, instructions must operate in a single cycle. This generates the swiftest performance possible for a given VLSI speed; when the VLSI implementation can be scaled down even further, the processor will run faster. For example, if IBM builds its RISC microprocessor in 1.5-μm CMOS instead of the current n-MOS process, the chip will speed up significantly.

EFFICIENT TARGETS

The third, and most subjective, qualification for a true RISC architecture by Henry's definition is that all instructions should be designed to be efficient targets for high-level languages. High-level-language compilers are then built to take advantage of the benefits of such architectural principles as the separation of storage from the processor. For example, the compilers must be able to organize instructions and data flow to use the architecture efficiently. "Therefore, we will get good compilers [as a fallout] from the work on RISC architectures," Henry says.

Henry's idea for the best term to replace the often misleading and confusing acronym RISC, is optimized-instruction-set computer (but OISC is more difficult to pronounce). "The optimized instruction set is optimized for compilers, optimized for maximum performance from individual processors, and optimized for not wasting silicon area," he says.

The opposite of optimizing the use of the silicon area is the temptation to exploit silicon technology. HP's Birnbaum considers complex instruction sets the outgrowth of what he calls "creeping elegance," which arises from this temptation. "There is an argument," he says, "that silicon is free—that we have reached a level of lithography such that it doesn't cost much to put extra transistors on a chip, within certain pin and power limits. So why be dumb enough to have only 100 instructions when for no extra hardware cost you can have 200? This is 100% fallacious. You pay for those extra instructions every time you execute any instruction, in several different ways."

One way is in design complexity, Birnbaum says. "If you have many instructions, you have many more conditions to prepare for and recover from. The design takes longer, and it is harder to change. You even pay in extended time to market." Patterson agrees, saying that with computer power increasing 20% to 40% each year, a complex design may lag the state of the art by the time it reaches the market.

Patterson expresses the actual mechanism by which complexity degrades performance in an equation relating factors that affect program execution time:

$$\text{Program time} = I \times C \times T$$

where I equals the number of instructions executed for a program, C equals the average number of clock cycles per instruction, and T equals the length of each clock cycle.

The basic RISC principle—one instruction execution per clock cycle with no complex microcoded instructions—obviously makes C smaller. It was by reducing this factor that the first Berkeley RISC chips performed so well against commercial microprocessors. Microcoded machines may take 5 to 10 clock cycles per instruction, versus 1.2 to 1.5 for RISC architectures, Patterson says.

Birnbaum and Stanford's Hennessey contend further that the complex instructions will affect cycle time itself. Birnbaum says the key point is "if you have more complexity and more checking, invariably your cycle time will increase. The machine will pay something in performance for all of the extra combinations ... there will be one extra step of the decoder, or the error recovery path will be longer. You pay for complexity even when you are not using it." HP's Spectrum design team paid close attention to the three factors expressed by Patterson's equation (see "How HP made architectural tradeoffs on Spectrum," p. 31).

Both HP and Mips Computer Systems made extensive studies of the effect of adding an instruction on a machine's basic cycle time. Loads, stores, and branches account for more than 80% of all instructions, Hennessey says. "It's then very hard to find an instruction that won't hurt the clock speed." The Mips Computer Systems tests paralleled HP's in pinpointing the number of logic levels required, and the way the system deals with exceptions and interrupts, as the main factors tending to increase cycle time.

Because of those tests, says Birnbaum, "whenever someone suggested we really ought to have a wonderful instruction, like 'test left, shift mask, dim the lights,' we had to ask: 'How often will we execute it, and what is the performance degradation?' If you have a hundred instructions, and one of them is executed only 1% of the time, you had better not incur more than a 1% penalty. Our rule was nothing gets in until we do that analysis."

A THORNY QUESTION

The other factor in the program-execution equation is path length (the number of instructions executed in running each program). It is one of the thornier questions for RISC proponents. Hennessey says a RISC machine will pay about a 30% penalty in added instructions over a machine that uses microcode. "We are willing to take a 30% hit in return for a fivefold improvement in cycles per instruction," he says.

The design goals of the system determine which tradeoffs are acceptable, Birnbaum says. When HP undertook the Spectrum design, one of its goals was to maintain compatibility among the new system and all old machines it would eventually replace. "If we had had no compatibility objective, our job would have been immeasurably simpler," he notes.

As if application-code compatibility was not challenging enough, HP required much more than that. "There's another part—peripheral subsystems, interrupt responses, and input/output compatibility," Birnbaum says. "We worked hard on I/O architecture. The first version HP released in February is essentially our old architecture, because we wanted to use existing peripherals and channel controllers. But what is coming is RISC I/O: direct attachment to the bus from any peripheral. RISC/CISC is down in the noise compared to that problem."

As difficult as the RISC choices were, Birnbaum says, they paid off in a great deal more than just simple system performance. "There is a tremendous flexibility that comes from imposing the discipline of not adding anything unless it pays its way," he says. "Building a microprocessor on a smaller chip, as RISC architecture permits, gives you two different ways to play the game. You can make a very small chip and get high yield and lower manufacturing cost. That might be a good idea for a semiconductor manufacturer. But the chip cost isn't terribly significant compared to system cost, so instead we have the option to put more on a single chip. It's easier to put cache memory, or floating-point circuitry, or virtual memory management on the chip, and run at chip speed instead of package speed. The 950, HP's first RISC minicomputer, is a 7-mips machine not because we have 1-μm technology but because the architecture lets us put the whole processor on a single chip."

PRIME MOVER. John Hennessey spawned a company and a new RISC computer.

Birnbaum predicts that even greater benefits are possible in the future. On-chip coprocessors that straddle the cache and memory buses will make possible very fast special-purpose signal processing, graphics, or encryption systems. "We now have the silicon area to put this circuitry on," he says.

RISC, says Birnbaum, is another iteration of the experimental process in computer design. "In an ideal world, 30 or 40 years from now," he concludes, "people will design computers the way they design airplanes with really good knowledge of aerodynamics and fluid mechanics. But airplanes flew before the science of aerodynamics was invented."

The RISC concept may be at the Kitty Hawk stage, and skeptics may argue that it's just too simple to be practical. But real-world practitioners of computer design retort that the RISC principles are a foundation upon which to build practical machines that are now working well. After all, IBM and HP are no-nonsense outfits—they are not given to taking fliers on shaky propositions. □

HOW HP MADE ARCHITECTURAL TRADEOFFS ON SPECTRUM

To William Worley, principal architect of the Hewlett-Packard Co. Spectrum computer line, the question of reduced-instruction-set computers versus complex-instruction-set computers is not an argument, but a matter of principle.

Worley says three factors affect time to execute a program: average number of clock cycles per instruction, cycle time, and path length (number of instructions used). "RISC reduces the value of the first two of those terms," he says. But making tradeoffs among these three principles is not always straightforward, cautions Worley, who is head of system architecture for the Spectrum project in Cupertino, Calif. Instructions that increase cycle time must be justified by reductions in the other two terms.

The principal influences on cycle time are the way a system handles interrupts and exceptions and the number of logic levels an instruction requires. Interrupts normally affect the critical path of an execution and lengthen it gradually.

The number of logic levels is a step function. "If an instruction requires computation and suboperands that is used in the next instruction, we may reach a number of logic levels that is larger than can be computed in one cycle, and the basic cycle would get larger," Worley explains. "If the instruction repertoire requires n levels of logic to accomplish all of the instructions, an additional instruction requiring $1.5n$ levels would clobber the cycle time."

Data operations can be plotted, since data moves from a register through an arithmetic logic unit and back, Worley says. HP found that the optimum number of logic levels for primitive operations in the instruction set was equal to one more than the minimum possible number of levels.

Instructions requiring more logic levels were broken up. One 8-byte instruction for 32-bit address displacements, for instance, was divided into two 4-byte instructions. That's not the same as resorting to a complex instruction, since it is still executed in direct hardware and does not require microcode, Worley says.

WILLIAM WORLEY: Opting for a RISC architecture is a matter of principle.

Simple instructions can reduce cycle time; but one of the basic RISC/CISC arguments is over how to make the tradeoff between many simple instructions and a few complex ones. "We have to learn to keep the path length small as well," Worley says.

One way HP has approached this problem is through the design of the instruction set. In 33 cases, Worley says, his group found ways to combine in a single instruction operations that formerly took two or more. One example: an instruction to compare two quantities, which previously required a comparison and a conditional branch. HP put the operation in one branch.

"Our tradeoffs don't hit path length or cycles per instruction," Worley says. The tradeoffs made in architecture don't take place in a vacuum and must stand up in different markets, he emphasizes. "We have to distinguish between architecture and implementation. Some implementations will realize all of the theoretical efficiencies of RISC. Not all will. Each implementation needs to make sense as a business proposition. We can push the architecture to the limit, but not every time." *–Clifford Barney*

CONFESSIONS OF A CORPORATE MAVERICK.

"Here I am, considering a major acquisition.

You wouldn't believe what my staff has given me to work with."

There it sits, one metric ton of computer data, entombed in neat binders. "Decision Support," I think they call it.

The information I need is probably buried somewhere in there. But it would take the patience of an archeologist to dig it out. And the biceps of a linebacker.

Young Marley may be my best hope. Tall as a telephone pole, left shoelace untied, he has offered to help. Wants me to go to his office and work with—would you believe this—his computer terminal.

Just what I need. More gross tonnage from a computer. (If you know of any bright young MBAs who can say Yes/No without referencing computer data, send them here, pronto.)

Marley speaks. "Really, Harold," he says, "I think that with MAPPER® Software, the computer can be especially useful to us." He says this with more confidence than any 28-year-old has a right to have.

"MAPPER Software? What's that?"

"You'll see in a moment." Seated at the terminal, the kid looks like a Swiss Army penknife with all the blades and screwdrivers open. Legs and arms are everywhere.

He taps a few keys and—what do you know—there on the display screen is our intended acquisition, stripped bare, financially speaking. Five-year earnings record. Debt-to-equity ratio. Current ratio. The works.

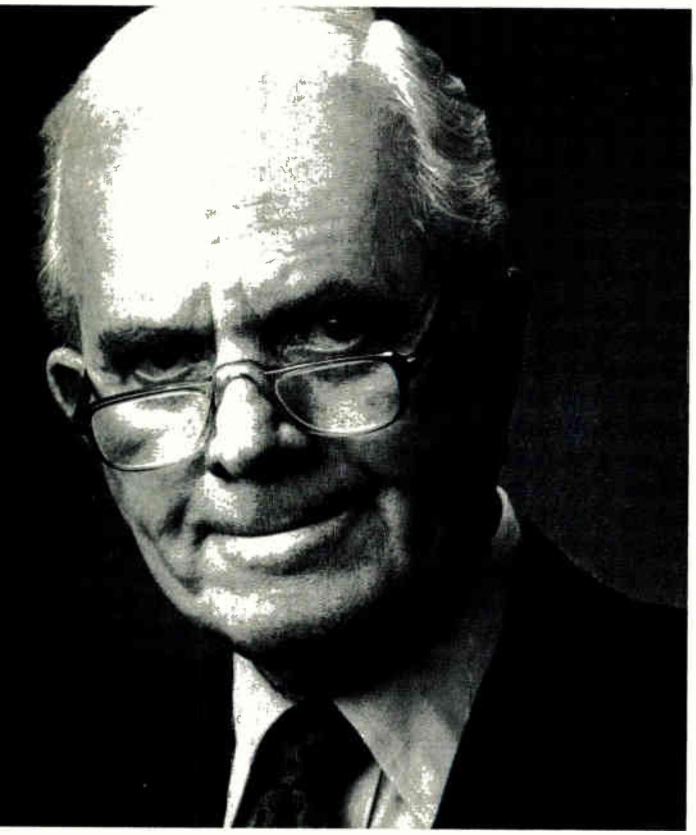
But these figures, of course, are only a beginning. I need to see how the company stacks up against the industry as a whole. How it has performed in recessions and expansions. I need to know a whole lot more, and I tell Marley that. "Have a seat, Harold," he says. "Here, at the terminal."

"I don't know how to use that thing, Marley. And what's more, I don't want to know."

"Try it, Harold."

Within the space of a half-hour, this Ivy League Svengali has me working the computer with some semblance of virtuosity. I'm cross-referencing and correlating and integrating information to a fare-thee-well. Mind you, Marley's coaching me; yet there's a certain logic to it all. I seem to know intuitively what to do.

But most important, I'm getting precisely the information I need. Not someone else's notion of what I need.



"So what do you think, Harold?"

Notice that this gangly overachiever uses my first name at every opportunity. Probably sees it as a merit badge. One more trophy on his way to Eagle Scout. Whatever. I say nothing of this, of course. The protocols of corporate democracy must be maintained.

"Do we have a buy, Harold?"

"That, I don't know yet. There are other things to consider. Like how the acquisition will fit in with our long-range goals. Things like that."

The kid's eyes brighten. "Maybe MAPPER Software can help there, too, Harold."

"Marley, what *is* this MAPPER thing?"

"MAPPER, Harold, is the advanced Sperry software system we've just been working with. It enables end-users like us to develop their own custom applications. Without programming help from DP people, which really saves a lot of time. You can use it for ad hoc or permanent applications. Matter of fact, our whole company is using it, to build systems for operations control and strategic planning and—"

"Marley, spare me that computer double-talk. I'm essentially a simple man."

"Yes sir."

"You called me ...*sir*?"

"You're the president and CEO, Harold."

"What's *your* first name, Marley?"

The kid-looks terribly pained. There's a long pause before he replies. Finally, in a small, choked voice, he tells me. "Penrod. My first name's Penrod, Harold."

I think it's to my credit that I don't so much as blink an eye.

"You've been very helpful, Marley. You and that MAPPER Software. You've saved me the agony of having to plow through all those computer reports over there. I thank you both very much."

As the kid's leaving the room, I notice that now his right shoelace is untied, too. Somehow, I feel...well...kindly disposed towards this giant foal. "Marley," I call after him, "fix your shoelaces."

Nice, intelligent kid; I have to admit that.

But *Penrod*?

Could the extraordinary power of Sperry MAPPER Software solve a difficult information problem for you? It's easy enough to find out. Bring your problem to us and we'll come back with a MAPPER solution. The problem can be operational or managerial: over 500,000 users are running MAPPER solutions for everything from complex accounting systems to strategic planning to shop floor control.

You should know, too, that MAPPER Software can run on hardware configured to serve a single user or hundreds. And you can have MAPPER power without actually buying or leasing a computer—even on a low-cost, short-term trial, if you like.

But first things first. To arrange for a MAPPER demonstration or for a copy of our Information Package No. 16, call us toll-free: 800-547-8362. Or write: Sperry Corporation, Box 500, Dept. 100, Blue Bell, PA 19424-0024.

MAPPER® Software. For whatever you have in mind.

SPERRY

HOW IBM DESIGNED ITS RISC-TECHNOLOGY PC

MEMORY MANAGEMENT CHIP MAKES UP FOR RISC'S MAJOR DEFICIENCY

IBM Corp.'s RT PC work station has two hearts—the ROMP reduced-instruction-set microprocessor and a memory-management unit—but they beat as one. The microprocessor is linked to memory by the efficient MMU (Fig. 1). A RISC chip's stripped-down architecture requires heavy use of memory-resident software instructions, and the MMU provides the large bandwidth necessary to deliver these instructions quickly enough to keep the processor running at top speed.

The two complex, highly integrated custom chips, along with such new techniques as inverted page tables to handle very large virtual memories and tagged memory references to eliminate the need for a cache, serve as the cornerstone of the RT PC effort. The chips contribute advanced functions and high performance to the machine, which is one of the newest commercial RISC units (see p. 28).

The IBM ROMP (for Research/Office Products Division Microprocessor) chip has 118 instructions (table, p. 35). Only the load and store instructions reference memory; the rest are register-to-register instructions. ROMP has 16 general registers. All instructions, except load and store, run in one cycle. The instruction set does not include the classical multiword operations; rather, it does things one word at a time.

There are several major performance features of the ROMP architecture. The relatively small number of instructions leaves more silicon for other uses. Also, the load, store, and branch instructions are overlapped with other instructions—the next instruction ahead, for example. There is almost always another instruction that can be executed during a load, store, or branch—the compiler only has to be smart enough to find it. And the powerful and very fast interface between processor and memory is especially useful for fetching instructions.

One of the disadvantages of RISC is the need for a large bandwidth to deliver instructions: because the instructions are simple, many more of them are required for many functions than there would be for complex instructions.

Many RISC designs use cache memories to provide a fast processor-to-memory interface—Hewlett-Packard Co.'s Spectrum architecture, for example. Instead, the RT PC has a very fast memory bus and a tagged architecture. It can transfer one word of data and one address every machine cycle (170 ns). The bus has 32 lines that function as address lines during half the cycle and as data lines the other half.

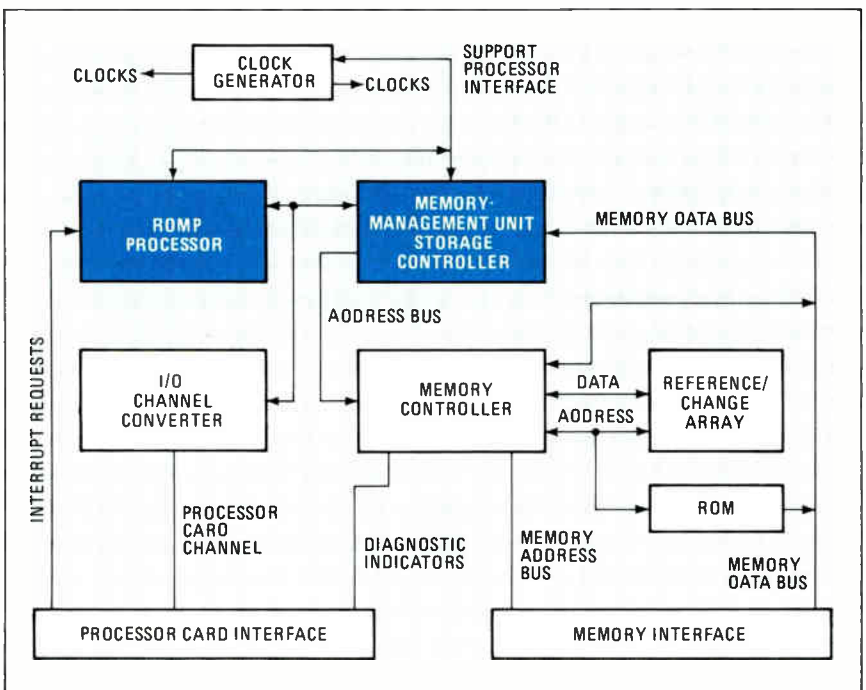
The processor has a continuous need for instructions, so ideally it should never have to wait for them. For this reason, the ROMP processor has a four-word buffer for incoming instructions that is used as a pipeline to feed instructions to the processor fast enough to keep it busy. The memory bandwidth of the system is faster than the current processor needs, which indicates that IBM will probably upgrade the RT architecture with faster processors.

State-of-the-art 150-ns memory chips, interleaved banks of memory, and the high-speed bus make it unnecessary for the RT PC architecture to use cache, according to G. Glenn Henry, IBM Fellow and manager of hardware and software system development for the RT PC at the company's Engineering Systems Products division in Austin, Texas. Eliminating the cache lowers the cost of making the machine.

TAGGED MEMORY REFERENCES

IBM developed a system of tagged memory references to eliminate the need for cache. Each memory reference gets an identification tag from the 32 available. This means that the request for data can be separated from the response, which in turn means that requests and responses can be all mixed up. The memory subsytem does not have to hold back new requests until the current request is filled. This is yet another way to speed up the input and output between memory and the processor.

When the data is ready to be delivered in response to a request, it carries the tag to tell the MMU its destination by matching the tag to the tagged request. Any piece of data can be transmitted as soon as it is ready.



1. RISC PAIR. Two VLSI chips form the core of the RT PC processor board—the reduced-instruction-set ROMP processor and the memory-management unit storage controller.

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

As good as the ROMP processor is, it is the MMU that is the most important part of the RT PC architecture, maintains Henry. The very fast ROMP needs a good MMU to realize its potential. The RT PC's MMU produces 40-bit virtual addresses and fast address translations.

A new technology, called an inverted page table, was developed for the RT PC's MMU. In typical or classical virtual memory systems, there is a page table for translating virtual addresses to real-memory addresses. For every virtual page, there is one entry in the page table, which points to the page in real memory. The problem with this scheme is that the page-table size can get very large and eat up a lot of main memory when a large virtual address space is required.

The inverted page table of the RT PC architecture can handle very large virtual addresses—40 bits—without consuming a large portion of main memory for the table. Inverting the page table means that it contains only one entry for each page of real memory instead of pointers for every page in virtual memory. Therefore it never has to be bigger than the number of pages in real memory, even for very large virtual addresses.

When a virtual address is issued in a request to memory, a search must be made of the page table, called the translation look-aside buffer (TLB). But because the virtual addresses are not in order, a search cannot be made on this basis. Instead, an associative table lookup is performed. This is a hardware parallel search of the TLB to find the real address that is paired with the virtual address in the request. The full TLB is located on the MMU chip, but a fast subset of the TLB is placed on the processor chip so address lookup can keep up with the processor's need for instructions and data. This subset holds only those virtual addresses that are currently in use, were most recently used, and are most likely to be used in the near future.

Periodic reloading of the subset TLB is necessary during system operation to keep it up to date. The IBM System 38 (which Henry designed) had the first inverted page table ever devised; this one was reloaded by software. The RT PC has hardware to reload the TLB. The end result is very fast memory-access times, which lessen the bottleneck between the processor and memory.

The RT PC was developed from the start as an integrated system with hardware and software designed together. Initially, one of the key goals was to include a derivative of the single-level store concept, like that of the earlier IBM System 38 architecture. A single-level store means that all objects (programs and data) are accessed through a single level of virtual addressing. For this to be effective, virtual addresses must be very large. However, Henry and his team of RT PC designers decided that the machine did not need the full 48-bit-address single-level-store of the System 38. A 40-bit virtual address was deemed enough.

A single-level store treats virtual memory differently than do most virtual memory schemes. In the single-level store system, programs and data are never moved from files into virtual memory. Programs and blocks of data are given unique virtual addresses so that they are stored in virtual memory and paged directly into real memory as needed. Reads and writes are the same as loads and stores. Such a single-level store system needs more than 32 bits of addressing to give unique virtual addresses to all the active programs and data the system might have.

The 40-bit address of the RT PC system provides enough address space (2 terabytes) for all active objects. The virtual memory is structured as 4,096 segments of 256 megabytes each. Each object can get up to 16 segments (4 gigabytes) of virtual memory. The payoff of the big 40-bit address comes from high system throughput for programs that require multitasking, lots of files, and plenty of I/O.

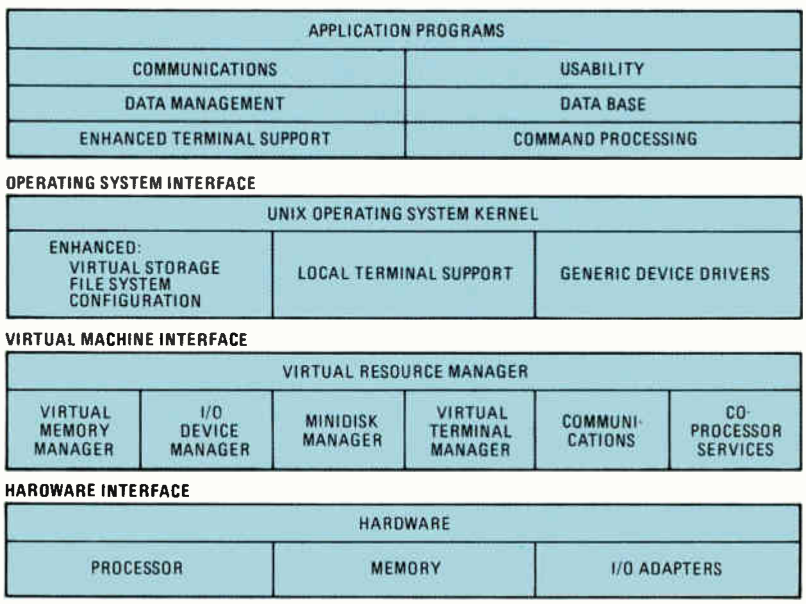
This project was different from most IBM development projects because it did not have a product with an established customer base to worry about. In fact, the project started not as a product development but as a technology project to design an advanced-function work station. At that time, Apollo Computer had just announced its first Domain work station and network system. Sun Microsystems Inc., which today is another major work station vendor, did not yet exist.

Because the original RT PC project was a joint microprocessor program with IBM Research and not driven by market and product constraints, the design team was able to stress technology and apply invention. The goal in the early days of the project was to incorporate what technical professionals would want in a work station—in effect, what the engineers on this project wanted in a work station. Only after the prototype was completed did project development begin.

SOMETHING OLD, SOMETHING NEW

Yet the RT PC is not all new. "We applied newness and invention where it would have high value to the user," says Henry. "And we also adhered to the dictum, 'if it ain't broke, don't fix it,' so we used some old stuff and some borrowed stuff." Some of the old stuff was standard vendor memory (150-ns 256-K dynamic random-access memories) and the IBM Personal Computer's I/O bus and adapters. Something borrowed was the Unix operating system (AT&T Bell Laboratories' System V), but with many enhancements.

"The RT PC is a more of an open system than even the open IBM PC for two out of three groups of people. For makers of add-on hardware, the system is more open than the PC because the bus interfaces are more modular and much better documented. And for third-party software vendors, it is more open than the PC because AIX [Advanced Interactive Executive, IBM's version of Unix System V for the RT PC] is more modular than PC DOS," says Henry. For example, device-driver



2. LAYERED. The RT PC's four functional layers make it easy for users to customize above the virtual machine interface and for IBM to make transparent changes below the interface.

ROMP PROCESSOR INSTRUCTIONS	
Instruction class	Number of instructions
Memory access	17
Address computation	8
Branch and jump	16
Traps	3
Moves and inserts	13
Arithmetic	21
Logical	16
Shift	15
System control	7
Input and output	2
Total	118

codes are separate, and new ones can be added easily.

But for the third group of people—the clone builders—the RT PC system is not as open as the PC. The base system unit is proprietary to IBM, and other vendors cannot buy the two chips—the RISC microprocessor and the MMU. The two chips are documented well for builders of add-on devices and software, but the clone builders are shut out.

IBM believes that add-on software products will drive the RT PC market and is strongly encouraging software developers. "The RT is easy to do applications for," Henry says. "Unix applications are easy to port."

The development team's toughest decision was whether to use Unix, according to Henry. But once the decision was made to go with Unix, the designers had to decide how to get a version that would run on and take advantage of the RT PC architecture. They decided not to do a standard adaptation of Unix to new hardware—rewriting the kernel to interface with the machine—mainly because they decided the Unix kernel did not have many of the features that the RT PC architecture was designed to provide. It did not have real-time support, which was needed to handle fast I/O devices and networking efficiently. It did not have a provision for the 40-bit virtual-memory addressing that they wanted the machine to support. Nor did the kernel support multitasking well enough for the variety of user-interface peripherals the designers wanted the machine to have—such as multiple displays, a mouse, and sound capability.

To fine-tune Unix to meet the goals of the RT PC project, IBM developed a virtual resource manager (VRM), a piece of software to control the real hardware of the machine (Fig. 2). VRM sits between the Unix kernel and the hardware and isolates the operating system from the hardware by presenting a virtual machine interface to Unix and other possible future operating systems. The RT PC's VRM provides what the Unix kernel lacks: real-time I/O, 40-bit virtual memory, and rich and efficient multitasking.

The VRM interface is exposed, open to all, carefully designed, and well documented. This means that RT PC original-equipment manufacturers and large end users can buy the RT PC with only VRM and not AIX. Because there is no read-only-memory-resident basic I/O system for the machine, these users get raw hardware plus a powerful virtual-machine control program. "A user can do what he wants with it," says Henry. Users could put any operating system on top of VRM or even develop their own operating systems. Yet users who buy AIX get VRM bundled in, and they do not have to know the details of how VRM and the bare machine work. They need only write or adapt Unix programs. "We did the same kind of VRM interface in the System 38, but did it better here," says Henry.

The IBM Austin team also added a whole gamut of other extensions to Unix. These came from this group's very early work on Unix—they were working with Unix from the start of the research part of the project. "We decided to take it [Unix] for its strengths and fix the 18 or so deficiencies. Yet the result is still compatible with the industry-standard System V," says Henry. "We think we have some good solutions to enhancing Unix and hope others will use them. And where other people have better solutions, we use them."

There are two sets of compilers right now for the RT PC: those shipped with Release 1 and the advanced PL.8 compiler technology inside IBM that is not yet designated a product. Initially, IBM is shipping the Unix compilers from AT&T with some optimization at the back end. The PL.8 compiler system was developed over several years at the Thomas J. Watson Research Center, and it incorporates the primary theoretical advances in compiler design of the past decade. "It is the best compiler ever written and the best thing that [IBM] Research has done," says Henry. "Not a lot of work had to be done on PL.8 to have it generate good code for the RT PC."

John Cocke and Fran Allen at the Watson Research Center developed a procedure of data-flow analysis—a technique for analyzing the interval of execution over which a variable is used, and using that information to produce more efficient code and to assign variables to registers. For the RT PC, the compiler's scheduling algorithms use the results of the data-flow analysis to take advantage of the ROMP's architecture, for example, by using the pipelining as efficiently as possible. The PL.8 compiler can also intersperse memory references and register-to-register operations to save time, because only the load and store instructions reference memory—the register-to-register operations can overlap the memory references. In addition, the compiler uses the branch with execute instruction, which allows the execution of an instruction following the branch while the branch target instruction is being fetched. □

VETERAN POINT MAN RUNS RT PC TEAM

To manage the development of its RT Personal Computer, IBM Corp. called upon G. Glenn Henry, one of its veteran computer designers and research-and-development managers, who has been involved in the design and management of big computer-system development projects ever since he joined IBM in 1967 in San Jose, Calif. Among others, he worked on the IBM 1800, IBM System/3, System/32, and System/38. He was responsible for many of the architectural innovations in the ground-breaking System/38 and received an IBM corporate award for this work in 1982.

Now Henry is the manager of Hardware and Software System Development at IBM's independent business unit in Austin, Texas, known as Engineering Systems Products. Henry directed a team of hardware and software designers there to create the RT PC. The project also involved coordinating the work being done by hardware and software researchers at the company's Thomas J. Watson Research Center in Yorktown Heights, N. Y., and integrated-circuit designers and process engineers at the IBM General Technology Division in Essex Junction, Vt.

HENRY: Headed the team that designed IBM's RISC work station.

A 1967 graduate of the California State University at Hayward with an MS in mathematics, Henry has recently been awarded an IBM Fellowship.

After years of keeping quiet about the work, Henry now says, "We believe we have achieved a real technical leadership position on this project [the RT PC], and we are glad to finally be able to talk about it." □

A NEW TOOL LAYS OUT COMPLEX ASIC DESIGNS FAST

NOW MACRO AND STANDARD CELLS CAN BE COMBINED AUTOMATICALLY

The name of the game for designers of application-specific integrated circuits is turning out their increasingly complex designs faster and faster, while they pack in circuitry as densely as possible on the silicon surface. One way to get such complexity is to mix standard cells and macrocells on the same chip. But up to now, laying out this mix and then routing the combination has been a slow and cumbersome task. Most of the software tools available for placing and routing require the designer to intervene manually in order to place macrocells within a standard-cell array. And most routers use a grid system that often wastes silicon real estate.

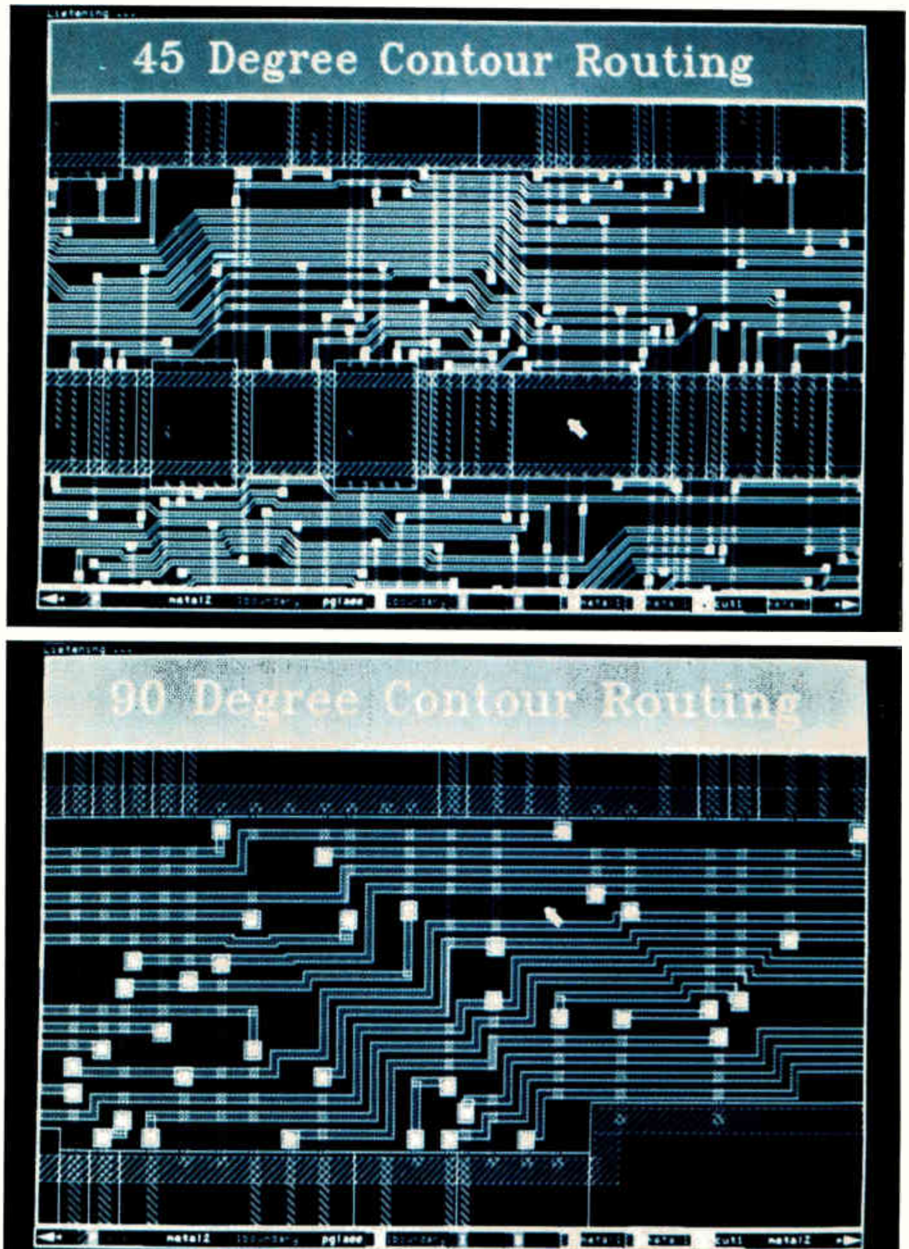
Now relief is on the way. SDA Systems Inc. has come out with MacroEdge, a layout tool that not only automatically places and routes standard cells but also performs interactive placement and fully automatic routing of mixed macrocell and standard-cell arrays. In addition, its routing method improves chip density.

Up to now, the only software tools that could automatically lay out standard cells and macrocells together were experimental developments at the University of California at Berkeley. The Berkeley tools, utilizing an algorithm based on a concept called simulated annealing, are computer-intensive and very slow. In fact, using the simulated-annealing algorithm as a benchmark, MacroEdge runs 20 times faster, the company claims.

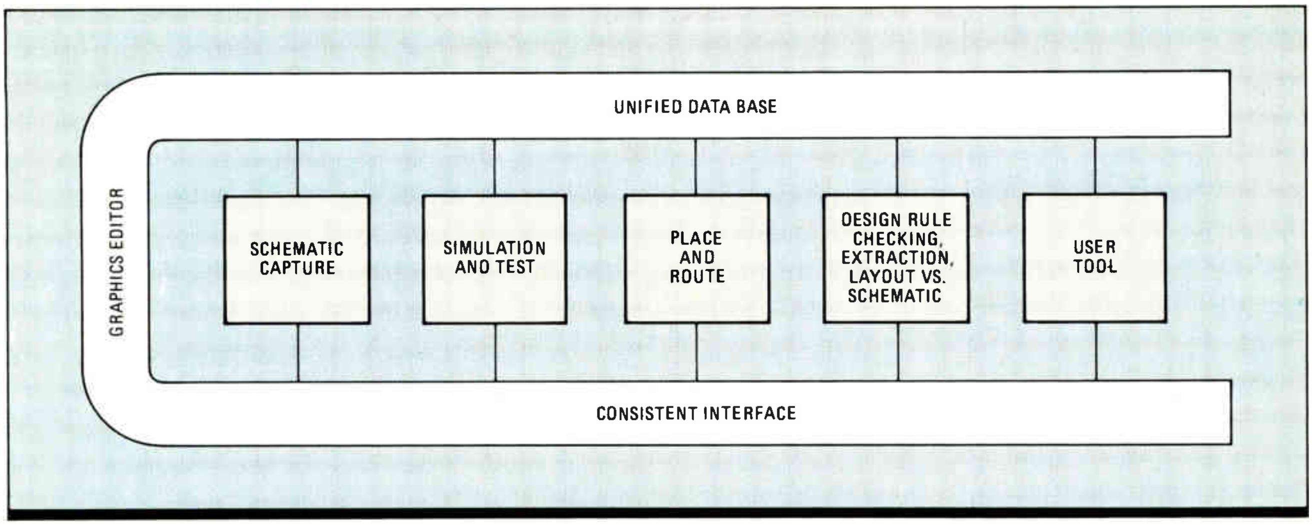
One way the MacroEdge channel router improves density is that it doesn't need a fixed amount of space between traces. Traditional routers are based on a grid that does requires fixed spaces. And they can lay out only straight lines and 90° angles, where SDA Systems' channel router can route straight, 90°, and 45° channels for maximum flexibility and efficiency (Fig. 1). The upshot is ASICs that are 20% to 30% denser than those routed conventionally, the company says.

MacroEdge, which runs on a work station, is designed to fit into the typical set of design tools used by designers in dedicated ASIC foundries, captive foundries in systems companies, and merchant semiconductor manufacturers in the ASIC market (Fig. 2). "In the past, there have been only one or two automatic programs to perform placement and routing of standard cells, without macroblocks, that have been commercially interesting," says James Solomon, founder and president of the Santa Clara, Calif., company. "There have been no commercially available automatic programs to place and route standard cells with macroblocks added."

A standard cell is a predefined circuit element containing combinations of logic gates, flip-flops, shift registers, counters, or input/output circuits. Usually rectangular, the cells are interconnected by the designer using an interactive computer-aided design system. On an ASIC, the cells must be laid



1. HIGH STYLE. MacroEdge's 45° (a) and 90°(b) contour-routing capabilities and variable spacing between traces in the channel contribute to a 20% to 30% improvement in ASIC gate density.



2. FRAMEWORK. SDA Systems' MacroEdge layout tool lies at the center of an advanced set of design software aimed at dedicated foundries turning out application-specific integrated circuits. It also will run with other companies' design tools.

out in a row, so that two sides abut adjacent standard cells and two sides must have I/O connections for routing.

By contrast, a macrocell can have larger amounts of logic or functional blocks. It can even contain other macrocells: for example, a microprocessor, read-only memory, random-access memory, and a programmable logic array can in turn make up a single-board computer macrocell. These macroblocks can be any rectilinear shape—such as L- or T-shaped—and can have I/O pins on all sides, which substantially increases the number of routing possibilities.

To handle this complex situation, MacroEdge uses a clustered-placement algorithm that partitions the design into clusters, then arranges them for optimum placement. It breaks the initial clusters into smaller ones and repeats the process until the chip is routed. "We've attempted to build a placement algorithm that mimics the way a designer manually lays out a design on silicon. It is very area-efficient," explains Larry Rosenberg, group director of research and development at SDA Systems.

SPEEDY BENCHMARK

The algorithm not only executes 20 times faster than the placement algorithm under development at Berkeley, but the density of its standard cells is nearly equal. SDA Systems' cluster algorithm has a further advantage in that there is a linear relationship between design size and placement time: if the number of elements to be placed doubles, run time doubles as well. On other algorithms, the relationship between the number of gates and placement time is nonlinear: placement time increases substantially more.

The advanced placement algorithms being developed at Berkeley are based on a fundamental model in physics called simulated annealing, which describes the way a crystal cools. During cooling, the crystal's randomly moving molecules tend to settle into a position determined by the force applied to it in the crystal. Molecules are analogous to macroblocks in a macrocell array. The designer can bias the placement of blocks in an array to minimize wire lengths, which will maximize the speed of a macrocell chip. One difficulty with the simulated-annealing algorithm is that it is a very computer-intensive algorithm. One placement can take tens of hours of a large minicomputer's time.

In last year's benchmark test comparing Berkeley's simulated-annealing software with the SDA Systems placement tool and simulated annealing, the chip had 2,400 cells. It consisted of mostly standard cells, but with two embedded macroblocks. "The conventional wisdom three or four years ago was that automatic place and route of such a chip was not possible," says Rosenberg. "A year ago, it would have required a mainframe. Now it is being done on a work station."

SDA Systems' algorithm was considerably faster than simulated annealing—doing the job in 5 hours as opposed to 120. With the latest work stations based on Motorola MC68020 microprocessors, the MacroEdge algorithm will run one half to one third faster than in last year's test.

In a typical complex ASIC, the mix of standard cells and macrocells can vary over a wide range. "From 2 to 12 macrocells can be placed among a larger number of standard cells," says Solomon. "It is hard to put a limit on how many macrocells can be accommodated," he goes on. "The area in some of the chips containing standard and macrocells is two-thirds macroblocks and one-third standard cells." In general, for a chip where macrocells contain other macrocells, the software handles up to 500,000 transistors. It accommodates up to 1 million transistors if the designer uses a macrocell with embedded macrocells. That number is impossible using only standard cells.

Designers tend to follow no fixed pattern in adding macrocells to a standard-cell array, resulting in irregular channel terminations. MacroEdge has three routers—global, channel, and stub. The global router analyzes the chip's topology to determine where interconnections should go. Then it divides the chip into vertical and horizontal routing regions to minimize constraints and maximize the area available for routing. Any area not covered by I/O pads and macroblocks becomes a routing channel.

A VERSATILE ROUTER

The channel router can route any rectilinear macroblock, such as a ROM, RAM, or PLA, and automatically routes blocks that have pins on any or all sides. It can route around blocks protruding into the channel, thus conserving silicon area. MacroEdge's channel router works equally well whether the material is polysilicon, single-layer metal, or double-layer metal. The tracing jogs around bonding pads using the spaces between the pads. By changing directions or jogging on a single layer, the channel router minimizes the use of vias or contacts. To perform routing this complex, it has three routing styles—straight, 90°, and 45°—for maximum flexibility.

In straight routing, the least efficient of the three, the wire traces are straight and do not bend around obstacles or vias in the channel. Among the design applications for this routing style is the laying out of gallium arsenide chips, which cannot accommodate angles in the routing layout.

A 90° router follows the channel contour by making right angles when going around protruding cells, macroblocks, and vias. The 45° contour router uses 45° angles to minimize wire lengths and area.

Finally, the channel router accommodates a trace capability called over-the-cell routing. ASICs enable internal pins to be defined inside the cell. With over-the-cell routing, an internal pin in one cell can be linked with the internal pin of another cell, with the connecting trace that goes over a cell located between the two. Moreover, because the trace is going over a cell, it does not use space in the routing channel. In competing tools, over-the-cell routing requires manual intervention from the designer. In MacroEdge, it is automatic.

The third router is a stub router, a simple straight-line router that makes short-range connections between adjacent cells. With this router, an internal pin in one cell can be connected to the internal pin of an adjacent cell without running a trace into the routing channel.

"Another reason the design is so area-efficient is that there is no extra space," Rosenberg says of MacroEdge. "Competitive systems have manual compaction. In these, once routing is complete, the designer must manually squeeze the channel down to get more space." The problem is not critical when a chip has a small number of macrocells. But with 20 to 30 macrocells, the designer must deal with the effect of compaction on the part of the chip already placed and routed.

To turn MacroEdge into a fully automatic macrocell placement tool, SDA Systems offers a package called Force Directed Placement that places blocks based on their connectivity to the I/O frame. It helps the designer spread the block apart to provide a first attempt at placement. Thereafter, the designer uses interactive graphics tools to place the blocks to minimize silicon area. The company expects to offer fully automatic placement of macrocells in a later version of MacroEdge.

In laying out macrocells, the automatic place and route software has a jigsaw puzzle to solve. It has to take into account not only the relative placement of the cells but also such factors as aspect ratios and orientations. The next generation of software will address this need to optimally place irregularly shaped macrocells.

"A future version of place and route software will be aimed at automatic fast turnaround of ASIC chips," says Solomon. "This is the version of place and route where the designer pushes a button and the chip is automatically placed and routed with little or no interactive placement."

Another improvement the company plans to make in the near future is the addition of floor planning, an intelligent tool for optimizing the way functional blocks are laid out on a chip to make the data flow more efficient. The designer can use the tool to work out timing and area constraints. For example, if the design has a large block, such as a PLA or a RAM, on a critical path in the horizontal direction and not in the vertical direction, the designer could want to change the shape of the block to fit the horizontal orientation. □

EX-CHIPMAKER TURNS TO MAKING TOOLS

SDA Systems Inc. began life out of a need at National Semiconductor Corp. for design tools to help develop future-generation very large-scale integrated circuits. "Design times were getting longer and the number of revisions was increasing," says James Solomon, SDA Systems' founder and president. At the time, he was manager of the MOS analog group at National. "We decided that there would have to be a new design methodology and tools to go along with the method."

National decided to spin off a company to create the tools. At first, Solomon's task was to help raise the capital to get the new venture going. It was his idea to get outside companies to finance the startup.

With $1 million in seed money from National, Solomon got Harris and GE Semiconductor to chip in $1.5 million each to fund the company initially. National added $1.5 million to its original commitment and, a short time later, LM Ericsson anted up $1.5 million.

A second round of financing brought $4.5 million from the venture community. More recently, the corporate partners and venture capitalists gave $8.3 million to the enterprise, bringing the Santa Clara, Calif., company's total funding to nearly $20 million [*Electronics*, April 21, 1986, p. 22].

After unsuccessfully trying to find someone to lead the company, Solomon wound up taking the job himself. "I kept thinking that the company needed someone to champion its cause at the beginning. My sense was you could not hire that kind of person."

Solomon, a personable, energetic man in his late 40s, was suited to the task. At National, he was responsible for developing several major product lines, including signal processing, data acquisition, and telecommunications. His fund-raising skills and business background match his technical acumen. He holds 23 patents in various electronics areas. A graduate of the University of California at Berkeley with bachelor's and master's degrees in electrical engineering, he is also an IEEE Fellow.


JAMES SOLOMON: Building tools for a new design methodology.

Evaluating the business prospects for the new venture, Solomon realized that the company could not simply build tools for the merchant semiconductor manufacturers. The market was too small.

At the time the company was formed, application-specific integrated circuits had just begun to hit the semiconductor market, Solomon recalls. "There was a belief in the business that by 1990 ASICs would account for 50% of the total semiconductor business." Because the design styles used for complex VLSI is similar to that for ASICs, the company focused on building products for both.

He set out to put together a research and development team, collecting the best people he could find. One such find is Larry Rosenberg, who had more to do with SDA Systems initially than even he realized. His contribution started with a paper he wrote three years before SDA Systems was even conceived.

"Larry had written a fundamental paper on a computer-aided engineering data base," Solomon says. "It had influenced UC Berkeley professor Richard Newton, who before SDA was formed had been involved with National and others in the development of the EDIF [electronic design interchange format] and later with SDA when we set out to design our own CAE data base called Framework."

Says Rosenberg, "My remark when I first saw the SDA product was 'It's a CAE designer's dream.'" Rosenberg joined SDA Systems after 15 years at RCA Corp., where he had headed one of the company's design automation groups, working on various aspects of design automation, including physical layout, simulation, and test. Rosenberg is now group director of R&D at SDA, responsible for the direction of three groups—data base and graphics, physical design verification, and automatic place and route.

PROBING THE NEWS

A THREE-WAY TUG OF WAR HITS THE 32-BIT MICRO BUSINESS

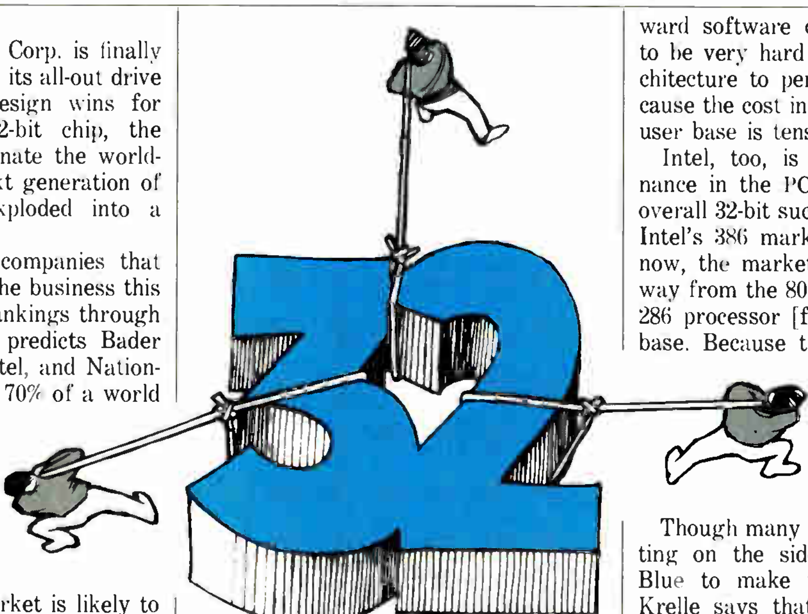
INTEL'S ENTRY INTENSIFIES THE MARKET'S POSITIONING PHASE

by Alexander Wolfe

NEW YORK

Now that Intel Corp. is finally up to speed in its all-out drive to capture design wins for the 80386 32-bit chip, the fight to dominate the worldwide market for the next generation of microprocessors has exploded into a three-way tug of war.

And the three U.S. companies that will end up dominating the business this year should hold their rankings through the end of the decade, predicts Bader Associates. Motorola, Intel, and National are expected to share 70% of a world market for the microprocessors that is forecast to soar to $215 million in 1990, according to the Mountain View, Calif., market researcher. The remaining 30% of the 32-bit market is likely to be shared by about nine others. AT&T and Zilog may edge closest to the big three, while other likely finishers will probably include Fairchild Semiconductor, Inmos, and such Japanese companies as Fujitsu, Matsushita Electrical Industrial, NEC, Oki, and Toshiba.



"The next year and a half is going to be pretty intense; the market is probably going to be in a positioning phase for 15, 18 months," expects Mel Thomsen, senior industry analyst at Dataquest Inc., San Jose, Calif. During this period, he predicts, chip makers will try to capture design wins and work on improving their manufacturing die yields.

This year the market for 32-bit microprocessor chips will hit $36 million, Dataquest estimates. But when peripherals such as memory-management units and arithmetic coprocessors are added, that figure quadruples. Motorola Inc., whose semiconductor operations are based in Phoenix, Ariz., was out front with a 60% share last year and will lead again in 1986 with 57%, Dataquest predicts.

National Semiconductor Corp., Santa Clara, Calif., was No. 2 last year with a 30% market share. But it "has lost steam and will drop to a market share of 10%" in 1986, forecasts Dataquest researcher Janet Oncel. Intel Corp., also based in Santa Clara, was not in the market last year for all practical purposes because its 32-bit entry was available only in sample quantities. But this year, Intel will surge past National to capture 30% of the market, Oncel predicts. The rest of the competitors, she says, will share the 3% remainder.

Because it buys so many microprocessors, the personal computer industry will play an important role in the 32-bit race. That's good news for Intel. Its 80386, introduced last October, succeeds the company's 16-bit 80286, which rules the world of IBM Corp. Personal Computer AT and AT-compatible machines.

In fact, one key observer thinks the 386 is strong enough to push Intel over the top. "I think everybody gets a share someplace, but in terms of sheer volume I think the 386 is going to dominate," predicts Ben Rosen, the venture capitalist who is also chairman of Compaq Computer Corp., the leading maker of PC-compatible microcomputers. "In the business-personal-computer market, the 386 is going to dominate because of the upward software compatibility. It's going to be very hard for an incompatible architecture to penetrate this market, because the cost in applications held by the user base is tens of billions of dollars."

Intel, too, is betting that its dominance in the PC AT arena will lead to overall 32-bit success. Says Dana Krelle, Intel's 386 marketing manager, "Right now, the market is moving in a major way from the 8086 and the 8088 into the 286 processor [for the] mainstream PC base. Because the 386 can run all the code from the 86, 88, and 286 unchanged, it's a pretty obvious upgrade potential from those earlier machines."

Though many industry players are sitting on the sidelines waiting for Big Blue to make the first move, Intel's Krelle says that it's possible the first 386-based personal computer may come from another computer house. "When people moved from the 86 to the next generation, [they] were really unsure of where IBM Corp. was going to go and what they were going to do as far as compatibility was concerned. And then the AT came out on the 286. This time around, the target for what the machine has to be able to run is pretty clear," she maintains.

Hitting that software bull's-eye means the ability to run programs written for the 8088 and the 80286, says Krelle. "So because the target this time around appears to be very clear, we find a lot of people being quite aggressive in what they want to do." That's why a clone may be first.

WHO'S ON FIRST? Intel positions the 386 as a blue-chip microprocessor—"right at the high end," says Krelle. In fact, Intel claims that its chip is the fastest of those offered by the three market leaders. Not so, maintains Motorola's Dean Mosley, manager of technical communications for the M68000 family, who makes the same claim for his company's product. "The M68020 is by far the highest-performance 32-bit general-purpose microprocessor on the market," he says. John Ferrick, sales manager for National Semiconductor's 32000 series, is willing to give his colleagues an even break. "If you get everybody down from a technical level, all of us are in the same performance range. All it depends on [is] who chooses what cleverly constructed benchmark.

"National is taking a different approach to the market than our two major competitors," according to Ferrick. "We see Intel predominantly positioning themselves in the IBM-compatible arena. We see Motorola going in predominantly as an upgrade to the 68000-based designs. The products that competitors are bringing to market are basically major architectural changes to accommodate the movement to the 32-bit market," he says.

National chose instead what Ferrick calls "a true superminicomputer architecture"—as did Digital Equipment Corp. for its VAX machine—and implemented it at the microprocessor level. "We did not evolve from 4- to 8- to 16- to 32-bit micros," he says.

National says its strategy is to offer a broad range of products, and it groups 8- and 16-bit chips in the 32000 lineup. All the microprocessors in the series have 32-bit internal data buses, but their external bus widths vary. "Our customers are selecting from a range of processors that all have total software compatibility, instead of [from] a single offering," says Ferrick.

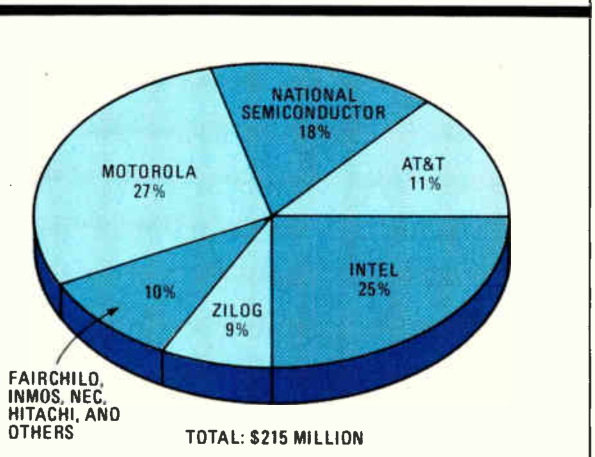
On tap for early 1987 is the 32532, National's top-of-the-line 32-bit chip. Its architecture features more pipelining for higher performance. The 32332, claims Ferris, uses about half the transistors of competing products. "In the 532, we're going to boost the transistor count, but the performance should probably outperform the market by a factor of 2 to 3 times," he says.

EARLY START. National introduced the 32032 in 1983, and the company has used its early start to secure design wins in the important parallel-processing arena. As a relatively new commercial technology, parallel machines constitute an important high-profile showcase for a 32-bit chip's capabilities. In parallel processing, National has already caught on with heavyweight players such as Encore, Flexible, Sequent, and Tolerant. "We feel [parallel processing] is probably the most exciting market right now, because it is a major alternative to the traditional minicomputer," says Ferrick. "It also tends to use large quantities of processors."

The second of the big three into the market, Motorola, introduced its main 32-bit entry, the 68020, in 1984 and built up its business by upgrading the already large base of 68000 users. The company claims to have captured 80% of the 32-bit-microprocessor market in 1985. "We have a long list of customers that have announced products for us at this point," says Mosley, "and we're happy to see that [the chip is] being designed in a wide variety of applications." The 68000 family as a whole has been particularly strong in applications for work stations and for machines running AT&T Co.'s Unix operating system, Mosley says.

The basic 68000 chip features 32-bit registers internally but uses a 16-bit external data bus and a 24-bit address bus. The 68010 is a virtual-memory machine. The high-end 68020, on the other hand, uses 32 bits internally and externally.

MOTOROLA WILL RANK FIRST IN 1990 32-BIT MARKET



SOURCE: BADER ASSOCIATES

Motorola is pegging part of the family's sales on the Unix connection. "In the past, the vast majority of Unix applications have been 68000-family-based products," says Mosley, and a second generation of software-support products for the 68000 series is just beginning to hit the market. Optimizing compilers designed to use the 68020's instruction cache more efficiently are due this year, he adds. Intel has also recently announced that additional compilers are on the way for the 80386.

Also, says Mosley, "we're trying to bring the 68020 down the learning curve, just like we did the 68000. When the 68000 came out in 1979, it was about $400, and now you can buy them for $15." That is typical of the learning curve that all the 32-bit chips are expected to follow.

A notable Motorola market niche is in controllers, those embedded processors used to control various factory and environmental functions such as robotics and numerical control. "Mitsubishi has shifted over to the 68020 for all of their numerical control functions as well as their robotics controllers," says Mosley. Currently, approximately 10% to 20% of 68000 series chips go into controllers. "But we see that growing dramatically, because as the price comes down, it's more cost-effective to use it as a controller."

The 68020 is well-suited to function as a controller, says Mosley, because of its on-chip instruction cache. This cache allows a small group of instructions to be loaded onto the chip and repetitively executed without fetching instructions from memory. This turns the chip into a fast, dedicated processor.

SCRAMBLE. Despite the domination by Intel, Motorola, and National, the 32-bit marketplace inevitably will lure new players. Not all of them will make money, but there are other compensations. "Some companies may be in the marketplace even though they're not making money at it, just to have a strategic presence," says Intel's Krelle. "I think there is some definite image value in having a 32-bit-processor offering on the market and I think a lot of people will try to get in the business for that."

The smaller players will likely go after market niches not served by the big three. For example, Zilog Inc., Campbell, Calif., is targeting military, graphics, and signal-processing applications, and "we plan to capture 30% of those markets," a company spokeswoman says. After several false starts since word of the product first leaked in February 1984, Zilog has been offering sampling quantities of its Z80,000 since January. The chip is expected to go into production in the fourth quarter of 1986.

AT&T, on the other hand, categorically rejects consignment to a niche. "Our objective is to be one of the top three vendors," says Al Hoffman, marketing manager for the company's 32-bit-chip line. Currently, that line contains the WE32100 microprocessor, also called the 32-bit Unix Microsystem in company literature. Production quantities of the chip became available late last year.

As the originator of that popular operating system, AT&T is aiming its chips strongly at Unix applications. A higher-performance WE32200 has also been announced and is due to be shipped in September.

"This is the year of [market] penetration," says Hoffman. "Last year was the year of establishing presence." Hoffman does not have figures on AT&T's current share of the 32-bit microprocessor market, but says that when captive sales are added in, AT&T tops the list of 32-bit vendors. □

CAN TOUCH-SCREEN TECHNOLOGY MOVE BEYOND SPECIAL USES?

LOWER PRICES COULD OPEN BROADER SPECTRUM OF APPLICATIONS

by Tobias Naegele

NEW YORK

The long wait to jump into the mainstream may be nearing an end for touch-screen technology as sharply lower prices fuel its drive into more applications. Touch long has been used mainly for military and process-control jobs, but a relatively recent surge in popularity has the companies that make the systems talking big about their minuscule market.

"We're seeing an explosion of applications," says Alan Hochman, marketing vice president at Carroll Touch Inc., a leading supplier based in Round Rock, Texas. "Many companies are either in development or test stages with touch-based products," he says, with "interactive video the fastest-growing market for touch in the last year or so. He lists such likely applications as coupon-dispensing machines in supermarkets, point-of-sale systems that act as computerized product listings in catalog and automobile showrooms, and public information systems in high-rise office buildings and amusement parks.

Office-automation products, such as the Xerox Corp. laser printer, are also likely applications, as are machine-control systems for automated factories. IBM Corp. used touch technology in a system called CAMS, for Computerized Automotive Maintenance System, which it developed for General Motors Corp.

"Machine control is a natural for touch because you can take someone who has very little experience or training and let them run a system," Hochman says. Another advantage, he says, is that "you can give the display different personalities—it can be a maintenance panel, operator panel, whatever." And Europe could emerge as the biggest market of all because of the popularity there of videotex, he adds.

And even in the old standby military and avionics area, Hochman says, "touch is becoming very hot right now. A touch screen takes up less space than all the switches it can replace, and doesn't have the kind of mechanical failure you have with switches." Carroll boasts that the mean time between failures is about 50,000 hours for its standard product line. "That's five years of continuous use without a breakdown," Hochman says.

The rosy picture was foreshadowed about 30 months ago as Hewlett-Packard Co. called attention to the technology when it offered touch as an option on its new HP 150 personal computer [*Electronics*, Oct. 6, 1983, p. 105]. That computer, with its proprietary architecture, is used mostly in systems built around the HP300 series of business computers. But now, HP has given touch a real vote of confidence by making it a $400 option on the Vectra, which it introduced last year and which presumably will find a much larger audience because it is compatible with the IBM Personal Computer AT.

But the bottom line is price, and prices for touch systems have been plummeting—for example, a 19-in. infrared touch screen that had a unit price of $2,500 in late 1984 can now be had for less than $900, says Carroll's Hochman. And as with any other emerging technology, rising interest and falling prices feed on each other. "With prices going down, it makes it possible for more and more applications to consider and utilize touch. Our systems now sell for 30% to 40% of what they did 18 months ago," he says.

A 12-in. capacitive-overlay system can be had in quantity from Microtouch Systems Inc. of Woburn, Mass., for $350. And in a paper to be delivered at the Society for Information Display Symposium in San Diego this week, Arthur Carroll, Carroll Touch's founder, writes that by 1987 and 1988, volume orders for some touch systems could drive prices to as little as $40 for low-end systems and $120 for high-end systems ruggedized for harsh environments.

MOVING FINGER. Used mostly for military and industrial-process applications, touch screens are poised to find a wider market.

Driving prices down, Hochman says, is the increased use of microprocessors. Carroll's newest product line, called Smart-Frame, eliminates the need for a separate controller card by building intelligent controllers directly onto the opto-matrix frame. "When we brought out our Smart-Frame, we reduced the parts content by 45%," he says. "That not only made it cheaper, but reliability went way up, too." And at Microtouch, Logan says prices should drop this autumn when the company substitutes integrated circuits for the discrete components in its controller.

But it is difficult to judge the potential accurately. As Hochman explains, "It's such a new and small market that nobody really knows how big it can get." However, International Resource Development Inc., a Norwalk, Conn., researcher, estimates the market was worth about $20 million in 1984 and $27 million in 1985, will reach $35 million this year, and will at least double by 1987.

IR APPROACH. Whatever the potential market, several approaches are competing for it. Most companies, including Carroll, use an IR technique that superimposes an invisible light matrix over a conventional display. In one application, the computer offers a menu to the user, who touches the desired point on the screen. That breaks the IR light beams, thereby indicating the user's response.

Another method uses overlays, usually of glass, that rely on current or capacitive changes caused by the application of pressure to their surfaces. Still another system, being explored by Zenith Electronics Corp., uses surface acoustic waves pulsing back and forth on a screen's surface. Touched, their amplitude drops; the timing and depth of the drop indicates the location of the touch (see "Several techniques chase infrared scanning," p. 43).

Carroll's leading competitor, Elographics Inc. of Oak Ridge, Tenn., relies on overlay technologies, as does Microtouch Systems. Now, says Hochman, Carroll will make it three when it introduces its first overlay product in the next two months.

The major point of comparison among the various technologies is clarity. Assigning IR systems 100% clarity, Microtouch president James Logan rates his company's capacitive overlay at 87% to 90%. For Elographics, which uses a resistive overlay, the rating ranges from 50% to 85%, depending on who does the estimating. However, says marketing vice president Robert Highfill, "Our touch screen is more accurate because it responds to finger pressure, whereas with the IR system, it's finger shadow that invokes response."

Carroll, a subsidiary of Amp Inc., is widely acknowledged as the leading commercial supplier of touch technology, with its screens incorporated in systems built and marketed by the likes of AT&T, Honeywell, Kodak, and Xerox. Carroll is also a leading choice for military systems such as the Marine Integrated Fire and Air Support System, which has a touch-based system for coordinating battlefield strategy.

The company is growing fast, says Hochman, and although he won't say how big it is, he will say that Carroll recently doubled the size of its manufacturing facility. "We're hiring as fast as we can find personnel," he adds.

Microtouch's Logan says, "Right now, I'm quite confident that we are bringing in more new customers [who have never used touch before] than either Carroll or Elographics." He estimates that Carroll has 35% of the market, Elographics has 25% to 30%, and Microtouch is third with more than 10%.

The first touch systems were developed in 1961, but the first development work in IR screens came out of a need in the early 1970s for an input method that could be used easily by children. The University of Illinois at Urbana wanted to develop a reading and mathematics course using Plato, its computer-based instruction system, and keyboards were found to be impractical because few children can type.

Although touch technology was slow to catch on, companies such as Xerox built it into their commercial systems. For example, Xerox used the technology in its 5700 laser printer, and Tektronix Inc. built touch-input capability into some of its logic analyzers, says Hochman.

Perhaps the most successful use of touch technology so far has been at the Epcot Center at Disney World near Orlando, Fla. Arthur Carroll notes that the touch-based World Key Information System there went into operation in 1982, and allows visitors to get directions and other information, play educational games, and even make restaurant reservations in several languages.

Hochman is optimistic that the technology will catch on in the U. S. in consumer-oriented areas such as video games and personal computer software. "I think you'll see touch on the screen of your household computer as it becomes easier for the user to install, as the price falls, and as software becomes available," Hochman says.

That will open up what he calls a two-tiered market, where low-end products can be aimed at the benign office environment and high-end systems can serve the harsher factory and military markets. "We'll see low-end products that won't have the reliability of the military systems, but won't need it either," Hochman says. "That will allow prices to come down." □

SEVERAL TECHNIQUES CHASE INFRARED SCANNING

Competitors approach touch screens with a variety of different schemes. The dominant approach is called infrared scanning.

In this method, two edges of a display—either a cathode-ray tube or a flat panel—are lined with IR light-emitting diodes, while the opposite edges are lined with phototransistor detectors. This creates an IR beam matrix just above the screen's surface. When a finger breaks the light beams, the location is indicated.

The newest method, from Zenith Electronics Corp., uses ultrasonic surface acoustic waves to drive down the cost.

The approach gives each X and Y coordinate two transducers—one each for transmission and reception. On a typical 13-in. screen, the transmitter launches a 4- or 5-MHz pulse every 5 ms. These pulses are redirected back and forth across the screen's surface by reflector strips until they reach the receiving transducer. A touch causes an amplitude dip whose timing and depth indicate the touch location and the finger pressure. Touch pressure can be used as a third coordinate, offering greater accuracy on inputs.

The Zenith system is not yet in production, and project engineer James Fitzgibbon says he cannot speculate on the timing of future products, but he maintains it is a cheaper and more accurate solution to the touch problem. Parallax, which can be a problem with both overlay and IR systems, is eliminated, he says, because the sound waves can travel over a curved surface, such as a CRT. IR systems, on the other hand, must be raised above the display's edges so that the light beams can "see" over the apex of the curved CRT surface. Another advantage over the IR approach, he says, is that dust or bright light cannot interfere.

Resolution is very high as well, because "you only have to change the clocking rate of the electronics to change resolution," Fitzgibbon says. Unlike IR systems, which require the addition of more LEDs each time resolution is boosted, the actual construction of a surface-acoustic-wave system remains the same when resolution is improved. "Our demonstration system is running with 25 touch points per inch, and basically we know we can double that," Fitzgibbon says. "But for an LED system, for every touch position you have to add a diode and a receiver at each point. There is a point where you can't stack them any closer, and that can become a problem."

Still other techniques use a touch-sensitive material directly on the display surface. These approaches rely on conductive, resistive, or capacitive effects to gain their touch sensitivity.

In the conductive method, two layers of glass or some other transparent material are etched so each has an electrode grid. The two conductive layers are separated by a thin insulating layer, but when pressed together, the electrodes close a circuit indicating the X and Y coordinates of the touch location to the computer.

In the resistive technique, a sheet of glass is coated with a resistive material and mounted on a CRT. It is then covered by a conductive film, with a thin layer of air between. A voltage is applied to the glass substrate in both the X and Y directions, so that when the layers are pressed together the film returns two proportionate voltages that can be analyzed to determine the touch location.

Capacitive overlays have a thin layer of capacitive material coating a glass shield over the display. A conductive stylus, which changes the capacitance, is used. *—T. N.*

A BRUISED NASA HANGS IN WITH SPACE-FACTORY PROGRAM

MATERIALS MANUFACTURING, A FAVORITE OF INDUSTRY, MOVES AHEAD

by George Leopold

WASHINGTON

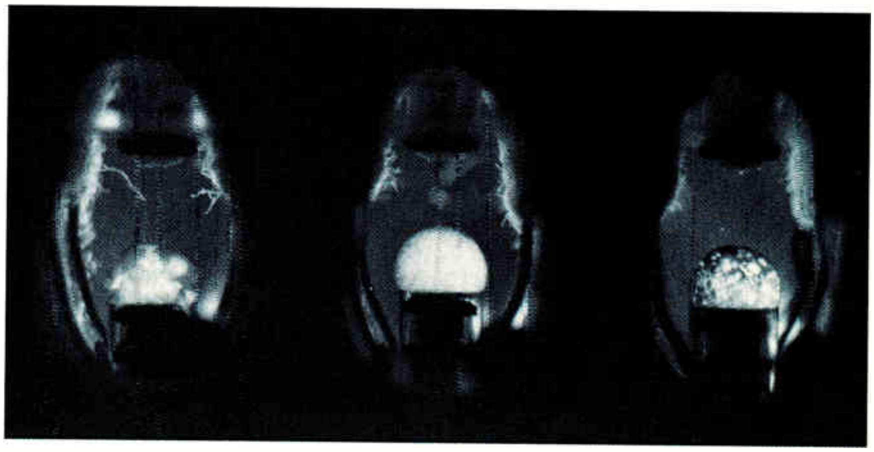
Despite the one-two punch of the Challenger tragedy and the subsequent wave of mismanagement charges, a battered National Aeronautics and Space Administration still has at least one program that has emerged unscathed. In fact, that effort—manufacturing in space—is actually gaining momentum. The program, which also encompasses ground-based experiments, takes advantage of the weightlessness of space to manufacture new, defect-free materials that may be used to fabricate tomorrow's semiconductors and electro-optical devices.

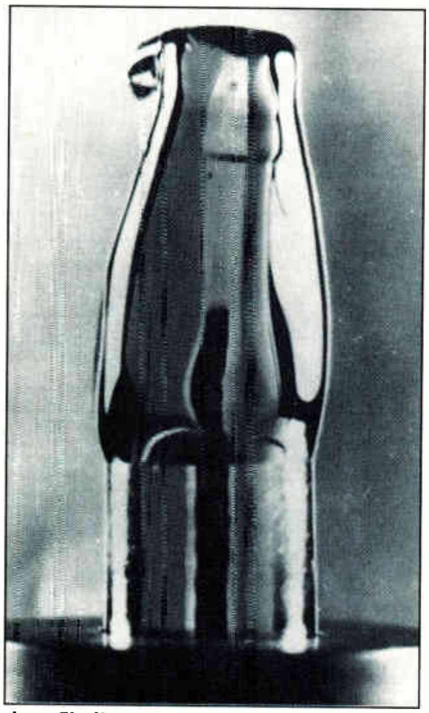
The reason for its luster at the space agency is that industry likes it. Not only does NASA "see a stronger and stronger interest on the part of corporate America in space" in general, says William Oran, chief of market development in NASA's Office of Commercial Programs, but space manufacturing is a favorite. Oran is convinced that the increasing number of companies approaching NASA about its new commercial centers will add to the program's momentum over the next five years.

Those centers are the key to NASA's expanded ground program. Created last year, they include a microgravity laboratory and five centers for space commercialization that focus on materials processing and crystal growth. The sites are designed to investigate the potential for developing materials and processes of commercial significance. NASA is initially funding them over five years at amounts ranging from $750,000 to $1.1 million on a year-to-year basis.

Even though the shuttles needed for the space portions of the experiments have been grounded, NASA's backing of the new centers means "there will be sustained interest [in space manufacturing] for the next five years," agrees Edward W. Collings, technical director of the materials science department at Battelle Columbus Laboratories' Center for the Commercial Development of Space. Battelle, in Columbus, Ohio, is one of five centers named by NASA last August. "Activity is intense," he notes.

The one fly in the ointment is the grounding of the shuttles in the wake of the Challenger loss, although NASA managers say that there is still plenty of work to do on the ground. One, Robert J. Naumann, a materials-processing and project scientist for the space station at the Marshall Space Flight Center in Huntsville, Ala., acknowledges the loss of an orbiter will hurt the space-manufacturing program. But then he points to a way the setback can focus effort on getting the most out of groundside work: the program lacks flight-qualified equipment—furnaces, for example—needed to optimize allotted flight time, and "this compels us to go back and do some hard rethinking." Naumann says NASA expects to have flightworthy furnaces ready to go once the flight schedule is resumed, though no one can say when that will be.





SPACED. Protein crystal, above, and flawless single crystal of extremely homogenous indium antimonide, left, were produced aboard Skylab as part of NASA's program.

From an engineering standpoint, NASA and industrial researchers are still working to overcome such problems as uncontrolled convection currents that result in uneven distribution of dopants in molten materials. But Naumann believes processing in space is the best way to solve these problems.

YIELDING TO MILITARY. Nevertheless, some researchers fear that pressures inside the government will force a chastened NASA to give military payloads top priority. They feel that a one-year interruption in shuttle flights—and with it, in-orbit experiments—will hamper the progress of their projects. "We are as close to production [in space] as we are to flying," says one university researcher working on commercial gallium arsenide crystal growth. "But we are not flying."

Adds Robert H. Doremus, a professor at the Rensselaer Polytechnic Institute whose fluoride glass levitation experiment was bumped along with a scheduled June shuttle flight, "You have to do the flight experiments to guide your ground work." NASA managers counter

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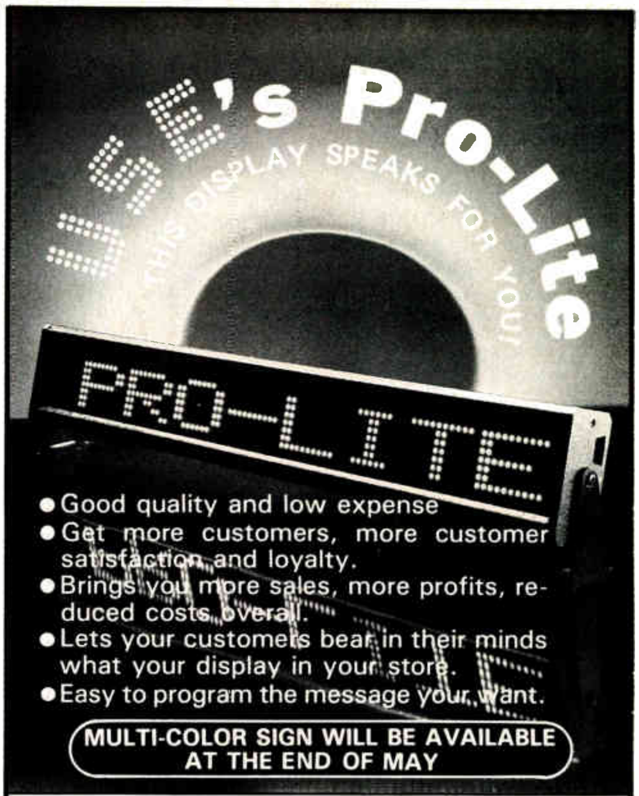

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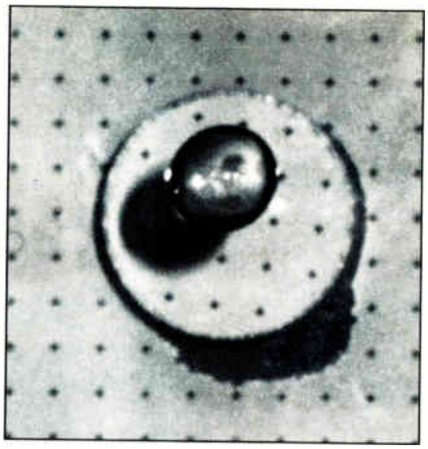
by saying there is still plenty of work to be done on the ground.

One way to do some space-like work is to go to Cleveland. There, at NASA's Lewis Research Center, the Microgravity Materials Science Laboratory that opened last September is offering university and industry researchers a low-cost, low-risk method of testing proposals for materials processing in space without leaving the earth. Along with such facilities as furnace systems and mockups of flight hardware, the lab also offers access to Lewis's two drop towers, which help achieve weightlessness for up to five seconds.

Thus far, only GTE Laboratories of Waltham, Mass., has used the microgravity lab to conduct GaAs crystal-growth experiments. Fred Kohl, chief of the NASA lab's materials-science branch, says the experiment, scheduled to fly on the shuttle at the end of 1986, remains in a "holding pattern."

But Kohl and Leslie Greenbauer-Seng, a microgravity lab manager, quickly point to the large store of ground-based work yet to be done. "We're at the front end of things," notes Greenbauer-Seng.

Those "things" started about 15 years



HANGUP. Drop is suspended in an experiment performed aboard Skylab 3.

ago. Since the early 1970s, NASA has been investigating several methods for processing low-defect semiconductor materials in space. Among the processes under investigation are crystal growth by chemical vapor transport, seeded containerless solidification of materials such as indium antimonide, and steady-state growth and segregation of indium antimonide. A vapor crystal-growth system that was designed for use on the shuttle has also been used to grow single crystals from vapor.

NASA has 37 existing or pending joint agreements with industrial partners for space manufacturing. Ken Taylor, office chief for Marshall's Commercialization of Processing in Space Group, says 13 joint agreements are in electronics and electro-optics. That number is surpassed only by the biological experiments.

One of most promising research areas is the production of purer GaAs in space. Microgravity Research Associates Inc., Coral Gables, Fla., entered a joint-endeavor agreement with NASA in 1983 to demonstrate the superiority of GaAs crystal material produced in space. Now it's developing process technology and hardware needed to grow GaAs in space from a seed crystal [*Electronics*, Jan. 26, 1984, p. 89].

USING MIT PROCESS. Microgravity Research is using a liquid-phase electroepitaxial growth process developed at the Massachusetts Institute of Technology's Electronic Materials Laboratory in Cambridge. According to Richard L. Randolph, the president of the company, GaAs crystals up to 5/8 in. in diameter have already been grown. "At these small dimensions, we're growing crystals routinely," says Randolph. To begin commercial production in space, however, the company must grow 3-in. crystals. Randolph says that portion of the work was scheduled to be performed two years from now, when a series of seven shuttle flights was to be launched. Thus, current delays have so far had a minimal impact on the project.

Harry C. Gatos, director of the MIT Electronics Materials Lab, is more anxious. "All of the technical problems [associated with] space manufacturing have been resolved," he says. "We look forward to achieving homogeneity not attainable on earth." Shifting the project to space won't improve the quality of crystal growth, Gatos explains, but will enable Microgravity Research to increase the size to that needed for commercial production. Devices ranging from radiation-hardened components to repeaters for trans-oceanic fiber-optic cable systems are possible, he says.

Another joint endeavor, between NASA and 3M Co., St. Paul, Minn., is designed to investigate the growth of organic crystals using two processes: diffusive mixing of organic solutions (DMOS) and physical vapor transport of organic solids (PVTOS). The most recent of two DMOS experiments flew on the shuttle last November and included four crystal-growth cells. Two were devoted to studying the ordering of molecules under near-ideal conditions, while the second pair examined the way crystals pack together and how this affects their electro-optical properties.

Christopher J. Podsiadly, director of 3M's Science Research Laboratory, says the most important result of the second DMOS experiment was the large amount of mixing that occurred under large density variations between chambers filled with dye solutions and others containing methanol and heptane. Initial study of the space-grown crystals has so far shown no difference with crystals grown on earth, however.

Commercial production of semiconductor material isn't imminent

The PVTOS experiment represents the first attempt to grow organic crystals in space by the vapor-transport method. It is also the initial experiment using specific substrates for crystal growth. Nine experimental cells each contained an organic solid that was vaporized to migrate through a buffer gas to a substrate consisting of a thin film deposited on a silicon wafer.

The experiment, which flew on the shuttle last August, produced thin-film layers at the angstrom level, Podsiadly reports. "What we got were varying depositions depending on the carrier gas." Two chambers also produced pinhole-free thin films previously impossible to grow on earth. 3M's goal is the fabrication of optical devices for applications such as image processing, but a 3M representative adds that such a device remains five to ten years away.

Podsiadly says polymeric systems will eventually be tested, and 3M has another thin-film payload ready to go once the shuttle flights resume. "We're anxious to get going again," he says, "because the results were so good." Still, no one expects actual commercial production of low-defect semiconductor materials to begin any time soon. Instead, NASA officials say they want to overcome engineering problems in order to demonstrate that superior materials can be processed in space. □

CAN INTERGRAPH CATCH IBM IN CAD/CAM MARKET?

ITS MARKET SHARE GROWS FROM 14% TO 17% IN THE PAST TWO YEARS; SOME SAY COMPANY COULD HIT IBM's 20% BY 1987

HUNTSVILLE, ALA.

When a group of engineers left IBM Corp. in 1969 to start up M&S Computing Inc., the possibility that someday they would end up challenging their former employer for the lead in a $4 billion market was probably the furthest thing from their minds.

That tiny startup, however, has quietly evolved into Intergraph Corp. (the name changed in 1980), the fastest-growing maker of turnkey interactive-graphics systems in the U. S. The company is now gaining share in the computer-aided design and manufacturing market at a pace that could soon make it IBM's equal.

Intergraph has expanded its share from 14% to 17% in the past two years and could reach IBM's 20% level by 1987, some industry analysts predict. With 1985 revenue totaling more than $526 million—up 30% from the $404 million achieved in 1984—Intergraph was the only company besides IBM to grow faster than the CAD/CAM market itself last year. Its growth rate so far in 1986 is running at 37%. This year the market should hit $5.2 billion, according to Dataquest Inc. And by 1990, the San Jose, Calif., market researcher predicts sales will total $11.5 billion.

Intergraph gets high marks from some industry experts for its heavy investment in applications software and in the use of Digital Equipment Corp. VAX minicomputers, which it customizes extensively for CAD/CAM uses. Other observers argue that the company emphasizes hardware at the expense of software, which they predict will soon become more important.

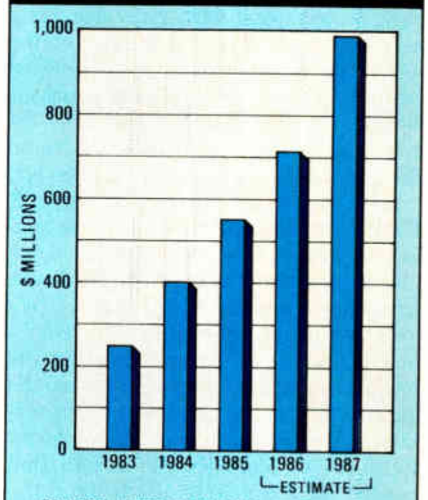
Much of Intergraph's success comes at the expense of such former leaders as Computervision, General Electric Co.'s Calma subsidiary, and Applicon [*Electronics*, April 14, 1986, p. 46]. CAD/CAM makers generally had a relatively dismal 1985 as the industry went through what Dataquest called a permanent market correction. Industrywide, revenue growth slowed to 22% from its historical annual rate of 35% to 40%. IBM grew 24%, to $870 million; Computervision slipped 21% to $441 million.

"What we want to provide is interactive solutions to engineering, corporate, and project-level problems," says Keith H. Schonrock, executive vice president. He attributes the company's success to its tight focus on interactive graphics and applications solutions along with its dedication to serving customer needs.

FIRM COMMITMENT. "Intergraph is firmly committed to not just being a workstation supplier, or a components supplier, or a software-package supplier," says Schonrock, who says the company wants to be known for doing well in all three categories. He founded the company along with president James W. Meadlock and executive vice president Nancy B. Meadlock.

Industry analysts agree that the commitment to customers has fueled the company's rise. "What Intergraph has that other companies don't have is a great awareness of what the customer means to them," says Peter D. Schleider, an analyst at L. F. Rothschild Unterberg Towbin Inc., New York. Nevertheless, he is among those who say that the company "focuses too much on hardware. That's a mistake."

FOR INTERGRAPH, BOTH REVENUE . . .

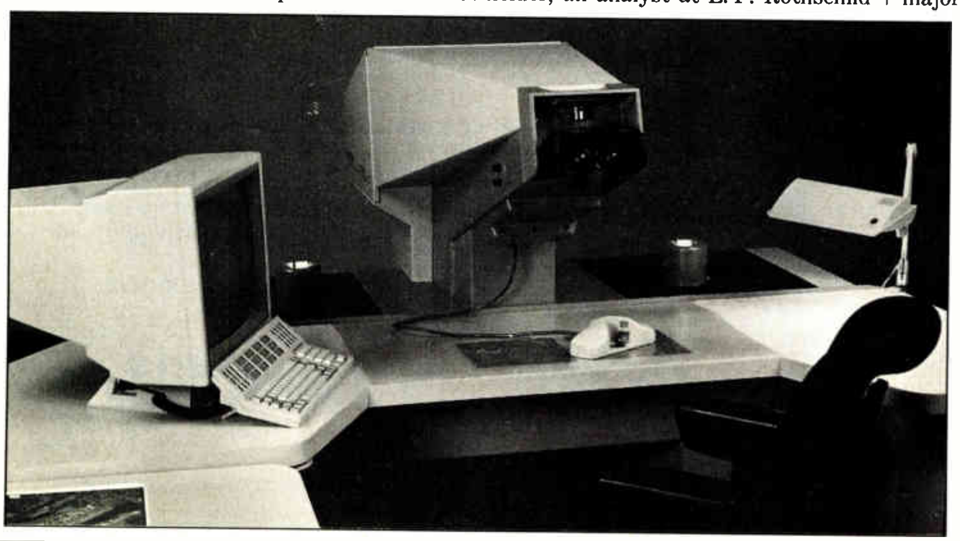


SOURCES: INTERGRAPH CORP., INDUSTRY SOURCES

Instead, he argues that makers of CAD/CAM systems should focus on software development. The emphasis on hardware is misguided, he says, because performance has become a secondary consideration for customers. Predictably, Intergraph executives disagree. "I don't think there's any less emphasis or interest in responsiveness," Schonrock says. "The need for responsiveness is what's pushing the [engineering] marketplace." Adds William D. Zarecor, executive vice president for product marketing, "You need to tailor your hardware to maximize the use of your software." As far as unbundling software, says Zarecor, "It's a pretty good way to go broke."

Intergraph first made its name by developing mapping systems for the government. It's still a major supplier to the Defense Department's Mapping Agency. Its strategy to expand into the major CAD/CAM market segments began in the mid-1970s. The company went on to garner nearly 33% of the architectural and engineering design market.

By 1983, it had expanded a line of mechanical-design and drafting packages first introduced in 1980, shipped its first electronic CAD systems for printed-circuit-board routing and layout, and entered the technical-publishing market. And working with Tangent Systems Corp., Santa Clara, Calif.—which helped develop the Unix-based Interpro 32 work station—Intergraph has moved into very-large-scale integrated-cir-



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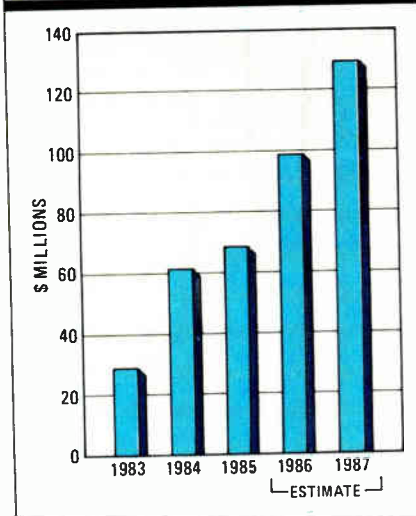

cuit and standard-cell design.

H. W. Barbour, executive manager for electronics marketing, says Intergraph is now beta testing software packages for such activities as logic-circuit simulation and schematic-design capture. Unlike other CAD/CAM players, Barbour argues, Intergraph is taking existing technology and leveraging it into a new market segment.

That strategy seems to be working. "We project Intergraph will snare fully 9% of the ECAD business by 1987," says Peter E. Heymann, of Drexel Burnham Lambert Inc., New York.

To attain its goals, the company recently bolstered and restructured its sales force. Marketing head Zarecor says the skyrocketing number of applications dictated the creation of a vertical sales force divided into three areas: mapping and energy exploration, mechanical design, and electronics and electronic publishing. The sales force alone has grown by one third since late 1985, and Intergraph is adding new employees at a net rate of 100 per month. The company employs 5,289 now versus 3,483 in November 1984.

CRITICAL ISSUE. Intergraph is also keeping its eye on the factory floor by endorsing the Manufacturing Automation Protocol (MAP), a communications protocol for factory-automation equipment championed by General Motors Corp. In addition, it is embarking on a network-development effort code-named Bed Rock. Intergraph considers network development to be a critical customer issue, says William Payne, executive manager for technical marketing. Indeed, doing more than merely paying lip service to network support is what would allow it to be more than a niche supplier, says Schonrock.

With activity picking up in March and a 1986 growth rate estimated by Drexel Burnham's Heymann to be about 37%, Intergraph is setting its sights on IBM. And officials show no signs of modifying their time-tested strategy.

"You maximize performance, throughput, and bang-for-the buck in a system if you intimately integrate software, hardware, and firmware design," says Schonrock in explaining Intergraph's success. "Our growth as a company over the past 10 years has certainly reflected our successful implementation of that philosophy." *–George Leopold*

FIRST IT WAS THE YUGO, NOW IT'S THE ISKRA VME

FARMINGDALE, N. Y.

Good things in small packages seem to come these days from Yugoslavia. The country that brought you the $4,000 automobile—the Yugo—is now ready to take a run at single-board computers with its own brand of VMEbus technology. Iskra, a name well known in Europe, is about to try to crack the U. S. market through its Iskra VME Technologies Inc. unit. And because the young company can count on the backing of its 40-year-old, $2 billion parent, Iskra VME would seem to have the resources needed in order to play this high-stakes game.

ZIVKOVIC: The head of Iskra VME Technologies has big plans for his U. S. company.

Iskra VME is making its debut with some impressive hardware: two thoroughbred single-board computers with full operating-system support [*Electronics*, April 28, 1986, p. 13]. Several more CPU cards and a raft of controller cards are already in production in Europe, and industry observers are betting they will be introduced to the U. S. Add to the equation the parent company's software talent and Iskra appears to be a potent force among more than 100 companies scrambling for a piece of the

BOTTOM LINES

HYBRID CIRCUIT USE TO HIT $9 BILLION BY 1990

The consumption of hybrid circuits in the U. S. climbed to slightly more than $5 billion last year and could reach $9 billion by 1990, according to a new study by Gnostic Concepts Inc., a San Mateo, Calif., market-research company. That represents an average annual growth rate of 12.9%, or nearly 2.5 percentage points per year faster than the growth in consumption of electronics equipment in the U. S. in the same period, the company estimates. Of the total hybrid production in the U. S. last year, 61% was captive production. This should fall to 58% by 1990, Gnostic Concepts estimates, as more companies turn to the merchant market for their needs.

SYMBOLICS, MERRILL LYNCH IN R&D DEAL

Symbolics Inc., the Concord, Mass., artificial-intelligence computer company, will get help in funding its next generation of products from Merrill Lynch Ventures Limited Partnership, New York. Under terms of a research and development agreement between the two organizations, Merrill Lynch Ventures will contribute about $7 million over the next several years to Symbolics' $16 million project to develop an advanced computing system based on full-custom very large-scale integrated circuits. Symbolics will provide the rest of the funds.

DECISION DATA ACQUIRES PANATEC

Decision Data Computer Corp., a supplier of products and services for IBM Corp.'s System/3X line of computers, has acquired Panatec, a Garden Grove, Calif., software developer. Terms were not disclosed. Decision Data, of Horsham, Pa., said the addition of Panatec would help support its strategy of developing advanced computer products and vertical-market applications software.

FIBER-OPTIC STARTUP GETS $1.1 MILLION

Lightcom Inc., a two-year-old company that makes a fiber-optic universal data multiplexer, has raised $1.1 million in its second round of venture financing. The Hayward, Calif., company said this brings its total financing to $2.6 million. The company's multiplexer is targeted to large companies that need high-speed, cost-effective data communication in large buildings, on campuses, and in campus-like environments.

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Software Electronics Engineer, for Design and development of 68000, 6802, 8086 and Z80 based-microprocessor systems using microprocessor development equipment including in-circuit emulators, linkers, loaders and higher level languages such as C and Pascal. Design and development of discrete control sequencers using logic design techniques, switching circuit theory, and microprogramming. Design and development of communications networking and distributed processing products. Interface with customers, engineers and marketing to determine software specifications; design software using Yourdon's Structured Analysis & Structured Design techniques and State Transition Tables/ Diagrams. Master of Science degree in Electrical Engineering with a major field of study in Computer Engineering required with at least 2 months of industrial or academic research in planning, design and implementation of an 8086-based microprocessor interface. Incumbent must have had at least one course in the following areas: Distributed Processing Systems; Microcomputers; Logic Design & Implementation; Switching Circuit Theory. 40 M/F, 8:30-5:00, $31,000/yr. Send resumes and social security numbers to: Illinois Job Service, 910 South Michigan Avenue, Room 333, Chicago, Illinois 60605, Attn: Mrs. S. Chalem, Ref. #5394-S, An Employer Paid Ad.

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$240 million VME market.

The company's muscle comes from the state-owned, multinational Iskra Electronics, a conglomerate that offers VME-based work stations, software, telecommunications equipment, and components worldwide. Iskra "has established a presence in more than 60 countries around the world, with production facilities in such countries as Austria, Spain, Switzerland, and France," says Iskra VME president Miki Zivkovic, who came from Yugoslavia to head the startup.

Iskra set up its U. S. arm in 1967 but didn't begin a concerted effort to crack the U. S. market until last spring, when it launched Iskra Software International to market the Formatics forms-generator package for Digital Equipment Corp. computers. Formatics is intended to help novices and nonprogrammers generate forms in a DEC environment.

Iskra VME is a natural complement to the software effort, and the thrust of the two concerns seems to be for the high ground in computer markets. Iskra is steering clear of commodity products such as memory boards and micro-based software and aiming instead for high-margin units, where it can leverage its hardware and software expertise to greatest advantage.

A COMPATIBLE LINE. For example, Iskra VME's two central-processor-unit board offerings include a version of Intel Corp.'s 80286/87 processor fully adaptable to either Xenix or MS-DOS operating systems; the other board uses DEC's J11 processor optimized for the RSX-11M operating system.

Slated for fall introduction in the U. S. are a 68010 CPU board and a Z80-based communications controller. Zivkovic says other products are also on the way, including a memory-expansion board, a disk controller, and graphics cards. But he is tight-lipped about whether the company will market here its 9-slot VME work station, dubbed Trident, now sold in Germany and the UK.

"The work station comes from the three CPU architectures it supports," he says. "Besides its ergonomic design, it was designed to give customers the flexibility to choose among three processor architectures—DEC, Intel-IBM, and Motorola—and independence, because it's based on a standard bus structure."

If Iskra is on new ground with its U. S. hardware sales effort, it can draw on the lessons learned from software sales. Its software has been a hit with credit-collection agencies, Zivkovic says. "We never suspected credit collection was such a big business here. We don't have this in my country. Also we learned that it is necessary, since we found out that sometimes customers disappear and you don't get paid." *–Robert Rosenberg*

WHY O'ROURKE IS SELLING CIM PRODUCTS SO HARD

PALO ALTO

When Rockwell International acquired the Allen-Bradley Co. early in 1985, the word went out from Rockwell's Pittsburgh headquarters that the old-line industrial controls maker was to be left to plot its own course, without interference from the new parent. "Allen-Bradley will call you when they need you—until they do, leave them alone," is the way that its president, J. Tracy O'Rourke, remembers the directive from Rockwell president Don Beall.

O'Rourke and Allen-Bradley had already charted a true course as a provider of industrial automation systems, without Rockwell's help. In any case, the energetic O'Rourke would have been hard to find. In eight years at the Milwaukee company, first as vice president of corporate development, then as chief operating officer, and since last month as chief executive officer, he has consistently evangelized across the nation for the cause of U.S. factory automation. He gives 30 to 40 speeches a year extolling computer-integrated manufacturing as the savior of U.S. industry.

BLUE-COLLAR COMPUTERS. Last month, he was at Stanford University, where he spread the gospel of CIM to a conference on industrial productivity. The essence is that what O'Rourke calls blue-collar computers will have to replace blue-collar workers or the long-term competitiveness of U.S. manufacturing will erode. "The idea that we can transform ourselves into a service and information economy is utopian," O'Rourke says. The service economy adds value inside very artificial boundaries. Try building an oil tanker and paying for it with McDonald's hamburgers."

O'Rourke knows of what he speaks. He has guided Allen-Bradley in its transition from a manufacturer of electromechanical controls to a provider of sophisticated CIM systems. "The company ran very successfully for 75 years as a general-purpose hardware company," he points out. "It let other people innovate, and it would then improve on the innovations."

J. TRACY O'ROURKE: The U. S. cannot exist as solely a service economy.

When O'Rourke came on board in 1978, he says, the company was just beginning its transition. "We had to become a company that participated in solutions. We never even had a field sales organization. When a motor starter failed, it was replaced. Now our field sales organization does repairs, applications engineering, and training. We supply not only hardware but also software, service, and systems for CIM."

BUILT PYRAMID. Allen-Bradley organizes its plant-wide automation products according to what it describes as a five-level pyramid. At the bottom of the pyramid, the machinery process level, are the basic sensing and control devices that actually operate on manufactured goods. Next up is the station level—programmable controllers and other equipment that converts input from the sensors to commands, based on direction from higher levels.

The cell level contains color graphics systems and advanced controllers that tie together these islands into an automated system by means of a token-bus local-area network. All these industrial controls are integrated with management computers at the next level, the center level, where data from lower levels is analyzed and production scheduled. The plant level, at the top, performs overall planning. The entire system is designed to work with the Manu-

PEOPLE ON THE MOVE

CORNELIUS VAN DER KLUGT

☐ Dutch electronics giant Philips has named Cornelius J. van der Klugt president. He succeeds Wisse Dekker, who has become chairman of the supervisory board. The 61-year-old van der Klugt joined the Eindhoven company in 1950 and for 15 years held management positions in Latin America. In 1978, he became a member of the management board and four years later was named vice president.

JERRY LOUNSBERY

☐ Software producer Stella Systems Corp., Cupertino, Calif., has appointed Jerry Lounsbery, 32, as executive president. Lounsbery previously served as a consultant to companies in Japan. Stella operates in conjunction with its sister company, Stella Systems of Japan.

TOM BAY

☐ Hytek Microsystems Inc., Los Gatos, Calif., has brought on board a director of corporate strategy. Tom Bay, who has been a private investor and serves on several boards of local companies, initially will direct strategy and sales for Topaz Semiconductor, a wholly owned Hytek subsidiary specializing in DMOS products.

DAVID M. BOTTOMLEY

☐ Seco Systems Inc. has named David M. Bottomley president, replacing Murray Simpson, who retired on April 15. Sedco, a Melville, N. Y., subsidiary of Raytheon Corp., makes electronic countermeasure equipment. Bottomley, 51, joined Sedco in 1975 and was a vice president at the time of his promotion.

ISAO IWASHITA

☐ SEH America Inc. has named Isao Iwashita president. He replaces Tom Kaya, who will return to the parent company, Shin-Etsu Handotai Co., Tokyo, as managing director of international operations. Iwashita comes to the Vancouver, Wash., silicon-wafer manufacturer from the UK, where he was president of SEH Europe since 1984.

RON IMBRIALE

☐ Northwest Instrument Systems Inc. has promoted Ron Imbriale, 39, to vice president. He joined the Beaverton, Ore., company in Germany in 1982 to set up its European operations, returning in 1985 as director of U. S. sales and European operations. Previously, he was European sales manager for Tektronix Inc.'s Design Automation Division in Amsterdam.

ALEX BENNETT

☐ Lattice Logic, Edinburgh, Scotland, has chosen Alex Bennett as its managing director. Bennett, who began his career at the age of 15 with Ferranti as a student apprentice, previously established the British operation of Burr-Brown Inc., Tucson, Ariz. Lattice Logic manufactures computer-aided design software.

facturing Automation Protocol that General Motors Corp. is championing as a factory-floor standard.

O'Rourke, who holds a BS in mechanical engineering from Auburn University, concedes that the transition to automated manufacturing will incur "a lot of short-term human discomfort. There will be no more 40-year jobs. It's a major shift. The poor guy who is going to get caught is the 40- to 55-year-old worker." He says business and government should recognize this problem now and unite to help.

But in O'Rourke's view, the disruption will subside. Eventually, when the baby-boom work force has peaked in the 1990s, the U.S. may actually have a shortage of workers, he says. And when automated manufacturing drives down costs, goods will be more affordable for everyone.

The transition to CIM won't happen overnight, O'Rourke notes, because "products that are well along in their life cycles are not good candidates for CIM." But whether or not his scenario is accurate, the change to CIM is inevitable, he insists. "The United States can contribute capital and technology. It has priced itself out of the market in labor."

And offshore manufacturing is not the solution to high labor costs. IBM, he points out, is bringing much of its manufacturing back to automated plants in the U.S. "They have reduced their work force by half and are producing more units," O'Rourke says. "They still have some downtime but their costs are competitive. When they get more uptime—which is realistic—they will be the lowest-cost producer of keyboards and printers in the world."

DIVERSE BACKGROUND. Although O'Rourke, 51, has helped to guide Allen-Bradley into the realm of electronics, he has a diverse corporate background. He came to the company from Allegheny International Corp., a Chicago conglomerate that bought and sold companies as if they were Oriental rugs. Allegheny had been the white knight that bought out O'Rourke's previous employer, another conglomerate called Chemetron, for which he also performed strategic planning. "I am an expert at being acquired," he says.

O'Rourke went to Allen-Bradley after Allegheny began to sell off pieces of itself and he ended up having very little to do. He is delighted to be part of Rockwell.

"The two sides have gotten together and started to build bridges. The technology flow has started. They are good customers, and they have phenomenal strength in semiconductors, sensors, and materials. We are enormously better off as part of Rockwell than we have ever been." *–Clifford Barney*

PEOPLE

AN 'OLD JAPANESE HAND' FACES TOP CHALLENGE

TOKYO

At 34, James Shinn is already an old hand at dealing with the Japanese, having spent time in their country as a banker and government trade negotiator. Now he's facing his toughest challenge yet: to top $300 million in sales in Japan for Advanced Micro Devices Inc. by 1990.

As general manager of AMD operations in Japan, Shinn's goal is to produce a fivefold increase over the company's estimated $65 million Japanese sales last year. The Philadelphia native, who took over the post 13 months ago, thinks he has the product mix and the home-office commitment to reach or exceed that target.

Shinn's optimism is based on more than enthusiasm. Since January, the Sunnyvale, Calif., company has been manufacturing products aimed at the Japanese market [*Electronics*, April 14, 1986, p. 44]. Among the most promising are a coming generation of complementary-MOS versions of its 32-bit microprocessor building blocks for such growth markets as artificial intelligence and Japan's Fifth Generation Computer Systems Project, Shinn says.

He also predicts that, as the office-automation market picks up, a strong demand will develop for products such as AMD's 7970 CEP compression and expansion processors, which shrink bit maps up to 50 times to achieve faster facsimile transmission and increased optical-disk storage capacity.

"This is AMD proprietary technology, which makes it highly profitable even during market downturn periods," says Shinn, who joined the company in 1980 as a product planner, later became a product marketing engineer, and was district manager in New York when he accepted his present post.

His understanding of the Japanese market comes from hands-on experience. As a banker, he spent two years handling Chase Manhattan's portfolio of high-technology companies in Tokyo. As a State Department trade negotiator in U.S.-Japan semiconductor talks in the late 1970s, he came face to face with what he describes as "tough but incredibly well-prepared Japanese bureaucrats. I learned to understand them and respect them."

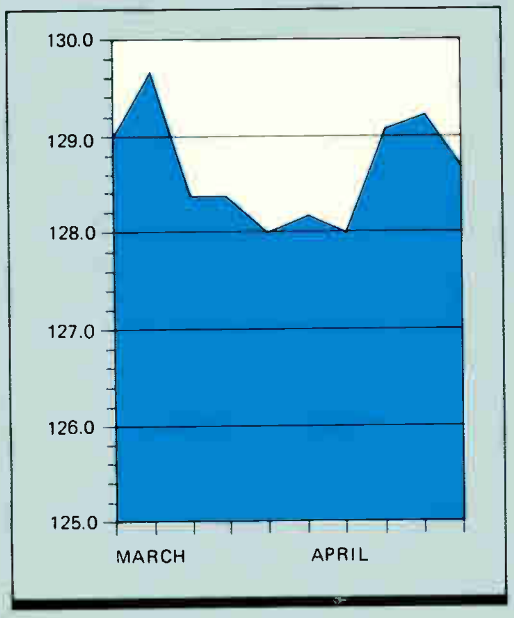
He later earned an MBA at Harvard Business School, where yet another "Japan connection" developed. His wife, Masako, was a classmate at Harvard. She's now a securities dealer in Tokyo.

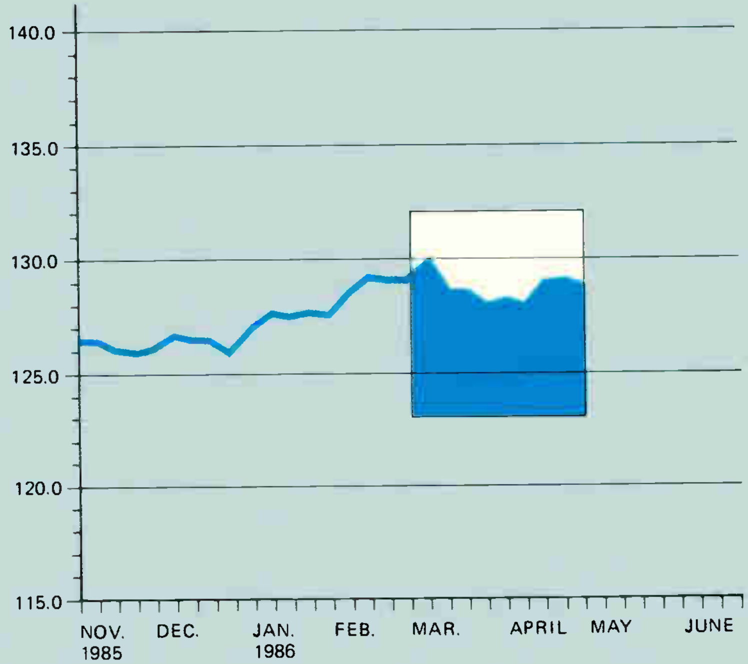
Shinn's BA is from Princeton University, where he majored in economics and minored in computer science. He has also attended Tokyo University to study Japanese, a pursuit he calls "never-ending"—he's still taking regular early-morning tutorials. But the effort allows him to converse easily in Japanese with his 38-member staff, making a demanding job more manageable.

Nonetheless, he's often forced into unconventional scheduling. "I'll come back at 5 p.m. from a day of working with customers, and I know I've got another three to four hours of work ahead of me. So I go next door where there's a swimming pool, do a few laps, and that clears my mind." Then he goes back to the office. *–Michael Berger*

JAMES SHINN: From Chase Manhattan, to Harvard, to AMD's general manager in Japan.

ELECTRONICS INDEX





THIS WEEK	=	128.7
LAST WEEK	=	129.2
YEAR AGO	=	127.4
1982	=	100.0

The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U. S. ELECTRONICS PRODUCTION

	February 1986	January 1986	February 1985
Office and data-processing equipment	263.0	268.2	264.0
Communications equipment	217.4	220.4	218.1
Radio and TV equipment	152.3	159.4	144.3
Electronic and electrical instruments	141.8	142.0	138.7
Components	238.7	242.1	283.8

U. S. GENERAL ECONOMIC INDICATORS

	February 1986	January 1986	February 1985
Index of leading economic indicators	175.4	174.1	167.4
Budgeted outlays of the federal government ($ billions)	78.290	82.849	74.851
Budgeted outlays of the Department of Defense ($ billions)	21.268	20.945	19.785
Operating rate of all industries (% capacity)	77.4	77.9	79.1
Industrial-production index	125.7	126.6	123.7
Total housing starts (annual rate in thousands)	1,997	2,034	1,632

Just as the U. S. electronics industry appeared to be snapping out of its business doldrums, it had a setback in February. Production of electronics goods fell 1.9%, the first decline in output in four months. February was also the first time in more than a year that output fell in all industry sectors. The drop in production caused the *Electronics* Index to fall half a point last week.

Makers of TV and radio equipment led the month's industrywide downturn with a 4.5% drop. Meanwhile, production of office equipment slipped 1.9% and output of both electronic components and communications equipment fell 1.4% in the month. Instrument manufacturers cut production by only 0.1%.

But there is still some cause for optimism. The overall U. S. economy could soon begin to turn up more strongly—the foremost sign was the 0.7% surge in February's index of leading indicators. That advance was the most vigorous since last November.

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NEW PRODUCTS

A BUILDING-BLOCK APPROACH TO DESIGNING RISC COMPUTERS

SYSTEM DESIGNERS CAN PICK FROM A FAMILY OF BOARDS AND CHIP SETS

Superminicomputers à la carte are on Mips Computer Systems' product menu. The company is serving up a family of reduced-instruction-set computing products that includes component kits, CPU boards, memory boards, and a development system for design and software engineers. The R2000 line is targeted at system designers who make high-performance multiuser Unix computers for the engineering, communications, and aerospace markets.

With either the components or the boards, engineers can build superminicomputers with sustained performance of 3, 5, 8, and 10 million instructions/s. A systems designer could build a computer that, at 10 mips, would be about 10 times faster than the Digital Equipment Corp. VAX 11/780—at a price comparable to that of work stations.

Exact pricing varies with system performance and the system designer's value added; but Mips's basic 3-mips CPU card sells for as little as $3,170. "By delivering RISC technology at various levels of integration, we assist our customers in quickly bringing products to market with superior price/performance," says Mips president Vaemond Crane.

The Mips architecture is simpler and leaner than most other RISC implementations, the company says. The hardwired machine code is free of the factors that typically degrade cycle time, pipeline efficiency, and responsiveness: Mips excludes such elements as hidden registers, condition codes, variable-length instructions, and multiple address modes.

CUSTOM PROCESSOR. At the heart of the R2000 product line is a custom 32-bit processor that delivers 10-mips execution, a floating-point coprocessor, and a write buffer that consists of four gate arrays. The processor contains 32 general-purpose registers and instruction-set support for three external coprocessors. The processor also includes a cache-control unit—a 64-entry, fully associative, translation look-aside buffer that provides access to the CPU's 4-gigabyte virtual address space.

The chip is fabricated in 2-μm double-metal single-polysilicon CMOS; it integrates about 100,000 transistors on a die measuring 8.5 by 10 mm, which is packaged in a 144-pin ceramic pin-grid array. It dissipates less than 3 W. The floating-point accelerator, which is also implemented in CMOS, operates as a tightly coupled coprocessor that at peak operation executes about 3 mips.

The component kits are available in two versions. The R2065/12 consists of a 12.5-MHz processor capable of 8 mips, the floating-point accelerator, and the write-buffer gate arrays. It is priced at $1,750 each and available 90 days after ordering. The R2065/16 contains a 16.7-MHz version of the main processor with a 10-mips rating.

RISC. Mips's boards or chips build Unix-based RISC systems that deliver up to 10 mips.

It will sell for $2,250 and be available in the first quarter of next year.

Engineers who want to start from board-level products have three choices, the 3-mips R2100, the 5-mips R2300, and the 8-mips R2600. They're designed around both VMEbus and Multibus II architectures. Each board contains the main processor chip, the high-speed instruction and data caches, separate buses for I/O and computation, memory interface circuitry, and a socket for the floating-point coprocessor.

The R2100, R2300, and R2600 boards sell for $3,170, $4,775, and $6,420 each in large quantities. VMEbus versions of the R2100 and R2300 are available 90 days after ordering. The R2600 will be available in the fourth quarter. The company will anounce availability of the Multibus II versions later in the year.

To go with the CPU cards, Mips is providing a memory card, also available in both VMEbus and Multibus II versions. The memory card, the R2350, provides 4 megabytes of read-only memory for use with the R2300 and R2600 CPU boards. The memory board, which will be available in the third quarter for $3,300, is dual ported to the CPU board, over the Mips private memory bus and the system bus.

HEAD START. To give customers a head start, Mips has a development system for $59,000 in single quantities. The M/500 is configured around the R2300 board and is housed in a 12-slot VMEbus card cage. The basic configuration consists of 4 megabytes of memory, a 337-megabyte hard-disk drive, a 60-megabyte ¼-in. cartridge-tape drive, an Ethernet controller, and eight serial input/output ports.

The development system's price includes software packages also available separately to customers working with the chips and boards. The Umips operating system is based on AT&T Co.'s Unix. Two versions are available, one that is compatible with AT&T's System V and the other with the 4.3bsd version developed at the University of California, Berkeley. Included with both are an assembler, an optimizing C compiler, a linker, a loader, and a symbolic debugger. When available next quarter, a source-code copy will be priced at $125,000 and a binary-code copy at $300.

Optional software offerings include a Fortran 77 compiler that will go for $75,000 in source code and $125 in binary when available next quarter, and a Pascal compiler with the same pricing and availability schedule.

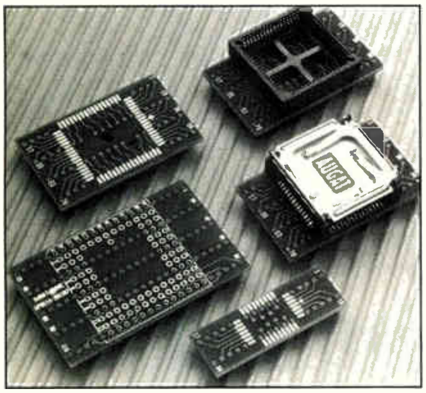
To interest engineers building engineering work stations, Mips has come up with a version of Sun Microsystems Inc.'s Network File System (NFS), which allows Mips-based products to communicate in a network of systems using the NFS protocols. When available in the third quarter, the software will sell for $275 for use with the chips and boards and for $975 for use with the M/500 development system. *–Steve Zollo*

Mips Computer Systems, 930 Arques Ave., Sunnyvale, Calif. 94086. Phone (408) 720-1700 [Circle reader service number 338]

SMD ADAPTERS AID PROTOTYPING

Up to now, engineers had no way to use ICs housed in surface-mountable packages and pin grid arrays on their wrapped-wire prototyping boards. Now, Augat's Densepak line of adapters permits these packages to be mounted on universal wrapped-wire panels.

The Densepak adapters can be positioned anywhere on the board, helping



keep wiring paths as short as possible. The adapters use only about 20% more space than the actual devices, with no wasted pins.

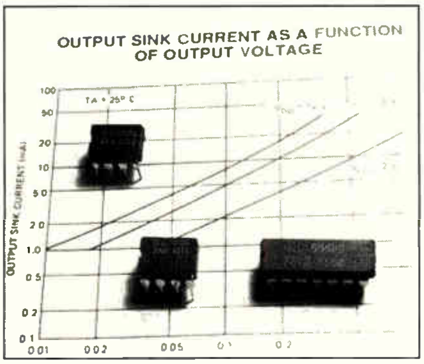
The APG series, for mounting PGAs, comes in versions with 70, 72, 80, 88, and 104 pins. The SSM and RSM, which are for square and rectangular leaded or leadless chip carriers, come in 20- and 28-pin models. Priced from $5 to $50 each, the adapters are available immediately.

Augat Inc., Components Division, 33 Perry Ave., P.O. Box 779, Attleboro, Mass. 02703. Phone (617) 222-2202 [Circle 350]

CMOS TIMER PROVIDES 80-mA DRIVE CURRENT

A monolithic timer, fabricated in silicon-gate CMOS, boasts a wide frequency range but still provides an 80-mA drive current at 5 V. The part consumes just 100 μA. The ALD555 is Advanced Linear Devices Inc.'s first part and is pin-compatible with the industry-standard bipolar NE555 timer.

On the high-frequency side, the ALD555 offers 500-ns monostable-mode



and 2-MHz astable-mode operation. The chip's low quiescent current minimizes switching-current spikes, suiting the part for use in battery-operated equipment or in environments with high noise levels.

Housed in a 14-pin DIP, the ALD555 costs $1.18 each in lots of 100 pieces. It is available from stock.

Advanced Linear Devices Inc., 1030 W. Maude Ave., Suite 501, Sunnyvale, Calif., 94086. Phone (408) 720-8737 [Circle 351]

AMD ADDS TIMER TO ITS 80286 FAMILY

A CMOS programmable interval timer chip rounds out Advanced Micro Devices' family of low-power microprocessors and peripherals for 80286-based systems. AMD's 24-pin 82C54 is plug-compatible with the 8254 n-MOS timer peripheral from Intel Corp.

The CMOS peripheral, however, consumes only 6% of the power of the n-MOS chip. The 82C54 interval timer dissipates 50 mW in the active mode, 50 μW in standby.

When used with other components in AMD's low-power 80286 central-processor chip set—such as the 82C288 bus controller, 82284 clock generator driver, and Am9517A multimode direct-memory-access controller—total power dissipation of the host CPU subsystem will be 2.3 W lower than implementations using other n-channel parts. This suits the 82C54 and the entire chip set for a range of portable computer and instrumentation system applications.

Housed in a 24-pin ceramic DIP, the 82C54 costs $7.85 each in 100-piece quantities. The part is also available in an 8-MHz version and a 10-MHz 82C54 is slated for shipment in the third quarter.

Advanced Micro Devices Inc., 901 Thompson Pl., Sunnyvale, Calif. 94088. Phone (408) 732-2400 [Circle 370]

SOFTWARE DESIGNS STATE MACHINES

Intel has created a design package called iState that lets systems hardware designers use erasable programmable logic devices to develop a state-machine design and enter the design into iPLDS. The software runs on the Intel Programmable Logic Development System.

Programming is by means of logic-programmer pods included in the iPLDS or with an Intel Universal Programmer. Once a state-machine design has been coded using iState, the program is used as input to the Intel Programmable Logic Software package. The iPLS software optimizes the code's logic, determines the best fit of the state-machine design to the EPLD selected, compiles the program, and produces a Jedec or Intel hexfile for programming.

A complete iPLDS system costs $2,500. An iState upgrade, available now, costs $500.

Intel Corp., Literature Dept. W-298, 3065 Bowers Ave., Santa Clara, Calif. 95051 [Circle 352]

VAX GETS A VALIDATED ADA COMPILER

TeleGen2, Telesoft's new Ada development system, carries Defense Department validation for use with Digital Equipment Corp.'s VAX computers. TeleGen2 consists of a cross-compiler, cross-development system, comprehensive development system, optional language-productivity and embedded systems tools, optional source-level debugger, and optional global optimizer.

The Ada development system supports large applications that exceed 250,000 lines of code. The compiler itself processes Ada source lines at a rate of 500 to 1,000 lines/min for a wide range of benchmarks.

Features include an architecture that supports real-time systems, simulators, and emulators based on the MC68000 family of processors; highly optimized interrupt handling; very fast target code; and fast compilation of multiple units in the same file. TeleGen2 license fees start at $4,500. Shipments will be made 60 days after receipt of order.

TeleSoft, 10639 Roselle St., San Diego, Calif. 92121. Phone (619) 457-2700 [Circle 353]

SIMULATION MODELS BOW FOR 80386

Logic-simulation support is now available for the new Intel 32-bit microprocessor, the 80386. The SmartModels package is a collection of behavioral-level logic-simulation models that allows designers to perform logic simulation on circuit-board and systems-level designs.

SmartModels provides the logic characteristics and timing data needed by simulators to assess a circuit's operation. A troubleshooting capability called Symbolic Hardware Debugging checks for timing and other error conditions. If errors are found, the models generate error messages that pinpoint the exact cause, location, and time of the problem.

The SmartModels package runs on popular computer-aided engineering stations and is priced at $1,830. It will be available later this month.

Logic Automation Inc., 19545 N.W. Von Neumann Dr., Beaverton, Ore., 97005.
Phone (503) 690-6900 [Circle 355]

ION IMPLANTER HANDLES 8-IN. WAFERS

The NV-8200 medium-current ion-implantation system, which can handle 8-in. wafers, contains a proprietary electrostatic digital scanner that maintains a ±1° beam angle of incidence on the wafer. The digital scanning system also delivers an ion dose across an 8-in. wafer with a uniformity difference of less than ±0.5%.

Particulate contamination and wafer breakage are held to a minimum, even with throughput of 250 wafers an hour. The user can control wafer tilt and orientation through the system's computer. Pricing for the system was unavailable.

Eaton Corp., Ion Beam Systems Division, 2433 Rutland Dr., Austin, Texas 78758.
Phone (512) 837-7600 [Circle 357]

ETCHER WRITES 0.5-MICRON LINES

The Rib-Etch 160 reactive ion-beam etching system uses a wide-angle ion beam with chemically reactive gases to selectively etch patterns as small as 0.5 μm. The Rib-Etch 160 handles a wide range of materials and applications, including chromium masks, radio-frequency devices, and magnetic bubble memories. The system etches new materials, such as silicides and III-V compounds, as well as standard materials.

The microcomputer-controlled system stores up to 99 programs. The stainless-steel process chamber takes up to 6-in. wafers onto a water-cooled stage. The ion gun is likewise water cooled, and

ion-beam uniformity is profiled before each run by an automatic current sensor. Another ion gun can be mounted in the ceiling of the chamber for low-temperature depositions.

The Rib-Etch 160 meets Class 10 clean-room standards. The company will quote the price of an installed system and delivery time.

Coberly & Associates, 2100 E. Foothill Blvd., Pasadena, Calif. 91107.
Phone (818) 792-4158 [Circle 356]

64-K STATIC RAM HAS 55-NS ACCESS TIMES

The model MSM5188, a 64-K SRAM built in 2-μm silicon-gate CMOS, suits applications in high-speed cache or buffer memories. The SRAM is organized as 16-K by 4 bits and comes with maximum access times of either 55 or 70 ns. A 45-ns version fabricated in 1.5-μm CMOS will soon be available.

The MSM5188 operates from a single 5-V power supply and is TTL-compatible. Its power dissipation is only 468 mW in operation, or 11 mW in the standby mode. Available in a 300-mil-wide, 22-pin plastic DIP, the 70-ns version costs $8.35 in 100-piece quantities. Delivery is from stock.

Oki Semiconductor, 650 N. Mary Ave., Sunnyvale, Calif. 94086.
Phone (408) 720-1900 [Circle 363]

ECL RAM BOASTS 7-NS ACCESS TIME

The DM10422A-7 claims a worst-case access time of 7 ns. Developed for scratch-pad memory, buffers, and writable control-storage applications, the emitter-coupled-logic SRAM is organized as 256 by 4 bits, but can also be configured as 512 by 2 bits or 1,024 by 1 bit through externally accessible block-select controls.

The DM10422A-7 is voltage-compensated and fully compatible with 10K and 10KH ECL parts. A RAM compatible with 100K ECL will be available in the third quarter. In lots of 100, the ECL RAM in a 24-pin ceramic DIP is $13 each. It is available now.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95052.
Phone (408) 721-5540 [Circle 364]

DIGITIZER HITS 1.3 GIGASAMPLES/S

The model 6880 waveform recorder digitizes and records high-speed signals and waveforms at 1.3 gigasamples/s—the manufacturer says that's faster than any other waveform digitizer on the market. Analog-to-digital conversion takes a sampling period of 742 ps, with 8-bit resolution, on signals with bandwidths from dc to 250 MHz.

The 6880 targets applications involving high-speed single-shot or repetitive events, including pulse characterization of fast transitions and propagation delays in

ECL devices. Computer manufacturers will also find the instrument useful in testing high-speed logic boards, LeCroy says. Other uses include the monitoring of electromagnetic pulse experiments and insulator characterization.

Available in 30 days, the 6880 costs $15,500. The model 6010 controller, which costs $3,950, or an optional keyboard enables the system to be operated as a stand-alone benchtop digital oscilloscope.

LeCroy Corp., 700 S. Main St., Spring Valley, N.Y. 10977.
Phone (914) 578-6038 [Circle 368]

PARTS TESTER FINDS STATIC SENSITIVITY

As ICs and other components get more complex, testing them for their susceptibility to electrostatic discharge becomes more difficult. Now, the model 400A from Penril Corp.'s Electro-Metrics Division provides two key features for ESD simulation.

Based on IBM Corp.'s Personal Computer, the system offers easy and flexible programming of key test parameters. In addition, it has a wide voltage supply range—50 to 5,000 V positive polarity and −50 to −2,000 V negative, with 50-V resolution.

Operators can use the model 400A to

program a test-charge storage capacitance of 100 to 700 pF in 100-pF increments, allowing for precise characterization of an IC's ESD susceptibility. Up to 64 pins of a DIP or chip carrier may be subjected to a charge, in any order.

Including the PC, the model 400A costs $32,495 each and is available now.

Penril Corp., Electro-Metrics Division, 100 Church St., Amsterdam, N.Y. 12010.
Phone (518) 843-2600 [Circle 369]

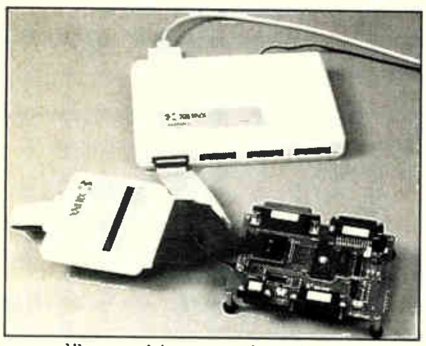
XILINX'S ARRAY GETS IN-CIRCUIT EMULATION

The model XC-DS 24 from Xilinx gives users working with the company's Logic Cell Array in-circuit emulation capability for debugging their application-specific IC designs. Previously, engineers used simulation to verify ASIC designs, a process that can take several weeks, rather than the seconds that in-circuit emulation takes.

The in-circuit emulator works with the company's XACT development system. In-circuit emulation is a combination of hardware and software that allows a design engineer to observe, control, and modify the operation of ASIC logic.

The XC-DS 24 is priced at $3,600. The XACT design-editor software package, which provides interactive placement and automatic routing of logic and I/O blocks, also goes for $3,600. Both are available now.

Xilinx's Logic Cell Array uses a gate-

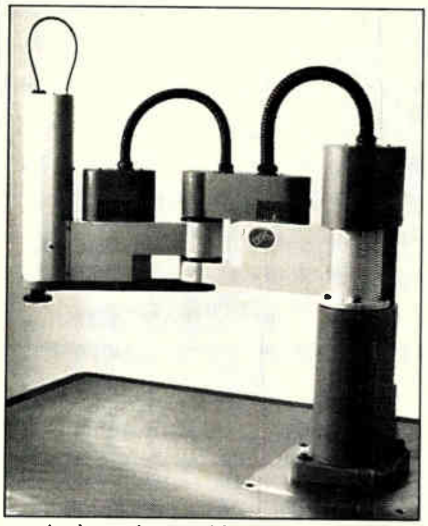


array-like architecture but is user-programmable because it is fabricated in static-RAM technology. Users can configure the logic and I/O blocks and interconnect them in any way.

Xilinx Inc., 2069 Hamilton Ave., San Jose, Calif. 95125.
Phone (408) 559-7778 [Circle 371]

ASSEMBLY ROBOT HAS 22-LB PAYLOAD

The IBM model 7576 manufacturing system is a selective compliant assembly robot arm for light assembly applications. With a maximum payload of 22 lb and a maximum reach of 31.5 in., the



manipulator is capable of speeds up to 173 in./s and repeatability to within ±0.002 in.

The robot, which comes with an IBM 7572 servo power module and the 7576 manipulator, is programmed with an IBM 7532 industrial computer using the licensed AML/2 manufacturing control system program. Price of a typical 7576 system will be $38,700 when it becomes available in the third quarter. A second robot, the 7575, has an 11-lb payload.

IBM Corp., Information Systems Group, 900 King St., Rye Brook, N.Y. 10573.
Phone (914) 934-4488 [Circle 367]

PAGE SCANNER HAS AUTOMATIC FEEDER

The JetReader page scanner uses an automatic mechanism that accepts and feeds a stack of up to 10 sheets. The scanner, which is the new addition to Datacopy's Word Image Processing System (WIPS), comes with software that recognizes 12 different type fonts. In addition, the scanner can be programmed to recognize any 10- or 12-pitch type style.

The scanner has a resolution of either 200 or 300 dots/in. A postprocessing software package formats the scanned text into any of five popular word processors. The WIPS software creates graphics and text on the same page, giving users the ability to manipulate images, size them to fit a preselected space in the word-processor document, and erase or add pixels to an image on a pixel-by-pixel basis.

Applications for WIPS include reports, real-estate listings that contain a photograph of the property, and personnel files. The JetReader is priced starting at $2,950 and will be available this month.

Datacopy Corp., 1215 Terra Bella Ave., Mountain View, Calif. 94043.
Phone (415) 965-7900 [Circle 354]

VME CONTROLLER RUNS ESDI DRIVES

The model 712 disk controller gives VMEbus systems designers the ability to work with Enhanced Small Disk Interface disk drives. The disk controller can support up to four ESDI disks. Its proprietary pipelined architecture delivers a high-speed direct-memory-access rate of 10 megabytes/s. The user can tune the system for optimum performance by controlling the length of time the 712 remains on the VMEbus.

The 712, which operates in a Unix environment, has a 2-K-byte command buffer and an 8-K-byte first-in first-out buffer. In quantities of 1,000, it is priced at $1,295, and it is available 60 to 90 days after receipt of order.

Xylogics Inc., 144 Middlesex Turnpike, Burlington, Mass. 01803.
Phone (617) 272-8140 [Circle 365]

DISK CONTROLLER HAS ON-BOARD CACHE

The Rimfire 3200, a Storage Module Drive disk controller for the VMEbus, contains a 0.5-megabyte on-board sector cache; the firmware that manages the cache is a real-time executive written in C language and is executed by an on-board 80186 microprocessor.

The controller uses multiple circular command queues; this allows the Rimfire 3200 to look ahead at pending commands in a multiprocessing environment. Other features include an on-board defect map to avoid unnecessary seeks, and compatibility with 24-MHz drives. The controller sells for $2,805.

Ciprico Inc., 2955 Xenium Lane, Plymouth, Minn. 55441.
Phone (612) 559-2034 [Circle 366]

PROCESSORS CREATE PRIVATE X.25 NETS

A hardware and software offering from NCR Comten is aimed at users seeking to establish a private X.25 network or integrate one into an existing IBM Corp. Systems Network Architecture. Three packet-switching processors are available—low end, midrange, and high end—depending on network requirements. They offer switching rates of 100, 400, or 800 packets/s, respectively, over 64 to 480 full-duplex lines.

Actual system prices depend on configuration, but base prices range from $23,000 to $72,000 for this packet-switching hardware and software. The private X.25 network is currently available.

NCR Comten Inc., 2700 Snelling Ave. N., St. Paul, Minn. 55113.
Phone (612) 638-7777 [Circle 359]

MEETINGS

LASER APPLICATIONS SHINE AT CLEO

Optical devices in electronic systems will be getting a lot of attention at this year's Conference on Lasers and Electro-Optics—it will be the focus of about one third of the meeting's 82 sessions.

CLEO, which will run simultaneously with the International Quantum Electronics Conference at San Francisco's Moscone Center June 10-12, will highlight new work in communications, diode lasers, semiconductor processing, sampling, and optical data storage.

One of the seven communications sessions features a paper from the U.S. Naval Research Laboratory on new optical techniques for generating and detecting microwave signals. Peter Moulton, program chairman and vice president of Schwartz Electro-Optics Inc., Orlando, Fla., says the technique combines the outputs of two semiconductor diodes to generate microwave signals.

At one of five diode-laser sessions, a paper from Lightwave Electronics Corp. and Stanford University describes single-mode lasers that can be used as coherent laser radar transmitters. The lasers use a powerful single-frequency source and can be used to measure Doppler shift, according to Moulton.

Semiconductor processing, the subject of four sessions, will feature an invited paper from Bruce M. McWilliams of the Lawrence Livermore National Laboratory that describes a laser-write process for fabricating very large-scale integrated gate-array interconnections.

One paper to be presented at a session on ultrafast sampling is a collaboration between the University of Rochester and the Massachusetts Institute of Technology that covers electro-optic characterization of picosecond permeable-base transistors. "Light pulses are generated and shined on the gate of a PBT to inject a signal, then you look at the output of that PBT," Moulton explains.

Optical data storage, with two sessions, will be represented by papers from Hitachi, IBM, NEC, RCA, Sony, and a few smaller companies.

International Microwave Symposium, IEEE (Edward C. Niehenke, Westinghouse Electric Corp., P. O. Box 746, MS 339, Baltimore, Md. 21203) Convention Center, Baltimore, June 2-4.

Printed-Circuit World Convention IV, Japan Printed-Circuit Association *et al.* (Institute for Interconnecting and Packaging Electronic Circuits, 3451 Church St., Evanston, Ill. 60203), Tokyo Prince Hotel, Tokyo, June 2-5.

Circuit Expo '86, Worldwide Convention Management Co. (Mary Burns Sheridan, Worldwide Convention Management Co., 17730 W. Peterson Rd., Libertyville, Ill. 60048-0159), Convention Center, Long Beach, Calif., June 3-5.

International Conference on Consumer Electronics, IEEE (Marvin Gottlieb, M. Gottlieb Associates, 6009 N. Milwaukee Ave., Chicago, Ill. 60646), Westin Hotel, Rosemont, Ill., June 4-6.

1986 IEEE International Symposium on the Applications of Ferroelectronics, IEEE (Wallace Arden Smith, Philips Laboratories, 345 Scarborough Rd., Briarcliff Manor, N. Y., 10510), Lehigh University, Bethlehem, Pa., June 8-11.

VLSI Multilevel Interconnection Conference, IEEE and University of South Florida (Thomas E. Wade, College of Engineering, University of South Florida, 4202 Fowler Ave., Tampa, Fla. 33620), Santa Clara Marriott Hotel, Santa Clara, Calif., June 9-11.

CLEO/IQEC '86: Conference on Lasers and Electro-Optics/International Quantum Electronics Conference, IEEE and Optical Society of America (OSA, 1816 Jefferson Pl. N. W., Washington, D. C. 20036), Moscone Convention Center, San Francisco, June 9-13.

Usenix Conference and Exhibition, Usenix Association (P. O. Box 385, Sunset Beach, Calif. 90742), Atlanta Hilton and Towers, Atlanta, June 9-13.

CISC-86: Combat Identification Systems Conference, (Systematics General Corp., Brinley Plaza, Rte. 38, Wall Township, N. J. 07719), Fort Monmouth, N. J., June 10-12.

Comdex International in Europe, The Interface Group Inc. (300 First Ave., Needham, Mass. 02194), Acropolis Conference Center, Nice, France, June 10-12.

Nepcon East '86, Cahners Exposition Group (1350 E. Touhy Ave., Des Plaines, Ill. 60017-5060), Bayside Exposition Center, Boston, June 10-12.

Rochester Forth Conference, University of Rochester (Maria Gress, Institute for Applied Forth Research, 478 Thurston Rd., Rochester, N. Y. 14619), University of Rochester, Rochester, N. Y., June 10-14.

NCC '86: National Computer Conference, IEEE *et al.* (NCC '86, American Federation of Information Processing Societies, 1899 Preston White Dr., Reston, Va. 22091), Convention Center, Las Vegas, June 16-19.

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ELECTRONICS WEEK

DEC SEES NO UPTURN YET

Despite a 14% gain in revenue and an 86% surge in profits for its third quarter, Digital Equipment Corp. sees no clear sign that the computer industry is pulling out of its slump. President Kenneth H. Olsen blames the doldrums on top management's delegation of purchasing decisions to lower-echelon managers who buy just for their own departments. This in turn fosters the purchase of disparate equipment that can't be integrated and used to fullest benefit, he claims.

DOES JAPAN AIM TO AVOID PENALTIES?

Japanese chip makers, looking to cut the risk of being penalized for dumping domestically produced mass-memory exports in the U. S., may be fashioning a Southeast Asia strategy. Several makers, including Hitachi, NEC, and Toshiba, plan to assemble and ship 256-K dynamic random-access memories from plants in Malaysia and Singapore directly to the U. S. starting this summer.

AEG TO BUY MODCOMP

In a move to bolster its position in the U. S. factory-automation market, AEG AG, Frankfurt, wants to buy all of Modular Computer Systems Inc. AEG has held a 19% share of the Ft. Lauderdale, Fla., process-computer maker since 1980. The takeover, still subject to approval by U. S. and West German antitrust authorities, would amount to about $42 million. AEG hopes to use Modular Computer's sales network to distribute products from its various divisions in Germany.

MONSANTO, HITACHI IN SILICON DEAL

Monsanto Co. and Hitachi Ltd. have signed a cooperative agreement in which the St. Louis company could supply up to 5% of Hitachi's silicon needs by the fourth quarter. Monsanto and Hitachi engineers will work together to tailor Monsanto's silicon products to the Tokyo company's specifications. Monsanto, which is building a plant in Japan, says its long-range objective is to become a significant supplier of silicon wafers to Hitachi.

TOSHIBA IN FRENCH COPIER VENTURE

In the initial stage of a plan to increase sales of its office-automation equipment in Europe, Toshiba Corp. of Kawasaki, Japan, is establishing a joint venture with Rhône-Poulenc SA, France's leading chemical company, to manufacture and market plain-paper copiers. If the deal wins approval from the French government, the new company, to be known as Toshiba Systèmes (France) SA, will start up in the Paris suburb of Montrouge in June. It will begin producing the copiers by the end of the year, using existing manufacturing facilities of the French company, and expects annual production to reach 200,000 units within three years.

GENRAD, IN SLUMP, GETS BIG ORDER

A bright spot has developed in GenRad Inc.'s otherwise dismal business picture: the Concord, Mass., company has landed the largest order in its 71-year history, from Jaguar Cars of Coventry, England. The automaker has ordered test systems from GenRad valued at $13 million for delivery in 1986. In fiscal 1985, GenRad suffered a revenue decline and a $52 million net loss. The company reports that results from its first quarter, ended March 31, show a continuation of the slump. It expects losses to continue into the second quarter.

EXPERT SYSTEMS FIRM GETS BOOST

Cognitech SA, a two-year old Paris-based expert systems company, after having struggled along with capital of not much more than $250,000, is about to get a $4 million shot in the arm from a new group of shareholder-partners. Put together by founder Jean-Michel Truong-Ngoc, the investors are nationalized computer manufacturer Bull SA, banks Paribas and Crédit Lyonnais, the French Atomic Energy Commission, and an unnamed government agency. So far Cognitech has landed orders for a total of 53 expert systems, including one from nationalized aluminum producer Pechiney for a system analyzing faults in cast aluminum.

LEXICON BIDS FOR SCOPE INC.

Lexicon Corp., a developer and manufacturer of microcomputer-based data-communications products, will offer a stock-swap scheme in order to complete the acquisition of Scope Inc., a Reston, Va., electronics company specializing in bar-code systems. Lexicon says it will exchange two of its shares for each share of Scope common stock still owned by others. The Ft. Lauderdale, Fla., company now owns 43% of Scope's common stock. Lexicon executives own enough additional stock to form a controlling interest. The remainder is worth about $7.8 million.

CONVERGENT, BULL EXTEND OEM PACT

Convergent Technologies Inc. and Group Bull, Paris, have extended to 1988 their original-equipment manufacturing agreement allowing Bull to market the San Jose, Calif., company's modular NGEN work stations in Europe. Bull calls the line Questar 400. The agreement also extends Bull's right to manufacture some NGEN products worldwide. The companies are also discussing additional engineering, marketing, and manufacturing exchanges.

CORNING SETS UP SPANISH VENTURE

Corning Glass Works and Spain's telephone company, Compañia Telefónica Nacional de España SA, have formed a Spanish company to manufacture optical fiber for domestic sale and export. The Corning, N. Y., company will own 65% of Compañia de Fibra Optica Telcor SA, whose location will be decided later this month. Construction of a manufacturing facility with a capacity of 85,000 km of optical fiber annually is scheduled to begin in mid-1988.

CROW PLANS THIRD COMPUTER MART

Despite persistent industry reports that his Dallas Infomart computer center is still short of occupants after more than a year of operation, Texas real estate mogul Trammell Crow is planning a second European technology mart, in West Berlin. Construction of the first, in Paris, is scheduled to begin in June. Crow expects construction of the 400,000-ft^2 Infomart/Berlin to start in the winter. No completion date has been set.

FUQUA IS NEW AIA PRESIDENT

Rep. Don Fuqua (D., Fla.), outgoing House Science and Technology Committee chairman, will become president and general manager of the Aerospace Industries Association, the AIA announced last week. Fuqua is retiring from Congress when his term expires and will assume the post in January, replacing Karl G. Harr, president for the past 23 years. The Washington-based association represents U. S. defense and space manufacturers.

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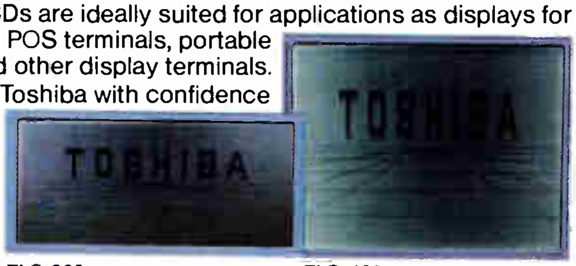
2,000 sharper-than-ever characters all on a portable LCD display.

Toshiba's newest LCD modules give you 640 × 200 dot displays in a choice of two viewing sizes. One is approximately the size of a magazine, and the other about half that size.

Both sizes put an enormous amount of information on view . . . an array of 80 characters × 25 lines. But still bulk and power consumption are at a minimum. Battery powered, these slim modules interface with various systems through LCD controller without renewing software.

Toshiba's advanced technology has also eliminated surface reflection and developed a sharper contrast which gives a brighter and easier to read viewing screen. And for low light or dark viewing an optional backlightable LCD is available.

These versatile LCDs are ideally suited for applications as displays for personal computers, POS terminals, portable word processors and other display terminals. You can also look to Toshiba with confidence for a wide range of sizes and display capacity to suit your LCD requirements.



TLC-363 *TLC-402*

Specifications

		TLC-402	TLC-363B
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W×H×D)		274.8×240.6×17.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		−20° – 70° C	−20° – 70° C
Operating Temperature		0° – 50° C	0° – 50° C
Supply Voltage	VDD	7 V	7 V
	VDD − VEE	20 V	20 V
Input Voltage		0≦VIN≦VDD	VSS≦VIN≦VDD
Recommended Operating Conditions			
Supply Voltage	VDD	5±0.25V	5±0.25V
	VEE	−11±3V Var.	−11±3V Var.
Input Voltage	High	VDD − 0.5V min.	VDD − 0.5V min.
	Low	0.5V max.	0.5V max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		3	3
Viewing Angle		15 – 35 degrees	15 – 35 degrees

Design and specifications are subject to change without notice.

TOSHIBA

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