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APRIL 7, 1986

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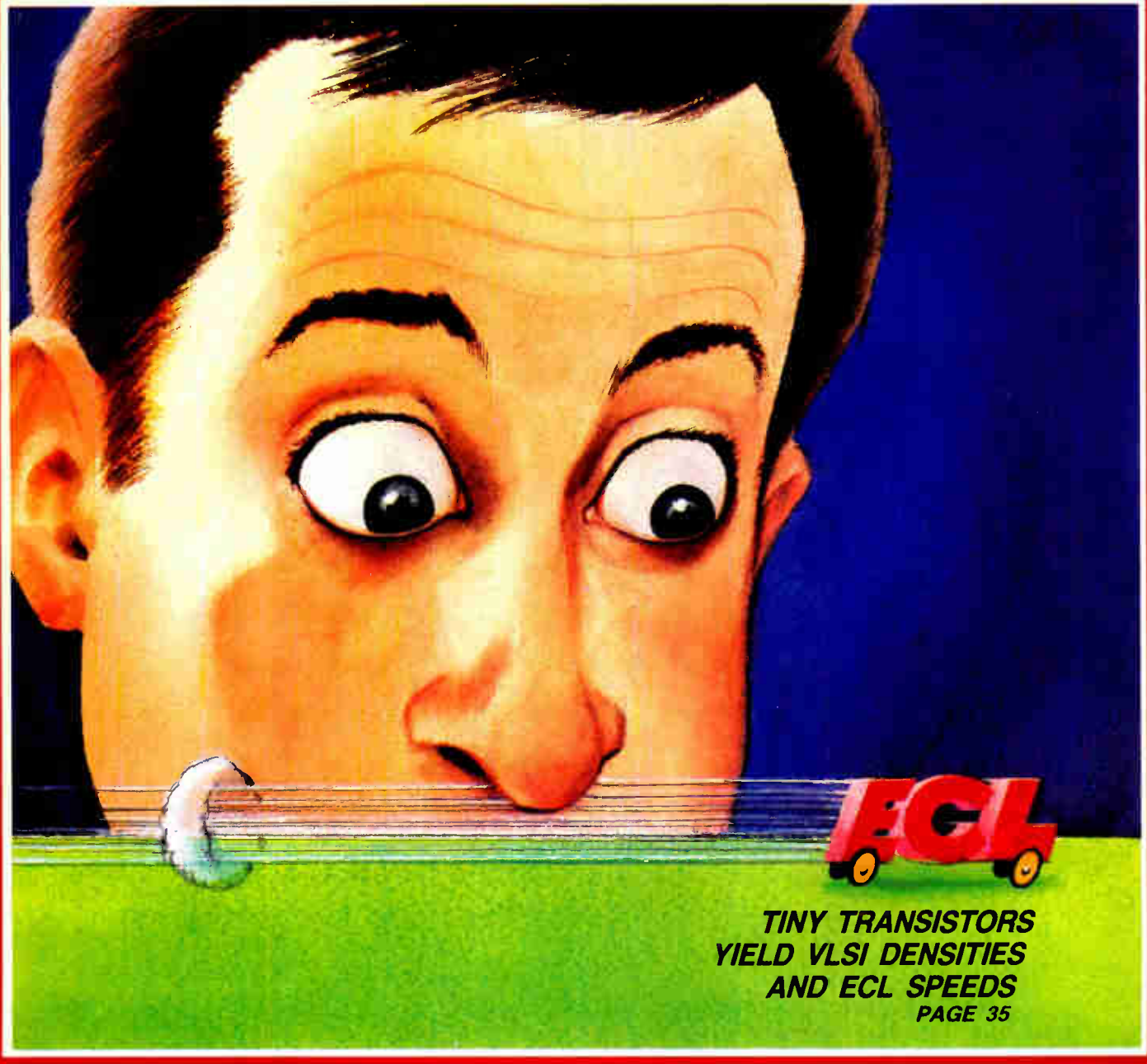

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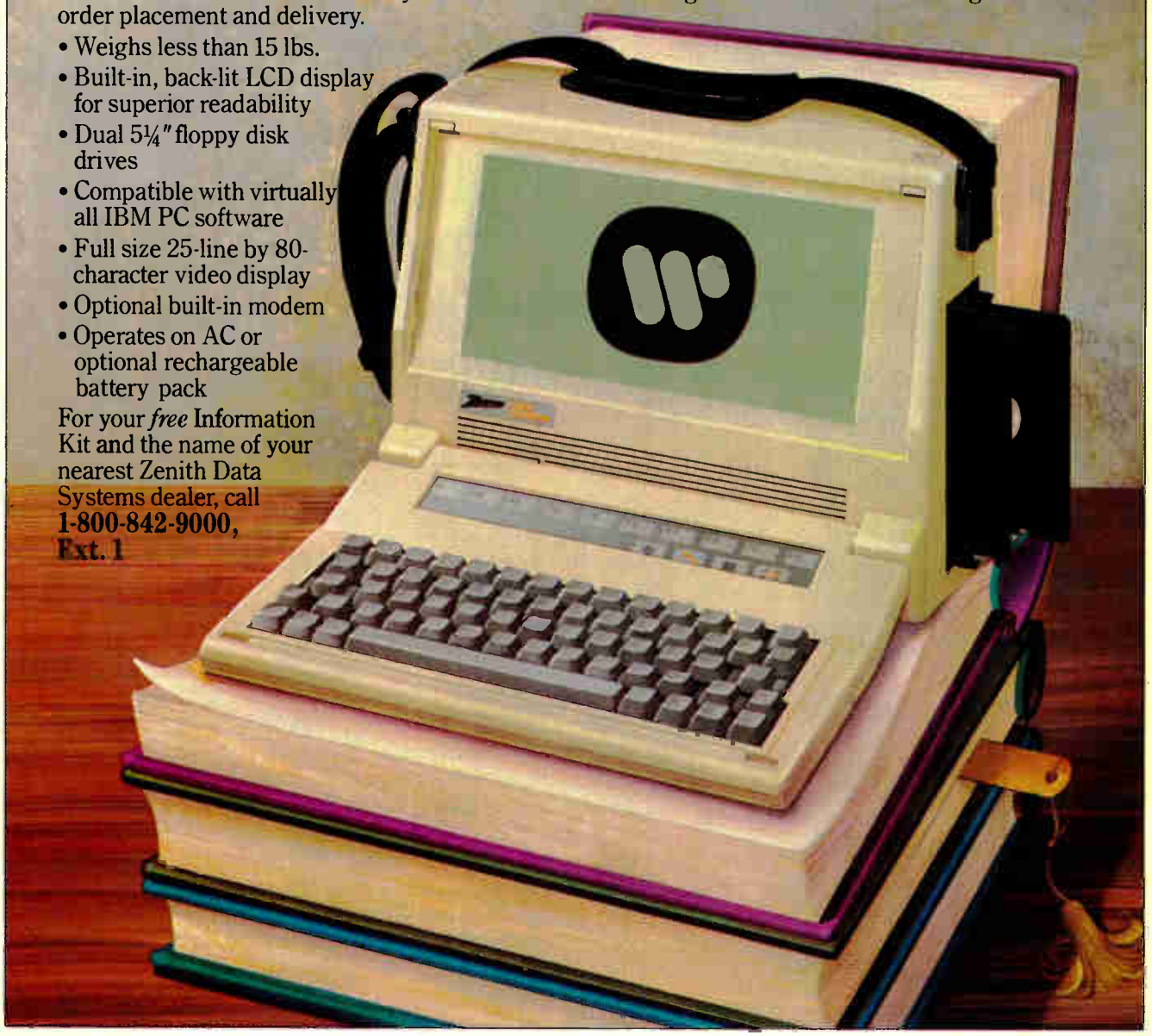

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Electronics

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To most Americans and Europeans, Tokyo is Japan. The capital is, after all, the world's largest city as well as a global commercial and financial center. But anyone who has spent any time in the island nation, either as a tourist or on business, learns quickly enough about the distances between Tokyo and the other major cities such as Kyoto and Osaka. In fact, Japan's northernmost island, Hokkaido, is closer to the Soviet Union than it is to Tokyo.

For Charlie Cohen, who in January passed the 20-year mark as *Electronics'* bureau manager in Tokyo, such ignorance of Japan's geography can make it difficult to meet what turn out to be impossible deadlines.

COHEN: To the well-traveled editor, Japan is not just Tokyo.

"Japanese executives don't like to answer questions over the phone or be interviewed on the spur of the moment," the Brooklyn native explains. "It's just not the way the Japanese do things. So when a New York editor assigns me to do a story and wants it the next day, he doesn't realize that not only must I make appointments, but sometimes I have to spend most of the day traveling just to get to the source and back to the office."

His news story about silicon carbide materials for FETs, in the section beginning on p. 14, sent him to Tsukuba. But for the Probing the News about Japan's supercomputer progress, on p. 42, Charlie had to make several trips.

But travel aside, working on the supercomputer story enabled him to confirm that at least some things in the Japanese computer industry haven't changed much—for example, the chronic weakness in software. "This was brought home to me when I was talking to the people at Tokyo University about their supercomputer," Charlie recalls. "They said that they were generally pleased with their Hitachi S810-20 because there has been no downtime in three years. But there was some disenchantment with its Fortran compiler.

"So Hitachi's short-term goal is to develop a better one, meaning the company has to put off work on the other operating systems or languages that are starting to appear in the U. S. And that's a gamble, especially because Cray's Unix compiler could become the future de facto standard."

And Charlie turned up a company that has ordered a Cray as well as a Fujitsu to be used by its multiple businesses. The outfit, called Recruit Co., is engaged in several pursuits, including one rather curious task: it is trying to remake Japan in the American image by encouraging employees to switch companies in midcareer.

"And that," says Charlie, "*really* isn't the Japanese way."

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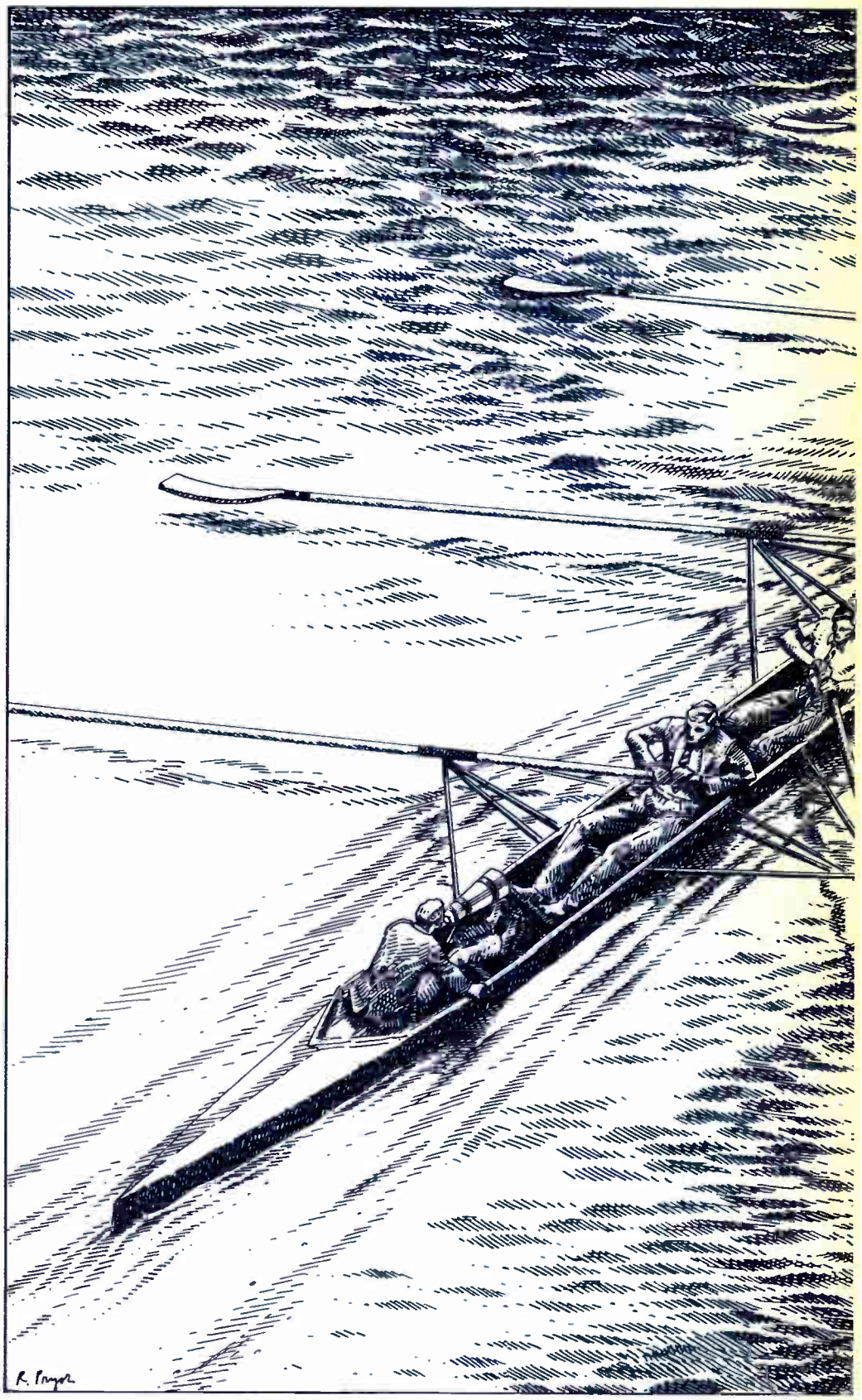

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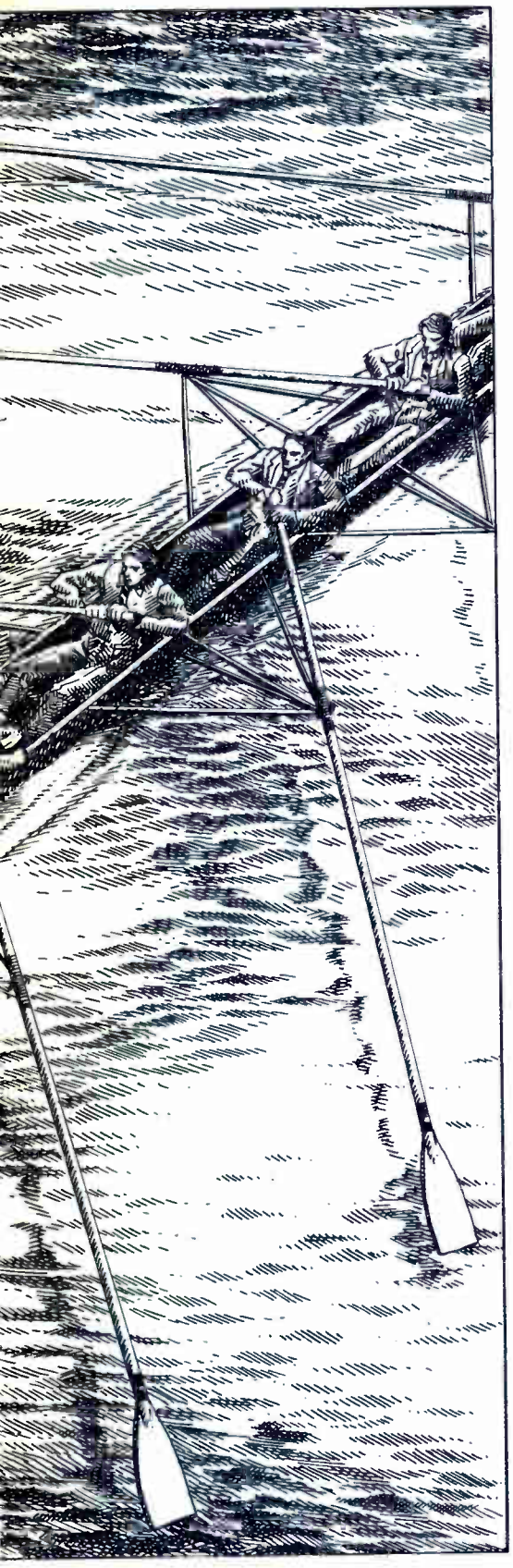

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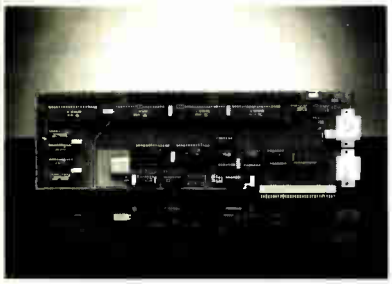

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BOOKS

SILICONNECTIONS: COMING OF AGE IN THE ELECTRONIC ERA

Forrest M. Mims III
McGraw-Hill Book Co.
$16.95/208pp

Forrest Mims stands right in the tradition of Alexander Graham Bell—to whose memory he dedicates his book—and all other scientists and inventors who did it their way. He has written a quirky, warm, fascinating book about his private wars with the Air Force Weapons Laboratory and Bell Labs, as well as development of the Altair 8800, which sparked the beginnings of the personal computer industry, to mention only the more public aspects of Mims's career. Because he is as adept at the keyboard as at the bench—*Siliconnections* is his 50th book—there is a great deal of information about electronics magazine empires; the two chapters on the silicon press should be required reading for every high-tech journalist.

This is an insider's book that can be enjoyed and understood even by readers whose contact with the industry stops at the control panels of their microwave ovens. Because the last section is titled "Silicontinuations," one can hope that Mims plans further installments of his siliconfessions.

THE MICROELECTRONICS INDUSTRY

Joseph LaDou, MD, ed.
Hanley & Belfus
$22/198pp

Important health issues are surveyed in *The Microelectronics Industry,* volume 1, number 1 of the Occupational Medicine quarterly review series. LaDou presents analyses of labor statistics indicating that employees involved in semiconductor and electronic-component manufacture in the U.S. report a much higher incidence of occupational illness than their counterparts in other manufacturing industries. Contributed articles discuss health hazards related to substances such as toxic gases and solvents and review risks from carcinogens and radiation exposure in the workplace.

The editor is acting chief of the Division of Occupational and Environmental Medicine at the University of California School of Medicine, San Francisco.

COMPUTER INDUSTRY ABSTRACTS

Data Analysis Group
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This quarterly market analysis started in January 1986 tracks computers, storage devices, printers and terminals, data-communications equipment, and software. Information is abstracted from over 150 major computer and business publications and presented in a form suitable for inclusion in reports and presentations. *Computer Industry Abstracts* is available in both hard copy and Lotus 1-2-3 formatted data-disk form from the publisher at 8263 Vista Dr., La Mesa, Calif. 92041.

1986 PRODUCT HANDBOOKS

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Intel has just released its annual update on its microprocessors, microcommunication products, memory components, and systems. The handbooks contain data sheets, application notes, article reprints, and other design information; the free *Product Guide* is an overview of all products. The company's toll-free order number is (800) 548-4725.

CD ROM: THE NEW PAPYRUS

Steve Lambert and Suzanne Ropiequet, eds.
Microsoft Press
$34.95/619pp

The portability and low cost per bit of the compact-disk read-only memory justify calling it "the new papyrus," says Bill Gates of Microsoft Corp. in his foreword to this collection of papers. The occasion was Microsoft's first international conference on CD ROM; Microsoft has formed a group within the company to explore this technology, and contributors come from inside and outside the electronics industry [see *Electronics,* Sept. 16, 1985, p. 26 for an overview of CD ROM's development position].

The volume is divided into sections on the CD system, producing CD ROM, design considerations, applications, and CD ROM publishing. There are no discouraging words here; the question is not whether we will do this but how far it will take us.

PICK FOR USERS

Martin Taylor
Computer Science Press/ Blackwell Scientific Publications
$17.95/183pp

The Pick operating system has its supporters in a specialized branch of the business-software market, and this handbook may increase their number. The author, who is UK technical support manager for Unison Technology plc, guides nonspecialists through the use of examples and practical information. He describes data-base structure and the system editor, the print spooler and security in Pick, and concludes by advising how to "keep it simple" in Proc, Pick's job-control language.

World Radio History

TECHNOLOGY NEWSLETTER

NEW PROCESS HALVES COST OF MULTILAYER PC BOARDS

By marrying polymer thick-film technology with conventional plated-through-hole techniques, a Bensenville, Ill., pc-board maker claims it can nearly halve the cost of a multilayer pc board—to between 16¢ to 20¢ per square inch for a four-layer board, compared with 30¢ to 40¢ for a conventional board. West-Tronics Inc. starts with a standard double-sided copper-laminated glass epoxy board and etches away the copper around the pad areas, separating them from the copper ground planes. The company puts down successive alternating layers of screened conductive polymer ink traces (which connect to tails on the copper pads) and insulating polymer inks to separate the layers. Then conventional drilling and through-hole-plating techniques are used to finish the job. The boards are cheaper to make because expensive lamination and etching steps are not needed, says West-Tronics president Clare Turek. Based on three months of testing, the firm says reliability should match or exceed conventional boards. About 150 companies, including AT&T and Motorola, have requested prototype boards since the technology was unveiled late last month. □

TI TO ROLL OUT DEVELOPMENT TOOLS FOR IBM'S TOKEN NET

System integrators and programmers who want to dissect software running on IBM Corp.'s Token-Ring Network to make sure their own will work soon will get help from Texas Instruments Inc. Later this month, TI will introduce two development boards that will turn IBM Personal Computers and compatibles into software-evaluation stations for the local-area network. The "network scope" boards enable users to copy all frames off the network and store them for evaluation. One adapter board will fit 8088-based PCs; the other will be for 80286-based IBM PC AT models and compatibles. □

HIGH-DEFINITION TV GETS A BOOST FROM SONY

High-definition TV got a big lift when Sony Corp. announced last week that it had developed a 41-in. Trinitron cathode-ray tube. Sony developed the tube in accordance with the Hi-Vision HDTV system promoted by the Japan Broadcasting Corp. for High Definition Video System display. Because it has a maximum horizontal resolution of 1,861 phosphor trios (each trio is composed of red, green, and blue dots), Sony says the tube can be used in computer-aided design and manufacturing work-station displays. The 41-in. diagonally measured tube features a near-flat surface and virtually square screen corners. HDTV has been making steady progress since it was proposed by the International Radio Consultative Committee in October 1985, says Sony. □

SIEMENS JOINS GROUP PUSHING EUROPEAN MAP STANDARD

Europe's counterpart to the Manufacturing Automation Protocol standard took on a more solid ring when it signed on Europe's No. 1 producer of industrial-automation equipment, West Germany's Siemens AG. Like MAP, the European Communications Network for Manufacturing Applications aims to establish protocol profiles for automated-manufacturing networks and to test and evaluate them in practical applications. CNMA is a project of the European Communities' Esprit research and development program. Besides Siemens, participating companies include automakers BMW and Peugeot; aerospace manufacturers British Aerospace and Aeritalia; computer makers Nixdorf Computer, Bull, Olivetti, and the UK's General Electric Co. Because of its activities in industrial automation are worldwide, Siemens will also continue to support MAP, which is being championed in the U. S. by General Motors Corp. and the National Bureau of Standards. □

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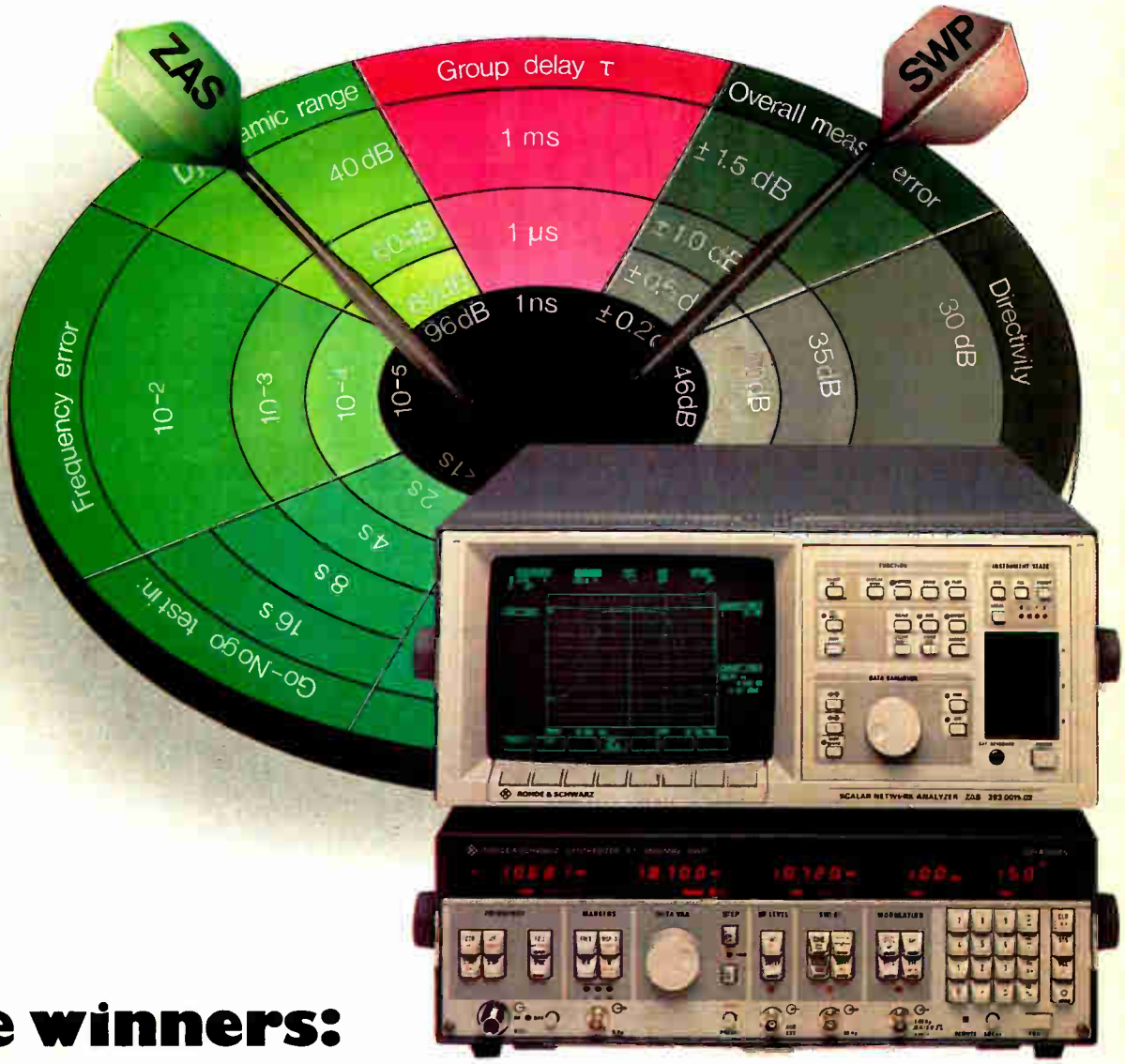
Scalar Network Analyzer ZAS & SWP



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ELECTRONICS NEWSLETTER

SHARP AND PHILIPS MAY TEAM UP TO MEET COMPACT-DISK DEMAND

Sharp Corp. of Japan and Philips of Eindhoven, the Netherlands, may soon be working together to meet the surging demand for compact-disk players. The two companies are negotiating a deal for cross-licensing and technology transfer that would give Philips the technology to manufacture semiconductor laser diodes for CD player pickups; in return, Sharp would get the know-how for manufacturing the aspherical plastic lenses also needed in the pickups. Sharp is the leading manufacturer of semiconductor lasers for CD players in Japan, with a 70% share of that market. It now produces 800,000 lasers per month and expects further production increases later this year. In 1985, Japan's domestic market for CD players was four times its 1984 size, and its exports grew to more than five times their 1984 level. The domestic market for 1986 is expected to almost double to more than 2 million units; meanwhile, exports will grow more than 1.5 times to reach more than 4.7 million units. □

MACHINE VISION WILL BOOM, BUT HOW MUCH?

Machine-vision sales will zoom upward between now and 1990, but not as fast as predicted by most financial analysts and market-research outfits. That's one conclusion of a report put out recently by the Automated Vision Association that is billed as the first industry-generated study of the business. The AVA report puts 1985 machine-vision sales at $58 million and projects annual growth of 62%, to $457 million in 1990. That's well below most figures generated by other industry watchers, some of whom have predicted a $1 billion market by the end of the decade. However, the study talks in billions only when predicting sales of systems that incorporate machine vision, which the AVA, a trade group with 40 firms as members, says will grow from $188 million in 1985 to more than $2 billion in 1990. □

MICROSOFT AND EX-AGENT ASCII TO COOPERATE IN JAPAN

Microsoft Corp. shed its long-time Japanese partner ASCII Corp. early this year, but the two will continue to work together in many areas after the Bellevue, Wash., software developer starts up its wholly owned Japanese subsidiary, Microsoft KK, on May 1. As expected [*Electronics*, Feb. 17, 1986, p. 46], ASCII will get worldwide marketing rights and provide support for the jointly developed MSX home computer; Microsoft will retain all other systems and applications software and languages that it developed in the U. S. To maintain the same high profile it had in Japan during the eight years of its relationship with Tokyo-based ASCII, Microsoft intends to set up research and development facilities at its Japanese subsidiary. Microsoft KK will adapt and extend the parent company's products for the Japanese market as well as create new products. □

DEMAND FOR DRI'S GEM COULD SOAR BECAUSE OF IBM DEAL

Digital Research Inc., Monterey, Calif., may have struck gold with an agreement whereby IBM Corp. will distribute DRI's five GEM graphics-oriented applications packages for IBM's Personal Computer family. DRI president John Rowley says it's hard to estimate the potential, but considering IBM's huge direct-sales force, the deal should "very dramatically accelerate demand for GEM." Already, GEM applications have an installed base of 50,000 in the PC market, primarily in Fortune 1,000-type companies, which are IBM's forte. DRI already has the applications in a 3½-in. floppy-disk format for the Atari ST computer, so packages for the IBM PC Convertible, released last week (see story, p. 46), should not be long in coming. □

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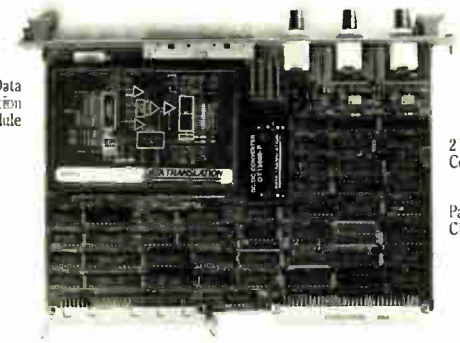

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PRODUCTS NEWSLETTER

NCR, CADNETIX BUNDLE STANDARD-CELL DESIGN SOFTWARE

A new standard-cell chip-design kit developed jointly by NCR Corp.'s Microelectronics Division, Fort Collins, Colo., and Cadnetix Corp., Boulder, supports 3- and 2-μm CMOS processes. The package, which both companies will begin marketing in midyear, runs on Cadnetix's 68010-based engineering work stations. Its licensing cost is $7,000. NCR provided a VLSI interconnection and timing-analysis tool set as well as its Sentpex test-pattern extractor. Cadnetix provides interface software, including the Tegas design language and a netlist generator. The software provides a path from 3-μm single-level-metal to NCR's 2-μm double-level-metal CMOS. □

NEC INFORMATION SYSTEMS TO UNVEIL PC AT CLONE EQUIPPED FOR CAD

Look for NEC Information Systems Inc. to unveil at this month's Comdex show in Atlanta an enhanced IBM Corp. Personal Computer AT compatible that the company equipped for computer-aided design. The APC IV, based on the 8-MHz 80286, will cost 10% to 15% less than the $5,295 PC AT, and will come with a choice of three graphics options—the highest having a resolution of 1,120 by 750 pixels. The standard APC IV is equipped with 640-K bytes of RAM and offers a choice of 360-K-byte or 1.2-megabyte floppy-disk drives and 20- or 40-megabyte 5¼-in. Winchester drives. Exact delivery dates from the Boxborough, Mass., company have not been set. □

PHILIPS ANALYZER COMBINES HIGH SAMPLING RATE AND CHANNEL CAPACITY

Philips will be unveiling more than a low-cost oscilloscope (see stories, pp. 39 and 55) at this week's Industrial Fair in Hanover, West Germany. The company will also introduce a high-performance logic analyzer that combines high channel capacity and a high sampling rate. The PM3570, which can support 8-, 16-, and 32-bit processors, is a modular system whose maximum setup yields 83 state-analysis channels plus 32 100-MHz timing-analysis channels for software and hardware development. Alternately, the 32 timing channels can be configured as eight 400-MHz channels for fast sampling—speedy enough to catch glitches down to 5 ns in real time. The PM3570 will sell for between $8,500 and about $20,000. □

MICRO LINEAR CORP. ENHANCES ITS LINEAR CAD SOFTWARE

Micro Linear Corp. is making the lives of linear-circuit designers easier with an enhanced version of its software program that turns an IBM Corp. Personal Computer/XT or PC AT into a linear-design work station. The new program, called Linear CAD II, features an additional 12 macrocells, as well as the device models for the San Jose, Calif., company's 12-V high-performance linear bipolar process. Priced at $10,000, Linear CAD II includes a schematic capture program with a graphics editor, hardware compiler, netlist processor, the PSpice simulation software, and the macrocell library, which totals 29 cells. It is available now. □

IMAGE PROCESSOR CAN WORK AT SPEEDS FASTER THAN REAL TIME

Imaging Technology Inc.'s series 151 image processor lets users process a portion of an image at speeds faster than real time. The image-processing industry considers real time to be 33.3 ms. The Woburn, Mass., company's VMEbus-based system, which connects to an IBM Corp. Personal Computer AT, can process pixels at 10 MHz—faster than RS-170 video standards. For example, a quarter of an image can be processed in 8 ms. The 151 will be available in 60 to 90 days for $11,495 to $15,490. □

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Electronics

STARTUP IS FIRST TO MARKET WITH SUBMICRON CMOS CHIPS

PERFORMANCE SEMICONDUCTOR'S PARTS HAVE 0.8-MICRON CHANNELS

SUNNYVALE, CALIF.

Performance Semiconductor Corp. is the first to enter the market with submicron CMOS parts. The Sunnyvale startup is offering a kit of parts designed with 0.8-μm effective channel lengths. Typical functional delays are about 3 ns, or "faster than FAST," quips founder Thomas A. Longo, citing Fairchild Semiconductor Corp.'s bipolar technology, whose best is about 4 ns.

But just as interesting as its products is the fact that Performance Semiconductor has put its fabrication in place at relatively little cost. And although it is building a military-standard microprocessor, the company has bootstrapped itself without the financial benefit of being a part of the Defense Department's Very High Speed Integrated Circuits program.

Dubbing its technology PACE—Performance Advanced CMOS Engineered—the company is first introducing a family of octal bus-interface parts. Its sights are set on high-performance static memories, logic, and microprocessors for the military and commercial markets. One potential customer is Cray Research Inc. of Minneapolis—Longo has been on Cray's board since 1974.

Longo, president and chief executive officer, came from Fairchild, where he was manager of the Palo Alto Research and Development Laboratories and a corporate vice president of Schlumberger Ltd., Fairchild's New York parent. He chose to found a CMOS-only company because "this is the first time in history you can do everything you want to do in one technology." Longo says CMOS is that technology because, for one thing, it avoids the power dissipation at high gate densities which he says "will kill" emitter-coupled logic.

PACE provides greater device density than available CMOS technology, because of a 2.7-μm metal pitch, which compares with typical 1.2-μm processes having 4-μm metal pitches. The 0.8-μm channels allow Performance Semiconductor to design devices with 500-ps loaded internal gate delays. The unloaded internal gate delays are 200 ps.

The bus-interface parts are available in an $80 PACE kit, which consists of preliminary data sheets and two each of the following parts: a gated octal latch, a D-type flip-flop, a buffer/line driver, a transceiver, and a 256-by-4-bit 12-ns static random-access memory. The transceiver and buffer have 64-mA sinking output current and the flip-flop has a toggle rate of more than 250 MHz. One of the company's flagships will be a 64-K SRAM. The small geometries will allow Performance Semiconductor to put 650 gross 64-K SRAM dice on a single 6-in. wafer. First silicon for the 16-K-by-4-bit part was debugged in February.

The other star this year will be a Fairchild-9450-equivalent 16-bit microprocessor that executes the DOD's military-standard 1750A instruction set. The PACE1750A will be available in 20- and 30-MHz versions for military temperature ranges, with the faster version performing at about 2 million instructions/s under the Air Force Digital Avionics Information Systems benchmark. A 40-MHz commercial-temperature part is under development.

CLEAN. Performance has a Class 2 clean room.

DROP-IN ALTERNATIVES. Hoping to take market share away from Fairchild's 1750A line, Performance Semiconductor is making its parts as drop-in alternatives to Fairchild's 9450 bipolar parts. The company has just completed design and will take it into silicon next month. At half the die size of the Fairchild part, Longo says, it will net a higher profit margin.

Performance Semiconductor has been operating off of $18 million raised in its October 1984 initial financing. This includes funding from principal individual investors Longo and Seymour Cray, and from U.S. venture capitalists led by Northwest Venture Partners and Brentwood Associates. It also includes a $6.6 million lease line from Westinghouse Electric Corp. for capital equipment.

On that kernel of investment, the company built one of the world's most advanced semiconductor production facilities. A Class 2 fabrication area houses a 6-in. CMOS dry-etch fab line capable of generating revenue of $60 million a year, Longo says. It is surrounded by a Class 100 room for support equipment. The money has also purchased about $1 million in test equipment and $1 million in computer-aided design equipment.

Performance Semiconductor uses a two-layer metal process on an epitaxial substrate. Ion implantation is used six or seven times during the process, and 1-μm 1:1 steppers are employed.

Though the parts may sound esoteric and the production specialized, Longo smiles when he projects revenue for 1987 "in the several tens of millions of dollars." *–Ere Bennett*

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SEMICONDUCTORS

SILICON CARBIDE FETs AIM FOR 300°C OPERATION

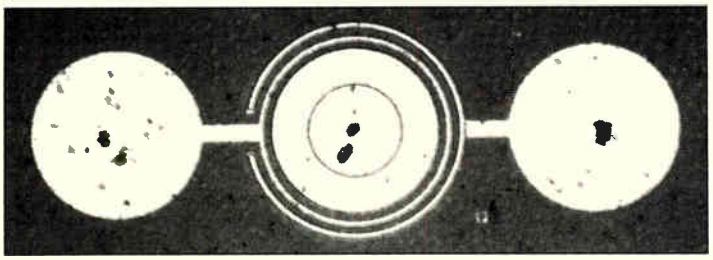
TSUKUBA, JAPAN

Researchers at a Japanese government lab have succeeded in building FETs on cubic-lattice silicon carbide layers atop a silicon substrate. Although little testing has been done, it is expected that the SiC FETs will operate at ambient temperatures above 300°C, suiting them to special market niches where high-temperature capability is required. SiC's characteristics may also suit it to fabrication of power devices.

Three types of FETs were developed by two teams at the Electrotechnical Laboratory in Tsukuba as part of a project on future electron devices [*Electronics*, Sept. 8, 1983, p. 94]. The teams developed experimental Schottky-gate FETs, p-n junction FETs, and MOS FETs, all three types conventionally available in silicon. Bipolar SiC devices have not been built.

Operation of all three types of FETs was confirmed at room temperature; the MOS FETs were also confirmed at 150°C. Ohmic contacts and gate junctions have been checked at 300°C, but device characteristics have not yet been measured at this temperature. The researchers emphasize that the SiC substrates and the devices themselves are at a very early stage of development.

The overall leader of the project, Masatoshi Ono, is head of the Electrotechnical Laboratory's Space Environment Engineering Section. His space-environment interests in SiC are clear: spacecraft encounter extremes of temperature in space. But the major use of the devices in Japan is expected to be in high-power applications and in engine compartments of cars and airplanes. In the U. S., uses might include down-hole drilling equipment and military and other gear for extreme environments.



HOT ONE. Japanese researchers have built MOS FETs on layers of silicon carbide atop a silicon substrate; they expect them to work at 300°C.

Electron mobility in SiC is about the same as in silicon, but saturation velocity is twice as high, says Yutaka Hayashi, head of the lab's Semiconductor Device Section, where the MOS FET was made. This means SiC should be able to withstand twice the voltage for equal device dimensions. Its thermal conductivity is also three times that of silicon; both factors are important in power devices.

The FETs were fabricated on cubic-lattice SiC, a form of the material that can be epitaxially grown on silicon wafers. Wafers can be made in a manner similar to silicon-on-sapphire wafers. Previously, FETs, bipolar transistors, and light-emitting diodes have been fabricated on alpha SiC, which has a hexagonal lattice, but these FETs are the first devices fabricated on cubic SiC. Alpha SiC must be grown by a Czochralski crystal-pulling process. So far, this difficult process has yielded only small ingots.

BUFFER LAYER. Epitaxial growth of the SiC layers on 2-in. silicon wafers and fabrication of the two junction-type FETs took place in the lab's Electronic Refractory Materials Section under the supervision of Sadafumi Yoshida. The lattice-constant mismatch between silicon and SiC is extremely high: the lattice constant is 5.4 Å for Si and 4.3 Å for SiC. Therefore, a thin buffer layer of polysilicon carbide is used to form a transition between the materials. Epitaxial growth of the active layer is a vapor-phase heteroepitaxial process on the polycrystalline layer.

Dopants are used during the growth process to form n- or p-type layers. The experimental devices were formed in n-type layers on top of p-type layers. Reactive-ion-etching techniques were developed to pattern the extremely hard and chemically inert SiC.

The junction FETs were built using aluminum ohmic contacts; the Schottky device also uses a gold gate. To make the aluminum-gate MOS FETs, polysilicon source and drain contact fabrication was followed by thermal oxidation of gate oxide. *–Charles L. Cohen*

INTERNATIONAL TRADE

JAPAN-U. S. CHIP TALKS ARE STILL ALIVE

WASHINGTON

Prospects for a negotiated settlement on semiconductor trade between the U. S. and Japan are still alive despite the fact that the U. S. suspended the latest round of talks on March 28, say industry and government officials on both sides. Indeed, talks dealing specifically with U. S. access to the Japanese market could resume later this month, after the scheduled visit to Washington by Japanese Prime Minister Yasuhiro Nakasone April 12-14.

Resumption of trade talks aimed at increasing U. S. access to the Japanese semiconductor market is seen as crucial because pressure continues to build in Congress for retaliatory legislation. Meanwhile, U. S. officials say they will continue investigations into unfair-trade complaints against the Japanese.

The U. S. asked for the suspension to reassess its position. A spokesman for the Office of the U. S. Trade Representative says a firm date hasn't been set for resumption. He denies reports that talks could resume this week, but adds, "We're not ruling out this month."

LACK OF PROGRESS. "This is just another round in a typical U. S.-Japan negotiation," says a U. S. government official in Tokyo. "It's much too early to say that these talks have broken down." U. S. industry officials add that the faltering talks are symptomatic of a general lack of progress in negotiations that spawned the trade complaints.

Suspension of the Washington talks followed a recent private meeting between U. S. executives and Japanese industry and government officials in Los Angeles. During that meeting, the five leading Japanese companies—Fujitsu, Hitachi, Mitsubishi, NEC, and Toshiba—offered to increase their purchases of U. S. semiconductor products by 20% of their overall annual total by 1990.

U. S. executives reportedly did not reject the offer, which includes a 20% increase in purchases by second-tier Japanese companies by an unspecified date. But they did reiterate their position that genuine market access, not a "managed market share," is its goal.

The Japanese proposal "is a step forward for those five companies," says George Scalise, chairman of the Semiconductor Industry Association's public policy committee. Nevertheless, Daryl Hatano, SIA's government affairs man-

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ager, says an investigation of unfair trade practices filed last July will proceed "full speed ahead."

The administration had hoped to resolve the trade dispute, which also includes widening U.S. access to the Japanese telecommunications market, before Nakasone arrives for three days of talks beginning Saturday. The administration is under increasing bipartisan pressure from Congress to make trade a high priority during Nakasone's visit.

Just as trade talks were getting under way in late March, 53 senators, including majority leader Robert Dole (R., Kan.), and minority leader Robert Byrd (D., W.Va.), sent a letter to President Reagan warning that "stopgap solutions" would increase the chances of Congress passing protectionist legislation. The president has repeatedly opposed such free-trade barriers.

"We have not retaliated against the Japanese" for limiting U.S. access, notes Ira H. Goldman, an aide to Sen. Pete Wilson (R., Calif.), a member of a congressional working group on semiconductor trade. "I think this is the case to do it." One retaliatory measure being considered is the imposition of quotas on Japanese semiconductors, he adds.

But industry officials seek a more permanent solution. Says Hatano, "No agreement sure beats a bad agreement."

–George Leopold and Michael Berger

DATA PROCESSING

AT LAST: PARALLEL-ENGINE BENCHMARKS

ARGONNE, ILL.

Relief is in sight for scientific computer users who face the confusing task of evaluating the widening array of new multiprocessor and supercomputer architectures available today. By midyear, the National Bureau of Standards plans to begin electronic distribution of a set of benchmark programs aimed at comparing the performance of various parallel architectures.

The new service could help meet a crying need in the industry. Upwards of three dozen vendors and startups have recently rolled out new machines that aim to provide supercomputer-like punch for a fraction of the price by harnessing the power of multiple processors working in parallel [*Electronics*, Oct. 28, 1985, p. 32]. But the problem comes in finding a way to effectively compare the performance of the machines, which encompass almost indescribable diversity in their architectural approaches.

"There are machines which have shared memory and communicate across a bus, all the way to the other end of the scale to machines that have local memory and send messages back and forth to do their communication. And in that context, it's very hard to come up with a benchmark that's fair for everybody," says Jack J. Dongarra, scientific director of the Advanced Computer Research Facility at Argonne National Laboratory.

Dongarra is the author of the Linpack codes, a package of about 400 Fortran subroutines for solving dense systems of linear equations. Available at no charge over the U.S. Defense Department's Arpanet, the Linpack routines have within the past couple of years become perhaps the best-known benchmark for comparing performance across a broad range of computer systems.

"Linpack is the most widely used measure and it's the fairest, because the vendor must run it exactly as defined by Jack, and the vendor or the software developer also has an option to use assembly language for those computational-intensive tasks, to really show off performance," says Wayne A. Ray, director of Cyberplus Parallel Processing at Control Data Corp., Minneapolis.

TESTS THE GAMUT. One attraction of Linpack is the fact that it offers a performance comparison for solving a kind of problem (full of floating-point operations) that is frequently encountered in scientific computing, industry officials point out. In addition, Linpack has run on more than 100 different computers, ranging from the largest supercomputers down to personal computers.

Dongarra has been collecting data for a decade on the amount of time that a machine requires to execute the Linpack routines; he publishes an informal report and updates it with information on new machines as it becomes available. In an effort to accommodate a variety of architectures, Dongarra recently added two versions of the Linpack routines using larger matrixes and allowing for more vendor freedom in how the problem is solved. One version offers a matrix-vector approach to solve equations for a 300-by-300 matrix (table). Compared with the original Linpack routines involving straight vector operations on a 100-by-100 matrix, the matrix-vector approach better enables "advanced scientific computers," such as high-end vector supercomputers and some of the new breed of parallel machines, to show their stuff, Dongarra says.

HOW ONE BENCHMARK RANKS THE SUPERCOMPUTERS

Computer	Fortran compiler	Megaflops*
Cray X-MP-4	CFT (coded matrix-vector routines)	480
Cray X-MP-4	CFT (coded Isamax)	356
NEC SX-2	Fortran 77/SX	356
Cray X-MP-2	CFT (coded Isamax)	257
Fujitsu VP-200	Fortran 77 (using compiler directives)	220
NEC SX-1	Fortran 77/SX	207
Fujitsu VP-200	Fortran 77	183
Cray X-MP-1	CFT (coded matrix-vector routines)	171
Cray X-MP-2	CFT	161
Hitachi S-810/20	FORT77/HAP	158
NEC SX-1E	Fortran 77/SX	140
Cray X-MP-1	CFT (coded Isamax)	134
Cray X-MP-1	CFT	106
Cray-1-M	CFT (coded Isamax)	83
Cray-1-S	CFT (coded Isamax)	76
Cray-1-M	CFT	69
Cray-1-S	CFT	66
Floating Point Systems FPS-264	FO2, F77 (coded matrix-vector routines)	33
Control Data Corp. Cyber 205	ftn 200, option 1 (coded matrix-vector routines)	31
IBM 3090 model 200/VF	VS Fortran V2 (coded matrix-vector routines)	27

*This benchmark uses standard linear-equation software in a Fortran environment and a matrix-vector approach.

SOURCE: ARGONNE NATIONAL LABORATORY

A number of vendors use Linpack benchmark results in marketing their parallel-processing machines, along with other popular benchmarks such as the Livermore loops developed at the Lawrence Livermore National Laboratories. But like other benchmarks, Linpack measures performance for only a particular class of problem and was not specifically developed with parallel processing in mind.

For his part, Dongarra is in the early stages of developing a separate benchmark aimed more squarely at measuring performance of high-end vector- and parallel-processing machines. Similar work is under way at a number of other research centers. In general, "there's a tremendous need for more benchmarks," says Control Data's Ray.

The situation could ease this summer, thanks to the NBS effort to collect and distribute benchmarks specifically for

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comparing machines with different parallel architectures. The NBS solicited donation of programs from the scientific community last fall, says Kenneth Dymond, the computer scientist in charge of the project at the NBS Institute for Computer Science and Technology in Gaithersburg, Md.

FREE ACCESS. So far, 15 benchmarks have been collected. The NBS plans to make the suite available at no charge on Arpanet by June. It will use software Dongarra developed to give a user access to the desired benchmark without human intervention, Dymond says. The NBS service should help users decide which vendors' machines might be best for a given application, he notes, because it will offer benchmark programs for solving a variety of computer jobs. The set so far contains code aimed at measuring a machine's performance in areas that include fluid dynamics, artificial intelligence, image processing, and general scientific computing.

The NBS plans later to offer the benchmark software over networks other than Arpanet, probably including a new net planned by the National Science Foundation. Known as NSFnet, it will be similar to Arpanet but will be aimed at university researchers, says John W. Connolly, NSF director of advanced scientific computing. He expects about 100 universities on line when the network goes up about a year from now.

Schools tied into the net will include those the NSF recently funded in a $200 million program to establish five national centers for supercomputer research. "One of the things we want to do as soon as we can," says Connolly, "is get the five centers involved in benchmark studies." *–Wesley R. Iversen*

COMPONENTS

PHILIPS TO OFFER SIGNAL PROCESSOR

EINDHOVEN, THE NETHERLANDS

Another major player is jumping into the exploding digital signal-processor market. The move is important for two reasons: The player is Philips, Europe's leading chip maker, and its new DSP is super fast. The company says its SP50 family of 2-μm single-chip CMOS DSPs is capable of 8 million instructions/s.

Benchmarks for standard algorithms such as filters and fast Fourier transforms "show a two- to sixfold improvement in performance over other single-chip DSPs," claims Ton van Kampen, Philips's DSP strategic marketing manager. Besides enhancing existing uses, he says "the SP50 brings processing power to a whole range of new applications that were difficult, if not impossible, to implement with earlier single-chip devices."

While Motorola's new DSP [*Electronics*, March 10, 1986, p. 30] runs at 10.25 million instructions/s, Philips has a structure that will allow a maximum throughput of 48 million primitive operations/s with highly efficient programming, van Kampen says. This is because each instruction contains fields that control some action in up to six different functional blocks for these DSPs.

The family has two members so far: the PCB5010, which contains a read-only memory for the program, and the PCB5011, a ROM-less version for prototyping, small production runs, and applications requiring program memories with up to 64-K instructions. Samples of the 5011 will become available in May, with volume production to start at the end of the year. The 5010 will follow a few months later.

High throughput is possible for these DSPs because of a pipelined Harvard architecture that allows simultaneous control of functional blocks and transfer of data between blocks. Keys to this design, says van Kampen, are two 16-bit data buses, one control bus, and five functional blocks—"all operating at a degree of parallelism unmatched in other single-chip designs." Forty-bit instruction words support the parallel processing, and instruction cycle is 125 ns.

Future DSP chips with features smaller than 2 μm will have an instruction-handling capability much higher than the current 8 mips and, consequently, an operation throughput exceeding the present 48 million per second. In fact, with DSP test chips using a 1.5-μm process, Philips researchers have obtained what they consider promising results.

Thus far, van Kampen adds, systems demanding significant processing power have had to be built with multichip DSP configurations consisting of expensive power- and space-consuming components. With the SP50 single-chip processors, systems makers can cut costs as well as space and power requirements, and at the same time achieve high performance and reliability.

Applications for the new devices range from speech recognition, synthesis, and compression to telecommunications, engine control, mobile automatic telephony, and digital high-fidelity audio. Possible configurations include stand-alone DSP systems, host-controlled systems, and multiprocessor systems with DSP chips connected in parallel, in series, or both.

Programming the 5010 takes about one tenth the time it does with previous single-chip DSPs, van Kampen says. The speedup results from each functional

WHY PHILIPS IS JUMPING INTO DSP MARKET

Philips has been working overtime to get into the digital signal processor business with its SP50 family, because the market is growing so fast. Worldwide sales of all types of DSPs will reach $1.5 billion by the end of this decade, according to a forecast by Benn Electronics Publications of Luton, England.

The market researcher forecasts that general-purpose DSPs, dedicated versions, and DSP building blocks will split the market equally. Benn predicts that by 1993 the world DSP market will come to about $6.5 billion.

"We must be in DSPs because part of the microprocessor and microcontroller market will be taken over by DSPs," says Ton van Kampen of Philips, Eindhoven, the Netherlands.

Vying for shares of the DSP business is a small but growing league of semiconductor manufacturers, among them NEC in Japan; Texas Instruments, Motorola, and National Semiconductor in the U.S.; and ITT Intermetall GmbH, Thomson-CSF, and, now, Philips in Europe. The DSP club will eventually be shaken out to a few major suppliers, van Kampen believes.

Philips is convinced it will be a winner, and aspires to be among the world's top three suppliers within a few years, hoping that its DSP implementation will emerge as a standard. Its confidence rests on the know-how Philips has gained with DSPs for in-house use and dedicated to specific tasks such as signal processing in compact-disk players and telecommunications systems.

Philips is also banking on the big applications support it can give as Europe's top electronic systems maker. What's more, the company can provide a full range of development tools such as simulators, assemblers, and real-time emulators, as well as a vast library of programs for implementing such functions as filters and fast Fourier transforms.

To help it become a major player in the field, the Dutch company has lined up a semiconductor producer it will not currently name to second-source its devices.

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WE COULD HAVE CALLED IT A 32-BIT MICROPROCESSOR.

WE COULD HAVE CALLED IT A 10-MIP COMPUTING ELEMENT.

WE COULD HAVE CALLED IT THE FIRST CONCURRENT SOLUTION.

INSTEAD WE CALL IT THE TRANSPUTER.

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INMOS introduces the transputer family. A range of evaluation boards for the first transputers is available now.

The transputer is a fast, easy to use VLSI component designed for applications ranging from single microprocessor systems to supercomputers.

The IMS T414 is the first transputer, integrating a 32 bit microprocessor, four inter-transputer communication links, 2 Kbytes of RAM, a 32 bit memory interface and a memory controller onto a CMOS chip.

The microprocessor runs at 10 MIPS and is designed specifically for the execution of high level languages. It combines direct support for multi-tasking, floating point, block transfer and record handling with sub-microsecond procedure call and task switching.

Each transputer link provides a full duplex, 10 Mbits/sec, point to point connection with an on chip DMA controller. Links are used for inter-transputer communication or, via an INMOS Link Adaptor, interfacing to industry standard byte wide peripherals.

The memory interface provides access to a linear 4 Gbyte address space at a data transfer rate of up to 25 Mbytes/sec.

Transputers are designed for ease of engineering. All transputer family devices operate from a single 5 MHz clock input, which is used to derive high speed internal clocks for all on chip systems.

When transputers are directly connected via links, additional components are not necessary. Independent or common clocking can be used, regardless of timing skew.

The configurable memory controller also requires no external components. It provides all the necessary timing and refresh signals for memory systems, comprising any mix of ROM, SRAM, DRAM and memory mapped peripherals.

Transputers are designed for ease of programming. INMOS offers development systems which provide integrated editing, compiling and source level debugging for both single and multiple transputer applications, using C, Pascal, Fortran and occam.

In applications requiring only a single computing element, the transputer's speed, minimal support component requirements and programming efficiency provide significant cost/performance advantages over conventional microprocessors.

Systems of any size can be built from interconnected transputers, using the links. The same program can be configured to run on one, tens or thousands of transputers allowing a simple trade off between performance and cost.

The transputer family already includes 32 bit and 16 bit transputers, peripheral controllers, evaluation boards and development tools. Start assessing its capability for yourself now with an IMS T414 evaluation board.

TRANSPUTER PRODUCTS	
IMS T414	**32 Bit, 2 Kbyte RAM, 4 Transputer links**
IMS T212	**16 Bit, 2 Kbyte RAM, 4 Transputer links**
IMS C001	Transputer Link Adaptor. Separate 8-Bit input and output
IMS C002	Transputer Link Adaptor, Multiplexed 8-Bit input/output

DEVELOPMENT TOOLS	
IMS D100	INMOS Transputer Development System
IMS D600	Transputer Development Software, VAX-VMS
IMS D700	Transputer Development Software, IBM-PC

EVALUATION BOARDS	
IMS B001	Double Eurocard, IMS T414, 64 Kbyte RAM, 2 x RS232C ports
IMS B002	Double Eurocard, IMS T414, 2 Mbyte RAM, 2 x RS232C ports
IMS B004	IBM-PC add on card, IMS T414, 1 Mbyte RAM

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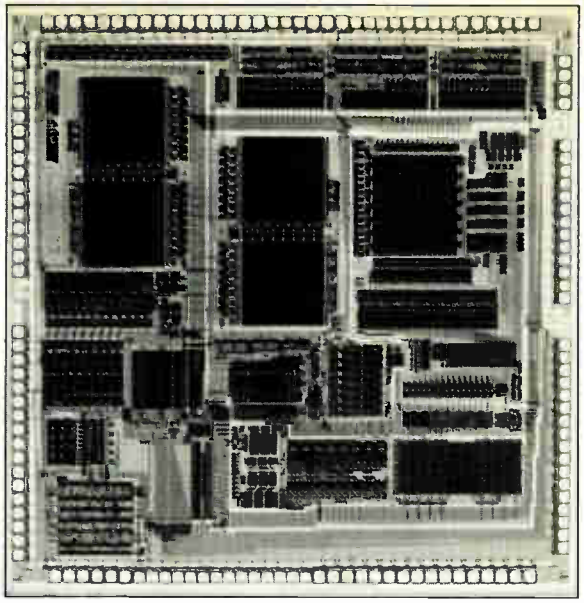
section being under the control of a different field within each 40-bit instruction word. The programmer need concentrate on only one field at a time rather than deal with unwieldy instructions controlling several functions.

The chip's five functional blocks are the program control unit with program store; the multiplier-accumulator with barrel shifter and format adjuster; the arithmetic logic unit with a scratchpad register file; a block with data and program ROM, two data random-access memories, and three independent address computation units; and a serial-parallel input/output section consisting of five I/O interfaces.



PACKED. The PCB5011, a ROM-less version in the SP50 DSP family, packs 75,000 transistors on an 89-mm² chip.

Besides the high level of parallelism that allows functional blocks to operate simultaneously, another unusual feature is the way interblock communication is handled, van Kampen claims. The main communication routes are the two 16-bit data buses, which closely couple all functional blocks.

LOCAL BUSES. To prevent congestion on the main buses and thus maintain high throughput, the Philips designers have incorporated dedicated local buses between certain devices within each block. These run, for example, between the multiplier and accumulator, between the ALU and register file, and between the ACUs and the data stores.

The serial I/O ports work independently of the rest of the chip. Because it has five I/O interfaces, the chip can serve telecom terminals, which often have many ports.

The 16-by-16-bit multiplier with pipelining register produces a full 32-bit result. The 40-bit accumulator (including 8 overflow bits) supports multiprecision product accumulation; the barrel shifter supports multibit shifts. The barrel shifter and format adjuster extract two 16-bit words in parallel and can alter the format as in, say, bit reversal.

Philips plans to extend the SP50 family to include DSPs upwardly and downwardly compatible with the 5010 and 5011, as well as DSPs dedicated to the needs of particular market segments. Peripheral devices will also be included.

The SP50 family is the result of a two-year joint development effort of the Philips Research Labs in Eindhoven and two German subsidiaries: components producer Valvo GmbH in Hamburg, and Tekade GmbH, a communications equipment maker in Nuremberg. Valvo will make the devices. *–John Gosch*

SUPERCOMPUTERS

TUNING CMOS MACHINES WITH DELAY TECHNIQUE

CAMBRIDGE, MASS.

The problem of clock skews within the large cabinets needed to house supercomputers and fast multiprocessors may be solved much more easily with a dynamic delay technique developed jointly by the Massachusetts Institute of Technology and Bolt, Beranek & Newman Laboratories Inc. The new approach holds the promise of a flexible electronic method for tuning the biggest and fastest CMOS computers.

The MIT-BBN approach, slated for discussion this week at an MIT conference on advanced very large-scale-integration research, will draw greatest attention for what developers say is an ability to compensate for temperature fluctuations.

As CMOS technology scales down, the buffers required to drive signals across system lines take up increasingly large fractions of the clock cycle. Given that these buffers are temperature-sensitive, their responsibility for system variability will increase. This factor must be minimized with elaborate cooling systems or other approaches that can compensate for temperature changes.

The MIT-BBN prototype circuit routes signals to five different delay lines on the input buffer of a receiving chip. Outputs of the delay lines are in turn routed to both a multiplexer and a comparator circuit. The comparator circuit decides which of the delay lines is appropriate to best synchronize the incoming signal with the internal clock phase.

The comparator's output is sent to a low-pass filter that controls the multiplexer. The multiplexer selects the delayed version of the input signal that is to be used. The prototype was implemented in 3-μm CMOS and achieved 50-Mb/s transmission rates, but developers say the target is 200 Mb/s in 1.25-μm CMOS.

THE BIG PROBLEM. The biggest issue with this design, for which BBN is seeking a patent, is the metastability problem; this arises when the circuit's comparator cannot assign the appropriate delay line quickly enough, leading inevitably to a machine crash.

The problem is minimized in the MIT-BBN design by the low-pass filter, which is slow enough to reduce the chance of comparator hangup to an acceptable level. The filter will continue to pump out the last value until the comparator makes a change.

"The design incorporates a theoretical probability of synchronizer failure of less than 10^{-20} per second," says Lance Glasser, assistant professor of electrical engineering at MIT and a consultant with BBN in Cambridge.

To avoid lowering the bandwidth of the signal channel, it was necessary to make the update rate of the filter hundreds of times slower than the clock frequency. Because the filter and the input bandwidth are decoupled, however, the system is not slowed down. And though the filter is slow compared with the data rate, it is sufficiently fast relative to such changes as machine temperature.

Up until now, computer architects have used one of two options to tune their machines. The older method entailed cutting wires to precise lengths to ensure signal synchronization. "That traditionally takes a hell of a lot of time," says Tony Vacca, head of technology development at ETA Systems Inc. in St. Paul, Minn. For one large ETA machine, which might include 4 million to 6 million gates, cutting and measuring took from four to six weeks, says Vacca.

ADDING INCREMENTS. These days, ETA uses an alternative approach that electronically tunes the computer. In this scheme, a master clock runs out of a multiplexer whose lines add the appropriate number of picoseconds required for tuning. This requires an LSI chip dedicated to the clock, with delay selection made inside the chip.

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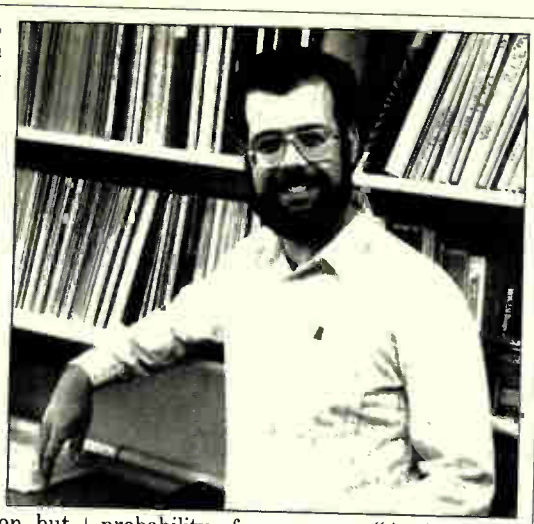
PROBLEM SOLVER. Lance Glasser, assistant professor at MIT and a BBN consultant, helped develop the dynamic delay technique.



In a large machine, overhead is appreciable with this approach; a half dozen or so chips may be required. And both the wire-cutting and the electronic-tuning approaches are static adjustments.

There have been previous attempts to build alternatives that require comparators, but these have foundered because they could not overcome the metastability problem. "For 25 years, I've seen that son of a gun. Everybody thinks they have a solution, but there's always a condition when it occurs," according to Vacca.

Glasser concedes that his approach does not eliminate the problem, but he argues that the problem is reduced in this latest design to an insignificant probability of occurrence. "A 180° phase change could break [the circuit]," he says, "but you could restart the machine. Compare that to a machine where you cut the wire lengths. You'd have to take wires out and put in wires of new length." *–Craig Rose*

BUSINESS ABROAD

KOREA KEEPS INVESTING IN CHIPS DESPITE DOWNTURN

SAN JOSE, CALIF.

South Korean companies came a day late to the world semiconductor market, but not a dollar short. A just-completed report—Korean Semiconductor Industry Analysis from Dataquest Inc., San Jose, Calif.—shows that despite the down market, Korean companies put $528 million into capital spending last year, nearly as much as the $586 million they invested in 1984.

Just five years ago, South Korean participation in semiconductors was mainly limited to producing discrete components and installing circuit assemblies. The report says the Korean government is now aiming for a self-sufficient semiconductor industry by 1990.

Major Korean production facilities came on line in 1984 as the industry was riding on the highest crest it has yet seen. Mike S. Bae, a consultant on the Dataquest report and president of his own consulting firm, Macro LSI of Santa Clara, Calif., points out that the Korean companies "were caught by surprise" by 1985's recession. "Their plans were for a recession in 1986."

TIME LAG. This left them in a tough position: capacity was up and prices were dropping before efficiencies in the manufacturing process could be brought to bear in the cost of production. As one result of that recession, Hyundai Electronics Industries Co. last fall curtailed its expansion into Silicon Valley's Santa Clara [*Electronics*, Oct. 7, 1985, p. 11]. Bae, who had worked for Hyundai and built the Santa Clara facility, calls that "a premature, short-sighted decision."

Pointing to the capital investment made by Korean companies, Gene Norrett, Dataquest vice president and director of its Japanese Semiconductor Industry Service, says, "the Koreans have said there's no backing out."

Though the semiconductor industry worldwide is expected to grow 16% in 1986 (in contrast to a decrease of about 16% last year), Norrett says the Korean growth will be over 100%, even if this turns out to be a bad year elsewhere. In 1985, the Korean market was about $265 million, with $39 million—15%—of it native production. By contrast, Japan's market was $8.5 billion and the U. S.'s was about $9 billion.

Bae says that in 1990, Koreans hope to have about 2% of a $100 billion semiconductor market. But Norrett points out that it is difficult to say how that will translate into a percentage of the U. S. market. Like Japan, Korea is characterized by large, vertically integrated corporations; they can use their semiconductor production to manufacture their own consumer products if the external market for their chips is weak.

COOPERATIVE BENT. But in Bae's analysis, the Korean mindset is to cooperate with the U. S. rather than to exploit that market. "For Koreans, the U. S. is the savior," says Bae, a Korean native who lived there under foreign rule. The cooperation is demonstrated by at least 20 technology-transfer agreements between U. S. and Korean companies to trade manufacturing for advanced design and production techniques.

Norrett indicates that recent rulings by the U. S.'s International Trade Commission regarding Japanese semiconductor competition is also good for Korean companies. "It is good news for the Koreans that the U. S. will probably not lose market share in the next year or two," he concludes. Norrett expects competition in Asia to come down to "a feature war between the Japanese and the Koreans." *–Eve Bennett*

PARALLEL COMPUTERS

FLEXIBLE DEMONSTRATES AS-YOU-LIKE-IT STRATEGY

DALLAS

Flexible Computer Corp. will soon demonstrate why its founders selected such a name when they formed the company in 1983. It is introducing a new 32-bit computer board that will allow customers to mix rival 68020 and 32032 microprocessors in the same multiple-computer system.

The result is a pliable parallel-computing environment that can simultaneously apply different processor instruction sets to a single application while using the same data. "To our knowledge, it is a first," says Nicholas Matelan, Flexible's president.

The company's Flex/32 hardware and operating systems can automatically set up interprocess communications between dissimilar processor boards as well as apply the appropriate compiler to the right instructions and hardware. "From the beginning, we took a lot of extra time to make sure that everything we did would have a smooth map to anyone's instruction set," says Matelan.

The newest processor board from Flexible, due for shipment by the end of the second quarter, is called C2C and is based on Motorola Inc.'s 68020. Matelan says customers are expected to prefer its processing power (up to 2.5 million instructions per second) for real-time computing applications. The existing C1C board, based on National Semiconductor Corp.'s 32032 and running at a

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slower 0.75 mips, will likely be used for such applications as data-base interfaces, says Matelan. Flexible intends to support both processors, as well as future 32-bit microprocessors and a number of custom processors with the multiple-bus Flex/32 [*Electronics Week*, May 13, 1985, p. 49].

The strategy is also intended to attract early users of parallel-computing systems, affording them the flexibility of mixing and even replacing multicomputer boards without having to rewrite programs.

"The software is 'invisible' to the hardware it is running on. Software runs against logical engines instead of physical engines," explains Matelan. "Our system is the perfect home for different kinds of instruction sets running at the same time." Fundamentals behind Flexible's concept stretch back to computer-science pioneer Alan Turing. The Turing machine mathematical model defines a simple computer with an infinite tape and three instructions it uses to perform all known general-purpose functions.

"All instruction sets are isomorphic to a Turing machine," Matelan says. "All general-purpose instruction sets can compute any general-purpose function, and there should be no reason why any program written in a standard language cannot be computed on any processor. . . . The key is structuring the way you do things up front so you don't block yourself from being mapped to the processor. Many other companies try to take advantage of processor [architectures] too early.

MIX AND MATCH. Owners of Flex/32 systems from Flexible Computer can now use 68020- and 32032-based processor boards in parallel.

"We take advantage of each processor type, but at the kernel level," he adds. The front end of each compiler is similar, while the back end is specific to an individual multicomputer board. Flexible's approach enables the company to ready processor boards with new processors in six to eight months, in contrast to the normal development time of about two years, says Matelan.

"Flexible is not just the name of the company, but it is the whole philosophy of being able to put building blocks together in any combination," says Matelan. In the fourth quarter, Flexible plans to offer a third board, dubbed the "scientific card," which is an array processor and add-on vector floating-point hardware made from bit-slice integrated circuits.

"In the future, we will do the same thing for artificial-intelligence processors and instruction sets. If the market feedback shows a demand, we will have a graphics-engine instruction set and even a RISC [reduced-instruction-set computer] multicomputer," says Matelan. —*J. Robert Lineback*

PERIPHERALS

COLOR INKJETS MAY DROP IN COST

IVREA, ITALY

It isn't news that one of the best methods of printing computer-generated color images is the ink jet. What is news, however, is that the technology has now been developed to do this complex job at a reasonable cost. Full-color ink-jet printers cost upward of $5,000. Research engineers at Ing. C. Olivetti & Co. have developed a working prototype that seems to have overcome most of the key problems keeping the price at such a level.

The compact printer operates at high speed, producing high-quality images and letter-quality alphanumerics that are highly stable on any kind of paper. Clearly conceived with inexpensive applications in mind, the technology fits with Olivetti's strategy of focusing on the low end of the data-processing market.

Olivetti will not say when or even if it will market a product based on this technology. Because the printer is the fruit of a research project, no product plans are necessarily implied, says Arnaldo Pasini, the Italian company's research and development director. He does admit, however, that along with work in magnetic storage and speech recognition and synthesis, his laboratory's work in printing technology is considered one of the most strategically important areas for the company's future.

The Olivetti printer is based on the drop-on-demand principle, whereby a piezoelectric element squeezes a glass tube that in turn ejects a single ink drop per impulse. Such systems have previously created a dilemma.

Olivetti's working prototype overcomes most of the problems

To obtain a clean, high-definition image, drop-on-demand printers needed high-viscosity inks, which meant that copies dried slowly unless they were printed on special absorbent paper. Water-based inks that dry on contact with any paper to solve that problem generated satellite droplets of ink, which hurt the quality of the printed copy.

Olivetti's breakthrough was finding a way to eject uniform single drops of water-based low-viscosity inks. The company's analysis found that the satellite droplets were caused by reflected waves of ink in the glass tube that ejects ink at its junction with the feed-pipe, which connects it to the ink supply. These waves are produced by conflicting forces set in motion by the tube being squeezed some 10,000 times/s; they become even more severe as the operating frequency of the print head increases.

THE EQUALIZER. Olivetti's proprietary system, which Pasini declines to describe, equalizes the impedance throughout the tube and at its junction with the feed-pipe. This produces uniform drops up to an ejection speed of some 13,000 drops/s, well above the point where the process would be of commercial quality.

The Olivetti printer's head consists of four such tubes—one each for yellow, cyan, magenta, and black. Black is used to produce alphanumeric characters; the other three colors, used in correct combinations, can produce any other color. Each tube is controlled by a related piezoelectric transducer and connected by a feed-pipe to a cartridge containing ink.

The four elements of the head begin

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life as standard Pyrex tubes. To realize the ink-ejecting opening, a tube segment is heated by two burners at 750°C until it forms an hourglass shape with a diameter of 60 μm, ±1 μm, at its narrowest point. It is cut at this point by a diamond grinding wheel, then cut and polished until flat. An oxide is deposited on the rim to inhibit wetting as ink drops are ejected. Olivetti has automated the entire process in its laboratory to determine production feasibility.

The printer based on such a head is small—about the size of a standard dot-matrix machine. It prints in full-color process any digitized color-separated image, including photographs. Image quality resembles that of color newspaper photographs, with somewhat lower definition. However, color clarity, including flesh tones, is excellent.

Besides development of the printing head, Olivetti also put significant effort into developing suitable inks. Pasini explains that producing homogeneous drops of light-resistant, fast-drying inks while avoiding clogging requires strict control of the degrees of metallic and organic impurities, surface tension, and dynamic viscosity. *–Robert T. Gallagher*

CONVENTIONS

CAN MANHATTAN LURE THE BIG SHOWS BACK?

NEW YORK

Over the past decade, the New York Coliseum, once the premier showplace in the nation, decayed into a cramped and expensive nightmare for promoters. Large-scale exhibitions, such as the National Computer Conference, abandoned the outdated and undersized building—and New York—for better facilities elsewhere. Now the Big Apple is back: last week, it closed the Coliseum and opened its new showplace, the $486.2 million, 1.8-million-ft² Jacob K. Javits Convention Center.

After spending all that money, the Big Apple's big question is: will the modern glass, metal, and concrete building be enough to lure back shows that swapped the market strength of New York for the glitter and cost advantages of the likes of Las Vegas?

Initial indications say yes. NCC organizers, committed to alternate between Chicago and Las Vegas through 1989, are considering New York for 1990 and 1993. "Up until the Javits Center, there were no facilities on the East Coast that could accommodate NCC," says Ann-Marie Bartel, special projects coordinator at the American Federation of Information Processing Societies Inc., which coordinates NCC. Now Afips is ready to revert to its old ways. "Our philosophy at NCC has always been to rotate East, Center, West," Bartel says. That hasn't been possible in recent years, she says, because NCC was too big for any East Coast building.

The return of NCC to New York would be a major coup for the Javits Center, since the convention—which boasts about 2,500 booths and 70,000 attendees each year—is the industry's largest. NCC's promoters may be waiting, however, to see how the facility fares for another major electronics industry show—Electro/87. Electro will be the first major industrywide event at the Javits Center, which can legally accommodate up to 85,000 people in 720,000 ft² of indoor exhibition space and sports such high-tech features as a global teleconferencing center.

But any hope that New York might have of keeping Electro to itself (the show shifts between New York and Boston) is premature. "We book our shows 10 years out," says Mickey Green, operations coordinator of Electronic Conventions Management, which manages Electro for its sponsor, the Institute of Electrical and Electronics Engineers. Green adds that all eight shows the company manages rotate between two regional locations.

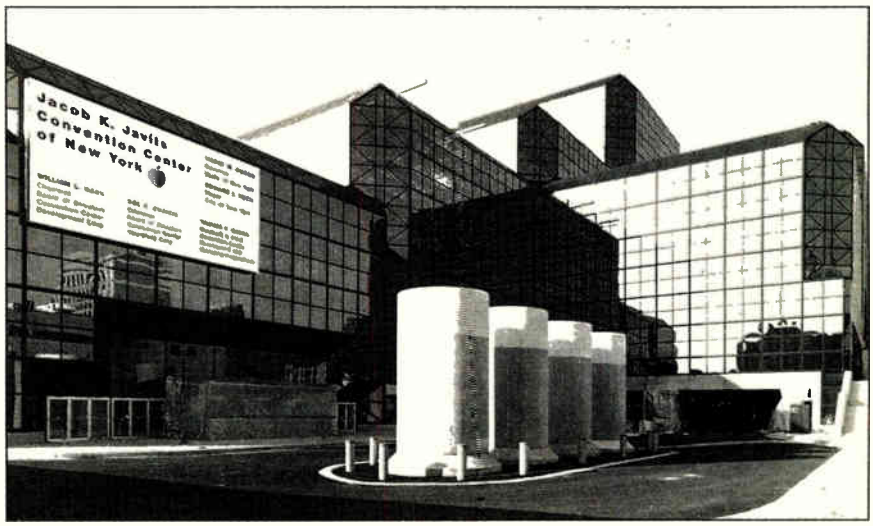
Some show promoters say they will continue to avoid New York. A spokesman at the Interface Group Inc., the Needham, Mass., sponsor of the Comdex shows, says Interface has no plans to hold a New York convention. Similarly, a spokesman at the Electronic Industries Association says the EIA will not hold the semiannual Consumer Electronics Show in New York in the foreseeable future.

Long before Electro/87, however, smaller industry shows such as PC Expo and Computer Graphics New York '86 will try out the building for size. Computer Graphics, which is being held by Exhibition Marketing and Management Co., a McLean, Va., show manager, will mark the electronics industry's first appearance in the new building this month. And for Justin Webb, the company's vice president of marketing, the prospects are exciting. "The facilities are a vast improvement," he says. "From the organization to loading the equipment, it's much better" than the Coliseum. Says Ralph Iamuzzi, director of PC Expo, "The building's awesome. It's stunning."

One of the biggest troubles with the Coliseum, Webb says, was the high cost of moving into and setting up in the multilevel facility. Moving in took too long, with much time wasted just waiting for elevators or loading docks. But the Javits Center boasts 50 loading docks (compared with four for the Coliseum) and 18 elevators.

"New York is a difficult exhibition town," Webb says. "The unions are tough, and everything you do seems to cost you more." That may still be true. Installation costs may be somewhat less, but not by much. So the Javits Center's managers are promising promoters that while costs will be substantially the same, it will be easier to set up and conduct shows in this huge space with its 35- and 55-ft ceilings.

"New York for a lot of electronics shows is ideal—it's one of the biggest markets in the U.S.," Webb says. "People have tended to avoid New York in the past, and I think the Javits Center should change that." *–Tobias Naegele*



LURE. The 1.8-million-ft² Jacob K. Javits Convention Center will lure NCC and other big shows back to New York, backers hope, though the city remains an expensive place to do business.

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INSIDE TECHNOLOGY

SPECIAL REPORT: VLSI GIVES BIPOLAR A SECOND WIND

IT GETS A BOOST FROM DEEP GROOVES AND TRENCH ISOLATION

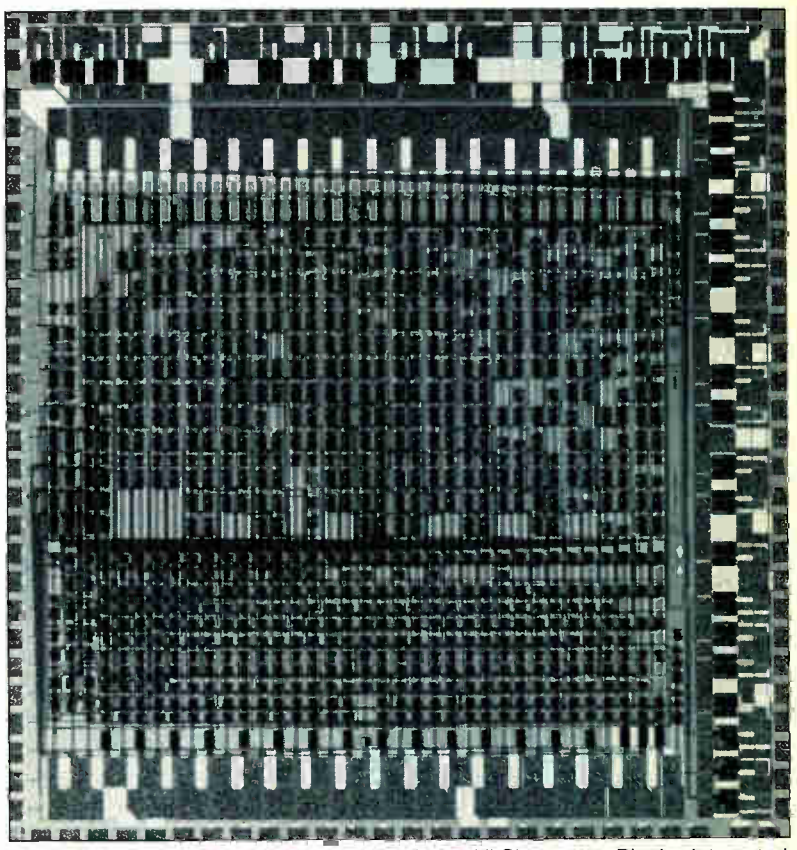
by Bernard Conrad Cole

Pure bipolar circuit technology seemed to be running out of steam just as its competitors started moving in for the kill. Now, though, it is getting a second wind and should be able to head off the assault at the low end of its performance range from CMOS, at the high end from gallium arsenide, and from all over the map by bipolar-CMOS combinations. Giving bipolar new momentum is a plethora of advanced processing techniques as IC makers move below 1-μm very large-scale integrated circuits and closer to sub-0.5-μm ultrascale chips.

Already in the works are bipolar process variations, such as deep-groove and trench-isolation techniques, and designs with multiple levels of interconnections, all of which should allow bipolar technology to maintain its hold in high-speed digital and static memory circuits as well as in linear building-block functions. This next wave of technology should also give CMOS a run for its money in ICs requiring a mix of analog and digital functions, agree many device physicists, process engineers, and circuit designers.

Research laboratories and IC companies are exploring a wide range of applications. Designers in the U. S. and in Japan are investigating:

- Arrays approaching 80,000 gates, 250-ps delays, and power dissipation measured in microwatts.
- 256-K static random-access memories with access times in the 10- to 20-ns range, 16- to 64-K RAMs under 10 ns, and 1- and 4-K designs approaching picosecond speeds.
- 8-bit digital-to-analog converters with clock frequencies approaching 0.5 GHz and analog-to-digital converters in the 200-MHz range.
- And all manner of mixed analog and digital circuitry. Here, observers say, bipolar can match CMOS in density yet retain its peerless linear performance.



1. SPEEDY SYSTEM. Using an advanced bipolar VLSI process, Bipolar Integrated Technology's B3018 does a 16-by-16-bit multiplication in 5 ns.

Traditionally, MOS technology has offered better possibilities for higher densities, lower power, and higher speed/power ratios because the circuits are self-isolated and simply structured, says Michael Mulholland, director of bipolar design at National Semiconductor Corp., Santa Clara, Calif. In addition, they offer higher resistances on a small surface to facilitate lower power dissipation, albeit at the cost of lower switching speed. The strength of bipolar devices, he says, lies in their extremely high switching speeds. But their complicated structures and the need to keep transistors isolated have limited higher levels of integration.

Great strides have been made in bipolar design and in processing techniques to overcome these drawbacks while maintaining the technology's inherent speed advantages, says Mulholland. Some borrowed (from MOS), some new, these advances include improved routability and chip utilization through the use of multiple interconnection levels, self-aligned device structures, ion implantation and polysilicon emitters, deep-groove isolation, and elimination of parasitic transistor junctions. Added to this, says Robert Stehlin, new products and technology manager at Texas Instruments Inc.'s Logic Division in Dallas, is the promise that geometries can be brought far below 0.5 μm without many of the second-order and hot-electron effects that plague submicron CMOS VLSI circuits.

"The combined effect of these new processing and fabrication tools on bipolar technology has been revolutionary," says Chris Lattice, manager of bipolar technology at Fairchild Semiconductor Corp.'s High Speed Logic and Memory Division in Puyallup, Wash. "The only comparable period in its history was the transition a decade ago from junction isolation to oxide isolation." Indeed, says TI's Stehlin, studies in device scaling are showing that no physical phenomena block the

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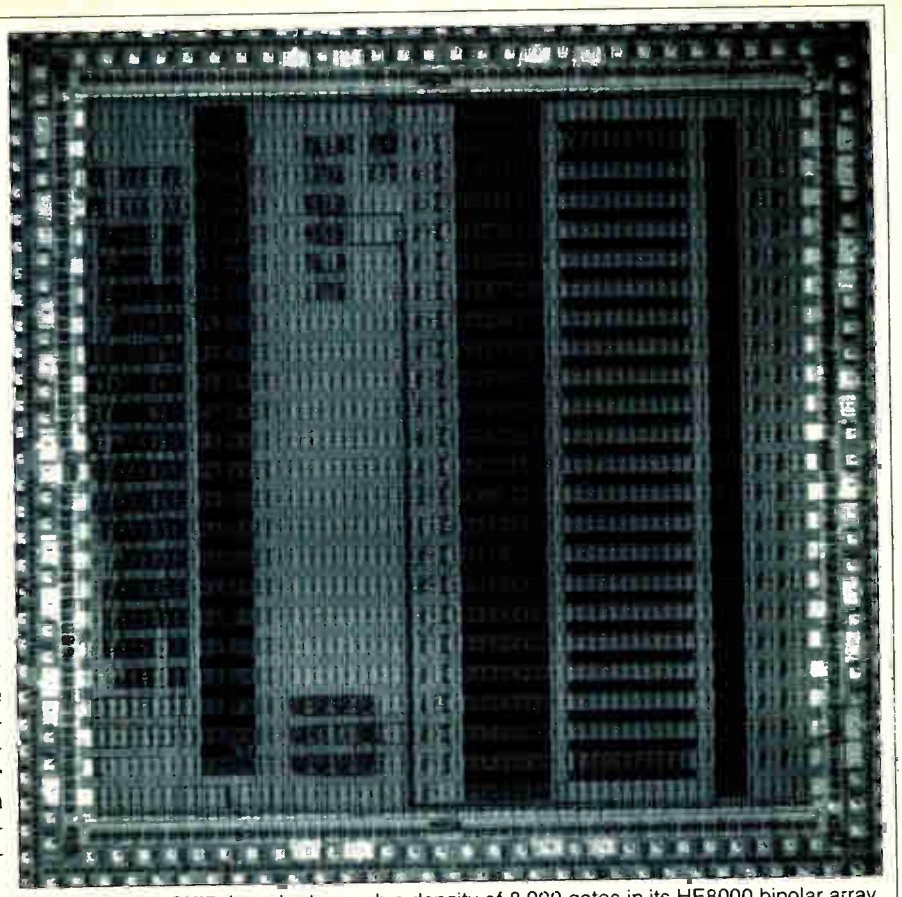
fabrication of bipolar transistors with submicron dimensions.

One of the first density-improving techniques developed for bipolar circuits was the use of multiple interconnection levels. In fact, says Stehlin, bipolar designers pioneered the use of this technique to improve gate utilization, global signal wiring, and power distribution. The method simultaneously increases circuit density and reduces noise sensitivity. Now when CMOS designers are just moving to two levels of metal interconnection, many three-level bipolar designs are already well through the design cycle and designers are toying with four. Four levels would allow the four degrees of freedom required for silicon-efficient computer-aided auto-routing software [*Electronics*, Dec. 2, 1985, p. 34].

The layout of a bipolar transistor is very sensitive to the overlay accuracy between masking levels, according to TI's Stehlin. This means that the overall size of the structure is considerably larger than the active device area defined by the emitter. Hence the interest in self-alignment schemes, which eliminate the tolerance problem and reduce base-to-emitter spacing. Not only is the collector junction area reduced but so is the total base resistance, resulting in significant improvements in circuit speed.



2. 8,000-GATE CHIP. In order to reach a density of 8,000 gates in its HE8000 bipolar array, Honeywell is using an advanced current-mode-logic design.

Ion implantation is another technique attracting the attention of bipolar designers. This technique allows the formation of much shallower impurity profiles on the active device, says National Semiconductor's Mulholland, which is crucial in making reproducible ultrathin base regions with the high doping concentrations necessary for scaled submicron devices.

Another important technical advance is the use of poly emitters to achieve higher gains in a given transistor over conventional structures. "The effect of the higher gain is to lower the amount of power needed to drive a particular gate at a particular speed, thus reducing the power dissipation of the total chip," says Fairchild's Lattice. Such transistors have shallower junction depths and increased junction doping, both of which result in higher operating frequencies.

Much work has also been done in deep-groove isolation. The use of this technique for isolating the n^+ sublayer regions in bipolar transistors is increasing, says John Burgoin, managing director of bipolar programmable read-only memories and programmable logic arrays at Advanced Micro Devices Inc., Sunnyvale, Calif. Deep grooves, especially with an oxide sidewall and a dielectric filler such as undoped poly, provide isolation with higher breakdown voltage and less parasitic capacitance. At the same time, the area occupied by the isolation region is reduced, which significantly improves density.

In addition, trenching allows designers to reduce the pitch—the distance between individual transistor emitters—from an average of 20 μm to 6 or 7 μm, making space for about three times as many transistors. The greatest impact will be on memory arrays, says Lattice, and to a lesser extent on logic circuits—particularly those, such as gate arrays, with regular, repeated structures.

Finally, increased bipolar speed and density are abetted by the ability of process engineers to fabricate devices with extremely flat, or planar, surfaces. With such surfaces, the steplike transitions between metalization layers can be eliminated. "Whenever a metalization step is required, the metal thins out, lowering the ability to carry current," says Stehlin. "Planarization also reduces the capacitance of the second level of interconnection by widening the space between layers, thus improving switching speed."

Trenching creates space for three times as many transistors

All the new bipolar techniques are tools for semiconductor manufacturers, who are rushing into production with a wide variety of logic, memory, and signal-processing circuits. Initially, they are applying the new fabrication methods to the traditional logic families such as TTL, Schottky transistor logic (also called integrated Schottky logic), emitter-coupled logic, and current-mode logic.

Indicative of the increasing activity was the flurry of papers at this year's International Solid State Circuits Conference [*Electronics*, Feb. 17, 1986, p. 23]. Among the products described were a high-performance bipolar mainframe on a chip, several advanced static-memory designs, a smattering of gate arrays, and numerous custom circuits.

ONE-CHIP MAINFRAME

The one-chip mainframe was perhaps the most spectacular introduction. This is a single-chip 32-bit CPU implementation of the 801 reduced-instruction-set minicomputer architecture from IBM Corp.'s Los Gatos, Calif., research facility. Fabricated with an experimental bipolar process developed originally for static RAMs and implemented in a multilevel variant of ECL called differential cascode ECL, the single +5-V chip has a 60-ns cycle time and dissipates 8 W.

It uses deep trench isolation to minimize device capacitance without reducing density and three levels of metalization. The

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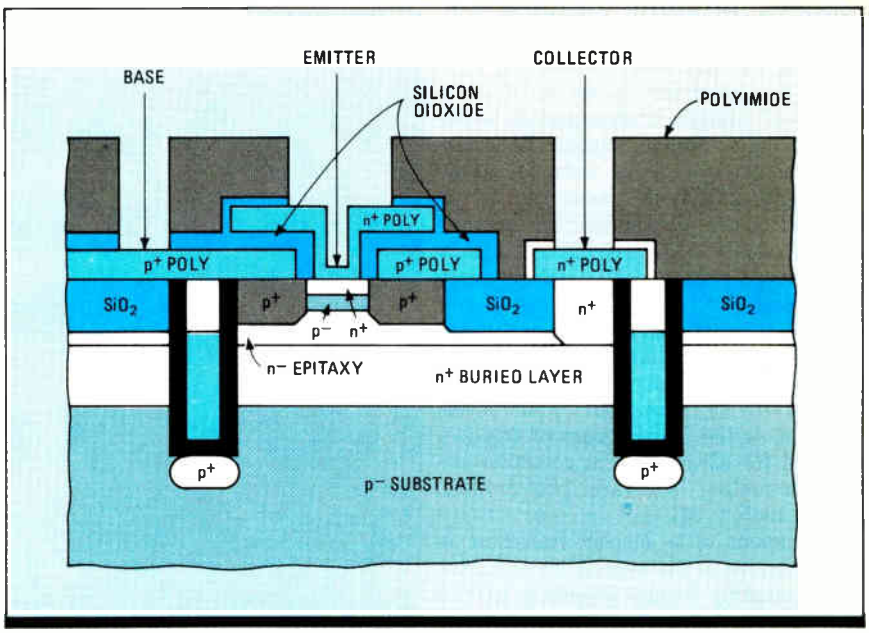
use of differential cascode ECL allows the design of very high-density circuits with eight logic levels in a binary switching tree architecture. Biasing the transistors near breakdown means high power is dissipated at low current.

Equally impressive were the bipolar SRAMs, including a 4-K-by-4-bit design from NEC Corp., Kanagawa, Japan, featuring 4-ns access times and a power dissipation of only 1.6 W. A similar 16-K design from Hitachi Ltd., Tokyo, has a 3.5-ns access time and dissipates 2 W. Perhaps the most innovative SRAM shown at the meeting was a 3-ns 32-K-bit design from IBM's General Technology Division, Hopewell Junction, N. Y. This circuit combines poly-base npn transistors and poly-filled trench isolation with an unclamped complementary transistor switch memory-cell architecture. According to the designers, this means high speed with 20% to 30% smaller cell area, twice the soft-error immunity, six times the leakage tolerance, and fewer current-hogging problems than previous designs.



3. FAST ECL. Fairchild hopes to reach gate speeds of less than 100 ps with emitter-coupled logic by using trench isolation and self-aligned emitters in its arrays.

This activity is only the tip of the iceberg. A number of companies are developing technologies and products that are pushing bipolar logic and memory to higher levels of integration and speed. Among them is Bipolar Integrated Technology Inc., Beaverton, Ore., a recent entrant in the bipolar game. The company has developed a proprietary bipolar process it calls BIT1 (see related story, p. 35) for use in the fabrication of a high-performance line of TTL and ECL data- and signal-processing elements, such as multipliers, finite and infinite response filters, fast Fourier transforms, image processors, and graphics devices. The BIT1 process can fabricate transistor structures as small as 14 μm^2, with gate delays as low as 300 ps at 300 μW, a tenfold improvement over conventional ECL circuits, according to company president George Wilson. The first product fabricated using BIT1 is a 16-by-16-bit fixed-point multiplier, the B3018 (Fig. 1). The ECL version boasts a typical multiply time of 5 ns at 2.9 W.

Another bipolar technique recently announced is the IMOX III-Slot process from AMD [*Electronics*, Feb. 10, 1986, p. 35]. The company is applying IMOX III to a broad spectrum of devices, including PROMs, SRAMs, and field-programmable logic circuits. The first available product is a 128-K bipolar TTL PROM, the Am27S51. Its access time of 35 ns is approximately equivalent to a nontrenched 16-K PROM, but it uses one eighth the power. In addition to using IMOX III in a family of lower-density TTL and ECL PROMs, the company is applying it to a series of ECL SRAMs, a 1-K-by-4-bit RAM with a 10-ns access time, a 16-K-by-1-bit RAM with a 15-ns access time, a 4-K-by-4-bit RAM, and a proprietary 512-K-by-9-bit part with on-chip logic for cache-memory systems. It is also being used in the production of a group of high-performance, fusible-link, field-programmable logic devices.

For throughput, designers will usually choose bipolar

TI is taking an even more sweeping approach to bipolar fabrication. It plans to apply its Impact-X process [*Electronics*, Dec. 23, 1985, p. 45] across all its bipolar TTL, Schottky transistor logic, and ECL product lines as well as to bipolar ECL SRAMs. Among the products slated for Impact-X are TI's next-generation 32-bit microprocessor chip set, a 64-K bit-programmable ROM, a family of ECL-type field-programmable logic devices, and the entire 888 ECL family. When Impact-X is applied to TTL, the result is 5-ns gate delays at 0.5 mW—half the dissipation of earlier processes, says TI's Stehlin. In Schottky-transistor-logic designs, gate delays as low as 800 ps at 0.1 mW are possible, almost twice as fast as earlier generations. Applied to ECL designs, he says, Impact-X results in gate delays of 200 ps at 5 mW, almost 2.5 times faster than earlier designs.

Honeywell Inc.'s Digital Products Center in Colorado Springs, Colo., has also entered the fray, applying its ADB-III 1.5-μm bipolar process, developed for the Pentagon's Very High Speed Integrated Circuits program, to a family of commercial gate arrays. The three-level-metal process features gate speeds in the 150- to 600-ps range, with power dissipation per gate of 1.3 to 6 mW, toggle frequencies approaching 1 GHz, and gate densities approaching 15,000, says David Wick, manager of system applications engineering at Honeywell. One of the first commercial products using this process is the HE8000 gate array (Fig. 2), which combines current-mode and integrated Schottky logic. It has a maximum gate density of 8,000 and an average gate delay of 225 ps, and it dissipates 6 to 8 W per chip. Now in development is ADB-IV, a sub-0.5-μm all-current-mode-logic four-level-metal process featuring gate delays of about 100 ps and gate densities exceeding 80,000, says Wick.

Gearing up for production on its next generation of fine-line FAST-Z bipolar logic and memory products is Fairchild Semiconductor Corp., Mountain View, Calif. The Fairchild process is based on a sub-100-ps bipolar ECL technology. It uses an advanced trench-isolation technique and self-aligned poly-walled emitter and base structures with two levels of poly (Fig. 3).

SLIGHT SEPARATION

In this approach, a layer of p^+ poly topped with thermal oxide is deposited on the device island, and an area for the emitter is defined. Using chemical vapor deposition of oxides and an isotropic plasma-etching process, sidewall spacers are created. Emitters are then formed by depositing an n^+ poly layer. This allows for a separation of no more than 3,000 Å between the n^+ emitter and p^+ extrinsic base.

The technique also enables the placement of contacts outside the active device island, which reduces the collector base capacitance and base resistance by a factor of three or more.

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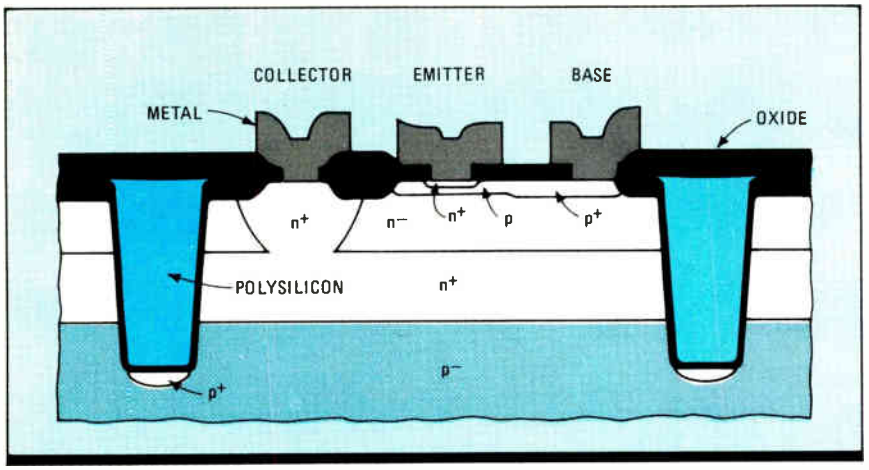

4. IN THE TRENCHES. Fujitsu is using trenched oxide and polysilicon isolation in the fabrication of its VLSI circuits to reach picosecond gate delays and gigahertz clock rates.

Trench isolation makes it possible to vertically align the edges of the buried layer, the base, and the walled emitter, says Fairchild's Lattice, reducing transistor size. With 2-μm design rules, a typical transistor is no larger than 1.5 by 3.5 μm^2. Moreover, transistors can be spaced as close as 1.5 μm, separated only by the trench.

Using 2-μm lithography (1.5-μm emitters), unloaded gate delays of 80 ps have been reached in test arrays and ring oscillator circuits. Peak cutoff frequency per gate is 10 GHz. For a loaded gate, wiring capacitance contributes 170 ps/pF and gate loading adds 6 ps per fan-out in a 1-mA emitter follower circuit. Scaling the process down to 1 μm results in gate delays of about 30 ps and cutoff frequencies approaching 15 to 18 GHz.

PROMISING APPROACH

The Fairchild approach holds much promise, especially in light of the company's earlier success with a non-trench-isolated version of the process. Using it, engineers at the company's Research and Development Laboratory in Palo Alto fabricated a 2-μm 64-K ECL SRAM with an average gate delay of 200 to 300 ps and read/write times of less than 15 ns. Cell size was 200 μm^2, about one third to one fourth that required with Fairchild's older Isoplanar technology. Chip size is less than 40,000 mm^2. If 1-μm design rules are used, the researchers believe a 256-K SRAM of about the same size and speed is possible.

Japanese companies are equally fervent in finding new uses for bipolar techniques. With the second generation of its super-self-aligned process, Nippon Telegraph & Telephone Corp.'s Atsugi Electrical Communication Laboratory in Kanagawa has used 1-μm lithographic techniques to fabricate a number of logic and memory circuits with gate delays as low as 25.8 ps and cutoff frequencies of 15 to 20 GHz. A 2,500-gate current-mode-logic masterslice array with a gate delay of 78 ps has been fabricated; so has a 6-ns 16-by-16-bit parallel multiplier with a carry/lookahead adder. Using four layers of metalization and 2-μm design rules, the process has resulted in an 8,300-gate macrocell array with cell delays of 333 ns and a cutoff frequency of 800 MHz. It also has been used to build a 16-K ECL SRAM with an access time of 15 ns and a 4-K ECL RAM with an access time of no more than 3.5 ns.

From Fujitsu Ltd., Kawasaki, Japan, comes a trench-isolation process called isolation by oxide and polysilicon. This technique boasts gate delays of about 325 ps loaded and 163 ps unloaded at 0.2 mA in ECL circuits. A key feature (Fig. 4) is deep U-groove isolation with a thick field oxide layer under the wiring channel regions. Circuits made with this process include a 10.38-GHz 563-mW frequency divider and a 5.03-GHz multiplexer, as well as a 1-K ECL SRAM with an 850-ps access time and dissipation of 950 mW.

As a result of these developments in processing and transistor design, bipolar technology should be able to maintain a dominant position in the high-performance end of the market and even give CMOS a run for its money in certain low-power high-density applications. This is because as CMOS moves down in device size from 2 μm to about 0.05 μm, the transistor structures and processing required get more complex. For bipolar circuits, the reverse is true. William Kean, strategic marketing manager for bipolar and CMOS VLSI at Texas Instruments, expects that bipolar's ascendancy will last through the early 1990s.

For the time being, he says, head-to-head comparisons between the two technologies are impractical because each has intrinsic characteristics that are attractive in different situations. "It will be necessary, as a result, to make decisions on the basis of system requirements rather than on straight device-to-device, family-to-family comparisons," he says. Where the requirement is for throughput, no matter what the power dissipation, the choice in most cases will be bipolar—for its lower gate delays, lower internal loaded gate delays, and the amount of external capacitance it can drive.

Speed requirements aside, says Kean, bipolar technology will be applied with best results to what he refers to as nonrecursive structures, such as random logic and gate arrays, and CMOS to recursive structures, such as RAMs, ROMs, and structured multipliers. In a recursive structure, a small number of cells are interconnected in a highly ordered manner, and individual cells have minimal internal line capacitance and fan-in/fan-out requirements. Nonrecursive circuits, on the other hand, are characterized by cells having different functions and connected with less regularity. The latter have large fan-in/fan-out requirements.

In ultra-LSI, the rules favor bipolar over CMOS

A number of developments are emerging that could upset this delicate balance. First of all, designers are moving to regain bipolar's position in designs requiring both high-density digital circuitry and linear functions on the same chip. Traditionally, system designers have chosen the high density of CMOS technology when working on mixed analog and digital circuits, despite its poorer linear characteristics. In addition, "bipolar offers higher gain, more precise matching of critical parameters, lower noise, higher operating voltages, as well as better dc specifications," says Steve Ulrich, head of the high-speed data-acquisition design group at Honeywell's Digital Signal Processing Center in Colorado Springs. Now a number of bipolar processes are emerging for use in high-performance linear as well as in high-density digital circuits.

For example, says Ulrich, designers at the center have combined the company's current-mode-logic-based 1.25-μm ADB-III digital process with its new high-performance 2.5-μm advanced linear bipolar (ALB-III) process. ADB-III features 500-ps gate delays, cutoff frequencies approaching 1 GHz, power dissipation of 300 μW per gate, and the ability to integrate up to 15,000 gates on one chip. The linear process features a 1.5-GHz npn cutoff frequency and gains approaching 100. Breakdown voltage is 20 V and minimum npn transistor area is 0.8 mil^2. Using it, the company has developed an 8-

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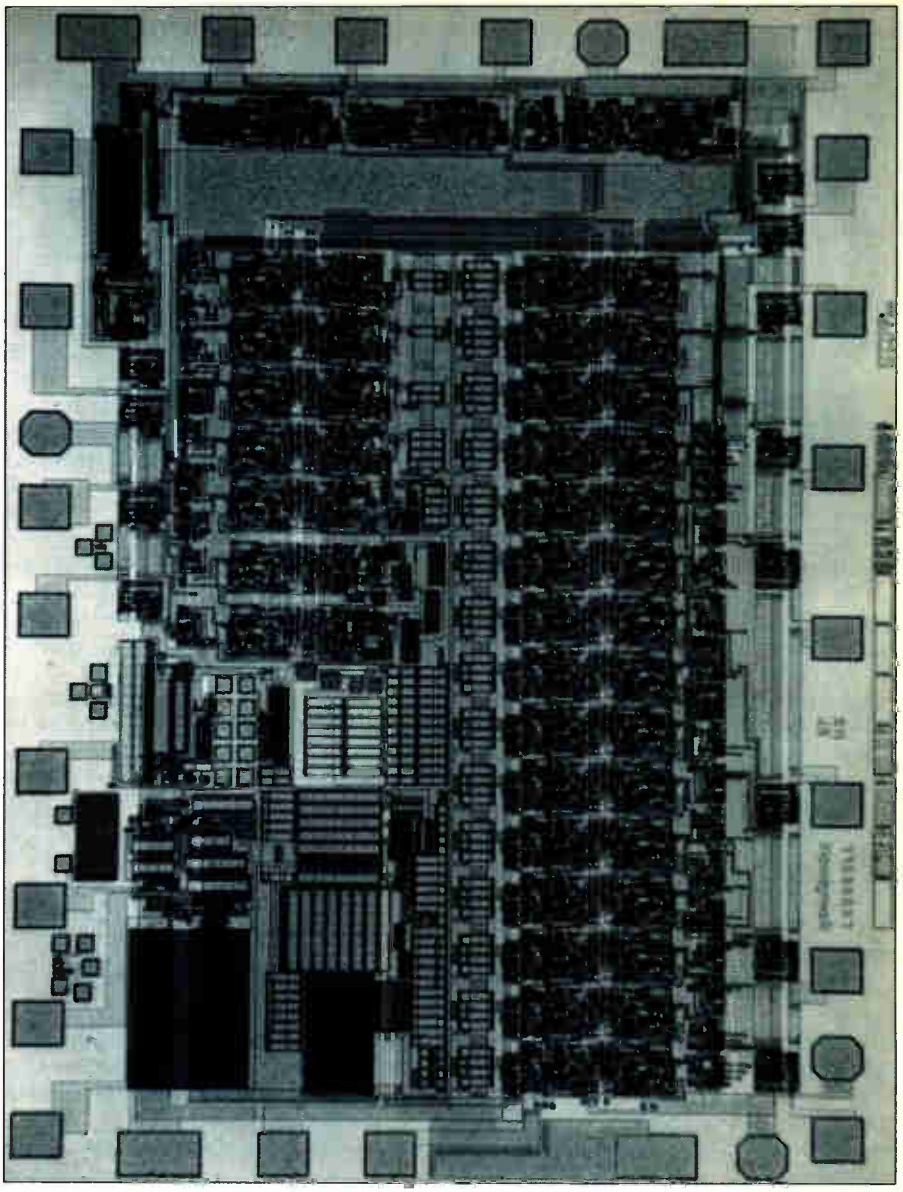
bit DAC with clock speeds in excess of 0.5 GHz (Fig. 5).

From Fairchild Semiconductor's Palo Alto research lab comes a single-poly ECL process for fabricating both analog and digital circuits. Using 2-μm design rules, the lab has recorded gate delays of 900 ps and cutoff frequencies as high as 8 GHz. The self-aligned process uses a single layer of poly that, with proper doping, forms the base, emitter, and collector contacts of the transistors. The results are high density and high speed. The lab has tested a variety of digital and analog macrocells based on the process.

An even denser circuit is under development at Hitachi Ltd.'s Takasaki Works, Gunma, Japan. It is fabricated with an advanced, mixed analog and digital, bipolar VLSI technology that combines 2-ns, 80-MHz, integrated-injection-logic gates on the digital side with 5-GHz vertical npn and 150-MHz lateral pnp on the linear side. In a typical circuit, densities as high as 10,000 I^2L gates and 1,000 linear devices on a chip are possible.

Efforts aimed at achieving truly complementary bipolar structures are rapidly gaining momentum. These are aimed at offsetting CMOS's lower active power and lower noise immunity, which are due to its complementary structure. Historically, the problem with complementary bipolar circuits has been the lack of vertical pnp devices that are equivalent in quality and performance to vertical npn devices. Compared with those of vertical npn structures, pnp parameters are less reliable and harder to control.

Researchers at Hitachi's Central Research Laboratory, Kokubunji, Japan, have come up with an analog-compatible high-speed bipolar logic process designed to overcome these problems and permit the fabrication of reliable vertical pnp transistors. The key is a technique called semi-well isolation. It uses an epitaxial layer with two different thicknesses and keeps isolation diffusion only in the thin portion. This allows thick epi layers to be fabricated without the deep isolation diffusions that previous approaches required. Breakdown voltages as high as 180 V have been achieved, with toggle frequencies as high as 50 MHz. Logic circuits formed with this technique have propagation delays as low as 35 ns/gate for I^2L and 2 ns/gate for complementary Schottky transistor logic.



5. MELTING POT. In a 0.5-GHz 8-bit digital-to-analog converter, Honeywell combines the features of 1.25-μm digital and 2.5-μm linear bipolar processes.

SHALLOW JUNCTIONS

Under development at IBM's Data Systems Division, Fishkill, N. Y., is a complementary vertical pnp/npn process that makes use of a high-dosage, boron-implanted poly layer to form the emitter. Limited to use in low-voltage digital applications and medium-power analog circuits, such devices feature breakdown voltages ranging from 5 to 18 V. Current gain is in excess of 200, and cutoff frequencies approach 3.6 GHz. The use of the boron-implanted polysilicon makes it possible to keep the silicon substrate free of defects, allowing fabrication of very shallow junctions and thin epitaxial layers.

The most far-reaching news in bipolar is the finding by device physicists and circuit designers that at the ultralarge-scale-integration level, below 0.05 μm, the rules of the game appear to favor bipolar.

"Unlike MOS, there do not seem to be any fundamental barriers—in terms of the physics of such devices—blocking bipolar technology's migration to submicron levels," says Lanny Ross, general manager of Fairchild Semiconductor's Gate Array Division, Milpitas, Calif. By comparison, he says, n-MOS and CMOS are "fraught with process and scaling difficulties, including a variety of second-order and hot-electron effects, making progress to submicron dimensions much more uncertain."

This is not to say that bipolar technology will replace CMOS as the process of choice at 0.5 μm and below, he says. CMOS has the advantage of institutional momentum: companies have committed dollars and talent to push CMOS to higher densities and speeds. Bipolar is the poor stepsister by comparison. "The most accurate assessment of the situation is that, as they have historically, bipolar and CMOS will coexist," says Ross, "slugging it out down to the smallest dimensions." □

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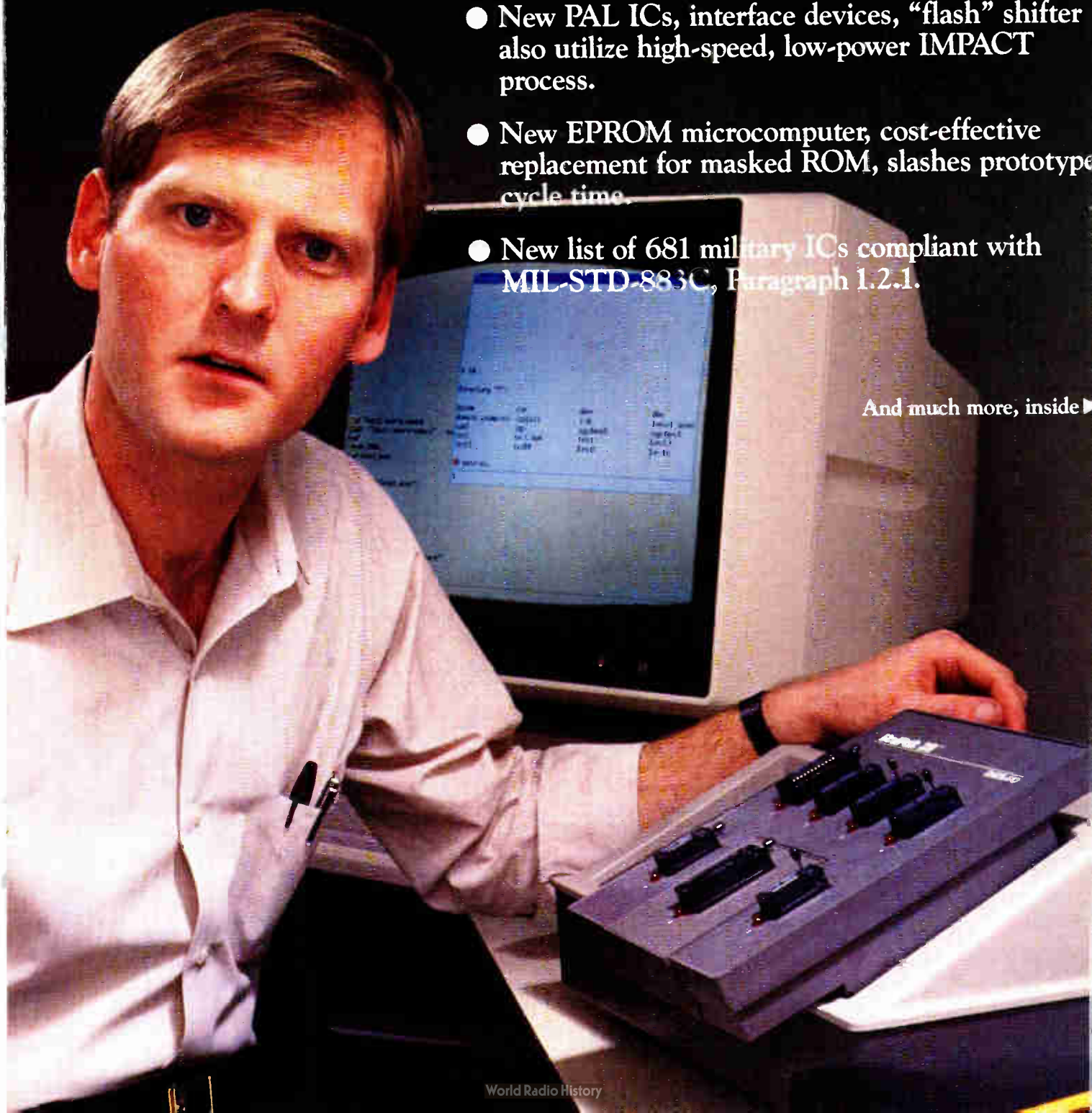

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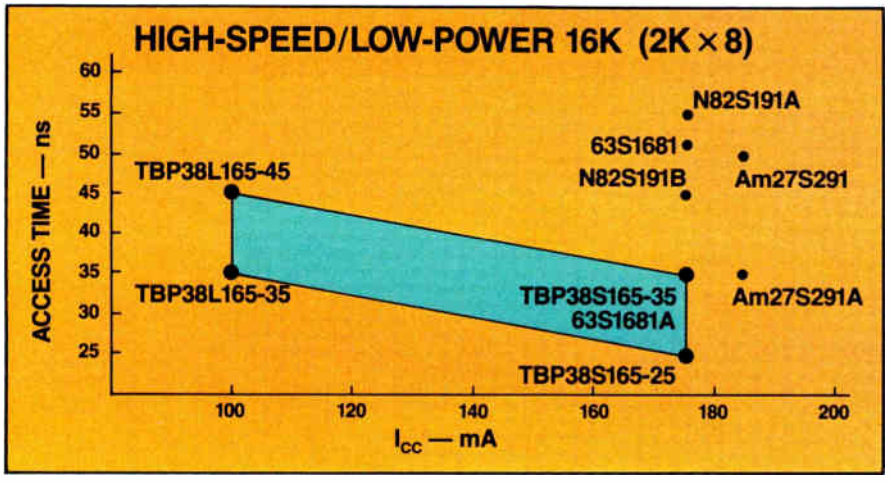

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Because of its improved clocking scheme, the IMPACT TIB82S105B is not a direct replacement for the TI or Signetics N82S105A. But it is ideal for those new high-speed state machines designed to control peripheral I/O, dynamic memory systems, and video blanking systems.

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6

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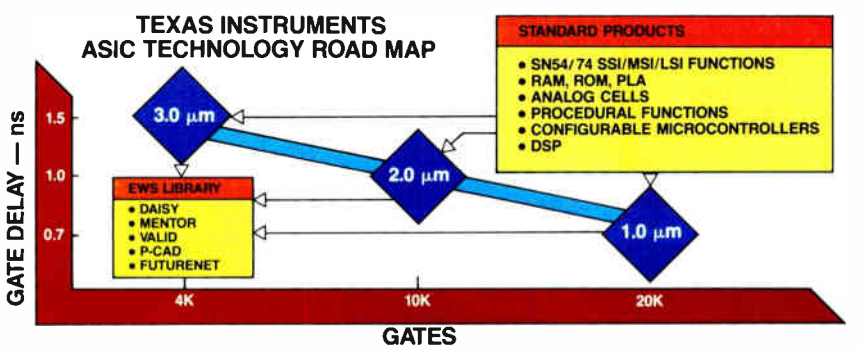

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7

New series of input-latched and registered PAL ICs lowers parts counts.

Eight new 30 MHz PAL devices from TI are the first input-latched (TIBPALT19XX) and input-registered (TIBPALR19XX) PAL ICs in the marketplace. Functionally similar to TI's TIBPAL20XX series, they include either 11 D-type transparent latches or 11 D-type input registers on chip. This added circuitry allows you to synchronize inputs without external registers or latches. These devices can reduce your parts counts and simplify your design task in a wide range of applications such as random logic, bus-interface logic, and input synchronization to custom controllers.

8

And now, a new, easy-to-use EPROM microcomputer.

TI's new TMS7742 EPROM microcomputer can cut to zero your lead time for development, prototyping, field tests, and product qualification. And it bridges the gap to ROM-based volume production. For low-volume applications, it can be a cost-effective alternative to mask-programmed ROM. Its 4K bytes of on-chip EPROM are identical to TI's TMS2732A — transferred into the chip area vacated by masked ROM. So if you can program the TMS2732A you can program the TMS7742. This new microcomputer provides EPROM capability for the TMS7020, the TMS7040, and the new TMS7042 ROM microcomputer.

Also new to TI's TMS7000 family is the ROM-less TMS7002 microprocessor. Both the TMS7002 and the TMS7042 feature 256 bytes of RAM, a serial port for USART and serial I/O functions, 32 I/O lines, and three timers. And with their 60% performance increase over earlier TMS7000 ICs, they can improve system performance in such applications as disk and tape drives, printers, and industrial and motor controls.

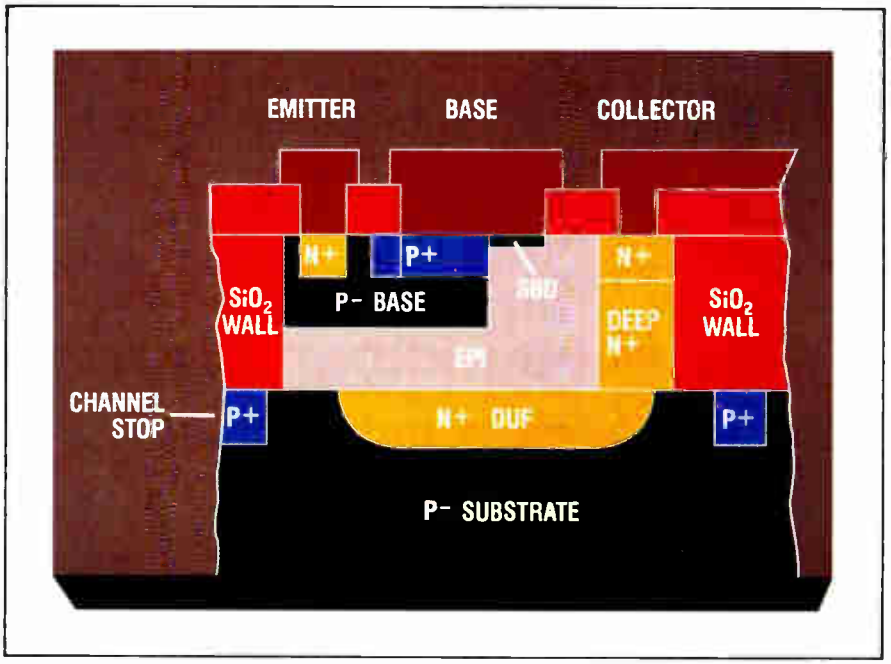
World Radio History

High-density IMPACT circuits speed logic, memory access.

TI's unique *Imp*lanted Advanced Composed *T*echnology (IMPACT) capitalizes on the advantages of ion implantation, oxide isolation, and composed-masking techniques to increase the speed and density of bipolar ICs.

This innovative technology dramatically reduces the size and the sidewall capacitance of circuit elements (*see diagram*). As a result, speed/power ratios are significantly improved: In PROMs that cut power consumption by 43%, or more than double the speed (*see story opposite*). In PAL ICs that reduce propagation delay by as much as 40% — to only 15 ns at 180 mA.

With the high speed and low power that TI's IMPACT process makes feasible, its potential for large-scale integration will reduce package counts in many high-complexity circuits.



A major reduction in capacitance results from the 2-μm feature size which TI's IMPACT processing makes possible. Silicon dioxide is the isolation material. Switching speed is further enhanced by utilizing this silicon dioxide for emitter and base sidewalls.

Composed masking yields high density

In composed masking, critical components are defined on the chip with a minimum number of masks. Thus they can be more tightly defined and more densely spaced than by conventional masking.

The IMPACT process also makes it possible to insulate critical base and emitter components with oxide walls. This insulation reduces sidewall capacitance, which, at the 2-μm dimensions of IMPACT features, can represent as much as half the overall capacitance. Small size and oxide walling together contribute significantly to the increase in switching speed.

DRAM technology spurs IMPACT growth

The IMPACT process is not a direct descendant of DRAM technology. Nevertheless, TI's commitment to DRAM production has provided IMPACT technology with vital processes.

It was the DRAM effort, for example, that drove photolithography to its present advanced state and contributed key dry-etching processes. Ion implanters designed to produce CMOS DRAM ICs enhance the quality — and the economy — of TI's bipolar IMPACT ICs. And this vital "cross-fertilization" from VLSI memory is one reason Texas Instruments — almost alone among U.S. semiconductor manufacturers — is committed to the development and manufacture of DRAM devices.

◀ **More chips per slice** help cut costs. The 150-mm wafers now used on TI's advanced MOS 256K DRAM wafer-fabrication line have 125% more area than the 100-mm slices formerly used.

World Radio History

8 new ways TI can help sharpen

1

A new alternative for memory-systems design: TI SIP DRAM modules.

Memory-intensive packaging for the future is available today — in TI's highly reliable modules in single-in-line packages (SIPs). With them you can have the many advantages of surface-mount technology (SMT) — while using through-hole-mounted or socketable packages. Thus without changing your manufacturing technology, you can increase memory density by a factor of up to 3.5 over dual-in-line packages (DIPs). And you can simplify board layout while facilitating replacement and future upgrades.

Each SIP module uses DRAM chips in plastic leaded chip carriers (PLCCs), surface-mounted along with decoupling capacitors on an epoxy substrate. Since all connection points are on one edge of the substrate, the module "stands on end" to make the most of your board area.

TI's full line of SIP memory modules — from 64K × 4 to 256K × 9 and 1M × 1 — includes standard DRAMs and Multiport Video RAMs in various organizations. And all are available through your authorized TI distributor.

For more information, just check the appropriate box on the reply card.

Memory can be 3.5 times denser using fully-qualified, production-proven RAMs configured in SIP modules. TI SIPs combine the density of surface-mount technology with economies of through-hole insertion.

2

Interface performance enhanced by TI.

Also new from Texas Instruments is an improved direct replacement for the UCN5812 vacuum fluorescent display driver. TI's TL5812 is 11% faster and draws 60% less current. With an output voltage swing of 70 V and an output source-current capability of 40 mA.

Only TI's patented BIDFET technology — combining bipolar, double-diffused MOS (DMOS) and N-channel and P-channel CMOS transistors on the same chip — makes these improvements possible. And at a competitive price.

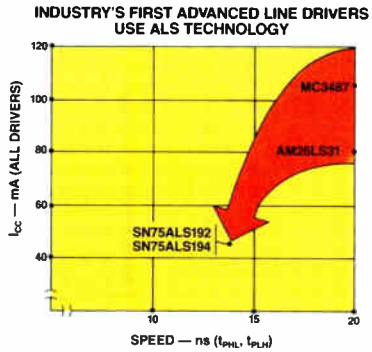
3

Fast line drivers and bus transceivers from TI.

In the new SN75ALS192/194 quadruple EIA Standard RS-422-A differential line drivers, TI's exclusive ALS 1.5 process technology (oxide-isolated Advanced Low-power Schottky) yields the best speed/power ratio in the industry: At approximately half the power consumption, these devices are 30% faster than the competition.

A new family of differential bus transceivers, SN75176B, 177B, 178B, and 179B, are faster than earlier versions. Designed for bidirectional communication on multipoint transmission lines in noisy environments, they meet EIA Standards RS-422-A and RS-485. Typical propagation time is only 22 ns.

Want to know more about these new interface products from TI? Just check the appropriate box on the reply card.



Advanced TI line drivers are 30% faster, typically draw only half the power of the devices they are designed to replace.

4

Fast, economical new 8-bit SAR A/D converters.

Now Texas Instruments offers 8-bit SAR (serial-approximation resolution) A/D converters that are as economical as any you can use. And because they use LinCMOS™ polysilicon-gate-process technology, they are unsurpassed in speed. TI's TLC549 analog-to-digital converter performs 40,000 conversion cycles per second (cps), while the new TLC548 pushes speed to an unprecedented 45,500 cps. At any supply voltage between 3 and 6 V. And typical power consumption is only 6 mW.

Performance of the serial-approximation algorithm is not only fast. It's accurate: Conversions are performed with the guaranteed low error rate of ±0.5 LSB (least significant bit) across the temperature range from −55° to 125°C.

5

681 military TI devices comply with 1.2.1.

Now designers of military electronics have the broadest choice ever of devices that comply with the requirements of MIL-STD-883C, Paragraph 1.2.1. The vast majority of TI's military ICs — 681 different devices — now qualify:

Product Type	Number
ALS/AS	83
TTL	131
LS/S	238
HCMOS	80
PAL ICs	16
Linear	113
Memory/LSI	19
MOS DSP	1
TOTAL:	681

For more detailed information on specific TI military devices, just check the appropriate box on the reply card.

World Radio History

Texas Instruments quality recognized in Tokyo and Detroit.

Outstanding Texas Instruments quality-assurance programs were lauded during 1985 both at home and abroad. In June, Ford Motor Company granted TI linear products the coveted Q1 Award. And in November, TI's wholly owned Japanese semiconductor operation received the prestigious Deming Prize. Both awards recognize exceptional levels of quality and reliability, achieved through aggressive defect-prevention programs.

First Ford Q1 Award to a semiconductor supplier

Ford Motor Company's Q1 Award to Texas Instruments Linear is the first ever to a major U.S. semiconductor manufacturer.

Qualification is based on a demonstrated defect-prevention program, along with Ford's review of warranty returns, specifically keying part numbers to failures. Thus it recognizes both initial product quality and continuing reliability.

Both quality and reliability are attributes that TI Linear has pursued aggressively through its "monitor program," begun in 1979. The goal of the program has been to achieve levels of quality and reliability equal to or better than the best worldwide competition. And the Ford Q1 Award is one visible token of its success.

First U.S. winner of Japan's Deming Prize

At ceremonies on November 11 in Tokyo, the Japanese Union of Scientists and Engineers awarded the prestigious Deming Prize for total quality control to TI's bipolar semiconductor operation in Japan.

The prize, never before won by a wholly U.S.-owned company, recognizes outstanding quality-control achievement in all aspects of business — including marketing, engineering, manufacturing, and support. It is named for W. Edwards Deming, the American statistician whose work in defining and measuring quality control in Japan after World War II became the basis for the legendary Japanese commitment to quality. In 35 years, the Deming Prize has been awarded to only 48 individuals and 111 institutions. Texas Instruments Japan, Ltd. was one of only eight companies so honored in 1985.

As is the case with the Ford Q1 Award, sensitivity to customers' requirements is a key factor in selecting winners of the Deming Prize. TI's successful commitment to quality and reliability in support of all our customers' needs has been demonstrated twice again. And TI is justifiably proud of this achievement.

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More news upcoming from TI in the next issue:

- **A new CMOS version** of TI's trend-setting TMS320 Digital Signal Processor.
- **More new additions** to TI's growing family of IMPACT PAL ICs.
- **New CMOS standard cells** and gate arrays that augment TI's leadership in Application-specific Integrated Circuits (ASICs).
- **And more ...**

For more information...

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MM09	☐ SIP memory modules	PN01	☐ TMS7742 EPROM microcomputer
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SURPRISE! ECL RUNS ON ONLY MICROWATTS

TINY TRANSISTORS YIELD VLSI DENSITIES AND ECL SPEEDS

Bipolar emitter-coupled logic has finally broken the shackles of high power and large geometries. Bipolar Integrated Technology Inc.'s BIT1 process uses 2-μm design rules and MOS-like self-aligning polysilicon techniques to shrink transistors to about 14 μm^2 and gate delays to as low as 300 ps. More important, this performance comes with a per-gate power dissipation of no more than 300 μW—about one tenth that of conventional ECL at comparable gate propagation delays.

Because the process uses the same techniques as MOS fabrication, bipolar very large-scale integrated circuits can be manufactured with existing semiconductor processing equipment. This use of standard steps and equipment enables the Beaverton, Ore., company to develop products and bring them to production without the risks and costs generally associated with new technologies.

The principal feature of the process is a very small, high-speed bipolar transistor well suited to VLSI ECL custom products, gate arrays, and memories. The total area of a minimum-geometry BIT1 transistor is 14 μm^2 (Fig. 1). Conventional bipolar technologies using ECL produce transistor areas about 20 times as large, says company president George Wilson. Transistors that big dissipate high power—typically at least 2 to 3 mW per gate and up to 8 W per chip—and limit circuit densities to about 3,500 gates per chip, far less than the 20,000 gates possible with CMOS technology. As a result, bipolar offerings generally have had to sacrifice density or speed to reduce power dissipation to levels that can be accommodated by current packaging technology.

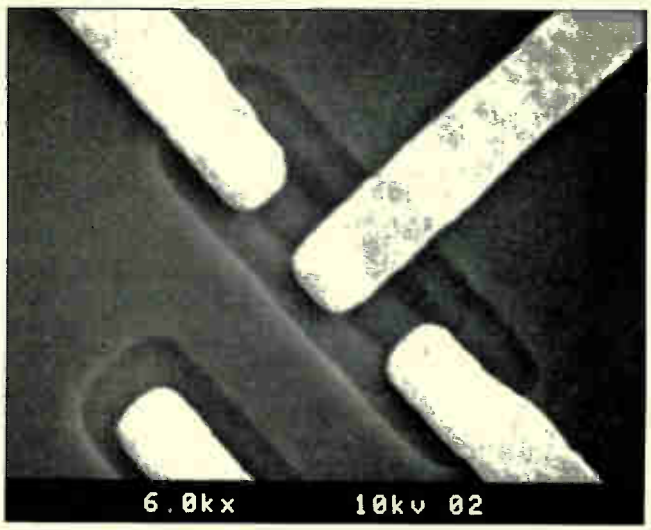
By comparison, a single two-input NOR gate using BIT1 transistors (Fig. 2) occupies 770 μm^2, allowing circuit densities equivalent to that of 1.5-μm CMOS. The company will use the process to make computational building blocks for the high-end digital signal-processing and data-processing markets. Bipolar Integrated Technology's first BIT1 product is the B3018, a 16-by-16-bit fixed-point multiplier (see related story, p. 57).

"The small device area and shallow junctions result in a very fast transistor at low currents," says Wilson. "The f_t [the cutoff, or transition, frequency] is greater than 5 GHz at 50 μA, and the junction capacitances are on the order of 5 fF." This means that the transistor can switch quickly with very low power requirements. By comparison, Wilson says, conventional bipolar transistors would exhibit f_t of 3 GHz at 2,000 μA and 50 fF of junction capacitance.

To achieve such densities and speeds, BIT1 takes advantage of poly self-aligning techniques similar to those used in sub-2-μm silicon-gate CMOS. For example, the emitter is doped from an n-type poly source and all contacts to the silicon are through poly. Other processes contact the transistor directly from the metal, says Wilson, which results in less consistently reproducible alignment. To reduce the parasitic capacitance, the resistors are also poly. They are not diffused resistors but are formed simultaneously with the base contacts.

The minimum feature size projected onto the wafer with the BIT1 process is 2 μm—"well within the capabilities of existing production photolithographic tools," says Ken Schlotzhauer, vice president of engineering. Two layers of 4-μm-pitch gold, rather than aluminum, are used for the chip's interconnection lines, he says, because the pitch is not disturbed by interlayer metal contacts (Fig. 3). Furthermore, gold handles about 10 times as much current as aluminum before the onset of electromigration.

Thanks to the self-alignment features and to the small



1. SMALL AND SPEEDY. Key to the high density, low power, and high speed of the BIT1 process is a transistor size of 14 μm^2.

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transistor area, the process is inherently high-yielding, says Schlotzhauer. The active areas occupy only 0.1% of the total die area. "As a result, the probability of a random defect that can cause a failure is small," he says.

A BIT1 ECL gate can drive interconnection capacitance about five times faster than a MOS gate of similar size because of its higher transconductance per unit of active area and the fact that interconnection delay scales with the ratio of interconnection capacitance to transconductance. Within its own speed domain, from about dc to 30 MHz, CMOS does indeed operate at lower power dissipation because it scales linearly with operating frequency. For ECL, dissipation is a constant, independent of frequency. "However, if a comparably dimensioned CMOS circuit were able to operate at the clock speeds attainable with the BIT1 process—from 100 to 400 MHz—it would dissipate much more power than BIT1 devices," says Wilson.

RETAINING THE SPEED EDGE

CMOS will continue to improve in speed, he acknowledges, thanks largely to size reduction achieved with improved photolithography. But BIT1 will retain its present 5 : 1 speed advantage because it too will take advantage of these improvements.

BIT1 achieves speeds comparable to those of state-of-the-art ECL processes, but at one tenth the power, says James Pickett, vice president of manufacturing. "In other words, for a given power dissipation, a device built with the BIT1 process will have a 10 : 1 speed advantage. The only exception is in the output drivers, where the two are equivalent." This is because the driver's power dissipation is determined by the external load, rather than internal geometries. Much of the power-delay advantage results from BIT1's high density. As a result, interconnection lengths are much shorter, significantly reducing line capacitance. This, in turn, reduces the power necessary to drive the interconnection by an amount equal to the ratio of the lengths.

The company's initial product strategy is to apply its bipolar technology to digital VLSI chips requiring high gate densities. In this category are high-complexity digital data-path elements for high-performance 16-, 32-, and 64-bit processors for signal processing and general-purpose data processing, says Les Soltesz, vice president of marketing. "The increased speed possible with the BIT1 process improves performance at the most basic level, the critical computation-cycle-time loop," he says.

The BIT1 process's speed, density, and lower power-dissipation levels offer several significant benefits to the system user. First, smaller transistors enable higher density and thereby allow the implementation of more complex functions on a chip. Second, with greater density, the system designer uses fewer parts and power requirements are lightened. As a result, the speed and throughput of the overall system are increased because the part's interconnection delay can be greatly reduced.

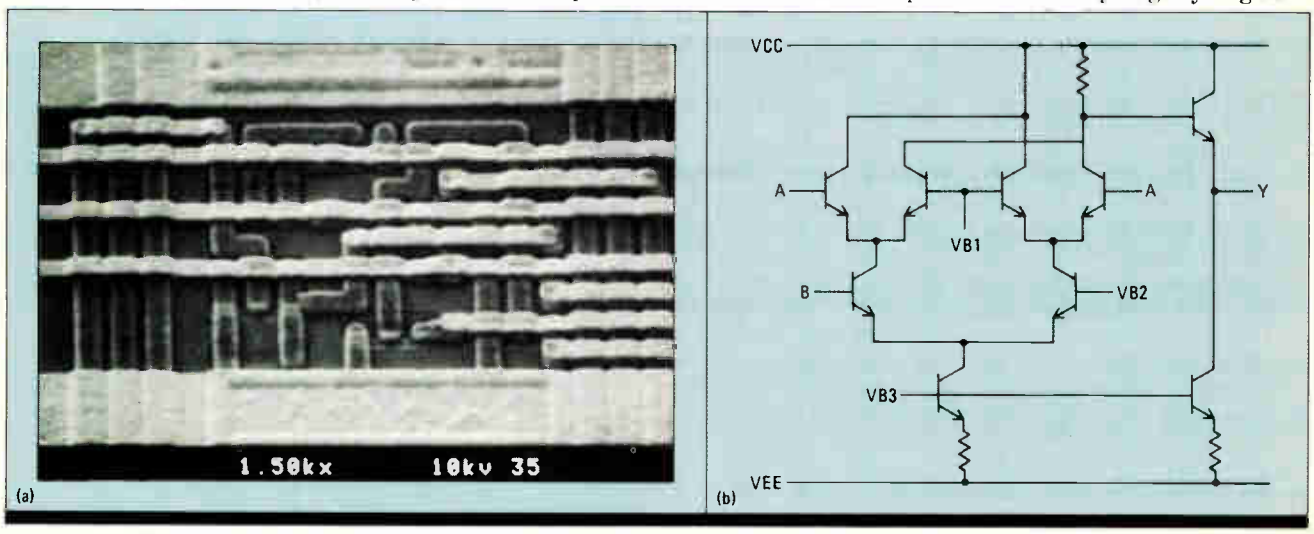
Bipolar Integrated Technology chose to make the B3018 (Fig. 4) its first BIT1 product because multipliers are basic building blocks in all high-performance processing. Wilson notes that it is a traditional test circuit for any new VLSI process because of its mix of highly regular circuitry with random logic, "as well as to meet a universal need for higher multiplier speeds." Many routine brute-force designs exist, he says, but the company's designers were able to take advantage of their process to build a circuit with a bit more finesse and imagination.

The adder array incorporates most of the conventional techniques for performing multiplication, such as modified Booth recoding, the use of a Wallace tree configuration, carry/save adders, and a carry/lookahead adder for final products. Where the company's multiplier differs, says Schlotzhauer, is that the chip was designed not only to minimize gate delay but also total delay time, where interconnection delays are critical to chip performance.

The result is an array size of 121 by 135 mils for the 11,600 transistors required. At room temperature, the adder array dissipates about 1.8 W. A typical multiplication can be performed in about 5 ns, about five times faster than current designs in both bipolar and CMOS. Interface and other functional circuits raise the multiplier's total transistor count by about 19% to 13,800 in a 166-by-178-mil area. Typical total power is increased to 2.9 W for ECL and 2.2 W for TTL.

The natural interface for parts fabricated with the BIT1 process is ECL, says Soltesz, and for this reason the company has adopted –5.2 V ECL 10KH for the fastest versions of their products. For the ECL version of the B3018, for example, the typical clocked multiply time is 5 ns, and drives terminated 50-Ω outputs, which have short delays relative to the on-chip operation times, to ensure high system speeds, he says.

"But the majority of systems are still TTL," says Soltesz. "And even with the longer output buffer delays, TTL systems can benefit from faster operation times, particularly in pipelined systems." So the company will offer TTL versions of all BIT1 products with only slightly degraded



2. CMOS DENSITIES. Fabricated with BIT1 transistors, Bipolar Integrated Technology's two-input NOR gate uses emitter-coupled logic but takes up an area of only 770 μm^2. This permits circuit densities equivalent to those produced with 1.5-μm CMOS.

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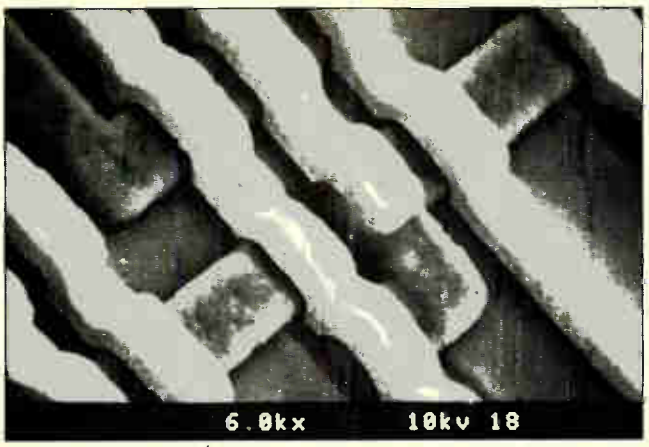


3. GOLD PITCH. In the BIT1 process, two layers of 4-μm-pitch gold replace aluminum for metal interconnection lines on a circuit.

performance. In the TTL version of the multiplier, the pipelined B2018, typical operations take 10 ns.

TTL buffers, Soltesz says, must trade off output delay, power consumption, edge-rate crosstalk, and transition-time power-supply noise generation. On the company's products, the TTL outputs have been purposely slowed to broadly match the edge rates and transition times of advanced Schottky logic for easier system design. A result is that the TTL versions have lower power dissipation than their ECL counterparts.

Taking advantage of the higher speeds and functional densities at VLSI levels their process makes possible, as well as higher pin-count packages, designers at Bipolar Integrated Technology can incorporate features in their bipolar designs which were not possible before, says Wilson. For example, in the B3018, the full 32-bit product is brought out in parallel as an independent port rather than sharing 16 bits of output with an input port as in older products. "Removing this bottleneck makes the full speed of the circuit realizable in a system," says Soltesz. However, a multiplexer is provided for use with 16-bit buses. In the ECL version, this is done by an external wired-ORing of the output so as to not introduce an additional gate delay. The TTL version does this multiplexing on chip where the additional gate delay is less than ORing of open-collector TTL outputs.

Three enhancements have been made in the way the B3018 does format adjustment, a standard feature in contemporary multiplier designs. When signed fractional data formats are used, format adjustment provides an optional single-bit left shift to align the product binary point with that of the input operands. "Normally, the left shift truncates the higher-order bit, which represents the -1.0×-1.0 product of $+1.0$," says Schlotzhauer. In the B3018, this is now detected as an overflow condition and a status flag is set, so this result is not lost. Second, the sign bit is brought out separately as an unambiguous status flag, which is correct for any format, overflow condition, or portion of the product being sent to the output.

Of more value is the addition of a lower-order zero so that the full product is numerically correct after format adjustment. This also has the benefit of making the format adjustment useful for unsigned or integer formats by always providing a single-bit arithmetic left shift. "The effect of these enhancements is that it is not necessary to make compromises in order to make use of format adjustments, only a choice of benefits," says Schlotzhauer.

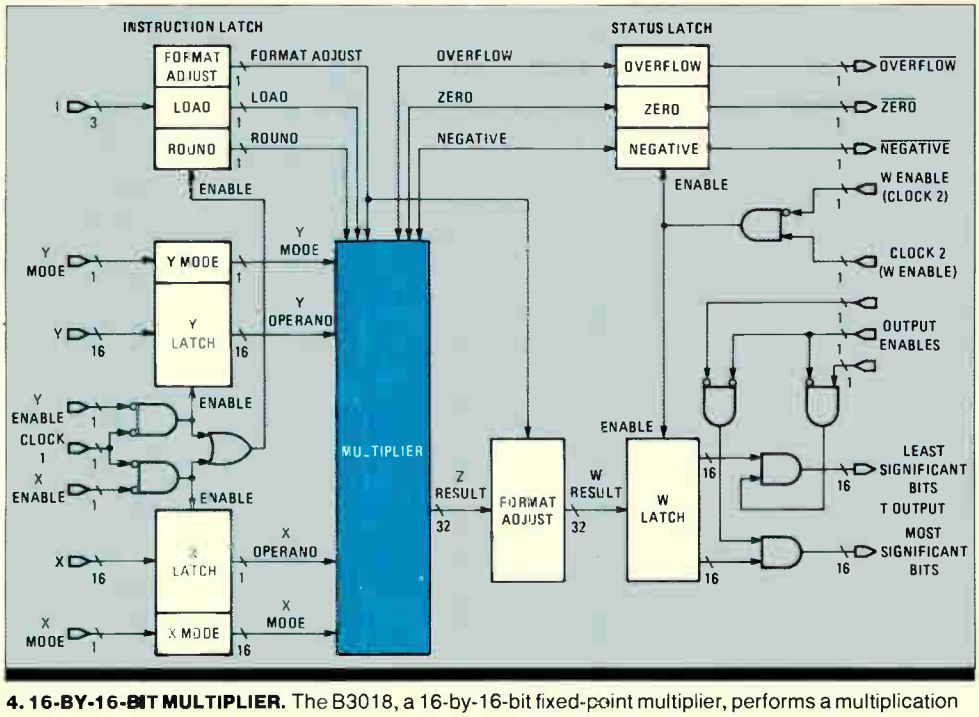
IMPROVED ROUNDING

The designers also enhanced the way the B3018 performs rounding, a valuable feature in multipliers when only the most significant 16 bits of the product are to be retained. Typically, the location of the additional bit for rounding must track the format adjustment, says Schlotzhauer. On the BIT1 chip, in addition, the zero status flag also tracks the rounding operation and format adjustment, making it correct for only the most significant format-adjusted 16 bits.

Another enhancement is the ability to load the output directly from the input operands rather than only through the multiplier, as in previous designs. In this approach, the input operands are chained into a single 32-bit result. This signed or unsigned number is then rounded, format-adjusted, and tested, just as the product is. This is valuable for use on previously generated products and variables, says Schlotzhauer, and for system test purposes. "It provides for direct testing of each function and flag as well as a direct path from the input buses to the output bus."

Also on chip are latches at all input/output data ports, says Schlotzhauer. "Clock and data skews due to printed-circuit-board wiring are a major system design consideration and require maximum flexibility in clocking and data storage to maximize bandwidth," he says. When clocked, these on-chip latches minimize delay times in pipeline operation. They are transparent when enabled, allowing the multiplier to be used for flow-through operations.

And to squeeze as much performance as possible out of the multiplier, the compa-



4. 16-BY-16-BIT MULTIPLIER. The B3018, a 16-by-16-bit fixed-point multiplier, performs a multiplication in 5 ns—some five times faster than present designs. Its 121-by-135-mil array holds 11,600 transistors.

World Radio History

ny's designers have provided on-chip gating of the latch-enable signals. Labeled as input clock CK1* and as output clock CK2, with individual enables for each latch, these latch-enable signals may be connected to configure the multiplier as a one-, two- or three-clock device. The single clock connection made by connecting CK1* and CK2 in parallel provides the edge-triggered-like operation of the master-slave latch for the whole device.

The high speed and high functional density allowed by the BIT1 process provided both problems and opportunities for the company's designers as far as packaging is concerned, say Wilson. In the B3018, he says, the ECL transition rates required short lead lengths for low inductance and resistance connections to transmission lines, impossible to do in conventional 64-pin packages.

"Also, additional pins were needed to let the additional speed and possible chip functions be truly usable," according to Wilson. But because of the low power dissipation of the BIT1 process, it was possible to use the high-pin-count, short-leaded PGA package. A special multilayer version of this package is used in the B3018 to provide a ground plane for good signal integrity and transmission-line impedance continuity.

In addition, the chip is mounted in the PGA directly on a metal slug, which provides a low profile and low thermal resistance. "The result is that, unlike other bipolar ECL implementations, no heat sink or moving air is needed under normal ambient temperatures and moderate system densities," he says.

Scheduled to be available in June, the B3018 fixed-point 16-by-16-bit multiplier is only the first of the company's new data-path elements using its proprietary BIT1 process. A fixed-point multiplier/accumulator extension to the multiplier is in the latter stages of development and will follow within months of the B3018, says Wilson.

The ECL version of the 16-by-16-bit multiplier/accumulator, designated the B3011, features dual 40-bit accumulators and full 40-bit outputs as well as double-precision shifting and transparent latches, enables, and clocks. Speed in the clocked mode will be 6 ns and power dissipation will be 3.8 W. In the TTL version, the B2011, the speed will be in the 16 ns range and power dissipation about 3 W. Also in development are a multiport register file and a floating-point chip set providing 32-bit fixed-point operations as well as 32- and 64-bit IEEE and Digital Equipment Corp. floating-point functions.

Ultimately, Wilson predicts that the application of the BIT1 process and its finer-geometry successors to general-purpose data-processing applications will allow the design of computers that hit 50 million floating-point operations per second without parallel processing. For digital signal processing, it means 100-MHz real-time processing of signals with much more than just a few bits of dynamic range, he says. □

THREE BIPOLAR ENTHUSIASTS WORKED ON HIGH-DENSITY PROCESS

For dyed-in-the-wool bipolar technologists, the electronics industry's current love affair with CMOS is a bit hard to take. Any one of them will tell you that a bipolar integrated circuit has a five-to-one speed advantage over CMOS. And with proper attention to improvements in design and circuit technology, this advantage should continue.

Three bipolar enthusiasts who bet the bank on their beliefs are George Wilson, Kenneth Schlotzhauer, and James Pickett. They are cofounders of Bipolar Integrated Technology Inc., a three-year-old semiconductor startup in Beaverton, Ore., that is just entering the market with a family of high-performance digital signal-processing circuits based on a proprietary new bipolar process.

Company president Wilson is a 20-year industry veteran who holds the patent on the industry-standard Wilson Current Source. With a BSEE from the University of Washington and an MSEE from Seattle University, Wilson's main claim to fame before Bipolar Integrated Technology was as the man who started nearby Tektronix Inc.'s IC design operation, managing the group that designed circuits and processes for over 150 Tektronix products. In addition to his 17 years with Tektronix, Wilson's experience also includes two years at Motorola Inc.'s Linear Design Group in Phoenix, Ariz.

Schlotzhauer, vice president of engineering, has specialized in bipolar technology since he received his PhD in electrical engineering from the University of Waterloo, Ont., in 1973. During his 11 years at Tektronix with Wilson, he was responsible for the design of numerous high-performance analog-bipolar ICs and led a team in developing a high-speed digital-bipolar large-scale-integration process.

Pickett, the inventor of the BIT1 process, is vice president of manufacturing and was responsible for planning and developing the company's 23,000-ft² manufacturing facility. With 20 years experience in process development, chip design, and manufacturing, Pickett worked for four years at Motorola in the Semiconductor Products Division and 14 years as manager of the IC processing laboratory at Tektronix.

According to Wilson, the company plans to focus its attention on the high end (50 to 200 MHz) of the digital signal-processing market, for which the San Jose, Calif., market watcher Dataquest Inc. predicts a cumulative annual growth between 1985 and 1989 of 37%, to $700 million.

"Currently, the product offerings in this market are divided into two broad segments, with high-performance high-power-dissipation bipolar circuits on one side and medium-performance low-power CMOS on the other," he says. But what the users really want, says Wilson, is high performance and low power. "What this means is that there is a large segment of the market that is still largely unserved," says Wilson. "We think our proprietary BIT1 process is an answer."

Also betting that the company has the answer is Analog Devices. The Norwood, Mass., company provided the seed money for the new venture as well as participating in a first round of funding that resulted in $19 million from companies and investors such as Raytheon, Iterven Partners, Banc-Boston Ventures, and Union Venture. Another first-round investor was the State of Oregon, which raised $3.9 million through an industrial revenue bond offering.

BIT PLAYERS. Bipolar veterans (from left) Pickett, Wilson, and Schlotzhauer led development of the BIT1 process.

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HOW PHILIPS SWEATED THE COST OUT OF ITS NEW SCOPES

PLASTIC CHASSIS SLASHES ASSEMBLY TIME, COMPONENTS COUNT

Philips is all set to launch an all-out drive to capture the lead in the world market for general-purpose, medium-frequency oscilloscopes. The Dutch company aims to do this with a new line of low-priced scopes that offer greater reliability and a gang of new features (see story, p. 55). Key to this product strategy is radically simplified assembly, which is made possible by shifting to a one-piece, injection-molded chassis.

The Philips effort to marry high performance, functionality, and low cost in one scope is similar to fabrication techniques that originated in the consumer products business. The one-piece plastic chassis design for mounting the component parts is common in such consumer products as radios, tape recorders, and TV sets as well as in simple industrial equipment such as voltmeters. With Philips' PM3050 family of scopes, this approach is being used for the first time to build a mechanically complex instrument.

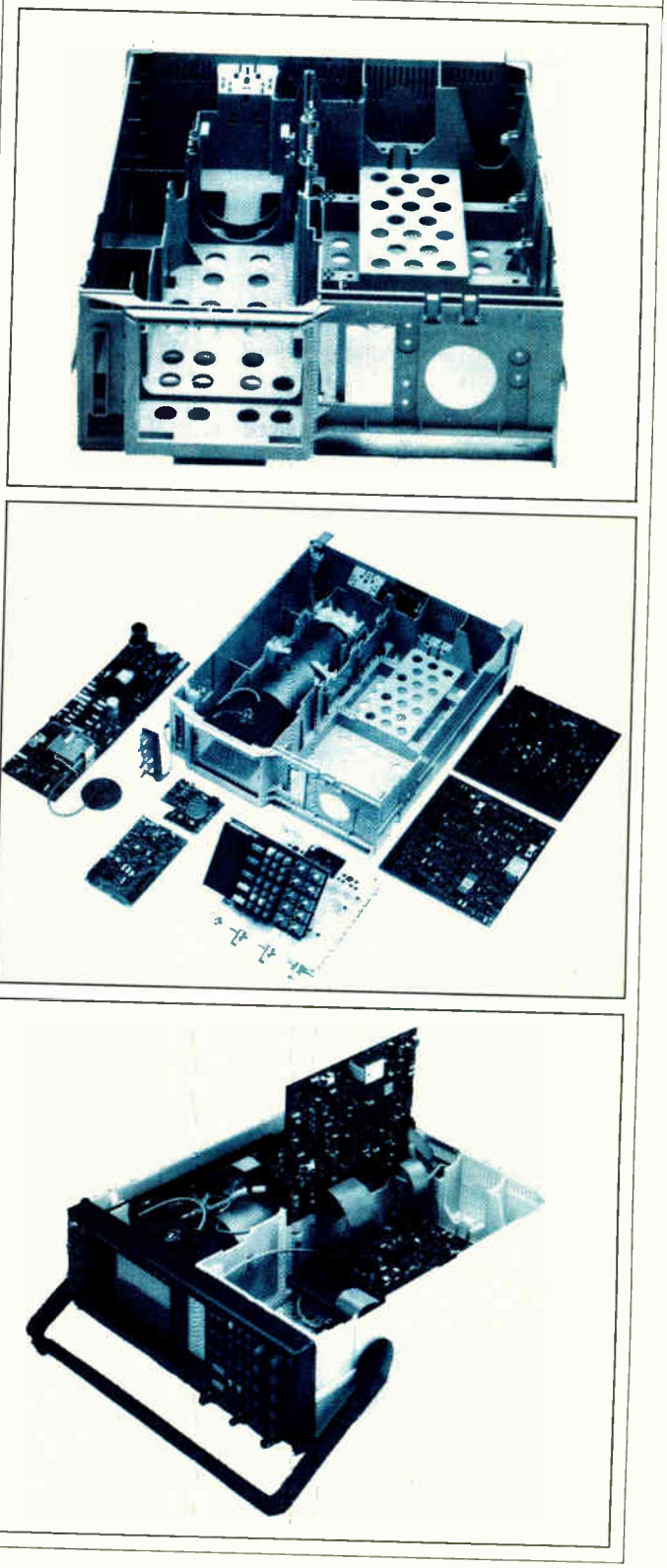
The scope line may be just the beginning for the new chassis design. "Considering the savings in assembly time it provides, the use of a one-piece plastic chassis may well become a trend in making similarly complex industrial electronics equipment," maintains Hans Fjärem, product manager for oscilloscopes at the Philips Industrial & Electroacoustic Systems Division in Eindhoven, the Netherlands.

Philips typically needs eight weeks to build, test, and calibrate a conventional general-purpose oscilloscope; that also includes stuffing the printed-circuit boards. Its new manufacturing techniques slash this process to only 5½ days. Assembling a scope takes only 20 minutes, Fjärem says, thanks to the one-piece chassis, the relatively few parts needed to mount components, modules, and pc boards as well as to the computerized test procedures (Fig. 1). In contrast, it takes an average of 10 hours to assemble the company's other models.

Because of this simpler, faster process, the PM3050 family will cost less than competitive low-end models—even from Japanese companies, Philips says. For example, a single-time-base model will cost $1,245 in the U. S. The family has two members so far: the basic single-time-base model 3050 and the dual-time-base 3055. Philips will unveil them at the Hanover industrial fair, which starts its eight-day run in West Germany on April 9.

The new chassis is made of a plastic called Bayblend, a mixture of acrylonitrile, butadiene, and styrene with polycarbonate, supplied by Bayer AG. This material was chosen for its strength and rigidity down to –40°C. Fjärem says that most other materials turn brittle long before that point, and this can cause the chassis mounting fixtures to break off. A Bayblend chassis can also withstand high temperatures—up to about 75°C. Bayblend is nonflammable and self-extinguishing, in accordance with standards specified by such organizations as Underwriters Laboratories in the U. S. Furthermore, the material is nontoxic and its color remains consistent from one batch of plastic to the next. It easily fulfills shock and vibration tests when military standards specify them.

The Philips chassis comes equipped with most of the click-



1. SIMPLIFICATION. A one-piece plastic chassis (top), snap-fit subcomponent mounting, and a sharply reduced parts count (center) make it easier to assemble and service (bottom) Philips' new PM3050 family of oscilloscopes.

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fit mountings, snap-in fixtures, stops, posts, and guides needed to mount or insert the instrument's eight basic functional modules—an attenuator, a vertical amplifier, X- and Y-amplifiers, a time-base unit, a cathode-ray-tube control, a power supply, a front-panel control unit, and a liquid-crystal display unit. Only a few nonintegrated fixtures are needed to retain cables and to hold certain other parts in place. In-place guides for the wiring contribute to a neat internal layout (Fig. 2).

BOARD-MOUNTED CONTROLS

In assembly, only two screws are required to fasten the top and bottom cover plates to the chassis. All switches, potentiometers, and push buttons come mounted on a pc board. After this board is in place behind the front panel, no screws or other parts are needed to install the scope controls.

The one-piece chassis contrasts fundamentally with a conventional scope's frame. Such a frame includes many individual parts, usually in the form of pressed metal sections that must be screwed or welded together—a time-consuming and labor-intensive operation, as is attaching or screw-mounting the CRT, pc boards, cables, front-panel controls, and other components. What's more, gaining access to the various modules for service and repair may be difficult and require considerable dismantling.

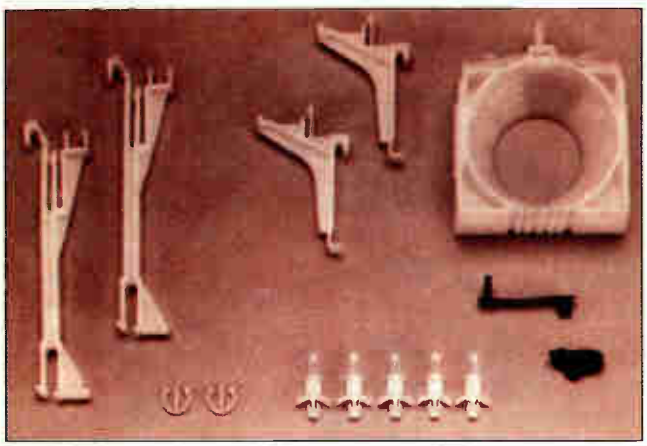
By contrast, the new Philips chassis offers a number of advantages. For one thing, it serves as a convenient mounting jig clearly defining the exact position in which the components and modules are fitted. This further simplifies and speeds assembly. The box-like chassis, closed at the bottom and all four sides, affords easy access from the top.

High assembly accuracy is another plus. This accuracy is built into the chassis die; this means that mechanical tolerances need not be continuously monitored as might be necessary in putting together a conventional scope. The plastic chassis construction also makes it easy to get to components during servicing. Servicing a faulty module involves nothing more than loosening a screw to remove the top cover. The pc boards then hinge upward or can be raised and placed in slots for access to both sides. Plug-in flat-cable wiring allows quick board replacement with no soldering. The West German company IBS is producing the chassis for Philips (Fig. 3).

Another advantage of the integrated chassis is a logistical one. Because most fixtures are already part of the chassis, less hardware for mounting components needs to be kept in stock. By contrast, a conventional oscilloscope might call for hundreds of different small parts, including screws, washers, spring clips, and the like, for installing the components onto the frame.

In addition, the lightweight (1.5-kg) plastic chassis is about two and a half times less expensive than a metal frame for a conventional scope of comparable dimensions, yet it equals the latter's strength and rigidity. At first, Fjärem says he was skeptical about using a plastic chassis for industrial equipment; Philips' styling and standards committees had similar reservations about the wisdom of the design. But given the improvements in the quality of these materials, Fjärem became an advocate of the approach and convinced the company of its advantages.

2. SNAPFIT. Only a few additional nonintegrated fixtures, which snap into holes molded into the chassis, are required to hold parts in place.



HIGH-TOOLING COSTS

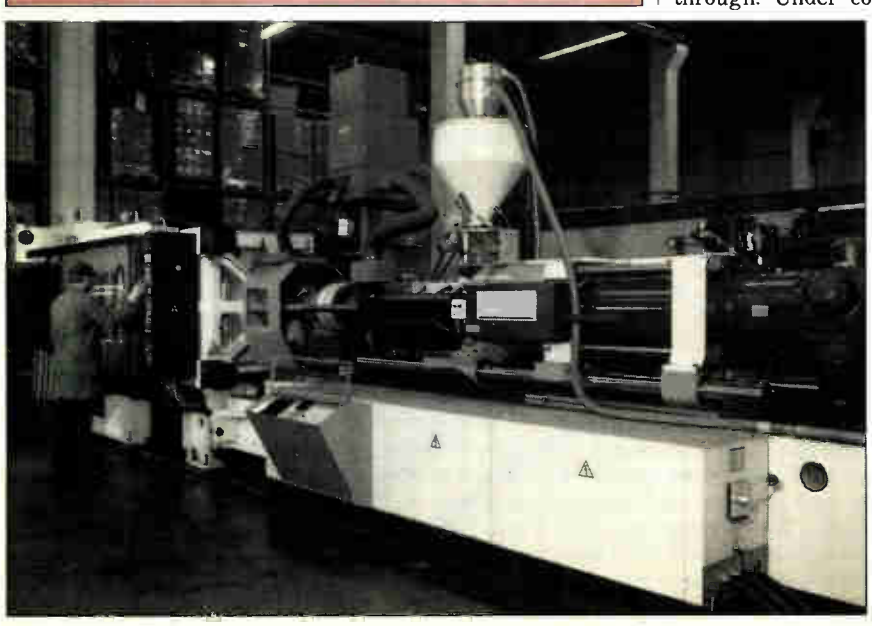
The one piece of bad news is that a one-piece plastic chassis involves high tooling costs—about seven times higher than what Philips pays for making the tools for a multipiece metal frame. For the plastic version, the company spent some $280,000 for tooling—half for die design and engineering, half for actually making the die.

Still, that expense can be recovered many times over by the saving from the quick assembly time, according to Fjärem. With most attachment fixtures already integrated into the chassis, the assembler simply inserts or snaps the pc boards, CRT, power supply, and other modules into place.

Several measures combine to achieve the short flow-through. Under computer control, a components-sequencing system takes all devices—such as diodes, resistors, capacitors, and transistors—from their packaging tapes and puts them on a new tape in the order needed for mounting them in the board assembly. Automated processes then place and solder the devices onto the board.

Another speed-enhancing measure—the use of an automated module test system on the 3050 production line—also makes for high finished-product quality levels. Testing at module levels—interim testing, as it is called—ensures that no faulty modules are ever built into an instrument. Interim testing also cuts the final test and calibration time.

When necessary, modules are adjusted during testing to bring them to specified performance tolerances. Any fault-finding



3. PRESSING ON. A giant injection-molding machine from IBS required a complex die design to produce the one-piece chassis.

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and module repairs take place off-line so that repairs do not slow down overall scope assembly. In conventional fabrication, a defective module can remain undiscovered until final, post-assembly testing. By that stage, spotting and diagnosing faults can be a time-consuming process that slows down the factory's output rate.

HIGH-PERFORMANCE FEATURES

The scopes that result from this new fabrication approach boast the specifications and user features that put them into the realm of high-performance instruments. For example, a microprocessor-controlled autoset key on the 3050 series automatically optimizes settings for deflection amplitude, timebase, and triggering to bring a signal into range, allowing the displayed trace to show up without the need for time-consuming manual settings. This autoset key is a common feature on Philips' higher-frequency oscilloscopes, but this is the first time it has ever appeared on any low-cost, general-purpose, medium-frequency instrument, says Fjärem.

Both new oscilloscopes also use an uncommonly high acceleration voltage on the cathode-ray tube—16 kV—compared with only 12 or 14 kV for many other units. This makes for high write speed and greater light output for a brighter trace, especially at high sweep speeds. Another feature is the use of rocker-switch controls. Such switches are less bulky, more reliable, and more durable than commonly used rotary controls. A backlit auxiliary liquid-crystal display (for control-setting readouts, parameter values, and menus) and softkey-programmable switch functions are also unique to scopes of this class, says Fjärem.

As an option, the scopes can accommodate a separate IEEE-488 general-purpose interface bus (GPIB) adapter. In addition to enabling operation in automated-system environments, this option is handy in automatic performance verification and calibration programs that use an external computerized metrology system. □

SELLING THE NEW CHASSIS IN-HOUSE WAS THE HARDEST PART

"A major task in developing the 3050 family was explaining to our in-house styling and standards committees why we took the route we did for the oscilloscope's mechanical construction and other design aspects," explains Hans Fjärem, product manager for oscilloscopes at Philips's Industrial & Electroacoustic Systems Division. Fjärem is the man behind the 3050 project. "Not that the committees objected to our proposals," he says, "but the design was just so revolutionary that they had to take a long second look before approving it."

The 35-year-old Swedish-born Fjärem has more than 12 years of experience in instrumentation, all of it at Philips. Starting in 1968, he serviced instruments for three years in Sweden. Then he attended a private engineering school in Stockholm, graduating with a BSEE in 1974. He went back to Philips to head service operations of numerical control systems and other industrial equipment in the Nordic countries.

There followed a two-year stint in Toronto, where Fjärem was responsible for servicing Philips test and measurement equipment in Canada. Back in Europe in 1978, he worked in Sweden again and then in 1982 became product manager for oscilloscopes in Eindhoven, the Netherlands.

From the outset, the Philips manager was confronted by a major task: synchronizing the efforts of the many groups involved. Participating in the project were not only electronics specialists but also mechanical engineers, production staff, logistics experts, and outside suppliers.

"Another problem was finding a plastics supplier that could come up with the right mix of materials that would meet our needs for strength, rigidity, and low and high temperature resistance of the one-piece injection-molded plastic chassis," he says. "We finally found that supplier in Bayer AG."

Fjärem emphasizes how constructing the chassis called for close cooperation between Philips and West Germany's IBS, the maker of the die for the chassis, as well as with Bayer, the supplier of the plastic material called Bayblend.

"To help optimize the die design, Bayer used a special mold-flow computer program," notes Fjärem. The program determined, for example, that the number of injection points must be raised from the usual two to three in order to ensure optimum material flow into the die's complex contours. "Indicative of the die's complexity is that the drawings needed to produce it encompass no fewer than 1,250 different dimensions," says Fjärem.

Philips invested heavily—around $5.4 million—to get the 3050 family ready. During the two and a half years Fjärem coordinated the design and development, the company's Industrial & Electroacoustic Division spent about $2.8 million for engineering, 10% of that for designing and producing the die needed for injection-molding the chassis.

LEADER. Fjärem says Philips will lead in general-purpose scopes.

The division spent another $2.6 million to start up production, make the tooling jigs, and build the equipment for production testing. In all, the division spent 60 man-years to engineer the scope and another 10 man-years to develop the software for the test equipment.

Given the low price and high performance of these instruments, Fjärem is convinced that Philips will become the top contender in the general-purpose, medium-frequency oscilloscope market. Citing an unnamed U. S. consultant, he says the world market is currently dominated by Tektronix Inc., which is figured to have a 45% share of the world's total market. Together, about eight Japanese oscilloscope makers claim a 20% share. Philips checks in with 12.5% of the market.

To hear Fjärem tell it, the 3050 will change that ranking: "We are clearly going for market leadership. The targets are a 30% slice of the global market during the first year after the family's launch and a share approaching 50% during the second." In some countries, notably those in Europe, Philips' goal is to double market share within the first year from the current average of 30%.

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PROBING THE NEWS

JAPANESE SUPERCOMPUTERS: THEY HAVEN'T TAKEN OVER YET

BUT DON'T START CELEBRATING: THEY MAKE GOOD PROGRESS AT HOME

by Charles L. Cohen

TOKYO

Three years ago, the U. S. was being warned that Japanese supercomputers were going to take over the world. At the very least, authorities from industry and academia predicted ominously, the U. S. lead in supercomputers was in imminent danger of evaporating.

That hasn't been the case. The immediate threat has been headed off by American makers' ability to improve price/performance figures and by such moves as the $200 million National Science Foundation grant establishing five centers to perform research and development using supercomputers [*Electronics Week*, March 4, 1985, p. 13].

But don't start the victory celebration yet. The experts now say that the real measure of just how far the Japanese have come is not so much how many machines it has sold around the world; it is the proliferation of the giant number-crunchers in Japan itself.

Kenneth Wilson, the Cornell University physics Nobel laureate, speaks for these experts when he says, "I think the key issue is how many Japanese machines are sold in Japan and how many people are getting training on them." The outcome of the race now hinges on the relative success of Japanese and American engineers and scientists in harnessing the supercomputers to develop new products and new science—using them, in effect, as progress engines.

That is where the Japanese have made considerable progress. Where formerly only two or three government laboratories and Tokyo University housed machines, by the end of this year the room-size supercomputers from the three Japanese manufacturers—Fujitsu, Hitachi, and NEC—will be running in perhaps 11 academic organizations,as well as in private firms (table).

The Japanese train users and develop products with them

The Japanese are using their supercomputers for everything from attracting engineers and scientists to developing products. At the University of Tokyo Computer Center, associate professor Yasumasa Kanada says that many supercomputers will be sold because they help companies recruit the best university graduates, and brighter employees coupled with better tools should prove to be a winning combination.

Medium-size manufacturers are also using the new supercomputers to shorten development cycles, says computer watcher Yuji Ogino, managing director of IDC Japan Ltd. Many will not admit it, though; Yasumasa Sakano, general manager of Fujitsu Ltd.'s Computer Systems Marketing Division, says that many companies insist that supercomputer orders be kept confidential to prevent further exacerbation of trade frictions with the U. S.

AHEAD IN HARDWARE. Trade frictions aside, the power of the supercomputer as progress engine ultimately hinges on improvements in hardware, and the Japanese are making significant strides in this arena. For more than a year, NEC Corp. has boasted that its SX-2, with a speed of 1.3 billion floating-point operations/s, is the world's fastest supercomputer, beating out the Cray-2 (1.2 gigaflops) and Fujitsu's VP-400 (1.14 gigaflops). Now reports circulating in Tokyo say Hitachi will deliver a machine with a peak speed of 1.6 gigaflops to the government's Institute for Molecular Science in Okazaki in the summer of 1987.

FROM THE LEADER. Fujitsu, with 22 systems sold in Japan, is the leader. Half the installations are the bottom-of-the-line VP-50 system.

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SCORECARD OF JAPANESE SUPERCOMPUTER INSTALLATIONS

Organization	Model	Maker	Government funded
Advantest	VP-50	Fujitsu[1]	no
Central Research Laboratory, Hitachi	S-810/10	Hitachi[2]	no
Chiyoda Chemical Engineering & Construction	VP-50	Fujitsu	no
Computer Center, University of Tokyo	S-810/20	Hitachi	yes
Fuji Electric	VP-50	Fujitsu	no
Hitachi Works	S-810/10	Hitachi	no
Houston Area Research Center	SX-2	NEC[3]	no
Institute for Molecular Science	S-810/10	Hitachi	yes
Institute of Plasma Physics, Nagoya University	VP-200	Fujitsu	yes
Ishikawajima-Harima Heavy Industries	VP-50	Fujitsu	no
Japan Atomic Energy Research Institute	VP-100	Fujitsu	yes
Kyoto University	VP-200	Fujitsu	yes
Kyushu University	VP-100	Fujitsu	yes
Matsushita Electric Industrial	VP-100	Fujitsu	no
Meteorological Research Institute	S-810/10	Hitachi	yes
Musashi Works, Hitachi	S-810/10	Hitachi	no
National Laboratory for High Energy Physics	S-810/10	Hitachi	yes
NEC Scientific Information System Development	SX-2	NEC	no
Osaka University	SX-1	NEC	yes
Power Reactor and Nuclear Fuel Development	VP-100	Fujitsu	yes
Recruit Co.	VP-400	Fujitsu	no
Tohoku University	SX-1	NEC	yes
Toyota Motor	VP-100	Fujitsu	no

[1] Fujitsu has 22 orders in Japan, of which it has shipped about half. It has also received 13 overseas orders, but the only U. S. purchaser has been Amdahl. Those listed are the only ones disclosed.

[2] Hitachi has received nine orders, but discloses only six of its customers. Seven of the computers are in operation.

[3] NEC has received four orders, including one from a subsidiary that acts as a service center for NEC users. The in-house systems are used only for hardware and software development.

SOURCE: *ELECTRONICS*

To beat out that kind of competition, Americans would have to deliver machines that are better and cheaper, says Sakano. He apparently does not expect to see that happen soon and, in fact, expects Japanese supercomputers to maintain their high market share at home—his company has 60%. He says there are six Japanese orders for Crays; these he sees primarily as attempts to alleviate trade friction.

Although other sources point out that U. S. supercomputers can sometimes be a better deal because of the larger amount of application software available, Sakano claims that his company's products are attractive to 80% of the mainframe user base in Japan that has IBM Corp. machines and compatibles from Fujitsu and Hitachi. That reflects the Japanese strategy of making their machines IBM-compatible so that they can acquire a broad user base fast.

All this makes the home market a heated one. Based on orders and installations, Fujitsu is in the lead with 22, followed by Hitachi with nine. NEC, with four, has had the slowest start: it was the last to announce and ship products, and neither its mainframes nor its supercomputers are compatible with those of other companies.

Kunio Okuwa, a marketing manager at NEC, says his company's strategy is different from Fujitsu's, whose sales are heavily skewed toward its bottom-of-the-line VP-50. He says NEC aims at the higher-performance area and claims its SX-2 has attained the world's highest sustained performance.

U. S. CHANGES. Eventually, Japanese manufacturers are going to have to go after the biggest market, the U. S., where it is estimated that there will be 1,675 installations by 1990, up from 286 at the end of 1986. But that market has changed considerably: for one thing, where once there were only Cray and Control Data Corp., now several dozen new entrants are aggressively marketing minisupercomputers.

These companies bring renewed vitality with new operating systems and languages to what has been a very conservative user community wedded to Fortran. They also add to the size of the market that Steve Wallach, vice president of technology at minisupercomputer maker Convex Computer Corp., says must reach $1 billion before IBM will decide to offer a full-fledged supercomputer.

IBM already has gotten its feet wet with an almost-supercomputer in the form of its Vector Facility [*Electronics*, Feb. 3, 1986, p. 35] for the 3090 mainframe. But whether it is a full-fledged player or not, Big Blue has the others looking over their shoulders.

Fujitsu offers an example of IBM's power. Fujitsu general manager Sakano admits that IBM's Vector Facility is competitive with his firm's high-volume VP-50, offering about two thirds the peak processing power at a much lower price. Marcelo Gumucio, executive vice president for marketing at Cray Research Inc., says, "I can only speculate that Fujitsu [which is selling through Amdahl] was counting heavily on IBM compatibility."

But the IBM Vector Facility killed that hope and "really made it very difficult for Fujitsu to be successful," he says. Not only did IBM offer vector-processing power at a much more attractive price/performance ratio than offered by Fujitsu; when it added its own Vector Facility, it made changes that wiped out Fujitsu's compatibility.

Hitachi is not offering its supercomputers in the U. S., but it would have the same problems if it were. NEC, which has made one sale in the U. S., still has the problem of selling equipment with a unique operating system.

Interestingly, Hitachi and NEC have long offered optional integrated array processors for vector computation—the equivalent of IBM's Vector Facility. In NEC's ACOS 2000, the array processor is standard equipment. Thus U. S. purchasers of Hitachi computers from National Advanced Systems and NEC computers sold by Honeywell Inc. will have enhanced vector-processing capability. Fujitsu no longer offers an array processor because its VP-50 is a better deal.

Although Cray is No. 1 worldwide in supercomputers, IBM could follow the path of the Japanese and start out achieving far higher economies of scale than Cray even at a lower production rate. NEC's supercomputers have been used as a test vehicle for developing packaging and integrated circuits for its mainframes. Hitachi's and Fujitsu's are modifications of their mainframes.

But hardware economy limits manufacturers to the technology used in mainframes. Though Japanese semiconductors are not as innovative as Cray's gallium arsenide and ETA's cryogenic CMOS chips, the government's high-speed computer project will most likely build a supercomputer with high-electron-mobility transistors (HEMTs), improving the price-performance ratio of their machines. Meanwhile, mainframers are building up capabilities in GaAs and HEMT devices and are researching Josephson junction devices. □

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CAN IBM'S NEW LAPTOP BUILD A VOLUME MARKET?

THE INDUSTRY THINKS NOT; FOR SOME, A 'GIANT YAWN'

by Robert J. Kozma

NEW YORK

It's put-up-or-shut-up time for the laptop computer market. Having limped along as it waited for the big guy—IBM Corp.—to show up, this embryonic business finally has a Big Blue product to run interference: the IBM PC Convertible. Few doubt that IBM's long-awaited entry into the market last week is going to get things moving—if there is indeed a laptop market to be moved.

By no means can that be assumed. Though IBM's presence legitimizes the laptop as nothing else can, it offers nothing surprising in the way of new technology that would open up the market. "We have only the briefest of information, and it has probably extracted a giant yawn," says John V. Roach, chairman of Tandy Corp., which pioneered the laptop market a few years ago with a line of non-IBM-compatible laptops.

The Convertible "has no new technology in it. It is basically the same as we are using in our laptop," says Charles Boyd, manager of the Computer Systems Division at Texas Instruments Inc.'s Data Systems Group in Austin.

At Compaq Computer Corp., which pioneered the heavier "luggable" personal computer, president Rod Canion still doubts that IBM will be able to pack enough new technology into a laptop form factor to dramatically change the market's potential. Canion, however, promises that if his engineers see enough in the IBM design, they can develop their own laptop in six months.

IBM's battery-driven 12-lb machine, as expected, uses 3½-in. disks and comes with a liquid-crystal display—a screen that's the Achilles' heel of most current models, though IBM says its design is new and improved. At $1,995, it's cheaper than comparable products now being sold, but that is still not a mass-market price, according to some experts.

More important, the new entry does come from IBM, the market maker. "This is a valid product that can't be dismissed," says John McCarthy, research manager at Forrester Research Inc., Cambridge, Mass. "Just the IBM nameplate will give it credibility."

The real question is: how many laptop personal computers will be sold this year? More, of course. The market has already been stimulated by Zenith Electronics Corp.'s well-publicized win [*Electronics*, March 3, 1986, p. 16], over IBM for 15,000 machines for the Internal Revenue Service. Demand "won't jump through the roof," predicts Forrester's McCarthy. He says laptop shipments this year will probably double, hitting from 120,000 to 135,000, depending on how fast other vendors enter the market or bring out improved products. In 1985, 50,000 to 65,000 units were shipped.

John Frank, marketing vice president at Zenith Data Systems, a Zenith subsidiary in Glenview, Ill., tends to agree.

VERSATILE. IBM's PC Convertible features a specially designed liquid-crystal display, but a CRT monitor (top) can be added.

"The IBM entry will further stimulate general interest in portable computing," he says. So does Tandy's Roach: IBM "will certainly make the laptop market marginally larger just because there are more people in the business now, but there has not been any shortage of quality products."

The Convertible "will not make that much of a difference" in market size, says Charles Boyd, manager of the Computer Systems Division at TI.

Data General Corp.'s Cliff Bream likes the added visibility for the market—in which its Data General/One at $2,195 is not exactly breaking sales records—but adds, "I'm not going to say the IBM announcement has made our day." Bream, vice president and general manager of the distribution division at the Westboro, Mass., company, says the market suffers because customers do not understand either the role portables can play in their computer solutions or the functionality available in the current generation of machines.

HOME AND OFFICE. To some industry observers, however, the new IBM laptop is really aimed at a far larger market. Thomas Rooney, an analyst with New York investment company Donaldson Lufkin Jenrette, views the machine as basically an office model. "I do not believe there is a substantial market for a laptop computer," he says, adding that he doesn't think IBM does either. IBM, he says, is looking at the Convertible as a small-scale low-cost desktop machine that a user can take home. "IBM promoted it as much as a desktop machine as they did as a true portable," he says. "It's a better use of space than a standard PC." He thinks IBM agrees.

"Unless they're fools," he says, "they see a bigger market out there for this thing than just laptops." With its high-speed production line—Rooney estimates IBM can make one Convertible every

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six minutes—IBM "could fulfill the entire [laptop] market demand in one week. Ultimately it will be successful as a very good office computer."

IBM is pitching the Convertible not merely as an easy-to-carry personal computer, but as a tool that can be used at home, on the road, or in the office. William C. Lowe, president of IBM's Entry Systems Division in Boca Raton, Fla., touts the machine as the second computer for those who already have one. He claims three important attributes: it offers improved readability over other laptop products on the market, it is fully compatible with other IBM PCs, and it's a desktop as well as a traveling machine.

One contribution the Convertible could make is its 3½-in. disk drive. Zenith's Frank believes that IBM, which invented the floppy-disk drive, could provide the impetus that moves the market to the new 3½-in. size. "If anybody can get 3½-in. drives to be more universally accepted in the marketplace, it's obviously IBM. I don't, however, see an immediate mass movement to 3½-in. drives. It will take some time before 3½-in. drives would actually displace 5¼-in. as the new industry standard."

The product has twin 740-K, 3½-in. disk drives. To let users exchange data between the Convertible and other IBM PCs, the company is introducing an external 3½-in. disk drive that hooks onto existing IBM products.

BETTER DISPLAY. The machine uses a specially designed LCD that IBM says provides good readability because a new technique bonds an antiglare filter to it with minimal distortion. IBM also redesigned the character font for greater readability. The Convertible's LCD panel is detachable, and IBM has two new CRT monitors—one color, one monochrome—that attach to the Convertible for use in the office.

The $1,995 price disappointed some. Frank notes that although "it's an attractive price point," whether it will stimulate downward pricing pressure in the market is "always related to what the product brings to the party."

TI's Boyd says, "Our feeling is that the price-sensitivity point is significantly lower than that. The market data we have had for the past year shows the price point to be down toward the $1,000 range to generate a lot of interest in the market. I think it will take the next generation of technology."

But McCarthy of Forrester thinks "some real vertical target markets—such as sales/distribution, auditing/accounting, and insurance—will jump for this. The big thrust in the next few years will be to sales-force automation, to get control of the sales call," and the Convertible could prove just the ticket.□

IBM SQUEEZES THE PC DESKTOP COMPETITION

A laptop computer wasn't all that IBM Corp. announced last week. The Armonk, N. Y., giant also cut prices by up to 25% on its existing Personal Computers and beefed up the PC line with speedier machines. The reason is simple: it wants to stay ahead of—and make things tougher for—its competition.

"You can expect very frequent announcements and enhancements," says William C. Lowe, president of IBM's Entry Systems Division in Boca Raton, Fla. IBM's announcements will be "frequent enough so that the competition will have to move fast to stay competitive."

One IBM watcher thinks the company could have made things harder on other suppliers. "I was surprised that IBM didn't dramatically cut the price of a PC with two floppy-disk drives," says John McCarthy, research manager at Forrester Research Inc., Cambridge, Mass. IBM reduced a PC with dual 360-K floppy drives by 13%, to $1,995 from $2,295. "You would have thought that they would get closer to the competition," McCarthy says. The analyst believes IBM doesn't want a price war with the cheaper Far East-made PC-compatibles.

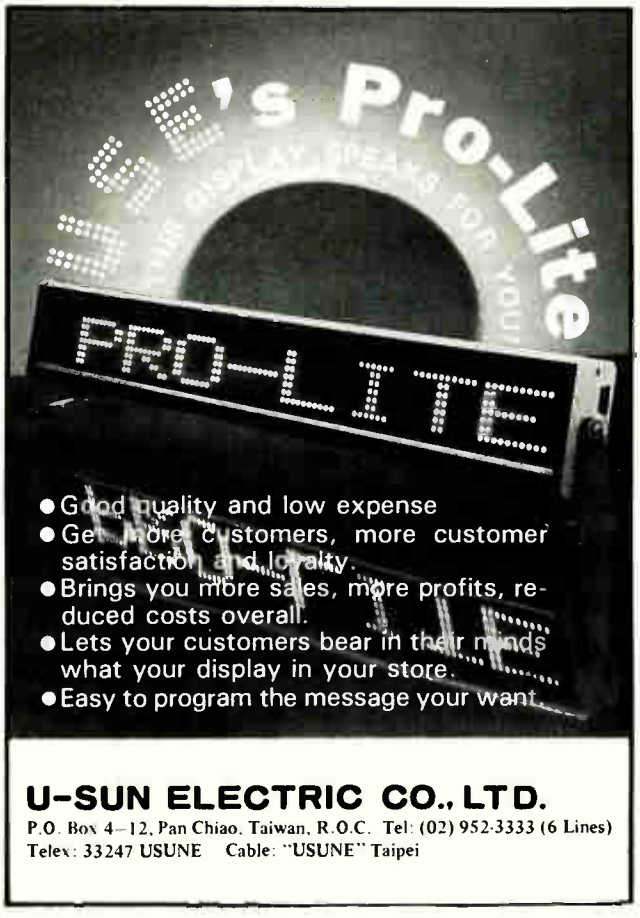
IBM's price cutting was "much more aggressive on the PC/XTs," McCarthy notes. "They don't mind the clones stealing the low end [of the PC market], but IBM is staking out ground in the hard-disk market."

Cuts on existing PC/XTs range from 5.5% to 25.7%. An XT with 256-K of internal memory and one 360-K floppy-disk drive fell to $2,145 from $2,270, and an XT with two floppy drives is now priced at $2,295, reduced from $2,570. The same configuration with a 10-Mb hard disk costs $2,895, compared with the old price of $3,895.

A PC AT with a 512-K internal memory, one 1.2-Mb floppy drive, and a 20-Mb drive now costs $4,895, down from $5,795. The same model with a 30-Mb drive sells for $5,295; it was $5,995.

IBM introduced three new XTs with either 256-K or 512-K of main memory and one or two half-height 5¼-in. 360-K drives, also with 20-Mb hard disks. The new prices: $2,145 for a single floppy; $2,295 for double floppies; $2,895 for a single floppy and a 20-Mb hard disk.

IBM also brought out a faster PC AT: 8 MHz, versus 6 MHz for the original. The AT now comes with a 30-Mb hard-disk drive and a 1.2-Mb disk drive, with a 512-K memory expandable up to 10.5 Mb. Its price is $5,295. *–R. J. K.*



Circle 45 on reader service card

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IS THE METROPOLITAN-AREA NET THE NEXT HOT TELECOM ITEM?

IEEE READIES A STANDARD TO LINK LANs VIA OPTICAL FIBER

by Tobias Naegele

NEW YORK

Another networking concept has suddenly popped to the surface. What's being called a metropolitan-area network, or MAN, is attracting the attention of a fast-growing number of users and vendors. Already developing hardware are such powerhouses as AT&T Co. and Burroughs Corp.

Born of the desire to link the burgeoning population of local-area networks, or LANs, that connect a single building or group of buildings, a metropolitan-area net would integrate voice, data, and even video signals in a single high-speed, private or semiprivate net over distances of up to 25 miles. Large corporations are investigating MANs because they figure they could save money by linking offices scattered over an urban, suburban, or even rural area, say industry observers, who predict a boom in MAN installations by 1990.

Not surprisingly, regional telephone companies are looking at ways they can implement MANs because they don't want to see their public nets bypassed by new independent carriers operating cheaper, shared metropolitan networks.

Most activity in MANs centers on a standard being devised by a task force of the Institute of Electrical and Electronics Engineers. IEEE 802.6 will use fiber-optic links for its high-speed backbone (see "How the new network would operate under the IEEE standard") and will transmit at three rates—about 11 Mb/s, 44.7 Mb/s, and between 200 and 250 Mb/s. But the 802.6 protocol will not be the only game in town for MANs. The IEEE standard will likely face challenges from technologies that rely on other means of transmission, such as cable-TV lines or coaxial cable.

The 802.6 standard will depend on the use of existing fiber-optic technology, says James Mollenauer, chairman of the 802.6 committee. "The telephone companies are installing fiber like it's going out of style. We're really trying to devise standards for systems that can build networks on top of the telephone company's networks." His task force expects to issue a MAN standard and protocol within a year. Last week, the IEEE sponsored its first workshop dedicated to MANs in St. Petersburg Beach, Fla.

Private nets could link corporate offices up to 25 miles apart

Of the three companies known to be designing parts for an 802.6 communications system—AT&T, Burroughs, and Tecmar—only Burroughs is willing to talk about its plans. Daniel Sze, the San Diego-based director of networks at Burroughs, says the Detroit company has designed and built 802.6 parts in silicon and the first 11-Mb/s media access chips "can be had today." He adds that he expects "to see first silicon of the 45-Mb/s parts in a few weeks."

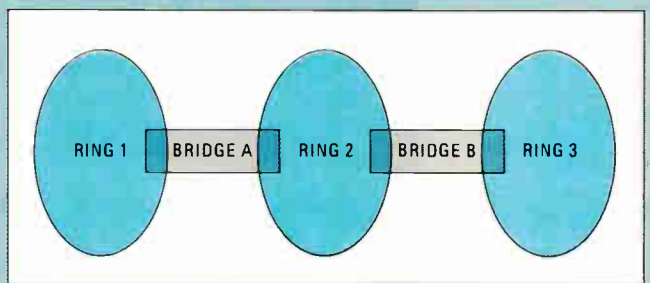
THE REAL THING. Such talk encourages Mollenauer, a senior technical staff member at Computervision Corp., Bedford, Mass. "Given that people are working on silicon prototypes, 1987 or 1988 installation and products aren't out of the question. This thing is real."

In fact, MAN is so real that some experts even believe that the more capable MANs could supersede the LANs. One MAN booster is Martin Alpert, president of Tecmar Inc., a Cleveland systems integrator and maker of microcomputer add-on boards. He notes that IBM Corp.'s Token-Ring Network, one of the latest and hottest LANs, "looks like it's out there all by itself. But the real story is that it's not," Alpert says. "Not only is there an alternative, but

HOW THE NEW NETWORK WOULD OPERATE UNDER THE IEEE STANDARD

The metropolitan area network set forth by the Institute of Electrical and Electronics Engineers' pending IEEE-802.6 standard would use the existing fiber-optic transmission lines of the regional telephone companies. It is built around a series of rings made up of multiple nodes that are linked serially, input to output, in a circular topology. In turn, these rings are connected by bridges that transfer data from one ring to another, both isochronously (that is, at equally spaced time intervals) and nonisochronously.

Each bridge has two isochronous address templates, one for each direction data can travel. The templates specify which channels on each ring are to be read from and which are to be written to. A pair of mapping functions specifies how channels from adjacent rings are to be connected. Bridges also have a pair of nonisochronous address templates—again, one for each direction.



CROSSING. Bridges transfer data isochronously or nonisochronously.

In the network diagram, three rings are connected by two bridges. Each bridge has individual address templates for each ring. Bridge A's individual address template for ring 1 contains the addresses of rings 2 and 3—all the rings reachable from ring 1 by means of bridge A. Likewise, bridge B's individual address template for ring 3 contains the addresses of rings 1 and 2.

However, bridge A's address template for ring 2 contains just one address, ring 1, because that is the only ring reachable over that bridge. Similarly, bridge B's template for ring 2 shows only ring 3's address. The network architecture as described in the IEEE standard will also permit the use of multiple bridges to connect two rings, which would increase the data rate between them. *–T. N.*

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it's a better alternative. MAN will win."

Sze backs Alpert up. "The token ring allows you to connect terminals and work stations," says Sze, who from 1978 to 1980 managed an IBM Corp. group in Zurich that helped develop the Token Ring Network. "What we're doing now takes the lessons we learned from the token ring to integrate voice, data, and media—real-time image transmission."

COMPUTER AS PERIPHERAL. Initial research into MANs appears to extend naturally from LANs, which themselves developed out of the computer field rather than the telecommunications sector. But "with MAN, what makes a difference is that communications will control computing," says Tecmar's Alpert. "The computer becomes the peripheral to the communications system."

However bright a future MANs may have, it's a mistake to think the 802.6 standard will be the only way to go, says Stephen Weinstein, division manager of network services research at Bell Communications Research, the research arm for the Bell operating companies. "There are a lot of things still being tried and still to be tried."

The BOCs are looking at piggyback alternatives, Weinstein says. These virtual private nets—including 802.6—can ride along on the public telephone network, he says, cutting costs by using available bandwidth rather than duplicating lines already installed. For example, one paper at last week's IEEE workshop reported on the operation of a coaxial-cable-based MAN that links computer systems at the Zurich universities. Another detailed the integration of data and voice onto a cable-TV network.

Bell's Weinstein sees a more limited role for MANs initially than its bigger boosters expect, as well as plenty of competition for the pending IEEE standard. "The interconnection of local-area networks for corporate customers is more or less the present function" being envisioned for MANs, he says, hinting that right now there may be little need to integrate digital voice and video into an asynchronous data network, making the 802.6 protocol less of a necessity.

For high-speed data applications, 802.6 faces competition from FDDI, the Fiber-Distributable Data Interface. This is another IEEE standard under development, which would provide 100-Mb/s data speed on the same fiber lines, but without the voice or video integration. Burroughs's Sze doesn't see it that way. "FDDI is designed to interconnect mainframes within the computer environment," he points out. MAN, on the other hand, "is intended to integrate a complete network. It is not a backplane for a computer system. We are talking about connecting personal computers, terminals, mainframes, and PBXs." □

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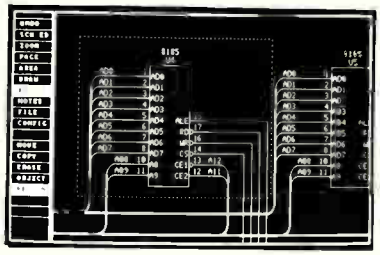

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SORD BEGINS TURNAROUND FIRMLY IN TOSHIBA FAMILY

ONCE KNOWN AS JAPAN'S APPLE COMPUTER, IT EXPECTS TO TURN A PROFIT IN 1986 AFTER A YEAR IT CALLS A 'TOTAL LOSS'

TOKYO

A year has passed since Toshiba Corp.'s 11th-hour rescue of the faltering Sord Computer Co., and the company's recovery seems well under way. Sord is not just surviving but should be profitable this year.

In its heyday, Sord was called the Apple Computer of Japan. The company's founder was a young entrepreneur with plenty of panache, whose innovative products quickly captured a chunk of his country's nascent personal computer market [*Electronics Week*, March 4, 1985, p. 32]. But Sord's success evaporated when larger computer makers started flexing their marketing muscles.

Sales stagnated and market share plummeted until Toshiba stepped in. In March 1985, the electronics giant bought 50.1% of Sord's shares. It has since added $19.6 million plus management and research personnel.

BACK ON ITS FEET. The company appears to be back on its feet financially, says Takayoshi Shiina, Sord's 42-year-old founder and president. Sales in 1986 should equal 1984's $104 million—a tad below the level of the glory days but far superior to 1985, which Shiina terms "a total loss." Moreover, the company is developing new products, with a greater emphasis on the software for which it is best known, and is forging joint development projects with Toshiba.

Most significant to some observers, Toshiba is encouraging the feisty spirit for which Sord is known—and which many feared would be snuffed out in the merger. When megalithic Japanese companies buy smaller ones, personal style is typically steamrollered in favor of a corporate ethic that some consider oppressive.

Fear that this would happen at Sord sent scores of engineers and managers running when the tie-up with Toshiba was announced. "People feared it would be like the military," Shiina recalls. But Toshiba quickly made known its intention to foster Sord's creativity.

SHIINA: Sord's founder says it should be profitable in 1986.

Still, there's no doubt that Sord is firmly in the Toshiba family. "Sord could now be described as a Toshiba subsidiary," says Jun Kobayashi, senior managing director in charge of overseeing the Sord operations at Toshiba. Even the independent-minded Shiina proclaims, "My idea now is a Toshiba idea. I don't have any complaints—I want to be a good Toshiba man."

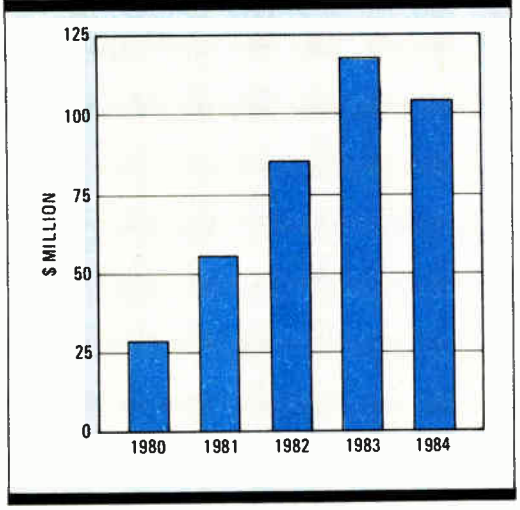
Working with Toshiba, Sord hopes to regain the luster of its youth. Founded in 1970, Sord by 1980 had achieved $27.4 million in sales for its line of desktop personal computers and peripherals, and it held an estimated 20% of the personal computer market in Japan. By 1983 sales had rocketed to $118.3 million, but market share had slipped to around 10%. The following year sales edged downward to $104.2 million, and while Sord hasn't yet released 1985 results, Shiina calls the year a washout, with market share dipping under 4%.

The major reason for Sord's decline, observers say, was the late-1970s entry into the personal computer market of Japan's multibillion dollar electronics giants: Hitachi, Fujitsu, and particularly NEC, which now dominates the personal computer market in Japan. When the market began to shift rapidly from lower- to high-end business machines, these companies "had the staff and resources to move rapidly into Sord's little-challenged niche market," says Peter Rawle, an analyst with W. I. Carr & Sons (Overseas) Ltd. in Tokyo.

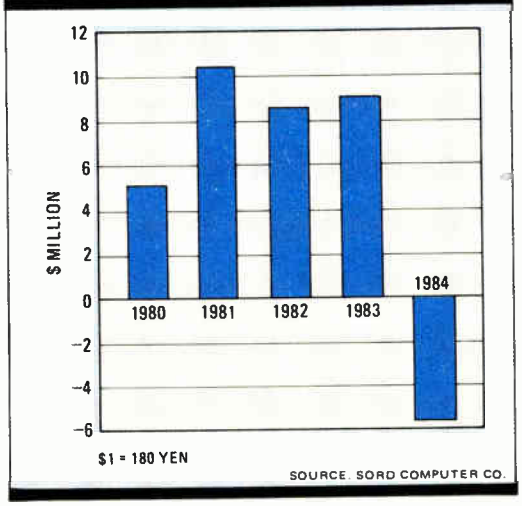
RISKY BUSINESS. Compounding those problems were several risky attempts to penetrate the U. S. and European markets with a small portable computer, attempts that Shiina admits were "not so successful."

The strong-willed Shiina was also partly to blame, observers believe. The very quality that made him a good entrepreneur became an obstacle when Sord needed some experienced managing. "I was so strong," he admits, "I didn't listen much" when the market started changing. "Instead, I was rushing to catch up." Such an experience is not unusual for small, independent companies, says Toshiba's Kobayashi. "When a venture business gets bigger than 300 people [Sord now has about 900 employees], people begin running around all confused. They need management."

WHY SORD NEEDED HELP: SALES FELL . . .



. . . AND INCOME DROPPED AS COMPETITION ROSE



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In return for its investment, Toshiba, whose computer line includes a family of IBM Corp. Personal Computer compatibles, got a company with some of the most highly praised software in Japan. "Sord's strength is its software," says Kobayashi, and he says this market sector will become increasingly important.

TOSHIBA'S KOBAYASHI: "Sord's strength is its software."

Software sales now account for 20% of Sord's business, says Shiina, and he aims to raise that to 40% during the next five years. Having just hired five Korean software writers, he will set up an office in Seoul in May and will begin operations there in October to write software for the Japanese market. He doesn't plan to keep all his software production in Korea, however, even though Korean wages are lower and Japan has a shortage of software writers. For now, the Korean's will be doing the laborious coding and debugging operations.

In February, Sord introduced its third-generation PIPS (for pan-information processing system) software package. Called Super PIPS, it is built on simple commands and Japanese word-processing and graphics capabilities. It also boasts a pull-down menu, windowing, multitasking, and index-sequential filing.

The program can run on top of the MS-DOS operating system and works with a third-party's software. "PIPS is making a real good stab at software," according to a Tokyo representative for a leading U.S. personal computer maker. "It offers something that you don't see a lot of around here—a productive and easy to use program."

In hardware, Kobayashi says Toshiba plans to concentrate on value-added systems such as work stations and powerful business personal computers, leaving most of its lower-end business personal computer production to Sord. Already, Sord makes Toshiba's Pasopia 1600, a low-end 16-bit office computer. Both companies will use the other's distribution networks. For the time being, however, at least 80% of Sord's output will carry the Sord brand name. But there is some development overlap. For example, they are working together on a multiuser work station running AT&T Co.'s Unix operating system.

And Sord, which has always been primarily a business personal computer maker, will aggressively expand its popular M68 MX 8-bit personal computer line. Later this year, it will unveil two new business computers, an Intel 80286-based 16-bit machine that runs MS-DOS and a Motorola 68020-based 32-bit personal computer that runs Unix. *–Jonathan Joseph*

BOTTOM LINES

AUTOMATION SPURS EXECUTIVE DEMAND

As U.S. companies increasingly automate their manufacturing operations, demand for executives with factory-automation experience is rising sharply, says Christian & Timbers Inc., a Cleveland executive search firm. "We've seen a 34% increase in demand over last year for managers who establish and run automated manufacturing facilities," says managing director Robert King. The top jobs are vice president of advanced manufacturing, vice president of engineering with automation experience, director of software development, and director of computer-integrated manufacturing, he says. "Most of the hiring is coming from large corporations that had never automated their factories before."

1986 JAPAN CAD/CAM MARKET: $1.5 BILLION

The Japanese market for computer-aided design and manufacturing equipment could reach $1.5 billion this year, an increase of 45% over the 1985 market, according to a new report from Eurogestion KK, a Tokyo consulting company. The report forecasts similar growth in 1987. "CAD/CAM systems are playing an important role in the new industrial revolution which is now taking place in Japan," it says. "They are becoming a must for manufacturing companies to survive their competition." The U.S.-made Cadam from Lockheed along with systems from Computervision and Calma are the top three sellers in Japan, but domestic vendors are mounting a campaign to catch up, the report notes. Hitachi, Mitsubishi Electric, NEC, and Univac Japan are among the domestic companies that have developed systems for the Japanese market, it adds.

CROWNTEK SELLS KAPTRON UNIT

Crowntek Inc., Toronto, has sold its wholly owned Kaptron Inc. subsidiary to a group of original Kaptron shareholders and key personnel. Crowntek, which acquired the Palo Alto, Calif., fiber-optics company in October 1983, says it has now shifted its business strategy toward software and services and is reducing participation in other areas. Kaptron produces fiber-optic communications interface components, fiber-optic test and alignment instruments, and passive and active fiber-optic subsystems. Crowntek will retain a 5% interest in Kaptron. It will receive a five-year interest-free note for an unspecified amount as well as royalties for seven years.

DU PONT BUYS PART OF IMAGING COMPANY

Du Pont Co., the chemical, energy, and specialty products manufacturer, has bought a 12% equity position in ImagiTex Inc., a Nashua, N.H., maker of electronic imaging systems. A Du Pont representative says the move will broaden the Wilmington, Del., company's role in the imaging-systems market, which accounted for about $1 billion of Du Pont's 1985 sales. Du Pont also has contracted with ImagiTex to develop a new black-and-white electronic scanner/recorder system for the worldwide graphic arts market. ImagiTex, which was founded in 1982, expects sales of about $12 million in 1986 and double that in 1987.

MICRO LINEAR ADDS $15 MILLION TO FUNDS

Micro Linear Corp., San Jose, Calif., has raised $15 million in its third round of venture financing. The company, which makes linear and combined linear/digital custom and semicustom integrated circuits, says this brings its total capitalization to $31 million. Micro Linear will use the funds as operating capital for product development and to expand its computer-aided design and manufacturing facilities.

CALIFORNIA MICROWAVE INVESTS IN ADVENT

California Microwave Inc., Sunnyvale, Calif., has bought a majority interest in Advent Communications Technology Inc., a San Jose, Calif., maker of telecommunications test equipment, for an undisclosed amount. Advent makes transmission and channel-access test sets and has annual revenues of about $1 million. California Microwave makes electronic communications equipment and systems for telephone companies.

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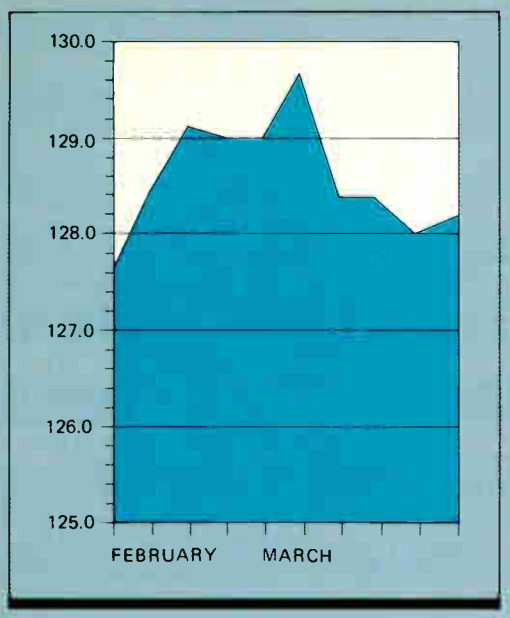
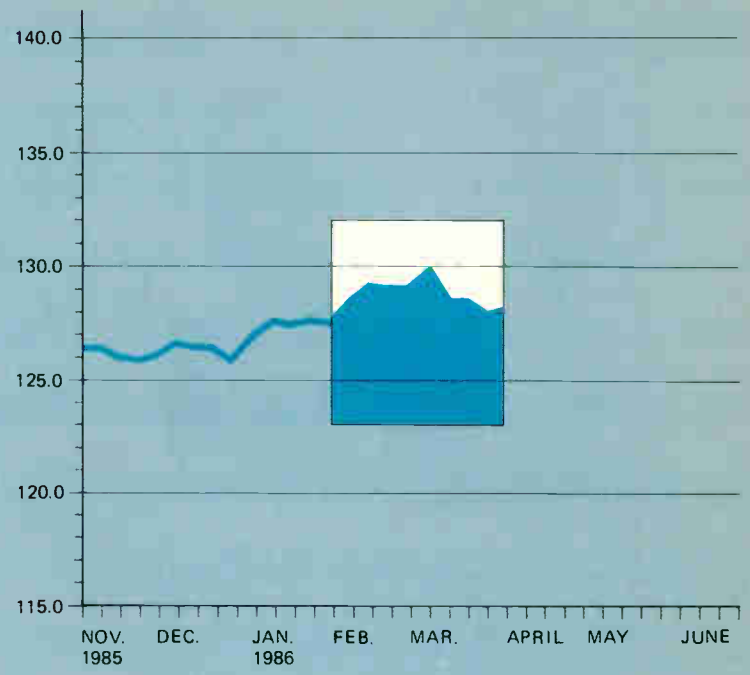
ELECTRONICS INDEX





THIS WEEK	= 128.2
LAST WEEK	= 128.0
YEAR AGO	= 128.0
1982	= 100.0

The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U. S. ELECTRONICS COMPONENT-PRODUCER PRICE INDEX (1967 = 100)

	February 1986	January 1986	February 1985
Digital bipolar integrated circuits	62.1	61.6	60.5
Digital MOS ICs	31.8	30.8	42.6
Linear ICs	57.9	57.1	60.4
Capacitors	185.3	185.8	191.8
Resistors	194.1	189.6	187.7
Relays	313.1	313.1	312.4
Connectors	237.0	237.0	232.9

Prices of a variety of U. S.-made electronic components edged upward by an average of 0.6% in February, led by digital MOS integrated circuits and resistors. This was the largest monthly price increase for components producers in more than a year.

Despite the slight 1.9% slip in U. S. components production in January, the price hike clearly signals stiffening demand for semiconductors and related parts. The overall surge in component prices helped push the *Electronics* Index higher than its year-ago level for the first time in more than a year.

Prices in February for relays and connectors, those mature mainstays of the component sector, stayed level with January. This put relays 0.2% and connectors 1.76% ahead of their February 1985 levels. Resistor prices, on the other hand, climbed a healthy 2.4% in February over January's figures, raising these products 3.4% above their level of a year ago.

Only capacitors dropped in price during the month, although the decline was modest. The 0.3% slide brought the cost of these components down 3.4% from the level reached in February 1985.

In most categories, integrated circuits recorded strong price gains in February. The best performers were MOS ICs, which bounded ahead 3.2% over the January 1986 level. Though this increase brought some measure of relief for their financially hard-pressed manufacturers, MOS IC prices remain a disheartening 25.4% below the February 1985 level.

The second-best performers in the integrated-circuit category were linear ICs, which increased 1.4% in February. Again, however, prices are 4.1% below those recorded for the year before.

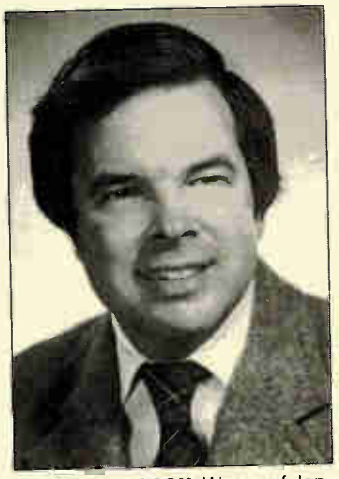
Manufacturers of digital bipolar ICs reported a rise of 0.8% in the latest month, bringing prices for the year up 2.6% from February 1985.

World Radio History

WILSON STILL SEES THREAT TO U.S. SUPERCOMPUTERS

ITHACA, N.Y.

Three years ago, Kenneth G. Wilson predicted that supercomputers would become a boom market. And he even suggested what to some was unthinkable—that one day "the U.S. may find itself building supercomputer systems around Japanese hardware." The Cornell University Nobel laureate's first prophecy has come to pass. Though the second has not, the Japanese are making progress (see story, p. 42). Three Japanese companies have orders for 35 machines and are now battling world market leader Cray Research Inc. as well as Control Data Corp. spin-off ETA Systems Inc. and a host of U.S. minisupercomputer makers. And the director of Cornell's Center for Theory and Simulation in Science and Engineering is already cautioning about the next phase of Japanese expertise.



KENNETH WILSON: Warns of Japanese supercomputer dominance.

At the time he made his observation, Wilson was among a vanguard of scientists calling for more federal aid for U.S. supercomputer research at a conference sponsored by government funding agencies. The impetus was expected Japanese competition in a burgeoning world market for the behemoth machines [*Electronics*, Sept. 8, 1983, p. 87].

Wilson says the issue now is the Japanese getting the expertise to use the machines to make their industries more competitive. "This is what I've been concerned about all along. Given the fact that the Japanese could acquire a technology that is comparable to ours—and as far as I can see, they have done that—do they make more effective use of supercomputers in their R&D efforts than we do in ours?"

Wilson is encouraged by stepped-up U.S. supercomputer funding since the 1983 conference. Most notable is a $200 million National Science Foundation grant to establish five national centers for research and development at U.S. universities, including Cornell [*Electronics Week*, March 4, 1985, p. 13]. The Cornell center is training graduate students in supercomputing techniques.

Wilson, who earned a doctorate in physics in 1961 from the California Institute of Technology, was named director of the new Cornell center following 23 years as a professor at the university. He won the Nobel Prize for physics in 1982 for his research involving special cases of phase transitions of matter.

NEXT PHASE. Wilson calls the NSF program "the most important response made to date" in making supercomputers available for use by U.S. universities and scientists. But he wonders about the next phase. "It isn't yet clear that the U.S. [funding agencies] will move fast enough to support the universities when we move to parallel computing," he says.

The possibility that Japanese manufacturers will come to dominate supercomputers is a legitimate concern, Wilson says, particularly in light of Japan's growing semiconductor expertise. He notes that in recent years the Japanese have been moving much faster than U.S. vendors. "The question is, will that continue? Will they be so much better than us five years from now that there will be no question?"

U.S. vendors are responding to the Japanese threat, the Cornell researcher notes. Cray has accelerated its product-development efforts over the past year or so, he says. "In the short term, it is clear that Cray has responded. And IBM is also responding in terms of the 3090 with vector boards. But the concern re-

PEOPLE ON THE MOVE

JOHN F. AKERS

☐ IBM Corp. has picked president and chief executive officer John F. Akers to take over the company's chairmanship when John Opel retires on June 1. Akers, 51, will be the first IBM executive to hold all three titles concurrently since Frank Cary in 1973. The 61-year-old Opel, who took over as chairman in 1983 and steered IBM through some of its most profitable years, will remain on IBM's board of directors. He will succeed Cary, a 38-year IBM veteran, as chairman of the board's executive committee.

CHARLES ASKANAS

☐ Lee Data Corp., the Minneapolis maker of IBM 3270-compatible systems, has appointed Charles Askanas as president and chief operating officer. Askanas joined Lee last December when the company acquired Datastream Communications Inc., a Santa Clara, Calif., manufacturer of protocol converters for display terminals and microcomputer-to-mainframe communications software. Askanas, who was Datastream's chairman and president, will report to John M. Lee, who retains the posts of chairman and chief executive officer.

KLAUS LUFT

☐ The board of directors of West Germany's Nixdorf Computer AG has appointed Klaus Luft to succeed Heinz Nixdorf as chief executive officer of the Paderborn company. Nixdorf died last week at the age of 61. Luft, at 44 a 19-year Nixdorf veteran, is a member of the company's board of managers. He is credited with having built Nixdorf's worldwide sales and service organization.

PETER G. PARASKOS

☐ Thorn EMI has made Peter G. Paraskos president and CEO of its major U.S. subsidiary, Systron Donner Corp., Concord, Calif. Mr. Paraskos moves from executive vice president, a position he has held only since January. Before that he was manager of Systron's Inertial Division.

RAYMOND C. RASK

☐ MultiComm Telecommunications Corp. has named Raymond C. Rask vice president of operations, engineering, customer service, and strategic planning. Rask, an award-winning researcher and a consultant to the satellite and data-communications industries, will also assume responsibility for the Arlington, Va., company's nationwide FM subcarrier information network and for development of its teleport near Washington. Most recently, Rask headed Telecommunications Transmission Systems, Salt Lake City, Utah. He had been director of satellite and corporate engineering for the Mutual Broadcasting System.

JAMES N. HUFFORD

☐ Atlantic Research Corp., Alexandria, Va., has promoted James N. Hufford to president and chief executive officer of its recently acquired subsidiary, Systematics General Corp., Sterling, Va. Hufford, one of the first employees to join Systematics General when it was founded in 1969, has been executive vice president since the mid-1970s.

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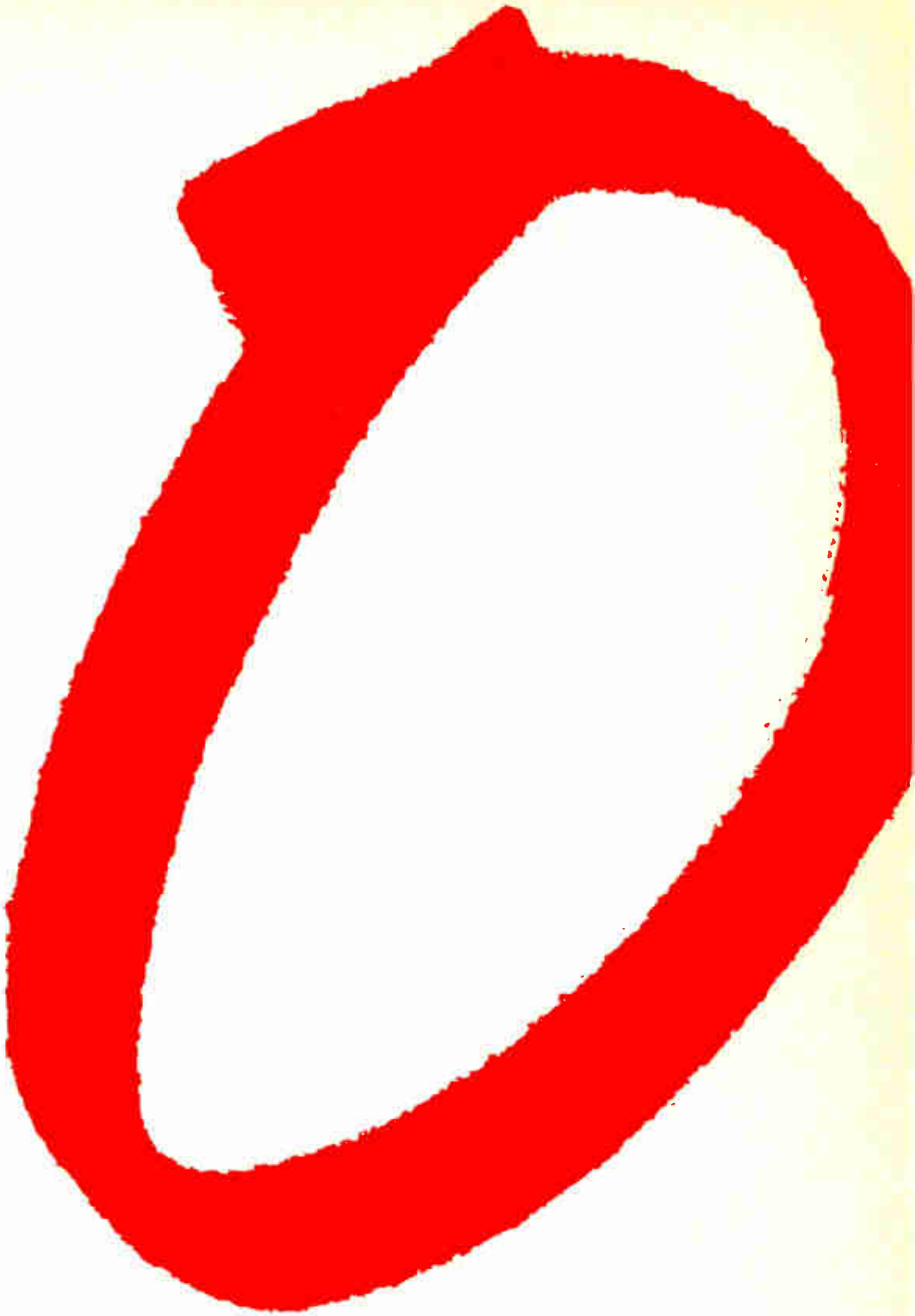

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PHILIPS

Electronic components and materials

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Some IC companies talk about defect standards of 500 ppm as if they were proud of them. At Philips, we have a different philosophy: one defect is one too many. So zero defects is the standard we've set for our ICs. And the warranty for that standard goes like this: when you receive IC components from Philips, if you find a single defect in that batch, we'll take them all back for re-screening or replacement. The reason we can offer this warranty is that after 100% testing, we sample every batch. If we find a single defect, that batch isn't delivered.

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It's a state of mind marked by a determination to prevent all defects. By working with you and examining rejects, we'll carry zero defects beyond a standard to a reality. You'll find that same commitment to quality throughout Philips. That applies whether we're designing a VLSI chip containing more than 100 000 transistors, meeting delivery schedules, double-checking the accuracy of our paperwork, or simply getting your name right when you telephone us.

So while many IC companies are bragging about a standard of 500 defects per million, the people at Philips are working their way towards zero. And when you put your trust in that kind of individual commitment, you can't lose.

To find out more about the ways in which the Philips IC Zero Defects Standard can help you, contact your nearest Philips National Organisation and ask for more information.

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Circle 53 on reader service card

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mains for the longer term."

Wilson believes that a lot depends on whether U.S. and Japanese supercomputer vendors provide an upgrade path from their low-end to their top-end machines. What industry needs is entry-level supercomputing power priced at about $50,000, with an upgrade path all the way up to $100 million systems, he says. This would let scientists and engineers at many more companies get into the race by using their annual budgets to upgrade their systems. Today's emerging crop of "Crayettes" or minisupercomputers generally don't cut the mustard, he says, because they don't provide the upgrade path.

It is not yet clear that either U.S. or Japanese supercomputer vendors will offer $50,000 to $100 million scalable systems, says Wilson. Further clouding the picture is the prospect of parallel computing.

"There is the possibility that we're beginning to make the switch from serial or vector computers to parallel supercomputers." That, Wilson observes, "may turn out to be a whole new ball game, for both us and the Japanese." *–Wesley R. Iversen*

VAN EYCK'S WANDERLUST: A CURE FOR APPLE JAPAN?

SELLING COAL IN NEWCASTLE. Van Eyck is the latest to try to build up a Japanese market for Apple Computer.

TOKYO

"I've got a bit of wanderlust in me," says Alexander (Sandy) van Eyck, explaining the rapid relocations his career has undergone in the past few months. Just after the New Year, he left his job as vice president in charge of Far East operations for MCI Corp., Ryebrook, N.Y. Three days later, he was being welcomed at the Cupertino, Calif., headquarters of Apple Computer Inc. And four days after that, he walked into his new office in Tokyo to take over as the president of Apple Computer Japan Inc.

Apple will likely present van Eyck with the biggest challenge of his career. The company has had little success so far in the Japanese personal computer market, despite an all-out effort [*ElectronicsWeek*, June 10, 1985, p. 34]. "The idea of going to Japan to build a company from virtually ground zero was irresistible," he says.

The move is not van Eyck's first overseas assignment. He first worked in Tokyo six years ago, representing Western Union International Inc. in its dealings with Kokusai Denshin Denwa, Japan's international carrier. After MCI took over Western Union International in 1982, he stayed with MCI until he made his jump to Apple. Van Eyck, 44, says he gets his wanderlust from his grandfather, a Dutch physician who lived much of his life in Indonesia and loved to tell stories of his experiences in the East Indies.

He became interested in Apple while he was browsing through a bookstore and noticed a book on the top-100 U.S. corporations. "Apple was one of the top rated. I bought the book and wrote them a letter," says van Eyck, who holds a degree in economics from Notre Dame University and a doctorate in law from Fordham University.

Though he will not reveal his market strategy, one of van Eyck's first moves is almost sure to be the development of products designed for the Japanese market. Engineering design applications, for instance, is a market niche with great growth potential.

GLOBAL SCALE. Van Eyck says a major reason he took the job was that Apple is "determined to play the computer game on a global scale. I intend to be a strong contributor to the Apple goal of building our international business to between 25% and 35% of total sales by 1990."

His immediate task is building confidence in his staff, which has seen two changes at the top within three years. "I want to give my staff and our customers the feeling that they're part of a long-term future."

That is why van Eyck has no idea of how long he'll be in Tokyo. "The happiest years of my career were spent here. I love living and working in Japan. I'm going to stay here until we're successful," he says. *–Michael Berger*

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NEW PRODUCTS

LOW-COST PHILIPS SCOPES GET HIGH-PRICED FEATURES

AUTOSET BUTTON AUTOMATICALLY SETS UP ALL PARAMETERS

Philips has been able to pack sophisticated features into its low-priced PM3050 family of 50-MHz general-purpose oscilloscopes, thanks to a major redesign effort that has greatly reduced manufacturing costs. Its single-time-base 3050 scope will sell for $1,245, and the dual-time-base 3055 will go for $1,345 in the U. S. Despite their modest price tags, the new scopes boast features usually found only on higher-priced instruments, says Hans Fjärem, product manager for oscilloscopes at the company's Industrial and Electroacoustic Systems Division.

A combination of a one-piece injection-molded plastic chassis with modular subsystems dramatically cuts the instruments' assembly time (see story, p. 39). Also contributing to lower production costs are a reduced components count, computerized testing during manufacturing, and highly automated pc-board production.

The closest competing scopes in the same general-purpose class are a pair from Tektronix Inc., the 2213 and 2215, both 60-MHz instruments. The 2213A single-time-base version sells for $1,275 and the 2215A dual-time-base scope is priced at $1,500. But the Tektronix scopes do not have intelligent features that the pair of Philips scopes offers.

SINGLE-CHIP. The 3050 family's most sophisticated feature is an autoset button, controlled by a single-chip microcomputer, which automatically sets up all the scope's parameters—amplitude, time-base, and triggering. Any signals applied to it instantly and clearly show up on the CRT's screen regardless of the signal's characteristics. This function does away with the time-consuming manual setting procedure usually needed to bring unknown signals into range, Fjärem explains.

When manual settings are needed, the 3050 family makes the job easier by replacing the traditional rotary knobs with rocker-switch controls for setting the amplitude, attenuator time base, and delay-time multiplier. The rocker switches also have a longer and more trouble-free lifetime compared to the bulky rotary controls, Philips says.

The array of function switches typical in conventional scope design is replaced by a few multiple-purpose softkeys. These keys are under the control of the microcomputer and permit the user to step through all functions sequentially. Software for the preset functions is contained in the microcomputer's 8-K ROM.

SMART SCOPES. The PM3050 family makes manual setup optional.

Because the rocker and pushbutton switches do not provide a visual confirmation of the settings as a rotary switch with a scale does, the scope includes an LCD panel to show status and settings continuously.

Philips has also incorporated a feature to give the user fast verification of correct operation. This is done by a built-in automatic checking routine in combination with a calibration signal. The checking routine encompasses a series of tests to execute all major scope functions. The on-screen displays indicate correct performance.

The 3050 and 3055 each weigh 16.5 lb and have sensitivity of 2 mV/division, with the highest value up to 10 V/division. Trigger bandwidth is up to 100 MHz.

The CRT's 16-kV acceleration voltage—rather than the 12 or 14 kV common for most other scopes—provides higher writing speeds, more light output, and good spot quality. Features such as high sensitivity, accurate stigmatic focusing, and beam centering, as well as improved deflection orthogonality combine to improve the CRT's performance.

The 3050 family offers an optional remote IEEE-488 bus control for all pushbutton functions. This is needed in system-oriented operation such as semiautomated production. The interface box will sell for around $500 in the U. S.

Philips will unveil the 3050 and 3055 scopes at this week's Industrial Fair in Hanover, West Germany. The oscilloscopes will be available for delivery from stock at the end of May. *–John Gosch*

Philips Test and Measuring Inc., 85 McKee Dr., Mahwah, N. J. 07430. Phone (201) 529-3800 [Circle reader service number 338]

Philips N. V., I&E Press Office, HKF, Eindhoven, the Netherlands [Circle 344]

ANALOG SCOPE STORES 700-ps EVENTS ON SCREEN

As digital storage oscilloscopes get faster, they start to compete for some applications that CRT scopes lay claim to. But no matter fast they get, they have limitations: they cannot capture an entire waveform, and they are too slow to capture the most elusive glitches. Tektronix's 7934, an analog CRT storage scope, overcomes these limitations by offering an extremely fast stored writing rate for capturing waveforms such as high-speed transients, low-repetition laser pulses, and random glitches in TTL, ECL, and CMOS.

The 7934 boasts a bandwidth of 500 MHz and a fast single-shot rise time of

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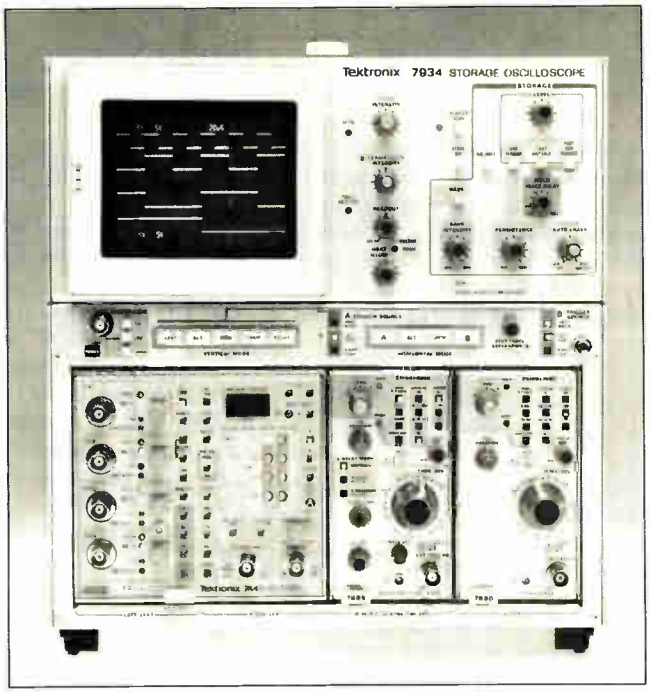
700 ps. The real speed, however, is in the 7934's 4-cm/ns stored writing rate, which allows 700-ps events to be stored on screen for direct viewing. According to Nellie W. Brock, marketing product line manager for the Laboratory Instruments Division, this storage capability is orders of magnitude greater than the fastest digital storage scopes and more than twice that of most specialized transient digitizers, which are typically used along with analog scopes.

"A digitizer would have to sample at a real-time rate of 1 GHz to even begin to compete in capturing transients, random events, or even high-speed low-repetition signals," Brock says. There is no 1-GHz digitizer on the market today. And a digital scope would need a 5-gigasample/s sampling rate.



FLAGSHIP. Tektronix Inc. tops its line of analog oscilloscopes with a 500-MHz model with a 700-ps single-shot rise time.

The 7934, which replaces the 400-MHz 7834 as the company's top-of-the-line scope, offers two types of storage: bistable and variable persistence. Bistable storage provides long viewing times; this allows time-lapse displays of changing events, suitable for checking pulse jitter or digital timing margins, for example. With bistable storage, the scope detects biases that digital scopes cannot. Bistable storage provides viewing times of up to 30 minutes.

Fast variable persistence with reduced sean captures fleeting events such as arcing or plasma discharge. A save mode lets users extend the viewing time up to 30 times. And a storage-level feature adjusts the writing rate, which is useful in suppressing storage of random noise on low-level signals, for example. Total waveform distortion is less than 5%.

The 7934 comes in a 500-MHz configuration for $20,355. This price includes the 7934 mainframe, a 7A29 vertical amplifier plug-in with a 500-MHz bandwidth, and a 7B92A dual time-base plug-in for 500-MHz triggering. Delivery takes four weeks. Also available for the two remaining slots is a selection of over 30 vertical-amplifier, time-base, digital, and special-purpose plug-ins.

The plug-ins let the scope take on special tasks. The 7A42 logic-triggered vertical amplifier and other digital delay units tailor the 7934 for digital system analysis. Likewise, a spectrum analyzer plug-in offers frequency-domain studies. *–Steve Zollo*

Tektronix Inc., Marketing Communications Dept., P. O. Box 1700, Beaverton, Ore., 97077. Phone (800) 547-1512; in Ore., (800) 452-1877 [Circle 339]

PROCESSOR MOVES COLORS FASTER

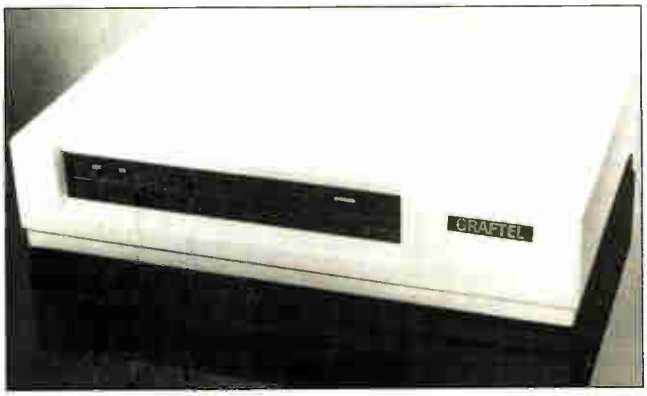
Today's printers are not fast enough for the new high-powered graphics terminals. When users want printouts, they must wait until the slower printers can accept all the data making up the image on the screen before they can use their terminals again. But Graftel Inc.'s latest color video processor transfers the entire display in as little as 2 s and then frees the terminal for other tasks.

"The VP 210 marks a quadruple improvement over our earlier product," says Jack Flynn, U. S. vice president for sales and marketing. The 60-MHz VP 210 can grab a page from the screen in 2 to 8 s, compared with the capture rate of 8 to 30 s on the VP 200. Minimum horizontal-line time is 18 μs, compared with the VP 200's 38 μs. With these capabilities, the VP 210 can handle color terminals that were too fast for the VP 200, such as Silicon Graphics' Iris series, the Lexidata 2410, and Apollo Computer's DN550 and DN660 work stations, according to Flynn. The company has also added two more sampling thresholds—the values used to differentiate among colors—to bring up the number of colors supported from 8 to 64.

NO DRIVERS. The VP 210 accepts red-green-blue input directly from the terminal, eliminating the need for software drivers. "Companies that make output devices were telling us they were losing business because they couldn't offer graphics to match high-end terminals," says Flynn. "So now we can write a driver in firmware for their peripheral equipment that will bring them up to par." Peripherals supported by the VP 210 subsystem include thermal-transfer, ink-jet, or electrostatic printers and plotters.

After acquiring the color-graphics page data, the VP 210 stores it in a 1- or 2-megabyte buffer, then commands the printer to produce the color hard copy. "The large buffer space is essential to high-resolution graphics—a 1,024-by-1,024-pixel image needs a full megabyte of buffering," Flynn says. The VP 210 handles screen resolutions up to 1,280 by 1,024 pixels.

The VP-210 requires a simple one-time menu-driven setup procedure to match the terminal or personal computer, the VP 210 accepts images from the terminal and produces output to the printer merely by pressing the "print" button. Two switches provide a double-



FASTER STILL. Graftel's new graphics processor keeps pace with such fast graphics systems as Silicon Graphics' Iris 3000.

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size printout and a repeat-printer mode, respectively.

Besides the VP 200 and the VP 210 color video processors, Graftel manufactures a buffered multiplexer that lets up to four personal computers or terminals share two printers or plotters.

The VP 210 graphics processor sells for $2,995 for the model with a 1-megabyte buffer and $3,495 for the 2-megabyte version. Both models include firmware for the selected output printer or plotter. Units are available now for immediate delivery. *–Ann Jacobs*

Graftel Inc., 400 Executive Blvd., Elmsford, N. Y. 10523.
Phone (914) 592-3700 [Circle 341]

200-MHz ECL MULTIPLIER DISSIPATES ONLY 2.9 W

With a clocked multiply time of 5 ns, Bipolar Integrated Technology's B3018 16-by-16-bit integer multiplier is five times faster than its nearest bipolar competitor. And it dissipates only 2.9 W, about half that of the competition.

The company credits the B3018's performance to its BIT1 bipolar very large-scale-integration process (see story, p. 35), which is capable of 200-MHz input clock rates. With polysilicon self-aligning techniques similar to those used in MOS fabrication, BIT1 achieves densities comparable to 2-μm CMOS. It is also the lowest-power ECL process, offering a tenfold power-delay improvement over traditional ECL processes.

BUILDING BLOCKS. The multiplier is targeted at applications in which speed is crucial. "By providing computational building blocks that are fast, small, and low in power, we can help designers maximize the speed and density of a wide range of digital-signal-processing and data-processing applications," says president George Wilson. Applications include finite- and infinite-impulse-response filters, fast Fourier transforms, and image processing and graphics.

The B3018's bipolar competition includes TRW Inc.'s video-speed MPY016K, which has a 40-ns multiply time with a whopping 4.6-W power dissipation, and Advanced Micro Devices Inc.'s AM29516, which comes in two speed-power versions—a 38-ns part with a 4-W power dissipation and a slower 90-ns part with a lower 2-W dissipation.

The B3018 has a full 32-bit product output port, and it supports the unsigned 2's complement and mixed-mode operands. The full 32-bit result is available in parallel or as separately enabled 16-bit least- and most-significant portions. Separate negative sign, overflow, and zero-status flags are provided.

The minimum mask feature size is 2 μm, and typical gate propagation delay is 300 ps. Individual-gate power dissipation is 0.3 mW.

The B3018 multiplier will be available in June at $260 each. The company also plans to introduce a TTL version at $205 each. *–Steve Zollo*

Bipolar Integrated Technology Inc., 1050 N. W. Compton Dr., Beaverton, Ore., 97006. Phone (503) 629-5490 [Circle 342]

FIELD-PROGRAMMABLE ARRAYS RUN 40% FASTER

Fairchild Semiconductor is using its tried-and-true bipolar process and vertical-fuse technology to create a family of field-programmable logic arrays. The first members in the Fastpla family are 15-ns parts, the 16P8B, 16RP8B, 16RP6B, and 16RP4B, which are compatible with industry-standard versions (16L8, 16R8, 16R6, and 16R4) from Monolithic Memories Inc. and others.

About 40% faster than standard bipolar parts, Fastplas incorporate synchronous D-type registers at the output of the fixed-OR array. They feature programmable output polarity, power-up reset, and power-up three-state outputs. Designed for full ac and dc testing, they are manufactured with the Fairchild Advanced Schottky TTL (FAST) process and the company's highly reliable isoplanar-Z vertical-fuse technology.

Initially, all vertical fuse cells are unprogrammed. The unprogrammed output-polarity fuses are equivalent to low-impedance connections from the exclusive-OR gate to ground. Therefore all outputs are initially active low. Once the polarity fuse is programmed, the output is permanently active high.

At power on, outputs remain in the high-impedance state until dc power-supply conditions are met, after which they are controlled by dedicated programmable enable product terms. For testability, a register-preload feature is provided, allowing the user to individually preset the registers to either a high or low level through the use of an 11-V control signal. This allows all states of a sequential design to be tested.

The 16P8B is organized with 10 dedicated inputs, two dedicated outputs, and six bidirectional I/O pins. By using the programmable polarity feature, a circuit designed with the 16P8B can be configured as either a 16L8 or 16H8. The output polarity also can be individually programmed. Each output buffer is enabled by a dedicated active-high product term.

The 16RP4 and 16RP6 both have combinatorial output cells with feedback and programmable output enable and sequential-output cells with register feedback and dedicated output enable. The 16RP8 has eight sequential-output cells with register feedback and dedicated output enable.

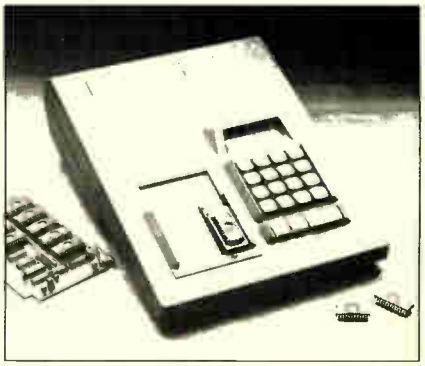
Available now in sample quantities, the 20-pin Fastplas cost $5.49 each in lots of 100. Production quantities are expected to be available late in the second quarter. *–Bernard C. Cole*

Fairchild Semiconductor Corp., Memory and High-Speed Logic Division, P. O. Box 5000, M/S 2C17, Puyallup, Wash., 98373.
Phone (206) 841-6646 [Circle 343]

PROM PROGRAMMER SELLS FOR $1,150

The model 201 programmer from Data I/O offers customers who are programming small numbers of ROMs a moderately priced, single-socket, entry-level unit. The $1,150 price tag includes support for more than 140 devices, including MOS and CMOS EPROMs and EEPROMs. The company says its market is manufacturers doing preproduction prototyping or small production runs.

The 201 contains algorithms that can be upgraded by the user, an RS-232-C interface, full editing capability, and a scrolling menu. The unit performs con-



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tinuous automatic calibrations to preserve the integrity of the waveforms that reach the programming socket.

Lead time from receipt of order to delivery is eight weeks.

Data I/O Corp., 10525 Willows Rd. N. E., P. O. Box 97046, Redmond, Wash. 98073. Phone (800) 426-1045; in Washington State, (206) 881-6444 [Circle 366]

SPECTRUM ANALYZER FINDS HIDDEN BUGS

For installing and servicing systems as well as locating hidden eavesdropping transmitters, the PSA-35 portable spectrum analyzer covers frequencies from 10 to 1,500 MHz and 3.7 to 4.2 GHz.

The instrument checks signal strength, in-band attenuations, filter alignment, and cable loss; the company calls it very portable and easy to use in the field. Priced at $1,965, the PSA-35 is available now.

Avcom of Virginia Inc., 500 Southlake Blvd., Richmond, Va. 23236. Phone (804) 794-2500 [Circle 367]

LOGIC DEVICES ARE MASK-PROGRAMMED

A family of 17 CMOS mask-programmable logic circuits offers a peak propagation delay of 35 ns and consumes 100 μA maximum in standby mode, or 3 mA/MHz in active mode. The ZHAL 20 circuits are hard array logic devices—similar to programmable logic arrays—that are metal-mask-programmed at the factory rather than in the field. The result is a cost break in volume production. Available for commercial, industrial, and military temperature ranges, the circuits can be used in portable computers and in battery-backed systems that need zero standby power.

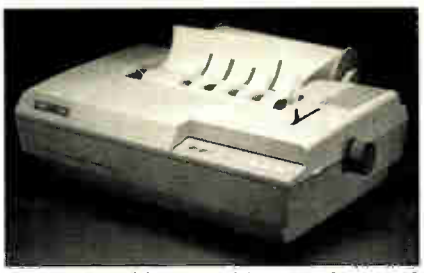
Lead time for production is four weeks. Volume-quantity pricing is $2.10 each for the ZHAL circuits, and there is a one-time charge of $5,000 for mask generation.

Monolithic Memories Inc., 2175 Mission College Blvd., Santa Clara, Calif. 95054. Phone (408) 970-9700 [Circle 359]

INK-JET PRINTER RUNS GRAPHICS AND TEXT

The model 4020 ink-jet printer integrates text and color graphics on one page for such business-graphics applications as prints, transparencies, charts, and diagrams. In addition, for users of work stations based on personal computers, the printer produces quick check plots and hard copies.

The 4020 works in two switch- or soft-



ware-selectable graphics modes and prints up to seven colors and more than 4,000 shades. It takes four minutes to print a page in near-letter-quality mode (240 by 120 dots/in.), and it will integrate text on the same line as graphics.

The 4020 features a Centronics parallel interface, and an RS-232-C serial interface is optional. Units will be available in April, at $1,495, and a supplies starter kit is priced at $170.

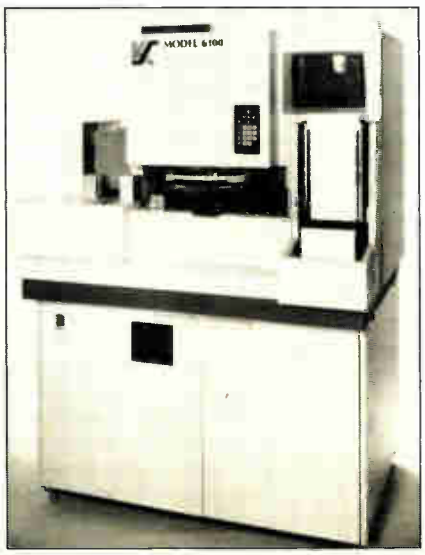
Xerox Corp., Printing Systems Division, 101 Continental Blvd., El Segundo, Calif. 90245. [Circle 369]

EPOXY DIE BONDER HANDLES 8-IN. WAFERS

The inverted-die presentation system of the model 6100 automatic epoxy die bonder eliminates stretching as 8-in. wafers pass through the system. An automatic die-selection and -inspection system reduces the need for wafer mapping and verifies each die before pick-up and bonding. Other features include high-speed bonding, front-access material handling, and a color monitor.

The model 6100 also incorporates the manufacturer's proprietary Semiconductor Assembly Management System, a communication interface. Pricing and delivery information were unavailable at press time.

Kulicke & Soffa Industries Inc., 507 Prudential Rd., Horsham, Pa. 19044. Phone (215) 674-2800 [Circle 375]



SYSTEM SOLDERS BOTH BOARD SIDES AT ONCE

A soldering system, model SPS, attaches all types of surface-mounted and through-hole components on both sides of the board at one pass. The 15-ft conveyor carries successive boards over a dual solder wave and then over a heated debridging air knife—a patent of the manufacturer—that clears the bridges so effectively that solder drainage is not necessary. This means that the SPS conveyor can be oriented horizontally rather than at an angle, which makes for more efficient throughput, the company says.

The efficient arrangement of air knives also means greater throughput, and the heat is evenly distributed, with no laminate scorching. The single-unit machine is slightly longer but otherwise the same size as a conventional wave-soldering unit, the company says.

Configuration and installation will determine price and shipping time.

Hollis Automation Inc., 15 Charron Ave., Nashua, N. H. 03060. Phone (603) 889-1121 [Circle 374]

PC CAD SYSTEM WORKS WITH VAX

A computer-aided-design and -engineering system, ESP/C, lets the designer of application-specific ICs create circuits on an IBM Corp. Personal Computer AT, then upload them to a Digital Equipment Corp. MicroVAX II for final batch assembly and analysis. It does this with the Opus532 Personal Mainframe, a Unix-based coprocessor that converts the PC AT to a VAX-like work station.

ESP/C performs schematic capture, logic simulation and testing, layout design and editing, interactive design-rule checking, and electrical rule checking.

Scheduled to become available in June, ESP/C will sell for $25,000 for the first station, which will include the software and Opus532. Hardware requirements include the PC AT, an IBM Professional Graphics Monitor, and IBM Professional Graphics Controller.

Factron Electronic Design Automation, 269 Mt. Hermon Rd., Scotts Valley, Calif. 95066. Phone (408) 438-2880 [Circle 350]

SOFTWARE LAYS OUT VARIABLE SHAPED ICs

MacroEdge is a design system for placement and automatic routing of ICs that consist of standard cells of varying shapes. The company says it greatly reduces design time over laying out circuits geometry by geometry. It auto-

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matically interconnects cells that have been designed for certain functions or are contained in a cell library.

Included in MacroEdge are tools for library management, floor planning, automatic assisted macrocell placement, routing-channel generation, and layout verification. An upgrade to a combined standard- and macrocell product is available, and several features for mixed analog and digital physical design are provided.

Prices for the software package begin at $60,000 and at $113,000 for turnkey systems.

SDA Systems, 2461 Mission College Blvd., Santa Clara, Calif. 95054.
Phone (408) 727-7811 [Circle 351]

PC AT CAN DESIGN GATE ARRAYS

A complete computer-aided engineering service uses a system based on the IBM Corp. Personal Computer AT and a library of semicustom digital arrays to provide standard-cell flexibility with gate-array-like pricing.

The system is tightly coupled to the cell library, called optimized gate arrays, and the base arrays. Symbolic layout is done at the cell level, with predefined cells and interconnection grids; postlayout extraction of electrical parameters ensures accurate postlayout timing analysis.

The two-level-metal CMOS digital arrays are called optimized gate arrays because the designer uses a standard-cell procedure to optimize the die size. Then the rows of cells are automatically completed to transform the base layers of the circuit into a new gate-array base. This lets the designer modify the circuits or update them at the lower gate-array cost.

Design starts are available now, and prices are based on configuration. There is no charge for the CAE software.

Intercept Microelectronics, 2890 Zanker Rd., San Jose, Calif. 95134.
Phone (408) 434-7070 [Circle 353]

IMAGE PROCESSOR TARGETS INSPECTION

The PIP-4000 image processor monitors a variety of digitized functions in real time. Its applications lie in high-speed machine-vision inspection systems, computer-integrated manufacturing, medical imaging, and other automated monitoring systems.

The image processor can handle as many as eight video cameras simultaneously and has up to 32 frames of image memory, depending on configuration. Each frame handles up to 512 by 512 by 8 bits.

Specialized software packages include moiré edge enhancement and particle-distribution measurement and analysis. A total of 48 commands are built into firmware governing data entry, storage, display, and transfer.

The 37-lb unit offers such hardware options as array processors and color operation. Pricing and delivery information were unavailable at press time.

A. D. S. Imaging Systems, 467 Hamilton Ave., Palo Alto, Calif. 94301.
Phone (415) 322-8450 [Circle 354]

SOFTWARE FITS PC AT GRAPHICS CARDS

Image-Pro 1000 software is designed for use with 1,024-by-1,024-pixel graphics boards. It provides a gray scale with 256 gradations for the IBM Corp. Personal Computer AT. It performs spatial filtering, edge detection, contrast enhancement, and image averaging.

Image-Pro 1000 accepts lower-resolution images from other Image-Pro systems. Its library can be called from Lattice C and the Microsoft languages. The Halo-vision image editor, which is included in Image-Pro 1000, supports text annotation and graphics overlay and is icon-driven. The price of Image-Pro 1000 is $2,000, and a complete image-processing subsystem including camera, optics, and display for the PC AT sells for $14,500. It is available now.

Media Cybernetics Inc., 8484 Georgia Ave., Suite 200, Silver Spring, Md. 20910.
Phone (301) 495-3305 [Circle 355]

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MEETINGS

GRAPHICS SHOW TO EYE INDUSTRIAL AUTOMATION

The major focus at Computer Graphics '86 will be on streamlining production processes. Sessions covering industrial automation are more than double last year's total, says Ronald E. Ball, conference director. Twenty-eight of this year's 92 sessions will cover such topics as computer-aided design, manufacturing, and engineering, and computer-integrated manufacturing, says Ball, advertising director for California Computer Products Inc. of Anaheim, Calif.

Carl Machover, president of Machover Associates, a computer-graphics consulting company in White Plains, N. Y., will chair two industrial automation sessions. The first, on CAD and CAE, will present "a lot of applications stuff, with a fair amount of concentration in the personal computer area," he says. Topics will include automatic data capture, CAD/CAE for very large-scale integration, expert systems, and the use of film recorders.

The second session will focus on new hardware, including display devices and processors, a laser color printer, optical storage devices, recent developments in film from Eastman Kodak Co., and voice systems. Machover spots two trends developing: the cost-effectiveness of voice input and output for graphics devices, and optical storage becoming "increasingly important in the CAD environment."

Also covering industrial automation are sessions on CAM/CIM, future software directions, and recent developments in the Manufacturing Automation Protocol and the Technical and Office Protocol.

The conference, to run May 11-15, also has sessions on artificial intelligence, pattern recognition, and video technology.

1986 SID International Symposium, Society for Information Display (Mark Goldfarb, Palisades Institute for Research Services Inc., 201 Varick St., New York, N. Y. 10014), Town & Country Hotel, San Diego, May 6-8.

Videotex 86, Online International Inc. (Cynthia Parsons, Online International, 989 Avenue of the Americas, New York, N. Y. 10018), Infomart, Dallas, May 6-8.

NTT International Symposium, Nippon Telegraph & Telephone Corp. (Ruder Finn & Rotman Inc., 110 E. 59th St., New York, N. Y., 10022), Keidanren Kaikan, Tokyo, May 7-8.

Computer Graphics '86, National Computer Graphics Association (2722 Merrilee Dr., Suite 200, Fairfax, Va. 22031), Anaheim Convention Center, Anaheim, Calif., May 11-15.

Comdex/Europe '86, The Interface Group Inc. (300 First Ave., Needham, Mass. 02194), RAI Congress & Exhibition Centre, Amsterdam, the Netherlands, May 12-14.

1986 Microwave Power Tube Conference, IEEE *et al.* (David Zavadil, Northrop Corp., 600 Hicks Rd., Rolling Meadows, Ill. 60008), Naval Postgraduate School, Monterey, Calif., May 12-14.

CICC: Custom Integrated Circuits Conference, IEEE (Tom Foxall, Pacific Microcircuits Ltd., 240 H St., Blaine, Wash. 98230), Riverside Convention Center, Rochester, N. Y., May 12-15.

ITCA 3rd Meeting, International Teleconferencing Association (ITCA, 1299 Woodside Dr., Suite 101, McLean, Va. 22102), Concourse Hotel, Madison, Wis., May 12-16.

7th International Conference on Digital Satellite Communications, Deutsche Bundespost and Intelsat (Horst Heyder, VDE-Zentralstelle Tagungen, Stresemannallee 15, 6000 Frankfurt am Main 70, West Germany), Hilton International München, Munich, May 12-16.

PC Fab Expo, PMS Industries (1790 Hembree Rd., Alpharetta, Ga. 30201), Radisson South, Minneapolis, May 13.

Computer Standards Conference 1986, IEEE (Computer Society, 1730 Massachusetts Ave., N. W., Washington, D. C. 20036-1903), Sheraton Palace Hotel, San Francisco, May 13-15.

Electro/86, Mini/Micro Northeast, IEEE and Electronic Representatives Association (Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045), Bayside Exposition Center and World Trade Center, Boston, May 13-15.

Opto 86: 6th European Optoelectronics Conference, ESI Publications (General Secretariat, ESI Publications, 12, rue de Seine, 75006 Paris, France), Palais des Congrès, Paris, May 13-15.

CAT '86: Computer Aided Technologies in Manufacturing, World Computer Graphics Association Inc. (2033 M St., N. W., Suite 399, Washington, D. C. 20036), Conference Center, Stuttgart, West Germany, May 13-16.

INFO Show: Information Management Exposition & Conference, Cahners Exposition Group (999 Summer Street, Stamford, Conn. 06905), Los Angeles Convention Center, Los Angeles, May 14-16.

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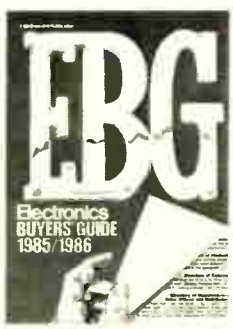

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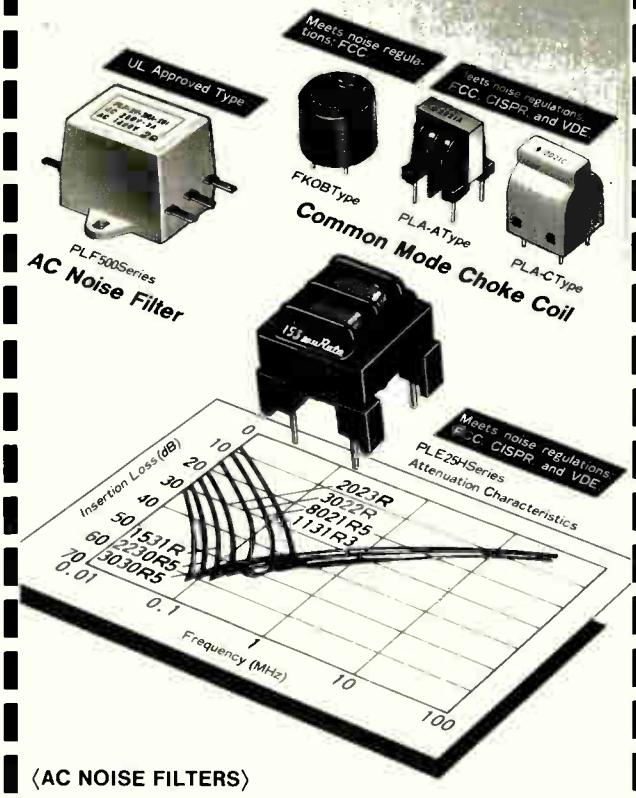

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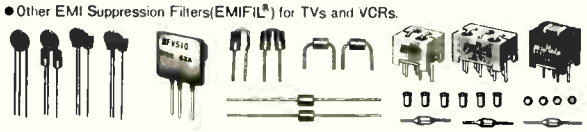

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ELECTRONICS WEEK

SLOW GROWTH SEEN FOR U. S. MARKET

A study published in the UK last week sees the growth rate of the U. S. electronics markets lagging behind those of their European and Japanese counterparts between now and the end of the decade. Figures highlighted in the *Yearbook of International Electronics Data*, published by Benn Publishing Co. in Luton, indicate that the average annual growth rate through 1990 will be no more than 5.2% in the U. S. The European and Japanese markets should expand at annual rates of 6.2% and 6.5%, respectively.

THOMSON CUTS ITS WORK FORCE

Aiming to increase its own competitiveness in the face of growing Japanese competition, Thomson SA, the nationalized French electronics conglomerate, plans to decrease the 8,500-person workforce of its European color-TV-set operations by more than 25%. The cuts will hit 920 workers in West Germany, 380 in France, and 200 in Spain. The move is part of an overall plan to restructure Thomson's consumer electronics activity, which lost some $30 million last year.

BUDGET AX THREATENS EOSAT

The Earth Observation Satellite Co. (Eosat), created last year to take over operation of the federal government's Landsat satellite program, is falling victim to federal budget constraints. The Lanham, Md., company was informed in late March that the administration had cut its $87 million government payment from the fiscal 1987 budget. Eosat was scheduled to receive a total of $250 million from the government to develop and launch two new satellites and build a new headquarters and data-processing building. It received $125 million last year, and Eosat officials remain optimistic that Congress will restore the fiscal 1987 funds, along with another $20 million to $30 million due in fiscal 1988.

IBM JAPAN POSTS IMPRESSIVE GAINS

Thanks mainly to increased sales of the new 3090 system and medium-sized System/38 and 36 computer families, IBM Japan Ltd. has announced a substantial increase in sales and profits for 1985. Total earned gross revenue was $5.08 billion last year, 19% more than 1984. Net income was $405.5 million, an impressive 33.7% increase.

WHITE-COLLAR JOBS INCREASE

In a reversal of last year's trends, demand for high-technology white-collar talent will grow faster than the general economy, according to a survey by Christian & Timbers Inc. The executive search company in Boxborough, Mass., predicts executive demand in 1986 will be 5.2% over 1985 levels; it notes that most forecasts for growth in gross national product during the same period range from 3.2% to 3.8%. Last year, high tech lagged behind the general economy: demand for white-collar workers increased 1.23% over 1984 while the GNP grew 4%. The largest gains in executive demand this year are expected to be in the software, automation, and systems and services sectors.

UTC MAY SELL BUS-BOARD UNIT

United Technologies Corp. is holding acquisition talks with several companies it won't identify that are interested in buying the computer-board division it spun out of Mostek Corp. last summer. The Digital Systems unit, which makes VMEbus and STD bus boards, was originally part of Mostek in Carrollton, Texas. United Technologies transferred the business to its Hamilton Standard subsidiary, Windsor Locks, Conn., before selling Mostek to Thomson-CSF of France last fall. In response to lagging sales, the unit recently laid off 37 employees, bringing the payroll to 213. United Technologies intends to trim that further, to about 200.

FAIRCHILD BUYS INTO DAC STARTUP

Fairchild Semiconductor Corp. has purchased a 5% interest in Brooktree Corp., a San Diego startup specializing in advanced digital-to-analog and analog-to-digital converters. Fairchild paid $3.6 million for rights to second-source Brooktree's innovative DACs, which are being designed into computer graphics, imaging, and telecommunications and test equipment. The partnership agreement gives Brooktree a six-month head start on product sales and access to Fairchild's advanced emitter-coupled-logic and CMOS fabrication lines.

IBM FINDS DENSER STORAGE MEDIA

Scientists at IBM Corp.'s Almaden Research Center, San Jose, Calif., have identified a new group of materials that could be an important step toward developing an experimental, high-density data-storage technique. The technique, called frequency domain optical storage, uses thousands of laser colors, or frequencies, to record computer data by selectively exciting and bleaching groups of molecules. It has the potential, says IBM, to store up to 100 billion characters per square inch—the highest ever achieved. The materials, which allow data to be recorded, read, and erased, consist of inorganic rare earth ions in an alkaline fluoride crystal along with organic material of carbazole molecules in a boric acid glass matrix.

GE GETS BIG DOD SOFTWARE AWARD

In an effort to reduce future software costs by making Department of Defense programmers more productive and software products easier to maintain, the U. S. Air Force has awarded General Electric Co., Schenectady, N. Y., a three-year, $2.6 million contract. The goal is to shorten by at least a factor of 10 the time required to write programs in Ada, the standard language for the Defense Department's embedded computers (those built into various systems). The development project is the largest ever by the funding agency, the Air Force's Avionics Laboratory at Wright-Patterson AF Base in Dayton, Ohio.

GCA SELLS GROUP, LOSES DIRECTORS

Struggling GCA Corp. of Bedford, Mass., has sold its Chicago-based Instruments and Equipment Group to American Sterilizer Co. of Erie, Pa. The unit, which manufactures laboratory equipment, has had annual sales of about $30 million. Its sale raises money for cash-hungry GCA, which is suffering large losses in its primary wafer-fabrication equipment business. The glimmer of good news was tempered by the resignations of four of the six board members, including GCA's founder, prompted by the expiration of the company's liability insurance for board members. Richard Riffenburgh, chairman, president, and chief executive officer, has appointed two new board members to bring the total membership up to four.

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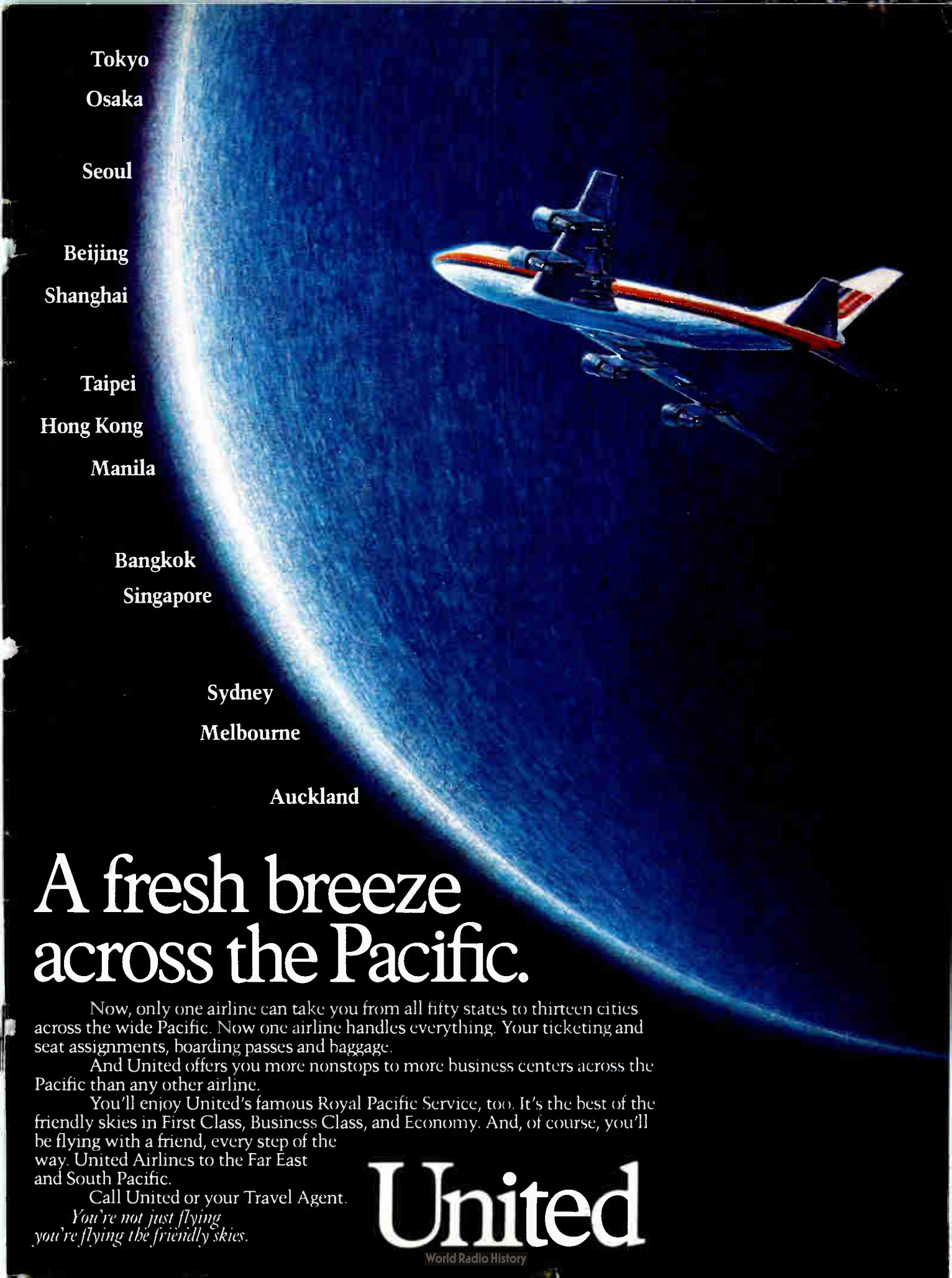

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Toshiba's newest LCD modules give you 640 × 200 dot displays in a choice of two viewing sizes. One is approximately the size of a magazine, and the other about half that size.

Both sizes put an enormous amount of information on view . . . an array of 80 characters × 25 lines. But still bulk and power consumption are at a minimum. Battery powered, these slim modules interface with various systems through LCD controller without renewing software.

Toshiba's advanced technology has also eliminated surface reflection and developed a sharper contrast which gives a brighter and easier to read viewing screen. And for low light or dark viewing an optional backlightable LCD is available.

These versatile LCDs are ideally suited for applications as displays for personal computers, POS terminals, portable word processors and other display terminals. You can also look to Toshiba with confidence for a wide range of sizes and display capacity to suit your LCD requirements.

TLC-363 *TLC-402*

Specifications

		TLC-402	TLC-363B
Display			
Number of Characters		80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format		8×8, alpha-numeric	8×8, alpha-numeric
Overall Dimensions (W × H × D)		274.8×240.6×17.0 mm	275.0×126.0×15.0 mm
Maximum Ratings			
Storage Temperature		−20° – 70° C	−20° – 70° C
Operating Temperature		0° – 50° C	0° – 50° C
Supply Voltage	V_{DD}	7 V	7 V
	$V_{DD} - V_{EE}$	20 V	20 V
Input Voltage		$0 \leq V_{IN} \leq V_{DD}$	$V_{SS} \leq V_{IN} \leq V_{DD}$
Recommended Operating Conditions			
Supply Voltage	V_{DD}	5±0.25V	5±0.25V
	V_{EE}	−11±3V Var.	−11±3V Var.
Input Voltage	High	V_{DD} – 0.5V min.	V_{DD} – 0.5V min.
	Low	0.5V max.	0.5V max.
Typical Characteristics (25°C)			
Response Time	Turn ON	300 ms	300 ms
	Turn OFF	300 ms	300 ms
Contrast Ratio		3	3
Viewing Angle		15 – 35 degrees	15 – 35 degrees

Design and specifications are subject to change without notice.

TOSHIBA

Toshiba America, Inc.: Electronic Components Business Sector: Head Office: 2692 Dow Avenue, Tustin, CA 92680, U.S.A. Tel. (714) 832-6300
Chicago Office: 1101 A Lake Cook Road, Deerfield, IL 60015, U.S.A. Tel. (312) 945-1500
Toshiba Europa (I.E.) GmbH: Electronic Components Div.: Hammer Landstrasse 115, 4040 Neuss 1, F.R. Germany Tel. (02101) 1580
Toshiba (UK) Ltd.: Electronic Components Div.: Toshiba House, Frimley Road, Frimley, Camberley, Surrey GU 165JJ, England Tel. 0276 62222
Toshiba Electronics Scandinavia AB: Vasagatan 3, 5 TR S-111 20 Stockholm, Sweden Tel. 08-145600

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