APRIL 19, 1984

TOP-OF-LINE DISK-DRIVE MAKERS AUTOMATE TO STAY ONSHORE/101

Choosing a touch-screen technology/140

Fault-tolerant computer transacts business fast/147

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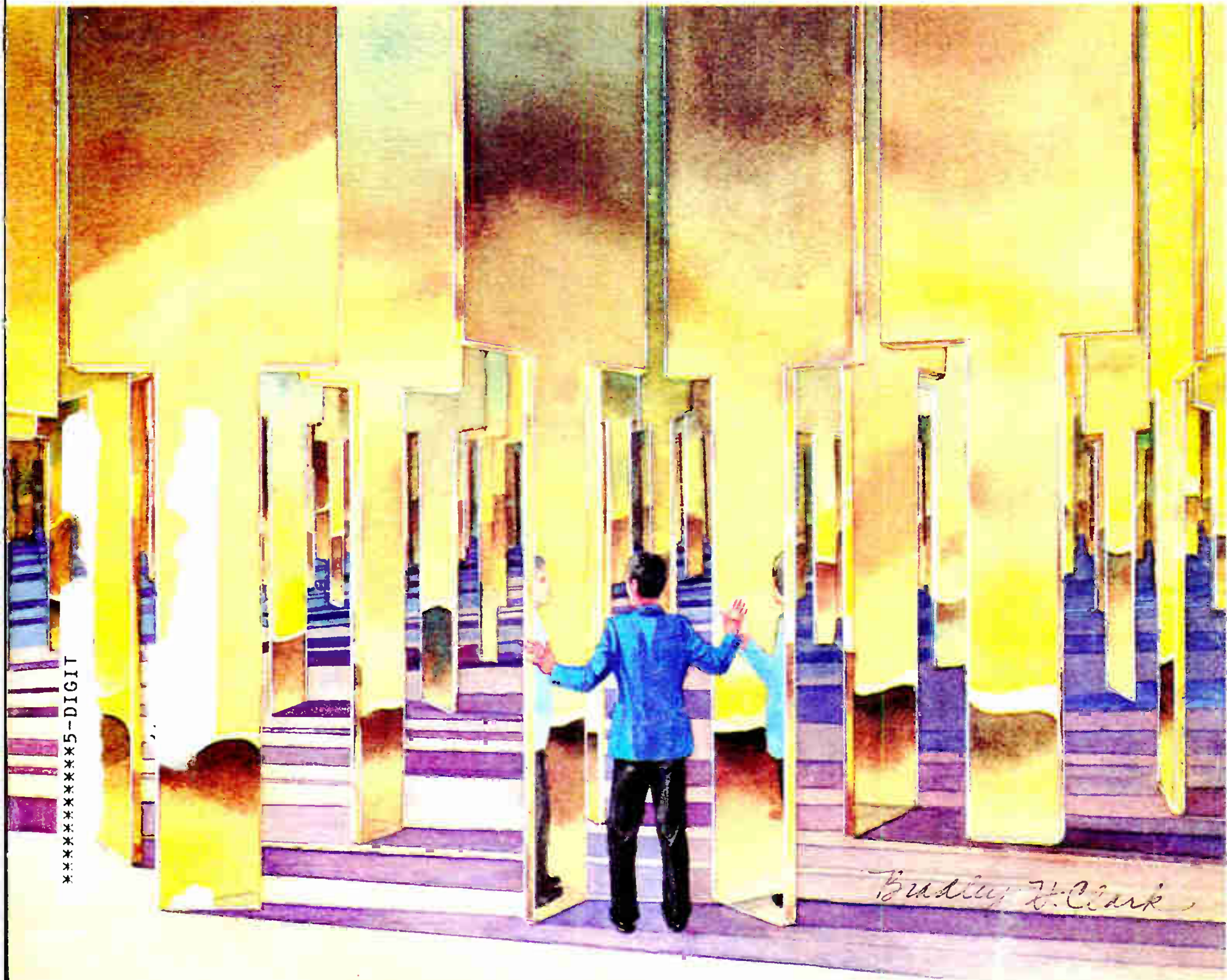

SPECIAL REPORT

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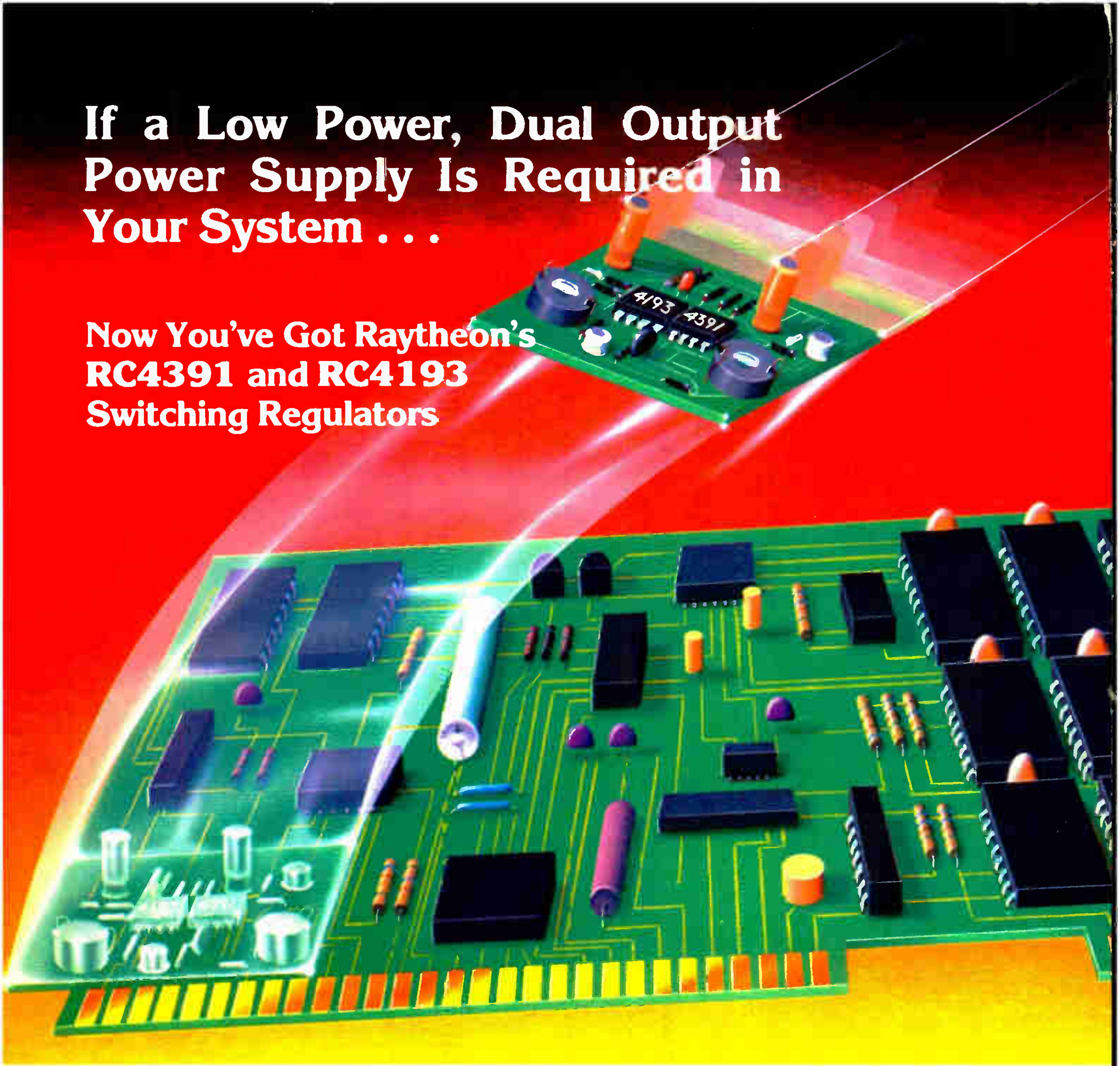

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The International Magazine of Electronics Technology and Business

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Electronics International

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Cover illustration by Bradley H. Clark

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Highlights

Four technologies vie in touch-screen terminals, 140

Intensive development is underway in the field of touch-screen terminals, as computer makers turn to them for user-friendly interfaces. This article reviews the advantages and drawbacks of the four types of touch screens—resistive membranes, capacitive sensing, acoustic-wave sensing, and optical sensing. It also discusses how they compare with the keyboard and the mouse, and more.

On-line transaction-processing computers work twice as fast, 147

These days, computers for on-line transaction processing cannot just be fault-tolerant, reasonably priced, and capable of maintaining the integrity of data. In addition, their growing popularity means that they must handle an ever-increasing number of transactions per second. To improve their performance, designers have added parallel data paths, pipelining, large cache memory, and 32-bit hardware. The NonStop TXP system is at least twice as fast as its predecessor, the NonStop II, yet also keeps software compatiblity.

Disk-drive makers' choices: automate, emigrate, or evaporate, 101

Faced with short product-development cycles, foreign competition, and unceasing pressure on prices, U. S. disk-drive makers must choose a new production strategy to stay afloat. Firms that make bottom-of-the-line hardware tend to go offshore. Many producers of high-performance drives figure that it would be better to invest heavily in plant automation and keep research and development close to production—in the U. S.

What's ahead....

Electro 84: Hewing to tradition, the coverage of this show, to be held May 15–17 in Boston, will include a preview of new products that will be making their debuts. In addition, there will be a report on how business is flourishing on Route 128, the hub of the area's electronics activity. . . . **May 3.**

Electronic Components Conference: As a report on this annual conference, scheduled for May 14–16 in New Orleans, will make clear, the show will be devoted as much to manufacturing and packaging technology as to materials and reliability. . . . **May 3.**

Data-base systems: This special report will clarify the issues surrounding data-base systems for microcomputers. What are the advantages of relational data-base systems? What types of systems are offered? The article will answer these and other questions. . . . **May 17.**

Smart power devices: A staff-written analysis will review recent developments and future trends in smart-power technology: the integration of logic and power on a single chip. . . . **May 31.**

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Editor's letter

Whenever VLSI designers get together, you hear talk of shrinks and densities and yields, as well as much bragging about chip-size reduction and breakthroughs in such performance parameters as noise margins and speed and access times. But you almost never hear these designers talk about testing. That's because—like everyone else—they prefer to discuss problems that are yielding to progress, not such intractable ones as testing.

Every advance in very large-scale integration brings with it many new problems in testing. You don't have to be a genius to realize that checking out a chip with 100,000 devices on it, and getting a reasonable assurance that it will process faultlessly whatever combination of inputs and timing may come its way, represents a formidable problem—one that chip designers often don't care to think about.

Nevertheless, some people do think about the unthinkable, and some of them work for *Electronics*. One is senior editor Howard Bierman, who is charged with covering test and measurement technology and agrees with me that testing will probably be the most important limitation on the advance of semiconductor technology. For his special VLSI testing report, which begins on p. 125, Howard began gathering information last fall at Philadelphia's Cherry Hill International Test Conference. He also traveled widely, talking to test-equipment manufacturers and users to find out what progress is being made or planned.

Besides his own overview of what's going on in the VLSI test world, Howard's report includes two other articles. One, from a leading test-equipment manufacturer, deals with the increasingly common need to test both analog and digital functions on the same complex VLSI chip. The other is from a testing expert: as the technical vice president of Viking Laboratories, an independent organization that specializes in testing semiconductor devices for qualification under military specifications, Eugene Hnatek is in an excellent position to discuss the complex problems of VLSI testing. He brings to the discussion a unique objectivity that is hard to find in this field.

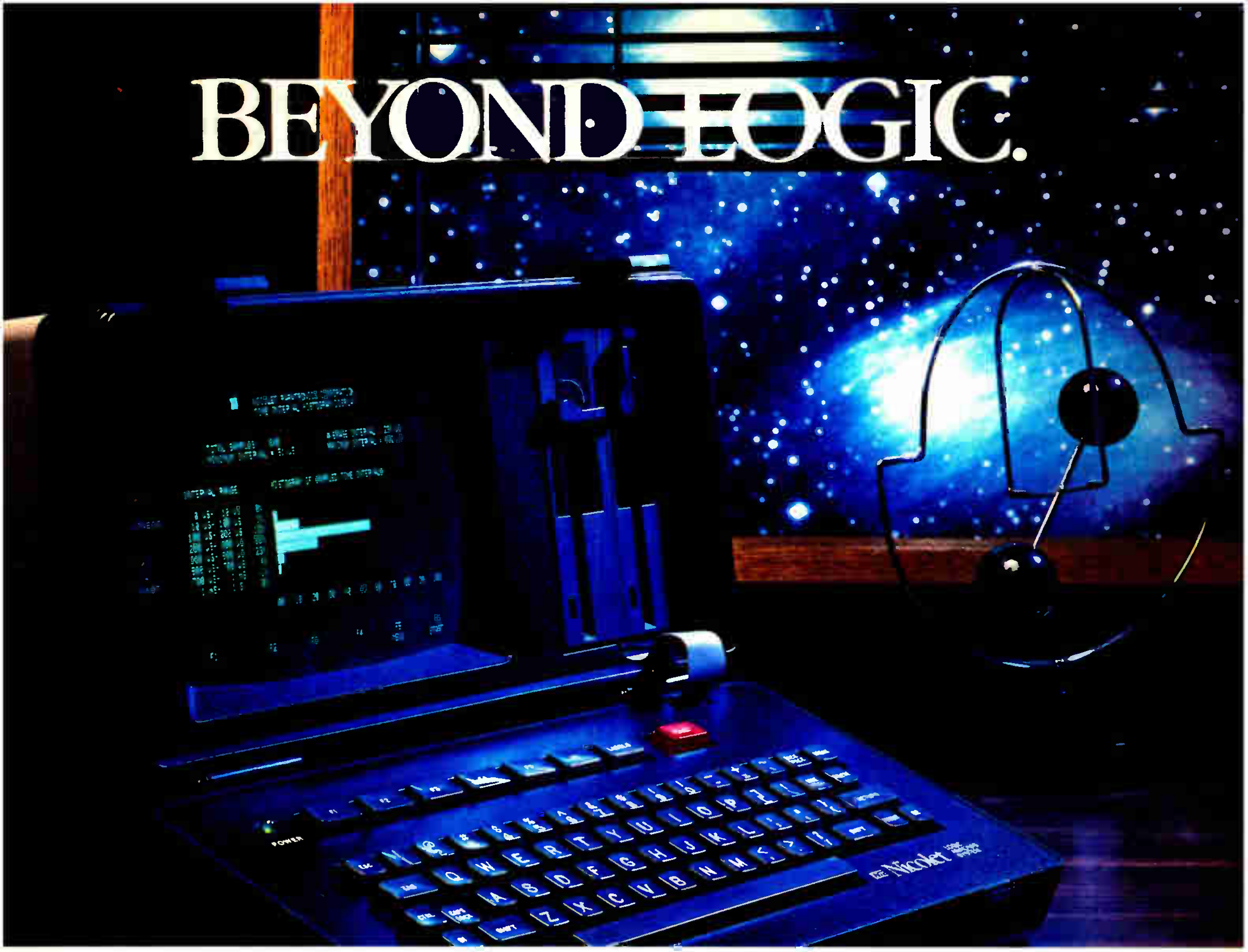
If ever proof were needed that the electronics marketplace is international in scope and that any publication aspiring to cover it responsibly must have worldwide resources, that proof is furnished by four stories in this issue.

First, there is the emergence of Korea as a potential force in the electronics marketplace (p. 105). With a billion-dollar funding kitty, four Korean firms are getting set to plunge into sophisticated memory and personal computer markets. To report on this significant new development, we sent Mike Berger, the Tokyo bureau chief of McGraw-Hill World News, to Korea.

Closer to home is a story (p. 101) from Los Angeles bureau chief Larry Waller on the difficult decision faced by U. S. Winchester-disk-drive makers: whether to automate or to move offshore to stay price-competitive with foreign competitors in this volatile market segment.

The third story (p. 108) is an account by Frankfurt bureau manager John Gosch of how the semiconductor division of the German giant AEG-Telefunken, nearly bankrupt two years ago, has made a remarkable recovery with a little U. S. help.

Another example of our U. S editors covering a story domestically that ends up with international implications, is communications editor Terry Feldt's report on the burgeoning market for low-noise amplifiers and converters, which is being stimulated by the development of direct broadcast satellite services (p. 114). Terry covered the recent Satellite Systems Conference held in Orlando, Fla., and found himself spending a lot of time with engineers from NEC Corp., the dominant suppliers of GaAs components for direct-broadcast-satellite earth stations.



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Readers' comments

Acceptance, not partnership

To the Editor: The quote attributed to me in "Philips seeks partner for high-quality, high-definition TV scheme" (March 22, p. 56) was not quite accurate. I am quoted as saying that "we [Philips] would feel much more comfortable" with a partner. What I said was that Philips would like to see other companies aware of the developments at Philips Laboratories, and this was one of the reasons we were happy to hear that your publication was interested in conveying the results of our research.

We felt that when the NTSC industry became aware of the success we achieved with signal processing using new charge-coupled-device field-memory integrated circuits, there would be further interest in adopting our developments. Acceptance by the industry would indeed make us feel more comfortable than confronting the disarray that would evolve if alternative or incompatible approaches to high-definition television were undertaken.

Joseph S. Nadan, Ph. D.
Philips Laboratories
Briarcliff Manor, N. Y.

TV sets as video displays

To the Editor: Regarding your article "VCR can be low-cost interface between personal computer and TV" (March 8, p. 152), I would like to offer a few words of caution.

First, although all home computers are designed to be connected to home television sets, personal computers often require special monitors. For example, International Business Machines Corp.'s very popular Personal Computer has a monochrome high-resolution output that cannot be used with a home TV. Some personal computers are noted for nonstandard scanning rates or synchronization signals, which often prevent their use on the latest TV sets—those without vertical hold controls.

Even computers that use Electronic Industries Association RS-170-type video signals may not be employable with home TV sets, because most have extremely poor bandwidth to prevent color interference. A

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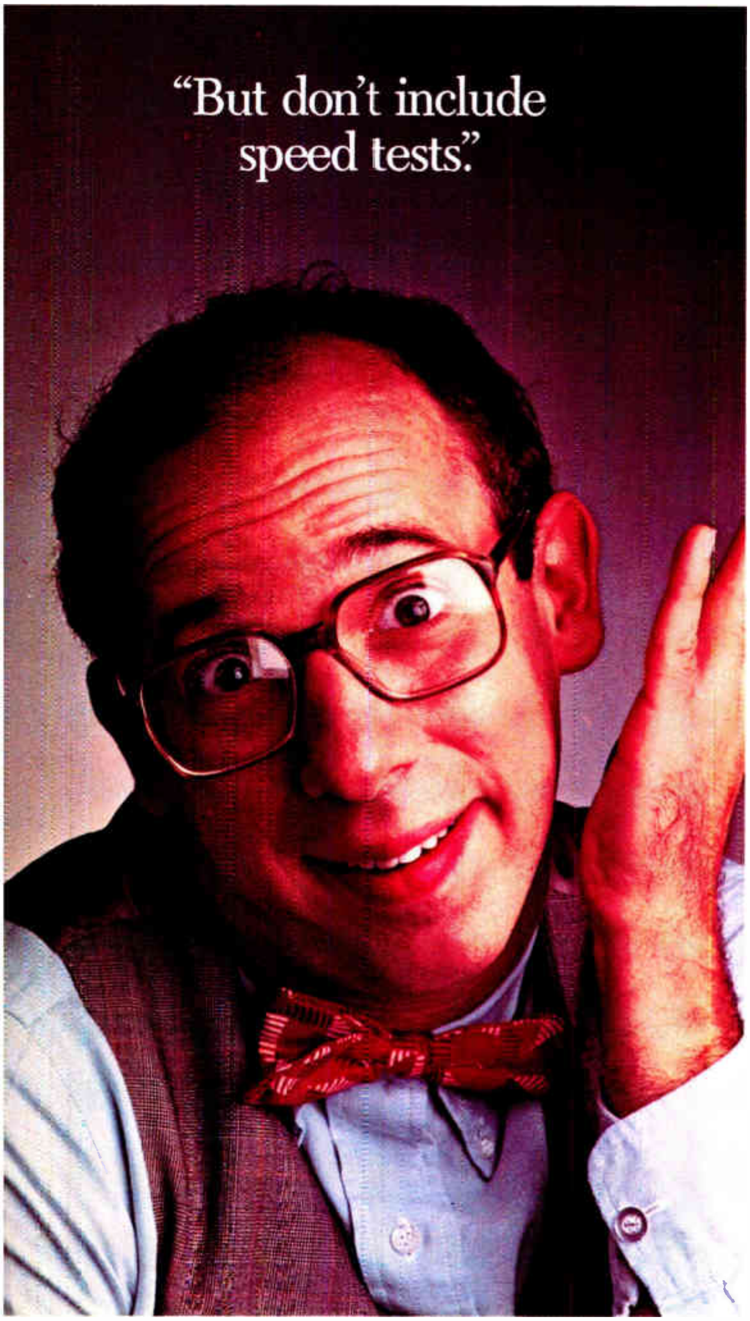

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Readers' comments

bandwidth of 2 megahertz would allow only about 100 light-dark cycles to be displayed across the width of the TV screen, and that is not at all adequate for a display of 80 characters.

Since most home TV sets are overscanned, the chances are excellent that they will lose the left and right columns and the top and bottom rows of information. What's more, on color sets, the registration of colors is concentrated on the center of the picture, so the critical upper-left corner may be bedevilled by annoying color fringes.

Even on those few sets that do use comb filters to increase video bandwidth, the pictures will be fuzzy after playback from a video-cassette recorder, which is likely to limit the bandwidth to 2 MHz. Furthermore, many VCRs just will not record signals with nonstandard synchronization signals, a phenomenon that has been exploited for popular antipiracy encoding techniques.

VCRs are therefore most useful when they are employed in conjunction with home computers that offer an unrestricted number of characters per row with standard video output. Unfortunately, however, most of these home computers have been designed to include built-in radio-frequency modulators.

One final note of caution: some VCRs will disconnect their tuners in favor of whatever happens to be plugged into their video input jacks. Leaving a computer plugged in, even if it has been turned off, may therefore prevent VCRs from being used to record TV programs.

Mark Schubin
New York, N. Y.

A correction

In Fig. 5b of our special report on flat-panel displays ("Flat panels are getting bigger, better, and brighter," March 22, p. 119), the colors were inadvertently interchanged. The color for the curve that depicted the brightness of the red phosphor should have been blue, and the color for the curve that depicted the brightness of the green phosphor should have been black.

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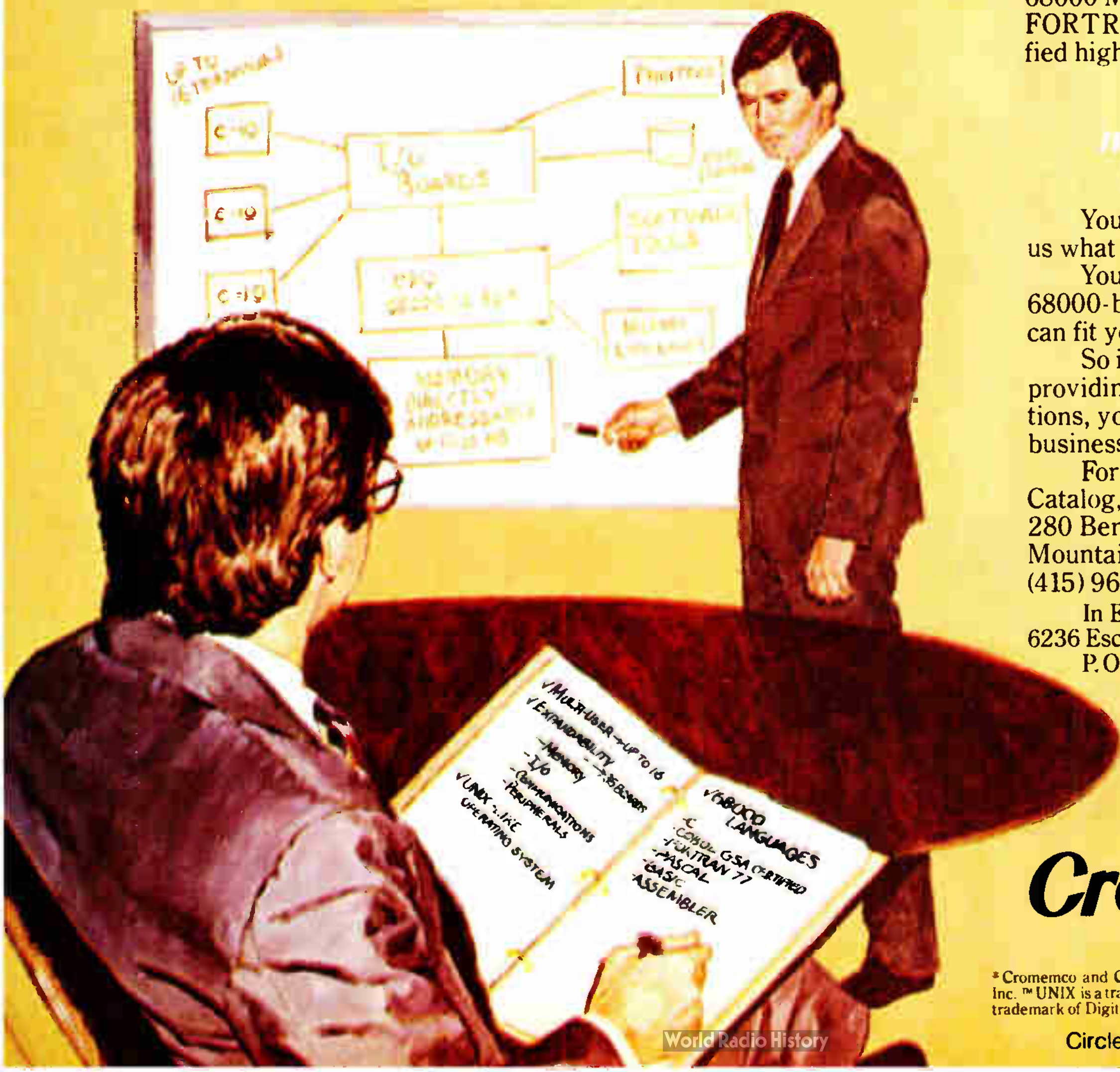

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People

Samsung's Engelbrecht aims for a spot in the top 10

Among the four heavyweight Korean companies charging after the world semiconductor markets (see p. 105), the Samsung Group, of Seoul, is first off the mark. One of its key players is Ronald G. Engelbrecht, vice president for marketing and sales at Tristar Semiconductor Inc., the subsidiary that Samsung set up in Santa Clara, Calif., in mid-1983 to develop chips, wring out their design, and get them into pilot production.

The strategy that Engelbrecht is helping implement is to do the high-technology part of the business in Silicon Valley and then move the process back home for mass production. Samsung's long-term goal in semiconductors is to become one of the world's top 10 producers soon after 1990. "It's very aggressive, but you have to have goals," says the 19-year veteran of the Silicon Valley semiconductor scene and the only native-born American among Tristar's half-dozen top executives.

"We are now turning out 2,000 five-inch wafers a month," he explains. "The chip is a 64-K dynamic RAM that we bought from Micron Technology [of Boise, Idaho]. It's really a trial run for the 80,000 wafers a month that Samsung will be producing by 1987."

Tristar's next major offering will be an electrically erasable programmable read-only memory designed jointly with Exel Microelectronics, San Jose, Calif. Both RAM and EE-PROM are in n-channel MOS, but complementary-MOS chips will be coming off the line by midyear. "We'll design our own 64-K EE-PROM, 64-K static RAM, and 256-K dynamic RAM in C-MOS," adds Engelbrecht, a graduate of the University of South Dakota, where he studied math and physics.

"For the next couple of years, about 80% to 90% of our business will be in memories," Engelbrecht says. For the moment, the remainder is mainly operational amplifiers and telecommunications chips. But later on the company plans to diversify with microcomputers, more telecom chips, a line of fast C-MOS logic, and a C-MOS cell library.

The Korean influence could be crucial in helping Tristar to achieve these goals. "Work is a way of of life and not just a vocation for Koreans," Engelbrecht says.

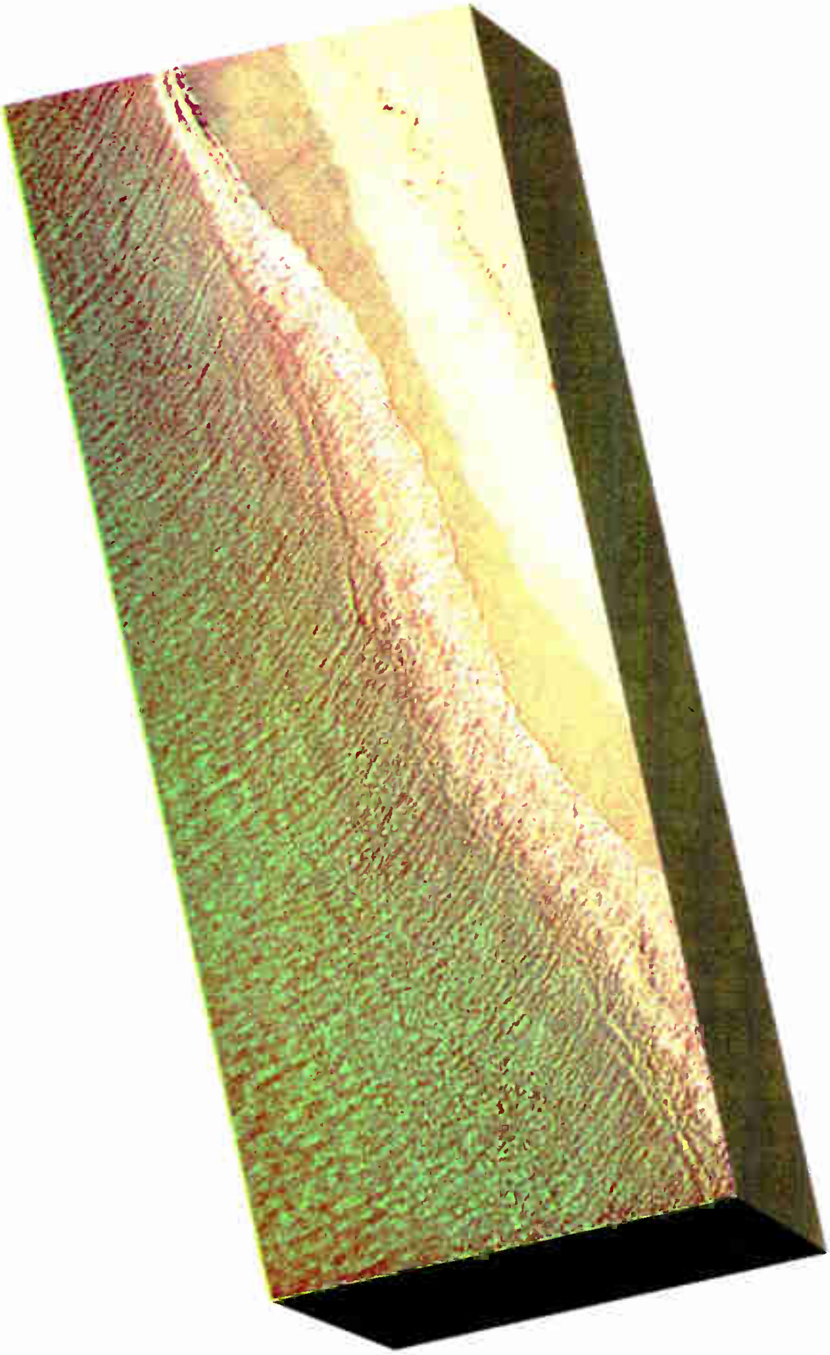
Ambitious plans. Ronald G. Engelbrecht will lead Tristar into microcomputers and other advanced chips.

Poppa leads BMC Industries down the acquisition trail

Ryal R. Poppa is at it again. The chairman, president, and chief executive officer of BMC Industries Inc., in St. Paul, Minn., is hard on the acquisition trail. Since coming on board in early 1982, the executive has already masterminded nine corporate takeovers for BMC involving some 20 separate firms, with more coming.

This fact will come as no surprise to those who recall his eight-year tenure at the reins of Pertec Computer Corp., an Irvine, Calif., systems firm, where Poppa gained a reputation for an acquisition-driven growth strategy before Pertec itself was swallowed by West Germany's Triumph-Adler AG in 1979.

Poppa, 50, does not profess to be a technology expert, but rather describes himself as a trend watcher. And although he intends to maintain BMC's presence in its historical businesses—including precision aperture masks and optical lenses and eye-



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People

Thinking big. Ryal Poppa wants BMC Industries to be a major packaging firm with emphasis on advanced surface mounting.

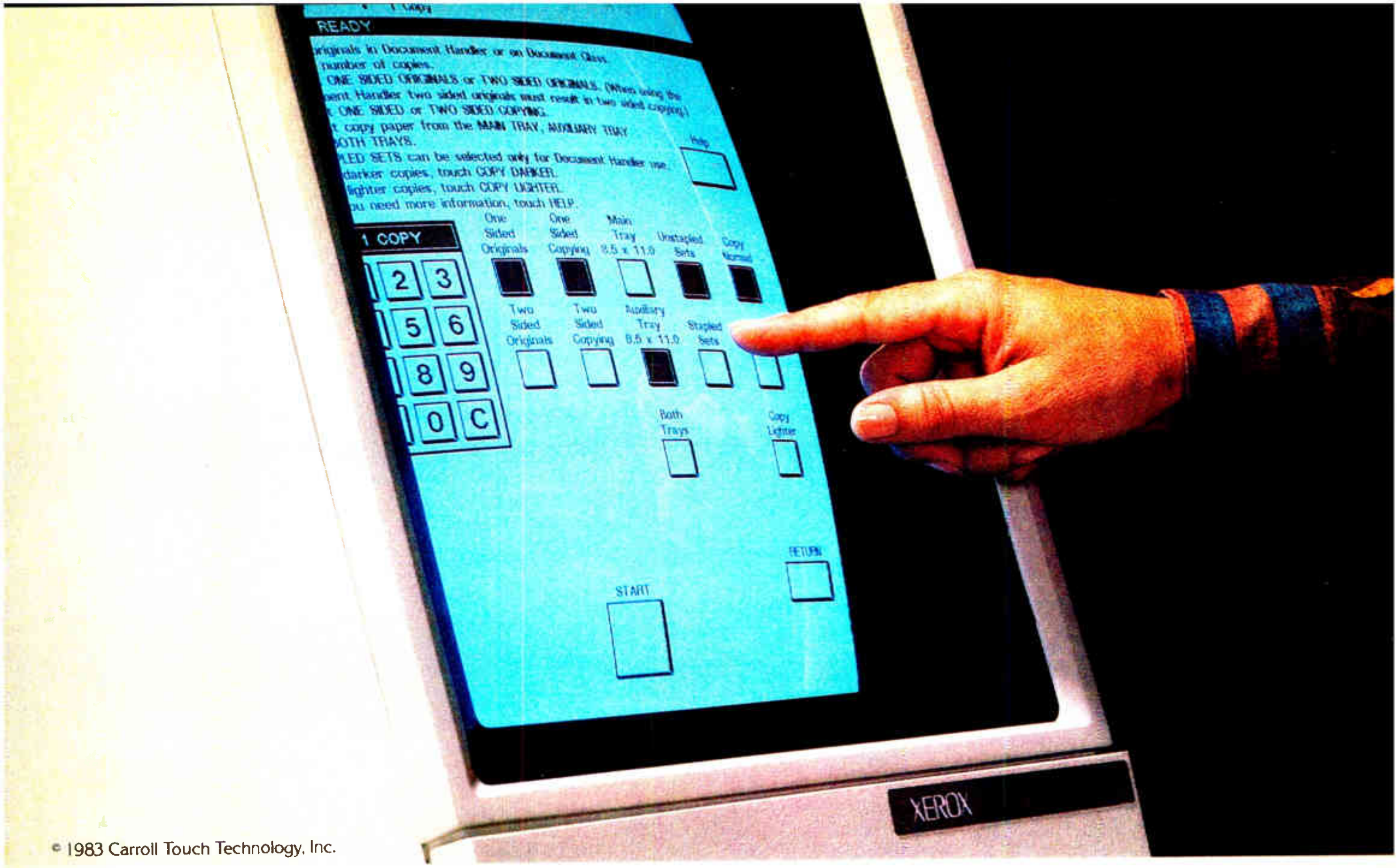
glass frames—he is placing his major bets on the trend he sees toward electronics surface-mounting technology.

His plan is to build BMC (formerly Buckbee-Mears Co.) into a major electronics packaging and interconnection house, with expertise in advanced surface-mounting technologies. "I believe there's going to be a massive change in the packaging business, and I want to be on the front edge," he says.

BMC sales last year totaled $156 million. Most acquisitions so far have been in the $2 million to $14 million range, and include firms with interests in flexible and multilayer printed-circuit boards, pc-board drilling- and routing-machine tools, and custom hybrid circuits.

This year, sales are expected to climb to the $300 million to $325 million range, thanks largely to more than $100 million in anticipated additional revenues from the newly acquired Tampa Operations of Honeywell Inc. Poppa expects sales in the $750 million range by 1987.

A North Dakota native, Poppa has no formal technical education; he graduated from Claremont Men's College, Claremont, Calif., in 1957 with a bachelor's degree in economics and finance. But he has spent his entire career in the computer industry, first with 10 years in sales at International Business Machines Corp., followed by top-level executive posts at such firms as Greyhound Computer, Data Processing Financial and General, Mohawk Data Sciences, and Pertec.



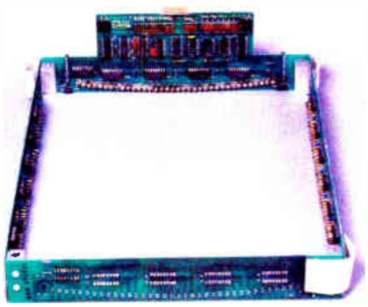
Carroll put the touch on Xerox

It would have taken 129 buttons to activate the functions of the Xerox 5700 electronic printing system. But thanks to a friendly input system from Carroll Touch Technology, all it takes is a touch.

The Xerox laser printer incorporates Carroll's scanning infrared touch system. That means the full capabilities of every Xerox 5700 are literally at your fingertips. Touch the screen, the system responds. Quickly. Easily. No buttons or keyboard required.

Carroll's touch input system is not an overlay. Nothing distorts or interferes with a clear, sharp image.

The Carroll system uses a matrix of LEDs and phototransistors mounted around a video display screen. A grid of infrared light beams covers the entire display, invisible to the naked eye. Whenever a light beam is broken by the user's fingertip or stylus, the system reacts.



Carroll makes standard touch input systems for a variety of CRTs and flat displays. Custom designs for military and OEM use are also available.

Carroll has designed and manufactured touch input systems for AT&T, Raytheon, TRW, United Technologies (Norden), and other Fortune 500 companies. Now, let us design a touch input system for you.

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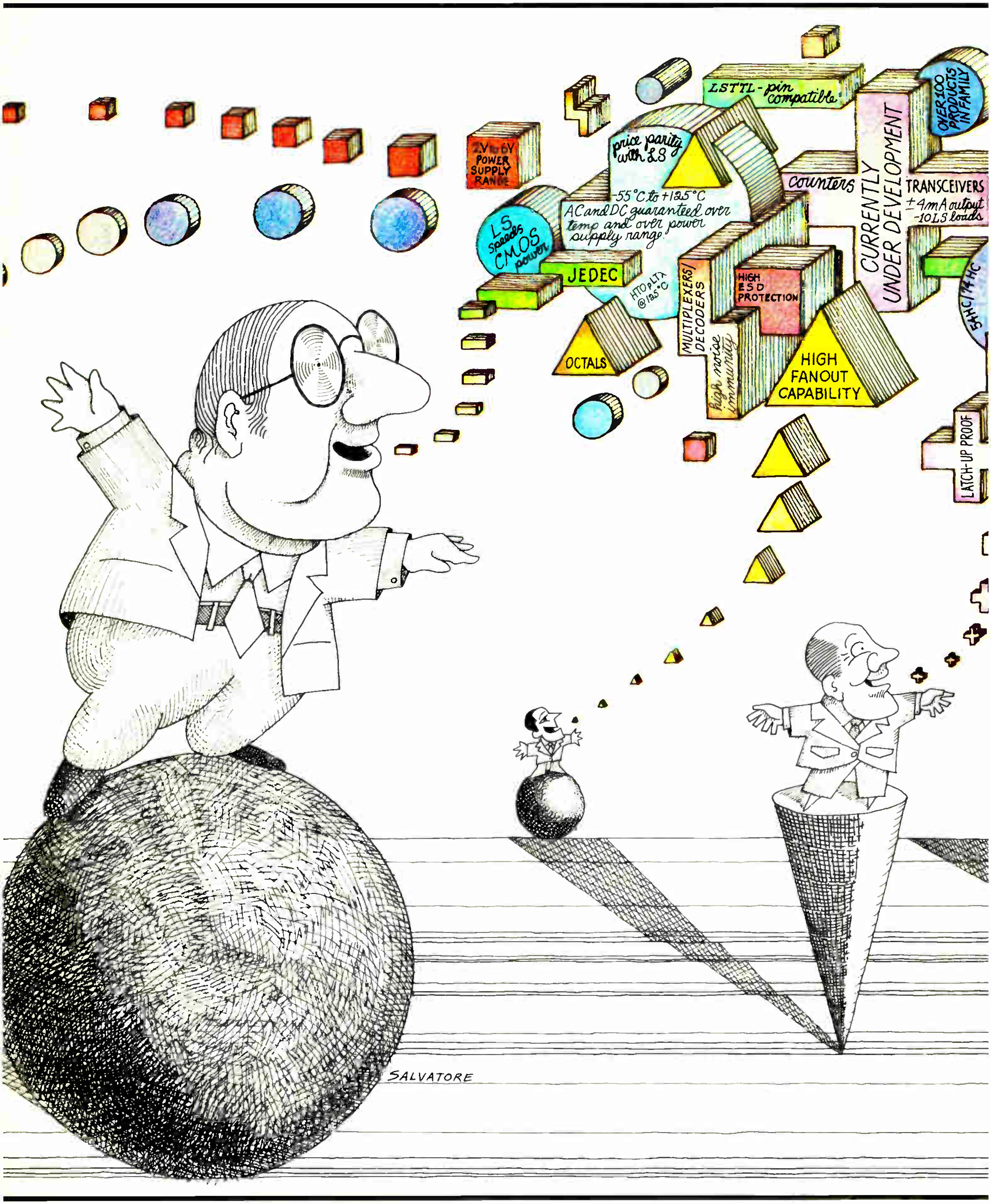

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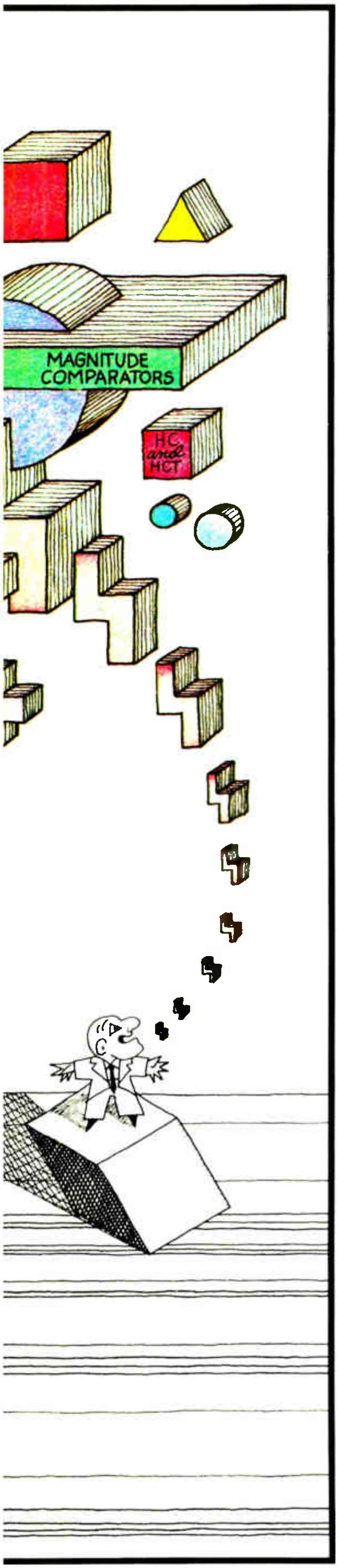

Everybody talks high-speed CMOS logic.

But only National goes beyond talk with the broadest and most completely specified HC logic family.

"ESD protection!" "Latch-up immunity!" "LS speeds!"

It's easy to talk a good line.

But at National, we've actually *built* one: our 54HC/74HC microCMOS family. The broadest HC logic line in the industry. With 195 products documented, characterized and specified. On paper.

Products that are easier to design with because National guarantees AC and DC characteristics over temperature (−40°C to +85°C for 74HC and −55°C to +125°C for 54HC), and over the entire power supply range of 2 to 6 volts. And they're alternately sourced by Motorola Inc.

Reliability?

Our 54HC/74HC logic family is latch-up proof when tested at 500mA and +125°C on the outputs. It's also protected from ESD. Tests show it exceeds the ESD resistance of bipolar logic.

How is this possible? Because our small geometry, silicon-gate, oxide-isolated microCMOS manufacturing processes yield exceptional quality and reliability.

Statistics prove it. Our outgoing electrical process defect average (AOQL) is under 80PPM, with an actual failure rate (HTOpL) of less than 0.04%/1000 hours at 125°C.

So, if you're thinking of designing high-performance CMOS into your next project, remember: At National, we're not just talking about it. We're doing it.

For a copy of our microCMOS brochure, contact us at 2900 Semiconductor Drive, MS 23200, Santa Clara, California 95051.

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NEC NEWSCOPE

JORDAN MOVES UP TO CELLULAR MOBILE TELEPHONE

NEC will install an advanced cellular mobile phone system in Jordan by the end of 1984. The system will provide high-grade mobile telephone service in the 800MHz band. Initially, it will serve 1,500 subscribers in the capital and its suburbs (Greater Amman). It will have six mobile base stations (10 radio zones). Plans call for expansion to accommodate 10,000 subscribers with a network of mobile base stations covering the entire nation of Jordan.

A digital switching system will serve as the control center of the mobile telephone network. An MTS version of the renowned NEAX61 central office system will be used to interface the mobile service with the public switched telephone network. This interface will be handled through a tandem switching system.

NEC's Advanced Mobile Telephone System is a highly sophisticated cellular system integrating every type of equipment required for fully automatic mobile telephone service. It facilitates communications between vehicles and land subscribers and between vehicles.

NEC installed the world's first commercially operated cellular mobile telephone system in Tokyo. Other NEC cellular systems installed include an 800MHz system in Hong Kong, 400MHz systems in Mexico and Singapore and a 500MHz system in Australia.

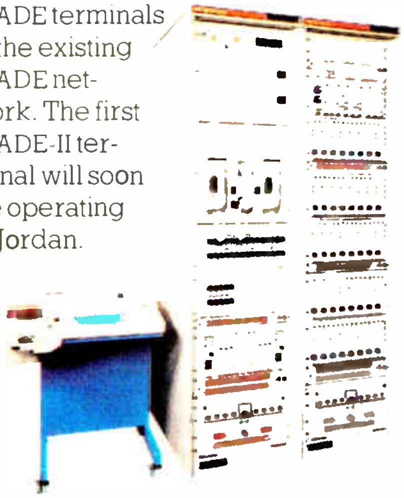
NUMBER 130

SPADE-II FOR INTELSAT ATLANTIC REGION

SPADE-II terminal equipment, designed to the latest INTELSAT SPADE Specification and completely compatible with existing SPADE terminals, will soon make its operational debut in the INTELSAT system, Atlantic Ocean Region. Incorporating state-of-the-art microprocessors and LSIs, it provides excellent reliability as well as simple operation.

The SPADE system allows a user to establish a communications circuit on demand with any other SPADE user, greatly improving satellite transponder utilization efficiency. It handles several times more telephone traffic using the same number of SCPC channel units. In addition, it considerably reduces annual operation cost because each SPADE circuit is billed not on a fixed annual rate but on an actual utilization basis.

NEC supplied 28 of the original SPADE terminals in the existing SPADE network. The first SPADE-II terminal will soon be operating in Jordan.



NEW LDR SYSTEM FOR BUSINESS COMMUNICATIONS

NEC now offers a highly sophisticated 10.5GHz digital local distribution radio (LDR) system. It meets the increasing need for low-cost, high-speed, and quality transmission of digital data for business communications.

NEC's 10.5GHz system, first put into operation in New York City, was developed as an advanced technological solution to local distribution problems. The system is based on a field-proven 2GHz LDR system using TDMA technology.

The new system provides point-to-multipoint digital microwave links for local distribution of data and voice from a node station to many subscribers with a single pair of radio frequencies. Each system covers a 90-degree sector with a radius of up to 15km. As many as 26 subscriber stations in each sector are served by one local node station. Radio frequency reuse in several quadrants can significantly increase the service range and maximize system flexibility.

The LDR system transmits up to twenty-six 56 or 64 kbps data or voice channels—a total bit stream of approximately 1.8 Mbps per carrier. As many as 104 subscribers can be accommodated by one node with a maximum configuration.

A key feature of the system is its low interference susceptibility. The system allows a very low carrier-to-noise ratio to obtain the required error rate performance by using quadrature phase shift keying (QPSK) modulation, thus enabling many frequencies (up to 20) to be used in the same area.

NEW 1,300nm LASER DIODES

NEC's new laser diodes feature our exclusive Double-Channel Planar Buried Heterostructure (DC PBH). This feature improves efficiency and reduces the temperature dependence of the operating current. Double channel structure also minimizes crystalline defects to provide more stable operation.

As a result, new laser diodes guarantee 5mW minimum output up to 60°C. They eliminate the need for thermo electric coolers and thus permit more compact equipment design. They also feature low threshold and operating currents: 20mA/50mA(25°C, 8mW).

The improved service life results in an estimated MTTF of more than 100,000 hours for 5mW operation at 50°C. Other features include stable fundamental transverse mode and nearly circular beam.

NEC
NEC Corporation
Tokyo Japan

Engineering is no threat to the funding of science

Scientists and engineers have decided to reheat their ancient and high-toned rivalry just as we thought it was safe to poke our heads inside the lab once again. The fuse was lit at recent hearings of the House Science and Technology Committee, which was considering proposed amendments to the National Science Foundation's legislative charter that would require it to give equal funds to engineering research and development.

It is irrelevant to say that the public cares less about this issue than about whether the sun will shine on Sunday. At stake is nothing less than a great deal of Federal financial support, which seems to generate more ardor than we might expect from bespectacled gentlemen hacking at one another with furled umbrellas. And of course, engineers have traditionally been quick to take umbrage at the haughtiness of certain self-styled "pure" scientists who peer down at them as little more than glorified technicians tainted by commerce.

This struggle for equality of funding under the NSF is not new. Engineers argue that without their work, science would have no value that would justify the Government in spending so much money on it. Conversely, the poohbahs of science have opposed such parity as a threat to their most important source of funding. NSF president Frank Press summed up the scientists' argument for the committee. "What are the likely outcomes?" he asked in his prepared testimony. His reply: "A major change, I fear, may be to dilute the fundamental mission for which the foundation was created—to support basic research in all the sciences."

He said too that "in contrast to engineering, many of the sciences depend on the NSF for a predominant fraction of their support." And with that argument, Press implied a mouthful, for many sciences also depend on engineering for support. Such institutions as Bell Labs, IBM's Watson labs, and RCA's Sarnoff labs are monuments to the mutual needs and goals of science and engineering, and so is the space program, for which engineers got little credit but provided much of the wherewithal.

In this fast-moving world, "pure" is no more useful an idea than phlogiston or the epicycles of Ptolemy. We doubt that science would be the loser in an NSF that gave equal weight to engineering. In fact, it has much to gain, for it is engineers, with their can-do bent and fine-tuned commercial antennas, who perform the cross-pollination that prevents science from withering away into irrelevance.

Press also claimed that he has given the National Academy of Engineering equality with the NSF. But the fact that the engineering academy's president, Robert M. White, supports the equal-status amendments speaks for itself.

Finally, we are indebted to the always urbane journal New Scientist for its definitions of science and technology (for which read engineering) and for the chance to apply them to the current controversy. Here they are, translated from the British.

Pure science: it's mine, and I'm not going to explain it to you.

Technology: the result of giving large sums of money to possessive pure scientists.

THE SWITCH IS ON TO EECO THUMBWHEELS

Good news travels fast. And the news is EECO has added six new innovative switches to the broadest line of quality thumbwheels anywhere. And on-time delivery of the entire line is assured through our international sales network.

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New MIL-S-22710/15 QPL'd Thumbwheel *EECO's Series 7000 is the most rugged and reliable thumbwheel ever. Environmentally sealed—with a host of options, features and codes—this front-panel Hercules offers the versatility to meet most any military application.*

The Reliable Standards 1776/1976 *Since introducing the 1776/1976 in 1978, these thumbwheel switches have established themselves industry-wide as a standard of reliability and excellence. Made to last, offered with a wide choice of options, and affordable—these switches are EECO's tried-and-true performers. And still revolutionary.*

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Meetings

Computer Graphics 84, National Computer Graphics Association (8401 Arlington Blvd., Fairfax, Va. 22031), Anaheim Convention Center, Anaheim, Calif., May 13–17.

Seventh Conference of the British Robot Association, British Robot Association (Conference Organiser, British Robot Association, 28-30 High St., Kempston, Bedford MK42 7AJ, UK), Cambridge, England, May 14–16.

International Conference on Communications, IEEE (T. A. C. M. Claasen, Philips Research Laboratories, WY-2, 5600 MD, Eindhoven, The Netherlands), RAI Conference Centre, Amsterdam, May 14–17.

Electro/84 and Mini/Micro Northeast/84, IEEE (Electronic Conventions Inc., 8110 Airport Blvd., Los Angeles, Calif. 90045), Hynes Auditorium, Boston, Mass., May 15–17.

Communications 84, Industrial and Trade Fairs Ltd. (Communications 84, Industrial and Trade Fairs Ltd., Radcliffe House, Blenheim Court, Solihull, W. Midlands B91 2BG, UK), National Exhibition Centre, Birmingham, May 15–18.

C³I Long-Range Planning Conference, Department of the Air Force and Electronic Industries Association (EIA, Government Division/Requirements Committee, 2001 Eye St., N. W., Washington, D. C. 20006), Mitre Corp. Auditorium, Bedford, Mass., May 16–17.

Printed-Circuit World Convention III, Institute for Interconnecting and Packaging Electronic Circuits, European Institute of Printed Circuits, Japan Printed-Circuit Association, *et al.* (Printed-Circuit World Convention III, c/o IPC, 3451 Church St., Evanston, Ill. 60203), Sheraton Washington Hotel, Washington, D. C., May 20–25.

Custom Integrated-Circuits Conference, IEEE (Savvas G. Chamberlain, Electrical Engineering Dept., University of Waterloo, Waterloo, Ontario, N2L 3G1 Canada), Genesee Plaza Holiday Inn, Rochester, N. Y., May 21–23.

AAMSI Congress 1984, American Association for Medical Systems and Informatics (AAMSI, Suite 402, East-West Highway, Bethesda, Md. 20814) Hilton Hotel, San Francisco, Calif., May 21–23.

Fourth Jerusalem Conference on Information Technology, Information Processing Association of Israel & IEEE (Noah S. Prywes, Program Co-Chairman, JCIT-4, P. O. Box 639, Silver Spring, Md. 20901), Jerusalem, Israel, May 21–25.

Naecon, IEEE (Jerry Duchene, 7327 Brandvista Ave., Dayton, Ohio 45424), Dayton Convention Center, Dayton, May 21–25.

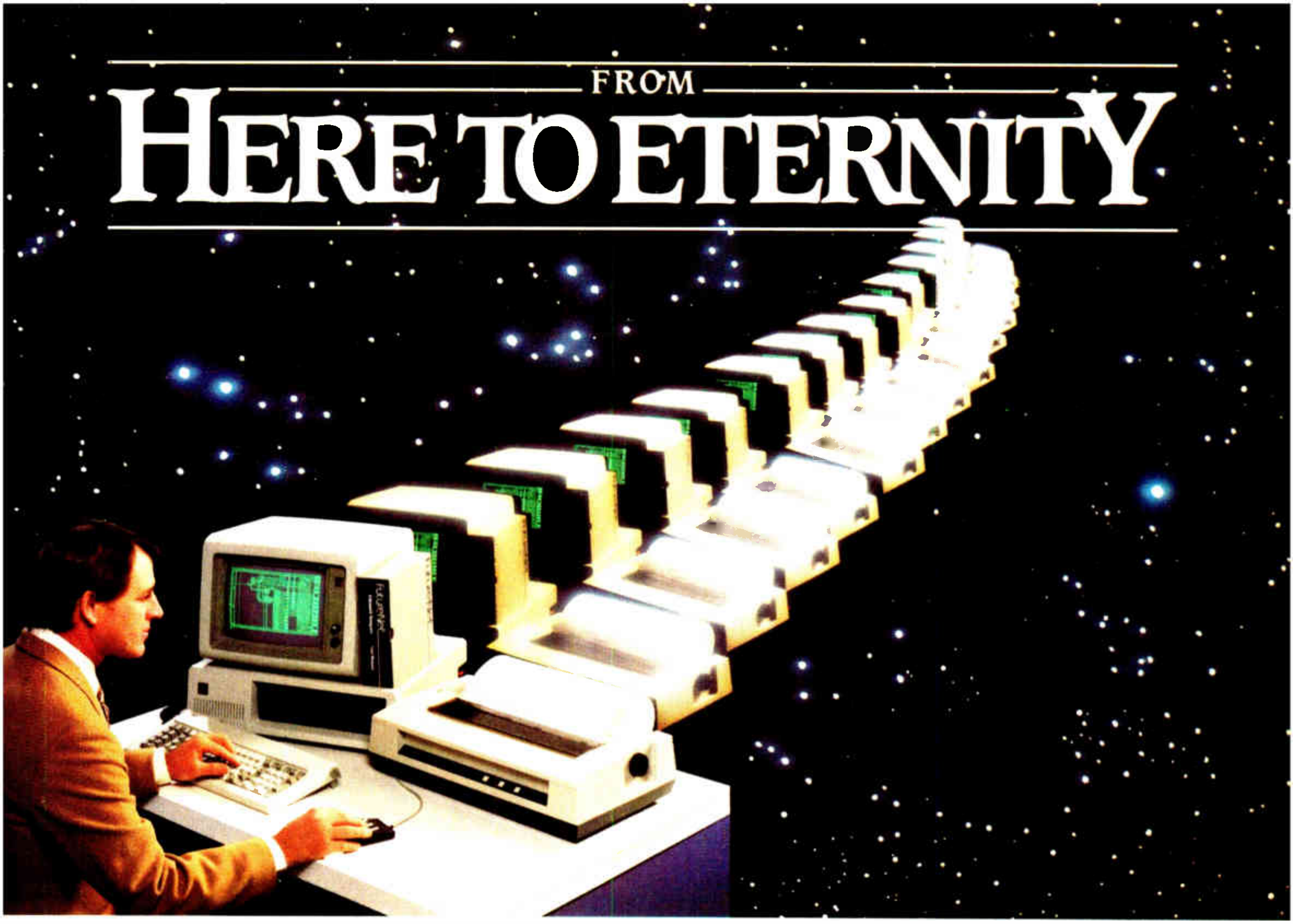
Semicon/West 84, Semiconductor Equipment and Materials Institute Inc. (Susan Castillo, SEMI, 625 Ellis St., Suite 212, Mountain View, Calif. 94043), The Fairgrounds, San Mateo, Calif., May 22–24.

Comdex/Spring 84, The Interface Group Inc. (300 First Ave., Needham, Mass. 02194), Georgia World Congress Center, Atlanta, Ga., May 22–25.

1984 Trends and Applications Conference, IEEE and National Bureau of Standards (Helen Wood, A255, Technology Building, NBS, Washington, D. C. 20234), Gaithersburg, Md., May 23–24.

First Australian Automated Manufacturing Conference and Exhibition, Automach Australia 84, The Society of Manufacturing Engineers (One SME Dr., P. O. Box 930, Dearborn, Mich. 48121), Royal Hall of Industries, Sydney, May 23–25.

International Symposium on Electron, Ion, and Photon Beams, IEEE (John Kelly, Hewlett-Packard Laboratories, 500 Deer Creek Rd., Palo Alto, Calif. 94304), Westchester Marriott Hotel, Tarrytown, N. Y., May 29–June 1.



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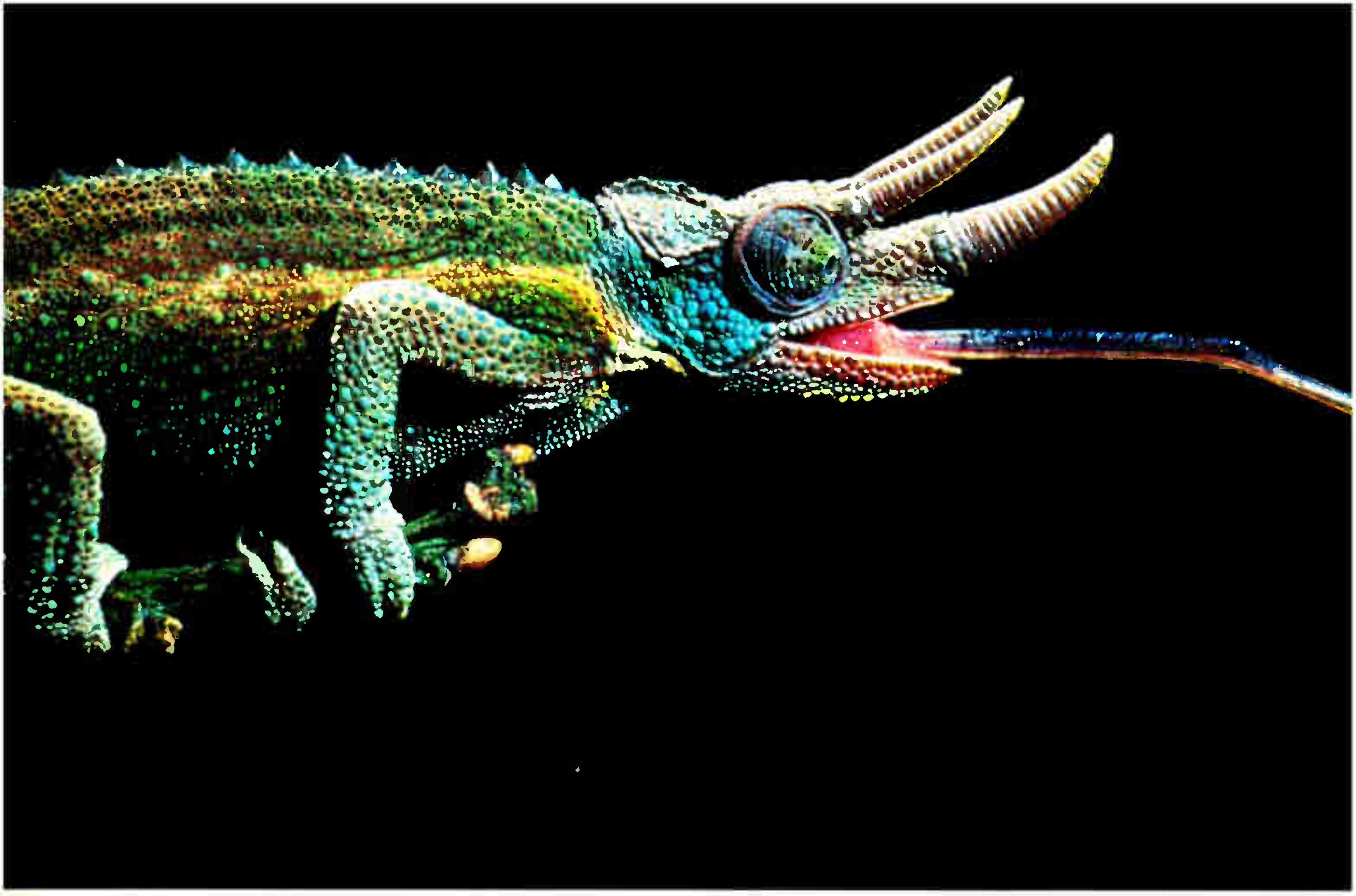


WHEN SPEED IS THE ISSUE

GaAs ICs FROM HARRIS MICROWAVE SEMICONDUCTOR

The Three-horned Chameleon (chamaeleo jacksonii) *depends on speed to stay alive. With a tongue faster than a small-caliber rifle bullet, it can strike a fly in flight at six inches. With clock rates 5 times as fast as silicon ECL, Harris Microwave Semiconductor's new Gallium Arsenide ICs give you design freedom never before possible with digital technology.*

OUTPERFORMS ALL AVAILABLE DEVICES

A universal Shift Register operating at up to 1.4 GHz clock speed, and a Binary Counter running at data rates up to 2.0 GHz outperform all known products in applications requiring subnanosecond system response times and reliable operation. At last, designers of EW signal processing systems, supercomputers, instrumentation, and high-speed data communications systems have the speed and bandwidth necessary to realize the full potential of their designs.

ECL/GaAs COMPATIBLE

Harris' Shift Register and Counter (the first two in a family of GaAs SSI & MSI products), are compatible with ECL, and with other GaAs devices, to provide significant speed improvements and design flexibility for a broad range of high-speed digital applications.

Hermetic package to minimize parasitic and cross-talk performance degradation.

Harris' HMD-11141-1 universal 4-bit Shift Register is housed in a hermetic package suitable for microstrip, stripline, and co-planar circuit design media. Features include:

- *1.4 GHz clock speed*
- *Shift right or shift left, parallel entry and hold operations*
- *Flatpack packaging provides optimum performance for GHz signal transmissions*
- *Reliable Ti/Pt/Au metallization system*

The Harris HMD-11016-1 Binary Counter divides by 2, 4 and 8, and supplies these three outputs simultaneously to facilitate bit-steering. Features include:

- *DC to 2.0 GHz input data rates*
- *Asynchronous master clear and clock enable*
- *50 ohm drive capability*
- *ECL and GaAs compatible*

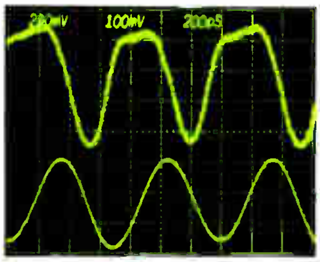
VERTICAL INTEGRATION— THE KEY TO HIGH VOLUME PRODUCTION AND RELIABILITY

Harris Microwave Semiconductor has refined Gallium Arsenide technology to accomplish production reliability goals in the finished product. The manufacture of its own Gallium Arsenide materials and substrates makes possible the rigorous control necessary for superior quality in these high complexity devices.

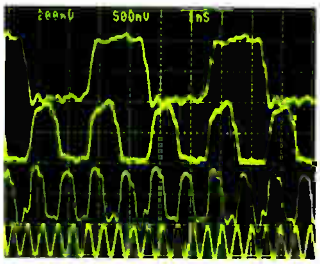
AND MORE TO COME

In the next few months, Harris Microwave Semiconductor will introduce a potent array of flipflops, diff amps, NAND, OR, NOR and Exclusive OR gates for data rates up to 4 GHz. More GaAs IC's for EW, computer, instrumentation, and high-speed data communications are soon to follow.

So, when speed is the issue in your designs, contact the people who are writing the Gallium Arsenide book at Harris Microwave Semiconductor, 1530 McCarthy Boulevard, Milpitas, CA 95035. Call (408) 262-2222, or TWX 910 338 2247.



High toggle rate HMD-11141-1 Shift Register showing clock (lower trace) and output functions.



HMD-11016-1 Binary Counter's 2, 4 & 8 synchronous division with 2.0 GHz input. (Input & output data attenuated for presentation purposes.)

Harris Microwave Semiconductor. ***To do it right, we start from scratch.***

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IF IT WEREN'T FOR UNIX WE NEVER COULD HAVE BUILT THE PYRAMIDS

Ordinary computers, yes. But not a Pyramid Technology 90x.

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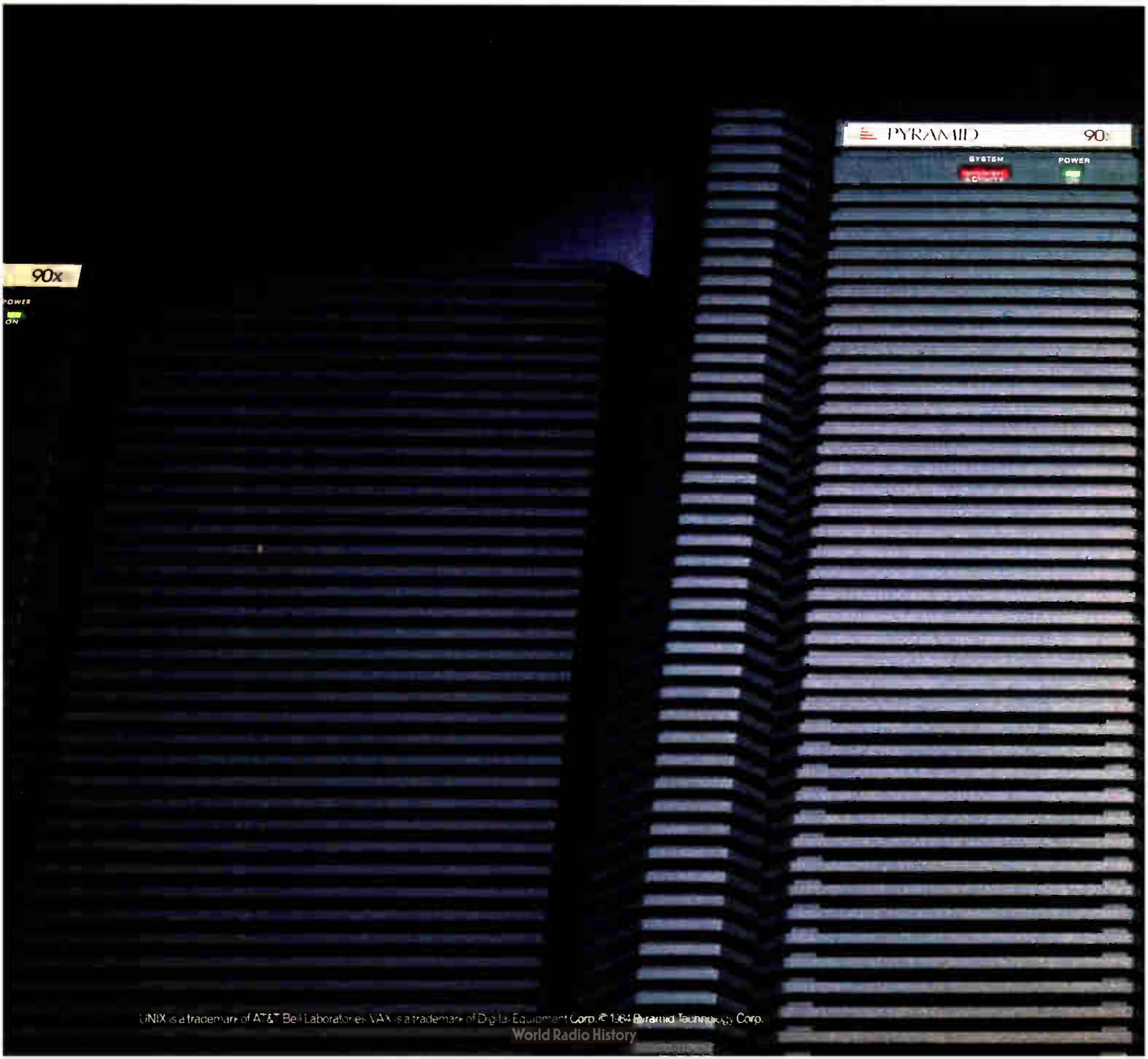
The secrets of this Pyramid are a thorough understanding of UNIX, a few fundamentals of RISC (Reduced Instruction Set Computer) theory, more registers than 30 VAXs, and a 32-bit proprietary architecture that outperforms a roomful of micros.

All combined to speed up UNIX just where it likes to slow down.

For example, gone are 85% of performance-robbing memory references. The endless parameter shuffling of yesterday's technology has been replaced with a hardware register win-



dow. Even context switching takes less than one percent of the CPU's time.

It's amazing what hardware architects can do, given the chance. It's almost as startling as what our software wizards did.

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We do admit to one feature not compatible with other UNIX systems. Our single-source support.

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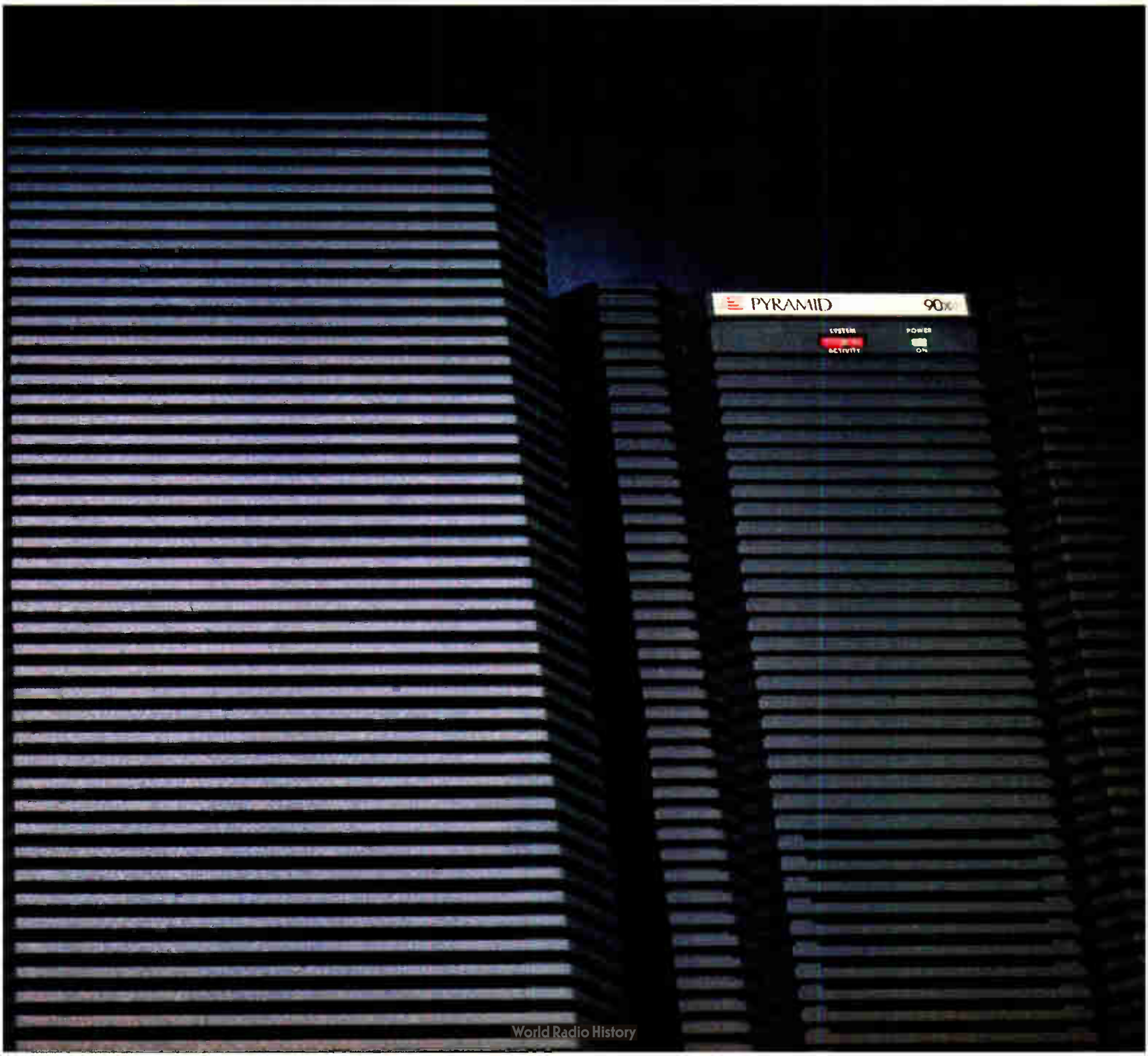
Because when it comes to running UNIX, a Pyramid looks good from any angle.

PYRAMID TECHNOLOGY



News update

Although units have yet to start rolling off the assembly line in volume, Storage Technology Corp., in Louisville, Colo., is still confident that its laser-based optical-storage subsystem and disk medium will generate revenues of $100 million during this first full year of sales. Last fall, STC officially tossed its 14-inch platter and 7600 subsystem into the optical-memory ring, aiming the $130,000 system at large minicomputers and mainframes [*Electronics,* Oct. 20, 1983, p. 101].

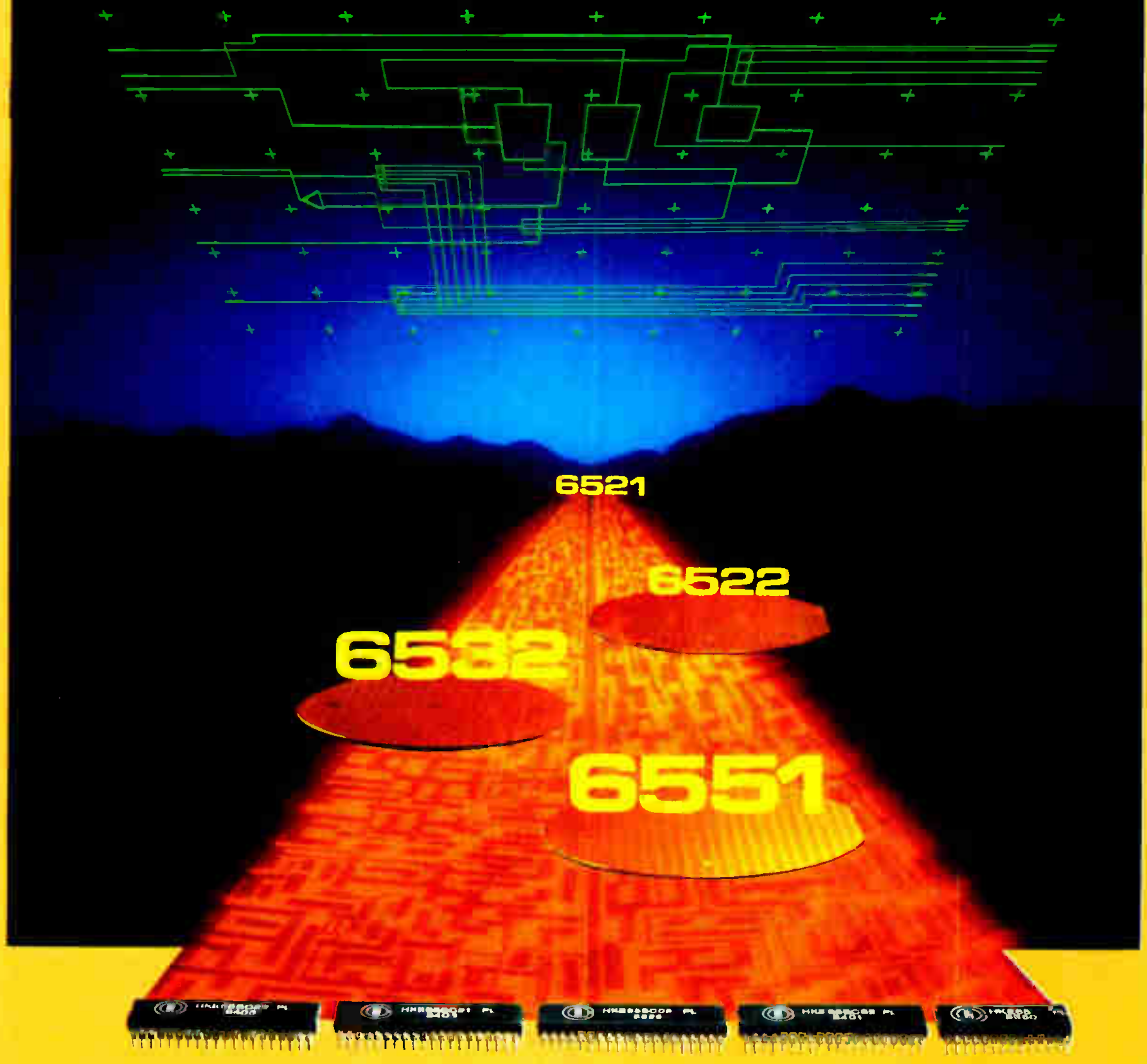
Today, much of the firm's health hinges on the success of the new technology, which can put 4 gigabytes of nonerasable data on one side of the disk. STC dropped a $75 million complementary-MOS mainframe project in January to give more attention to the 7600 and its delayed 8380 magnetic disk drive. Also dropped was the Virtual Storage System, a cache-memory controller. STC officials say they are counting on $1 billion worth of optical-storage sales over the next five years.

Sure of 1984. That $100 million 1984 sales goal is "in the bag," says a confident Ronald L. Brown, marketing manager for original-equipment manufacturers at STC's optical-storage plant, in Longmont, Colo. STC salesmen visiting big system-integration houses are striking deals at a rate three to four times higher than he first expected, he says.

STC has only one working beta-test site, at the National Center for Atmospheric Research, in nearby Boulder. There, the laser-storage unit logs weather data pouring in from a Cray supercomputer. The date for the beginning of volume shipments has slipped from the second quarter of this year to the second half. In fact, STC is not planning to deliver initial production units for engineering evaluation until this summer.

To increase the output of platters, STC is installing a high-volume materials coater in Longmont. This equipment—which puts thin films of recording material atop an aluminum substrate—is expected to boost third-quarter throughput to 450 platters an hour, as compared with fewer than 50 today. **–J. Robert Lineback**

CMOS 6502 MICROPROCESSOR THE HKE65SC02 FAMILY AND PERIPHERAL CHIPS



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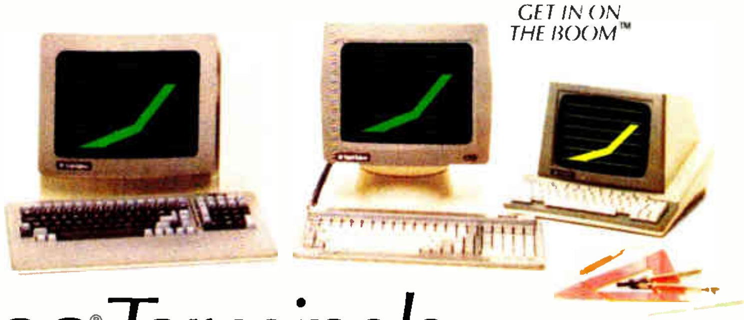

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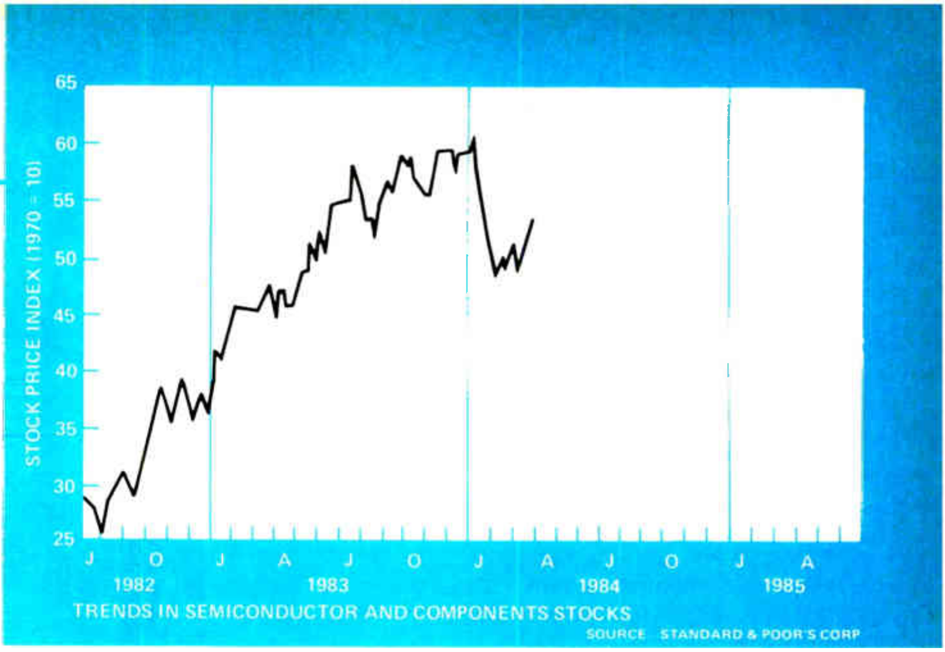
Business activity

"Trends in semiconductor and components stocks" records the stock market activity of a selected group of publicly owned semiconductor and component manufacturers. The index weights the companies by size and therefore reflects their relative performances.



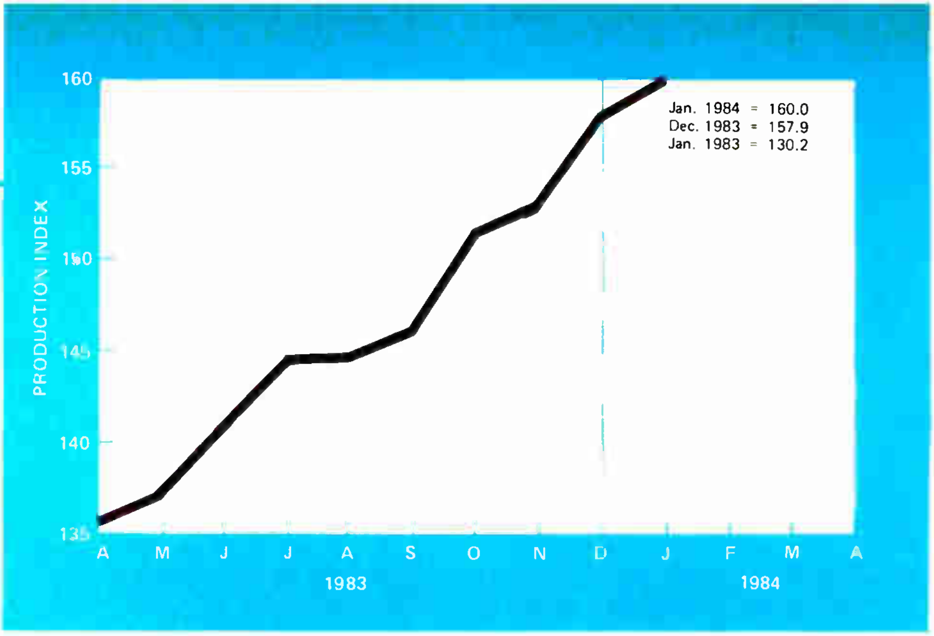
The largest real gains in 20 years for U. S. Government research and development funding is forecast for 1984 by the *National Science Foundation*, in Washington, D. C. The NSF projects 1984 Federal R&D funding will grow 18% (12% in real dollars), to $45.5 billion from 1983's $38.7 billion. Federal funding in 1983 was up 6% (2% real growth) from 1982's level of $36.4 billion, the NSF reports. Of 1984's funds, research will get 32% (14% for basic research and 18% for applied research) while development work will garner 68%. In 1983, research funding amounted to 37% of the total (16% for basic, 21% for applied), while development soaked up the remaining 63%. "The major factor in the growth of funds to industry—and in the 18% increase in total Federal R&D funds—is the growth planned for R&D programs of the Department of Defense," the NSF says. DOD plans to increase its R&D support by 29% to $29.7 billion in 1984, from 1983's $23.1 billion. Funding for mathematics and computer sciences will increase 21%, "by far the largest relative increase of any field," to $482 million, according to the NSF. The Defense Department "will provide increased applied research support to this field, especially in the computer sciences area," the study predicts.

Production of electronic equipment could soar by 20.4% this year, to $156.6 billion from 1983's $130.1 billion, as the strong U. S. economy, coupled with recoveries in Europe and the Far East, boosts demand for computers and instrument products, says market research firm *Henderson Ventures*, Los Altos, Calif. With strong performances by the equipment sector, "there will be heavy demand for electronic components," it notes. The firm sees a 33% gain in semiconductor purchases this year and a 24.2% rise in passive component buys. As growth in the U. S. economy slows, 1985 electronic equipment production will slow to 13.9% to $178.5 billion, it projects.

Company financings . . . *Cypress Semiconductor Corp.'s* second round of financing brought the San Jose, Calif., firm an additional $9.7 million in equity funding. . . . A first round of financing raised $3.5 million for *Syntelligence,* in Menlo Park, Calif., which is in the process of developing expert systems based on artificial-intelligence concepts for commercial applications. . . . Winchester-disk-drive maker *Vertex Peripherals Inc.,* in San Jose, secured $6.75 million in a third round of equity financing. **–Robert J. Kozma**

Business activity

The *Electronics* production index is a seasonally adjusted measure of the level of production activity among U. S. manufacturers of office and data-processing equipment, communications and radio-television equipment, instruments, and components. As a reference point, the 1977 yearly average = 100.



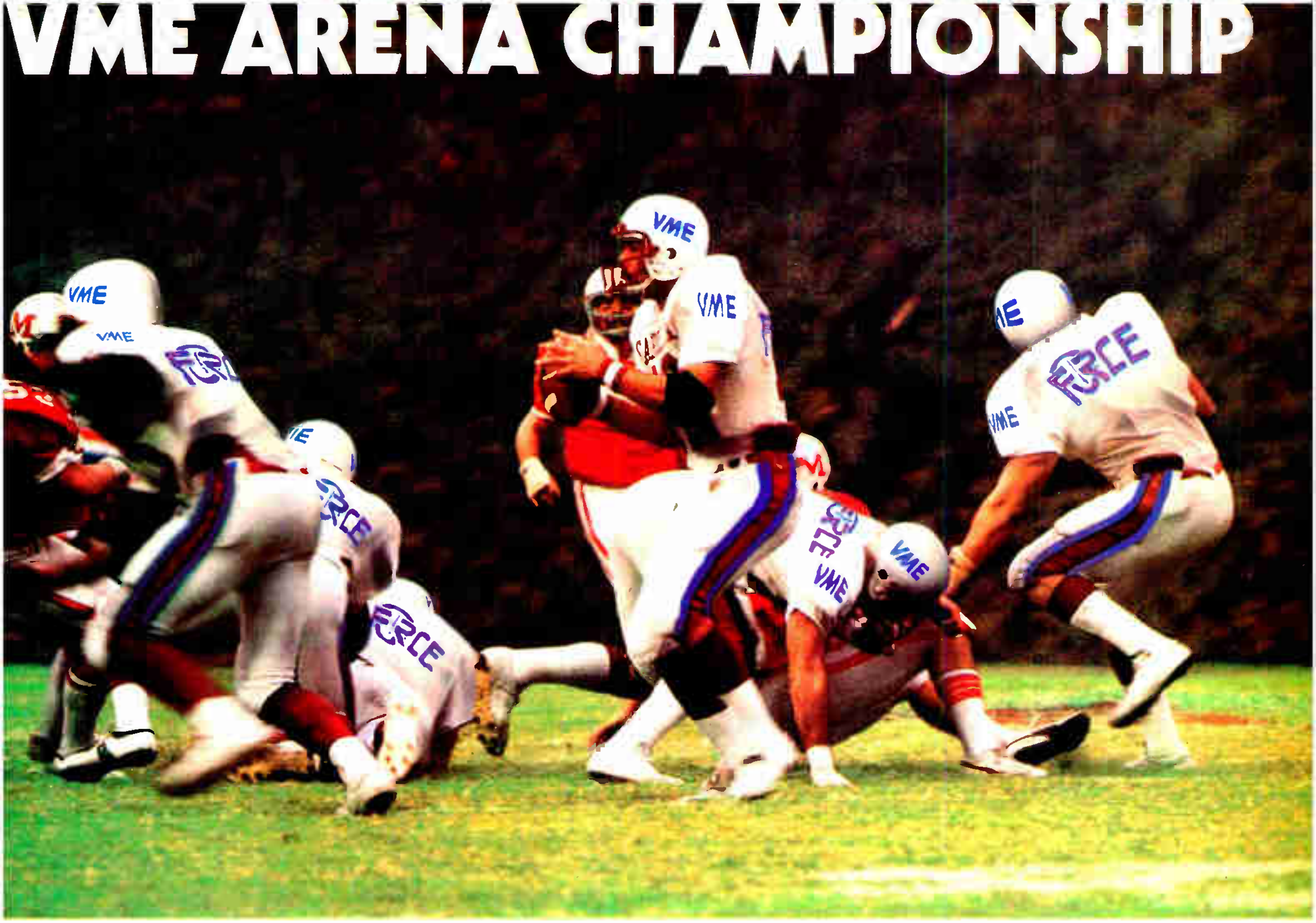
U S INDUSTRIAL PRODUCTION INDEX[1]	January 1984	December 1983	January 1983
Office and data-processing equipment	299.2	300.8	250.8
Communications equipment	193.1	186.6	172.0
Radio and TV equipment	112.3	110.0	79.9
Electronic and electrical instruments	168.9 (Feb. '84)	167.0 (Jan. '84)	153.4 (Feb. '83)
Components	416.4	401.0	318.8

U S ELECTRONICS ECONOMIC INDICATORS			
Production workers[2] (thousands)	January 1984	December 1983	January 1983
Office and computing machines	200.1	200.2	189.1
Communications equipment	271.3	269.5	261.4
Radio and TV receiving equipment	62.5	63.9	59.8
Components	388.4	384.2	317.1
Shipments[3] ($ billions)	January 1984	December 1983	January 1983
Communications equipment	4.603	4.910	3.733
Radio and TV receiving equipment	0.910	0.750	0.696
Electronic and electrical instruments	4.598	4.655	4.101
Components	3.290	3.218	2.609

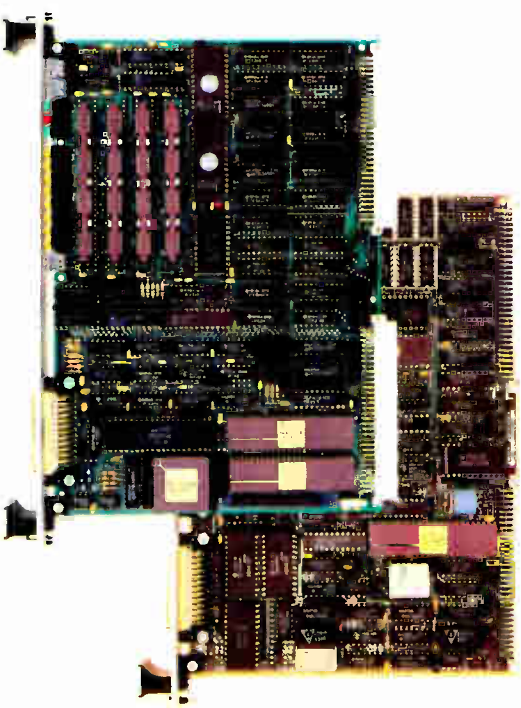
U S GENERAL ECONOMIC INDICATORS	February 1984	January 1984	February 1983
Index of leading economic indicators[4]	165.9	164.8	147.4
Budgeted outlays of the Federal government[5] ($ billions)	68.267	68.052	64.152
Budgeted outlays of the Department of Defense[5] ($ billions)	18.515	18.283	16.567
Operating rate of all industries[6] (% capacity)	80.2	79.4	70.5
Industrial-production index[1]	159.9	158.0	138.1
Total housing starts[3] (annual rate in thousands)	219.7	197.6	170.6

Sources:
[1] Federal Reserve Board (1967 = 100) [2] Bureau of Labor Statistics [3] Bureau of the Census [4] Department of Commerce (1967 = 100)
[5] Department of the Treasury [6] McGraw-Hill Publications Co., Department of Economics

VME ARENA CHAMPIONSHIP



IN THE VME ARENA FORCE PUTS MORE POINTS ON THE BOARD



OUR OFFENSIVE LINE: CPU-1, CPU-2, CPU-3* ALL VMEbus COMPATIBLE

128KB/512KB 68000 CPU-1 VMEbus Board
SYS68K/CPU-1

- On-board storage 128K/512K byte DRAM
- 128K bytes of EPROM
- 3 serial I/O ports plus 1 parallel I/O port
- Real time clock with battery back-up

256KB/1MB 68000 CPU-2 VMEbus Board
SYS68K/CPU-2

- Dual ported RAM 256K/1M byte
- 16K bytes of SRAM, 64K bytes of EPROM
- Floppy Disk Controller (5 1/4 ", SA 460)
- Multiprocessing, multimaster capability
- 1 serial multiprotocol plus 1 parallel port
- Real time clock and battery back-up capability

MMU-DMA 68000 CPU-3 VMEbus Board
SYS68K/CPU-3* (Preliminary Spec.)

- Memory Management Unit
- Direct Memory Access Controller
- 16K bytes of SRAM, 64K bytes of EPROM
- 4 level on-board bus arbiter
- Multiprotocol controller
- Real-time clock with battery back-up

Other FORCE products of the SYS68K VMEbus family:

- Analog I/O boards
- Dynamic RAM boards
- Static RAM boards
- Floppy/Winchester controller
- SASI Interface with DMA capability
- Multiprotocol serial I/O board
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Circle 37 on reader service card

THE CASE F

It measures 5.00"x 6.62"x 14.75". And it fits smartly beside many of today's popular microcomputers. But the case in point, Xebec's new 10-megabyte 9710 Universal Storage Subsystem, has more to do with the components inside—specifically, the controller and the disk drive—than with the dimensions and the aesthetics outside.

Actually, the most important thing on the outside of the case is the name. Xebec. A company whose 5.25" hard disk controllers are found in more business micros—including those of IBM, Hewlett Packard, TI and Eagle—than any other, anywhere. What put us there was—and remains—our ability to *engineer in* more features and *manufacture in* more quality—zero defect quality, delivered on time and in quantity.

What puts us here, in the subsystem business, is at once a derivative and encompassing quality issue. The fact is that the more sophisticated we make our controllers, the more obvious become the deficiencies of the disk drives they control—the very drives found in all of the subsystems for small business computers being sold today. And all the more obvious becomes the need for someone to create a new standard for bringing these critical components together.

The Xebec 9710 is that new standard. First, it houses the industry's best selling 5.25" hard disk controller, the Xebec S1410, with its patented architecture, state-of-the-art feature set and VLSI design. But the real key is the incorporation of a disk drive that is "quality matched" to that controller, not just "component compatible." A drive that goes through the most rigorous testing possible before it goes into a 9710.

The results are directed at the serious end users and system integrators of microcomputer mass storage. Superbly matched components that deliver unmatched performance and reliability, right down to a complete range of host adaptors—for the IBM PC, Apple IIe, S-100, Multibus and Q-bus—that give the Xebec 9710 its impressive "universatility."

And lest you think that our case for quality is made at the expense of other important considerations—like price and availability—consider this. The 9710 is founded on a commitment to the processes that optimize all of these factors—computer-aided design, manufacturing and test. A commitment most recently demonstrated by our $20 million investment in advanced robotics equipment.

The case we are making is not, then, an empty one—no high-minded cliché thrown into the promotional fray. It is solid and smart.

It is, bottom line, an open and shut case for quality.

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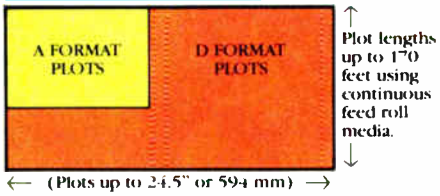
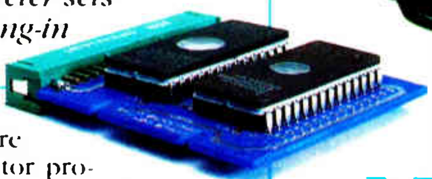


Now you can create virtually any size plots you want up to 24.5" wide, including ANSI sizes A-D and ISO sizes A4-A1, on cut sheet or roll media. Use standard bond paper, glossy bond, vellum, clear film or mylar.

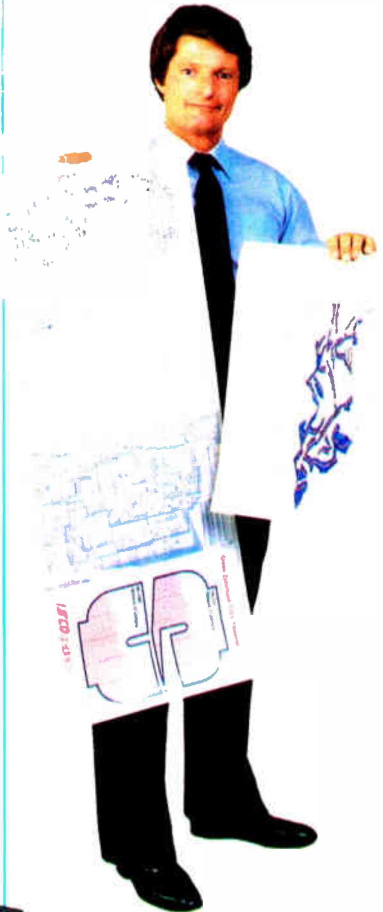
Run dozens of entirely different plots automatically thanks to a built-in microcomputer that can be pre-programmed to plot on roll media up to 170 feet. Then quickly switch to cut sheet plotting – great for your pre-printed forms. The ZETA 822 is the only plotter that can do both.

Best of all, we've got line quality and throughput at a price that makes us the cost-effective choice for just about anybody's plotter applications. You'll get vector independent speed of 25 ips. And 2 g acceleration insures the plotter reaches top speed fast. With resolution of one-one thousandth's of an inch.

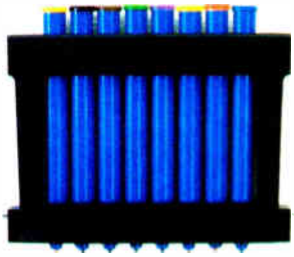
Change character sets just by plugging-in a ROM chip.



Our firmware character generator produces typeset quality lettering similar to the popular Helvetica font with user-controlled proportional spacing. Now you can add special character symbol sets for both engineering and architecture simply by plugging in a new ROM chip.



Eight color, carriage-mounted pens eliminate time-consuming pen changes.



Incredibly, some plotters still grind to a dead stop to change pens. Not ours. We put all eight pens on the carriage. You'll be amazed at what that does for plot throughput. And when you want to use our liquid ink option, just snap in our four-pen cartridge.

You have total user control over such variables as speed, pen pressure, acceleration and pen up/down delay times. Touch controls automatically adjust the ZETA 822 for perfect liquid ink plots.

Naturally, we support most computer protocols. And you can use the ZETA 822 on-line, off-line or remotely via RS 232C or IEEE 488 interfaces.

Call (415) 372-7568. Nicolet Computer Graphics Division, 777 Arnold Drive, Martinez, CA 94553 TWX 910-481-5951

Circle 40 on reader service card

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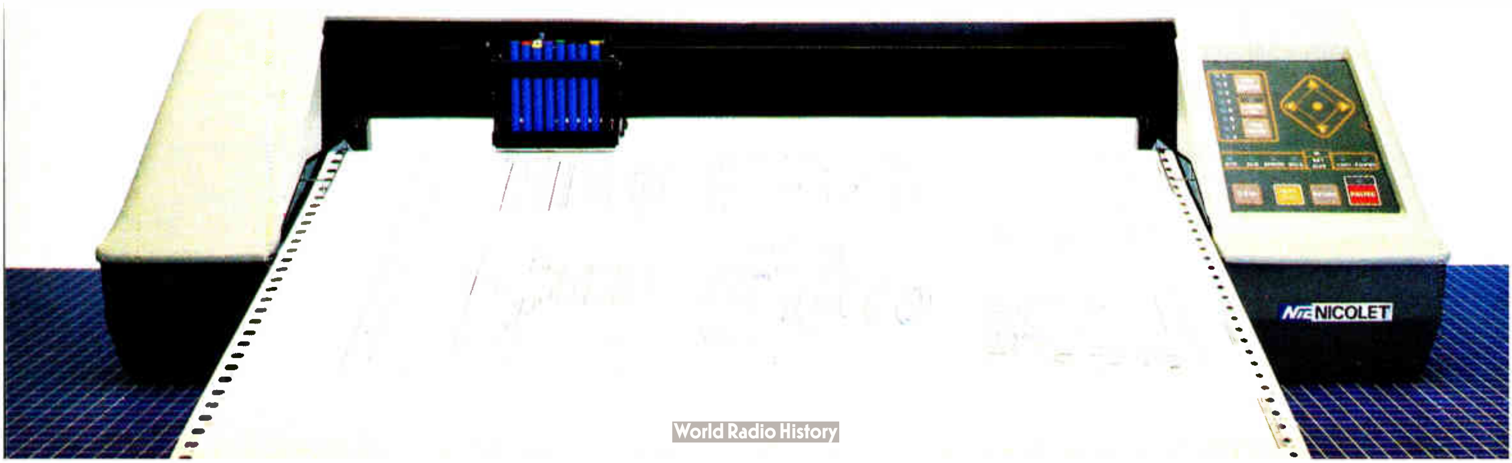


Plastic leads cause woes; IEEE panel investigates

The post-molded plastic leaded chip-carrier—a device many industry observers predicted would become as popular as the plastic dual in-line package—is having some teething problems. The package's compliant leads, usually made of copper or alloy 54, are turning out to be not so compliant after all, many users complain. **As a result, solder joints connecting leads to the pads of printed-circuit boards are cracking under mechanical flexing and thermal cycling.** This problem has spurred formation of a task force of the computer-packaging committee of the Institute of Electrical and Electronics Engineers (composed of representatives from Apple, DEC, IBM, AT&T, GTE, ITT, Hitachi, Amp, and Thomas & Betts). It will test leaded-chip-carrier samples from various manufacturers and report at the Oct. 28 meeting of the International Packaging Society in Baltimore. The upshot may be redesigns or use of different metals for leads.

CDC-Philips firm to make optical disk drives

A joint venture to bring optical disk drives to market has been formed by Control Data Corp., of Minneapolis, and Philips, of Eindhoven, the Netherlands. Optical Storage International will have its headquarters in Santa Clara, Calif., and will include the two development companies that CDC and Philips formed jointly in 1982—Optical Media Laboratory, in Eindhoven, and Optical Peripherals Laboratory, Colorado Springs, Colo. **Its first product, expected by year-end, will be a 12-in. 1-gigabyte cartridge and drive with a laser read-write mechanism.**

C-MOS PLA emulates bipolar circuits

Semi Processes Inc. has developed an electrically alterable complementary-MOS logic array with all the building blocks needed to emulate bipolar programmable array logic, which lets users set both AND and OR functions. **The C-MOS array is designed to be pin-for-pin compatible with the bipolar IC** and is programmed at 20 V. Its write time is 50 µs. To be able to erase connections without adding extra pins to what is usually a read- and write-only chip, the company made the circuit voltage-sensitive; when voltage goes over 8.5 V, all pins become inputs except V_{cc} and ground. The logic cell is implemented in a dual polysilicon double-diffused MOS technology, using a 100-Å oxide for the erase mechanism. Read time is 70 ns. The test circuit is an 8-input AND/OR gate; by the fourth quarter, the San Jose, Calif., firm expects to have a C-MOS version of the commercial 16L8 PLA.

Sperry puts mainframe on five C-MOS chips

A five-chip set that may be the first complementary-MOS implementation of a mainframe-class computer could show up in Sperry Corp. products next year. **The Micro 1100 chip set will provide performance in the range of Sperry's 1100/80 general-purpose mainframes.** With as many as 200,000 transistors to a chip, the ICs will be built with a process featuring 1.2-µm geometries and double-level metal. Other computer makers—including Digital Equipment, Data General, Hewlett-Packard, and NCR—are producing chip-set versions of superminicomputers and mainframes or plan to do so, but the other designs are typically done in a more power-hungry n-channel-MOS process. The chip set is now entering the prototype stage at the Eagan, Minn., Semiconductor Operations plant described on p. 54.

Electronics newsletter

Perq readies network operating system for engineering work stations

Pittsburgh's Perq Systems Corp. is attempting to strengthen its position against such front-running competitors as Apollo Computer Inc. and Sun Microsystems Inc. in the market for general-purpose engineering work stations. **Its weapon will be a network operating system that can provide totally transparent resource sharing on a network of up to 1,024 Perq work stations.** Known as Accent, the operating system was developed at Carnegie-Mellon University and will run on Perq hardware using an Ethernet-compatible network. Accent is compatible with AT&T Bell Laboratories' Unix operating system.

CCD camera from RCA uses frame transfer

Using a process it calls frame transfer, RCA Corp. has developed a $37,500 television camera using charge-coupled devices that it says offers vastly improved high-sensitivity, low-output capacity, while eliminating trailing smears on images of moving objects. The frame-transfer CCD **is immune to magnetic fields, and it eliminates acoustical interference and geometric distortion of the picture.** The camera's signal-to-noise ratio exceeds 62 dB—4 to 6 dB better than portable tube-based cameras.

NuBus accommodates 'private' connections

Hoping to encourage more system integrators to hop aboard its processor-independent 32-bit NuBus, Texas Instruments Inc. is developing **supplemental bus structures that allow private backplane buses to be easily bolted onto the back of card cages.** TI's Austin, Texas, Data Systems Group believes supplemental data pathways will be useful in tackling high-speed graphics-processing markets.

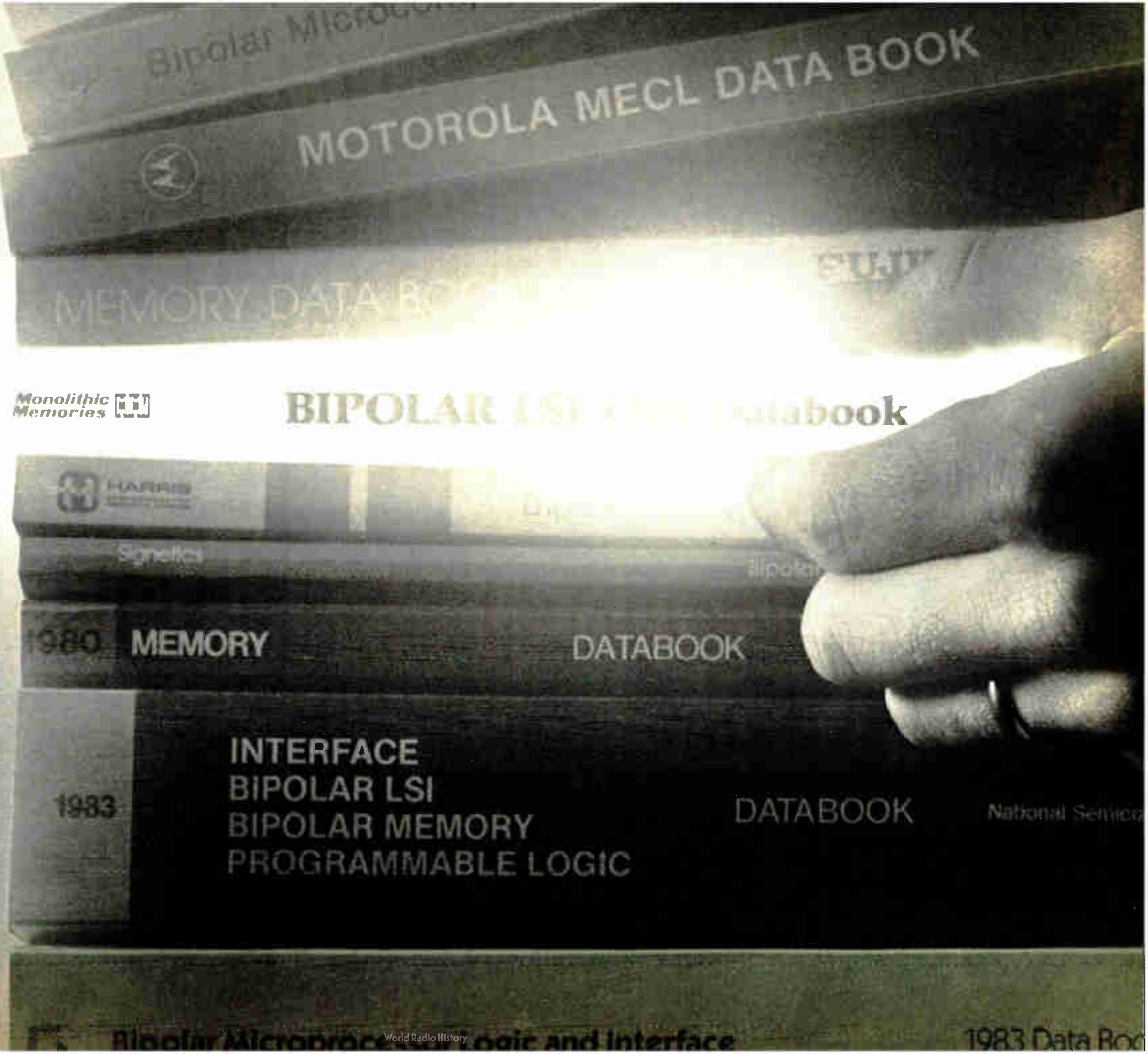
Sandia capacitors store five times more energy

Research into capacitor design at Sandia National Laboratories has led to components that can store 5 to 10 times more energy than components made with conventional technologies can. Researchers at the Albuquerque, N. M., labs discovered that **leaves of Mylar film with layers of a perfluorocarbon are a better dielectric than the traditional oil-impregnated paper.** The lab has produced long-lived capacitors with high energy density and reliability.

Addenda

Semiconductor Research Corp., the Triangle Park, N. C., microelectronics-research consortium, has given a three-year, $3.1 million contract to the University of California, Santa Barbara, **to develop very fast digital gallium arsenide ICs.** . . . Voice mail seems to be growing into a sound business. That's what officials at VMX Inc., of Richardson, Texas, are saying after the firm, which pioneered the electronic store-and-forward voice-messaging business three years ago, **reported its fourth consecutive increase in quarterly profits:** $1.4 million on revenues of $6.1 million in the quarter ended March 31, compared with a loss of $171,000 on sales of $2.1 million a year ago. . . . . Advanced Micro Devices Inc. has joined the list of semiconductor makers switching to complementary-MOS technology. **The Sunnyvale, Calif., firm is shipping its first C-MOS product,** a 4-K-by-4-bit static random-access memory, to one customer and will introduce six additional products this year.

Look up the leader



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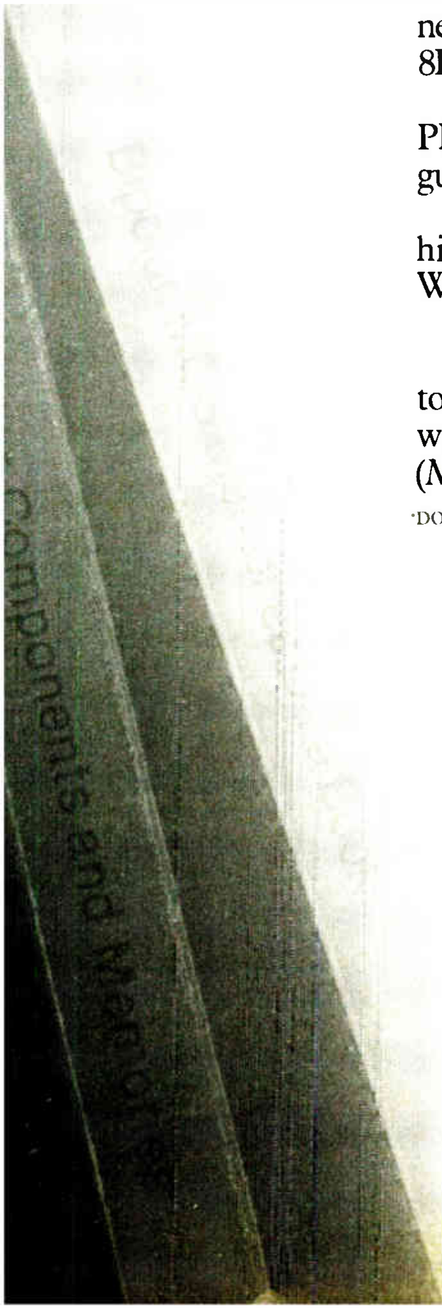
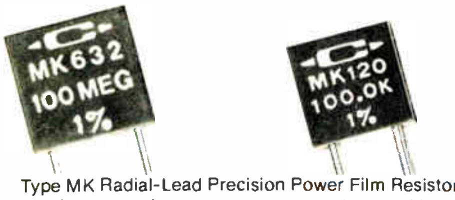


IdeaLogic. The big idea in system design.

Monolithic Memories MMI

Radial-Lead Precision Film Resistors from Caddock combine high values and tight tolerances with a choice of two high-power densities or three low TCs.



Type MK Radial-Lead Precision Power Film Resistors

MK 132 and MK 632
10 ohms to 100 Megohms

MK 120 and MK 620
30 ohms to 40 Megohms

Type TK Temp-Stable Precision Film Resistors

TK 121 and TK 621
1 Kohm to 2 Megohms

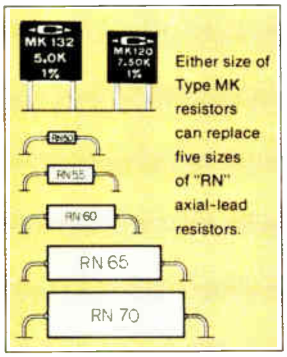
TK 133 and TK 633
1 Kohm to 10 Megohms

TK 139 and TK 639
1 Kohm to 10 Megohms

Type MK Radial-Lead Precision Power Film Resistors utilize Caddock's Micronox® resistance films to achieve high power density and an extended range of resistance values:

Available in two rectangular radial-lead packages that include values as high as 100 Megohms, these high-density film resistors permit electronic circuit designers to optimize packaging and PC board layouts with resistors that meet all these specifications:

	MK 120	MK 620	MK 132	MK 632
• Resistance Range	30 ohms to 2 Megohms	2.1 Megohms to 40 Megohms	10 ohms to 5 Megohms	5.1 Megohms to 100 Megohms
• Resistance Tolerance	±1.0% is standard, to ±0.1% on special order, depending on value and model.			
• Wattage	0.5 Watt	——	0.75 Watt	——
• Voltage	200 V	200 V	400 V	400 V
• Temperature Coefficient	50 PPM/°C	80 PPM/°C	50 PPM/°C	80 PPM/°C
	Temp Range: -15°C to +105°C, ref. +25°C.			
• Package Size	.250" square, .100" thick		.300" square, .100" thick	



These full-size photos comparing the Type MK resistors to "RN" style axial-lead resistors show that the largest Type MK, which is rated at 3/4 watt, requires less board space than the 1/20 watt "RN 50".

And within their voltage ratings, both sizes of Type MK resistors can replace five sizes of "RN" resistors, including the 1/2 watt "RN 70" which requires 10 times the board space of the MK 132 !

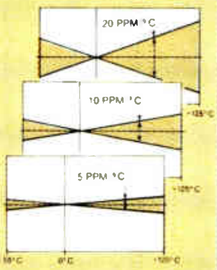
This combination of higher power rating and smaller size can also lower procurement costs by replacing many sizes of axial-lead resistors with Type MK resistors that have a 'standard' size and mounting dimensions.

Type TK Temp-Stable Precision Film Resistors with Caddock's Tetrinox® resistance films combine a choice of TCs of 5, 10 or 20 PPM/°C, a wide resistance range and tight tolerances.

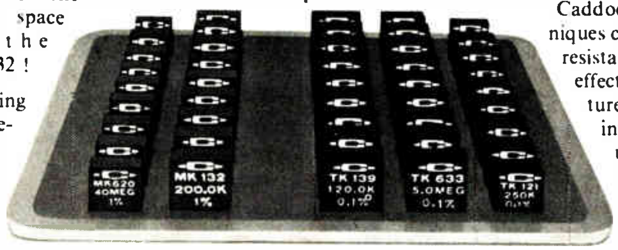
Type TK Temp-Stable Precision Film Resistors provide a combination of performance advantages that are unique in a miniature resistive component:

- **Three Standard Temperature Coefficients:** 5 PPM/°C, 10 PPM/°C or 20 PPM/°C over the temperature range from -55°C to +125°C. (+105°C max. for values above 500 Kohms or 1.5 Megohms, depending upon model.)
- **Resistance Range:** 1 Kohm to 10 Megohms.
- **Precision Tolerances:** ±1.0% is standard, and tolerances as close as ±0.05% are available on special order.
- **Load Life Stability:** 0.05% maximum ΔR after 2000 hours at full power at +125°C. (0.2% max. for values above 500 Kohms or 1.5 Megohms, depending upon model.)
- **Two Power Ratings:** .2 watt and .3 watt.

Each model of Type TK resistors has three TC options:



The Model TK 121, TK 133 and TK 139 precision film resistors have demonstrated performance which meets the requirements of Mil-R-55182/9 for thermal shock, moisture resistance, shock and vibration, dielectric withstanding voltage and low temperature operation.



Caddock's high-thru-put manufacturing techniques combined with our advanced Tetrinox® resistance film technology provide this cost-effective way to match the needs of temperature stable circuitry. For price and delivery information on both production and evaluation quantities, contact Caddock's main offices in Riverside, California.

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Circle 46 on reader service card

Dual-bus scheme opens door to processor flexibility

by J. Robert Lineback, Dallas bureau

Separate processor-to-memory paths make it possible to shift microprocessors' differences to a 'memory bus'

Today's increasing emphasis on software has forced systems integrators to think differently about hardware bus structures. No longer inspired solely by the popularity of any one processor type, many systems houses are trying to get more marketing mileage from buses and backplanes that can quickly accommodate a variety of microprocessor families.

Mixing a little of the old with the new, a Boulder, Colo., start-up believes that it has built such a host-independent vehicle by teaming the decade-old Q-bus with separate processor-to-memory pathways. Ford/Higgins Ltd. thinks this dual-bus approach, which it calls the interchangeable CPU architecture, can make it easier to add new central processing units by offloading many differences among separate microprocessors onto the added "memory bus."

The Q-bus then becomes a high-performance input/ouput highway that is used for peripherals to the system, notes C. Reed Ford, who is the fledgling company's cofounder and vice president for research and development.

The two-bus architecture also turns main memory boards into dual-ported storage, with one pathway taking processor fetches and instructions to random-access memory while the Q-bus handles direct-memory access from disk. "Using the Q-bus, we get a bandwidth of about 3.5 megabytes per second—which may be slow for the new higher-performance microprocessor. But as a peripheral I/O, it is very adequate," says Ford.

Packaged power. At first, Ford/Higgins will serve multiuser business computer markets with an expandable system called Powerframe, built around a standard Q-bus and a Digital Equipment Corp. PDP 11/23+ 16-bit processor. The cabinet also boasts 40 megabytes of hard-disk storage, an eight-slot chassis, main memory, and a 250-watt power supply. Introduced earlier this month at the DEXpo show, in Boston, the Powerframe 2340 costs $13,990 in single quantities with 256-K bytes of internal memory.

By summer, the firm will add a 16-bit-wide memory bus to the Powerframe so customers will be able to use a more powerful 68010-based CPU. The memory bus can handle a 12-megahertz 68010 processor with no wait states. Coupled with the Q-bus, the memory bus will raise performance levels close to those of a VAX-11/750, Ford predicts.

Later in 1984, a similar scheme will offer CPU boards based on National Semiconductor Corp.'s 16000 microprocessors. Ford/Higgins says it will probably expand the processor-memory link to support full 32-bit microprocessors.

"We have designed a machine and concept that expands in two different dimensions," says president J. David Higgins, who founded the company with Ford last fall. "It expands in the peripheral dimension, so customers can start out with very low-cost devices and build up a more expensive system. They also can start out with a processor and switch to another when the software needs change."

The variable architecture derives from Higgins' belief that thousands of businessmen, made aware of software's importance by their personal computers, are now shopping for multiuser systems. The trick, says Higgins, is to reach these potential customers as quickly as possible with a software-oriented hardware product. "There is a need for new high technologies, but I be-

Card trick. Adding a memory bus to the Q-bus-only congfiguration held by David Higgins lets it use a 68000 microprocessor as well as other processor families.

lieve we represent the new-breed companies that take high-quality technology already existing in the marketplace and solve new problems with it," he adds.

Software

'Bus' tracks down mix of codes

Hunter & Ready Inc., a firm that provides real-time operating systems for embedded systems, has developed a method by which software components—not subroutines, but modules that perform specific operating chores—can be stored independently of the application software and called by programs that have no information about their addresses. That means components can be written in any high-level language, on any development system, and still run together in the final system.

Writing software in stand-alone modules is a useful way of providing functionality when it is needed by application programs. Until now, however, the calling programs needed some knowledge about where the modules were located in memory; this requirement meant that the different sections of code had to be assembled or compiled and linked together. That is part of the task performed by development systems.

In the Hunter & Ready scheme, the components are called by a convention that the Palo Alto, Calif., firm likens to a "software bus" because the software modules "plug into" it much as a memory board plugs into, say, a Multibus slot. This bus is actually a component vector table that provides a run-time linkage to each component. The table is accessed through a software trap built into the host microprocessor.

A better trap. Every microprocessor architecture includes a series of instructions that allow a program to interrupt processing much as a hardware device would. The Motorola 68000, for example, has 16 trap instructions, while the Intel iAPX family defines a series of INT (for interrupt) instructions. Hunter & Ready uses one of these instructions to interrupt the processor, which passes the request for a particular component on to the component vector table.

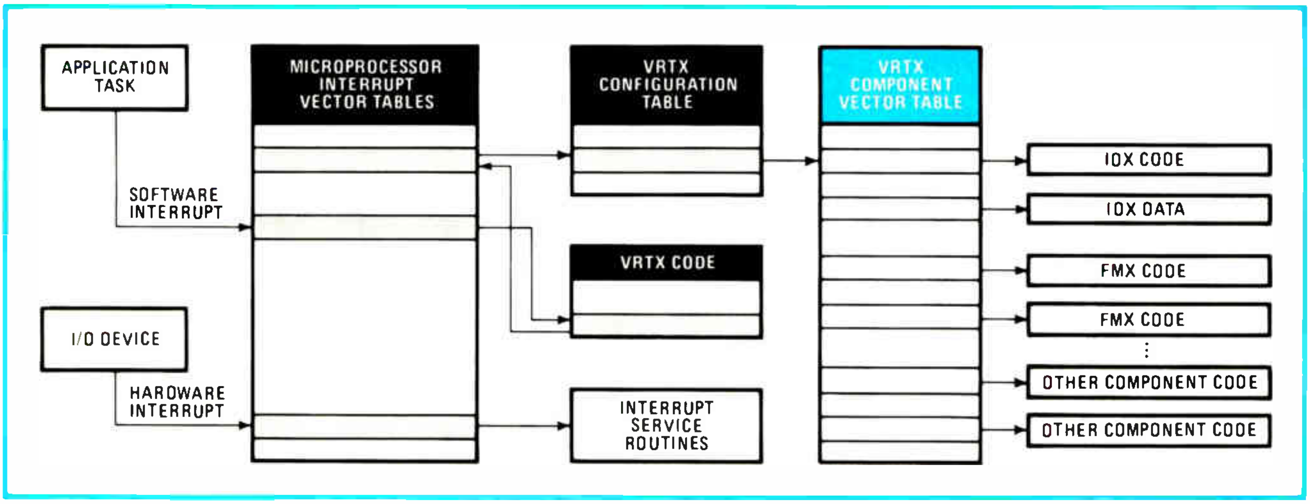
The software bus relieves users of some of the messy details of software integration. "Traditional software makes tons of assumptions about memory location and file structure," says the firm's vice president, James F. Ready. "Most people don't pay any attention to them until they find themselves locked into a particular development system."

In a development-system environment, Ready says, it is not necessary to write position-independent code, because the system has its own linkers and locators. The linker incorporates a software module called by the application program into that program after finding the module in a library; the locator then maps the entire combined program into the address space of the target machine, producing what is called an absolute object module, which can be executed. The called software module now has a specific address, and the calling program knows where it is.

Furthermore, the software bus makes it possible to use position-independent modules without the development-system environment. This is where the increased freedom comes in: users can develop their application programs in any language on any machine—a VAX, for instance—and can call the modules by the software bus: they do not need to worry about code's compatibility with a development system's linker and locator.

Ready concedes that the new calling convention entails some system overhead in passing the pointers from the microprocessor vector table to the component vector table. However, he says, if a call is worth making, it is certainly worth the half dozen extra memory fetches involved.

Hunter & Ready's first two components written for the new convention are an input/output manager and a file manager for its VRTX real-time operating system. The system



Soft bus. A calling convention executes only VRTX system calls, sending others to the proper software component. Vector in processor's vector interrupt table addresses VRTX configuration table, where an entry points to the component vector table, or "memory bus."

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leaves room for 128 components from Hunter & Ready and 128 user-written components, all of which can be accessed through the same processor software trap. –Clifford Barney

Polyglot compilers speak in 6 tongues

To upgrade programmer productivity in a significant way, a small New England software firm has spawned a family of six high-level-language compilers that can run on any computer using the Motorola MC68000 processor and AT&T Bell Laboratories' Unix operating system. The compilers sport a feature that is likely to catch eyes in programming circles: in any program, each compiler can mix routines written in the different languages.

"It means a programmer is no longer restricted to a single language for writing applications," explains Anthony Goschalk, director of product marketing at Language Processors Inc., Waltham, Mass. The firm introduced the compilers earlier this month, at Comdex/Winter. A number of large computer manufacturers—among them Wang Laboratories, NCR Corp., and AT&T—have already bought some examples of the compiler family and are testing them in the field, says Goschalk.

Shortcuts. The polyglot capability might, say, be used by a programmer working with Pascal who needed to manage data files, said to be one of the weaker aspects of the language. Data management could be written in Cobol and then integrated into the Pascal program, and so could parts of any existing program in the six languages: Pascal, Cobol, RPG-II, C, PL/1, and Basic. PL/1 will be available this summer, Basic, later; the rest are available now.

The company says its compiler array provides a two-year head start over any rival software developer that might wish to create a similar product. A new compiler usually requires hundreds of bytes of computer code and thousands of programming hours. Language Processors shortened the course with a five-part compiler architecture, four parts of which—the optimizer, code generator, run-time library, and source-level debugger—are identical for all the languages.

The only component that changes is the front end, which has the command structure and the syntax for particular languages. Even here, about one third of the command structure and syntax is common to all the compilers. The firm notes that its six languages are true compilers, so they get higher performance than interpreters do. For example, the company says benchmark tests show that a Cobol program runs 10 times faster on the Language Processors compiler than on a well-known interpreter. Supporting the polyglot feature is a high-level multilanguage debugger that works in whatever language the programmer employs and is therefore easier to use than a symbolic debugger, which operates on the assembly-language level.

Computer manufacturers are the initial market for the compilers, priced at $50,000 plus royalties for the first language and $25,000 for each additional one. Software developers are being approached, too, says Goschalk. –Larry Waller

Solid state

Honeywell seeking to strike it rich by selling wide-open GaAs wafer spaces

Down in Richardson, Texas, Honeywell Inc.'s Frederick J. Strieter and Wallace Shaunfield have pieces of valuable real estate selling for $15,000, $25,000, and $35,000. It is not basin land with oil-producing potential but space on 3-inch wafers of processed gallium arsenide.

Property rights. Honeywell's Frederick J. Strieter with a 3-inch gallium arsenide wafer like those on which space may be bought in the multiproject test-chip program.

The real-estate—dubbed the "multiproject test chip" by Honeywell—is an effort to promote GaAs technology. The project spreads the cost of materials and processing among a number of different customers who share the same wafer, explains Strieter, director of materials development and fabrication at Honeywell's Optoelectronics division. This year, the Minneapolis-based company will move the production of GaAs integrated circuits to Richardson, where it has begun to construct a new 3-in.-wafer front-end facility.

Customers give Honeywell the tapes of computer-generated designs; the circuits are then placed in standard square die areas measuring 50, 100, or 150 mils on a side. Ten dice, costing $15,000, $25,000, or $35,000, will be delivered. Processing one lot of wafers costs about $100,000—an expense that may be too high for most prototype work. Silicon would cost a tenth of that sum.

Cost sharing. "One of the problems in this early stage of GaAs development is the high cost of materials. Another is processing with the use of direct steppers for mask making," Strieter says. "So we are saying if we place a number of circuit designs on the same set of masks, customers will only have to pay a portion of the overhead."

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used to cut research costs at universities and laboratories. Honeywell believes that the concept is now the right way to encourage commercial and military use of GaAs.

Tektronix Inc. agrees that the time is right for small-volume deliveries of GaAs prototypes. To serve that need, the Beaverton, Ore., firm is offering a GaAs foundry service [*Electronics*, Feb. 9, p. 50].

Tektronix is not offering multiproject wafers. Instead, it is accepting orders for as few as eight wafers a year—all eight for less than $100,000, says Al Patz, general manager of the GaAs IC business unit. A minimum run is four wafers. Tektronix is converting its 2-in. wafer line to 3-in.

CAD is lacking. The need for experimental GaAs circuits is partly due to the lack of computer-aided-design tools and well-established design rules, says Shaunfield, Honeywell's deputy manager of GaAs efforts. Among other projects, the company has a contract from the Defense Advanced Research Projects Agency to establish GaAs foundries with Rockwell International [*Electronics*, Feb. 23, p. 41].

By this month, Honeywell was scheduled to deliver the first test chips. Four more runs are scheduled in Minneapolis, but production will be moved to Richardson by early 1985, says Strieter.

Using ion implantation to produce 1-micrometer geometries, the firm's metal-semiconductor GaAs field-effect-transistor technology yields circuits with a typical power dissipation of 3 to 10 milliwatts per gate and speeds of 100 to 250 picoseconds. The wafers carry digital chips [*Electronics*, April 5, p. 164] and analog circuits. –**J. Robert Lineback**

RCA will not drop video-disk research

RCA Corp. has finally gotten out of the consumer end of the video-disk business, but it is not ending its work in the field. The company will continue to undertake research into different technologies and applications for interactive home and institutional video systems, including full-motion video, graphics, and text displays.

"The general work is going to be broadened to look at storage devices for wider applications, such as teletext, videotex, home computers, and interactive computer storage," says Roy Pollack, executive vice president in charge of RCA's laboratories and assorted electronics divisions. "We will come back [with the video disk] in a broader application from a 1984 perspective."

That broader application must surely include the commercial and industrial markets. "RCA has done some very impressive work in their labs on laser-disk technology with tremendous storage capabilities," notes Mark Hassenberg, a securities analyst with Donaldson, Lufkin & Jenrette Securities Corp., in New York. "There are substantial opportunities [for the technology] on the commercial side." Charles K. Ryan, a research analyst with Merrill Lynch, Pierce, Fenner and Smith Inc., New York, believes that the potential size of the industrial and commercial markets can save RCA's video-disk efforts.

RCA's rivals were mostly noncommittal. NAP Consumer Electronics Corp., of Knoxville, Tenn., a North American Philips company that makes the Magnavox line of optical video-disk players, declined comment. Executives of another company that makes a video-disk product, Pioneer Video Inc., in Montvale, N. J., were not available. However, Hitachi Ltd., which makes a capacitance-electronic-disk (CED) player similar to RCA's, as well as a laser player, is planning a conservative approach to marketing its players to the consumer market. Says a spokesman: "We will meet the consumer's demand." And CBS/Fox Video, which manufactures CED disks, says, "We are still very much in the marketplace." –**R. J. K.**

Companies

VideoDisc dead, RCA eyes new areas

Hopeful after ending production and marketing of its VideoDisc players—and taking a $500 million bath—RCA Corp. says it will now turn its attention to new and unexplored segments of its businesses, including computers, peripherals, software, and services. RCA is also continuing research into different video-disk technologies.

True, by dropping the video-disk player, the electronics and communications giant was able to write off $175 million. "We took the VideoDisc decision with obvious disappointment in the face of continuing losses and narrowing prospects that the business would turn profitable," explains RCA chairman Thornton F. Bradshaw. The company will continue to turn out disks, however.

"Our mistake was we were late" in bringing the system to market, says executive vice president Roy Pollack. If the company had come out with the product five years earlier (the VideoDisc was introduced in May 1981), "it would have been a huge success. If we came out with it three years earlier, it would have been a good success," Pollack says.

In the end, what killed VideoDisc was another darling of the home-electronics marketplace, the videocassette recorder. Bradshaw says that to succeed, RCA had to expand the available market, get other companies to participate in it, invest heavily to get manufacturing costs down, and rapidly build its own software label and distribution.

But the rapid advance of the VCR smothered all that. Prices for VCRs, which, unlike the play-only VideoDisc, can record, fell faster than anyone expected, leading to phenomenal sales growth. (Bradshaw estimates 7 million will be sold in the U. S. this year, bringing the installed base to 20 million by 1985.) In addition, the move to cassette rental, rather than purchase, further spurred the VCR market, as did a decision by movie studios to get into the business.

The success of the VCR, in turn, kept other companies out of the vid-

eo-disk business. This left RCA to fight the battle against VCRs—as well as against the Philips-Pioneer laser-disk player—virtually unaided.

"While we were making progress, the window of opportunity was closing," Bradshaw says. RCA, which has sold about 550,000 VideoDisc players, was facing a further pretax loss of $100 million this year. "The product was a technological success," he adds, "but a commercial failure." Still, RCA is continuing research in the field (see "RCA will not drop video-disk research," p. 52).

Lighter and richer. Having cut loose the VideoDisc anchor, and about to pocket $1.5 billion from the sale of its C. I. T. Financial Corp. subsidiary, RCA wants to sharpen the focus of its corporate efforts on the home-video and business- and government-information markets.

Although RCA sees its efforts in the home-video market centering on the receiver, Bradshaw says this market also includes "software development, entertainment, production, information systems, servicing, transmission and receiving equipment, teletext and videotex, broadcast, cable, satellite transmission, and a number of other things." Many of these businesses provide a good fit with RCA's National Broadcasting Co.

Nor does Bradshaw rule out a move into the home-computer business. "Some form of home processing, storage, and communication system—whatever it is called—would be a rational addition to the marketing, manufacturing and service experience of RCA," he says. Pollack says the company could offer for sale under its label a home computer made by a third party. —**Robert J. Kozma**

Manufacturing

Sperry IC plant floats on concrete and air bags to prevent vibrations

By housing wafer-stepping equipment and other critical research and production gear on a concrete slab that floats on a cushion of air bags, Sperry Corp. has isolated critical fine-line semiconductor fabrication equipment from vibration in its new 240,000-square-foot plant in Eagan, Minn. Nonetheless, the design has raised some eyebrows, even in California's tremor-prone Silicon Valley.

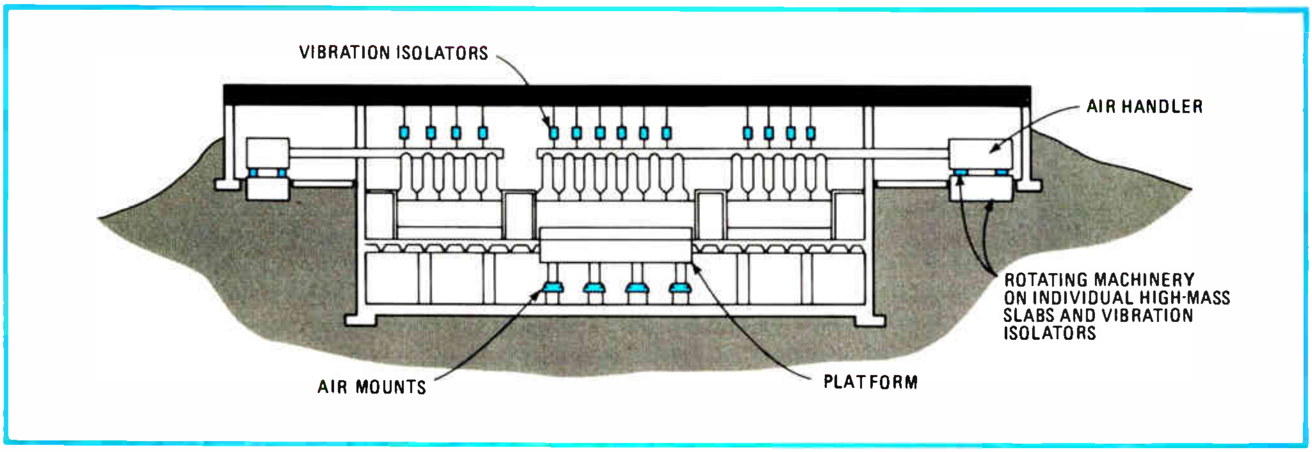
The 11,000-ft^2 platform weighs 3 million pounds. The firm expects it to reduce floor vibration to less than 0.005 mil of movement across a range of 5 to 100 hertz, says Ralph L. Kerler, director of resource management for Sperry's Semiconductor Operations. That compares to 0.010 to 0.020 mil on the grounds surrounding the plant and 0.050 mil typical in an office building when someone walks across the floor, notes Kerler. "We're satisfied that this is the lowest-vibration platform in the industry today," he boasts.

Separated from surrounding laboratory areas by conventional vibration-isolation building joints, the platform is supported by 64 rectangular 2-by-5-foot pillars, each of which rests on an inner-tube–like rubber air bag inflated to 140 pounds a square inch (see figure). A mechanical level-arm system on each pillar regulates height, causing air to be pumped into the bag or bled.

Supplied by Firestone Tire & Rubber Co., Akron, Ohio, the bags—known as air mounts—were actually developed for use in trains, trucks, and other heavy vehicles, says Donald E. Baxa, an associate professor of engineering mechanics at the University of Wisconsin, Madison, and designer of the Sperry system. They sell for $700 to $800 each.

Some questions. The Sperry design elicits skepticism among some in the semiconductor industry. "It's a huge step. It's tough to imagine anybody floating a whole damn fab line on air mounts," notes one plant construction official at National Semiconductor Corp., Santa Clara, Calif. "I can't help but think it will cause more problems than it will solve."

A similar sentiment comes from Ronald P. Robinson, manager of plant engineering at Burrough Corp.'s semiconductor facility in



Floating on air. Sperry's new semiconductor plant is designed to be isolated from vibrations much less than those caused by a person walking across an office floor. The key to the system is the air mounts, which inflate and deflate as needed.

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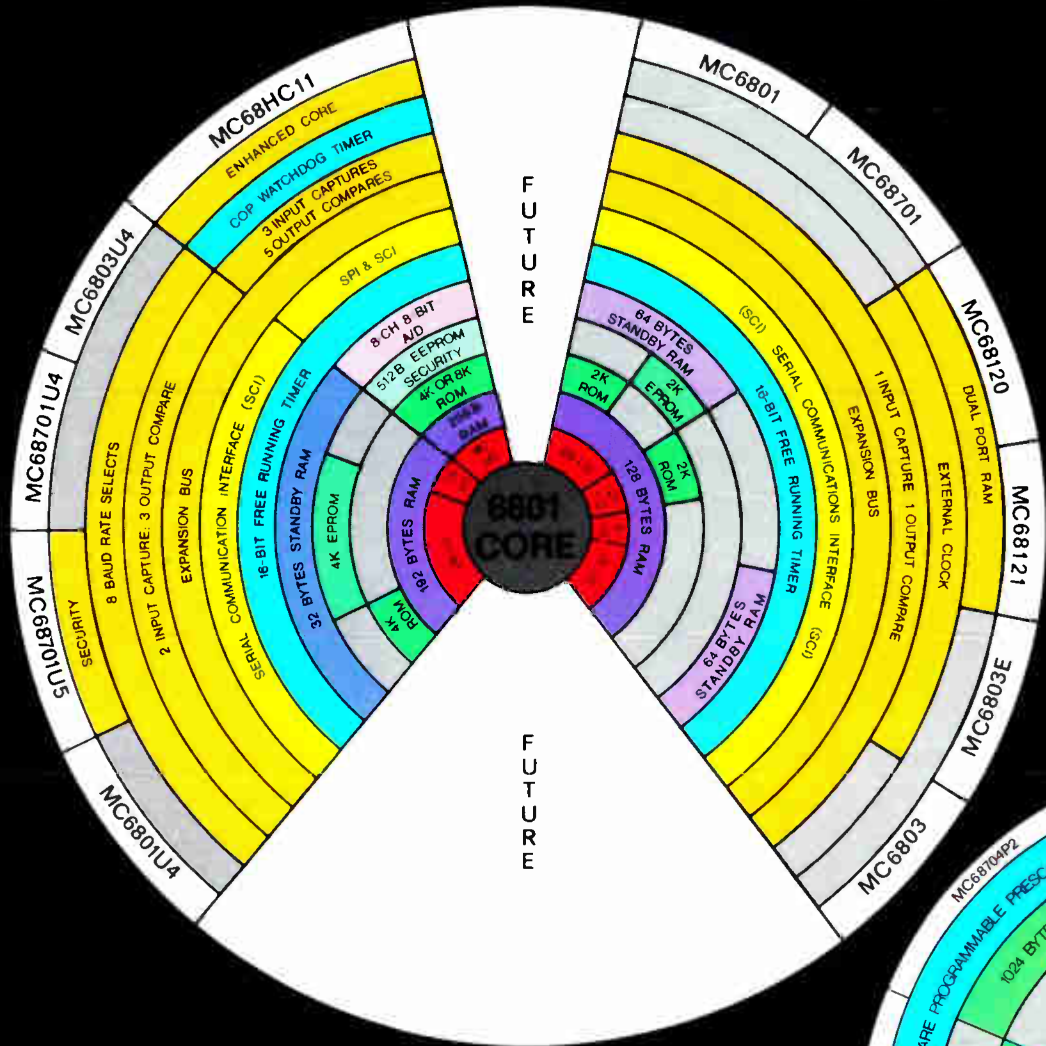

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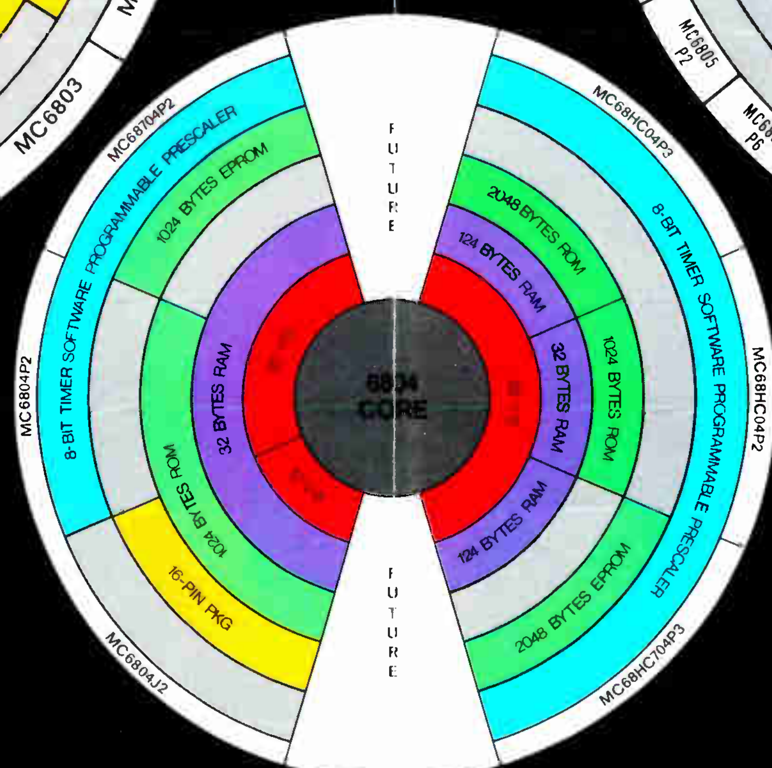

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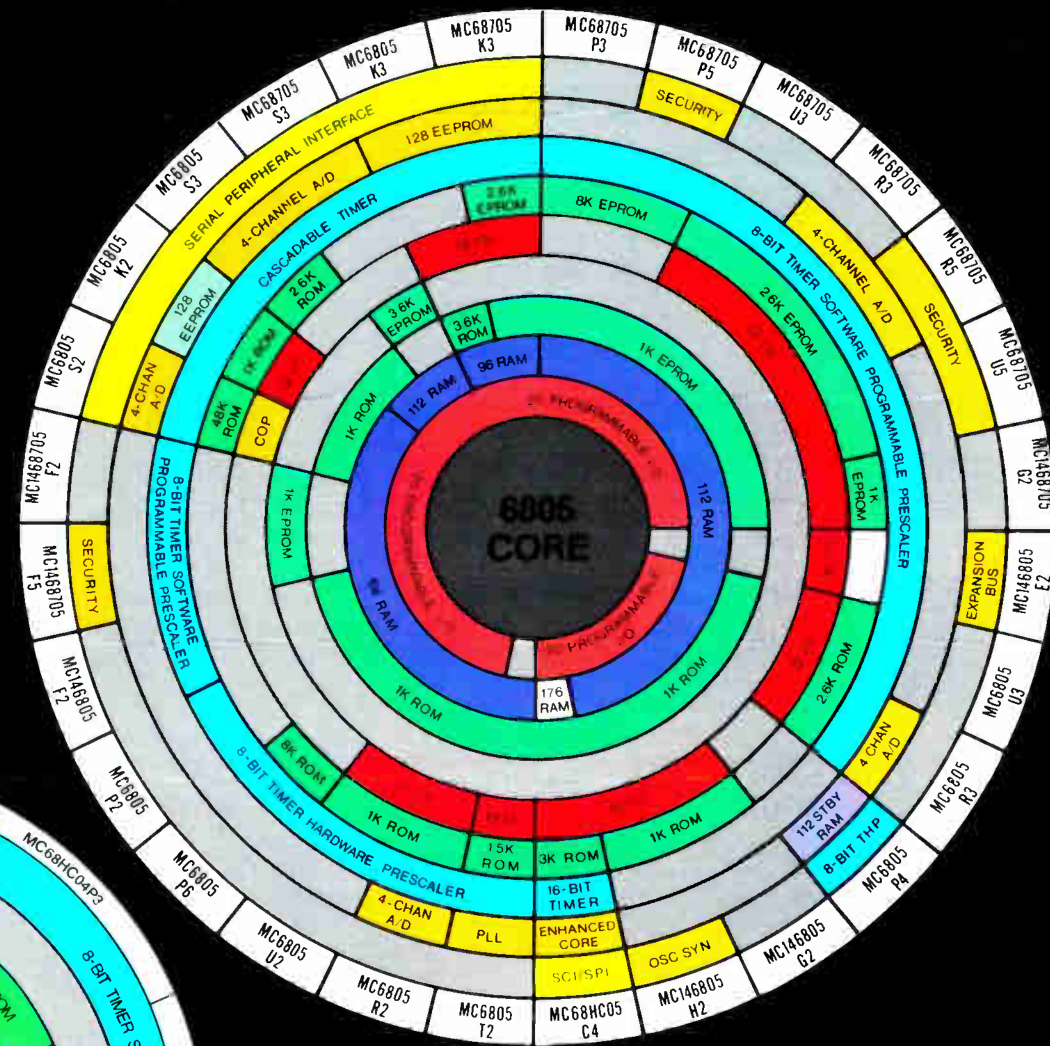

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SCI = Serial Communication Interface
SPI = Serial Peripheral Interface

STBY = Standby
THP = Timer Hardware Prescaler

HMOS = MC68XXX
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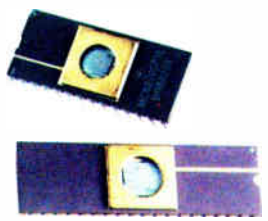

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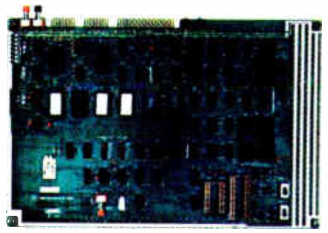

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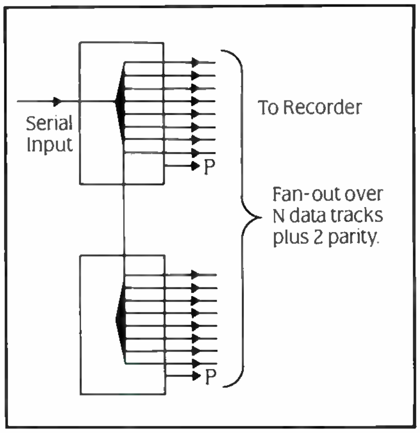

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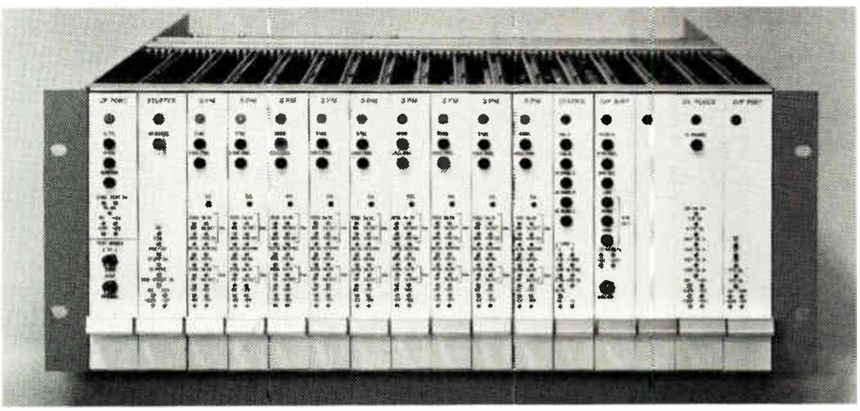

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Rancho Bernardo, Calif. "It sounds as though they've really gone exotic. I'm surprised they could justify something this elaborate," he says.

Like others, Robinson believes that conventional industry practices, such as putting air handlers and other vibration-generating equipment in separate areas or on isolated concrete slabs set in the ground, will be sufficient for vibration isolation. Lithographic systems and other critical gear come equipped with spring or pneumatic self-isolation systems.

Sperry's Kerler concedes that using the floating slab to control vibration is probably not a necessity for the firm's current work. Prototyping efforts are currently under way on chips with minimum feature sizes of 1.2 micrometers for MOS ICs and 1.5 μm for bipolar parts. But Kerler points out that the year-old plant was designed "to support us throughout the 1980s." Successive generations of chips will reach submicrometer geometries, for which better vibration isolation may be necessary.

Kerler maintains the floating platform "is not an exotic system." In fact, he observes, "most people who have seen it have been fascinated by the simplicity of what has been done." Though he cannot provide figures, he says that the platform did not significantly increase the cost of the plant, about $30 million, plus $31 million for specialized processing equipment. –**Wesley R. Iversen**

Military

Pentagon shopping for walking vehicle

Not to be outdone by Hollywood, the Pentagon's Defense Advanced Research Projects Agency has started qualifying potential contractors for a "Star Wars" robot vehicle. Darpa's version of the film's Scout Walker, which the agency calls the autonomous land vehicle, will clomp around battlefields on legs, guided by a vision system and a supercomputer to help it distinguish among objects cluttering its path.

This is just one of three systems under development in the agency's four-year, $600 million Strategic Computing Program, intended to put artificial intelligence into military equipment. The second, a pilot's associate, is to help identify incoming hostile targets or aircraft malfunctions and disclose them in a synthesized voice. The third item is a supersophisticated command-control-and-communications (C^3) battlefield-management system that will use AI technology to predict battle scenarios and suggest countermeasures.

By combining the results of advanced work in microelectronics, very high-speed supercomputers using parallel architectures, and AI, Darpa intends to produce prototype machines with intelligent functions that can be mixed and matched for the desired application. Major work will be in understanding natural language, signal interpretation, knowledge and data management, and simulation-modeling-control.

Teaming up. Equally novel is the way Darpa wants to do business with the program's contractors. Bidders are being asked to form university-industry teams, all of whose members—prime contractors, subcontractors, and universities—will have to deliver their work to suit project product schedules. One Defense Department insider says that Darpa will use the same techniques it has tried out in the Very High-Speed Integrated-Circuits (VHSIC) Program, where it set up information networks.

The team approach is meant to foster intimacy between universities and industry—"the right attitude," says R. David Lowry, manager of marketing development at Denver-based Denelcor Inc., the manufacturer of HEP-1 supercomputers [*Electronics,* Oct. 6, 1983, p. 125]. Denelcor is working with a major contractor and a university to develop its autonomous-land-vehicle proposal.

Others feel less sure about Darpa's approach. Cray Research Inc., in Minneapolis, and ETA Systems Inc. (the St. Paul supercomputer builder spun off from Control Data Corp.) want to participate, but both are waiting for the agency to clarify its focus. Cray spokesman Brett Berlin, vice president for government relations, says his company is trying to figure out "how to assist the national effort without cramping our own efforts to stay preeminent in the field."

Some universities seem eager to work on the autonomous land vehicle. "Just moving down a road in a well-lit environment is not all that difficult," says Azriel Rosenfeld, a professor and director of the Center for Automation Research, at the University of Maryland, in College Park. But when the vehicle moves off the road and when the light and background are varied, the challenge both to computers and to the vision-recognition equipment is stiff, he observes. –**Robert Rosenberg**

Research & development

MCC seeks to draw smaller companies

Microelectronics & Computer Technology Corp. is opening the door for small U. S. companies and start-up ventures to join the Austin, Texas, research and development cooperative by offering an associates' program. For a much lower fee than full members pay, those participants will receive nonproprietary information based on MCC's advanced research. They will not be voting members.

The cooperative is targeting its research at four areas: software, semiconductor packaging, advanced computer architectures, and computer-aided design of very large-scale integrated circuits. The cost of an associate membership will be calculated on a sliding scale based on a firm's revenues and purchases in the industry, says B. R. (Bobby) Inman, president and chairman of MCC.

At the same time, confident that the research talent already assembled will produce significant results, the 15 shareholders in MCC are doubling the fee for new full members. Starting in May, U. S.-owned companies that have not yet applied for membership will have to pay $500,000 to join. Also, Inman says that a 16th

Electronics report

shareholder will be announced in about a month.

Two in fold. Announced last week, the associates' program already has two members: Scientific Applications Inc., of La Jolla, Calif., and Quotron Systems Inc., of Los Angeles. "For the most part, associate-program members will be companies with revenues less than $100 million that would otherwise be unable to become full participants in the advanced research programs," says Inman.

A corporation with full membership status is expected to provide funding and personnel for at least one of seven advanced research thrusts. Inman estimates that the minimum yearly expense of an MCC shareholder participating in one of these (for example, CAD) would be $1 million. In fact, members participating in all seven will pay about $7.5 million a year.

But Inman remains confident that shareholders will get their money's worth now that he has named six of the seven MCC vice presidents to head these programs. The six are Woodrow Bledsoe, artificial-intelligence and knowledge-based systems; Eugene Lowenthal, data-base architectures; Peter C. Patton, parallel processing; Raymond Allard, human-factors technology; John Hanne, VLSI CAD; and Barry Whalen, semiconductor packaging and interconnections. He expects to have the seventh—for software technologies—by early May. —**J. Robert Lineback**

Trade

NTT's IC seminars get mixed notices

The list of integrated circuits qualified for use in equipment sold to Japan's Nippon Telegraph & Telephone Public Corp. weighs well over a pound and contains some 5,000 part numbers—but none is attributed to a U. S. manufacturer. Although inclusion on this list is not, strictly speaking, required to sell into the NTT market, it is important enough for some 40 U. S. IC makers to have

Circle 61 on reader service card

Circle 231 on reader service card

sent representatives to a series of seminars held by NTT during the past month in Tokyo, San Francisco, and Boston to explain the qualification process. They came away with much documentation and a sense that while NTT was definitely opening the door to U. S. suppliers, the process is going to be a slow one.

Ostensibly, the meetings concerned quality and reliability standards. NTT buys no ICs, but it does qualify parts for some of the equipment it buys. For quality and reliability engineers, the seminars were a discussion of procedures similar to those set up under U. S. military specifications. For sales managers, however, the meetings were one more step in a complicated formal dance whose end may be years away.

The NTT specs were, in fact, more stringent than U. S. IC makers are used to. However, a National Semiconductor Corp. reliability manager, Robert West, commented later, "I think we can do anything they want us to in the way of reliability." The actual NTT requirements were not at issue, only the use to which they would be put. Many of those present questioned whether NTT would actually buy equipment with U. S.-made components inside.

Made in Japan. An Intel Corp. executive challenged NTT at the San Francisco meeting to estimate the volume and value of its equipment according to microprocessor architectures. He pointed out that one of the parts on the NTT approved list was an 8080 microprocessor developed by Intel—but in this case manufactured and sold by Japan's NEC Corp. "There is a real question as to whether it is worthwhile to pursue the market at all," he said.

On the other hand, U. S. systems and equipment makers do report a more hopeful story. Last year NTT bought $140 million in equipment from U.S. suppliers, up from $48 million in 1982 and only $18 million in 1981. "The situation is dramatically different from three years ago," says William Finan, special assistant to the Under Secretary of Commerce for international trade. "For a long time, NTT would never concede that

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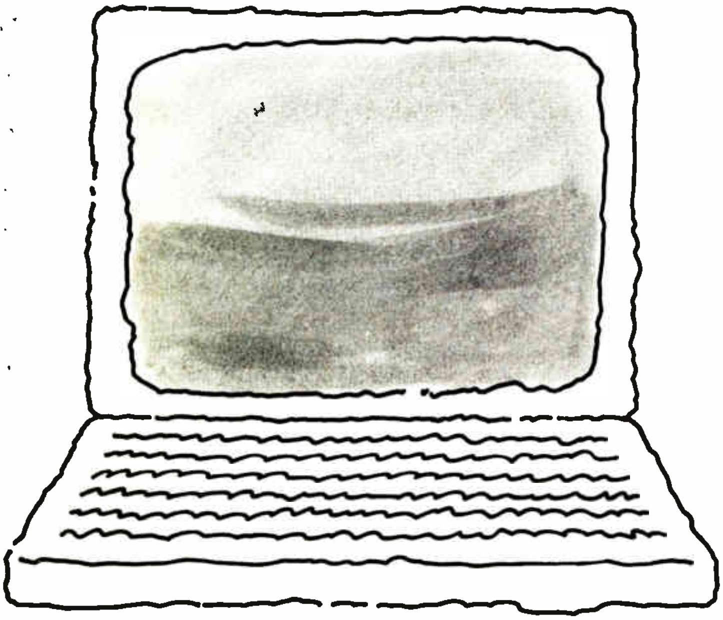

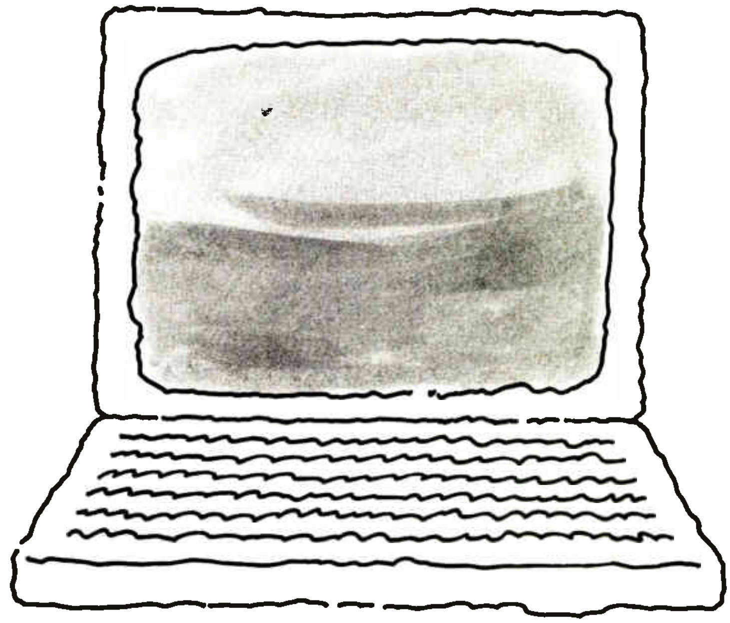

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The Midnight Sun Rises in the West

it had anything to do with semiconductor specification and design. Now, if an IC maker is told by one of NTT's suppliers that their part doesn't meet NTT specs, Japan's phone company will cooperate in the qualification process or even indicate that the part does not have to be qualified."

Even as U. S. IC makers pondered their options, NTT selected the Rolm Corp., of San Jose, Calif., as supplier of digital private-branch exchanges, which NTT will resell. The Rolm equipment contains U. S. ICs that need not be qualified by NTT since the whole system has met specifications. The value of the NTT agreement will be $12 million to $14 million this year. —**Clifford Barney**

Personal computers

IBM moves to take the office market

With competition for office business on the rise from other personal-computer makers, International Business Machines Corp. is enhancing its Personal Computer line, placing the best-selling machine in an even stronger position to dominate the work-station market. The new products "turn the Personal Computer into a new system," says Philip D. Estridge, president of IBM's Entry Systems division. He adds that they "take the PC family of products into the mainstream of office functions."

The enhancements include:

- New word-processing software from the Displaywriter text-processing system, now redesigned for the IBM PCjr home computer, the PC, the PC XT, and the portable PC. The software for the home computer will cost $99, for the others, $299.
- Communications software that lets PCs send documents written with the new DisplayWrite word-processing software to other similarly equipped PCs, Displaywriters, and mainframe computers ($375).
- Software linking PC work stations to IBM's Professional Office System (Profs)—office-automation software

that runs on IBM's 4300 and 370 computers ($200).

- A new low-end System/36 processor, the 5362, to handle up to 86 terminals ($13,000 to $28,000).
- File-transfer programs (for $950) to let the PC communicate with IBM's System/36 and System/38.
- A videotex capability for the PC and PC XT or the PCjr, for $250 or $220, respectively.
- A $429 color monitor for PCjr.

End in sight? The total package makes IBM "more competitive [in the office-automation marketplace] than before," thinks Sanford J. Garrett, a research analyst with Paine Webber Mitchell Hutchins Inc., in New York. "What IBM is saying is that the PC will be the universal terminal for the office. It marks the end of the line for other systems."

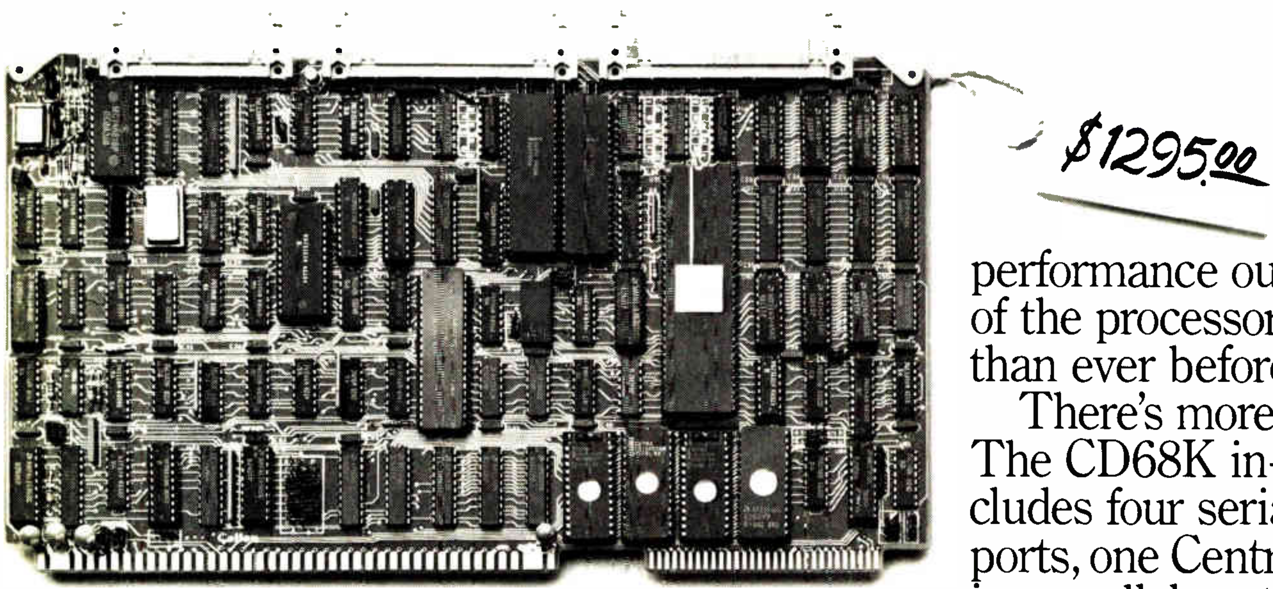
George F. Colony, president of Forrester Research Inc., Cambridge, Mass., foresees increased demand for the PC, which he calls "the most popular work station in the Fortune 1,000 market." Colony believes that PC shipments will top 1.2 million this year and hit 1.8 million in 1985.

Making a splash. Meanwhile, Commodore International Ltd., Norristown, Penn., has introduced an IBM-compatible portable computer at the Hannover Fair, as well as a Z8000-based microcomputer for office use. However, many observers think it is out of its element.

Made under license from Bytec-Comterm Inc., of Ottawa, Ont., Canada, maker of Hyperion IBM-compatible computers, the Commodore portable and office-oriented model probably will not hit the U. S. until next year. "Commodore will be late to the market," says industry consultant Amy Wohl, of Advanced Office Concepts, in Bala Cynwyd, Pa. In addition, it is "perceived as a consumer-product vendor rather than a business supplier," she says.

"The office market requires a fairly substantial support network," Paine Webber's Garrett adds, and Commodore is "totally removed" from this environment. "There's no way they can make a move into the office." –**Robert J. Kozma**

CALLAN GOES UNDERBOARD.



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Limit of 6% foreseen for DOD budget rise . . .

Real growth in fiscal 1985 Pentagon spending will be held to roughly 6% above last year's level if the influential subcommittee chairmen of the House Armed Services Committee prevail in an ongoing congressional debate. That increase is less than half the 13% President Reagan has proposed [*Electronics*, Feb. 23, p. 91] and it could go still lower. For example, more concerned about the Federal deficit and the economy than about national security, **the House Budget Committee is urging only 3.5% real growth in defense spending for the year that starts this Oct. 1.** The 6% growth would put the Defense Department's budget authority at about $280 billion rather than the $305 billion first sought.

. . . as strength is forecast for military electronics despite possible cuts

In mid-April, Chairman Les Aspin (D., Wis.) of the personnel subcommittee of the House Armed Services Committee forecast cuts that would be made in the event of a 6% real-growth rate. The $34 billion-plus for research and development would be cut by $3.4 billion, he said, while the $107.6 billion sought for procurement would drop by $8.8 billion. Spending for sea power would fall by $1.5 billion, and readiness funds would loose $2.7 billion from the $81.4 billion now sought for operations and maintenance. **Some military electronics contractors anticipate larger election-year cuts in some of the more visible programs,** such as the M-X Peacekeeper intercontinental missile and some aircraft. Although stiff reductions for intercontinental ballistic missiles and for ships are anticipated, most congressional sources regard military electronics programs as relatively invulnerable to cutbacks—particularly command, control, and communications efforts, which are expected to stay strong.

FCC policy changes mean more competition, less revenue for Comsat

The Communications Satellite Corp. can expect intensifying competition and declining revenues, thanks to changes in international communications policies made by the Federal Communications Commission. Most important are two decisions that radically alter the rules on the relationship with the International Telecommunications Satellite Organization: first, common carriers now have the right to build and operate their own earth stations to access basic Intelsat services; second, non-Comsat carriers may transmit Intelsat's specialized business services through their own gateway stations. Previously, the only route to Intelsat was through Comsat ground stations. **The commission also told Comsat to clean up its financial act.** Finding that the company's profits on the Intelsat and Inmarsat satellites were well in excess of what the FCC permits, the commission told Comsat to file new fees by June 15 that yield no more than the mandated 11% to 12.5% rate of return.

Transportation unit chooses R&D adviser

The Department of Transportation has created the new job of science and technology adviser and handed it to Howard Dugoff. Virtually unknown to the electronics industries, he served with the National Highway Traffic Safety Administration for 10 years, most recently as head of research and special programs. **In his new post, Dugoff will oversee research and development programs,** including those of the Federal Aviation Administration. He will also be Secretary Elizabeth Hanford Dole's scientific representative to industry and academia.

Teaching teachers about Congress

"I've visited all the right congressmen and all the right senators on all the right committees; I've made myself, my organization, and my plans known to them. They listen and they smile, and they appear to agree, but then nothing happens. What's going wrong?"

That complaint by a prominent electronics engineer is one of long standing among those who come to Washington in search of funding for everything from a new corporate research and development effort to improvements in the curriculums of the nation's secondary schools. What are these engineers doing wrong? For one thing, they are letting their egos blind them to the realities of Washington's political arena, itself a place known for its many enormous egos.

Engineers and scientists, particularly those from academia, could learn a great deal from businessmen's approach to lobbying Congress, Capitol Hill staff members agree. Asked where these well-meaning individuals go wrong, one committee staff director observed, "First, they are inclined to lecture the members when they appear before a committee. If they are distinguished in their field—say, the holder of a Nobel Prize—they sometimes come on with a bit of arrogance, suggesting that anyone who challenges their position must be close to idiocy." Committee members don't expect witnesses to genuflect before the panel; but it seems clear that Senate and House members want more consideration than they are now getting from high-technology specialists.

Getting perspective

"Many academics, particularly from the more rigid disciplines of science, expect us to accept their premises at face value," argues one Senate subcommittee staff member, who becomes upset when such witnesses "are clearly put out by what they feel is our failure to have done our 'homework' before coming to the lecture. The point is that our hearings are where we get our homework assignments; they are not meant to be a lecture series. Hearings are meant to be free and open dialogues."

The congressional staff members with whom the topic was discussed over a period of months see other limitations in the lobbying efforts of teaching engineers and scientists who fail to get their proposed legislation made into law. At the top of the list are three problems that one House staff member identifies as the failure to put their issues in a national political perspective, an unwillingness to compromise, and a lack of tenacity in promoting final passage.

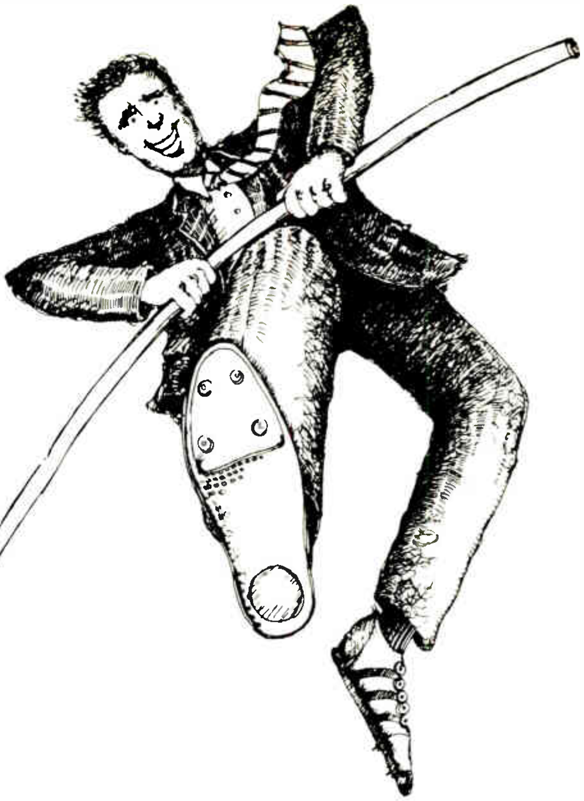
"Getting perspective," explains a House committee investigator, "means simply familiarizing yourself with the problems overall that face both the legislative and executive branches, learning their priorities, and getting to know the key members of the agencies and Capitol Hill committees and subcommittees that could affect your interest. For example, a year when unemployment and trade deficits are on the rise, while corporate revenues are slipping, is not a good year to promote more money for some sort of new scholastic endeavor. Neither the money nor the support will be there, and you won't get much of an audience."

Think compromise

An unwillingness to compromise also frustrates congressional members who must deal with the scientist or engineer determined to move straight ahead, without deviation, toward his goal. "Getting a start on their programs with a small amount of money from an unexpected source in one session, say, and then getting the rest next year often doesn't occur to these people," gripes another subcommittee director. "No one can afford to be singleminded all the time and expect to succeed," he contends.

The lack of tenacity in pushing, driving, hammering, calling, and mailing letters to the Congress to get passage of a program is seen by most members and their staffs as the biggest failing of engineers and scientists in both the corporate and academic world who want Federal support for their programs. "Too often the Congress gets hit with the one-shot march on the Capitol by academicians eager to gain congressional support," points out another Capitol Hill staff member, adding that, "more often than not, they want to stop something, rather than start it, and stopping is always harder to do. Anyway, the single-shot system doesn't work."

What is effective? Contributions to the reelection campaigns of the legislators that the engineer or scientist is trying to persuade sometimes can be a starting point, he explains. "An effective lobbying effort needs good timing, an appreciation of the realities and priorities, plus a steady effort." **–Ray Connolly**



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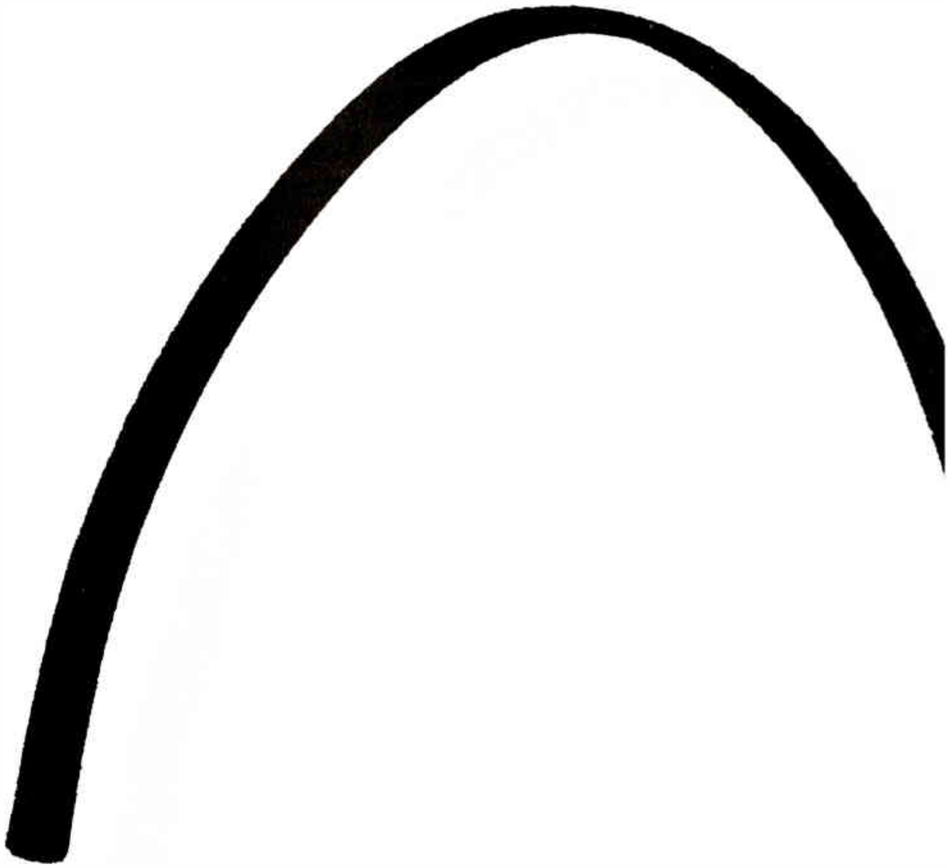

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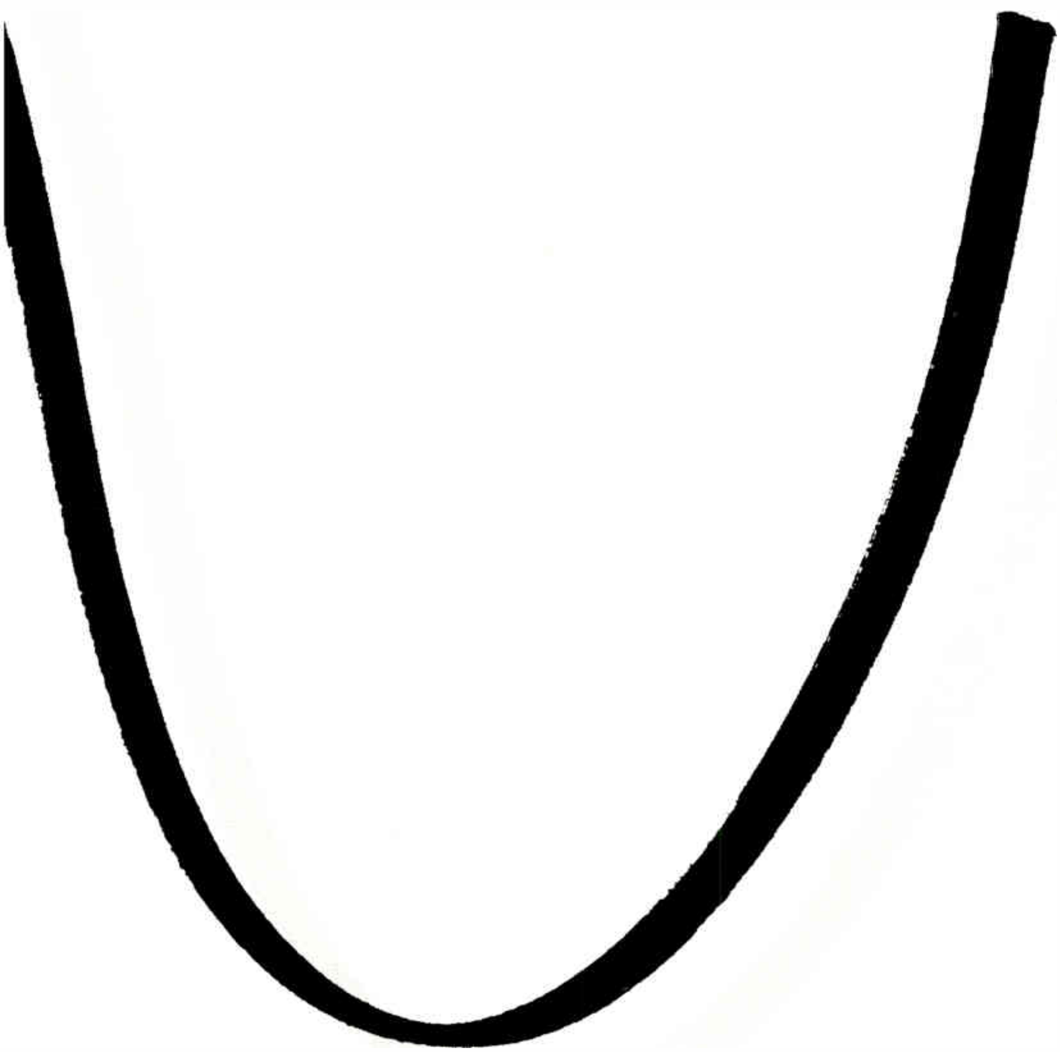

Fujitsu plans thrust in value-added networks . . .

Japan's leading computer manufacturer, Fujitsu Ltd., has signaled its intention of becoming the front runner in the country's up-and-coming value-added-network market. In 1985, it will start a common-carrier network, which will include facsimile and TV conferencing as well as digital communications and data processing. The net, operating on 6.3- and 1.5-megabyte/s circuits, will also connect Fujitsu's 13 major branches and plants. Prior to full operation, a pilot system will be installed in the firm's new headquarters building and five other facilities. Fujitsu president Takuma Yamamoto predicts that **annual sales will grow from $4 million in 1985 to $400 million in 1990.** He says that investment for the whole plan will be about $89 million. Fujitsu's terminals and otherhardware will feature an open interface so that data-exchange compatibility with other manufacturers will be possible. Specifications for terminals and software have not yet been announced.

. . . while U. S. firms hope for easier entry into the market

The U. S. has apparently won a battle in its struggle to gain equal entry into Japan's emerging value-added-network market [*Electronics,* March 22, p. 94], but will it win the war? The Telecommunications Business Act has been approved by the Japanese cabinet and now goes to the Diet (parliament) for probable approval, with implementation to take effect April 1, 1985. "The bill is liberal on the surface," says Timothy Dwyer, president of Prime Computer-Japan Inc., meaning that **no limits have been placed on foreign capital participation in leased-line networks**—the category of greatest interest to U. S. firms—and apparently simple application procedures have been adopted. "But," he cautions, "the administrative instructions have yet to be written. What worries me is the room for bureaucratic mischief." U. S. Embassy officials in Tokyo are planning to follow up their earlier contacts with the Ministry of Posts and Telecommunications after the bill passes in early autumn. "That is when the administrative instructions will be written," says an embassy official. "We want to make sure they keep things simple."

Nationalized Bull buys into U. S. computer company

To plug one of the major holes in its product line, Bull, the data-processing group controlled by the French government, has purchased 10% of the common stock of Ridge Computers, Sunnyvale, Calif. **Bull will thus get access to the U. S. company's 32-bit scientific and industrial computer,** with a virtual memory of 4 billion bytes and a current processing performance of 3 million instructions/s (against a theoretical limit of 8 MIPS). By year-end, Bull will start producing the machine at a factory in Echirolles, near Grenoble. The Parisian company, caught up in a general recovery program, recently announced it had trimmed its 1983 losses to less than $8 million.

Philips and Siemens in joint venture to develop memories

A deal is in the making between Europe's No. 1 and No. 2 electronics producers, Philips in the Netherlands and Siemens AG in West Germany, that aims at a joint development program in submicrometer technology. **The talks involve setting up production facilities for static and dynamic random-access memories** with densities of 1 and 4 Mb, respectively. Behind this venture, Munich-based Siemens says, is the decision to exploit the firms' combined semiconductor know-how, thereby making their development efforts more effective. This can help them come out with such key components as high-density RAMs at around the same time—in the late 1980s—as Japanese and U. S. producers.

Cell library adds 8-bit d-a converter needing no trimming

Watch for Plessey Research (Caswell) Ltd., in Northants, UK, to add a fast, small, 8-bit digital-to-analog converter to its library of complementary-MOS cells used in the design of semicustom very large-scale ICs. The great attraction of this new cell, to be described at the Custom Integrated Circuits Conference, May 21–23 in Rochester, N. Y., is that it can be fabricated in a standard 2.5-μm C-MOS process, without add-ons or trimming. Until now, C-MOS data-conversion chips have used either laser-trimmed thin-film resistors or capacitor arrays. Instead of a resistor array, **the Plessey converter uses multiple current sources, no one of which contributes more than 1/16th of the total current,** so current variations from source to source tend to balance out.

British Telecom to be denationalized

Paving the way for Western Europe's biggest sell-off of a state-owned industry, Britain's Parliament has approved legislation to turn the country's telecommunications network run by British Telecom into a private entity. Pledged to promoting a deregulated marketplace, the Conservative government has said **it will sell 51% of its holding in British Telecom and float the shares on the stock exchange later this year.** The transaction is expected to raise more than $6 billion and follows on the heels of the denationalization of other holdings, all part of a plan that will put $15 billion into the government's coffers by 1988.

Radar remembers targets for a better view

Researchers at McGill University, Montreal, have developed an on-ship radar system that uses high-speed image processing, now used in weather and air-traffic-control radar, to avoid sea clutter. The new system's 16-bit microcomputer—a Digital Computer of Canada PDP-11/23—stores sequential radar pictures, which it displays as a nonfading color picture on a high-resolution color monitor. Although it can display each radar picture separately, **this system does scan-to-scan averaging so that items that move stand out more than others,** making targets easier to distinguish than in conventional systems.

U. S. know-how, UK sterling establish new chip manufacturer

A marriage of UK venture capital with U. S. technology will yield Britain's first new fully independent semiconductor manufacturer in many years. Integrated Power Semiconductors Ltd., to be based in Livingston, Scotland, is being set up by six Silicon Valley semiconductor executives. **The company will turn out smart power devices** for use in power management systems, power drives, computer disk drives, printers, and related equipment. Funding, to the tune of $22 million, came from a UK investment consortium and the Scottish Development Agency. Integrated Power Semiconductors' production facility will be on stream within 18 months, but an outside foundry is being used so that chips can be delivered before then.

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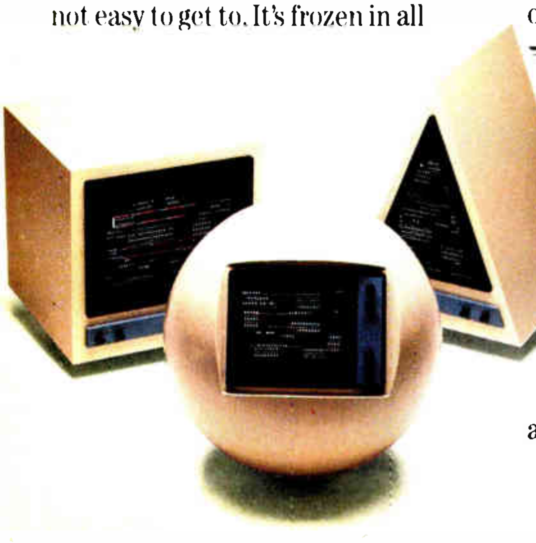

You can't get at a problem you can't get into.
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Not easily. Because the tools you need for data analysis aren't easy to use. And they don't work together. Which means you have to be fluent in many different computer languages.

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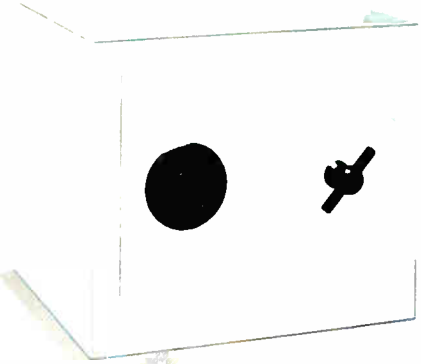
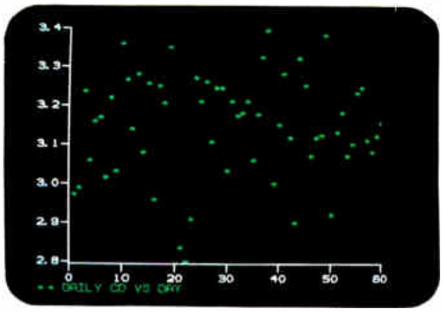


know programming inside and out, you're stopped cold. Frozen.

You can't visualize a problem you can't see.
Computer printouts. How do you turn them into useful information?

With a graphics software package? Good luck. Try to use it for real analysis. Try to change variables and regraph on a plotter, a printer and a color terminal.

You'll feel like someone's plotting to overthrow your sanity.



Pieces that don't fit won't solve the puzzle.
If you analyze data in manufacturing, quality assurance, research and development or general management, you're paid to make decisions. But your problem solving tools are often themselves a problem. They're awkward and incompatible. They waste your time and your company's money.

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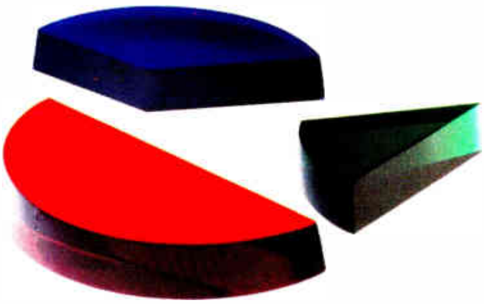
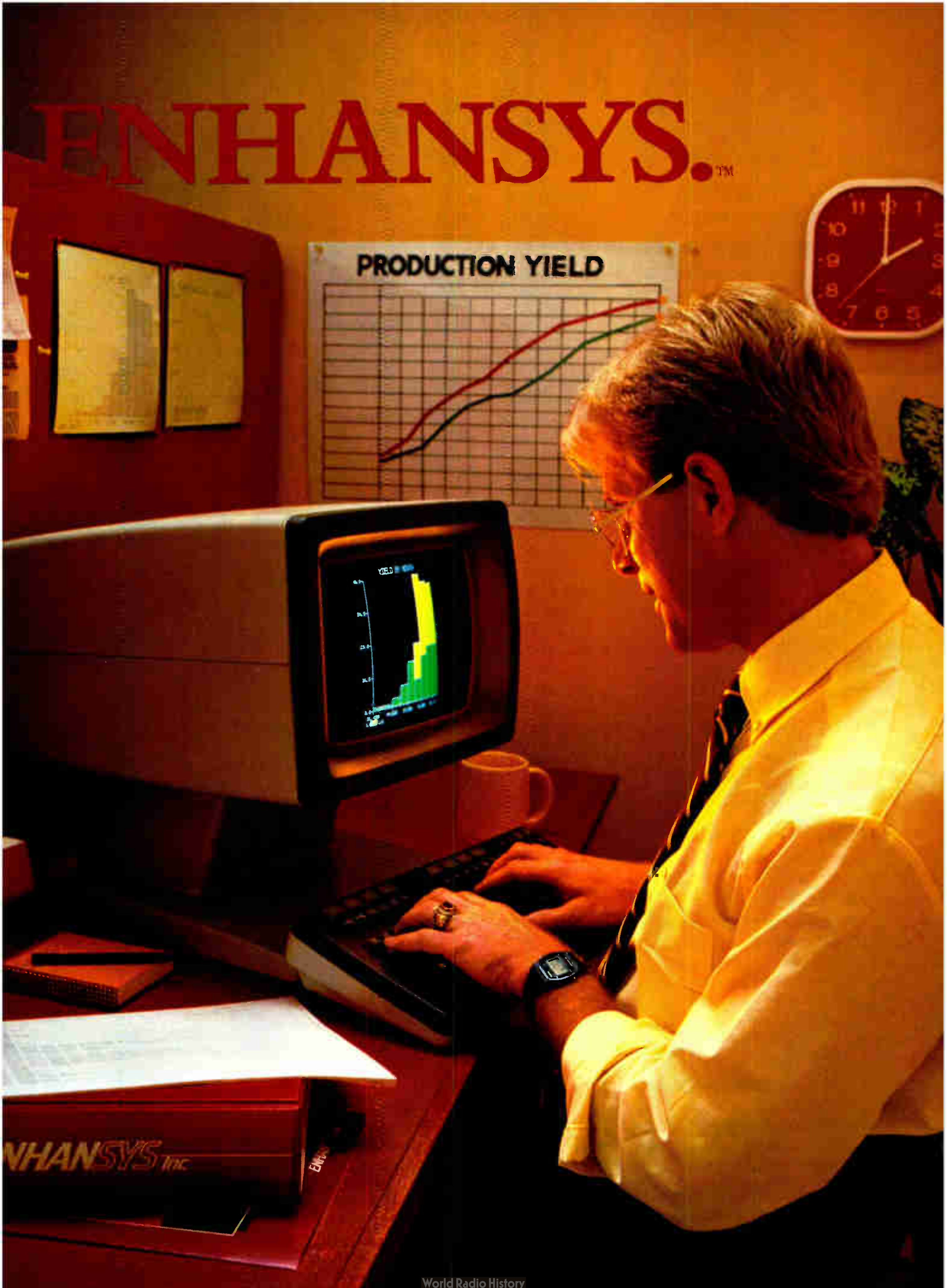


Now follow us through a new chapter in faster, more efficient problem solving and decision making.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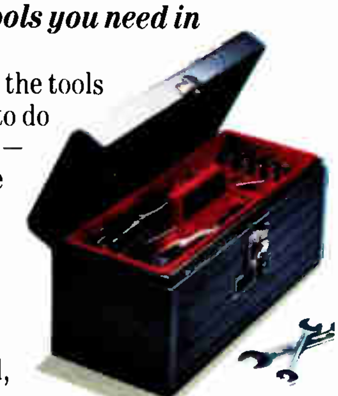
So you've got the data. What then? ENHANSYS software gives you everything you need to manage and analyze it. Like sophisticated, yet easy-to-use sorting, screening, grouping and table management capabilities. Plus a complete range of statistical and mathematical functions. So you can look over the numbers without having them overwhelm you.

Put the problem on the table. Or a chart. Or a graph.

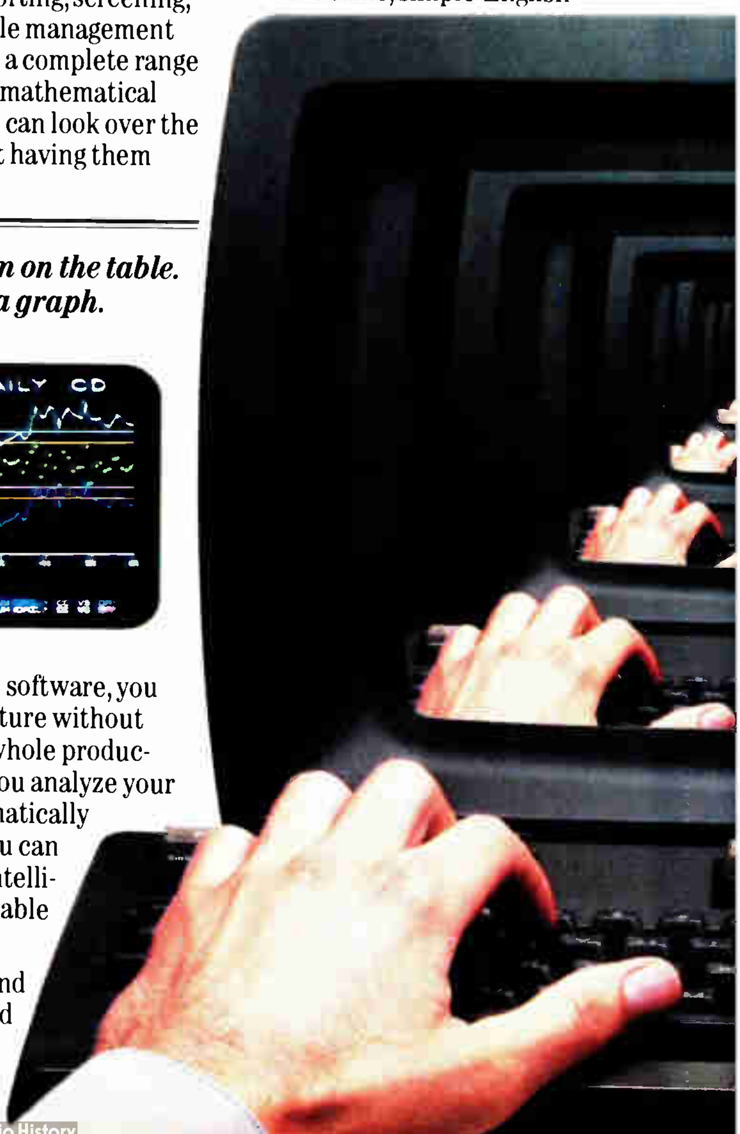
With ENHANSYS software, you get the whole picture without going through a whole production. Then after you analyze your numbers mathematically or statistically, you can display them as intelligible, understandable information.

Enter the command "TRENDLINE" and perform a linear regression. And plot the line directly onto a graph with your original data. In full color. With a hard copy for hard evidence.

All the tools you need in one kit.



You get all the tools you need to do your work— and all the tools work together. They're totally integrated, sharing the same data, using the same, simple-English



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commands, operating identically no matter what system you're on.

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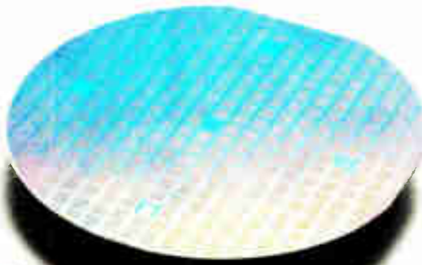

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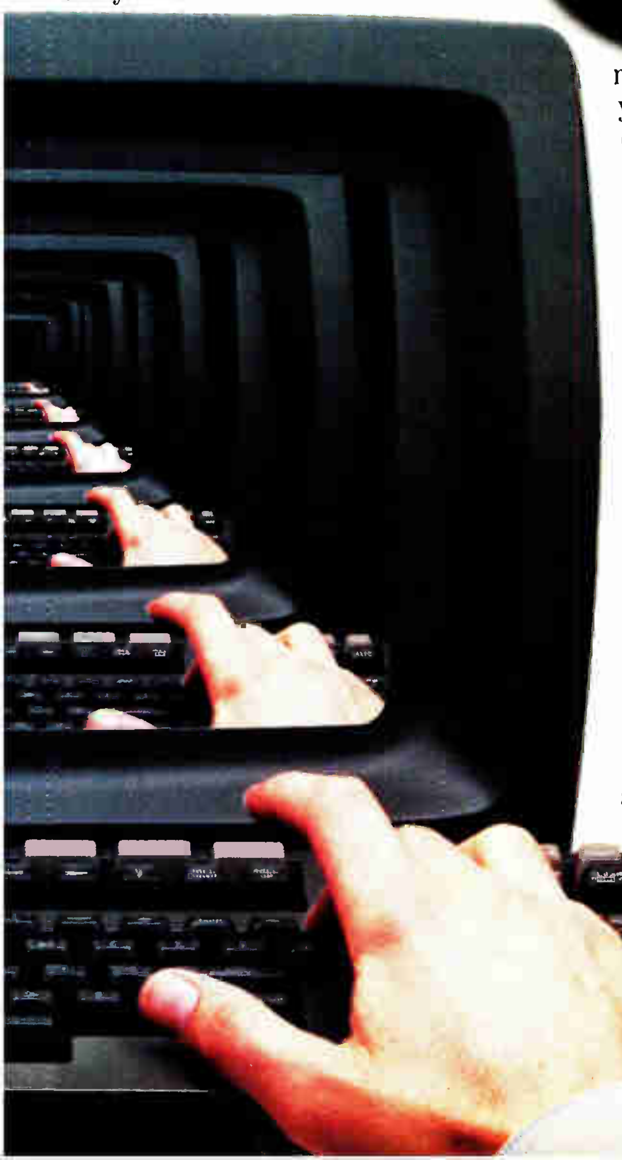

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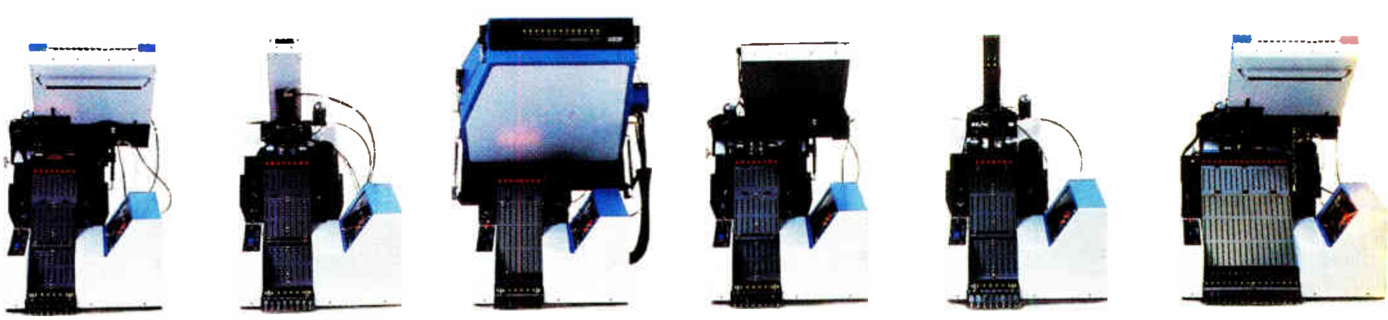

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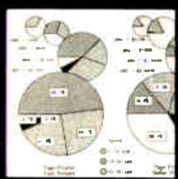

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Laser disks may be used as computer ROMs

by Charles L. Cohen, Tokyo bureau manager

12-centimeter audio disks have a capacity of more than ½ gigabyte and can be stamped out at high speed

Digital read-only memories with capacities higher than ½ gigabyte are among the new applications being developed for the recently introduced 12-centimeter laser-pickup digital audio disks. With a capacity roughly equal to 250,000 pages of typewritten text—some 500 to 1,000 times greater than the capacity of five-inch floppy disks—the ROMs should prove attractive as a low-cost medium.

These Compact Discs were first developed for high-fidelity sound equipment by NV Philips Gloeilampenfabrieken of the Netherlands and Japan's Sony Corp. and standardized by an international group of 59 firms. Popularly priced Compact Disc players are now in retail stores, and similar ones with digital output terminals should be easy to make at very little difference in cost. Several companies are working on new products, but they are keeping their information very close to the vest and will only speak off the record.

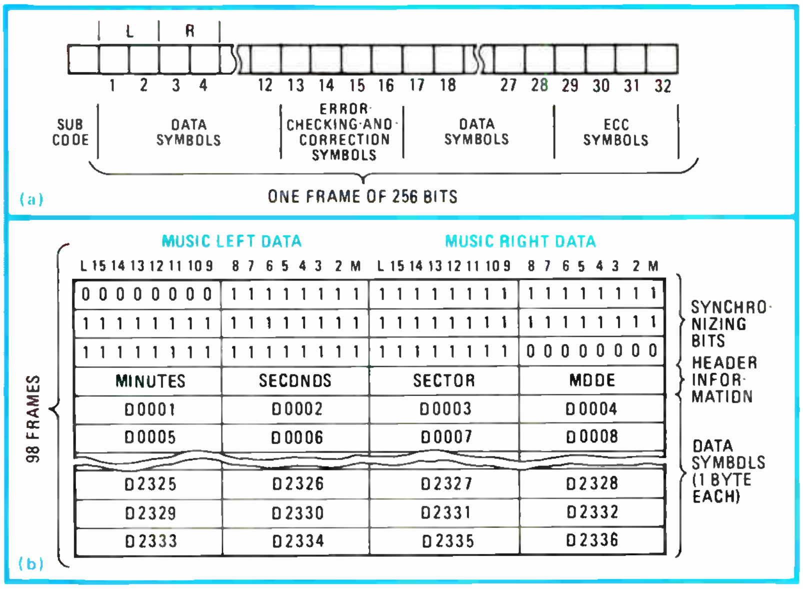
Inexpensive, too. Disks should be relatively inexpensive, too. After a one-time mastering charge of about $2,500, copies can be stamped out at high speed at a cost lower than that of unrecorded floppy disks. Floppies are usually recorded in real time instead of stamped.

For home and educational computer applications, Sony, Philips, and other firms are striving to develop a single digital-disk standard compatible with the music disks. So they are standardizing not only the data format, but also lists of European and Chinese characters, type faces, and other output attributes needed to print out texts and musical scores. Of course, the disks will also be used for digital storage of data, application programs, and systems software. For specialized applications, nonstandard formats could be used, much as they are with floppies, for which manufacturers have developed a variety of formats.

In the standardized digital ROM, the data used for the left and right audio channels will be employed for digital data storage, while the subcode used for housekeeping—including track numbers and playing

CD has plenty of ROM for data

The upper diagram shows the format (a) of an encoded frame of encoded music on an optical digital audio disk (Compact Disc). The first two data symbols are a single music sample from the left track, the next two are from the right track, etc. The 2,352 data and housekeeping symbols shown on the lower half of the figure (b) represent only one sector of Compact Disc ROM. They represent the 588 music samples that would be in one sector of a music disk. Note that 16 bits are required for music samples on either left or right track. Subcode symbols and error-correcting-code symbols in the sector are omitted for clarity. Each group of 8 bits is called a symbol, not a byte, probably because before recording on disk there is an 8-to-14 transform (conversion). –**C.L.C.**



times—will be not be changed. This technique provides sectors with 2,352 data bytes each, though for ease of use in digital data applications, only 2,048 bytes in each sector will be used.

Even so, the capacity for the nominal 60-minute disk playing time totals 552.96 megabytes [*Electronics*, April 21, 1983, p. 108]. The spare bytes will probably be used for error-correcting code over and above what has already been built into the music system.

The music disks use 16-bit straight-line encoding of samples of the analog signal (see "Plenty of ROM for data," p. 85). Right and left channels are recorded alternately. Every 12 bytes, 4 error-correction bytes are inserted; and two such sequences, a total of 32 bytes of data and error-correcting code, are preceded by a subcode byte and constitute a frame. Because the subcode bytes are designed with a sequence that repeats every 98 frames, the 2,532 data bytes in them became the basic addressable sector. Sixteen sector data bytes are used for synchronization and a header.

Redundancy methods. Redundancy is ensured both in the recording of pits on disk and in the coding of the data recorded. To provide a pit pattern that has low direct-current content, low-frequency bandwidth, and high clock-frequency content, the 8 bits of each byte are converted to 14 by a lookup table. Moreover, 3 interface bits are inserted between each sequence of 14.

Before recording, redundancy coding of the digital signal is provided for with a Reed-Solomon code to derive the first 4 redundancy bits in each frame from the 24 data bytes. (Reed-Solomon is a high-efficiency code for error detection and correction of digital data configured as words.) To interleave the bytes along the track and thereby prevent a burst error from deleting one or more complete frames, different delays are furnished at each bit position so that the bytes are distributed over three sectors.

A second Reed-Solomon encoding provides further redundancy by adding four more redundancy bytes. During readout, the start of the data output stream is delayed a fraction of a second, until the first three sectors have been stored in the 16-kilobit random-access memory in each Compact Disc Player. Then the data is transferred at a steady rate of 1.2 megabits a second—the equivalent of 153.6 kilobytes/s.

Testing

Electron beam tests dense VLSI chips

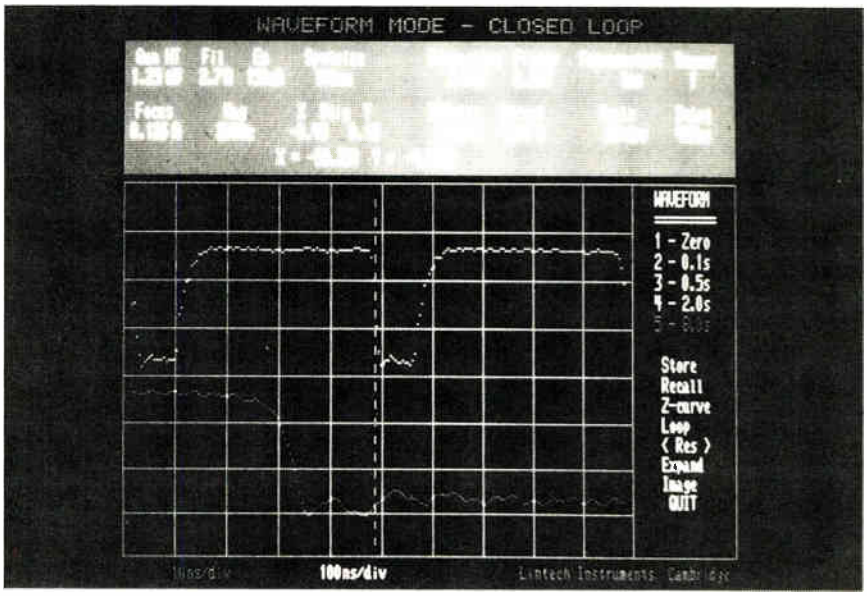
Circuit designers will soon have a powerful new aid in debugging very large-scale integrated circuits containing several hundred thousand transistors apiece. An electron-beam prober, made by Lintech Instruments Ltd. in Cambridge, UK, makes a bow this week in Philadelphia at SEM 84, the showcase exhibition mounted for the scanning-electron-microscope industry.

The machine [*Electronics*, April 5, p. 64] will help solve a major headache—examining the operation of a working IC when only 64 to 120 nodes can be accessed externally. Using Lintech's prober, an electron beam can be directed to any node on the chip's surface and the voltage at that point picked off. The node's operation can be displayed and examined as the circuit ticks at clock speeds up to 250 megahertz. The system can capture waveforms with rise times as rapid as 400 picoseconds.

Alternately, in a sampled-imaging mode, the entire wafer surface can be examined with the chip's high and low states visible as contrast differences at any point in the clock cycle. This mode quickly reveals memory cells and logic blocks stuck in one logic state. "Stuck-at" cells in a random-access memory would be immediately visible.

Known technique. These sampling-electron-beam techniques have been known since the late 1960s. An earlier system, also developed by Lintech and launched in 1981 [*Electronics*, June 30, 1981, p. 73] adapted a standard SEM for operation in sampling mode. But these first systems, confesses Graham Plows, Lintech's managing director, need a highly qualified operator and are ill-suited to the development environment.

Now Lintech has produced a machine that is dedicated to the task. There is an extra-large electron-beam chamber able to accommodate wafers up to 6 inches in diameter as



Quick prober. The color monitor of Lintech Instruments' electron-beam prober uses high-resolution graphics to display waveforms with rise times as rapid as 400 picoseconds. The display is also used with a single keyboard, showing operating modes and parameter values.

Circle 87 on reader service card

well as mounted ICs; all the instrument parameters have been brought under computer control and can be set up through keyboard and menu-driven display, and image processing facilities have been added so that clean flicker-free images of the chip's surface are presented on a standard raster-scanned TV display.

The electron-beam column has to be large enough to contain the digitally controlled table that positions the wafer or mounted chip under the electron beam to an overall precision of 0.2 micrometer. The electron beam itself is 0.1 μm in diameter.

Rapid access is also important, so Lintech has come up with an unusual column design in which the column splits horizontally and the bottom half can be removed. Another advantage of this arrangement is that the IC driver electronics can be kept outside the cavity and the lead-throughs can still be kept to less than 10 millimeters—that is important when working at emitter-coupled-logic speeds. Provision is made to accommodate wafers or packaged chips with up to 64 pins. Two sockets are provided so that direct comparison can be made with a known-good chip.

There are two displays, a high-resolution color-graphics display for showing voltage traces and for controlling the instrument's operation, and a second high-resolution black-and-white display used when the instrument is in imaging mode. Backing this display is a full-screen image store. Comprising 512 by 768 picture elements with a 16-bit grey scale, the store is used to capture and enhance a displayed image. In this mode, the system can be used as a conventional SEM, with a resolution of 20 nanometers. –**Kevin Smith**

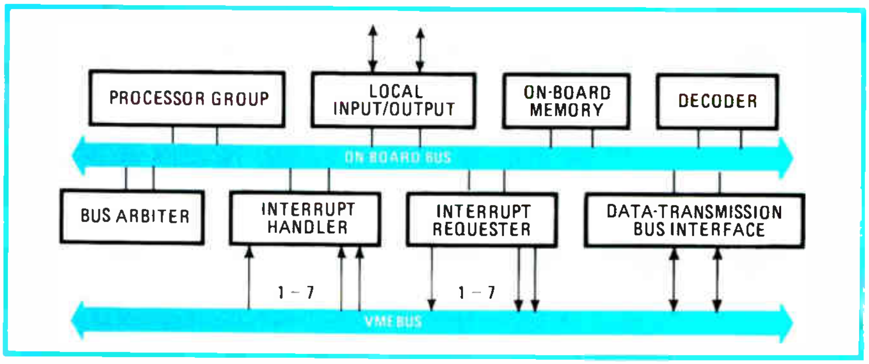
Computers

Microsystem power touches mini's realm

A new design concept from Philips, in the Netherlands, may bring to microcomputers capabilities heretofore found only on minicomputers—and even mainframes—in that they combine distributed processing, real-time operation, and multiprocessing. This trio of features is being implemented in what the company calls its DRM (for distributed real-time multiprocessor) systems. These microsystems, based on 68000 processors, keep software and hardware essentially independent.

In contrast to Inmos Ltd.'s transputer with its Occam language [*Electronics*, Nov. 17, 1983, p. 109], the Dutch system can be programmed either in the widely used C language or in assembly language. The Philips approach uses from several to several hundred 68000 processors, all processing data in distributed fashion. With no centralized components in the system, the breakdown of one processor is of little consequence as others step in.

In development at the Philips Research Laboratories in Eindhoven for several years, DRM systems are now being readied for commercial use at the company's Science and Industry and Electronic Components and Materials divisions, both also in Eindhoven. Among the first products to appear later this year (in the U. S., early in 1985) is a VMEbus central processing board, which has interrupt-handling facilities for communications with other processors, as well as a fast-access local memory for real-time jobs. It will be compatible with all existing non-DRM VMEbus boards (see figure).



Debut. Among the first distributed real-time multiprocessor products to appear is a VMEbus CPU board which has interrupt-handling facilities for communication with other processors as well as a fast-access local memory for real-time jobs.

Lambert van den Hoven, in charge of strategic marketing for microcomputer software at Elcoma, sees prime applications in process control, advanced communications systems, factory automation, test and measuring, and fault-tolerant computers. DRM systems will also make it possible to build fifth-generation mainframe machines using distributed real-time multiprocessing with a large number of computing elements that operate concurrently.

Design independence. One of the system's most important aspects, van den Hoven says, is the relative independence of software design from the hardware. Existing design methods require that data relating to the hardware (such as network architecture and peripheral equipment) on which the software is implemented be taken into account at an early stage in the chain of steps between the initial application system design and the final test. If a system test fails as a result of, say, the wrong choice of a network architecture, it is necessary to go through all the design steps again.

That is not the case in DRM system design. Here, the hardware data is introduced into the design process as late as possible, typically during system integration. This hardware independence considerably shortens the design process, although van den Hoven is not yet prepared to put a figure on the time savings.

The key to hardware independence is the virtual-processing environment, realized in two ways. One is the Hama, for hardware machine, and the other—the Soma—for software machine. A DRM system may

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The Kontron Logic Analyzer is available in 32, 48, or 64-channels and also records simultaneously with up to four clock and 12 clock qualifiers; latches and stores glitches as short as 5 ns and displays them as half-height lines on a 9″ CRT screen. The KLA Series also provides sequential triggering (at up to 14 levels); has a "babysitting" (compare) mode which not only determines a failure without stopping, but also logs how many times they occur over a test; has skew comparison in both time and data domains; provides data qualified and transitional recording; and has optional disassemblers and personality probes for both 8 and 16-bit microprocessors.

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have only one Hama and only one Soma, but typically it has several of each.

A Hama consists of one or more processors with a common address space, one or several input/output facilities, and a local memory. Spreading the intelligence among the Hamas results in a faster system response than is possible in a centralized system where the central processor communicates with nonintelligent remote units.

A Soma consists of one or more processes, each being a distinct body of program code written in either C or assembly language. These processes operate simultaneously on different parts of the application problem. The application may be distributed over a number of Hamas. If a Hama fails, then the Soma may be redistributed among the configuration's remaining Hamas. The free distribution of Somas not only makes optimum use of hardware—it also ensures reliability, since a Hama failure does not generally affect the overall system operation.

Somas also implement operating-system functions. They rely on the communication software layer, which, in the system's hierarchy, lies under the operating system. That approach, resulting in relatively small system overhead for communication facilities, is in contrast to the traditional approach, which implements the communication software layer on top of the operating system.

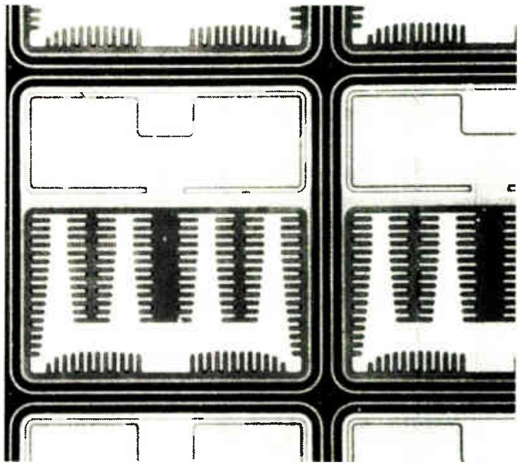
The decentralized operating system provided by the Somas yields distributed processing. In addition, the application programs, like the operating system, are stored completely in the memory. **–John Gosch**

Solid state

Low-cost line unites MOS and bipolar

Equipment designers of industrial and consumer products, long tantalized by promises of low-cost components with MOS input and bipolar output, may soon have them in hand, thanks to RTC-La Radiotechnique Compélec. The principal French subsidiary of Philips will soon be shipping samples of components produced in a technology it will market under the name Mosbip.

The Parisian company reckons it can outpace competition already announced by RCA, Motorola, and General Electric in flexibility and price. Bearing out its contention of low price is the first product, a 450-volt 10-ampere switch meant for use in converters and motor control. When it goes into full production next year, it will cost no more than $1.25 in quantities of 10,000 and more.



Neighbors. This RTC Mosbip chip is able to withstand up to 450 V when it is used in conversion and command applications. The bipolar structure is at the top of the chip, the MOS appears at the bottom.

Combining MOS and bipolar transistors on the same chip has long been a technical possibility. But cost has held back general use of such a technology in high-volume consumer and industrial fields. In automobiles, for example, a virtual revolution that would replace the electrical harness with an optical fiber carrying multiplexed information is being stymied by the lack of cheap electronic switches to replace mechanical relays that cost less than 40¢ each. In a first step toward this goal, starting next year RTC plans to supply a switch to replace the mechanical part for the identical price. Moreover, the use of simple, reliable synchronous motors in household appliances needs only a drop in the price of the command circuitry necessary to drive them to be profitable.

Simple manufacture. RTC's answer is a simple planar technology that simultaneously produces MOS and bipolar transistors on a monolithic crystal. Though patent restrictions limit disclosure of the structure's details, the company does say that, in addition to standard bipolar fabrication techniques, production requires only a single mask to define the MOS transistors' gate oxide.

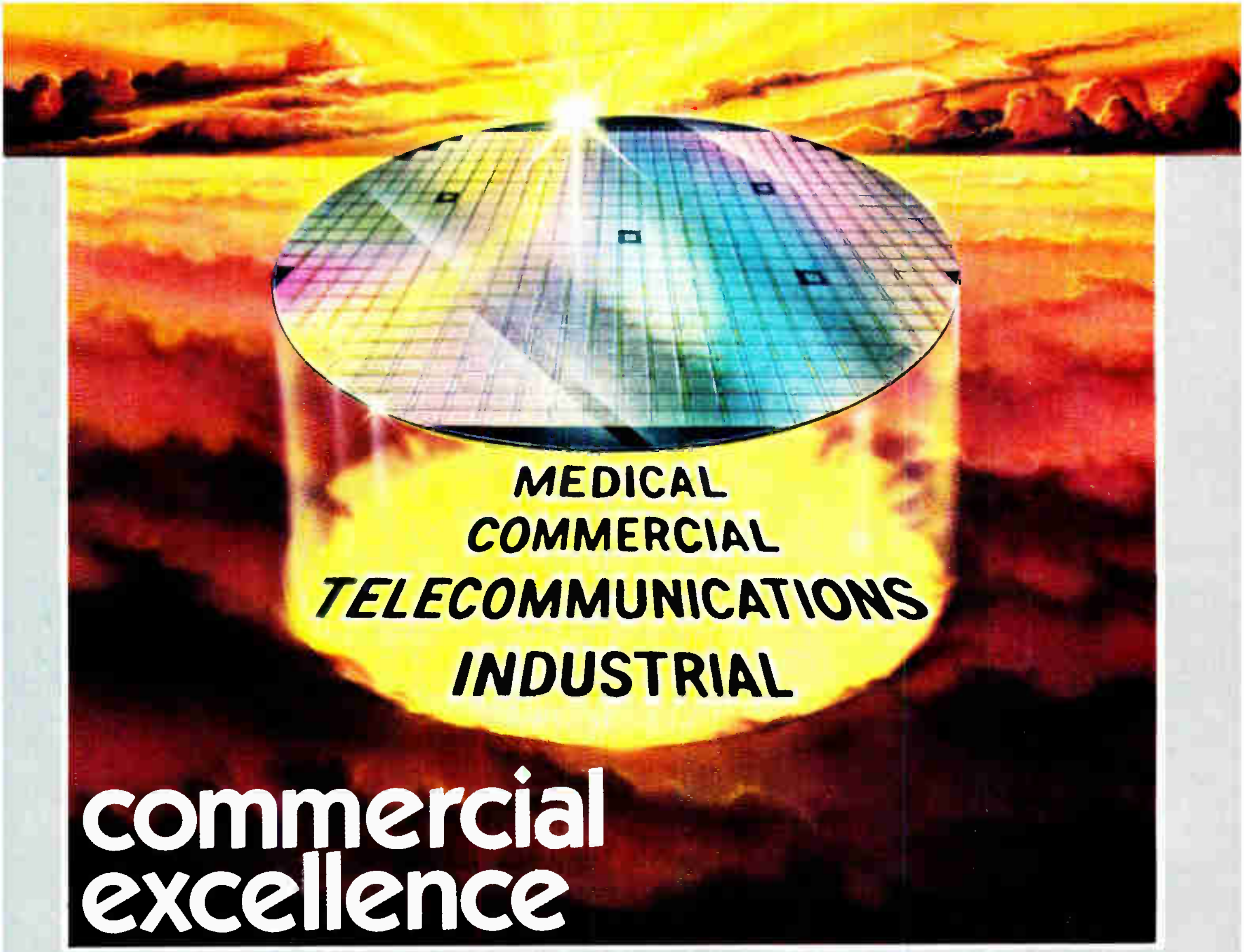
Mosbip's smaller MOS surface sidesteps the yield problems of cascode components, which also need two dedicated command circuits where the RTC parts can be controlled directly by microcircuits. In addition, the new parts can function at much higher frequencies than do MOS thyristors.

RTC's claim to flexibility rests on the fact that the technology can be produced in four basic structures that permit a tradeoff of the high input impedance and fast switching time of power MOS against the high-power-switching capability of a bipolar Darlington amplifier. The first is the high-voltage-switching structure with which RTC will first go to market and which in future versions will be able to withstand up to 1,000 V.

The second will be a Mosbip with separated drain and collector. This is the structure RTC will use for the electronic switch that will mark the company's entry into the automotive-components market.

By 1988, when RTC estimates that that market will start to boom, it plans to have evolved the structure to a point where the MOS control logic is sufficiently sophisticated to make multiplexing a reality at reasonable cost.

The Mosbip range of components will be completed by two Darlington structures. A low-voltage component will be aimed at replacing the cumbersome standard bipolar Darlington structures with simplified command circuitry where slow switching is sufficient. **–Robert T. Gallagher**



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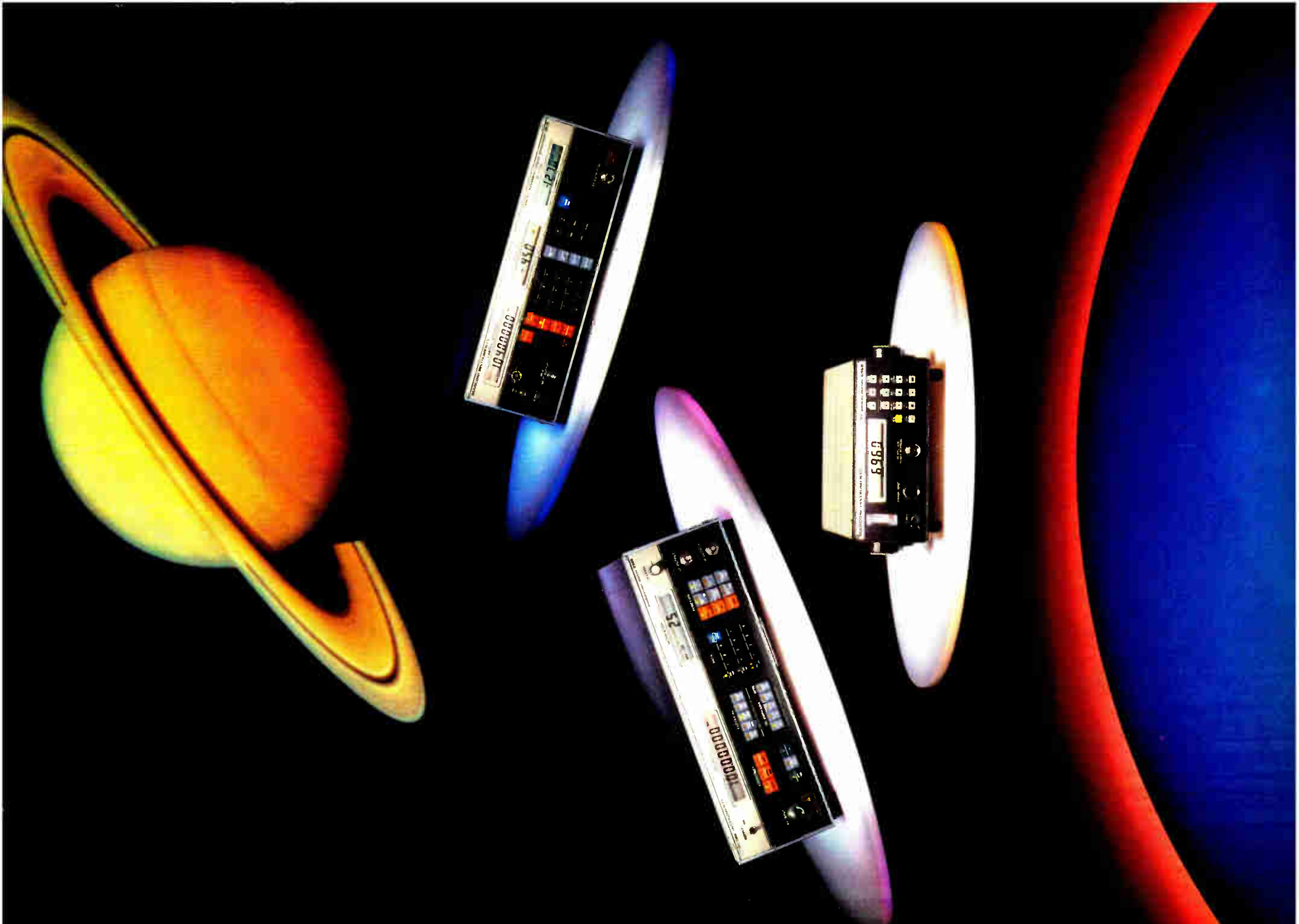

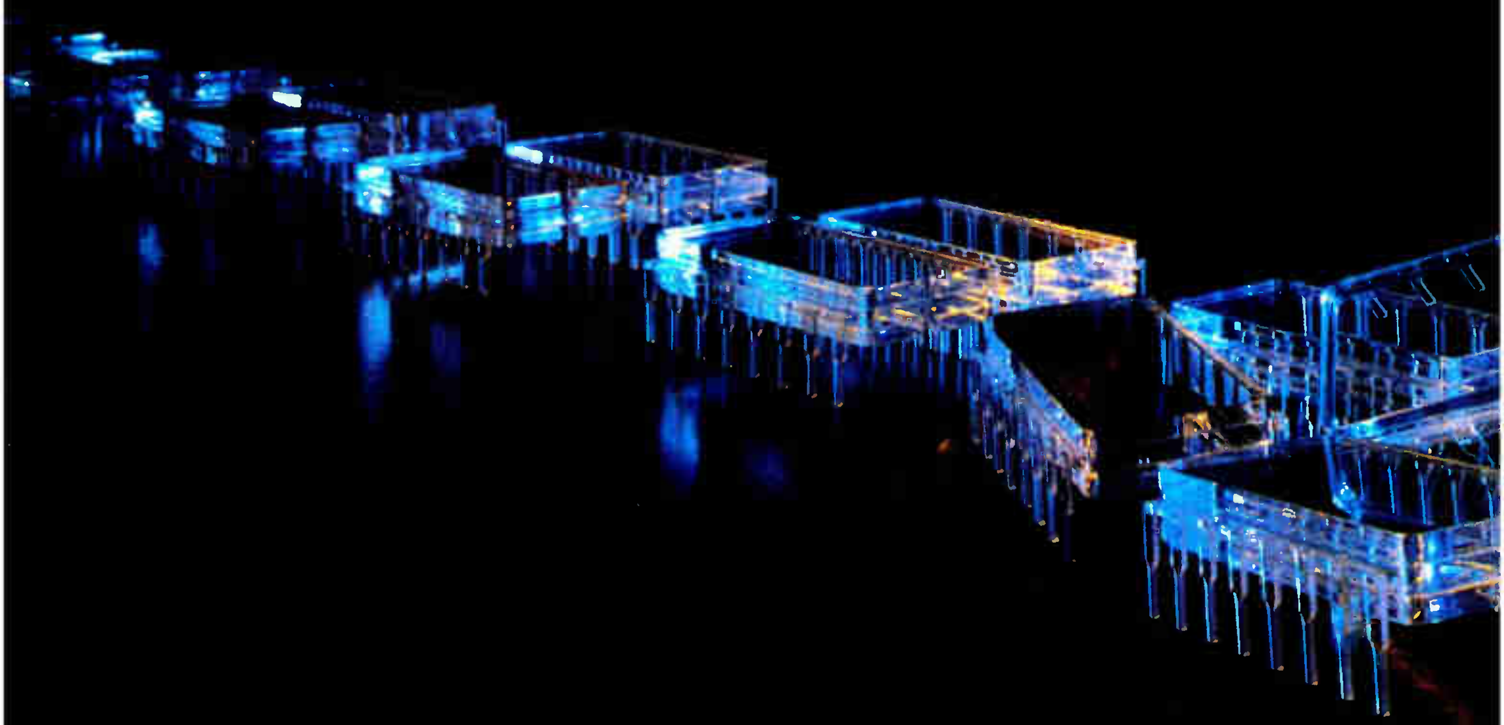

Test Area Manager

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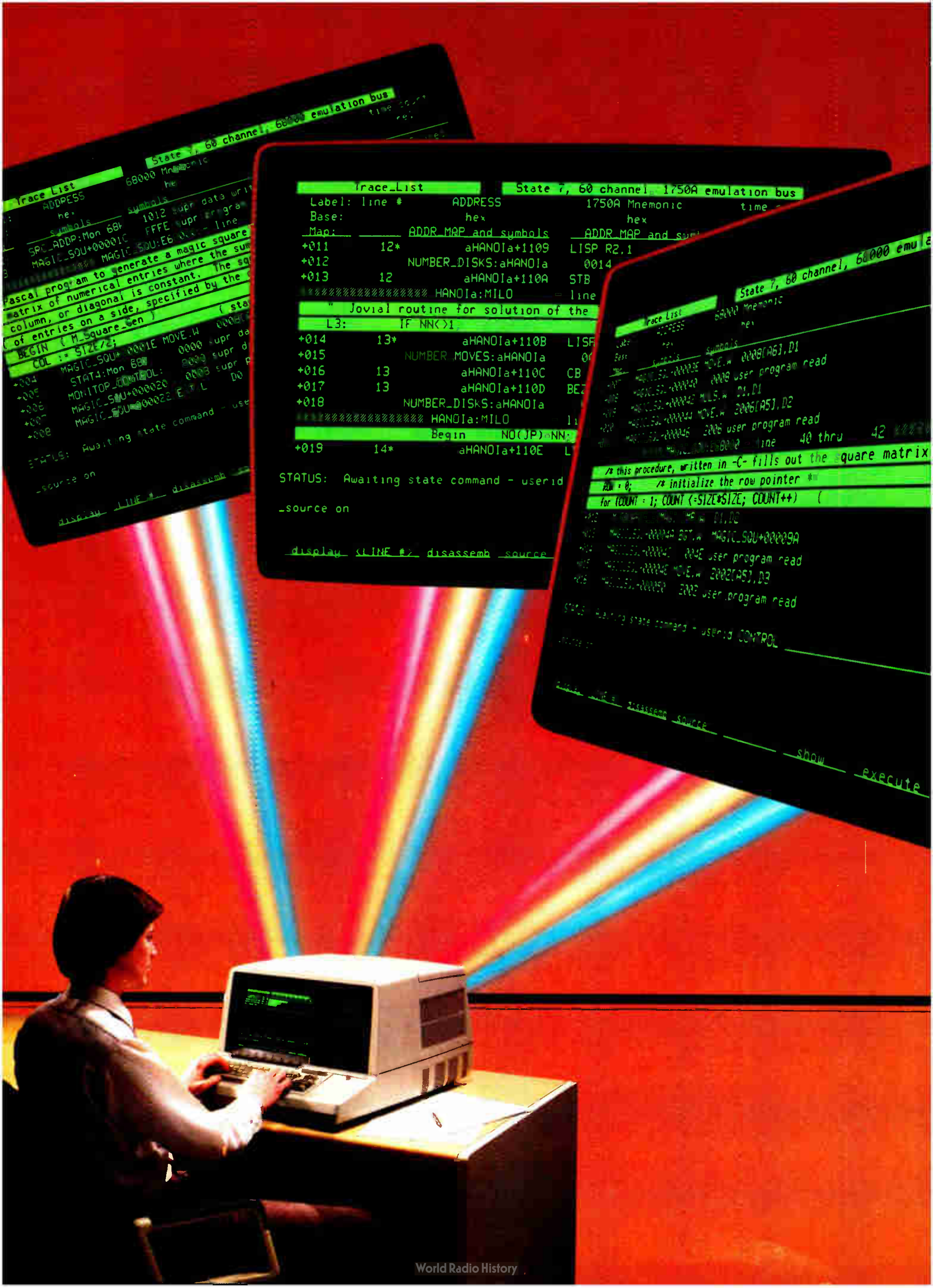
Trace_List
State 7, 60 channel 1750A emulation bus
Label: line #
ADDRESS
1750A Mnemonic
Base:
hex
hex
ADDR_MAP and symbols
+011 12* aHANOIa+1109 LISP R2,1
+012 NUMBER_DISKS:aHANOIa 0014
+013 12 aHANOIa+110A STB
HANOIa:MILO
Jovial routine for solution of the
L3: IF NN<>1
+014 13* aHANOIa+110B
+015 NUMBER_MOVES:aHANOIa
+016 13 aHANOIa+110C CB
+017 13 aHANOIa+110D
+018 NUMBER_DISKS:aHANOIa
HANOIa:MILO
Begin NO(JP)=NN;
+019 14* aHANOIa+110E
STATUS: Awaiting state command - userid
_source on
display <LINE #> disassemb source
/* this procedure, written in -C- fills out the square matrix
/* initialize the row pointer */
for (COUNT = 1; COUNT (=SIZE*SIZE; COUNT++) {
show
execute

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Automate, emigrate, or evaporate

That is the dilemma enmeshing U. S. makers of disk drives as they face the prospect of boosting volume, lowering prices, and raising performance

by Larry Waller, Los Angeles bureau

Building Winchester disk drives, as U. S. disk makers tell it, is the most challenging business in a mercurial industry. Since about 1980, the rule has been fast product-development cycles and many production glitches in turning out a sophisticated unit—all in an environment of heavy demand that cannot be entirely filled, as customers ask for still lower prices. But even as foreign competition grows, many Americans thrive.

Now, disk firms are making yet another crucial and difficult decision, all the more far-reaching since it should influence the shape of drive making for years. It is nothing less than choosing where and how they will manufacture their product—as the catch phrase has it, automate, emigrate, or evaporate.

The first option is to stay in the U. S. The advantages are availability of top engineering talent and proximity to customers; the disadvantage is the need for enormous investments in relatively unproved automated-production technology.

The second option is to go offshore where cheaper labor and material costs and tax breaks beckon. But the pitfalls there stem from distance and culture gaps and their effects on quality. As veteran disk executive Stuart P. Mabon, president of Micropolis Corp., puts it, "Quality control and the subtleties of the manufacturing process are too difficult to coordinate offshore."

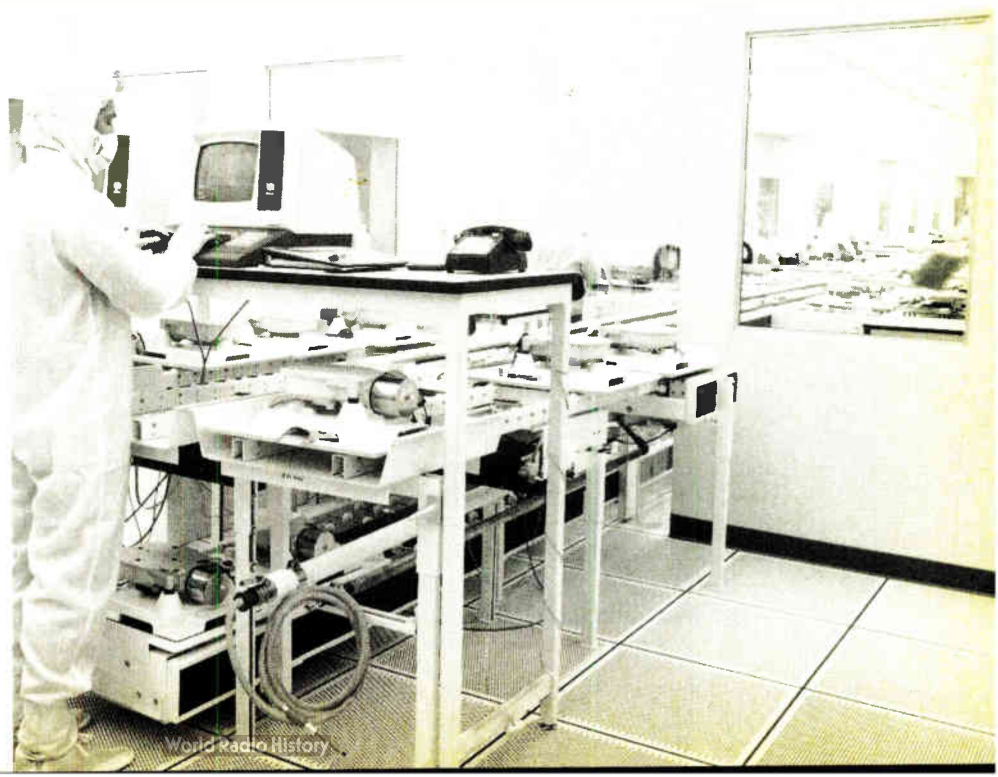
Most drivemakers already have made their decision. Some, in fact, are trying to get the best of both worlds by building low-performance drives offshore while keeping advanced developments at home. Which strategy is best is not yet clear, but what is apparent are market forces that have pushed makers into placing their bets early.

Meeting demand. Foremost is the surge in production necessary to meet demand. "Dozens of firms accustomed to building 5,000 to 10,000 drives a year soon must turn out many times that," says Mabon. Proven, largely manual assembly techniques cannot do that, particularly in the newer high-performance drives of 50 megabytes and up.

The crossover point, when the problem becomes overwhelming, is put at 20,000 drives a month. That rate, now achieved by few, could separate the survivors from those that fall by the wayside, in Mabon's view. "Above that, you're playing in the big leagues and must bring large investments to bear," he says. His Chatsworth, Calif., firm makes bigger drives, and is firmly in the made-in-USA-by-automation camp.

Also on the automation side is Priam Corp., San Jose, Calif., which also manufactures high-performance drives: up to 500 megabytes. In fact, William J. Schroeder, president and founder, thinks the choice has less to do with volume considerations than with "maintaining quality and keeping production and design product engineering tightly linked." He sees these requirements as impossible to meet with engineers in the U. S. separated from offshore plants. Priam is the first U. S. diskmaker to open a new plant designed with the latest automation wrinkles, in late 1983.

Schroeder's beliefs about drive performance determining where produc-



Clean and fast. In a clean room at Priam Corp., which has chosen to invest in automation of its production, an automatic materials-handling system is in use.

tion occurs finds backing from James Porter, industry consultant and publisher of the newsletter Disk Trend Report. Porter divides the business into high performance—closed-loop, voice-coil technology—and low-performance, which is stepper-motor technology. Much of the low-end production already is overseas and virtually all floppy-disk drives are built there, he notes.

Same quality. On the offshore side, the initial high-end drive built entirely outside the U. S. will be from Maxstor Corp., of San Jose, at a Singapore plant that has been turning out subassemblies since last year. To be shipped by the end of 1984, the drive will have a capacity of 65 to 140 megabytes.

Maxstor anticipates no problems, says Ray Niedzwiecki, vice president for operations. "We can produce drives in Singapore with the same quality as in San Jose," he says. One reason was the training: Maxstor brought the core Singapore staff to San Jose first, where they built the equipment, tested it, and then shipped it to Singapore, where they went through the process again.

Also seeing no decline in quality at offshore sites is Seagate Corp., far and away the largest U. S. hard-disk manufacturer. The Scotts Valley, Calif., firm, which shipped 210,000 drives in the final quarter of 1983 alone, finds that quality overseas equals that of the U. S. product and since late 1982 has been widening its Far Eastern commitment. Accordingly, by June, Seagate will make half its drives in Singapore, including all its workhorse 10-megabyte units. The firm does believe, however, that only mature products should be moved offshore.

Another disk-drive maker well into offshore production is Quantum Corp., which in 1983 opened a plant in Puerto Rico, where it builds drives of up to 40 megabytes. The operation is a replica of the Milpitas, Calif., home base, in line with a plan of moving products offshore as they mature.

Distant commands. Whatever the choice, management first has to look closely at a number of issues that are more difficult to judge in advance than the cost of labor or materials. Take coordination and control: nearly all concerned consider the separation of thousands of miles and the unsynchronized working hours as major drawbacks.

An exception is Maxstor, which claims tight liaison through Telex, facsimile, and electronic mail. Moreover, the 16-hour time difference between California and Singapore actually works to advantage "since problems that turn up at one end can be fixed at the other end overnight," says Niedzwiecki.

On the other hand, Priam decided to automate domestic manufacture because it saw three offshore problem areas that it believed insurmountable. First, management and support costs are substantial because engineers must be sent to train local people and help them build a supporting infrastructure. Second, a trained foreign workforce cannot be easily redirected to new processes; this inertia can be deadly to a disk firm that must deal with product life cycles averaging as little as 18 months. Third, the instability of some foreign governments can lead to paralyzing crises.

But another faction questions the panacea of manufacturing automation, at least in terms of the present state of the art. One skeptic is Disk Trend's Porter, who maintains that "the only automation is moving the material around and testing."

Staying modern. However, Priam's Schroeder addresses this question in his new facility by putting all available automation in place today and designing the production lines so robotic assembly techniques can be added as developed. Mabon, of Micropolis, says his company is doing that as well, with robotic advances in labor-intensive assembly operations that could start to pay off later this year. "Of 10 steps needed to fully automate disk-drive production, we're just at the third now," he says.

Decisions to go offshore or stay, although rooted in hard economic data, often can be controversial, too, as they eliminate U. S. jobs. For example, the early March announcement by Tandon Corp., in Chatsworth, Calif., that it will move much of its manufacturing to India and Singapore, at the cost of 1,000 Southern California jobs, caused much criticism there.

Mabon, though, takes a longer view of the present transition. He sees disk drives moving up from simple low-cost boxes to the high-performance peripherals demanded by the new 16- and 32-bit work-station computers. "It's really just started, and a new tier of leadership firms should emerge," he notes. Moreover, he believes U. S. firms had better establish production of high-performance drives at domestic plants, "or we will be another example of equipment manufacturing that has gone away forever." □

Biggest Japanese maker looks offshore—to U. S.

Japanese hard-disk manufacturers have chosen to stay at home and automate, rather than seek offshore savings. But volume leader Fujitsu Ltd. would make an exception if it could find a way to resolve the high taxes imposed by the state of California, where it would like to locate a facility. California's unitary tax, protested by multinational businesses because it levies against profits generated everywhere, not just in the state, is the major stumbling block. Fujitsu might look elsewhere in the U. S., for the same reason firms in Japan keep manufacturing at home: to be close to big customers.

Now operating two hard-disk-drive plants in Japan, Fujitsu plans a third this year that emphasizes production technology and efficiency. Its present volume is easily more than 20,000 drives per month, sources say. Other major manufacturers, Hitachi Ltd. and NEC Corp., say it is necessary to pursue automation benefits, and both are continually improving production lines. NEC agrees with U. S. firms that say that quality control is a critical factor in keeping production at home. Japanese firms already have what amounts to a two-year lead in installing plant automation, according to U. S. competitors, though the level of sophistication is about equal. –**Larry Waller**

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Inside the news

Business abroad

Korea arms for export assault

With a five-year, billion-dollar war chest, four conglomerates will use U. S. know-how and Korean labor to capture world markets

by Michael Berger, Tokyo bureau chief, McGraw-Hill World News

South Korea's four largest electronics firms will invest almost $1 billion in the next five years to storm their way out of conventional components manufacturing and into sophisticated world markets for advanced memories and personal computers. Hyundai, Gold Star Semiconductor, Samsung Electronics, and Daewoo Telecom do have somewhat different marketing plans. But they are all following the same general pattern: hiring Korean technical talent in the U. S., completing product development and testing in Silicon Valley, mass-producing the goods in Korea, and hitting world markets with all they've got.

What they now have is limited. Although Korean exports of conventional electronic components grew 40% last year, to a total of $1.4 billion, the country's efforts to enter the big leagues [*Electronics*, Nov. 3, 1983, p. 110] are just getting under way. Three companies are either constructing facilities in Silicon Valley or have opened them. But only one, Tristar Semiconductor, a subsidiary of Samsung Electronics Co., is producing anything—and only in modest volume: about 10,000 64-K dynamic random-access-memories a month. It is using 5-inch wafers and a design purchased from Micron Devices Inc., of Boise, Idaho.

Tristar predicts it will make 2 million 64-K dynamic RAM chips this year, with sales totaling $10 million. Despite a possible slump in world demand, the firm expects its annual sales to grow to almost $100 million by 1986. According to the company, the reason is that the Micron Devices die size it uses is the smallest and most economical on the market.

Samsung says it wants to start 256-K production as soon as possible but adds that the earliest feasible date will be next year. Since Japan is the competitor Samsung has decided to chase, its best hope may be a market in which that country is not yet strong: erasable programmable read-only-memories. Tristar has purchased E-PROM technology from Exel Microelectronics Corp., in San Jose, Calif., and will begin test production at its Santa Clara, Calif., plant in July (see story, p. 14). Mass production is expected to start early next year.

"We must export [256-K dynamic RAMs] within two years because the captive market and the Korean domestic market will be saturated by then."

Jang-Kyu Lee, Gold Star Semiconductor

Samsung's move to enter the computer market began early this year, when the company inked a pact with Hewlett-Packard Co. to build the Unix-based HP-3000 in Korea. Production will begin late this year, says Young Han Kim, Samsung's senior manager for computer sales, with 40% of the anticipated monthly production of 4,000 units to be marketed abroad by HP. Kim would not reveal a market price.

Like Samsung, Gold Star plans to mass-produce 64-K dynamic RAM chips by next year,though with significant technical assistance from a partner, American Telephone & Telegraph Co., which owns 44% of a joint venture. By year end, the first 64-K dynamic RAMs will come off the line of a new plant now under construction at Gumi, south of Seoul, where Gold Star sales director Jang-Kyu Lee says his firm will also produce Zilog Inc.'s Z8 microprocessor and peripherals.

Says Lee: "Our 64-K dynamic-RAM production will be exclusively for our in-house captive market at first." He expresses little confidence that his firm, or any other firm in Korea, would be able to compete successfully in the world memory market "until we build up our capabilities." Gold Star says that it hopes to have 256-K dynamic-RAM samples ready by late 1985, with mass production beginning in 1986.

"We have a 64-K dynamic-RAM capability now, and we can leapfrog into 256-K if we decide to go into memory."

Sung Kyou Park, Daewoo Telecom Co.

Despite modest expectations for the near future, Lee thinks "we must export within two years because the captive market and the Korean domestic market will be saturated by then." Gold Star's best export bet, he feels, will be the Z8 microprocessor. "Zilog already has trained most of our engineers for production, and our new plant will be ready in May, with equipment installation in June, testing this summer, and samples off the line by October."

U. S. connection. Gold Star is also investing $60 million in a Sunnyvale design center, which is purchasing production equipment for the new plant in Korea. By the end of the year, the new office will be offering custom design services to potential U. S. clients, says Lee.

A third project, designed to give the company a 5-in.-wafer production capability, calls for an $18 million investment in a research and development center near Seoul. A staff of 64 researchers, several of them Koreans hired from U. S. firms, will be complete by the end of 1984.

The most ambitious Korean electronics development project also seems to be the riskiest. Hyundai Corp., the country's largest conglomerate but a company that has no electronics experience, has committed more than $400 million for semiconductor development alone. It is trying to build a new business without embarking on any joint ventures with foreign firms. (Besides Gold Star's link with AT&T, Samsung Electronics has a technology agreement with ITT Corp. Also, Daewoo Telecom and Northern Telecom Corp. have a wide-ranging technology-and-design pact.)

Modern Electrosystems, Hyundai Corp.'s new U. S. subsidiary, is constructing an impressive 120,000-square-foot plant in Sunnyvale but will not start producing 16-K static RAM chips until early 1985, with 64-K static RAMs to follow. The company says it has targeted static RAMs because prices are more stable and competition less intense than in dynamic RAMs.

Modern Electrosystems also hopes to break into the E-PROM market, which it puts at $325 million worldwide by 1988. But parent Hyundai Co. admits that technology-licensing agreements are the only way to achieve this goal. Overtures to that end are in progress, says the company, though it refuses to name names.

At Daewoo Telecom Co., formed last year to handle industrial electronic products for the Daewoo conglomerate, the strategy is somewhat different. Daewoo has established its own Silicon Valley subsidiary, ID Focus, in Santa Clara, Calif. But executive vice president Sung Kyou Park says that his company may bypass the commodity market and concentrate on developing custom designs.

"We have a 64-K dynamic-RAM capability right now," Park says, "and we can leapfrog into 256-K if we decide to go into memory. But custom chips are now roughly 20% to 25% of the world market, and by next year, we estimate that ratio may be 40%." ID Focus was set up to develop in-house industrial designs for Daewoo Telecom and its sister firm, Daewoo Electronics Ltd., a producer of consumer electronics. Park, a former senior research engineer at Schlumberger Ltd., says that his immediate plan is to turn Daewoo Telecom's semiconductor-production pilot plant near Seoul into a full-fledged manufacturing operation. It is scheduled to turn out 800 wafer starts a day for a range of products, including video-cassette recorders and audio tuner components for Daewoo Electronics.

Among Daewoo's newest products is a home computer based on the MSX hardware and software system, which has been adopted by most Japanese makers. Named the IQ-1000, the Daewoo 32-K Korean-language model was placed on the domestic market in late March, priced at $321.

In part, the Korean drive in memories has been fueled by emotion: Korea's desire to free itself from dependence on Japanese suppliers. "Our competitors are not Korean," says C. Leon Kim, executive vice president of Daewoo Electronics. "They are Japanese. We'd like to produce more refrigerators and other items this year because of strong market demand, but we can't get enough integrated circuits from our Japanese suppliers.

"Our competitors are not Korean. They are Japanese."

C. Leon Kim, Daewoo Electronics Ltd.

"One of our executives used to work for a smaller Korean firm. Then, he said, he had no problems with the Japanese. Now that he's working for us, he can't get confirmations on his orders." □

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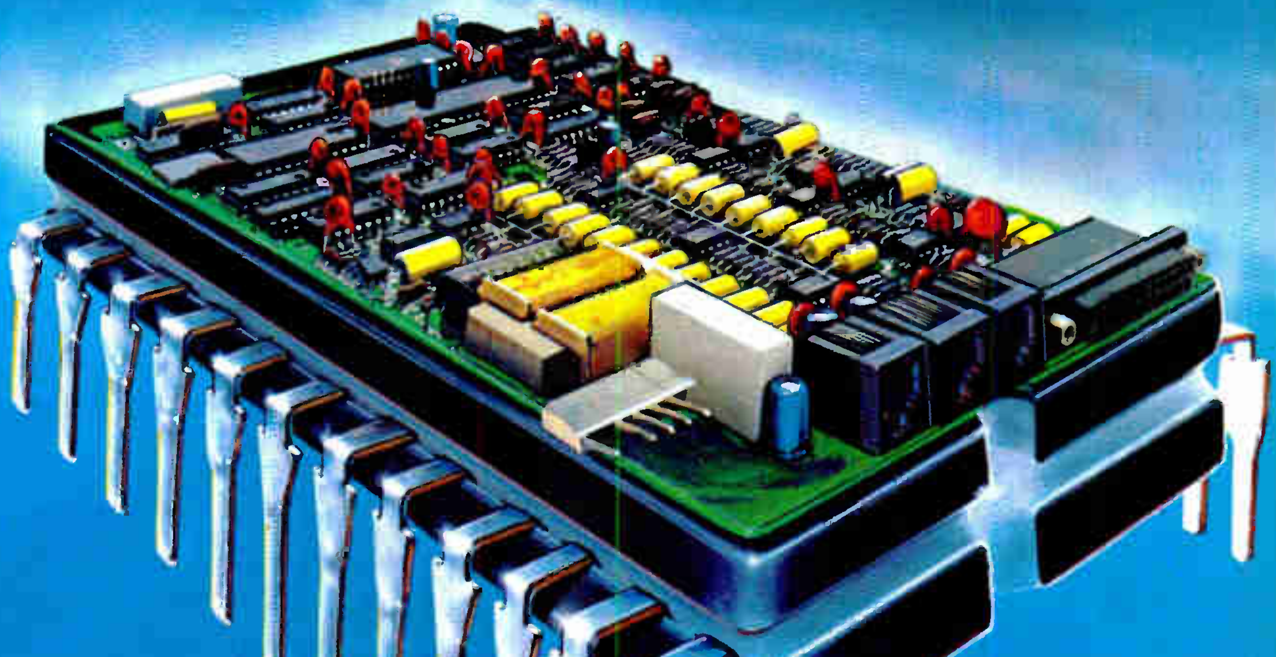

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Business abroad

AEG revives its semiconductor business

Nearly bankrupt two years ago, AEG-Telefunken allied itself with UTC to turn an ailing semiconductor division into a moneymaker

by John Gosch, Frankfurt bureau manager

When financially ailing AEG-Telefunken filed for West Germany's equivalent of Chapter 11 for protection from creditors while reorganizing, a utility company in Heilbronn threatened to cut off power to the company's Semiconductor division should it default on its electricity bill. Only after the division's executives had finally managed to scrape together some money from customers did the utility's owners feel sure that they would get paid.

That episode, in the summer of 1982, points up the crisis the division was facing that year. With its Frankfurt-based parent near bankruptcy and the semiconductor industry in the doldrums, the future seemed bleak indeed for the 5,500 employees at the division's headquarters facility in Heilbronn and at seven production plants in West Germany, Austria, and the Philippines.

In fact, however, the division has managed to do more than just survive. With the help of powerful U. S. allies—Hartford, Conn.-based United Technologies Corp. and its Texas chip-making affiliate, Mostek Corp.—it pulled off a remarkable turnaround, becoming one of the few profitable semiconductor houses in Europe last year. Indeed, with a new emphasis on coordinated game plans, the German and U. S. firms are aiming at a bigger piece of the market.

It all began on November 1, 1982, when years of negotiations between AEG and UTC culminated in the founding of a new company, Telefunken electronic GmbH—TEG for short—in which the U. S. firm and AEG each have a 49% interest and a German banking group a 2% share. The 51% in native hands enables TEG to bid on government contracts as a German firm.

"Had it not been for the participation of a strong outside company, we would have ceased to exist as a viable operation," says Rolf Schlenker, vice president for planning and control and a member of the triumvirate heading TEG. Indeed, few industry analysts had given the old organization much chance of survival.

Versatile. Some of the technologies used by TEG in fabricating selected devices are bipolar; others combine bipolar and C-MOS, bipolar and I²L—and other technologies as well.

But with UTC now behind the German operation, industry observers are optimistic. "Although it is too early for a full assessment, indications are that TEG will keep up its push and become a factor on the market," says Malcolm Penn, of London-based Dataquest UK Ltd., an affiliate of the U. S. market research firm. "Mostek is certainly providing an impetus and new technology."

Under AEG, things had gone from bad to worse. Although the division had many good designs—in the early 1970s it developed Europe's first microprocessor, the CP3-F [*Electronics*, Dec. 12, 1974, p. 33]—it had to make products that its parent wanted but did not do well on the open market.

Further, funds for new projects were slow in coming from financially strapped AEG, so that developments had to be postponed or planned only for the short term. On top of this came the early 1980s' global slump in semiconductors, which led to shorter work weeks for hundreds of workers in integrated-circuit production at the Heilbronn facility.

For all the poor starting conditions, the first year of operations under the new parent constellation turned out to be a successful one for TEG—"in some respects, more successful than we expected," Schlenker says. Total sales last year rose a respectable 11%, to $141.2 million. Of that amount, TEG put some 13.7% into development work, an unusually high amount for the industry.

Besides investing 8% of last year's sales in plant and equipment, TEG acquired 43.6% of Eurosil electronic GmbH, a Munich-based producer of

complementary-MOS ICs, in February 1983. Also participating in Eurosil are UTC and West Germany's Nürnberg-based Diehl Group, with 43.4% and 13%, respectively. What's more, TEG made money. At around 1% of gross sales, its profits may not be overwhelming by U. S. standards, but the figure places TEG among the handful of European semiconductor makers in the black last year.

To have capacity ready for future demands, TEG is drawing up an investment program calling for 70% more funds than this year's program involved. With good connections to a number of German and U. S. banks, the new program's finance seems assured.

Foreign sales. Industry watchers and rival firms in West Germany do not doubt TEG's ability to maintain its upward course. One factor that will benefit the company is its heavy sales outside Germany, for in such places as the U. S. and some Asian countries, demand for semiconductors is likely to be stronger than it is at home. "About half of our semiconductor business is abroad," points out Fritz-Georg Höhne, worldwide marketing director. He expects further expansion of export sales, notably in the U. S., Hong Kong, and Taiwan. "On American markets, a big plus is having UTC as one of our parents," he says.

In tackling their markets, the trio of companies that UTC has brought together—Mostek, TEG, and Eurosil—has a clear-cut product strategy. A technical council consisting of the development chiefs of the three firms coordinates their efforts to cooperate. While the Carrollton, Texas, company's emphasis is on a broad range of very large-scale integrated MOS chips—particularly on memories and microprocessors—Munich's Eurosil concentrates on dedicated products made with standard and low-voltage C-MOS technologies.

As for TEG, "our credo is not to participate in the murderous battles being fought between makers of volume-produced devices, like memories," declares Klaus Bomhardt, vice president in charge of research and development and also one of the troika of executives that is in charge of the firm.

Accordingly, TEG has mostly set its sights on a number of special-product lines in which relatively few firms are competing. The technologies used in fabricating selected ICs are bipolar techniques, as well as such combined methods as bipolar plus C-MOS, standard bipolar plus integrated injection logic, and the like.

This "special-product" (as opposed to "make-everything") strategy has served TEG quite well. In ICs, a noteworthy development is a one-chip radio receiver circuit being sold worldwide. Also important are ICs for TV applications, such as video intermediate-frequency and frequency-divider circuits. Automotive parts, like ignition, directional-indicator, and remote-controlled door-lock circuits, have been generating substantial business, as well.

Optimistic. Rolf Schlenker, buoyed by greater-than-expected sales, thinks that the worldwide components business will keep expanding, with TEG keeping pace as a participant.

In discretes, the emphasis is on optoelectronic devices, power transistors for high voltages, and transistors and diodes for high-frequency applications. TEG is Europe's biggest optodevice producer, claiming a 30% to 35% share of the German and 18% of the European market.

UTC and the three companies it has brought together make much of the benefits the combination is bringing to each partner. To UTC, among the largest industrial enterprises in the U. S., participation in TEG and in Eurosil spells a further expansion into the field of electronics components. The Hartford company had already acquired Mostek in 1979 and set up the United Technologies Microelectronics Center in Colorado Springs, Colo.

Combined with Mostek's European business, UTC's engagement in TEG and Eurosil made the company No. 5 in the Continent's 1982 semiconductor sales, behind Philips of the Netherlands, Texas Instruments Inc., West Germany's Siemens AG, and Motorola Inc.

TEG and Eurosil are counting on their liaison with UTC to help them expand their export business and, particularly, penetrate further into the lush U. S. market. A potentially big outlet for the German-made products is UTC's Automotive division.

No small consideration is the fact that TEG and Eurosil can now tap the combined know-how of Mostek and of the Colorado Springs microelectronics center. Eurosil will especially benefit from a U. S.-to-Germany technology transfer because of its activities in application-oriented MOS circuitry and, notably, C-MOS VLSI chips. In Europe, where Mostek maintains its own sales network, "we throw the ball [orders] in their direction and they do that in ours," says marketing director Höhne.

TEG and Eurosil—with larger markets and with their two German and U. S. parents themselves substantial users of components—expect to have bigger production runs, thus achieving better economies of scale. Also, it will be possible to drop unprofitable product lines. □

NEWSLINE

SGS product expansion headed by top-performance LS404 quad op amp.

An expanded product line that includes one of the industry's widest package selections, increased production capability and aggressive pricing are enabling SGS to make major inroads in the op amp market. One of the most notable developments in the expanded line is the LS404 quad op amp. The LS404 combines SGS-developed bipolar technology and linear design with a proprietary low noise process. An important feature of this device is the patented input stage which remains in the active region even with signals more negative than the substrate. This makes the LS404 particularly versatile in single supply applications, and useful, too, in industrial control circuits. Standard DIP and SO-package versions are available. The new expanded line also includes a dual op amp (LS204) as well as the complete family "LM" and "MC" types of op amps and comparators. Due to SGS' recent investment in fully automated assembly lines, all op amps and comparators are available at significant price breaks with increased reliability.

PERFORMANCE COMPARISON: LS404 vs. COMPETITIVE TYPES

	LS404	RM4156	SE5532A (High Cost)	TL084	LM324 (Low Cost)
QUALITY FACTOR $\frac{BW}{I_s}$	9	3.1	2.5	2.1	2.1
MAX INPUT NOISE VOLTAGE $(nV/\sqrt{Hz})$ $R_g = 10k\Omega$	15	14	6	25	—
HARMONIC DISTORTION (%)	0.04% max @ 1kHz 0.03% typ @ 20kHz	Not Specified	Not Specified	Not Specified	Not Specified
GROUND COMPATIBILITY OF INPUTS	−0.5V (protected against inversion)	$2V_{BE}$	$V_{BC} + V_{CESAT}$	$2V_{BE}$	−0.3V
CURRENT CONSUMPTION I_s (mA)	1.3	4.5	8	5.6	1.5

Single-chip L296 IC switching regulator delivers 160 watts.

SGS ion implanted technology has resulted in the development of a monolithic linear IC that houses all circuitry necessary to build a complete switchmode power supply. The L296's combination of power, performance and space-saving capabilities is already leading to greater cost efficiency in a wide range of applications. The device has a minimum of external components and features an output power stage which can deliver 160W at up to 100kHz. Operating as a step-down switching regulator, the L296 employs pulse width modulation to provide regulated voltages from 5.1V to 40V. All essential control circuitry is integrated in the chip: soft-start, internal precision reference, output overvoltage sensing and a reset signal for a microprocessor.

Dual power op amp unequalled at 1A output current.

A dual operational amplifier/power booster now available from SGS is capable of delivering up to 1A of output current. This figure is unequalled by competitive monolithic power op amps. In addition, the L272 linear IC operates at voltages as low as 4V and as high as 28V. The high-grain, high-power features of the device make it suitable for a variety of applications. For example, the L272 can be used with motor servos, voice coils and in valve actuation configurations. Other performance advantages include full thermal shutdown protection, low saturation characteristics (1V/0.5A), true differential inputs and single or dual supply. The L272 is available in 16-lead powerdip or 8-lead minidip packaging.

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With over 100 new silicon gate fast CMOS functions currently available, SGS is helping to accelerate the jump from LSTTL logic to fast CMOS. The SGS product line offers pin-for-pin compatibility with standard LSTTL, while providing wider supply voltage usage, higher clock frequencies, better noise immunity, and less power consumption. SGS fast CMOS devices feature typical working clock frequencies of up to 60MHz, a power supply range from 2V to 6V, output drive current to 5mA (4mA to 85°C for standard gate, 400mV thresholds and an operating temperature range from −40°C to + 85°C. Typical quiescent power consumption is only 0.01W. In order to remain at the forefront of this new technology, SGS will substantially expand its family of fast CMOS products during 1984.

For more information on the above products, call SGS at 602/867-6100 or write: SGS, 1000 East Bell Road, Phoenix, Arizona 85022.

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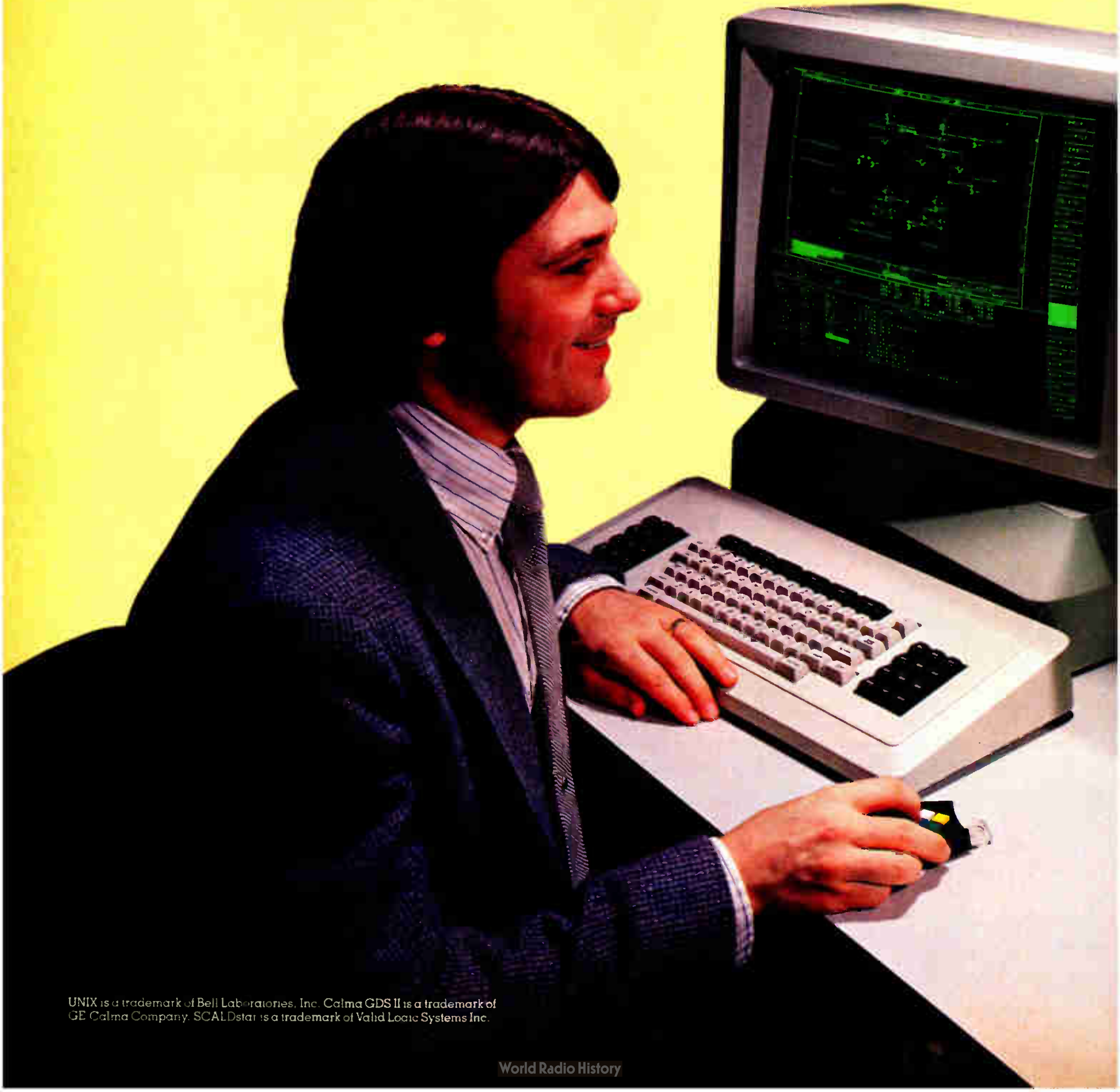

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Satellite broadcasting

Industry pushes for lower-noise LNAs

NEC leads as supplier of GaAs chips for DBS earth stations, but competitors in the U. S. and Europe are eyeing the market

by Terry Feldt, Communications and Microwave Editor

The day may not be far off when millions of rooftops will be peppered with small earth-station antennas for direct-broadcast-satellite television receivers. That portends an eventual market in the hundreds of millions of dollars for the low-noise receivers required for 12-gigahertz DBS reception. Japan's NEC Corp. was the first firm to realize the market's potential, and so far has it almost all to itself.

Cost-conscious. For a consumer receiver, price is paramount, so its designers cannot turn to expensive big antennas to enhance performance. What's more, wind-loading considerations make large dishes impractical for housetops. A much better way to enhance performance is by decreasing the noise figure of the receiver—always prominent in any link budget—and thereby increasing the link's tolerance to interference and fading.

Working to squeeze every decibel of performance out of every dollar spent to produce an earth station is NEC's Microwave and Satellite Communications division, Yokohoma, Japan. According to Kazunori Handa, a supervisor in the device development department, gallium arsenide field-effect-transistor amplifiers for low-noise-amplifiers (LNAS), which are used in low-noise converters (LNCs), will be making continued gains over the more conventional parametric amplifiers, especially at the higher frequencies.

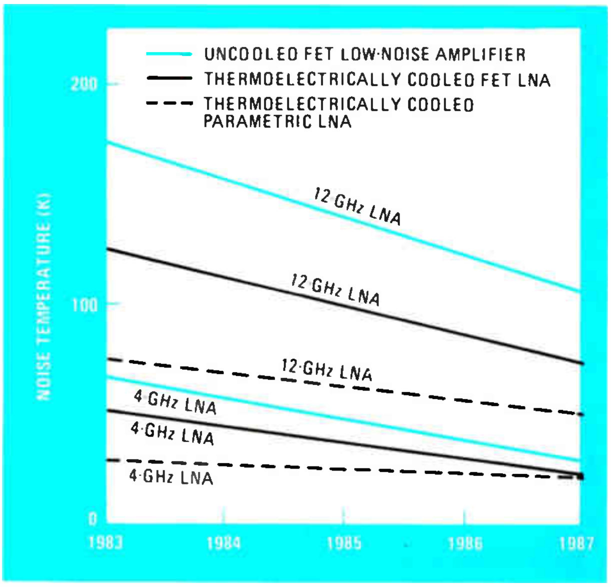
NEC now produces, and continues to develop, parametric and thermoelectrically cooled amplifiers as well as the uncooled GaAs FETs, which "can minimize cost, size, and maintenance," says Handa.

In a paper presented at the American Institute of Aeronautics and Astronautics' Communication Satellite Systems Conference held in mid-March at Orlando, Fla., Handa and four co-authors predict that the noise-temperature performance gains of the newer uncooled GaAs FET LNAs will continue to outpace parametric and thermoelectrically cooled LNAS through 1987 (see figure).

With earth stations, as with TV receivers, "low cost is very important, so uncontrolled, uncooled GaAs FET LNAS are standard," says Handa. Work on GaAs amps continues, he says, with NEC's semiconductor arm in Kawasaki providing the prototype FETs to be used in prototypes put together at the Yokohoma facility. Next on the agenda for NEC researchers is experimental aluminum GaAs FETS with which the firm hopes to accelerate the noise performance of the next generation of LNAS.

NEC, of course, is not alone in the quest for low-cost, low-noise components. In France, the Laboratoires d'Electronique et de Physique Appliquée (LEP) of the Philips group has shown a prototype single-chip GaAs receiver [*Electronics*, March 8, p. 81]. In the UK, Plessey Research Ltd., Caswell, Northants, has a set of three chips—LNA, mixer, and oscillator—in development for the same application. Ray Pengelly, Plessey's manager for GaAs integrated circuits, explains that the chip set, which will become available during the last quarter of 1985, is the predecessor of a single-chip circuit that will follow in late 1986. Plessey partitioned the chip for the initial development in order to optimize each section for low noise. The set has an overall noise performance of about 3 dB.

Closer to home, the Satellite Communications Group of Avantek Inc. has no 12-GHz low-noise components on the consumer market yet, but "we are moving in that direction," declares William LeDoux, product marketing manager. For commercial applications, the Milpitas, Calif., facility now has a product line of 12-GHz low-



Forecasts. Noise temperatures of low-noise amplifiers will continue to improve, particularly for uncooled GaAs FET LNAs that find their way into domestic earth stations for TV reception: both DBS at 12 GHz and TV-receive-only units at 4 GHz.

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Inside the news

noise-block down converters with noise-temperature ratings in the 225-to-285-K range, but it will not reveal the noise performance of its developmental LNCs for consumer receivers.

LeDoux is in fact buoyed by the success of Avantek's C-band GaAs LNC used in television-receive-only installations—and rightly so, with an estimated 5,000 to 7,000 dealers in the U. S. now at work planting the units in a projected 500,000 to 700,000 backyards in 1984 alone. Despite Avantek's past inability to become a supplier for DBS installations, "it would be a natural" for the company with its 10 years of expertise in GaAs FET technology, still to succeed in capturing a significant portion of the market.

On the air. First with DBS services, is United Satellite Communications Inc., of New York, which started a broadcasting service last November. Because no satellite is yet in place for the allocated DBS band (12.2 to 12.7 GHz), United Satellite, like all current DBS operations, uses the fixed-satellite-service frequency range (11.7 to 12.2 GHz).

General Instrument Corp.'s Satellite Systems division won an exclusive contract to supply United Satellite with 1 million home earth stations over a five-year period. When it set out two years ago to meet the contractual demands, the Toronto, Ontario, division went in search of LNCs with a maximum noise figure of 3.2 dB (316° noise temperature). According to microwave systems engineer John McClellen, "At the time, there was no company outside Japan that could consider the quantities, specs, and cost we were asking for. The 3.2-dB noise figure was the edge of technology."

While many firms could produce suitable LNCs in small quantities, only the Japanese had quality LNCs that could be produced in large quantities. The three firms that GI eventually lined up are DX Antenna Co., Kobe; Matsushita Electric Industrial Co., Osaka; and Alps Electric Co., Tokyo. But since NEC supplies the low-noise parts to these firms, NEC is "the real winner in this," says McClellen. □

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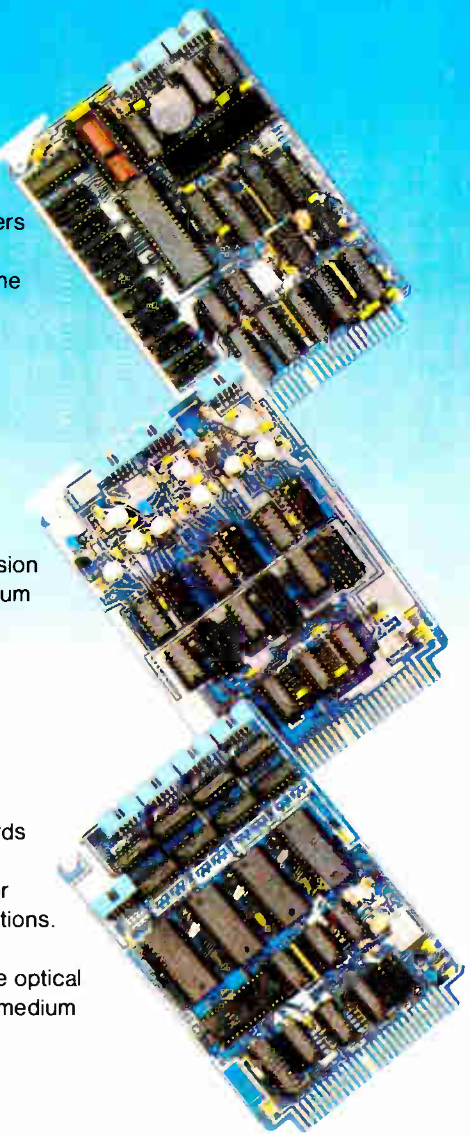

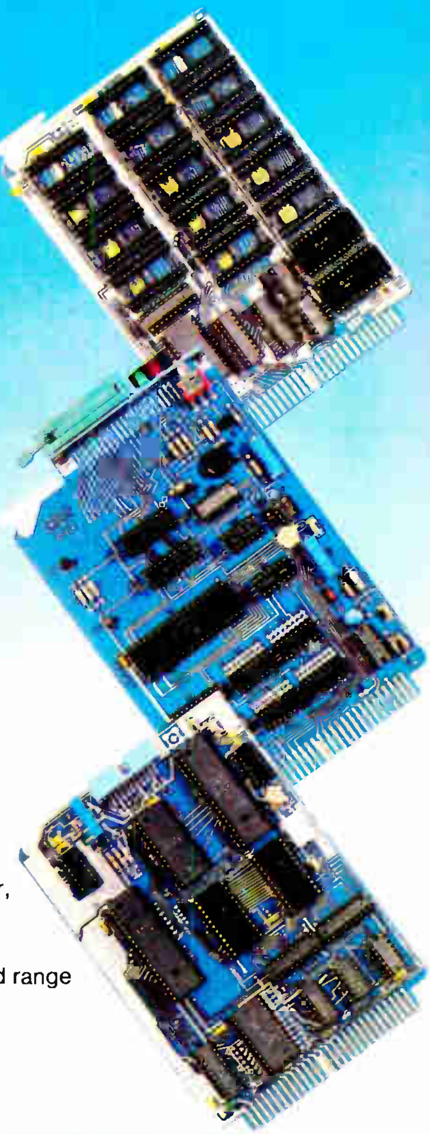

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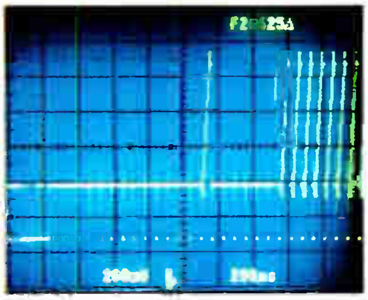

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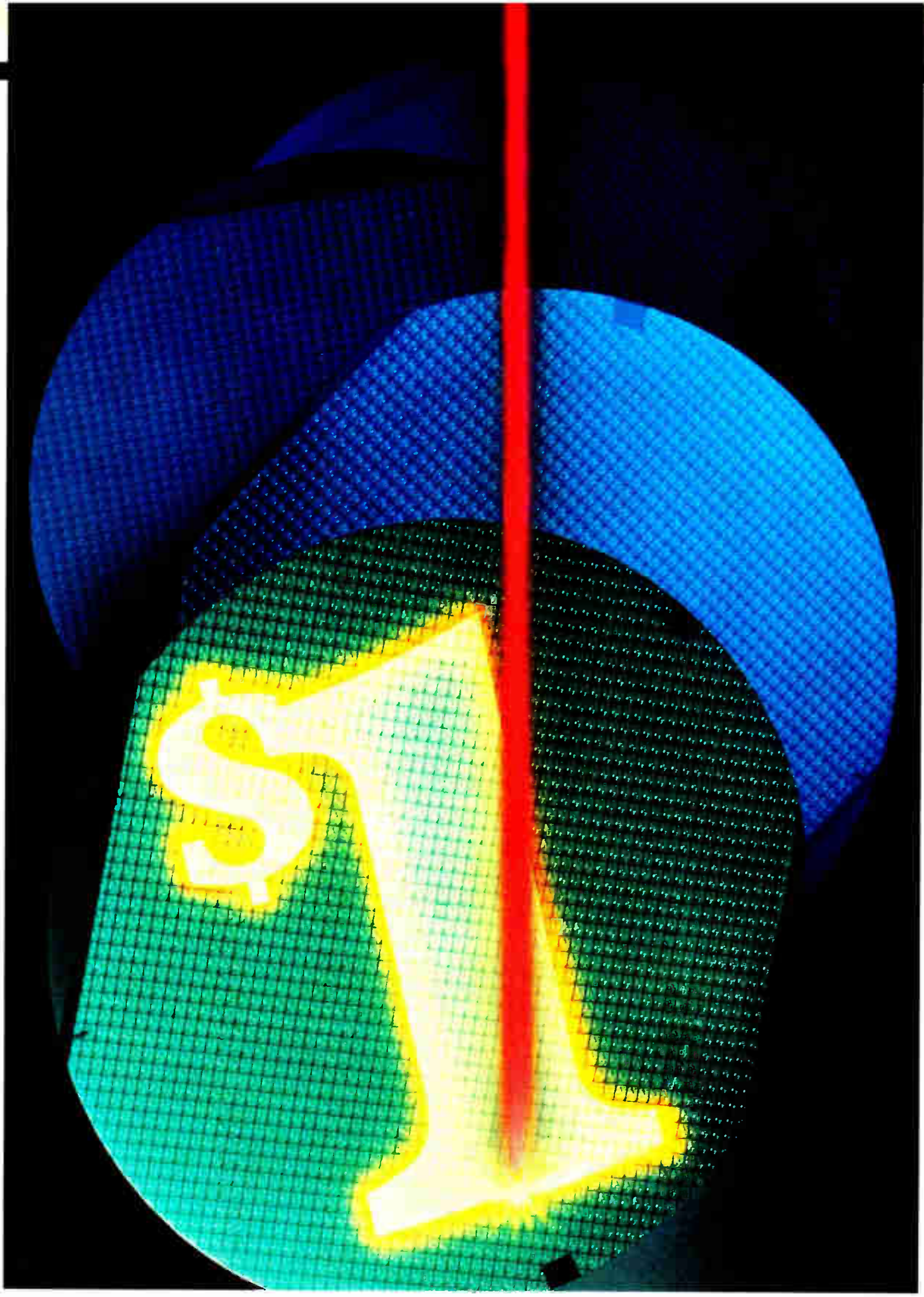

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Circle 121 on reader service card

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Typical performance examples of geophysical, medical imaging and signal/image processing applications.

Application Example	AP-120B	FPS-5410	5420	5430
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2. Tomography Preprocessing	60 sec.	25 sec.	16 sec.	12 sec.
3. Multispectral Image Classification (512 x 512 pixels 8 Bands, 4 classes)	49 sec.	25 sec.	13.3 sec.	10.5 sec.
4. 2D FFT (512 x 512 complex)	3.4 sec.	1.4 sec.	.7 sec.	.5 sec.
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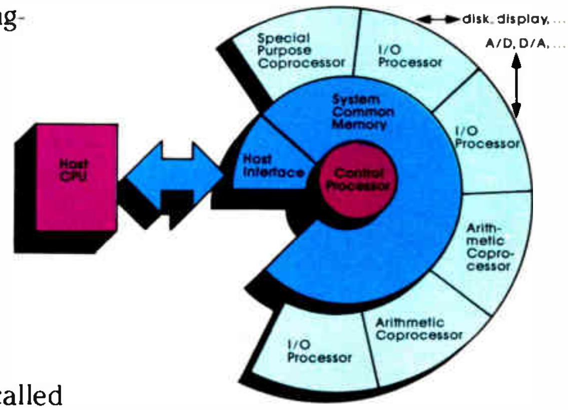
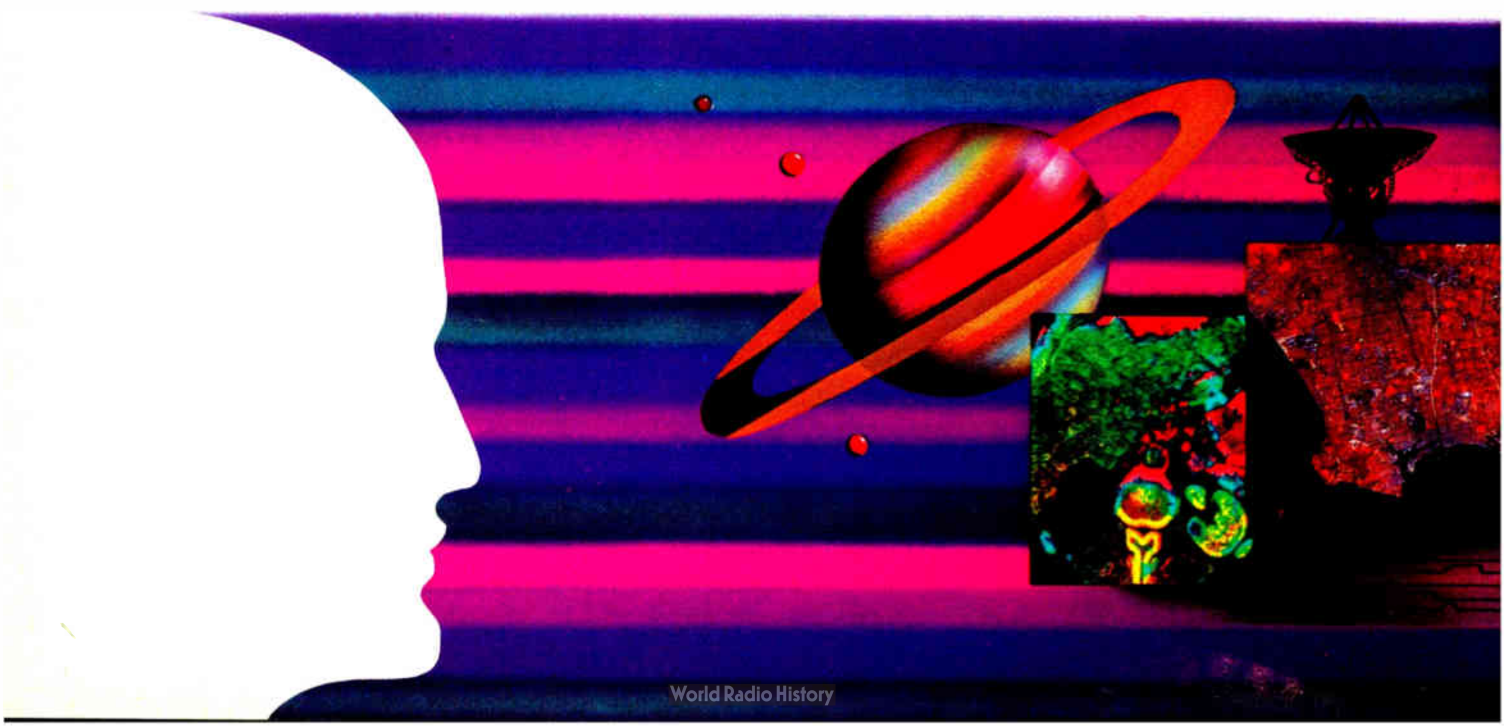
FPS-5000 Series Architecture





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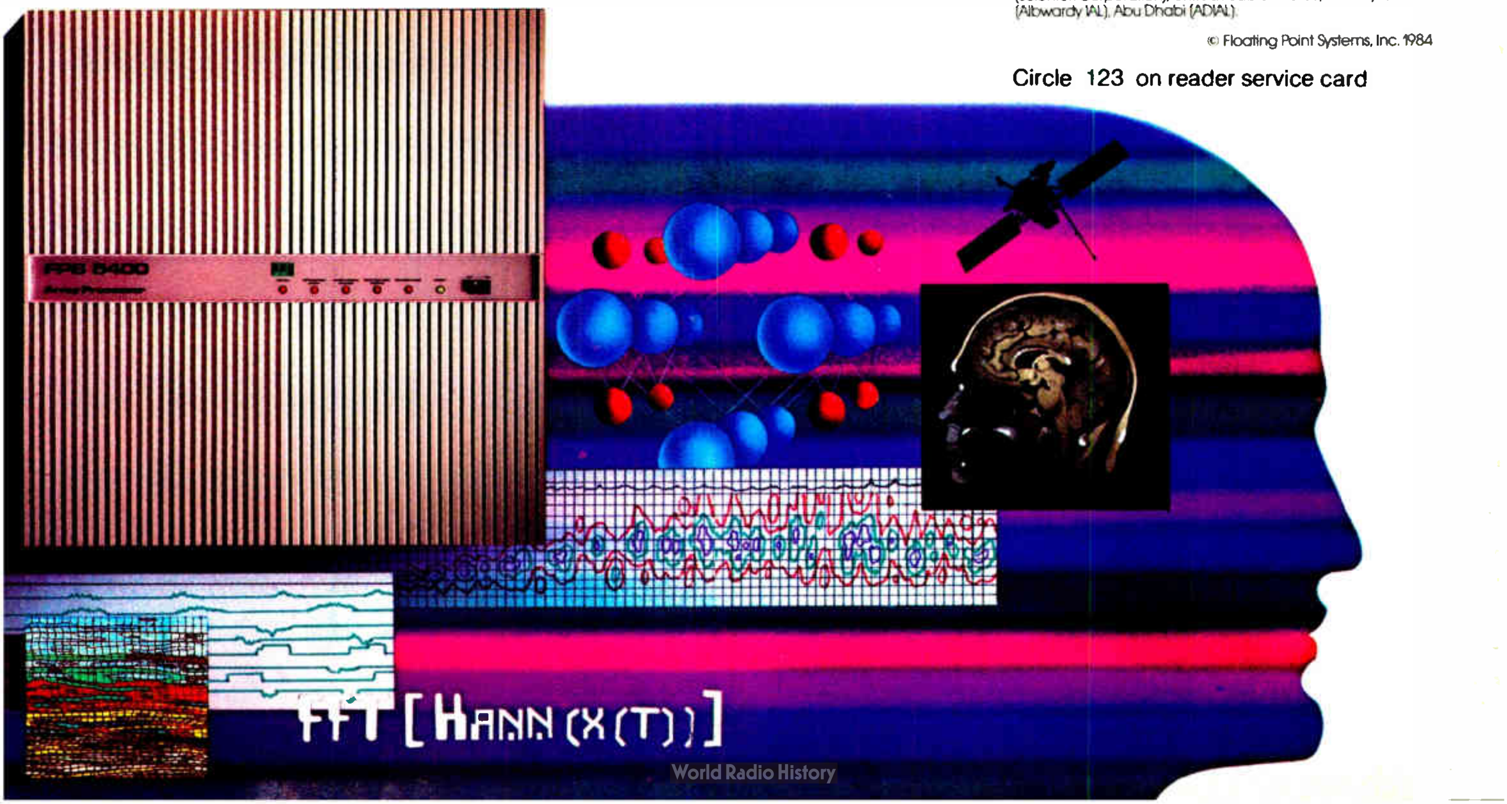

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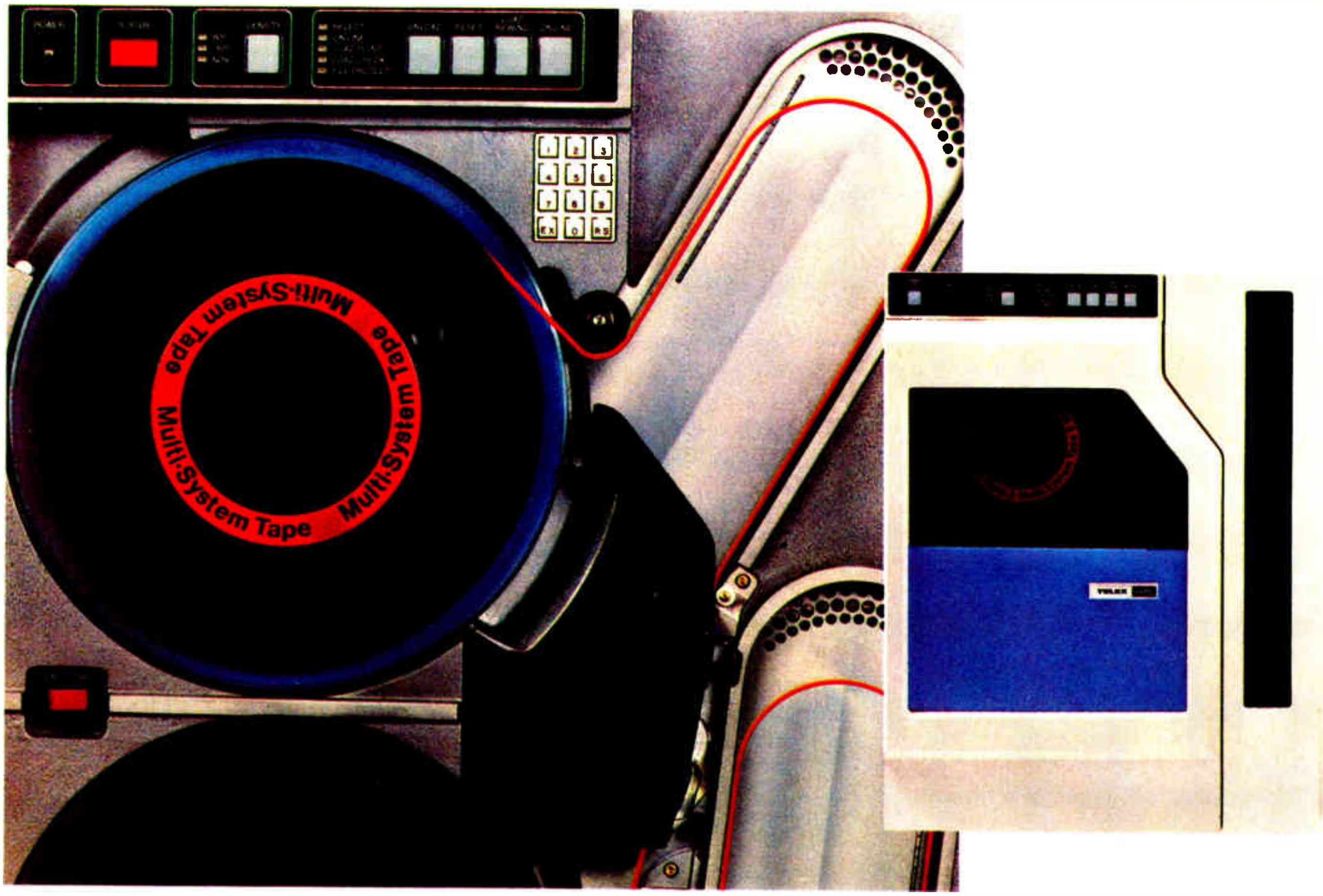

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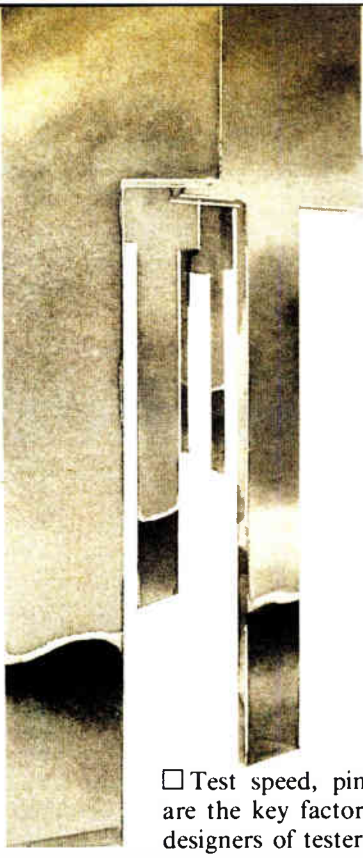


SPECIAL REPORT

VLSI test gear keeps pace with chip advances

More powerful test equipment copes with faster speeds, higher pin counts of very large-scale integrated circuits

By Howard Bierman, *Senior Editor*

□ Test speed, pin count, and throughput are the key factors being addressed by the designers of testers of very large-scale integrated circuits. Advanced Schottky logic and emitter-coupled-logic arrays demand 50-megahertz and higher speeds; increased gate counts demand increased pin counts; and, since throughput is determined by the number of functional tests required to exercise logic, denser chips demand longer test times. Such requirements call for significant advances in the tester state of the art.

Today's VLSI testers can handle up to 300-pin channels, provide complex levels of functional testing, and make provision for interfacing with computer-aided-design and -test equipment. Since a primary function of the VLSI tester is to time-test patterns, signal-timing relationships can be defined precisely with better than 1-nanosecond accuracy. And signal timing is program-selectable and can be changed in real time from one test cycle to the next, up to a maximum cycle rate of 100 MHz.

Fast-moving field

VLSI testers are experiencing a rapid and wide-ranging pace of development, just as the chips they are testing are evolving rapidly. This review of the major players in the field is accompanied by two other articles. Beginning on page 129, Eugene Hnatek, of Viking Laboratories Inc., Mountain View, Calif., delineates the technological trends shaping VLSI testers. Then, starting on page 135, Dean Johnson, of Fairchild Camera & Instruments Corp.'s San Jose, Calif., Analog Test Systems Group, presents a solution to the problem of testing high-performance chips that mix analog and digital signals.

As these articles make clear, the new generation of digital test systems has focused on the pressing issue of design-for-testability. One object of design-for-testability is to reduce programming and test times; another objective is to limit the skyrocketing costs and excessive time needed for VSLI testing. Currently available digital VLSI testers follow the traditional shared-resources architecture in equipment supplied by Tektronix Inc., Cybernetics Technology Inc., GenRad Semiconductor Test Inc., Teradyne Inc., Fairchild's Digital Test division, Takeda-Riken America Inc., and Ando Corp. However, a new test-per-pin architecture was introduced last fall by Megatest Corp. at the International Test Conference. A comparison of key performance specifications for eight major VLSI testers is shown in the table.

A typical shared-resource architecture (Fig. 1a) includes a master clock generator, a number of timing generators (generally fewer than 20) followed by a complex switching matrix to distribute timing signals to waveform formatters, and pin-electronics drivers and comparators. Since a large number of different paths are possible through the switching matrix for ICs with high pin counts, signal delay (or skew) varies for different input/output pin combinations, making calibration or deskewing difficult. Another serious obstacle with shared resources is the lengthy programming time that is required to schedule the routing of timing signals through the switching matrix.

A straightforward arrangement is to provide every pin of the chip to be tested with its own testing resources, or test-per-pin architecture (Fig. 1b). Thus each pin is supplied with a programmable high-speed timing generator, waveform formatter, dc parametric unit, pin driver, pin comparator, and programmable current load. Since there is no longer a need to switch signal routing, greater accuracy is possible. Also, software is simpler and faster to develop, and the tester-per-pin modular structure permits higher pin-count sections to be added conveniently. Shared-resource architecture is less costly, obviously, since less hardware is demanded, but the tester-per-pin approach seems to become more appealing as the complexity of the chips being tested increases.

On-chip testing has surfaced as a viable way of testing VLSI ICs more effectively and will have to be taken into account by new generations of test gear. Called by various names, including scan-path, serial-scan, and level-

SPECIAL REPORT

sensitive-scan-design (LSSD), the technique structures the logic so that its response is independent both of the order in which inputs change and circuit delays between logic elements. Thus the IC is converted from a time-dependent sequential circuit to a combinational circuit. The key advantage is that combinational circuits are responsive to truth-table analysis, while sequential circuits are not, and truth tables can be generated quickly and efficiently by large mainframe computers. Although roughly 20% more silicon is required on the chip for the added test circuits, more than 98% of a chip design can be checked using the serial-scan technique.

Now available

The key to the 100-MHz test operand speed in Cybernetics Technology's Viking 200 VLSI tester is the high-speed computer architecture and manufacturing know-how acquired as a sponsored spinoff of Control Data Corp. The Viking 200, now scheduled for delivery from the Eden Prairie, Minn., company in late fall, will handle up to 256 I/O pins at rates of up to 100 MHz, with multiplex capabilities up to 200 MHz for emitter-coupled-logic characterization. For the purpose of production testing, a 50-MHz Viking 100 is being readied with 20-picosecond timing accuracy and 1-ps precision, capable of handling as many as 128 pins.

As shown in Fig. 2, the testers in the Viking series are composed of three basic sections: a system-control computer, a local network serving as the interconnecting test bus, and one or more test stations. The system controller, which is either a Digital Equipment Corp. VAX-11/730 or VAX-11/780, handles data management, communications, programming capability, and storage of test programs sent to the test stations over the local net. In addition, the system controller performs data analysis on test results.

A second level of computer control is contained at each test station, thus allowing it to operate independently of the system controller once it has been loaded with appropriate test programs. Since different circuit technologies dictate different signal and impedance levels, the pin-electronics section at each test station provides high voltage for TTL and MOS unipolar chips and low voltage for ECL bipolar parts. Instead of mechanical relays, electronic switching is used to provide faster and more reliable testing.

Test stations may be programmed in several languages, allowing users to select a familiar language or one most suitable for a specific test application. A common interface allows a routine written in one language to be called from a program written in another. Languages supported include the Abbreviated Test Language for All Systems (Atlas), Pascal, Fortran, and Comprehensive Tester Application Software (CTAS). The latter language enables inexperienced programmers to create additional test sequences in any of the supported languages, to rearrange the order of sequences, and to modify test specifications where necessary.

The S-3295, from Tektronix of Beaverton, Ore., is a 20- or 40-MHz VLSI test system supporting up to 256 pins and configured as 128 input and 128 output pins, which can be combined in pairs as I/O pins. To handle the diversity of logic types, pin-electronics cards contain provisions for testing MOS, TTL, and ECL ICs, as well as hybrid chips with mixed-logic families.

A high-speed pattern processor in the S-3295 is capable of compressing and recreating functional patterns during a test run, which reduces the system's storage requirements; in addition, other patterns can be switched in or out on a cycle-by-cycle basis. The pattern processor feeds test vectors to each IC pin by the pin-electronics cards. Each pin card provides two input and two output channels and handles I/O switching, output loading, and error recording. Each pin-card data channel is provided with 64-K of local memory, or 256-K per card.

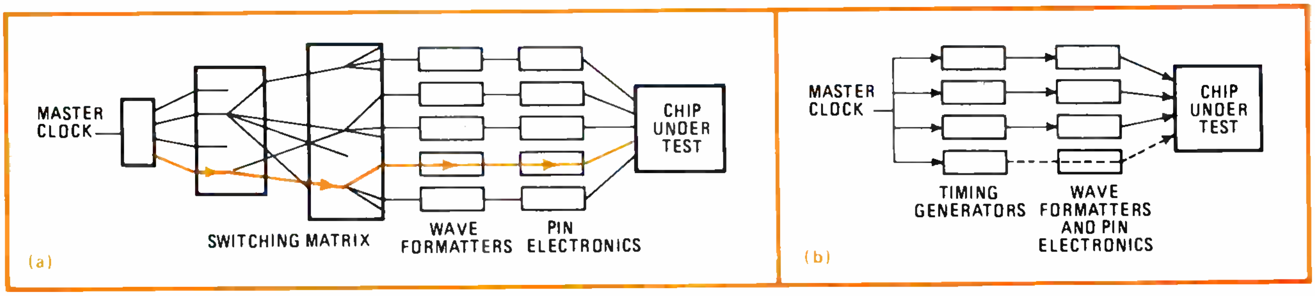
Since fast ICs tend to have fewer pins than slower units, the S-3295 takes advantage of a multiplexing technique to combine the data streams of two adjacent drivers on a pin-electronics card. Although the number of driver circuits is cut in half, two driver pulses can be inserted within one cycle, thus exercising the device under test at double the standard test-system rate, or up to 40 MHz.

The DUT outputs are furnished with programmable active load circuits to allow ICs to be tested under actual operating voltages and currents. For ECL chips, a 50-ohm terminating resistor is connected and the programmable load is removed.

Skewing, or a shift in timing between two signals that should be coincident, is the result of propagation and cable delays, as well as stray capacitance along the signal paths. To overcome this deficiency, the S-3295 uses look-up tables to correct skew differences on every pin card;

SUPPLIERS OF TEST EQUIPMENT FOR VERY LARGE SCALE INTEGRATED CIRCUITS

Manufacturer	Model	Maximum speed (MHz)	Maximum number of pins	Timing accuracy (Ps)	Timing resolution (Ps)	Estimated selling price ($ millions)
Cybernetics	Viking 100 Viking 200	50 100	128 256	20 20	1 1	0.5–0.9 0.9–1.9
GenRad	GR 18	40	288	900	125	0.9–2.2
Takeda Riken	3340	40	256	800	125	0.8–2.2
Tektronix	S-3295	40	128	500	100	0.8–1.3
Teradyne	J941	40	96	1,000	100	0.6–1.2
Megatest	Mega One	40	256	700	100	1.2–2.7
Ando	DIC 8035B	40	256	500	100	1–1.6
Fairchild	Sentry 50	50	256	600	40	0.85–2



1. Different strokes. Traditional VLSI testers (a) feed a limited number of timing generators through a complex switching network to the pins of the chip being tested. In the alternative, tester-per-pin architecture (b), each pin is supplied with its own resources.

this produces pin-to-pin driver and comparator skew figures on the order of 500 ps. For testing serial-scan chips, the S-3295 includes an optional pattern generator backed by a 3-megabit serial memory (1 Mb each for force, compare, and mask).

Separate resources

A bold approach to VLSI testing, taken by Megatest Corp., San Jose, Calif., provides independent resources behind each pin rather than sharing resources, as commonly done in traditional tester designs. Critics of the Megatest concept argue that equipment costs are quite prohibitive and claim that the tester-per-pin architecture is a case of overkill. But proponents of the concept point to significant savings in software development costs and, more important, to the substantially faster test-program development times, which allow state-of-the-art chips to be brought to market sooner.

To test a logic chip, the Mega One [*Electronics*, Nov. 8, 1983, p. 101] feeds it signals simulating the voltage, current, and timing waveforms and states that it would encounter in its intended application. It then compares the output responses with the values anticipated by the designers. Shared-resource architecture makes use of time generators routed though a switching matrix to the specified pins of the DUT, where waveform conditioning creates appropriate test signals for each pin. For small-pin-count devices, shared resources are effective; for VLSI ICs with high pin counts, the test programmer becomes heavily burdened with such hardware details as relay closures, settling times, and path routing. In addition, as the switching matrix becomes more complex, skewing correction becomes more difficult and costly.

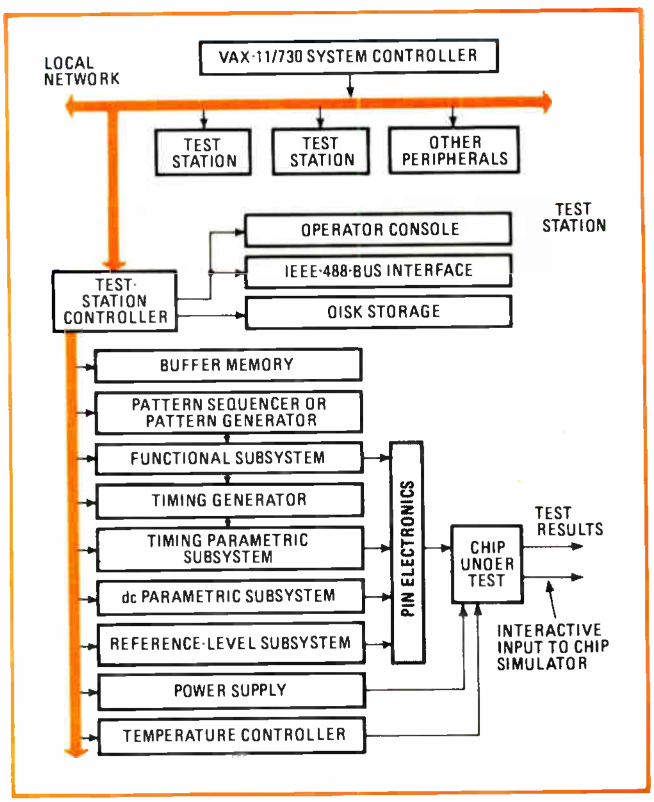
Megatest's Mega One provides each pin of the DUT with its own programmable timing generator, waveform formatter, dc parametric tester, pin driver, pin comparator, and programmable current load. The only high-speed signal routed though the test system is the system clock, distributed to all sections in parallel, without the need for a switching matrix.

Thus signal paths are short and dedicated, allowing precalibration of each pin individually. Since each pin is supplied with its own independent resources, test systems handling up to 512 pins are feasible. Timing and waveform shapes can be changed on the fly at a 40-MHz rate. The tester can operate at 40 MHz on any of its 256 pins and at 80 MHz on designated pins. Software is based on AT&T Bell Laboratories' Unix 4.2 operating system, with test programs written in standard Pascal using Megatest-supplied functions and procedures.

New entry

Early this year, Fairchild's long-awaited Sentry 50 tester was introduced, capable of a 50-MHz test speed (100 MHz multiplexed) with up to 256 I/O pins per test station. The system's distributed architecture is managed by a VAX/11-730 and a VMS operating system: up to 5 megabytes of main memory and 121 megabytes of disk storage, which can be doubled by adding a second disk, are available.

A key design feature of the San Jose, Calif., Digital Test division's Sentry 50 is the local memory section, which has a 64-K-word interleaved main memory and a 1-K-word high-speed subroutine memory. Multiple functional parameters can be passed from main memory to



2. 100-MHz test station. A DEC VAX-11/730 takes care of data management, communications, and storage of test programs to be routed to the test stations of the Viking 200 tester. Over 100 taps along a one-mile run can be handled by the 10-MHz local network.

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subroutine memory by means of a parameter-enable memory. On a cycle-to-cycle basis, this memory determines whether a particular pin is fed functional data from a subroutine memory as constant data or from the main memory as a parameter. Subroutines can be written to compress considerably the vector memory space required for bus-oriented parts, like microprocessors.

Pascal/50, a superset of standard Pascal, is the test-programming language and supports user-defined lists of tester pins. Three Pascal programming techniques are provided to optimize computational loading and cut communications tasks between the test-system and test-head controllers: data packets, elemental procedures, and pin lists. These techniques are said to raise throughputs by as much as three orders of magnitude. To test ICs housing test circuitry, such as the LSSD scheme, a serial-data memory is optional. This reconfigurable memory can generate serial-bit streams at a 50-MHz rate and can be programmed to provide one, two, four, or six channels, which can be routed to any tester pin.

Competitors abound

GenRad's latest entry in VLSI testers is the GR-18, built around a DEC PD-11/44 with an unmodified RSZ-11M operating system. The 40-MHz system from the Milpitas, Calif., subsidiary of GenRad Inc. can test and characterize a variety of technologies, including C-MOS, TTL, and ECL, as well as multichip modules with mixed technologies (such as MOS and TTL) and hybrids with mixed analog and digital functions. Up to 288 pins can be tested using two test heads programmed to operate in a combined mode; each test pin is provided with drive, compare, and load located in the test head. Either 16- or 12-system timing phases, with 125-ps resolution, are available on the fly.

Included in the GR-18 is a serial-data generator for efficient storage of long patterns used with scan-design and bus-oriented chips. A user-interface system provides test operators with easily understood menus to control the various systems modes. Network interfacing is by GenRad's GRnet, consisting of a pair of coaxial lines operating at 655-K-bytes per second.

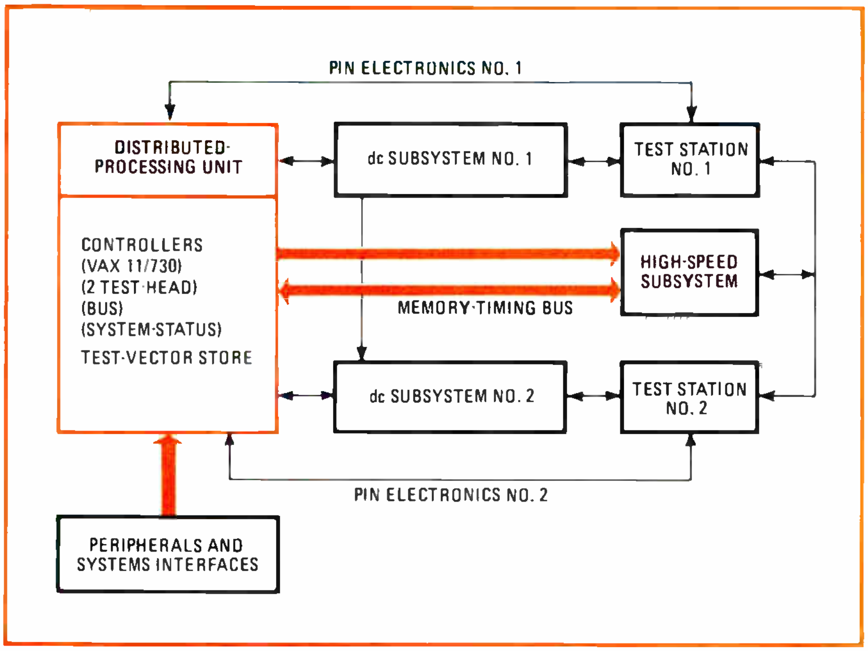
Two Japan-based test-gear manufacturers supplying 40-MHz 256-pin units for VLSI chips are Takeda-Riken America, of Englewood Cliffs, N. J., with its Advantest T3340, and Ando of San Jose, Calif., with its DIC-8035B. Takeda-Riken's T3340 includes two types of pin electronics for either high-speed ECL chips or a high-voltage driver, as well as a high-impedance comparator for MOS and TTL circuits. A four-level automatic-calibration subsystem guarantees test-system accuracy to within 800 ps for the high-speed test station and 1.6 ns for the high-voltage station.

Each of the test pins can operate in any one of 24 drive modes with full waveform-format control, real-time sense control within a test cycle for microprocessor testing, and multiplexed I/O for memory testing. The data-clock rate can be selected in 1-ns increments from 1 kilohertz to 40 MHz, and the timing clock can be set within 125-ps resolution. The clock rate and each of the 32 phase clocks are selectable on the fly for 16 levels of timing values.

For LSSD or scan-path testing, the T3340 can generate primary patterns and scan vectors. Testing is done using an optional superbuffer memory to rewrite portions of the stimulus-and-expected-vector buffer memory. A hold mode is used to store the primary patterns while the serial pattern is being applied and exercised at the chip.

Ando's DIC-8035B 40-MHz system improves throughput with processors for parallel testing of two chips at the same time, the ability to perform up to eight simultaneous dc measurements using analog switching, and a 2.75-Mb/s program transfer speed. The resolution of the timing generator operating from a 500-MHz basic clock is 1 ns; the test rate varies from 1 to 25 ns.

Improved software is the area that Teradyne has pursued since the introduction of its J941 40-MHz tester several years ago. The latest extension to the Woodland Hills, Calif., Semiconductor Test division's Test Analysis Program (TAP) simplifies debugging by its ability to display pattern-generation memories and to allow the user to alter the test program through expanded symbolic editing capabilities. The user can review the contents of pattern memories in binary, octal, or user format and modify programmed formats and timing values. An automatic edge-lock program monitors edge-timing accuracy and automatically compensates for different channel propagation delays. □



3. Computer power. In addition to the VAX-11/730 distributed-processing unit, the Sentry 50 has test-head controllers that are self-contained computers directed by 68000 microprocessors. Up to two test heads can be supported for 256-pin capability.

A merger of CAD and CAT is breaking the VLSI test bottleneck

New computer-aided-design and -testing techniques ensure that chips are testable and cut the time needed to generate and execute test programs

by Eugene Hnatek, *Viking Laboratories Inc., Mountain View, Calif.*

☐ Testing has emerged as the biggest recurrent cost in the production of very large-scale integrated chips and as the bottleneck in the forward march of chip complexity and new-product development. For the complexity created by VLSI transistor counts and circuit functions has dramatically raised the amount of time needed to design and generate test programs.

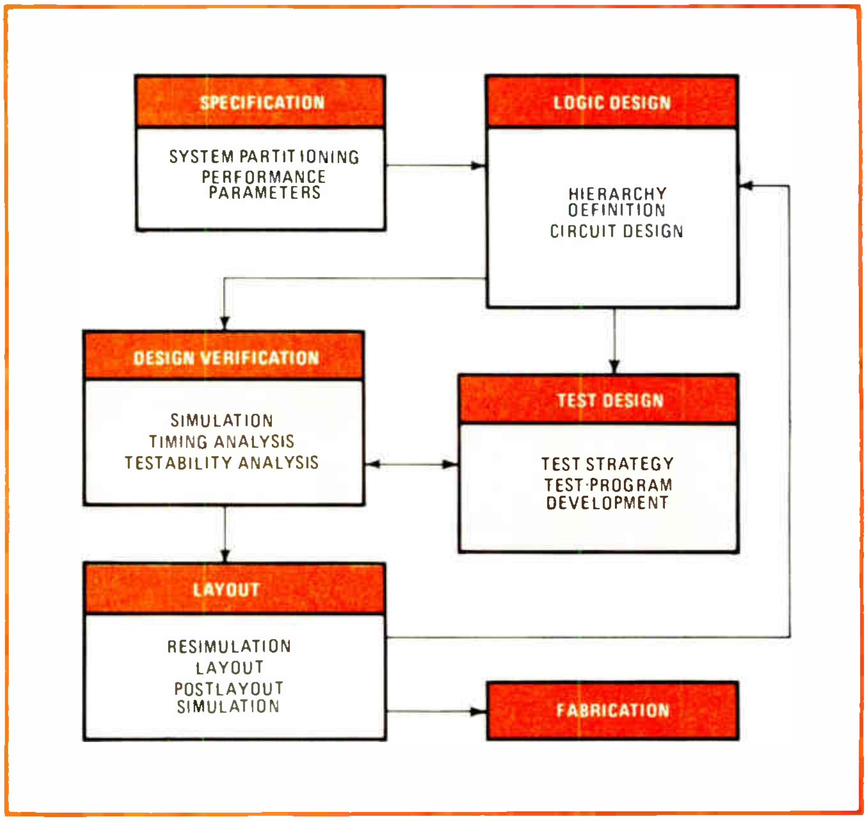
Meanwhile, over the past 10 years there have been great advances in chip packaging and front-end wafer processing, which can at last be fully automated. Testing cannot—neither program generation nor design-for-test methods. In an effort to overcome this bottleneck, test engineers are now developing new techniques to ensure that chips are testable, to cope with their increasing complexity, and to reduce the amount of time needed to generate and execute test programs.

VLSI chips will require a new thought process. No longer isolated circuits, they are now systems-on-a-chip and geared to specific applications. Semicustom and custom circuits will coexist with a few standard integrated circuits, such as array processors, fast multipliers, signal-conditioning circuits, and combinations of memories and microprocessors. But most VLSI circuits will be custom in nature and characterized by many different designs (circuit, processing, and layout), low quantities of parts, sequential on-chip circuits, rapid change, a need for flexible and comprehensive test programs, high density, high pin (input/output) counts, and high speed.

The roles of design, systems, and test engineers are therefore changing. Design engineers must have access to technology menus listing complete systems-on-a-chip. They and design and test engineers will have to design test menus for these systems in partnership, concurrently with the circuit design, if these systems-on-a-chip are to be available in standard libraries.

To help users realize their designs quickly and efficiently, most major IC vendors have established remote design centers throughout the world. Many systems houses are also creating an internal capability for designing ICs and developing software. They will use IC vendors merely as silicon foundries to implement their designs in silicon, and this exponentially complicates the problem of generating tests. Each design will require its own test program, which must be compatible with the vendor's automatic test equipment, as well as the user's.

VLSI chips are being designed by groups of engineers, each working on a part of the chip. The exchange of data from a common data base is essential. To achieve the desired system design, VLSI circuits will be implemented



1. CAD/CAT merge. Interaction between the VLSI design and test groups, mapped out in this flow chart of an interleaved CAD-and-test-program system, must occur in the early specification stage in order to optimize test strategies and ensure device testability.

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with the best design and processing technology. They will contain mixed functions, both digital and analog, fabricated with one or more technologies: n-channel MOS, complementary-MOS, vertical-gate MOS, and bipolar processes. These realities also complicate test-program generation and call for a general-purpose mixed-technology tester.

Beyond redundancy

To increase yields and system reliability, extra elements (redundant circuits) will be common in chip designs. Externally, users of redundant chips cannot detect whether or not they have been repaired with redundant elements, so effective testing is impossible. To help users test these chips, vendors will have to use a silicon-signature technique to identify the redundant circuits used to repair a given circuit. Besides redundancy, VLSI chips will have either a design-for-testability or a built-in-test capability. External parts will be available for this and for on-chip error correction.

Such problems as escalating chip complexity and diversity will surely have to be solved through the clever coordination of automated work stations. Computer-aided design, manufacture, and test will all be required. Through mainframe computers, CAD systems used for chip design will have to be related intimately to the system generating automatic test programs. Ideally, the mainframe should have a resident translation program that would allow the automatic-test-generation program to create test vectors for any commercially available ATE the vendor may own. Figure 1 shows a flow chart of an interleaved CAD-and-test-program system.

Testing any logic chip involves simulating the voltage, current, and timing environment that it would find in a real system, sequencing it through a series of states, and then checking actual against expected responses. Testability is the main issue. In order to come up with a design characteristic that lets a chip's status be determined with confidence and with speed, all of the inputs must be controlled simultaneously, and many of the outputs must then be observed simultaneously, too.

Structural method

To make it easier for users to develop test programs, they will take a more application-oriented, as opposed to component-level, approach. In this structural (or menu-driven variation on a theme) method, the test engineer generates a skeleton, or master, program and then lets the CAD system develop specifics for multiple patterns. This technique reduces test-program development time for such generic product types as gate arrays that have hundreds and thousands of custom gate interconnection patterns for products of a given level of density. The test engineer first generates a test program for a family of chips and then goes on to adapt specific ones to fit the general concept.

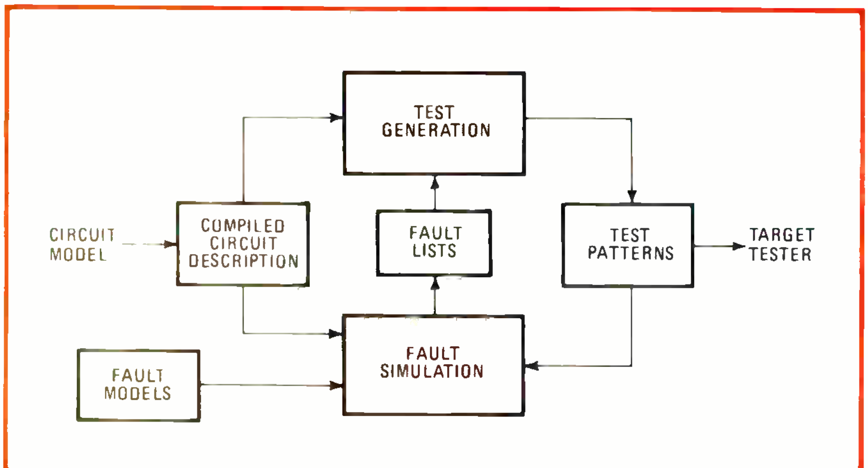
It would be desirable if vendors provided source codes or test vectors, which dramatically cut the time needed to develop test programs but still take up engineering time—to make the vendor's software compatible with the user's ATE. For example, Digital Equipment Corp., in Maynard, Mass., receives 30% to 40% of its source codes from IC vendors. Because programs for different product lines have different formats, the company's engineers must still spend an average of 100 man hours per generic chip type to debug these source codes and adapt them to the DEC environment. Table 1 indicates typical development times for manually generated test programs.

The challenge of testing VLSI chips must first be approached with the attitude that the chip is basically untestable. Solid engineering decisions have to be made about what to test, what not to test, and what depth to test within the constraints of material, capital, and personnel resources. It is no longer possible to review a chip-specification or data sheet, define all possible test conditions, and implement that test.

Test generation involves a search for a sequence of input vectors that cause relevant faults to be detected

TABLE 1: DEVELOPMENT TIME FOR MANUALLY GENERATED TEST PROGRAMS

Chip type	Number of on-chip transistors	Test program development time (h)
Small- and medium-scale integrated circuits	200	120
Peripheral chips	2,000	320
Microprocessors	20,000	1,000
Very large-scale integrated microprocessors	200,000	3,300



2. Design test. A typical computer-aided-test (CAT) system includes a test generator and fault simulator applied to a model of a VLSI circuit developed at the gate level. This figure represents the test-design block in Fig. 1.

on the primary chip outputs. A complete set of functional vectors does not imply an adequate test, however. With VLSI chips, test generation is complicated by buried flip-flops, asynchronous circuits, complex clock conditions, indeterminate states, the needs of circuit initialization, and nonfunctional inputs.

Test generation has a twofold goal: verifying the design of a chip and detecting faults through fault simulation, and the analysis of a given circuit's operation under fault conditions. Chip designers must analyze, classify, model, and test the physical failures of VLSI chips, taking into account the processing technology used to make them. The principles both of physical (chip layout) and logical design-for-testability must be applied, so the resulting circuit will be testable and cost-effective.

The effectiveness of fault simulation, the most critical step in generating VLSI test programs, is measured by the ensurance that the test patterns generated are accurate and that all faults have been detected. The result is usually a full fault-coverage vector set causing long test times. Automating this process with a common design data base, as well as pattern and test-program compression, can cut test times.

A computer-aided-test system is a set of tools to generate and evaluate test sequences for a component and tester by using logic and fault-logic modeling techniques. Figure 2 shows a typical CAT system architecture, an expansion of Fig. 1's test-design block. Logic and fault models have been the only practical ways of generating test programs with exhaustive test coverage for LSI chips, while keeping the number of test vectors to manageable levels.

By tradition, both pattern generation and fault simulation have been based upon quite simple fault models of "stuck-at" nodes or gate inputs and short circuits between nodes. A test pattern is applied to a computer simulation of the logic network. One output from a single gate is simulated as though it had gotten stuck at 1 or at 0. In this case, if the output does not perform as it had done back when no faults were simulated, the stuck-fault test has surely detected a fault.

Many CAT tools are available. The nomenclature has not been standardized, so the tools are sometimes confused and sometimes assumed to be interchangeable. All test tools help create test vectors (the digital inputs and correct outputs of a circuit used to verify correct operation) or test programs (the actual software for the test computer that performs the automatic test). Any logic simulator can verify test vectors created by the logic designer, but fault coverage of the test is not known. Some logic simulators include fault modeling, which gives designers a count of the faults detected by test vectors. The designers can then devise additional vectors to catch undetected faults.

Other CAT tools are used to help create test

TABLE 2: TYPICAL COMPUTER AIDED TESTING TOOLS

Tool	Logic simulation	Fault-simulation/grading	Automatic vector generation	Program generation	Comments
Tegas	Yes	Yes	Minimal	—	Models ambiguous and high impedance states
Logicap	Yes	Yes	—	—	
Lasar	Yes	Yes	Minimal	Yes	Compatible with Teradyne testers, mainly used for printed-circuit boards
Newsim 2	Yes	Yes	—	—	Addresses oscillating faults, models ambiguous and high impedance states
CATS				Yes	
Hilo-2	Yes	Yes			Features hierarchical design approach with functional modeling
Hi test		Yes	Yes	Yes	Compatible with GenRad, LTX, Fairchild, and Teradyne automatic test equipment
Scoap		Yes			Determines circuit's level of testability. Will be incorporated in Tegas 6

Note: All fault and logic simulators model logic 1 and logic 0 states

Creating test programs manually

Engineers develop test programs for integrated circuits in a sequence of steps described below:

1. From vendors and other sources, learn IC organization and electrical specifications, including:
- Functional description.
- Logic functions.
- Controlling signals to each pin of the IC.
- Block diagram of the internal structure.
- Pinout.
- Timing diagram for each critical sequence.

2. Develop the test strategy.

3. Generate test code from documentation:
- Observe signals and compare them with functional truth and logic diagrams.
- Start with simple and basic functional and dc tests to confirm that ICs are behaving properly.
- Include additional tests to exercise remaining IC pins.
- Create more complex pattern and timing tests.
- Debug and refine software.

4. Perform characterization testing to determine which patterns are effective in weeding out faults and which should be used in 100% testing.

5. Generate 100% inspection test programs.

6. Release test program.

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programs. Typically, these tools translate from a higher-order test language into the detailed language of the particular computer the ATE uses. At the moment, however, there is no completely automated method of taking the logic diagram, which performs logic and fault simulation, as well as testability analysis, and then generating the ATE test vectors.

Table 2 summarizes the available CAT tools. Such logic simulators as Tegas and Logcap, the ones most widely used by IC designers, provide fault simulation, which can be used to grade manually generated test vectors but can be very expensive. (Simulating a 1,000-node network for 1,000 patterns costs $10,000 to $30,000.) The quality of fault coverage of the patterns depends entirely on the designer's skill.

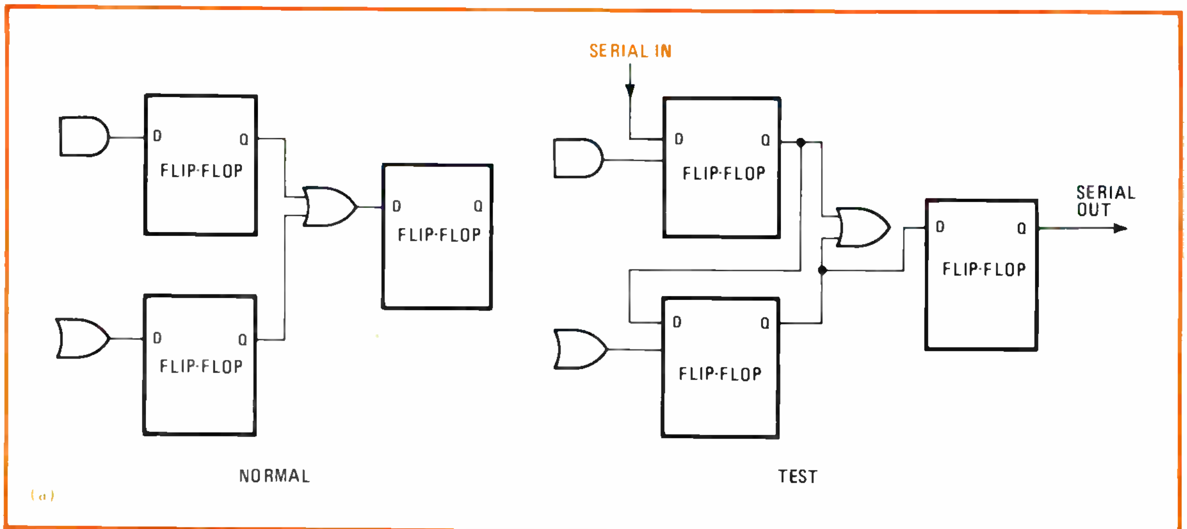
The most noticeable feature of test programs produced by current CAT systems is the absence of pattern structure or intuitive meaning. To handle test problems with the complexity of current VLSI chips, CAT architectures

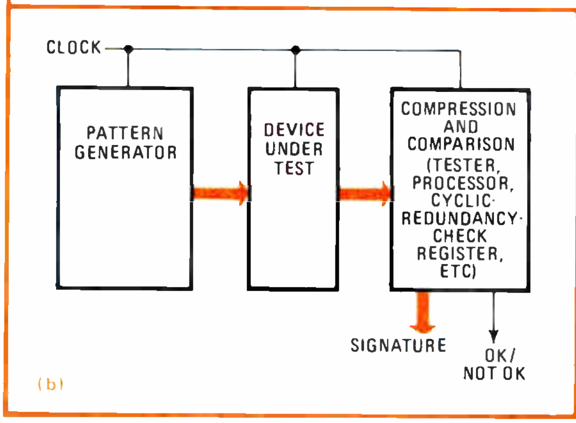
Design-for-test: making sure the VLSI chip can be tested

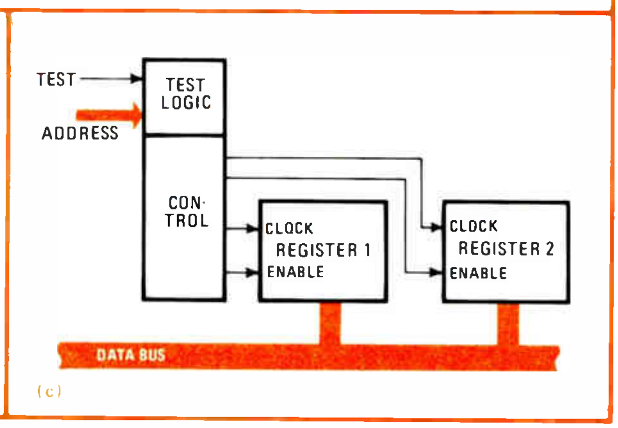
Design-for-test is the process of making a deliberate design effort to ensure that very large-scale integrated circuits can be tested thoroughly and successfully with minimum effort and cost. It is the most effective way of cutting test-development and -production costs.

Design-for-test for VLSI chips was much in evidence during the IC discussion sessions at 1984's International Solid State Circuits Conference, 1983's International Test Conference, and 1983's Fault-Tolerant-Computing Conference. At ISSCC, Toshiba introduced a 256-K complementary-MOS electrically erasable programmable read-only memory with on-chip test circuits; Texas Instruments described a VLSI communications processor designed for testability; and Siemens unveiled a 256-K dynamic random-access memory with redundancy test capability.

The 1983 Fault-Tolerant-Computing Conference featured three papers on built-in test, and 1983's International Test Conference included 15 papers on that subject. The University of Michigan has used on-chip generation of test sequences to produce a 64-K dynamic RAM that tests both the cell partitions and individual cells within an area of the cell array. The U. S. Government's Very High-Speed Integrated Circuit (VHSIC) program is pushing testability, evidenced by an allocation of more than $40 million for built-in







must develop techniques similar to those used by human experts (see "Creating test programs manually," p. 131). At present, no CAT system generates a full vector set without manual intervention.

Test engineers can generate tests that are compact in source form and make use of all the repetition and pattern-manipulation facilities of the ATE. Normally, these tests use more patterns than current CAT systems can generate. Test engineers can also generate tests for circuits much larger than those that current CAT systems can handle. Future CAT systems must contain reference libraries of testing techniques and solutions that can produce and implement test strategies. Such systems will be interactive, so that users can choose alternative algorithms for all stages of test production.

Level-sensitive-scan-detection and other scan techniques (see "Design-for-test: making sure the VLSI chip can be tested," below) promote economical design with low test-generation costs for LSI circuits. With current scan designs, the upper limit of CAT appears to be a few

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and fault-tolerant test development. Recently introduced commercial ICs with design-for-test or built-in-test circuitry include Motorola's 6802, Intel's 2920, National Semiconductor's SCX series, Advanced Micro Devices' AM 29818, and Monolithic Memories' 54/74S818.

All design-for-test methods ensure that a design has enough observability and controllability to provide for complete and efficient testing. An observable node can easily be read from an IC output; that is, the user can easily determine that node's state. Controllability is the ease of controlling (or forcing) a node to a particular value. Complete testing of a logic network involves forcing every node to each logic state and verifying that the node "took" it.

Current design-for-test techniques include serial scan, level-sensitive scan detection (LSSD), signature analysis, unstructured design-for-test, and addressable registers. Scan-design approaches change the difficult problem of test generation for sequential circuits into the much easier task of generating tests for combinational circuits. They also reduce the need to run tests at system speed. With scan-set testing, more than 98% of a given circuit can be tested without resorting to more complex methods.

Serial-scan is a test mode that reconfigures all a logic network's flip-flops into serial shift registers, shown in (a). This design-for-test technique makes all flip-flop inputs quite accessible and all flip-flop outputs observable. Since the rest of the logic is only combinational, test vectors can be generated easily, though tediously. Since algorithms have been designed to create vectors to test combinational logic, the test-vector generation task can be computerized straightforwardly.

When serial scan is added to a logic network using a synchronous single-clock design, a multiplexer is needed on each flip-flop's input. In the worst-case—random-logic design with many clock sources—a second multiplexer and control line are added as well. In IC design, the added wiring associated with the control, clock, and serial string signals has an impact on chip area: an additional 5% for current-mode-logic designs and as much as an additional 50% for random-logic C-MOS.

LSSD is the serial-scan technique that is used by both Sperry and IBM. Instead of the flip-flop employed in serial scan, this technique makes use of a level-sensitive latch as the basic memory element. The serial chain requires the addition of a second latch and clock phase. Since both phases of the clock are independently controlled, users can test for on-chip delays by changing clock phasing and speed with LSSD. The major difference between it and serial scan is that LSSD is more applicable to MOS circuits, since the latch is implemented with only one transistor, and latch-type designs are more common.

The characteristics of the serial scan and the LSSD design-for-test styles are similar. The design-for-test rules are easy to apply, and if they are followed throughout the design, test vectors can be generated automatically and at a low cost compared with manual generation.

Signature-analysis techniques, shown in (b), involve the generation and application of many parallel test vectors, generated manually or randomly and applied to the device. As a result of the large number of patterns, all output vectors are not compared directly with good results, but rather compressed. The compressed result is then compared with the desired one. The technique can be implemented on chip for an effective self-test.

An addressable-register design-for-test, shown in (c), has the same objective as the serial-scan technique—easy access to all storage elements—but achieves it with a parallel bus rather than a serial-shift register. Each storage element (flip-flop, register, and so on) gets an address, so the tester can view all chip storage as elements in a memory with a specific location. The tester then has access to any storage element in one or two clock cycles. Logic must be added either in the control section or at each storage element to map the storage elements onto addresses. If the architecture has a central control block, this addition of logic can be provided for easily and with little area impact; if the logic must be added at each storage element, the area impact could be huge.

Addressable register characteristics are similar to serial scan. Vectors must be generated manually, although the job will be easier than it is for other design-for-test methods, since accessibility and controllability are good. Pin overhead is low and consistent with serial-scan techniques.

Unstructured (or ad hoc) design-for-test—conventional logic design with the later addition of design-for-test—is the dominant technique for today's IC designers. A few rules are applied, like requiring the logic circuit to reset to a known state, breaking long counters, and adding test nodes and pins where needed. In essence, designers must only satisfy their own requirements to create an initial vector set.

Test time is moderate to high, with typical vector counts of several thousand to 100,000. Pin overhead and area penalty are low, since only the features needed for testability are added.

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thousand gates. Scan paths can limit a circuit's performance, and they do not eliminate the need for real-time functional testing. "Requirements for CAT systems" lists the needs of CAT systems; "Problems with CAT" summarizes the shortcomings of the current CAT systems.

Software verification

Once a complete VLSI test vector set has come into existence, the test engineer must then verify that it does everything that it is supposed to do: exercise and test the chip in a way that is both accurate and complete. With test software that has been generated manually, every step (test vector) in the sequence is comprehensible and checked by the test engineer for errors that have been generated manually.

By contrast, the complexity of VLSI test programs and CAD/CAT-generated test vectors makes it unrealistic to check each step in the test sequence manually. Fault-simulation and logic-modeling errors could show up in the automatically generated truth table. The test program must therefore be checked or verified.

One way of verifying the integrity of software that has been generated by fault simulation and logic modeling is to run such programs against a discrete implementation of the VLSI chip. First, the test vectors are fed as inputs to the discrete implementation, and then the outputs are monitored for functionality.

Another method is to use software simulation to exercise the input, output, and associated routines under conditions approximating those of actual test operations, without using the ATE itself. The problem here is that errors contained in the CAD/CAT process for logic modeling and fault simulation are further simulated—and thus they are also compounded.

If software-simulation verification is to be used in an effective manner, the test program must be broken down into chunks that are comprehensible as well as bite-sized. Simulation is used only at those points where the possibilities for uncovering errors are greatest. It is at this stage that experienced circuit designers and test engineers will succeed in generating meaningful tests that are compact, cost-effective, and also capable of uncovering critical design errors.

When small- and medium-scale integrated circuits were developed, circuit-design engineers were isolated from test engineers. That isolation created anxiety and friction among both groups and reduced efficiency as well. A circuit designer was not required to know very much about testing or testability. However, a test engineer was expected to perform as a circuit and system designer, a components engineer, a reliability/quality-assurance engineer, a software expert and programmer, an ATE expert, a failure analyst, a physicist, a chemist, a metallurgist, and a statistician.

Of necessity, the prevailing philosophy of design and test has shifted. From the first, VLSI circuit designs must be conceived with testability in mind and must also provide internal circuit-node points for testing. During the period of initial specification and design, a closer working relationship between design and test engineers is vitally necessary to give testability and design-for-testability equal priority with logical functionality.

The user-vendor interface must change as well. IC vendors covered their LSI chips with a shroud of secrecy, supposedly for competitive reasons. Not enough logic details were given to synthesize the data base, and test programs and vectors were withheld.

Users had little help developing the tests they needed to ensure the electrical integrity of the chips they bought, so they resorted to a brute-force approach based on a functional description of the chip. An open relationship between vendors and users—a relationship based on mutual trust, understanding, and respect—is critical to overcome the enormous burden of VLSI testing. □

Requirements for CAT systems

- Ability to generate program from computer-aided-design logic simulation, fault simulation, and fault verification.
- High flexibility for different circuit functions (both analog and digital) and CAD-to-tester interfaces.
- Easy translation from CAD systems to automatic-test-equipment systems, like those from Fairchild, GenRad, Teradyne, Takeda-Riken, and Accutest.
- Cost effectiveness.
- Rapid program generation based on menu philosophy for gate arrays and custom-cell circuits.
- User-friendly interface.
- A reference library of previous test techniques.
- Interface manipulation of alternative algorithms by test engineer.
- Pattern compression through host computer, performed in conjunction with a CAD system.
- Standard interface and standardized software.
- Design-for-testability implemented in very large-scale integrated circuits. .

Problems with CAT

- Lack of complete documentation on available computer-aided-test systems.
- Test programs lack pattern and structure when algorithms are generated without knowledge of the circuit's overall structure and function.
- Simulation techniques must be developed to permit evaluation of complex patterns without the need to simulate all signal changes.
- Current systems can handle only several thousand equivalent gates.
- Lack of functional-test generation and related design-for-testability considerations.
- Lack of fault-simulation systems with the ability to address multilevel models and functional faults.

VLSI testers ramp up capabilities for mixed-signal chips and hybrids

Full digital timing checks coupled with fast analog measurement check parts that mix analog and digital signals, like data converters and codecs

by Dean Johnson, *Fairchild Camera & Instrument Corp., Analog Test Systems Group, San Jose, Calif.*

☐ High-performance mixed-signal integrated circuits, such as data converters and codecs, require a high degree of flexibility in automatic test equipment in order to reduce the need for user-customized hardware add-ons—and that requirement applies to software as much as to hardware. Moreover, the ATE should be capable of performing fast and highly accurate analog, ac and dc parametric, and functional testing. Digital signal-processing techniques combined with automatic dc calibration and full timing provisions provide the necessary capabilities.

In addition to testing data converters and codecs, a mixed-signal tester should be equally effective in testing traditional analog ICs, such as operational amplifiers, filters, comparators, voltage regulators, and audio circuits. The system architecture should easily interface with external auxiliary equipment, such as probers, handlers, environmental chambers, and bus-controlled instrumentation. Finally, the ATE should exhibit high throughput and expandability and be capable of accommodating new processing techniques.

Mixed-signal testing

The digital portion of a tester must be able to handle four types of devices: mixed-signal ICs, mixed-signal hybrids, and small- and medium-scale MOS and bipolar ICs (table). Many of the key test parameters for these chips are associated with timing and measurement accuracy. Mixed-signal ICs and hybrids, in particular, demand such sophisticated test capabilities as precise timing and accurate ac parametric measurements. The primary testing requirements for SSI and MSI chips are fast dc and ac parametric measurement.

An ATE system drives the inputs and monitors the outputs of the device under test. The system exercises the DUT by transferring test-vector data from system memory to the test head, which interfaces directly with the chip. These test vectors, which define the input data, expected output data, and all associated timing, are transferred to the DUT at the system functional-test rate. Since the system measures the time differential between input transitions and output strobes to determine DUT propagation time, speed and timing accuracy are essential, making these events occur precisely at preprogrammed times.

The test-system timing environment generally is the responsibility of a subsystem composed of a crystal-controlled master clock and several timing generators. An example, shown in Fig. 1, is the General-Purpose Digital Option (GPDO) of the Fairchild series 80 tester (see "Analog and digital ATE in a single socket," p. 137). Here, the real-time clock and address-control unit determines the rate at which a program sequencer executes microcoded instructions stored in an instruction memory.

Operations executed by these instructions include the selection of pin-data formats, pin-data sources, and test periods, as well as the triggering of test-vector burst generation. The master clock also provides the time base for system- and pin-timing generators that create timing edges for controlling the events at the pins of the DUT.

Timing generators

The system-timing generator may be connected under program control to one or more device pins, either directly or as a delayed timing source connected to inputs from the pin-timing generator. The GPDO may have up to four system-timing generators. The system-timing parameters can be changed on the fly under software control. However, the pin-timing generator operates independently of other timing generators and cannot be changed on the fly.

In the GPDO, the pin-timing generators provide seven timing edges for each DUT pin during each test period. The series 80's central processing unit controls these edges. Each timing edge has several timing ranges, with the fastest ranges providing the greatest resolution. Maximum resolution is governed by the master clock's period and a vernier delay circuit with 8-bit resolution.

Two of the seven timing edges are used by the pin-

KEY DEVICE CHARACTERISTICS IN DIGITAL TESTING

Device type	Pin count	Speed	Timing requirements	
			Measurement (ns)	Accuracy (ns)
Mixed signal hybrids	64–512	100 kHz–5 MHz	5–15	1
Mixed signal ICs	16–48	500 kHz–10 MHz	3–8	1
Small- and medium-scale MOS ICs	16–48	5–25 MHz	1–5	0.5
Small- and medium-scale bipolar ICs	16–48	10–70 MHz	0.5–2	0.1

data-formatting logic to control the pin driver's leading and trailing edges; two edges control pin-driver transitions to and from the high-impedance output state used for DUT input/output pin testing, and two control the comparator strobe. The last edge is used to make the comparison data coincide with the expected outputs of the DUT, whose pin-response edges are generated by similar timing generators.

When combined, as in Fig. 2, system- and pin-timing generators bring unique advantages to a mixed-signal ATE system. With an analog chip (containing digital registers) that operates at a few kilohertz, one test requirement might be to check the registers' setup and hold time, which is on the order of 2 to 10 nanoseconds. If the test equipment has only a system-timing generator, it can be set up to provide the required timing accuracy at the low frequency, but the same accuracy at digital frequencies is unacceptable because resolution is lower.

Another way

An alternative is to establish the accuracy of the system-timing generator for the shortest range and to slave a number of pin-timing generators to it. Using the system-timing generator as a coarse control, timing accuracy now remains the same for both millisecond- and nanosecond-edge placement. The actual measurement is performed by a time-measurement unit (TMU), which can measure the delays, widths, and rise times of test-device pin-data pulses.

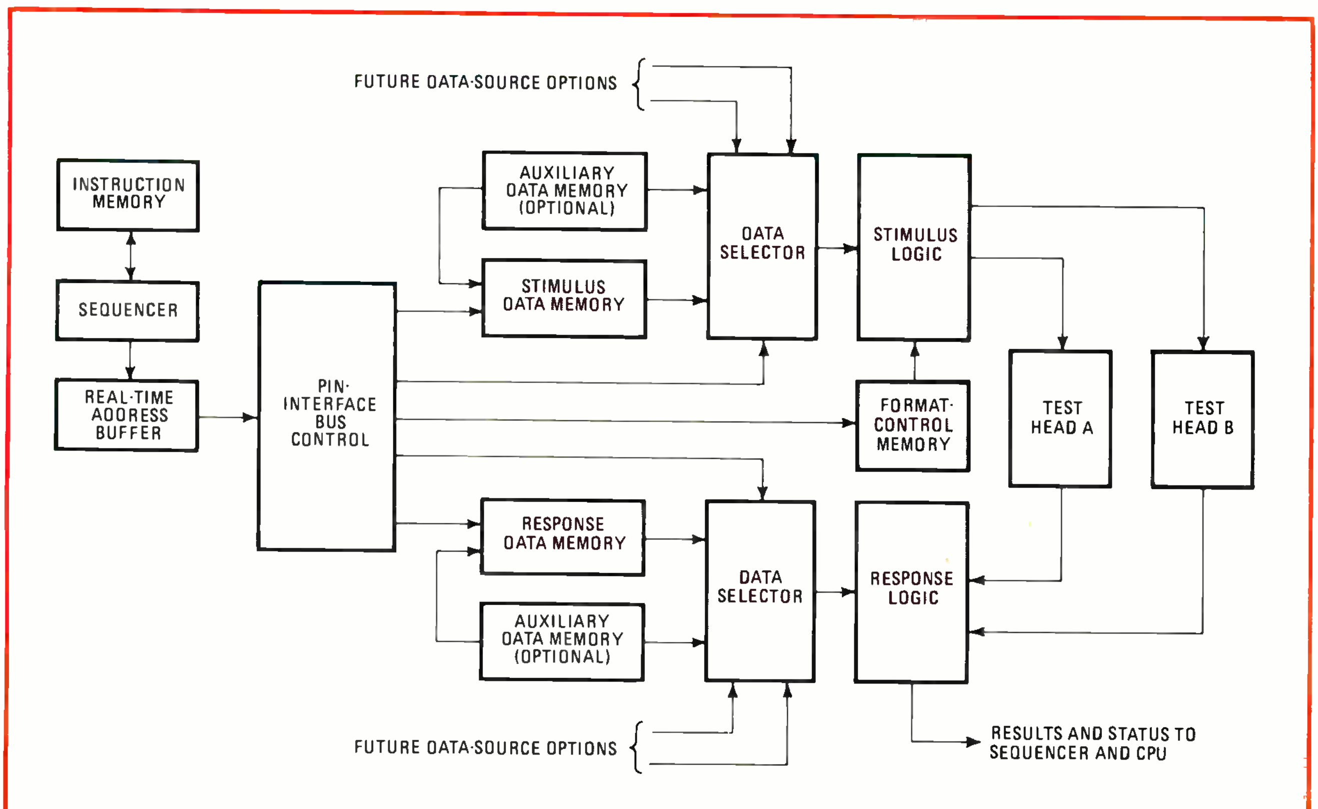
If the system provides independent timing for each device pin, then it can test devices with a different timing requirement for each pin. An example of this would be testing an IC combining MOS, TTL, and analog circuits.

In a mixed-signal system, the accuracy of signal-amplitude and offset measurements is influenced chiefly by the calibration methods used and the hardware architecture. In the GPDO, the system CPU supports automated calibration of all device-pin voltages, timing delays, and pin-driver ramps. Autocalibration is performed at system initialization, when the test program is loaded, and periodically during testing to align dc voltages, timing deskews, and ramp circuits.

Dc calibration uses internal standards traceable to National Bureau of Standards references. For the timing standard, the system uses a length of high-quality coaxial cable with an expanded Teflon dielectric. In addition, a measurement is performed on the cable to determine the gain of the time-measurement circuit.

Traditional test systems use a number of common resources multiplexed to selected pins as required to measure signal amplitude or offset. Pin voltages routed from reference voltage sources on the individual pin-electronics cards may be inaccurate because of slight circuit differences between cards. An alternative to this approach is to use one digital-to-analog converter per pin for all test functions. This architecture allows a more flexible and more accurate stimulus capability.

Another desirable feature for mixed-signal testing is programmable rise and fall times. Without this capability, the pin-driver circuits would either be too fast for C-MOS circuits or too slow for testing fast TTL circuits.



1. Identical architecture. Split-pin capability is feasible with the functional flow architecture in both the stimulus and response sections of the General-Purpose Digital Option of the series 80 tester. The function blocks (tinted) are replicated on the test-head interface cards.

Analog and digital ATE in a single socket

The General-Purpose Digital Option is a Fairchild series 80 subsystem that fully supports testing of digital and mixed-signal (combined analog and digital) integrated circuits. The GPDO hardware has three major functional parts: control and common resources, the test-head interface, and the test head.

The control-and-common-resources (CCR) module contains the control logic, system timing generators, and control memory that govern the overall functioning of the GPDO. Each test-head-interface (THIF) module contains the test-data memories, timing generators, and waveform formatters for each pin of the device under test, up to a maximum of 32 DUT pins. These two modules are housed in series 80 mainframe cabinets.

The number of GPDO cabinets required is a function of the number of DUT pins supported. The first cabinet houses the CCR module and one THIF module, supporting 32 pins. Additional cabinets house added THIF modules.

The GPDO manipulator-mount test head contains the pin-electronics drivers and comparators, supporting power supplies, and optional pulse generators. These units are housed in a half-bay cabinet, which also forms the base for a manipulator that supports the test-head module for use with handlers and probers.

The present design of the GPDO test head supports up to 64 DUT pins. Future designs will support ICs with up to 256 pins. The test head also supports the required analog test functions for mixed-signal chips.

With programmable rise and fall times, the test program can assign these parameters as required for each device pin. Until recently, this feature was available only in digital ATE equipment.

Split I/O pins are another advanced digital test-system technique that is highly valuable in mixed-signal ATE. This capability allows each test-head pin to be defined either as a device input, output, or both. To be exploited fully, split I/O must be supported by a system stimulus-and-response architecture, which, under program control, can be applied to each pin as required.

Split I/O advantages

A split I/O system can increase effective pin counts by as much as 50%. For example, no IC is partitioned to have an equal number of inputs and outputs. Instead, a typical low-pin-count chip has a 30 : 70 ratio of output to input pins—or vice versa for chips with large pin counts. Thus a 60-pin system can in all probability test an IC with from 96 to 100 pins using the split I/O capability. Without timing-per-pin and multiple-bit-per-pin capabilities, however, split I/O cannot fully support the stimulus and response data needs.

In the architecture of the stimulus and response circuitry shown in Fig. 1, the data memory, data selector, and logic functions for the stimulus side of the diagram are almost a mirror image of the response side, the format control memory being the only exception. Under program control, either the stimulus or the response side can be applied as required to any device pin to make it an input or an output. If the DUT has a pin that during the course of its operation functions sometimes as an input and sometimes as an output, then both the stimulus and response sides can be connected to that pin, with each side activated as required. Because the two sides are identical, no functionality at all is lost in the split-pin mode of operation.

The same is true of the timing architecture shown in Fig. 2. Again, the pin-timing generator, multiplexer, and format logic for the stimulus side of the diagram are the same as that for the response side. Consequently, either input or output timing signals can be applied as required to any pin, and no performance penalty is incurred.

Finally, a true split I/O feature should also be supported by a multiple-bit-per-pin capability that offers each test-head pin access to several bits, each serving a different function. In Fig. 2, for example, the stimulus and data memories each store test vectors on a per-pin basis. During testing, each memory supplies either one of two data bits to its associated device pin channel for each and every period. In the stimulus data memory, one bit specifies either a high or low state for the pin driver, and the second bit controls the pin-driver high/low impedance states. Similarly, the response data memory contains two bits used to compare the expected device output state and to mask don't-care DUT outputs.

The system's error memory continuously collects device fail or error data from the DUT output pins during real-time testing. When the test is completed, this data is transferred to the system CPU for analysis. The memory can also serve as a recorder for a learning mode in which the response of a known-good device is stored and compared with other chips of the same type.

System software

Except during real-time testing, the GPDO operates under the direct control of the software executed by the series 80 CPU. The programming language used for the CPU is a natural extension of the series 80 Analog Factor language, with all existing syntax preserved. New commands have been added to control real-time test execution and to specify test configurations, signal-path and logic setups, and stimulus and response test vectors.

Testing throughput is largely a function of system software and its associated architecture. The auxiliary memories shown in Fig. 1 provide up to 256-K of storage depth to the GPDO test-vector memories. The auxiliary memory can be downloaded directly into the pattern memory when switching between test heads holding different devices requiring different test programs. Alternately, upon command from the instruction memory, the auxiliary memory can issue a burst comprising from 2 to 256,000 vectors. Using the auxiliary memory in the burst mode effectively increases test-cycle frequency from 12.5 MHz to about 40 MHz. Both capabilities have the advantage of higher speeds (a 10-million-vector-per-second

SPECIAL REPORT

rate) over systems that reload local memory through direct memory access at a 2-megabyte-per-second rate. Since the GPDO test-vector memories are reconfigurable, they can be used to perform what is called deep serial testing. For example, many logic devices with small pin counts typically include memory circuits that are either very deep and narrow (such as 4-K by 1 bit) or shallow and very wide (such as 1-K by 4 bits). In such cases, the test-vector pattern can be configured by the ATE user to accommodate the unique testing requirements of the device.

A set of instructions stored in the instruction memory controls the operations of the GPDO. This microcode is loaded into the memory by the CPU through direct memory access and is executed by the control sequencer. Each 128-bit microcode word is partitioned into several fields controlling the operations to be performed during a given cycle and the section of the next instruction field.

Two methods for configuring instruction memory are in current use. One approach is to use an instruction for each test vector. However, to avoid prohibitive costs, the number of bits per pin must be limited, at the penalty of handling less powerful instructions. The GPDO approach uses one instruction to set up pin-test conditions and another instruction to trigger a burst of test vectors out of local memory. This method conserves memory space, while retaining a very powerful instruction set.

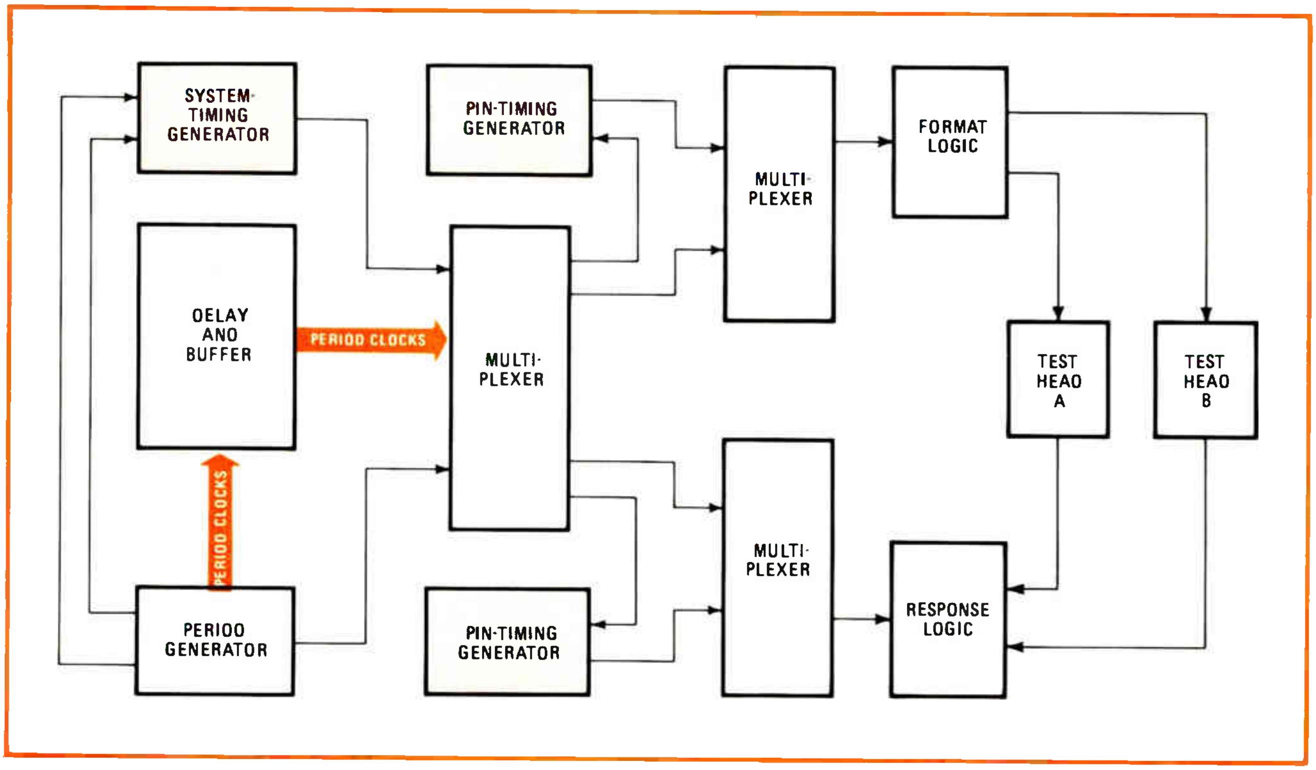
ATE system designers usually partition hardware to reach a balance between ease of manufacture, optimum performance, and ease of maintenance. Some ATE vendors arrive at this balance by partitioning tester functions. This approach, for example, might group all timing-associated hardware on a circuit card or family of cards. The GPDO approach is to partition hardware by pin to provide maximum serviceability, while also optimizing performance.

All stimulus and response hardware associated with a pin or a pair of pins is found in a card-cage assembly located in the GPDO mainframe. The card cage houses three types of pin-oriented circuit cards: test-head interface, pin-timing control, and pin-interface control. The test-head interface cards each consist of local memory, pin timing generators, first-level TMU, multiplexer, formatter, and comparison logic. Each of these cards services two system pins.

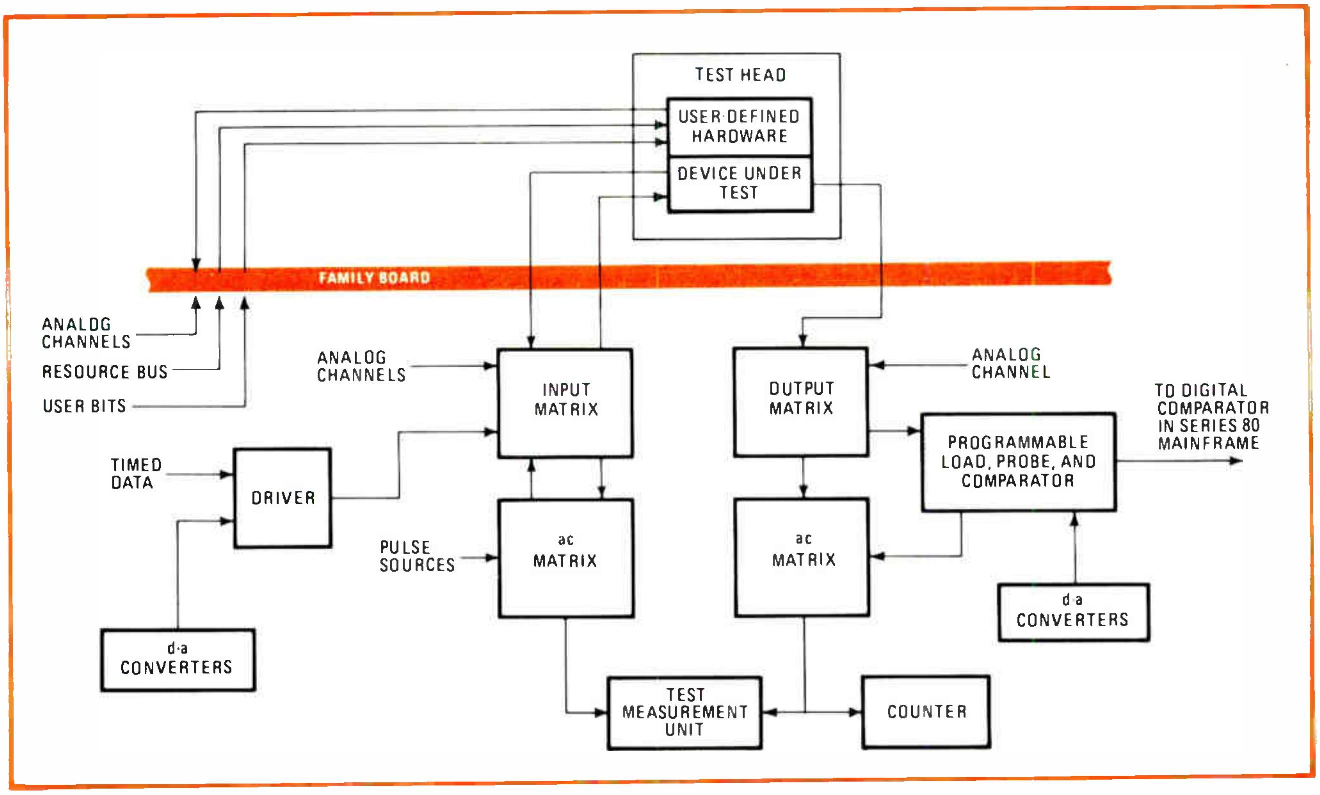
The pin-timing control card, one for each pin, has a second-level multiplexer and control circuits that multiplex and buffer timing signals to the test-head interfaces. The pin-interface control cards, also one for each pin, buffer address and control lines to the test-head interface.

Similar partitioning exists in the test head, which is a separate enclosure. The test head (Fig. 3) houses the pin-electronics assembly and the DUT interface circuits. These circuits are packaged as a single auxiliary test-head interface board plus pin-electronics cards, one for each two pins of the test head. The auxiliary test-head interface board contains the analog references, system probes, a peripheral I/O interface, and an ac scanner. Each pin-electronics card carries the driver, comparator, a programmable load, and I/O matrixes for two pins.

Therefore, any pin-related problem can quickly be traced to one of the cards in the card-cage assembly. If there is a question as to whether a problem exists on the mainframe card or the test-head card, signals at the mainframe I/O and the DUT connection points can be



2. Combining generators. A system-timing generator provides a wide timing range but poor accuracy; pin-timing generators offer high accuracy but poor range. Combining the two in the GPDO results in high accuracy with a wide timing range.



3. Test head. The test head provides all the necessary connection points for attaching any user-defined hardware to the analog portion of the integrated circuit being tested. An audio card is available to test telecommunications circuits.

multiplexed back through the time-measurement system to check the inputs and outputs of any board in order to isolate the problem source.

The test head interfaces directly with the user and thus receives the most abuse. Consequently, about 90% of any system malfunction will be pin-related and quickly isolated to the appropriate board.

Test-head design

One of the most critical aspects of advanced ATE design is the test head, of course. This is particularly true for a mixed-signal system, which must merge the two seemingly incompatible worlds of analog and digital signals. Without capabilities for digital and ac parametric testing, an analog test system generally does not need a test head. Instead, the great diversity of analog testing requirements calls for the support of an equally diverse assortment of user-customized load boards—not only for each different device but for each different application of a single IC as well.

To test purely analog chips, such as operational amplifiers, the user needed only to design a 5-by-5-inch printed-circuit board containing a few discrete components and several other op amps. Other devices, such as analog switches and regulators, required even less circuitry. General-purpose signals were fed to the board and DUT through long cables from the tester.

Today's analog chips are much more complicated and require more sophisticated tester support hardware. For example, a d-a converter requires about a square foot of pc board occupied by complex circuitry. Moreover, the nature of the analog signals involved requires the tester resources to be closer to the DUT. To measure leakage current, for instance, the distance between a picoammeter and the DUT must be as short as possible. Thus the increasingly stringent requirements of evolving analog devices have forced analog ATE designers to move their system resources closer and closer to the DUT—where digital resources have been all along.

This trend has culminated in the GPDO test head, a true mixed-signal design that minimizes the need for user-customized hardware and for the first time combines advanced test capabilities for single-insertion, single-shot ac and dc parametric analog and digital testing. The test head has two 50-ohm ports per pin; to these ports, a variety of external devices can be connected, including pulse generators, function generators, waveform analyzers, counters, and rf generators.

For testing the analog portion of an IC, a test head provides all the necessary connection points for attaching any user-defined hardware. Depending on the degree of accuracy and performance desired, interconnections can be made using anything from plain wire to semirigid technology, such as a microstrip board.

Both high-quality digital and analog support circuitry are available to the DUT socket through the expansion bus. An example of the combined power of sophisticated digital and analog test circuits is an audio card that allows the GPDO to test telecommunications circuits. For this application, the GPDO provides digital accuracies at analog frequencies. This capability is equally valuable for testing voltage-to-frequency and frequency-to-voltage converters that handle analog signal frequencies down to 10 hertz. □

Touch screens let your fingers provide a fast, simple entry into the computer

Resistive, capacitive, acoustic, and optoelectronic touch screens make the computer available even to untrained users

by Elisabeth Panttaja,
Electro Mechanical Systems Inc., Champaign, Ill.

☐ The search for easy-to-use alternatives to the traditional computer keyboard has led to such recent developments as the touch screen (Fig. 1) and the mouse. The touch screen has already received considerable hardware and software support, and touch technology appears likely to experience strong industrywide growth. In view of this situation, industry observers and systems designers should become knowledgeable about the benefits and drawbacks of the four types of touch screens; how they stack up against the keyboard and the mouse; touch-screen applications; and the touch screen's likely place in the future.

Basically, in a touch-screen system, the user presses a finger against a cursor, number, letter, or symbol on the display screen to initiate a computer command. Currently there are four ways to sense touch—resistive membranes, capacitance sensing, acoustic sensing, and optical sensing. There has been some confusion over the merits and shortcomings of the four touch-sensing technologies and over the types of technology best suited for particular applications and environments. Although recent improvements have alleviated some of the problems, each method has advantages and disadvantages, of which a systems integrator must be aware.

A touching subject

In Fig. 2's resistive-membrane touch screen, two translucent Mylar sheets are placed over the cathode-ray tube. Wires are etched into each sheet. Electrodes going in the X direction are on one sheet, and electrodes etched along the Y axes are on the other. When a finger or stylus presses the surface sheet into the second sheet, behind it, the contact between the two shorts a pair of electrodes, and the XY coordinates of the contact point are transmitted to a host processor.

Resistive-membrane technology can achieve a very high resolution. The whole contact area made by the stylus is averaged out so that, with a little practice, even a bulky pointing device, such as a finger, can execute the fine movements required for cursor control. In addition, because the user must apply firm pressure to the surface to produce a "hit," the system is less likely to be triggered accidentally.

However, the resistive-membrane approach has two serious flaws. The Mylar sheets are easy to scratch and puncture with long fingernails and other sharp objects. In addition, coffee and soda spills are potential hazards, so the system is not considered practical for use in public places or in industrial environments.

Critics of the resistive approach also claim that the plastic film is difficult to attach securely to the CRT and

1. Sans keys. The touch screen can eliminate the keyboard in certain applications. Electro Mechanical Systems' Touch Information Display was designed from the ground up as a touch-sensitive terminal. One microprocessor controls both terminal and touch functions.

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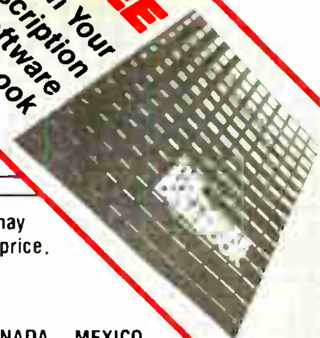

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thus its position is liable to shift over time. Elographics, Inc., Oak Ridge, Tenn., has solved this problem by form-fitting a ¼-inch-thick glass plate over the CRT. A transparent, conductive grid of indium tin oxide is then pyrolitically sealed onto the glass, and voltages pass along the grid in both the X and Y directions. A sheet of Mylar over this grid, then, is used only as a voltage probe, so that potential slippage will not affect the functioning of the system.

Capacitance and acoustic sensing

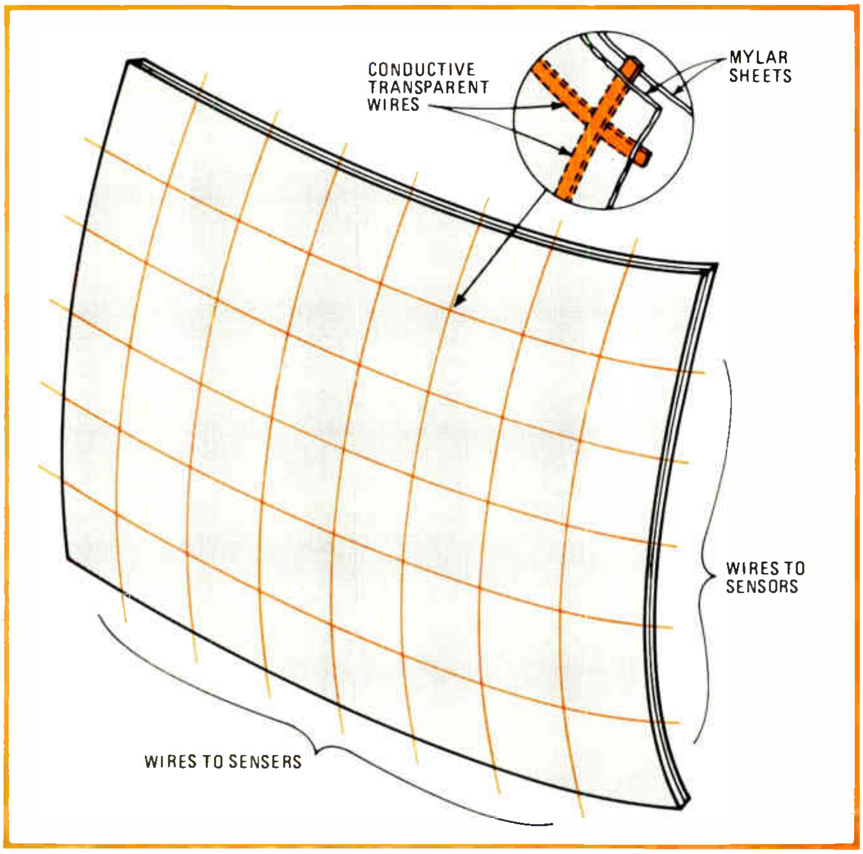
In the capacitance-sensing system (Fig. 3), the CRT's faceplate is subdivided into discrete areas, and a thin, transparent conductive material is fired onto each area. A wire connects each of these pads to the controller board, which continually scans the faceplate and samples the pads until a touch is detected. In touching one of the pads, the body's capacitance is added to the circuit. When the controller senses a change in capacitance, it sends a flag code to alert the system and follows this with a pad-identifier code.

The main advantages of a capacitive-sensing system are that the metal coating over the glass plate is fairly transparent and the system is durable. One of the drawbacks is that the system will only detect the touch of a conductive stylus such as the human finger; the tip of a pencil or a factory worker's gloved hand will not be detected. In addition, capacitive systems have been criticized for their failure to adjust to fluctuations in capacitance caused by ambient conditions, such as temperature and humidity. However, firmware that makes automatic adjustments has recently been added to capacitance-based systems.

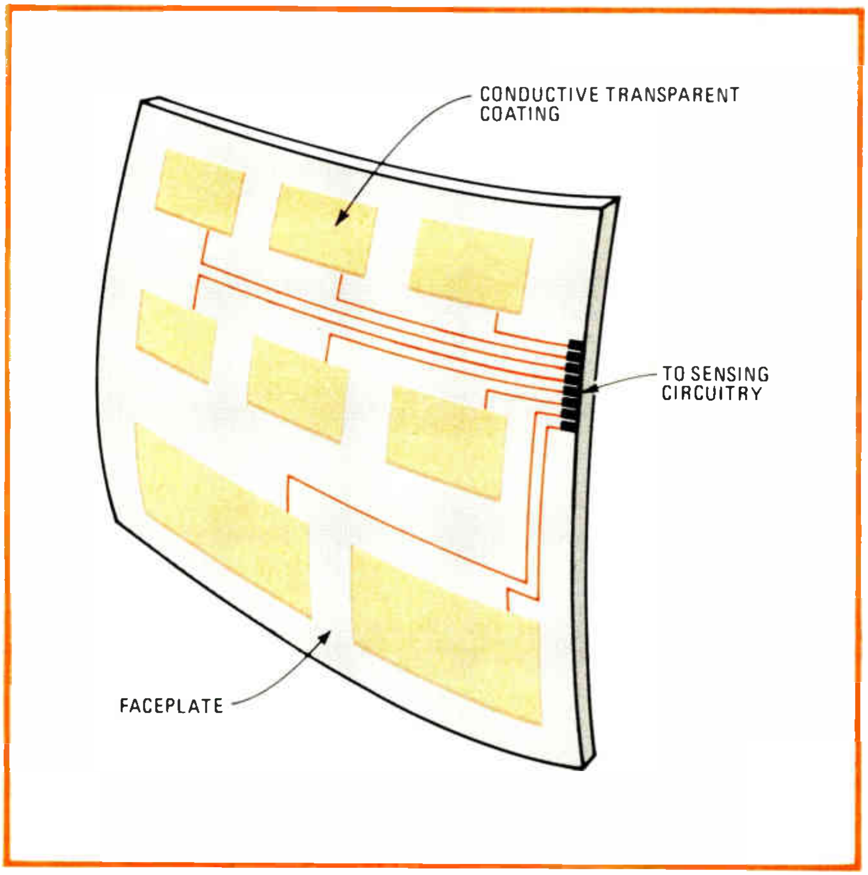
The most serious shortcoming of the capacitive approach also appears about to be solved. Up till now, capacitive touch screens have been limited to a fixed number of pads (usually 32) because space must be allotted for the conductors that connect each pad to the edge of the screen. Having a limited number of pads poses no problem in applications with simple menu-driven routines, but it is impractical in more sophisticated applications. Recently, Interactions Systems Inc., Newtonville, Mass., has come out with a capacitance system with the equivalent of a continuous 100-by-100 grid. The system, called the TK-1000, is based on a faceplate fully coated with a transparent metallic film rather than an actual metallic grid. The controller of the system measures the capacitance from each of the four edges and then calculates the coordinates of the point touched.

Less problematic than the capacitive sensing system is the acoustic touch screen (Fig. 4), based on acoustic surface waves generated by piezoelectric transducers located along the X and Y axes of a screen. Any object that touches the faceplate reflects the acoustic waves back to the transducers that generated them. Acoustic-wave touch screens afford a clear view of the screen and allow the user to program touch-active areas, making this technology especially suitable for a number of sophisticated applications.

Although acoustic systems can achieve high resolution, they cannot locate the center of a large object such as a finger, so that practical resolution is limited to points about ½ in. apart. The high resolution comes from the ability to place transducers at close proximity to each other, but this also heightens the touch screen's sensitivity to dust and dirt and thus increases the likelihood of misreadings. Because of their sensitivity, acoustic touch



2. Resistive sensing. In a typical resistive membrane for a touch-sensitive overlay, two Mylar sheets are separated by a space containing a wire matrix. As the overlay is pressed by, say, a finger, two crossing wires make electrical contact and this XY coordinate is fed to a processor.



3. A capacitive touch. A capacitance-sensing overlay is constructed by depositing pads of a conductive transparent coating on the glass faceplate. When a pad is touched by a finger, the sensing circuitry detects the added capacitance.

screens are best used by trained personnel who know how to keep the screen clean.

In optical touch screens, rows of light-emitting diodes and photodetectors are placed around the periphery of the screen (Fig. 5), producing a grid of infrared light beams across and close to the surface of the CRT. Each optoelectronic device along an axis has a unique address. Multiplexing each control line connected to each LED identifies which of these diodes is turned on and thus which photodetector on the opposite side should be receiving a signal. When a finger or stylus touches the display, the light beams are interrupted, and the XY coordinates of the interrupted beams are transmitted to the host computer.

Boosting resolution

By staggering the optical devices, optical touch screens can achieve a resolution as high as 1/10 in. Through software averaging of the position signal, resolution can double to 1/20 in. Another advantage of an optical touch screen is that the operator can define touch-active areas of any size or shape. Thus, these screens offer considerable programming flexibility for a wide range of applications.

In addition, optical touch screens operate reliably in hostile public or industrial environments. No overlay comes between the user and the display, so this type of touch screen always affords a clear view of the screen. Because optical devices are housed under the bevel, there are no sensitive or moveable parts accessible to the user. And because the infrared touch screen uses all-solid-state components, it has a longer lifespan than other touch-sensing devices.

The main drawback of light-beam technology is parallax at the edges of the screen. Parallax is caused by light beams travelling in a straight line across a curved CRT surface. The light beam will be close to the CRT at the center of the screen but farther away near the edges. This effect can make it harder for the user to break the light beams that correspond to the spot that he wishes to activate, near the screen's edge.

Electro Mechanical Systems reduces the parallax problem by mounting LEDs and photodetectors in a curved row on the CRT frame to follow the curvature of the display. The company also recommends making the touch-active areas slightly larger than the visual target, so that if a finger enters the infrared matrix at a slight angle to the display, the touch will still be identified with the correct touch area.

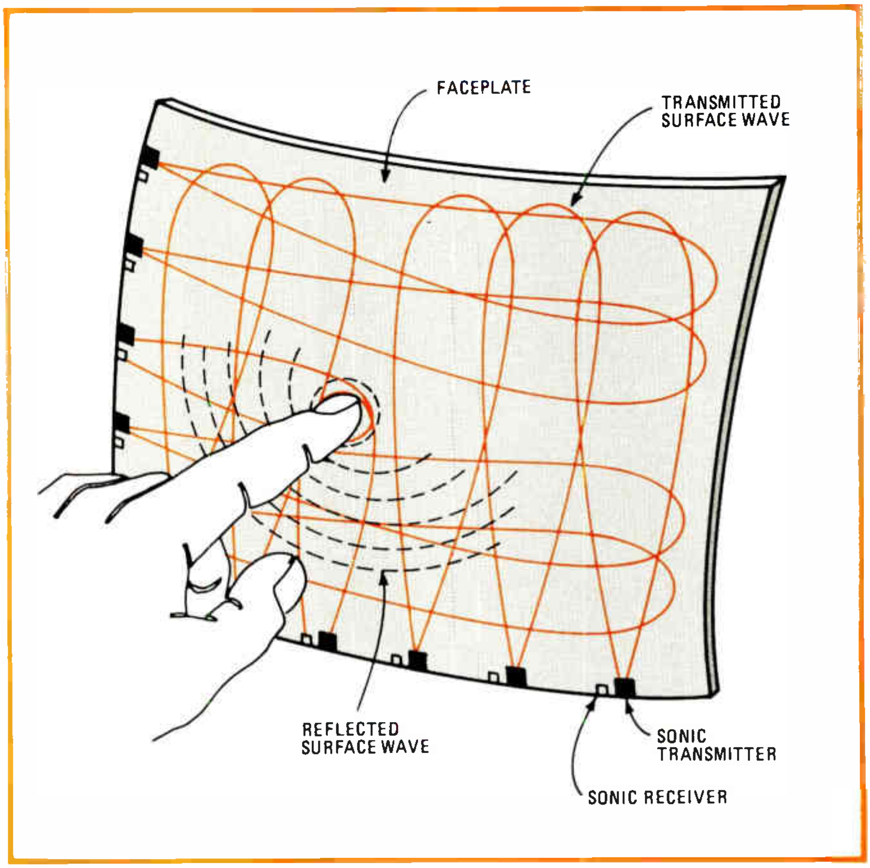
Since an object the size of a finger will probably break light beams in more than one row and column, an EMS touch panel completes an entire scan before it reports interrupted beams. It then averages the values of the interrupted beams to locate the center of the stylus. If a single beam is interrupted for longer than a second, it is considered defective and removed from consideration on subsequent scans. Therefore, one defective beam does not affect the operation of the entire system.

Many logic tricks may be used to check for invalid hits. For example, if the system knows the size of the stylus, it can check to make sure that the number of interrupted beams falls within a range corresponding to that size. Hits outside this limit—caused by an insect, a piece of dirt, or a person's entire hand, for instance—are considered invalid.

Previously, high levels of ambient light have interfered with optical touch screens. But ambient-light-compensation circuits have now eliminated this problem.

Regardless of what type of sensing a touch-screen terminal employs, it still faces the competition of the full keyboard to some extent. While the touch screen will never replace the keyboard in intensive data-entry applications, it does have important advantages over the keyboard in many other applications.

Operating a keyboard inevitably places some burden on the user. He or she must have training in control language, some typing skill, and enough knowledge to interact with the computer. Touch screens subtly redefine the interaction between user and computer. Because the menu-driven program presents complex processes step by step, the burden of directing the interaction is lifted from the user. He merely responds to choices on the screen and is not required to make decisions about the way the computer is operating. Thus, touch makes the computer accessible to all users, regardless of training or experience, and in many applications, a touch screen is a faster and more accurate user interface than the traditional keyboard.



4. A sound decision. In the acoustic-wave sensing overlay for a touch screen, sonic transmitters send surface waves across the faceplate. Any object touching the waves reflects them back to sonic receivers, from which the processor calculates the object's position.

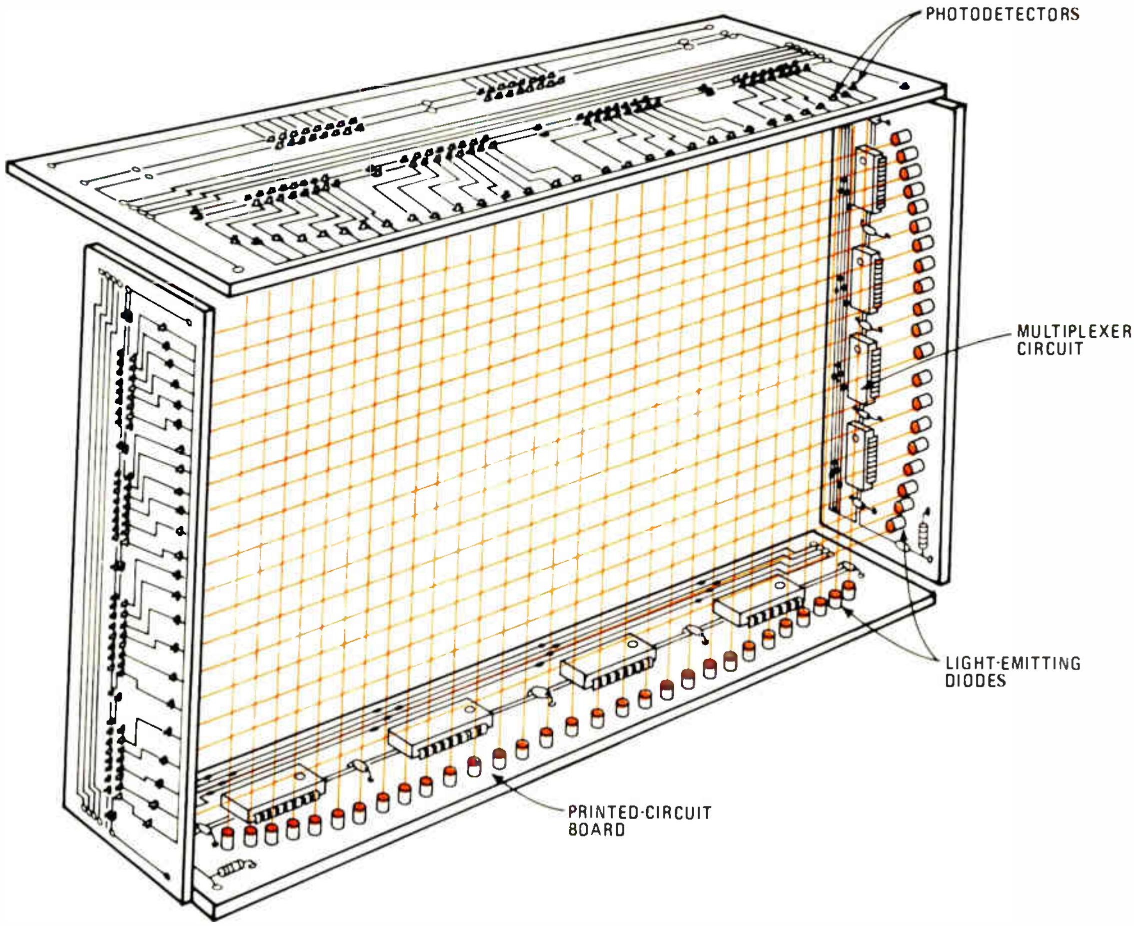
Any data-input device is effective only when it is an integral part of the system as a whole and is useful only to the extent that it is supported by application software. When a mouse is used as an add-on device, its interfacing often causes problems. Although new mouse software is constantly being developed by such companies as Logitech, there is still not enough of it available to make it useful more widely. Currently, the mouse is certainly an excellent device for cursor control and for computer-aided-design and interactive-graphics applications, but it is still widely considered impractical for spreadsheets, word processing, and in business-management software. Basically, the mouse was designed as a supplement to, rather than a substitute for, the keyboard.

Touch technology in action

The touch screen, on the other hand, can be fully integrated with the system, and in many applications it can replace the keyboard entirely, as in EMS's touch terminal, Touch Information Display (TID), which uses a single microprocessor to control both terminal and touch-panel functions. A few easy commands in terminal-resident software can program the visual display and the touch panel. Thus, both trained computer operators and novice users can write their own touch-active programs for original-equipment-manufacturer or personal applications. The Hewlett-Packard HP 150's touch screen is also fully integrated with the system and is backed by an array of popular software programs.

According to HP, its designers chose the optical approach for a variety of reasons. First, because no physical overlay is required, the optical touch panel does not interfere with the contrast and visibility of the CRT. Second, by using automated production and relatively inexpensive optical devices, HP could keep production costs relatively low. Finally, the optical touch screen was the only technology that promised to be at least as reliable as the other components in the system.

One of touch technology's most obvious uses is to provide information to the public at such places as banks, libraries, airports, shopping malls, and tourist attractions. Touching portions of a screen to learn current mortgage rates, flight schedules, or the way around Disneyland is easy as well as enjoyable, especially for people who are keyboard-shy. In addition, by rigidly sequencing procedures and directing the operator's actions, the



5. Touching the light. In the typical touch panel, opposite rows of light-emitting diodes and photo detectors along the periphery of the faceplate form an XY grid of light beams. A break in a beam is detected and this information is converted into XY information for the processor.

touch screen can be used as a highly accurate device for data collection.

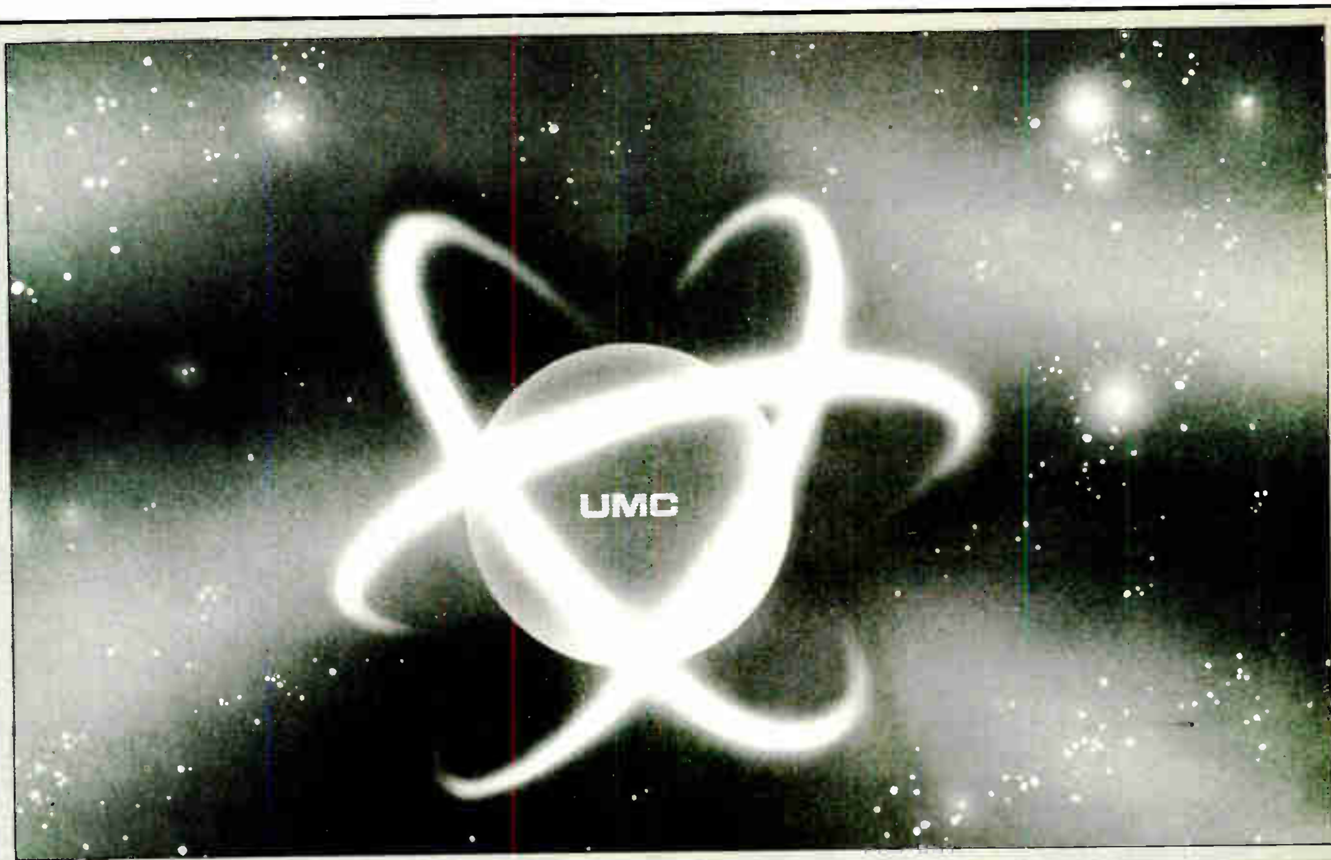
Yet touch is not limited to such simple interactive applications; its benefits extend to the seasoned computer user. For example, touch-active displays are widely used in process-control applications. Processes to be controlled are usually represented graphically, and operators can quickly stop, start, or regulate parts of a complex system from a single screen by means of a touch. Currently, touch screens are serving as control panels on General Motors assembly lines, regulating Shell Oil storage tanks, and monitoring ABC television studios in New York.

Using touch screens in control applications actually improves efficiency. The Tektronix 1240 logic analyzer, for example, uses on-screen soft keys that are activated by a touch. The soft keys handle about 50 functions that would otherwise require a cluttered keyboard. Rather than use terse abbreviations designed to fit on small hardware keys, the soft keys make it possible to use descriptive labels that clearly communicate their functions.

Office-bound

Now touch is slowly making its way into the office. Santa Barbara Development Laboratories has proposed its own idea of the office of the future by developing what it calls a transparent executive system, which combines a touch-sensitive screen with voice-recognition technology and extensive graphics software. The system has been designed for managers, and the touch screen is used for menu selection and cursor control, replacing the keyboard. □

UMC-The nucleus of MOS ICs



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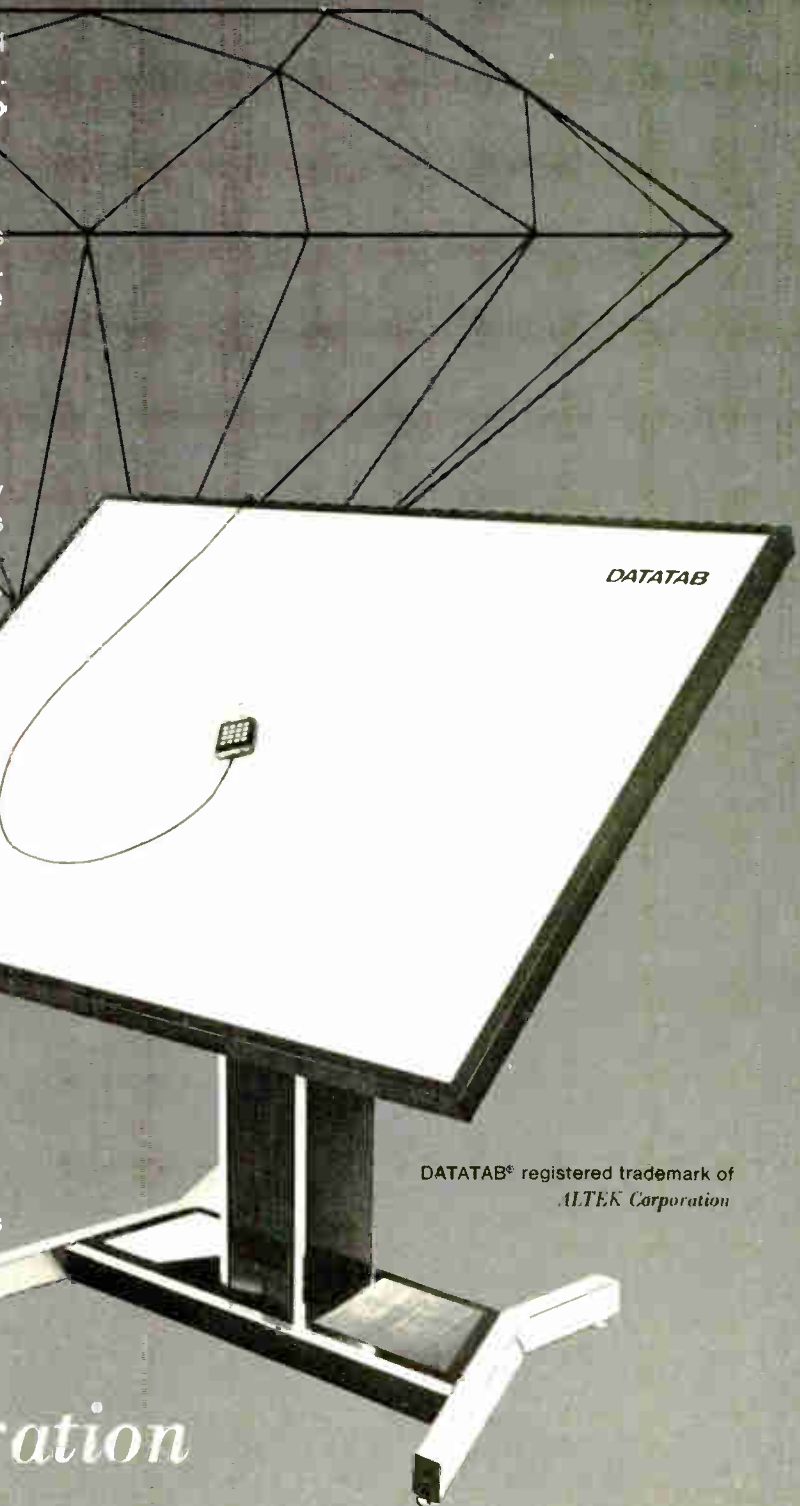

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Circle 146 on reader service card

New system manages hundreds of transactions per second

Parallel data paths, pipelining, large cache memory, and 32-bit hardware combine to increase transaction system performance

by Robert Horst and Sandra Metz, *Tandem Computers Inc., Cupertino, Calif.*

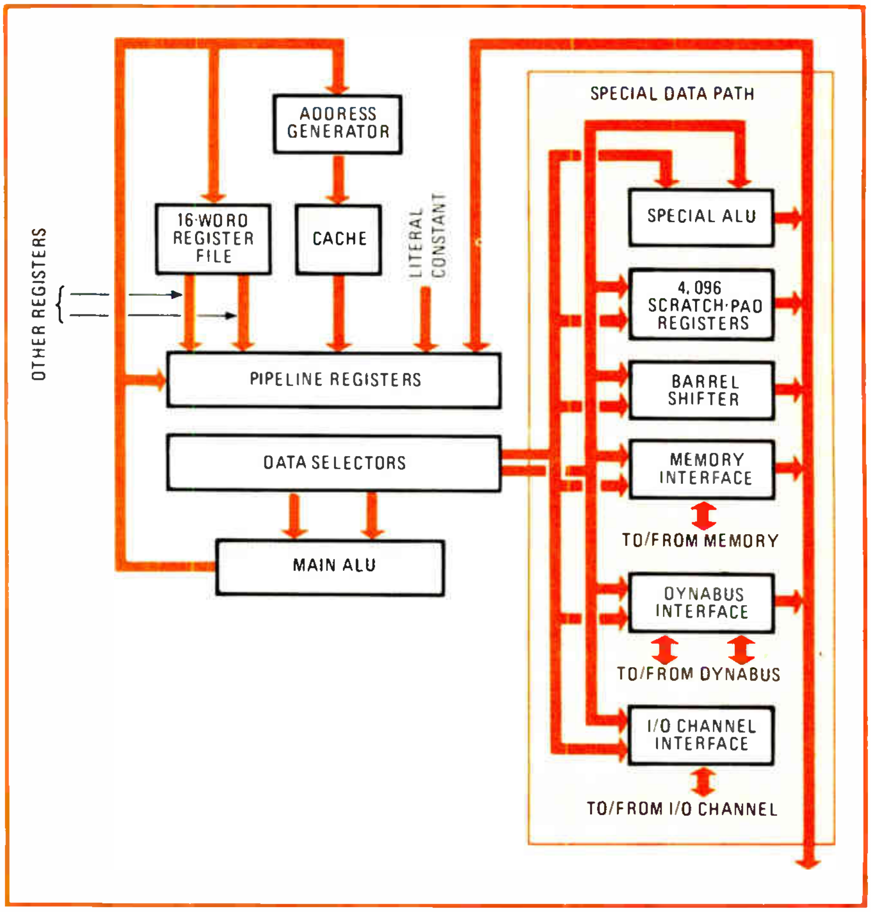
☐ Computer systems for on-line transaction processing have a unique set of requirements that pose an enormous challenge to designers. These systems have to be fault-tolerant, expandable through the addition of modules, and able to process multiple transactions at a reasonable cost, while maintaining data integrity. The coming generation of transaction-processing systems must also address a fast-growing need for very high-volume applications that require the processing of more and more transactions per second.

Designed to handle very high-volume transaction processing, the 32-bit NonStop TXP system reaches two to three times the speed of the NonStop II system it supercedes, while retaining complete software compatibility. Without reprogramming, a TXP system can grow from a single system containing from 2 to 16 processors, to a local cluster of up to 224 processors linked with fiber-optic cables, to a worldwide network of up to 4,080 processors.

Many of the problems in designing the TXP processor had already been solved in the NonStop II processor and system design. The NonStop II extended the instruction set of the NonStop 1+ system to handle 32-bit addressing but did not efficiently support that addressing in hardware. The existing 5-megabyte input/output bus and 26-megabyte Dynabus, Tandem's proprietary bus structure, had more than enough bandwidth to handle a processor with two to three times the performance. The existing packaging had an extra central-processing-unit card slot for future enhancements, and the existing power supplies could be reconfigured to handle a higher-power CPU.

The main problems involved designing a new microarchitecture that would efficiently support the 32-bit instructions at much higher speeds, with only 33% more printed-circuit-board real estate and an existing backplane. This involved eliminating some features that were not critical to performance and finding creative ways to save area on the pc board, including clever uses of programmable array logic and an unusual multilevel control-store scheme.

Since the new TXP processor was to be object-code-compatible with the Nonstop II system yet have a significant price-performance advantage, it was expected that soon after announcement much of the company's produc-



1. Parallel data paths. The NonStop TXP's architecture lets the main arithmetic and logic unit operate in parallel with either a special ALU, one of 4,096 scratch-pad registers, a barrel shifter, the memory interface, the Dynabus interface, or the input/output channel.

TABLE 1: COMPARE-BYTE INSTRUCTIONS (INNER LOOP)

Clock cycle	NonStop TXP		Traditional architecture
	Main ALU	Special ALU	
1	extract byte 1	extract byte 2	extract byte 1
2	compare bytes	—	extract byte 2
3	(repeat)	(repeat)	compare bytes
4	—	—	(repeat)

TABLE 2: DYNABUS-RECEIVE MICROCODE INSTRUCTIONS (INNER LOOP)

Clock cycle	NonStop TXP		Traditional architecture
	Main ALU	Special data path	
1	compute checksum on previous word	read next word from bus queue	compute checksum on previous word
2	address next memory location	write data to cache and memory	read next word from bus queue, increment address
3	(repeat)	(repeat)	write data to cache and memory
4	—	—	(repeat)

tion would have to shift quickly from the NonStop II system to the TXP system. This required that efficient board-testing procedures be in place by the time the product was announced and precluded the use of traditional functional board testers, which need months of programming after the design is finished. Instead, scan logic was designed into the processor and a scan-based board-test system using pseudorandom test vectors was developed.

Performance improvements

The performance improvements in the NonStop TXP system were attained through a combination of advances in architecture and technology. The NonStop TXP architecture uses dual 16-bit data paths, three levels of macroinstruction pipelining, 64-bit parallel access from memory, and a large cache (64 kilobytes per processor). Additional performance gains were obtained by increasing the hardware support for 32-bit memory addressing.

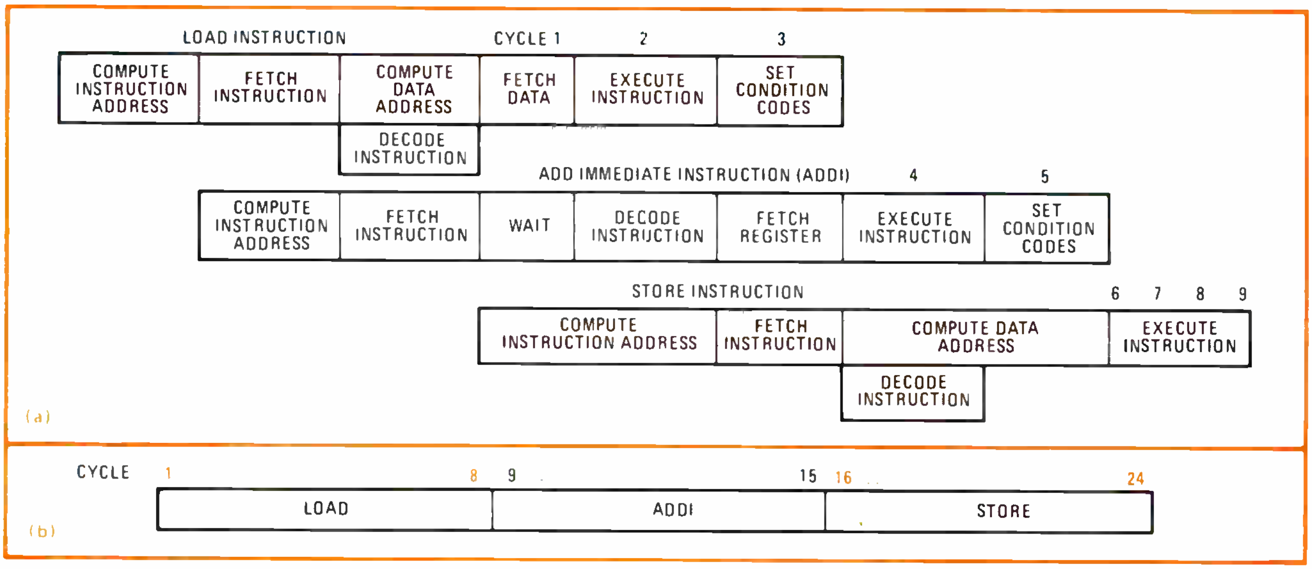
The machine's technology includes 25-nanosecond programmable array logic, 45-ns 16-K static random-access-memory chips, and Fairchild Advanced Schottky Technology (FAST) logic. With these high-speed components plus a reduction in the number of logic levels in each path, a 12-megahertz (83.3 ns per microinstruction) clock rate could be used.

The system's dual-data-path arrangement increases performance through added parallelism (Fig. 1). A main-arithmetic-and-logic-unit operation can be performed in parallel with another operation done by one of several special modules. Among them are a second ALU that performs both multiplications and divisions, a barrel shifter, an array of 4,096 scratchpad registers, an interval timer, and an interrupt controller. Other modules provide interfaces among the CPU and the interprocessor bus system, I/O channel, main memory, and a diagnostic processor.

The selection of operands for the main ALU and the special modules is done in two stages. In the first, data is accessed from the dual-ported register file or external registers and placed into two of the six registers. During the same cycle, the other four pipeline registers are loaded with cache data, a literal constant, the results of the previous ALU operation, and the result of the previous special-module operation.

In the next stage, one of the six pipeline registers is selected for each of the main ALU inputs and one for each special-module operand. Executing the register selection in two stages, so that the registers can be two- rather than four-ported, greatly reduces the cost of multiplexers and control storage, while the flexibility in choosing the required operands is unimpaired.

Some examples of the way microcode uses the parallel data paths are shown in Tables 1 and 2. The first example shows the inner loop of the compare-bytes instruction. Each of the dual ALUs in the TXP system extracts one byte; then the extracted bytes are compared. This operation takes two clock cycles on the TXP system



2. Pipelined. The instruction pipeline of the NonStop TXP system allows parts of several instructions to be processed simultaneously (a)—nine cycles are required to execute three typical instructions. Without pipelining (b), 24 clock cycles would be required.

Hardware-performance monitor helps optimize design

While new architectural concepts were being developed for the TXP system, a hardware-performance monitor was built to record measurements of the software-compatible NonStop II processor. Xplor consists of two large Wire-Wrap boards plus a small board to interface to the processor under test. It has approximately 800 Schottky TTL components and took more than two years to develop.

This general-purpose tool is capable of capturing 64 bits of data every 100 nanoseconds and reducing that data to usable form. The 256 kilobits of internal memory can be configured in many different word lengths to record, for instance, a 64-bit count of 4,096 different events, a 32-bit count of 8,192 different events, or a single flag for 256-K events. In addition, Xplor has programmable state machines with which data can be captured based on complex sequences of events; it includes hardware for the emulation of various cache organizations.

Two different Xplor configurations were developed to gather data for the TXP processor. The first was an instruction histogram measurement that records the frequency with which each instruction occurs, the percentage of time spent in each instruction, and the average number of code and data reads and writes performed by each instruction. The data is recorded in 64-bit counters, so in effect an unlimited amount of real-time data can be taken before the counters overflow.

The second Xplor configuration monitors memory addresses and emulates the tag store of a cache. Hit ratios for many different cache organizations can be determined by varying the effective cache size, associativity (one-, two, or four-way), block size, and replacement algorithm. Because the data is taken in real-time and reduced on-line, the hit-ratio measurements are much more accurate than the traditional technique, in which short address traces are recorded on tape for later analysis. This is especially important in transaction processing, since a large amount of process switching takes place; some individual transactions can last several seconds, during which millions of memory references take place.

Once the measurement methods were working, Xplor was attached to an eight-processor NonStop II system. A typical transaction-processing benchmark was brought up on the system, and transactions then were generated by another system, running software that simulated users at a number of terminals. At that point, histogram and cache measurements were taken for several of the central processing units.

The results of the histogram measurements helped determine some of the data-path widths and organizations for the TXP processor. Once the most frequently executed instructions were known, the design was modified to provide more hardware support for them. Since the measurements distinguished different paths through some instructions, tradeoffs could be made in the microcode to make the frequent cases faster.

The results of the cache measurements brought about some major changes in the original cache organization. In one measurement, the hit ratio went from 97% for the original cache to 99% for the final one, for an overall CPU performance gain of over 15%.

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but would require three if the extract operations could not be done simultaneously.

The dual 16-bit data paths tend to require fewer cycles than a single 32-bit path when manipulating byte and 16-bit quantities and slightly more cycles when manipulating 32-bit quantities. A 32-bit add takes two cycles rather than one, but the other data path is free to use the two cycles to perform either another 32-bit operation or two 16-bit operations.

Time disadvantage

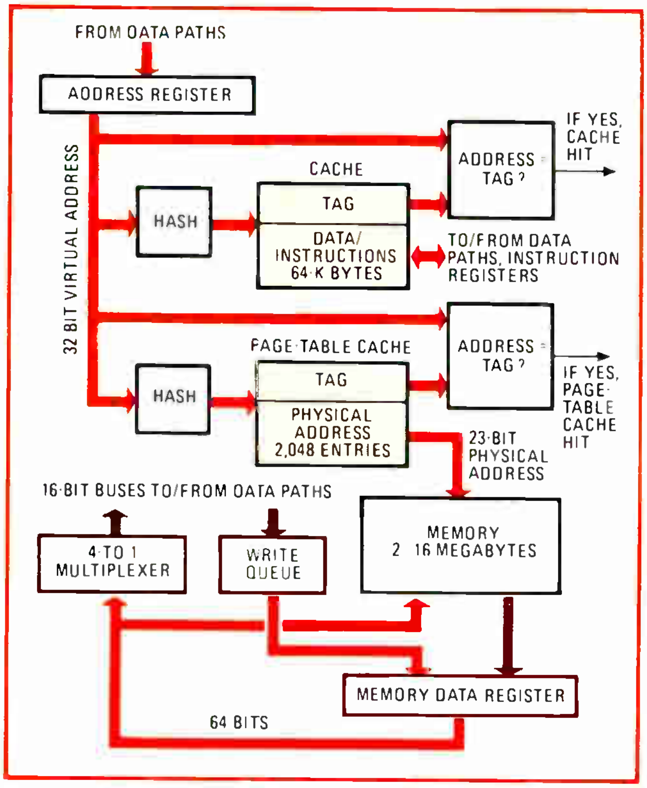
The time disadvantage in performing a single 32-bit operation is partially offset by the cycle-time advantage for 16- versus 32-bit arithmetic (32-bit arithmetic requires more time for carry propagation). Measurements of transaction-processing applications have shown that the frequencies of 32-bit arithmetic are insignificant relative to data-movement and byte-manipulation instructions, which are handled more efficiently by the dual data paths than by a single 32-bit data path. Most instructions have enough parallelism to let the microcode make effective use of both data paths.

To control the large amount of parallelism in the NonStop TXP system processor, a wide control-store word is required. The effective width of the control store is over 100 bits. To reduce the number of RAMs required, the control store is divided between a vertical control store of 8-K 40-bit words and a horizontal control store of 4-K 84-bit words. The vertical control store controls the first stage of the microinstruction pipeline and includes a field that addresses the horizontal control store, whose fields control the pipeline's second stage. Lines of microcode that require the same or similar horizontal controls can share horizontal-control-store entries.

Unlike microprocessor-based systems that have microcode fixed in read-only memory, the NonStop TXP system microcode is implemented in RAM, so it can be changed along with normal software updates and new performance-enhancing instructions can be added.

The NonStop TXP processor uses three-stage pipelining for both macro- and microinstructions. Figure 2 illustrates the operation of the macroinstruction pipeline for a sequence of three instructions. The first is a load instruction that loads a word into the hardware stack. The second is an add immediate instruction that adds a constant to a register on the hardware stack, and the third is a final store, which stores the result in memory.

With no pipelining, this sequence would require 24 (8+7+9) clock cycles to execute, but because the prefetch and part of the execution of each instruction can be overlapped with previous instructions, the actual execution time is just 9 (3+2+4) clock cycles. Because instructions are pipelined, the TXP processor can execute its fastest instructions in just two clock cycles (167 ns),



3. Memory access. The simple but extensive organization of the TXP cache provides an average hit ratio of over 96%. With a cache hit, the data is read out of the cache in 83 nanoseconds. When the data requested is not in cache, a cache miss results and the 64-bit-wide access to memory speeds the cache refill.

and it can execute load and branch instructions, which are frequently used, in only three clock cycles (250 ns).

Each NonStop TXP processor has a 64-K-byte cache that holds both data and code. A 16-processor NonStop TXP system has a full megabyte of cache memory. To determine the organization of the cache, a number of measurements were performed on a NonStop II system using a specially designed hardware monitor (see "Hardware-performance monitor helps optimize design," p. 149). The measurements showed that higher cache hit ratios resulted with a large, simple cache (directly mapped) than with a smaller, more complex cache (organized as two- or four-way associative). Typical hit ratios for transaction processing on the NonStop TXP system are in the range of 96% to 99%.

Cache miss

Cache misses are handled in a firmware subroutine rather than by the usual method of adding a special state machine and dedicated data paths for handling a miss. Because of the large savings in cache hardware, the cache can reside on the same board as the primary data paths; keeping these functions proximal reduces wiring delays and contributes to the fast 83.3-ns cycle time.

The cache is addressed by the 32-bit virtual address rather than by the physical address, thus eliminating the extra virtual-to-physical translation step that would otherwise be required for every memory reference. The virtual-to-physical translation, which is needed for refilling the cache on misses and for storing through to memory, is handled by a separate page table cache that holds mapping information for as many as 2,048 pages of 2-K bytes each (Fig. 3).

A cache memory by itself does not necessarily boost a processor's performance significantly. It is of little use for the cache to provide instructions and data at a higher rate than the rest of the CPU can process. In the TXP processor, the cache's performance was tuned to provide instructions and data at a rate consistent with the enhancements to instruction processing provided by increased pipelining and parallelism.

32 bits and more

The two concerns related to a system's word length are capability and performance. The NonStop TXP system has 32-bit virtual addressing built into the hardware, so is capable of addressing a gigabyte of virtual memory. In addition, the TXP processor can manipulate 32 bits of data at a time through its dual 16-bit data paths. Thus the 32-bit NonStop TXP system has the additional advantage of being able to run software that was originally written for the 16-bit NonStop II system; both systems have been provided with instructions that can operate on 8-, 16-, 32-, and 64-bit data types.

In transaction processing, measurements of instruction frequencies show that data-movement instructions (loads, stores, and moves) occur much more frequently than 32-bit arithmetic instructions. For this reason, the NonStop TXP system is optimized to handle data movement by providing 64-bit access to main memory and 32-bit buses and address registers to make memory addressing as efficient as possible.

The NonStop TXP processor was implemented on four large pc boards using high-speed FAST logic, PALs, and high-speed static RAMs. The CPU's logical and physical partitioning was carefully controlled to ensure that the machine's basic cycle time would not be slowed by long propagation delays. The four CPU boards are:

- SQ: containing the control store and sequencing logic.
- CC: containing the I/O channel and various special modules.
- IP: holding the main data paths and cache.
- MC: providing the memory interface, barrel shifter, and interprocessor bus interface.

Each CPU module also has from one to four memory boards. On the initial release, each memory board contains 2 megabytes of error-correcting memory implemented with 64-K dynamic RAMs. A 16-processor NonStop TXP system can therefore contain up to 128 megabytes of physical memory.

The NonStop TXP system was designed to be easy to manufacture and efficient to test. Data and control registers were implemented with shift registers configured into several serial-scan strings. The scan strings are of value in isolating failures in field-replaceable units. This serial access to registers also makes board testing much faster and more efficient because the tester can directly observe and control many control points. A single custom tester was designed for all four CPU boards and for the memory-array board as well.

The NonStop TXP system is the first product to be

MIPS and transactions per second

Determining relative performance among computer systems has never been an easy task. The often-quoted millions-of-instructions-per-second rate is intended as a way to compare basic central-processing-unit-hardware performance. Comparisons are also made on the basis of benchmarks. CPU-intensive benchmarks measure the performance of the CPU hardware and compiler; more extensive benchmarks measure the entire system performance—including the hardware, compiler, operating system, and data-base-management system. In general, the more extensive benchmarks give a more accurate prediction of actual system performance.

Each of the various measurement techniques has pitfalls. The MIPS rate is perhaps the least accurate way to compare systems. One reason is that there is no easy way to relate the power of one instruction set to another. In addition, vendors vary in the way they measure MIPS: some use it for the speed of the fastest instructions, others measure the speed of the most frequently executed instructions, and still others measure the speed of a "typical" mix of instructions. According to these definitions, each NonStop TXP processor is 6, 4, or 2 MIPS, respectively.

developed using Tandem's proprietary computer-aided-design system. The CAD system's capabilities for logic entry, logic simulation, and automated pc-board routing were instrumental in reducing the design time. While most high-performance CPUs require four to five years to develop, the NonStop TXP processor took just 2½ years—six months to complete a written specification, one year to construct a working prototype, and another year to reach volume production.

Performance measurement

Some simple benchmark programs have recently become popular in measuring performance (see "MIPS and transactions per second," p. above). One is the Puzzle benchmark, which is a CPU-intensive program to solve a three-dimensional puzzle. Execution times for Puzzle can vary widely for the same machine, depending on whether the program accesses arrays through subscripts or pointers and whether frequently used variables are assigned to registers. Versions of the Puzzle benchmark with pointers and registers were used to compare relative performance for a TXP processor.

Puzzle was written in TAL (transaction application language, the company's system-programming language); the execution time, using a single TXP processor, was measured at 1.67 s. This compares with 4 s on a VAX-11/780 for Puzzle written in C.[1] Because Puzzle does not measure such system features as support for virtual memory, I/O bandwith, and the ability to do fast context switching, a standard benchmark for comparing transaction-processing systems is still needed.

One transaction-processing benchmark has been developed by a third party, however. The U. S. Public Health Service ran an extensive benchmark in 1981 to determine which system to select for a large on-line medical-information system.[2] In that study, a 15-processor Tandem NonStop system running a 1981 version of Tandem's Encompass DBM system performed the benchmark at a rate of 4.5 transactions/s. An International Business Machines Corp. System 370/168-3 running version 3 of the Adabas DBM system performed the same benchmark at 2 transactions/s.

This benchmark gives a data point for comparisons between Tandem and IBM systems. A 15-processor NonStop system performs the Public Health Service benchmark 2.25 times as fast as an IBM 370/168-3. Though it would be desirable to compare the TXP system directly to one of IBM's newest systems, such as the IBM 4381-2, no competitive benchmarks have been published. However, comparisons of the MIPS rate of different processors within a single family are fairly accurate and can be used to extrapolate to newer systems.

According to market research performed by the Gartner Group,[3] the IBM 4381-2 is rated at 2.7 MIPS, compared with the older IBM 370/168-3's 2.4 MIPS rating—a ratio of 1.125 : 1. Company tests have shown the NonStop TXP to have a MIPS rate approximately three times that of the NonStop processor. The extrapolation of the Public Health Service benchmark performance to the two newer systems is shown in Table 3.

Unlike many shared-memory multiprocessor systems, Tandem systems provide linear growth in transaction-processing power as the system expands. A single system can include up to 16 processors, and clusters with as many as 224 NonStop TXP processors may be configured with Tandem's fiber-optic link. Clusters with up to 60 processors are currently in operation, and their users have verified the linear-performance growth within a cluster of this size.

The largest IBM mainframe today is the IBM 3084, which is rated at approximately 23 MIPS. Extrapolation from the benchmark data suggests that the performance of a cluster of 224 TXP processors is on the order of 10 times as powerful as IBM's top-of-the-line 3084 processor. □

TABLE 3: TANDEM VERSUS IBM PERFORMANCE COMPARISONS

	U.S. Public Health Service benchmark: results (transactions per second)	USPHS benchmark: extrapolated results* (transactions per second)
IBM 370/168-3	2	—
Tandem NonStop 15-processor system	4.5	—
IBM 4381-2	—	2.25
Tandem NonStop TXP 3-processor system	—	2.7

*Not actual measurements

References
[1]Malcolm A. Gleser, Judith Bayard, and David D. Lang, "Benchmarking for the Best," Datamation, May 1981.
[2]Computer Architecture News, 10 : 1, March 1982, p. 29.
[3]Gartner Group Inc., Stamford, Conn., market research surveys.

The power and the portability: evaluating the C programming language

Although C is less inherently structured than Pascal, it is emerging as the language of choice for a wide range of systems

by Paul Miller, *Horizon Software Systems Inc., San Francisco,* and James A. Watson, *Modulator SA, Bern, Switzerland*

☐ Before application developers choose a programming language, they must answer two important questions: first, is the language powerful enough for the intended purpose, and, second, will it make the application transportable? The C programming language is becoming popular among developers because for it, the answers to both questions are in the affirmative.

The power of C is attested to by its use in AT&T Bell Laboratories' Unix operating system and in CP/M-86, in such data-base-management systems as Unify and Informix, and in office-automation software, like the Horizon Software System. As for transportability, with compilers available for such operating systems as CP/M, on 8-bit machines; MS-DOS, on 16-bit machines; and Unix and VMS, on 16/32-bit machines, C clearly meets the test.

Control without bother

Besides being powerful and transportable, the ideal language should also increase a designer's productivity without sacrificing efficiency of implementation. C provides constructs that let programmers stay close to their target machines but still has the advantages of such higher-level constructs as named variables and macro expansions. C's structure permits designers to deal more directly with the programming process. They can spend more time analyzing program dynamics, uncovering bottlenecks, and developing optimization routines, as well as less time worrying about the gritty detail of the machine, since C gives them control over registers without the bother of digging down into the microcode.

A wag once observed that objects must exist before operations can be performed upon them. C combines a wide range of data types, easy definition of new types and structures, and simple, clean conversion between types—all of which give programmers a truly valuable flexibility when they approach problem solving. C's wide range of data types extends from bits to double-precision real numbers. Designers who work with C let the implementation determine the data type and use compilers that offer 8-, 16-, or 32-bit integers and 32- or 64- bit real numbers (Table 1).

When predefined data types are inadequate, user-defined structures can be built (Tables 2–4). For example, engineering and scientific applications frequently require complex numbers. If so, a new data type can be defined as "complex," consisting of two real (or double-precision) numbers. Unlike Pascal and other languages, once the new data type is defined, it can be manipulated with all the functionality of standard data types. That is, it can be be passed as a function parameter or returned as a function result.

Data types can also be easily converted under C. The

TABLE 1: COMMON DATA TYPES ON VARIOUS COMPUTERS

	DEC PDP-11 (ASCII protocol)	Honeywell 6000 (ASCII)	IBM 370 (EBCDIC protocol)	Interdata 8/32 (ASCII)
Character (bits)	8	9	8	8
Integer (bits)	16	36	32	32
Short integer (bits)	16	36	16	16
Long integer (bits)	32	36	32	32
Single-precision floating-point type (bits)	32	36	32	32
Double-precision floating-point type (bits)	64	72	64	64

conversion is automatic if no information will be lost as a result of it—for example, when integers are upgraded to real numbers in expression evaluations or when data must be forced with cast operators, the model for the target data type enclosed in parentheses. A data operator defines the type of data; for example, INT X: defines X as an integer and CHAR Y: defines Y as a character. CHAR * L: defines L as a pointer to a character. If X rather than an integer was needed as a pointer to a character, a cast of X defined as (CHAR *)X casts X as a pointer to a character only at that one location.

C-language operators include the standard flow-control ones, such as While, For, and Until loops, as well as If-Then-Else evaluators. C includes several novel operators, too. At first blush, they may seem a bit user-unfriendly; but they are valuable, and with familiarity comes respect for their functional power. The novel operators can be broken down into two categories. The first includes those that extend the capabilities of the language, such as bitwise operators and shift operators (Table 5). The second consists of those operators that improve the efficiency and compactness of the language. This category includes such arithmetical operators as increment (++) and decrement (—), which permit the statement i = i + 1 to be rewritten into the more concise i++, and a novel arithmetic assignment operator that permits such statements as i = i + 2 to be expressed as i + = 2.

Fortran and other languages developed before the advent of structured programming lack many control and program-structuring techniques and thus tend to be difficult to read and maintain. By contrast, C has a set of tools for building the flow-control and branchings needed for structured programs. But these tools are not forced on programmers, so it is still possible for them to produce code that is cryptic and difficult to understand.

Closer ties

In addition, C provides closer ties to a machine's architecture while giving designers more freedom. In fact, many designers have described C as the structured assembler. Various control structures, including For and While statements, as well as tools for building data structures, give C most of Pascal's facilities. However, C gives programmers more freedom and power than Pascal does, because C lacks forced declarations and makes type-casting operations rather easy. Pascal, of course, provides a more structured environment but also makes system-level programming harder to perform.

Of course, the freedom promoted by C creates the dangers that freedom always involves. Pascal's inherently rigid nature keeps programmers out of trouble; C gives them all the rope they need to tie themselves into knots.

Pascal lacks C's flexibility and modularity. In Pascal, all variables, functions, and procedures must be declared before use, a requirement that produces programs with subroutines defined before the main body of the source file. The routines must be declared and compiled in each source file where they are used before the first reference to the routine. They must contain the

TABLE 2: UNARY OPERATORS IN C

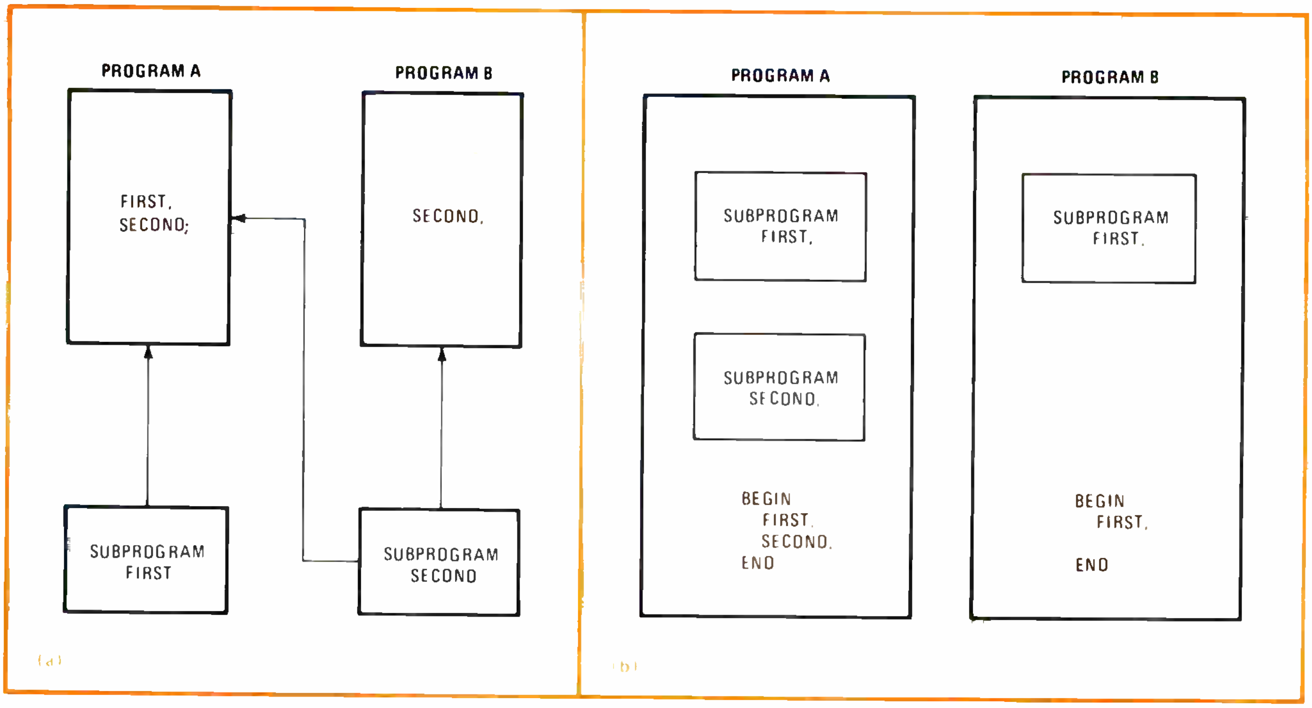
Symbol	Operator
•	pointer
&	address of
-	minus, negative
!	logical not
~	1's complement
++	increment
--	decrement
SIZEOF	size of some object (number of bytes)

TABLE 3: BINARY OPERATORS IN C

Symbol	Operator
•	multiply
/	divide
%	modulus
+	add
—	subtract
>>	shift left
<<	shift right
<	less than
>	more than
< =	less than or equal to
> =	greater than or equal to
= =	equivalent
! =	not equivalent
&	bitwise addition
^	bitwise OR
|	bitwise union
& &	AND (intersection)
||	OR
? :	conditional tertiary operator

TABLE 4: ASSIGNMENT OPERATORS IN C

Symbol	Operator
=	assign
+ =	add increment and assign
- =	subtract decrement and assign
• =	multiply by increment and assign
/ =	divide by increment and assign
% =	remainder and assign
>> =	right shift and assign
<< =	left shift and assign
& =	bitwise intersection and increment
^ =	exclusive OR and assign
\ =	OR and assign



Flexibility in C. In the Pascal programming language (a), the subroutines (shaded) of all programs must be both declared and compiled before the main body each time they are used. However, the C programming language (b) permits the subprograms (shaded) to be compiled separately, then called into the main source. All that C needs to call the subprogram is the name of the file containing the object module.

complete argument list and any required return values—a methodology that discourages the use of libraries of common routines.

C has no such constraints; so long as all procedures are provided before the final phase—linking the program—procedures may be written and compiled separately in whatever way is most convenient for programmers (see figure). For example, they can define a set of standard functions—such as as complex addition, subtraction, multiplication, division, exponentiation, and so forth—on the complex data types.

Whenever and wherever

These routines can be compiled as a separate unit, then referenced whenever and wherever they are needed in other programs, and there is no need to redefine all the calling parameters. All programmers have to do is to supply, somewhere in the compile command, the name of the file containing the object modules.

C has other advantages, as well. For instance, when a programmer can identify a small number of very heavily used variables—such as array subscripts, counters, and the like—they can be labeled as "register variables" and the compiler will attempt to allocate machine-register storage locations for them. As a result, many operations can be performed significantly faster than they would be otherwise and will produce more compact code. But the exact number and types of variables that can be declared are very implementation-dependent.

TABLE 5: BIT OPERATORS IN C

Symbol	Operator
&	bitwise AND
|	bitwise inclusive OR
^	bitwise exclusive OR
<<	left shift
>>	right shift
~	1's complement (unary)

Finally, C gives designers very great portability. The language is small and elegant, and many functions—like input/output and functional arithmetic—are found in libraries external to the language itself.

Without modification

C compilers have been implemented in environments ranging from 8-bit microprocessors running CP/M all the way up to parallel-processor Denelcor HEP-1 supercomputers. For example, the Horizon Software System is composed of many integrated office-automation functions, including a spreadsheet, word processing, list processing, and spelling checks and correction—all of them performed by many thousands of lines of source code written in C.

Horizon runs without modification on all the popular microprocessors, on several mainframe computers, and on many minicomputers, and it is line-for-line and character-for-character identical in all operating environments. The same source code even supports implementations in such natural languages as French, German, and Italian. Without further modification, the programs run under Unix version 6, system III, system V, BSD 4.1, BSD 4.2, Idris, Xenix, PC/IX, Eunice, and Coherent.

C offers both the portability and power required in a programming language. As the language of Unix, it is being implemented across a wide range of machines. As a high-level language, it facilitates program development. □

Engineer's newsletter

New standard defines key characteristics of chip-carrier sockets

A new standard, RS-506, from the Electronic Industries Association should go a long way toward resolving the conflicting specifications in sockets for ceramic leadless type A chip carriers on 50-mil centers. **The standard establishes a unified numbering system to be used for chip-carrier sockets** and will standardize the dimensional characteristics and functional levels of sockets, as well as establishing standard test methods and gauges for socket examination. This document will provide information to be used in the selection of sockets for leadless ceramic chip carriers and will provide guidelines by which the user may develop a socket specification. Standard 506, generated by the EIA's P-5.2 working group on sockets, delineates socket types and configurations, contact terminations and finishes, mating configurations and design requirements, and specifies mechanical, electrical, and environmental test procedures. The military has used this document as the basis for MIL-STD-38533. Copies of this chip-carrier socket standard are available from the Electronic Industries Association, Standards Sales Department, 2001 Eye St. N.W., Washington, D. C. for $10 per copy.

Kit helps designers make thick-film hybrids from surface-mounted ICs

With all the hoopla about surface mounting of components on printed-circuit boards, it is best to keep in mind that surface mounting originated in the thick-film-hybrid field. In fact, **surface mounting on ceramic substrates results in a relatively low-cost, high-performance alternative to standard die-and-wire-bonded hybrids**. Cermetek has developed a designer's kit to lead electronic and packaging engineers through the complex process of designing custom thick-film hybrids based on surface-mounted components. The kit consists of a 20-page instruction manual, a laminated design grid (4× scale), self-sticking icons of small-outline integrated circuits (SOICs), transistors, diodes, chip capacitors, chip inductors, chip resistors, and 10 vellum overlays for the designer to indicate circuit-to-circuit interconnections. Once a layout is completed on the grid, a designer returns it to Cermetek for a quote on prototyping and production. Usually, Cermetek will have a quote in seven working days and deliver prototypes within eight weeks. The kit, available from Cermetek or any of its sales representative, costs $25, which will be refunded with the first order. For more details, contact Neil Madonick, Cermetek Microelectronics Inc., 1308 Borregas Ave., Sunnyvale, Calif., 94089, or call (415) 434-3670.

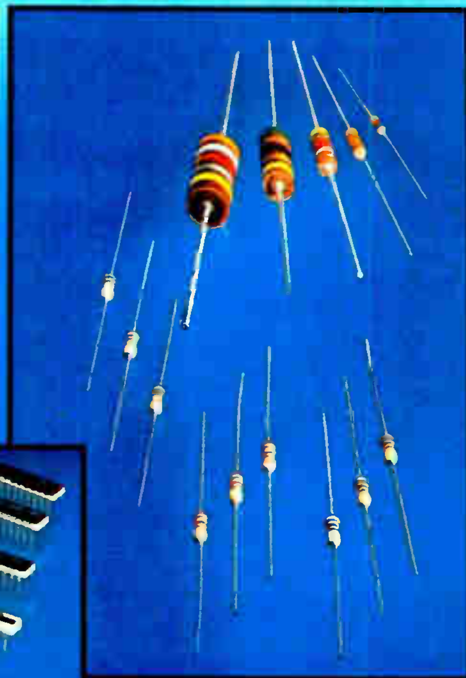
Mathematical analysis rids fast oscilloscopes of timing jitters

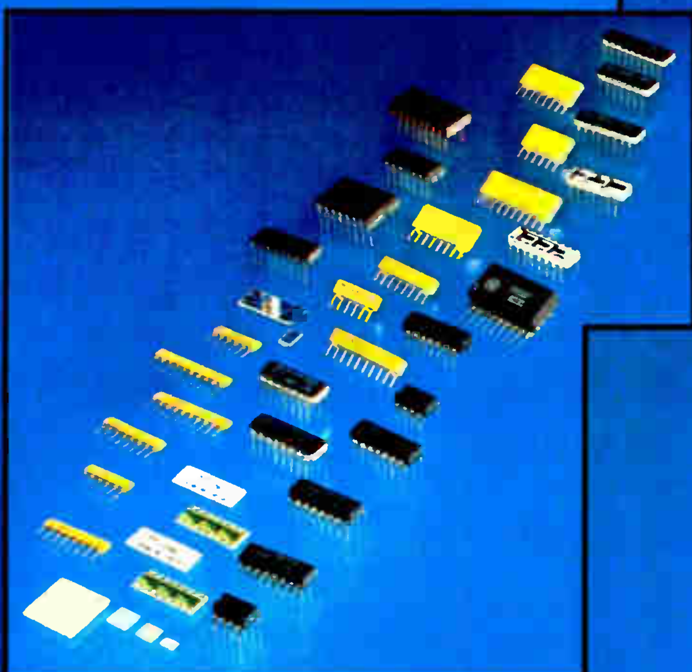
The National Bureau of Standards has developed a method for removing the distorting effects of time jitter from waveform measurements made with a fast (20-ps) equivalent-time-sampling oscilloscope. Previously, the calibration of fast-pulse generators was difficult because the faster the measured-pulse waveform, the more distorted the measurement became. The NBS method first measures or estimates the time-jitter-probability density function and then treats it as a pseudo-network impulse-response function, where the distorting effects are removed from the measured-pulse waveform using a network-deconvolution algorithm. **Computer simulations indicate that peak errors of less than 1% in fast-pulse waveform estimation can be obtained with this algorithm**. For more information, contact W. L. Gans, Division 723.05, National Bureau of Standards, Boulder, Colo., 80303.

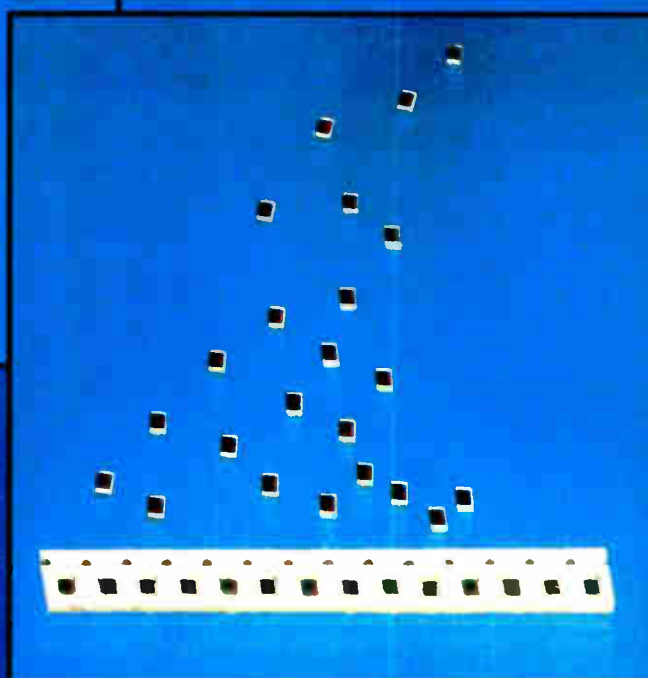
-Jerry Lyman

SPECIAL ADVERTISING SECTION

RESISTORS







A MULTITUDE OF RESISTOR TYPES RESPONDS TO TECHNOLOGY'S NEEDS

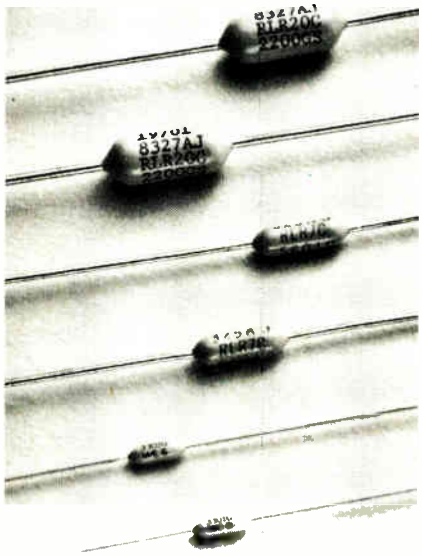
Probably the most widely used component in electronic circuits, the resistor is benefiting from advances in materials and manufacturing processes. What follows is an report on the progress in the most popular resistor types—wire-wound, carbon-composition, carbon-film, metal-film, chips, networks, and precision resistors—and where each is heading. The tradeoffs that must be made in deciding what type of resistor to specify will also be examined.

Wirewound Resistors

If only a few ohms of resistance is needed in a circuit, the resistor can simply be a piece of nickel-chromium wire of suitable width and length. Nichrome wire has a much greater resistance than standard copper wire, making it easier to build wirewound resistors of a reasonable length. This nichrome wire (sometimes called resistance wire) is usually wound around a ceramic core, and covered with some insulating material.

Although the oldest of the resistor technologies and considered by many to be the dinosaur of the industry, this product group continues to maintain its position, notes Margaret Nowicki, advertising coordinator for Dale Electronics Inc., Columbus, Neb. Though inflation has contributed to growth in wirewound resistors, the broadening of the end-product markets leads Nowicki to estimate a 1984 market of some $88 million, compared with a 1980 market of $74.1 million. On the other hand, the maturity of this resistor market segment does not lend itself to the development of new products with improved temperature coefficients, resistive-value ranges, and tolerances.

An example of how wirewound resistors are losing their place in applications is the voltage divider. Now commonly made of thin-film resistor networks, it once was assembled from discrete wirewound or film resistors.


S-level military qualification approval, the highest level, has recently been bestowed on Mepco/Electra's RLR series. The Morristown, N.J., company sells the 10-kΩ ⅛-W RLR05 for 15¢ each in lots of 1,000 pieces. The firm now boasts three types that meet S-level MIL-R-39017 standards. [Circle reader service number 421]

Even in this mature market segment, however, the buyer is presented with a great range of choices. For example, Dale's special products section within the wirewound division can offer nonstandard resistor designs with variations in packaging, leads, matching, and special types. Packaging options include heat sinks, silicone coating, epoxy or silicone molding and hermetic sealing. Leads, in addition to being axial or radial, can be threaded, insulated, or made of special materials and in special dimensions. The units can be matched in pairs by value and sets, within close tolerances, by their resistor ratio, or by their temperature coefficients. Such special types as those with extended low- or high-resistance ranges or very low or high temperature coefficients and those with special wire alloys to alter electrical characteristics can be selected also.

The capacitance and inductance inherent in all resistors can become significant at high frequencies. For wirewound resistors, inductive effects are predominant in low-value resistors (below 1,000 Ω) and capacitive effects become predominant in high-value parts. Some companies offer noninductive lines of resistors that use Aryton-Perry winding—two single-layer parallel windings in opposite directions—to cancel most of the inductive and capacitive effects.

Two longtime competitors of wirewound resistors are carbon-composition and carbon-film units, with markets estimated to be $60 million and $28.7 million, respectively, in *Electronics'* 1984 World Markets Survey and Forecast.

Allen-Bradley Co. has a surprisingly wide line of composition resistors made in a process the Milwaukee, Wisc. company calls hot-molded. Available with tolerances of ±5%, ±10%, and ±20% and in power ratings of ⅛, ¼, ½, and 2 watts, the resistors are offered with standard ranges from 1 Ω to 100 megohms. On special request the resistors can be made with resistance values to 1 teraohm.

Easy Solderability

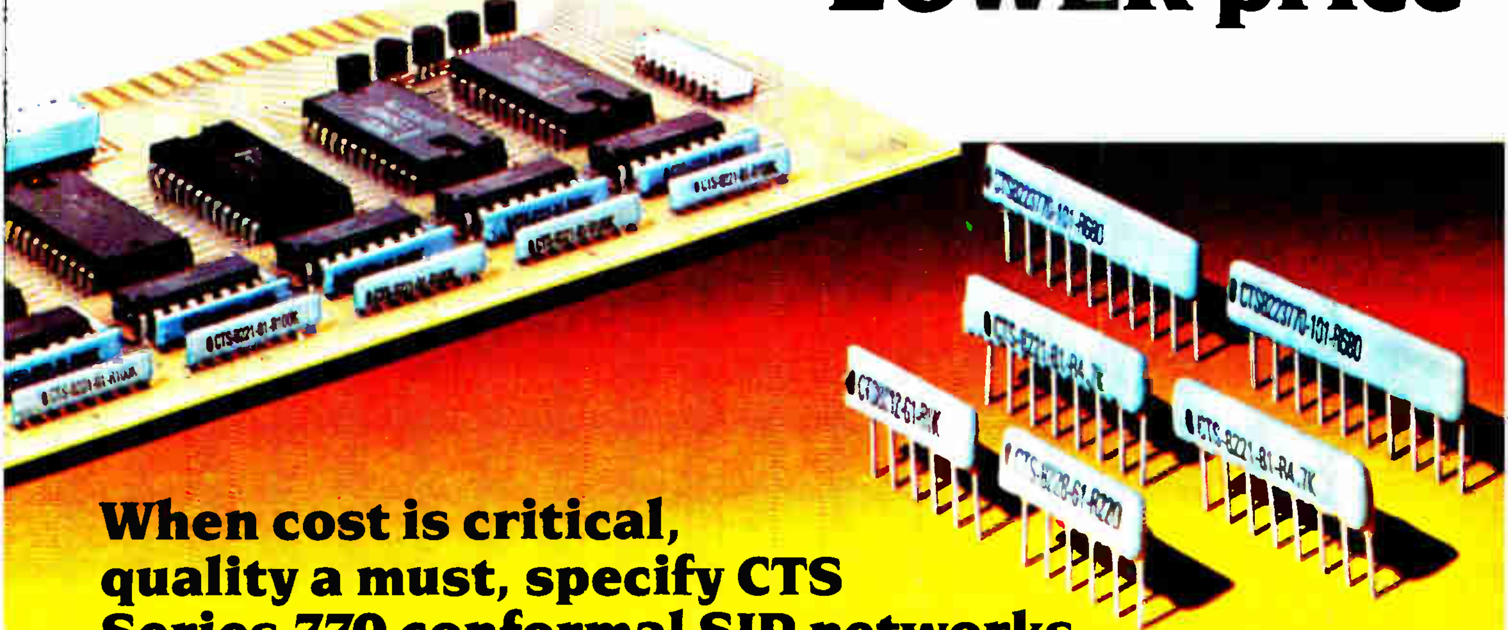
The resistors' hot-solder-coated leads remain easy to solder even after long periods in stock. The oxygen-free copper leads are readily weldable and allow considerable weld-schedule latitude. Stocking resistors with two different lead materials to accommodate various soldering processes is unnecessary.

The resistors, which Allen-Bradley claims are the most reliable of all electronic components (based on 35 years of testing and field experience), exhibit extremely uniform tracking characteristics. For example, in flip-flop circuits, resistors used in pairs that are

The photographs on the cover came from Allen-Bradley Co.

NEW CTS conformal SIP networks offer...

LOW board profile (.195") LOWER price



When cost is critical, quality a must, specify CTS Series 770 conformal SIP networks

CTS, acknowledged leader in resistor networks, now offers a line of conformal SIP's with an on-board height no greater than a DIP package (.195"). CTS experience in resistor network technology is now available in a new conformal network featuring a low selling price. Priced lower than molded or ceramic networks, CTS conformally coated SIP networks are finding more and more applications.

Series 770 networks are designed for high volume, cost-sensitive applications such as electronic games, personal computers, telecommunications gear and automotive devices. They are winning acceptance from OEM's who demand CTS reliability at a reasonable price.

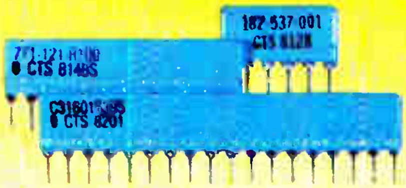
Available in 2 to 12 pin sizes, these SIP networks can be supplied for large volume custom requirements or in many standard resistance values for fast off-the-shelf delivery.

Contact your CTS Distributor for off-the-shelf delivery or write for complete specifications to: CTS Corporation, 406 Parr Road, Berne, Indiana 46711. Phone: (219) 589-8220.

CIRCLE NO. 212

CTS Series 771 Standard height (.350") SIP Networks also available

When higher power handling is a consideration the Series 771 conformal SIP is the answer. They offer the same well-known CTS reliability and are available in 4 to 20 pin sizes.



CTS means Reliability

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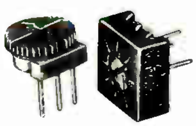

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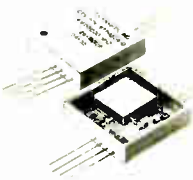
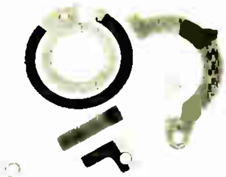


Temperature Compensated Crystal Oscillators High stability and reliability.
Phone: (815) 786-8411
CIRCLE NO. 244



Series 710 Custom conductive plastic strip or disc resistors.
Phone: (704) 684-6451
CIRCLE NO. 245

drawn from the same package or reel (a standard mass-production practice) will track with each other throughout changes of temperature, humidity, and load.

Carbon-film resistors, like carbon-composition resistors are losing ground to metal-film and other technologies because they cannot be made in as precise values; they are more sensitive to temperature fluctuations; and they are noisier. However, they do offer low voltage coefficients, high stability, and good high-frequency characteristics.

Moreover, some carbon-film units, such as a couple of lines from Dale Electronics, are offered with tighter tolerances than are carbon-composition units. In addition to 5% tolerances, Dale offers tolerances of 1% and 2%.

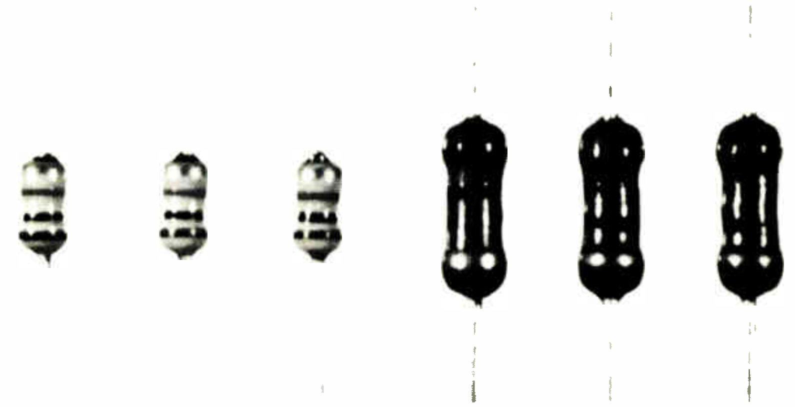
A relatively new package used for housing carbon-film resistors, as well as other types of resistors and components, is the MELF, for metal-electrode face-bonding. It is similar to chip resistors in that the devices mount directly to the printed-circuit board. The parts' cylindrical shape eliminates the need to consider orientations in mounting in most cases; some MELF parts, however, have to be mounted in a certain direction.

Solderable Package

The use of metallic electrodes with special plating at each of the two ends of the MELF parts gives them strength against mechanical force and soldering stress. There is no need to worry about damage to MELF parts during assembly. They can withstand direct-flow soldering at 260°C for 5 to 8 seconds.

KOA Denko Ltd. of Ina City, Japan, makes ⅛- and ¼-W resistors with tolerances of 1% or 5% in MELF packages. Mouser Electronics, Santee, Calif., also houses a line of ⅛-W resistors with 5% tolerances in MELF packages.

MELF packages do have at least one disadvantage. Once a part has been removed from a pc board, it cannot be reused because the mounting electrodes are damaged. Sometimes the entire resistor is broken when it is removed from the board.



Panasonic Industrial Co.'s Electronic Components Division offers a carbon-film resistor that is smaller than comparable ⅛-W devices. At only 3.5 mm long, its leads, after bending, can fit a standard printed-circuit-board wiring grid of 5 mm. The Secaucus, N.J. firm's resistor is available in resistances from 1 Ω to 1 MΩ. [Circle 422]

The metal-film resistor market is continuing to grow as both applications and the product base expand, according to Dale's Margaret Nowicki. As improvements in the metal-film technology occur in the form of widening resistance ranges, better temperature coefficients, improved tolerances, and more competitive pricing, this resistor type should continue to capture more of the market from carbon and wirewound products.

Dale projects 1984 metal-film consumption at $113 million. *Electronics'* consensus market survey produced nearly the same results, estimating the year's consumption to be $105 million.

Because the thermal characteristics are different, a metal-film resistor can be housed in a package somewhat smaller than that of a carbon-composition resistor of comparable power rating. However, when specifications for film resistors were being written in the late 1950s, it was thought to be better to have carbon-composition and film resistors of equal power ratings in same-size packages.

Now, Mepco/Electra Inc., Morristown, N. J., is taking advantage of metal-film's better thermal characteristics and offers what it calls the Space Miser. It is a 1/3-W part in the package size usually used for a ⅛-W unit. Offered with resistances from 10 Ω to 100 kilohm, the part has a ±1% tolerance and a ±100 ppm/°C temperature coefficient.

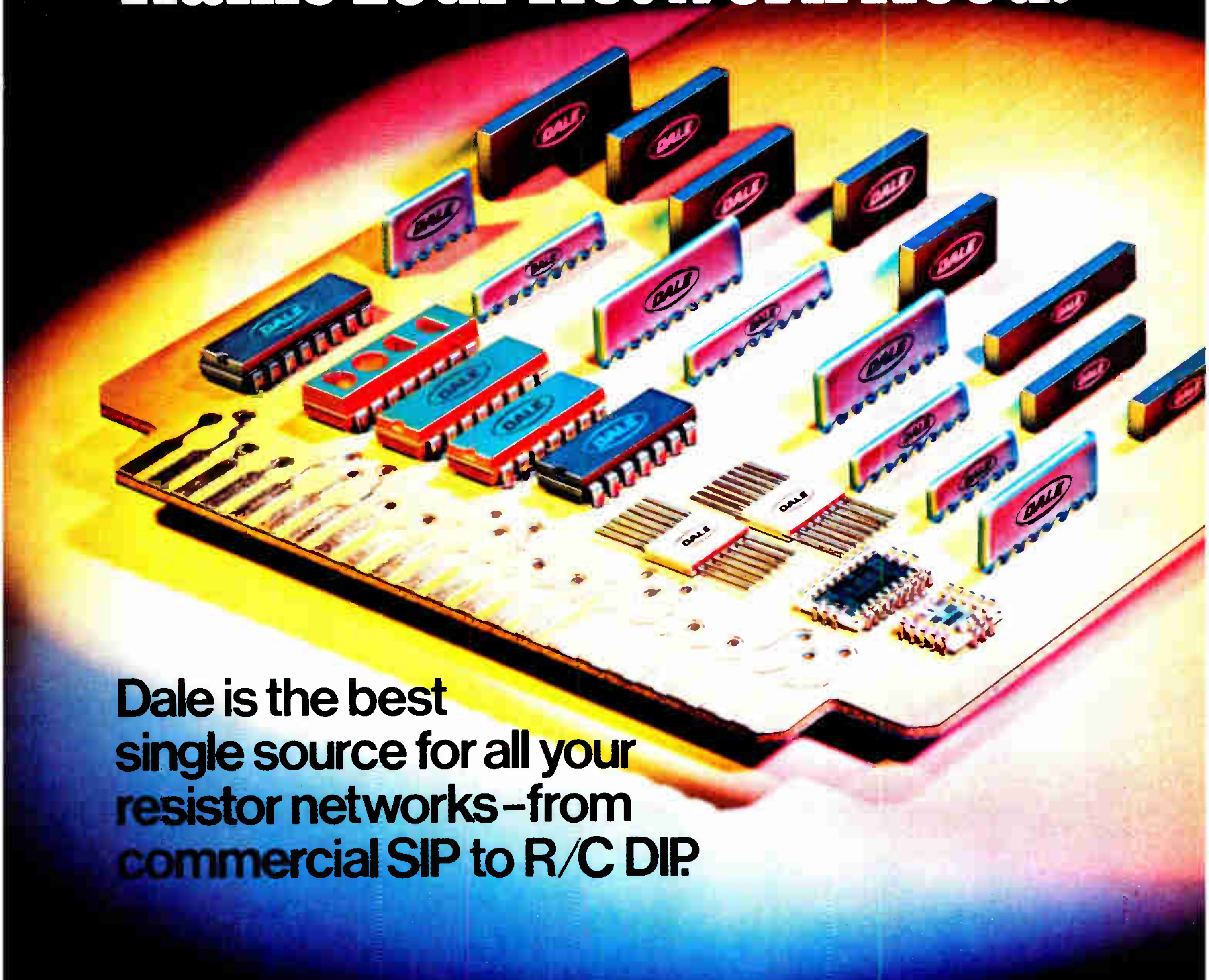
In high-accuracy analog circuits and precision instrumentation, where outstanding long-term circuit performance is required in spite of variances in the environmental temperature, Caddock Electronics Inc., Riverside, Calif., offers more stable resistors made with resistance films called Tetrinox. Stability is quoted as close as 0.01% per 2,000 hours, tolerance is specified at 0.01%, and temperature coefficients are less than 5 ppm/°C.

Advanced Technology

Constructed with advanced-technology complex-oxide resistance films that are fired onto ceramic substrates, the Tetrinox resistors come in resistance ranges from 1 kΩ to 125 MΩ. They are suitable for high-stability applications like input voltage dividers, precision bridge circuits, precision voltage-reference circuits, ultra-stable voltage dividers, ultra-low-power precision circuitry, and precision decade voltage dividers.

Neohm SpA, a Turin, Italy, company offers a line of metal film resistors with ±50, ±100, and ±200 ppm/°C temperature coefficients and tolerances of 2% to 5% (for 200 ppm/°C) and 1% to 2% (for 100 and 50 ppm/°C) parts. Power ratings range

Name Your Network Need.



Dale is the best single source for all your resistor networks—from commercial SIP to R/C DIP.

Dale can help you get a lot more value out of thick film networks—because we give you more networks to choose from. We're producing the most versatile line-up of types and sizes available from any one manufacturer. It includes:

- **Low cost commercial coated SIP**
- **MIL-R-83401 molded DIP/SIP in the industry's broadest range**
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You'll find that working with Dale is an efficient way to quickly evaluate all your design options... and to make certain of getting the quality level you need. Check it out. Write for your copy of our new thick film resistor network catalog or contact us today. Phone 915-592-3253.

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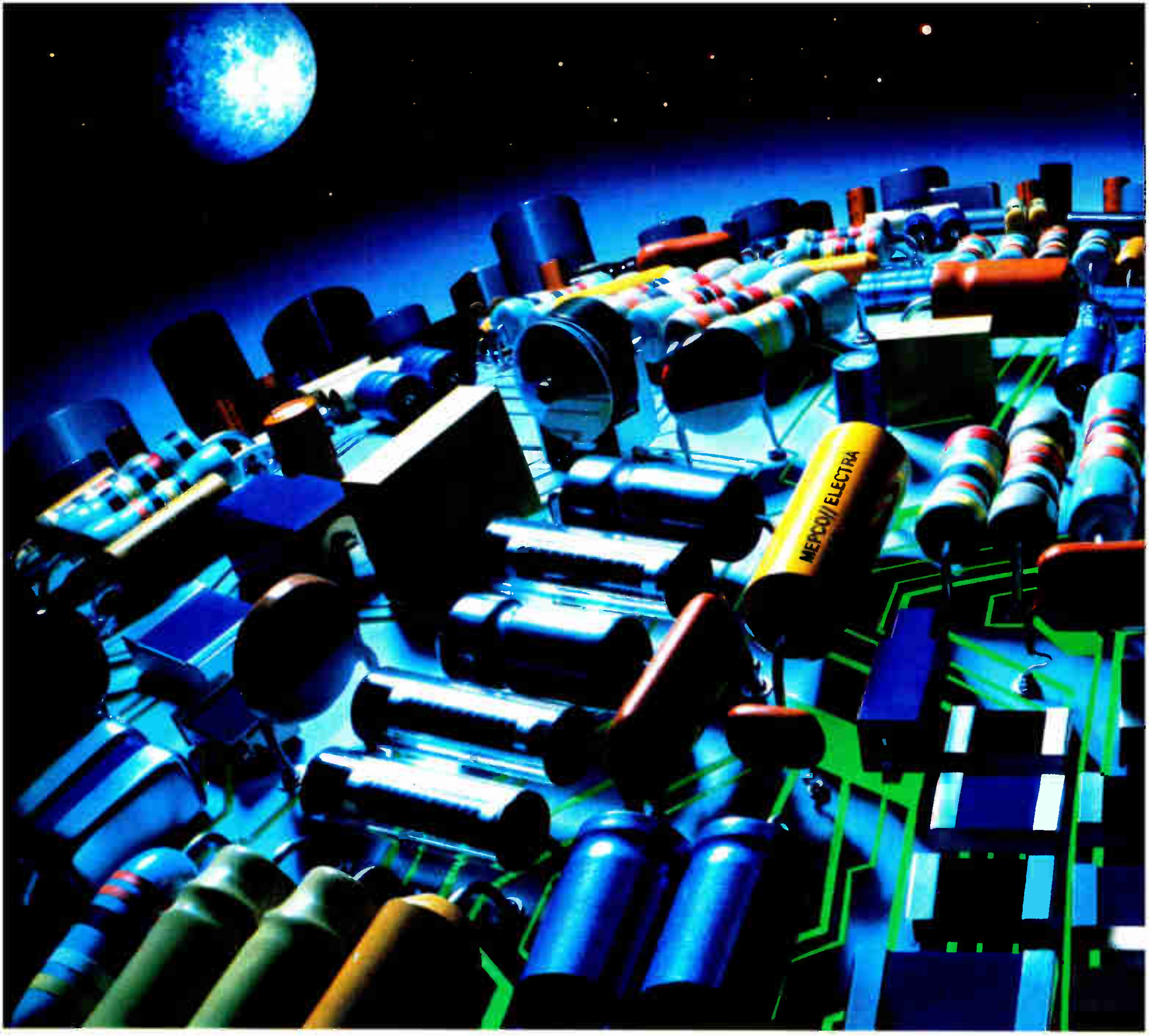
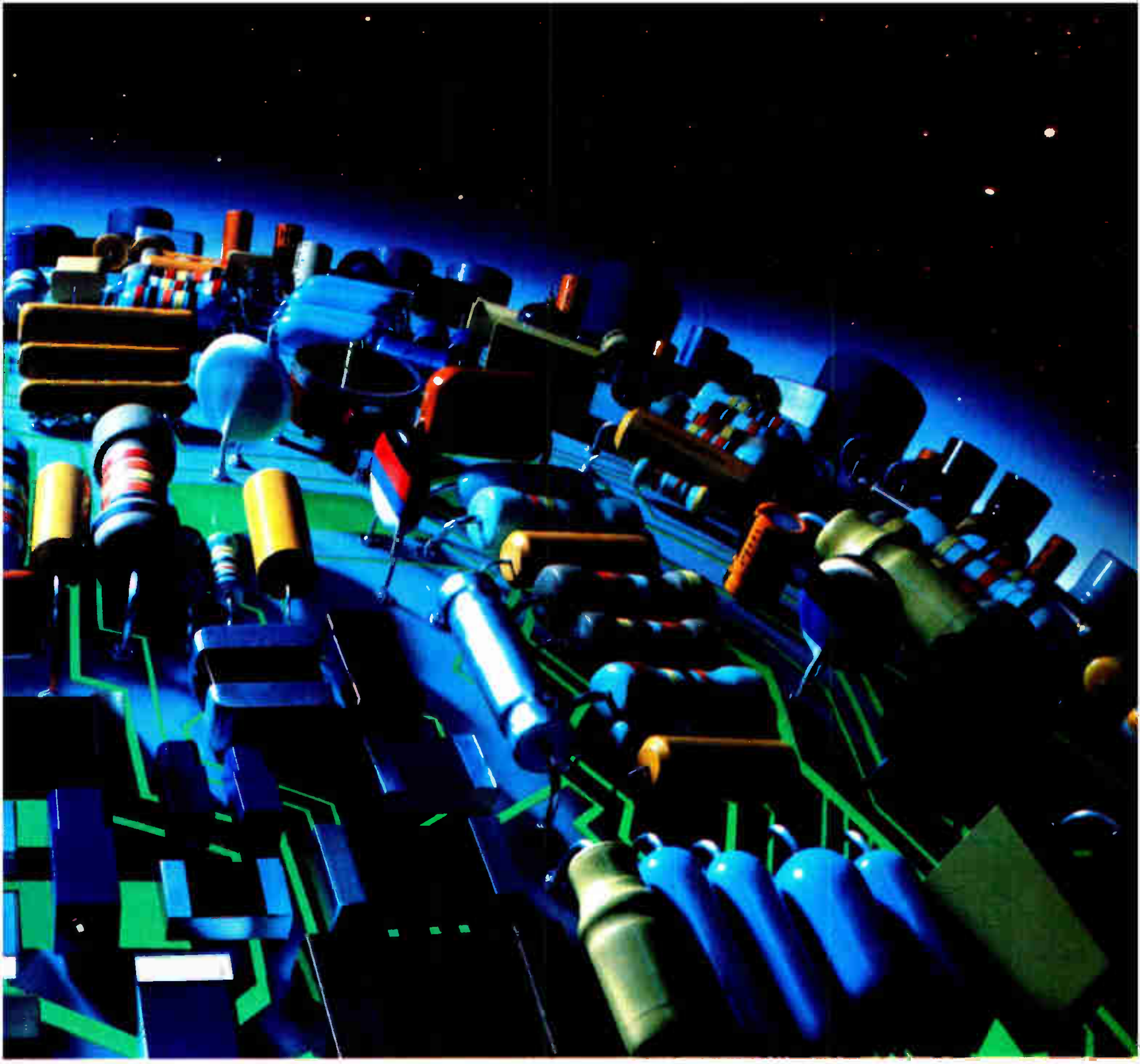
Circle 213 on reader service card



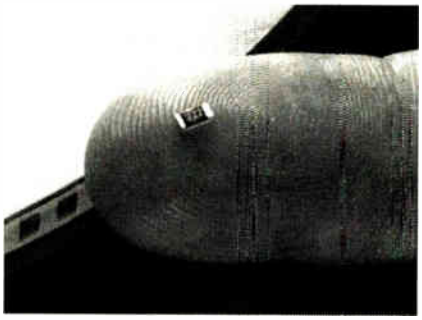
Reliability across the board.
It makes a world of difference.



from ¼ to ¾ W. Neohm's resistive element is a thin film of metal obtained by evaporation of a nickel-chromium alloy in modern vacuum machines onto a high-purity alumina core (or steatite for medium-power applications). Next, a spiral is cut through the film to the nonconductive substrate by an automatic laser.

Metal caps are then force-fitted onto the ends of the cores to allow perfect electrical and mechanical connections with the resistive element. The leads are tin-lead electroplated copper, highly resistant to oxidation even after long storage periods.

Allen-Bradley is another company that vacuum-deposits nichrome film on solid alumina substrates. Its resistors are then laser-trimmed for tight tolerances, down to ±1%, and stability. On the other hand, Dale, Mouser Electronics, and KOA Speer Electronics Inc., a Bradford, Pa., subsidiary of KOA Denko are some of

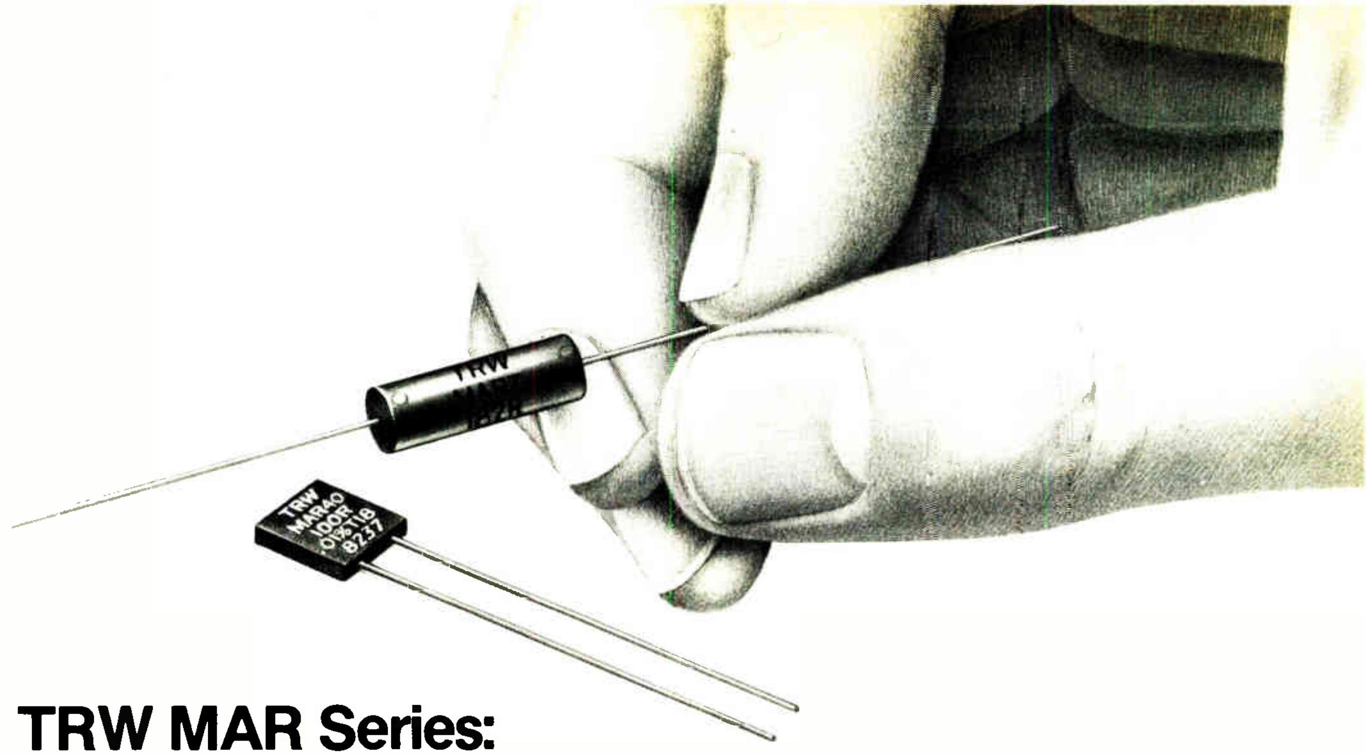


Glass-passivated on pure alumina substrates, the P series chip resistors from Stetron International Inc. are available in resistances that stretch from 10 Ω to 3.3 MΩ. The Markham, Ontario, firm packages the chips on 8-mm tape for use with automatic printed-circuit-board placement equipment. [Circle 423]

the many companies that use sputtering techniques to manufacture their metal-film resistors.

Corning Glass Works also produces a multitude of metal-film resistors. Using its expertise in glass, the Corning, N. Y. company makes a line of flameproof resistors with a ceramic insulating coating. With models having power ratings as low as ½ W, the resistors are especially suited for circuitry where functions, environments, and duty cycles demand small, low-power resistors with exceptional frequency characteristics and the ability to withstand overloads up to 100 times the rated power without any trace of flame.

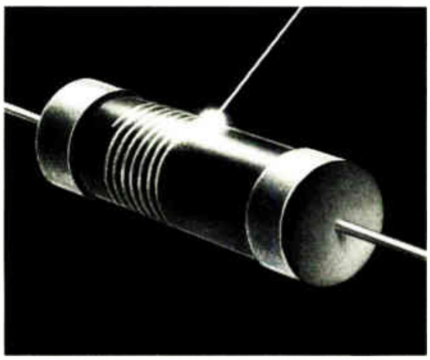
Vishay Intertechnology Inc., of Malvern, Pa., offers a resistor line using its Bulk-Metal-film foil resistive element. Selected temperature-coefficient tracking is available to 0.5 ppm/°C. The Bulk-Metal foil alloy used in Vishay products also provides exceptional long-term shelf- and load-life stability and high-frequency response characteristics. Self-generated noise is so low as to be virtually unmeasurable and resistance tolerances are readily



TRW MAR Series: discrete design flexibility in an ultra-precision bulk property metal film system.

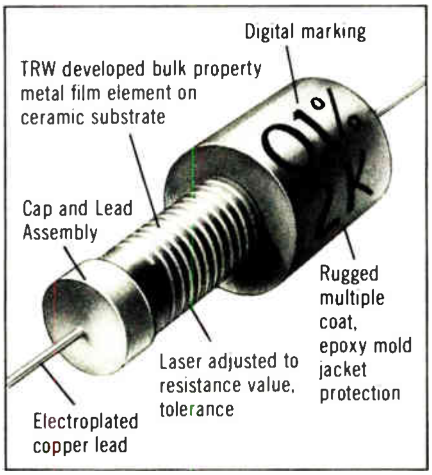
TRW MAR Series metal film resistors advance the state of the art with bulk property deposition, and ultra-precision laser trimming as low as ±.01%.

TRW ultra-precision MAR Series optimizes parameters like accuracy, speed, reliability, and resistance range. Extremely low -30 db noise level and 11.6 nanosecond rise time.



More cost effective than precision wirewounds. Reliable film construction, compact size, and transfer molded encapsulation.

Rugged multiple coat, epoxy molded jacket protection with easy-to-identify digital marking. Extremely stable base range deposition combined with laser magnification techniques.



Now also available in an economical conformally coated industrial version.

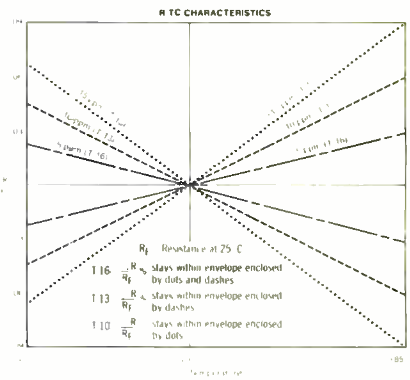
MARS are available in discrete sizes from 1/20 to 1 watt including the box radial MAR 40.

MIL-R-55182 qualified to RNC55. Resistance range capability from 10 ohms to 10 megohms. Board space as low as .015 sq. inches.

Absolute TCs from ±2 ppm/°C to ±15 ppm/°C. TCR tracking to ±1 ppm/°C. Tolerances from ±.01% to ±1%.

These characteristics are available in discrete, matched set and modular network configurations.

Matched sets and packaged ultra-precision networks can be engineered to your custom specifications.



Call your local TRW distributor.

Or the TRW Fixed Resistor Distributor Operation, 215-923-8230. For technical information call 512-992-7900, or write: TRW Resistive Products Division, 4222 S. Staples Street, Corpus Christi, TX 78411

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available to as low as ±0.001%.

Metal-film resistor technology lends itself to construction of precision resistors—devices with lower temperature coefficients, lower noise, and tighter tolerances, among other features. Dale, for example, offers precision metal-film resistors with tolerances down to 1%, 0.5%, 0.25%, and 0.1%. Resistors with power ratings as low as 1/20 W are available.

Achieving Precision

Dale's market analyst, Chris Rathe, explains that there are tighter controls on the processing of the precision film resistors than on regular resistors. For example, heat treatments and calibration techniques are used.

Lester Rice, president of KOA Speer, also indicates his company keeps tighter controls in production. KOA Speer's precision resistors are manufactured at a slower pace as well.

Almost all of the companies mentioned have lines of what are called established-reliability resistors, devices that are targeted for the military market. Corning's precision metal-film resistors are available in military versions that have power ratings down to 1/20 W and can operate in temperatures up to 125°C. The temperature coefficient is just ±50 ppm/°C. Also available is a 1/10-W part with a ±25 ppm/°C temperature coefficient.

In terms of temperature coefficients, one of the most precise resistors available is a self-correcting thermotropic resistor from Vishay. The VHP100's temperature coefficient essentially is 0. Its self-correcting thermal stability is achieved by programming the resistance to change or turn in the desired direction in response to a specified stimulus (tropic); the stimulus in this case is the temperature (thermo). As temperature changes cause the resistance to move away from the desired ohmic value, the corrective factors reverse the direction of resistance change to restore the resistance to its initial ohmic value.

Since the resistor's temperature coefficient is almost immeasurable at 0.6 ppm/°C, Vishay suggests a new term, window, to get a grip on its actual value. Window specifies the total temperature coefficient across the device's entire temperature range. The resistance of Vishay's part stays within a 60-ppm/°C window over the entire −55-to-+125°C military range. For comparison, a resistor with a typical ±5-ppm/°C temperature coefficient would be contained in a window of 900 ppm/°C.

Many customers who need more board space but are not ready for the chip resistor, have yet another package alternative with two lines of resistors, the D series carbon-film and the N series metal-film, from Stetron International Inc., of Markham, Ontario. These parts, which can withstand solder dipping, can be mounted on the bottom of the board, thereby reducing the space used. The resistors can withstand solder-flux temperatures of up to 260°C for 10 seconds without causing detrimental effects to the resistor, the company says. Parts are available in power ratings from 1/6 to ½ W and resistance values from 22 Ω to 10 MΩ.

Although the metal-film market is gaining market share at the expense of other resistor technologies, it, too, is subject to erosion due to the increased use of chip resistors and resistor networks, both of which offer considerable pc-board space savings over their axial-leaded counterparts.

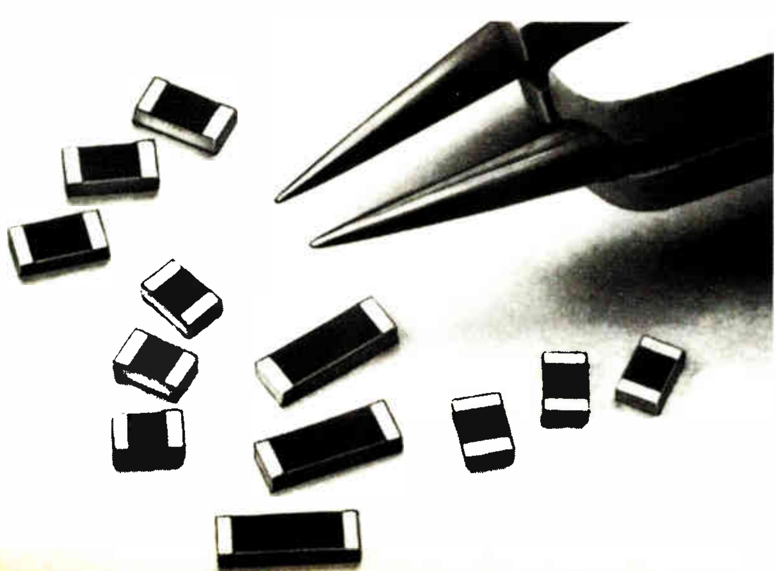
Chip Resistors

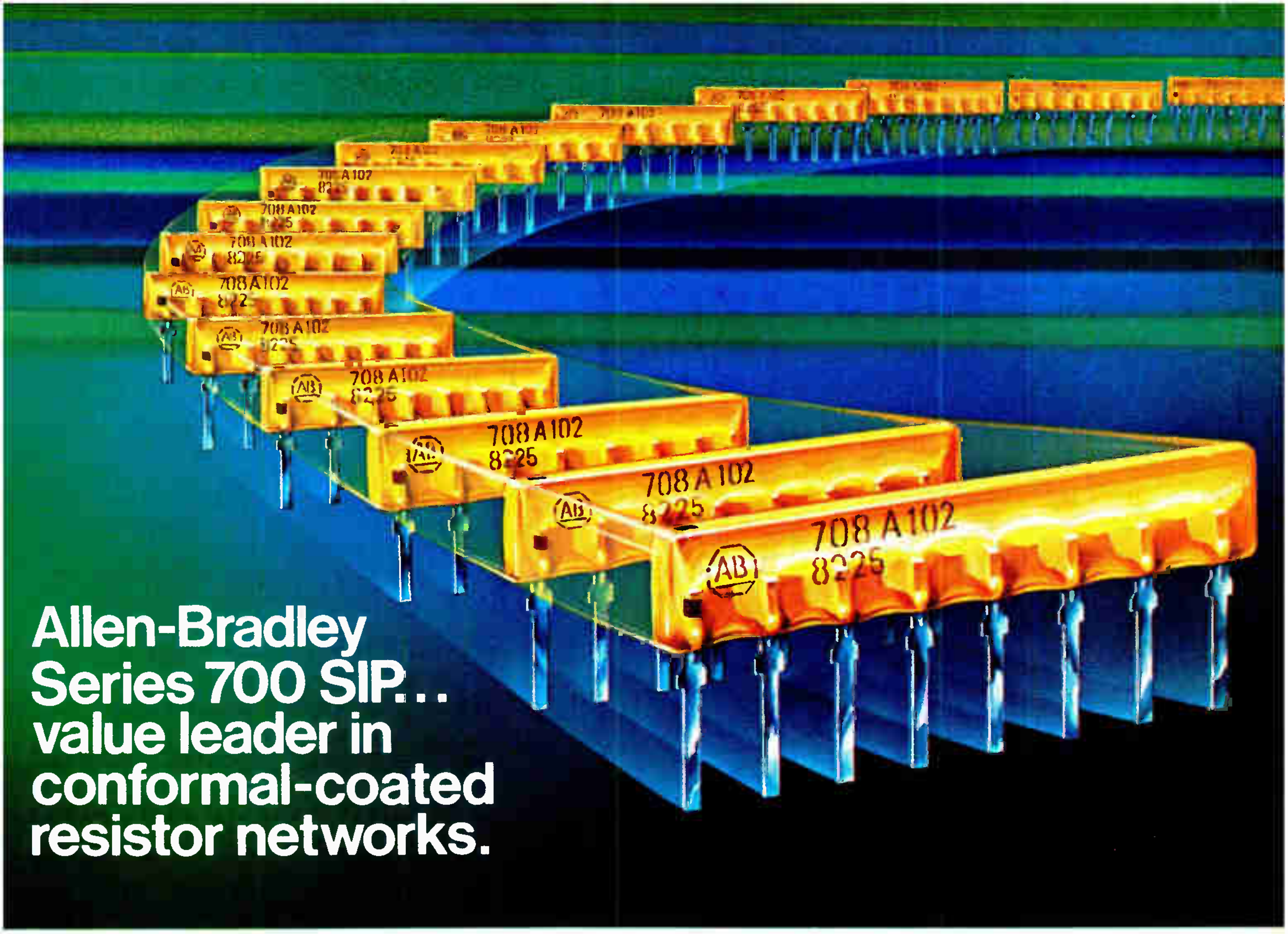
Perhaps the most exciting resistor technology, in terms of its growth potential and what it has to offer thick-film hybrid circuit makers and designers working with surface-mounted integrated circuits, is chip resistors. *Electronics* predicts that the 1984 market for chip resistors will approach $35 million.

These small light chips are well-suited to automatic placement and wave-soldering onto pc boards. Typically they are 1.6 by 3.2 by 0.6 millimeters, although some half that size are available. This regularity of structure is a boon to automated design because standard rectangular shapes are more convenient in computer-aided layout. Chip resistors have low parasitic inductance and also hold the potential for good accuracy and temperature-drift specifications.

The bulk of available chip resistors are constructed using the same thick-film techniques used in making hybrid circuits. According to Neohm, chip resistors consist of a ceramic body on which is deposited resistive paste. A wrap-around termination is placed at each end of the resistor to allow reflow or wave soldering. The resistive layer is

The RMD series of chip resistors from Mepco/Electra is available in four sizes, ranging from 0.05 by 0.05 in. to 0.05 by 0.15 in. with a maximum height of 0.04 in. Qualified to the P level of MIL-R-55342, this established-reliability line of resistors has tolerance ratings down to 1% and temperature coefficients as low as ±100 ppm/°C. [Circle 426]





All gold-colored networks are not alike! There are meaningful differences between Allen-Bradley networks and look-alikes, including "generic" SIPs.

Top marked pin #1 indicator speeds assembly and inspection, particularly on densely packed boards.

True low-profile package meets the popular .190" maximum package height specification. Some look-alikes are too tall.

Legible laser marking. Permanent laser marking is easy to read and resistant to board washing fluids.

Allen-Bradley quality. Our aggressive program, TQMS (Total Quality Management System), is based on quality materials, proven domestic manufacturing and skilled people. Quality is built from the start into each network for performance with demonstrated consistency and reliability.

Availability. Select from a wide range of Series 700 standard circuits and popular ohmic values in 6, 8 or 10 pin packages.

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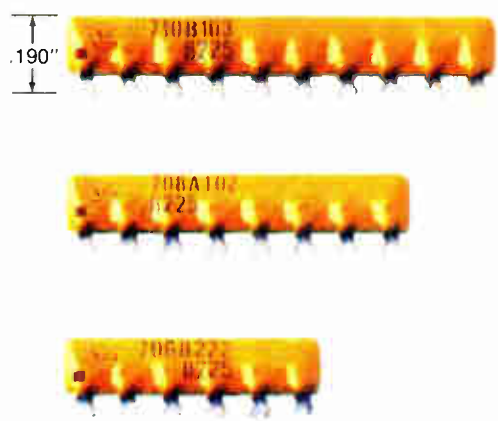

Series 700 — 6, 8 and 10 pin; 50 resistance values from 22 ohms to 1 megohm.

We close quality gaps...like nobody else.

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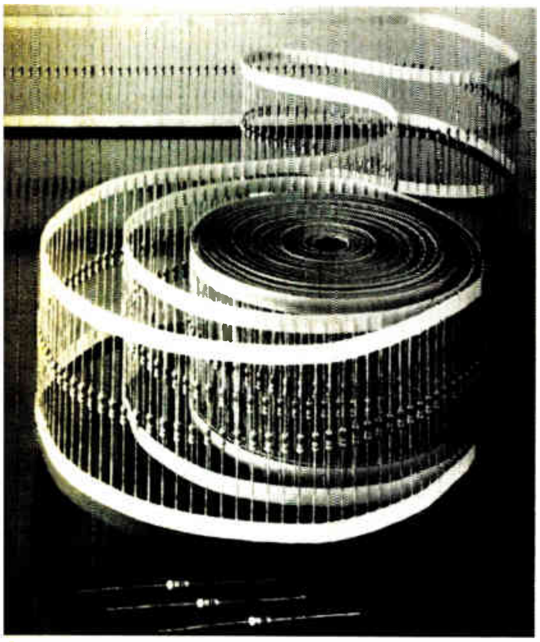
EC 247

Circle 217 on reader service card



Packaged on standard Electronic Industries Association RS-296-D Class I tape reels for automatic-insertion equipment, these metal-film resistors from Allen-Bradley Co., Milwaukee, Wisc., are rated at ¼ W at 70°C with ±1% tolerances and ±100 ppm/°C temperature coefficients. Resistances vary from 10 Ω to 1 MΩ. [Circle 427]

covered with a protective coating to assure mechanical and environmental integrity. The fundamental requirements for a substrate can be summarized as:

- Excellent electrical insulation.
- Mechanical strength to support the screen-printed components and added components.
- Dimensional stability at the firing temperature of thick films (usually 850°C).
- Good thermal conductivity.
- Dimensional characteristics (planarity, thickness) that meet the precision needs of screen printing and the surface characteristics (roughness) upon which some screen-printed-film properties depend.
- Producibility in different shapes, thicknesses, and with holes for inserting output pins.

Of the materials that can be used—cordierite, steatite, forsterite, berylia, and procelain—alumina is the most common because it has all the desirable properties listed above. The purity of ceramic varies from 85% to 99.9%.

The resistive pastes are obtained by dispersing a glass powder and a conductive powder in an organic vehicle and thinner. Different proportions of the glass and conductive powders produce a wide range of resistivities so that resistors can made that vary from a few ohms to hundreds of megohms.

User Calibration

Allen-Bradley's BC line of chip resistors, one of the first to be offered by a U. S company, has a user-trimmable option so that the user can calibrate the resistor in a system. Resistors can be laser-trimmed under actual circuit operating conditions, providing in-circuit setability.

Dale offers a line of resistors supplied with either one-surface or wrap-around terminations and a similar line of established-reliability versions that meet the MIL-R-55342 military specifications.

Panasonic Industrial Co., Matsushita's Secaucus, N. J. subsidiary, has a line of chip resistors composed of a metal-glaze element on a high-purity alumina substrate coated by special glass. The unique construction of the chip's termination prevents silver migration of inner electrodes by special coating of the resistor edge.

International Manufacturing Services Inc., a Portsmouth, R. I. company formed 10 years ago to serve the hybrid circuit industry, prides itself on its ability to deliver chip resistors overnight. IMS president Joseph P. Earabino says that the firm can receive a call from the West Coast at 3:00 p.m. and have the parts delivered to the customer out there by 11:00 a.m. the next day.

The firm's chip-resistor line is broad, ranging from 30-mW to 10-W parts, with resistance values from 10 Ω to 20 MΩ and tolerances from ±1% to ±20%. On special order, customers can get resistance ranges from 1 Ω to 10 Ω and 26 MΩ to 100 gigohm. Like Allen Bradley's chip resistors, IMS's units can be actively trimmed to match circuit requirements.

In picking a chip resistor, it is important to find out what its tolerance to soldering is. For example, the chip resistors from KDI Pyrofilm Corp. Whippany, N. J. have a less-than-0.5% resistivity change when completely immersed for 4 s in 360°C molten solder.

The solder acts both as an electrical contact and mechanical retainer. Placement of chips can be done by any one of the commercially available machines. The chips' rectangular shape, tight dimensional tolerances, and tape and reel packaging make them suitable for automatic placement. Chips can be mounted on pc boards or ceramic substrates. Their wrap-around terminations lend themselves to both reflow and wave soldering. Chips can be mounted on the bottom side of a double-sided pc board, thus practically doubling space utilization.

Widespread Uses

Chip resistors have found their way into television sets, radios, tape recorders, watches, video cameras, calculators, instrumentation, telecommunications equipment, medical equipment, and automotive electronics. The penetration of the chip resistor into traditional resistor applications will depend upon the former's ability to be price-competitive, to have an economy of scale that offsets the cost of placement equipment, or to afford the resistor user significant pc-board space savings to justify the premium price of the chips.

For now, chip resistors are caught up in a vicious circle. Usage of chips is not high because they are expensive and placement equipment is expensive. The price of chips would come down as the makers went down the learning curve, which of course occurs only when they are making lots of chips. And placement-equipment makers could sell the equipment for less if they knew that there would be a large demand for it—which, of course,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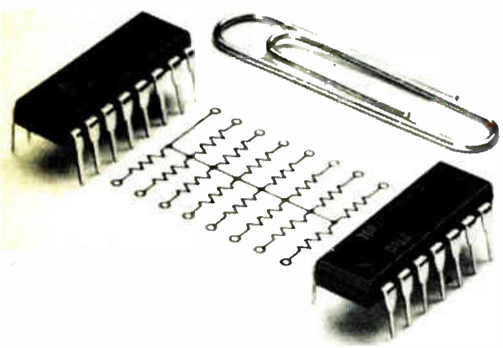

These thin-film resistor networks from Dale Electronics Inc. are available with 13 or 15 nominally equal resistors, each connected between a common pin and a discrete board pin. The Columbus, Neb. firm's networks have tolerances to within 1%, 0.5%, and 0.1% and temperature coefficients of ±25 ppm/°C. [Circle 424]

depends on volume sales of the chips.

Although further price erosion is expected as manufacturing techniques improve and increased usage occurs, the cost of the chip resistor is not expected to match that of the current axial-leaded metal-film resistor in the the near future.

Another resistor area where there is growth and action is in networks.

Electronics expects the 1984 market for the thick-film segment of resistor networks to be a bullish $159 million, an 11% increase over last year's market, and for the infant thin-film segment to be $19.8 million. Dale's estimate for thick-film networks is virtually identical at $160 million, while it sees just a little better growth for thin-film networks, at $21 million.

Corning estimates that 1983 sales of resistor networks hit $150 million and predicts a 25% annual growth rate. Allen-Bradley concurs, according to Jack R. Polakowski, the company's manager of technical marketing.

"The demand for thick-film dual-in-line-packaged networks has multiplied several times since 1975, from 15 million units to over 100 million, in 1983, and should double again to over 200 million units" within a few years, Polakowski says. Similarly, thick-film networks in single in-line packages have more than quadrupled in volume in the same time period, from 65 million units to over 300 million, and should double again to over 600 million units in the near future, he adds.

The rush to packaged networks is due to the advantages they bring the designer. Jim Childress, networks sales manager of Beekman Instruments Inc., Fullerton, Calif., reports that networks' primary benefits are to reduce board real estate and cost while increasing reliability. According to Walter W. Fischer, who is the manager of marketing communications for Allen-Bradley, the networks provide high resistor density and space savings on the board. With a network, moreover, there is only one part to purchase, stock, inspect, and assemble. And, with all the resistors on one substrate, there is similar electrical and environmental behavior.

Manufacturing Process

The thick-film network manufacturing process is virtually identical to that of chip resistors. Most manufacturers offer their networks either as individual resistors or bused together in series or parallel and housed in a variety of packages.

An example of the space savings that can be gained with a DIP is that 28 discrete ⅛-W resistors in a digital line termination can be replaced by one network in a 16-pin DIP. A SIP not only achieves comparable savings, but can be stacked side by side on the pc board, with four SIPs fitting in the same hole spacing as one DIP. About 75% of all networks come in SIPs, and, by all accounts, this ratio is expected to hold up for the next couple of years.

The Thick-Film Products Operation of Sprague Electric Co., in Nashua, N. H., which makes thick-film networks

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Circle 220 on reader service card

in both DIPs and molded and conformally coated SIPs, estimates that by placing up to 28 resistors in a standard DIP, the costs related to the stocking and assembly of a large number of discrete components are reduced by 85%. The pc-board area required typically drops by over 40%, the company says.

One of the major changes in SIP resistor networks is the emergence of a lower-cost conformally coated net with a clip-on lead frame. This configuration does not have the ruggedness and performance of the standard SIP construction, and it cannot currently be automatically inserted—but because it can be mass-produced on computer-controlled equipment, it can lower user costs.

With networks, which contain from 3 to as many as 19 resistors, resistance is specified as a range, typically from a few ohms to a couple of megohms. Temperature coefficients can easily be in the ±50 ppm/°C.

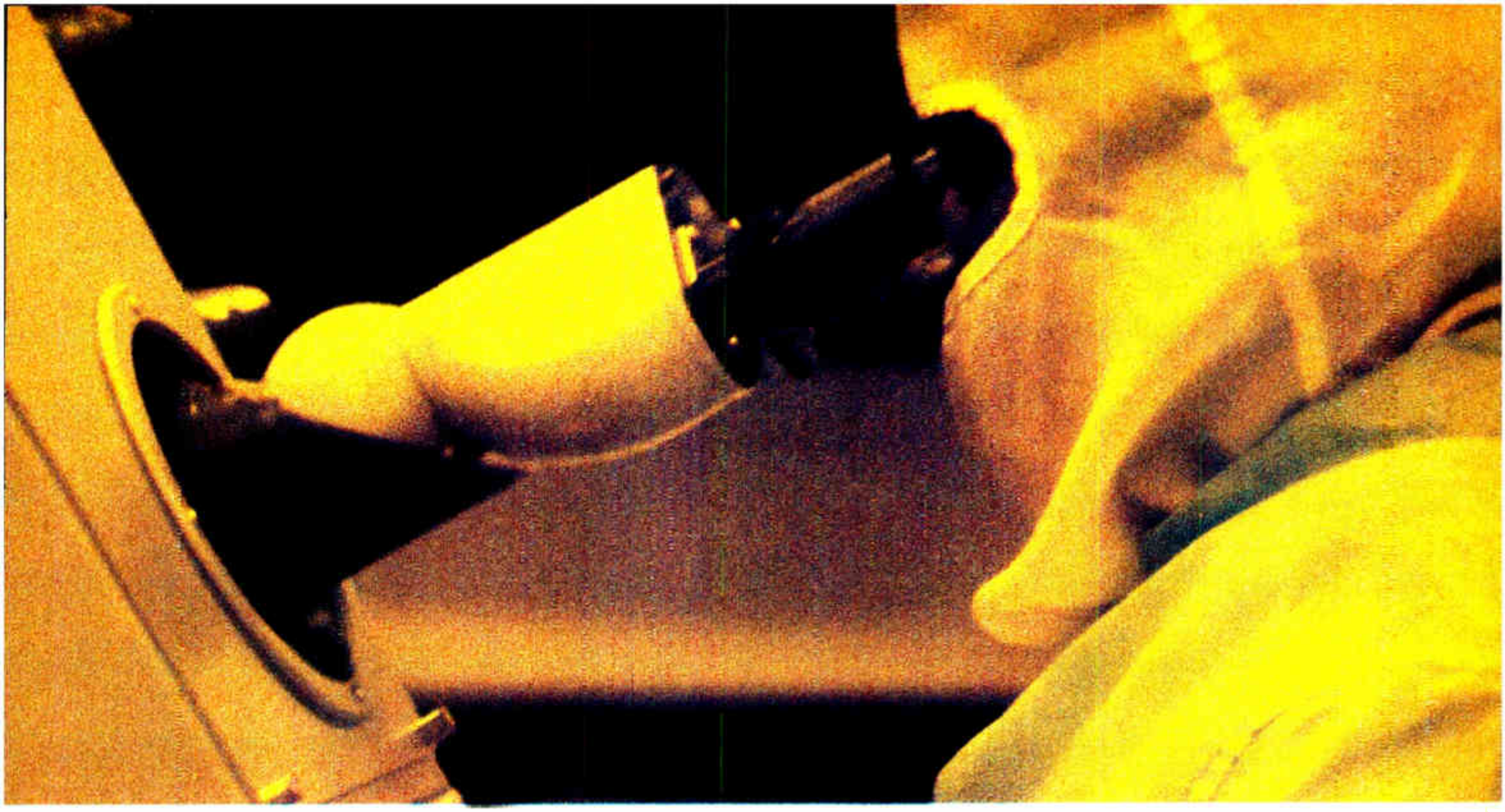
Many companies are varying the packaging style of their networks. Panasonic offers a low-profile line of networks that rise just 0.2 in. above the board. Mepco/Electra houses resistors designed to meet MIL-R-83401 specifications in flat packages. Vishay makes a line of resistor networks housed in various TO packages, including the TO-18, TO-5, and TO-8. The TO-18 package is a four-pin can that houses up to five of Vishahy's 50-by-50-mil chip resistors or one 150-by-50-mil resistor and two 50-by-50-mil chips.

Terminator Nets

Makers of supercomputers using 10K and 100K emitter-coupled-logic ICs can make good use of terminator networks from Mepco/Electra. The 10K ECL Terminator is an eight-pin conformally coated SIP, consisting of six resistors, one 0.01-microfarad capacitor, and a common pin. The 100K ECL Terminator is a 10-pin conformally coated SIP with six resistors, two 0.01-μF capacitors, and two common pins. In the 10K part, resistance values of 68, 100 and 150 Ω are available, and in the 100K model, values of 50, 68, and 100 Ω can be had.

KDI Pyrofilm offers what it calls chipless thick-film RC networks. These nets do not contain add-on capacitor chips. Instead a thick-film screen-and-firing technique is used to fabricate the capacitors as an integral part of the network. The part's resistance range is from 10 Ω to 10 MΩ, and the capacitance range extends from 10 picofarads to 560 pF. Tolerances can be within ±0.5%.

Corning, which recently expanded



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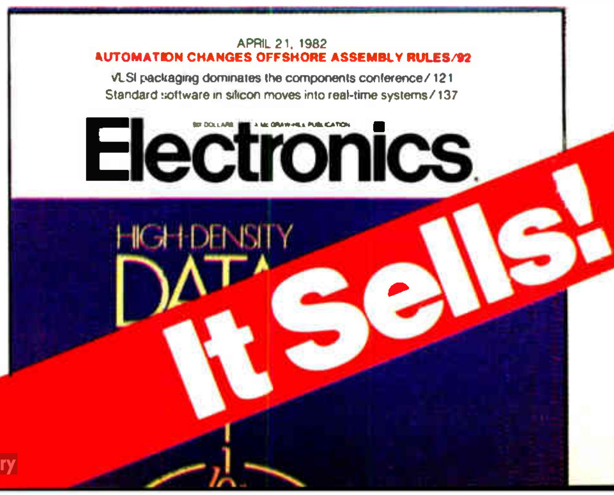
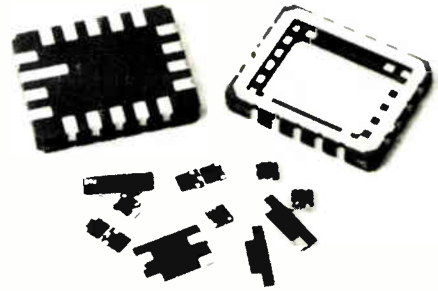


its custom capability, now can make custom resistor, RC, and capacitor-array networks in the SIP configuration. Custom resistor circuits are also available in DIPs.

In manufacturing its networks, Allen-Bradley uses high-purity glass and alumina substrates to provide good film adhesion, precision resistance tolerances, and stable operation. A chromium cobalt thin film provides consistent long-term stability. Metal-film interconnections mean no welded or soldered joints. Molded or conformally coated surfaces protect the devices against the environment, the firm says.



This ceramic leadless carrier from Vishay Intertechnology Inc., Malvern, Pa., is a 16-terminal network with gold-plated terminals that wrap around the package to provide for either socket mounting or reflow soldering. The carrier can accommodate up to 12 of Vishay's 50-by-50-mil or four 150-by-50-mil chip resistors. [Circle 425]

Dale offers a pair of thin-film resistor networks with tolerances as low as ±0.1% and temperature coefficients down to ±10 ppm/°C. Resistance ranges from 100 Ω to 100 kΩ. The first line, in molded DIPs, provides a choice of 13 or 15 nominally equal resistors each connected between a common pin and a discrete pc-board pin. The second line, also in molded DIPs, offers a choice of 7 or 8 nominally equal resistors with each resistor isolated from the others and wired directly across. Temperature-coefficent tracking is ±5 ppm/°C over a −55-to-+125°C temperature range.

Complementary Nets

According to Allen-Bradley's Polakowski, thick- and thin-film networks are complementary. The thick-film nets are aimed principally at performance levels of typical discrete metal-film resistors, while the thin-film nets have the precision-resistor properties of tight tolerances, tight temperature coefficients, and tight tracking. The thin-film nets are suitable for replacing individual precision resistors and matched pairs of resistors. What's more, the greater demand for ±0.1%-tolerance resistors is met by thin-film resistor networks,

RESISTORS

Polakowski points out.

As the end-product markets, principally computers, that make use of thick-film resistor networks continue to show substantial growth, this type of resistor will also enjoy continued growth. This market is probably the most sensitive of all resistor markets to technological innovation and change.

On the other hand, the thin-film market is still in its fledgling stages as applications for this new product slowly develop. However, the advantages of improved temperature coefficients and resistance tolerances give this product a competitive edge over the other technologies. Applications for these products should increase as electronic equipment is asked to perform more and more functions with greater and greater accuracy. Although not a resistor type destined for the dollar volumes of its thick-film counterpart, the thin-film net will experience significant growth in the years to come.

A Time for Choices

When asked what are some important criteria a customer should consider in making a choice, Beekman's Childress said, "quality, quality, and above all quality." Fischer of Allen-Bradley says the customer should choose a resistor that meets the application requirements, that has a proven history of quality and reliability, and that is cost-effective when judged not only by current acquisition cost but by total product life cost.

Along those lines, Lee Sanchez, product manager of Stetron, picks out certain resistor performance parameters that should be kept in mind: line-power rating, resistance, overload voltage, noise effect, tolerance, current rating, and temperature coefficient.

James Ramich, marketing manager for resistors at Corning, believes the choice has to be made with broader concerns, such as service, quality, technical support, financial strength of the supplier, worldwide supply capability, and price. □

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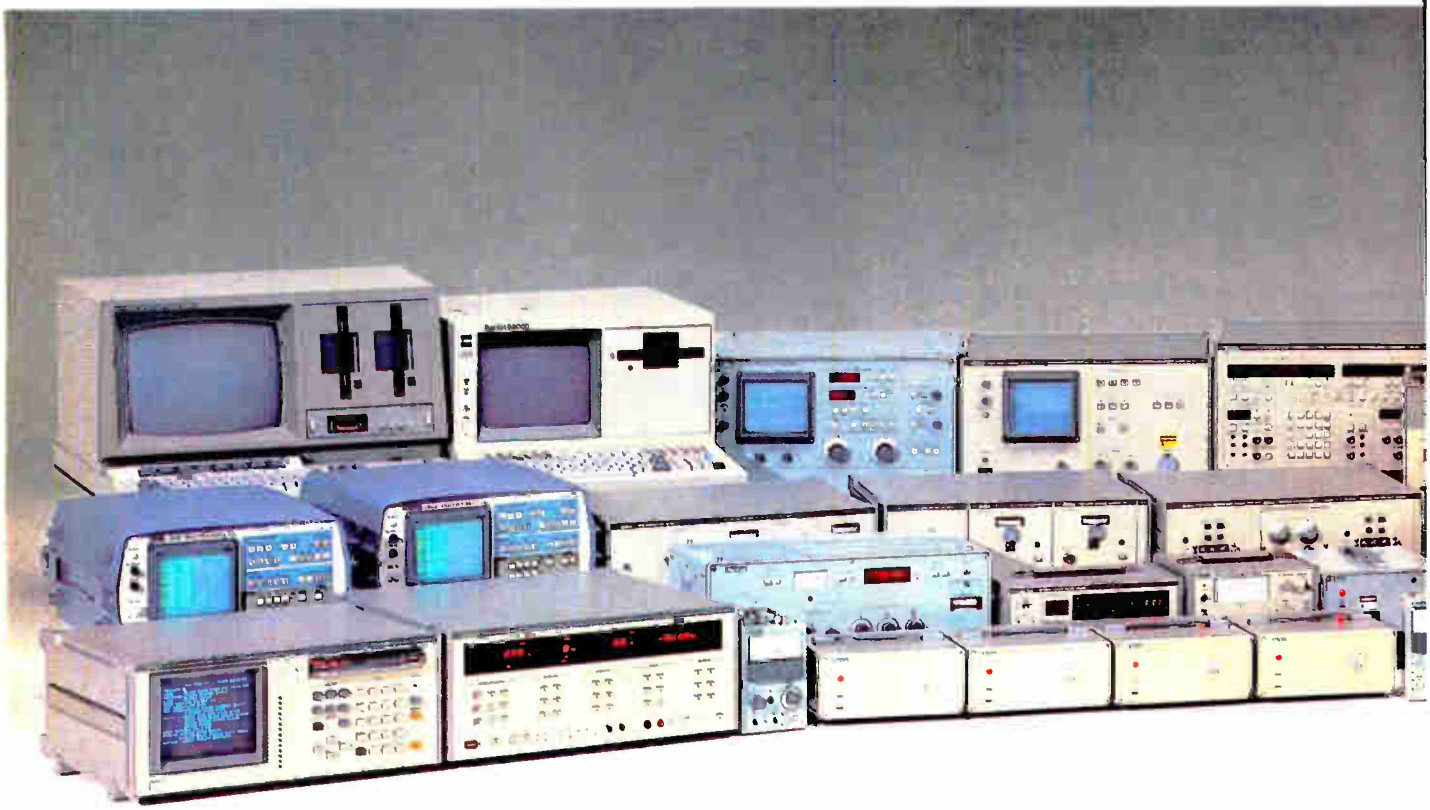

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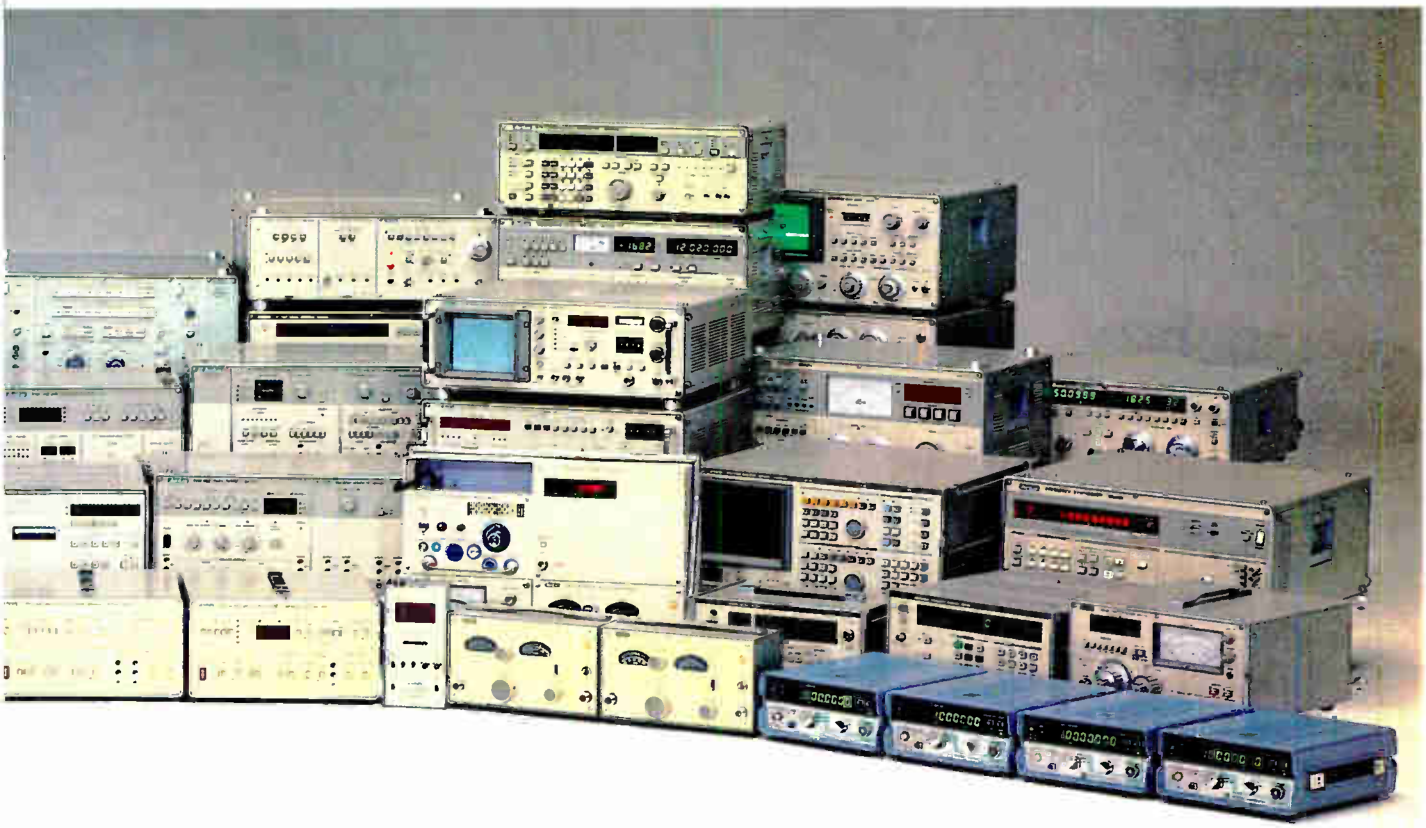

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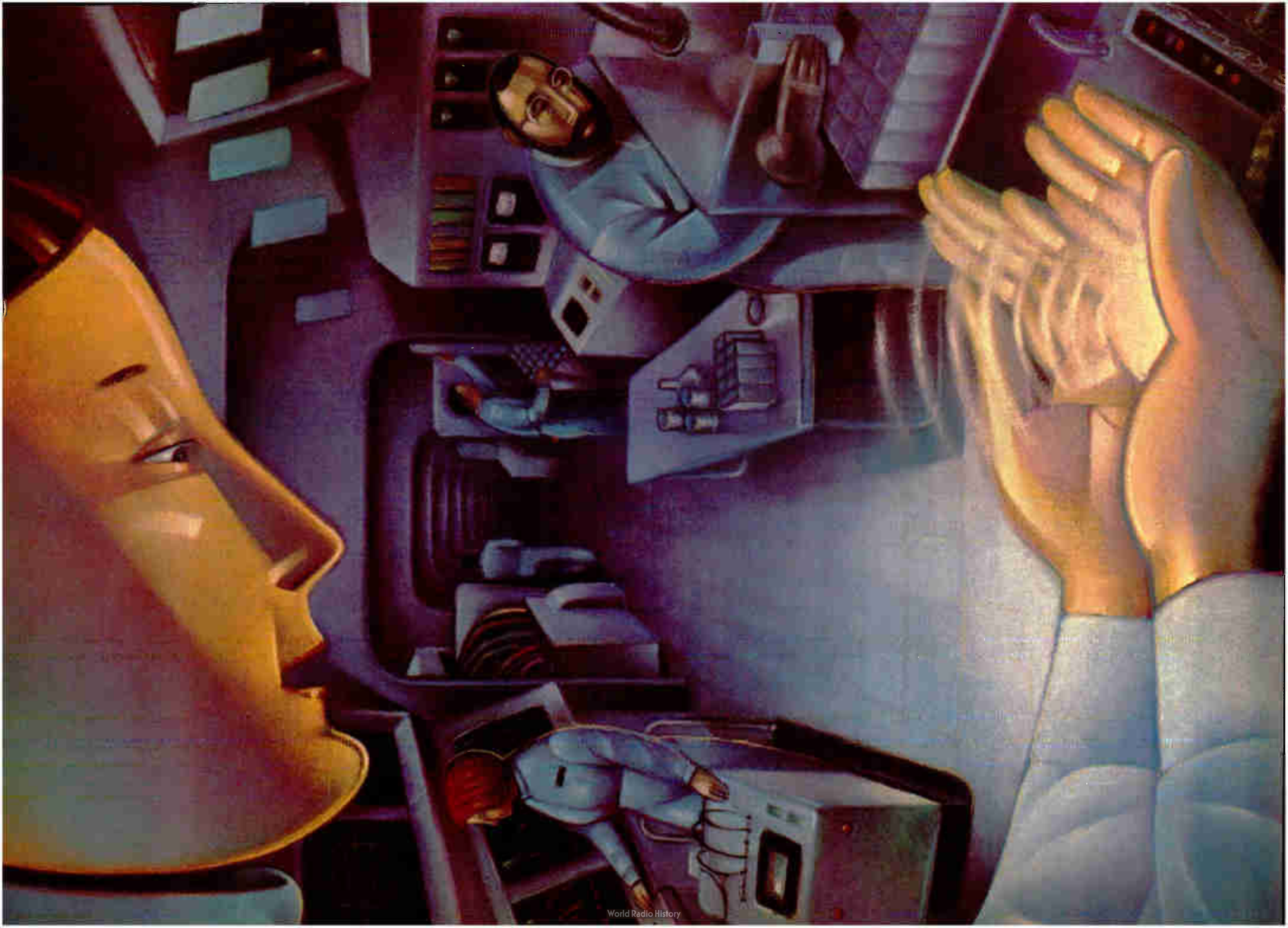

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Board controls Winchesters for IBM XT

The 5¼-in. drive controller follows ST506 interface standard; changing a single chip modifies the board for other computers

by Larry Waller, Los Angeles bureau

With its lineup of established Winchester-disk controllers as a springboard, Western Digital Corp. is now offering systems integrators and desktop-computer manufacturers a choice of either complete stand-alone controller boards or the chips to build their own. Furthermore, the boards can be tailored to a particular application with a change in only one chip.

The first board is the WD1002-WX2, for International Business Machines Corp.'s PC XT and XT-compatible machines. A stand-alone general-purpose board, it is based on the Seagate Technology ST506 interface standard and will control up to two 5¼-in. Winchester drives. The drives do not need identical capacities or configurations; all receivers and drivers required for direct connection are included right on board.

The WD1002-WX2 incorporates two Western Digital circuits already widely used for disk control: the WD1010-05 controller-formatter and the WD1100-13 error-correction circuit. "It is a new part—the WD1015-04 control processor—which tailors the board to the XT," says Kathy Braun, director of marketing for storage-control products.

Similarly, versions of the control processor dedicated to computers other than the XT are being developed by the company. "Since we manufacture our own very large-scale integrated circuits, we can offer to systems manufacturers the option of boards or chip sets to build their own controllers," Braun says.

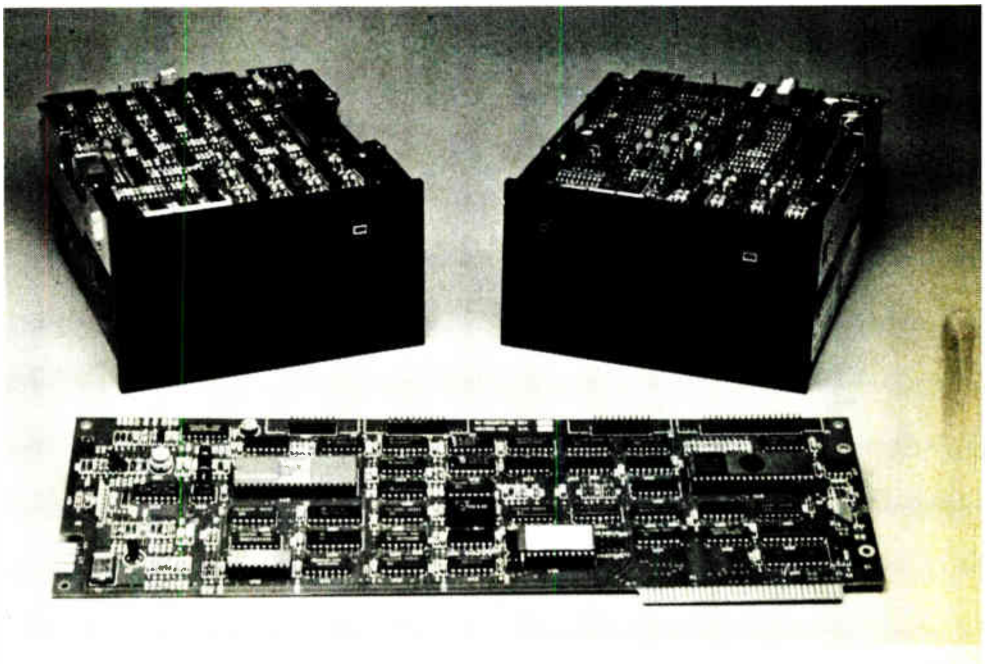
The WD1002-WX2 provides data-transfer rates of up to 5 Mb/s, along with on-board data separation and write-precompensation circuitry designed for controlling Winchester disk drives. One of its two interface buses is a 20-bit bus that provides addressing for processor instruction execution and the on-board read-only memory. An 8-bit bidirectional data bus permits communications between the host and controller, in addition to handling status communication. Access to the controller is through either host input/output addressing or direct memory addressing.

Daisy chain. The Western Digital board has four on-board connectors, the largest a 62-pin card-edge type for interfacing with the host. A 34-pin connector allows two drives to be daisy-chained; and two 20-pin connectors permit direct linkage to the controller on each drive.

The controller ensures that the format of a track is completed in a minimum of 300 μs before the signal activating the drive. Thus the drives can use the servo-wedge embedded-servo scheme, which lumps the gap areas at the end of the track rather than distributing them equally among the sectors within it.

Another feature of the board is sector interleaving, whereby the controller will accept any interleaving value between 0 and the number of sectors per track minus 1. The interleaving value then tells the controller the location of the next logical sector in relation to the current one.

Firmware driver routines for the controllers, supplied by Western Digital, reside in a ROM that can be directly addressed by the host processor. A board socket wired to accommodate a 28-pin dual in-line package accepts a 2764 electrically progammable ROM, a 64-K ROM, or a 32-K ROM.



The specifications of the controller include 17 512-byte sectors/track, eight head-select inputs, as well as two drive-select lines; and the write-precompensation time is 12 ns. The maximum allowable cable length is 20 ft for both control of a daisy-chain setup and for data applications. Power requirements are +5 V dc and +12 V dc, with a maximum current drain of 1.5 A on the +5-V supply and 100 mA on the +12-V supply.

The WD1002-WX2 is available in production quantities now. It sells for $245 in lots of 100, with volume discounts available.

Western Digital Corp. 2445 McCabe Way, Irvine, Calif. 92714. Phone (714) 863-0102 [Circle reader service number 338]

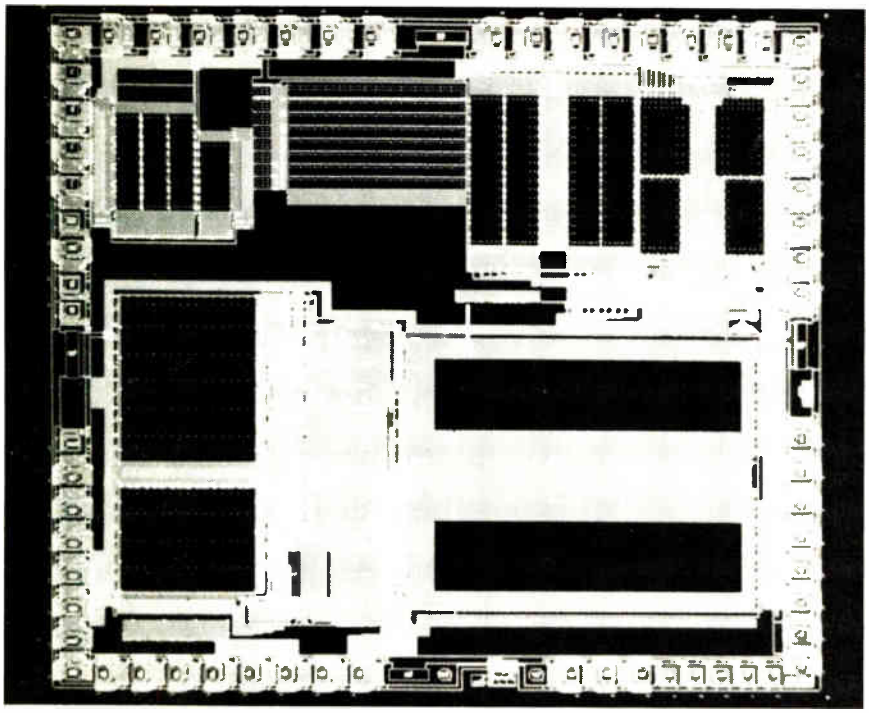
Color-graphics controller chip set reduces parts count, incorporates microcomputer

Microcomputer-based graphics systems may soon be easier to design and use and could offer significantly improved price-performance characteristics with far fewer components, thanks to a new color graphics controller chip set from NCR Corp.

Indeed, officials at the firm's Microelectronics division in Colorado Springs, Colo. are billing the NCR 7300 color-graphics controller chip (pictured) and associated 7301 memory-interface controller as the first of a new generation of graphics-controller chips with improved capabilities. For many applications, the 7300 will offer performance four to five times that of the widely used 7220 from Japan's NEC Corp., contends Michael R. Shapiro, NCR's marketing manager for logic products.

With initial samples set for availability in late summer, the 7300 will be fabricated in n-channel MOS using NCR's 3-μm, VLSI-2 process that can integrate over 100,000 transistors on chip. The 7301 will integrate about 15,000 transistors and will be built with the same process.

The NCR chip set will work in any 8- or 16-bit microprocessor-based system. Unlike the 7220, the 7300 incorporates a complete 10-bit microcomputer on chip. When used in conjunction with one to four 7301 chips that provide an interface to a frame buffer up to 1 megabyte in size, the 7300 can unburden the host processor by taking over a variety of graphics-processing tasks. These include computation of picture-element addresses for the frame buffer, control of frame-buffer refreshing and timing, and handling direct-memory-access control.



Firmware. One feature that will make the 7300 easier to use is its on-chip firmware for interpreting high-level graphics commands from the host processor. The command set is based on that proposed for the Virtual Device Interface standard currently under development by the American National Standards Institute.

Other special-feature commands in the set include an extensive windowing capability. This feature will greatly simplify the programmer's task by allowing him or her to write in terms of high-level graphics primitives, explains 7300 designer David L. Henderson. "It should really cut down the amount of time required to write new device drivers or write applications programs," he adds.

The basic data type for the 7300 is the picture element. Each pixel can contain from 1 to 8 bits of information, with each 7301 in a system contributing 2 bits of data. Thus, for a full 8-bit pixel depth, which results in the maximum-displayable 256 colors, four 7301 devices must be used. A system equipped with a single 7301 could display only four colors simultaneously.

Pixel bus. Each 7301 in a system handles 16 dynamic random-access-memory data lines from the frame buffer and provides a 4-to-1 multiplexing and demultiplexing function in transferring data back and forth between the frame buffer and the 7300. Each 7301 is connected to the 7300 by a 4-bit pixel bus. During screen refreshing, data is transferred from the frame buffer through the 7301 and into the 7300, which performs an additional 2-to-1 multiplexing function before sending the data on to the display monitor at clock rates up to 30 MHz.

Whereas chips like the 7220 re-

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Circle 167 on reader service card

quire off-board circuitry to convert digital data from the frame buffer to analog form to drive a display monitor, the 7300 integrates the digital-to-analog conversion function on the chip, Henderson points out. Separate red, green, and blue analog output ports on the 7300 controller chip can thus drive a display monitor directly with only a minimum amount of buffering to provide high-voltage isolation.

This feature alone will provide a system-level saving of at least $100, compared to using a hybrid circuit to provide the d-a conversion, Henderson estimates. Additional savings in space and cost come with the 7301 chips, each of which can replace between 12 and 20 TTL parts commonly used to do multiplexing and demultiplexing in current graphics systems, he says.

In 1,000-piece quantities, the 7300 controller chip will be priced initially at about $80 each. The 7301 memory-interface controller will go for about $15 each in similar quantities. NCR plans to begin production on the chips during the fourth quarter.
NCR Microelectronics Division, 1635 Aeroplaza Dr., Colorado Springs, Colo. 80916. Phone (800) 525-2252 or (303) 596-5612
[Circle 342]

Dense 256-K pseudo-static RAM uses C-MOS peripheral circuitry for low power

Many of the advantages of a 256-K static complementary-MOS random-access memory, but at a price comparable to that soon to be charged for dynamic RAMs, are incorporated in Hitachi's HM65256P pseudo-static RAM. The memory cells feature a dynamic single-transistor design fabricated in the same 2-μm process used in the firm's dynamic RAMs to attain a much higher packing density than is possible in static RAM cells, which need four transistors and two resistors. The memory's peripheral circuitry uses 2-μm C-MOS processing for low standby current.

The chip's 32-K-by-8-bit configuration makes it a natural for small systems such as personal computers, terminals, and printer buffer memories. It is equally suitable for graphics-processing equipment where a large memory capacity is required, and its by-8-bit configuration provides higher bandwidth than a by-1-bit or by-4-bit memory chip. The firm is now developing a 32-K-by-9-bit chip for customers who need a parity bit with each byte.

Versions are available with 150- and 200-ns access times. Internal operation is initiated when an address change is detected by the address-transition detector. Because precharging is eliminated, the part features identical cycle and access times.

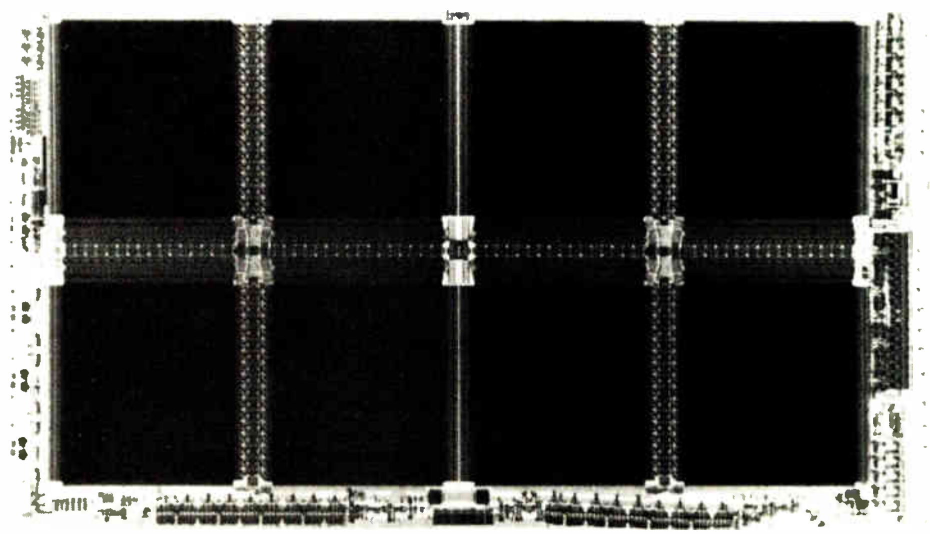
In many systems, the chip's combination of low operating-power consumption and extremely low standby-power consumption permit higher packing density, eliminate the need for cooling, and cut power-supply size and cost. Moreover, the incorporation of automatic- and self-refresh modes in this RAM favors its use in simple systems, without the bother of complex refresh control, and in some battery-backup applications.

The new chip can be used in its automatic-refresh mode in many systems that now use static RAMs because of difficulty in coordinating column- and row-address-strobe timing with read and write cycles. The self-refresh mode makes backup by battery or supercapacitor possible over a period of one to several days. True low-current static-memory chips are superior for intermittently used portable equipment with battery backup, though.

Refresh. Automatic refresh is nearly as simple as its name implies. A logic high signal is applied to the chip-select pin, and then the output-enable/chip-refresh pin is driven high at least 256 times during each 4-ms interval. Circuits within the chip detect the positive-going transition and a refresh-address counter generates the proper refresh signals in sequence.

If the refresh pin is held high for more than about 4 μs, the chip goes into its self-refresh mode. In this mode, one refresh pulse is generated approximately every 15 μs. Typical power drain is 10 mW. Power drain is higher than for static C-MOS, which flows in short, high-current pulses.

The cells' dynamic nature necessitates a 5-V power-supply voltage. True static memories can often retain information with supply voltages as low as 2 V. The RAM is housed in a 600-mil 28-pin dual in-line package with a Joint Electron Devices Engi-



neering Council pinout that extends the pinout now used for 64-K static RAMs. The chip's typical power consumption during operation is 200 mW. It falls to 5 mW during true standby mode. The chip maker has not yet set the chip's maximum values, however.

Hitachi will not market a product making full use of the 32-K-by-9-bit chip's 288-K capacity until a second source is available—even though its engineers say some equipment manufacturers always design memory systems with parity. Nor has it decided what package and pinout to use for the 288-K version.

Samples of the 256-K HM65256P will be available this month at a price of $252 for the 150-ns version and $219 for the 200-ns version. Production will start in October. Favored customers, however, will have priority, and Hitachi says that some customers may not be able to obtain samples until sometime early next year.

Hitachi America Ltd., 1800 Bering Dr., San Jose, Calif. 95112. Phone (408) 292-6404 [Circle 339]

Microprocessor peripherals build a card that replaces 15 LSI-11 timer boards

Bringing microprocessor peripheral-chip technology into DEC's Q-bus environment, Codar Technology Inc. has come up with a dual-wide board that is the functional equivalent of 15 of Digital Equipment Corp.'s KWV11 16-bit timer boards. Targeted at real-time data acquisition and digital-control applications using LSI-11 computers, Codar's model 140 M-Timer is compatible with all DEC LSI-11 and Micro-VAX I processors (16-, 18-, and 22-bit). It also can be used in 68000-based Q-bus systems.

The Longmont, Colo. company's coup rests on three Am9513 counter-timers and two Am9519A interrupt controllers from Advanced Micro Devices. Each 9513 has five 16-bit counters, which may be driven from an external source, an internal programmable prescaler, or the preceding 16-bit counter. The 15 on-chip counters can be programmed into one of 18 modes. The two 9519As offer 16 user-definable programmable or maskable interrupts.

Although the board is not software-compatible with the KWV11 boards, it may be programmed to act like them. Optional diagnostic and software routines are available from Codar on disk or tape.

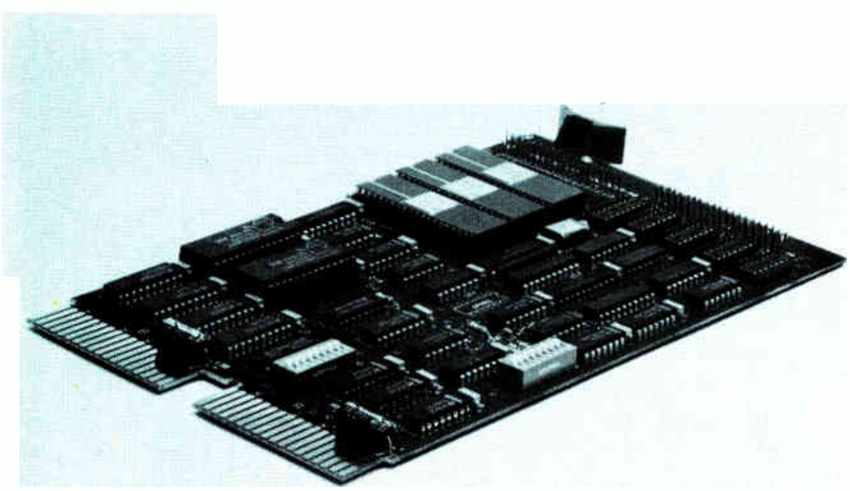
The 5.2-by-8.9-in. M-Timer module can handle such functions as frequency synthesis, duty-cycle waveforms, complex pulse generation, coincidence alarms, frequency shift keying, system-clock generation, and watchdog timing. Codar believes the timer board is particularly well-suited for a wide range of scientific data-acquisition applications and industrial-control systems.

"We think this is one of the first products that takes peripheral chips designed for the microprocessor world and integrates them into the DEC Q-bus world," says Mike Evans, president. "If discrete logic were used, it would take 15 boards to handle the same features." Systems designers may control 15 analog-to-digital converters from a single M-Timer module, he says.

In single quantities, the M-Timer sells for $875. Deliveries are made within 60 days of receipt of orders. The Q-bus counter-timer has a 76-pin input/output connector and 36 buffers, which may be configured by wire wrapping to suit customer system requirements. For original-equipment manufacturers, Codar will preconfigure M-Timer terminations, customizing the modules according to customer specifications.

The M-Timer board comes standard with a 4-MHz crystal oscillator with prescaler for timing cycles that can be stretched from just microseconds up to years.

Codar Technology Inc., 1428 Florida Ave., Longmont, Colo. 80501. Phone (303) 776-0473 [Circle 344]



CP/M-based computer is housed on Eurocard

With the aid of five programmable-array-logic chips and one gate array, Megatel Computer Corp. has packed a full 256-K-byte, CP/M-compatible computer—including extensive input/output facilities and control electronics for ST506-type Winchester and most floppy-disk drives—onto a single Eurocard measuring 3.9 by 7.5 in. The Quark/300 is based on a 6-MHz Z80B microprocessor and also includes a video controller with bit-

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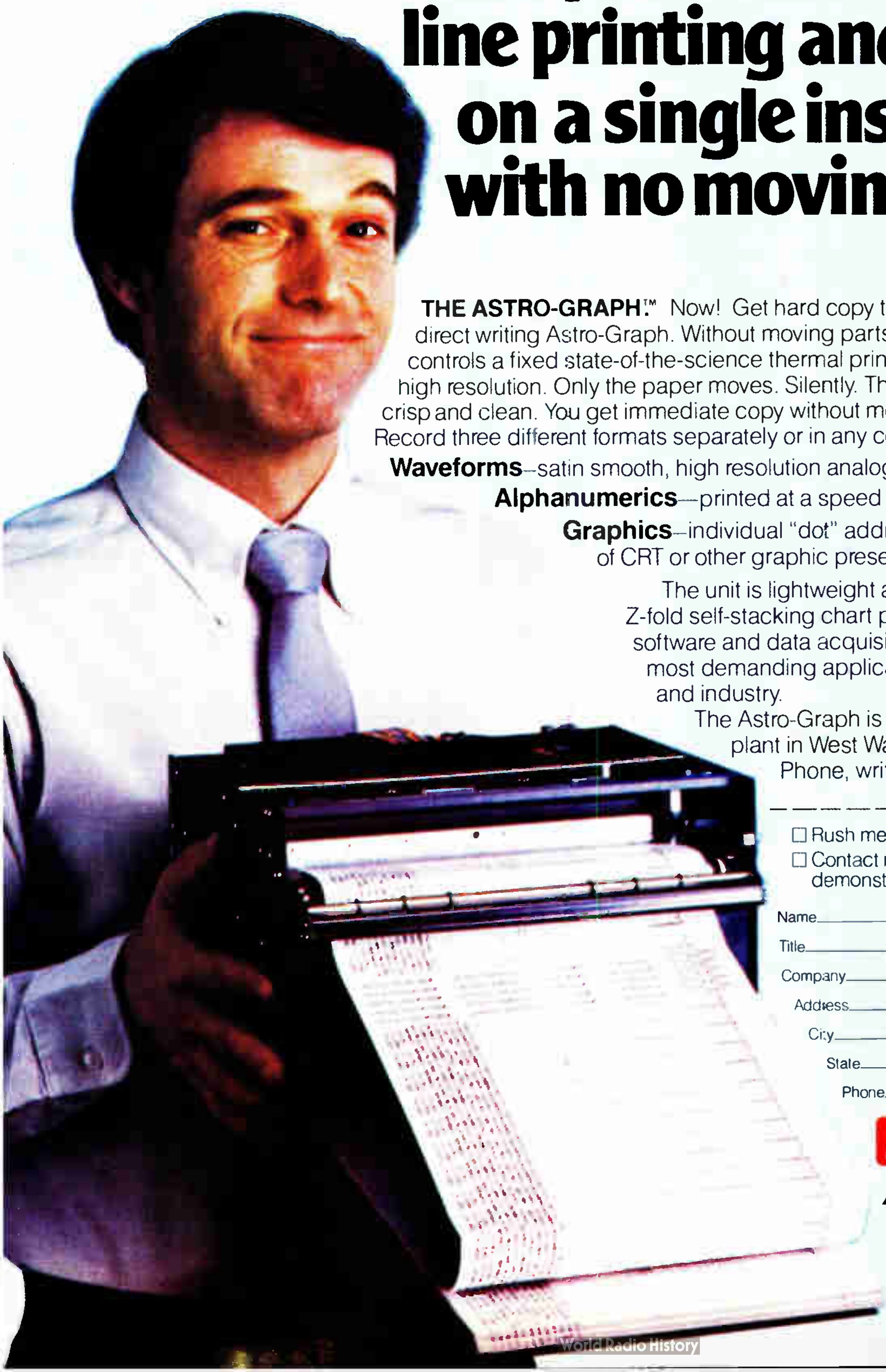

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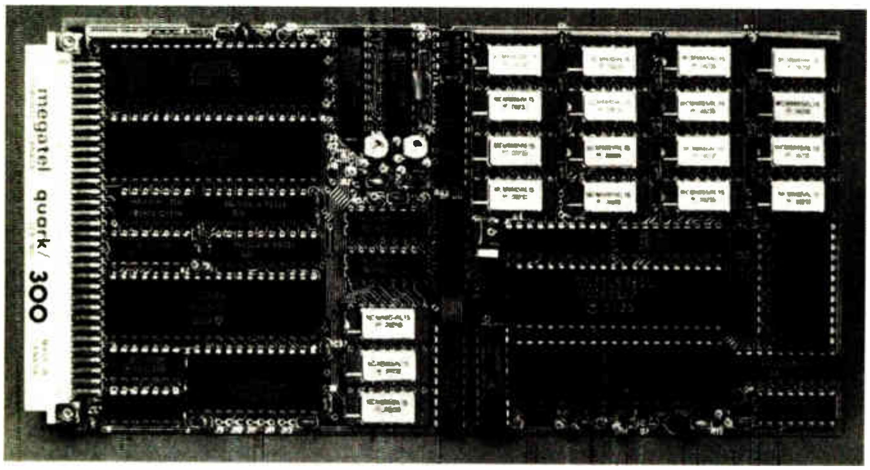


mapped graphics capability.

A comprehensive software package is available with a basic I/O system (BIOS) for CP/M, disk and terminal drivers, utilities, and a menu-driven installation program for quick configuration to the user's disk-drive and I/O requirements. Well-documented source code of the BIOS comes with the package.

In addition to CP/M 2.2, CP/M Plus version 3 is available for the Quark/300, as are the MP/M II multiuser multitasking operating system and the DR Soft/Net networking system for use with CP/M and MP/M. All of the operating systems work in a memory-banked environment, making full use of the 128- or 256-K bytes of main memory on the board.

The Quark/300 joins a line that is built around a basic product, the Quark/100. Each of the other computer cards adds some special capability: the Quark/150 offers color video, the Quark/200 has Omninet local-network circuitry, and the Quark/300 adds hard-disk control.

Disks. Many of the functions required for the hard-disk interface are provided by the floppy-disk control circuitry, which uses a Western Digital 1793 controller chip. Both floppy- and hard-disk drives can be connected simultaneously, within the limits of the three side-selection lines. For example, one four-platter Winchester and a single double-sided floppy can be accommodated, or a two-platter Winchester and two double-sided floppies. An eight-platter Winchester can be controlled, but it leaves no side-selection lines open for use with floppy-disk drives. The floppy drives can be 5¼- or 8-in. units with a wide variety of formats.

A 12-K-byte track buffer aids Winchester operations. Automatic error-detection and retry is provided, and error-correction facilities can be added. Seek operations can be either buffered or not.

The Quark/300's video-display interface runs in an alphanumeric mode supporting 80 columns by 24 to 28 rows and a software-programmable character set. In graphics mode, it offers a resolution of 640 by 240 picture elements. A composite-video monitor can be connected as well as a direct-drive (TTL) monitor; alternatively, a standard terminal can be connected to the full-duplex RS-232-C port and a terminal driver from the software package utilized.

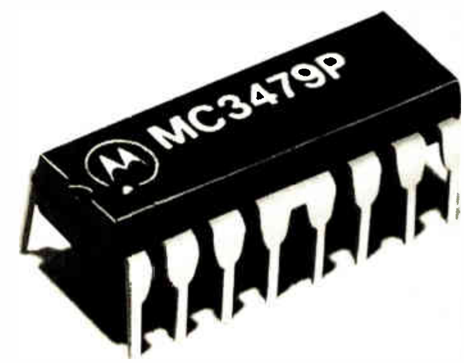
The small board also carries a second RS-232-C port for simplex operation only, a parallel printer port, and 22 general-purpose I/O lines for keyboard input or other applications. Access to the central-processing unit's address, data, and control lines is also available on the board's single 96-pin connector. This connector mates with another card, the Quark transition board, which provides space for the user's connections to the system.

A development package consisting of a Quark/300, installation software, device drivers, utilities, CP/M, BIOS, a connector, a transition board, and manuals costs $1,095 for CP/M 2.2 and 128-K bytes of random-access memory. For CP/M Plus and 256-K bytes, the price is $1,495. Prices for the basic Quark/300 range from $495 to $895, depending on quantity and the amount of RAM ordered.

Megatel Computer Corp., 150 Turbine Dr., Weston, Ontario M9L 2S2, Canada. Phone (416) 745-7214 [Circle 341]

Stepper-motor driver chip provides 350 mA, performs logic decoding and sequencing

Zeroing in on an application niche in high-volume disk drives, Motorola's Bipolar Linear division is unveiling an integrated circuit for driving a two-phase stepper-positioning motor. Outputs of the MC3479P can provide up to 350 mA to each of two coils of a two-phase motor. The chip consists of four input sections, one for logic decoding and sequencing, two drive stages for the coils, and an output to indicate the phase-A drive state.



While stepper-motor driving initially was accomplished with circuitry incorporating a number of components, largely TTL with driver arrays, user demands for lower cost and higher re-

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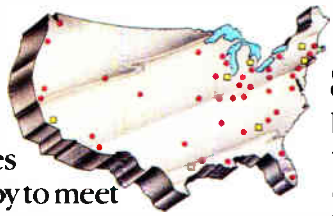

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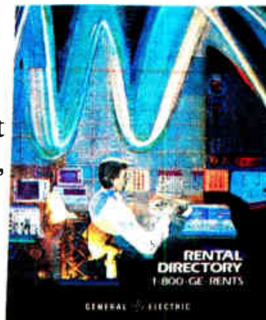

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liability have prompted the semiconductor industry to move to one-chip solutions. Motorola's entry is intended to offer the most possible self-contained functions, according to the company. Moreover, the 16-pin package lends itself to automated handling procedures increasingly used by disk-drive manufacturers. The driver also can be employed in the fast-developing robotics field.

Half step. Among the important functions of the IC is selectable clockwise or counter-clockwise motor operation, which allows reversing the rotation. Also, it has a feature that causes the motor to rotate either one full step or one half step, depending on the logic input, the company says. In the half-step mode, precise output-impedance control permits high-speed stepping directly into a track of a disk drive; the alternative is gradual slowdown through employing a special algorithm for this purpose, according to Motorola.

The driver chip has a single power-supply pin for both the logic circuit and motor-coil current, in a range from 7.2 to 16.5 V. Four ground pins for the logic and motor-coil current have a physical configuration that aids in dissipating heat from within the supply package.

Clamp diodes are provided in order to protect the outputs from voltage spikes that may occur when motor coils are switched on and off. Operable in ambient temperatures of 0° to +70°C, the MC3479P driver circuit accepts input voltages that range from 0 to +5 V and draws maximum of 8 mA of current; input hysteresis is 400 mV minimum.

It is available from stock, priced at less than $2 in original-equipment-manufacturer quantities.

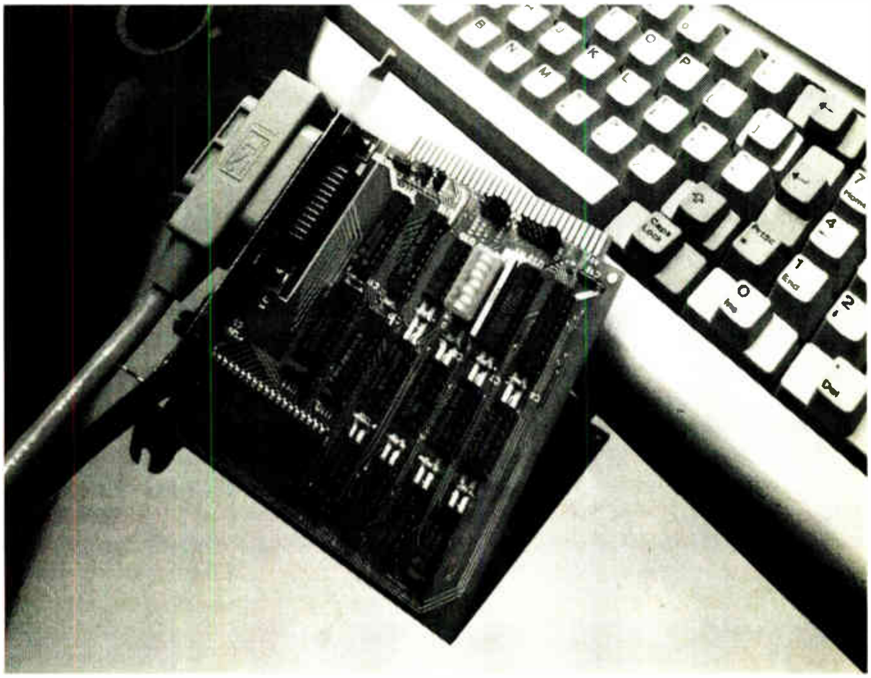
Motorola, Inc., Semiconductor Sector, Bipolar Linear Division, Box 20912, Phoenix, Ariz. 85036. Phone (602) 897-3826 [Circle 340]

Card controls instruments for IBM PC equipped with data-acquisition system

Instrument control as well as data acquisition will soon be at the fingertips of users of the International Business Machines Personal Computer, thanks to a new instrument-control card. The Plus500 links the IEEE-488 bus with an IBM PC or XT equipped with one of the Keithley DAS series 500 data-acquisition and -control systems.

Integrated with the Plus500, which fits in any of the slots in the PC or slots J1–J7 in the XT, is an easy-to-use software package. "The integration of our software means an engineer can use an IBM PC to simultaneously control his IEEE-488 instruments and gather data from multiple analog sources," explains Steven Wilson, Keithley DAS's managing partner. The company is a joint venture of Keithley Instruments Inc., of Cleveland, Ohio, and Data Acquisition Systems Inc., of Boston, Mass.

Up to 15 instruments can be managed from a single keyboard with the Plus500, which extends the IEEE-488 protocol to include such advanced features as automatic serial polling of multiple instruments, programmed triggering from up to 12 events, and adjustable timeouts to avoid hangups.



The board can transfer data at rates up to 300-K bytes/s using direct-memory-access transfers; however, as in any system, the actual data rate and overall throughput depends on the transfer speed of the slowest device in the transfer and the number of bytes transferred in one operation. The software supports programmed input/output data transfers as well as DMA transfers.

Extended software. An extension of the Basic programming language, the Plus500 software shares the structure and operating environment of Soft500, Keithley DAS's time-critical multitasking software for the DAS series 500, and can be used concurrently with it. Also, the Plus500 software can translate an engineer's Basic program into IEEE-488 commands. "Unlike the IEEE-488 protocol itself, Plus500 software is very easy to program," Wilson points out.

The Plus500, which sells for $595 with the software, requires a +5-V supply from the IBM PC I/O channel. Its current load is typically 0.5 A. It will be available starting in June.

Keithley DAS, 349 Congress St., Boston, Mass. 02210. Phone (617) 423-7780 [Circle 343]

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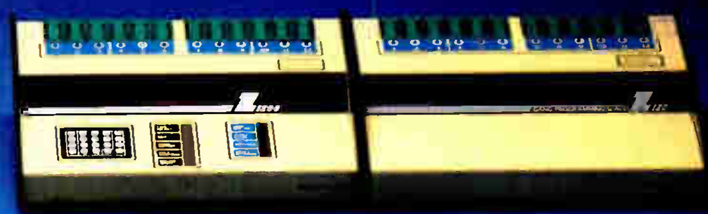

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Circle 177 on reader service card

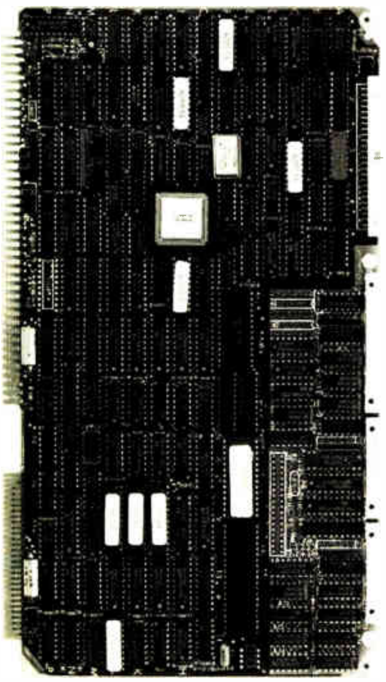
Microcomputers & systems

Disk controller also handles QIC-02 drives

A line of multifunction peripheral storage controllers that support Multibus-based systems features a gate array that provides direct-memory-access transfers at 2.5 megabytes/s and another that provides the error-checking and correction logic necessary to implement a 32-bit ECC algorithm that will correct up to 11 bits.

The first two products in the line, Xylogics' 421 and 422, permit the simultaneous operation of a QIC-02 tape drive plus a choice of either ST506/412 or Enhanced Small Disk Interface (ESDI) disk drives.

Both controllers are based on a modular design that provides all Multibus- and tape-control functions on a common motherboard and implements the disk-drive interface circuitry for each drive on a flush-mounted daughterboard. Therefore, the dual controller requires only one card slot. Drives for Unix and RMX-86 operating systems, as well as diagnostics written in C, will be available when production begins.



The 421 and 422 peripheral controllers are priced at $995 for 250-piece quantities. Deliveries are scheduled to begin in May.

Xylogics Inc., 144 Middlesex Tpke., Burlington, Mass. 01803. Phone (617) 272-8140 [Circle reader service number 361]

Color-display adapter's text quality is better than IBM's

BoB (for best of both), a single-board color-display adapter, not only provides users of International Business Machines Corp.'s Personal Computers with all of the color graphics features of IBM's color-display adapter, but also improves upon the alphanumeric text quality of IBM's monochrome-display adapter. Compatible with the PC graphics software, it supports either a standard-color mode with 16 colors or a black-and-white mode with 16 levels of gray (compared with IBM's two shades of gray) when connected to a monochrome monitor.

The board is designed to interface with advanced high-resolution monitors, such as 14-in. models. It makes possible a system with a color monitor linked to a single-chassis-slot display-adapter board capable of supporting color graphics and text-oriented applications.

BoB offers standard-intensity red-green-blue as well as composite-video monochrome outputs. It displays an 8-by-12-dot character in a 10-by-16-dot grid, producing character resolution better than the IBM monochrome display, the company says.

In addition, the board supports a 24.83-kHz horizontal rate to provide 400 vertical-scan lines, a resolution significantly higher than that of the IBM color-display adapter, which supports 200 vertical scan lines operating with a 15.75 kHz horizontal rate.

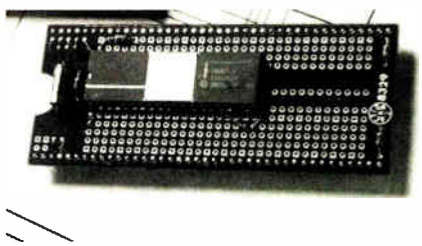
Available now, the BoB display adapter is priced at $425 per unit.

Personal Systems Technology Inc., 15801 Rockfield Blvd., Suite A, Irvine, Calif. 92714. Phone (714) 660-1010 [Circle 362]

Accelerator speeds simulation by up to a factor of 500

Designed for use with its manufacturer's Scaldsystem computer-aided-engineering work stations, the Realfast simulation accelerator boosts simulation speeds by up to a factor of 500, the company says. At the same time, it maintains the Scaldsystem's user-interface and interactive-simulation capabilities.

According to the company, the simulator can handle 500,000 evaluations per second. It consists of two high-speed bipolar simulation engines. One, which performs scheduling and unscheduling, looks ahead to see if a gate must be evaluated on any particular pass through the logic. The second, a dedicated-simulation processor, performs evaluations of device primitives needing them. Realfast is implemented with an expandable board set housed in either a desktop or small floor-standing cabinet and connected to a Scaldsystem S-32 computer by ribbon cable.



Priced at $29,500 in its basic configuration, the simulator will be available in late 1984.

Valid Logic Systems Inc., 1395 Charleston Rd., Mountain View, Calif. 94043. Phone (415) 940-4000 [Circle 363]

Programmable array processor runs at 20 million operations/s

The ZIP 3200 series of software-programmable array processors for microcomputer-based systems is designed for image- and signal-processing as well as scientific applications, among them medical imaging, seismic processing, vision, and comput-

Modulation measurement reaches new peaks in performance

A MODULATION METER THAT'S A COUNTER, R.F. POWER METER AND AUDIO ANALYZER

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Circle 179 on reader service card

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N2305A

er-aided engineering.

The series is based on dual-processor data-flow architectures, and its first two products differ only in their arithmetic pipelines. The 3216, primarily for image and signal processing, does 16-bit arithmetic at 20 million computations/s and 32-bit arithmetic at 5 million computations/s.

The 3232 performs 32-bit arithmetic at 10 million computations/s, and is designed for graphic and scientific uses. Both processors operate concurrently with a 10-MIP control processor and an internal 40 megabyte/s bus connecting system components.

In their basic form, both products consist of a three-board Multibus card set. Chassis versions are offered for Q-bus and VMEbus systems. The memory is 128-K bytes; expansion is available to 16 megabytes.

The price of the 3216, available 30 days after receipt of order, is $8,000. The 3232, priced at $10,000 will come out in late 1984.

Mercury Computer Systems Inc., 600 Suffolk St., Lowell, Mass., 01854. Phone (617) 458-3100 [Circle 369]

Multibus computer card has 2 megabytes of RAM

Built on a single Multibus card, the GVC-16 demand-paged virtual-memory microcomputer combines the NS16000 microprocessor chip set, up to 2 megabytes of random-access memory, a Winchester-disk-drive interface, and the peripherals needed for a high-performance multiuser system. The large on-board memory allows a 10-MHz central processing unit to run without wait states, making the GVC-16 well suited for multiprocessor systems.

Four universal asynchronous receiver transmitters, a disk interface, time-of-day clock, and other peripherals allow the systems designer to work with a fully equipped single-board system, while the Multibus interface and dual-port memory provide an easy route to expansion.

The GVC-16 standard-board configuration includes 512-K bytes of memory and the interrupt control unit. The GVC-16 is priced at $3,295 with 512-K bytes of random-access memory. For orders of three boards or less, it is available in one to two weeks. For larger quantities, delivery takes five weeks.

GVC Microcomputers Inc., 222 Third St., Cambridge, Mass. 02142. Phone (617) 576-1804 [Circle 366]

Chassis, seven VME modules build Unix-based systems

The initial products in a line of VMEbus compatible modules for building Unix-based systems include the DVME 909 rack-mountable system chassis, seven VMEbus cards, and a development system based on the AT&T Bell Laboratories Unix operating system. The line uses the 233-by-220-mm Eurocard format, which allows fewer cards per system.

The seven cards consist of two 68000-based processor cards, a 512-K-byte dual-port memory card with a 10-MHz video-refresh port, a universal byte-wide memory card, a serial and parallel input/output card, a Z80A-based intelligent disk-drive controller, a bit-mapped color graphics card with 256-K bytes of memory, and a graphics controller.

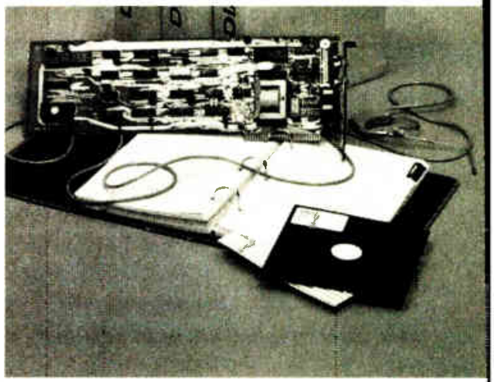
Available now, the DVME 909 is priced at $5,000 and the cards range from $1,200 to $3,000.

DY-4 Systems Inc., 888 Lady Ellen Place, Ottawa, Ontario, Canada K1Z 5M1. Phone (613) 728-3711 [Circle 367]

Voice I/O products offer real-time storage, retrieval

The Dialog 1/2/3 series of voice input/output products designed for the International Business Machines Corp.'s Personal Computer provides high-quality, real-time voice storage as well as retrieval for business applications.

A Dialog board requires one expansion slot and runs under PC-DOS. The series is intended for use in such office-automation applications as voice annotation of text for word



processsing and remote messaging.

Priced at $295, Dialog/1 provides basic voice capability. Dialog/2, for $495, adds a phone interface, autodial and auto-answer firmware, and tone decoding. Dialog/3, priced at $595, also includes a 300-baud modem and digital-transmission firmware. Delivery takes four weeks.

Dialogic Corp., 164 McKinley Ave., East Hanover, N. J. 07936. Phone (201) 386-0202 [Circle 368]

Single-board computers have high-throughput capacity

Based on the 80188 processor, the ZT 8814/8815 single-board computers offer systems designers high-throughput capacity and such features as direct memory access and interrupt controllers.

The ZT 8814 and 8815 computer boards, 5- and 8-MHz units, respectively, provide five byte-wide memory sockets. One socket accepts the company's debug monitor, which can be replaced later with a user's programmable read-only memory of up to 32-K bytes. The four other sockets on the 8814 and 8815 accept random-access memories and PROMs of up to 32-K and 64-K, respectively.

The 80188 comes with two DMA channels, an interrupt controller, timers, clock, and peripheral or memory chip-selection logic.

Deliveries of the ZT 8814 and 8815, which are priced at $650 and $695, respectively, will begin in May.

Ziatech Corp., 3433 Roberto Ct., San Luis Obispo, Calif. 93401. Phone (805) 541-0488 [Circle 365]

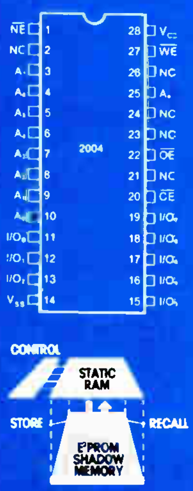
Xicor NOVRAMs.
The Byte-Wide Innovation.

Nonvolatile static RAMs. NOVRAMs.* At Xicor, we invented them. We were the first to introduce them. The first to perfect them. And the first to deliver them. Over the past four years, our family of nonvolatile memory products has evolved to meet the demands of a changing market.

And with our new byte-wide series, we've done it again.

For those familiar with the performance advantages of Xicor NOVRAMs, the byte-wide series provides a versatile new option for improving system performance. One that is simple to implement. Because it's organized in the universal microprocessor format: a byte. With the added advantage of hardware and software control of all nonvolatile operations.

For new users, the byte-wide series is the perfect complement for 8 and 16-bit micro-based design applications. Their nonvolatility allows them to remember critical information indefinitely—without battery backup. Information like pre-power-loss operating conditions. Or system configuration parameters. And because of their convenient dual-line control, they eliminate bus contention.



Byte-wide NOVRAMs come in three configurations: X2001 (128x8), X2002 (256x8) and X2004 (512x8). The entire series is packaged in JEDEC-approved pinouts for byte-wide memories and is available in a variety of temperature ranges.

If you'd like information on pricing, delivery and performance about these or other NOVRAMs, write us at 851 Buckeye Court, Milpitas, CA 95035 (408) 946-6920.

*NOVRAM is Xicor's nonvolatile static RAM device.

Xicor

Circle 182 on reader service card

Instruments

Six-pen plotter does waveform recording

The HP 7090A measurement plotting instrument combines the functions of waveform and X-Y recorders, digital plotters, and data-acquisition systems into one laboratory-graphics device. The unit is designed to meet the test, measurement, and presentation needs of engineering and scientific professionals.

As a low-frequency waveform recorder, the HP 7090A provides 1 kiloword by 12 bits of buffer and a 30-kilosamples/s analog-to-digital converter per channel. Sine response is 3 kHz, and multiple triggering modes with pre- and post-trigger viewing are provided to examine transient phenomena.

As an analog X-Y recorder, the unit offers three high-common-mode rejection rate inputs for X-Y or Y-T recording, 41,000 calibrated sensitivity ranges and zero offsets, 2-g constant acceleration, and 127-cm/s slewing speed.

When connected to a controller or a smart instrument, the six-pen HP 7090A can be used as a plotter. It includes 42 of the company's graphics-language instructions and draws at 75 cm/s. As a component in a data-acquisition system, the HP 7090A can acquire and send data to a controller through an IEEE-488 bus at a streaming rate of up to 250 samples/s. The system is priced at $4,400 and can be delivered six weeks after receipt of order.

Hewlett Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [Circle reader service number 351]

Light-pulse generator has built-in power meter

The 6020 calibrated light-pulse generator and modulator has a built-in power meter that operates at up to 150 MHz with 500-ps rise times and generates 500-ps impulses.

The 6020's operating features make it possible for the user to vary pulse rates, delays, and widths; generate single or double pulses; externally trigger or modulate the light output; and control baseline level and peak power. The power meter measures and displays the peak and baseline levels, with up to three-digit

resolution and durations that are as narrow as 5 ns.

Serving as a basic electro-optics tool, the 6020 is best suited for detector response characterization, local-network testing, fiber-optics data communications, and fiber-dispersion testing.

Available 60 days from receipt of order, the 6020 is priced at $5,950.

Berkeley Nucleonics Corp., 1198 10th St., Berkeley, Calif. 94710. Phone (415) 527-1121 [Circle 353]

Software lets analysis system test and verify VLSI circuits

A software package transforms Tektronix's DAS 9100 digital analysis system into a VLSI verification and test unit that interfaces with other VAX-based engineering tools, such as logic simulators. After using schematic entry, simulation, and physical layout tools to design a very large-scale integrated circuit, the engineer can use the same system to verify the chip's operation when it returns from fabrication. The actual hardware test functions are performed by modular instrument cards within the DAS mainframe, which is interfaced with a VAX computer running under AT&T Bell Laboratories' Unix operating system.

The DAS 9100/VAX test system allows streamlined test operations through interaction with other VAX-based tools.

For instance, the test-pattern vectors used by a logic simulation program can be downloaded to the DAS 9100 and used as a simulation program during testing.

Available immediately, the 91DVV software package sells for $1,000. A typical DAS 9100 configuration for this application is priced at about $40,000.

Tektronix Inc., P. O. Box 1700, Beaverton, Ore. 97077. Phone (800) 547-1512 [Circle 359]

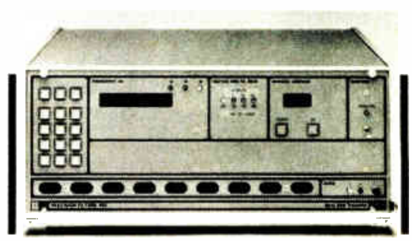
Frequency translator enhances spectrum-analysis equipment

A multichannel programmable frequency-band translator called the Precision 1776 serves as a super-bandpass filter or as a frequency-band translator that can extend the capacity of old equipment used in spectrum analysis.

The system obtains 80-dB bandwidth-octave skirts by translating the frequency band to 0 and passing it through a low-pass filter. Acting as a bandpass filter, the instrument can translate back to the starting frequency band or any other part of the spectrum. For bandpass filtering, a configuration of up to eight programmable phase-matched channels is available.

For analog zooming, a 16-channel programmable configuration extends the capability of existing equipment. The instrument zooms in to extend the frequency range while making possible much finer resolution.

For beam forming and modal analysis, the Precision 1776 system gets rid of unwanted noise, and it also



lowers the sampling frequency. The price of the frequency-band translator system starts at $12,000; delivery takes up to 120 days after receipt of order.

Precision Filters Inc., Dept. 1776P, 240 Cherry St., Ithaca, N. Y. 14850 (607) 277-3550 [Circle 355]

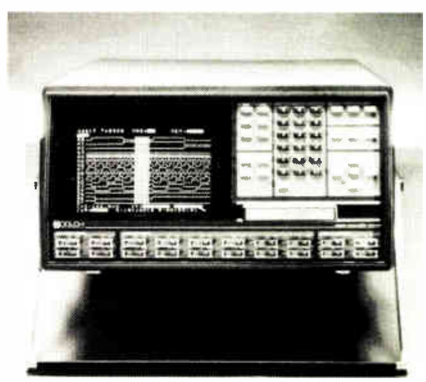
Logic system is enhanced with software routines

The 64300S logic-analysis system, an enhanced version of the company's 64300 series, is fully modular in 16-channel increments and has 16 asynchronous channels operating at 300-MHz for timing analysis and 48 synchronous/asynchronous channels operating at 25/50-MHz for state/timing analyses.

Its software enhancements are labeling, area-trace, and reference-timing functions. With labeling, users can add names up to seven characters long to all 64 channels on the timing display. Area trace enables the 64300S to limit the information it records to user-specified blocks of data. Up to 10 areas can be defined across 16 data bits.

With reference timing, a timing diagram can be created for data stored either in the analyzer's data memory or in a DataPak module. The 64300S is priced from $11,350 to $18,150 depending on options. It can be delivered in four weeks.

Dolch Logic Instruments Inc., 3052 Orchard Drive, San Jose, Calif. 95134. Phone (408) 945-1881 [Circle 352]



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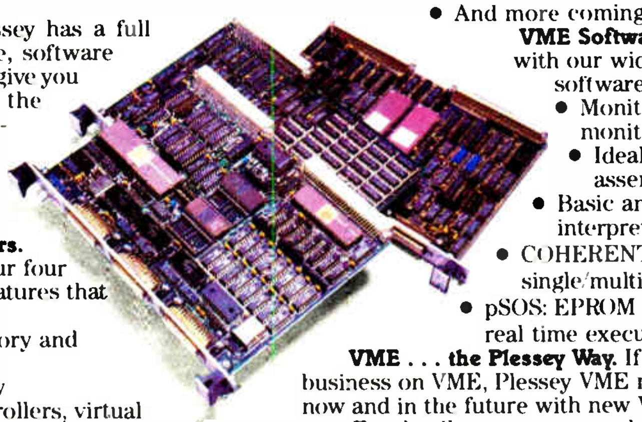
Introducing Plessey VME. Plessey has a full range of VME board level hardware, software and technical support services. We'll give you the languages, operating systems, the drivers, complete technical assistance and, of course, that famed Plessey guarantee with worldwide backup. All to support our superior VMEbus products including . . .



VMEbus Single Board Computers. Build your systems around any of our four new single board computers with features that include up to:

- 10 MHz 68000, 512 Kbytes of memory and 128 Kbytes EPROM
- 512 Kbytes of dual ported memory
- Memory management, DMA controllers, virtual memory processors
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- Floppy disk controller, real time clock with battery backup
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VMEbus Memories. Enhance your system with add-in memories including:

- Parity boards up to 4 Mbytes capacity with 270 ns access time
- ECC boards up to 3 Mbytes capacity with 300 ns access time.
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- And up to 128 Kbytes high speed static RAM boards with 140 ns access time and on-board battery backup.

VMEbus Controllers, Graphics and I/O Boards. Plessey VME also includes:

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- 6-channel serial I/O boards
- And more coming.

VME Software. Support your system with our wide range of firmware and software products:

- Monitor: EPROM resident monitor/debugger
- Ideal: EPROM resident assembler/editor
- Basic and Forth language compiler/interpreters
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Circle 187 on reader service card

Software

Link lets IBM PC access Ramis II data base

A mainframe-to-microcomputer link connects the Ramis II mainframe data-base management system with a number of personal computer software packages, thus facilitating bidirectional data transfer between mainframes and microcomputers.

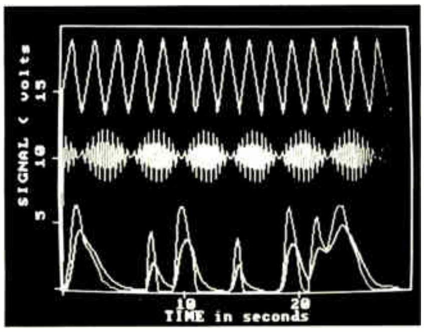
With RAMlink, users can upload and download data between mainframes and IBM's Personal Computer and PC XT. Through a modem requiring no additional protocol-conversion hardware, RAMlink gives PCs and dumb terminals full-screen 3270-type terminal access to all Ramis II's mainframe capabilities.

Available now for immediate delivery, the mainframe portion of RAMlink costs from \$4,500 to \$9,000, depending on the performance level of the central processing unit. RAMlink floppy disks for the PC or XT are priced at \$185 each.

Mathematica Products Group Inc., P. O. Box 2392, Princeton, N. J. 08540. Phone (800) 257-5171 [Circle 371]

Software is fashioned to replace scientists' notebooks

A software package called the Real-Time Lab Notebook has been developed to replace old-fashioned laboratory notebooks by integrating such functions as data acquisition, real-time charting, data filing, curve fitting of theory to data, and the generation of technical reports and statistics. The software runs on IBM Personal Computers and works with a variety of data-acquisition and input/output control boards, as well as with RS-232-C interfaces.



With a delivery time of 30 days from receipt of order, the product sells for \$495.

Laboratory Technologies Corp., 328 Broadway, Cambridge, Mass. 02139. Phone (617) 497-1010 [Circle 372]

Software transfers bulk data from PCs to mainframes fast

A software component that manages the movement of data among systems is designed for high-speed bulk information transfer. Its capabilities include remote job entry, which gives users direct access to the central-processing power and application resources of all major mainframes and networks.

Designed for use with IBM Personal Computers, BARR/HASP+ can move periodic transaction batches, programs, messages, and object or executable files. It has an unattended mode of operation, so the PC can be told by a remote computer to pick up or deliver information. These features make it possible to control and maintain programs centrally and also facilitate periodic processing of applications.

Available within 30 days, the BARR/HASP+, including a synchronous interface, costs \$890.

Datanex Inc., P. O. Box 1728, Eugene, Ore. 97440. Phone (503) 687-2520 [Circle 373]

Software lets engineers create 10-by-16-in. pc boards

A printed-circuit-board artwork editor for electrical engineers facilitates interactive control over the placement-and-routing process. The program runs on the IBM Personal Computer without special hardware.

Designers can make use of the SMARTWORK program to produce

single- or double-sided pc boards as large as 10 by 16 in. The layout can be displayed in color or in black and white, and plots twice the normal size can be made on a dot-matrix printer.

Camera-ready artwork can be produced on a pen-and-ink plotter. The program costs \$895 and is available immediately.

Wintek Corp., 1801 South St., Lafayette, Ind. 47904. Phone (317) 742-8428 [Circle 376]

CAD software lets users design circuits with Boolean algebra

A computer-aided-engineering software package compiles logic designs for programmable logic arrays and programmable read-only memories in a common syntax and also helps designers create circuits using any combination of Boolean equations, truth tables, and state diagrams.

Called Abel, the software makes design more flexible by letting designers choose both the appropriate

part for a circuit and the natural form to express the intended circuit function.

At first, three versions of Abel will be available: for Bell Laboratories' Unix operating system, MS-DOS, and VMS, respectively. Abel's features include free-format structured syntax; direct use of Boolean, relational, and arithmetic operators; and automatic DeMorgan conversion.

In the U. S., the version for MS-DOS systems sells for $895; its counterparts for VMS and Unix cost $2,495 each. Delivery is from stock.

Data I/O Customer Service, 10525 Willows Rd. N. E., P. O. Box 97046, Redmond, Wash. 98073-9746. Phone (800) 426-1045 [Circle 374]

Programming tools are made for use with 8086/88

Four programming tools—a full-screen text editor, a dynamic debugger, an object-module linkage editor, and a library manager—are available for use with 8086/88-based systems running under PC-DOS, MS-DOS, or CP/M-86.

The features of the P-MATE86 single-keystroke editor include automatic disk buffering, ten auxiliary buffers, and horizontal scrolling. Those of the P-FIX86 symbolic debugger include windowed full-screen display, inline assembler, and test evaluation at breakpoints.

The P-LINK86 linkage editor handles the output of compilers and assemblers. To reduce memory requirements, overlays can be specified with no modification to the application program, and they can be combined into one or more disk files. The P-LIB86 object-library manager can build libraries from scratch, delete modules from existing libraries, merge libraries, and produce cross-reference listings.

P-MATE86 costs $225, P-LINK86 $395, P-LIB86 $125, and P-FIX86 $245. All the tools are available immediately.

Phoenix Software Associates Ltd., 1420 Providence Hwy., Suite 260, Norwood, Mass. 02062. Phone (617) 769-7020 [Circle 377]

Monolithic vs Hybrid vs Modules

All contemporary manufacturing technologies are important at Burr-Brown, but only as a means to an end. They are not the end. Rather, the objective or end, here, is the best possible solution to a customer's problem. As a result, we mix and match technologies—monolithic integrated circuits, thin-film networks, thick-film substrates—to arrive at the optimum product for the customer's application...one that provides the right cost/performance ratio. If necessary, in fact, we'll buy the best available technology, and merge it with our own, to produce the high-performance, precision products that have built our reputation as a performance-driven company.

Technological Evolution

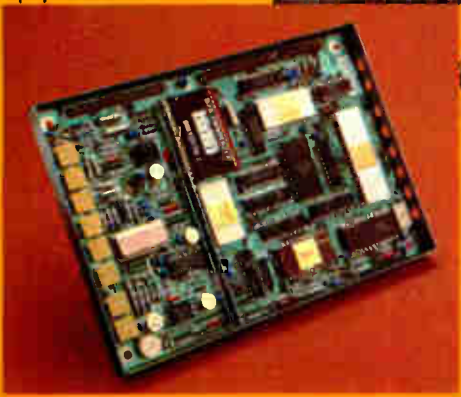
To insure upward mobility for our customers' products, without costly redesign, we frequently evolve our products from one technology to another, while maintaining pin compatibility. For example, in 1974, we introduced DAC45, the industry's first 16-bit D/A converter. It was composed of discrete devices in modular form. The next year saw DAC70, an improved version, in hybrid form. Still later, DAC71 integrated more functionality while maintaining the hybrid form.

Recently, we introduced DAC700, the first totally monolithic 16-bit D/A converter. Tomorrow...who knows? That monolithic chip may well be used as part of a hybrid to provide even greater functionality.

That's another reason why we don't restrict ourselves to a single technology. Still another is performance. We'll use whichever one or whichever combination yields the best performance for the particular application. Monolithic vs Hybrid vs Modules...

The Debate Ends Here

For more information about how Burr-Brown is *Putting Technology To Work For You*, circle the Reader Service Number or write: Burr-Brown, Corporate Capabilities, 6730 S. Tucson Blvd., Tucson, AZ 85706.



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Circle 191 on reader service card

How To Guarantee Your Product

The Cost-Effective Ando Way

ANDO
ANDO ELECTRIC CO.,LTD.
Tokyo, Japan

Ando's new VLSI Test System—up to 256 pins, up to 40MHz

With tests accounting for a large and growing share of IC production costs, it's no wonder managers are ever on the lookout for cost-cutting ways. And cost-effective throughput is what you get with an Ando IC tester.

Take the new Ando DIC-8035B VLSI Test System. It can handle several devices in parallel, running as many as 256 pins at up to a full 40MHz.

The compactly designed and built DIC-8035B is flexible—its hierarchal/distributed system concept enables you to expand your Ando test system as your own requirements grow.

Also, thanks in part to Ando's easy-to-use programming language called SUMMIT, it's easy to provide full functional testing as well as test data analysis for an astonishing variety of VLSI devices, including those still on the planning board.

Like all Ando IC testers the new DIC-8035B has a unique connection that completely eliminates error-causing cables between tester and handler or prober—even if you're using an auto-handler or wafer prober.

What's more, you can hook up the DIC-8035B with a telecommunications network. An important bonus in this day and age of global industrialization.

To find out more about how Ando IC testers can help you lower overhead costs without sacrificing product quality, call your Ando representative.

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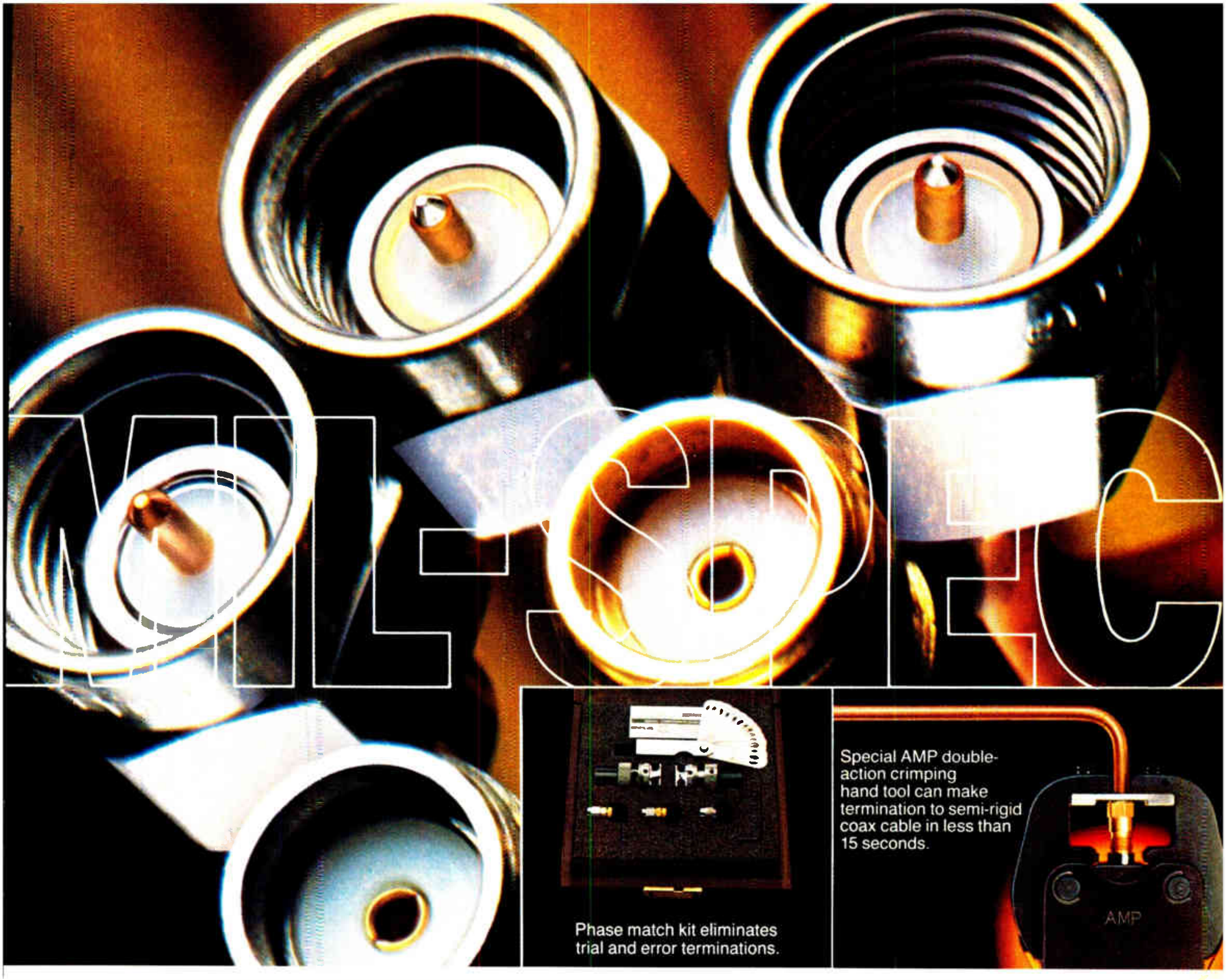


Special AMP double-action crimping hand tool can make termination to semi-rigid coax cable in less than 15 seconds.

Phase match kit eliminates trial and error terminations.

MIL-C-39012, Category F.

We've taken the heat off SMA coax connections.

And you.

You're looking for an SMA semi-rigid coax connector to meet MIL-Spec. But you're not looking forward to the heat problems created by soldering. Or the time taken by X-ray testing.

See AMP—and get the solderless MIL-C-39012 SMA coax connector. It's fast. It's reliable. It comes completely pre-assembled. It's intermateable with existing designs, and qualified to Category F.

And it's tough. Unlike soldered connections, the AMP SMA can take the cold and heat, the vibrations, the hostile environment of deep space.

Its MIL-C-22520 tooling and Phase Match Kit (makes a perfect connection everytime to save time) together give you the easiest, most secure SMA installation in the industry. And our retractable coupling nut version allows visual alignment for perfect mating.

Our SMA is just one more connector to join the ranks of AMP products for avionics, microwave, and military applications.

We deliver the help you need, too, in design, engineering, all the way through project development. We'll do our best to take the heat off you with the product quality you expect, and the personal attention you should have.

CIRCLE NUMBER 125

For more information, call the AMP MIL-C-39012 Desk at (717) 780-4400.
AMP Incorporated, Harrisburg, PA 17105.

AMP means productivity.

Semiconductors

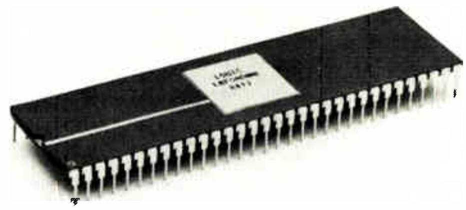
C-MOS circuits multiply fast at low cost

A line of 8-by-8-, 12-by-12-, and 16-by-16-bit complementary-MOS multipliers that are compatible with TRW's MPY and Advanced Micro Devices' Am29500 bipolar chips are just as fast yet consume less power. The company claims their prices are lower than the bipolar parts.

The 8-by-8-bit multipliers, with 65-ns typical multiply times and 60-mW typical power dissipation, sell for $56 each in plastic packages in lots of 100. The LMU08 is a parallel 2's complement multiplier and the LMU8U is a parallel unsigned-magnitude version. The two 12-by-12-bit multipliers, the LMU12 and LMU13, multiply in no more than 80 ns and consume about 100 mW of power. Housed in plastic, the parts sell for $88 each in lots over 100.

With a 100-ns multiply time, the 16-by-16-bit multipliers, the LMU16 and LMU17, consume 125 mW and sell for $120 in plastic packages for orders of 100 pieces or more. All the multipliers, which are available now, also come in ceramic packages.

In addition to the line of multipliers, the firm has an 8-word-by-8-bit multiport-register file with a 25-ns access time and a 60-mW power consumption at 10 MHz. For implementing dynamically reprogrammable architectures, the LRF08 features five independently addressable ports: two dedicated inputs, two three-state outputs, and one bidirectional port. In lots of 100, the ceramic version of the multiport register sells for $138.



Logic Devices Inc., 628 E. Evelyn Ave., Sunnyvale, Calif. 94086. Phone (408) 720-8630 [Circle reader service number 411]

256-K ROM offers choice of MK38000 or Jedec pinouts

Suited for memory-intensive electronic systems that use a large amount of software in silicon, the RO9256 256-K read-only memory offers mask-programmable options that give the user a choice of Mostek MK38000 or Joint Electron Device Engineering Council standard pinouts. The 32-K-by-8-bit memory has a standard maximum access time of 250 ns, fully static operation, three-state outputs, and +5-V-only operation.

Using late-mask programmability, the company can program customers' ROMs late in the manufacturing cycle. In lots of 10,000 pieces, the RO9256 sells for $10.50 each. Production quantities should be available this month.

General Instrument Corp., Microelectronics Division, 600 W. John St., Hicksville, N. Y. 11802 [Circle 415]

64-K RAMs peak at 200 mW, stand by on 16.5 mW

Designed for 100- and 120-ns read-access time, the F4164-10 and F4164-12 64-K dynamic random-access memories are fabricated in a double-polysilicon n-channel MOS Isoplanar-H process. Operating from a single 5-V supply, the 64-K-by-1-bit chips require no more than 200 mW when active and just 16.5 mW when standing by.

The memories use multiplexed addressing to permit use of standard 16-pin dual in-line packages. Their operational modes include random read or write, read-write, read-modify-write, and page cycling. In lots of 100, prices are listed at $13 for the 100-ns F4164-10 and $11 for the 120-ns F4164-12 in plastic packages. Samples are available now.

Fairchild Microprocessor/MOS Division, 464 Ellis St., Mountain View, Calif. 94042. Phone (415) 962-3885 [Circle 412]

Junction-isolation technique cuts access times of ROMs

Using advanced junction isolation, a pair of small read-only memories operate 50% faster than the firm's earlier designs. The 82A126A, configured as 256 by 4 bits, carries two chip-enable inputs, one for active-high inputs and one for active-low inputs. The commercial grade has a 27-ns access time and the military version a 35-ns speed.

Organized as 32 eight-bit words, the 82S23A has one active-low chip-enable input. The maximum access time of the commercial-grade memory is 25 ns; the military model's is 35 ns. Prices range from $1.25 to $4.60.

Signetics Corp., 811 E. Arques Ave., P. O. Box 409, Sunnyvale, Calif. 94086. Phone (408) 739-7700 [Circle 413]

2-K RAM made nonvolatile by duplicate 2-K of EE-PROM

The byte-wide NCR 52002 nonvolatile random-access memory, which operates from a single 5-V supply, consists of a 2-K RAM with a duplicate area of electrically erasable programmable read-only memory. The shadow RAM, as it is called, has a typical access time of under 300 ns.

It is fabricated with an n-channel silicon nitride oxide semiconductor process. The number of possible store cycles is guaranteed to be at least 10^4. In lots of 100, the RAM sells for $18.70 each. Samples are available now.

NCR Microelectronics Division, 8181 Byers Rd., Miamisburg, Ohio 45342. Phone (800) 543-5618 or in Ohio (513) 866-7217 [Circle 414]

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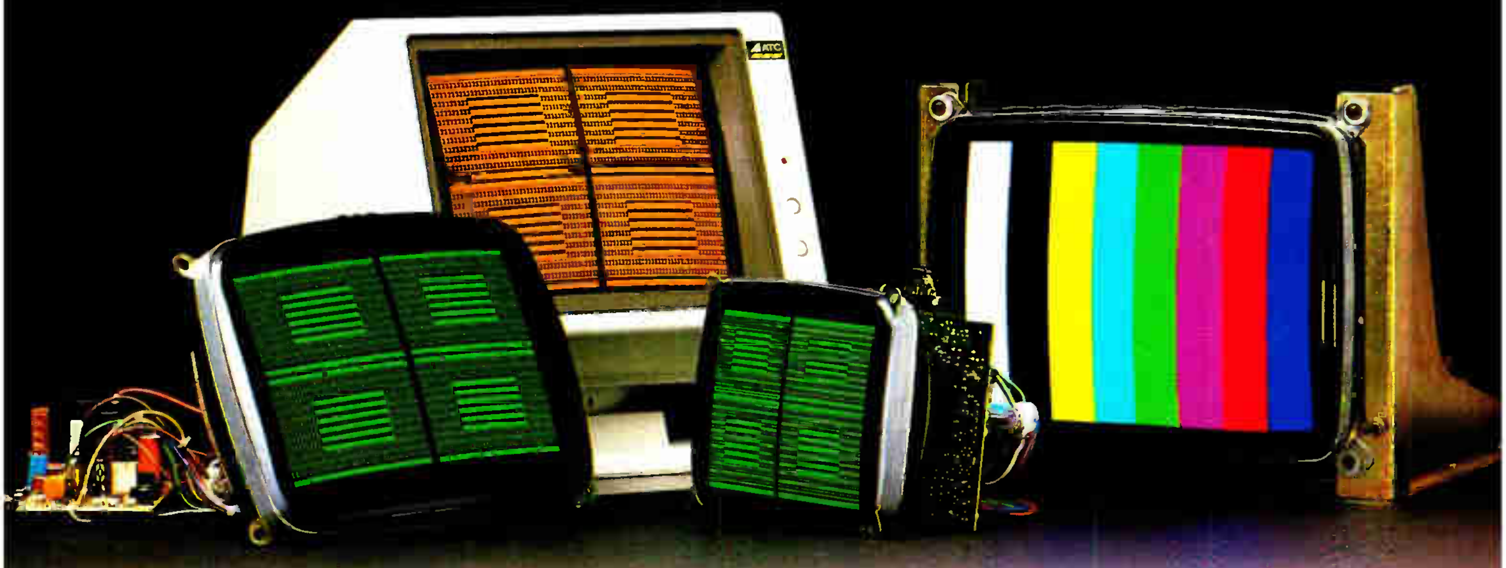

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Circle 195 on reader service card

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UNIX System V for Development

Derived from AT&T-licensed UNIX System V, our new UN/System V includes a full set of UNIX development tools, Bell license, Berkeley extensions, access to UNIX application programs, and support for Fortran, RM/COBOL,* C, Pascal, BASIC, and Unify* relational database.

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UNOS, our proprietary UNIX-compatible operating system, has real-time capabilities that UNIX can't offer. Capabilities, like eventcount synchronization, priority scheduling, and enhanced file system reliability, that are essential in industrial and scientific applications. And application programs written using UN/System V run under UNOS without modification and without a UNIX license, a saving that OEMs can pass on to customers.

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UN/System V and UNOS run on our Universe 68 family of computers. They are true super micros, with a 32-bit, 12.5MHz 68000 processor, a second 68000 front-end processor, 32-bit 4Kb cache, 32-bit bus, up to 5Mb of 32-bit RAM, high-capacity disk drives, and 1.25 MIPS performance. Quantity-one OEM prices start under $10,000.

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Circle 197 on reader service card

System integration

Converter links any printer to IBM systems

A protocol converter that lets a variety of ASCII printers emulate International Business Machines Corp.'s popular 3278 printer series on an IBM 3274/3276 cluster controller promises to save users 50% to 80% when they add printing capacity to their systems. A board-level version of the PA1500 protocol converter will also afford original-equipment manufacturers a competitive foothold in printer markets that have been previously dominated by IBM's 3278 line.

The PA1500 will initially link printers sold by Dataproducts, Anadex, Epson, NEC, Okidata, and Diablo to the IBM 3274/3276 cluster controller. The company says it plans to accommodate more printer models as time goes on. The converter sits between the printer and the cluster controller, connecting to the latter through a coaxial cable.

The unit's easy-to-install single connector supports either RS-232-C serial connections or parallel Centronics-compatible connections without modification of the printer unit. Five dual-mode front-panel switches enable users to configure a printer for all IBM 3278 functions as well as to select additional capabilities not found on IBM printers but offered by a competing model: graphics, bar-code generation, alternate character sets, and the like.

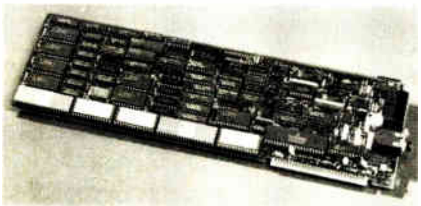
While the IBM 3278 family offers speeds of 80 to 120 characters/s at prices ranging from about $4,800 to $6,000, equally speedy non-IBM printers, often with additional capabilities, sell in the $500 to $1,000 range. Since the PA1500 unit costs $1,495 in its stand-alone end-user version, many users will find it a bargain to add a non-IBM printer to an IBM-based system, the company maintains. For OEMs, the per-unit cost of adding the PA1500's capabilities to their printer lines will be negotiable, but will typically be around 40% of the end-user price, according to its manufacturer.

Available now as a compact, 2.5-by-9.5-by-11.5-in. box for end users, the PA1500 also comes in a board-level version, which the company says will help OEMs customize it for incorporation into particular printer product lines.

Avatar Technologies Inc., 99 South St., Hopkinton, Mass. 01748. Phone (617) 435-6872 [Circle reader service number 401]

Card recognizes, synthesizes speech; also manages phones

The VPC 2000 Voice Card provides voice recognition, speech generation,



and telephone management on a single plug-in card. With Voice Key Software, the Voice Card can be used for speech command and control of any application programs running on the International Business Machines Corp.'s Personal Computer and its bus-compatible brothers.

For each application program, the user may define up to 64 voice utterances that are linked to sequences of key strokes. The Voice Card listens for voice commands and automatically types the key strokes linked to each command.

The system also features the company's continuous speaker-dependent recognition, which allows individuals to speak without pauses between words. A word-spotting capability picks out target words located anywhere within a stream of normal conversation. Voice Card also has telephone interfacing capabilities, including automatic answering and dialing, encoding, and decoding.

The VPC 2000, composed of a printed-circuit board that plugs into an auxiliary-system bus slot on the IBM PC. Microphone, speaker, software, and documentation are included. Priced at $2,450, the system is available now.

Votan, 4487 Technology Dr., Fremont, Calif. 94538. Phone (415) 490-7600 [Circle 403]

System monitors data net and does matrix switching

A single system for centralized management and control of small and large data-communications networks integrates network-performance monitoring, matrix switching, and management reporting. With Intelli-MAX, users can identify and correct network problems and analyze network performance from one cathode-ray-tube terminal.

Intelli-MAX produces color-graphics displays of up to seven layers of network activity and presents information on communications activities. Color-coded alarms on the screen notify the user of network-component problems or failures. Once a failure has been identified, Intelli-MAX's matrix-switching capability supports instant reconfiguration of the network using the same CRT terminal.

The system also displays network activity minute by minute and in five-minute color trends. Another feature, a cumulative-events alarm, tracks user-specified network conditions over a designated time period and warns the user of sporadic network failures.

To facilitate network planning and documentation, Intelli-MAX's dual data bases—host and local—can provide management reports both on the screen and in hard copy. The local data base can be accessed to produce standard reports on network utilization and performance. Through dy-

Our new round connector is a great big zero.

ITT Cannon's Commercial/Industrial Division announces the first round ZIF connectors. Anywhere. For low-cost reliability in demanding situations.

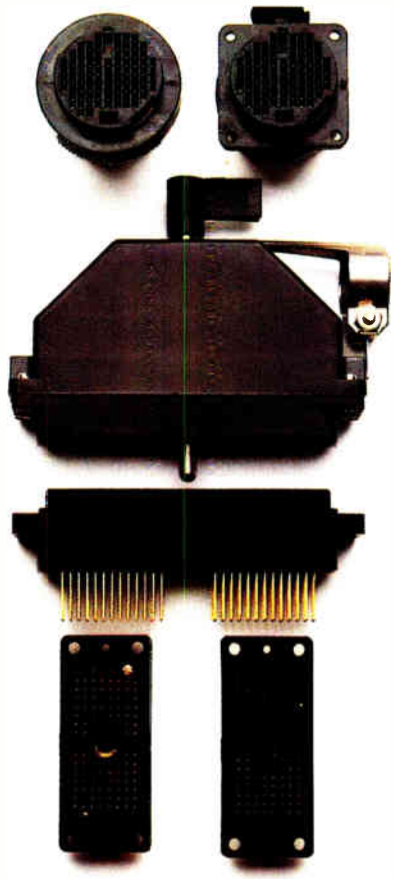
The new round ZIF is a high-performance, multiple-wire power and signal connector that features the popular 22-shell size and up to 82 contact positions. It fits existing circular-type size 22 panel holes, yet provides higher pin density.

And what less can we say?

Except that its total installed cost is less than that of comparable normal-force connectors. But that's just the start. We made our new RDL to be fast and strong. Its low torque requires only a quarter-turn to couple.

And our ZIF contact design makes the RDL a lasting connection. With a rated minimum life of 5,000 matings/unmatings; that's ten times greater than most standard connectors.

The RDL/DL Zero-Insertion-Force Connectors



These new RDLs are available for cable-to-cable and cable-to-panel applications.

Because your engineering requirements may call for a quality ZIF connector other than our RDL, we also make the rectangular DL connector, with all of the performance features of our RDL ZIF connector.

Call ITT Cannon for all of your connector needs, and you'll see how we turn zeros into pluses.

Contact the Commercial/Industrial Division of ITT Cannon, a Division of ITT Corporation, 10550 Talbert Avenue, Fountain Valley, CA 92708. Telephone: (714) 964-7400. For the sales office nearest you, call toll-free: (800) 845-7000.

CANNON ITT
The Global Connection

Circle 199 on reader service card

namic rotational monitoring, the system can be tailored to meet each user's needs. With this feature, users can monitor portions of their network at will, without disrupting service and without having to move T-connectors from line to line.

The Intelli-MAX system can support 16 to 512 communications lines. Fully configured systems, including the control processor, a color terminal, a color printer, and scan units, start at $61,400. They will be available in the fourth quarter.

Data Switch Corp., 444 Westport Ave., Norwalk, Conn. 06851. Phone (203) 847-9800
[Circle 402]

Controller links work stations, terminals to dissimilar hosts

The Netway 274 Multi-Dissimilar Host Cluster Controller connects a variety of work stations and peripherals to multiple and dissimilar hosts. Each Netway 274 supports up to 16 work stations connecting up to five multipoint and 16 point-to-point host connections.

The system includes a floppy-disk system for loading system software and configuration information and a parallel printer port. The company also offers an optional networking software package that connects up to 128 Netway 274s over an unlimited geographic region.

Protocols suppported by the Netway 274 include IBM 3270 Binary Synchronous Communications, IBM 3270 Systems Network Architecture/Synchronous Data-Link Control, Burroughs Poll/Select, and asynchronous start-stop. Features include password-protected configuration parameters that can be altered on line without affecting other users on the system and printers that can be dedicated to a single application or shared by many work stations.

Prices for the product, available now, start at $9,150. A configuration capable of connecting eight work stations sells for $12,510.

Tri-Data, 505 E. Middlefield Rd., Mountain View, Calif. 94039. Phone (415) 969-3700
[Circle 405]

The Ultimate in IEEE-488 Data Storage

So It's Always There When You Need It

Dylon, the world leader in magnetic tape systems and controllers for GPIB (IEEE-488) users, offers the ultimate in data recording and storage. Whether your bus controller system is Hewlett Packard, Tektron x, Fluke, DEC or the IBM Personal Computer, you keep the data you need at a cost you can afford.

Built for reliability, Dylon magnetic tape controllers and systems give you field-proven dependability in such demanding applications as military aircraft, shipboard or other mobile installations throughout the world.

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Dylon Data Corporation

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Circle 201 on reader service card

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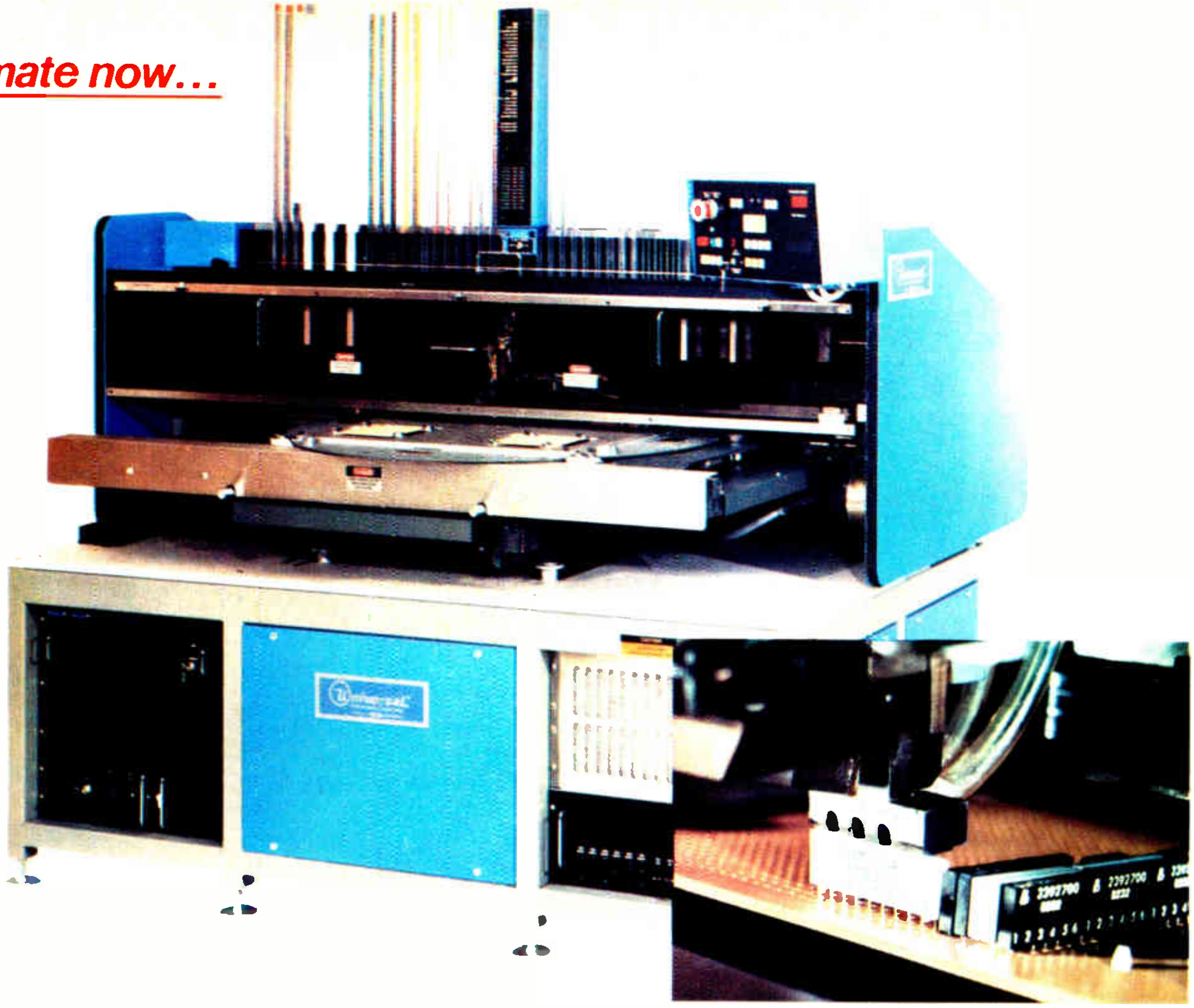

This new high speed sequence, insert, and clinch system just made molded SIPs an important component design for large volume users.

Only Universal's "Convertible SIP System"

- Automatically inserts high, medium or low profile molded Single In-Line Packages with 2, 4, 6, 8 and 10 leads.
- Has a cycle rate up to 3,600 an hour, depending on insertion pattern and magazine location.
- Can virtually "brickwall" SIPs because of its high density insertion tooling.
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- Is controlled by new software that is more "user friendly" and designed to grow with all Pass-Thru II modular systems.

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Circle 202 on reader service card

Factory automate later.

We promised. We delivered.

Company	Model	Speed	Accuracy
CyberTech	V200-HV	100 MHz	50 ps
Fairchild	S50	50 MHz	600 ps
GenRad	GR18	40 MHz	1000 ps
Megatest	MegaOne	40 MHz	700 ps
Takeda Riken	3340	40 MHz	800 ps

Comparisons from Electronics Test, January 1984, and manufacturers' literature.

We're former test engineers, now solving VLSI testing problems. You needed an accurate, high-speed VLSI tester, and CyberTech built it. The performance chart summarizes the story. CyberTech promised you 100 MHz speed, unprecedented accuracy, and up to 256 pins. This isn't the whole story. CyberTech made a VLSI tester that's easy to program, easy to network, without learning complex new languages.

CyberTech engineers were evaluating components for supercomputers long before adequate testers were available. So, we applied supercomputer technology to solve the component testing problem.

Supercomputer test architecture, affordable, American-built. Menu driven, high-level test software makes the Viking 200 user friendly for test engineers. Plus, automatic calibration.

Think CyberTech for your most demanding VLSI, ASIC (Application Specific IC), or VHSIC program requirements.

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Circle 203 on reader service card

A tough epoxy that can cure at room temperature is a suitable choice for potting electronic devices to protect against moisture, breakage, and contamination or to conceal the contents. With a low viscosity (1,000 centipoise, typically), it can be used with pouring equipment, can fill voids and cavities, and level out to a smooth surface when cured. EPO-TEK 509F contains no solvents and has a low thermal coefficient of expansion. A 1-lb evaluation kit is available now for $13.25.

Epoxy Technology Inc., 14 Fortune Dr., Billerica, Mass. 01821. Phone (617) 667-3805 [Circle reader service number 477]

Improvements made to the model 2100 transparent static-shielding bag include a 25% stronger seam, thanks to an increase in the bag's thickness and to the use of an improved sealing process. Also, a new additive incorporated into the bag's inner polyethylene layer further improves protection against triboelectric (frictional) charging caused by parts moving within the bag. The bags are available now in 24 sizes ranging from 4 by 4 in. to 24 by 36 in. Prices remain as they were for the earlier versions. Custom sizes are available on special request.

3M Co., P. O. Box 33600, St. Paul, Minn. 55133. Phone (612) 733-1186 [Circle 478]

An oxide-free solder cream, SMD P100, improves the reliability of soldered assemblies using surface-mounted devices, thanks to uniformly sized spheres in an inert, temperature-stable material. The spheres, which are 100 mm in diameter, are entrapped in the solder joint. As a result, there is uniform spacing between the substrate and the component lead. This controlled spacing provides clearance for vapor dissipation during the soldering process and solvent flushing where postsolder cleaning is required. The inert spheres do not affect the electrical or mechanical properties of the solder joint. Pricing of the material depends on the alloy and flux required.

Multicore Solders, Cantiague Rock Rd., Westbury, N. Y. 11590. Phone (516) 334-7997 [Circle 480]

A single-component low-fire fritless silver paste is slow-drying and can thus be used to screen conductors on printed-circuit boards. Aremco-Coat 560 can be cured at temperatures as low as 95°C in 1 h. The material adheres well to plastics and metals and can be screened in line widths down to 0.002 in. The 560 silver produces a high conductivity pattern in

thicknesses down to 0.00025 in., which can then be copper-plated. Its sheet resistivity is less than 0.04 ohms/square.

Available two to three weeks after receipt of order, the material sells for $1.65 per gram. A minimum order of 50 g is required.

Aremco Products Inc., P. O. Box 429, Ossining, N. Y., 10562. Phone (914) 762-0685 [Circle 479]

With a tensile strength of 8,000 lb/in.², the Flextherm 08A41H insulating material is resistant to abuse and can be employed for jumper cables and printed-circuit-board interconnections. Measuring 0.006 in. thick, the material consists of 0.0015-in. polyester bonded to 0.004-in. vinyl. Bond strengths between layers give excellent resistance to delamination. The material's dielectric strength is 2,200 V/mil. Available in master rolls up to 54 in. wide and 2,500 running yards, the material conforms to Underwriters' Laboratories 83 and 94 flammability ratings. It is priced at $3 to $10 per yd².

Keene Laminates, P. O. Box 4305, West Providence, R. I. 02914. Phone (404) 434-2340 [Circle 430]

An ultraclean line of static-control table mats can drain electrical charges from people, tote boxes, and components. The Statfree CP604's single-layer homogeneous construction provides a cushioned work surface. Available in three colors, the nonflammable mats are safe for use in clean rooms.

Resistant to most chemicals, detergents, flux, and solder, the Statfree mats provide 10^9 ohms/square surface resistivity per ASTM D257 and are rated static dissipative by Department of Defense Handbook 263.

A 2-by-2-ft mat costs $22, a 2-by-4-ft one $38. They are available now.

Charleswater Products Inc., 93 Border St., West Newton, Mass. 02165. Phone (617) 964-8370 [Circle 432]

A lead-frame tape called Lead/Lock offers semiconductor manufacturers and packagers superior bonding and high-temperature resistance for securing highly cantilevered leads. The tape is easy to handle, permits bonding, and comes in 150- or 300-ft rolls without splices or interleaving.

The six widths range from 0.190 to 0.580 in. The tape is made of a Kapton polyimide-base film that is coated with a proprietary modified-acrylic adhesive system in a clean room. Bond strength is typically 250 lb/in². Available now, the tape costs as little as $7.60 a roll.

Rogers Corp., Circuit Materials Division, 2001 West Williams Field Rd., Chandler, Ariz. 85224. Phone (602) 963-4584 [Circle 434]

With a VO flammability rating from Underwriters' Laboratories, the Technoply 3003VO is suitable for high-temperature printed-circuit boards in TV sets, radios, and control systems. The polyimide-and-fiberglass copper-clad laminate is also available in prepreg form.

Its glass-transition temperature is 270°C. The product comes in sheets measuring 36 by 48 in., 36 by 42 in., 24 by 36 in., and 18 by 36 in., clad or unclad. Cladding materials include copper, aluminum, and stainless steel. Priced at $6 per square foot for copper on both sides, Technoply 3003VO is available in four weeks.

Howe Industries Inc., 13704 Saticoy St., Van Nuys, Calif. 91402. Phone (213) 781-4122 [Circle 433]

PACE MBT-200

PACE CONTINUES TO MEET THE EVER-CHANGING REWORK AND REPAIR DEMANDS OF THE ELECTRONICS INDUSTRY, WITH THE NEW, TOTALLY SELF-CONTAINED MBT-200 SYSTEM.

Designed for fast, spike-safe desoldering and temperature controlled soldering of electronic assemblies, the MBT-200 system represents a new breakthrough in desoldering technology, featuring the PACE "instant rise", rotary carbon vane pump. Vacuum rise time is now instantaneous, which insures the non-destructive removal of any solder joint. The system's new low voltage, light weight, pencil-grip handpiece has the best "tip-to-grip" ratio in the industry — with integral finger-tip actuation, it permits more precise operator control.

The MBT-200 System is designed to meet UL as well as international electrical standards to satisfy high production requirements of the most sensitive and demanding desoldering applications.

Of course, low cost makes the MBT-200 especially attractive. Arrange for your demonstration today!

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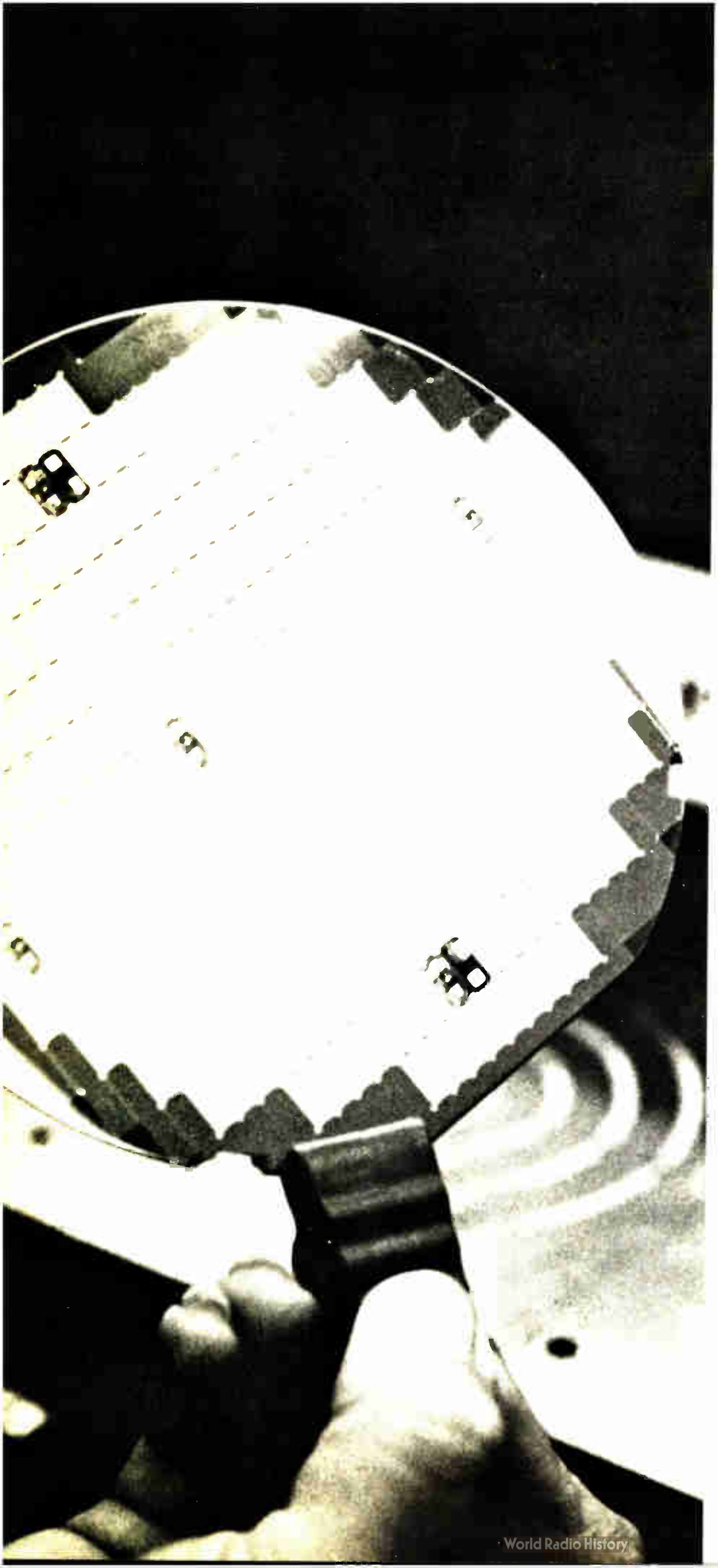
Systems for Repair, Development and Production of Electronic Assemblies



Opportunities in Orlando
for VLSI Product, Process Test
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Start-up the world's newest, most exciting, high-volume VLSI manufacturing facility.

AT & T Technology Systems is seeking experienced MOS product, process, test and packaging engineers. Candidates should have a BS in Electrical/Mechanical/Chemical Engineering and 2-5 years experience in process development, facility installation, characterization and device yield improvements.

Our Orlando facility is currently under construction to manufacture the technology of tomorrow. Orlando offers you the unique opportunity to participate in the start-up, construction, planning and daily operation of a new semiconductor facility.

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Wide applications

Some LEDs let you do what you can. Stanley's new Super-Bright LED with a luminous intensity of 2,000mcd at 20mA lets you do what you want. For example, the world's brightest LEDs can create a traffic signal that requires neither periodical checks nor maintenance. It can create super-bright tail lamps for automobiles. Or with equal ease and brightness, it can create a high-tech light source for optical-fiber communications or solid-state light source for a facsimile or other office machine.

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Stanley's Super-Bright LED can be as bright as 100mcd at 1mA — a fraction of the current you needed until now for 100mcd. Connected directly to CMOSs, matrix display equipment and other machines literally shine with new energy efficiency. In addition to red LEDs with luminances ranging from 500mcd to super-bright 2,000mcd, Stanley can supply high luminance 80mcd and 200mcd LEDs in green, yellow and orange. For variety and applications unlimited, specify Stanley. Now more than ever, we can make all your bright ideas shine even brighter.

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Products newsletter

Start-up firm launches high-performance amp

Barely nine months after its founders spun off from National Semiconductor Corp. and Intersil Inc., Elantec Inc. has announced its first six products, a series of high-performance amplifiers. **Elantec will specialize in high-speed, high-bandwidth, high-power, and high-slew-rate amps used in analog-to-digital and digital-to-analog converters.** They are all hybrid versions of National chips, available from stock. The Milpitas, Calif., firm's next products will be dielectrically isolated monolithic operational amplifiers.

Mobile module supports video conferencing

The Vitalink Corp., a Mountain View, Calif., satellite communications firm, has introduced a two-way, full-motion video-conferencing module that can be rolled into conference rooms. **The module integrates video cameras, monitors, speakers, and a codec for image and audio processing.** A separate earth station links the user with Vitalink's satellite communications system. The video conferencing module costs $159,500; with an earth station, prices start at $295,000. The system includes graphics transmission with three times the resolution of video images.

System tests, repairs static and dynamic RAMs

Fully integrated test and repair of random-access memories with redundant circuitry extends to both static and dynamic parts with Teradyne Inc.'s J386A/M118 memory-test and -repair system. Like its predecessor, the J385A/M118, which handled only dynamic RAMs, **the newer system speeds optimization of testing, defect-analysis, and repair programs by using a common language called Pascal-T** [*Electronics* Nov. 17, 1982, p. 233]. The J386A/M118, whose laser beam disconnects faulty circuits and activates substitutes from a RAM chip's redundant elements, will cost about $500,000 and will handle memories of up to 256-K densities, Teradyne says. The system, which will also sport a new $52,000 option for automatic wafer transport and positioning, will make its debut at next month's Semicon West show, in San Mateo, Calif. Delivery from the Boston, Mass., firm will take about 30 weeks.

Digital interface chip will transmit at 144 kb/s

Mitel Corp., Kanata, Ontario, Canada, and Elektrisk Bureau Communications, Oslo, are jointly developing a two-wire digital interface chip based on the Norwegian firm's patented adaptive echo-canceling techniques. **The complementary-MOS IC provides two-wire line transmission at an aggregate data rate of 144 kb/s.** Two 64-kb/s channels for information transfer and one 16-kb/s channel for signaling and packetized data transfer are provided by the IC, which complies with the International Consultative Committee for Telegraphy and Telephony's recommendations for ISDN integrated-services digital networks. Mitel expects to begin volume production by early 1985.

Tool maker enters instrument market

OK Industries Inc., a New York maker of tools for assembling electronic products, has diversified into the test and measurement market. **The company's new products include a full-capacity 1-MHz a-m/fm function generator; a 50-MHz pulse generator;** a 200-MHz universal counter; and a 1.3-GHz universal counter with microwave capability. Prices range from $275 for the function generator to $875 for the 1.3-GHz counter, and delivery takes four weeks.

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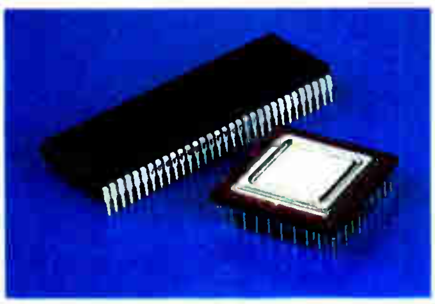

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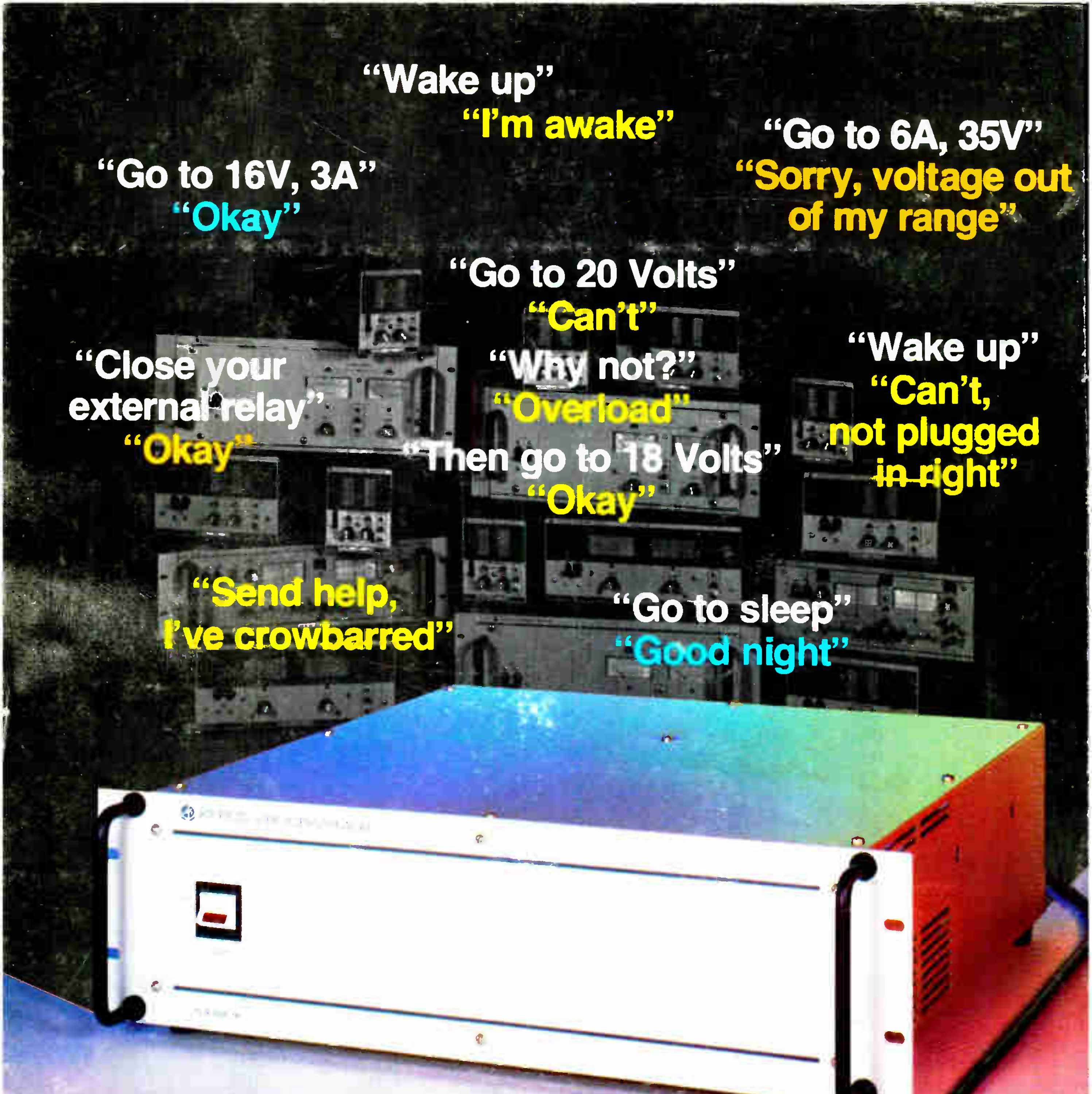
Circle 901 on reader service card



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