MARCH 10, 1983

GEAR FOR BYPASSING LOCAL PHONE SERVICES LURES BIG USERS/93

Software verifies computer maintenance program/144

Work station boasts high-level interactive graphics/129

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Electronics

SPECIAL REPORT

Self-testing the untestable

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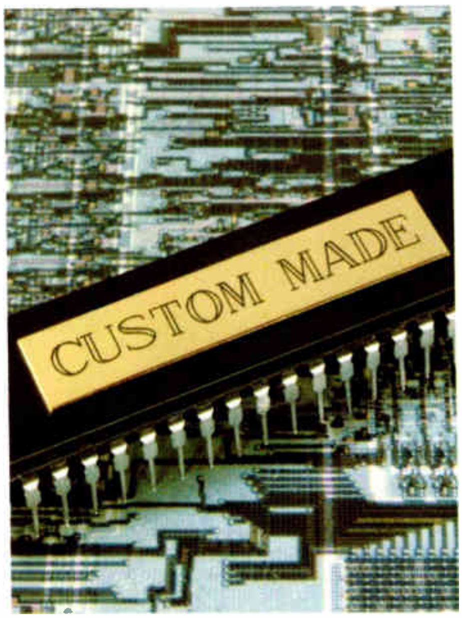

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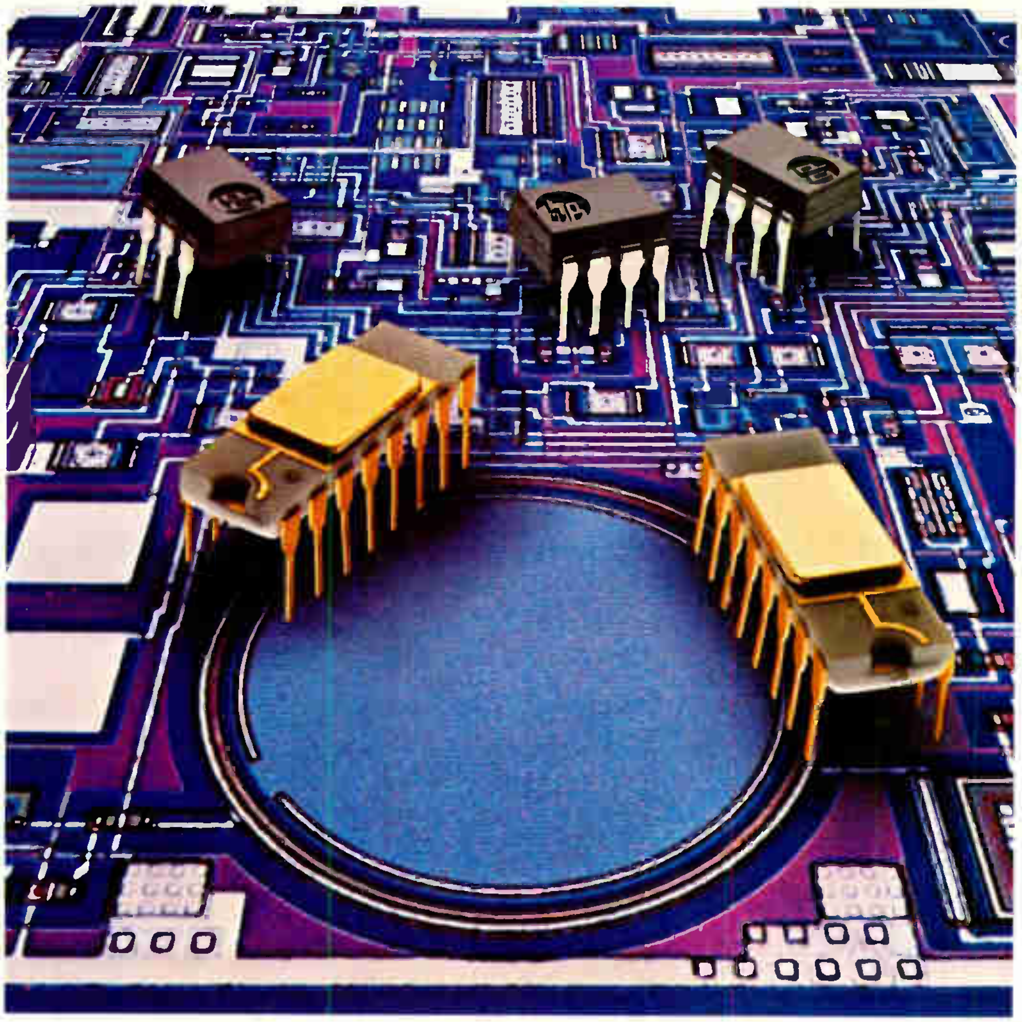

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The cover story

Major New Developments

NEWSLETTERS

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Vol. 56, No. 5 • March 10, 1983

Electronics Review

Electronics International

Probing the News

Technical Articles

New Products

Highlights

Cover: Self-testing comes to the VLSI world, 109

Testing very large-scale integrated circuits is a nightmare of complexity, so considerable effort is going into self-testing schemes. This special report presents three such developments. For self-testing from IC to system levels, an on-chip combination of level-sensitive scan design, pattern generation, and signature analysis is already proving itself (p. 110). For microprocessor boards, a package of software and shift registers can be added to test all portions of the processor sequentially (p. 116). Testability is a design concern, and a software adjunct for the Tegas computer-aided–design system answers that challenge directly (p. 120).

Ship-to-stock takes root in U. S. semiconductor arena, 96

New emphasis on improved quality levels and closer working relationships with customers are enabling U. S. chip makers to supply parts that vastly simplify the incoming test chore: an approach known as ship-to-stock.

All-dynamic circuitry lowers power use in microcomputer, 125

A well-known 4-bit p-channel MOS microcomputer emerges from a redesign with all-dynamic logic, thereby achieving complementary-MOS power use at low cost.

Terminal takes over graphics-processing functions, 129

Incorporating two microprocessors, a terminal for computer graphics systems takes over most of the geometry-processing and display-control functions from the central processing unit. To make life easier for the system designer, it comes complete with high-level interactive graphics software.

Closed-loop servo combines performance, reasonable cost, 139

After evaluating the three existing types of closed-loop servomechanisms for positioning read-write heads, designers of a Winchester disk drive came up with a refinement that retains the accuracy in positioning of its progenitor, yet costs significantly less to realize.

Fault-simulation model helps debug electromechanical devices, 144

With the aid of a package of simulation software, designers and manufacturers of printers and other peripherals for small computers can model their electromechanical devices and check out the accuracy of maintenance programs intended for both debugging and troubleshooting in the field.

Coming up . . .

Real-time operating systems for 16-bit microsystems . . . a 4-megabyte bubble-memory package . . . automated calibration and characterization for greater accuracy and versatility in a phase-noise measurement system.

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Circle 5 on reader service card

Publisher's letter

To buy the benefits of very large-scale integration, part of the price is the cost of testing circuits with thousands of transistors packed onto them. The multitude of nodes simply cannot be probed one by one as can chips having only hundreds of transistors, and with many designers using VLSI, there is now the threat that boards and systems could become impossible to test. Even with just LSI, testing chips, boards, and finally systems is painstaking and expensive.

To counter that threat, digital-circuit designers are turning to self-testing techniques that isolate faults down to bad chips. "The first papers on self-testing surfaced at the International Test Conference at Cherry Hill some four years ago," remarks Jerry Lyman, our packaging and production editor. "At the last Cherry Hill, in November, there were two whole sessions devoted to it. And papers appeared for the first time at ISSCC [International Solid State Circuits Conference] this year."

Self-testing, then, is an idea whose time has come. "There are cradle-to-grave savings, starting with the chip makers and going all the way out to the field engineers who service the equipment," says Richard Comerford, our test, measurement, and control editor. Still another driving force for the spread of self-testing is that it is mandated for the Department of Defense's Very High-Speed Integrated Circuits program.

"We'll see many more commercial chips with self-testing," Rich predicts. And that will change the facts of life for automatic-test-equipment suppliers, he adds. "Circuit and board testers will be less complex in the future because the chips themselves will be doing much of the job." He expects self-testing techniques, currently the province of large, highly sophisticated companies, to trickle down fairly soon to medium-sized and small producers of equipment as well.

New techologies almost unfailingly bring with them a lingo all their own. So when Rich and Jerry talk about self-testing, terms like LSSD, Bilbo, and Microbit pepper the conversation. Not surprisingly, these same terms turn up time and time again in the three-part special report the two have compiled on self-test schemes (it starts on p. 109).

IBM pioneered self-testing for computers in the early 1970s, with an approach it called level-sensitive scan design (LSSD). Says Jerry, "Every time IBM does something very sophisticated, others say it would be too expensive for them though they finally come around to it."

One company that has come around to its version of LSSD is Storage Technology Corp. The Louisville, Colo., firm has paired the IBM idea with the built-in logic-block observer (Bilbo) concept, first devised in West Germany, to bring self-testing to a gate array (p. 110). Another early convert to self-testing is Siemens. The Princeton, N. J., research unit of the West German company has worked out a microprocessor built-in test technique (Microbit) based on a pair of Bilbos (p. 116). For the many other engineers who must add self-testing to their chip designs, work-station software is already available (p. 120).

Paul W Bin

Time to order your *Electronics* editorial index

An index of the editorial material that ran in 1982 (Vol. 55) is now available. To get your copy, simply circle No. 475 on the reader service card inside the back cover. If the card is no longer there, order by letter from Kathleen Morgan, *Electronics*, 1221 Avenue of the Americas, New York, N. Y. 10020. There is no charge for the 1982 index; if you want indexes for earlier years, they can be obtained from our reprint department for $6.00 each.

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Circle 7 on reader service card

Readers' comments

Robbing Peter

To the Editor: In your In my opinion column ["Industry must help the university," Dec. 29, 1982, p. 20], Prof. Comer proposes that industry help universities by donating $1,000 for each graduate hired. Yet hiring a school's graduates is precisely the means by which industry supports universities.

Schools logically depend on students to pay for the educational services provided. A school that graduates 100 electrical engineers per year probably has a total of about 500 engineering students. Increasing tuition by $100 per semester would bring in the same $100,000 per year as Comer's proposed industry contribution. Likewise, it should be noted that industry could obtain this money only by reducing the pay of its new hires. The schools would then be hurt as the lower salaries reduced the number of students attracted to their courses.

Having industry pay the universities to educate students is not wise. We should avoid even a small step in that direction. Carried to the limit, such an action would have industry running the schools, and Prof. Comer would then work for a corporation as well.

Richard G. Wiley
Syracuse Research Corp.
Syracuse, N. Y.

Getting the big picture

To the Editor: Regarding your Probing the news feature of Dec. 29, "High-definition TV is still on hold" (p. 51), I should like to point out that current theories of high-definition television (HDTV) fail to distinguish HDTV as an improved medium from HDTV as a new medium. That distinction is reached, it seems to me, when the image displayed is so large—with a corresponding increase in the number of pixels to maintain resolution—that television is no longer foveal in character.

It is well-known (but often improperly explained) that a two-hour lecture can be easily tolerated in person, but the same lecture is hopelessly tedious when televised. The common explanation, the fact of being there, is not correct; the lecture would be equally dull viewed from the next room through a 25-inch hole. The real difference lies in the larger field of view and the ability to look at the lecturer's shoes whenever the viewer wants to.

Nonfoveal TV could eventually occupy 4,000 TV lines at 60 frames a second, a mind-boggling 3 gigahertz in uncompressed bandwidth. But such a medium would be as different from foveal television as movies are from slides. Though 4,000-line technology will not be practical in this century, it would be shortsighted at this point to consider the resolution of 35-millimeter film as the ultimate in image quality, which is what is now being done. Instead, upwardly flexible standards that also account for image size should be set. The best of the currently proposed HDTV systems will be slightly nonfoveal and, if implemented, will inevitably presage a market for more large-scale video image displays.

Incidentally, nonfoveal television is intrinsically incompatible with foveal television, so that the simple compatibility standards being discussed will not work. In the former, different (and less) camera work is required because the viewer selects his or her own point of attention.

Adam L. Carley
Atkinson, N. H.

Correction

In our Probing the news story "High-definition TV is still on hold" (Dec. 29, p. 51), some data from the graph credited to the February 1980 SMPTE Journal was inadvertently deleted or misplaced. The graph, which summarizes data from the the Society for Motion Picture and Television Engineers' HDTV Study Group Report by Donald Fink, should have compared the subjective sharpness of 8-, 16-, and 35-millimeter film—both projected and displayed on a 525-line studio video monitor—to that of both 525- and 1,100-line TV systems. However, only the data for film converted by telecine for video display was given. The omitted ratings for film viewed on a projection screen would have shown 35-mm film at its best rated as slightly superior in sharpness to 1,100-line TV (HDTV) at its best and 16-mm film at its best rated as sharper than 525-line TV but less sharp than the 1,100-line system. Likewise, the "good–very good" bar for video-tape sharpness attributed to the 1,100-line system should have represented a "good" rating for the 525-line system.

1983 WORLD MARKETS FORECAST ERRATA

The following changes correct two tables in the 1983 world markets forecast [*Electronics*, Jan. 13, 1983]. These figures are in millions of dollars.

On page 128, U. S. semiconductor consumption should have read:

	1981	1982	1983	1986
Semiconductors, total	7,006.9	7,860.0	9,613.9	16,550.5
Integrated circuits, total	5,416.1	6,277.3	7,923.2	14,432.2
Custom ICs, total	336.7	425.8	584.3	1,410.9
Fully custom	241.1	240.0	260.0	331.6
Gate arrays	74.5	132.0	211.1	596.9
Standard-cell	21.1	53.8	113.2	482.4

On page 146, West Europe equipment consumption should have read:

	1982
Consumer products, total	14,512.1
Audio equipment, total	5,204.8
Car audio	723.6
Hi-fi equipment, total	2,146.3
Components	1,553.6
Consoles and compact systems	592.7
Phonographs & radio-phono combinations	354.5
Television receivers, total	5,396.3
Color	4,981.3
Black and white	415.0
Test and measuring instruments	
Oscillators	54.0
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COHERENT is compatible with UNIX both at the **C** source level and at the user command (shell) level. This makes the large base of software written for UNIX available to the **COHERENT** user.

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- multiuser and multi-tasking facilities,
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- tree-structured, hierarchical file system,
- pipes, asynchronous software interrupts, and memory sharing for interprocess communication,
- generalized internal segmentation model allowing flexibilities such as memory sharing,
- ability to lock processes in memory for real-time applications,
- fast swapping with swap storage cache,
- minimal interrupt lockout time for real-time applications,
- power failure recovery facilities,
- fast disc accesses through disc buffer cache,
- device drivers, the swapper, and some other system facilities are loadable, considerably simplifying configuration and driver development,
- process timing, profiling and debugging trace features.

*UNIX is a trademark of Bell Labs.

Software Tools

In addition to its facilities for basic file and process manipulation, **COHERENT** provides well over 100 utility programs and an extensive subroutine library. The following major software components are included: **SHELL,** the command interpreter; **STDIO,** the standard C I/O library; **MATH,** library of mathematics routines; **AS,** an assembler for the host machine; **CROSS,** a number of cross-assemblers and cross-compilers for other machines are available with compatible object formats; **DB,** powerful symbolic run-time and postmortem debugger for **C** and assembler; **ED,** a context-oriented text editor with regular expression patterns; **NROFF,** text formatting, spelling checking and other utilities related to word processing; **SORT,** sort program with generalized key and record specification; **SED,** a stream editor (used in filters) fashioned after **ED; GREP,** efficient file search for a pattern; **DIFF,** give minimal differences between 2 or 3 textual files; **AWK,** a pattern scanning and processing language; **M4,** macro-processing language; **LEX,** generates lexical analyzer programs; **YACC,** advanced language to generate parsing program from a grammar; **MAKE,** aids in construction and maintenance of a program or software package; **SCCS,** maintain several versions of source code and documentation for a large software project; **LEARN,** computer-aided instruction about **COHERENT; BC,** arbitrary precision desk calculator language; **QUOTA,** various programs to account for system resource usage; **MAIL,** an electronic personal message facility; and **DUMP,** incremental file backup system.

Of course, **COHERENT** will have an ever-expanding number of programming and language tools and basic commands in future releases.

Language Support

The realm of language support is one of the major strengths of **COHERENT**. The following language processors are supported:

- **C** — a portable compiler for the language **C**, including stricter type enforcement in the manner of **LINT**.
- **PASCAL** — portable implementation of the complete ISO standard Pascal.
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The unified design philosophy underlying the implementation of these languages has contributed significantly to the ease of their portability. In particular, the existence of a generalized code generator is such that with a minimal effort (about one man-month) all of the above language processors can be made to run on a new machine. The net result is that the compilers running under **COHERENT** produce extremely byte-efficient code very closely rivaling that produced by an *experienced* assembler programmer. Finally, the unified coder and conformable calling sequences permit the intermixture of these languages in a single program.

Operating System

Because of the language portability discussed above, and the substantial effort in achieving a greater degree of machine-independence in the design and implementation of the **COHERENT** operating system, only a very small effort is required to transport the whole system to a new machine. This means that an investment in **COHERENT** software is not tied to a single processor. Applications can move with the entire system to a new processor with about two man months of effort.

COHERENT is available for all Digital Equipment Corporation PDP-11 computers with memory management, such as the PDP-11/23, PDP-11/34, PDP-11/44, and PDP-11/70. The system is implemented for the Intel 8086/8087/8088, the Zilog Z8002, and the Motorola 68000 processors. Future plans call for **COHERENT** implementations for many other machines, including the DEC VAX-11 family and IBM 370-compatible computers.

Because **COHERENT** has been developed independently, the pricing and licensing is exceptionally attractive. Of course, **COHERENT** is completely supported by its developer. To get more information about **COHERENT,** contact us today.

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Circle #11 for literature

Editorial

It's time to take a cue from the Old World

Learning to live with the Japanese industrial machine isn't just a U. S. problem. Across the Atlantic, West Europe's Economic Community recently reached agreement with Tokyo on how many video-cassette recorders and television tubes the Japanese may export to Europe and also on monitoring the export of other sensitive electronic items.

Under the agreement, Japan's Ministry of International Trade and Industry has undertaken to limit exports of VCRs to 4.55 million sets, or about 60% of the European market, leaving Philips of the Netherlands and and Grundig AG of West Germany with a minimum share of 1.2 million sets, or 20%. The Japanese have also agreed to align VCR prices with those of West European manufacturers.

The accord has had a mixed reception. Common Market ministers are enthusiastic, since Philips and Grundig have thus won a chance to establish a competitive position in the world market even while individual European countries like France are still free to negotiate their own national agreements. But the popular press is concerned that the consumer will have to foot the bill to protect European industry.

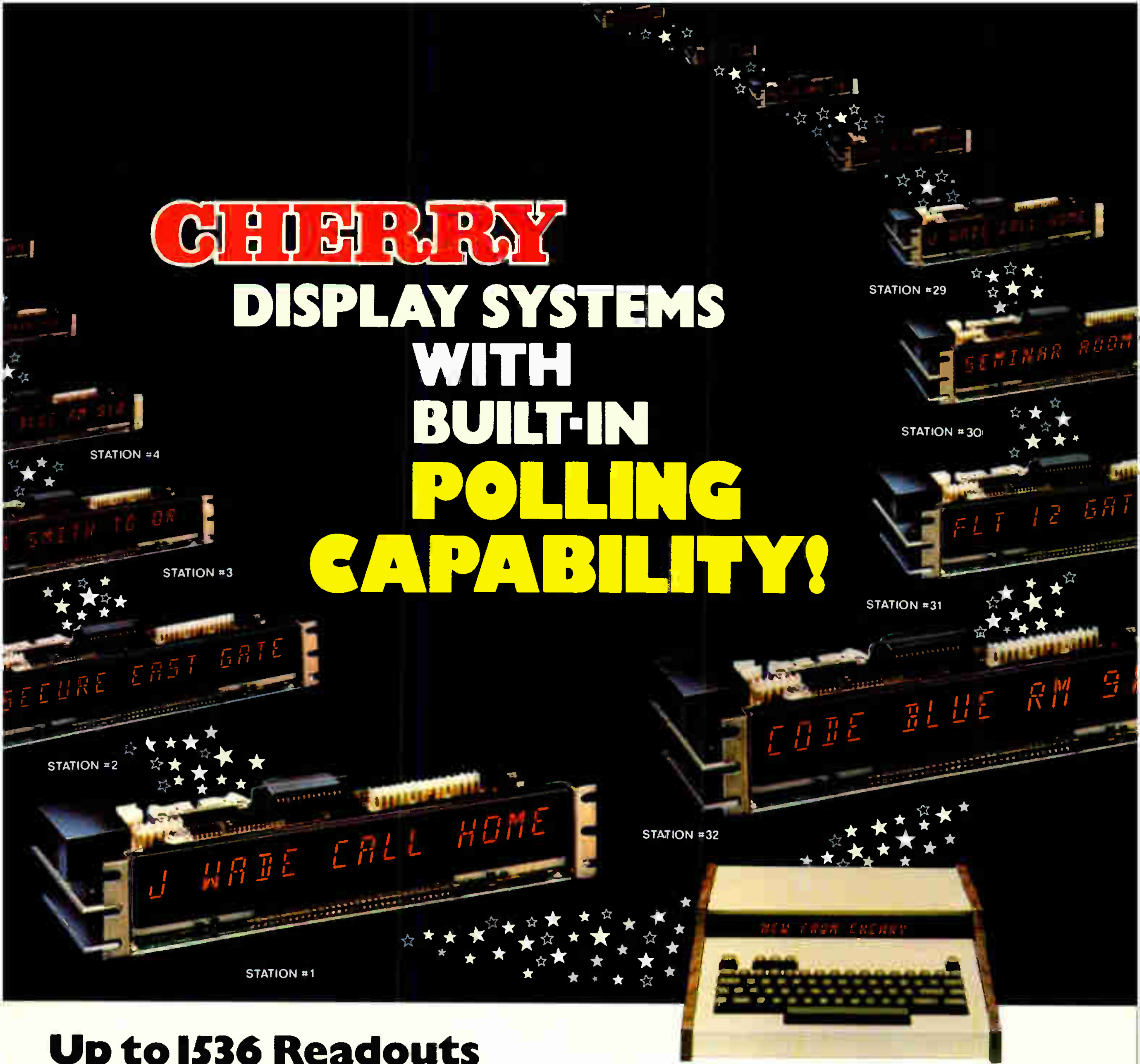
Is the European example a lesson for U. S. semiconductor makers worried about competition from Japan, particularly in memories? The answer is probably yes. A compromise can be reached, but it takes determined negotiation by government and industry. The Japanese are shrewd and wily negotiators and will give nothing away unless they have to. They use protection of their domestic markets as an industrial strategy for building production volume and must still wonder, even as they thank their lucky stars, why the countries they trade with do not retaliate in kind.

At least one lesson that the U. S. industry seems to be absorbing from its Japanese competitors is that of the effectiveness of collaborative research. The advent of such groups as the Semiconductor Research Cooperative should go a long way toward righting what Americans view as an imbalanced and unfair advantage enjoyed by their government-subsidized adversaries.

Just to show it means business, the U. S. Government could start by following the European example and—before the clamor for protection becomes overwhelming—driving for an agreement with the Japanese to monitor sensitive items like memories. If the negotiations start soon enough, the U. S. might even be able to avoid the spectacle of negotiating for a 20% share of its own market in memories. It might, too, avoid the kind of accord that fixes home prices and fails to keep manufacturers honest.

Wanted: more EEs in the political trenches

Even as governments agonize over just how much protectionism is too much, a program that has been conducted since 1973 by the Institute of Electrical and Electronics Engineers has quietly been equipping engineers to deal more effectively with the interleaved levels of the Federal legislative and political process. Called Congressional Fellows, selected EEs work in Washington on the staffs of elected representatives or of committees. The idea, to give technology a voice in the proceedings, is one that is gaining popularity, and the program, described on page 207, is one that the IEEE should consider expanding. It is time for scientists and technologists to discard the notion that politics, and the accompanying hard work of influencing America, is beneath them.



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People

Canion says new products will propel Compaq Computer

As the portable-computer business continues its fast-paced growth, companies must be quick to bring out new products if they expect to stay on top of the competition. That goes double for new companies, says Rod Canion, who a year ago helped form Compaq Computer Corp. in Houston.

After a steady year of product engineering, system prototyping, and negotiations for financing, Compaq is now entering yet another critical period as it tries to establish itself as the leader in portable personal computer markets, says the 37-year-old president.

"The next four months are going to be extremely important for us as we gear up the production side of the business," states Canion. The company—which last fall introduced a portable IBM-compatible personal computer [*Electronics*, Nov. 17, 1982, p. 198]—began delivering its first production units in late January.

Compaq officials have grown accustomed to a swift pace. Officially formed in February 1982, the firm first began work on its prototype design about a year ago. During the summer, officials began previewing the unit for prospective dealers and investors. After the fall product introduction, Compaq began hiring production workers. Last month, it had just over 170 employees. By the end of March, Canion expects 250 to be on the payroll.

"That number could double by the end of the year," states the graduate of the University of Houston with an MS in electrical engineering. Prior to starting Compaq, Canion worked for Texas Instruments Inc. for 13 years. TI is now suing the new company, claiming that Canion and his partners began developing the portable unit while working at its Terminals and Peripherals division in Cypress, Texas. Canion emphatically denies the charges, accusing TI of filing a "nuisance suit" to discourage the departure of other employees.

In parallel with Compaq's manufacturing buildup, the firm is testing a wide range of software diskettes being marketed for use in the IBM Personal Computer. Its engineers also are continuing work on future system enhancements and new products. "By the time someone else comes out with a similar portable, we intend to do them one better," Canion adds.

Big days. Rod Canion's new firm is adding workers and facilities even as it strives to develop new products.

RCA Americom's Tietjen to keep its lead in birds

From the viewpoint of satellite-communications companies, "a strong NASA research posture would be in the best interests of the country's effort to cope with foreign competition," says James J. Tietjen, 49, the new president and chief operating officer of RCA American Communications. "U. S. firms do not have a strong history of joint research and development efforts, and I don't see that many in the future."

Tietjen speaks from an R&D background of more than 25 years since receiving his undergraduate degree in chemistry from Iona College of New Rochelle, N. Y., in 1956. After gaining a doctorate in the same field from Pennsylvania State University in 1963, Tietjen began his 20-year

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People

Selling satellite services. To James Tietjen, new RCA Americom head, marketing is key.

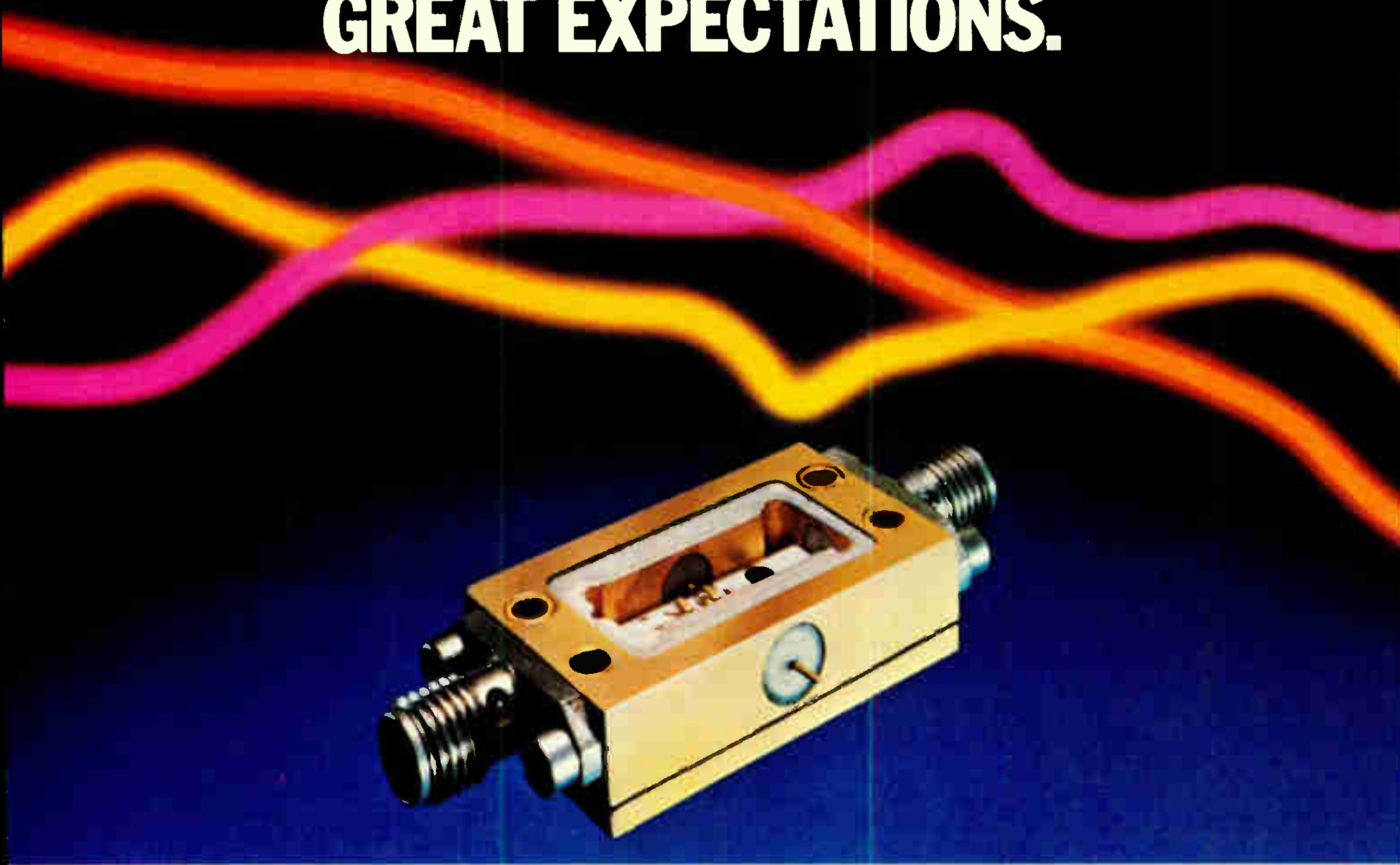
career for RCA—a path of increasing responsibilty, culminating in his directing, as staff vice president of an RCA research division, the effort that produced the RCA VideoDisc.

Under Tietjen's stewardship, RCA Americom will attempt to maintain what he sees as its leadership position in the range of satellite services offered. Access to those services will greatly increase when the company's K-band (10-to-12-gigahertz) satellite system is launched in 1985.

The system, employing 40-watt transponders, offers two advantages over the common C-band (4-to-6-GHz) satellites. "Interference with microwave transmissions is greatly reduced, making the satellite more amenable to TV transmissions," he notes. "Smaller ground antennas can be used with the K band, which dramatically improves the flexibility in the location of ground stations." Antennas, which may be placed on a rooftop, will give satellite access to smaller groups.

Spreading the word about RCA to its potential new customers is one of Tietjen's major challenges. "While we still must develop and take advantage of emerging technologies, the race for the satellite-communications market share is one of marketing, more so than of developing new technologies," says the native of New York. This is not to imply that satellite technology is reaching a plateau, he says. In fact, he is able to foresee the day when satellites may become communications switches in the upper atmosphere. ☐

POWER AND RANGE BEYOND GREAT EXPECTATIONS.



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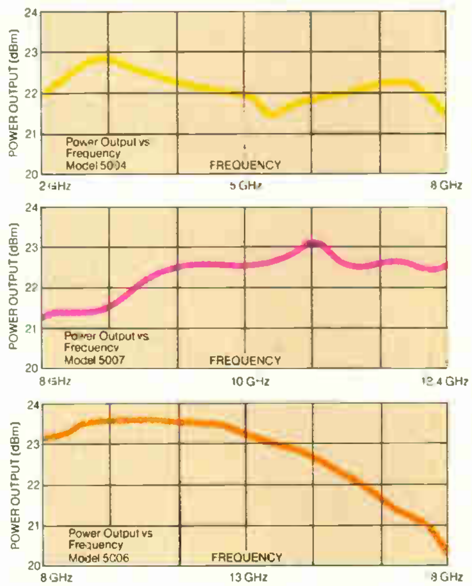

Model 5004. Our lowest frequency amplifier operates over the 2 to 8 GHz band. Power out is $\geq$20 dBm. Gain is 12 dBm min.

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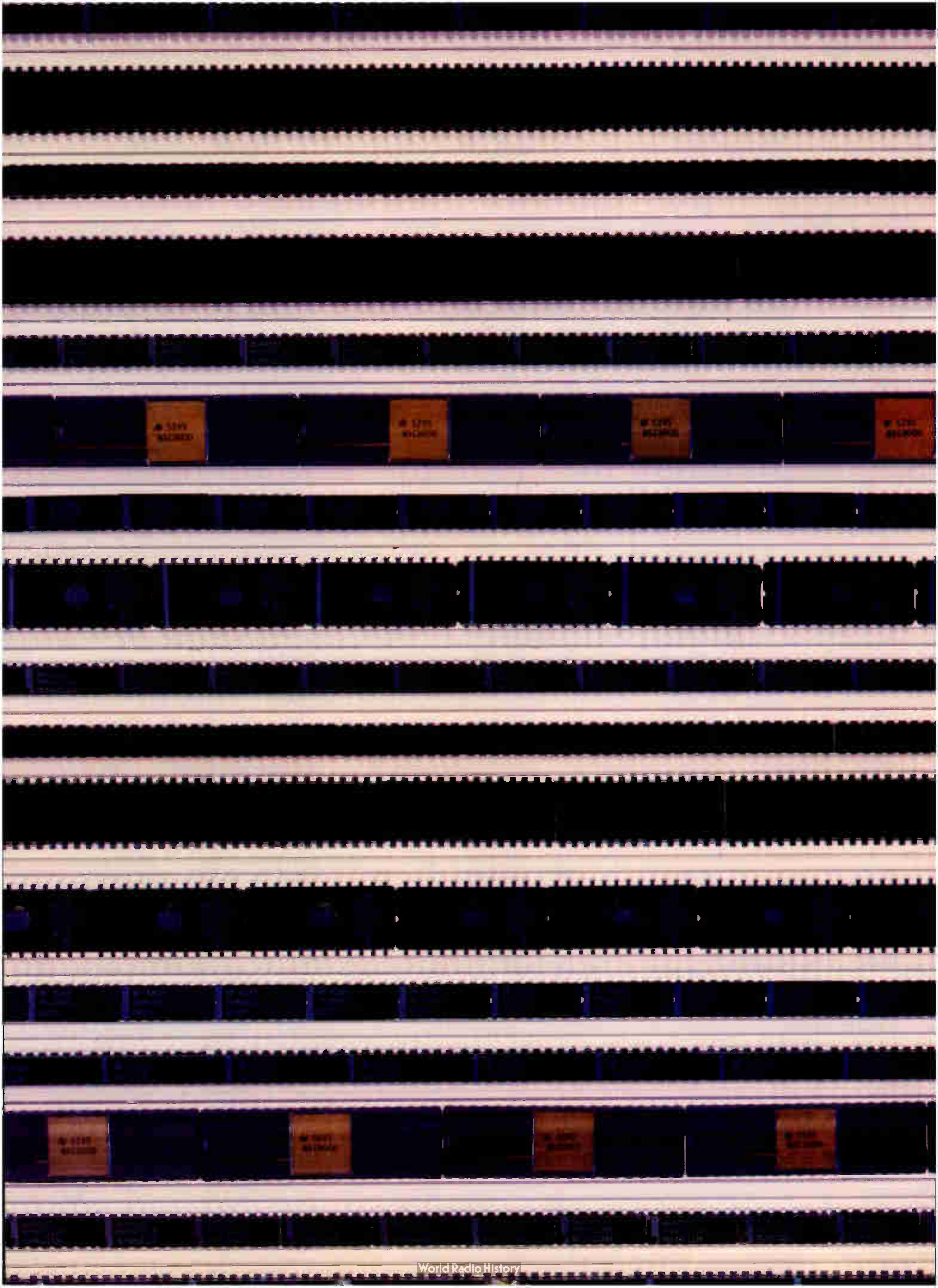

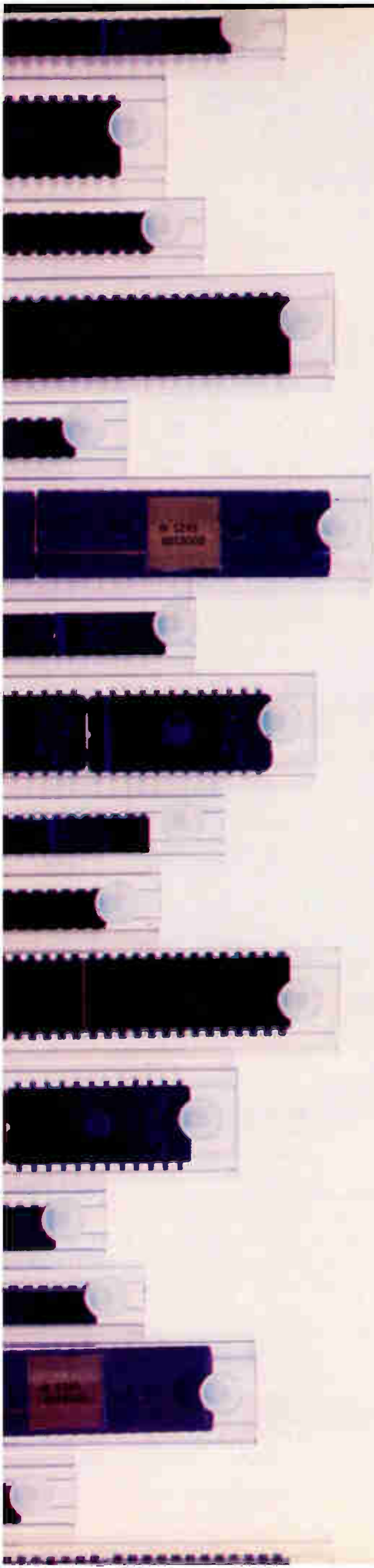

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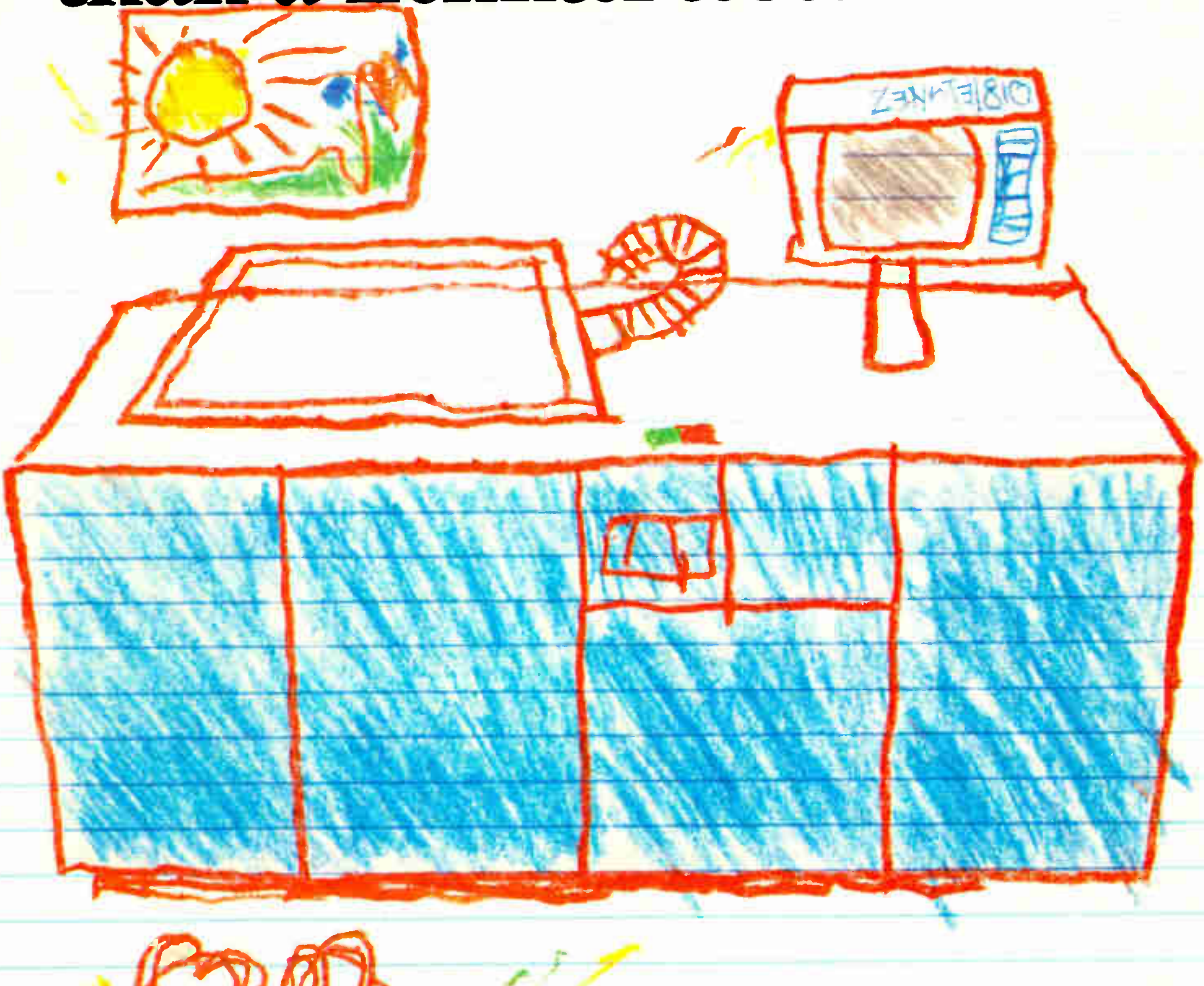

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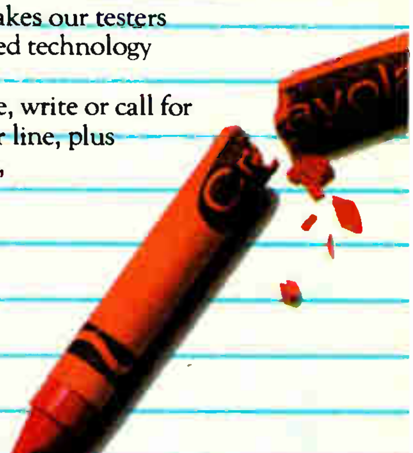

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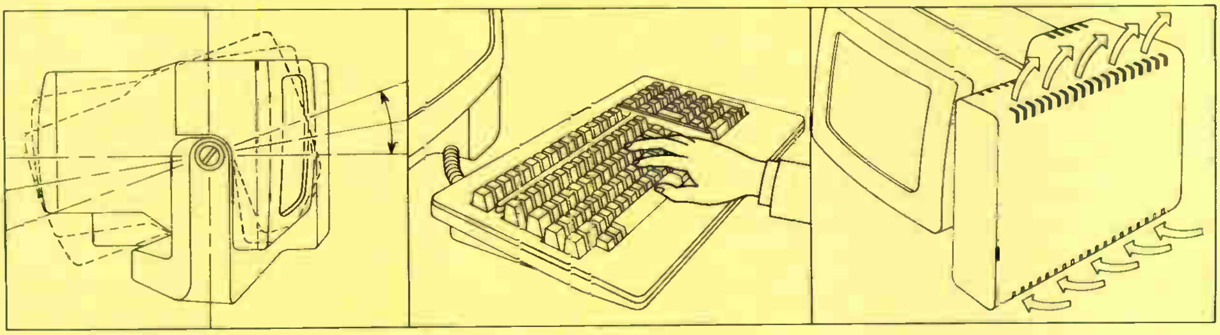

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Circle 23 on reader service card

Protecting trade secrets

by **Marc E. Brown,** *patent attorney practicing in Los Angeles*

Unlike patents and copyrights, virtually anything that gives a business a competitive advantage is potentially entitled to protection as a trade secret. Ideas, processes, methods of doing business, lists of customers, and formulas can all be protected. An additional advantage is the potential ability of trade secret protection to last indefinitely.

Requirements for protection. The key to legal protection is secrecy. To put it simply, perhaps the best policy is: "Don't publish—and keep your mouth shut."

Surprisingly, however, absolute secrecy is often not legally required. Protection has been afforded in the past even though it was shown that a few outside parties were aware of the trade secret. If the information is "generally known or accessible to the trade," however, protection is almost certain be denied.

Lack of general knowledge or accessibility is not the only requirement for trade-secret protection. Reasonable efforts must also be made to maintain the secrecy of the information. Courts do not look kindly on trade-secret lawsuits when the proprietor has taken absolutely no precautionary measures himself to protect the secrecy of the information.

At the very least, security measures should be taken. Access to the trade secret should be carefully limited by the use of safes, alarms, "Authorized Personnel Only" signs, and rigid adherence to procedures carefully designed to prevent unauthorized disclosure.

Contractual restrictions should also be consistently imposed. All employees, contractors, licensees, customers, and others who might come in contact with the trade secret should be bound by written agreements before they are exposed to the trade secret. The agreements should carefully limit their right to disseminate and use the information, especially after termination of their relationship with the trade-secret proprietor. All documentation disclosing the trade secret should also be conspicuously marked "confidential" and should carry clear instructions limiting its dissemination, duplication, and use.

Misappropriation. Trade-secret law protects a trade secret only against its appropriation by "improper means." If the trade secret can be ascertained by inspecting, dissecting, or testing a lawfully obtained product that embodies or was made from the secret (known as "reverse-engineering"), the information so obtained may lawfully be used without the permission of the trade-secret proprietor, assuming that no patent or copyright exists [*Electronics*, Feb. 10, 1982, p. 24; March 10, 1982, p. 24]. Anyone who independently discovers the trade secret, moreover, is also free to use it.

What is prohibited is when the trade secret is obtained by fraud, theft (including electronic espionage), or bribery. It is also unlawful to breach a contract prohibiting disclosure, as well as to induce another bound by such a contract to commit such a breach.

Available relief. Perhaps the most important relief is the right to an injunction—a court order prohibiting further use or dissemination of the trade secret by the wrongdoer. In appropriate cases, the court might also order materials that have been misappropriated to be returned, as well as destruction of unauthorized copies. Compensation for any damages suffered by the trade-secret proprietor can also be obtained, together with any profits that may have been made from unlawful use of the trade secret. Punitive damages in egregious cases might also be awarded.

One of the most important practical requirements for obtaining meaningful relief is to act quickly. If legal action is not instituted until after widespread dissemination of the trade secret has resulted, legal protection against further dissemination or use is likely to be denied. Although the original dissemination was unlawful, the result cannot be undone—the information is no longer a secret and therefeore cannot be protected. The wrongdoer, of course, will be liable for the loss. However, he might not be sufficiently solvent to be able to fully satisfy the judgment, or might disappear, making it difficult even to bring a lawsuit. Moreover, it is often difficult to establish by proof the full amount of damages caused by the loss of the trade secret. In short, the best protection for a trade secret is physical security, not high-powered lawsuits.

This column sets forth basic principles of law and is not intended as a substitute for personal legal advice. Questions and comments are invited and should be sent to Mr. Brown in care of Electronics.


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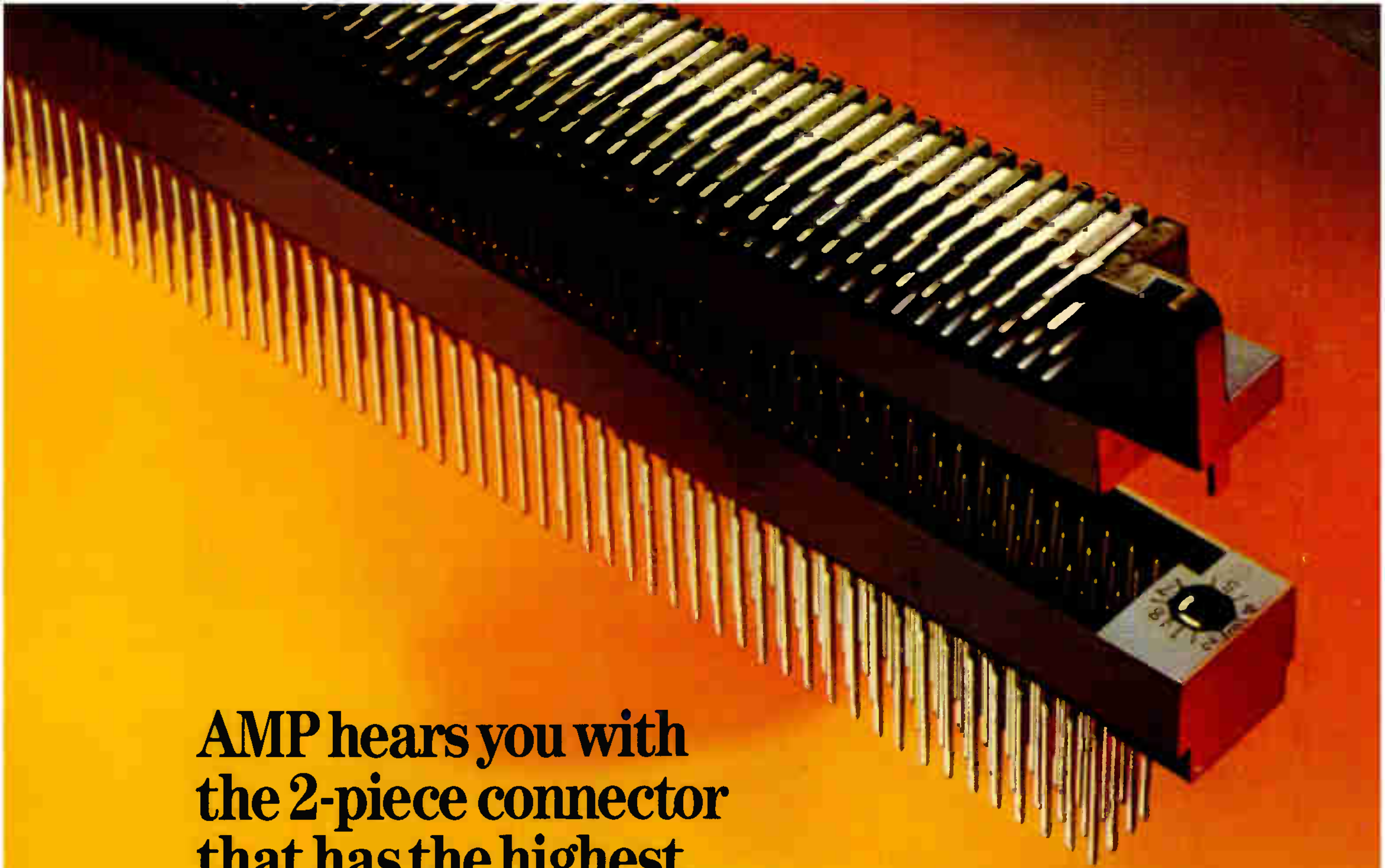

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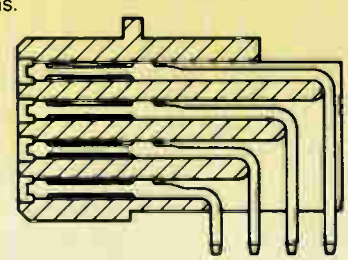

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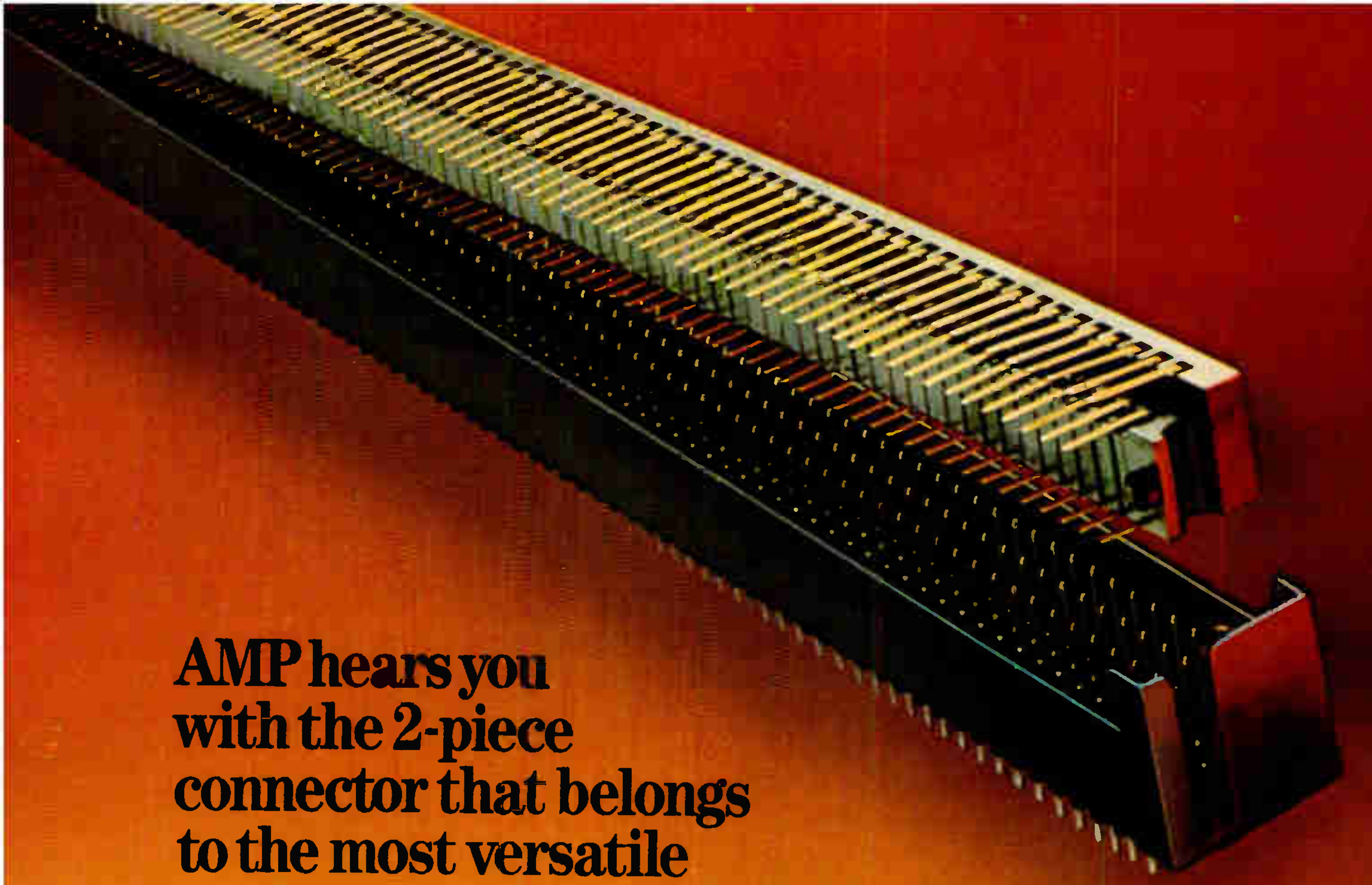
AMP Incorporated, Harrisburg, PA 17105.

Circle 26 on reader service card



AMP hears you with the 2-piece connector that belongs to the most versatile interconnection system.

Anywhere.

Save valuable real estate on your boards. Have the advantage of a 2-piece connector that's part of the interconnection system proved and popular around the world.

The AMPMODU 2-piece connector.

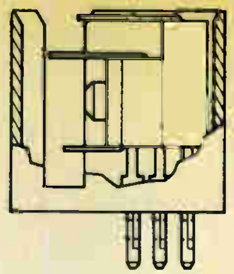
Its 2 and 3 row design accommodates up to 300 positions. Its shortened signal path improves signal performance in your high-speed applications. Receptacle is qualified to Mil-C-55302.

What's more, if your packaging calls for compliant pins and precision plating—it's part of our package.

AMP Facts

Slotted ends of header assemblies for polarization assure easy and sure mating.

Enclosed box design provides perfect post-to-receptacle connections.

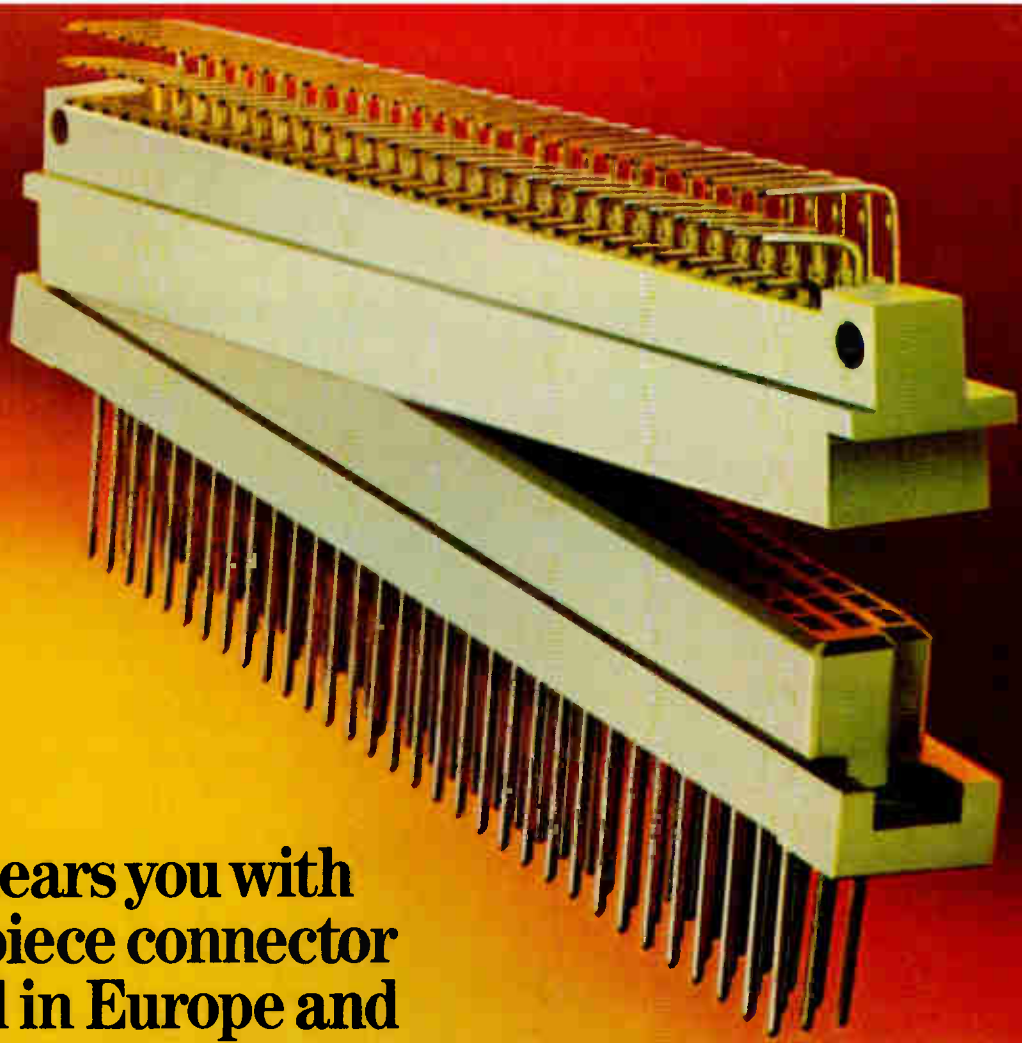


For more information, call the AMPMODU Desk at (717) 780-4400.

AMP Incorporated, Harrisburg, PA 17105.

AMP and AMPMODU are trademarks of AMP Incorporated.

Circle 26 on reader service card



AMP hears you with the 2-piece connector proved in Europe and made in America.

For over 10 years, we've made the standard 2-piece connector in Europe for Europe.

The AMP Eurocard connector.

Now we're making it here to give you the same cost-saving advantages.

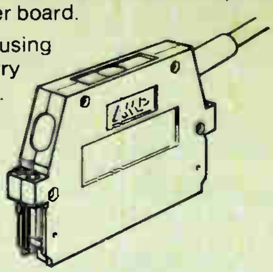
Eurocard comes with or without our selective plating and compliant pins. Offers 2 or 3 row designs that can handle up to 96 positions. Also available in B and C type configurations, this is the economical 2-piece connector with the kind of reliability that gives you more for your money.

AMP Facts

Mates with all DIN connectors of similar type and contacts.

Inverse version allows the use of less expensive pin-half on mother board.

Wire-to-board housing permits cable entry from 3 directions.



For more information, call the AMP Eurocard Connector Desk at (717) 780-4400.
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Circle 26 on reader service card

AMP means productivity.

Meetings

Very Large-Scale Integration Test Workshop, IEEE (Jerry Kunert, Naval Air Engineering Center, Code 92A32, Lakehurst, N. J. 08733), Park Place Casino Hotel, Atlantic City, N. J., March 30–31.

International Symposium on Very Large-Scale Integrated Technology, Systems, and Applications, National Science Council of the Republic of China, IEEE *et al.* (Paul P. Wang, Old Orchard Road, Armonk, N. Y. 10504), Taipei, Taiwan, March 30–April 1.

Technical Symposium East '83, SPIE (The International Society for Optical Engineering, P. O. Box 10, Bellingham, Wash. 98227), Hyatt Regency Crystal City Hotel, Arlington, Va., April 4–8.

International Reliability Physics Symposium, IEEE (David L. Burgess, Hewlett-Packard Co., 1501 Page Mill Rd., Building 28A, Palo Alto, Calif. 94304), Hyatt Regency Phoenix Hotel, Phoenix, Ariz., April 5–7.

Computer Culture: The Scientific, Intellectual and Social Impact of the Computer, The New York Academy of Sciences (Conference Department, The New York Academy of Sciences, 2 East 63rd St., New York, N. Y. 10021), Grand Hyatt Hotel, New York, April 5–8.

Intermag—International Conference on Magnetism, IEEE *et al.* (Ann Marie Pittman, Courtesy Associates Inc., 1629 K St., N. W. Suite 700, Washington, D. C. 20006), Franklin Plaza Hotel, Philadelphia, April 5–8.

International Optical Computing Conference, IEEE (S. Horvitz, P. O. Box 276, Waterford, Conn. 06385), Massachusetts Institute of Technology, Cambridge, Mass., April 6–8.

National Association of Broadcasters Convention (NAB, 1771 N St., N. W., Washington, D. C. 20036), Las Vegas Convention Center, April 10–13.

20th Annual Meeting and Technical Conference, Numerical Control Society (519 Zenith Dr., Glenview, Ill., 60025), Convention Center, Cincinnati, Ohio, April 10–13.

Comunicaciones Expo '83, Latcom Inc. (1200 East St., P. O. Box 860, Westwood, Mass., 02090), Convention Center, Miami Beach, Fla., April 10–13.

Southeastcon '83, IEEE (Russell E. Theisen, Martin Marietta Aerospace, 2667 Fitzhigh Rd., Winter Park, Fla. 32792), Sheraton Twin Towers, Orlando, Fla., April 10–14.

Hanover Fair '83, German Ministry for Research and Technology (Hanover Fair, P. O. Box 338, Whitehouse N. J. 08888), Fairgrounds, Hanover, West Germany, April 13–20.

International Conference on Acoustics, Speech, and Signal Processing, IEEE (Peter Blankenship, Lincoln Laboratory, Lexington, Mass. 02173), Sheraton Hotel, Boston, Mass., April 14–16.

13th International Symposium on Industrial Robots, Society of Manufacturing Engineers (1 SME Drive, P. O. Box 930, Dearborn, Mich. 48128), Conrad Hilton Hotel, Chicago, Mich., April 18–21.

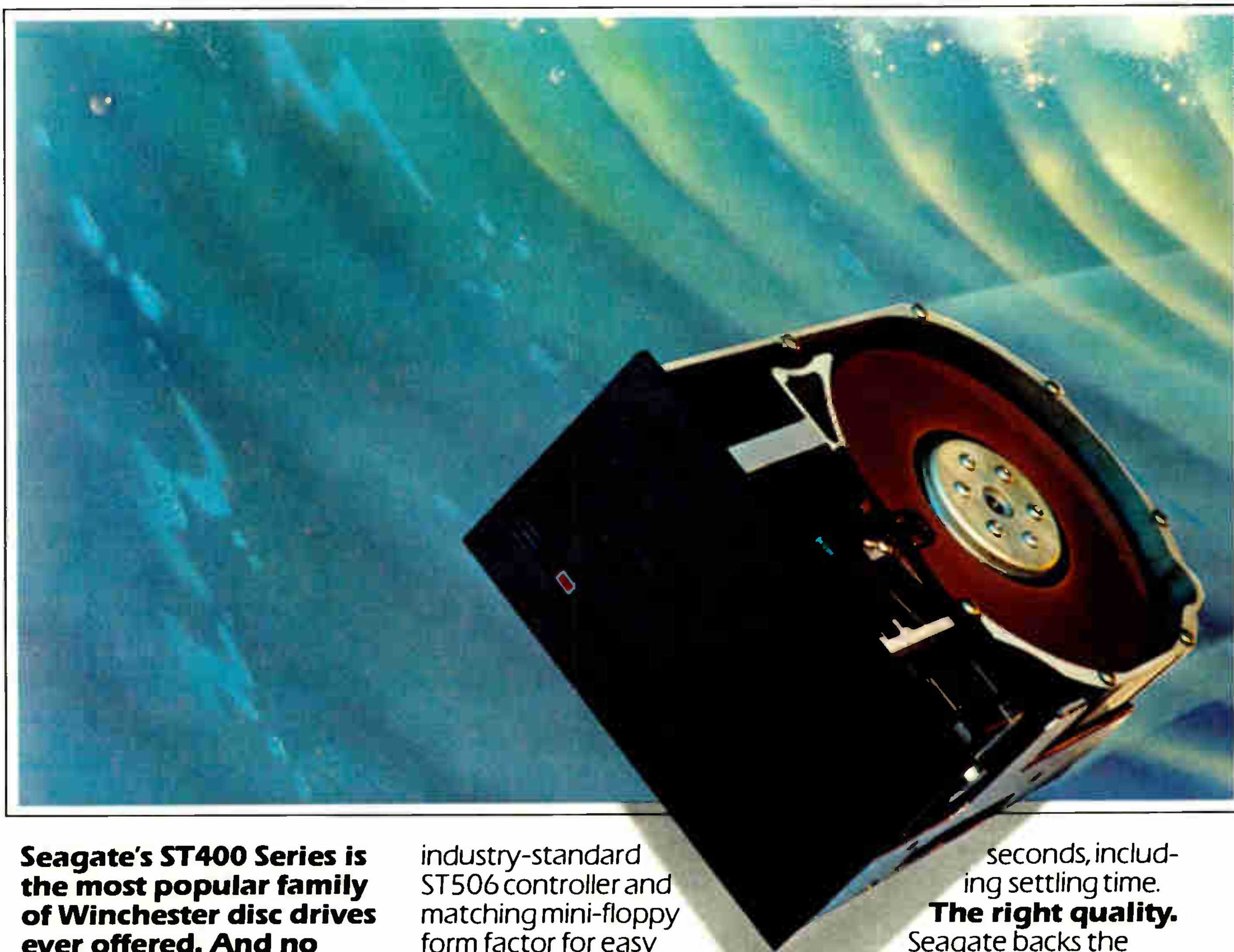
Infocom-83, IEEE (Infocom '83, P. O. Box 639, Silver Spring, Md. 20901), Town and Country Hotel, San Diego, Calif., April 17–22.

Circuit Technology '83, Electronic Components Industry Federation (Slaughter Steadman & Co., 79 High St., Tunbridge Wells, Kent, England), Kensington Exhibition Center, London, April 18–20.

Seminars

Structured VLSI Design, Los Angeles, April 11–13; **X.25 and Other Protocols,** Los Angeles, April 18–20, Washington, D. C., June 8–10; and **Local Data Networks,** Washington, D. C., April 25–27, sponsored by Technology Transfer Institute, 741 10th St., Santa Monica, Calif. 90402; phone (213) 394-8305.

The Seagat



Seagate's ST400 Series is the most popular family of Winchester disc drives ever offered. And no wonder. These 5¼" Winchesters deliver more value for your money. More quality. More reliability. More performance. And all at a better price.

The ST400 Series offers the right capacities. 6.38, 12.76 or 19.14 megabytes (unformatted). All use the same industry-standard ST506 controller and matching mini-floppy form factor for easy upgrade.

The right features.

All use manganese-zinc heads, advanced stepper motor, metal band actuator, open loop head positioner, and patented air flow spindle pump. An onboard microcomputer provides buffered seek and fast step algorithm for an average seek of 85 milliseconds, including settling time.

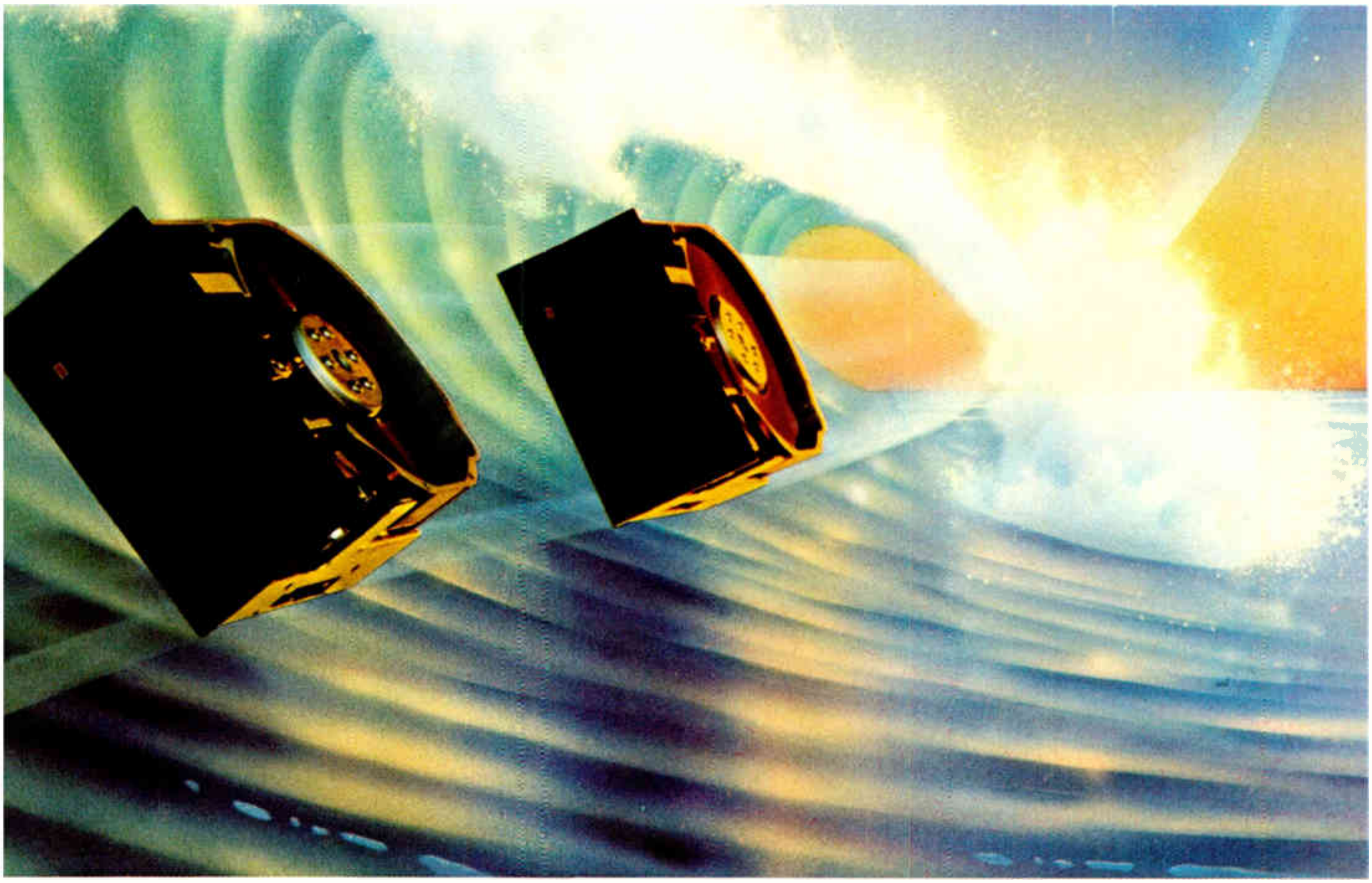
The right quality.

Seagate backs the ST400 family with a full one year warranty, our industry-leading "105% Seagate Guarantee," and the world's biggest support team devoted entirely to 5¼" Winchesters.

Meeting special needs.

Looking for faster, more reliable removable storage? Go with our new ST706

e tide is in.



removable cartridge drive. Need a more compact drive? Pack more data in less room with our new ST206 half-high Winchester. Both new drives store 6.38 megabytes (unformatted) with reliable bit and track densities.

We have what you want in Winchester.

Selection. High volume delivery. Quality. Competitive pricing. So go with the tide. Call Seagate.

The ST400 Series

	ST406	ST412	ST419
Unformatted capacity (MB)	6.38	12.76	19.14
Formatted capacity (MB)	5	10	15
Average access time (ms)	85	85	85

Now Shipping In Volume

Seagate Technology

360 El Pueblo Road, Scotts Valley, California 95066 (408) 438-6550, TELEX 172114 SCVL
Regional Sales Offices: Hopkinton, Massachusetts (617) 435-6961; Newport Beach, California (714) 851-9964; Richardson, Texas (214) 783-6711; Schaumburg, Illinois (312) 397-3727
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Authorized U.S. Distributor: Arrow Electronics

"Turning the tide in disc technology"

Circle 31 on reader service card

News update

■ To nurse a product from concept to final implementation usually takes longer than expected. Such is the case with the railroad-car identification system designed by Identronix Inc. of Santa Cruz, Calif., and marketed by the General Railway Signal Group of General Signal Corp. of Rochester, N. Y. [*Electronics*, March 24, 1982, p. 40]. It has taken a year longer than planned to put together a configuration that U. S. railroads would test, which, according to General Railway, they will soon do.

Called Identifier, the system is built around a complementary-MOS transponder. A microwave signal beamed to the transponder powers it and initiates the reading action of the car's identifying number.

One delay was that the system had to be repackaged to meet the Association of American Railroads' shock and temperature specifications, an unanticipated requirement for the test program. "And we had to design a programmer for encoding a 12-character word that is unique for each railcar-mounted transponder," says George Arena, General Railway's marketing manager. The association wanted to handle the encoding itself instead of relying on transponders supplied already encoded by General Railway.

The programmer is an ac line-powered unit. The code is entered through a keyboard, displayed on a light-emitting-diode readout, then transferred to a programmable read-only memory in the transponder. According to Arena, tests by U. S. railroads will begin "shortly," which is what the company said last year. General Railway also plans to approach the truck and mass-transit bus industries with the system.

Meanwhile, Identronix has found other applications. "With automated factories becoming a reality, the need to track material flow is an ideal application for the system," says Victor Grinich, who is Identronix' president. Both General Motors Corp. and General Electric Co. are now evaluating the system, and Identronix will demonstrate it in April. —**Stephen W. Fields**

The power FET solid state relay. It's a major advance in SSR technology. It provides hybrid and semiconductor reliability. That means years of trouble free operation. That's an important savings, because with a relay your greater expense is not the small difference in the initial purchase price, but rather the high labor costs for replacement.

Because our FET SSR relay is more reliable, it means a savings many times the original price compared to DIP reed relays.

Using power FET technology, Teledyne Relays offers the C46 and C47 solid state relays. They are pin compatible with DIP reed relays. They are also bounce free for low EMI.

We've reduced the ON resistance in the output stage to as little as 3 ohms. Which means that low level signals can be switched with no offset voltage. It also means that these units handle full load currents at higher ambient temperatures.

But the low ON resistance is only one of the features. We've also included buffering so the relay can be driven directly by TTL logic. Optical isolation is used to protect the sensitive input circuits from voltage transients.

And, by use of hybrid micro-electronic techniques, we've been able to package all this capability in a TO-116 DIP.

So it makes sense to start thinking power FET SSR, instead of DIP reed relay.

You'll like them more, because you replace them less.

TELEDYNE RELAYS

The best little relays in the world.

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U.K. Sales Office: Heathrow House, Bath Rd., Cranford, Hounslow, Middlesex, TW 5 9QQ • 01-897-2501
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Japan Sales Office: Nihon, Seimei Akasaka Building • 8-1-19 Akasaka, Minato-Ku Tokyo, 107 Japan (03) 403-8141

Patent number 3,791,025

Circle 33 on reader service card

The New µP-Based Scalar Network Analyzer System.

Running it is as simple as A, B, C, D, E, F!

It's a Wiltron. You're going to make accurate automated measurements far easier using the new Wiltron Series 5600 Automated Scalar Network Analyzer from 10 MHz to 40 GHz. And for less!

You'll discover this 3-element system offers a much better way to measure return loss, transmission loss or gain and power automatically. You'll find the powerful Wiltron Series 5600 features distributed microprocessor architecture and storage of 99 test set-ups.

40 dB Directivity. Series 5600 offers 40 dB directivity over a 10 MHz to 18 GHz continuous sweep range. Dynamic range is 66 dB with −50 dBm sensitivity. The system offers 82 dB attenuation programmable in 0.1 dB steps. ROM corrected frequencies are accurate to +/− 10 MHz from 10 MHz to 18 GHz. Six models span the 10 MHz to 40 GHz range.

The new 6600 Programmable Sweep Generator, a key element. Fundamental oscillators used in the 6600 avoid substantial errors generated by the harmonic products of multiplier type oscillators. The result, low harmonic content, −40 dBc, 2-18.6 GHz, low residual FM and greater stability.

Unpack and you're ready to go. Connect the SWR Autotester and detector, plug-in the factory programmed cartridge, turn on the power, enter a few simple inputs and you're ready to measure. It's all as...

Simple as A, B, C, D, E, F!

A. System Set-up

B. Frequency Selection

C. Calibration Enter ID for device under test. Select averaging of open/...

D. CRT display of characteristics Select marker frequencies and amplitude limits and adjust device under test, if necessary.

E. Measure Press key to start automatic measurement sequence.

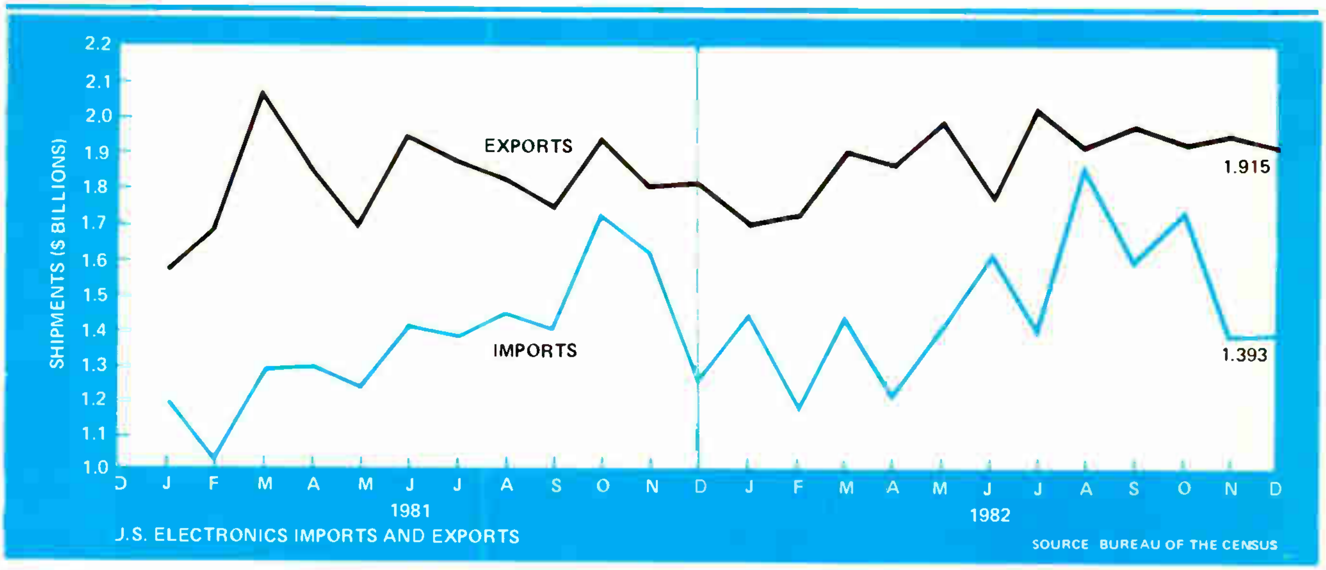
F. Hard-copy output

Ask for an early demonstration, write for 16 page brochure. Call Walt Baxter, (415) 969-6500 or write Wiltron, 805 E. Middlefield Road, Mountain View, CA 94043.

WILTRON

Circle 34 on reader service card

Business activity



U.S. ELECTRONICS IMPORTS AND EXPORTS[1] (MILLIONS OF DOLLARS)

	IMPORTS			EXPORTS		
	Dec. 1982	Nov. 1982	Dec. 1981	Dec. 1982	Nov. 1982	Dec. 1981
Accounting, computing, and data-processing machines	105.153	86.737	64.423	477.216	440.036	452.623
Calculators	22.035	33.942	29.901	7.941	10.362	11.225
Parts for data-processing machines and office calculators	153.277	140.970	101.654	332.162	355.089	323.859
Telecommunications, sound-recording, and sound-reproducing equipment	645.529	697.870	666.695	305.975	314.187	268.600
Electronic or electric instruments	64.843	63.450	64.622	475.022	475.268	414.603
Printed-circuit boards	13.384	20.392	13.610	9.573	10.512	12.380
Integrated circuits, diodes and other semiconductors, tubes, piezoelectric crystals, parts	375.843	326.444	311.677	297.679	336.468	319.639
Fixed and variable resistors	13.206	14.678	14.423	9.701	10.622	11.078

U. S. ELECTRONIC-COMPONENTS PRODUCER PRICE INDEX[2] (1967 = 100)

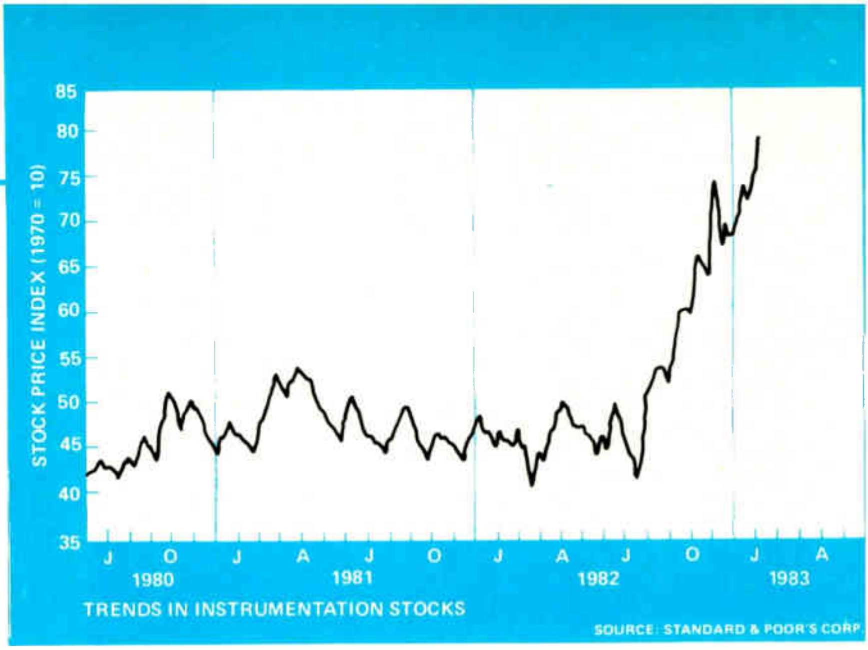
	January 1983	December 1982	January 1982
Digital bipolar integrated circuits	48.6	48.6	51.4
Digital MOS ICs	42.4	43.0	47.7
Linear ICs	58.8	58.7	56.2
Capacitors	192.6	191.8	195.2
Resistors	180.7	180.5	174.4
Relays	232.0	241.9	234.4
Connectors	222.0	221.4	217.2

GENERAL U. S. ECONOMIC INDICATORS

	January 1983	December 1982	January 1982
Average prime rate (%)[3]	11.16	11.50	15.75
Retail sales ($ billions)[4]	91.575	91.482	83.320
Unemployment rate (%)[2]	10.2	10.7	8.4

SOURCES. [1]Bureau of the Census [2]Bureau of Labor Statistics [3]Federal Reserve Board [4]U. S. Department of Commerce

Business activity



The latest economic news emanating from Washington seems to indicate a further strengthening of the nation's economy as spring approaches. In its most recent statement on the subject, the Federal Reserve Board says U. S. industrial production increased a seasonally adjusted 0.9% in January, following a revised 0.1% gain in December. The January increase represented the largest rise in business performance since an adjusted 1.6% gain in February 1982. In addition, the FRB reports that U. S. factories in January operated at 67.8% of capacity. That is half a percentage point higher than December's 67.3%, which was the lowest rate since the FRB started maintaining this statistic in 1948. From the Commerce Department came news that housing starts exhibited their best one-month gain since the Government started keeping tabs on them in 1959, growing 35.9%. As a result, home-building activity reached its highest level since September of 1979. The three indicators add support to the belief that the economy is turning around.

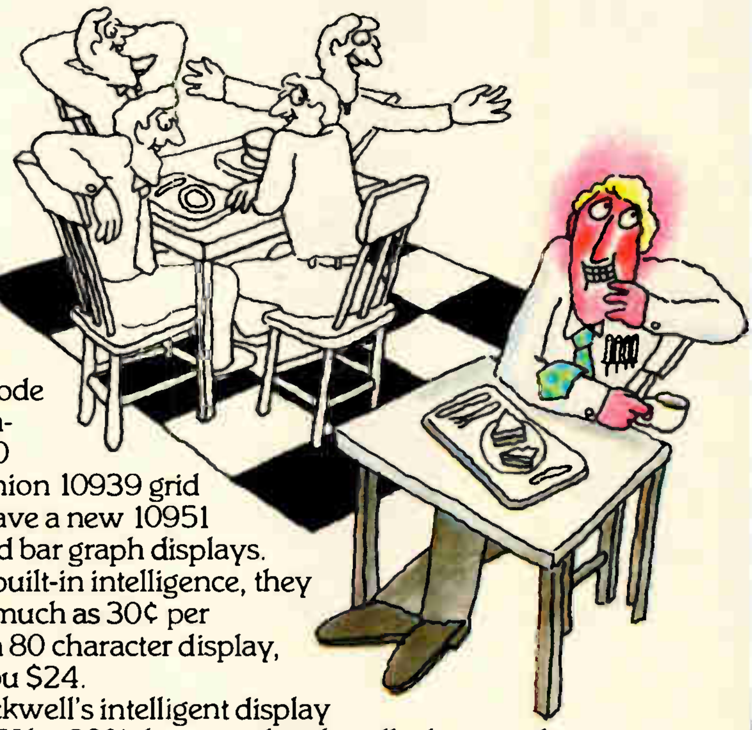
But does this improvement signify a true recovery or just a repeat of the false promise of last spring, when many thought the recession was ending and better times were ahead? According to one industry source, the recovery this time is real. "We're definitely on the upswing," says John O'Boyle, vice president in charge of the Components division of Gnostic Concepts Inc., a Menlo Park, Calif., market-research firm. "This is indeed a real recovery, not a spurt like last year." O'Boyle cites increased order levels in the electronic components area and, more especially, renewed activity on the original-equipment-manufacturing (OEM) front. The economy's apparent revival last year "was more of an inventory adjustment," he says. "There were not a lot of positive signs with it." Though 1982's short-lived upturn came primarily in semiconductors and just a few other areas, "things are really turning around across the board" this year.

Manufacturers are remaining cautious about the near-term outlook, according to O'Boyle, but all the signs point to increased levels of production to meet actual orders, not merely to rebuild inventory. "There are pretty reasonable levels of activity, even in the mundane relay area," the market watcher says. Such items as printed-circuit boards, connectors, capacitors, and resistors are also attracting good orders, he says, adding: "They don't jump without a reason."

Inventories will be watched carefully by all electronic-equipment manufacturers, O'Boyle maintains, not so much because vendors believe high inventory levels necessarily contributed to their recessionary experience, but because high inventories mean high cost due to the fact that capital is still expensive.

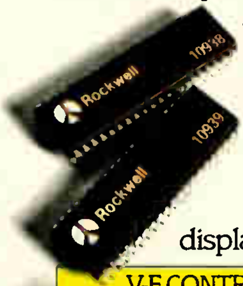
–Robert J. Kozma

"FIRST THINGS SECOND" IS OUR RULE. SOMEBODY BROKE IT.



SO ROCKWELL HAS TO INTRODUCE SIX NEW INTELLIGENT DISPLAY CONTROLLERS. Our rule was already broken when we came up with the 10937, the first single-chip controller for alphanumeric displays. Now the offense has been repeated not once, but six times, to give Rockwell International the leading family of intelligent controllers that directly drive VF displays of up to 60 volts.

Our new 10938, 10941, 10942, and 10943 anode drivers simplify your design job for all sizes of alphanumeric displays, from 8 character segmented to 80 character 5x12 dot matrix. All four, and the companion 10939 grid driver, accept either serial or parallel I/O. We also have a new 10951 single-chip controller for numeric and bar graph displays.



Because all of these devices have built-in intelligence, they lower your hardware costs by as much as 30¢ per character. If your product has an 80 character display, our controllers typically save you $24.

Besides eliminating TTL parts, Rockwell's intelligent display drivers reduce the load on your CPU by 90%, because they handle the complete display refresh function. It's bad enough having these advanced parts for VF displays, but it doesn't stop there. All 7 work with any host processor with just 2 I/O pins through a serial interface.

We've been reluctant to talk about our leadership in display controllers. On the other hand, our distributors will be more than happy to talk about filling your order. Check the chart to get an idea of the best combination for your application, then contact your nearest Rockwell distributor. Or the Electronic Devices Division, Rockwell International, at (800) 422-4230. Or write us at P.O. Box C, MS 501-300, Newport Beach, CA 92660.

V-F CONTROLLER APPLICATIONS

DISPLAY TYPE	SINGLE CHIP DISPLAY CONTROLLER	MULTI-CHIP DISPLAY CONTROLLER	
		ANODE DRIVER TYPE	GRID DRIVER (10939)
8 CHAR. 14-18 SEG.	1 (10937)		
10 CHAR. 14-18 SEG.	1 (10937)		
16 CHAR. 14-18 SEG.	1 (10937)		
20 CHAR. 14-16 SEG.		1 (10941)*	1
32 CHAR. 14-16 SEG.		1 (10941)*	2
40 CHAR. 14-16 SEG.		1 (10941)*	2
20 CHAR. 5x7 MTX		1 (10938)	1
32 CHAR. 5x7 MTX		1 (10938)	2
40 CHAR. 5x7 MTX		1 (10938)	2
40 CHAR. 5x12 MTX		1 each (10942 & 43)	2
80 CHAR. 5x7 MTX		1 (10938)	4
80 CHAR. 5x12 MTX		1 each (10942 & 43)	4
Numeric & Bar Graph	1 (10951)		

*Also Controls Bar Graph Displays.

Rockwell International

...where science gets down to business

Circle 37 on reader service card

Now hear this: You can get super high-quality synthesis of **actual** speech and **natural** sounds in low-cost, low-power CMOS with the new

OKI RealVoice™ Series.

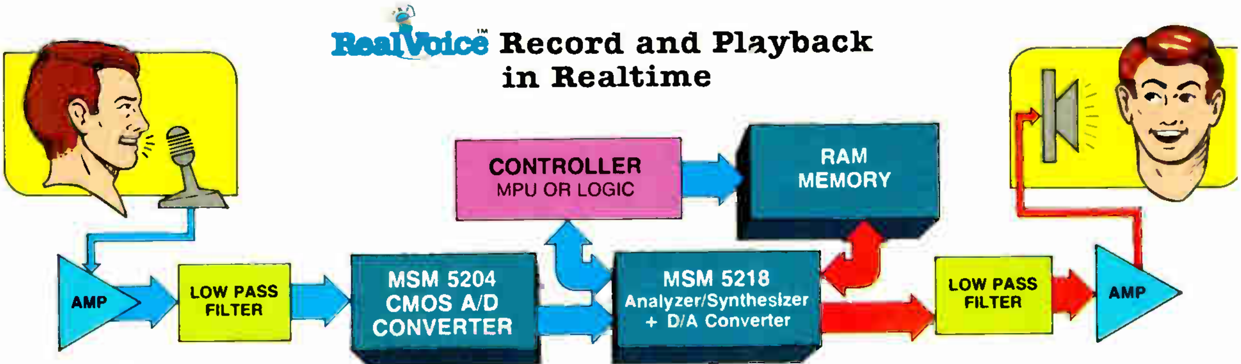
OKI deals in **reality** in speech synthesis! We're setting new standards for quality sound reproduction – now so realistic it's hard to believe it comes from a chip. And so realistically priced and formatted, implementation of the Real-Voice Series is a cinch.

No more stilted computer monotones. We make it easy to record and playback any natural sound. Use **real** voices – man, woman, child, in any language. Use **real** sound effects – bells, sirens, animal cries. Use **real** music – singers, groups, full orchestras.

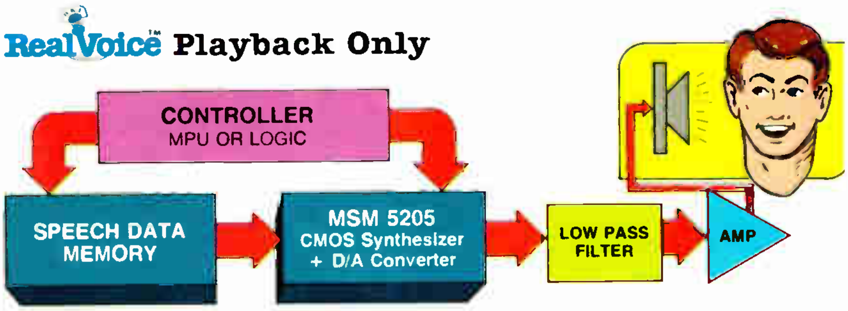
A real voice-synthesis breakthrough. Developed by a company with over 100 years in voice-communication equipment that is also a major source for low-power CMOS/LSI technology. Just the right mix to apply ADPCM **telephone** techniques to **electronic** speech synthesis . . . and come up with a new CMOS family of LSI chips offering complete capabilities in high-fidelity, low-cost sound reproduction.

Ready to go: the MSM5218 analyzer/synthesizer for realtime record and playback. For playback-only systems: the MSM5205 synthesizer – or, in very high-volume applications, our stand-alone MSM6202 or 6212 with on-chip ROM. And OKI's commitment to ease of use has produced optimized demonstration and prototyping tools – our new SAS systems.

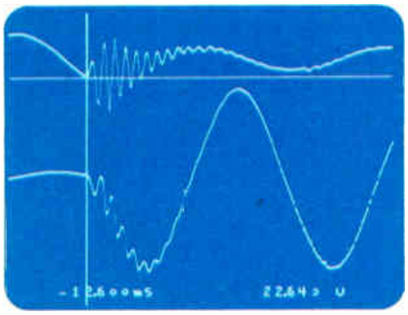
With this strong development support backing up our on-going expansion of CMOS synthesizer options, OKI can offer any designer fast access to Real-Voice system enhancement . . . at the most **realistic** time/capital cost available today.



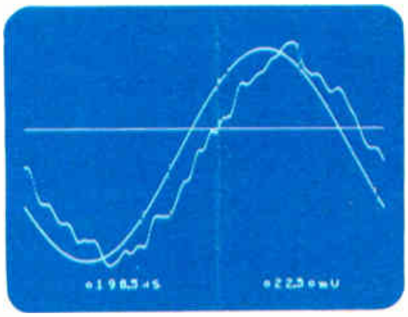
These typical system layouts illustrate Real Voice Synthesis ease of use – characteristics available through OKI's application of Adaptive Differential Pulse Code Modulation. ADPCM processes allow audio waveforms to be digitized and compressed for efficient memory storage. This method of analysis and synthesis offers excellent reproduction of original waveforms by providing easy encoding and playback of natural voices or any other audio source.



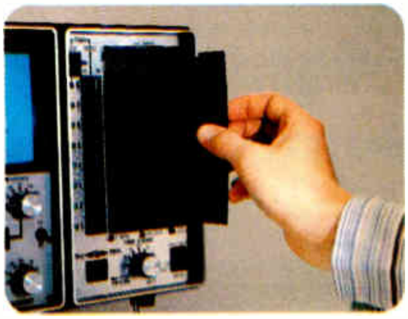
Compare.



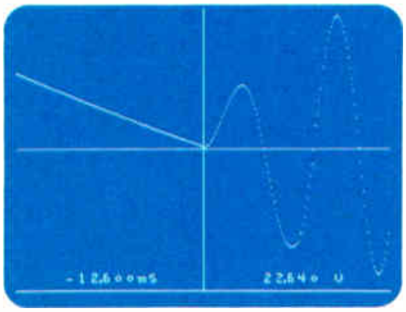
Realtime Monitoring and Storage.
Nicolet Oscilloscopes can monitor, capture, and store signals with both pre- and post-trigger information.



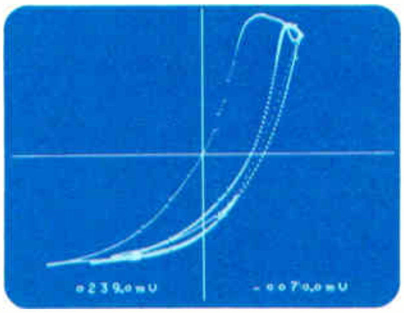
Waveform Comparison.
Nicolet Oscilloscopes can display a live or stored signal with a previously stored reference or a second signal.



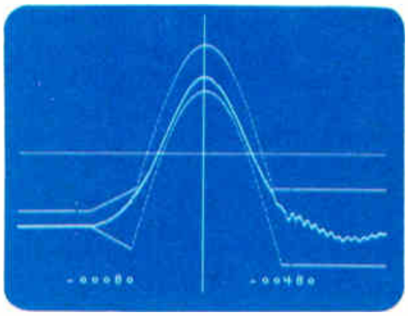
Permanent Storage and Hardcopy Records.
Nicolet Oscilloscopes can store waveforms permanently on a built-in floppy disk for later recall and/or output to an external plotter.



Expansion, Resolution and Accuracy.
Nicolet Oscilloscopes can expand any selected feature up to X256 with resolution up to 0.002% and accuracy as high as 0.2%.



X/Y Display.
Nicolet Oscilloscopes can display a waveform as a function of another, either in live or stored mode.



Digital Interfaces.
Nicolet Oscilloscopes can interact with computers or calculators. (In this case, comparing a live waveform to computer-drawn limits.)

Compare these features with any other oscilloscope.

The choice should be obvious.

For more information on the 2090 Series or the more powerful 4094, call 608/271-3333. Or write Nicolet Instrument Corporation, Oscilloscope Division, 5225 Verona Road, Madison, Wisconsin 53711.

NICOLET INSTRUMENT CORPORATION
OSCILLOSCOPE DIVISION

Nicolet *Digital* Oscilloscopes

Circle 40 For IMMEDIATE NEED

Circle 41 For LITERATURE ONLY

Electronics newsletter

Tandy slates trio of new computers and rehires Lenninger

Responding to the flood of personal computers that has been loosed in the past few months, Tandy Corp. is preparing to introduce three models in its popular Radio Shack line. What's more, the Fort Worth, Texas, company **is bringing back Steve Lenninger, designer of the TRS-80 model 1,** as director of advanced product development. Lenninger, who started a consulting business when he left Tandy, will preside over the introduction of several machines. They include a South Korean–built replacement for the Color Computer, a model 100 portable designed to be Tandy's answer to the Epson HX-20, and a model 4 sporting a built-in hard-disk interface as well as 128-K bytes of random-access memory.

Japanese computer threat is overrated, says research firm

Fears of Japanese domination of the computer industry are vastly exaggerated, according to a report due later this month from Venture Development Corp., Wellesley, Mass. In fact, the report, entitled "The Japanese Computer Industry: Strategic Analysis," concludes that U. S. firms are strongly positioned to resist Japanese incursions in the minicomputer, small-business–computer, and personal-computer markets. **Only at the extreme low end of the market, with handheld models, are the Japanese capable of overwhelming U. S. competitors,** notes Timothy F. McMahon, manager of the company's Computer Group and author of the study.

10-Mb data-transfer rate sought for 5¼-in. disks

Hoping that an informal committee of disk-drive and controller manufacturers can agree this month on a high-speed data-transfer interface, at least two manufacturers of high-capacity 5¼-in. Winchester disk drives are ready to announce products in the range of 300 megabytes or over. Led by the Maxtor Corp., a new Santa Clara, Calif., company, more than 20 manufacturers both of drives and controllers have already met three times to discuss a 10-Mb/s interface **that would double the transfer rate of the present *de facto* ST506 standard.** A vote on the proposed new standard, called the Enhanced Small-Disk Interface (ESDI) is scheduled for March 17.

NCR computer is first in new 32-bit family

Look for NCR Corp. to unveil a medium-sized business computer next week that will be the first in a new family to employ the NCR/32 processor chip set brought out last fall [*Electronics,* Sept. 8, 1982, p. 47]. To be known as the NCR 9300, the desktop, four-board, 32-bit system is expected to be software-compatible with current NCR I-Series computers, such as the I-9040, **while achieving a 10 : 1 improvement in power consumption and reliability,** a 7 : 1 reduction in size, and as much as a fourfold improvement in the cost-performance ratio.

TI slips into high-speed C-MOS

Falling in line with nearly a half dozen makers of complementary-MOS circuits, Texas Instruments Inc. has quietly begun shipments of its first high-speed C-MOS logic components. TI's initial HC-MOS logic devices will eventually grow into an extensive family of commercial and military parts, duplicating the company's current bipolar 54/74 product lines. The Dallas-based firm—which during the past decade has established a huge volume business in Schottky TTL—is expected to unveil its HC-MOS logic strategy within the next month. At that time, it will map out plans to complement its exisiting bipolar logic offerings with the low-power HC-MOS series. Made from TI's p-well silicon-gate process, **the new logic parts will be compatible with the growing number of HC-MOS chips now hitting the market.** The new family will include the full range of standard small- and medium-scale integrated logic components as well as a number of advanced-function parts.

TRW drops out of Fujitsu venture

TRW Inc. is dropping out of its highly publicized joint venture with Fujitsu Ltd. formed in 1980 to sell small-business computers and other equipment in the U. S. The Los Angeles–based TRW-Fujitsu Co.'s intent was to merge Japanese hardware and manufacturing skills with the U. S. company's marketing and maintenance organizations. TRW gave no reason for quitting the partnership, but sources say **delays in developing new machines, the recession, and difficulty in coordinating management all played a part.** Fujitsu is said to be planning to continue on its own through its U. S. subsidary.

17% to 18% efficiency claimed for solar cells

A Rockville, Md., maker of solar cells claims that it has achieved 17% to 18% efficiency with semicrystalline silicon. **This efficiency compares with 10% for thin-film amorphous-silicon techniques and is equal to the best figure attained by single-crystal silicon cells,** says Zim Putney, president of the company, Semix. He says the proprietary process—called Split for simultaneously present large-impurities technology—refines metallurgical-grade silicon before casting it into cubes 20 cm on a side. The cubes are then sliced into wafers 0.010 to 0.015 in. thick.

GM to supply Isuzu with engine controls

For the first time, General Motors Corp.'s Delco Electronics division will supply electronic engine controls for non-GM cars. The Kokomo, Ind., division will supply Isuzu Motors Ltd., Kawasaki, Japan, with 40,000 units in the first year and 200,000 annually in subsequent years for use in Isuzu's new "R" cars. Calling the contract a major milestone, a Delco spokesman says the Isuzu deal is **the first to come out of a push begun by Delco about a year ago to market automotive electronics products to outside customers.** Isuzu is partially owned by GM, which imports some of its models for sale in Buick dealerships. Negotiations with other auto makers are under way, Delco says.

Addenda

Hot on the heels of Apple Computer's announcement of the Apple IIe, **add-on products are starting to emerge.** The first out of the gate is the Premium Softcard IIe from Microsoft Corp., Bellevue, Wash. The video-controller card contains a Z80 microprocessor, 64-K bytes of random-access memory, and an 80-character display generator. . . . International Business Machines Corp. plans a product announcement shortly, but it will not be the new low-end personal computer that industry insiders believe it is readying for market. Instead, IBM is **expected to unveil enhancements for its Personal Computer including increased memory, a 5¼-in. 12-megabyte disk drive** from Seagate Technology of Scotts Valley, Calif., and an optional color monitor. . . . Data General Corp.'s new MV-10000 minicomputer **can be linked to an Ethernet or IEEE 802 local network** using a board from Interlan Inc. of Westford, Mass.

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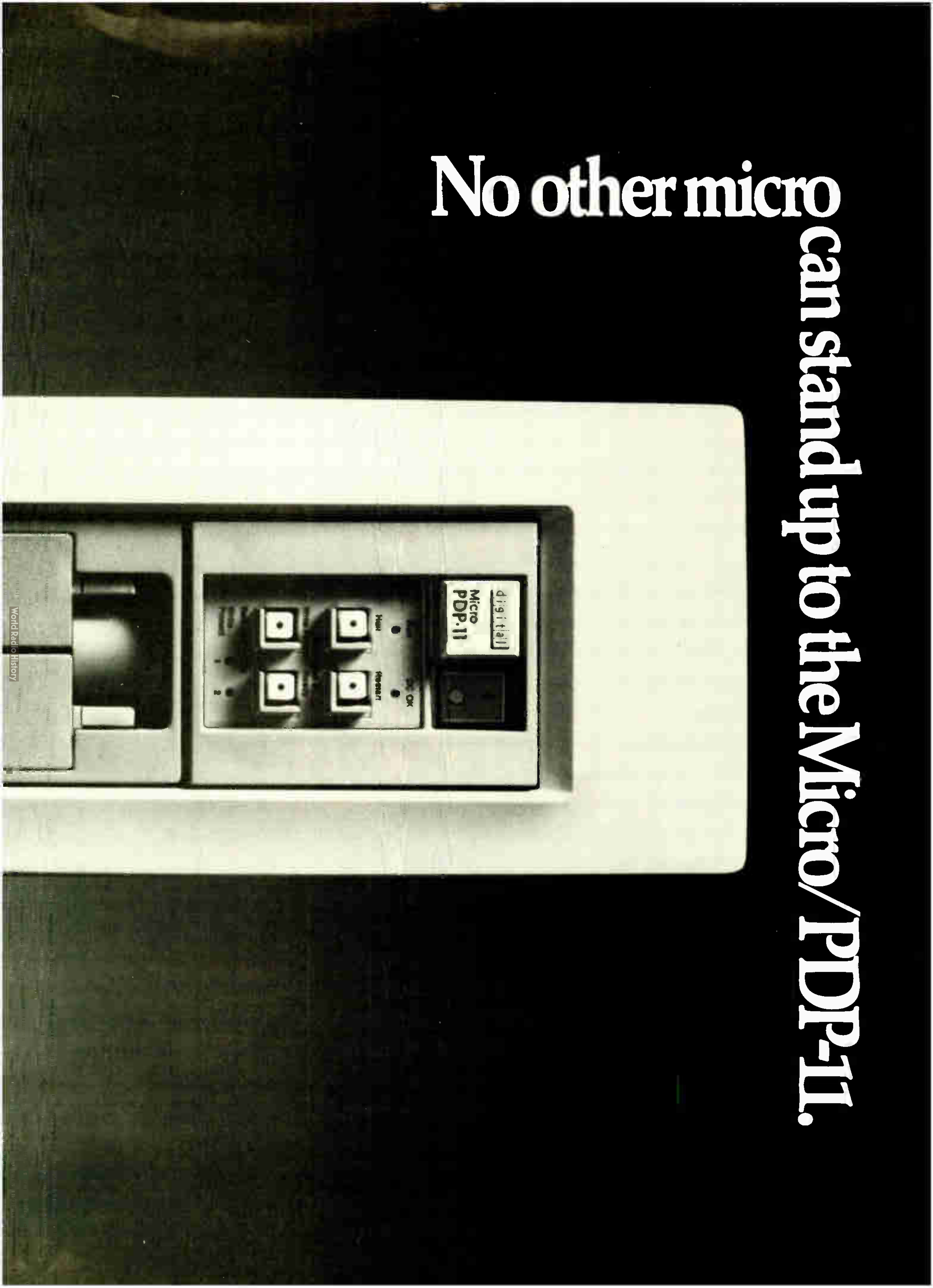
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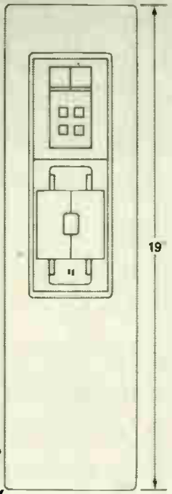

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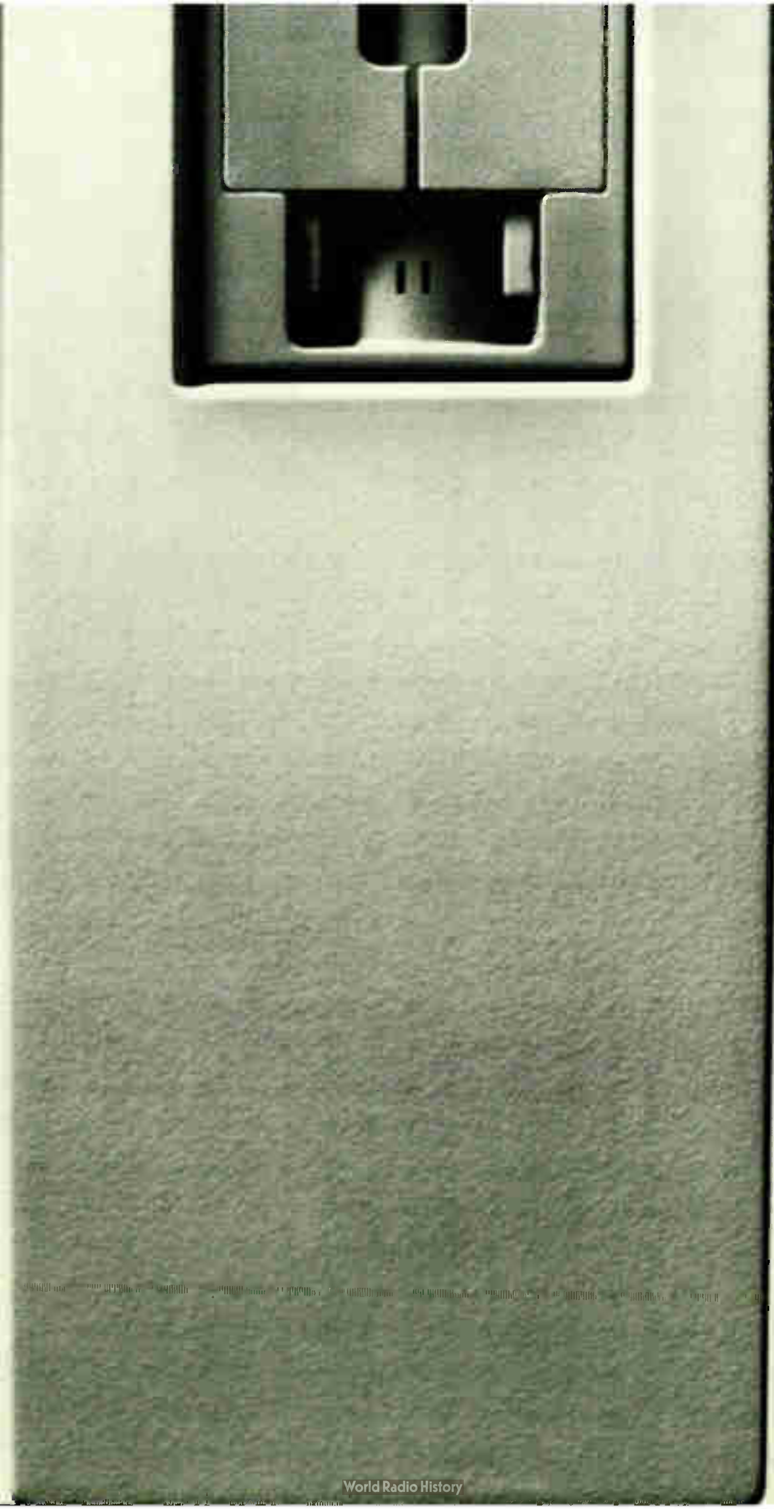

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Pacemakers pick up performance with custom C-MOS chips

by J. Robert Lineback, Dallas bureau

Specially designed processors enable the units to offer more sophisticated pacing possibilities and longer life

Two makers of implanted heart pacemakers are turning to custom microcomputer designs in an effort to boost performance of their newest programmable pacer systems and to lengthen battery life. The desire is "to make 'smarter' units that last much longer," says Stanley H. Saulson, vice president of engineering at Cordis Corp., Miami, Fla.

Cordis last month became the first American manufacturer to receive approval from the U. S. Food and Drug Administration to market commercially a programmable pacemaker based on a custom microcomputer chip. In 1980, it was also the first to market a pacemaker built with an off-the-shelf microprocessor, the 8-bit complementary-MOS RCA 1802.

The goal is to reduce the risk of life-threatening failures while doing a better job of implementing a sophisticated pacing scheme like dual-sensing, dual-pulsing, demand pacing. In DDD pacing, the unit essentially acts as two pacemakers, sensing and pulsing the two major chambers of the heart, the auricle and ventricle. As a demand pacemaker, the unit would intervene only when it recognized an abnormal heartbeat by sensing the electric potential in the heart muscle that occurs just before contraction.

Cordis's upgraded pacemaker, the Sequicore II, substitutes a 4-bit custom C-MOS chip for the 8-bit 1802. The new chip, developed with Intersil Inc. of Cupertino, Calif., also integrates circuits that had been on five other chips, so that current drain goes from 60 microamperes down to 10 μA. Battery life is affected dramatically, rising to between 6 and 10 years under worst-case operating conditions, says Saulson, whereas the earlier model, which included a separate 2-K-by-8-bit read-only memory, ran for only about two years. Only minor surgery is required to replace batteries in implanted pacemakers.

Link. The 4-bit chip, measuring some 190 mils on a side, is slated also for Cordis's still newer pacemaker, Gemini. Its circuits include sensing amplifiers, voltage couplers, output stages, ROM, random-access memory, and a receiver-transmitter link used to check the pacemaker and change pacing parameters from outside the chest cavity. According to Saulson, Cordis can offer more combinations of sensing and pulsing settings with its 4-bit microprocessor than with the 8-bit one.

Gemini, already in clinical testing, offers a still greater number of settings than the upgraded Sequicore II, which needed less testing time before coming to market.

Also with a custom-chip pacemaker in clinical testing is Intermedics Inc., Freeport, Texas. Its Cosmos pacer relies on an 8-bit chip and compiles data on heart performance for the physician. Designed and produced by custom-chip maker Zymos of Santa Clara, Calif., in which Intermedics owns a majority interest, the C-MOS chip is code-named Lazarus and measures 225 mils on a side. It sends information from its RAM that includes such data as the number of times each side of the heart works on its own or must be paced. "This gives the physician diagnostic information that until now has generally not been available," notes Richard V. Calfee, Intermedics vice president of engineering.

Cosmos—like other microcomputer-based systems—can be reprogrammed by a physician who downloads software from outside the chest via a hand-held programmer. Pulse-position–modulated binary-coded data is transmitted over the communications link, which includes "a lot of redundant transmission and error checking," says Calfee. Doctors

Pacer. Built around a custom 8-bit microcomputer, Intermedics' Cosmos pacemaker can store diagnostic data for the physician that has generally not been available.

can adjust such things as heart rhythm, pulsing relationships between the major heart chambers, sensing levels, gain of amplifiers, and output signal strengths.

Intermedics has also developed an 8-bit desktop computer, which maintains patient history and billing records. Further, software in an on-chip ROM allows Intermedics to change the algorithms of the microcomputer to tailor it for other implantable medical systems. For example, the same chip is now being used in a programmable drug-delivery system under development.

Both Intermedics and Cordis have loaded their chips with hardware and software redundancy aimed at recognizing and averting a number of system failures long associated with DDD pacing. For example, a pacer can get stuck in an endless loop by sensing its own pulsing signals, causing the heart to race—a dangerous condition known as tachycardia. Cosmos also has a redundant self-checking scheme that turns pacing duties over to a second smaller custom chip if the main one fails. But the new features are costly: the price of the new units is boosted to the $5,000 range from around $2,000.

Distributors

Wyle takes on semicustom lines

The technical aid and hand holding that is part of bringing a semicustom integrated circuit from idea to product is gaining a new sales outlet: the friendly neighborhood distributor. Wyle Distribution Group, a medium-sized distributor headquartered in Irvine, Calif., with sales in 1982 of $160 million, has taken on exclusive representation of NCR Corp.'s line of n-channel and complementary-MOS standard-cell parts.

"Semicustom ICs will be half of the semiconductor business by 1990. Distributors are going to have to figure out a way to fit in," says Wyle president Charles M. Clough. The hard-driving Clough, 53, who came to Wyle last August after 27 years at Texas Instruments Inc., most recently in TI's top marketing post [*Electronics*, Nov. 17, 1982, p. 14], thinks coming out of the gate early gives his firm a big edge.

In NCR's view, the deal with Wyle provides a broader exposure for its semicustom line, as well as its standard IC products, in the 11 Western states served by the distributor from nine stocking locations. Having entered the merchant semiconductor market late, in mid-1981, NCR has no outside sales force and has depended largely on some 21 sales representative firms.

Wider vistas. "This is a big step for us," says James H. Van Tassel, vice president of NCR's Microelectronics division in Dayton, Ohio. NCR is currently negotiating with other semiconductor distributors for similar deals, he says. "We want to be across the country by year-end."

That expansion, however, will wait until the arrangement with Wyle is running smoothly, he notes. The bedrock problem to be solved is how to train combination design and sales engineers to carry a customer from specifications to a working device.

First comes the training of Wyle's engineers to identify potential customers for semicustom designs and, next, classes in applying NCR's 4-micrometer C-MOS and n-channel MOS standard-cell libraries. "It's going to take six months of good hard work with Wyle to get us where we want to be," estimates Van Tassel.

Wyle will not need to buy special computer-aided design equipment, he believes, for NCR's CAD tools for accessing circuit cells or modules from a library and arranging them to suit a customer's specs are available on the computer time-sharing network of Cybernet Services, the Control Data Corp. subsidiary. Only a standard terminal and printer are needed to access the library.

Wyle is to sell the NCR products through its Computer Products division, which handles minicomputers, processor boards, and peripherals. It is already staffed by sales engineers and computer scientists with qualifications akin to those of the technical staffs of electronics firms.

In addition, Wyle brings along a wide customer base in areas of prime possibilities. "Any customer buying 150,000 TTL gates a month has potential for stepping up to a semicustom device," says Clough. He points out, too, that Wyle will act as a buffer between customers and NCR, holding devices in inventory after a fabrication run and selling them in monthly allotments. Profit margins—at 40% to 45%—will be double the usual figures, a reflection of the complex selling required.

Skepticism. Certainly, whether Wyle engineers can mesh smoothly with customer and NCR types must be demonstrated—a question, in fact, that stirs most industry skepticism. Alfred J. Stein, chief executive at silicon foundry VLSI Technology Inc., Santa Clara, Calif., which builds semicustom devices, voices a representative *caveat*: "I'm just not sure how a distributor fits into a heavy engineering interface."

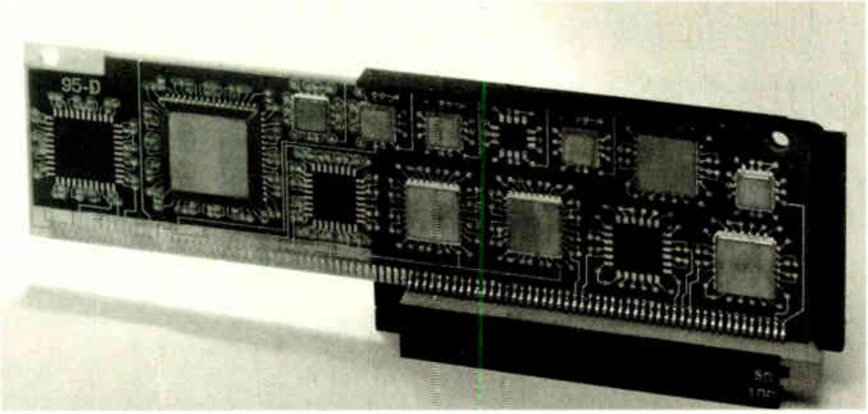
The Wyle move is certain to get close distributor scrutiny. For one, Hamilton/Avnet, the giant distributor in Culver City, Calif., decided to pass it up, says William C. Cacciatore, executive vice president of worldwide operations. He concludes that semicustom demand can be satisfied with off-the-shelf parts.

However, Motorola Semiconductor Sector, Phoenix, a big Hamilton vendor, is considering offering through distributors its line of Macrocell gate arrays, which many feel bridges the gap between standard and semicustom products. Should this happen, Cacciatore may well change his opinion. **–Larry Waller and Wesley R. Iversen**

Packaging

Chip-carrier TCE finds its match

The addition of a few thin metal layers has yielded epoxy-glass printed-circuit boards whose temperature coefficient of expansion comes close to matching that of ceramic leadless



Success. This 5.5-by-2-in. metal-layered pc board was thermally tested with various leadless ceramic chip-carriers, whose temperature coefficient of expansion it closely matches.

chip-carriers. Thus, the possibility exists that basically simple boards and common pc techniques could be used to make boards for these carriers, which are so popular with the military, say engineers at General Electric Co.'s Ordnance Systems department, Pittsfield, Mass.

To reduce the epoxy-glass board's normal expansion coefficient of 15 to 18 parts per million per °C to that of the carriers' 5 to 7 ppm/°C, two 5-mil-thick layers of either copper-plated Alloy 42 steel or a copper-Invar-copper sandwich are added to a conventional four-layer pc board. These extra metal layers not only act as expansion compensators but, according to GE, have the added attraction of also serving as ground and power planes.

Thermal cycling tests with the copper-Invar-copper samples demonstrate that the boards can withstand 1,500 cycles with no solder-joint failures at the soldering pads where the leadless chip-carriers are attached, according to the developers.

Other ways. "Previous to this design, other approaches to matching the ceramic's tempco either involved using a thick metal core of 25 to 30 mils as strictly a structural member, or the use of extremely expensive laminates such as Kevlar polyimide or quartz polyimide," notes James Hauser, electronic product design engineer at the Ordnance division.

Another method covers each board with a shock-absorbing elastomeric layer. "The GE approach not only uses the two metal layers electrically but, overall, the multilayer is only 40 mils thick," he adds. "And no special processing is required."

Preliminary work at GE showed 10 mils of Alloy 42 with 2 mils of copper plating plus 30 mils of epoxy glass would have a composite expansion coefficient of 7 to 8 ppm/°C. Actual samples checked out to within 10% of the values that had been predicted.

To check their findings, Hauser's group built 33 six-layer samples each consisting of four circuit layers plus power and ground planes made of 5-mil-thick Alloy 42. The top layer accommodated leadless ceramic chip-carriers with 14, 24, 32, 44, and 64 terminals that were vapor-phase–soldered to the board. Thermal tests covered a range of –55° to +125°C.

The 64-terminal devices failed after 300 and 400 cycles, while the other types suffered their first solder-joint failures after 800 to 900 cycles—an acceptable level. A redesign of the surface of the metal layers pushed the failure point for 64-terminal carriers out to 900 cycles. During this test there were no failures.

In later tests, two 5-mil-thick copper-Invar-copper sandwiches, whose measured tempco was between 5 and 6 ppm/°C, replaced the Alloy 42 layers. Three six-layer samples using the same board pattern as the earlier samples were thermally cycled over the same temperature extremes. The carriers' solder joints withstood 1,500 cycles.

Hauser has already designed a functional module using the copper-Invar-copper substrate. GE plans to evaluate the method for modules for the Trident missile. –**Jerry Lyman**

Local networks

Files appear local on Unix network

Now that local networks make it easy to distribute processing power and data storage, system houses are finding new solutions to the problem of how to access a remote file. What is called a fully distributed system overcomes some of the drawbacks associated with traditional methods, and Plexus Computers Inc., Santa Clara, Calif., is bringing such a system to market for its network of superminicomputers.

The Plexus network relies on the high-speed version (12.5-megahertz clock) of the Motorola 68000 16-bit microprocessor. Its distributed file system avoids some of the usual shortcomings either of duplicating data—by copying files from one local node to another—or of centralizing it and making a single machine a master file server for all nodes. The system is simpler to use because a file may be accessed at any node, and all data appears to be locally available. Moreover, data is not stored in a central place, where a failure could bring the entire net down, nor do different versions of files develop out of multiple copies, for there is only one copy of a file.

Adaptation. Plexus has adapted the hierarchical structure of Bell Laboratories' Unix operating system to implement its distributed file system. Because each file in the Plexus system has a unique name, the user need not know where a file is located. Unix files are organized in logical trees that branch out from a "root" directory that encompasses all files in the system. Each logical level has a directory listing all the levels beneath it; a file is identified by a series of names, called a pathname, that trace the relationship of the file to the directories logically above it. A

Unix command, "mount," will attach a branch of one tree to the root of another.

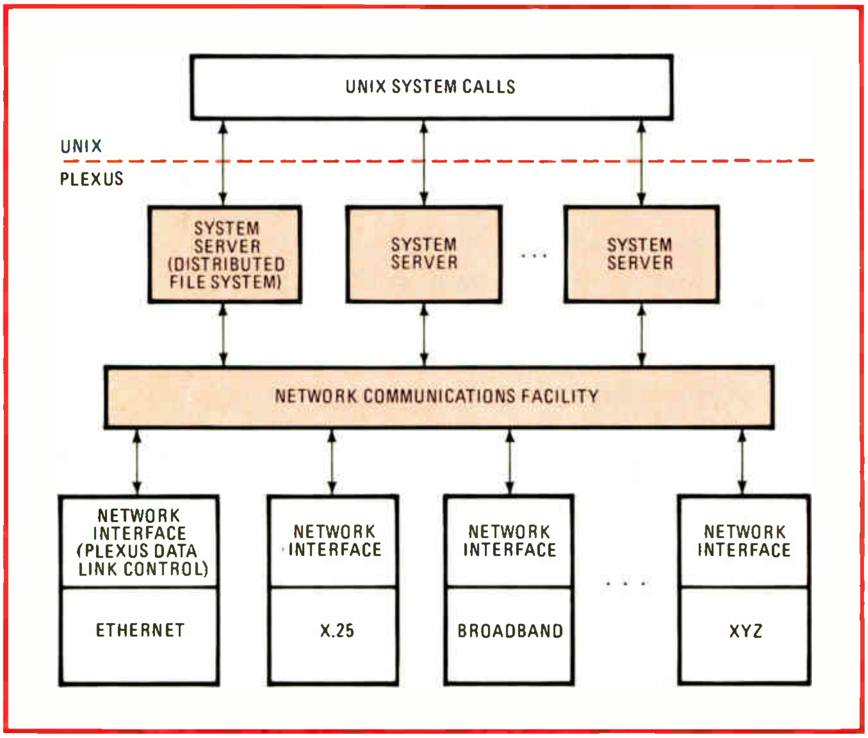
Plexus has modified the mount command so that any branch of a file-system tree in one network processor may be mounted on any branch of a file-system tree in another processor in a way that makes the logical pathname to a file the same from any system. The company has also added an interface with Unix that converts logical pathnames into physical network addresses. Users can call up a file without knowing where it resides on the system and work with it just as though the file were locally resident.

A similar system is under development at the University of California, part of Berkeley Unix 4.2; and an Italian firm, Software Sistemi SpA of Bari, has described a conceptually analogous method for transparent distributed files on the Olivetti BCS 2000 system. Apollo Computer Inc., Chelmsford, Mass., has announced an even more powerful distributed system, with all network entities related to a single root, in a 12-megabit-per-second local network for its Domain II engineering work station.

Insulators. The structure of the distributed file system is shown in the diagram below. Access is by standard Unix system calls, such as open, read, write, or close. These calls activate system-server software, a set of modules that insulates the user from the physical network. The file-system server, for example, translates logical pathnames into physical addresses on the net. (Other system servers provide other functions, such as allowing one terminal to attach to a remote processor.)

The actual interface with the network is through a software module called the network communication facility. It buffers and formats data according to the protocol requirements of a given network. The first interface implemented by Plexus is for Ethernet; in the offing are links to X.25 and broadband networks.

Plexus's line of superminis run under the Bell System's Unix System III. Linking the processors in a distributed file system affects performance because of the overhead incurred in maneuvering files around the net. Plexus's goal, by the time it offers its distributed file system as an option to its Unix operating system next month, is to limit degradation to 20%, which, it says, would be nearly imperceptible to a user on an interactive system. –**Clifford Barney**



Shield. The Plexus Distributed File System insulates a user logically and physically from the presence of a network. A system server turns logical Unix pathnames into physical addresses; a network communication facility performs the data formatting needed to interface with a network. Plexus has developed its own data-link control, PDLC, for Ethernet.

Consumer

Smart card gets U. S. Army checkup

The smart card is donning government-issue khakis this month for a half-year field test that pits it against the magnetic-striped card as a future means of identification for U. S. armed forces personnel. Involving 2,000 to 3,000 cards, it is the first large-scale trial for the chip-in-a-credit card in the U. S., although major tests in three French cities have been under way since last year [*Electronics*, March 24, 1982, p. 96].

Safeguard. The Army's Fort Lee, Petersburg, Va., is the site for the smart cards, part of a Department of Defense effort to replace the antiquated paper-card ID system that, easily counterfeited, costs it millions each year in fraudulently obtained benefits. The smart card puts a better lock on those benefits because it buries its encoded information in erasable programmable read-only memory in an opaque plastic resistant to tampering by ultraviolet light.

Its chief disadvantage at this point is price—about $7 to $10, says Steve Szirom, president of HTE Management Resources, a Sunnyvale, Calif., market researcher. Though that is much lower than the $30 or so of several years ago, he notes, it is still extravagant in comparison with the 50¢ magnetic-striped card.

The DOD program, called Rapids, for real-time automated personnel ID system, is being directed by the Navy. The smart card, resembling a standard credit card in size and feel, will be handed out to base personnel, their family members, and retirees

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Rapids is keyed to the DOD's central data base containing health care entitlements and other information, called Deers, for defense enrollment eligibility reporting system. Deers would be updated automatically each time a card was issued or changed.

French cards. The cards are supplied by Philips Data Systems of Paris, France, a subsidiary of NV Philips Gloeilampenfabrieken of the Netherlands, which is also leasing programming and card-reading equipment to the Government. It is a two-chip card, containing an 8-bit microprocessor and a 16-K E-PROM (of which 12-K is available), says software engineer Ava Kushner of Input Output Computer Systems Inc., Bethesda, Md., the systems-integration contractor for Rapids. Military operators will take care of issuing and updating the cards using menu-driven application programs, she adds.

Since the purpose of Rapids is merely identification, the smart card is a bit of overkill, concedes Charles Erdrich, an IOCS program manager in Waltham, Mass. Moreover, the personnel data—consisting of name, rank, social-security number, sex, and so on—takes up only about 2-K. "We wanted to test the top of the line," says Cmdr. Bert Robbins, assistant Rapids project officer, adding that more use of the card's capabilities may be made in the future.

The magnetic-striped card, simpler, cheaper, but more prone to counterfeiting, will be tested at five locations: the Marine Corps' air station in Cherry Point, N. C.; Seymour Johnson Air Force Base in Goldsboro, N. C.; the Naval Amphibious Base in Little Creek, Va.; a Navy ship in the Norfolk, Va., area; and a military entrance processing station in Richmond, Va. The complete Rapids test program will issue some 30,000 to 35,000 cards, Erdrich says. –**Marilyn A. Harris**

Fort Harrison runs its own smart-card test

The soldier data card is the handle they give it at the U. S. Army Soldier Support center at Fort Benjamin Harrison in Indianapolis, but it is an even smarter card than the one being used in the project about to get under way at Fort Lee. "We're looking at a 64-K memory chip," says Chris Occhialini, the civilian chief of the team studying it, "and our scope is much vaster than Rapids"—the acronym designating the Department of Defense identification system at Fort Lee and five other military installations.

The Army envisions keeping a soldier's complete personnel, medical, and financial records on the card, using most of the 64-K memory available, Occhialini continues. "There won't be any paper in the next war," he says. "Soldiers won't be carrying their intake records from installation to installation in a theater of operations.

"We envision keeping everything from physical and dental exam information to paycheck provisions on the card, and possibly even weapon and clothing issuance," he adds. "Rapids is a peacetime identification application to eliminate fraud. Our system will be good in war and peace. It's decentralized at the lowest level—no on-line central data base to go down, though we will have that redundant capability."

Rejection. The Army started to explore the smart card in January 1982 as a complete records-keeping vehicle after the Rapids planners, several months earlier, had originally rejected the technology as too new and unproven, preferring at that stage the magnetic-striped card, says Occhialini. The Fort Lee smart-card trial was decided on later, but by that time Fort Harrison was well on its way. Occhialini points out it is strictly an Army effort—Rapids is a joint-services program—but he describes the other services as very interested.

A limited demonstration is set for May, with a full trial slated to be ready to roll by November. "We're fleshing out exactly what we need now and are considering EE-PROM [electrically erasable programmable read-only memory] as well as E-PROM," Occhialini says. "I haven't seen any instructions to 'buy American,'" he adds, "but I am concerned about that." **–M. A. H.**

Testing

EE-PROM boasts own test circuitry

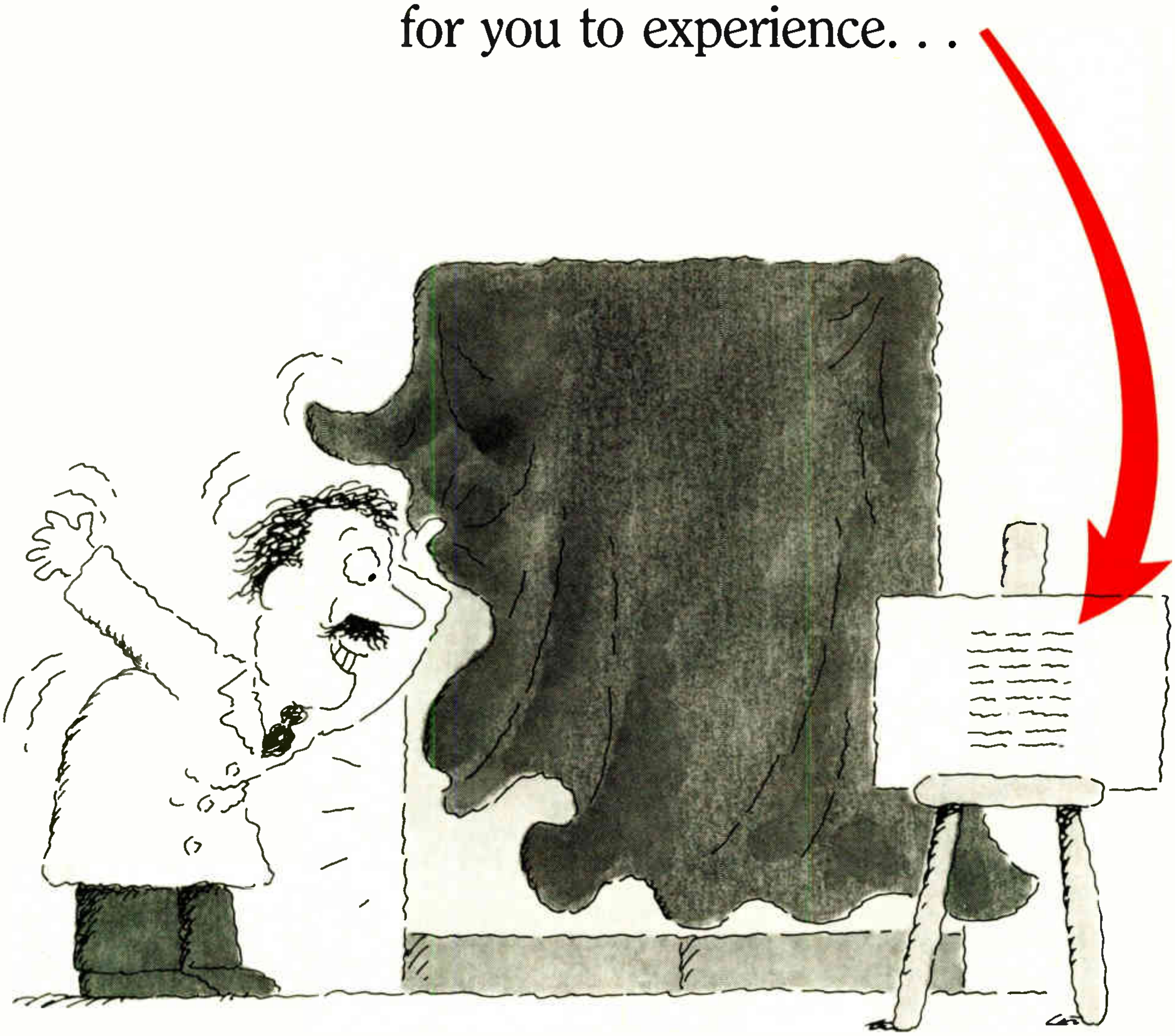
Although the thrust for increasing the testability of circuits has come mainly from those who must deal with logic circuitry, a paper given at the International Solid State Circuits Conference in New York last month indicates that testability disciplines are invading the area of memory design as well.

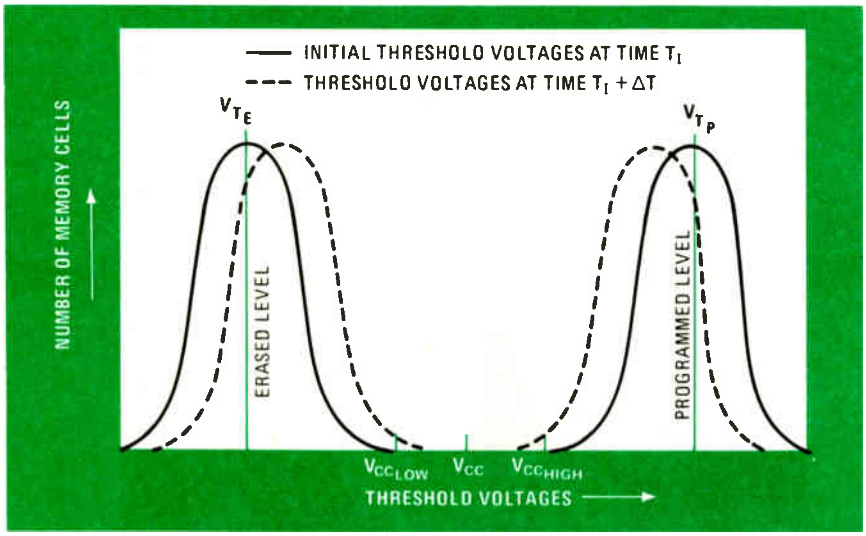
The paper's author was Mark Knecht of Signetics Corp., Sunnyvale, Calif., who discussed his company's design of a 64-K electrically erasable programmable read-only memory, a complementary-MOS 8-K-by-8-bit part with under-100-nanosecond access times. The part was given special on-chip circuitry that not only allows multiple addresses to be programmed simultaneously, instead of one address at a time, but permits the thresholds of all memory cells to be examined by manufacturer and user alike.

According to Knecht, the proprietary test circuitry consists of about 50 transistors, keeping the real-estate overhead of the 175-by-167-mil part acceptably low. The payback to the manufacturer is significant.

Faster sort. At the wafer-sorting stage, for one, the circuitry permits up to 4 bytes, instead of 1 byte, to be programmed at once, which reduces by 50% the time to find bad die. Then, in burn-in testing, the circuitry allows a stress voltage to be placed on all cells in the memory array simultaneously. According to Knecht, "this means that a 100-hour burn-in test can be performed in a mere 23 minutes," a time-reduction factor of around 250.

But it is a third test mode that will likely result in the biggest windfall





Failure mode. Erased and programmed thresholds of EE-PROM cells can shift with time, causing read errors. While in use, Signetics' 64-K part lets shifts be found and corrected.

for memory manufacturer and user alike. In this mode, the threshold voltages of both programmed and erased cells, V_{T_P} and V_{T_E}, respectively, can be measured and logged.

These threshold voltages (see diagram, above) are critical to the memory's operation. If an erased cell gains charge, a common failure mode of EE-PROMs, then above some level, $V_{CC_{Low}}$, the cell looks as if it has data stored in it. Though manufacturers do have some feel for the causes and effects of this phenomenon, Knecht believes that no one knows exactly what is going on.

Thus the new testability feature will allow Signetics more closely to measure and characterize devices, since measurements can be made with standard memory testers used on today's production lines. Knecht believes that specification of threshold stability will, therefore, eventually become part of data sheets.

However, the ability to measure cell thresholds has an important potential application for users as well. If they place a variable voltage source in their system, one that can be set to the desired thresholds for reliable memory operation, then the chips can be tested *in situ*.

Automatic. This approach would add to system reliability. It would allow users to see if the cell thresholds have shifted over time. Thus, their system could be designed to reprogram the chips automatically, thereby resetting thresholds to the desired levels. Further, chip status could be automatically logged, and service personnel informed when a marginal chip needs replacement.

Knecht notes that the feature could be added to other types of memory chips, as well. Though he will not say so, it is likely, considering the advantages offered to both manufacturer and user, that future chips to be developed by Signetics would also make use of the scheme. **–Richard W. Comerford**

Industrial

Auto makers focus on vision systems

Computer vision systems integrated with specialized tooling and fixturing are moving increasingly onto the factory floor for a variety of jobs involving production and final testing. In the U. S. automotive industry, the latest examples come in instrumentation, where divisions of both General Motors Corp. and Ford Motor Co. plan to bring up internally developed vision-based systems to automate the calibration and inspection of analog fuel gages and the testing of digital electronic clocks.

"Computer vision is definitely a developing field here at AC Spark Plug and throughout the [automotive] industry," says Donald E. Lemke, a process engineer in the Instrument Products group at GM's AC Spark Plug division in Flint, Mich. Lemke co-authored a paper given last week in Detroit that describes the so-called Gagesite system developed for fuel-gage calibration and final inspection at AC Spark Plug.

"We require a human to put the [gage] pointer on the [gage's] spindle, but we don't need human intervention again until we pack the finished, inspected gage for shipment," says Lemke of the system, which is slated for factory installation next year. The system's description was presented at the 1983 International Congress and Exposition sponsored by the Society of Automotive Engineers.

Stylish. With software techniques and fixturing flexible enough to handle more than 200 different styles of analog fuel gages, the Gagesite system will rely mainly on off-the-shelf components such as eight Reticon Corp. solid-state cameras and nine Digital Equipment Corp. PDP 11/23 computers—one serves as system controller. These are combined with three specialized machines directed by a Gould Modicon division 584 programmable controller, also under system control, that perform tasks automatically, including the staking of gage pointers in place and the inclusion of one of seven resistors matched to the calibration resistance of the particular gage.

Gages moving through the system are viewed by four separate cameras; the pointer is calibrated at both E and F (for empty and full) and then inspected at both positions. Run rate depends upon pick-and-place equipment still being developed that will move the gages from machine to machine, says Lemke. The target rate is about 1,000 gages an hour, about the same as with manual methods. But by automating the process, the GM division hopes to halve labor costs while at the same time reducing the number of gages calibrated improperly because of human error.

The other vision-based system was described in Detroit by Ford's Elec-

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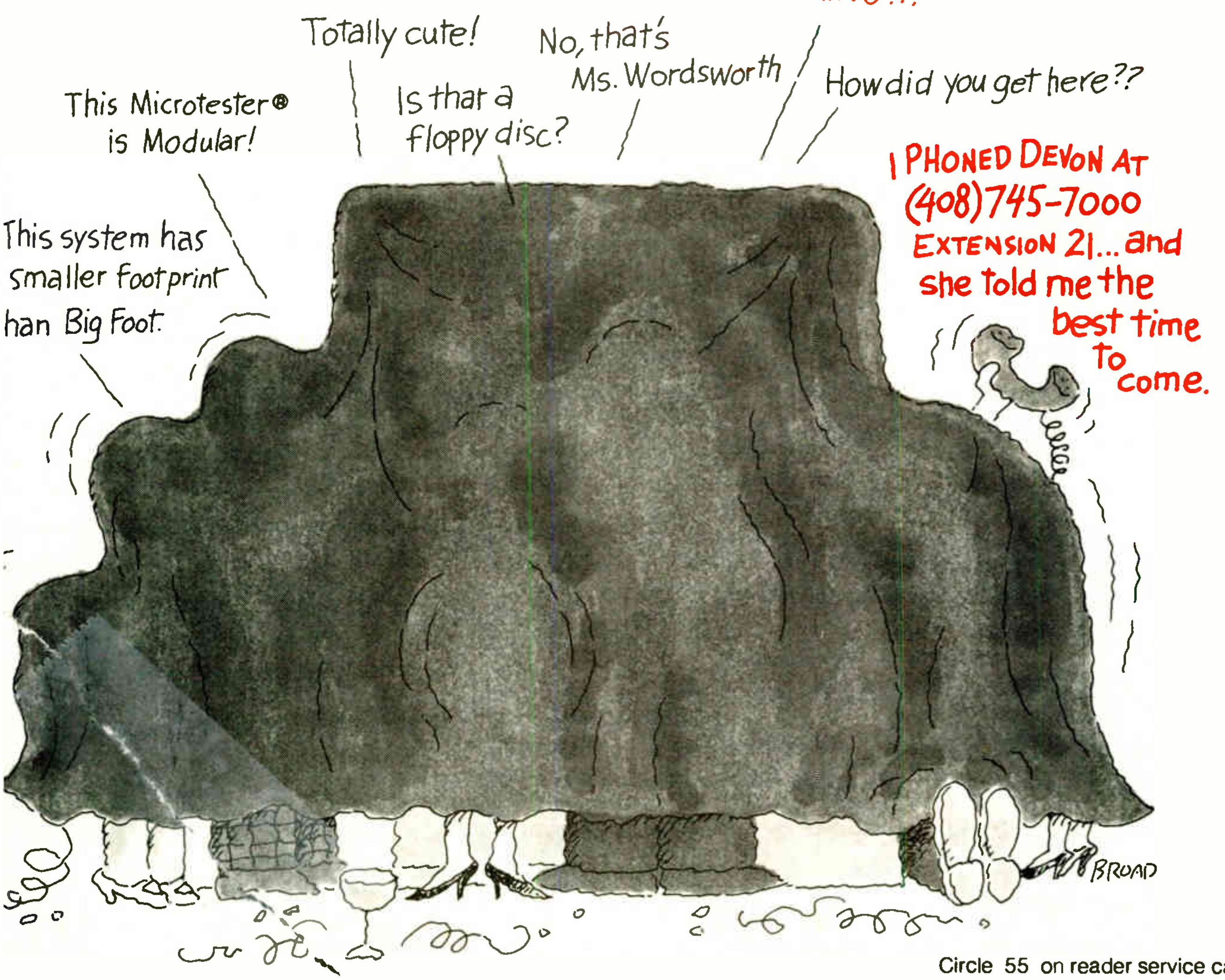


Circle 55 on reader service card

News Briefs

Home computer turns up with hazard possibility

With things looking bright for the Texas Instruments Inc. 99/4A home computer, the firm halted shipments last month to fix a potential defect in the power transformer sold with the unit. The fix is ready—an adapter between the line-voltage outlet and the transformer—and TI expects to resume shipments by mid-March. It is already mailing adapters to 99/4A owners. TI is correcting what it says is a remote possibility, revealed by its Consumer Group in Lubbock, Texas, that transformer failure could cause an electrical shock or damage to the computer. No such incidents have been reported.

The transformer is assembled in Mexico by a vendor. No other computers are believed involved, according to the Federal Consumer Products Safety Commission. The 99/4A has a large share of the booming U. S. home computer market, with an estimated half million sold. The suspension of deliveries will lower pre-tax first-quarter earnings by $50 million, say TI officials.

Plane maker goes commercial with switching power supplies

Boeing Aerospace Co. is going after the military market for custom switching power supplies. It enters the business after trying unsuccessfully to buy supplies with 65% efficiency, 1%-to-3% regulation, and 98% reliability factor, according to Albert J. Mateu, power supply program manager at the Electronics Support division, Seattle, Wash. Boeing had to build its own units, he says, for systems aboard craft like the 757 and 767 passenger planes and the MX missile. Mateu adds that the company has developed a new lightweight inverter and will pack in 5 watts per cubic inch, yet remain within junction and case temperatures set in guidelines released last April by the U. S. Navy.

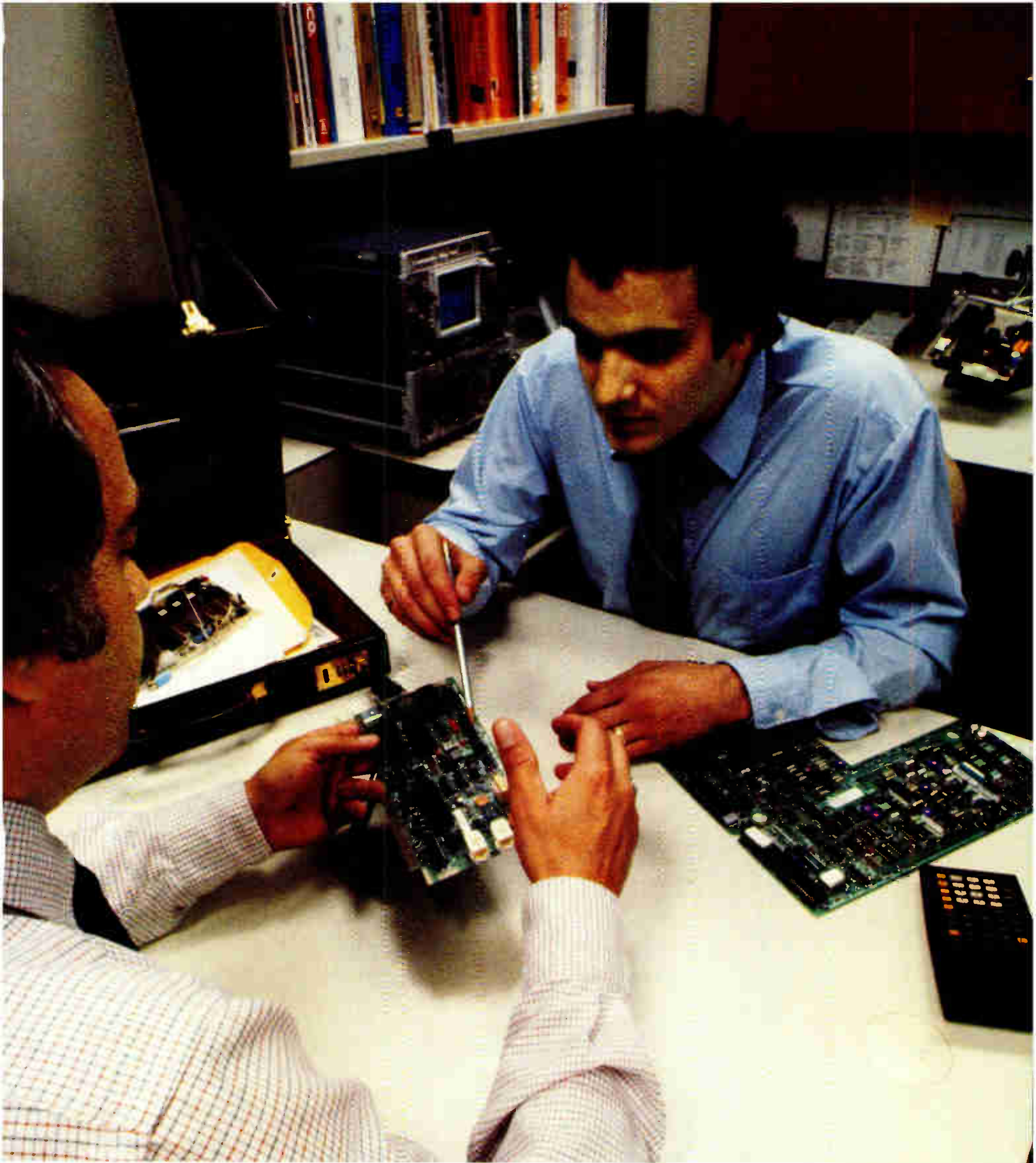
First microcomputer chip promised with EE-PROM

The promise of Seeq Technology Corp., San Jose, Calif., last month to offer the first microcomputer chip with electrically erasable programmable read-only memory should pique the interest of system integrators. The EE-PROM will replace on-chip ROM in Texas Instruments' two-year-old family of 8-bit TMS7000 microcomputers. Flexibility and longer life without servicing are key advantages, as programs for such things as process-control, robot, and instrument systems could be adapted to changing environmental and process conditions, component drift, and aging. Programs could be downloaded over communication lines into the 3-micrometer n-channel MOS parts that operate from a single 5-volt supply. Available first in the second quarter will be the 72720 with 2-K bytes of EE-PROM replacing 2-K bytes of ROM.

IBM changes guard

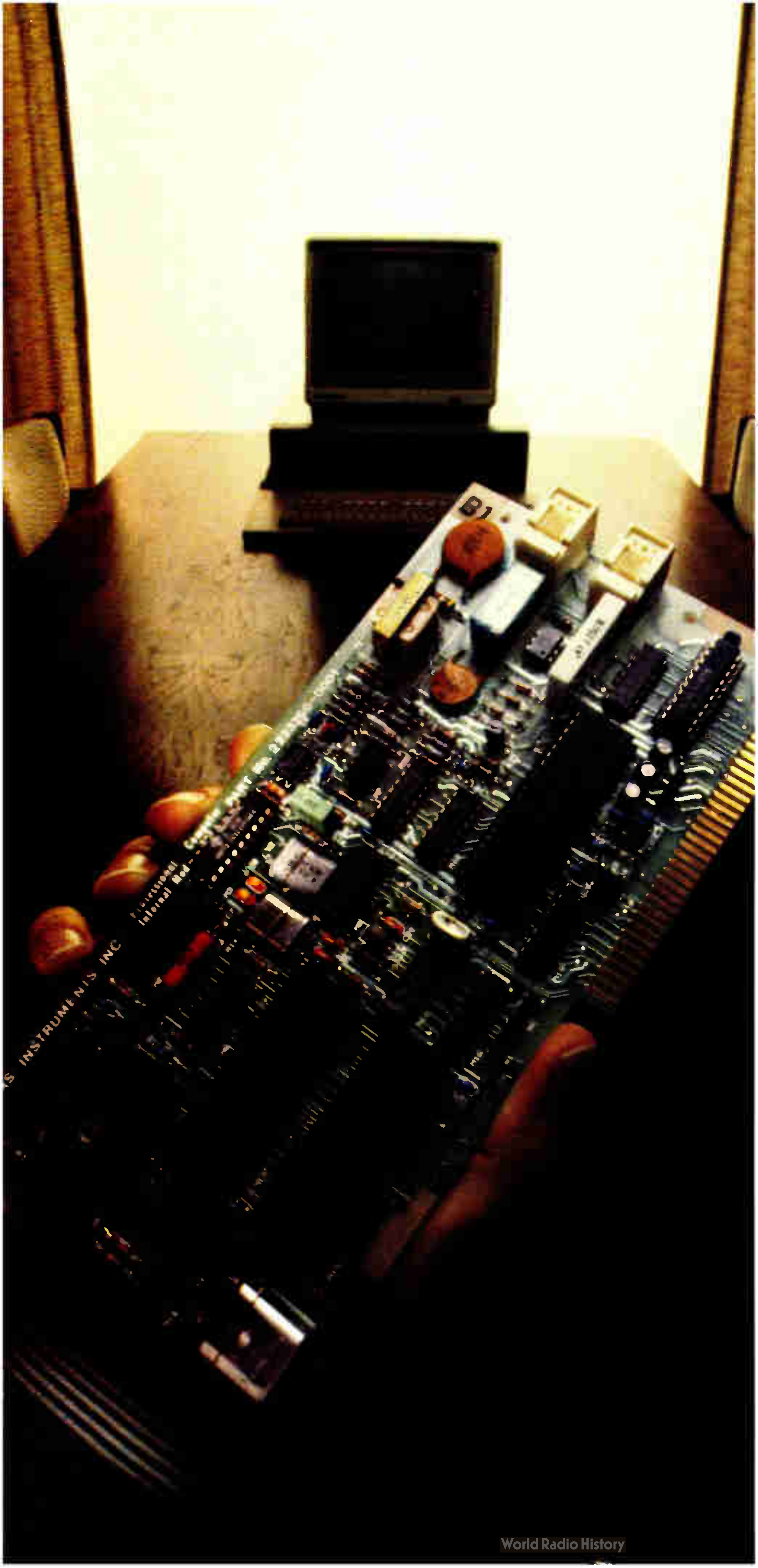
International Business Machines Corp., Armonk, N. Y., has shuffled top management following the resignation of chairman Frank T. Cary, 62, who held that position for 10 years. John R. Opel, 58, president since 1974, moves up to replace Cary and continues as chief executive officer. Cary now chairs the board's executive committee. Replacing Opel as president is John F. Akers, 48, the senior vice president and group executive in charge of IBM's Information Systems and Communications Group. That group handles worldwide development and U. S. manufacturing of telecommunications and office systems products, as well as the successful IBM Personal Computer. Akers, besides joining the board, becomes a member of the corporate office, which provides overall direction to the firm.

tronics & Refrigeration Corp. subsidiary. It will install three four-camera systems this month in its Lansdale, Pa., plant for testing digital electronic clocks destined for Ford cars, says William N. Frick, a section supervi-



Texas Instruments and Racal-Vadic team up to slim modems down.

- **TI's new TMS99532 modem chip** enables Racal-Vadic to slim modems down from large subsystems to small-scale components (*Page 2*).
- **Packing more functionality on chip,** TI universal microprocessor peripherals cut system size, boost overall performance (*Page 3*).
- **New CMOS A/D peripherals** reduce component count and power requirements in microprocessor-based systems (*Page 4*).



By using cuts size

That's only the beginning of what's happening to modems at Racal-Vadic, world's largest supplier of low- and medium-speed modems. Couple those space savings with 3-to-1 reductions in power requirements. And in costs.

Racal-Vadic's key to shrinking the modem is the new TMS99532 FSK modem chip from Texas Instruments.

Result: Modems no longer need be large PC boards, or expensive, space-consuming, stand-alone subsystems. They are simply becoming small-size components in such equipment as the new professional computer shown here, in interactive terminals, in point-of-sale and in credit-verification systems.

Performance-packed package

Racal-Vadic calls TI's TMS99532 "the only complete Bell 103-compatible modem chip on the market." In a space-saving 18-pin DIP, the '99532 provides all the modulation, demodulation, and filtering functions needed for a serial, asynchronous-communications link.

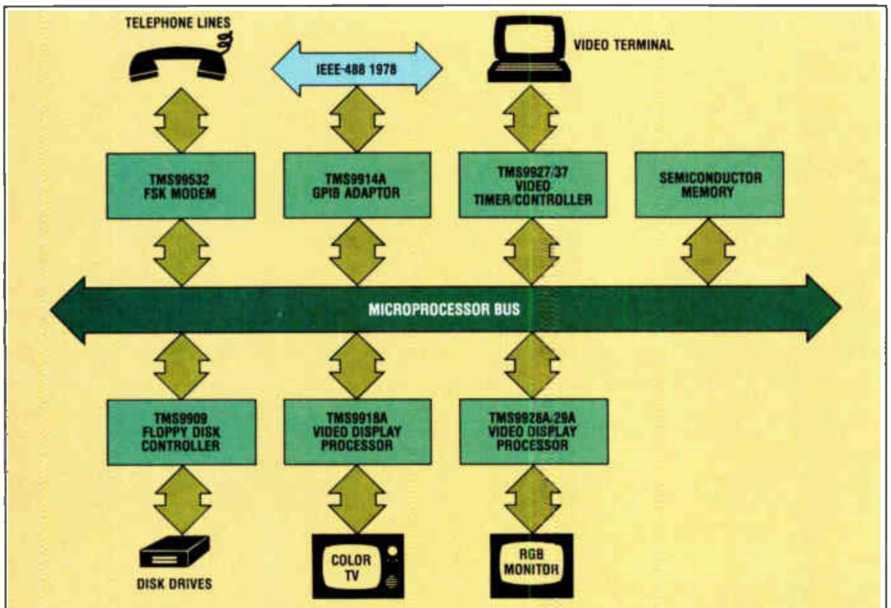
Parts count in Racal-Vadic full-duplex modems has been cut by around 40 ICs and board size reduced from approximately 75 square inches to 25. But with room left for Racal-Vadic to add needed intelligence — for auto dialing, pulse and tone dialing, as well as number storage.

TI's '99532 modem chip has a maximum continuous power dissipation of 550 mW and a TTL-compatible digital interface. It can be direct-connected electronically through FCC registered interface circuits, or acoustically via a microphone and speaker. Interface to a handset requires only a few operational amplifiers. Racal-Vadic finds the TMS99532 extremely reliable and uses the device in other products.

For more information on the TMS99532, as well as the TMS99543 designed to meet European requirements, return the coupon at the end of this ad. Or call your nearest TI distributor or TI field sales office.

◀ **Slim size, trim cost** characterize Racal-Vadic's innovative modems. Full utilization of the functionality packed into TI's new TMS99532 modem chip results in substantially fewer components.

TI's '99532 chip, Racal-Vadic of modems by two-thirds.



Universally applied with any microprocessor, TI's new highly functional, single-chip peripherals reduce component count, cut costs, and improve reliability in popular 8- and 16-bit microsystems.

TI's advanced microprocessor peripherals: Fewer parts, lower costs, better reliability.

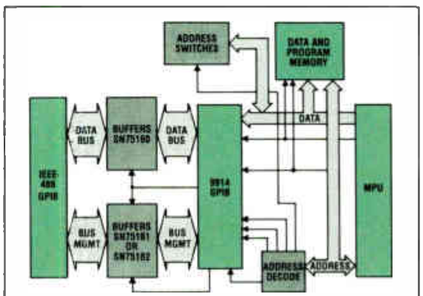
The TMS99532 modem chip that helped Racal-Vadic pare modem size is just one of TI's advanced microprocessor peripherals. Each new single-chip component performs functions that usually require multiple devices. Or entire boards.

Best of all, they are *universal* — compatible with all popular 8- and 16-bit microprocessors. So you can upgrade your design now, yet save your software investment.

Flexible, versatile floppy disk controller

TI's TMS9909 controls the floppy disk drives used in today's word processing, business, and industrial systems, as well as personal computers.

The TMS9909 reads from or writes into partial, single, or multiple sectors of hard or soft disks. It simultaneously controls two different disks and can support any combination of up to four different single/double-sided standard 8" or 5¼" mini disk drives. It can be used with all data-recording formats and frequency-modulation data-encoding formats.



Minimum System Solution using TMS9914A GPIB Adapter

Single-chip GPIB adaptor

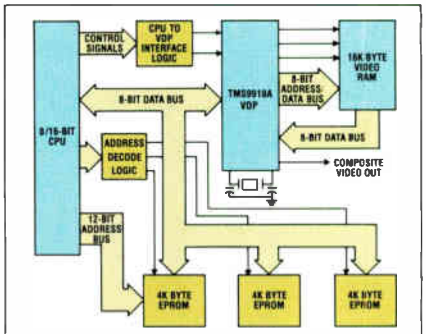
The Texas Instruments TMS9914A combines talker, listener, and controller in one General Purpose Interface Bus Adapter. And meets IEEE Standard 488-1975, 1978, and 1980 revisions.

TI's TMS9914A provides a flexible, unambiguous interrupt structure which separately latches all interrupts. No lost interrupts. No spurious interrupts.

And the '9914A is fast on the bus: Data rates as high as 500K bytes per second are possible.

Simpler color video display processor

Video and arcade games. Home computers. Graphics terminals. Learning aids. Industrial process monitoring. Drafting and animation systems. You create an entire color system for any of these using only TI's TMS9918A display processor and picture storage dynamic random access memories (DRAMs). The composite video is generated directly on the chip, and refresh of the DRAMs is automatic and transparent.



Minimum System Solution using TMS9918A Video Display Processor

The '9918A produces 15 colors plus transparent, with 256 x 192 pixel on-screen resolution. The similar TMS9928A (525 lines) and TMS9929A (625 lines) offer separate luminance and chromance outputs for better resolution with R-G-B monitors.

Industry-standard video/timer controller

Pin-compatible with industry-standard 5027s and 5037s, the TI single-chip TMS9937 generates video display timing signals for EIA Standard RS-170, as well as for non-standard CRT monitors. In non-interlaced operation, with an even or odd number of scan lines per data row. Or in interlaced operation, with an even number of scan lines per data row. And the '9937 can be programmed for interlaced operation for an odd number of scans per data row. This eliminates character distortion caused by the uneven beam current associated with odd/even field interlacing of alphanumeric displays.

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Six new TI CMOS A/D converters slash microprocessor parts count.

TI's New 8-Bit A/D Converters

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Digital Inputs (To Register)	—	0	0	6 to 12*	6 to 12*	0 to 6*	0 to 6*
Resolution	Bits	8	8	8	8	8	8
Unadjusted Error	LSB	±0.75	±0.5	±0.5	±1.0	±0.5	±1.0
Analog Access + Conversion Time	µsec	70	200	300	300	300	300
Supply Range	Volts	4.5 to 6	3 to 6	4.5 to 6.5	4.5 to 6.5	4.5 to 6	4.5 to 6.5
Operating Power (Typ)							
At 5 Volts	mW	2.5	2.5	15.0	15.0	15.0	15.0
At 3 Volts	mW	N/A	0.3	- Not Available -		- Not Available -	
Operating Power (max)	mW	5.0	0.6	88	88	88	88

* Includes 6 multipurpose (analog or digital) inputs.

Designed as peripherals for 8- and 16-bit microprocessor-based systems, TI's new family of CMOS A/D converters offers the designer six alternatives to cut space and power requirements.

You can now build a microprocessor-based system that can read and respond to a set of analog inputs with a low IC part count and low (CMOS) power. The new Texas Instruments family of six CMOS ICs, designed as peripherals for both 8- and 16-bit microprocessors, all make available an 8-bit digital conversion to the processor's data bus of any one of 8 to 15 analog inputs. They replace A/D converter, multiplexer, sample-and-hold, and control ICs.

The TL520 Series is a modern "switched-capacitor" 8-input A/D peripheral that replaces the "standard" ADC0808 and ADC0809 with lower power and a wider power supply range.

The new TL530 Series offers the greatest flexibility to the system designer. These ICs can handle either digital inputs and/or analog signals from up to 21 different sources — making this data available to the 8-bit or 16-bit processor on the 8-line data bus via an 8-pin I/O port. Furthermore, the TL530 Series can be controlled and its inputs selected (from the data bus) through this same I/O port.

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88

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sor in the subsidiary's equipment engineering department.

The Ford system employs air-driven plungers to push buttons on the front of the clock that set up readings of date, time, and elapsed time. As voltages are applied, the clock's electrical response is measured using conventional meters, while a Reticon camera focuses on the display and checks the accuracy and brightness of the clock's four-digit, seven-segment vacuum fluorescent display. (Such checkout of displays has been done for years by Texas Instruments on its calculators.)

Each Reticon MC520 camera has its own controller and a DEC LSI 11/23 computer for processing images. Overall system control is an HP9825T desktop computer's job.

Frick says Ford may use its system to test other products, like radios, with relatively simple displays and controls. But for a complex instrument cluster, for example, the firm may buy equipment from one of a growing number of outside vendors. Officials at both divisions note that several turnkey systems now available are becoming cost-effective compared with vision systems developed internally. –Wesley R. Iversen

Companies

Prime turns on to CAD/CAM

Companies can become nervous if they rely on but a single product line, and especially so when the Wall Street analysts who follow them notice and begin to talk about it amongst themselves.

Such was the case with Prime Computer Inc., the superminicomputer maker in Natick, Mass., in the summer of 1981 after its long-time president left abruptly. When it took five months to find a successor, many analysts became convinced that the company's spectacular growth was at an end and that it had seen its best days.

But with a new management team headed by Joe M. Henson from IBM

At the helm. "Very well positioned" is how John Buckner describes Prime Computer's CAD/CAM Business Group, which he heads.

Corp. and a $50-million-a-year foothold in computer-aided design and manufacturing to complement its 32-bit supermini product line, Prime has convinced leading analysts it is now poised for new growth.

"CAD/CAM is a very large and rapidly growing market, and we are very well positioned to take advantage of it," says John K. Buckner, chief financial officer and acting president during the interregnum, who was chosen in January to head the new CAD/CAM Business Group. What's more, Prime closed out its fiscal year on Dec. 31, 1982, with record sales of $435 million, up more than 19% over 1981.

Observes market analyst Ulric Weil, principal at Morgan Stanley & Co. in New York, the company is now ready to take advantage of two huge growth markets. The annual growth projections are 25% to 32% for superminis, he notes, and 35% to 40% for CAD/CAM.

Early comers. Even before Henson arrived, Prime, looking for applications for its powerful computers, saw CAD/CAM as a logical new market. And unlike its software-oriented CAD/CAM competitors, who turn typically to Digital Equipment Corp. for hardware, Prime is able to draw on its own hardware, data-base management, and networking capabilities. Meanwhile, the company has been busy stockpiling proprietary rights to CAD/CAM programs and entering third-party software development agreements right and left.

Buckner feels Prime already has weighty presence in the mechanical,

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electrical, and architectural engineering and construction fields. At least 185 CAD/CAM programs can be run on its model 50-series computers. Competing with DEC VAX machines, models such as the 550-II and the more powerful 750 sell for $100,000 and up. In addition, the company has exclusive rights to over 20 application programs, including the successful Medusa program, developed by Cambridge Interactive Systems Ltd., Cambridge, England, for solid modeling of mechanical designs. Prime has exclusive marketing rights for Medusa outside West Europe through 1985.

Likewise, in acquiring Compeda Ltd. of Stevenage, England, the firm gained rights to what is, says Buckner, a highly valued program, PDMS, (for plant-design management system) for designing nuclear power plants, chemical refineries, and oil rigs. PDMS, he says, is the only such program that has been used to design major industrial plants that were subsequently built.

Electronics, too. With its own recently introduced Electronic Design Management System (EDMS) for multiple users, the firm has also established itself in the integrated-circuit and printed-circuit–board design markets. EDMS adds a centralized components library and powerful data-base management capabilities to the third-party software programs with which it interfaces.

Prime feels that EDMS, combined with the Scicards program of Scientific Calculations Inc., Fishers, N. Y., offers the most powerful available tool for the design of dense multilayer pc boards. EDMS can also be interfaced with such programs as Merlyn-G for gate-array routing and Tegas for logic simulation.

Meanwhile, Prime has regained the favor of computer-industry analysts. Its stock price has tripled since its market low of under $16 last year. The company has "established a unique strategy for a minicomputer maker," says Marc Shulman, vice president at First Boston Corp. in New York. "The situation there was a recipe for disaster. But the disaster never happened." **–Norman Alster**

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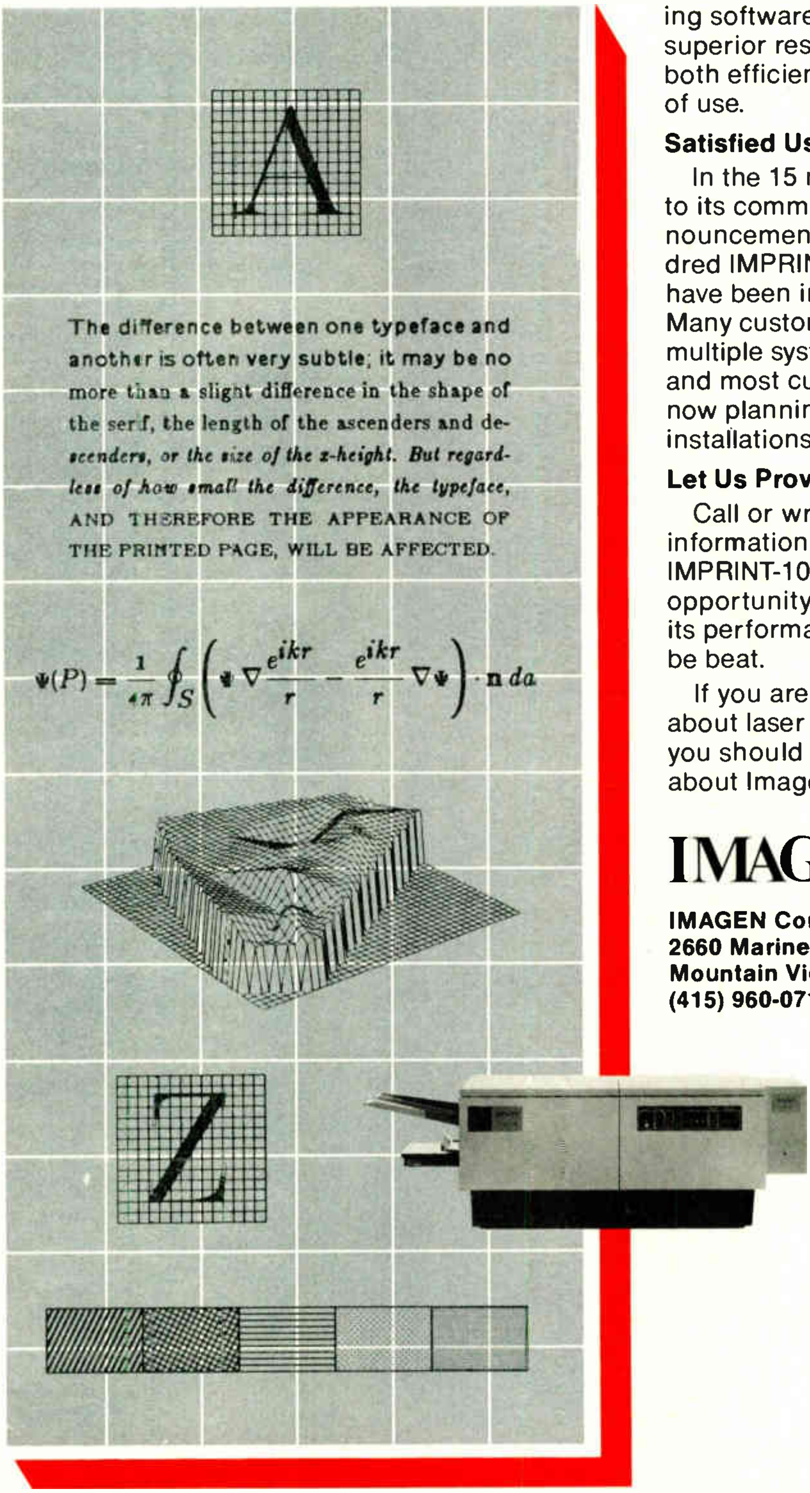

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Washington newsletter

Lockheed team picked to develop Milstar . . .

Although a firm contract is not expected for two months, the Air Force has picked a team headed by Lockheed Missiles & Space Co. of Sunnyvale, Calif., for full-scale development of the satellite and payload for the Milstar communications system [*Electronics*, Feb. 24, p. 57]. Lockheed, working with Raytheon Co. of Lexington, Mass., and General Electric Co. of Valley Forge, Pa., will develop the **eight satellites to be used in the multibillion dollar system for strategic and tactical forces.** Overseeing the work is the Air Force Space division in Colorado Springs, Colo. The first launch is scheduled for 1987.

. . . RCA, Rockwell win design awards for emergency network

Competitive design contracts for the low-frequency emergency military network for use during and after nuclear attack have been awarded to RCA Corp. and Rockwell International Corp. Called GWEN, for ground-wave emergency network, the digital system is due to be in operation in the late 1980s. **More than 300 relay sites will link the White House and other national command authorities with all major U. S. military sites,** including the North America Aerospace Defense Command, Strategic Air Command, missile-launch control centers, and key surveillance and warning sites. Major commands will be able to send and receive, while others will be able to relay and receive only. RCA's Government Systems division in Camden, N. J., was awarded $3.95 million; Rockwell's Collins Communications division in Richardson, Texas, received $4.95 million. The Air Force is managing the program through its Electronic Systems division in Bedford, Mass.

NASA process promises high-temperature devices

The National Aeronautics and Space Administration is offering instrument manufacturers a practical new process for producing silicon-carbide semiconductors able to endure temperatures up to 870°C. The most likely takers, says NASA, are developers of instruments used by the aviation industry to make measurements in jet engines and by energy firms for readings far below the earth's surface. **Another promising use would be in extremely high-frequency communications where silicon carbide may be a key to using frequency bands measured in hundreds of gigahertz.** Developed by Herbert Will and three other physicists at Lewis Research Center, Cleveland, the technology centers around the heating and coating of a silicon wafer in a 1,400°C chamber. Though ready for transfer to interested companies, commercial availability of the process is a number of years away, say the developers. A major obstacle to mass production is the need for new techniques to etch patterns on the ultrahard material.

Navy and Air Force disagree on HARM cuts

The Navy and Air Force are divided on how much to reduce proposed production of 21,000 high-speed antiradiation missiles (HARM) by prime contractor Texas Instruments Inc., Dallas. **Rising costs and engineering changes for the estimated $7.8 billion program** have the Navy considering dropping the search for a second production source and substituting a 200-lb missile called Sidearm, a variation of its successful Sidewinder air-to-air missile developed by Raytheon Co., Lexington, Mass. Although a Sidearm weighs far less than the 800-lb HARM, its range is also far less and its passive radar receiver is less effective in identifying ground radar targets, say Air Force advocates of HARM. The Air Force has already cut its proposed HARM purchase from 14,000 missiles to 9,000.

NSF and industry fund material-handling R&D . . .

A new Material Handling Research Center being set up at Georgia Institute of Technology in Atlanta—a collaborative effort between the National Science Foundation and industry—**has 11 electronics manufacturers among the 18 corporate members that will pay $30,000 annually apiece to support it.** The goal of the center, set to start up in May, is to aid U. S. companies in remaining competitive by automating in-plant material handling in order to boost productivity and cut costs through reduction of material inventories.

. . . as Litton equips the research center

The first year's budget for the Georgia Tech center will be $740,000, including $200,000 from the NSF as part of a five-year $700,000 grant. In addition, Litton Industries Inc.'s Unit Handling Systems operation in Florence, Ky., is contributing $500,000 for laboratory equipment. **The NSF estimates corporate membership will make the center financially independent within five years.** Besides Litton, corporate members in electronics include: Data General, Digital Equipment, IBM, Lockheed-Georgia, Texas Instruments, Xerox, Boeing, General Dynamics, Grumman Aerospace, and Westinghouse Electric.

Honeywell to lead R&D on production automation

The military's interest in automated manufacturing using real-time sensors and robotics has engendered a $3.35 million contract to an industry-university team. Awarded by the Defense Advanced Research Projects Agency and the Air Force Materials Laboratory at Wright-Patterson Air Force Base in Dayton, Ohio, the initial 27-month effort will be led by Honeywell Inc.'s Technology Strategy Center in Minneapolis, **which has responsibility for systems integration and the development of computer hardware and software and sensors and controls.** Unimation Inc. of Danbury, Conn., will supply the robots, while Stanford University will do research in basic robotics and artificial intelligence and SRI International Inc. of Palo Alto will handle applied robotics. The program was initiated as a result of a recommendation by the Defense Science Board [*Electronics*, May 5, 1982, p. 96] that the military give automation and robotics R&D the same high priority as the Very High-Speed Integrated Circuits (VHSIC) program.

Failed transmitters trouble NASA satellites

National Aeronautics and Space Administration officials are concerned about the promised lifetime of the K-band transmitter built by TRW Inc., Redondo Beach, Calif., for the Tracking and Data Relay Satellite scheduled for launch later this year aboard the new Challenger space shuttle (itself troubled by engine problems). The transmitter contains components in the frequency amplifier and modulator **similar to those in the Landsat 4 earth-mapping satellite's X-band transmitters, the second of which failed Feb. 15.** On the Landsat, the shutdown of the X-band subsystems, also built by TRW, cut off the flow of high-resolution data from the satellite's thematic mapper.

SCIENCE/SCOPE

Fusion energy machines that would turn sea water into electricity, though still 20 years away, are a step closer to fulfilling their promise of satisfying much of the world's energy needs. In plasma-heating experiments, Hughes Aircraft Company researchers have demonstrated a gyrotron with the highest performance yet reported. It produced 285 kilowatts at 60 gigahertz at 45% efficiency under pulsed conditions. The short-range goal of this research program is to generate 200 KW at 60 GHz with long pulses in excess of 100 milliseconds. The long-range goal is to generate 1 megawatt at 100 GHz. The Oak Ridge National Laboratory sponsors the program for the U.S. Department of Energy.

Technologies of laser holography and diffraction optics have led to an experimental visor for protecting military pilots from potentially blinding laser beams. The visor reflects light at wavelengths used for lasers without significantly reducing visibility. It would replace devices employing dyes, which produce distracting discolorations, absorb light, and cut visibility. Designed by Hughes for the U.S. Navy, the visor could be adapted for ground troops.

An Advanced Medium-Range Air-to-Air Missile has intercepted a drone target, showing its ability to find low-flying targets amid high clutter caused by the missile's radar returns reflecting from the ground. The prototype AMRAAM was fired from an F-15 fighter from an altitude of 16,000 feet and a range of about 13 miles. The remotely controlled target flew toward the F-15 only 400 feet above the ground and operated an electronic countermeasures pod in an effort to jam the missile's seeker. Hughes is producing AMRAAM under a full-scale development contract for the U.S. Air Force and Navy.

A cleanroom believed to be the world's largest serves as the birthplace for such military electro-optical devices as laser rangefinders, laser designators, and infrared night vision systems. The new Hughes complex spans 60,000 square feet. It is environmentally controlled to be free of contaminants because even one particle of dirt barely visible to the naked eye could ruin sensititive optics. Although the electro-optical components themselves are delicate and require meticulous assembly, a completed device is hermetically sealed and built to withstand rugged use in the field.

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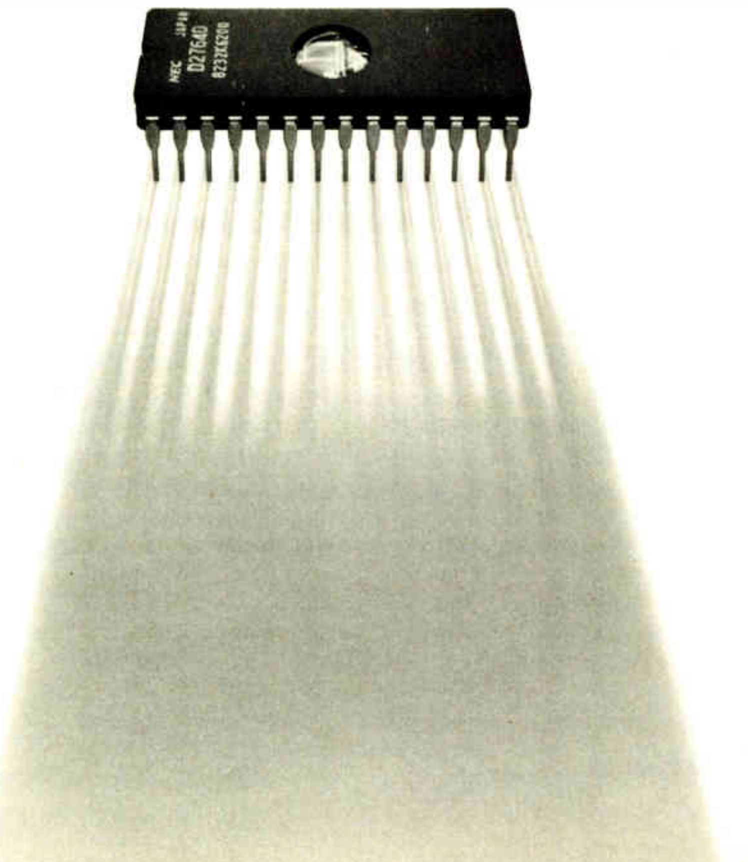

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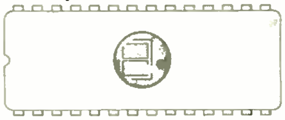

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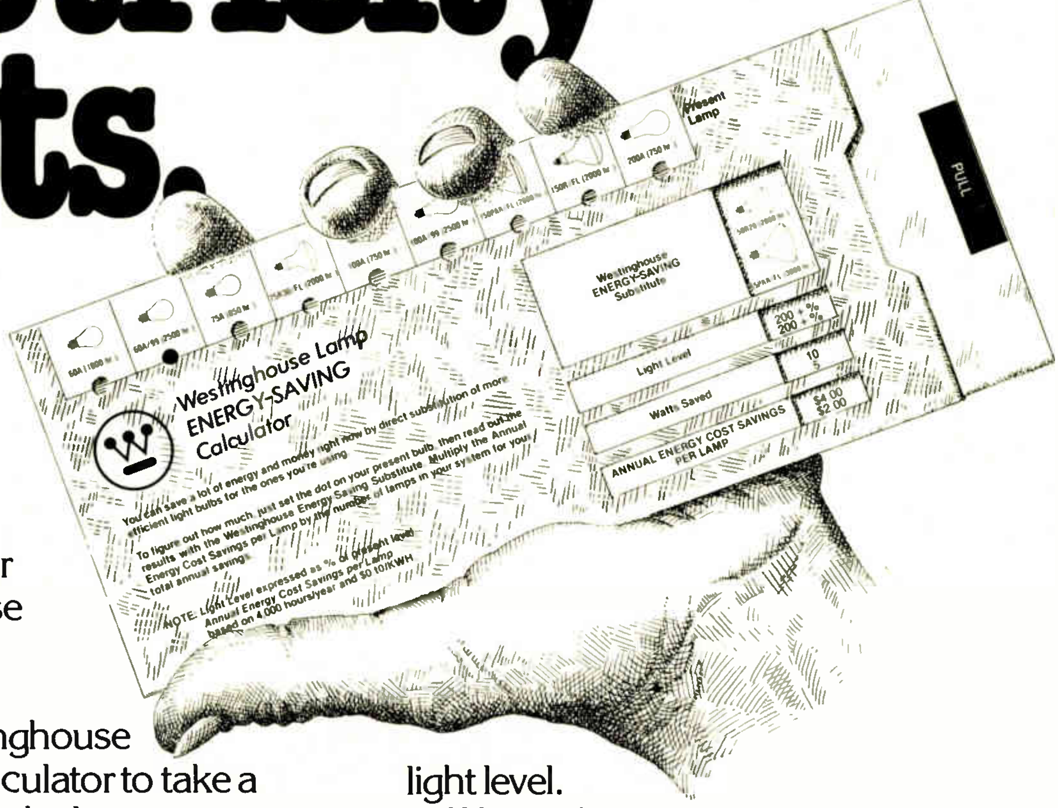

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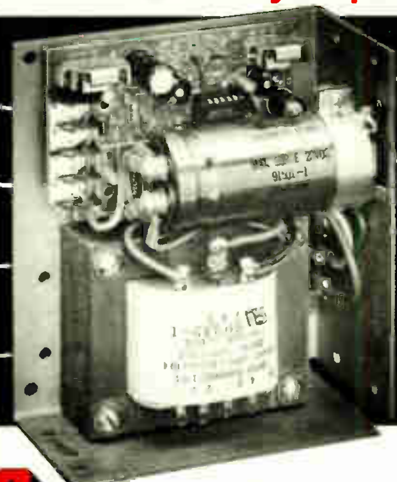

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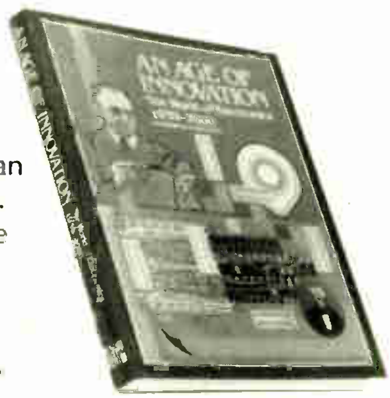

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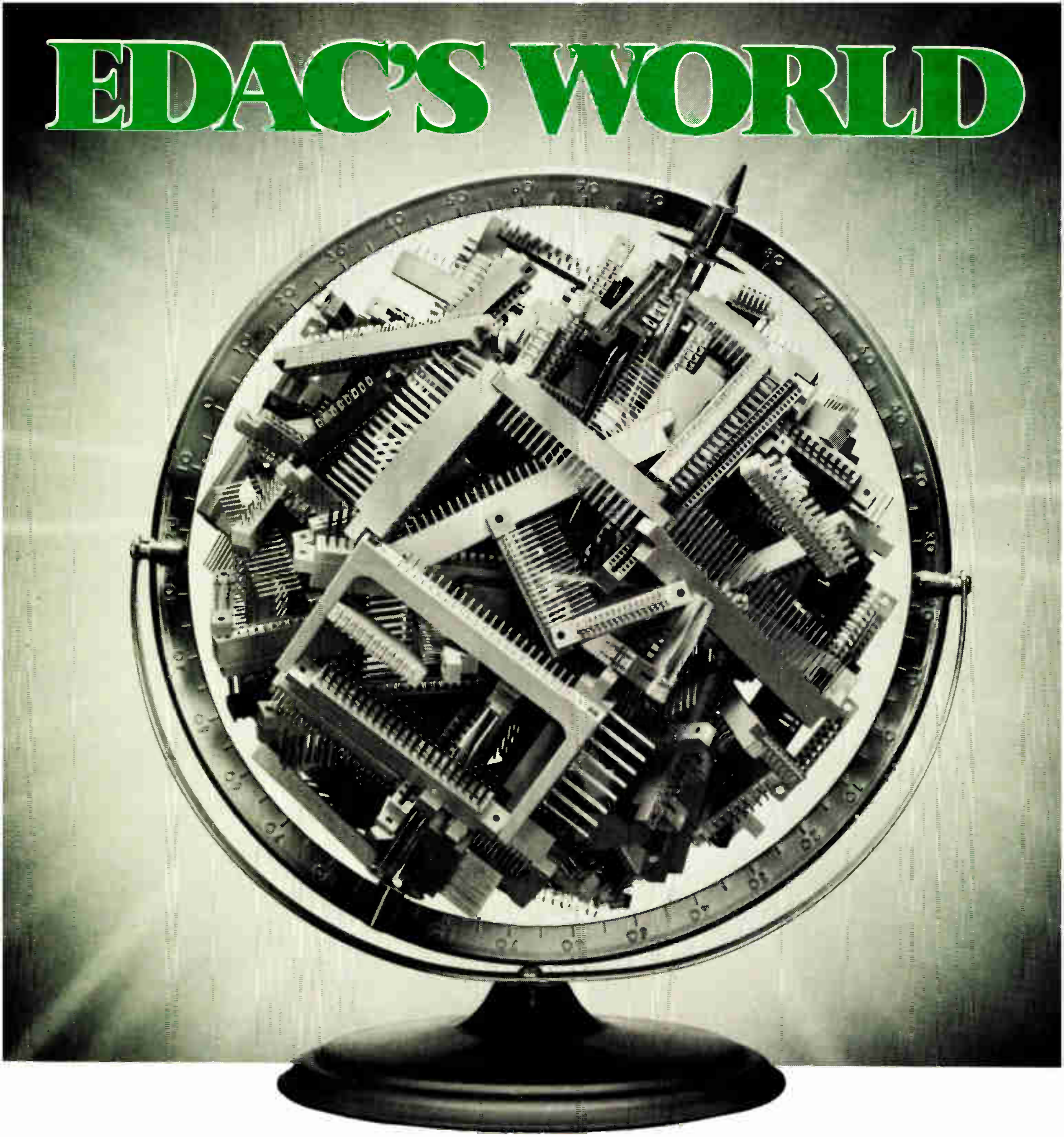

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International newsletter

Israel's first robots are forerunners of national industry

Two Israeli companies are going to market with that country's first locally designed and manufactured robots. The two are part of a group of 10 Israeli companies currently involved in a $40 million effort to develop a national robot industry, for both domestic use and export. The country is expected to have 1,000 robots operational within four years, double that by the end of the decade. Sharona Electronics Co. of Petah Tikva (near Tel Aviv) designed its Gil-1 robot for loading, unloading, welding, assembly, and the manufacture of fragile parts. The company expects to have three models 1 on the market by the end of the year. Developed at a cost of $3 million, **the robot is meant primarily for export and will sell for $50,000 to $100,000,** depending on the add-on needs of the customer. MTC Industries & Research Co. of Carmiel unveiled its $80,000 MTC 404R multipurpose robot for separate use or for integration with other robots in highly complex computerized manufacturing processes. Work on a smaller model, selling for about $50,000, is already under way. The firm, marketing in the U. S. and Europe, predicts export sales of its robots will reach about $2 million within three years.

3.5-in. Winchester drive aims to set standard

Winchester-disk manufacturer Rodime plc, in Glenrothes, Scotland, is bidding to set a *de facto* industry standard with the first 3.5-in. Winchester disk drive. The top-of-the-line RO 352 is a two-platter model packing 10 megabytes of formatted data storage in a space measuring 1.625 by 4 by 5.25 in. Those dimensions are such that **one RO 352 can be interchanged with a 3.5-in.floppy-disk drive or two may be packed into the same space as a half-height 5.25-in. Winchester to provide 20 megabytes of storage.** Alternatively, it and its controller could replace a full-size 5.25-in. drive. The new drive uses much the same technology as Rodime's 5.25-in. RO 200 series, such as the ST 506 electrical interface, the oxide storage medium, and ferrite heads. Data-transfer and -access times are similar, too, at 5 Mb/s and 85 ms. Among the applciations of the 2.2-lb unit will be portable personal computers, intelligent typewriters, cash registers, and teleprinters. There is also a single-platter 5-megabyte model.

French government funds new CII-HB line of data-processing products

CII-Honeywell Bull and the French government have signed a corporate plan **to develop an entire range of data-processing products** going from software, original-equipment–manufacturer components, office-automation networks, and mini- and microcomputers through to medium-sized and large systems. Now the company's majority shareholder after the extensive nationalization program, the government will invest most of the $1.3 billion needed over the next four years. European data-processing executives, however, are skeptical of the plan, describing it as"dispersed" and "overambitious" and suggesting CII-HB concentrate on a few strategic lines rather than attempt to do everything. The plan calls for Paris-based CII-HB, which lost nearly $200 million in 1982, to be profitable by the end of 1986.

Japan's MITI promoting word-processor standards

Japan's Ministry of International Trade and Industry is actively promoting the standardization of information exchange among Japanese-language word processors and office computers. Floppy-disk formats are to be standardized before the editing control codes. A committee of member firms of the Japan Electric Industrial Development Association is in charge of disk track format, while a committee of the Information Processing Society of Japan is responsible for data format. **Track and data formats for 8-in. floppy disks are scheduled to be standardized by the end of March 1984.** Standards for 5-in. floppy disks are to be proposed in that same month and adopted a year later, at which time a Jeida committee will propose standards for word-processor editing codes.

Speaker panel improves public-address system

A new type of speaker, which inventor NV Philips Gloeilampenfabrieken promises will revolutionize public-address systems and speaker stacks, will debut at the Audio Engineering Society exhibition March 15 to 18 in Eindhoven, the Netherlands. The Dutch company's Bessel system consists of high-powered speakers **constructed simply from standard, low-cost loudspeakers mounted on a flat panel** and connected according to the coefficients of a Bessel function. No enclosure is needed, and the sound output is radial. Suitable for movie houses, theaters, and conference-hall speaker systems, the panel overcomes such drawbacks as the high cost and distortion of a single large speaker and the need for acoustic enclosures for several smaller speakers.

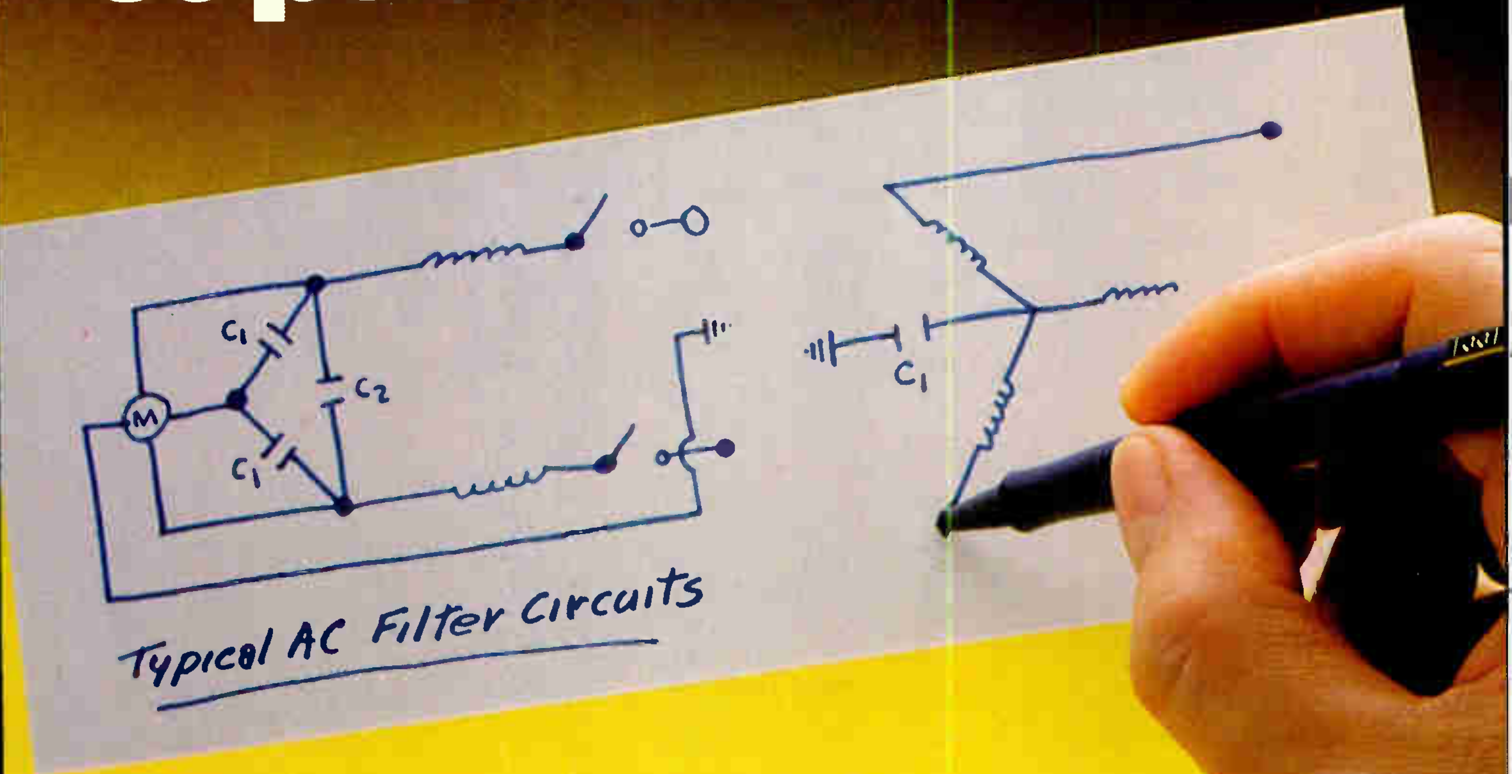
France, Italy team up on electronic typewriters

In the offing from CIT-Alcatel of Paris and Ing. C. Olivetti & Co. SpA of Ivrea, Italy, is a joint venture to develop a new generation of electronic typewriters. Olivetti's price for lending its electronic-typewriter know-how to the venture will be a reduction of the current French government holding in its stock from 33% to about 10% and the transfer of that stock to **CIT-Alcatel, a government-controlled company that Olivetti deems an appropriate partner.** The stock is currently controlled by St.-Gobain-Pont-à-Mousson, which was nationalized in 1981.

Addenda

In a move to consolidate further the French electronic components industry, discussions are under way that could lead to **extensive cooperation between Semiconducteurs Alcatel and Matra SA on custom and semicustom ICs.** . . . The Szki Institute for the Coordination of Data Processing in Budapest, Hungary, has begun production of a personal computer built of components supplied by Orion and Mom, both also of Budapest. The computer was developed by Szki in cooperation with the Automation Department of Budapest Technical University. **An initial output of 250 to 300 computers is foreseen for 1983.** . . . An Israeli company headed by Meir Amit, former head of the Mossad (Israel's secret service), is planning to launch a communications satellite that **will offer channels for TV, radio, Telex, and data transfer for private clients in Africa and the Mediterranean basin.** The satellite, to begin operation in about four years, will be manufactured by Fairchild Industries and launched by the U. S. National Aeronautics and Space Administration. Project coordinator is London-based General Satellite Co. . . . The Swedish Postal Administration expects tough international competition for an upcoming $30 million contract for some 4,000 terminals to replace those located at each postal clerk's station. The sophisticated **terminals will be capable of optical-character reading plus a number of extra services, such as ticket sales** for sporting events and theater.

Tradeoffs in capacitor selection



There's no tradeoff for safety.

Shock protection. Noise supression. Reliable shielding against input voltage spikes. There's no room for compromise if you want to protect your equipment and the people who operate it.

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AC Voltage Rating	330	370	460	200
Dielectric Strength VDC	900	1500	2100	400
Max. Corona-Free VRMS	412	460	600	290

TRW-42 is the ultimate. Rated at 460 VAC. With a high dielectric strength of 2100 VAC. And with sufficient electric shock protection to handle virtually any application, from motor speed controls to large cooling fans. When specifying TRW-42, simply choose the minimum capacitance value your circuit requires to limit leakage to the case.

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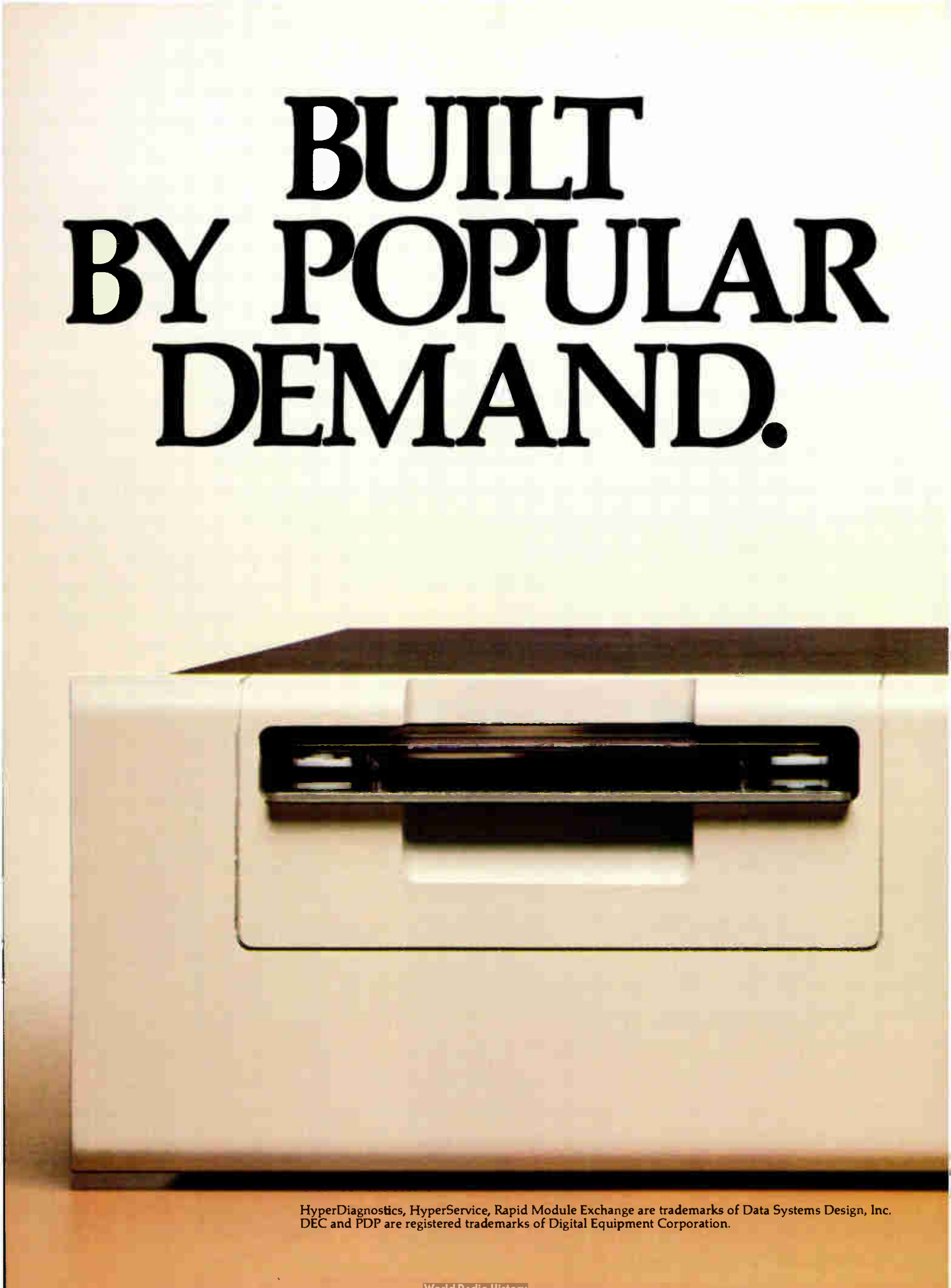
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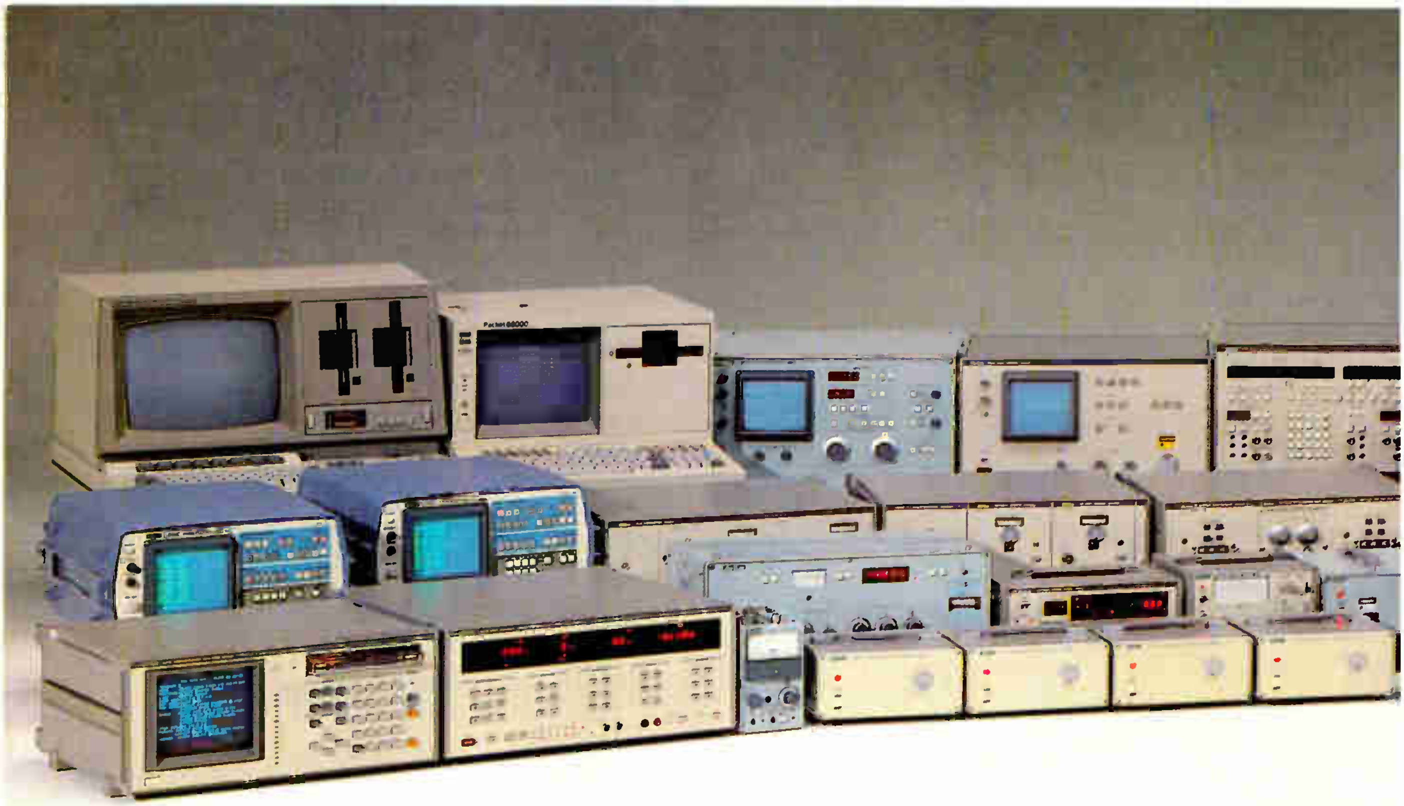

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Whether it's an Anritsu electronic voltmeter, a network analyzer or a complete GPIB-based automatic test system, you'll find a basic field-proven ruggedness built in. And you'll find controls that actually make sophisticated measurements simpler to perform.

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Circle 81 on reader service card

How to turn data you can see

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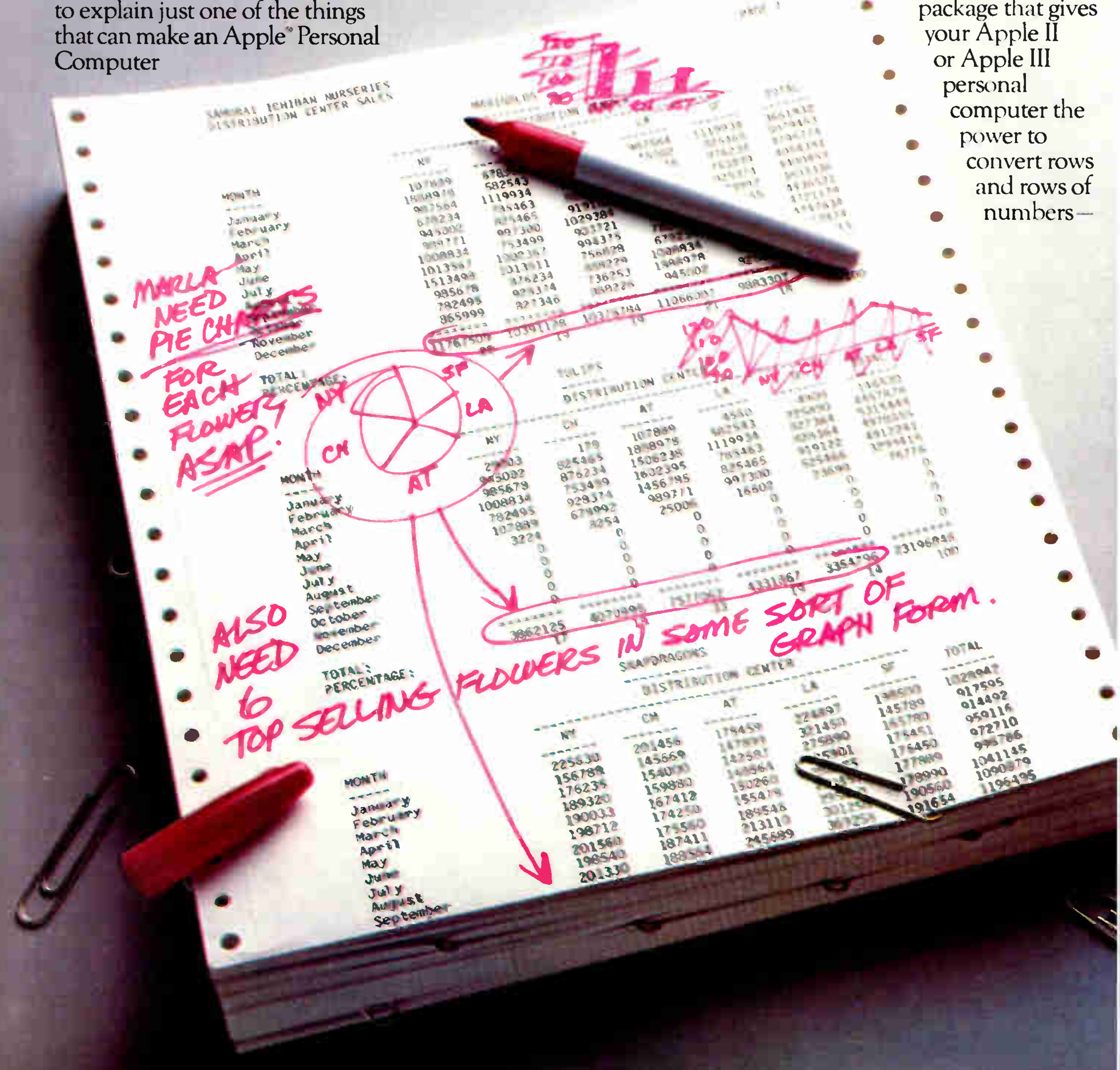

a sea of data into

or pounds of printout—into one simple, colorful, comprehensible illustration.

And that gives you the power, for example, to thoroughly understand relationships and comparisons in a complex market analysis. Without having to spend hours sifting through

Horizontal bar graph (a unique feature) makes it easy to compare the profitability of six different products – from periwinkles to petunias.

dull data—armed with little more than a ruler, a compass and a few not-so-magic markers.

With Apple Business Graphics, all you do is enter the data or transfer it directly from your VisiCalc® model or a number of other computer files. Your Apple will take it from there.

Helping you to get the big picture in a variety of ways. Line or area graphs, bar graphs, pie charts or scattergrams.

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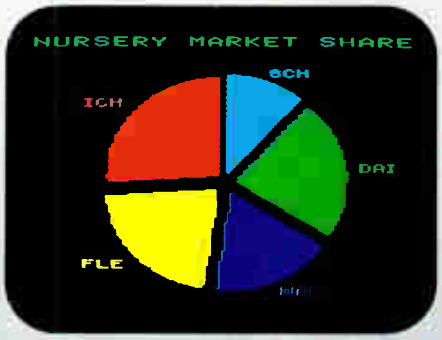
Moreover, sophisticated Apple features like exploded views,



To get the overall market share picture, (and any other percentage related data) Ichiban management consults this easy-to-digest pie chart.

unlimited overlays and floating titles allow your displays to be remarkably flexible.

By combining Apple Business Graphics with various slide-show packages, charts and graphs on your monitor can easily be converted into impressive slides and transparencies.

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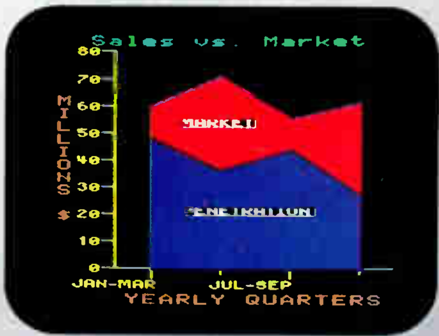

With up to six colors per graph, employees can easily see just how their annual sales blossomed relative to the rest of the market.

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Circle 83 on reader service card

500 Watt Switchers

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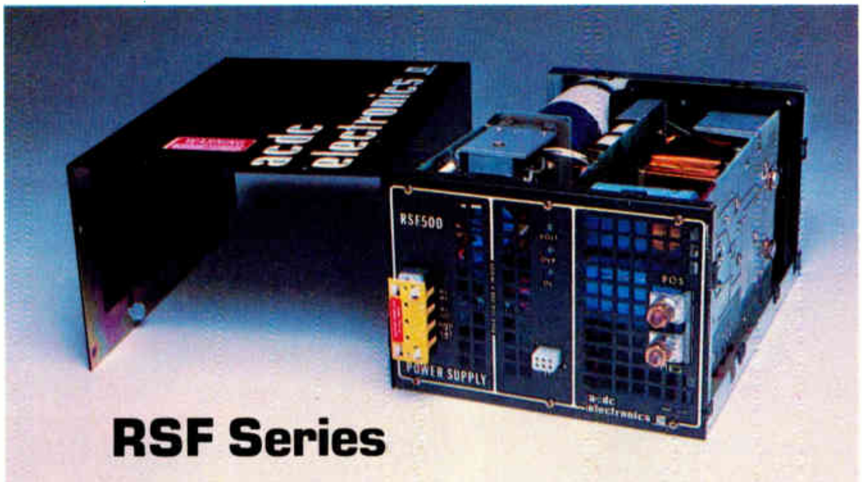

Sub-Modular construction, an ACDC exclusive, assures high MTBF and low MTTR. The latest LSI inverter circuitry, power semiconductors and fault/error detection IC'S reduce parts count for a truly modern, cost effective design. Quality is assured through a 48-hour burn-in and hard copy test data with every unit. RSF units are also available with an optional filter to meet FCC 20780 and VDE 0871 requirements. At about a dollar per watt in OEM quantities, you can't beat it.

Feature	Function	Benefit
Sub-modular construction	Eliminates internal wiring; lowers production cost.	Higher reliability, low MTTR; easy to test and trouble shoot. Lower cost; quick delivery.
Design based on proven product.	The best features of our highly popular "RS" and "EAGLE" series in a new 500W package.	Low risk . . . a new product with proven reliability.
Proportional drive	Switching transistor drive circuit.	Switching Transistor failure does not damage control circuit. Few components, thus higher MTBF and lower cost.
A complete 500W family	Singles, dual, triples and quads.	One supply to replace multiple supplies or upgrade system.
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5	100A
12	42A
15	35A
24	21A
28	18A
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5	80A
12	33A
15	27A
24	17A
28	15A
HI-POWER OUAL OUTPUT $739.00	

RSF 502 DUAL OUTPUT 500W MAX.		
OUTPUT VOLTAGE	MAX. CURRENT RATINGS IN AMPS	
	OUTPUT 1	OUTPUT 2
2	N/A	16A
5	80A	16A
12	33A	16A
15	27A	14A
24	17A	8A
28	15A	7A
DUAL OUTPUT $650.00		

RSF 503 TRIPLE OUTPUT/RSF 504 QUAD OUTPUT 500W MAX.				
OUTPUT VOLTAGE	MAX. CURRENT RATINGS IN AMPS			
	OUTPUT 1	OUTPUT 2 & 3	OUTPUT 4	SEMI-REG. OUTPUT 4
2	N/A	8A		
5	80A	8A	5A	
12	33A	8A	2A	
15	27A	7A	2A	
24	17A	4A	1A	
28	15A	3.5A	1A	24V @ 4A 6A PEAK
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Circle 84 on reader service card

Combo interconnect reduces stress on chip-carriers

by Kevin Smith, Senior Editor

The carriers are first bonded to a flexible circuit and then mated to a rigid metal mounting structure

Flexible circuits, traditionally used to replace bulky cable harnesses in military and avionics systems, may soon be taking on a new role as an interconnection medium for all kinds of surface-mounted components. Teamed with an aluminum or copper sheet for rigidity and to carry heat away, they have many attractions—the combination provides reliable bonds, good thermal dissipation, and high interconnection densities.

Independently of each other, two British companies, Welwyn Electric Ltd. in Bedlington, Northumberland, and interconnect consultants SB Enterprises (Electronics) Ltd. (SBEEL for short), in Winnersh, Berkshire, have developed an interconnection technology based on this approach and are in process of filing patents. They are also supplying prototypes to British Telecom's Martlesham Research Laboratories, which is running trials on various surface-mounted technologies.

Basics. Like the other contenders in these trials, SBEEL and Welwyn have delivered a single Eurocard board with 48 kilobytes of erasable programmable read-only memory packed onto a substrate measuring 6 by 4 inches. That density could easily be increased fourfold by switching from the 2-K-by-8-bit E-PROMs used to denser chips.

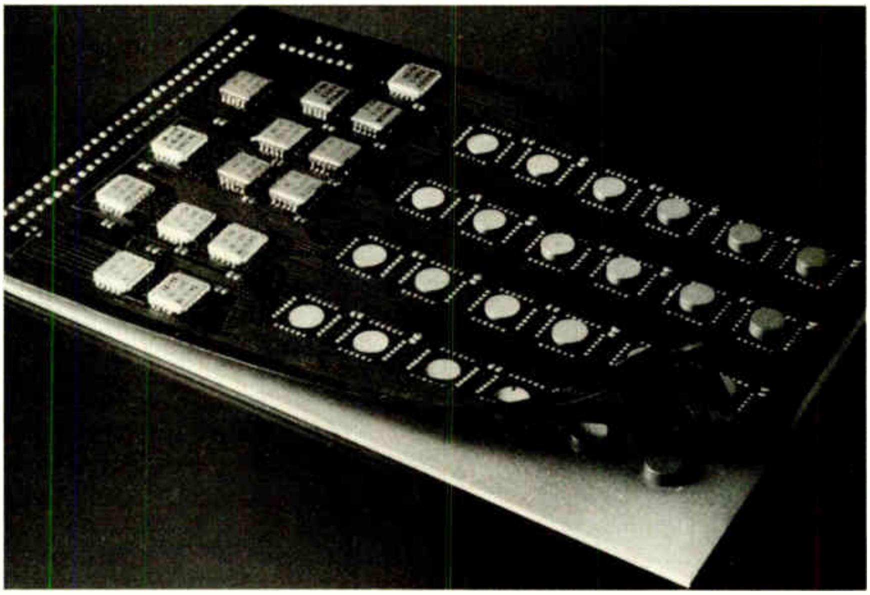
A snag is encountered with surface mounting, however, when a reliable solder connection has to be provided between the leadless chip-carrier and the substrate. The different thermal expansion rates of the two surfaces can stress solder bonds badly enough to fracture them. But a flexible substrate can accommodate such expansion, ensuring a highly reliable bond.

However, there remain the problems of providing a rigid mechanical mounting structure and of dissipating the heat from the chips. The solution for both SBEEL and Welwyn is a separate aluminum or copper sheet with a number of studs formed in its surface. Each stud protrudes through a hole punched in the flexible circuit to make contact with the underside of the chip-carrier.

During manufacture, chip-carriers are reflow-soldered to the flexible circuit. Then the combination is defluxed—an operation that is easier than with conventional means because of the holes beneath each chip-carrier—and the loaded flexible circuit is placed on its heat sink.

Differences. The companies part ways on how to to hold chip-carriers in place. SBEEL flash-solders them, whereas Welwyn contains the chip-carriers by clipping on another flat sheet of aluminum to form a strong sandwich construction only a few millimeters thick.

With the Welwyn approach, two or more assemblies can be stacked together, omitting the flat overlay metal sheets, so as to create a compact, thermally efficient structure with flexible interconnection at each level. At present a two-layer flexible-circuit laminate is used, but, says Peter Kirby, director of research for



Flexible sandwich. Solving the problem of thermal-expansion stress on solder joints, chip-carriers are bonded to a flexible circuit, which accommodates expansion. Rigidity is provided by an aluminum or copper sheet with studs protruding to make contact with the chip-carriers.

Welwyn, extra circuit layers can be added while still retaining maximum flexibility.

There are other differences of detail between the two approaches. For example, SBEEL injects an additional silicone rubber layer for cushioning between the laminate and the heat sink during the final stage of manufacturing.

A further refinement worked out by SBEEL for one computer company is a water-cooled heat sink, according to founder-director Stan Bracey. Instead of a flat-plate sink, a metal cavity with an inlet and outlets for water circulation is used. The firm devised a self-sealing valve so that the structure could demount.

France

Switchless UV laser boosts reliability

Engineers at the Compagnie Général d'Electricité's Laboratoires de Marcoussis have found a way to vastly extend the life of ultraviolet gas lasers while also doubling their efficiency. Such an improvement could help high-power UV lasers fulfill their promise in semiconductor production, making feasible such achievements as submicrometer lithography and precise annealing of an entire wafer in a single pass.

CGE engineers achieved their goals by eliminating the most unreliable component, the spark-gap generator used to break down the gas in the laser and initiate its discharge. Once the gas has been ionized, causing it to lase in the UV region, the electric discharge is high—dissipating 100 megawatts in 100 nanoseconds. Consequently, the laser system is only good for around 10^7 or 10^8 shots, equivalent to 14 to 140 hours of continuous use.

Optically exciting. Instead of hitting the gas with a brute-force voltage above its breakdown threshold, CGE engineers now bring it to near its breakdown (ionization) voltage, then induce self-discharge by exciting the gases optically. In effect, this is a switchless technique, in contrast to the conventional method in which the spark-gap generator serves to switch the laser on. With the spark-gap generator eliminated and solid-state electronics introduced, reliability is increased by at the very minimum a factor of 10.

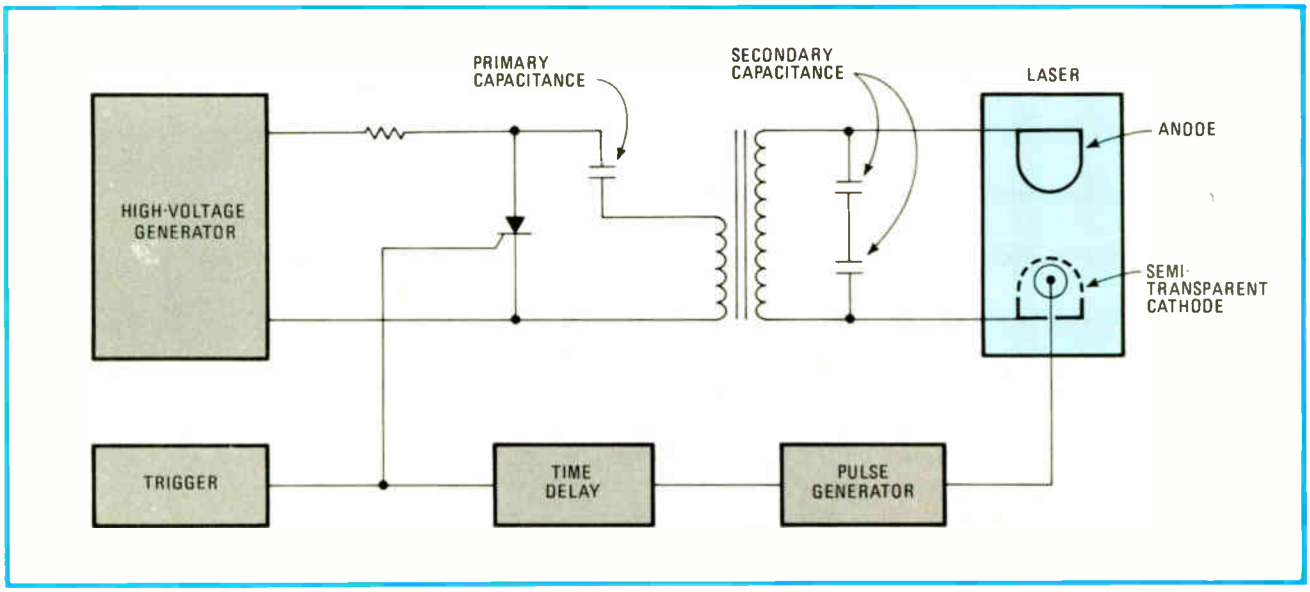
"Using a long preionization pulse and a short voltage rise time, the spark gap has to withstand something like 100 mW for 100 ns," explains Bernard Lacour, the engineer coordinating development of the system at the labs in the Paris suburb of Marcoussis.

The first CGE experiments were carried out on a laser with electrodes 20 centimeters long and spaced 5 to 10 millimeters apart. Serving as the energy store was a copper water line, in which water serves as the dielectric. This arrangement further adds to the reliability, as the dielectric in a standard condenser can deteriorate.

Self-switching. Basically, the switchless mode works thus: the very-low-impedance water line is connected directly to the two electrodes of the laser. A continuous rising electrical voltage is applied up to 8 kilovolts, a value just below the discharge threshold of the gas.

An impulse generator then applies an electrical impulse to the cathode, and the resulting photoionization creates the conductivity necessary to start the discharge. This procedure results in the self-switching of the laser, which can achieve up to 200 pulses per second with preionization energy consumption less than a tenth of the laser energy.

Operated in this way, the supply-voltage rise time is 10 microseconds and the preionization pulse is 10 ns. Peak power is 500 kilowatts during rise time and 200 kW during preionization, compared with 100



Water power. Using water lines—copper condensers with water dielectric as energy store—and eliminating the spark gap by manipulating the preionization and voltage discharge enables CGE to increase the reliability of its ultraviolet laser tenfold while greatly extending its life.

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N-CHANNEL	IRFD 1Z0	100	2.4	0.5	4.0	1.0
	IRFD 1Z3	60	3.2	0.4	3.2	1.0
	IRFD 110	100	0.6	1.0	8.0	1.0
	IRFD 113	60	0.8	0.8	6.4	1.0
	★ IRFD 120	100	0.3	1.3	10.4	1.0
	★ IRFD 123	60	0.4	1.1	8.8	1.0
	★ IRFD 210	200	2.4	0.6	4.8	1.0
	★ IRFD 213	150	1.5	0.45	3.6	1.0
P-CHANNEL	★ IRFD 9110	-100	1.2	-0.7	-5.6	1.0
	★ IRFD 9113	-60	1.6	-0.6	-4.8	1.0
	IRFD 9120	-100	0.6	-1.0	-8.0	1.0
	IRFD 9123	-60	0.8	-0.8	-6.4	1.0
	★ IRFD 9210	-200	3.0	-0.4	-3.2	1.0
	★ IRFD 9213	-150	4.5	-0.3	-2.4	1.0

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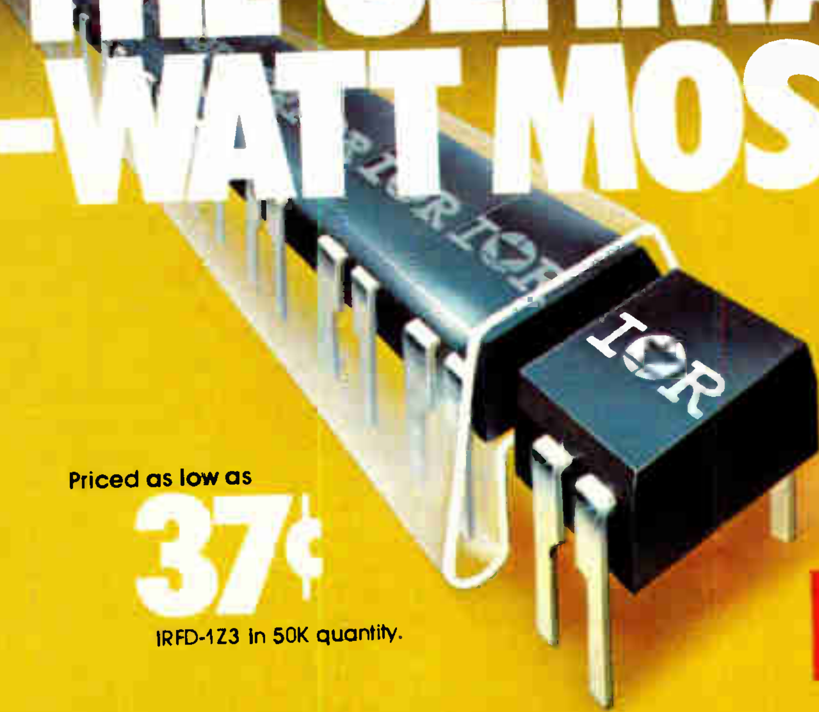

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Circle **87** on reader service card

MW and 20 kW, respectively, in standard switched operation.

What's more, the switchless operation achieves nearly double the under 1% laser efficiency of the standard method for all the gases tried—xenon chloride, krypton fluoride, and nitrogen.

Now the company has moved on to a larger laser with 30-cm electrodes and with 1-cm spacing, using six water lines. This setup increases the energy-storage capacity to 10 joules, or 10 times that of the smaller laser. According to Lacour, the life span of this laser's electronics would be measured in years when it was operated at 50 pulses per second.

Future research will concentrate on scaling the present setup to higher energies. Also, because the larger laser can be equipped with a gas circulation loop, the CGE engineers plan work that will increase the repetition rate. –Robert T. Gallagher

Great Britain

Local nets hitch up with a satellite

A satellite can bounce wide-bandwidth point-to-point links over intercontinental distances. A local network can hook up many users in a single building, or other relatively small area, to a wideband data link. Two such compatible technologies should therefore readily combine to extend the local-network concept over a wide geographical area.

British researchers have made just that association in Project Universe, a $6 million experiment largely sponsored by the Science and Engineering Research Council (SERC). Currently under way, it links 150 computers at six sites throughout the UK as if they were connected in a local network. The goal is to discover the problems of linking local nets in this way and to ascertain the kinds of wideband services users really need.

The European Orbital Test Satellite is being used to link the nets, with British Telecom's packet-switched service acting as a backup. For the longer term, British Telecom has announced plans to establish its integrated digital network (IDN) that could provide the bandwidths needed to connect local networks.

Project Universe uses 3-meter dish antennas at six of its test sites—the universities of Cambridge and of Loughborough; University College, London; Marconi Research Centre in Chelmsford, Essex; British Telecom Research Laboratory at Martlesham Heath, Suffolk; and SERC's Rutherford Appleton Laboratory at Chilton, Oxfordshire. A high-speed terrestrial link connects the network at University College with the seventh test site, Logica Ltd. in London.

Operating in the 11-to-14-gigahertz band, Project Universe's satellite channels provide a 2-megabit-per-second link to the satellite. This performance is well matched to the 2-to-10-megahertz bandwidth of the Cambridge Ring. Developed at the university, the Cambridge Ring is a low-cost, modular local net [*Electronics,* Aug. 28, 1980, p. 80].

A General Electric Co. Ltd. 4065 computer links each satellite terminal to its local network. Using computers of such power could be overkill in a commercial net, but in an experiment like Project Universe, they can be quickly reprogrammed to accommodate any network changes.

Teletex test. The project will serve as a testbed for new communications technologies. British Telecom's Martlesham research center wants to evaluate the application of wideband data links of this kind to teletex electronic-mail and videotex services. Logica will be conducting experiments on data encryption using the encryption standard devised by the U. S. National Bureau of Standards.

Loughborough University will be carrying out investigation into facsimile and slow-scan TV transmissions. Cambridge University is working out a system of authentication that ensures that only authorized users gain access to the network's resources. And University College has a key role in monitoring the network's hardware and software availability.

Coordinating the program is the government's Rutherford Appleton Laboratory. Of course, university researchers will be able to access any computer on the network as if it were connected to their local net.

One of the biggest attractions of such a net is its ability to transfer bulk data files rapidly. This feature is particularly important for updating records held simultaneously at several sites. Instead of transmitting file changes as at present, the update's originator could broadcast a new file recorder to all users simultaneously, says Roger Needham of Cambridge University's Computer Science Laboratories. The Martlesham research center, in particular, could use this to update Prestel videotex data bases.

Slimmed-down protocols. To define the service, researchers had to create a set of protocol procedures that would not bog down transmissions and so would capitalize on the performance offered by the hardware. Thus the protocols assume that the error rate of the satellite link will be very low and that retransmissions due to errors may be treated as an exceptional condition.

Also, there is no flow control on the network; so when a gateway buffer overflows, the data block is dumped and a retransmission is triggered if required. The transport protocols adopted conform with those in the International Standards Organization's open-systems interconnection reference model for networks.

Eventually there will be three transmission options. One will set up a point-to-point virtual circuit, another will provide a broadcast facility so that all sites will receive a message, and a third will be a one-shot facility allowing a user to interrogate a remote site and receive a single-shot reply. –Kevin Smith

Japan

Ink-jet printer offers greater color range

Microdot ink-jet printers may be the solution to the growing demand for considerable brightness gradation in

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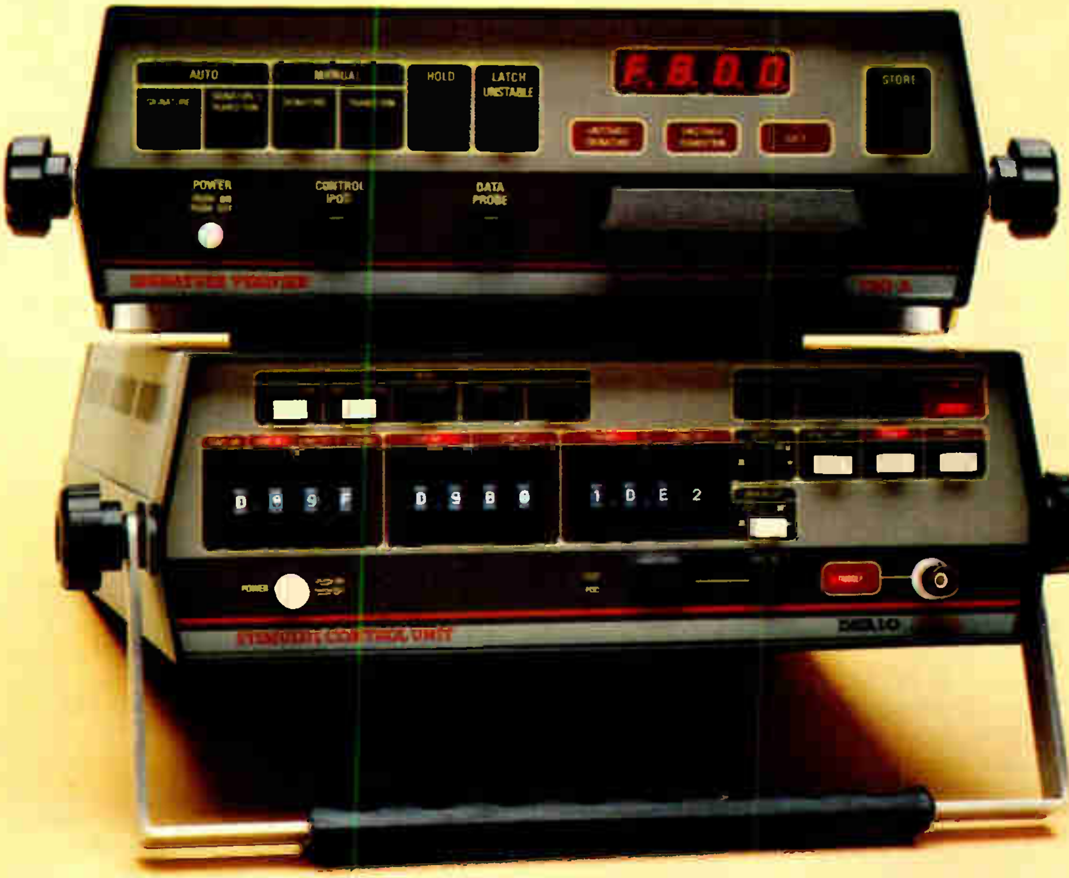

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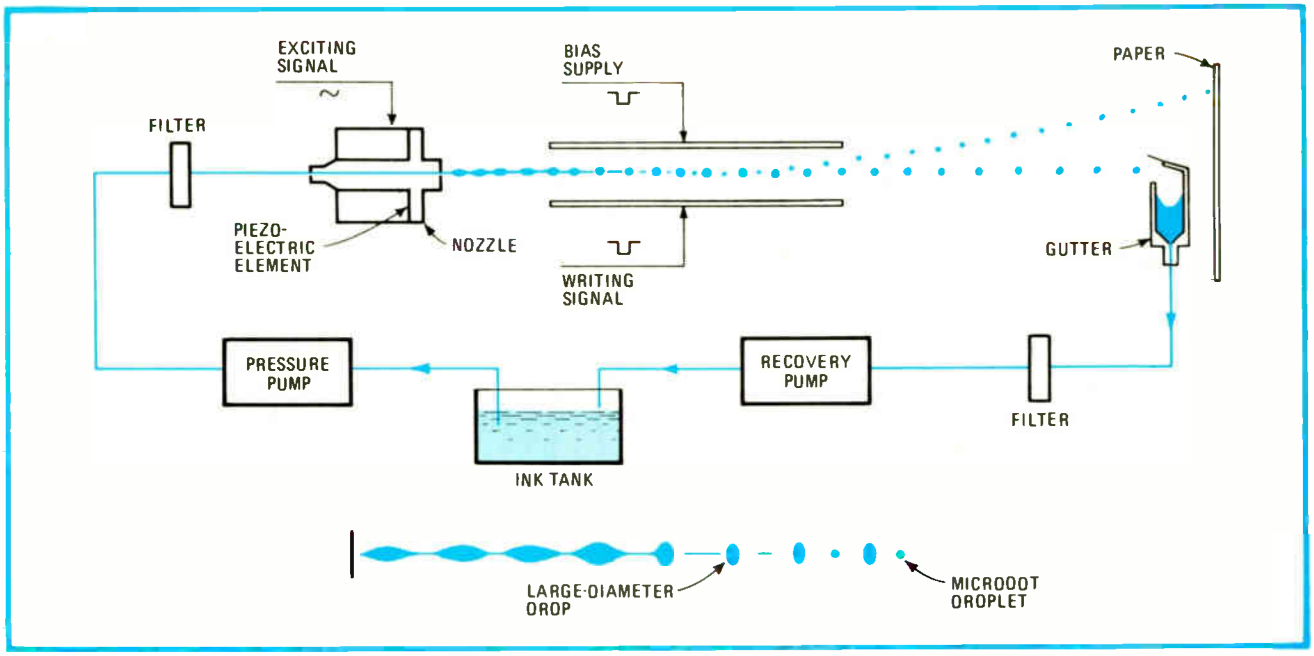

Excitable. Color inks, fed under pressure to four nozzles, are excited with an ultrasonic signal. This produces a standing wave on the stream of ink, causing it to break up into large and small drops. Writing signals on a pair of electrodes are timed to charge the microdrops. These are deflected by the electrodes' constant-voltage difference, clear the gutter, and strike the paper. The uncharged drops are collected and recycled.

color copies made from electronic cameras, TV signals, and graphics terminals. Increasing that likelihood is a new type of ink-jet printer, developed by Hitachi Ltd., that offers higher resolution and speed than other units already announced.

The new printer will have a density of 16 dots per linear millimeter, compared with the 10 dots/mm of conventional ink-jet units. High dot density is necessary because the color gradations are controlled by varying the number of ink dots in a unit area corresponding to each individual picture element.

In general, for a given dot density, the tradeoff for more gradation steps is lower resolution. The user of the new printer may select 16, 32, or 64 gradation steps. Individual dots in each pixel are not visible at normal viewing distance.

Four ink jets. Developed at the firm's research laboratory in Hitachi, Ibaragi Prefecture, the printer uses four ink jets, one for each of the three process colors—yellow, magenta, and cyan—and a fourth for black. Ink is fed under pressure to a nozzle excited with an ultrasonic signal.

Ultrasonic excitation produces a standing wave on the stream of ink issuing from each nozzle, breaking it up into individual drops. At this point there is a tendency for a small satellite drop to form between each pair of regular drops because of higher-order harmonics. The Hitachi printer uses these satellite drops for printing, discarding the regular ones.

Thus the system is designed for stable generation of the satellite drops—a setup that is the direct opposite of the conventional ink-jet printer, in which the satellite drops are parasites to be eliminated.

The microdrops are both charged and deflected by a single electrode pair (see figure). In contrast, conventional systems use a single electrode to charge the ink drops and then a pair of electrodes to deflect them.

Writing signals on the electrode pair are timed to charge the microdrops when printing is desired. The drops are deflected by a constant-voltage difference between the electrodes, clear a gutter, and strike the paper. The uncharged microdrops and the large drops between them strike the gutter and are recycled.

Because the uncharged large drops shield successive microdrops from each other, every microdrop is available for printing. This feature produces double the printing rate of conventional ink-jet printers for the same excitation frequency and printing density. In conventional printers, alternate drops must be left uncharged to provide shielding between charged drops.

Large nozzle. In the prototype printer, the nozzles are a whopping 65 micrometers in diameter, large enough not to clog. Microdrops are only half to three quarters the nozzle's diameter, though, compared with 1.5 to 2 times the nozzle's diameter for regular drops.

These parameters leave sufficient margin for Hitachi to state that it will develop an even more advanced printer with a density of 40 dots/mm after it produces production models of the 16-dot/mm printer. The 40-dot/mm printer will have a nozzle of 30 μm in diameter, the same size as that in conventional ink jets of 10-dot/mm printers.

The 16-dot/mm unit will print one letter-size page simultaneously in four colors in two minutes, about the same speed as a conventional 10-dot/mm ink-jet color printer. The 40-dot/mm printer will require about six minutes a page. —**Charles Cohen**

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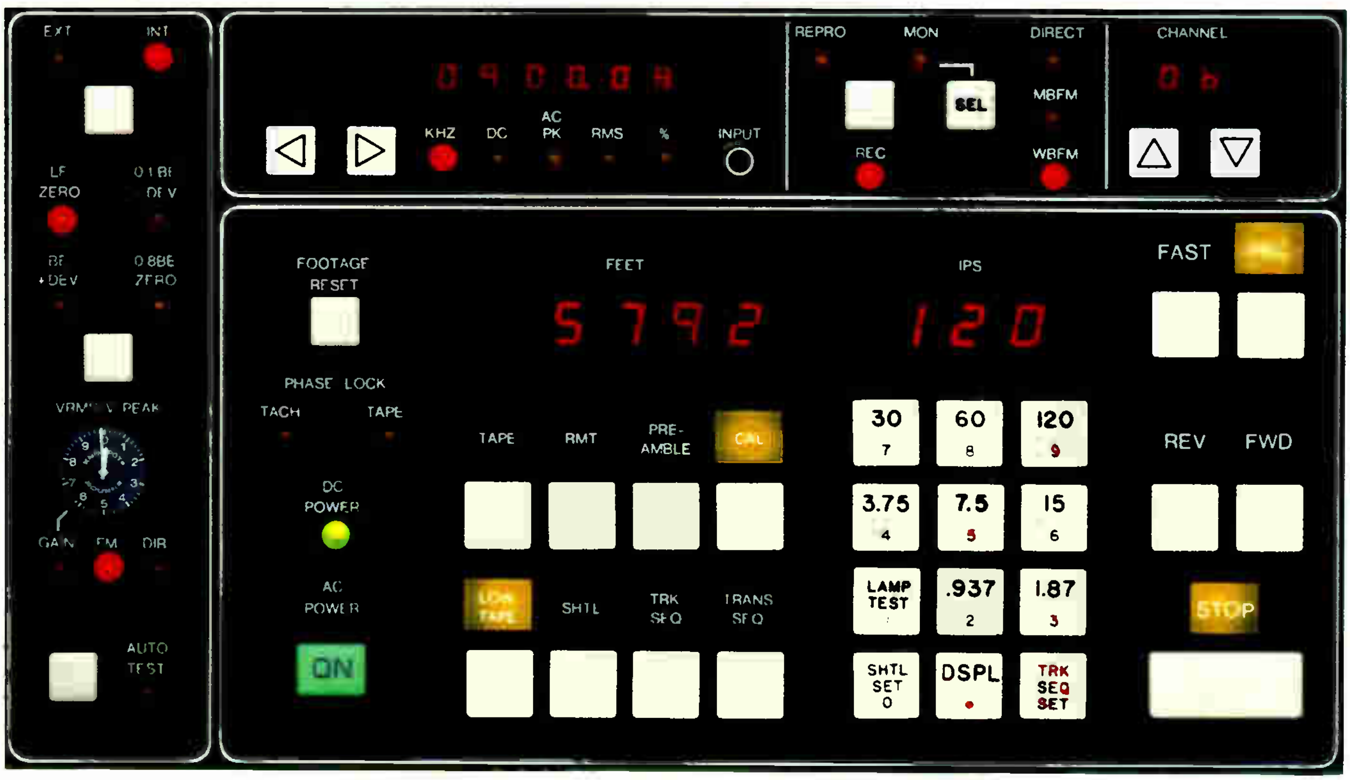

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Interest swells in bypassing phone net

Competition for traffic attracts users of all sizes as well as suppliers, with newly divested phone companies the potential losers

by Roger J. Godin, Communications & Microwave Editor

Say "bypass" to most people, and they will associate it with heart surgery. However, for those who are in the telecommunications business, the word has taken on a new meaning. To them, it refers to the opportunity of companies to develop communications networks independent of the local telephone company or to connect directly to long-distance carriers, often with significant savings.

The nascent bypass market is broad and includes several technologies, such as digital microwave radio, two-way cable, direct satellite stations, and cellular radiotelephone. Its growth has been spurred by three factors: Federal deregulation; the proliferation of word processors, personal computers, and other modern office equipment; and the aggressive marketing of private branch exchanges and similar telecommunications equipment. All this has heightened corporate awareness of, and hence sophistication in, voice-communications management.

Added to that, the industry is in the throes of American Telephone & Telegraph Co.'s divestiture of its local operating companies, leaving many questions about the impact of such bypass networks on local phone rates. The upcoming Federal Communications Commission decision on access charges will answer some of those questions. However, many bypass alternatives are completely beyond the reach of regulators and will force the divested operating units to acclimate themselves to open-market competition for local service faster than they might have expected.

Along with various other service rates, access charges—the FCC-set rates for a long-distance carrier's interconnection to the local phone company's customer network—will be a major factor in the economic viability of bypass communications. But there are other elements. For example, in the most readily available bypass technology—digital microwave radio in several frequency bands, including the 10.5-gigahertz range set aside by the FCC for Digital Termination Service (DTS)—the cost for equipment and operation of 9.6- and 56-kilobit-per-second channels is at present barely competitive with that of leased phone lines.

However, telecommunications users are realizing more and more that the benefits of having complete control and management of their telecommunications resources go beyond the basic cost per call. As a result, many are purchasing PBXs, concentrators, multiplexers, gateways, and other telecommunications equipment perviously marketed only to the telephone company. According to Bob Harcharik, vice president for data services at MCI Inc. in Washington, D. C., the fact that only about 10% of the present long-distance traffic is data is a main reason that microwave radio is not cost-competitive with leased phone lines. If the inclination of companies to buy intelligent work stations and communications equipment continues to grow, a profound shift to data traffic could make that bypass alternative more attractive.

This trend appears already to be a strong one in another microwave frequency range, the 21-to-24-GHz K band. General Electric Co.'s microwave link operation in Owensboro, Ky., makes line-of-sight equipment called the Gemlink that can send T1 (1.544 megabits per second) or T1C (3.152 Mb/s) channels over a distance of several miles.

Cost factor. The 10.5-GHz DTS frequencies allocated by the FCC are catching on more slowly because of the relative cost tradeoffs with leased lines. However, 10 of the soon-to-be-divested operating companies have applied for DTS licenses, and private companies such as Tymnet Inc. of Cupertino, Calif., have already been licensed. Equipment is available from several companies, including TXR Inc., a subsidiary of California Microwave of Santa Clara; LDD Inc., a subsidiary of M/A-Comm of Burlington, Mass.; and Nippon Electric Co. of Tokyo. The typical DTS system is offered as either a number of 64-kb/s pulse-code–modulated voice channels or a 1.544-Mb/s T1 carrier. No equipment has yet been installed; William Combs, vice president of marketing at GTE Telenet in Vienna, Va., sees it as a cost-versus-traffic problem: although a DTS station will cost the customer about $11,000, the long-distance common-carrier equipment can typically run around $1 million.

This cost differential will require common carriers to have approximately 20 DTS users per installation, says Combs. That requirement, he believes, will probably result in the existence of one or two major DTS providers servicing only the major markets, leaving smaller markets to leased phone lines or other bypass technologies.

Combs, with Harcharik of MCI and others, expects two-way cable will be the most significant long-term bypass approach. The reason for this is that cable can solve the two main problems of microwave radio: bandwidth and interconnectivity.

More channels, jobs. A standard 6-MHz television channel could accommodate nearly 1,000 voice channels. On the other hand, even at the upper K band, microwave equipment using the standard 64-kb/s pulse-code–modulation rates for voice traffic can carry only 48 or 96 voice channels. In addition, cable systems have the potential for providing a wide variety of services such as videotex, electronic funds transfers, and electronic mail.

The major bottleneck for two-way cable is the lack of switching equipment that is truly competitive with telephone switching; such gear is needed to make connections on a shared transmission medium. However, experiments with switched two-way cable are under way. In Omaha, Neb., MCI is working with Cox Cable Co., and in suburban Chicago, a system is being built by Times Fiber Communications Corp. and Multimedia Cablevision Inc. using fiber optics and a digital addressing architecture that could handle full two-way service increase [*Electronics*, Feb. 24, p. 42].

Other bypass alternatives, such as cellular radiotelephone and stations linking sender and receiver directly by satellite, may have much longer-range implications, but for now their applicability is limited. Direct satellite links are proven and in service now as part of the internal telecommunications networks of some of the largest corporations in the world, but the high cost of transponders and large data volume required make such systems impractical for most users (see "Who's wooing whom with data services?").

Cellular radiotelephone is a potentially significant bypass technology, but until extensive cellular networks are operational, the number of users will be too small for entirely bypassing the local phone network. In addition, most cellular systems are expected to be closely linked to the local phone companies so that calls to fixed stations will be economical.

Parking space. A final factor in the bypass equation will be the so-called high-technology office park. These developments, under construction in several cities, are basically leased office parks that provide advanced computer or communications systems installed by the landlord.

A major advantage, according to Ken Robinson, a policy adviser in the U. S. Department of Commerce, will be the fact that satellite links have already been ruled outside the authority of state public-utility commissions and, since such services are usually considered enhanced, they are also beyond FCC regulation.

With concentration of the purchase of information-preparation equipment such as multiplexers and packet assemblers, and management of the telecommunications network under the landlord's authority, bypass technology may become affordable to users of all sizes. □

Who's wooing whom with data services?

At present, only large organizations—those that spend around $1 million per year on communications—can afford to bypass the telephone company. But, as the amount of data modern companies produce increases dramatically because of personal computers and other office-automation devices, the number that might want to join the bypass group is becoming significant enough to attract attention.

There are some heavyweights vying for the private-net dollars. Naturally, there is American Bell Inc., whose Dimension System 85 and Net/1000 offer complete office automation and large network services. Just as naturally, there is IBM Corp., whose Information Network competes directly with Net/1000. What's more, its recent Document Content and Document Interchange enhancements to the System Network Architecture, plus its technology program with Mitel Inc. of Kanata, Ont., Canada, for private branch exchanges, give IBM even more muscle. Then, as part of the deregulation that frees American Telephone & Telegraph Co., International Telephone & Telegraph Corp. is permitted to compete in the U. S. market and is doing so aggressively from a strong position in overseas telex and telephone markets. United Technologies Corp. also has been positioning itself for a share by buying most of Stromberg-Carlson, a PBX and central office manufacturer, and ComDev, a call- and message-accounting-equipment firm.

In addition, many companies involved with satellite systems, such as M/A-Comm and Harris Corp., are now marketing private turnkey communications networks that include on-site local loops and satellite links. They hope to use their experience in satellite networks as a wedge into the teleconferencing and office-automation business. Finally, there are numerous cooperative programs involving computer and telecommunications companies that are aimed at the distributed-computer and communications network-applications. Perhaps most significant are the moves by Northern Telecom Inc., Nashville, Tenn., in making its Open World network compatible with Digital Equipment, Sperry Univac, and Data General computers. —**Roger J. Godin**

Solid state

IC makers, users adopt ship-to-stock

Quasi-partnership aims to cut cost and time of incoming inspection, as integrated-circuit makers boost quality and reliability efforts

by Larry Waller, Los Angeles bureau

Since the late 1970s, the quality and reliability of U. S.–made semiconductor circuits have been sticky issues for manufacturers and their customers. What could have been a partnership working toward a better end-product often split up over device quality. The touchiest issue of all was the thicket of expensive and time-consuming testing and incoming inspection steps that repeated procedures already followed by the manufacturer, also at high cost. Neither side liked the duplication, but quality competition from Japanese firms left little choice.

However, such duplication is fading, influenced by steady device improvements that set the stage for a much closer relationship. Still in its early development, the relationship is more nearly a partnership focusing on an ambitious goal: drastic reduction and, soon, elimination of excessive incoming part testing.

Besides a closer working relationship, the other crucial step in the alliance is a major effort on the part of manufacturers to build in higher quality from the start. These developments have even picked up a trendy name: "ship-to-stock," which signals so much confidence on both sides that components can be delivered directly to inventory.

The term, however, is not universal; some major firms think it promises too much too soon. Motorola Corp.'s Semiconductor Products Sector, for example, describes its effort as a Certified Parts Program. General Motors Corp.'s Delco Electronics division, a massive buyer, calls it No-Inspection Verification. Intel Corp.'s program has no special name.

By whatever description, all hands agree, eliminating testing is a development of importance for the U. S. industry, one that has the potential to change the patterns of component procurement. Centering solidly on cutting costs and improving products, its advantages are compelling on both sides—so much so that virtually the entire semiconductor industry bubbles with enthusiasm.

A typical opinion comes from Joe Flood, veteran reliability and quality executive who heads this program at Motorola's Bipolar division in Mesa, Ariz. "There's nothing to lose and everything to gain," he says. Flood's counterparts at other major houses echo his assessment.

For customers, cost benefits stand out. Burning in 64-K memories can run to 50¢ apiece; less complex parts cost 25¢. With big users buying hundreds of thousands each month, it is easy to understand why impetus for ship-to-stock comes first from them.

Furthermore, eliminating customer testing frees parts for immediate use, enabling inventories to be smaller and turnover faster. Finally, since new components often mean new testing equipment and procedures, this customer overhead also can be reduced. One customer of National Semiconductor Corp., for instance, estimates a $1 million outlay just to set up testing of integrated circuits in one new product line.

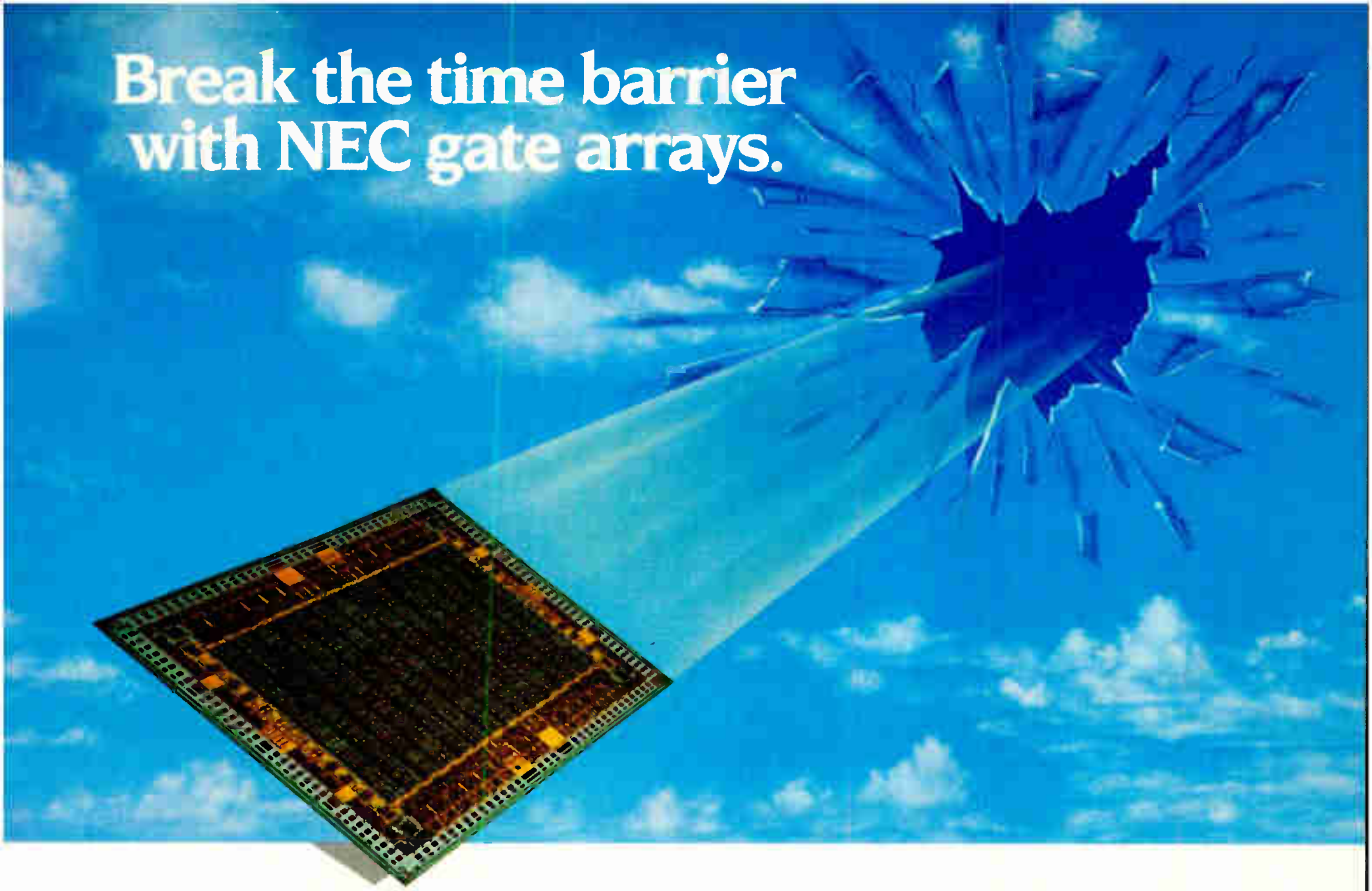
Reticent users. However, users are much less willing to talk about ship-to-stock than are suppliers. The main reason, sources speculate, is that several big firms announced years ago they were closing in on this target, but they never got the job done. One example is Delco, which sought to have up to 30% of its integrated circuits shipped this way by the end of 1981. But that goal still eludes it.

However, the identities of major users leading the way are well

Parts must be good for program to work

Ship-to-stock programs can thrive only if supported by semiconductor device quality that steadily reduces failures, measured in defective parts per million. On this score, major U. S. suppliers cut the rate to 1,000 ppm for 1982 from many times that several years ago, estimates Steve Kent, reliability manager at Siliconix Inc. in Santa Clara, Calif. His firm is aiming at 500 ppm by year-end, which is the level he thinks it will take to compete.

Other semiconductor houses report similar goals and results. Motorola Inc.'s Bipolar division in Mesa, Ariz., had a 792 ppm rate at the end of 1982 for all its product lines, and Texas Instruments Inc. of Dallas says its standard low-power Schottky parts had defects of no more than 400 ppm under dc parameter tests. At Signetics Inc. in Sunnyvale, Calif., overall quality levels were less than 1,000 ppm, with the best devices coming in at 200 ppm. In El Segundo, Calif., International Rectifier Corp.'s Hexfet power devices now carry a 341-ppm quality rating. National Semiconductor Corp. of Santa Clara, Calif., gives a single figure for its entire product mix, from simplest discrete part to most complex IC: 150 ppm. –L. W.



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known. International Business Machines Corp. is deeply involved, as are Digital Equipment Corp., Hewlett-Packard Co., and Tektronix Inc.

HP confines its comments to noting that each of its 50 divisions makes its own decisions on such matters, and "you'll find it going on around the company" but not as formal corporate policy, says a spokesman. Tektronix is just beginning to set up a ship-to-stock program, according to a spokesman.

Other boons. Although not immediately apparent, semiconductor makers see advantages, too, beyond the obvious one of removing a prickly issue. For one, wiring in closely to users gives manufacturers access to field-failure data that in the past has been hard to get on a systematic basis. Top executives, in fact, have called this lack a major weakness of U. S. semiconductor firms competing with the integrated Japanese companies where such feedback is common.

A big leap for U. S. firms, ship-to-stock is old hat for those integrated Japanese firms with semiconductors and end products under one umbrella. Hitachi Ltd.'s Semiconductor division says its customers started asking for it four or five years ago.

Ship-to-stock's time has apparently arrived, an evolutionary advance that has resulted from pressure to improve devices and close the performance gap with the Japanese, most sources agree. The latest quality figures for U. S. firms indicate substantial improvement, with defective parts per million at less than 1,000 (see "Parts must be good for program to work," p. 96).

Paradoxically, improved quality levels poses a thorny technological challenge for most users, points out industry consultant David S. Cochran, vice president and general manager of Integrated Circuit Engineering's Western division in Sunnyvale, Calif. "At 500 ppm, their testing is not that precise. There has to be another way of determining quality."

In the meantime, suppliers have cranked up their quality and reliability efforts. "The key word is partnership," says Motorola's Flood. Adds John Montesi, vice president of quality and reliability at National, "The major work comes from initial setup of the program; the customers can't be reluctant bridegrooms."

Although ship-to-stock relations between vendors and customers are still forming along practical give-and-take lines, more formal programs are taking shape, too. Both Motorola and International Rectifier Corp. of El Segundo, Calif., have outlines for setting up such efforts. Motorola traces certification through a 13-step checklist; International Rectifier lists a sequence of events that traces each phase from the initial decision to the analyzing of field data together.

One question that will be answered only with experience is how much testing users should still do. International Rectifier's vice president of operations, Derek Lidow, argues for "none at the device level after it is qualified. Simply handling them can destroy 400-ppm quality." He recommends that testing do done instead at the board and subsystem level.

Motorola's Flood strongly emphasizes that customers "don't entirely drop testing, if only as an auditing procedure." But it need not be nearly as extensive. Signetics notes that a customer's going in stages from testing every shipment to ship-to-stock arrangement is part of "a trust-building process."

Culls: who pays? Another unresolved puzzle concerns responsibility for failed parts, especially at the product level. Before ship-to-stock, it was the user's responsibility once the part had been accepted. Now, with a partnership, "this is a difficult and maybe a dangerous matter," observes one semiconductor official who declines to be named. "Warranties on parts are out of the question if that makes you liable for failure of the end product."

Finally, there remains the question of whether ship-to-stock parts should command premium prices, since savings to the user are significant. Some companies are willing to pay 5¢ more per part, one manufacturer reports. Others expect ship-to-stock quality free as part of doing business, notes Lidow. Integrated Circuit Engineering's Cochran suggests both sides split any gains. □

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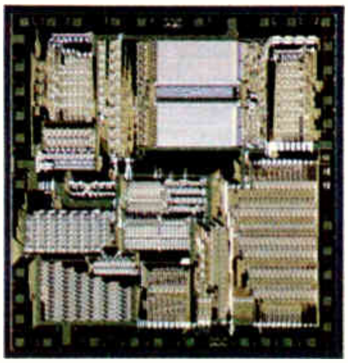

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Trade

U. S. warns NTT to open door wider

U. S. Trade Representative threatens to recommend that Congress end trade agreement if Japanese do not buy more U. S. telecom gear

by Robert Neff, Tokyo bureau

An old bugaboo of U. S.– Japan trade relations is raising its ugly head after two years of dormancy. Nippon Telegraph & Telephone Public Corp., it seems, is not buying enough telecommunications gear from the U. S. to satisfy Washington. If NTT does not dramatically improve its performance soon, U. S. Trade Representative William E. Brock warned in Tokyo in mid-February, Congress may refuse to renew the three-year bilateral government procurement deal the two countries made in January 1981.

Talking it over. U. S. Trade Representative William E. Brock has a warning for Japan's minister of trade and industry, Shintaro Abe.

Under that pact—opposed by the U. S. Electronic Industries Association as too complex and favorable to Japan—the Japanese government agreed to have its telecommunications monopoly give would-be foreign suppliers an equal crack at NTT's annual $3 billion in equipment procurement, a traditional preserve of Japanese suppliers. In return, Japanese companies were given continuing access to U. S. Government procurement, where they have long done some business.

Now Brock is concluding that the agreement has been of "very little value" to the U. S. and is threatening to testify to that effect before Congress. Other American officials say Congress could retaliate, not only by letting the agreement lapse, but perhaps by closing the U. S. telecommunications hardware market to imports. That market earned Japan more than $750 million last year.

"Japan's inflexibility and foot-dragging" in opening NTT procurement "has produced a very sour taste here," says a senior American trade official in Washington. "The time for getting Japan to act positively is slipping away fast," he says, as pressures on the U. S. Government increase from both industry and labor. If the picture does not improve fast, he warns, "the barriers will go up in America, and it will hurt Japan a lot more than it hurts us."

NTT president Hisashi Shinto retorts that Washington's expectations are unrealistically high. He argues that NTT's foreign procurement has doubled during each of the past two years and will at least double again this year from 1982's $37 million, with most of it coming from the U. S. When reminded that this is barely 1% of NTT's total procurement, he snaps: "Don't argue in terms of percentages. We're just at the starting stage. Business takes time." Shinto says Brock did not tell him directly of the possibility Congress would not renew the agreement.

By all accounts, Shinto genuinely wants to end discrimination against foreign products, as does NTT's International Procurement department. They have bent over backward in many ways to assist would-be foreign suppliers [*Electronics*, Dec. 29, 1981, p. 58]. But they have not yet managed to rally NTT's massive and recalcitrant bureaucracy to the same cause. U. S. suppliers say that, once the Procurement bureau decides it likes their products, they get caught in a seemingly endless morass of red tape at NTT's Engineering bureau, which enforces specifications.

Some disappointment. "We've been after NTT for years and are now just at the point where it looks like we'll get some business, but not much," says the Japanese representative of an American company who insists on remaining anonymous. "What we got was a token of their effort to open up." He says he is "definitely disappointed" with his experiences at NTT to date and figures he would not be succeeding at all if his product competed with ones made by the notorious NTT "family" of Japanese telecommunications suppliers.

While that view is probably most representative of American suppliers, it is not unanimous. "NTT has been very sincere in its dealings with us on all issues," says George A. Needham, president of Nippon Motorola Ltd. With its widely publicized contract to sell pocket pagers to NTT and its bright prospects of supplying mobile telephones, Motorola is the Japanese giant's most successful foreign supplier. "Motorola is really dedicated to serving NTT in the manner they want to be served. We're enjoying an excellent supplier-customer relationship with them," Needham says.

Indeed, some U. S. suppliers characterize most of their compatriots as little more than crybabies who expect business to be handed to them. "They sit there year after year and say they want to penetrate the Japanese market, but they don't bother to learn how to do it," says William H. Crawley, director of Japan operations for Rolm Corp. of Santa Clara, Calif. "What Brock should be doing is figuring out a way to solve the problem, such as holding seminars on how to do business in Japan. The problem is not NTT, not really."

Effort needed. Some U. S. officials admit that American companies could be trying harder. Some also now agree that the agreement was for too short a period, that three years is not enough time to win significant business in Japan. But what matters at this point, they argue, is the lack of evidence to show Congress that the agreement is working.

What could NTT do to get out of the doghouse? U. S. officials closest to the scene suggest that it decide soon to buy some central-office digital switching gear from the U. S. Four American suppliers have approached NTT with products but have gotten a noncommittal reaction.

In any case, NTT and its family of suppliers have spent considerable time and money to develop their own prototypes of the expensive, sophisticated switches and hardly want to countenance foreign intruders at this point. But the American companies argue that their switches are proven products and that NTT's are not as sophisticated as claimed.

"Central-office switching is the heart of the system," says a U. S. official. "As long as the U. S. is locked out of that, it's difficult to hang other [U. S.] things on that system." NTT remains coy about its plans, but it is at least keeping the door open.

Perhaps a brighter long-run opportunity for U. S. telecommunications suppliers is Japan's interconnection market. When it opened NTT procurement, the Japanese government also drastically liberalized qualification procedures for interconnection equipment—that which is sold on the open market to end users.

So far, all five U. S. companies that have applied for type approval have received it, although some complain that specifications are still too severe. At least Rolm claims to be off to a fast start, with its private-branch-exchange gear. Sales are ahead of projections, Crawley says.

The interconnection market could get a boost with the imminent elimination of laws requiring all users to buy their first telephone from NTT and to purchase an expensive bond. This change will give foreign suppliers a crack at the first-phone business and will probably stimulate the entire interconnection market by making phone purchases cheaper.

Still, the day seems distant when the U. S. can bring its telecommunications trade with Japan into balance. Against the $750 million-plus that Japan sold to the U.S. in 1982, it imported no more than $50 million. And the perceived attitude in the U. S. of NTT's intransigence will feed protectionist fires.

Some measure of the difficulties that must be overcome can be gained by the attitudes about one area: fiber optics. NTT says it is accepting bids from foreign suppliers on two advanced systems. The bidding will fall under the Track 3 classification, which means bidders will cooperate on research and development with NTT. Granted that getting a bid accepted is not the same thing as winning a contract, the attitude of one American trade official is instructive.

"Advanced technologies such as fiber optics, new switches, and so forth are where the action will be in the future," he says. "Japan knows that as well as we do, but it continues to play catch-up in things like switches, keeping U. S. companies out, and it won't get into joint R&D ventures in areas where it seems to have a lead, like fiber optics. Either way, the U. S. is getting screwed and we are tired of it." □

Additional reporting was provided by Ray Connolly, Washington bureau manager.

Business

Enriched GE ready to go shopping

Sale of mining firm for $2.4 billion gives it kitty for acquisitions, probably in robotics, factory automation, and office automation

by Robert J. Kozma, Business Trends Editor

Those friendly folks at General Electric Co. may soon be making some calls—friendly and otherwise—on a variety of high-technology companies around the U. S. The reason: it has a barrel full of cash and wants to make some high-tech acquisitions. Naturally enough, GE is not tipping its hand, but other sources think the industrial giant is looking into areas ranging from robotics and factory automation to office automation.

The bulk of the money that the Fairfield, Conn.–based conglomerate plans to spend as it travels the acquisition road will come from the proposed sale of its Utah International Inc. subsidiary for about $2.4 billion in cash to the Broken Hill Proprietary Company Ltd., an Australian-owned natural-resources company. Utah International, a producer of metallurgical coal in Australia with interests in the mining of iron ore, copper, and steam coal in North and South America, was acquired in 1976, when then-chairman Reginald Jones sought to diversify operations.

New course. With the world enmeshed in the problems of rising oil costs and constrained supplies of coal, GE management evidently felt that owning a large coal and mining firm would help counterbalance the cyclical nature of its traditional businesses. The acquisition, for $2.17 billion in GE stock, was called the largest in U. S. history.

But times have changed, the economy has changed, and more importantly, GE's top management has changed. Following the retirement of Jones, John F. Welch Jr. took over as chief executive officer in 1981 with the philosophy of making GE the No. 1 firm in its familar markets, primarily through acquisitions. And it is acquisitions—especially in high technology—on which Welch is counting for his company's growth.

"GE is determined to become firmly positioned at the leading edge of the high-technology products and the high-growth services segments of industry. This is where our human, technical, and financial resources give us unique advantages," said Welch in disclosing the sale of Utah to Broken Hill. "The sale of Utah will enable GE to focus these resources on the areas we've identified for future growth for product and services leadership."

Besides the $2.4 billion that will become available from the sale, GE also has almost $2.6 billion in cash and marketable securities, forming a formidable kitty. One aspect of GE's acquisition strategy concerns the size of potential takeover candidates. "I don't think GE would do one big acquisition," says J. Terence Carleton, a research analyst in minicomputers and computer-assisted design and manufacturing with Kidder Peabody Inc., Boston.

What to buy. "To acquire a company that doesn't have any problems, they would have to pay 50% above market value," which could be too dear for GE. While it may not try to buy one of the top high-tech firms, "they may pick up one of the 'smaller' $1 billion companies," he says.

One name that has been much bandied about as a possible acquisition target is minicomputer giant Data General Corp., Westboro, Mass. However, as Robert T. Cornell, who follows GE for Paine Webber Inc. of New York, points out, "Chairman Welch said in De-

Westinghouse is not sitting still

"Both companies, interestingly, are clearly dogging each other again." That's the reaction of Wall Street analyst Laura Conigliaro of Prudential-Bache Securities Inc. to a comparison of activities by industrial rivals General Electric Co. and Westinghouse Electric Corp. GE, of Fairfield, Conn., intends to make high-technology acquisitions, whereas Pittsburgh-based Westinghouse last month completed its takeover of one of the premier robot manufacturers in the U. S., Unimation Inc. of Danbury, Conn., for $107 million. "This is an important step in Westinghouse's plan to be a leader in factory automation," says retiring chairman Robert E. Kirby. "We're prepared to allocate the appropriate resources to help the Westinghouse-Unimation team remain a leader."

Westinghouse and General Electric are going after the same market and may wind up going head to head in the acquisition game. "Both companies have an eye out for opportunities," notes Paine Webber Inc. research analyst Robert T. Cornell in New York. Westinghouse, which also owns a 42% interest in Siliconix Inc., a Santa Clara, Calif., semiconductor firm, might like to acquire other firms, Cornell says. Adds Conigliaro: "$100 million [spent on Unimation] is not in itself a lot of money. But it's just the beginning of what Westinghouse will have to spend there to get a positive effect." **–R. J. K.**

cember that the company wouldn't try a big zinger" when it acquires anyone, which seems to rule out Data General.

In addition, GE's Calma Co. unit is phasing out the 16-bit Data General computers it used in its CAD/CAM gear and is planning to use 32-bit Digital Equipment Corp. VAX processors for future offerings. With GE is itself a DEC user, the Calma move would seem to work against against any formal union with Data General.

Also, Cornell adds, GE's capital spending totals almost $2 billion a year. So though the company "will have $5 billion available after the Utah divestiture, I think [GE] will make smaller acquisitions and boost its capital spending. There's an outside chance of [the company's] doing a large deal."

Growth the lure. The reason for GE's emphasis on acquiring high-tech companies is simple: they promise high growth, which is something that its core operations may not provide. ("The mainstream business won't grow much," claims a former member of GE's corporate technology staff who requests anonymity.)

GE ended 1982 with sales for the full year down about 3% to $26.5 billion compared with 1981 sales of $27.24 billion. Net income for the year, however, rose 10% to $1.82 billion from the prior year's $1.65 billion. The results were attributed by Welch to "the success of ongoing actions by people throughout the company to reduce overhead and improve operating efficiency."

GE's efforts to improve operating efficiencies include the use of something that it expects to sell to other companies: factory automation. Having acquired Calma (for $100 million late in 1980) and semiconductor maker Intersil Inc. (for $235 million in 1981), GE is making a big push in the factory-of-the-future marketplace to be the first to offer a totally integrated automated factory. It might well make an acquisition in this area, company watchers note.

"They've made no bones about being in the factory-automation marketplace," says Laura Conigliaro, a research analyst with Prudential-Bache Securities Inc., New York. "They've collected a variety of parts that theoretically will integrate together." Besides CAD/CAM equipment from Calma, these parts include industrial robots that GE provides through license from Japan's Hitachi Ltd. and Italy's DEA, information processing through its General Electric Information Services Co. (Geisco) unit, and computer-aided engineering services and software through GE-CAE International Inc., a joint venture with Structural Dynamics Research Corp. of Milford, Ohio.

Eyes for robots. According to Conigliaro, GE could attempt to fill in some pieces of its factory-automation offerings, especially in the robotics area. "I don't believe they've fully understood the robotics market," she says. GE has made some changes in its robotics operation, and there are a number of small robot manufacturers that may be available for acquisition if it decides to go in that direction. One robot firm that is no longer available is Unimation Inc., which Westinghouse grabbed (see "Westinghouse is not sitting still," p. 104).

General Electric is "positioned with a lot of power" in the factory-automation market, says Maurice Klapfish, who follows this area for Venture Development Corp., Wellesley, Mass. Klapfish cites GE's corporate strength and its good acquisitions to date, especially Calma Co. According to Klapfish, Calma has garnered about an 11.5% share of the CAD/CAM market, which totaled $746 million in 1981. He feels GE would acquire a robot manufacturer "in a minute; a robot acquisition sounds good to me."

Still, the factory-automation marketplace is not the only avenue that GE may pursue. One former employee claims the firm has developed a list of possible takeovers ranging from office-automation companies to instrument firms. "I think they will continue to make smaller acquisitions in the factory-automation, medical-instrument, and software areas, and possibly the materials business," says Paine Webber's Cornell.

Whatever kind or size of company GE tries to acquire, it will want one that "is manageable and that will fit in easily without hurting its earnings or its balance sheet," Kidder's Carleton maintains. In fact, "the balance sheet is paramount for GE," says a former employee. □

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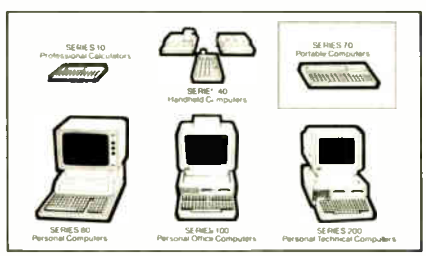

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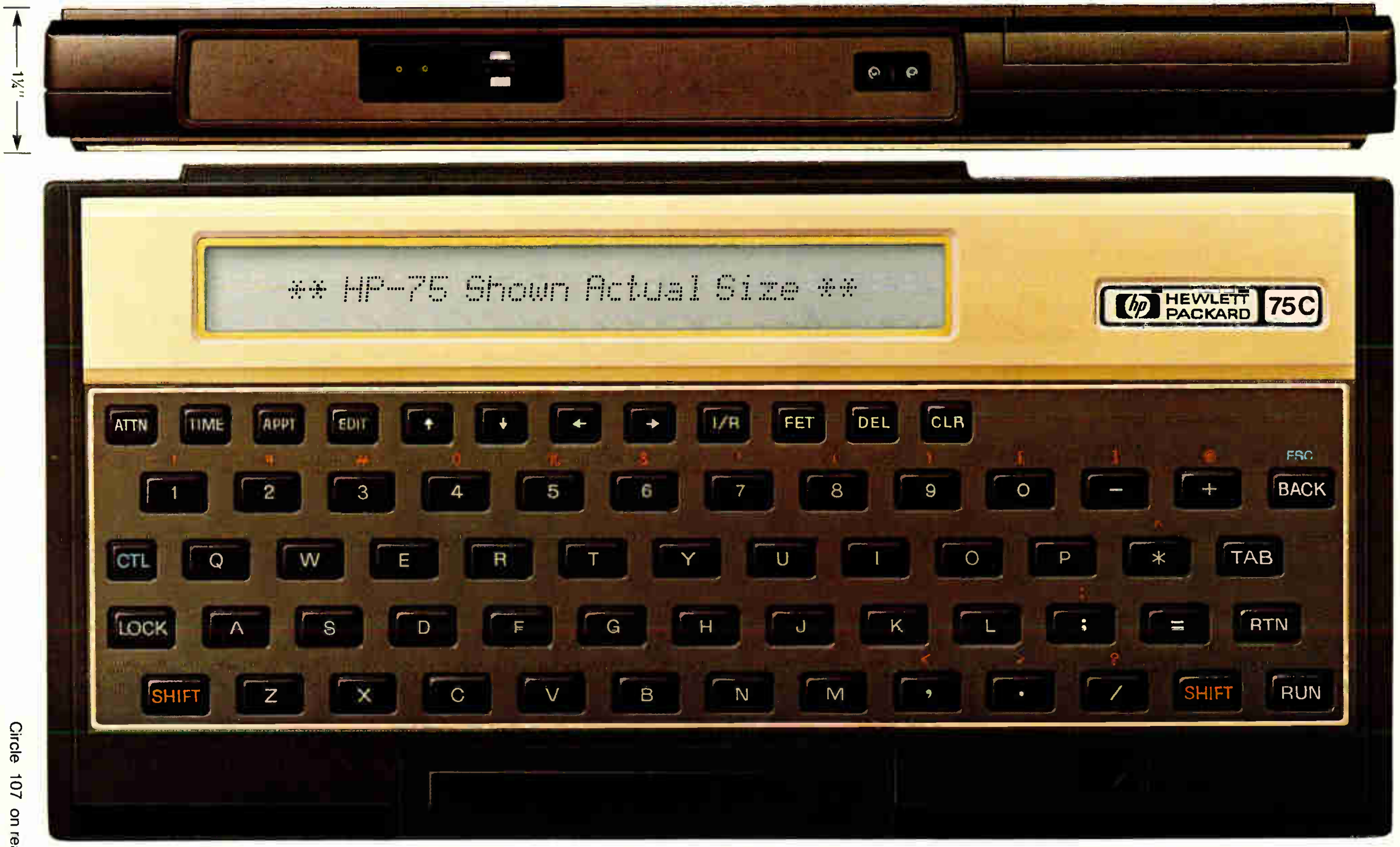

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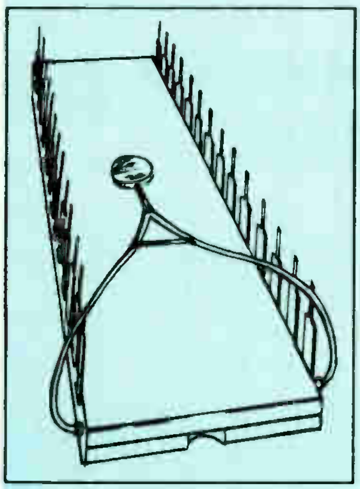


SPECIAL REPORT

A little extra circuitry on chip and special software lets VLSI test itself chip by chip and board by board

by Richard W. Comerford, *Test, Measurement & Control Editor*
and Jerry Lyman, *Packaging & Production Editor*

Testing digital large-scale integrated circuits and the printed-circuit boards built around these complex semiconductors at present requires more extra baggage than is convenient—computer-controlled automatic test equipment, plus the extensive software base on which this equipment depends. The next generation of chips and boards will snarl the testing problem further, since circuit nodes will be even less accessible than in the case of LSI. In fact, the possibility of very large-scale integrated circuits and boards that simply cannot be tested at all has become a real worry.

An attractive solution to this problem is the concept of self-testing. In self-testing, a chip or a board loaded with chips actually is made to test itself without the aid of external equipment or software.

Back in the early 1970s, IBM Corp. introduced its approach to self-testing in computers, known as Level-Sensitive Scan Design, or LSSD. In this system, which may be employed at the chip, board, and system levels, special shift-register latches (SRLs) are added to each chip [*Electronics*, March 15, 1979, p. 108]. These latches are chained into one long shift register. A serial test pattern from the computer's internal test processor is fed, or scanned, into the input of the register and exercises the chip's normal circuitry. The output of the chain is then compared with the expected states of the register also stored in the test processor.

Strictly speaking, however, that test processor is extraneous to the rest of the system, and designers have been busy looking for a fully self-contained self-testing method. One such achievement is the Bilbo (built-in logic-block observer) technique first reported by Bernd Koenemann of the Institute for Theoretical Technology, Aachen, West Germany, at the 1979 Test Conference at Cherry Hill, N. J.

In this method, two identical programmable flip-flop shift registers are added to the logic circuitry to be tested. The input shift register is programmed to act as a pseudorandom-pattern generator, while the second shift register is formed into a signature-analysis register. The pattern generator feeds its parallel pattern into the chip or board under test. The chip's output is fed into the signature register, whose output in turn feeds a decoder to generate a pass-fail indication. The Bilbo concept was tested successfully on combinatorial circuits at Siemens Corp., Cherry Hill, N. J. [*Electronics*, May 19, 1982, p. 164].

A very recent piece of action in the expanding self-testing field combines LSSD and Bilbo features. Storage Technology Corp., Louisville, Colo., has developed an LSI self-testing method using LSSD circuits already designed onto a gate-array chip (see p. 110). Pseudorandom test patterns are generated by combining some of the LSSD shift-register latches into a shift register of maximal length. Then the pattern responses of the on-chip logic are analyzed by a Bilbo-like built-in signature register.

Another important extension of self-testing is the Microbit (for microprocessor built-in test) concept developed at the Corporate Research and Technology division of Siemens in Princeton, N. J. (see p. 116). In this self-testing technique, two Bilbos plus a small amount of test circuitry must be added to a microcomputer board. Also, a special test program is stored in the processor's programmable read-only memory. The program sequentially tests all portions of the microcomputer.

Questions remain, however. For instance, can a design using a self-testing technique actually produce a chip that is fully testable? A new software set from Comsat General Integrated Systems Inc. in Austin, Texas, can provide the answer to that question where it is most needed—at the designer's work station (see p. 120). This software is an adjunct to the Tegas computer-aided design program that is widely used in chip design. When an engineer employs it to evaluate a design, he or she gets immediate feedback both on whether there are any parts of the design that cannot be tested and on the difficulty of performing tests.

Armed with this knowledge, the chip designer can modify the design before capital is spent on prototyping. Further, the software can then pass the testability results to the program-generation portion of the package so that it may create a test program. If this program is downloaded to, for instance, a read-only memory, the ROM can be incorporated on a self-testing board.

Synthesis of techniques creates complete system self-test

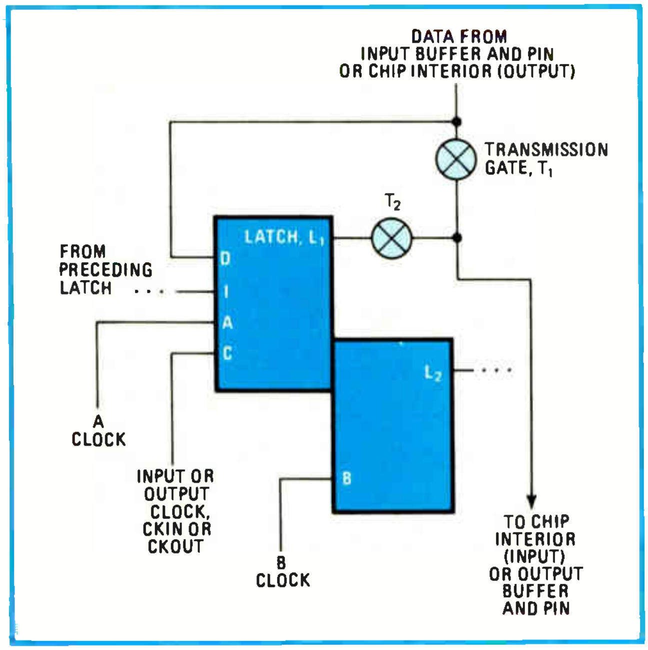
Level-sensitive scan design, pattern generation, and signature analysis combine to let chips, wafers, boards, and systems find their own faults

by Donald Komonytsky, *Storage Technology Corp., Louisville, Colo.*

☐ Very large-scale integrated circuits hold the promise of their own testing salvation. They can be made painlessly and completely self-testing by combining an adaptation of IBM Corp.'s level-sensitive-scan-design (LSSD) [*Electronics,* March 15, 1979, p. 101] with pseudorandom test-pattern generation and signature analysis [*Electronics,* March 3, 1977, p. 83]. Further, these self-testing features can be hierarchically extended from wafers to boards and ultimately systems, as LSSD in its original form does.

Even better, the greater the density of VLSI chips, the more cost-effective these self-testing techniques become. The facts are that the complexity and silicon-real-estate costs of self-testing remain fairly constant, while the cost and effort of testing using standard techniques increases geometrically. Thus in the next few years, self-testing VLSI will begin to relegate the panoply of VLSI test systems, functional and in-circuit board testers, diagnostic programs, and test-generation software to the technological junk heap of history.

Self-testing VLSI chips can be designed with a minimum of effort and overhead logic by adding a ring of shift-register latches (SRLs) around the periphery of the chip. Scanning data into or out of this scan ring then makes it possible to stimulate or observe the chip's input and/or output.



1. I/O latches. Putting the shift-register latches above at the input and output pins of a gate-array chip is the first step in a new VLSI self-testing scheme. Transmission gates T_1 and T_2 are simple switches that let data pass when on or block it when in an off state.

The ring around the chip

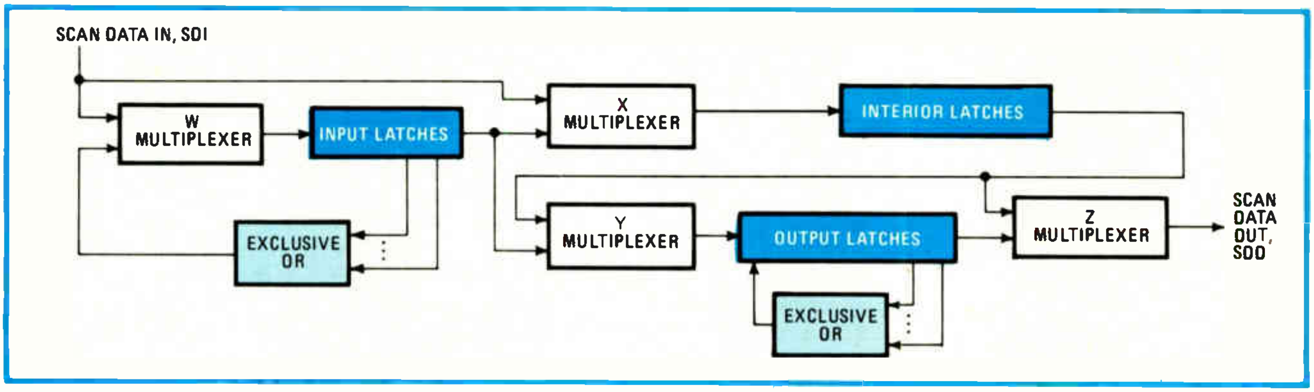
For connecting to an input or output pin of a chip (Fig. 1), the SRL consists of master latch, L_1, and a slave latch, L_2, organized as in LSSD. The clock signal CKIN or CKOUT, when input to latch L_1, sets it to the value of data input D, while clock A sets it to the value of the I input. Similarly, clock B sets L_2 to the value of the L_1.

Both L_1 and L_2 are transparent whenever their clocks are high. By connecting each L_2 output to the I input of the succeeding L_1 latch, it is possible to hook the SRLs together into a shift register. Clocking A and B alternately will shift data through the register.

In a gate array, these SRLs and their associated transmission gates can form an integral part of the I/O buffers at the periphery of the chip. Thus they need not utilize any of the transistors inside the gate array proper. The silicon area used by these enhanced buffers can thus be minimized. In addition, each buffer can be wired by automatic routing programs. The periphery of the gate array has its own routing channels, so that the SRLs may be connected to each other, to the interior of the chip, and to the A, B, input (CKIN), and output (CKOUT).

The logical interconnection of the SRLs is shown in Fig. 2. All SRLs of the chip are arranged in three groups: input latches, all SRLs connected to input pins; output latches, all those connected to output pins; and interior latches, SRLs that form the registers and latches inside the gate array itself. The input latches are not necessarily physically contiguous, but are connected so that all input latches form a single shift register; the same is true for the output latches.

By making the interior of the chip conform to the LSSD discipline, all interior latches also form a single long shift register into and out of which data can be scanned for testing. The scan-data-in (SDI) and scan-



2. Latch connection. All the input latches (Fig. 1) are connected to form a logical block as shown above, as are the output latches. Interior latches result from applying LSSD design, while the four multiplexers and the exclusive-OR circuits are part of the gate-array logic itself.

data-out (SDO) pins are I/O pins, while the multiplexers and exclusive-OR gates in Fig. 2 are part of the logic of the gate array and not part of the I/O scan ring. The I/O connections shown in Fig. 2 will be the same for any chip, allowing automatic placement and routing software to wire the chip once the locations of the input and output pins have been defined.

Random patterns

With this latching hardware, a self-testing VLSI chip would use pseudorandom patterns produced by a pseudorandom–test-pattern generator, which can be built from some of the input SRLs (Fig. 3). The pattern thus created can be viewed as a serial stream of random 1s and 0s arriving at the first latch and being shifted into the other input latches. The patterns are shifted into the interior latches through the X multiplexer in Fig. 2.

With n latches, the test-pattern generator will produce 2^n-1 pseudorandom patterns before the cycle repeats. The exclusive-OR gates feed back certain L_2 outputs of the latches to the I input of the first latch. Each cycle of the A and B clocks produces a new random pattern in the input latches.

Table 1 gives the needed feedback terms for each choice of n. For example, if the desired n is 24, the L_2 outputs of latches 1, 2, 7, and 24 (numbering them from left to right) are exclusive-ORed to the I input of latch 1. At most, only four terms are ever required, so that the maximum amount of feedback logic is just three two-input exclusive-OR gates.

The test-pattern generator is a very cheap and simple way to store and apply a huge number of test vectors to the inside of a chip. Running it thus generates as exhaustive a set of patterns as would an n-bit counter, but with less overhead in logic.

Signature analysis

The responses of the self-testing chip to the pseudorandom patterns can be compressed into an 8-bit signature using the serial-parallel signature register in Fig. 4. This register, which resembles a built-in logic block observer, or Bilbo [*Electronics*, May 19, 1982, p. 164], has four distinct modes of operation.

The first two modes occur when the disable line is high; the register can load the values on lines Z_1–Z_8 in parallel by clocking C, or the register can be used as a shift register in the usual SRL fashion by alternately clocking A and B. The serial data coming into the first latch is unaffected by the feedback line when the disable line is high. The other two modes occur when that line is low; the register can compute the signature of data on Z_1–Z_8 in parallel by clocking C, or serially on data from upstream SRLs using alternate clocking of A and B.

A signature computation on successive parallel words requires that L_1 be transferred to L_2 after each parallel load. Once a signature is sitting in the signature register, it can be shifted out through the SDO pin and observed, or else it can be compared internally with an expected signature and the result of the comparison used to provide a go or no-go indication.

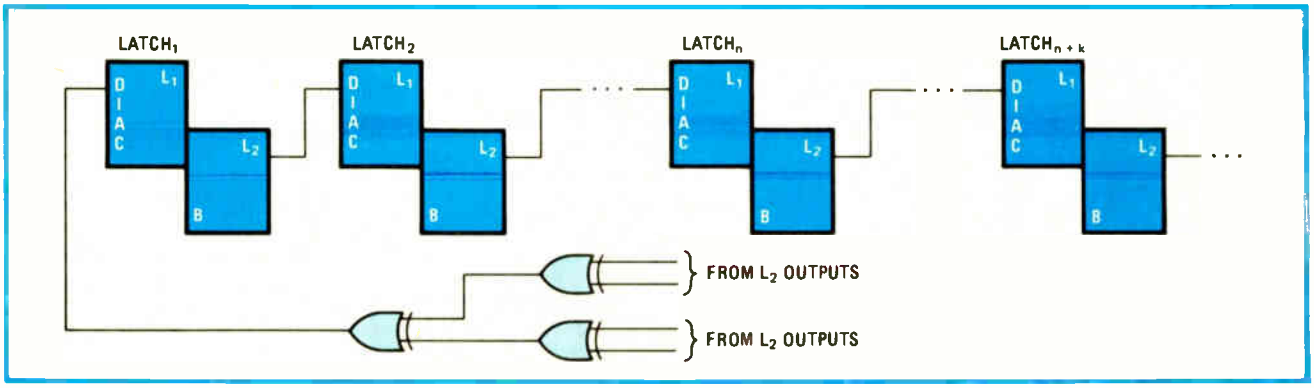
The signature register is built from the last eight output latches before SDO and the exclusive-OR and the NOR gates that are part of the interior gate array. With an 8-bit signature register, bit inversions caused by faults in the chip will be detected with a 99.6% probability. If desired, the signature register can be made longer, but this will have little effect on the probability of detection.

Testing modes

These three building blocks—the I/O scan ring, the pseudorandom–test-pattern generator, and the signature register—are all that is needed to design VLSI chips with a high degree of testability. To control testing, the chip needs to have eight special pins: the A, B, CKIN, CKOUT, SDI, and SDO pins already discussed, plus two test-mode pins. Table 2 shows the four test modes of operation of the chip and the functions the pins must perform.

In the normal-operation, or LSSD, mode (test mode 0), the interior latches can be scanned independently of the input and output latches, and the chip looks like a typical LSSD chip. Although the I/O scan ring can be made to sample the I/O pins by clocking the CKIN and CKOUT lines, they do not otherwise enter into chip operation at this point.

In the pin-test mode (test mode 1), the peripheral scan ring can be scanned independently of the interior latches,



3. Pseudorandom source. With the same basic SRLs used in Fig. 1, a pseudorandom-test-pattern generator can be built on chip to provide stimuli for self-testing. Using n latches, up to four of whose L_2 outputs are used as inputs to an exclusive-OR feedback, produces $2^n - 1$ vectors.

and the signature register is disengaged (the disable line in Fig. 4 set to 1, or high) at the last eight output latches before SDO. The output latches apply their values through T_2 latches (Fig. 1) to the chip interior. The pin-test mode is used to test the interconnections between chips with externally applied test vectors.

The ring-scan mode (test mode 2) is a variation of the pin-test mode that allows the contents of the I/O scan ring to be shifted out while all chips of the system continue running. Because T_2 is turned off, this scanning cannot affect chip operation.

In test mode 3, the chip enters its true self-test mode: that is, the input, interior, and output latches become one continuous shift register, the test-pattern generator becomes operational, and the signature register is engaged. The self-test mode requires only externally applied clocks, since pseudorandom patterns are generated automatically inside and the chip diagnosis itself uses signature analysis.

Figure 5 shows the configuration of an LSSD-based chip that has been put into the self-test mode. SRL sets S_1, S_2, and S_3 are those used during normal chip operation and are clocked by nonoverlapping system clocks C_1 and C_2. N_1, N_2, N_3, and N_4 are combinational networks, while E_1 through E_7 are the internal signal trunks among these networks. PI_1 and PI_2 are the primary inputs to the chip, and PO_1 and PO_2 are the primary outputs, each consisting of a plurality of signal lines. SRL sets I_1 and I_2 constitute the set of input latches, O_1 and O_2 the set of output latches. All SRLs form a long scan ring from SDI to SDO: input latches first, then interior latches, and finally the output latches.

TABLE 1: PSEUDORANDOM PATTERN GENERATOR CONFIGURATION FACTORS ON SELF-TESTING VLSI CHIP

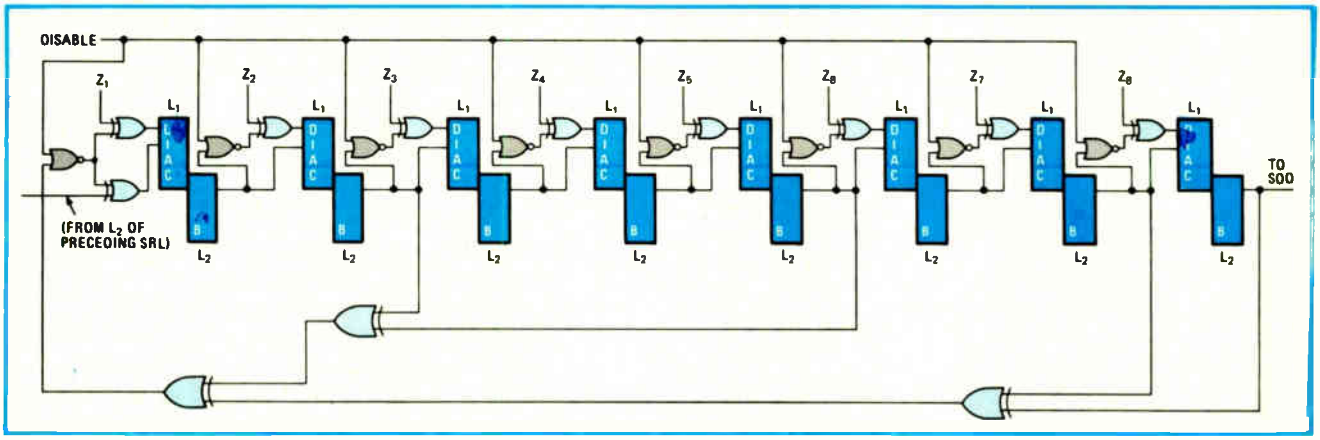
Number of elements (n)	Number of vectors (× 10^6)	Feedback elements (numbered left to right)
20	1.05	20, 3
21	2.10	21, 2
22	4.19	22, 1
23	8.39	23, 5
24	16.8	24, 7, 2, 1
25	33.6	25, 3
26	67.1	26, 6, 2, 1
27	134	27, 5, 2, 1
28	268	28, 3
29	537	29, 2
30	1,07 -	30, 23, 2, 1
31	2,15 -	31, 3
32	4,29 -	32, 22, 2, 1
33	8,59 -	33, 13
34	17,2 - -	34, 27, 2, 1

The self-test details

To initiate the self-test, both the pseudorandom–test-pattern generator input latches (SRL set I_2) and the signature register on the last eight output latches are loaded with starting values to provide a deterministic starting point. This is done by setting the chip into the pin-test mode and scanning in the desired values. All the interior latches are set to 0 by setting the chip to normal-operation mode and scanning in 0s. The input latches must not be cleared to 0s, however, or the test-pattern generator will stay locked in a 0 state forever. After all latches have been initialized, the chip is put into the self-test mode. At this time, the first test pattern is applied inside the chip. For example SRL set I_1 stimulates network N_1, S_1 stimulates N_3, S_2 stimulates N_4, and so forth.

Clocking the system clocks C_1 and C_2 allows S_1, S_2, and S_3 to capture the responses of N_1 and N_2. Then clocking CKOUT allows the output latches to capture all signal values on the primary outputs of the entire chip. Because the signature register is enabled, the signature is computed in parallel when CKOUT is clocked. If any faults inside the chip have been detected by the current test vector, the resultant incorrect response will be captured inside some of the interior or output latches.

The next step is to provide enough A and B clocks to completely scan out all interior and output latches. If any fault responses have been captured in latches, they will eventually be shifted into the signature register, causing an incorrect signature. As the serial data stream enters the signature register, a signature is computed serially. Simultaneously, the input latches are shifted and the test-pattern generator produces serial pseudorandom



4. Signature latches. Using 12 exclusive-OR gates and 8 NOR gates, a signature-analysis circuit with 99.6% fault coverage can be created from eight SRLs at the output pins of a chip. Disabling the NOR gates lets the SRLs serve their normal, LSSD output functions.

patterns that enter the input latches and are propagated to the interior and output latches.

When the scan is complete, a new random pattern sits in I_1, I_2, S_1, S_2, and S_3, stimulating the combinational networks. The test cycle can now be repeated, clocking the system's clocks, CKOUT, and so forth.

Enough test cycles are run to ensure an adequate fault test score for the chip. This fault test score can be determined by simulation of the chip. After the last test cycle the signature can be examined by scanning out the signature register and comparing its contents with an expected signature, also determined from simulation. For completely self-contained testing, the expected signature can be prestored in the chip, which can compare it internally with the actual signature and then issue a go or no-go indication.

Because the test cycle consists of nothing more than toggling the clocks to the chip, no expensive VLSI tester is needed. In fact, a test-driver chip can provide the stimulus for the other chips on a printed-circuit board or in a multichip module as in the pin-testing technique. Furthermore, the clocks can be cycled at system speeds, allowing for rapid, thorough testing. For example, if the clocks are applied every 100 nanoseconds and if 100 interior and output latches are shifted every cycle, then 18 million pseudorandom vectors can still be applied every minute to the chip.

All together, too

Finally, since the clock sequencing is similar for any chip, differing only in the number of system and A and B scan clocks, multiple chips can be tested in parallel, the number of clocks in a cycle being the largest needed by any chip. Shifting the scan ring in a chip more than needed does not destroy the validity of the self-test but merely wastes part of the set of pseudorandom test vectors produced.

The pseudorandom test vectors produced inside the chip of Fig. 5 can test the chip effectively because all sequential logic has been reduced to combinational logic by the architecture of LSSD. The combinational logic has further been partitioned into nonoverlapping networks such as N_1, N_2, N_3, and N_4, which can be controlled and observed by nearby SRL sets.

Ac testing

If the system and scan clocks in the self-testing cycle have the same clock width, periods, and phase relationships that they would have for operation at maximum speed in the normal-operation mode, then the self-test will be a dynamic test of the chip as well as a static test for stuck-at faults in chip, board, or system.

For instance, assume that for the circuit of Fig. 5 the time between the rising edge of the last A clock in the scan portion of the cycle and the falling edge of C_1 is equal to the worst-case delay through network N_1. This last A clock causes the new random vector to be loaded into I_2 and to stimulate N_2. Then if N_2 has a delay fault or if some process variation has produced a slow chip, one or more of the latches in S_3 will at some time during the test be set incorrectly, eventually causing an incorrect signature. The same considerations apply to any of the networks within the chip as well as to the SRLs.

Under dynamic clock conditions, therefore, if the chip passes a self-test, it ensures both that the chip has no faults and that it meets worst-case performance requirements; it is a go–no-go type of test. It is also possible, however, to gauge the speed of a given chip relative to other chips of its type by wiring the scan latches inside into a ring oscillator and measuring the period of this oscillator.

It will be recalled that in the normal-operation mode (test mode 0), all interior latches form a continuous scan ring, so that a long delay chain from SDI to SDO can be formed by simply raising the A and B clocks, causing all interior latches to become transparent. Similar considerations apply to the I/O scan ring in the pin-test mode (test mode 1). Because the latches are noninverting and since the feedback paths in the the test-pattern generator and signature registers are disabled, a signal applied to SDI will appear at SDO uninverted after some delay. Tying SDO back to SDI through an inverter turns the entire scan into a ring oscillator. The period of the oscillator will characterize the ac performance of the chip, since process variations will affect the switching times of the transistors in the scan path, and these differences will be magnified due to the many transistors in the path.

Pin testing

The ability of the SRLs in the I/O scan ring to control or observe any I/O pin makes the testing of interconnections between chips extremely easy. In a typical situation, chips are strung into a single multichip scan ring through connections from the SDO pin of one chip to the SDI pin of the next chip.

For testing, the test mode is set to 1, and a test pattern is scanned into the output latches of each chip. Since the output latches have T_2 (Fig. 1) turned on, the value in L_1 is sent through the output buffer across the signal wire to the pin of a connecting chip, then through the input buffer to the D input of the corresponding input latch. Clocking CKIN for all chips allows the input latches to capture the signals at their D inputs. The entire multichip scan ring is then scanned out for examination at the same time as another test pattern is being scanned in.

Generating tests for all possible wiring stuck faults and shorts is so straightfoward that no test-pattern–generation programs are needed. Just two test patterns can test for all stuck faults: all 0s and all 1s. Before the test, a pattern of 1s and 0s is scanned through the multichip scan ring to verify its correct operation.

To test for all possible shorts, each output latch is assigned a serial set of values such that the binary number constituted by these values is a unique binary number composed of at least one 1 and one 0. For example, the test set for all shorts between three wires contains three tests that assign the values 001, 010, and 011 to the corresponding output latches.

TABLE 2: INTERNAL VLSI-CHIP CONFIGURATIONS SELECTED BY VARIOUS SELF-TEST MODES

Mode	Configuration (see Figs. 1 and 2)
LSSD (mode 0)	Select SDI through X multiplexer Select interior latches through Z multiplexer Select A and B clocks to interior latches Turn T_1 on and T_2 off for input and output latches
Pin test (mode 1)	Select SDI through W multiplexer Select input latches through Y multiplexer Select output latches through Z multiplexer Select A and B clocks to input and output latches Turn T_2 on and T_1 off for output latches Disable signature register
Ring scan (mode 2)	Same as for pin-test mode, except that T_1 is turned on and T_2 is turned off for output latches
Self-test (mode 3)	Select exclusive-ORs through W multiplexer Select input latches through X multiplexer Select interior latches through Y multiplexer Select A and B clocks to all latches Enable signature register

The test set is such that each pair of wires is assigned a differing pair of values in at least one test. Thus if a short exists, at least one of the wires will receive a value the opposite of its unshorted value as seen at the input latches of the receiving chip, so that the short will be detected. The number of tests needed for all shorts is approximately equal to the base-2 logarithm of the number of wires, so even for 1,000 wires only about 10 tests are required and no special hardware is needed.

Since the tests are so simple, a microcomputer can do the test sequencing and response analysis. In fact, one of the chips can be designated as the test driver to check out the interconnections across the whole module. Such a scheme is excellent for system self-diagnosis because the test-driver chips can be engaged at any time to test for faulty wiring, all modules of the system being tested in parallel. The test vectors need not be stored: because of their simplicity they can be generated algorithmically in the test-driver chips when needed.

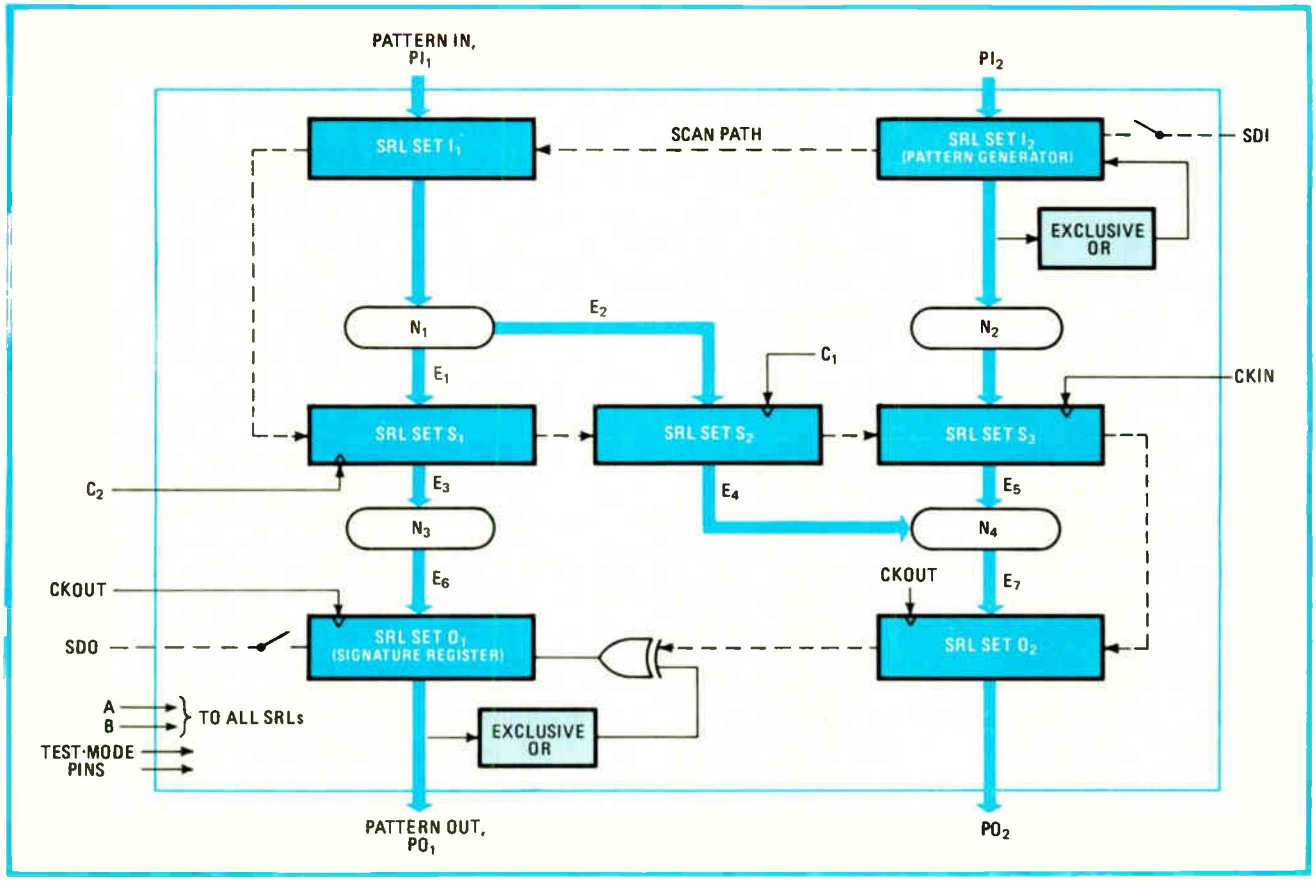
Furthermore, by adding signature registers inside the test-driver chips—to perform a serial signature analysis on the multichip scan ring as the ring is scanned out—the need to store expected response vectors is also eliminated. This testing scheme is equally valid in cases where chips are individually packaged and those packages are mounted on multilayer printed-circuit boards.

Wafers, packages, boards, systems . . .

The self-test features described thus far enhance not only chip testability but testability at each level of the hierarchy from VLSI wafers to a full digital system. At the wafer level, probing is simplified because only the test control pins and chip clocks need be contacted. If contact wires are run from central probe points on the wafer to individual chips, every chip can be tested simultaneously. The wafer, in effect, becomes a self-testing wafer. Furthermore, all this is accomplished without the need either to generate test and response vectors or to use elaborate VLSI testers. The wafers can also be sorted for ac performance by measuring the periods of the scan-ring oscillators of sample chips.

At the level of the packaged chip, much the same considerations apply. The packaged VLSI parts can still be self-tested in parallel and their ac performance characterized. In addition, the pin-test mode makes it easy to test bonding leads for shorts and opens. Being able to set the outputs of pins to desired values likewise simplifies parametric testing of the buffers in the chip.

At the multichip module and pc-board levels, pin-test mode elminates the need for functional or in-circuit testers. If a chip or part of a chip is designed as a test sequencer to test the other chips on the board or module, external test hardware can be completely eliminated. Not only can the interconnections between chips be tested, but the chips themselves can be functionally verified in self-test mode. Each chip can test itself in isolation from surrounding chips because the T1 transmission gates are turned off during self-test mode for both input and output buffers. Such testing is valuable in ensuring that the



5. Working together. Configuring input latch set I_1, made up of n SRLs, as in Fig. 3, and eight-SRL output set O_1, as in Fig. 4, makes a chip truly self-testing. In all, such a scheme requires that eight pins be used for testing, a small burden for VLSI considering the test cost saved.

insertion of the chips has not damaged them.

If the test-driver chip is given the capability of driving the rest of the chips through their clock sequences in parallel and then monitoring the signature registers for go/no-go indications, the board or module becomes self-testing too. The test-driver chip does not itself need to be tested because if it is not functioning properly, the other chips will all produce bad signatures. Alternatively, redundant driver chips can be used to check each other.

But it is at the system level that these self-test features can have the most spectacular effects. If the chips, modules, and boards of a system are all self-testing, a faulty system can be diagnosed down to a single failing chip or signal wire by having a diagnostic processor, which can be a self-testing unit, put the system into self-test or pin-test mode, engaging all test driver chips and monitoring the results of the tests at each driver chip. For self-test mode, every chip computes its own signature so that fault resolution penetrates right down to the individual chip. In the pin-test mode, each test-driver chip has a signature register that computes the signature as the multichip I/O scan ring is scanned out.

In system testing, faults are resolved initially to the board or module level with the aid of a bad signature in the test-driver chip. However, the driver chip in question can signal the diagnostic processor that it has found a bad signature, and the diagnostic processor can thereupon reinitiate the test in that driver chip, this time having the scan data shipped back to it. By comparing this data with the expected data, the diagnostic processor can isolate a failure down to a single wire. These tests can be run without human intervention at a remote site and the results transmitted back to a diagnostic center.

For the record

Finally, the SRLs in the I/O scan ring and in the interior of the chip can be used to capture information in the event of a real-time failure in the system. This information can be scanned out to aid in fault diagnosis. Clocking CKIN and CKOUT allows data at the I/O pins of the chip to be captured in the input and output latches. This can be done on the fly as the system runs. Putting the chip into ring-scan mode then allows data to be shifted out of the I/O scan ring without affecting the interior SRLs, so that the system can keep running throughout.

Such a feature is particularly valuable for capturing transient events in prototype debugging or system testing. In the event that error-checking circuitry detects a failure, the clocks can be shut down and the state of the system frozen in all SRLs, which can be scanned out to the diagnostic processor before system self-test begins. ☐

Microbit brings self-testing on board complex microcomputers

Special software and modified shift registers test and diagnose circuit blocks of microprocessors

by Patrick P. Fasang, *Siemens Corp., Princeton, N. J.*

☐ As microprocessor-based systems and devices take quantum jumps in complexity, their associated test costs are skyrocketing, making functional self-testing at both the board and system levels a matter of some urgency. An attempt to answer this concern is a novel approach to self-testing of microprocessor-based systems called Microbit 1 (for microprocessor built-in test), which requires only the addition of some on-board circuitry.

Microbit is a general concept for testing printed-circuit boards that contain a microprocessor or any microprocessor-based system. It can be applied regardless of the microprocessor type, but hardware and software implementation of the Microbit 1 concept on an 8085 8-bit microprocessor and subsequent testing confirm its potential benefits, which include:

- Elimination of functional-test equipment—the test is completely self-contained.
- Speedier troubleshooting—diagnostic capability is built in.
- Elimination of all efforts required to develop suitable test vectors because all test programs are stored in the microcomputer's read-only memory.
- Greatly simplified field testing because of the self-contained nature of the built-in tests.
- Relatively fast testing time—on the order of a half minute for an 8-bit microcomputer.

On-board additions

Microbit incorporates additional hardware and software into a microprocessor-based system to provide the self-testing capability, obviating conventionally required external equipment. Its aim is to test the system at the functional level, assuming that various chips making up the system have been previously tested and have passed parametric tests. To speed troubleshooting, the system also provides diagnostics for fault location. Resolution of the fault location found by the on-board diagnostics is a function of how much hardware and software is added.

Figure 1 depicts the basic microcomputer-based system used to test the Microbit concept. Four functional blocks plus a display have been added to a standard basic microcomputer configuration. The 8085-based system in its minimal configuration is Multibus-compatible, has 1-K of random-access memory, 2-K of programmable read-only memory, serial input/output ports, and 22-line parallel-I/O ports. The cycle time is 1.3 microseconds. Further, the system can perform bus arbitration and is expandable. Besides the 8085 microprocessor, standard computer functional blocks include a clock and reset circuit, extenders, address-latch circuit, control logic, 8155 RAM, I/O, timer, port-test logic, Multibus adapter, and serial-port test logic.

The four major functional blocks added for the Microbit implementation are the pseudorandom pattern generator (PRPG), the signature register (SR), the divide circuit, and the start-test switch. Although all these blocks have been built with off-the-shelf chips and their functions are almost self-evident, there are certain functions peculiar to the presence of the Microbit logic within the system. For this reason, a closer examination of Fig. 1 is necessary.

The clock and reset circuit produces the basic system-clock reference. All flip-flops within the system are initialized by the reset signal generated by this block.

Extenders (bus drivers) to prevent possible signal degradation have been added to the system because the overall hardware involved several wire-wrapped boards connected by flat cables. If all system components were on a single board, no bus drivers would be required.

The control logic block actually consists of several subblocks that generate timing and control pulses. The subblocks are: a ready circuit, pseudomemory circuit, memory-address–acknowledge circuit, and input/output-address–acknowledge circuit. These circuits serve two functions. First, they allow the microprocessor to differentiate between signals coming from on-board and off-board circuits. Second, they sense memory addresses for the added self-testing hardware.

RAM and PROM memory total 3-K bytes—1-K byte in the RAM and 2-K bytes in the PROM. The RAM consists of two 2114A 1-K-by-4-bit static chips; the PROM comprises two 2716 chips. On a single 8155 chip are 8155 RAM, I/O, and timer, along with 256 bytes of RAM, three parallel I/O ports, and a countdown timer.

What's more, port-testing logic has several address-decoding circuits that provide enabling and clock signals for the 8155 demultiplexer, the 8155 demultiplexer front-end latch, and the 8155 output buffer. Serial-port test logic allows the serial I/O data to be captured and returned to the microprocessor. It also contains a multiplexer for differentiating between and selecting real or test data. The divide circuit contains three divider circuits for reducing the basic system-clock frequency to other frequencies required in testing.

The PRPG (Fig. 2) is a four-function linear feedback register with eight flip-flops and three feedback paths. Depending on the logic state of the control line, B1A, the circuit can serve as either a PRPG or a signature register, or SR. For Microbit, the PRPG generates a repetitive sequence of 256 pseudorandom patterns of numbers. The reason for calling these number patterns pseudorandom is that the sequence in which a number appears is in fact predictable and not random at all. These numbers are used to test the RAM as well as the Multibus adapter.

Both the PRPG and the SR circuits are known as Bilbos, or built-in logic-block observers [*Electronics*, May 19, 1982, p. 164]. While the PRPG provides test inputs, the SR captures and compares parallel data to yield a signature.

During the tests, numbers were assigned to various subsystems of the microprocessor board, as shown in the table. The display used in the experiments is a single hexadecimal digit that shows the identification number of a faulty functional subblock.

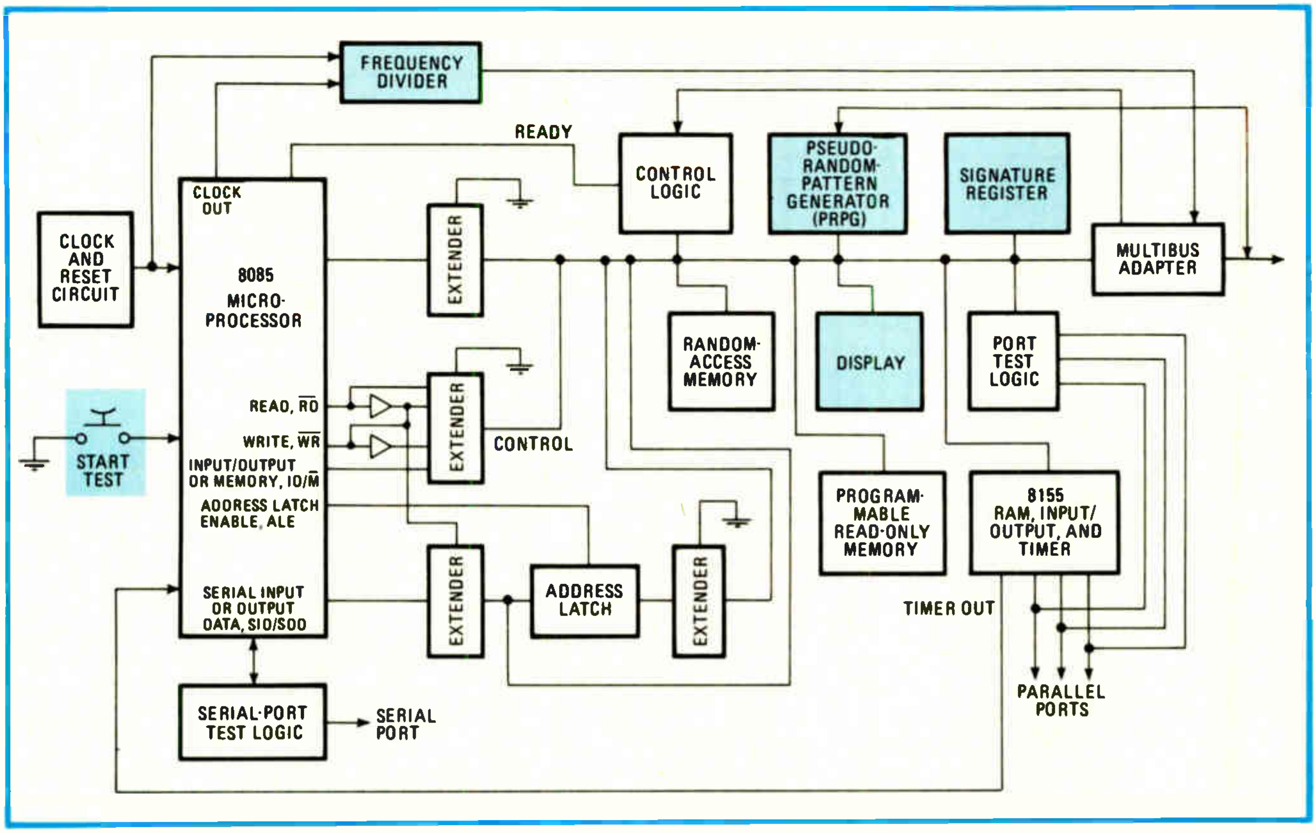
The second vital element of Microbit is its software. The entire program (written in 8085 assembly language) occupies about 700 bytes of memory. It is broken down into nine independent and self-contained modules. Thus, if a particular subblock is absent, the corresponding module is bypassed or omitted. Assembly language was chosen to conserve memory space. An aim of the software writers was to integrate these codes with an application program and place both in PROM.

Development-system software was done conventionally. For example, in case of the PRPG, once the concept was formulated, a flow chart was prepared. Next, the program was written, tested, and debugged (Fig. 3). The entire PRPG program occupies 15 lines of code.

In operation (once the system is powered up, all flip-flops are reset and the system is initialized), the most fundamental test—the kernel test—is performed first. This checks the microprocessor (with respect to only a few instructions), buses, clock and reset circuit, the display, and the address and data lines. This is done by adding two special numbers such as 10101010 and 01010101 and comparing the result with 11111111. If correct, the microprocessor then checks the display by displaying 0, 1, 2, . . . F.

Next the PRPG is tested by loading a known initial word. It is then clocked 256 times, 0 through 255. Then the PRPG contents are transferred to the microprocessor and compared with a known value that was computed independently. If the numbers agree, the PRPG passes.

The SR test that follows is identical to the PRPG test. In the succeeding step, the PROM is tested by loading the



1. Microbit. Microbit (for microprocessor built-in test) is a technique for enabling microprocessor boards to test themselves. Additional hardware, shown tinted, must be added to the original system. In the 8085-based system shown, 75% of all inserted faults were detected.

SR with the 2,047 PROM bytes, 1 byte at a time. In the SR, this data is compressed, and the final contents of the SR are compared by the microprocessor with the contents of PROM cell No. 2,048, which corresponds to the correct answer. If the two numbers agree, the PROM is good.

Testing of the RAM starts with loading its first page (the first 256 bytes) from the PRPG. Page 2 is then filled with PRPG contents plus page 1. Page 3 is filled with the PRPG contents plus page 2. Finally, page 4 is filled with the PRPG contents plus page 3. Then the entire 1-K byte of RAM is transferred to the SR, a byte at a time, and clocked after each byte. The signature in the SR after all the 1-K byte has been processed is transferred to the microprocessor and compared with a known answer stored in the PROM. The two numbers must agree; otherwise the RAM is defective and the number 5, designating the defective RAM, lights up on the display.

After the RAM test comes a comprehensive test of the microprocessor, designated as the MPU II test. In this software module, other 8085 instructions are executed. Intermediate results are checked with known-good answers. If computed values differ from the known answers at any point, the microprocessor fails the test.

Since the next test module (for the 8155) must test a RAM, an I/O port, and a timer, the RAM is tested first following the same procedure as that for the 1-K RAM. Next, the three parallel ports are tested, first as output ports and then as input ports. Operands 00000000 and 11111111 are used in these tests to detect a stuck-at-1 or a stuck-at-0 fault on any of the data paths.

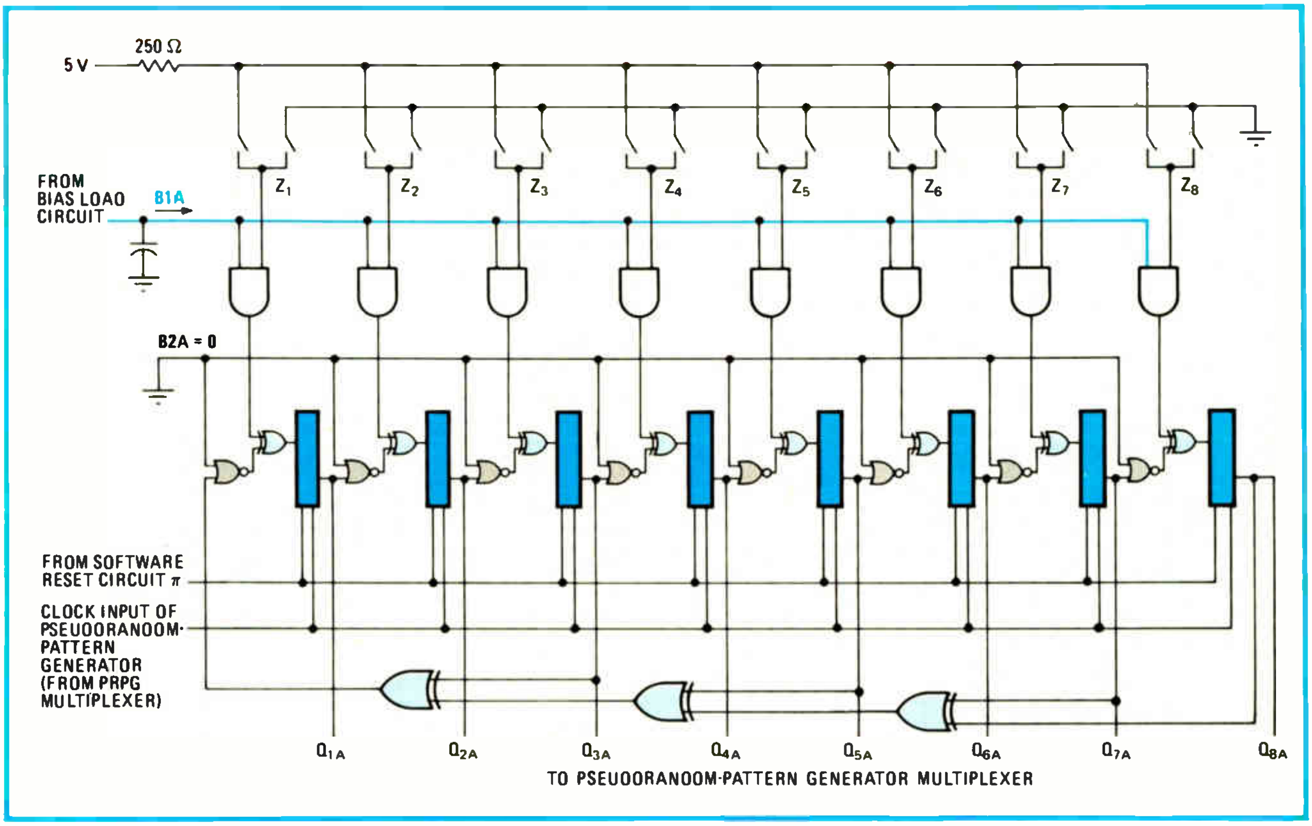
Last, the countdown timer is tested by loading a known number into the 8155's timer register. Then the timer is clocked; while it is counting down, program execution is passed to a time-delay routine. Timing is set such that if the timer is working correctly, it will finish its time period before the routine is completed.

Once the countdown is done, the timer sends a signal to the 8085's interrupt input. As a result, program execution vectors to a certain location, say location 3C. From here, program execution is transferred to a program that displays the hexadecimal digit C if the timer is good.

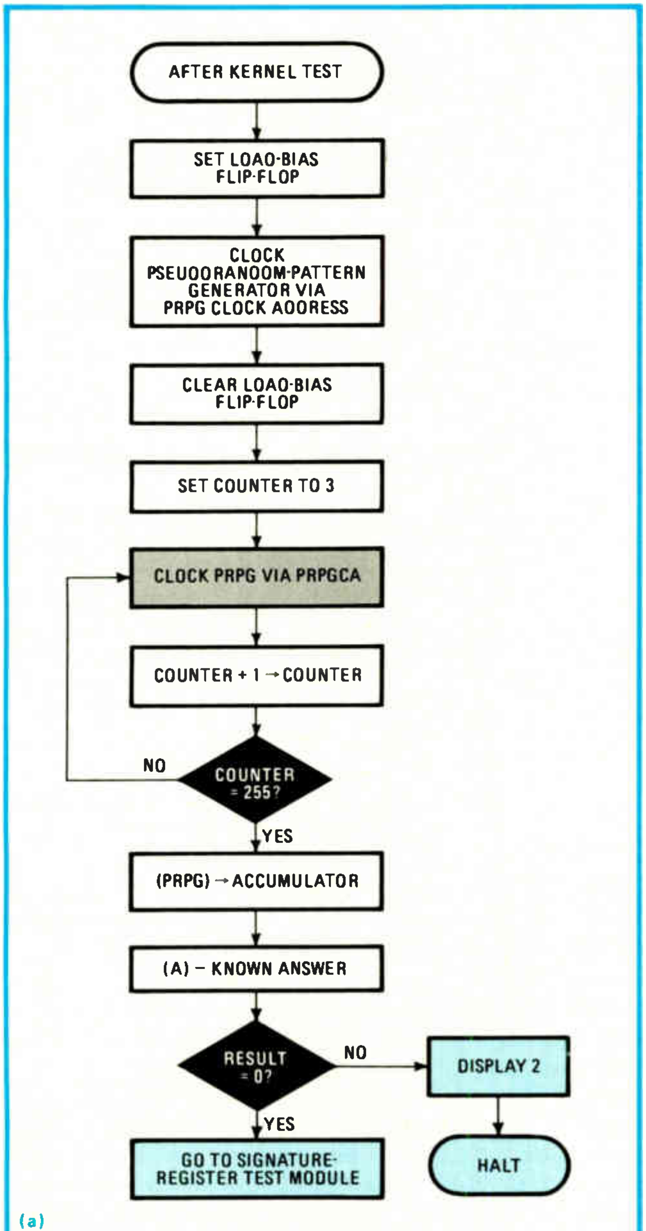
In the serial-I/O module, a 1 and a 0 are placed (a bit at a time) in the most significant bit of the accumulator. Then they are sent out to the serial-output-data pin of the 8085. This data is captured by the serial-port test logic and is fed back to the serial-input-data pin of the 8085. Each time, the captured data is compared with the earlier values. If they agree, the serial port is good.

The 8219 Multibus access arbitrator test module clocks the PRPG by using the Multibus address lines. The output of the PRPG is transferred to the microcomputer over the Multibus data lines and compared with a known-good answer. If the two agree, the chip passes.

To check the practical validity of the Microbit approach, a series of fault-detection experiments were carried out. To this end, certain hardware faults were intro-



2. Pseudorandom. The core of Microbit is two circuits: a pseudorandom-pattern generator and a signature register. Both are formed from the basic circuitry shown, a four-function linear feedback register. The state of control line B1A determines the circuit type.



(a)

```
;      PRPG TEST: IOEA IS TO CLOCK THE PRPG (256 – 1) TIMES
;
PRPG:   MVI  A, 00H    ;LOAO ACC WITH BIAS VALUE
        STA  SRESET    ; SOFTWARE RESET
        STA  SETB      ;SET LOAO-BIAS FLIP FLOP
        STA  PRPGCA    ;CLOCK IN BIAS VALUE
        STA  CLRB      ;CLEAR LOAO-BIAS FLIP FLOP
        MVI  B, 03H    ; LOAO COUNTER TO 3 !
LOOP1:  STA  PRPGCA    ;CLOCK THE PRPG
        INR  B         ;INCREMENT LOOP COUNTER
        JNZ  LOOP1     ;IF LOOP COUNTER NOT ZERO CONTINUE
        LOA  PRPGO     ;NOW OBTAIN THE PRPG REGISTER VALUE
        CPI  07FH      ;CHECK ACC FOR CORRECT FINAL VALUE
        JZ   SR        ;IF CORRECT GO TO –SR–TEST
        MVI  A, 02H    ;NOT CORRECT SO
        STA  EOIS      ;DISPLAY ERROR CODE –02–
        JMP  INIT      ; GO BACK TO INIT ROUTINE
```
(b)

duced and evaluated experimentally. All faults were either "output-stuck-at . . . " or "bus-stuck-at . . . ." Over 400 stuck-at-1 and stuck-at-0 faults were introduced after analyzing the system schematics for the most probable failures. Stuck-at-0 faults were introduced by grounding the involved circuit node, and stuck-at-1 faults were simulated by applying the collector supply voltage (+5 volts dc) to the appropriate point by means of a suitable resistor.

Approximately 75% of the artificially introduced faults were detected by the self-testing mechanism. Analysis of the undetected faults revealed that they all could have been detected if an attempt at optimizing the technique were undertaken.

Several other observations were made during the experiments that highlighted certain drawbacks in this self-testing approach. One problem is that the test has a limited resolution. That is, if a function (say, RAM) consists of 10 or more individual chips, the test will not pinpoint the faulty device. Rather, it will only signal that the RAM is defective. Another disadvantage is that the Microbit is an off-line test, whereas in many instances it is quite desirable to test a system while it performs its assigned functions. On-line testing essentially increases the reliability of a system by detecting functional faults as they occur.

Extending Microbit

Now that the Microbit self-testing concept has been proven, the next obvious step is to apply it to computer-based systems of higher complexity, for example, 16- and 32-bit machines. Conceptually, such an extension is straightfoward. In practice, however, there are certain obstacles that must be overcome. Chief among them is increased testing time. For example, with an 8-bit system, the system is cycled 256 times during testing. With a 16-bit system, the number of cycles would be upped to 2^{16}, unless some tricks are employed. One obvious approach would be to partition the testing, that is, to run two 8-bit test procedures on a 16-bit system. Such parallel testing would not only reduce the testing time, but would also permit the use of some of the software developed for 8-bit systems.

In any case, the incremental cost of implementing self-testing systems in 16- and 32-bit systems would be less because the amount of hardware added for testing does not increase linearly with an increase in system complexity. For instance, in the case of an 8-bit system, a total of 40 chips might be used, with 10 of those devoted to testing. As the number of chips on a board doubles, the number of Microbit chips may increase to, say, 15. Incrementally, the testing portion of hardware in an 40-chip 8-bit system is 25% as against about 19% in an 80-chip system. □

3. Self-testing. A flow chart of the self-testing routine of the pseudo-random-pattern generator is shown in (a). The actual debugged program is shown in (b). The 15-line program is totally independent and, other than a start-stop switch, requires no external equipment.

Software checks testability and generates tests of VLSI design

This adjunct to Tegas computer-aided-design package tells how easy a circuit design is to test and passes results on for automatic test generation

by Tom Kirkland and Victor Flores, *Comsat General Integrated Systems Inc., Austin, Texas*

☐ The technological advances that made very large-scale integration possible also created a dilemma for the designer. It is now possible, and often easy, to design digital circuits that cannot be produced either because they are not testable or because it is too costly to develop good tests for them. Several techniques, termed design for testability, have emerged to aid design and test engineers in realizing testable designs. These techniques range from those that impose structure on the engineer, such as level-sensitive scan design (LSSD), to simple cookbook-like rules based on an engineer's personal experience.

Now, a new set of software is aiming to bridge that gulf between designer and tester regardless of the technique employed by the designer. Called Coptr, for controllability-observability-predictability-testability report, it adds a new measure, that of testability analysis, to the existing techniques of controllability and observability-predictability analysis. The testability results are then used to drive an improved automatic test generator (ATG) to produce tests for complex digital circuits.

Controllability-observability analysis is a powerful tool when used with an advanced test-generation algorithm in the production of digital test patterns. Not only is execution time reduced significantly and detection percentage greatly improved, but the number of patterns needed to detect a fault is reduced compared to previous programs.

By combining circuit analysis and test synthesis in a single program, Coptr assures its users that if the program grades a design as more testable, it is in fact easier to generate tests for it. Thus, a designer need not worry that an improvement in the testability numbers generated by the Coptr program and explained below will not result in improved test generation. By passing the testability figures from analysis to test generation, Coptr avoids the problem of incompatible systems.

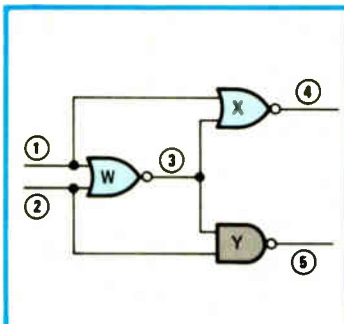
Totally automatic test-pattern generation for VLSI may still be in the future, but Coptr/ATG provides a powerful tool for the design or test engineer to reduce the amount of work involved. Further, the network evaluation of testability supplied by Coptr not only identifies those portions of a circuitry network that are difficult to test, but also yields a figure of merit that can be used by the designer to assess the testability and improve the design. Thus, these tools both enhance the design-for-testability process and also relieve most of the tedium of test-pattern generation.

Coptr evaluates a design in three stages: controllability analysis; observability analysis; and testability analysis. Each stage computes a set of numbers for each point in the circuit, or network. The numbers generated represent the relative weights assigned to each point in that network. From the numbers, a designer can get an overall idea of the testability of the design as well as particular information about trouble spots.

A definition of terms

The only way to control a digital circuit is to apply known values to its inputs. Controllability analysis is an attempt to analyze how easily a particular point in a digital circuit can be set to a desired value—a 0 or a 1. Thus, controllability analysis is a method of determining the simplest set of inputs that are required to create the desired result.

In Coptr, four controllability values are computed for each node in a network: combinational-0 controllability, combinational-1 controllability, sequential-0 controllability, and sequential-1 controllability. Combinational controllability is a number that represents the least number of nodes that have to be set to control the desired node, plus the node itself. Sequential controllability is a number that represents the number of states into which a circuit must be set before the desired value can be made to



NOR-gate status	NODE 1	2	3	4	5
Good	0	0	1	0	1
	0	1	0	1	1
	1	0	0	0	0
	1	1	0	0	1
Output stuck at 1	0	0	0	1	0
	0	1	0	1	1
	1	0	0	0	0
	1	1	0	0	1

1. Fault detection. The simple circuit above demonstrates the concepts of controllability and observability. To check for a stuck-at-0 fault at node 3, both inputs 1 and 2 must be controlled. To observe a fault, either node 4 or 5 can be watched, as the truth table shows.

occur at the node. To achieve a complete analysis, these values must be computed in both the combinational and sequential sense for setting a node to 0 and to 1, hence the four controllability values.

Just as it is important to control a particular node, so also is it important to be able to observe the value of each node. This measure, called observability, is determined by the number of other nodes that must be set to cause the value of the particular node to be observed at a circuit output.

As in controllability analysis, observability implies both combinational and sequential values. Thus, each node has a combinational observability value that represents the least number of nodes through which the value must propagate to reach some output at which it can be observed. It also has a sequential observability value that represents the number of states the circuit must be set to before the desired logical value is observed at the output.

Observability is associated with the inputs, and controllability is associated with the outputs of elements. The three observability values must be obtained for each fan-in of an element, while the four controllability values are obtained for each element output.

The observability figures cannot be computed until the values of controllability have been fully computed. Some nodes in a circuit may be uncontrollable, unobservable, or both. These nodes will affect the controllabilities and observabilities of other nodes, of course. For example, if an input to an AND gate is uncontrollable to a 1, then the other inputs to the gate will be unobservable.

For use in test generation, however, still a third measure is required, test observability. Called testability in Coptr, test observability is defined as the number of nodes that must be set, combinationally and sequentially, to allow a sensitized value to be observed at a circuit output. Test observability differs from observability in that the output is a sensitized value—one whose value in a specific faulty circuit is different from that in its good counterpart. Observability, on the other hand, applies only to the good circuit.

There are many definitions of testability for digital circuits. The one used by Coptr is a measure of the ease of detecting a faulty node at the outputs of the circuit. It is derived from the number of nodes that must be controlled, the predictability of the nodes, and the observability of the faulty node. Testability analysis thus computes a number that represents the relative difficulty of detecting a stuck-at fault in a network at a particular point. The higher the number, the more difficult it is to test for a stuck-at fault on that node.

Combined with controllability analysis, testability analysis determines the relative difficulty of developing a test pattern to detect the particular faulty node. For example, Fig. 1. illustrates how difficult it might be to detect if the output of NOR gate W is stuck at 0 (SA0). To develop a test, at least two things must be done. First, the circuit inputs that should set the output of Gate W to a 1 must be determined. To set the ouput of W to a 1, the test engineer must be able to set both inputs to 0. Therefore, the node would have a combinational-1 value of 3, the two inputs that must be controlled plus the node itself. Since setting the inputs sets the output to 1, the node has a sequential-1 controllability of 0, no toggling of flip-flops, say, is necessary to produce a logic 1. Control of the two inputs alone will provide the criteria for determining the difference between a good circuit—with output of W at 1—and a faulty circuit—with output of W stuck at a 0.

Second, the difference in the output must actually be detected. Since the output of W is internal to the device, it must be propagated to one of the two output pins for the test engineer to observe what is happening at the node. For the value to propagate to the output of NAND gate Y, it must pass through one node and hence the node has a combinational observability of 1. The circuit does not have to be placed in any other state for the value to propagate to the output, and thus the node's sequential observability is 0.

Because the output of W is observable through a predictable path, the testability of the node is the same as its combinational observability, 1. If, however, the only propagation path of output W was through an unpredictable element, say a flip-flop that could not be set to a known state, the node would be untestable and in Coptr assigned a value of –1.

To measure the difficulty of the first task, controllability analysis was used; to measure the difficulty of the second, testability analysis was employed. Using both, it is possible to find the difficulty of developing a test for a fault at each node. But rather than have an engineer compute these measures, Coptr does it automatically.

Checking with Coptr

The first step in Coptr analysis is to code the network description using Tegas Description Language (TDL), the standard language of Tegas, a computer-aided–design and –manufacturing software system. Once the network is properly described, compiled, and linked, Coptr analysis can begin. No test patterns need be developed or simulation performed prior to the use of Coptr, and since Coptr analysis is very efficient and uses very little computer time even for large networks, it can be used early and often in the design process.

To illustrate how Coptr can be used to improve the testability of a design, consider the shift network of Fig. 2a. Once it has been coded, compiled, and linked with Tegas, the execution of Coptr for this circuit results in the Coptr report (Fig. 2b).

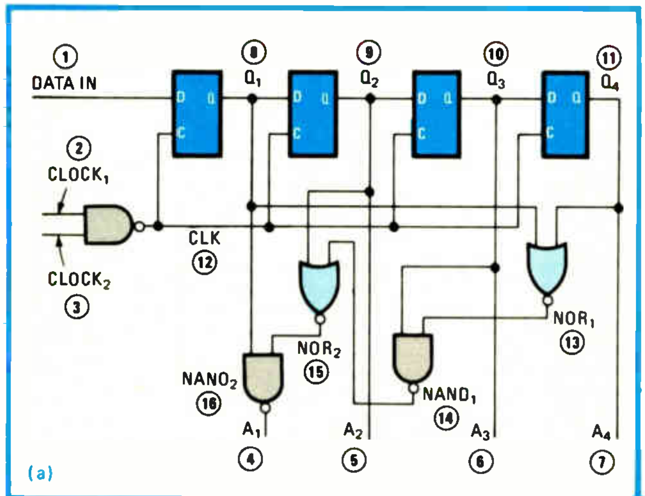
The first section of this report is the controllability section. This section contains two major columns: one for combinational and one for sequential controllabilty. Each has separate columns for 0 and 1 controllability values, for a total of four columns. The values in these columns indicate the relative ease of setting a particular node to a 0 or a 1. For example, to set node 4, the output A1, to a 0 requires that 75 nodes be controlled in all during a sequence of 11 states.

The presence of a –l indicates that the particular node cannot be controlled to the value for the column. Uncontrollable nodes can be the result of, say, an incompletely connected circuit. The presence of a –1 should trigger a further look at the circuit to determine why that node cannot be controlled.

None of the nodes of this circuit are uncontrollable, but it should be noted that nodes driven by uncontrollable elements are themselves uncontrollable. Because the effect may ripple through the rest of the circuit, it is important to identify the first uncontrollable element in such a chain and to determine why its output is uncontrollable. The presence of uncontrollable nodes in a network will also affect the observability analysis, so they should be eliminated as soon as possible.

The second section of the Coptr report in Fig. 2b is the observability section, which includes the testability figure. This section consists of three columns: combinational, sequential, and test. The combinational column indicates the number of combinational nodes that must be set to observe the indicated element output; the sequential column, the number of sequential states that must be induced.

The test observability is quite different. Since it includes not only the observability but also the predictability of each element in the observation path, it may be different from the combinational observability value. In fact, a particular node may be easily observable in the good circuit, but, because its obseration path contains an unpredictable element, it may be test-unobservable. An example of this in the report is element 12 (CLK), which is test-unobservable. Such difficulties can be removed by noting the reasons for such test unobservability and removing them; Coptr tells the designer where to look.



Circuit node number	Controllability				Observability			Name
	Combinational		Sequential		Comb.	Seq.	Test	
	0	1	0	1				
1	1	1	0	0	12	2	12	(DATA IN)
2	1	1	0	0	10	2	–1	($CLOCK_1$)
3	1	1	0	0	10	2	–1	($CLOCK_2$)
4	75	8	11	1	0	0	0	(A_1)
5	13	13	2	2	0	0	0	(A_2)
6	19	19	3	3	0	0	0	(A_3)
7	25	25	4	4	0	0	0	(A_4)
8	7	7	1	1	6	1	6	Q_1
9	13	13	2	2	0	0	0	Q_2
10	19	19	3	3	0	0	0	Q_3
11	25	25	4	4	0	0	0	Q_4
12	2	3	0	0	8	2	–1	CLOCK
13	8	33	1	5	42	6	42	NOR_1
14	53	9	8	1	22	3	22	$NAND_1$
15	10	67	1	10	8	1	8	NOR_2
16	75	8	11	1	0	0	0	$NAND_2$

(b)

Total 0-comb. controllability	347
Total 1-comb. controllability	252
Total 0-seq. controllability	51
Total 1-seq. controllability	37
Total combinational observability	118
Total sequential observability	19
Total test observability	90
Total 0-comb. uncontrollable nodes	0
Total 1-comb. uncontrollable nodes	0
Total 0-seq. uncontrollable nodes	0
Total 1-seq. uncontrollable nodes	0
Total combinational unobservable nodes	0
Total sequential unobservable nodes	0
Total test unobservable nodes	3
Average 0-comb. controllability	21
Average 1-comb. controllability	15
Average 0-seq. controllability	3
Average 1-seq. controllability	2
Average combinational observability	7
Average sequential observability	1
Average test observability	6

2. Testable? The shift circuit shown in (a) is analyzed by Coptr once it is described using the Tegas language. The Coptr report (b) indicates, by relatively high numbers in the test column, nodes that are hard to test, while –1s point to nodes that cannot be tested.

Improving circuit testability

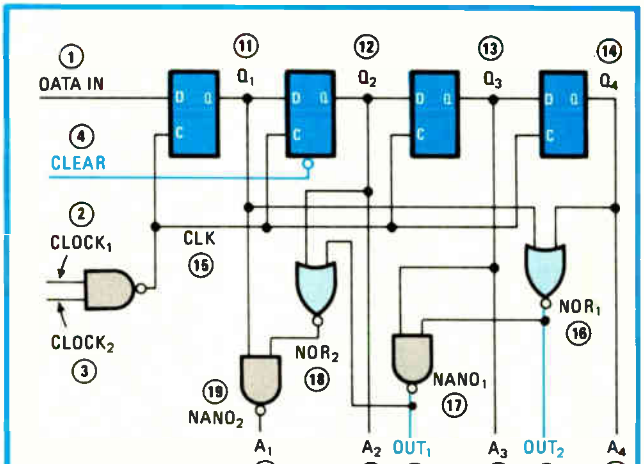
Coptr can be used in a variety of ways in the creation of more testable designs. To illustrate the techniques employed, the design of Fig. 2a will be refined by improving its observability and predictability, as in Fig. 3.

The quickest way to improve the observability of a circuit is to place test points at those nodes that are most difficult to observe. Since Coptr can identify these nodes, the engineer need only bring the nodes to output pins and rerun Coptr to observe how the changes that he has introduced in the design will affect the observability of that design.

While many designs have very few spare output pins to use for test points, the technique serves well for VLSI circuits where the relative increase in pins is small. The two least observable nodes internal to the circuit are the nodes NOR_1 and $NAND_1$. To improve their observability, each of these two points is brought to a new output: OUT_1 and OUT_2, respectively. The wiring changes necessary can be seen by comparing the logic diagram of Fig. 2a with that of Fig. 3a.

The testability of the circuit in Fig. 2a can be improved by eliminating the unpredictability of its elements as well. Unpredictable points are usually the beginning of a chain of untestable points, which are depicted by −1s in the Coptr report. The untestable nodes in the circuit are the $CLOCK_1$ and $CLOCK_2$ inputs and the CLK node internal to the circuit. These nodes are untestable because the clock's output (CLK), or node 12 in the Coptr report, is the input to a flip-flop that is unpredictable. Thus, the clock inputs and its output cannot be propagated to the output in a known way.

The flip-flop is unpredictable because there is no mechanism to set the device to a predictable state other than the clock to be tested. Consider the case when the flip-flop is turned on, a logic 1 is applied to DATA IN and $CLOCK_1$ (nodes 1 and 2 in the Coptr report, respectively), and a clock source to $CLOCK_3$ (node 3). After two clocks have been applied at node 3, a good circuit will have a 1



(a)

Circuit node number	Controllability				Observability			Name
	Combinational		Sequential		Comb.	Seq.	Test	
	0	1	0	1				
1	1	1	0	0	13	2	13	(DATA IN)
2	1	1	0	0	11	2	10	($CLOCK_1$)
3	1	1	0	0	11	2	10	($CLOCK_2$)
4	1	1	0	0	13	2	13	(CLEAR)
5	56	8	9	1	0	0	0	(A_1)
6	3	14	1	2	0	0	0	(A_2)
7	9	20	2	3	0	0	0	(A_3)
8	15	26	3	4	0	0	0	(A_4)
9	44	9	7	1	0	0	0	(OUT_1)
10	8	23	1	4	0	0	0	(OUT_2)
11	7	7	1	1	7	1	7	Q_1
12	3	14	1	2	0	0	0	Q_2
13	9	20	2	3	0	0	0	Q_3
14	15	26	3	4	0	0	0	Q_4
15	2	3	0	0	9	2	8	CLOCK
16	8	23	1	4	0	0	0	NOR_1
17	44	9	7	1	0	0	0	$NAND_1$
18	10	48	1	8	8	1	8	NOR_2
19	56	8	9	1	0	0	0	$NAND_2$

(b)

Total 0-comb. controllability	293
Total 1-comb. controllability	262
Total 0-seq. controllability	48
Total 1-seq. controllability	39
Total combinational observability	72
Total sequential observability	12
Total test observability	69
Total 0-comb. uncontrollable nodes	0
Total 1-comb. uncontrollable nodes	0
Total 0-seq. uncontrollable nodes	0
Total 1-seq. uncontrollable nodes	0
Total combinational unobservable nodes	0
Total sequential unobservable nodes	0
Total test unobservable nodes	0
Average 0-comb. controllability	15
Average 1-comb. controllability	13
Average 0-seq. controllability	2
Average 1-seq. controllability	2
Average combinational observability	3
Average sequential observability	0
Average test observability	3

3. Testable! Relatively simple changes to the circuit of Fig. 2 (a) make it much easier to generate tests for the circuit, as indicated by the Coptr report (b) generated by rerunning the program. Used by Coptr's automatic program generator, the report ensures test improvement.

output at A_2 labeled node 5 in Fig.2.

But will there be any difference if a fault is present at node 3? Unfortunately, the answer is maybe not. The uncertainty arises because if the flip-flop whose output node is Q_2 happens to power up with a 1 on its Q output, it will stay at 1 if its clock input is stuck-at-0 (SA0). After two clocks have been applied at input 3, the node Q_2 will still be at a 1, and the logical value at node 5 will be the same as if the clock were not stuck at 0.

The astute engineer might suggest at this point that the test person try to clock a 0 through input 1. This test will work only if the Q_2 node flip-flop does not power up with its Q output set to 0. Hence it becomes obvious that the difficulty in testing the circuit is that it is not possible to predict how to test it until after some tests have already been run; a series of values at the outputs must be observed in order to detect if the clock is stuck at either 0 or 1.

The reason it cannot be tested with a single value at a single output is that the state of the flip-flop output could not be predicted. But if the initial state of the flip-flop could somehow be predicted, the circuit could be tested for a stuck clock with a single observation on a single output. To improve the predictability of a flip-flop is a relatively simple matter in the design stage; the designer need only add an accessible preset, or clear, input line as shown in Fig. 3a. The line permits the flip-flop to be controlled independently of the clock and set to a known value at power-up.

Rerunning Coptr on the improved circuit produces the result shown in Fig. 3b. As seen in the report, not only have the testability and observability of signals NOR_1 and $NAND_1$ been improved, but the CLK signal has also been made testable. And whereas the testability of some nodes, such as DATA IN, has become slightly more difficult, the overall testability of the circuit has improved significantly, as can be seen by comparing the total test-observability figures for each circuit.

The improvement process need not stop here; further refinements can be made in the circuit by connecting the CLR signal to the clear inputs of the other flip-flops. This will make each flip-flop predictable and will result in an even more testable design. The process of improvement should continue until the designer is satisfied that the design can be tested as economically as possible. There is, of course, a tradeoff between the economics of improvement and those of testing. However, in almost all cases this balance is heavily in favor of improvement very early in the design process, since the reduction in cost of testing improves by an order of magnitude at each stage in the production process.

Information in the Coptr file is accessed by the ATG program to make intelligent path and pattern choices. Coptr data is used in two separate ways: during forward propagation and during backward propagation.

As noted earlier, each fan-in to an element has an associated set of values for observability. These observability values are used during forward propagation to make an intelligent choice of the fan-in that will most likely result in propagation of a fault to an output. Like road signs in the forest, these values are used by the ATG program to determine when to turn right or left, and when to continue straight ahead.

The result is that more straightforward paths are taken and much less time is spent examining fruitless paths. In addition, paths that are known to be unobservable are skipped entirely. For a given amount of computer time, the resulting improvement in efficiency produces smaller test sets as well as higher fault-detection percentages.

During the process of backward propagation, the values of node controllability are used to select from among the inputs of an element the most promising path and pattern for sensitizing. If it is necessary, for example, to produce a 0 on one of the inputs to an AND gate, the input that is most controllable to a 0 is chosen. This will usually result in the fastest and easiest test pattern.

Additionally, if a particular pattern cannot be produced because certain inputs cannot be controlled, the pattern need not be tried. An example of this would be an attempt to produce a 1 on the output of an AND gate when one of its inputs is not controllable to a 1. Obviously, the designer would like to know of such a situation (and will through Coptr), but so would the ATG program. The Coptr file informs it of such cases.

A COMPARISON OF AUTOMATIC TEST GENERATION RESULTS WITH AND WITHOUT COPTR

Circuit type (64 bit)	Number of faults	Fault detection (%)		Execution time (min, s)	
		Coptr	Other	Coptr	Other
Adder	2,850	100	100	2, 12	12,0
Arithmetic and logic unit	5,464	98	83	9, 57	n. a.
Counter	2,505	95	0	15, 0	n. a.

Test data

The Coptr/ATG system has been tested on a variety of circuits, both combinational and sequential. The results for three such circuits using Coptr are shown in the accompanying table, along with the results obtained from an existing implementation of an older automatic test-generation algorithm and without network analysis.

Results have been considered not available (n. a.) where no good estimate for how long the older program would have run could be obtained, as it was stopped when the results were obviously uneconomical in terms of computer time. This waste of valuable computer time does not happen with Coptr/ATG, since obviously useless paths and patterns are never tried.

As shown, the Coptr/ATG combination provides significant improvement in execution speed for the simpler combinational circuits, while making it possible for the first time to generate tests for larger sequential circuits such as the 64-bit counter. Because of its highly sequential nature and large number of propagation paths, this circuit had previously resisted all efforts to automatically generate test patterns. □

Dynamic logic lends C-MOS power levels to low-cost p-MOS microcomputer

Recasting a popular 4-bit chip in all-dynamic circuitry achieves milliwatt active power in an economical process

by Jerald Leach and Ben Oliver, *Texas Instruments Inc., Houston, Texas*

□ Dynamic circuitry cuts a unique path among the options for cost, power, and performance in MOS integrated circuits. Economizing on the number of transistors, consuming little or no dc power, and often switching faster than static circuits, a little dynamic logic has been the savior of many a chip designer. In some applications, at least, there is good reason to go to the extreme: recasting an entire logic IC in dynamic circuitry achieves the low power consumption of complementary-MOS at the lower cost of a p-channel MOS process.

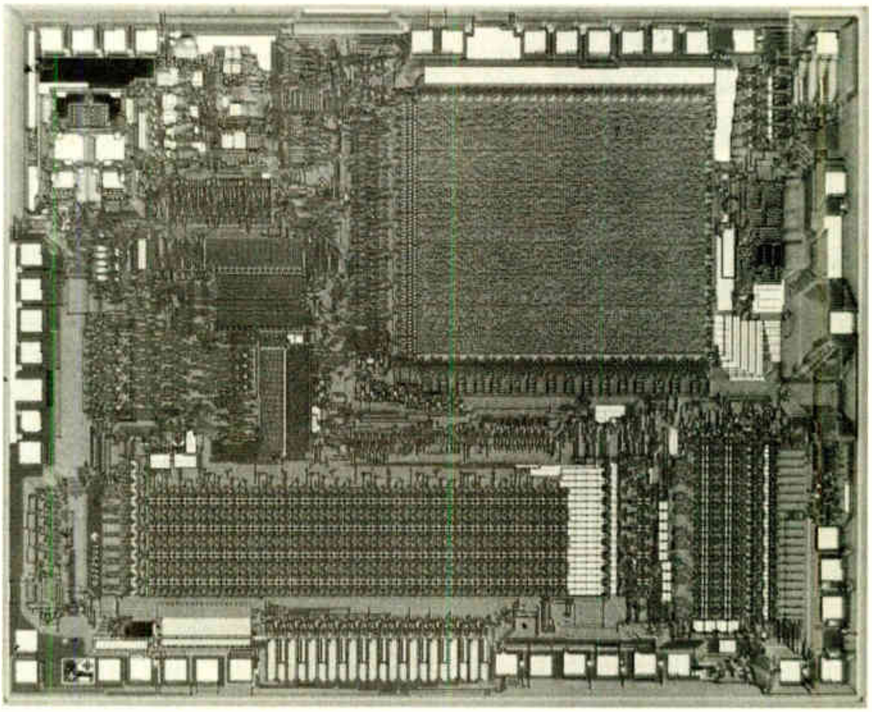
That claim is made for a family of dynamic logic circuits called L-MOS (for low-power MOS) that closely resembles n- or p-channel MOS in cost and performance, because the fabrication process differs only slightly from the conventional one. At the same time, wholly dynamic circuit design eliminates almost all of the dc current paths on the chip, limiting standby power consumption.

Though static C-MOS circuitry may still be preferred for ease of design and large noise margins, the L-MOS alternative suits very cost-sensitive applications. The first L-MOS ICs are 4-bit microcomputers that directly drive liquid-crystal displays (Fig. 1), the sort of chip going into hand-held calculators. Because of simpler processing and denser layouts, these p-MOS chips cost less than comparable C-MOS units.

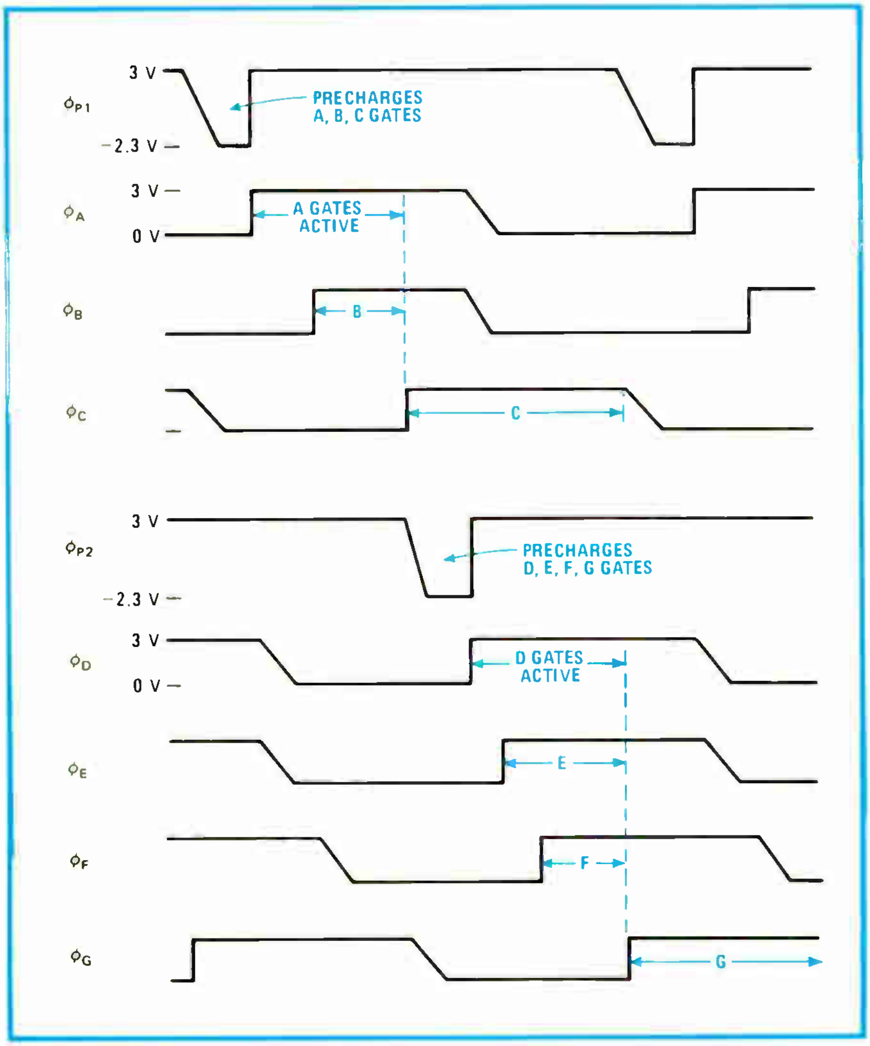
Unfortunately, limitations of dynamic circuitry prevent L-MOS from tackling all of the product lines served by C-MOS. For one, to achieve C-MOS logic levels (from ground to the power supply) in a p-MOS circuit, some nodes are bootstrapped, or pumped, below ground level, and this requires a supply voltage of at least about 2.5 volts. Watches and hearing aids that operate on battery voltages below 2 V are therefore excluded. Also, dynamic circuitry rarely eliminates standby current completey, as in, for example, the case of C-MOS. Therefore, long-term battery backup, such as might be needed for memories, also precludes L-MOS.

L-MOS constitutes a circuit design technique that can be applied to either n- or p-MOS devices, with the former usually chosen for higher performance and the latter for lower cost. Conventional static logic circuits in either p- or n-MOS dissipate both dc and ac power. The ac, or transient, current consumed to charge and discharge the capacitance of devices and their interconnections increases in proportion to the switching frequency and at low frequencies is insignificant compared with the constant dc current. If the constant current is eliminated, then n- or p-MOS circuitry will consume no more power than C-MOS. The essence of L-MOS is its almost exclusive dependence on dynamic logic gates, which consume no dc current and can be clocked at low rates for a low standby-power consumption.

In fact, on the TMS 2220 microcomputer, only the oscillator circuitry, which generates the clock signals, consumes any dc power. This circuit, though it uses



1. C-MOS or p-MOS? Although built in a p-channel process, this 4-bit microcomputer's dynamic circuitry operates at C-MOS power levels. Thanks to fewer transistors per gate and a more compact layout, the 30,000-square-mil chip is about 25% smaller than C-MOS units.



2. Seven phases. The clocking scheme for the gates calls for two precharge periods and seven phases (A through G). The intervals (color) show when the gate types of Fig. 3 are active as determined by the combinations of clock signals controlling the gates.

tion means that to implement the NOR function, additional input transistors are connected in series with the ones shown. Conversely, additional input devices in parallel create the NAND function.

Each of the seven types of gate is active in sequence, as determined by the combinations of clock signals controlling the gates (see Fig. 2 again). A logic network is then implemented with phase-A gates constituting the first stages, phase-B versions in the second level, and so on, through phase-G gates in the seventh level of logic, each responding in its turn in one of the seven phases of the clocking period.

In this way, precharging operations do not interfere with the logical operations, and every gate is constrained to switch in a known time interval. One instruction cycle of the 2220 therefore comprises seven stages of logic gates—that is, every operation must be implemented with seven or fewer sequential logic functions.

In addition to the seven gate types shown, two types that do not use precharged outputs are also occasionally needed. For example, in a dynamic random-access memory, if all of the address lines were precharged low, the cells would be shorted together and lose their stored information. Lacking the precharge function, these gates must be larger and higher-powered than the others and are therefore avoided wherever possible. Where they are used, they are active on the third and seventh phases of the timing chain.

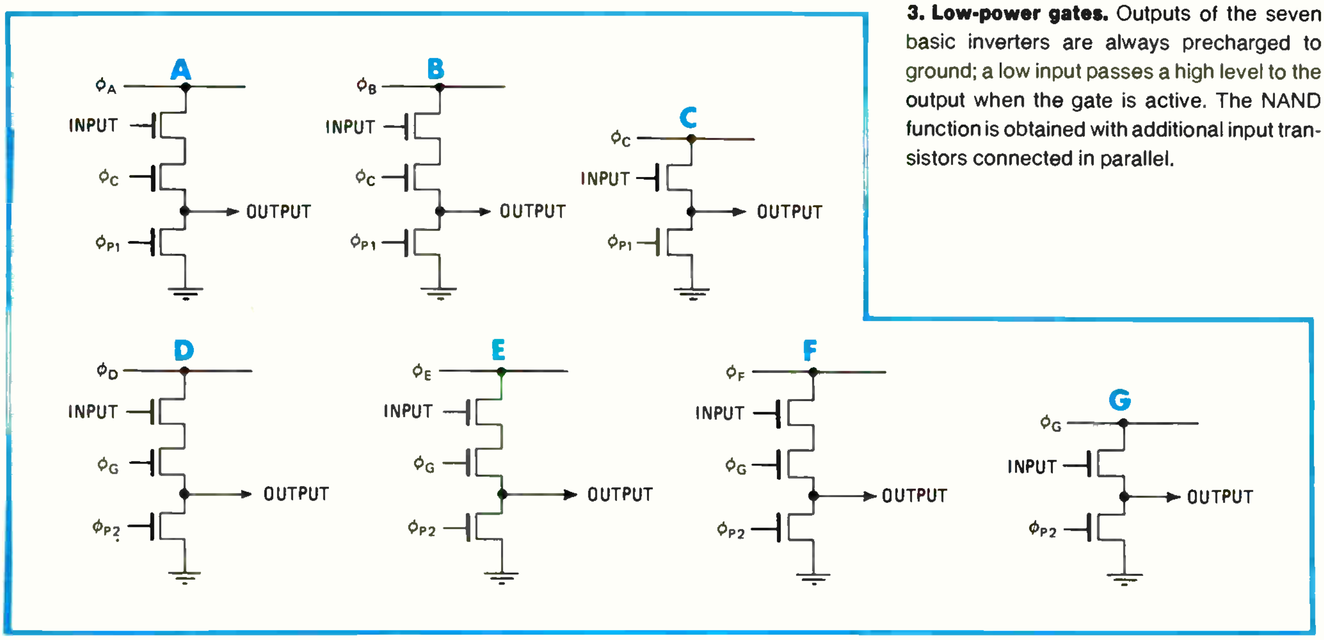
dynamic logic gates, also incorporates push-pull buffers that dissipate standby power. As might be imagined, completely dynamic logic for a large-scale IC demands a complex clocking scheme. A total of nine clock signals (Fig. 2) is used in the chip's seven-phase timing chain. The clocks are driven all the way to 0 V by signals that are bootstrapped below ground. In addition, two of the nine clocks are themselves pumped to −2.3 V, for use in precharging logic gate outputs to ground.

Seven stages of logic

Seven basic gates, all dynamic, provide the microcomputer's logic functions (Fig. 3). In each case, the output is precharged to ground when either the Φ_{P1} or Φ_{P2} clock goes low. When the other clocks controlling a gate are active, the input can affect the output. For example, a phase-A inverter is active when Φ_C is low and Φ_A is high. When that happens, a low (0-V) input will turn on the input transistor, rapidly driving the output high. On the other hand, a high input keeps the device off, and the output remains at ground. As the inputs are active when low for p-channel devices, a positive logic conven-

The 2220 microcomputer is the first member of the 4-bit TMS 1000 family to be recast in L-MOS. Its hardware implements the signals for scanning the lines of an LCD; the data to be displayed is loaded either directly or through a decoder, into the display RAM. All of the clocking for the display is generated by hardware. The chip includes 2-K bytes of mask read-only memory and a 128-by-4-bit RAM. Clocked at 300 kilohertz, the chip consumes a maximum of 2 milliwatts from its 3-V supply. In the standby mode, the clock rate is reduced to 15 kHz, and the power consumption drops to 180 microwatts or less. To maintain the dynamic RAM's data with this low clock rate, the entire array is refreshed at once, rather than row by row. With conventional sequential refreshing on such a low clock rate, the stored charge would leak away before it could be restored. In fact, the entire chip will operate correctly on the slower clock, although obviously at about one twentieth the execution speed.

In addition to the standby mode, which maintains the



3. Low-power gates. Outputs of the seven basic inverters are always precharged to ground; a low input passes a high level to the output when the gate is active. The NAND function is obtained with additional input transistors connected in parallel.

stored data and hence the data being displayed, a halt mode can be initiated by setting a bit in one of the registers. The chip then shuts down all of its circuitry, and the only power consumed is that due to stray leakage paths through the devices, totaling some 3 μW.

With such low power consumption, the typical battery life of a calculator using an L-MOS chip will be some 3,000 hours from two silver oxide button cells (rated at 180 milliampere-hours). That figure is comparable with C-MOS microcomputers. However, the L-MOS chip costs far less to produce than the C-MOS version.

To begin with, the L-MOS process is essentially that of metal-gate p-MOS and requires seven mask levels for p^+ diffusions, gate oxides, two contact hole cuts, metalization, a boron implant, and contacts to the bonding pads. Although the boron implant, used in conventional p-MOS to make depletion-mode load devices, is not needed for that purpose in L-MOS because dynamic logic uses no load devices, the step is retained and done after the gate metaliztion. With that modification, the implant can be used to self-align source and drain regions to the metal gates as well as to form resistors.

In contrast, a metal-gate C-MOS process calls for five more mask levels, including p-well and n^+ diffusions, a phosphorus implant, and threshold-adjustment implants for both transistor types. Besides a higher processing cost, C-MOS chip area will be larger than that for n-MOS or p-MOS, even if dynamic logic is used. The C-MOS gates require both a p well for the n-channel transistors and a p^+ guard ring. The L-MOS implementation saves about 25% of the area, both because these two features are absent and because the output contacts only one diffusion in the L-MOS case, but two in a C-MOS gate.

Those savings yield a die size of 30,000 square mils for the 2220. As a result of the smaller die and the simpler processing, 2220s will sell for around $3, as against $5 to $8 for comparable C-MOS units.

The success of L-MOS in the application described hinges on several factors, primarily the premium placed on a low-cost implementation and the relatively relaxed timing constraints. In contrast, present very large-scale ICs, such as 16-bit microprocessors, are reaching clock rates 30 or 40 times faster than the 2220's 300 kHz. The vagaries of completely dynamic logic—involving for the most part the relative timing of the various clocks at every point in a system—present a stiff challenge in such an application. However, much can be gained from conversion to dynamic circuitry, even if some functions are left in static logic.

The power dissipation of static n-MOS logic is already pushing the limits of readily available packaging technology. Although a few well-placed C-MOS gates can dramatically reduce the dc power consumption of n-MOS logic chips, dynamic circuitry can do the same job in the simpler n-MOS process.

However, because the dynamic logic gate's output must be precharged (to ground in the p-MOS case and to the power-supply voltage for n-MOS circuits), the timing of critical operations is complicated. With multiple clock phases, the precharge operation can generally be removed from the critical paths; if it can, dynamic logic can be even faster than static implementations.

In a static n-MOS logic gate, the load device (generally a depletion-mode transistor) limits the switching speed. The ratio of the load transistor's length to width is usually around seven times the driver transistor's to optimize the logic threshold. As a result, the load device's current capability is reduced, and the rising transition is slowed. If a minimum-geometry transistor acts as the load device to make that transition as fast as possible, the driver device must be proportionately wider, to present a larger capacitance to preceding stages.

In contrast, if dynamic circuitry can be used, the rising transition is handled by the precharge operation, and in many or most cases a fast, minimum-size driver accomplishes the downward transition. Such reasoning has already led many designers to the use of dynamic circuitry in advanced static parts, like fast RAMs. □

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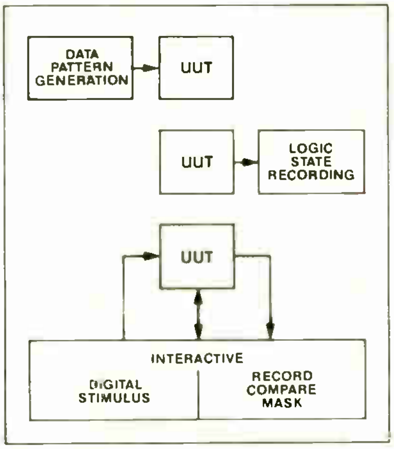

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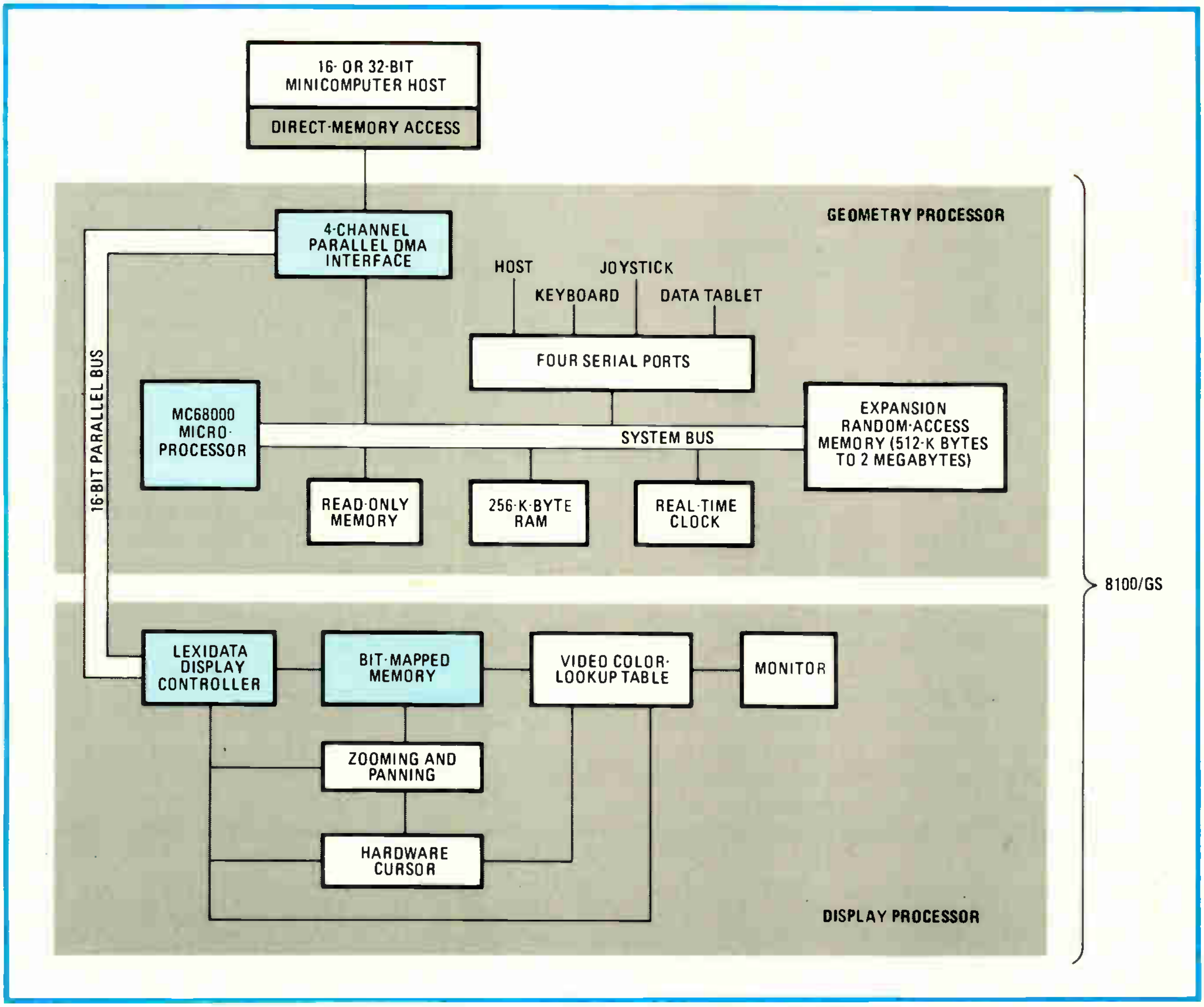
Multiple processors equip terminal for high-level graphics functions

Host computer's processing load drops; original-equipment makers can treat the subsystem as an intelligent building block

by Sheldon Lowenthal and David Grabel, *Lexidata Corp., Billerica, Mass.*

□ Taking over the bulk of the geometry-processing and display-control functions from the host computer, the Lexidata 8100/GS provides the basis of a distributed-processing raster-scanned graphic subsystem. With multiple-microprocessor intelligence, this terminal gives builders of computer-graphics systems a powerful new tool. It also incorporates high-level interactive graphics software so that the system designer can focus on developing application programs without having to build the fundamental graphics-support software first.

The 8100/GS combines the advantages of high-resolution color raster graphics with an object-oriented data



1. Picture power. The basic architecture of the 8100/GS is a hierarchy. The graphics processor, based on a Motorola MC68000 microprocessor, handles the picture generation. The proprietary 12-bit bipolar display processor generates the screen images.

What interactive computer graphics takes

As the capabilities and cost-performance ratios of computer graphics hardware have increased, the sophistication of its application software has also risen. The first interactive computer-graphics system was the SAGE air defense system, and it was essentially just informational. Soon after, graphics systems for computer-aided design were displaying images of three-dimensional real-world objects such as cars, printed-circuit boards, and integrated circuits.

What made the design of these important products possible was the development of algorithms for converting mathematical descriptions of objects into lists of vectors to be displayed. The mathematical representation defines the objects in terms of a high-precision, 3-d cartesian-coordinate space known as world coordinates. By applying scaling constants, the user can convert world coordinates into micrometers, mils, grid units, or any other unit of measurement.

For most applications, a world-coordinate representation is too detailed to be displayed, even with the highest-resolution displays. So, often a window is defined around a small portion of the object and it alone is displayed.

The window operation is typically performed with what is known as the Cohen-Sutherland windowing algorithm and a clipping algorithm. These two algorithms determine which vectors are to be displayed, which vectors cross one or two edges of that window, and where those vectors intersect the window.

The algorithms for transforming 3-d objects into 2-d displays, translating, rotating, and scaling them, as well as those for windowing and clipping, involve much computation, even for simple objects. Complex shapes and designs typically contain hundreds of thousands of vectors. Early interactive graphics systems therefore implemented these algorithms in special-purpose hardware. These experimental systems could transform objects in real time, but they were too expensive for industrial use.

However, the development of software support tools for large computers brought computer graphics into industry. One set of these tools mainly serves analytic environments yielding large amounts of data; examples are economic studies, deomgraphics, and scientific data. A second set serves turnkey interactive computer-graphics systems intended chiefly for computer-aided design and manufacturing and for business presentation graphics.

Within the last 10 years, a third class of software has been developed by several manufacturers of computer-

structure; that is, one composed of fundamental graphics elements describing a real-world object to be modeled. The dual-processor architecture and the rich set of programmed functions support extensive manipulation of screen images. This manipulation can be accomplished either by transforming the objects or by changing window size or position.

Manipulating images

Objects may be transformed by any combination of scaling, rotation, or translation, and the corresponding image changes are immediately reflected on the screen. When additional detail is required, the window size can be changed dynamically, providing a software zoom capability. Changing a window position effectively pans over the locally stored object data.

In addition to offloading display functions, the 8100 serves as a front-end input processor. It supports interactive peripherals such as a data tablet, a keyboard, and a joystick. The intelligence in the terminal processes the data from these peripherals, as well as echoing keyboard entries without interrupting the host computer. Responses to commands are presented to the operator in real time, even though the host might be heavily loaded with other tasks. The host is free to maintain system resources, such as large master disks, data bases, line printers, and communications hardware. Thus it is possible to support multiple 8100 graphics terminals from one host—a significant cost-saving.

The 8100/GS uses a hierarchy of three processors (Fig. 1) linked together with a parallel direct-memory-access interface or an RS-232-C interface. It consists of two resident processors; the geometry processor that maintains the object data and the display processor that manages the frame buffer and the video controller. Completing the hierarchy is the user's host computer, which functions as the master controller.

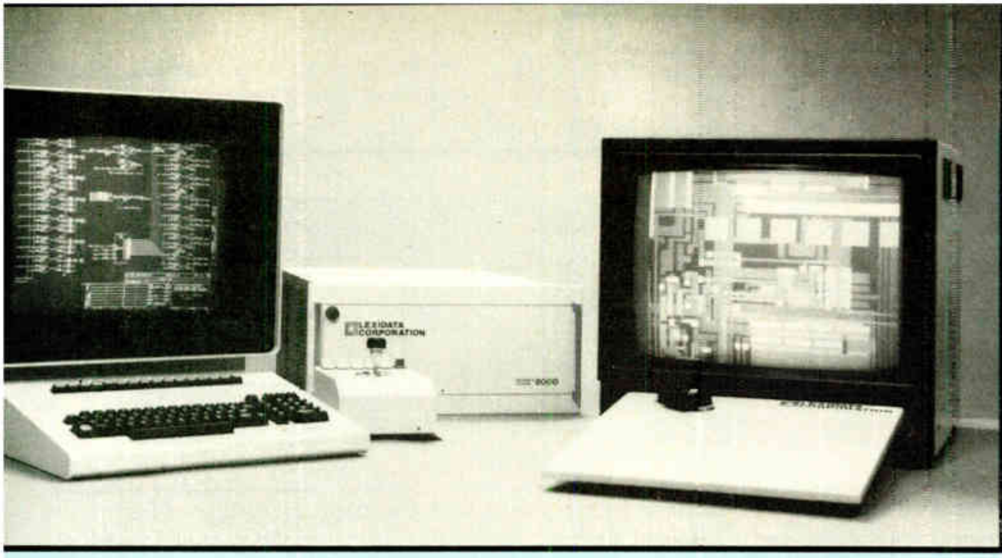
A Motorola MC68000 microprocessor provides the computational power for the geometry processor. There are sixteen 32-bit registers for addressing and data manipulation. The processor's 14 addressing modes, 16-megabyte direct-addressing range, and rich instruction set make it extremely fast—ideal for geometrical tasks.

The 8100/GS controller board contains the following features in addition to the MC68000:

- Four serial ports to communicate with peripherals, such as keyboard, joystick, and data tablet, and optionally with a host at up to 19.2 kilobits per second.
- A real-time clock for the operating system.
- 256-K bytes of random-access memory for software, buffers, and stacks.
- Up to 48-K bytes of programmable read-only memory for self-testing, bootstrapping, and utility programs.
- A bus interface for additional RAM and future expansion of peripherals.
- Four high-speed, full-duplex DMA channels to communicate with the host computer and the display processor.

The memory in the basic system can be expanded by adding 512-K bytes to 2 megabytes of error-correcting RAM. Parallel DMA interfaces are available for most popular 16- and 32-bit minicomputers. Host links over longer distances use the RS-232-C interface.

The display processor controls bit-map manipulations and other video-display functions. This proprietary 12-bit bipolar microprocessor executes a display-oriented instruction set at 225 nanoseconds per instruction. It has a 4-K-word program memory for the execution of



tube and to display any new views of it or alterations to it quickly. It is also often desirable or necessary to display these changes dynamically—to drag or rotate a shape across the screen, for instance. Moreover, the host computer controlling these applications is often shared with other users doing a variety of tasks, such tasks as software development, plotting, finite-element analysis, and pattern generation.

graphics terminals. These programs are generally interactive packages for use on a variety of minicomputer and mainframe host computers. They execute the basic graphics and display computations on the host and generate the commands to drive the display. Though they save users the trouble of developing them, they take up a lot of the host's time and occupy much of its memory.

All three categories of computer-graphics applications have several requirements in common. Each needs to display an image of a real-world object on a cathode-ray

The trend now is to unload the burden of all this graphics processing onto very intelligent display terminals. With this distributed approach, a less expensive host can be used, or a given host can either handle more terminals or be freed up for other applications without reducing response time to the terminal operator. The Lexidata 8100/GS shown above, can serve in any of these situations, for all the functions for creating and manipulating an image on the raster display are executed entirely within the terminal.

GDOS, Lexidata's graphics-display operating system.

Six basic display models offer a wide range of resolutions, extending to 1,280 by 1,024 picture elements in either color or monchrome. Options include hardware zooming and panning, blinking, and overlay memories. Zooming and panning are nondestructive and instantaneous. Individual objects can be blinked without affecting other parts of the display. User application programs access the 8100 through a series of Fortran subroutines supplied by Lexidata. These subroutines link users' software with the 8100's parallel DMA interface. Since the 8100 performs all computations, this subroutine library merely reformats data. This method burdens the host much less than more traditional graphics packages do.

The general-purpose geometry operations of the 8100/GS build on a commonly recognized set of high-performance graphics functions. The basic model for the software is the Core standard proposed to the American National Standards Institute by the Graphics Standards Planning Committee (GSPC) of the Association for Computing Machinery's Special Interest Group on Computer Graphics (Siggraph).

Lexidata has used the two-dimensional subset of the GSPC Core as the starting point of the functions of the 8100/GS and has extended it to provide an even better interactive computer-graphics system. For example, the 8100 stores the complete coordinates for unclipped objects (see "What interactive computer graphics takes," above).

More recent efforts in graphic standardization have focused on the Graphic Kernel System (GKS). The 8100/GS Object Data Structure (ODS) is conceptually closer to GKS than it is to Core. Both the 8100 software and the GKS standard store retained segment data prior to window and clipping operations.

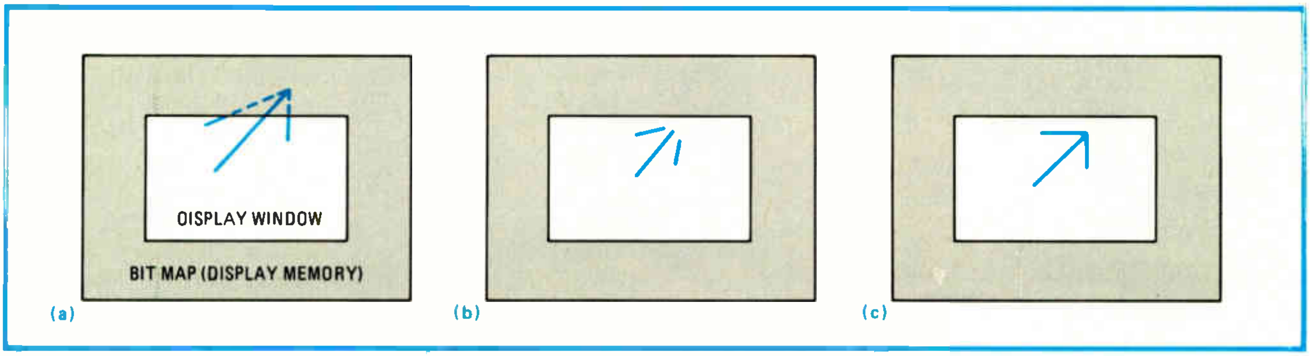
World coordinates are used to define an object in terms of its various component shapes located on the grid. A world-coordinate description can be most simply described as a geometrical representation of the object on a 2-billion-by-2-billion-coordinate grid. Most graphics software offers absolute device coordinates, which are device-dependent. In contrast, the 8100 world coordinates are device-independent, so they may be translated to absolute device coordinates for particular display resolutions without modifying the user's software.

Local data storage

The large direct-addressing space of the Motorola MC68000 and low-cost dynamic RAM make it possible for the 8100 to store the descriptions of complete objects in its local memory. This capability permits powerful manipulation of objects and helps minimize the transmissions between host computer and display processor.

The object-oriented data structure is based on simple graphics primitives, such as lines, polylines (connected sequences of lines), polygons, circles, text, and messages. Each primitive has a set of associated attributes such as a color-intensity index value that, together with the contents of the video color map, define the color (or gray scale) and intensity level. Lines, polylines, polygon outlines, circles, and text may be weighted (given a thickness in display units) or displayed as dashed lines. Polygons and circles may be filled or unfilled, and the fill may be either a solid or a pattern. Text and message strings are displayed in a user-specified size.

The data is organized in terms of segments—packets of



2. Clipped and restored. In a standard graphics-display system, the part of an image clipped by a window (a) will be missing when the image is changed (b). In the 8100/GS graphics processor, the clipped portion is stored in the object data structure and can be restored to the display (c).

primitive graphic data. They fall into three classes: temporary and retained segments, plus cells. Segments are collections of output primitives, and objects are, in turn, collections of segments.

Temporary segments, defined by the user, are not permanently retained in the data structure. This feature permits objects to be displayed until another operation causes the image of the object to be erased from the display.

Retained segments are the data structure upon which the 8100's powerful image-manipulation algorithms operate. Objects described to the subsystem may be stored under user control in these segments. A retained segment may be selectively modified by altering the conditions under which it is visible or by applying coordinate transformations to adjust its position and orientation. These features are known as dynamic segment attributes in the Core terminology.

Cells are a special class of segments, representing a concept that should be especially familiar to those who have been exposed to integrated-circuit computer-aided-design systems. The user provides descriptions of the objects within a cell. These cell definitions are similar to those for retained segments, but they specify such parameters as position, orientation, and scale for each instance in which the cell is used.

This cell feature adds enormous power to the 8100 by permitting the user to define and invoke special symbols unique to the application. Whereas retained segments are displayed as soon as they are defined, cell definitions are stored away and displayed only when indicated by the system user. What's more, cell definitions can be included in other cell definitions, nested to a depth of 32 levels.

Controlling the view

The 8100 provides users with a good deal of control over the physical display itself. They may partition the screen into subsets called viewports, which may overlap. They may then define one or more rectangular windows into the world-coordinate space containing the picture and project each of them into a specified viewport. Thus any rectangular portion of the picture may be displayed at any magnification.

The data structure also lets the user change a window and automatically update the display with a different view of the image. The software zoom shows the object in greater detail than does the pixel replication used in a hardware zoom. The windowing operation is performed completely by the 8100.

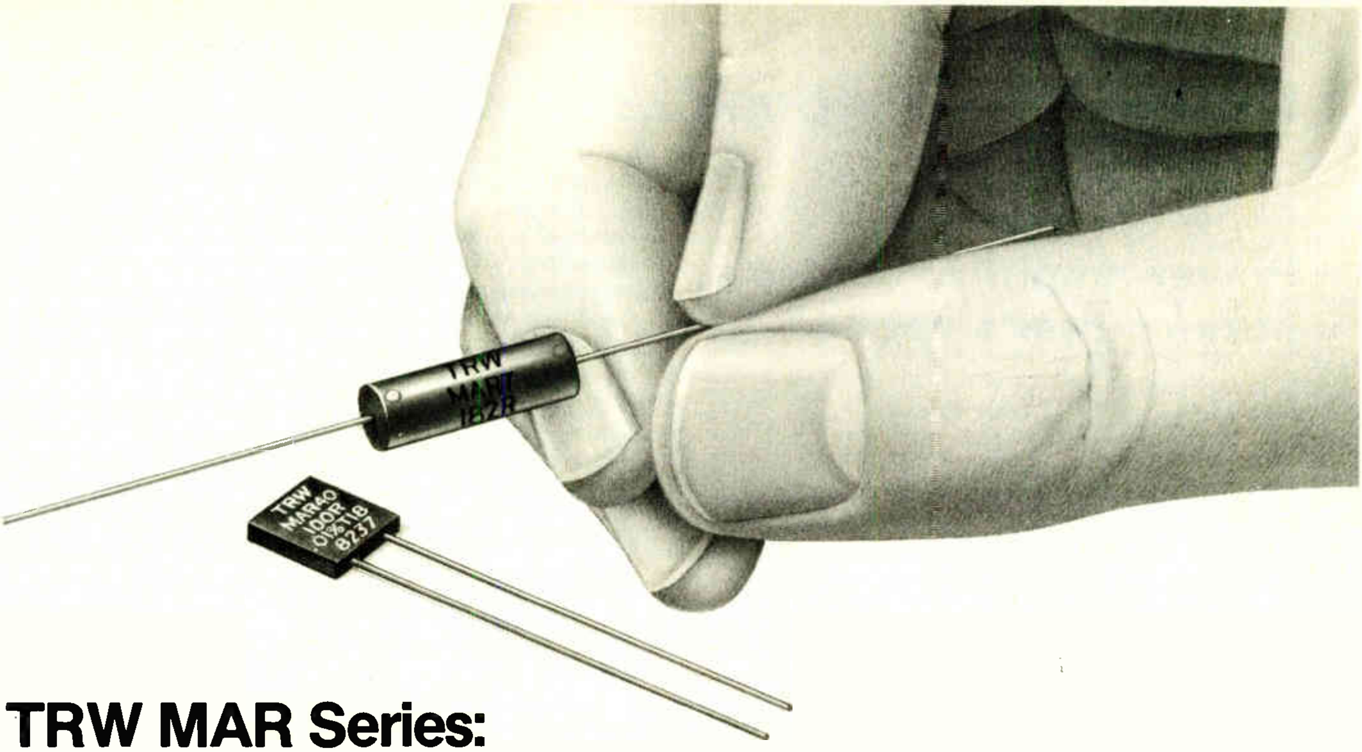
The advantage of maintaining a world-coordinate object data structure as opposed to a clipped normalized-device coordinate image is apparent in the following example. Clipping occurs when an object such as an arrow crosses the defined window. The image may then be transformed to bring it entirely into view (Fig. 2a). A system such that implements the Core proposal would retain only clipped images and after the transformation would display only the portion of the arrow that was originally within the viewing window (Fig. 2b). Because the 8100/GS retains a description of the entire arrow, the complete image can be displayed on the screen (Fig. 2c) when its perspective is altered.

Graphics-input devices

Under user control, the 8100 handles all interrupts from the input devices. Input from these devices is buffered until requested from the main system software, eliminating the need for the host to respond quickly to device interrupts. This capability is particularly useful for keyboard control: because the 8100 performs local echoing and buffering of data typed by the operator, the host will only be interrupted once per input line rather than once per character.

The display processor also controls the locator devices (trackballs, joysticks, and tablets). Position information may be read from them in device units (the position in terms of the locator), normalized device coordinates, or world coordinates. Where world-coordinate tracking is selected, the user controls the mapping between device position and the corresponding world-coordinate position. In addition to returning world-coordinate positions to the user, the 8100 may echo the locator's world-coordinate positon with a hardware cursor without imposing any burden on the host.

A high-resolution color or monochrome graphics subsystem must be flexible to provide future CAD system designers with a solid foundation. That flexibility is evident in the many unique 8100/GS features, such as the locally maintained object definition, the high-speed dual-processor architecture, and the local support for multiple interactive input devices, all supported by a large amount of local memory. □



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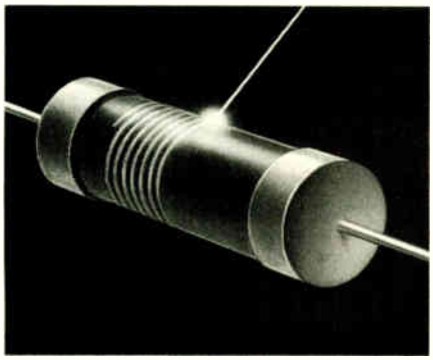

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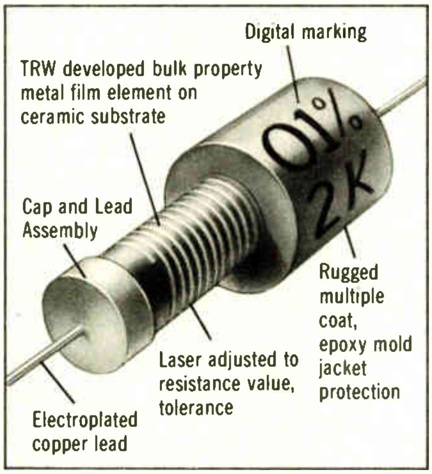

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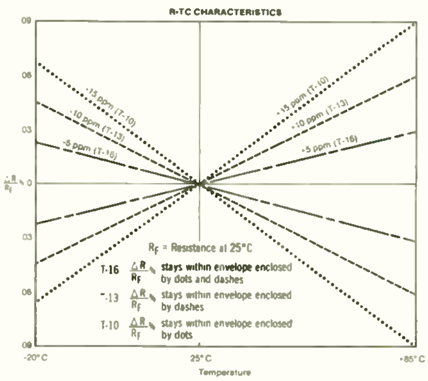

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Circle 133 on reader service card

Power amplifier controls servo motor's speed

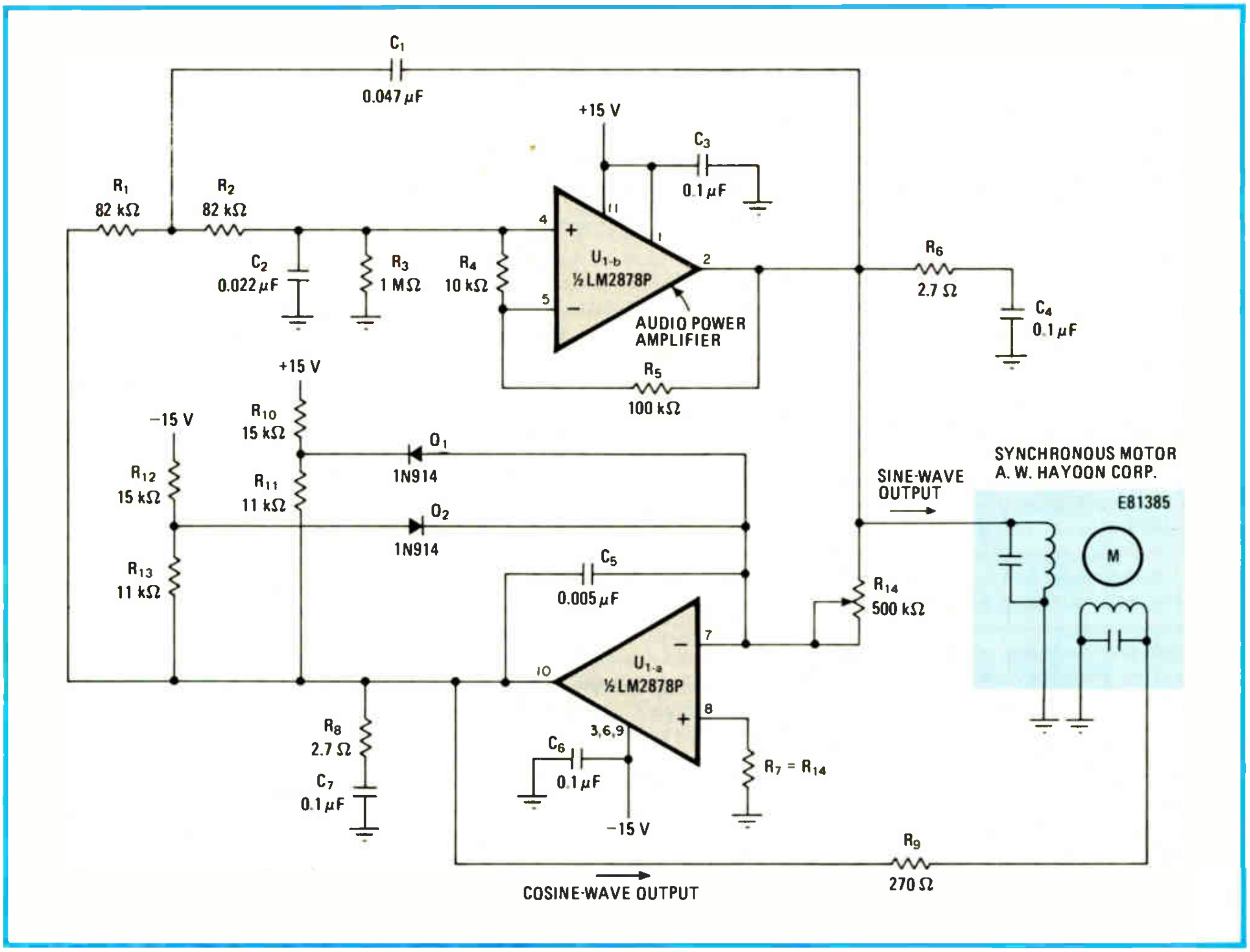
by Fred Cheng
National Semiconductor Corp., Santa Clara, Calif.

This inexpensive servo-motor drive circuit exploits the high power-output and good power-dissipation capabilities of the monolithic LM2878P audio amplifier. In addition, the on-chip thermal shut-down and current-limiting functions of the LM2878P provide the necessary protection both for a two-phase, 60-hertz motor and for the circuit.

The motor's speed is controlled through a frequency generated by National Semiconductor's 5-watt dual-amplifier chip. $U_{1\text{-a}}$ shifts the input signal's phase by 90°, while $U_{1\text{-b}}$ introduces a phase delay of –90° at its cutoff frequency. $U_{1\text{-a}}$ functions as an integrator, and $U_{1\text{-b}}$ acts as a second-order low-pass filter whose cutoff frequency is 60 Hz. When the filter's cutoff frequency is reached, the total loop phase shift is zero and the circuit keeps oscillating at the set frequency.

This oscillation frequency is $f_0 = 1/2\pi R(C_1C_2)^{1/2}$, where resistor $R = R_1 = R_2$. Capacitor C_1 is equal to twice the value of C_2 when the low-pass filter is critically damped. The proper loop gain for sustaining oscillations is obtained by adjusting potentiometer R_{14}. In addition, to reduce the offset effect of the input bias current, the value of R_7 should be near R_{14}.

Diodes D_1 and D_2 stabilize the oscillation amplitude, which is set by resistors R_{10}, R_{11}, R_{12}, and R_{13}. Networks R_6, C_4 and R_8, C_7 compensate for the amplifier output stages. To reduce noise for high-output power conditions, the values of the decoupling capacitors connected to the line must be increased. □

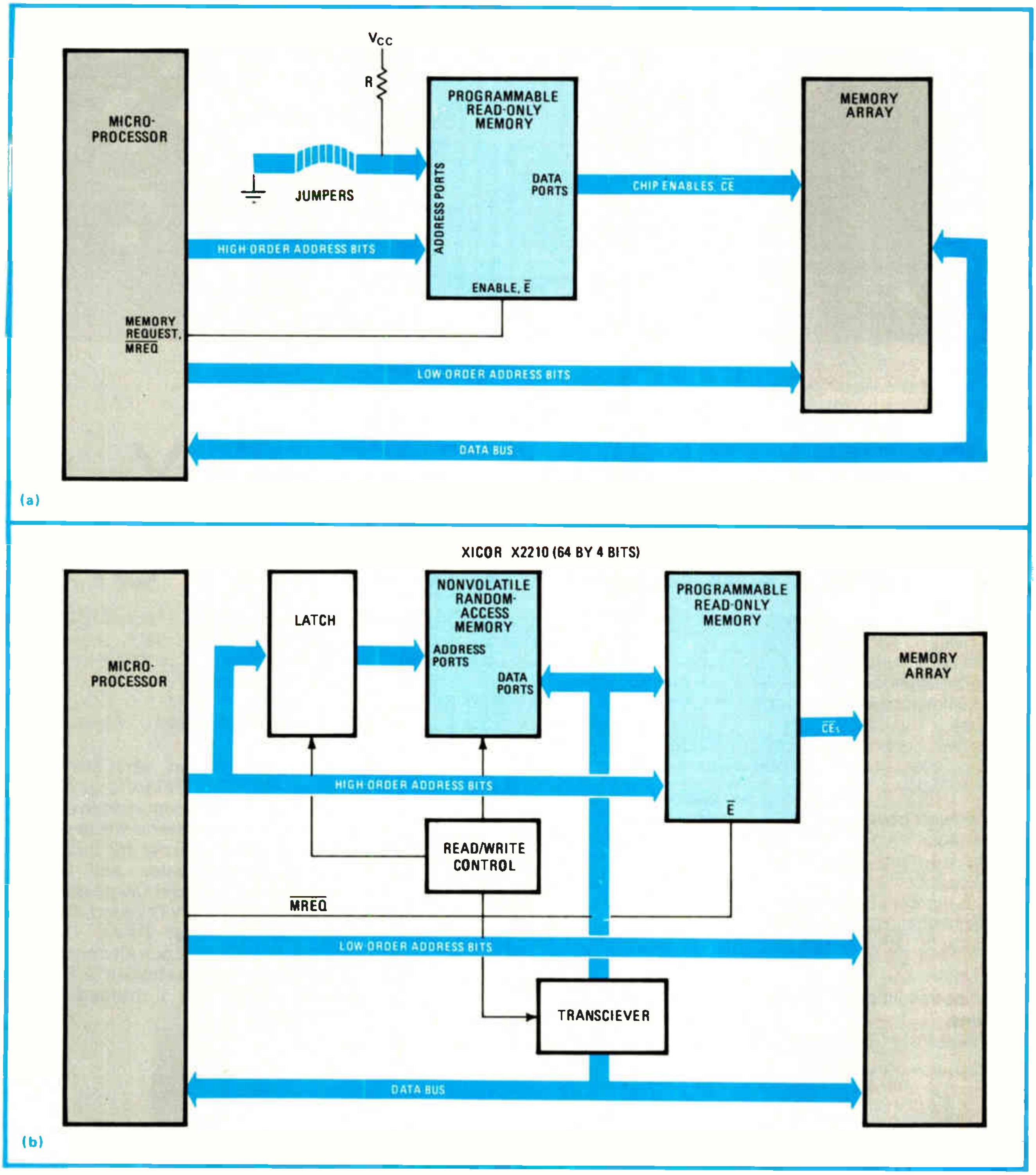


Speed control. Using National Semiconductor's dual-audio-amplifier chip LM2878P, this circuit generates an oscillation frequency to control the servo motor's speed. $U_{1\text{-a}}$ functions as an integrator that shifts the input signal by 90°, while $U_{1\text{-b}}$ serves as a second-order low-pass filter that introduces a phase delay of –90° at its cutoff frequency. Since the total phase shift at the filter's cutoff frequency is zero, oscillation is sustained.

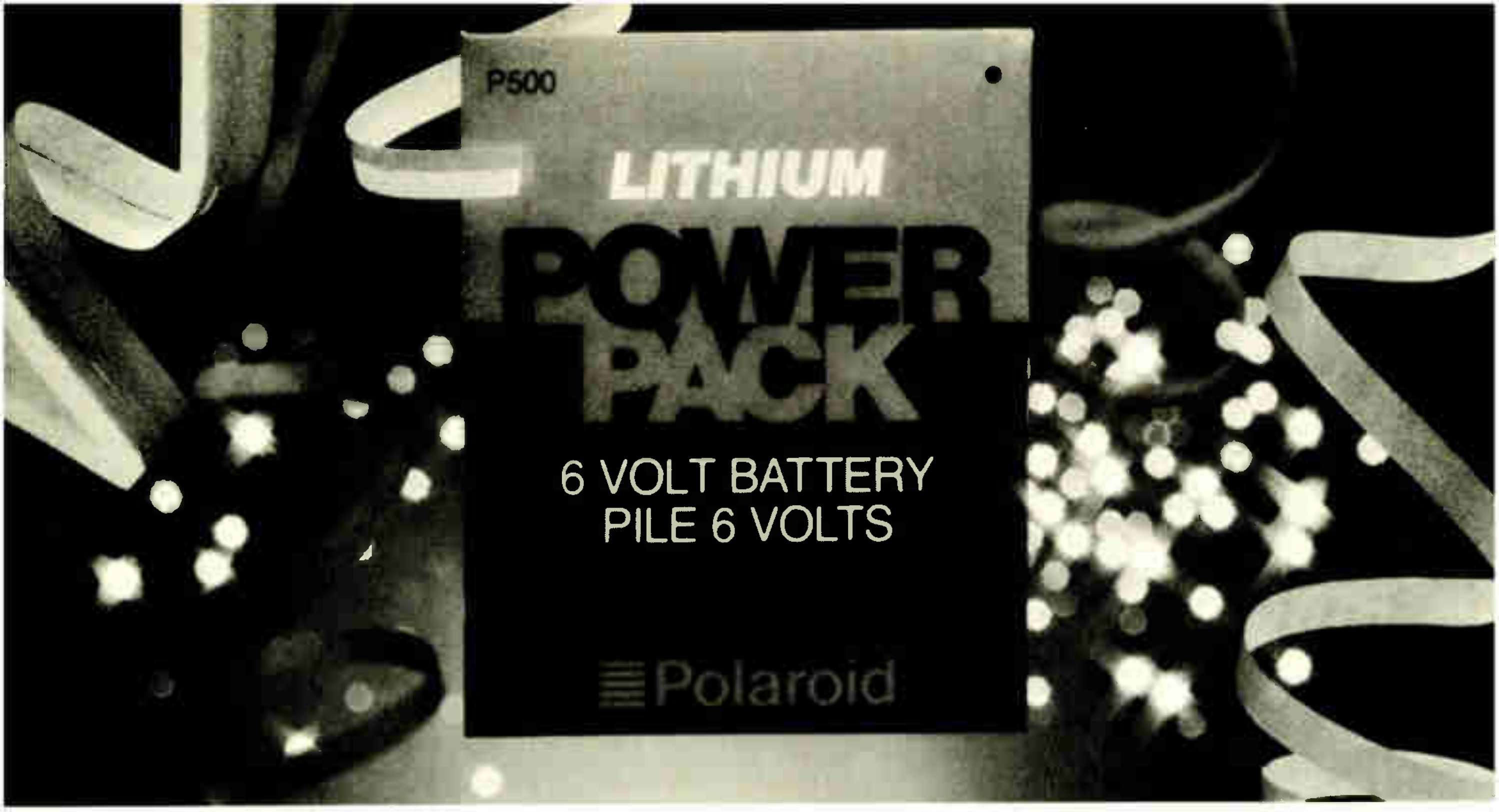
Static RAM relocates addresses in PROM

by Irving Gold
Basic Systems Corp., Santa Clara, Calif.

With programmable read-only memories steadily decreasing in price, their use is becoming a cost-effective means of interfacing a microprocessor with its memory. Unfortunately, the user must replace the PROM each time the address-decoding space needs changing. However, by using a static random-access memory, this design allows dynamic-address relocation and translation, provides remote control and diagnostic capabilities, and enables the



Relocating. Jumper wires select address location options for a system that uses a PROM to interface the microprocessor with its memory (a). When the jumpers are replaced with Xicor's 64-by-4-bit static RAM (b), dynamic address decoding under program control may be attained.



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Circle 136 on reader service card

operator to select address locations easily.

To interface a processor with its memory, a high-order address from the microprocessor is usually fed into the PROM address inputs, and the PROM data-output lines enable chips in the memory array. The data pattern corresponding to the desired address space is then preprogrammed into the PROM that decodes the address. However, the PROM must be replaced whenever the address space has to be changed.

A better method is to preprogram the PROM with various address options and to use jumper wires to select the desired address location (a). But this solution is incomplete because the system must still be shut down to remove the board and latch up the right jumpers.

The shortcomings of earlier designs may be overcome by replacing the jumpers with a 64-by-4-bit RAM like the Xicor X2210 (b). This substitution allows the user to load the static RAM directly with a data pattern corresponding to the desired address space. As newer high-speed static RAMs are introduced, it may prove possible for just one of them to replace this latch, static RAM, and PROM combination. □

Lf dual-staircase generator has adjustable phase

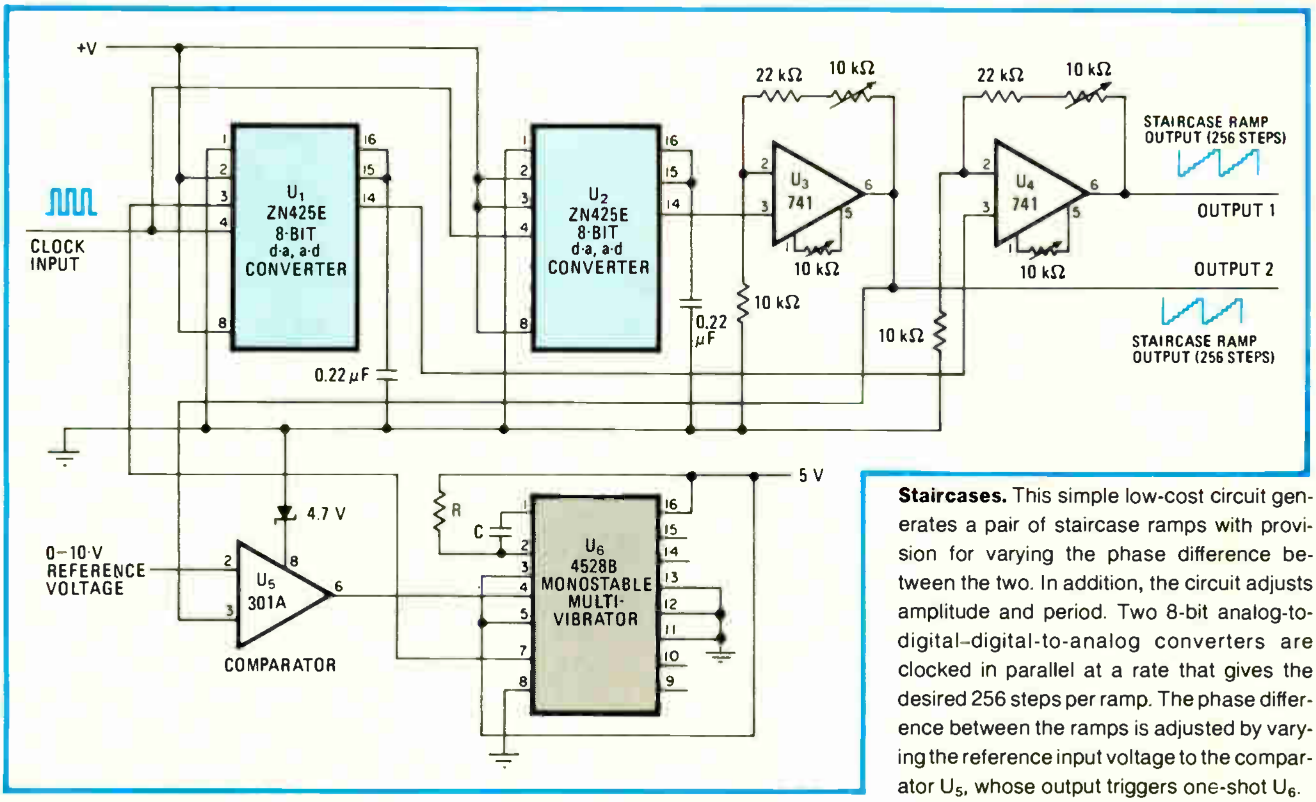
by Christopher J. Garland and T. George Barnett
London Hospital Medical College, London, England

Many biomedical experiments, like investigations of skin temperature variations, need ramps having varying amplitudes and periods. This low-frequency ramp generator provides two 0-to-10-volt staircase ramps whose phase relationship may be varied as required by changing the 0-to-10-V input reference voltage. In addition, the periods of the ramps may be varied from a few seconds to several hours.

Two 8-bit analog-to-digital–digital-to-analog converters U_1 and U_2 with on-chip binary counters generate the staircase ramps that are reset by pulling the counter-reset pin low. The converters are driven in parallel by the clock input at a rate that produces 256 steps per ramp output. In order to set the amplitude of each ramp between 0 and 10 V, the output from each converter is fed to variable-gain and -offset amplifiers U_3 and U_4.

U_1's counter-reset pin is driven by the high-Q output of monostable multivibrator U_6, while the reset pin of U_2 is held high to generate a repeating staircase ramp continuously. The output of comparator U_5 triggers one-shot U_6. As a result, whenever the ramp output of U_2 exceeds the comparator's reference voltage input, a reset pulse is generated by monostable multivibrator U_6. Thus varying the input reference voltage varies the phase difference between the two staircase ramps.

The pulse width of one-shot U_6, which is set by resistor R and capacitor C, must be of shorter duration than the clock input. □



Staircases. This simple low-cost circuit generates a pair of staircase ramps with provision for varying the phase difference between the two. In addition, the circuit adjusts amplitude and period. Two 8-bit analog-to-digital–digital-to-analog converters are clocked in parallel at a rate that gives the desired 256 steps per ramp. The phase difference between the ramps is adjusted by varying the reference input voltage to the comparator U_5, whose output triggers one-shot U_6.

In head-to-head comparison, there's really no comparison. Our OS4040 stacks up best.

The Gould OS4040 digital storage oscilloscope vs. the Philips PM3310 and Tektronix® 468.

The right balance between sampling speed and detail, for accurate measurement. The faster sampling rates of the Philips and Tek units don't mean much without supporting memory. The Gould OS4040 can capture and store 5,120 words on a single waveform compared with 256 for the PM3310 and 512 for the Tek 468. That means the OS4040 can expand a stored trace by 50 times horizontally and still give you 100 data points across the screen. Under the same circumstances, with Philips' 256 words you would get only 5 actual data points. Tek would give you 10 data points. For a detailed display, the OS4040 is the clear winner.

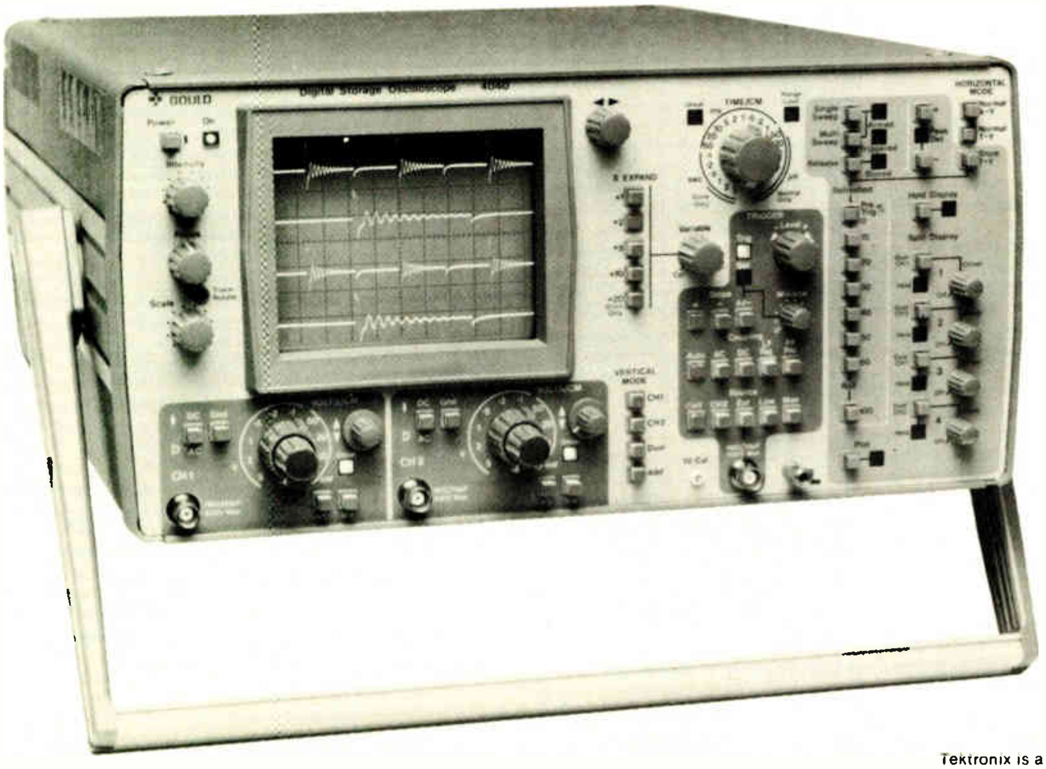
Fast capture of sequential signal events, as in digital logic circuits. The OS4040 can capture up to four signals from a single channel and hold them in separate storage for later analysis. It does this with direct store access at up to 10 MHz. While the Philips can capture the signals, it requires considerably more time between the capture of each event since it can only access its store via a 78 kHz ADC from its CCD line. Tek can only capture up to two sequential events from a single channel.

The most flexible interface facilities. Only the OS4040 can copy captured waveforms onto a chart recorder from both channels simultaneously, and is able to plot one signal against another, for example, as in hysterisis curve plotting. The PM3310 and the Tek 468 can only output one channel at a time.

The OS4040 can "baby-sit" for you. It has a "baby-sitter" mode, so each signal captured can be automatically transferred to the chart recorder, and the store re-armed for the next signal event. the PM3310 offers neither repetitive analog output nor a "baby-sitter" mode. And while the 468 provides an analog option, it is not capable of "baby-sitting."

Exclusive direct digital user port. Even though all three systems offer an IEEE output, only the OS4040 offers a direct digital user port as a standard option for situations where the IEEE is too slow for the buffer store to be cleared before the next signal capture.

The Gould OS4040 digital storage oscilloscope. For the whole story, contact Gould Inc., Instruments Division, 35129 Curtis Boulevard, Eastlake, OH 44094. Phone 800/321-3035.



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Circle 138 on reader service card

Refined closed-loop servo enhances low-cost disk drive's accuracy

For Winchester drives, four of these head-positioning techniques exist, but one stands out as the best performer at a reasonable price

by Larry Sarisky, *SyQuest Technology, Fremont, Calif.*

☐ The quest for greater track densities in Winchester disk drives has led to closed-loop servomechanisms for their superior accuracy in positioning read-write heads. However, the prize is not without its drawbacks, because closed-loop servos have been expensive.

Thus high track density at low cost was the biggest challenge facing the designers of the SyQuest SQ-306, a 3.9-inch removable-cartridge and fixed-disk Winchester drive [*Electronics,* June 2, 1982, p. 183]. They evaluated three existing types of closed-loop units—the dedicated servo, the embedded servo, and a scheme whereby only the outside and innermost tracks are servo tracks. Dissatisfied with these options, they developed a new type of embedded servo, called Digilok, which combines reasonable cost with high positioning accuracy.

Dedicated tracks

In drives using very accurate and fast head positioners, one complete disk surface is often used for defining the track positions for what is called a dedicated closed-loop servo system. The track positions are written on the servo disk at the factory, and a read-only head is mechanically tied in tandem to all the read-write heads for the data surfaces. The tracks on the servo system's disk define the tracks on all the data surfaces. As the servo head reads the reference tracks, it constantly sends error signals to the head-positioning electronics that control the voice-coil actuator. Any mispositioning of the read-write heads over the center of the track is instantly corrected.

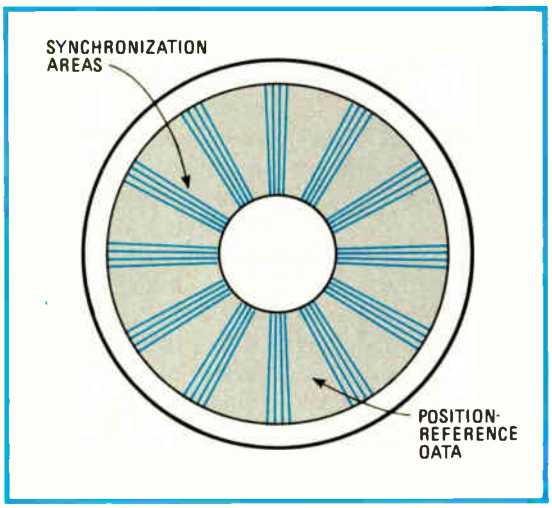
The major disadvantage of the dedicated servo is its high cost. A complete set of read heads and an entire disk surface is needed solely for positioning the data heads. Also, the electronics for controlling head positioning are expensive.

Nor would this method work well with removable disks. To achieve interchangeability, one side of each removable platter would be needed for the dedicated servo system, and the cost of such cartridges would be quite high.

However, dedicated servo surfaces are a must on high-performance, nonremovable, multiple-platter drives. The servomechanism is a continuous closed loop where the track position is constantly being monitored and head drifts off the center of the track are immediately corrected. Consequently, tracks can be spaced very close together on the platter.

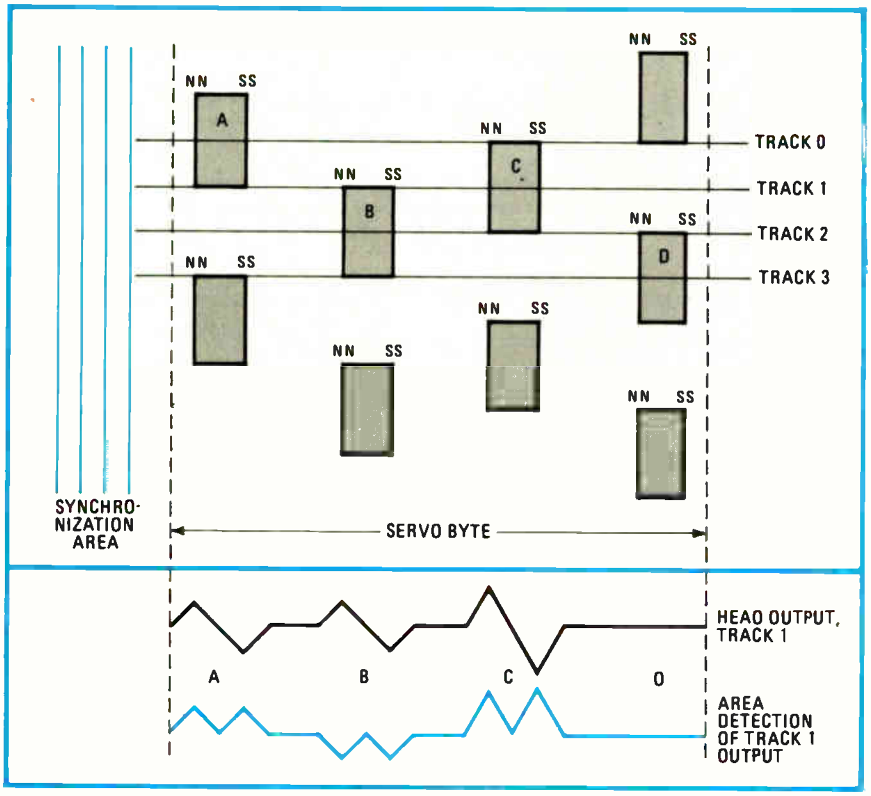
Also, moving the head from one track to another—the seek operation—is done quickly and accurately. For example, on the high-performance IBM 3380 and comparable drives, the average seek or access time is only 18 milliseconds—the same time a high-performance, open-loop, stepper-motor positioner takes to move from one track to an adjacent one.

The head positioner performs the seek operation by counting the track crossings—the information on the servo tracks is used only for keeping all read-write heads centered over the data tracks. This postion-reference information is written as a series of bytes around the circumference of each track. Each servo byte begins with a sychronizing area that runs from the edge of the disk toward the center in a straight line across all tracks (Fig. 1). This synchronizing area consists of several solid magnetic strips, each like a bar magnet with its south pole adjacent to the south pole of the neighboring strip.



1. Starburst. In a dedicated closed-loop servo system, one complete disk surface has servo information written on it at the factory. The usual format for this information is regularly spaced synchronization areas, permenant magnetic strips radiating from the disk center, that separate the track servo data areas and identify the first servo byte.

When the servo read head picks up this regular magnetic pattern, the associated circuitry knows that the positioner has reached the beginning of a servo byte. Within the servo byte, position signals, called double bits, are recorded. The type of dedicated servo system shown in Fig. 2 is called a quadrature system and has a series of four double bits—one on each side



2. Quad. A quadrature servo data scheme uses four double bits in each servo byte to give the servomechanism the information needed to keep the head centered over the track. Area detection of the head output produces the signal (color) used to center the head quickly.

of the track, one straddling the track evenly, and the fourth not touching it at all. Each double bit is centered over one track, with its ends at the edges of the two adjacent tracks. This pattern, characteristic of a quadrature servo system, is replicated several times within one servo byte.

If the head is centered over track 1 when it passes beside double bit A, it detects a peak in one direction followed by a peak in the other direction as it passes from the north to the south pole of the double bit—see the head-output signal line at the bottom of Fig. 2. Likewise, a similar signal is detected as the head passes double bit B. However as it moves through C, it produces two peaks at maximum height. The head gets no signal from double bit D during normal operation.

Comparing voltages

Circuitry converts these head outputs to alternating positive and negative dc voltages (shown as the area detection line in Fig. 2) with magnitudes corresponding to the areas under the two halves of the output waveforms. By comparing the voltages, the positioner can send command signals to the actuator motor to relocate the head over the track. For example, a larger voltage from A indicates that the head is drifting toward track 0, while a larger voltage from B points to a drift in the opposite direction.

A quadrature servo system performs well in the seek mode, as well as in maintaining position over a track. In the seek mode, a velocity loop and a forcing function are substituted for the feedback signal applied to the actuator motor in the position mode. The effect of the forcing function is to introduce an error signal in the closed-loop servo which, in turn, causes the actuator motor to move to reduce the error.

A tachometer counts the number of track crossings. Once the desired number is reached, it initiates a turn-off of the forcing function, and the positioner returns to the position mode to center the head over the new track and to keep it there.

In the second major closed-loop servo-positioning method, servo information is embedded between sectors on each data track. The chief difference between an embedded servo and a dedicated servo is that the servo information from the former is available only intermittently, rather than continuously. Embedded servo systems typically achieve a lower track density than dedicated servos. Also, head positioning speed and accuracy are less with embedded servo schemes because of head-switching and settling-time delays.

With the servo information available only once per disk rotation, the positioning information is in a different format than with dedicated units. Similarly, the intermittent availability of the information requires a different method of track identification.

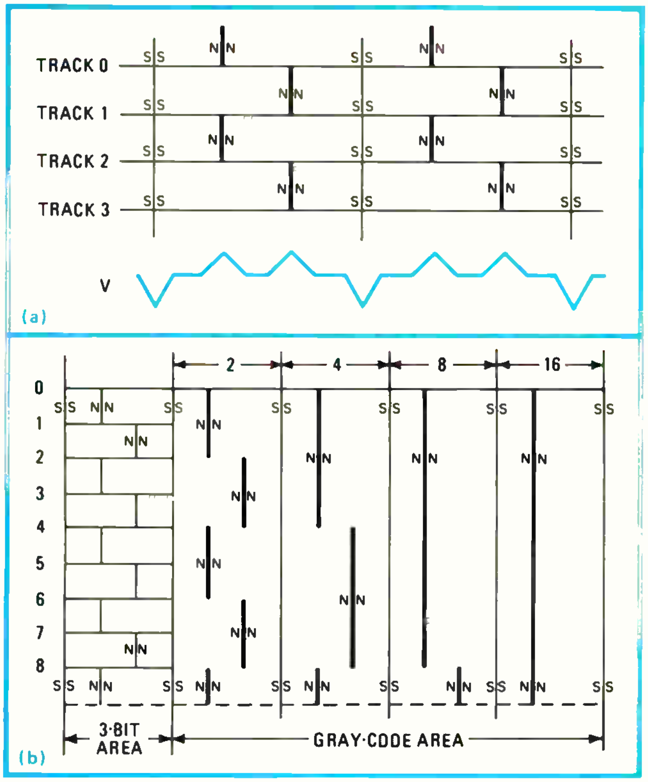
Track-position information is contained in a series of three magnetic reversals called triple bits (Fig. 3a). A solid magnetic strip from the disk edge to the center begins each triple-bit series. Line V shows the head output voltage as a read-write head passes along track 1.

Voltage signals

For example, track 1 first crosses the two south poles of the solid strip and then crosses two more magnetic transitions before the next solid strip. The read-write head coming up on the start of this triple-bit series detects the two adjacent south poles and produces a negative peak voltage. As it passes the next two sets of adjacent north poles, it produces two positive voltage peaks. Equal amplitudes of both positive peaks indicate an on-track condition for the head.

In a dedicated system with a whole surface devoted to servo information, the servomechanism always knows what track it is on without needing a encoded track number. It simply counts track crossings as it moves the head across the platter.

With an embedded servo, however, it would not be accurate enough to count track crossings. During a seek, the read-write head will not always be over the embedded information when crossing the tracks. In fact, the head most probably will be over a data sector when it crosses a track and, therefore, will not be able to count that track.



3. Triple bits. For embedded servo, track-positioning information consists of a series of three magnetic reversals—for example, track 1 crosses the solid SS strip then two NN magnetic reversals—produce a negative and two positive voltage peaks (a). An immediately following information field (b) contains the encoded track number.

Thus, to ensure that the servo knows where it is at all times, track-identification information follows a series of triple-bit triplets (Fig. 3b). This information is in Gray code, in which successive numbers differ only by a single bit in order to reduce errors. The first set of magnetic transitions under heading 2 is twice the length of the transitions in the triple-bit series. Likewise, the transitions under heading 4 are four times the length; under heading 8, eight times as long; and under heading 16, sixteen times. With this encoding, the servo system can tell over which of 32 tracks the head is positioned.

Once the read-write head is over a track, it can read along the Gray-coded portion of the servo information to find out which track it is. Track 1, for example, will produce 10101010, reading from left to right. Similarly, for track 2, the code is 11101010, and so on.

One limitation of embedded servos is their incompatibility with high-performance, fast-access drives. The relatively maximum speed of the seek operation, which depends on how frequently the servo information can be read, on the intermittent availability of the positioning information, and on the rotation speed of the disk, can frustrate fast accesss.

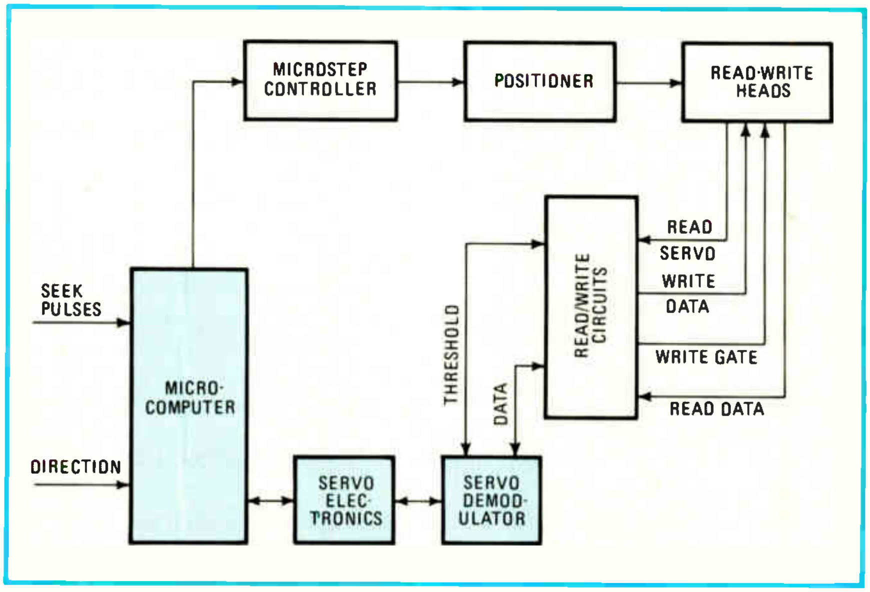
The embedded servo works well in removable-cartridge drives. It supports interchangeability of cartridges among drives, as a dedicated servo would, but it does not require dedicating an entire surface of each cartridge to positioning information, as do dedicated servos. Because interchangeability is the major hurdle for cartridge drives, some type of high-accuracy closed-loop servo is needed to ensure that tracks recorded on one drive can be read on another.

Unfortunately, the hardware is relatively expensive. Cartridges with embedded servos still cost about $100 for 8-in. disks and only slightly less for 5.25-in. disks.

Inside, outside

A low-cost solution for the problem of an affordable closed-loop servomechanism is to write one dedicated servo track as the inside track and another at the outside ring. Called ID-OD for inside diameter-outside diameter, this method is especially appealing for the low-cost 5.25-in. Winchester drives. These two servo tracks contain a conventional positioning scheme like dedicated servos do. However, the track-id scheme is different from those used in the other closed-loop servos.

For positioning, the drive first reads the outside servo track and then makes fine adjustments to position the headover the track center. For this low-cost drive, a

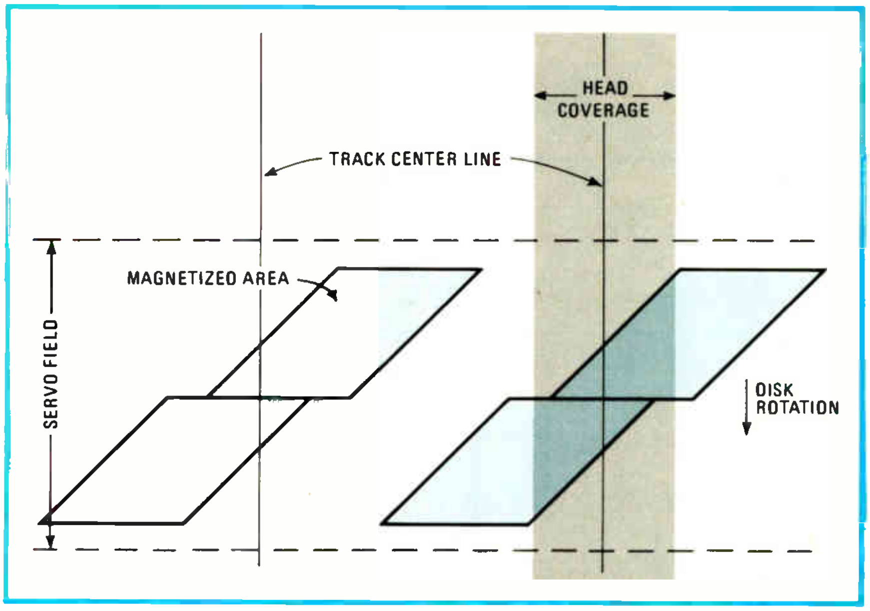


4. Best bet. The low-cost Digilok servo technique sports the advantages, and eliminates most of the problems, of embedded and inside-outside servos. The servo demodulator, servo electronics, and a microcomputer do all the analysis and computation for track-centering corrections.

stepper motor is used for head positioning. Then the positioner moves to the inside servo track, counting the step pulses as it goes. At the inside servo track, the positioner then fine-positions over the center of that track. While doing the fine positioning over each servo track, the positioning mechanism notes the amount of correction needed to find the track centers.

With knowledge of the number of step pulses between the outside and inside and the amount of fine-step correction required at each servo track, the positioner can calibrate its position to a new cartridge.

The major benefit of this method is that it is cheaper to write the two servo tracks than it is to produce a disk with embedded servo information in every track. Another benefit is the absence of a fixed sector size on the data tracks. Fewer electronic parts are required than for embedded servos, but it still costs more than a drive with no positioning scheme.



5. Critical pattern. The pattern of the magnetized areas in the servo field of the Digilok servo system determines the signal patterns used by the servo electronics and microcomputer to position the heads correctly. When centered, the head sees is a symmetrical pattern; when it is off-center, it sees an asymmetrical pattern.

The main problem, however, is that each time a positioning failure occurs, the drive has to repeat the calibration process. If this happens frequently, much time is lost and the drive's performance degrades. There is also no guarantee that once the head is on a data track, it will stay in place, for there is no mechanism for making the necessary readjustments.

The third man

Having eliminated the dedicated-servo approach on the grounds of its cost, SyQuest designers moved to eliminate the problems of both embedded servos and the ID-OD scheme and retain the advantages of both by developing the Digilok technique. Instead of locating the servo information between fixed-length sectors, this variant on the embedded method writes it once on each track as part of the track index mark, which indicates the beginning of each track. Also, it uses an accurate stepper motor, rather than a voice-coil actuator, as the head positioner.

Like the original embedded servo, Digilok provides feedback information during the reading and writing of data, except it is available only once every revolution. This method also allows a flexible data-sector size like the ID-OD scheme. Moreover, it eliminates the calibration cycle that slows down the ID-OD servo, although it does have a longer read time for the servo information than does the original embedded servo.

The only additions to the usual read-write circuits of the drive are a very simple, low-cost demodulator and the servo electronics (Fig. 4). The circuits for these functions are all digital. The demodulator's simplicity results from the nature of the servo data.

Magnetic positioning data in the Digilok method is written on the disks in the index mark of each track (Fig. 5). The amplitude of the signal read from the magnetized areas of the positioning field is demodulated and is fed as a series of pulses to an up-and-down counter in the microcomputer. When the head is flying exactly over the center of the track, it will move across the servo data with the head gap within the dotted lines.

As the head approaches the servo data, the signal increases for the up-count bytes. The down-count bytes start at a maximum, then decrease to a minimum. The demodulator starts looking for positioning information after it detects the index mark. The reading of the index mark triggers the reset for the servo electronics.

The up-and-down counter counts up from the detected up bytes in the servo data and then counts down with the down bytes. The microcomputer compares the resulting count. If the up and down counts are equal, the head is centered; otherwise the microcomputer directs the head positioner to correct the positioning. The head can be moved in increments of 1/30th of a step for a positioning resolution of 76 microinches.

Moving corrections

The servo does a position correction as soon as it reads the servo byte. At the next revolution, it again checks the position of the head relative to the track center, averages the new error, if any, with the previous error and makes another positioning correction if required, using the average of the two errors. The moving average continues over all revolutions.

The Digilok servo technique is much more accurate than the ID-OD method. Though it is a little less accurate than an embedded servo, it costs less than both embedded and ID-OD servos. Contained in a single low-cost complementary-MOS chip, it provides variably-sized sectors. Digilok positioning allows a density as high as 435 tracks/in. and is eminently suited to removable disks that may have to be played on more than one drive. □

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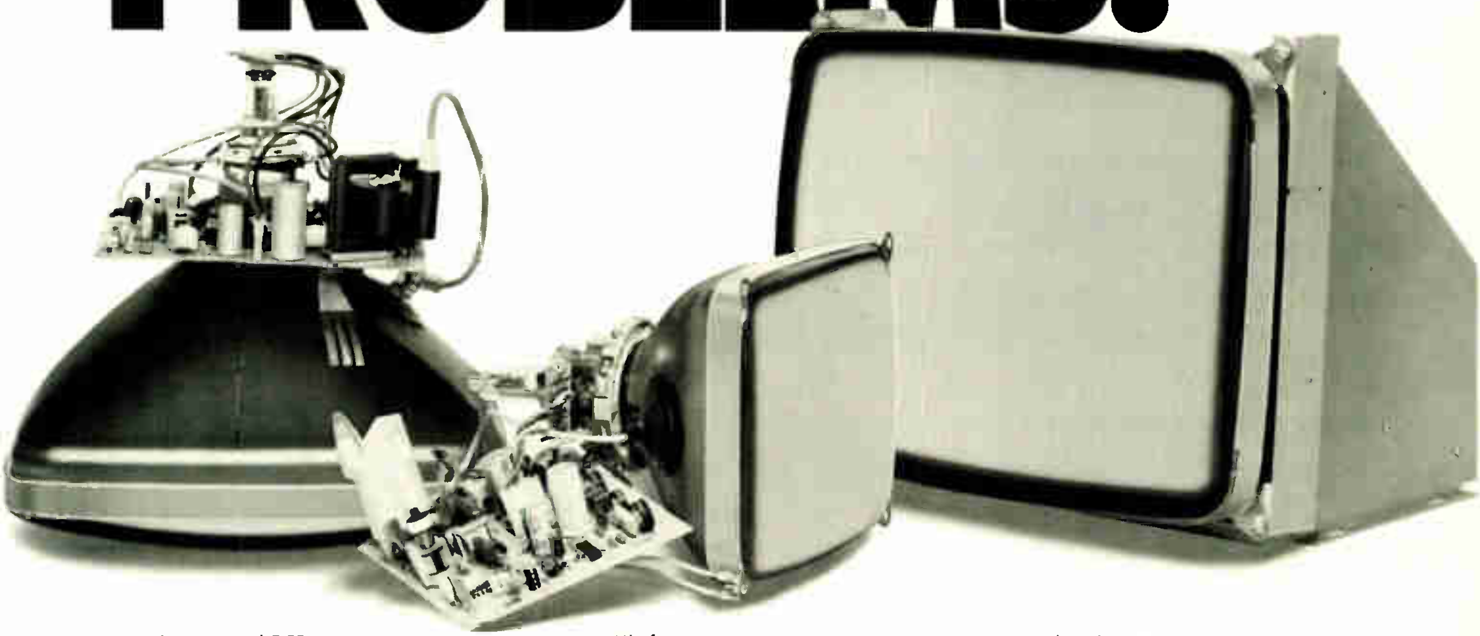

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Analog modeling simulates the faults of electromechanical components

Simulation software verifies maintenance analysis package; terminal can display results graphically

by H. D. Jackson, *International Business Machines Corp., General Technology Division, Endicott, N. Y.*

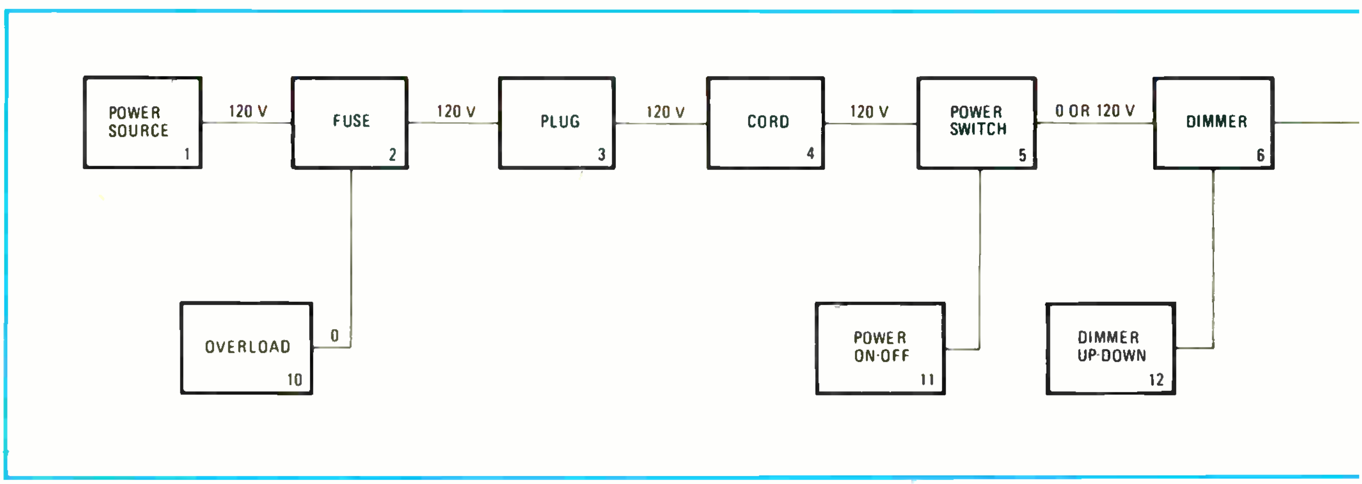
□ "Physician, heal thyself" has long been the credo of large computers that contain sophisticated quick-fix packages and use extensive bugging and debugging procedures to determine their effectiveness. But the same is not true for mechanical devices—like printers—that are connected to small computers. Simulating the faults of such devices with software is difficult because they cannot pretend to malfunction as easily as can electronic circuitry. Without doing permanent harm to the equipment, it just is not possible to break a belt in a random manner, cause a gear to wear, or make a printer hammer fire sluggishly.

However, by creating a model of an electromechanical device and inserting random or intermittent faults into it, a designer can both run and check out the accuracy of a maintenance program that detects mechanical errors. Models with simulated faults are exercised and the results are applied against the maintenance package. Repair and adjustment procedures are also run to ensure that this part of the package is effective.

In general, troubleshooting programs for peripherals linked to small computers have not been keeping pace with the expanding market and technology of such systems—they do not allow the user to determine the cause of failure and make his own repairs. For small computers, which are constantly updating their large-scale-integrated circuitry, a problem of program verification faces designers, and manufacturers are using extensive testing procedures to ensure the accuracy of their software packages. Errors or failures are usually placed on a peripheral, and its associated computer then runs the maintenance package. However, if computers that employ ineffective packages that do not find a failing component or isolate the wrong one, their terminals will ultimately require field service by the manufacturer. On the other hand, a fault-simulation model should both help designers debug machines and release valuable prototype equipment for other uses.

Developing models

Before such a model is developed, the simulated equipment must be reduced into a set of individual functions. In addition, a list of models describing each part is gathered. Thus an analog diagram is obtained for each part and becomes the base of a software model. This model has three main parts: input, status, and output. The input portion obtains control information from an external source. The status portion of the model examines each block as described by the analog diagram. Each block's status is obtained by examining the state of previous blocks and using available fault information from the external control source. Finally, the output section consists of routines that display the simulation results—in either a prose or graphic-display or animated format.



In addition to a software model, two tables—status and fault—are needed to describe the machine. The status table contains the current state of each block used in the model, and the fault table describes how each block will react in an error situation.

The model is then run and is controlled by the keyboard. Results are displayed, as requested, and the status table is updated by both the model's reactions to stimuli and the contents of the fault table.

Fault simulation

The software model is loaded into storage, and the status and fault tables are set at a known starting state. In addition, the execution sequence for the blocks is initiated, and each block's status is calculated from that of previous blocks. The output may be analog—voltage levels or mechanical positions may be represented. The fault table is then examined to determine if the block's status should be stored as calculated or whether a failure may have occurred.

Information is stored in the fault table in terms of block-failure probability. Thus a solid failure would have the probability set at 100%, and an entry of 0% indicates a block with no failures. Each time a block is calculated, a number between 0 and 100 is generated. If that number is less than what is contained in the fault table for that block, the figure in the table is retained; a larger number, however, replaces the figure in the table. This procedure may be varied to allow for more than one type of fault per block.

When the status of the block has been determined, it is stored in the status table and the next block is processed. When all blocks have been calculated, the output model is activated and data may then be displayed. Visual information relayed by devices like light-emitting diodes on the model should be displayed automatically. Other information may be displayed upon request.

Once the requested output data has been updated and displayed, external data may be obtained from a dynamic interrupt. The data may be entered by pressing keys on the host keyboard. If this capability is not present or difficult to implement, the model may be told to cycle N number of times, after which the keyboard is unlocked for external data. These methods can gather fault, repair, and display data. As the data is gathered, all required tables or output models are updated and the simulation process repeats until another request is made for external information.

Repairing failures

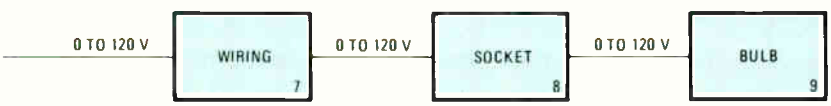
All of this information is useless, however, if the program does not repair a problem after it has been isolated and ensure that the repair corrects the error. But by adding a list of field-replaceable units to the model, a user may check the repair. The list catalogs the devices that can be physically replaced and the analog blocks that correspond to each unit. When a repair is needed, the unit number is fetched from the external data, and the fault tables for the associated blocks are set to zero. The model is then exercised to determine if the machine is operating properly.

The best way to illustrate the modeling process is through a simple example like a lamp that is controlled with a dimmer (Fig. 1). Each block in the diagram corresponds to both a lamp component and a table index number, which is needed in the model code. Blocks 11 and 12 may be manipulated from the host keyboard to turn the lamp on or off and adjust the dimmer, respectively. Block 10 turns on automatically whenever a short occurs. This block may also be set externally to represent an overload on the line. When it turns on, the fuse will open, so to speak.

Analog diagram

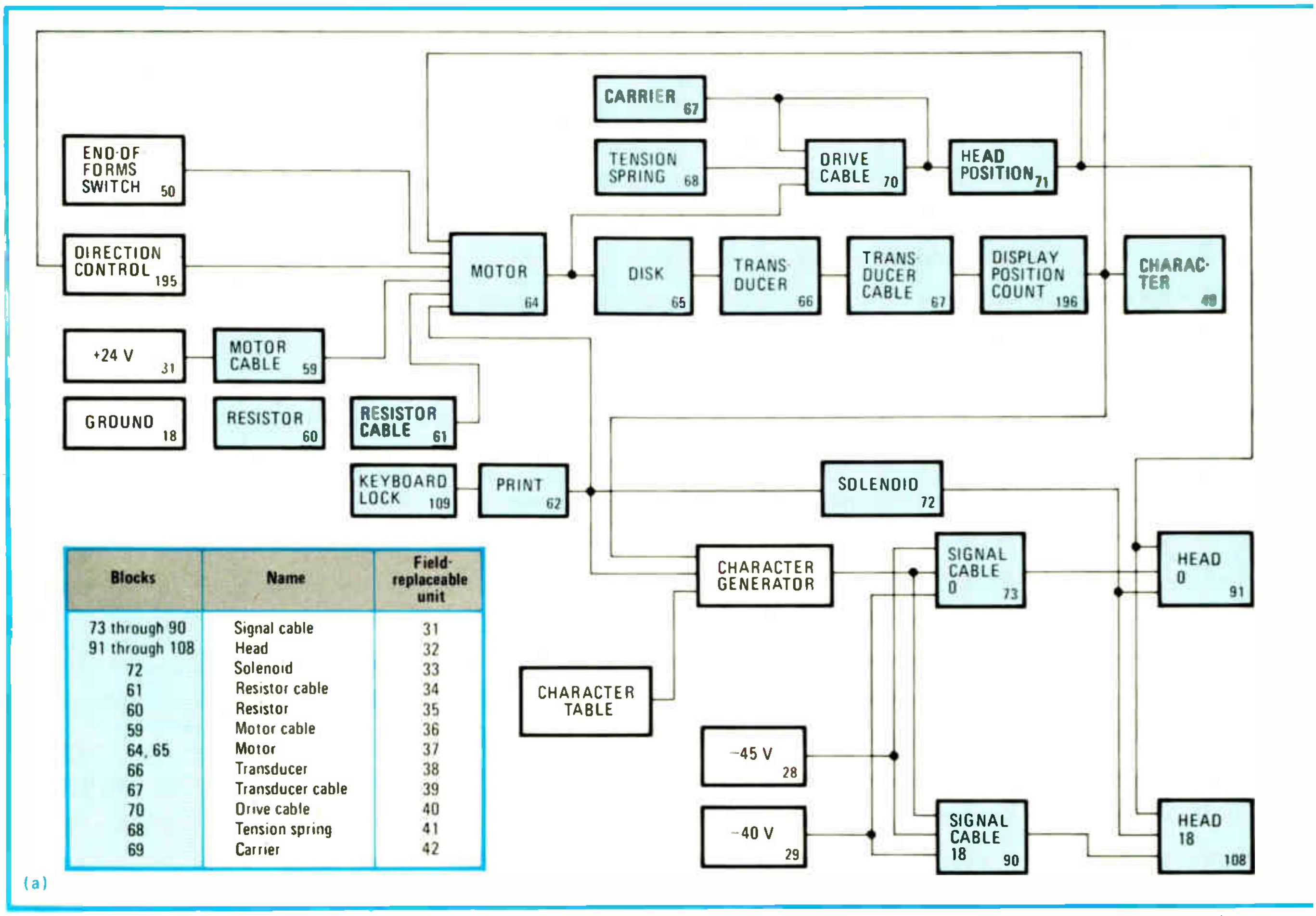
An analog diagram and a field-replaceable–unit list are used in the software model, which consists of routines that set up an example, calculate analog-block status, determine faults, display results, and obtain external information. A program for the model (Fig. 1) may be easily written in a popular language like APL, Basic, or Pascal.

Although the block-calculation portion of the model is rather important, the output section cannot be overlooked: it is used by the operator to describe results. A simulation is of little use if its values are displayed in an ambiguous manner. The type of output is highly depen-



Blocks	Name	Field-replaceable unit
2	Fuse	1
3, 4	Power cord	2
5, 6, 8	Socket assembly	3
7	Wiring	4
9	Bulb	5

1. Lamp analog. Analog diagrams help generate software models of electromechanical devices. A simple electric lamp containing a dimmer is shown in the above diagram. This analog drawing blends both mechanical and electrical characteristics into one model.



Blocks	Name	Field-replaceable unit
73 through 90	Signal cable	31
91 through 108	Head	32
72	Solenoid	33
61	Resistor cable	34
60	Resistor	35
59	Motor cable	36
64, 65	Motor	37
66	Transducer	38
67	Transducer cable	39
70	Drive cable	40
68	Tension spring	41
69	Carrier	42

2. Print and move. Diagrams (a) and (b) are the analog representations of the print head and paper movement of a matrix printer, respectively. When combined with power and indicator analog representations, a simulation allows the model to be checked against a variety of faults that could not easily be inserted in the actual printer.

dent upon the capabilities of the output peripherals. Most of the systems have, as a minimum, a video-display terminal that is adequate for mechanical simulation. Thus, at least an alphanumeric and low-resolution graphic output may be presented.

However, if the terminal has a high-resolution graphics capability, high-resolution animation may enhance the visual effectiveness of the model. Color capabilities will also enhance the output function. For example, the lamp or bulb in the lamp model could be drawn on the screen with the power switch and dimmer control. Thus, instead of just printing the bulb's status, the terminal may change its color as the dimmer is adjusted.

On the *fritz*

But a simple lamp and bulb setup does not represent the kind of failure most users encounter. A more appropriate example is an electroerosion matrix terminal printer with bidirectional printing capability. The printer may be broken down into four sections that are diagrammed and modeled independently. The separate models are then integrated and the output and external portions are added.

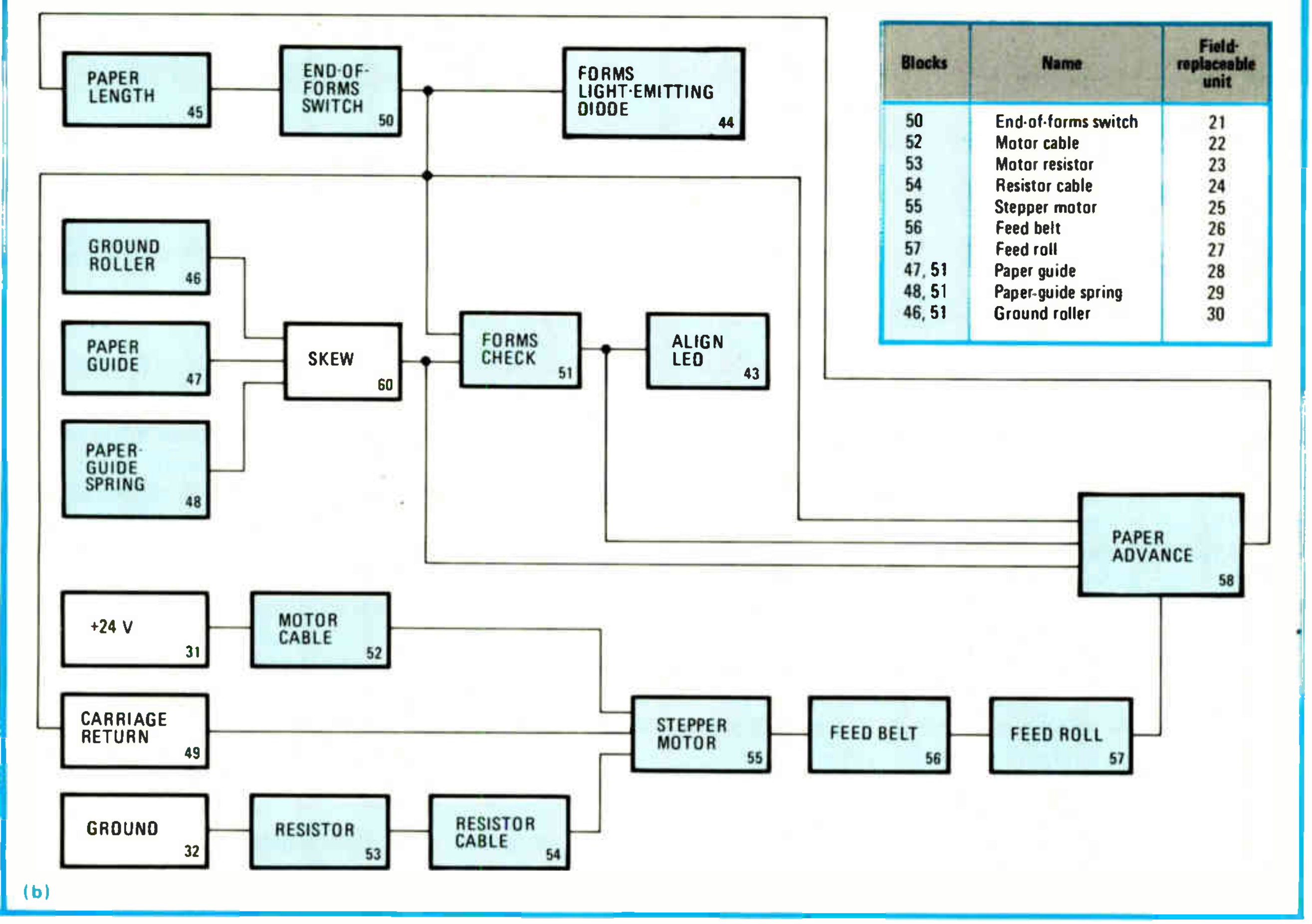
The first part of the printer is power and cooling. This portion includes distribution cables and thermal checkers in addition to voltage control and overload protection. The second part represents the indicator LEDs that may be seen by the operator. Paper movement along with printer-head functions (Fig. 2) controlling both the head's bidirectional capabilities and the wire activation mechanism, which forms a dot matrix of characters, round out the quartet.

The model includes external routines that turn the power on, insert paper to prevent an end-of-form condition, make line-print requests, create fault conditions, and monitor functions.

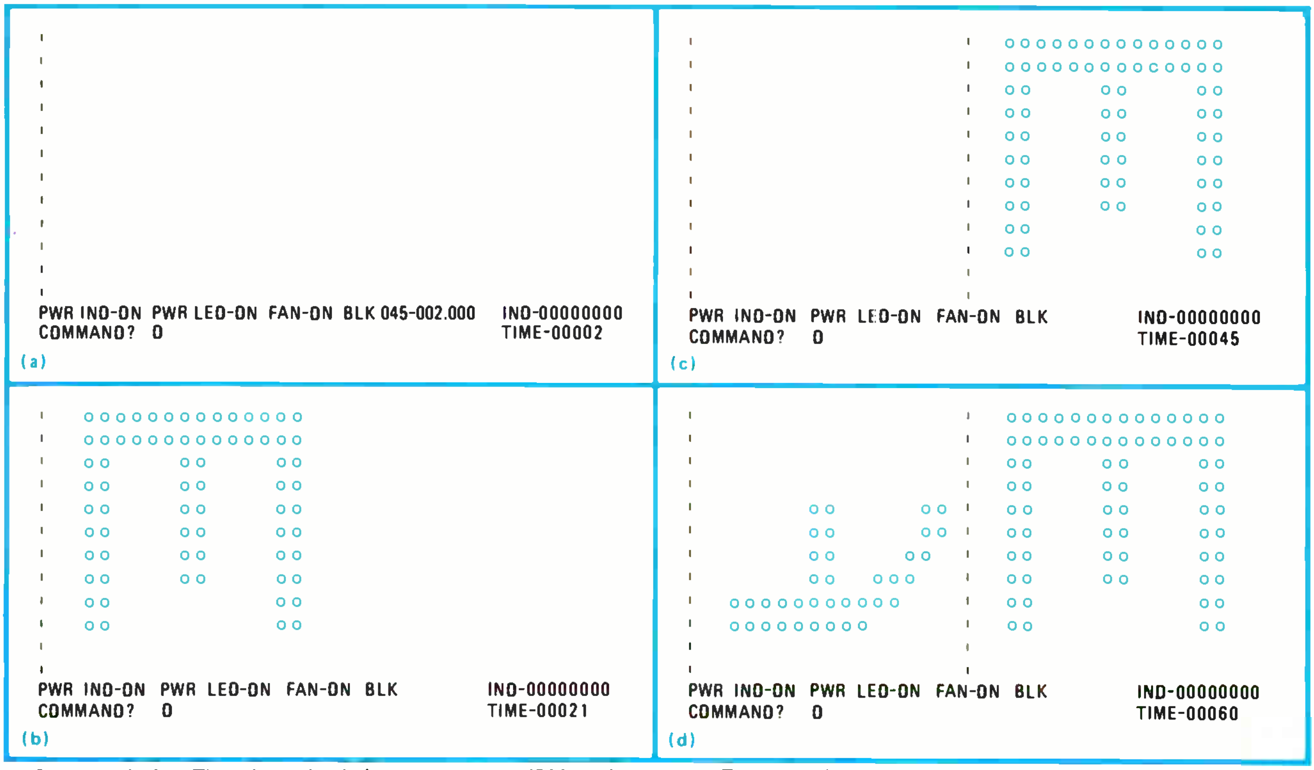
When a line-print request is received from an external routine, the print head will move from one side to the other generating a character on the output screen. Once a line is printed, head motion will cease and the paper-advance section of the model is activated. Another line-print request will cause the head to move in the opposite direction to print a character.

Overloads can be placed on the model to cause internal fuses to fail. Also, passive mechanical features such as a paper guide, a head-tension spring, and a head carrier are included. Improper adjustment of these features can cause skewing of the paper or faulty character formation.

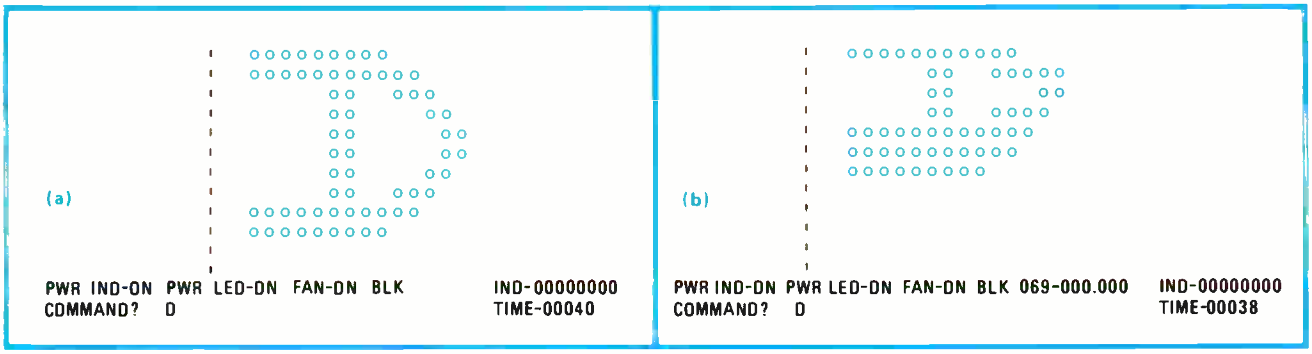
The printer simulation model was implemented on an



Blocks	Name	Field-replaceable unit
50	End-of-forms switch	21
52	Motor cable	22
53	Motor resistor	23
54	Resistor cable	24
55	Stepper motor	25
56	Feed belt	26
57	Feed roll	27
47, 51	Paper guide	28
48, 51	Paper-guide spring	29
46, 51	Ground roller	30

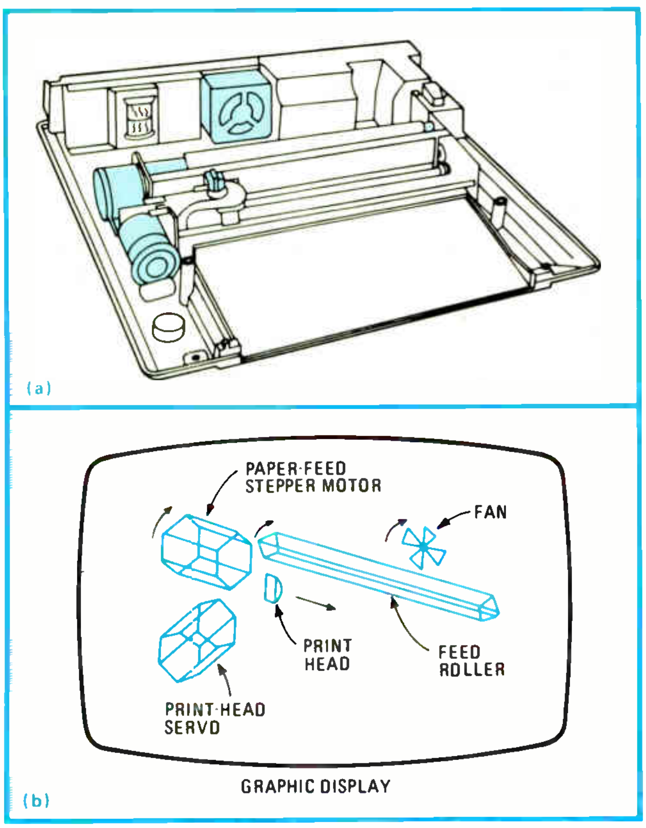


3. Screen printing. The printer simulation was run on an IBM 5110 computer. Frame (a) simulates a printer with no input, and frame (b) displays the letter E. Paper advance is illustrated in (c), while (d) shows the model in the midst of printing the character A.



4. Faulty characters. Faults may be introduced into the modeled printer and displayed. View (a) shows a normal printing of the letter A. The distortion in (b), causing the character to squeeze, is the result of a head-carrier fault that binds the print head.

IBM 5110 computer using Basic. Basic was selected so that the model could be easily copied. Figure 3 represents a sequence of frames from the computer's video terminal of a machine with a good output and combines low-resolution graphics with words to describe the simulation. Figure 3a shows the output after power has been turned on and paper has been loaded into the machine. The line of dots on the left represents the paper position or perforations. Because of screen limitations, the letter's 12-by-18-character matrix could not be represented in its usual position, and it was turned on its side. Thus left-to-right printing will appear to move from top to bottom, and the paper will advance across the screen from left to right instead of bottom to top.



5. An animated printer. If the same printer (a) is modeled in a personal computer having high-resolution graphics and a three-dimensional animation package, the main sections of the printer may be seen in motion (b).

The lines across the bottom of the screen represent the visual indicators available to the operator and the simulation's status. The bottom line is also used to insert external commands. In addition, the status of any analog block that is requested is represented in the BLK command. Block 45 in Fig. 3a indicates in inches the amount of paper left in the machine.

The simulation is nearly complete in Fig. 3b. The head, whose position is represented by the quad character, is moving from top to bottom, and the paper is advanced (Fig. 3c). Figure 3d represents the start of another simulation. On the other hand, faults and their results can be placed on the model and observed. Figure 4 shows the result of a head-advance fault that was applied to the model.

A head-carrier fault that caused the head to bind is shown in Fig. 4b. If this fault remained on the model, it would eventually cause the head-drive cable to break.

An animated output

The same model that was used on the IBM 5110 was transferred to a personal computer having high-resolution graphics. Minimal conversions were required, and the block-calculation portion of the model remained essentially the same. However, the external input routine was changed so that a user could interact with the display to determine when commands were to be entered, as opposed to, depending on the simulation-cycle counts that were used on the 5110.

The major modifications to the model concerned the graphics output. The model was linked to a three-dimensional graphics-animation package. This software package permited solid objects to be represented with X, Y, and Z coordinates (Fig. 5). In addition, other controls are available so that objects may be moved around all of the axes.

However, mechanical-fault simulation should not be limited to maintenance package validation. It could be used to develop maintenance analysis procedures. A detailed model of the subject machine can be prepared. The model can be "bugged" and exercised, and the resulting output can be used to generate procedures instead of just validating them.

The model may also be used to justify maintenance features. These features, not planned for inclusion in the prototype machine because of cost or performance considerations, can now be evaluated with the model. □

ZyMOS Custom Design Report 2

Choice Of CAD Workstation Can Insure Working Silicon.

Automated design tools for creating customized ICs are reaching new levels of sophistication. Today's system designer can "tailor" VLSI circuits within weeks—without the need to know complex semiconductor device physics.

Getting working silicon the first time out, however, requires the judicious selection of a CAD workstation. And the vendor supplying it. In this report, second in a series, ZyMOS presents the key factors in CAD workstation selection as they relate to standard-cell chip design.

Pick Software Before Hardware.

Despite the numerous workstations now available, very few come equipped with the necessary software to insure working silicon. CAD software that generates testing parameters, for example, is seldom furnished with a workstation. Also missing from most workstations is the essential software to perform placement and routing.

When it comes to standard-cell chip design, software should be evaluated before the hardware selection is made. The best workstation packages include a complete range of software that is tied to a well-modeled applications library.

ZyPAWS Turnkey Workstation. *Equipped with ZyP software, this automated workstation from ZyMOS employs a 32-bit computer with virtual addressing, along with 1.5 Mbytes of main memory and up to 160 Mbytes of disc memory. This universal system supports up to 30 users and includes color graphics capabilities.*

From logic simulators through placement-and-routing to test-vector generation, the system designer should be concerned with two questions: "How well does the software allow me to verify my logic design?" and "How can I be assured of quickly moving to production volume of working silicon that matches my logic simulation?"

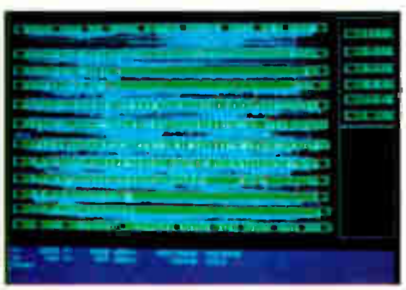
Take The Risk Out of Vendor Selection

Although most suppliers of CAD workstations strive for working chips the first time out, nobody pursues this objective with more vigor than the IC manufacturer. After all, the IC manufacturer's livelihood ultimately depends on selling working chips—not the hardware/software used to create them.

The most effective CAD software is supplied by experienced semiconductor manufacturers. Those manufacturers truly committed to IC design automation will guarantee that your custom chip matches your logic simulation.

Look For Universality In Workstations

When you evaluate workstations, look for one that is universal. The ideal choice will run the sophisticated CAD software you need today, as well as the applications libraries of the future.



Logic-Level. *All interaction with ZyP, including mask artwork design, is performed at the logic level where system designers are most productive.*

A well-modeled applications library is critical to the success of a standard-cell IC design program. The ZyP applications libraries from ZyMOS are a good example of a rich selection of well-modeled cells, with over 350 to choose from.

Once you've picked the CAD workstation package you need, there's one more important consideration. Be sure there's a qualified second source that can make chips from the applications library you use.

Start Your Evaluation With Us

As a leading proponent of standard-cell chip design, ZyMOS wants to help you negotiate the custom IC maze through this series of reports. Look for others including: *Evaluating Standard Cells for Automated Custom IC Design; Designing for Testability; Second Source Alternatives; Simulation/Modeling for Accurate Performance Prediction;* and *Importance of Extensive Applications Libraries.*

If your need is immediate, call or write today. Ask about our 3½ day course that gets you ready to design your first custom chip. And get the details on ZyPAWS (ZyP Automatic Workstation). Designed as a standard-cell, turnkey system, ZyPAWS is the industry's first fully integrated workstation available from a semiconductor manufacturer.

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ZyMOS
Producing The Standard In Custom VLSI

Program displays contents of memory on printer

by David V. Fansler
Biomedical Reference Laboratories Inc., Burlington, N. C.

RCA's CDP18S694 microcomputer development system—a low-cost solution when programs in Basic or assembly language need to be created—may be linked with the proper interface to Centronics' compatible parallel interface printer for hard-copy output. With this program, an operator can use the printer to print out the contents of the development system's memory in the format employed by the system's built-in monitor UT-62.

MEMORY DISPLAY PROGRAM FOR RCA's CDP18S694 DEVELOPMENT SYSTEM

```
0000 ;                   0014                     ORG =F000
F000 ;                   0015                     SP = =02
F000 ;                   0016                     PC = =03
F000 ;                   0017                     CALL = =04
F000 ;                   0018                     RETN = =05
F000 ;                   0019                     ERROR = =8085
F000 ;                   0020                     OPTION = =8200
F000 ;                   0021                     PRMPT2 = =82
F000 ;                   0022                     OSTRNG = =83F0
F000 ;                   0023                     INIT2 = =83F6
F000 ;                   0024  . .
F000  7100 ;             0025  DIS, =00                            . . DISABLE INTERRUPTS
F002  F8F0B3 ;           0026  LDI A.1 (DISPLY); PHI PC            . . LOAD PROGRAM COUNTER
F005  F80BA3 ;           0027  LDI A.0 (DISPLY); PLO PC            . . WITH PROGRAM ADDRESS
F008  C083F6 ;           0028  LBR INIT2                           . . GOTO INITIALIZATION SUBROUTINE
F00B  E3 ;               0029  DISPLY:   SEX PC                    . . SET X → PROGRAM COUNTER
F00C  6101 ;             0030            OUT 1, =01                . . SELECT PRINTER I/O
F00E  E2 ;               0031            SEX SP                    . . SET X → STACK POINTER
F00F  D483F00D0A ;       0032            SEP CALL; , A (OSTRNG), =0D0A
F014  4D454D4F525920 ;   0033            , T 'MEMORY DUMP TO PRINTER', =0D0A
F01B  44554D5020544F ;   0033
F022  205052494E5445 ;   0033
F029  520D0A ;           0033
F02C  46524F4D2D544F ;   0034            , T 'FROM-TO', =00
F033  2000 ;             0034
F035  D48200 ;           0035            SEP CALL; , A (OPTION)    . . GET DUMP ADDRESS
F038  FB0D ;             0036            XRI =0D                   . . IS LAST ENTRY A CARRIAGE RETURN
F03A  CA8085 ;           0037            LBNZ ERROR                . . IF NOT GOTO ERROR
F03D  F80DBF ;           0038  OUTPUT:   LDI =0D; PHI RF           . . ELSE LOAD A CARRIAGE RETURN
F040  D4F0D8 ;           0039            SEP CALL; , A (PRINT)     . . AND PRINT
F043  D4F073 ;           0040            SEP CALL; , A (OUT1)      . . GO PRINT ADDRESS
F046  F820BF ;           0041  SPCOUT:   LDI =20; PHI RF           . . PRINT A SPACE
F049  D4F0D8 ;           0042            SEP CALL; , A (PRINT)     . .
F04C  0BBF ;             0043  DATOUT:   LDN RB; PHI RF            . . GET DATA
F04E  D4F0B8 ;           0044            SEP CALL; , A (OUTDAT)    . . GO OUTPUT DATA
F051  9A ;               0045            GHI RA                    . . GET HIGH-BYTE COUNT
F052  3A60 ;             0046            BNZ NOTDON                . . IF NOT 0 BRANCH
F054  8A ;               0047            GLO RA                    . . GET LOW-BYTE COUNT
F055  3A60 ;             0048            BNZ NOTDON                . . IF NOT 0 BRANCH
F057  F80DBF ;           0049            LDI =0D; PHI RF           . . LOAD A CARRIAGE RETURN
F05A  D4F0DE ;           0050            SEP CALL; , A (PRINT1)    . . AND PRINT
F05D  C00082 ;           0051            LBR PRMPT2                . . RETURN TO UT62
```

```
F060  2A ;          0052  NOTDON:  DEC RA                 .. ELSE BYTE COUNT-1
F061  8BFA0F ;      0053           GLO RB; ANI #0F        ... GET LOW-BYTE COUNT
F064  3A6E ;        0054           BNZ SAMELN             .. IF NOT 0 BRANCH
F066  F83BBF ;      0055           LDI #3B; PHI RF        .. ELSE LOAD ';'
F069  D4F0D8 ;      0056           SEP CALL; , A (PRINT)  .. AND PRINT
F06C  303D ;        0057           BR OUTPUT              .. GOTO OUTPUT
F06E  F6 ;          0058  SAMELN:  SHR                    .. SHIFT BYTE COUNT
F06F  334C ;        0059           BDF DATOUT             .. IF DF = 1 BRANCH
F071  3046 ;        0060           BR SPCOUT              .. ELSE PRINT A SPACE
F073  9B ;          0061  OUT1:    GHI RB                 .. GET HIGH ADDRESS
F074  F6F6F6F6 ;    0062           SHR; SHR; SHR; SHR     .. MASK LOWER FOUR BITS
F078  FCF6 ;        0063           ADI #F6                .. AND CONVERT TO
F07A  3B7E ;        0064           BNF TY4                .. HEXADECIMAL
F07C  FC07 ;        0065           ADI #07                ..
F07E  FFC6BF ;      0066  TY4:     SMI #C6; PHI RF        .. CONVERT TO ASCII
F081  D4F0D8 ;      0067           SEP CALL; , A (PRINT)  .. AND PRINT
F084  9BFA0F ;      0068           GHI RB; ANI #0F        .. GET HIGH ADDRESS
F087  FCF6C7 ;      0069           ADI #F6; LSNF          .. MASK FOUR HIGH BITS
F08A  FC07 ;        0070           ADI #07                ..
F08C  FFC6BF ;      0071           SMI #C6; PHI RF        .. CONVERT TO ASCII
F08F  D4F0D8 ;      0072           SEP CALL; , A (PRINT)  .. AND PRINT
F092  8B ;          0073           GLO RB                 .. GET LOW ADDRESS
F093  F6F6F6F6 ;    0074           SHR; SHR; SHR; SHR     .. MASK FOUR LOW BITS
F097  FCF6 ;        0075           ADI #F6                .. THEN CONVERT TO
F099  3B9D ;        0076           BNF TY5                .. HEXADECIMAL
F09B  FC07 ;        0077           ADI #07                ..
F09D  FFC6BF ;      0078  TY5:     SMI #C6; PHI RF        .. CONVERT TO ASCII
F0A0  D4F0D8 ;      0079           SEP CALL; , A (PRINT)  .. AND PRINT
F0A3  8BFA0F ;      0080           GLO RB; ANI #0F        .. GET LOW ADDRESS
F0A6  FCF6C7 ;      0081           ADI #F6; LSNF          .. MASK FOUR HIGH BITS
F0A9  FC07 ;        0082           ADI #07                .. THEN
F0AB  FFC6BF ;      0083           SMI #C6; PHI RF        .. CONVERT TO ASCII
F0AE  D4F0D8 ;      0084           SEP CALL; , A (PRINT)  .. AND PRINT
F0B1  F820BF ;      0085           LDI #20; PHI RF        .. LOAD A SPACE
F0B4  D4F0D8 ;      0086           SEP CALL; , A (PRINT)  .. AND PRINT
F0B7  D5 ;          0087           SEP RETN               .. THEN RETURN
F0B8  9F ;          0088  OUTDAT:  GHI RF                 .. GET DATA AND MASK
F0B9  F6F6F6F6 ;    0089           SHR; SHR; SHR; SHR     .. THE FOUR LOW BITS
F0BD  FCF6 ;        0090           ADI #F6                .. CONVERT TO HEXADECIMAL
F0BF  3BC3 ;        0091           BNF TY6                .. THEN
F0C1  FC07 ;        0092           ADI #07                ..
F0C3  FFC6BF ;      0093  TY6:     SMI #C6; PHI RF        .. CONVERT TO ASCII
F0C6  D4F0D8 ;      0094           SEP CALL; , A (PRINT)  .. AND PRINT
F0C9  4BFA0F ;      0095           LDA RB; ANI #0F        .. GET DATA AND MASK
F0CC  FCF6C7 ;      0096           ADI #F6; LSNF          .. THE FOUR HIGH BITS
F0CF  FC07 ;        0097           ADI #07                .. CONVERT TO HEXADECIMAL
F0D1  FFC6BF ;      0098           SMI #C6; PHI RF        .. CONVERT TO ASCII
F0D4  D4F0D8 ;      0099           SEP CALL; , A (PRINT)  .. AND PRINT
F0D7  D5 ;          0100           SEP RETN               .. THEN RETURN
F0D8  9F ;          0101  PRINT:   GHI RF                 .. GET DATA
F0D9  FB0A ;        0102           XRI #0A                .. CHECK FOR LINE FEED
F0DB  32F0 ;        0103           BZ EXITDF              .. IF SO GOTO EXITDF
F0DD  9F ;          0104           GHI RF                 .. ELSE GET DATA
F0DE  9F ;          0105  PRINT1:  GHI RF                 .. GET DATA AGAIN
F0DF  FBFF ;        0106           XRI #FF                .. AND INVERT
F0E1  52 ;          0107           STR SP                 .. PLACE ON THE STACK
F0E2  34E2 ;        0108           B1 •                   .. LOOP IF PRINTER BUSY
F0E4  66 ;          0109           OUT 6                  .. OUTPUT DATA
F0E5  22 ;          0110           DEC SP                 .. REPOSITION STACK POINTER
F0E6  9F ;          0111           GHI RF                 .. GET DATA
F0E7  FB0D ;        0112           XRI #0D                .. CHECK FOR CARRIAGE RETURN
F0E9  3AF0 ;        0113           BNZ EXITDF             .. IF NOT GOTO EXITDF
F0EB  F80ABF ;      0114           LDI #0A; PHI RF        .. IF SO OUTPUT A LINE FEED
F0EE  30DE ;        0115           BR PRINT1              .. AND PRINT
F0F0  D5 ;          0116  EXITDF:  SEP RETN               .. AND RETURN
F0F1  ;             0117
F0F1  ;             0118
F0F1  ;             0119  END
0000
```

In addition, UT-62 communicates with the user's terminal, cassette-storage and memory-handling functions and produces a hexadecimal memory display on the terminal.

The development system selects the printer port by issuing a 61_{16} output instruction with group number 01_{16} while output instruction 66_{16} feeds data into the printer. In addition, external flag EF_1 monitors the busy and acknowledge lines of the printer. The stack pointer, program counter, subroutine-call program, and subroutine-return program are assigned to registers R_2, R_3, R_4, and R_5. ERROR, OPTION, PROMPT2, OSTRNG, and INIT2, which are subroutines of the UT-62, are also incorporated in the program.

An initialization procedure ends with the beginning address in register RB and the byte count in register RA. The American Standard Code Information-Interchange code for a carriage return is loaded in register RF.1, as is all other data that is to be printed. As a result, when the print subroutine is called, it initiates a carriage return followed by an automatic line feed. Thereupon a subroutine jump to OUT1 via TY5 converts the address of the first byte on the line into ASCII and prints it.

DATOUT loads the data from the address in RB into RF.1 and then calls subroutine OUTDAT. This subroutine converts the data into a pair of ASCII hexadecimal characters for printing. Upon return from OUTDAT, DATOUT checks RA for a zero byte count. If the byte count is zero, a final CR is printed and the program returns to the monitor. Otherwise the byte count is decremented by 1 and a check is made to see if the 4 least significant bits of the address are F_{16}. When this condition is met, a semicolon is printed and the program branches back to OUTPUT; if the condition is not met, the LSB is checked at SAMELN.

When the LSB bit is 1, the program branches to DATOUT for the next byte of data, but when it is 0, goes to SPCOUT for printing a space between printed data. ☐

Software notebook is a regular feature in *Electronics*. We invite readers to submit short, original, unpublished programs and software solutions to engineering problems. Explain briefly and thoroughly the program's operation. We'll pay $75 for each item published.

64-K dynamic RAMs act as peripheral storage for Z80

by B. J. Sparling
University of Reading, Whiteknights, Reading, England

Most users will confess that their computer never has enough storage space. Unfortunately, extra dynamic random-access memory is usually difficult to incorporate. This hardware and software integration allows the 8-bit Z80 microprocessor to tap a maximum of four 64-K dynamic RAMs.

To drive this peripheral memory system, a read and a write routine are used. In addition, with two more octal latches and a high-byte data port, the design can be expanded with simple software commands to operate with 16-bit processors.

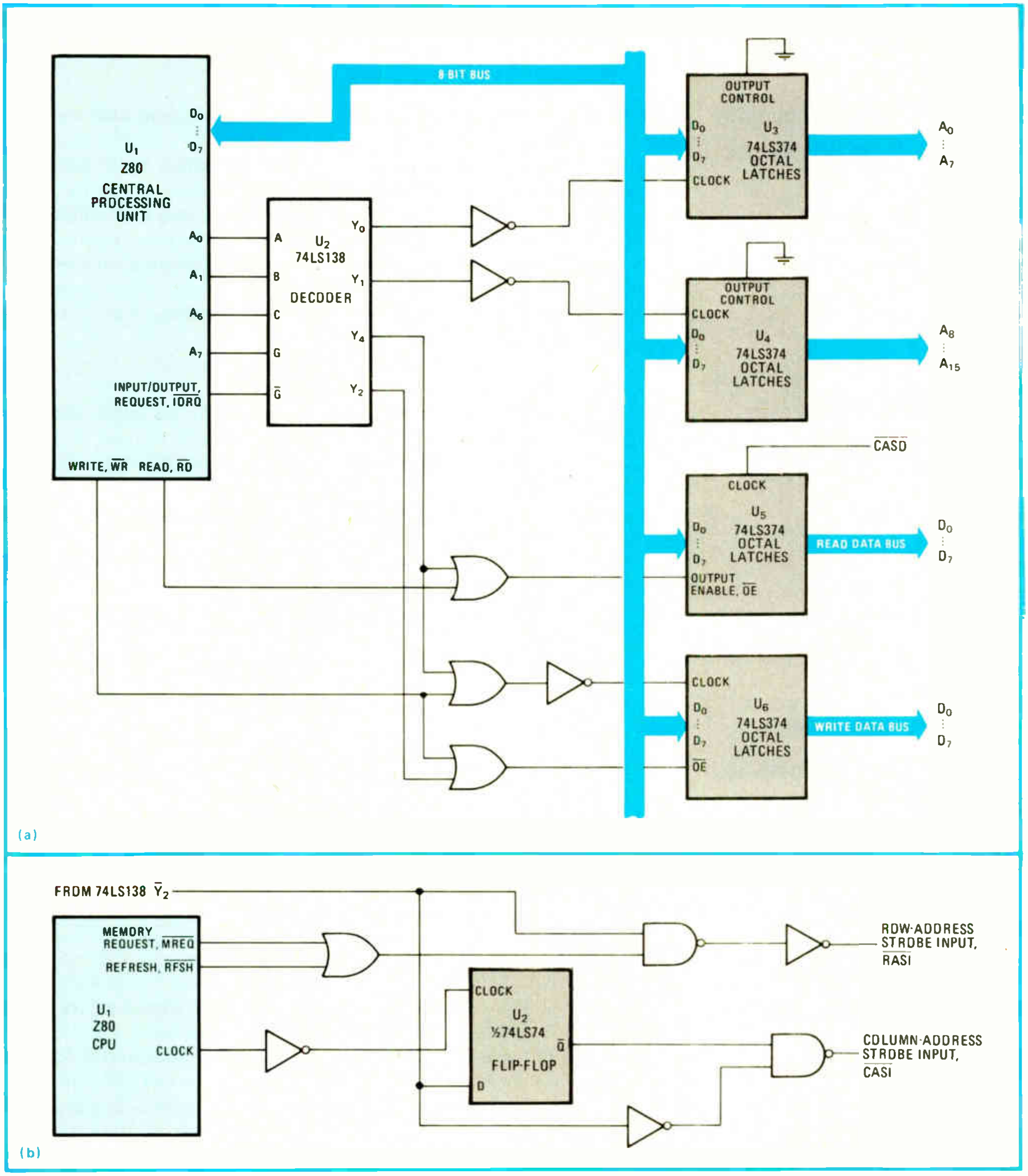
The read routine requires 80 clock (T) cycles, while the write routine uses 83 T cycles. Thus with a 4-megahertz clock, the memory access time is 20 microseconds. Memory is accessed through the processor's input/output request line IORQ and decoder U_2 (a).

Octal latches U_3 through U_6 are used as ports to hold address and data bytes that are generated by the central processing unit. The I/O decoding presents the low and high bytes of address at ports 80_{16} and 81_{16}, respectively. In addition, the data port is at $C0_{16}$, while the control port, which enables the latches that are set, is at port 82_{16}. The address latches are permanently enabled and clocked by the appropriate outputs from decoder U_2.

For writing data into memory, the data latch is enabled when the write line is active and the control port is selected. This latch is also clocked by both the data port and the write line. For reading data from memory, the data latch is enabled when the data port is accessed and the read line is active. The data latch is clocked by the

ROUTINES FOR PERIPHERAL RANDOM-ACCESS MEMORY

```
LOWADD  EQU  80H
HIADD   EQU  81H
CTRL    EQU  82H
DATA    EQU  C0H
;
;       Routine to read a byte of data
;       HL contains address to read from
;       Result returned in register E
;
READ  LD C, LOWADD      ; C = low address
      OUT (C), L        ; Output low-address byte
      INC C             ; C = high address
      OUT (C), H        ; Output high-address byte
      INC C             ; C = control port
      IN C, (C)         ; Control read
      LD C, DATA        ; C = data port
      IN E, (C)         ; Read data byte
      RET
;
;       Routine to write a byte of data
;       HL contains address to write to
;       Byte to be written is in register E
;
WRITE LD C, LOWADD      ; C = low address
      OUT (C), L        ; Output low address
      INC C             ; C = high address
      OUT C, (H)        ; Output high address
      LD C, DATA        ; C = data port
      OUT (C), E        ; Output data byte
      LD C, CTRL        ; C = control port
      OUT (C), C        ; Control write
      RET
```



Facility. This Z80 hardware-software integration lets dynamic random-accesss memories be added as peripheral storage. The memory is accessed through the CPU's IORQ line and decoder U_2 (a). Octal latches U_3 through U_6 are utilized as ports to hold address and data bytes generated by the CPU. D-type flip-flop 74LS74 introduces the desired delay between the row-address and column-address pulses (b).

column-address–strobe (CAS) output from the dynamic controller, which is used to refresh the dynamic random-access memory.

Since a row-address–strobe (RAS) pulse is generated either when the control port is accessed or when a refresh cycle is initiated, it is necessary to introduce a delay between the RAS and CAS pulses in order to accommodate the setup times contained within the dynamic RAMs. The delay is achieved with a D-type flip-flop that produces a CAS pulse on the falling edge of the system clock pulse (b) immediately after the control port has been accessed. □

Engineer's newsletter

Repairing removable data-module disk packs

Winchester-type data modules, which have been discontinued by most disk-pack manufacturers, may now be repaired quickly and inexpensively. Used in drives like IBM's 3340 or NCR's 6590-0201, the modules will be completely remanufactured by Precision Methods Inc. at its Salem, N. H., facility. **In addition, the units will come with a new pack warranty.** The repair of data modules is a complex process, and the firm has all the necessary tools and instrumentation. Additional information may be obtained by writing to Ogden Thompson, vice president, Precision Methods Inc., 8825 Telegraph Rd., Lorton, Va. 22079, or calling (703) 339-7050.

Ionic process raises linear IC reliability

Called Nitride plus, this ionic protection process shields linear ICs from the harmful effects of chemicals, sodium ions, moisture, and electrical charge and thus substantially improves their performance and reliability. Conventional plasma-deposited nitride passivation techniques have been ineffective for such circuits because of their high-voltage operation and tendency to spread lateral charge. However, National Semiconductor Corp., Santa Clara, Calif., solves the problem with a **process that has demonstrated an 85% improvement in the performance of bipolar operational amplifiers, a 98% improvement in junction–field-effect-transistor op-amp** performance, and an 86% improvement in voltage-regulator performance.

Packaging technique keeps static away

Sealed Air Corp. will be conducting a series of seminars on the use of antistatic packaging in the first half of this year. To be held in such cities as Atlanta, Boston, Chicago, Houston, and Hayward, Calif., the seminars will introduce manufacturers to a packaging and shielding technique that **helps reduce product damage due to electrostatic discharge.** If you would like more information on the meetings, write to Bill Armstrong, Sealed Air Corp., Old Sherman Turnpike, Danbury, Conn. 06810, or call (203) 792-2360.

Home-study kit teaches semicustom design

If you're a design engineer with a need to convert logic schematics into semicustom ICs, you might find a new self-study training kit of help. Released by NCR Corp.'s Microelectronics division, it takes you through all the steps of IC design using NCR's complementary-MOS and n-channel MOS cell libraries. In addition, it trains you in how to use the computer-aided design tools supporting NCR's Semicustom Design System. The exercises contained in the study guide closely simulate all the tasks that engineers must perform in the actual design process, including the use of CAD programs. Buyers of the kit may also use a complete set of advanced CAD programs, provided they have access to a standard terminal and a public time-sharing network.

The $4,995 training kit includes **study guides, audio-cassette tapes, a user's manual, NCR's n- and C-MOS standard-cell libraries, and program instructions.** However, the price does not include computer time used in accessing the CAD programs. If you are interested in obtaining more information, write to NCR-SDS Training Kit, NCR Microelectronics Division, 8181 Byers Rd., Miamisburg, Ohio 45432, or call (513) 866-7217.

–Ashok Bindra

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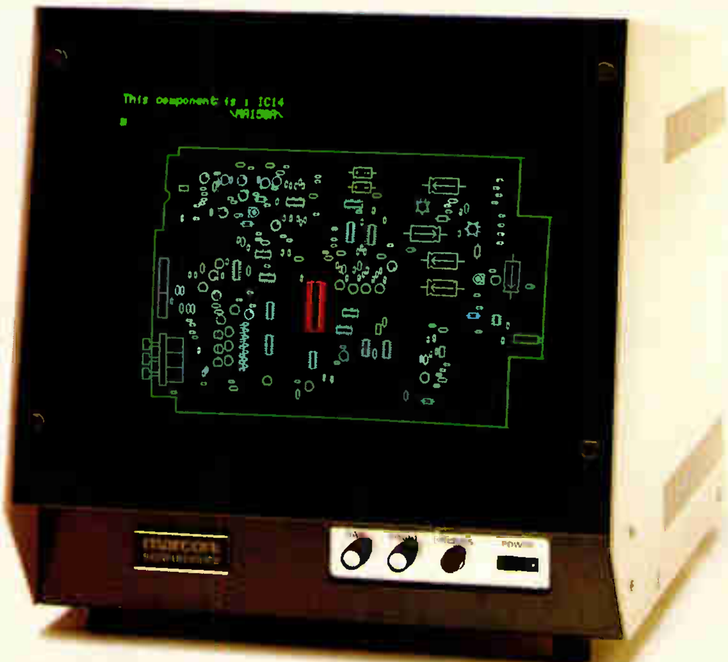

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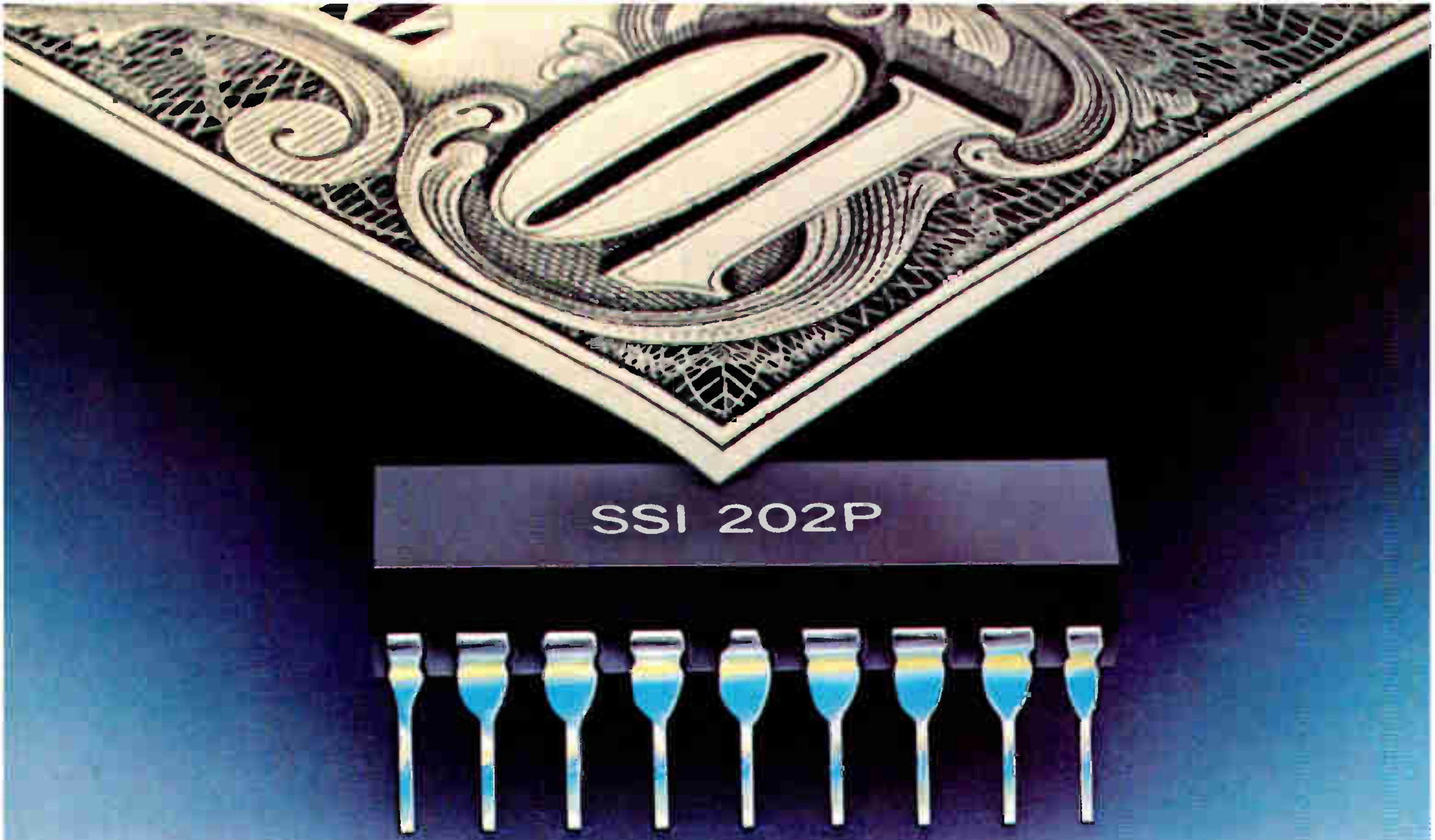
Circle 155 on reader service card



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Circle 156 on reader service card

System superimposes graphics on video

Display generator synchronizes computer-graphics output with standard video signal from any of a number of sources

by Linda Lowe, Boston bureau manager

Combining high-resolution color graphics with video images on a display screen should become a more affordable option with the GraphOver 9500 raster-scan display generator. A boon for applications demanding video's realism together with interactive graphics, its developer, New Media Graphics Corp., says the $9,850 GraphOver 9500 is an off-the-shelf implementation of a process that formerly involved expensive retrofits of graphics systems with video capabilities (or *vice versa*).

Such customized solutions have often driven system costs into the tens of thousands of dollars, notes Martin Duhms, president of New Media Graphics. Thus the 9500 could spur a wider range of applications, from military or industrial simulation and training (where, for instance, graphics showing changing aircraft conditions could overlie video footage of the view from the cockpit window) to industrial training and production prompting (where a graphics display of changing production parameters might be combined with video pictures of parts being manufactured).

The 9500, which can operate as a stand-alone unit or as a peripheral on a host computer, incorporates an 8-bit Motorola MC6809 microprocessor as a controller and uses NEC Microcomputers Inc.'s μPD7220 graphics display controller (GDC). With the system's Sigos operating system, users can program graphics applications in whatever language their host computer supports.

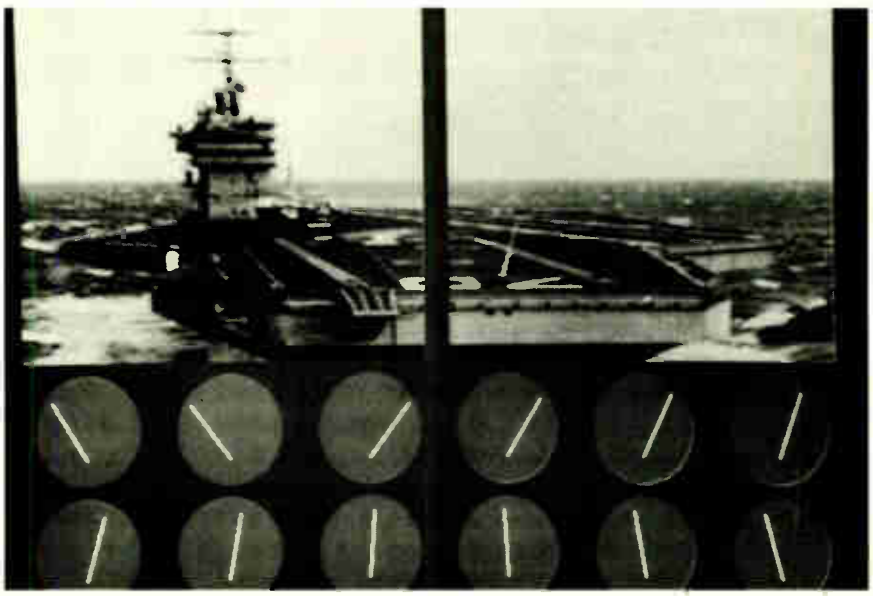
The generator synchronizes and merges its generated graphics images with video signals it receives from all standard video cameras, video-disk players, and video-cassette recorders. It drives standard red-green-blue and National Television Standards Code (NTSC) displays.

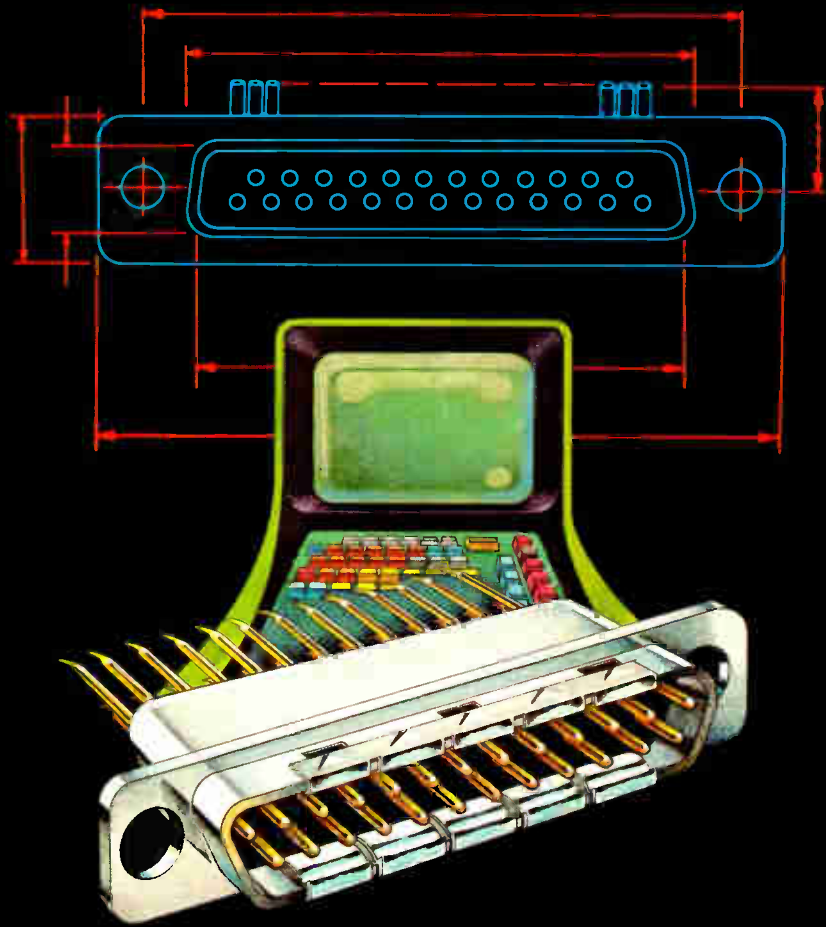
Getting in sync. Exact synchronization of graphics with video signals, the critical element in producing clear, stable displays, required that the 9500 be designed from the ground up to avoid the need for expensive, specialized components, notes Jeffrey L. Wise, vice president of engineering. Compounding the problem, he adds, is the fact that some video signals, particularly those from laser–video-disk players, may be quite noisy and prone to missing synchronization signals.

The 9500's video interface, called a gen/lock, contains a synchronous detector that senses only those signals arriving at the standard NTSC-prescribed rate, thus screening out much random noise, says Wise. The gen/lock also includes a dedicated phase-locked loop whose local oscillator synchronizes with the phase and frequency of incoming video signals; in case of an interruption of the signal, the loop automatically locks to the unit's own internal reference oscillator and supplies its own generated version of the missing signal without disturbing the flow of video information to the display screen.

The phase-locked loop's local oscillator acts as master timekeeper for the whole system, supplying the clock rates of the unit's MC6809 supervisor and μPD7220 GDC. Thus driven, the GDC can generate graphics signals perfectly synchronized to the video. Drawing alphanumeric and graphics information at a rate of up to 850,000 picture elements per second, the GDC drives the 9500's 64-K-byte display memory.

The display memory stores images in a 768-by-682-pixel buffer in which all pixels are individually addressable. Pixel data passes from the dis-





play memory through video shift registers and a hardware area-fill circuit, into a 16-word-by-8-bit lookup table that defines up to 16 pixel color values from a palette of 64 hues. Reloadable by the 6809 during one vertical retrace interval, the lookup table makes possible fast redefinition of colors, animation, and blinking. Other graphics functions include pan, zoom, and hardware-implemented area fill at video rates.

Switch hitting. Once out of the lookup table, graphics information passes through a digital-to-analog converter, which breaks it into its component colors. The analog graphics data then feeds, along with a video signal also coded into its component colors, into a keyer switch that can switch either video or graphics to the output in 20 ns.

The generator has both an RGB and an NTSC output stage: graphics and video signals are encoded into both formats and can drive both kinds of monitors simultaneously. It produces a 30-kHz interlaced display, with graphics appearing in a matrix of 768 by 480 pixels.

The 9500 supports inputs from up to two video-disk players, switching between them in receiving their incoming signals. It also incorporates an audio switcher that can accommodate two stereo audio sources.

The generator connects to host computers over an RS-232-C asynchronous serial link with a selectable transmission rate of 110 to 19,200 bauds; for higher-speed applications, a Centronics-compatible parallel interface with a data transfer rate of 20 kilobytes/s is also available. Cables for these as well as for audio and video connections cost $55 each, plus $1 per foot of cable.

The GraphOver 9500 also comes with optional interactive peripheral devices, such as an 11-in.-square graphics tablet and a joystick, which both cost $1,450. The system supports touch-sensitive screens and can drive video hard-copy devices in addition to all standard monitors.

Deliveries will begin in March.

New Media Graphics Corp., 145 Main St., Cambridge, Mass. 02142. Phone (617) 547-4344 [338]

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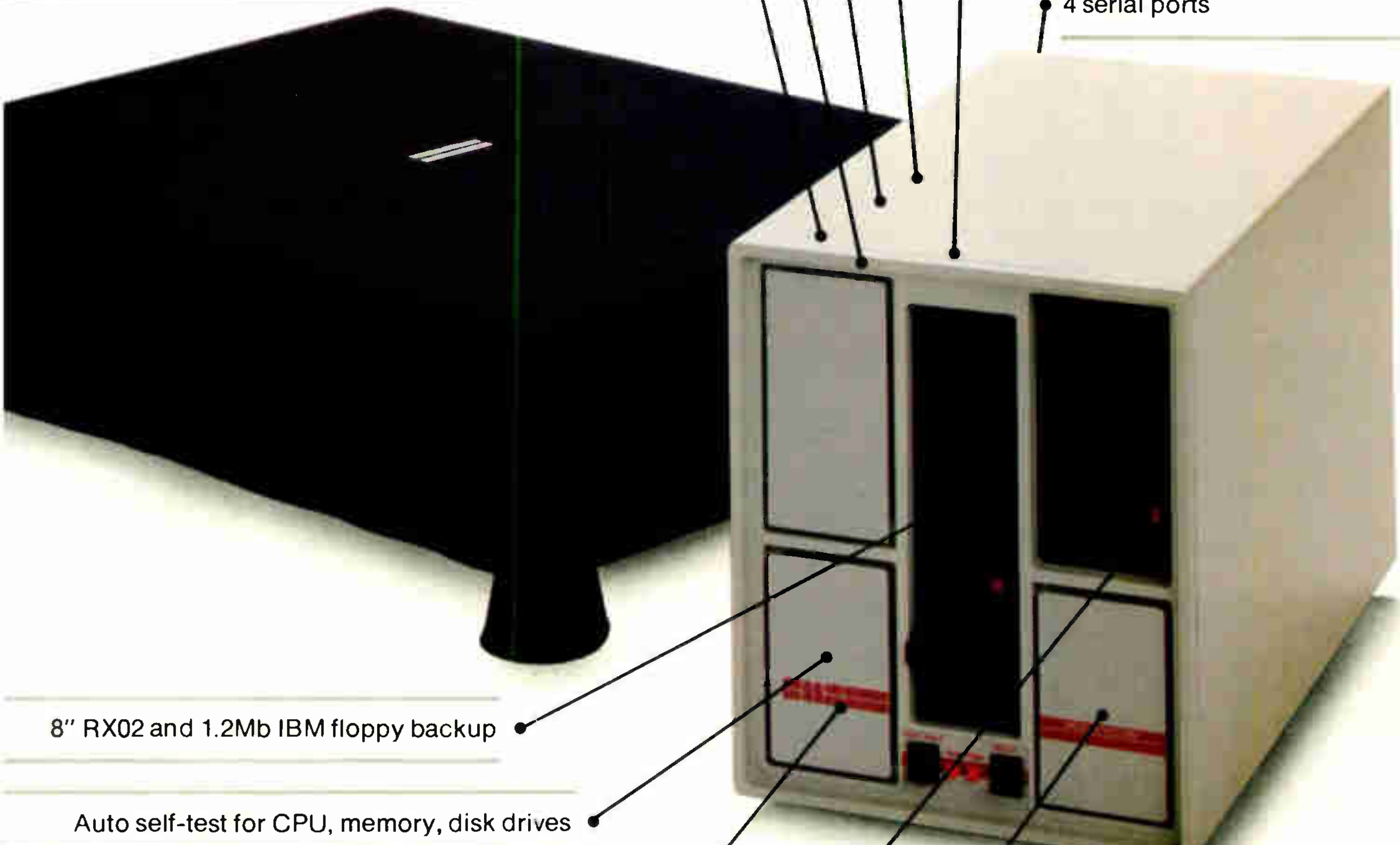

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Circle 159 on reader service card

Computers & peripherals

Power doubles in 32-bit line

Superminicomputer holds line in price despite performance jump to 2.5 million whetstones

In the race for midrange computer power, the Eclipse MV/10000 leapfrogs over the MV/8000 as Data General Corp.'s high-end superminicomputer, providing twice the performance at roughly the same price. The 32-bit machine with virtual memory [*Electronics*, Feb. 24, p. 41] clocks in at 2.5 million single-precision and 1.9 million double-precision whetstone operations per second, according to the firm.

Supporting up to 192 users and having a main memory expandable to 16 megabytes, the 10000 is targeted for computer-aided engineering and design, technical time-sharing, and real-time computation applications. The model adds a dedicated address generator, a dual-board floating-point processor, and advanced Schottky logic chips to the highly pipelined parallel 8000 architecture to achieve its superior performance.

Project engineer Robert W. Beauchamp notes that the 10000 is the first Data General computer to incorporate a dedicated address generator. As one instruction is executed, the next address is generated in parallel. "This cuts memory access time in half," he explains. Since microcycle time in the 10000 has been clipped from 220 ns down to 140 ns, the benefits of parallel address generation are compounded. Thus, a load-and-store instruction requiring two cycles on the 8000 would be executed in 440 ns. On the 10000, execution time is just 140 ns.

Using advanced Schottky logic and memory chips helped Data General reduce microcycle time. Beauchamp cites the use of Texas Instruments' new 74AS881 and -82 chips in the arithmetic and logic unit and of Fairchild Semiconductor's 74F3374 for its octal register. In addition, the firm turned to Intel for its new n-channel MOS 2125H-2, 2147H-1, and 2147H-2 static random-access memories, and the gate-array chips in the instruction parser were custom-designed by Fujitsu.

Division of labor. A key to the 10000's price and performance is the efficient division of labor between two identical hardwired floating-point processors. One board handles single-precision operations, the other double-precision ones. A mode bit produced by the instruction parser indicates whether an operation is single- or double-precision.

"We couldn't get the performance we wanted on one board," explains Beauchamp. "And once we decided to go for two, it was clear that the cheapest way to achieve economies of scale in production was to make them identical. We feel we've extended the concept of bit-slice to the board level in wiring up the two identical boards."

The third design enhancement in the 10000 is the use of two input/output controllers, allowing a doubling of bandwidth into the central processing unit. With each controller able to handle 14.3 megabytes/s, the dual-controller configuration makes possible an aggregate I/O rate to and from the CPU of 28.6 megabytes/s. The second I/O controller, available later this year, is an option.

Board memory, available in 0.5-, 1-, and 2-megabyte modules, is expandable to a total of 16 megabytes. The system supports a virtual address space of 4 gigabytes. Total on-line storage capacity with two I/O controllers is 18.5 gigabytes; with one I/O controller, it is 9.4 gigabytes.

The 10000 runs both the Data General AOS/VS operating system and the real-time AOS/RT32. Among the languages it supports are Fortran 77, Cobol, Basic, Pascal, PL/1, C, APL, RPG II, and DG/l.

Equipped with 2 megabytes of main memory, a 147-megabyte disk drive, tape drive, 16-channel multiplexer, hard-copy console, and AOS/VS operating system license and entitlements, the 10000 is priced at $211,100. With 8 megabytes of main memory and a 602-megabyte disk drive, it is priced at $291,100. Delivery is in 90 to 120 days.

Data General Corp., 4400 Computer Dr., Westboro, Mass. 01580. Phone (617) 366-8911 [361]

Printer trades speed, density

Multiple-pass dot-matrix units can approach letter quality or run at up to 180 characters/s

Having had notable success with its Spinwriter printer line, which puts out fully formed characters, NEC Information Systems Inc. is entering the dot-matrix market with two multiple-mode models priced under $1,000. "These new Pinwriter models are multifunction high-reliability products at an affordable price. As far as I am aware, the combination of quality and reliability is unique in this price range," notes Pete Lowry, printer product line manager for the subsidiary of Japan's Nippon Electric Co. He notes that the Pinwriter line is another step in NEC's plan to become a factor in all printer markets.

The P1, priced at $895 in single units, runs at 180 characters/s using

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a seven-by-nine-dot matrix and in a high-density 13-by-9-dot mode at 90 c/s. Lowry describes the latter mode as "near letter quality."

The P2 model offers both these modes and adds 30-c/s dual-pass operation. After the initial pass, the paper is advanced half a dot and reprinted for higher resolution. Though the P1 comes equipped with four fonts and the P2 with six, more fonts can be added and stored in the P2. The P2 is priced at $995.

Long life. The 18-pin print head used in the machines has an estimated life of 200 million dots per pin, according to Lowry. Mean time between failures is said to be 4,000 h, with a mean time to repair of 20 min. The Pinwriters require no periodic lubrication or adjustments.

Both the P1 and P2 models print 80 columns at 10 characters per in. Dot size is 0.3 mm, and resolution is 120 dots/in. both vertically and horizontally. Line spacing is selectable as 3, 4, 6, or 8 lines/in. A third unit, the $1,150 model P3, has the same features as the P2 but prints 136 columns at 10 c/in.

The standard pinch-roller feed of the P1 and P2 can accommodate paper 4.5 to 10 in. wide. Adjustable tractors are optional. The printers' endless-cassette fabric ribbon is rated at 2.2 million characters. The noise produced by the Pinwriters is at a relatively low level: 62 dBa at full speed and 64 dBa for high density.

The P1 is available for initial shipments in April. The P2 and P3 will be available in October.

NEC Information Systems Inc., 5 Militia Dr., Lexington, Mass. 02173. Phone (617) 862-3120 [362]

68000-based microsystem offers megabyte main memory

Strengthening its family's claim in minicomputer territory, the Sage IV 16-bit microsystem comes with 128-K bytes of main memory, expandable to 1 megabyte, and can serve six users at a time. Like the firm's Sage II (which has a 512-K-byte maximum), the new machine is based on an 8-MHz 68000 and can execute 2 million instructions a second.

Built into the desktop Sage IV is a drive accommodating a 5-to-30-megabyte Winchester disk with a 5¼-in. floppy-disk unit for backup. The computer operates without wait states, thus speeding access to auxiliary storage. A 20-K-byte file can be loaded from the floppy disk in 1 s or from the hard disk in 0.10 s.

Other standard features of the Sage IV include the UCSD p-System version 4.1 operating system, compilers for Basic, Fortran 77, and Pascal, a screen-oriented editor, and two RS-232-C serial commmunications ports. With a 128-K-byte random-access memory and facilities for a 5-megabyte hard disk, the Sage IV has a list price of $6,800.

Sage Computer Technology, 35 N. Edison

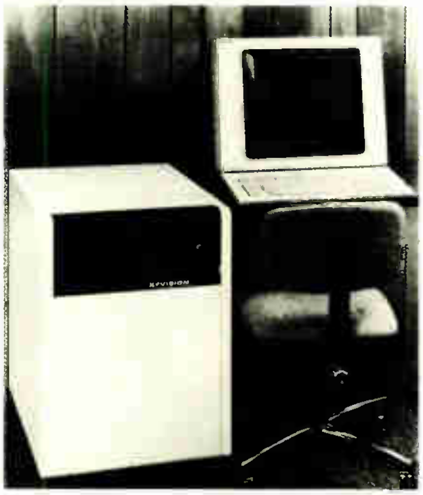
Way, Suite 4, Reno, Nev. 89502. Phone (702) 322-6868 [363]

Clustered publishing system aids editing, page composition

Offering a cluster approach to text editing and composition, the Xyvision can come with two types of terminals, one for text input and editing and the other for text and graphics display, plus a system control unit. Such a cluster can include up to 105 megabytes of hard-disk storage, and a larger system may be formed by linking up to 100 clusters with a local net like Ethernet.

Aimed at commercial and corporate publishing applications, the Xyvision system provides on-screen page makeup and background pagination processing. It will send the formatted data to automated typesetters over communications lines.

Text may be entered into the system with the Xytext editing terminal or over a serial-communications link with local or remote word processors, digitizing scanners, and other computer systems. The Xyview terminal shows complete page layouts or groups of pages, and the operator can edit, manipulate, and reformat pages or parts of pages on the screen.



Like the Xyview terminal, the Xycomp system control unit uses a 68000 processor. The 35-, 70-, or 105-megabyte hard disk is backed by a 1-megabyte drive using double-sided dual-density floppy diskettes.

A basic system composed of one of each of the Xytext, Xyview, and Xycomp components sells for $65,000. One Xycomp can support up to four Xytext and two Xyview units, which sell individually for $4,000 and $20,000, respectively. Deliveries will begin in May.

Xyvision Inc., 52 Cummings Park, Woburn, Mass. 01810. Phone (617) 938-8095 [364]

Plasma display is built to survive nuclear blast

Designed to withstand the adverse effects of radiation and electromagnetic pulses from a nuclear blast, the PD-3500RH terminal has a flat-panel plasma display. It meets the nuclear-hardness and maintenance standards of AFWL TR-76-147.

The terminal's high-contrast 8.55-by-8.55-in. screen combines with its 512-by-512-line resolution to permit the display of more than 4,000 characters. Microprocessor-controlled, it can display alphanumerics, point plots, and vector graphics.

The terminal's base price is $35,000; delivery takes 120 days.

Interstate Electronics Corp., 1001 E. Ball Rd., P. O. Box 3117, Anaheim, Calif. 92803. Phone (714) 635-7210 [365]

Multiuser microsystem family boosts memory, bus speed

A second generation of modular multiprocessor microsystems features four times the file-processor memory, double the bus-transfer rate, and twice the disk capacity of its predecessors. The Supermicro 64X and 32X serve up to 64 and 32 users, respectively, each with his or her own Z80A card with 64-K bytes of random-access memory.

These separately purchased processor cards are connected to a system bus running at 400-K bytes/s, a 100% speed improvement over the A series. The file processor in the X series is Z80B-based and comes with 256-K bytes of random-access memory; the A series file processor uses a Z80A and 64-K bytes of RAM.

The 32X has a 60-megabyte disk drive as standard equipment and can be expanded to a maximum capacity of 240 megabytes. A 136-megabyte drive is standard on the 64X, expandable to 272 megabytes.

Other improvements include extra capacity to handle the addition of Performance Accelerators. Each of these is a 8086 processor with up to 1 megabyte of RAM and is accessible by any user. Both the A and B series are compatible with CP/M and CP/M-86 application software.

The standard Supermicro 64X and 32X list for $22,995 and $18,995, respectively, and will be available in the second quarter. The company has also cut the price of the entry-level eight-user system in the A series by 25% to $5,995. X-series processor cards list for $995 each, and A-series processors have dropped from $995 to $695.

Molecular Computer, 251 River Oaks Parkway, San Jose, Calif. 95134. Phone (408) 262-2122 [366]

Terminal for APL programming offers extensive character set

As a multipage editing terminal for the APL programming language, the 16-APL can display 321 different elements from a variety of character sets, including 96 APL, 128 ASCII, 32 line-drawing, and 32 subscript and superscript characters, as well as 33 special symbols for math and other purposes. Also included with the

ANSI X3.64-compatible terminal are 64 manufacturer-defined mosaic characters for use in shading segments of the screen.

A four-page nonvolatile or volatile display memory is standard (expansion to eight pages is possible), but the page capacity can be increased by redefining logical line and page lengths. Unused portions of the display memory, if chosen to be nonvolatile, may be added to the standard 512-character function memory; this memory may be used for storing up to 32 variable-length programmable functions.

The 16-APL displays a 24-line-by-80-column page on its standard 12-in. screen—9- and 15-in. versions are also available. The screen's bottom line is used to display terminal status, feature selection, and computer messages. The available visual display attributes are dimming, blinking, underlining, reverse video, and blanking. The unit also has a built-in calculator and real-time clock.

Two buffered bidirectional RS-232-C ports are included with the 16-APL, which comes in four enclosure styles. Quantity discounts are offered from the list price of $1,695; delivery is in four to six weeks.

Research Inc., Teleray Division, Box 24064, Minneapolis, Minn. 55424. Phone (612) 941-3300 [368]

Low-end superminicomputer runs under version of Unix

For $49,950, the 3210 32-bit superminicomputer's price now includes the Edition VII Workbench version of the Unix operating system. The machine stands at the low end of the 32X0 family, all of whose members use Workbench. The 3210's price covers 512-K bytes of main memory, 64 megabytes of disk memory, a terminal, and eight communications lines.

Available immediately, the newly discounted package gives the user access to a large library of application software developed under Unix.

Perkin Elmer, Data Systems Group, 2 Crescent Pl., Oceanport, N. J. 07757. Phone (201) 870-4768 [367]

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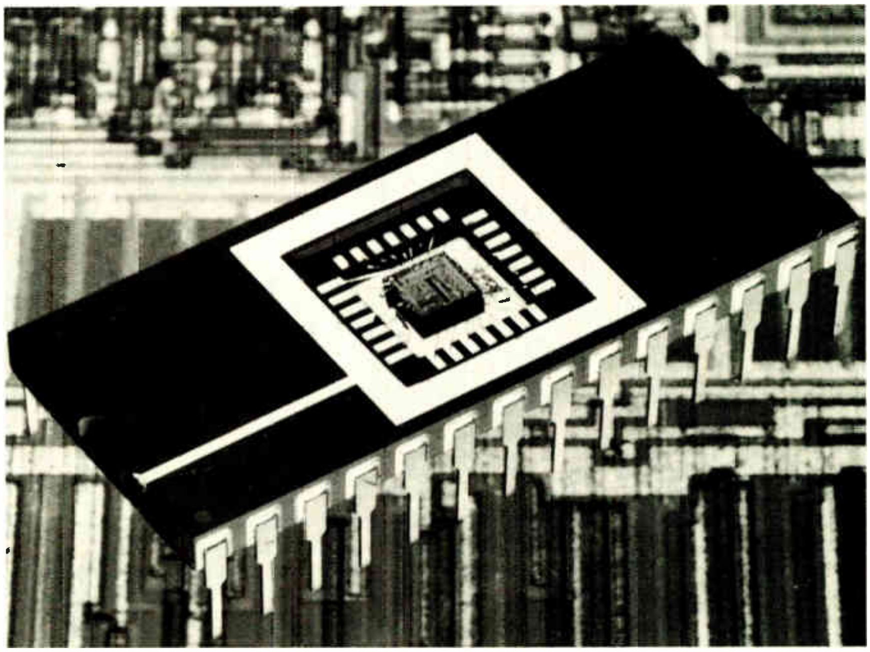
Circle 165 on reader service card

Data acquisition

10-bit converter runs on 112 mW

C-MOS analog-to-digital chip converts in 80 μs at most, indicates polarity of input



High speed and low power combine in Analog Devices Inc.'s AD7571, a complementary-MOS 10-bit-plus-sign analog-to-digital converter. Using successive-approximation techniques, the chip boasts a maximum conversion time of 80 μs, making it the fastest 10-bit C-MOS converter available, says product marketing manager David B. Fitzgerald.

Although monolithic bipolar parts and hybrids outrun the AD7571 with conversion speeds as low as 20 μs, those converters dissipate as much as 400 mW more, Fitzgerald notes. By contrast, the AD7571's typical and maximum power-dissipation levels are 50 and 112.5 mW, respectively.

The converter's combined TTL and C-MOS control logic lets it operate as a memory-mapped device interfaced with standard 8- and 16-bit microprocessors. The part includes an on-chip comparator that senses input polarities; it lets the AD7571 run as a unipolar or bipolar part, accepting differential analog inputs in a ±10-V range and requiring only a single external positive reference. With positive-only inputs, the AD7571 can run off a single power supply. The unit also has an on-chip clock, but can be run by an external clock as well.

One word or two. The AD7571 comes in six models that range in price from $19.50 to $83.85 in 100s. All have three pin-programmable output formats. Full parallel output suits the part for 16-bit microprocessors and most nonmicroprocessor applications; a double-byte output suits work with 8-bit microprocessors; and a serial output lets users add optical isolation for remote data-acquisition applications.

Depending on the model, the converter has a relative accuracy of ±1 or ±2 least significant bits. Two AD7571 models are available in each of three operating-temperature ranges: 0° to +70°C, –25° to +85°C; and –55° to +125°C. Over their full temperature range, the units offer a maximum gain error of either ±4 or ±5 LSB. Both gain and offset typically drift by no more than ±5 ppm/°C.

The AD7571 comes in a plastic or ceramic 28-pin dual in-line or Cerdip package. Small quantities and samples are available now. The two models with military temperature ranges will be available with processing to MIL-STD-883B sometime in the third quarter of 1983.

Analog Devices Inc., Rte. 1 Industrial Park, P. O. Box 280, Norwood, Mass. 02062. Phone (617) 329-4700 [381]

A-d converter for digital video supports 150-MHz update rates

Designed for color or monochromatic digital video systems, a hybrid 8-bit video digital-to-analog converter aims at improving the picture quality of raster-scan type displays.

Smaller, faster, and more accurate than its predecessors, according to the company, the AH8308E combines a large-scale integrated circuit with precision-made thick-film resistors deposited on its hybrid substrate. This setup gives it a better temperature stability and lower drift than was possible for its less integrated forerunners. In addition, the device can be used in high-speed, high-resolution digital applications where data is updated at rates as high as 150 MHz.

The AH8308E receives video data, along with timed blanking and synchronization digital commands, and generates the analog composite video signal internally. It has a 75-Ω source impedance and has sufficient analog output power to drive a 75-Ω cable or cable termination directly. No additional buffer amplifier or impedance-matching circuitry is necessary. Output level is 1 V when driving 75 Ω. The AH8308E does not require any external deglitching circuitry to eliminate noise caused by switching transients.

The d-a converter provides a standard 0.286-V sync signal, a 0.643-V video gray-scale range, and a pin-programmable setup of blanking level. For sharp line transitions, it has rise and fall times of 4 ns maximum.

Housed in a 0.87-by-1.37-in. 24-pin package, the AH8308E has a power dissipation of 1.2 W maximum. It is priced at $60 each in

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For further information, contact
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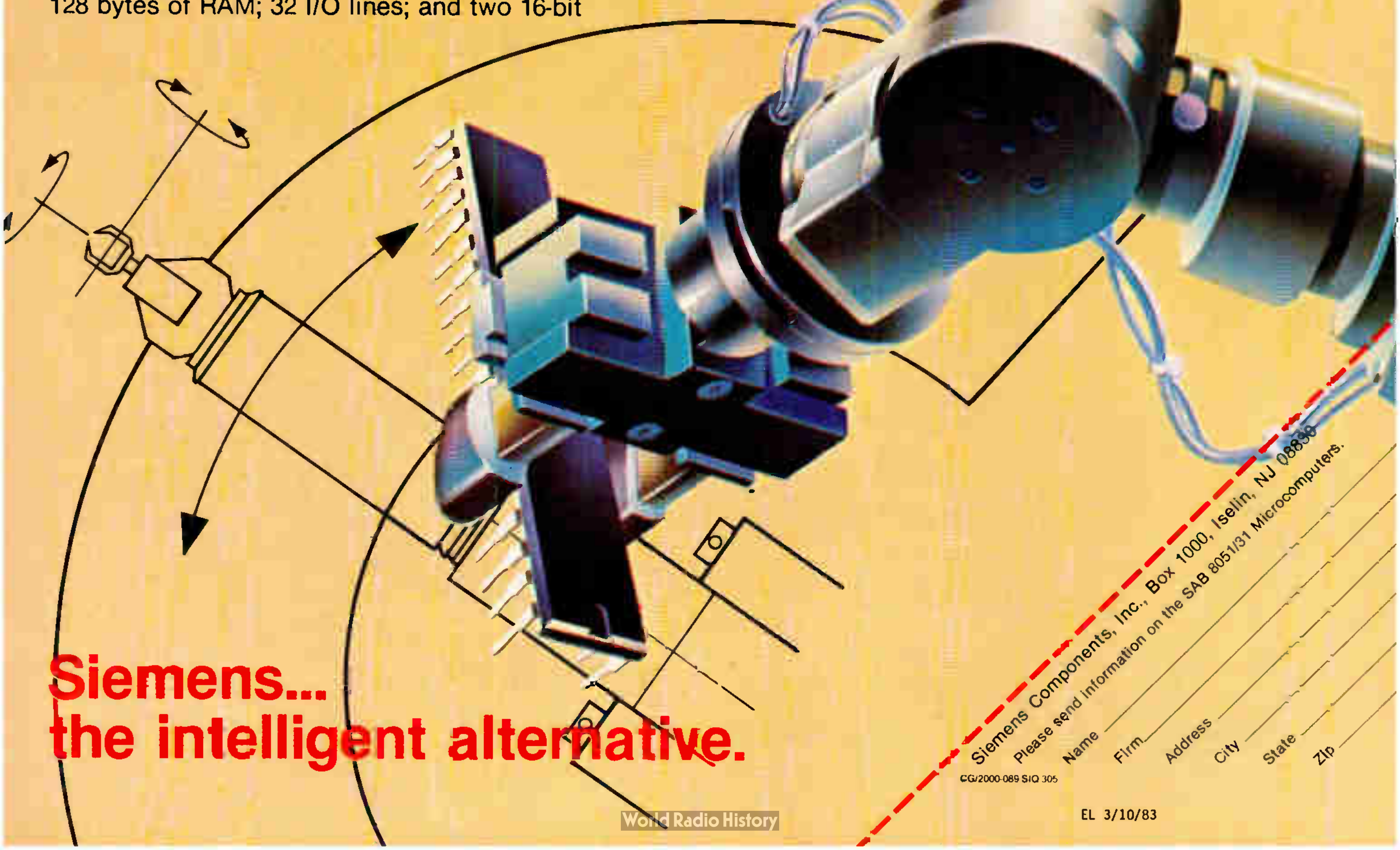
Iselin, NJ 08830.
(800) 222-2203.
(In Canada,
(514) 695-7300).



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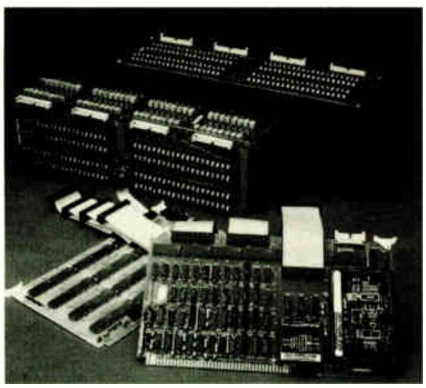
quantities of 100. Delivery takes three to four weeks.

Analogic Corp., Audubon Road, Wakefield, Mass. 01880. Phone (617) 246-0300 [383]

Multibus analog input boards offer up to 512 channels

The DT712 series Multibus-compatible analog input boards are designed to interface large numbers of analog input channels with computer-based systems. The basic boards may be supplemented by expansion boards to quadruple the capacity.

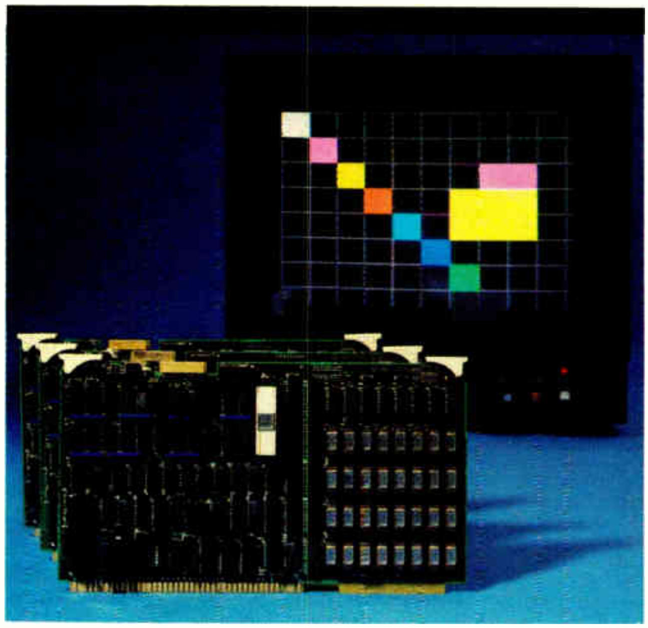
The 712 and 714 boards provide for up to 128 single-ended or 64 differential input channels on a single board. Each can be expanded with a



single 713 or 715 expansion board for up to 512 single-ended or 256 differential channels.

Connection of input signals to the 712 series is facilitated by the 705, a 5.25-in.–high screw terminal panel with terminals and ground connections for up to 128 single-ended or 64 differential inputs. A companion, the 706 passive signal-conditioning board plugs directly into the 705, thereby allowing the user to install filters, voltage dividers, and other passive circuits.

The entire family features 25-kHz analog-to-digital throughput rates with 12-bit resolution, jumper-selectable 20- or 16-bit input/output capabilities, and user-selectable 8- or 16-bit data transfers for compatibility with various Multibus processors. Other standard features include an on-board programmable clock, con-



trol for internal and external a-d triggering methods, and selection of sequential and random channel-scanning modes.

The DT712, with 128 single-ended or 64 differential channels, is priced at $1,495. With 64 differential channels, it sells for $1,595. The DT713, providing up to 384 single-ended or 192 differential channels, is $1,595, and the DT715, with 192 differential input channels, is $1,695. Delivery is from stock to 30 days.

Data Translation, 100 Locke Dr., Marlboro, Mass. 01752. Phone (617) 481-3700 [386]

Converter eliminates need for external voltage reference

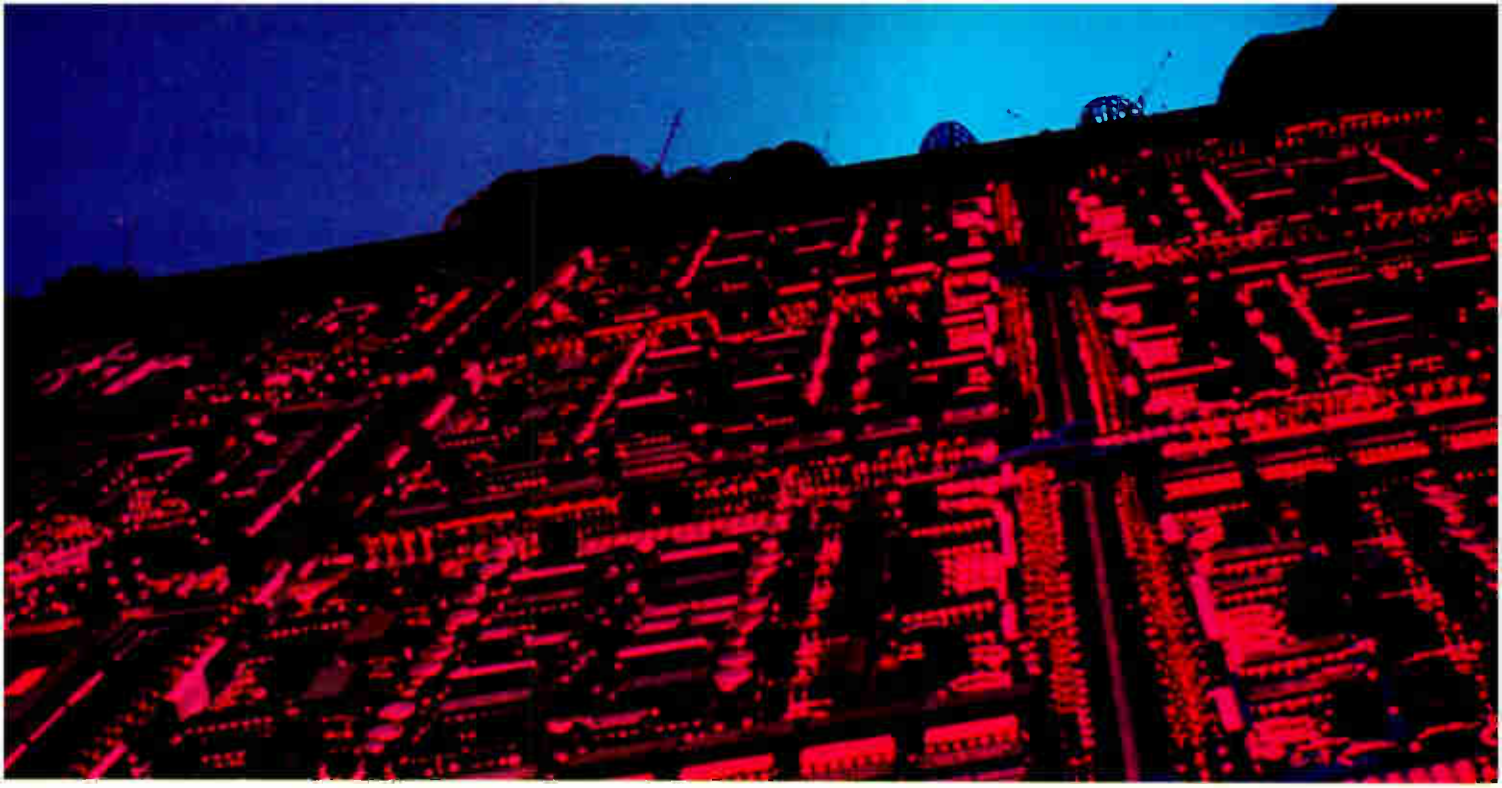
A single-chip 3½-digit complementary-MOS analog-to-digital converter incorporates internal oscillators, a zener-diode reference voltage circuit with a 20-ppm/°C typical temperature-drift coefficient, and segment and backplane drivers to drive a liquid-crystal display.

Designated the TSC7106A, it can achieve a 50-ppm/°C maximum drift

limit, which can eliminate the need for high-performance external voltage references. It improves the conventional two-phase dual-slope conversion technique with an automatic-zero cycle that corrects conversion errors induced by its offset voltage.

The converter has a 1-count maximum linearity error on the 200-mV-to-2,000-V full-scale range. Its high-impedance differential C-MOS analog input has a maximum leakage current of 1 pA typically and 10 pA maximum, which minimizes errors caused by high-output impedance sensors or RC filters at the input.

The TSC7106A has applications in



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thermometry, bridge readouts, digital panel meters and other instruments, power-supply readouts, and process monitors. In quantities of 100 to 999, the converter is priced at $9 in a 40-pin plastic dual in-line package and $21 in a Cerdip package. Delivery is from stock.

Teledyne Semiconductor, 1300 Terra Bella Ave., Mountain View, Calif. 94043. Phone (415) 968-9241 [384]

16-bit hybrid converter is accurate to ±0.0008%

A 16-bit successive-approximation analog-to-digital converter with 16-bit accuracy is now available for less than $100 in a 32-pin triple-width dual in-line package. Designated the HS9516, it contains a clock, reference, comparator, successive-approximation register, and a low-power 16-bit d-a converter.

The HS9516 has a conversion time of 100 μs for a full ±0.0008% accuracy. With a clock-control input, the conversion time can be decreased to 50 μs, cutting accuracy to ±0.003%.

The converter accepts analog unipolar inputs of 0 to +5, 0 to +10, 0 to +20 v, and bipolar voltages of ±2.5, ±5, and ±10 v. Output data is either parallel binary or in 2's complement form. In addition, the HS9516 has a power consumption of 900 mw, which is nominally 50% below other 16-bit hybrid a-d converters available, says the firm.

Three models, the HS9516-4, -5, and -6, have a linearity of 14, 15, and 16 bits, respectively. All models operate from 0° to 70°C. Deliveries are from stock to four weeks.

Hybrid Systems Corp., 22 Linnell Circle, Suburban Industrial Park, Billerica, Mass. 01821. Phone (617) 667-8700 [385]

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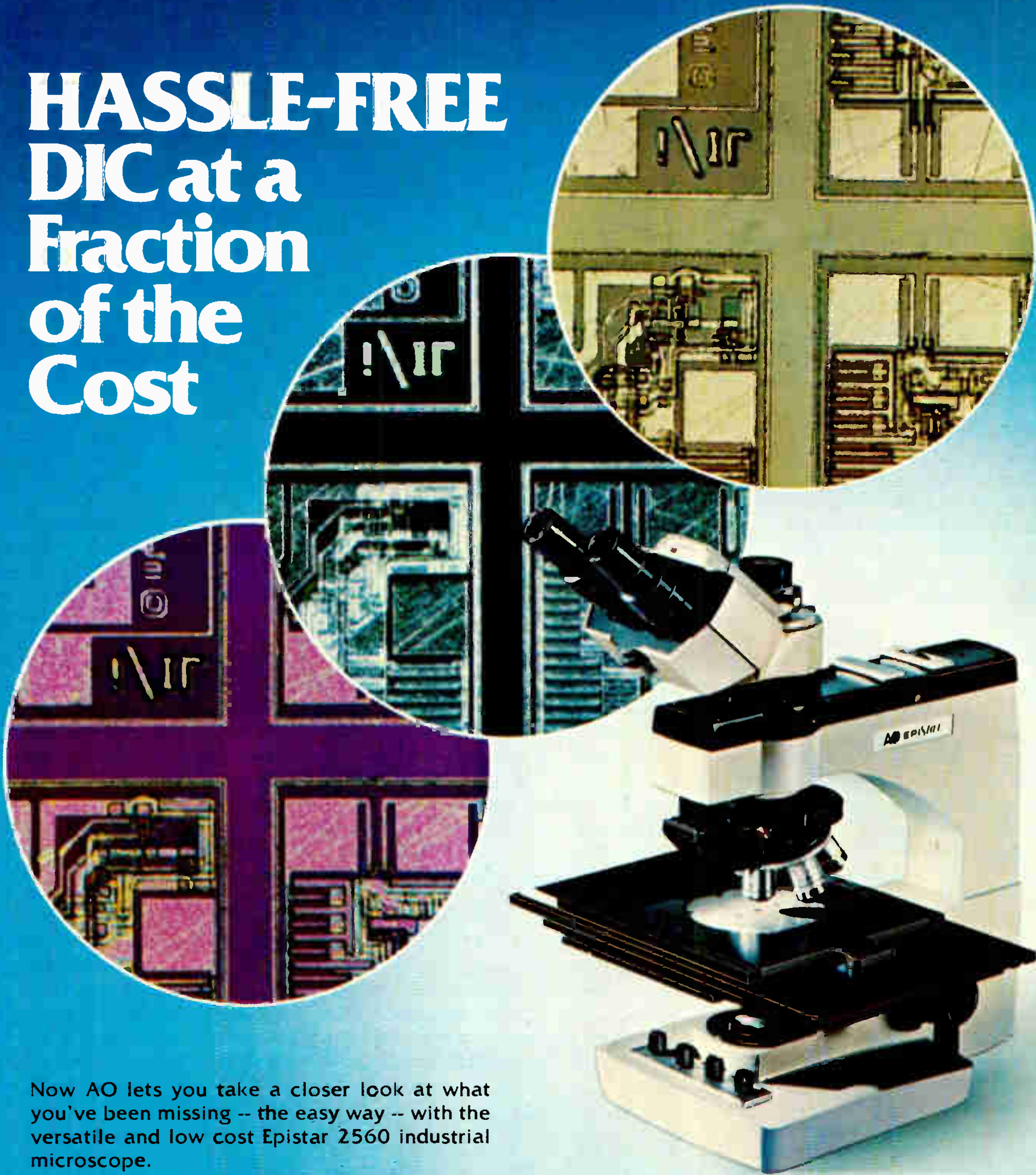

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Drafting system is only $24,000

Based on LSI-11/23, system includes terminal, digitizer, plotter, disks, and software

Andromeda Systems, which earns its keep by adding value to DEC LSI-11 computers, is bringing the LSI-11/23 into the computer-aided drafting arena with a low-cost but complete system called the A-CADS/1. With central processing unit, cathode-ray-tube terminal, disk drives, B-size plotter, digitizer, and software, the A-CADS/1 sells for $24,000—about a year's salary for a class B draftsman, the company points out.

The A-CADS/1 system, which is suited to preparing electrical schematics, piping and plant layouts, and flow charts, will handle a variety of predefined figures and symbols. Other figures and symbols the user may define by building on the library of basic graphic elements. The system also boasts extensive text-handling capability with eight fonts available in the basic software package; again, the user may create additional fonts or else buy them from the company.

Multilayered. Drawings are constructed from a full set of geometric primitives like solid lines, broken lines, arcs, circles, polygons, and ellipses, among others. These are assembled within the system's memory in a User Work Area (UWA), upon which the CRT acts as a window. Three-dimensional coordinates are maintained within the UWA for each point entered by the user, with a 32-bit integer holding the value of each axis coordinate. The system supports up to 16 layers within a particular drawing—for example, the layers of a printed-circuit-board layout. Each layer may be examined separately or overlaid to check for interference.

As drawings are constructed, including line work and text callouts, the system will store them in the Winchester disk or send them to the plotter for hard-copy output. Moreover, drawings can be transmitted over phone lines to another system, in effect making the A-CADS/1 a node on a network.

The system offers the engineer or draftsman a variety of graphic editing functions that allow him or her to delete, move, or manipulate defined areas of the UWA. Drawings may be scaled up or down, rotated, or relocated.

An original drawing is maintained unless specifically deleted in order to simplify recovery from mistakes made in modifying originals. A particularly useful feature is the ability to retrieve non-graphic data from drawings. Designers can extract part numbers from assembly drawings to create a bill of materials for the purchasing department, for instance.

Within the system card cage resides an LSI-11/23 CPU, 64-K bytes of random-access memory, five serial RS-232-C ports, a video-display controller, a floppy-disk and Winchester-disk–drive controller, and joystick interface, as well as several expansion slots. A 5-megabyte Winchester disk drive is included; a 512-K-byte floppy-disk drive provides removable-media storage.

Easy in. The input/output devices include the firm's VDT11-C monochrome graphics display terminal with a raster display whose resolution is 512 by 256 picture elements. The display terminal can emulate the Tektronix 4010 in the graphics mode and DEC's VT52 in the alphanumeric mode. A joystick is the primary input device for creating drawings.

Completing the hardware complement is a B-size plotter handling paper measuring 11 by 17 in. Under system controls, it can select up to eight pens for varying color or line width and an 11-by-11-in. digitizing pad with a four-button cursor. The pad may be used to digitize drawings or outlines from photographs, allowing existing documents to be entered into the computer drawing file.

To enable all the hardware to work together, Andromeda chose a version of the Design Graphix software package developed by Engineering Systems Corp. The software, which runs under DEC's RT-11 operating system, was modified to achieve performance criteria specified by Andromeda. The result is a highly interactive package, with the user able to view the graphic data on the CRT and enter commands and coordinates for image manipulation through a keyboard, joystick, or digitizing pad. Two software features aid users in mastering their system: a teaching program helps train users, and a help function lists available commands and options.

The system may be expanded with more main memory, larger plotters and digitizers, and extra software for multiuser and multitasking environments. Specific packages for producing electrical schematics, piping layouts, logic diagrams, and flow charts will be made available by the compa-

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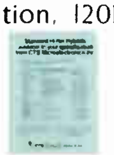
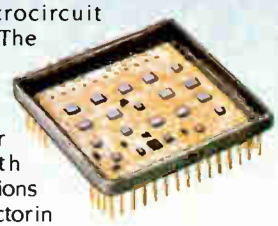


CIRCLE NO. 208

Advanced Air Force Communications System uses CTS Hi-Rel Hybrid

The prime contractor for the Air Force SEEK TALK anti-jam voice communication system selected a CTS Hi-Rel unit as a primary microcircuit component. The need for high reliability in this system linking fighter aircraft with command stations was a major factor in the selection of CTS.



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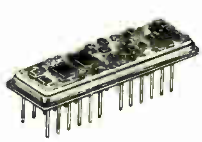

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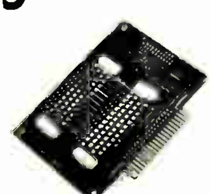

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ny. The $24,000 price tag includes one year of on-site support.
Andromeda Systems Inc., 9000 Eton Ave., Canoga Park, Calif. 91304. Phone (213) 709-7600 [351]

3-d graphics terminal aids plant designers

Plant designers now have available a three-dimensional graphics terminal that, using Plant Management Design System software, can help designers improve their designs and cut down on construction errors.

The Design Station One (DS1) allows complex plant views to appear in color and be interactively moved about, rescaled, and viewed from different directions. Designers can add and change piping components, with the DS1 ensuring that only legal components are used. The DS1 also ensures that pipe alignment is correct and that connections are precise.

Manufacturing drawings can be produced with the product as well. The work stations can be linked, allowing designers access to information about each other's efforts.

The PDMS software, able to handle a plant construction project from a single data base, is separately available on a time-sharing or licensing basis. PDMS can also be licensed by users of Prime 750 or 850 computers. One DS1 work station costs $89,000, with volume discounts available. Delivery is scheduled to begin in May.
Cadtrak Corp., 823 Kifer Rd., Sunnyvale, Calif. 94086. Phone (408) 730-2591 [355]

Mechanical-design stations are driven by Medusa software

Targeting computer-aided mechanical design environments, the Prime Workstation 200 series (PW200) is a family of CAD machines built around a 32-bit virtual memory processor and a 32-bit graphics processor. The series is driven by dedicated modules of Medusa, a software design system offering either two-dimensional design and drafting or three-dimensional modeling capabilities.

The PW200 graphics hardware consists of a 19-in. color monitor with 1,168-by-860–picture-element resolution, alpanumeric keyboard, data-entry tablet, and joystick for cursor manipulation. The graphics processor drives a display controller, which in turn supports six RS-232-C ports, four of which are dedicated.

The monitor can also serve as a system console. Text can be scrolled at the bottom of the screen or displayed over the full monitor.

One megabyte of memory is included with the virtual memory processor, accompanied by one sealed 68-megabyte hard disk and a 15-megabyte tape-cartridge drive for data backup and transport.

The work stations can be purchased with Primenet networking software, allowing commuications with any of the company's series 50 32-bit microcomputers. Prices for PW200 units vary from $61,000 to $100,000, depending on the software options desired. Deliveries are expected to begin in the third quarter.
Prime Computer Inc., Prime Park, Natick, Mass. 01760. Phone (617) 655-8000 [356]

Ethernet integrates stations into circuit-design office

With a ¾-megabyte random-access memory and a 40-megabyte Winchester disk, the Ethernet-based Logician computer-aided–engineering work station has facilities that assist

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NVRAM	52002	256 x 8	200/300
NVRAM	52001	128 x 8	200/300
NVRAM	52212	256 x 4	200/300
NVRAM	52210	64 x 4	200/300
*EEPROM	53004	512 x 8	300
*EEPROM	53002	256 x 8	300
*EEPROM	53001	128 x 8	300
EEPROM	52817	2K x 8	300/450
EEPROM	52832	4K x 8	300/450
*EEPROM	52864	8K x 8	300/450
EEPROM	52801	16 x 16	125KHZ (Serial)

*Future Products

Non-Volatile RAM (NVRAM) circuits combine high performance static RAM with electrically erasable PROM (EEPROM) on a single integrated circuit.

All NCR NVRAMs and EEPROMs are available in commercial, industrial, and military temperature ranges.

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The SNOS process and 10 years of semi-conductor experience have made NCR a leader today in NV memory devices. And tomorrow you can look forward to an even broader product line of high quality, reliable products with even higher densities and expanded features.

For more information on SNOS memory chips, call your local NCR Microelectronics representative. Or contact Dave Major at NCR Microelectronics Division, Box 606, Dayton, Ohio 45401. The toll-free number is (800) 543-5618. In Ohio call (513) 866-7217

NCR
Microelectronics Division

Circle 177 on reader service card

the designer from functional description through project simulation and certified design.

The work stations are built around an 8-MHz 8086 processor and a proprietary processor dedicated to graphics. A Unix-like operating system provides the environment for the Logician's design tools. In addition to a logic simulator, a timing verifier, and a stimulus or test-pattern generator, other tools included are: an interactive simulator that reduces overhead by simulating only the portions of a design that have been changed since the last simulation; a results comparator that compares output files of simulations for behavioral-, gate-, and functional-level descriptions and points out any differences; and a so-called virtual logic analyzer, which takes output from simulation programs and formats it as state or timing-waveform diagrams.

Compilers for Fortran 77, Pascal, and PL/M are included, as is data-base–access software. The list price of the Logician is $85,000; an Ethernet interface is an extra $5,000. A version of the Berkeley Spice simulation program optimized for the unit is another $3,000.

Daisy Systems Corp., 139 Kifer Court, Sunnyvale, Calif. 94086. Phone (408) 773-9111 [357]

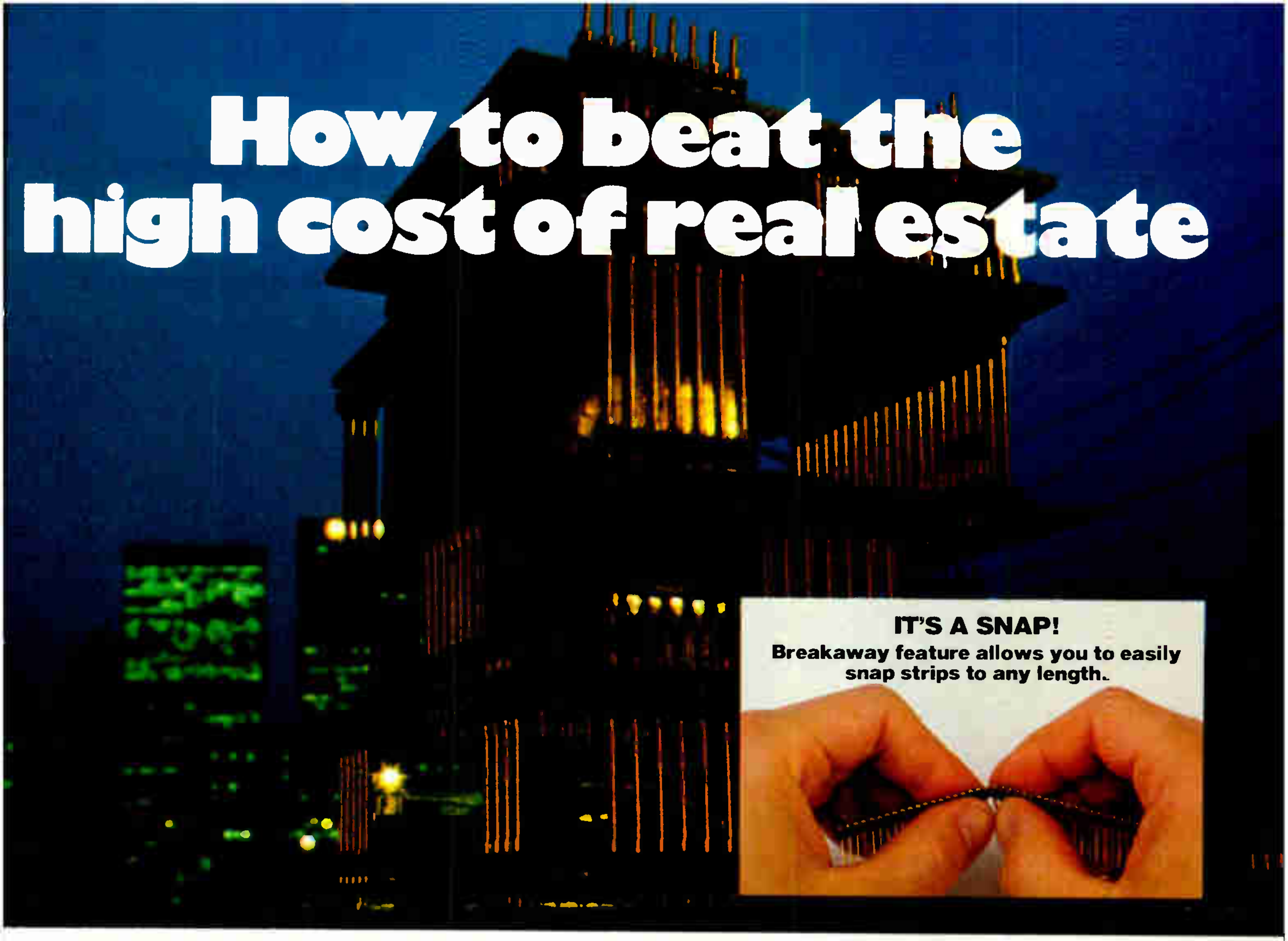
Giant-sized digitizers extend product line

Capable of being used with any Altek controller, two digitizers have been added to the firm's line of Datatab tables. The new digitizers, in 48-by-80-in. and 42-by-130-in. sizes, have an accuracy within 0.005 in. over distances of up to 2 ft and resolution and repeatability of ±0.001 in.

The units are available with an opaque surface; the free-cursor digitizers can be equipped with binary-coded decimal, ASCII, or EBCDIC output through an optional RS-232-C port. The 48-by-80-in. AC T48 lists for $11,000; the larger AC T413 is $14,000. Delivery is in 60 days.

Altek Corp., 2150 Industrial Pkwy., Silver Spring, Md. 20904 [358]

How to beat the high cost of real estate



Versatile Samtec Snap-Strip socket and terminal strips save valuable on-board & between-board space.

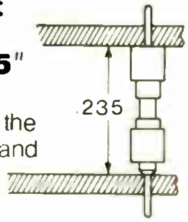
1 Fit where other sockets or connectors won't.

Compact, low-profile Snap-Strips are side and end stackable, allowing maximum space utilization and interconnection flexibility. Used in sets, they're mating connectors.

2 Accept just about anything.

There's a Snap-Strip socket to accommodate all standard or "odd-ball" components, jumpers, connectors, plugs and terminals . . . round or square pins. Now you can place connections and components where you need them.

3 Interconnect and stack boards from .235" to 1." spacing.



Mating Snap-Strips are the perfect way to connect and stand-off stacked p.c. boards.

4 Even more flexibility.

Snap-Strips are available in several lead sizes, shell styles, and a wide variety of termination and mounting styles. Gold, selective gold or tin plating. May be polarized for positive orientation.

5 Lower cost-per-pin... better inventory control.

One strip can replace fifteen discrete socket or terminal sizes. One mating set can replace many more connector sizes.

6 All this PLUS highest reliability.

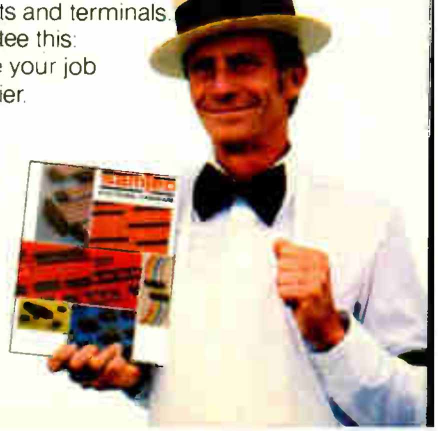
Tapered entry for easy lead insertion.

Four finger closed entry beryllium copper inner contact for low contact resistance and high lead retention.

Sealed base prevents solder or solvent from wicking up.

GET THE SPECS

Let me send you our complete Snap Strip catalog containing literally *thousands* of variations of sockets and terminals. I guarantee this: It'll make your job a lot easier.



samtec

ELECTRONIC HARDWARE

810 PROGRESS BOULEVARD, NEW ALBANY, INDIANA 47150 (812) 944-6733

Circle 179 on reader service card

Components

C-MOS filter cuts parts count

Two low-pass switched-capacitor filters fit on chip suited to use in high-performance modems

A dual low-pass linear-phase switched-capacitor filter chip has been fabricated using Motorola's low-power complementary-MOS processing technology. Targeted at high-speed modems and a number of synthetic-speech applications, the 16-pin device contains two five-pole filters, one with a gain of 18 dB at dc and the other with unity gain. The chip also features two uncommitted comparators for signal-limiting and -sensing functions.

The MC145415 has on-chip digital clocking circuitry, which allows low-pass break frequencies to be tuned by an external clock. No other external components are needed to tune the filter, which sits on a 14,800-mil² die.

With a 153.6-kHz clock, for instance, the part will have a 3-dB rolloff frequency of 2,400 Hz. The cutoff frequency scales with the clock in a linear fashion. The maximum idle-channel noise for filters is expected to be better than 24 dBrnC. Gain tracking is better than ±0.3 dB. Both filters on the chip have the same response curves, according to the firm; preliminary data puts the 300-Hz response at ±0.6 dB.

Housed in a ceramic dual in-line package, the filter is priced at $7.90 each in lots of 100. In plastic, the device sells for $6.42 each. Volume deliveries are to begin next month.

Split supplies. The 145415 uses a power supply that can range from 4.5 to 16 V. In addition, the chip can be wired to operate using split power supplies such as +5 and –5 V. It operates at from –40° to 85°C.

One of the 16 pins can be tied to a voltage that defines the lower level of the clock input (the upper level is set by the power supply). This eliminates the expense of external level-shifting components otherwise needed to adapt the integrated circuit to use with different logic types. In many high-performance modem designs, the filter can replace as many as five ICs as well as a number of capacitors and resistors, according to the company. The firm also expects the filter device to make its way into a number of military and industrial-control designs.

Motorola Inc., 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 928-6506 [341]

LED lamps with 2-mcd luminous intensity use 2 mA

High-efficiency light-emitting-diode lamps of the HLMP line are compatible with both complementary-MOS and TTL and run on just 2 mA, qualities that make them suitable for battery-powered products. The red and yellow lamps come in T1¾, T1, and subminiature packages.

The LEDs have a luminous intensity of 2 mcd and a low forward voltage. Since the red lamps have a 2.2-V maximum requirement, two can be driven in series from a 5-V supply.

At moderate currents, like 5 mA, the lamps are from two to five times as bright as a standard LED operating at 10 mA. In lots of 5,000, the red (HLMP-4700) and the yellow (HLMP-4719) lamps in T1¾ packages are priced at 41¢ each. The T1 yellow lamp (HLMP-1719) and red lamp (HLMP-1700) go for 38¢ each. In subminiature packages both the red (HLMP-7000) and the yellow (HLMP-7019) are each priced at 31¢. All are available now.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [343]

LCD module displays text, accepts ASCII-coded input

Two models of alphanumeric ASCII-input liquid-crystal displays with a small footprint—new members of the Daystar line—can be read in sunlight, are portable, need little power, and interface easily. The models display one line of 40 characters in either a five-by-seven–dot matrix plus cursor (model 3802-06-040) or a 5-by-10–dot matrix plus cursor (model 3802-07-040).

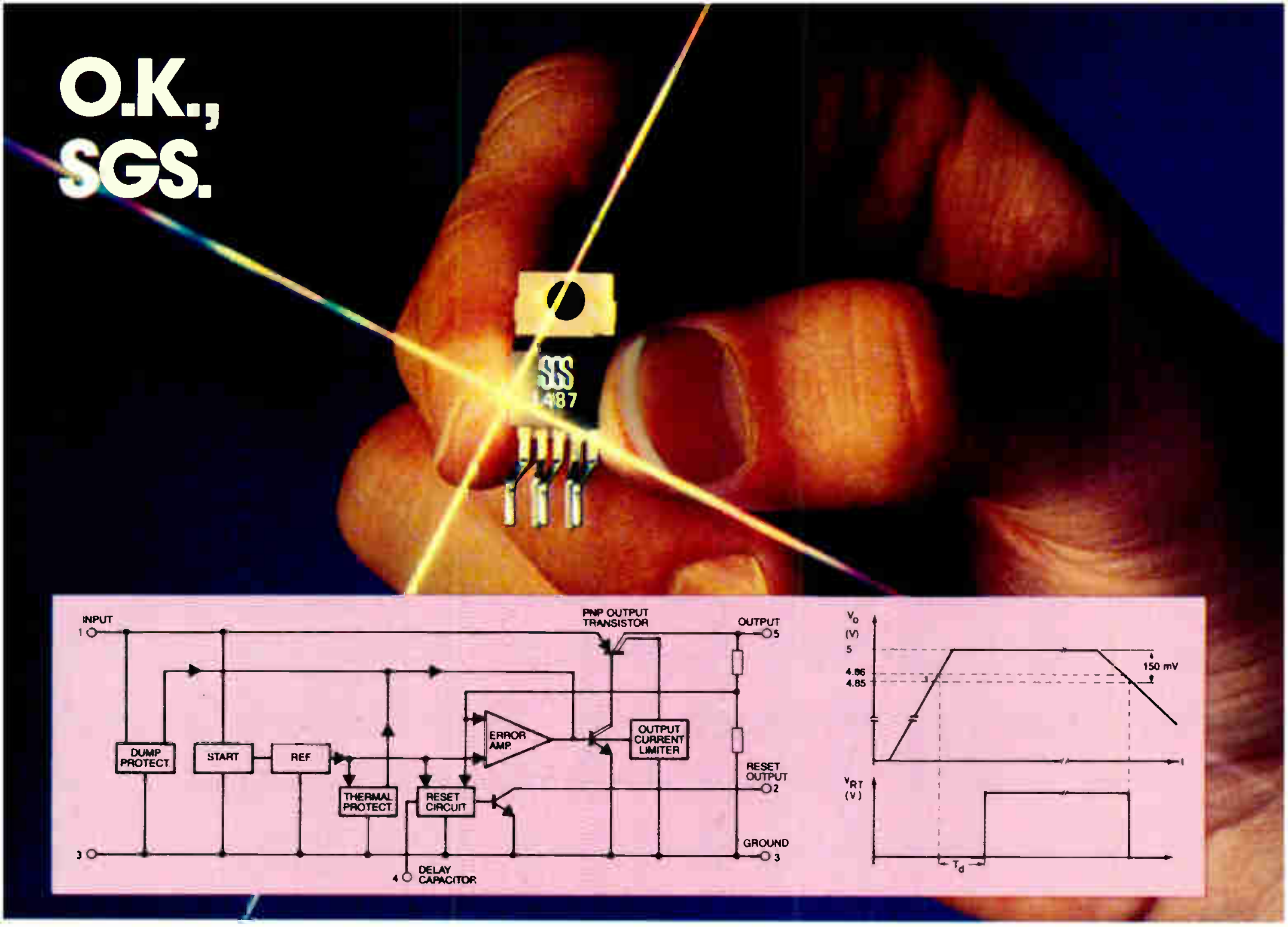
The five-by-seven–dot model can display the full 96-character font; the 5-by-10 matrix can, in addition, display true descenders on the lower-case letters. The modules, which consist of the display panel plus integrated drive and control electronics, employ complementary-MOS for the character-data random-access memory, character-generator read-only memory, and the scanning refresh and multiplexed-drive electronics. This circuitry provides an 8-bit parallel interface in a small package.

Engineers need only provide ASCII data and a single +5-V supply to operate the display. Prices start at $107 in 100-piece quantities. Delivery takes up to six weeks.

Industrial Electronic Engineers Inc., 7740 Lemona Ave., Van Nuys, Calif. 91405. Phone (213) 787-0311 [345]

Breakout box for RS-232-C interfaces sells for $38 or less

Called by its maker a poor man's breakout box, the model 51 Mini-Patch box sells for just $37.95 in unit quantities and gives users of RS-232-C interfaces the ability to reconfigure



Tell me how a voltage regulator can keep an MPU from going down for the count.

The L487 is a very low drop 5V/.5A voltage regulator designed to supply a variety of systems. It could be the missing link in your MPU-based products. That is because this Pentawatt® packaged device provides a stabilized supply voltage, plus a reset function from a single chip. The reset circuitry guarantees that when the microprocessor's operating voltage falls below minimum specifications, a signal is available to reset the unit.

Unlike most reset circuits, the L487's reset signal is directly dependent on the supply voltage. That means the L487 is capable of continually assessing supply voltage to insure that a supply voltage is present and has been present for a specific time as controlled by your circuit's delay capacitor.

In addition, the L487 operates with an input-output voltage differential as low as 600mV to provide reduced power dissipation and increase total system efficiency.

Complete Range of Protection Features
The L487 provides circuitry for high voltage positive (+80V) and negative (−80V) transient protection. Reverse voltage and thermal protections are also incorporated in the device.

The L387 Very Low Drop Voltage Regulator
The SGS L387 voltage regulator with reset function may be used in place of the L487 for applications not requiring high voltage transient protection.

In addition to the L487 and L387, SGS offers a complete line of industry standard and special voltage regulators designed to cover a broad range of applications.

ELECTRICAL CHARACTERISTICS			
Characteristic	MIN	TYP	MAX
V_i Forward input voltage			30 V
V_i Reverse input voltage			−18 V
Transient peak input voltage			±80 V
V_O output voltage	4.80 V		5.20 V
V_i-V_O dropout voltage (I_O = 500 mA)		0.6 V	
Output current		500 mA	

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Circle 180 on reader service card

the connections or signal paths. The model 51 is equipped with a male and a female 25-pin connector, allowing the placement of the box in series with any RS-232-C cable path.

Of the 25 pins, pin 1 (frame ground) and pin 7 (signal ground) are carried through from the male to the female connector. The remaining 23 signals from each connector terminate on female jack receptacles. Supplied with 25 jumper plugs, the interconnections are patched by the user; for those applications where many signals must be patched together, the Mini-Patch box provides two busing areas where multiple signals may be connected together.

All patch jacks are clearly marked on the plastic enclosure, which measures 2.125 by 2.250 by 0.625 in. In lots of 100, the price of the model 51 breakout box drops to $29. It is available from stock.

Remark Datacom Inc., 4 Sycamore Dr., Woodbury, N. Y. 11797. Phone (516) 367-3806 [348]

Color graphics monitor has 0.31-mm–pitch dot matrix

A high-resolution 20-in. color cathode-ray-tube monitor uses self-convergence, in-line technology, and a 0.31-mm–pitch dot matrix to produce sharp, accurately registered colors. Compatible with TTL, the CD-2053D (made by Hitachi and sold through a U. S. sales organization) displays seven colors: red, green, blue, yellow, magenta, cyan, and white.

The recommended display density is 3,040 characters in a seven-by-nine–dot pattern. For text processing, this works out to 38 lines, each containing 80 characters. Horizontal sweep frequency is specified at 24.2 kHz, vertical at 54 Hz. The monitor consumes a maximum of 150 W.

Built-in circuitry includes a video amplifier, horizontal and vertical deflection circuits, high voltage supply, power supply with voltage regulator, high-voltage limiting circuit, and automatic degaussing circuit. The CRT's chassis, which measures 20 by

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Coatings are clear for component identification and all provide excellent electrical insulation and resistance to moisture and fungus. Products protected with the coatings can still be repaired, reworked, and resprayed.

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Circle 183 on reader service card

18 by 19 in., has sufficient space for additional logic boards. In lots of 1,000, the monitor sells for $1,200.

Nissei Sangyo America Ltd., 40 Washington St., Wellesley Hills, Mass. 02181. Phone (617) 237-9643 [347]

Opto-isolators withstand 4,000 V rms for 1 minute

The members of a family of opto-isolators that features dependable isolation and high current-transfer ratio contain a high-efficiency gallium arsenide light-emitting-diode source coupled to an npn silicon phototransistor. The CK2200 series is targeted at coupling and isolation circuits.

CK2200 series opto-isolators are mounted in a six-pin dual in-line package. Transparent silicon resin provides strong interface adhesion, and interface reflectivity is improved by the white epoxy case. The devices boast a minimum isolation rating of 4,000 V root mean square for 60-s intervals with typical coupling efficiencies of 200%.

In lots of 1,000, the isolators range in price from 56¢ to 73¢ each, depending on the operating characteristics required. Delivery is from stock.

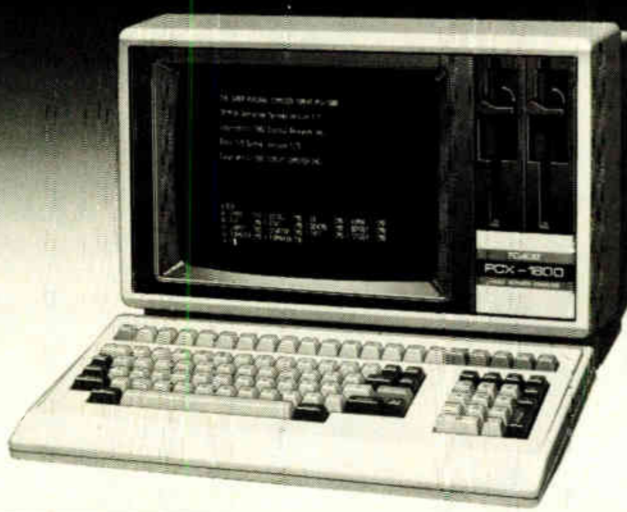
Raytheon Co., Industrial Components Operation, 465 Centre St., Quincy, Mass. 02169 [344]

Buffer keeps peace between CRT controller, processor

Made from the firm's Coplamos technology, the CRT 9212 double-row buffer, an n-channel silicon-gate MOS device, enhances microprocessor throughput in cathode-ray-tube terminals by eliminating memory contention between a CRT display controller and the system microprocessor. The CRT 9212 appears to the host system as two variable-length octal shift registers of up to 135 bytes each. The apparent shift-register length depends on the system needs and is changed dynamically.

Each buffer consists of a 1,080-bit random-access memory, address

Introducing the TOMCAT Family of Super Small Computers



Super personal computer TOMCAT PCX 1600/1800

Taking a step towards the new generation of personal computers, the TOMCAT PCX series offers the flexibility of both the 8-bit and 16-bit CPU. Ideal for a wide range of needs — form personal to business network — the user can select from the complete software library available under CP/M®, CP/M-86®, and MS-DOS®.

- Operating system — MS-DOS®, CP/M-86®, CP/M®
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- IBM software compatibility.

TOMCAT Model 1600

• 16-bit with quick access • Super low cost • IBM compatibility (CP/M)

TOMCAT Model 1800

• Both 8-bit and 16-bit CPU • 8-bit CPU for personal computer software • Graphic capability

TOMCAT Model 3000

• Multibus system • A wide range of network capability • Up to 16 terminals controllable • Designed for technical and business uses

SPECIFICATIONS

	1600	1800	3000
CPU	8086	8086, Z80A	8086, Z80A
PROM	16KB	24KB	16KB
RAM	128KB—384KB	192KB—448KB	128KB—1MB
Display	12-inch CRT monitor (80 chs × 25 lines)	12-inch CRT monitor (640 dots × 400 lines graphics)	14-inch CRT color monitor with color graphics capability 8 colors
Disk Drive	5¼-inch double-sided, double-density floppy disk × 2	5¼-inch double-sided, double-density floppy disk × 2	5¼ or 8-inch floppy disc or hard disk Hard disk capacity: 5—27MB
Operating Systems	CP/M-86®, MS-DOS®	CP/M®, CP/M-86®, MS-DOS®	CP/M®, CP/M-86®, MS-DOS®

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Dowa Bldg. 5-10-5 Shinbashi, Minato-ku, Tokyo, Japan TELEX: J32475 MIPOWER FAXNO.: (03) 434-3690 PHONE: (03) 433-4433

Circle 185 on reader service card

 Circle 186 on reader service card

counter, and data latches. The CRT 9212 has switching logic to toggle from one buffer to the other at alternating data rows, so the two buffers can share one 8-bit output path.

One of the device's buffers may be loaded at the same time as data in the other buffer is being read by the display. The actual loading of the write buffer may occur during any of the scan-line times that data is read from the read buffer. This very relaxed time constraint lets the processor handle, during a single video scan line, various priority interrupts.

The CRT 9212 may be used with any popular CRT controller. It is available in both ceramic and plastic 24-pin dual in-line packages. In orders of 100 pieces, the plastic-packaged version sells for $17.75.

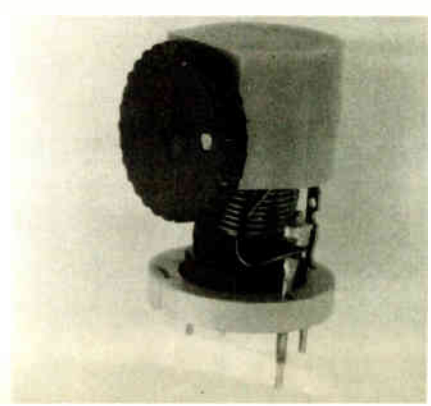
Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, N. Y. 11788. Phone (516) 273-3100 [349]

Variable-linearity coil is useful in CRT displays

A series of variable-linearity coils designated 3508 through 3512, for use in high-resolution computer terminals, offers operation at up to 65 kHz. The coils can be adjusted by hand with a rotating magnet to compensate for tolerances of materials manufactured in a standard way and to provide improved linearity in cathode-ray-tube displays.

The coils meet all Underwriters Laboratories' 94 V-2 nonflammability requirements and use a circle of printed-circuit-board space 0.8 in. in diameter. The firm can customize the coils to meet specific needs. Standard coils are available from stock for under $1 in volume.

Prem Magnetics Inc., 3521 North Chapel Hill Rd., McHenry, Ill. 60050 [346]



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Because the TypeMaster is much more efficient than ordinary electric typewriters, we estimate that it can pay for itself in a year... or less. For example, while one document is printing out, your secretary can be typing another on the screen. So work gets done faster, and there's time to handle other jobs.

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After using the TypeMaster for a few weeks, you'll see how it gets your typing back faster, looking better and right the first time. You'll also see how responsive we are in training, service and support. With all this in mind, we think you'll want to keep the TypeMaster.

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Communications

'Etherbox' eases ties to local net

Plug-in unit connects computers with 8-bit parallel port and handshaking into Ethernet loops

When Henry Ford introduced his Model A, he brought to the motoring public a mass-producible car with a built-in self-starter. The driver no longer had to get out and turn the crank and so could get on the road with a minimum of fuss. 3Com Corp.'s Etherbox Model A is likewise a fuss remover: it allows the owner of any computer system with an 8-bit parallel port with handshaking capability to link up with an Ethernet local network.

Once the input and output connections to the box are made, it need only be plugged into an ac outlet. Both transceiver and controller functions are handled by the unit.

The Model A complies with Version 1.0 of the Digital-Intel-Xerox Ethernet specification and implements the physical and data-link layers of the International Standards Organization's seven-layer reference model for open-system interconnection. It is built around a very large-scale integrated Ethernet chip [*Electronics*, Oct. 6, 1982, p. 89]. The box has its own power supply and a Manchester encoder-decoder in addition to the Ethernet transceiver.

No programming or modification of the Etherbox is necessary. Indeed, the box has no on-board intelligence, being managed by the host system. For example, the Etherbox must be initialized by its host so that it detects packets sent to an individual station address, packets with broadcast and multicast addresses, or combinations of the two. To do this, control registers set by the host system determine the types of packets that will cause interrupts when they are received.

The Etherbox contains 6-K bytes of memory for packet buffering. A single 2-K-byte transmit buffer can accommodate the maximum-sized Ethernet packet. The two receive buffers are also 2-K bytes in size. These two receive buffers make it possible to receive back-to-back packets separated by the minimum packet spacing.

The parallel-port interface on the Model A Etherbox contains eight bidirectional data lines and one parity line. It is entirely controlled by the host computer system, with the timing of data input and output operations set by host-generated strobes. In addition to the nine-line data bus, there are five control and timing signals. Two output lines (from the host system to the Etherbox) control the data-bus direction and indicate whether packet data or Etherbox command or status information is being transferred. A host-generated strobe controls the timing of data transfers.

The maximum data-transfer rate across the parallel port interface is 2 Mb/s for reading and 3 Mb/s for writing. This is accomplished through a standard 25-pin D-type connector with TTL voltages. The Model A is 2.5 by 8.5 by 17 in. and consumes 30 W maximum. It is designed to operate at temperatures from 0° to 55°C and at a humidity of 5% to 95% (noncondensing).

Etherbox is priced at $995 in single units; quantity discounts of up to 45% are available to original-equipment manufacturers. Prototypes are available now, and volume shipments are to begin in April.

System integrators should also inquire about other connections to Ethernet. For example, an Etherbox to connect gear based on an IEEE-488 bus to an Ethernet is under preliminary consideration.

3COM Corp., 1390 Shorebird Way, Mountain View, Calif. 94043. Phone (415) 961-9602 [401]

VLSI chip pair interfaces nets

Single-board package handles both baseband and broadband systems

The two very large-scale integrated circuits developed jointly by Ungermann-Bass Inc. and Fujitsu Ltd. [*Electronics*, Oct. 6, 1982, p. 101] have been packaged in a network interface unit (NIU) marketed at half the price of its less integrated predecessor. The Ungermann-Bass NIU-150 is a functional replacement for the company's model 1 NIU.

Both network interface units have six ports for attachment of a variety of devices to baseband (Ethernet), broadband (CATV), or hybrid local networks. The model 1 has three printed-circuit boards and is priced at $5,575; the NIU-150 is packaged on a single board, with no cooling fan necessary, and sells for $2,800. Both prices include a $700 input/output interface on a cable-connected daughterboard.

The chip set for the NIU 150 consists of an MB502 full-duplex codec that implements level 1, the physical link, of the International Standards Organization open-systems network standard and an MB61301 controller that is based on Ungermann-Bass's existing Ethernet controller (ISO level 2). The Ethernet interface also conforms to the standard adopted by committee 802 of the Institute of Electrical and Electronics Engineers and leaves buffering instructions to the system implementer.

The NIU contains 64-K bytes of random-access memory and a Z80 processor with a number of optional interfaces. It supports RS-232-C, RS-449, IEEE-488, high-speed serial V.35, 8- and 32-bit parallel, and Digital Equipment Corp. W-DR11-W/B interfaces.

The model 1 is already being put to use by Hewlett-Packard Co. in its 32-bit series 9000 engineering work station. Ungermann-Bass also markets an expandable version of the NIU, the model 2, that can accommodate six boards and 24 users. The company says that the chip set will be integrated into the model 2 sometime this year. The chips alone are available in sample quantities from Fujitsu.

Ungermann-Bass Inc., 2560 Mission College Blvd., Santa Clara, Calif., 95959. Phone (408) 496-0111 [402]

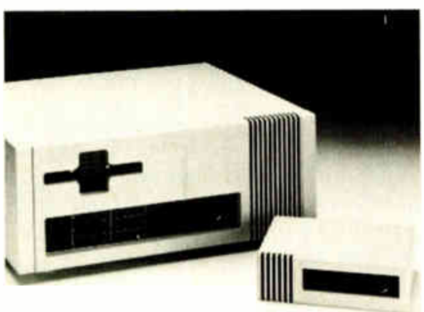
Interface builds networks out of units with dissimilar protocols

With the Netway family of network building blocks, original-equipment manufacturers can create flexible information systems with multiple dissimilar hosts and work stations regardless of the local or remote protocols employed. The Netway family supports any RS-232-C– or RS-422–compatible work-station device, including display terminals, personal computers, word processors, and teleprinters.

The multitasking, multiprogramming communications operating system called NCOS provides work-station and host transparency, can easily be extended and configured, has a friendly interface with help messages, and allows the CP/M Plus operating system to run as a task for application-program development.

The family is based on the Netway 200 communications processor, which provides remote and local networking facilities for up to 32 work stations and host ports. The Netway 50 local network interface handles connections to devices up to two miles away from the processor. The Netway 200 is priced at $6,800 and the 50 is $200.

Also part of the family are the Netway 100 device interface processor and the Netway 150 network interface processor. The device interface processor, which sells for $420, provides terminal emulation and presentation services. It is downloaded from a Netway 200. The 150 is a remote connection for a Netway local network. Its architecture includes elements of the 100 and 50. It also sells for $420. All products will be available in the second quarter.



Tri-Datam, 505 East Middlefield Rd., Mountain View, Calif. 94043. Phone (415) 969-3700 [403]

Smart data switch handles as many as 92 subscribers

Priced at only $5,500, Dataswitch model 9001-2, an intelligent switching system, performs prioritized queuing, keeps security passwords, and does automatic record keeping and recording of system statistics for management guidance. The model 9001-2 is intended as an entry-level switch—it may be used with two or more minicomputers and by 23 to 92 subscribers in a system.

The basic system, which operates in an asynchronous mode only, consists of a table-top rack-wide cabinet 28 in. high along with all the necessary hardware. Through software, the system may be configured for the number of subscribers involved. Features include speeds of up to 19.2 kb/s and automatic-calling-unit support, among others.

The Dataswitch controls and coordinates all ports, integrates dial-up and dedicated-access approaches, and permits nonbiased use by operating on a first-come, first-served basis. It is available now.

Develcon Electronics Inc., 4037 Swamp Rd., Doylestown, Pa. 18901. Phone (215) 348-1900 [404]

Converters put ASCII devices in touch with IBM computers

A pair of protocol-conversion units permits ASCII terminals to communicate via the X.25 public packet network with devices that use the Systems Network Architecture/Synchronous Data Link Control protocol.

Each converter consists of a pair of interfaces that allow microcomputers, personal computers, ASCII terminals, hard-copy keyboard-printers and other ASCII devices to communicate with an IBM 3270 host or to replace the 5251 models 11 and 12 terminals and 5256 printers in the IBM System 34 and 38 computers.

The 1051X acts as an interface between an ASCII terminal and an X.25 node and provides the ASCII–to–SNA-SDLC–to–X.25 conversion. The second part of the converter, the 73SX, performs the SNA-SDLC to X.25 conversion on the System 34 or System 38 host side of the network. Likewise, the 1076X and 73SX team up to provide the links between the X.25 network node and the ASCII terminals and between the X.25 and the 3270 host, respectively.

Each interface set permits up to 56 ASCII devices to operate simultaneously through the X.25 network. Both the 1015X and 1076X carry price tags of $4,500 for the one-port model and $8,500 for seven ports. Models with three and five ports are also available. The 73SX, which serves both conversion systems, sells for $5,500.

Protocol Computers Inc., 6150 Canoga Ave., Woodland Hills, Calif. 91367. Phone (800) 423-5904 [405]

Concentrator accepts mixed protocols at up to 9.6 kb/s

The 792 network concentrator adds to its maker's family a low-end model that can be used in multinode communications networks and in simple point-to-point statistical multiplexing applications. The 792's output link or links may operate at speeds as high as 72 kb/s.

The concentrator is end-to-end–compatible with the existing 790 and with Supermux 480, 680, and 780 statistical multiplexers. The inputs may be any combination of synchronous and asynchronous, dial-up and dedicated at mixed speeds (to

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Manufacturer	Device	Access Time	Operating Current	Standby Current
RCA	CDM6116-1	250 ns	35 mA	100 μA
RCA	CDM6116-2	200 ns	35 mA	30 μA
Hitachi	HM6116P4	200 ns	70 mA	2,000 μA
Hitachi	HM6116LP4	200ns	60 mA	100 μA
Toshiba	TC5517AP	250 ns	70 mA	30 μA
Fujitsu	MB8416	200 ns	60 mA	10 μA

RCA Solid State headquarters: Somerville, NJ. Brussels. Paris. London. Hamburg. Sao Paulo. Hong Kong. **Circle 191 on Reader Service Card**

The new RCA CDM6116 RAMs offer lower operating current than today's best-sellers.

9.6 kb/s) and protocols. The unit accommodates such binary synchronous protocols as IBM's BiSync, Honeywell's GERTZ, and CDC's UT-200. The concentrator is said to be able to handle new protocols as they come into being.

Switching and contention capabilities, which are optional, let users select and contend for ports on any local computer. Any asynchronous terminal or computer port may be connected to any other compatible terminal or computer port without human intervention. Available in 90 days, the 792 concentrator is priced starting at $4,500.

Infotron Systems Corp., Cherry Hill Industrial Center, Cherry Hill, N. J. 08003. Phone (800) 257-8352 [406]

Audio-video modulator serves master-antenna TV

Employing a surface-acoustic-wave filter for optimum adjacent-channel filtering and performance, the CDM 1160 audio-video modulator provides up to seven channel modulators in one 7-in.-high rack-mountable package. Designed specifically for the master-antenna television market, the crystal-controlled fixed-frequency modulator consists of a card shelf, a plug-in power-supply module, and from one to seven plug-in modulator boards.

Each modulator board accepts baseband audio and video inputs at the rear panel and provides a composite video-modulated radio-frequency output. The unit operates on any channel in the low-, mid-, or very-high-frequency range.

A typical installation would use a combiner to sum the modulator outputs for distribution on a master-antenna TV cable system. Potential applications include apartment buildings, hotels, and schools. Available in 30 to 45 days, the CDM 1160 is $945 for the card shelf with power supply and one modulator card. Additional cards sell for $495 each.

Comtech Data Corp., 350 N. Hayden Rd., Scottsdale, Ariz. 85251. Phone (602) 949-1155 [407]

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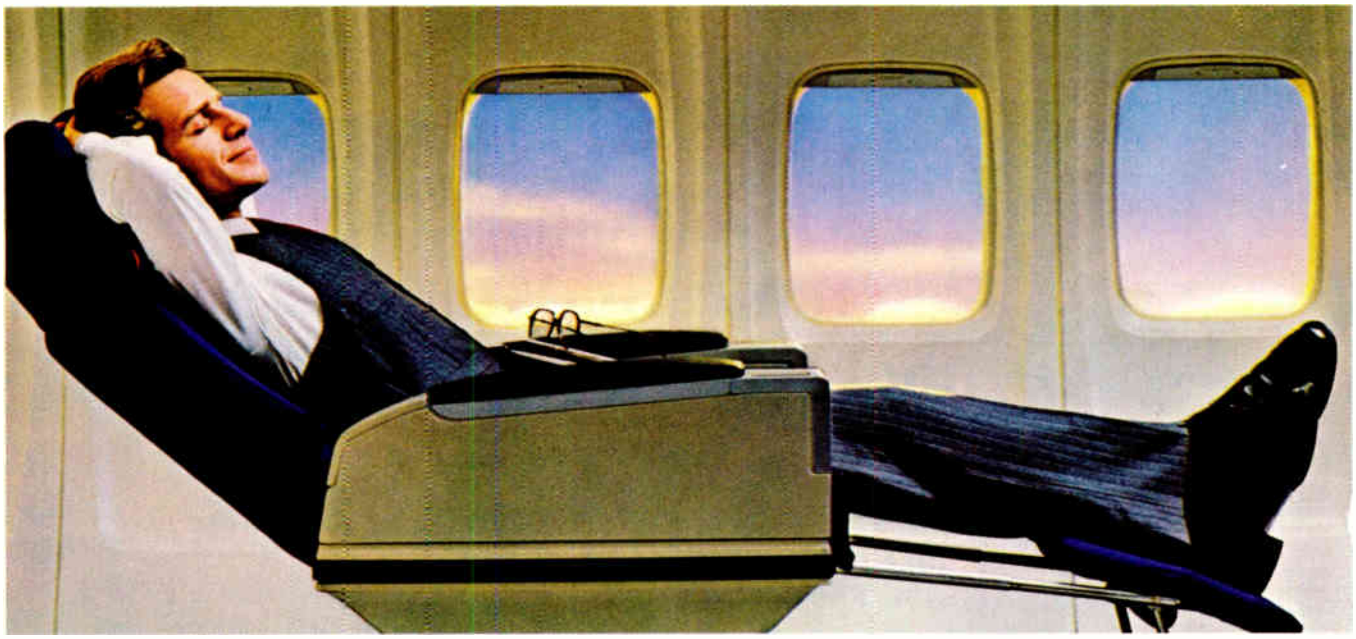

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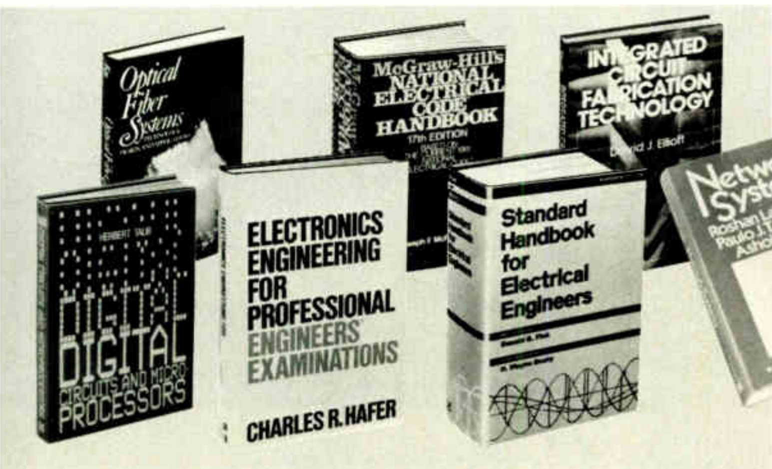

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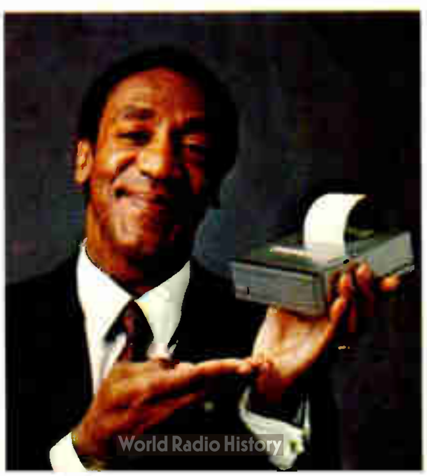

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Wire wraps link carrier sockets

Isolated ground plane protects leadless packages from voltage-plane noise

The increased use of leadless chip-carriers has given rise to a corresponding need for breadboarding tools suited to chip-carrier designs. Methode Electronics Inc. is addressing that need with three logic boards that can be wire-wrapped.

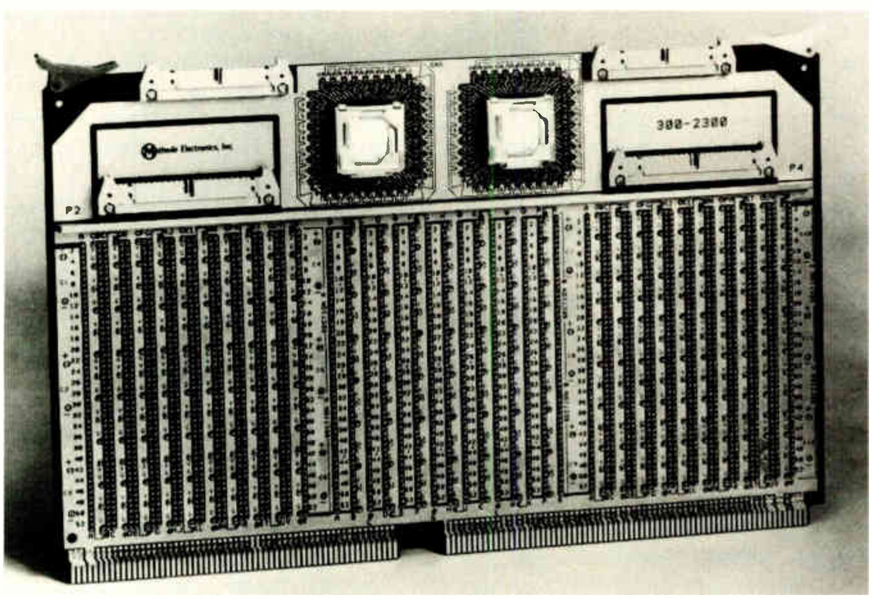
Scheduled for introduction at last week's Nepcon '83 West show in Anaheim, Calif., Methode's Multibus- and Versabus-compatible boards include mounting footprints for Joint Electron Device Engineering Council type A chip-carrier sockets. "To our knowledge, we're the first to marry a chip-carrier socket and a wire-wrappable board," says Methode product manager Edward L. Boonstra. Earlier, the firm brought out a similar board compatible with Motorola's 6800 EXORciser bus [*Electronics*, Jan. 27, p. 137].

The Multibus-compatible boards, known as the 2200 and 2600 series, are equipped with single or dual chip-carrier sockets, respectively. The Versabus board is offered in a dual-socket version only, known as the 2300 series. All three boards also contain an integrated-circuit field. On the Multibus boards, this field amounts to 28 columns of 53 pins each on 0.300-in. spacings, allowing a total board capacity of 84 16-pin DIPs. The 2300 contains 55 columns of 53 pins each on the same spacings, enough for 162 16-pin DIPs.

An important option available on the Methode boards is the location of the chip-carrier sockets on an isolated ground plane, says Boonstra. Isolating the sockets from the board's voltage plane reduces noise and potential damage to the sensitive devices packaged in chip-carriers is reduced. This is an improvement, says Boonstra, over current techniques for prototyping designs with chip-carriers, which involve adapters that plug into standard, single-plane boards that can be wire-wrapped.

All three boards are available with either gold- or tin-plated terminals. In single quantities, the 2200 single-socket and the 2600 dual-socket Multibus-compatible boards with gold-plated terminals are priced at $485 and $560, respectively. With tin-plated terminals, these boards go for $425 and $500 each. The 2300 Versabus-compatible board sells for $925 with gold-plated terminals and $805 with tin, also in single quantities. The firm promises deliveries in two to four weeks.

Methode Electronics Inc., Logic Board Division, 7444 W. Wilson Ave., Chicago, Ill. 60656. Phone (312) 867-9600 [391]



Unit simultaneously bonds all leads to pads of VLSI chips

Capable of assembling very large-scale integrated chips, the model 220 inner-lead bonder uses tape-automated-bonding techniques to bond simultaneously all the leads of a carrier tape to the bonding pads of a VLSI chip having 200 or more connections. Its features include the ability to bond large and more complex chips in wafer format up to 6 in. in diameter compared with the 4-in. limit of competitive bonders.

Also, the model 220 is capable of handling 5-in. wafers, and chips as large as 1 in.^{2} present no problem either. Chips can be presented either in wafer-matrix or in presorted format. Other options include the choice of pulse-eutectic or thermal-compression bonding-head subsystems. The width of the tape ranges from 8 to 70 mm.

Typical VLSI packaging applications include complex hybrids, chip-carriers, plastic quad in-line packages, and gate arrays, among others. Priced at from $65,500 to $95,500, the model 220 bonder will be available in four to six months.

International Micro Industries, P. O. Box 604, Cherry Hill, N. J. 08003. Phone (609) 424-3112 [393]

Rapid heating system anneals silicon and GaAs wafers

A rapid heating system that uses radiant energy can anneal silicon and gallium arsenide in a controlled environment in the space of 10 to 30 seconds versus the 30 to 60 minutes needed by such traditional annealing techniques as diffusion furnaces. The Heatpulse 210T is a benchtop unit intended for process development rather than production situations. It

New products

uses a dedicated microcomputer to control heating cycles and the intensity of the tungsten halogen lamps.

Ion-implanted sources and drains can be annealed with a silicide or refractory metal gate. Gallium arsenide can be annealed after channel or contact implantation. Since the heating cycle is short, no cap is required.

In addition to annealing, the 210T has a variety of other uses where rapid heating of wafers is an advantage, the firm claims. They include oxide reflow, alloying, silicide formation, and activation of controlled, high-resistivity polysilicon layers.

The model 210T is priced at $38,000 and is available now.

AG Associates, 1052 Elwell Ct., Palo Alto, Calif. 94303. Phone (415) 961-6823 [394]

One-piece connector mates ribbon cable to board

The series 303U one-piece connector makes it possible to interconnect flat high-speed data-transmission cables and printed-circuit boards in a single motion without automatic locking. The resulting structure can withstand a 7-lb pull without separation. Disassembly also requires but a single motion.

The connector uses a direct snap-on assembly to the board to achieve high contact force with a reliable gas-tight connection. Spring contacts are made of a tin-plated brass alloy on 75-mil centers and are integrally cast into a glass-reinforced polyester body. The connector can handle circuit boards as thick as 0.070 in.

Each contact terminates in the Cone Point, used in all of the company's connectors. The termination creates high pressure at the tin-plated surface of each circuit-board finger and enhances proper registration. In lots of 5,000, the connector is typically priced at $1.20 each.

Teledyne Kinetics, 410 South Cedros Ave., Solana Beach, Calif. 92075. Phone (714) 755-1181 [395]

Laser welding unit hermetically seals aluminum packages

A turnkey laser welding system, model PW-567, designed especially for hermetic sealing of microelectronics packages, is particularly suited to the hard-to-weld aluminum kind. Welding speed for a typical 0.040-in. weld penetration is 20 in./min. A 3-by-3-in. aluminum package can be welded in only 36 s at a welding cost of about 5¢, claims its maker.

Included with the system are a 400-W pulsed yttrium-aluminum-garnet laser, a dry-box enclosure, a vacuum bakeout oven, and an antechamber. In addition, an X-Y motion system and a computer-based numerical controller are provided.

Because the zone affected by the laser's heat is the narrowest of any thermal process, chances of damage to delicate electronic components are reduced significantly. Welding can be done within 0.0900 in. of temperature-sensitive materials, including soldered-in feedthroughs.

Besides aluminum packages, the laser welding system handles stainless-steel packages equally well with no significant part distortion. Deliveries take six months.

Raytheon Co., Laser Center, Fourth Avenue, Burlington, Mass. 01803. Phone (617) 899-8400 [396]

Insertion system boosts productivity with two heads

Thanks to a twin working head, productivity is more than doubled for the Autosplice insertion unit, which costs only 20% more than a single-headed unit. The computer-run machine inserts wire-wrapped or connector pins, standoffs, test points, and male terminals into printed-circuit boards, connector housings, and bobbins.

Pins are fed from reels of pre-notched pin material. The continuous square or round wire pins are formed end to end and wound on the reels, a method that facilitates high-speed terminal insertion and reduces pin costs, its maker claims. Pin material is normally electroplated brass or phosphor bronze. A reel holds 40,000 pins.

The computer can store up to 99 different programs and supports four subroutine levels. The complete dual-headed system is priced from $20,000 to $35,000. Pins are priced from $2.50 to $6.50 a thousand. Delivery takes up to 12 weeks.

Autosplice Inc., 59-12 37th Ave., Woodside, N. Y. 11377 [397]

Plater deposits gold on up to 30,000 pins per hour

A fully automated, controlled-depth plating machine deposits gold on connector pins at production rates of 10,000 to 30,000 pins/h. The Sel-Rex Pinmaster, as it is called, is said to combine great production flexibility with precision plating and thereby reduce gold consumption by as much as 75% over traditional barrel-method plating.

Pins can be loaded in bulk into a vibrating-bowl feeder and are then oriented and fed through the built-in plating cycle through a notched cathode wheel. The wheel can be quickly replaced with another to accommodate pins of different sizes and profiles to suit particular plating requirements. Gold is deposited precisely where it is needed in thicknesses ranging up to 5 μm.

A separate master console provides easy operator monitoring and production control.

The Pinmaster's price starts at about $70,000 and rises with options. Delivery is in six weeks.

Sel-Rex Plating Systems, 75 River Rd., Nutley, N. J. 07110. Phone (201) 667-5200 [398]

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Products newsletter

Work-station terminal resolves graphics to typesetting quality

The market for real-time electronic typesetting and layout systems, though an embryonic one, is already attracting the attention of designers on the lookout for ever-better graphics displays. Now they can work with what Instrumentation Laboratory Inc.'s Pixel division in Andover, Mass., bills as the highest-resolution raster-graphics terminal yet. The Pixel 80G graphics/engineering work station uses a bit-mapped display of 1,728 by 2,180 picture elements, or pixels, with a resolution fine enough to display very small type sizes and magazine-quality halftone illustrations. Interactive **layout of text, graphics, and halftones also gets an assist from the 80G's speed, which is 35% to 40% better than that of conventional graphics terminals,** says Pixel. Based on Motorola's 10-MHz 68010 microprocessor, the 80G uses hardware-implemented raster functions to process up to 9.75 million pixels/s and refreshes its 70-kHz interlaced display at 150 million pixels/s. The terminal, which can be used for computer-aided design and manufacturing as well, will sell for $19,900 with 1 megabyte of memory, 0.5 megabyte of refresh memory, and 40 megabytes of hard-disk storage.

TI dual-function chip saves line-card space

Using its silicon-gate complementary-MOS and switched-capacitor technologies, Texas Instruments Inc. is making available telecommunications line-card components that integrate the supervisory and hybrid functions onto a single semiconductor [*Electronics,* Feb. 24, p. 115]. Designated TOM4204 and 4205, **TI's subscriber-line control circuits are designed to reduce space and power consumption,** which contribute to a general limit of four lines per card. The chips typically dissipate 100 mW in active mode and 10 mW in standby or line-monitoring modes. They also contain two independent programmable attenuators and can be programmed by software to select one to three external balancing networks, allowing the line signal to be automatically adjusted for the distance of the phone from the exchange or central office. In a ceramic package, the 24-pin 4204 sells for $11.74 in lots of 100. The 4205 is $11.99; it has 28 pins, providing for an external ground-start reference and control of extra relays. Both are available now.

Upgraded printers handle Wordstar and Visicalc

The Microline 84 dot-matrix printer marketed by Okidata Corp. of Mt. Laurel, N. J., has been enhanced so that it is compatible with a number of software packages, including Wordstar and Visicalc. The new model, called Step 2 Microline 84, **also sports a switch-selectable interface, select-deselect control, Spanish-language character set, and forward-feed superscript and subscript printing.** It prints bidirectionally at 200 characters/s or 50 c/s in the letter-quality mode with proportionally spaced characters. An RS-232-C interface that runs at up to 19,200 baud is also standard on the unit. Its suggested retail price is $1,495 ($1,395 with a parallel interface), and it is available now.

Single-chip modem gets 50% price cut

Six months after volume production has started, the TMS99532 single-chip modem from Texas Instruments Inc. is undergoing a drastic price cut. The 18-pin, 200-b/s modem chip [*Electronics,* March 24, 1982, p. 180] was priced at $24.99 each in lots of 1,000. **Citing recent increases in yields,** TI is reducing the price of the plastic-packaged parts to $12.75 in lots of 1,000.

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Career outlook

A look at Congress from inside

With toxic wastes, multibillion-dollar weapons systems, and other technology-related issues on the nation's agenda, the need for technically competent people contributing to the U. S. legislative process is becoming increasingly obvious. Rare is the engineer or scientist, however, who prefers the political infighting, deal-making, and painstaking detail work of Capitol Hill over the silicon, design specifications, and operating systems of corporate and academic engineering.

In an effort to fill that technical gap in the legislative process, particularly in the ranks of the researchers gathering information for congressmen and senators, the Congressional Fellows Program of the Institute of Electrical and Electronics Engineers places a few of its members, chosen competitively, right in the midst of the Washington, D. C., lawmakers each year. This year, two IEEE members will immerse themselves in the inner workings of Congress.

"Diverse" best describes the many opportunities that the fellows have to contribute to a congressman's personal staff or to the professional staff of a congressional committee. In his or her one year in the capital, a fellow might review proposed legislation from a technical perspective, lead a research effort about a particular issue, and help a constituent solve a local problem.

"A year's intimate exposure to our legislative branch can greatly broaden one's perspective on the larger issues our country faces about science and technology," says Eli Fromm, a professor at Drexel University in Philadelphia who began his fellowship in September 1981. The IEEE gives the fellows flexibility in choosing their assignments, and the chance to examine policy issues was one reason Fromm picked the House subcommittee on science, research, and technology. Although a fellow can choose an assignment that demands more of his or her special expertise, most participants in the program apply to it in the hope of broadening their horizons.

The opportunity for this exposure was first offered in 1973, when the engineering and science community followed the lead of the American Political Science Association in trying to involve people with special expertise in the legislative process. Seven fellows from various professional societies, including the IEEE, the American Association for the Advancement of Science, and the American Society of Mechanical Engineers, were sent to Washington.

Over the life of the program, the IEEE has contributed 21 members to the overall program out of a total of more than 100 from all societies. However, its selection criteria are different from those of some of the other groups.

"IEEE is one of the few groups that look at experience as one of the major selection criteria," says Tom Suttle of the IEEE. Ten years of engineering work after the bachelor's degree is required, fewer for those with a master's or doctorate. "Some of the other societies prefer to have people who have just gotten their doctorates. We want someone with a breadth of experience."

No party politics. In addition to a solid technical record and demonstrated service to the profession, fellows must have belonged to the IEEE at the member grade or higher for four years at the time of application, and they must also be U. S. citizens. Political affiliation is specifically excluded as a criterion of selection.

"Customarily, we receive about 15 to 20 completed applications," says Suttle. "This means the references, the detailed background information, and necessary letter of support from the applicant's organization." Participants usually maintain their salary during their fellowship, with half of the funds coming from the IEEE and half from the employer. Suttle notes that the letter of support, IEEE's assurance that the fellow's career will not be damaged by his year-long sabbatical, "is not always easy to get." But, as former fellow Fromm emphasizes, the experience is well worth the effort: "Seeing the Government workings from the inside really opened my eyes." **–David W. Campt**