DECEMBER 29, 1981




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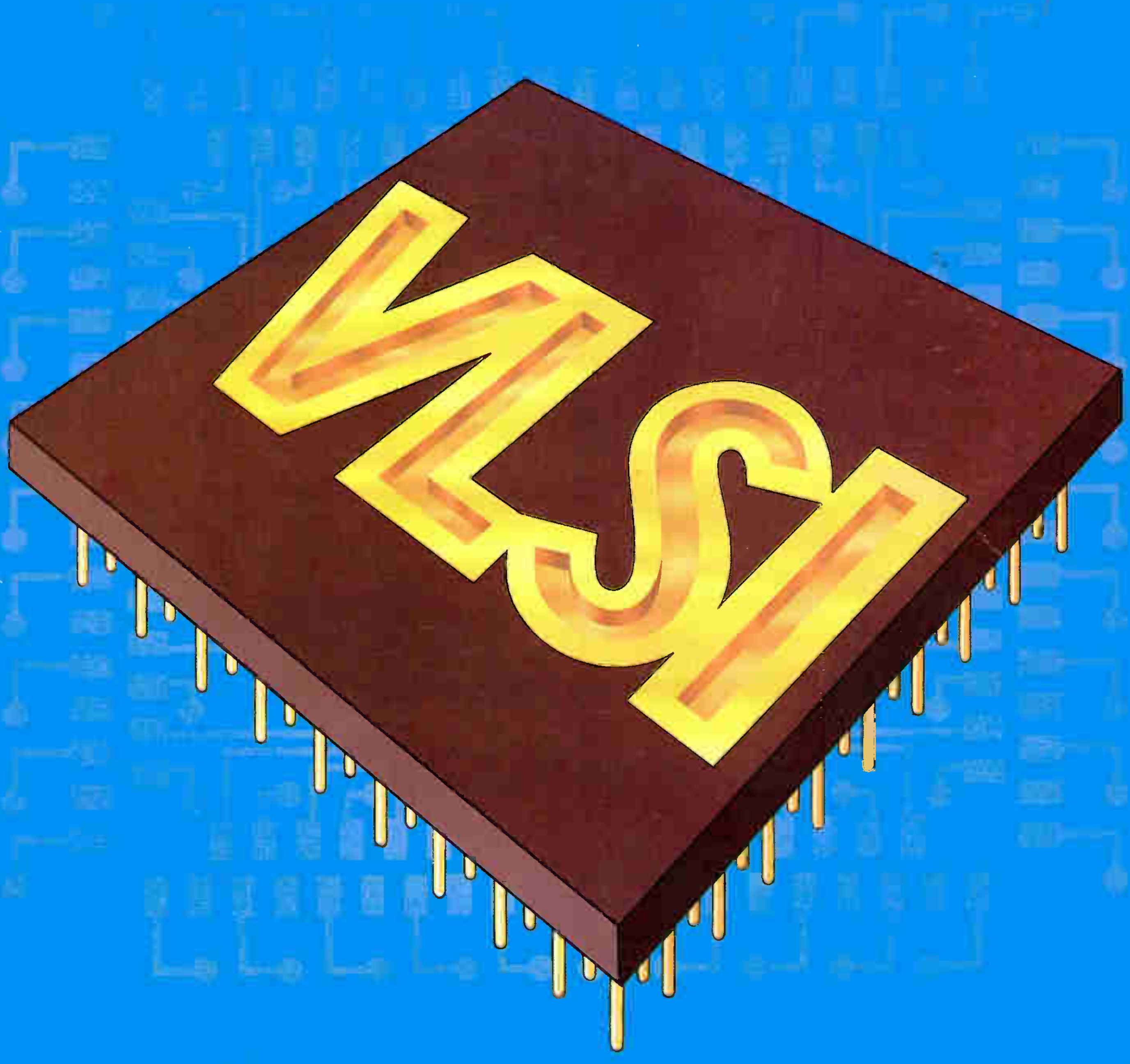
# Electronics®

## Making its mark on packaging



# HP introduces a new series of pulse/function generators.


## 8116A PROGRAMMABLE PULSE/FUNCTION GENERATOR

## Great performance and convenience at half the price you'd expect.

Fully HP-IB programmable, the outstanding new 8116A generates pulse and haversine/havertriangle as well as sine, square, and triangle functions over the entire 1 mHz-50 MHz frequency and 32 Vpp amplitude ranges.

The new 8116A offers true pulse capabilities such as 6 ns transition times and 10 ns minimum pulse width, plus variable duty cycle for the other functions. Any waveform can be generated in a choice of external trigger and modulation modes. And, you can always combine AM, FM, PWM or VCO with external trigger, gate, width, sweep or burst controls. Internal/external burst mode and logarithmic sweep are optional.

**Simple operation, high reliability.**
Easy to program, the friendly HP 8116A features a self-prompting menu and built-in error recognition for highly simplified operation.

Custom HP IC's and a low operating temperature contribute to high reliability. And, the 8116A is easy to service thanks to self-test, signature analysis and accessible modular design.

For bench or system, the new HP 8116A is a prime choice at just $3,440.* But if manual operation meets your needs, we have another outstanding new instrument. . .

## 8111A MANUAL PULSE/FUNCTION GENERATOR

## Digital display and plenty of capabilities at your fingertips.

HP's new 8111A offers the same waveforms as the 8116A, over a full 20 MHz frequency and 32 Vpp amplitude range at about half the price — just $1,775.* Variable duty cycle (10%-90%) and pulse width down to 25 ns are combined with fast 10 ns transition times for excellent pulse and squarewave fidelity.

**Digital readout for all parameters.**
For operating ease in bench, service and educational applications, the 8111A's digital readout allows simple parameter setting and resetting — in most cases, there's no need for additional instrumentation to set and repeat parameters. And, digital readout also allows specified accuracy, repeatability and resolution.

For complete information, write to: Hewlett-Packard, 1820 Embarcadero Road, Palo Alto, CA 94303. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

*Domestic U.S.A. prices only.

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Circle 1 on reader service card

# RF trans-formers

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## 0KHz-800MHz...balanced, DC isolated, center-tapped
## 6 off-the-shelf models from Mini-Circuits from $2.95

Select from the economical, microminiature T–series (plastic case) or TMO series (hermetically-sealed metal case) covering 10 KHz to 800 MHz. These models operate from 12.5 to 800 ohms with insertion loss typically less than 0.5 dB.

For large dynamic range applications, specify the T–H series which can handle up to 100 mA primary current without saturation or distortion.

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Of course, Mini-Circuits' one-year guarantee is included.


Bent Lead version, please specify

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| Model No. | T1-1 TMO1-1 | T1-1H | T1.5-1 TMO1.5-1 | T2.5-6 TMO2.5-6 | T4-6 TMO4-6 | T9-1 TMO9-1 | T9-1H | T16-1 TMO16-1 | T16-1H |
|---|---|---|---|---|---|---|---|---|---|
| Imped. Ratio | 1 | 1 | 1.5 | 2.5 | 4 | 9 | 9 | 16 | 16 |
| Freq (MHz) | .15 400 | 8-300 | .1-300 | .01 100 | .02 200 | .15-200 | 2-90 | .3-120 | 7-85 |
| T Model (10-49) | $2.95 | $4.95 | $3.95 | $3.95 | $3.95 | $3.45 | $5.45 | $3.95 | $5.95 |
| TMO model (10-49) | $4.95 | | $6.75 | $6.45 | $6.45 | $6.45 | | $6.45 | |

**CENTER-TAPPED DC ISOLATED PRIMARY & SECONDARY**

| Model No. | T1-1T TMO1-1T | T2-1T TMO2-1T | T2.5-6T TMO2.5-6T | T3-1T TMO3-1T | T4-1 TMO4-1 | T4-1H | T5-1T TMO5-1T | T13-1T TMO13-1T |
|---|---|---|---|---|---|---|---|---|
| Imped. Ratio | 1 | 2 | 2.5 | 3 | 4 | 4 | 5 | 13 |
| Freq. (MHz) | 05-200 | .07-200 | .01-100 | .05-250 | 2-350 | 8-350 | .3-300 | .3-120 |
| T Model (10-49) | $3.95 | $4.25 | $4.25 | $3.95 | $2.95 | $4.95 | $4.25 | $4.25 |
| TMO model (10-49) | $6.45 | $6.75 | $6.75 | $6.45 | $4.95 | | $6.75 | $6.75 |

**UNBALANCED PRIMARY & SECONDARY**

| Model No. | T2-1 TMO2-1 | T3-1 TMO3-1 | T4-2 TMO4-2 | T8-1 TMO8-1 | T14-1 TMO14-1 |
|---|---|---|---|---|---|
| Imped. Ratio | 2 | 3 | 4 | 8 | 14 |
| Freq. (MHz) | .025-600 | .5-800 | .2-600 | .15-250 | 2 150 |
| T model (10-49) | $3.45 | $4.25 | $3.45 | $3.45 | $4.25 |
| TMO Model (10-49) | $5.95 | $6.95 | $5.95 | $5.95 | $6.75 |

**FT FTB**

| Model No. | FT1.5-1 | FTB1-1 | FTB1-6 | FTB1-1-75 |
|---|---|---|---|---|
| Imped. Ratio | 1.5 | 1 | 1 | 1 |
| Freq. (MHz) | .1 400 | .2-500 | .01-200 | .5 500 |
| (1 4) | $29.95 | $29.95 | $29.95 | $29.95 |

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# Electronics

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# Electronics

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## Highlights

**Cover: Wealth of new techniques updates pc-board packaging, 66**

To meet the packaging needs of very large-scale integrated circuits, a host of new techniques are surfacing that are likely to change the face of printed-circuit boards. As well as updated dual in-line packages and leadless chip-carriers, pin- and pad-grid arrays are garnering attention. Also, the Department of Defense's Very High-Speed Integrated Circuits program (VHSIC) is spurring the development of more innovative techniques, such as flip chips combined with new versions of tape-automated bonding.

The cover is by Meyers & Noftsinger.

**U. S. firms shun sales to Japan's NTT, 58**

Just a year ago, the Nippon Telegraph & Telephone Public Corp. reversed its procurement policy to open its doors to foreign suppliers. Some U. S. companies have won contracts, but more have responded lackadaisically.

**Testing: changing strategies meet the needs of a changing world, 79**

Testing grows more important and costly as products grow more complex—yet little practical knowledge of new techniques is being disseminated. Inaugurated with the following two articles, this series is intended to lay the groundwork for the implementation of test strategies for the 1980s.

**Testing: the proper plan covers all bases, 80**

A look at the process of developing strategies uncovers the desirability of testing earlier to test more easily and points up the need, not just to find the right answers, but to ask the right questions.

**Testing: careful test scheme speeds development of processor, 84**

The first examples of a complex microprocessor chip functioned perfectly, and much of the credit goes to a test regimen that began in the early stages of development. The approach was to use both a logic simulator and a breadboard emulator.

**Electrochromic research paying off, 89**

The legibility and wide viewing angle of colorful electrochromic displays has fueled steady research efforts around the world to overcome their shortcomings. Recent advances include the development of materials that offer improved operating lives and a scheme that implements what amounts to matrix addressing.

**. . . and in the next issue**

The annual world market report . . . the fastest superminicomputer yet . . . an alternative to matrix addressing for complex light-emitting-diode displays . . . a family of 23-gigahertz microwave links that serves local networks.


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# Publisher's letter

**The functional impact** of very large-scale integration is beginning to make itself felt in the design world. The sheer power of tens of thousands of devices on a chip makes designers lick their lips in anticipation of all the wonderful systems that will be born out of all this capability.

But VLSI is not just a glorious step forward in technological capability. It could in fact be several steps backward for engineers and companies that are not prepared to cope with the problems being introduced by its order of magnitude increase in complexity.

In this issue we deal extensively with two of those problems—packaging and testing. The appearance of VLSI has left in its wake a host of difficult engineering questions that must be successfully resolved before the new capability can be widely applied. Protecting the big complex chips from hostile environments, yet providing access to the outside world with lead counts up to 300 pins, and at the same time allowing cost-effective insertion into heavily populated printed-circuit boards—all in a reasonably sized package—is a challenging job. And the challenge is being met.

Jerry Lyman, our packaging and production editor, has been following the evolution of packaging of ICs for many years, and he never ceases to be amazed at the steady stream of package innovations that are forced by the growth of ICs. "As much ingenuity and thoughtfulness are going into package design now as in the design of the circuits themselves," he observes, "and a lot of the cost, too." In his special report on page 66, Jerry pinpoints how major firms around the world are coming to grips with packaging problems and coming up with endless new terms like pin-grid and pad-grid arrays, fine-pitch chip-carriers, and tape-automated bonding.

**The testing community,** too, is feeling the burden of VLSI. Richard Comerford, our test and measurement editor, became aware of this on his visits to many firms, but especially after he talked to users of test equipment at the recent Cherry Hill Test Symposium in Philadelphia. It was there he conceived the idea of a series of articles by users who were faced with specific testing challenges and responded with a strategy that worked.

"I see a vast need for information on how existing equipment can be used cost-effectively to solve complex test problems," Rick says. "It's not just a matter of ordering another machine, but—particularly in the case of VLSI—it's necessary to plan the whole test strategy, which involves what kind of test to perform, where to perform it, and how to use existing resources to the fullest."

The series on test tactics begins with two articles in this issue, starting on page 79. The first is by Jon Torino and H. Frank Binnendyk of Logical Solutions Inc., a consultant firm specializing in testing strategy. Both have extensive experience in testing. Torino, founder of the firm, has had positions with John Fluke Manufacturing, Instrumentation Engineering, and Tektronix. Coauthor Binnendyk had four years of test experience at Beckman Instruments. Their lively article tells how manufacturing costs can be cut with a comprehensive test plan.

The second article in the series is by a quartet from Texas Instruments—Karl Guttag, Robert Puckett, Stephen Sacarisen, and Thomas Dye. They were charged with the design of a new 16-bit microrocessor, the 99000. In this article, they tell how a carefully worked-out test strategy helped them not only hit their design goals on the first pass, but also produced effective test procedures and software before the first chip came off the line.

There will be more of these vital test case histories coming along in future issues.

# ISO-CMOS.™ THE HIGH SPEED, LOW POWER REVOLUTION.

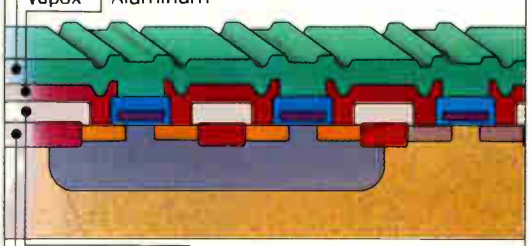
*When we developed the ISO-CMOS process at Mitel we also developed a way of thinking. We ensured that applications for the technology were kept foremost in mind–every step of the way.*

*Design Philosophy? Right from the start we made sure that our integrated circuit designers were exposed to the system environment, not just the component environment. In developing worldleading PABXs this perspective allowed Mitel Semiconductor to develop integrated circuits with well thought out general purpose interface capability.*

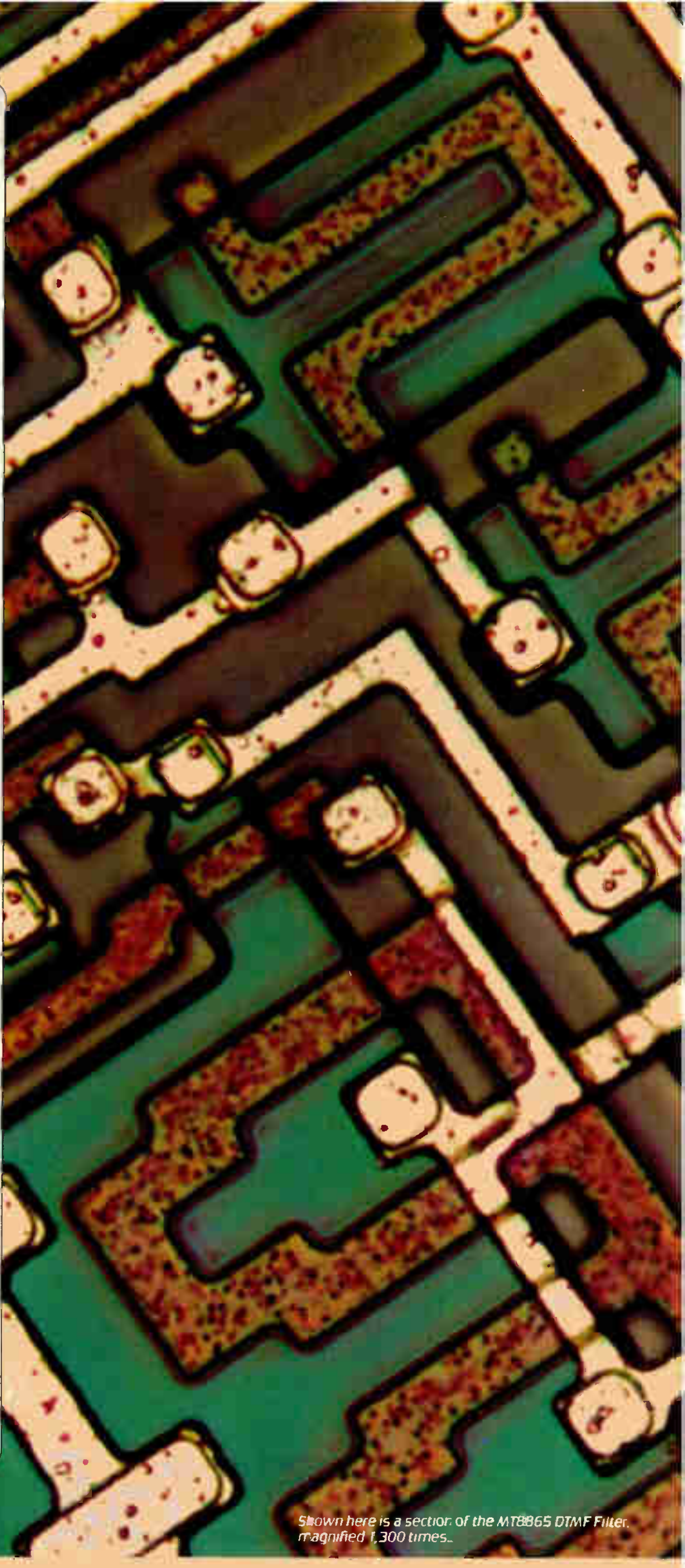
*Quality and Reliability? Our ISO-CMOS production technique and our quality assurance screens are based on* MIL Standard 883 Test Methods and Procedures. *Every ISO-CMOS device is hermetically packaged and 100 percent burned in. So ISO-CMOS quality and reliability is built in at the start of the process and is maintained through to completion.*

*Availability and Capacity? Mitel Semiconductor products are being marketed world-wide, with a supporting network of sales offices and distributors. In addition to a continuing expansion of manufacturing capacity by Mitel Semiconductor, Mitel ISO-CMOS devices are now sourced under licence by three major manufacturers, making our products and process the number one multi-sourced choice for new designs.*

*ISO-CMOS. It has created a revolution in the telephone, PABX and digital logic markets based on a capability for high speed, low power and high density. The continuing evolution of this superior technology is assured by the ongoing commitment by Mitel to the process.*




*Discover what Mitel Semiconductor can do for you, by contacting your local Mitel sales office.*



*Shown here is a section of the MT8865 DTMF Filter, magnified 1,300 times.*

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## News update

■ The no-inspection-verification (NIV) program at General Motors Corp.'s Delco Electronics division, Kokomo, Ind., has fallen behind schedule. Delco had hoped by year end to place 20% to 30% of all integrated-circuit purchases under the NIV program—which calls for eliminating conventional receiving inspection of incoming devices that met high-quality standards in previous shipments [*Electronics*, May 19, 1981, p. 141].

Despite strong performances by vendors, however, no ICs are yet being accepted on an NIV basis. One Delco official blames the delay on "foot dragging" by receiving and inspection employees, who see their participation as "working themselves out of a job." Delco now hopes to begin placing discrete semiconductors and ICs in the program within the next few months. The division already accepts a large number of passive components without inspection. **-Wesley R. Iversen**

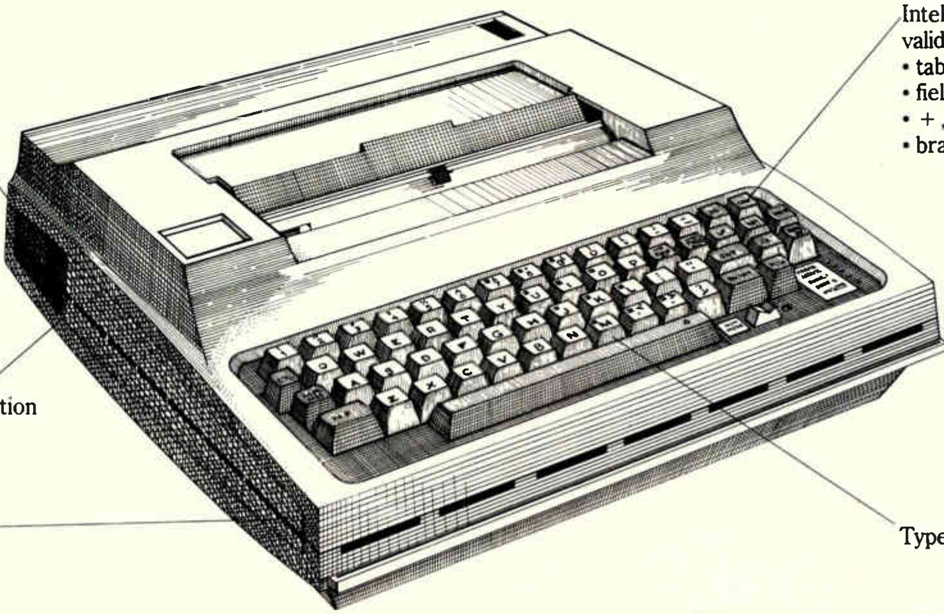
■ New big-board test systems are off to a fast start, says David B. Ruggiero, marketing manager of the Board Test division of GenRad Inc., Concord, Mass. Announced this autumn [*Electronics*, Sept. 22, p. 169], the model 2271 and 2272 board testers are the most comprehensive currently available—one configuration of the 2272 can test board subsystems with more than 3,000 nodes using a bed-of-nails test fixture with more than 3,500 pins. These systems test both linear and digital circuit boards.

GenRad's Ruggiero expects to have shipped more than 20 of the giant testers—prices range from $150,000 on up—by the end of this year. He is increasingly optimistic. "Originally, we felt that such systems aimed at the upper 10% of the board test-system market—at users with high-pinout and high-node-count digital boards. Now after adding in prospects in the peripheral equipment, industrial control, and the large- and small-computer sectors, we think we may be addressing something like 30% of the board-tester market." **-James B. Brinton**

# Information Specialist.

## 767 KSR

### Bubble Memory Data Terminal




TI's *Silent 700** Model 767 Electronic Data Terminal is ideal for remote data entry applications – especially those where data integrity is essential. The versatile 767 offers the advantage of high-speed batch synchronous communications with integrated nonvolatile bubble memory data storage for reduced connect time and communications costs. Featuring TI's Data Entry Validation and 3780 protocol capabilities, the 767 easily accommodates integration into new or existing distributed data entry networks.

TI is dedicated to producing quality, innovative products like the Model 767 Electronic Data Terminal. And TI's hundreds of thousands of data terminals shipped worldwide are backed by the technology and reliability that come from 50 years of experience.

For more information on the Model 767, contact the TI sales office nearest you. In Europe, write Texas Instruments, M/S 74, B.P. 5, Villeneuve-Loubet, 06270, France, or phone (93) 20 01 01. In Asia Pacific, write Texas Instruments Asia Ltd., 990 Bendeemer Rd., Singapore 1233. Telex RS 21399, or phone 2581122.

*TI invented the integrated circuit, the microprocessor and the microcomputer.*

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INCORPORATED

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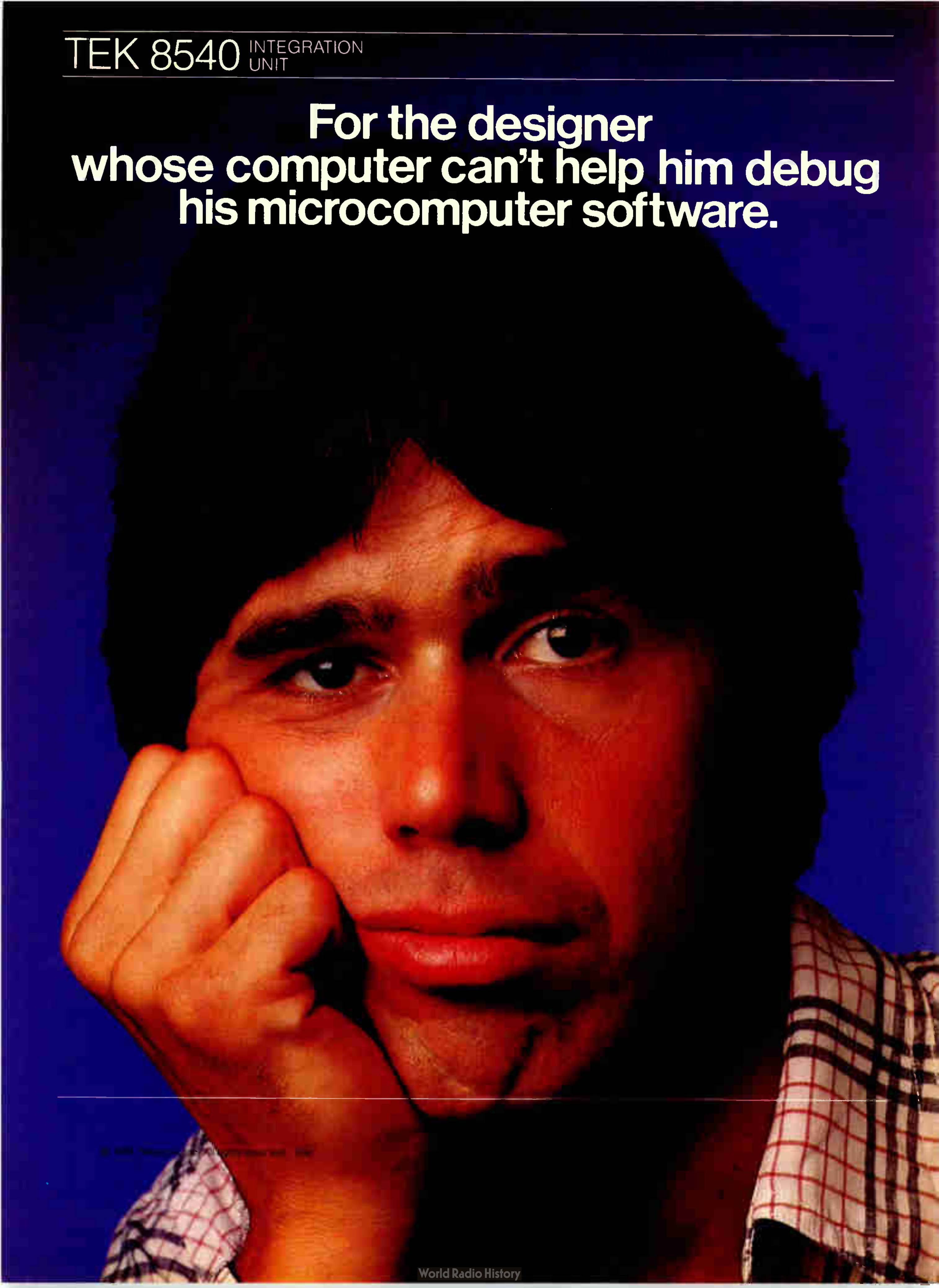
TEK 8540 INTEGRATION UNIT
For the designer whose computer can't help him debug his microcomputer software.

# Tek announces the 8540 Integration Unit.

When designing with microcomputers, your resident host computer can be a powerful ally in the fight against impossible design schedules.

But, ultimately, it only gets half the job done.

Even though it gives you everything you need for fast, accurate code development, you still have to install and debug your developed code in the prototype hardware. A process that often consumes half your total design time.

**Enter the 8540 Integration Unit.**


When it comes to hardware/software integration, Tektronix has the answer. The 8540 Integration Unit. It interfaces easily with almost any host computer using ASCII terminal communications. And, once connected, its high-performance emulators and debug software handle the entire integration process.

All with an unmatched range of chip support.

## Your host & the 8540: A synergistic team.

The 8540's sophisticated interface features make the most out of your host's processing power. Like the ability to download symbolic debug tables along with object code to the 8540. Or permanently store your specialized, host-oriented debug commands aboard the 8540 as either key words or command strings.

Breakpoint halts program execution at the address label "LOOP." Also shown is a detailed description of the processor's internal status at the breakpoint.

To retain any terminal-oriented command structures you've developed, the same terminal can be used for direct communication with either the 8540 or the host system. There's even a local printer interface on the 8540 so its printing operations won't burden the host.

## A Trigger Trace Analyzer for real-time prototype monitoring.

In many applications, the timing of code execution becomes critical. To fully support real-time debugging, the 8540 includes an optional Trigger Trace Analyzer. It has four trigger channels ready to track down even the remotest sections of code execution.

You can do things like identify all non-ASCII writes to an I/O port. Or count the number of calls to a specific subroutine. Or measure the elapsed time of an interrupt handler routine.

| Chips The 8540 I.U. Supports: | | |
|---|---|---|
| 16-bit | 8-bit | |
| Z8001 | 6809 | 8088 |
| Z8002 | 6800 | 8048 |
| 8086 | 6808 | 8039 |
| 68000 | 6802 | 8039-A |
| | Z80A | 8035 |
| | 8080A | 8021 |
| | 8085A | 8022 |
| | 8049 | 8041A |

Let the 8540 finish the job your computer started.

Contact your nearest Tektronix field office about buying or renting the 8540.

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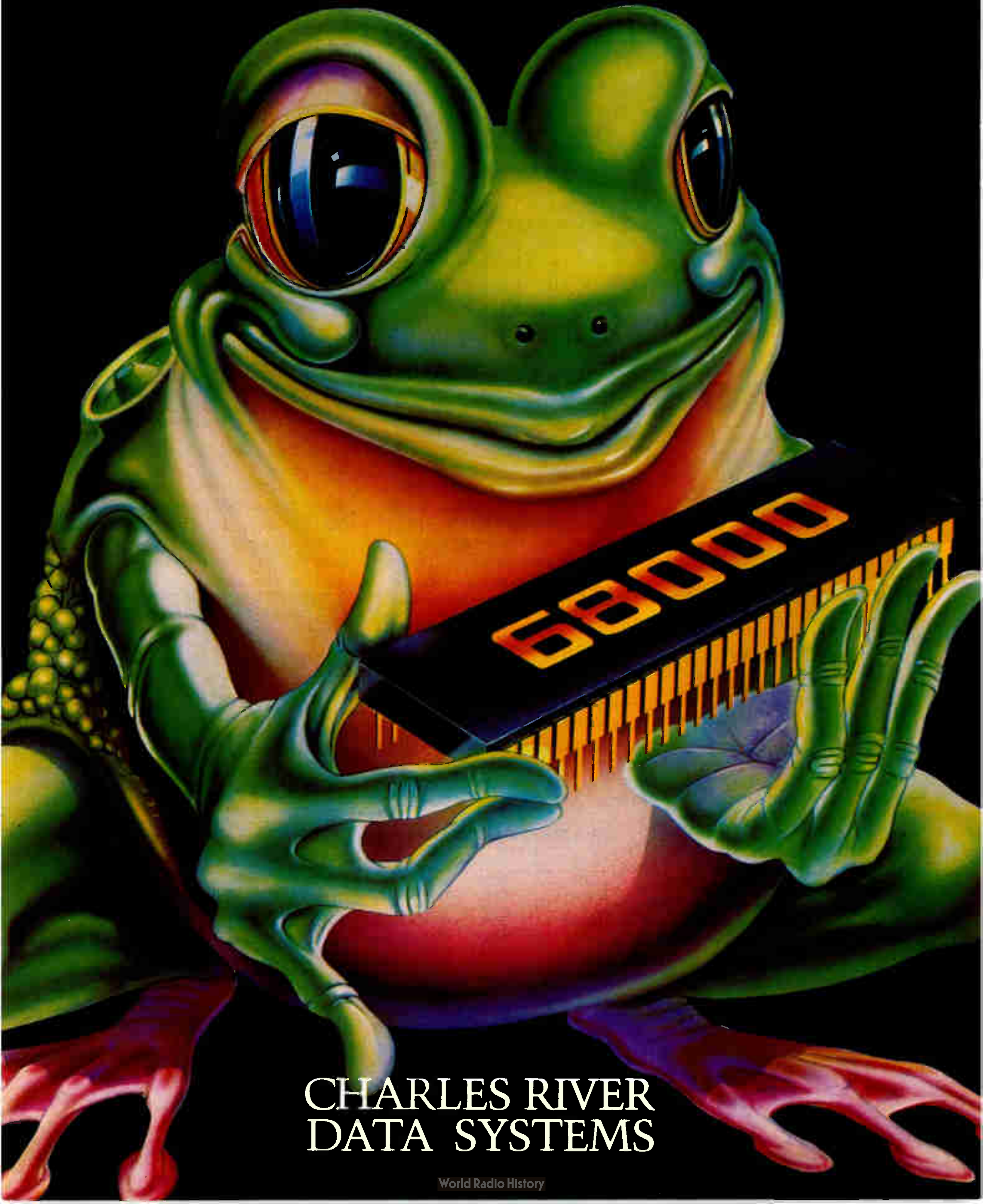
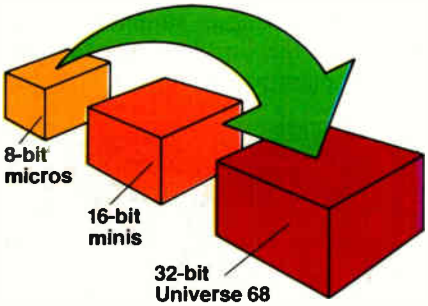
# Universe 68 leapfrogs the 16-bit minis.



## Introducing the first 32-bit supermicro for OEMs

Our new Universe 68 computer system offers powerful 32-bit architecture, a microcomputer price, the programming efficiency and portability of a UNIX-like operating system, and the refreshing experience of working with a computer supplier whose business practices are actually designed to make life easier for OEMs.




## Jumping over outmoded 16-bit architecture

Built around the Motorola 68000 microprocessor, the Universe 68 system is a 32-bit supermicro that leapfrogs conventional 16-bit minicomputer technology. It has directly addressable, non-segmented address space of 16 million bytes, compared to the 64-kbyte limitation imposed by 16-bit architectures.

That means greater functionality per dollar, increased program development efficiency, and power to tackle demanding new applications.

*The Universe 68/10 computer system*

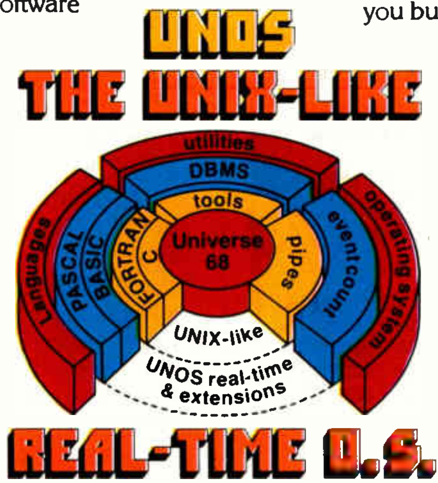
## Outhopping supermini prices

The Universe 68 gives you 32-bit performance at micro prices- -while the big frogs in the minicomputer pond are still offering 32-bit technology only in expensive "superminis." A Universe 68/10 with 32-bit processor, 256 kbytes of memory, floppy disk, and Winchester disk sells for under $20,000. Order ten, and the unit price drops to $16,860, including system software.

## Springing past conventional system software

UNOS, our UNIX-like operating system, is part of the new generation of more flexible, easier to use software written in the high-level systems programming language C. To help OEMs develop products faster and less expensively, it incorporates UNIX features (such as "pipes," I/O redirection, and hierarchical files), plus portability that conventional systems software can't match.

To its UNIX-like base, which supports FORTRAN and C languages, UNOS adds PASCAL and BASIC, an expanded data base management system (DBMS), and an array of run-time oriented, real-time transaction processing capabilities, including a highly sophisticated "Eventcount" process synchronization mechanism. These extensions can be the key to implementing real-time and information systems applications.




## Croaking obsolete business practices

OEMs often find computer suppliers tough to deal with. Bundled hardware and software limit flexibility in configuring systems, while proprietary busses and assembly-language software can lock you in to one vendor.

We're out to change all that by offering OEMs a choice. You can buy complete systems from us, and just add application software. Or buy some components from us, and go elsewhere for others. You can even buy UNOS from us and run it on someone else's hardware. And by building the Universe 68 computer around standard, non-proprietary technology like VERSAbus, SASI bus, and the 68000, we've made second-sourcing easy.

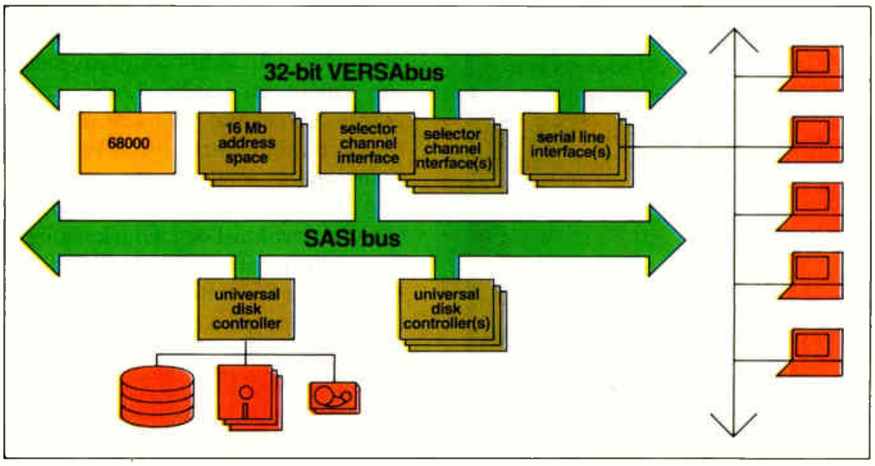
We've also introduced a more sensible approach to discounts. We give you discount credit for everything you buy. Our software discounts are based on how many licenses you buy, not in one year, but over *twenty* years. And they cut deep—all the way to 98%. We think this honestly reflects our costs: software development costs are almost entirely loaded at the front end, and support costs fall quickly once an OEM has gained experience.

## Swallowing up the competition

If you need 32-bit power at a micro price and you can't wait for the minicomputer giants, you should know more about the Universe 68 computer and UNOS. For full information, call or write Charles River Data Systems, 4 Tech Circle, Natick, MA 01760, (617) 655-1800.

With the price/performance story we have to tell, we're ready to make a megasplash in the minipond.

*The Universe 68 system takes advantage of standard building blocks, such as the 68000 microprocessor, 20-megabyte-bandwidth VERSAbus, and SASI bus.*

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SASI bus is a trademark of Shugart Associates. UNOS is a trademark of Charles River Data Systems.

# People

## Clark follows his feelings and lands Chinese contract

*Fingerspitz gefühl* is what Otto A. Clark calls it—a feeling in the fingertips. Though he lacks a formal technical education, the 56-year-old Clark means by this that after 23 years in the copier business, he knows a good copier design when he gets his hands on it.

The Chinese government obviously agrees with Clark's high evaluation of his company's CMC 2000—a low-cost plain-paper unit that delivers 18 copies a minute. Surprising to some in the industry, Clark's tiny $1.5 million suburban Chicago firm, Clark Copy International Corp., last month landed a copier deal with the Chinese that is expected to net $60 million for the company over the next three years.

Initially, says Clark, 6,000 CMC 2000s manufactured in Melrose Park, Ill., will be purchased by the Chinese. After that, an additional 200,000 units are to be manufactured in China.

He attributes his firm's success in part to a Chinese preference for dealing with American businessmen. Also, his fluency in German as well as French, Slovak, and English was an aid in the Chinese negotiations, he says. In addition, Clark concedes, a Chinese dislike for the Japanese may have helped his company snatch the business, since U.S. copier giants Xerox and IBM sell machines that are made partially or completely in Japan.

A naturalized U.S. citizen, the Czechoslovakia-born Clark came to this country in 1950 armed with a law degree from Bratislava University. He obtained a master's degree in economics from Ohio State University in 1953, then founded a firm known as Intercontinental Photocopy Corp., which he headed until selling out in 1971. Clark Copy was then founded in 1976.

With fiber optics and complementary-MOS logic in its electronic design, Clark believes the CMC 2000 is priced right at $1,995. Though Japanese suppliers today dominate the world market for low-priced plain-paper units, Clark has ambitious intentions. Once Chinese manufacturing begins, "we have plans to go to Tokyo to sell it [the CMC 2000]," he declares. "Our Japanese friends are making money in this country. There's no reason we shouldn't be doing it there."

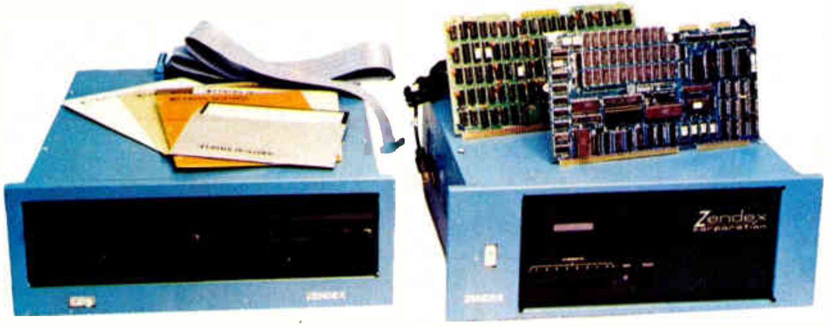
**Feeling good.** Otto Clark's $1.5 million company beat out the industry giants for a big copier sale to the Chinese.

## Thurston to help lead AEA toward solving EE shortage

"The electronics industries growth rate in the '80s is going to be limited by the number of technical professionals available," says William R. Thurston, newly elected chairman of the American Electronics Association. "But only about a third of the applicants to engineering schools are accepted," he adds. "Obviously there is a bottleneck at the higher education level."

President and chief executive officer of GenRad Inc., Thurston is going beyond the point of simply defining the problem. With the AEA board of directors, he plans to move to solve it.

One answer is more aid for colleges and universities, he feels. Thus,









the AEA is fostering an engineering education foundation. "We are suggesting that AEA member firms set aside 2% of the amount they will be spending on R&D each year," he says, "and that they give this in either cash or kind to the school of their choice" [*Electronics*, Oct. 20, p. 346]. By his reckoning, the foundation should increase the funds available to colleges and universities by $50 million to $100 million yearly, but he adds that "this is just a start, the beginning of a decade-long effort to boost their output."

Thurston's other key priority is lowering trade barriers. "We must rationalize our Government's policies toward high-technology exports," says the head of the Concord, Mass., company. "There are documented cases of American firms being denied export licenses for equipment sold without hindrance by our allies. If we are going to keep America's balance-of-trade positive, penetrate Third World markets, and

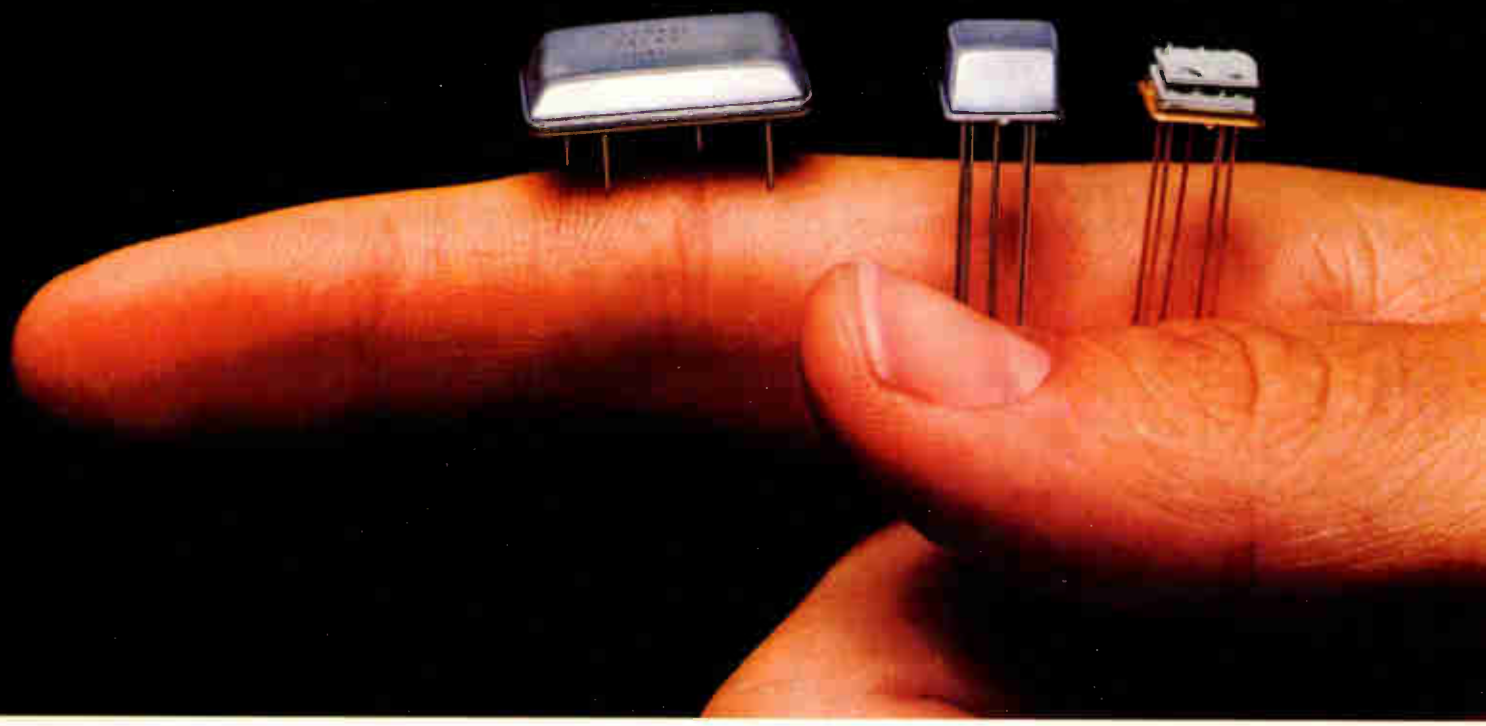
**Unplugging bottlenecks.** William Thurston wants AEA to help schools, unfetter trade.

contend with Japanese competition, we have to coax industry and Government into cooperation."

Thurston hopes there will eventually be a new mechanism to address questions about technology exports. "We really need a system for resolving the conflicts that now take place. When industry and government are on opposite sides of an export issue, there should be something like a joint, high-level government-industry board of arbitration to settle such issues fast." The hoped-for result would be increased exports without risk to national security. □

# The Power FET SSR

# Its low resistance is a real turn-on



It certainly is. We've used power FET technology to reduce the ON resistance in the output stage below 0.3 ohms. That means it can switch low level signals with no offset voltage. It also means it can handle full load currents at higher ambient temperatures.

But the low ON resistance is only one of the goodies. We've included buffering so the relay can be driven directly by CMOS as well as TTL logic. And we incorporated a Schmitt trigger in the CMOS mode to prevent false triggering in a noisy environment.

We've used some special circuits to control turn-on and turn-off times. That virtually eliminates the on-off spikes and results in very low EMI. And optical isolation is used to protect the sensitive input circuits from voltage transients.

By use of hybrid microelectronic techniques, we've been able to package all this capability in a tiny Centigrid® package (690 Series), or in a metal DIP (685 Series) which permits full current operation up to 75°C. Both are designed to meet MIL-R-28750, and are available for either AC or DC operation.

The power FET SSR. It is a major advance in SSR technology. You can use it in a wide range of low level and power switching applications. Call or write us if you want assistance or ideas.

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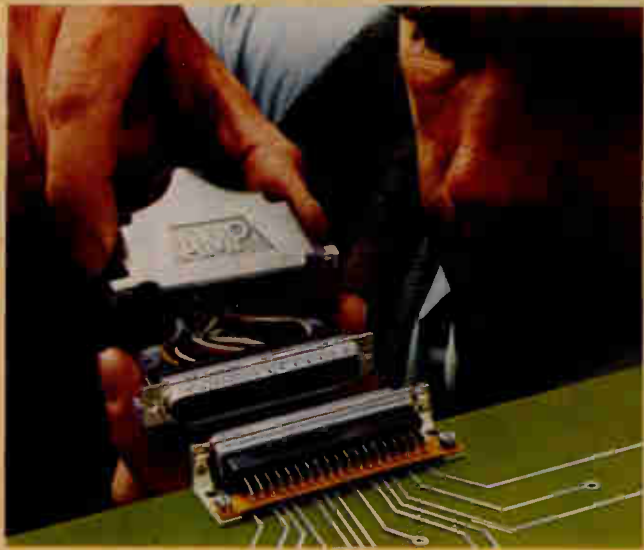
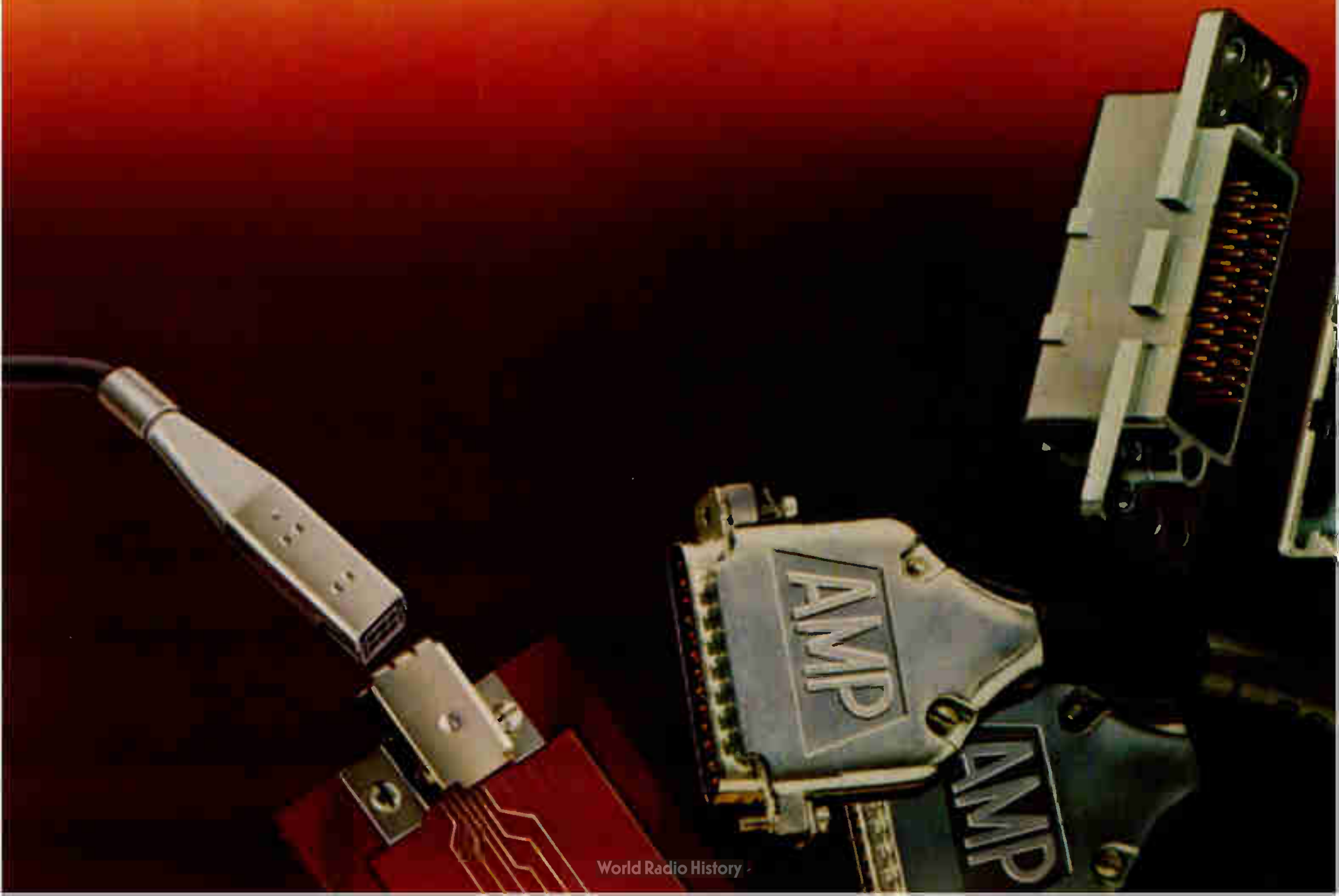


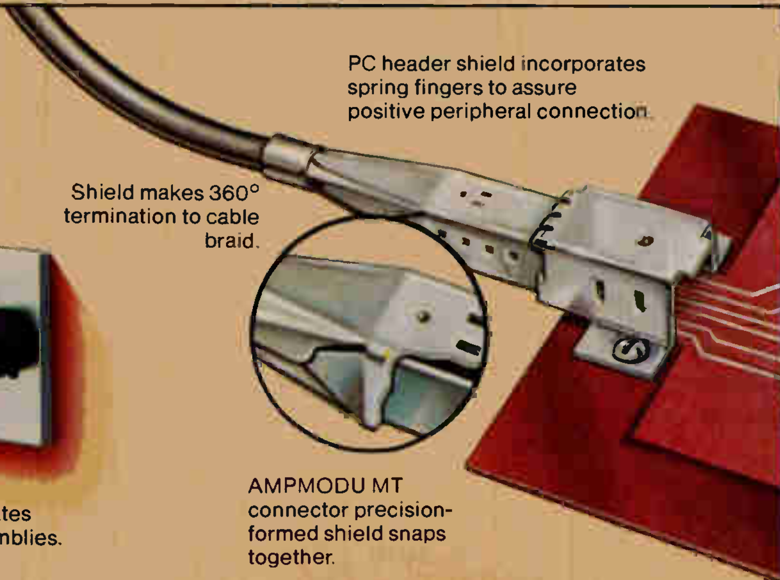

If you prefer a circular connector, our shielded version offers a positive one-turn locking ring. And for high pin counts, the CR Series gives you zero insertion force mating.

You couldn't ask for better protection.



# AMP Facts

CHAMP panel mount connector mates with IEEE 488 shielded cable assemblies.




**For more information, call the AMP Shielded Connector Desk at (717) 780-8400.**

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# BELIEVE IT OR AN EASIER WAY TO

These days, there are at least a dozen places where you could buy microprocessor peripherals.

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That's great. If you feel like spending half your time shopping around. And then trying to breathe life into the collection of spare parts you've picked up.

But if you'd rather build a system where all the pieces work together as one tight unit, then you've only got one real choice.

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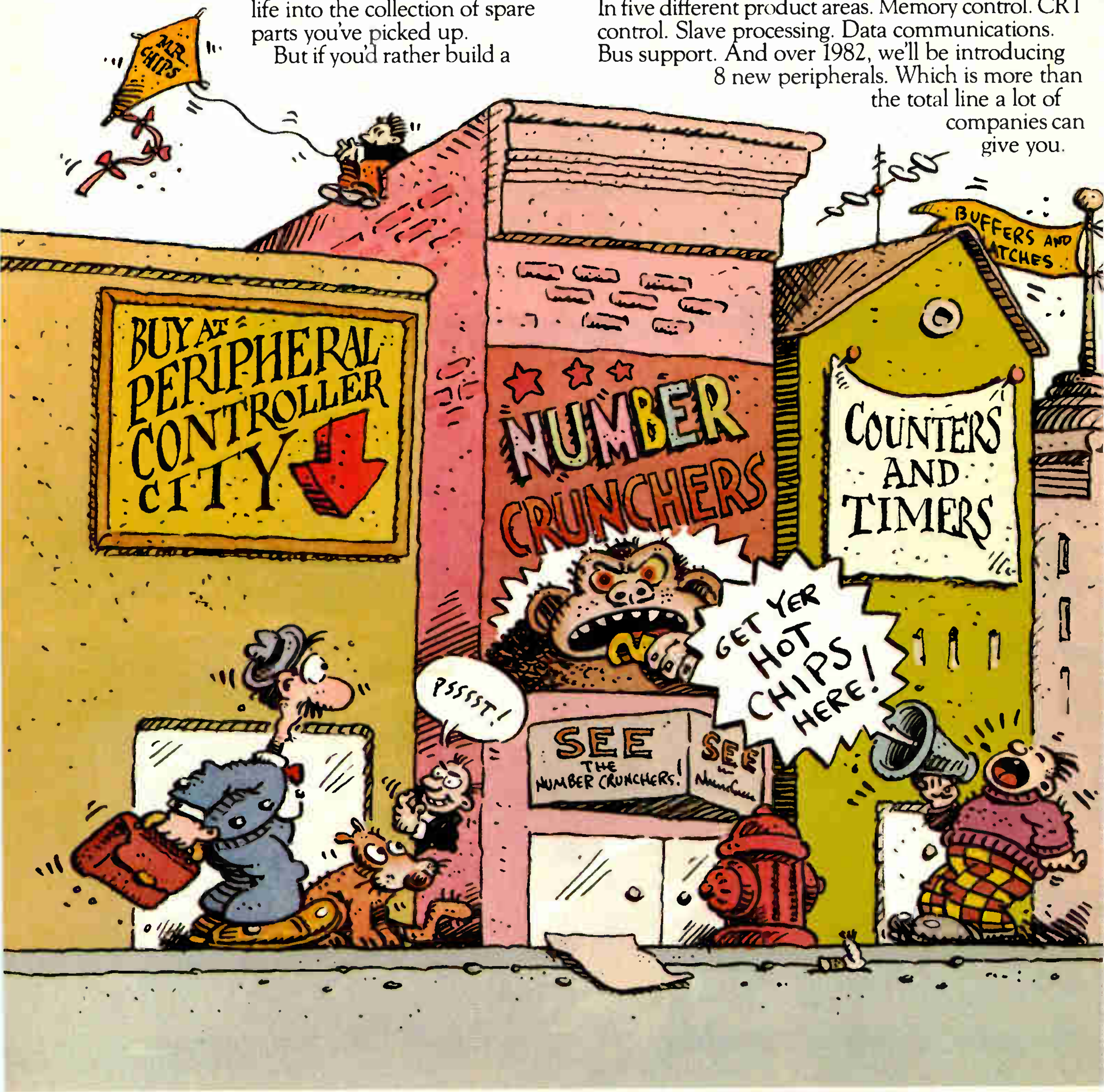

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Obviously, there's a much better chance you'll get exactly what you need from us. But that's only part of the story. Thanks to our common bus interface, each one of our peripherals is perfectly compatible with all the others. And with all our CPU's. Past, present, and future.

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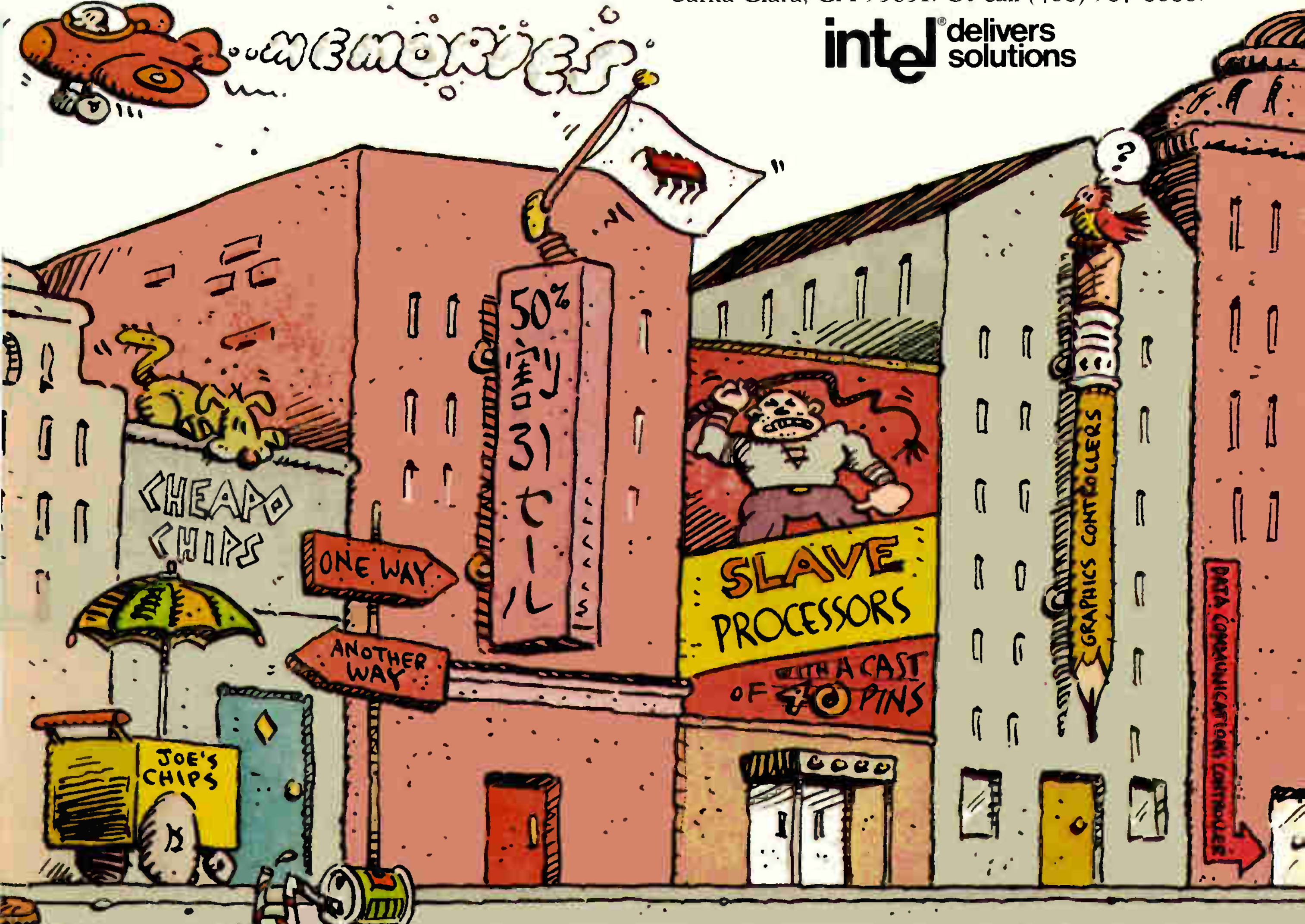


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# "If you can't measure it, you can't improve it."

*Alex d'Arbeloff, President*
Teradyne

Quality begins with knowledge. Once you know where you are and where you want to be, the rest is just a matter of commitment.

In electronics, knowing where you are means testing. Not just good-bad testing, but testing that gets inside a device and probes the subtle differences between pretty good and very good.


The subtleties vary from device to device. For high-performance memories, where the issue is usually speed, you need a test system that can set timing edges to within a quarter nanosecond. For precision D to A converters, you need a system that can integrate noise measurements over programmed time intervals. For codecs, you need a system that can measure idle channel noise in the submillivolt region.

Measurements like these are not easy, but they're not impossible. Teradyne test systems have been making tough, critical measurements for years – on digital and linear ICs, discrete semiconductors, hybrid circuits, film resistors, automotive electronic modules, analog LSI devices, and printed circuit boards.

What all this experience gives us is a sense of what really matters in the testing of electronics.

What it gives you is the kind of in-depth measurement you need to improve product quality.

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*We measure quality.*

## Editorial

# A New Year's wish list

As the electronics industries approach 1982—a year sure to be filled with pitfalls, surprises, winners, and losers—we know that deep in the hearts of the participants in this magnificently volatile marketplace lie profound hopes and fervent prayers. To these, we add our own wishes for the coming year:

■ For semiconductor-industry pundits, both on Wall Street and in company boardrooms, a chance to reassess predictions of growth through 1981 with only a short pause.

■ For U. S. semiconductor manufacturers, a way to make a profit on 16-K random-access memories selling for 80¢ each.

■ For Silicon Valley, another year without the big quake.

■ For U. S. communications equipment vendors, more orders from Nippon Telegraph & Telephone Public Corp. than they can handle.

■ For personal-computer manufacturers, another year before the Japanese invasion.

■ For the same group, S-100–compatible boards that are compatible with the S-100.

■ For the National Aeronautics and Space Administration, discretionary funds to orbit David Stockman.

■ For David Stockman, a remote magnetic-tape eraser.

■ For the U. S. Patent and Trademark Office, computerized quill pens to bring the patent search system into the 20th Century.

■ For office workers, automated, programmable, and user-friendly managers.

■ For all, a modern-day Moses to go up on the mountain to bring back tablets inscribed with worldwide videotex standards.

■ For the Pentagon, a way to base the MX without spending more on concrete and community relations than on missiles.

■ For venture capitalists, a spate of sure-thing start-up investments.

■ For entrepreneurs, a surplus of venture capitalists who do it for kicks.

■ For photovoltaic manufacturers and users, a good 5¢, 30%-efficient solar cell.

■ For the American Electronics Association, a solution to the engineer shortage.

■ For the Institute of Electrical and Electronics Engineers, confirmation that there is no engineer shortage.

■ For military suppliers, a mil spec that can be met with existing technology.

■ For engineering educators, a willingness to listen to the needs of the industrial and social communities they serve and then restructure their curricula accordingly.

■ For engineering students, a sudden influx of skilled, exciting instructors, a reduction in tuition fees, and a laboratory crammed with modern equipment.

■ For graduate schools, the same sudden influx of skilled, exciting instructors who do not care about money.

■ For test engineers, a design-automation system that slaps a designer's hand when he puts together an untestable circuit.

■ For field-service managers, a tester that tells the service technician how to get to the customer's site.

■ For Intel Corp.'s Gordon Moore, inspiration on what to do with a chip holding 1 million transistors.

■ For computer makers, natural languages that sound just like English (or French, or Japanese).

■ For makers of personal computers, customers who really want to use them to file recipes and maintain checkbooks.

■ For Texas Instruments, National Semiconductor, and Rockwell, a chorus of "I'm Forever Blowing Bubbles."

■ And finally, for all nations, their industries, and engineers, signs of progress in U. S.-Soviet arms-reduction negotiations at Geneva, so that we all may turn to more applications of electronics for the enhancement of life.

# What makes Pro-Log's new OEM cards so great?

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**Pro-Log's extraordinary quality at economical OEM prices.**

Now you can configure an economical STD BUS system with Pro-Log's three new processor cards designed especially for the OEM and featuring the 6809, 8085 and Z80A microprocessors.

Like all our STD 7000 series cards, these OEM cards are built with proven, 100% tested industry-standard components, burned-in for reliable performance. And they come thoroughly documented, including assembly prints, schematics and users' manuals.

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Every one of our STD 7000 Series STD BUS cards is backed by a two-year parts and labor warranty.

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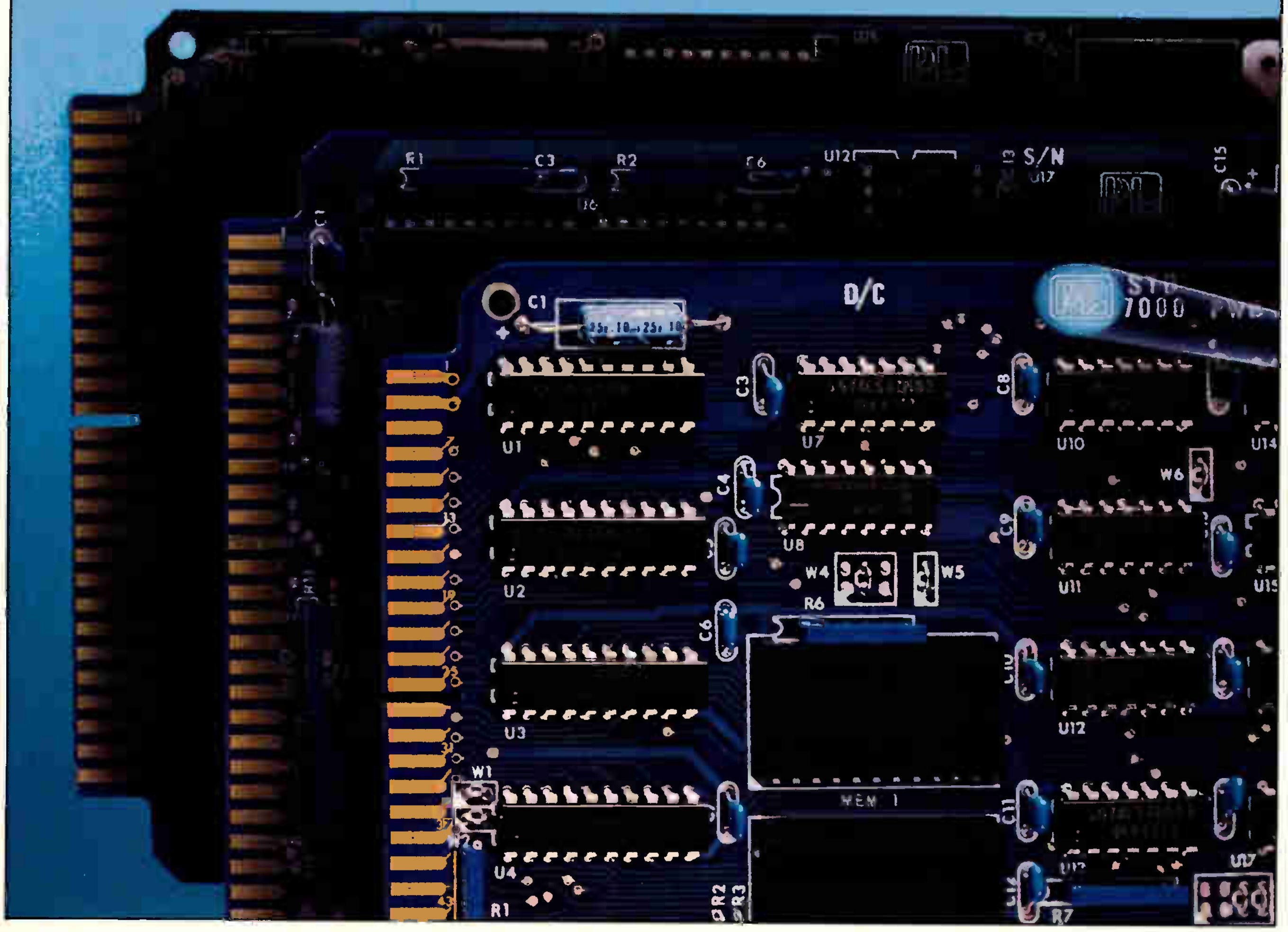

# Meetings

**5th Los Angeles Technical Symposium,** International Society for Optical Engineering (SPIE, P. O. Box 10, Bellingham, Wash. 98227), Los Angeles Marriott Hotel, Los Angeles, Jan. 25–29.

**1st Spacecraft Electronics Conference,** EIA (Frank A. Mitchell, EIA, 2001 Eye St., N. W., Washington, D. C. 20006), Hyatt Hotel, Los Angeles, Jan. 26–28.

**Advanced Semiconductor Equipment Exposition and Conference,** Electronic Representatives Association and Cartlidge & Associates Inc. (CAI, 491 Macara Ave., Sunnyvale, Calif. 94086), Convention Center, San Jose, Calif., Jan. 26–28.

**Annual Reliability and Maintainability Symposium,** American Society for Quality Control, IEEE *et al.* (H. C. Jones, Westinghouse, MS 3608, P. O. Box 1521, Baltimore, Md. 21203), Biltmore Hotel, Los Angeles, Jan. 26–28.

**Advanced Plasma Technology Conference,** E. T. Electrotech, Inc. (Walter Becker, E. T. Electrotech, 40 Oser Ave., Hauppauge, N. Y. 11788), Sheraton-Waikiki Hotel, Honolulu, Hawaii, Jan. 26–28.

**Workshop On Reliability of Local Networks,** IEEE (Robert S. Swarz, Prime Computer, Inc., 500 Old Connecticut Path, Framingham, Mass. 01701), South Padre Hilton Resort, Brownsville, Texas, Feb. 3–5.

**16th Annual Television Conference,** Society of Motion Picture and Television Engineers (Lynne Robinson, SMPTE, 862 Scarsdale Ave., Scarsdale, N. Y. 10583), Opryland Hotel, Nashville, Tenn., Feb. 5–6.

**5th European Exhibition and Congress for Telecommunications,** Online GmbH (Postfach 10 08 66, D-5620 Velbert 1, West Germany), Düsseldorf Fairgrounds, West Germany, Feb. 8–11.

**Aerospace and Electronic Systems Winter Convention,** IEEE (Tom S. Schuler, Rockwell International, P. O. Box 3105, Anaheim, Calif. 92803), Sheraton-Universal Hotel, Hollywood, Calif., Feb. 9–11.

**International Solid State Circuits Conference,** IEEE (L. Winner, 301 Almeria Ave., Coral Gables, Fla. 33134), Hilton Hotel, San Francisco, Feb. 10–12.

**2nd Conference on High-Frequency Communications Systems and Techniques,** The Institution of Electrical Engineers, (Savoy Place, London, England WC2R 0BS), Savoy Place, London, Feb. 15–16.

**9th Plating in the Electronics Industry Symposium,** The American Electroplaters' Society (Jack Sheehan, 1201 Louisiana Ave., Winter Park, Fla. 32789), Sheraton-Atlanta Hotel, Atlanta, Feb. 16–17.

**Nepcon '82 West,** Cahners Exposition Group (222 West Adams St., Suite 999, Chicago, Ill. 60606), Anaheim Convention Center, Anaheim, Calif., Feb. 23–25.

**Compcon Spring,** IEEE (Harry Hayman, P. O. Box 639, Silver Spring, Md. 20901), Jack Tar Hotel, San Francisco, Feb. 26–28.

**9th Communications Satellite Systems Conference,** American Institute of Aeronautics and Astronautics (1290 Avenue of the Americas, New York, N. Y. 10104), Town and Country Hotel, San Diego, Calif., March 7–11.

## Seminars

**Millimeter Wave Technology,** Palisades Institute for Research Services Inc. (201 Varick St., New York, N. Y. 10014), Sheraton Harbor Island Hotel, San Diego, Feb. 1–3, and Holiday Inn, Washington, D. C., March 29–31.

**Programmable Controllers Seminar,** Society of Manufacturing Engineers (Darlene Corp, SME, P. O. Box 930, Dearborn, Mich. 48218), Radisson St. Louis Hotel, St. Louis, Feb. 2–4.

# WIND YOUR Ps & Qs

To give TDK's originally shaped PQ*core a winding is to understand the sheer perfection of its design. The PQ core's centre pole is circular which makes it far more adaptable to winding than the square variety. Another advantage is the large cross-sectional winding area which allows for bigger outputs than the square type. Also, the magnetic shield effect is high enough to enable transformers to be designed with minimal power loss.

Bobbins and clips are also TDK originals. The bobbin, made of UL 94V-0 material, has as many as 12 or 14 pins which makes it easier to terminate the winding.

The PQ core is perfectly suited to the new breed of high power and high quality transformers.

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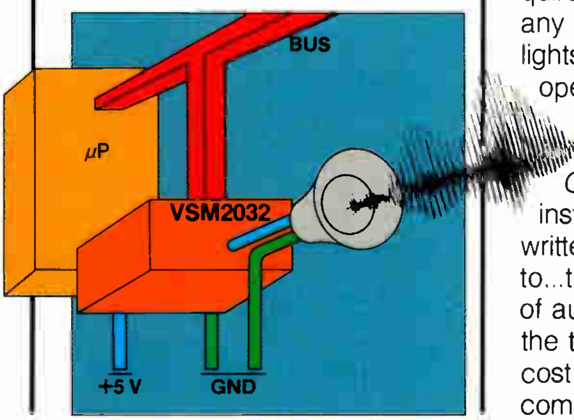
**The human speech process... an amazingly complex system has just been reduced to a single chip...the *Orator*... speech synthesis approached from an entirely new perspective by the people who know what they're talking about... General Instrument.**

## Speech data compression without giving up low cost.

Although several technologies of speech data compression exist, each has its own inherent drawbacks. In fact, data compression is, in its simplest form, a trade-off of speech quality versus ROM capacity. To gain on one end, you sacrifice on the other. General Instrument's engineers, were, on the other hand, successful in utilizing Linear Predictive Coding (LPC) for data compression with minimal ROM support. That only left the question of speech quality. To obtain truly natural speech, a 12 pole cascade filter is used to implement a mathematical model of the human vocal tract so that Aunt Mary sounds exactly like Aunt Mary and not like Uncle Walter.

Until *Orator* was born, speech synthesis devices fell short of reproducing any human voice... male, female or child, with natural inflection, tonality and essence...and maintaining *low cost.*

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General Instrument's world-wide speech labs are available to meet the challenge of your specific speech synthesis project. Already, vocabularies in German and Japanese are being used with *Orator* technology, and as far as we're concerned, with *Orator*...you will have the last word. For more information, applications assistance and a demonstration (including Linear Predictive or allophone coding techniques) call the Microelectronics Division office nearest you.

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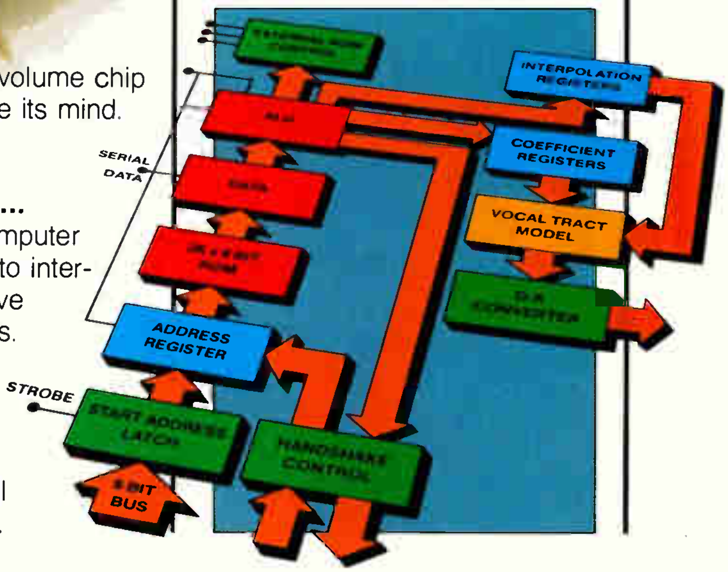
***Orator...the off-the-shelf module that talks by itself...*** a complete voice synthesis system that you plug into a power supply and speaker to have it speak.
The VSM2032...you can have it talking almost as fast as you can read this ad.

***Orator* SP-0250...for the designer who knows what he wants to say.** A single chip speech synthesizer you program yourself and interface with any standard micro-computer and external ROM.

The low-cost, high volume chip that lets you change its mind.

***Orator* SP-0256 Speech Processor...** the talking microcomputer that you need only to interface with inexpensive support components. It's all in one chip... a 12 pole cascade filter, 16K ROM, a micro-controller and digital to analog converter.

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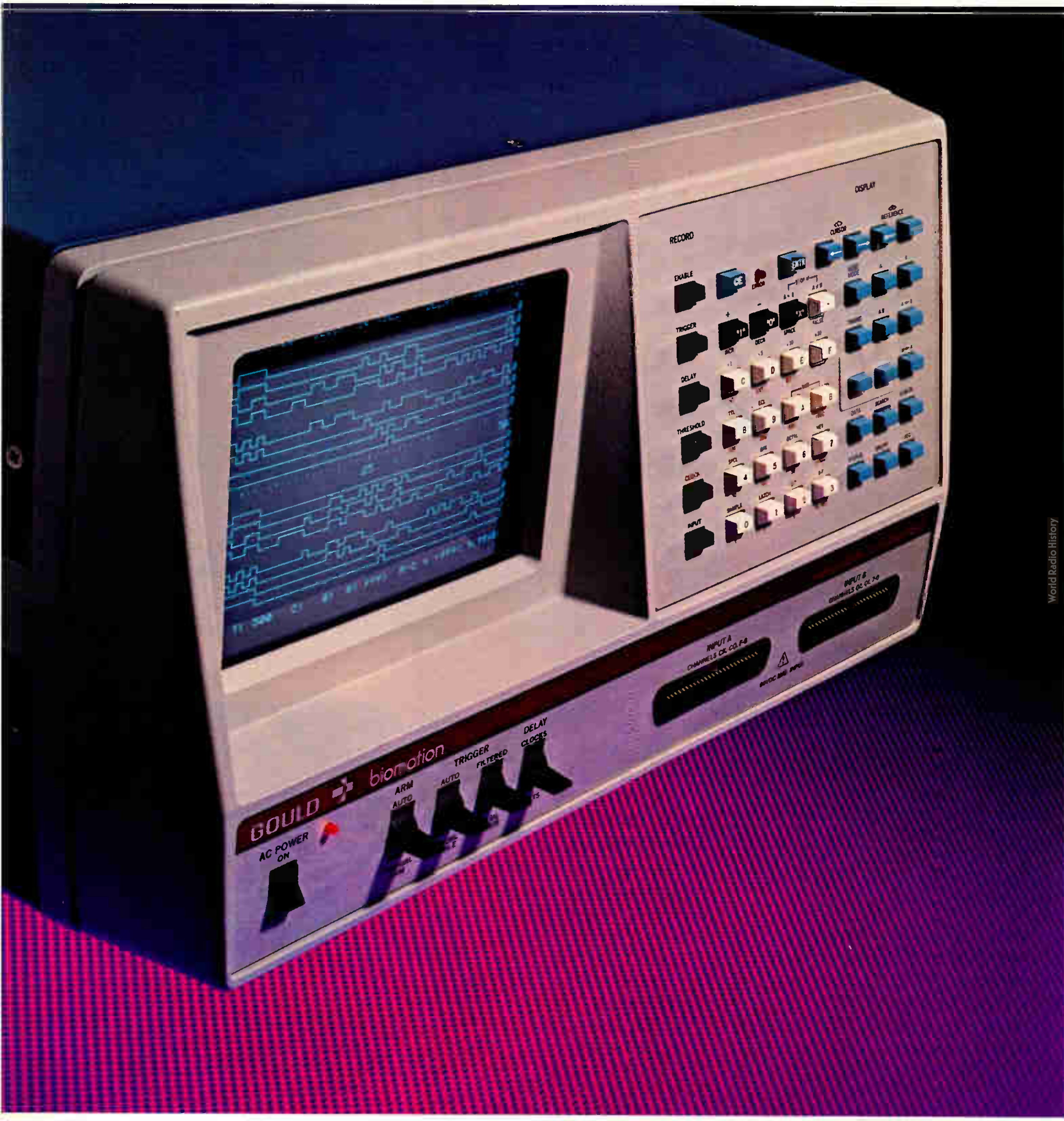

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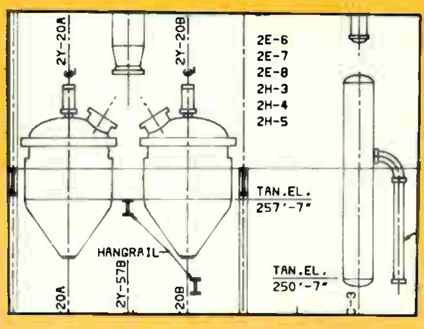


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**Sharp to transfer C-MOS technology to Rockwell**

Watch for Rockwell International Corp. to start second-sourcing a complementary-MOS version of Motorola's 6800 microprocessor next year. Rockwell is well along in negotiations with Sharp Corp. to acquire the Japanese firm's C-MOS production technology, a know-how transfer that will require—and presumably will get—approval from the watchdog Ministry of International Trade and Industry (MITI). **The deal underscores the advances in semiconductor technology that Sharp and other Japanese producers have wrought** over the past decade. The last time the two companies transferred technology in the late 1960s, it was Rockwell that sold p-channel MOS production know-how to Sharp.

**MIT, Government try to boost robotics research**

With funding from the office of Naval Research and the Defense Advanced Research Projects Agency, the Massachusetts Institute of Technology's Artificial Intelligence laboratory in Cambridge, Mass., has declared 1982 the year of the robot. **The goal is a "quantum jump in robotics," and to that end, the laboratory will invite robotics experts to Cambridge from industry and academe worldwide.** The kickoff of a multiyear effort, the plans for 1982 include new seminars and courses at MIT and a new journal, the International Journal of Robotics Research, which would collect research reports now published in a variety of places. There also will be two main research goals during the months to come: design and control of a multifinger robotic hand with tactile sensors and the design of a high-level, task-oriented robotics programming language.

**Futuredata to offer emulation tools for Intel processors**

Beefed-up development-system support for Intel Corp.'s 16-bit microprocessor family is coming from the Futuredata division of GenRad Inc., complete with plug-in in-circuit-emulation modules and software. **The system will permit the first simultaneous emulation of Intel 8086/87 and 8088/87 processor pairs,** says the Culver City, Calif., division. Along with co-emulation, modules being offered have a 5-MHz speed for the 8088 and 8 MHz for the 8086—higher than Intel's own MDS packages. Meanwhile, Futuredata itself is being spun out of GenRad. Investors include division officers, with the deal expected to be closed early in 1982.

**$2,995 pulse generator to take on HP unit**

Poised to challenge the industry-standard Hewlett-Packard 8080 system pulse generator is a 1-GHz model to be introduced for $2,995 by tiny Colby Instruments Inc. of Santa Monica, Calif. **A key specification in the model PG1000 is a blazing 150-ps rise-fall time** in emitter-coupled-logic output, said to be critical for research and development and for testing new-generation computer and communications gear. The TTL output has a 350-MHz repetition rate with a less-than-750-ps rise-fall time. The generator will be ready in February, Colby says.

**VRTX system signed for National 16000**

The dream of software components is a step closer to reality with the adoption by National Semiconductor Corp. of the VRTX operating system, which is a read-only-memory-based real-time system for embedded applications. Produced by Hunter & Ready Inc. of Menlo Park, Calif. [*Electronics*, Oct. 6, p. 48], **VRTX dovetails neatly with National's ROM library concept** for its 16000 16-bit microprocessor, in which software modules can be permanently installed.

# Electronics newsletter

**Diffraction-grating technique shapes laser radar beams**

The Massachusetts Institute of Technology's Lincoln Laboratory in Lexington, Mass., has developed a low-cost, low-loss method of converting a circular–cross-section laser beam into one with a highly elliptical cross-section. Laser radar systems need such elliptical shapes for air search or target acquisition applications, where it is necessary **to sweep large volumes of space quickly rather than to generate the most accurate elevation data.** The new method uses a diffraction grating to vary phase relationships within the beam and two polycrystalline gallium arsenide lenses to control final beam shape. The approach has been used successfully with carbon dioxide lasers and has achieved an efficiency of about 90%, higher than that scored by mask or polarization-rotation techniques, as well as lower in cost. Unlike most present polarization-rotation techniques, the new system also is electrically passive, requiring no current.

**Chinese seeking 3-in.-wafer gear**

The Peoples Republic of China is shopping for 3-in.-wafer processing equipment to install at two newly constructed semiconductor plants in Shanghai and in the city of Wuxi in Jiangsu province. "They have made up their minds they are going to buy a totally intact 3-in. line somewhere, with or without U. S. approval," says William I. Strauss, an official with Integrated Circuit Engineering Corp., Scottsdale, Ariz., who recently returned from a client-sponsored Chinese tour. **The Chinese currently rely upon equipment they have manufactured themselves** for processing 1.5- and 2-in. wafers, able to produce about 4-to-5 $\mu$m minimum geometries, Strauss notes. Though equipment for handling 3-in. wafers could likewise be manufactured in China, it would require a time-consuming retooling process, he explains. The two new semiconductor plants—which have already been completed and stand waiting for equipment—are expected to fulfill more than half of China's near-term needs.

**Program promising for IC verification**

Officials at Argonne National Laboratory, Argonne, Ill., believe that a software program originally developed for proving mathematical theorems may have applications in a variety of fields including the verification of integrated-circuit designs and application software programs. Known as AURA (for automated reasoning assistant), **the program has already been used in the design of very simple multilevel logic devices.** The 10-year-old program—which was developed originally by a team from Argonne's Applied Mathematics division and from Northern Illinois University—currently runs on IBM 370-class machines and typically requires between 250 and 650 kilobytes of memory space to solve a given problem, says Larry Wos, an Argonne official. A more portable version of AURA, written in Pascal for use on smaller computer systems, is under development, however, and could be available as soon as next summer, Wos says.

**Northern pushes up Displayphone production**

Demand has been so great for Northern Telecom Inc.'s experimental desktop Displayphone that the company has started U. S. manufacturing **more than a year and a half ahead of schedule.** When Northern Telecom announced test-marketing plans for 250 prototypes of the unit [*Electronics*, March 10, p. 41], it planned to start volume production first in Canada, with U. S. manufacturing to follow 6 to 12 months later. But the number of test units quickly grew to 800 following a flood of requests, and mass production has begun both in Canada and Minneapolis.

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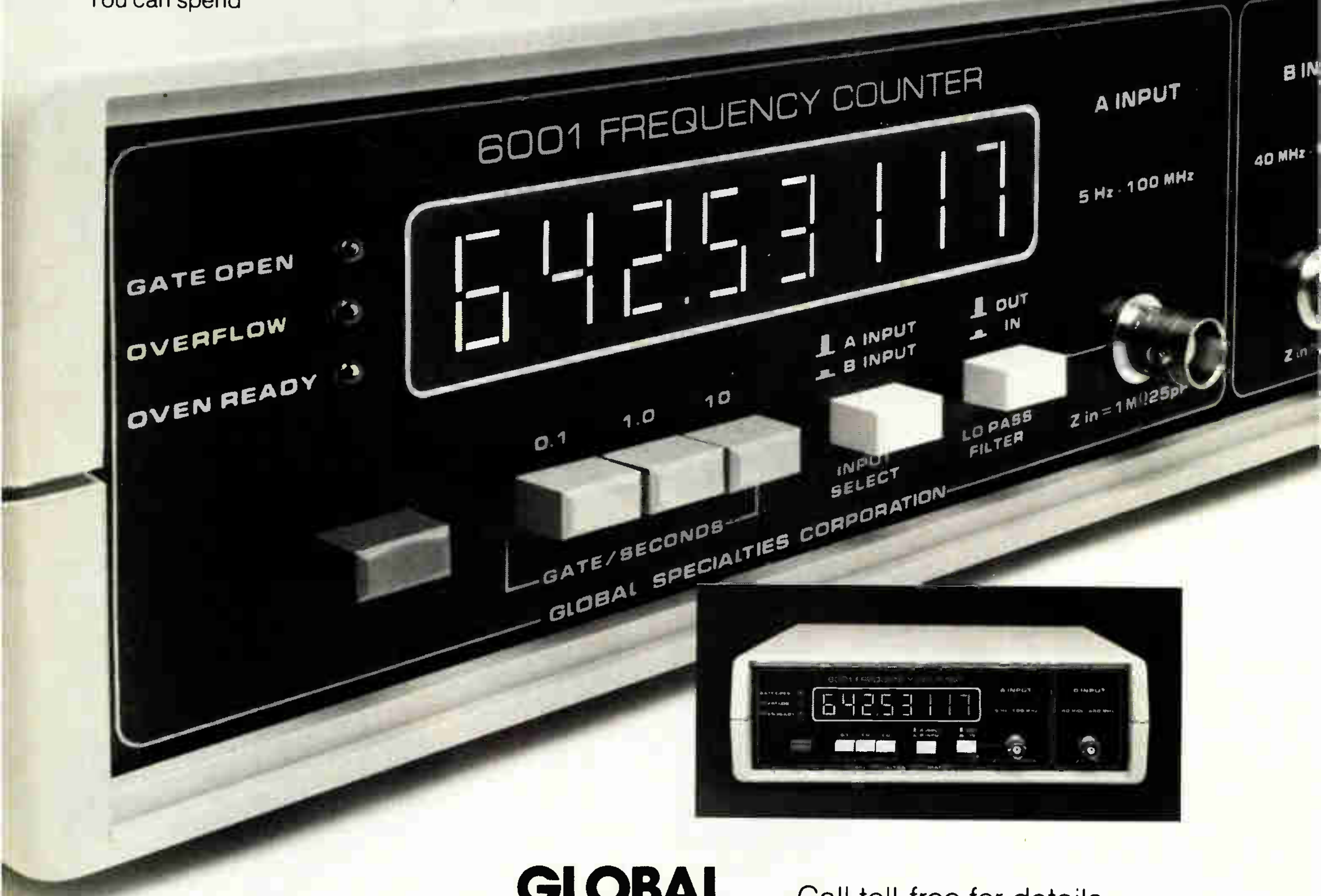


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# Deposition yields insulating oxides for ICs at low temperatures

*by Larry Waller, Los Angeles bureau*

Emerging from Hughes, process works between 50°C and 300°C, yielding uniform films of many materials

**For years, semiconductor** manufacturers have hunted without much success for a low-temperature dielectric oxide whose application does not itself change delicate integrated-circuit properties. Such an approach just emerging from military research laboratories at Hughes Aircraft Co., therefore, already is stirring keen industry interest.

Dubbed Photox, for photochemical vapor deposition of oxide, the Hughes process is unique among chemical-vapor–deposition techniques. It relies solely on selective absorption of light for the excitation of oxygen, in contrast to high-temperature-thermal and radio-frequency plasma approaches.

A long list of troubles spring from the high temperatures (450°C and up) presently needed to deposit silicon dioxide. These problems include the unwanted lateral diffusion of dopants that inflates device area, distorted channel lengths that pull device threshold voltages off target, and even lowered resistance to the effects of radiation.

At pressures less than 1.0 torr and temperatures between 50°C and 300°C, depending on the substrate material, electrically neutral atomic oxygen is photogenerated from nitrous oxide by the action of ultraviolet light in the range of 1,700 to 2,000 angstroms. Liberated from nitrous oxide, the oxygen atoms oxidize vapors like silane or trimethyl aluminum to form silicon dioxide or aluminum oxide, which are then deposited on the wafer surface.

**Outstanding.** "We think it's the answer since it provides outstanding step coverage and exceptionally low pin-hole densities," says inventor John W. Peters, senior scientist at Hughes' Electro-Optical division, Culver City, Calif. He has demonstrated the uniform step coverage necessary to prevent thin spots that can cause electrical breakdown.

Results with a 1.0-micrometer-thick silicon dioxide film deposited over 1.0-μm polysilicon steps are shown in the photograph. Nearly perfect films with less than two pin holes per square centimeter are possible, Peters believes.

The need to protect radiation-hardened characteristics of devices for military programs led Hughes in 1978 to low-temperature photochemical vapor deposition. "Photox does not generate charged particles and so totally eliminates the radiation problem present with plasma processing," Peters claims.

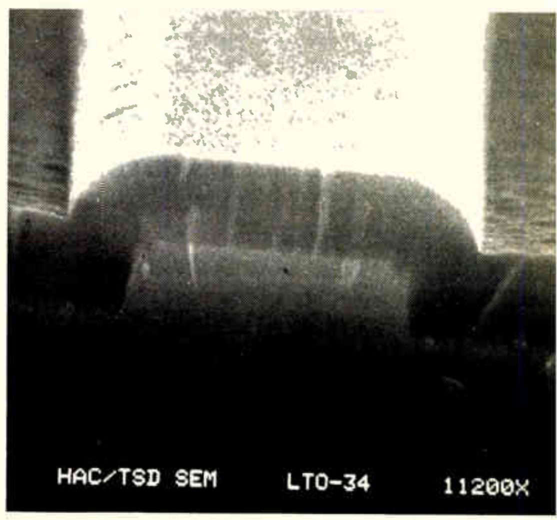
Of more interest to commercial device makers, the process fits in well with high-density–device technology. Besides allowing better control over dopants, it prevents another pesky problem associated with high-temperature dielectrics. This problem is the growth of hillocks, or bumps, in aluminum that punch through and damage double-level metallization layers.

Although Hughes went public with Photox only this month at the International Electron Devices Meeting, word of mouth earlier brought an avalanche of inquiries, according to Peters. For instance, Larry Pollock, process-development manager for bipolar memory at Advanced Micro Devices Inc. Sunnyvale, Calif., says, "It's got advantages over anything I see now."

Pollack's only reservation: the deposition growth rate of some 400 angstroms per minute—that depends on the intensity of the UV radiation—might be too slow for quantity fabrication. But he notes the low-temperature technique could begin the insulating process, then existing processes could take over.

**Product.** A major maker of chemical-vapor–systems, Tylan Corp., Carson, Calif. is working on high-throughput equipment. It is set to introduce Photox units for R&D costing about $100,000 each.

Hughes has tested the silicon diox-




**Good-looking.** Photograph taken with scanning electron microscope reveals excellent unformity in 1-μm-thick silicon dioxide film deposited over 1-μm polysilicon steps using Hughes' Photox process.

ide process for forming gate insulators on a number of semiconductors, including silicon and indium phosphide, with excellent results. Photox also works well with oxides of gallium, germanium, titanium, and tungsten, among others. Hughes licenses the process exclusively.

## Avionics

# One chip interfaces with airborne network

Users of the military's standard local network for aircraft communications will soon have a one-chip interface with which to tie in their electronics gear. In addition, it will handle the Manchester protocols added to the network standard, MIL STD 1553B, to boost network noise immunity.

The chip was designed by Grumman Aerospace Corp., Bethpage, N. Y., a builder of aircraft and airborne electronic systems, in cooperation with Standard Microsystems Corp. in nearby Hauppauge, which is fabricating it. Grumman wanted a single chip that would replace the bulky and expensive TTL and hybrid packages with which the interface is now usually being implemented.

In existence since 1973, the standard is set down in a triservice document that establishes requirements for serial, digital, command-response, and time-division–multiplexing techniques on aircraft. Given the long lead times in the military, it has only recently come into widespread use. The interface is going aboard such aircraft as the F-16 and F-18 fighters and the Lamps (light airborne multipurpose system) helicopter, and it is also destined for practically all new avionics systems requiring local networks.

**Entry point.** The interface chip is the network entry point to the 1-megabit-per-second data bus for the on-board computer that controls the aircraft and communicates with remote systems in a master-slave mode. The network is used, for example, for updating guidance systems of missiles with the aircraft's ever-changing location relative to a distant target.

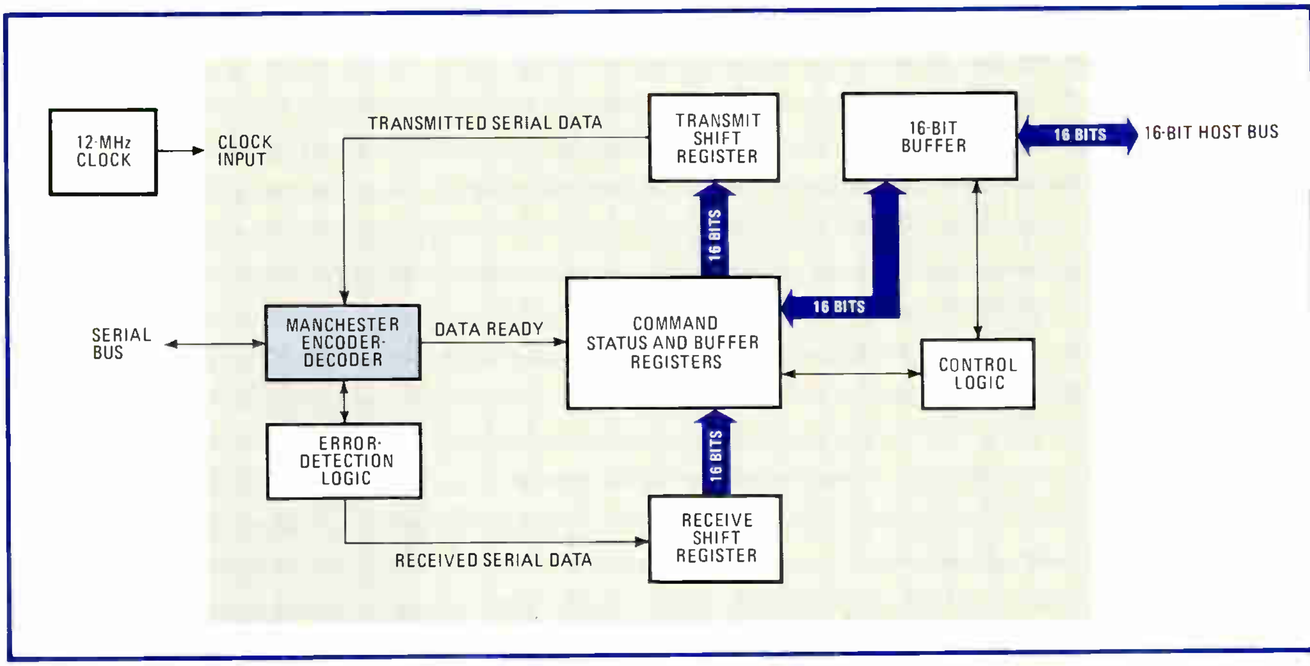
Standard Microsystems already had a chip for the initial version of the network, made obsolete by the B-version of the standard. In particular, the new chip includes Manchester data encoding that increases the network's noise immunity and simplifies the part as well.

A well-known technique, Manchester encoding supplies a timing pulse train with the data, which not only makes it easier to extract data but simplifies the circuitry at the receiver because timing signals need not be regenerated.

"The 1553B mil spec has been a moving target over the last few years mainly because of the communications protocols," says Art Sidorsky, senior vice president at SMC. "But now it has finally been settled."

**Either/or.** Standard Microsystems' bus-interface chip functions in either a master or slave capacity that is switchable by a codable read-only memory. That option and the Manchester encoding give the part its relatively large die area. At 55,000 square mils, it is 50% larger than the earlier 1553 chip and has a large gate count—some 7,000. The entire chip is fabricated with n-channel MOS technology using 4-micrometer design rules.

The chip has a 16-bit parallel connection to the host computer and provides direct-memory access under interrupt control. It detects errors involved with improper Manchester codes, synchronization, and parity, as well as catching no-response con-




**Network chip.** A single chip interfaces with the 1553B military-standard local network for avionics applications. The 16-bit on-board host computer is interfaced in parallel with a serial bus running throughout the aircraft. Manchester encoding increases noise immunity.

ditions in the remote slaves.

Others have attempted to fabricate VLSI solutions to the bus interface presented by the new specifications, but none has yet done it on a single chip. Harris Corp., Melbourne, Fla., has a single chip that performs the slave function, but not the master. And Smiths Industries Aerospace & Systems Co. in London has a four-chip set in complementary-MOS that can be used in various combinations to implement master and slave functions.

Standard Microsystems will have the part in a 40-pin dual in-line package in the second quarter of 1982. It will also be sold by Grumman, which is now deciding just how to market it, says John Cavin, technical specialist at Grumman's Engineering Development Center. The potential exists for sales of anywhere from 10,000 to 100,000 chips per year, he says, depending on whether industrial applications such as robotics also select the chip. Price is not yet set, but for now, Sidorsky puts it somewhere in a broad range between $100 and $200. **-R. Colin Johnson**

## Software

# Unique tools add to 16-bit capabilities

Reaching into its minicomputer bag of tricks, Texas Instruments is unveiling unique software tools for one of its 16-bit microprocessors—the 99000. These tools enable programmers to manage the 99000's large memory space (16 megabytes with 24-bit addressing) for multitasking operations and to use a Pascal high-level language to debug programs without resorting to assembly language.

Moreover, a single program in this high-level language can have both compiled and interpreted parts. This ability allows programmers to mix the two modes, thus optimizing different parts of the program for speed or memory conservation.

Called Advanced Microprocessor Pascal, the new tools are simply a natural evolution of processing development, explains Thomas Miller, manager of TI's microprocessor development systems in Houston. Memory management schemes and debugging in high-level languages have all been possible in the minicomputer and mainframe world, he points out. For TI it was a matter of transferring to microcomputers the software expertise gained as the U. S.'s No. 4 minicomputer maker—its 990-series minicomputer was introduced in 1971.

**Executive.** Memory management is handled by a binder utility called RXMAP that automatically assigns data and program slots in high-speed semiconductor main memory and then keeps track of them. Generally, this memory tracking in the microprocessor world must be set up literally by hand with a pencil and paper.

Miller describes RXMAP as a library of real-time executive modules managing all resources that are local to the 9900/99000 system bus, with message channels supporting multiprocessing. These channels allow several execution sites to coordinate their activities and communicate asynchronously.

The executive includes a scheduler, memory and communications managers, and routines for starting and stopping processes. Its memory requirements range from 1.5 to 6 kilobytes, depending on the number of modules.

A debugging feature is not yet available but will soon be out in a version of RXMAP called RXBUG. "It is time-consuming to write microprocessor Pascal and then, after it has been compiled and located in memory as a bunch of machine instructions, to figure out what may have gone wrong," Miller says. "We have what's called 'source-level debug.' It's faster and has been available to larger-machine users for years."

**One thing more.** The third new capability that TI had added is peculiar to the microprocessor world. Switching between the native (compiled) and p- (interpreted) modes uses memory space efficiently. Some 90% of a computer system's time may be spent on only 10% of the code, according to accepted industry figures. Putting those critical elements into compiled code speeds up the computation by a factor of 3 to 10, says Miller, although it will take up to twice as much memory.

This sort of tradeoff could prove attractive in industrial-control applications. Memory is often a less critical commodity in the larger-scale computer systems, which is why they are usually totally compiled.

Primarily for the 99000, the advanced Pascal will also operate with TI's 16-bit 9900 and 9995. Prices range from $3,200 for a floppy-diskette version to $3,900 for a hard-disk one. RXMAP is available separately. **-J. Robert Lineback**

## Packaging

# Decoupler sits right in lead frame

Casting about for new applications for its multilayer ceramic chip capacitors, AVX Corp. has hit upon something unusual: memory-chip lead frames with decoupling capacitors built in.

Adding capacitors is a straightforward technique for preventing transients generated by high-speed switching from feeding back through the power supply and disturbing the rest of the system. It all becomes less straightforward, however, when the transients are so large and sharp that the inductance of the capacitor's leads and circuit-board wiring can no longer be ignored. This is the case with the new high-speed 16- and 64-K dynamic random-access memories. Lead impedance can become so high that the capacitor no longer acts to short the transients.

**In between.** AVX mounts the decoupling capacitor between the RAM, which operates from a single power supply and the lead frame's flag, the surface to which the RAM is usually die bonded. This holds lead and wiring length to an absolute minimum, points out Elliott Philofsky, vice president of technology at

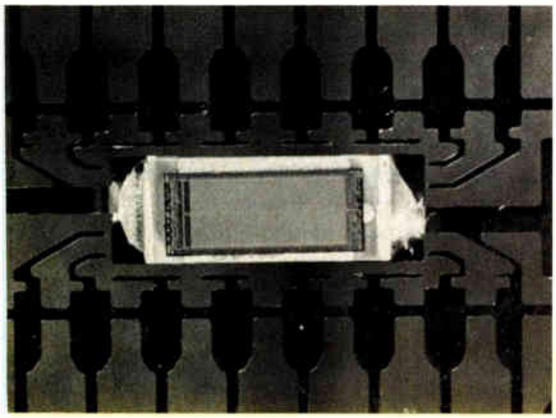
AVX's corporate research and development labs in Myrtle Beach, S. C. Actually, the RAM rests atop the capacitor in a lead frame, he says. The inductance introduced by the decoupling capacitor is far below the 10 nanohenries the firm calculated as the maximum tolerable.

AVX calls its decoupling technique BitGuard. So far, it has worked with frames for 16-lead dual in-line packages, as shown in the photo. In a standard frame, the flag floats electrically. But with the new approach, the flag is split in half: pin 8 (+5 volts) is connected to one end of the flag and pin 16 (ground) to the other. A multilayer capacitor ranging between 0.1 and 0.5 microfarad is bonded between the two halves with solder or conductive epoxy. A 16-K or 64-K MOS memory chip is then die-bonded to the capacitor's top surface and the memory's input/output pads are conventionally wire-bonded to the frame.

Comparative power supply noise tests run by AVX on a 16-K 2118 RAM have shown a 3:1 noise reduction when the internal decoupling capacitor is used instead of conventional external decoupling, Philofsky asserts. The company, which had been supplying its multilayer chip capacitors largely for hybrid thick- and thin-film circuits, will supply the BitGuard devices either separately or mounted in the lead frames. The same idea can be applied to other packaged digital and linear integrated circuits, Philofsky says. The price of the capacitor, heavily dependent on quantity, is in the $1 range.

AVX, one of the largest suppliers of chip capacitors for hybrid thick- and thin-film circuits, expects full production of the lead frames in January. The first U. S. integrated-circuit maker will also be ready to introduce a 64-K RAM with BitGuard, says Philofsky. **-Jerry Lyman**

**Underneath.** It's difficult to see, but AVX's ceramic chip decoupling capacitor is beneath this rectangular 64-k bit RAM. Both rest in a 16-pin lead frame.



## Communications

# Dial-up calls coming to airlines

By late next year, passengers on many U. S. long-distance commercial flights may make direct-dial telephone calls to the ground. AirFone Inc. is installing the system, and Western Union, which owns 50% of AirFone, will service and maintain the equipment and ground stations.

Calls will be transmitted from the planes in the 899-to-901-megahertz band and signals from ground stations in the 944-to-946-MHz band. A microcomputer-controlled receiver system in the plane will focus on a ground station by measuring the doppler shift of a pilot frequency each station sends out. Each station will be assigned 1 of 10 such frequencies.

The frequency with the largest doppler shift will help define the farthest usable station. Which station is most usable depends on the strength of the received signal, as well as the value of its doppler shift coupled with each station's known position relative to the aircraft.

Interestingly, the man behind Washington, D. C.-based AirFone is John D. Goeken, its president, who back in 1973 formed MCI Corp., the first specialized common carrier to go into competition with American Telephone & Telegraph Co. for intercity phone calls. As before, Goeken is resorting to off-the-shelf technology to implement his service.

Single-sideband transceivers, using the same type of amplitude companders as in standard telephone systems, will be installed at 26 ground stations. These stations will automatically switch the calls into the ground telephone network.

As the plane moves through the air, the closest ground station will be continually monitored and its memory location changed. Goeken says that no calls will be transferred from one ground station to the next, as in present experimental cellular mobile-radio schemes.

A plane should be able to maintain adequate contact with a ground station for at least 20 minutes, he says. Each station will be able to accommodate thirty-one 3-kilohertz-wide channels for the calls.

**Credit calls.** A would-be caller aboard an aircraft simply inserts a major credit card into a telephone. Billing will be handled through the card at a rate of $7.50 for the first 3 minutes and $1.25 for each minute thereafter. AirFone is also considering making calls to planes possible and, if needed, may equip planes with a modem for data communications to the ground.

Of course, there is also the question of whether the service is necessary. Goeken believes it will be, citing studies showing that 20 to 30 calls would be made for every 100 passengers on board. So far, a dozen airlines, including American, Trans World, and United have signed up for the service. **-Steve Zollo**

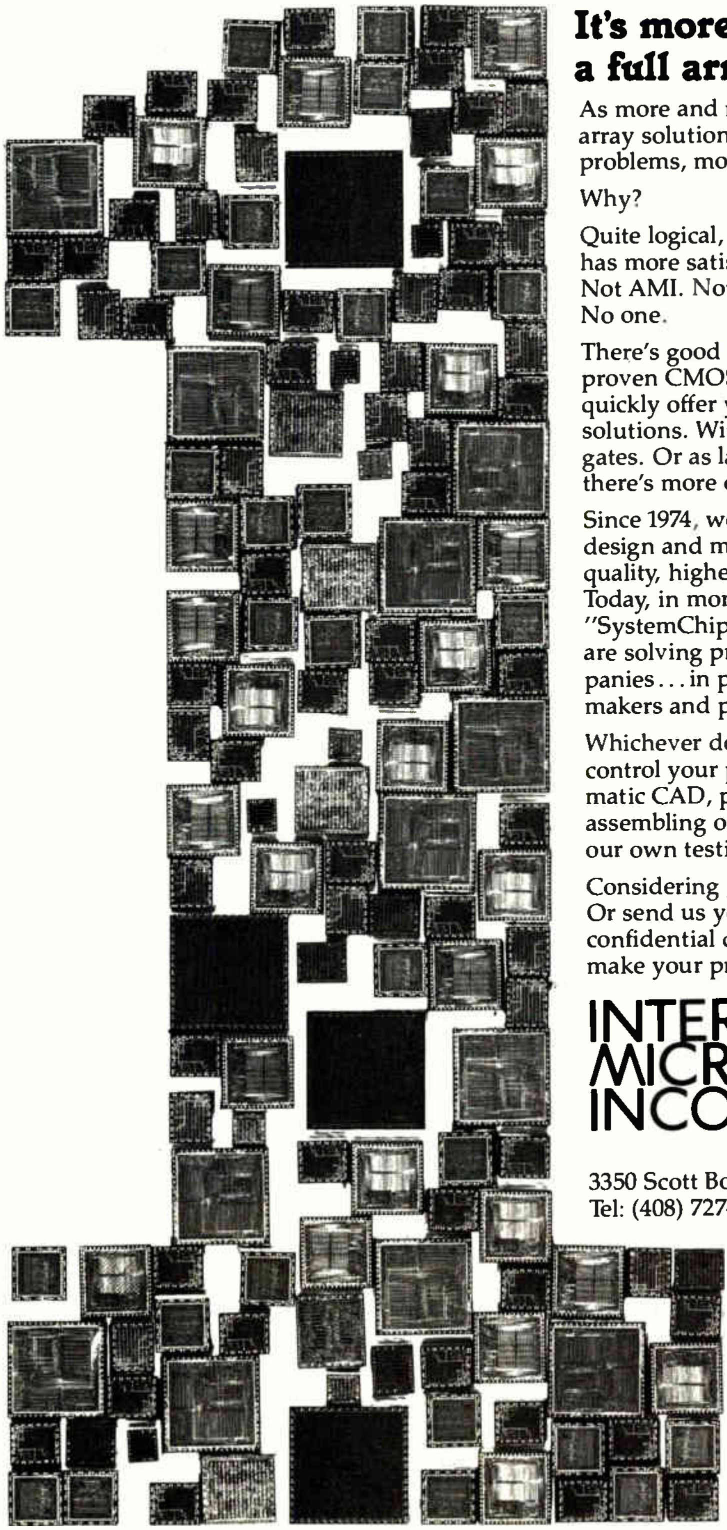
## Education

# Industry group to fund Ph.D.s

Acknowledging a shortage of basic research and Ph.D. graduates in areas vital to its interests, the Semiconductor Industry Association has established a fund in an attempt to reverse the trend. To be called the Semiconductor Research Cooperative and have the status of a wholly owned subsidiary of the SIA, Cupertino, Calif., the industry fund has the support of key members of the semiconductor industry and hopes to receive 0.1% of their sales revenue.

"We see the principal benefit of the SRC as the creation of more trained manpower," observes Robert Noyce, SIA chairman and vice chair-

# LeaderChip



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man of Intel Corp. "We want to support those areas of research that we would feel guilty about not supporting, but could not justify individually on the basis of short-term goals." Noyce notes that the establishment of the fund is, in part, a response to the challenge posed by the Japanese. "If we did not perceive a long-term threat to our survival without such research as this, we might not have been spurred to create this kind of support," he asserts.

**Goals set.** Although the SRC program has the support of major integrated-circuit vendors and users, Tom Hinkelman, executive director of the SIA, acknowledges that it may take a while for the SRC to obtain 0.1% of industry sales in contributions. "We expect to collect about $4 million to $5 million in 1982, and we would like to see that grow to $30 million to $40 million in 1985," he says.

The SRC plans to use the money to support research at universities and independent institutes such as SRI International and Battelle Memorial Institute. Disciplines include X-ray and electron-beam lithography, the physics of small structures, and design-automation and test-automation strategies. "We want to support research on how to align things better than the best microscopes can show us, on how to get rid of damage to semiconductors resulting from E-beam exposures, on film deposition and removal, and on refractory metals," Noyce says.

"We also want to explore designing things in silicon, distributed-processing architectures, and the impact of architecture on software." Noyce adds that the SRC will avoid duplicating the efforts of the Department of Defense's Very High-Speed Integrated-Circuits program in areas like fault tolerance, signal processing, and data flow.

**Significance.** Using a thumbnail estimate that it may take $200,000 to $300,000 including overhead to create every Ph.D.—even a $10 million figure would result in only 40 to 50 Ph.D.s. Even this small figure, however, takes on significance when it is noted that only 523 Ph.D.s were awarded in electrical engineering in the U. S. in 1980.

According to an American Electronics Association study, "Technical Employment Projections, 1981–1983–1985," those 523 Ph.D. degrees were accompanied by 3,660 master and 13,594 bachelor of science degrees in electrical engineering. The areas of device physics and equipment support form an even smaller portion of these graduates. "In the specific areas that we are supporting, we estimate that the SRC may be providing up to 20% of all funding," says Noyce.

The SIA claims that membership in SRC is open to foreign manufacturers, provided that their home nations permit similar access. This clause may rule out the Japanese, who do not allow U. S. participation in their very large-scale integration design centers. **-Martin Marshall**

## News briefs

**MCI to buy Xerox's WUI . . .**

Canaries can sometimes swallow cats, as MCI Communications Corp. demonstrated with the disclosure that it has agreed to pay $185 million in cash to Xerox Corp. for its WUI Inc. subsidiary. This launches MCI, a specialized common carrier now largely handling long-distance voice, into the international and domestic data-transmission markets.

MCI's diversification, still to be approved by the Federal Communications Commission, will be funded out of the company's large cash surplus of approximately $160 million, with the remainder in bank loans. WUI, acquired in 1979 by Xerox, was spun off by Western Union Corp. in 1963. Last year, it earned $18.5 million on revenues of $159.5 million, about 80% of which came from record-carrier services. With a 23% share in the market, WUI ranks third behind International Telephone & Telegraph Corp. and RCA Corp. With sales and earnings rising rapidly, MCI reported profits of $26.1 million on revenues of $201 million for the nine months that ended Sept. 30.

**. . . as AT&T buys into Ireland**

At the same time, AT&T International, a foreign sales and services subsidiary of American Telephone & Telegraph Co., quietly made ready to ingest a foreign bird with its planned acquisition of 45% of the capital stock of Ireland's Telectron Ltd., a Dublin-based manufacturer and exporter of telecommunications products that employs 800 people. Completion of that purchase is expected in "a couple of months," says AT&T. AT&T International, formed in 1980 by the combination of two relatively unsuccessful AT&T subsidiaries, American Bell International and Western Electric International, refused to discuss the terms of its Telectron purchase—as it has likewise kept mum about other recent foreign joint ventures, like Korea's Gold Star Semiconductor Ltd. earlier this year.

**High-end system plus own acquisition slated for Four-Phase**

Four-Phase Systems Inc., Cupertino, Calif., plans to introduce a new high-end interactive computer system next year that relies on multiple Motorola 68000 16-bit microprocessors. Code-named Sprint, the system is expected to provide distributed intelligence, self diagnostics, and color and high-resolution graphics. Word of its unveiling—most likely at next June's National Computer Conference—comes while Motorola Inc., the manufacturer of semiconductors and communications equipment, proposes to buy Four-Phase is a $250 million stock swap. The deal signals a push by Motorola of Schaumburg, Ill., which has sales of $3.1 billion, into computer systems and office automation. Four-Phase already has lower-end systems in these areas, as well as IBM plug-compatible machines built by Two Pi Corp., acquired last January.

A one-time darling of Wall Street, Four-Phase fell from favor in 1980 when its earnings plummeted to $5.5 million from $16.7 million in 1979. Profits this year are up, and year-end 1981 revenues are expected to top $230 million compared with 1980's $197 million.

# Washington newsletter

**Action conference on engineer shortage lists Keyworth**

Presidential Science Adviser George Keyworth is expected to be among the approximately two dozen top-level participants in the first National Engineering Action Conference scheduled for April 7, 1982, at Exxon Corp.'s headquarters in New York. Edward A. David, Exxon Research & Engineering Co. president and a former science adviser to the President, will be chairman. **The closed meeting is expected to evolve a national policy to cope with the perceived shortage of engineers and scientists in the U. S.** It will include other Cabinet-level officials, key congressional leaders, university presidents, and chief executive officers of high-technology companies as well as U.S. professional engineering societies. One major emphasis of NEAC, say meeting planners who are still compiling the invitation lists, will be to get the nation's industrial and university communities to issue a policy statement on what U. S. high-technology industries can do to resolve the shortage.

**Foreign EEs in U. S. schools on the increase**

The number of foreign full-time graduate students in electrical engineering and computer science at U. S. doctorate-granting institutions continued to grow faster in 1980 than the number of U. S. citizens in the same fields. The new data assembled by the National Science Foundation shows **the total number of foreign EE graduate students climbed to 4,184 last year, up 11.4% from 1979,** for a 9.6% growth rate between 1974 and 1980. At the same time, the total number of U. S. citizens in the same category rose to 5,528, up 8.5% from 1979, and the growth rate between 1974 and 1980 was a mere 0.6% because of declines in the middle years. According to the NSF study director, Penny Foster, 34% of foreign engineering doctoral candidates were in the U. S. on temporary visas, indicating they probably will return to their homelands to work and teach. The 1980 percentage is, she says, more than double the 1970 level of 14%.

**DOD to seek 50 research fellowships**

The Defense Department is sufficiently worried about the U. S. engineering and science talent shortage that President Reagan's fiscal 1983 budget to be delivered in January to Congress will contain 40 to 50 new research fellowships. According to Leo Young, former president of the Institute of Electrical and Electronics Engineers and now the Pentagon's director of research and technical information, **the grants will be funded at approximately $15,000 each,** compared with National Science Foundation fellowships worth approximately $7,000. They will be administered by the American Society of Engineering Education.

**SRI study to cast fiber optics as national resource**

The premise that fiber-optic technology is a national resource critical to the nation's communications network and future weapons systems will be developed in a new study at SRI International's Strategic Studies Center, Arlington, Va., expected to be made public late next spring. Heading the effort for the nonprofit corporation's national security unit will be Francis B. Hoeber, **who believes the potential of fiber-optic technology and resultant markets "will eclipse the electronics revolution."** Hoeber agrees with the rejection by American Telephone & Telegraph Co. of Fujitsu Ltd.'s low bid of $33.3 million for components for the AT&T's proposed fiber-optic network linking the Boston-Washington areas. The award went to Western Electric Co.

## The NSCCE: a new national program

As the U. S. runs scared before the continuing decline of science and engineering education in the nation's high schools, the Defense Communications Agency is moving to implement a national action program to cope with it. The decline has led to a shortage of engineering faculty in the universities and a drop in the output of engineers to cope with the Soviet challenge in military electronics on the one hand and Japan's continuing assault on the world's civilian electronics markets on the other.

The project is called the National Science Center for Communications and Electronics. To be located on a 34-acre site at the Fort Gordon, Ga., headquarters of the Army Signal Corps, the center will really be "a campus without walls," says Lt. Gen. William Hilsman, DCA director and a principal sponsor of the program. He carefully notes that the center is designed to be built and operated with industry funds privately solicited outside the military. Money will be raised by the Armed Forces Communications and Electronics Association and other industry organizations interested in turning around the national decline in science and engineering education. General Hilsman is "elated with the response" so far from the more than 100 communications and electronics companies that say they will support the effort.

The NSCCE board of directors—chaired by Robert Sarnoff and composed of presidents and senior executives of 25 of the largest U. S. electronics and communications companies—already has in hand contributions of $500,000 each from Rockwell International and United Technologies, with more to come. American Telephone & Telegraph Co., for example, is being asked to contribute $1 million initially.

Scheduled to begin operations in 1983 with an initial budget of approximately $18 million from contributions—although Gen. Hilsman says Sarnoff and others think it should be larger—the NSCCE will be run by the Signal Corps at a cost to the Army and the other two armed services of not more than $1 million. While the services will have access to the facilities for educating and training their own personnel, as well as those of 44 other allied nations, the center's principal goal will be to work with industry to develop education and training courses for the nation's secondary schools, colleges, and universities willing to participate.

As now conceived, available options from NSCEE would include everything from the development of audio-video data banks all the way up to courses beamed by direct broadcast satellites to domestic schools or U. S. military installations worldwide. Two-way communications for student-teacher interaction would be a key segment of this program, says the DCA's Maj. Robert Wiltshire, who is managing the military side of the effort for Gen. Hilsman.

Yet Hilsman stresses that it will take far more than money from industry for a successful program. Critical to the effort, he says, will be the involvement of chief executives in assigning people to visit and work with local school systems in evaluating their academic programs, upgrading the programs with information and contributions of equipment for laboratories and teaching aids, and lending competent technical personnel to teach courses.

### Coping with criticisms

Hilsman is fully aware that academia may cringe at the prospect of the military-industrial complex marching onto the nation's campuses. "It could be a very delicate issue," he acknowledges, one that will require very careful handling by promoters of the program. That, he says, is why the NSCCE plans to begin its effort at the secondary level with 1,672 schools that now have junior Reserve Officers Training Corps programs, on the premise that such schools will not view military interest in education as a threat to academic freedom. At the same time, reaction in the rest of the nation's 27,000 secondary schools will be monitored.

For the military's in-house science education and training, Hilsman says the center will have an advisory board made up of officers at the two-star level. The Navy is already on board, and the Air Force will sign up shortly.

As for executive-branch support, the DCA director disclosed that Deputy Secretary of Defense Frank Carlucci believes the NSCCE program is of such national importance that he has written President Reagan's top aide, Edwin Meese, urging that the President host a White House reception for industry leaders supporting the program. That idea is getting positive White House consideration, Hilsman says.

If the President opts for the wine-and-cheese party route, he would do well to include as many of the nation's academic and congressional leaders he can find who support the NSCCE concept—as well as those who may question it. To persuade the doubters, the President may want to recall Thomas Jefferson's line that "science is important to the preservation of our government, and it is also essential to its protection against foreign power."

**-Ray Connolly**

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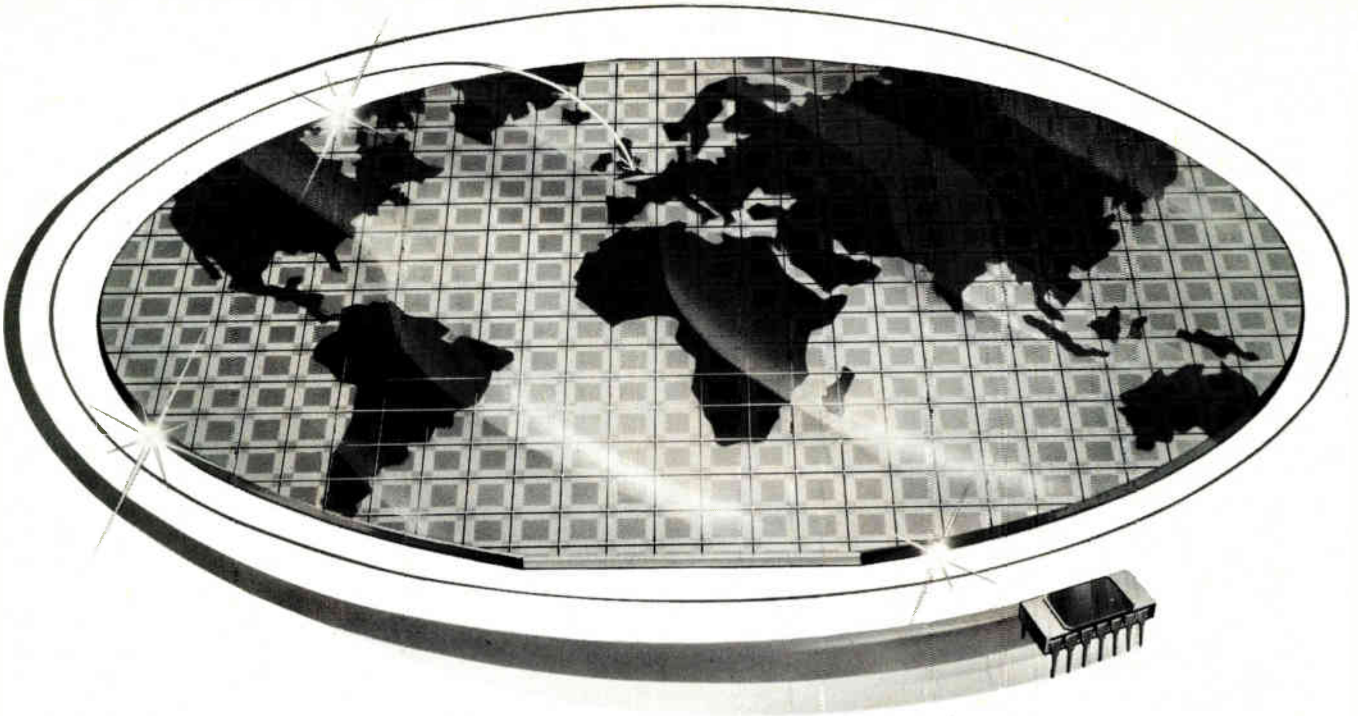

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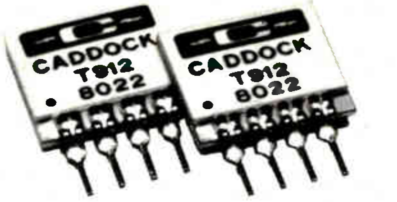
# Electronics International

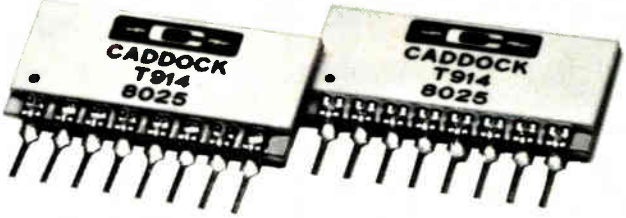
## Light-switching array creates solid-state printer: page 53

A full-range pocket computer has been introduced by Sharp that includes a large custom complementary-MOS chip: page 56

# Type T912/T914 Ultra-Precision Resistor Networks from CADDOCK provide Ratio TCs to 2 PPM/°C and Ratio Tolerances to ±0.01% for precision analog designs.




Type T912 Ultra-Precision Resistor Network 'Pairs'




Type T914 Ultra-Precision Resistor Network 'Quads'

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- **Absolute Tolerance:** 0.1% for all resistors.
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- **Ratio Temperature Coefficients:** From 10 PPM/°C to 2 PPM/°C.
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- **Ratio Stability of Resistance at Full Load for 2000 Hours:** Within ±0.01%.
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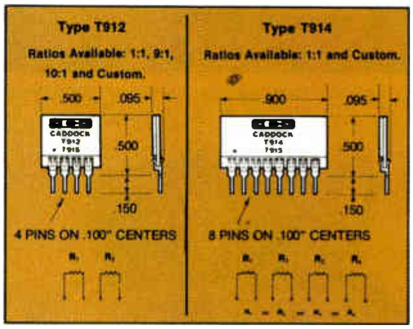
This exceptional combination of performance specifications – and the compact, in-line configuration of the Type T912/T914 precision resistor 'pairs' and 'quads' – provides the single-package matched resistor characteristics and stability required by high-accuracy analog circuits, including –




- **Precision analog amplifiers.**
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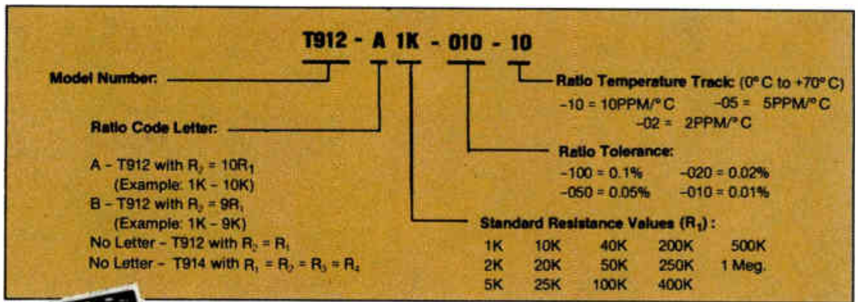
## Standard models of Type T912/T914 precision resistor 'pairs' and 'quads' include 14 off-the-shelf resistor values with a wide choice of Ratio Tolerances, Ratio TCs and Resistance Ratios:

This standard part number provides a selection of over 500 in-production models of Type T912/T914 precision resistor 'pairs' and 'quads':





As an example of the price/performance advantages of this advanced resistor technology, the Model T912-A1K-010-10 shown here provides a 1K-10K resistor 'pair' with a ratio tolerance of ±0.01% and a ratio temperature coefficient of 10 PPM/°C at a 1000-lot unit price under $2.55. The same resistor 'pair' with a ratio tolerance of ±0.1% delivers at a 1000-lot unit price under $1.50!

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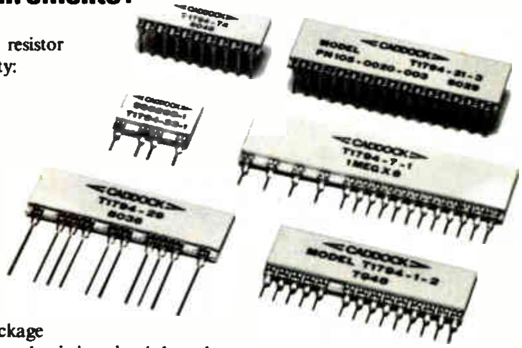

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# International newsletter

## France halts EEC move to liberalize trade in telecom gear

French opposition has stalled a Common Market effort to free new telecommunications technologies from national restrictions. In a meeting of the Common Market's council of ministers, the French opposed opening national markets to suppliers that do not produce much of their telecommunications equipment within the European Economic Community. **The objection holds up proposals on common guidelines for new integrated-service digital networks.** The aim would be to offer compatible services throughout Europe after 1983. Also put on hold is a recommendation that would decontrol the market for new telecommunication terminals so that users as well as public administrations could hire or buy equipment from suppliers. The French objection applies to efforts to open up to non-EEC suppliers purchases of transmission, switching, telephone, and other requirements by the public telecommunications agencies.

## Matsushita, Hitachi to market compatible 3-in. floppy disk

Another standards controversy may be brewing in Japan, this time over a format for small floppy-disk drives for office-automation equipment and personal computers. Matsushita Electric Industrial Co. and Hitachi Ltd. plus subsidiary Hitachi Maxell Ltd. have developed a 3-in. double-sided, double-density disk with a standard format. **Last year, Sony Corp. introduced a 3¼-in. single-sided floppy disk with a different format** for its office and personal-computer gear. Matsushita and Hitachi designed their system for data compatibility with 5¼-in. drives, getting the same unformatted capacity of 250 kilobytes per side in 40 tracks. Recording density is 100 tracks/in. and 9,000 or 4,500 b/in.

## Bubbles stake out place in System X

Bubble memories are ousting disk memories in Britain's System X all-digital central exchange program, adding system reliability and performance while reducing capital and running costs. Plessey Microsystems Ltd. in Caswell, Northants. (charged by British Telecom with the development), has now delivered its first systems to DEC Telecommunications Ltd., which is integrating the 18-megabyte store with its second-generation System X processor for first delivery in 1982. Orders for System X exchanges now total 30. **Each of the 18 boards in the memory system packs in 1 megabyte of bubble memory** together with driving, sensing, error-correction and bus-interface circuitry. The memory can stream data at 100 kilobytes/s with an average random-access time of 17 $\mu$s. Plessey will use 1-Mb bubble chips from Motorola, now available in sample quantities, but is delivering first units with 256-K Motorola parts. It will also second-source the memory boards itself, using Hitachi bubbles.

## Siemens expanding large computer line with Fujitsu help

West Germany's Siemens AG is expanding its 7.800 family of large computers—again with processors from Japan. The new models, 7.890 and 7.892, use Fujitsu Ltd.'s MH280 and M382 processors. They are scheduled for delivery in the spring of 1983 and will be marketed throughout Europe. **The larger of the two, the 7.892, is said to be 15 times more powerful than the 7.865,** the smallest in the 7.800 family. The single-processor model 7.890 has a main memory capacity of up to 64 megabytes while that for the multiprocessor model 7.892 can be expanded to 128 megabytes. Both models can be fitted with up to 64 channels, the total throughput being 96 megabytes/s. Key components are logic devices with a 350-ps delay and 64-K memory chips.

**U. S. firm backs new Israeli computer**

Computer Consoles Inc. of Rochester, N. Y., has bought a 66% share in Time Machine Ltd. of Haifa. It will invest between $3.5 million and $4 million in the Israeli firm. Time Machine claims to have developed a 32-bit computer that is in the range of the Digital Equipment Corp. VAX 11/780 series and the Data General MV/8000 series. **However, the company says its new mini has as yet unannounced novel and revolutionary aspects.** First deliveries are expected in October 1982. The agreement with Time Machine gives the Israeli company rights to the European market as well as 15% of the proceeds from the American market.

**ICL ponders selling IC plant to Fujitsu**

ICL Ltd. is discussing the sale of its microelectronics design center to Fujitsu Ltd., one of several suitors. Such a deal would save ICL around $50 million a year, while providing Fujitsu with an instant European foothold. The Japanese firm would likely re-equip the West Gorton, Manchester, unit with its own large-scale integrated complementary-MOS technology, **creating a European design center to serve ICL and other customers.** ICL needs a fast prototype service for C-MOS gate arrays, the chosen technology for its projected DM/1 distributed mainframe, and the facility would provide that service. Meanwhile, the UK company has posted record losses of $259 million (including $150 million for layoffs and plant closures) on revenues of $1,365 million, marginally down from last year.

**Laser system detects gases**

A carbon-dioxide-laser–based system for detecting gas pollutants from a distance has been developed by the Compagnie Générale d'Electricité at its research center in Marcoussis, south of Paris. Destined for military use in chemical warfare, the **system operates on the principle of absorption differential:** laser beams of different wavelengths are directed at natural objects, like trees, that serve as retrodiffusers. One beam serves as a reference, and the other or others are intended to be absorbed by the gas or gases suspected of being present. Analysis of the reflected beams identifies gases like ethylene ammonia, sulfurous anhydride and freons.

**Sharp shaves cost of Japanese-language word processor**

Sharp Corp. has chopped the price of Japanese-language word processors down to less than $5,500 with its desktop WD-1000. The price is low enough, says Atsushi Asada, general manager of the industrial instruments group, for the units to be marketed through office-equipment dealers rather than the firm's small-business-computer dealers who sell its more expensive models. **Intelligence and much of the memory in the system are tucked into a package the size of an encyclopedia volume.** Rounding out the system is a minifloppy-disk drive and an impact printer.

**Addenda**

Munich-based Siemens AG has licensed Western Digital Corp. of Irvine, Calif., to **manufacture its Eurocard-based microcomputer line and sell it in the U.S.** The 80 items in the board-level family, based on the Intel 8080A, 8085A, 8086, and 8088 microprocessors, constitute a modular line for applications in process control, industrial automation and measuring systems. . . . Leasametric Inc., a major supplier of rental test instruments and electronic equipment in the U. S. **has moved into the European market with the formation of Leasametric GmbH,** a joint venture with Kontron Elektronik, GmbH, a distributor of equipment in West Germany.

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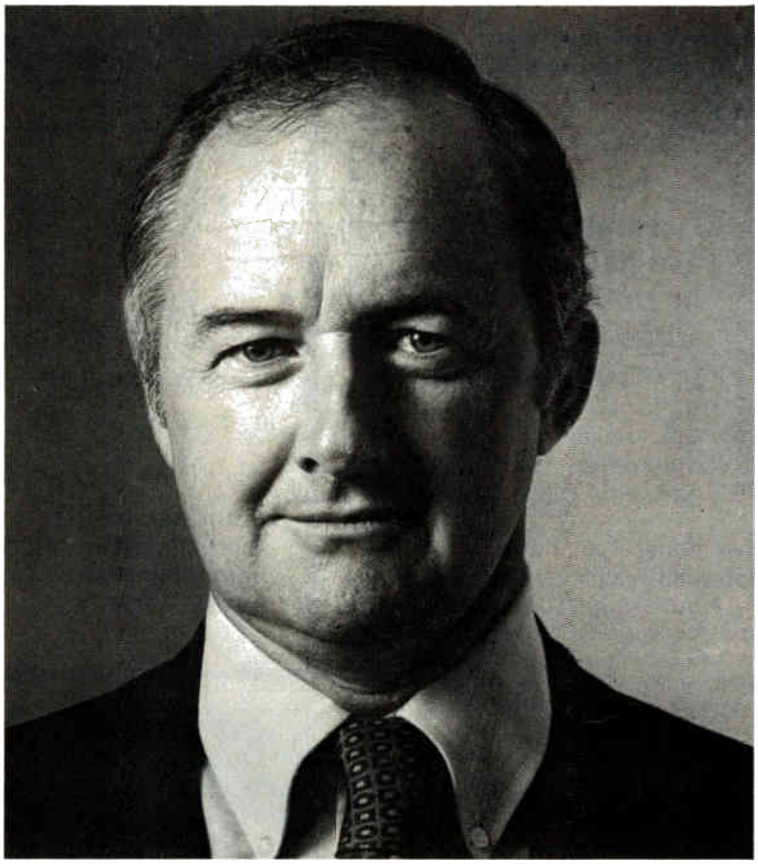

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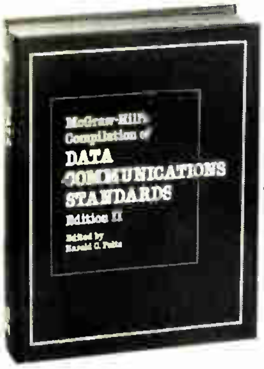


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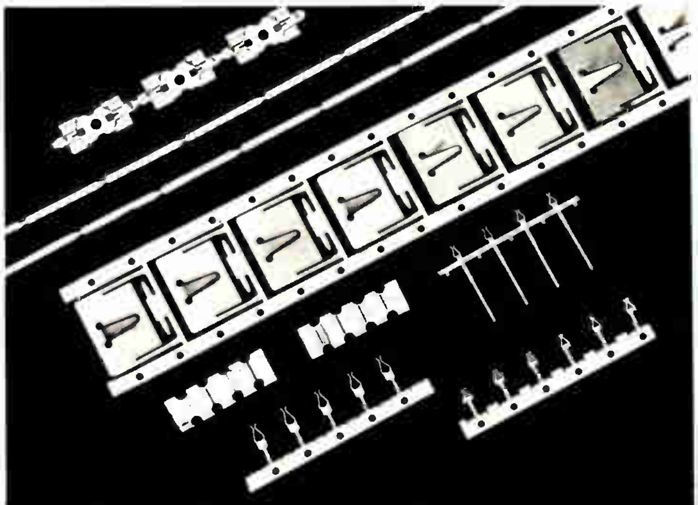

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# Magneto-optics begets new display technology

*by John Gosch, Frankfurt bureau manager*

Thin-film device employs linear and matrix arrays of light-switching cells in wholly solid-state approach

**Designers will soon** have a new kind of component to work with: a solid-state, electronically controlled light-switching device that uses magneto-optic principles to implement new printing and display technologies.

Based on techniques worked out at the Philips Research Laboratories in Hamburg, West Germany, the thin-film device consists of a number of light-switching cells that can be configured as a linear array. Such an array could be used as a pattern generator in optical line printers, for example. When arranged in a matrix, the cells could form the basis for a data display, being capable of storing as well as displaying the information fed to them.

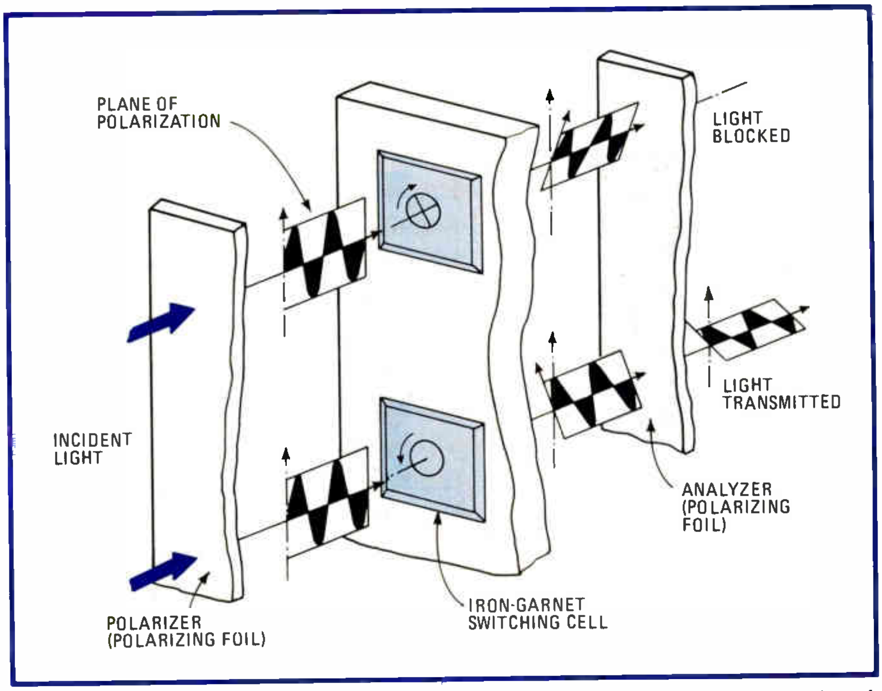
In a printing application, the device has several advantages over current techniques. In contrast to laser-based systems with their moving deflectors, the Philips device uses no moving parts. It handles information in parallel fashion, which enhances speed and simplifies cell addressing. Unlike other solid-state approaches, such as light-emitting diodes, the cells do not heat up because the light source is separate.

Valvo GmbH, the Hamburg-based, components-producing subsidiary of Philips Gloeilampenfabrieken NV of the Netherlands, has translated the research results into samples of a light-switching device for printing applications. Dubbed Lisa, for light-switching array, the device has already sparked the interest of a number of U. S. firms, Valvo says. Produced in volume, Lisa devices with 512 cells could cost less than $100 each, the company estimates.

**Recipe.** Building the device begins with depositing a 5-micrometer magneto-optic iron-garnet film on a single-crystal transparent substrate of gadolinium gallium garnet. The film is etched to form tiny islands—the light-sensitive cells—typically 70 by 70 $\mu$m in size. The area between the cells is covered with a metal film to block light.

The film's magnetization can be either parallel or antiparallel to the normal of the film. If linearly polarized light traverses the cell, the light's plane of polarization is rotated either to the left or right depending on the direction of magnetization (see figure below). This Faraday rotation, as it is called, is the basis for light switching.

The cell-carrying substrate is sandwiched between two polarizing foils, the first producing the polarized light. Emanating from the cells is light with different planes of polarization for the different directions of magnetization. The second foil blocks the light associated with one plane of polarization and partially passes the light associated with the other. Thus, to an observer of a Lisa device, the cells appear either bright or dark. The spectral range over which good bright-dark con-




**Lisa.** Light's plane of polarization is rotated to the left or right depending on the direction of magnetization. This is the basis of the magneto-optical-light switching array.

trast is obtained is 530 to 650 nanometers, the company says.

To switch magnetization from one direction to the other, the Philips researchers are using a thermomagnetic effect: a heat pulse, about 150°C and lasting for 15 microseconds, is applied to the cell. The stability of the magnetization then temporarily drops and its direction can be reversed. The heat pulse is generated by a short current pulse fed via a network of metal conductors to a thin resistance layer deposited on top of each cell (see figure below).

To reverse the direction of magnetization, a 3-µs magnetic field pulse is used. This pulse can be generated by sending a current pulse through, say, a one-turn winding designed as a metal conductor and running alongside the cell. The direction of magnetization switches within a fraction of a microsecond.

**Cool switching.** The cells feature an effective optical switching time of less than 1 µs. With only 0.5 microjoule per switching event, the switching energy is so small that the cell hardly warms up.

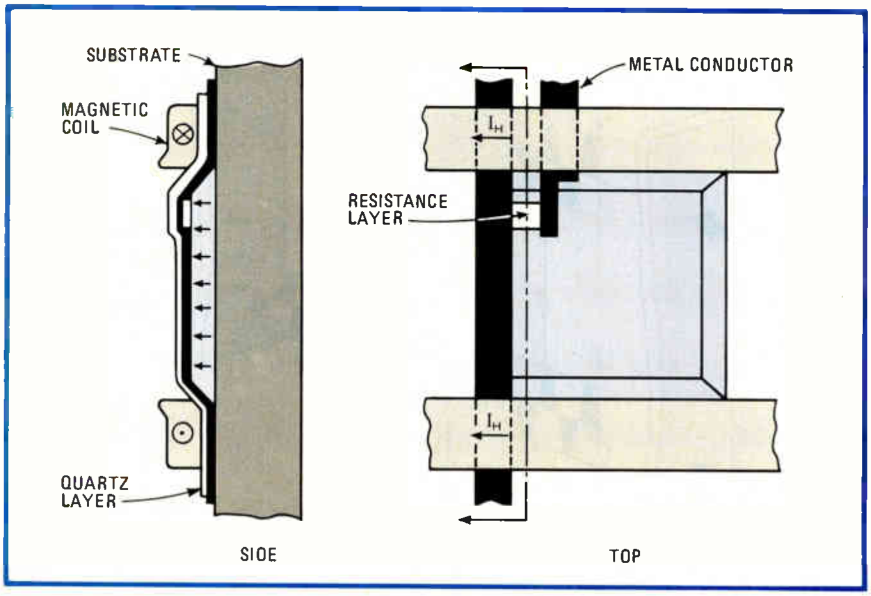
Using these principles, the Valvo designers have built their first device, which is designated Lisa 512, for printing applications. The device contains a chip with 512 cells arranged in a zigzag configuration. The conductor lines end at bond pads located along the substrate. The "optical" length of the device, that is, the length of the row of cells, is 32 millimeters.

Supplying the current pulses for the resistance layers are four integrated circuits, two on either side of the chip. The pulses for driving the coils that set up the magnetic switching field come from external current sources. Power consumption of the device is between 2 and 3 watts, Valvo says.

**Photo finish.** In an experimental printer, Philips researchers have arranged a number of Lisa devices next to each other to form a linear array of up to 1,536 cells. Focused onto the cells is light from a linear source—in this case a lamp whose light is guided to the devices via glass fiber. The light dots from the cells are projected through a lens system onto light-sensitive material—for example, on a photoconductor drum rotated under the cell array. Because of the high switching speed and light-dot density, the information is of photographic quality.

To generate text, the light-switching cells are controlled by the same four ICs that feed the heat current pulses. The ICs incorporate shift registers for sequential write-in and parallel read-out to allow parallel cell control. The average input data rate is typically 1 megabit per second split into separate data input channels of 500 kilobits per second for the two upper and two lower ICs.

Besides printing, other potential applications for Lisa-type devices are in electrophotography and displays. Philips researchers have already realized an experimental matrix of 256 by 64 individually addressable cells that could lead to a device for display systems. Because of the cells' storage capability, the written-in information stays displayed even after power is shut off.




**Switch.** Demagnetizing heat pulse is generated by a short current pulse fed via a network of metal conductors to a thin resistance layer deposited on the top of each cell.

## Great Britain

# Digital data links edge nearer reality

Not to be outdone by private enterprise, British Telecom is planning a wideband digital data service of the kind needed to support electronic mail and other advanced business services on private networks. The move follows the recent announcement by three British companies of the Mercury service, which is scheduled to start in 1983 (see "Mercury hits the ground running").

The first stages of British Telecom's X Stream service will become operational in late 1982. X Stream takes in a range of options: a Megastream service in which local fiber-optic links, microwave radio relays or wideband data links are used to pipe data into a customer's premises at 2 megabits per second; and a Kilostream service that uses the existing local network to provide a 64-kilobit-per-second service—four times faster than the best link available today—on two unconditioned twisted-pair telephone lines.

Then, in late 1983, a first switched service, called Switchstream and based on a System X digital exchange, will come into operation in the City of London. At about the same time, the European business satellite service—run in collaboration with other European telecommunications authorities—will be

## Mercury hits the ground running

Before Mercury, the high-speed data-service to be set up in competition with British Telecom, can get under way in mid-1983, its backers, Cable & Wireless Ltd., British Petroleum Co. (Britain's largest company and a major potential user), and Barclay's Merchant Bank Ltd. must first build a network from scratch, using the latest in transmission technology.

To start with, there will be an optical-fiber ring linking the major urban conurbations and using a four-fiber cable with a capacity of at least 140,000 bits per fiber. The equipment, to be purchased from STC, General Electric Co. Ltd., and Plessey, would conform to the standard of the International Consultative Committee for Telegraphy and Telephony and resemble first-generation systems already delivered to British Telecom. The network will be laid in ducts alongside British rail tracks.

Connection to city distribution centers would be via digital microwave links. The distribution nodes themselves will consist of transceivers operating in the 10-gigahertz band on one or more low-profile horn antennas.

Transmission from the node to the subscriber will employ time-division multiplexing, a subscriber antenna only 2 feet in diameter being sufficient to transmit and receive signals. Like System X, the service will employ 64-kilobit-a-second channels, conforming to CCITT standards, up to data rates of, say, 2 kb/s. The network will provide either voice or data channels and will, the consortium hopes, interconnect to the public net at a subscriber's private branch exchange. **-K. S.**

getting under way. In the U.S., American Telephone & Telegraph Co. has plans for a digital data service [*Electronics*, Dec. 15, p. 38].

British Telecom plans to provide voice and data facilities in a single Integral Data Network by means of a digital overlay, or thinly spread trunk network of System X digital switches. It is not expected to complete the net until the late 1980s.

**Choice.** There are two methods of introducing digital switching technology. One is to replace entire areas *en masse*. The other is to provide a spinal network that overlays the existing network and can be accessed by those customers prepared to pay for the advanced business services it offers. In the end, the final solution is the same—to move the entire network over to digital technology. But this takes time and money.

So, in the interim, the company plans to lease wideband digital links using pulse-code-modulated digital transmission on lines that are already in place. The new service will not be switched, but it will let high-volume users put together their own dedicated data networks.

Both Cable & Wireless Ltd. and British Telecom, for example, will provide wideband links at up to 2 Mb/s—the equivalent of thirty 64-kb/s voice channels that interface directly with the new generation of digital private automated branch exchanges being developed as the hub of the office of the future. But smaller users, too, will benefit from the wideband services.

GEC-Marconi Communications Ltd., in particular, worked with British Telecom's research labs to develop equipment to pipe high-speed 64-kb/s services—four times that possible with the fastest modem—over the local network, using two unconditioned twisted-pair cables.

Data is piped over the local network with the aid of a modulation technique that was developed at British Telecon's research center. Based on the Walsh digital coding technique, it has the advantages of simplicity and an easily extracted timing signal needed to maintain both ends of the link in synchronism.

In essence, the data clock signal serves as a carrier, while the modem is a simple exclusive-OR gate that puts out a positive- or negative-going "top hat" signal that is easily transformed into a digital data stream. The technique uses a large bandwidth—around 120 kilohertz to support a 64-kb/s data rate—but in the local network there are no bandwidth constraints as there are in the trunk network.

In essence, the setup consists of a local digital-line system operating at up to 64 kb/s—the channel rate for System X—feeding a 2-Mb/s multiplexer at the local exchange. This gathers data from up to 31 subscribers and produces a data stream like that of other 2-Mb/s multiplexers in the system. Additional control signals in the appropriate time slot allow operation at lower rates such as 2.4, 4.8, 9.6, 48, and 64 kb/s. The equipment will operate at up to 5 kilometers from the exchange.

Routing signals through the network occur at cross-connection sites where incoming 2-Mb/s data streams are demultiplexed and then either hardwired to outgoing pulse-code-modulated data links or distributed locally. Comprehensive supervisory and control facilities are provided by framing each 6-bit data word with 2 control bits.

**Enthusiastic.** Brian Bowsher, product planning manager for line products at GEC-Marconi, is enthusiastic about the prospects. Ultimately, the European communications authorities, he explains, want to combine voice and data into a single local service—to be called the Integrated Services Digital Data Network (ISDN)—and much development is going into harmonizing standards. In fact, Switchstream, based on a System X exchange in the City of London, is a pilot for upcoming ISDN services.

In the interim, he sees a big market for data-only services—British Telecom's plans alone call for 1,100 systems. The company has already placed orders with Marconi Communications for more than $9.43 million worth of equipment, and a further order for over $5.65 million is expected shortly.

The equipment will also be used internally by British Telecom to run its digital network more efficiently. Its packet-switched network, for example, could run on digital PCM links instead of the high-speed analog trunk links used at present. The equipment will be used to link distant users into System X or to connect them to its European business satellite service as well as to carry slow-speed Telex traffic on its PCM network. **-Kevin Smith**

## Japan

# Hand-held computer does almost anything

Sharp Corp.'s PC-1500 has an amazing range of features for a hand-held computer. It boasts a new 8-bit complementary-MOS microprocessor, extremely fast execution speed, string variables, and Boolean operations, among other refinements [*Electronics*, Dec. 15, p. 71].

The PC-1500 uses a 16-K read-only memory that contains a greatly enhanced version of Basic compared with the earlier PC-1211 [*Electronics*, Feb. 28, 1980, p. 40], which contains a 12-K ROM. It also has 3.5 kilobytes of C-MOS random-access memory, up from 1.6. An additional 4-K bytes of C-MOS RAM is available as a plug-in option.

The price of the new unit in Japan, where sales start next month, will be $277, plus an extra $70 for the memory module. Thus Sharp has placed itself between the newly introduced $170 hand-held Casio FX-702P [*Electronics*, July 28, p. 67] and Panasonic/Quasar's new $600 Hand-Held Computer. The Casio unit features a C-MOS RAM with almost 1.9-K-byte capacity that can store up to 10 programs. The other unit has an internal 4-K-byte RAM, which can be expanded externally, and a maximum internal ROM of 48-K bytes made up of three 16-K-byte program capsules.

The custom 8-bit C-MOS microprocessor that is the nucleus of Sharp's computer is both the computing engine and the display controller. To keep the system simple and inexpensive, the 6-by-6-millimeter chip is packaged in an 18-by-18-mm flatpack with 76 leads on 0.8-mm centers radiating from all four of its sides—in other words, enough pins to handle all signals without multiplexing. The external connections include an 8-bit data bus, a 16-bit address bus, control lines, an 8-bit input port for the keyboard, and seven lines for driving the display backplate.

**Cycle time.** The processor's architecture is relatively standard. The machine cycle time is 770 nanoseconds. The minimum instruction time is four machine cycles.

That execution speed is a definite plus when running long programs. Two-letter variables permit naming of variables, and the inclusion of two-dimensional arrays vastly increases the range of problems that can be handled. Other features, besides the string variables and Boolean operations, are a random-number generator and a large number of statements including data statements, matrix dimensions, and three types of ON . . . GOTO statements. Furthermore, a real-time clock has been built in and can be incorporated into programs.

Sharp claims that this is the first true pocket computer with a Qwerty keyboard arranged in diagonal columns like a typewriter, rather than in a checkerboard pattern like a calculator. The keyboard also has soft keys that can be programmed for three separate functions each. Still, the unit's size is only 86 by 195 by 25.5 mm, and it weighs just 375 grams.

The display is a 7-by-156-dot matrix, permitting full graphics capabilities. The $231 printer, using a mechanism purchased from Alps Electronics, is an intelligent drum-type X-Y plotter using red, green, blue, and black ballpoint pens.

Akira Tobe, senior executive director at the company, expects that the higher performance and price of the PC-1500 will shift its market to businessmen from the 50-50 split between businessmen and students for the lower-priced PC-1211. Sharp will also export the new model, but its plans have not yet been made public. **-Charles Cohen**


**Scribe.** Sharp's new pocket computer, the PC-1500, shown with printer attached, has powerful graphics capabilities, with the necessary commands included in the interpreter. The printer is an intelligent, drum-type X-Y plotter with ballpoint pens in four colors.

# Logical Logic Analysis

The only logical way to analyse multiplexed data is to demultiplex it. Which is just what Philips PM 3543 and '42 Logic Analyzers do.

Moreover both instruments feature a disassembler option, allowing data to be displayed in the same language as the relevant processor.

So what you see, is what you thought and wrote.... for most popular 8- and 16-bit µPs.


LAs with dual clocks mean that multiplexed address and data can be captured sequentially, but displayed side-by-side, on the same line. Philips LAs also make the same kind of savings on probe connections as the multiplexed devices make on pins.

This makes PM3542 ideal for 8-bit µCs like the popular 8048, while PM3543 covers all 8-bit and multiplexed 16-bit µPs.

The multiple disassembly option enhances analysis even further by supporting the 8048, 8080, 8085, Z80, 6800 and 6502 in a single package. (Note: a single package supporting 8086/88, Z8000, 6809 and 1802 will be available by end '81.)

Both LAs feature a real-time analysis facility, allowing the software instruction and hardware implementation to be related directly. They also, as an added bonus, function as excellent 35 MHz/2 mV oscilloscopes.

Full details from:

Philips Industries, TQ III-4-62,
Eindhoven, The Netherlands.

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# Epitaxy-collector technology cuts losses in switching devices

*by Robert T. Gallagher, Paris bureau*

Line of 150- and 250-W bipolar switching transistors have 25% less voltage drop and price hike of only 10%

**By changing the** technology used in the manufacture of its Superswitch line of fast switching transistors, the Thomson-CSF Discrete Semiconductor division claims to have improved on both the line's dynamic and static losses and its reliability without significantly increasing the price.

Called Superswitch II, the line consists of 10 transistors organized in three homogenous groups. The first four, BUV 39 to 42, operate at 90 to 250 V with a collector saturation current of 6 to 20 A for an output of 150 W. The other two groups, BUV 50 to 52 and BUV 60 to 62, both operate at 125 to 250 V, though the former group has collector saturation currents of 10 to 30 A for an output of 250 W.

These transistors supersede the equivalent BUX line and offer either 20% to 35% lower dynamic losses or fast switching without negative base polarization and also a 25% to 40% lower static loss. What's more, the fall time of less than 300 ns is specified at a junction temperature of 100°C and thus avoids derating for worst-case simulation.

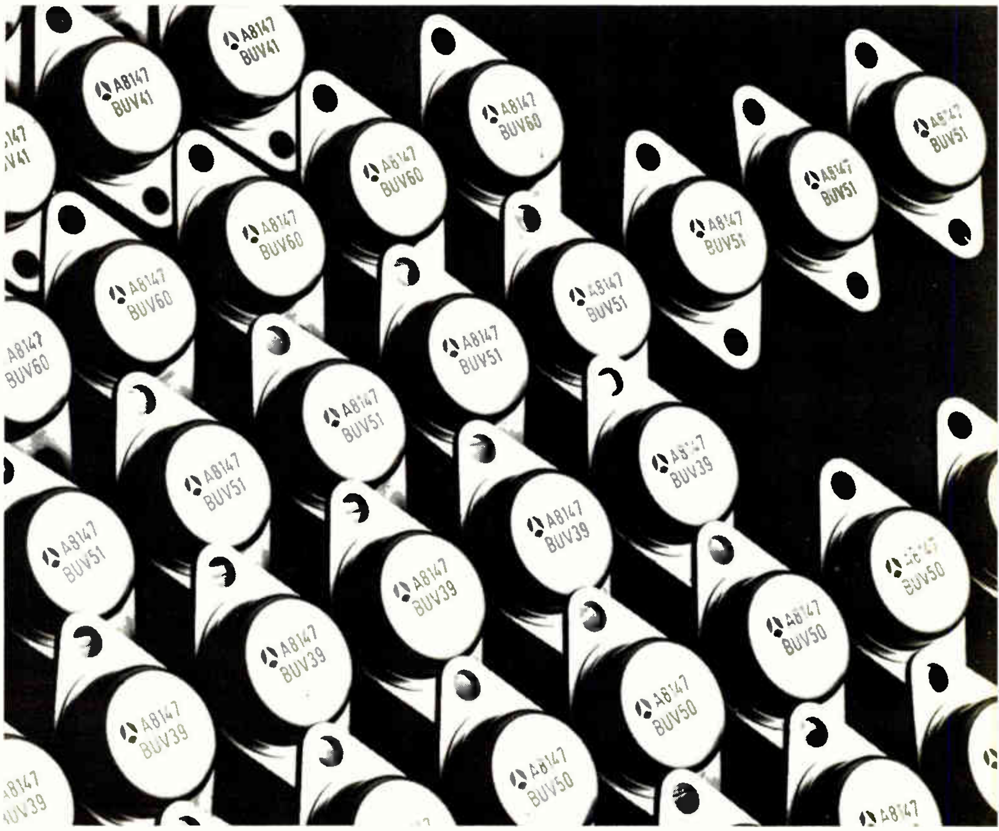
The key to the improved specifications is the company's change from triple-diffused to epitaxy-collector device technology. "To see just what a difference the change in technology makes, it is worth looking at some precise comparisons of the Superswitch and Superswitch II lines," says Lucio Bossi, sales manager of the Discrete Semiconductor division.

"The old BUX 10 had a maximum rating of 1.2 V at a collector current and a base current of 20 and 2 A, respectively," he goes on. "With the equivalent Superswitch II, the BUV 50, the maximum rating is only 0.9 V at the same current specifications, so we have a 25% gain on dissipated power."

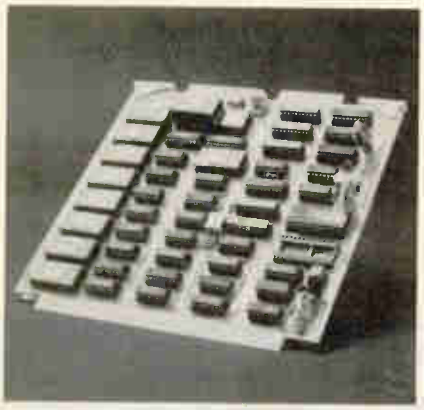
Another example, using the same transistors, demonstrates that they also boast an easier base drive. With a saturation voltage of less than 0.7 V for the BUV 50 and 0.6 V for the BUX 10, both transistors have a collector current of 10 A. But the base current of the BUX 10 is a hefty 1 A, whereas the BUV 50 cuts that in half, thus allowing it to be driven directly by an integrated circuit.

At present, the 90- and 125-V models (BUV 39, 50, and 60) are in production, and the others will be available early next year. Despite the more expensive epitaxy-collector device technology, the company says that the price increase from Superswitch to Superswitch II transistors will come to less than 10%.

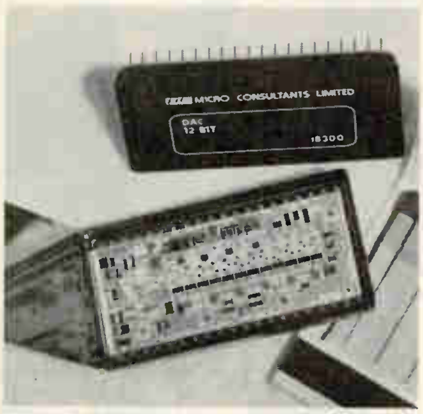
Thomson-CSF, Discrete Semiconductor Division, 50 rue J. P. Timbaud, 92402 Courbevoie, France [441]



Suitable for power supplies, the MB25 series of rectifiers can deliver 25 A dc continuously (at a 350 A maximum peak surge) and have repetitive peak reverse voltage ratings from 100 to 1,200 V. Marconi Electronic Devices Ltd., Carholme Road, Lincoln LN1 1SG, England [442]



The voice-output module uses a Z8 central processing unit and 32- and 256-K bytes of erasable programmable read-only memory. External connections are made with a RS-232-C or an 8-bit input/output interface. Unitronic GmbH, P. O. Box 330429, D-4000 Düsseldorf, West Germany [443]




The 18300 series hybrid digital-to-analog converters offer 8-, 10-, or 12-bit resolutions with typical settling times at 10, 20, and 30 ns, respectively. They offer differential- or single-ended line-driving voltage outputs. Micro Consultants Ltd., Kenley House, Kenley Lane, Kenley, Surrey CR2 5YR, UK [444]

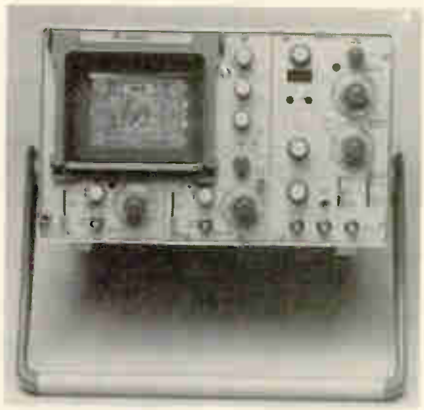
Relative humidity ranging from 15% to 100% may be measured in less than 10 s with the Hygrometer Type CH-2. The device operates over a temperature range of 0° to 150°C and has an accuracy better than ±4%. Chichibu Cement Co., 2-1-1 Tsukimi, Kumagawa-shi, Saitama 360, Japan [445]

The SC-7501 microprocessor-controlled logging meter has 12 input channels for measuring voltages from 1 μV to 270 V dc and 10 μV to 270 V ac root mean square, resistance from 1 mΩ to 19.999 MΩ, and temperature. Iwatsu Electric Co. 1-7-41 Kugayama, Suginami-ku, Tokyo 168, Japan [446]

Model 2040 measures temperature difference and temperature change over time. It accepts up to 10 type K thermocouple inputs to measure from −200° to +1,372°C with a 1° resolution. Comark Electronics Ltd., Rustington, Littlehampton, West Sussex BN16 3QZ, UK [448]


The JPRC dc-dc converters have inputs of 10 to 30 V dc, outputs of ±15 V at 100 mA (model JPRC-15012) and 5 V at 1 A (JPRC-05101), floating outputs, and input-to-output isolation of 500 V ac minimum. Jannu Systems Co., 1-25-27 Minami Nagasaki, Toshima-ku, Tokyo 171, Japan [449]


The position of a short circuit on printed-circuit boards may be located with the Toneohm 550. Plug-in probes move along the track until a tone sounds at 200 mΩ. Polar Electronics Ltd., P. O. Box 97, Lowlands Industrial Estate, St. Sampsons, Guernsey, Channel Islands [450]



A binary-coded decimal time base generator is used in the 30-MHz dual-trace oscilloscope OS3351 for examining television signals or displaying a TV picture. Its 16-kV cathode-ray tube provides a bright display. Gould Instruments Division, Roebuck Road, Hainault, Essex 1G6 3UE, UK [451]

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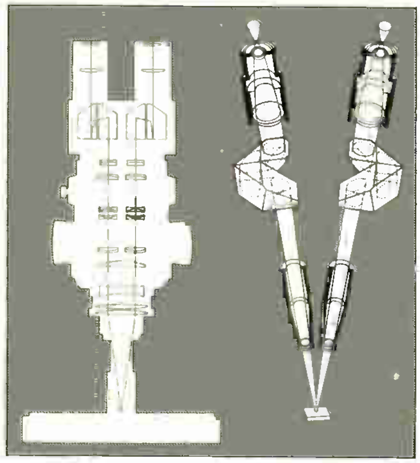

*The common main objective system of the Wild stereomicroscope, left, offers the advantage over the Greenough system, right, in that the intermediate image planes are parallel to the object plane and there is no tilt between them.*

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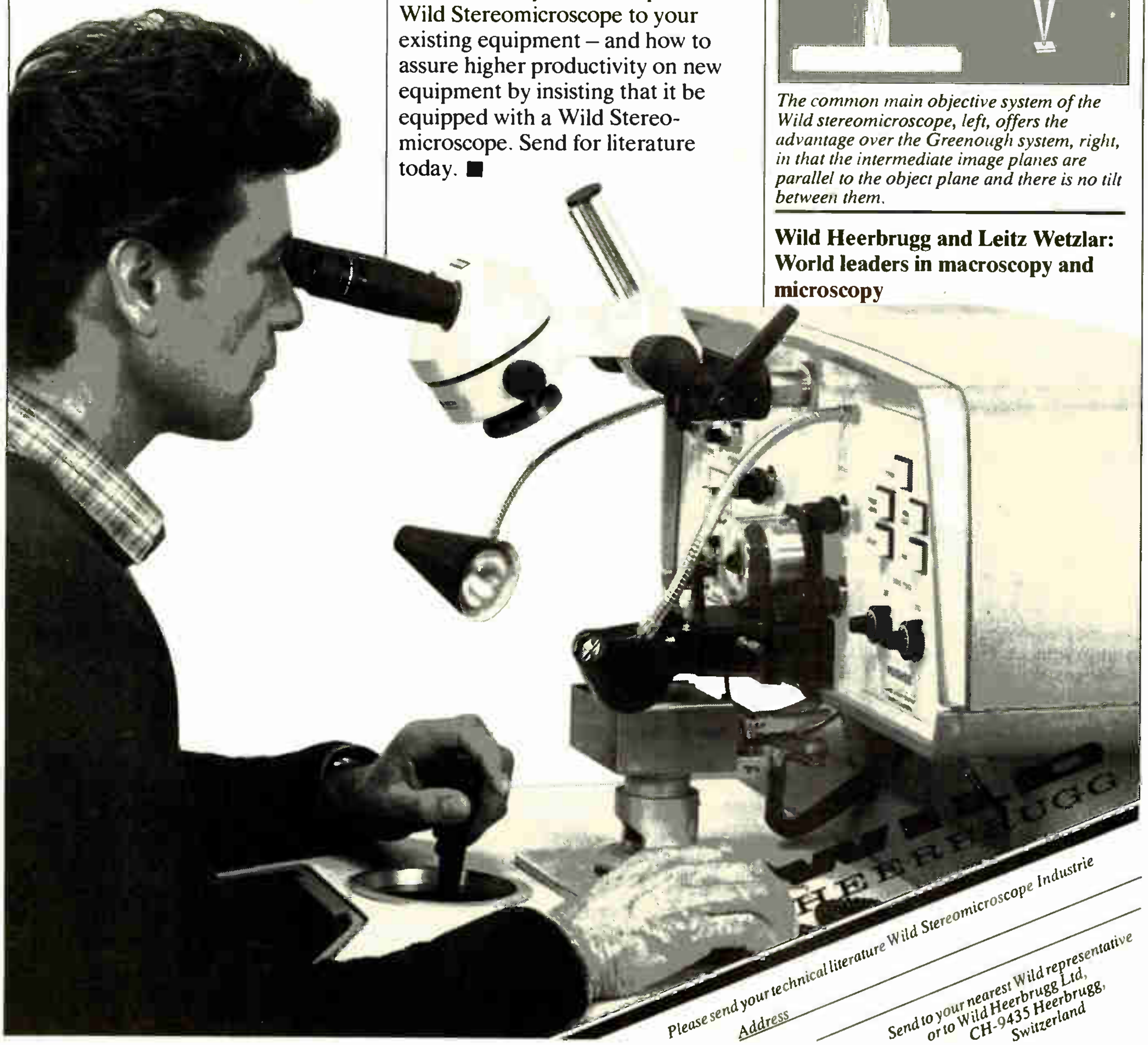
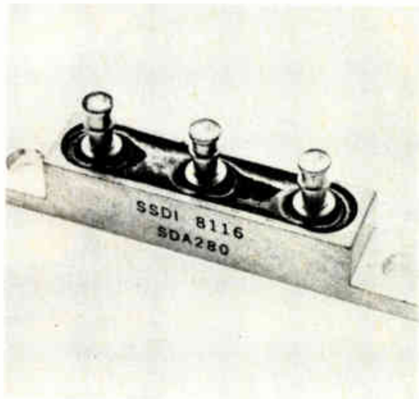



EL 12-2

## New products international

The RJ-4 sealed cermet trimmers require a small space (60% of conventional ¼-in.-diameter trimmers). They have a resistance of 10 Ω down to 2 mΩ, a temperature coefficient of ±100 ppm/°C, and can handle 0.5 W. Copal Electronics Co., 1-17-1 Toranomon, Minato-ku, Tokyo 105, Japan [452]




With a recovery time of 150 ns maximum, the SDA 280-A through -G series of rectifiers are suitable for switching regulator supplies. They carry 15 A average with a peak inverse voltage of 50 to 100 V. GE Electronics Ltd., 182/184 Campden Hill Rd., Kensington, London W8 7AS, UK [453]

Multiple-burst frequency and phase delays in degrees and revolutions a minute can be measured with the 1-GHz PM 6672 and 120-MHz PM 6671 and PM 6670 timer-counters. Time-interval averaging is used for a resolution down to 10 ps. Pye Unicam Ltd., York Street, Cambridge CB1 2PX, England [454]

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**h** ☐ Components & Subassemblies

8 Source of Inquiry—All Other INT'L.

**j** ☐ Independent R&D Organizations
**k** ☐ Government

**Your design function** (check each letter that applies):

**x** ☐ I do electronic design or development engineering work.
**y** ☐ I supervise electronic design or development engineering work.
**z** ☐ I set standards for, or evaluate electronic components, systems and materials.

**Your principal job responsibility** (check one)

**t** ☐ Management
**v** ☐ Engineering Management
**r** ☐ Engineering

**Estimate number of employees** (at this location): **1.** ☐ under 20 **2.** ☐ 20-99 **3.** ☐ 100-999 **4.** ☐ over 1000

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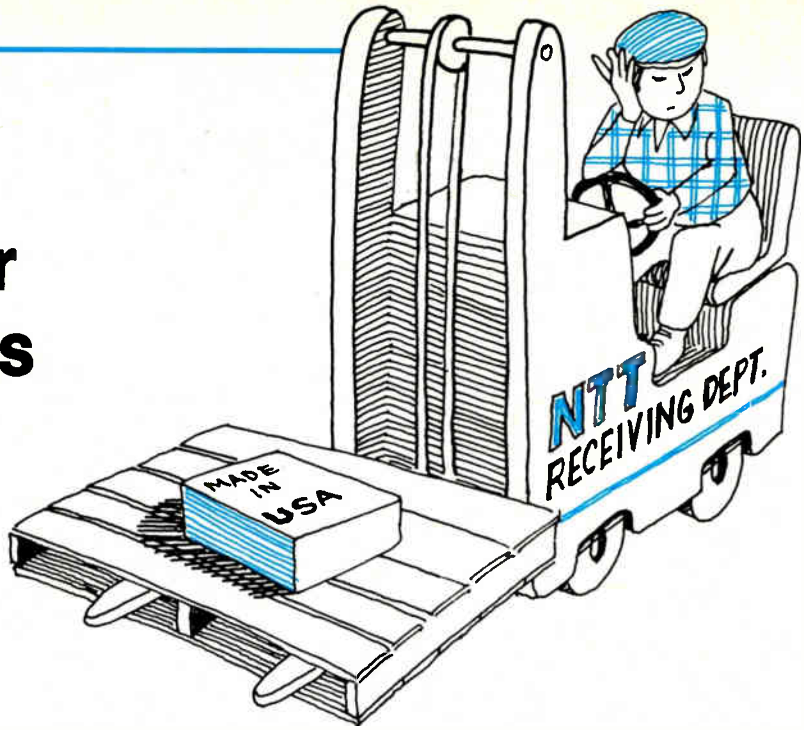



# NTT's open door draws no crowds

Evaluation of buy-foreign policy at end of its first year shows that company is cooperating but potential U. S. suppliers are disappointingly nonaggressive

*by Robert Neff, Tokyo bureau*

**One year ago,** the U. S. won a key battle in the seemingly endless war to force open Japan's import markets: under relentless pressure from Washington, the Japanese government ordered Nippon Telegraph & Telephone Public Corp. to drastically liberalize its procurement policies so foreign suppliers could have a realistic chance of selling to the telecommunications monopoly.

It also agreed to significantly speed up type approvals for foreign gear aimed at Japan's $800-million-per-year interconnect market. American suppliers, confident of their telecommunications prowess, began dreaming of cashing in on NTT's $3.3 billion in annual procurement. The only question, they said, was whether NTT would implement its promises in good faith.

Now that the first year has passed, how is the new agreement working? Juries in both countries are still out. But experts on both sides, while cautioning that it is too early for even preliminary conclusions, agree that NTT is bending over backward to cooperate with would-be foreign suppliers. Perhaps more surprisingly, most hands also express disappointment at a perceived lack of aggressiveness by U. S. firms

"NTT has gone way beyond our expectations," says one U. S. official, noting that the company has printed its procurement procedures in English, conducted three seminars for potential foreign suppliers, and established more flexible rules for bid-qualification applications than the 45 other Japanese government agencies covered by the government procurement code set down in the General Agreement on Trade and Tariffs (GATT). NTT has also established a special team in its engineering department to deal with foreign suppliers and has another office specifically charged with implementing the agreement.

**Hanging back.** Observers do not give such high marks to U. S. companies that stand to benefit from NTT's new penetrability. "Not enough foreign companies are going through bidding prequalification procedures," says Robert F. Connelly, executive vice president of Procurement Services International, a new Tokyo-based firm that provides daily Telex reports in English to worldwide subscribers on Japanese government tender announcements.

NTT officials profess similar disappointment. "American suppliers are not participating as positively as we expected in our procurement procedures," says Takehiko Hashimoto, deputy director of NTT's procurement policy division.

There are three procurement tracks (see "Getting untracked in Japan," p. 59). Ichio Kata, a senior manager in NTT's procurement and supply bureau, reveals that through November, nine foreign companies had won Track 1 bids, for basic, off-the-shelf items, worth a total of $3.5 million. NTT's total Track 1 bid awards through November were $34.5 million. Eight of the nine foreign winners were American or U. S.-Japanese joint ventures. Kata notes that 27 foreign firms, including 23 from the U. S., have so far qualified to bid in Track 1. By comparison, 104 Japanese firms have qualified and 32 have won orders.

U. S.-related winners to date are: Sumitomo, 3M, and Graham for magnetic computer tape; Advanced Semiconductor Materials, Perkin-Elmer, and Varian for semiconductor production equipment; Digital Equipment Corp. for a minicomputer system, and Calma and Applicon for graphic design systems. Kata says he expects purchases from foreign suppliers to grow by the end of fiscal 1981 in March. By then, NTT plans to be able to announce Track 1 tenders worth $313 million for 63 different products.

But Track 1 accounts for only about one eleventh of NTT's procurement. Fully $3 billion this year will go for Track 2 and 3 purchases, covering more sophisticated equipment, and Tracks 2A and 3A, for follow-on sales. By the end of November, NTT had requested applications for the supply of eight products from these tracks. As of Nov. 30, it had received 19 Japanese applications but only one from an American firm—Motorola is one of 10 applicants to provide mobile telephone gear under Track 3A.

To be sure, far more foreign firms made inquiries. American Telephone & Telegraph Co., for example, responded to NTT's announcement on digital echo suppressors by arguing that its own nascent echo-canceler technique is superior. Sources say NTT is likely to invite proposals soon under Track 3 for development of such technology.

Also lackluster so far is foreign response to the new opportunities in the interconnect market, in which users of the NTT network can buy their own telephone and data-communication equipment from private suppliers. Before the bilateral agreement took effect on Jan. 13, foreign suppliers had won type approval for their interconnect products under severe and dilatory NTT type-approval regulations. Since the far simpler and faster procedures have taken effect, though, only one foreign firm has won approval. That company, the Santa Cruz, Calif., division of Plantronics Inc., in June started selling headsets in Japan through the giant trader, Sumitomo Corp. On the other hand, adds Phil Battey, marketing vice president, selling his headsets to Japanese government agencies is much tougher.

**Language barrier.** Battey is not the only American businessman to express frustration at trying to market to the Japanese government. One oft-cited problem is language. Tenders and requests for proposals are in Japanese and must be responded to in kind, often within 30 days. Others complain that NTT is much too picky. Hewlett-Packard, for example, gave up even attempting to sell oscilloscopes to NTT after learning it would have to replace the inch-denominated front panel screws with ones of metric standard, says Kata. Still others complain that NTT has been slow to announce big-ticket items.

Many experts view these complaints as petty, however. "The Japanese speak our language and I spent about three years learning theirs," says Donald L. McDougall, Massachusetts-based director of Japanese business development for Data General Corp. "I don't think it's a fair criticism." NTT's Kata claims that in most cases, foreign firms respond to tenders with products that do not even come close to NTT's specifications and are far more reluctant than Japanese suppliers to modify their products. "Some tell us we should buy products based on their specs," he says.

**Heavy-handed approach.** Indeed, some American executives sneer at the amateurishness of their peers. "Some are so unsophisticated as to write letters in English saying, 'Just tell us what you need. We can get you anything,' " Connelly claims.

By contrast, such U. S. firms as Motorola and AT&T appear to recognize that profiting from NTT requires considerable investment. Motorola spent fully three years working closely with NTT before finally winning the right last month to start selling pocket paging devices to NTT local operating companies. It joins five Japanese firms already supplying such devices but hopes to sell as many as 30,000 next year alone. "It took us three years to learn about NTT and the Japanese way of doing business," says Kazuo Suzuki, director of engineering at Motorola Communications Japan Inc. "We had to design a brand-new product from scratch."

AT&T is a far more recent arrival, having opened a one-man office in Tokyo in September. That man is Ron Green, managing director of AT&T International-Japan, and he estimates his first-year start-up costs at $250,000. "That's a big up-front expense," he concedes. "By the end of the first year I think we should have a good fix on our potential. If it's good, we will keep our office here and reevaluate it in a year."

Green makes clear that AT&T believes penetrating NTT requires a presence in Japan. His initial function is to gather market data and identify areas where AT&T could introduce its products. Already he is zeroing in on digital toll-switching machines with which AT&T is replacing its electromechanical switching equipment in the U. S. He describes the AT&T No. 4 ESS electronic switching system as the most modern and powerful in the world and adds, "We think it has a place in the network in Japan." At roughly $16 million per unit, it would convert AT&T's heavy initial investment into a tidy little profit.

Other U. S. firms are especially intrigued with the potential of Track 3, specially designed equipment. "It's genuine that NTT wants this partnership in R&D," says one American executive who has done business with the company. "Being a partner is a big advantage for us over the long run. But it's good for them, too—tapping overseas technology they couldn't before." □

## Getting untracked in Japan

There are three so-called tracks through which U. S. suppliers may sell to Japan's telecommunications giant, Nippon Telegraph & Telephone Public Corp. The first was established under the government procurement code of the General Agreement on Trade and Tariffs, or GATT. The other two were set up under a bilateral agreement with the U. S. All three aim to "provide nondiscriminatory competitive opportunities to both domestic and foreign manufacturers."

Track 1 is for the purchase of such basic off-the-shelf products as data terminals, private branch exchange and facsimile equipment, batteries, conduits, and instruments in lots worth at least $200,000. Track 2 comprises equipment already on the market that can be used as is or with modification; Track 3 encompasses products that must be specially developed for or with NTT. For follow-on purchases of such equipment, they are designated Tracks 2A and 3A. **-R. N.**

Computers

# Home computers: a corporate puzzle

As more employees acquire their own desktop machines, company data-processing centers must provide ancillary services

by Tom Manuel, Computers & Peripherals Editor

**Computing at large** corporations has been inexorably moving from the fortress of the big data-processing computer rooms into the offices and onto the desks. This redistribution of computing is now accelerating, propelled by several recent technological developments. Personal computers, local networks, office automation, and computer graphics are creating major waves in the information-processing environment of large organizations.

Perhaps the most visible impact is that of the growing tide of personal computers flowing into large organizations. Operating professionals and middle-level managers are using them as personal productivity tools. They are buying them any way they can—about half use their own money—because they need them to do things that the corporate data-processing department cannot.

At an executive conference sponsored recently in New Orleans by International Data Corp., the talk was about the impact of various new computer technologies on large information-processing operations. Those attending agreed that the role of the centralized data-processing center must change: it can no longer try to be the provider of all computing and computer-related services for the company.

Integrated electronic office systems and isolated personal computers are creating a clientele with "computer smarts." What these customers need from the corporate data-processing department is different from what has been provided in the past.

The DP center cannot serve the total computing needs of these workers, executives concede. Office automation, to be successful, has to start small and grow at a rate that can be absorbed smoothly, whereas DP groups are accustomed to large projects and long-range plans. Personal-computer users are isolated from the big machines at first, but as their applications and expertise grow, they see a need for access to company data on the big computers.

As well as access to the mainframes, DP departments can provide such services as modern program-development tools and training. They also can provide data bases and data-base management; application-level connectivity among the company's computers—not just hardware or file-level interconnection—through higher-level protocols; and integration of the personal computers into the company's total information-processing environment. Finally, they can negotiate volume purchase agreements for personal computers—in effect, become an in-house computer store—and coordinate access to public data bases.

**No toys.** Some typical DP departments have not figured out how to deal with personal computers. At first they ignored them or thought of them as toys—a mistake, because the personal computers being bought today are as powerful as the mainframes of the 1960s.

The capabilities of the personal computer are being rapidly recognized, and their enhancement of personal work productivity is quickly proven. In fact, many corporate users estimate that the personal computer pays for itself in just a few months.

A huge market is coming alive. *Electronics* estimates that the U. S. consumption of small business computers and personal computers costing less than $10,000 will be $2.5 billion in 1982 and will grow to $6.4 billion in 1985. Four market research firms, International Data of Waltham, Mass.; Venture Development Corp. of Wellesley,

**Coming on.** One estimate is that IBM's new Personal Computer will capture 30% or more of the market in a few years. Another sees a bigger lead.

Mass.; Strategic Inc. of San Jose, Calif.; and Future Computing Inc. of Richardson, Texas, all tend to agree that the U.S. installed base in 1980–81 is about 1 million units and that it will triple by 1984–85.

In two recent studies of personal computer users, one question dealt with the size of company employing the user. In a Venture Development survey, 13.2% of the sample works for companies with annual revenues of $250 million or more. In one just published by Newsweek magazine, 17% of the sample of users and owners work for companies with 2,500 or more employees.

**Used for business.** In the Newsweek study, business applications are the most frequently mentioned expected uses (53%). Also, 48% of the respondents did not pay for the computer themselves. The median price paid for each computer was $1,926 for the initial purchase—$2,325 was the median spent by those working for smaller companies and $1,643 for those working for larger companies.

International Business Machines Corp. is by far the major influence in large-scale data processing. Now that it is also in the personal computer business, IBM should have considerable impact in that sector, in particular with large companies.

International Data estimates that IBM will take a 30% or greater share of the personal computer market in a few years. Future Computing Inc. is projecting that the IBM Personal Computer's retail sales volume will match that of the two current leaders, Apple and the Radio Shack TRS-80, in 1982 at or near the $400 million level each. By 1985, IBM will be way ahead of the other two with annual sales of about $1.6 billion and Apple at $800 million and TRS-80 at $500 million to $600 million, says the market researcher.

IBM probably entered the personal computer market because it could see computing moving onto the desks of workers and away from the Armonk, N.Y., company's traditional source of revenue, the large mainframes in the big data-processing centers. Though the mainframes are not going to go away, the really explosive growth segment of the total computer and information-processing market—perhaps the biggest growth market for the rest of the century—is the personal productivity tool represented by personal computers and integrated personal work stations. But for those users of personal computers who may want to connect to mainframes, IBM is promising to have an emulation of a subset of 3270 terminal software for its Personal Computer.

**Swelling market.** In a recent report on the computer giant's new baby, Future Computing states, "IBM will also expand the Fortune 1,000 market for professional users. This is the area where IBM will have the greatest impact. The DP managers have strong influence on the product selection, and they will overwhelmingly select IBM."

The company, of course, recognizes this, and that is why the Personal Computer will be sold by IBM's new Information Systems Group, in the National Accounts division.

By using the Intel 8088, a 16-bit processor with 8-bit data and input/output paths, IBM has surpassed Apple and Tandy Corp.'s Radio Shack in processing power by offering essentially a 16-bit personal computer. Also, it would not be difficult to offer an upgraded version of the Personal Computer with a full 16-bit processor, such as the 8086 or the even more powerful iAPX286.

Both Apple and Tandy must introduce products based on bigger processors to keep from losing too much market share to IBM. Tandy is expected to unveil a model based on the MC68000, and Apple has gotten over some initial problems with its Apple III, still an 8-bit processor but more powerful than the Apple II.

Apple also has to worry about its retail distribution channels. It must maintain good relationships with distributors and computer stores and convince stores taking on the Personal Computer not to drop Apple. The company is also trying hard to reach the large corporate customers through its recently introduced National Account Program.

Tandy, on the other hand, does not have to worry about losing its distribution channel. But, if it wants to keep a market share in the large companies, it will have to make some new changes in marketing strategy.☐

Solid state

# VLSI schools popping up

## Courses teach systems engineers chip layout using design automation and Mead-Conway approach

*by Terry Costlow, Costa Mesa bureau*

**As chip designers** come to grips with very large-scale integration, the advantages of the technology are being disseminated to systems designers by private schools springing up throughout the industry. The classes range from introductory overviews to actual hands-on sessions that include chip design and fabrication and serve to promote both VLSI and the silicon-foundry concept.

Whether simply introductory or more involved, the courses have two common threads: explanation of state-of-the-art automated-design offerings for VLSI use and centralization around the Carver Mead–Lynn Conway approach to design and fabrication as separate steps. Thus, their graduates can concentrate on design and leave production concerns to silicon foundries.

Two California firms involved in the fabrication of chips, VLSI Technology Inc. in Santa Clara and SynMos Corp. in Palo Alto, are paving the way in hands-on courses. Both VTI, a foundry for VLSI components, and SynMos, a broker that handles operations after design completion, hold detailed classes that include the actual fabrication of a chip designed in class by the student.

The courses are similar in content. Both discuss n-channel and complementary-MOS logic design and offer design-automation systems with software developed by the firm. Students at both learn some of the basics of IC design using the Mead-Conway textbook, "Introduction to VLSI Systems," and then design a chip of their own selection, which they keep.

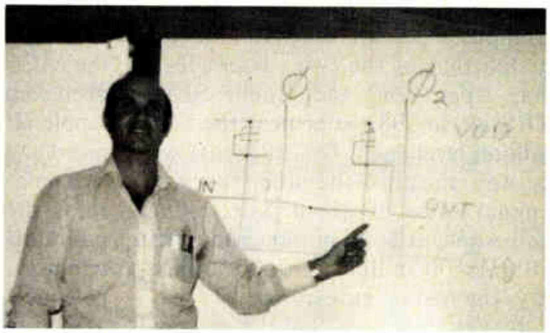
But course length and price vary sharply. VTI offers a four-week course that meets five days a week and costs $6,000. SynMos classes meet three hours a week over 10 weeks; tuition is $3,000.

Both firms are currently teaching their second groups. Burrel Smith, the manager of digital hardware at Apple Computer Inc., Cupertino, Calif., attended the first SynMos session and says, "You get an amazing amount of technology for the money. Apple will get immediate rewards back from the course."

The companies offer similar follow-up to the courses, video tapes and software that can be used to form in-house programs with graduates as teachers. This gives equal footing with larger firms that can afford internal training, they believe.

**Brings in business.** Both VTI and SynMos are start-ups that expect a twofold return from their educational endeavors. First comes the tuition revenue, which will help them stay afloat until their other services bring



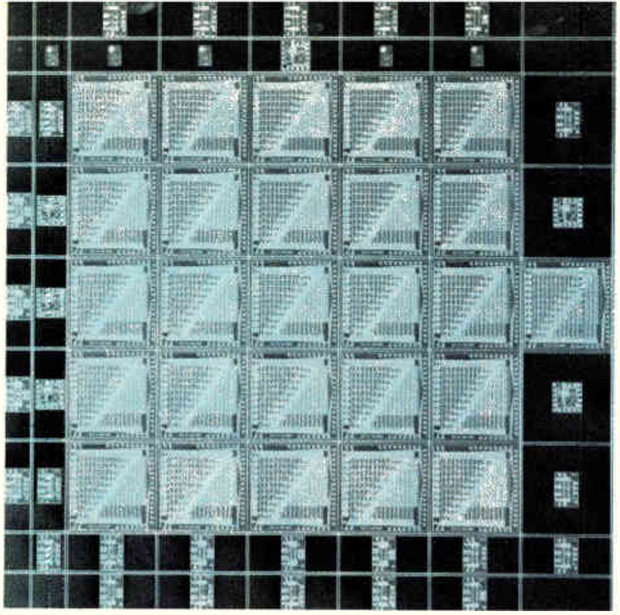
**Making a point.** Jim Lipman, above, director of training at SynMos, conducts a class at the company's VLSI school. The SynMos course meets three hours a week for 10 weeks, costs $3,000, and includes fabrication of a chip.

**Eye on VLSI.** VLSI Technology instructor Doug Fairbairn, left, uses the Mead-Conway technique to teach a class in MOS technology. The four-week course meets five days a week; the tuition is $6,000. The company's main business is as a silicon foundry for the fabrication of ICs.

in more revenues.

But the second benefit is potentially greater. In teaching designers from systems houses, the firms are mainly reaching companies without fabrication capabilities — potential foundry customers.

While both stress methodologies that are applicable to any foundry, they obviously emphasize software and processes with which they are most familiar. And the personal contacts may lead to contracts when the students convert their knowledge to products. "One main reason for the courses is to enlarge the customer base for both foundries and brokers," says Jim Lipman, director of training at SynMos.



**Parade of triangles.** This is a merged wafer, the fruit of SynMos's multiple-project–wafer concept of shared silicon technology. The Palo Alto, Calif., firm is a chip broker.

While the pair hopes to cultivate business over the long term, others have short-term interests in mind. Hellman Associates in Palo Alto, Calif., Integrated Circuits Engineering Corp. in Scottsdale, Ariz., and Western Digital Corp. in Irvine, Calif., have all begun courses. Hellman's are three-day affairs that offer a broad overview, while ICE's class offers some work with design automation. Western Digital offers classes geared to each firm, from an overview to complete instructions in design and fabrication.

As VLSI technology emerges, many predict a proliferation of schools, but they also see a trend that may be short-lived. Andrew Haines, marketing manager of VLSI activities at VTI, sees "a dramatic upswing in the next couple years, but then schools devoted solely to that will decrease." However, he predicts that some, like his, will continue for some time.

Carlo Sequin, head of the Computer Science department at the University of California at Berkeley, who teaches the Hellman course, feels "it will peak next year when enough of the people are informed." He then predicts people will use facilities that have design-automation equipment and software to design their chips.

**Some skeptics.** Detractors of the schools feel they may not last that long. Gene Potter, chairman of Silicon Systems Inc., a Tustin, Calif., custom house, says that once the foundry business takes off at the new firms, the teachers will be drawn into customer service. "You don't want your best designer teaching," he notes. However, both VTI and SynMos say classes are an important part of their plans and, as such, will not be compromised.

Other critics say that a designer cannot learn the full scope of IC design in a matter of weeks, that it takes months of daily work to learn the process well enough to do high-quality work. "That's not true," responds Frank Riherd, software engineer at Hayes Microcomputer Products Inc., Norcross, Ga. He recently attended the VTI course and asserts, "One of the things the course did was give me a very good idea of how to simply design a chip, by having me design one." Still, even instructors admit their students lack some expertise yet, but insist they make up for it in other areas.

"The chip done by a system designer might be bigger and not as fast as what an expert does. But a real expert may not be able to do it because he doesn't understand the system problem as well," maintains Haines. □

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Circle 65 on reader service card

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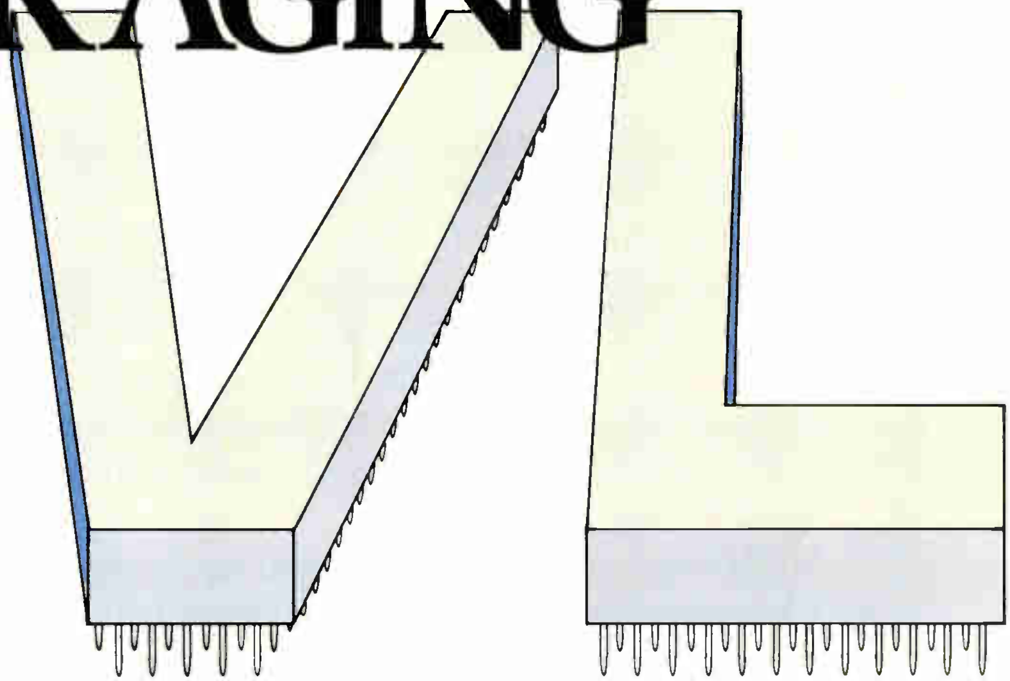


VHSIC's imperative also has been met by combining techniques, like flip chips with tape-automated bonding, to kick lead counts over the 100-plus goal

by Jerry Lyman, *Packaging & Production Editor*

□ Very large-scale integration has already fired the starting shot in the race to greater lead counts in integrated circuits. By 1985, ICs with pin counts of 200 to 300 will be commonplace, and the old faithful, the dual in-line package, will be relegated to small- and medium-scale ICs because of its excessive size.

Stimulated by the Department of Defense's Very High-Speed Integrated Circuits program (VHSIC), a number of companies are spawning whole families of new packages to compete for space on the large- and very large-scale IC boards. These include updated ceramic-glass DIPs (Cerdips) and plastic DIPs with pins on 50-mil centers, a wealth of leaded and leadless chip-carriers in plastic, and, newest of them all, the multilayer ceramic pin- and pad-grid arrays.

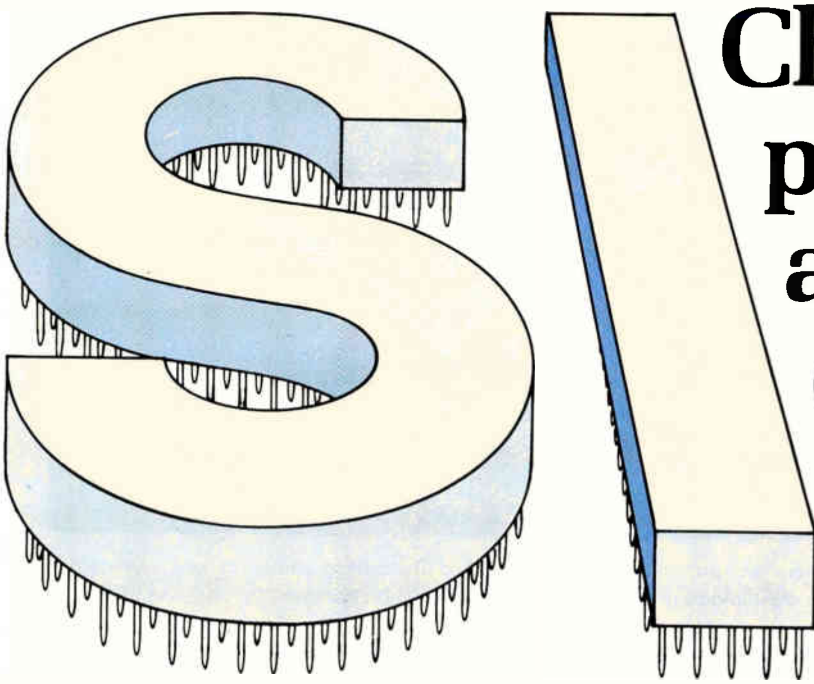
VHSIC participants like Honeywell Inc., International Business Machines Corp., and Texas Instruments Inc., among others, are generating innovative packages using either chips on tape in a conventional tape-automated-bonding approach (TAB) or flip chips combined with the new area TAB. Fantastic by today's standards, these techniques must perform to requirements for high gate density and superior power dissipation. The commercial package of the near future is sure to bear the imprint of these new developments.

Though these VHSIC-stimulated VLSI packages will eventually increase both density and chip speed, their more immediate effect will be on chip bonding and the design of package attachments and printed-circuit boards. New bonding and soldering methods will have to be developed to cope with these porcupine-like packages, whose leads and bonding pads will necessarily be on extremely tight centers.

The pc boards of 1985 will have much tighter lines and spaces than those of today. Small vias will replace plated-through holes in many of the next generation's designs as more and more components are surface-mounted. To meet these specifications for the next generation of boards, the pc industry will have to fine-tune its current manufacturing techniques and perhaps introduce new technology.

## A DIP renaissance

One of the newest packages available for LSI, the 50-mil DIP, is simply an adaptation of the DIP on 100-mil centers. It is available in Cerdip 64-, 48-, and 40-lead Diapak B packages from Diacon Inc., San Diego, Calif., and in a 64-lead plastic version from Zilog Inc. of Cupertino, Calif. Zilog is using its miniDIPs for the Z8 single-chip microcomputer and its peripherals.



# Chip-carriers, pin-grid arrays change the pc-board landscape

The 50-mil DIP takes up much less board space than its larger cousin. For example, a 40-lead version of the Diapak B takes up half the board space of a comparable package on 100-mil centers. In higher lead counts, the 50-mil version is even more effective—evident in the 64-lead miniDIP, which takes one third the board space of a full-size DIP. In fact, a 64-pin high-density DIP, when plugged into a special Robinson Nugent socket that accepts leads on 50-mil centers and converts them into dual rows of staggered leads on 100-mil centers, succeeds in taking up less board space than a standard 64-pin chip-carrier in a socket.

With only slight modifications, standard DIP-handling and -insertion equipment can be used on the new smaller packages. An additional advantage is that the Diapak B can be automatically wire-bonded by equipment that is available at the present time.

The Diapak B and its Zilog plastic clone will no doubt suit commercial and industrial board designs based on full-sized DIPs on 100-mil centers. The smaller DIPs can easily be designed into the 100-mil grid either directly or with the special sockets.

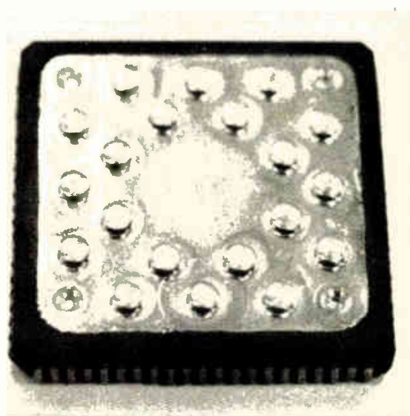
But perhaps the best use of this small package is to mount it directly on 50-mil centers—in fact, Diacon constructed pc boards just to demonstrate this. Further, military and aerospace customers for some time have been mounting chip-carriers on 50-mil centers on pc boards based on 100-mil grid spacing.

The leadless ceramic chip-carrier in all its forms—cavity up, cavity down, multilayer, single layer, square, rectangular—is now fairly well accepted by the electronics industry. More, all the major IC firms have been supplying IC chips in this type of package.

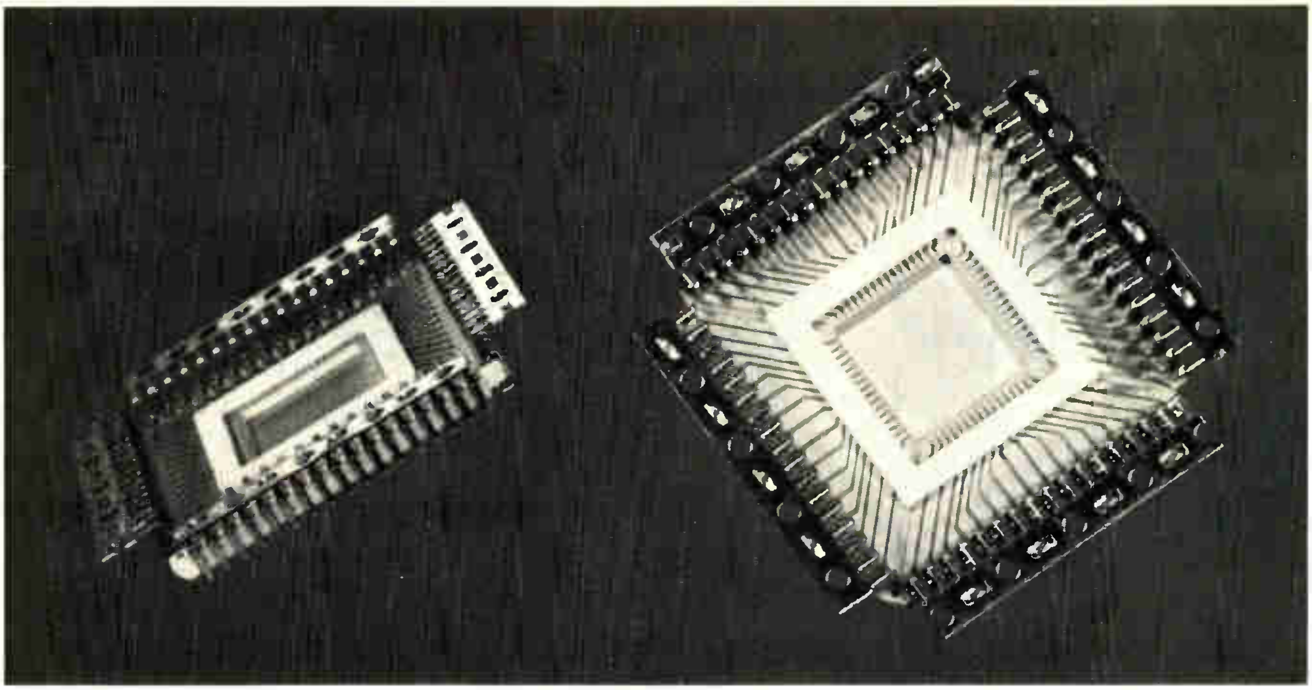
Though relatively costly, these reliable, hermetically sealed packages target military and aerospace use and similarly rugged environments. However, designers have yet to make such carriers easy to attach to conventional epoxy-glass pc boards. Usually what is needed is a metal and plastic composite board with a thermal coefficient of expansion matching that of the carrier's alumina [*Electronics*, Oct. 20, 1981, p. 155].

### Leading the way

But the industry was cheered by the recent arrival of a lower-cost, easily attachable version of the leadless carrier, the leaded post- and pre-molded plastic leaded chip-carrier (PLCC). Whole families of the packages are cur-



**1. VLSI in plastic.** By 1982 plastic leaded chip-carriers with extremely high lead counts will begin to be available. Illustrated is an 84-pin prototype package that was designed by Texas Instruments Inc. for a gate array.



**2. Leads that follow.** Solderable edge clips on 50-mil centers have proven to be a reliable method of attaching leadless ceramic chip-carriers to printed-circuit boards. The unit shown in the figure is manufactured by the Berg Electronics division of Du Pont.

rently being released by TI, Signetics, National Semiconductor, Intel, and Motorola. In fact, by the end of 1982 every major semiconductor firm expects to have products in the leaded carriers. The leads of the new packages are folded under the plastic body and are designed to be surface-mounted—part of an industry-wide trend in surface-mounting techniques that can also be used for small-outline devices and passive chips.

TI was the first IC company to supply IC products in the plastic carriers. The firm's product was designed according to the established Joint Electron Devices Engineering Council standard (mechanically similar to the earlier Amp Inc. premolded version). By the end of 1982, TI is expected to supply a complete family of these carriers, including 20-, 28-, 44-, 69-, and 84-lead units.

The company's 84-pin unit, shown in Fig. 1, was designed for a gate array. Interestingly, its optimization for heat transfer was accomplished by using a copper leadframe and attaching the die to an integral copper heat sink. Finning the heat sink produces a 25% increase in secondary surface.

**TABLE: STANDARD AND FINE-PITCH CHIP-CARRIER FAMILIES**

| Ceramic size (in.) | Terminal count | | |
|---|---|---|---|
| | 50-mil centers | 25-mil centers | 20-mil centers |
| 0.400 | 24 | 44 | 60 |
| 0.450 | 28 | 52 | 68 |
| 0.560 | – | 68 | 92 |
| 0.650 | 44 | 84 | 108 |
| 0.720 | – | 92 | 124 |
| 0.750 | 52 | 100 | 124 |
| 0.950 | 68 | 132 | 164 |
| 1.150 | 84 | 164 | 204 |
| 1.350 | 100 | 196 | 244 |
| 1.650 | 124 | 244 | 388 |

SOURCE THOMAS & BETTS

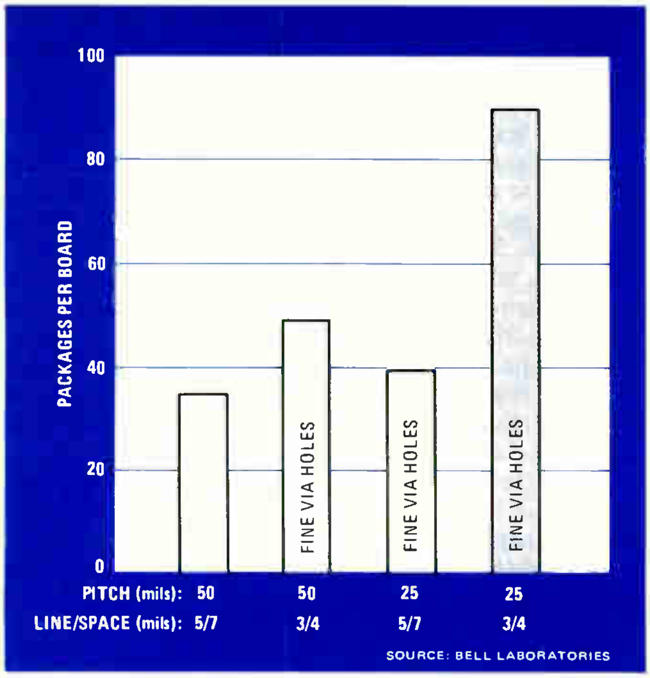
Signetics Corp., Sunnyvale, Calif., is also creating a family of products in 20-, 28-, 44-, 68-, and 84-pin postmolded plastic leaded carriers. The 68-lead unit is also aimed at gate arrays, and the firm is in the midst of temperature and humidity tests of chips encased in its 28-lead package.

Motorola also has an extensive program for the plastic carriers and schedules a full family in standard Jedec sizes by the end of 1982. National Semiconductor Corp. and Intel Corp. are other companies that have programs to develop postmolded versions.

The likelihood that by 1982 the plastic leaded package should be available from almost any IC manufacturer will have a large impact on all board designs. It is noteworthy that all the IC firms intend to put out postmolded packages in standard Jedec pinouts, with the hope that this may hold down the variety of packages that have to be tooled.

However, Amp Inc. of Harrisburg, Pa., has been making the unit in a premolded version since 1977. The Amp package is for users who wish to bond and seal-in their own chips into the carrier. Recent environmental tests on passivated chips sealed with silicone gel or RTV silicone rubber have shown the Amp premolded carrier does in fact hold up under humid conditions [*Electronics*, July 28, 1981, p. 44].

Since the IC firms were familiar with the manufacturing methods for the postmolded plastic DIP, it is not surprising they took the postmolded approach. However, Arnold Rose, manager of packaging technology for Signetics' Advanced Technology Center, believes that premolded units could additionally offer special advantages




**3. Change of pitch.** A decrease from 50 to 25 mils on centers in the input/output spacing of a chip-carrier means more leads per inch and thus more smaller packages per board. To fully exploit 25-mil spacing requires printed-circuit boards with 3-mil lines and spaces.

for certain types of LSI and VLSI chips.

He notes that a postmolded carrier's epoxy molding compound contains contaminants that could affect a chip's operation. The premolded carrier's Ryton plastic has none of these contaminants.

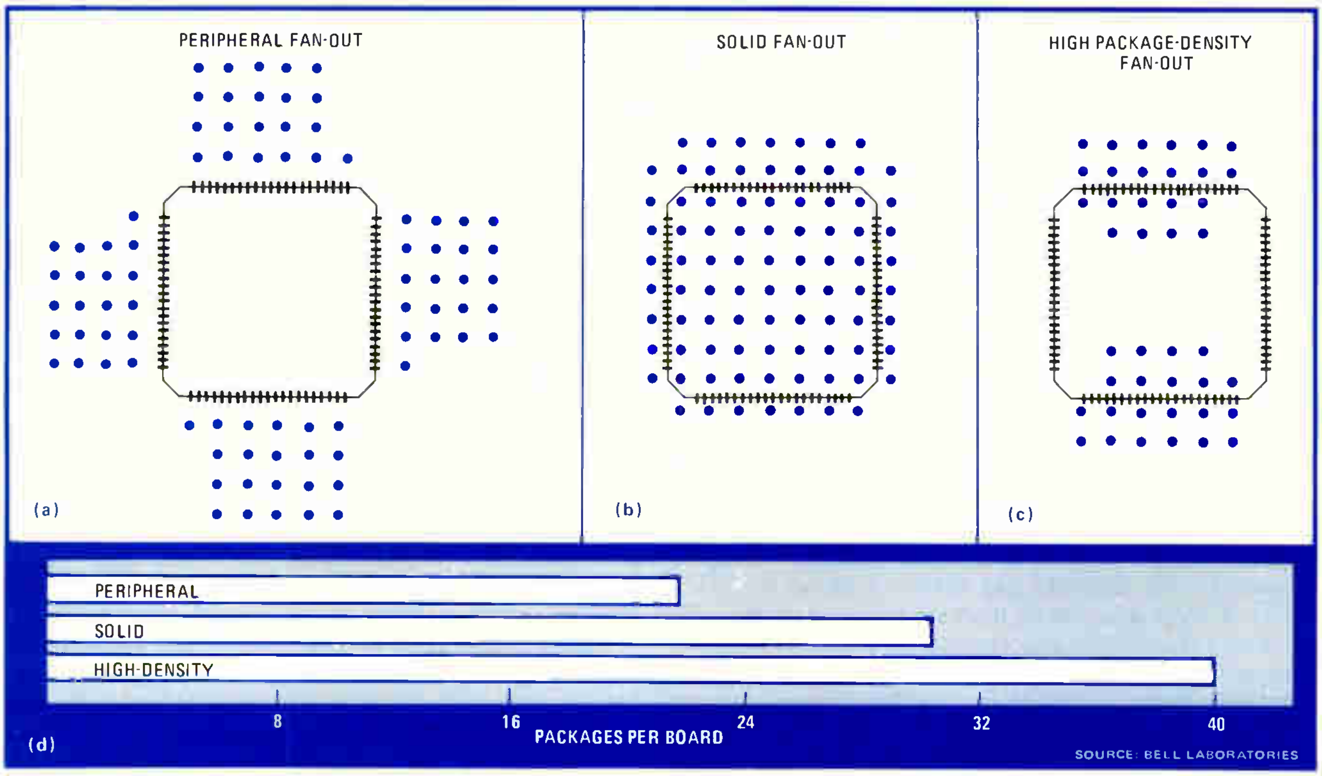
Rose further points out that postmolding puts a strain on a chip, a problem Signetics has confirmed by putting strain sensor patterns on typical chips molded in plastic. The strain was found to cause die cracking, piezoelectric effects, or even changes in thin-film ladder resistances in data-conversion chips. In contrast, the chip in the premolded version is bonded to an open cavity and covered with either silicone gel or RTV silicone rubber before a lid is put on. These two silicone-based materials cushion rather than squeeze the chip.

### An alpha barrier

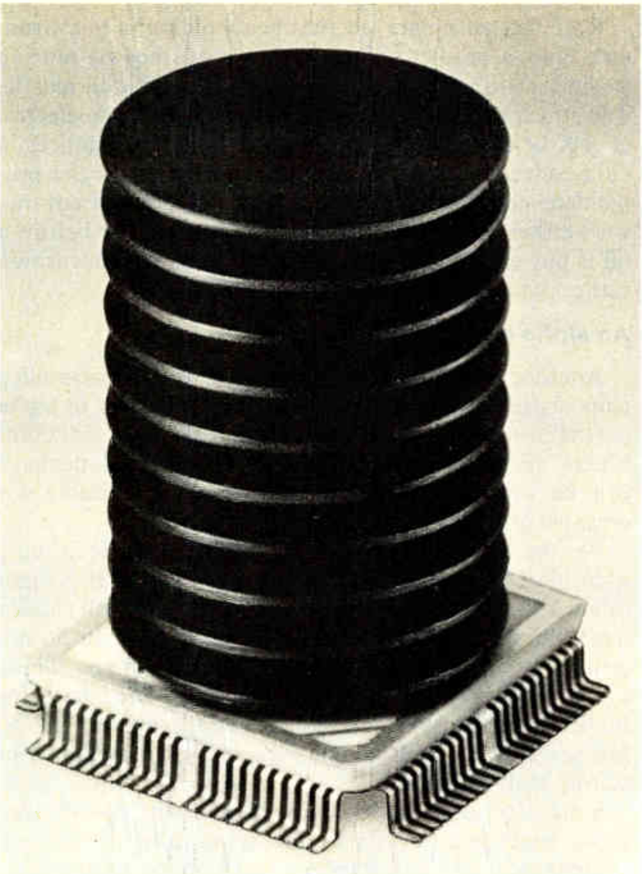
Another advantage of the silicone-sealed premolded chip-carrier is that the silicone acts as a barrier to alpha particles, which can cause soft errors in IC random-access memories. And finally, the premolded package can be sealed with a transparent cover suitable for erasable programmable read-only memories.

As the Cerdip followed the plastic DIP, it is only natural that a ceramic and glass chip-carrier should follow the plastic leaded chip-carrier. Diacon will shortly market a 68-pin unit of this type with leads on 50-mil centers and a 124-lead unit on 25-mil centers. These carriers can be supplied with a beryllia oxide base for higher heat dissipation. Signetics alone among the IC firms is working on developing its own in-house family of Cerdip chip-carriers.

Square ceramic leaded chip-carriers with side-brazed leads have been available for some time from such companies as 3M and Kyocera International. But another square leaded chip-carrier, the flatpack, is still extensively used in the U. S., Japan, and Europe. The package has flat banks of leads out of either two or four sides,




**4. Patterned.** Two of these chip-carrier via patterns are fully testable from both sides (a) or underneath (b). The third, however, being surface-mounted, is not testable in circuit (c). The bar chart (d) compares package density for the three patterns.



**5. Tightly spaced.** Amdahl's 580 computer uses this 84-lead ceramic chip-carrier with leads on 25- rather than 50-mil centers to house an emitter-coupled-logic large-scale integrated circuit. The tower-like heat sink dissipates up to 4½ watts with air cooling.

depending on the density of the enclosed chip.

The flatpack is the favored son of Japanese firms like Hitachi and Toshiba. For example, Takashi Kaiho, manager of technical marketing and sales promotion in Hitachi's semiconductor and IC division, expects its production line to use lower-cost flatpacks for more than other high-lead-count packages like the pin-grid array. Hitachi now makes three types of flatpacks—plastic, ceramic shielded by a metal cap, and ceramic shielded by low-temperature glass—all in versions with up to 100 leads. Kaiho expects the next development will be a 160-lead flatpack, but at the same time predicts that for ICs with even higher pin counts the company will resort to the pin-grid array—a ceramic chip-carrier whose inputs and outputs are a matrix of pins on 100-mil centers.

Toshiba mainly makes plastic flatpacks with 44 to 92 leads. Kiyoshi Ishikawa, manager of the assembly engineering group in Toshiba's Semiconductor division, expects plastic flatpacks and DIPs to take up the lion's share of its production in the next few years, primarily because the company concentrates on commercial applications, which seem to demand their use. But for packages with more than 92 leads, Toshiba also will look at the chip-carrier and the pin-grid array.

In the U. S., the flatpack is still heavily used in military applications, though a few computer firms make use of it for high-speed logic. It is interesting to note that the flatpack is the choice of one of the competitors in the VHSIC program's phase I, which specifies IC features of 1.25 micrometers. Yet flatpacks also can be suitable for VLSI applications because of their capacity for handling up to 156 leads.

An alternative approach to the leaded ceramic chip-carrier is to solder edge clips to the input/output pads of leadless ceramic chip-carriers. These clip-on devices, shown in Fig. 2, can be used in the "leads last" approach, where a user, by attaching the leads at his facility, can minimize lead damage from shipping and handling—the potential for damage expands in direct proportion to the IC lead count. An additional advantage to using edge clips, which can be soldered, is that if damaged they need not be scrapped along with an expensive chip, but can be easily removed and replaced or repaired. In other types of IC packages with high pin counts, pin or lead damage occurring during transit is often irreparable.

Clips of this type are available from Berg Electronics division of Du Pont, New Cumberland, Pa., and NAS Electronics, Hackensack, N. J. Besides the solder application, leads may be shaped for surface mounting rather than insertion into plated-through holes. Sperry Univac, Digital Equipment Corp., and Western Electric are some of the companies that have been successfully attaching these clips to leadless carriers.

### Smaller package makes its pitch

As the standard leadless chip-carrier with its 50-mil I/O spacing reaches the 100- to 124-terminal range, it becomes increasingly inefficient in its use of space. For example, a 100-terminal 50-mil carrier is 1.35 inches on a side—a dimension that has caused packaging designers to look to other, smaller alternatives such as the fine-pitch chip-carrier and the pin-grid array.

At present Jedec is in the process of standardizing two families of 20- and 25-mil–center chip-carriers in the existing Jedec ceramic sizes. The table compares the 50-mil family with the newly proposed 20- and 25-mil fine-pitch chip-carriers.

Other attractions offered by the fine-pitch chip-carriers are their greater interconnection density and better electrical performance due to shorter runs on the carrier's ceramic. However, they still involve a stretch for today's pc fabrication capabilities.

The key parameters in applying fine-pitch leadless carriers were listed in a paper entitled "Fine-Pitch Carrier Routability Study," given at the recent International Electronics Packaging Society meeting in Cleveland by Nick Teneketges and Wulf Knausenberger of Bell Laboratories, Whippany, N. J. These included chip-carrier pitch, number of signal layers, line widths and spaces, via land size, fan-out pattern, and the number of I/O terminals on the package.

Figure 3 compares 50- and 25-mil–pitch 84-pin carriers on an 8-by-13-in. board with two signal layers. Merely increasing the pitch does not increase packaging density significantly—only by going to 3-mil lines and 4-mil spaces will there be a large increase in density. And boards with this resolution and the small vias required are not yet commercially available.

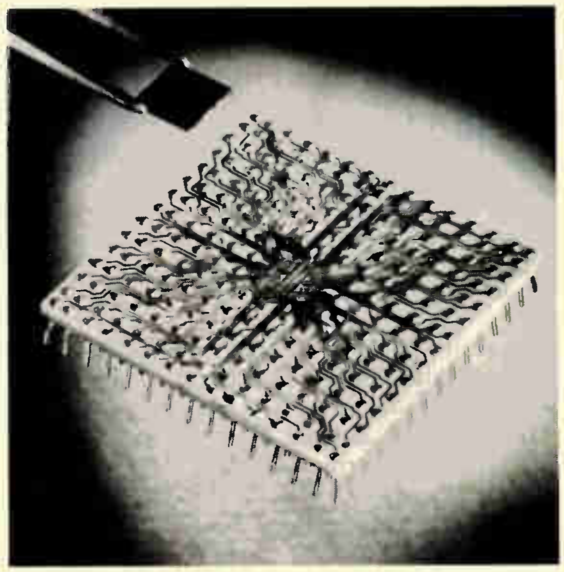
## A thin-film pin-grid array

How to interface a very large-scale integrated circuit with 354 solder bumps to 216 connector pins in a minimum volume while minding coupled noise and heat dissipation is not an everyday problem. But the innovative engineers at IBM's Essex Junction, Vt., facility tackled it recently when they decided to package the experimental IC that contained on a single chip the equivalent of the System 370's entire central processing unit [*Electronics*, Oct. 9, 1980, p. 139]. This large complex chip, 1/4 inch on a side, contains an array of 5,000 gates.

IBM's standard pin-grid arrays, which are multilayer thick-film ceramic cofired types, could not handle the complex wiring required for the interface of this chip with any chip-carrier. To skirt this immediate obstacle, the company developed the experimental thin-film pin-grid array shown above. The new carrier was developed from a standard 187-pin module measuring 36 millimeters (1.42 in.) on a side. The pinout was increased to 216 by adding around the perimeter a row of pins that was re-formed to the standard 100-mil centered grid. All the thin-film wiring in the unit is actually on the top surface of the ceramic module rather than in internal thick-film conductive layers.

The experimental carrier has three layers of thin-film wiring built up through the deposition of chromium and copper alloys. Wiring widths range from 0.025 mm to 0.38 mm. Layers of polyimide insulation about 0.01 mm thick separate the wiring levels. Thin-film metalization is based on the technology in IBM's high-density memory chips.

The most critical wiring is from the IC's solder bumps to the metal pads of the chip cavity deposited directly under the face-down circuit. Here, because of the great number of solder bumps, only one conductor is allowed to pass through adjacent pads. Three levels of insulated wiring triple the area available for connection pathways.



Packaging density for fine-pitch chip-carriers is also sensitive to routing patterns. Three proposed routing patterns are shown in Fig. 4, two are fully testable patterns of vias where all points can be accessed (a and b), with the second occupying less board area. The third shows a high-density pattern (c) that occupies even less space but does not provide functional test sites. The figure also compares the packaging density for the three patterns(d). The high-density pattern can pack roughly 25% more packages than the solid grid.

Besides their problems with the second level of interconnection—to the pc board—fine-pitch chip-carriers are more expensive to make. Also, ceramic-package manufacturers point out that dimensional tolerances in the cofired ceramic process for the present may be a constraint, limiting the manufacturer of devices on 20- and 25-mil centers to the 175-to-200-pin range.

Another concern connected with the closely spaced carriers is how to effectively solder great numbers of closely spaced pads to some type of substrate. In the 50-mil-center carriers, vapor-phase soldering has been used quite successfully—but the technique has yet to prove its mettle for fine-pitch carriers.

### Striking a close lead

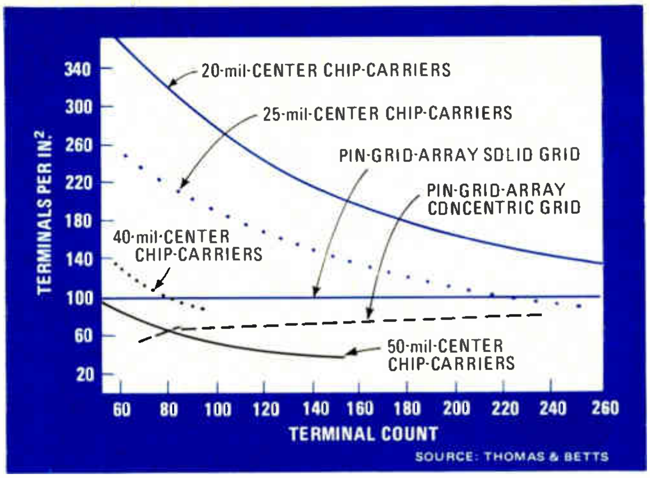
The trend toward closer lead spacing is noticeable in other package types as well. TI has proposed to Jedec a twin-row leaded plastic chip-carrier [*Electronics*, Oct. 6, 1981, p. 42], which has two staggered rows of leads on 50-mil centers, producing the equivalent of leads on 25-mil centers. Typically, a 124-lead package occupies the same room as a 68-lead version on 50-mil centers.

Flatpacks with tighter lead spacing are also becoming more common, especially in Japan. Fujitsu has a 90-lead flatpack with leads on 40-mil centers. Hitachi in its 44- to 60-pin models uses 40-mil spacing. For 80-pin types, Hitachi uses 32-mil spacing and for a proposed 100-pin flatpack, the company plans a 20-mil separation. Toshiba uses 27.6-mil spacing for its 92-lead flatpack.

In the computer world, Amdahl Corp. of Sunnyvale, Calif., and Fujitsu have been using leaded chip-carriers on 20-mil centers in their high-speed computers. The photo in Fig. 5 shows an Amdahl 84-lead side-brazed ceramic chip-carrier for an LSI emitter-coupled logic chip. This package is used in Amdahl's latest unit, the model 580—Amdahl's older model 470 uses the same type of carrier (though with different ICs). The 470's heat sink also differs from that of the present 84-lead carrier, which can dissipate more than 4.5 watts with its unique tower-like heat sink, also shown in the figure.

Despite Amdahl's success with fine-pitch chip-carriers, for VLSI most electronics firms now plan to go to a ceramic package with a pin grid rather than a peripheral-interconnection scheme. This package, which was originally conceived by IBM in the late 1970s, has become known as the pin-grid array.

The pin-grid array is a multilayered, cofired chip-carrier with a matrix or grid of pins on 100-mil centers on its bottom side. At IBM, a chip with solder bumps is reflow-soldered face down into the carrier's cavity. IBM's




**6. Grid versus peripheral.** These curves plot terminal density versus package terminal count for fine- and standard-pitch chip-carriers and pin-grid arrays. The terminal density for the fully gridded array is constant, unlike for the other package types.

arrays have up to 23 layers and 261 pins and often contain multichip arrays rather than a single chip. The company has also recently made experimental thin-film pin-grid arrays with an even higher wiring density (see "A thin-film pin-grid array," p. 71).

Commercially supplied pin-grid arrays are also available from 3M, Kyocera, Augat Technical Ceramics, and NTK Technical Ceramics. These units usually have three to four conductive layers and have single rather than multiple chips wire-bonded into their cavities. Commercial units have been fabricated with as many as 324 pins, and Kyocera has even made an experimental 1,024-pin model.

### Pinned to the board

The cavity-up aproach is IBM's usual choice for its pin-grid packages. But commercial units are supplied either cavity up or down, and even though the cavity-down style does not permit a full grid and presents some bonding difficulties, it is favored for chips that need high heat dissipation.

One of the most significant advantages of this new package—in the fully gridded approach—is that its number of terminals per square inch is constant with lead quantity. Figure 6 compares its terminal density with chip-carriers on centers spaced 50, 40, 25, and 20 mils apart. All the other packages have a decreasing terminal density with an increasing I/O count, which makes for larger package sizes. For example, a 100-pin fully gridded array is 1.1 in. on a side, whereas a leadless carrier with 100 terminals placed on 50-mil centers measures 1.35 in. per side.

The 100-mil spacing of its pins is the pin-grid array's other main advantage, because the carrier can then be wave-soldered or socketed into readily available pc boards that are made of standard materials and that have plated-through holes on 100-mil centers. The fine-pitch leadless carrier, on the other hand, requires a fine-line board of a nonstandard pc material.

And for in-circuit testing, a standard bed-of-nails fixture on 100-mil centers can connect with a board with pin-grid arrays on it, whereas chip-carriers with closer spacing will necessitate special fixturing in order to accomplish in-circuit testing.

Its requirement for blind soldering is the main disadvantage of any pin-grid approach, for the technique produces solder joints that can only be inspected by X ray. Clearly, the visual inspection possible with the solder joints of perimeter packages is preferable. In addition, the pin-grid array is extremely difficult to remove and replace in the field, unlike the chip-carrier.

As the number of pins on pin-grid packages increases, the spacing of the bonding pads and spaces around the chip cavity must shrink. This in turn leads to bonding difficulties with present-day equipment and techniques, the reason behind the major ceramic package firms' adoption of a two-tier array. In this configuration, the package's chip cavity contains two vertically stacked staggered rows of bonding pads allowing the use of common wire-bonding techniques, though in the end a more expensive package results.

With commercial fine-pitch chip-carriers still a few years off, then, the pin-grid array and the standard 50-mil chip-carrier are still the main warriors in the VLSI package arena. The crossover between the two is around the 84-to-100-pin mark.

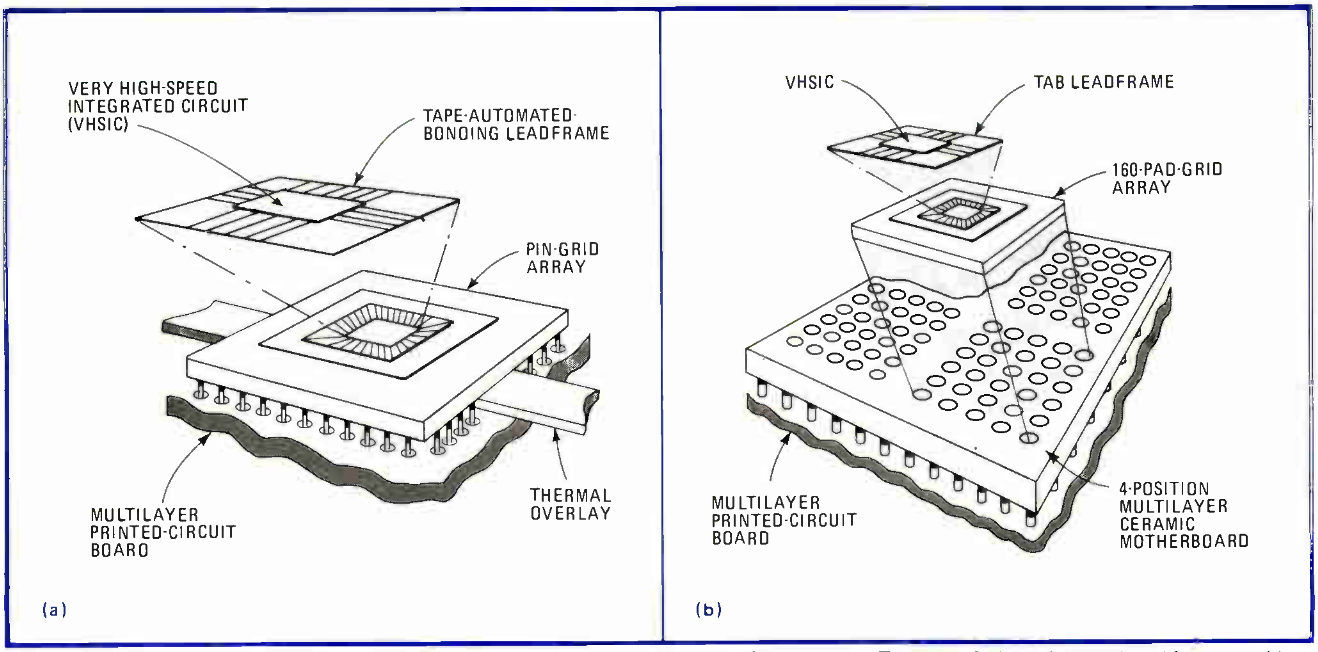
### Surface mounting versus through holes

Another choice facing the system designer is whether to go with the surface-mounting technology of the chip-carrier or the through-hole approach of the pin-grid array. Surface-mounted devices are soldered to the top-level conductors of a pc board, whereas through-hole device leads extend completely through the circuit board. Vias (small holes interconnecting board levels) are so much smaller than plated-through holes they can outnumber them by as much as five to one.

This difference in hole size limits the freedom with which second-level interconnections may be routed since the larger holes have the effect of reducing useful board area. Jon Prokop of TI, coauthor of "Design for VHSIC Packaging," a paper at the recent IEPS conference, notes that surface-mounted routing gives typically twice the density of through-hole routing. He cites an example of high-density interconnection that required 120 in. of wiring per in.$^2$ with 8-mil lines and spaces. In a surface-mounted application three circuit layers were sufficient to meet this requirement, whereas a through-hole mount required six layers.

3M, in St. Paul, Minn., has produced a variation of the pin-grid array that can be either surface-mounted or socketed and is known as the pad-grid array. It can be thought of as a pinless array with a grid of 70-mil contacts on 100-mil centers on its bottom face. The pad-grid array can be socketed similarly to 3M's QUIP [*Electronics*, Jan. 4, 1979, p. 130], but will face the same problems of attachment to standard substrates as the leadless carrier. However, the pad-grid array is equivalent to a low-terminal-count leadless carrier, which is relatively easy to solder to the standard glass-epoxy board. In fact, Honeywell is considering the pad-grid array in its packaging approach for the VHSIC program.

For the most part, though, the focus is on the pin grid,




**7. VHSIC packages.** For phase I of VHSIC, Honeywell proposes two package types. To the left is a large pin-grid array with a tape-automated-bonded chip in its cavity. To the right is a large pad-grid array that will house four such TAB chips.

which is currently being used or evaluated by such computer firms as IBM, Sperry Univac, Control Data Corp., and Storage Technology. Moreover, IC producers like TI, Motorola, National Semiconductor, Intel, and others are already looking at the device for units with over 100 leads.

Yet overseas, as in the U. S., there is continuing controversy over the relative merits of chip-carriers and pin-grid arrays. In Japan, Fujitsu and Hitachi use the pin grid. And Toshiba now supplies 120-pin-grid arrays and is planning a 256-pin unit. But Kiyoshi Ishikawa of Toshiba notes that a big problem in boosting pin count is a loss in productivity—he says that if wire bonding is used, more than 1 to 2 minutes is required per piece. Also, the pin grid's reduced spacing makes bonding accuracy chancy. He further points out that test sockets and pc-board design for pin-grid arrays are hard to make. For these reasons, Toshiba still sees advantages in chip-carriers for packages with over 100 pins.

At Siemens AG, Hans Ullrich, an engineering executive in the Munich firm's components division, predicts the future shakedown of the following packages for VLSI applications: leaded chip-carriers for up to 156 pins and leadless chip-carriers for more pins; bare TAB for up to 200 pins; and pin-grid arrays for up to 250 pins. At Philips, the pin-grid array also is foreseen as the most likely package for future high-lead-count IC chips.

## VLSI on tape

While the chip-carrier and the pin-grid array fight it out as the VLSI package of the future, it appears now that multileaded chips will be mass-bonded onto the popular types of chip-carriers and grid arrays.

In TAB, chips with special metalic bumps are mass-bonded to the inner lead patterns of spidery copper patterns etched on successive frames of a copper-coated, insulated film with a sprocketed format. In SSI work—14 to 16 leads—the outer leads of the chips on tape are mass-bonded to leadframes in preparation for eventual molding into plastic DIPs.

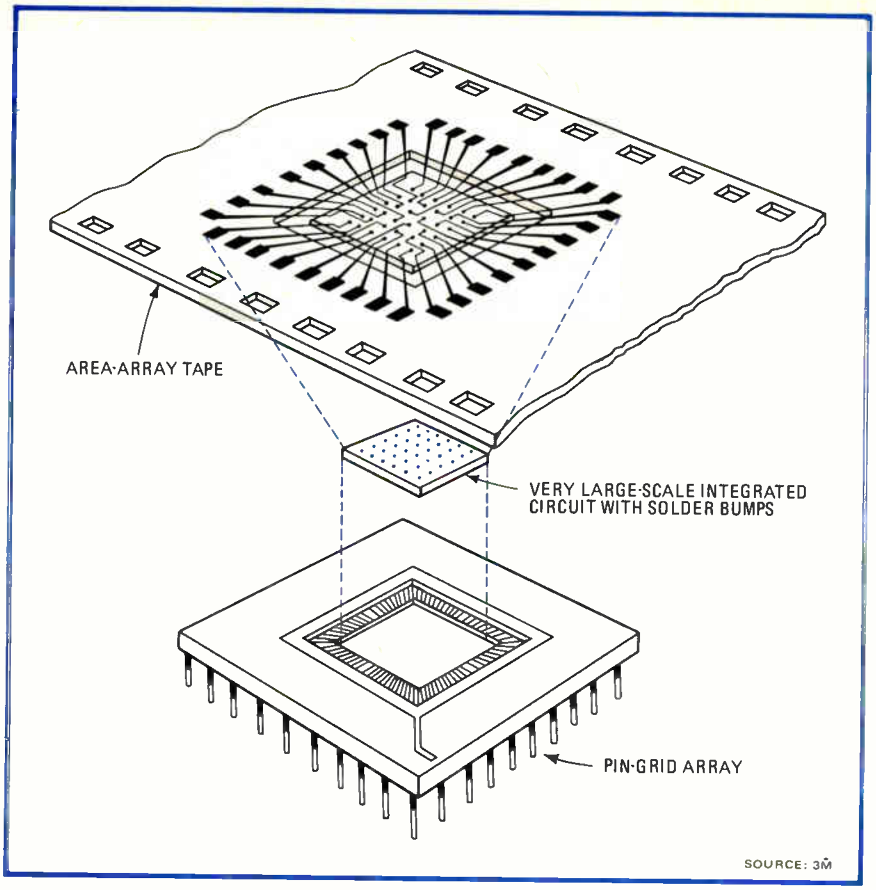
In a more advanced application of TAB—for example, at companies like CII-Honeywell Bull in France, Nippon Electric Co. in Japan, several divisions of Honeywell Inc., Bell Laboratories in Allentown, Pa., Westinghouse Systems Development Center in Baltimore, and General Dynamics Corp. of Pomona, Calif.—the TAB chip and its beam-like leads are excised from the tape frame and wire-bonded or soldered to thick- or thin-film conductors on large multilayer ceramic substrates [*Electronics*, Dec. 18, 1980, p. 102]. The maximum number of leads used in this mode of TAB—sometimes called bare TAB—has so far been limited to 40 in production applications.

As the number of IC leads increases, the bonding pads on the IC are squeezed together and TAB can take over where wire bonding cannot be used. For this reason, it appears that for the future VLSI and VHSIC chips with 100 to 300 I/Os, TAB will be a secondary package used mainly for its bonding ability. It is of course conceivable that new bonders or different wire-bonding techniques will come along to change this.

The present wire bonders tie 1-mil gold wires to 4-mil-square pads on 8-mil centers. What will be needed for the coming VLSI chips will be pads approximately 2 mils square on 4-mil (or smaller) centers.

Already, 3M has made samples of a 184-lead two-layer tape with inner leads composed of 2-mil lines on 5-mil centers. And Koltron Corp. from Sunnyvale, Calif., is in the midst of a program to demonstrate a high-lead-count three-layer tape with 2-mil inner leads spaced on 4-mil centers.

Both of these experimental tapes employ a plastic support ring to support the cantilevered leads. Some potential users would rather avoid the support ring because they view its plastic a possible source of contam-




**8. Area TAB.** An advanced VHSIC program proposed at Honeywell may use an area-array tape being developed by 3M. The area-array tape is basically a means of interconnection between a solder-bump array and a very large-scale integrated circuit. The tape's outer leads will be mass-bonded to pads on the cavity of the pin-grid array.

ination. To answer this concern, Koltron is researching various copper alloys that will simultaneously maintain rigidity without the support ring yet supply sufficient malleability for bonding.

In any case, the feasibility of manufacturing and mass-bonding of high-lead-count TAB must still be proven out. Still, the technique does have the potential of high-resolution bonding, testability, an ability to allow chip burn-in on tape, and suitability for automation—features that explain why several of the VHSIC phase I competitors are considering TAB designs in their packaging approaches.

### VHSIC packages

At the very apex of the packaging pyramid—where the glamor is—stands the challenge of finding suitable packages to house the fine-line, high-speed, multileaded ICs of VHSIC's phase I for 1.25-micrometer IC details. The participants take two basic approaches. One is to develop innovative new designs that will advance the state of the art, and the other exploits existing packaging technology to its limits.

The companies generating some of the more innovative ideas for VHSIC are Honeywell, IBM, and TI, the last of which has even hit on a variation of surface mounting it calls open vias. IBM has a system named Decal, and Honeywell envisions a special technique that combines TAB with the flip chip.

Honeywell's packaging ideas for phase I are shown in Fig. 7. On the left side of the figure, a 160-pin chip is mass-bonded into the cavity of a 160-pin-grid array whose pins are on 100-mil centers. A thermal overlay or bar in the multilayer pc board carries the package's heat to a heat exchanger. To save space, the same arrangement could possibly be manufactured in a similar package with pins on 50-mil centers.

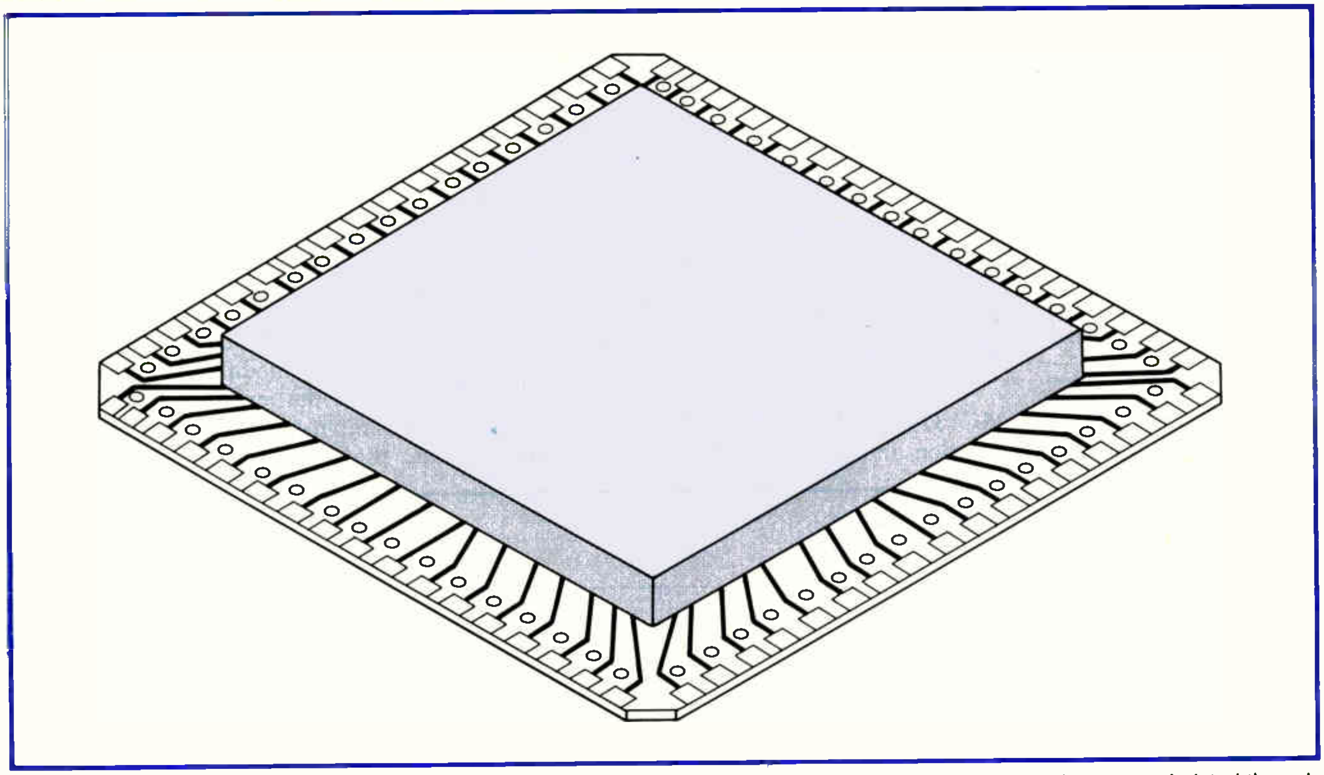
The right side of the figure shows a denser approach with 160-pad-grid arrays reflowed to a larger, pinned, multilayer ceramic board. Again TAB chips are bonded to the cavities of the four pad-grid arrays, a method that can be used with even larger arrays of chips.

In conjunction with 3M, Honeywell is considering a blend of TAB and the flip-chip or solder-bump techniques for advanced chips with 240 to 280 I/Os. A conceptual drawing of this method is shown in Fig. 8.

A VLSI chip connected with solder bumps is first die-bonded to the cavity of a pin- or pad-grid array. Then a special polyimide area-array tape is used to contact both the soldered chips of the IC and the bonding pads of the ceramic carrier. The area-array tape, unlike the conventional beam tape, has multiple layers. The area-array tape simply functions as a dense interconnection rather than as a leadframe, as in conventional TAB.

The major advantages of this concept are that it gives access to pinouts on the interior of the die and allows preassembly testing or burn-in of the die. Honeywell, through its Microswitch division, has over five years experience with flip chips, and 3M has a two-year VHSIC contract to prove out the area-array tape concept.

IBM Federal Systems division in Oswego, N. Y., is handling the packaging for IBM's VHSIC contract. In phase I, the company will provide a 240-pin version of its



**9. Open vias.** For VHSIC, Texas Instruments proposes an open-via leadless ceramic chip-carrier. By adding an inner row of plated-through holes on staggered 50-mil centers, I/O density for a standard chip-carrier is almost doubled.

standard ceramic module, where an IC with a flip-chip array is reflow-soldered to a multilayer pinned ceramic module with pins on 100-mil centers.

Another developmental approach by the Federal Systems division, for even higher lead counts, is the Decal flexible-film module. In this method the IC, with its solder bumps facing up, is mounted in the cavity of a pinned multilayer ceramic module. The solder bumps are reflowed to chrome-copper-chrome conductors plated onto a thin single-layer polyimide frame. Outer leads (6 mils wide) on the polyimide are then bonded to 6-mil pads on 12-mil centers on the side of the chip cavity.

The Decal method has several advantages over the company's standard ceramic-module method. It not only results in shorter lead lengths and higher thermal transfer, but also the interface of the solder bumps with the tape is more reliable over a wider temperature range than the link-up of the solder bumps and the alumina in the standard multilayer module. As with all IBM designs, the pinned array is on 100-mil centers.

## Open vias

In TI's VHSIC chip set, the company has selected surface-mounting chip-carriers over pin-grid arrays because they make it easier to mount second-level interconnection, they improve thermal management for conductor cooling, they are easy to remove from the board, and they raise system-packaging density.

In TI's brass-board phase I, standard Jedec 68- and 84-pin leadless ceramic chip-carriers on 50-mil centers will be used. For phase II—submicrometer IC details—the company will opt for the open-via ceramic chip-carrier shown in Fig. 9 because this mode gives almost double the I/O density of a standard chip-carrier in the same ceramic area.

The open-via scheme, named for the holes it uses, incorporates some of the features of both the chip-carrier and the pin-grid array while retaining the advantages of surface mounting like simplified board fabrication and easy removability. It involves two sets of I/O terminals.

The first set of terminals includes the normal peripheral contacts on 50-mil centers. The second set takes the form of rows of plated-through holes that are located in the body of the package and parallel to its edges. These vias are staggered on 50-mil centers.

TI and 3M are working together to develop a range of open-via ceramic chip-carriers with from 76 to 300 I/Os. An example would be a 124-contact open-via carrier that would take up the same 0.903-in.$^2$ surface areas as a standard 68-lead carrier. Both the outer and inner solder joints here are easily inspected. It is interesting to note that this device and the company's plastic chip-carrier with a staggered leadframe are designed to share the same pc-board footprint.

TRW and Motorola working jointly, Hughes, and Westinghouse are the remaining VHSIC phase I entrants. TRW and Motorola will use a 132-lead chip-carrier with leads on 25-mil centers. Hughes's approach is a 148-lead flatpack also on 25-mil centers.

Westinghouse proposes a package with leads with extremely tight spacing, a 200-lead chip-carrier on 12.5-mil centers. The firm has already built 0.7-in.$^2$ prototypes of this package that are designed to be placed on a pc board with a 50-mil grid and 3-mil lines and spaces. The company expects to bond the chip into the package cavity either by automatic bonding or TAB. □

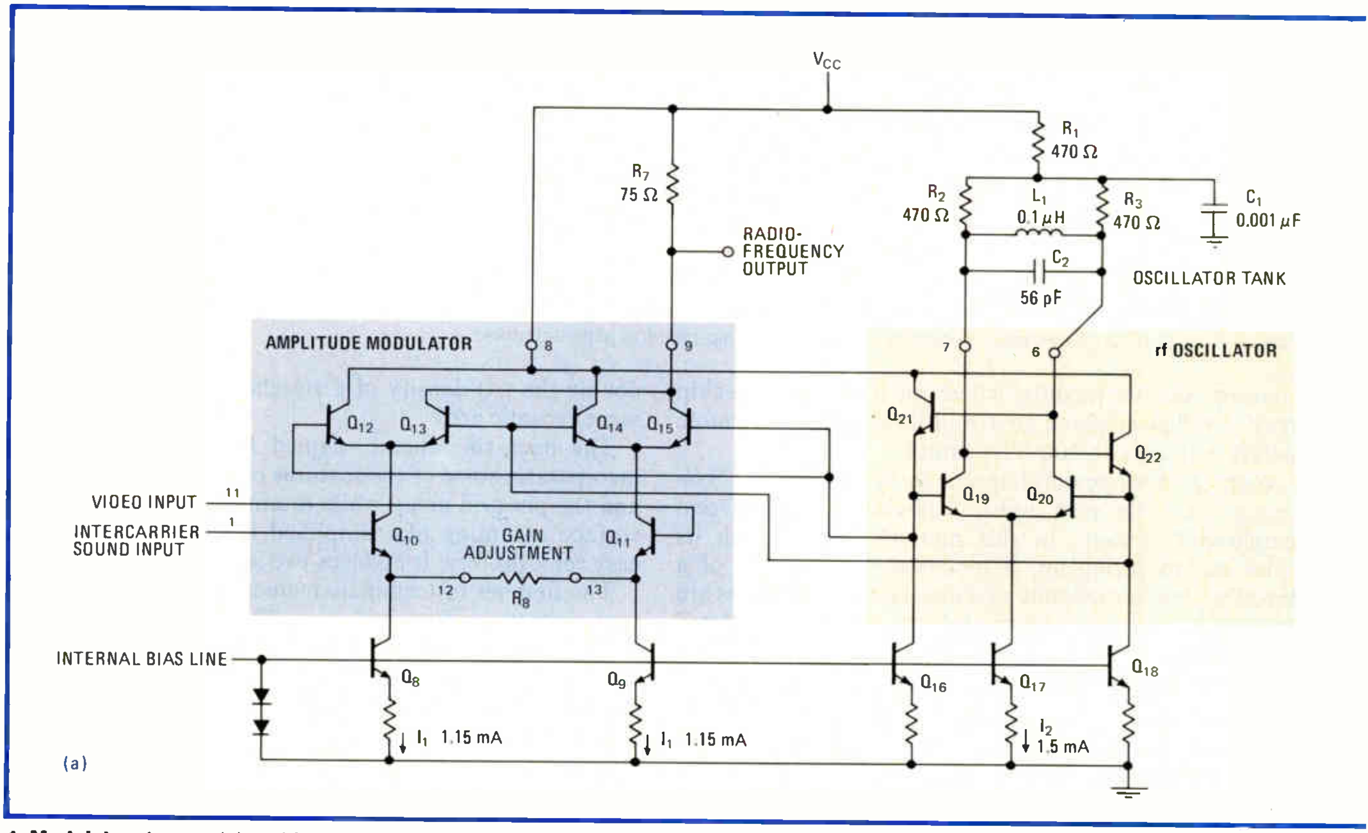
## Linear one-chip modulator eases TV circuit design

by Ben Scott and Marty Bergan
*Motorola Semiconductor Products Sector, Phoenix, Ariz.*

The fact that Motorola's MC1374 chip has both frequency- and amplitude-modulation and oscillator functions simplifies the design of a television modulator. The device is ideally suited for applications using separate audio and composite video signals that need to be converted into a high-quality very high-frequency TV signal.

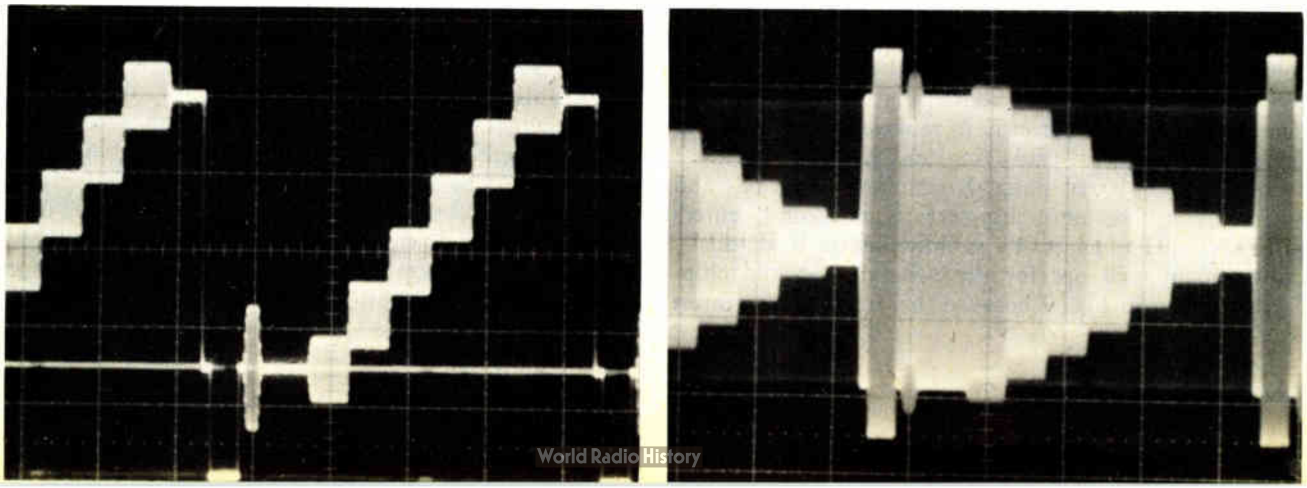
The a-m system (Fig.1a) of the 1374 is a basic multiplier combined with an integral balanced oscillator that is capable of operating at a frequency of over 100 megahertz. The fm oscillator-modulator (Fig.1b) is a voltage-controlled oscillator that exhibits a nearly linear output-frequency versus input-voltage characteristic.

This characteristic provides a good fm source with




**1. Modulator.** An a-m (a) and fm (b) modulator and oscillator are incorporated in the design of MC1374. The complete TV modulator circuit (c) uses a simple low-loss second harmonic output filter. Gain resistor $R_8$ is 2.2 kΩ for an intended video input of about 1 V peak at sync tip. With a 12-V regulated supply there is less than a 10-kHz shift of rf carrier frequency from 0° to 50°C for any video input level.

**2. Performance.** The IRE test signal (shown at left) is used to evaluate the video modulator. The resulting modulated rf output (shown at right) from the MC1374 has a differential phase error of less than 2° and a differential gain distortion of 5% to 7%.



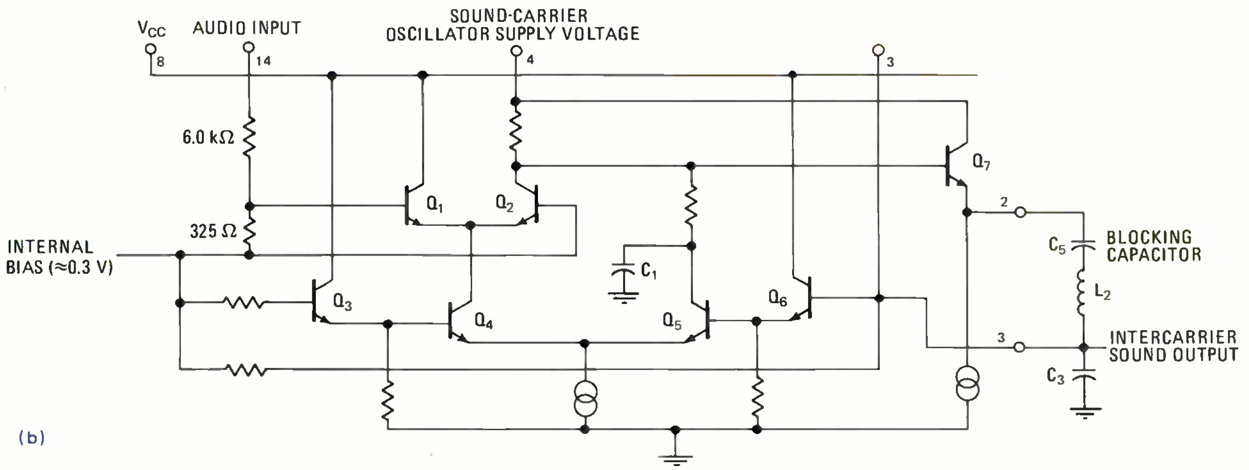
only a few inexpensive parts (no varactor is necessary). The system has a frequency range of 1.4 to 14 MHz and can produce a ±25-kilohertz–modulated 4.5-MHz signal with only 0.6% total harmonic distortion.

The a-m output for a complete TV-modulator circuit (Fig.1c) is taken at pin 9 through a double-pi low-pass filter with the load ($R_7$ = 75 ohms) connected across pins 8 and 9. Access to both (video and audio) inputs enables the designer to separate video and intercarrier sound sources.

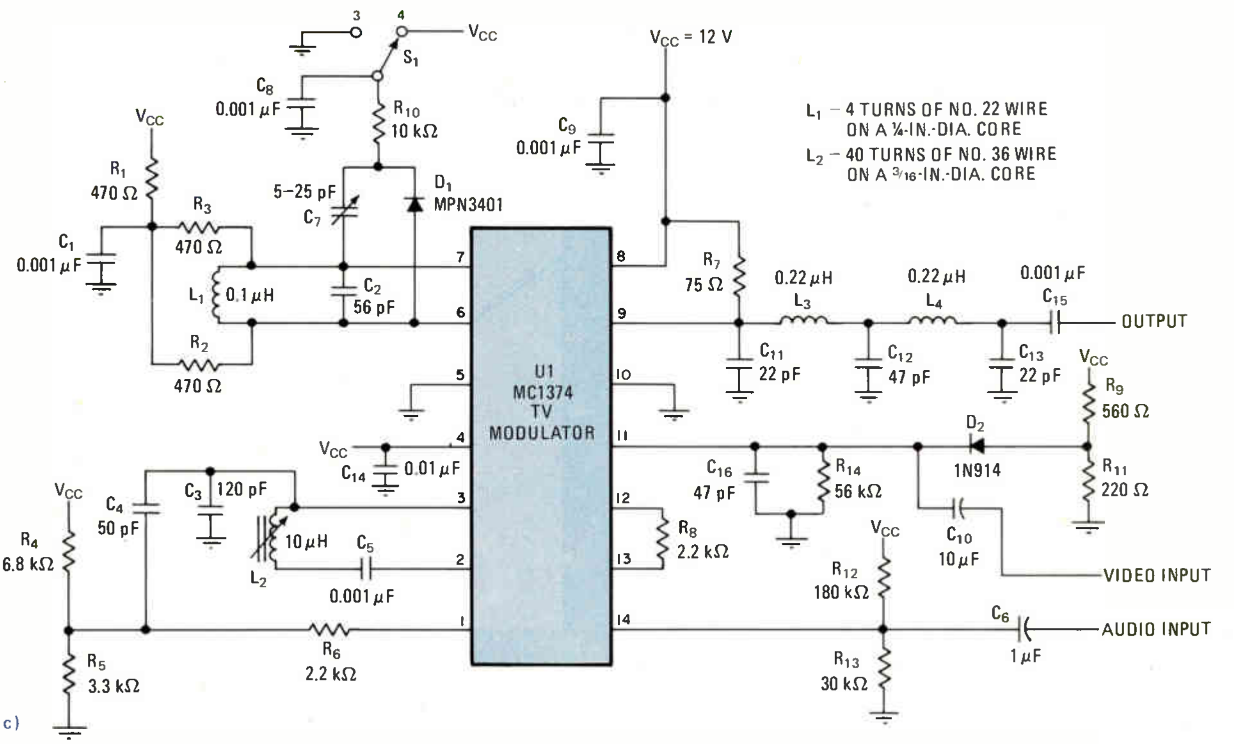
The gain-adjustment resistor ($R_8$) is chosen in accordance with the available video amplitude. By making $R_8 \cong 2$ (peak video) volts/1.15 milliamperes, a low-level 920-kHz beat is ensured. To keep the background noise at least 60 decibels below the standard white carrier level, the minimum peak video should be at least 0.25 V.

An oscillator for channels 3 and 4 (61.25 and 67.25 MHz) uses a parallel LC combination from pin 6 to pin 7. For this configuration, the value of coil $L_1$ is kept small and the capacitance large to minimize the variation due to the capacitance of the MC1374 chip (approximately 4 picofarads).

Sloppy wiring and poor component placement around pins 1 and 11 may cause as much as a 300-kHz shift in carrier frequency (at 67 MHz) over the video input range. This frequency shift is due to transmission of the output radio frequency to components and wiring on the input pins. A careful layout keeps this shift below




(b)




(c)

10 kHz. The video signal and the corresponding modulated rf output (Fig. 2) have a differential phase error of less than 2° and differential gain distortions of 5% to 7%.

The fm system is designed specifically for the TV intercarrier frequency of 4.5 MHz for the U.S. and 5.5 MHz for Europe. The fm system's output from pin 2 is high in harmonic content, so instead is taken from pin 3. This choice sacrifices some source impedance but produces a clean fundamental output, with harmonics decreased by more than 40 dB.

The center frequency of the oscillator has approximately the same resonance as $L_2$ and the effective capacitance from pin 3 to ground. In addition, by keeping the reactance of the inductor at a point between 300 and 1,000 Ω, the overall stability of the oscillator is ensured.

Optional biasing of the audio-input pin (14) at 2.6 to 2.7 V dc reduces harmonic distortion by about 2 to 1. A separate oscillator power supply (pin 4) permits the sound system to be disabled while the a-m section is being aligned.

The modulator circuit has channel 3 and 4 band-switching, video synchronous tip clamping, and audio biasing to reduce distortion further. The value of $R_6$ permits the intercarrier amplitude to be adjusted easily with the minimum of rf oscillator coupling to pin 1. With a 12-V regulated power supply, there is less than ±10-kHz shift of rf carrier frequency from 0° to 50°C for any video input level. □

# OTA multiplier converts to two-quadrant divider

by Henrique S. Malvar
*Department of Electrical Engineering, University of Brazilia, Brazil*

An inexpensive two-quadrant divider that is useful in tunable and tracking filters and special-purpose modulators and demodulators may be built using an operational transconductance amplifier (see figure). This circuit is based upon a multiplier circuit by W. G. Jung[1].

The desired circuit response is achieved by placing the CA3080 multiplier within the feedback loop of the 308 comparator. This method implements the divider function more easily than—and just as accurately as—the logarithmic and antilog converters often employed.

The transfer function of the circuit is given by:

$$V_{out}/V_{in} = -(1+k)/kR_2g_m = -[2(1+k)V_T/kR_2I_B]$$

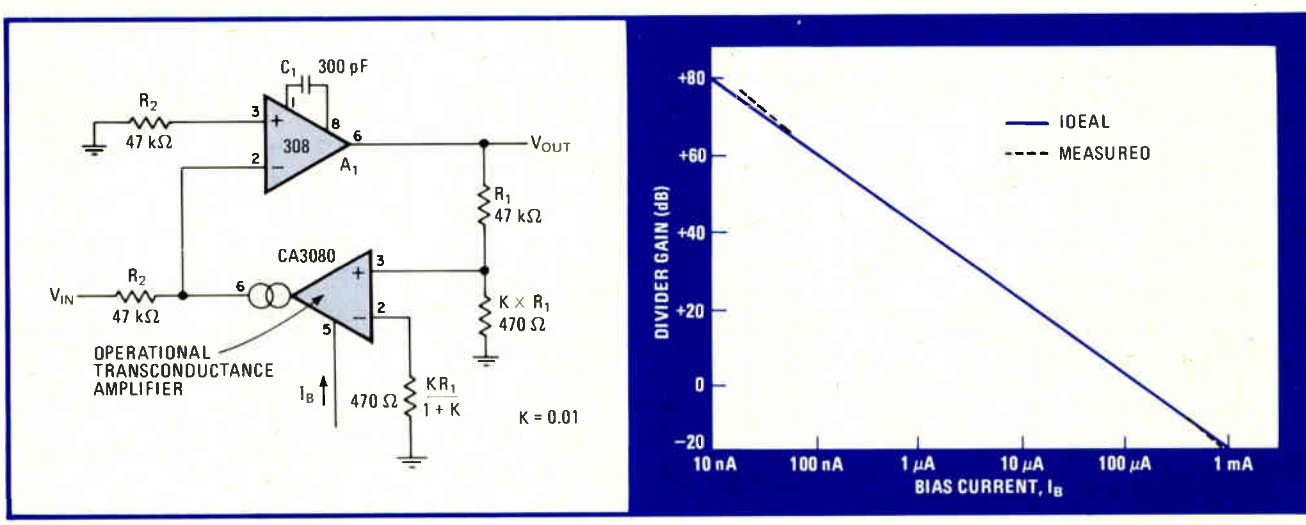
where k = the resistance scaling ratio and $g_m = I_B/2V_T$ for the CA3080. $V_T$ is the thermal voltage (26 millivolts at 23°C). The divider gain is thus inversely proportional to the input bias current, $I_B$. The plot in the figure shows the divider's nearly ideal response. Gain measurements were made with a selective voltmeter having a bandwidth of 10 hertz (HP 3581C) to eliminate noise effects—the circuit's linearity extends over five decades.

The offset of the 308 is also amplified as the circuit's bias current is reduced. Thus, $I_B$'s lower limit should be around 20 nanoamperes. Also, the compensating capacitor must be at least equal to $A_{max} \times 30$ picofarads, where $A_{max}$ is the maximum attenuation given by the divider circuit. The circuit uses a 300-pF capacitor because the maxiumum attenuation is 20 decibels.

The circuit's response to temperature variations is minimal, but in critical applications compensation is necessary for $V_T$. A temperature-compensating resistor having a thermal coefficient of 0.33% per °C for the resistor value $kR_1$ is used in this instance. □

**References**
1. W. G. Jung, "Get gain control of 80 to 100 dB," Electronic Design, June 21, 1974, pp. 94–99.






**Inverse.** A basic two-chip multiplier is easily transformed into a two-quadrant divider by the appropriate feedback. This scheme is simplier, no less accurate, and less costly than those using log and antilog converters. Circuit linearity extends to five decades of control current, $I_B$. Except for the most critical applications, temperature compensation is not required.

# TEST TACTICS FOR THE 1980s

**The beginning of a series, the following two articles draw from the experiences of high-technology firms to define how and when testing should be done**

Testing has played second fiddle to design in the past, when the emphasis was placed on putting together a product with the right features and functions in the most ingenious way. But the times are changing.

Electronics companies are realizing that a major part of their assets and their personnel are actually tied up in testing those great new products. In addition, they are finding that more money and labor may have to be invested if they want their products to have the reliability demanded by today's marketplace.

At the same time, there is a paucity of information about how to test in the most effective manner. The curriculums of most engineering schools still emphasize electronic theory and design practice. Laboratory courses do provide some exposure to instrumentation, but they do not tackle the theory of test approaches in a practical environment. So industry can only turn to a few specialists for the help it needs.

The purpose of the series of articles beginning in this issue is to provide a forum for the exchange of practical testing knowledge gained through actual experience. The articles that make up this continuing forum are based on problems encountered in a day-to-day engineering environment and the well-thought-out solutions to those problems. Although each instance may not be directly applicable to a reader's own problems, the process by which those problems were solved will serve as a model that can be adapted to a wide variety of real situations.

The first of the two articles that begin the series gives an overview from Logical Solutions Inc. of the entire process of developing test strategies. Noting the fact that testing is now becoming a major cost in most companies, the authors develop the philosophy of testing earlier and more easily to deal with that problem.

The second article is an excellent example of just that approach, but at a level of detail that will be the hallmark of this series. Designers at Texas Instruments Inc. explain how they were able to achieve fully functioning first silicon in their high-speed 99000 16-bit microprocessor—a feat never before accomplished with a processor and seldom if ever accomplished in general product design. TI's combination of hardware and software testing—employing both the latest computer-aided design tools and well-established breadboarding techniques carried to a new height of sophistication—was key to that success. It was a case of testing early enough to prevent foulups that would have been costly and time-consuming for their customers to correct.

Future articles in the series will deal with test strategies for all levels of support, from the early stages of product design through the production cycle and out into the field. **-Richard W. Comerford**

# Comprehensive test strategies help cut costs of manufacturing

In today's world of complex electronic products, a test plan must cover all contingencies to save money

by Jon Turino and H. Frank Binnendyk
*Logical Solutions Inc., Campbell, Calif.*

☐ The mushrooming costs of product testing are creating a new imperative: the development of test strategies that will minimize expenditures on the production line while keeping the failure rate at an acceptable level. Traditionally, product testing has been just that: a check of the product as it comes off the assembly line. But today's complex electronic products are expensive to test, and failure rates can be high.

For companies that intend to achieve significant cost savings and production improvements, the new watchwords are "test earlier and easier." Studies have proven that the earlier a fault is removed from an item, the easier (and cheaper) the fix is. In addition, testing at the component, not the system, level costs less in terms of equipment requirements and software development.

However, as will become clear, testing only components is hardly a comprehensive test strategy. To keep failure rates down and remove faults economically, testing must be continual throughout the manufacturing process. Examples drawn from actual case histories will show the importance of a comprehensive strategy.

## Many opportunities

As Fig. 1 shows, the manufacturing process is studded with opportunities to implement test steps. The proper test strategy—which steps to implement and what equipment and procedures to use—stems from examination of the total product cycle, from concept through design and manufacture to service. The decision on each test step should take into account the effect on it of previous steps in the cycle and its impact on succeeding steps.

Important considerations in developing a test strategy include product reliability goals, end use of the product, and how it will be serviced. The failure mechanisms (experienced or estimated) at each stage in the entire process must be determined, as must the availability of test facilities and equipment. Important, too, are the quantities to be tested and the skill levels required of the testers: in all, the list of factors to be considered should be quite comprehensive.

The common denominator in any test strategy is cost. The objective is to produce the maximum number of good products at the minimum testing cost. Other factors may affect the strategy, but starting with the cost of each step and its effects on subsequent steps in the manufacturing cycle provides a sound comparison.

Although the main reason for the current focus on test strategies is the high cost of testing, the cost of not testing is equally important. For example, a production run using a total of 5,000 untested, unscreened integrated circuits could exhibit a typical failure rate of 2%, with total testing costs of $4,150 (see Table 1). On the other hand, the initial screening of these ICs might cost about 12¢ each, or $600. Thus loss of profits from failure to test early is $3,550.

All in all, component testing and associated steps like thermal cycling and burn-in cycles are not unavoidable nuisances, but rather opportunities to increase profits. For other examples of the importance of thorough testing, see "The long-term impact on costs," p. 82.

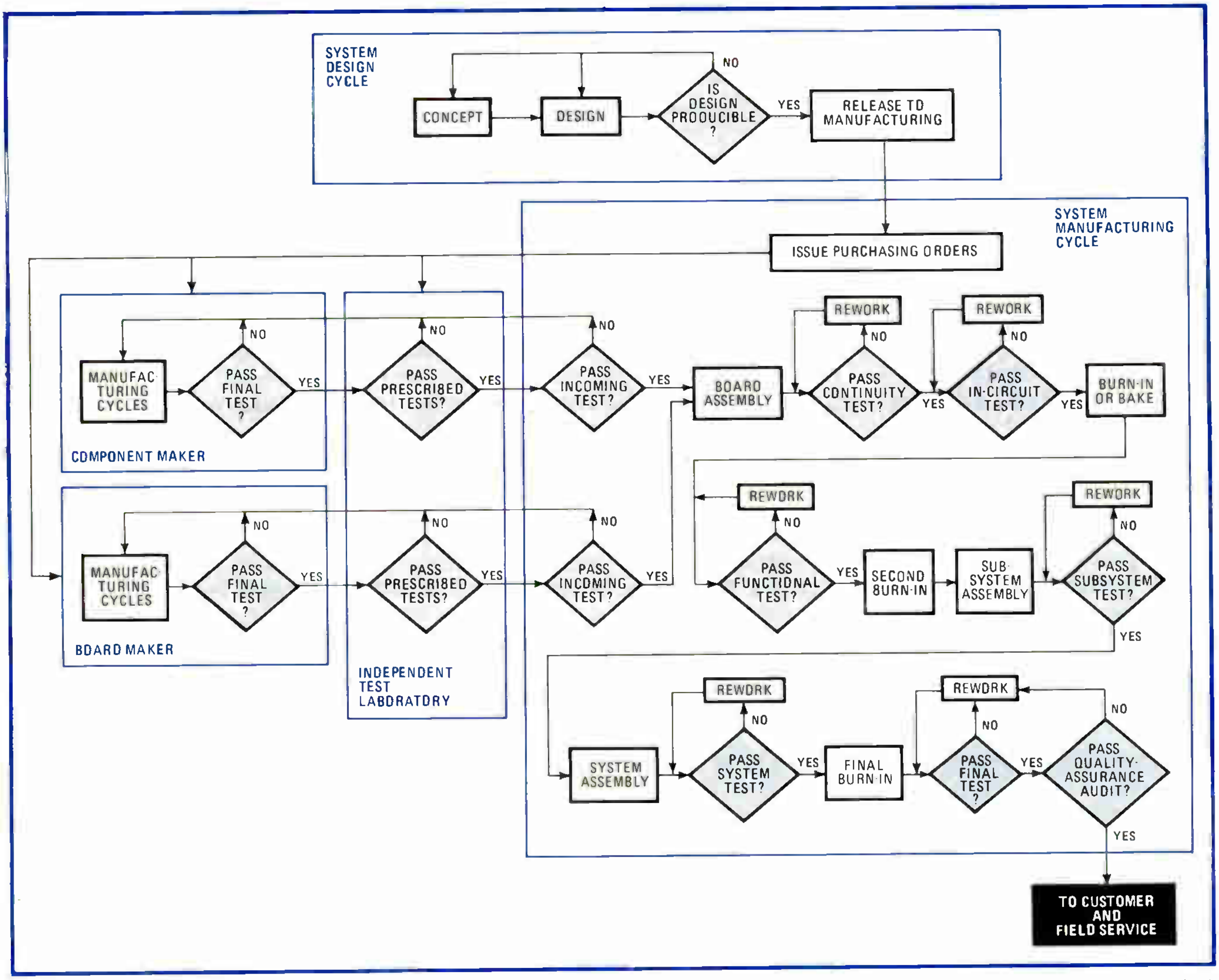
## A complex process

Procuring screened components seems like the most straightforward response to the "test earlier and easier" philosophy. However, such a strategy is not always easily realized. For example, company A, medium-sized with limited component-testing capabilities, decided to purchase 100% of its components requirement from already screened lots. But decisions made earlier during the design process complicated the move.

All too often, the design engineer selects components that meet or exceed application specifications without considering the test question. High-performance components may be selected even though they are not necessary, simply because of their specs—but often test programs are unavailable for these parts unless developed at the purchaser's expense.

In fact, most component manufacturers have testing programs for most of their standard parts. However, long lead times for screened parts sometimes clash with users' production schedules.

To screen untested parts—be they high-performance components for which no test programs exist or standard components purchased before they went through the manufacturer's test program—a user can turn to an independent testing laboratory. Such a move however, is not the end of company A's quest for a comprehensive test strategy, for the decision tree that is applicable to




**1. Opportunities.** Whereas testing was once quite simple, today's more complex products demand more complex test strategies. In a typical manufacturing cycle like that above, there are 13 separate areas in which testing related to the products may be performed.

this situation can contain many more branches (Fig. 2).

For example, an important point for company A to consider was whether to perform acceptable-quality-level (AQL) screens on incoming parts. Such sampling can keep the component manufacturers and test labs honest. What's more, if time constraints should shift and eliminate the option of any outside testing, the AQL sample size can be enlarged to 100%, thereby keeping catastrophic part failures from the assembly line.

Testing decisions at points in the manufacturing process beyond the acceptance of 100% screened components can be even more complicated. It is not just a matter of finding the right answers, but of making sure the right questions are asked. Some examples of real-life cases will illustrate this point, as well as highlighting some of the available test-strategy options.

Company B believed it had a field-service testing problem, for users were reporting what appeared to be many dead-on-arrival boards received from the company's four repair depots. The vice president of marketing sought a solution from the engineering manager, who recommended buying $1 million worth of automatic test systems for the repair depots. Faced with a $1 million solution, the company sought an outside opinion.

## The real story

Asking the right questions disclosed that the number of DOA boards actually amounted to less than 1% of the boards sent for repair. It happened that the marketing vice president had been the field-service manager, so he was getting 100% of the complaints.

Furthermore, the cycle time for board repair was three months. Also, because of inadequate field-test procedures, marginal boards could cause difficulty for the

**TABLE 1: COSTS OF USING UNTESTED PARTS**

| Test level | No. of failures | Unit cost | Repair cost |
|---|---|---|---|
| Printed-circuit board | 55 | $ 10 | $ 550 |
| Subsystem | 30 | $ 20 | $ 600 |
| Final product | 10 | $ 50 | $ 500 |
| Field failures | 5 | $ 500 | $ 2,500 |
| Total cost | | | $ 4,150 |

user more than once before they were finally repaired.

In this case, the correct strategy was to install one test system dedicated to board repair at a single facility, hire one technician to do the work, and revamp the transportation system. These moves cut the repair cycle time in half and pinpointed responsibility for DOA boards. Asking the right questions saved $750,000 in capital and improved the company's reputation for customer service.

In another actual case that illustrates the need for asking the right questions, company C was moving to select a test system for printed-circuit boards that combined medium- and large-scale integrated logic with microwave components. The impetus for this move was the high failure rate after product burn-in: about 30%.

## The long-term impact on costs

An excellent example of the impact a test strategy can have on a manufacturer's cost is in medical equipment, where the maker's liability in the event of product failure can be especially expensive. A pacemaker, say, may have the test costs shown in the table below.

Now, one liability suit resulting from a pacemaker failure could easily cost the manufacturer $10 million in legal fees, based on recent court history. As the table's statistics show, the maker will spend an extra $900,000 to drop the failure rate from 1 unit per thousand to 0.01 unit. This move slashes liability costs from $10 million per thousand pacemakers to $10,000, so the total cost of testing plus liability for a 0.1% failure rate is $10,100,000 versus $1,010,000 for a 0.001% failure rate. Clearly the extra $900,000 is well repaid.

Another slant on the impact of test strategy is the case of a telecommunications satellite. Repair in space is out of the question and is likely to remain so until the space shuttle becomes a reliable field-service vehicle. Therefore, thorough testing prior to launch is essential.

**PACEMAKER TESTING**

| Test factors | Failure-rate objective | |
|---|---|---|
| | 0.1% | 0.001% |
| Quantity per production lot | 1,000 | 1,000 |
| Test cost per product | $100 | $1,000 |
| Test cost per lot | $100,000 | $1,000,000 |
| Field failures per lot | 1 | 0.01 |

The existing test strategy involved dedicated systems with one pc board removed, that empty slot being used for testing the boards coming off the production line. Company C's managers decided this board-testing approach was inadequate because when boards failed, there was no simple way to determine the cause.

However, they soon hit a roadblock. An extensive survey of available equipment disclosed that none of it would fill the company's needs. The managers then considered the option of building their own, but the amount of high-priced labor and hardware it would take to develop the necessary system gave them pause.

A thorough review of the problem uncovered the fact that almost all the products worked before the burn-in test, which seemed to vindicate the company's board-test strategy. It turned out that the 30% failure rate after burn-in was due to defective components, not to the board design or to faulty assembly, both of which a tester would have checked.

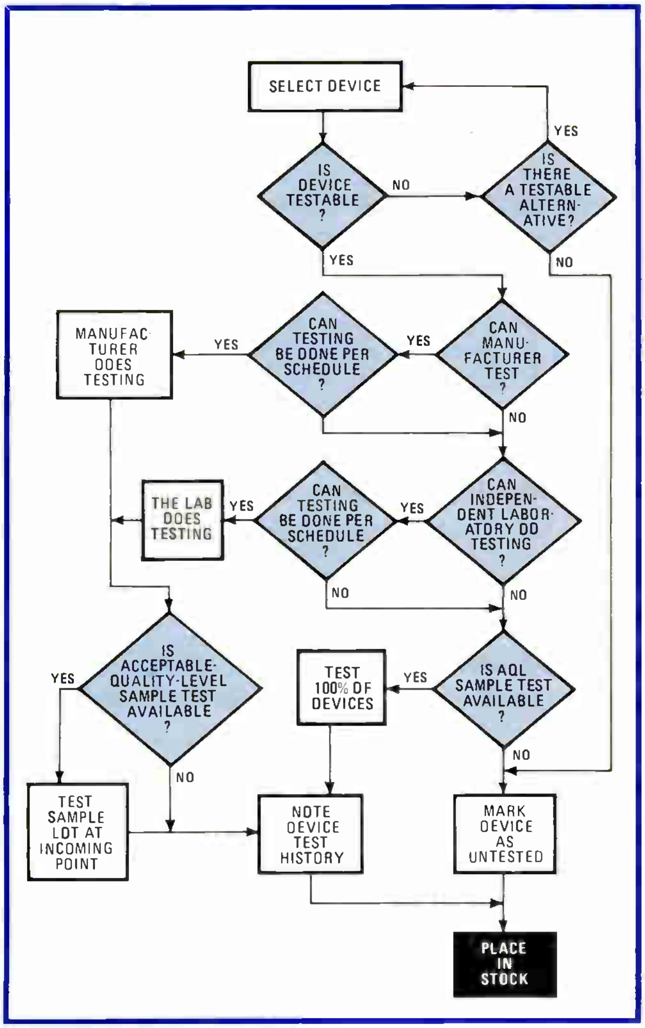
Examination of a year's worth of failure data disclosed that 90% of the failures could be attributed to only eight components. Therefore company C implemented a burn-in test program for these parts prior to assembling them on the pc boards. The cost for this extra testing step was minimal, especially since only a few components were involved. The board failure rate after burn-in testing went from 30% to 5%, resulting in a savings of two orders of magnitude over the investment in the extra component-test step.

### In the beginning

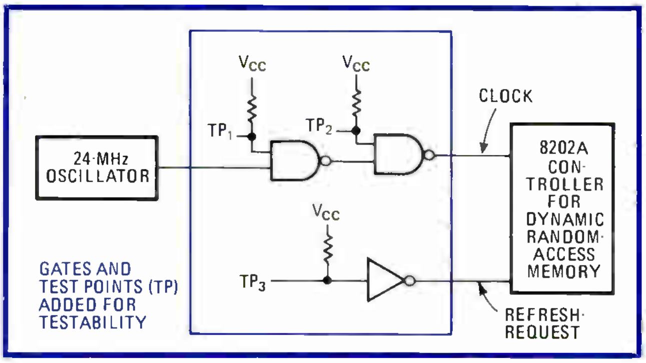
Designing for testability is fast becoming a byword with original-equipment manufacturers that use LSI components. It also contributes to the formulation of a comprehensive test strategy, as the following dilemma will illustrate.

Company D was developing a memory board containing 128-K bytes of dynamic random-access memory, controlled by a pair of 8202A dynamic-RAM controllers. By looking at the schematic of the assembly, the test engineering department determined that the design would be untestable: its free-running oscillator allowed no way to synchronize the unit under test with the company's automatic test equipment, and there was no external control over the refresh capabilities of the 8202A controllers. The 24-megahertz oscillator drove the 8202As at frequencies far beyond the capabilities of the 5-MHz automatic testing equipment.

The lack of control over the 8202As' refresh capabilities stems from this chip's ability both to generate refresh cycles of the RAMs and to handle external refresh requests. The controllers could delay an external request if it were made during a command cycle, such as fetch, where it is intended for the refresh cycle to follow, or they could ignore it altogether if the internal refresh had just been triggered.




**2. Between source and stock.** Choosing the right part is not simply a matter of evaluating its specifications, as this flow chart illustrates. If the only option is to use an untestable part, proper marking will at least indicate that there may be problems on the manufacturing line.




**3. Testability logic.** Without the addition of the two NOR gates and the refresh-request test-point amplifier, a board tester would not be able to gain control over the 8202A controllers on a RAM board. Thus, finding a fault in an economical way would be impossible.

Thus the 8202As posed a complicated testing problem: designing a program that would take into account the controllers' operating modes while performing diagnostic routines on them. However, it was not the selection of this complex chip and the free-running oscillator that promised testing havoc for company D; rather it was the failure of the designer to take testability into account.

## Design fix

In fact, it took a few simple design changes (Fig. 3) to solve the test problems. Two unused NAND gates on the board were reconfigured to allow disabling the free-running oscillator and insertion of a signal supplied by the ATE. Then it was necessary only to break a 13-level feedback loop and to provide a controllable input signal to the 8202A's external-refresh-request line.

| TABLE 2: TEST-STRATEGY DOCUMENTATION LIST |
|---|
| Test-plan assumptions |
| Product quantity data |
| Task estimates for each element |
| Technical tradeoffs |
| Economic analyses and tradeoffs |
| Product-testing strategy |
| Manufacturing test flow |
| Manpower loading |
| Detailed task schedules |
| Test specifications |

As these case histories illustrate, development of a comprehensive testing strategy must involve many considerations. Furthermore, the number and types of these factors will no doubt vary considerably from company to company. Unfortunately there is little formal training on test engineering, and it usually fails to emphasize the development of a logical testing strategy that takes into account the individual requirements of each situation.

It is important to do an orderly development of the test plan, but it is equally important as well to document it in a formal test plan. At the very least, this plan should contain the information listed in Table 2.

The test plan should be a living document; that is, it should be updated as new data is available and as new lessons are learned throughout the total life cycle of the product. Also, it should be refined through a constant feedback process. The importance of data gained in this way cannot be understated, for without good data, good planning is categorically impossible.

As well as being based on good data, test strategies must be drawn with an eye toward the dynamics of the business cycle. This stricture means that test-engineering professionals must widen their horizons to include knowledge of economics, planning, standardization, and design for testing. □

# Test strategy enhances, speeds the development of a microprocessor

A part that met its design goals on first pass owes its success to a well-thought-out test plan designed to cover all bases

by Karl Guttag, Robert Puckett, Stephen Sacarisen, and Thomas Dye, *Texas Instruments Inc., Houston, Texas*

☐ Testing is an inherent part of the development of any new product, but it can be especially important during the development of a new microprocessor. By working out a careful test strategy in concert with the chip design, the task force that produced the 99000 16-bit microprocessor hit its design goals on the first pass.

With special checking done even before first silicon was obtained, the initial parts were fully operational, besides being in full compliance with the design goals. Such an achievement is not fortuitous; it came about because the design team devised a test regimen that covered both key areas of functional uncertainty.

The first of these areas was compatibility with Texas Instruments' existing offerings. The design goal was a high-performance machine—operating at an internal frequency of 6 megahertz—that would be fully compatible with its predecessors, the 9900 and 9995, and with the 990/10 minicomputer. The new part is not simply a scaled-down version, so its compatibility could not be checked simply by comparing it with its predecessors.

The 99000 adds several important on-chip features to TI's 16-bit microcomputer architecture, and these needed thorough checking out. Among them is the capability to perform signed multiplication and division, as well as more complex 32-bit arithmetic. The complexity of these operations posed difficult test problems.

The new part adds a macrostore feature, in which a high-speed internal read-only memory interprets external instructions as macros. This feature also demanded an innovative testing strategy.

The processor was designed to operate with memory inputs every 166 nanoseconds, so allowance had to be made for times when data could not be supplied at that rate. Thus the unit was designed so that it could be

## Alternative strategies considered

In deciding which testing path to take in the development of the 99000, several of the methodologies receiving widespread attention today were considered. For one, serious thought was given to adding extra hardware for better testability.

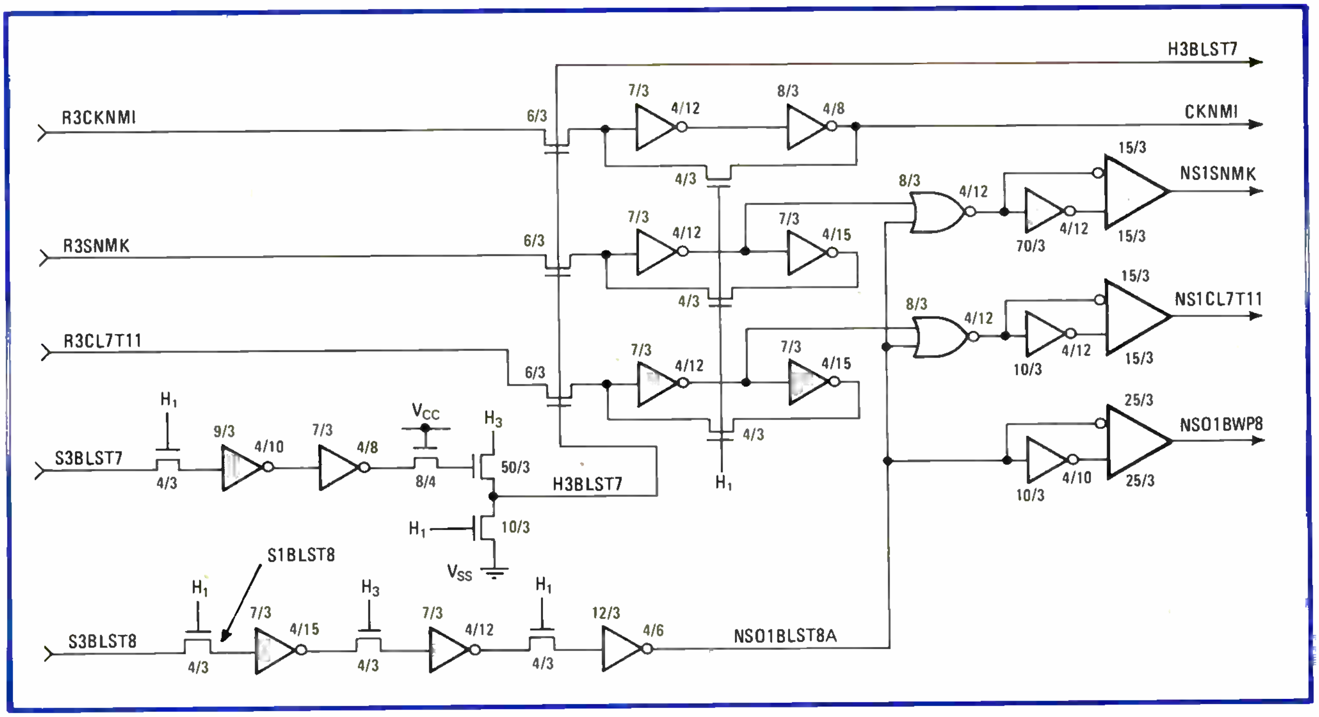
For example, the use of additional circuitry to allow microcode to be driven into the chip from an external source was contemplated. In the earlier stages of debugging this would have permitted microcode to be debugged, even though large sections of the hardware were not operating. In addition, this feature might have come in handy in later stages of testing, because it would have permitted microcode to be tested independently instead of as part of the overall chip's functionality.

With the 99000, there were several reasons why the approach was avoided. For one, the new microcomputer can load and read back all its internal registers speedily, with very few instructions required for the task. Thus the extra hardware would not have improved test time significantly in the later stages of testing. Further, this debugging mode would not have been a natural, native mode of operation, so certain unusual, hardware-related conditions could go undetected during testing.

There were other considerations that helped rule out extra hardware. One was that the 99000's workspace-pointer architecture is highly visible from a user's standpoint and operates at high speed, so it would be easy and quick to test. Another was the task force's belief that the design effort should be directed toward ensuring the circuitry would work correctly and reliably, rather than working from a "design-for-failure" philosophy.

Another testing possibility was a functional computer model to simulate the new microcomputer's operation on a mainframe computer, a technique used previously at Texas Instruments. If a model could run the same software and produce the same results as did the 9900 and the 9995, then it would have achieved compatibility.

For the 99000, however, there were considerable drawbacks to using a functional model. One was that it would have taken a large amount of mainframe time just to functionally simulate one 99000 cycle. Thus it would have been far too expensive and time-consuming to use a functional model to verify compatibility. Furthermore, such a model would not have given the level of detail needed to determine how the MOS circuitry of the new chip would behave logically—information the designers required to check the operations of each segment of the procesor before it was actually built.




**1. Layout.** The logic diagram for a typical 99000 cell includes the major signal paths, such as R3CKNMI, and secondary paths of interest, such as NSD1BLST8A, clearly marked. The drawing also contains device length and width dimensions—for example, 4/10—in micrometers.

placed in a wait state, and this characteristic also created special testing needs to be met.

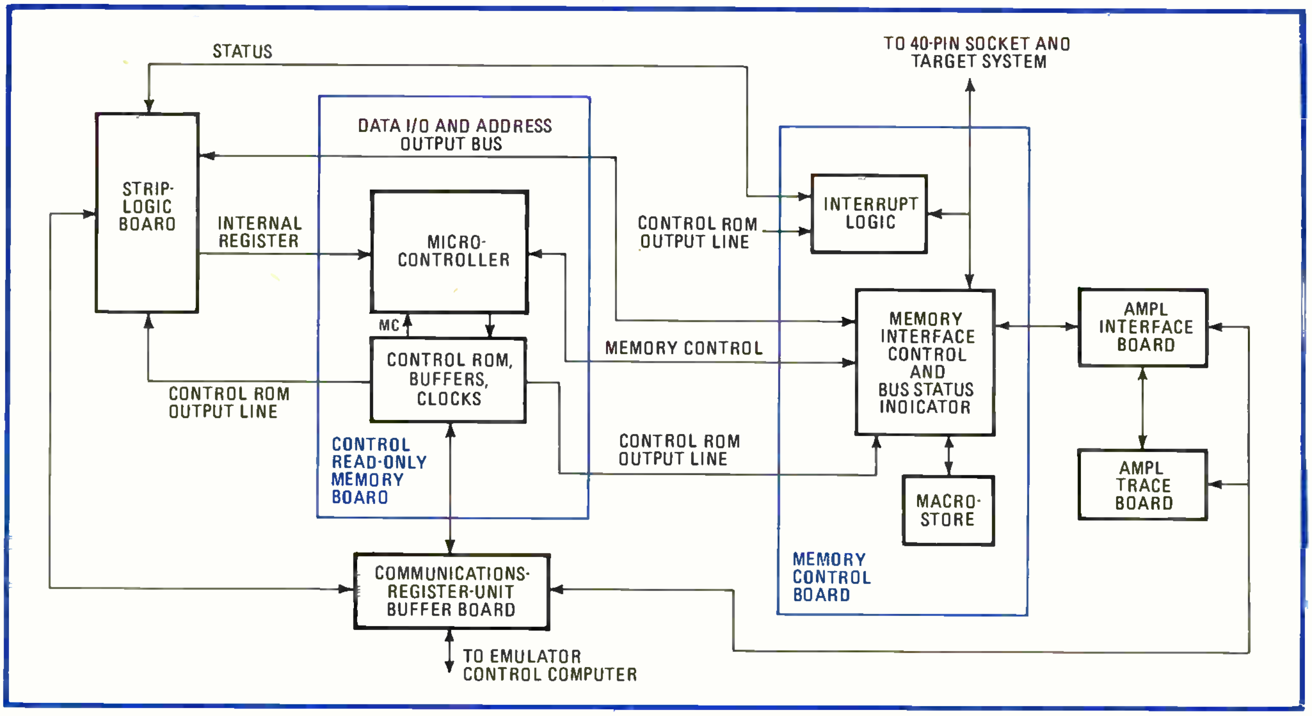
A major question, of course, was which testing approach to take, and an early review of the options eliminated two popular development methodologies, on-chip test circuitry and a functional computer model (see "Alternative strategies considered," opposite). Instead the design team developed a two-pronged path for verification and testing.

The testing strategy for the 99000 was to use both a logic simulator and a breadboard emulator. This dual approach combines some of the latest computer-aided design techniques with hardware methods having a proven history in design evaluation and testing.

The first part of this approach, then, was to use a logic-level simulator to verify that each circuit would perform in the correct logical manner. In functional models, a classic problem is that the transistor is modeled as a simple device with a single direction of flow—but in many cases

```
BLOCK ISCON:
   (S3BLST7, R3CL7T11, R3SNMK, R3CKNMI)                        @INOUT;
   (S4RTINT2, S3BLST8)                                         @INOUT;
   (NS01BWP8, CLRINT, NS1SNMK, NS1CL711,
   CKNMI, S01BLST8)                                            @INOUT;
 STRUCTURE
   ISCON01 : BTR_INV  S3BLST7, H1, ISCONS1, 4, 3, 9, 3, 4, 10;        (*0*)
   ISCON02 : INV      ISCONS1, ISCONS2, 7, 3, 4, 8;                   (*0*)
   ISCON03 : E_GCLK   ISCONS2, H1, H3, H3BLST7, 8, 4, 10, 3, 50, 3;
   ISCON04 : BTR_INV  S3BLST8, H1, ISCONS4, 4, 3, 7, 3, 4, 15 ;
   ISCON05 : BTR_INV  ISCONS4, H3, ISCONS5, 4, 3, 7, 3, 4, 12;
   ISCON06 : BTR_INV  ISCONS5, H1, NS01BW8A, 4, 3, 12, 3, 4, 6;
   ISCON08 : NOR2     NLCL7T11, NS01BW8A, S1CL711A,
                      12, 3, 12, 3, 4, 12;
   ISCON09 : N_FPSPL  S1CL711A, NS1CL711, ISCONS9, 10, 3, 4, 12, 15, 3, 15, 3;
   ISCON010: NOR2     NLSNMK, NS01BW8A, S1SNMKA, 8, 3, 8, 3, 4, 12;
   ISCON011: N_FPSPL  S1SNMKA, NS1SNMK, ISCONS11, 10, 3, 4, 12, 15, 3, 15, 3;
   ISCON012: INV      NS01BW8A, S01BLST8, 12, 3, 4, 6;
   ISCON013: N_FPSPL  S01BLST8, NS01BWP8, ISCONS13,
                      10, 3, 4, 10, 25, 3, 25, 3;
   ISCON016: BTR      R3CKNMI, H3BLST7, ISCONS16, 6, 3;
   ISCON017: BTR      R3SNMK, H3BLST7, ISCONS17, 6, 3 ;
   ISCON018: BTR      R3CL7T11, H3BLST7, ISCONS18, 6, 3;
   ISCONC19: REGC     ISCONS16, H1, CKNMI, ISCONS19,
                      4, 3, 8, 3, 4, 12, 8, 3, 4, 8 ;                 (*0*)
   ISCONC20: REGC     ISCONS17, H1, ISCONS20, NLSNMK,
                      4, 3, 7, 3, 4, 12, 7, 3, 4, 15 ;
   ISCONC21: REGC     ISCONS18, H1, ISCONS21, NLCL7T11,
                      4, 3, 7, 3, 4, 12, 7, 3, 4, 15 ;
 END ISCON ;
```

**2. Model.** In the computer model for simulating the cell shown in Fig. 1, a structure is given a name (such as ISCOND1) and defined functionally; its input signals (S3BLST7, $H_1$), the structure's output, and related dimensions (used for schematic verification) are given.




**3. Breadboard.** All the functions of the new 99000 microprocessor are modeled in this TTL emulator. The interface and trace boards from TI's AMPL development system give the designers the means to follow in great detail the operation of the 990/10-controlled emulator.

it is actually a bidirectional switch; both the charge and logic flow can be in either direction through a transistor. In ESIM (for electrical simulator), the logic-level simulator developed by TI's design-automation department, this factor is taken into account.

ESIM takes off from the MOS logic drawings for each circuit—a typical drawing, for the interrupt-state control is shown in Fig. 1. From this drawing, the logic-level model in Fig. 2 was created.

### Careful tracking

It should be noted that the nomenclature in the model tracks that of the logic diagram; each time a logic drawing was changed for any reason the logic model was also changed. This tactic ensured that no errors could creep into the final design because of improper simulation. After a model change, a simulation was run to ensure that no other part of the processor was affected.

Although the logic-level simulator was excellent for many purposes—it did, for example, simulate the 99000's complex arithmetic and logic unit with an extremely high degree of accuracy—it had a drawback similar to that of a functional model. It would require minutes of mainframe time to simulate a full 166-ns cycle of the entire processor.

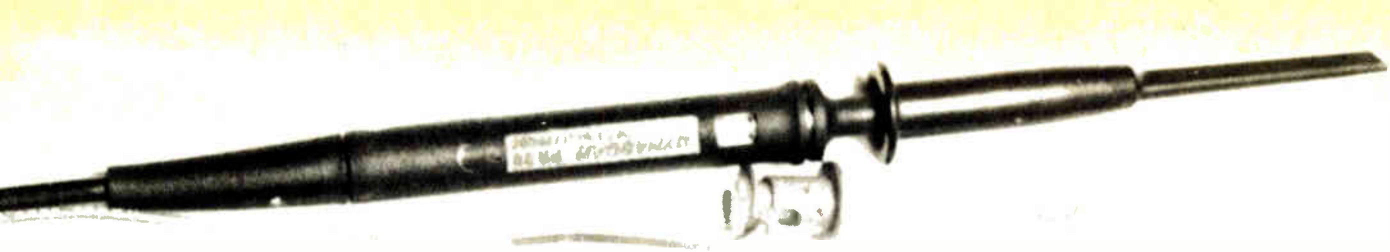
Thus it was decided that, for major testing of the 99000 design, a full-scale hardware emulator (Fig. 3) would be built using TTL parts to provide the speed that the final MOS processor would have. This hardware was not as flexible nor as easy to change as a computer model, but it did provide a speed advantage.

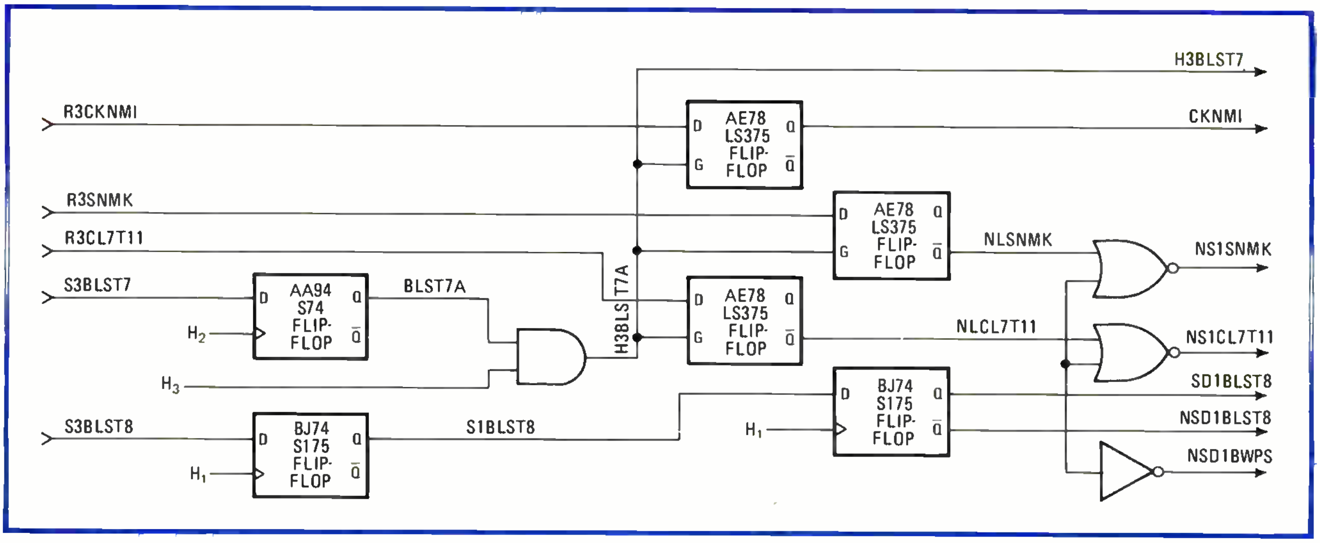
The logic-level simulator was first used to gain assurance that the circuits would work properly, then the hardware model was built to run verification tests. If a logic drawing was changed, the hardware emulator, like the simulator, was updated to conform to the change. Tight control and the use of feedback was a must to ensure design integrity.

To some, the use of a breadboard might sound like a standard practice, and to a degree it is. However, most breadboards (and simulators, for that matter) are only functional models, and the modeling is at a fairly high level; that is, only the major functions and signals are modeled. The TTL emulator is a much more detailed model than other breadboards, in that it modeled practically all the internal timing characteristics of the 99000, not just the major signals.

Comparing Fig. 4, the TTL emulation for the interrupt-state–control function, with Fig. 1 demonstrates the detailed level of this modeling. To model the entire processor, over 900 small-, medium-, and large-scale integrated packages were used, about four times the number ordinarily used in a functional breadboard.

Going to this level of detail allowed the actual processor to be checked out to the internal nodes, which would correspond to those in the final processor. It also permitted the 99000 to be checked out in an actual operating environment (Fig. 5).






**4. In TTL.** In the TTL version of the cell shown in Fig. 1, the electrical timing follows that of the final MOS circuit of the microprocessor. Also, this version brings out signals from internal nodes, such as SD1BLST8 and NSD1BLST8, which are critical to the cell's correct operation.

The emulator was plugged into a host computer, using a dual-in-line connector, to produce the functional equivalent of a 990/10 minicomputer. With this tactic, the software equivalent of 40 boxcars of Hollerith cards could be be used to check the 99000 design in a real operating environment. The software used to debug and verify the 990/10, as well as other Pascal, Fortran, and Cobol applications programs, was run.

## Leveraging software

When the first 99000 was produced, the emulator was unplugged, the actual processor put in its place, and the same software used again to verify compatibility. The unit ran this software without a hitch, and thus the software work done for the 990/10 was successfully leveraged for the 99000.

Before the first units were produced, the loop between the simulator and the emulator was closed by using the simulator-generated test software to check the emulator, which was plugged into the test system that would be used in actual production testing, and it successfully passed all tests. Additionally, this procedure allowed the tester's control software to be debugged even before the first units started rolling down the line. Thus, from the start of production, time was spent verifying the 99000 rather than debugging the tester.

The software used to debug a simulator has to be as efficient as possible in order to minimize the cost of running each simulation. It is too costly to verify a simulation with an exhaustive set of test vectors because of the run time involved and the manpower needed to check this results. Thus the vectors used to test the simulator have to be judiciously chosen.

For the 99000, the effort of choosing these vectors was greatly simplified, since it had already been done for those instructions common to it and the 9900 and the 9995. Further, using the same procedures to verify the software models and the hardware ensures that the two methods are compatible.

As previously noted, the 99000 has a number of more complex instructions than the units with which it had to be compatible. These features, such as the signed multiplication and division, entailed many more boundary conditions, which had to be checked.

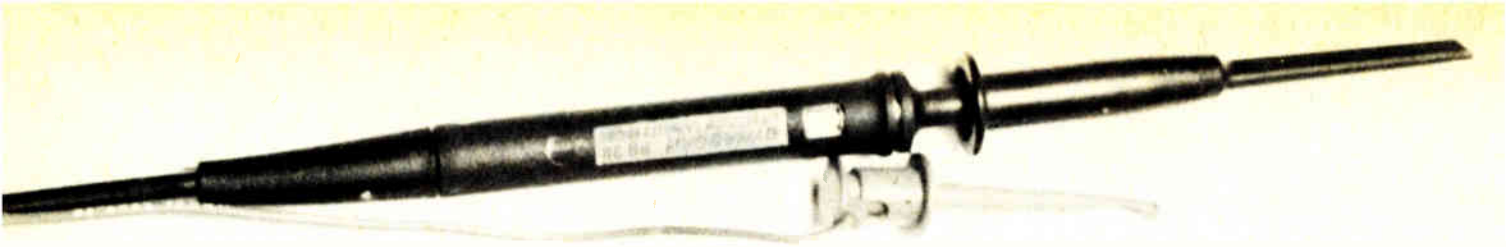
For instance, with an unsigned multiplication, the boundaries of the test are multiplying by two very large numbers, by two very small numbers, and by zero. With a signed multiplication, the boundaries and thus the number of test cases increase. For example, $8000_{16}$ is a negative number for which no positive equivalent exists, and thus it adds new test cases to the overall test plan. The same is true for, say, a 32-bit add, and in general the number of test cases tends to increase exponentially as instructions are added to the processor design.

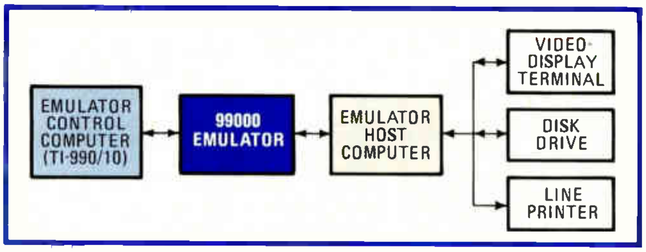
## Saving test time

As well as generating and running the test cases peculiar to the 99000, the design team had to run and check all tests used with the 9900 and 9995. The rise in the number of cases seemed to indicate that testing and test-generation times might become staggeringly long.

Fortunately, the internal architecture of the 99000 provides a great advantage in test development. It needs many fewer clock cycles than the 9900 to execute a given instruction, and the number of clock cycles needed tends to be proportional to the complexity of testing.

For example, the 9900 takes 14 clock cycles to perform a register-to-register move. This characteristic meant verifying 14 sets of output line conditions. This verification used the software model to generate the






**5. Test bed.** By plugging the emulator into a host computer, the 99000 could be checked out in a real multitasking environment. The emulator was also plugged into a tester so that tester software could be debugged even before first silicon was obtained.

output, with the output checked by hand. In contrast, the 99000 takes only three cycles to perform a register-to-register move, so a verification required less run time and less hand checking. Also, because computer models existed for all three processors, a computer could compare the results of some test-program runs.

The reduced number of clock cycles was more than a benefit in generating tests: tied to the 99000's fast operation, it turned out to enhance the testing of the final parts. The combination of characteristics meant that seven tests could be run in the same time that it took to run one on the 9900. Thus the 99000 could actually be checked more thoroughly than the 9900.

In reviewing the testability of the new chip, the design team found that its new macrostore feature presented a particularly thorny problem. In a macrostore, very complex routines such as floating-point multiplication are stored so a user can call the operation from outside the chip with a single instruction. Such routines could take thousands, if not tens of thousands, of clock cycles to execute. Thus testing and generating tests for the macrostore in the same manner as for other instructions would have been impossible.

It was decided that the only way in which a reasonable verification of the macrostore could be performed was by ROM dumping—reading all the code in the macrostore ROM and checking to see that it agreed with the code originally specified. There were two possible ways this could be done: by using special hardware to perform a transfer akin to a direct-memory access to the output data lines, or by providing an instruction that let the 99000's control processing unit read out the contents of the macrostore.

### Instruction route

Although a DMA transfer would speed up testing by as much as four times, it could present problems that would be very difficult to uncover. This kind of problem cannot occur if the ROM were read by the internal CPU, the same manner in which it would be read in actual operation. At the same time, all the control lines and data paths that would be used in a typical macrostore operation are exercised, thus ensuring these work properly. Then, too, this method was in keeping with the philosophy of concentrating on correct circuit design rather than adding more hardware.

In addition, it was decided that the design would be modified to permit execution of macrostore instructions from an external memory. This decision separated macrostore software from hardware debugging, and it gave users the opportunity to develop their own macrostore routines, which could then be put into the macrostore ROM when parts are ordered. In the final testing of such semicustom ROMs, dumping would permit the custom program to be checked against the user's specification.

The TTL emulator also provided the means to check the 99000's wait-state operations quickly. The processor can go into a wait state under two conditions: when it requires information from a memory system that is not ready to supply that information, or when it is told to prepare for a DMA transfer.

Since the 99000 is designed to process memory data every 166 ns, all data from a current operation has to be saved when it is placed in a wait state. The part must be checked to see that it does this correctly.

Using the logic-level model to check this facility would have proved extremely time-consuming and costly. Instead, the TTL simulator running in real time was bombarded with wait states, and any conditions to which the device might be sensitive were found. A representative subset of these conditions could then be verified, using the logic-level simulator and appropriate test programs generated to check production parts. □

## A thorough final check

Most integrated circuits are now checked using a computer to verify that certain types of simple design rules have not been violated. For instance, a typical design-verification program would check to see that metalization lines are not so narrow that they would break and that they are not too close to create short circuits.

For the 99000, a more thorough preproduction design-verification program, called SVER for schematic verification, was used. SVER takes as input the computerized version of the logic layout from which the mask is made, the logic model, and the device design rules for the part. It checks for the characteristics usually verified, as well as evaluating the actual interconnections to be sure that the logic is correct and the device sizes to make sure that they are in tolerance.

For the 99000, SVER identified five interconnection errors that most likely would have caused some level of nonfunctionality. It also located 212 deviations in device sizes. These deviations would probably not have caused a malfunction *per se*, but they would have resulted in degraded performance or yield loss. By using SVER, TI was able to produce parts that worked to the design specifications on the very first run.

# Electrochromic displays prepare to hoist their colors

Given long-lasting materials and matrix addressability, these attractive devices should have broad consumer appeal

by J. P. Randin, *Asulab SA, Neuchâtel, Switzerland*

☐ Sheer good looks could start winning electrochromic displays a sizable market in as little as two years' time. With their ink-on-paper contrast and wide viewing angle, they are a strong candidate for applications in which appearance counts heavily—in watches, clocks, telephones, arrival and departure displays, or radio and television channel indicators, for instance (Fig. 1).

Low power and voltage requirements and the ability to store images also make them attractive for these purposes. But before they can enter full-scale industrial production, they do have problems to overcome in the areas of life time, response speed, and matrix addressing. Once these are solved, electrochromic displays should become viable competitors of electrophoretic, electroluminescent and light-emitting-diode displays and especially of liquid-crystal displays.

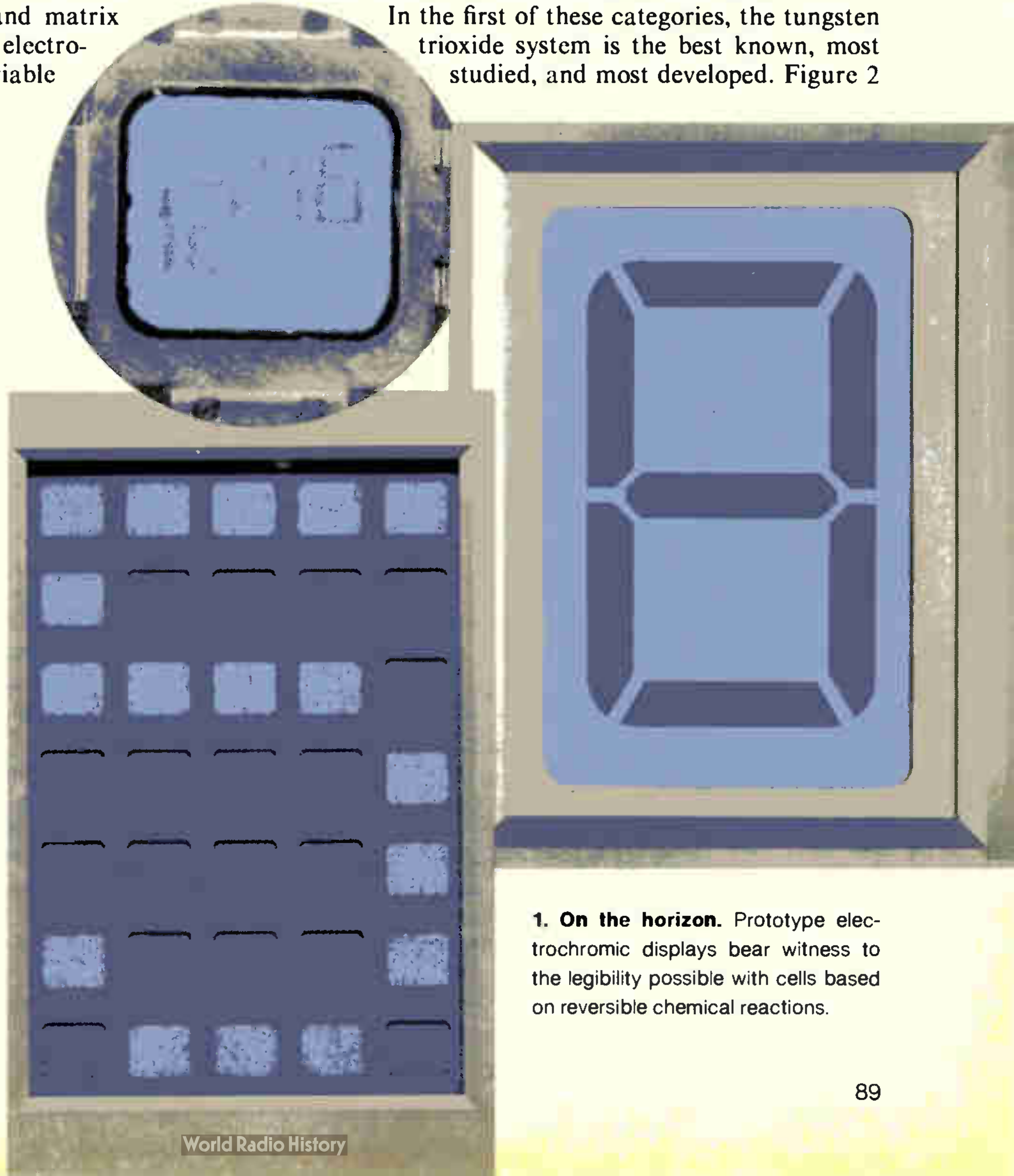
At present the devices have achieved roughly the same balance of pluses and minuses as LCDs had when they first went public about 10 years ago. So companies the world over are experimenting busily with ways to bring the technology up to commercial scratch.

Electrochromism may be broadly defined as a persistent but reversible color change induced in a material by an applied electric current. An electrochromic display is essentially a rechargeable battery in which one electrode changes color from one state of charge to the other. In principle, that electrode retains its color along with its charge, so that the device exhibits open-circuit memory. But in practice various side reactions produce a more or less rapid decay of the electrode's colored state.

Another problem is that the electrochromic display is not intrinsically matrix-addressable since it lacks both a well-defined threshold voltage and a short-circuit memory. Its main assets are excellent legibility and insensitivity of contrast to viewing angle. By way of comparison, a twisted-nematic LCD has a much dimmer background because it uses polarizers.

Reversible color changes can be induced in solids or liquids by a wide variety of physical phenomena. Three systems appear to be closest to practical display applications: injection of hydrogen or metal atoms into transition metal oxides; the reduction and oxidation of organic compounds such as viologens; and the deposition and dissolution of thin films of metals like silver.

In the first of these categories, the tungsten trioxide system is the best known, most studied, and most developed. Figure 2



**1. On the horizon.** Prototype electrochromic displays bear witness to the legibility possible with cells based on reversible chemical reactions.

presents it schematically. The electrochromic film is deposited on a transparent electrode. An electrolyte conducts ions between the electrochromic and counter electrodes and also blocks the flow of electrons. In most applications a pigment is added to the electrolyte to provide a strongly light-diffusing background.

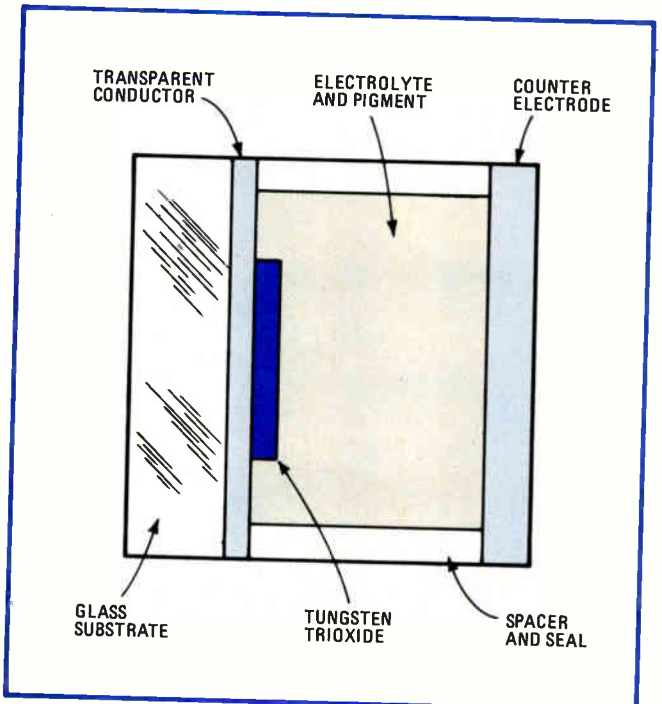
The counter electrode acts as a reservoir of atoms to be injected into the electrochromic material. The mobile cations—typically hydrogen or alkali ions—are what turn the host oxide a deep blue, though an electron accompanies every ion injected. The reaction is reversible: the ions are repeatedly injected and removed by controlling the potential between the oxide's electrode and the counter electrode.

The voltage required to drive a tungsten trioxide display is comparable with a galvanic cell voltage—about ±2 volts or less. The optical density of the colored state is proportional to the applied charge; energy consumed in writing a cell is typically 5 to 20 millijoules per square centimeter of the electrochromic film.

### Liquid or solid electrolytes?

The earliest tungsten trioxide displays used acid electrolytes mixed with organic compounds such as glycerin or glycol. American Cyanamid Co. of Stamford, Conn., led the way here. However, device lifetime suffered: the electrochromic film corroded at a rate of about 20 angstroms per day.

This chemical instability has been eliminated by using polymeric acid electrolytes—semisolids containing some water to keep their proton conduction high. The loss of water must be avoided by hermetically sealing the device. With such an electrolyte, researchers at American Cyanamid and Asulab SA of Switzerland report a lifetime of better than three years at room temperature. No failures occurred as a result of electrode erosion either in storage or after more than $10^7$ switching cycles at 0.5 hertz. The cells switch in less than 1 second and employ a signal of about 1 V.




**2. Blue in the face.** The most promising electrochromic display system is based on tungsten trioxide films that turn deep blue when injected with hydrogen or alkali metal ions. The operation of the cell is similar to the charging and discharging of a battery.

In Switzerland the same materials have been used at Ebauches SA and Asulab SA to construct a prototype watch display, a five-by-seven-dot matrix, and a single large digit (see Fig. 1 again). The response time at room temperature for the watch-size display was about 0.3 s, and its operating temperature ranged from −10° to +50°C. Its open-circuit memory lasts several days at room temperature, making devices of this kind attractive for displaying information that changes infrequently.

Several Japanese companies (Sharp, Seiko, Sanyo, Matsushita, and Toshiba) have announced the development of electrochromic displays using lithium salts dissolved in a nonaqueous solvent. These devices are somewhat slower than those based on purely protonic electrolytes and fail to erase completely after several months of cycling, but their tungsten trioxide film dissolves much less fast than in aqueous electrolytes.

Solid-state electrolytes theoretically offer the best answer to the stability problem and would also make packaging easier since hermetic sealing would become unnecessary. Truly solid-state devices using a sodium-alumina electrolyte have been investigated at London's Imperial College of Science and Technology. This water-free system is expected to have a long life, but it shows slow response and needs a relatively high voltage.

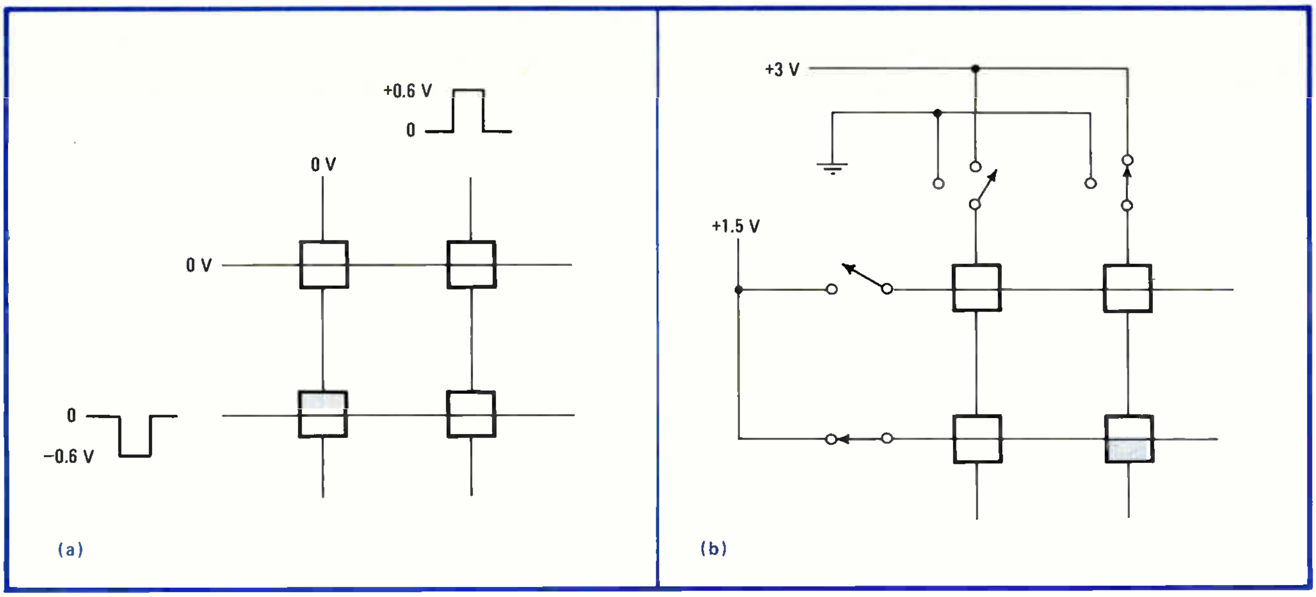
Iridium oxide film, grown either anodically or by sputtering, is another promising electrochromic material, according to scientists at Bell Laboratories in Murray Hill, N. J. Unlike tungsten trioxide, it is colored by anodic oxidation rather than cathodic reduction.

### Speedier switching

On the plus side, small iridium-oxide–based cells are capable of switching in 0.1 s in a variety of liquid electrolytes, their response time remains below about 0.25 s at temperatures higher than or equal to −10°C, and those using the more stable sputtered films seem not to have degraded at all after more than 10 million cycles. However, the material needs roughly four times as much injected charge as tungsten trioxide to produce the same optical density change in the visible spectrum.

Display devices using viologen (dipyridinium salts) have been known for about 10 years, but no commercial product based on it has ever been announced. The system employs electrochemical reduction and oxidation—the reaction product is deposited as a purple film on the electrode. The absorption maximum of the deposited film corresponds to the maximum sensitivity of the human eye, at about 550 nanometers. The electrical charge efficiency is therefore better than that of tungsten trioxide for which the maximum of the absorption band is located in the near infrared.

Unfortunately, some mechanism prevents the complete decoloration of the deposited viologen film, especially after it has been left in the colored state for a long time. The effect may be due either to the occurrence of a




**3. Inhibitions.** One of the chief drawbacks of electrochromics is its poorly defined turn-on threshold that leads to high crosstalk, as in (a). One solution is pictured in (b), where switches disconnect unselected cells, allowing them to retain charge and hence their color.

second and irreversible reduction step or to the recrystallization of the film, or both. This difficulty has so far rendered viologen-based systems unsuitable for long-life display applications.

## The electroplating plus

A system relying on the anomalous optical absorption in thin films of silver is being developed in France as a passive display device by Laboratoire d'Electronique et de Technologie de L'Informatique (LETI) in Grenoble in collaboration with an industrial firm in Paris, Jaeger SA [*Electronics*, Jan. 27, 1981, p. 82]. In this display, a silver film is electrodeposited from a nonaqueous solution of silver salt on a transparent conductive surface. A pulse of reverse polarity dissolves the silver film and thus erases the display.

The memory is limited by secondary reactions involving the iodide used as the anion of the silver salt. Although the speed of response is about twice that of the tungsten trioxide system, the charge efficiency is about a third. The degree of contrast depends on the current density and on the operating temperature, most probably because these parameters happen to influence the structure of the silver film.

If the driving circuit has to take these parameters into consideration, the display will be complicated and therefore relatively expensive to build. The main advantage of the system is its wide operating temperature range, which extends from −40° to 80°C without much change in response time.

As the foregoing indicates, electrochromic displays are in many ways attractive passive devices. Besides a too short operating life, their slowness of response and matrix addressing difficulties remain the two chief obstacles to their commercialization.

Improved response times will require the development of transparent electrodes with higher electronic conductivity and of electrolytes with higher ionic conductivity. Larger diffusion coefficients for ions in the metal oxides would also shorten the response time. Moreover, an improvement of about one order of magnitude in power consumption is theoretically possible if electrochromic materials with better absorption characteristics are used.

As for matrix addressing, it seems to be possible, at least within certain limits. The problem is that the electrochromic cell, unlike an LCD or LED, lacks a well-defined threshold for turning on because its coloration proceeds linearly with the applied current. Consequently, in a conventional matrix-addressing scheme, half-selected dots would turn on to about half of the intensity of fully selected dots, giving unacceptably high crosstalk (Fig. 3a). The solution is to inhibit all the unselected electrodes, rather than leave them at ground level.

## Matrix addressing

One simple means to this end has been demonstrated by Optimal Logic Corp. of New York and uses field-effect-transistor switches to gate drive signals to the row and column electrodes. The switches' off state—a high impedance that approximates an open circuit—lets no appreciable current flow to a half-selected cell. In this case, rows of electrochromic electrodes are sequentially brought to ground potential through the switches and returned to the open state. While the selected row is held at ground, the desired columns' counter electrodes are raised to about +1.5 V for writing or lowered to −1.5 V for erasing.

Eliminating the negative voltage supply should also be possible, since the total voltage difference required is only about 3 V. For example, selected rows could be held at 1.5 V, with columns raised to 3 V and lowered to ground for writing and erasing (Fig. 3b). Three-state bus-interface chips, which can have off-state leakage currents as high as 100 microamperes, are inadequate, since currents as large as this would quickly erase an electrochromic cell. However, bilateral complementary-MOS switches like the 4066 could be used, as their rated off-state leakage currents are about 10 picoamperes. ☐

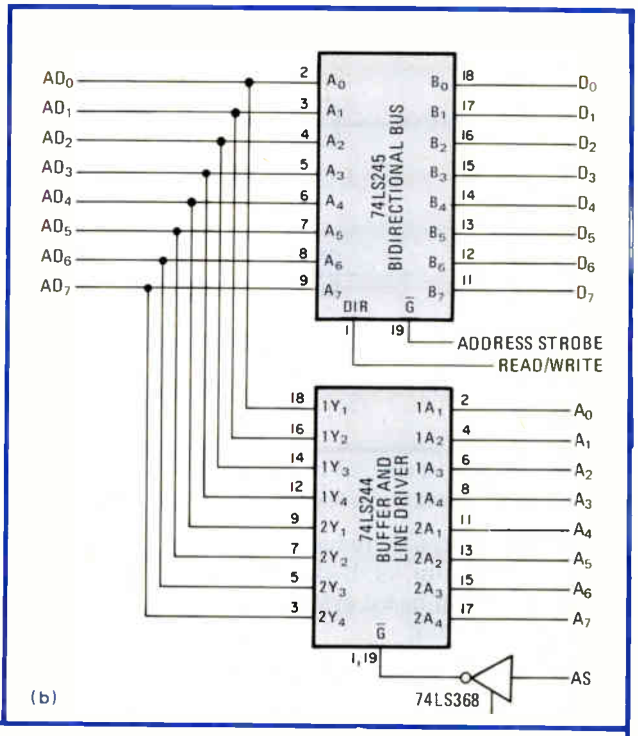
## HP64000 emulates MC6801/6803 using bidirectional multiplexer

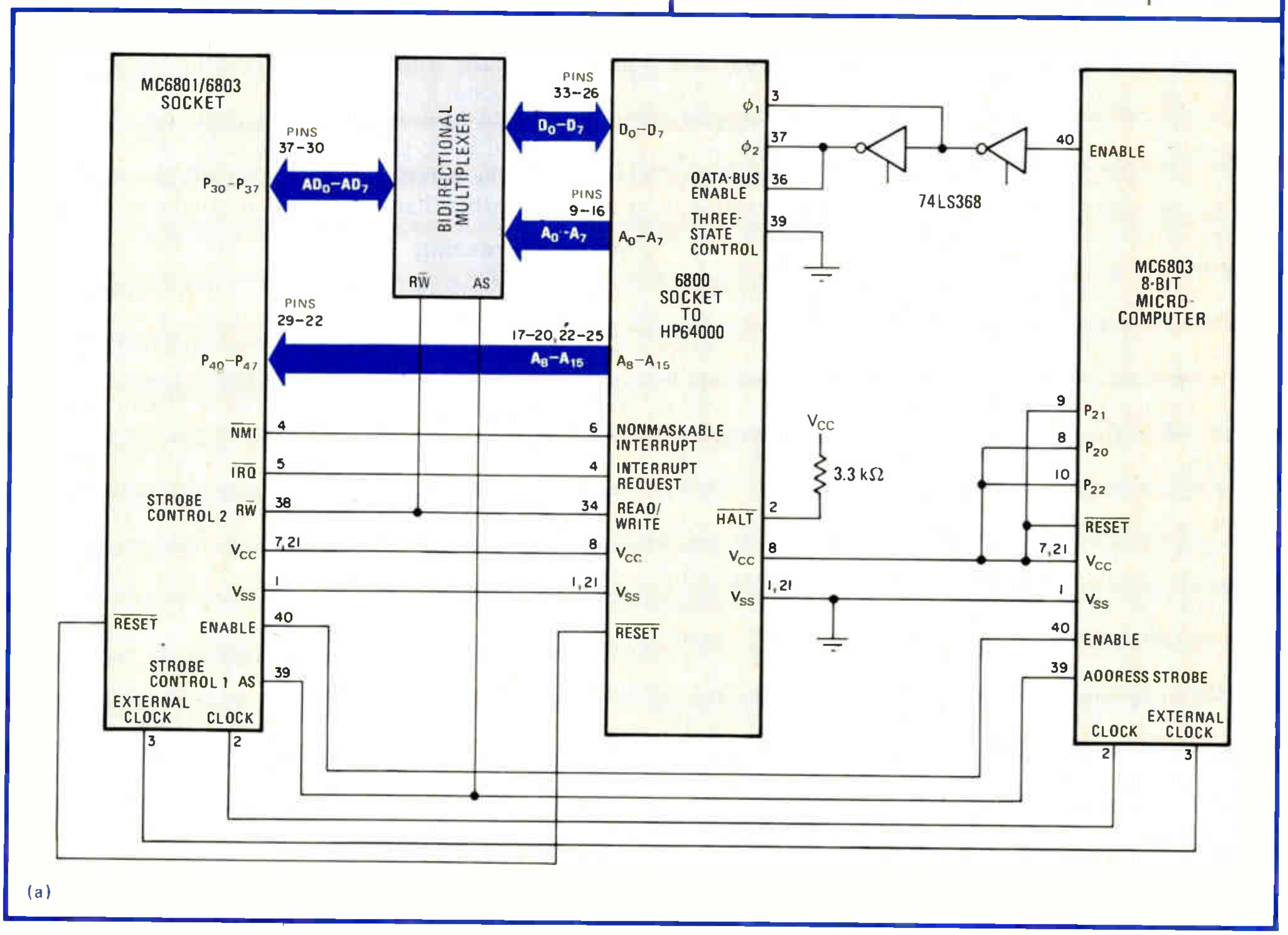
by M. F. Smith
*Department of Computer Science, University of Reading, Reading, England*

Because Motorola's MC6801 and 6803 single-chip, 8-bit microcomputers have a multiplexed address and data bus, they are not compatible with MC6800 hardware and therefore cannot exploit the 6800 in-circuit emulation available on the HP64000 development system. However, with the aid of a two-chip bidirectional multiplexer, the HP64000 can be made to emulate the processor portion of these nearly identical chips.

The devices are attractive for a wide range of applica-

**Emulation circuit.** The circuit (a) allows the HP64000 to emulate the microprocessor portion of both the MC6801 and 6803 by using a converter board that is connected to the HP64212A emulator probe. The bidirectional multiplexer (b) combines the nonmultiplexed address and data lines of the MC6800 emulator.



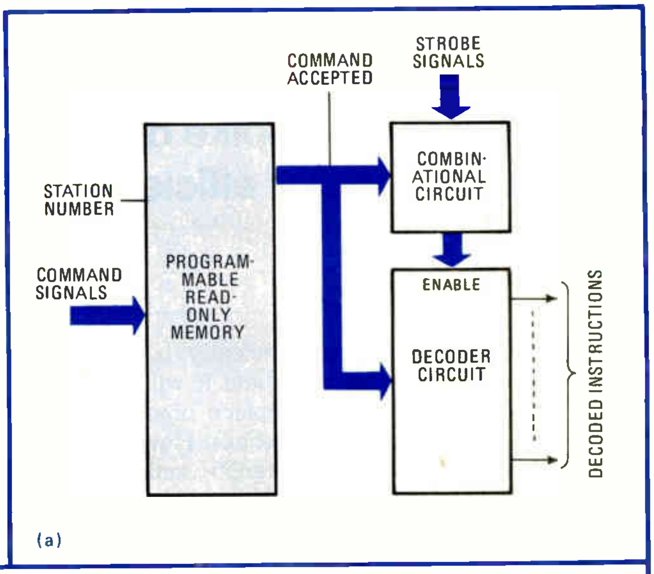
tions, particularly with Hitachi's recent introduction of a complementary-MOS version of the 6801. Besides having complete source and object compatibility with the 6800 software, they have extra instructions for 16-bit operations, an 8-bit multiply, and an X: = X+B instruction, not to mention PSHX/PULX. The units are about 20% faster than the 6800 at the same clock speed.

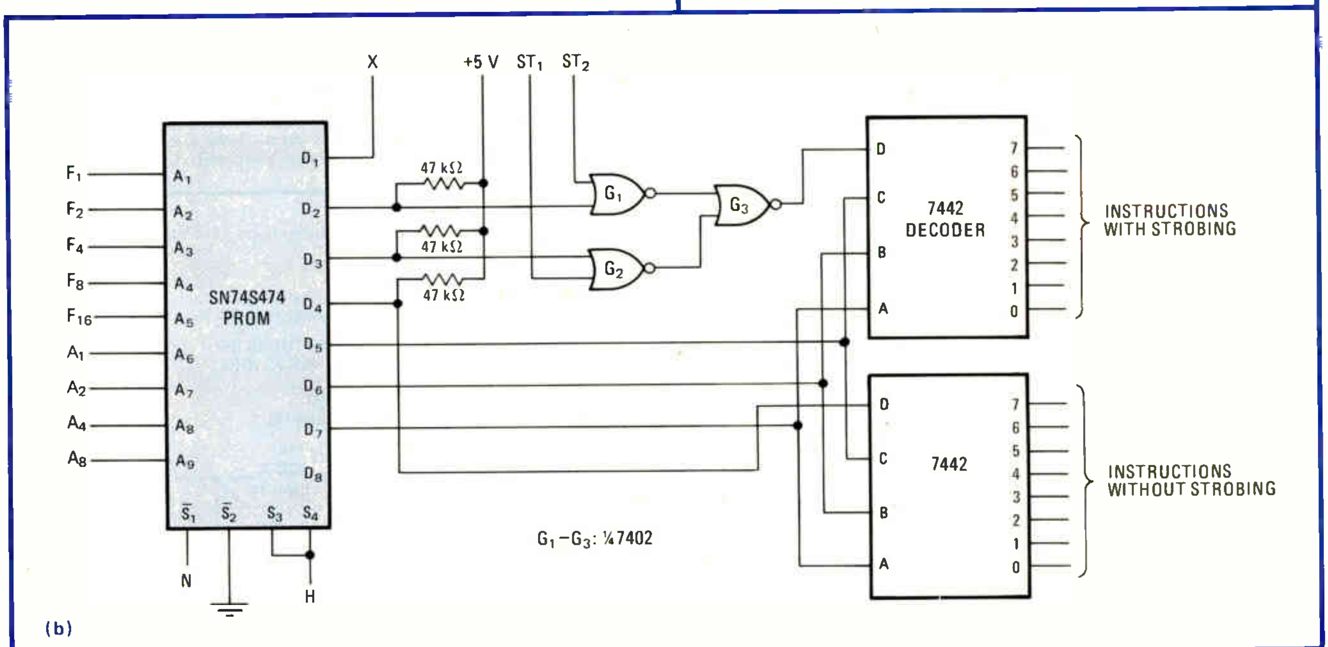
The circuit (a) allows the HP64000 development system to emulate the microprocessor portion of both the 6801 and 6803 by using a converter board that is connected to the HP64212A emulator probe. The bidirectional multiplexer (b) combines the nonmultiplexed address and data lines of the MC6800 emulator. An address strobe is derived by using a dummy 6801 or 6803 as a clock generator. The circuit allows only the expanded multiplied mode to be emulated. Thus it is not possible to emulate the random-access memory or the input and output of the 6801 or 6803 with this circuit. The assembler of the HP64000 for the 6800 allows use of the extended instruction set of the MC6801/6803. □

# Bipolar PROMs make versatile Camac instruction decoders

by István Hernyes and János Nagy
*Central Research Institute for Physics, Budapest, Hungary*

Whenever a computer is hooked up to peripheral devices using a data bus and there are more data lines needed than can be provided by an IEEE-488 interface system, the Camac instruction and interface standard may be inserted into the IEEE-488 to pick up the slack. Inexpensive and versatile, the computer-automated measurement-and-control instruction decoder may be easily built by exploiting the fast access time and low cost of bipolar programmable read-only memories. This principle may




**Decoder.** A Camac instruction decoder (top) uses a bipolar PROM as a code converter. The PROM's output also controls the combinatorial circuit employed to strobe the decoded instructions. One such circuit (bottom) uses the SN74S474. Various pull-up resistors are connected to the pins $D_2$ through $D_4$ to guarantee high-level logic when the module is not selected by N.

also be applied to other bus-oriented systems.

Codes for every Camac instruction are programmed into the memory, and the decoder uses a bipolar PROM as a code-converter prior to the decoding circuit (see figure, top). The Camac module is specified by a station number N. Five function lines: $F_1$, $F_2$, $F_4$, $F_8$, and $F_{16}$, and four subaddress lines: $A_1$, $A_2$, $A_4$, and $A_8$ constitute a command for a specified module.

During each command operation, the Camac controller generates two sequential strobe signals $ST_1$ and $ST_2$ on separate bus lines. Whenever a module recognizes a command, it generates an active logic level on the X-line. The command signals are maintained for the full duration of dataway operation.

The station N and the function and subaddress lines are all tied to the address input of the PROM, which converts the 9-bit instruction into a 6-bit instruction for the decoder and combinational circuit. The N line may be connected to the enable input as well.

The output of the decoder circuit corresponds to different Camac instructions and one output of the memory represents an X-answer. The decoder circuit may be enabled for a full Camac cycle or the duration of a strobe signal.

The circuit in the bottom of the figure uses a 512-by-8-bit PROM that has three state outputs. The $D_1$ pin of the PROM gives the X answer when the Camac instruction is identified by the module. The combinational circuit has three NOR gates. The zero through seven pins of the upper 7442 decoder correspond to instructions that must be strobed by either $ST_1$ and $D_2$ (low) or $ST_2$ and $D_3$(low). Pins 0 through 7 of the lower 7442 generate instructions without strobing and are selected by pin $D_4$ of the PROM. □

# Reverse magnetic spike drives switching transistor efficiently

by John Klimek
*Pretoria, South Africa*

Driving switching transistors efficiently is a problem faced by power-supply designers, and it will take some time for V-MOS transistors to replace bipolar ones in high-current power-supply applications. However, starting conduction with a reverse magnetic spike can both cut design costs and improve switching efficiency.

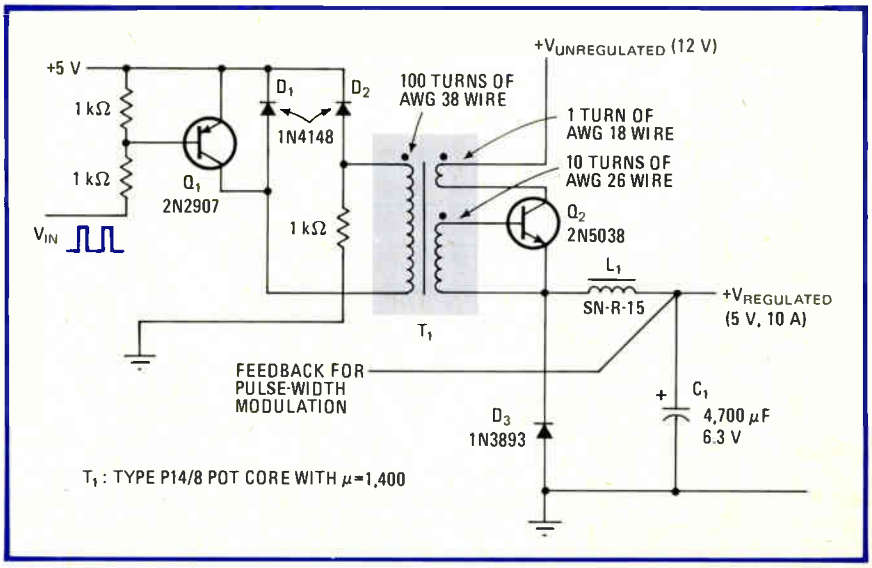
The conventional method of using a simple resistor-limited drive generates high power losses, and a Darlington transistor connection is lossy due to high $V_{ce(sat)}$ and increased switching times. In addition, a current transformer drive is efficient but lacks the ability to start and stop the current cycle in a power transistor.

The current transformer, $T_1$, is the heart of this circuit. Transistor $Q_1$ conducts when $V_{in}$ is low and supplies about 5 milliamperes into the 100-turn transformer winding. When $V_{in}$ becomes high, $Q_1$ turns off and the stored magnetic energy develops a reverse spike simultaneously on all three transformer windings.

The spike through the 10-turn winding starts to conduct $Q_2$, which is now in the current-transformer self-driving mode. When $V_{in}$ goes low again, $Q_1$ starts to conduct and along with $D_2$ shunts the voltage across the 100-turn winding, thereby terminating the driving current of $Q_2$. This shunting is followed by the termination of the main current. Once the main current is stopped, the magnetizing current is supplied to the 100-turn winding and the entire cycle repeats.

The high turns ratio of 100:1 enhances switching efficiency because only 150 mA of current is shunted by $Q_1$ to stop 15 amperes through $Q_2$. In addition to efficiency, the circuit provides excellent insulation between the switching transistor and driving circuitry. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.




**Drive.** The current transformer $T_1$ reduces ohmic and switching losses, thereby driving the transistor efficiently. In addition to an efficient high-current drive, it also provides good insulation between the switching transistor and driving circuitry.

### Counter checks rpm to tune car systems

The modern breakerless high-energy automotive ignition system presents something of a problem when it comes time to tune it up. Most standard tachometers will not work with it, yet frequent tune-ups are a must to keep an engine and an emissions control system operating efficiently. According to William D. Kraengel Jr. of Valley Stream, N. Y., one solution is to view the ignition system as a black box providing certain relevant output information. The spark-plug firing pulses this unit generates **radiate sufficient energy for detection by a simple whip antenna** placed near a spark-plug wire.

The ordinary automobile engine with four strokes per cycle fires its spark plugs once every two revolutions. Hence the frequency (in hertz) indicated on a frequency counter connected to the antenna is multiplied by 120 to find the engine's revolutions per minute. For the two-stroke-per-cycle engine of some motorcycles and lawnmowers that fires its plugs once each revolution, the rpm is 60 times the indicated frequency. If the antenna is placed near the ignition wire connecting the pickup coil to the distributor, then the indicated frequency must first be divided by the number of cylinders before calculating engine rpm. For example if 20 Hz is measured near the coil distributor wire on a four-cylinder automobile engine, the engine is running at 120(20/4) or 600 rpm. Finally, since ignition voltages can be as high as several tens of thousands of volts, no direct connections should ever be made.

### Pipe cleaners have hi-tech uses

Pipe cleaners, usually a relatively thick wire wrapped in a soft material, are not ordinarily associated with electronics. However, a Greenwich, Conn., manufacturer of these low-cost items, U. S. Tobacco Co., recently found itself with some fairly large unsolicited orders. The cleaners' lint-free 50% acrylic, 50% cotton outer wrap was what attracted the customers, firms completely unrelated to the tobacco industry.

A little investigation revealed that the flexible, fuzzy product was being used by one firm to clean circular wirewound potentiometer windings before final assembly and by another to wipe off unwanted resistive thick-film material from the gold leads of a thick-film resistor substrate. The soft outer material of the cleaner **did not abrade or scratch the resistive wire or the gold leads.** It also turned out that yet other electronics firms used U. S. Tobacco's pipe cleaners to touch up solder joints and remove flux while inserting components into printed-circuit boards.

### Workshops set on pc boards

The Institute for Interconnecting and Packaging Electronic Circuits will conduct a series of workshops this coming year that are aimed at helping printed-circuit–board firms keep abreast of the latest developments in their field. The sessions include: the technology of combining rigid and flexible boards, Irvine, Calif., Jan. 19–20; microsection techniques and practices, Palo Alto, Calif., Jan. 27–29; **computer-aided artwork generation, Sunnyvale, Calif., Feb. 10–11;** electronic assembly-soldering technology, Sunnyvale, May 25–26; a mass lamination workshop, Andover, Mass., Sept. 21–22; surface mounting of components, Newark, N. J., Nov. 15–16; plasma etching for smear removal, Seattle, Wash., Nov. 30–Dec. 1; and computer-aided design of pc boards, Orlando, Fla., Dec. 12–15. Additional information can be obtained by writing or calling IPC headquarters at 3451 Church St., Evanston, Ill. 60203. The institute's phone number is (312) 677-2850.

**-Jerry Lyman**

# Scope speeds voltage, time readings

60-MHz oscilloscope's built-in autoranging voltage and frequency meter increase the operator's efficiency

by Richard Comerford, Test, Measurement, & Control Editor

**The past year's** emphasis in the under-100-MHz oscilloscope market has been on trimming the price tags of units with traditional features. But as much as unit price is a factor in the test and service business, so too is the cost of the technician who operates it. With its model SC61, Sencore is offering to reduce the latter expense by boosting the operator's efficiency.

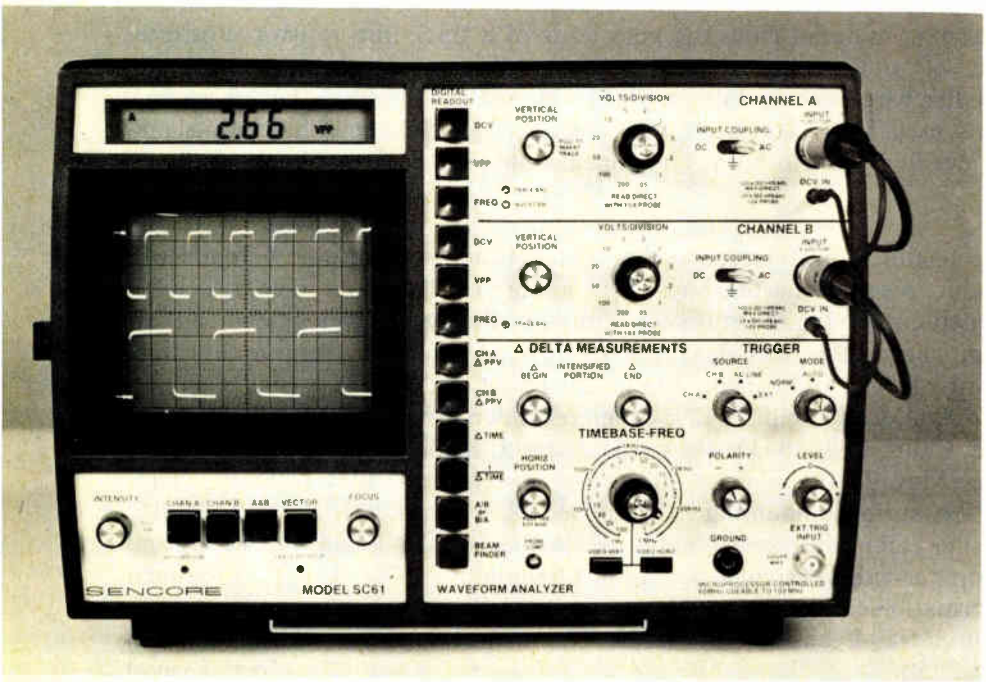
The model SC61, which the company refers to as a waveform analyzer, is a 60-MHz oscilloscope (usable to 100 MHz) that automates the most common measurements for which a scope is used. For either of the signals displayed on the dual-trace unit's 8-by-10-cm screen, a user can press a button and automatically obtain the dc voltage level, peak-to-peak voltage, or a frequency reading. Readings are displayed in a second or less on an integral liquid-crystal display.

"We've eliminated all that graticule counting, calculation, and 'head work' in general," the firm's national account manager, Jim Smith, says. "You get the answer 10 times faster than any conventional scope method, and the accuracy is 10 to 10,000 times better, depending on the function used." In fact, the company backs up its guarantee that the SC61 will cut overall measurement time by at least half with an offer to take back the unit for a full refunding within 30 days.

With the SC61, the user gets an automated digital voltmeter and frequency counter for $3,275. As a digital voltmeter, the unit is autoranging across four ranges—0–2, 2–20, 20–200, and 200–2,000 V—giving 3½-digit readings accurate to within ±(0.5% + 1 count).

For peak-to-peak voltage readings, the SC61 employs a special circuit, on which a patent is still pending, that automatically tracks a channel's vertical attenuator. Peak-to-peak measurements are also autoranging in four ranges—0–8, 8–80, 80–800, and 800–2,000 V—and are accurate to within ±(2% + 5 counts) calibrated at 1 MHz.

As a frequency counter, the unit has six ranges that are automatically selected—1–100 Hz, 100–1,000 Hz, 1–100 kHz, 100–1,000 kHz, 1–10 MHz and 10–100 MHz. Using the optional PR47 probe, measurements can be extended to 600 MHz.




**More automation.** Not only does the scope make basic measurements possible with a single button, but a cursor speeds delta measurements. Setting the cursor with two knobs to indicate the starting and ending points of the measurement, the user can take the peak-to-peak difference between points other than the maxima and minima of signals. Also, the time between two events or a wave's period can be measured.

Particularly useful for ascertaining the response of phase-locked loops and frequency multipliers and dividers is the ratio function. To make such measurements, the user need simply place, say, channel A's probe on the input and channel B's on the output and press a button. The scope's processor then takes over, calculates the frequency ratio, and displays it on the LCD.

Delivery is in 30 days.

Sencore, 3200 Sencore Dr., Sioux Falls, S. D. 57107. Phone (800) 843-3338 [338]

Instruments

# System eases test generation

## Engineer needs no software training to set up tests on functional board test system

The 8150 and 8175 functional digital and analog board test systems from Elecon Inc. offer high throughput at low cost and boast a unique waveform-display approach to test-vector generation and board diagnostics. The 8100-series systems are modular in design for very flexible configuration. Although they are primarily intended to test boards, including those combining analog and digital circuitry, their versatility makes them useful for integrated-circuit testing as well, according to the two-year-old firm.

The systems use vacuum beds-of-nails fixtures with a minimum of 408 points and a maximum of 768 to probe all the nodes on a board. Automatic diagnostics are thus able to guide the operator to the earliest failing node without the use of a hand-held probe. Each test point is backed by at least 1-K of 100-ns random-access memory for storing test vectors.

Digital or analog drive modules send the locally stored test vectors to the unit under test, and receiver modules collect and save the output response vectors. The receiver modules simultaneously compare the output vectors against known-good responses stored in RAM, passing failure data to the control module if discrepancies are found. These operations are performed in parallel at a step rate greater than 2 MHz. Typical test times are less than 15 s per board and rarely more than 30 s, says Elecon.

The system has a dual-threshold hysteresis band on each independent receive pin; the thresholds are programmable over a 30-V differential range. This allows the test system to catch marginal logic levels and to test boards that use a mixture of logic families (emitter-coupled logic requires an optional module).

Digital driver modules allow logic-0 drive levels to be set at 0 to 0.7 V and logic-1 levels at 3 to 15 V; if negative drive for logic 0 is needed, an analog drive module can be used. Analog drive modules can generate waveforms at test step speed, ranging from −15 to +15 V (−30 to +30 V, optionally). The power supplies driving the unit under test can source or sink up to 2 A at 30 V.

Elecon has focused on a major source of trouble with test systems—test software generation. The 8100 system can be programmed by a test engineer with no software experience, eliminating a major bottleneck in this process. Generating test stimuli entails manipulating graphics (on a built-in cathode-ray tube) that look just like a logic analyzer's timing diagram. A known-good board is then used to store the proper response in system memory. Elecon offers programming services to assist customers with a backlog problem, as well as a customer-training program.

**Automated analyzer.** The logic-diagram approach is also used to communicate detailed failure data. The system captures all nodal data and displays it as oscilloscope waveforms, much as if the diagnostician had a 768-channel logic analyzer that eliminated all set-up and probing problems and that could find the earliest failing node automatically. The technique is well suited to boards using microprocessors and parallel buses.

The 8100 systems use an Intel 80/30 central processing unit, dual 8-in. floppy-disk drives, and a 20-column thermal printer for diagnostic messages during go–no-go testing. A standard 8175 system at $90,000 includes a 1,700-point Pylon vacuum receiver cabled for 768 points (Elecon offers a complete fixturing-fabrication service), a 50-slot system bus, software, and assorted modules, including four for digital receiving, four for digital drive, two for analog receiving, one for analog drive, a power regulator, and a system-bus extender. A minimum 8150 system can be had for $82,000. This configuration is cabled for 408 points and includes half the number of digital driver, digital receiver, and analog receiver modules, compared with the standard 8175.

Delivery is in 70 days.

Elecon Inc., 2106 Ringwood Ave., San Jose, Calif. 95131. Phone (408) 946-6000 [351]

# HP-41C gets loop interface

## Serial loop lets calculator control DMM, peripherals in low-cost portable system

A little brother to the IEEE-488 bus has been born at Hewlett-Packard. A module implementing the HP interface loop, or HP-IL for short, plugs into any of the four ports in the firm's HP-41C or -41CV hand-held programmable calculators, giving the microprocessor in these devices low-cost, low-power 40-kb/s twisted-pair serial communications with and control over such peripherals as tape drives, printers, and instruments.

Making possible a versatile, fully portable computer system is the concurrent introduction of compatible battery-operable peripherals: the 82161A digital cassette drive, 82162A thermal dot-matrix printer/plotter, and 3468A digital multimeter. Also available are the 8293A HP-IL interface card for HP 83 and

85 personal computers and the 82166A HP-IL converter, which is intended to be built into any microprocessor-based product for connection to the loop. The firm plans to offer a larger impact printer, a video (television or monitor) interface, interfaces that link the HP-IL to RS-232-C lines and IEEE-488 buses, and other compatible instruments and peripherals.

A 2-byte addressing scheme allows a potentially large number of devices to share a single communications loop. Data is passed in one direction around the loop and checked for errors on its return to the originating device. Zip cord allows a 10-meter distance between one device and the next; a twisted shielded pair extends the possible distance to 100 m. As devices are added to the loop, each one powers the loop to the next device; thus the cost of and power supply for communications is shared among devices rather than heaped upon a single unit.

The loop makes use of miniature pulse transformers for isolation (devices such as multimeters can be floated at a different potential from ground relative to other system units), immunity to noise, and elimination of ground loops. The transformer is a passive device requiring no standby power. A three–voltage-level redundant data-coding scheme contributes to the reliability of communications on the loop.

For $125 a user can buy the 82160A HP-IL module, which plugs into the calculator and allows it to talk with up to 30 devices on one loop. (Extended addressing could allow a controller to communicate with up to 960 devices.) In addition to the pulse transformer, the small module contains a large-scale integrated circuit that implements the HP-IL protocol and most of the necessary driving and receiving functions. This chip is made using silicon-gate complementary-MOS technology; it helps keep down parts count, power use, and price. The loop structure provides for automatic device-address assignment, device identification, and power on-off control. A device on the loop can be a talker, a listener, or switch between the two roles.

**Mass storage.** The 82161A digital cassette drive, priced at $550, stores 131,000 bytes on one miniature cassette. This HP-IL-compatible drive has bidirectional access, reading at 9 in./s and searching at 30 in./s. It operates on an ac line or battery power and makes the HP-41 useful for data-collection and management jobs previously requiring a larger computer.

The battery- or ac-powered portable 82162A 24-column printer/plotter puts out hard copy of data, program listings, bar code, and graphics. Priced at $495, it has all the features of the 82143 printer/plotter, plus HP-IL interface, enhanced graphics, and a larger buffer.

The first HP-IL-compatible digital multimeter is the 3468A, a fully programmable five-fuction unit priced at $695. Data logging using this meter and an HP-41 can be done at the lowest cost yet, says HP. The meter's 12-character, 14-segment alphanumeric liquid-crystal display shows readings, measurement units, and messages generated by either the meter or its controller.

The user can adjust the 3468A's resolution to 3½, 4½, or 5½ digits with a proportional tradeoff in measurement speed. At 3½-digit resolution, it can take 71 dc voltage readings per second, for instance; at 5½-digit resolution, the reading rate is 4.4/s. The integrating multislope analog-to-digital converter that makes the speed-resolution tradeoff possible also achieves high normal-mode noise rejection—80 dB at 50 or 60 Hz in the 5½-digit mode.

The 3468A's functions are calibrated without trimmers and without removing the cover; there are no internal adjustments. Calibration constants are stored in C-MOS random-access memory backed by a lithium battery; this nonvolatile RAM can remember the constants for 10 years. The rest of the unit's electronics are powered by ac line power or an optional rechargeable lead-acid battery pack.

Functions of the 3468A include two- and four-wire resistance measurement and ac current and voltage measurements with true root-mean-square conversion from 20 Hz to 300 kHz. Ac accuracy at midrange is within 0.25%; other functions' 90-day accuracy specifications are typically within 0.008% of reading or better. The 3.9-by-9.4-by-10.9-in. meter weighs 4.6 lb; with the lead-acid battery pack it weighs 6.8 lb.

A similar DMM, the 3478A, is being introduced at a price of $1,300. It interfaces with the IEEE-488 bus instead of the HP-IL, reads somewhat faster than the 3468A, and has better sensitivity on dc, ohms, and current ranges.

The 82166B HP-IL converter for integration into other devices is priced at $125 in quantities of 10. It buffers 32 bytes of data from host or the loop, accepts TTL-level signals from its host, and runs on 5 V dc at 90 mA maximum. A prototyping kit for the converter, designated 82166A, is available for $395.

**More modules.** Four modules for the HP-41C or -41CV are also being introduced, all priced at $75 each. The time module, model 82182A, gives the calculator a clock function so it can execute a program, control a peripheral, or set off an alarm at specific predetermined times. With it the calculator can display time and date and provide calendar data over a 2,738-year span.

The 82183A extended input/output module allows the HP-41 user to copy programs and data from one cassette drive to another. It also allows programs to be printed in bar code by the printer/plotter. The 82181A extended memory module adds 4,221 bytes of RAM.

Using the latter module requires an 82180A extended function/memory module. This module adds 889 bytes of RAM and 47 functions to the calculator. The functions allow the user to change memory configurations and keyboard function assignments under program control. The file-structure and file-management capabilities it provides increase the HP-41's flexibility and memory efficiency. It allows ASCII files to be created, in addition to program and data files, making possible communications with larger computers.

The modules, peripherals, and multimeters described are available now from HP and its dealers.

Hewlett-Packard Co., 1820 Embarcadero Rd., Palo Alto, Calif. 94303 [352]

## Optimized unit tests op amps, converters, regulators only

An optimized version of Teradyne's larger A300 analog LSI tester, the A351 industrial linear IC test system offers the same accuracy as the bigger unit, but is directed exclusively at operational amplifiers, voltage regulators, and medium-precision digital-to-analog converters.

The A351 has four-way multiplexing to automate handlers or probers and uses the same software as the A300. Also like the A300, the A351 uses the Test System Manager, a second-level computer, for uninterrupted testing and parallel job programming and data analysis.

The basic source and measurement module includes seven ±60-V, ±200-mA programmable voltage or current sources. Its measurement accuracy is typically 0.05% of reading or an order of magnitude better with an optional high-precision module. Twenty-four channels of static digital drivers and detectors are included with data rates up to 100 kHz and job programming is done in Pascal/Steps, a high-level modular language. When delivered in mid-1982, the A351, which includes four test sockets, will range in price from $88,000 to $144,000.

Teradyne Inc., 183 Essex St., Boston, Mass. 02111. Phone (617) 482-2700 [353]

## Programmable bit-pattern generator runs up to 20 Mb/s

With these two generators, the PO-1 or the VF-1, users can test digital circuits and telephone noise and transmission levels. The PO-1, a universal pattern generator, is programmed like a simple computer to put out special and unique digital bit patterns. The user builds patterns by entering message bits and commands such as go-to, repeat, and send. Once entered, the patterns can be sent as often as necessary or modified.

The PO-1 will prove its value in testing data-communications hardware and protocols like X. 25, microprocessors, and process-control monitors. Controlled by an IEEE-488 interface bus, the small unit is compatible with TTL, complementary-MOS, and emitter-coupled logic and can operate at up to 20 Mb/s. The PO-1 sells for $7,300, with delivery in 30 days.

For making telephone transmission-line level and noise tests, the VF-1, both a generator and receiver, features a synthesized signal generator for frequency stability and simultaneous digital readout of level and frequency, as well as an accuracy of 0.1 dB for 1,000-Hz test-tone measurements. It has a built-in speaker for listening tests and four noise-weighting filters. The VF-1 is designed to meet the recommendations of Bell Publication 41009 and sells for $1,995.

W&G Instruments Inc., 119 Naylon Ave., Livingston, N. J. 07039. Phone (201) 994-0854 [354]

## In-circuit testing goes portable

Enhancing GenRad's 2225 portable service processor and 2235 logic test system to include in-circuit as well as functional testing is just one of the 2255 test adapter's purposes. When used with the 2225 and 2235 test systems, the unit reduces the time it takes to isolate faults and improves fault resolution.

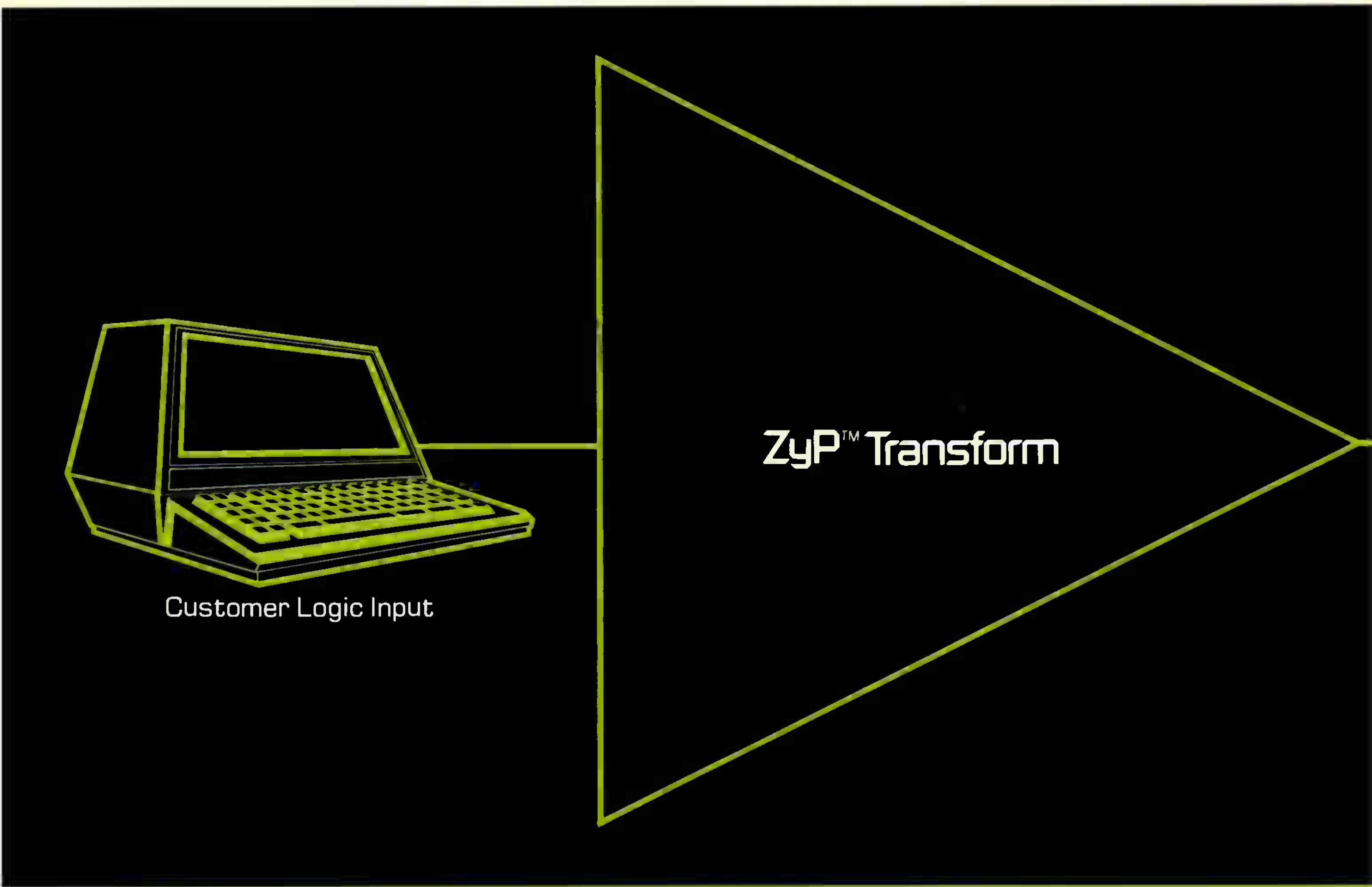
A library of standard devices implemented in emitter-coupled logic, complementary-MOS, TTL, and diode-transistor logic minimizes both the time and cost of programming by eliminating the need to generate unique programs for each printed-


circuit-board type, as was previously required for units that were tested solely functionally. Nonstandard devices are programmable by means of truth-table inputs.

The adapter can also aid in board initialization and preconditioning, thus reducing the overall test-program time for the 2225 and 2235 systems. Pricing for the 2225 in-circuit test adapter begins at less than $10,000.

GenRad Inc., 300 Baker Ave., Concord, Mass. 01742. Phone (617) 890-4900 [355]

# The ZyP™
# The First Comprehensive CAD VLSI

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Software

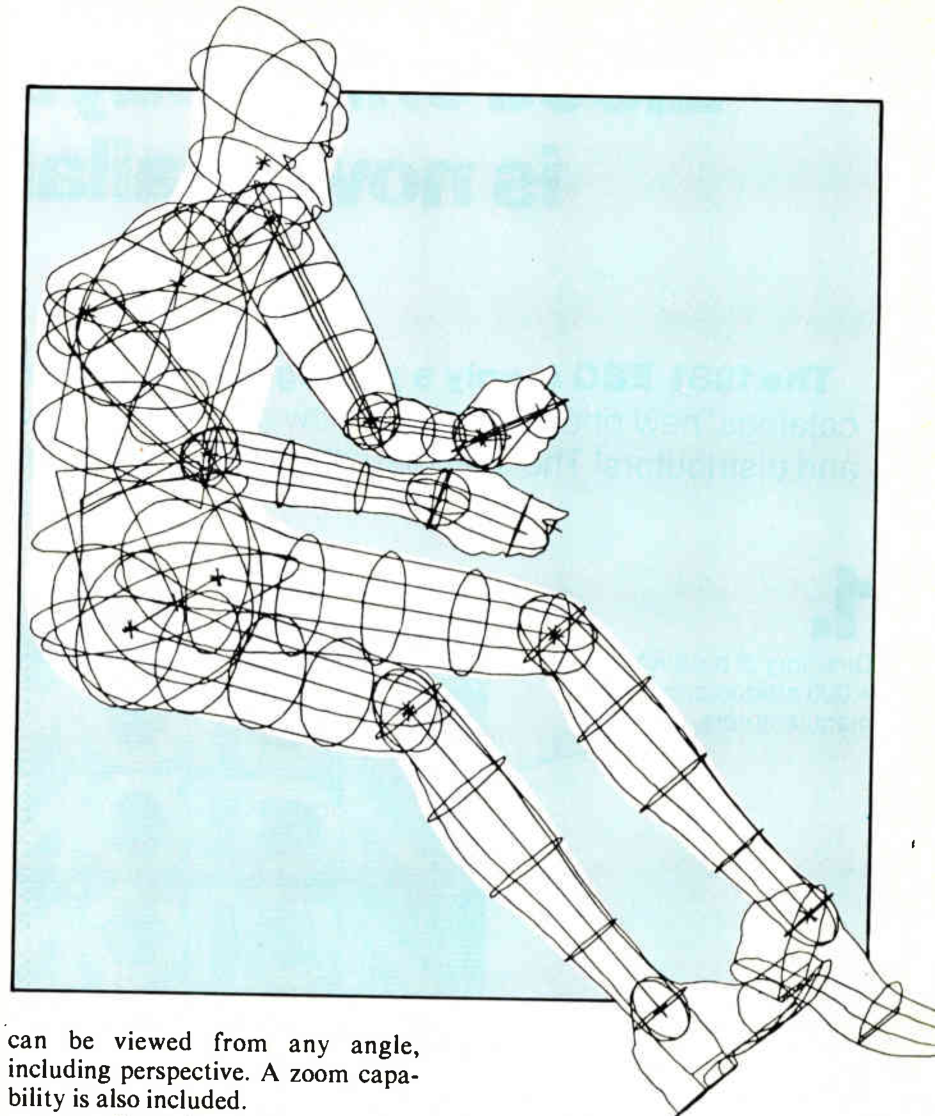
# CAD program creates man

## Along with graphics software, program draws 3-d man for human-factors engineering

Human-factors engineering is at last within the province of computer-aided design now that a three-dimensional software package designed to interface with other graphics software is available from Control Data Corp. Known as Cyberman, the $60,000 package is being sold under license from Chrysler Corp., which developed the program initially for its own use. Development of the stand-alone version for outside sale came at the request of Volkswagen, which recently installed the package at its engineering division in West Germany.

Written in a Fortran-based high-level language known as Quickcon, Cyberman is intended for use on Tektronix 4010, 4014, or 4016 graphics terminals that are linked to a CDC Cyber series 170 or 700 mainframe. CDC says the package could be useful not only in automotive design but in any application in which such human factors as reach, positioning, and comfort are a consideration. Aerospace and materials-handling equipment design are likely applications, as are workplace analysis studies, the firm adds.

The Cyberman program is designed for static positioning of its manikin in attitudes preselected by the operator. The manikin can be represented either in stick-figure or wire form and is created by entering as prompted at the terminal numbers that define joint angles and body position. The data-entry process takes less than five minutes, according to Chrysler engineers, and positions can be stored in memory for later use. Fine positioning can be done by selectively substituting new control number values. The manikin can be viewed from any angle, including perspective. A zoom capability is also included.



Body dimensions of the manikin are based on a standard from the Society of Automotive Engineers. Unless otherwise directed, the package brings up on the screen a so-called 95th percentile man, who is 6 ft, 3 in. tall. There are, however, no constraints on the size of the manikin used.

The Cyberman package is available on magnetic tape for disk loading. The package requires 130-K bytes of main memory when in use.

Control Data Corp., 5001 West 80th St., Bloomington, Minn. [371]

## One package manages data, uses it in letters and lists

With its new word-processing capabilities, the Sequitur data-base–management system can produce form letters and mailing lists and manipulate text as well as run a data base and generate reports.

The screen-oriented Sequitur takes a unified approach to data-base definition, data entry and editing, and command specifications with its matrix-like data display and graphics query language. This graphically implemented command language provides screen prompting for all fill-in-the-blank commands. Status lines provide current information about the system's state.

The core package includes capabilities for selecting, sorting, combining, and copying data from tables and parts of tables, as well as a report generator and a form generator that formats reports. Basic computations and statistical data analyses are other abilities. The word-processor functions let the user edit any part of a table, create form letters and mailing lists from stored data, and retrieve information.

Sequitur will soon be enhanced with packages such as programming-language interfaces, arithmetic computations from data for reports and selections, and structured document processing. Sequitur operates on any 16-bit machine under the Unix version 7 or Unix–look-alike operating systems. Available in January, Sequitur will retail for $3,495.

Pacific Software Manufacturing Co., 2608 Eighth St., Berkeley, Calif. 94710. Phone (415) 540-0616 [373]

## Software maintains data base, performs general accounting

Using an easy-to-understand system language, the Formula lets nonprogrammers create sophisticated program modules for business applications. In addition, it increases the efficiency of veteran programmers.

It creates, maintains, updates, and modifies data-base files; develops data-entry routines; implements user-defined menus; and sorts data-base elements. It also generates free-format reports. Word-processor characteristics let the user highlight or underline text.

The Formula also contains a general accounting system that includes accounts receivable and payable and general ledger. It uses an indexed sequential-access method for data retrieval.

The package is available for all Z80- or 8080-based microprocessor systems running under CP/M or Cromix. It sells for $595.

Dynamic Microprocessor Associates Inc., 545 Fifth Ave., New York, N.Y. 10017. Phone (212) 687-7115 [374]

## Spreadsheet program automates financial modeling

Multiplan, an interactive, menu-driven program, places numeric planning and modeling applications like financial analysis, home budgeting, marketing evaluations, sales projections, and record keeping at the fingertips of nonprogrammers. It provides a grid of cells, called a work sheet, for holding the information the user supplies.

After figures and formulas are entered into memory, they may be modified or rearranged. The program preserves the relationships on the work sheet and recalculates totals and formulas on command or automatically when new information is entered.

The program has eight cells, a help command, and cell formatting and allows easy entry of commands and data. The user can assign descriptive names to work sheet sections for use in formulas and commands and to link a work sheet with off-sheet references.

Multiplan will be available in January and can be used with systems operating under CP/M and with the Apple II computer. It will cost $275 and is also being offered to original-equipment manufacturers.

Microsoft, 10800 N. E. Eighth, Suite 819, Bellevue, Wash. 98004. Phone (206) 828-8080 [375]

## Screen builder supports four CP/M packages

Quickscreen adds screen-building capabilities to four popular microcomputer software tools: Microsoft's Basic, Compiler Systems's CBasic, Ashton-Tate's dBase-II data-base system, and Systems Plus's FMS80 data-base system. The interactive program simplifies and quickens the creation of screen formats, allowing nonprogrammers to build screens in under 3 minutes.

The screens produced may be used for data entry, printing mailing labels, and generating form letters or any type of report. A graphics capability lets users draw lines and columns with a single keystroke.

Each of the four versions of Quickscreen sells for $149, with quantity discounts available.

Fox and Geller Associates Inc., P. O. Box 1053, Teaneck, N. J. 07666 [378]



Circle 133 on reader service card





Circle 105 on reader service card

Communications

# Plug-in modem connects directly

## All-C-MOS interface card for Microboard computers runs at 300 or 1,200 b/s

A single-board modem gives owners of any RCA Microboard computer data-communications capabilities without the headaches of an acoustic coupler. Approved by the Federal Communications Commission for direct connection, the CDP18S653 complementary-MOS auto modem uses only two chassis slots.

RCA's Solid State division is offering two versions of the modem. The Bell 103-compatible -V1 operates at 300 b/s for full-duplex operation, and the Bell 202-compatible -V2 operates at 1,200 b/s for half-duplex operation.

Both boards have automatic and manual answering and originating modes. In the automatic originating mode, a manual switch selects either Touch-Tone or pulse dialing. Software detects the choice and automatically selects the appropriate signaling code. In the manual originating mode, an input connector is provided for optionally attaching an inexpensive two-of-seven keypad that operates either the Touch-Tone or the pulsing dialer.

**Repeat dialing.** In addition, both modems feature dial-tone and busy-tone detection that permits tandem dialing, while busy-tone detection allows repeated dialing. Either board can optionally be configured to provide a full intercomputer data link. This link is for memory-to-memory transfer of files between terminals A and B, as follows.

Station A calls the other from its keyboard. When the link is established, a transparent mode in which A and B can talk back and forth is created. B can type the file name he wants A to send and its hexadecimal destination address.

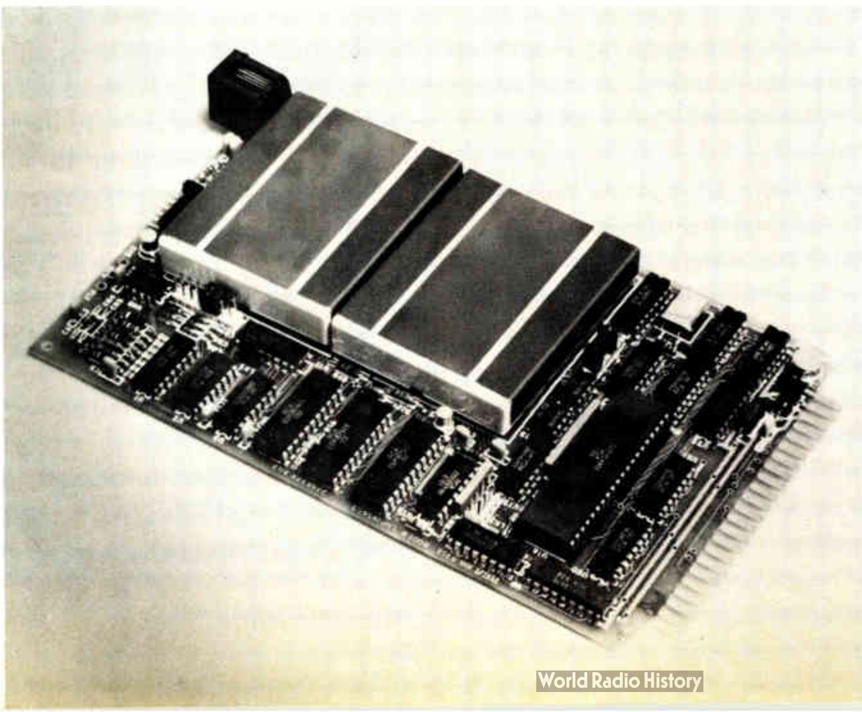
A then types the file destination address on prompting from his terminal, as well as the source address and number of bytes to be transferred. A carriage return starts the transfer. A simple acknowledged–not-acknowledged protocol provides error checking and retransmission if necessary.

The board's all C-MOS design insures minimum power dissipation. Analog loop-back self-testing is provided, as well as a subminiature light-emitting-diode indicator that glows when the modem is connected to the phone line and blinks during outpulsing.

An input connector is optional for attaching a terminal to the modem board with a standard RS-232-C modem port. Power supplies needed are +12 and +5 V, with −5 V required if the modem's RS-232-C port is to be used.

Their maker says these boards will find applications in remote data-acquisition systems incorporating analog-to-digital and d-a converters, in which a central computer or terminal can communicate with the system over phone lines. Available in the first quarter of 1982, the 300-b/s full-duplex version sells for $399, while the 1,200-b/s half-duplex model goes for $449. Quantity discounts are available for original-equipment manufacturers.

RCA Solid State Division, P. O. Box 3200, Somerville, N. J. 08876. Phone (201) 685-6000 [401]



## Fiber-optic data set hits full-duplex 57.6 kb/s

Phalo/O. S. D.'s fiber-optic–systems product line has been expanded to include a synchronous data set, model ODS-209+ for use in high-speed serial synchronous communication between computers and as a communication link for the IBM 3274 remote control unit for repeaterless distances up to 5 km. In addition, the ODS-209+ has a fiber-optic front end that replaces the Bell 209 data set that is designed for 9.6-kb/s digital transmission.

The unit is plug-compatible with the RS-232-C data-set standards and optionally with the IBM 3274 and the RS-422/449 interface standard. It operates in full-duplex mode at standard synchronous data rates from 1.2 to 57.6 kb/s either in an internally or externally clocked mode. The unit also can operate asynchronously at data rates up to 19.2 kb/s.

The ODS-209+ has three-level built-in automatic test circuits for remotely-activated testing in a data-loopback mode; checking the data transmission path for loss of signal, signal quality, and level; and manually activating the local data-loopback mode.

The unit is available in a desk-top model selling for $750 and in a rack-mounted version for $675. Delivery is from stock to six weeks.

Phalo/O. S. D., 9240 Deering Ave., Chatsworth, Calif. 91311. Phone (213) 998-3177 [403]


## Facsimile unit transmits 8½-by-11-in. page in 30 s

The FA 500K is a high-speed automatic digital facsimile transceiver capable of transmitting up to 9.6 kb/s, with automatic step down to 2.4 kb/s. Interfacing with large network-communication equipment, the FA 500K can transceive information in a 8½-by-11-in. format in as fast as 30 seconds.

The transceiver is enclosed in a 250-by-640-by-500-mm housing and has automatic receiving, document-feeding, and reduction functions, along with polling, password and telephone identification features. The end user price is approximately $5,000. The company plans to market the unit to original-equipment manufacturers and to customers who require large quantities of electronic communications equipment.

Mitsubishi Electonics Inc., 2200 W. Artesia Blvd., Compton, Calif. 90220. Phone (213) 637-6246 [405]

## Full-duplex modem operates over a single-fiber cable

The Fibronics FM-801 fiber-optic modem operates in full-duplex over a single fiber-optic cable at standard synchronous data rates to 19.2 kb/s and at asynchronous transmission rates up to 4,800 b/s. According to the manufacturer, transmitting data to computer peripherals and remote process-control equipment at distances up to 3 km, requires only a one-channel fiber-optic cable. Thus cable costs can be cut by 40%, and termination costs by half.

The FM-801 is suitable for point-to-point and multi-drop applications using Fibronics TS-10 optical splitters. To verify link operation, the unit has automatic self-test features, remote loopback and local loopback modes of operation, and continuous fault-monitoring control. All RS-232-C handshaking features are built in. Data input and output are transmitted through a standard 25-pin electrical connector.

The unit is available in rack-mounted or stand-alone versions and is priced at $750 or more, depending on options required. Delivery is eight weeks after receipt of order.

Fibronics, 655 Concord St., Framingham, Mass. 01701. Phone (617) 872-9870 [404]


## Wideband mixers cover the 6-to-12.5-GHz range

Miniature wideband mixers covering the radio-frequency range of 6 to 12.5 GHz are Magnum Microwave Corp.'s MO64M and MO64P. Both mixers feature an intermediate-frequency bandwidth of up to 2.5 GHz, a typical conversion loss of 6.0 dB, and an intercept point of +15 dBm typical at a local oscillator drive of 10 dBm.

The MO64M comes in a drop-in package measuring 0.52 by 0.56 by 0.19 in., and the MO64P comes in a subminature type A connector package measuring 0.676 by 0.892 by 0.375 in. They are priced at $160 and $205, respectively, in quantities of one to nine. Delivery takes from two to four weeks.

Magnum Microwave Corp., 1080 E. Duane Ave., Suite D, Sunnyvale, Calif. 94086. Phone (408) 738-0600 [406]

Semiconductors

# C-MOS logic parts run at 25 MHz

First eight members of family arrive to do battle with low-power Schottky TTL

The first eight members of what will be a large line of high-speed complementary-MOS digital logic devices has been unveiled by Motorola Inc.'s MOS Integrated Circuits Group.

Samples are being made available of the new MC54/74HCXX series, which offers the low-power advantages of C-MOS but has speeds and drive capabilities of low-power Schottky TTL. The fast C-MOS series is being developed by Motorola and National Semiconductor Corp., which will be second sources for each others' independently-developed devices [*Electronics*, Dec. 15, p. 137].

Motorola's initial offering in the new family are: a quad two-input NAND gate, the MC54/74HC00; a quad two-input NOR gate, the MC54/74HC02; a triple three-input NAND gate, the MC54/74HC10; a dual four-input NAND gate, the MC54/74HC20; a quad two-input exclusive-OR gate, the MC54/74-HC86; a binary-coded-decimal decade counter with asynchronous reset, the MC54/74HC160; a 4-bit counter with asynchronous reset, the MC54/74HC161; and a quad two-input exclusive-NOR gate, the MC54/74HC266. Devices with MC54 serial numbers have a temperature range of −55° to +125°C and are housed in ceramic packages. Those with MC74 serial numbers carry a temperature rating of −40° to +85°C and are available in both plastic and ceramic packages.

Prices for samples of the plastic-housed devices in 100-piece orders are: 51¢ each for simple gates (HC00, HC02, HC10, and HC20), 65¢ each for complex gates (HC86 and HC266), and $1.24 each for counters (HC160 and HC161).

The high-speed C-MOS family features include: pin-for-pin compatibility with low-power Schottky TTL; the drive capability of 10 low-power Schottky TTL loads (4 mA sink); a guaranteed 25-MHz clock frequency for counters and 30 MHz for all other devices; and a maximum propagation delay of 15 ns for the simple gates. Deliveries of volume production are set to begin within the first quarter of 1982.

Motorola says more than 100 additional logic devices are scheduled to be introduced to the series next year.

Motorola Inc., 3501 Ed Bluestein Blvd., Austin, Texas, 78521. Phone (512) 928-6880 [411]

## Speaker-independent chip responds instantly to 8 words

Reacting instantly, the speaker-independent WTV008, a single-chip voice-recognition system, recognizes words or phrases in two pages of up to eight words each. The chip has an error rate of less than 10% for 90%

of the user population.

The WTV008 consists of a single-chip digital processor with an analog speech-input preconditioning circuit that receives speech from a low-cost microphone. Recognized utterances activate one of eight bit-line outputs and a four-line binary-coded decimal number output; an output strobe indicates recognition. Indication of recognized output is in real time, and utterance length is limited only by chip data-storage capacity.

For a one-time engineering fee, the manufacturer implements in read-only memory a customer's vocabulary of up to 16 words or phrases. The device will find use in such consumer and industrial items as games, toys, radio- or wire-controlled models, and a variety of appliances.

In a 28-pin dual in-line package, the WTV008 operates over a temperature range of from 0° to +75° C. In quantities of 100,000, the device sells for under $10 each.

Weitek Corp., 3255 Scott Blvd., Santa Clara, Calif. 95050. Phone (408) 727-6625 [414]

## 128-K ROM accesses in 300 ns, dissipates 450 mW

Boasting high speed and low power are two static n-channel silicon-gate MOS read-only memories. The 64-K 2364 and 128-K 23128, in 28-pin dual in-line packages, offer a standard worst-case access time of only 300 ns. The 23128 dissipates 450 mW, while the 2364 is rated at a maximum of 440 mW.

Both ROMs have programmable chip-select inputs, allowing the customer to define high or low and set the desired logic level as part of the masking process. This feature and wired-OR compatibility on the outputs let memory be easily expanded. The parts are TTL-compatible, require only one +5-V power supply, and are available in plastic or ceramic packages screened to either commercial or military temperature ranges. Their maker says that with these ROMs, new, fast versions of 8- and 16-bit microprocessors can be operated without wait states.

The high-density devices are suited to mainframe computers, high-performance microprocessors, terminals, word processors, and telecommunications systems, as well as computer-based teaching systems. In 1,000-piece lots for the commercial temperature-range part, the 2364 is priced at $10 each, while the 23128 sells for $18 each. Prototype delivery is eight weeks after code pattern verification.

Signetics, 811 East Arques Ave., P. O. Box 409, Sunnyvale, Calif. 94086. Phone (408) 739-7700 [415]

**B-staged treated fabric tapes,** Fusa-fab and Fusa-flex are used in electrical and other applications. Fusa-fab, a semicured polyester-treated fiberglass cloth, is available with either Class F insulation capable of withstanding 155°C or Class H insulation, which can handle 180°C. Fusa-flex, a semicured epoxy-treated polyester-glass tape, withstands up to 155°C.

The fabric tapes cure to a tough, rigid structure resistant to moisture, chemicals, and refrigerants. Fusa-fab is available in rolls 108 in. long at prices ranging from $4 to $11, depending on tape width. Fusa-flex, also in 108-in. rolls, ranges from $5 to $26 depending on width.

General Electric Co., Insulating Materials, One Campbell Road, Department 826, RV14, Schenectady, N. Y. 12345 [384]

**A high-purity flux,** #183-SCG Aqua-Sol Flux, free from halide activators and other contaminants, is for use in manufacturing semiconductor devices and soldering the high-density printed-circuit assemblies that are found in high-frequency instrumentation and monitoring or alarm devices. The residues left after soldering are totally soluble in water and can be cleaned to levels exceeding MIL-P-28809 specifications. The flux contains no glycols, which can degrade the insulation resistance values of some insulating materials, and it has a mild acidity (a pH of 3.8) that is excellent for removing tarnish. It has a specific gravity of 0.852 at 77°F (25°C).

The #183-SCG Aqua-Sol flux is available in 1-, 5-, and 55-gallon containers.

Kenco Alloy & Chemical Co., 418 West Belden Ave., Addision, Ill. 60101 [385]

**Silver Protector Strips** help prevent electronic components from tarnishing during processing, shipment, and storage. By absorbing the atmospheric sulphur from the surrounding area, they protect components for two years or longer when used in closed electronic packages. They need not touch the components to be fully effective.

The strips come in 2-by-7-in. paper sheets. Several may be necessary for adequate protection in large shipping cartons, whereas a smaller package may require just a portion of a strip. Depending on the quantity desired, the strips cost from 10¢ to 12¢ each.

3M, Department DM81-1, P. O. Box 33600, St. Paul, Minn. 55133 [383]

**Eccosorb** MF is a series of eight magnetically loaded epoxide rod, bar, and sheet materials for use as absorbers, attenuators, and terminators in waveguides, coaxial lines, and striplines. The series has approximate relative impedance magnitudes in the 0.3 to 0.5 range. Attenuation in decibels per centimeter ranges from as low as 2.0 for the lightest loading to 70 for the highest loading.

The Eccosorb MF series has a service temperature of 180°C, a density of 1.6 to 4.9 g/cc, a tensile strength of greater than 8,000 lb/in.$^2$, a thermal expansion coefficient of $30\times10^{-6}$/°C, and a weight gain of less than 0.3% when immersed in water for 24 hours.

Emerson & Cuming Microwave Products, Dewey and Almy Chemical Division, W. R. Grace & Co., Canton, Mass. 02021 [386]

**An antistatic solution,** Plastistat 101 is a mixture of cationic quaternary ammonium compounds. It was formulated for use in the medical, optical, electronic, and chemical industries to improve equipment operation, control dust and contamination, reduce hazards of explosion and fire, and improve product quality and usefulness. In addition, materials such as polyethylene, polypropylene, nylon, and polyester can be coated with this solution.

Plastistat 101 is soluble in water, acetone, lower alcohols, and dialcohols. It is provided as a 25:1 concentrate for $65 per gallon in quantities of one to four gallons, $59 in 4- to 40-gallon quantities, and $56.50 for amounts over 40 gallons. For many applications, dilutions of 100:1 can be used.

Plastic Systems Inc., 88 Ellsworth St., Worcester, Mass. 01610 [387]

**A polyimide adhesive** developed for attaching dice and other electrical components to ceramic substrates or metal frames has been designated the SA 100. It is available as a conductive paste with either silver or gold powder and as a nonconductive paste with a thermally conductive ceramic filler and is rated for continuous service at up to 250°C.

The adhesive will cure in 90 minutes at 270°C and is resistant to benzene, xylene, acetone, and methylene chloride. It has a volume resistivity of 0.00012 Ω-cm maximum, a die-shear strength of 6 to 20 lb for a 0.1-by-0.1-cm die, depending on bond line, and a weight gain of less than 0.01% after being immersed in water for 24 hours.

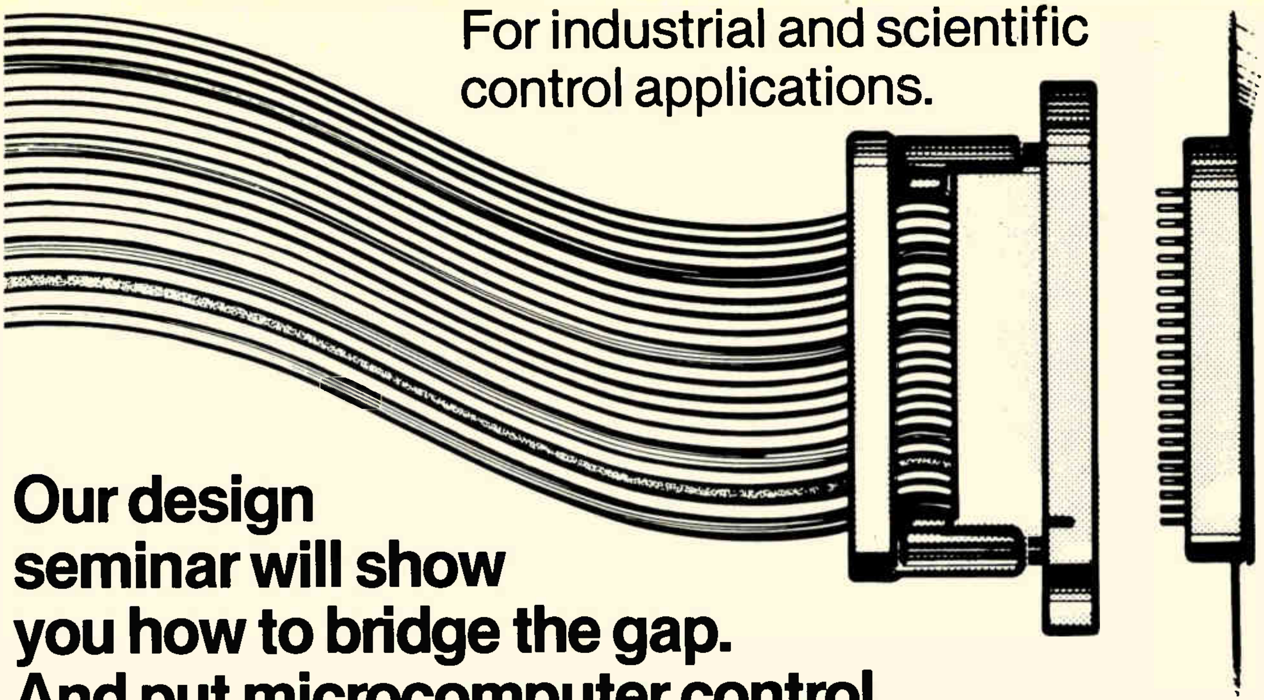
SA 100 adhesive is priced at $50 for 20 g and $100 for 100 g and in volume quantities, 75¢/g.

Zirmex Inc., 2045 North Forbes Blvd., Tucson, Ariz. 85705 [388]

**A gold conductor material,** the series C-5757 paste covers approximately twice the area that is normally covered by comparable gold conductor materials. Only 1 oz of the paste will extend over 500 to 600 in.$^2$ of substrate surface. For easily bondable surfaces with backlit optical densities of over 90%, only a thin layer of the paste (typically 0.2 mils) need be applied to the substrate. It can be used for wire-bonding and for resistor terminations. It permits smooth glass layers to be made for multilayer circuits.

The series C-5757 paste fires to a dense film at temperatures from 850° to 950°C, resolving line widths as small as 0.005 in. It comes in 50- to 300-g quantities at $15.29/g.

Cermalloy Inc., Union Hill Industrial Park, West Conshohocken, Pa. 19428 [389]



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A nominal fee will be charged to cover lunch and course materials. To obtain complete details and reserve a place for yourself, telephone the individual at the seminar location nearest you (see below).

**Agenda**

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- ☐ Demonstration of control capabilities of single-board computers, including AIM 65, RM 65 and AIM 65/40.
  - Software concepts
  - Hardware approaches
  - System solutions
- ☐ Building a system from a single-board computer.
- ☐ Things you need to know/decide in planning your system configuration.
- ☐ CRT and floppy disk controller demonstration.
- ☐ Controlling the software dilemma. You don't have to be a professional programmer to use the power of a microcomputer.
- ☐ We'll talk about BASIC, FORTH*, PL/65 and Pascal.
- ☐ Problems and solutions for typical applications.

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## European Seminar Schedule

| DATE | LOCATION | CONTACT | TELEPHONE NUMBER |
|---|---|---|---|
| Jan 25 | Stockholm, Sweden | Mr. Forsberg | 08-820-280 |
| Jan 27 | Copenhagen, Denmark | Mr. Eyde | 45 6816522 |
| Jan 28 | Oslo, Norway | Mr. Hakimi | 010-472-545-130 |
| Feb 1 | Edinburgh, Scotland | Mr. Lamb | 0592-773902 |
| Feb 3 | Manchester, England | Mr. Davies | (02) 4431 2367 |
| Feb 4 | Brighton, England | Mr. Dale-Smith | 44 (0273) 722155 202949 |
| Feb 5 | London, England | Mr. Mapes | (01) 898 4761 |
| Feb 8 | Milan, Italy | Mr. Cardone | (02) 95.20.551-95.20.651 |
| Feb 10 | Den Haag, Netherlands | Mr. Banse | 015-1349 40 |
| Feb 15 | Paris, France | Mr. Bourveau | 954 9113 |

| DATE | LOCATION | CONTACT | TELEPHONE NUMBER |
|---|---|---|---|
| Feb 15 | Paris, France | Mr. Pogi | (01) 687 1258 |
| Feb 17 | Rome, Italy | Mr. Cardone | (02) 95.20.551-95.20.651 |
| Feb 19 | Zurich, Switzerland | Mr. Affeltranger | 01/44 33 00 |
| Feb 22 | Vienna, Austria | Mr. Chab | 43 (222) 85 86 46 |
| Feb 24 | Munich, Germany | Mr. Rienznek | 30 40 11 |
| Feb 26 | Stuttgart, Germany | Mr. Langer | 49 (07136) 5031-36 |
| Mar 1 | Berlin, Germany | Mr. Langer | 49 (07136) 5031-36 |
| Mar 3 | Dusseldorf, Germany | Mr. Breiden | (0211) 626364-67 |
| Mar 5 | Braunschweig, Germany | Mr. Lang-Nickel | (0531) 314097-99 |

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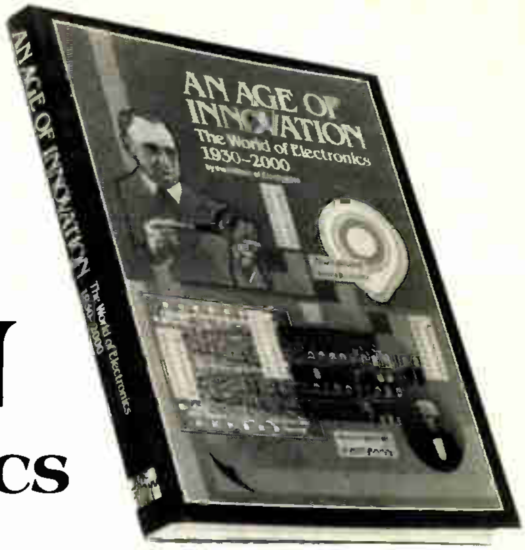


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# Products Newsletter

**16-K static RAMs meet MIL STD 883-B**

Deepening its recent thrust into military semiconductor markets, Mostek Corp. is unveiling a 2-K-by-8-bit static random-access memory fully screened to meet MIL STD 883-B, method 5004. Designated MKB4802, the chip operates over a temperature range of −55° to +125°C. **In orders of 1,000, the 200-ns version costs $54.30 each, and a 120-ns part goes for $65.** The Carrollton, Texas, firm plans to offer a 90-ns chip early next year. A high-reliability commercial-grade version with a −40° to +85°C operating range, the MK14802, is also offered. In quantities of 1,000, it sells for $23.70 each for 200-ns parts and $35.80 for 120-ns devices.

**New firmware ups printer's speed**

Responding to speedy products from competitive printer manufacturers, Dataproducts Corp., Woodland Hills, Calif., will unveil next month an **upgrade of its 900-line/min B-900 band printer to 1,000 lines/min.** The 64-character printer, to be redubbed the B-1000, will be standardized with the configuration used on the firm's B-300 and B-600 models, but with a number of major firmware changes. Pricing, however, will remain $9,932 in single units.

**Enhancement boosts CAD productivity**

Designer Logic, an enhancement for Applicon's very large-scale integration computer-aided design software, is **one of the earliest computer aids to offer VLSI designers features for schematic entry and connectivity-pattern extraction,** boosting productivity tenfold compared with the Burlington, Mass., firm's earlier package. Much of the increase is due to automatic data-base manipulation—changing schematic diagrams, for example, is no longer done by hand. Available in February, Designer Logic will go for $15,000.

**PABX services 254 terminals**

Data traffic management is the forte of the most recent addition to Codex Corp.'s IMS 7000 line of equipment for private automatic branch exchanges, the 7800 electronic switching system. Microprocessor-controlled, the 7800 can accommodate as many as 254 terminals concurrently, **allowing both asynchronous and synchronous communication among users and a number of host computers;** automatic queuing is also available. Although primary routing and control are configured through a cathode-ray-tube console, users can request a specific host or application through their own terminals, according to the Mansfield, Mass., firm. The system also includes automatic redundancy, a fail-safe feature for continuous operation despite hardware failure. Prices vary with configuration, ranging from $42,200 to $83,000.

**Winchester drive holds 160 megabytes**

To satisfy compact system applications that require a lot of data packed into a small space, the model 5350, a 14-in. Winchester drive from Harris Corp.'s Computer Systems division in Fort Lauderdale, Fla., offers an unformatted capacity of 160 megabytes, 144 megabytes formatted. It has a mean time between failures of more than 8,000 h without scheduled maintenance. **The 5350 uses four disks, recording data on five disk surfaces at a density of 680 tracks/in.** It has a 30-ms average seek time and a 1.2-megabyte/s data-transfer rate. Including an input/output controller, the 5350 is priced at $28,300; the model 5351, without the controller, sells for $20,900.

# Career outlook

## Computers: where it's at

Executives who are in the information-systems and data-processing sector will be gratified to know they are in the right place at the right time, or so says an annual survey of senior executive demand. The findings were made by Russell Reynolds Associates Inc., a New York executive-search firm that sent questions last month to the chief executive officers of 1,300 major firms across the U. S. Among other companies, the respondents represent the 1,000 largest industrial corporations, according to Reynolds.

Overall, short-term demand is down, reflecting the recession. "However," the report says, "we see this period as preliminary to a heightened need for senior executives as the economy recovers." Most respondents, some 68%, said they felt that the vast majority of executives hired in 1982 would be filling vacancies rather than occupying newly created slots.

But the outlook for information systems and data processing is comparatively rosy over the short term and even better for the next five years. Some 26% of the respondents declare they will hire more top officials in those areas in 1982; 39% say they will hire about the same number as they did in 1981; 19% believe they will hire fewer.

In the long term the overall picture really brightens. In the 11 categories listed, all of which will experience some demand over the next five years, 58% of the respondents select information systems and data processing, a full nine percentage points ahead of runner-up general management, and 20% more than third-place research and engineering.

As to the subdued demand overall next year for executives, however, 64% name high interest rates as the villain, while 24% point to inflation in general. Yet 11% of the respondents detect a glimmer of hope in the imminent future—the recent Federal tax legislation, they predict, might result in increased hiring; but 65% foresee no such change. ☐

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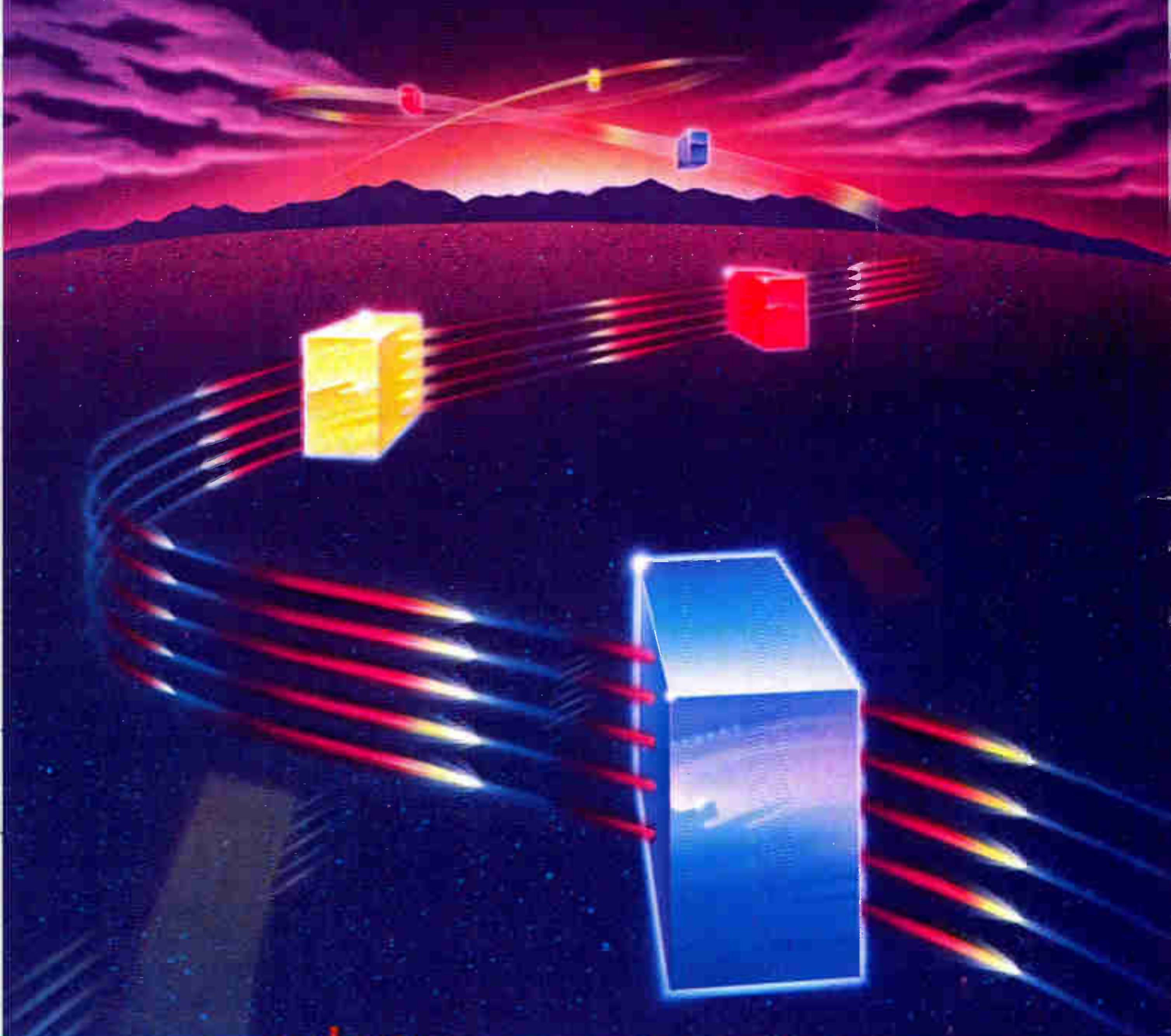

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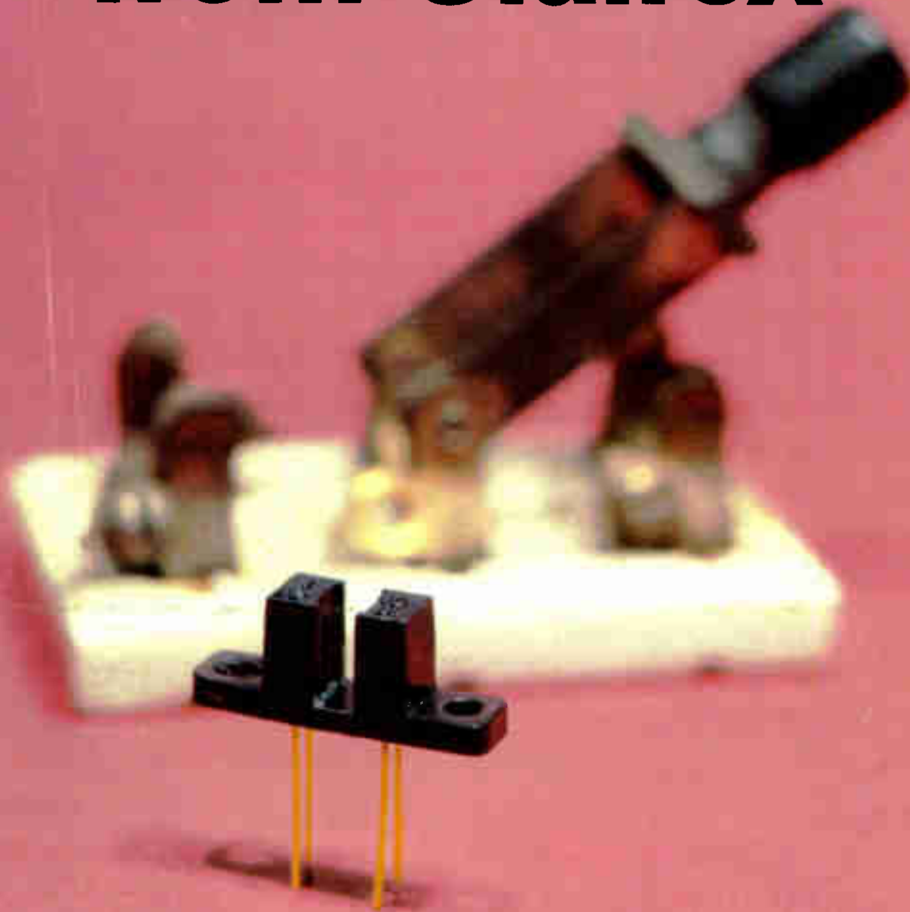

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