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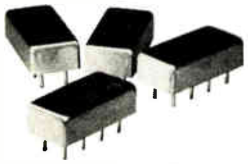
AT-10	10	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W
AT-20	20	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W



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Electronics
The International Magazine of Electronic Technology
Vol. 54, No. 20 • October 6, 1981

103 Technical Articles

A 10-PART SPECIAL REPORT: C-MOS TECHNOLOGY

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Electronics

Highlights

C-MOS flowers, with applications in many areas, 103

Complementary-MOS technology has grown in sophistication to rival n-channel MOS, adding speed and design flexibility to its vaunted low power consumption. As a result, it is being used for very large-scale integrated circuits in a wide variety of applications. The articles in this special issue look at both the technology and the applications.

The cover illustration is by Myers & Noftsinger.

In the next issue . . .

The annual Technology Update . . . *Electronics'* 1981 achievement award.

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IF	DC-500	DC-1000	DC-500	.5-500	DC-600
CONVERSION LOSS, dB					
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total range	8.5	7.0	8.5	9.0	8.5
ISOLATION, dB, L TO R					
lower bandedge	50	50	45	45	50
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For complete specifications and performance curves refer to the 1980-1981 Microwaves Product Data Directory, the Goldbook or EEM.

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Publisher's letter

For the entire technical feature section of an issue to be devoted to a single subject, that subject has got to be an important one. Indeed, our message this issue is that complementary-MOS technology, and the role it will play in many industry segments, has become exceedingly important. In fact, C-MOS is slated to become the dominant technology in the latter part of the decade.

"When you think about it, the issue really isn't devoted to one subject because the 10 articles cut across many segments of the industry," explains Ray Capece, technical managing editor. "What we're trying to show is that the advantages of the C-MOS process—wide supply and temperature range of operation, good noise immunity, and of course, low power consumption—will benefit any equipment it goes into."

The idea for the special issue sprung forth from solid-state editor John Posa last spring. Says John, "In discussing C-MOS with fellow department editors, we found that the process was infiltrating all their areas. It was then that we got together to plan this series of articles." So the staff set out this summer to gather stories that would present a snapshot of C-MOS's status. John, who provided an introduction to the series of articles that begins on page 103, solicited some state-of-the-art 16-K memory articles: a fast static random-access memory from a new start-up company called Integrated Device Technology and a fusible-link programmable read-only memory from Harris. Microsystems and software editor Colin Johnson garnered some equally exciting C-MOS processor stories—Bell Laboratories' 32-bit machine, and a high-performance 16-bit processor from Toshiba built with silicon-on-sapphire technology.

Telecommunications is a natural for C-MOS, and communications and microwave editor Harvey Hindin scored some real coups: from Mostek, one of the first chips to integrate both the codec and its filter, and a switching chip from Mitel that handles a remarkable array of 256 by 256 channels. "The telecommunications area will unquestionably be the first—and probably the largest—segment to use the C-MOS process exclusively," asserts Harvey.

The remainder of the articles are in diverse areas equally suited to C-MOS's characteristics. A single-chip speech synthesizer from Hitachi takes advantage of low power for battery-powered talking equipment; an analog-to-digital converter adds to the foundation of components for low-power data acquisition, which can greatly benefit from C-MOS's analog as well as digital circuit flexibility; an automobile-engine controller needs C-MOS to weather its harsh under-the-hood environment; and finally, a computer work station for the office chooses C-MOS for the bulk of its chips to beat the heat and keep power-supply requirements down.

Let it be said: C-MOS is the new workhorse of the '80s.

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Readers' comments

Disputed delay

To the Editor: Intel's redundancy article in the July 28 issue of *Electronics* ["Equipping a line of memories with spare cells," p. 127] contained a glaring discrepancy that should be brought to the readers' attention. On page 128 of the article, authors Robert Abbott, Kim Kokkonen, Roger Kung, and Ronald Smith state: "Row redundancy does add a 3- to 5-nanosecond stage delay as the decision to use an original or a replacement row is made."

What is not discussed, however, is the effect this has on chip access time. Careful examination of Fig. 2a shows not one, but three stage delays. This clearly adds 9 to 15 ns. to the access time of the part and consequently affects the performance of the device.

Brad Hartman
Inmos Corp.
Colorado Springs, Colo.

■ **Author Kim Kokkonen replies:** *Mr. Hartman does not seem to clearly understand the effects of high-performance H-MOS II transistors on the 2167 redundancy design. The gate delay for H-MOS II driving a fan-out of three is only 0.6 ns. Even for a larger output load, the gate delays are limited to 1 ns with proper driver design.*

The normal-element-disable circuitry in question has been carefully optimized with proper trigger points and native zero-threshold devices to minimize the propagation delay. Simulations, tester characterization, and system level measurements all confirm that the access time delay induced by row redundancy is 3 to 5 ns, as stated earlier. The Inmos technology, with less aggressive scaling and no zero-threshold devices, may not have been able to achieve this result.

We admit that the Inmos column redundancy approach will have 3 to 5 ns less impact on access time than Intel's. However, we believe we have taken a more global approach to redundancy optimization by considering reliability in the equation, as well as die yield and speed.

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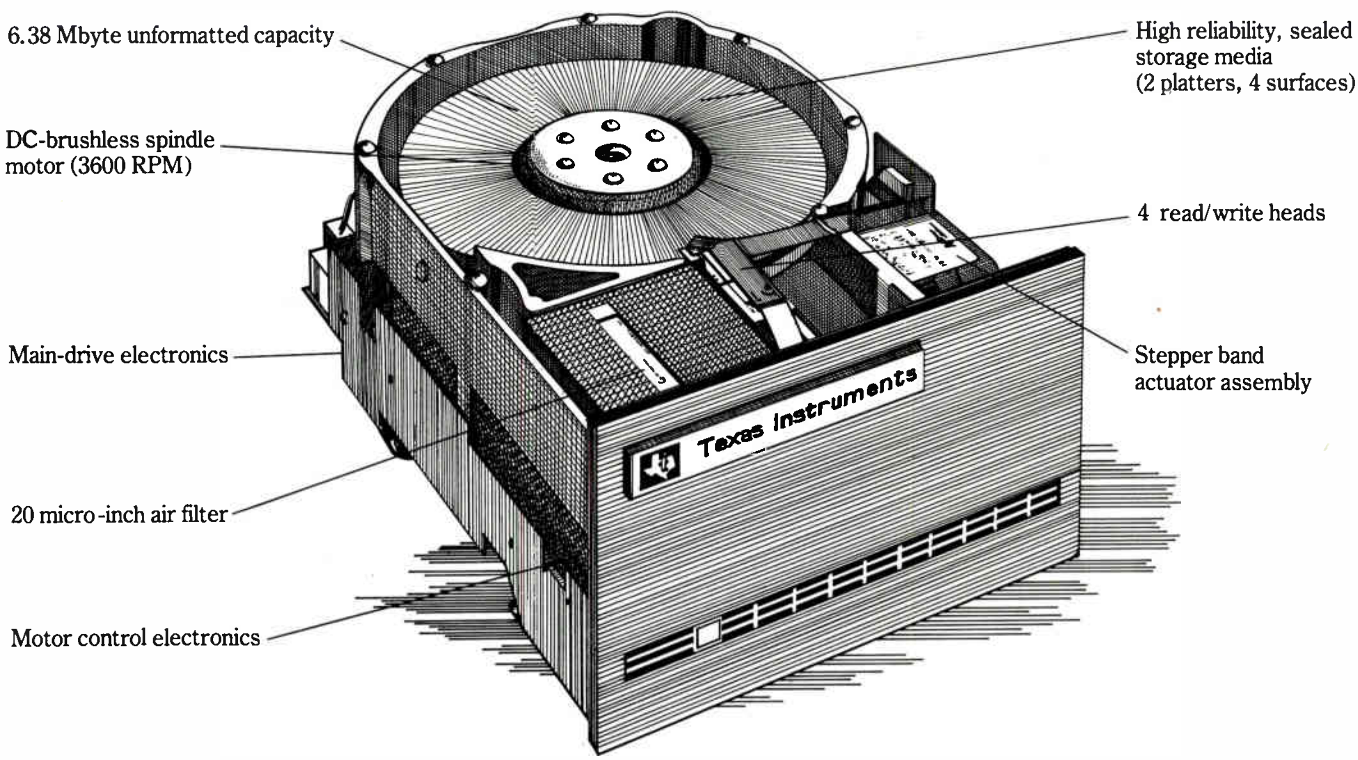

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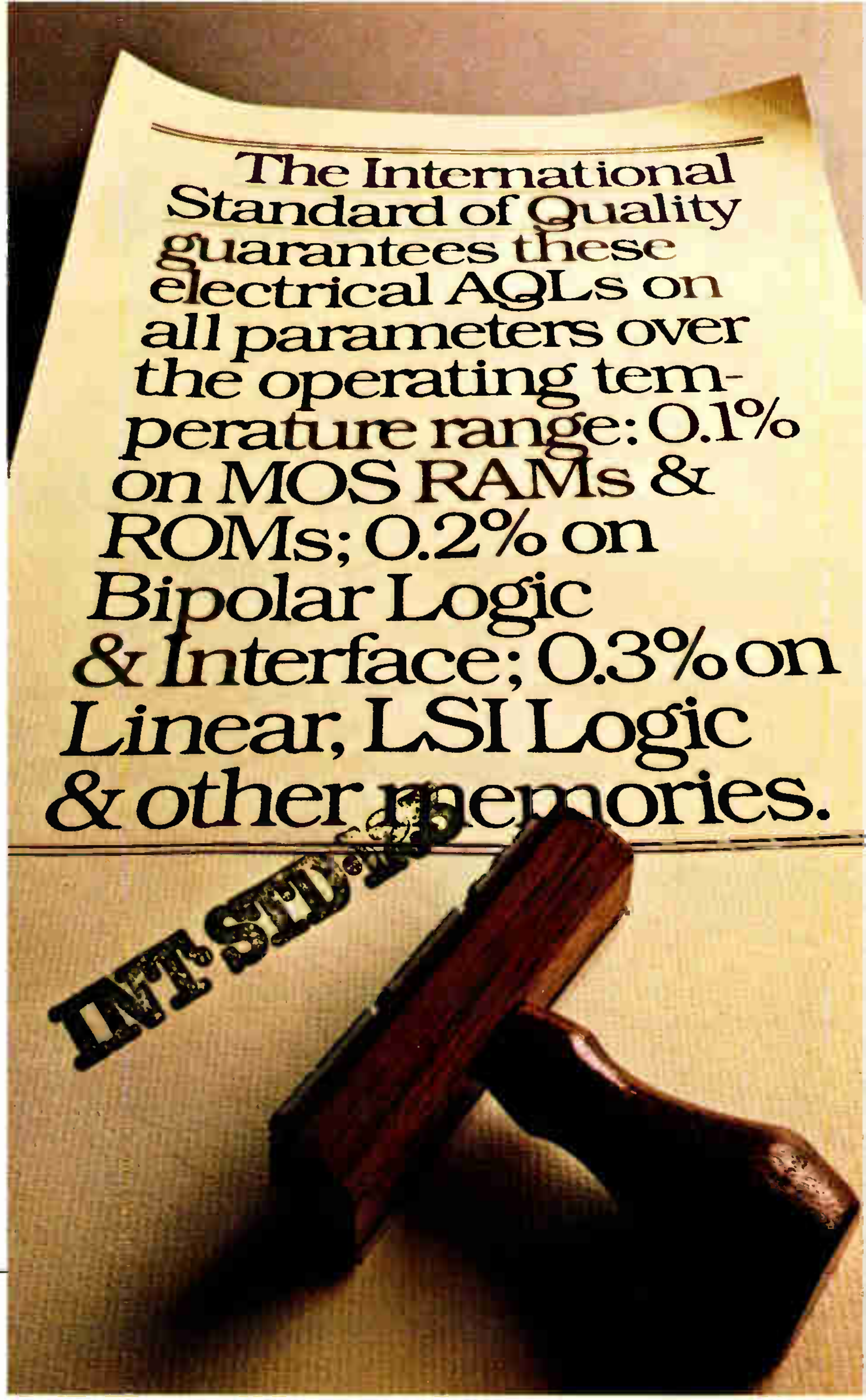

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Readers' comments

improvement in 2167 reliability over a design without these features. We also feel that column redundancy for fast static random-access memories is potentially unreliable unless the faulty columns are fully disconnected from the internal data bus to ensure that column shorts to ground and similar failures will not affect functional cells.

Finally, Intel's use of a higher-capacitance double-polysilicon cell in combination with a polyimide die coat is likely to show significantly lower soft-error rates than devices without these features.

Best estimate

To the Editor: I would like to apply a bit of fine tuning to the opinions attributed to me ("64-K RAM battle is murky," Sept. 8, p. 89) regarding the 64-K random-access memory market. The fault in communication is mine—I was attempting only to point out that various industry estimates for 1981 sales range from a few to the quoted 11 million units. As suggested earlier in my own newsletter, I have qualitatively assessed present 64-K production as lower than Japanese news sources would lead us to believe. The difficulties in estimation are caused by the fact that many of the units manufactured in 1981 are going into Japanese computers without reaching the open market.

Finally, my correctly quoted comment on the lack of precise figures was in no way intended to denigrate Dataquest's estimate. Dataquest is well respected in the industry as a reliable source of memory shipment information and is respected by myself as a worthy competitor.

Mel H. Eklund
Integrated Circuit
Engineering Corp.
Scottsdale, Ariz.

Correction

In "3-d graphics dazzles display conference" (Aug. 25, p. 46), it was stated that the Motorola MC68000 microprocessor was used in Lexidata Corp.'s System 3400 XV7. The 16-bit chip is used in the firm's Graphics System 8000 display terminal.

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People

Goshorn pushes low price with International Robomation

Lawrence Goshorn sees himself as one of the pioneers of the minicomputer industry, having helped bring board-based systems to the forefront with General Automation Inc., a firm he founded 14 years ago. Now Goshorn is again pioneering, this time by forming International Robomation/Intelligence in Carlsbad, Calif., and announcing an industrial robot that will sell for less than $10,000.

"Picture 1961. Robotics is where minis were in that time-frame," says Goshorn, who sees high prices and a lack of competition as the only remaining obstacles to widespread use of robots in factories. To clear these hurdles, Goshorn has priced his pneumatic-powered robot to undercut the $40,000-or-higher price tag usual for U. S.-made robots powered by hydraulics or electric motors.

Robot entrepreneur. Larry Goshorn concentrates on low-priced pneumatic robots and artificial intelligence.

The 48-year-old engineer calls such high-priced robots a case of overkill because they offer tolerances of 0.004 or 0.005 inch and capacities far beyond what's needed for many applications. His new company's robot can heft 50 pounds, about what an average worker will handle, and is accurate to 0.040 in. "This is a narrow approach. We're tuned to become the DEC of the robotics industry," he notes.

Comparisons from his minicomputer roots crop up frequently in Goshorn's conversation. He built General Automation into a $150 million company before being unseated by the board of directors for a variety of reasons, including losses. He says he is now glad to be out of the "established" minicomputer industry and to be in "commando country," as he calls the emerging robotics industry. The move from factory automation at General Automation into robotics was a logical step, which Goshorn had considered briefly while still there, he says.

The new robotics entrepreneur feels he can undercut both the Japanese and American competitors with his prices and approach. The Japanese use dumb robots to control smart machines, he says. (For an overview of Japanese robotic activity, see p. 87.) But IRI's robot utilizes five Motorola 68000 microprocessors, so it provides the intelligence to control a dumb machine at a much lower cost for both the robot and the machinery needed for the task, he notes with satisfaction.

Although IRI is currently designing its first production model and preparing a public offering, the 11-month-old firm also is already heavily involved in artificial intelligence research. Introduction of artificial intelligence products are now set by Goshorn for the 1982 National Computer Conference. "In the mid-1980s, we'll be leaders in AI. By the end of the 1980s it will be booming, and in the 1990s you'll see commercial products," he predicts.

Sevin and Rosen to invest in application start-ups

Semiconductors should surely be the focus when an astute, highly respected securities analyst specializing in the semiconductor industry joins up with the co-founder and longtime chief executive officer of a

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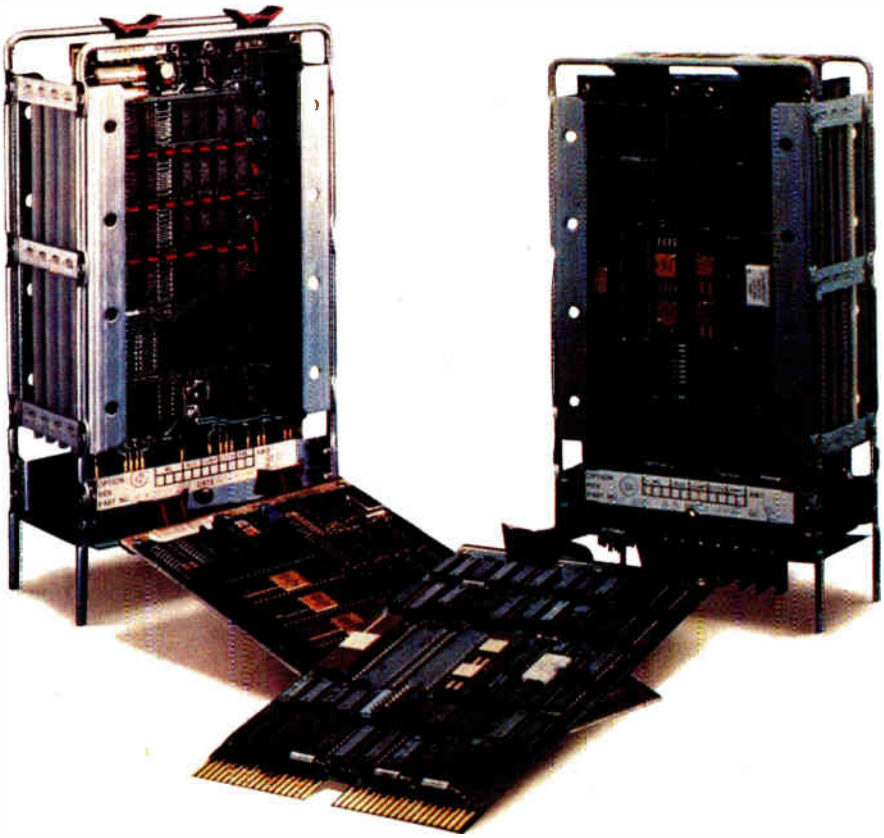

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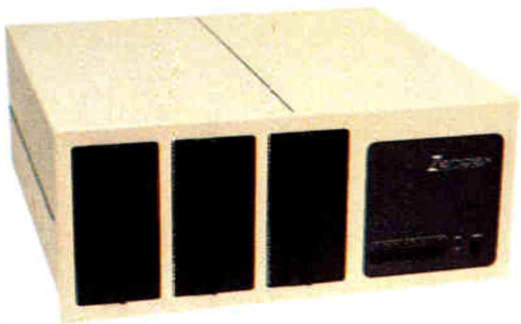

major semiconductor manufacturer as venture-capital partners. But Benjamin M. Rosen, the securities analyst, and L. J. Sevin, who recently left Mostek Corp. after 12 years, do not agree. They intend to invest Sevin Rosen Partners' $25 million fund in start-up ventures involving computer systems, software, telecommunications equipment, industrial controls, office and factory automation, and robotics.

The money was raised from an international group of financial institutions, major corporations, and individual investors, about 30 entities in all. The ventures, according to Rosen, will require far less capital, carry relatively less risk, and offer more attractive return than semiconductor start-ups. "The development of high-performance microprocessors and advances in large-scale integration have created a tremendous number of opportunities for businesses founded on applications. In particular, we'll be looking for projects aimed at solving problems in specific market areas. One example might be a system package for the auto parts industry."

Rosen, 48, is president of Rosen Research Inc., a publishing and technology consulting firm. Before that he was a vice president and senior electronics analyst at Morgan Stanley & Co. He holds a bachelor of science degree in electrical engineering from the California Institute of Technology, a master of science degree in the same field from Stanford University, and a master's degree in business administration from Columbia University.

Sevin, 51, resigned as chairman and chief executive officer of Mostek Corp. after it was acquired by United Technologies Corp. in 1980. Before that he spearheaded Texas Instruments Inc.'s MOS integrated-circuit activities.

Sevin Rosen Partners will maintain its principal offices in New York and Dallas. Sevin will operate from Texas, where he says native venture capitalists are rare birds. "There's a lot of talent down here, however," he says. "Texas is attracting people from both coasts." ☐

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measurement and control systems
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Circle 17 on reader service card

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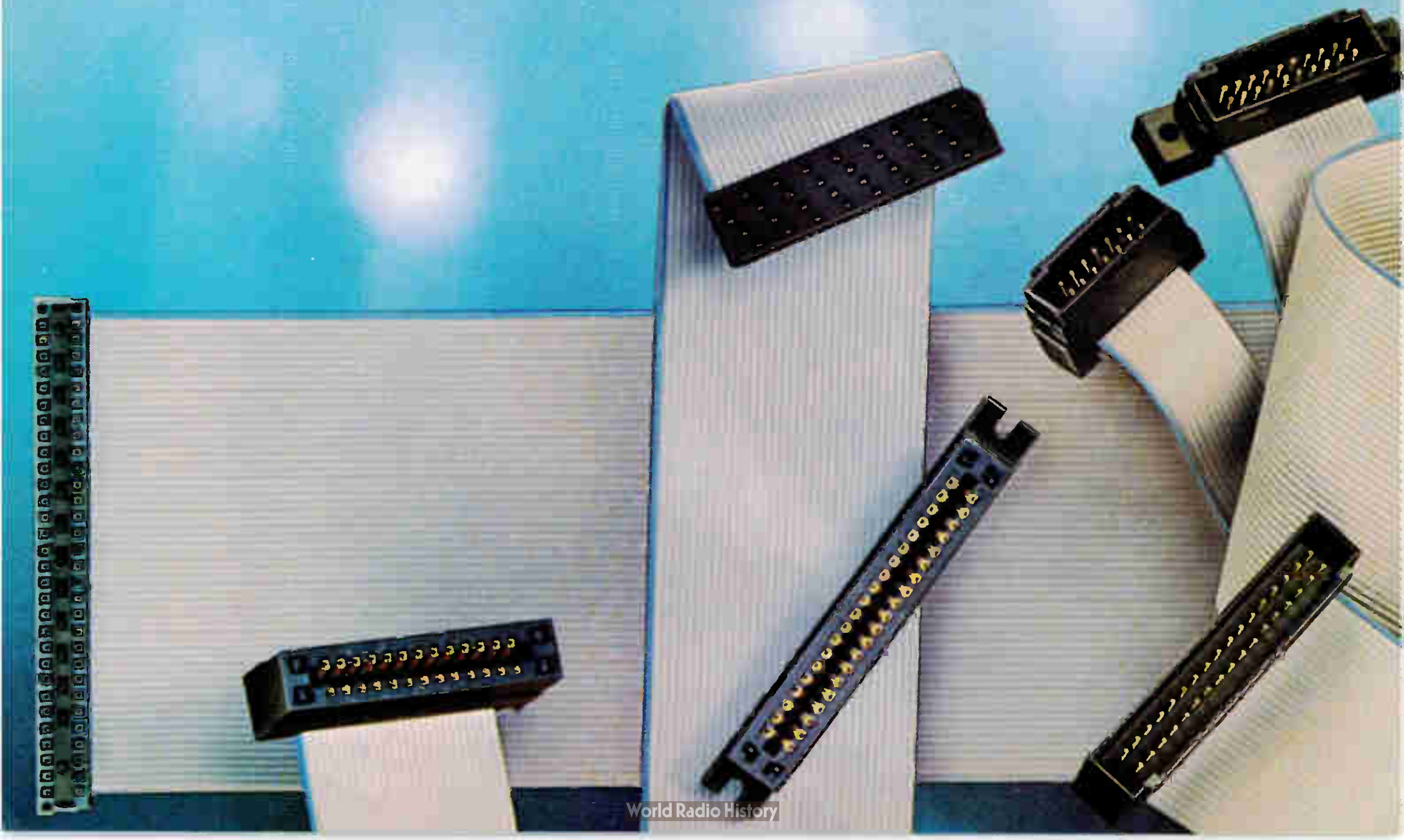
Now you can terminate AMP Latch connectors at the rate of 450 an hour. That's more than double the speed of what you can do with other ribbon cable connectors.

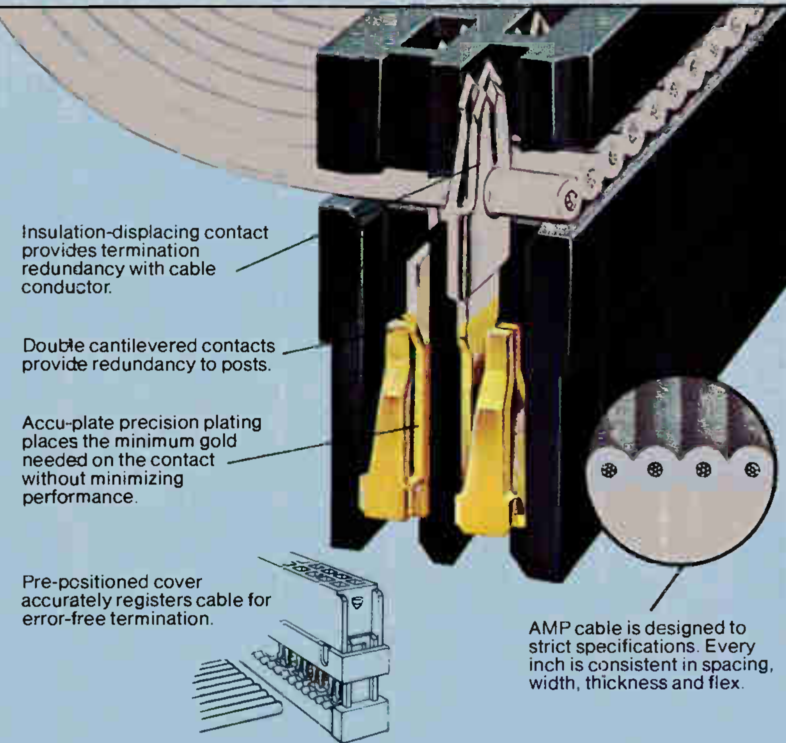
Our new semi-automatic tool makes it happen. It precision feeds, positions and terminates preassembled receptacle connectors in one step. Our precision cable further minimizes rejects, because it's designed and manufactured to strict dimensional specs. And our complete range of fully shrouded headers includes a positive locking type you can squeeze-to-release with one hand.

With these continued advancements and our wide mix of connectors, the AMP Latch system is more productive than ever.



AMP Facts

Wire Types: Small-gauge solid or stranded discrete, plus flat ribbon, woven ribbon and other types of flat cable with round conductors on .050" centers.
Size: 10 through 60 positions.
Connector Types: Wide variety of cable-to-cable, card edge, DIP and receptacle connectors available.
Electrical Current Rating: 1 ampere (continuous).
Operating Temperature Range: −55°C to +105°C
Dielectric Withstanding Voltage: 500 volts RMS.
Tooling: Pneumatic, manual and semi-automatic bench termination machines.



For a free sample, call the AMP Latch Information Desk at (717) 780-8400.

AMP Incorporated, Harrisburg, PA 17105

AMP means productivity.

Local segments. Fast redraw. Refresh dynamics.

Why work harder, when you can work faster?

The power you've always wanted is right before your eyes. The new Tektronix 4114 combines host computer power with unprecedented local intelligence and transmission speed. It combines the unequaled resolution of 19-inch storage tube with the capacity to construct, store and manipulate graphic elements locally, without transmission from the host. It includes 3000 short vectors of local refresh and new fast redraw.

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Optional enhanced version keeps refreshed information in high-contrast color. A particularly convenient, easy-viewing feature in high-density graphics environments.

You can expand memory to a full megabyte, and add optional integrated single or dual flexible disk mass storage. You can consolidate and reorganize files, display directly from disk, or send data from disk to plotter while you turn the terminal to other tasks.

With our PLOT 10 Interactive Graphics Library (IGL), you enjoy fast start-up, easy maintenance, CPU and terminal independence. PLOT 10 IGL is the world's most popular implementation of the 1979 ANSI proposal for a computer graphics software standard.

Your local Tektronix sales engineer can show you the 4114 in action. Or call toll-free, 1-800-547-6711 (in Oregon, 1-800-452-6773) for complete product details.

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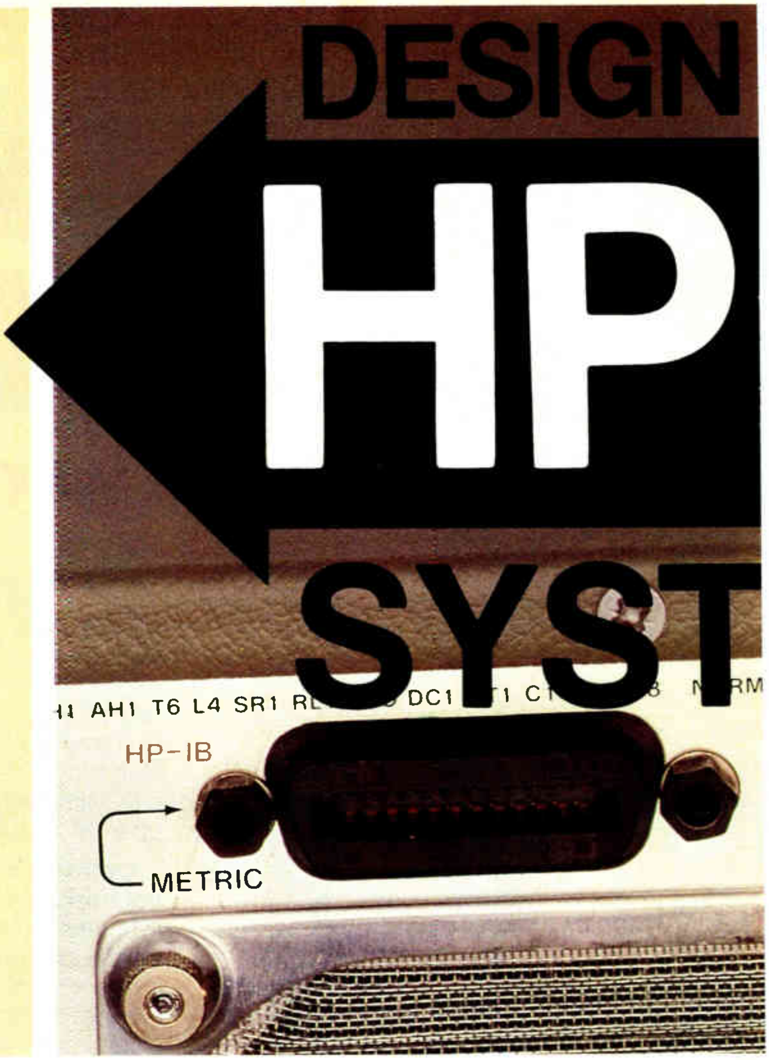
This symbol means faster measurement system development. . .



The familiar HP-IB (Hewlett-Packard Interface Bus) symbol is HP's way of identifying instruments and computers that conform to the IEEE-488 standard. But it means much more than just bus architecture and system compatibility. The HP-IB symbol also stands for the documentation and support that helps you get a measurement system operational in weeks instead of months.

Five reasons why you'll save time and effort.

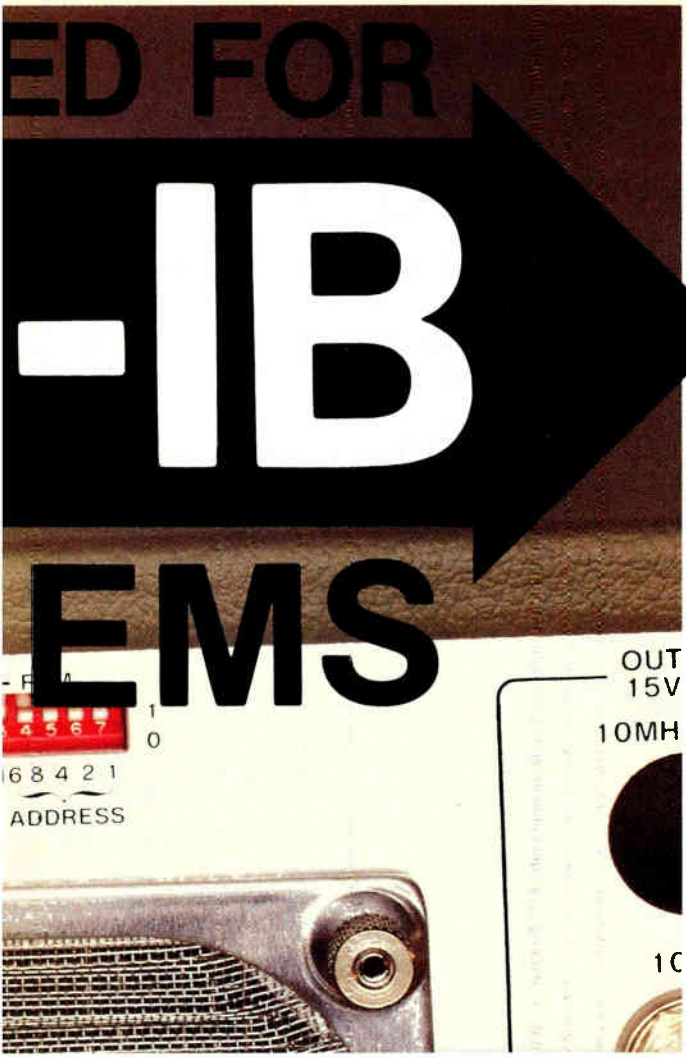
Choose HP when you need a measurement system and you get these advantages: 1) All devices and all documentation come from a single source which means consistency in design and documentation. 2) Every member of the HP-IB family of instruments and computers — over 140 in all — is designed for and tested to rigid HP-IB standards of compatibility. 3) Just as important, every HP-IB device comes with complete and comprehensive documentation that's easy to follow and consistent in its approach to implementation. You'll receive service manuals and operating manuals that typically include a guide to the implementation of computer based systems. 4) You can choose from more than 100 HP application notes. Many of these will teach you how to accomplish specific measurements in conjunction with the controlling computer. Software examples are included in a number of these to help you get to a solution even faster. In fact, one of these examples may be just what you need for your exact application. And many HP application notes list the results of performance tests to help you verify proper system operation. 5) HP also offers training, system engineering support and on-site service . . . assistance from start to finish. But these aren't the only reasons HP is the logical choice for measurement system development.

Over ten years of experience to call on.

When you design and build a measurement system, you can have the confidence of working with the company that was there when the need for a standard was realized. HP invented the 3-wire handshake technique and ever since then we've been designing and building HP-IB compatible components. By choosing an HP instrument or computer, you get the benefit of over 10 years experience in interface bus architecture, and how it can best be implemented.

Choose from a wide variety of computers.

With more than 140 different HP-IB instruments and computers to choose from, you can configure the measurement system that's just right for your application.



because it stands for system documentation and support on more than 140 HP-IB instruments and computers.

For your computing controller, you can choose from among the seven members of HP's powerful, flexible 1000 series family. Or you can select one of five friendly and flexible desktop computers. All HP computers have powerful, high-level languages that make it easy for you to write application programs.

Sticking with you.

HP offers all "Designed for Systems" devices with post-warranty support you can count on. You can continue this beyond the normal warranty period with an HP Maintenance Agreement. That means you'll enjoy yearly fixed cost, regularly scheduled preventive maintenance, priority response, and even more.

Meet the HP-IB family.

To find out how HP-IB compatible instruments and controllers can speed you to a faster system solution, send for our free brochure, "Do your own system design in weeks, instead of months." Just write: Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

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080/21

Circle 23 on reader service card

Editorial

Laissez-faire won't work in telecommunications

"You are not my flock and I am not your shepherd." That judgment, delivered by Chairman of the Federal Communications Commission Mark Fowler to a meeting of radio and television broadcasters at September's end, applies just as aptly to his view of the telecommunications industry in America. It is a pronouncement that troubles almost everyone in the telecommunications equipment and services industries, except American Telephone & Telegraph Co. and Japan's eager equipment exporters.

No one disputes Fowler's goal of substituting free and fair competition for FCC regulation. What AT&T's competitors do challenge is his method of getting there without regard for what one wag has called AT&T's ability to "reach out and crush someone."

That challenge now has the support of the General Accounting Office. As the investigative arm of Congress, the GAO has just completed a two-year study in depth of legislative and regulatory actions that it says are needed for the changing domestic telecommunications industry. Many of its conclusions support the fears of AT&T's competitors.

The FCC's second Computer Inquiry decision in 1980 is but one example. Scheduled for implementation next March, it would let AT&T compete in new unregulated markets for information-processing equipment and services by means of a subsidiary, instead of spinning off a separate corporation that would prevent AT&T cross-subsidization. The FCC approach, says GAO, "does not go far enough in providing for organizational restructuring and separation conditions. Further, the commission has moved too quickly . . . before many essential costing, accounting, and depreciation problems have been resolved."

The GAO also recommends in its 219-page study that the Congress amend the Communications Act to require the FCC to "rely on competition to the maximum extent possible," while permitting it to exempt from any or all regulations those companies whose lack of market power precludes their domination of a market. Thus, concludes GAO, "the Commission could then focus its resources on improving the regulation of those carriers whose market dominance requires continued regulation." Those recommendations seem eminently sensible—as does another that would have the FCC create "an industry analysis section" of specialists to monitor the common-carrier industry structure.

As the FCC's Common Carrier Bureau now stands, its staff of 300 contains but 30 accountants to audit the Bell System and everyone else. And what about staff to implement the Computer Inquiry II ruling? It recently numbered four persons, says an FCC source, though two now perform "other functions." That, indeed, is deregulation.

Nevertheless, chairman Fowler says he has "a plan," even though he has been on the job less than five months. That statement before a joint meeting of two House Energy and Commerce subcommittees on telecommunications seemed to surprise FCC Commissioner Joseph Fogarty, who interjected that he has been waiting two years for such a plan and has yet to see one.

If chairman Fowler's plan is nothing more than to reject the role of shepherd and desert the flock, that will leave AT&T virtually uncontrolled. That is not good enough, of course. The telecommunications industry is changing rapidly. Many innovative U. S. companies, some new and small, must not be set up as lambs for slaughter. Letting AT&T compete in new and unregulated markets is desirable only if the Congress establishes sufficient safeguards to guarantee that such competition will be fair. To achieve that goal, it would do well to read its GAO recommendations carefully and then act, as the law requires, in the public interest.

Standard, yes. But all STD BUS cards are not alike.

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Pro-Log cards use only proven, industry-standard parts. So you can always count on availability and consistent performance.

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Choose Z80, 8085 or 6800 CPU cards. Add the memory cards you need. Support them with digital or industrial I/O cards, peripheral interface and utility cards.

When you're ready to expand or change your system, just add or swap cards. Simple.

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Pro-Log cards are backed by a 2-year warranty.

We're proud of the high quality of our STD 7000 cards and back it with a two-year parts-and-labor warranty—the longest in the industry.

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Our customers are using Pro-Log STD 7000 cards in a multitude of applications . . . from earthquake monitors to electronic games, from automobiles to missiles.

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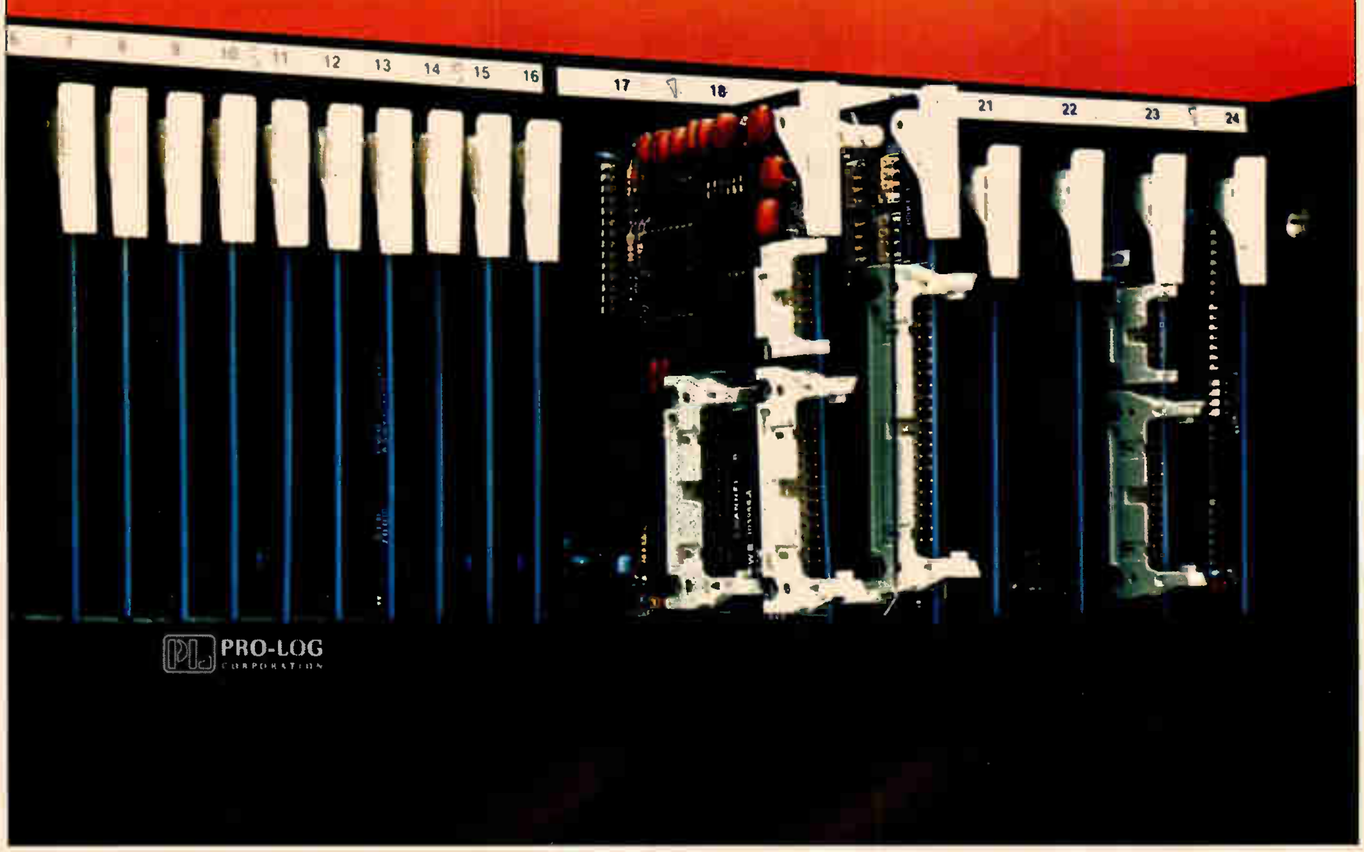

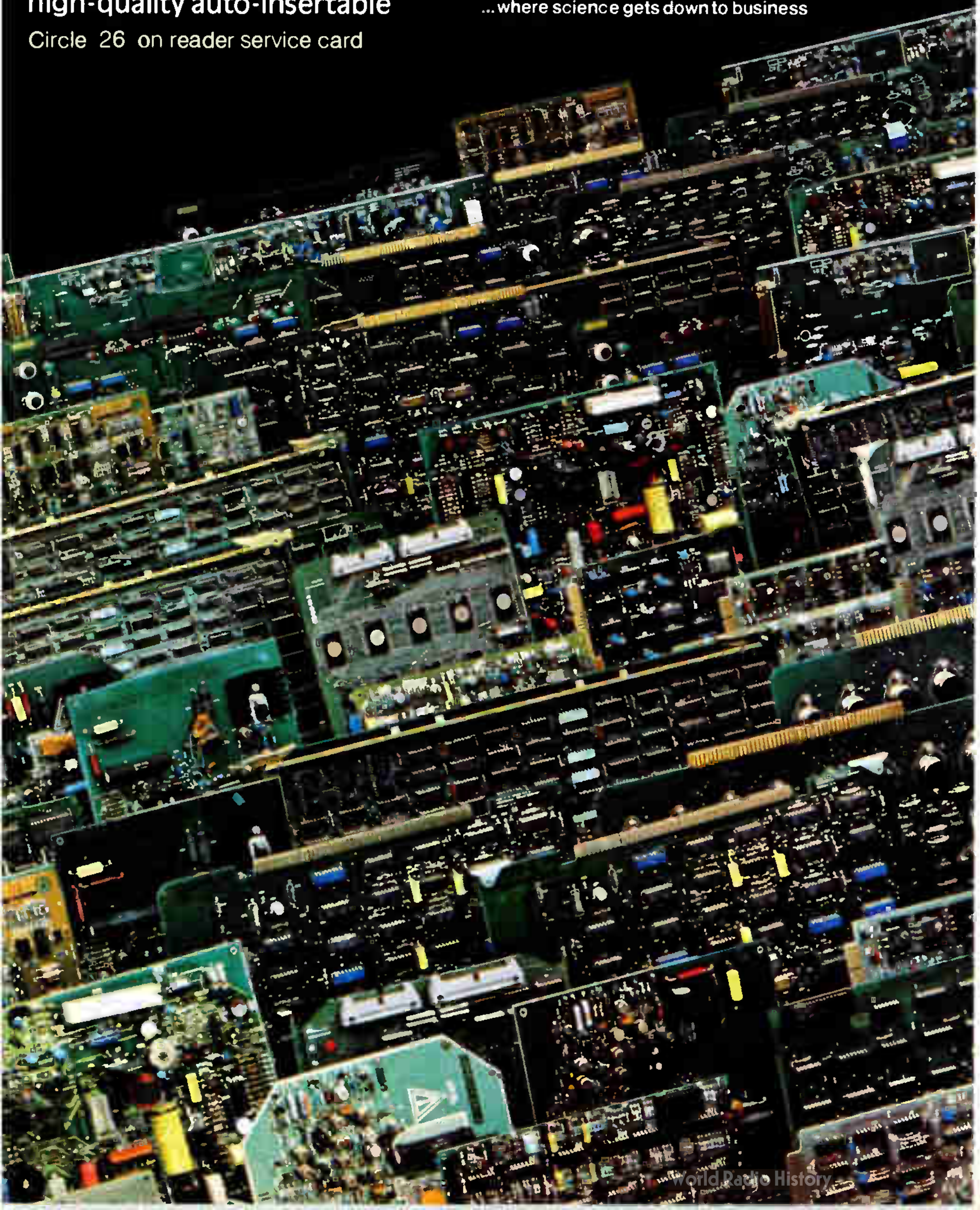

Meetings

1981 International Test Conference—Cherry Hill '81, IEEE (Doris Thomas, P. O. Box 371, Cedar Knolls, N. J. 07927), Franklin Plaza Hotel, Philadelphia, Oct. 27–29.

Gallium Arsenide Integrated Circuit Symposium, IEEE (Varley L. Wrick, Westinghouse Research and Development Center, 1310 Beulah Rd., Pittsburgh, Pa. 15235), Town and Country Hotel, San Diego, Calif., Oct. 27–29.

15th Asilomar Conference on Circuits, Systems, and Computers, IEEE (Harry Hayman, P. O. Box 639, Silver Spring, Md. 20901), Asilomar Conference Center, Pacific Grove, Calif., Nov. 9–11.

Autofact III—Conference and Exposition on the Automated, Integrated Factory, Society of Manufacturing Engineers (P. O. Box 930, Dearborn, Mich. 48128), Cobo Hall, Detroit, Nov. 9–12.

IECI '81—International Conference on Industrial, Control and Instrumentation Applications of Mini- and Microcomputers, IEEE (H. Troy Nagle Jr., Department of Electrical Engineering, Auburn University, Auburn, Ala. 36830), Hyatt Regency Hotel, San Francisco, Nov. 9–13.

Midcon/81, IEEE (Electronic Conventions Inc., 999 N. Sepulveda Blvd., El Segundo, Calif. 90245), Hyatt Regency O'Hare Hotel, Chicago, Nov. 10–12.

Seminars

***Electronics* magazine** has scheduled a series of seminars for engineers and managers running through January 1982. Topics include microprocessor design, single-chip microcomputers, power amplifier design, speech recognition and synthesis, and digital filters. They are given at cities that include New York, Chicago, Boston, Atlanta, and Toronto. For information write to McGraw-Hill Seminar Center, 305 Madison Ave., Room 3112, New York, N. Y. 10017, or phone (212) 687-9211.

Wouldn't it be great if every kind of keyboard had our kind of performance?

SC Series Capacitance Membrane Keyboard

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Now they do.

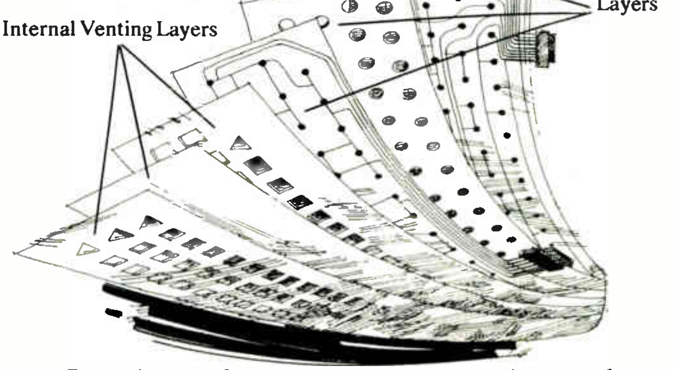
Until now, getting a keyboard at the price you needed could have meant giving up the kind of performance you wanted.

But not anymore.

Because, with the introduction of three new membrane keyboards, MICRO SWITCH has become the world's only full-line supplier of reliable keyboards. We offer a high-performance and cost-effective solution for virtually any application.

Now, in addition to our time-proven Hall effect offerings, you can specify MICRO SWITCH SC Series full-travel capacitance membrane or CT Series contact membrane keyboards, and KD Series touch panel membrane keyboards.

Whatever type of seal you need, all you have to do is ask. The capacitance membrane units are the world's only capacitance keyboards with all the benefits of membrane sealing. And we're the first to solve the venting problems associated with previous membrane designs. Both our capacitance membranes and contact membranes are internally vented to maintain their seal while preventing switch collapse due to air pressure or temperature changes. And for especially severe environments, the touch panel keyboards give the added feature of panel sealing.



It's those features, among others, that make these new keyboards more reliable than other capacitance and hard-contact designs.

And because all three new keyboards have been designed with traditional MICRO SWITCH quality and reliability, each carries a 1% Acceptable Quality Level and 2-year warranty.

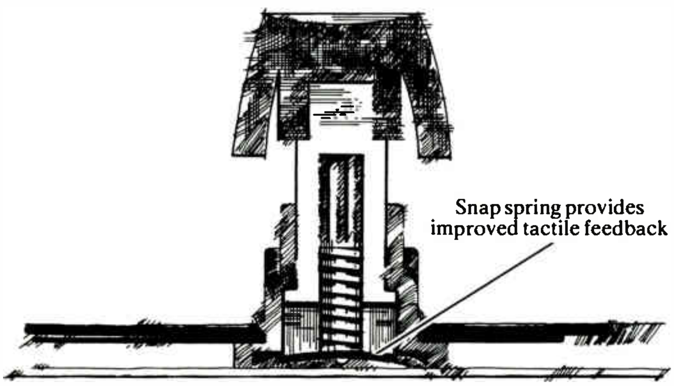
Now any combination of keyboard features you can name can have the MICRO SWITCH name on it.

Now your keyboard specifications are only limited by what you want. Not by what you can get.

Our full-travel series, for example, are available in a wide variety of keyboard configurations, with a choice of over 40,000 legends.

Because legends are screened on our touch panel designs, the graphic possibilities are endless. And, we can combine full-travel and touch panel actuation in a single assembly, featuring either capacitive or hard contact technology.

We make it easier to comply with European standards, because our full-travel membrane designs are available in low-profile versions to meet world requirements.



And, the actuator module for the full-travel membrane keyboards helps achieve new levels of tactile feedback and operator satisfaction.

So you can come to MICRO SWITCH for the keyboard technology, travel, actuation, sealing, appearance, profile, electronics, and special features you need.

And get them all – backed with the experience and full application support that's been a MICRO SWITCH tradition.

Being able to design a keyboard to fit any application is important. But doing it to fit any operator is imperative.

It's important to understand that half of any keyboard application is a human being. There's probably no keyboard manufacturer who understands that better than MICRO SWITCH.

Our unique human factors research—an intensive, on-going program for over 20 years—has given us the tools to develop industry standards for key speeds and multi-key roll-over; tactile, visual, and audible feedback; and various keytop shapes, spacing, configurations and travel. We're continually improving the man/machine interface.

This human factors research is part of

what makes our keyboards unique. And it's part of every keyboard we make.

Instead of resting on our laurels, we're relying on our research.

Being able to add state-of-the-art capacitance membrane, contact membrane, and touch panel keyboard types to our Hall effect offerings is the result of extensive planning, research and testing.

But it's only the beginning.

Each of these keyboard types will be continually subjected to the refinements growing from our human factors research, customer feedback, and our unmatched R&D facilities which include backup by our Honeywell corporate facilities.

Also, every keyboard customer benefits from a manufacturing capability that stands unmatched: it's large enough to handle the most extensive order; responsive enough to give the modest order the same kind of intensive, individualized and quality-conscious attention.

All of these efforts are to make sure that, as your keyboard needs change and grow, you'll always have the choice of a progressive alternative with one unchanging feature: the MICRO SWITCH name. With all the performance that name implies.

For more information on our keyboard technologies, call 815-235-6600. Or write, MICRO SWITCH, the Keyboard Consultants, Freeport, IL 61032.

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BIOMATION K101-D

BREAKTHROUGH

The most powerful general purpose logic analyzer you can buy for the years ahead.

It's here. Biomation K101-D. The first logic analyzer to combine high-speed 50 MHz data and 100 MHz time domain capabilities with advanced 48-channel recording. With enough powerful extras to demolish your toughest hardware/ software integration problems—even on the most complex multiplexed microprocessor.

Fast, accurate software debugging.
With its 50 MHz clock rate, 48-channel recording and 16 triggering levels, the K101-D isolates software bugs faster and more precisely than ever before. Sophisticated disassembly firmware generates precise mnemonics that cut analyzing time. And 12 external clocks (AND or OR) let you demultiplex 16-bit microprocessors, 16- and 32-bit minicomputers and bit-slice processors.

100 MHz high-speed hardware analysis.
The K101-D's advanced high-performance hybrid probes let you capture glitches as narrow as 5 ns. And, with 48-channel recording, 515-word memory and 16-level triggering, you'll trap the data you need. The convenient display formatting and expansion simplify analysis.

Call now for a free demo.
See for yourself why the K101-D is a breakthrough in logic analyzers for the years ahead. For a demonstration or a copy of our detailed product brochure, write Gould Inc., Biomation Operation, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For fastest response, call 408-988-6800.

For powerful software debugging, K101-D data domain capabilities include disassembly, 50 MHz clocking, 48-channel recording, 12 external clocks, 515-word memory, demultiplexing, 16-level trace control for triggering, 6 display code formats, and reference memory.

For powerful hardware debugging, K101-D time domain capabilities include 100 MHz clocking, 48-channel recording, 515-word memory, 5-ns glitch capture, 16-level triggering, channel labeling, new high-performance probe design, as well as horizontal and vertical display expansion for easy reading.

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State of the Mind Interconnect Systems

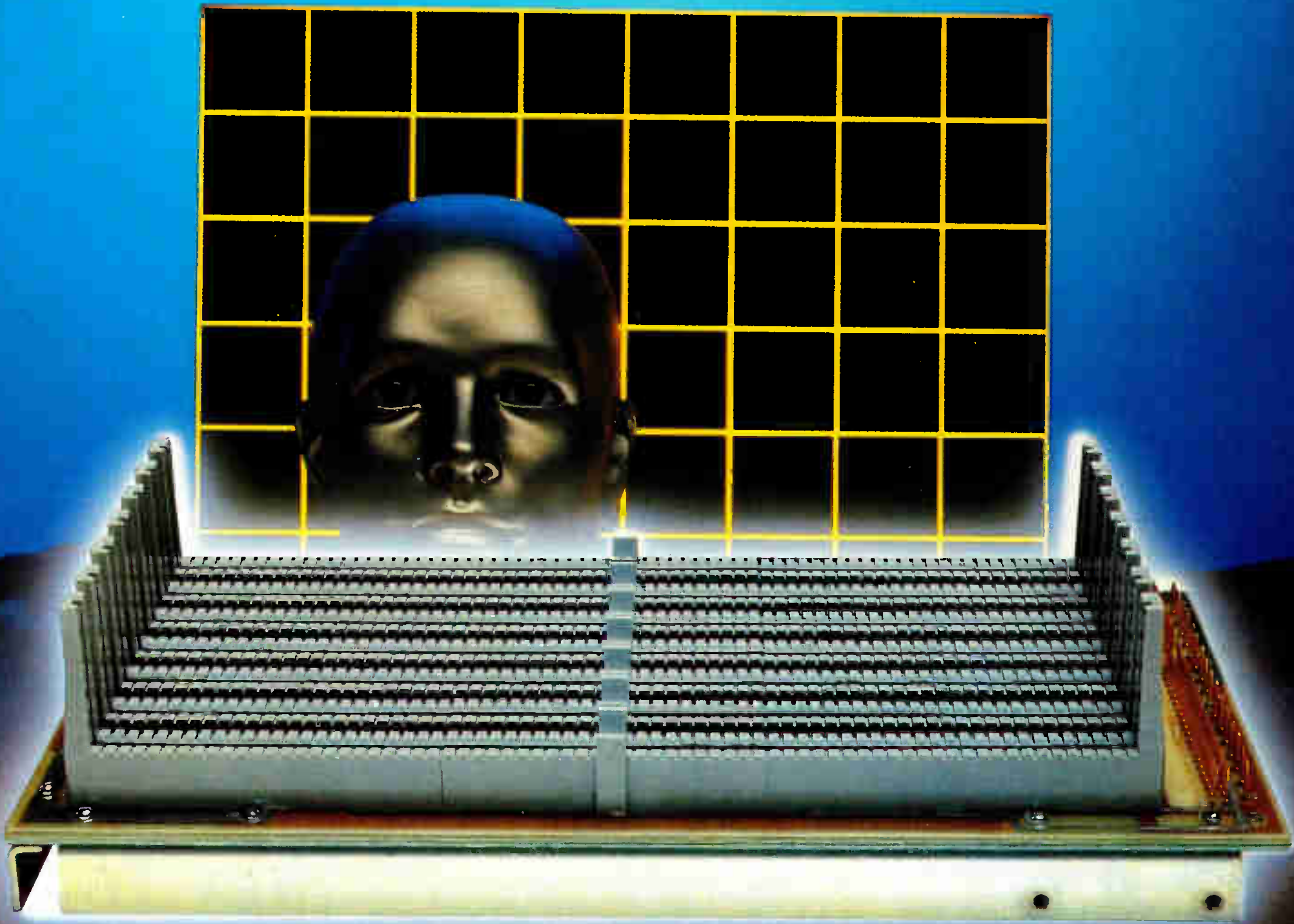
What the mind conceives, Elfab converts to press-fit.
Six layers of circuitry held together with high force solderless, press-fit contacts provide the density needed in this sophisticated computer backplane. Via or pass-thru holes, not possible with laminated assemblies, allow plane to plane access with no loss in density.

Product innovations like this have made Elfab's press-fit systems accepted worldwide. Over the past decade, Elfab's press-fit technology has offered design engineers the ability to go from "State-of-the-Mind" to state-of-the-art in solderless interconnects. Today, we are tooled on more contact styles, more connector types, and more board configurations than any other press-fit supplier.

Hybrid Systems for Thought
Solid pin (non-compliant) press-fit, by totally eliminating solder, has given the designer complete freedom to use both circuit etch and wire wrap tails in a single system.

The unique ability to use wire wrap contacts with a stack of copper bus planes, two-sided boards, or impedance controlled multilayer boards, combines the best of three technologies. Multilayer, metal plane, and wire wrap technologies in one solderless hydrid system.

Integrated Manufacturing That Puts Your Mind At Ease.
Elfab's vertically integrated manufacturing facility assumes complete responsibility for reliability and integrity of the total system. From contact machining to select gold plating, from injection molding of plastic parts to complete state-of-the-art multilayer production and complete product assembly and electrical testing.



ELFAB

Where press-fit makes state of the mind . . . state-of-the-art

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Circle [illegible]2 on reader service card

Intelligent tester mixes three functions

With Interface Technology Inc.'s new three-function RS-4000, the move continues toward intelligent, multifunction instrumentation [*Electronics*, Sept. 8, p. 96]. The San Dimas, Calif., firm's tester combines the functions of **digital word generator, comparator, and logic data recorder.** Slated to bow later this month at the Cherry Hill '81 International Test Conference in Philadelphia, the unit is based on a bit-slice microprocessor with a 200-ns instruction-execution time. It can generate, test, and record data on 16 to 512 channels simultaneously at up to 20 million 16-bit words per second. Base-priced at $21,500, the RS-4000 should serve both as a benchtop tester and as a subsystem in automatic test equipment.

Danelcor readies HEP, termed most powerful scientific computer

Danelcor Inc. of Denver, Colo., is about to deliver its first HEP-I 64-bit supercomputer, a system said to be several times more powerful than either the Control Data Cyber 205 or the Cray-1. HEP, for heterogeneous element processor [*Electronics*, Oct. 23, 1980, p. 202] is an ultrafast, multiple-instruction, multi–data-stream, parallel-processing system. The modular, field-expandable HEP is based on an emitter-coupled-logic central processing unit capable of executing 10 million scalar or vector instructions per second. **It will be available in configurations of 1 to 16 such processors and as many as 128 1-megabyte main memory banks,** making possible system speeds of 160 million instructions per second. In comparison, the Cyber 205 reaches 50 scalar MIPs, and the Cray-1 significantly fewer. A one-module HEP would cost only about $1.7 million.

32-bit multiprocessor is fail-safe, includes networking

Watch for announcement late this year of what could be the most powerful fail-safe computer yet developed. Due from Stratus Computer Inc. of Natick, Mass., the new 32-bit system offers several levels of redundancy, so that multiple hardware failures can occur without affecting processing. Present continuous-processing systems typically catch failures only after one or more machine cycles, after which degraded data must be purged and processing begun again; **such recovery, is said to be unnecessary with the new system, which cuts off bad modules before data is lost.** From an initial configuration claimed to be about half the price of competing fail-safe computers, the Stratus computer expands to become a multiprocessor that includes networking, performing tens of millions of operations per second. Deliveries are due early next year.

Signetics, Honeywell to sign gate-array technology exchange

A technology exchange and mutual second-sourcing agreement to be announced later this month between Signetics Corp., Sunnyvale, Calif., and Honeywell, Inc., Minneapolis, could result in some Honeywell integrated-circuit technology reaching the market through Signetics—a Philips subsidiary. The agreement covers **integrated Schottky logic (ISL) gate arrays.** Both firms are working on new-generation oxide-isolated arrays with up to 2,000 gates and delays as low as 1 to 2 ns.

Processors tailored to Pro IV software

Minicomputer maker Microdata Corp. of Irvine, Calif., is racing to be first to sell a system specifically designed for Pro IV software. Los Angeles–based C. Itoh Electronics Inc. should follow shortly. Pro IV, which combines software generation and data processing to speed programming by end users, originated with Data Technical Analysts Inc. of

Honolulu [*Electronics*, April 7, p. 39]. Microdata's computer should start at $100,000, and C. Itoh's, to be made by Hitachi, at $20,000.

Written in C, planning software supports a variety of computers

A C-language master program will soon start spinning off business and engineering planning packages for diverse computers. Supercomp-20 will be **available for Unix-based and Digital Equipment Corp.'s VAX-series computers** by year's end, says Access Technology Inc., Wellesley, Mass. Packages for the IBM 360/370, DEC PDP-11, HP 1000, and several Honeywell and Univac computers will follow. Licenses are $1,000 to $8,000, the company says.

IBM Personal Computer to be in short supply

Industry insiders believe that the supply of IBM Personal Computers will fall short of demand when the machines go on sale this month—only 15,000 have been produced, they say. What's more, the single board is said to use a great deal of small-scale integration and almost no large-scale integration outside of the 8088 and 8087 processors and the 16-K dynamic random-access memories. However, the same industry people feel that IBM's flair for optimization will cause such a version to emerge soon.

Meanwhile, a report from the Norwalk, Conn., consulting firm International Resource Development suggests **that the public could desert home computers** much the way it has abandoned home video games at a rapid rate. A report from the firm says that less than 20% of sales are to individual consumers and estimates that up to 90% of bottom-of-the-line home computers lie unused on dusty shelves.

Century Data fields hollow-spindle drive

Claiming more efficient cooling, the Century Data Systems division of Xerox Corp., Anaheim, Calif., is introducing 190- and 380-megabit disk drives with hollow spindles for improved air flow. The new 14-in., multiplatter units are said to maintain error rates equal to Winchester drives' rates, but **over a much broader ambient temperature range—from 50° to 104° F** for the new Advanced Marksman series versus a 60° to 90° F spread for typical Winchesters.

Addenda

The No 5. ESS electronic switch, which the Bell System will employ for years to come as it goes all-digital, **will use fiber-optic cables to transmit digitally encoded control, timing, and traffic signals** among its modules. The distributed hardware controlling all those functions depends on software written in Bell's own C language. No. 5 can handle voice, data, and video. . . . One of the first step-and-repeat X-ray lithography systems, built by Cameca, a branch of Thomson-CSF in Paris, is being shown in the U. S. for the first time. The XPWS 301, **to sell for $1.1 million to $1.2 million,** accepts up to a 3-in. wafer with overlay and alignment accuracies of 0.02 μm and can expose line widths down to 0.1 μm. . . . 3Com Corp. of Mountain View, Calif., **is offering the first two controllers** to connect Q-bus and Unibus computers to Ethernet. . . . Texas Instruments Inc. of Dallas is readying a 16-K-by-4-bit dynamic random-access memory **that should attract makers of small systems and terminals,** especially those who need memory 4 or 8 bits wide but who will address fewer than 64 or 128 kilowords.

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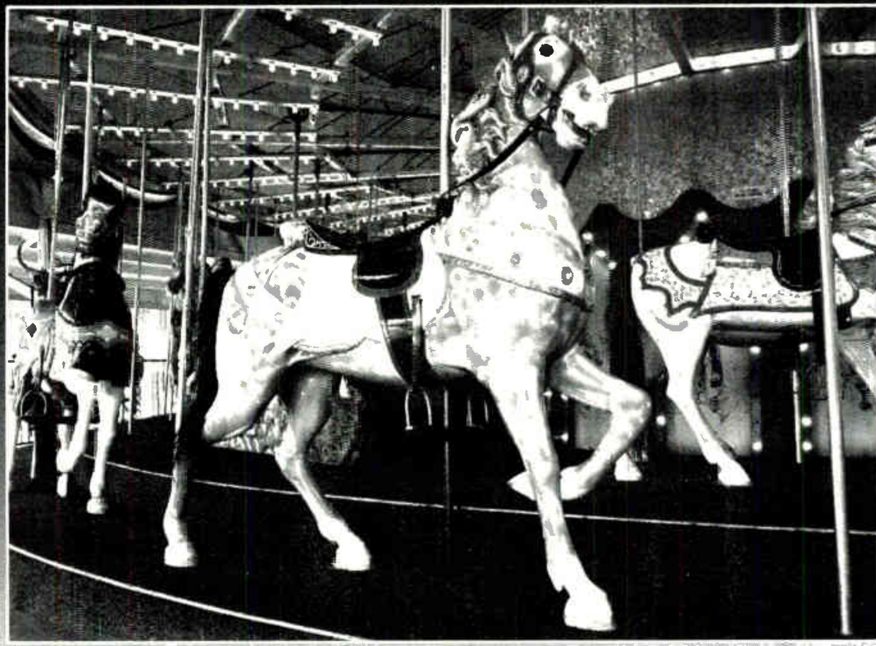

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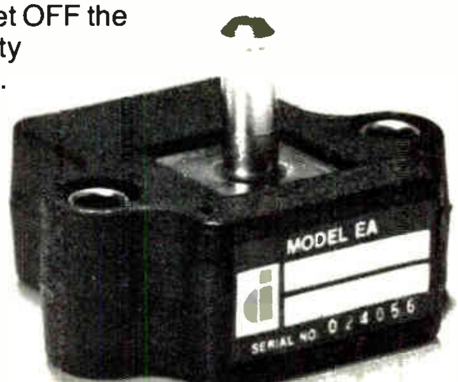

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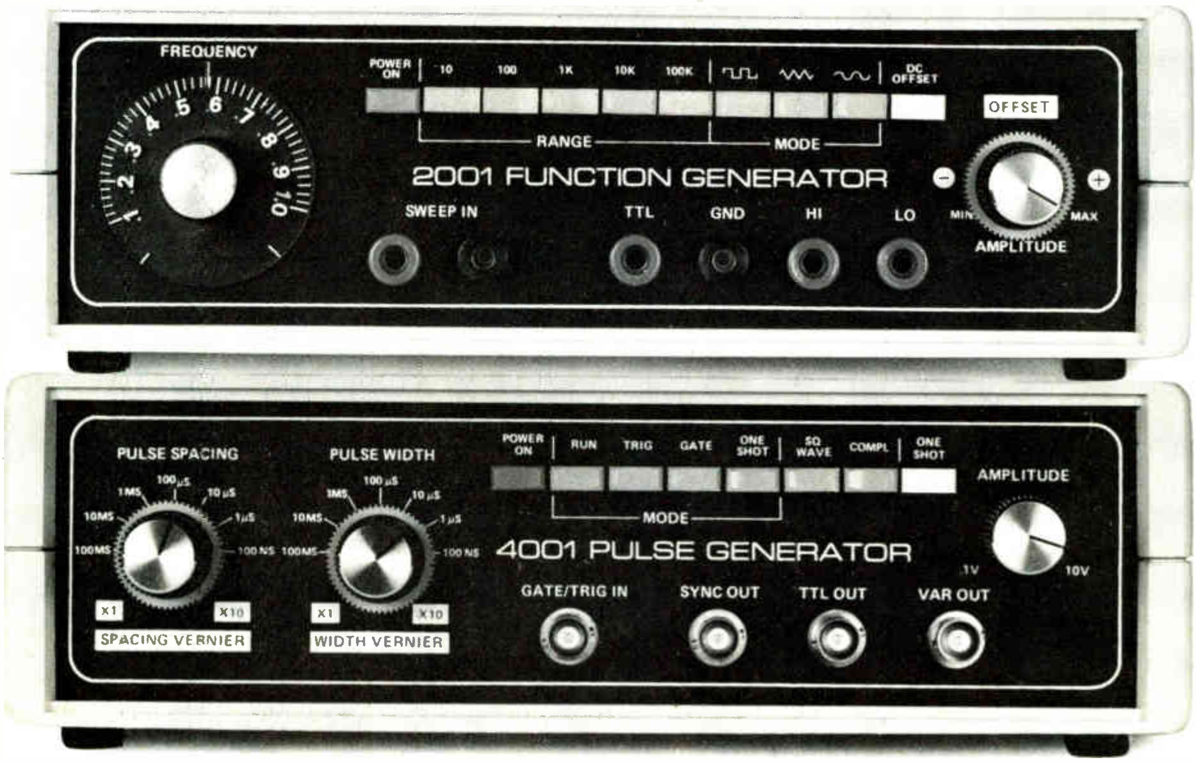

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Range of software for 16-bit processors broadens dramatically

by R. Colin Johnson, Microsystems and Software Editor

Adaptations of high-level languages for new IBM personal computer yield tested, ready-to-go packages

With its new Personal Computer, IBM Corp. may have broken the ice for a flood of 16-bit personal computers to follow. The big reason is the software that seems to have rushed into existence, largely through the efforts of Microsoft Inc., Bellevue, Wash., under contract to IBM.

Microsoft has adapted its own already popular high-level languages to the 16-bit microprocessor that IBM uses. Moreover, these languages—Basic, Pascal, Fortran, Cobol—run under Microsoft's own disk operating system (MS-DOS), also developed for the IBM machine.

Nor is Microsoft stopping there. The disk operating system was designed from the beginning to be upwardly compatible with three more sophisticated operating systems, capped by Xenix—a licensed version of Bell Laboratories' Unix. Unix is preferred by many professional programmers because it is easy to use and has well-regarded program-development tools.

Given the anticipated popularity of the IBM Personal Computer and the availability of the Microsoft programs, not to mention the backing of the largest software publisher, Lifeboat Associates Inc., MS-DOS should become as popular for 16-bit microsystems as CP/M-80 is in the 8-bit realm, predicts Tony Gold, president of Lifeboat in New York (see "IBM Personal Computer to spread the faith," p. 38).

For Microsoft, the work with IBM has been particularly rewarding in terms of the quality of the final product, points out Microsoft's president, William Gates. "As a result of IBM's super-extensive testing, the quality of our 8086 language offerings is higher than even our most mature 8-bit offerings," says Gates, who had 35 of his staff of 100 working on the IBM project for more than a year. IBM itself is said to have had more than 450 people on the computer project.

Dedication. "IBM dedicated two dozen software experts to validate Microsoft's code with a grueling set of test programs and with guinea-pig user studies," Gates continues.

Looking ahead. Bill Gates, president of Microsoft, looks forward to being able to offer one of the largest software bases available to users of the 8088 and 8086.

"They found the most obscure bugs that would have taken years of user field testing to catch."

All told, Microsoft wrote more than 250-K bytes of code for the operating system, for the Basic and Pascal high-level languages, and for an 8088 assembler. (The IBM Personal Computer is built around an Intel Corp. 8088, a software-compatible version of its popular 8086 microprocessor.) The Fortran and Cobol compilers are still in the course of being written.

The operating system for IBM, referred to as PC-DOS, is based on a kernel purchased from Seattle Computer Products Inc. and written by Tim Patterson, who is now with Microsoft. It was designed to emulate CP/M-80 system calls so that Microsoft's high-level languages, which run under CP/M, could be easily rewritten for the 8088.

For Gates, the issue of software compatibility is particularly important. "All our 16-bit high-level languages will be compatible with their 8-bit predecessors," he says. "This means we'll have the largest software base around available to 8088 and 8086 users."

In addition, these languages execute fast because they have all been rewritten for the 8086 rather than having been designed to rely on cumbersome cross-compilers. Also, support for the 8087 arithmetic processor chip, whose socket is on the central processing board, is built into all the operating systems. This chip will speed up operation of the IBM Personal Computer even further.

The first operating system that was developed is a single-user version with minimum capability. A

IBM Personal Computer to spread the faith

The introduction of IBM's Personal Computer is "potentially the most significant event to date in the history of microcomputing," asserts Tony Gold, president of Lifeboat Associates, New York, the largest publisher of personal-computer software. Adds Eddie Currie, second in command at Lifeboat, "IBM has legitimized the personal computer, which has always been hindered by the public perception of it as a toy for hobbyists." Moreover, he claims the operating system adopted by IBM, Microsoft's MS-DOS, "is already the industry-standard operating system for 16-bit microsystems."

He holds this opinion even though the IBM machine and its software are being released only this month and Digital Research Inc., Monterey, Calif., which developed the standard 8-bit operating system, CP/M-80, is offering CP/M-86 for the IBM machine as well. Because software written under the 8-bit standard cannot run under CP/M-86, Digital Research will offer its own high-level languages written by Compiler Systems Inc.—authors of the popular C-Basic—which it recently acquired.

MS-DOS will become a standard because people trust IBM's stability and follow what it does, Gold and Currie explain. They expect that MS-DOS will be accepted in the same way that, for example, the 8-inch, single-density 3740 floppy-disk storage format, introduced by IBM in the early 1970s, became the *de facto* industry standard.

But even more significant is the fact that IBM will sell a large number of machines. In fact, Lifeboat is already negotiating with applications software suppliers and has ordered 25 Personal Computers so that it can validate the programs it receives. Gold says his MS-DOS software catalog will start off with 100 offerings in November and 10 to 20 additions each month thereafter. Lifeboat will also publish CP/M-86–compatible application software.

Currie has nothing but praise for how IBM went about its design. "They chose a 16-bit processor for a long product life and ended up with the fastest personal computer available to boot," he says. "They made the right software choice too, since it now has an instant software base because of its compatibility with Microsoft's high-level languages. And the Personal Computer also has the promise of acquiring the largest application-software base around, which Lifeboat will publish."

-R. Colin Johnson

multitasking system will follow shortly. Both are based on floppy disks. Above these will be two other systems—one a full-blown Xenix requiring a hard disk and the other resembling Xenix but trimmed down to fit in a floppy-based system.

Microsoft will be demonstrating its Xenix implementations for the 8086, 68000, and Z8000 at the Comdex '81 show in Las Vegas in November. It is also bringing up its operating system on IBM's Displaywriter and is incorporating mouse-type graphics in it as well as kanji output for marketing in Japan.

Industrial

Sensing a pulse on inrush current is key to efficient motor drive

Inventors are not shy when it comes to boasting about their inventions. So when Parker Electronics Inc., Fort Lauderdale, Fla., unveiled its energy-saving controller for induction motors, it was no surprise that the company claimed it had bettered a power-factor controller developed by the National Aeronautics and Space Administration. This invention of Frank J. Nola, at last count, had been licensed by NASA to almost 200 firms in the U. S. alone.

The surprise is, however, that the National Bureau of Standards agrees with Parker and has recommended support by the Department of Energy for the Energy Economizer, as the invention is called.

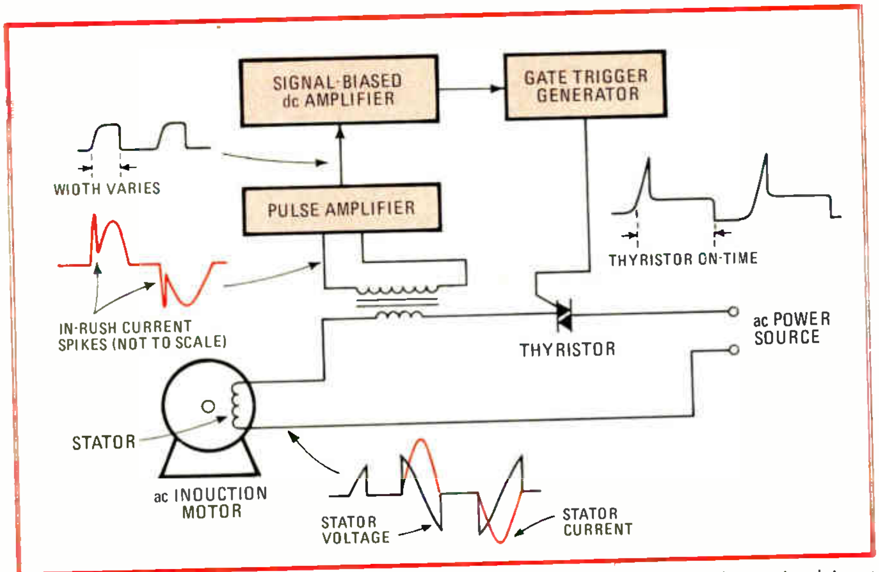
The controller, patented by Louis W. Parker and Rhey W. Hedges, was evaluated by the NBS Office of Energy-Related Inventions, Washington, D. C., under the Federal Nonnuclear Energy Research and Development Act of 1974, which provides free technical evaluations for energy-saving devices. Says Albert L. Hedrich, chief evaluator, "Parker has a better scheme for sensing motor efficiency, so NBS is recommending support to allow the Energy Economizer to enter the marketplace in competition with Nola's controller."

Less power. Hedrich notes that both inventions have the same goal: to reduce the power applied to a motor when it is operating at less than full load. Roughly 90% of the power consumed by electric motors is used in industrial applications that could benefit from such controllers. These motors turn up in machine tools, hoists, and blowers, as well as clothes dryers in the home.

Nola, to control power efficiently, developed a simple circuit that monitors the phase lag between applied voltage and stator current in the motor—an indication of motor efficiency. Both inventions use a thyristor switch to periodically interrupt, and, hence, vary, the ac power driving the motor. But Parker takes a completely different approach to sensing operating efficiency.

A stator excited by a partial sine wave, Hedges points out, experiences an inrush current with a very short characteristic pulse whose width depends inversely on the motor load. Moreover, the pulse's width, magnitude, and rise time are directly related to motor efficiency. Thus, the device relies on this pulse to tell it when to switch off the motor's power source.

The economizer monitors the inrush current for the first few hundred microseconds after the voltage is switched on. A transformer couples the pulse to an amplifier that removes the current variations due to the sinusoidal driving voltage—in effect, leaving only the inrush pulse, as shown in the figure.



Follow the blip. Parker Electronics' Energy Economizer senses the short pulse that exists on the inrush current to the stator winding and that varies with the load on the motor.

The amplifier also stretches the pulse duration to several milliseconds, maintaining the width's proportionality to motor load. A signal-biased dc amplifier converts this pulse train into a dc control voltage that controls the on-time of the thyristor switch.

Thus, for example, if the motor load drops to zero, as when the motor idles, the inrush current pulse width increases and the dc control voltage drops. This reduces the thyristor on-time and hence the power applied to the stator.

According to Hedges, who is vice president and technical director, "the phase lag between current and voltage indicates efficiency only for a full sine-wave input. When partial waves reduce the applied power, this parameter is an unreliable gauge of motor performance."

The Energy Economizer achieves nearly optimal energy savings because it directly measures the efficiency in each cycle, he says. It also avoids one of the NASA controller's early problems—instability in the control loop at low motor speeds.

However, as NASA's Nola points out, "it's hard to find a simpler design than the NASA controller. And as several companies have shown, the instability problem can be overcome." One of these firms, Nordic Controls Co. of Batavia, Ill., took Nola's device as its starting point. It then refined it to achieve what Nordic also says is nearly optimal energy savings. Nordic's units, range from a 115-volt, single-phase controller for a one-third horsepower motor at $130, to a 575-v, 50-hp controller for $1,750.

The Energy Economizer is at present under review at DOE, where Robert Bell is coordinating Government efforts. If a funding proposal is accepted, the agency could provide as much as $70,000 to $80,000 to help Parker develop and test prototypes and preproduction units. The company will then look to license the technology. **-Roderic Beresford**

Military

Air Force wants electronic ejection

The Flight Dynamics Laboratory at the Wright-Patterson Air Force Base in Ohio is about to solicit proposals for a microprocessor-controlled, digital ejection seat guided in all three axes. The service is worried that future generations of aircraft will make aerodynamic demands that might shave safety margins off the current ejection seats, which are based on mid-1960s technology.

Ejection seats now are almost totally mechanical. When ejection handles are pulled, an electric signal ignites a propellant charge to rocket the crewman from his plane. Pitot tubes and aneroid barometric sensors track the seat's speed and altitude to help control the parachute-opening sequences. But these are about the only parameters monitored, and no control is exerted over the propellant either; ejection can mean a rough ride.

Platform. In the system envisioned by the Air Force [*Electronics*, Sept. 8, p. 57], a small inertial platform similar to those used in missiles would monitor acceleration and attitude both of the aircraft before ejection and of the seat during and after ejection. It would track such parameters as aircraft pitch-and-roll angle to ensure as safe an ejection as possible. This could be critical to airmen flying at high speeds and low altitudes where a fraction of a second difference could mean ejection into the air or into the ground.

The heart of the system would be a fast microprocessor, possibly a 16- or 32-bit unit, with as much as 32-K bytes of random-access memory. The processor would monitor the outputs of the inertial platform of the traditional pitot tube and aneroid altitude sensor and also tie into the aircraft's data bus.

Although the seat processor would have to be independent of the bus—and indeed, independent of all aircraft electronic systems—it would be able to confirm its own picture of the world as relayed from the seat's inertial platform by comparing that picture with information from the aircraft's sensors.

Needed data. Thus, at the time for ejection, the microprocessor would be ready with all the data needed for safe ejection and a smoother ride, even with a damaged aircraft data-processing system.

At ejection, instead of simply triggering a charge under the seat, the microprocessor might control the thrust magnitude and direction of a rocket engine. Alternatively, the unit might control the sequenced firing of a number of small rockets variously directed. Both approaches offer directional control, making ejection possible from aircraft flying in unusual, previously unsafe regimes.

The microprocessor also would control the timing of the speed-absorbing drogue parachute's deployment and, after speed had sufficiently slowed, the deployment of a standard umbrella-like parachute.

What is available. The first step in the Air Force program will be to survey available technology. The team hopes to find the least costly high-performance inertial platforms, but meantime a unit will likely be borrowed from a missile program. Also, the flight lab suspects that existing mil-spec microprocessors are not fast enough for the task.

Because of the many new parameters to be monitored and the brief time it has for its tasks, the microprocessor may be the program's pacing factor. Today's escape seats go from a pull of the ejection seat handles to full chute deployment in about 3.5 seconds; the bulk of the computations might have to take place in only about 250 milliseconds. The Air Force would like to do it much more quickly.

Air Force engineers are willing to consider either the military qualification of one of today's faster commercial microprocessors or an array of smaller mil-spec microprocessors, each handling different parts of the timing and guidance task.

Requests for proposals may be out before the end of this month. Contractor selection could follow quickly enough for the program to start early in 1982. **-James B. Brinton**

Computers

32-bit world gets a low-end entry . . .

The superminicomputer market is seeing new highs in price-performance ratios as two more machines—one from Data General Corp., the other from Charles River Data Systems Inc.—join the machine announced last month by Perkin-Elmer Inc. At least a dozen companies now serve this market, with the new systems aimed squarely at one of the most popular of the products, Digital Equipment Corp.'s VAX-11 series.

International Resource Development Inc., Norwalk, Conn., a market research firm, estimates the 1981 market for the 32-bit computers at $300 million and predicts growth of 60% next year.

At the low-priced end of the spectrum, offering "32-bit precision on a budget," is Charles River Data Systems in Natick, Mass. CRDS, a longtime supplier of DEC-compatible disk hardware, now makes no bones about competing with DEC. The company's entire pitch is angled toward attracting DEC's present and future customers.

According to marketing vice president, W. Daniel DeLea, a Universe 68, as it is called, with 256-K bytes of main memory, one parallel and two serial ports, an 8-megabyte Winchester 8-inch hard disk drive, an 8-in. floppy-disk system, a Unix-like operating system, C language, and a cathode-ray tube terminal would list for only about $23,000. The discount on quantities of 50 drops this to $14,840.

16/32 bits. The machine is based on Motorola's MC68000, which is generally placed in the world of 16-bit microprocessors. But "since the chip uses a 32-bit internal architecture and our bus can handle 32-bit-wide transfers at rates of up to 20 megabytes per second, we consider that the Universe 68 offers '32-bit functionality,' " says DeLea. "System price is close to that possible with a DEC LSI-11/23, while our machine's speed exceeds that of most PDP-11's, and finally, it offers the 32-bit precision possible with a VAX-class computer."

Though the MC68000 has 32-bit data and address registers and performs 32-bit logical and arithmetic operations, it at present has a 24-bit program counter and can only use 16-bit-wide incoming and outgoing data. In the next 12 to 24 months, DeLea expects Motorola to extend the counter to 32 bits and repackage the chip to accommodate a 32-bit-wide input/output. With the enhanced 68000, CRDS will use the pin-out spec to make a simple circuit-board modification and change the Universe 68 from a "16/32-bit machine to a true 32-bit computer," says DeLea.

Thus CRDS is going not only after DEC's market among original-equipment manufacturers, but after users upgrading from PDP-11 series computers—and Data General Novas—who need 32-bit precision on a budget. The Natick company is even optimistic about snaring a few price-conscious users who would otherwise buy smaller VAX-class machines.

CRDS also plans to sell its operating system and software separately and to discount software by as much as 98% to quantity OEMs. In addition, it will sell board-level versions of the 68. **-J. B. B.**

. . . and a machine at the mid-range, too

At Data General Corp., Westboro, Mass., the wraps are coming off the Eclipse MV/6000 [*Electronics*, Sept. 22, p. 33], the company's answer to the mid-range of the supermini machines—DEC's VAX-11/750, Prime's 550-II, and IBM's 4331-2. Speed and price are the MV/6000's two key features, though Data General spokesmen also speak warmly of the 6000's full suite of 32-bit software and its rack-mountable size.

But the bottom line is the price-performance ratio, and here the new machine may win out. Its performance in double-precision Whetstone standard benchmark tests is faster than that of its competitors in merely single-precision operation, the company asserts. The MV/6000 clocks in at 1191 single-precision Whetstone operations per second and 400 double-precision Whetstones. The Whetstone performance measurement is the number of instructions in a standard mix that a computer can execute in one second.

According to Data General marketeers, "our pitch can be simple. Though we have other features like software and ease of maintainability, we could sell on speed and price

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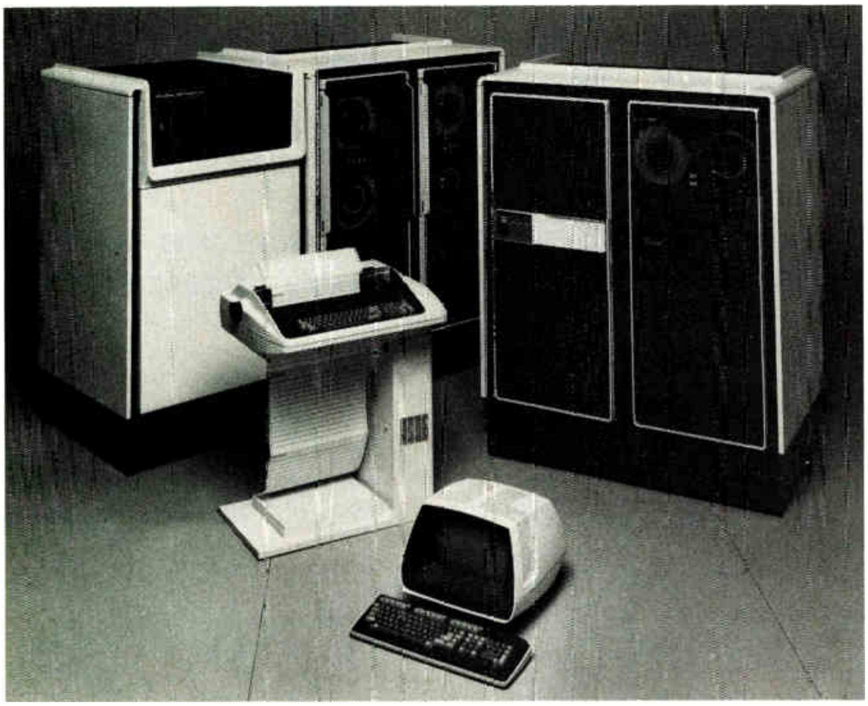

New member. Eclipse MV/6000 superminicomputer runs under the 32-bit Advanced Operating System/Virtual Storage and operates Data General's 32- and 16-bit software.

alone. The 6000 is two to four times faster than the competition at single-precision work and from 1.3 to 3.5 times faster at double precision."

In average configurations, all four systems are priced within less than $80,000 of each other. An MV/6000 costs in the region of $215,000, a VAX-11/750 about $210,000, IBM's 4331-2 is $290,000, and Prime's 550-II about $210,000.

The MV/6000's speed is possible because it uses the same pipelined processor as the company's larger MV/8000. Also, the machine holds up to 2 megabytes of main memory, cutting disk transfers. Maximum program size is 2 gigabytes, "doing away with the program size problem forever," as a spokesman puts it.

Last month's introduction of the Perkin-Elmer 3210 at $49,000 [*Electronics*, Sept. 22, p. 43] will not make things any more comfortable for the other 32-bit computer makers. The 3210's performance belies its low price. According to Richard Donnelly, 3200 series product line manager, the 3210 achieves single-precision Whetstone performance of 561 operations per second, as well as 454 double-precision Whetstones. It offers 512-Kbytes of main memory, two 13.5-megabyte disk systems, one fixed and one removable, a Perkin-Elmer 550 display console, and the company's version of Unix.

Thus the heat is now on DEC. Its entire VAX line, as well as some of its PDP-11s, have been bracketed by recent 32-bit introductions, especially when Data General's MV/8000 Eagle and the more recent 32/87 from Gould Inc.'s Systems subsidiary are considered [*Electronics*, April 21, p. 247]. Attention now will probably focus on the forthcoming VAX-11/730, a new low-end 32-bit machine originally scheduled for introduction this fall but apparently delayed. **-James B. Brinton**

Packaging

Chip-carriers sport twin rows of leads

Hoping to win industrywide acceptance, Texas Instruments Inc. is backing the development of a new chip-carrier that roughly doubles input/output pin counts without increasing the package's size.

To do this, TI is asking the Joint Electron Devices Engineering Council to approve a chip-carrier format for both plastic and ceramic packages that employs twin rows of leads or pads along each of its four sides. According to the proposal, chips would be mounted on frames with leads on 25-mil center lines, as shown on page 44. (Lead frames of conventional chip-carriers are on 50-mil centers.) When placed inside the chip-carrier, the frame would extend only every other lead to the outermost edge of the package. The others would form a second row 50 mils behind the outer row. In any one row, leads on the plastic packages—and pads on the ceramic packages—are on 50-mil centers.

Twice the count. TI says the twin-row carrier could be mounted directly to printed-circuit boards and other substrates that use 10-mil minimum line widths and spacings. Therefore, according to the Dallas electronics firm, the new configuration would allow about twice the I/O count but keep it within today's mounting and processing technologies.

The proposal, a result of work in the corporation's Equipment Group and its semiconductor central packaging operation, will be completely outlined during Jedec's next meeting in Washington, D. C., in December. "By the end of [1982], we are shooting to have at least registration and possibly standardization," says Jon S. Prokop, manager of the Equipment Group's hybrid microelectronics laboratory, which is heading up the development of the ceramic package. Both the ceramic leadless chip-carrier and the plastic leaded chip-carrier, being developed by the central packaging operation, will bear the same footprint.

In the plastic leaded carrier, the two rows are formed over castellated edges on the package, creating outer and inner rows. In the ceramic package, the inner row of pads would actually be a series of metalized holes resembling donuts extending all the way through the carrier. To check solder joints of a directly mounted device, for example, "you

SCIENCE/SCOPE

A device that directly converts electrical input signals into output images could be used for optical data processing and the projection of very bright TV pictures on a large screen. The device, a CCD liquid-crystal light valve, uses a charge-coupled device array and a metal oxide semiconductor readout structure to transfer signal charges to a liquid-crystal layer. The readout source can be common white light or a laser in the spectral range from near ultraviolet to infrared. Hughes has demonstrated a fully operational 64x64-element device.

A fiber-optic communications system may lead to an anti-armor missile whose many advantages include firing without being exposed to enemy counterfire and locking on a target after launch. The concept calls for a missile with an imaging seeker to relay signals to the gunner over a glass thread that pays out as the missile flies. The gunner would select and acquire a target which he sees on a TV screen. The system would be low in cost because much of the data processing is done at the launcher, not the missile. It also would be reliable because the missile is immune to countermeasures and is controlled over the entire flight. Hughes and principal subcontractor ITT Electro-Optical Products Division are developing the Integrated Fiber-Optic Communications Link for the U.S. Army.

A new window material for infrared sensors to see through has shown to be highly resistant to damage from nuclear radiation. The material, produced using a reactive atmosphere process recently developed for oxide material, is a glassy silica called fused cristobalite. In tests at Hughes the material suffered no damage when exposed to gamma radiation of 1 million rads. Conventional fused silica, though known to be one of the materials least affected by radiation, is heavily discolored by doses even 100 times smaller. Fused cristobalite has slightly different physical characteristics from other fused silicas, such as a higher melting point, but it maintains the same high optical quality.

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A millimeter-wave radar has demonstrated its ability to track targets and guide missiles accurately through smoke and rain. The radar, under study because it has more resolution than conventional radar and can penetrate adverse weather better than infrared, was used to guide TOW (Tube-launched, Optically tracked, Wire-guided) missiles to stationary targets. In three of the successful launches, the target was obscured by heavy smoke and aerosols. In one of those, visibility was further deteriorated by rain. The demonstration was conducted by Hughes for the U.S. Army and the Defense Advanced Research Projects Agency.

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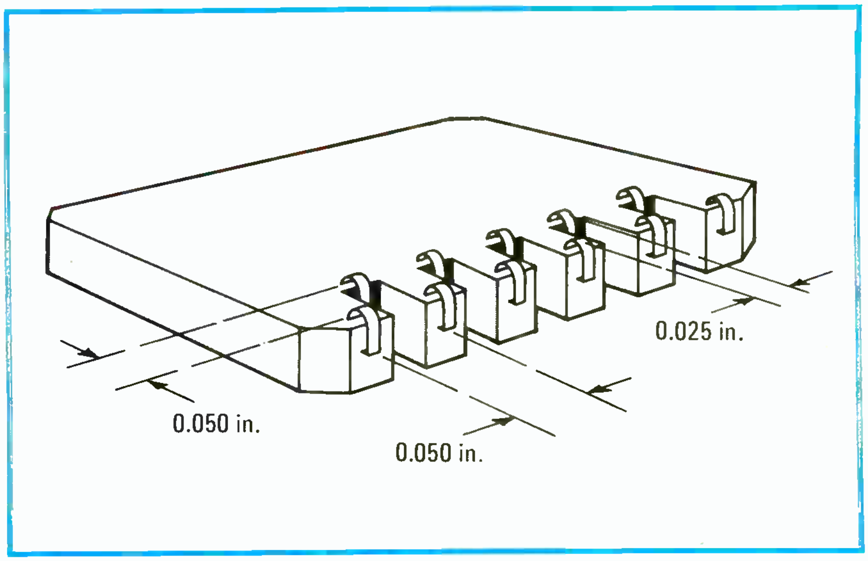


Castellations. TI wants to double the pin count of chip-carriers by bringing pins out alternately to a pair of rows on all four sides. (Only one side is shown here.)

Telecommunications chips get big supplier

Texas Instruments Inc., stepping out big into telecommunications, plans to introduce in the next two quarters a series of semiconductors dedicated strictly to that market's needs. These devices, coupled with recently announced second-source devices, will be targeted at a worldwide noncaptive market that the Dallas-based semiconductor giant predicts will hit $10 billion in 1991. This figure includes both multipurpose devices and those dedicated specifically to the industry. Currently, TI is a leading supplier of multipurpose ICs to the telecommunications industry, but up until now it has not provided the dedicated devices.

Multipurpose integrated circuits—such as microprocessors, memories, low-power Schottky, linear, and TTL—will make up about two thirds of that total business. The rest will be filled by dedicated telecom parts, such as ringers, speech circuits, line coders, tone encoders, codecs and filters. Spurred by the move to digital switching, the market's demand for dedicated parts will grow at a rate of 35% per year in the 1980s, predicts TI. It places the total market growth rate at 20% annually.

To produce the new telecom products, TI will employ five different technologies: 150-volt merged complementary-MOS, bipolar, and lateral power field-effect transistor (bid-FET); bipolar junction-FET (bi-FET); linear bipolar; metal-gate C-MOS; and silicon-gate n-channel MOS.

Eventually, the company believes, metal-gate C-MOS will be replaced by an advanced C-MOS silicon-gate technology that uses an n well in a p substrate. This substitution would reduce power requirements and increase density and performance.

The company is entering the telecommunications business after two years of work at 10 TI design centers—7 situated in France, England, Germany, and Italy and 3 in the U. S. It is setting up its telecommunications front-end operation in Dallas.

TI hinted at its intentions to enter the field last month with its announcement of two separate second-source agreements with Intel Corp. of Santa Clara, Calif., and Mostek Corp. of Carrollton, Texas. Under one agreement, TI will second-source three Mostek tone encoders: the MK5087, MK5089, and MK5092. TI has also agreed to second-source Intel's 2910A pulse-code–modulation encoder-decoder. Last month, TI and Intel also announced an agreement to manufacture a combination codec-filter with common pinouts and functionality. **-J. R. L.**

could look through the holes and see if the solder has made a good connection," Prokop says. "The metalized holes could also be used to self-align the carrier in test sockets and actual system sockets."

The twin-row format almost doubles the I/O count. For example, today's 44-pin package, measuring 0.650 inch square, would increase to 76 pins but remain the same size. A package with 68 I/Os, at 0.950 in. on a side, would contain 124 pins. At the high end, today's 156-pin package, at 2.050 in., could contain as many as 300 pins.

Prototypes. TI plans to have prototypes of the 124-pin ceramic double-row carriers by the end of the year. It believes that 300 pins would be the practical limit for this format in the plastic leaded chip-carrier. However, ceramic carriers' pad counts could be increased by adding a third row. The equipment group is currently studying this possibility, according to Prokop. "By putting another row of metalized hole contacts on the carrier, you could get up to a total of 436 [pins] in a 2.1-in.-square package," he says.

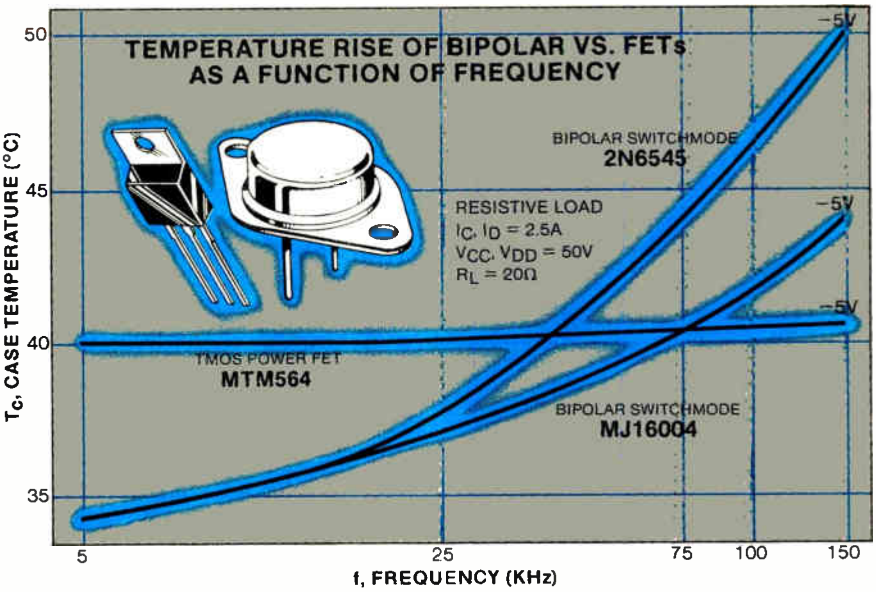
Theoretically, even more rows could take that total up to 600 or 700 contacts—a feature that is attracting the attention of a number of contractors working on the Department of Defense's Very High-Speed Integrated Circuits program. Some VHSIC devices may require as many as 500 contacts in phase II of the program. **-J. Robert Lineback**

Production

Graphite strip anneals simply

Annealing ion-implanted semiconductors to realign their crystal structures is costly or time-consuming and often both. But now a research team at the Massachusetts Institute of Technology's Lincoln Laboratory in Lexington, Mass., has developed a new method that heats by contact, is especially applicable to the needs of experimentation, and promises to be

Technological leadership.



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For anything under 100 kHz where the majority of designs are, bipolar Switchmode may be a better answer. Exhibiting lower "on" losses, it runs cooler and more efficiently than MOSFETs, even with their higher power gain.

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News briefs

Digitized voice message market gets IBM entry
IBM Corp.'s General Systems division, Atlanta, has introduced a computer-based message system that records and stores voice messages digitally before forwarding them to their destinations. Called the Audio Distribution System, it is one of several such products for improving the efficiency of business communications that have hit the market this year [*Electronics*, April 21, p. 99]. American Telephone & Telegraph Co. is also awaiting the Federal Communications Commission's approval of its plans to offer a similar system called Custom Calling II. The IBM system includes a Series/1 computer equipped to answer and dial telephones. Cost of a turnkey package ranges from $115,000 to $235,000 for up to 1,000 lines.

Ontario begins $11 million Telidon system
The province of Ontario, Canada, has begun installing an $11 million system of 2,000 terminals with 19-inch-diagonal screens for displaying information of interest to tourists and business travelers. The system uses the Canadian Telidon videotex system and is being installed mostly in the Toronto area by Infomart Inc. of Toronto.

Users will access a central data base of some 50,000 "pages" of information covering topics like local attractions, shopping, services, restaurants, accommodations, and the weather. The installation marks the first time a videotex system will be used for this purpose, the Canadians say.

both speedy and inexpensive.

The most common method used today is heat treatment in a furnace, where wafers roast for more than half an hour at upwards of 1,000° C temperatures. Compared with the Lincoln Lab approach, the cost, energy use, and time needed for furnace annealing is overkill. This is especially true in situations where an ion-implantation "recipe" is being "tuned" or where the characteristics of only a single wafer are of interest, so that speed and ease of use are important, not the annealing systems' throughput.

Down side. The Lincoln Lab system places a die or wafer with its implanted side facing down on a strip of graphite. Alternating current heats the graphite, which in turn heats the semiconductor material. Annealing, say the experimenters, occurs in less than 30 seconds.

The process takes place in a nonoxidizing-gas chamber—argon and hydrogen are used. To control the heating process, a thermocouple is embedded in the graphite, and its output is led first to an analog-to-digital converter and then to a microprocessor.

Controlling as much as 350 amperes through the graphite, the microprocessor is programmed to bring the strip up to annealing temperature in 5 seconds. In the Lincoln Lab experiments, the highest temperatures needed were between 700°C and 1,200°C. The temperature is held for 10 seconds and the current cut off, allowing the graphite to drop quickly back to ambient temperature. "This thing is so simple, it's probably not patentable," says John C. C. Fan, assistant group leader at the lab. "In fact, most people will probably build their own."

Cheap. Several versions of the annealer have been built. The most costly component is a 20- or 30-volt constant voltage transformer at about $1,000; beyond this, the cost of the rest of the system almost vanishes. Team members point out that the cost of 6 to 10 square inches of graphite is almost negligible and that, though the team used a low-cost 8-bit microprocessor and monolithic converters for control, manual control is easy and cheaper. The system also has worked in the open air, so a chamber—a stainless steel drum was used—is not necessary. An entire system could be built for $1,000 to $1,500, depending on what is already on hand.

In one experiment, the lab engi-

neers first implanted silicon wafers with various doses of 120-kiloelectronvolt positive arsenic ions, a common semiconductor dopant, producing amorphous layers. The wafers were then divided into 1-centimeter-square samples; some were annealed with the strip heater and others in a furnace at 1,000°C for 30 minutes. In both cases, annealing of the implanted layers was complete, and sheet carrier concentrations and average mobilities of the silicon were about equivalent. Conversion of the amorphous silicon into crystalline form took place at temperatures as low as 700°C with the strip heater. Measurements also showed that as much as 98% of the arsenic atoms wound up exactly where they should in relocation sites in the lattice.

Face down. The approach seems quite forgiving. "We have annealed chips both face up and face down," says staff member Bor-Yeu Tsaur, who is the lead scientist on the project. And when the annealing is done in the open air, "the only disadvantage is the graphite plate doesn't last quite as long."

Devices were checked to see if any of their characteristics had drifted as a result of free air annealing. There was no drift, indicating that "any [graphite] contamination problem appears to be negligible," says Tsaur. **-James B. Brinton**

Software

Z8000 gets its own silicon software

As software requirements for specific applications become better understood, more functions will be burned into silicon, rather than kept on a disk or in volatile memory. Intel started this trend for its 8086 microprocessor and has now been joined by a start-up company that has developed a similar silicon software system for the Z8000 16-bit microprocessor family.

The company is Hunt & Ready in Menlo Park, Calif. Its VRTX (pronounced vertex) is an interrupt-driven multitasking executive that relieves the application programmer of the burden of coordinating and synchronizing several concurrent processes. Rather than writing a monolithic program that solves the whole problem, the programmer merely writes a separate program to handle each of the various processes and uses the predefined routines in the VRTX to handle inter-process communication and synchronization.

Same tasks. This is also the approach that was taken by Intel Corp. of Santa Clara, Calif., with its 80130 real-time multitasking kernel chip for its 16-bit 8086 microprocessor [*Electronics*, Sept. 8, p. 135]. In fact, even though both parts were developed independently, there is a remarkable similarity in the kinds of tasks they perform, showing that real-time control is becoming a well-understood problem and a likely target for silicon software.

Each chip is organized not as one large program but as a group of independent system subroutines that are burned into a read-only memory. They allow task creation (that is, they allocate memory and interrupt status to a process located in main memory), task deletion (which deallocates memory and disables an interrupt), message passing between processes, and process suspension while waiting for an external event, with resumption when it occurs. They also include routines for timing, input/output, and interrupt servicing.

Lookup. The major difference between the two software systems, besides their running on different processors, is that the 80130 has the timers and an interrupt controller on chip, whereas VRTX may be configured to suit the target system by an external lookup table that can be as small as 14 bytes. In addition, VRTX uses streamlined routines because it does not have to maintain compatibility with an existing operating system, as Intel must for its iRMX-86. For example, it takes 128 microseconds to create a task with VRTX, whereas the 80130 takes 1.36 milliseconds due to its more elaborate mechanisms. **-R. Colin Johnson**

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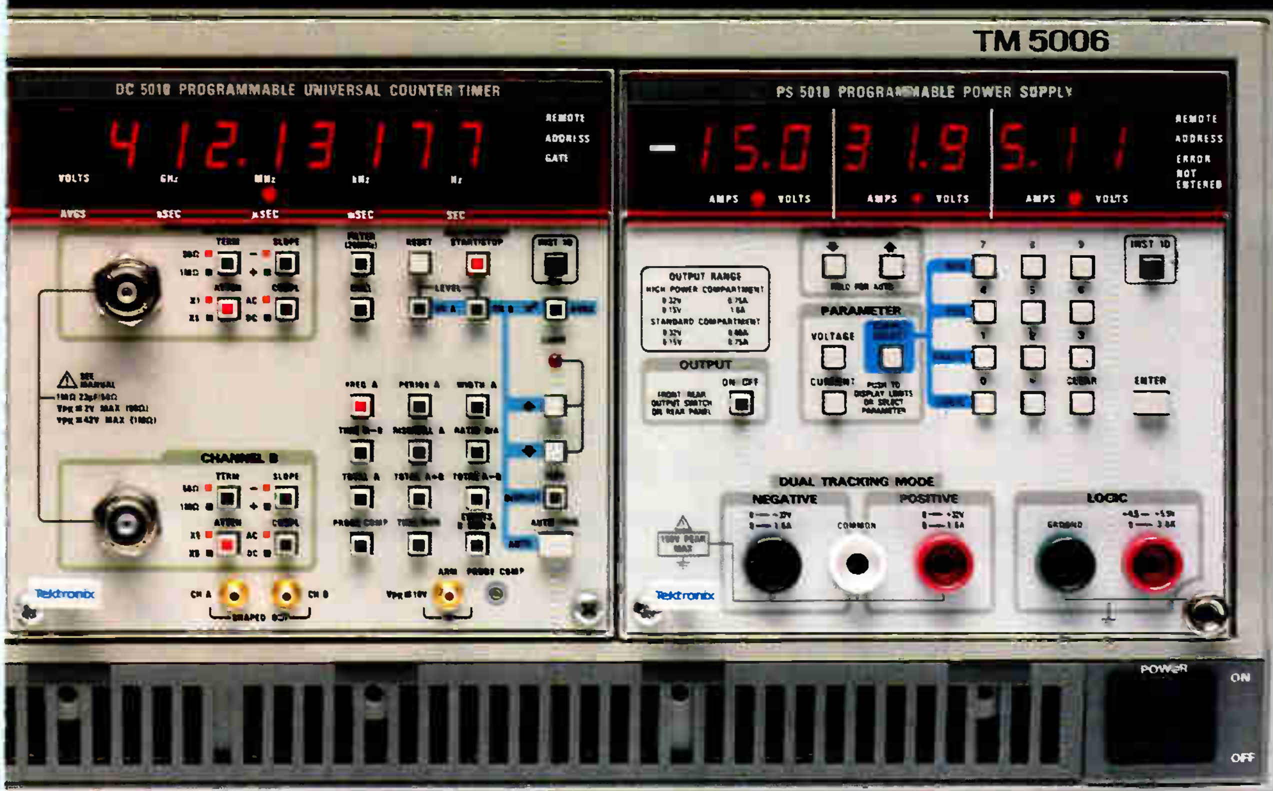

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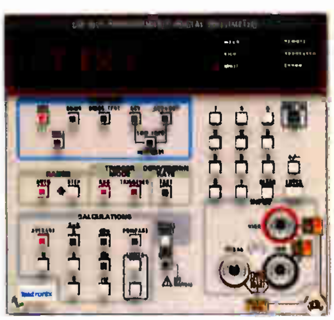

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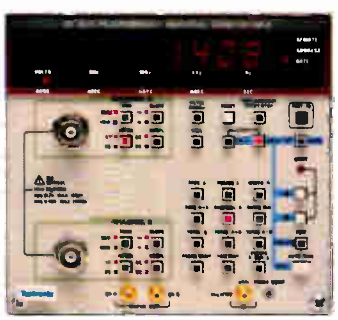

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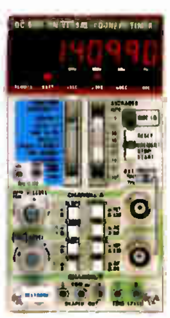

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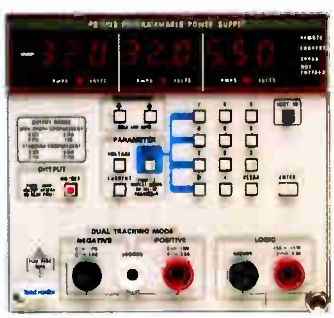

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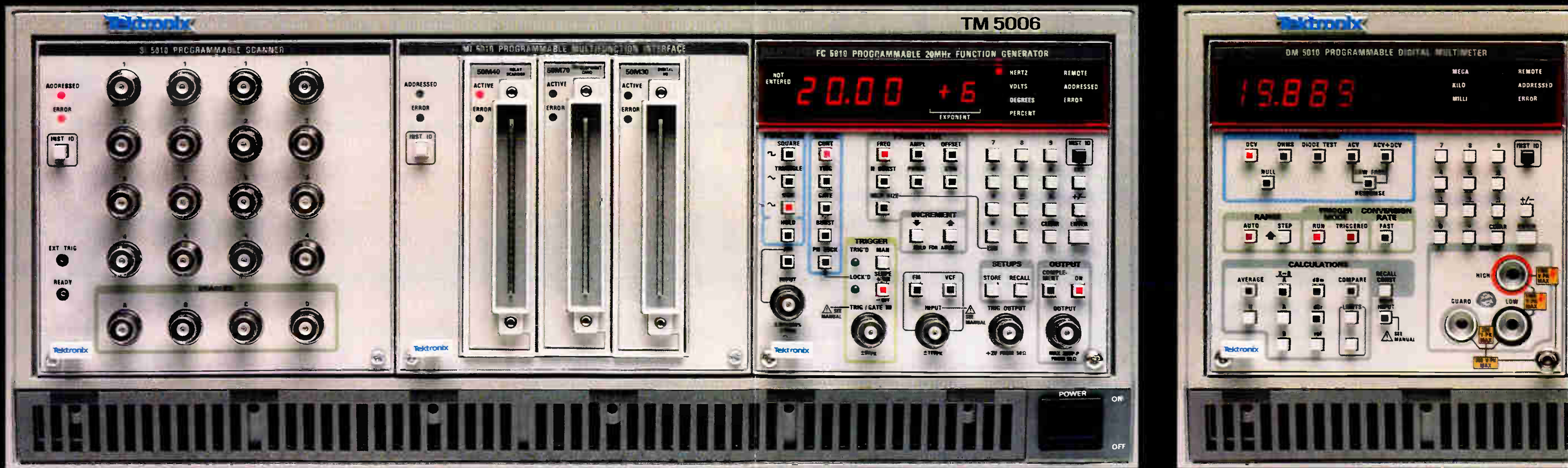

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4041 Controller provides program development facilities and system control.

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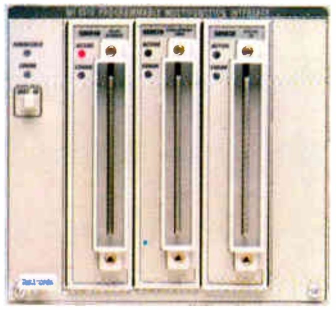

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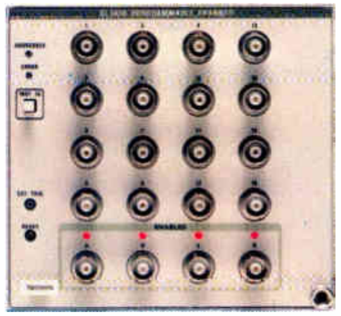

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Washington newsletter

Intelsat orders three more satellites from Ford Aerospace

The exploding demand for international telecommunications in the Atlantic and Indian Ocean zones has caused the International Telecommunications Satellite Organization to double its order for Ford Aerospace & Communications Corp.'s series V-A satellites to six. The new order with the company's Western Development Laboratories in Palo Alto, Calif., **will cost the Washington-based consortium of 106 member nations about $75 million** plus orbital incentive payments and inflation provisions. Each of the six Intelsat V-As, scheduled for launch beginning in 1983, can carry up to 15,000 simultaneous telephone calls plus color-TV signals. These birds, plus nine earlier V series from Ford, are expected to serve until the Intelsat VI series, with a 40,000-call capacity, is available in 1986.

U. S. telecommunications market gets new French competitor . . .

With the beginning of operations by Alphatel Corp. in the Washington suburb of Vienna, Va., the U.S. market for advanced telecommunications gets another foreign-owned competitor. **Major stockholder in Alphatel is the Paris-based Les Echos, France's major daily financial newspaper.** Alphatel, guided by Pierre Gaujard as chief executive officer, says it will develop, market, and sell videotex turnkey systems, using Antiope, Didon, and Teletel technologies. The systems are targeted at customers providing such services as data banks, cable TV, and common-carrier lines.

. . . Alphatel ownership split among five companies

Four other French companies participating in Alphatel (through U. S. subsidiaries) are: Cap Gemini-Sogeti, a software company with two American subsidiaries (DAS-D in Milwaukee, and Cap Gemini in Vienna, Va.); **CCS, a producer of Antiope decoders (Signatec Inc., Los Angeles);** Unitel, a maker of Antiope editing systems (Unitex Inc., to be formed in Los Angeles); and Antiope and Telematics Inc., a U. S. company to be formed by the French telecommunications agency.

DOD set to license Japan's VLSI technology for U.S. weapons

Watch for a formal agreement between the U. S. and Japan before the year is out that will permit the Pentagon to license domestic production of Japanese microprocessors and very large-scale integrated circuits for use in American weapons systems [*Electronics*, Aug. 11, p. 49]. U. S. officials say **the principal barrier to completion of the formal agreement lies in Japanese laws,** a product of the American occupation after World War II, prohibiting export of weapons-related technology. One loophole reportedly being considered by Japan would be to transfer the technology to the American military based there, who would then forward it to Washington.

NTT and IBM move toward deal on cross-licensing

The latest twist in the long campaign to get Japan's Nippon Telegraph & Telephone Public Corp. to open its procurement channels to U. S. manufacturers is likely to be a cross-licensing technology agreement between NTT and IBM Corp. If all goes well, the five-year deal will be signed this month, **reportedly giving NTT access to IBM computer-production technology and IBM access to NTT electronic-switching and other communications technology.** NTT does no manufacturing itself, and its buy-Japanese policy has been modified only recently after long negotiations between the two governments.

Tactical weapons upgrades: an electronics growth market

Makers of tactical military systems picked up another signal near the end of last month that their customers are unwilling to wait for a costly, all-new replacement of an existing weapon when for less money and in less time they can enhance its performance by buying a modification for it.

The source of the latest signal is the Army Helicopter Improvement Program. Under AHIP, Textron Inc.'s Bell Helicopter division is receiving $148 million for full-scale engineering development of modifications to its Scout helicopter that will give it day-night reconnaissance, communications, and target designation capabilities using a laser at the forward edge of a battle area. If the prototypes from the Fort Worth, Texas–based contractor perform as promised, the Army could ultimately spend up to $1 billion to upgrade its Scout inventory.

Scout versus Sotas

The AHIP/Scout, managed out of the Army Aviation Research and Development Command in St. Louis, contrasts markedly with the service's troubled Stand-Off Target Acquisition System. In development since 1979, Sotas cost estimates have soared more than 68% to their most recent level of $2.2 billion, while performance of its Motorola side-looking radar and Harris air-ground data link has yet to meet specifications [*Electronics*, June 30, p. 96]. Moreover, Sotas uses the larger and more vulnerable Sikorsky YEH-60B Black Hawk, whose costs and performance are being challenged in Congress. Motorola received a stop-work order for the Sotas radar from the Army earlier this year, and the Department of Defense is reviewing the whole effort with an eye to possible cutbacks or cancellation.

It is worth remarking that the AHIP/Scout program and its collection of subcontractors will use advanced television, infrared sensors, and a new high-frequency radio, on which much research and development has already been done, to accomplish the same sort of mission as Sotas will. Not only does AHIP/Scout promise lower cost, but it will in addition be ready for deployment sooner.

Keeping it simple

The near-term Scout will deploy its advanced television and infrared sensors, provided by Northrop, atop McDonnell Douglas Astronautics division's mast, which is extended above the center of the helicopter's rotor system. Reconnaissance data on an enemy's movements will be transmitted to the rear using an hf radio to be provided by Rockwell International's Collins Telecommunications Products division. The radio will also be used to call for and correct artillery fire and coordinate the actions of attack helicopters and other close air support, while the system's laser will pinpoint targets for the precision-guided munitions of other weapons systems. As plans stand at present, AHIP/Scout will carry only missiles for self-defense. Other subcontractors will be Litton Data Systems' Guidance and Control division for the heading and reference subsystems, plus Sperry Univac's Flight Systems division for what is described as the first completely integrated, multiplexed cockpit to be used in any Army helicopter.

Defense officials like to point to AHIP/Scout as a remarkable example of the new leadership's program called P³I for preplanned product improvement [*Electronics*, June 30, p. 88]. But though the Scout program is now incorporated into the P³I effort, the Army's helicopter improvement predates the Reagan Administration's acronym by months, during which the AHIP office evaluated the alternatives of using Bell's Scout or a competitive model from Hughes Helicopter.

Needs versus names

Whatever acronym may be assigned to the tactical military electronics improvement programs or whoever gets the political credit is less important outside Washington than the message conveyed by the P³I programs themselves. The message is that the DOD and Congress will more readily approve requests for money that can be used to upgrade a mature tactical system than they will approve funds for weapons whose deployment in quantity is a decade away.

The need to quickly develop and deploy target detection and strike systems that can operate day or night in any weather is clearly the most crucial tactical requirement of all three of the armed services today. They already have a variety of ground, sea, and airborne platforms on which to mount such systems. What the military needs now are the innovative combinations of advanced TV and infrared equipment to be employed in AHIP/Scout, upgraded radars, and the communications links to make them effective. That cannot be done efficiently by going back to square one. **-Ray Connolly**

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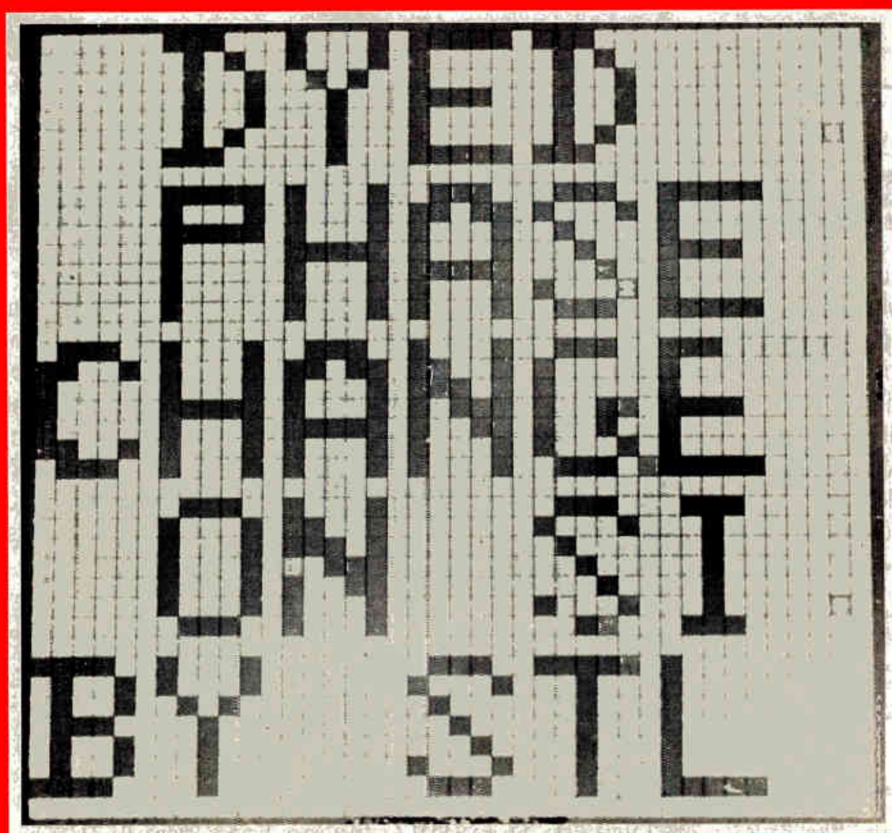
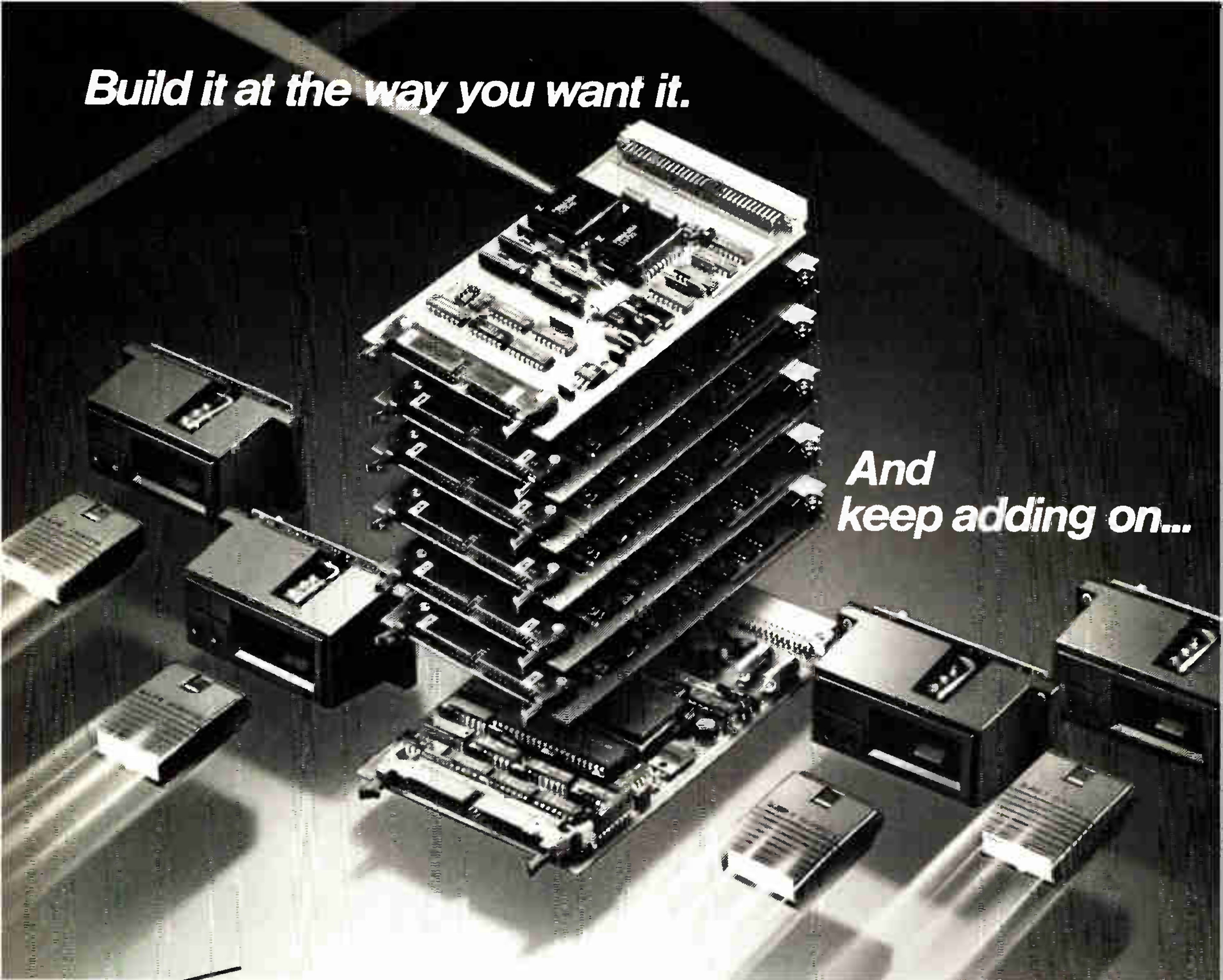
Oct. 6, 1981

Electronics International®

Siemens announces Europe's first 64-K RAM: page 72

This display's black liquid crystal when disordered absorbs light and when aligned passes it, creating a strong contrast: page 71





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Circle 61 on reader service card

International newsletter

GaAs 8-bit RAM attains 0.6-ns access

A fully decoded 8-bit gallium arsenide static random-access memory with a typical access time of 0.6 ns for a total power consumption of 80 mW has been developed at Thomson-CSF's Central Research Laboratory in the Paris suburb of Corbeville. The device uses enhancement-mode metal-semiconductor field-effect transistors with a low pinch-off voltage of 0.0 ±0.2 V. The minimum transistor widths are 20 μm and gate lengths are 0.8 μm. To simplify interfacing, the input voltage swing was kept down to 0.8 V. Thomson plans soon to **extend the design to a 256-bit RAM with an access time of less than 1.5 ns.**

Personal computers from NEC offer highest memory-money ratio

Two personal computers from Japan's Nippon Electric Co. are setting new records for installed memory in their price ranges. The consumer-oriented $389 PC-6000 has 16-K bytes (extendable to 32-K bytes) each of random-access and read-only memory. Many of its application programs will be supplied in ROM form. The $987 PC-8800 is oriented toward business and advanced personal applications. It has 72-K bytes of ROM containing two versions of Basic, 64-K bytes of main memory, and 48-K bytes of graphic RAM, with ROM and RAM being expandable to 64- and 320-K bytes each.

Like their predecessor, the PC-8000, the new step-up and step-down models use NEC's 4-MHz version of the Z80A microprocessor. Priced at $727 in Japan, the PC-8000 now **has 45% of the market there,** according to its maker, and for the time being is the only model being exported.

Glass display needs no driver board . . .

Two original display technologies have emerged from the Reading-based Display Products division of Britain's Racal Research Ltd., recently formed to develop highly reliable displays up to 49 in.² in area. Its circuits-on-glass technology eliminates the usual display driver board. Instead, **the back plate of the glass and liquid-crystal sandwich is extended to form the substrate for a hybrid integrated circuit,** supporting screen-printed tracks and driver electronics. An integrated eight-digit 200-MHz frequency-counter module, for example, requires just four external connections and is suitable for mass production.

. . . and front panel configures itself

Also, by combining touch-panel and liquid-crystal-display technologies, the Racal group has developed a front panel much like a menu-driven cathode-ray-tube display. By touching the panel, the user can select from a series of prompts, whereupon the display reconfigures itself and **shows a new series of prompts.** The group has supplied other Racal companies exclusively until now—one such product is a 32-character seven-by-five-dot matrix display that meets full U. S. military requirements—but is now offering a commercial custom-design and manufacturing service.

Five chips to blanket speech-synthesis uses

Five speech-synthesizer chips employing three modes of speech synthesis so as to cover a wide variety of applications have been announced by Nippon Electric Co. An adaptive differential pulse-code–modulated synthesizer in n-channel MOS delivers 8 seconds of speech at a price of $172 for the coding and $8.60 per chip in lots of 1,000. A formant synthesizer in complementary-MOS delivers 13 seconds of speech at a coding cost of $1,720 and $12.90 per chip in lots of 10,000. But **the three waveform-**

segment synthesizer n-MOS chips are the way to go for high-volume applications, even though coding is expensive. For one version with 8-K of on-chip memory, there is a software charge of $4,297 for 1 to 3 seconds of speech but only $3 per chip in lots of 10,000.

Transatlantic fiber-optic cable being pondered

A 3,500-mile fiber-optic cable could be carrying around 12,000 telephone calls across the Atlantic by 1988. A study group set up after a recent meeting in Brighton, England, of U. S. and European telecommunications authorities is to decide whether the technology can be readied in time. Called TAT-8, the project could finally be launched in 1983 at about the same time as TAT-7, a 4,000-circuit cable using conventional analog technology, enters service. A transatlantic fiber-optic cable would probably have three pairs of fibers and use **monomode transmission of at least 280 Mb/s** so as to give a basic carrying capacity of 4,000 calls per fiber.

European VCRs aim at the U. S. . . .

The Netherlands' Philips Gloeilampenfabrieken NV and West Germany's Grundig AG are getting ready to venture next year into the lush U. S. market for video-cassette recorders. Both firms have already demonstrated NTSC versions of their jointly developed Video-2000 system, and Philips in particular **sees good sales chances in the U. S.,** where affiliates Sylvania and Magnavox command a 15% share of the TV market. A strong TV position is considered essential to success with VCRs.

. . . accept stereo in West Germany

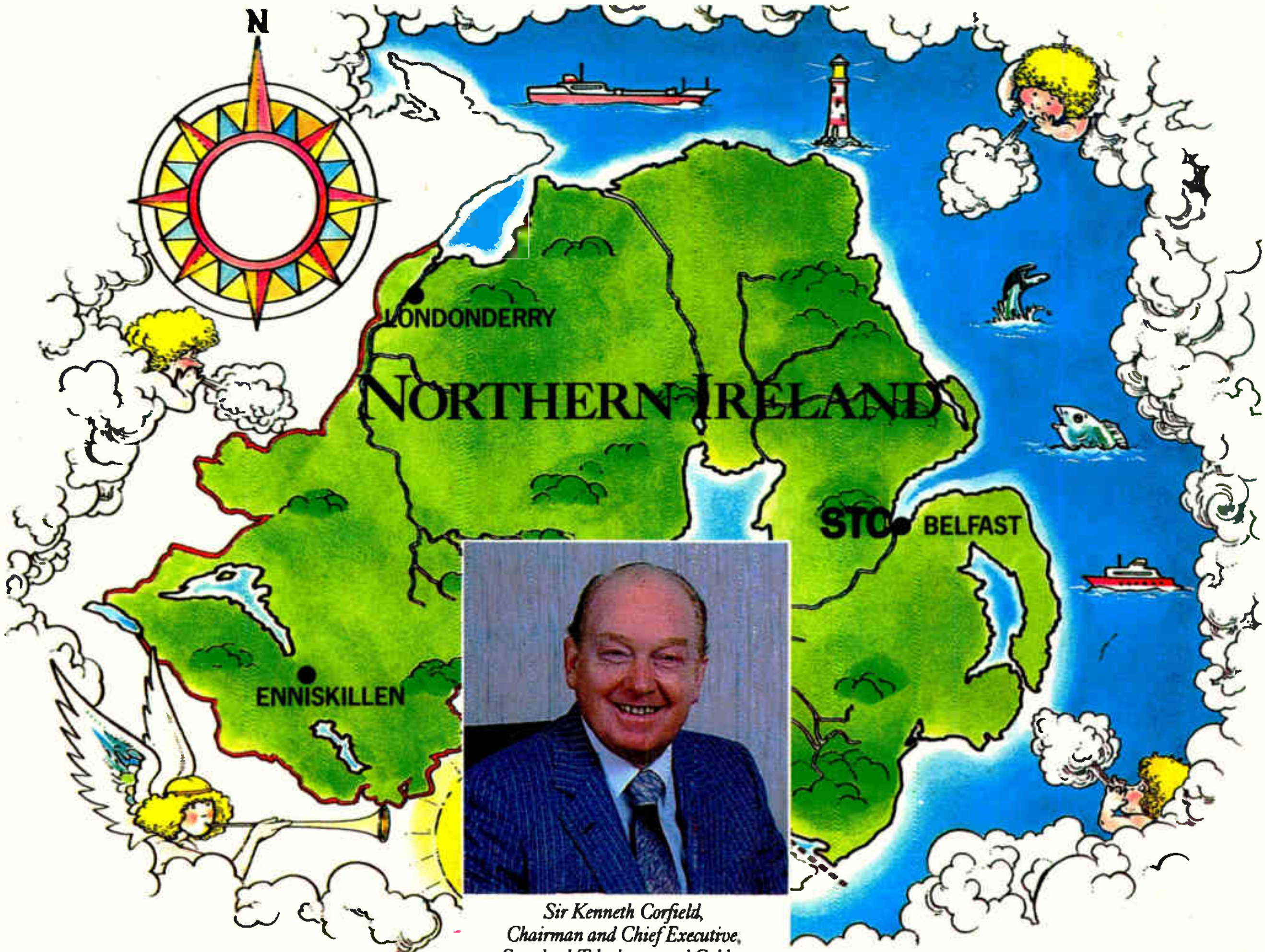
Back on their home turf, Grundig and Philips, Europe's only two video-cassette-recorder producers, are about to come out with VCR models for stereophonic TV programs—programs that West Germany's Second Television Network started broadcasting early in September. **Recording is on two 0.25-mm-wide tracks.** To reach the market in November, the stereo VCRs will cost about $90 more than monaural types.

C-MOS version of 6801 arrives

An enhanced instruction set and higher execution speed together with much lower power consumption are among the features of Hitachi Ltd.'s HD6301V, a pin-compatible n-well complementary-MOS version of the n-channel MOS 6801 microcomputer. The 88 basic instructions include the entire 6801 set plus bit-manipulation instructions, register-to-register exchange, and two low-power modes. Pipelined control—which microcomputer engineering department manager Hiroyuki Nakano thinks is **a first for an 8-bit computer**—enables many instructions to execute in half as many clock cycles as the 6801, producing a 20% increase in throughput.

Futures of memory technologies vary

Shipments of electronic and electromechanical memories will reach $150 billion worldwide by 1990, with the electronic types accounting for 45% of that figure—up from 40% of the $9 billion 1980 market, according to a new 10-month study from Luton, England–based Mackintosh International. It predicts that **bubbles will gain and maintain a 1% share of the market by 1990** and continue to enjoy a fourfold advantage in packing density over dynamic MOS random-access memories. But the report is lukewarm about Josephson junctions, favoring instead nitrogen-cooled gallium arsenide devices for high speed.



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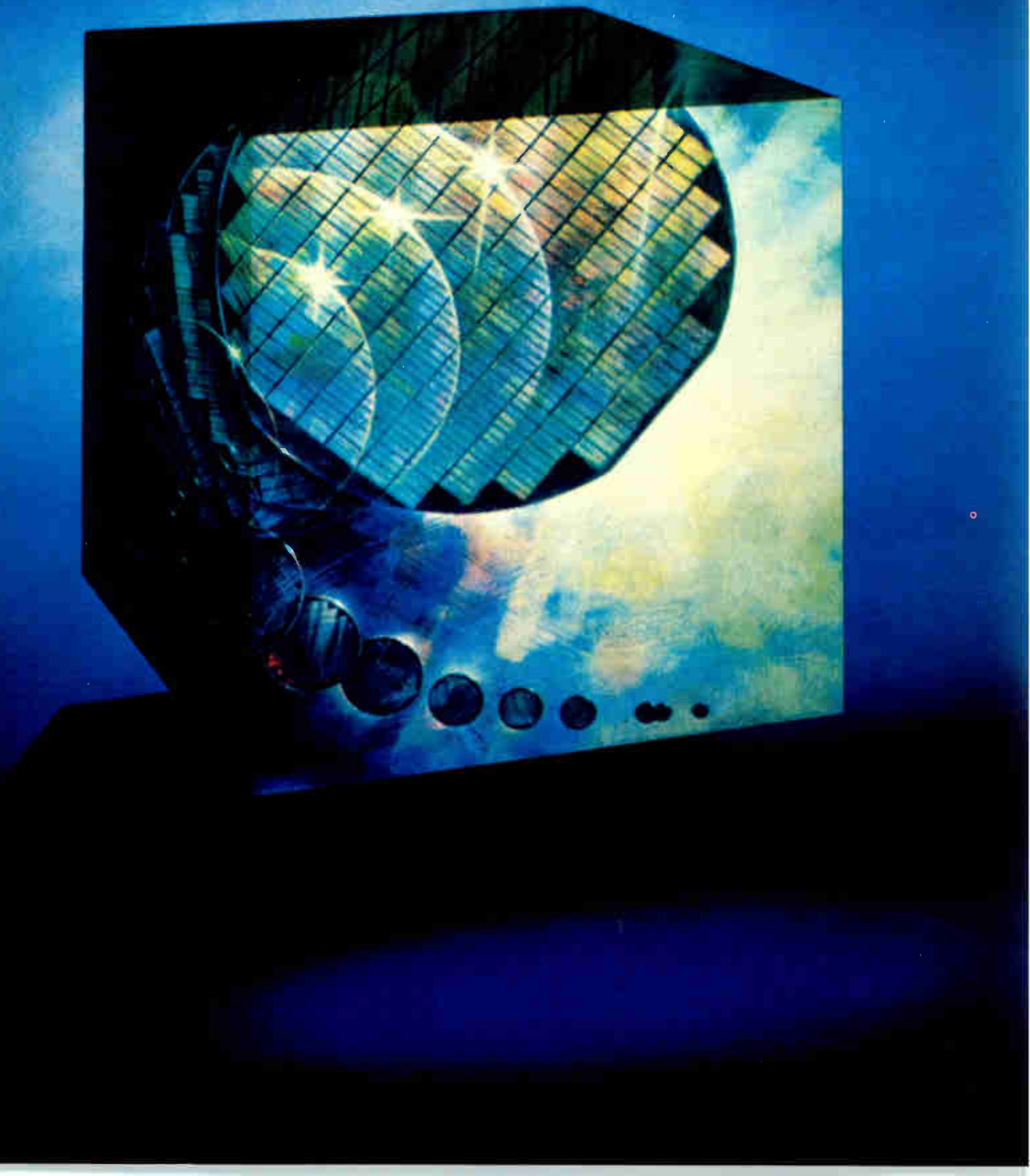

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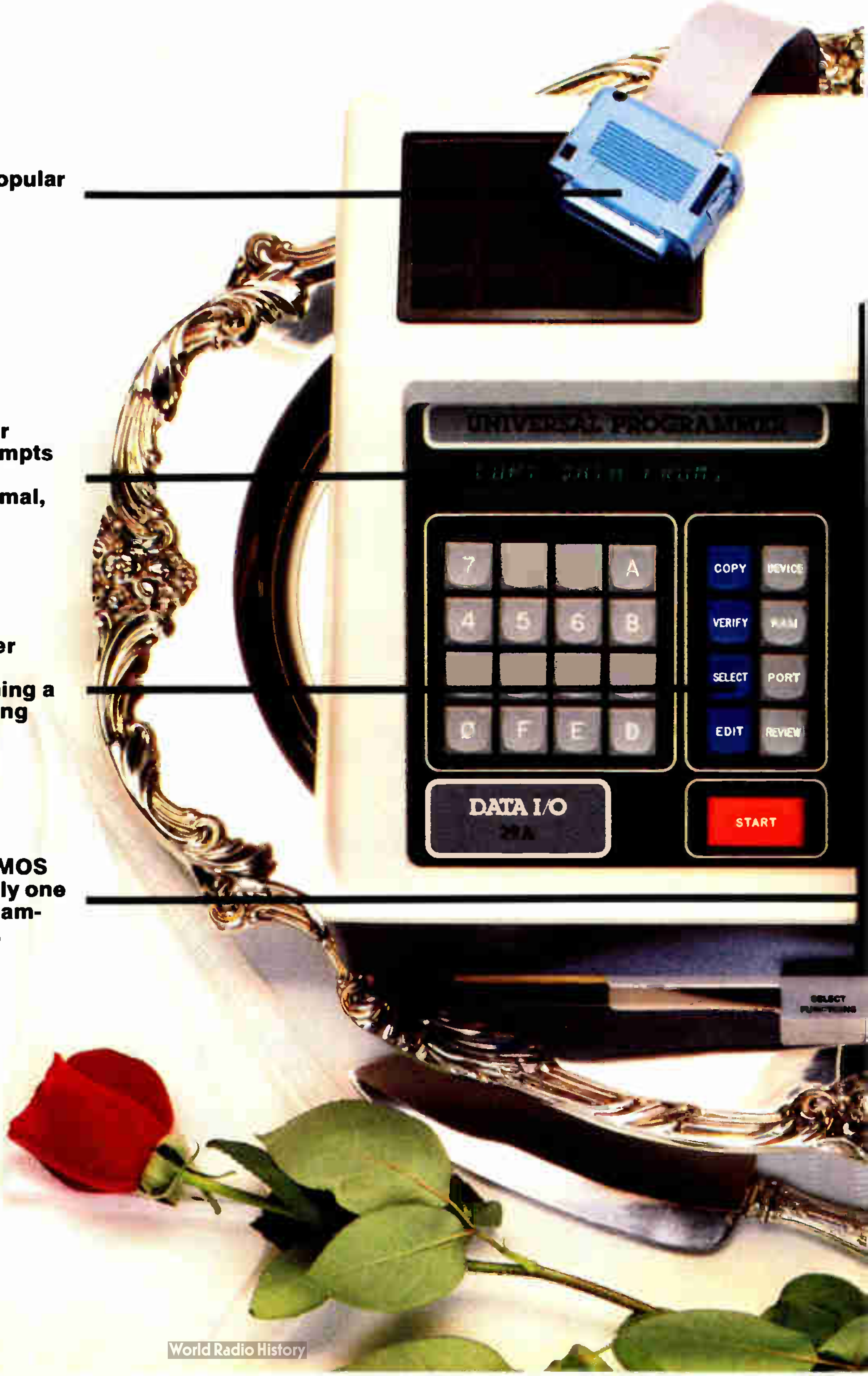

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PHILIPS

LCD stays legible in cockpit glare

by Kevin Smith, London bureau manager

Dyed phase-change dichroics produce strongest contrast yet; MOS FET control circuitry underlies liquid crystal

A miniature, low-power replacement for the cathode-ray-tube display has moved a stage nearer at Britain's Standard Telephone Laboratories, Harlow. There researchers are combining dyed phase-change liquid crystal, which yields printlike black-on-white legibility, with a silicon wafer 3 inches in diameter that incorporates the driver circuitry for the display matrix.

The display area of just 1.4 in. (36 mm) a side is small. But according to W. A. (Bill) Crossland, who recently presented a paper on it at the Society of Information Display's conference in New York, it shows that "very large arrays of LCD picture elements can be addressed in this manner without penalty in contrast or viewing angle."

The group is now working on a display that will incorporate a 240-element-square matrix, or 57,000 picture elements, on a silicon substrate 4 in. in diameter. The display would be 2.7 in. square and its 100-line-per-in. resolution should clearly display a full viewdata page of 24 lines of 40 characters each.

The technology's viability, says Crossland, will rest on the incorporation of the row and column drivers and decoders on the wafer at acceptable yields. If this can be achieved, the technology could find many military and civil applications.

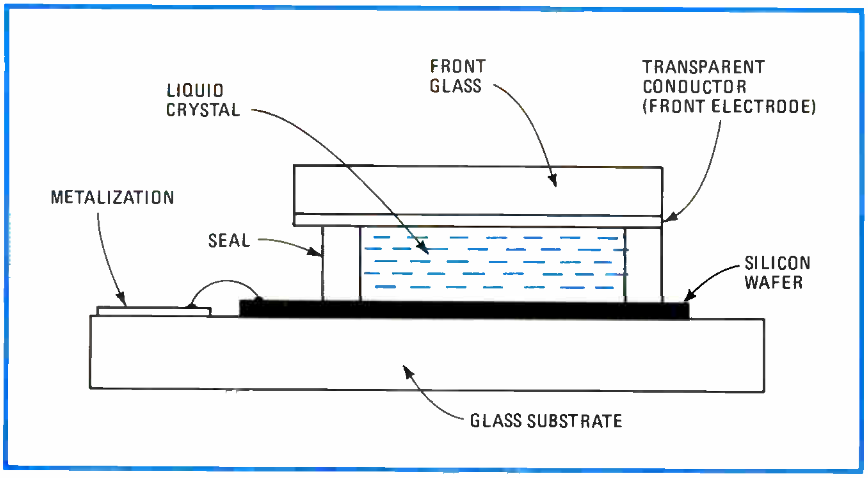
Britain's Ministry of Defence, for one, is interested in its use on the flight deck, and British Telecom sees use in compact viewdata telephones. The flat-screen television set, though, is not one application contemplated, as today's dyed phase-change dichroics have a poor gray-scale response.

Sample. STL's first prototype comprises a front glass with a single translucent electrode on its inner surface, a thin sandwich of dyed liquid crystal, and a 3-in.-diameter silicon substrate on which some 1,600 picture elements, each 1 millimeter square, have been formed in a 40-by-40 matrix. The matrix pads are covered with an insulating CVD silicon layer that also prevents a reaction with the liquid crystal.

Since the LCD is intended for crowded cockpits amid strong ambient light, good legibility is important. STL researchers use, perhaps for the first time, a black-dye phase-change liquid crystal that works by absorbing light rather than scattering it and provides "the nearest that LCD technology can approach to print-on-paper types of contrast," says Crossland. The device has a viewing angle of better than 60°.

To overcome the LCD's limited addressing capability, STL researchers, like one or two other labs, have in effect incorporated a display memory into the silicon wafer with a matrix of n-channel MOS field-effect transistors each connecting to a display driver pad. When the transistor is conducting, the pad can be charged to 16 volts, sufficient to activate the liquid crystal. When it is turned off, the charge remains trapped, holding the liquid crystal on.

Other driving elements such as thin-film transistors are being developed, particularly for use in large displays. But transistors used to drive displays need a low on-resistance for rapid charging and a high off-resistance to limit charge leakage when they are turned off. In these respects, cautions Crossland, thin-



Darkness at noon. This picture element turns black when the MOS FET in the silicon wafer turns on, letting the driver pad connected to it charge the dyed phase-change liquid crystal.

film transistors are no match for the MOS FET, which should win out for smaller displays.

The display is scanned a row at a time, a single metalized line opening the gates of every MOS FET in that row. Meanwhile, row data is applied to the column address lines—diffused channels formed in the substrate. Driver pads connected to high column lines are charged to turn on, while pads connecting low lines remain off.

An added complication is the need to reverse the polarity of the display voltage every 20.5 milliseconds to avoid electrochemical degradation of the display crystal. To facilitate this reversal, a blanking interval is inserted, during which time charge stored on driver pads is dumped.

The relatively large display driver pads and their associated transistors can readily be shrunk—from 1 mm^2 for the driver pads to 0.25 mm^2. When STL researchers have so redesigned their display and incorporated the row and column driver electronics on boards so that the chip will accept a serial data stream, the cathode-ray display may at last have a challenger. Others, though, are working on similar lines, including Panelvision in Pittsburgh and Hughes Aircraft Co.'s Industrial Products division in Carlsbad, Calif.

West Germany

Siemens takes aim at the 64-K market with low-power, simple-to-alpha-proof RAM

Industry observers have long been wondering what Siemens AG is up to in 64-K dynamic random-access memories. Now the West German company's Components division is ready to tell them—a 64-K MOS RAM it claims matches competitive devices and in some respects even surpasses them—for example, in power requirements and the ease with which it is made resistant to alpha radiation.

"Although we have had samples for some time, we deliberately held off announcing our 64-K," says Gernot Oswald, head of microcomputer activities and director of marketing for integrated circuits at the Munich-based division. "We wanted to be sure we had a reliable product on our hands, one that lived up to its specifications and had a chance of being among the world standards."

Customers will not have to wait long for the device. Volume production, at Siemens's new semiconductor facilities in Villach, Austria, will begin at the end of this year, "and during 1982 we will be fabricating more than 100,000 units a month," declares Hans-Jörg Penzel, operations manager for MOS memories. Thus, Siemens will be Europe's first semiconductor maker to mass-produce 64-K RAMs. "Barring any unforeseen circumstances, the least expensive version will be priced at about $10 in volume quantities next year," Oswald says.

Though at least one U. S. semiconductor firm in West Germany says it is too late for Siemens to enter the 64-K race, other companies as well as industry insiders feel it is right on target with its plan. Says one memory expert, "The company has a good chance of becoming a big factor on the 64-K market. And I trust them to have products as good as those from the Japanese." Adds an official at Darmstadt-based Gnostic GmbH, an affiliate of the U. S. market research firm, "I'm not sure whether Siemens is investing enough in 64-K production facilities, but the company has the technology to come up with top products."

Refresh reduction. The HYB4164 is a 65,536-word-by-1-bit memory fabricated with an n-channel silicon-gate technology. For high speed at low power consumption, it employs dynamic storage cells and dynamic control circuitry and half the usual number of read amplifiers, thanks to the use of 256 refresh cycles instead of 128. As a result, it uses only half the power of many competitive devices, says Penzel.

Of the two versions of the device, the fåster 4164-2 has access and cycle times of 150 and 280 nanoseconds, respectively, yet consumes only 120 milliwatts typically and 150 mW at most. The slower 4164-3 has corresponding values of 200 and 330 ns and 100 and 150 mW. For both, the typical standby power is between 12 and 15 mW and the maximum is 20

A RAM with a golden fleece?

With its HYB4164 64-K random-access memory, Siemens AG is entering a market that could turn out the most lucrative for the semiconductor industry. "Like some other companies, we believe that by the mid-1980s, worldwide sales of 64-K RAMs will reach $1 billion a year, thus becoming, in terms of both value and units sold, the best-selling single semiconductor item yet made," says Gernot Oswald, head of microcomputer activities and director of marketing for integrated circuits at the West German company.

Last year's worldwide 64-K market, he says, accounted for fewer than 1 million units. Not before 1985 will the number of 64-K RAMs exceed the number of 16-K types likely to be sold next year, Oswald declares.

Siemens appears determined to cash in on that market. "Out of the score or so of actual and potential 64-K producers, only 5 to 10 will be around in 1985 and Siemens will be one of them," Oswald predicts. In Europe, he adds, "we want to play a decisive role, and we see good chance in the U. S." A company should command at least a 5% a share of the world's 64-K market, otherwise it will find "little joy" on that market, he says.

The Siemens director bases his confidence on two factors: the know-how his company has gained with 16-K devices, and its standing relative to the competition. Oswald believes his company is ahead of many U. S. firms and technologically "as good as the Japanese" in the 64-K arena. -J. G.

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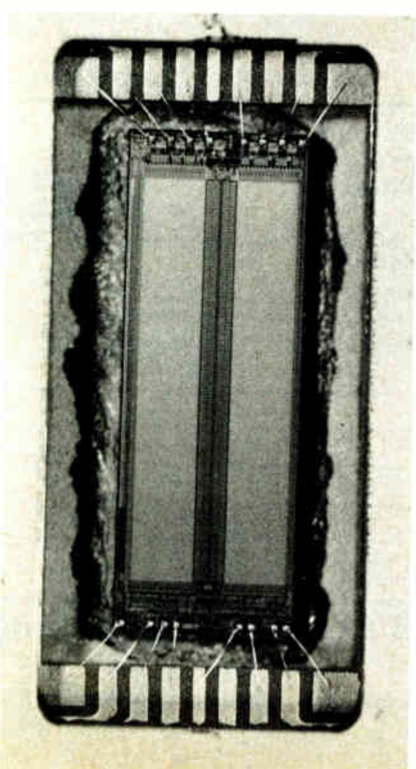
mw. In addition, to help minimize effects of alpha radiation, the Siemens engineers employ a photoreactive polyimide chip covering. Developed at the firm's research laboratories in Erlangen [*Electronics*, June 16, 1981, p. 73], the organic material can be applied by standard photoresist methods, thus reducing the number of processing steps normally needed to add it. But the memory does not neglect the customary defenses against alpha particles—it employs very high cell capacitances, word-line boosting circuits, and active pull-up resistors as bit lines.

Noise is equalized by an on-chip circuit that stabilizes the memory's substrate voltage. Also, over-and under-shooting on input levels of 6.5 V or −2 V for a period of 30 ns influences neither the functioning nor the reliability of the device. This gives the user much greater driving capability.

No spares. The Siemens chip uses no redundancy measures. "It's all a question of tradeoffs between yield, on the one hand, and additional costs and reliability-related factors on the other," Penzel notes. This philosophy, he adds, is also shared by other semiconductor makers today, notably the Japanese.

The HYB4164 chip measures 3.27 by 9.04 millimeters and comes in a ceramic package. Multiplexed address inputs permit the RAM to be put into an industry-standard 16-pin dual in-line package. System-oriented features encompass on-chip address and data registers, which eliminate the need for interface registers, as well as fully TTL-compatible inputs and outputs, including clocks. Common input/output capability is given by using "early write" operation. **-John Gosch**

Halved. Siemens AG configures its new 64-K RAM into two 32-K elements. The only other 64-K manufacturer to do so is Texas Instruments; the rest favor smaller modules.



Japan

C-MOS promises huge dynamic RAMs

Complementary-MOS technology, long considered a practical proposition only for static random-access memories, now looks as though it could be the ideal way of building dynamic RAMs. According to a team at the Central Research Laboratory of Hitachi Ltd., C-MOS is capable of producing 1-megabit and larger dynamic RAMs with an optimal balance of characteristics.

Their research has shown that devices using p-channel memory cells in n wells and made with 1-micrometer rules have breakdown voltages in excess of 15 volts. As a result, small cells can store a lot more charge than comparable n-MOS cells with their breakdown voltages of less than 5 V. Both drain breakdown and hot-carrier degradation contribute to the lower permissible operating levels of the n-channel cells; gate oxide leakage limitations of both types are similar.

No sacrifice. This high voltage breakdown is not obtained at the expense of performance—the p-MOS cell is faster than the conventional n-MOS cell because its source is connected directly to the bit line. Furthermore, the n-well configuration increases the cells' immunity to alpha particles, while the C-MOS processing of peripheral circuits—including a high-sensitivity cross-coupled C-MOS sense amplifier—provides an excellent balance of speed and power.

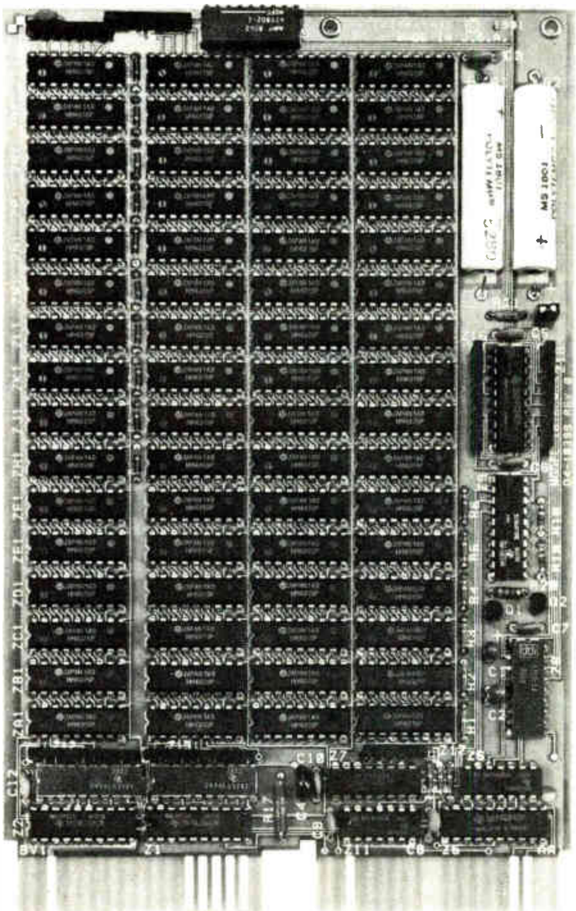
Noise disturbances caused by collector supply voltage bumping are also reduced because the storage capacitor cell plate is connected to the source supply voltage, which is grounded, and not to V_{CC}, as in most n-MOS devices.

To confirm that the new configuration is indeed practical, a 4-K-by-1-bit n-well C-MOS dynamic RAM with a cell size of 6 by 12 μm was fabricated on a 2.0-by-2.5-millimeter chip. It was made with two levels of polysilicon and 2-μm photolithography. In layout it resembles a conventional dynamic RAM, and it has folded bit lines and quasi-static peripheral circuits. Its typical access time is 40 nanoseconds, and its typical cycle time is 150 ns. Active power is 35 milliwatts, standby power—mainly for the bias generator for the n well—is 5 mW.

Standard of comparison. As a control, another 4-K-by-1-bit dynamic RAM was made in n-MOS technology using the same 2-μm lithography. Researcher Hiroo Masuda says that the characteristics of the two devices give a fair comparison of the technologies even though the n-MOS RAM uses a single level of polysilicon and open bit lines. Cell size is 11.2 by 16.8 μm, and chip size is 1.96 by 2.1 mm. This device has a typical access time of 60 ns with a cycle time of 150 ns; active power is 50 mW.

In fact, the circuits of a conventional n-MOS cell and the n-well p-MOS cell used in the C-MOS dynamic memory are similar in everything except operation. The p-MOS cell is fast even though its transistor is intrinsically slower than the one in the n-MOS cell. That happens because the transistor's source is connected to the data (bit) line. As the negative-going signal on the word line turns the transistor on, the voltage of the bit line falls by only a small amount. Consequently, the transistor is rapidly overdriven and circuit response is fast.

The n-MOS cell is slow because its source is connected to one side of the



Electronics international

cell's storage capacitor. As the positive-going signal on the word line turns the transistor on, the voltage of the capacitor to which the source is connected also rises. Thus the gate-to-source driving voltage applied to the transistor is barely enough to keep it turned on and circuit response is slow.

The device configuration provides immunity to cell-charge destruction by electrons injected into the substrate by alpha particles or TTL undershoot. An on-chip well-bias generator provides the n well with a positive bias of 1.5V_{CC} that prevents the electrons from being collected by the well. Tests show that the memory operates without error even with 500 microamperes injected into a positively biased substrate. This, memory can even be operated with the substrate at ground potential, a feature that has been mostly avoided in conventional RAMs (except those from Texas Instruments) because of the errors that are caused by TTL undershoot. **-Charles Cohen**

France

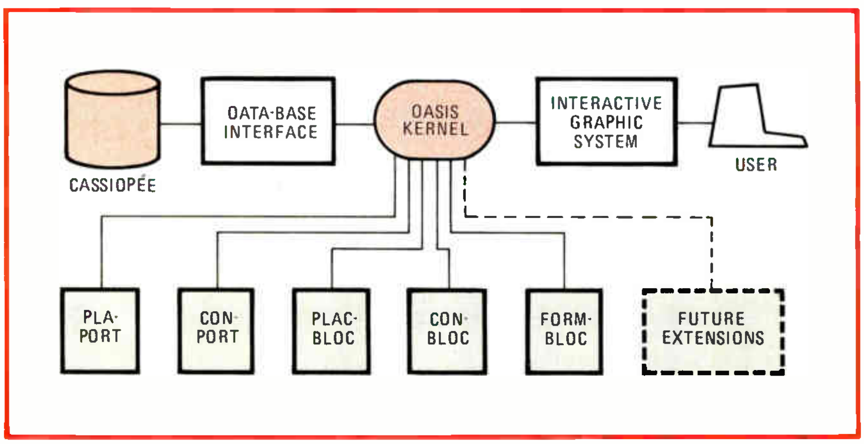
Multidrain-MOS technology yields Oasis for computer-aided design

The complexity of very large-scale integrated-circuit design can tax even a computer's powers with its excessive demands upon memory and for manipulation and computation time. But now, the multidrain-MOS technology designed specifically to simplify such computer-aided design problems [*Electronics*, June 5, 1980, p. 73] has culminated in a CAD system called Oasis.

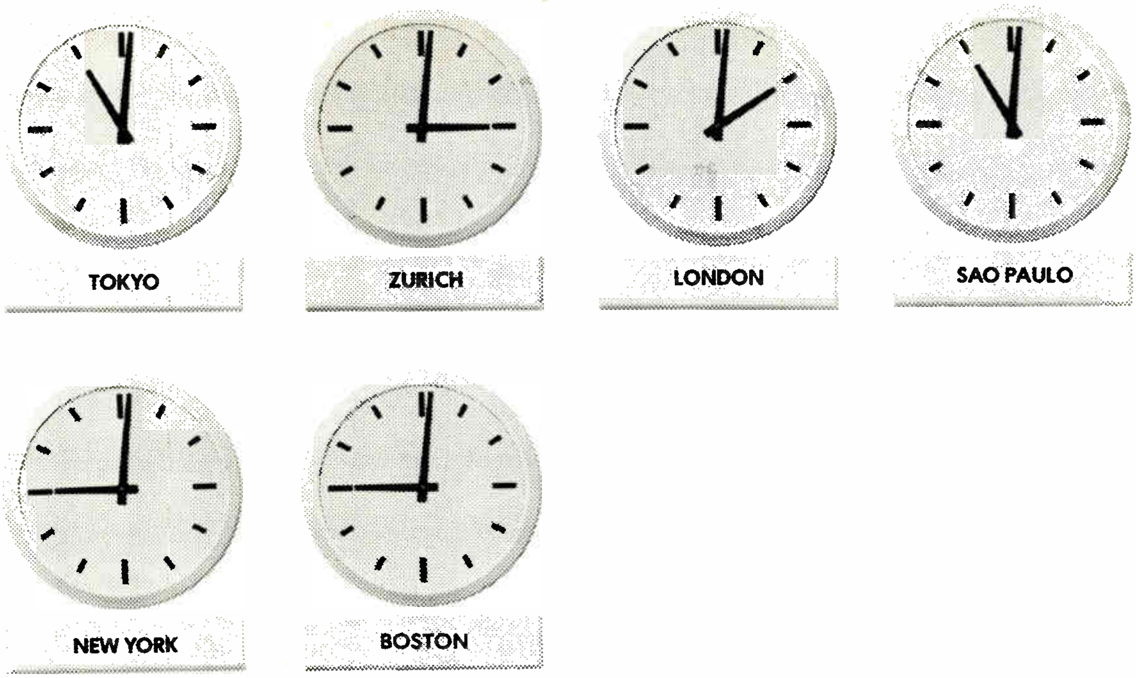
Developed at the Laboratoire d'Informatique et de Mathématiques Appliquées of Grenoble, France, Oasis stands for the French for automatic design tool for symbolic layout of circuits. It is part of Cassiopée, an integrated CAD system for integrated circuits developed at the Centre National d'Etudes des Télécommunications of Grenoble. Cassiopée contains data on numerous CAD systems, including Oasis

Simple symbolism. MD-MOS is ideally suited to CAD because it uses a simple symbolic-design format. A standard n-channel logic gate is combined with a variable number of drains. A depletion-mode n-channel transistor pulls up the gate of an enhancement-mode logic transistor. The gate also acts as the input line, and the drains serve as outputs. Because the gate width is constant, drains can be tightly packed.

According to Giles Serrero, one of the engineers who developed it, Oasis uses a three-level approach



Roots. One element of the Cassiopée CAD system is Oasis, four of whose six software modules (tinted gray) exploit the CAD-oriented design of multidrain-MOS devices.



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involving recursive definition of the circuit, either from the top down or the bottom up. The language used is Pascal.

In the top-down method, the dimensions of the elements at a given level (blocks, for example) are evaluated and laid out, thus defining the input/output connection points. Then the elements of next lower level (cells, say) are laid out in terms of the I/O points of the previous level. Any changes the new level requires in the layouts of previous levels are taken care of automatically.

With the bottom-up method, the elements at, say, the cell level are laid out, thus defining the input/output points for the next higher level. But this way there is no need to adjust a lower-level layout in light of the higher-level requirements.

Eight elements. Oasis consists of six software modules and two interfaces, one with Cassiopée and the other with a Calma graphic system. The central software module, called the Oasis kernel, controls the sequence of operations, data-exchange operations, and the data path between the user and Cassiopée and the other five modules. Three modules are defined for MD-MOS symbolism: Plaport automatically places the MD-MOS gates; Conport routes connections as segments along rectangular grid; and Formbloc connects the cells into the blocks so that any two adjacent cells share a common line. Finally, there are two general modules—Placbloc, which places the blocks, and Conbloc, which routes the connections between them.

"We are going to put the system into operation towards the end of the year on our Perkin-Elmer 8/32 and our Calma graphic system," says Serrero. "Oasis will be stored on disks but, since it is completely software, it could be used on any computer with enough capacity to handle it and all the modules could be stored on one or several disks or even on magnetic tape."

Oasis was described by Serrero and his colleague Rao Malladi last month at the European Solid-State Circuits Conference in Freiburg, West Germany. -**Robert T. Gallagher**

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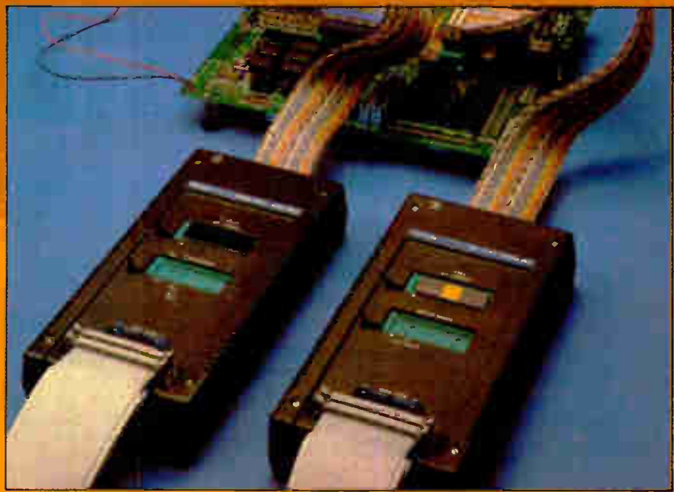

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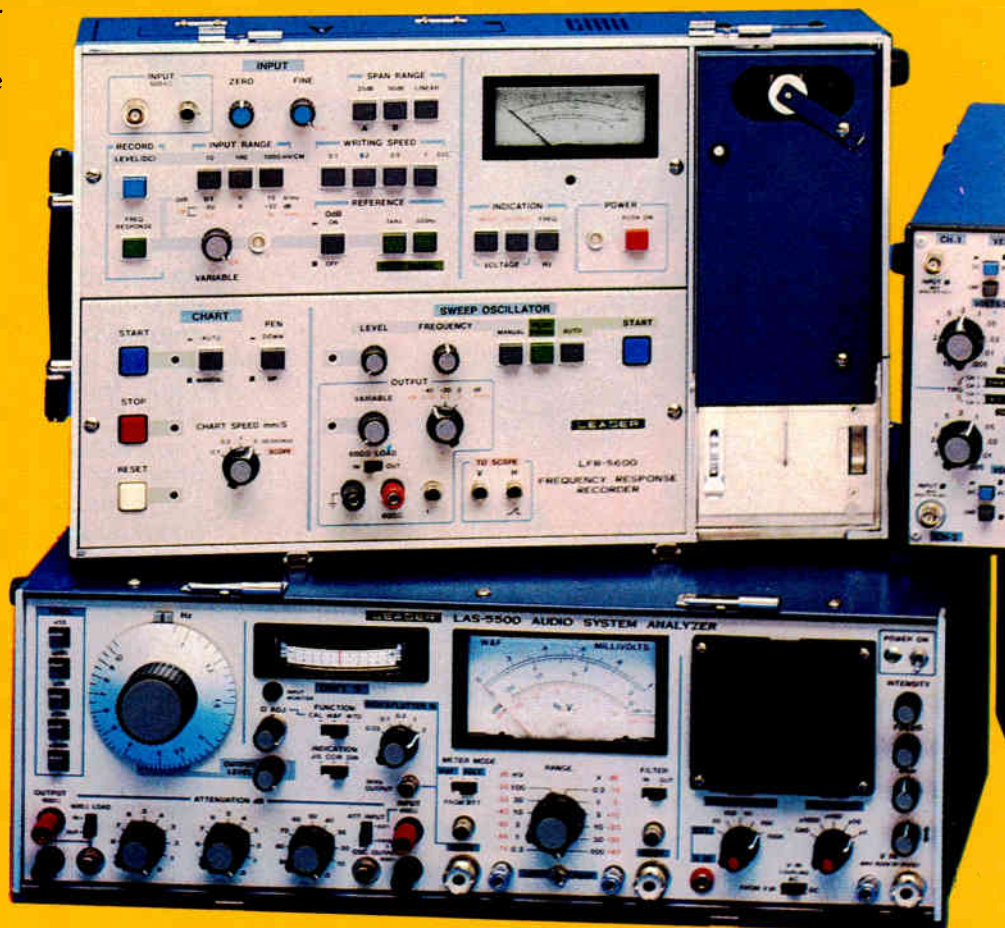

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Blue-light LED joins red and green chip in package

by Charles Cohen, Tokyo bureau manager

Silicon carbide LED puts out blue at 480 nm with 3.5-V drive; red and green LED is multilayer gallium phosphide

A **full-color** light-emitting-diode lamp capable of emitting red, green, and blue and the colors in between—that is, the entire gamut of colors needed for television and other displays—will be shown by Sanyo Electric Co. at the upcoming Japan Electronics Show, to be held Oct. 7–12 in Osaka.

The new devices should initially prove invaluable in a wide variety of applications from full-color indicators to graphic displays, where their performance will more than make up for their higher cost than ordinary LEDs. It may be a while, though, before commercial flat-panel full-scale TV displays with 13,000 to 26,000 of the devices are offered for sale.

Two chips are sealed into each LED to provide its full-color performance. One of the chips, which emits blue light at 480 nm, has just been developed. It uses two liquid-phase epitaxial layers of silicon carbide on a silicon carbide wafer. The other chip, which emits green light at 565 nm and red light at 700 nm, has four liquid-phase epitaxial layers of gallium phosphide on a gallium phosphide substrate. Four leads, one of which is common, make it possible to independently control the brightness of the three colors.

Brightness of the blue chip is about 2 millicandelas at a current of 20 mA. The driving voltage must be about 3.5 V because of the large band gap in silicon carbide. Although this is almost double the voltage drop of red and green devices, it is only about half that of metal-insulator-semiconductor devices ex-

Twentieth Japan show fills five halls

The six-day Japan Electronics Show, the twentieth, will be the largest held so far in Osaka when it opens its doors on Oct. 7. It will also be the first in which the foreign firms, 170 of them in 134 booths, will be distributed throughout the show, rather than concentrated in a foreign exhibitors' ghetto as at past shows.

This year there will be a total of 421 exhibitors in 1,278 booths, up from 320 exhibitors in 933 booths at the Osaka show two years ago. At last year's show in Tokyo, the site of the show in even-number years, there were 477 firms in 1,400 booths—for the largest show ever.

Leading the parade of foreign firms will be the U. S. with 101 firms, followed by West Germany with 28 firms, England with 11, Taiwan with 9, Switzerland with 8, and Hong Kong and France with 3 each. There will be one firm each from Canada, Finland, Sweden, Denmark, Norway, and Australia. Furthermore, electronics industry associations from France, Norway, and Australia will have public relations booths.

Last year there were a total of 3,700 overseas visitors from 98 countries. The largest contingent was 1,346 persons, or 36.5% of the total, from Asia. The largest single country delegation, though, was the United States with 21% of the total. Other regional groups visiting were Western Europe, 27.2%; Central and South America 4.7%; Pacific Oceania 3.3%; Mideast 2.7%; Africa 2.4%; and Eastern Europe 2%.

There will be a total of five halls at this year's show, with the first hall devoted to promotional films shown on video projectors. As in last year's show, components and consumer products will be featured, with many domestic test equipment manufacturers opting for private shows. The second hall will feature consumer electronics; the third, components; the fourth, semiconductors and assembled equipment; and the fifth, industrial equipment, including test equipment together with still more components. There will also be displays of text-multiplexing television and electromechanical actuators and sensors put on by the Japan Electronics Show Association, which sponsors the show.

This year video disks, digital audio disks, and TV cameras will be featured in the consumer hall, which is also expected to emphasize personal computers and microprocessors in the consumer electronics, equipment, and semiconductor booths.

However, most test and measuring equipment manufacturers will be saving their important new product introductions for the international exhibition sponsored by the Japan Electric Measuring Instruments Manufacturers Association, to be held in Tokyo from Oct. 19 through 23 at the Tokyo international fair grounds. Audiophiles will also have a show in Tokyo in October. The 29th all-Japan Audio Fair will be held at the Tokyo international fair grounds from October 15-19.

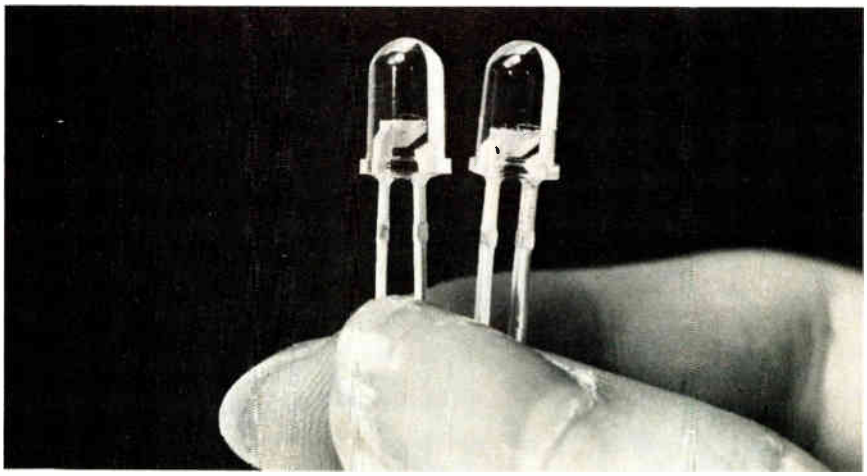
perimentally fabricated by others—including a gallium nitride device made earlier this year by a subsidiary of Matsushita. The quantum efficiency of Sanyo's blue device is also reasonable.

The silicon carbide LEDs are fabricated by a proprietary process on wafers about 15 mm on a side. One key to their moderate price is the relatively large wafer—single-crystal silicon carbide is not easy to make, but Sanyo managed to do so.

Successive n and then p layers are grown on each wafer by liquid-phase epitaxy from a silicon melt in a carbon boat—which provides the carbon. Nitrogen is the dopant in the n layer, aluminum the dopant in the p layer. The firm will not say what metal it uses for ohmic contacts, but says the chip size is on the order of 250 to 300 μm on a side—about on a par with other LEDs.

The red and green LED chip consists of an n-doped gallium phosphide substrate with four successive epitaxial layers. The first n layer grown on the substrate is doped with zinc and nitrogen, the second with sulphur and nitrogen. Ohmic contacts are made at the substrate, the central p region, and the second n-doped layer.

Forward current through the junction between the first p and the first n layers produces red light, which is transmitted almost unattenuated through the overlying layers. Forward current through the junction between the second p and n layers produce green light. Green light output is about 3 mcd at 10 mA, which corresponds to a driving voltage of about 2 V. Red light output is 3 mcd at 5 mA, which corresponds to a driving voltage of about 1.9 V.



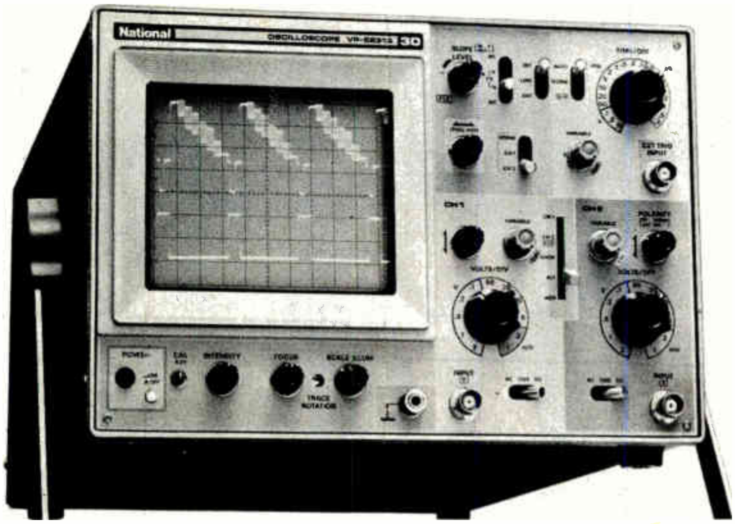
Sample price of the red-green LEDs is $2.20, that for blue LEDs only $1.32. A Sanyo spokesman says that the two-color gallium phosphide units—with no blue chip—when purchased in quantity should cost less than twice the price of two single-color LEDs.

Sanyo Electric Co. Ltd., 2-18 Keihan Hondo-ri, Moriguchi, Osaka 570, Japan [441]

Dual-trace scopes have 1-mV/division sensitivity

Matsushita Communication Industrial Co. is introducing at the 1981 Japan Electronics Show the Panascope series of dual- and single-trace oscilloscopes, including the 15-MHz VP-5215A single-trace unit and the 15-MHz VP-5216A, 20-MHz VP-5220A, and 30-MHz VP-5231A (shown) dual-trace scopes. All four models have automatic fixed-level triggering for stable waveforms, a sensitivity of 1 mV/division for both channels, sweep rates from 0.2 μs to 0.5 s per division, a sharp-graticule cathode-ray tube with automatic focusing, and trigger couplings for ac, dc, and vertical and horizontal television signals. The mean time between failures specified for the oscilloscopes is 15,000 hours.

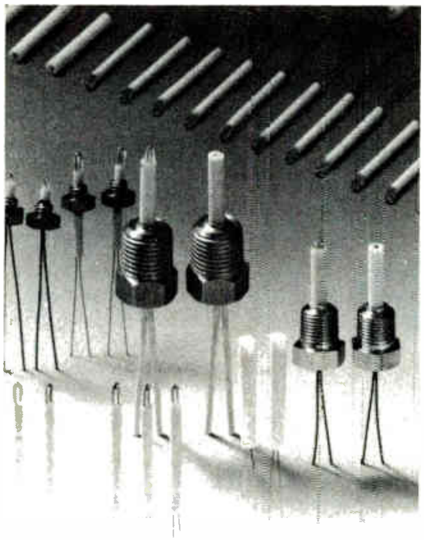
Matsushita Communication Industrial Co., 3-1 Tsunashima Higashi, Kohoku-ku, Yokohama 223, Japan [442]



Measurements of temperature, torque, pressure, or strain made on a rotating engine, motor, turbine, or propeller shaft are transmitted at 30 to 70 kHz for reception at a safer place by the RT-2000 wireless telemeter. Meisei Electric Co., 2-5-7 Koishikawa, Bunkyo-ku, Tokyo 112, Japan [443]

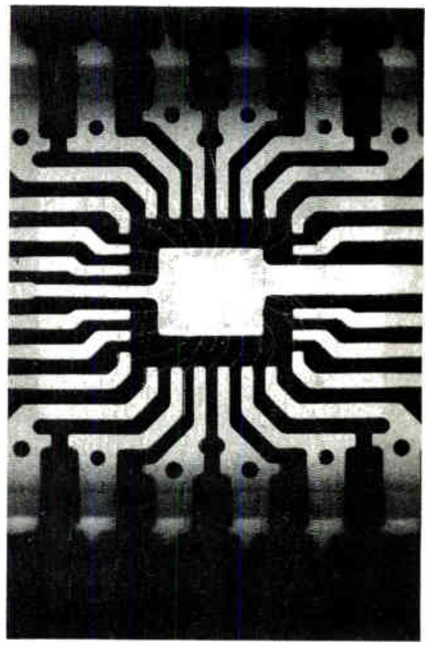
RVF8-series trimmer resistors have molded-resin substrates that eliminate loose terminals and other problems of bakelite substrates. They operate at 150 V dc, maximum, and dissipate 0.1 W at 79°C. Murata Manufacturing Co., 2-26-10 Tenjin, Nagaokakyo, Kyoto 617, Japan [444]

The SP-150 miniature impact dot-matrix printer has a Japan Industrial Standard 128-character set and prints up to 16 characters per line at about 1 line per second. Nada Electronic Laboratory Ltd., 4-13-28 Fukae Kitamachi, Higashi Nada-ku, Kobe 658, Japan [449]



The Neo-thermy high-temperature thermal sensor has electrical characteristics similar to those of traditional thermistors. It is resistant to chemicals, electrolytic corrosion, water, and humidity and responds quickly. Shibaura Electronics Co., 520 Machiya, Urawa, Saitama 338, Japan [454]

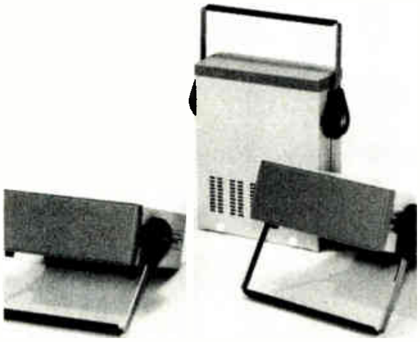
The LPC-5020 and LP-5020 serial dot-matrix label printers put out the 128 characters of the Japan Industrial Standard code in three character sizes at a maximum rate of 1.8 seconds per line. Nada Electronic Laboratory Ltd., 4-13-28 Fukami Kitamachi, Higashi Nada-ku, Kobe 658, Japan [459]



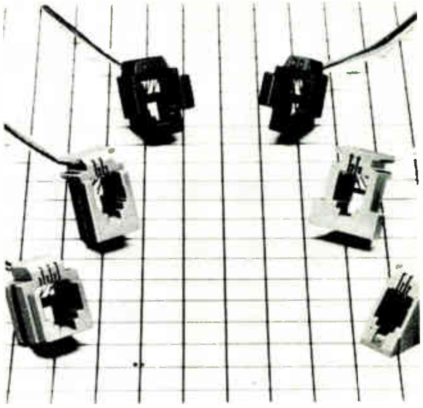
The Soken cabinet X-ray system is used with a specially designed television monitor for nondestructive inspection of the bonding wires of integrated circuits and semiconductors that are over 25 μm in size. Soken Co., 1-7-13 Yaesu, Chuo-ku, Tokyo 103, Japan [461]

Circle 130 on reader service card

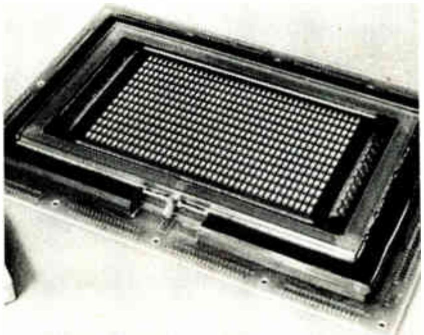
New products international



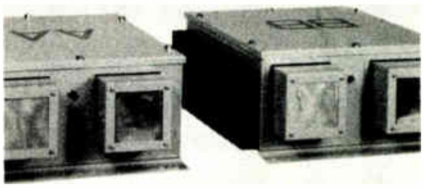
The BE series test instrument cases are portable and will accept several printed-circuit boards. They have an aluminum front panel and a handle that tilts and are available in 235-, 295-, and 360-mm sizes. Settsu Metal Industrial Co., 6-4 Yagumo Nishimachi, Moriguchi, Osaka 570, Japan [455]



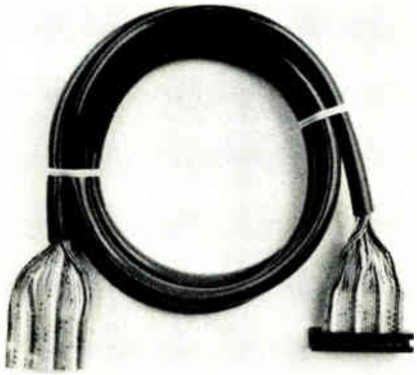
The TM series of connectors can be easily connected to telephones or other small electronic equipment. It is compatible with Western Electric's 616W series and withstands harsh environments. Hirose Electric Co., 5-5-23 Osaki, Shinagawa-ku, Tokyo 141, Japan [448]



The Itron DC40125A is a 480-character vacuum fluorescent dot-matrix display housed in a thin 235-by-145-mm envelope. It has 3.65-mm-high 5-by-7-dot characters and an operating voltage of only 50 V peak to peak. Noritake Co., 3-1-36 Noritake Shinmachi, Nishi-ku, Nagoya 451, Japan [446]



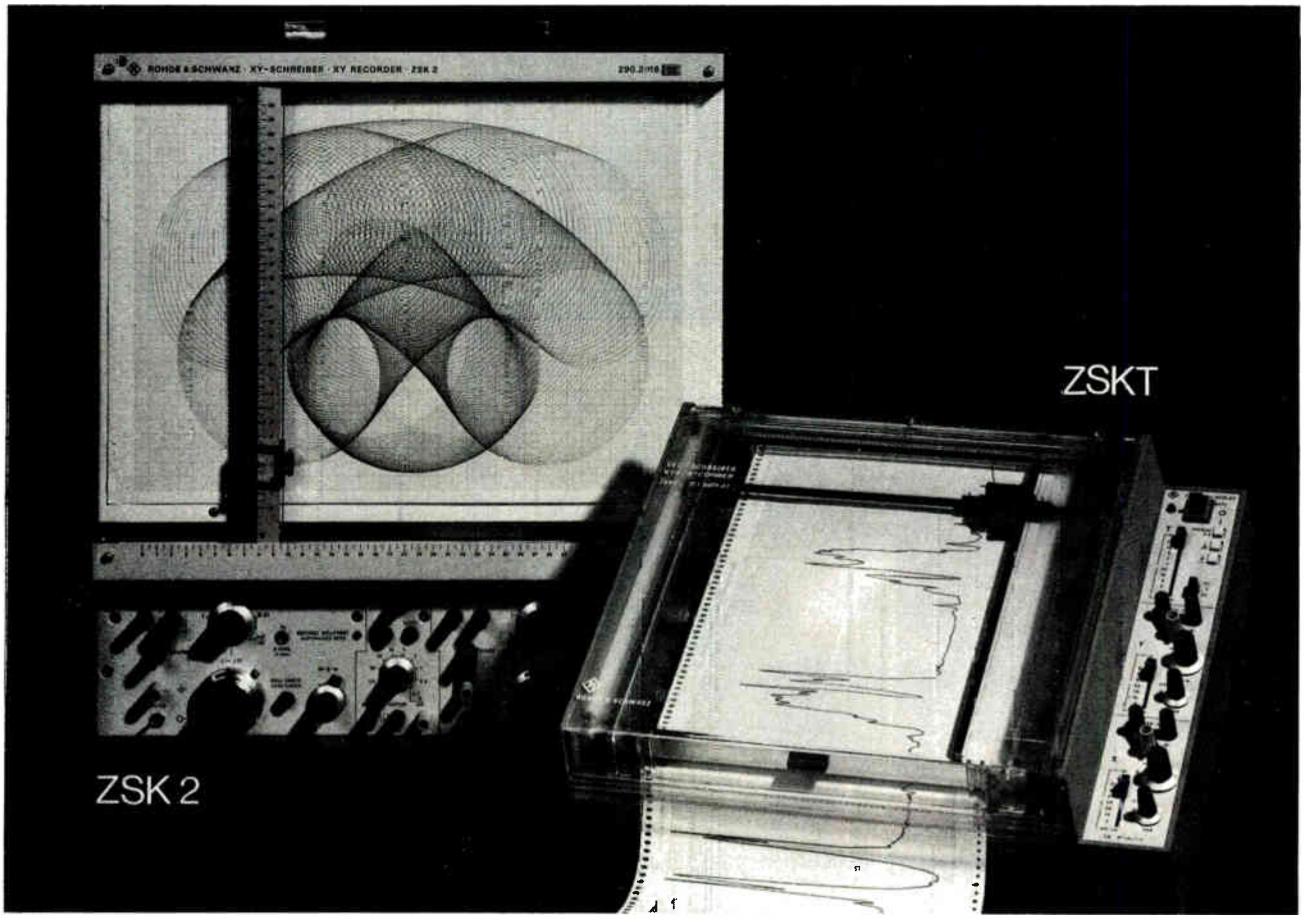
The WK63 Super Guard warns large moving machines such as gantry cranes of travel endpoints with an alarm that can be set between 6 and 15 m. An optional automatic power cut-off switch can stop the machine. Meisei Electric Co., 2-5-7 Koishikawa, Bunkyo-ku, Tokyo 112, Japan [450]



This interface cable is designed to be connected to computers and facsimile and business machines. It is first cut to the required length and then bonded at each end to insulated conductors to form a flat cable. The Fujikura Cable Works Ltd., 1-5-1 Kiba, Kotoku, Tokyo 135, Japan [447]

The PMP-S10-XM inclinometer was developed for mounting in a narrow space. It has a sensitivity of 0.01° maximum, an inclination range of ± 10°, an input voltage of up to 8 V, and operates from 0° to +75°C. Response is in about 0.3 s. Midori Precisions Co., 2-17-1 Kokuryo-cho, Chofu 182, Japan [451]

Versatile, fast and economical



On the basis of just two units Rohde & Schwarz are able to offer a range of recorders to meet all needs. Both have electronically limited writing area, extremely low overshoot of less than 1 mm and the same dynamic characteristics on both axes.

Precision XY recorder ZSK 2
with identical characteristics, independent of position, in X and Y channels. Switchable for format DIN A3 or DIN A4, for YT mode too with a timebase. Writing speed > 110 cm/s in both directions, constant calibrated setting of deflection factor between 10 μV/cm and 5 mV/cm plus controlled zero shift (max. ±1 writing width, up to ±100 cm with external signal). Common-mode voltage 100 to 500 V, DC and AC common-mode rejection 120 to 200 dB.

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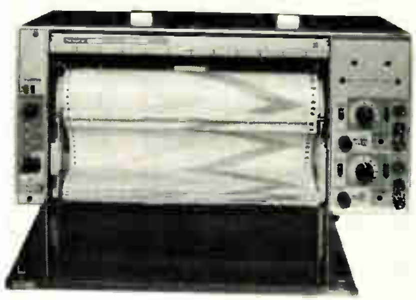
Circle 132 on reader service card

The DA-610 and DRA-610B thermoelectric cooler and power controller is for chemical-vapor deposition on wafers. It has a range of −8° to +70°C, regulation within ±0.15°C and ±0.5°C distribution. Komatsu Electronics Inc., Fuji Bldg., 3-7-4 Kasumigaseki, Chiyoda-ku, Tokyo 100, Japan [452]

The V8EK-PV trimmer potentiometer consists of a carbon-resin film on an epoxy-glass substrate for resistance to heat and humidity. These 500-Ω-to-1-MΩ resistors have ratings of 0.1 W and 100 V. Teikoku Tsushin Kogyo Co., 335 Kariyado, Nakahara-ku, Kawasaki 211, Japan [453]



The VP-6223A pen recorder has a dc-type thermo-control circuit for a high thermal response and therefore sharp traces. Felt pens can be used for multicolored recordings. Matsushita Communication Industrial Co., 3-1 Tsunashima Higashi, Kohoku-ku, Yokohama 223, Japan [445]

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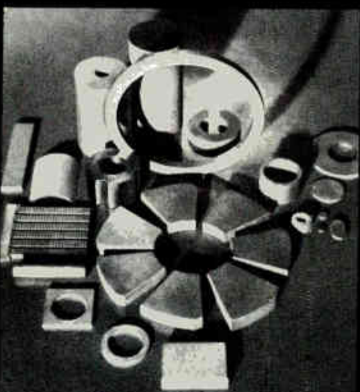
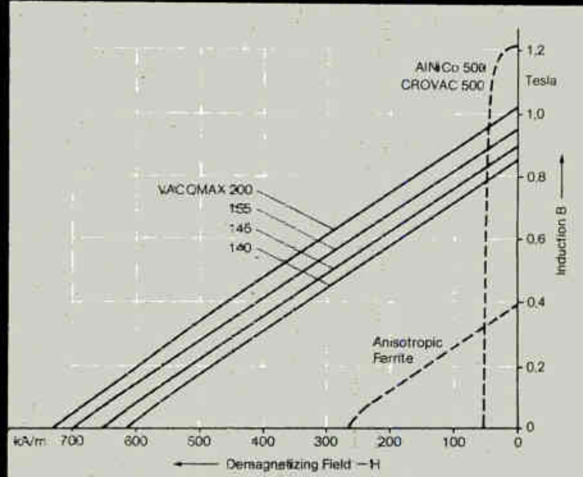
For further details see our Company Leaflet M 040.



M-2e



Characteristic curves of **VACOMAX** (in comparison with other permanent magnet materials).

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Cable: Vacuum Hanau

Telex: 04 184 863
Phone: (06 181) 362-1

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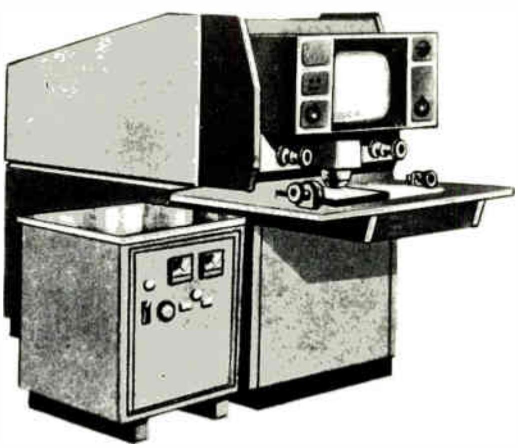

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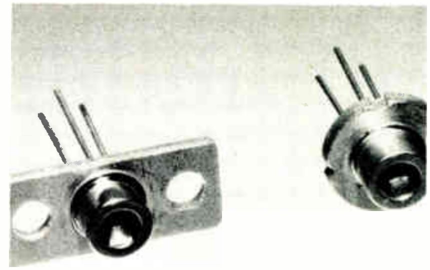
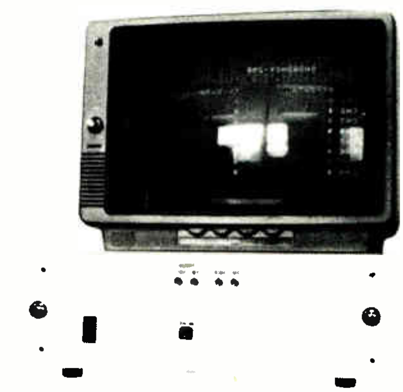
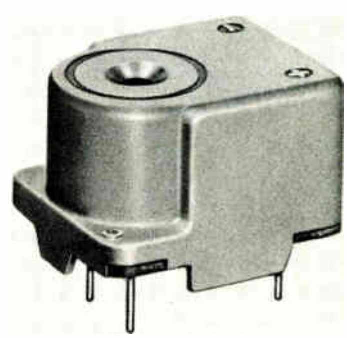
New products international



The HL7801E and HL7801G laser diodes are used as a visible light source for optical audio- and video-disk players. They have a wavelength of 780 nm, a maximum output of 5 mW, and an expected life of at least 100,000 hours. Hitachi Ltd., 1-5-1 Marunouchi, Chiyoda-ku, Tokyo 100, Japan [456]



The MM-16 multiplexing modem accommodates 16 channels with data rates up to 9,600 b/s and transmits them through an optical-fiber cable at 2 Mb/s for a distance of up to 2 km. Showa Electric Wire & Cable Co., Toranomon Bldg., 1-1-18 Toranomon, Minato-ku, Tokyo 105, Japan [457]



The KMB-06 and −12 miniature buzzers produce clear 2,000-Hz sounds through a built-in speaker. They can be driven by a small input signal. The KMB-06 operates on 4 to 8 V and the KMB-12 on 8 to 16 V. Star Manufacturing Co., 194 Naka Yoshida, Shizuoka 422-91, Japan [458]

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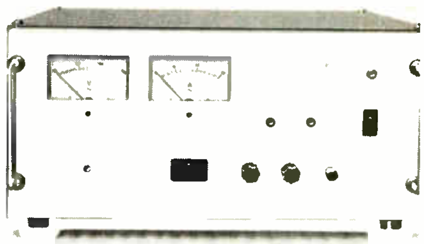
Single-Chip microcomputers from Siemens

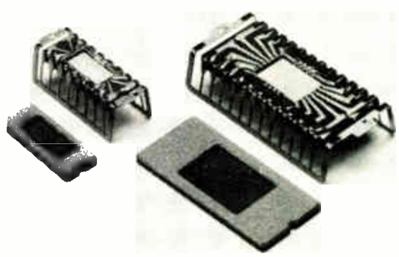
Circle 137 on reader service card

New products international

The VP-8179A a-m/fm signal generator has a frequency range of from 10 kHz to 240 MHz and an output of 0.1 μV to 4 V root mean square. Fm distortion is lower than 0.01%. Matsushita Communication Industrial Co., 3-1 Tsunashima Higashi, Kohoku-ku, Yokohama 223, Japan [460]



The YHR-1K 1-kVA voltage regulator uses a fast waveform-correcting power amplifier. It requires a single-phase input of 110 or 220 V ±10% for an output of 110 or 220 V ±0.1%. Yamabishi Electric Co., Takahashi Bldg., Higashi San-gokan, 3-3-3 Tenjin Bashi, Kita-ku, Osaka 530, Japan [462]



Low-alpha ceramics are used with ceramic dual in-line packages for high-density random-access memory devices to prevent soft errors. The material has an alpha radiation emission of 0.03 count/h/cm². Narumi China Corp., Narumi-cho, Midori-ku, Nagoya 258, Japan [463]

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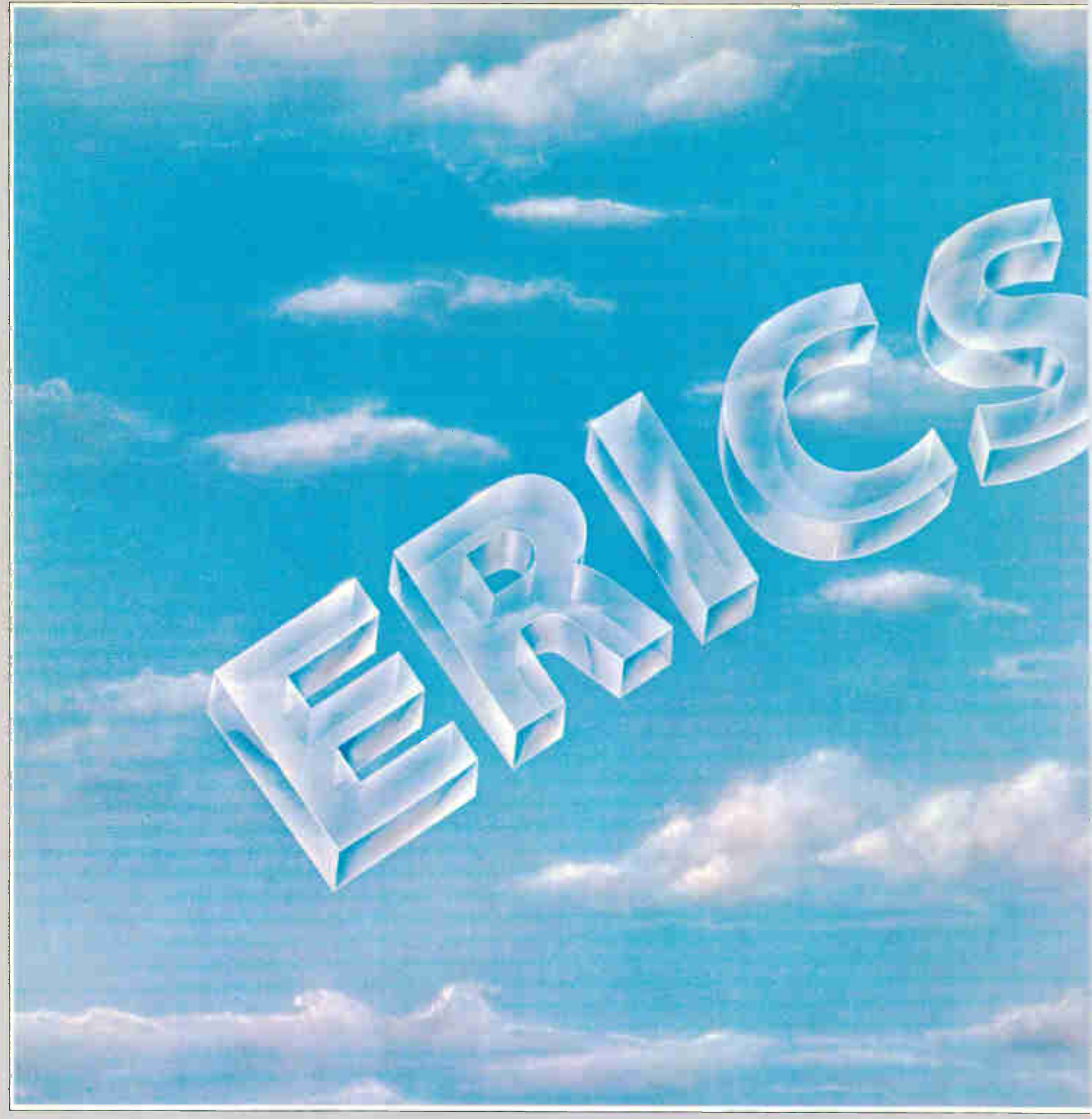

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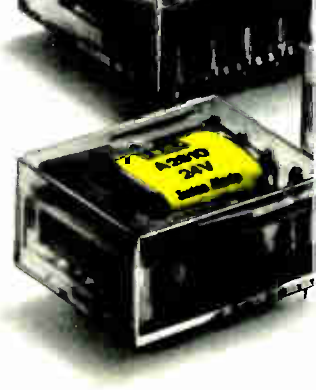

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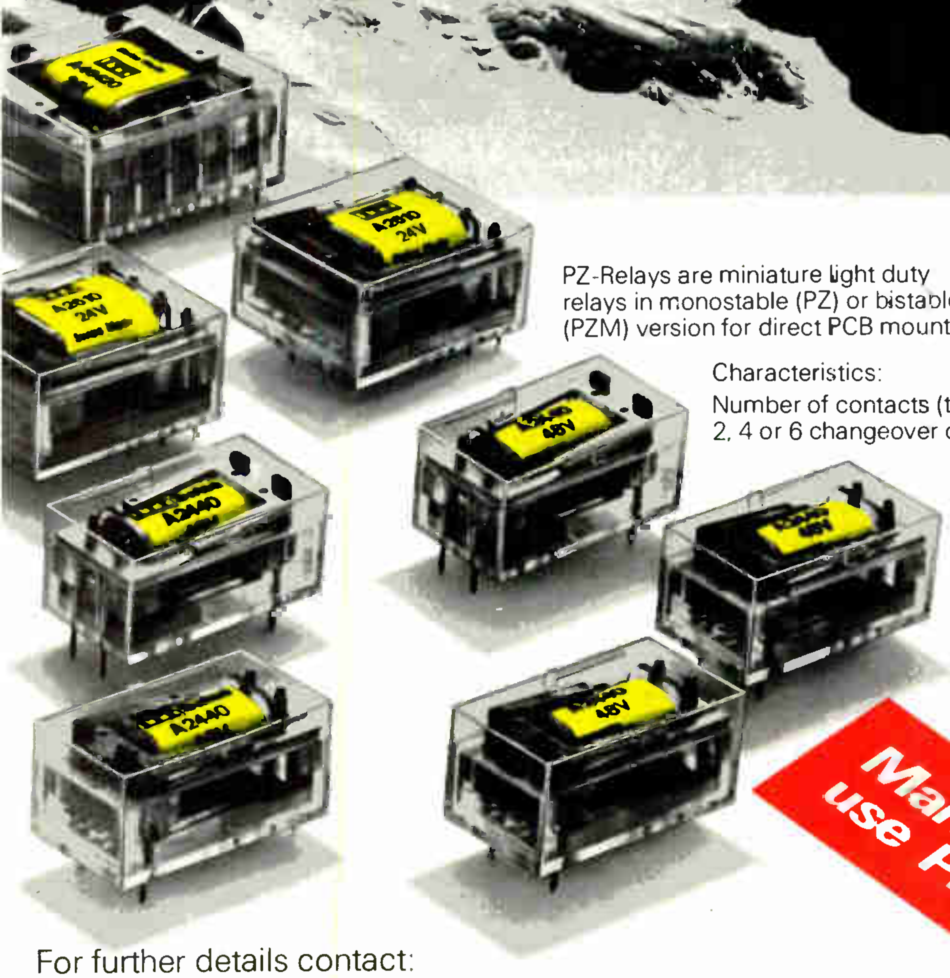

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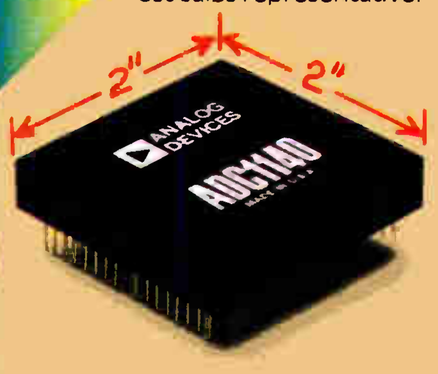

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9/16
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And now there's TMS9995 — for all those tough tasks that demand 16-bit speed and processing power.

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TMS9995—Key features

- 16-bit CPU
- 12 MHz clock with on-chip clock generator
- 256-byte on-chip RAM
- 16-bit on-chip interval timer/event counter
- 7 levels of vectored interrupts
- instruction prefetch
- automatic first wait-state generation
- MID — macro-instruction detect interrupt
- single 5-V power supply
- 40-pin dual-in-line-package.

Performance plus

Three times faster than the TMS9900, TMS9995 executes a 16x16-bit multiply in just 7.67 µs. A 32-bit number divided by a 16-bit number in just 9.33 µs. TMS9995 can run with 120-ns access time memories, or by using automatically generated wait states, 450-ns access time memories.

256-bytes of fast on-chip RAM is organized as 128 x 16-bit words, allowing a full 16-bit word access in one clock cycle.

And, TMS9995 uses an intelligent pipelined architecture where the op code of the next instruction to be performed is prefetched. For example, the microcode for Branch and Jump instructions direct TMS9995 processors to prefetch the true next instruction instead of blindly prefetching from the next sequential memory location.

And now, a word about memory-to-memory architecture

The innovative architecture at the very heart of the 9900 Family reaches it's performance peak in the TMS9995 thanks to on-chip RAM. Comparison of execution speed benchmarks clearly show the advantages.

Support, support, support.

Necessary for any microcomputer family. TI's 9900 Family is supported by Pascal, Basic and Fortran software and software and hardware development systems, including a low-cost Evaluation Module, TMAM6095, for $800.* TI also offers training, documentation and expert field assistance. Training, service and design assistance are available at Distributor System Centers, and TI's Regional Technology Centers.

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The continuing introduction of new, advanced, high-performance 9900 Family CPUs, with TI's state-of-the art technology and production-proven resources, clearly demonstrates a commitment to leadership. To choice. To the future.

For more information about the new TMS9995, or any other 9900 Family member, contact the TI distributor or field sales office nearest you, or write to Texas Instruments, P. O. Box 202129, Dallas, Texas 75220.

Execution Time Benchmarks

	Automated Parts Inspection (Seconds)	Computer Graphics XY Transform (Seconds)	Bubble Sort (Millisec)	Block Translation (Millisec)	16 Bit Multiply (Microsec)	Single Vectored Interrupt (Microsec)
9995 (12 MHz) w/120ns PROM	0.666	0.863	1.240	1.767	10.00**	8.0
9995 (12 MHz) w/450ns EPROM	0.950	1.081	1.956	2.696	12.67	10.67
8088 (5 MHz) w/450ns EPROM	1.596	2.402	2.254	1.522	40.8	77.6
6809 (2 MHz) w/450ns EPROM	9.67	57.1	2.376	3.01	91.9	27.6

Benchmark algorithms from Intel Application Note AFN01551A.

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**7.67 µs if multiplicands do not have to be saved

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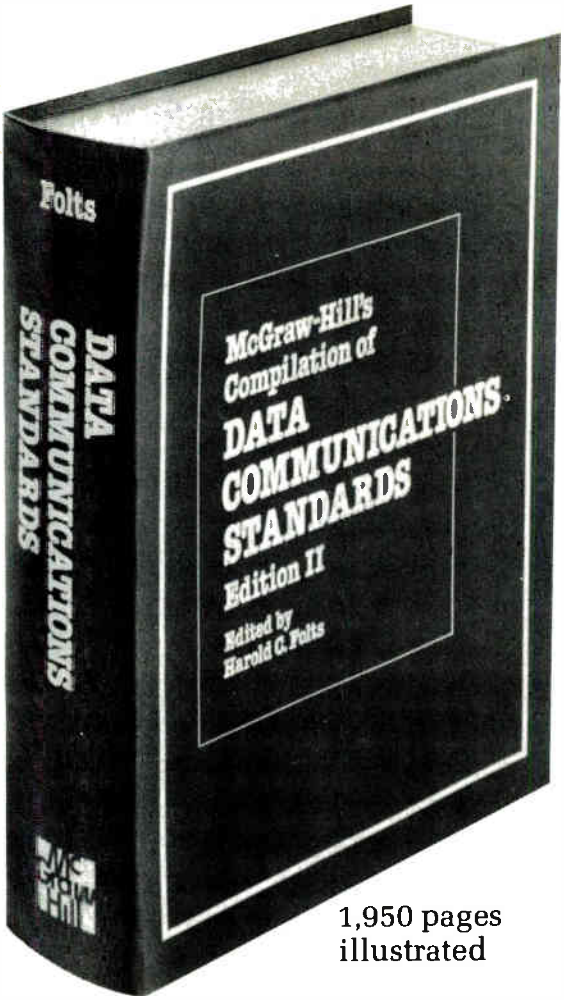

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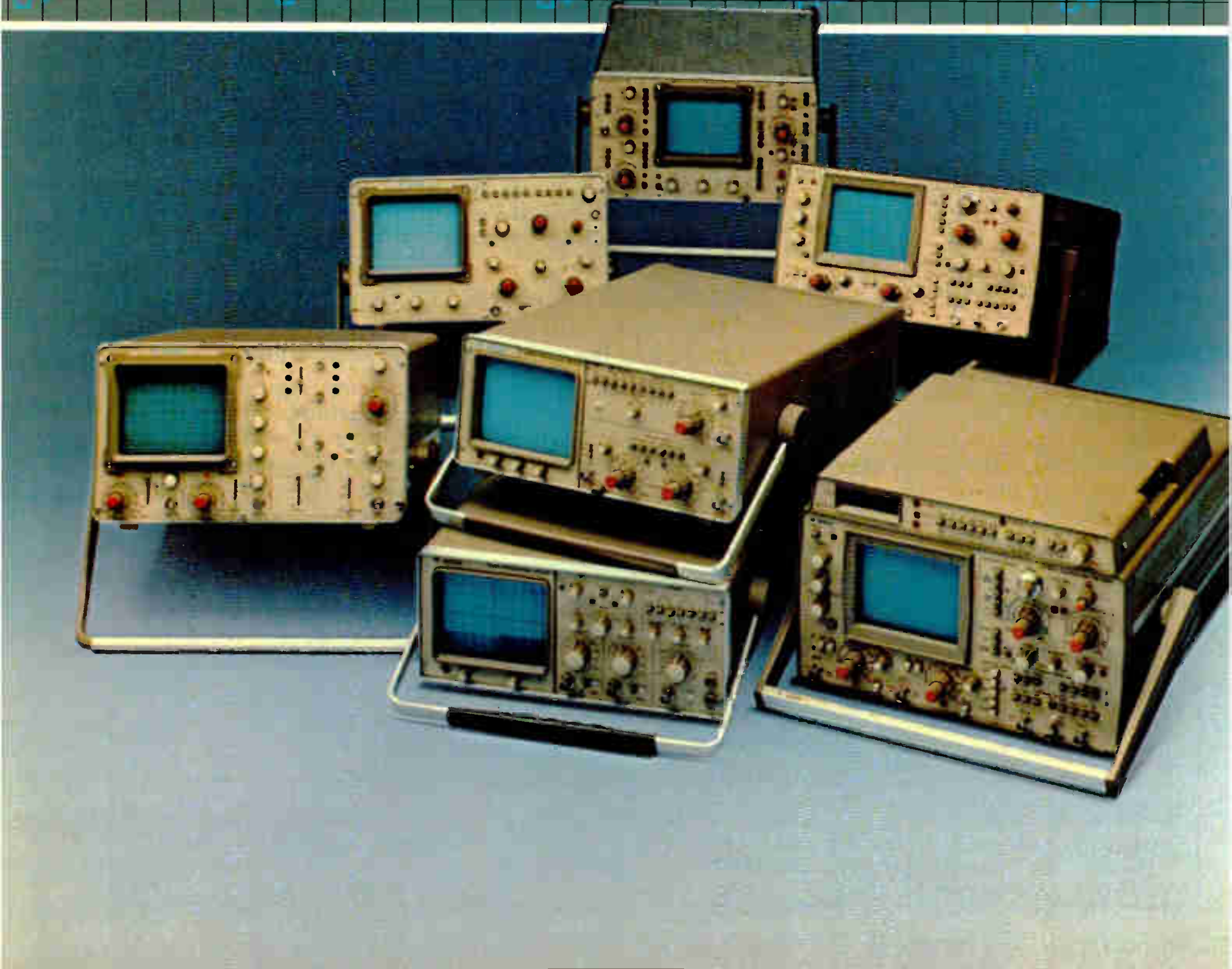
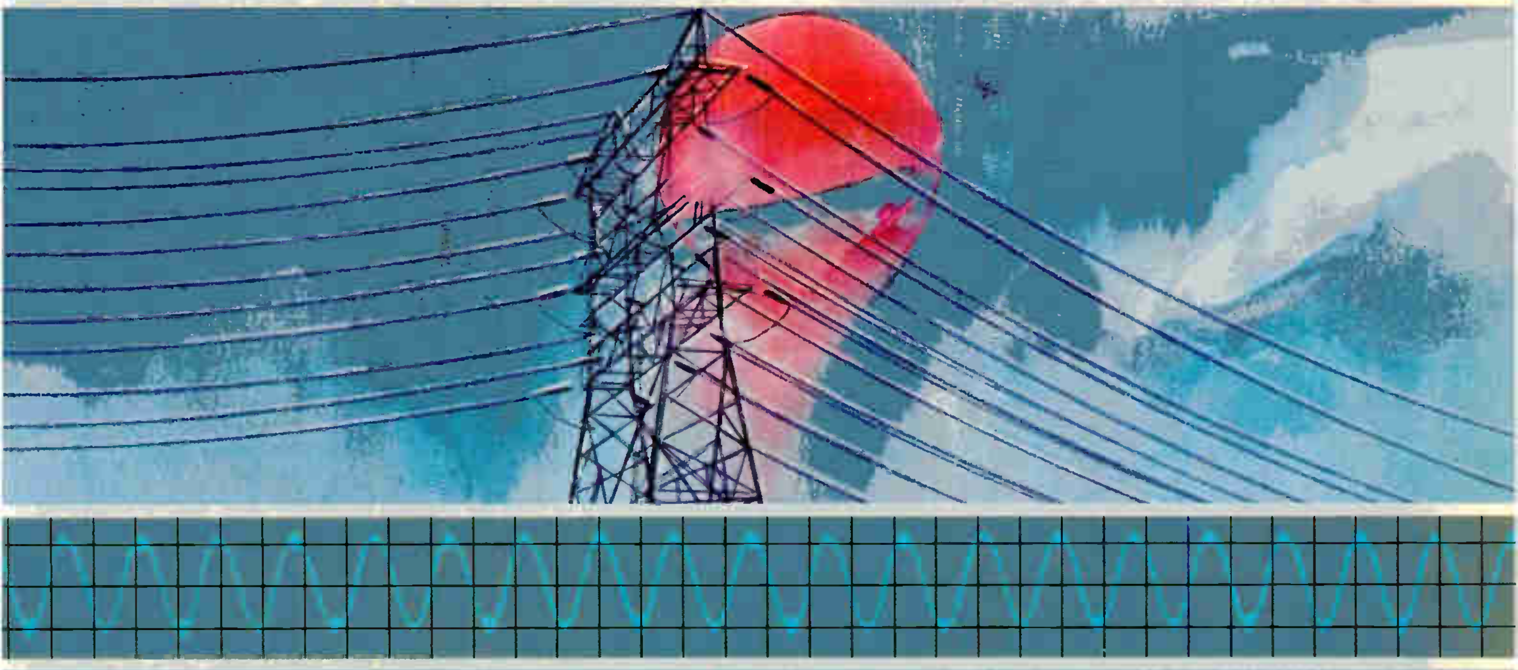


to high-voltage transmission.



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Circle 110 on reader service card

Japanese rush to robot production

19,900 produced in fiscal 1981 as workerless plants proliferate; MITI pours $57 million into project to add lasers to systems

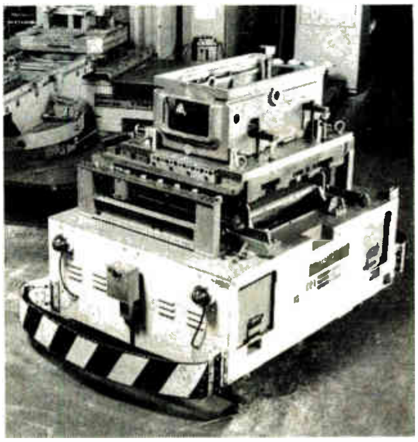
by Robert Neff, Tokyo bureau

Manless plants, flexible manufacturing systems, computer-aided manufacturers—those are today's buzz words in Japan, where industry is artfully melding data processing and robotics to fashion the world's most advanced factories.

Although the first applications of such systems have tended to be in metalworking plants, major electronics firms like Toshiba Corp., Hitachi Ltd., and Nippon Electric Co. are moving to adopt them. The irony is that while U. S. executives are flocking to Japan to learn blue-collar management techniques, the Japanese are building plants that all but obviate workers.

The results are striking. At its highly publicized robotized Fuji plant that opened in January, Fujitsu Fanuc Ltd. is turning out 100 robots per month with about 100 workers, one fifth the number previously required. At a new factory in Hokkaido, where 50 workers turn out 800,000 cutting-tool inserts per month, Sumitomo Electric Industries Ltd. has achieved similar labor savings. What Toshiba Tungalloy Co. calls its new programmable precision manufacturing system turns out about 1,500 cutter bodies per month with 16 workers and 6 machine sets covering just 350 square meters, against a conventional 70 workers and 50 machine sets scattered over an area of 1,480 m^2. The installation operates at full tilt throughout the night without a single worker on site.

Future rosy. With all this, Japanese robot makers are anticipating a tenfold increase in sales by 1990. According to industry sources, in the fiscal year ended March 31, sales totaled 19,900 robots worth $340 million. The dollar value was almost double that of the previous year, when 14,000 units were turned out. Exports account for just 2% to 3% of the total sales, most of that to the U. S. The same industry sources says that in the 1980 fiscal year, the U. S. built 3,250 units; West Germany, 850; Sweden, 600; Italy, 500; and Britain, 185.



On its way. Murata Machinery's FMS, for flexible manufacturing system, features these driverless vehicles that move about the factory guided by wires implanted in floor.

"Today's small plant is making different products in small batches every day," says Shotaro Ozaki, director-general of the production engineering department at the Ministry of International Trade and Industry's mechanical engineering laboratory. "The issue is to automate them, which we call making them flexible"—hence the term FMS for flexible manufacturing system. The FMS payoff: efficiencies of mass production in small-lot manufacturing of diverse products.

Experts do not agree on exactly what constitutes an FMS, but a general definition would include several robot-equipped numerically controlled machine tools or machining centers linked to each other and a warehouse by some form of automatic materials-handling device. A central computer monitors and controls all operations, stopping and starting the system automatically.

Robots at the warehouse load driverless carts or conveyor belts with metal blanks or other raw materials for conveyance to the appropriate work site. There, a robot unloads the materials and inserts them into the machine tool. Then, when the machine finishes its work, the robot replaces the part onto the conveyor belt or cart for return to the warehouse or to another work site.

Few human jobs. By this definition, Sumitomo Electric and Toshiba Tungalloy cannot boast a pure FMS because they lack automatic materials handling. But experts regard their plants as very advanced in computer control and flexibility. In the ultimate FMS, humans need only feed production schedules into the central processor and make tapes to guide the numerically controlled machine tools.

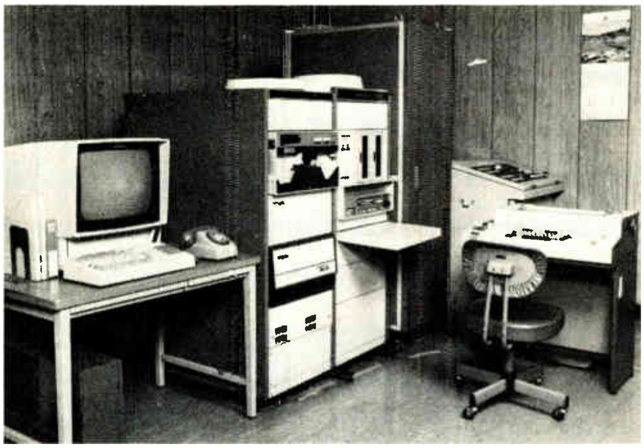
"Japan is the most advanced country in FMS," boasts MITI's Ozaki. And it is spending prodigiously to stay ahead. MITI is pouring $57 million into a seven-year project headed by Ozaki to develop a "flexible manufacturing system complex provided with a laser." Twenty Japanese companies are sharing in the largesse. The goal is a system that will build machine subassemblies weighing up to 1,100 pounds in maximum lot sizes of 300 and take only half as much time to produce as with conventional systems. MITI also subsidizes the design of other systems, such as Toshiba Tungalloy's.

The Japanese do not disguise their fear of being overtaken by the U. S. in FMS. Ozaki notes that the U. S. Air Force is spending $175 million to $220 million on an integrated computer-aided manufacturing (ICAM) project for making aircraft fuselages. "We're jealous of the U. S. investment in ICAM," says Koichi Wakasugi, general manager for technical operations at Hitachi Seiki, one of Japan's major FMS suppliers. "Without national backup, we can't develop the linkage between computer-aided design and computer-aided manufacturing that is so important."

Partly for this reason, several companies with the most advanced FMS plants in Japan strictly prohibit visitors. But Murata Machinery is glad to show off its "operatorless conveyance system" largely because it wants to market it. Central to the system are driverless carts that move about the factory floor, guided by wires implanted in the floor and linked to the central computer. Competitor Wakasugi of Hitachi Seiki calls it "wonderful."

More efficient. Murata is marketing similar systems for $650,000. They include two driverless carts, pallet changers, and software, which engineering director Tadataki Shiomi says accounts for about half the price. The payoff, Murata claims, is two to three times more efficient use of equipment, since it can be operated 24 hours a day, and huge labor savings. Murata's spindle running time, for example, has increased to 600 hours per month from the previous 250 hours.

Shiomi is still not satisfied, though, and says it will take another two years for Murata to perfect its operatorless system. One thing he wants more flexibility in automatic tool changing. Conventional horizontal machine centers can hold only 40 to 60 different tools and vertical models only about 20. "This is absolutely too few" to produce 1,500 parts, he says. "Tools now must be changed by humans, so at night we can only make goods that don't require tool changes. That limits flexibility." So Murata is developing a system whereby sensors at each machine center will alert the central computer that a tool not held in the center's magazine will be needed for the part being processed. The computer will order a driverless vehicle, on which a robot will be mounted, to bring the proper tool from the warehouse. "When we solve these problems, we have the ideal FMS," Shiomi concludes. He also disdains systems using tram cars or conveyors to move parts and materials as "full of defects." They are less flexible than operatorless vehicles, he says.



Nerve center. This is the central computer control station for the Murata FMS. The firm markets a operatorless conveyance system.

But even systems without automatic materials handling can achieve quantum leaps in flexibility and economy. Sumitomo Denko's $7.4 million Hokkaido plant, for example, has cut the work force and lead times by 80%. "We don't use automatic carts because we don't have enough production to justify them," explains Tadamasa Sho, chief engineer of the company's alloy production department.

The key feature of Sumitomo Electric's insert-making system is the combination of batch and flow processes into one operation: processes that once occurred in different buildings are all under one 3,800-m^2 roof. Computerized automation has essentially replaced people in such functions as inspecting and adjusting the thickness and weight of compacted items, monitoring and controlling sintering and vacuum conditions, recording and analyzing inspection results, and controlling powder inventories. Robots and other automatic equipment handle materials, load machines, and package the final product.

Toshiba's plans. Plans by Toshiba Corp. dramatize what FMS can mean to the electronics industries. Starting this fiscal year, Toshiba has embarked on a three-year, $220 million FMS binge that will bring FMS to 35 production lines at Toshiba computer, semiconductor, telecommunications, and consumer-electronics plants. The 2,500 workers now employed on those lines will fall to 500 by March 1984 with no reduction in production volume or quality.

But that is just for starters. Ultimately, Toshiba expects FMS to cut its production workforce by 10,000 persons to 15,000. Most of the freed-up workers will be assigned to software production.

Such plans are music to the ears of FMS designers and suppliers, who have waited a whole decade for a market to develop. Since supplying its first FMS line nine years ago, for example, Hitachi Seiki has 12.

Shiomi at Murata, though, sees promising prospects. His firm expects to sell 40% more driverless carts than the 100 it sold last year. And since April, Murata has received more than 1,300 requests to view its pilot operatorless system.

Experts agree that a key stimulus to FMS sales will be adoption of standardized software, which would cut costs and reduce confusion. The Japanese worry that the U. S. is progressing far more rapidly toward this end, jeopardizing Japan's present lead in FMS. "Japan as a country is not moving toward standardization of software and information," laments Wakasugi of Hitachi Seiki. "The U. S. is frightening." □

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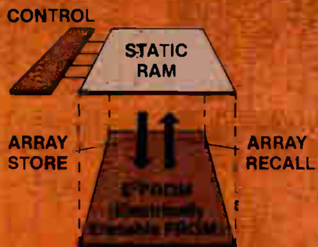

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Avionics

Program blends air firepower, safety

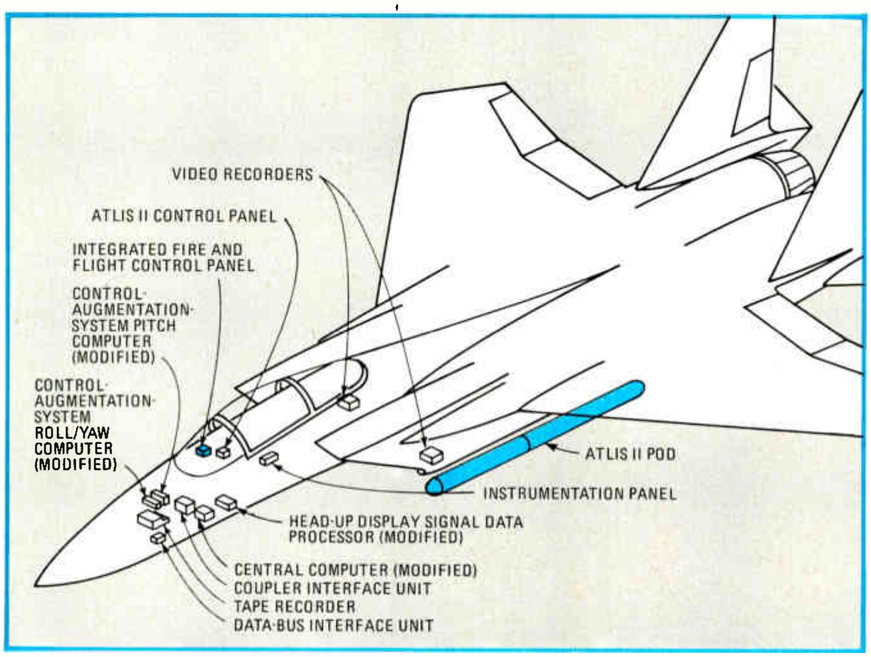
Integrated flight- and fire-control effort aims to permit fighter pilots to take evasive action while firing accurately

by James B. Brinton, Boston bureau manager

An F-15 now flying at Edwards Air Force Base in California is setting the pace for the computer-aided fighters of the 1980s and 1990s. As part of the Air Force's Integrated Flight- and Fire-Control (IFFC) program, this F-15 takes data from a target-tracking pod slung under its fuselage to generate flight and weapons-control commands that make it more potent and enable it to survive longer. There is also a good chance that this combination of lasting longer and fighting harder may trigger a retrofit of the IFFC techniques now in development to current aircraft, opening a new avionics market.

Today's fighter pilot hoping to hit his adversary must fight and fly while maneuvering an aiming point, or pip, on his head-up display onto the target that he sees on the same display—no mean task in a dogfight. On bombing runs, he must keep a velocity-vector symbol on an azimuth-steering symbol. In practice, this means flying over the target with wings level. While wings-level delivery is accurate, more experienced pilots prefer the greater safety, if lower accuracy, of tossing ordnance at a target, bobbing and weaving to avoid ground fire.

With IFFC, both missions become simpler and more effective. Target range and bearing data from the IFFC pod are converted into aircraft-control and bomb-release commands. Now a pilot can give full or partial control of the plane to its on-board digital computers; the system can "aim the aircraft" for him.



Vital pod. A key to the effectiveness of the Air Force's new Integrated Fire- and Flight-Control program is the Atlis II pod containing lasers and a video camera.

If he faces heavy counterfire, he may retain some flight control and fly evasively while IFFC takes care of accurate firing.

IFFC is an advanced development program, not one aimed at developing operational hardware. But according to its managers in Ohio at the Flight Dynamics and Avionics Laboratories, Wright-Patterson Air Force Base, some form of IFFC is likely to appear on new fighter-bombers, and already early results from the IFFC program are being fed into the Air Force's Advanced Fighter Technology Integration program.

Far better. It is easy to see why the Air Force is enthusiastic about IFFC. Simulations performed by General Electric Co. project huge improvements in performance. In air-to-air gunnery, the Air Force expects:

- Four times the number of gun-firing opportunities.
- Three times the number of hits.
- A halving of the time to first hit on a target.

In air-to-surface gunnery, rounds would remain on target, and on bomb runs bomb accuracy would double, even though the aircraft would be able to move much more freely to evade fire. Giving the advantage of speed and maneuver back to the attacker could result in a tenfold increase in a plane's probability of surviving linear-predictor–directed ground fire.

It all adds up. An enemy plane is four times as likely to be fired upon in a dogfight, is three times more apt to be hit each time, and comes under fire sooner than formerly possible. An Air Force fighter becomes perhaps 12 to 24 times more lethal than

a similar plane without IFFC, and the chances of an enemy surviving an encounter with an IFFC-equipped aircraft fall sharply.

Force multiplier. Thus, James E. Hunter, the IFFC program manager, considers the concept a powerful "force multiplier." The effect is as if a single plane suddenly had the fighting power of many and as if all pilots were aces.

The technology needed to implement the advanced development version of IFFC did not prove to be exotic, and some was even available off the shelf. Moreover, as such modifications go, those needed to adapt the F-15 aircraft to IFFC were straightforward.

The bulk of the $24 million IFFC effort was contracted to the Aircraft Equipment division of GE in Binghamton, N. Y., and to McDonnell Douglas Corp.'s McDonnell Aircraft division in St. Louis. In addition to earlier systems-definition and -simulation work, GE acquired a Martin-Marietta Atlis II (automatic and laser illumination system) target-tracking pod.

The pod supplies target range, rate, and bearing data. GE-supplied processors and software reduce this data and couple it into the F-15's fire-control electronics. McDonnell-supplied gear couples flight- and fire-control system electronics and adapts the F-15's control augmentation computers to accept IFFC inputs. McDonnell also did the job of integrating the IFFC system.

IFFC's most visible element is its Atlis II. Originally developed by Martin for ground-attack missions, Atlis also tracks aircraft despite maneuvers or brightness variations caused by clouds or sun glint. Though some modifications were needed, Atlis basically came off the shelf. It contains a video camera, laser ranger, laser target designator, and a laser spot tracker; its optical tracking system can focus to a field of view as narrow as 1°, and "look" at angles as much as 160° away from the line of flight.

In the IFFC tests now under way, the F-15's radar and Atlis work together. The radar supplies initial tracking data—the pod's optical sensors being slewed into boresight with the radar—and then supplies range and bearing information to the IFFC system. The Atlis outputs feed video-displayed data to the cockpit as well as newly developed, IFFC-oriented symbols for the pilot's head-up display. Although Hunter expects future IFFC systems will use radar, as well as forward-looking infrared and other sensors, today's radar systems are "noisy" in one or two axes, and the Atlis system gives more accurate bearing data.


Equipped. This is the F-15 fighter aircraft now flying at Edwards Air Force Base in California and equipped with a laser target-tracking pod suspended beneath the port intake.

First bomb away. The IFFC F-15 now is completing initial flight tests—"We dropped our first bomb last month," says Hunter—and to date there has been more trouble with range instrumentation than with the flight- and fire-control electronics. As soon as the last wrinkles are ironed out, IFFC will begin a series of up to 150 flight tests over a period of up to 15 months. The first nine months will be spent with test pilots in the cockpit, operating under controlled conditions to validate GE's optimistic computer projections. Months 10 through 15 will see a series of Tactical Air Command pilots put IFFC through its paces on the bomb and gunnery range at Nellis Air Force Base in Nevada.

Even before the flight test results are in, the IFFC system is obtaining converts. Hunter says that McDonnell Douglas will include concepts derived from it in any new aircraft proposals it makes, and its proposal for the Strike Eagle attack version of the F-15 originally included a maneuvering attack system similar in concept to IFFC, if more limited. General Dynamics also is said to be considering IFFC concepts.

The $34.3 million Advanced Fighter Technology Integration program, AFTI/F-16, includes IFFC in its digital flight control and advanced-maneuvering attack systems. AFTI, under prime contractor General Dynamics Corp., Fort Worth, Texas, equips an F-16 with new electro-optic sensors and advanced aerodynamic systems to enhance the fighter's maneuverability and fighting ability. Experiments with the AFTI/F-16, which will enter flight test early next year, may eventually investigate radar-based IFFC; tests with forward-looking infrared trackers and laser trackers have already been scheduled.

The Air Force Armaments Laboratory at Florida's Eglin Air Force Base is watching IFFC for possible effects on its own stabilized gun program. The stabilized gun would be aimed independently of the aircraft's centerline and thus would be able to engage targets over a wider area and potentially more accurately than fixed weapons.

Retrofit likely. Meanwhile, the mid-1980s are likely to see some form of IFFC retrofit. Few spokesmen wish to be quoted, but many state that both the Navy-Air Force fleets are good candidates for such a retrofit.

If IFFC proves itself and is as potent a force multiplier as predicted, the air staff will have the option of hugely multiplying the effectiveness of the fleet at minimal expense; retrofit of the system might cost only a tenth to a fifth the price of building a new aircraft. □

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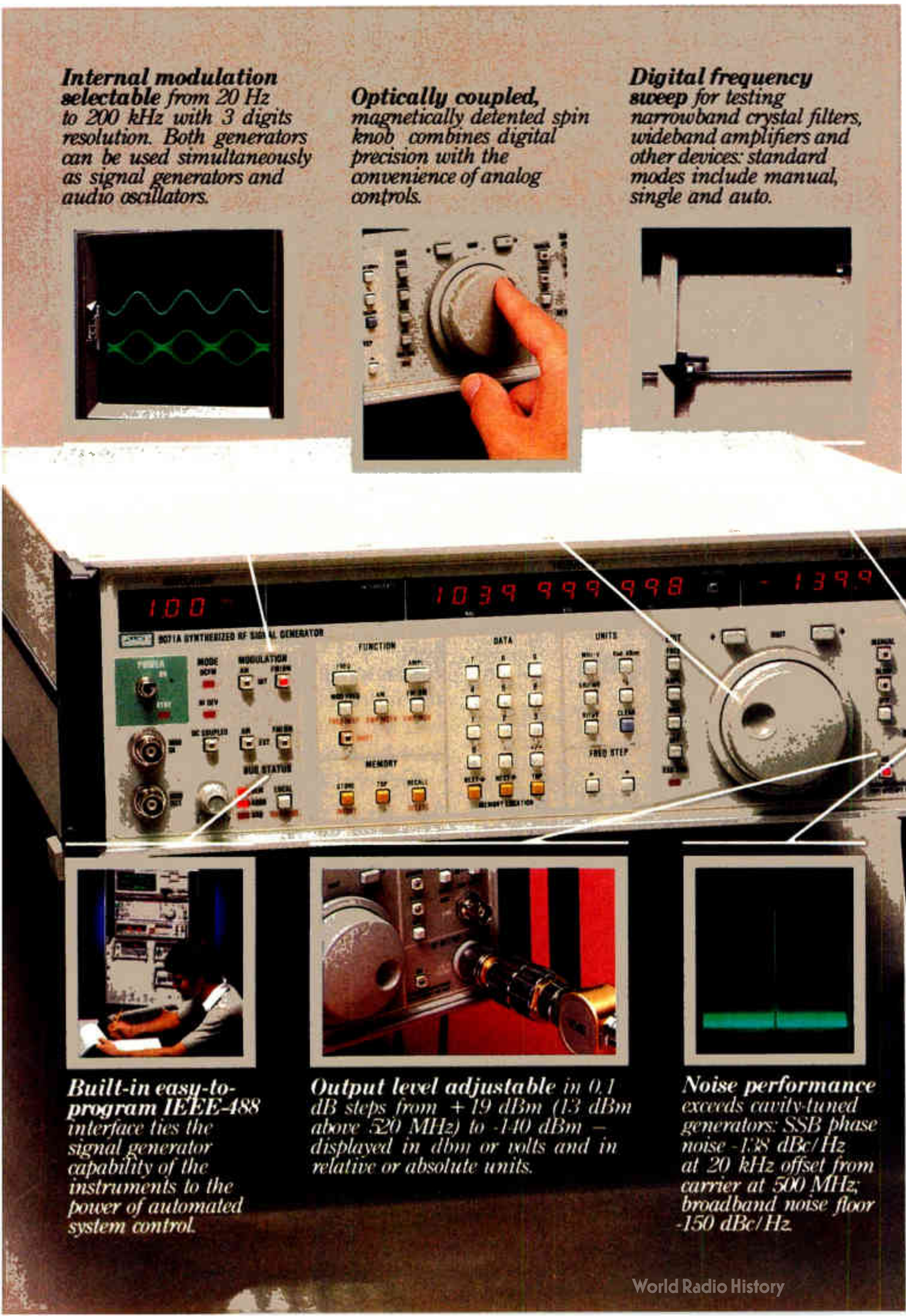

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Industrial electronics

Flight simulator market soars

New FAA training requirement combined with high price of jet fuel forces airlines to buy sophisticated new systems

by J. Robert Lineback, Dallas bureau

A young airline pilot stares intently out the cockpit window, searching for the faint glimmer of runway lights in a thick blanket of fog. He knows it's rough out there; his crew has been tossed about for the past 30 minutes. "There she is," he sighs as the familiar flash appears directly ahead. It has been a harrowing flight, with two near-collisions and an engine fire. But no one has been hurt, no plane was lost.

The craft is actually a 32-bit-computer–based flight simulator winging its way through a digital world. The anxious pilot is attempting to upgrade his status to captain in accordance with the Federal Aviation Administration's new advanced simulation plan, a three-phase program aimed at total training in simulators (see "The three-phase FAA simulation program," below).

The year-old plan is affecting both airlines and the flight-simulator industry. Many commercial carriers are quickly buying new simulators and retrofitting existing equipment with new high-speed computers and state-of-the art digital systems. Initially, total simulation training was inspired by concern for air safety—giving pilots real-world, real-time rehearsals in emergency situations that cannot be staged in real flight. But in an age of sky-high jet fuel prices and plunging airline profits, carriers are eager to replace costly training flights with simulator time.

Braniff International's vice president of flight, Capt. D. R. (Dale) States, estimates that direct operating costs of a Boeing 747 jetliner are $6,500 to $7,000 per hour compared with $250 to $300 in simulators. So far, Braniff is the only airline to qualify for training credits in Phase 2—improved visual response times. American Airlines, which hopes to receive its first Phase 2 certification next month, had as many as 13 jetliners devoted to training in the 1960s. "Now we won't have three [jet] trainers a week; the rest of it is done in the simulator," explains Capt. Walter W. Estridge, director of training at American's flight academy in Fort Worth, Texas.

Attractive market. Meanwhile, the FAA's plan and increasing interest from the U. S. military have caused the simulator business to take off. The list of companies producing simulators and the crucial computer-generated–image (CGI) visual systems continues to grow. Brisk commercial simulator sales are reported by such oldtimers as the Link Flight Simulation division of the Singer Co. in Binghamton, N. Y.; Rediffusion Simulation Ltd. in Crawley, England; and McDonnell Douglas Electronics Co. in St. Charles, Mo. Graham Wilson, president of Rediffusion's CGI firm in Arlington, Texas, estimates that the worldwide simulator market for visual systems alone will hit $160 million and account for $2.1 billion in the next decade.

General Electric Co.'s Simulation and Controls Systems operation in Florida—which entered the military business via the Apollo space program—plans to develop a commercial system to meet the FAA requirements. And outside the U. S., interest is also soaring. In Japan, Hitachi Ltd. recently entered the commercial flight simulator business. In France, Thomson-CSF Simulators continues work on CGI systems for the commercial market.

The FAA's move toward total simulation credits is based on the belief

The three-phase FAA simulation program

The Federal Aviation Administration's advanced simulation program generally breaks down this way:

Phase 1: Simulators must accurately depict an aircraft's performance in takeoff and landing maneuvers (such as decreased drag and ground fusion effects) as well as emulate handling on the ground. This setup allows credits for already jet-qualified pilots. Most major carriers have simulators with Phase 1 certification.

Phase 2: Machines are required to have an improved visual response time from 300 milliseconds to 150 ms and increased fields of vision. This will allow airlines to upgrade copilots to captains on the same craft or laterally transfer crew members from one aircraft type to another entirely in the simulator.

Phase 3 (total simulation training): Simulators must have daylight capabilities plus additional adverse weather features. This phase will allow pilots who are not jet-qualified to move into the copilot's seat. From there, the copilot can move up to captain via the Phase 2 credits, therefore allowing total simulation training. Predictions on when the first Phase 3 credits will be achieved differ among industry experts, with some saying as early as next year and others predicting it will take two to three years. **-J. R. L.**

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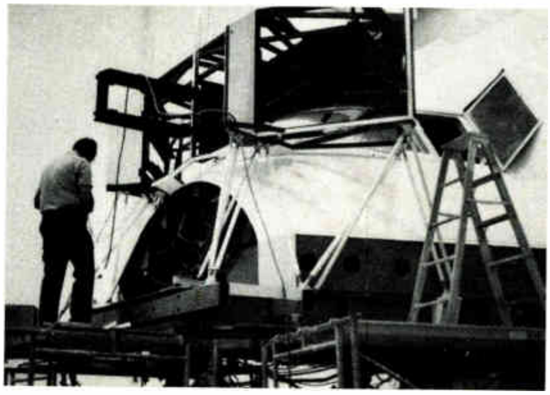
Probing the news

that technology—particularly computer technology—has advanced to the point that total real-world, real-time effects are now possible and within the budgets of airlines. The agency and carriers also believe state-of-the-art simulation training can be better than actual flight.

Technology parade. And to prove it, simulator manufacturers are turning to very large-scale integration, custom circuits, 32-bit host computers, special software, hardwired logic, special-purpose image processors, large data bases, and high-resolution video display tubes. The low cost of solid-state memory has made such systems practical.



Not wild, not blue, not yonder. Technician works on American Airlines' flight simulator. The airline once had 13 jets for training, now has fewer than three flights weekly.

For the most part, commercial simulators "fly" through data bases filled with edges, surfaces (sometimes called shapes), and light points, all of which are configured three-dimensionally to represent real places and airports. Edges—invisible straight lines—are borders that define surfaces, which are colored and shaded to represent buildings, runways, mountains, lakes, other airplanes, and so on. Light points are most commonly used in night and twilight scenes to represent ground lights and other effects. Because of the limitations of straight-edged systems, the U.S. military is funding research into edgeless techniques, which are those that create surfaces via curves.

Model service. Link, McDonnell Douglas, and Rediffusion's subsidiary in Texas all provide data-base-modeling services. Working from maps, layouts of airports and runways, and photographs, the models are created. Some data is entered by digitizer, but most information is fed into the memory by keyboard and X, Y, and Z axes. Many individual objects may be modeled five to six times with various levels of detail. The closer an object appears, the more detail is shown.

The trick is to gradually phase in the different levels in a computing scheme called blended level of detail. Daytime scenes may have thousands of edges and hundreds of surfaces, which are updated 50 times a second. Many CGI models cover an area of 40 by 40 nautical miles.

McDonnell Douglas is offering a third-generation Vital IV system, which is being used to meet the FAA's Phase 2 requirements. The firm anticipates its first Phase 2 approved system soon at Eastern Airlines.

Meanwhile, Link is aiming at Phase 2 and Phase 3—total simulation training—certification with its Advanced Simulation Technology (AST) system. AST, introduced in 1976, is targeted at both military and commercial markets. Link's own full-color CGI visual system, called DIG for digital image generation, is capable of delivering up to 12,000 edges in a single scene and has daylight capabilities. Link anticipates the first AST Phase 2 credits before the end of the year at Flying Tiger Airlines.

Rediffusion, which built all three of Braniff's Phase 2 simulators, is offering two commercial CGI simulator systems: Novoview SP1 and SP2. The SP1 uses a relatively low-brightness beam-penetration CRT for night and dusk scenes. The SP2 uses a high-brightness shadowmask CRT for night, dusk, and daylight scenes. Rediffusion, which jointly produces its CGI visual system under an agreement with Evans and Sutherland in Salt Lake City, Utah, plans to meet Phase 3 requirements with SP3, a recently introduced enhanced version of SP2. □

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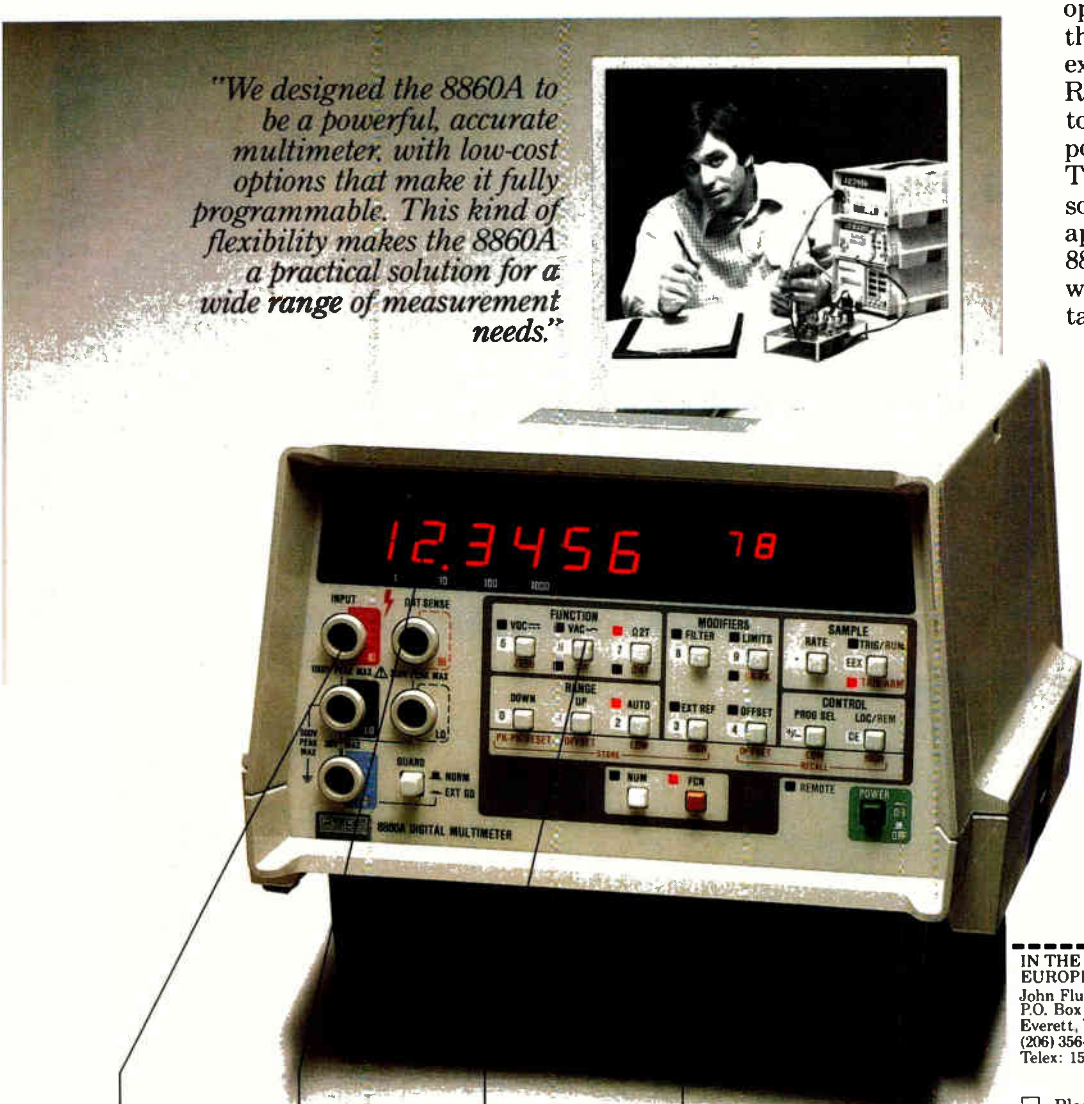

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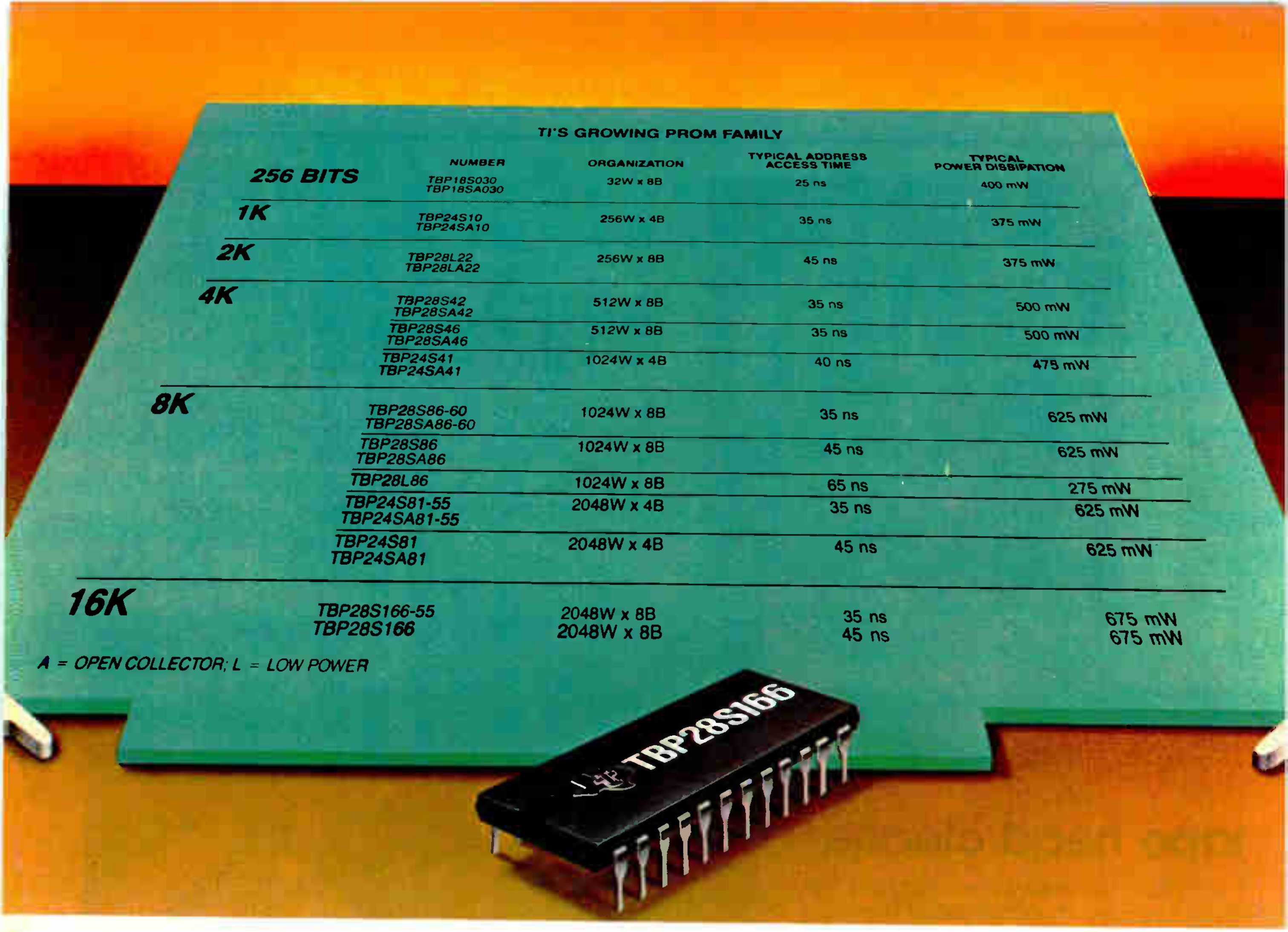

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	NUMBER	ORGANIZATION	TYPICAL ADDRESS ACCESS TIME	TYPICAL POWER DISSIPATION
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1K	TBP24S10 TBP24SA10	256W x 4B	35 ns	375 mW
2K	TBP28L22 TBP28LA22	256W x 8B	45 ns	375 mW
4K	TBP28S42 TBP28SA42	512W x 8B	35 ns	500 mW
	TBP28S46 TBP28SA46	512W x 8B	35 ns	500 mW
	TBP24S41 TBP24SA41	1024W x 4B	40 ns	475 mW
8K	TBP28S86-60 TBP28SA86-60	1024W x 8B	35 ns	625 mW
	TBP28S86 TBP28SA86	1024W x 8B	45 ns	625 mW
	TBP28L86	1024W x 8B	65 ns	275 mW
	TBP24S81-55 TBP24SA81-55	2048W x 4B	35 ns	625 mW
	TBP24S81 TBP24SA81	2048W x 4B	45 ns	625 mW
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C-MOS

INSPIRES THE BEST CHIPS YET FOR COMPUTER, CONSUMER, AND COMMUNICATION APPLICATIONS

Growing process sophistication has brought both speed and design flexibility to a semiconductor technology once famed mainly for its low power dissipation

by John G. Posa, *Senior Editor*

☐ Complementary-MOS technology has always been hailed for its low power consumption. But until very recently, that was about all it was ever praised for. As late as three years ago, C-MOS was also viewed as inherently bulky and ill-suited to high-performance applications. It had its place for low power-drain battery-driven consumer products, but its higher processing costs at one time discouraged speed and density improvements.

When n-channel MOS was being adorned with self-aligned polysilicon gates and then double-polysilicon processing, C-MOS sat quietly at the back of the class. Some of the fault lay with uninspired design practices. As a matter of course, a p-channel load transistor was hung onto almost every n-channel driver device on a C-MOS chip, inflating die size and dashing hopes for very large-scale integrated C-MOS circuits. Indeed, for a time it was mistakenly believed that C-MOS was inherently slower than n-channel MOS.

But no longer are C-MOS's p-channel transistors viewed simply as load devices by MOS IC designers. Now they are looked upon as valuable tools, able to reduce power consumption, raise performance, provide new functions, and simplify layout. Increasingly, the couple of implants or masks the devices add to the process complexity of C-MOS are deemed well worth the trouble.

C-MOS's rise to glory is related to several factors. As n-channel MOS grew in density, its current requirements went up. VLSI n-channel MOS chips now routinely burn hundreds of milliwatts. Though very creative circuit design has been used to lower their power dissipation, this often meant more masks for natural (not implanted) devices, and so forth. Even with the more complex processes, some of the densest n-MOS parts still brush dangerously close to the limit of about 1 watt for cheaper, plastic packaging. But C-MOS automatically powers itself down.

Packaging limitations not only stunt increases in density—the lower densities also rule out otherwise very desirable VLSI designs. Gate arrays are perhaps the best example. The bigger they are, the better, because design automation can then be used to integrate entire systems onto the chips. Whereas n-channel gate arrays are almost nonexistent, C-MOS slices are rapidly approaching a fantastic 10,000 gates apiece. It is safe to say that C-MOS gate arrays will one day be offered by most integrated-circuit manufacturers.

Just as the smaller energy appetite of C-MOS makes it practical for new applications, so do its higher noise margins and its related ability to hold up at extreme temperatures. Both of these other assets were factored into RCA's decision to use C-MOS for its two-chip engine controller (see p. 139). C-MOS's sharp transfer characteristics and wide power-supply tolerance let it work under the hood of a car or down in a hot well. Reliability without fan-cooling was a key factor in Digital Equipment Corp.'s choice of C-MOS for a new small computer (p. 116).

Hand-me-downs

One by one, the niceties that n-MOS enjoys have been applied to C-MOS. As a result, the performance and density of C-MOS circuits now rival those of n-MOS designs. The high speed has been achieved by scaling down device dimensions and using polysilicon gates, though the high density results in part from the judicious use of the p-channel transistors. Area is being conserved by using them sparingly—in memories, for example—rather than by assigning one to each n-channel device.

In fact, this adoption of a high ratio of n-channel field-effect transistors to p-channel FETs has inspired an entire new branch of C-MOS processing, one that Motorola calls merged-MOS. In chips with large, regular cell arrays—like RAMs and VLSI microprocessors—the memory portions are built with n-MOS and the p-channel devices are reserved for the C-MOS control and input/output circuits in the chip's periphery.

Even in pure logic circuits there is no need to mate each n-channel device with its complement. Figure 1 shows some of the C-MOS circuit configurations now in use. The first circuit—a two-input NOR gate—is built with conventional static C-MOS. A NAND gate is similar, except that the load devices would be in parallel and the driver devices in series.

Figure 1b shows two possible enhancements of the basic static C-MOS gate. One is the addition of a standard C-MOS transfer gate on the output, resulting in a pseudo-static logic configuration. This speeds up the circuit by allowing nodes to be precharged high and then pulled low by the faster n-channel devices.

The gate's power dissipation can be lowered by adding the switching devices at the top and bottom of the circuit. With these, large logical networks can be isolated from the rest of the circuit when inactive. Toshiba Corp.'s clocked C-MOS, or C^2-MOS, which has been around since 1970, basically takes the static gate of Fig. 1a and adds to it the p- and n-channel isolation devices shown in Fig. 1b.

Bell Labs' domino C-MOS logic, described in the article on its Bellmac-32 microcomputer (p. 106), resembles clocked C-MOS, except that only n-channel devices are used in the block labeled logic gate in Fig. 1b. Also, the p-channel pull-up and n-channel pull-down devices are driven from a common clock line that keeps all of the logic circuitry shut off during precharging. When inputs are applied to the first gate in a chain of these circuits, logic states quickly ripple through the network, discharging gate after gate like dominos.

One of the most dynamic forms of C-MOS is depicted in Fig. 1c. The precharge and sample clocks do not overlap with one other, but each overlaps with the hold clock. The hold and sample clocks bootstrap the circuit to enable full rail-to-rail logic-signal excursions. In addition, the frequency of these clocks can be dropped significantly for standby.

C-MOS processing allows bipolar transistors and analog circuits to be constructed on the same chip as the digital MOS logic. The resulting circuit design flexibility alone justifies the added process complexity of C-MOS, say many MOS chip designers.

In Harris's C-MOS fusible-link programmable read-only memories, outlined in its article on p. 124, vertical npn transistors are used to supply the current to blow polysilicon fuses. Such a creative application of C-MOS would be impractical with straight n-MOS since the vertical emitter followers would not be available. For the same reason, when a MOS memory compatible with emitter-coupled logic becomes available, it will probably be made out of C-MOS.

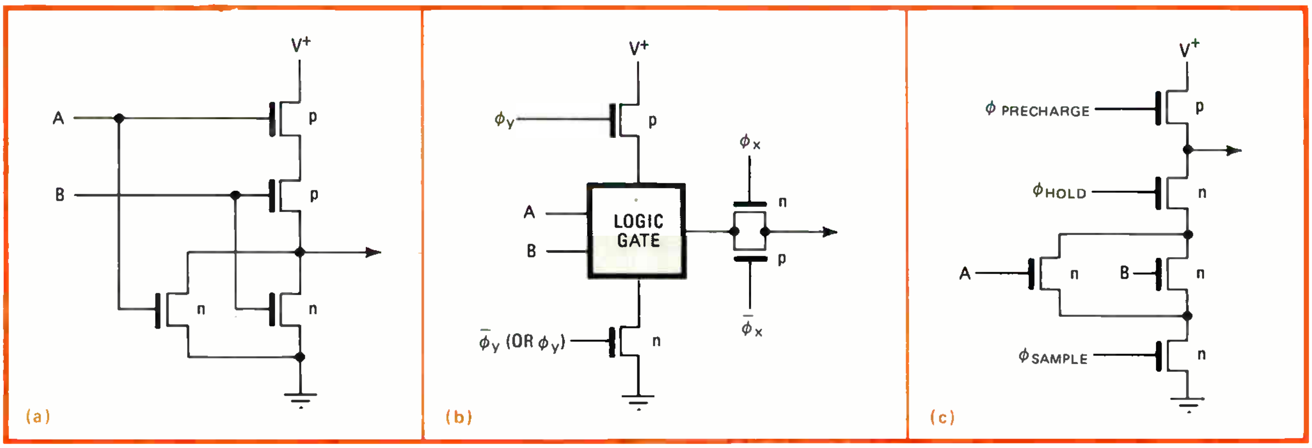
Analog advantages

On the analog side, C-MOS's complementary devices allow efficient current sources and sinks to be referenced from either power-supply rail, and this simplifies the design of differential input stages and push-pull output stages. Indeed, most C-MOS gate arrays can handily support linear circuits on chip [*Electronics*, Aug. 11, 1981, p. 109] as stages for linear amplifiers.

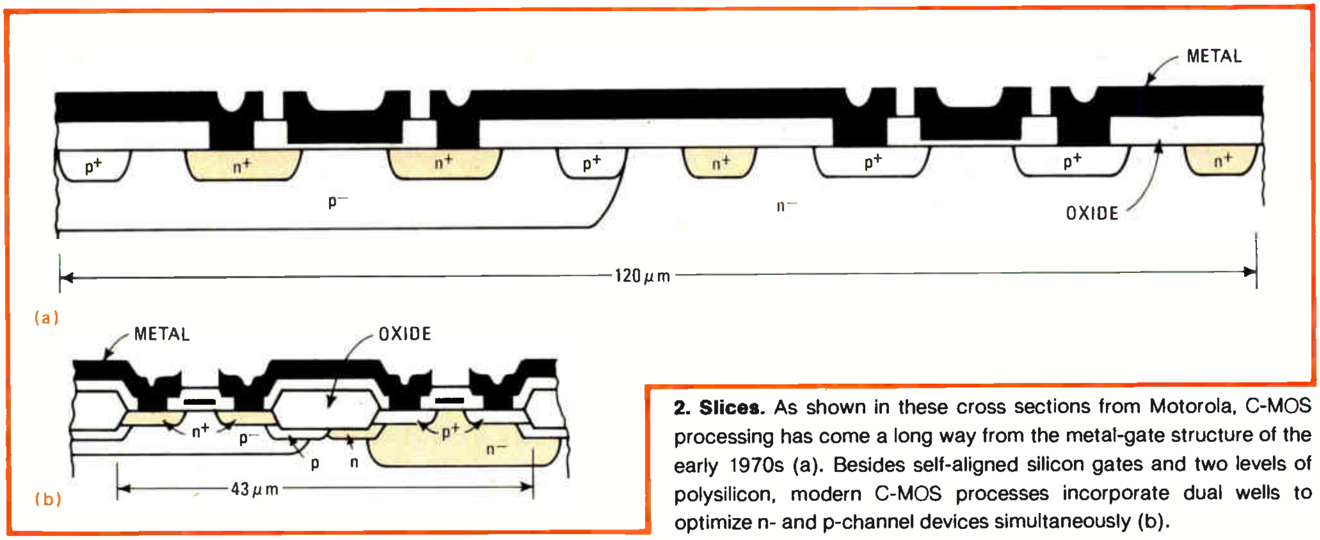
Moreover, when a double-polysilicon process is employed to get C-MOS, high-quality switched capacitors can be built entirely in the oxide above the substrate. This is precisely the approach used to build the single-chip codec from Mostek described in the article starting on page 130. American Microsystems Inc., a long-time proponent of C-MOS, is said to be working on a single-chip C-MOS speech synthesizer; but unlike Hitachi's (p. 127), AMI's will be an analog device.

C-MOS's analog side is also benefiting digital devices like RAMs. In the 16-K static RAM from Integrated Device Technology (p. 120), sense amplifiers are basically C-MOS operational amplifiers. Not only are they simple to build, but they are also extremely high in gain—a feature that promotes efficient latching.

With p-channel devices on hand, bootstrapping—the process of boosting a transistor's gate voltage to overcome its threshold voltage—is no longer necessary. When the gate of a p-channel device is grounded, its source and drain are virtually shorted, so that charge pumping is not required. Paralleled n- and p-MOS FETs



1. Circuits. Circuit improvements have reduced the power and raised the speed of the basic static C-MOS gate (a). The pull-up and pull-down devices and transfer gates on the output can isolate logic blocks to save power (b), and dynamic clocking can sharpen signals (c).



2. Slices. As shown in these cross sections from Motorola, C-MOS processing has come a long way from the metal-gate structure of the early 1970s (a). Besides self-aligned silicon gates and two levels of polysilicon, modern C-MOS processes incorporate dual wells to optimize n- and p-channel devices simultaneously (b).

make efficient transfer gates; National makes extensive use of these in its data converter (p. 136).

Hitachi was among the first to use C-MOS with a higher percentage of n-channel transistors. In its 6147 4-K static RAM, a so-called ubiquitous p well is diffused for all of the storage cells, which are built exclusively with n-MOS FETs. Besides lower active and much lower standby power requirements, the p wells brought side benefits—at least in this application.

The RAM's ubiquitous p well acted as a barrier to carriers generated by alpha particles, and the p wells associated with the n-channel FETs in the periphery could be used to build lateral bipolar npn transistors for pulling up highly capacitive nodes and loads alike.

Why the p well?

Hitachi's Hi-C-MOS process and the metal-gate processes that preceded it evolved from p-channel MOS—hence the p-type wells (Fig. 2). Besides, at the time, p-type boron was the only dopant available to form deep yet lightly doped wells. But with C-MOS circuits high in n-channel FETs, a process with n-doped wells seemed more appropriate. Intel Corp. was one of the first to describe a commercial device based upon n-well C-MOS: a 4-K RAM, announced at this year's International Solid-State Circuits Conference.

Several C-MOS chip vendors have either started with or switched to n wells. The next step is twin wells—one for the p-channel FETs and another for the n-channel devices. In the articles that follow, Integrated Device Corp. and Bell Labs use twin-well technology for their 16-K static RAM and 32-bit microcomputer respectively.

Dual wells become particularly important as geometries are scaled down. It gets increasingly difficult to independently optimize each transistor type with only one polarity of well. With twin wells, both device types can be simultaneously protected from second-order effects, punch-through, breakdown, and so forth.

In the future, C-MOS's p- and n-channel FETs will continue to be isolated with steep-walled recessed oxides. Mitel Corp. was one of the first companies to selectively oxidize a C-MOS wafer. The thick field oxide plus two polysilicon layers resulted in chips like the 64-K cross-point switch described in the article on page 133.

Twin wells also help to remove latchup—one of C-MOS's few remaining stigmas. With dual wells, the substrate is best doped very lightly and this lowers the gain of parasitic npnp and pnpn thyristor-like structures associated with C-MOS processes. Two wells, plus guard bands around a chip's I/O transistors, manage to control latchup to the point where real abuse is needed to make it happen.

To eliminate latchup altogether, it seems that C-MOS must be built on an insulating substrate. In the U. S., C-MOS-on-sapphire circuits are very popular for military contracts. Rockwell, Hughes, and RCA Corp. all supply C-MOS-on-sapphire chips to the Government, and one or more will continue doing so through the Department of Defense's Very Large-Scale Integrated Circuits program [*Electronics*, Sept. 22, 1981, p. 89].

In Japan, Toshiba Corp. is pushing C-MOS-on-sapphire for commercial applications. So far on sapphire it has built a 4-K static RAM and a 16-bit microprocessor described in this series of articles. As Toshiba points out on p. 112, if an insulating substrate like sapphire makes sense for any process, it makes sense for C-MOS. The source of a p-channel load transistor will still be connected to the drain of an n-channel driver, but the source and drain regions can butt up against one another and make a direct connection because on an insulator no wells are in the way.

There are even more creative plans afoot to further compact C-MOS geometries. They attempt to stack the n- and p-channel devices on top of each other. One such structure places the two channels perpendicular to each other in a single-device well [*Electronics*, May 5, 1981, p. 39]. Another vertical C-MOS inverter can be made with two levels of polysilicon if the upper level is annealed and doped to function as a second channel located above the first-level polysilicon gate. Two techniques for doing this will be detailed at the upcoming International Electron Devices Meeting. □

TWIN TUBS, DOMINO LOGIC, CAD SPEED UP 32-BIT PROCESSOR

by B. T. Murphy, L. C. Thomas, and A. U. Mac Rae, *Bell Laboratories, Murray Hill, N. J.*

☐ The nonstop increase in computer power that has marked the last three decades seems unlikely to slow in the foreseeable future. The emergence of very large-scale integrated circuits with submicrometer dimensions alone implies single-chip computers executing some 100 million instructions per second (MIPs) and thus performing on the same level as many mainframes (Fig. 1).

As the technology that yields the most MIPs per watt, complementary-MOS will feature prominently in the VLSI advance. Bell Laboratories had already recognized this power factor in the mid-1970s and from the start based its microprocessor design program on C-MOS. Its search for the best semiconductor process and circuit combination led first to the Bellmac-8 microprocessor and then the Bellmac-4 microcomputer and has found its most recent expression the Bellmac-32, a 32-bit microprocessor that exploits twin-tub C-MOS technology, domino C-MOS circuitry, and automated design.

Rising to 32 bits

The Bellmac-8 microprocessor, which became available in 1976, was primarily a software-driven design. As microcomputer systems had become more complex, high-level language programming called for an efficient compiler, and this in turn called for a microprocessor with a wider range of memory modes than was then obtainable. Both 8- and 16-bit capabilities were required. Because of these features, the control structure had to be unusually complex.

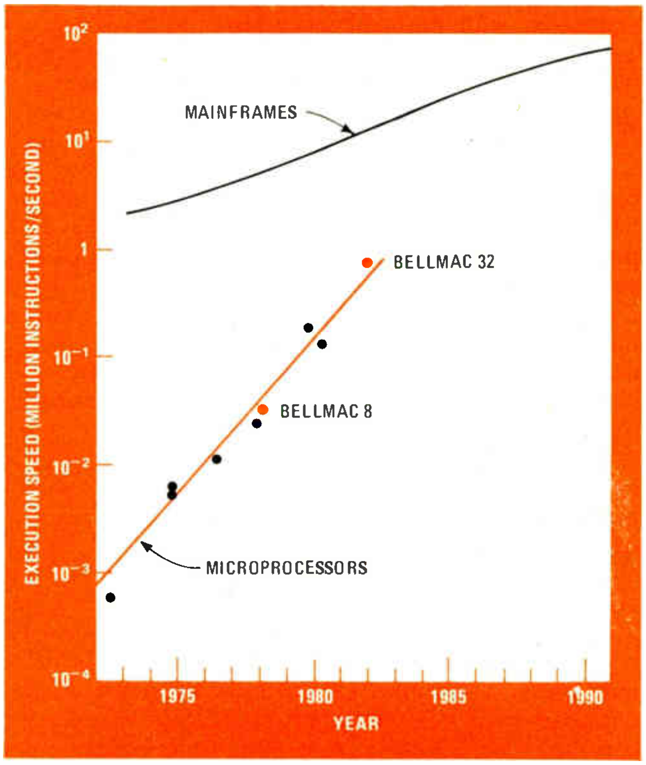
The result—the Bellmac 8—included an 8-bit arithmetic and logic unit, a 16-bit address-arithmetic unit (AAU), and a pointer register. All working registers were in main memory, and pointers could directly address 16 registers with overlapping stacks anywhere in main memory. This pointer structure made subroutine calls and returns, for example, efficient enough to exploit structured programming techniques properly.

The 8-bit ALU was implemented in hand-designed pseudo-n-channel MOS circuitry. Since the ALU was active only about one cycle out of every six, the use of a ground switch reduced power dissipation markedly. The high average fan-in made the pseudo-n-MOS more effective than static C-MOS in both speed and packing density.

In the 16-bit AAU, on the other hand, the simple address arithmetic being performed led to a low average fan-in and the unit was in continuous use, so that conventional C-MOS was chosen for this design. Pointer registers also used conventional C-MOS. Computer-aided design support for the data path was restricted to simulation of the hand-drawn logic, and the ALU was simulated with Bell Labs' MOS timing simulator software (Motis).

The control selection was complex for its day, for the rich instruction set included several addressing modes and both 8- and 16-bit data types. Though microcoding, the simplest method of implementing complex control functions, was considered, the read-only memory needed was just too large and slow. A programmable-logic array implementation was more efficient, but even in this case the straightforward single-PLA approach would have led to a large, slow chip.

The approach finally chosen was a pipelined design using two PLAs—a main control PLA supplemented by another one dedicated to ALU control, with each PLA having multiplexed outputs to minimize its size and to achieve Bell Labs' speed objectives. Within the PLAs, a row of gates between levels eliminated near-redundancies. As a result, the PLAs could be efficiently packed with code that was generated automatically by system-level simulation programs.



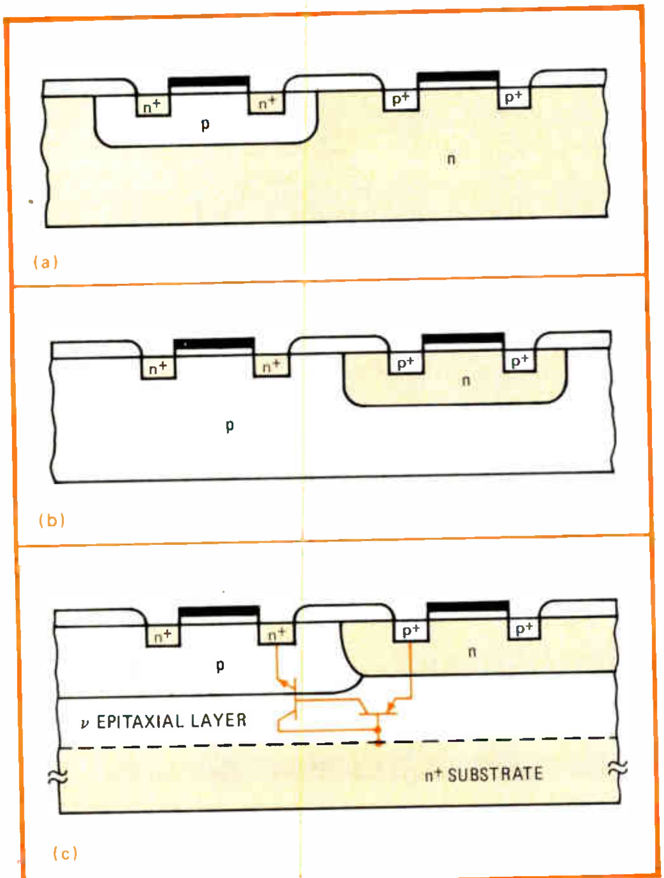
1. Approaching mainframes. As can be seen from the graph, the Bellmac-32 single-chip microcomputer is approaching the performance of a mainframe. In fact, if the two growth curves are extrapolated, they will meet some time later this century.

The overall chip layout used metal for bit lines and polysilicon for the control lines orthogonal to them. The control lines got their signals from the demultiplexing logic controlled by the main and ALU PLAs.

This design, first executed in 7.5-micrometer design rules in p-tub, latchup-free C-MOS technology, was later manually updated to 5-μm rules for higher performance and lower cost. Typical gate speeds for these rules were 7 to 30 nanoseconds, depending on gate function and load. Power dissipation at full clock rate is 0.5 W.

The Bellmac-4 microcomputer, which came out in 1980, had about the same complexity and used the same design techniques as Bellmac-8 microprocessor. However, it featured 4-, 8-, 12-, and 16-bit instructions operating under the control of a software-settable register, with four address modes for each of its two source and one destination operands. On-chip random-access memory and ROM were designed by hand, but the I/O control logic was built up from a mixture of PLAs that were automatically wired polycells. This was the first, or one of the first, uses of CAD tools in the design of any microprocessor or microcomputer.

The same circuit design techniques were employed for the Bellmac-4 microcomputer, except that they were implemented in the twin-tub C-MOS technology, which has higher switching speeds. Typical ALU gate delays using 3.5-μm design rules ranged from 3 to 12 ns. Employing a new format that can be technologically updated, the chip has now been shrunk to 2.5-μm design rules that lower gate delays to 2 to 5 ns. At the typical 10-MHz operating frequency, the time to add two 16-bit numbers is 8 microseconds and the power dissipation is 100 milliwatts.



2. Twin-tub C-MOS. The traditional complementary-MOS process uses a p well in an n-type substrate (a). However, the same principle can be used to form an n-channel device in a p-type substrate (b). The best of both worlds can be had by using two tubs (c).

A 32-bit microprocessor

The Bellmac-32 is a full 32-bit, single-chip microprocessor. Control logic, a 32-bit bus, and 63 I/O channels all fit on the same chip. Its instruction set and address modes are similar to those of today's minicomputers in the 1-MIP range. It was designed to support the structured C language under the Unix operating system, with virtual memory capability implemented in hardware.

All this called for a processor 10 times more complex than its two predecessors. In fact, when it became clear how large the chip would have to be, it at first seemed that the control logic and bus interface might better be put on two chips. But then, on the grounds that a 32-bit machine would most probably be used in systems with so much memory that it would dominate system cost, the decision was made to give chip performance precedence over chip cost.

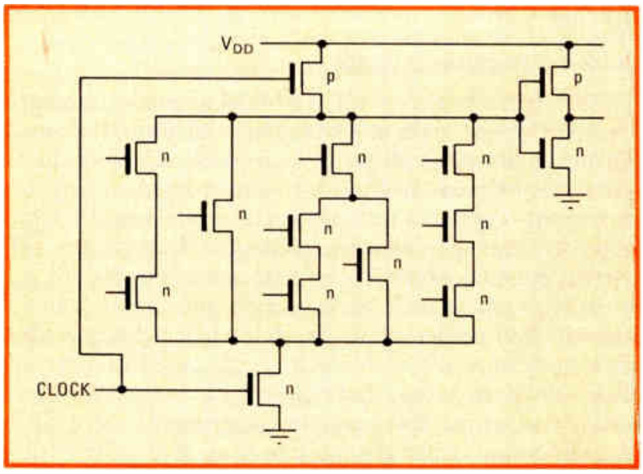
However, the use of two chips would have hurt performance because of the long delay inherent in communication between them. Also, little savings in cost could be reaped unless the bus between them were narrow enough to prevent chip I/O from adding deleteriously to the size of the two chips. Furthermore, a product of this complexity and power would probably have a long lifetime during which its size could be reduced repeatedly as smaller design rules became feasible. So the final choice was a single-chip design in a format whose technology could readily be updated.

New ideas

Nevertheless, innovation was needed on many fronts before it was to be possible to manufacture this chip. In the 1978 planning phase that preceded actual design, several new approaches were selected. The development of the twin-tub C-MOS technology and domino C-MOS circuits was started, to meet the performance needs for this machine. Updatable polycells were developed to support the need for a rapidly correctable automated design of the random logic in the control section, while an updatable gate-matrix layout technique was designed to give a densely packed, high-performance internal bus structure. The modularization of the design used in the Bellmac-8 microprocessor was carried to a much higher level in a hierarchical, modular, top-down approach to the control section. Finally, chip-level logic and timing simulation were supported by automatic generation of component parameters from the mask data base.

Traditionally, C-MOS circuits have had slower switching speeds than n-MOS circuits, but in spite of this difference, they can still perform better chip for chip if the total number of gates in a chip is limited by power dissipation. In addition, C-MOS's longer gate delay is not a fundamental defect but a matter of technology choice and circuit configuration. With appropriate technology and circuitry, the power dissipation advantage of C-MOS can be combined with competitive and in some cases superior gate-level performance—even though the n-MOS transistors within C-MOS chips have traditionally had slower switching speeds than those in purely n-MOS chips.

C-MOS circuits have a higher input capacitance but better drive capability than n-MOS when low fan-ins are involved. For high fan-in situations, other C-MOS circuit alternatives are available, however.

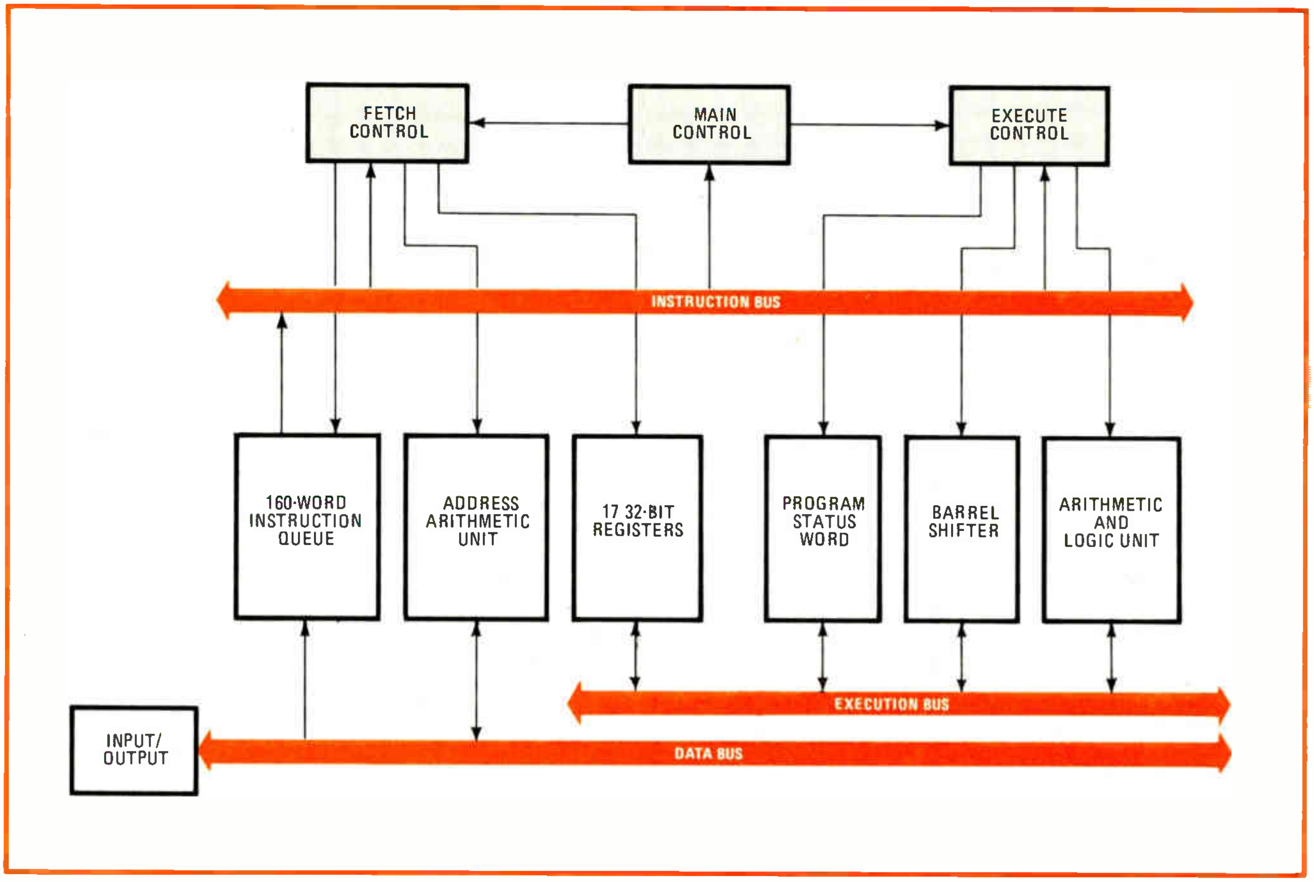


3. Like dominos. This form of dynamic C-MOS doubled the speed of the processor's arithmetic and logic unit. A low clock pulse biases all of the gate outputs and inputs to a logical 0. When the clock rises, logic signals cascade from the first gate to the last.

Some options

Figure 2a shows a conventional silicon-gate C-MOS cross section. The p-channel transistor is formed in the n-type wafer doped to give the right threshold voltage—about 1 volt. A p-tub is formed in the n wafer to accept the n-channel transistor. The p-tub doping therefore has to be much higher than the n-wafer doping in order to overcompensate it with some degree of control. This leads to higher drain and source capacitances and also a high back-gate bias effect. The last causes poor performance whenever the source voltage goes above ground potential—for example, in transmission gates or transistors in the serial string of transistors in NAND gates—causing the channel to pinch down and in the extreme case to pinch off completely.

This poor performance can be improved for the n-channel transistors by using an n-tub C-MOS technology (Fig. 2b) that is just the converse of the p-tub process. The n-channel transistor then has the performance of



4. Parallel control. The Bellmac-32 has separate fetch and execution functions. The fetch control section has a separate address-arithmetic unit for address calculations and a 160-word-deep instructional queue. The execution unit features a barrel shifter.

that obtained in normal n-MOS technology, an important advantage. Unfortunately, the converse problem to p-tub C-MOS exists—the p-channel transistor has capacitance and back-gate bias problems.

The complete answer to the performance problem is shown in Fig. 2c—twin-tub C-MOS, in which, ironically, both types of transistor are formed in tubs; but in this case the background doping is very low, so that each tub can be implanted with the optimum dose for its corresponding transistor.

Finer design rules are easily accommodated in this twin-tub technology since such problems as punch-through are minimized by the ability to dope each tub separately. The structure also has the advantage of symmetry. The tubs are self-registered with respect to one another—wherever there is no n tub, there is a p tub, so that only one mask is needed for both tubs. (Twin-tub C-MOS, incidentally, is also being used for linear circuits, such as codecs, by the addition of another level of polysilicon to form capacitors.)

No latchup either

Traditional C-MOS technology also causes latchup because the parasitic pnp and npn transistors combined to form a latching pnpn device, usually when there are current surges in an input or an output. The surge current flows into the base of either the npn or pnp device, and once turned on, the pnpn transistor remains latched until the power supply is turned off. This effect can be eliminated by using an n^+ substrate as shown in Fig. 2c. The n^+ substrate forms a base contact to all of the parasitic pnp transistors. By connecting this substrate to the positive power supply voltage, it is possible to provide a low-resistance path across the base-emitter junction of the parasitic pnp transistors.

The corresponding solution for n-tub technology, however, does not work as well, since it calls for a p^{++} substrate that would have lower conductivity and cause more out-diffusion problems than an n^+ substrate. In the I/O circuits, additional protection is provided by surrounding the p-channel transistors with n^+ guard rings and the n-channel transistors with p^+ guard rings. The former gives additional contact to the pnp bases, the latter a contact to the npn bases. I/O circuits take up only a small proportion of the total area in a VLSI chip—4% in the case of Bellmac-4 microcomputer—and the guard rings are a small fraction of this area.

Another factor that has limited the application of C-MOS in the past was the relative complexity of the process. But if C-MOS wafer-processing costs have increased in the search for higher performance, n-MOS costs have risen even faster for the same reason. The days of the simple four-mask process have long gone, and depletion-mode n-MOS, with one chip containing three and even four different kinds of transistors implanted to give different threshold voltages, are now not uncommon. C-MOS is no longer the most expensive MOS process around.

With a correct choice of technology, then, the performance of conventional C-MOS logic circuits can be made competitive with those of n-MOS logic circuits. And with a correct choice of circuits, the situation can be improved even further.

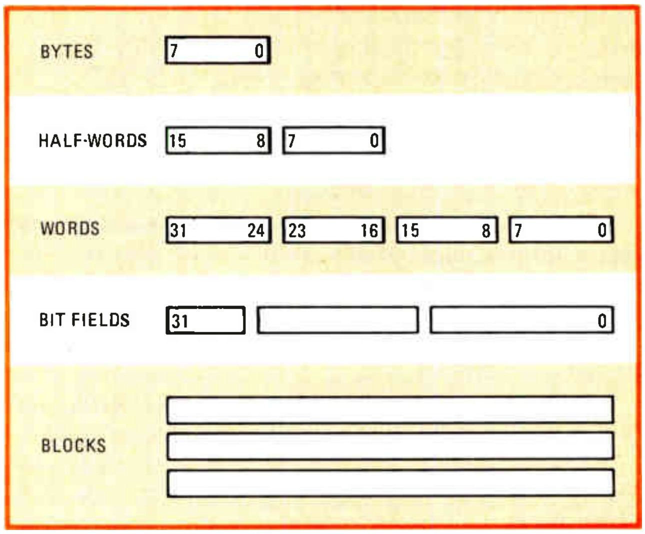
The existence of opposite-polarity transistors within a C-MOS chip can be exploited in many ways other than for low-power dissipation. The p-channel device makes an excellent passive-load device, and since its source is grounded in that configuration, it does not suffer from back-gate bias effects. The pseudo-n-MOS circuit performs a similar function to that of a depletion-mode n-MOS circuit and has a similar performance, given a similar n-channel device.

Room for creativity

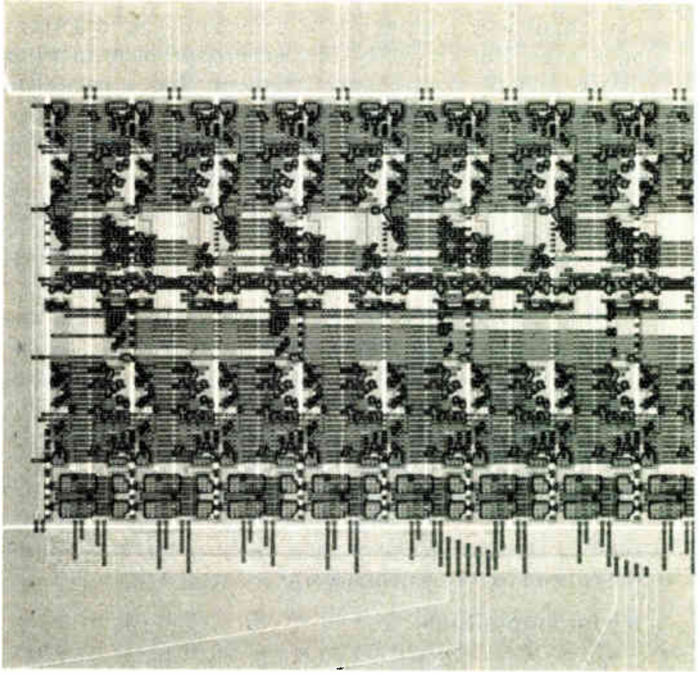
Dynamic circuits can be used for saving die area in C-MOS circuits just as they are in n-MOS, but here again the p-channel device gives additional circuit design flexibility. In PLAs the p-channel device is in this case being used as an active device with its gate under clock control. The p-channel device pulls up or precharges a word line and logical operations are performed on it. The n-channel transistors are controlled by a ground switch that is also under clock control.

Another form of dynamic C-MOS—domino C-MOS—is illustrated in Fig. 3. Here the p-channel pull-up devices and n-channel ground switch or pull-down devices are driven by a common clock line. Precharging occurs on the high-to-low clock-pulse transition. Discharging, under the control of the n-channel input transistors, happens as the clock signal rises.

The output inverter buffers the output signal and also ensures logic transmission without noise spikes or glitches. During precharging all circuit outputs—and hence, circuit inputs—are supposed to be low. When discharging begins, the first logic stage is activated, then the second, and so on (hence the name domino). If one of a circuit's inputs happens to remain high from a previous



5. Data structures. The Bellmac-32 microprocessor is a byte-oriented machine capable of operating on 8-bit bytes, 16-bit half-words, and 32-bit words. The device is also able to work effectively with variably sized bit fields and with large blocks of data.



6. Compacted. This is just the ALU portion of the machine. It contains 20,000 transistors and took nine months to complete. Recently scaled down using 2.5-micrometer design rules, the ALU now operates at 8 MHz. Overall die size will be about 150,000 mil².

phase, it might generate a high-level output. However, the inverter makes certain that the inputs to the next stage remain low during discharging regardless of input conditions.

Use of domino C-MOS gave twice the speed of conventional C-MOS in the ALU module. Moreover, only a single clock line is required, whereas an equivalent n-channel MOS circuit would demand two. Additional transistors can also be added to make the circuit quasi-static and immune to charge-sharing effects.

A 32-bit architecture

The focus of this work on C-MOS technology was, of course, the Bellmac-32. It is the first chip ever to use domino C-MOS logic—in its ALU, its barrel shifter, and its AAU.

As the block diagram in Fig. 4 shows, the chip also includes two temporary registers, a barrel-shifter, seventeen 32-bit general-purpose registers, an instruction queue 160 words deep, and a program counter. All of these units are 32 bits wide. The 32-bit multiplexed data-address bus is split into two parts that communicate through the two-ported register set. This splitting provides faster operation of each part and allows parallel data transfers for increased throughput. I/O transfers are also 32 bits wide for wide-path communication with all peripherals.

The 32-bit machine is byte-oriented in its data structure (Fig. 5) and in its instruction and address coding. It supports three address instructions—separate addresses for each of the two source and the destination operands. Multiply, divide, modulo, subroutine call and return, and system call and return can each be executed with a single instruction. Also, there are four levels of execution: kernel, executive, supervisor, and user, with different access privileges in each mode. Privileged instructions are provided for operating system use, as is reliable exception-handling mechanism.

Design automation helps

Layout of the 100,000-transistor-site chip was finished within three months of receipt of final logic, and chip debugging took a further five months. Only three minor logic errors were found, with the remaining errors being problems introduced by the hand-stitched power and ground connections.

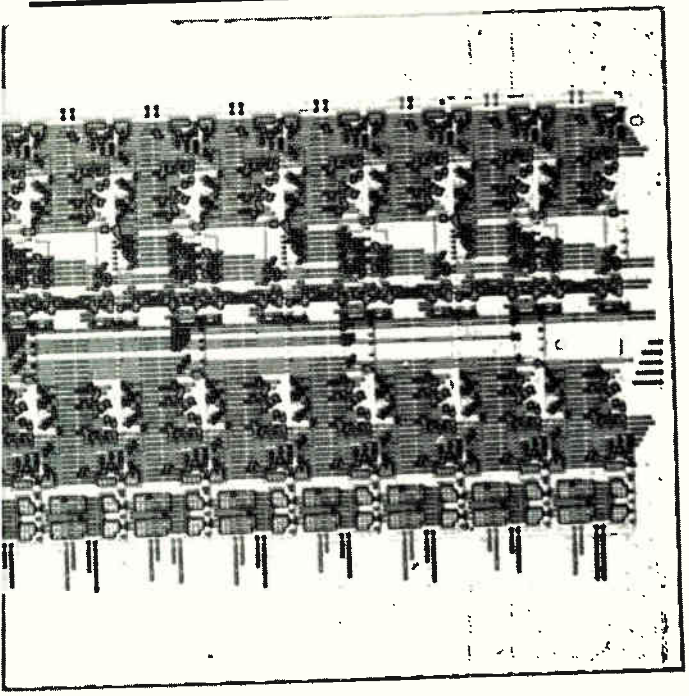
The design of the 20,000-transistor ALU took nine months from the receipt of the functional description to fully debugged and functional chips (Fig. 6). The period included the time needed to debug the new design and circuit tools.

The 32-bit ALU uses carry-look-ahead at the 4-, 16-, and 32-bit levels. Simulations predicted an add time of 124 ns with worst-case two-sigma limits on processing parameters for 3.5-μm design rules. Actual measurements of delay on the same slice yielded 105 ns, as compared to a 98-ns prediction by the simulator—an indication of the latter's accuracy. Simulations of all portions of the data-address path showed that all would pass a 4-megahertz test with worst-case processing. Actual measurements of a number of chips showed that the typical frequency was in fact 6 MHz—none was as low as 4 MHz. The ALU portion of the machine has now been updated to 2.5-μm rules with a typical operating frequency of 8 MHz.

The control section of the Bellmac-32 is hierarchically organized. A main PLA distributes control to other slave PLAs, with demultiplexing logic passing the control signals to the bus interface and I/O sections of the machine. The first stage of the the hierarchical structure is instruction decoding. The second stage is carried out in a random-logic design using CAD-supported polycell layout with automatic signal wiring for all but the power and ground connections.

The chip area was 1.45 square centimeters in 3.5-μm design rules. Yield, though of course low for a chip of this size, fit the expected value based on an extrapolation from smaller chips. Also, although the yield could easily have been too low for it to be possible to distinguish between design and processing defects, this turned out not to be the case. Debugging proceeded quite well on chips with a single or even two processing defects. Enough defect-free chips were obtained for their code to be run in a single-board computer in order further to study the design and use of this machine.

The present chip has provided much valuable feedback on its design and technology, of which extensive use is being made to shrink it down to 2.5-μm design rules. The new version will have a clock distribution system that has been substantially improved for higher throughput. Also, more of the control logic is implemented in PLA



structures, and the remaining random logic is being implemented in the PLA style, rather than as polycells, for greater density and performance. The overall layout will occupy 1 cm^2.

The performance of the chip in a system is difficult to measure, as it varies with the memory speed and the instructions required for each application. Moreover, the MIP term is vaguely defined and hard to interpret, since a chip with a high MIP value may do well in one application program for which its instruction set is suitable but poorly in another for which it is not. Clock frequency alone is useless as a performance measure, since throughput depends on what the machine is designed to accomplish within a clock cycle.

Figure of merit

In view of all this, the performance objectives for the Bellmac-32 microprocessor were established by the software users in terms of throughput on seven user-defined benchmark programs. The throughput of the Bellmac-32 microprocessor was then defined as a percentage of an existing Western Electric minicomputer, whose performance on these same programs is comparable with a 1-MIP minicomputer when coupled with a memory system with average access time of 400 ns.

A major design consideration for a VLSI microprocessor is that its product life cycle is likely to be much longer than the interval between design rule changes, primarily because of the large investment in software and hardware needed to realize a design. Improvements in its operating speed and cost can be obtained by implementing the existing design with the new design rules, but it must be possible to do this quickly and for reasonable cost. This is now accomplished in the Bellmac series by means of designing all of the parts in a design-rule–independent way.

Appropriate CAD software calls out the actual design rules from a design-rule file and from them generates the mask and simulation data bases. Designs can then be implemented in silicon with state-of-the-art design rules and, as smaller rules become feasible, can be followed by rapid technology updates with a minimum of the agonizing effort that traditionally accompanies new layouts.

The above factors were basic considerations in the selection of a design methodology for the members of the Bell Labs microprocessor and microcomputer family. A typical microprocessor has three major parts—the data-address bus structure, the control logic, and the I/O logic—for each of which different methodologies are appropriate.

Fitting designs

The bus structure consists of several subsections that can be designed separately, each having a regular structure imposed by the bit-organized nature of the circuits. Thus its complexity is low, and it can be designed in a reasonable time. The control logic is much less regular, and a well-disciplined, machine-aided design approach is definitely needed. I/O, however, is highly modular and is the latest major section to undergo the transition from hand to machine design, mostly out of a desire to ensure that the technology can be updated.

The design methodology employed by Bell Labs has taken these factors into consideration and has evolved from family member to family member as the complexity and therefore the pressure to find faster and surer design techniques has increased. The design approach for the bus structure has consequently evolved from a hand-packed design to the use of gate matrix, which is a regular but hand-packed design done at a symbolic level, with machine generation and verification of the resultant layout and circuit.

Within the control section, the major control functions have been implemented as PLAs with multiplexed outputs to keep the PLA sizes within bounds set by performance constraints. The demultiplexing logic has been implemented with increasing levels of CAD support as its complexity has increased. In addition, increasing emphasis has been placed on modular design, so that individual modules could be handled as separate, less complex, designs. Inevitably, however, there is more interaction between modules in the control section and less regularity in intermodule communication than is the case in the bus structure.

The resulting problems are best handled with a top-down, hierarchical design. A module function, its approximate size and shape, and its I/O are defined, and wiring between modules is done automatically before the interior of the module is finalized. In this way, it is possible to keep track of long intermodule communication paths from the early phases of the design, preventing surprises in machine timing and wiring area. This methodology consciously emulates that of structured programming, which has been increasingly used in the last decade to ease the problems of development of complex software. □

SAPPHIRE SUBSTRATE BOOSTS MICROPROCESSOR DENSITY

by Tsuneo Kinoshita, Tai Satô, Hiroyuki Tango, and Jun Iwamura, *Toshiba Corp., Kawasaki, Japan*

□ When low power and high density must combine in a complementary-MOS integrated circuit, forsaking bulk-silicon C-MOS for the more expensive variant on a sapphire substrate makes sense. So it was that Toshiba turned to C-MOS on sapphire for its T-88000 16-bit microprocessor, an IC designed to meet a wide range of complex processing jobs. The part also incorporates n-channel MOS devices.

Because it is intended for disparate applications, the T-88000 (*Electronics*, Feb. 24, 1981, p. 140) has an alternate instruction set, realized by placing the control memory off chip, as Fig. 1 makes clear. For speed, it utilizes several special-purpose hardware units, plus a multiplexed 32-bit bus interface. The IC includes microinstruction support of high-speed input/output operations, thereby supplanting special-purpose support chips.

C-MOS is a good candidate for very large-scale integrated logic, but ordinary bulk-silicon devices need island isolation, which requires extra chip area and reduces speed. Silicon-on-sapphire substrates, however, overcome these problems.

About 10 years' work with SOS technology culminated in 1978 in a 7,000-gate processor designed for a pattern-recognition system. That processor combined C-MOS and n-channel enhancement- and depletion-mode devices. C-MOS devices were used where driving large capacitances and high noise immunity are necessary, and n-MOS devices were used for complex logic because of their higher packing density.

Saving space

One interesting point to note, however, is that some simple C-MOS SOS devices like the inverter that is shown in Fig. 2 occupy less space than do their n-channel counterparts. Silicon-gate C-MOS SOS does not require the extra area for the connection between the output line and the source-drain region shared between the drive and load devices.

Compared to bulk C-MOS, SOS can cut chip area about 30%, because a direct connection, rather than a metal or polysilicon bridge, can be made between the p^+ and n^+ regions of the p-channel load and n-channel driver transistor, respectively. Moreover, SOS devices have about half the stray capacitance bulk devices must live with. To achieve that speed with bulk processing, minimum design rules would have to be scaled down to 2.8

A C-MOS-on-sapphire memory

Toshiba is also developing a high-speed, low-power complementary-MOS-on-sapphire 4-K-by-1-bit static random-access memory. This RAM has a typical access time of 18 nanoseconds with a power dissipation of 200 milliwatts (at 5 megahertz) with a standby power of 50 microwatts while using only a single 5-volt power supply.

The RAM uses molybdenum silicide gates with a gate length of 2 micrometers with an effective channel length of 1.5 μm and a gate oxide thickness of 500 angstroms. Rather conservative 3.5-μm design rules were adopted, except for the gate length.

Starting epitaxial-silicon thickness is 0.7 μm, and double ion implantation of deep boron and shallow phosphorus is used to suppress the back-channel leakage current and to adjust the threshold voltage of the channel region of n-channel devices. Likewise, deep phosphorus and shallow boron are implanted into p-channel devices.

The sheet resistivity of the 3,000-Å molydenum-silicide gate layer is about 3.5 ohms/square. This low sheet resistivity reduces a wiring RC delay along the word-select lines to a tenth of the polysilicon gates' delay.

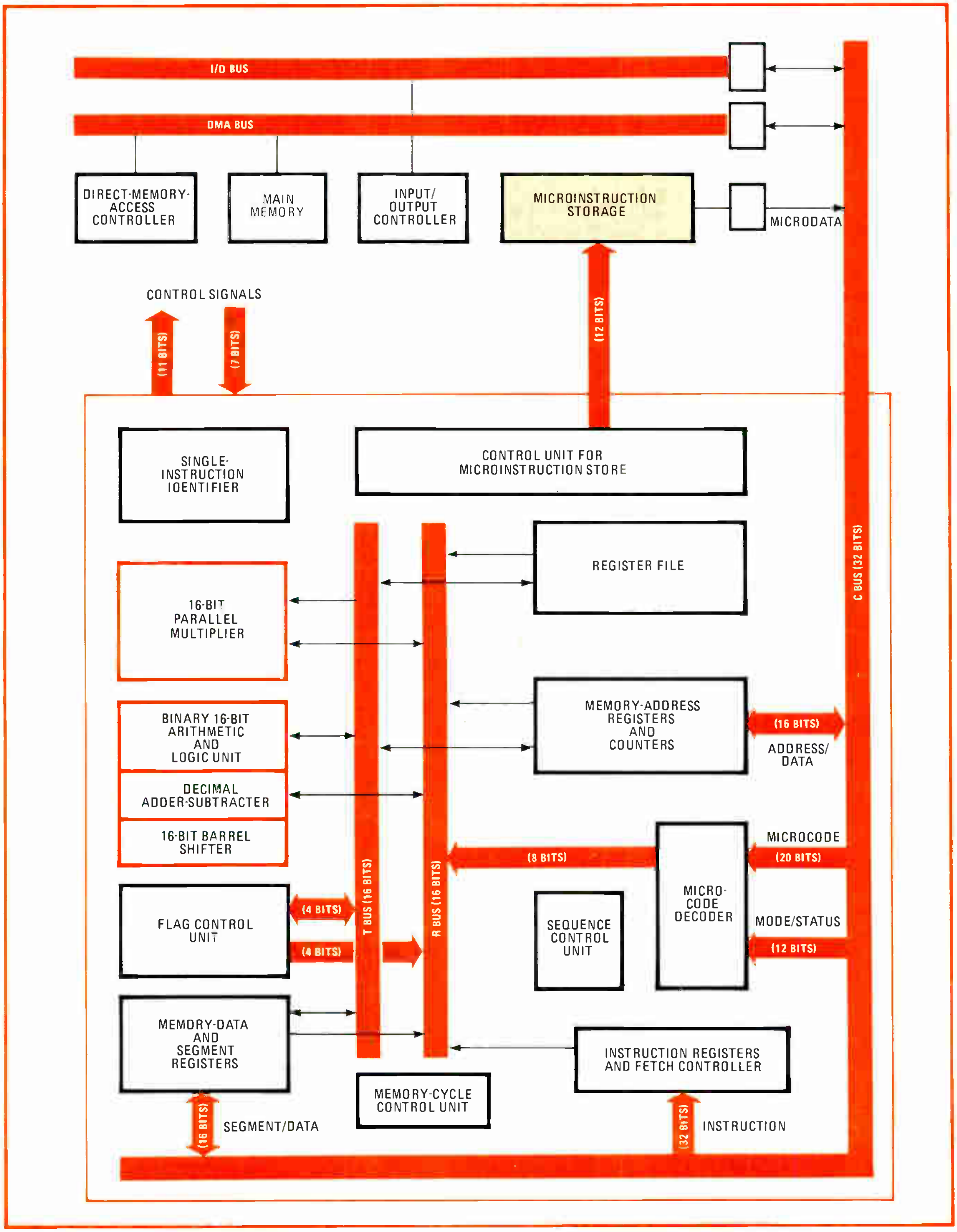
The RAM uses the standard six-transistor C-MOS flip-flop memory cell. Each bistable node of the memory cell is connected to one of a pair of bit lines through a transfer-gate transistor. The memory boasts a two-stage sense amplifier to do high-speed read operations.

The first stage, the balance-differential sense amplifier, consists of column amplifier circuits and load circuits and four p-channel load transistors arranged commonly for each column. This first stage amplifies a small voltage difference between the bit lines to get a medium level.

Then the second stage amplifies the signal to get a larger voltage swing. Each substrate of the n- and p-channel transistors in the sense amplifiers is tied together with its own source to prevent the unstable hysterisis operation due to the floating substrate effects of the silicon-on-sapphire transistor.

The cell size is 36 by 36 μm, and the chip size is 3.11 by 4.07 millimeters. The low standby power lets the part be used in a battery-backup application. The RAM is free of latch-up and has high soft-error endurance because of the C-MOS SOS structure and the six-transistor cell. All input/output levels are TTL-compatible.

The memory-access time essentially equals the chip-select and read-cycle times. The low operating power allows these chips to be offered in a low-cost 18-pin package—and this savings helps make up for the increased cost of the sapphire substrate over silicon.



1. Powerful processor. The 16-bit T-88000 microprocessor includes special-function circuitry, such as a parallel multiplier and a barrel shifter, to speed processing. However, the microinstructions are stored off chip, thereby permitting a choice of instruction sets.

micrometers. The process used for the 88000 is a scaled-down version of the one just described, standard C-MOS silicon-gate SOS using depletion-load ion implantation. As with the original chip, n-MOS is used where density is important. Sources and drains are formed by implanted arsenic and boron with an effective channel length of about 2.8 μm. That same process is used for Toshiba's new 4-K random-access memory (see "A C-MOS-on-sapphire memory," p. 112).

The 88000 consists of 12,000 gates using over 30,000 transistors on a die whose dimensions are 6.66 by 7.46 millimeters. It dissipates 0.7 watts, is housed in a 64-pin dual in-line package, and requires only a 5-volt supply.

External instructions

For greater flexibility, the 88000 uses an external store that can hold 256 microinstructions, thereby freeing the hardware from dependency on any particular instruction set. The instruction store is vertically oriented—20 bits wide—allowing easy emulation of other instruction sets.

The processor incorporates two operating modes for either standard or custom macroinstructions. The standard set consists of 92 instructions closely matched to the microinstruction set; in fact, almost every macroinstruction is executed by a single microinstruction.

Using the standard instruction set gains speed because the 88000 provides a fast address-lookup table for it. The on-chip table contains the starting address of the 159 microinstructions that implement the standard instruction set's macroinstructions.

The remaining 97 microinstructions may be used to extend the standard set or to set traps for illegal instructions. Users may extend the set by supplying external starting address for the 97 extra commands. Alternatively, fully custom microinstruction sets may be instituted, with the entire lookup table of starting addresses stored in the same read-only memory as the instructions.

The basic repertoire includes both decimal operations, for business processing, and floating-point operations, for scientific purposes. It also includes a full set of primitives for high-speed input/output, eliminating the need for an independent I/O processor.

Microinstructions are provided to handle the external address-translation hardware, which segments a 16-megabyte space into variably sized pages ranging from 256 64-K-byte pages to 256,000 64-byte pages. The address-expansion logic is built up from standard parts and is tailored to each application.

Designed for speed

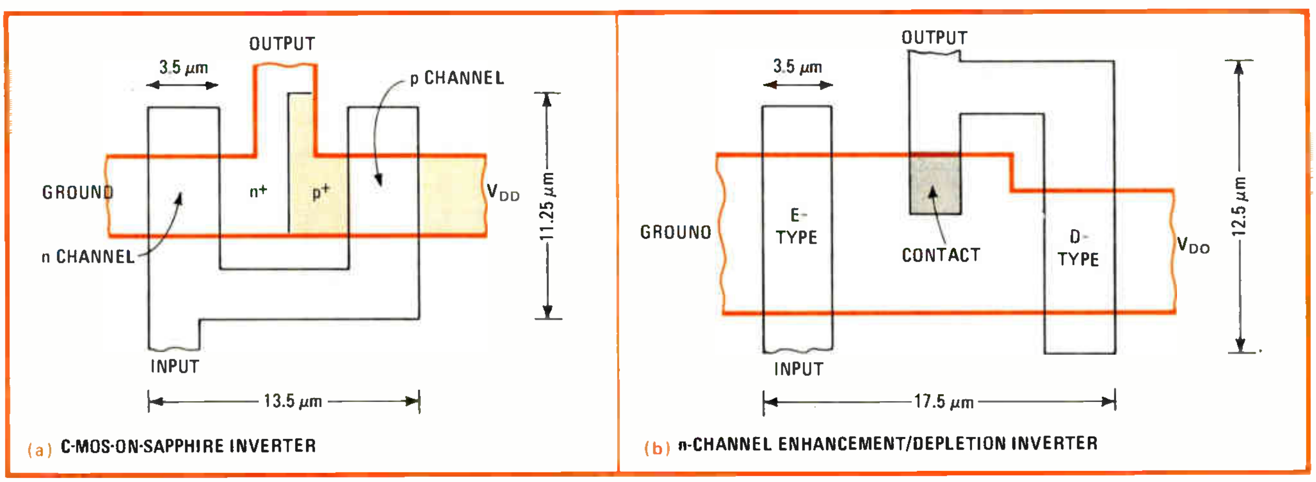
At the outset, the decision was made to make the 88000's architecture adaptive and fast. Its arithmetic performance was targeted to compare favorably with the traditional minicomputer's (Fig. 3) enabling it to be used even for real-time signal processing.

To this end, the chip is equipped with a parallel multiplier, a barrel shifter, and a decimal adder-subtracter. High-speed number crunching, particularly in signal processing, uses an abundance of multiply and shift instructions, making dedicated hardware units practical. The decimal adder-subtracter streamlines business applications.

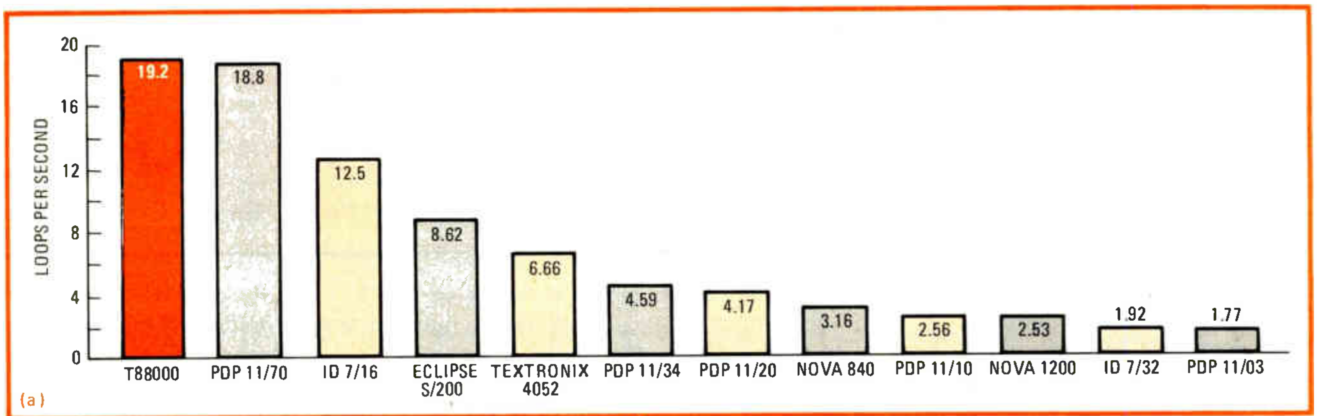
Several benchmarks are provided in the table comparing the processor to Intel's 8086, Zilog's Z8000, and Motorola's 68000. With its parallel multiplier, the 88000 performs a 16-by-16-bit multiplication with a 32-bit result in only four machine cycles (400 nanoseconds a cycle). With the barrel shifter, the processor takes only a single cycle to shift from 1 to 15 bits.

During multiplication, the 88000's internal buses are free for use on another operation, since the multiplier has independent latches on its inputs. In this way, multiplications can be overlapped with add cycles to accumulate the results for iterative multiplication, a common operational sequence in signal-processing applications. The total time for a multiply-and-accumulate operation (with 16-bit accuracy) requires a mere 1.2 microseconds, comparing favorable with dedicated signal-processing chips.

In order to maintain a reasonable pin count, the 88000 makes use of an innovative 32-bit multiplexed common-



2. C-MOS versus n-channel. For most circuits, a higher packing density can be achieved using n-channel devices. However for some simple circuits like this inverter, a C-MOS circuit built on sapphire can actually be smaller, since the output does not connect to a gate.




```
      INTEGER A2 I1(4),I2(3),L(40)
      DATA P1/3.14159/
      P=P1
      A=0.0
      READ(4,100)L,M
100   FORMAT(40A2/16)
      CALL TIME(I1,I2,K1,M)
      DO 10 I=1,N
      F=P/FLOAT(N)
      X=F*FLOAT(I)
      E=ABS(ALOG(EXP(X))/X)-SQRT(SIN(X)
     1 **2+COS(X)*COS(X))
      A=A+ABS(F)
10    CONTINUE
      CALL TIME (I1,I2,K2,M)
      K=K2-K1
      T=FLOAT(K)/1000.0
      A2=A/FLOAT(N)
      WRRITE(5,200)L,N,K1,K2,T,A,A2
200   FORMAT(1H1,/////1H,40A2,/
     1 1H,20X,17H COUNT           = ,I15,/
     2 1H,20X,17H STARTED TIME    = ,I15,/
     3 1H,20X,17H DONE       TIME = ,I15,/
     4 1H,20X,17H EXECUTION TIME  = ,F15.2,
     5            7H SECOND,/
     6 1H,20X,17H TOTAL ERROR     = ,F15.8,/
     7 1H,20X,17H AVERAGE ERROR   = ,F15.8)
      STOP
      END
```

(b)

3. Fast as a minicomputer. The 88000 compares favorably with many popular minicomputers (a). The benchmark program (b) was run on a variety of minicomputers and suggests that a microprocessor-based system can indeed be as fast as a minicomputer.

bus interface. The bus is shared between memory address and data, instruction-store data, and I/O paths. Since most user instructions are 16 bits wide, two can be fetched simultaneously. Careful evaluation by the designers has shown that the 88000's four-stage queue serving as an instruction prefetching buffer is sufficient, since the next instruction is always in the queue except after a branch instruction.

COMPARISON OF NEW 16-BIT MICROPROCESSORS				
Capability	T88000	8086	Z8000	68000
Addition (μs)	0.4	0.38	1.0	1.0
Multiplication (μs)	1.6	18.75	17.5	17.5
Division (μs)	13.6	22.88	23.75	39.5
6-bit shifting (μs)	0.4	9.0	8.25	4.5
Floating-point instructions	yes	no	no	no
Decimal instructions	yes	no	no	no
Memory space (Mb)	16	1	8	16
Clock frequency (MHz)	10	8	4	8

Another advantage of the 32-bit bus is that it allows a rather long memory cycle time (600 ns), even for the full-speed 400-ns instruction-cycle time. Also, instruction store cycles of 400 ns can be met with widely available memories offering 200-ns access times.

Variable bits

The interfacing scheme of the 88000 uses 12 bits on an independent bus to address the 4-K-byte instruction store; and on the common bus, 20 bits for microinstruction data, 24 bits for main-memory addresses, and the full 32 bits for main-memory or I/O data transfers. The instruction store can easily be expanded, since it is implemented with 24-bit words of which only 20 are used for microinstruction data. The 4 extra bits can be used to point to an address beyond 4 kilowords.

Internally, a full complement of registers is provided to support the 88000's high-speed operations. There are sixteen 16-bit general-purpose registers that can be used as accumulators or stack pointers or for indexing. Also, there are eight 16-bit working registers for use by the microinstructions. Both register sets have two ports to the internal buses so that two transfers can be made simultaneously. In this way, two operands can be fetched from the register files and fed to the inputs of the arithmetic and logic unit or multiplier in a single cycle.

Also, all functional subunits have input latches to free the internal buses from having to wait for operations to terminate. To increase processing speed further, the 88000 adopts a pipelined control structure in which instruction fetching, decoding, and execution operations are overlapped.

Toshiba is planning to sell a whole range of application boards and systems using the 88000. These products will be very compact, yet will pack the power of a minicomputer. The central processing unit used for the benchmarks in the table occupies about half of a 12-by-12-inch four-layer printed-circuit board. The other half of the board is packed with 64-K dynamic RAMs to provide 512-K bytes of main memory. □

CUSTOM MICROPROCESSOR POWERS OFFICE WORK STATION

by Carl P. Gerstle and Donald A. White, *Digital Equipment Corp., Small Systems Engineering Group, Maynard, Mass.*

□ Generous use of complementary-MOS semiconductor technology in a new processor chip and in many other circuit components imparts high performance and outstanding reliability to a combined small-business computer and office-automation work station. Beneficiary of the C-MOS magic is the DECmate Work Processor, the newest member of the fully compatible family of word- and data-processing systems based on the 12-bit PDP-8 architecture. Its new integrated-circuit processor, called the 6120, runs an extended PDP-8/A instruction set, including memory-address expansion on chip.

For both the 6120 processor and the 6121 input/output controller, C-MOS was deemed superior to less-power–efficient static n-channel MOS technology and also to more complex dynamic n-MOS technology. Although dynamic n-MOS could have reduced the amount of power required, as compared with static parts, a dynamic design would not have been as clean to work with for the logic functions needed.

In the asynchronous environment of static logic, chip designers need not be as precise in planning timing tolerances as is necessary to maintain two-phase clock synchronization in dynamic logic. Moreover, single-step design debugging in static logic allows the designer to see individual problems as they happen at slow clock speeds. The system clock may be brought down to dc if desired, there being no minimum cycling rate required.

C-MOS is superior

The 6120 chip (Fig. 1) was a joint development project between DEC's Small Systems Engineering group and the Harris Semiconductor division of Harris Corp., Melbourne, Fla. It is about three times faster than the predecessor 6100 C-MOS processor used in the earlier WS78 computer.

The speed improvement was measured executing a representative mix of instructions. In fact, the 6120 is even a little faster than a PDP-8/A minicomputer running the software of the WS200 multiterminal word-processing system.

Two differences between the 6100 and 6120 are chiefly responsible for the speed hike. First, the 6120 was designed to perform some operations in parallel, but the 6100 processes all functions serially. For example, the page addresses in memory are calculated at the I/O pins while data is being computed in the arithmetic and logic unit. Secondly, the shrink from 6-micrometer geometry in the 6100 to 4-μm features in the 6120 reduced on-chip capacitance, boosting transfer speeds with little increase in power dissipation.

A significant jump in transistor density on the 6120 owes much to the move to 4-μm technology, but it is also due in part to enhanced on-chip interconnection techniques. The die size of the 6120 is 230 mils by 210 mils—only a 20% increase in die area for a 175% increase in transistor count as compared with the 6100.

Old reliable

The high reliability experienced with the 6100 C-MOS chip in more than four years in the field, as well as the low power consumption and other design benefits of this technology, made it an easy decision to use such logic in the 6120 processor chip. Furthermore, there were many good reasons to extend the use of C-MOS in preference to n-MOS and TTL logic wherever possible among support functions surrounding the central processor.

C-MOS was also chosen for the 6121 custom I/O controller chips designed for this product—two of them on the processor board and one on the optional communications-controller board. C-MOS is used, as well, for the read-only and random-access memories in the control store of the processor board and for the universal asynchronous receiver-transmitters in the serial printer and keyboard control circuitry, also on board. The control memory is used for such functions as self-testing, terminal I/O emulation, floppy-disk control, and a buffer memory and control registers for the video display.

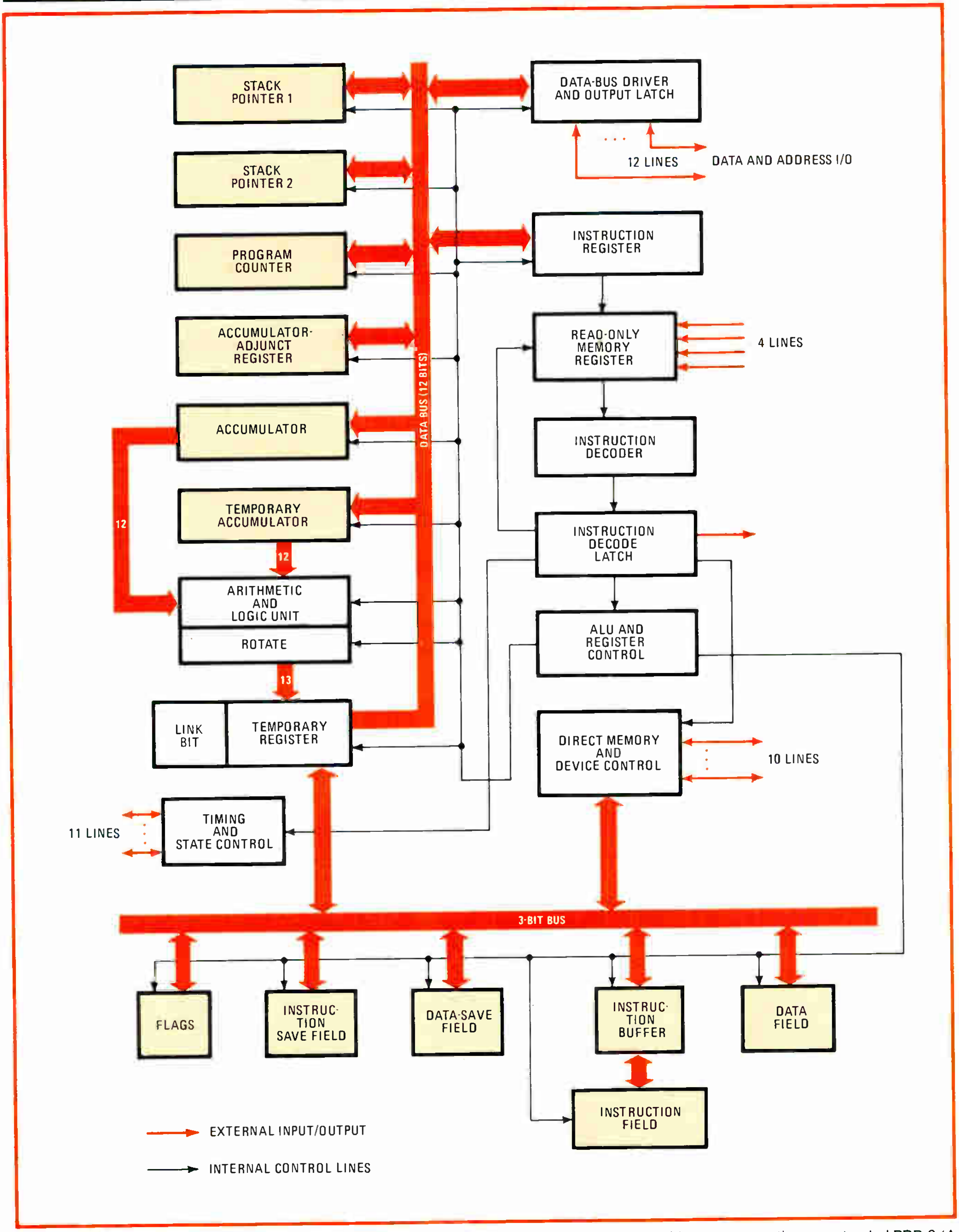
Altogether, there are 27 static C-MOS ICs on the microcomputer board and 14 more on the communications-controller board. However, dynamic n-MOS was chosen for main memory to achieve the maximum storage capacity per dollar. These RAMs are the only dynamic circuitry on the processor board.

Memory control

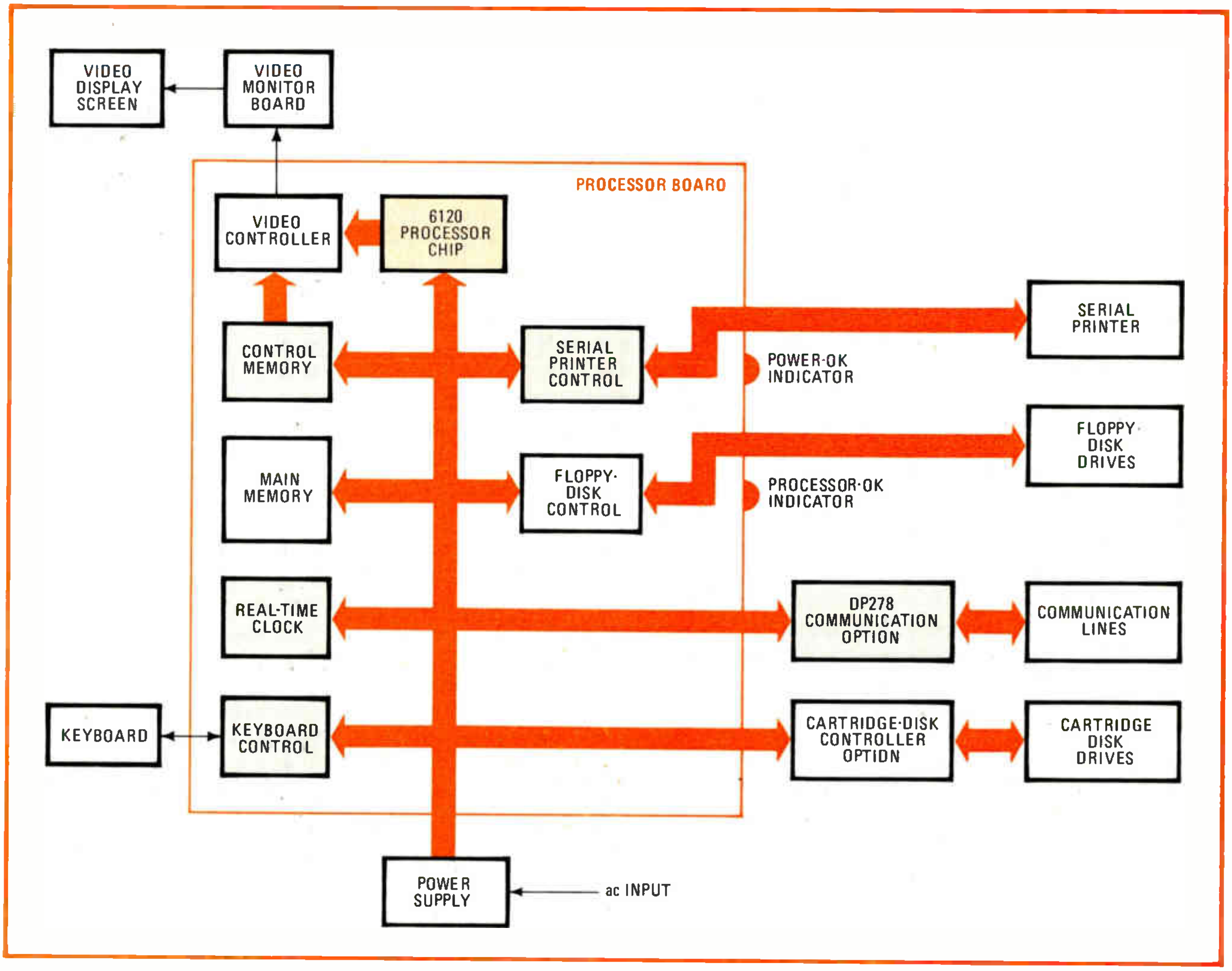
On-chip memory-extension control in the 6120 boosts its addressing capability over previous family members from 4-K 12-bit words to 32-K words in each of two separate memory spaces. In addition, the new chip executes the memory-extension instructions faster. It also contains 12 special-purpose registers and control logic, along with the arithmetic and logic unit.

Extensions to the PDP-8/A instruction set include stack-command macroinstructions that permit more efficient encoding of the ROM-based firmware. Another benefit from the expanded instruction set is the addition of power-up self-test diagnostics. The 6120 costs about the same as the 6100, but by taking over memory-extension control, it reduces total system cost.

The mostly C-MOS, cool-running single-board micro-



1. Chip off the old block. The 6120 C-MOS processor chip implements the much-used PDP-8 architecture, executing an extended PDP-8/A instructions set. The design uses two system buses — the data and address I/O bus and the C-bus — and 12 special-purpose registers (tinted).



2. Energy-efficient worker. The C-MOS–intensive DECmate desktop system packs a lot of function onto a small number of low-power boards. The processor board alone handles eight functions. The building blocks implemented totally or partly in C-MOS are shaded.

computer (Fig. 2), requiring a mere 15 watts, is the controller of all functions in the computer. The 11.1-by-10.5-inch DEC-standard extended quad board contains eight major functional units: the processor, the 32-K 12-bit–word main memory, address space for as much as 32-K words of control memory, a real-time clock, and four control circuits.

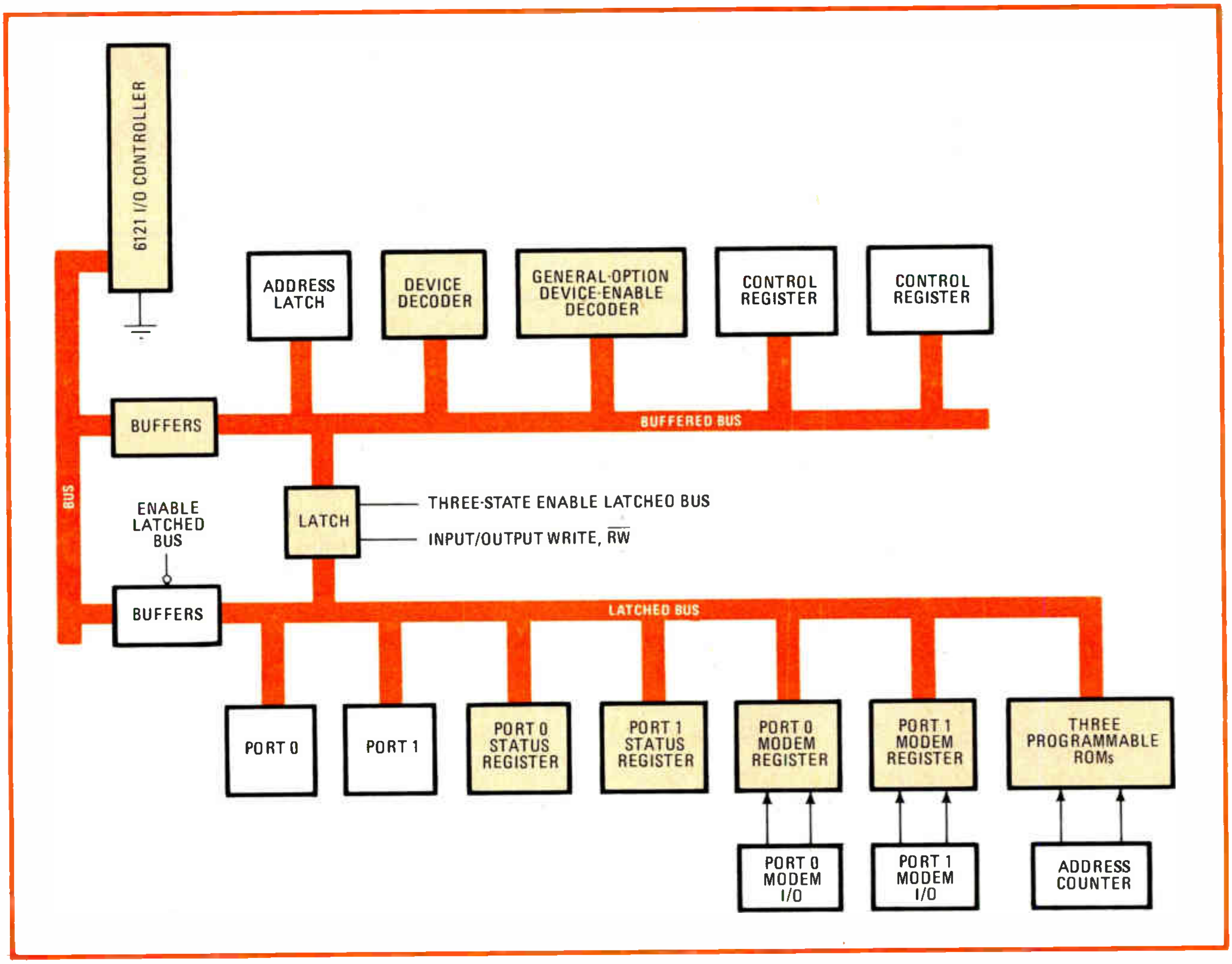
Smaller package

The new chips allow the microprocessor and its main memory to fit on a single board. The equivalent ICs including the 6100 processor in the older WS78 occupy three larger boards and one slightly smaller one. The number of 14-pin–chip equivalents was reduced from 375 in the WS78 to 200 in the DECmate. The 80% net reduction in board area stems in part from the use of large-scale integrated circuits, the other factors being the combining of the terminal and central processors that were separate in the WS78 and the tighter board layout possible with improved printed-circuit boards.

The almost 50% reduction in chip population increases long-term reliability because it reduces the total number of gold-wire bonds subject to temperature cycling and possible failure. Equally important is the massive switch to cool-running, low-power C-MOS. The temperature rise on such a die is only about 25% above the ambient temperature, while the rise on a similarly sized TTL or n-MOS die is roughly 100%. In the latter case, then, a much greater temperature strain is imposed on wire bonds and metal lines, as well as on the IC devices themselves.

Like any MOS part, a C-MOS IC is self-limiting—circuit currents drop as temperature rises. In TTL parts, higher temperatures result in increased currents—which can ultimately lead to cyclic degeneration or thermal runaway. Since C-MOS runs cooler than other MOS technologies, the resultant parts offer a more generous temperature safety margin.

Through the use of static C-MOS logic in the 6121 I/O controller, board space and power were saved again. Because the 6121 spends much of real time in an inactive state, dynamic logic would have required a good deal of refresh circuitry either on the chip or in discrete logic. The three 40-pin 6121s perform I/O control for five



3. C-MOS to the rescue. When the DP278 communications controller for the DECmate was using too much power, consumption was cut from 6 to 4 watts by using the C-MOS 6121 I/O controller chip and replacing 16 TTL chips with 14 C-MOS chips (tinted).

channels each. They are programmable, so the board designer has more flexibility in establishing channel characteristics.

C-MOS logic also offers reduced ringing and overshoot—a cleaner signal that is especially valuable on a bus. There tend to be fewer difficulties with electromagnetic and radio-frequency interference—a point that has increased importance today in view of the new Government emissions regulations on office equipment. The noise margins offered by C-MOS are superior to those of TTL, there being a wider tolerance for noise introduced between the maximum input and output low voltages: 1.4 V versus 0.4 V. Similarly, a C-MOS receiver has a high-voltage margin of 1.4 V versus 0.4 V.

Little watts

Low power consumption, chiefly as a means of optimizing reliability, was, from the beginning of the design effort, a principal reason for specifying C-MOS in both custom and off-the-shelf parts. Whenever off-the-shelf C-MOS chips were available, they were used in preference to their TTL counterparts for bus buffering, special hardware registers, and dedicated address decoding. In general, this reduced system bus noise and power requirements.

The system power requirements were set at a low enough level so as to ensure reliability within a convection-cooled terminal housing. An important design goal was as small a power supply as possible, while maintaining the ability of adding options. A 60-W supply is used, requiring 75 W from a wall outlet. As a comparison, the WS78 used somewhat over 200 W.

Well into the design effort, the small power supply, coupled with a fixed power allotment for the processor board and any further options, necessitated a very limited power allotment for the DP278 communications-control optional board. The DP278 was originally designed in n-MOS (four ICs) and 7400-series TTL parts to minimize cost. The TTL, however, caused the module's power requirement to be 50% over its allotment. So in the 10 functions shaded in Fig. 3, C-MOS parts were used to cut the projected power to 4 W at 5 V dc. Replacing 16 TTL chips were 14 C-MOS equivalents—about 19% of the module. □

COOL-RUNNING 16-K RAM RIVALS N-CHANNEL MOS PERFORMANCE

by Frank Lee, Norman Godinho, and Chun P. Chiu, *Integrated Device Technology Inc., Santa Clara, Calif.*

☐ Complementary-MOS has successfully begun to compete with n-channel MOS as the technology of choice for memory and microprocessor applications. The competition stems not only from C-MOS's lower power dissipation, but also from the rapidly diminishing differences in speed, chip size, and price that exist between the two technologies. Certainly there remains a price premium for C-MOS products, but that difference promises to narrow considerably (see "Closing the price gap," on the opposite page).

As densities increase, all integrated circuits dissipate more power. However, a point is reached where heat dissipation becomes a barrier to further integration and forces the chip designer to adopt special packaging techniques or—as with many n-channel MOS static random-access memories—to include additional circuitry whose only function is to power down the product during periods of nonselection.

With C-MOS, there is no need for special power-down circuitry. When the device is not toggling, it is inherently powered down. Compared with a powered-down n-MOS device, the C-MOS device will dissipate two orders of magnitude less power.

In addition, since C-MOS integrates both p- and n-type devices, npn transistors to handle fast, high-current drive functions—such as those found in a RAM's data-output circuit—can be routinely included. Designers can mix n-channel and p-channel MOS and bipolar devices to implement various linear circuits, such as analog-to-digital converters and comparators. Thus, by taking advantage of the different types of devices available through C-MOS technology, it has proved possible to build a large-capacity static memory chip, such as the 2-K-by-8-bit IDT6116, that is fast, physically small, and low in power dissipation.

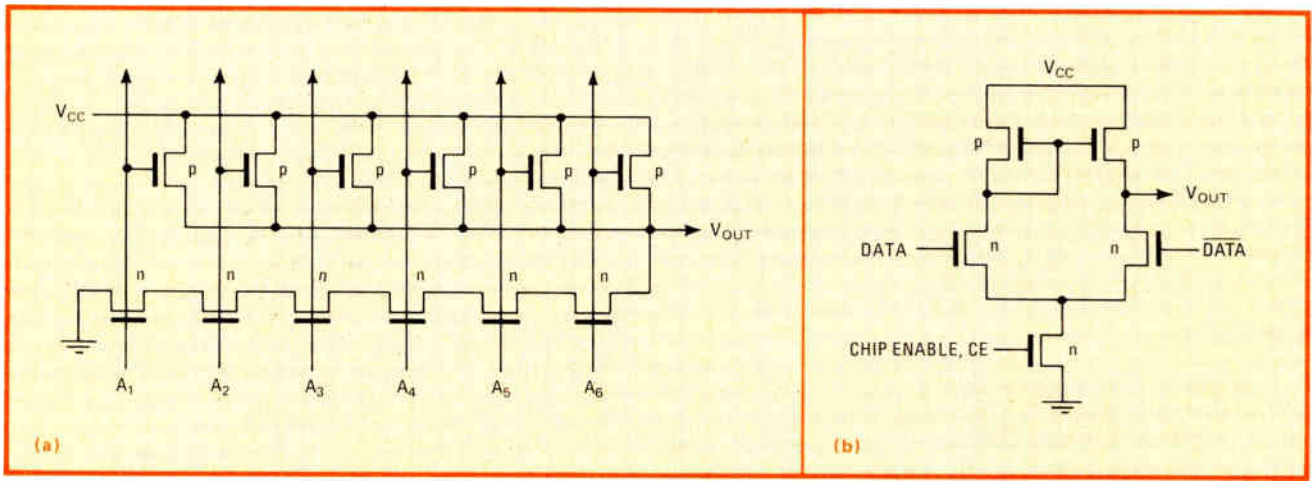
Since the storage array occupies the most die area on a memory, some static RAM manufacturers have switched from six-transistor cells to four-transistor cells with polysilicon load resistors. Such a four-transistor cell with polysilicon loads is found in the IDT6116, and area is further conserved by using a second polysilicon layer so that the load resistors can be located directly above their driver transistors.

Main squeeze

Circuit density was also increased through other space-saving techniques, like self-aligning field implants and edge-coincident contacts. As a result, even when compared with other static RAMs incorporating four-transistor cells, the IDT6116 is smaller. In fact, the chip's 1.1-square-mil cells are the smallest of any byte-wide RAM made with comparable design rules, and its 34,200-mil² chip area measures less than that for any 16-K byte-wide RAM.

The remaining die area is taken up with decode, control, and input/output circuitry. Except for the data-output circuitry, all of the peripheral circuits are implemented using complementary devices. Here the requirements are for high speed and low power; space was less of a consideration because this area is much smaller than that of the array.

Circuitry such as that for the decoder takes full

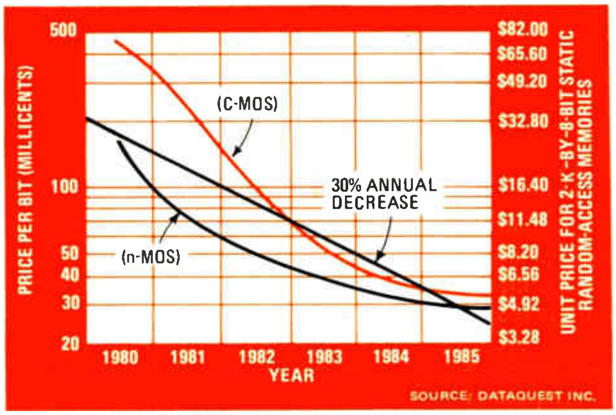


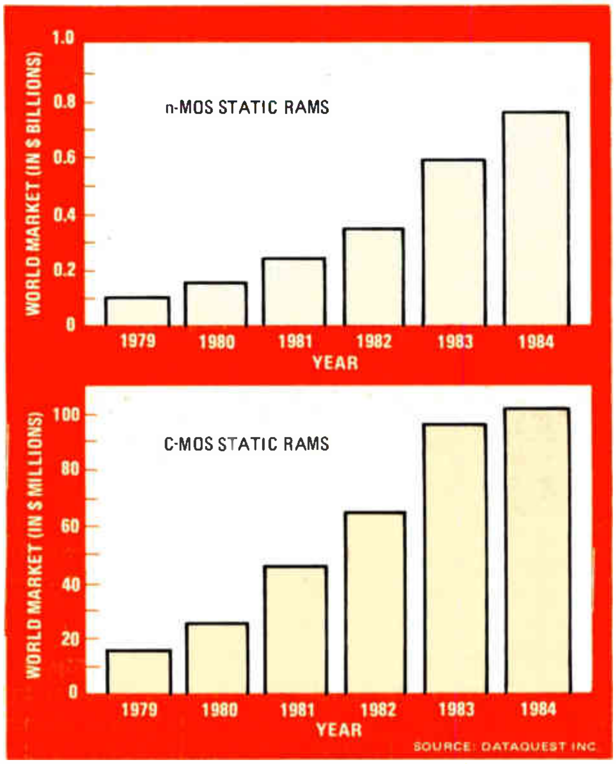
1. Making C-MOS work. Circuits in the 16-K memory use p-channel transistors for reasons other than low power. In an address decoder (a), they result in an efficient and elegantly simple implementation. The differential sense amplifier (b) has extremely high gain.

Closing the price gap

One obvious disadvantage of C-MOS today is its higher price than n-MOS. However, the gap is expected to narrow significantly by the end of 1984 (see chart below). The price of a 2-K-by-8-bit C-MOS RAM is expected to drop from an average of $24 down to $6.00. In the same time period, a byte-wide 16-K RAM is expected to decrease from about $10 to $4.50. In other words, the price premium for C-MOS will shrink to only 20%.

In terms of volume, 1981 will end with 45 million C-MOS static RAMs sold for a value of $250 million. The outlook for 1984 is an encouraging 100 million units sold for a market of $750 million (see graph at right).





advantage of C-MOS technology (Fig. 1), and as a result, its power consumption is virtually zero during idle periods. The sense amplifier, shown in Fig. 1b, uses a C-MOS differential amplifier that supplies both a large voltage gain and dc voltage level-shifting in a single stage. By contrast, a similar function processed in n-channel technology would typically require two to three stages for the required gain and dc levels.

The data-output circuitry benefits from the ease with which npn transistors can be created with C-MOS. With an npn transistor acting as an active pull-up device and an n-channel MOS field-effect transistor for active pull-down, the memory's data-output characteristics are far more symmetrical and sharper than those of an n-channel–only configuration.

Maintaining speed

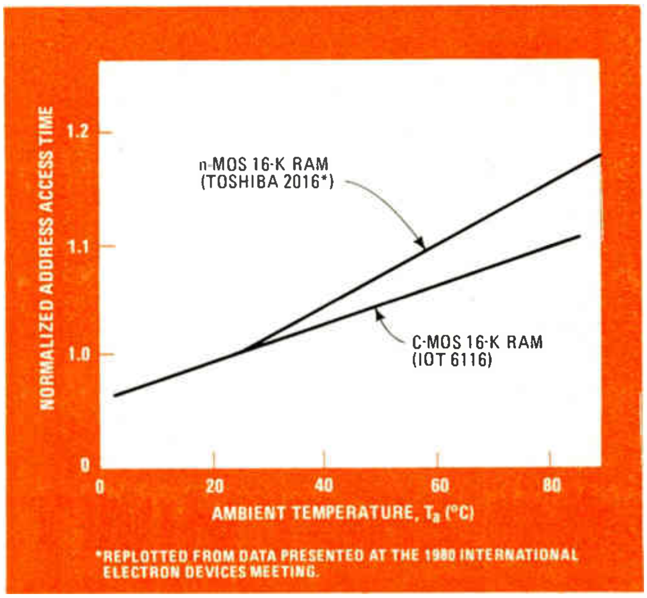
An additional asset is the chip's ability to maintain speed with rising temperature. Heat slows down n-channel MOS FETs but tends to hasten the speed of npn transistors. Since the output exploits both device types, the npn device somewhat compensates for any slowing of the n-channel device. Empirical data indicates that, for the 20°-to-80°C temperature range, the IDT6116's address access time increases only 9% compared with 15% for a comparable n-channel MOS version (Fig. 2). The memory also can retain data with the supply voltage as low as 2 volts in the data-retention mode.

Access times of less than 100 nanoseconds were once the exclusive domain of bipolar RAMs. Only recently has an 16-K MOS RAM broken the barrier. The standard version of the 6116 is speed-selectable for 70-, 90-, and 120-ns access times. In its active mode, the fastest unit consumes a maximum of 500 milliwatts; in standby it uses a mere 10 mW. A lower-power version has speed selections of 90, 120, and 150 ns. Typically, this device has a 20-microwatt power appetite in standby. The chip needs only a single 5-V power supply, conservatively rated at a ±10% tolerance. The memory is housed in a 24-pin plastic standard dual in-line package.

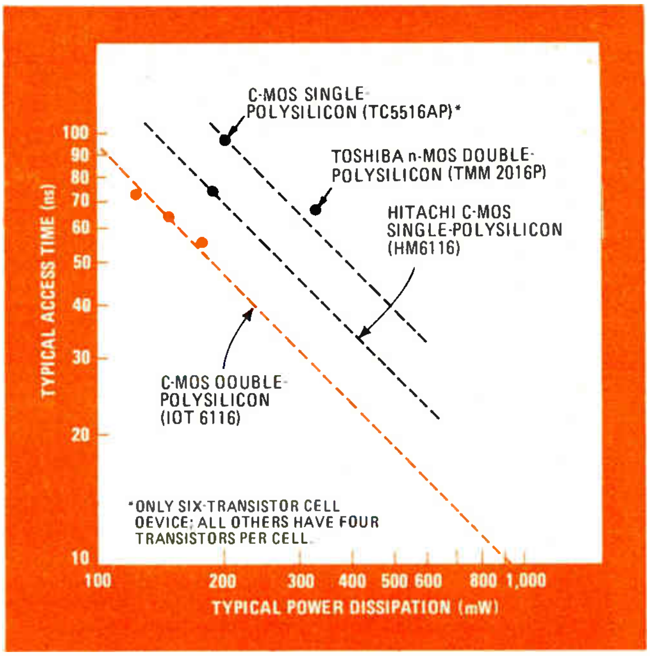
In considering speed-power relationships, Toshiba Corp.'s TC5516AP and n-MOS TMM2016P 2-K-by-8-bit static RAMs are similar enough to the 6116 to allow a fair comparison to be made on the basis of data presented in papers delivered at the 1979 and 1980 International Electron Devices Meetings [*Electronics*, Nov. 20, 1980, p. 136 and Dec. 6, 1979, p. 124]. Like the IDT6116, the 2016P part uses 3-micrometer design rules, has four-transistor cells, and is built using two layers of polysilicon.

Both parts achieve higher speeds at the expense of power dissipation. Using 70 ns as the point of comparison, the IDT6116 dissipates approximately 130 mW; the n-channel product requires more than twice that amount, or 280 mW (Fig. 3).

Hitachi Ltd. detailed a comparable 2-K-by-8-bit C-MOS static RAM, the HM6116, at the 1980 International Solid-State Circuits Conference [*Electronics*, Feb. 24,



2. Slower rise. To sharpen up transfer characteristics, the IDT6116 uses bipolar npn transistors as active pull-up devices. Rising temperature slows down n-channel MOS devices but speeds up the npn transistors. This compensation tends to stabilize access time.



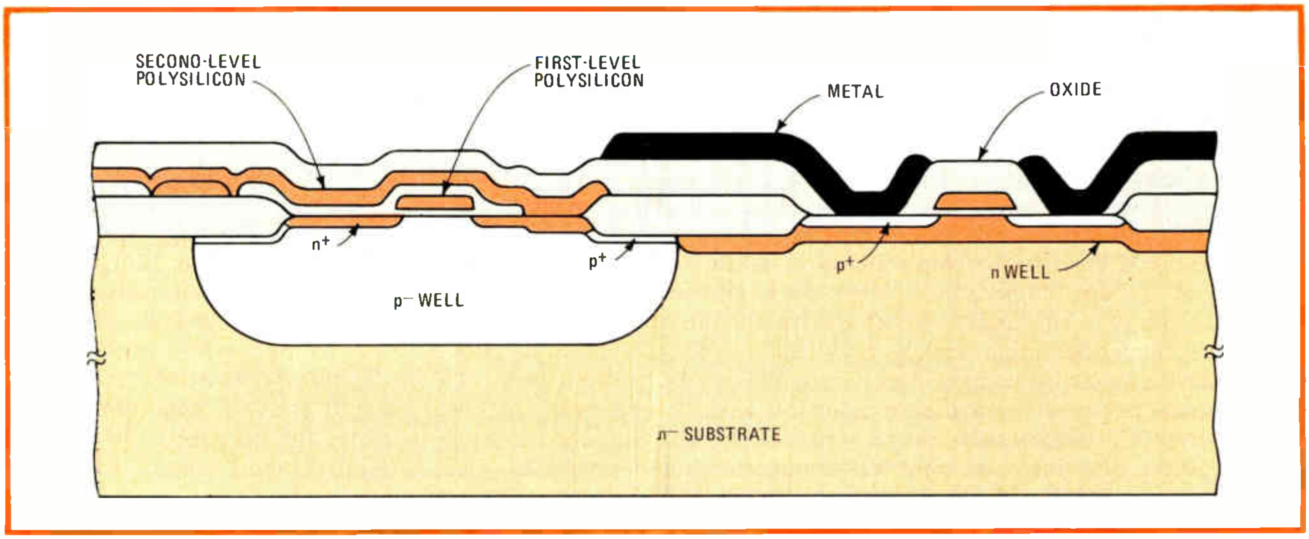
3. Competitive. The power-delay products of four 2-K-by-8-bit static MOS random-access memories are compared. One of Toshiba's chips is made from n-channel MOS; the others are C-MOS. The IDT6116 scores the highest because it combines both.

p. 141]. Again, choosing 70 ns as the point of comparison, the Hitachi part consumes 200 mW compared with the 6116's 130 mW. The lower power dissipation of the IDT6116 is largely due to the lower bus-line capacitance loading resulting from its double-polysilicon technology.

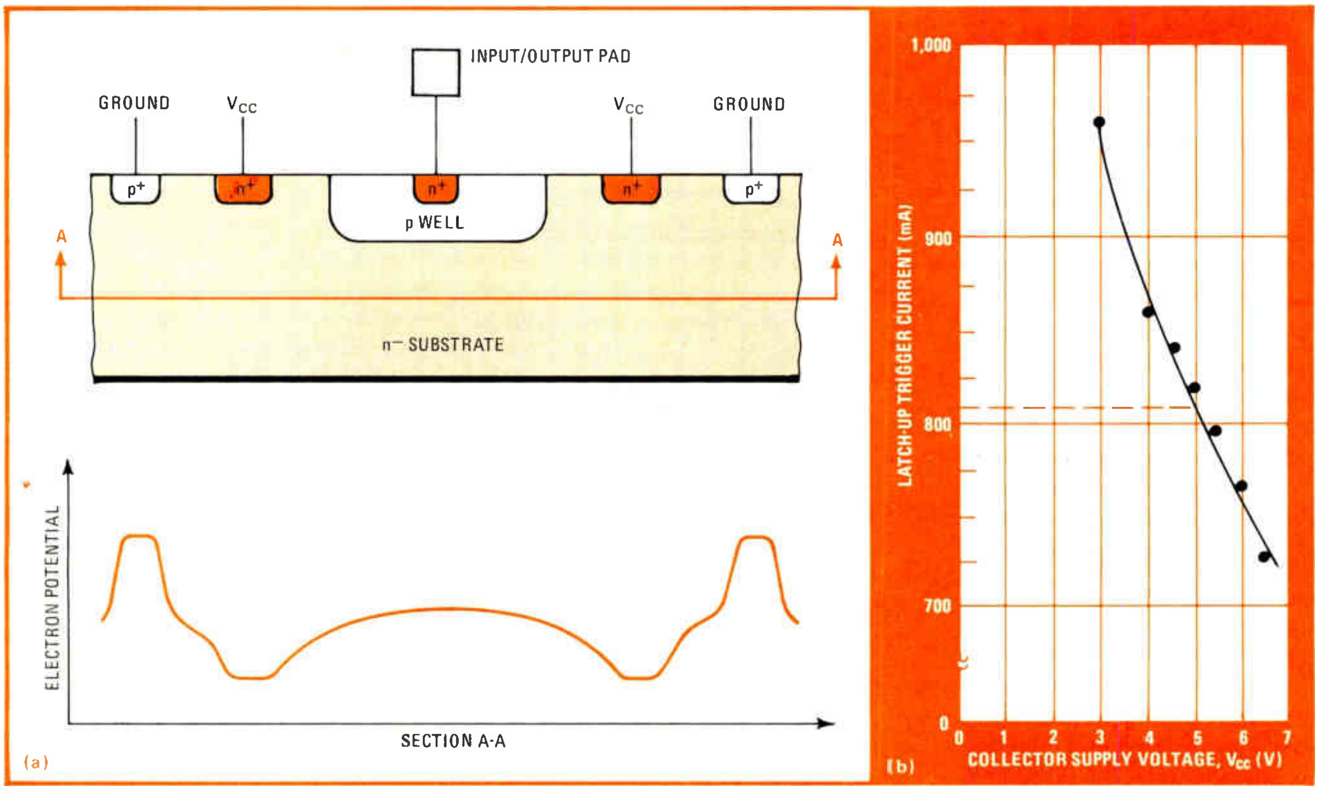
One problem that has affected RAMs in general is alpha-particle–induced soft errors. Before an alpha particle comes to rest in a chip's substrate, it leaves a trail of electron-hole pairs in its wake. This temporary charge can cause a nonrepeatable error if it is close enough to a sense line or cell storage node. For the most part, C-MOS RAMs are less susceptible to these soft errors. The IDT6116 is even less vulnerable with its shallow p well. Alpha particles usually burrow deeper than the well and the charge created is swept away to the n-type substrate or ground line.

Both Integrated Devices and Bell Laboratories use a dual-well design in their C-MOS processes, and the philosophical rationale is the same. In both cases, the structure helps to suppress punch-through and minimize junction capacitance. However, Bell Labs uses a heavily doped n-type substrate with a lightly doped n-type epitaxial layer. The IDT6116, on the other hand, has a lightly-doped substrate with no epitaxy to reduce process complexity (Fig. 4).

Another problem that at one time plagued C-MOS



4. Process cross section. To optimize n- and p-channel transistors, twin lightly doped wells are employed. Such a structure helps suppress punch-through and minimize junction capacitance. A lightly doped substrate was used in lieu of an epitaxial layer to save cost.



5. Latchup suppression. One of the techniques used to subdue latchup in the IDT6116 is a double-ring guard band (a). This plus careful circuit layout and some proprietary methods all but eliminated the latchup phenomenon unless a huge 800-milliampere trigger is applied (b).

devices is termed latchup. Due to their proximity, the p- and n-channel devices can produce, in effect, a pnpn or npnp structure that will act like a silicon controlled rectifier under certain circumstances. Many techniques have been used to deal with this problem, including wider feature spacing, buried layers, gold doping, and guard rings. These techniques have brought a degree of success; however, some of them, like gold doping, are difficult to control and add process complexity. And wider spacing is obviously not in keeping with higher levels of integration.

Latchup in the IDT6116 is suppressed through a combination of careful design layout, selective use of guard rings, and some proprietary techniques. Input/output circuits are normally more sensitive to latchup, so only npn and n-channel devices are used. This eliminates latchup due to hole injection. To reduce latchup due to electron injection, I/O circuits are surrounded by an n^+ guard ring that acts as an electron collector. Should some electrons pass through this ring, an outer p^+ region acts to drive them back into the n^+ collector (Fig. 5).

The results have been gratifying. With a 5-V supply, at least 800 milliamperes of trigger current are required to cause latchup, as shown in Fig. 5b. This compares favorably with results achieved through more expensive and roundabout techniques.

In view of its design rules, there is certainly room for scaling down the IDT6116, if only on the basis of available lithographic equipment. However, before attempting to shrink the design, it had to be determined how the move would affect critical parameters, such as the threshold and drain-breakdown voltages.

The IDT6116's present CMOS-I technology uses 3-μm p- and 2.5-μm n-type channel lengths. With V_{cc} equal to 5 V, inverter delays are about 430 picoseconds per stage. While looking at the variations in threshold and breakdown voltage as the channel's effective length and width were reduced, it was found that a scaled-down CMOS-II process with 2.5-μm p-channel and 2-μm n-channel lengths would result in 250-ps delays with a 5-V supply.

Tests of the process confirmed this and suggested that even better speed-power products were in store. One interpretation of this is faster products with the same power dissipation as current ones. The byte-wide IDT6116 is just right for applications in industrial control, instrumentation, data terminals, and some military gear. To serve the market for cache memory and its special requirements for error detection and correction, a much higher-speed 16-K-by-1-bit C-MOS static RAM will be offered. On the drawing board also is a 4K-by-4-bit product specifically suited for high-speed, number-crunching computers like those in military.

Once CMOS-II is on line, this product line will be enhanced with 16-K RAMs having a variety of speed and power characteristics and with a 64-K static C-MOS RAM. With the densities and power-dissipation characteristics already achieved in RAMs, C-MOS will no doubt be able to successfully compete with n-channel MOS at 64-K and higher levels of capacity. □

PROM NEEDS FAR LESS POWER THAN BIPOLAR COUNTERPARTS

by Russell M. Pate and Richard Goslin, *Harris Corp., Semiconductor Digital Products Division, Melbourne, Fla.*

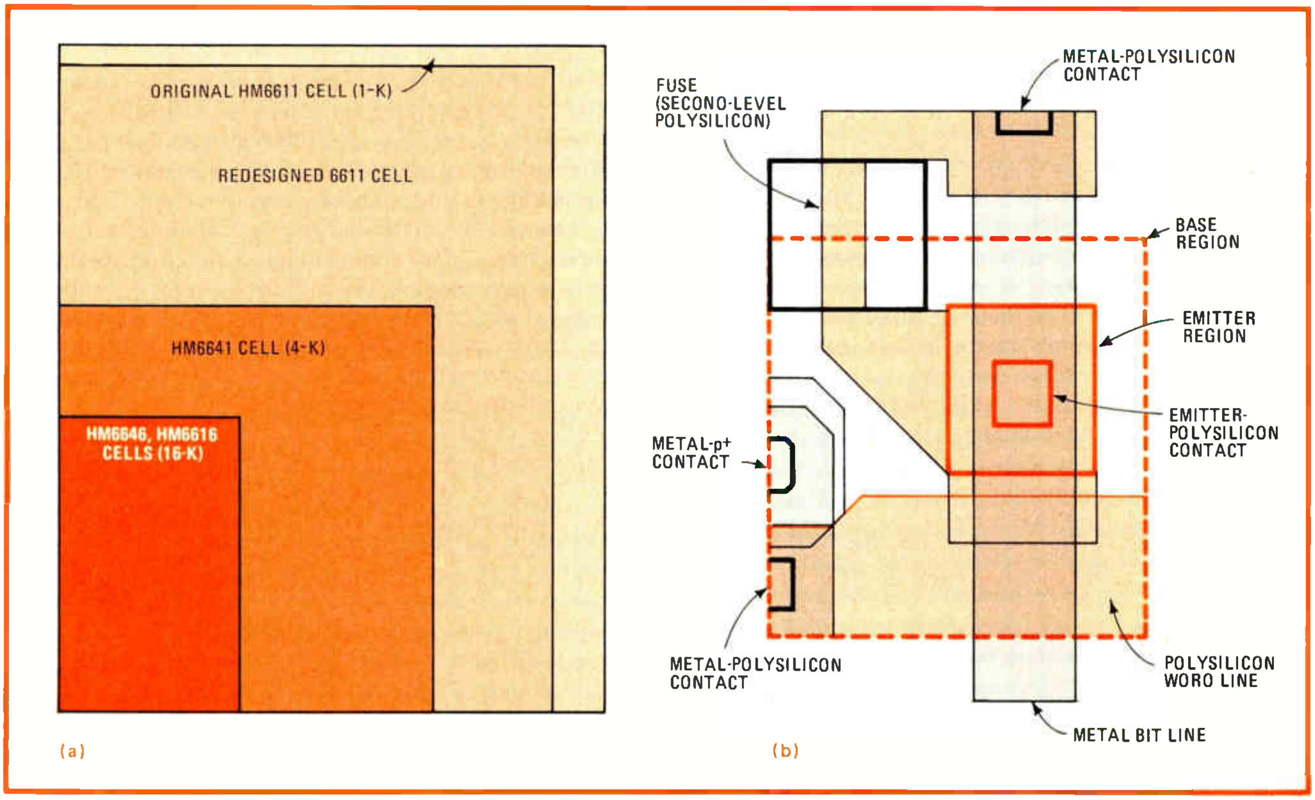
☐ Most complementary-MOS parts were first manufactured in bipolar technology, and then redesigned in n-channel MOS for higher packing density and lower cost before winding up in C-MOS for the lowest possible power consumption. The development of programmable read-only memories at Harris Corp. is not following quite this route: the intermediate n-channel implementation is being bypassed for the advantages of C-MOS. Compared with other field-programmable memories currently available on the market, the firm's continuing series of 1-, 4-, and now 16-K C-MOS fusible-link PROMs have a lower speed-power product than do any existing n-channel MOS or bipolar design.

In addition, data retention is far superior for such a PROM than for a floating-gate-type erasable storage memory—even under adverse radiation and temperature conditions. C-MOS PROMs are capable of reliable operation over the entire military temperature range of −55° to +125°C, and several users have applied them in systems that must operate above an ambient of +125°C. As a result, applications for C-MOS PROMs include low-power handheld microprocessor-based instrumentation and communications systems, remote data-acquisition and processing systems, processor control storage, and synchronous logic replacement.

Quadrupling density

The original chip in the PROM series, the 256-by-4-bit HM6611, had a 5.84-square-mil memory cell consisting of a polysilicon fusible link connected to the drain of a p-channel MOS transistor. It was fabricated using self-aligned silicon-gate technology employing a single level of polysilicon. For manufacturing simplicity, the fuses were deposited during the same process step used to form the gates of the MOS transistors.

To deliver enough current to blow a fuse through the MOS devices, high-voltage pulses of approximately 40 volts were required. The devices supplying this programming current within each cell had to be large and well-supplied with guardbands to prevent interaction with



1. Shrink plan. The cell size of 1-, 4-, and 16-K complementary-MOS fusible-link programmable read-only memories has diminished markedly (a). Two levels of polysilicon and a compact layout (b) give the 16-K chip an 0.8-mil²-cell, which is 65% smaller than the 4-K cell.

other on-chip devices, thus limiting density. The chip, consisting of 1,024 bits, had a chip area of 28,182 mil².

The 6611 was later redesigned with two levels of polysilicon for improvements in performance and programming yield. The fuses use the second level of polysilicon for better control of their necks' width and thickness without affecting the gates of the MOS transistors. With independent process control of the neck, the fuse could be thinned down, thus requiring less power to program. The programming voltage was indeed reduced to approximately 30 V; however, device size was still limited by the large MOS transistor in the fuse path and the guardband required.

Also, in this redesign, the second polysilicon level was wired in parallel with the first level's word line to reduce the RC delay across the matrix, thereby improving performance. The redesign has a 5.11 mil² cell area and a chip size of 23,660 mil²—a 17% reduction in die area from the original 6611.

Both the original and the redesign draw only typical C-MOS leakage currents in the standby or deselected mode. In the enable mode, however, dc currents on the order of 0.5 to 1.0 milliampere pass through each unprogrammed fuse of the addressed word and are detected by the sense amplifiers. Power consumption while reading is therefore a function of the number of bits blown in the word being read.

Advancements

The 4-K HM6641 improved upon density, speed and power consumption of the 6611 through architectural changes and process advances. In fact, the 6641 memory cell is 60% smaller than that in the original 6611.

Currently in the preproduction stages of development are two 16-K C-MOS PROMs: the HM6646, organized as 4 K by 4 bits, and the HM6616, organized as 2 K by 8 bits for a 2716-compatible pin out. The cell size is 0.795 mil²—a 65% reduction from the 6641, as shown diagrammatically in Figure 1. These memories are fabricated with 2.5-micrometer ground rules and have an architecture similar to that of the 6641, except that the outputs can be disabled by the enable input. Due to the increased packing density obtained through device scaling and process improvements, the 16-K C-MOS PROM family is expected to have access times much less than 175 nanoseconds.

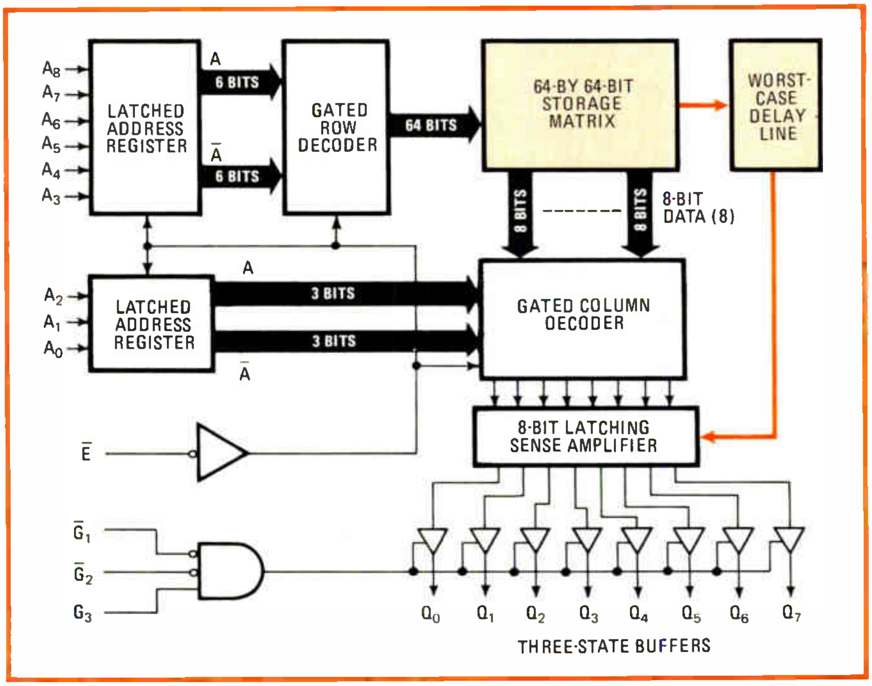
For more speed at less power, synchronous designs were chosen for the 6641, 6646, and 6616. Valid matrix data is latched at the sense amplifier, and the fuse-reading currents are shut off, causing the reading current in these parts to be virtually independent of the number of bits blown in a word. This was accomplished by gating the sense amplifier latches through a worst-case–delay path consisting of the row and column decoder and matrix delays, plus an additional delay (Fig. 2). Latching the output data in this manner insures that the internal delay line tracks actual access delays in spite of process variations. The outputs remain controlled by the output-enable signals.

Packing with bipolar

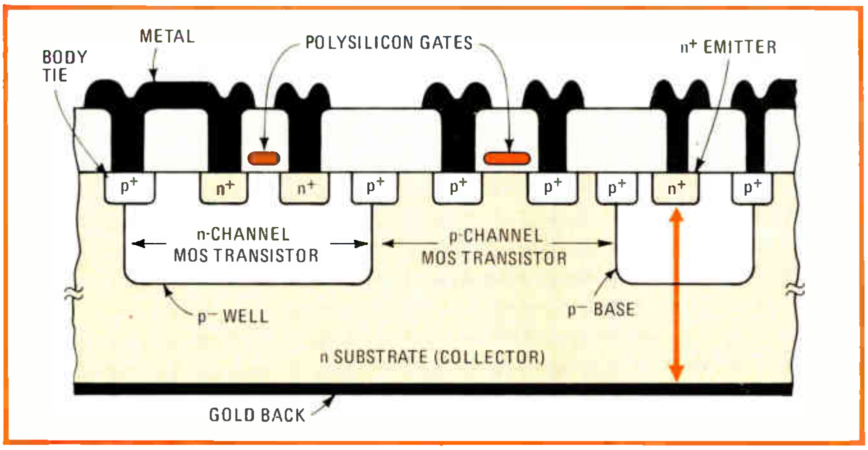
Although the main factor limiting C-MOS PROM density has been the size of the MOS transistors that must carry the fusing current, the limiting factor is now the dimensions of the fuse itself. Cell packing density has been enhanced in the 4- and 16-K designs by using a vertical npn transistor inherent with the p-well silicon-gate C-MOS process (Fig. 3). The npn device is operated in the emitter-follower configuration, as a very good current amplifier to deliver the power that is needed to blow a fuse.

A direct contact from the polysilicon fusible link to the n^+ emitter is also permitted in the process, which helps to reduce cell size by allowing the fuse to be placed directly over the cell transistor. The substrate functions as the collector for the vertical npn transistor and the V_{cc} collector connection is then picked up from the substrate tie-off.

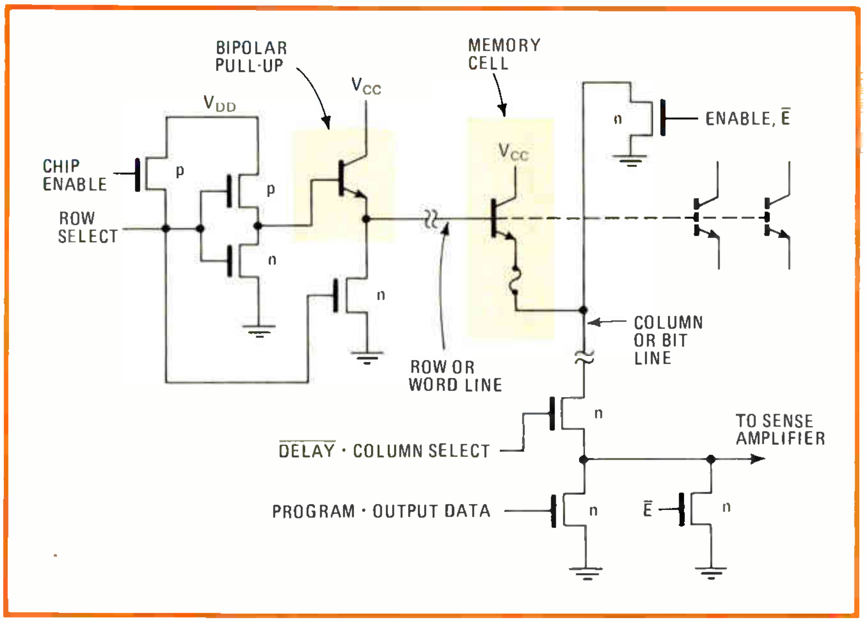
Initial characterization of the bipolar transistor showed a typical collector resistance on the order of 800 to 1,000 ohms, which appeared to be too large to pass the current required to program the fuses. But subsequent investigations uncovered a very useful phenomenon: as the collector current was increased, resistance dropped to



2. Normalizing circuit. The sense-amplifier latches are gated through a worst-case delay path to ensure that the access time remains the same despite process variations. Data output is still controlled by output-enable signals, however.



3. C-MOS plus bipolar. P-well C-MOS has a vertical npn bipolar transistor built right in. Current flow through this device is depicted with the heavy color line. This current is high enough to blow the polysilicon fuse because the npn transistor acts as an emitter follower.



4. Circuit tricks. The bipolar pull-up device aids in driving capacitive loads. Programming is performed by raising V_{cc}, forcing data onto the output lines, and applying a program-enable pulse. There is no dc path through the fuse while reading.

a value of between 100 and 200 Ω. Mathematical modeling revealed that this effect is produced by spreading of the emitter's depletion region into the lightly-doped base region. Propagation and access times were also reduced by using this npn transistor to assist C-MOS inverters in driving highly capacitive nodes such as those for clock and word lines (Fig. 4).

Deposition and fuse geometries

The polysilicon fuses lie on a thermally grown silicon dioxide insulator approximately 1,000 angstroms thick. An opening is made in a protective SiO_2 layer directly over each fuse to minimize heat dissipation to surrounding materials during fusing (when molten polysilicon temperatures will exceed 1,400° C) and to increase the speed of polysilicon separation. After gap formation, a permanent high impedance (megohm) condition is created. In addition to the data-matrix fuses, a row and column of test fuses are included in all the C-MOS PROM designs. These are blown when probing the wafer to assure a high programming yield.

In constructing the fuses, a sheet of intrinsic polysilicon is vapor-deposited over the entire wafer surface and then doped, normally with phosphorous, to achieve the desired fuse resistance in ohms per square. The polysilicon is then selectively etched over the matrix area to form the fuses. The fuses are connected to the emitter of the cell-driving transistor through an aperture to a diffused conductor. Their other ends attach to the column lines through a direct contact to the metallization.

As cell and fuse geometries decrease in size, the dimensions of the fuses and the accuracy of the processing become increasingly critical. As noted, a separate polysilicon fuse deposition step is used in the 4- and 16-K parts to increase control of critical fuse parameters. Further precision in fuse geometry is gained by using what is termed a half-dogbone, or bar, shape rather than the standard hour-glass shape which does little to reduce the effects of material bridging. The wider ends of the fuse are necessary to insure good contact between conductor and fuse.

Figure 4 illustrates the programming and reading path of a memory column in a newer family member. There is no dc path through the fuse during a read operation; only during programming are dc paths other than those carrying normal C-MOS leakage currents present in the PROM. Programming is performed by raising V_{cc} to 12.5 V, forcing data into the output lines, and applying a 12.5-V pulse to the program-enable input ($\overline{PE}$), which is used only during programming and is otherwise tied to ground. The column bit lines are precharged during the disabled period (in this case to a low state through a small n-channel device to ground), and the substrate npn transistor is used to speed the column-line transition from a precharged low to high if the cell data is a logical 0; that is, with the fuse intact.

Otherwise, the bit lines will remain at ground in the precharged state and no transition will be necessary for valid data to propagate to the sense amp and outputs. The fuse's load is primarily one of parasitic capacitance, reducing read currents to a small transient value. □

HIGH-PERFORMANCE PROCESS FITS SPEECH SYSTEM ON A CHIP

by Hiden Hara, Shuichu Torii, Yochitomi Toba, and Kosei Nomiya, *Musashi Works, Hitachi Ltd., Kodaira, Tokyo, Japan*

☐ Though speech synthesis is an attractive premium in many industrial and consumer products, the complementary-MOS process alone makes it applicable to hand-held battery-driven devices like talking calculators and time-telling watches. But a C-MOS implementation of a speech chip is not enough—only a single-chip speech system satisfies the cost and size criteria involved. That thinking brought forth the HD61885.

Its immediate parent was the HD38880, which has been applied to such diverse products as automobiles, vending machines, cash registers, office computers, clock radios, elevators, and even an abacus trainer. But whereas the 38880 requires a companion microcomputer and read-only memory for vocabulary storage, the 61885 packs control circuits and ROM onto one chip, needing only an external low-pass filter and amplifier circuit to drive a speaker.

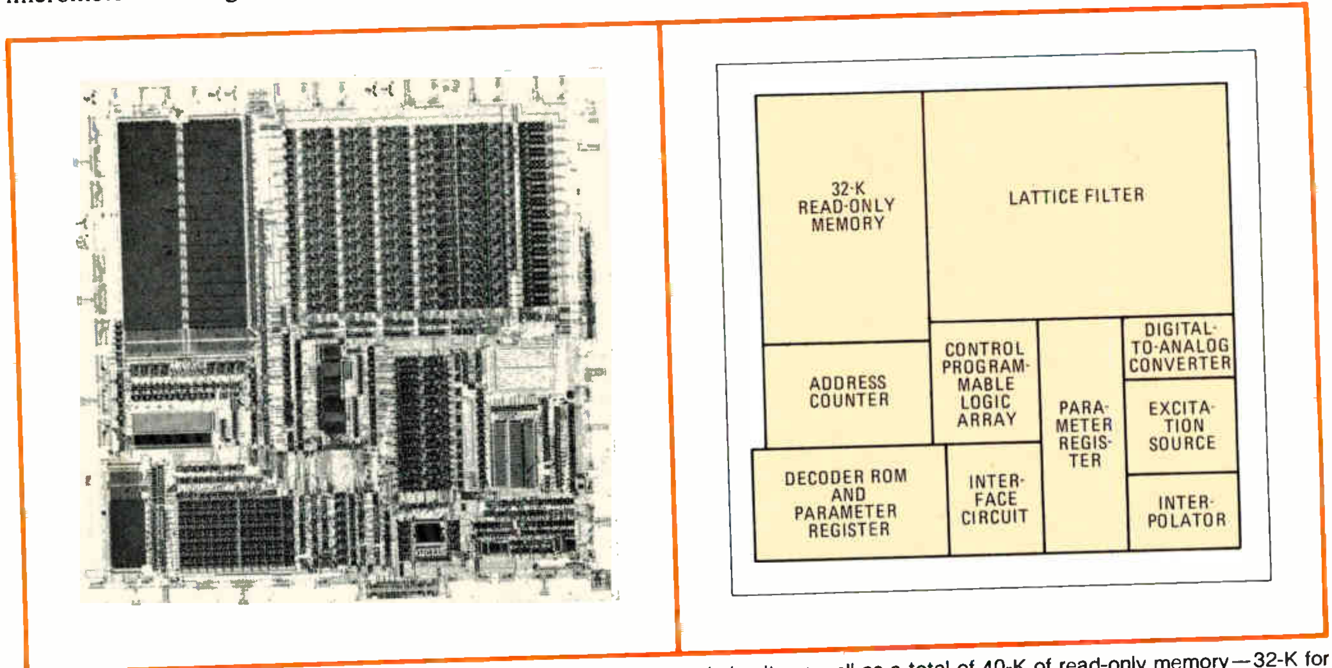
Moreover, it outperforms its predecessor, sounding even better than the p-channel MOS 38880. Thus, through its lower cost and better quality, it should extend the role synthesized speech can play in commercial and industrial applications.

To attain extremely low power yet put a 32-K speech-data ROM on the 61885 required an advanced, 3-micrometer silicon-gate C-MOS process. The technology used in the 61885 is the Hi-C-MOS that Hitachi originally developed for use in memory products; its 3-μm channel length significantly outclasses the 5-μm process used in the 38880 speech chip, which was designed about two years ago.

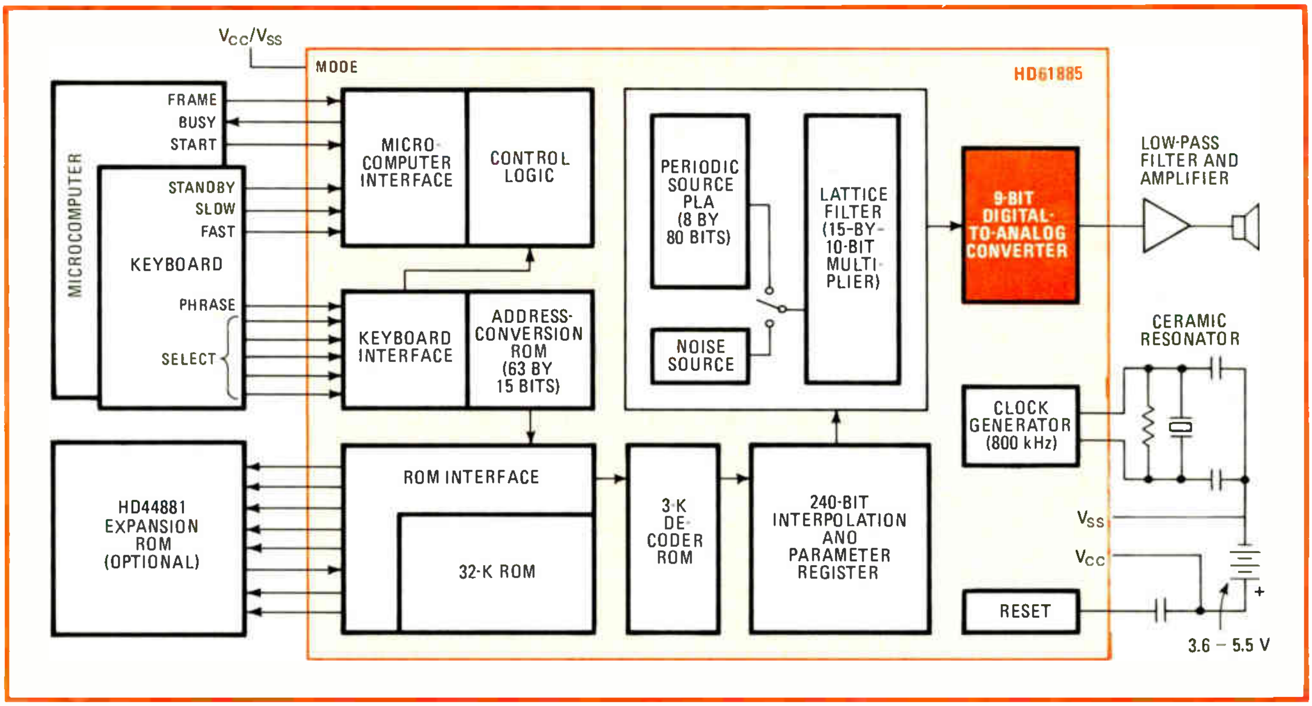
A photograph of the 61885 die is shown in Fig. 1. Packed into the 29.48-square-millimeter (5.40-mm-by-5.46-mm) chip (213 mil by 215 mil, or 45,800 square mils) are some 60,000 transistors that make up the synthesizer's 3,000 gates and 40-K of ROM. Because the 61885 is built with C-MOS, it not only operates from a single voltage supply, but tolerates a wide supply range: 3.6 to 5.5 volts. From 5 V, it dissipates only 30 milliwatts when operating at an 800-kilohertz clock rate and at most 25 microwatts on standby.

Elegant solution

Housed in either a 28-pin plastic dual in-line package or 44-pin plastic flat package, the 61885 is an elegant single-chip solution to speech synthesis. It even has an on-chip reset for depressing certain circuits in order to avoid the popping noise that would otherwise occur when the chip drops down to the standby power mode or returns to the operating mode. Moreover, its built-in digital-to-analog converter is of the current type and



1. Talky. The HD61885 is a single-chip speech system that packs control circuits as well as a total of 40-K of read-only memory—32-K for speech data storage, the rest for decoding and parameter storage—onto its 29.48-mm² (45,800 mil²) die.



2. Self-contained. The 61885 speech chip accepts commands from either a keyboard or microcomputer controller. Thanks to its 9-bit current-output digital-to-analog converter, which can drive a 50-Ω load, only a minimal output stage is required to drive a speaker.

provides an output of 500 millivolts, peak to peak, into a 50-ohm load. From there it is a simple matter to take a few discrete transistors and passive components and construct a low-pass filter and an amplifier that operate from the same 3.6-to-5.5-V supply.

Parcor approach

Since the sensational appearance of speech-synthesis chips in 1978, many efforts have been made to improve the quality of reconstructed speech. That was one goal in the design of the 61885.

Like the earlier 38880, the 61885 uses the partial-autocorrelation, or Parcor, method of modeling the vocal tract—also known as linear predictive coding. In the Parcor approach, the speech signals are regarded as the output of a lattice filter corresponding to a human vocal tract whose inputs comprise either periodic signals for voiced sounds or white noise for unvoiced sounds. Because the parameters that characterize the filter vary slowly with time, they can be encoded at a relatively low, regular rate whose period is referred to as a frame.

As shown in the block diagram of Fig. 2, the 61885, upon receiving the signal from the keyboard (or command from the microcomputer), converts the phrase code to be generated into the first address of the ROM where the speech parameters are stored. The parameters read out are expanded to a word length of 10 bits through the decoder ROM and are then sent to interpolation logic, which smooths their change with time. The interpolated parameters pass to the lattice filter that models the human vocal system to generate the speech. The digital lattice filter consists of a pipelined 15-by-10-bit multiplier, an adder-subtracter, and other logic.

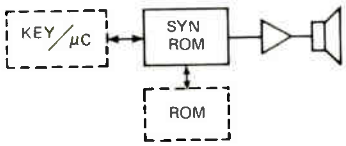
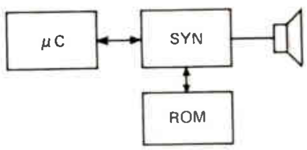
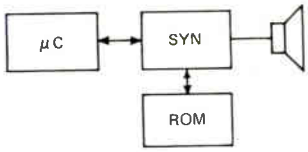
The Parcor approach is similar to that used by Texas Instruments Inc. in its TMS5100 speech chip. The table compares the characteristics of the 61885, the earlier 38880, and TI's 5100.

To improve speech quality in the 61885, several hardware revisions were made on the original 38880 design. First, the bit rate per frame was increased by 1 or 2 bits. Second, the sampling rate was boosted from 8 kHz in the 38880 to 10 kHz in the 61885. Both moves allow a higher resolution of pitch, improving the quality of female voices and sound effects. Finally, the periodic source ROM has been expanded from 8 by 16 bits to 8 by 80 bits. The additional words are there for flexibility. The customer can now, through a mask-programmable ROM option, choose the best periodic-excitation source waveform for his application—the selection is made at the time speech data is programmed.

If not otherwise specified, the 61885 is given with a periodic source waveform, one period of which has the sampled-data representation $f(n) = a^{-n}$, where n indexes the sampling time. This is a departure from the impulse function $f(n) = \sin^2 \omega n$ used in the 38880 and the function used by TI in the 5100, $f(n) = \sin \omega n^2$.

Sensitive spectrum

The reasoning behind this is simple. The first-order Parcor coefficent, k_1, corresponds to speech signals in the range of 0 to 1 kHz. The output spectrum's dependence upon that parameter is extremely sensitive, since on the average, most speech signal energy exists in that frequency range. Consequently even a small error in the parameter causes a large distortion in the spectrum of reconstructed speech signals.

<table>
<tr><th colspan="4">COMPARING SPEECH SYNTHESIS CHIPS</th></tr>
<tr><th></th><th>Hitachi HD61885</th><th>Hitachi HD38880</th><th>Texas Instruments TMS5100</th></tr>
<tr><td>Basic configuration</td><td>
</td><td>
</td><td>
</td></tr>
<tr><td>Process</td><td>C-MOS</td><td>p-MOS</td><td>p-MOS</td></tr>
<tr><td>Coding technique</td><td>Parcor</td><td>Parcor</td><td>Parcor
(linear predictive coding)</td></tr>
<tr><td>Bit rate (kb/s)</td>
<td><table><tr><th></th><th></th><th colspan="2">Frame (ms)</th></tr><tr><th></th><th></th><th>20</th><th>10</th></tr><tr><td rowspan="2">Bits/frame</td><td>50</td><td>2.5</td><td>5.0</td></tr><tr><td>99</td><td>4.95</td><td>9.9</td></tr></table></td>
<td><table><tr><th></th><th></th><th colspan="2">Frame (ms)</th></tr><tr><th></th><th></th><th>20</th><th>10</th></tr><tr><td rowspan="2">Bits/frame</td><td>48</td><td>2.4</td><td>4.8</td></tr><tr><td>96</td><td>4.8</td><td>9.6</td></tr></table></td>
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<tr><td>Bit assignment</td>
<td><table><tr><th>Bits/ frame</th><th>A</th><th>P</th><th>$K_1 - K_{10}$</th></tr><tr><td>50</td><td>8</td><td>7</td><td>7 5 3 3 3 3 3 3 3 3</td></tr><tr><td>99</td><td>8</td><td>7</td><td>10 10 10 8 8 8 7 7 7 7</td></tr></table></td>
<td><table><tr><th>Bits/ frame</th><th>A</th><th>P</th><th>$K_1 - K_{10}$</th></tr><tr><td>48</td><td>6</td><td>6</td><td>7 5 3 3 3 3 3 3 3 3</td></tr><tr><td>96</td><td>7</td><td>7</td><td>10 10 10 8 8 8 7 7 7 7</td></tr></table></td>
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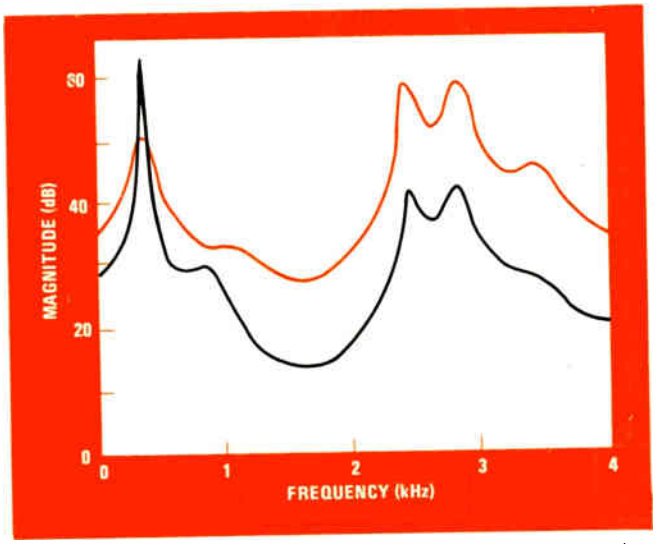
<tr><td>Capacity of read-only memory</td><td>32-K, on-chip expandable
to 128-K per ROM</td><td>external —
128-K per ROM</td><td>external —
128-K per ROM</td></tr>
<tr><td>Speech speed</td><td>0.8, 1, 1.3</td><td>0.6 — 1.7
(10 steps)</td><td>0.5, 1</td></tr>
<tr><td>Periodic source format</td><td>a^{-n}, mask programmable</td><td>$\sin^2 \omega n$</td><td>$\sin \omega n^2$</td></tr>
<tr><td>Sampling rate</td><td>10 kHz</td><td>8 kHz</td><td>10 kHz</td></tr>
</table>



3. Equalized. One reason for improved speech quality in the synthesizer is that the concentration of speech signal energy is better equalized over the spectrum by prefiltering the signals according to the function $f(Z) = 1-0.9Z^{-1}$. This flattens the spectrum (color) as compared with the unfiltered spectrum (black), which depends too heavily on the first-order Parcor coefficient.

To circumvent that strong dependence on k_1, the 61885 uses a flattened spectrum of the original speech signals over the entire frequency range of 0 to 5 kHz. All that's required is to pass the original speech signals, before they are analyzed to provide data for the 61885's ROM, through a filter of the form $f(Z) = 1-(aZ)^{-1}$, where a is a constant greater than or equal to 1.

Significant equalization

Figure 3 shows the effect of the prefiltering—the speech energy distribution, though still concentrated at around 3 kHz and below 1 kHz, is significantly equalized. Of course, to retrieve the original speech sounds, the reproduced speech signals must be passed through the inverse filter $f(Z) = 1/[1-(aZ)^{-1}]$. But because the lattice filter is linear, the effect of passing reproduced speech signals through the inverse filter can be realized by putting the excitation source, which is the input to the lattice filter, through the inverse filter. Putting an impulse function through the inverse filter yields the modified excitation source $f(n) = a^{-n}$.

If the prefiltering and spectral flattening are not desired, the user may encode the periodic source ROM with any desired response. □

LINEARITY, LOW POWER SUIT MONOLITHIC CODEC PLUS FILTER

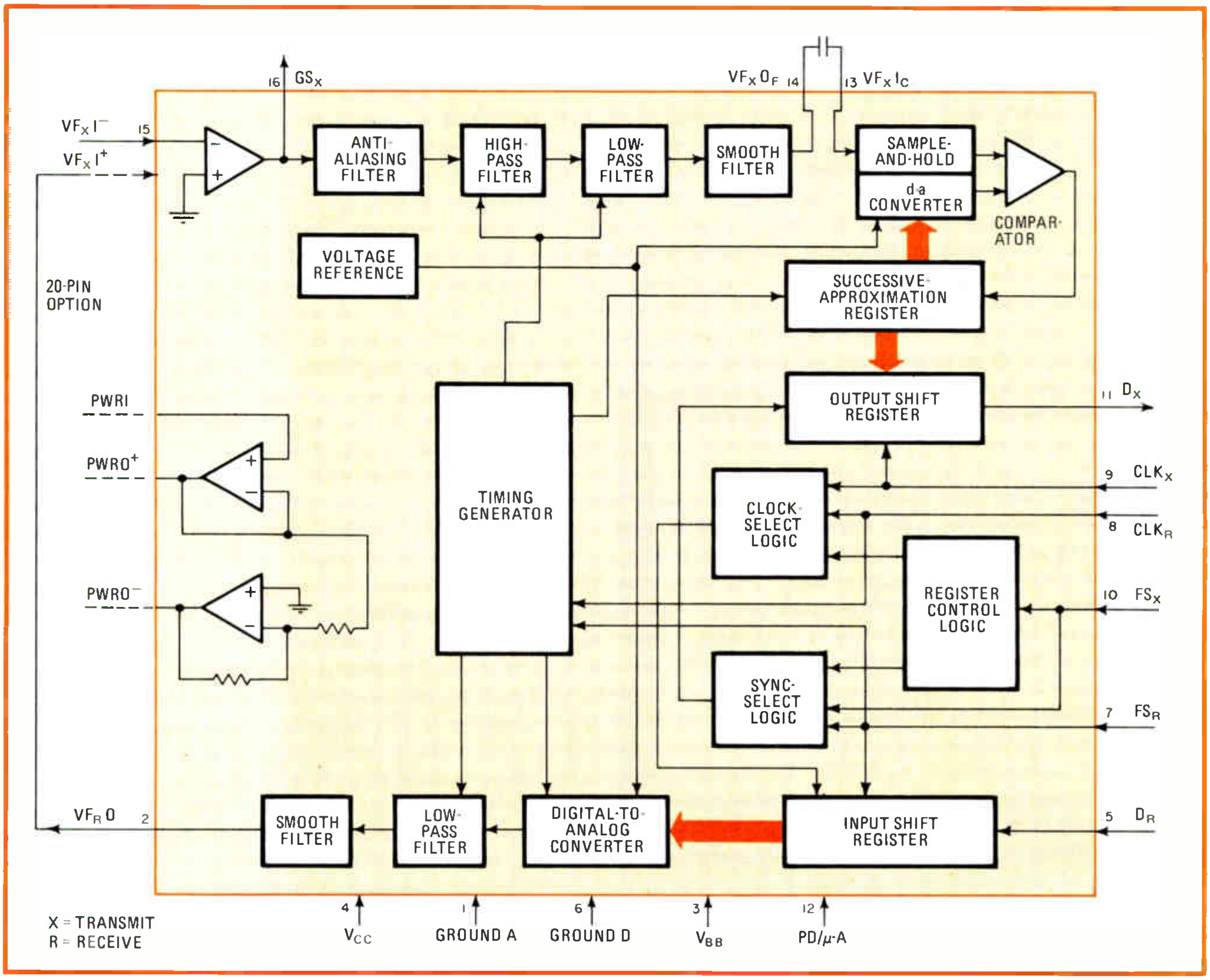
by Jim Garrett, *Mostek Corp., Carrollton, Texas*

☐ Although pulse-code–modulation systems were proposed for telephony use as far back as 1939, they did not prove practical until the advent of the reliable, low-cost semiconductor codec. But the next step—squeezing all of a codec's extremely precise analog as well as digital circuitry onto a single large-scale integrated circuit—is a challenge to the best of design engineers.

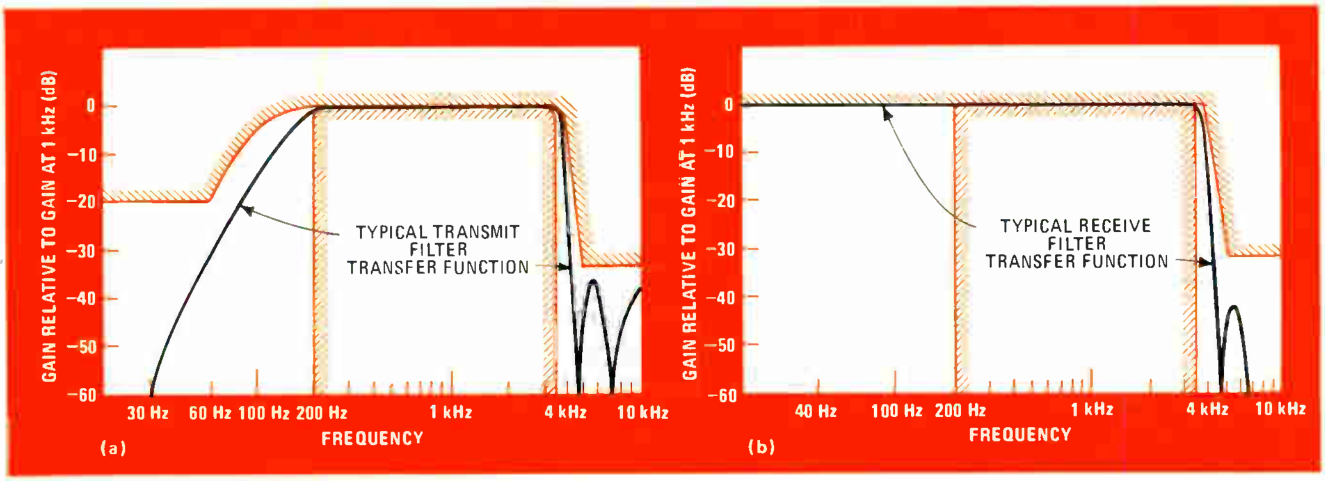
Complementary-MOS technology helps them meet that challenge. Most telecommunications applications need its low power consumption, and its dual polarity enables it to handle linear inputs well.

Metal-gate C-MOS was chosen by Mostek for its first codec, the MK5116 Codec I, which set the stage for the next-generation Codec II currently in development. Combined with a filter on a single IC, the MK5316 will head a complete line of parts intended to service the emerging PCM-based digital telephone set, central office, and private branch exchange markets.

The specifications these parts will have to meet are rigorous. For example, American Telephone & Telegraph Corp.'s digital channel bank requirements call for a codec with gain tracking of better than ±0.5 decibel



1. Two functions. Mostek's C-MOS MK5316 combines a codec and its associated filters. It has on-board voltage references and optional operational amplifiers for gain adjustment, as well as a novel external capacitor for voltage-offset adjustments.



2. Within specifications. The codec's transmit and receive filters perform their respective bandpass (a) and lowpass (b) functions with better specifications than required. Both filters are switched-capacitor devices and in corporate the necessary (sin x)/x smoothing functions.

for a 33-dB variation in the device's input signal range, as well as signal-to-distortion ratios of at least 33 dB at input levels from 0 to −30 dBmo. And topping off these demands is a need for analog-to-digital and digital-to-analog data conversion in less than 125 microseconds.

Capacitors to the rescue

Previous industry designs of a-d and d-a converters—the heart of a codec—used R-2R resistor networks in a successive-approximation register. This approach was ruled out for the design of the 5116 and the 5316 codecs because of the tolerance requirements of the resistive elements and the inherent power-dissipation problems.

An alternative is to base the successive-approximation register on the close-tolerance capacitors that may be constructed in C-MOS using a linear-ratio capacitor design. This approach is both accurate enough and eliminates the power drain associated with R-2R networks. Furthermore, C-MOS processing, when applied to linear-ratio capacitors in the 5116, produced a codec chip measuring about 40,000 square mils in area yet with satisfactory yields.

Consequently, the 5116 codec series has been widely second-sourced and has seen an installed base of over a million lines in little over a year. Moreover, the high production levels have justified the installation of extensive automatic test capabilities that can be used for the 5316, which is expected to have similar high yields.

Figure 1 is the block diagram of the ±5-volt silicon-gate C-MOS 5316. The chip, whose digital inputs and outputs are compatible with both C-MOS and TTL requirements, contains switched-capacitor transmit and receive filters (similar to Mostek's MK5912 single-chip filter) as well as the encoding and decoding portions of a codec. It also has internal voltage references.

The external capacitor (shown at the top of the block diagram) is a novel way of satisfying, under all operating conditions, the exacting offset specifications posed by AT&T and the International Consultative Committee for Telegraphy and Telephony. The low-tolerance, 1-microfarad ±20% device makes it possible to avoid voltage offsets from the filter to the codec—and certainly is a less risky way of doing so than designing autozeroing circuitry to fit in here. In addition, it facilitates testing the product, and dc signaling can be readily accomplished because there is separate access to the transmit codec section.

Several other design features are evident in Fig. 1. The separation of the encoder's successive-approximation register from the decoder's d-a conversion circuitry will minimize crosstalk. A −70-dB figure is expected—the same as the 5116's maximum value.

Figures 2a and 2b show the transfer characteristics of the transmit and receive filters. Amplifier stages adjust their gain to whatever the system designer requires.

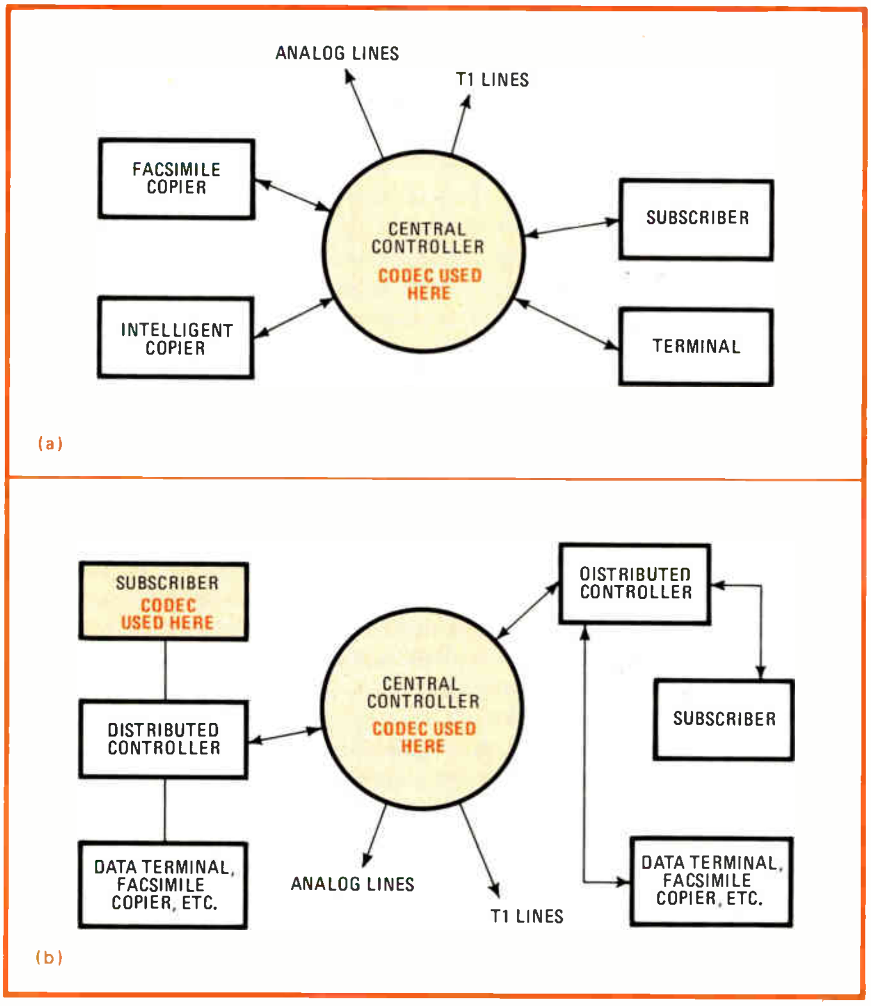
Two distinct pins on the codec-filter separate analog and digital grounds. This feature helps the system designer meet the low background noise requirement found in many digital system specifications.

Timing matters

The clocking requirements of the 5316 are such that either synchronous or asynchronous operation can be had from a low data rate of 64 kilohertz up to 4 megahertz. The 4-MHz upper limit grants great application flexibility. As is the case with the 5116, the 5316 timing system latches data on the positive-going edge of the transmit and receive clock pulses.

The serial output data port of the codec/filter is in a three-state mode until the transmit synchronization pulse is taken to a logic 1 level. The 8-bit serial data is then clocked out (with each clock pulse) on the transmit side. Conversely, in the case of the receive side, the valid digital input is clocked into the codec. These pulses may be either synchronous or asynchronous. Again, this allows the maximum design freedom.

Other electrical specification targets include a greatly enhanced power-supply rejection ratio for both positive and negative supplies, as well as less than 17 dBrnc0 for combined transmit and filter-idle channel noise and 14 dBrnc0 for combined receive-idle noise. The double-level–polysilicon C-MOS approach will provide the neces-



3. Adaptable. The 5316 codec-filter is designed for use either in a centrally controlled voice- and data-handling system (a) or in a distributed system (b), with a separate codec being employed in each individual voice- or data-handling device.

sary process control and density for this chip.

Mostek plans to have a prototype of its 5316 Codec II available by year end. The first part to emerge will be a 16-pin package and include the basic codec and its filters. For designers needing amplification from operational amplifiers to drive nonelectronic subscriber-loop interface circuits, a 20-pin codec will be provided. Both parts will permit gain setting of the receive and transmit filters using external resistors.

The architecture of the 5316 Codec II is similar to the combination of the 5116 Codec I and the 5912 filter, the latter of which is based on the pinout of Intel's 2912 filter. Thus, a product upgrade for a cost-reduction program will be nearly transparent to the design engineer currently using the 5116/5912 configuration.

The designer need not depend on one source for the features of the 5316. Mostek has agreed with Motorola on a second-source arrangement for each other's codec products. Thus, the Codec II will be second-sourced when it becomes available for production.

The 5316 codec-filter combination is structured to provide the system designer with an easy-to-apply building block for digital systems. The building-block approach maximizes the number of system architectures with which the device can be interfaced. This is important because of the current trend to merge both digital and analog information on the same chip for total system integration. In fact, the increased use of distributed processing in such applications as office-of-the-future equipment is aided by codec products that transcend unusual or cumbersome device architecture and timing requirements.

A good example of the new architectures for which the 5316 is designed is a common control system (Fig. 3a). In this approach, the subscriber loop may be analog until it reaches the central controller. There, a codec can digitize the analog voice for further switching and control. Because many codecs may be used in one controller in this type of system, low per-codec power dissipation becomes an important consideration.

One disadvantage of this system approach is the requirement for multiple runs of wire to each work station for the proper control of each subsystem. And, of course, the reliability of a central controller is a major concern. These disadvantages can be overcome by the use of distributed processing (Fig. 3b).

Codecs can be used even when distribution of the system control processing is placed at the system components level. In this case, the codec is simply inserted in the subscriber set itself. □

CROSS-POINT ARRAY IC HANDLES 256 VOICE AND DATA CHANNELS

by Lloyd Reaume, *Mitel Corp., Kanata, Ont., Canada*

☐ Squeezing the telecommunications switching function to a new density, the 271-by-275-mil Iso-C-MOS DX digital switching chip will replace three 8-by-15-inch printed-circuit boards stuffed with 100 TTL components. The DX functions as a 256-by-256-channel switching matrix, but with a size and power consumption far less than in other types of switching matrixes.

The new MT8980 integrated circuit (Fig. 1) is the basic building block of the soon-to-be-announced SX-2000 150-to-10,000-line digital switch. The DX, or multiple DXs, will route all voice and data signals and interface them with the switch's multiple microprocessors.

In the SX-2000, the DX handles a 2.048-megahertz bit stream, but it can receive and send at any speed up to 4 MHz. Its input/output architecture splits the 256 channels (subscriber lines) among eight time-division-multiplexed lines (buses). Each line's 32 time slots contains 8 bits, giving a per-channel data rate of 64 kilobits a second, as required for the pulse-code–modulated signals that are standard in digital telecommunications.

The end result of all this switching capability is routing signals in both time and space. Time routing is based on the ability to transpose any input time slot to any output time slot, or vice versa. Similarly, space routing depends on the ability to switch data from any input bus to any output bus, or vice versa.

Thus, the DX can be applied to most functions requiring time-division switching, space-division switching, or both. In fact, it is not limited to switching functions: its routing capabilities may be the basis for memory and memory-management systems for microprocesors.

The DX design gives in one chip a maximum size of 256 omnidirectional channels or 128 two-way voice and data communications, while still retaining nonblocking operation. In itself a significant advance over today's digital switches, this figure may be improved. A configuration of multiple DX chips (Fig. 2) can extend bus capability up to 128 by 128 lines, each carrying a complement of 32 channels.

How it's done

The chip's switching function requires 36,500 transistors, and it took the density and performance that Iso-C-MOS adds to the low power and noise immunity of conventional complementary-MOS processes to handle the job. The Iso-C-MOS process reduces the long propagation delays related to the inherent array capacitance of metal-gate C-MOS. Even more, its intrinsic high speed and low-voltage requirement considerably improve the chip's dynamic power requirement.

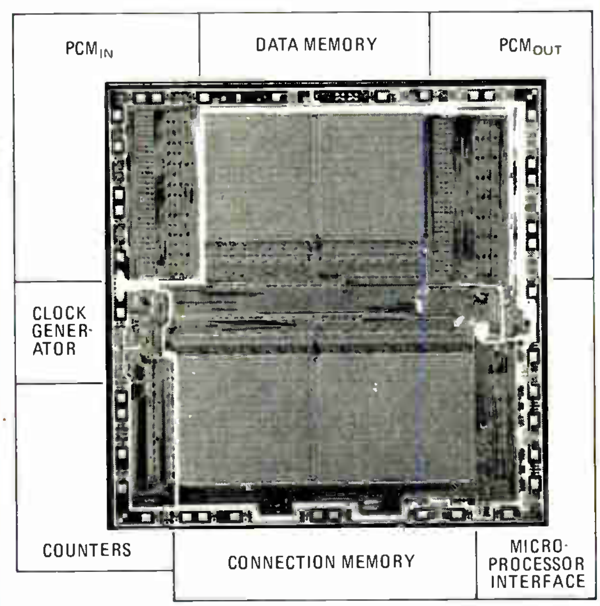
The performance advantage over metal-gate C-MOS is based on a self-aligning, recessed p-well, oxide-isolation technique applied to standard silicon-gate technology. The result is die sizes comparable to equivalent Shottky-TTL or n-channel MOS logic.

Performance improves because die area is available to construct I/O buffers with high drive capability. Iso-C-MOS has given rise to an IC family that boasts gate-propagation delays below 5 nanoseconds—rivaling those of standard low-power Schottky parts and offering significant improvement over the usual metal-gate C-MOS delays of 40 to 60 ns.

Memory on chip

In the DX configuration (Fig. 3), the memories are designed with a standard static C-MOS, six-transistor memory cell. The memories constitute 40% of the chip area. The IC's typical power dissipation is 150 milliwatts, which is consumed mostly by the memories. Although the DX can operate at up to 4 MHz, the memories were designed for 5 MHz to allow some speed margin.

Since it replaces 100 medium- and small-scale ICs, the chip represents significant savings in system cost, power



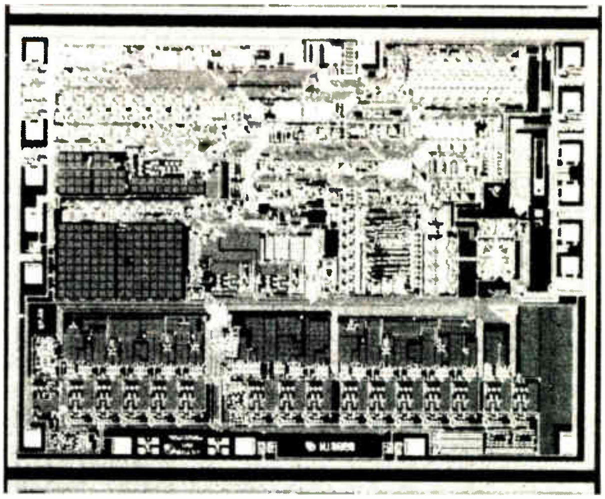
1. Unique. Mitel's MT8980 cross-point array can switch any of 256 input channels to any of 256 output channels in both space and time. The C-MOS chip has three-state outputs, is constructed in 5-micrometer geometry, and is 271 mils by 275 mils in size.

A versatile codec-filter

The MT8960 codec-filter integrated circuit has been designed so that it can be programmed during the final metalization process to accommodate either the North American μ-law or European A-law companding techniques. It can be directed to power-down if there is no voice traffic to handle, so that its low 35-milliwatt operating power can be reduced to only 5 mW.

The 8960 can be instructed to loop signals back at both the digital and analog levels for codec integrity checks. Thus, the operating status can be monitored from a remote location under microprocessor control.

The codec-filter has other unique features. For example, it has six drive points or digital outputs for controlling external circuitry. Furthermore, it has high-impedance outputs when it is inactive and operates from ±5-volt supplies. All these capabilities, plus variable gain for the transmitting and receiving channels, have been fitted to a 175-by-132-mil chip that can be held by a 350-square-mil 18-pin dual in-line package.



dissipation, and size, in addition to the benefit of Iso-C-MOS reliability. The design is under review for eventual fabrication in a 2-to-3-micrometer technology; now the process uses 4-to-5-μm geometry.

Other chips

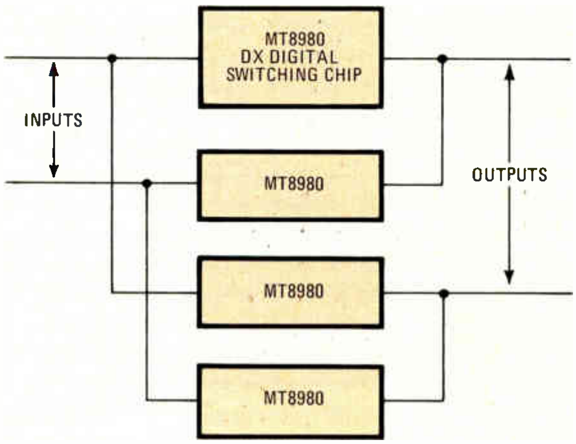
The SX-2000 digital switch, which depends on the DX, can function in a voice mode, data mode, or both. For the DX to operate in a voice mode, it must be complemented by the MT8960 codec-filter chip. This part converts an analog voice signal to a 2.048-MHz, 8-bit burst-format digital signal compatible with a 32-channel PCM multiplexed bus format (see "A versatile codec filter," above).

The signal from the codec-filter is received at the PCM input of the integrated circuit. It is then fed through a formatter, which converts the pulses to a form that can be stored in or read from the data memory.

This memory stores an entire frame of 256 words, each containing 8 bits. Each word of PCM data has a reserved location in the data memory and the addressing scheme is fixed during the write cycle. Each address consists of an 8-bit word that is stored in the connection memory as part of an 11-bit word.

The PCM data is directed to the DX's output circuitry by means of the address stored in the connection memory. The output circuitry then rearranges the data into its original format. The PCM output buffers are TTL-compatible and are designed to drive as many as 16 DX chips that may be wire-ORed on a common bus.

On leaving the DX circuitry, the PCM word goes to another MT8960 codec-filter to be transformed back into the original analog signal. While all these signal manipulations are taking place, the extra 3 bits of the connection memory's 11-bit word perform control functions, such as allowing the chip to switch voice and data simultaneously and allowing the chip to monitor its own performance on the fly.



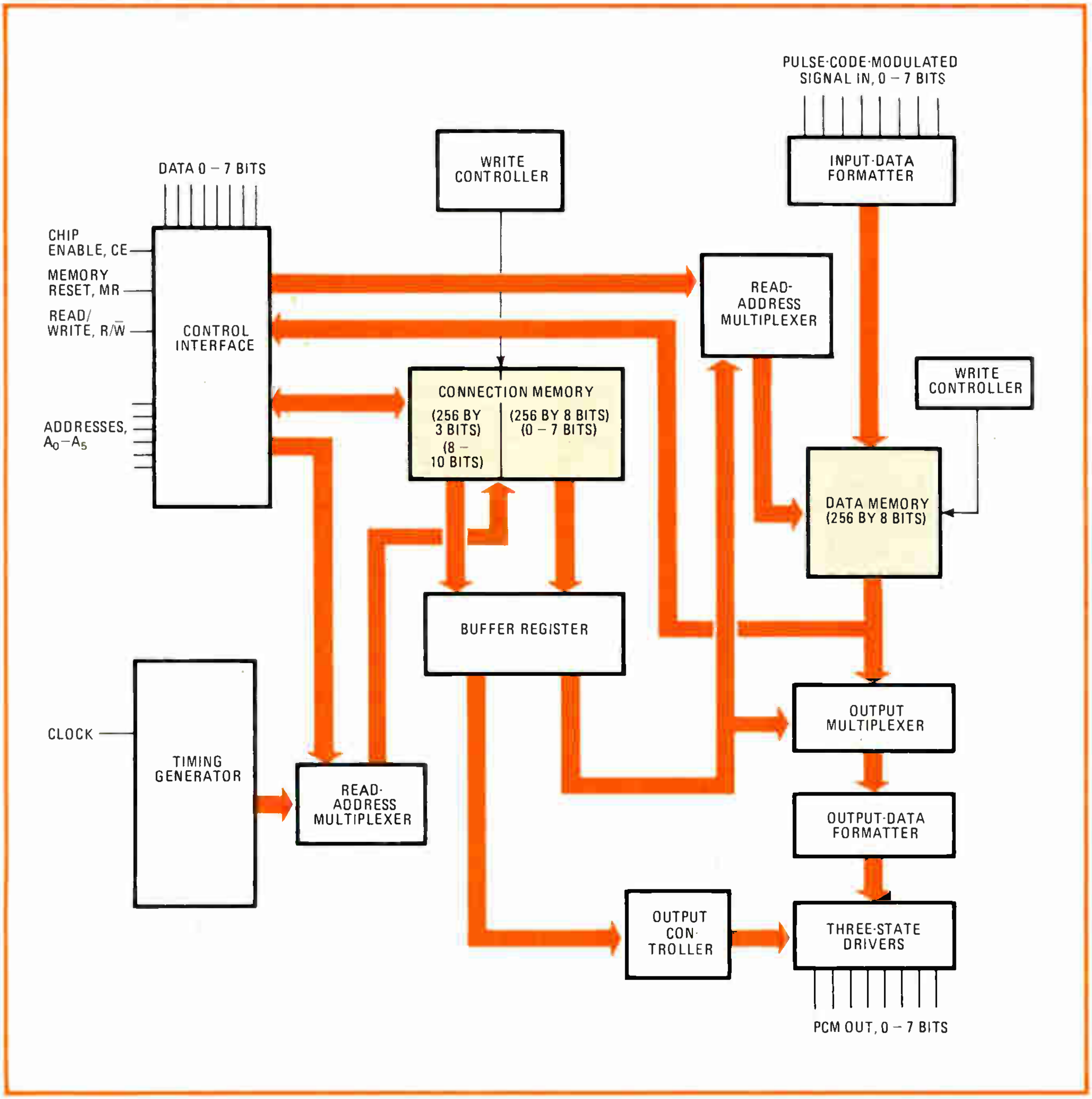
2. More ports. The basic DX module may be extended using this interconnection scheme. The 16-line system is fully nonblocking, and each eight-port serial output contains 256 data words. Extension to a 128-line architecture is the maximum possible.

Another helper

The DX requires another helpmate besides a specially designed codec-filter. It interfaces with the North American-standard T1 carrier signal via the Mitel DS1 interface chip. This IC reformats the data from a 24-channel 1.54-megabit/s data stream to the DX's 32-channel 2.048 megabit/s data stream.

This Iso-C-MOS part operates from a 15-volt power supply and is fully compatible with all chips on its inputs and outputs. In the SX-2000 switch, the DS1 chip is mounted on a T1 interface card, which also incorporates DX chips for multiplexing and demultiplexing the 32-channel data stream into the 24-channel T1 format.

In the data mode, the DX chip allows an efficient



3. Routing data. The DX's data memory is connected to an external microprocessor in a read-only mode. In contrast, the connection memory is accessible by the processor in both read and write modes. These chores may be accomplished with the Motorola 68000.

interface between 2.048-MHz data streams of any form and various types of microprocessors. For example, the microprocessor controlling the DX chip has access in a read-only mode to the data memory and has a read-and-write access to the connection memory.

The processor can route data arriving on the incoming serial buses to its own memory via the DX's data memory. It can even go a step further and route data from its own memory to the outgoing serial buses via the DX's connection memory.

A nonblocking high-capacity switch can be constructed from a Motorola 68000 microprocessor and a few DX chips. Such switches are used to transmit messages between microprocessors in the SX-2000.

There are still other applications for the DX. For example, its inherent qualities for both switching and memory storage and management are ideal for application in concentrators for message centers, digital switches for tandem switching units, and as the critical component in information-encryption equipment. Other applications for the chip, which will be sold as a stand-alone part, are in alarm and control systems where data from remote scanners is intermittently recorded on data loggers. □

CHARGE BALANCING IS KEY TO 10-BIT A-D CONVERTER CHIP

by S. W. Chin, L. L. Lau, T. P. Redfern, and T. M. Frederiksen, *National Semiconductor Corp., Santa Clara, Calif.*

☐ The proliferation of microprocessors has fostered a high-volume market for low-cost analog-to-digital converters and thus stimulated the development of monolithic converter products. Complementary-MOS has become a favored technology for achieving this goal, as its two device polarities lend a flexibility in designing analog functions on chip that is lacking with n-MOS, plus a simplicity in manufacture that is absent from bipolar processes. In addition, C-MOS processing yields, at no added cost, parasitic bipolar npn devices that can be used as emitter-followers in analog circuits (their collectors are the n-type epitaxial layer and hence are always tied to the positive voltage supply).

Tailoring a-d converter designs to exploit MOS technology also entails taking a system approach that capitalizes on the inexpensive and plentiful electronic switches that are available on an MOS chip. Sampled-data designs are just such an approach, in which switched capacitors periodically sample the input voltages. A C-MOS transistor used as a transmission gate forms an ideal analog switch. It can be turned on and off rapidly and can handle a wide dynamic range of analog input voltages, from slightly below ground to slightly above the power-supply voltage.

Charge-summing input

The key advance in National's C-MOS a-d converters is a novel multiple-input voltage comparator that simplifies the design of successive-approximation converters. This circuit accepts many differential voltage inputs simultaneously and weights each one by selecting the size of the associated input capacitor. Input voltages are converted to input charges with capacitors, and the resulting charges are then algebraically added at a charge-summing node.

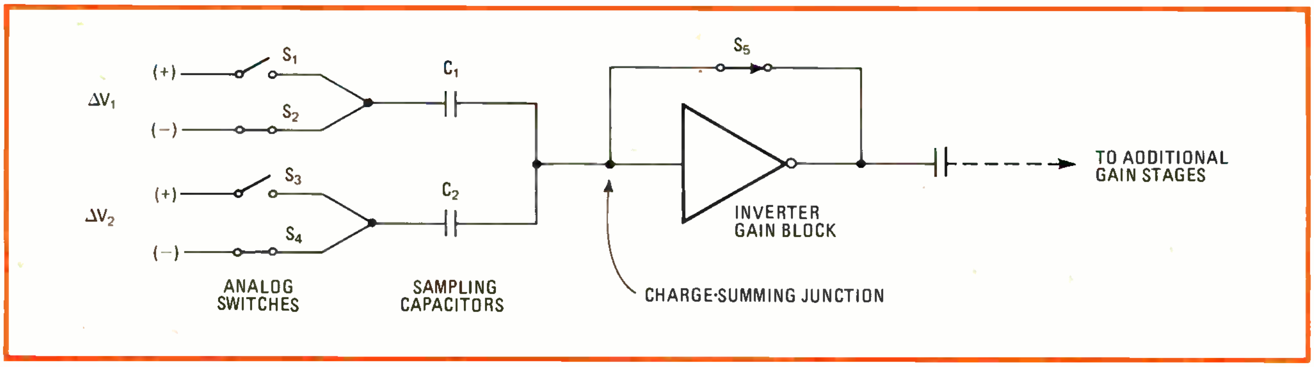
The traditional current-summing operational amplifier is similar in principle, but it accepts only single-ended voltage inputs and requires a feedback current loop. The charge-summing comparator takes advantage of analog switches to perform a zeroing cycle periodically, but operates open loop during a measurement.

The differential-input, sampled-data comparator is shown in Fig. 1. Switches S_1 through S_5 are set for a zeroing cycle. The input-output short created by closing S_5 around the inverting gain block causes this stage to bias at a fixed dc voltage—a standard C-MOS inverter will bias at approximately half of the power-supply voltage. At the same time, closing the input switches S_2 and S_4 precharges the input capacitors to the low sides of the differential input voltages. The input capacitors serve as storage elements for both the low input voltages and the biasing voltage of the gain stage.

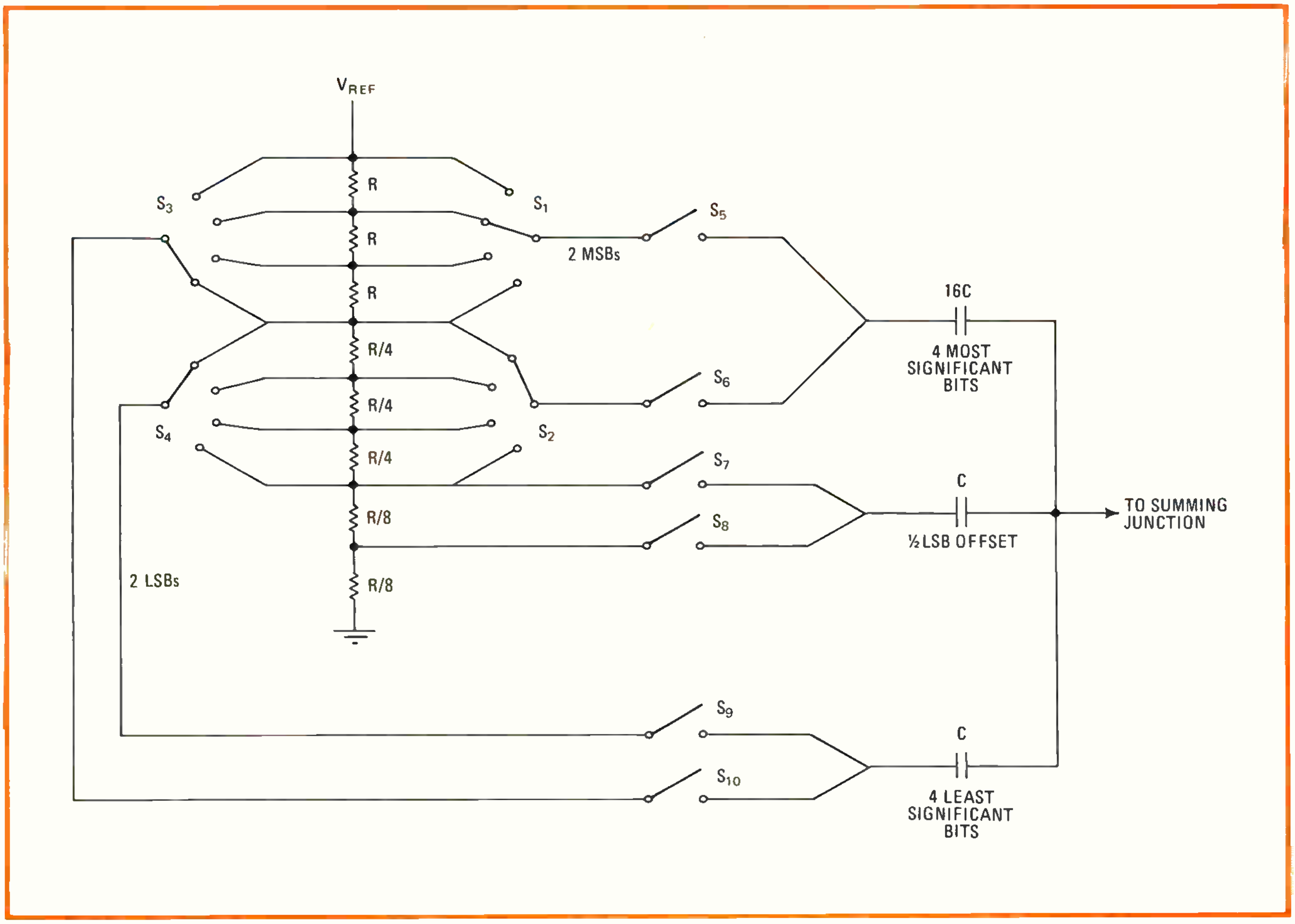
Once these zeroing switches are opened, the gain stage is active and will respond to any deviations in the input voltage. To sample an input voltage, switches S_1 and S_3 are both closed. For example, a positive ΔV_1 produces a charge Q_1, proportional to the value of C_1. If ΔV_2 is negative, a charge Q_2 proportional to C_2 will be removed from the charge-summing node. If the charges Q_1 and Q_2 are balanced, there is no net change in the input voltage to the inverting gain block.

The switches are dynamically cycled by the system clock to zero the input stage prior to each measurement interval. This operating mode has two principal advantages: it readily handles differential inputs, and it permits tighter control of drift and offset errors. Several of the inverter stages are capacitor-coupled to provide an adequate overall gain for the comparator.

In a successive-approximation converter, the analog input voltage is compared with voltages generated by an



1. Charge balance. A C-MOS charge-summing comparator uses input capacitors to convert differential voltages to charges. The measurement cycle includes zeroing (shown), input sampling, and holding. Using cascaded inverters can boost the comparator's gain.



2. D-a ladder. An 8-bit d-a converter exploits the comparator's differential input to reduce the number of resistors needed to generate 256 voltages. Two switches provide the 4 most significant bits, and the same voltages, scaled by a factor of 16 yield the lower 4 bits.

internal d-a converter. Use of a differential-input switched-capacitor comparator permits tremendous simplification of the resistor ladder network for an 8-bit d-a converter. The network used in the ADC0804 8-bit a-d converter (Fig. 2) derives the required 256 analog voltages from only eight resistors, making use of switches and weighting capacitors to send the correct charge to the comparator's summing junction.

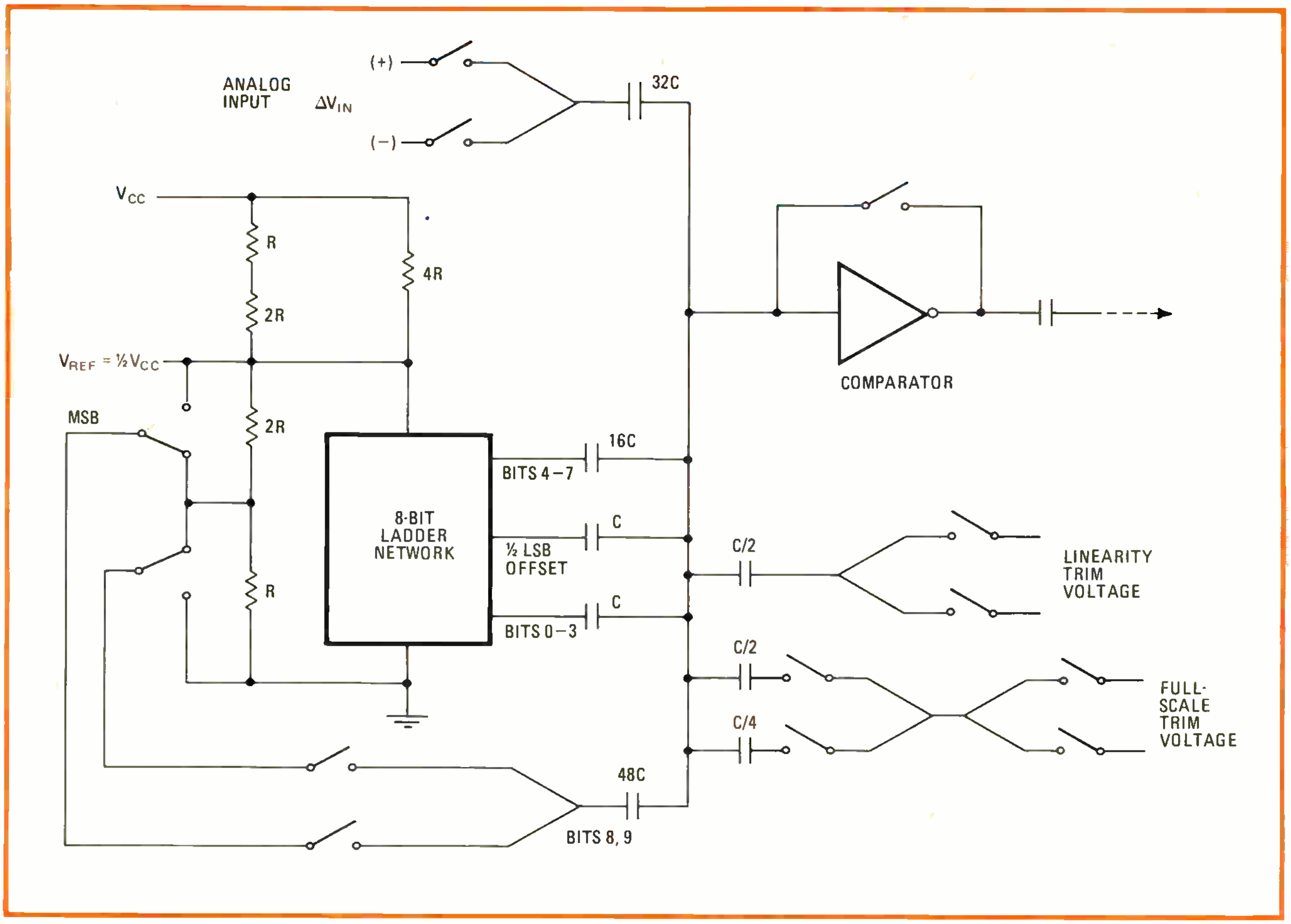
The 4 most significant bits of the 8-bit d-a converter are supplied by switches S_1 and S_2. As shown, the positions of S_1 and S_2 correspond to the digital code 1000_2 for the first 4 bits of the 8-bit word: S_1 is selecting ¾ V_{REF} and S_2 is selecting ¼ V_{REF}, so that the differential voltage that is sampled by S_5 and S_6 at the start of a successive-approximation search is ½ V_{REF}. The top three resistors each have ¼ V_{REF} across them while the next three resistors each drop 1/16 V_{REF}. The differential-input of the comparator therefore permits the increased resolution of the voltages selected by S_2 to be "fitted into" each section of the upper or S_1-selected voltages. In this way, 4 bits of resolution are realized with two four-position switches instead of one 16-tap ladder.

The same trick is used again with the left-side decoding switches S_3 and S_4. The same voltages supply charges reduced by a factor of 16 by making the input capacitor for this side smaller by a factor of 16. This supplies the 4 least significant bits with no additional resistors. The additional capacitor and the lowermost two resistors of the ladder supply a ½ LSB offset voltage, which in a-d converters, centers the intrinsic ±½ LSB quantization uncertainty of the converter about the integer LSB values of analog input voltage.

Two more bits

This basic 8-bit design has been extended to produce a 10-bit converter that is scheduled for release early next year. The LSBs of the 10-bit data word can be derived from an 8-bit design by scaling the associated input capacitors. The 2 additional MSBs for the 10-bit unit are added by means of another trick.

Since the 2 MSBs of the 10-bit d-a converter control four voltages, if these are chosen as ground, ⅓ V_{REF}, ⅔ V_{REF}, and V_{REF}, the two intermediate voltages can be picked up from a resistor divider with only one tap. The odd voltage values (⅓ and ⅔ V_{REF}) are adjusted by scaling the size of the input capacitor used for this section by a factor of ¾ so that it will provide the ¼ V_{REF} increments necessary for the 2 MSBs. Then the basic 8-bit circuit can be used in each of these four segments, with its contributed charge adding to one or another of



3. Expansion. Two more bits can be added to the a-d converter by scaling the input capacitances and interleaving the voltages from the 8-bit ladder in each of four intervals between 0 and V_{ref}. A correcting charge is supplied to adjust linearity and full-scale output of the a-d unit.

these ¼ V_{REF} values. Figure 3 illustrates the input section for the 10-bit design; the 8-bit ladder network consists of the resistors and switches that were shown in Fig. 2.

The two-resistor ladder produces no linearity errors in the segments with both of the 2 MSBs equal to 0 or 1. The first segment is error-free because the output voltage from the upper 2 MSBs is 0 volt. Similarly, assuming that the input capacitors are formed in the correct ratios, there will be no linearity errors in the last segment, because the full reference voltage is sampled. Any mismatch between the input capacitors for the analog differential-voltage input and the d-a converter's output voltage will cause a full-scale error, but not a linearity error.

Fringe benefits

Besides giving two end segments free of linearity errors, this scheme has an additional benefit in that any error in the exact value of the tap voltage on a two-resistor divider has inherently the same magnitude for the ⅓ V_{REF} and ⅔ V_{REF} voltages and is simply of opposite sign. A linearity trim of the upper two bits, therefore, need supply only a single quantity of correcting charge, adding it to the comparator's summing mode in one case, and removing it in the other.

Gain errors are also trimmed by introducing an additional correcting charge into the summing node of the comparator. This is done in steps: no correction is used on the first one fourth of the analog input voltage range, the next range receives one third of the total correcting charge, then two thirds, and finally the full charge is introduced in the last section. This sequence is achieved by dynamically altering the input capacitance associated with the trim voltage from zero to C/4 to C/2 and finally to 3C/4.

Understanding the scaling shown for the input capacitors begins by noting that it is the input charge that is balanced. A full-scale differential analog input voltage of 5 V produces an input charge of 5×32C, or 160C coulombs. When the d-a converter's input is 200_{16}, its output is $V_{cc}/3$. This is converted into an input charge by the 48C capacitor, giving ⁵⁄₃×48C, or 80C coulombs. Therefore, 200_{16} corresponds to one half of full scale, as it should. The code 080_{16} produces an output of ¼ V_{CC}, or 1.25 V, which gives an input charge of 1.25×16C coulombs, or 20C—one eighth of full scale.

The multiple-input, sampled-data voltage comparator makes the most out of C-MOS in the design of monolithic a-d converters. This innovative concept has further reduced die size, and appears to be an optimum solution for implementing low-cost, high-performance parts. □

IGNITION CONTROLLER BRAVES HARSH AUTO ENVIRONMENT

by Jim Gillberg and Nick Kucharewski, *RCA Solid State Division, Somerville, N. J.*

☐ Almost everything about complementary-MOS technology makes it a natural for automotive engine-control systems under the hood, where a harsh operating environment precludes n-channel MOS. Compared to the rival technology, C-MOS has a higher operating-temperature limit, better noise immunity, and greater tolerance of power-supply fluctuations. It also is easier to work with in computer-aided design.

Therefore, RCA chose C-MOS for its forthcoming low-cost system, dubbed Rombic for read-only-memory–based ignition controller. This system is a sharp departure from the usual engine-control setup: it uses a dedicated C-MOS controller; it eliminates the microprocessor; and it concentrates on spark control rather than on a host of engine-control parameters.

Typically n-MOS microprocessor-based systems have been mounted in the passenger compartment where the operating environment is comparatively benign. An under-the-hood mounting is closer to the engine sensors feeding data to the system, and this location avoids the lengthy wiring and extra connectors that can downgrade performance and raise costs.

Better mileage

The two-chip system, consisting of a controller (Fig. 1) and a ROM, is aimed at improving gas mileage in four-cylinder cars, rapidly growing in favor among U. S. car makers and long the standard in Europe. Because emissions control is simpler than in six- and eight-cylinder cars, the four-cylinder models can meet government pollution standards with the simpler Rombic system—especially if emissions requirements in the U. S. are to be relaxed.

This simpler solution can also save the car maker considerable money with its quantity price for the two chips of $7, compared with the $20-to-$40 chip-set cost for microprocessor-based systems currently planned for 1984. What's more, Rombic may be expanded in function if other chips are added to the system.

Chip implementation is in RCA's C²L (closed C-MOS logic) technology, a silicon-gate process with 6-micrometer design rules that has been in production since 1975. In C²L, devices appear on the chip as closed-geometry gates, rather than the linear ones seen in conventional C-MOS technology.

Since it is a mature technology, it offers a cost-effective and reliable process, paramount considerations for the auto manufacturer. It also allows chip designers to draw on a library of existing CAD cells. C-MOS and CAD go together well, because the technology's two-transistor setup is easier to design with than the transistor-plus-pullup format of n-MOS. For example, there is no need to worry about load-device sizing to optimize speed and power dissipation.

C²L offers the density levels needed for low cost: the controller chip measures 250 by 215 mils. Compared to hand layout, a CAD-produced chip takes up more real estate, but spreading the devices over a larger area does of course give a higher production-line yield. Future Rombic offerings, which could include more on-chip functions, could be realized in an existing 5-μm oxide-isolated C-MOS process.

Running on Rombic

Rombic is a system that sets the spark advance as a function of engine speed and manifold pressure. The two-chip set uses a dedicated hardwired program controller rather than a microprocessor, yet it is sufficiently flexible to handle six- and eight-cylinder cars as well as the four-cylinder models at which it is primarily aimed. Representing a significant cost reduction for the auto maker, it also promises to offer the driver a net fuel savings, compared with mechanical systems.

The two ICs are the TA11130 control chip with an on-board 5-bit analog-to-digital converter, and a standard C-MOS ROM, typically 1-K by 8 bits in size. The system (Fig. 2) is designed to take engine speed in

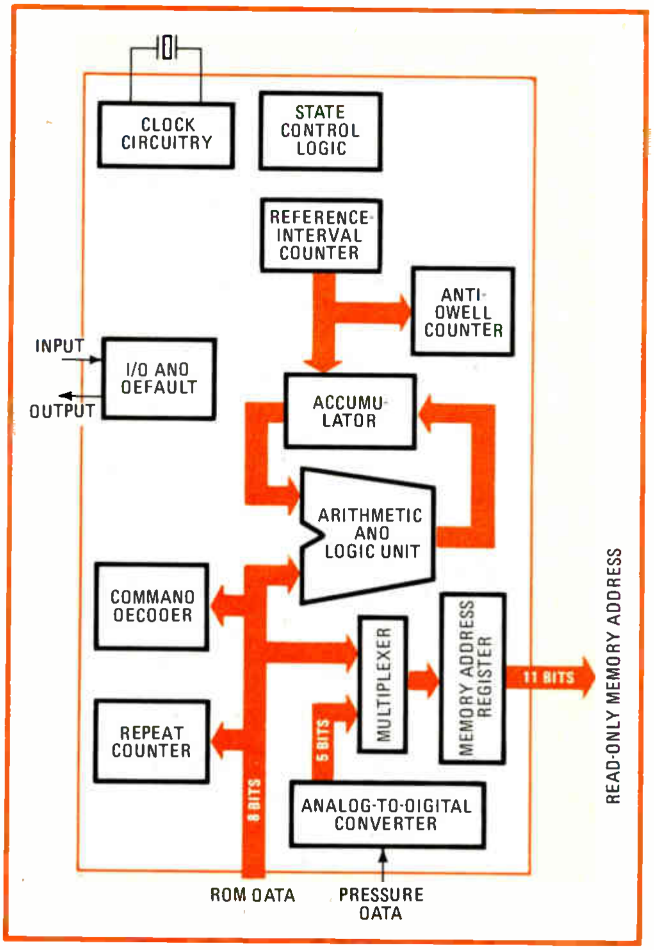
C-MOS controller. Pulling away from the more complex microprocessors typically used for automotive-engine controls, this controller chip is part of RCA's two-chip Rombic spark-advance controller. It measures 250 by 215 mils and uses 6-μm line widths.

revolutions per minute, usually digitally encoded timing information from the flywheel or distributor, as one input and a variable analog signal, such as manifold pressure received from an engine vacuum sensor, as another input. The output from Rombic in turn controls the ignition-coil driver.

In operation, the reference-interval counter on the TA11130 is enabled to count pulses during a specific reference interval of the digital rpm input. The pulses counted up during the reference interval are counted down at a faster rate during the next reference interval.

Because the first interval has the same period as the second, the countdown will reach zero before the end of the interval. The zero point is the time of the spark advance, relayed to the ignition by the 11130. (In practice, there is simultaneous counting up during the reference interval for one engine cycle and counting down for ignition timing of the previous cycle.)

In addition, the countdown clock rate is variable so the amount of advance can be modified. The variable countdown is accomplished with a subtraction algorithm beginning at the start of the countup interval. The algorithm subtracts the contents of the external ROM from



1. Rombic block. Rombic counts clocks pulses between rpm pulses and stores the count in the reference interval counter. ROM data is subtracted in the arithmetic and logic unit to adjust the succeeding countdown period and in turn to adjust the spark advance.

an accumulator containing the reference counter's value. The ROM data is chosen so that, when it is subtracted from the value in the accumulator at any given rpm, the correct spark timing will occur.

The speed and accuracy of this calculation is a function of the system clock. When used with a 4-megahertz crystal, Rombic can perform a 16-bit subtraction every 16 microseconds. Thus, the timing accuracy for spark firing is equal to 16 μs.

Fast, accurate, and compact

The controller addresses the ROM through the memory-address register. Separate advance curves are stored in the ROM, with memory addresses determined from the inputs of engine speed and level of vacuum.

The 5-bit a-to-d conversion of pressure data allows 32 separate curves, or schedules, of spark advance versus engine rpm to be stored. The result is a two-dimensional map of advance over a range of both manifold pressure, which is a function of engine load, and engine speed.

In order to compress the data, a 7-bit repeat value, as well as the actual subtraction value, is loaded from the ROM. In this way, a single subtraction value can be repeated up to 127 times. The repeat value is decremented after each subtraction interval, and once it reaches zero, new subtract and repeat values are extracted from the ROM.

The two-chip Rombic system is flexible in the type of signals it can process. In fact, three separate timing modes are available to establish which edges of the digital input signals determine the countup interval and the beginning of the countdown interval.

The reference interval may consist of timing between leading edges of the rpm input as shown in Fig. 3, or it can be the interval between trailing edges, or the interval from leading to trailing edges. Likewise, the beginning of the countdown interval can be selected to occur at either edge. Each of the input time options has system advantages dependent on the rpm sensor used.

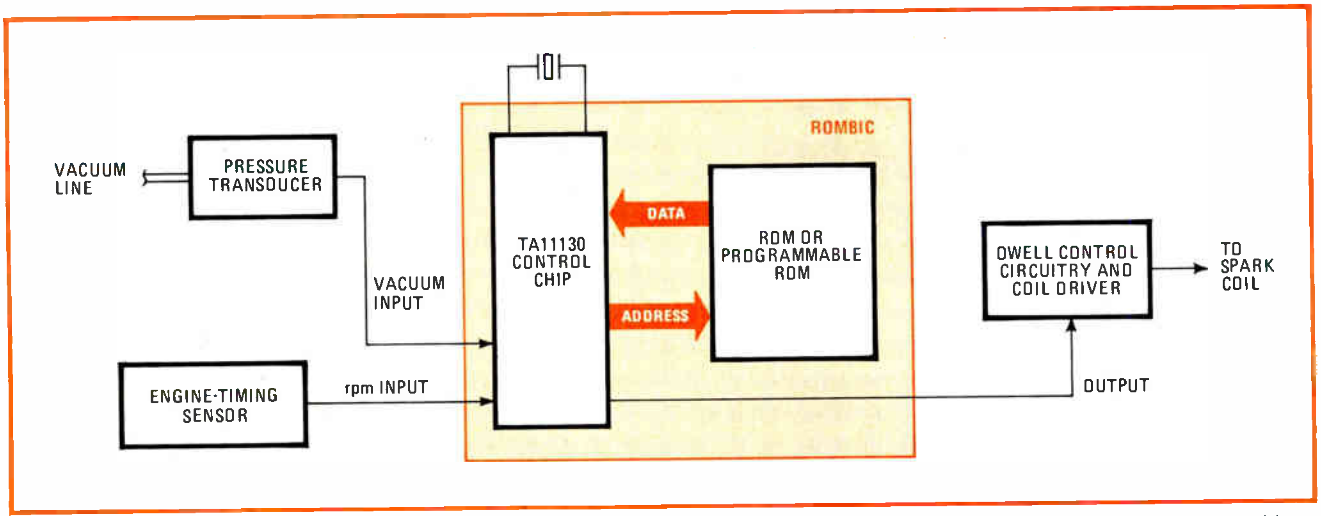
Different advantages

For example, the first two modes sample engine speed over a full period between the rpm pulses and start counting down at the beginning of the second period. In this way, only one edge of the input needs to be accurately timed. However, because the countdown interval starts a cycle after the countup period, there is a possibility of errors in ignition timing if the engine is accelerating or decelerating rapidly.

In the third mode, the reference interval and the starting point for the countdown interval occur within one cycle of the rpm input. Although both edges need to be accurate in this mode, the resultant spark firing is less sensitive to changes in engine speed.

The three timing modes differ in their transient response and sensor requirements, as well as in their ability to provide retard information. So it is up to the system designer to determine the best performance trade-off.

Reliable operation when controlling an automobile



2. Simple strategy. The Rombic system uses the two inputs of engine speed and mainfold pressure (vacuum) to determine a ROM address from which is fetched spark-advance data, which in turn times the signal sent to driver circuitry for the ignition coil.

ignition is a paramount consideration, lest a driver be left stranded. Therefore several default modes are incorporated into the Rombic system in the event of a failure.

There are four conditions in which the system will enter the default mode, during which the output signal will simply duplicate the input signal, effectively bypassing the circuitry. These conditions are: when the system is externally reset; when the clock oscillator fails; when engine speed is too low (causing the reference counter to overflow); and, optionally, when for any reason a spark firing does not occur before the next rpm pulse.

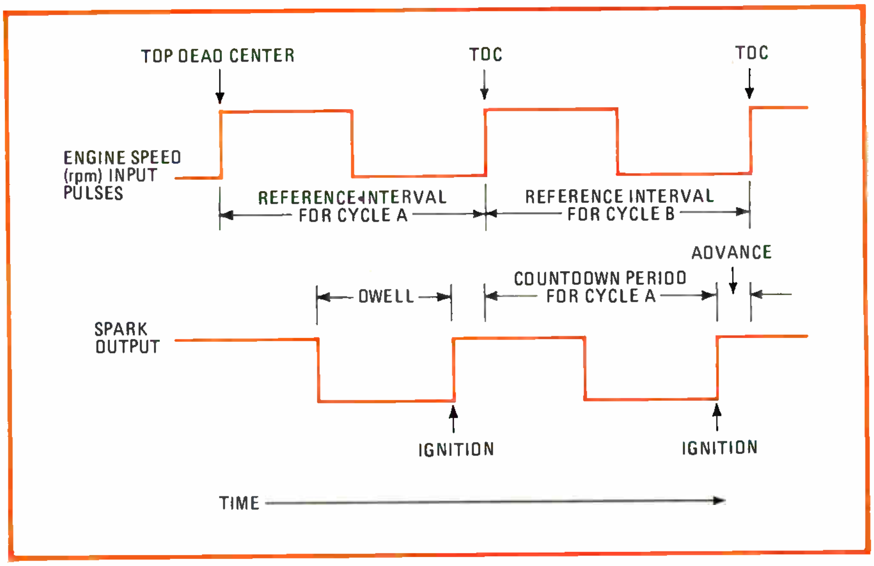
Built-in flexibility

Although Rombic is a dedicated two-chip system, it is flexible enough to control additional ignition requirements, such as dwell time. It determines ignition dwell, or ignition coil on-time, in one of three ways.

First, if the rpm input signal includes dwell information, Rombic will include it in the timing advance output. Secondly, the system can process rpm information that does not include dwell data, in which case it will provide only advance information to an external dwell-control module.

Finally, dwell may be controlled by an external IC driving Rombic's anti-dwell pin, which in effect responds to a "not-dwell" input. This optional third chip might also process throttle position and temperature information to satisfy additional emission requirements, or it could process knock-sensing information in order to improve overall engine performance. In either case, it is possible to further control and modify the output of the Rombic system.

Finally the system's memory size is expandable up to 2-K by 8 bits for more complex spark-advance curves. Rombic typically requires 10 to 70 bytes of ROM data per curve—each of which contains the spark advance data for one value of manifold pressure. It thus offers both hardware and software flexibility, which results in optimum cost and performance for various automotive applications. □



3. Two-timing. The reference interval, or countup period, occurs over one period of the engine-speed pulse, although it can occur between rising and falling edges. Spark ignition happens at the end of the countdown period, the timing of which is a function of the ROM data.

Comparator circuit regulates battery's charging current

by Ajit Pal
Indian Statistical Institute, Calcutta, India

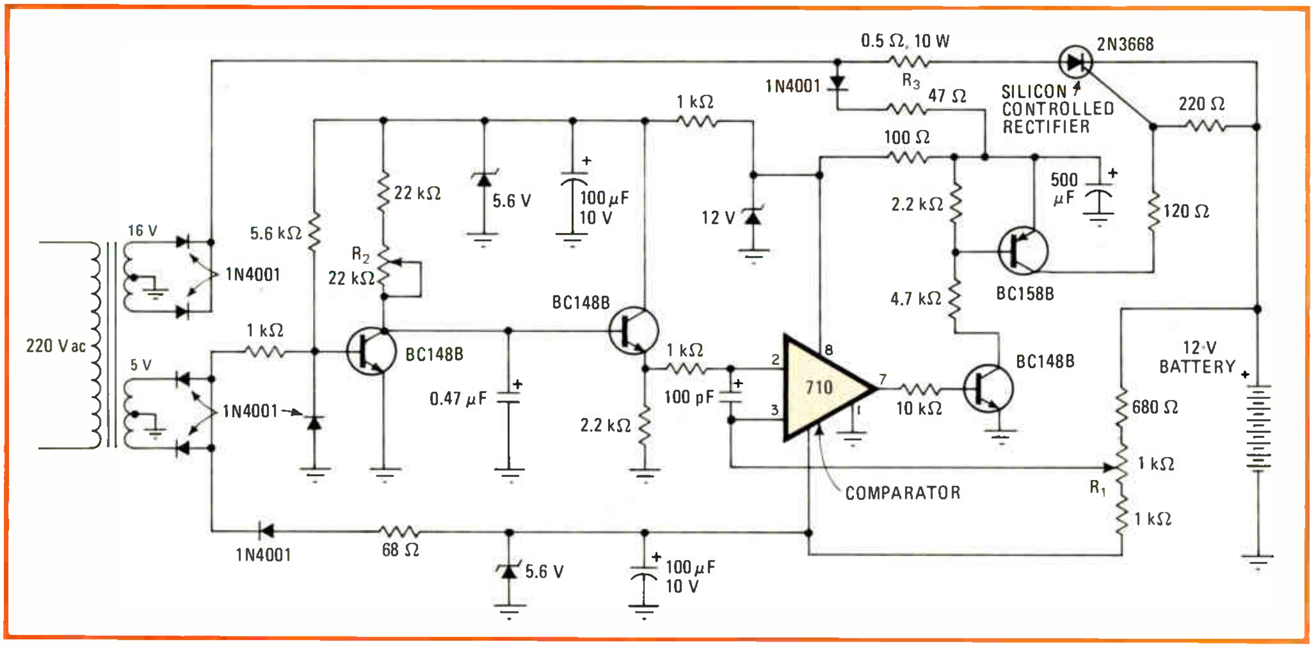
As charge builds up in a battery, its effective plate-charging area gradually decreases. To prevent damage, a good battery charger should continuously limit the charging current from the power line as a function of time. This completely solid-state charger performs the required regulation for a 12-volt automobile battery using a simple circuit built around the μA710 comparator. Although designed for 220-V operation, the charger is easily adapted for 110-V service, making it suitable for application in the U.S.

The comparator automatically adjusts the charging current by sensing the battery voltage, which increases as charge accumulates. The 710 also regulates the current by controlling the on-off switching times of a thyristor that is placed in series with the battery.

As shown in the figure, a dc voltage proportional to the battery voltage is applied to pin 3 of the comparator, with potentiometer R_1 determining the actual value. Simultaneously, a ramp signal that is derived from the power line is fed to pin 2 of the 710, with R_2 setting the slope of the ramp.

When the battery is being discharged, the voltage at pin 3 of the 710 is nearly equal to the lowest instantaneous ramp voltage, and so the output of the 710 is virtually always high. Thus, the thyristor is on for almost the entire 180° switching cycle.

At the other extreme, when the battery is almost fully charged, the voltage at pin 3 is practically equal to the highest instantaneous ramp voltage, and so the thyristor is on for only a small portion of the cycle. For intermediate conditions, the thyristor will be on from between 0° and 180° of the cycle. The maximum charging current is limited by the resistor R_3. □



Cutting down. This circuit progressively limits the amount of charging current through a standard 12-V automobile battery as it attains its nominal terminal voltage from its discharged condition, thus avoiding cell damage. The single 710 comparator performs comparison regulation functions. Other circuitry sets conditions where the thyristor can be fired over a 0° to 180° cycle.

Power-sharing bridge circuit improves amplifier efficiency

by Jim Edrington
Texas Instruments Inc., Austin, Texas

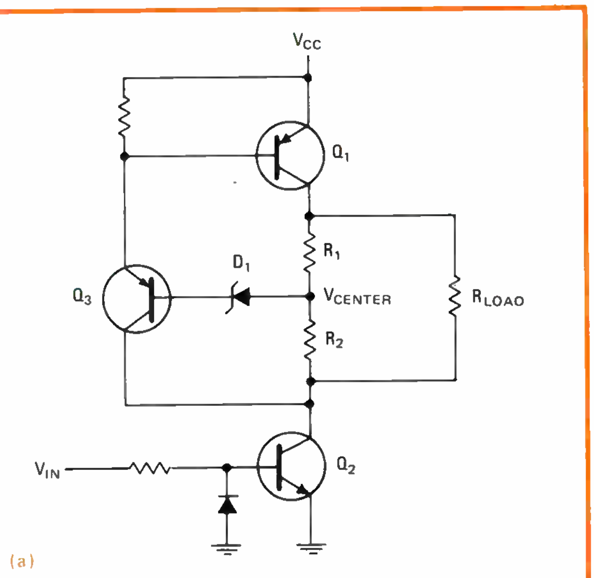
This linear bridge amplifier offers several advantages in driving motors and servo systems, including obtaining maximum efficiency with a single power supply and with dc coupling, which as a result reduces circuit complexity. Most notable, however, is that the four transistors in the amplifier will equally share load currents, as well as simplifying the drive requirements. These factors permit lower-cost transistors to be applied and allow their heat-sink requirements to be reduced.

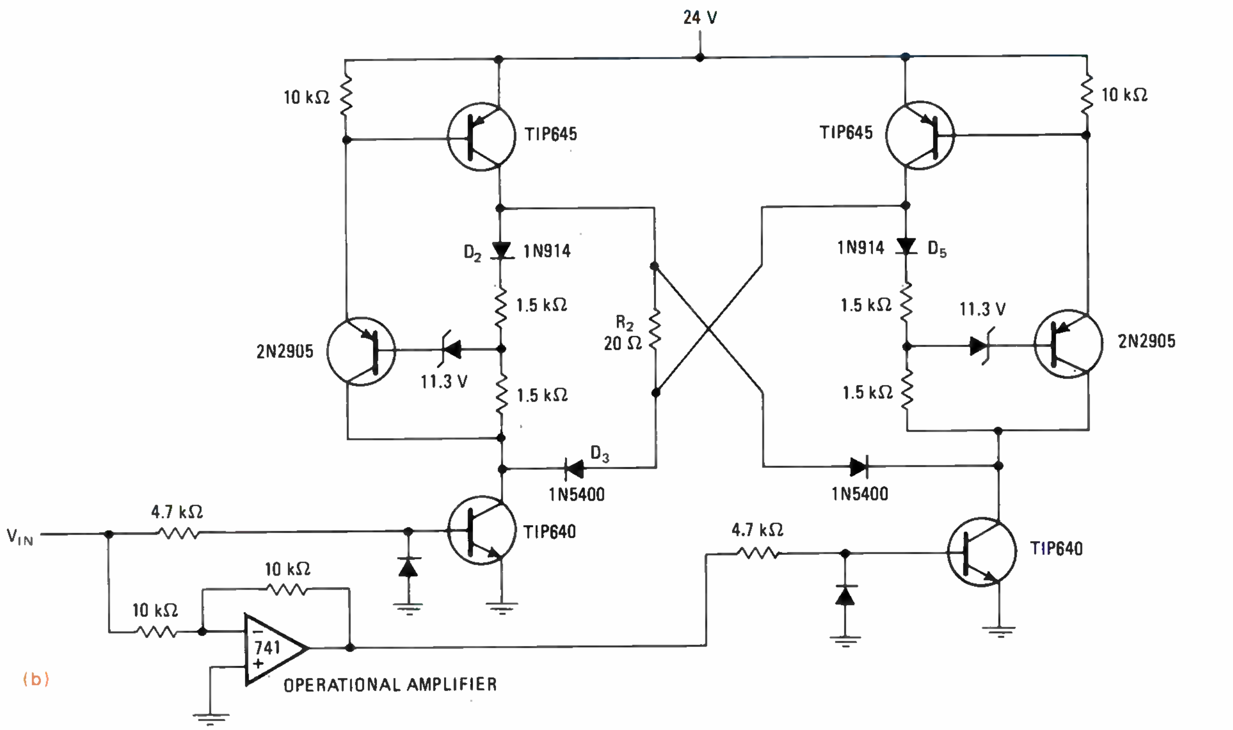
Shown in (a) is one half of the bridge-type circuit, which illustrates the amplifier's operation. Positive input excursions from the driver turn on current sink Q_2, with a portion of Q_2's collector current passing through transistor Q_3. Q_3's current flow causes source transistor Q_1 to turn on.

Because the majority of the flow must pass through Q_1 and Q_2, the collector-to-emitter voltage of both transistors must be equal to ensure equal power dissipation. This voltage-matching requirement is achieved by clamping the gain of Q_1 to the voltage at the center of the load with a zener diode. Thus the virtual center of the load will be maintained at $V_{cc}/2$ and $V_{Q_1ce} = V_{Q_2ce}$, provided $R_1 = R_2$. The zener diode, D_1, must have a value of $V_z = (V_{cc}/2) - 1.4$ to meet the requirement for the reference potential.

Two of these circuits may be readily incorporated into a full-bridge arrangement, as shown in (b), that is suitable for driving electromechanical devices. Adding diodes D_2 through D_5 isolate one branch's functions from the other. With this configuration, each branch conducts for half of the input cycle thereby eliminating virtually all crossover difficulties.

The isolation diodes will alter the divider's center voltage by 0.7 volts, however, and so the value of the zener voltage must be slightly changed. In this case, it will be $V_z = (V_{cc}/2) - 1.4 + 0.7 = 11.3$ v. In most applications, selecting the nearest standard zener value will suffice. □





Divided driver. A rudimentary amplifier (a) may be designed so that Q_1 and Q_2 carry equal load on a positive excursion of an input signal, using a zener diode of suitable value for biasing a load center to cause $V_{Q_1ce} = V_{Q_2ce}$. Combining two such sections in a balanced bridge arrangement (b) builds a dc-coupled amplifier that is simple, can run from one supply, and can ensure that all amplifiers may handle a proportionate share of the power. This combination reduces electrical specifications of individual transistors, thereby reducing their cost.

Multiplexer does double duty as dual-edge shift register

by James A. Mears
Dallas, Texas

Useful and sometimes unusual logic functions may be found disguised as parts with other functional names, and they often offer circuit advantages not found in the part designed for a given task. A good example of this principle is the 74157 quad two-input multiplexer, which can serve in a pinch as a clocked shift register.

Unlike other registers that advance on one edge of the clock, it will shift on each successive transition. This attribute is particularly useful when it is necessary to process data at twice the clock frequency without using a frequency doubler.

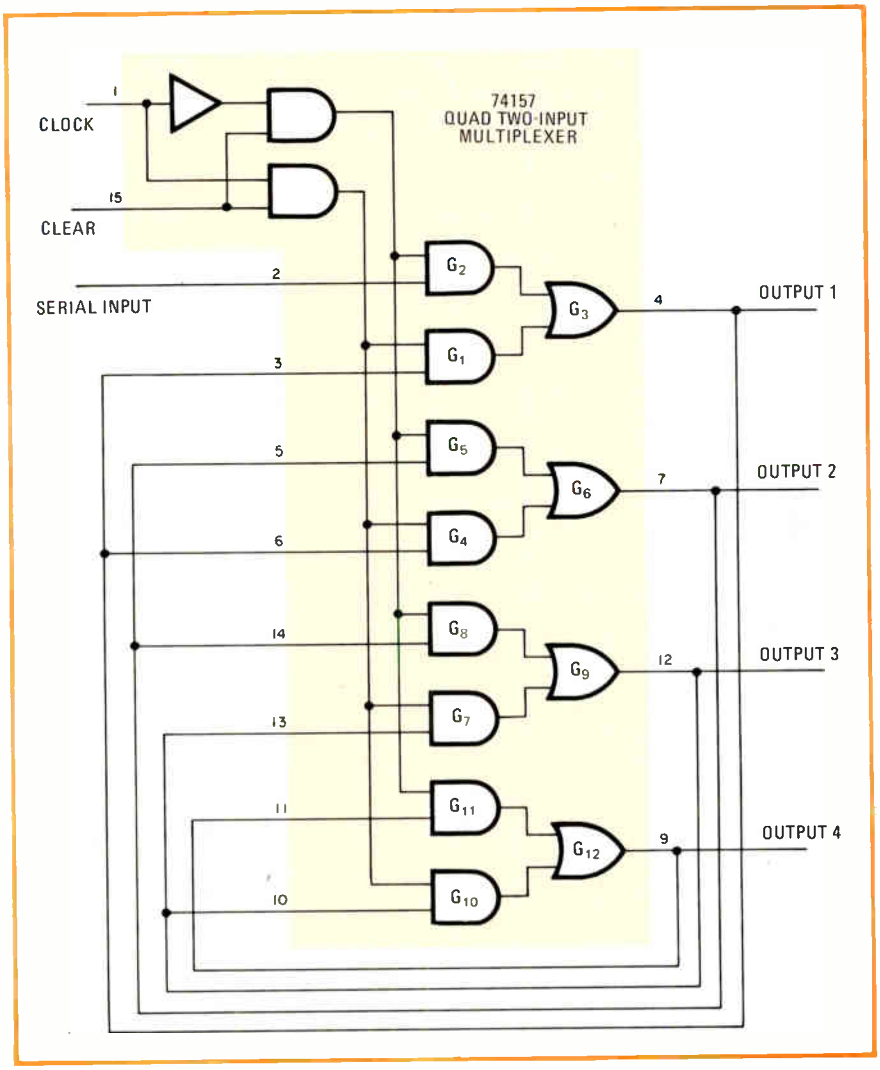
A good application for this type of register would be in the timing chain of a dynamic memory controller, where it could give a fine timing resolution without the need for a high-frequency clock. The pin functions in the figure have been renamed to give a better understanding of the circuit operation of the modified multiplexer.

Signals applied to the serial input are routed to output 1 through the AND-OR gate combination, G_1 through G_3, with output 1 connected to the alternate input of G_1 and to the corresponding input of the next stage, G_4 through G_6. The last three stages are connected similarly to form a chain of D latches (another good use for the 74157).

Thus, when the clock is high, the input signal will pass to the output, back to the alternate input and to the next stage. On the low-going clock edge, the output of the first stage is latched, and the signal is passed to the next stage's output. This process is repeated for each clock transition, thereby shifting the signal through the register. At any time, the register can be disabled (all outputs low) by bringing the clear input high.

Variations of this circuit can be built with the 74257, which is equivalent to the 74157 but has three-state outputs. The circuit can also be built with the 74158 (74157 with inverted outputs) by adding inverters to the outputs and connecting them up as before. Registers may be cascaded by connecting the serial input to the preceding stage's output. □

Designer's casebook is a regular feature in Electronics. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $75 for each item published.



Disguise. Many logic chips can simulate other functions, such as this 74157 quad multiplexer, which performs well as a shift register. This part also gives the added advantage of dual-edge clocking, thus eliminating the need for frequency doublers in such circuits as the timing chain of high-resolution dynamic memory controllers.

TI-59 program tracks satellites in elliptical orbits

by Janos Molnár
Siófok, Hungary

This versatile program for the TI-59 can find orbital parameters for man-made satellites that rotate in highly elliptical paths around the earth. Quickly solving an interrelated set of 26 equations based upon Kepler's laws of planetary motion, it will serve as an invaluable satellite tracking tool for the astronomy buff.

The program first determines the major-axis elliptical orbit, given the apogee (H_A) and perigee (H_P) of the satellite path, with the aid of formulas 1 and 2 from the equation set shown in the table. The rotating period of the satellite (τ) and its mean angular velocity (ω) depend only on the length of the major axis (a) and a few natural constants and so τ may be found.

Next, the time (t) relationship between the eccentric anomoly (E) and the time measured from the point of the perigee, (t_P) is solved using formulas 4 and 8. Then the relationship between the instantaneous central angle of the satellite (θ) measured with respect to its elliptical geometrical position is calculated by formulas 10 and 11.

The relationship between the axial rotation of the earth and its corresponding satellite equatorial-ascending position helps to ascertain the relative earth-based coordinates. These measurements are found with formulas 13, 14, and 15. Once the coordinates of the true observing point and the trace points (subsatellite) points are known, the spherical distance, elevation, and azimuth of the satellite may be found by applying formulas 12, 16, 17, 18, and 19.

Various properties of motion are also taken into consideration in this program. For instance, the attractive force from the earth pushes a satellite into an elliptical orbit and also rotates this orbit within a sphere. Slight path displacements that occur in the satellite's orbit are found by using formulas 21, 23, and 24. Perigee wandering and satellite nodal ascending time may be calculated with formulas 20, 22, 24, and 25.

An example illustrates the program's usefulness. Consider the case of an elliptical satellite in the Oscar series of amateur radio vehicles located over Budapest, Hungary, that has $\phi_O = 47.5°$ and $\lambda_O = 19.2°$. A tracking accuracy of $\delta = 0.005$ (n = 3) is desired. By entering an

LIST OF SYMBOLS

Symbol	Definition	Symbol	Definition
A	azimuth angle measured from North Pole in the horizontal plane (°)	T*	orbital period, presented (min)
a	major axis (km)	Δt	time between the ascending node and the satellite position (min)
B	parameter	t_p	time of perigee passage (min)
b	minor axis (km)	t_{po}	intital perigee passage time (min)
D	distance traveled by the satellite from the observation post (km)	t	time difference (min)
E	eccentric anomaly (rad)	δ	error limit of formula 9
E_p	eccentric anomaly at perigee (rad)	ϵ	eccentricity
e	elevation angle above the horizontal plane (°)	Δ	earth's central angle between the perigee and the observation post and the point of ground trace (°)
H_A	altitude of apogee (km)	ζ	parameter
H_P	altitude of perigee (km)	θ	orbital central angle between the perigee and the satellite position (°, rad)
i	inclination angle of the orbit that is related to the equatorial plane (°)	λ_E	longitude of an ascending node (°)
J	dimensionless term from the potential function	λ_{EO}	initial longitude of an ascending node (°)
k	parameter	λ_O	longitude of observation post (°)
M	mean anomaly-average angular velocity (rad/min)	λ_S	longitude of the subsatellite point (°)
M_P	angular velocity at perigee (rad/min)	μ	earth's gravitational constant (km^3/s^2)
n	root's precious number of formula 9	Σ	orbital central angle between the ascending node and the satellite (°)
R	orbital radius (km)	Σ_P	amount of perigee (°, rad)
R_F	mean radius of earth (km)	Σ_{PO}	initial perigee argument (°, rad)
R_{FO}	equatorial radius of earth (km)	τ	time measured from perigee passage (min)
T	time interval between two successive perigee passes, anomalistic period, calculated (min)	ϕ_O	latitude of observation post (°)
T_E	actual time of equatorial ascending node (h, min, s)	ϕ_P	latitude of the perigee (°)
T_N	nodal orbital period (min)	ϕ_S	latitude of the subsatellite point (°)
T_λ	rotation period of orbital plane (min)	ω	mean angular velocity (rad/min)
T_Σ	rotations period of perigee in orbital plane (min)	ω_F	angular velocity of the earth (°, min)

INTEGRATED EQUATION SET FOR SATELLITE-ORBIT ANALYSIS

(1) $a = \dfrac{H_A + H_P}{2} + R_F$

(2) $\epsilon = \dfrac{H_A - H_P}{2a}$

(3) $\omega = \dfrac{2\pi}{T} = 60\sqrt{\mu a^{-3}}$

(4) $\Sigma'_P = \sin^{-1}\left\{\dfrac{\sin \phi_P}{\sin i}\right\}$

$\Sigma_P = \Sigma'_P$ for $0° \leqslant \xi < 90°$

$= 180° - \Sigma'_P$ for $90° \leqslant \xi < 270°$

$= 360° + \Sigma'_P$ for $270° \leqslant \xi < 360°$

where $\xi = (\lambda_P - \lambda_E)\ \mathrm{sign}\ (\cos i)$

(5) $E'_P = \cos^{-1}\left\{\dfrac{\epsilon + \cos \Sigma_P}{1 + \epsilon \cos \Sigma_P}\right\}$

$E_P = E'_P$ for $0 \leqslant \phi_P$

$= 2\pi - E'_P$ for $0 \geqslant \phi_P$

(6) $t_P = \dfrac{E_P - \epsilon \sin E_P}{\omega} = \dfrac{M_P}{\omega}$

(7) $t = K\,\Delta t = T^* - T_E$

(8) $M = \omega(t - t_p) = \omega\tau$

$\tau = \tau$ for $0 \leqslant \tau < T$

$= \tau - T$ for $T \leqslant \tau$

(9) $0 = \epsilon \sin E - E + M$

(10) $\theta' = \cos^{-1}\left\{\dfrac{\cos E - \epsilon}{1 - \epsilon \cos E}\right\}$

$\theta'' = \theta'$ for $0 \leqslant E \leqslant \pi$

$= -\theta' + 2\pi$ for $\pi < E \leqslant 2\pi$

where $\theta = \theta''\,(180/\pi)\ \mathrm{sign}\ (M)$

(11) $R = a(1 - \epsilon \cos E)$

(12) $\zeta = \dfrac{R_F}{R}$

(13) $\Sigma = \Sigma_P + \theta$

Constants

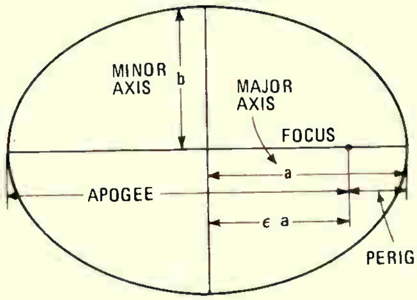
$R_F = 6{,}371.0$ km

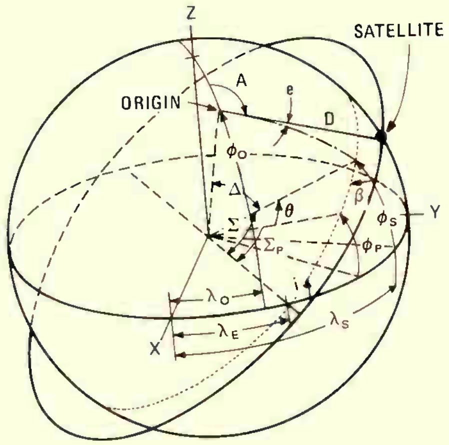
$R_{Fq} = 6{,}378.2$ km

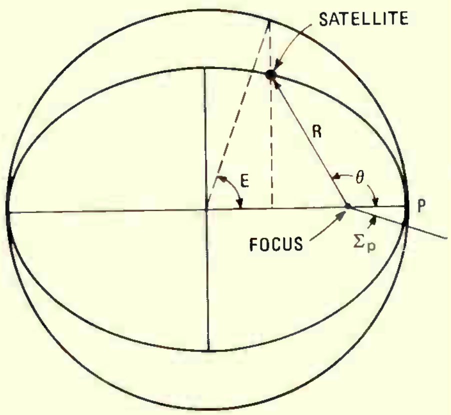
$J = 1.627 \times (10^{-3})$

$\mu = 398{,}603\ \mathrm{km^3/s^2}$

$\omega_F \simeq 0.25°/\mathrm{min}$







(14) $\phi_S = \sin^{-1}\{\sin i \sin \Sigma\}$

(15) $\lambda_S = \dfrac{\cos i}{|\cos i|} \cos^{-1}\left\{\dfrac{\cos \Sigma}{\cos \phi_S}\right\} - \omega_F t + \lambda_E$

(16) $\Delta = \cos^{-1}\{\sin \phi_O \sin \phi_S + \cos \phi_O \cos \phi_S \cos(\lambda_S - \lambda_O)\}$

(17) $e = \tan^{-1}\left\{\dfrac{\cos \Delta - \zeta}{\sin \Delta}\right\}$

(18) $|A| = \cos^{-1}\left\{\dfrac{\sin \phi_S - \sin \phi_O \cos \Delta}{\sin \Delta \cos \phi_O}\right\}$

(19) $D = R\sqrt{1 + \zeta^2 - 2\zeta \cos \Delta}\ \mathrm{sign}\ (e)$

(20) $\Sigma_P = \Sigma_{PO} + 360(t - t_{po})/T_\Sigma$

(21) $T_\Sigma = \dfrac{T}{B\,(5\cos^2 i - 1)/2}$

(22) $\lambda_E = \lambda_{EO} \pm 360(t - t_{po})/T_\lambda$

(23) $T_\lambda = \dfrac{T}{B \cos i}$

(24) $\dfrac{J}{4}\left(\dfrac{1}{\frac{H_A}{R_{Fq}} + 1} + \dfrac{1}{\frac{H_P}{R_{Fq}} + 1}\right)^2 = B$

(25) $T_N = T\left[1 - J\left(\dfrac{5\cos^2 i - 1}{2}\right)\left(\dfrac{R_F}{a}\right)^2\right]$

(26) $\delta = \tfrac{1}{2}\,10^{-n} \geqslant |f(E_O) - f(E)|$

PRINTER OUTPUT FOR TI-59 ELLIPTICAL SATELLITE TRACKING PROGRAM

TIM (t)	F (ϕ_S)	L (λ_S)	Δ	e	A	D	Σ	R
0.00	0.00	0.00	50.35	−9.33	154.72	−6,502.06	0.01	8,332.85
100.00	52.65	96.61	47.51	31.00	53.41	23,573.59	108.58	27,404.14
200.00	38.82	98.36	55.86	25.44	67.59	34,876.05	131.63	38,050.33
300.00	27.28	85.23	54.42	27.88	86.94	38,684.83	146.88	42,042.81
629.50	−56.80	105.10	126.19	−56.45	137.41	−14,849.06	266.12	10,168.44
659.50	9.50	−159.09	122.98	−56.57	2.01	−13,354.96	11.35	8,770.73

PRINTER LISTING: TI-59 PROGRAM FOR ELLIPTICALLY ORBITING SATELLITES

Location	Key										
000	LBL	043	7	086	RCL	129	STO	172	06	215	+
001	A′	044	2	087	18	130	00	173	INV	216	RCL
002	(	045	4	088	SUM	131	I X I	174	GE	217	26
003	STO	046	3	089	30	132	EXC	175	CE	218	=
004	09	047	0	090	RCL	133	00	176	π	219	SBR
005	SIN	048	SBR	091	30	134	OP	177	X	220	DEG
006	X	049	(	092	RTN	135	10	178	2	221	STO
007	RCL	050	2	093	LBL	136	STO	179	–	222	37
008	20	051	1	094	DEG	137	26	180	RCL	223	SIN
009	–	052	SBR	095	÷	138	CLR	181	27	224	X
010	RCL	053	(	096	3	139	STO	182	=	225	RCL
011	09	054	2	097	6	140	01	183	STO	226	14
012	+	055	7	098	0	141	RAD	184	27	227	SIN
013	RCL	056	SBR	099	=	142	PGM	185	LBL	228	=
014	00	057	(	100	INV	143	08	186	CE	229	INV
015	)	058	7	101	INT	144	E	187	RCL	230	SIN
016	RTN	059	5	102	X	145	COS	188	27	231	STO
017	LBL	060	SBR	103	3	146	X	189	X	232	31
018	(	061	(	104	6	147	RCL	190	1	233	RCL
019	OP	062	5	105	0	148	20	191	8	234	37
020	04	063	4	106	=	149	–	192	0	235	COS
021	RC*	064	SBR	107	RTN	150	1	193	÷	236	÷
022	28	065	(	108	LBL	151	=	194	π	237	RCL
023	OP	066	1	109	C	152	+/–	195	=	238	31
024	06	067	3	110	STO	153	STO	196	PRD	239	COS
025	OP	068	SBR	111	30	154	38	197	26	240	=
026	00	069	(	112	÷	155	÷	198	DEG	241	INV
027	CLR	070	1	113	RCL	156	(	199	RCL	242	COS
028	1	071	6	114	17	157	RCL	200	21	243	STO
029	SUM	072	SBR	115	=	158	06	201	PRD	244	32
030	28	073	(	116	INV	159	COS	202	38	245	1
031	LBL	074	7	117	INT	160	–	203	RCL	246	8
032	=	075	7	118	X	161	RCL	204	19	247	0
033	RTN	076	SBR	119	RCL	162	20	205	÷	248	X⇌T
034	LBL	077	(	120	17	163	=	206	RCL	249	RCL
035	D′	078	3	121	–	164	1/X	207	38	250	37
036	3	079	5	122	RCL	165	INV	208	=	251	INV
037	0	080	SBR	123	24	166	COS	209	STO	252	GE
038	STO	081	(	124	=	167	STO	210	39	253	)
039	28	082	ADV	125	X	168	27	211	LBL	254	RCL
040	FIX	083	RTN	126	RCL	169	π	212	Σ+	255	32
041	02	084	LBL	127	22	170	X⇌T	213	RCL	256	+/–
042	3	085	X⇌T	128	=	171	RCL	214	12	257	+

Instructions

- Key in program, first partitioning calculator for 40 data registers by entering (4) OP* 17
- Enter earth coordinates of observation point and accuracy index to which orbital parameters are to be found:
  (ϕ_O), *A*, (λ_O), *R/S*, (n), *R/S*
- Specify orbital parameters of apogee and perigee (km), inclination of orbit relative to equatorial plane (°), argument of perigee (°), longitude of ascending node (°), and actual time equatorial ascending (if known), in hours (h). minutes (min), seconds (s):
  (H_A), *R/S*, (H_P), *R/S*, (i), *R/S*, (Σ_P), *R/S*, (λ_E), *R/S*, (T_E), *R/S*
  Calculator will display satellite's orbital time, T, in minutes, between two successive perigee passes after entry of H_P
- Press B′ to find initial coordinates of satellite's perigee point as observed from specified earth location:
  t, ϕ_S, λ_S, Δ, e, A, D, Σ, and R are printed
- Select intervals of time at which satellite's position is to be found from its ascending node and time from its ascending node to the final satellite coordinates of interest:
  (Δt), *B*, (t), *C*
  Program finds orbital parameters from T_E to t, in steps of Δt
- Alternatively, specify the actual (real) time in from which the orbital parameters are to be found in steps of new Δt:
  (Δt), *B*, (t^*), *D*
- Press R/S RST CLR to terminate program

258	3	322	RCL	386	00	450	STO	514	=	578	24
259	6	323	39	387	=	451	10	515	STO	579	+/−
260	0	324	=	388	NOP	452	R/S	516	22	580	+
261	=	325	÷	389	SBR	453	STO	517	1/X	581	2
262	STO	326	RCL	390	X⇌T	454	11	518	X	582	X
263	32	327	33	391	IFF	455	R/S	519	π	583	π
264	LBL	328	SIN	392	01	456	STO	520	X	584	=
265	)	329	=	393	DMS	457	08	521	2	585	STO
266	RCL	330	INV	394	GTO	458	+/−	522	=	586	24
267	32	331	TAN	395	C	459	INV	523	STO	587	LBL
268	X	332	STO	396	LBL	460	LOG	524	17	588	1/X
269	RCL	333	34	397	DMS	461	÷	525	R/S	589	RCL
270	25	334	OP	398	INV	462	2	526	STO	590	24
271	=	335	10	399	FIX	463	STO	527	14	591	—
272	+	336	STO	400	÷	464	03	528	COS	592	RCL
273	RCL	337	36	401	6	465	=	529	OP	593	20
274	13	338	1	402	0	466	EXC	530	10	594	X
275	—	339	+	403	+	467	08	531	STO	595	RCL
276	RCL	340	RCL	404	RCL	468	R/S	532	25	596	24
277	30	341	39	405	23	469	STO	533	RCL	597	SIN
278	X	342	X^2	406	=	470	15	534	14	598	=
279	.	343	—	407	÷	471	STO	535	R/S	599	÷
280	2	344	2	408	2	472	20	536	STO	600	RCL
281	5	345	X	409	4	473	STO	537	12	601	22
282	0	346	RCL	410	=	474	21	538	X	602	=
283	6	347	39	411	INV	475	R/S	539	π	603	STO
284	8	348	X	412	INT	476	STO	540	÷	604	24
285	4	349	RCL	413	X	477	16	541	1	605	DEG
286	=	350	28	414	2	478	INV	542	8	606	6
287	SBR	351	=	415	4	479	SUM	543	0	607	.
288	DEG	352	$\sqrt{X}$	416	=	480	20	544	=	608	3
289	STO	353	X	417	INV	481	SUM	545	STO	609	STO
290	32	354	RCL	418	DMS	482	21	546	24	610	02
291	—	355	38	419	LBL	483	2	547	RAD	611	RCL
292	RCL	356	=	420	D	484	INV	548	COS	612	12
293	11	357	PRD	421	STF	485	PRD	549	+	613	R/S
294	=	358	36	422	01	486	20	550	RCL	614	STO
295	COS	359	RCL	423	FIX	487	INV	551	20	615	13
296	X	360	31	424	04	488	PRD	552	=	616	RTN
297	RCL	361	SIN	425	PRT	489	21	553	÷	617	STO
298	31	362	—	426	STO	490	6	554	(	618	23
299	COS	363	RCL	427	29	491	3	555	1	619	DMS
300	X	364	28	428	DMS	492	7	556	+	620	EXC
301	RCL	365	X	429	—	493	1	557	RCL	621	23
302	10	366	RCL	430	RCL	494	STO	558	20	622	RTN
303	COS	367	10	431	23	495	19	559	X	623	LBL
304	+	368	SIN	432	=	496	SUM	560	RCL	624	B'
305	RCL	369	=	433	CP	497	21	561	24	625	STF
306	31	370	÷	434	GE	498	RCL	562	COS	626	00
307	SIN	371	RCL	435	STF	499	21	563	=	627	GTO
308	X	372	10	436	+	500	INV	564	INV	628	Σ+
309	RCL	373	COS	437	2	501	PRD	565	COS	629	LBL
310	10	374	÷	438	4	502	20	566	STO	630	B
311	SIN	375	RCL	439	=	503	Y^X	567	24	631	STO
312	=	376	33	440	LBL	504	1	568	1	632	18
313	STO	377	SIN	441	STF	505	.	569	8	633	INV
314	28	378	=	442	X	506	5	570	0	634	STF
315	INV	379	INV	443	6	507	+/−	571	X⇌T	635	00
316	COS	380	COS	444	0	508	X	572	RCL	636	CLR
317	STO	381	STO	445	=	509	3	573	12	637	RTN
318	33	382	35	446	GTO	510	7	574	INV		
319	RCL	383	SBR	447	C	511	8	575	GE		
320	28	384	D'	448	LBL	512	8	576	1/X		
321	—	385	IFF	449	A	513	1	577	RCL		

apogee of 35,786 kilometers, a perigee of 1,500 km, and the previously mentioned parameters, λ_o and ϕ_o, the satellite's orbital time is discovered to be 656.195 minutes.

Now entering the angle of inclination relative to the equatorial plane (57°), the argument of the perigee (329.74°), the longitude of the ascending node (0°), and the actual time of equatorial ascending (13.1530), given an interval of time equal to 100 min at which the satellite's position is to be known, the set of data displayed in the table on page 147 is obtained by the program. The first four rows of the table is for the stipulated condition. The last two rows represent Δt being changed to 30 min and T* changed to 23.4500. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.

Engineer's newsletter

Filters optimize digital radios

Digital radio system designers will undoubtedly welcome the recent labor-saving research carried out by Larry J. Greenstein and Diane Vitello of Bell Laboratories in Holmdel, N. J. Since widely used digital radio modulations such as quaternary-phase–shift keying, minimum-shift keying, and sinusoidal-frequency–shift keying usually require some sort of transmitter filtering before they comply with the Federal Communications Commission's spectrum emission rules, the Bell engineers have developed numerical solutions to the problem of ascertaining **which Butterworth and Chebyshev filters have the largest bandwidth allowable under those rules.** The results, calculated for the 6-GHz common-carrier band, are accurate to within a few percent for the 4- and 11-GHz bands. For further information, write to the authors at Bell Laboratories, Crawford Corner Rd., Holmdel, N. J. 07733.

Learn all about AT&T's X.25

American Telephone & Telegraph Co. has joined IBM to support the international packet switching standard known as X.25. Manufacturers of data-communications equipment that will hook up to AT&T's advanced communication service (ACS) will want to know **what the telephone company means by its basic data transport network services.** For the descriptive technical reference, send $11 to the Publishers Data Center Inc. at P. O. Box C738, Pratt Street Station, Brooklyn, N. Y. 11205.

One transistor upgrades TTL clock

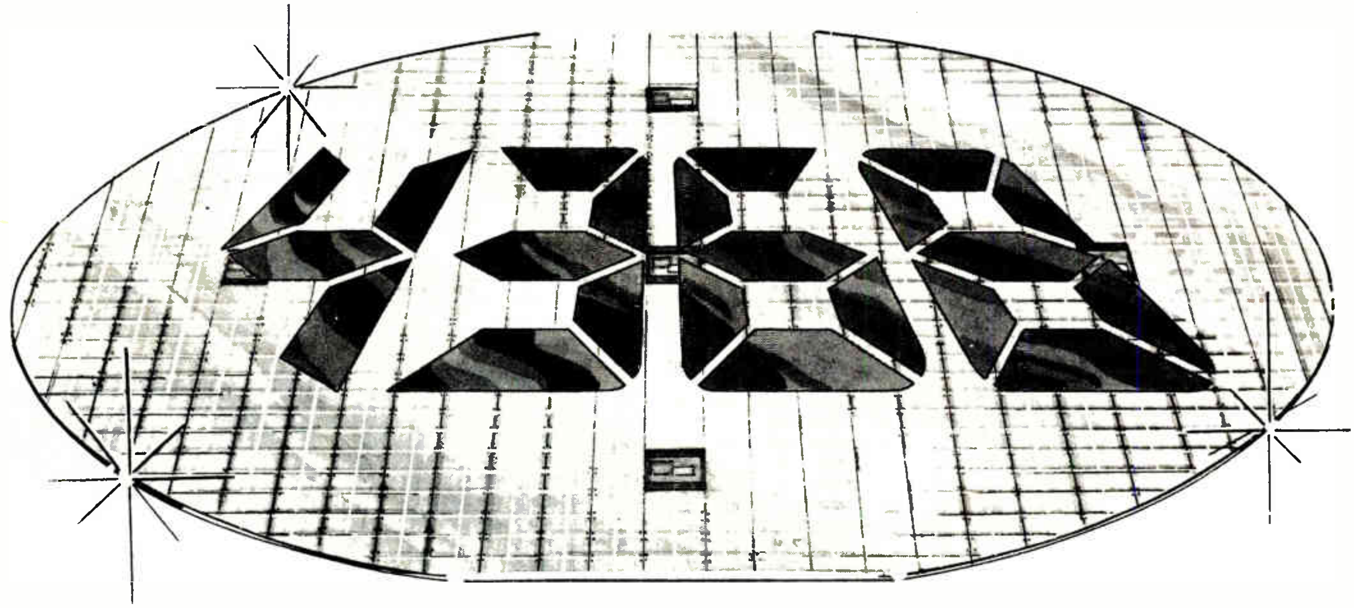
The use of a Schmitt-input inverter as a simple pulse generator may be common practice, but the circuit suffers from two drawbacks: the TTL input bias current places a practical upper limit of about 2,000 Ω on the resistor; and low-frequency operation demands the use of a large electrolytic capacitor, which in turn makes the circuit sensitive to power supply variations. According to A. A. Zuarets of the Nuclear Medicine division at Elscint Ltd.'s Advanced Technology Center in Haifa, Israel, these difficulties can be overcome **by adding an emitter follower at the input to the inverter.** With this circuit the resistor value can be hundreds of kilohms. This makes it possible to use smaller and more stable capacitors and operate at low frequencies with the bonus of improved power supply rejection. Zuarets can be reached at P. O. Box 5258, Haifa 31-051, Israel.

Improve optocoupler protection circuits

Peter H. Schwartz of Sunnyvale, Calif., points out that the optocoupler protection circuit shown in Engineer's Notebook [*Electronics*, Sept. 8, p. 153] has several potential problems. For example, the maximum permissible reverse voltage across a light-emitting diode is typically low (in the case of the 4N33, 3 V at most), and this may not be enough for this circuit. Moreover, the 4N33 is a Darlington-output device—while sensitive, it is slow to turn on, taking from 5 to 10 μs. And finally, because of the 4N33's Darlington configuration, its turn-on voltage is too high to be compatible with TTL logic—for example, the flip-flop shown must be complementary-MOS.

A possible cure, writes Schwartz, is to **insert 1N4148 diodes in series with the optocoupler input LEDs,** and to bridge those LEDs with resistors in the 50-kΩ range. Substitution of 6N137-type optocouplers for the 4N33 devices would also be helpful. One HCPL-2630 from Hewlett-Packard would replace both optocouplers.

-Harvey J. Hindin



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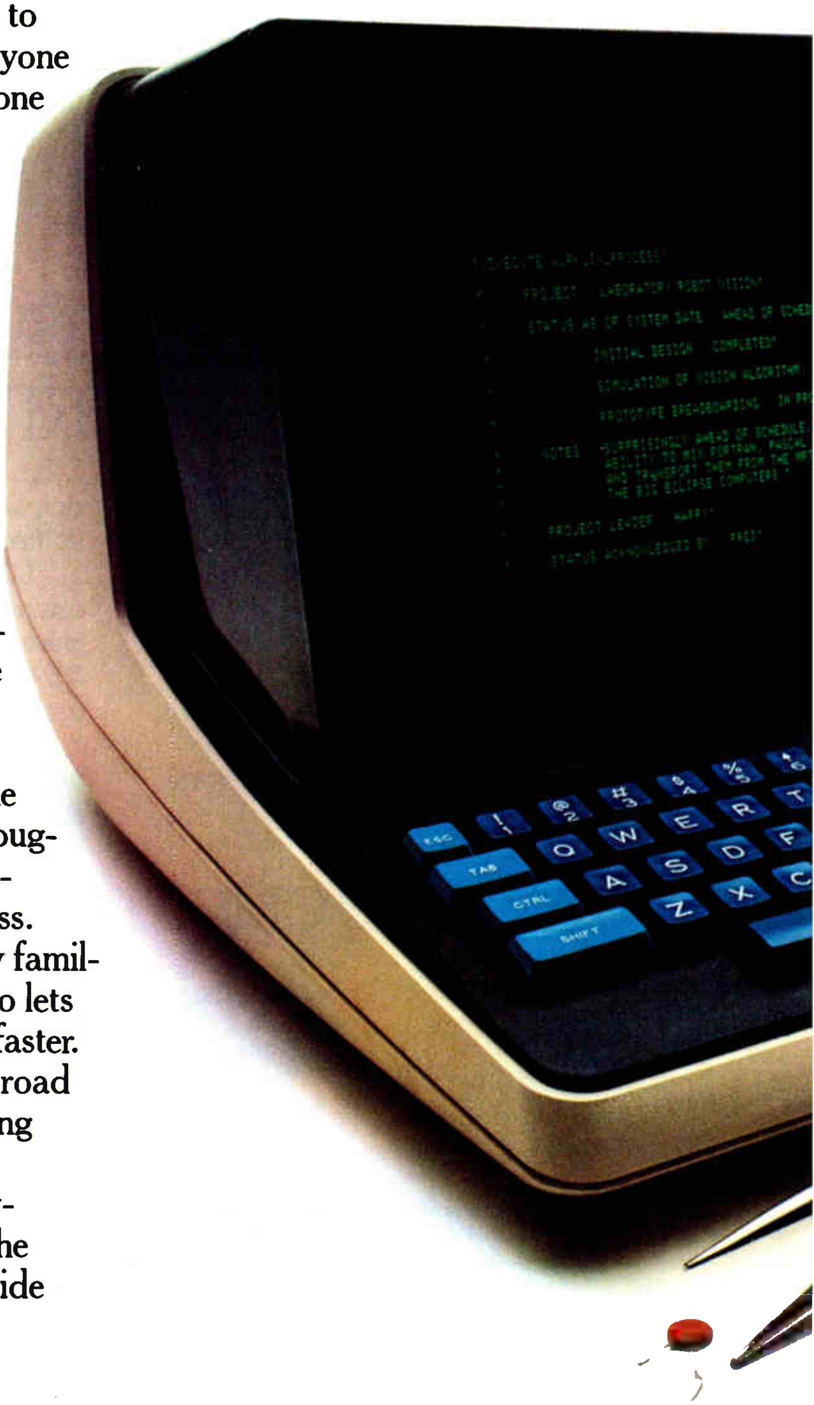

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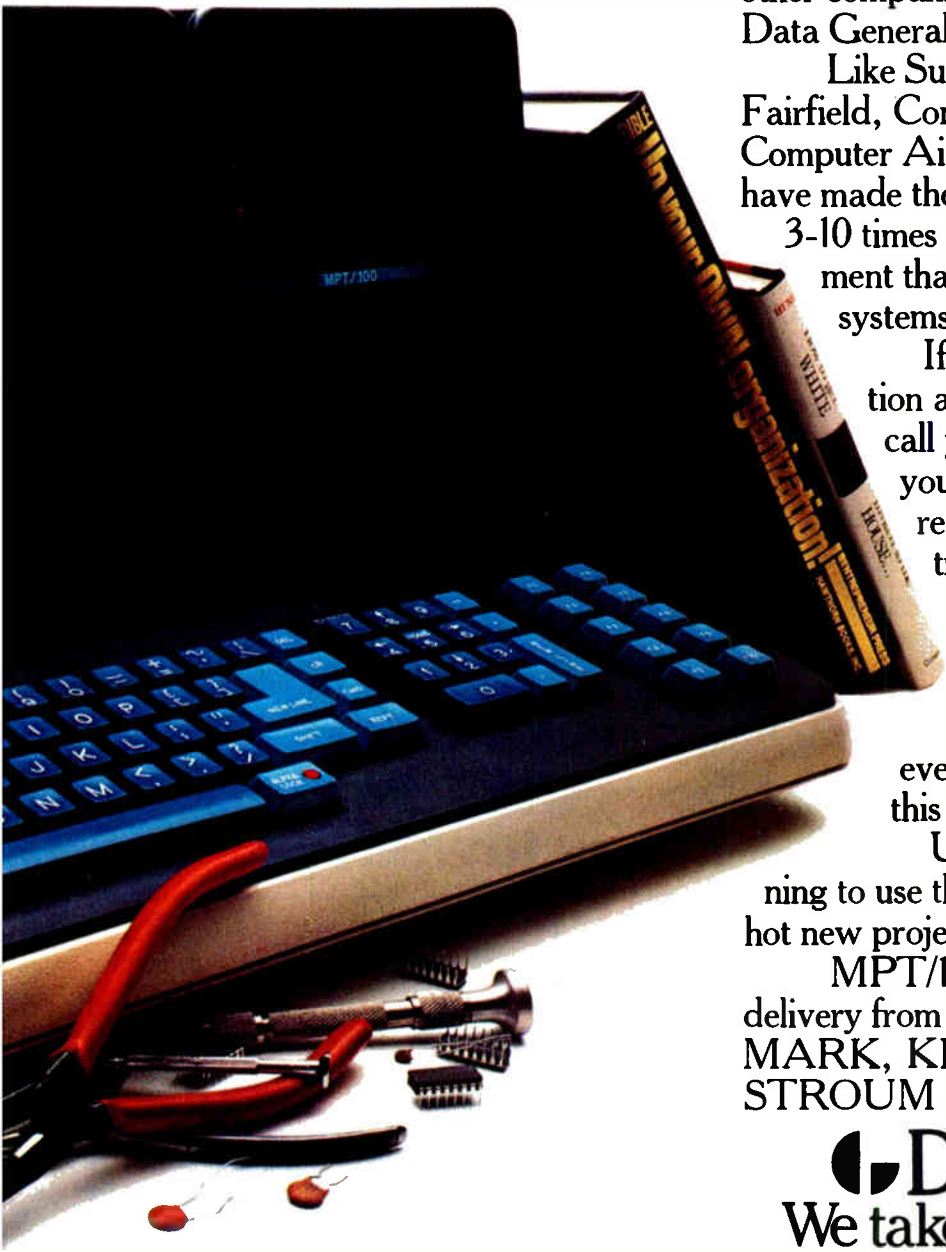

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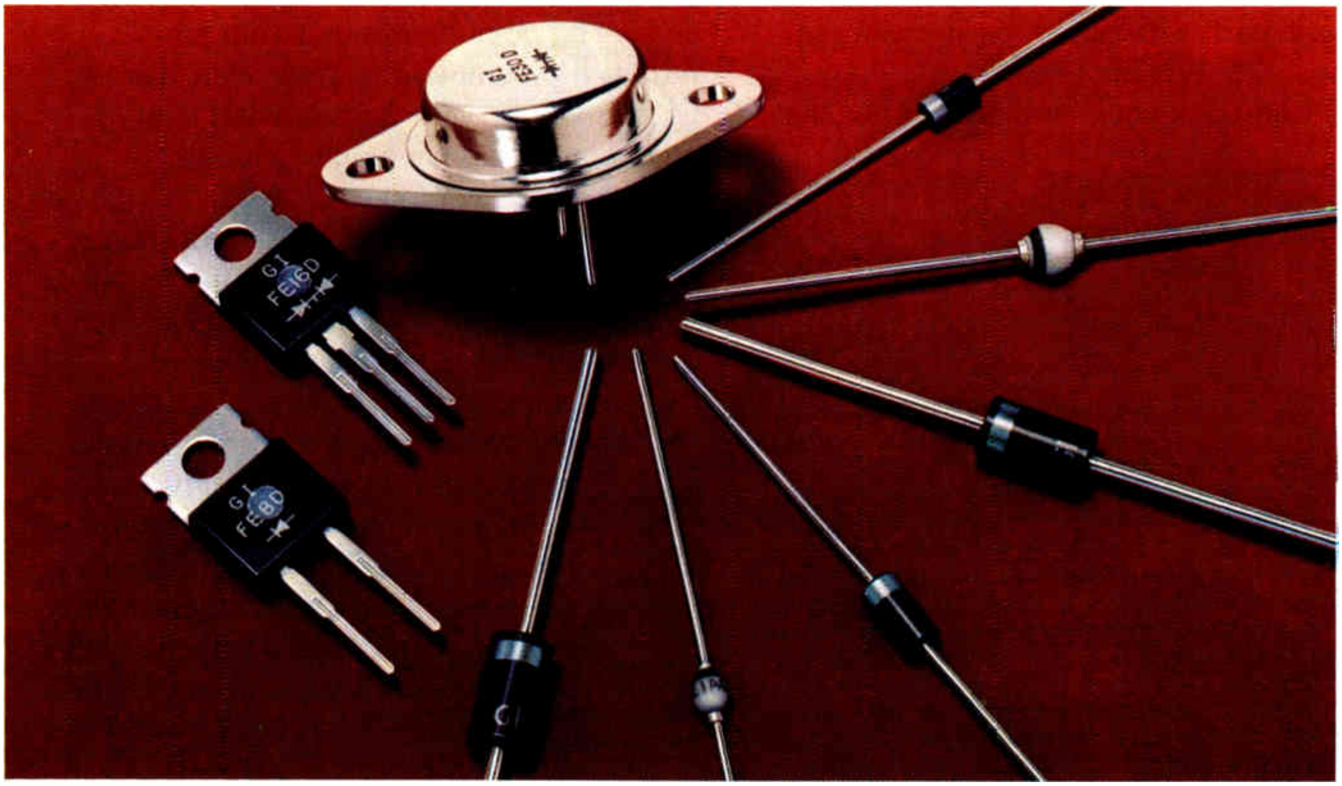

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GENERAL INSTRUMENT

Circle 154 on reader service card

Emulator links to personal computer

$1,495 5-MHz in-circuit emulator with full set of features works with Apple II and Intel development systems

by Martin Marshall, San Francisco regional bureau

As the personal computer has begun to do, an inexpensive in-circuit emulator may foster another cottage industry. The Apple II made it economical for the professional to bring computing power into his house; but the professional electronics engineer whose pet project was to develop a microprocessor-based system would be stymied because he still lacked the in-circuit emulation tools to marry his software ideas to his breadboard prototype—until, that is, the introduction of a truly low-cost 8-bit emulator unit from a Taiwan-based company.

The company is MicroTek International of Hsinchu, Taiwan, which has established a U. S. marketing arm called MicroTek Lab Inc., located in Gardena, Calif. The firm has developed a two-board slave module which sells for $1,495 and consists of a general-purpose board and a target-processor board. The processor-specific boards are currently available for the 8085A, Z80, 6502, NSC 800, 8048, 8049, and 8050, with more to follow.

The Z80A is also included, but the Z80B can only be implemented at speeds up to the emulator's limit of 5 MHz. A multiple-processor board called Micetrap is also available, with emulation boards for the 6809 and Z8000 processors and 2716, 2732, and 2764 erasable programmable read-only memories due out by the end of the year.

The use for MICE (for micro in-circuit emulator) is clearly more than as a home tinkerer's tool. Just as the home computer turned up in a large number of small-business environments, the MICE unit will find its way into a large number of price-sensitive laboratory development stations, because its feature set in many cases surpasses units costing upwards of $3,000.

One particularly useful feature is its control over direct memory access, including disabling DMA in software. Another benefit is that the target system retains full user memory and input/output spaces, which is not so with some emulators developed by microprocessor manufacturers. It also has a 32-bit-wide trace memory, which retains 256 cycles, and emulation memory of 8-K bytes of static random-access memory, not to mention an assembler, a two-pass disassembler, and control of nonmaskable interrupts, interrupt requests, and bus requests.

In addition, optional software drivers ($99 each) allow it to upload and to download to either an Apple II or an Intel series 800 or later development system. The MICE unit can also be used solely with a terminal in a setup designed for the evaluation of microprocessors.

The MICE unit lacks almost nothing but a real-time breakpoint feature. Instead, it has a software breakpoint function with a loop-counting option. It can both enable and disable traps, holds, and interrupts, as well as single-step and single-cycle the target system.

Its control processor module is run by an 8085 at 6.1 MHz, and it has from 8- to 16-K bytes of ROM and 1- to 2-K bytes of RAM, as well as an RS-232-C interface to a modem or terminal capable of running at rates selectable from 110 to 9,600 b/s. The emulation adds a target processor operating at maximum speed or at a clock speed supplied by the user, adding 8-K bytes of RAM with switch-selectable addressing and write-protection.

The MICE uses a command set consisting of any of 22 commands that are entered with single keystrokes. This includes two different download commands, one for Tektronix-format development systems and one for Intel-format development systems. It also includes a help command that prints or displays the command table as a form of self-contained documentation. Notes MicroTek Lab president Bobo Wang: "There are some super-powerful I/O commands in which a single input command can sample any port up to 256 times at intervals from 1 to 256 ms. A single output command can program the majority of LSI peripheral chips."

Delivery of the Micetrap multiprocessor module and the first batch of 8-bit processor emulators is immediate. Since MicroTek has yet to set up a dealer network, inquiries will be handled through a San Francisco-based representative.

GYC Inc., 2338 Divisadero St., San Francisco, Calif. 94115. Phone (415) 568-3720 [338]

Software aids high-tech managers

System is designed to manage complex parts inventories and simplify sales-analysis and quote-tracking tasks

by James B. Brinton, Boston bureau manager

One of the risks of high-technology ventures is the typical engineer's lack of management ability. Venture capitalists and entrepreneurs will thus be glad to know that now there is software available that can help compensate for this weakness, whether in new or existing high-technology firms.

The FM/3000 manufacturing control and accounting system from Computer Solutions Inc. is specifically slanted toward the problems of high-technology managers. It is a data-base-oriented system running on Hewlett-Packard's 3000 series of minicomputers. Priced at $35,000, it includes vendor-performance, purchasing-analysis, purchasing-order, inventory-control, and manufacturing-resource-planning modules as well as the typical accounts-payable and -receivable and general ledger subsystems. There also are sales-analysis and quote-tracking modules.

"What we offer that our competition does not," says Mitchell E. Kertzman, president of CS, "is the sort of software that high-tech firms need. General-purpose management software is either too slow, cumbersome, or just doesn't pay attention to their special needs"—techniques for coping with hot competition, long lead times, short product lifetimes, frequent technological change, and dramatic growth.

FM/3000 is tailored for use by people unfamiliar with data processing. It is menu-based and prompts users to the needed files; its help function bails out users if the software asks questions they cannot answer; its browse function opens files and lets users scroll through records alphabetically or numerically; finally, there is a document generation system that lets users select the type and the sorting criteria of data and generate reports almost instantly.

Inventory rigor. FM/3000's inventory management approach may strike the most resonant chord with electronics businessmen. Kertzman describes it as a method of "enforcing rigor in the engineering and manufacturing departments without loss of freedom—a good way to prevent needless inventory growth. Often, engineering will order materials that may be in stock but hard to locate. There is also a tendency to order parts very similar to other parts. Both actions can drive up inventory and stocking costs."

With FM/3000, instead of consulting a parts book that may be out of date, an engineer can consult a display terminal and browse through the list of parts in stock by category. Stock is entered in the FM/3000 data base upon acceptance, and key electrical parameters are noted.

Inventory projections are a keystone of manufacturing management and cost control. The FM/3000 package includes routines that take either marketing's or manufacturing's estimates of units to be sold or produced, refer to stored bill-of-materials data for these units, and then forecast parts usage rates and reorder times.

The explode function takes product forecast data and a bill of materials, generating a list of parts needed for, say, a year's production. The simulate function forecasts parts needs based on rates of use and lead times for delivery; it also refers to the bill of materials.

A vendor file tracks past delivery performance, duration, promptness, and the proportion of parts rejected at incoming inspection. All this data, plus the output of the explode and simulate functions, produces a statistically honest forecast of lead time between a purchasing order and receipt of sufficient materials for production needs. From this point, it is a short step to semiautomatic purchase-order generation.

Most systems for manufacturing resource planning force firms to enter parts in inventory before trans-

Modularity eases transition

Because of its modularity, the FM/3000 high-technology management software can be brought on line without inconveniencing the company it is supposed to help. The first step usually is entry of inventory data and can take one to two weeks for smaller firms; this allows the resource-planning function to begin operating, however, and gives managers control that can gradually be extended to the rest of the organization.

Although the modules are available separately, their total cost would be about $60,000. However, for $85,000 total, Computer Systems will deliver a complete hardware-software system with an HP 3000-40 minicomputer, HP 2622 display console, printer, a 67-megabyte Winchester storage with streaming-tape backup, and FM/3000 software.

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DOLCH
LOGIC INSTRUMENTS

Circle 157 on reader service card

fer to incoming inspection. But FM/3000 considers parts available from stock only when they have passed incoming testing. Parts in test are noted in the data base and, if urgently needed, FM/3000 flags management that incoming tests should be rescheduled.

According to Kertzman, high-technology firms tend to order materials for billing directly to work in progress, but ordinary purchasing-order software does not account for this. With FM/3000, users can order for billing to inventory, a work or job order, or a general ledger account.

The data base can be oriented to bills of materials as well, yielding ones like those used by engineering as part of a product description. "Having this BOM-handling function," says Kertzman, "saves time that would otherwise be spent re-creating similar BOMs and justifying them with other departments."

Quote tracking. With the FM/3000's price-quote tracking and sales-analysis routines, sales people's performance can be analyzed relative to the market, other territories, to each other, and so on. Quotes can be watched from the arrival of a request for a quote and the company's response to it and can be continually monitored and categorized as pending, won, lost, or abandoned.

FM/3000 is so comprehensive, feels CS vice president David DeWan, that if managers keep its data base current and frequently check the reports displayed by the system on a cathode-ray tube, their course of action should be obvious.

The system's ancestors have been evolving since 1974, largely in response to requests for specific functions from high-technology users. CS's customer list includes GTE, Data General, and Foxboro. "They have used the system for some time," says DeWan, "and their suggestions have shaped it." Now CS is moving out of the custom software business and into the merchant market with FM/3000. It is available for immediate delivery.

Computer Solutions Inc., 950 Watertown St., Newton, Mass. 02165. Phone (617) 332-1300 [339]

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For more information, contact Fairchild Test Systems Group, 1601 Technology Drive, San Jose, California 95115, (408) 998-0123, Ext. 2294. Fairchild Camera and Instrument Corporation.

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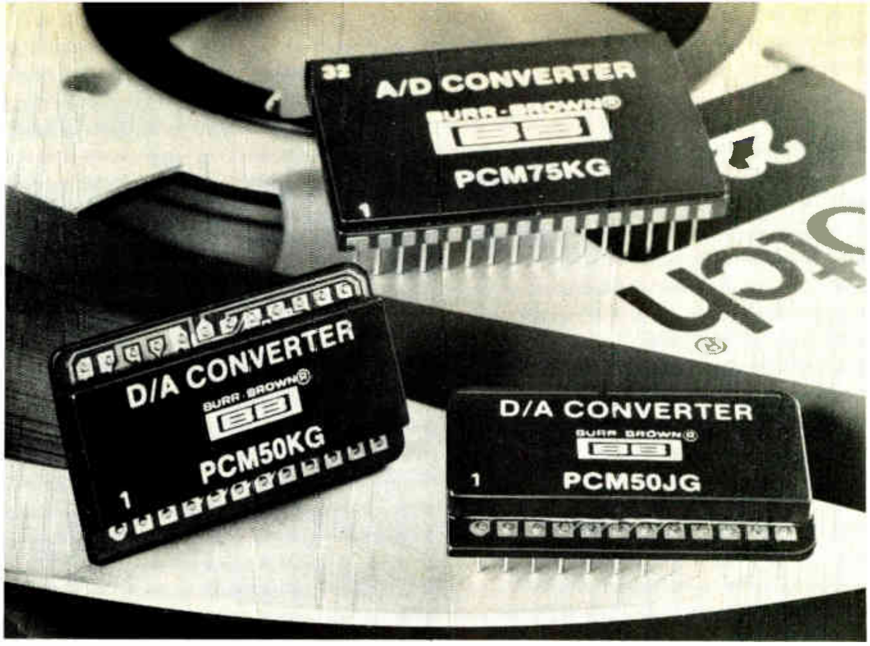
Components

16-bit converter adds little THD

Digital-to-analog hybrid settles in 5 μs for use in stereo equipment



With the pulse-code modulation formats of new-wave digital audio systems demanding better converter performance, Burr-Brown Research Corp. is responding with products to fill this need. The firm's PCM50KG 16-bit, hybrid digital-to-analog converter has a rapid 5-μs typical settling time.

Most applications of the PCM50KG d-a converter will be in studio equipment, predicts Clay Tatum, director of corporate planning. But since it can also operate with a 14-bit resolution, the single-package hybrid should find uses in stereo units, too.

Although some hybrid and monolithic 16-bit d-a converters are currently available, they need an external voltage reference, operational amplifiers, or buffers, which drive up prices, according to Tatum. "Burr-Brown just now has reached the point where a single-package DAC can be built for less," he says. The price of the PCM50 is $49.95 in lots of 100, with delivery from stock or within three weeks.

A fast settling time is important for stereo systems where multiplexing between channels requires at least 8-μs speed. Furthermore, the PCM50 has a wide dynamic range of 96 dB and 0.003% total harmonic distortion (typical) at full-scale range. Maximum distortion is only 0.02% at −15 dB. (Both specifications have a 16-bit resolution; a 14-bit resolution results in slightly higher distortion.)

Other key specifications include typical differential linearity of 0.0015% of full-scale range and typical drift of ±25 parts per million of full scale per °C. Warm-up time is a minimum of 1 minute.

The PCM50 is the second in Burr-Brown's conversion product line for digital audio systems, following the PCM75 analog-to-digital converter [*Electronics*, Sept. 22, p. 246]. In addition to professional recording and stereo equipment, the converters are suitable for industrial vibration-analysis measuring equipment as well as sonic, sonar, and acoustic instrumentation, according to the company.

The PCM50 converter contains an internal voltage reference, comes in a ceramic package, and weighs 8.4 g. It is compatible with the Electronic Industry Association of Japan's specifications for audio systems (EIAJSTC-007).

Burr-Brown Research Corp., P. O. Box 11400, Tucson, Ariz. 85734. Phone (602) 746-1111 [341]

650-V transistor integrates diode

Three 15-A bipolar devices and a fast 5-A, 1,000-V unit added to Switchmax line

The growing popularity in Europe of single-transistor forward-converter designs for switching power supplies is creating a hole RCA will attempt to fill with high-voltage additions to its Switchmax line of bipolar transistors. Just announced are the 2N6754, a fast npn transistor rated at up to 1,000 V that conducts 5 A with a maximum saturation voltage of 1 V, and the 2N677-4, -5, and -6, a series of 15-A parts with integrated commutating diodes and base-emitter resistors.

Although many power MOS field-effect-transistor makers are at or near the 1,000-V benchmark, none can offer the 150-W dissipation and $5.15 price tag (in 100-unit lots) of the 6754. And, according to Frank J. Rohr, power devices marketing manager, "RCA's marketing force in Europe has identified a strong and growing need for this kind of part." Along with the high-voltage capability, the 6754's 0.5-μs turn-on time and 3.4-μs turn-off time will allow it to be used in switching power supplies and motor controllers operating from 240-V power mains.

Pushing bipolars to the 1,000-V level is mostly a matter of passivation technology, but beyond that point speed would be degraded. "For the moment," says Rohr, "further transistor development is aimed at higher currents—higher-voltage parts will be turning to thyristor structures."

Meanwhile, the 6774 series is offering cost and performance advantages in the 450-to-650-V range by incorporating antiparallel diodes in the transistor structure, a move often seen in power Darlington design. This is accomplished by

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allowing the emitter metalization to contact the base region. Base drive current is not shunted by this short circuit, because it flows through a 100-Ω diffused resistor and the active base region before reaching the short. Such a diode is necessary in many switching supplies and motor controllers to shunt current stored in inductive loads. Because the diodes do not require extra space, the cost of an additional component and board space is saved.

The elimination of parasitic wiring inductance can make a difference in reaching switching frequencies over 40 kHz. Furthermore, the base-emitter resistor allows easier parallelling of several transistors, by relaxing the requirements on base-emitter junction matching.

The 6774 is priced at $5.90 in lots of 100. Delivery on both the 6754 and 6774 is from stock.

RCA Solid State Division, Route 202, Somerville, N. J. 08876. Phone (201) 685-7102 [342]

Isolation amp settles in 200 μs

Transformer-based module has 30-kHz bandwidth, isolates up to 3,000 V

Though the IA194 isolation amplifier uses transformer isolation, it is more than a match for usually faster optically isolated parts, maintains Richard Beede, vice president of engineering at Intronics Inc. The module has a bandwidth of 30-kHz and a specified 200-μs maximum settling time.

"Running the unit's transformers in a current mode rather than the more usual voltage mode gives us nearly twice the bandwidth and half the settling time we'd normally expect from this part," notes Beede. The one tradeoff, he admits, is a lower level of common-mode rejection; the ratio is 90 dB, about 30 dB less than that obtainable in voltage mode, but still sufficient for many multichannel data-acquisition and process-control applications demanding the IA194's high speed and stability.

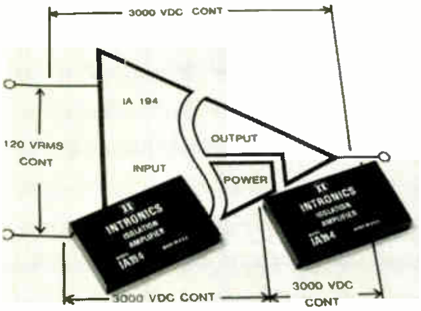
The IA194 affords three-port isolation—between input, output, and the internal floating power supply—to 3,000 V. Nonlinearity, typically 0.05% of full scale for a ±10-V output at 5 mA, is 0.1% maximum. Relative accuracy, including all offset, temperature, and nonlinearity effects, is ±0.5% maximum over the full operating range of 0° to 80°C. Stability over temperature is particularly good at 0.005%/°C.

Offset and noise. Initial offset voltage at unity gain is ±10 mA maximum, and is externally adjustable to zero. Offset voltage drift over temperature is to within ±100 μV/°C maximum. Input-difference current noise at 25°C typically is 10 nA (70 nA is maximum). An input voltage noise of 10 Hz to 1 kHz is a maximum 3 μV, and input current noise 40 pA peak to peak.

The IA194 has an externally programmable gain of up to 1,000, as well as external synchronization of an internal oscillator used for input isolation. An oscillator providing modulation and demodulation is also triggered externally to eliminate beat-frequency effects on the output signal. The unit is powered with 80 mA at 11.5 to 12.5 V dc.

Packaged in a 0.55-by-2.27-by-3.6-in. module, the IA194 is priced at $119 in lots of one to nine, with quantity discounts available. Delivery is from stock or up to six weeks.

Intronics Inc., 57 Chapel St., Newton, Mass. 02158. Phone (617) 964-4000 [349]



N-MOS reduces multiplier cost and power consumption

The performance of Weitek's n-channel MOS 16-by-16-bit parallel array multiplier design rivals that of bipolar TTL multipliers, yet it consumes half the power and sells for a third as much. The WTL1016 uses a modified Booth's algorithm and advanced n-MOS very large-scale integration to combine high performance with a low 2-W power consumption, compared with 4 W for the bipolar device.

Easier to construct and having a smaller die size (160 mil² compared with 200 mil²) than a bipolar device, the n-MOS device permits higher yields and lower costs, enabling a manufacturer to offer it for 30% to 50% less than the average bipolar version's $150.

The WTL1016 features input/output latches that may be operated in either clocked or transparent modes. Input data of 16 bits is accepted in 2's complement or sign-magnitude coding. The device operates on a 5-V power supply and has TTL-compatible I/O levels. The WTL1016 design is available under a design-licensing arrangement.

Weitek Corp., 3255 Scott Blvd., Building 2B, Santa Clara, Calif. 95050. Phone (408) 727-6625 [343]

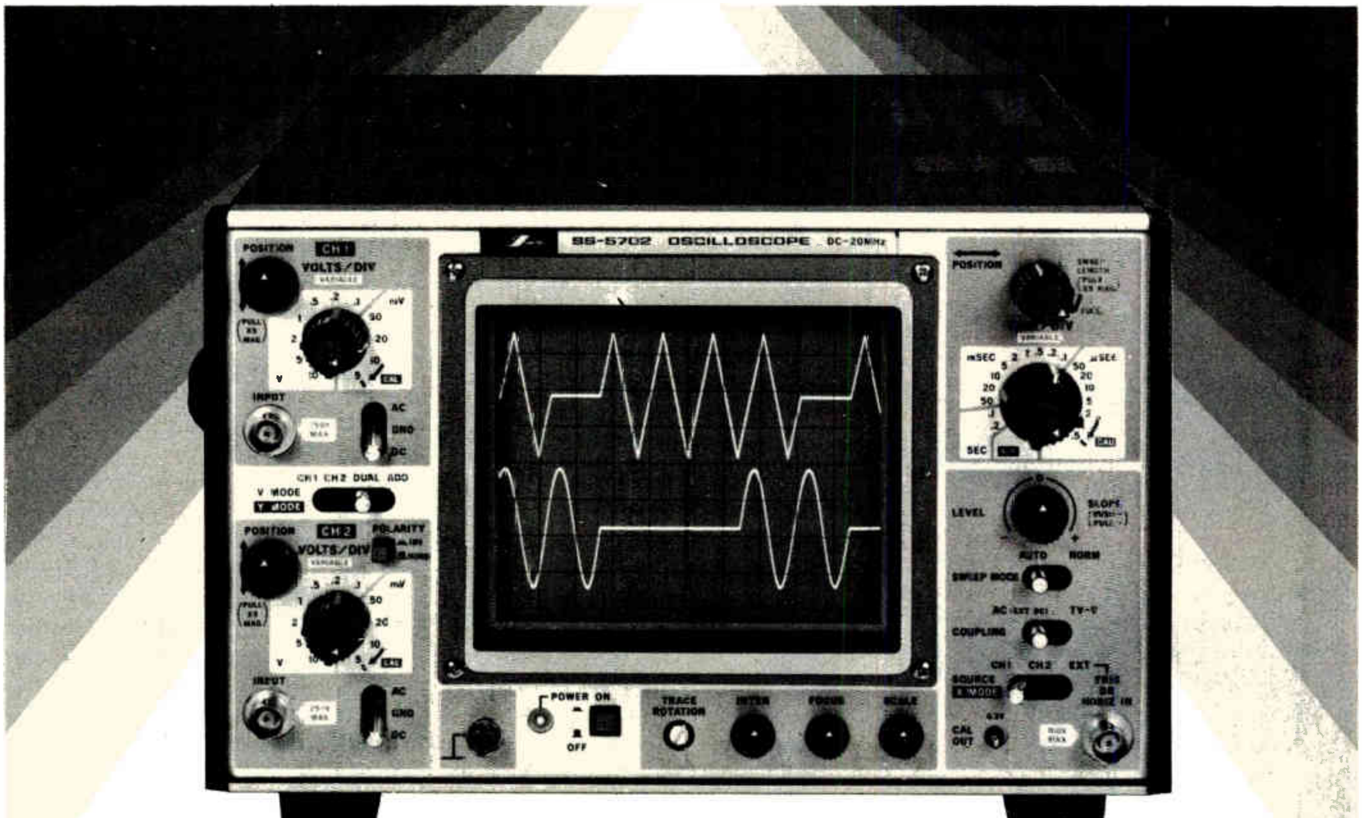
Charge-coupled device delays, stores TV signals

The MS1003 charge-coupled-device video delay line contains a 910-element analog shift register. It can store a National Television System Committee television line with a bandwidth of 5.5 MHz at a clock frequency of 14.3 MHz. It can also be used for applications requiring time delay, time compression or expansion, or analog-signal storage.

The MS1003 is available in two versions, one for delay-line applica-

AN INNOVATIVE 20 MHz OSCILLOSCOPE THAT EMPHASIZES OPERABILITY

The SS-5702 has flexibility and power which make it ideal for the maintenance and troubleshooting of TVs, VTRs, audio equipment and a wide range of other electronic systems by hobbyist as well as professionals. At the top of its class, the SS-5702 uses a 6-inch rectangular, parallax-free CRT.



IWATSU
SS-5702
DC~20MHz OSCILLOSCOPE

IWATSU makes more than 20 oscilloscopes as well as an impressive lineup of other instruments including logic analyzers and digital memory scopes. The fastest oscilloscope has a maximum frequency of 350 MHz. And the same technological expertise and product quality that make this super high-frequency oscilloscope possible are incorporated in the SS-5702.

- 6-inch rectangular, parallax-free CRT
- TV-V trigger
- Variable sweep length
- Double Lissajous figure
- 1 mV/div to 10 V/div sensitivity
- 100 ns/div to 0.2 s/div sweep
- Differential input with ADD mode
- DC operation (optional)

IWATSU®

IWATSU ELECTRIC CO., LTD.
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■ Austria: Universal Elektronik Import GmbH 54 15 88 ■ Canada: Associated Test Equipment Ltd. (416) 497-2208 ■ Chile: Importadora Janssen Y Cia. Ltda. 72 3956 ■ Denmark: Danstrument aps (03) 28 34 31 ■ England: ITT Instrument Services 0279 29522 ■ Finland: Oy Etra AB 780 122 ■ Italy: Radiel Spl (02) 213.30.56 ■ Netherlands: Klaasing Electronics BV 01620-51400 ■ New Zealand: G.T.S. Engineering Ltd. 546-745 ■ Norway: Solberg & Andersen A/S (02) 19 10 00 ■ Sweden: Teleinstrument AB 08/38 03 70 ■ West Germany: NBN Elektronik GmbH (0 81 52) 390 tions and the other for analog storage. In the delay-line version, the device is clocked continuously to give a dynamic range of 60 dB. For storing analog signals, a dynamic range of better than 60 dB is achieved for a 64-μs interruption period at an ambient temperature of 70°C.

Both versions will handle maximum input signals of 1.5 V peak to peak. The MS1003 is packaged in a 16-lead ceramic dual in-line package and operates over the −55° to +70°C temperature range. In lots of 100, each device sells for $45.

Plessey Semiconductors, 1641 Kaiser Ave., Irvine, Calif. 92714. Phone (714) 540-9979 [344]

High-voltage op amps slew at 200-V/μs rate

The Apex PA84 and PA84A high-voltage operational amplifiers have a 75-MHz gain-bandwidth product and a 200-V/μs slew rate, and through provisions for external phase compensation control, their response may be optimized for each application to maximize speed.

These power amplifiers have thermally efficient beryllia substrates, thick-film resistors, silicon semiconductors, and aluminum-wire interconnections. They accept power-supply voltages ranging from ±150 to ±15 V and deliver an output voltage of up to 290 V peak to peak at load currents of ±40 mA while safeguarding their output circuits with internal over-temperature protection.

The input circuitry contains cascaded field-effect transistors for a 3-pA input bias current; the input offset voltage drifts only 5 μV/°C. Internal current limiting enables the amplifiers to withstand a short circuit to ground without causing secondary breakdown. The output transistors are biased for a continuous-on condition to ensure maximum linearity.

In quantities of 100, the PA84 is priced at $66.50 and the PA84A sells for $77.50. For small quantities, delivery is from stock, but production quantities may take eight weeks.

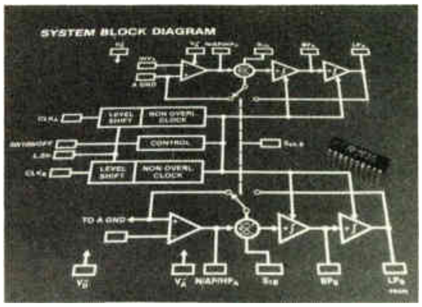
Apex Microtechnology Corp., 1130E East Pennsylvania St., Tucson, Ariz. 85714. Phone (602) 746-0849 [345]

Monolithic filter fixes center frequency within 0.6%

No external capacitors are needed to operate the MF10 monolithic filter, which is designed for telecommunications, signal-processing, audio, and instrumentation use. Unlike most other filters, whose center frequencies are adjusted by external resistors or capacitors, the MF10 has center frequencies of various second-order functions that are directly proportional to an external clock frequency and are fixed to an accuracy of within 0.6%.

The gain and filter selectivity are adjusted by external resistors. Because capacitors are eliminated, only minimal tuning of a center frequency, which may reach 20 kHz, is required. The clock is the only other external component necessary; it can drive an unlimited number of filters. The dual MF10 comes in a 20-pin molded package for $3.70 in 100s.

National Semiconductor, 2900 Semiconductor Dr., Santa Clara, Calif. 95051 [346]



Transducer converts pressure directly into current

Micro Switch's piezoresistive transducer converts pressure proportionally into current instead of voltage. It operates in the 3- to 15-lb/in.^{2} range and produces a 4- to 20-mA output.

The two-wire 149PC is a hybrid

16-bit software just caught up with 16-bit hardware.

A better marketing tool. Whether you're developing multi-tasking, multi-user, or networked systems, the XENIX™ operating system helps you get the most from your 16-bit product. XENIX' portability frees you from dependence on a single hardware source. XENIX' universality puts your product into more applications. And XENIX' high level language support cuts system development time for you and your customers. With XENIX, you're into more markets faster. With a better product.

Setting the standard. XENIX is Microsoft's implementation of the UNIX* operating system. It's a multi-tasking, multi-user OS for leading 16-bit microprocessors. In fact, XENIX is such a productive, portable system, that we expect it to become the de facto standard operating system for 16-bit microprocessor-based systems. A standard that will foster the development of applications programs that sell systems.

Support. XENIX is fully supported by Microsoft. In developing XENIX for 16-bit microprocessors, we improved the efficiency of the UNIX operating system. Then, we added enhancements specifically designed to make the system suitable for the commercial marketplace. You can create a total environment by adding Microsoft's standard software packages to the XENIX operating system. In languages, Microsoft's BASIC Interpreter and Compiler, FORTRAN, COBOL, and Pascal provide unique program portability between 8-bit and 16-bit systems. And, Microsoft is the single-source vendor for the XENIX operating system, languages and utilities. In addition, Microsoft's XENIX Clearinghouse will provide access to a library of XENIX applications software and utilities.

Want to know more? If you are developing a 16-bit microprocessor-based system, contact us. We can offer you single copy XENIX through our distributors, or, multi-copy XENIX with a low initial payment and a pay-as-you-sell OEM royalty program. To open a dialog, return the coupon below.

*UNIX operating system is a trademark of Bell Laboratories
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☐ PDP-11, ☐ Z8000, ☐ 8086, ☐ 68000.

I'm specifically interested in ☐ single copy, ☐ multi-copy OEM use.

☐ Please include information on the XENIX Clearinghouse.

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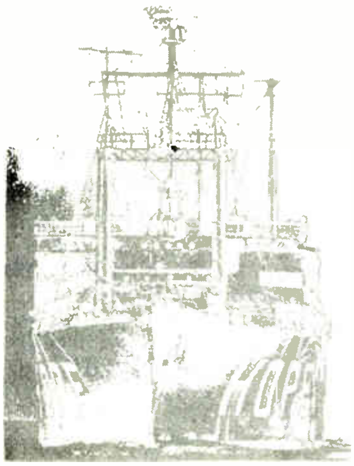
Company ____________

Address ____________

City ____________ State ____________ Zip ____________



integrated circuit and has a 1-ms response time. The heart of the sensor is a 0.1-in.^{2} silicon chip. A sensing diaphragm is etched into the chip, and resistors are ion-implanted in the diaphragm. Pressures applied to the twin ports of the transducer cause the diaphragm to flex and the values of the resistors to change, producing a current output that is proportional to the change in pressure.

Computer-controlled laser trimming of the thick-film resistors on the substrate ensure exact temperature compensation and precise end points for pressure range. Temperature error is ±1% of full-scale output over 0° to 50°C. The 149PC can sustain an overpressure of 50 lb/in.^{2}, and test units have withstood severe shock and vibration. The small plastic-packaged device will sell for under $100. Samples will be available this month.

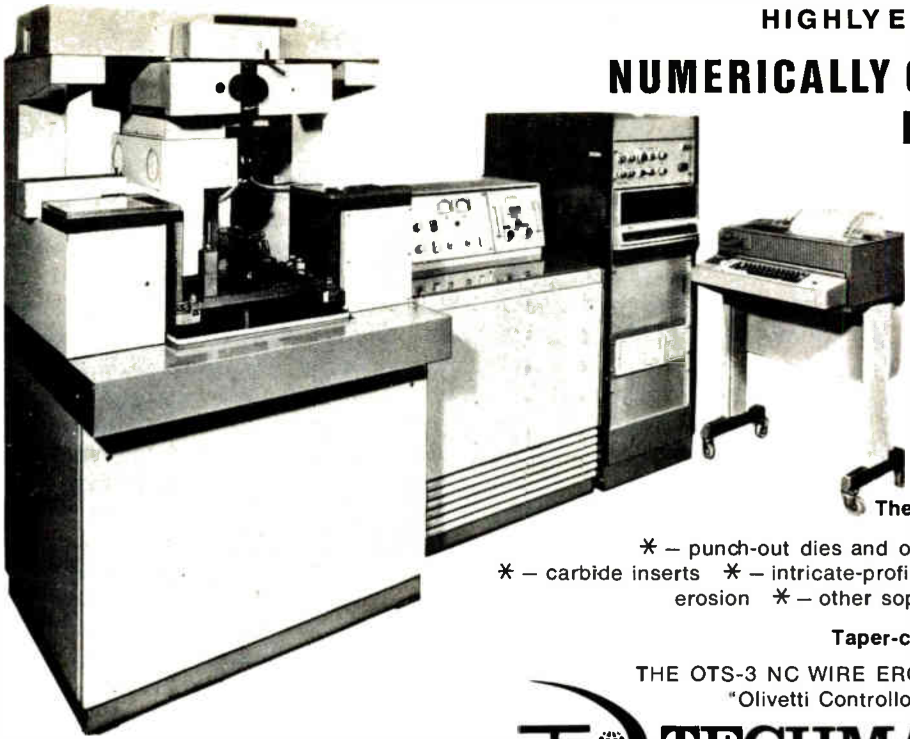
Micro Switch, 11 West Spring St., Freeport, Ill. 61032. Phone (815) 235-6600 [347]

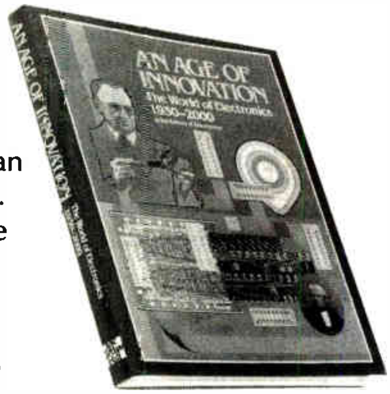
Applied voltage shifts microcircuit's phase ±600°

The Tau Tron PL-204M voltage-controlled microcircuit provides an output that can be shifted in phase over a range of ±600° with respect to the input clock. The unit operates over a frequency range of 50 to 200 MHz and gives continuous control over the phase shift with resolutions better than 20 ps.

The PL-204M is a three-terminal device using a phase-locked-loop approach to achieve its excellent linearity, stability, and edge-control accuracy. A hybrid circuit in a 24-pin dual in-line package, it is suitable for applications where precision high-speed delay and width control are required, as in p-i-n electronics, timing generators, and format converters. The unit is priced at $369 for single units with significant discounts for larger quantities. Delivery of the device takes 6 to 10 weeks after receipt of order.

Tau-Tron Inc., 27 Industrial Ave., Chelmsford, Mass. 01824. Phone (617) 256-9013 [348]





AN AGE OF INNOVATION

Instruments

Family grows for C-MOS testing

Extended voltage range of drivers and dual comparators let IC testers handle C-MOS

In a major upgrade of its two-year-old Q2 family of integrated-circuit test systems, Megatest Corp. has produced a software-compatible second-generation family. On the outside of the systems, the new family merely adds a 2 to the model number, changing the Q2/20, Q2/40, and Q2/60 to the Q2/22, Q2/42, and Q2/62 read-only memory, random-access memory, and large-scale IC tester, respectively.

Internally, the new family provides an extended voltage range that allows the systems to test complementary-MOS as well as hybrid devices. They now have dual comparators, which allow testing against both high- and low-voltage tolerances on a single pass. They have a faster computer that reduces test time; wafer mapping and shmoo plots to enhance process control; software-aided calibration; and a deskewing process that includes both edges of the window strobe.

The voltage levels of the drivers range from −1.5 to +7.0 V and those of the comparators are from −1.5 to +5 V, compared with 0 to 5 V for both drivers and comparators on the previous Q2 systems. This allows testing of the class of C-MOS circuitry in the 5-to-7-V range and more effective testing of TTL RAMs. The dual comparators may be set for both high and low voltage-output comparisons in one pass, doubling throughput relative to the single comparator on previous Q2s.

All Q2 systems are controlled by several distributed microprocessors, and the change from an 8080 to an 8080A-1 in the new series has resulted in a change from a 1.6-MHz clock to 2.6-MHz one on the system controller. This difference causes a corresponding increase in the execution rate of individual instructions.

The net result is a 40% reduction in the time required for mainframe operations. The drive and compare circuitry, on the other hand, can reach speeds up to 8 MHz for the Q2/20 and /22 ROM testers and Q2/40 and /42 RAM testers, while the Q2/60 and /62 LSI testers can reach 10-MHz speeds.

Two new commands in the vocabulary of the Q2 family make it easier to generate and store programs for microcomputers with on-board ROM. The command DEXLPP removes redundancies by isolating the parts of the test program that are unique in order to store the program in compact files. The BEXLPP command reinserts the unique data into the common functional sequence upon execution.

Two more new commands allow the disassembling of object code into high-level source statements, so that the test programmer can more easily analyze a device-under-test operation. These statements can be displayed and edited interactively, and the editing does not require recompilation of the test program.

Wafer maps or shmoo plots are also possible on the new systems through the creation of a tester-to-prober interface that uses two sets of up-down counters and prober signals for directional control and clocking. This creates an X-Y coordinate system for identifying die locations and for correlating them with test parameters such as leakage currents and temperature gradients.

Interactive calibration. Calibrating the test system is also made easier in the new family through a calibration control language that tells the user where to place probes and then makes the measurement automatically. In the deskewing procedure, the user is told which trimmer potentiometer to tweak. The deskewing process itself, one of the most crucial in test systems, is expanded in the new generation to include the trailing as well as the leading edge of the window strobe.

Delivery of the new family is immediate. The Q2/22 is $75,000, compared with $68,000 for the Q2/20. The Q2/42 is priced at $65,000, compared with $58,000 for the Q2/40, and the Q2/62 is $95,000, compared with $79,000 for the Q2/60. Host computers, which can each handle four test stations, are $31,500 for the /20 and /40, and $63,000 for the /60 series.

Megatest Corp., 3940 Freedom Circle, Santa Clara, Calif. 95050 [351]

Unit develops bit-slice, MOS microprocessors

Working with single or multiprocessor systems that can contain mixed bit-slice and single-chip MOS processors, the Step-4 microprocessor development system can independently control, examine, and monitor the internal states of each processor as well as interrogate and modify control registers of other large-scale integrated circuits within the microcomputer. It can debug both types of processors simultaneously.

With the system's dual independent logic analyzers, the designer can trace the path of execution of each processor and the data flow between processors. The trace option captures 250 words by 32 or 80 bits of processor information synchronously with respect to system clocks

High-performance additive.

Now, capture 20 kHz waveforms with a direct-writing recorder.

Our new waveform storage module lets you increase the frequency response of your Gould recorder to 20 kHz. Lets you selectively capture 20 μ sec. transients. Gives you high-quality records for as little as 2¢.

And it delivers the best hard-copy waveform in the industry. Better than more traditional waveform recording techniques such as scope and camera, or light-beam recorders. High frequency events are reproduced without distortion, attenuation or loss of quality. Plus, you get a crisp, clean permanent trace in 10 seconds without development time or fixing. And, no more fussing with film loading or camera/intensity settings.

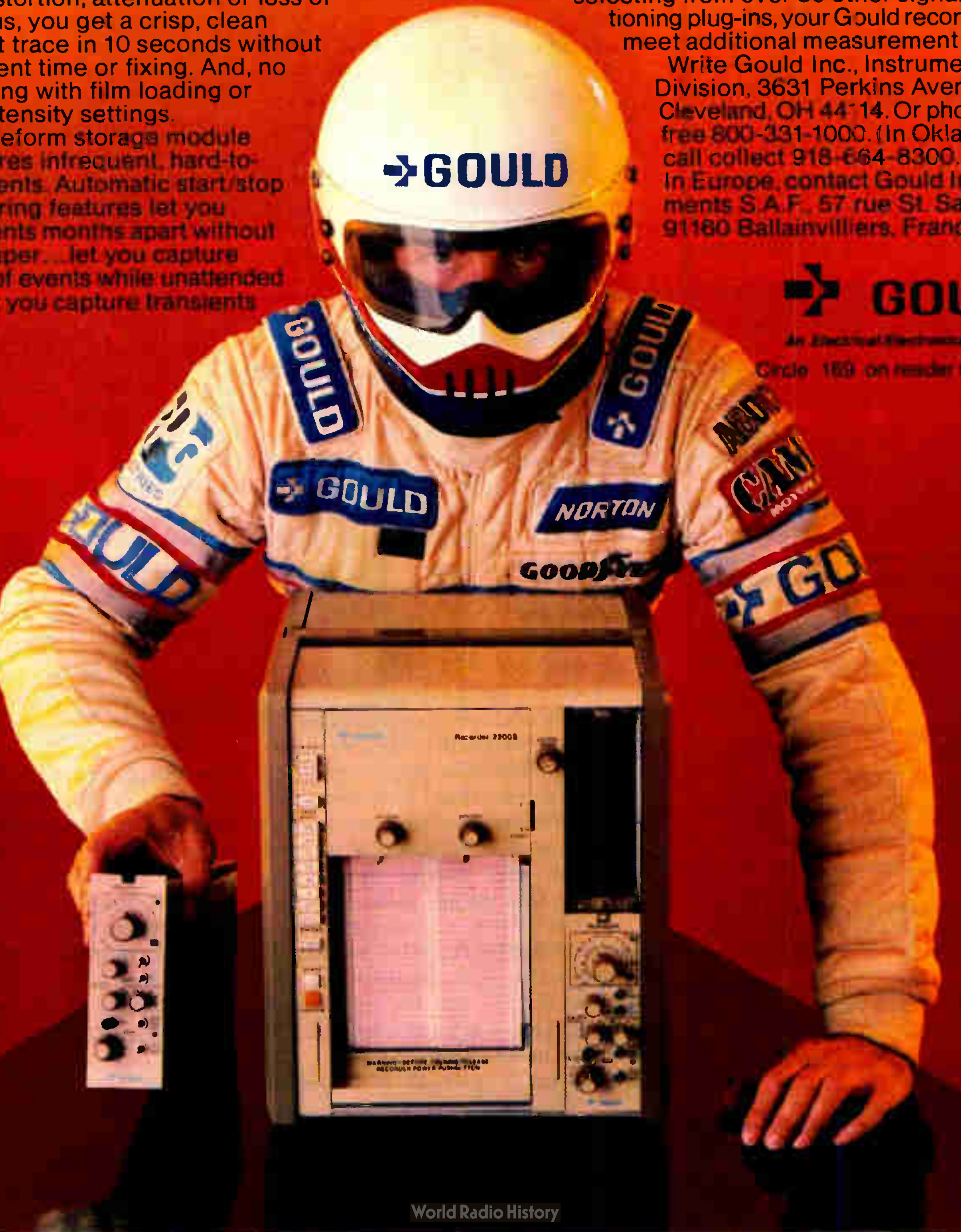
Our waveform storage module also captures infrequent, hard-to-find transients. Automatic start/stop and triggering features let you record events months apart without wasting paper... let you capture hundreds of events while unattended ... even let you capture transients buried within periodic waveforms. All made possible by our easy-to-operate features such as calibrated level triggering, selectable frequency triggering, pre-trigger viewing, window triggering, and more.

Find out how the new Gould storage module coupled with a Gould 2000 Series recorder gives you a total recording system: A waveform recorder. A transient recorder. A real time recording system. And, by selecting from over 30 other signal conditioning plug-ins, your Gould recorder can meet additional measurement needs.

Write Gould Inc., Instruments Division, 3631 Perkins Avenue, Cleveland, OH 44114. Or phone toll-free 800-331-1000. (In Oklahoma, call collect 918-664-8300.) In Europe, contact Gould Instruments S.A.F., 57 rue St. Sauveur, 91160 Ballainvilliers, France.

The Gould waveform storage module gives you...

- 20 kHz frequency response
- 2K of memory
- 10 bit A/D converter
- 100 mV to 1500 V full scale sensitivity
- For use with 1 to 8 channels
- Equivalent chart speed—to 100 meters/sec.



GOULD

Circle 169 on reader service card

the HP8350A microprocessor-based sweep oscillator, using the HP83592A 10-MHz-to-20-GHz radio frequency plug-in as its test signal source; the HP8410 microwave network-analyzer system with a specially configured 500-MHz-to-18-GHz reflection transmission test set for signal separation, detection, and analysis; and the HP85F desktop computer as the system controller, data collector and processor, and display unit.

Typical measurement ranges for the HP8408A are 60 dB for transmission and 50 dB for reflection.

The complete system is priced at $60,000, with delivery in 16 weeks. Optional variations are available.

Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, Calif. 94304. Phone (415) 857-1501 [356]

110-GHz network analyzer runs under computer control

The 4788XH computer-controlled millimeter-wave test system measures return loss, insertion loss, and gain over full waveguide bandwidths of up to 110 GHz with a 0-to-25-dB measurement range. An optional automatic control sets the frequency of the test generator to an accuracy within ±0.01%.

The automatic network analyzer includes the Hughes 4772XH millimeter-wave sweep generator; a Hewlett-Packard HP85 computer; a full-band reflectometer with 40-dB directivity couplers and calibrated standard; and an analyzer with built-in display. The sweep generator, with the new HP8350A mainframe and high-resolution digital displays, gives total computer control of all front-panel function settings. The sweeper comprises a sweep source, leveling loop, and sweep plug-in and makes all features of either mainframe available over full bandwidths through 100 GHz.

Prices begin at $45,625, and delivery takes 120 days.

Hughes Aircraft Co., Electron Dynamics Division, 3100 West Lomita Blvd., Torrance, Calif. 90509. Phone (213) 517-6400 [357]

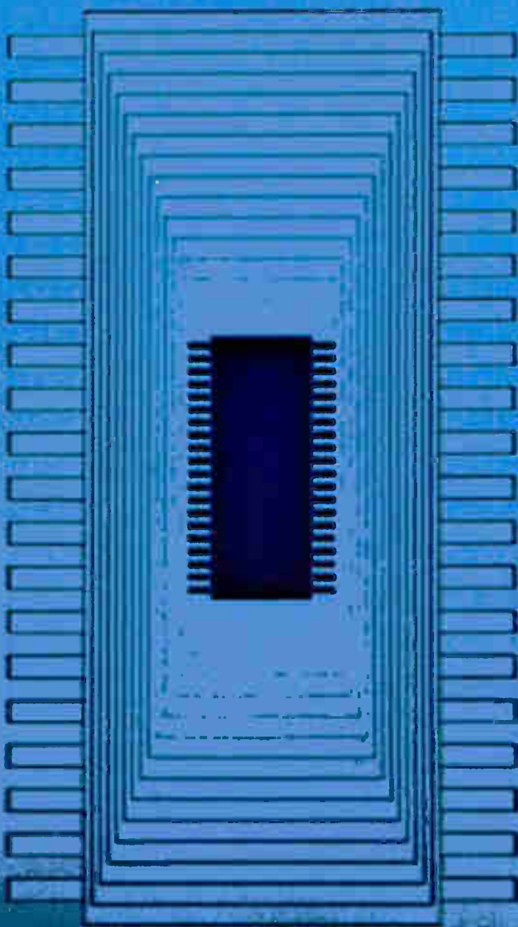
Now! One-chip microcomputers offer R6500 performance.

Presenting the Rockwell R6500/1 series: single-chip, 8-bit microcomputers and microcontrollers that are software compatible with the R6500 family, provide fast execution speed and may be interfaced readily with all R6500 I/O and memory devices.

R6500/1 features include 1.5K to 3K bytes of ROM, 64 to 192 bytes of RAM, 23 to 56 I/O ports, multiple use counter/timers, serial communication port, bit manipulation, expansion bus, multiple bus interface, directly executable RAM with low power standby, and multiple interrupts.

Rockwell. Your systems source.

To facilitate system and program development, Rockwell supports the R6500/1 series with emulator devices and interface lines to external memory, plus evaluation modules. One R6500/1 even is available as a back-pack emulator that accepts PROMs or ROMs in an on-chip socket. Additionally, the SYSTEM 65 microcomputer development system with R6500/1 personality module supports full-up hardware and program development, as well as in-circuit user simulation. Call Rockwell International toll free at 800-854-8099 (within California, 800-422-4230). Or write: Rockwell International, Electronic Devices Division, RC55, P.O. Box 3669, Anaheim, CA 92803.



Rockwell International

...where science gets down to business

Circle 173 on reader service card

R6500/1

Communications

Audio digitizer samples at 50 kHz

16-channel system is useful in digitized-speech research and other acoustic work

Digital Sound Corp.'s DSC-200 audio data-conversion system is an integrated computer peripheral system for speech and acoustic research, professional audio, and computer-music applications. It features multichannel analog-to-digital and digital-to-analog conversion capability together with support circuitry in a rack-mountable enclosure.

The system's modular design allows a multitude of system configurations to be built from the available components. For example, up to 16

a-d or d-a conversion channels with filters, in any combination, may be supported. A cable length of up to 200 ft can be tolerated between the DSC-200 and the host computer to provide the operator with a quiet recording or listening environment.

The 200 is designed to end the problem of high-performance data conversion in a computer-based laboratory, studio, or audio production facility. Its 16 channels can each be sampled simultaneously every 20 μs with 16 bits per sample for a 12.8-Mb/s data rate. Its frequency range covers 20 Hz to 20 kHz. There are up to three programmable passive elliptic-function filters per converter channel. Total harmonic distortion is but 0.1% with a 1-kHz input at 4 dBm. Crosstalk at the same test frequency is −75 dB.

The DSC-200 interfaces with a PDP-11 or VAX computer from Digital Equipment Corp. by way of the DMA11, a direct-memory-access controller. The DMA11 has two boards that plug into the standard peripheral controller slots of a PDP-11. The controller provides for half-duplex (record or play) data transfer with full-duplex operation (simultaneous record and play) possible with two controllers.

The controller, which has the base address and interrupt vector defined by on-board jumpers, contains registers for command and status, word count, and data. A second memory-array descriptor may be held in an 18-bit starting address and a 16-bit block-length register. By loading these registers with the descriptor for the next memory array, the DMA11 can automatically switch from the end of one data block to the beginning of the next. The capability, called data chaining, allows an entire block time for any necessary interrupt servicing. The DMA11 connects to the DSC-200 by means of two 50-conductor flat cables.

According to DSC's president James Pelkey, the 200's software support includes a package for either the PDP-11 or the VAX system and specific device drivers can be made to order. Pelkey says that almost every major player in the speech-synthesis game, including Texas Instruments, National Semiconductor, Hewlett-Packard, ITT, and Verbex, are using the DSC-200 in their investigations.

Configuration determines the price of a given system, with a typical system priced at about $17,000. Delivery is in 60 days.

Digital Sound Corp., 2030 Alameda Padre Serra, Santa Barbara, Calif. 93103. [401]

Fiber-optic splitter has less than 2-dB loss

Fibronics' optical splitter is compatible with the Hewlett-Packard product line of fiber-optic transmitters,

receivers, and connector-cable assemblies. With it, branching networks, duplex transmission over a single cable, and other multidrop network architectures can be set up.

The Fibronics model TS-HP optical splitter has built-in fiber-optic connectors as installed on the Hewlett-Packard HFBR-3001 to 3005 connector-cable assemblies. A 100-to-140-μm core-to-clad–ratio fiber with a numeric aperture of 0.3 is used within the TS-HP optical splitter. A 1:1 splitter ratio is standard, with other ratios available on special order. Excess optical losses are less than 2 dB plus normal connector losses. The model TS-HP is priced at $380, with delivery in four weeks.

Fibronics, M. T. M. Industrial Park, Haifa 31905, Israel. Phone (04) 536217/8/9 [403]

Jitter generator, receiver interfaces with CEPT, Bell

Hewlett-Packard's 3785A (CEPT) and 3785B (Bell) jitter-generator and receiver performs jitter tests to the specifications of CCITT G-series recommendation 0.171 for terminal and link equipment for characterizing and controlling jitter in digital transmission equipment.

Both instruments also have full control over the IEEE-488 interface bus and stored jitter tolerance masks to make measurements easy. When coupled with Hewlett-Packard's 3781 pattern generator and 3782 error detector and a controller, they become a powerful autotest system for error and jitter performance testing in production.

This capability lets manufacturers and operators interconnect equipment at different hierarchical levels

Our no-nonsense, low-cost circuit protector does double duty as an on-off switch, and sheds a little light on cost-cutting, too.

Designers, take note.

Heinemann puts an end to fiddling with fuses, and to the ugly-red-button syndrome of conventional circuit protection. Now, add style as well as sensible protection when you design in our new Series TX—the circuit protector that looks good enough to stay up front, and doubles as an on-off switch.

All with no hardware, for quick installation in a single panel opening.

Think about it. It probably costs less than you're already paying for the ho-hum, fuss-and-bother of the old way. Miles less if you add in inventory hassle and production time.

Clean up production. Clean up costs.

With current ratings from 2 to 20 amperes and your option of single-pole or two-pole configurations, Series TX from Heinemann cuts into your overheadaches by cutting straight into design complexity. Each pole in the two-pole TX can have a separate rating, so you can even protect an ac circuit and a dc circuit at the same time. And you stock only one component, install only one component.

Heinemann announces the end of ho-hum, high-hassle circuit protection.

Then, the optional light in the rocker has separate, isolated terminals. You can indicate power-on, or anything else—system-ready, hold, clear—any function you want.

And Series TX is UL-recognized, CSA certified, and designed to meet VDE requirements, so you can design it in right now.

Protection that makes sense.

Replacing two parts with one is design economy. Replacing a whole fistful—and cutting down on inventory, cutting down on production costs—is design brilliance. Heinemann's Series TX has everything you need to go from a ho-hum, high-hassle design to a very sunny number, indeed. Ask us about it. Request Bulletin TX-4020.

HEINEMANN ELECTRIC COMPANY
Trenton, New Jersey 08650
(609) 882-4800 • Telex 843431

Circle 175 on reader service card

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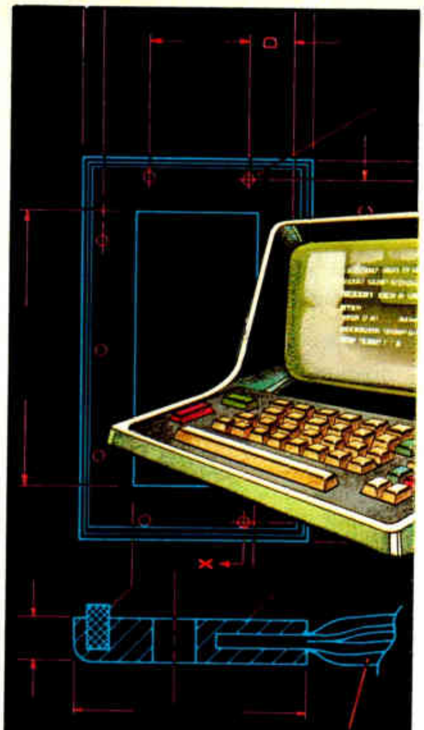
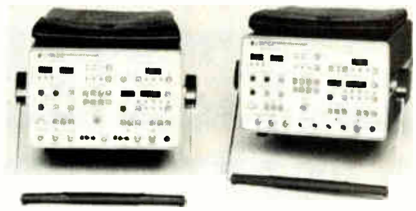


New products

to form an integrated digital network and an integrated services digital network. The 3785A is priced at $13,065 and the 3785B sells for $14,455. Delivery takes between 8 and 12 weeks.

Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, Calif. 94304. Phone (415) 857-1501 [404]



Fiber-optic video link operates over 20-Hz–10-MHz passband

The model FOL-10V wideband analog fiber-optic link for high-performance video applications can be used with all types of video signals, as well as other analog signals, within its flat ±1-dB passband of 20 Hz to 10 MHz. Its harmonic distortion is below 1% at full modulation, while its differential gain and phase are less than 1 dB and 3° respectively. Signal-to-noise ratio exceeds 58 dB at the maximum nominal length of 1,000 meters.

The transmitter module has a level control to allow proper optical modulation with inputs in the range of 0.5 to 2.0 V peak to peak, and the receiver has an internal gain control to compensate for optical loss and insure a nominal 1-V peak-to-peak output. Each module has a direct-coupled 75-Ω electrical connector. The optical source is an 820-nm light-emitting diode mounted in an SMA miniature microwave-compatible connector. Its power requirements are 110 or 220 V, 50 or 60 Hz, at less than 8 W.

The standard FOL-10V, without fiber, is priced at $750 for quantities of one to nine. Delivery takes four to six weeks.

Manage Inc., 165 Front St., Chicopee, Mass. 01013. Phone (413) 594-4026 [405]

Hawk 4020 monitors RS-232-C digital traffic

The Hawk 4020 data-communications analyzer for field service use performs interactive troubleshooting and passive monitoring of serial data associated with the RS-232-C digital interface. It has an optional teletypewriter interface. Data traffic is read out on a one-line, 20-character alphanumeric display. Sophisticated interactive and monitoring functions are configured from a menu selection format that displays the various system parameters.

It accommodates asynchronous and synchronous data rates of up to 19,200 b/s, and it captures and stores up to 256 characters, including four EIA control lines, for later analysis. The 4020 allows field service technicians to isolate data-communications problems, passively monitor and trap on-line data, perform a bit- or block-error rate test, and simulate both data-terminal and data-communications equipment for interactive communication with both local and remote network components. It can also be configured to transmit or reply to polling messages, to generate or verify cyclic

redundancy checks, and to measure the delay between rise of request to send and rise of clear to send as well as between the fall of request to send and the rise in data-carrier detect.

The Hawk 4020 sells for $3,595 in single-unit quantities, with delivery of the analyzer 90 days after receipt of order.

International Data Sciences Inc., 7 Wellington Rd., Lincoln, R. I. 02865. Phone (401) 333-6200 [406]

74LS. CMOS. SPI.

SPI's 74LS Devices In CMOS

SPI gives you 20 new reasons to celebrate.

If you're a system designer, you know that CMOS is the process of the 80s. And SPI is the CMOS innovator. We've taken 20 of the most popular 74LS devices and manufactured them in CMOS — to give you low power and increased system performance.

Our 74SC components are pin-for-pin compatible, direct plug-in replacements for low power Schottky devices. But you also get the advantages of CMOS: significantly lower power, higher noise immunity, full TTL compatibility (input and output) and the same high speed.

Best of all, they are available now at prices that will surprise you.

SPI CMOS Makes It Possible

Our 74SC devices are fabricated using a proprietary selective oxidation silicon gate process we call SPI CMOS. It's the same advanced technology that we use in our 500- and 1000-gate uncommitted logic arrays, so you know it's been proven where it counts — in the field.

SPI's new family of 74SC components covers the range of the most widely used devices. Decoders. Multiplexers. Octal drivers. Transceivers. Flip-Flops. Latches. All are direct plug-in replacements designed to solve marginal performance problems in existing designs. Or, with an eye on the future, you can design in the building blocks for tomorrow's high-speed, low-power CMOS systems.

Put SPI's CMOS 74SC products to work in existing applications where high-noise immunity and/or low power is desirable. And that's just the beginning.

On The Shelf Now

You can start using SPI's CMOS 74SC products today because they're available now.

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- **SP74SC237** 1 of 8 Decoder with Input Latches
- **SP74SC238** 1 of 8 Decoder
- **SP74SC239** Dual 1 of 4 Decoder
- **SP74SC240** Octal Inverting Buffer
- **SP74SC241** Octal Buffer
- **SP74SC244** Octal Buffer
- **SP74SC245** Octal Transceiver
- **SP74SC373** Octal Transparent Latch
- **SP74SC374** Octal D-Type Flip-Flop
- **SP74SC533** Octal Inverted Output, Transparent Latch
- **SP74SC534** Octal Inverted Output, D-Type Flip-Flop
- **SP74SC540** Octal Buffer
- **SP74SC541** Octal Buffer
- **SP74SC563** Octal Inverted Output, Transparent Latch
- **SP74SC564** Octal Inverted Output, D-Type Flip-Flop
- **SP74SC573** Octal Transparent Latch
- **SP74SC574** Octal D-Type Flip-Flop

SPI SEMI PROCESSES INC.

1885 Norman Avenue, Santa Clara, CA 95050, Tel: (408) 988-4004
TWX: 910-338-0025 SPI SNTA

SPI in Europe: Semi Processes Inc., Austin House, South Bar, Banbury, Oxfordshire, England, Tel: (44)-295-61138 Telex: 837594

Circle 177 on reader service card

Computers & peripherals

Unibus board supports X.25

Communications controller handles X.25 packet switching and IBM, Univac protocols

In distributed data processing, communications can consume up to 50% of the computing power of systems like Digital Equipment Corp.'s LSI-11/23 and PDP-11. But when it is handled by front-end processors like the Unibus Communications System from Plessey Peripheral Systems, the central processing unit is freed to handle other tasks. The UCS board handles communications using the increasingly popular X.25 packet-switching protocol [*Electronics*, Sept. 22, p. 34] and is available in versions designed for IBM and Univac protocols.

The introduction of UCS, which has been tested at three sites in Europe and the U. S., moves Plessey into the distributed data-processing market. The firm spent over a year testing its offering before stepping into distributed processing "because communications is a different world. We had to learn to deal with new problems in service and support and train our staff," explains Brent Vanderwood, communications products marketing manager.

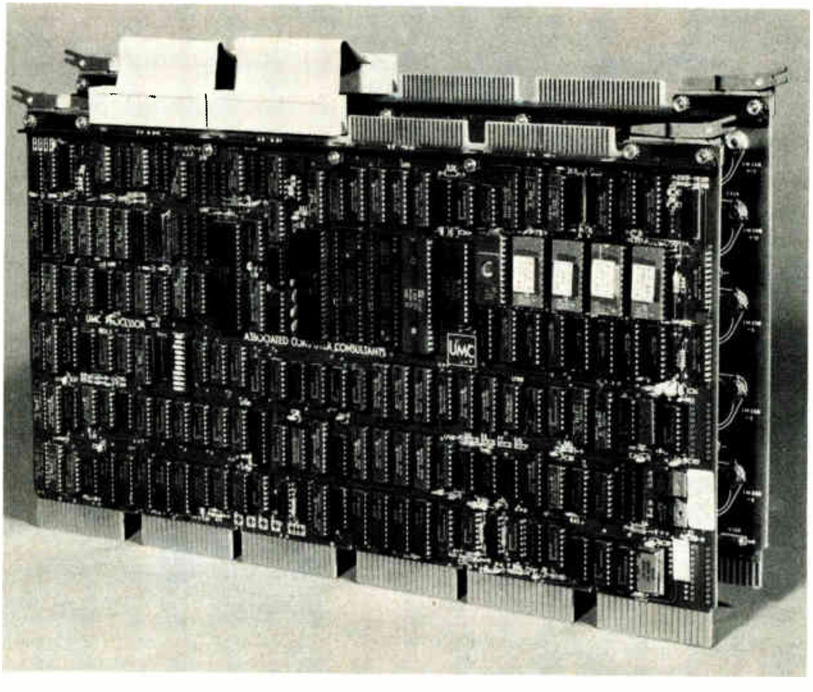
The UCS is designed to help users of Plessey's DEC-emulating systems communicate with host computers. The products for other protocols have some variations, but all use a processor board designed for Plessey by Associated Computer Consultants of Santa Barbara, Calif. The Z80A-based processor runs at 4 MHz and has 4-K bytes of random-access memory and 16-K bytes of user-programmable read-only memory. Like all the boards that work with it, the processor fits a single slot in a hex-width standard peripheral-controller backplane.

Although the product could be added to nearly any DEC-compatible system, Plessey plans to market it only to existing Plessey users and in new systems. It will be offered for the SYST-24, -34, and -44 and for the SYST-13VB and -23V, which require Plessey's Q-bus-to-Unibus converter.

The UCS communications board supports X.25 protocol to level 3, the highest level currently specified by the International Consultative Committee for Telegraphy and Telephony (CCITT). For X.25 use, the processor board coordinates with a memory-expansion controller, which provides buffering for the 32 virtual circuits necessary for X.25 communications. It provides 64-K bytes of RAM and does not add to the bus load. Software implementing the X.29 interactive terminal protocol is provided for users who require it, thus enabling communication with networks that use X.25 as well as Tymnet, Telenet, and others.

Other protocols supported are IBM's 2780/3780, Houston Automatic Spooling Program (HASP), and 3270; and Univac's Nine Thousand Remote (NTR), UTS-400, and U200/DCT1000. Hardware is the same for all, but firmware is altered for each variation. The IBM HASP and Univac NTR protocols require only the processor board, whereas the remaining modes demand a terminal controller board for full utilization. The controller is also a 4-MHz, Z80A-based card with 32-K bytes of RAM. It provides eight full-duplex RS-232-C lines. For block-mode terminals like the IBM 3277 and Univac U200, 16-K bytes of PROM is provided. Up to four controllers can be tied to a single processor board with the remaining protocols, supporting a maximum of 32 terminals.

With the controller board, users can connect ASCII terminals to the mainframe, emulating native terminals. With this emulation the mainframe determines the screen format of the terminals and communicates with the minicomputer using a direct-memory-access terminal interface. The DMA capability spans 256-K bytes. The latter setup eliminates the need for additional terminal controllers, such as DEC's DZ11 board.



The $10,000 for the X.25 products and $9,000 for the basic system include software. Boards in complete systems will add their price to the system price. Delivery of the communications system takes 60 days after receipt of order.

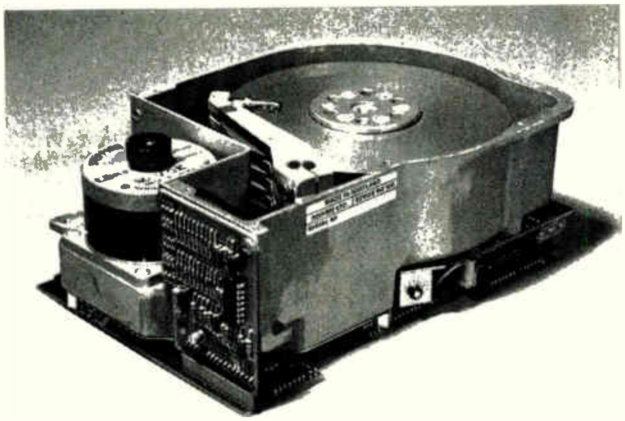
Plessey Peripheral Systems, 1691 Browning Ave., Irvine, Calif. 92714. Phone (714) 557-9811 [361]

MALLORY

5¼-in. drive has four platters

Compact Winchester drive stores 16 megabytes, accesses in 85 ms, average

A 5¼-in. Winchester disk drive developed in Glenrothes, Scotland, fits four platters into an 8-by-5¾-by-3¼-in. package, which is no larger than many competing drives with only two platters. At 8,100 b/in. and 260 tracks/in., the RO-100 drive's eight surfaces store a full 16 megabytes of unformatted data. The average access time for the unit is 85 ms and the track-to-track access time is 18 ms.



The drive's manufacturer, Rodime Ltd., is a spin-off from neighboring Burroughs Machines Ltd. that was founded by several veterans of the disk-storage business intimate with the exacting mechanical engineering so critical to hard-disk reliability. The four-platter design, for instance, calls for an extremely rigid head-actuator mechanism to position the head furthest from the bearings accurately. Rodime chose a rotary actuator with five head-carrying arms mounted on a common spindle.

This arrangement is not only more rigid than linear actuators, but it consumes less power and produces fewer wear particles, as there are fewer moving parts. A microprocessor calculates the optimum acceleration, decceleration, and damping required, buffers the incoming stepper-motor pulses, and compensates for mechanical positional hysteresis.

Air is pumped from the drive's upper disk-head chamber down into a lower chamber, where it passes over the actuator linkage and then back to the upper chamber through an absolute filter. This air flow keeps both chambers at the same temperature, improving compensation for thermal expansion in the arms, disks, and other components. The net result, according to marketing manager Malcom Dudson, is high actuator accuracy and the elimination of adjustments.

The company has also designed special shaft bearings and hubs, which improve air flow between disks enough for them to be packed closer together. New head and media technologies, says Dudson, may be incorporated at a later date without the need for total redesign.

The unit's microprocessor monitors the power-on sequence (the drive is up to speed in 10 to 18 s) and the motor speed, to within 1%, through use of a phase-locked-loop dc-motor controller. Fault diagnostics are built in; status codes are indicated by light-emitting diodes on the front panel.

Rodime is offering the drive with one, two, three, or four platters; the four-platter, 16-megabyte version is priced at $1,365 in 500-unit lots, and a single-platter drive is $690 in similar quantities. The firm already has over 100 evaluation models out in the field, claims $2 million worth of orders, and plans to ship 20,000 units next year.

Rodime Ltd., 12-14 Edison House, Fullerton Road, Glenrothes, Fife KY7 5QR, Scotland [362]

23591 El Toro Rd., Suite 208, P. O. Box 1122, El Toro, Calif. 92630 [369]

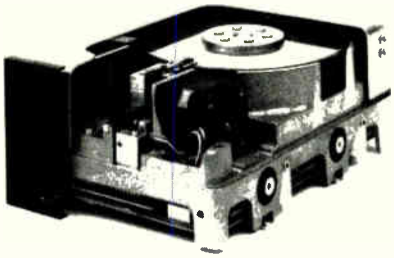
12.8-megabyte Winchester carries $845 price tag

The Miniscribe I 5¼-in. Winchester disk drive is available in one- and two-disk models providing 6.4 and 12.8 megabytes of unformatted storage capacity respectively. It is compatible with the Seagate ST506 interface, uses the same dc voltages, and has the same form factor as 5¼-in. floppy-disk drives.

The Miniscribe I provides area recording densities of 3.46 Mb/in.^{2} for Winchester disk drives using conventional ferrite heads and oxide disks. Reliable performance at this density has been achieved with a rack-and-pinion motion translator, which provides for the increased number of recording tracks while retaining the full step-holding torque and positioning repeatability of the stepper-motor actuator. The positioning repeatability over the 4° to 46°C operating range is enhanced by temperature compensation.

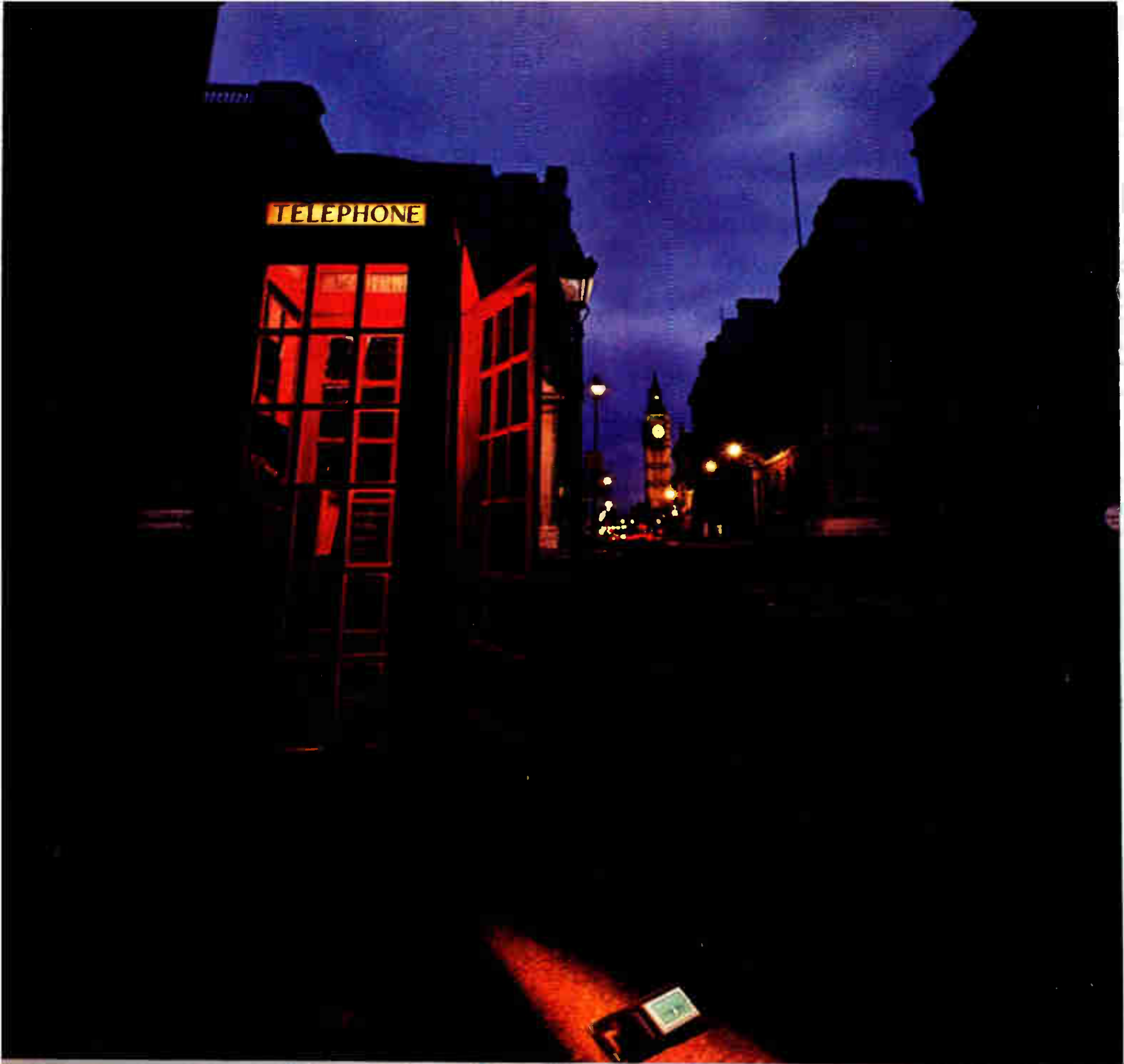
The drive features a 179-ms average access time and a data-transfer rate of 5 Mb/s. Prices for 1,000-unit lots to original-equipment manufacturers are $745 for the 6.4-megabyte version and $845 for the 12.8-megabyte model. Evaluation units are available now; production quantities are expected early in 1982.

Miniscribe Corp., 410 South St., Longmont, Colo. 80501. Phone (303) 651-6000 [363]



Multipurpose processor has ergonomic features

Datapoint's 8600 processor and work station incorporates such ergonomic features as a compact enclosure with

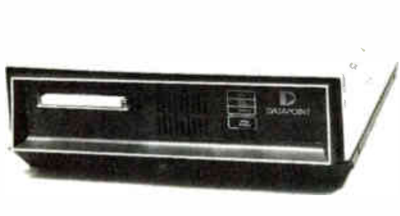

TELEPHONE

an optional tilt-and-rotate base and a 12-in. brown screen with amber characters. It has a powerful central processor and a memory capacity of up to 256-K bytes. While fully compatible with Datapoint's Attached Resource Computer local network, it can stand alone.

Operating with Resource Management System software, the 8600 can simultaneously perform Cobol execution, word processing, data entry, and electronic mail functions.

Introduced with the 8600 is the 9301 disk unit, a fixed-media minidisk system that can store 20 megabytes on a stack of 5¼-in. platters. The 9301 also includes in the same housing a cartridge tape drive that can transfer the entire disk's contents to a single ¼-in. tape cartridge at 56.3 in./s. Prices start at $7,500 for the 8600 and $22,950 for the 9301 and vary with options. The units are available immediately.

Datapoint Corp., 9725 Datapoint Dr., San Antonio, Texas 78284. Phone (512) 699-7059 [364]



Digital image analyzer accepts any medium

The MOP 30 digital image analyzer determines dimensional characteristics of images and analyzes with its measuring tablet all types of image media including photographs, transparencies, prints, and projections. An updated version of the MOP 3, it adds 20 different geometric parameters and provides for stereological calculations and standard statistics, including histogram printouts.

The MOP 30 has a built-in printer and an RS-232-C serial interface to connect to computers for data storage or more complex data processing. Users can thus take advantage of complete image analysis programs while retaining the speed of the dedicated microprocessor in the MOP 30. The $9,985 analyzer can be delivered from stock.

Carl Zeiss Inc., 444 Fifth Ave., New York, N. Y. 10018. Phone (212) 730-4475 [365]

CAD imaging display system offers 256 blinking 3-D colors

Advanced Electronics Design's AED512R full-color imaging display system is for computer-aided design and process control applications. The system employs a separate keyboard and controller for a working area free of electronics, and the controller is in a 5¼-in.-high rack-mountable housing. This configuration enables the AED512R to add powerful graphics and imaging capabilities to either a local or remote computer and to provide features that were previously obtainable only from more costly, bulkier graphics imaging display systems.

The AED512R is usually employed as a telecommunications terminal that can communicate serially via an RS-232-C interface or a 20-mA current loop. Alternatively, the unit can be supplied as a computer peripheral that is under direct-memory-access control of minicomputers like the DEC VAX, PDP-11, and LSI-11, as well as Data General Nova and microNova, Varian, and larger mainframe computers.

The AED512R offers resolutions of 512 by 512 by 8, 1,024 by 512 by 4, or 1,024 by 1,024 by 2 bits, or other combinations. Up to 256 symbols can be defined by the user as raster-graphic overlays, each with its own horizontal and vertical size. The user can simultaneously select 256 of 16.8 million colors and any eight colors can be blinked at independent rates to any other 8 colors. Also, the 256 colors can be shaded for a three-dimensional effect. The system sells for under $20,000 and delivery takes 30 days.

Advanced Electronics Design Inc., 440 Potrero Ave., Sunnyvale, Calif. 94086. Phone (408) 733-3555 [367]

Circle 185 on reader service card

"The dependable SM-2 relies on 27 flexible circuits of PYRALUX,"

says M. C. Keel, Vice President and Program Director, Standard Missile Programs, General Dynamics Pomona Division.

"SM-2 is a proven system with a high reliability record. That record was the result of painstaking effort, and part of the story was the selection of PYRALUX flexible composites to achieve reliable high density packaging," says Mr. Keel. "We can stack printed cable assemblies with PYRALUX 4 layers high in tight missile spaces, bend them 180,° and we know they won't fail. We use PYRALUX for all 27 flexible circuits in the Navy's SM-2 missile," he concluded.

The missile's autopilot and battery circuits of PYRALUX consist of two 4-layer flat cable assemblies containing power, signal, and shielded digital circuits.

PYRALUX® flexible composites are a family of tough, adhesive-coated, laminated substrates offering high strength for flexible, rigid/flexible multilayer circuitry. The PYRALUX WA/A adhesive provides excellent and uniform adhesion to KAPTON® Polyimide Film, minimizing the worry of physical or chemical delamination. Conventional production solvents and chemicals can be used without affecting the bond. PYRALUX also has excellent resistance to the thermal exposure of solder dip, wave and reflow. Circuits can be removed, repaired and resoldered reliably.

Investigate the advantages of specifying PYRALUX flexible composites for your circuitry. For more information, write Du Pont Company, Rm. X38894, Wilmington, DE 19898.

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Circle 187 on reader service card

Packaging & production

Trimmer's speed, quality improved

System for laser trimming of hybrid circuits gains new YAG laser, faster parts handler

Electro Scientific Industries Inc.'s model 44 laser-trimming system for hybrid microcircuit work is being equipped with a proprietary new laser and a higher level of automation that increases throughput. The company will exhibit the improved trimming system at the International Society for Hybrid Microelectronics show held in Chicago Oct. 12–14.

The high-power, medium-pulse-width yttrium-aluminum-garnet laser is both designed and manufactured by the company. Chief among its attributes is pulse-to-pulse stability; it promises both higher trimming speeds and higher-quality kerfs than previously possible, the firm says.

Throughput is also boosted by an automatic loading and unloading system for ESI's four-position carousel parts handler. In conjunction with a single-axis probe stepper for one-cycle trimming of multiple-circuit substrates, the parts handler surpasses step-and-repeat handler throughput in many cases and requires less of the operator. The handling system accepts cassettes carrying substrates ranging in size from 1 by 1 to 3 by 3 in. and having aspect ratios of less than 2:1.

The trimming machine's PDP-11/03 minicomputer has gained a Winchester disk drive to boost system speed and a soft-sectored floppy-disk drive for backup and software distribution. A VT100-compatible video terminal is available to take advantage of the new software-support package.

The new Version 7 software-support package includes ESI's Fastrim program and speed-optimized procedures for user-written Pascal programs. The Pascal compiler, now version 1.2, has been refined. The package also contains the latest release of Digital Equipment Corp.'s real-time operating system, RT-11 Version 4, with a high-level command interface, new text editors, a help facility, and other utilities that make program development easier.

A model 44 hybrid-circuit trimming system ordered with all the above options will be priced from $240,000 to $250,000. Deliveries are set to begin in April.

Electro Scientific Industries Inc., 13900 N. W. Science Park Dr., Portland, Ore. 97229. Phone (503) 641-4141 [391]

Wafer-transfer unit is gentle

System moves wafers from widely spaced cleaning racks to diffusion-step carriers

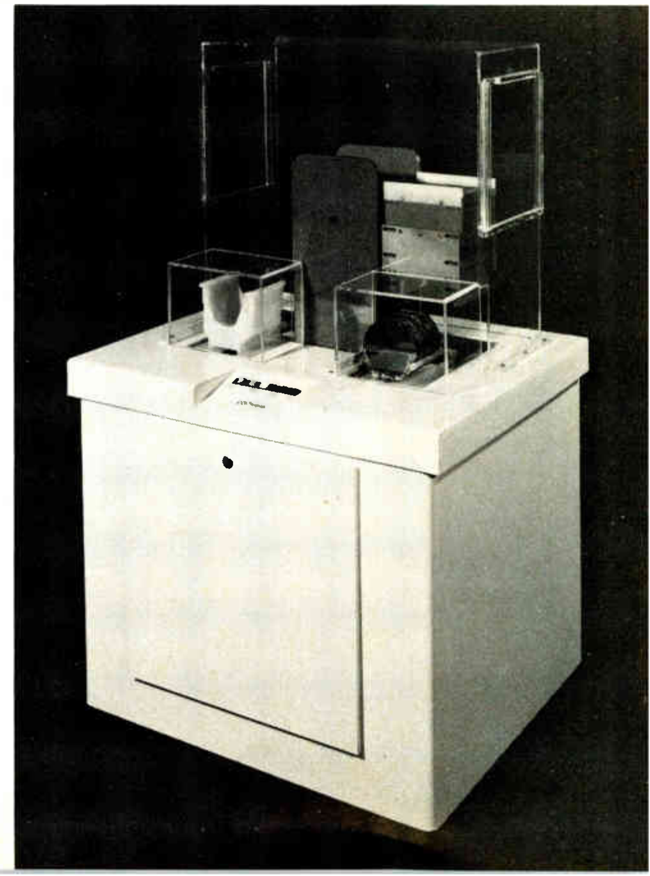
Transferring wafers from widely spaced cleaning-and-coating racks to narrowly spaced diffusion carriers often results in their chipping, scratching, breaking, and contamination. The Automatic Mass Wafer Transfer system from Micro Glass Inc. avoids this problem. It handles wafers as large as 6 in. in diameter, transferring production-size quantities from cleaning racks to diffusion carriers without using tweezers or vacuum wands.

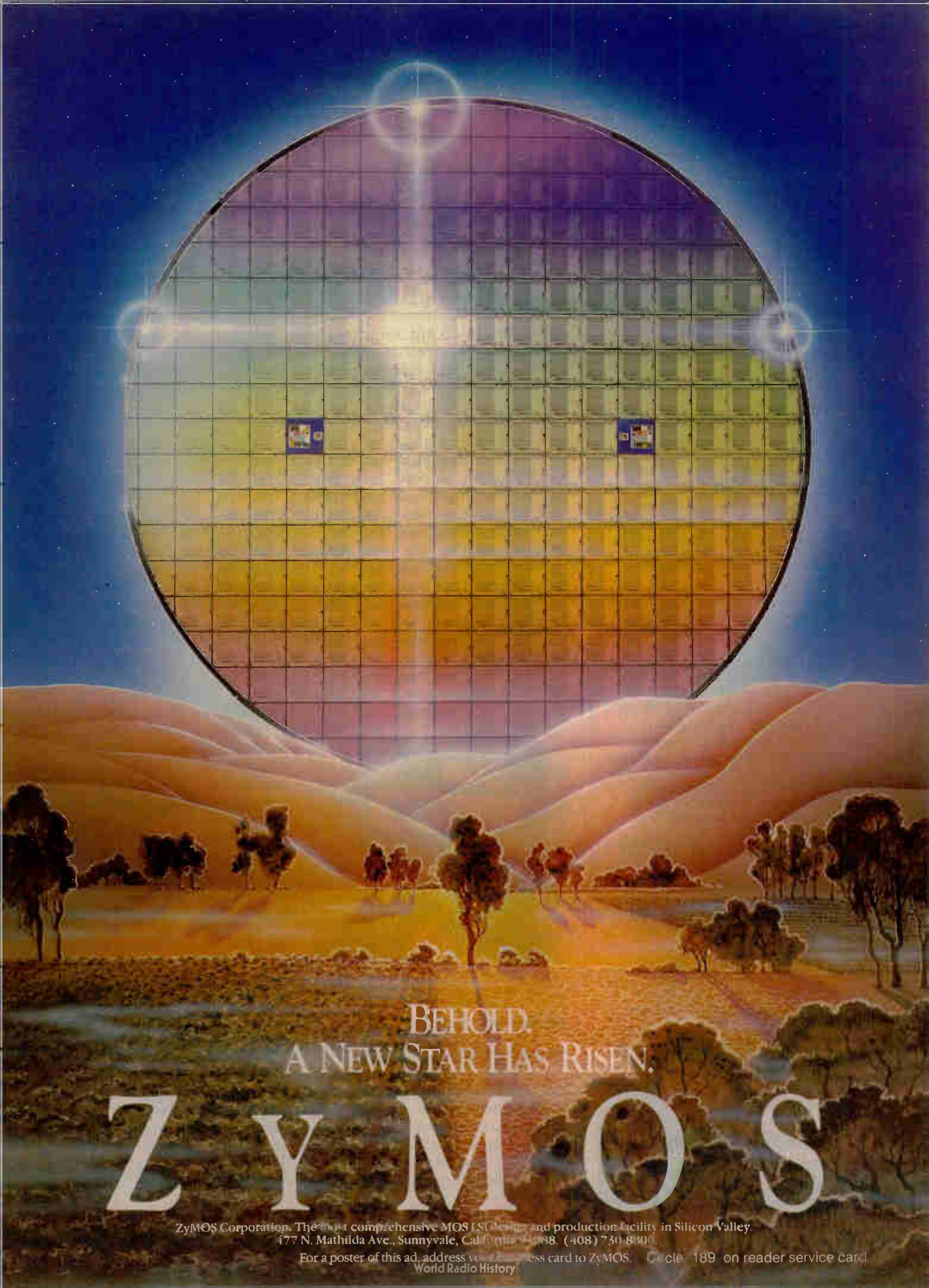
Microprocessor controlled. A patented space-index transition device, coupled with an automated drive, ensures low-impact transfer. When the wafers are moved under the force of gravity, the rate is sufficiently controlled and slow to reduce breakage from mechanical shock. A typical machine cycle, transferring fifty 5-in. wafers from two plastic carriers to one quartz diffusion carrier, takes less than 3 minutes.

The operater feeds the system with full plastic wafer-carriers and empty quartz carriers, and activates the microprocessor-controlled automatic cycle. At cycle's end, the loaded quartz carrier is ready to be inserted into the diffusion furnace. Backlighted push buttons on the front control panel signal instructions to the operator.

The Automatic Mass Wafer Transfer system may be fitted to handle wafers of 100-, 125-, or 150-mm in diameter. It can also be optionally furnished to transfer 25 wafers directly to 25 spaces, two racks of 25 each to a 50-spaces rack, or two 20s to a 40, for 125- and 150-mm wafers only. The system can also be set up to handle plasma-etched wafers at an even exchange of 25 to 25.

The machine operates on 80 lb/in.^{2} of clean compressed air or dry nitrogen and a 110- or 220-V ac power supply. Pricing starts at

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477 N. Mathilda Ave., Sunnyvale, California 94088. (408) 730-8300.
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$16,000 and delivery after receipt of order takes 8 to 12 weeks.

Micro Glass Inc., MGI Systems Division, 2026 West Campus Dr., Tempe, Ariz. 85282. Phone (602) 966-1474 [392]

Nickel thickness measured on printed-wiring boards

Printed-wiring-board manufacturers and incoming-inspection personnel have another tool in the Nickelderm N-80A for quality-control checking. By using the Hall-effect principle, the N-80A can accurately measure the thickness of nickel in mils or micrometers through overplates like gold, rhodium, tin-lead, brass, plastic, bronze, tungsten, aluminum, and zinc diecast on printed-wiring boards and small components. The instrument is available with probe guides, probes, and thickness standards that are designed for measuring printed-wiring boards and other small parts.

The Nickelderm N-80A sells for $2,595. Delivery is in three weeks after receipt of order.

UPA Technology Inc., Sales and Marketing Service, 60 Oak Dr., Syosset, N. Y. 11791. Phone (516) 364-1080 [393]

Solder-bearing lead clip ensures reliable interface

NAS Electronics' NASFLO edge clips should reduce hybrid and chip-carrier assembly production costs by eliminating fluxing, wicking, solder dipping, and solder pastes. Solid or cored solder is attached to the interface portion of their leads to ensure a reliable electric interface between the substrate pad and the clip, as well as the printed-circuit board.

The NASFLO edge clips are on either 100- or 50-mil centers and supplied in reel form with a wide variety of combinations of solders and flux. Leads for single in-line packages sell for $4.45 per thousand in orders of 10 million. Dual in-line types are also available. Delivery takes three to four weeks.

NAS Electronics, 381 Park St., Hackensack, N. J. 07602. Phone (201) 343-3156 [395]

Test handler accommodates 6- to 40-lead packages

Unusual lead configurations common to hybrid components can be accommodated by using the T-2095 test handler. It has similar features to other Trigon test handlers, such as easy operation and simplified mechanisms, but it also can handle 6- to 40-lead packages that measure 275 to 830 mils wide and 220 to 375 mils thick.

The T-2095 has fail-safe sorting, digital setup dials, five-sort programmable outputs, and serial or parallel operation. It sells for $20,000 and comes with software and installation instructions. Delivery takes 12 to 16 weeks.

Trigon Industries Inc., 311 Ravendale Dr., Mountain View, Calif. 94043. Phone (415) 965-3600 [398]

Mask aligner-exposure system handles variety of substrates

The OAI Hybralign series 400 mask alignment and exposure system handles a variety of substrates, including hybrids, liquid-crystal displays, microwave devices, and power semiconductors. It is composed of an exposure transport stage, viewing optics that accommodate split-field and stereo-zoom microscopes as well as video-display options, and a choice of light sources. Lamps are available with power ratings of 200, 350, and

SUPER TEX DECLARES WAR ON POWER HOGS

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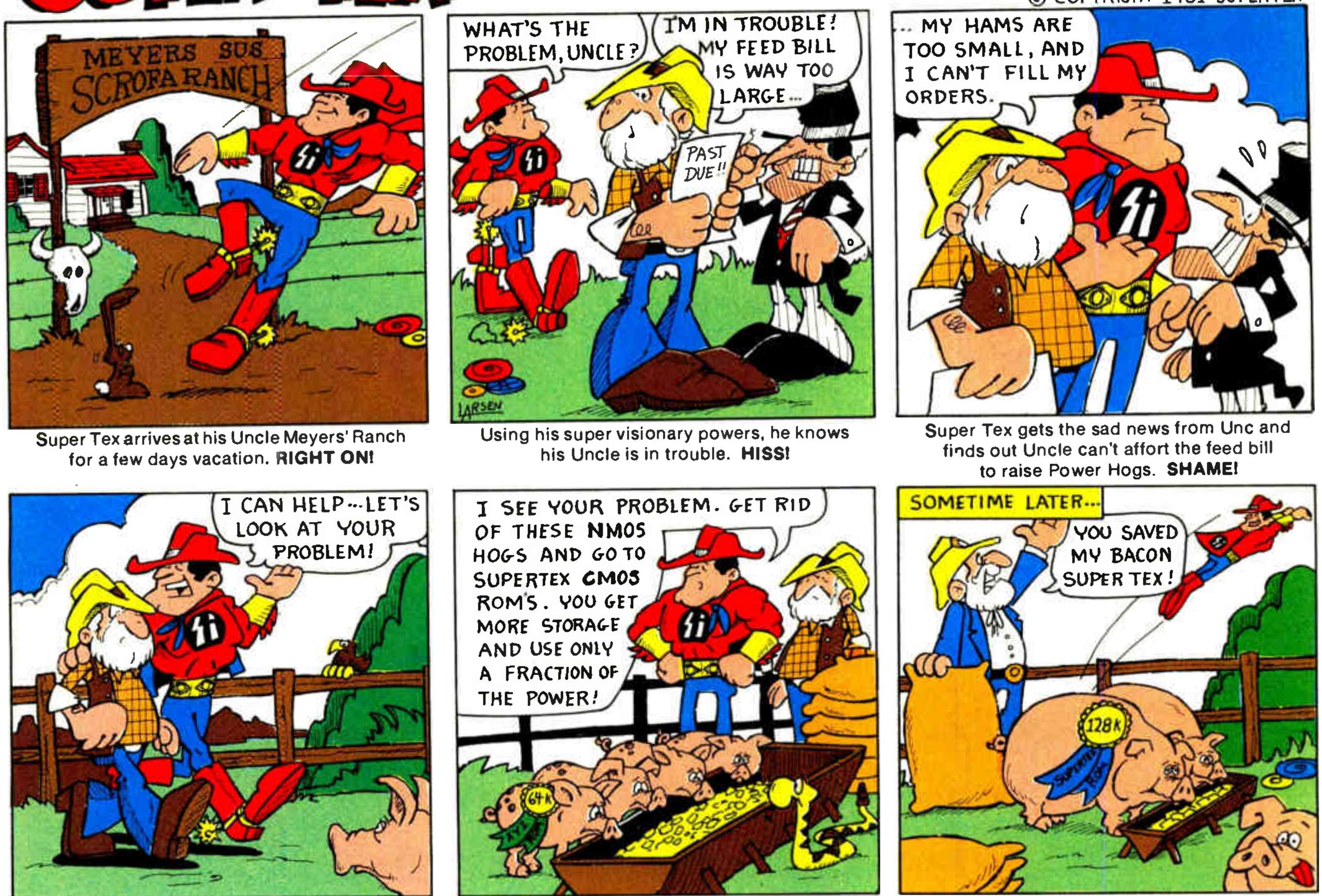

Super Tex arrives at his Uncle Meyers' Ranch for a few days vacation. **RIGHT ON!**

Using his super visionary powers, he knows his Uncle is in trouble. **HISS!**

Super Tex gets the sad news from Unc and finds out Uncle can't afford the feed bill to raise Power Hogs. **SHAME!**

"There has to be a simple solution to the problem, Uncle." **REJOICE!**

Uncle Meyers is not getting his money's worth with XYZ brand ROMs. **BOO!**

By changing his Uncle's system to Supertex extra low power ROMS the ranch is saved. **APPLAUSE!**

To be continued ....

If you are using Power Hogs ... Change now to Supertex SuperROMs and get:

- Very low power dissipation
  Standby 7μA typ.
  Operating 8mA typ.
- Large Capacity —
  16, 32, 64, 128, 256 K bits
- Fully Static
- 8 bit organization
- Low Cost
- 5V power supply
- High reliability, low power consumption eliminates packaging problems
- All Temp grades available —
  Commercial, Industrial, Military
- Plastic or ceramic DIP
- Perfect for battery and remote control applications

Call, clip the coupon, or circle the bingo, but start today on your evaluation of SuperROMs. We will send you a catalog by return mail.

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Supertex

1225 Bordeaux Drive, Sunnyvale, CA 94086
(408) 744-0100 TWX 910-339-9388

500 W. The system includes a controller that ensures constant intensity at the exposure plane regardless of lamp aging and power-line fluctuations. An exposure monitor and timer allows programmable photoresist exposure times in 0.1-second intervals from 0.1 to 99.9 s and 1-second intervals from 1 to 999 s.

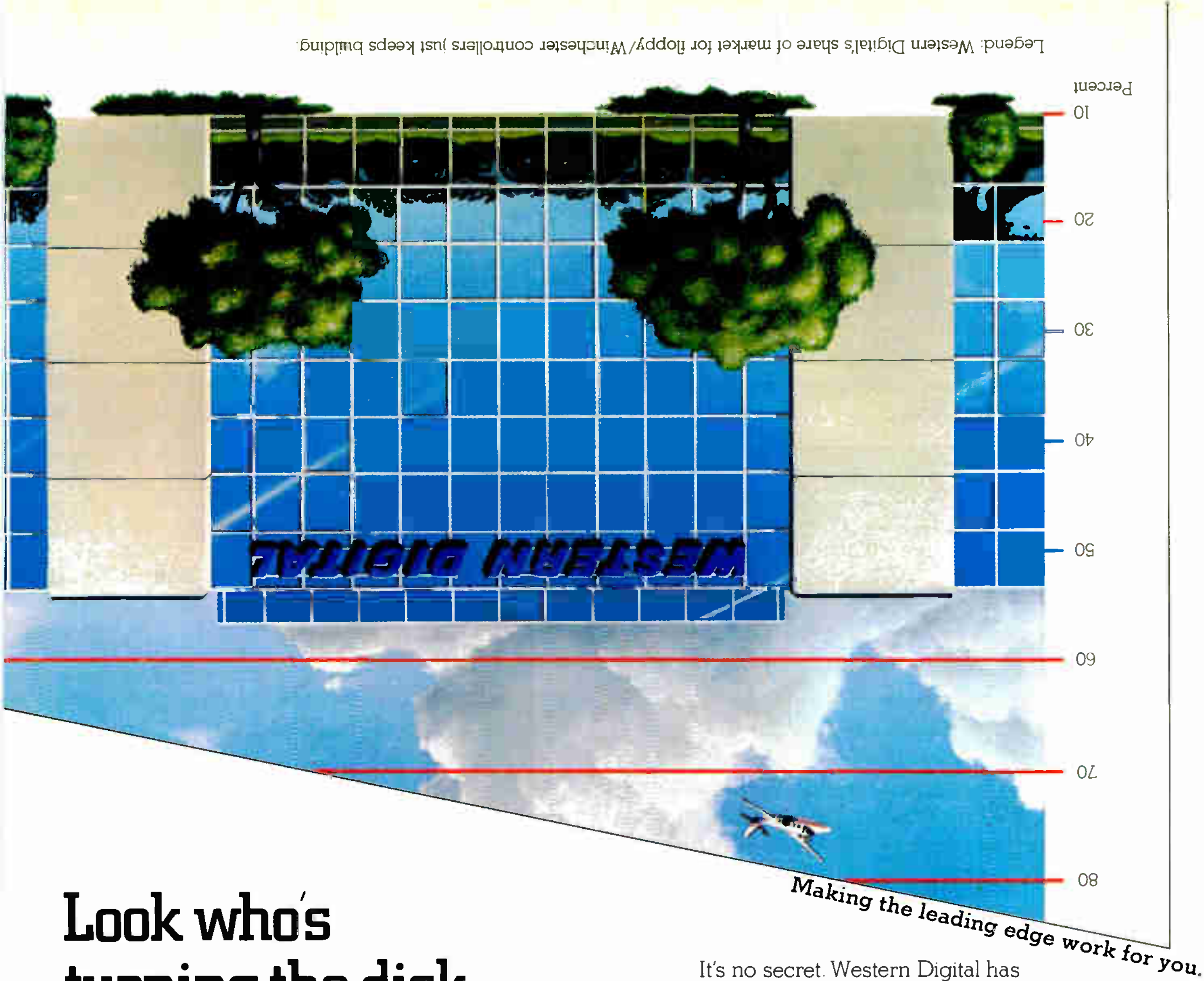
The Series 400 has micrometer-controlled X-Y adjustments that are independent and backlash-free. A vacuum chuck is mounted in a pre-loaded bearing assembly to minimize free play in the X-Y plane. Z-axis movement is achieved by raising and lowering the chuck rather than the mask. This feature prevents distortion in the substrate that can occur in cantilevered mask-frame designs.

Prices range from $15,000 to $35,000. Delivery takes six to eight weeks.

Optical Associates Inc., 3300 Edward Ave., Santa Clara, Calif. 95050 [394]

IC tester checks 128-K bytes of ROM in two seconds

Integrated-circuit tester ROM Test II can be used to check and verify 128-K bytes of read-only memory, programmable ROM, and erasable PROM in less than two seconds without in-circuit probing of data lines. To verify the memory, the user inserts a personality board into the unit, causing a single signature to be indicated on a four-digit display. The testing of a 64-K device would



Look who's turning the disk controller market upside down.

It's no secret. Western Digital has been building a reputation for innovative disk controllers for years.

It started back in 1977 with the world's first LSI floppy disk controller. And now includes the first Winchester disk controller, too.

What's more, today, Western Digital's 7-member family of floppy disk controllers is *the* industry standard. Giving you nothing short of the broadest selection of controllers in the business.

And only Western Digital offers the vital support chips for both data separation and DMA control.

Of course, our pioneering Winchester controller effort is equally impressive. Either as a fully-assembled board or money-saving chip set. And our extensive on-line design support services are yet another plus.

Better still, more breakthroughs are on the way. So contact the only disk controller maker holding all the chips.

Western Digital.

We'll stand on our head to give you better solutions.

WESTERN DIGITAL
C O R P O R A T I O N

Computer Products Division, 2445 McCabe Way, Irvine, CA 92714, (714) 557-3550.

Circle 193 on reader service card

normally require probing 80 data lines and reading 80 signatures, but the ROM Test II requires no probing and it reads only 10 signatures to check the device.

Applications for the ROM Test II include incoming-device inspection, production-line testing, memory verification after programming, and maintenance troubleshooting during service calls. It has an error-detection probability of 100% for single-bit errors and 99.998% for multiple-bit errors and can be operated from either 115- or 220-V ac power, switch-selectable.

The unit price for the ROM Test II is $795. The average personality board costs $35. Delivery is 10 days after receipt of order.

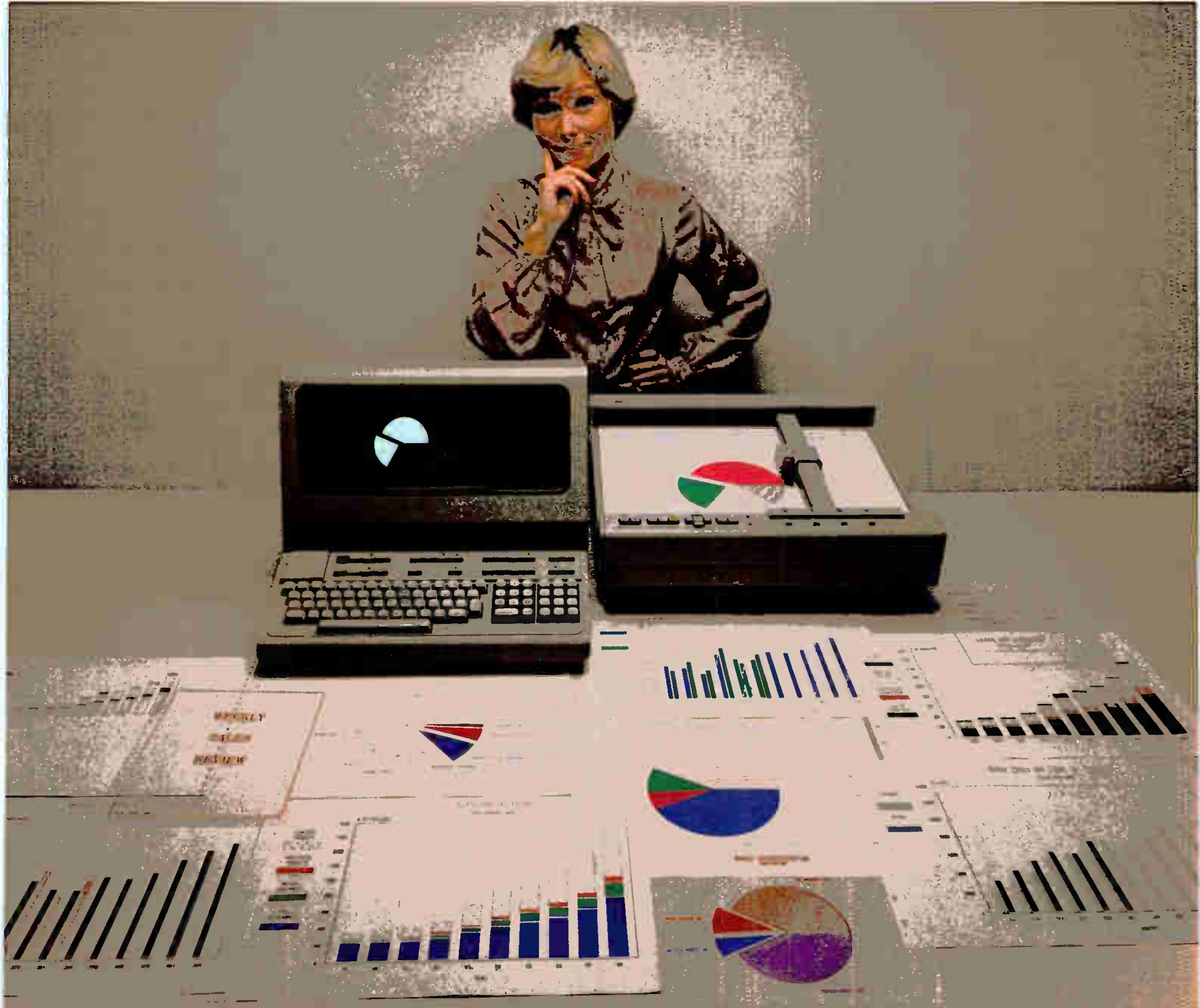
Kurz-Kasch Inc., 2271 Arbor Blvd., Dayton, Ohio 45439. Phone (513) 299-0990 [396]

Spring-loaded binding post is insulated to prevent shock

To help reduce the potential danger of shocks from exposed wires, the model 4770 insulated spring-loaded binding post allows wires and plugs up to 2.26 mm in diameter to be connected to it so that no metal is exposed when the connection is completed.

Measuring 51.3 mm when open, the post has a brass body and tin plating; its construction conforms to MIL-T-10727 standards. It comes in black, red, yellow, green, blue, and white and is rated at 630 V peak maximum. It is priced at $3.85 each, with delivery taking three to six weeks after receipt of order.

ITT, Pomona Electronics Division, 1500 East Ninth St., P. O. Box 2767, Pomona, Calif. 91766. Phone (714) 623-3463 [399]



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Circle 195 on reader service card

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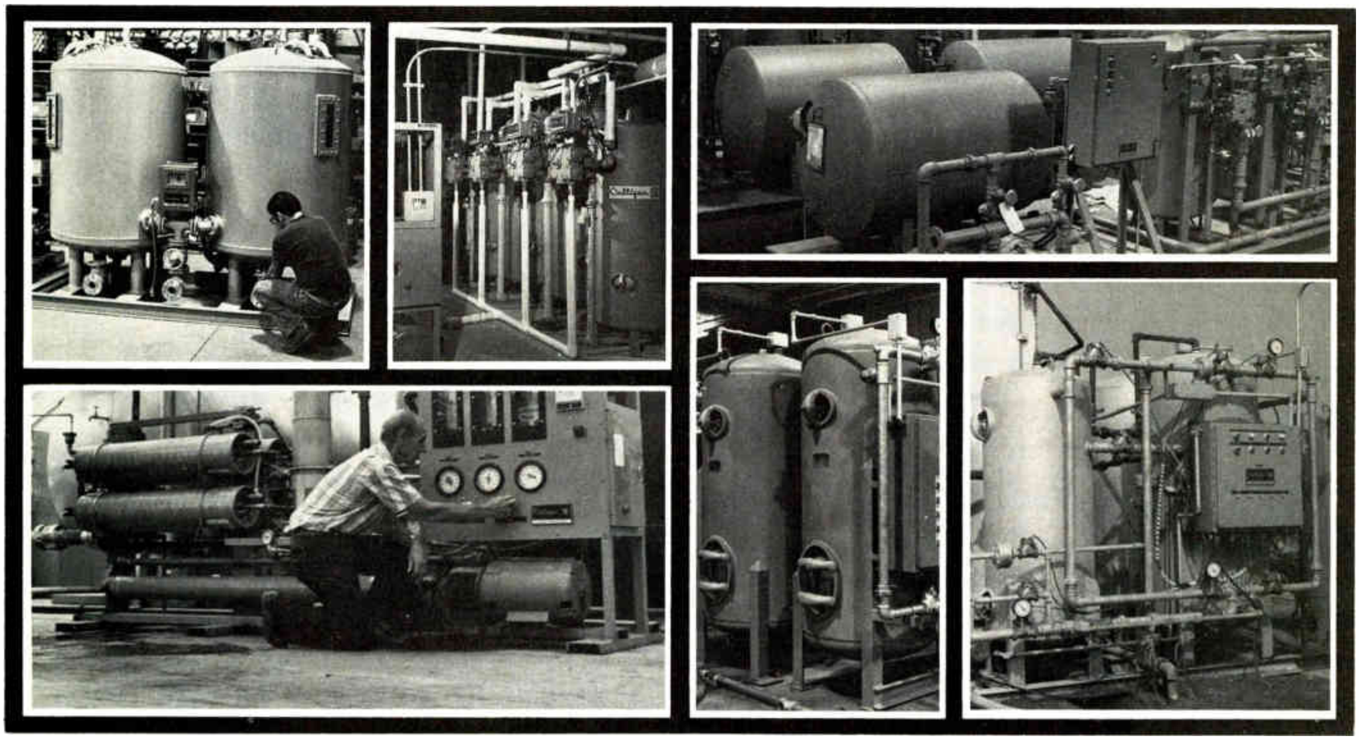

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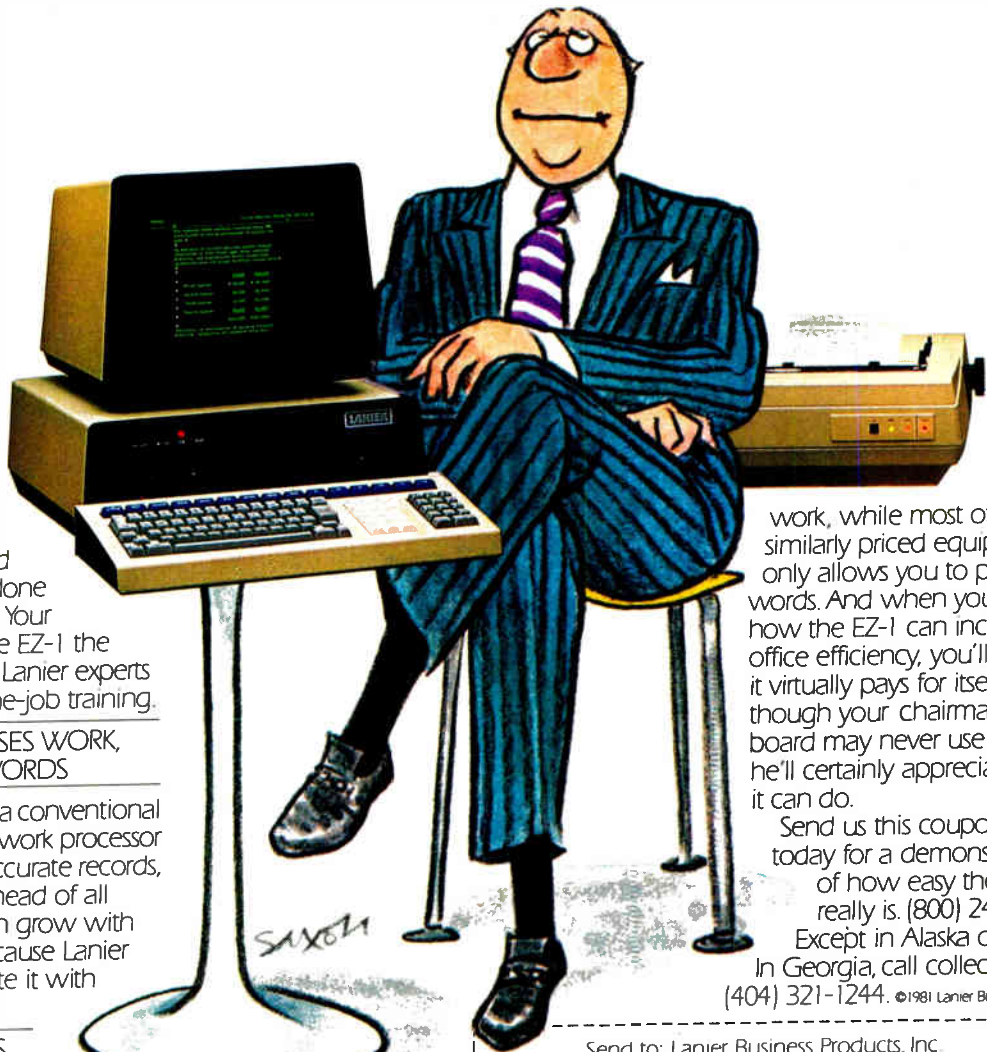

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Circle 197 on reader service card

Products Newsletter

Bubble memory adds 128-K bytes to Intel board computers

Undaunted by its competitors' exodus from the bubble-memory market, Intel Corp. of Santa Clara, Calif., is continuing to expand its product line with the introduction this month of a multimodule board that contains 128-K bytes of bubble memory and interfaces with the company's single-board computer line through the SBX bus. The new board is the iSBX-251, **which transfers data at a rate of 12.5-K bytes/s in either direct memory-access, interrupt, or polled modes.** The data access time for the iSBX-251 is 48 ms, and its placement on the SBX bus frees the Multibus for other traffic while the host computer accesses the bubble memory. The module will be priced at $1,200 in lots of 100.

Burn-in tester cites error's address

Reliability Inc. of Houston, Texas, is unveiling a second burn-in tester capable of providing performance data down to the individual cells. Intersect, which is smaller than the Intercept burn-in tester and comes just five months later [*Electronics*, May 19, p. 221], can hold up to 600 memory devices (16-K-by-1-bit and 64-K-by-1-bit dynamic random-access memories). In addition to simultaneously performing burn-in and functional tests, **the new system produces data on failing addresses on each chip and the number of errors.** It can be updated to handle 256-K RAMs and other memories such as the byte-wide and nibble-wide devices, read-only memories, and static RAMs. Reliability is aiming Intersect at semiconductor houses and large-volume users of memory. The basic 64-K model Intersect sells for $100,000, with delivery in early 1982.

Instrumentation tape recorders have analog or digital output

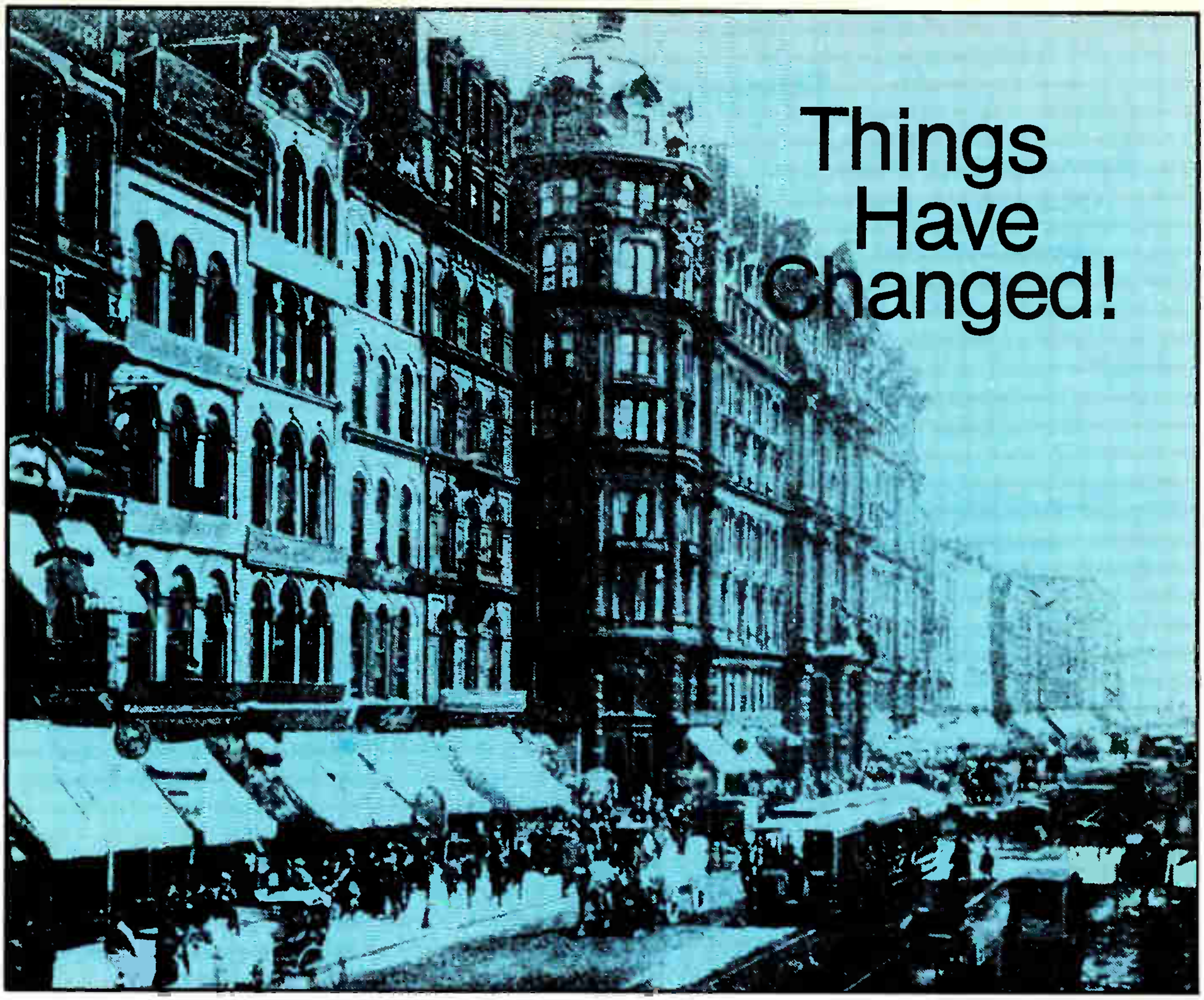
Gould Inc.'s Instrument division is entering the instrumentation tape recorder market with the 6500 series of portable ¼- and ½-in. tape units. Designed to complement the Cleveland-based division's line of oscillograph recorders, the 6500 series features built-in full-function calibration as well as optional plug-in modules for recording multiple-channel analog inputs for playback in either analog or digital form. Deliverable in 60 days, **a basic eight-channel chassis is priced at $8,459** and plug-in modules for fm, direct, or voice record functions are priced at $547, $450, and $230, respectively. The modules can be intermixed in any combination up to eight channels. For digital recording and playback, pulse-code–modulation modules will be available in January at an as-yet undetermined price.

Fiber-optic modem supports 3-mile links

The first major product of newly formed Artel Communications Corp. of Worcester, Mass., is a modem for fiber-optic links, said to be the first such unit compatible with IBM equipment. **Designed to connect IBM's 3258 control unit and 3550 graphics display systems,** the units both enhance communication security when compared with purely electronic modems and allow three-mile separations between control unit and display. The LS-100 modems include remote loop-back testing for full link diagnostics from either end of a cable.

Leadless chip-carriers house microwave driver

The new 207CC from New England Microwave Corp. in Hudson, N. H., may be the first p-i-n-diode driver to be offered in leadless chip-carriers. It **switches in 5 ns,** typically, and is for timed-switching, phase-shifter, or modulator applications. The devices are compatible with TTL levels and put out 70 mA.



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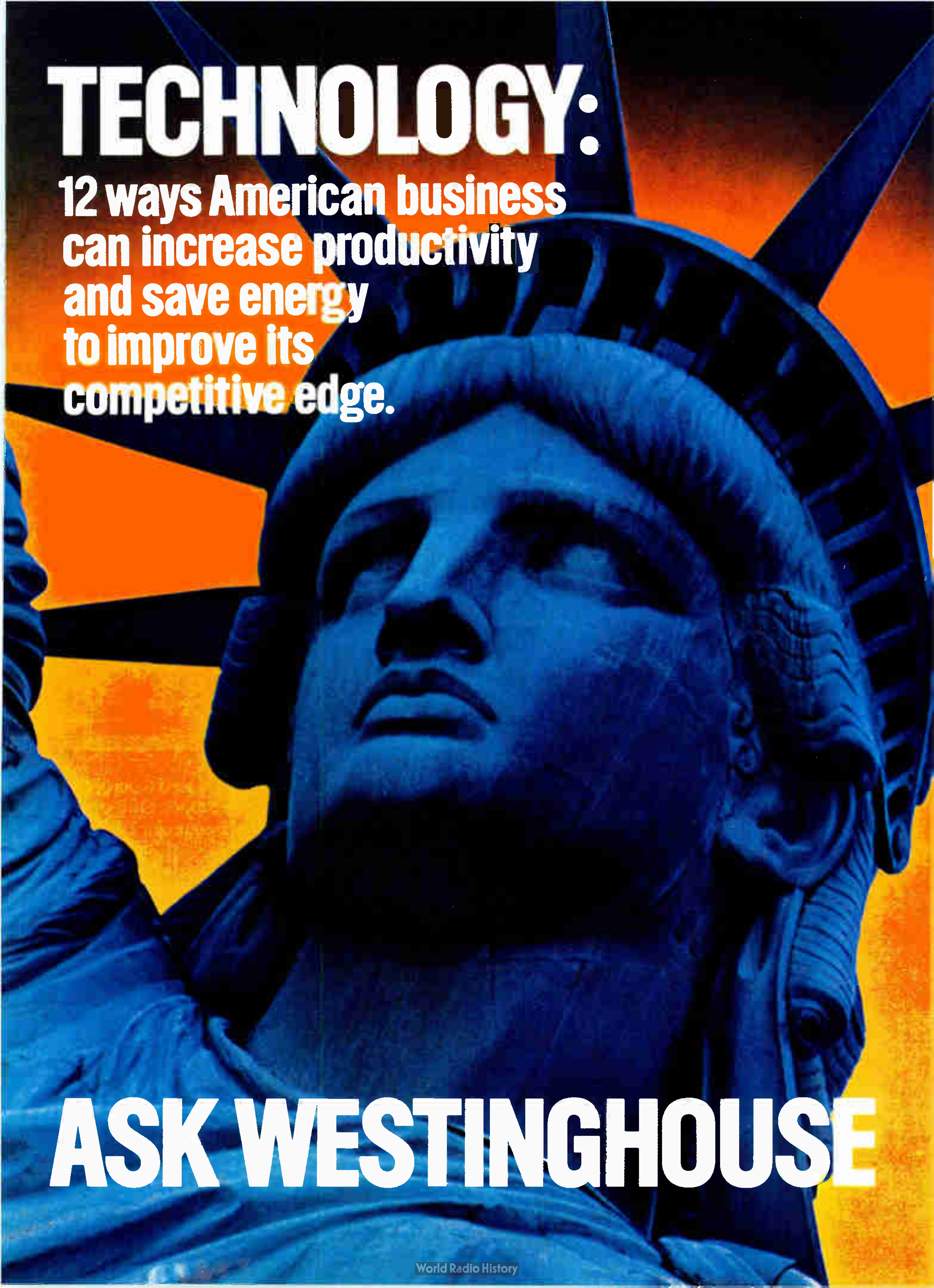
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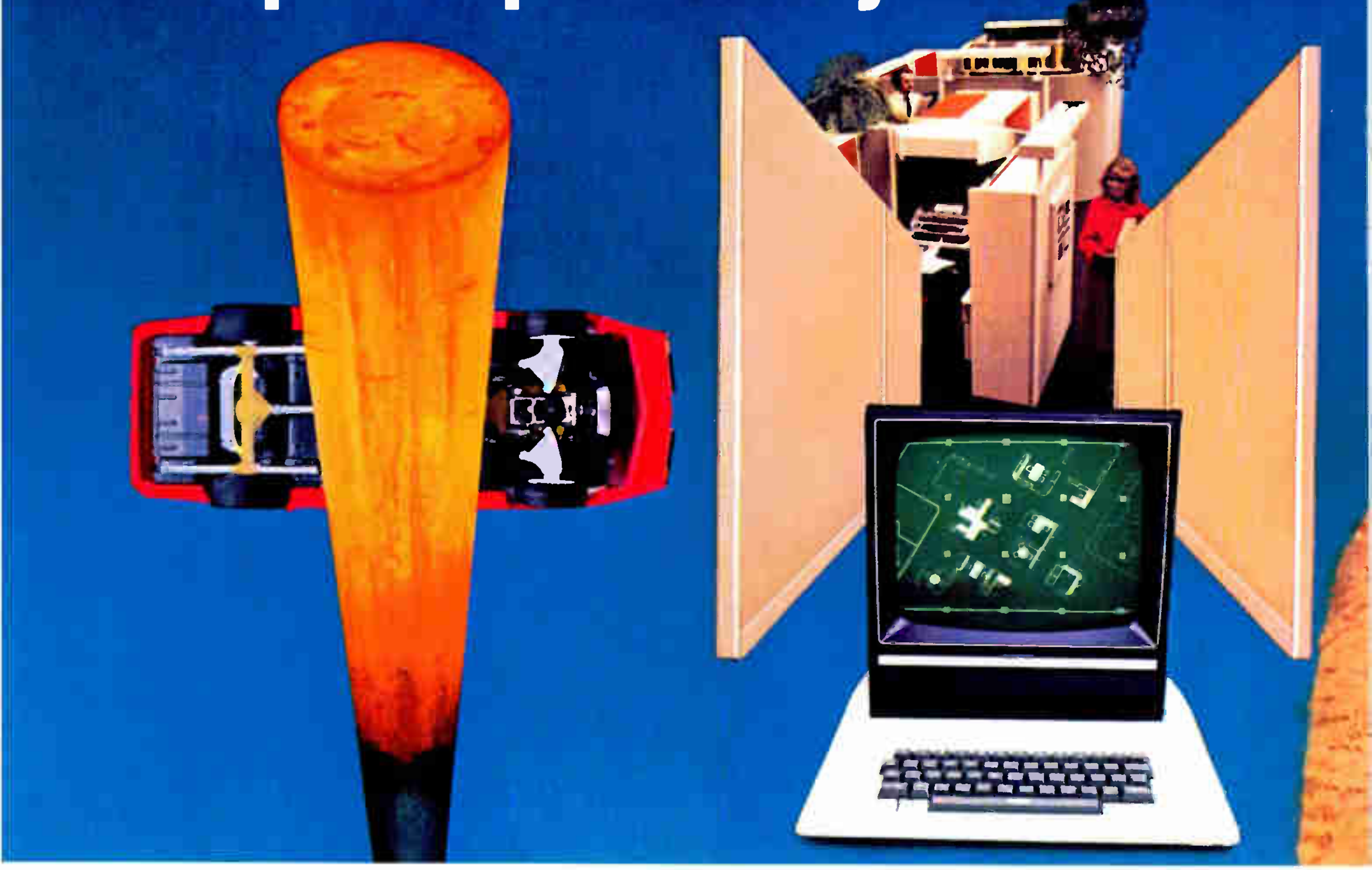


Precision Heating for Metal Processing increased productivity by 300 percent and cut energy costs by 50 percent for a forging facility.

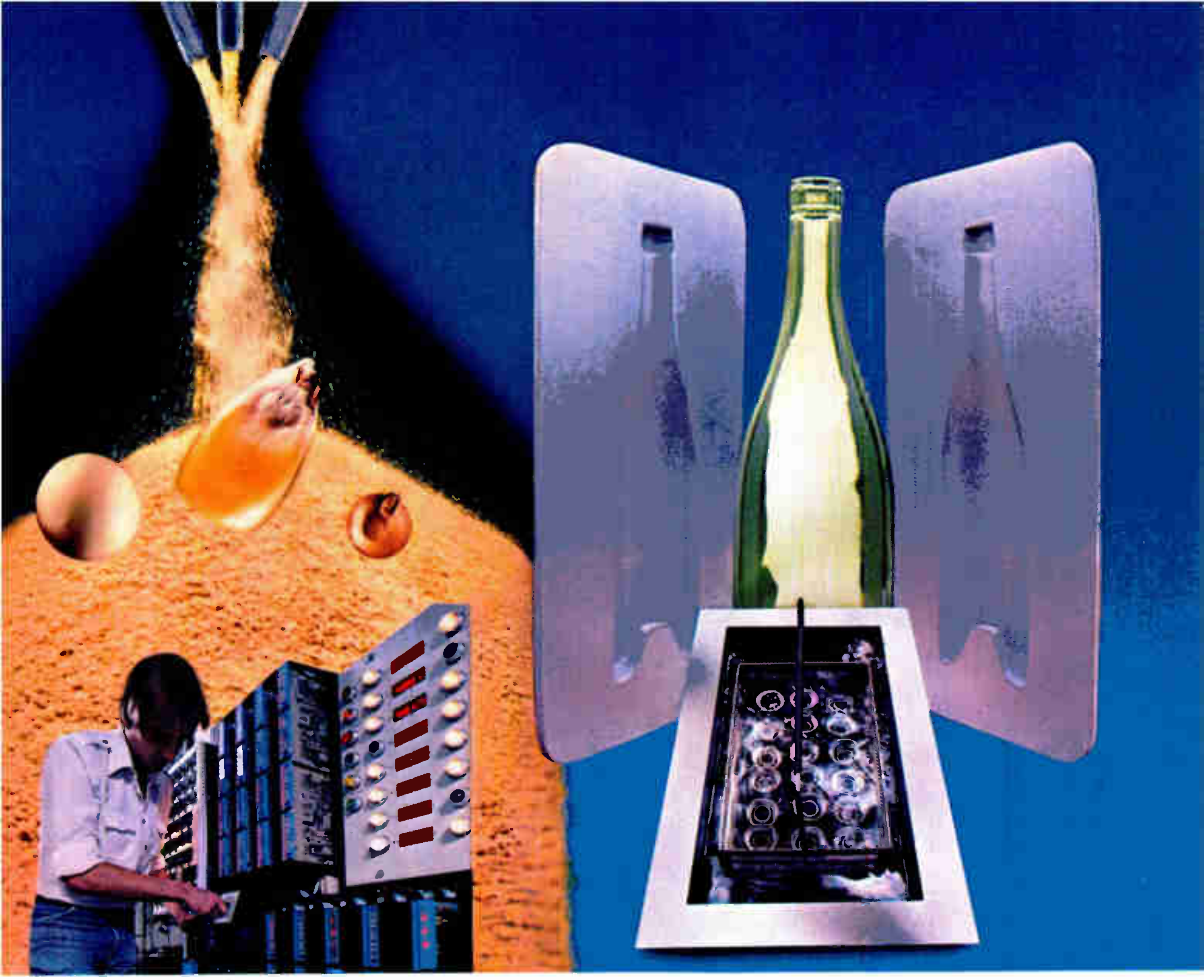
The Westinghouse induction heating system is so much faster than any type of surface heating, it enables the forge to produce parts at three times the old rate. That's because the controlled electric current flow within the bar stock heats to the precise depth required.

Such controlled heating from within significantly reduces the energy waste that accompanies surface heating. It also means an improved environment for employes involved with forging, forming, rolling, heat treating or curing of coatings.

Office productivity increased 6 percent when a Westinghouse "Open Office" System was installed by a major Eastern bank.

"Open offices" improved communications, provided efficient work stations and lowered noise levels for the bank's programmers and analysts. Productivity increased almost overnight.

Today, white collar employes represent half of the American work force, but white collar productivity has increased only 0.4 percent per year in the last five years. Installing "open offices" by Westinghouse can improve those figures.



Microprocessor-based production control increased productivity 300 percent for an agri-business.

A Westinghouse Numa-Logic™ PC-700 programmable controller system replaced manual batching. Now a single 8-hour shift can mix 720 tons of 30 different types of feed requiring 41 separate ingredients. With only a 1 percent weight error in a given ingredient.

Before Numa-Logic, the same output required two 12-hour shifts, and there was a 20 percent weight error.

The Westinghouse Numa-Logic can increase productivity in a wide variety of process and manufacturing operations.

Ultrasonic Cleaning and Degreasing increased productivity by over 900 percent for a manufacturer of iron molds.

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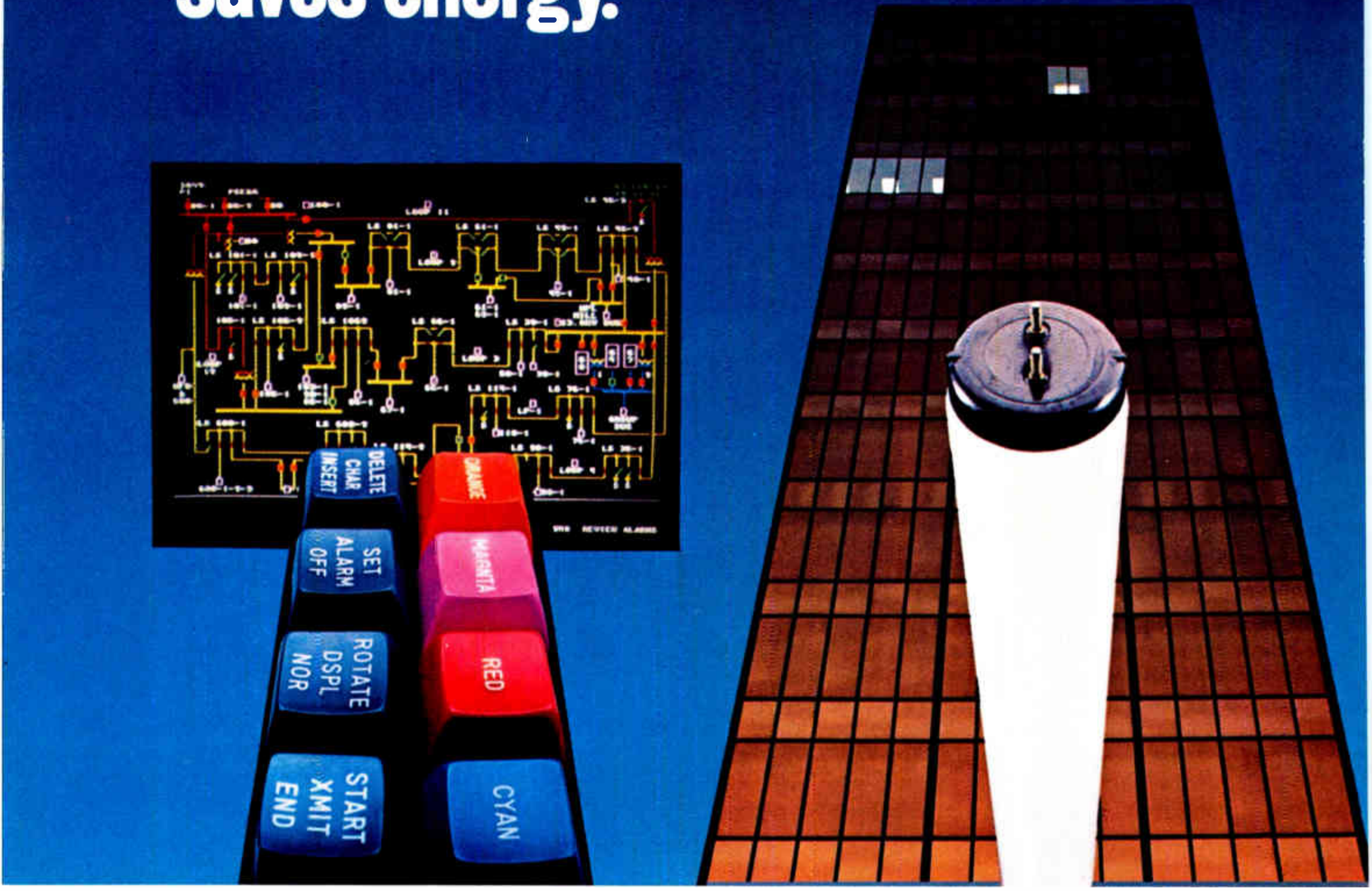
Westinghouse Ultrasonic Cleaning does a faster, more thorough cleaning job than any other method. Using less harsh chemicals and no elbow grease, high intensity sound waves implode small vapor bubbles that blast off dirt and residue.

If cleaning has been your productivity bottleneck, ultrasonics could be the answer.

Westinghouse technology saves energy.



Energy Management will save over $800,000 per year in fuel consumption and labor costs for a 600-acre, 150-building chemical plant.

A Westinghouse Industrial Energy Management System replaced the plant's slower, traditional ways of monitoring and adjusting energy generation and use.

Now, over 1,800 sensors provide the central computer with continuous data for real time analysis of the entire plant's energy generation, distribution and process systems.

Result: Any deviation from optimum operational levels–anywhere–can be spotted and corrected in seconds. By one operator. At the press of a button.

Illumination costs were cut $233,000 per year for a 22-story bank.

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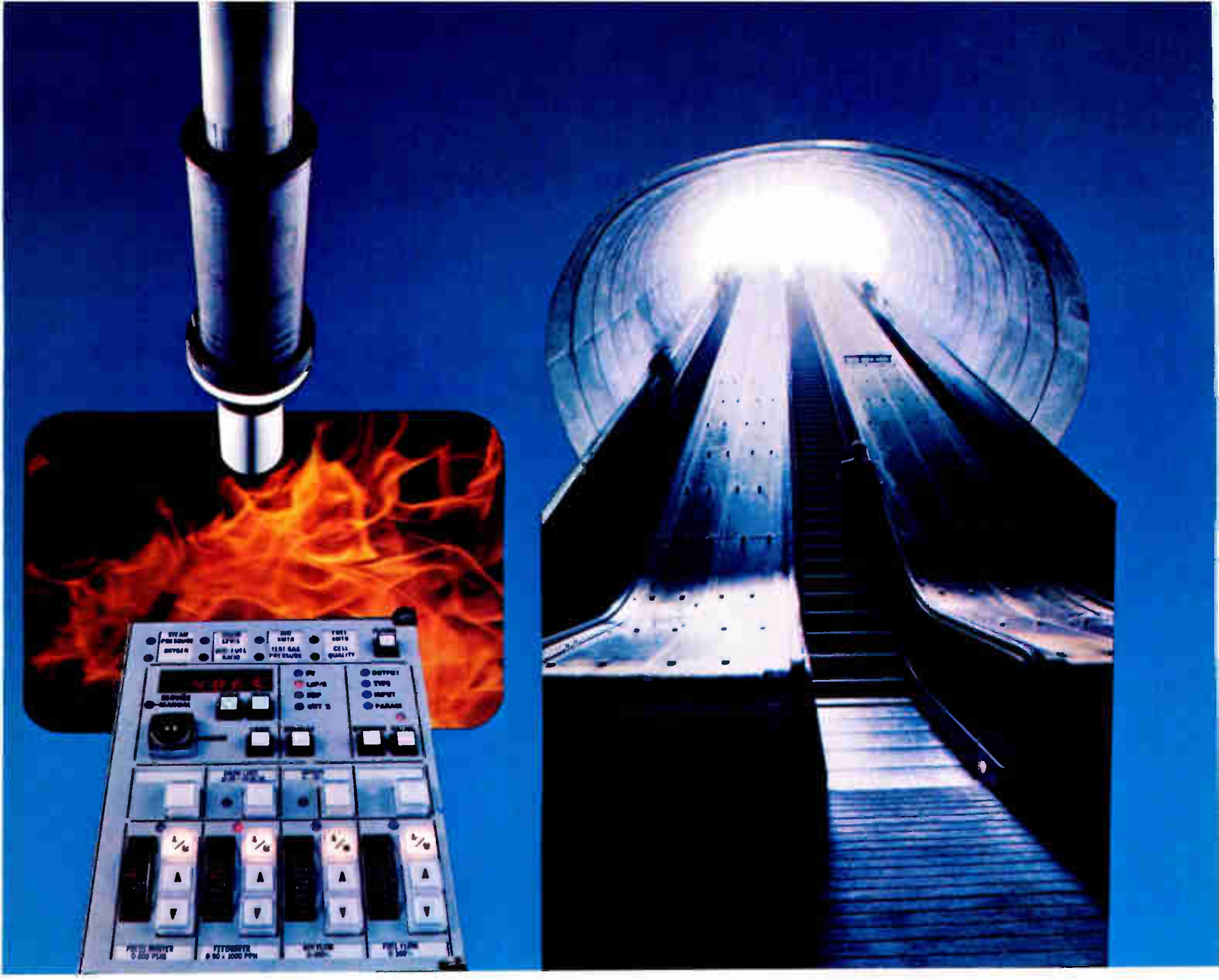
Two Westinghouse Ultralume Fluorescents provide the bank with a lighting environment which the employes agree compares to four standard fluorescents while using only half the electricity.

The bank has since installed Ultralumes in two other facilities. And is saving an additional $84,000 annually as a result.



Combustion Control has cut the fuel bill of an Eastern chemical company 15 percent, saving it $75,000 per year.

The company installed a Westinghouse fully automatic boiler system on one of its four boilers.

Combining a probe-type oxygen analyzer with a microprocessor-based oxygen trim controller, the system optimized fuel consumption, increased safety, and decreased excess oxygen by 8 percent.

It has been so impressive that the company has ordered similar equipment for its three other boilers.

Modular escalators will save over $150,000 per year in energy costs for the mass transit system of a major East Coast city.

The 354 Westinghouse Moduline 100® escalators used there save 30 percent of energy costs when going "up," 60 percent when going "down" compared to the conventional type.

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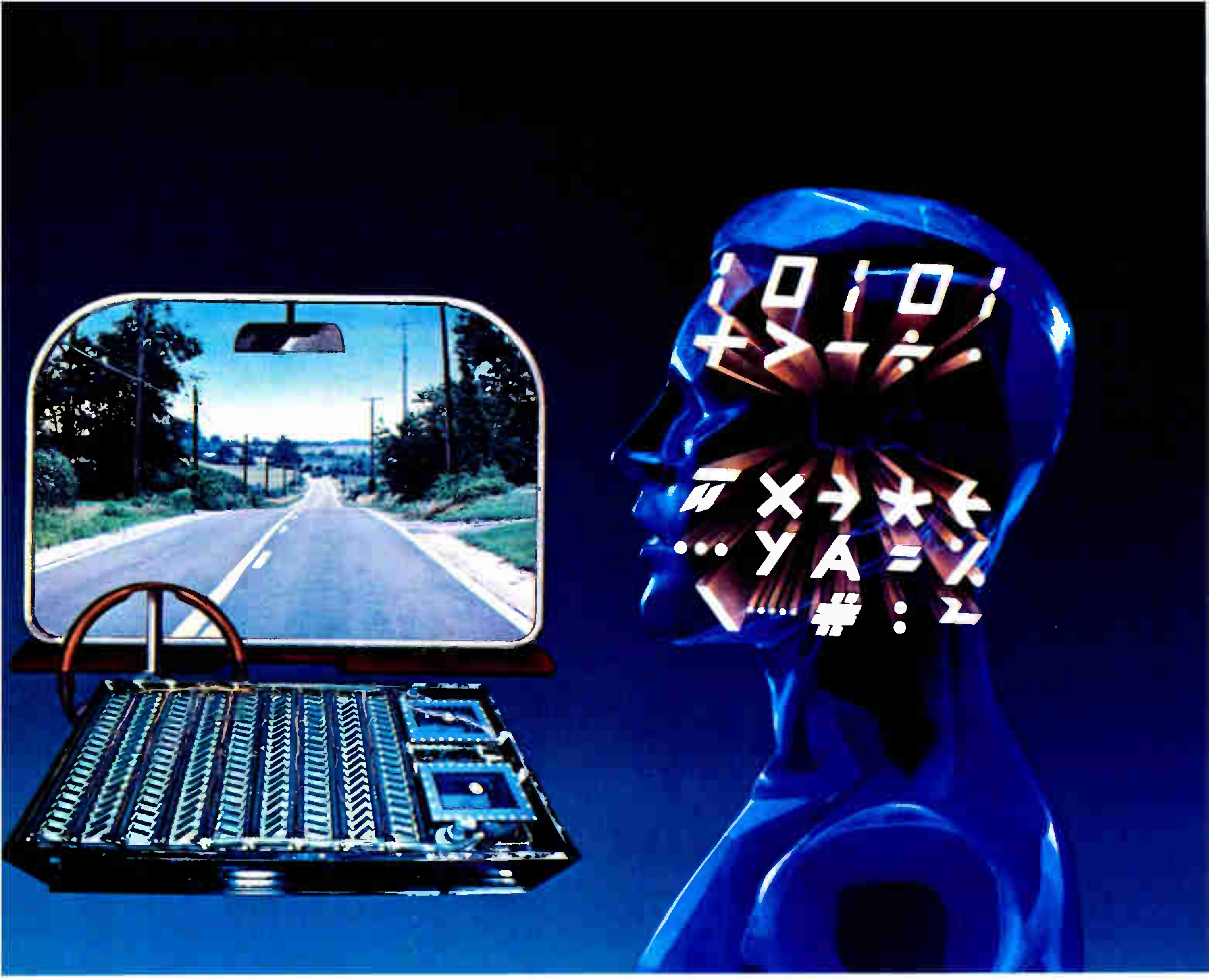

High Power Battery technology may soon give commercial vehicles such as delivery vans a 100-mile cruising range, take only 4 to 6 hours to recharge, and last 100,000 miles.

Westinghouse is developing a high power nickel-iron battery that offers the best combination of high energy density, long life cycle, longer time between charges and competitive life cycle costs.

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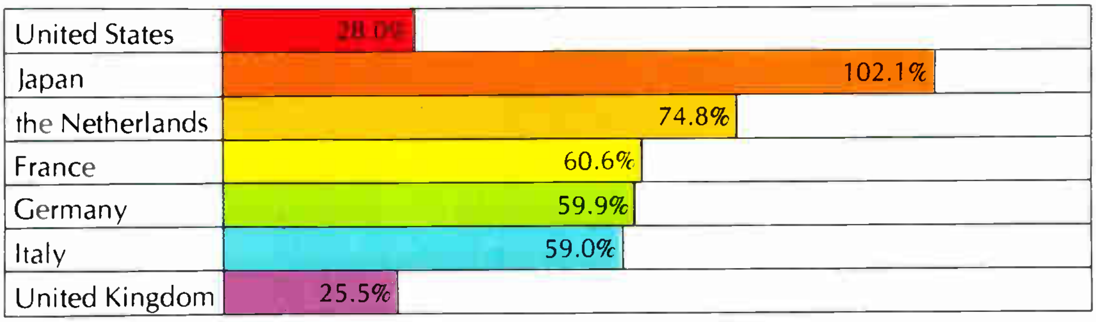

Source: Based on most recent data from the Bureau of Labor Statistics, United States Department of Labor, June, 1981

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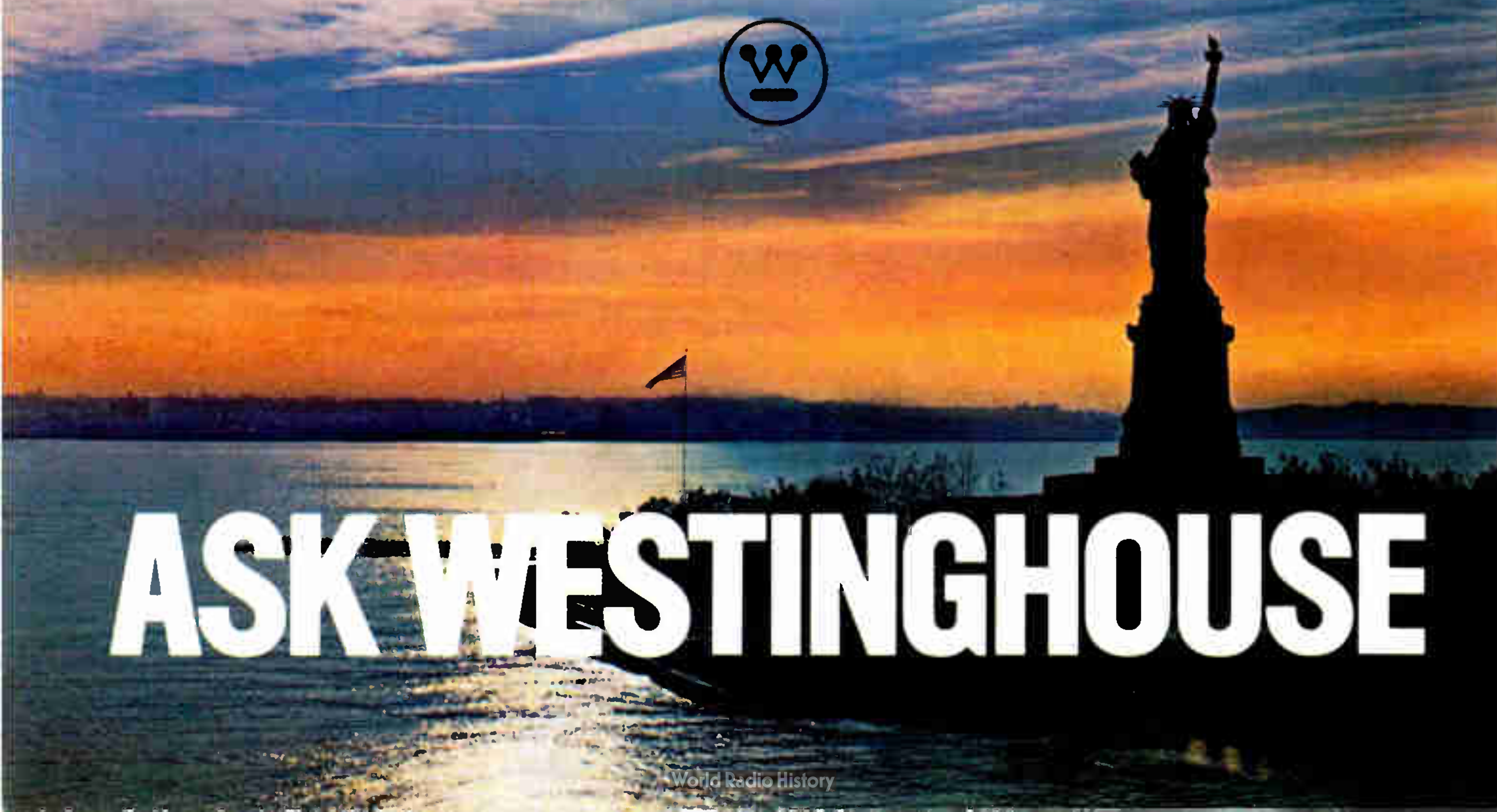

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Recessed Downlight Floods		
44 75R30/FL	____	____
52 150R/FL	____	____
Incandescent Bulbs		
60 60 Watt	____	____
68 100 Watt	____	____
PAR-Lamps		
76 150PAR/FL	____	____
84 150PAR/SP	____	____
Mercury		
92 400 Watt	____	____

Now in use	Total Number	
Ballast		
4' F40/RS	____	100
8' F96	____	105
8' F96HO	____	110
8' F961500MA	____	115

My energy rate is $ ___.___ per kilowatt hour (Divide total dollars from your last bill by total kilowatt hours used.) 120

Please send the savings analysis to:

Name ____________ 124
Company ____________ 159
Address ____________ 194
City ________ State ________ 229
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Phone ____________ 269

☐ Please have someone come out and help me fill out this form. 294

____________ 295

Circle 209 on reader service card

Career outlook

Where EE schools are heading

The pressures on U. S. universities to turn out more electronics engineers is mounting. Despite all those rides up and down the demand curve, not to mention the scare stories about EEs driving cabs or selling ice cream, the organizations that compile statistics about the need for professionals are coming up with the same message: the schools are not producing enough graduates to fill the available job slots.

At the same time, the skills demanded of a beginning engineer are more advanced than they were as recently as, say, a decade ago. Take computers. If today's graduate cannot program a computer in at least one language, he or she might as well go back to school—the employers that will accept someone without the skill are few and far between.

The 1982 graduate will also have to feel at home working, not only with discrete devices, but with integrated circuits as well. Finally, an advanced degree is more common than it was, even though it is difficult to rationalize a couple of more years of college when starting salaries are so temptingly high.

The questions that are starting to bedevil engineering school deans, however, is what about the 1990s? How must the college prepare the EE of the next decade?

In the scenic fastness of Ithaca, N. Y., a small town at the southern tip of Cayuga Lake, one of the Finger Lakes, Cornell University's College of Engineering has earned a place among the first rank of such schools. There, engineering dean Thomas E. Everhart has been giving the subject considerable thought. He says, "on the basis of my 20 years as a professor, and not necessarily speaking as Cornell dean, I perceive today's emphasis as being more on design than it was a decade ago. The reason is that a student using chips and a breadboard can make complicated devices, learning optimization and how much versatility is available to him."

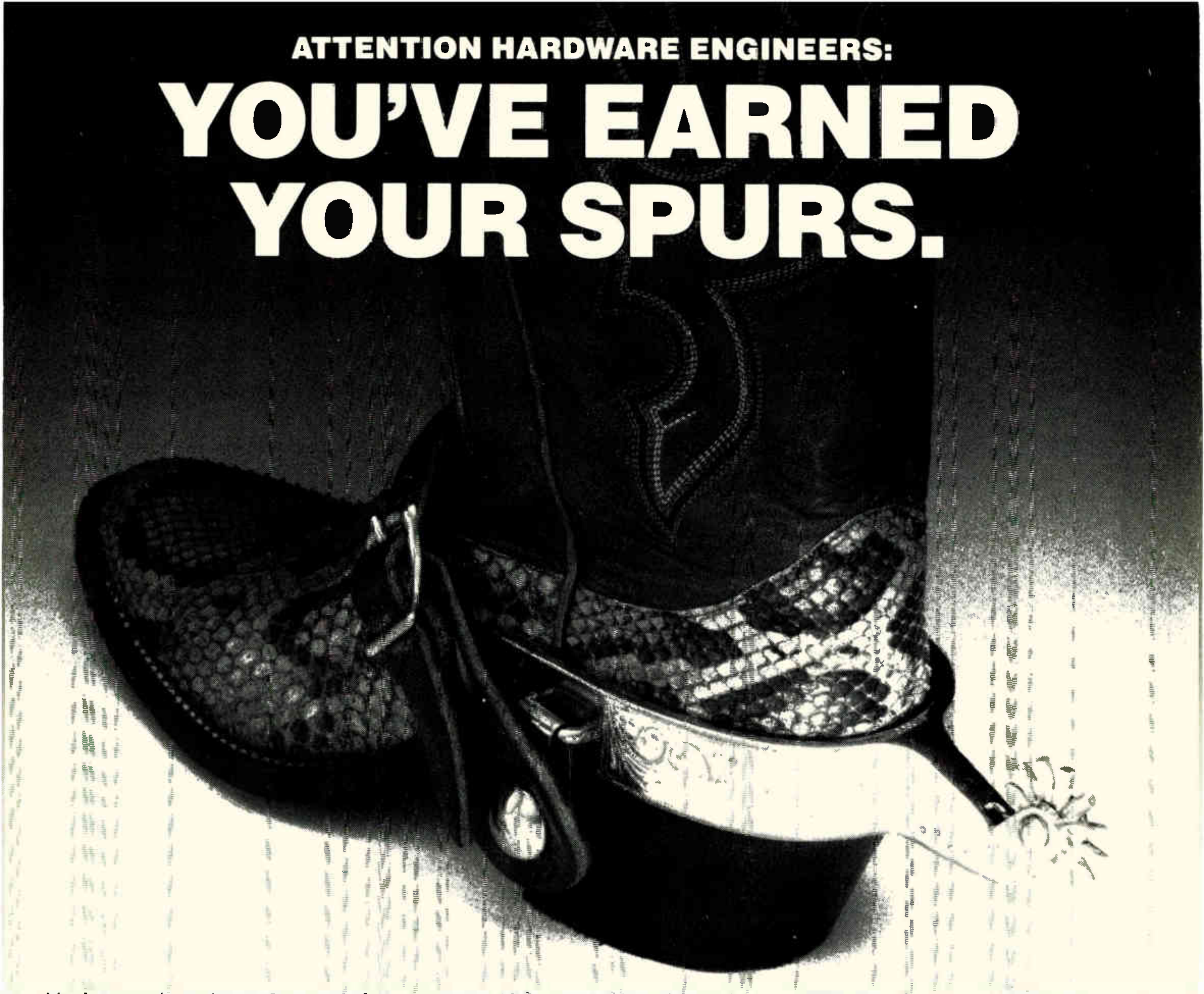
Looking down the road, Everhart says, in the next 10 or 15 years, the world of electronics will experience the development of more powerful and sophisticated computers on a chip. "The cost, however, will equal that of microprocessors when they first came out," he says.

Everhart expects to see some courses on submicrometer structures coming into the curriculum for advanced undergraduates and for candidates for the master's. But, he adds, "basics will still be taught because in the long term, engineers will keep coming back to them even after they enter management. We'll retain our core curriculum of math, physics, some basic chemistry, computers, and some mechanics and mechanical engineering or materials science."

Angstrom angle. Submicrometer structures interest him particularly because on Oct. 16 the university will dedicate its National Research and Resource Facility for Submicron Structures. Having received an initial grant from the National Science Foundation, scientists at Cornell have been working in that realm for four years and recently came up with what they consider the smallest structure ever made: a 15-angstrom line etched by electron beam on a single-crystal substrate. The new building will be attached to the existing engineering building and provide space and equipment for researchers from the university, as well as those from other institutions and companies to work toward fabrication of such ultrasmall devices.

Everhart does not foresee any increase in original research at the undergraduate level "because it takes up too much faculty time, and we are working now to try to use that time more productively." However, Cornell does permit undergraduates to help faculty members with their research and thus earn credits.

But whatever happens 10 years from now, he notes that the proportion of EE candidates in his undergraduate student body—limited to 2,250—is increasing. "We now have 30% of the students working toward their EE degrees, which is more than there were when I came to Cornell from Berkeley two years ago."



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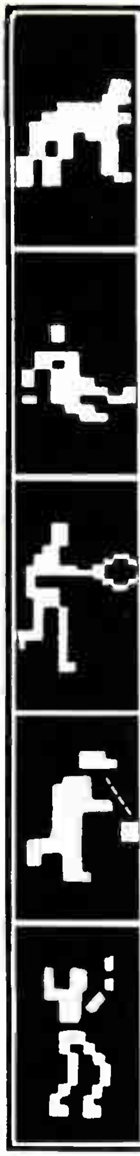

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Market managers:
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Semiconductors: Norman Rosen, Los Angeles

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Cleveland, Ohio 44113: John Uphues
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3000 N.E. 30th Place, Suite #400
[305] 563-9111
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1221 Avenue of the Americas
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4 Gateway Center, [212] 997-3617
Chicago, Ill. 60611
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Southfield, Michigan 48075: Jack Anderson
4000 Town Center, Suite 770, Tower 2
[313] 352-9760

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[713] 462-0757
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3200 Wilshire Blvd., South Tower
[213] 487-1160
Costa Mesa, Calif. 92626: Edward E. Callahan
3001 Red Hill Ave. Bldg. #1 Suite 222
[714] 557-6292
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Larry Goldstein, Lauren Scott
1000 Elwell Court, [415] 968-0280

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34 Dover Street, London W1
Tel: 01-493-1451
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and Simon Smith
Kungsholmsgatan 10
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Carol Gallagher
Production Manager
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Betty Preis
Production Manager Domestic
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