AUGUST 25, 1981

GETTING A PIECE OF THE VENTURE CAPITAL BOOM/94

New concepts in local network architecture/119

Wescon: a sellout once more in its third decade/154

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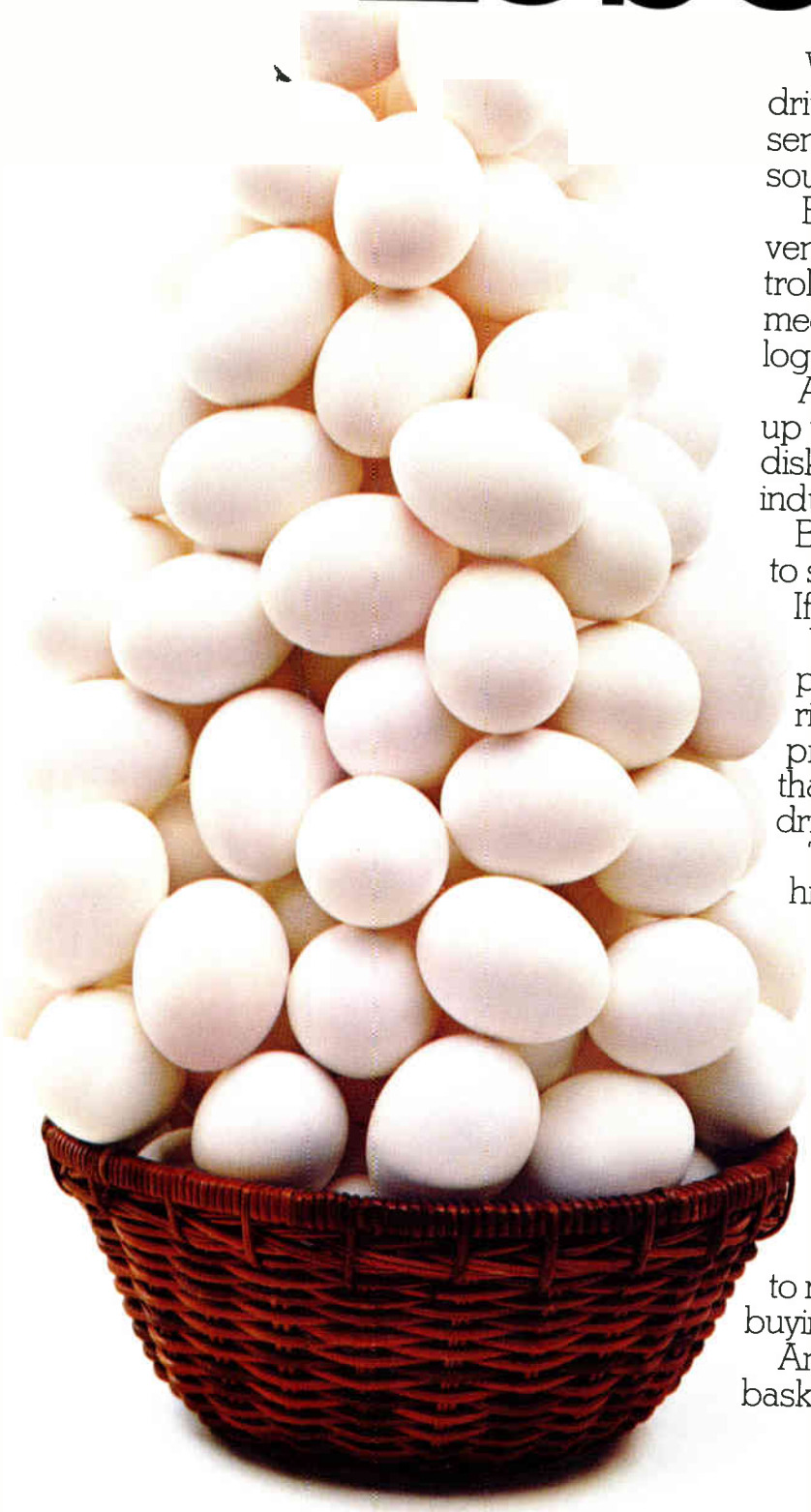
Electronics International

TRANSFORMER GOES PLANAR WITH THICK FILMS

OUR PHILOSOPHY:



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Electronics
The International Magazine of Electronic Technology
Vol. 54, No. 17 • August 25, 1981

Electronics

Highlights

Cover: Hybrid amplifier has thick-film transformer, 113

Thick-film technology has progressed to the point where it can produce flat-spiral windings for a compact, easily reproducible, low-cost transformer. The new circuit is the heart of a hybrid isolation amplifier, and its tight windings make for a wideband response.

The cover illustration is by Ron Chironna.

Snaring venture capital: what the entrepreneur must know, 93

In the booming electronics industries, start-ups are legion, but would-be entrepreneurs must compete for backing from venture capitalists. The good news is that the money is there; the bad news is that a good product idea is only the beginning of the effort to secure backing. This Inside the News reports on what the financiers look for before deciding to back a new firm.

Local networks extend their scope, 119

The use of local networks to tie together computing equipment is an idea whose time has come. Two related articles discuss a proposed six-layer local-net standard in which the first two layers are equivalent to the entire Ethernet scheme (p. 120) and introduce a low-cost network for personal computers in the office (p. 125).

8-bit microprocessors get memory management, 134

A memory management unit on a chip boosts the address limit of 8-bit microprocessors from 64-K bytes to 2 megabytes by widening the processor's 16-bit address to 21 bits. It also facilitates multitasking by providing separate register sets for the various users.

Board density jumps six times with leadless parts, 137

Leadless passive components and chip-carriers can boost packing density six times on printed-circuit boards. The approach is a cost-effective alternative to large-scale integration and hybrid technology for low-volume systems—in avionics applications, for example.

It's life on the fast track at this year's Wescon show, 154

The biggest San Francisco edition of Wescon yet will open its doors Sept. 15 with a full range of technical papers and a number of significant product announcements. This rundown on the technical sessions is followed by a report on product introductions, beginning on page 169.

In the next issue . . .

An operating system on silicon . . . a controlled-impedance wiring technique . . . designing logic arrays remotely . . . an update on surface-acoustic-wave devices . . . motor-control chips.

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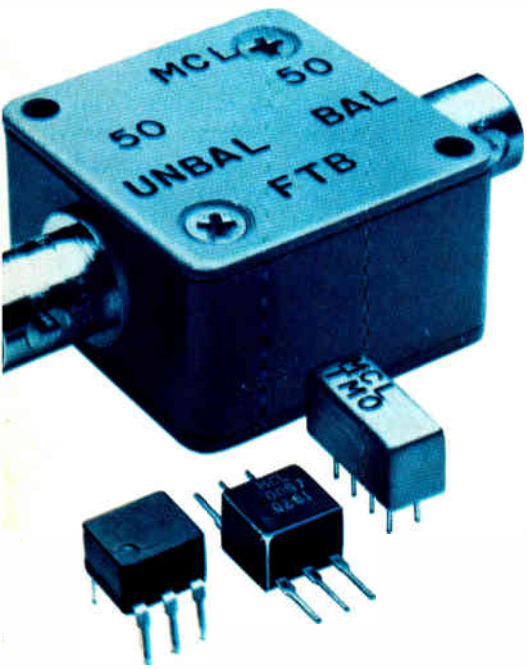

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Imped. Ratio	1	1	1.5	2.5	4	9	9	16	16
Freq. (MHz)	.15-400	8-300	.1-300	.01-100	.02-200	.15-200	2-90	.3-120	7-85
T Model (10-49)	$2.95	$4.95	$3.95	$3.95	$3.95	$3.45	$5.45	$3.95	$5.95
TMO model (10-49)	$4.95		$6.75	$6.45	$6.45	$6.45		$6.45	

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Imped. Ratio	1	2	2.5	3	4	4	5	13
Freq. (MHz)	.05-200	.07-200	.01-100	.05-250	.2-350	8-350	.3-300	.3-120
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Freq. (MHz)	.025-600	3-800	2-600	.15-250	.2-150
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Freq. (MHz)	.1-400	.2-500	.01-200	.5-500
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Publisher's letter

The Tax Reform Acts of 1969 and 1976 were prime examples of how misguided legislation can harm industry—particularly high-technology businesses like electronics where high risks and large quantities of start-up capital are required. When those acts doubled long-term capital gains taxes, restricted capital loss writeoffs, and eliminated treating stock options as capital gains, sources of venture capital practically dried up overnight. But when the capital gains tax was greatly reduced in 1978, venture capital suddenly resurged—more than $1 billion now is available, according to those who add these things up.

That tide has launched a whole flotilla of startups in electronics and, being at the center of much of this activity, Martin Marshall of our Palo Alto bureau became fascinated by the forces behind it—the sometimes obsessive drive of the would-be entrepreneur and the sophisticated risk-taking of the professional venture capitalist.

"I wanted to provide a kind of guide for readers who dream about building their own business," says Marty. "And I'm also intrigued by the venture capital community. They're all dynamic, intelligent men—and not just out to make money, but determined to use their money to create something new and important and lasting." You'll find the start of the story on page 93.

At the very least, the development of the hybrid-compatible transformer for Analog Devices' new isolation amplifier that is featured in our cover story (p. 113) is noteworthy in its bringing together of several exacting disciplines. Co-author Delip Bokil cites first the melding of his thin-film skills with co-author Bill Morong's expertise in magnetics.

"We knew we needed a different type of transformer," says Bokil. "The toroidal type is a neat package, but has problems with couplings between windings and is not well suited to production." So Bokil and Morong set out to build a prototype of their design, which required laying out the planar coils.

The next step in the project which began about a year and a half ago, required a ceramic laser-machining process that could later be adapted to tooling for mass production; for this he enlisted the services of Cermalloy Inc., West Conshohocken, Penn., whose Bruce Bertsch assisted in the preparation of substrates, including laying down the inks. "We never used copper before," notes Bokil.

He also wishes to acknowledge the help provided by Ron Overko of Mini-Systems in North Attleboro, Mass. in printing resistors over dielectric on the parent substrate. Finally behind every good engineer there's a good technician, and Bokil's case was no exception: Analog Devices' Jim Flaherty assembled the prototypes "superbly and with much enthusiasm," says Bokil.

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Readers' comments

The old buddy network

To the Editor: A letter published in your June 30 issue ["Amateurs training amateurs," p. 8] criticized the Accreditation Board for Engineering and Technology as "an old buddy network" and implied that ABET and its accreditation processes were exclusively populated by faculty and administrators from engineering colleges.

Beginning in 1977, the Institute of Electrical and Electronics Engineers began a deliberate effort to involve members currently employed by industry in the accreditation process. The Institute's goal was to have one-half of the visitors evaluating programs, for which the IEEE was responsible, be individuals employed by industry or government.

The data for the past few years clearly indicates that the procedures now used by the IEEE are appropriate for encouraging industry involvement in the accreditation process. In 1977, of the 53 visits made to academic institutions, 21 were by industry or government visitors and 32 were by visitors with academic affiliations. In 1978, 27 of 57 visits were by nonacademic evaluators; in 1979, 16 of 32 had participants with industry or government affiliation; and in 1980, 22 of 45 came from outside the academic community.

A further indication of the IEEE's commitment to the involvement of those from industry in the accreditation of engineering programs is the list of individual *ad hoc* visitors from which those participating in visits are selected. For 1981–82, the IEEE list for electrical engineering programs includes 57 individuals whose current employment is with industry or government and 47 individuals whose current employment is with an academic institution. At the present time, most visitors make only one visit per year.

A recent increase in the size of the Engineering Accreditation Commission of ABET (this is the group responsible for the accreditation of engineering programs) allowed the number of IEEE representatives to be increased to four. Of the four, two persons are currently employed by

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Features

COHERENT provides **C** language source compatibility with programs written to run under Seventh Edition UNIX, enabling the large base of software written to run under UNIX (from numerous sources) to be available to the **COHERENT** user. The system design is based on a number of fundamental concepts. Central to this design is the unified structure of i/o with respect to ordinary files, external devices, and interprocess communication (pipes). At the same time, a great deal of attention has been paid to system performance so that the machine's resources are used in the most efficient way. The major features of **COHERENT** include:

- multiuser and multi-tasking facilities,
- running processes in foreground and background,
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- the shell command interpreter—modifiable for particular applications,
- distributed file system with tree-structured, hierarchical design,
- pipes and multiplexed channels for interprocess communication,
- asynchronous software interrupts,
- generalized segmentation (shared data, writeable instruction spaces),
- ability to lock processes in memory for real-time applications,
- fast swapping with swap storage cache,
- minimal interrupt lockout time for real-time applications,
- reliable power failure recovery facilities,
- fast disc accesses through disc buffer cache,
- loadable device drivers,
- process timing, profiling and debugging trace features.

*UNIX is a trademark of Bell Labs

Software Tools

In addition to the standard commands for manipulating processes, files, and the like, in its initial release **COHERENT** will include the following major software components: **SHELL**, the command interpreter; **STDIO**, a portable, standard i/o library plus run-time support routines; **AS**, an assembler for the host machine; **CROSS**, a number of cross-assemblers for other machines with compatible object format with '**AS**' above; **DB**, a symbolic debugger for **C**, Pascal, Fortran, and assembler; **ED**, a context-oriented text editor with regular expression patterns; **SED**, a stream editor (used in filters) fashioned after '**ED**'; **GREP**, a pattern matching filter; **AWK**, a pattern scanning and processing language; **LEX**, a lexical analyzer generator; **YACC**, an advanced parser generator language; **NROFF**, an Nroff-compatible text formatter; **LEARN**, computer-aided instruction about computers; **DC**, a desk calculator; **QUOTA**, a package of accounting programs to control filespace and processor use; and **MAIL**, an electronic personal message system.

Of course, **COHERENT** will have an ever-expanding number of programming and language tools and basic commands in future releases.

Language Support

The realm of language support is one of the major strengths of **COHERENT**. The following language processors will be supported initially:

- **C** a portable compiler for the language **C**, including stricter type enforcement in the manner of **LINT**.
- **FORTRAN** portable compiler supporting the full ANS Fortran 77 standard.
- **PASCAL** portable implementation of the complete ISO standard Pascal.
- **XYBASIC**™ a state of the art Basic compiler with the interactive features of an interpreter.

The unified design philosophy underlying the implementation of these languages has contributed significantly to the ease of their portability. In particular, the existence of a generalized code generator is such that with a minimal effort (about one man-month) all of the above language processors can be made to run on a new machine. The net result is that the compilers running under **COHERENT** produce extremely tight code very closely rivaling that produced by an *experienced* assembler programmer. Finally, the unified coder and conformable calling sequences permit the intermixture of these languages in a single program.

Operating System

In part because of the language portability discussed above, and in part because of a substantial effort in achieving a greater degree of machine-independence in the design and implementation of the **COHERENT** operating system, only a small effort need be invested to port the whole system to a new machine. Because of this, an investment in **COHERENT** software is not tied to a single processor. Applications can move with the entire system to a new processor with about two man months of effort.

The initial version of **COHERENT** is available for the Digital Equipment Corporation PDP-11 computers with memory-mapping, such as the PDP 11/34. Machines which will be supported in the coming months are the Intel 8086, Zilog Z8000, and Motorola 68000. Machines for which ports are being considered are the DEC VAX 11/780 and the IBM 370, among others.

Because **COHERENT** has been developed independently, the pricing is exceptionally attractive. Of course **COHERENT** is completely supported by its developer. To get more information about **COHERENT** contact us today.

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Readers' comments

industry and two are employed by academic institutions. The other participating bodies of ABET have also committed themselves to increased participation by individuals currently employed by industry in the accreditation process and a conscious effort is being made to include representatives from industry as members of all visiting teams.

The facts concerning IEEE participation in the accreditation of engineering programs do not support the criticism by your readers.

E. W. Ernst,
vice president,
educational activities, IEEE,
Urbana, Ill.

Substrate suppliers

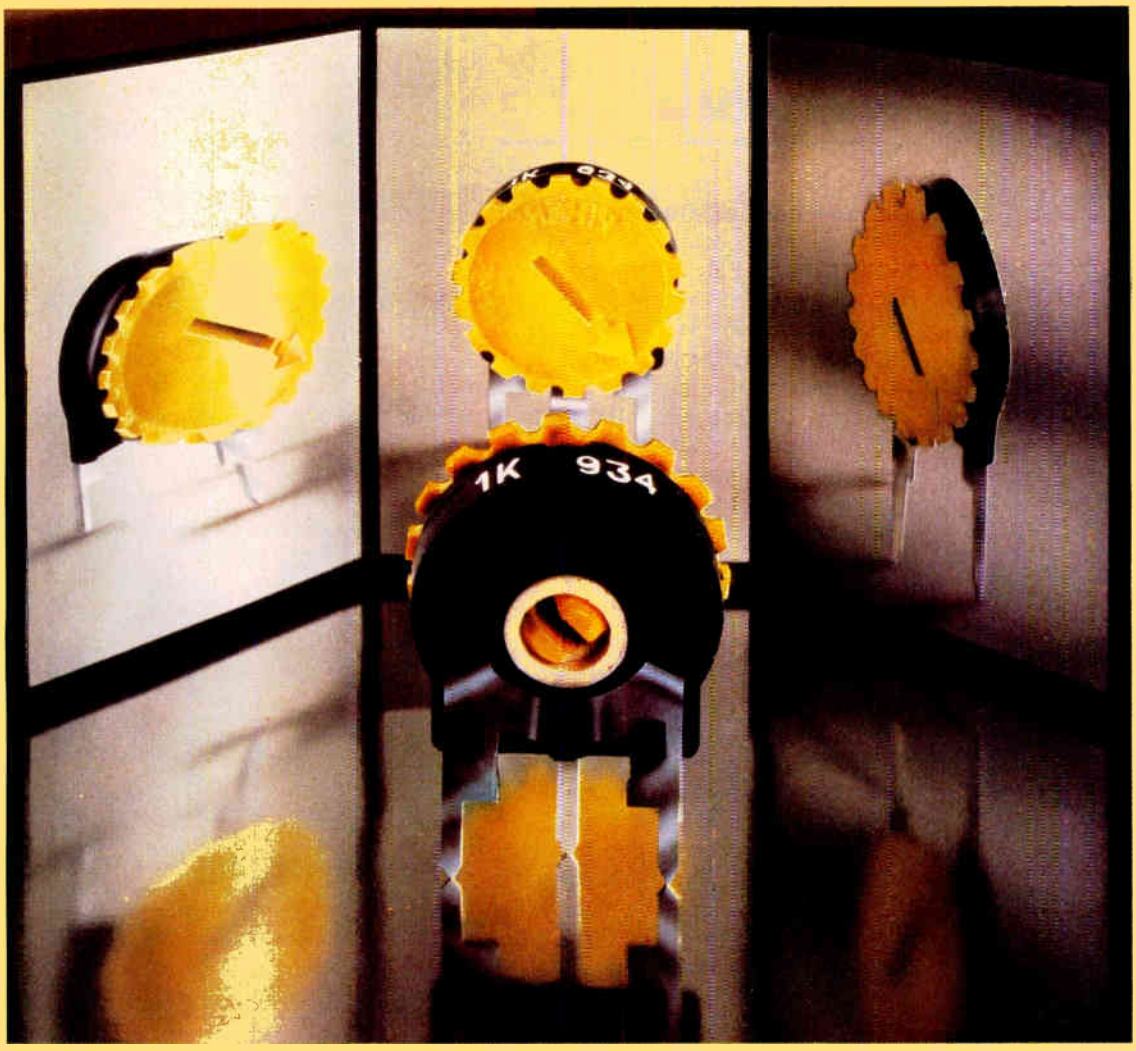
To the Editor: The June 16 issue of *Electronics* ["Copper plus Invar suits chip-carriers, p. 46] reported on Texas Instruments Inc.'s copper-clad Invar substrate material. However, the article seems to suggest that the Metallurgical Materials division is in the process of manufacturing printed wiring boards from this material and, therefore, in competition with the PCK Technology division of Kollmorgen Corp. and Bell Laboratories.

In truth, TI supplies only the clad metal. In fact, PCK Technology has evaluated the material and is now providing it, or Alloy 42, as the metal core in its Microwire development program at the customer's request. Bell Labs in Denver has also used Invar, in conjunction with a modified Lampac approach, and found the material to be acceptable for use with chip carriers.

Francis J. Dance,
program manager,
electronics materials,
Texas Instruments Inc.,
Attleboro, Mass.

Correction

In Figure 2 of "Dual-function amplifier eases circuit design" (July 28, p. 137), the emitter resistor of transistor Q_3 should have a value of 33 ohms, instead of 1 kilohm. Also, the LM329 zener diode shown at the lower left should be connected to the adjacent 3-kΩ resistor.



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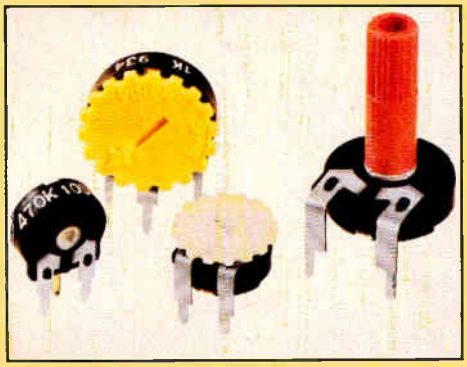

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News update

■ Toshiba Corp. has become pretty seriously involved with the T88000 16-bit microprocessor it unveiled last fall [*Electronics*, Oct. 9, 1980, p. 75]. The high-speed, complementary-MOS-on-sapphire part has already been designed into two medical-electronic products, and half a dozen more new products are in the works.

Moreover, Toshiba says it is designing silicon-on-sapphire chips for other applications and expects to sell them as components by next July. By then, the Japanese firm could also be producing the 4-K SOS static random-access memory for a mainframe cache memory it displayed last year [*Electronics*, Sept. 11, 1980, p. 80]. It has no plans to sell the T88000 separately.

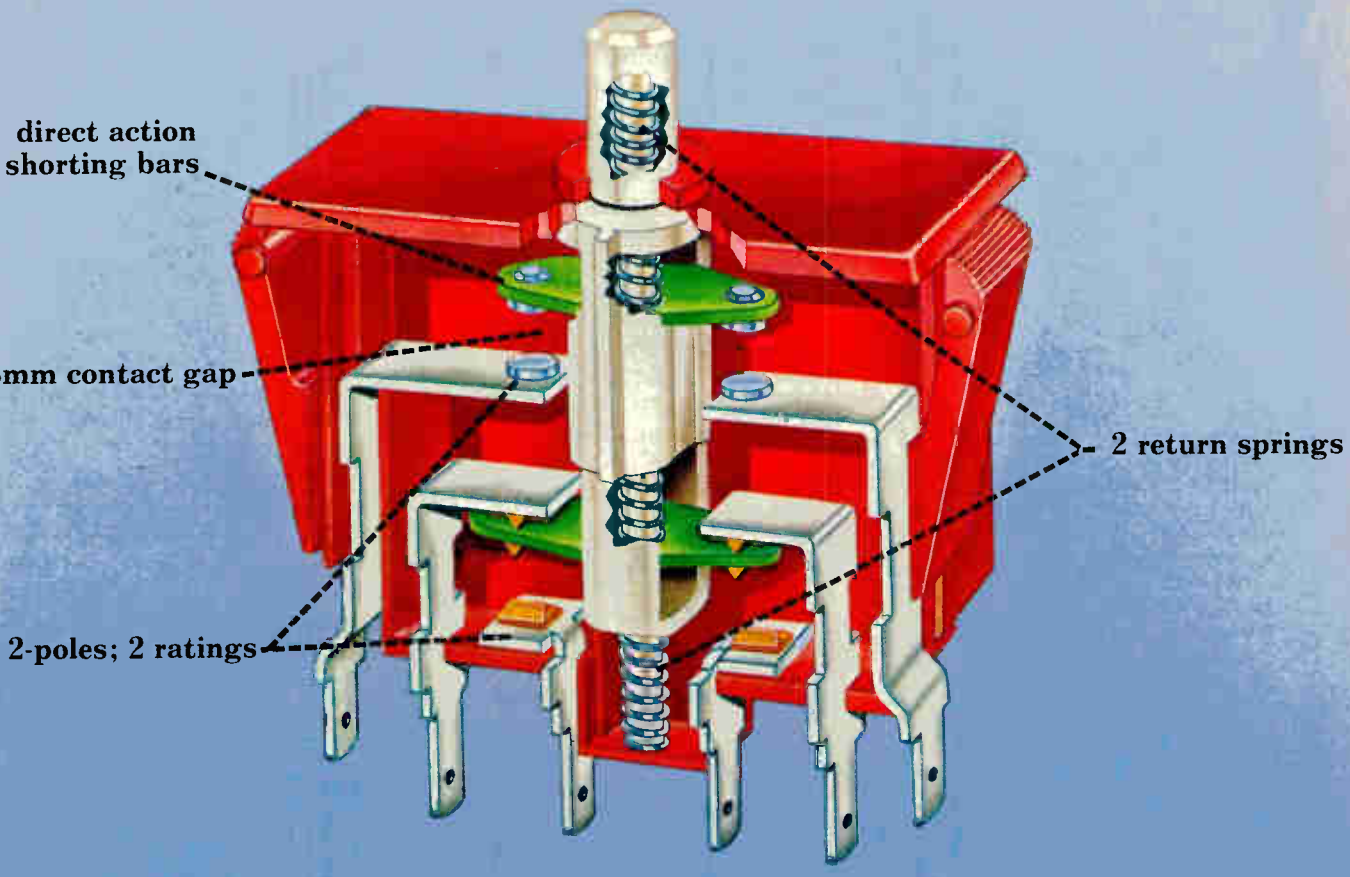
Mixed calculations can be handled three to six times faster with the T88000 than with Intel's 8086 or Zilog's Z8000, according to Toshiba. The clock rate is 10 megahertz, with the SOS technology bringing the average propagation time of a gate down to only 0.7 nanosecond.

With microcode in off-chip read-only memory Toshiba tailors the SOS chip's architecture to suit the application. A floating-point binary architecture is used for scientific products, and a fixed-point binary-coded decimal architecture is employed for office computers and products designed for business arithmetic.

Fast. One of the two products already built around the T88000 is the Tosmac 500 Easy, a medical information terminal. It needs a high-speed processor because it must turn out billing statements rapidly while handling a large pharmaceutical and an even larger patient file. The other product is a computerized tomography system, where the chip handles fast Fourier transforms and instrument control.

The microprocessor will also soon turn up in a rack-mounted minicomputer, in which a single central-processing-unit board will replace five boards. Also coming is an office computer; three desktop systems, including a Japanese-language word processor and a scientific computer; and an English-language word processor. **-Charles Cohen**

LINE-INTERRUPT switch meets latest specs... WORLDWIDE



This new safety interlock switch was designed to meet specs of such international agencies as VDE, BSI and others. U.L. listed and CSA approved.

A redundant switch is a safe switch. Cherry builds double protection into this 3mm contact gap line interrupt switch.

Four contacts on each pole, parallel return springs and direct action shorting bars provide an extra margin of safety.

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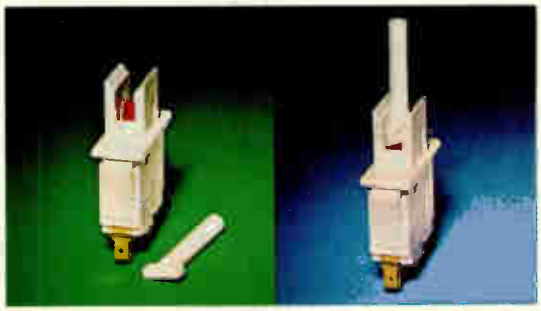

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Circle 13 on reader service card 13

People

Findex's Dashiell strives to do as well at home as abroad

The usual progression for a small microcomputer company in the U. S. is to build a strong domestic sales base, then move into overseas markets. But when George Dashiell took the reins of Findex early this summer, his overriding concern was to bolster domestic sales, until now dwarfed by the firm's 21-country international business.

Not surprisingly, the former vice president and general manager of Computer Automation's commercial division turned to a European product to help him make headway at home. His decision makes his Torrance, Calif., firm the first U. S. licensee of a popular European operating system developed by Holland Automation of Dordrecht. The HA software is used by—among others—the major Italian business-machine maker C. Olivetti & Cie., and by Zilog Inc. for a few systems it sells in Europe but not in the U. S.

Like other firms offering the Dutch software, Findex will sell it under its own brand name, calling its version the Findex Operating System. "We'll offer the operating system as an option. Users can buy either CP/M or the Holland package," the 56-year-old Dashiell says with a trace of a Virginia accent.

He turned to the HA system after seeing the advantages it brought when adapted to a Findex computer sold in the Netherlands—the HA Basic compiler operates at least 25% faster than the compiler based on CP/M, Dashiell notes. Also, HA offers small-business applications packages, thoroughly tested in Europe, written in Basic.

Although Findex has been building systems since 1979 in California, less than 10% of its sales have been in the U. S. Michael Wurmbrand, a Rumanian who started the firm and has since left it, found it easier to sell in foreign markets.

With the two operating systems and a wide range of applications packages to offer, Findex now plans to make its domestic sales equal overseas sales by entering vertical markets like accounting services and medical offices.

Findex sales were $2 million last year, and Dashiell plans to double revenues during each of the next three years. Doing that won't be easy, but he feels confident. "Working a year in this industry is like working five in any other. I've got 150 years' experience," he quips.

At home. George Dashiell seeks to balance Findex's sales at home and abroad.

TI's Rhines sees shorter design-in for 16-bit 9995

Texas Instruments Inc. is already changing some of its views when it comes to design-in cycles for 16-bit microcomputers, says Walden C. (Wally) Rhines, head of the recently created MOS Microcomputers division in Houston.

Until now, says the 34-year-old assistant vice president, the industry and TI have been anticipating lengthy design-in times. But the TMS9995—its speedy n-channel MOS microcomputer aimed at signal-processing applications [*Electronics*, Dec. 18, 1980, p. 90] has apparently shot down that notion at the Texas semiconductor firm.

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Circle 15 on reader service card 15

People

Achiever. He's only 34, but Wally Rhines heads TI's MOS Microcomputers division.

notes the youngest vice president the company has ever had. "We have already won over 50 designs with it, and we are delivering production volumes less than six months after introduction." He thinks that the success came because the 9995's rapid mathematical computations hit a set of user needs that had not previously been addressed and can do so with a three-chip-per-system design at minimum.

He estimates that the microcomputer market, including 4-, 8- and 16-bit units, will grow at an annual rate of 40% during the next five years. To meet this growth, TI is putting all of its microcomputer resources under a single division. The move is part of an effort to "combine support and software development for all TI microcomputers," explains Rhines, who holds a Ph.D. in material sciences and engineering from Stanford University.

The consolidation also was created to facilitate upgrades of 4-bit device users to 8-bit users. But that does not mean the firm is turning its back on the highly successful TMS1000 family.

"We are continuing to introduce new 4-bit products," states the nine-year TI veteran, who first served in the company's Central Research Laboratories in Dallas. After other assignments, Rhines went to Lubbock, Texas, in 1976 to head component design and engineering for consumer products.

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Terminal Strength	± 0.25%	± .05%
Moisture Resistance	± 0.5%	± .05%
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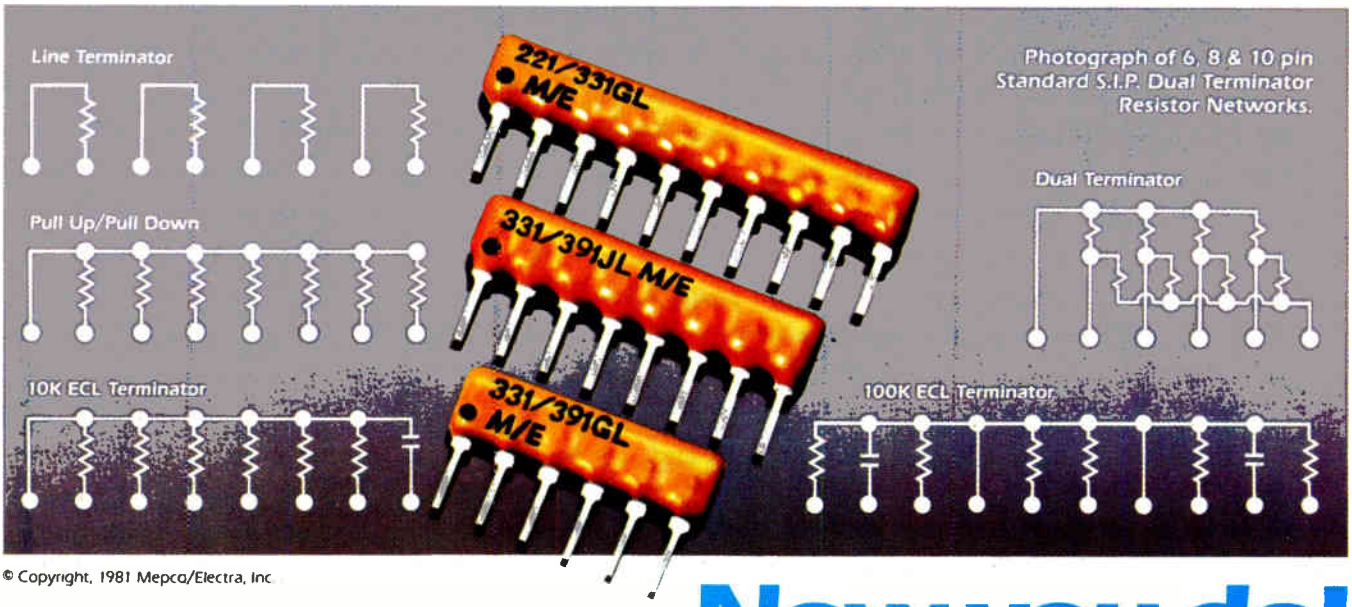

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Back in 1969, when we introduced the world's first integrated 64-bit RAM, we literally started the whole revolution in memory design.

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You know the way it works: we introduce a new memory, and it drives the technology forward. Our microprocessor people take advantage of this new technology. And use it to design new architecture. Which comes full cycle and drives our memory design group, who take the technology even farther forward.

Of course, it really amounts to momentum. And nobody else in the entire industry has the momentum we do.

Or the track record. We brought you the first MOS static RAM. The first integrated dynamic RAM. The first EPROM. The first 16K E²PROM. The first 1 megabit bubble. In fact, of the 31 breakthroughs in VLSI over the last decade, we delivered 24 of them first.

When you get right down to it, nobody else has the breadth we do, either. Our competitors might make memories for a few applications, but only Intel covers the entire scope of microprocessor-based products and gives you memories for every important system application. Commercial and military. Complete with development tools and applications support.

And since we plan to keep coming around full circle this way for years, we've invested an enormous percentage of our profits right back into our design and production capability. So we can deliver all the memory product you need. Right when you need it.

That's the broad picture. Now we'd like to show you product by product, how we're right on the leading edge of memory development.

RAMs

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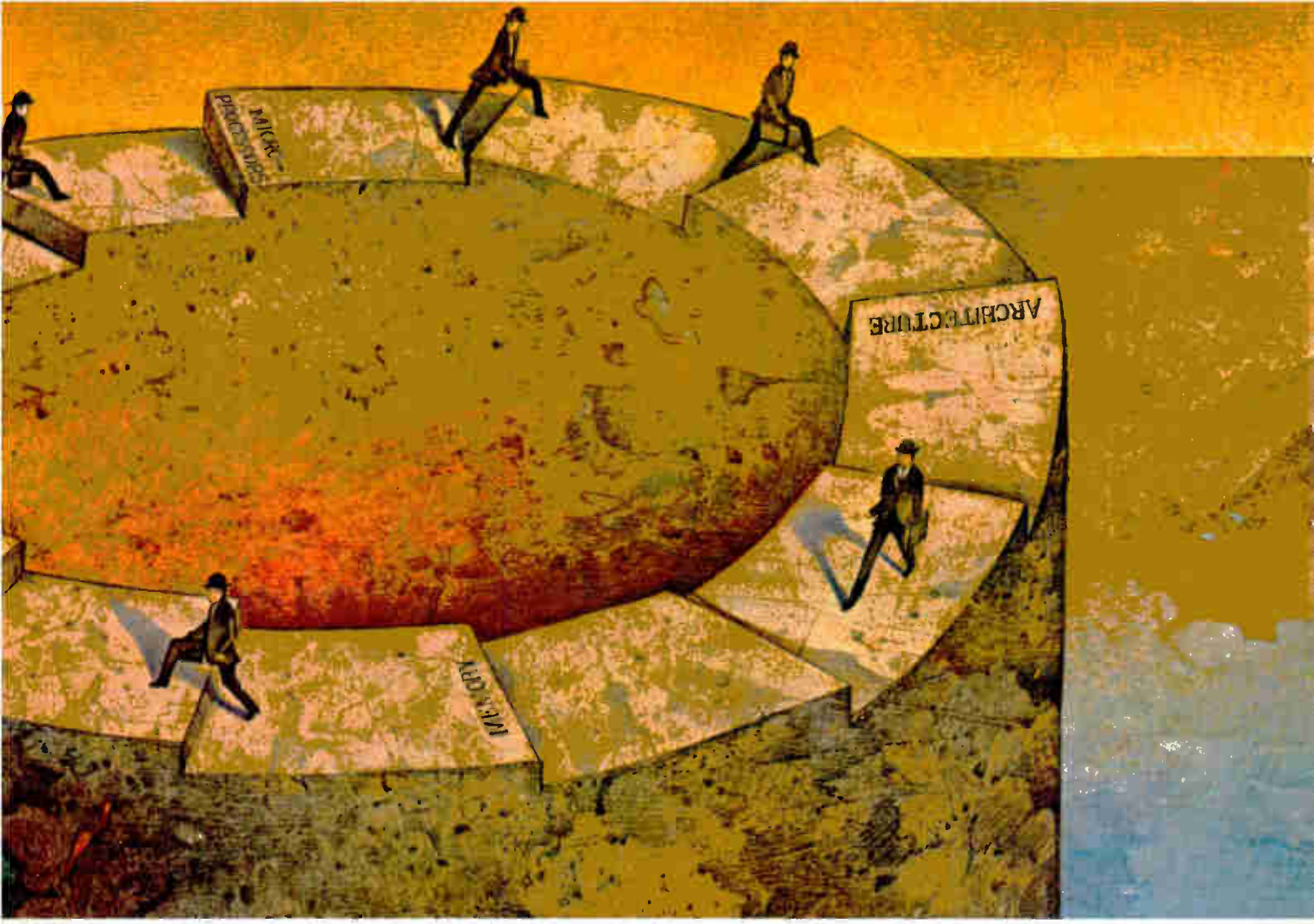

for a real breakthrough only one sensible way to go.

PROMs
Because of our process technology, we've always led the way in faster, denser PROMs, in MOS and bipolar.

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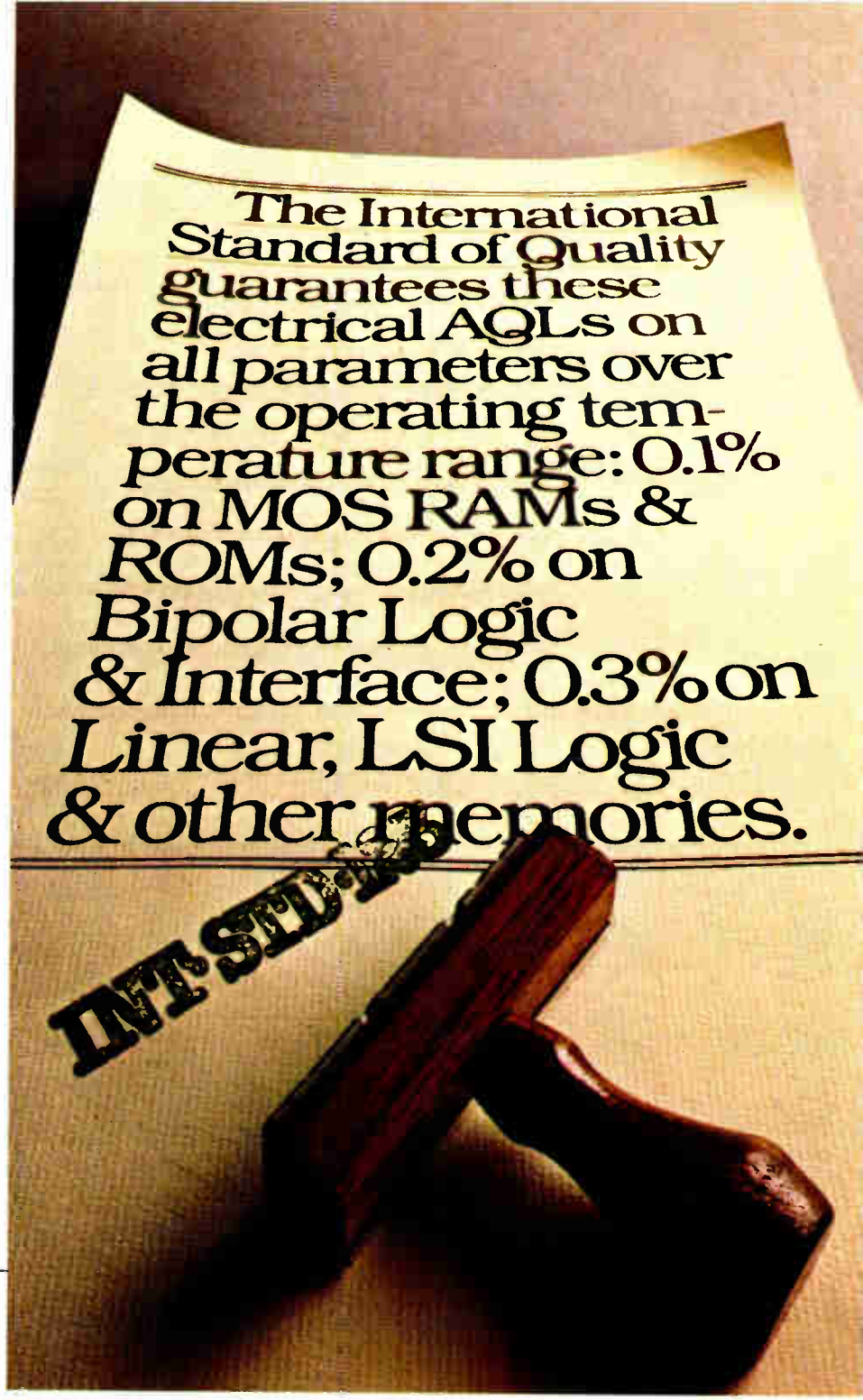

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Editorial

The FAA's sins of omission

August, happily, is not a big month for industry conferences and conventions. But for those few meetings that were scheduled, registrants formed long lines at public telephones during coffee breaks in the attempt to book a seat on a departing flight. That has been one of the small but personally most irritating consequences of the strike of the Professional Air Traffic Controllers Organization.

More important to the nation at large will be the repercussions on U. S. airlines and the aircraft and avionics manufacturers that supply them. The carriers posted large losses in 1980 and in the first quarter of 1981, and their shaky economic position is being made still shakier by the Patco walkout. Reported revenue losses are running between $20 million and $30 million daily.

For the makers of commercial aircraft and their engines and avionic systems, the crunch has yet to come. But it will. These manufacturers expect that airlines will begin calling later this year either to defer delivery of new planes or to cancel some orders altogether.

It could be an example of ricochet economics at its worst. Some Reagan economic advisers fear the decline of this business could compound the problems of the general economic downturn that has already been forecast for the remainder of this year and so extend it further into 1982.

The pathetic part of all this is that the strike need not have happened at all if the Federal Aviation Administration had lived up to its repeated pledges to upgrade and automate the nation's air-traffic control system. That would have reduced the need for many of the controllers, for available electronic technology can perform at least as well and probably better many of the functions they now perform manually. Yet the FAA, like some of its other Federal counterparts, has been long on promises and short on performance.

The FAA, gripes one system planning staffer, "does a great job when it comes to planning systems for use in the next decade, but it never gives much thought to today's problems or tomorrow's crisis. In the '60s we had great plans for the '70s. In the '70s we talked about the '80s. Today we are planning for the '90s."

Congress, too, has long been unhappy with FAA performance. As each new FAA administrator—backed up by the same old bureaucrats—has pleaded for funds to perform some technological magic on the air-traffic control system a decade hence, most Congressmen simply yawn. They have heard it all before.

The truly bad news is that the problem is unlikely to improve under the Reagan Administration as it continues to search for new ways to cut Federal spending and bring the budget into balance over four years. The FAA is a prime target in what is becoming a Catch-22 situation. For as the Patco strike reduces airline revenues, their taxable income will also decline, reducing Federal revenues even further and thus forcing even steeper cuts.

Laboring under that gloomy forecast, the outlook is discouraging at best for the FAA's automated en-route air traffic control system. Another 10-year effort with an estimated $2.8 billion pricetag, AERA lumps together almost every conceivable subsystem imaginable, from a nationwide digital data net to doppler weather radars, microwave landing system and a collision avoidance system in every airplane cockpit [*Electronics*, Dec. 8, 1980, p. 48]. If those sound familiar it is only because they represent what the FAA has been studying and restudying for years.

If President Reagan and Secretary Lewis truly intend to rebuild the air-traffic control system as they say they are, then they must not stop at retraining a whole new crew of controllers. The whole FAA bureaucracy needs rebuilding, with emphasis on finding ways to move new technology into the system rapidly before problems become crises.

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Meetings

Compcon 81 Fall—22nd IEEE Computer Society International Conference, IEEE (Victor Basili, Department of Computer Science, University of Maryland, College Park, Md. 20742), Capitol Hilton Hotel, Washington, D. C., Sept. 15–17.

Wescon/81, IEEE (Electronic Conventions Inc., Suite 410, 999 N. Sepulveda Blvd., El Segundo, Calif. 90245), Brooks Hall, Municipal Auditorium, and Hilton Hotel, San Francisco, Sept. 15–17.

31st Annual Broadcast Symposium, IEEE (R. A. O'Connor, CBS-TV Network, 51 W. 52nd St., New York, N. Y. 10019), The Washington Hotel, Washington, D. C., Sept. 16–18.

ISS '81—International Switching Symposium, IEEE (General Secretariat-ISS, Box 56, Station Ile des Soeurs, Verdun, P. Q. H3E 1J8, Canada), Hotel Bonaventure, Montreal, Canada, Sept. 21–25.

Semicon/East '81, Semiconductor Equipment and Materials Institute (625 Ellis St., Suite 212, Mountain View, Calif. 94043), Hynes Auditorium, Boston, Mass., Sept. 22–24.

7th European Solid-State Circuits Conference, IEEE, Convention of National Societies of Electrical Engineers of Western Europe (Bernd Hoefflinger, University of Dortmund, P. O. Box 500500, D-4600 Dortmund 50, West Germany), University of Freiburg, Freiburg, West Germany, Sept. 22–24.

Electrical Overstress/Electrostatic Discharge Symposium, IIT Research Institute (Nan Pfrimmer, Rome Air Development Center/RBRAC, Griffiss Air Force Base, N. Y. 13441), Aladdin Hotel, Las Vegas, Sept. 22–24.

National Conference on Software, Commission on Software Issues in the '80s (U. S. Professional Development Institute, 12611 Davan Dr., Silver Spring, Md. 20904), Shoreham Hotel, Washington, D. C., Oct. 5–6.

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Through the use of LSI high-speed modem, the NEFAX-6500 can transmit a standard "A4" size page in 20 seconds—and through ultrahigh-speed mode in 10 seconds.

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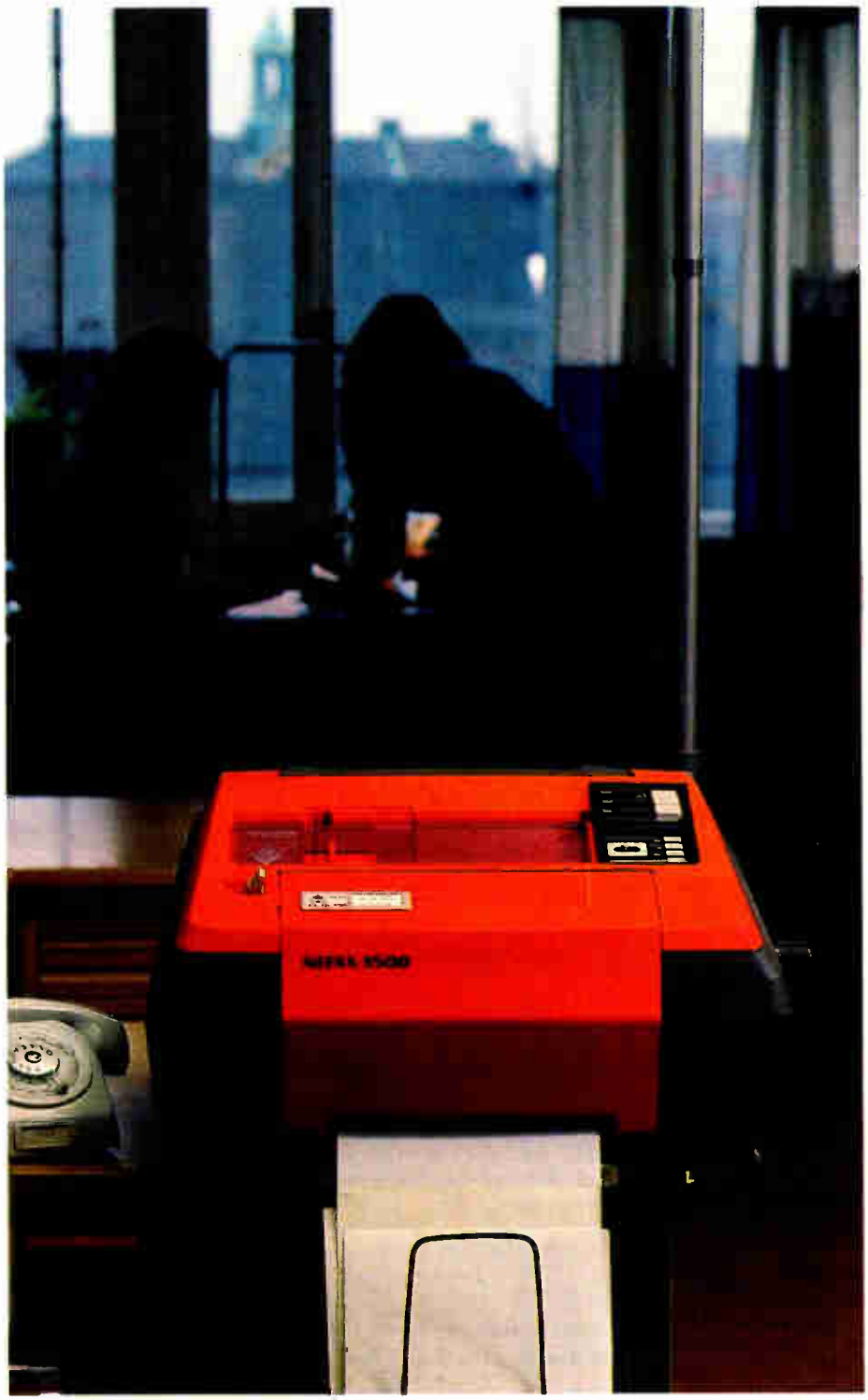
The NEFAX-3700 is an addition to the NEFAX-3000 Series of medium-speed facsimile machines that meet CCITT G2 standards. It has a Super Express Mode that shortens transmission time by skipping over blank (white) portions of a document. Another new feature, Hi-Grey Scale Recording, reproduces half-tone nuances such as those found in photographs. And like the NEFAX-6500, the NEFAX-3700 can automatically send up to 30 pages in sequence.

Designed to fit on any office desk, the NEFAX-2000 is an economical medium-speed (G2) machine. It consumes little power—about 70VA—and is practically maintenance-free.

With these three new additions, the NEFAX line-up is now comprised of seven facsimile machines.



LSI TRANSMULTIPLEXER INTRODUCED

NEC's new DTM-2400 transmultiplexer converts two 12-channel FDM group signals in the 60-108kHz band to a 24-channel digital carrier signal at 1.544Mb/s or vice versa.

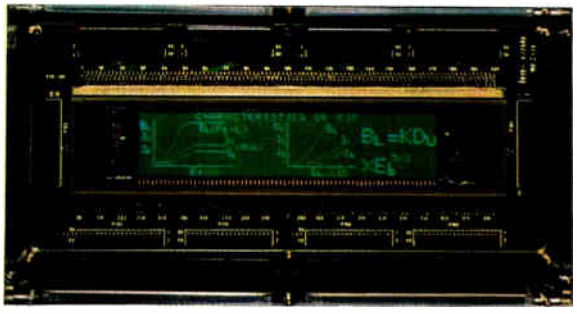
Designed to satisfy all CCITT Recommendation G. 792 specifications by a large margin, the DTM-2400 incorporates state-of-the-art LSI and digital signal processing technology that reduces equipment size, cost, and power consumption. It is housed in a compact W19" × H7" × D14" subrack mountable in an EIA standard 19" rack.

The DTM-2400 has various options for signalling conversion, clock synchronization and signal interface conditions. For example, two replaceable modules are available for signalling conversion: a 3,825 (or 3,850) Hz out-of-band signalling module and a 2,600Hz SF signalling module.

A transmultiplexer with a larger capacity will become available later this year. This, the DTM-1200, will be able to perform a bilateral conversion between two 60-channel supergroup signals (2 × FDM BSG) in the 312-552 kHz band and five 24-channel PCM (5 × 1.544Mb/s) signals or four 30-channel PCM (4 × 2.048Mb/s) signals.

FIP DISPLAYS FINE-PATTERN GRAPHICS

Because they are flat and provide easy-to-see displays without flickering or misregistration, graphic fluorescent indicator panels (FIP) are expected to replace cathode ray tubes in small display terminals.



The new FIP240A4XT from NEC is a large capacity 60 × 280 dot fluorescent indicator panel capable of displaying 240 characters (40ch. × 6 lines). In addition, it can display fine-pattern graphics such as illustrations, tables and drawings with even brightness, and free from deformation.

These capabilities are due to the FIP240A4XT's 16,800 dot cells that are arranged at uniform 0.65mm pitch intervals in an effective display area 38.80mm (vertical) × 181.80mm (horizontal). Each dot measures 0.45 × 0.45mm.

This large capacity graphic FIP is appropriate for a wide variety of hardware, including word processors, electronic typewriters, POS terminals and banking systems.

MEXICO TO EXPAND MICROWAVE COMMUNICATIONS SYSTEM

Mexico will have a fully solid-state 2700-channel microwave communications system installed by early 1982 along an existing link that extends about 2,200 kilometers from Guadalajara to Tijuana.

The new 45-station 2,200 kilometer microwave system was ordered from NEC by the Secretaría de Comunicaciones y Transportes, Dirección General de Telecomunicaciones (SCT), United States of Mexico. It will be equipped with NEC's latest 500 Series, including the TR-5G2700-500 microwave communications equipment.

The TR-5G2700-500 has a microwave signal output power of 7 watts, uses no travelling wave tubes, and can handle 2,700 telephone channels on one RF carrier. The new Mexican system will be designed so that its channel capacity can be expanded up to 13,500 in the future.

Notably absent from the project is the construction of new station buildings. This is because the slim 500 Series equipment requires minimum floor space and can be installed in existing stations.

The major equipment will be manufactured locally by NEC de Mexico, S.A., de C.V., headquartered at Edo. de Morelos, near Mexico City.

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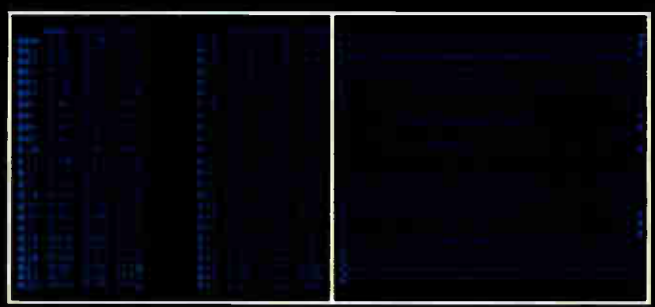
For powerful software debugging, K101-D data domain capabilities include disassembly, 50 MHz clocking, 48-channel recording, 12 external clocks, 515-word memory, demultiplexing, 16-level trace control for triggering, 6 display code formats, and reference memory.



For powerful hardware debugging, K101-D time domain capabilities include 100 MHz clocking, 48-channel recording, 515-word memory, 5-ns glitch capture, 16-level triggering, channel labeling, new high-performance probe design, as well as horizontal and vertical display expansion for easy reading.

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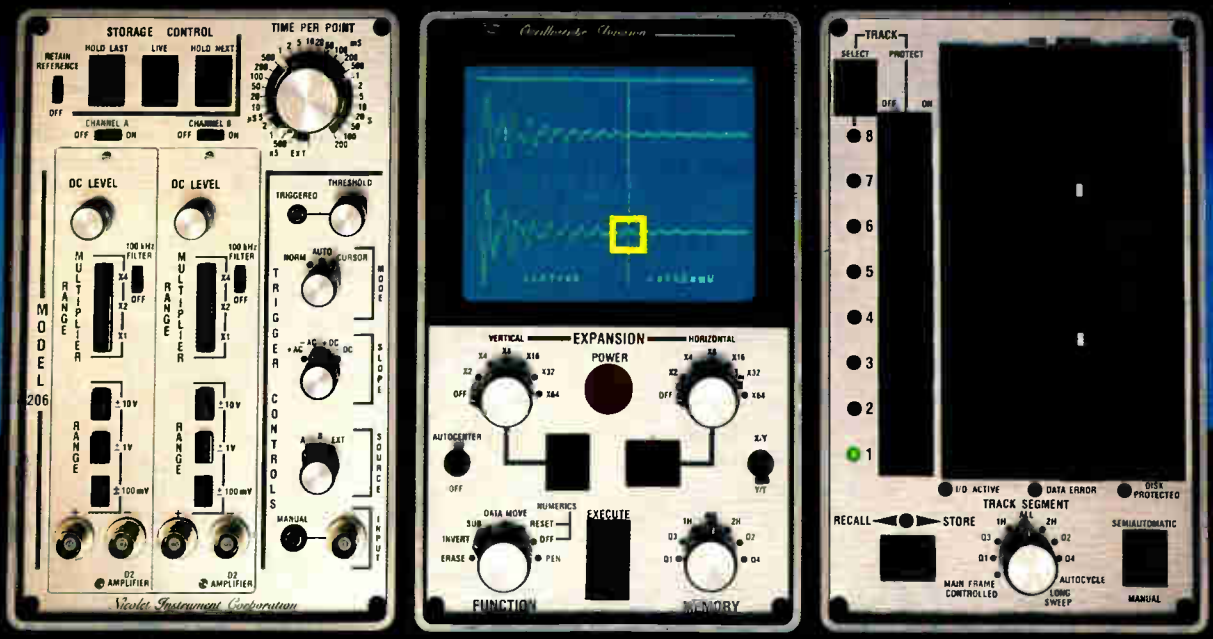

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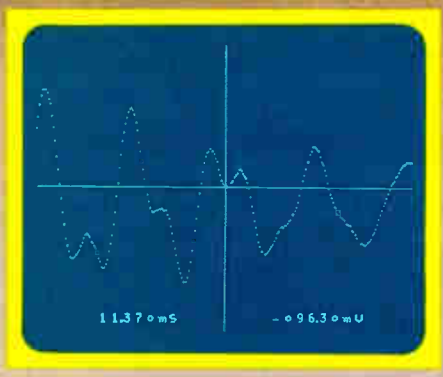

Expansion of selected area in above photo, for detailed analysis.

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Electronics newsletter

IBM poised to plug in 8087 number cruncher

Look for IBM Corp. to supercharge the number-crunching ability of its new personal computer (see p. 50) in early 1982. That's when it will be able to plug in Intel's 8087 arithmetic coprocessor, **which can be accommodated on the 8088 processor board.** The early 1982 date is when languages like PL/1-86, which can use the 8087, will become available. IBM will not discuss the matter.

1,000-V part among Motorola MOS FETs . . .

Backing up its strong commitment to power MOS field-effect transistors, Motorola Inc. expects to introduce about 180 new parts in the next six months. Scheduled from the Phoenix operation are 500-V p-channel FETs and soon to be announced 1,000-V devices—the highest voltage rating yet for a power MOS transistor. **Rated at up to 1 A with an on-resistance of 10 Ω, the kilovolt devices will sell for about $12.** Although attractive for European markets because of the higher voltages there, the general appeal of such devices is uncertain—Motorola is testing the waters.

. . . with high-voltage bipolars also listed

The expanded MOS effort does not mean bipolar devices are taking a back seat in the Power Products division at Motorola. Continued work on second- and third-generation Switchmode parts **will result in high-voltage bipolars, also.** Meanwhile, the Bipolar Integrated Circuit division is eagerly awaiting clearance to release semi-custom linear master-slice chips through Motorola's computer-aided design centers.

New instrument combines data capture, analysis, display

A marriage of computer, data-acquisition system, and digital oscilloscope, the under-$10,000 Data 600 from Data Precision Corp. in Danvers, Mass., is expected to bow within a month. Among its capabilities are acceptance of multichannel inputs at frequencies as high as 100 MHz and, using a 16-bit microprocessor, **performance of a variety of signal-processing and display tasks.** Many forms of sophisticated analysis are to be available with a single keystroke; among them is fast Fourier analysis.

North Star adds multiuser, graphics capabilities to line

Keeping pace with the rapidly building market, personal computers' capabilities continue to mushroom. The latest step upward is from North Star Computers Inc.: a multiuser personal system and a desktop unit with full graphics capability. The San Leandro, Calif., firm is expanding its Horizon line to make it accessible to up to five users by **incorporating a 5¼-in., 5-megabyte Winchester drive for the TSS/5 model,** or a 14-in., 18-megabyte drive in the TSS/18 with an optional 13.4-megabyte tape backup. Cost will average $2,508 per user, says North Star. The new machine with the graphics capability, called Advantage, will sell for $3,999. That will buy a 12-in. display, two 5¼-in. high-density floppy disk drives, and graphics software packages.

Redfield's new firm readies small computer

After a 16-month gestation period, the firm purchased in May 1980 by Peter Redfield, the man who founded and headed the ill-fated Itel Corp., is about to introduce **the first of a series of new products developed under his leadership.** The 13-year-old Digital Scientific Inc. of San Diego will unveil the Meta 4 2000, a Z80B-based small-business computer system

using the CP/M operating system with a disk capacity of up to 40 megabytes and a streaming tape drive backup for Winchester versions.

PDP-11, LSI-11 memories due from Cambex

Two high-density, single-board memories for Digital Equipment Corp.'s PDP-11 and LSI-11 systems will accelerate Cambex Corp.'s drive into DEC-compatible markets this fall. **The Waltham, Mass., firm says its 512-K byte LSI-11 memory, priced at about $2,400, is the densest yet** and takes advantage of the LSI-11's new 22-bit addressing capability. A second add-in, a 1-megabyte board for PDP-11 computers, will cost around $6,300. Also in final development is a semiconductor replacement for DEC's RK05 disk memory; with 256-K bytes to 5 megabytes of capacity, the system will cost about $11,000 per megabyte as a mainframe add-in.

Microcomputer boards to get silicone coat

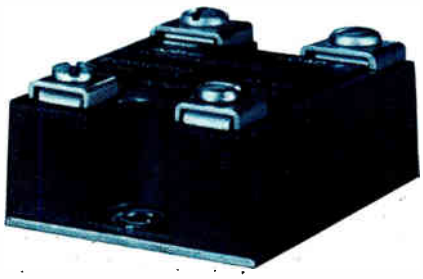
With the oil-exploration industry showing great interest in the finished product, Texas Instruments Inc. of Dallas plans to offer a new line of industrial-grade MOS microcomputer boards that will be conformally coated with a transparent silicone resin. A product of Owens-Corning Fiberglas Corp. of Toledo, Ohio, **the resin is designed to protect the board and its components against corrosion from acid, salt, moisture, dust, and abrasions.** Initially, TI will offer five members of the new TM990/C series of 16-bit-microprocessor–based boards. Each will be a complementary-MOS version of the standard TM990 microcomputer boards at present on the market. The coating, the C-MOS static memory devices, and special handling will add 25% to 30% to the price of the boards.

Ada gets first commercial compiler

The rapidly maturing Ada programming language is about to take a giant step toward practical applications with the commercial release of the first Ada compiler. From Telesoft of San Diego, the compiler will sell for $2,400 and is part of the company's Program Support Environment, **which includes Pascal and the ROS multitasking operating system.** Telesoft, which last spring merged with hardware maker Renaissance Systems Inc. [*Electronics*, May 5, p. 44], also is now offering its T68-KQ central-processing-unit board, which operates on the Digital Equipment Corp. Q-bus, and a work station that uses the board and includes an intelligent terminal with floppy-disk or Winchester storage and 256-K bytes of random-access memory.

Addenda

Arco Solar Inc. has terminated the $25 million contract under which it supported Energy Conversion Devices Inc.'s research on amorphous silicon photovoltaic cells. The Chatsworth, Calif., subsidiary of oil giant Atlantic Richfield Co. has told its former partner that **it has better options for research into thin-film amorphous materials,** ECD's specialty, but refuses to discuss the decision further. Industry speculation holds that a major reason is a multimillion-dollar investment Standard Oil of Ohio is reportedly making in the Troy, Mich.–based ECD. . . .LSI Logic Corp., the Santa Clara, Calif., firm that is working with Toshiba Corp. on an advanced complementary-MOS logic array family (see p. 64), **is also bent on becoming a full second source of Motorola emitter-coupled-logic Macrocells.** The 600- and 1,200-gate devices provide delays of 900 ps.



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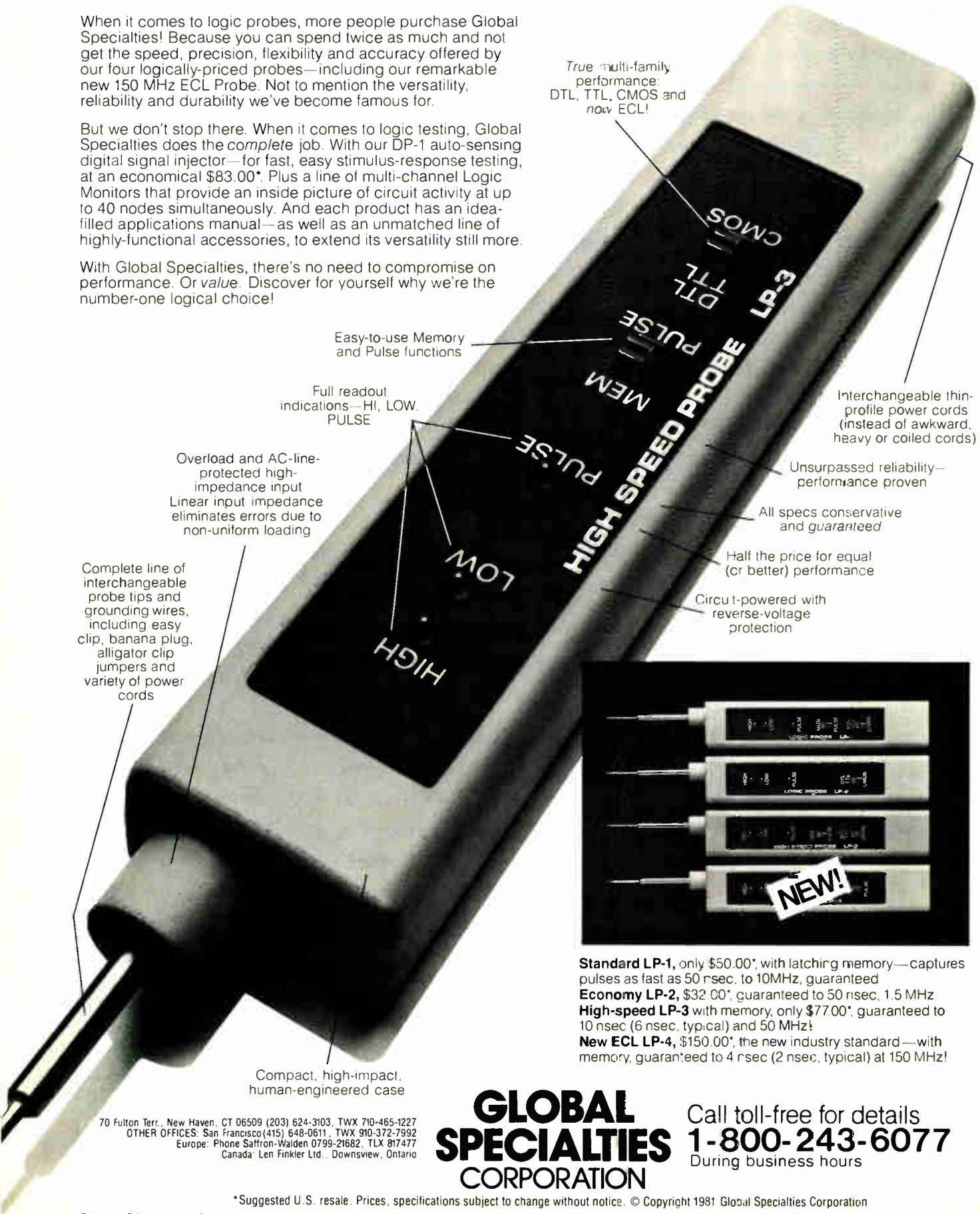

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High-frequency thin-film transistor operates at 200°C

by Roderic Beresford, Components Editor

Lithographic techniques adapted from IC fabrication form cadmium selenide devices on glass substrate

Microelectronics Engineering Corp., a small custom hybrid-circuit house in the Deep South, has quietly developed an advanced process for the fabrication of thin-film transistors that any large semiconductor house would envy: the process yields cadmium-selenide small-signal transistors that can withstand temperatures up to 200°C.

The two-year project that led to the new transistor-making technique is part of an Army manufacturing-technology improvement program. "We are using advanced computer-aided processing to manufacture thin films," notes Samuel Hartin, vice president of business operations for the Auburn, Ala., firm. "Photolithography and automated control of deposition parameters give us reproducible, high-yield devices." Thin-film transistors (TFTs) in the past have given relatively poor electrical performance, in part because small, tightly controlled geometries are impossible with the relatively crude masked-evaporation methods ordinarily used to fabricate them.

Heat beater. Familiar integrated-circuit industry techniques for patterning and deposition benefit TFTs tremendously. "They've abandoned the old masked-evaporation process," comments Robert Brown, general engineer at the Redstone Arsenal in Huntsville, "and are adopting standard lithography to produce perfectly viable devices for demanding applications where silicon just won't work." The key to the high-temperature performance is the semiconductor CdSe, whose thermal properties lead to transistors with temperature coefficients about an order of magnitude lower than typical silicon devices, adds Brown.

The TFTs are built up on a glass substrate, which is not only inexpensive, but also can be virtually any size desired. A thin layer of aluminum oxide is first deposited over the entire substrate as a high-purity isolation layer.

As shown in the figure, the source and drain regions—made of a material MEC will not name—are topped by polycrystalline gate insulation and metal contacts. They are formed by deposition and patterning steps using standard 2.5-to-4-micrometer photolithography.

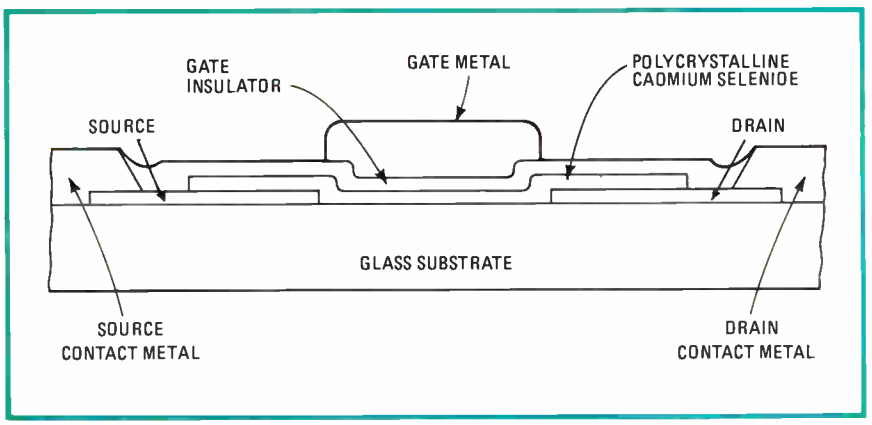
The accurate pattern control possible with photolithography keeps the gate-source and gate-drain overlap down to about 10% of the gate area, reducing the parasitic capacitance that limits frequency response. These field-effect transistors can operate at frequencies of a few tens of megahertz and could reach several hundreds. Transconductance at present is high—about 0.1 mho.

Although the small-signal transistors are not intended for power handling, their heat dissipation can be boosted by using substrates with higher thermal conductivity, such as anodized aluminum or beryllia.

As for low temperatures, the devices have been tested down to −65°C and are expected to stand up to significantly lower temperatures.

Although MEC has emphasized the transistor's high-temperature capabilities, its thin-film technology is "essentially the same as that developed at Westinghouse Electric Corp. in the mid 1970s," maintains Peter Brody, who left Westinghouse to work at his own firm, PanelVision, also located in Pittsburgh, Pa. [*Electronics*, March 13, 1980, p. 127].

The possibility of fabricating decoders and drivers out of thin-film transistors at low cost makes this



Advance. Cross section of thin-film transistor shows depletion-mode cadmium selenide channel formed by the photolithography of deposited polycrystalline material.

technology most promising for the eventual production of flat-panel electro-optical displays. Brody says the extensive work at Westinghouse is the source of most of the know-how behind current work in TFTs. "It's high time some others got into the act," he says.

MEC, which will use the TFTs in high-temperature military and commercial circuits, also works with thick-film hybrids. It has developed a fine-line fabrication process that produces 2-mil-wide interconnects. These dense thick-film circuits will be used in new versions of the controls found on passengers' seats in the 747, DC10, and L1011 jets.

Tailoring the 3600 to Lisp

The Lisp language was designed at the Massachusetts Institute of Technology in Cambridge primarily for investigations into how human intelligence could be modeled on computers. As it developed, the computer model grew to require a lot of main memory. Moreover, it executes relatively slowly on general-purpose computers, which is why Symbolics Inc. developed the 3600 computer hardware designed for the idiosyncracies of Lisp.

The language is highly symbolic and allows complex data structures—called objects—to be defined and manipulated by single instructions. An object could, for example, be a payroll record for John Doe. It would consist of different pieces of information, including Doe's address, social-security number, pay rate, and tax status.

Once the programmer defines the object, "John Doe," its individual parts (pay rate, for one), can be accessed by a relatively simple command like "Change John Doe's pay rate to $20,000." Lisp will then automatically retrieve the information from the object and update and store it. A programmer need not write any of the routines for manipulating data that an ordinary language requires, which greatly speeds program development.

To accomplish the same functions in another language would require just about as much memory as Lisp requires. However, because it is so easy for the programmer to manage and manipulate data objects, the tendency is to create ever more complex one, and the memory needed balloons.

But not only are programs larger with Lisp; the run-time environment is larger too, boosting memory requirements still more. For instance, an interpreter and compiler are stored in memory, along with an on-line editor and other utilities.

So much more must be done at run time that a well-written Fortran program, for example, will always run faster on a general-purpose computer than will an equivalent Lisp program. Symbolics' 3600, has been built with special hardware and microcoded architecture to speed up the chores specific to the language. For example, Lisp needs extensive run-time error checking and the 3600 performs the checks in parallel with instruction decoding. It needs this checking to insure that modules that may have been separately compiled do indeed refer to the same type of objects.

The 3600 also has special data paths to identify the data type being implied by a generic instruction. For example, Lisp allows a single instruction, like add, to be used with many data types; separate instructions like floating-point add and integer add used with other languages are not needed. This single generic instruction is possible because the microcode that decodes instructions first determines the data types being used.

Another important design facet of the 3600 is its ability to track with small cache memories the temporary storage locations used for Lisp. The language makes extensive use of dynamic storage allocation—data objects are created and deleted from memory during program execution. Keeping track of these locations can add significantly to the run time of an ordinary computer. In fact, many of the Lisp implementations on general-purpose computers must periodically stop the program from running in order to do such "garbage collection"—the identification and reclaiming of storage no longer being used. The 3600 handles this chore while hardly slowing the processing at all.

-R. Colin Johnson

Computers

Lisp language gets special machine

A powerful new minicomputer whose architecture exploits the high-level Lisp programming language is about ready to go. The Symbolics 3600 targets the booming software development business and its computer-aided design and artificial-intelligence segments that eat up memory capacity and demand high speed. The computer, to be built by Symbolics, Inc., Woodland Hills, Calif., has 1.125 billion bytes of address space (256 million 36-bit words) and processes more than 1 million instructions per second.

Although performance at least beats more expensive minicomputers, this is not its prime feature, says marketing director Henry Baker Jr., "Total integration of the hardware with a large proven Lisp software base" takes the spotlight, he says.

Closely behind is price, about $60,000 in quantity for a work station ($75,000 for one), far cheaper than roughly equivalent minicomputers programmed for Lisp and Symbolics' own lower level LM-2 introduced for $100,000 [*Electronics*, Aug. 11, p. 159].

Another view of the 3600's speed/price edge, according to Baker, is that it should operate twice as fast as a Digital Equipment Corp. VAX/780 computer selling for about $200,000 and nearly as fast as a DEC 20/60, at around $400,000, when both are running Lisp. These and other 3600 performance specifications are derived from simulations done on a Symbolics LM-2.

Although the 3600 shares with the LM-2 many basic operating traits common to Lisp, there are many differences. With any other computer, Lisp is just another program, but with the 3600, [Lisp's] features dominate the entire operating system and hardware architecture, Baker says. He sees the LM-2 as a transitional machine for Lisp experimen-

tation, with the 3600 taking over as a better and cheaper standard workstation.

One improvement that helps to boost speed to more than three times the LM-2 is data paths that permit parallel execution of the operations unique to Lisp. Other structural changes that push performance higher, according to Baker, include "an overlapped instruction fetch and an asymmetrical but dynamically more optimal instruction set."

Other upgraded features of the new Symbolics computer include packages that execute both Fortran-77 and Pascal, in addition to the primary Zetalisp in which all system programs are written. Also, a 68000-based front-end processor takes much of the load off the central processing unit during most operations by controlling low and medium-speed input/output devices and implementing error logging and recovery. It also debugs the 3600 when not running.

To simplify design and cut manufacturing costs, Symbolics chopped the board total to 6 from 14 in the LM-2. Chiefly, it did this by using more large-scale integration along with microcode to squeeze what were formerly separate I/O controller boards (including those for disk, display, and local-network interfacing) onto the processor. Also, mass memory uses 64-K random-access memories, instead of the LM-2's 16-K RAMs.

The 3600's basic hardware consists of a free-standing cabinet containing the microcoded CPU, 1,125 megabytes of main memory, a fast-access 67-megabyte Winchester disk, and Ethernet II interface and two serial lines. A graphics console holds a keyboard, a landscape-format 1000-line black-and-white bit-mapped display, a "mouse" (pointing device), and includes audio output. An option is a color monitor. Extensive graphics software is built into Zetalisp itself, allowing multiple overlapping windows of information to be easily displayed.

Symbolics will unveil the 3600 this month at the Seventh International Joint Conference on Artificial Intelligence in Vancouver, B. C., Canada. Production will start soon for initial deliveries next March with rates to peak at 15 a month by the end of 1982. LM-2 manufacture will likely be all phased out by then, says Baker. **-Larry Waller**

Microwaves

Surface-acoustic-wave signal processor reflects simplified correlator design

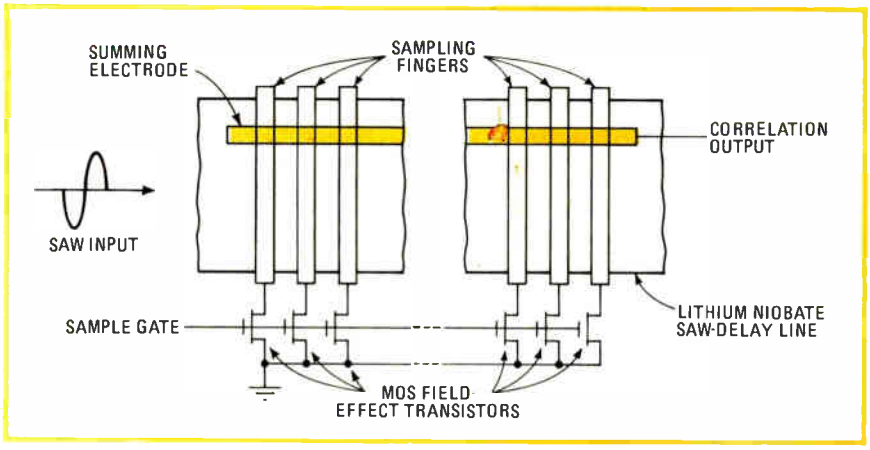
Military communications and radar systems are increasingly using pseudorandom-noise modulation or spread-spectrum multifrequency transmissions to make their signals harder to jam and detect. Receiving these more complex signals is not simple either.

The answer to date has been an ever more sophisticated series of analog correlators, convolvers, and filters, often built around surface-acoustic-wave (SAW) devices, that capture the signals in the midst of apparent noise [*Electronics*, July 31, 1980, p. 41]. Some of these devices have been fairly complex and costly to build, and some require large amounts of high-speed emitter-coupled logic to act as temporary memory for them.

Now, assistant group leader Richard W. Ralston, and staff member Daniel L. Smythe of the Massachusetts Institute of Technology's Lincoln Laboratory in Lexington, Mass., have developed what may be the simplest SAW correlator yet. Theoretically, it could be built monolithically and would not require costly outboard memory.

The unit consists of a lithium niobate piezoelectric SAW device resting on spacers about 350 nanometers above a silicon semiconductor sheet. On the silicon are 300 metal strips, or fingers, laid down at right angles to the direction of wave travel in the $LiNbO_3$. Each finger is connected at one end to an MOS field-effect transistor and, through the transistor, to ground.

Reference first. During operation, all 300 transistor gates are momentarily biased on, grounding each finger for 4 to 5 microseconds as a reference wave propagates down the SAW device. The wave's electrical fields interact with free carriers in the silicon to leave a positive or negative charge on each finger. The charge pattern varies with the envelope of the reference wave, and its characteristic pattern is captured when the FETs are turned off at the end of their 4-to-5-μs second sampling period. Turn-off takes about one nanosecond, more than fast



Finger wave. Lincoln Lab correlator relies on SAW propagating along lithium niobate to create a charge pattern in metal fingers resting on a silicon sheet containing MOS FETs.

enough for the intended purpose.

Once the correlator has been programmed with the charge pattern, any unknown signal—typically riding a radar or communication system's intermediate frequency—can be injected into the same $LiNbO_3$ SAW device. The unknown, sampled exactly like the reference, also charges the fingers, and if there is a strong correlation between the unknown and reference signals, these charges add together, producing a characteristic waveform at a summing electrode.

Compared with earlier, more complex devices, the new correlator has about 5 decibels less output, but it retains its memory of the reference and of the correlation for about the same time as more complex SAW devices do; it takes about 1 second for its output level to drop by 3 dB.

Earlier units with similar functions used arrays of diodes or charge-coupled devices as memory or to program the correlator. Thus, they needed separate inputs for reference and unknown signals. But the new unit does not, and its simple structure should be much easier to reduce to monolithic form.

The lab team suggests gallium arsenide as a good monolithic substrate material. Though it is more weakly piezoelectric than $LiNbO_3$, it is a semiconductor, and the team points out that a thin layer of zinc oxide could be laid down to improve piezoelectricity.

They also note that work in this direction is already under way at Motorola, Texas Instruments, and at United Technologies, and that both ZnO on silicon and on GaAs have been studied at these firms with the goal of producing devices similar to those unveiled by the Lincoln Lab.

A move to GaAs would make the present two-tiered structure unnecessary and possibly improve coupling between SAW waves and the finger structure. However, higher leakage currents with GaAs could cut memory time down from today's 1 second or so, to as little as 10 to 100 μs. That is ample when only about 15 μs is needed to completely reprogram the device. **-James B. Brinton**

Business

NEC buy-in charged on Comsat stations

Japan is again charged with dumping electronic products in the U. S.—this time in the burgeoning market for satellite earth stations. That is the claim of Aydin Corp., the Fort Washington, Pa., assembler of high-powered amplifiers using traveling-wave or klystron tubes for civilian and military earth stations.

The company is calling for a Federal investigation of two Communications Satellite Corp. January amplifier awards to Nippon Electric Co. The Aydin petition to the Federal government is being supported by the Communications division of the Electronic Industries Association.

NEC and its subsidiary, NEC of America, vigorously deny charges that they bought into contracts to crack the U. S. market, calling Aydin "a disgruntled bidder" whose petition "is flawed, inadequate and absurd," in its rebuttal.

The petition to the International Trade Commission and the Commerce Department's International Trade Administration to investigate the dumping is the first in the history of the U. S. telecommunications industry and should be the first test of the Reagan administration's high-technology trade policy. "These are important issues that need to be resolved quickly," says EIA vice president John Sodolski.

Issues. The two Comsat contracts that are cited by Aydin call for the design fabrication, and test of 29 high-powered amplifiers—nine using 3-kilowatt klystrons and 20 using TWTs. Both uplink transmission products, for civil and military satellites, operate in the C, X, and Ku bands.

NEC won both contracts with a unit-price bid of $23,596 for the klystron parts, which Aydin asserts in its petition is 36.7% below fair value, and a unit-price bid of $66,436 for the TWT amps without the tube or related linearizing components. Of the latter award, Aydin says the three competing U. S. firms—itself, Varian Associates of Santa Clara, Calif., and MCL Corp., La Grange, Ill.—bid between $105,000 and $125,000 per unit on the contract.

Comsat, however, says that both NEC proposals were technically superior and that the next lowest U. S. bid on the klystron amplifiers was only 2.9% higher—despite Aydin's claim. On the traveling-wave tube equipment, Comsat says, the U. S. bids were 39.5% and 40.5% higher than that of NEC.

The Japanese company raises the possibility of impropriety between Aydin and Varian on their bids for the 23 parts. Not only were the Aydin and Varian bids "within approximately 1% of each other," says the NEC filing, but both companies "claimed to have had the same or similar secret discussion concerning [the Nippon Electric bid] with Comsat's employees."

Injury. In its allegation of irreparable injury to domestic industry—a key point to be proven in any antidumping action—Aydin estimates that 40 to 50 TWT high-powered amplifiers are produced in the U. S. each year, with all but 10 going to the military market. Thus, says the company, the Comsat award forecloses the domestic commercial market to U. S. producers for two years, not counting the follow-on market for spare and replacement parts. Of the 100 to 120 klystron high-powered amplifiers built annually, all are for commercial use, according to the company.

The dumping damage, Aydin says, will force some of the companies still in the market to leave it—either itself, MCL, Varian, or Comtech Telecommunications Corp. of Smithtown, N. Y.

However, the NEC rebuttal in the dispute contends that Aydin is misleading the Commerce Department and the ITC by failing to note that Aydin "is merely an assembler" of high-powered amplifiers and does not manufacture any of the elements—the tubes, intermediate am-

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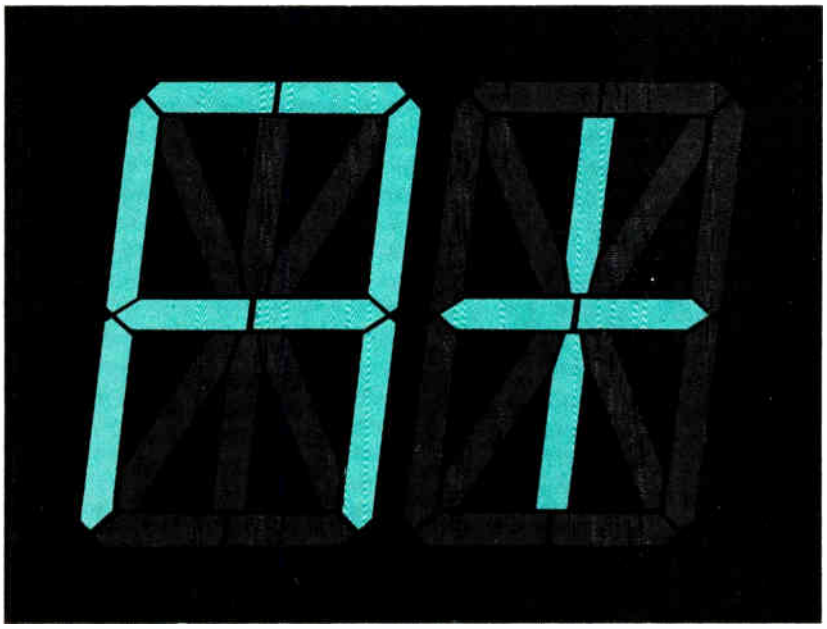

Sprague Electric continues to be No. 1 for cost-effective volume production of BiMOS vacuum fluorescent display drivers.

As the need for larger and brighter vacuum fluorescent displays has been increasing, Sprague Electric has been continually expanding its skills in the manufacture of complex array BiMOS drivers.

For nearly 10 years, Sprague has employed state-of-the-art processes to produce millions of display drivers. We have combined these processes with MOS logic and bipolar buffers in a single unit, permitting a lowest-cost approach to integrated display circuitry. As a result, both the reliability and economy of Sprague drivers have been repeatedly proven in point-of-sale terminals, computer peripherals, avionics, instrumentation, electronic games, and similar applications.

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plifiers, or linearizers—"while NEC manufactures all three, as well as integrated circuits and other devices required. For an assembler to compare its cost structure with that of an integrated manufacturer and not explain the difference between the two is by itself misleading, says the Japanese company.

The ITC is expected to recommend by the end of September whether or not to hold a full-scale inquiry in the case. **-Ray Connolly**

Packaging

Chip makers select leadless carriers

As 16-bit microprocessors quickly move into the age of ceramic leadless chip-carriers, three major U. S. manufacturers are lining up behind three different types of industry-standard packages.

Motorola Inc., which plans to unveil its strategy next month at Wescon/81, will soon be selling its MC68000 family in type C chip-carriers. This cavity-up package is suitable for sockets, clip-on leads, and direct soldering to substrates.

Also at Wescon, Zilog Inc. of Cupertino, Calif., will be showing its type B carriers. Like the C version, it has a cavity-up format but a different notch [sense] on the back for pin 1 identity.

Intel Corp. of Santa Clara, Calif., will be using type A carriers—a three-layer cavity-down package with pads only on its top. This kind is limited to socket and clip-on–lead applications.

Package. Type C leadless ceramic chip-carrier (above), suitable for socketing or direct soldering, will be used by Motorola for its 16-bit MC68000 family of devices.

Intel based its choice on predictions that direct-soldering applications will not represent much of the chip-carrier business. "The applications for most of the new microprocessor products [packaged] in chip-carriers will be field replacement in sockets," says Fred Burris, manager of advance packaging development.

"That way it's a lot easier to go out and replace a chip-carrier on a board," he adds. Though type A's cavity-down configuration eliminates direct soldering applications, it also dissipates heat better.

The carrier's socket, jointly developed by Intel and Textool Products Inc. of Irving, Texas, has an aluminum cover that acts as a heatsink on the back side of the package. (Power dissipates through the back side of the die.)

Intel has already introduced its first 16-bit device in the type A carrier, the iAPX 8206 error-detection and -correction unit. Other devices will follow in October, including the iAPX 286 next-generation error-correction chip.

Meanwhile, Motorola's microprocessor operation in Austin, Texas, is betting on the more versatile type C package. Like Intel, Motorola believes more than 85% of microprocessor chip-carrier products will be initially used in sockets.

But as the market matures, the company predicts, the percentage of carriers soldered directly to substrates will grow. Motorola selected the type C package to address these future applications at no additional tooling and production cost.

The firm, which is developing direct-soldering techniques, has begun providing a few samples of a multilayer version in ceramic with a metal lid. With its sights set on production quantities in the fourth quarter, it plans to be the first to offer a 16-bit family in carriers.

The multilayer carrier will cost the same as a ceramic dual in-line package. For example, the MC68000 8-megahertz version will cost $124 each in quantities of 100.

Within nine months, Motorola also plans to begin supplying samples of the 68000 in two versions of a lower-cost single-layer type C chip-carrier. One will have a plastic lid bonded by epoxy. This version will essentially have the same mechanical characteristics as a plastic DIP.

The other will have a ceramic lid hermetically sealed to the carrier by a glass weld. These single-layer carriers will be available for delivery in the final quarter of 1982.

Meanwhile, Zilog is offering a few samples of both 8- and 16-bit microprocessors and peripherals in type B packages. The company plans to phase in the chip-carrier through 1982. **-J. Robert Lineback**

Solid state

Nitride helps shrink rad-hard memory

Processing refinements are shrinking the size of radiation-hardened electronic devices, reports Harris Corp.'s Semiconductor Programs division. As proof, the Melbourne, Fla.–based division is ready to deliver a hardened version of its 4K-by-1-bit HM-6504 static complementary-MOS random-access memory. The memory occupies about the same area as a 1-K radiation-hardened RAM, says James E. Schroeder, principal engineer on the project.

Only about 10% larger than its commercial counterpart, the new HS-6504-RH equals the HM-6504's electrical performance, even when exposed to more than 2×10^5 radiation-absorbed doses, or rads, maintains Schroeder. Despite its scaled-down geometries, he adds, the RAM retains both the total dose hardness and latch-up immunity that has been achieved using earlier hardening processes. Its performance suits it to many applications in deep-space and

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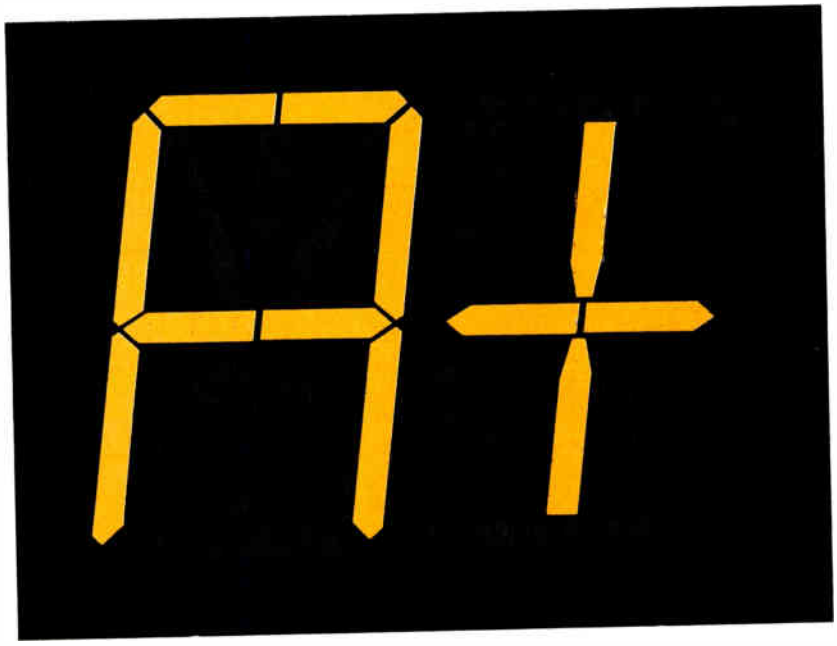

Sprague Electric continues to be No. 1 for cost-effective volume production of bipolar gas-discharge display driver ICs.

As the need for larger and brighter gas discharge displays has been increasing, Sprague Electric has been continually expanding its skills in the manufacture of bipolar high-voltage drivers.

For nearly 10 years, Sprague has employed state-of-the-art processes to produce millions of display drivers with voltage ratings well in excess of **100 V**. We have combined these processes with logic and buffers in a single unit, permitting a lowest-cost approach to integrated high-voltage circuitry. As a result, both the reliability and economy of Sprague drivers have been repeatedly proven in point-of-sale terminals, computer peripherals, avionics, instrumentation, electronic games, etc. Sprague is now developing **200 V** monolithic integrated circuitry for release shortly.

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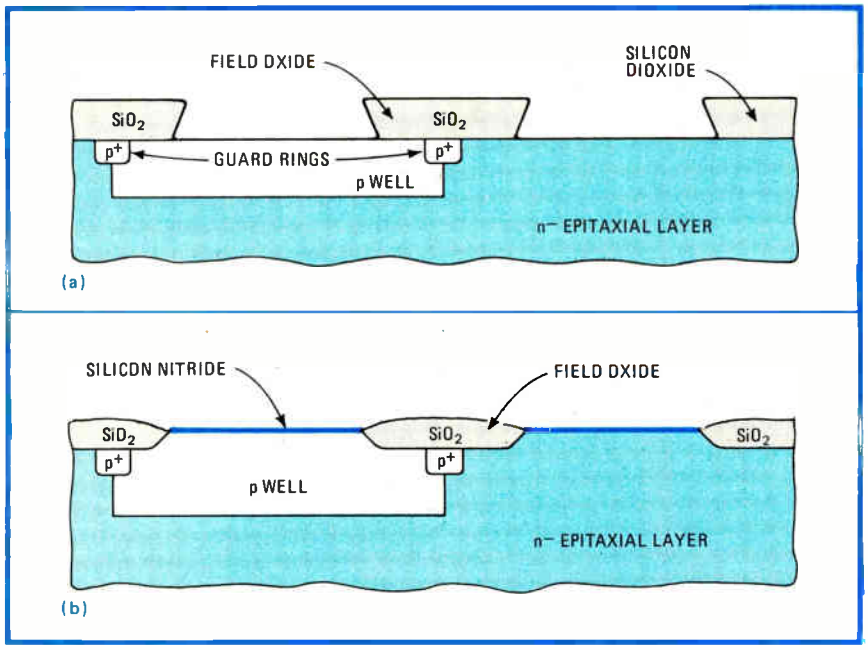

Flatter. The old method of oxidizing an entire wafer and etching (a) does not produce as flat a surface as using silicon nitride (b) to prevent oxidation of active regions.

weapons-radiation environments.

The Harris approach employs a special masking step and some additional processing to reduce chip size, although it preserves many chip characteristics of earlier techniques that were developed at Harris and Sandia National Laboratories in Albuquerque, N. M.

These features include an n^--on-n^+ epitaxial substrate that lends latch-up immunity, ion-implanted shallow source and drain junctions, and p^+ guard rings around n-channel devices that prevent radiation-induced surface inversion.

Both the old and new processes put a hardened silicon-dioxide layer between the epitaxial substrate and subsequent layers of polysilicon and aluminum. The oxide layer must be particularly thick (around 1 micrometer) in the so-called field areas between active device regions in order to minimize the parasitic capacitance between the substrate and overlying wiring levels.

In the old method, the entire wafer is uniformly oxidized to the required thickness, as shown in the figure. The oxide is then etched back in the regions where devices will be fabricated, exposing the silicon surface for gate oxidation.

The new method employs local oxidation instead, in which a thin silicon-nitride layer is deposited to prevent oxidation of the active regions while the thick field oxide is grown. Once the field oxide is completed, the nitride layer is stripped off the active regions. The result is a much flatter wafer surface—0.5-μm steps instead of the 1.2- to 1.4-μm height differences that existed between the gate and field oxide regions of the old technique. After the silicon nitride is removed, a thin silicon dioxide layer is grown.

Since the wafer surface is more planar, subsequent lithographic steps do not suffer from as much optical distortion as in the old method. This allows finer lines to be fabricated. The undercut profile of the etched field oxide in the old wafer-wide oxidation method is eliminated. Control of the active-region geometry is tighter, and these areas can be made smaller and closer together.

Besides the rad-hard HS-6504-RH, Harris has in final development a 1K-by-4-bit static C-MOS RAM, which is the hardened equivalent of the Harris HM-6514. Both the hardened RAMs have 4-μm interconnect spacings, compared with the 7-μm spacings in Harris's earlier 1-K rad-hard RAM. Channel lengths in the new RAMs are 4 μm for p- and 3 μm for n-channel devices; metalization pitch, with contact, is 1 μm.

Operating voltage for the 4-K RAMs is typically 5 V with an accuracy of $\pm 10\%$, compared with the 10-V operating levels of previous rad-hard memories, says Schroeder. Worst-case access time is 200 nanoseconds (150 ns is typical), and maximum cycle time is 450 ns. The RAMs draw a maximum of 7 milliamperes per megahertz when operating, and 100 microamperes in standby mode. Both parts, like their commercial twins, have TTL-compatible address inputs and output.

First deliveries of the rad-hard RAMs will be to sponsors of the Harris effort: Itek Corp.'s Advanced Technology division; the Jet Propulsion Laboratory; and the U. S. Naval Research Laboratory. Harris will begin offering samples this October, with pricing for both of the RAMs in the neighborhood of $300 in 1,000-piece lots [*Electronics*, July 28, p. 34]. **-Linda Lowe**

Displays

3-d graphics dazzles display conference

Three-dimensional computer graphics with powerful new processors for off-loading functions from host computers highlighted the Siggraph/81 conference in Dallas earlier this month. The hit of the equipment exposition, judging from the crowds it drew, was the SpaceGraph terminal, a 3-d display shown for the first time by Genisco Computers Corp., Costa Mesa, Calif.

The SpaceGraph [*Electronics*, July 28, p. 150] produces a true space-filling image—the object being displayed actually fills a volume of about 20 by 25 by 30 centimeters. This differs from the perspective projection of a 3-d image on a flat surface, which is what has been regarded as 3-d until now.

But perspective projection sytems showed life as well. It was apparent that designers of computer graphics

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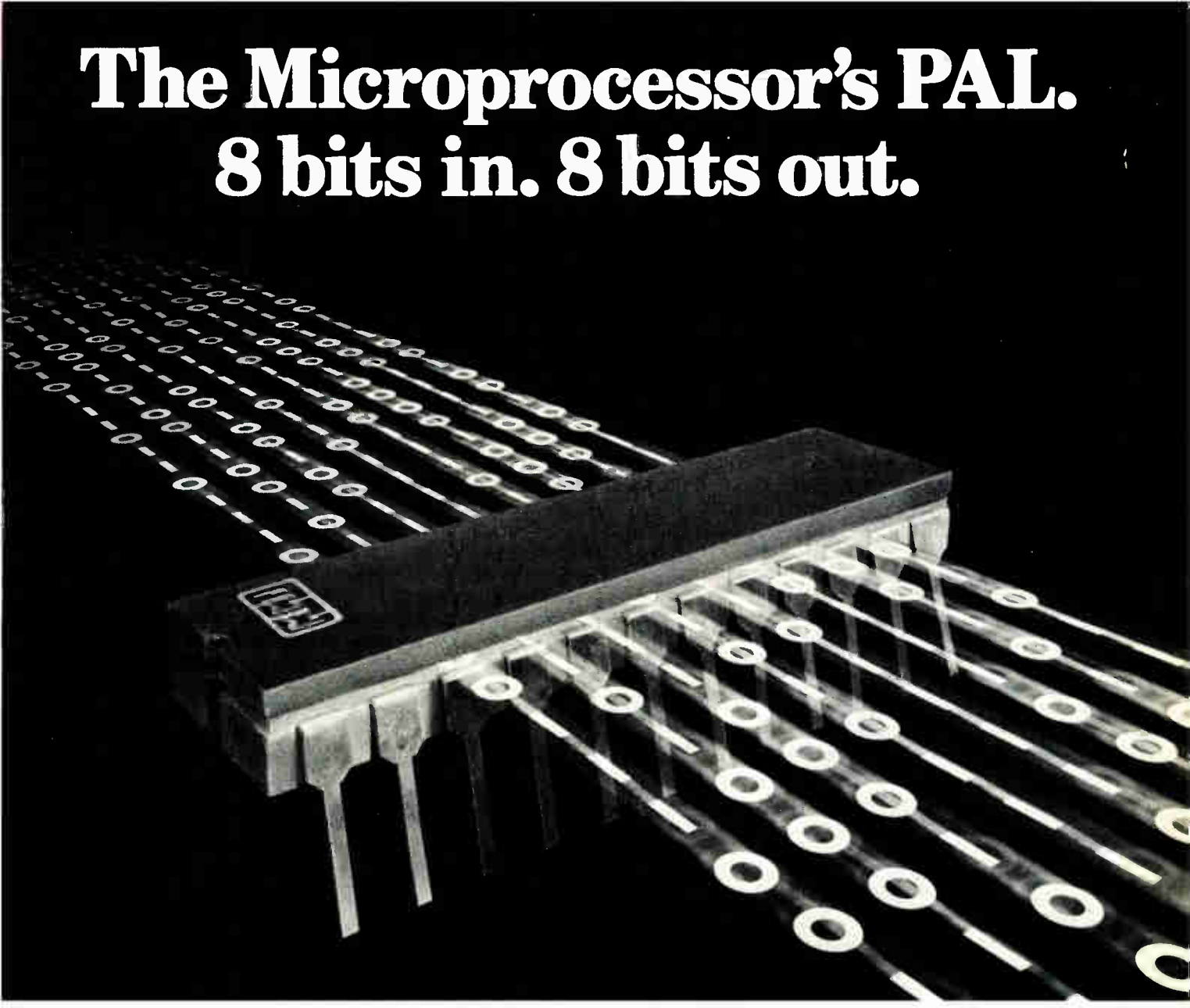

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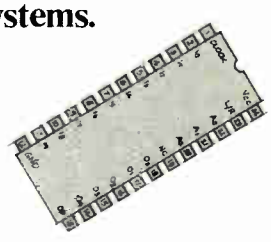

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Computer graphics industry set to climb

Multibillion-dollar markets are just a few years away for the computer graphics industry with its array of terminals for computer-aided design and manufacturing and for the business office. So say industry officials attending the Siggraph/81 Computer Graphics Conference Aug. 3–7 in Dallas. Siggraph stands for the Special Interest Group on Computer Graphics of the Association for Computing Machinery.

Low-cost, higher-density memories, and a shortage of skilled labor are among a number of factors driving development of graphics hardware and software packages for CAD/CAM, points out Ken Anderson, publisher of The Anderson Report, an industry newsletter. "Before, it was driven by economics, and certainly the cost of labor was part of that," explains Anderson, a participant in the five-day conference. "But now the simple unavailability of people [to design] is even a more pressing issue. When the market is out there but you don't have the people to serve it, you very quickly reassess your priorities."

Anderson estimates that the total available computer graphics market could hit $4.5 billion by 1984, with about half of that addressing CAD/CAM. The greatest percentage increase, however, will come from the office segment of the market. "There has been just a dramatic increase in the amount of software and systems dedicated to the creation of slides, viewgraphs, and charts of all kinds to help the manager run his company. It seems we have really underestimated the customer's acceptance of the technology," he notes. "I think it looks like $300 million to $400 million by the end of the year, with probably the [upward] knee in the curve occurring in the first part of 1982." And it was only in the beginning of 1981 that the business graphics systems really began to hit the market, he adds.

By 1984–85, Anderson predicts, business graphics sales will cross the $1 billion mark. "It's not unreasonable to expect a growth rate of 80% to 90%" in the low-cost segment," he notes. Others see rapid growth in other segments as well.

Richard L. Davison, vice president and general manager of the Graphics Systems division of Applied Dynamics International, Ann Arbor, Mich., likes what he sees for computer-assisted instruction, which he believes "will have one of the most dramatic impacts on everyday life." He envisions graphics equipment being used in many places to assist the public, including museums, shopping centers, and malls.

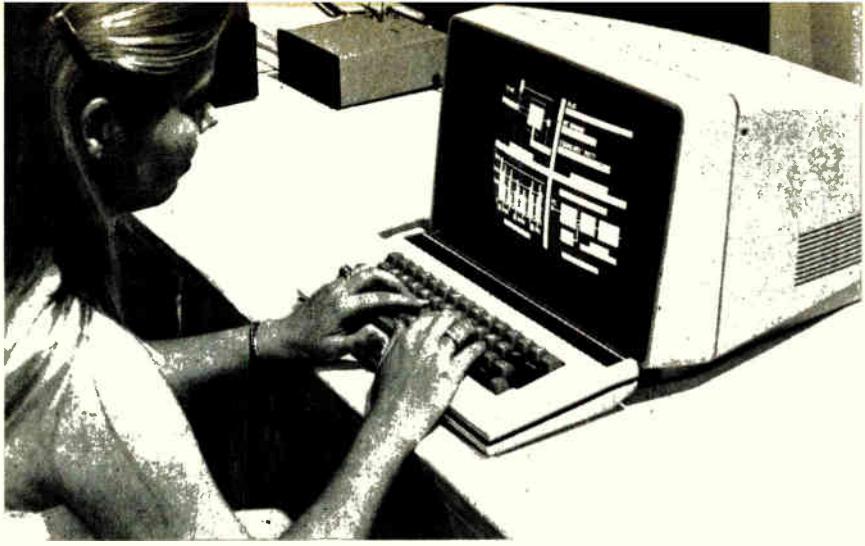
Attendance at Siggraph also seems to reflect growth. This year's show attracted more than twice as many people—11,700—as did the 1980 show. That edition was in Seattle, not nearly as centrally located as Dallas; but then the Dallas show had to contend with the first week of the strike by U. S. air traffic controllers. Exhibit floor space increased 80%, as the number of exhibitors at the conference rose from 95 to 130. **-J. Robert Lineback**

systems have been quick to apply the newest large-scale integrated-circuit technologies in their domain.

High-speed 16-bit microprocessors, 64-K memory chips, and special-purpose graphics chip sets were being employed in the new products to produce very intelligent graphics terminals with reduced costs, more functions, or both. The increased processing power and larger memories in these products also mark a trend toward distributed computer graphics in which the terminals perform more of the purely graphics functions, freeing the host computer to do more of the applications work.

Some of the more striking new product highlights of Siggraph came at the low-priced end of the spectrum. Here the target was the 3279 color display station from IBM Corp., which comes in two medium-resolution versions displaying either four or seven colors and selling for between $4,500 and $5,200. Two recently formed companies have taken on the 3279, with terminals that cost much less.

Integrated Terminals Inc., Addison, Texas, showed an eight-color terminal (model ITI 801) that sells



Capable. Twelve-inch-diagonal screen of Integrated Terminals' eight-color model 801 is set up to demonstrate several of the types of graphics displays it can present.

for $3,000 in single quantities (down to $2,200 each in 100-unit lots). Built around a Z80 microprocessor, the terminal has a 12-inch screen that displays twenty-four 80-character lines in a 640-by-240-dot matrix. A 48-line display will be introduced by the end of this quarter with two more models next year.

The other new terminal is the MVI-7 from Colorgraphic Communications Corp., Atlanta [*Electronics*, July 28, p. 14]. At $3,500 each ($2,800 in quantities of 100), this seven-color display uses a 720-by-280-dot matrix. It also has extra features, including horizontal scrolling and the ability to divide the screen into four areas that can be independently addressed and scrolled.

Both of the terminals emulate others already on the market, so they can be used immediately with existing software. Integrated Terminals' 801 is compatible with software from a leading terminal maker, Intelligent Systems Corp., and will soon be compatible with others as well. Colographics' MVI-7 can emulate and bring color to any of six popular monochrome terminals, including Digital Equipment Corp.'s VT100 offering.

The presence of the 16-bit microprocessor was perhaps nowhere more felt than in several new stroke- and raster-refresh terminals. A trio of new designs have applied the Motorola MC68000, capitalizing on its high processing speed and large amount of memory that can be directly addressed.

Emphasizing the distributed computing possibilities inherent with the 68000 was Vector General Inc., Woodland Hills, Calif. The firm's VG33000-series terminals apply the microprocessor to such chores as servicing display interrupt requests, buffer management, editing, and changing views and perspectives.

The 16-bit 68000 is also at the core of the industry's highest-resolution flicker-free raster-refresh display, the System 3400 XV7 from Lexidata Corp., Billerica, Mass. Its display, with a 60-hertz noninterlaced refresh rate is made up of a 880-by-704-dot matrix.

Yet perhaps the record for handling vectors is held by the PS300 3-d perspective-projection terminal from Evans and Sutherland, Salt Lake City. This $59,000 stroke-refresh unit can update an entire display of up to 95,000 line segments at 30 frames per second. **-Tom Manuel**

Production

Air Force to recruit robots for pc boards

The U. S. Air Force wants the productivity of defense contractors to rise sharply, so it has commissioned Westinghouse Electric Corp. to develop fully automated systems for the design, manufacture, and testing of printed-circuit boards.

Work on the three-year project at Westinghouse's Defense Electronics Systems Center at Baltimore, Md., started this month, and John A. Decaire, manager of manufacturing systems and technology, expects it

Electronics review

will lead to an eightfold increase in productivity in pc-board assembly processes and a tenfold speedup of manufacturing cycle times.

Shared benefits. These dramatic benefits will not accrue to Westinghouse alone. "The Air Force is in this to increase productivity, quality, and cost savings on defense contracts generally, not just at one company," says Lt. Gen. James W. Stansberry, commander of the Electronic Systems Division at Hanscom Air Force Base, Mass.

So, along with $7 million in seed money from the Electronic Systems division to get the project rolling, goes the requirement that Westinghouse must share its findings with over 100 other contractors through periodic seminars and briefings. All progress reports will be in the public domain, and Westinghouse will be obligated to license the know-how it develops, Stansberry points out.

An added industry-wide bonus, Decaire says, will be the establishment of standardized components for automated manufacturing systems as Westinghouse works with other firms engaged in the rapidly developing technology.

Along with the military grant money, Westinghouse plans on investing nearly $200 million of its own to implement the results of its work for plant modernization, Decaire reports. The company will pursue three main themes: a work center for automatic storage, location, and kitting of pc-board components; a work station for fully automated assembly and quality testing of printed-circuit boards; and a work station integrating design, manufacturing, and testing of electronic cables and harnesses.

Robots with both touch and sight will work in the stations, paired with high-speed computers and advanced software, interactive-graphics-design systems, and computerized data bases. The robots will be central to Westinghouse's design effort. The firm is working in this area already with Japanese firms like Seiko, Fujitsu Ltd., and Hitachi Ltd., as well as with American robotics maker Automatix, Inc., Burlington, Mass., the Carnegie-Mellon Institute, Pittsburgh, Pa., and the University of Rhode Island, which is in Kingston.

High return. Stansberry predicts the project, the first of its kind in that it will affect production across several Air Force programs, should receive a 20- to 30-fold return on its investment over the next 10 years at Westinghouse alone. He adds that the Air Force plans other such contracts under its technology modernization program.

All of these programs will aim at developing widely-available automated-production technologies, and their award will be conditional on a company's willingness to invest its own resources in modernizing its production facilities. **-Linda Lowe**

Personal computers

IBM elects to buy software outside

The long-awaited personal computer from IBM Corp. came as no surprise when it was announced Aug. 12. But the startling fact was that the world's largest computer manufacturer had departed from its traditional software stance of doing everything itself.

Instead, IBM is relying on software expertise that is accumulating explosively in the microcomputer marketplace [*Electronics*, April 21, p. 163]. Software for the IBM Personal Computer is being supplied by outside software vendors. Moreover, IBM is forming a third-party publishing operation that will sign up application programs.

Built around a 16-bit microprocessor, the IBM machine should offer a significant challenge to the personal-computer market now dominated by Tandy Inc.'s Radio Shack and Apple Computer Inc. since it is competitively priced with their 8-bit offerings. In fact, Portia Isaacson of the market research firm, Future Computing Inc., Richardson, Texas, predicts $1 billion in sales for the IBM computer by 1984, calling it

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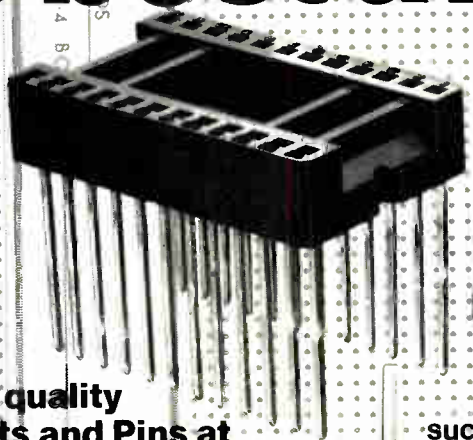

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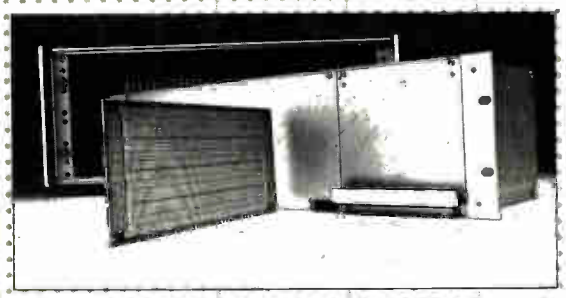

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Little guy. The components of IBM's Personal Computer include an 83-key keyboard, a 12-in. display, and a 16-bit microprocessor with dual 5.25-in. floppy disks.

"the most significant personal computer ever introduced."

Moreover, by designing around a 16-bit chip, IBM has ensured that its computer will have a long product life. Personal computers built around 8-bit processors do not have the processing speed necessary for things like the latest high-speed graphics and real-time interactive games.

In its basic configuration, it costs $1,565, as compared with $1,330 for an Apple II and $870 for Radio Shack's TRS-80. The higher price appears not to be just a reflection of the IBM name, but seems to reside in the quality of construction: 80% American-made, the machine is housed in metal rather than plastic, uses a 12-inch green-phospor cathode-ray tube and generally is more professional-looking than many of its counterparts. Also, it should help maintain U. S. market share, in the face of the Japanese import wave expected in 1982.

Based on Intel's 8088 microprocessor, the Personal Computer is enclosed in a chassis with a detachable 83-key keyboard and separate CRT. It comes with 40-K bytes of read-only memory holding Microsoft

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GENERAL INSTRUMENT

Basic and various system utilities. Its five-slot chassis is fully described by IBM so independent manufacturers may interface with it easily.

The computer employs 5.25-in. floppy disks holding 160-K bytes in IBM's own format, with 8-in. floppies on the way and hard disks further down the line. The display operates in three modes: twenty-four 80-character lines for text, and two color-graphics modes—320- and 640-by-200 picture elements. It also has all the standard home computer features including a speaker for music and inputs for game paddles and controllers.

Vendors. So far, two high-level languages, an operating system, and three applications packages have been written for the IBM computer by outside vendors. The languages use the Basic interpreter and Pascal compiler from Microsoft, which also has written a disk operating system. Personal Software Inc. has adapted VisiCalc, the popular program for handling lists of data. Peachtree Software Inc. has transferred its small-business management package, and Information Unlimited Software Inc., its EasyWriter word processor.

Other operating systems are being developed. Digital Research Inc. is adapting CP/M-86 and SofTech Microsystems Inc. to its UCSD p-system. In addition, IBM has established a software publishing department that will underwrite and market new application programs, paying royalties to authors.

It will, however, be the responsibility of the author to maintain the software. With IBM backing the 8088 architecture with software publishing operations, many more programs should become available.

In a configuration with 64-K bytes of user memory, dual disks and a CRT, the IBM Personal Computer will cost $3,660. That makes it about $450 more expensive than the Apple II, which has fewer features. The prices are almost equal if the Apple is expanded to include the interfaces for an 80-column display and upper- and lower-case characters, which are standard with IBM. **-R. Colin Johnson**

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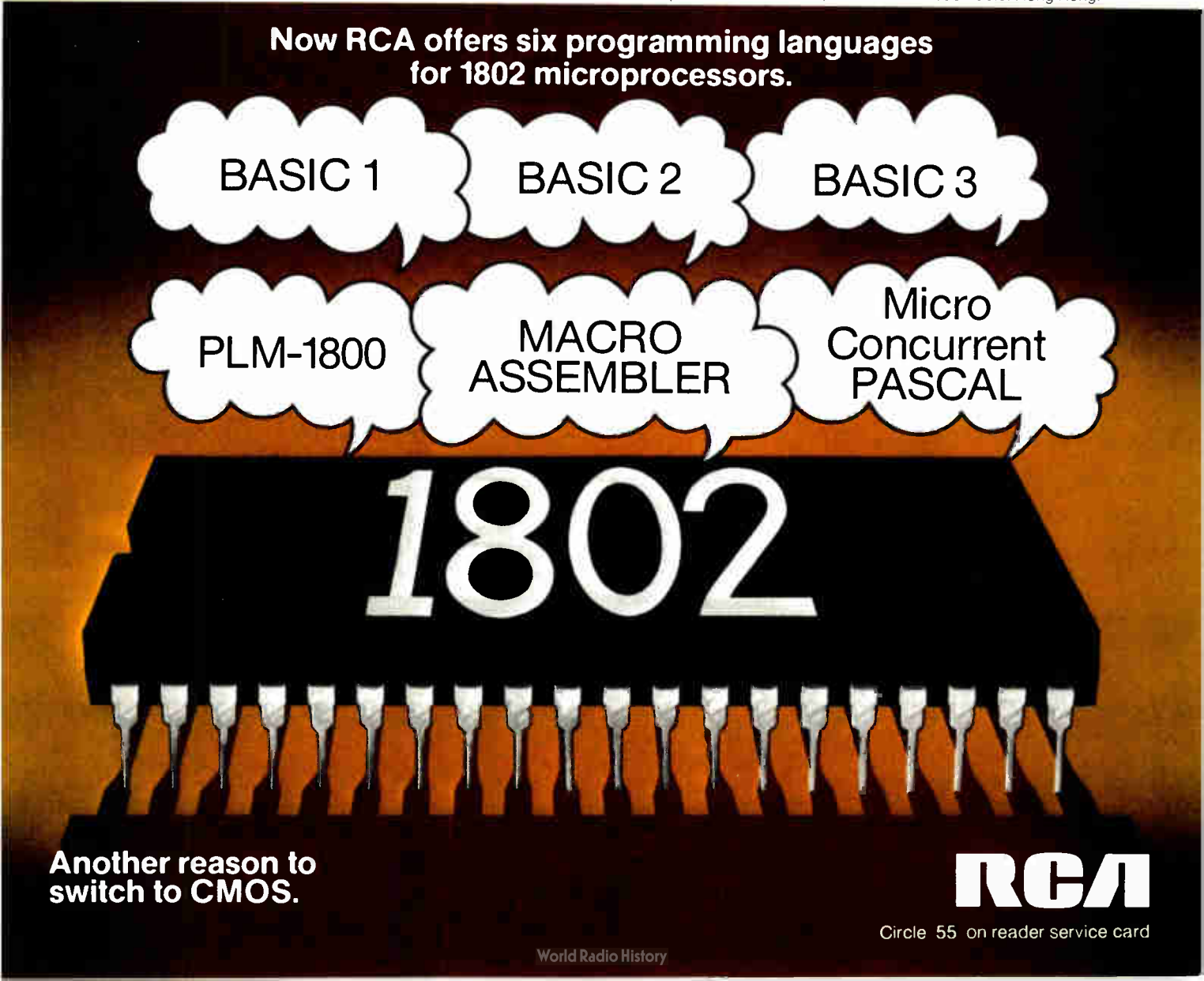

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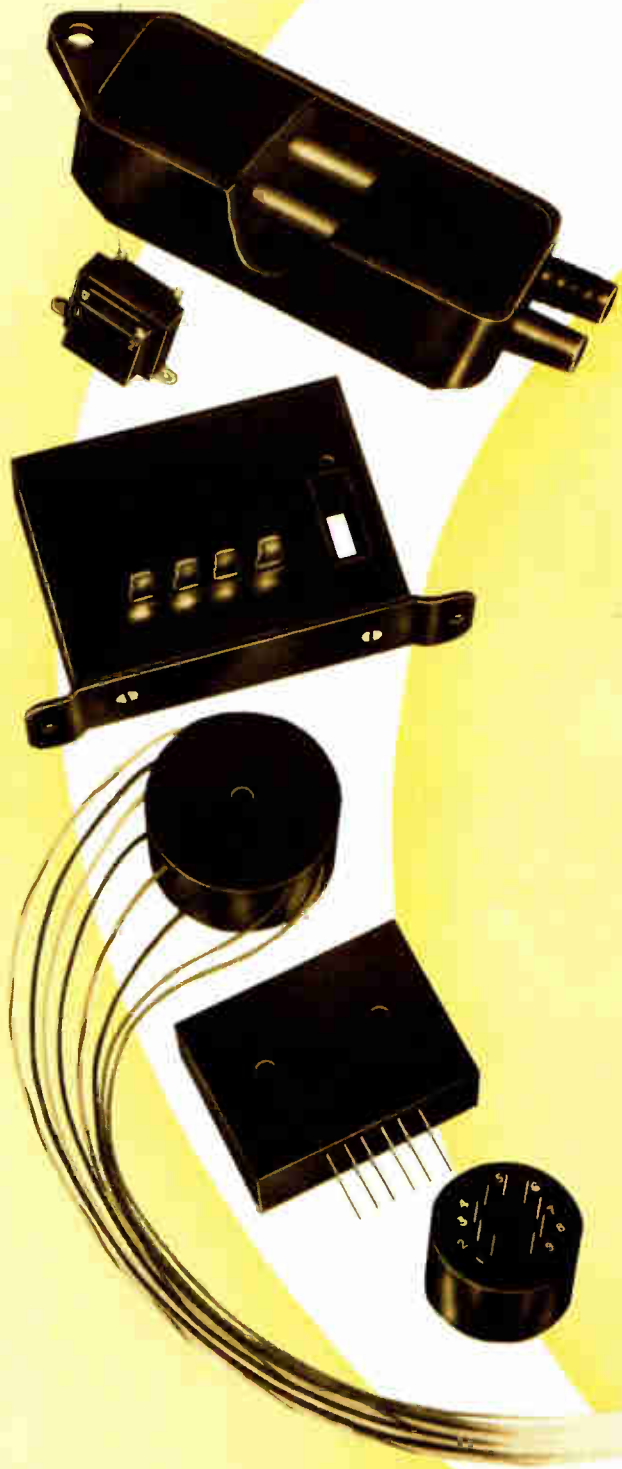

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Washington newsletter

NSA center to rate secure computers . . .

A new Computer Security Technical Evaluation Center is being set up by the National Security Agency for the Department of Defense and the intelligence community, says Adm. Bobby R. Inman, deputy director of central intelligence. Inman, former director of the NSA, the nation's chief cryptographic agency, told a National Bureau of Standards seminar on computer security that the new center will work with industry on developing secure computer systems and software for Government applications as well as in industry. **The center "will not make general endorsements,"** Inman emphasized, but as with the Pentagon's existing Qualified Product List, "the relative merit of a system in the hierarchy of evaluated products may be available publicly in order to provide incentive and encouragement for manufacturers to develop secure systems and for private-sector users to employ them."

. . . with budget set in $25 million range

The NSA Computer Security Evaluation Center will have separate facilities at Friendship, Md., in the industrial complex of the Baltimore-Washington International Airport, moving in "within a month or two," says NSA's George Cotter, the center's acting director. In an interview, Cotter estimated that the CSEC will have an annual budget of $25 million to $30 million, **"about two thirds of which—say, conservatively, $10 million—will be spent on research, development, and procurement"** with industry. Starting small, the CSEC staff will build up to between 200 and 300 persons over the next five years, he adds.

NTT chief to lobby U. S. congressmen

Nippon Telegraph & Telephone Public Corp.'s president, Hisahsi Shinto, is scheduled to spend Sept. 10 and 11 in Washington, D. C., promoting the opening of NTT's domestic telecommunications equipment market for U. S. suppliers in talks with Reagan Administration officials and members of Congress. **The visit is reportedly designed to assuage U. S. fears that Japan's next electronics export assault will come in the $20 billion U. S. telecommunications equipment market.** The 1980 U. S. trade deficit in telephone and telegraph equipment alone totaled $156.7 million last year, up 60% from the year before. The executive's schedule now includes meetings with Secretary of Commerce Malcolm Baldrige and members of the Federal Communications Commission and Congress, plus a reception sponsored by the Electronic Industries Association.

SBS proposes small-business digital network

Satellite Business Systems Inc. wants to build 32 microwave digital termination systems in as many U. S. metropolitan areas to service medium-sized– and small-business communications users. In its filing with the Federal Communications Commission, **the McLean, Va., company says its new data exchange service, called DXS, complies with FCC rules** for digital message services [*Electronics*, Jan. 27, p. 61]. The SBS proposal, using its satellite network as a backbone, calls for installation of a 2-ft-diameter antenna and associated 10-GHz terminal equipment on a user's rooftop or window. The terminal—aimed at a central transceiving station with three antennas that each provide 120° coverage and four-mile range—would have data channels at speeds ranging from 2,400 b/s to 1,544 Mb/s. SBS wants to implement the DXS in mid-1983 between Chicago, Dallas, Los Angeles, New York, and Washington, D. C., with the 27 other systems in place by the end of 1986.

Battling Japan for U. S. telecommunications

Washington's slow and soggy August is being enlivened with a new variation of the electronics trade war with Japan. It seems only yesterday that the conflict involved was the Japanese dumping of television receivers. Japan in effect won that battle, driving most American manufacturers either from the market or to offshore plants.

The new battle involves alleged Japanese dumping of telecommunications equipment, specifically high-powered amplifiers for domestic satellite earth stations (see p. 42). American manufacturers say that they have learned from the earlier bitter experience, and they are determined not to lose this one.

That determination was illustrated last month when the Electronic Industries Association's John Sodolski warned a House trade subcommittee that the $20 billion domestic telecommunications equipment market—about half the world total—is being "specifically targeted for a concerted attack by foreign competitors" whose home markets remain closed to U. S. exports [*Electronics*, July 14, p. 58]. What distresses EIA members most, says communications division vice president Sodolski, is that equipment makers in Japan and Europe can "price and sell marginally, especially in the United States," while supported by "assured long-term manufacturing contracts and [government]-subsidized research and development" at home.

Now the EIA division members are taking up the battle in earnest, building a war chest to support Aydin Corp. of Fort Washington, Pa., as it steps into the International Trade Commission arena. Aydin is charging that the Nippon Electric Co. of Tokyo is selling two types of earth station amplifiers to Communications Satellite Corp. at less than fair value—lower than the price set for the Japanese market—and thus threatening to damage U. S. industry. That is dumping.

A difficult case

As the U. S. telecommunications equipment trade deficit with Japan continues to expand, the timing seems right for the EIA move. Yet there are indications in the initial Aydin petition and the NEC rebuttal that the EIA may be backing the wrong American warrior in the upcoming battle.

In what shapes up as a down-and-dirty fight—with Comsat saying only that NEC's products were "technically superior"—Aydin will have a hard time proving not only that NEC's prices were below those in Japan, but also that Aydin has been or is likely to be damaged by the Comsat buy.

Aydin admits that Japan has few earth stations and that an accurate breakout of component prices is impossible because the stations are installed as complete turnkey packages. The company has therefore had to estimate and then reconstruct NEC's component costs for the amplifiers, using figures that NEC says represent "fanciful adjustments" to accurate prices and costs. NEC contends that its costs are lower because it is a vertically integrated manufacturer producing all the earth-station amplifier components for the uplink, while Aydin makes none of the components, buying them in the open market for assembly.

As to damage, NEC rejects Aydin's complaint by noting that the Pennsylvania company told the Securities and Exchange Commission and its stockholders in its April 27 first quarter earnings report that 1981 would be "another record year" for the company, even though NEC says the forecast came "after Aydin knew it had lost the Comsat contracts" in January and said nothing about it.

Equally troubling is the suggestion by NEC's lawyers that Aydin may have engaged in improprieties with Varian Associates, another losing competitor for the Comsat contracts. Price fixing is a serious charge and, of course, must be proven. As Japan knows well, it is not a practice peculiar to the U. S.

The impact of politics

In sum, however, Aydin's initial petition and the rebuttal by NEC indicate that U. S. manufacturers need to make a stronger case for telecommunications equipment dumping by Japan or anyone else than is evidenced in this first effort, for U. S. industry is handicapped, so to speak, by a regulatory and judicial system in which the burden of proof is on the petitioner. If the ITC or the Department of Commerce decides that Aydin's charges are worth a full investigation—and they may do so—it will likely be more a product of international politics than anything else, a welcome result of the Reagan Administration's toughening stance on equal access to Japanese and other national markets for U. S. industry. **-Ray Connolly**

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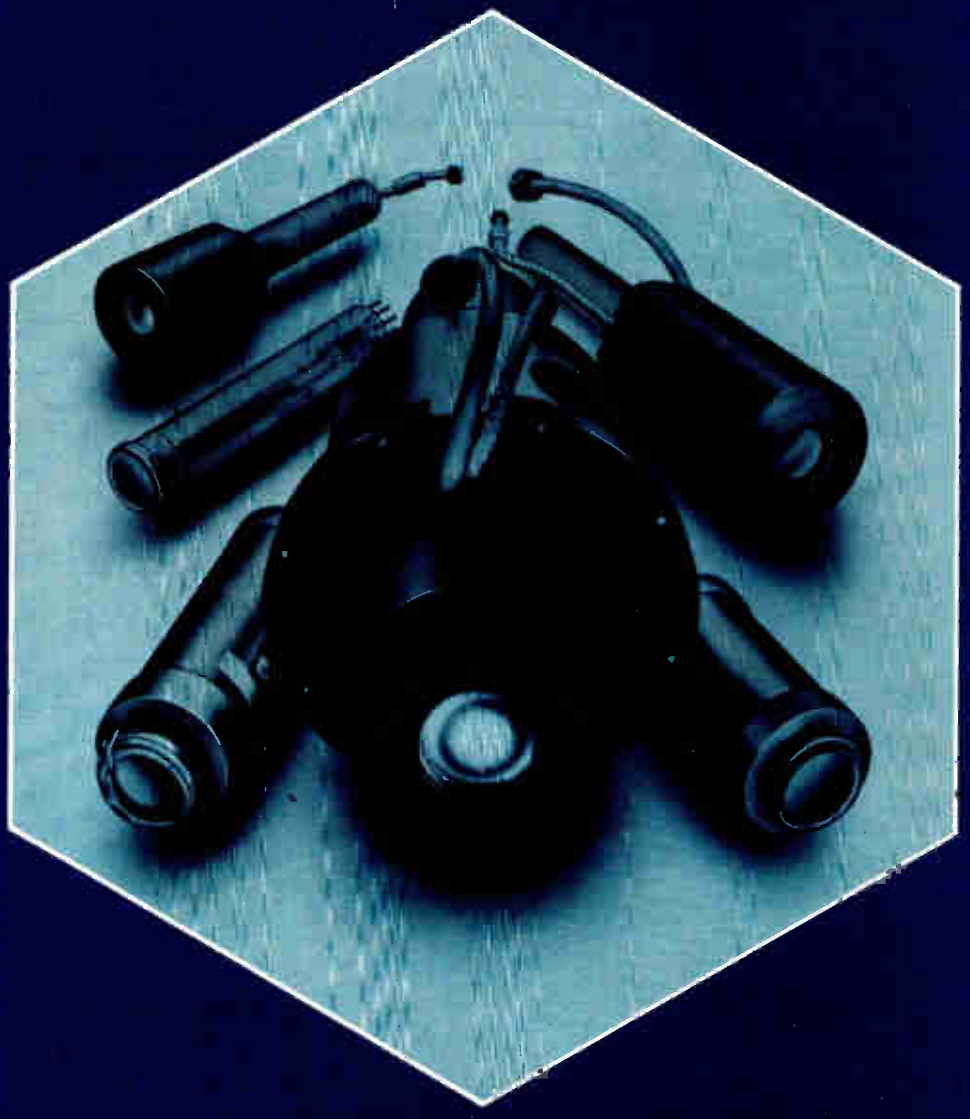

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August 25, 1981

Electronics International

Multimicroprocessor machine goes commercial: page 73

A large and a small Josephson junction below two control lines (across top) create compact three-dimensional AND gate: page 74

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PHASE C          300Vac
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PHASE B PULSE  595Vpk
PHASE C PULSE  604Vpk
DC              10.0Vdc
FREQUENCY       50.0 Hz
**********************

TIME          10:46:33
DC  HIGH        46:33
DC MAX 14.1V    46:47
DC  HIGH        46:47
A   UNDER       47:00
A MIN   92V   810 mS
A   OVER        47:09
A MAX  135V     47:10
A   PULSE -     47:20
A       101V    17 uS
ON BATTERY    10:49:57
POWER ON      10:50:03
A MIN    0V     50:03
DC MIN  0.0V    50:03
A   UNDER       50:04
A MIN  105V     10 mS
FREQ MIN 56.8   50 mS

****** STATUS ******
DATE          07-29-81
TIME          10:50:17
        INPUTS
PHASE A         115 Vac
PHASE B         115 Vac
PHASE C         115 Vac
3PH             112 Vac
DC              5.1 Vdc
FREQUENCY     60.0  Hz

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International newsletter

European market gets own CCD TV camera

A miniature black and white camera weighing just 2.2 lb that conforms to Europe's 625-line standard—unlike the 525-line standard adopted by U. S. and Japanese manufacturers—will be available next month from Britain's English Electric Co., Chelmsford, Essex, which is part of the General Electric Co. Ltd. group [*Electronics*, Sept. 11, 1980, p. 78]. The 13-cm-long, 6.4-cm-wide and 20.4-cm-high camera **uses a charge-coupled-device imager from GEC's Hirst Research Centre that packs 220,000 imaging elements onto a 1-by-1.4-cm chip.** The resolution—about 67% that of TV studio broadcast cameras—is better than already marketed home video equipment, says the company, and suitable for closed-circuit TV and industrial applications. The price has yet to be fixed but may well be under $4,000.

VHD video-disk launch delayed

Unable as yet to mass-produce disks, the international consortium of four companies developing the Video High Density video-disk format has announced a six-month delay in its product launch. VHD thus stands to lose further ground to the two alternative and incompatible RCA and Philips formats already on sale in the U. S. At a recent meeting in Los Angeles, top officials of Victor Co. of Japan, Matsushita Electric Industrial Co., General Electric Co., and Thorn EMI PLC decided to postpone introduction of their system until at least April in Japan and June in the U. S. Also likely to suffer are the 11 Japanese companies that have bought production rights to VHD. Many have invested in plants, and some, according to industry experts, have already started making players, which are worthless without disks to play. Meanwhile, **Pioneer Electronic Corp. revealed plans to become the first video-disk marketer in Japan** by starting to sell 5,000 Philips-type players early next month.

Netherlands charts three-way course for microelectronics

The Netherlands' Ministry of Science is currently drawing up a program for spending up to $10 million a year on promoting the application of microelectronic devices by small and medium-sized Dutch firms. The program has three parts. The first is the establishment of three consulting centers by the end of this year to which the firms can turn for technical, managerial, and marketing advice on the microelectronic-based products they are designing. **The second will give financial help to small and medium-sized companies engaged in the design of chancy products** using new microelectronic technologies. If a product proves commercially successful, the company must repay up to 70% of the government's financial aid. The third portion will help universities expand their research and development facilities to accommodate more graduate students.

Scrambling repels software pirates

Piracy of disk-based software for personal computer systems is a growing problem in the software industry, especially when software crosses national boundaries. But one British software publisher, London-based Little Genius Ltd., thinks it has the answer. It has developed a copy-proofing technique with which it plans to protect its own software—interactive teaching aids for Basic and Pascal programming—and which it is prepared to license. **The technique is to scramble the software before it goes on disk,** prefacing a program so stored with a preamble that configures the target machine to read it alone. Attempts to copy unscrambled programs trigger traps that erase them from user memory.

International newsletter

Israeli optical switch deflects fiber

A small Israeli company, Arel Control Systems Ltd., has constructed a prototype 2-by-2 optical switch, the forerunner of a 16-by-16 switch, **for use in analog optical exchanges such as closed-circuit TV or fiber-optic digital data networks.** The device is electromechanical: vertical and horizontal deflectors—piezoelectric elements mounted end to end in one pliable component—position an optical fiber within the focal plane of a miniature lens whose output is a collimated beam 3 mm in diameter. The deflectors steer the beam between two photodiode detector/repeaters.

Three firms to submit proposals for Japan's Badge defense system

The Japan Defense Agency has officially requested proposals by early next year for a new Badge (for base air-defense ground-environment) system from three of the five Japanese manufacturers preparing for the project [*Electronics*, July 14, p. 64]. Nippon Electric Co., Hitachi Ltd., and Fujitsu Ltd. were selected by the agency because only they among Japanese firms have both the computer and communications expertise required for the job, which includes **upgrading command installations at 27 sites throughout the archipelago and communications among them.**

NEC intends to bid as main contractor in a group that includes subcontractors Mitsubishi Electric, Toshiba, Oki Electric Industry, and Nippon Avionics (Nippon Avionics is a joint venture 51% owned by NEC and 49% owned by Hughes Aircraft). Hitachi is negotiating with System Development Corp., a U. S. firm, for the purchase of application software for use in this project.

Matilda tells it to the marines

The talking computer that warns a crew of danger is no longer science fiction. Called Matilda, it has been developed for the smaller class of warship by MEL, a division of Philips Industries Ltd. located in Crawley, Sussex. **The synthesized voice also indicates from which direction the radar-detected threat may be expected,** and a visual display simultaneously provides the same information to a command position. The miniature rapid-reaction system, which automatically initiates countermeasures, is on display at the Royal Navy Equipment Exhibition in Portsmouth, Sept. 7–11, an export promotion for UK manufacturers of defense equipment.

Japanese-American team to make C-MOS gate arrays

Complementary-MOS silicon-gate logic arrays customized by LSI Logic Corp. in Santa Clara, Calif., may be shipped to U. S. buyers next spring before wafer supplier Toshiba Corp. can ready chips for its Japanese customers. Toshiba will ship the wafers on a nonexclusive basis, complete except for two layers of aluminum interconnections, which LSI Logic will add with the aid of its LDS I development system before packaging the chips. A high-speed series will become available first, initially **in 880- and 2,000-gate devices, using 3-μm rules and offering typical per-gate propagation delays of 2.5 ns.** Late next year, a very high-speed series, using 2-μm rules and offering 1.5-ns delays, will become available, to begin with in 880-, 2,000-, and 6,000-gate densities.

Addendum

Malta, as the last European country to do so, has begun color TV transmission using the West German–developed PAL system. For starters, the country has **put Grundig AG under contract to supply it with some 10,000 color sets.**

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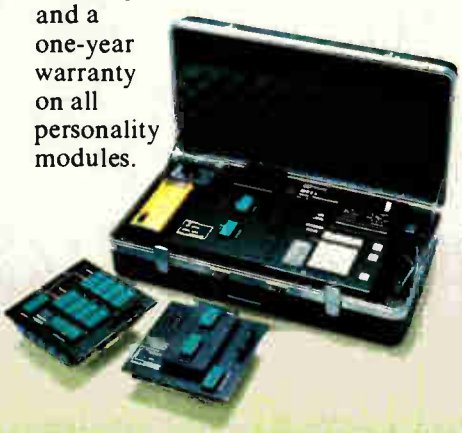

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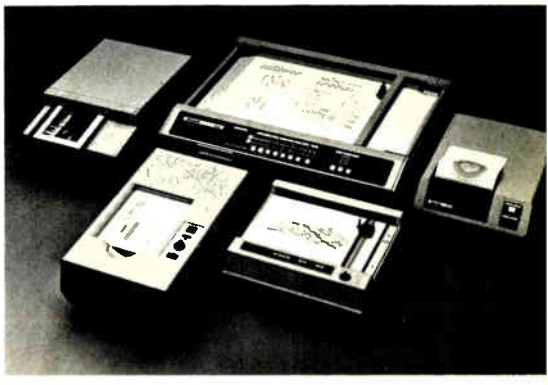

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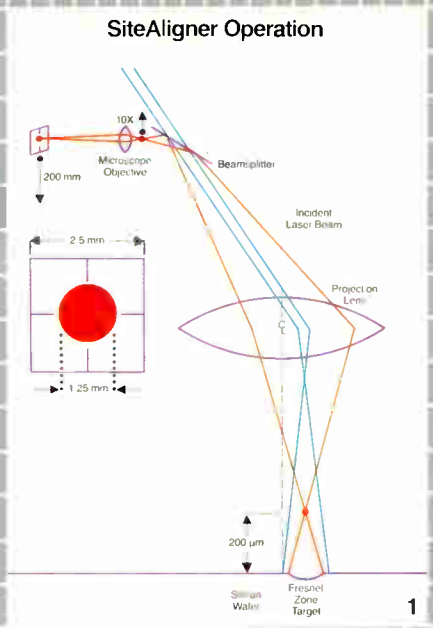

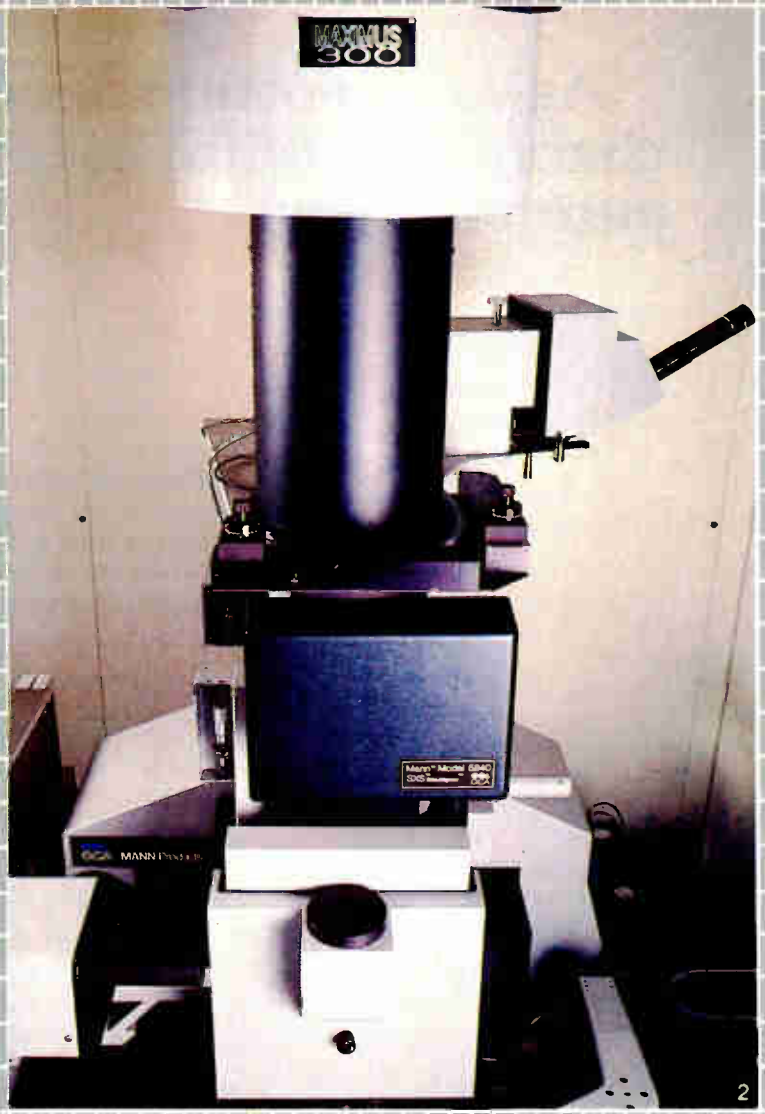

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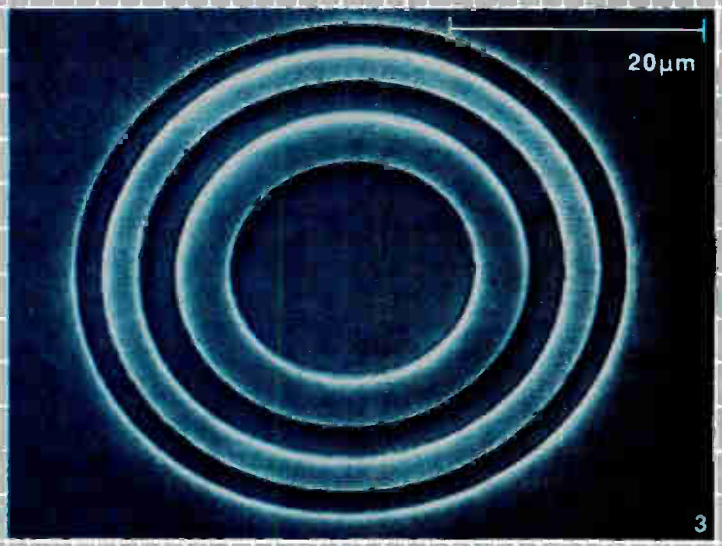

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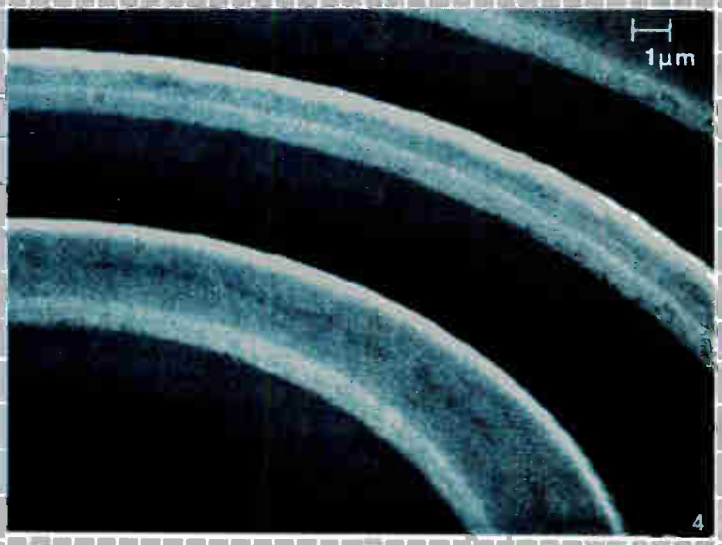

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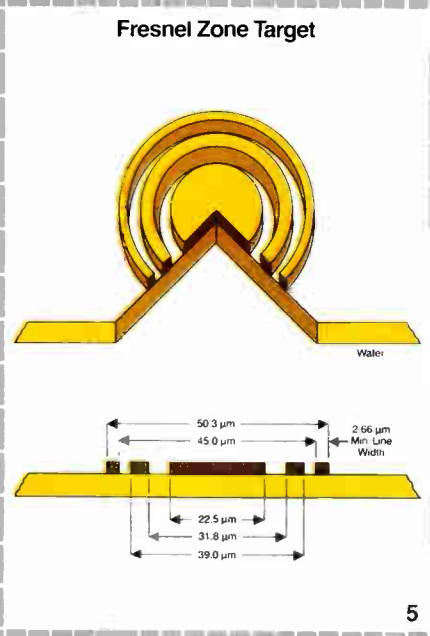

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1. Optical schematic of Mann Model 5840 SXS™ SiteAligner.™

2. SiteAligner mounted on the DSW® Wafer Stepper™ direct step on the wafer system.

3. Scanning Electron Microscope photo of Fresnel Zone Target on wafer (approx. 1600X).

4. Scanning Electron Microscope photo of Fresnel Zone Target on wafer (approx. 3000X).

5. Diagram of the Fresnel Zone Target. The Fresnel Zone Target allows alignment even if a target is damaged.

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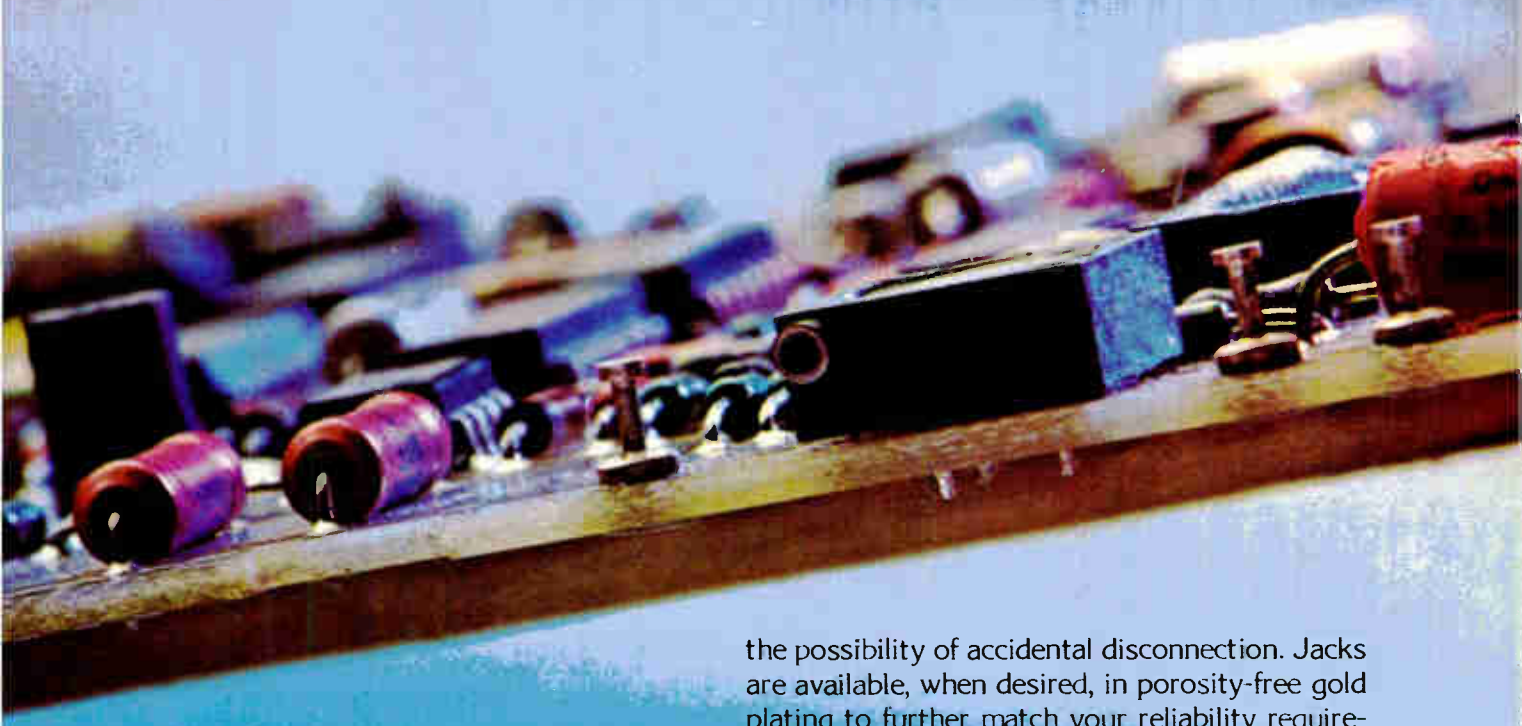

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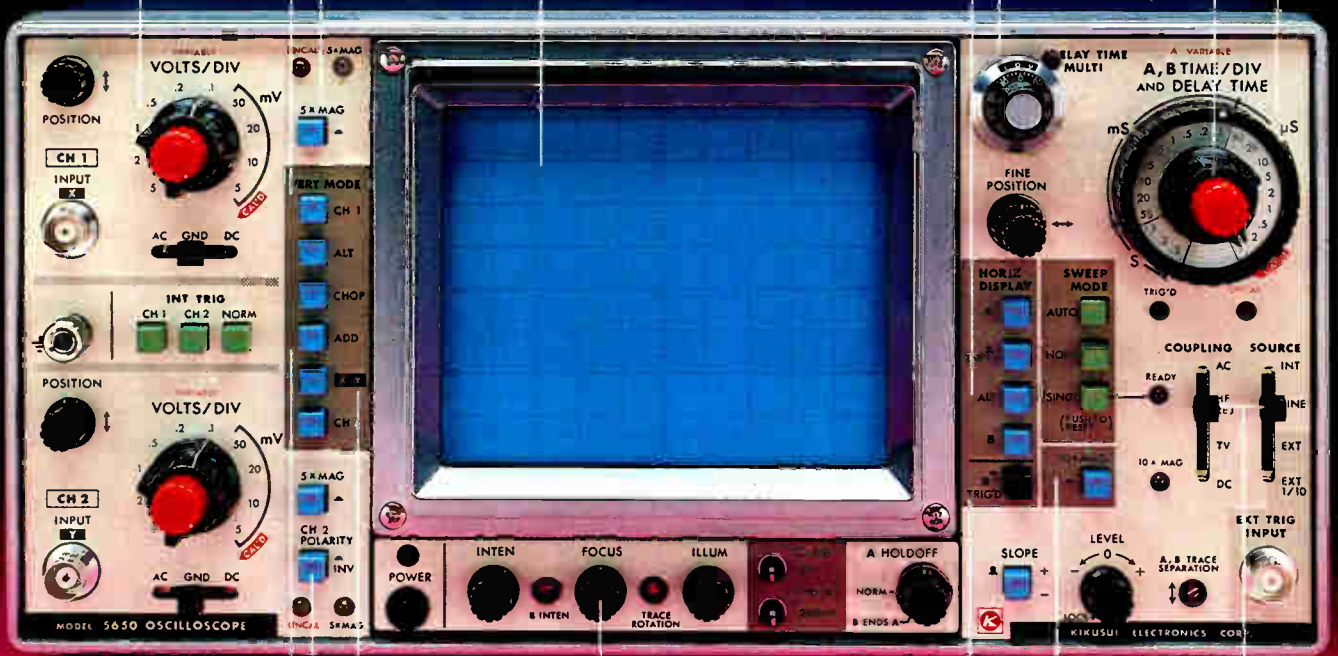

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Microprocessors in a ring take aim at mainframes

by Kevin Smith, London bureau manager

Commercial 16-chip unit is installed, even as research makes it possible to use 250 microprocessor chips

Powerful computer systems built from assemblies of inexpensive microprocessors may soon be ready to take on the conventional mainframe in industrial control, communications, data-base management, and other projects with a high degree of inherent parallelism. For example, the Demos design that began four years ago at Britain's National Physical Laboratory in Teddington, Middlesex, will shortly start earning its keep as an industrial controller, process monitor, and data-acquisition system.

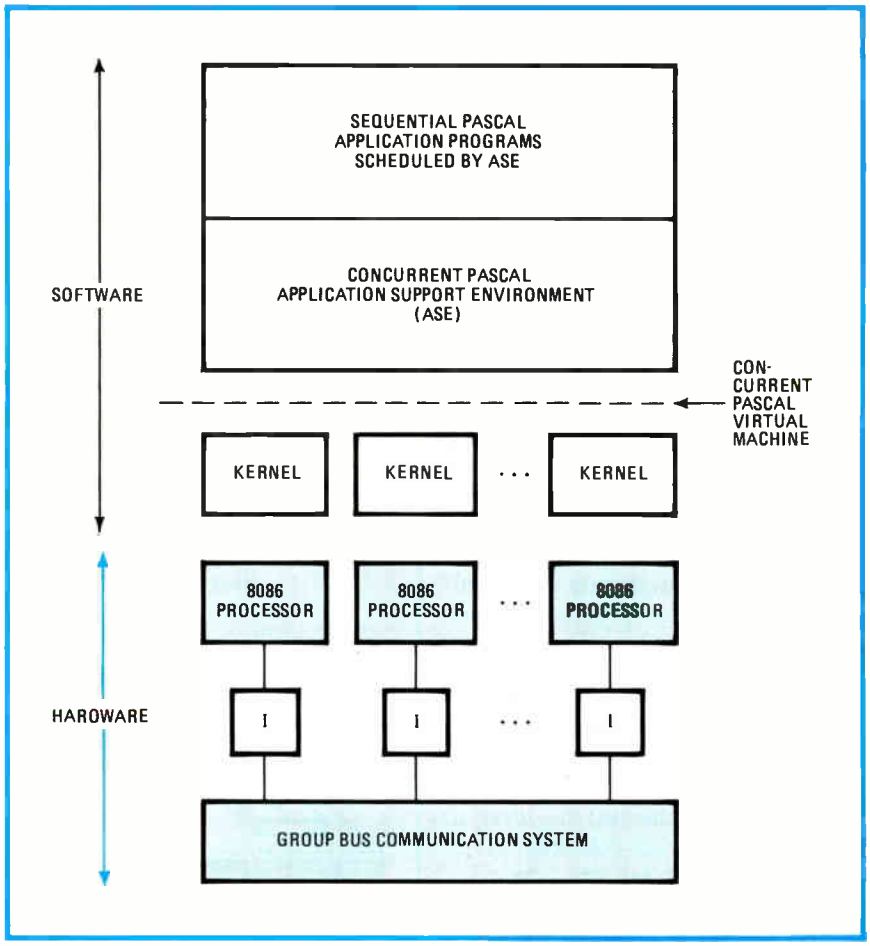
The machine has been given commercial form by Scicon Consultancy International, a subsidiary of British Petroleum Ltd., which is currently installing its first Scidac system at a customer's site. For it, Scicon uses an adaptation of the laboratory's earlier ring to run just 16 microprocessors—actually 16-bit Intel 8086s—in parallel.

Ring change. But much more powerful multiprocessor arrays are already on the way. NPL engineers are now completing development of a high-speed local ring that will run 250 microprocessors in harness as a single virtual machine.

Apart from supporting tightly coupled microprocessor arrays, the Mark II ring has other potential applications, for which NPL is seeking backers. With a data rate of 60 megabits per second over a local 8-bit bus, a worst-case response time of 4 milliseconds, and an ability to share capacity equally between users when fully loaded, it is suitable for use in office automation, private automatic branch exchanges, and other applications where voice and data must be combined.

The earlier Mark I ring proved too expensive for commercial realization, which was why Scicon adopted a far simpler bus system. But in reengineering its ring, NPL has taken advantage of the latest programmable logic array concepts, and is now projecting a very competitive $1,000 per ring node.

In Demos, the 8086 processors have their own individual stores and internal buses and communicate with each other over a unidirectional high-speed ring rather than through



Virtual machine. Programmers can write modules in sequential Pascal for Scidac system unaware of its complexity—16 microprocessors linked to a bus by interface boards (I).

shared memory. High-speed kernels handle interprocessor messages as procedure calls. Such calls conventionally fetch the needed subroutines into main memory for sequential processing, but in a distributed processor each call is routed to the processor dedicated to that task, which returns its results.

This arrangement, argues Barrie Brinkman, who heads the Scidac project at Scicon, is simpler, cheaper, and more flexible than the shared-memory approach. Moreover, the communications interface does not have to map messages into the addressed processors, so that memory is relatively hardware-independent. Consequently new micoprocessor products can readily be absorbed as they become available.

Transparent. Ideally, the user of a multiprocessor array should be unaware of the complexity of his system. In Demos, a user's application programs can be written as if for a single virtual machine, using a modular programming language like sequential Pascal. The component software modules are then allocated among processors during loading.

The operating system for Demos, however, is written in concurrent Pascal, which, says Peter T. Wilkinson, who heads the NPL project, lends itself to parallel processing with very clean interfaces between modules and allows fast high-quality programs to be written. Once a system has been developed for target configuration, its performance can be increased by the addition of more computer power without the need for software changes. This is achieved in a once-only operation with the aid of a system generator program, which reallocates the operating system modules among the available hardware, as the operator directs.

Fast interprocessor communication is essential for Demos to behave as a single virtual machine. The Mark II ring achieves this over a byte-wide data bus clocked at 8 megahertz. Messages are transmitted, a package at a time, by a token-passing system and can be up to 65 bytes long. The virtue of this organization is a fast response, as well as shared capacity between users when the bus is fully loaded.

In the Mark I ring, interface logic per port amounted to some 28 small-scale integrated circuits, but the Mark II ring uses field-programmable logic sequencers to cut the chip count to 25 devices per port. These fit on a double Eurocard.

Potential users, like Britain's Central Electricity Board, have been impressed with the ring hardware, and now NPL is talking to several manufacturers interested in commercializing it. Work at NPL and at London-based Scicon meanwhile is going ahead to further develop the system's fault tolerance.

Switzerland

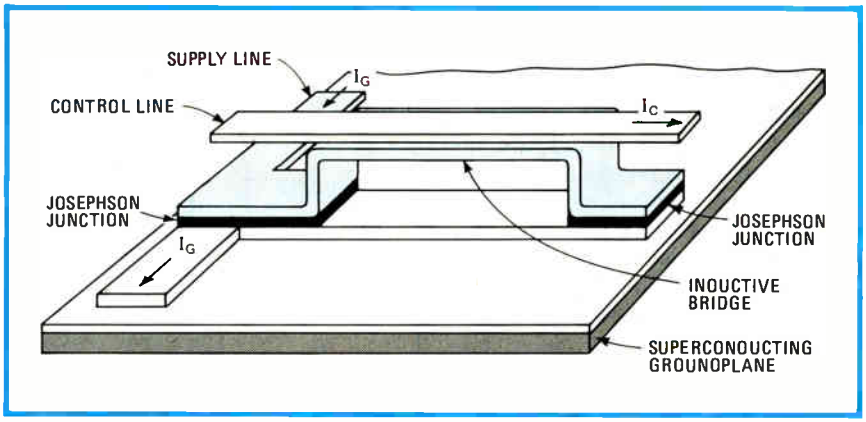
Two Josephson junctions in one device triple logic circuitry density

When it comes to Josephson junction technology, it's clearly International Business Machines Corp. that is leading the field, with hardly a year going by without experts at the company's research laboratories in Yorktown Heights, N. Y., edging toward a full-blown superconducting Josephson computer. [*Electronics*, Feb. 16, 1978, p. 43; Jan. 3, 1980, p. 41]. Now comes word of another major advance in the field from the IBM Zurich Research Laboratory of Rüschlikon, Switzerland.

There researcher Hansjörg Beha has designed and tested a new family of Josephson logic circuits termed magnetically coupled asymmetric interferometer logic—Mail, for short. To be discussed at the Seventh European Solid State Circuits Conference in Freiburg, West Germany, Sept. 22 to 24, the Mail device is an asymmetric two–Josephson-junction interferometer—asymmetric because one junction is much larger than the other (see figure).

Beha's work at the Zurich labs draws upon the investigations he carried out at the University of Karlsruhe in West Germany, where in 1977 he first proposed such an interferometer as a logic gate. The key feature of the Mail device is that it combines galvanic isolation and logic operation in a single device, in contrast to other Josephson logic families. The single-device implementation, achieved essentially by the asymmetric junction areas, yields triple the density of other Josephson logic components.

High gain. Furthermore, the threshold characteristic of Mail circuits is so steep as to make them insensitive to control current variations. Also, they exhibit high gain compared with other Josephson de-



Denser. Compact Josephson design uses two differently sized junctions. An AND gate results if a second control line crosses inductive bridge, parallel to that shown.

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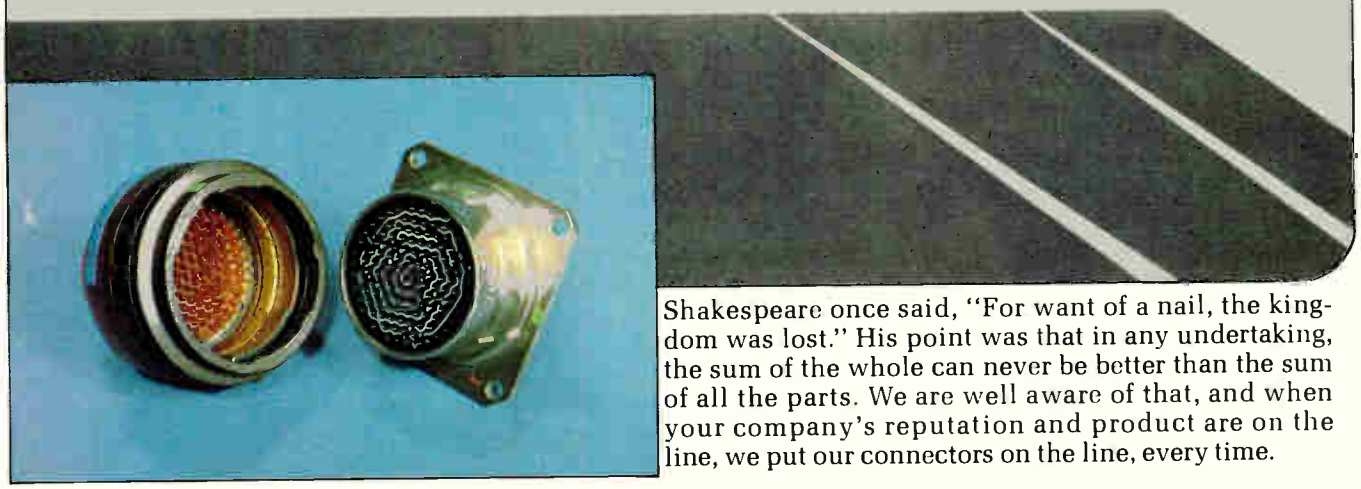

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vices. With the control current at its threshold value and with one junction area five times bigger than the other, the gain at the circuit's optimum gate current insertion point checks in at 9.8.

Computer calculations with OR and AND Mail device models based on 2.5-micrometer technology and lead electrodes point to a nominal gate delay of 25 picoseconds and a power dissipation of 5 microwatts per gate. That works out to a power-delay product of only 125 attojoules—at least three orders of magnitude smaller than that for silicon or gallium arsenide devices.

In a single-device two-input AND Mail circuit, the gate current I_G is applied to the larger Josephson junction, and currents along two control lines (one for each junction) set up the magnetic field coupling the inductance to the interferometer portion. The output line ends in a load resistor that matches the line's characteristic impedance. Connecting several such resistors in series permits a large fanout.

A proper choice of the ratio of the junction areas, and thus of the Josephson current ratio results in an almost ideal threshold characteristic for performing the AND function. The device switches from the superconducting logic 0 state to the voltage or logic 1 state when both control signals are applied. To convert an AND circuit into a two-input OR circuit, a third control line carrying a bias circuit must be added to the other two.

The interest of IBM—and of other computer makers, notably the Japanese—in Josephson devices is understandable. Dissipating about 0.1% the power of silicon circuits and exhibiting switching speeds of around 10 ps, Josephson components are at present considered the best way to large computers with cycle times approaching 1 nanosecond. What's more, their low power consumption makes very dense, three-dimensional circuit packages possible to build.

A major barrier that must still be overcome, however, is high fabrication cost. **-John Gosch**

Great Britain

Cuts and soldered wire links customize multilayer board in one or two weeks

One major bottleneck in the development of high-speed logic systems, the long 12-week turnaround times associated with multilayer boards, has been overcome by ICL Logic-layer Ltd., the Manchester-based printed-circuit–board manufacturing subsidiary of Britain's ICL Ltd. It has introduced a prototyping board, called Multiboard, for four-layer boards that can be customized with nothing more than a scalpel to remove unwanted track and soldered wire links to complete the desired pad connections.

With the kit, completed boards with component densities and electrical characteristics on a par with boards made from final artwork can be fabricated in one to two weeks, saving 10 weeks of development time and $5,000. If further modifications are required, the savings multiply. The company is marketing the kit in Europe, where, according to product marketing manager Jim Betts, it has been well received, and will be launching it in the U. S. next year, when the firm will have readied supporting computer design aids.

Difficult behavior. Double- and single-sided board prototyping kits such as socket and wrapped-wire boards are well established, but they neither look like a finished multilayer board nor behave in the same way when system logic is ticking at 10 to 20 megahertz and more. In the multilayer printed-circuit board, signal paths appear as matched 50-ohm transmission lines, eliminating the problem.

A Multiboard is the size of a double Eurocard—233 by 160 millimeters—and by itself sells for around $315. Its two inner layers carry a pair of interleaved power planes and a ground plane. X and Y logic tracks are carried on the two outer surfaces. The board is predrilled on a regular matrix with holes on an accurate 0.1-inch pitch. It will accept most integrated-circuit packages with a lead spacing of 0.3 to 0.6 in. "We can get between 35 and 40 packages, or up to 650 pins, on a board," says Betts, who reckons that compares well with a fully custom board.

The board has plated through-holes located at strategic intervals to connect to the ground and supply planes. Supply pads, says marketing manager Jim Betts, will always be between one to one and a half pitches of an IC's supply pins, no matter where it is placed on the board. Single tracks are laid between rows of holes with regular connections to every third pad. Unwanted tracks can be sectioned with a scalpel nick and the redundant sections peeled off.

Bridging the gaps. Where necessary, links between pads or between an IC lead and a pad are formed from solid tinned-copper wire. When bridging surface tracks, the links are sleeved. The board's 50-Ω characteristic impedance is maintained regardless of customizing. A bridge link, for example, alters the characteristic impedance by less than 0.5 Ω.

Changes of direction from X tracks atop the surface to Y tracks beneath are accomplished through copper-filled vias and additional bridge links, if needed. The board's X-Y structure lends itself to the development of logical bus-structured layouts, with buses formed on one plane and connections to them made on the other plane.

Customizing a multilayer board is a relatively simply though somewhat painstaking task. The circuit layout is first worked out on a pad diagram, marking logic connections, links, and nicks in pencils of different colors. When the design has been finalized, it can be recorded as a cut-and-link program produced on a pad address

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form. This data can be used by a technician to produce prototype boards and, if satisfactory, provides fully sufficient information for the manufacture of a customized multilayer board.

A natural next step is to commit the design layout to a small personal computer. The resulting cut-and-link program can subsequently be used to generate the artwork for a fully customized multilayer circuit board automatically.

-Kevin Smith

Japan

Gate–turn-off thyristors, microprocessors help to shrink subway trains

A minisubway being developed for the Osaka Rapid Transit Authority may provide Japanese heavy electrical manufacturers with their first opportunity to combine variable-voltage variable-frequency inverters and alternating-current traction motors with regenerative braking in subway trains.

The fact that the inverter-induction motor drive is smaller than the present chopper-series motor drive makes it indispensable for the minisubway, and prototypes mounted in old coaches have been in operation on a 300-meter test track since July 22. But it also has other outstanding features that guarantee it will be the wave of the future.

Variations. A group of three manufacturers—Toshiba Corp. and Mitsubishi Electric Corp. led by Hitachi Ltd.—are developing the traction equipment. Yoshihiko Syoyama, manager of Hitachi's rolling stock and facility engineering department, says that they will develop standard specifications for the equipment but that each firm's designs will reflect its own technology and so be slightly different.

For instance, each firm has developed gate–turn-off thyristors suitable for use in three-phase inverters operating from the 750-volt dc third rail of the proposed subway. GTOs simplify the design and eliminate the bulk and weight of the auxiliary thyristors and inductance-capacitance circuits needed to commutate inverters using silicon controlled rectifiers.

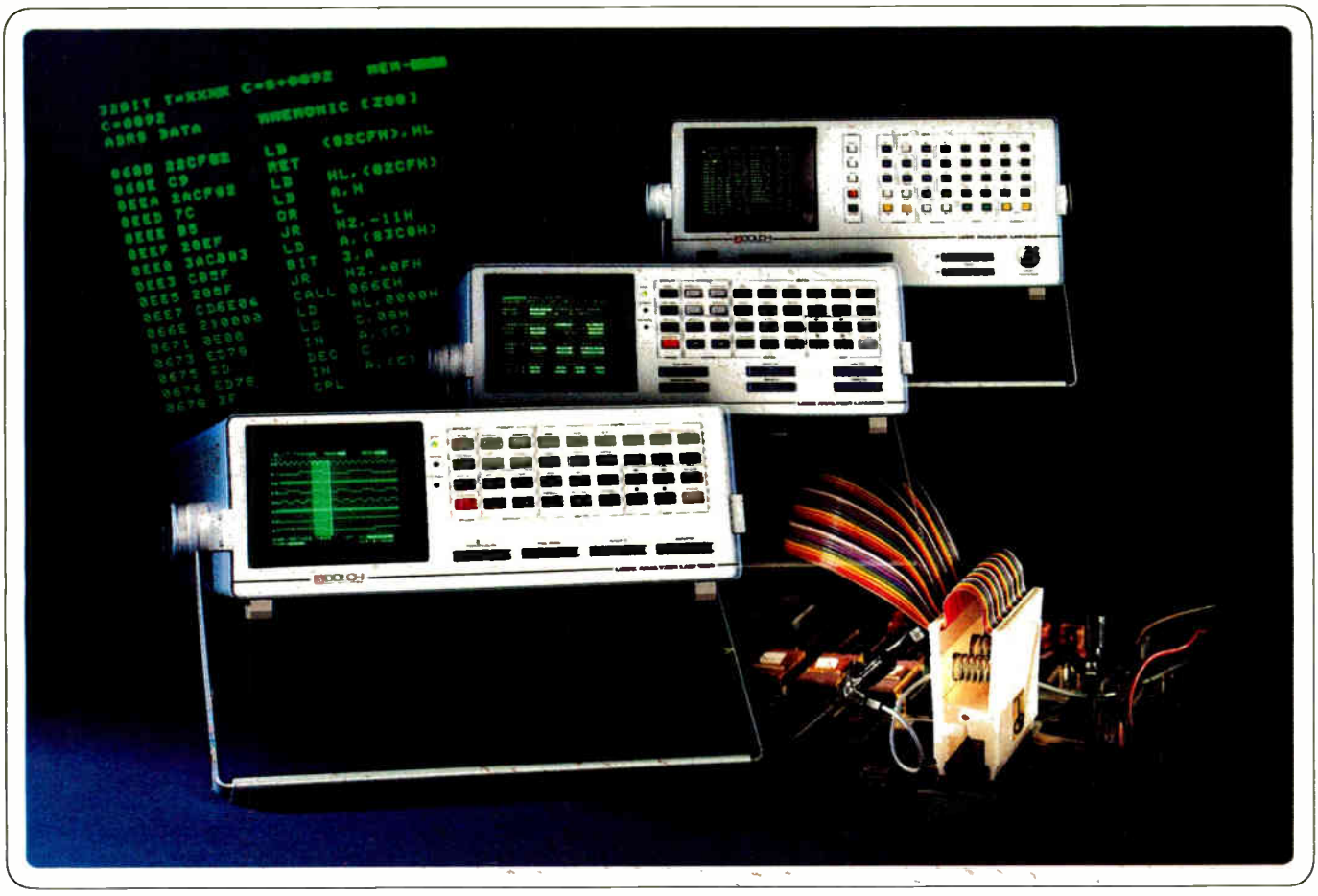
Smart. Each company also has developed microcomputer-based controls to provide the pulse-width modulation that enables the GTOs to invert the dc supply to alternating current varying between 3 and 125 hertz. The voltage maintained by the circuits must be constant over the higher part of the frequency range and proportional to frequency over the lower part.

Tests show that the lighter weight and improved traction of inverter

Smaller is better in subways, too

Osaka's municipal transportation bureau is considering building a minisubway in outlying districts, where there are too few people to justify the expense of a full-size subway yet too many to be transported efficiently with buses. Such a service could start in 1990. Passenger coach floors will be lowered by 34 centimeters (13.4 inches) to provide more than half of the overall height reduction of 65 cm (25.6 in.), while width will also be decreased by 40 cm (15.8 in.) from that of the standard coach. Thus the trains will be able to travel in a tube with an inside diameter of only 4.1 meters (13 feet 5 inches) compared with the normal 5.7 (18 ft 8 in.).

Since most subways are now bored rather than dug by a cut and fill method, the minisubway pays off in a tremendous reduction of energy for boring and in the amount of dirt that needs to be removed and carried away. There is also a saving in cost of concrete to line the tunnels. The more efficient trains further contribute to energy savings during operation.



16 TO 96

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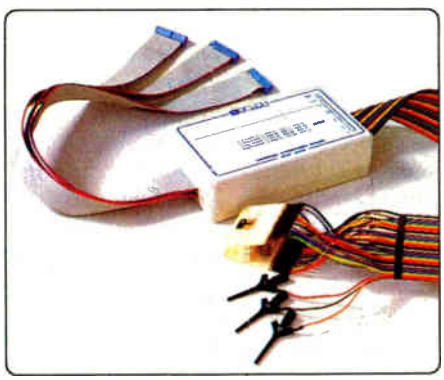

With a new channel expansion probe, Dolch's line of 16, 32 and 48 channel Logic Analyzers can easily be extended by a factor of two.

Disassembling bus activity and displaying the state information in Mnemonic code is the most efficient method of tracing program execution. Dolch proudly provides the industry's widest selection of μP personality probes and disassembly firmware, for both 8 and 16 bit machines, as well as standard bus interfaces (GPIB & RS 232).

Multilevel triggering, as provided in all Dolch Logic Analyzers, proves extremely useful in the debugging of a program that contains multiple levels of nested sub-routines.

A Battery-Backed Menu Memory is one of Dolch's many unique contributions to the industry. It lets you store up to 6 separate files of display and menu parameters, for up to three months without power. This allows you to recall complete test setups with a single keystroke.

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dli DOLCH
LOGIC INSTRUMENTS

drives enable them to operate with less energy consumption than chopper drives, even though the normal efficiency of the components is lower. Typically, dc motors have a 92% efficiency and ac motors one of only 90%, whereas chopper motors are 99% and inverters 97% efficient.

A full-size train operating at 32 kilometers per hour between stations 1.2 km apart regenerates 26% of its energy with chopper drive and 30% with inverter drives.

Adding up the pluses. Overall, the three-phase ac induction motor and its controls will be only about 80% as large and 90% as heavy as the series dc motor classically used in subway trains. Moreover, the induction generator can handle regenerative braking even at the highest speeds, but dc motors and chopper drives can control regenerative braking only at moderate to slow speeds.

During normal operation the rotor on an induction motor typically rotates several percent below synchronous speed, which is the speed of the rotating magnetic field set up by its stator. This mode of operation in effect raises the coefficient of friction between the train wheels and the track. Obviously motor torque falls toward zero as synchronous speed is approached. So if a motor spins the train wheels, speed increases only slightly, with rapid reduction in torque until the wheels again adhere to the track.

Antiskid. Also, an induction motor connected to an ac power line and driven mechanically several percent above its synchronous speed operates as a generator. If a train starts to skid during regenerative braking, the generator it is driving falls toward synchronous speed, and the greatly reduced torque reduces the braking force, ending the skid.

The higher coefficient of friction during both powering and braking make it possible to design a train with fewer powered coaches, cutting both its cost and weight and further reducing its gross energy input and expenditure.

This fall Osaka will decide on construction plans for one or more mini-subways. **-Charles Cohen**

Good news ... micropackaging to match microelectronics!

Looking for big space savings? Stop right here! These SO (Small Outline) ICs are shown actual size and yes, even that 40-pin device is less than stamp-size.

The new packages also come in 8-, 14-, 16-, 20-, 24- and 28-pin configurations and encapsulate most popular technologies... CMOS, LOCMOS, NMOS, bipolar analog and LP Schottky-TTL.

Their smaller-than-ever dimensions allow PC board sizes to be reduced dramatically, giving big savings in size and weight and a new competitive edge to your product. For applications where space is at a premium, SO-packaged devices can open up entirely new possibilities by allowing sophisticated electronics to be introduced for the first time.

They use the same chips as conventional DILs and power ratings apart, perform in exactly the same way, including reliability. SO packages can therefore go into existing designs easily and quickly. And of course they're ideal for your future designs employing automatic chip mounting techniques.

This topical, new type of packaging was pioneered by Philips* and our SO ICs have been used extensively in watches, clocks and hybrid ICs. We therefore have unmatched experience in micropackaging and as a result can supply the widest range of analog and digital circuits. In fact, you need look no further than the box alongside to see clear proof of Philips' world leadership in this newest and smallest area of miniaturisation.

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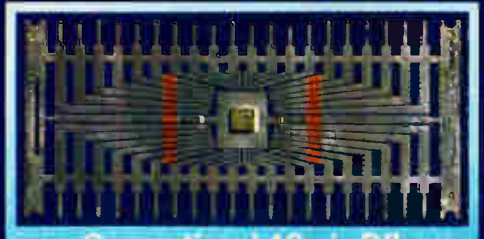
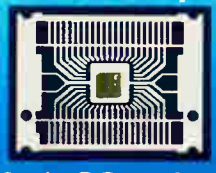


Conventional 40-pin DIL



40-pin SO package

Both devices are shown actual size. Despite its fine leads, this SO package can be mounted using all soldering methods, including wave and reflow. SO packages reduce PC board real estate, and also give additional design freedom since tracks can be run under the devices.

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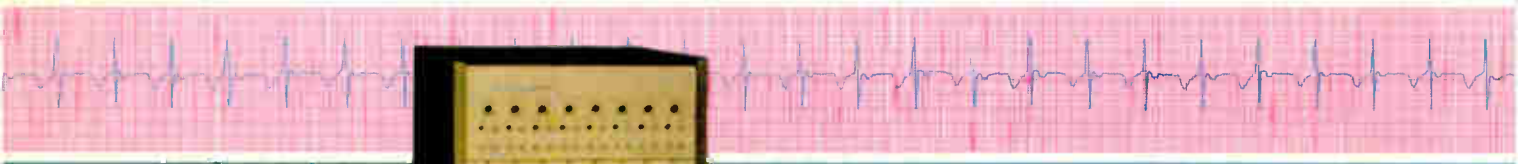

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Siemens communications test equipment

Data-communications analyzer has 20-min continuous tape loop

by Charles Cohen, Tokyo bureau manager

Software-controlled analyzer's tape drive gives operator time to react to unexpected trouble and halt recording

The MSO8A data-communications analyzer for systems using High-level Data-Link Control, bisync, and asynchronous protocols and operating at 50 to 9,600 b/s features an endless quad-density data cartridge that stores 20 minutes of data under full-duplex operation at the 9,600 b/s rate. Even though it represents about one third the cost of the $6,500 instrument, the cartridge drive was included because users requested facilities for storage of data for at least 10 to 15 minutes of operation.

Although the analyzer is designed to trigger on two character strings of eight characters each, system malfunctions other than those expected can occur. Thus it is necessary to store data for a reasonable period to give operators time to become aware of the trouble and press the break key to stop the instrument before the recorded data is overwritten with new data. The analyzer includes time in hours, minutes, and seconds in the header of each 7-K-byte block of data on the tape to facilitate the search for the data being transmitted at the time of system trouble.

Data is displayed on a 7.5-in. cathode-ray tube as 20 rows of 40 characters each. In full-duplex operation, transmitted and received data are displayed on alternate rows with received data underlined. In half-duplex operation, transmitted and underlined received data are displayed in sequence on the same lines.

Six different display codes are built into the analyzer: ASCII, EBCDIC, Baudot, hexadecimal, JIS7, and JIS8. (The Japanese Industrial Standard JIS7 code is similar to ASCII but includes a shift for characters of the Japanese katakana syllabary and is popular because it allows the use of the eighth bit for parity. The JIS8 code provides for the same characters without a shift but requires an external bit for parity.) Octal and binary displays are also implemented. Provision for shifting bits of display left or right makes it possible to shift a display that is garbled, because of the loss of one or more bits at an earlier time, until a reasonable message or control characters appear. This convenient feature is not commonly implemented.

Initial setup of the analyzer is facilitated by front-panel push-button selection of desired parameters from a menu offered on the CRT and two video printouts. Panel setup is stored near the start of the cartridge tape eliminating the need for battery-backed random-access memory for this function. Instrument test for initial checkout of the analyzer when first turned on is stored just before panel setup.

Menu setup. Trigger setting is done using a displayed menu that includes two eight-character strings, two timers, and two counters. Furthermore, the menu facilitates setting up a program directing the sequence of control to and from string-matching operations, time delays, and counts. Parity checks and block-check characters for cyclic and longitudinal redundancy checks

can also actuate the trigger.

Both the IEEE-488 instrument interface and the RS-232-C serial interface are available as options. This makes it possible to install the analyzer at a user's premises and remotely control it to perform diagnosis from a control center to allow improved maintenance while reducing personnel and other costs. Software is available for a personal computer, offered by Anritsu, that both controls the analyzer and reproduces the analyzer display on the microcomputer display.

The analyzer is completely software-controlled. To achieve the required speed, the functions of the analyzer have been split among six separate microprocessors—five 4-MHz Z80s and one 8035. The Z80s were chosen for their high speed and ability to control dynamic RAM, which is used with three of the processors. The processors are coupled through common memory via 8-bit parallel buses.

Multiprocessing. The 8035 performs real-time clock control. One Z80 with 10-K bytes of read-only memory and 16-K bytes of RAM handles main control of the analyzer, including control of panel keys and display, and acts as the instrument's central processing unit, while a second with 3-K bytes of ROM and 16-K bytes of RAM handles data capture and simulation. These two processors, together with a third that controls the cartridge tape, perform functions that other manufacturers also control by microprocessor.

The last two microprocessors execute functions usually done by hardware. One Z80 with 1-K byte of ROM and 1-K byte of Hitachi static complementary-MOS RAM executes the data trigger program, including decisions, while the second with a similar configuration checks character string matches.

A 511-bit pseudorandom pattern generator is included for making measurements of the number of bit errors or block errors. A 1,500-character transmitting buffer memory is included for system simulation tests.

Anritsu Electric Co., 5-10-27 Minami Azabu, Minato-ku, Tokyo 106, Japan [441]

SIEMENS

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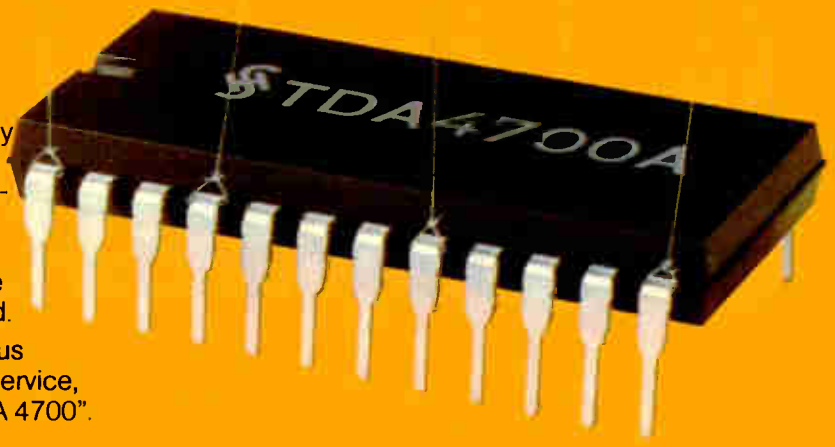

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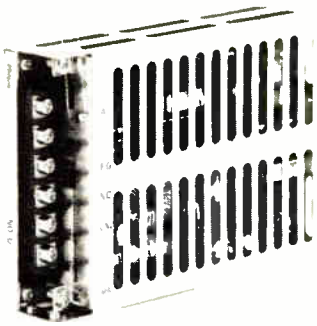
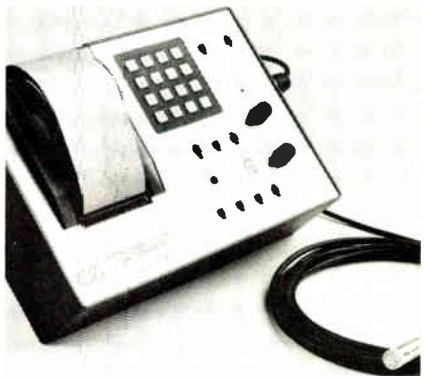
Circle 137 on reader service card

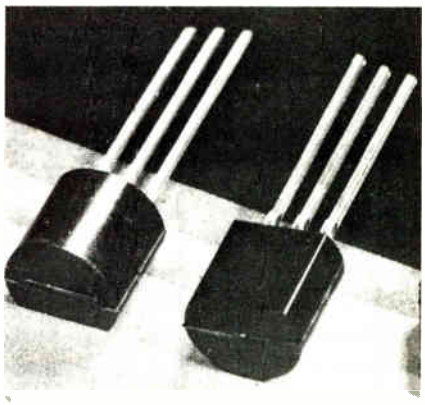
Electronics international



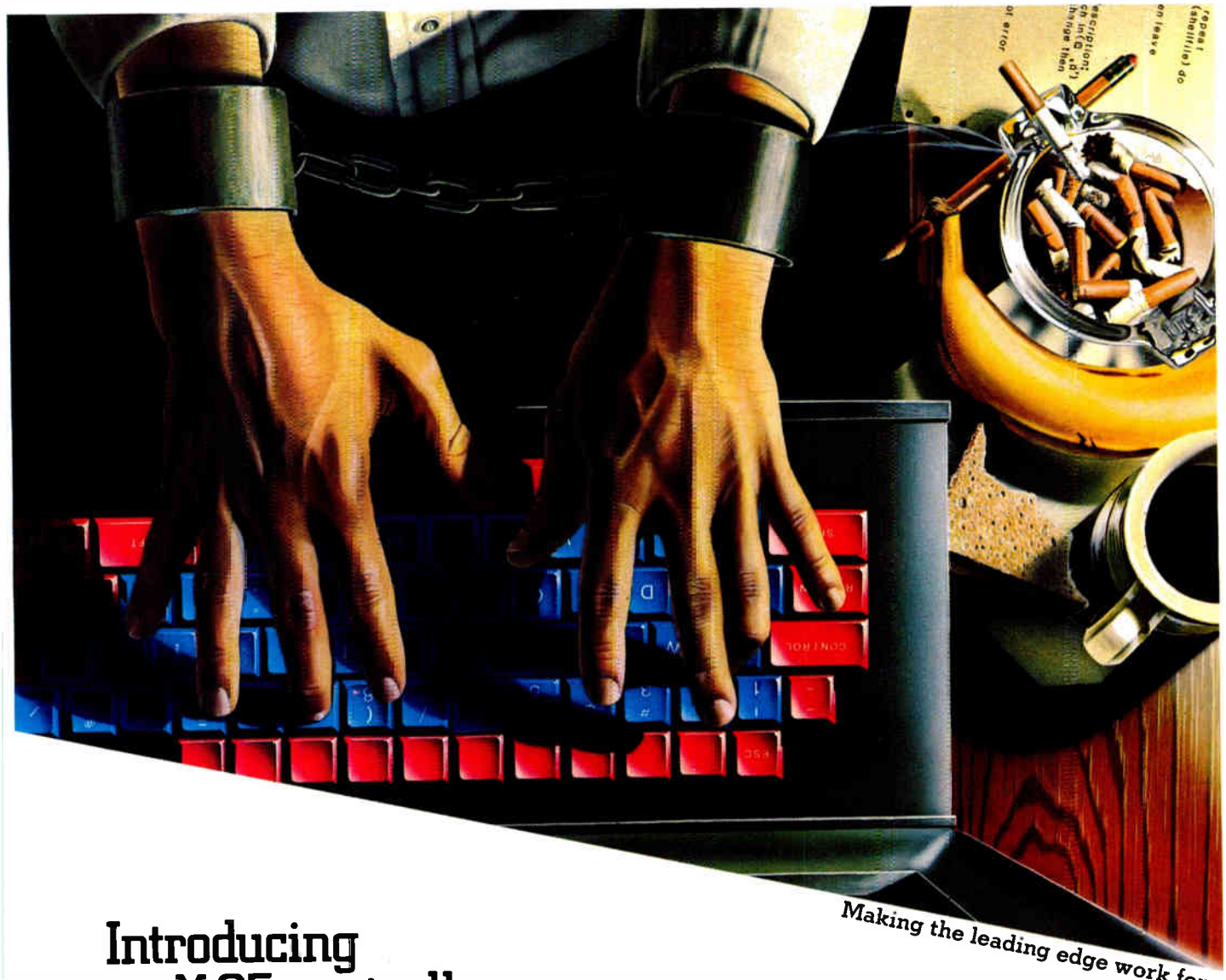
The VTM series of miniature switching power supplies deliver up to 15 W of power (1.04 W/in.^{3}) with outputs up to 24 V at 0.62 A. They have an efficiency of 70% and a wide input range of 90 to 132 V ac. Intertek Inc., Naito Bldg. 7-2-8 Nishishinjuku, Shinjuku-ku, Tokyo 160, Japan [445]



The CE- 160 graphic recorder digitally records waveforms of up to 10 kHz in real time onto aluminized recording paper using a built-in 1,800-word memory that automatically transforms data to hard copy. Computer Engineering Ltd., Wallace Way, Hitchin, Herts. SG4 OSE, England [446]



The U175M integrated circuit drives light-emitting diodes and glow lamps and causes them to blink at a frequency of 3 Hz. It has an output of about 30 mA and requires a supply voltage of 4.75 to 13.2 V. AEG-Telefunken, Theodor-Stern-Kai 1, D-6000 Frankfurt, West Germany [447]



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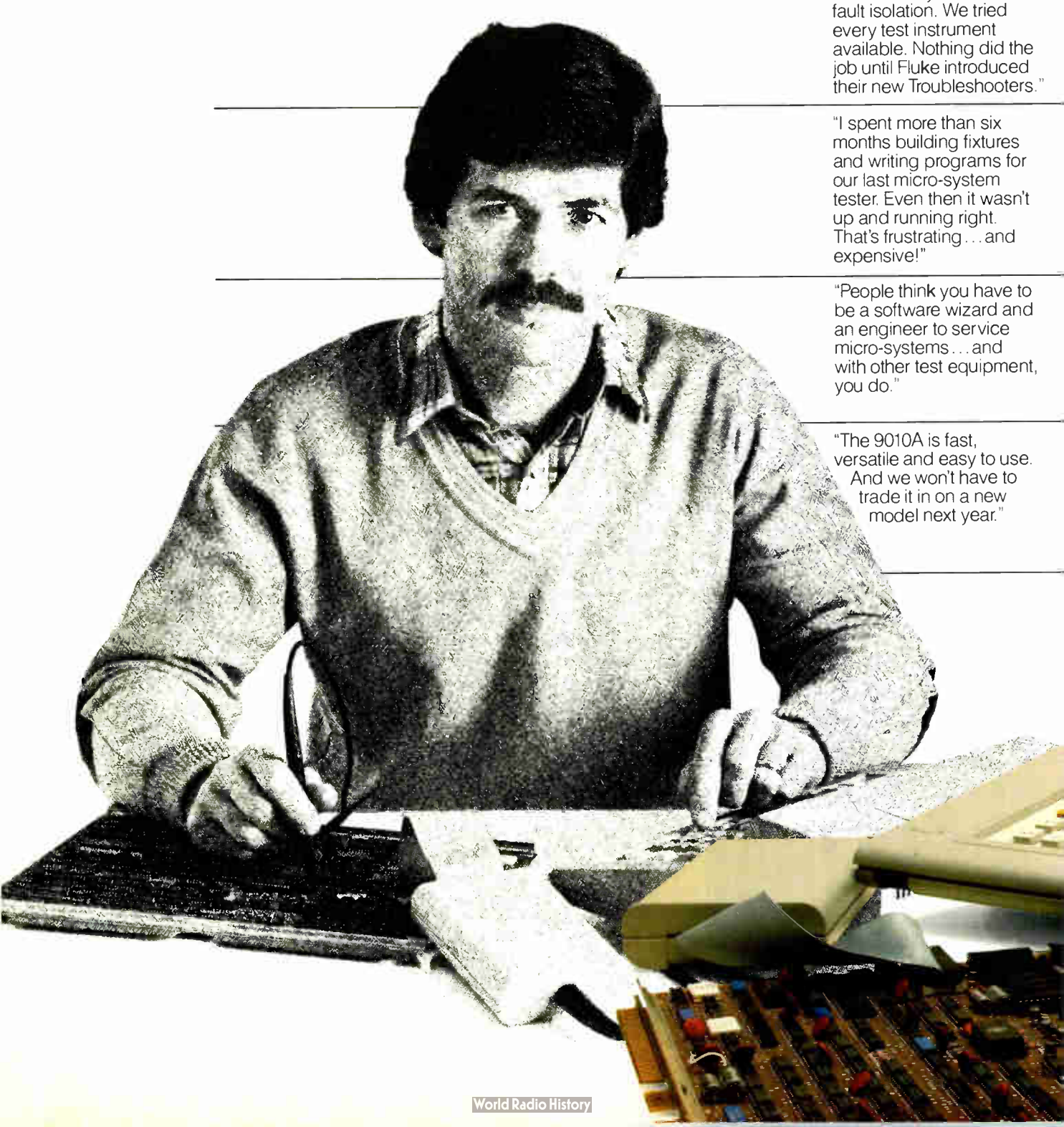

fies service

At Fluke, we spent over two years talking to frustrated manufacturing and field service people around the world about this critical problem, and designed the 9000 Series Micro-System Troubleshooters in direct response to their concerns. The 9010A, the first in the series, is available today.

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Fluke's solution is simple. The 9010A has the most practical interface you'll find: a self-contained pod for each microprocessor type. Just plug into the μP socket of a known good board, press the LEARN key and a revolutionary algorithm goes to work.

The 9010A automatically locates and identifies the RAM, ROM, and read/writable I/O on the bus of the unit under test and stores their characteristics in memory. No need for current software listings; this feature alone can literally save you months of front-end programming time. Operators without extensive training in digital logic can use the 9010A with confidence... and without delay.

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That's right. The 9010A is one of three Troubleshooters Fluke will introduce between now and January 1982. All of them will be fully compatible with 8-, 16-, and 32-bit μP's, All μP-dependent functions are located in the interface pods. Currently available pods include the **8080, 8085, Z80, 6502, 6800** and **9900.**

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The Fairchild 303S is built around a powerful new minicomputer with 256K bytes of MOS memory and resident operating software. Its advanced testing architecture is easily adaptable to virtually every test application, and allows even large PCBs to be quickly tested by executing complete programs entirely from memory. In addition, the new 303S offers a number of unique design enhancements that can dramatically cut PCB test time and significantly increase throughput.

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The new Fairchild Series 30/ Model 303S. More speed where it counts most.

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Automatic Wait Time™ (AWT) prevents improper fault diagnostics caused by the interaction between components on the same node. Through software control, AWT dynamically samples the measured value of the component under test and automatically waits until it has stabilized before comparing the value to the programmed limits.

HI-CURRENT capability allows the 303S to test boards containing mixed logic and bus-oriented circuit designs. When multiple devices on a bus must be disabled, HI-CURRENT capability is required, and no other test system offers it.

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The 303S isn't just built for speed, it's built for versatility. It comes with the largest number of uncompromised hybrid test points (927) in the industry, so it can be used to test either analog or digital points. By simply adding another low-cost terminal, our Foreground/Background programming feature enables programming to be done without tying up the system. And our datalogging feature gives you hard copy documentation of faults—by shift, day, week, or any other time increment—to accurately pinpoint manufacturing problems as they occur.

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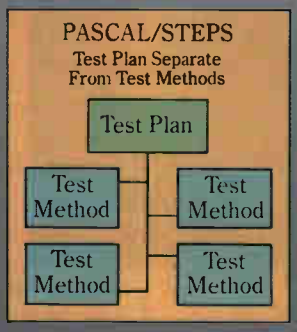

Unlike traditional job programming languages, PASCAL/STEPS separates the test plan from the tests (see diagram). There's no interweaving of tests, limits, binning strategy and test sequence. There's no confusion when new programs or change is demanded. There's only flexibility.

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TERADYNE

High-technology thieves peril nation

Industry must form first line of defense against theft and illegal export of strategic technologies, U. S. agencies say

by Larry Waller, Los Angeles bureau

Espionage, industrial theft, and illegal export of U. S. high-technology secrets are once more in the headlines. In the past few months alone, an alleged spy who passed along secret radar data was uncovered at Hughes Aircraft Co., convictions were obtained in the case involving a foreign ring that stole chips from three Silicon Valley firms, and officials of a small California firm were convicted and sentenced for shipping laser mirrors to the USSR.

Whether such activities are on the upswing is really not the point, warns assistant U. S. attorney Theodore W. Wu, who handles high-technology cases in Southern California. "Because such threats are always there, companies and officials must protect themselves," he adds.

Wu has been speaking out strongly in recent weeks because of what he sees as a danger to national security by agents who are zeroing in on the acquisition state-of-the-art technology developments that give the U. S. a military and industrial edge over foreign competitors.

Wu's main concern is stopping the export of industrial equipment and data that are on the prohibited list of commodities and covered by the Munitions Act. Although existing regulations list these commodities in detail, Federal agencies charged with enforcing the law generally lack the necessary funds and manpower to do a comprehensive job, he says. "Therefore, citizens and industry itself are the first line of defense. It's an honor system that must work to make the export system work."

Companies must take the initiative in protecting themselves against violating Federal laws controlling strategic exports. Not knowing the buyer is no excuse, so "somebody in a company better take it on himself to ask a few questions," says Wu.

Typical of the kind of commercial equipment covered by export control are big computers, communication and navigation gear, integrated-circuit production equipment, and advanced components. "Companies know their own business and customers better than anybody outside, and they have no excuse to be unaware of regulations," he adds.

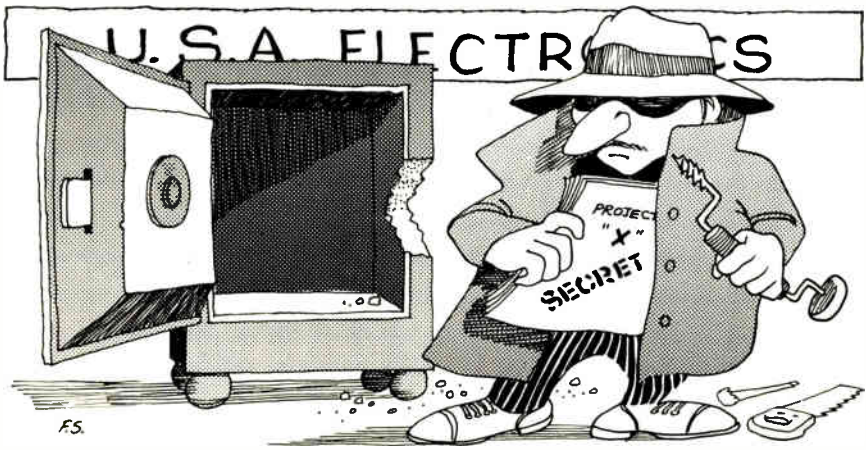
Indicator. A dead giveaway that something might be up is an order that comes from an unfamiliar customer for a large system normally used only by big companies or government agencies. "This is often a tipoff that the nominal customer plans to resell it to a foreign power, so find out the end user," advises Wu.

Any company official tempted to "close one eye to make a sale" would do well to consider that he and his company could be held criminally liable. Wu has prosecuted a number of such cases and gained convictions. His most recent trial success involved Spawr Optical Research Inc., a laser-component manufacturer in Corona, Calif. For knowingly selling precision mirrors required for high-powered lasers to the Soviet Union, two company officials received prison sentences and large fines.

Furthermore, a company such as Spawr that violates export laws "compromises itself with other customers so that its survival may be threatened." For example, Spawr's Government business was taken away.

Outright theft of secrets and small items such as ICs presents another problem that can be dealt with by better company security. While Wu does not directly state that U. S. internal plant security has become too lax, he maintains "companies should reassess it at once and modify as necessary to make it effective."

While it is tough to generalize about plant-security efficiency on an industry basis, and most sources do not attempt to, several common observations emerge. (Because of the subject's touchy nature, directors of



Probing the news

security at electronics and aerospace firms will discuss this topic only if they are not identified. Most of these officials generally share a Federal Bureau of Investigation background and keep in close touch.)

These sources agree that the threat of espionage is greatest at the highest technology levels, such as leading-edge microcircuits that have both commercial and military value. However, some managers and scientists, especially those who entered the industry after the late 1960s, do not take possible espionage as seriously as older hands who worked on classified or secret programs. This lack of seriousness is an attitude ingrained deeply at some Silicon Valley semiconductor firms, where information is exchanged freely outside official channels, and fast-moving technology advances often take precedence over security provisions.

In the opinion of many security officials, companies must start to forcefully bring home to younger engineers the need to keep important data from leaking out. "When his boss sits him down and explains what means in dollars and cents to his career, he starts to understand," says a veteran security director.

Also, many top managers and engineers do not realize the extent of surveillance that routinely occurs when they are involved in a secret program. Anyone with access to data about these programs can expect to be monitored, particularly when traveling. Many engineers with years of experience are still not aware they are watched during an overseas trip. Government agencies have learned that information is often passed outside the U. S.

The most recent example of this pattern is the Hughes Aircraft case, where William H. Bell is accused of having made several trips to Europe beginning in 1979 to deliver rolls of film to Polish intelligence agents. This case illustrates another vulnerability: those who handle classified material getting into financial trouble and thus becoming prey to foreign agents. Bell has admitted selling secret documents for large cash payments and the promise of more.

Although chances are slim of stopping the rare bad apple from compromising an important program, sources agree, aggressive security can shut off many problems in advance before they become critical. It is up to managers to know their employees well and be aware of those who have problems that might cause security risks, security men insist. Top-secret projects in the past (the U-2 spy plane of the 1950s, for one) have been protected in this manner, with much success. Although informers are not an appealing source of information, a few well-placed ones are a big help to security officers.

Probably the best security tool is the knowledge that most spies get caught. "Knowing they can't get away with it for long will stop those who are motivated only by money," notes one security officer.

Companies who do not live up to security-clearance regulations are making a big mistake, say security officials. "They work, if people take them seriously and abide by them," says John C. Hagerman, corporate director of security of Litton Industries Inc. ☐

Keeping police informed

"Since April of 1980 we have taken steps to better the security of our products," acknowledges the director of corporate security at Intel Corp. in Santa Clara, Calif. Besides beefed-up internal measures, says John O'Laughlin, a much higher level of cooperation now exists with law-enforcement agencies, particularly the Sheriff's office in Santa Clara County. "We need their help in investigations with search warrants and the like," he adds.

Intel and other Silicon Valley firms work hard in liaison with law agencies and have a security manager's group that meets monthly for this purpose. One aspect of the meeting is to help officers and prosecutors understand terms and technology better. "There's a jargon and mystique about the industry that often frightens them off," says O'Laughlin.

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BUILDING BETTER COMMUNICATIONS

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Time is ripe for entrepreneurs

Venture capitalists are on the lookout for high-technology start-ups, as cut in capital gains tax helps increase available cash

by Martin Marshall, San Francisco regional bureau

Last month, a small group of ranking technical managers walked out of National Semiconductor Corp. to form what may become the next major semiconductor company in California's Silicon Valley. Their next step was a round of meetings with the venture capitalists of the electronics industry, the people who can turn an entrepreneur's dream into corporate reality.

As with so many other fledgling entrepreneurs, their dealings with the venture capitalists who can supply cash, counsel, and coddling are crucial. The annals of the electronics industries are studded with stunning successes that were started with venture capital.

Nor is the group of former National technologists the only one making the rounds of the money men. Silicon Valley and other parts of the country like Massachusetts's Route 128 have seen a flurry of start-ups in the last year or so, and many more firms will follow.

The money is there, but the competition for it is likely to be intense. To get an edge, the prospective entrepreneur needs to know what venture capitalists expect of him.

Burning ambition. Hidden in the heart of every talented and ambitious technologist is the desire to run his own show. As his career progresses, he may become a product line manager, an engineering manager, an operations manager, or even the general manager of a division.

For a particularly ambitious few, however, running part of somebody else's show is not enough, and realizing the desire means becoming an entrepreneur. It means coming up with a big idea, gathering a team, seeking out sources of funding, and leaving the security of a salaried position at an established company to make a multiyear commitment to the unknown. For each of the heralded successes, such as Robert Noyce of Intel Corp., Jerry Sanders of Advanced Micro Devices Inc., Kenneth Oshman of Rolm Corp., Mike Markkula of Apple Computer Inc., or Jesse Aweida of Storage Technology Corp., there have been hundreds of obscure failures.

For those who are willing to take the plunge, there has never been a better time. "The 1980s will be the decade of the entrepreneur," asserts Stanley Pratt, editor of the Venture Capital Journal. "In 1979 and 1980, venture capitalists disbursed an estimated $1 billion each year—more than double the average annual disbursements of the prior five years." What's more, he figures that there is another $1 billion or so available in the pool of capital committed for investments in ventures, which amounts to $4.8 billion at present.

FLOW OF NEW MONEY INTO VENTURE CAPITAL
(In $ millions)

Year	Into venture firms	Directly into businesses
1969	171	450
1970	97	350
1971	95	410
1972	62	425
1973	56	450
1974	57	350
1975	10	250
1976	50	300
1977	39	400
1978	570	550
1979	319	1,000
1980	900	1,000

SOURCE: VENTURE CAPITAL JOURNAL

Although no one really knows how much of the money goes into electronics, Pratt notes that over 60% of venture activity is related to high technology. "Some of that is applied genetics, but most of it is computers and communications," he adds.

Geographically, the focus is in the San Francisco Bay Area. Western investors have their own explanation of the California start-up phenomenon. "The infrastructure exists on the West Coast, but I think it is more the risk-oriented mentality of the Westerner," declares Don Valentine, a managing general partner of the Sequoia Capital Fund and Capital Management Services Inc. of Menlo Park, Calif.

Brimming pool. The current pool of venture capital started to fill fast early in 1978, when the U. S. Congress passed the Steiger amendment to the tax code, which slashed the capital gains tax from 49% to 28%. The American Electronics Association lobbied heavily for its passage, as did the National Venture Capital Association under the direction of Reid Dennis. To document its case, the AEA surveyed 325 electronics companies to determine the effect of venture capital upon the electronics industries.

As reported to Congress by Edwin Zschau, chairman of System Industries Inc. and head of the AEA's capital formation task force: "We found that in one year alone—1976—each $100 of equity invested produced $70 in exports, $33 spent on R&D, $15 in Federal corporate taxes, $5 in state and local taxes, and $15 in personal income-tax revenues."

The brimming pool of venture

capital, of course, brought on a flood of entrepreneurs. "Compared with four or five years ago, there are more electronics entrepreneurs now, by an order of magnitude," observes W. Denman "Denny" Van Ness, vice president and partner in the venture capital fund of Hambrecht & Quist of San Francisco.

"The percentage of entrepreneurs funded, however, has remained about the same, or, if anything, it has increased," he says. "The reason is that more seasoned people are leaving their companies to become entrepreneurs." Historically, venture capitalists have funded only 1% to 2% of the proposals put to them. Once funded, however, an entrepreneur has a better than even chance to achieve some sort of success.

Making contact. With so many would-be entrepreneurs lined up around the edge of the investment pool, knowing how to approach an organization and understanding the way it sizes up candidates can provide a telling advantage for the applicant.

Notes George Quist, general partner of Hambrecht & Quist: "A critical factor for a guy getting started is sponsorship. If I get a cold call, the entrepreneur is not likely to get a strong reception. If that call is preceded by a call from someone I know who can tell me about him, then it helps considerably. If the entrepreneur has a track record in the industry, then he should know someone who can make that kind of connection."

John T. Neises, director of the National Venture Capital Association and general partner in the Charles River Partnership III in Boston, agrees that "an introduction from a known and successful businessman-entrepreneur is best. If you walk in with an introduction from Ken Olson [president of Digital Equipment Corp.], we will make time to listen to your proposal. The same is true of a recommendation from another respected venture capital house. Generally, the referral approach is the best approach.

"If you lack contacts, you have to engage in some G-2 work, selecting the venture houses most likely to be interested in and helpful to you. The venture capital guides in most business libraries are an aid. You need to know what kind of deal a firm is interested in, whether the firm is a lead or second-round house, and the size of the deal in which it can participate. You also need to know whether it has a conflicting venture in its portfolio."

Go West. Don Valentine, a California venture capitalist, believes most of the action is on the West Coast because, for one thing, people there have a risk-oriented mentality.

Other money men are rather more casual. "We are available and far more approachable," observes Sequoia Capital Fund's Don Valentine. "We don't have fancy screening methods, because it is very rare that a team comes in that is overwhelmingly right."

"Direct contact with the venture capitalist, preferably by the entrepreneurial president, is best," says Burton J. McMurtry, a partner in Technology Venture Investors and Institutional Venture Associates, Menlo Park. A telephone call can get a preliminary reaction and suggestions, while a crisp summary letter can also be used—with a longer response time.

Above all, would-be entrepreneurs should never broadcast their deals to a long list of financiers. Venture capitalists declare this approach means certain death for a proposal. They recommend that applicants limit their approach to about three firms. The turnaround time on such proposals is currently about a month to six weeks, as against three to six months earlier this year, they note.

People, not things. In the view of Thomas J. Davis Jr. (below), in new ventures "people are everything. People make products, products don't make people."

Premium on talent. Both people and a product idea are crucial to a start-up. "The principle of venture capital can be stated in four words: back the right people," asserts Thomas J. Davis Jr., who is a partner in the Mayfield Fund of Menlo Park. "People are everything. People make products, products don't make people."

Many of Davis's peers agree. "A new company seeks the level of its people, not its product," remarks Paul Wythes, general partner of Sutter Hill Investments in Palo Alto, Calif., a company that has helped some 80 electronics companies start up in its 19 years.

As John W. Poduska puts it, "Grade A people can take a Grade B idea and make a success of it. Conversely, Grade B people will run a Grade A idea into the ground." Poduska qualifies as a two-time winner in the venture capital stakes: he is the president of Apollo Computer Inc., a start-up in Chelmsford, Mass., and was one of the founders of Prime Computer Inc. of

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Other investors, however, choose to focus upon a product idea first. "Under our charter, the first criterion is advanced technology," says T. F. "Ted" Walkowicz, who is a general partner in Advanced Technology Ventures in New York. "After that screening, then the key factor becomes people."

Every venture capitalist has his particular yardstick for sizing up people who want backing for a start-up. "An entrepreneur who approaches me should have some experience in running a profit-and-loss center," says Arthur Rock of Arthur Rock & Co. in San Francisco, one of the best known of the venture breed.

When technologists with profit-and-loss experience are not available, some money men adjust their requirements accordingly. "I want to see an entrepreneur who is bright and who has a strong ego, integrity, knowledge of products in his marketplace, an empathy for people, creative thinking, and a good numbers sense," says Jack Melchor of Melchor Venture Management and the Portola Venture Fund in Los Altos, Calif.

As Fred Adler, general partner of Adler & Co. in New York, puts it: "We prefer a guy who has been a business unit manager, but we can also look at an engineering manager. He might be a guy who has identified a $200 million or $500 million market, but who has been impeded in realizing it by the company in which he works."

Teamed up. A few individuals like Gene Amdahl or Seymour Cray could command venture capital alone when they launched successful computer companies. But most financiers prefer to see an entrepreneurial team, however incomplete. "We prefer to have a management team in place when we start to fund a company," explains Eugene Kleiner of Kleiner, Perkins, Caufield, & Byers in San Francisco.

One of the founders of what was then called Fairchild Semiconductor, Kleiner notes that such a leader need not necessarily have been a company president before. "The good people then attract the rest of the management team, and we will help the company to find one or two people," he observes.

"Ideally, the entrepreneurs will be a group of people who worked together at a large company," declares Kenneth W. Rind of the Oxford Group in Greenwich, Conn. "The top guy will have had division or product line profit-and-loss responsibility, and he will be joined by a marketing manager, an engineer, and a controller. The classic instance would be a group out of IBM, but we would still be wary unless one of them had profit-and-loss experience." The group that recently left National Semiconductor [*Electronics*, Aug. 11, p. 46] thus rates as a dream team.

Spotty teams must be avoided at all costs, says Russell E. Planitzer, a partner of J. H. Whitney & Co. in New York. "Often guys get together, issue the stock among themselves, and because of a 'hire your friends' phenomenon, have a number of weak people holding amounts of stock they can't support within the firm," he says. "This not only makes the idea

Qualities. Jack Melchor wants the entrepreneurs that he backs to have "a strong ego, integrity, knowledge of his market, an empathy for people, and a good numbers sense."

Ready and willing. "We prefer to have a management team in place when we start to fund a company," says San Francisco venture capitalist Eugene Kleiner.

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unattractive to the venture capitalist, but also can make it tough to put a good second tier of managers together. You need stock as a lever."

Another caution is that applicants should not try to gloss over their own weaknesses. "We funded one entrepreneur who had been fired from his previous job," recalls Adler & Co.'s Adler, "because we looked into the reasons for it and decided it had nothing to do with how he would perform in the new company."

Adds Frank Caufield of Kleiner, Perkins, Caufield, & Byers, "One of the screens we apply is to ask ourselves if the entrepreneur will tell us the bad news as well as the good immediately. We want to know, when things get tough, if this is the kind of guy that we can get down in the trenches and work with."

Portrait. Venture capitalists have personal preferences for traits among entrepreneurs, but a rough composite can be pieced together. "A guy who just wants to be a millionaire is not very interesting to me," observes Sequoia's Valentine. "I'm looking for the guy who wants to build a $500-million-a-year company with perhaps $50 million in personal net worth."

He notes that the ideal entrepreneur can be a "narrowly focused, driven, often boring individual. He might be the kind of guy that I would be reluctant to spend my weekend off with."

Jim Riley, cofounder of Dataquest Inc., former president of Signetics Corp., cofounder of Intersil Inc., and part-time venture capitalist, agrees with Valentine. "The lead entrepreneur must have tunnel vision," he says. "He is willing to subordinate everything else to his venture, even including commitments in his personal life."

The key is how the individual operates under stress, avers John Woodman, vice president for research at the San Francisco office of Dean Witter Reynolds Inc. In preparation for his firm's entry into the venture field this summer as a general partner of U. S. Venture Partners, Palo Alto, he compiled a psychological profile of the entrepreneur.

"They are all rational-emotive, a normal state, when they come in through the door," he says. They "tend to move toward aggressive-directive behavior, and it is the function of the venture capitalist to help them redirect that energy in a fashion that nurtures the company."

Although most venture capitalists like an entrepreneur to have confidence bordering on arrogance, Mayfield Fund's Davis notes that such an attitude should not apply to the technologist's concept of marketing. The entrepreneur should not believe for a second in the old advice that if he builds a better mousetrap, the world is bound to beat a pathway to his door, he argues.

"He knows that everything has to be sold, and he does not react to every slump in sales by running back to the lab to try to invent something that will sell itself," he says. Davis wants the type of entrepreneur "who gets right up, belly button to belly button, with his customers, both to find out what they need and want and because he loves the action of making sales himself."

Double scrutiny. While the entrepreneur may come in for the heavier scrutiny, most venture capitalists caution that the selection process is two-way. "The entrepreneur should do his homework on the venture capitalist, because the corporate marriage lasts a long time," cautions Sutter Hill's Wythes. "He will want the venture capitalist to be there for the second and third round of financing, and he will need the venture capitalist's help to raise financing beyond that."

It is essential that the entrepreneur check to see how the financier has dealt with previous entrepreneurs. Fred Adler advises technologists to find out what successful companies potential backers have funded and then ask the company presidents what the investors did for them and what kind of board members they turned out to be.

The entrepreneur can be sure that, before funding, the venture capitalist will conduct an extensive checking process. "The reference check of the entrepreneur is the most important part," asserts James Bochnowski, a partner in Technology Venture Investors and a former president of Shugart Associates. "We talk to all the people that the entrepreneurs have dealt with in the past. Then, in the interview process, we try to be candid with them. We tell them where our discomfort lies, whether we would rather they had a different chief executive officer, and any

Small investors supply seed money

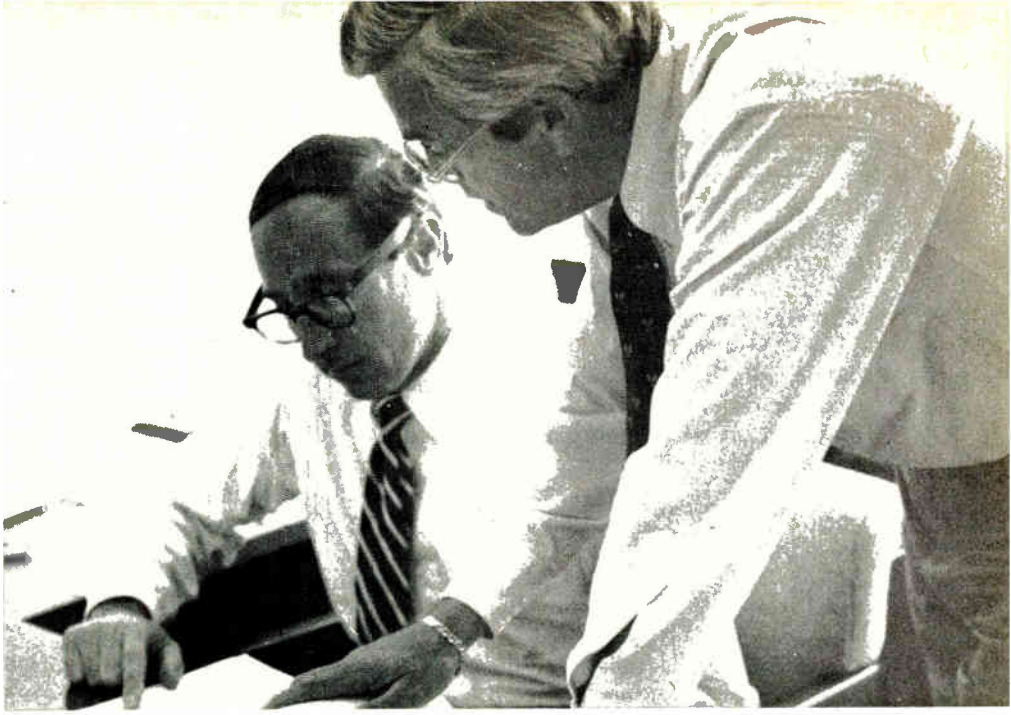
Rather than just an idea for a product and a plan for getting it to market, some entrepreneurs prefer to have a working prototype in hand before negotiating for a significant amount of venture capital money. A prototype can be more convincing to a venture capitalist, and so the entrepreneurs can retain more equity for themselves.

When seed money, as distinct from venture money, is needed, another class of capitalists comes into play. Venture organizations usually prefer to invest at least $250,000 and sometimes a minimum of $500,000, compared to the $10,000 to $100,000 that could be described as seed money. The reason for the minimum is that each principal venture investor can actively participate in only six to eight companies at a time. Since the fund is usually investing other people's money and only retains a small percentage, the minimum figure is calculated as the one that will make the venture capitalist's time spent worthwhile.

"Deals are getting bigger, and there is a propensity for venture capitalists to go for the big deals," observes Dataquest's James Riley, a part-time investor. "It's hard for them nowadays to do deals under $500,000. This has created a market for individuals to do smaller deals using their own money." Riley is one such seed sower and points out that "working with my own money, I can do deals with several zeroes less than the big funds."

Some venture capitalists are capable of investing both fund money and personal money, thus providing a natural follow-on to a seed investment. Among others, these include Jack Melchor, Pitch Johnson, Fred Adler, and Peter Wolken. **-M.M.**

Manager wanted. New Yorker Fred Adler wants "a guy who has been a business unit manager, but we can also look at an engineering manager" to head a start-up.



Top spot. Kenneth W. Rind of the Oxford Group in Connecticut, at left with partner Neil Ryan, says the top person in a start-up should have had division or product line responsibility.

weaknesses we see."

The astute venture capitalist also does not rely solely upon his own judgment. "We call the potential customers of a prospective company and ask them if they truly need such a product," notes Jack Melchor of the Melchor and Portola venture funds. "The two extremes that we have seen in that category are Triad Systems, which had clearly identified its customers, and Rolm, which had not immediately identified its customers. Both made it big" in the small-computer business.

A proper plan. A team's business plan comes in for hard scrutiny as well. The plan's initial degree of formality varies, but the applicant must convince the investor that he has put some serious thought into it.

"Sometimes the business plan is just a phone call and sometimes it is a rough plan," says Melchor. "I don't like a lengthy business plan; about 15 to 20 pages should be enough . . . especially, I hate to see a guy with a business plan that's been written by a consultant. If he doesn't know it himself, he can't be committed to it."

"The writing of a business plan is essential," adds Technology Venture's Bochnowski. "It should include the background of the key people, a description of the market the entrepreneurs wish to enter, their product development strategy, their manufacturing and service strategy, their projected balance sheets for three to five years, their proposed sources of capital, and the risks and potential problems they see."

There is a clear progression in writing of a business plan, observes Franklin "Pitch" Johnson, owner of Asset Management Co., Palo Alto. "It begins with a hypothesis, or 'genius leap,' but what separates it out is the entrepreneur's ability to think in concrete terms," he cautions.

"The whole reason to write a business plan is not to raise money; it is an exercise to see if the idea holds water and to get it squared away in the entrepreneur's head. If the business plan is written strictly as a selling tool to the venture capitalist, then it is unlikely he will fund it."

Apollo Computer's Poduska has this advice: "A business plan should run 10 pages plus a summary page, and it should address these issues in this order: the nature of the business; a description of the market with projections of growth and share of market; description of the product or service; and capital requirements."

Ezra Mintz, president of Minerva Ventures Inc. and of Colorgraphic Communications Corp., both in Atlanta, says that "most venture capital houses will tell you that they want a business plan, market projections, team description, competitive analysis, and so on. But most important may be a quantitative analysis of the competitive situation."

As for the rosy projections that sometimes color business plans, venture capitalists examine them carefully. "When I check out a business plan, I go backwards from the numbers to what it means in terms of the company and the marketplace," observes Johnson.

"Tandem [Computers], for example, had some very specific ideas. Some venture capitalists were skeptical that something could accelerate that much, but we had confidence in the management team and they did just about what they said they would do." In the end, Johnson notes, "it boils down to how closely the business plan's sense of reality matches my own."

Evaluations of business plans range from a minute analysis of an entry into an existing field to a gut-level reaction to a new field. In backing the Apple Computer venture along with VenRock Associates, the venture capital arm of the Rockefeller family interests, Arthur Rock declares, "We just thought that personal computers were a good idea."

When his group looks at a business plan, says Fred Adler, "We don't make judgments like whether C-MOS is better than SOS. We ask ourselves: if the supposition is true, what are the commercial implications? We can't second-guess on the

bits and bytes."

Adds George Quist: "I don't want to hear simply that someone wants a 5% share of a $200 million market. I want to see him pinpoint his markets. If it's a chip design, for example, then I want him to tell me 'Intel said they would produce this amount and National will produce this amount.' Then we contact the potential customers. That's one of the good things about technology, it's measurable."

Negotiating the deal. Once the entrepreneurial team has sustained the interest of a venture capitalist, the crucial stage of negotiating a deal follows. The profit expectations and stock demands of the money men can come as a shock. "The technologist generally thinks in terms of percentage, while the venture capitalist is interested in multiples," notes Peter Wolken of Associated Venture Investors of Menlo Park.

"We want to see a company that will increase the value of our investment by tenfold to a thousandfold over a 5-to-10-year period," he says. "The tenfold figure is not an objective; it is a minimum. The entrepreneur must raise his sights from the growth level of his present company to much higher rates."

While cautioning that each deal is unique, H. Dubose Montgomery of Menlo Venture Corp., Menlo Park, offers this description of a typical slicing of the corporate pie in a start-up: "For two guys and an idea requiring an investment of $2 million to $4 million over the course of 18 months to two years, it would be appropriate to ask for about two thirds of the company."

Advanced Technology Venture's Walkowicz agrees, noting, "A new venture is like a three-legged stool. One third of it is the entrepreneurs, and the other two thirds are two financial groups that are genuinely independent. That way no one is in the position to push anybody else around."

Technology Venture Investor's Bochnowski gives some idea of variability in this hypothetical case by adding, "I can make a case for asking 60% to 70% for a $2 million investment. If it's a better team, then 50% might be appropriate."

To get the number, Bochnowski determines the market risk and the dollar risk and comes up with a reasonable economic risk. "Then I would project a price/earnings ratio, risk-adjust it, and feed it back to the present. I would also check the numbers on similar deals," he explains.

Apollo Computer president Poduska says, "At the end of the first milestone, whether it's the first million dollars, the first year, or whatever, the fully diluted split generally runs about 60:40 in favor of the venture capitalist, though occasionally it is 70:30. But it is not the figure that precedes the percent symbol that's important; it is the one after the dollar sign."

Entrepreneurs should make every effort to bring their proposed company into the negotiation session free of ties. "Previous agreements with finders are a ball and chain to negotiations—and you simply don't need them in Silicon Valley," states Eugene Kleiner of Kleiner, Perkins, Caufield, & Byers. "I would also recommend to an entrepreneur that he leave his previous employer in a clean fashion and not take anything with him."

While the venture capitalist needs enough percentage to make his investment worthwhile, he must leave enough to keep the entrepreneurs interested. "We like to see the founders having 25% to 50% of the company," declares Kleiner.

For the same reason, Ted Walkowicz asserts that "we try not to dilute the management founders below 20% to 25%, so that they will keep their motivation. We also do more option plans to keep from diluting the entrepreneurs." Observes Fred Adler, "We also reserve a pool of stock that is earmarked to attract new people to the company."

Who's in charge? A psychological factor that sometimes enters the negotiations is the entrepreneur's fear of losing control of his company to the venture capitalist. This, the investors claim, comes from the failure to distinguish operational control from the amount of stock needed for return on investment.

"If control is an issue, I'm not interested in the deal," flatly states Arthur Rock. Adler agrees, warning, "If I detect paranoia, I run from the deal. Theoretical control is nonsense, because if the technical people walk away from the company, the investor is left holding a bag of air."

Rather than worry about a venture capitalist's nominal control and participation in a company, most entrepreneurs welcome it. A surprising number of electronics financiers are former entrepreneurs, company presidents, and operating officers of electronics companies. They can tender advice, as well as money, and can help out in the financial areas

Check. Reference check of entrepreneur is most important, says James Bochnowski, center. His partners at Technology Venture Investors are David Marquardt, left, and Burt McMurtry.

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on a winner. As selective as the investors may be, they know that some of their ventures will not meet expectations. "You haven't been in venture capital until you've had to write off one or two," says Wythes.

Pitch Johnson sees four kinds of companies resulting from venture deals. "Typically about 10% of the companies will fail. Some 30% to 40% of the companies will do well, which means that they will have a 40% to 50% compound annual return," he says.

"Then, about 20% will do very well, significantly surpassing the 10-times multiple over five years." The other 30% to 40%, says Johnson, constitute the "living dead": companies that do not go broke, but also do not return much on their investment.

Whatever the performance of the company, the venture capitalist cannot realize a profit on his investment until the company becomes liquid. That means that it must either be acquired, merge with a publicly held company, or make a public offering of its shares. Only then can the venture capitalist reinvest his money in other start-ups.

Go do it. When that money is reinvested, some believe that it will not gain the same returns as earlier deals. "Between 1974 and 1981, venture capitalists had a stellar record of investments," Jim Bochnowski says. "In 1974, in particular, only the very best deals got funded. I believe that in the next six years the percentage of winners cannot help but go down."

Even so, most venture capitalists are highly optimistic about the rash of start-ups. "The best time to start a new company is tomorrow morning," Melchor says. "There has never been a better time."

Others see a change in the nature of start-ups, particularly in Silicon Valley. "All ventures will upgrade from high technology to very high technology because the return per employee will have to be significantly higher," believes Associated Venture Investor's Wolken.

He regards the thrust into venture capital an American ace-in-the-hole in world economics. "The Japanese have the unfair advantage of low-interest loans and the restriction of competition from abroad," he asserts. "Our unfair advantage is venture capital."

Tommy Davis sees the whole venture-entrepreneur combination as a product of the American tradition, observing that "the dynamics of our economy and our social structure are such that no matter how hard the large companies try to hold their employees, a rather steady stream of them will leave in order to form teams to start new enterprises."

As Eugene Kleiner puts it, "Don't be afraid. Do it." □

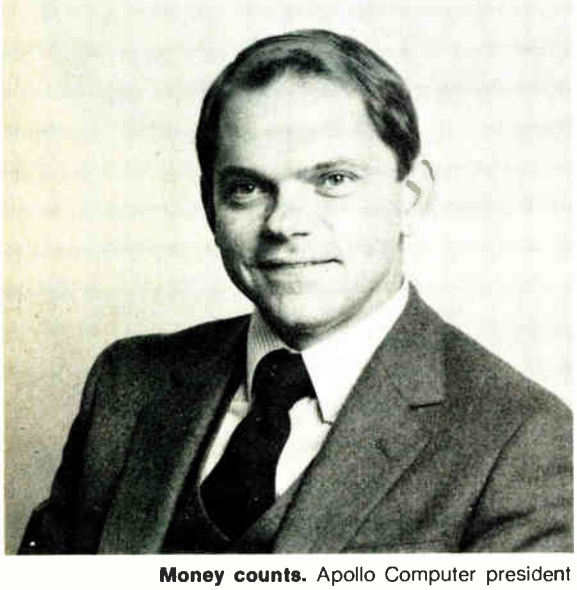
Reporting for this article was also provided by James B. Brinton and Linda Lowe in Boston and Ray Connolly in Washington, D. C.

For more information

"Guide to Venture Capital Sources," edited by Stanley Pratt, provides a complete list of venture capital sources as well as several practical articles on the subject. Contact Capital Publishing Corp., Wellesley Hills, Mass., (617) 235-5405.

Membership Directory, National Venture Capital Association, lists names, phone numbers, and addresses of members. Contact 1225 19th St. NW, Suite 750, Washington D. C. 20036; (202) 650-5756.

Membership Dirctory, Western Association of Venture Capitalists, in addition to names and addresses, gives areas preferred and avoided for investment, minimum and maximum investments desired, and types of financing and special help provided. Contact 3000 Sand Hill Rd., Bldg. 2, Suite 260, Menlo Park, Calif. 94025, (415) 854-1322.



Money counts. Apollo Computer president John W. Poduska advises entrepreneurs not to concern themselves with ownership percentages, but with the dollars.

Growth. Peter Wolken wants tenfold growth—not an objective, but a minimum—in 5 to 10 years. He is at left with Associated Venture Investors partner Jack Loustausnou.

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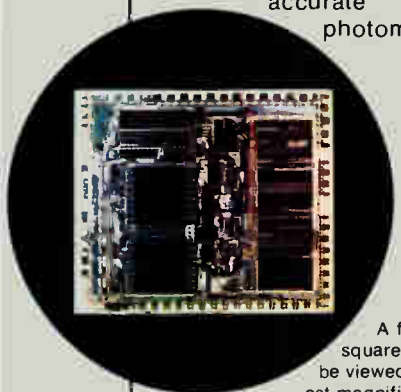

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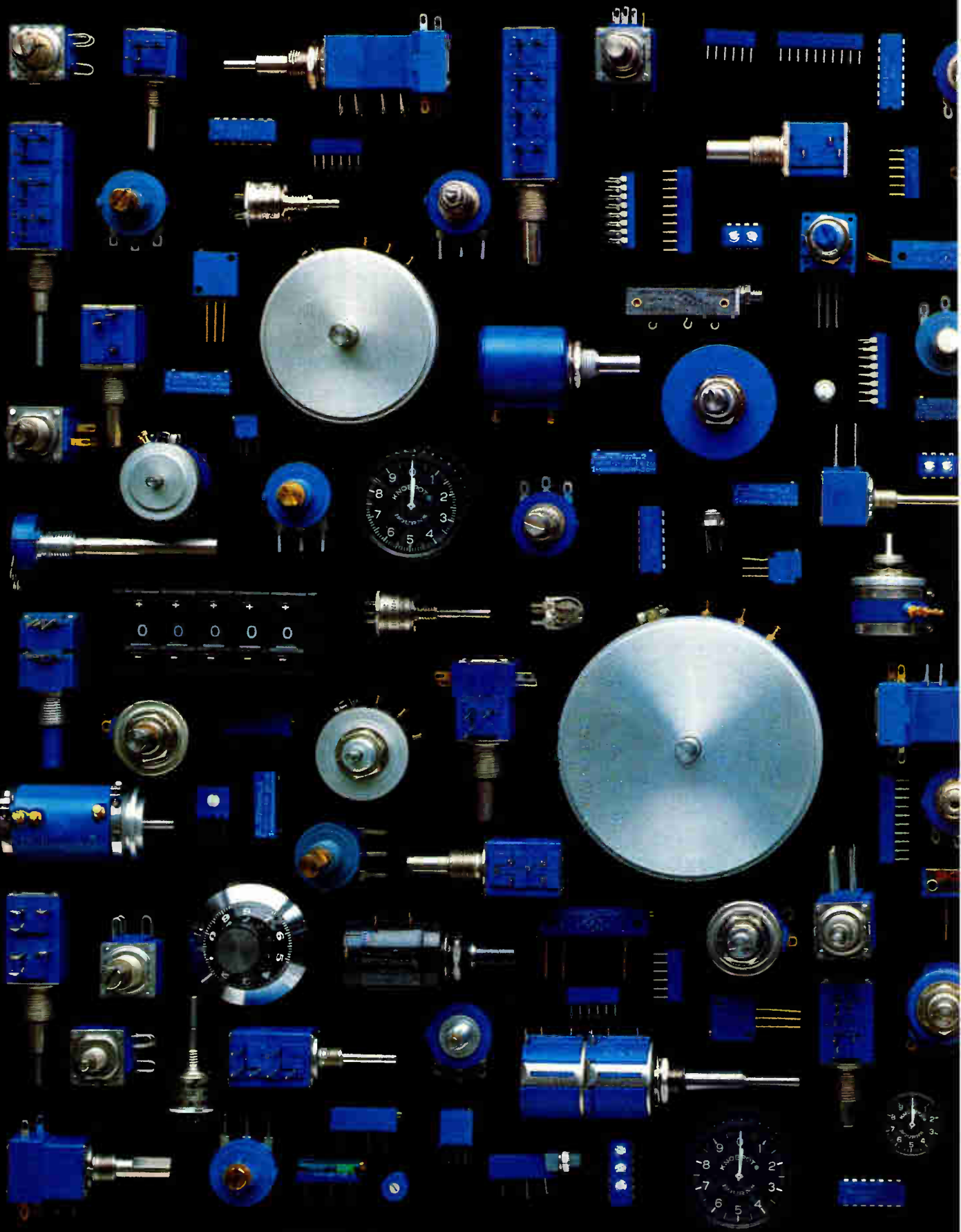

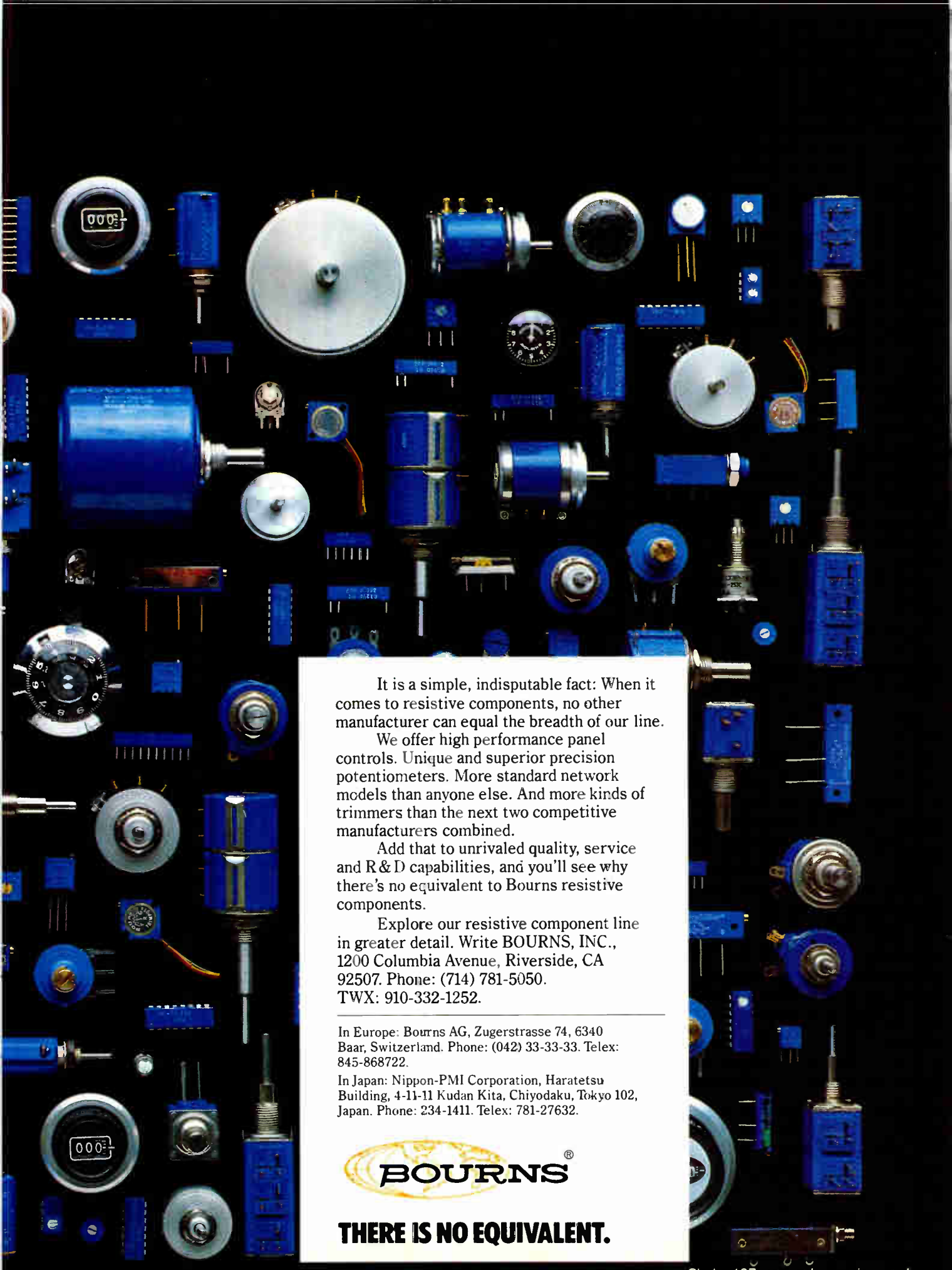

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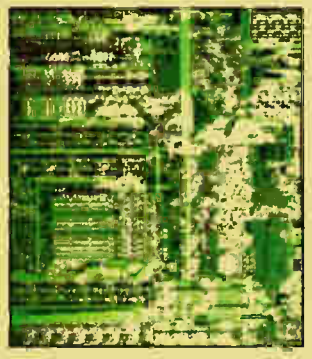

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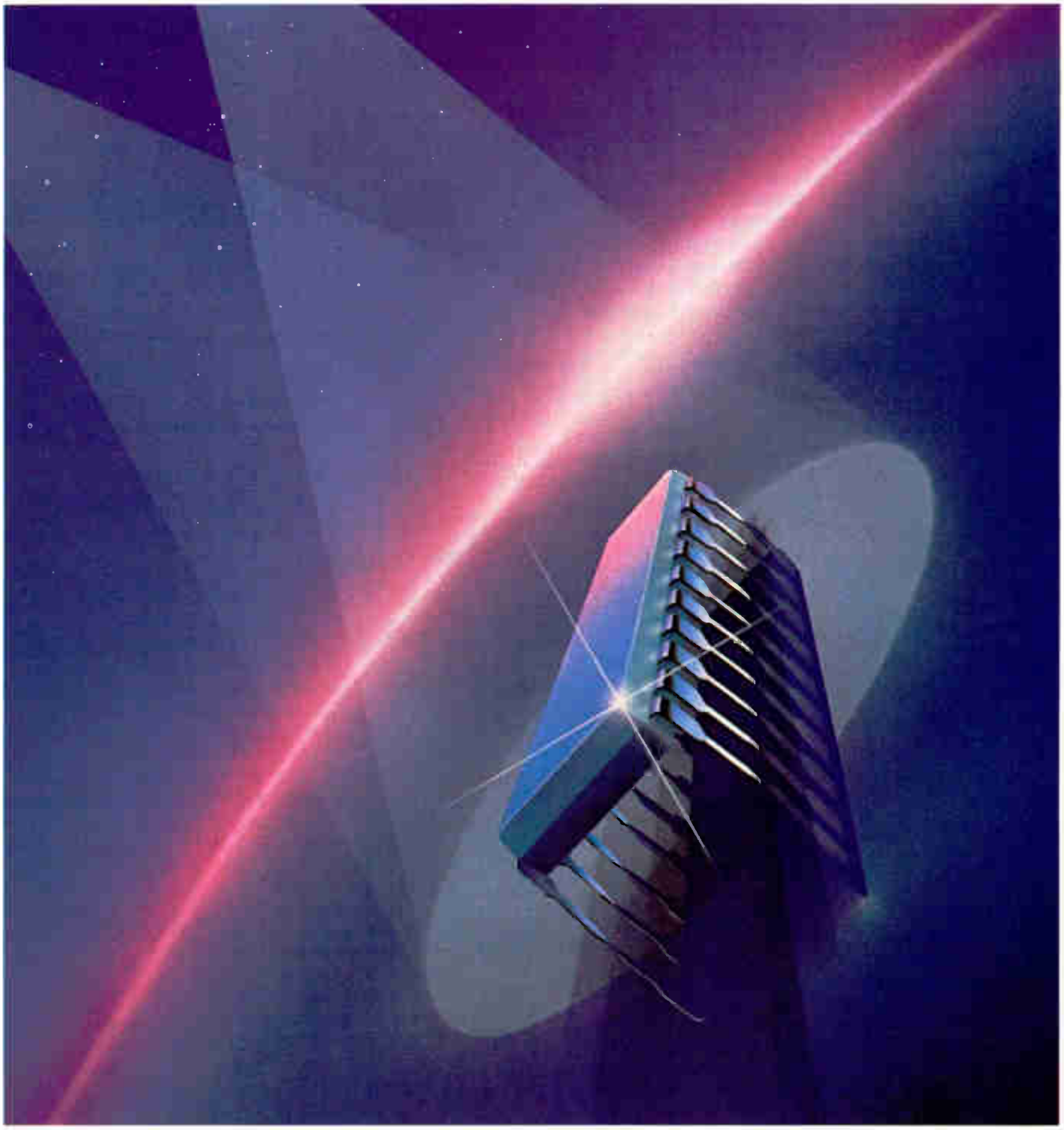

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Thick-film transformer advances hybrid isolation amplifier

Metal-ceramic sandwich forms low-cost flat-spiral coils that yield wideband coupling and high common-mode rejection

by Delip Bokil and William Morong,* *Analog Devices Inc., Norwood, Mass.*

☐ A transformer that uses thick-film technology for the task of producing a planar coil achieves tight windings and consequently a wideband response. The component's development was spurred by interest in a small, economical isolation amplifier for medical electronics and process control applications, but its potential uses extend far beyond these fields.

The transformer is the heart of the AD293/4, a hybrid flyback isolator design that offers superb electrical isolation, precise transfer characteristics, and low power consumption. Thick-film processing makes the new parts small, reliable, and inexpensive to produce and use.

Isolators have long suffered from the cost and inconvenience of bulky wirewound transformers. Even optical isolators usually need transformers for coupling power supplies across the barrier—only transformer coupling holds the promise of the transmission of both signals and power through a single isolation element.

Flyback is the choice

A single-transformer flyback isolator is the most reliable because it has only one critical insulation system, and it has proven adequate for low-accuracy amplifiers [*Electronics*, July 20, 1978, p. 105]. Such a part (Fig. 1) incorporates a power oscillator to produce an asymmetrical square wave that periodically energizes the transformer. When the oscillator switches off, the coil voltages reverse because the current cannot change discontinuously.

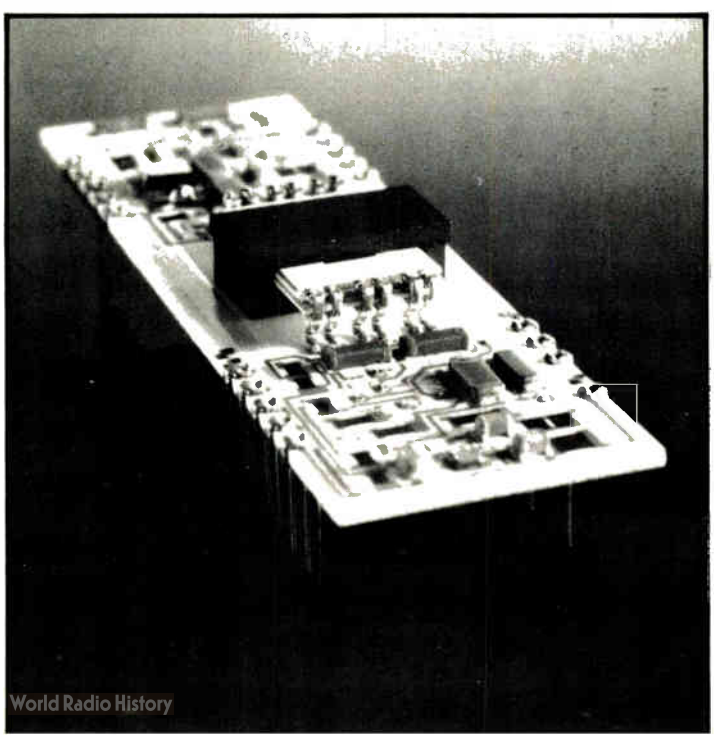
This flyback pulse is amplitude-modulated under control of input amplifier A_{in} and is demodulated by identical circuits in the input and output sections. The output of the first demodulator feeds back to A_{in}, which adjusts the modulator so that this signal—as well as the output of the second demodulator—follows the input voltage.

Past attempts to improve this technique have been beset with difficulties that are overcome by the flat-spiral coil in the AD293/4. Many of the earlier flyback isolators exhibit a bewildering variety of flaws, most of which trace back to the transformer (see "Flyback isolators pose problems," p. 114).

Conventional transformer and printed-circuit-board construction techniques have provided adequate modular and board-level isolation amplifiers in the past, but they could not meet the design goals for the AD293/4. Thick-film hybrid construction techniques promise fulfillment of the elusive goals of a small, hermetically sealed part that is economical to produce. Furthermore, recently perfected techniques for the deposition and trimming of thick-film resistors on dielectric substrates assure that dense hybrid amplifiers will have superior electrical performance.

The cost of these benefits is the challenge of fabricating the transformer as a thick-film component. Conventional transformers are large, mechanically nonuniform components, generally

Hybrid isolator. Thick-film fabrication techniques applied to the transformer coils can shrink the cost and size of isolation amplifiers. The ferrite core set is attached to the hybrid substrate and supports the thick-film windings.



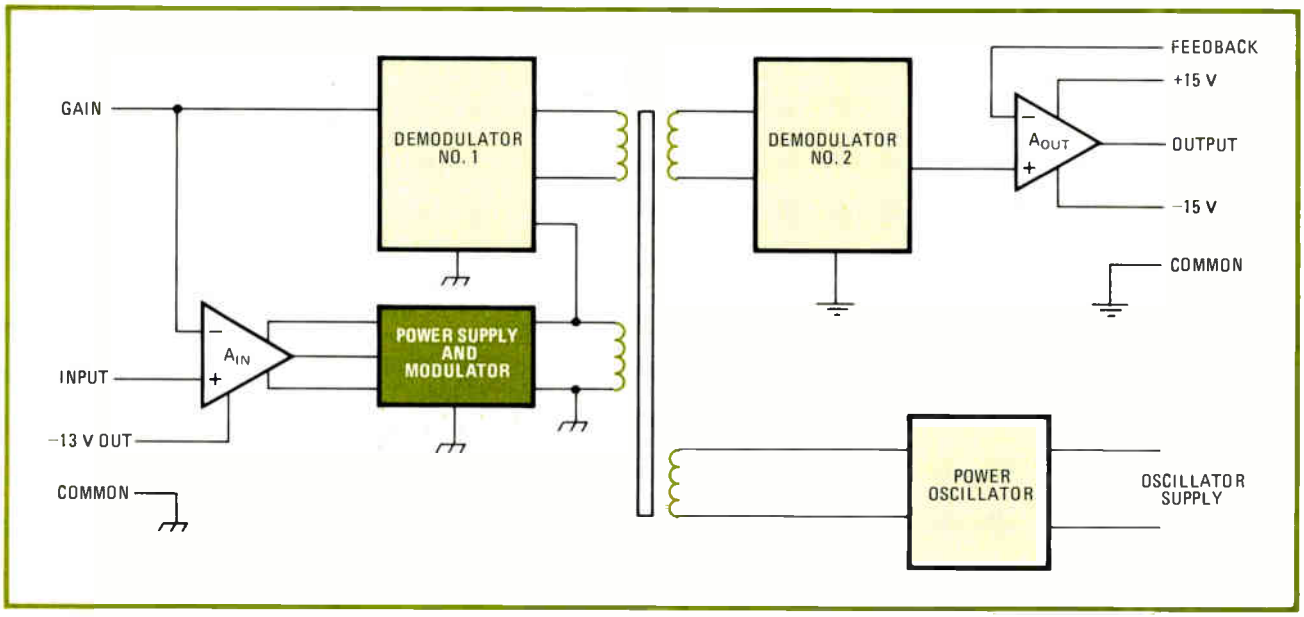
*Now with Intronics

handmade out of low-temperature materials and thus, on all counts, incompatible with thick-film fabrication techniques.

Isolator designers traditionally have sought small, economical transformers with superior coupling, high voltage insulation, and low interwinding capacitance. The designer of a hybrid isolator needs a device that, in addition, is easily secured by epoxy, has an ordered termination system compatible with standard thick-film techniques, and is completely testable before attachment to the hybrid substrate.

The transformer configuration (patent pending) shown in the opening photograph boasts several outstanding characteristics. The flat spiral windings can be mass-produced by thick-film deposition

1. Across the barrier. Flyback isolators use a single-transformer to transmit signals and power between the input and output. A power oscillator generates the flyback pulse that is modulated by input signals and demodulated in the output section.



Flyback isolators pose problems

A significant portion of the energy in a flyback pulse is at a much higher frequency than that of the isolator carrier. The ferrite core of the transformer is not the proper conduit for these signals, because the high-frequency properties of ferrites vary widely with temperature and applied and remanent magnetic fields, as well as from lot to lot. So, good transformer action at high frequencies must be obtained from the windings of the coils rather than from the core, which should be used merely to extend the low-frequency response.

Ideally, the primary and secondary windings of a transformer occupy the same space so that the flux lines of each one will envelop the other, giving excellent coupling over a wide bandwidth. In such a transformer, it is difficult to electrically insulate the primary from the secondary—the crucial step in constructing an isolation amplifier. There are at least four alternative winding methods that have been tried.

Multifilar windings couple well because the conductors of the different coils are wound together. But the conductors must be insulated to withstand, at any point along their length, the full potential across the isolation barrier. For high-voltage isolation, the large volume of insulation required makes such transformers unwieldy. Also, the close spacing of the conductors often makes the interwinding capacitance relatively high, thereby providing a leakage path for ac signals across the isolation barrier.

Sector windings group many turns of each coil in sequence, allowing thicker insulation that reduces capacitance and enhances high voltage endurance. However, the turns of a sector winding act in concert to produce a toroidal flux that tends to close upon that sector more easily than upon others. This unfavorable property causes inferior coupling, as evidenced by the relatively large leakage reactance of sector-wound transformers.

Interleaved windings in which portions of different coils are alternately stacked maximize the ratio of mutual to leakage inductance. This compromise method provides reasonably low capacitance and high breakdown voltage—if care is taken to avoid mechanical stress at the jumpers between the winding segments. High cost detracts from this relatively complex solution.

Flat spirals—seldom found in small transformers—are often seen as tape windings in high-power applications. The coil pitch limits the number of turns per layer, which in turn limits the inductance attainable without complex interleaving. Although low-frequency response is poor in spiral-wound transformers, bandwidth is excellent. In this respect, in fact, stacked spirals are similar to wound multiple transmission lines. The AD293/4 capitalizes on fabrication advances that make it possible to lay down finely pitched flat spirals in a thick film.

to give a stable, highly reproducible structure. Their low profile keeps the height of the finished hybrid package to a maximum of 0.375 inch, consistent with the standard 0.4-in. clearance between printed-circuit boards and test equipment. A durable ceramic substrate supports the transformer and insulates it from other circuit components. The ferrite E-I core set extends the transformer's low-frequency response. What is more, it gives a smooth flat surface for attaching the transformer to the main isolator substrate.

The wide transformer bandwidth so important for flyback isolators demands closely spaced coils that are often difficult to insulate. Careful design of the AD293/4's critical insulation system ensures that the planar windings perform reliably at high voltages. The spirals' flat profiles allow exposed conductors to be separated by up to 0.5 in. (12.7 millimeters), reducing the risk of breakdown along the outside edges of the insulating material. These regions are most vulnerable because they may be exposed to contaminants.

Each group of three windings that makes up the input and output sections is sandwiched between ceramic layers that are bonded together with a dielectric. Excluding air from this assembly prevents corona breakdown that can easily occur in voids between the insulating layers and lead to catastrophic failure. Thick-film processing itself promotes high-voltage endurance, because it does not produce sharp points or irregularities in the conductor or insulator patterns that could localize destructively large electric fields.

A significant layout challenge is attaining a large value of inductance in the limited space available. As a result, the winding's spiral must have a fine pitch, increasing the chances of short-circuited coils. A line width of 5 mils (127 micrometers) and a line spacing of 7 mils (178 μm) make a fair compromise between inductance and yield, and so these dimensions were selected for the AD293/4.

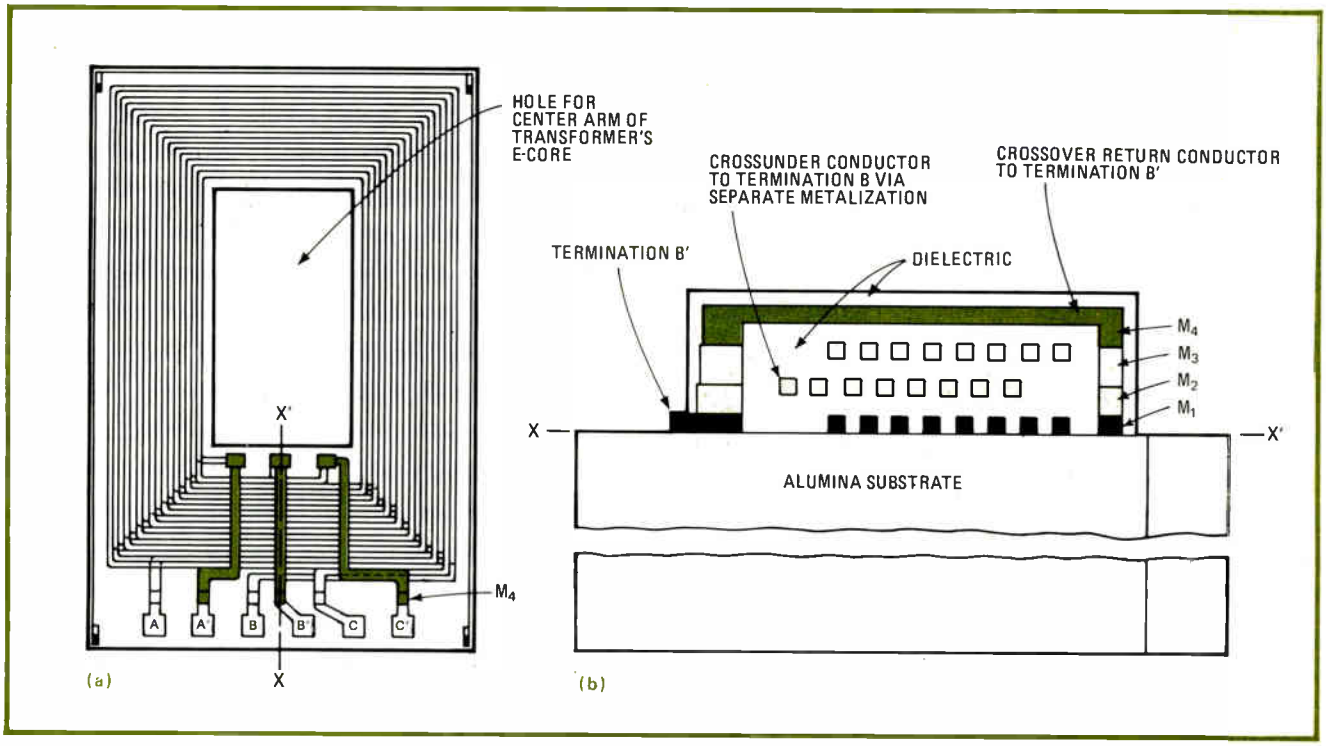
Gold is the traditional thick-film material of choice for reliable, low-resistance conductors, but recent price escalations dictate its elimination except where absolutely necessary. Thick-film copper conductors in the recent past were plagued by interdiffusion, delamination, and blistering, but newer compositions overcome these problems. Their surface conductivity of 2.4 milliohms per square (corresponding to a bulk conductivity of 2.9 $\times$ 10^{-6} ohm-centimeter) is low enough so that only a single layer is needed for each winding. Since copper can be deposited with fine resolution, the yield is not degraded.

Material progress

In this novel winding construction (Fig. 2), metal and dielectric layers are sequentially printed, dried, and fired using conventional thick-film techniques. Layers M_1, M_2, and M_3 are three separate input coils of eight turns each. Layer M_4 returns the inner end of each coil to a corresponding pad on the outer edge of the substrate.

Two identical substrates arranged back to back constitute the input and output winding sections of the transformer. The alumina ceramic substrates

2. Flat out. Conventional thick-film processing gives the spiral windings shown from above (a) and in cross section (b). To make room for eight turns the coil pitch is squeezed down to 12 mils. Sequential printing and firing builds up the conductor layers.



provide dimensional separation on top of a high-temperature dielectric so that the transformer exceeds its voltage-breakdown requirements and is compatible with high-temperature processing.

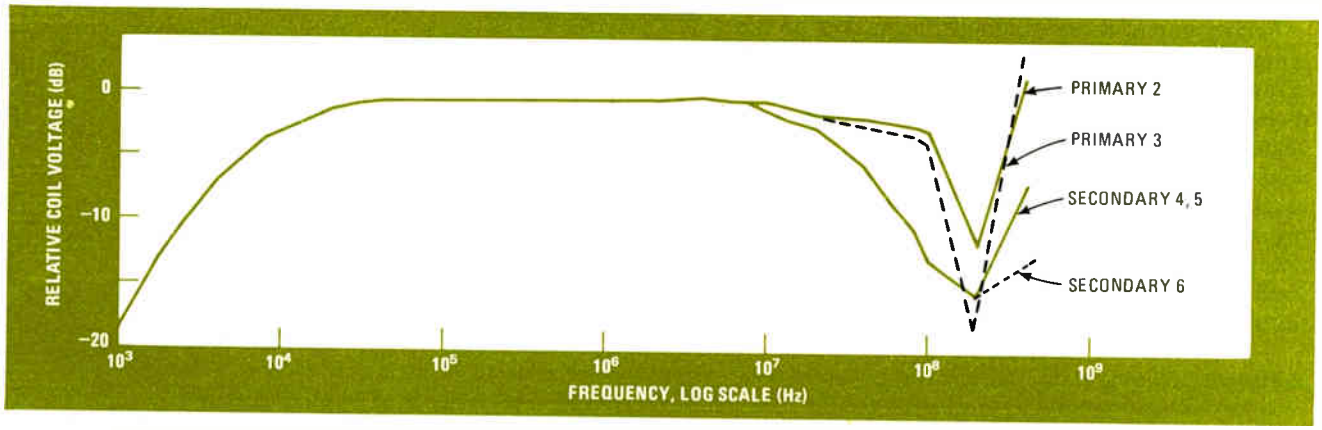
The number and correct placement of turns can significantly affect the electrical properties of a transformer. The inherent variability of these two factors in conventionally wound transformers often degrades their transfer characteristics and high-voltage endurance. The thick-film deposition process increases the uniformity of the turns, as well as allowing mass production of the transformer.

Transformer production

The uniformity of the coil fabrication process eliminates the need for traditional turns testing during and after manufacture—a simple functional check suffices as the final test. A "printing-press" approach that processes eight transformer segments on one substrate dramatically raises fabrication throughput by increasing the printing rate and reducing handling through the drying and firing cycles. Following visual inspection and electrical testing, the individual segments are separated along score lines.

To connect the completed transformer in the amplifier circuit requires a bonding method as reliable as the component itself, as opposed to traditional termination schemes that utilize staking, pin-swaging, or soldering. A hard look at those techniques uncovers many pitfalls. For example, insulation stripping typically involves dipping the wire ends in a solder pot at 260° to 370°C. The ends of fine wires often become brittle or disappear in the molten solder. Even worse, carbonized deposits remain and jeopardize high-voltage performance.

3. Broadband. The tight coil geometry of the thick-film winding's leads naturally to extended high-frequency response. The amplifier bandwidth is limited by the oscillator carrier frequency, which must fall within the transformer's passband.



Magnetic isolators still better for analog signals

Isolation amplifiers, which provide no electrical connection between their input and output circuits, have exceptionally high common-mode rejection and typically can withstand thousands of volts across their insulating barriers. Industrial process controllers, precision data-acquisition systems, and cardiac monitors are their principal applications.

Both optical and magnetic couplings are commonly used in these units to transmit the signals across the barrier. In optical isolators, the input signal modulates the output intensity of one or more light-emitting diodes, whose outputs are directed at photodiodes across the barrier. Because of the relatively poor aging characteristics of the optical components and the unpredictable propagation delay across the barrier, these isolators are better suited to digital applications where gain stability and amplifier accuracy are not critical.

The simplest magnetically coupled isolators use a single transformer to transmit signals and power between the input and output circuits. Sharing of the transformer is accomplished by periodically charging it with a brief current pulse and then using feedback control in the input section to force the flyback voltage to track the input. The stability and reproducibility of the magnetic components are generally better than those of optical parts, leading to better dc performance. The cost of magnetic components is not necessarily a disadvantage, since optical isolators almost always require magnetic couplings in order to transmit power to the input circuits.

In two-transformer isolators, an amplitude-modulated carrier couples signals through one transformer. The same carrier, unmodulated, is applied to the second transformer to power the input section. Separating these two functions gives the designer the flexibility to optimize the signal path for accurate dc performance, but it does increase the cost of the amplifier [*Electronics*, July 3, 1980, p. 151].

Since all types of magnetic isolators have an output ripple at the carrier frequency that must be filtered, their bandwidth is limited to well under the carrier frequency, which itself must fall within the transformer's passband—amplifier bandwidth is usually around 20 kilohertz at most. Optical isolators have comparable limitations, due to the response time of the photodiodes and the need for an optical feedback path to maintain gain stability. For the present, then, magnetic isolators are preferred in demanding analog applications because they give better dc performance at comparable cost. **-Roderic Beresford**

Alternatively, transformers are fitted with expensive preformed headers containing terminals in order to facilitate system assembly. A skilled operator is required to place strain-relief loops in each wire, attach them to a post, and solder the joint. Dangers abound in this process—the hot soldering iron often touches neighboring wires, destroying their insulation. Solder balls, carbonized flux, and cold solder joints impair long-term reliability. Fine wires often are unable to handle the stress imposed by the final encapsulation that may be added to improve the voltage rating of the transformer.

A different approach

The termination method in the AD293/4's transformer is a radical departure from the traditional and avoids all of the problems of the conventional approaches. Soldered-on edge clips or connectors with a 50-mil spacing for a dual in-line package are used for joining the transformer input/output pads to the device substrate.

The lead frame is first attached to the transformer substrate using solder paste and a vapor-phase reflow machine. This technique is a precisely controlled and well-ordered mass-termination process occurring in an inert atmosphere that prevents flux charring. A simple cleaning step removes all contaminants after soldering. The free ends of the transformer leads can then be attached to the parent substrate with a conductive epoxy, or they can be soldered to the metalized pads.

The thick-film spiral with its mechanically ordered termination system is a rugged, reproducible component. Since completion of the transformer is independent of parent substrate fabrication, testing before final assembly of the hybrid is simple—and salvage of the transformer or the parent substrate is possible, significantly improving the yield. The structure is amenable to encapsulation that enhances its mechanical and high-voltage endurance and also allows its use as a discrete component in other devices needing its excellent wideband characteristics.

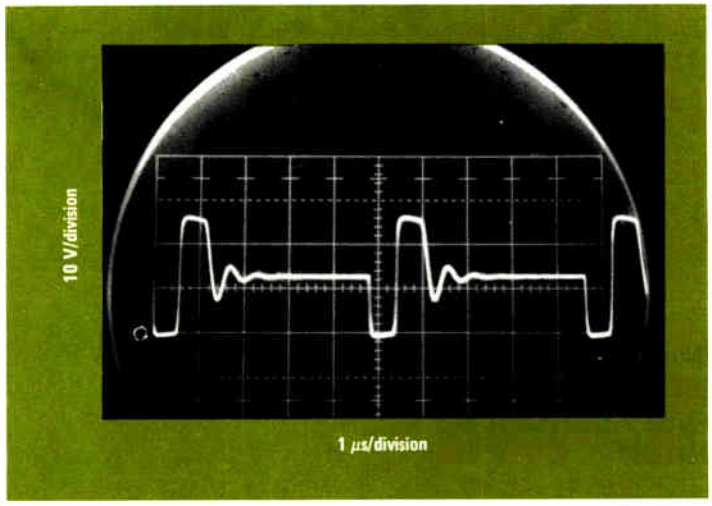
Broadband response

The superior frequency response of the hybrid transformer is evident in Fig. 3, which shows the transfer characteristics for the various windings from 1 kilohertz to 400 megahertz. In this test, a signal is applied to one of the transformer's primary windings, and the other five coils are shunted by 300-Ω load resistors. The coupling is nearly ideal up to 20 MHz and the low-frequency response extends to around 10 kHz.

The excellent performance of the transformer in the flyback isolator is apparent in the oscilloscope trace of Fig. 4, which shows two periods of the isolator carrier's waveform. The power oscillator provides the high-frequency square wave at the beginning of the period, and the input voltage controls the level of the flyback pulse that follows. Although the carrier's fundamental frequency is 200 kHz, much of the energy in the power pulses is at several megahertz and above, so that the hybrid transformer's wide bandwidth is necessary.

Not only does the transformer meet its design specifications, but prototype isolators incorporating it exceed their most important design goals (see table). Superior isolation is evidenced by the maximum common-mode voltage rating of greater than 2.5 kilovolts and the common-mode rejection ratio of nearly 120 decibels. The AD294 has a slightly thicker transformer substrate than the 293, allowing it to withstand 8 kV of common-mode voltage. The amplifier's excellent dc characteristics—low nonlinearity and temperature drift of the gain and offset voltage—will satisfy demanding data-acquisition system applications. □

4. On the job. The thick-film transformer is put to the test in the AD293/4 amplifier. Coils are energized briefly by the power oscillator (square wave), which is then switched off. The isolator's input controls the level of the flyback pulse that follows and is coupled to the output section.



PERFORMANCE DATA FOR THE AD293 HYBRID ISOLATION AMPLIFIER

	Design goal	Prototype result
Gain range, G	1 – 100	1 – 1,000
Minimum rated output voltage	±10 V	±10 V
Small-signal frequency response G = 1 G = 1,000	2.5 kHz —	3.3 kHz 2.2 kHz
Output nonlinearity, G = 1, ±5-V input	±0.035%	±0.006%
Maximum peak common-mode voltage, 1-min duration	2,500 V	>2,500 V
Common-mode rejection ratio, G = 100, 1-kΩ balanced source resistance	115 dB	119 dB
Input offset voltage at +25°C	—	±0.4 ±7/G mV
Offset voltage temperature coefficient, −25° to +85°C	150 μV/°C	75 μV/°C
Gain temperature coefficient, G = 1, −25° to +85°C	±50 ppm/°C	±7 ppm/°C

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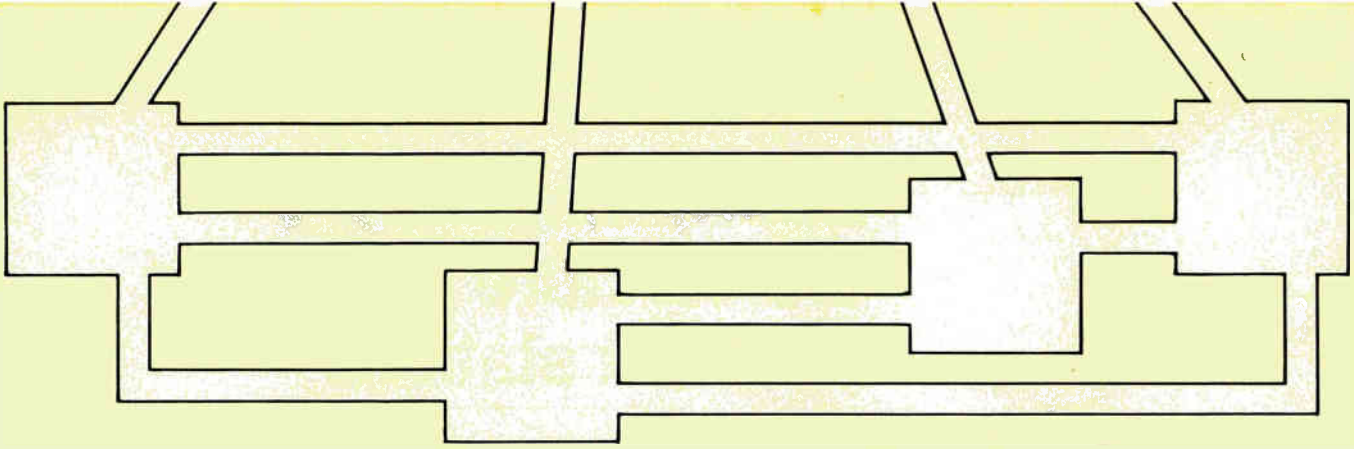


LOCAL NETWORKS TAKE TO THE FACTORY AND THE OFFICE

Diverse network schemes link personal computers, mainframes, mass storage, and many types of equipment

by Harvey J. Hindin, *Communications & Microwave Editor*
and Tom Manuel, *Computers & Peripherals Editor*

☐ Local networks have been part and parcel of distributed data-processing systems for some years. Lately, however, they have attracted a lot more attention because of the important role they are playing in integrating the many new computer-based tools intended for factory and office automation.

In the past year alone, many have entered the marketplace. Not bound by any one architecture, they range from low-cost networks for personal computers to very fast, high-volume links for mainframe units.

Some networks are proprietary and interconnect products from only one vendor. These include IBM Corp.'s Systems Network Architecture and the Series/1 Local Communications Controller, Datapoint Corp.'s ARC network, Prime Computer Corp.'s Primenet, and Digital Equipment Corp.'s DECnet.

Other local networks promise to be more flexible and, to varying degrees, can accommodate products from a variety of vendors. Some of these have been described in *Electronics*, including the Net/One from Ungermann-Bass Inc., the Z-Net from Zilog Inc., the Cluster/One Model A network from Nestar Systems Inc., and a network design from Motorola (see the issues of Sept. 25, 1980, p. 114; Feb. 10, 1981, p. 149; June 16, 1981, pp. 171 and 176). In the following articles, Corvus Systems Inc. introduces its Omninet, and Intel Corp. proposes a six-layer local network standard in which the first two layers equal the entire Ethernet scheme.

Perhaps the key area of application for these networks will be the office. In its report, "Advanced Local Networks," the Yankee Group, a Cambridge, Mass., consulting firm states, "It is clear that the local network will be a market imperative for office automation vendors within the next two years" since their ability to communicate will be the most important new feature of future office systems.

Yet there is an alternative to the local network that could win out, says Ken Bosomworth, president of the well-known data-communications consulting firm, International Resources Development of Norwalk, Conn. Private branch exchanges capable of handling both data and voice were introduced at a rapid rate throughout last year [*Electronics* April 7, p. 139], and existing voice PBXs can easily be updated with data add-ons. So it is this equipment, with its already installed networks, that will shape the office of the future, argues Bosomworth.

Industry experts do agree, however, that local networks will take as many forms as users require. Probably no single product can hope to dominate the market because of the diversity of user needs; but an astute vendor may win a profitable market share.

To achieve this, manufacturers will have to produce a low-cost local network capable of handling high-level languages and equipped with sophisticated operating systems, inexpensive mass storage, and the kind of high-performance communication facilities that allow data and expensive peripherals to be shared among many inexpensive terminals. Such a setup should have large-bandwidth communication to serve workstations separated by thousands of feet, should be easy to expand, and should be able to incorporate many different machine types. The failure of one component should not affect the operation of others, and finally, the system should be easily hooked up to remote local networks.

All this has not yet happened, of course. But the articles following indicate that vendors are attempting to meet these criteria in order to market local networks that can serve a broad spectrum of users.

Local network architecture proposed for work stations

General-purpose standard compatible with Ethernet will serve many applications at a wide range of performance levels

by Robert Ryan, George Marshall, Robert Beach, and Steve Kerman, *Intel Corp., Santa Clara, Calif.*

☐ Computer-based communicating work stations and microprocessor development systems, which promise to usher in an era of electronic offices and workplaces, will need to be attached to local networks through a standardized architecture in order to be cost-effective. In response to the lack of such a standard, Intel has come up with a local network architecture that is currently geared to work stations and development systems based on Intel microprocessors. Called iLNA, the proposed network takes advantage of the work already done in association with Digital Equipment Corp. and Xerox Corp. by using the Ethernet local network design as the basis for its own data-carrying scheme.

What has been proposed is a six-layer architecture combining software and hardware that will expedite all local network functions. Its goal is simply efficient, flexible communication between users and application programs, application programs and resources, and any other combination of users, programs, and resources within the local network.

The concept of a layered architecture is not new. Indeed, IBM's well-known Systems Network Architecture is layered, as is the forthcoming International Standards Oganization and American National Institute Reference Model of Open Systems Interconnection. What is new is the fact that a network architecture has been specifically designed for Intel- and Ethernet-based equipment (see "Specifying the network," p. 122). If eventually accepted as an industry standard, the proposal will become the basis for future network architectures, and manufacturers of equipment that hooks up to local networks will want their equipment to be compatible.

In developing a local network architecture, the primary goal has to be achieving cost-competitiveness with any general-purpose network design, while at the same time equaling the efficiency and performance of a network designed for a specific application. Likewise, the network has to facilitate communication through commonly used interfaces but not be bound by any one topology or internal communication mechanism. In addition, it has to function independently of any particular computer's operating system or hardware.

The network also has to act as an error-free message-delivery medium between communication processes (programs resident in equipment attached to the network) and permit an operator or program to monitor, maintain, and modify network operations. While performing all these chores, the network must also be able to serve low-cost, low-performance equipment and incorporate future technology. In addition, the failure of any device at a work station should have minimal effect on the operation of other work stations.

To perform all these tasks, the Intel network architecture defines a set of interfaces, algorithms, and protocols by which application programs on various kinds of Intel microprocessor-based work stations can communicate. It also establishes a process-to-process communication mechanism whereby a process (any application, function, or peripheral using the network) is defined as the active element in a communicating node and the ultimate source or destination for data. Thus, for example, terminals, files, and input/output devices can communicate with one another through the use of processes. Messages are sent and received by the designated processes through what is termed a communications socket, which is a hierarchical address composed of three unique identifiers—one each for the local network, the host, and the port to a process.

Each node in the network, which may consist of one or more pieces of equipment, has a unique host identifier that distinguishes it from all other nodes installed anywhere, to ensure eventual communications between equipment on various local networks. Within each node, each process is given a local address, or port identifier. The binding of ports to processes is the responsibility of the node, and the ports remain unique within each node. Certain ports, however, may be assigned numbers in accordance with a globally consistent scheme.

Each installed local network will be given a unique identifier, its network identifier, that identifies it in multiple-network applications. In a single-network application, the network identifier is not used, but its assignment assures that an orderly progression to an internetworking environment is possible.

In designing its architecture, Intel examined applications needs of its users and chose a suitable set of

interconnect functions to serve them. These functions were then defined in a series of layers that permit the network to achieve high performance across a wide applications base. The architecture is divided into six layers (Fig. 1). The ones of interest here are the physical-link, data-link, transport, session, and network-management layers. The network layer is used when one local network must be connected to another.

The lowest-level means of sending data from one node to another, the physical-link layer, is responsible for delivering the smallest unit of data (the bit) the network handles. This layer is the one directly concerned with the transmission medium, signal type, data rate, and mechanical interconnect specifications of the network. It can be implemented using two modems, two telephone sets, and a telephone line or using coaxial cable, a baseband line driver, receiver chips, and a universal synchronous-asynchronous receiver-transmitter (Usart).

Moving from node to node

While the physical link moves data bits from one node to another, it cannot guarantee successful transmission. Electrical noise in the environment causes errors, although some transmission media are less susceptible than others. For example, the error rates generally run between 1 bit-error per 10,000 bits and 1 bit-error per 100,000 bits for transmissions over a modem-telephone network, but can be less than 1 bit in 10 million for local coaxial-cable–based networks.

Error rates can be kept quite low at the physical link level if the network designer is willing to properly locate and shield the network cabling from rf interference by other electrical utilities in, say, a building. However, the higher-level layers are a better place to reduce errors because they can exploit such multiple-bit schemes as redundancy codes and automatic repeat requests that are not available at the physical link level.

In the Ethernet physical link, data is transmitted on a 50-ohm coaxial cable that is up to 500 meters long per segment. The Manchester-encoded, baseband signal carries data at a rate of 10 megabits per second. At the start of a transmission, a 64-bit preamble is used to stabilize and synchronize the communication channel circuitry. After reception, the preamble is removed and only the Ethernet header and data are passed on.

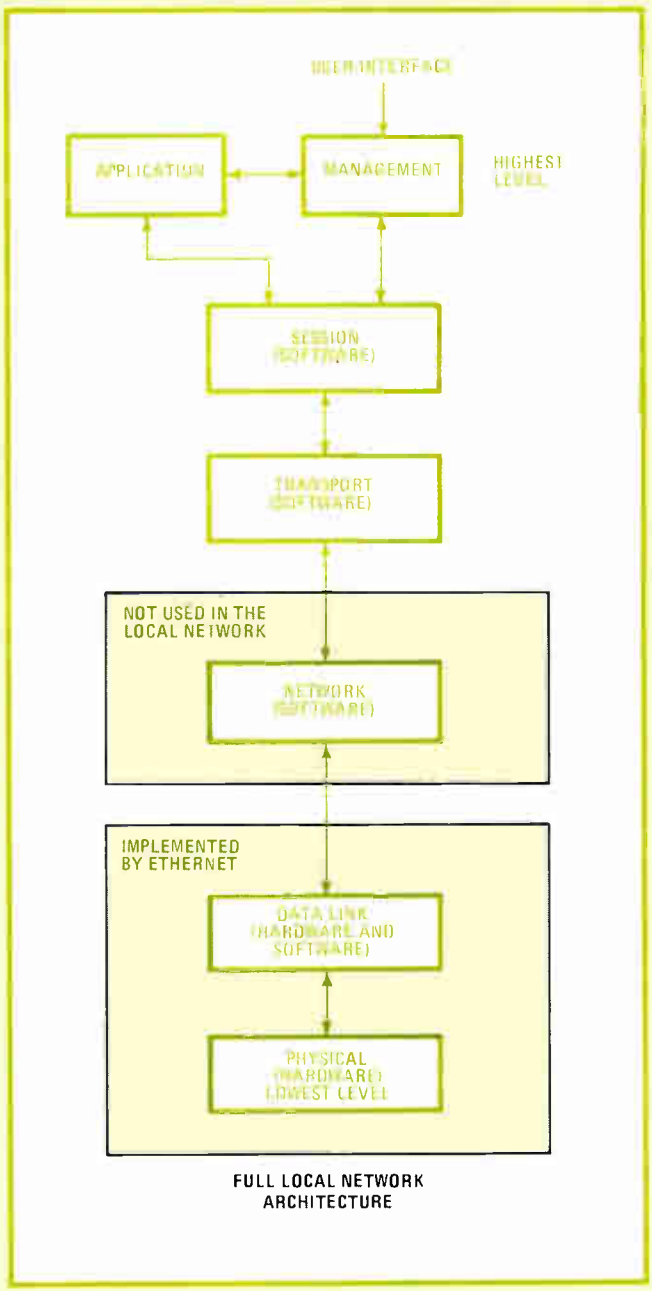
Packet-delivery service

The data-link layer makes possible a node-to-node packet delivery service. As such, it is the first step toward a process-to-process packet delivery system. The data link supplies some of the services missing from the physical link. Among others, it is responsible for framing, or the determination of where a message begins and ends; addressing, or the determination of which station should receive a message; error detection, or the determination of bit errors in the packet; and link management, which controls the access of multiple transmitters and receivers to the physical link.

A data link may deliver all the packets error-free by using various error-correcting protocols. Or it may provide, as the Ethernet data-link architecture does, a best-effort delivery service in which not all packets are delivered, but all those that are, arrive unmodified. With error-free packet delivery all packets are delivered (no lost packets), all packets are delivered just once (no duplicate packets), and all packets are received in the order sent (no nonsequential packets). However, when error-free packet delivery is required, data-link error control is necessary to perform packet sequencing and retransmission. In addition, besides having the higher-level error-coding alternatives previously noted, data-link error control also is expensive and, given the physical-link error rates, not cost-effective.

Data-link error control might provide a reliable node-

1. Layers. In the Intel local-network architecture, there are six levels of hardware and software, with the network layer omitted in strictly local (non–store-and-forward) configurations. The physical link and data link contain hardware; the others only software.



FULL LOCAL NETWORK ARCHITECTURE

Specifying the network

The Digital Equipment–Intel–Xerox specification for the Ethernet network is the first portion of Intel's forthcoming local network architecture, and the first hardware produced for this architecture will be the Ethernet intelligent controller. The two-board set, which plugs into an Intel Multibus chassis, supplies many of the functions of the physical- and data-link layers of the network architecture.

The data-link functions performed are framing (including packet-boundary delineation and address recognition), link management (including transmission scheduling and retries in case of a collision between packets), and error detection. The physical-link functions performed are preamble generation and removal and bit encoding and decoding. The set also handles a number of system-oriented functions, such as interfacing with the system parallel bus, communicating with the central processing unit, handling data movement to and from the buffers, and interfacing with the transmitter-receiver units.

The board hardware consists of an Intel 8086 5-megahertz microprocessor with local random-access- and read-only memory, direct-memory-access channels for sending and receiving data at the required 10 megabits per second, bit-serial send-and-receive logic, packet address-recognition logic, error detection logic, and interval timers. One board contains the microprocessor, memory, timers and DMA control; the other contains the serial send-and-receive and error-detection logic.

The boards implement part of the data-link layer and also contain seven major software functions. These include the executive (or scheduler), the rest of the data-link software, transport control, session control, network management, the bootstrap, and diagnostics. Typically these software functions are implemented with programs that occupy small amounts of memory space.

to-node delivery service, but it does not ensure a reliable end-process–to–end-process delivery service. That is particularly true in any internetworking environment where two or more local networks are connected and there are multiple gateways (the physical and software connections) acting as packet forwarders. The risk of packet nondelivery then is moderate to high. In addition, end-to-end delivery retransmission (error control) would still have to be performed at the transport layer, making error control at the data-link layer redundant.

Collision insurance

The data-link software supports a large address space—up to a 48-bit destination identifier and a 48-bit source identifier—to permit flexibility in managing internetwork gateways. In operation, data-link users must supply both transmit requests and standby receive-buffers to the network. The transmit requests contain the address of the destination nodes and the data to be sent. The data link combines both into a packet that is transmitted when the line becomes idle.

Should multiple nodes transmit concurrently, they all abort their transmissions, generate a jam signal that reinforces the initial collision signal, wait a random interval before retransmission to avoid repeated collisions, and then try again. The average retransmission interval increases as a function of channel load in order to achieve channel stability under overload conditions.

On the receiving side, the intended packets are recognized by the data link, which performs a 32-bit cyclic redundancy check. If the packet is good, it is placed in an empty receive buffer. A packet that has collided is recognized as such and dropped.

As noted earlier, the data link supports framing, addressing, error detection, and link management. In the Intel Ethernet approach to framing, a carrier-sense function determines the end of a packet. When the carrier is lost, the packet is finished. The two-bit beginning-of-packet indicator at the end of the preamble actuates carrier sensing.

The address scheme permits a received packet to be accepted by any number of nodes. The data link recognizes single-host, broadcast, and multicast addresses. The first bit within the destination address distinguishes between single-host and multicast delivery, and the next 47 bits determine the multicast group identifier. Broadcast addressing is simply a special case of multicast in which the next 47 bits are all logical 1s.

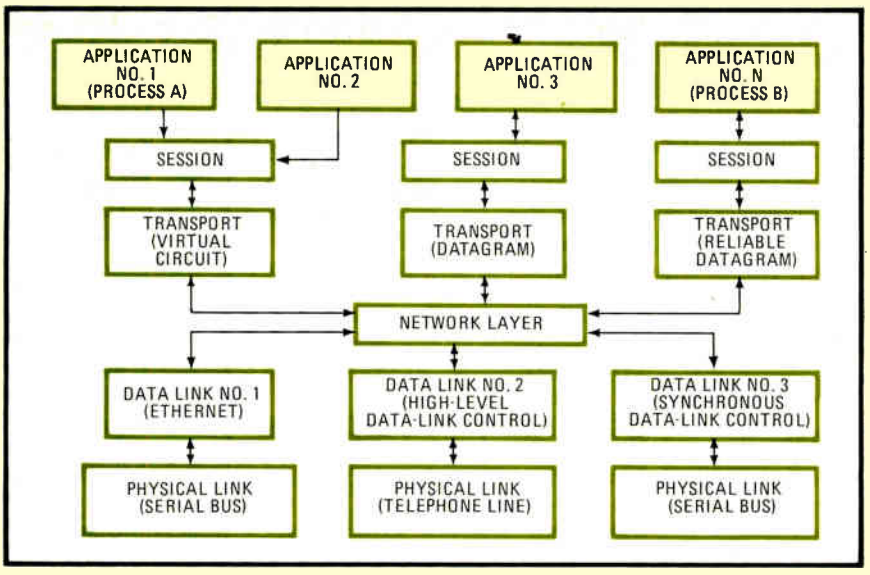
The link management function controls line access when two or more nodes attempt to transmit data simultaneously through an arbitration policy called carrier-sense multiple access with collision detection. With this system, when a packet is to be sent, the link management facility determines if another carrier is present. If this is so, or if the interpacket gap time has not expired, the waiting packet is not released onto the line. When the data packet is finally transmitted, the link management function monitors the line to determine whether a collision has occurred. If a collision is detected, the random waiting period for retransmitting the packet is chosen by executing what is known as a truncated binary exponential back-off algorithm.

Reliable transport

The transport layer software (there is no hardware in this layer) makes possible location-independent, reliable packet transmission. Users of this layer can establish, maintain, and terminate virtual circuits, which represent full-duplex data paths between sockets.

A virtual circuit is defined by its basic properties. First, it permits multiple virtual connections to exist between processes. Second, it can be dynamically managed by the communicating processes. Third, it can accommodate message lengths that are independent of transport communication. Finally, it transmits data in a full-duplex error-controlled and flow-controlled format.

While the data-link layer makes a best-effort attempt to move individual packets from one physical node to another, the transport layer is responsible for reliably moving a user's variable-length message, such as a file transfer, from one process to another, even though the underlying packet delivery service will occasionally drop packets, duplicate packets, or deliver them out of order. A secondary responsiblity of the transport layer is to



2. Extensions. The six-layer local network architecture can be extended to include remote network configurations by simply adding the network layer and the new data links. These new configurations can be co-located or geographically dispersed.

prevent fast transmitters from swamping slow receivers. It also must ensure that the network's communication subsystem resources (primarily media bandwidth, communications processor usage, and communications buffer memory) not be wasted in frequently retransmitting packets when there is a speed mismatch. Both are accomplished by a flow control function that throttles fast transmitters when the receiver cannot keep pace.

The transport software serves several other functions as well. Since the transport layer should insulate user software from the limiting characteristics of the underlying physical network, it performs fragmentation and reassembly services that let the user software send arbitrarily long messages over the network. To accomplish this, the transmitting transport software breaks messages into packet-sized chunks and the receiving software then reassembles them.

Acknowledge and over

In order to provide its services, the transport software carefully manages the user's service requests and the packets exchanged on the data link. For example, the transport software associates a unique sequence number with every packet it sends. Likewise, the receiving transport software sends back acknowledgment packets, indicating with the sequence number which packets have been correctly received and accepted. Packets not acknowledged within a specified time are automatically retransmitted by the sender.

The transport software controls the data flow by exchanging information on the amount of receive-buffer memory that each claims to have available. The amount of buffer memory available is called a window, and a receiver that has indicated it has a large amount of receive buffer space is said to have its window wide open.

Open window

If the transmitter has several data packets, they will be delivered much faster if the receiver has sufficient buffer space and has opened its window than if the window is small and requires an exchange of window information after each packet is sent. To expedite the information exchange, the transport software uses a combined error- and flow-control algorithm that permits both functions to work at the same time. For process-to-process addressing, the transport software adheres to the standard network-address structure, which consists of the network, host, and port identifiers.

The session control software layer identifies and locates process names within the network. In order to communicate, a process using the transport layer in one node must know the socket of other processes. Since, it is unlikely that the naming convention for processes under a given computer's operating system conforms with that used in another, the session layer resolves this problem through a location-independent scheme known as a binding function, which provides users with standard-format, location-independent names for remote processes they must access.

Ties that bind

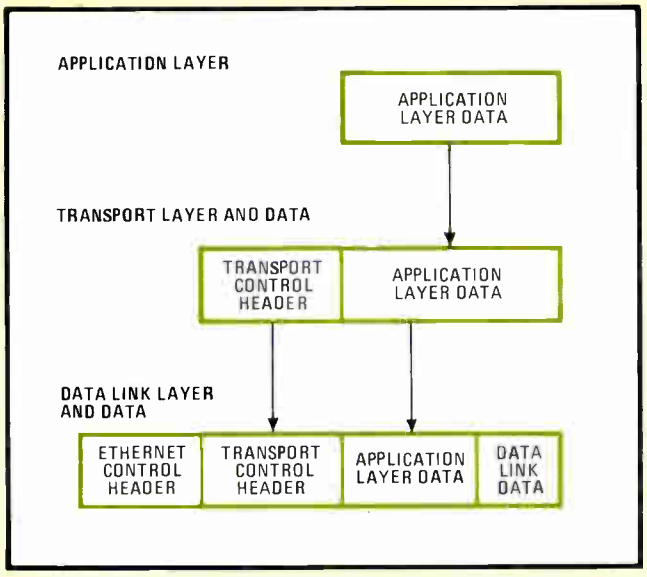
The binding function is composed of two operations—mapping and updating. Mapping is the function that, on demand from the user software, translates between process names and sockets. Updating distributes the mapping information throughout the network so that it is available when needed at each node.

The session software also supplies network status information to the application software. In turn, the transport software gives the session layer status information on its best estimate of the quality of the underlying network layers. However, the decision to abort a connection is left to the user for all but the most extreme cases, such as evidence of total equipment failure.

Network management

The network-management software layer provides the user with all those functions not required for normal operation. In addition, it includes diagnostic utilities for accessing the network components when any portion of the network fails. It also has maintenance tools that gauge the performance of various network components so users can plan for changing network demand.

Network management functions fall into one of three



3. Headers. If two processes on two different local network nodes want to communicate, the session layer software establishes a virtual circuit between them. The transport- and data-link layers add headers for identification, addressing, and control.

categories: operation, maintenance, or planning. The operation category includes all functions that are performed on a day-to-day basis as part of normal network operation. A major goal of the Intel network architecture has been eliminating the full-time network operator, and thus only the network bootstrap and the manual operations needed to add a new node to the network are included in the management layer.

The network bootstrap is the operational function used by a booting node to load its operating system from another network node. The bootstrap sequence begins when the booting node transmits a multicast packet addressed to any node that has a copy of the operating system and is willing to send it. If such a node exists on the local Ethernet data link, it will respond.

Should more than one node reply, the booting node will accept the first reply and ignore all others. If no reply is received, as would happen if either the request or reply is lost in the network because of line noise, the booting node will retransmit the request. If a reply still is not received after several retries, the bootstrap attempt will be aborted.

Preventive maintenance

The maintenance category detects failures in the network, even though it may be uncertain of exactly what the problem may be. Problem detection proceeds through three mechanisms. The first is a set of error counters made possible by the management layer; the second is an error-reporting and -logging mechanism; and the third is user observation.

The first problem detection mechanisms, the error counters, are maintained by the individual layers and record occurrences of recoverable errors. The presence of errors does not necessarily indicate a failure in that the layers are designed to operate normally in the face of a large number of errors. An excessive number of errors, however, may indicate that a problem is developing.

Since this set of counters is maintained at each node in the network, and since the nodes can be spread over a large area, the network management layer includes a remote examination function for interrogating nodes without interfering with network operations. The network management layer in a node desiring information from a remote node first sends a request to the network management layer in the remote node. The management layer in that remote node then performs the desired function and transmits a response to the requesting node.

Isolating errors

The error-counting mechanism is supplemented by an error-reporting mechanism that logs problems detected by the communication system to an error-logging file. Once a problem has been detected, it is isolated to some serviceable component through two mechanisms. First, the same error counters are used to isolate the error. Second, the management layer generates test traffic, including a loopback function within each layer, and observes the behavior of the system.

Generally, correcting the problem involves repairing or replacing hardware. Some problems, however, can be corrected simply by reinitializing a system component. In that case, the management layer can stop and reinitialize each layer.

In its planning function, the management layer supplies the network administrator with statistical information about the use of the network to help in planning network growth.

By way of example

To illustrate the operation of the software and hardware layers with a practical example, consider a case in which there are two processes, A and B, that reside on two different nodes (Fig 2). Application process A's request to communicate with process B on some remote node requires the cooperation of the communication layers of each node.

The source node's session layer first determines that process B resides at socket n, thus pinpointing process B to a specific port residing in a specific node on a specific network through the port identifier. By means of the transport interface, the session layer then attempts to create a virtual circuit between the source port and the destination port. Assuming there are no conflicts on the network, the virtual circuit is established after the two transport-layer sites exchange connection information.

The two processes can now send or receive over the virtual circuit so that data can be delivered in order, unmodified, and without duplication. The transport layer adds a transport header that includes the virtual circuit identifier and a sequence number to each piece of data it handles. It then passes the data, transport header, and application data to the Ethernet data link.

The data link adds its header (Fig. 3), consisting of the address (destination and source identifiers), framing, and error-detection bits, and it then attempts to transmit the packet. Once the data-link has established the carrier signal, the physical link is reponsible for the transmission of the bits over the serial link. □

Network minimizes overhead of small computers

A two-wire cable and a microprocessor-based interface board direct all the traffic in a low-cost 1-Mb/s local network

by Mark Hahn and Phil Belanger, *Corvus Systems Inc., San Jose, Calif.*

☐ Personal computers can approach their full potential in business applications only when they are tied into a local network. Such a network satisfies the need for efficient communications by enabling a collection of inexpensive computers to share not only data but also expensive peripheral equipment.

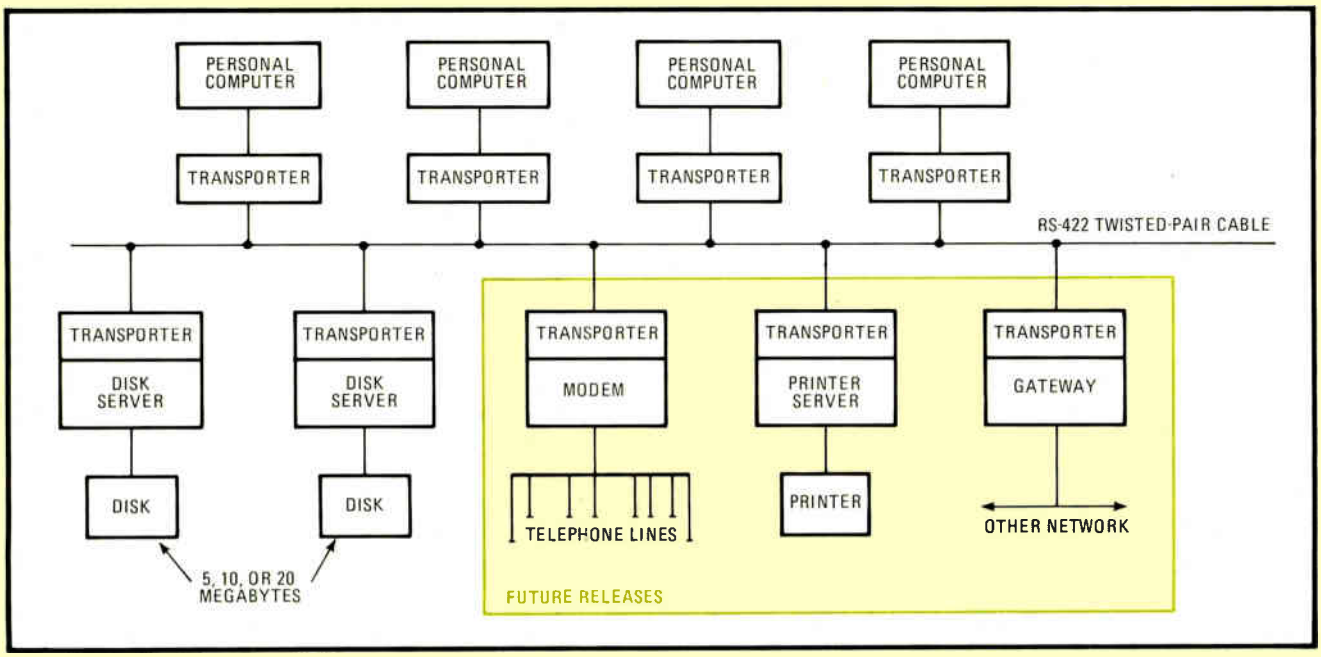
The Omninet local network from Corvus Systems connects many popular personal computers and minicomputers, from the Apple II to the LSI-11, using simple twisted-pair cable and a correspondingly simple network interface board (Fig. 1). The intelligent network interface, called a transporter, contains processors and software that eliminate the need for a complex cable and sophisticated network software in the host computer. The result of all this is a low-cost, durable, heavy-duty network operating in the medium-speed area of 1 megabit per second.

As many as 64 computers or peripheral devices, each with a transporter installed, can be supported on a network of up to 4,000 feet (1.2 kilometers) of twisted-pair cable meeting the RS-422 standard. No repeaters are required on networks of up to 2,000 feet of unshielded cable or 1,000 feet of shielded cable.

The transporter in each node manages the network for that node, thus serving as the common network interface for all nodes. Every transporter is the same except for a small part of its circuitry for interfacing with a particular host. No master network controller is required, as the individual transporters supply all the control needed for the chosen distributed network control scheme, known as carrier-sense multiple access (CSMA).

In addition, to reduce the burden on the host, the transporter performs many high-level network tasks that are often the responsibility of the host computer in other networks. Generating and receiving acknowledgments, retransmitting messages, and detecting duplicate mes-

1. All hooked together. A typical Omninet network may contain several personal computers and a disk drive or two, and in the future it will be able to add printers and modems for dial-up access by terminals and interconnection with other networks.



sages all are performed automatically by the transporter. A host computer sends messages by issuing a simple command and is not disturbed by the network transporter until a valid message arrives.

Heart of the net

The transporter implements the network protocol for the first four layers, or levels, of the International Standards Organization and American National Standards Institute's Reference Model of Open Systems Interconnection—that is, through the transport layer (Fig. 2). Hence the name, "transporter."

The transporter fundamentally consists of nine integrated circuits (Fig. 3). The basic design uses an interface for directly accessing the memory of a host computer (DMA) that can be adapted for almost any processor bus with a minimal amount of additional hardware. For example, the Apple II computer can be accommodated by adding only five ICs to the basic transporter.

A gate array customized for the Omninet transporter—one of three main chips—controls the interface between the transporter and the host computer's bus or a peripheral device. This control logic requires no buffering of data in the transporter—it can access the host computer's memory directly with a 24-bit address. It also controls the RS-422 driver and receiver circuits—the network transceiver.

Secondly, a Motorola MC6854 Advanced Data-Link Controller (ADLC) is the low-level network interface with the cable. The chip performs many of the functions of the data-link layer, including bit serialization; cyclic-redundancy-code generation and checking; packet framing; 3-byte first-in, first-out buffering; and implementation of the bit-level protocol, which uses nonreturn-to-zero inverted encoding. Zero insertion is also performed whenever the bit stream contains more than five 1s together.

A Motorola MC6801 single-chip microcomputer oversees the two interfaces and manages the conversion and transfer of data and control information between the host computer or peripheral device and the network. The 6801 is a 6800 microcomputer with expanded instructions, 2-K bytes of read-only memory, 128 bytes of random-access memory, 27 input/output pins, and a timer and counter, plus other features.

Complete control

The DMA interface is unusual in that each cycle is explicitly invoked by a 6801 instruction. When instructed, the gate array stops the 6801 processor's clock until a memory access of the host is completed. Through this feature, the transporter's software has complete control of the transfer of data between the transporter and the host computer.

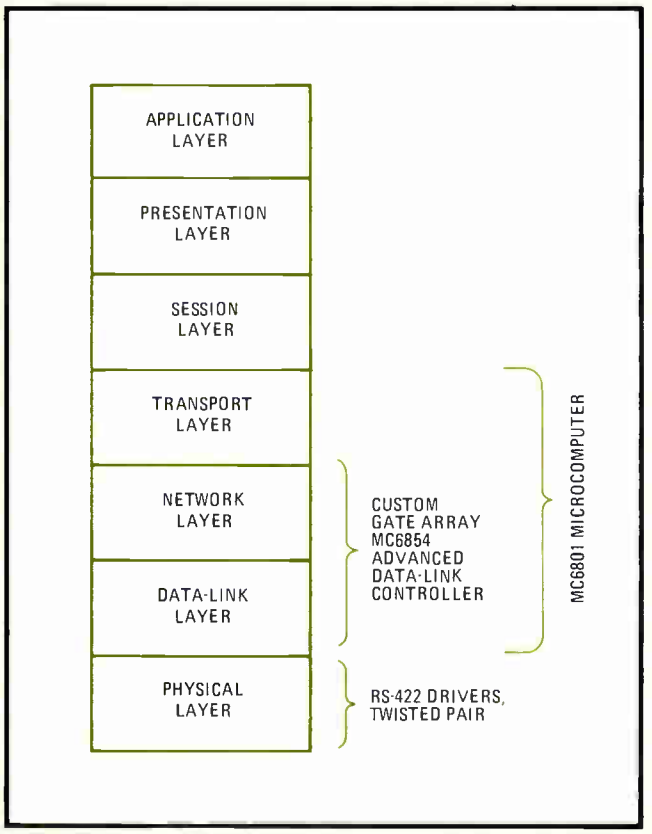
With this kind of control, two DMA cycles, one right after the other, can be completely unrelated with respect to their location in the host memory. This capability, in turn, makes possible the implementation of packet splitting and demultiplexing. An example of the 6801 software code for DMA reading and writing between the transporter and the host is shown on page 128.

The RS-422, or physical-layer, protocol, governed by the gate array, uses no carrier signal. However, a function in the Advanced Data-Link Controller, operated at the data-link layer, can tell if there has been a transition on the cable, or in other words, activity on the net. Omninet defines activity on the net as its carrier signal.

Carrier sensing takes place twice. When the ADLC senses that there has been no activity for 15 microseconds, it tells the software in the microcomputer that it may proceed with a transmission. The software then instructs the interface control logic to start a transmission. Because considerable time elapses during the execution of the software instructions—about 35 μs since the ADLC has reported no activity—a second level of carrier sensing is invoked. Special high-speed logic designed into the gate array makes a last-nanosecond decision by checking the network activity again before sending data out on the cable. If there has been no activity since the previous check, it proceeds with the transfer; if there has been activity, it aborts the transfer and tells the software that it must wait and try again.

Stopping collisions

With the two levels of carrier-sensing hardware and the collision-avoidance software, collisions—two or more stations trying to transmit at the same time—are almost always avoided. Consequently, Omninet operates efficiently without collision-detection circuitry, which would make the system more complex and more expensive.



2. Seven-layer cake. The layered reference model of the International Standards Organization and the American National Standards Institute divides local network functions into seven hierarchical layers, or modules. Omninet implements the four lowest layers.

The interface control logic also extends addresses, when necessary, for the DMA transfers between the transporter and the host computer. This address extension allows the 6801 to address host computer memories having up to 24 bits of address space, even though it itself has only 16 address bits.

Another cost savings results from the simple transceiver design. The complete transceiver is implemented with just two ICs, a Texas Instruments SN75174 differential line driver and an SN75175 differential line receiver. These interface circuits go beyond the RS-422 protocol by allowing any two interfaces to be active at once without damaging the circuits. They have a high level of noise rejection through hysteresis. Since the balance differential signals can have up to 24 volts of difference in their common-mode voltage, no isolation transformers or optical isolators are required, as would be the case with coaxial cable.

Twisted-pair rationale

There are several reasons why twisted-pair cable was selected. The first is its low cost. The second is that anyone can install a network—lay the cable and connect the Omninet transporters to it—using only pliers and a screwdriver (the task is similar to hooking up hi-fi speakers). On the other hand, shielded twisted-pair cable is no more susceptible to radio-frequency interference than coaxial cable.

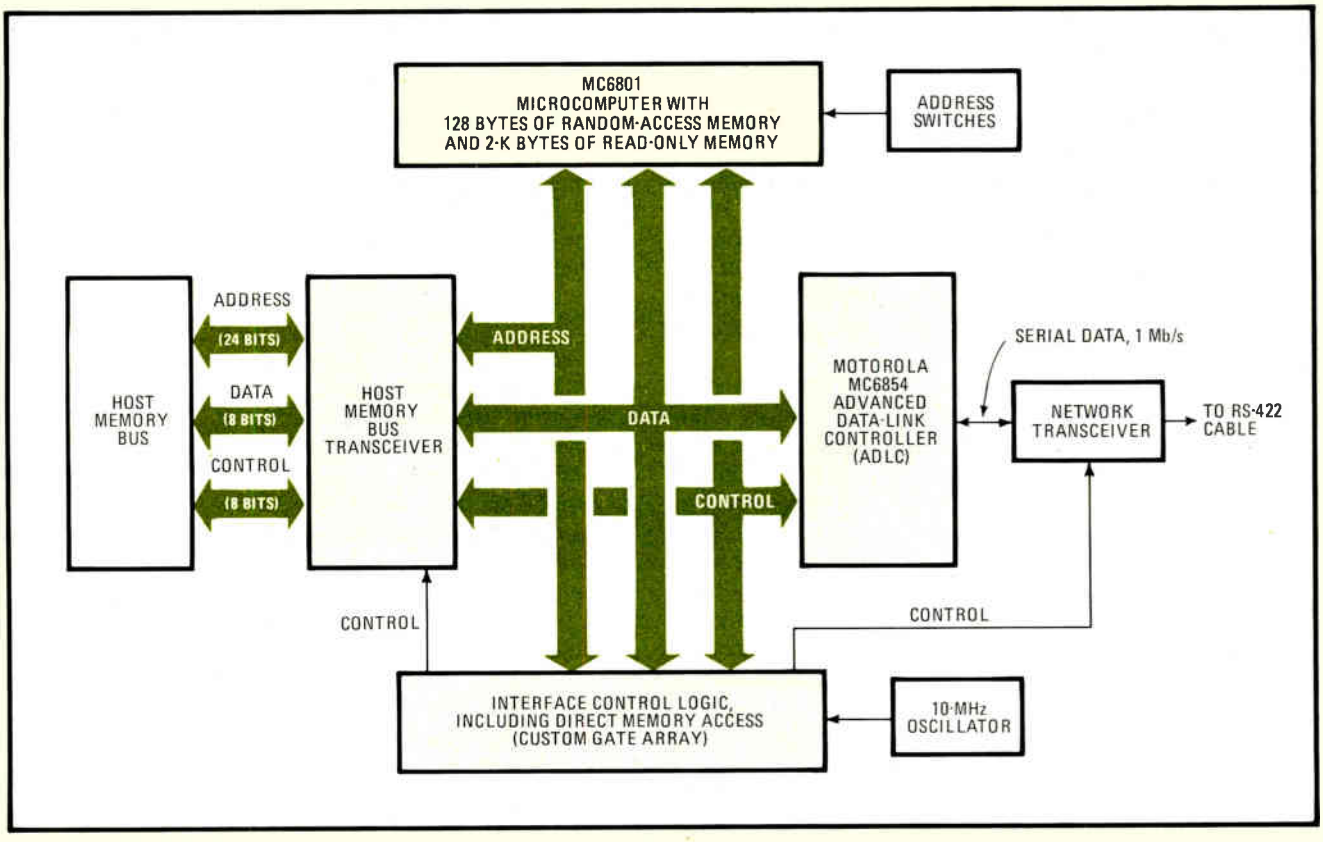
The performance of the network is enhanced by its efficient low-level acknowledgment scheme. Omninet uses what is called a positive acknowledgment protocol; that is, every message, if received correctly, is acknowledged by the receiving station. If a message is not positively acknowledged within 15 to 20 μs, the sending station will retransmit it after waiting a random time interval. A message is retransmitted until it is acknowledged or until it has been retransmitted a maximum number of times specified by the user.

The transporter receiving a message sends the acknowledgment as soon as the message has been validated. The receiving station does not wait or check the line for activity before sending the acknowledgment, but all other stations wanting to transmit are waiting because they will have detected that the line is busy. Therefore, acknowledgments are sent immediately and never lost. As noted, all the acknowledgments and retransmission processing is done by the transporters, without any involvement on the part of the host computers at each station.

Many factors determine how long the transporter software will wait before retransmitting a message after not getting an acknowledgment or after being told by the hardware that the line is busy. With the transporter's retransmission algorithm, the wait clock that measures the random time interval between transmissions ticks only when the network is idle. The busier the network, the longer it takes for this random time interval to elapse. Thus the transmission or retransmission rate is adjusted automatically according to the level of traffic on the network.

The algorithm also eliminates the queuing phenome-

3. Smart transportation. The Omninet transporter is really a small computer with its complement of intelligent digital hardware and software, including a custom gate array for interface control. The transporters perform distributed control of a 1-Mb/s local net.



6801 INSTRUCTIONS FOR TRANSFERRING ONE PACKET		
	PROGRAM	COMMENTS
	LDS ADDR	Load address of data buffer.
	LDD LENGTH	Get length from Omninet header.
DMALOOP:	INS	Increment stack pointer, causing hardware to stop 6801 clock, read byte from advanced data-link controller, and directly access the host's memory and store the data at the address in stack pointer.
	SUBD #1 BNE DMALOOP	Decrement loop counter.

non that is often a problem with the usual CSMA protocols. Queuing occurs in CSMA networks when two or more stations are ready to transmit a packet while another is being sent. Every station must defer its transmission until the network becomes idle again. Since each station with a message to transmit will try to send as soon as the current transmission is completed, another collision will usually result, and that would necessitate further waiting. When the retransmission interval is shorter than the time it takes to transmit a packet, queuing occurs and the randomness of the wait time is canceled. In the Omninet local network, the wait-time between transmissions does not elapse when the network is busy so several transporters will not queue up during the transmission of long packets.

Two types of services

The transport layer in network systems usually provides one of two types of services to the higher-level protocols: either diagrams or virtual circuits. A datagram is a single, short, one-way message that is not guaranteed to reach its destination. Datagrams are fast, efficient, and well-suited for transaction-based systems. They can take full advantage of the broadcast nature of the network. However, they are severely limited by their length and the fact that they are one-way.

A virtual circuit, in contrast, is a sequenced and synchronized two-way conversation that usually involves the exchange of several messages. Virtual circuits minimize the probability that messages will be lost, duplicated, or received out of order. They can be made up of datagrams, but that implies that each high-level protocol requiring reliable data transfer must implement its own dependable delivery mechanism.

Providing virtual-circuit service in the Omninet transporter would have required much more memory than that available in the 6801, and adding the necessary external memory and software would have increased the cost of the transporter to an unacceptable level. On the other hand, many of the hosts that will be used on Omninets will be 8-bit microcomputers with limited memory space and unsophisticated operating systems, and stealing memory from them is a bad idea. These systems can neither hold enough software nor spare enough processing time to perform reliable communications using just a simple datagram service.

In other words, datagram service was considered not good enough for personal computers, whereas complete virtual circuits are too expensive.

4. In the packet. The format of the Omninet packet has two header fields. The user header is optional and may be employed to split a packet. The network transporter software can put data from the user header in a different place in the host memory from the user data.

Toward a virtual circuit

The compromise decided on for Omninet's transporter is more reliable than datagrams but not as secure as virtual circuits. It is called a micro virtual circuit—because state information about message transfers is maintained for only microseconds and because it provides many of the same features as a virtual circuit. Micro virtual circuits guarantee that a message sent through the network will be received correctly by the appropriate host. If not, the sender will be notified that the message was not delivered. Furthermore, duplicate messages will be discarded and messages will arrive in the same order in which they were transmitted.

The network's responsibility for routing data does not end when the packet arrives. The transporter then transfers the data into the host computer's memory at the location specified in special memory-address sockets. Each transporter contains four sockets, any number of which may be activated at one time. The socket number is specified in a separate file in the packet header, and the transporter automatically loads the incoming packets into the correct places in host memory.

Packet splitting is another network function that uses the socket structure. As shown in the Omninet packet format (Fig. 4), a packet may include a user header. If a user header is specified, the transporter will transfer it into a different memory location from the one used for the data portion of the packet—for example, the former into the system memory and the latter into the user space. This technique eliminates the need for the host computer to move the data from one memory location to another each time a new packet is received.

Low-cost servers

Corvus Winchester disk systems can be installed on an Omninet network with the disk-server transporter. This stand-alone device is a standard transporter with extended 6801 code and a Corvus disk system interface; it costs little more than a standard transporter. All host computers on the network can share the disk storage. The disk server eliminates the need for a computer to interface the disks with the network, thereby contributing to low cost and high performance because no time is lost transferring the disk data into and out of a dedicated computer. Currently, one server can support up to four disk drives of 6, 11, or 20 megabytes, for a total of up to 80 megabytes of shared storage. Another device, similar to a server, is the Omninet gateway computer for interconnecting Omninets or linking them to other networks such as Ethernet, IBM's System Network Architecture, and public packet switched networks. □

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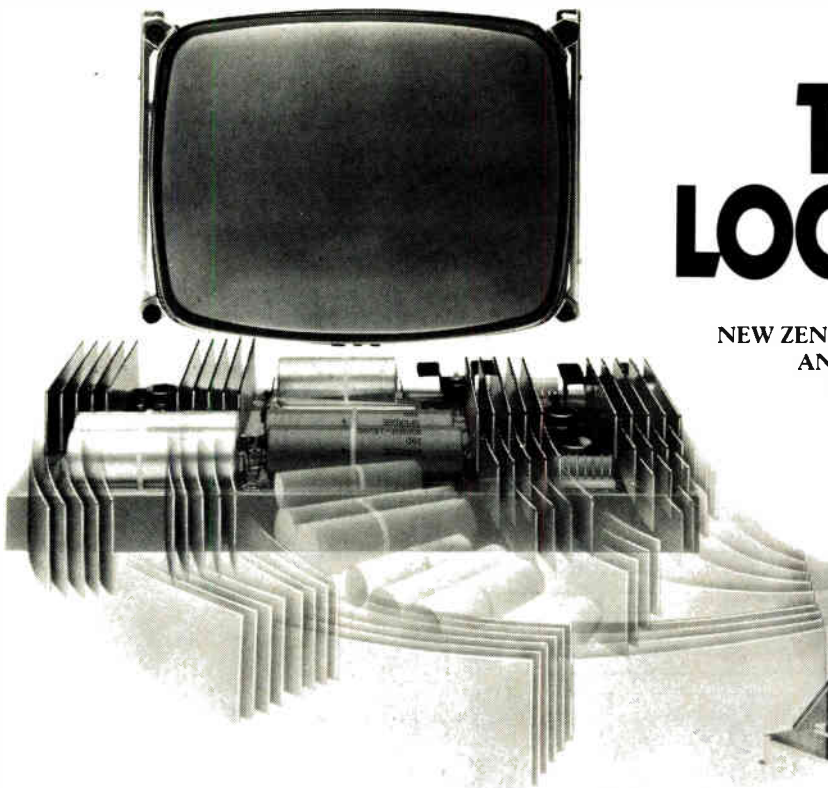

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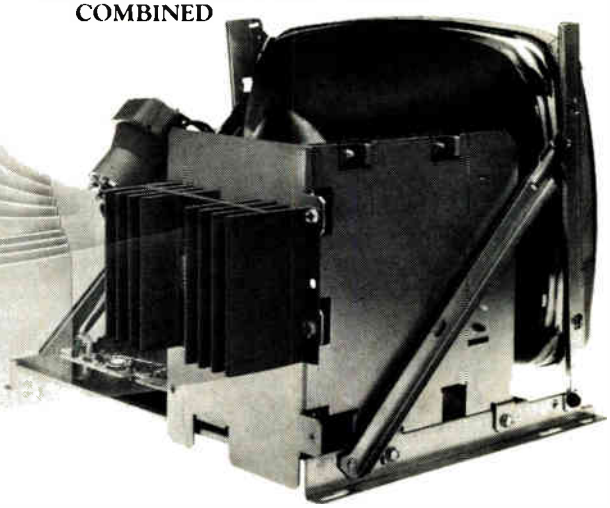


ZENITH®

The quality goes in before the name goes on.

Low-cost generator delivers all standard bit rates

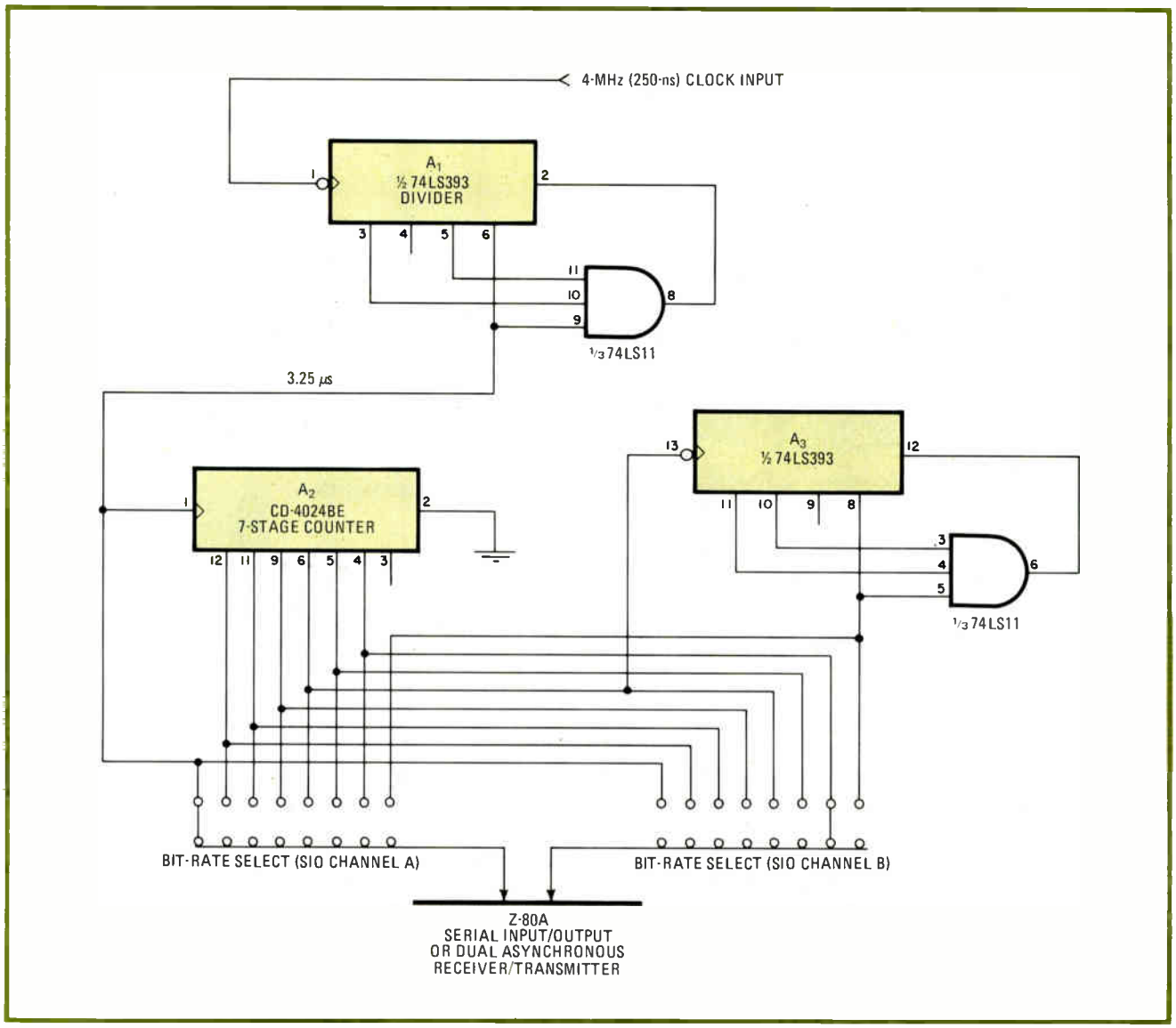
by Robert E. Turner
Martian Technologies, Spring Valley, Calif.

Costing only $2, this generator can drive universal asynchronous receiver-transmitters and other RS-232 serial interface chips at any standard bit rate selected by the user. It is especially suitable for systems based on the Z80 microprocessor from which the generator can derive its 4-megahertz quartz-crystal time base.

As the figure shows, a 4-MHz input clock is divided by 13 by the 74LS393 counter (A_1) and a 74LS11 AND gate, thereby providing a 3.25-microsecond signal that is suitable for driving the CD4024 seven-stage counter, A_2. This signal is close to 16 times the maximum 19.2-kilobit/s output frequency. Smaller divisions are handled by the counter, which supplies 9,600-, 4,800-, 2,400-, 1,200-, 600-, 300-, 150-, and 110-b/s outputs.

The counter outputs are wired so that a bit rate may be selected for both channels of a Z80A serial input/output module or dual asynchronous receiver-transmitter serial interface chip. The output frequency of the generator is 16 times greater than the bit rate, so each serial data bit is sampled 16 times per bit period.

The bit-rate clock frequency is selected with either



Trimmed taps. With a Z80 system clock trimming costs to $2, the four-chip generator delivers all standard bit rates for RS-232–based systems. The generated rate accuracy is high (see table). The system can be easily modified for older interfaces.

GENERATOR RESPONSE			
Period	Actual output (b/s)	Ideal output (b/s)	Error
52 μs	19,230.76	19,200	+0.16%
104 μs	9,615.38	9,600	+0.16%
208 μs	4,807.69	4,800	+0.16%
416 μs	2,403.84	2,400	+0.16%
832 μs	1,201.92	1,200	+0.16%
1.66 ms	600.96	600	+0.16%
3.33 ms	300.48	300	+0.16%
6.65 ms	150.24*	150	+0.16%
9.15 ms	109.26	110	−0.68%

*OUTPUT AVAILABLE, BUT NOT CONNECTED IN CIRCUIT SHOWN

printed-circuit–board jumpers or by small dual–in-line–packaged switches. The entire circuit is small enough to be mounted next to the Z80's DB-25 connectors that are mounted on its rear panel, making it easy for the end user of the RS-232 interface to select a bit rate. The dual-channel version of the circuit requires only five interface lines: the 4-MHz clock input, bit-rate clock A and B outputs, the 5-volt line, and logic ground.

As for the accuracy of the rates generated, they are well within the 1% timing variation standard required by the RS-232 interface (see table). The generator has been used with many different terminals and printers, and no operating difficulties have been encountered.

The circuit may also be used with most of the older serial interface chips like the 8251 and the 6850, if the user is willing to sacrifice the 19.2-kb/s output. In this case, the divide-by-11 counter would be driven by a 2-MHz clock, with the highest bit rate available becoming 9.6-kb/s. This signal drives the counter. The output of the counter that divides the 110-b/s signal by 11 (counter A_3) would then be connected to the new 1,200-b/s output of the seven-stage counter. □

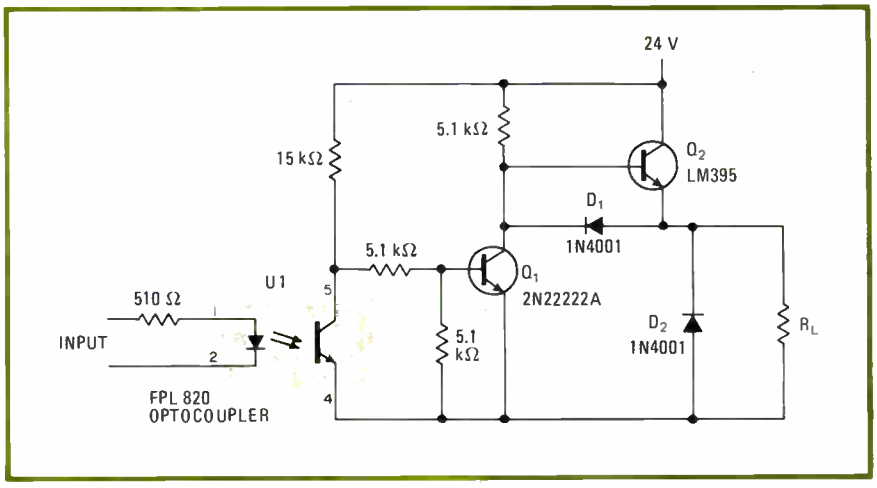
Improving the LM395 for low-level switching

by Yehuda Gabay
Israel Atomic Energy Commission, Beersheba, Israel

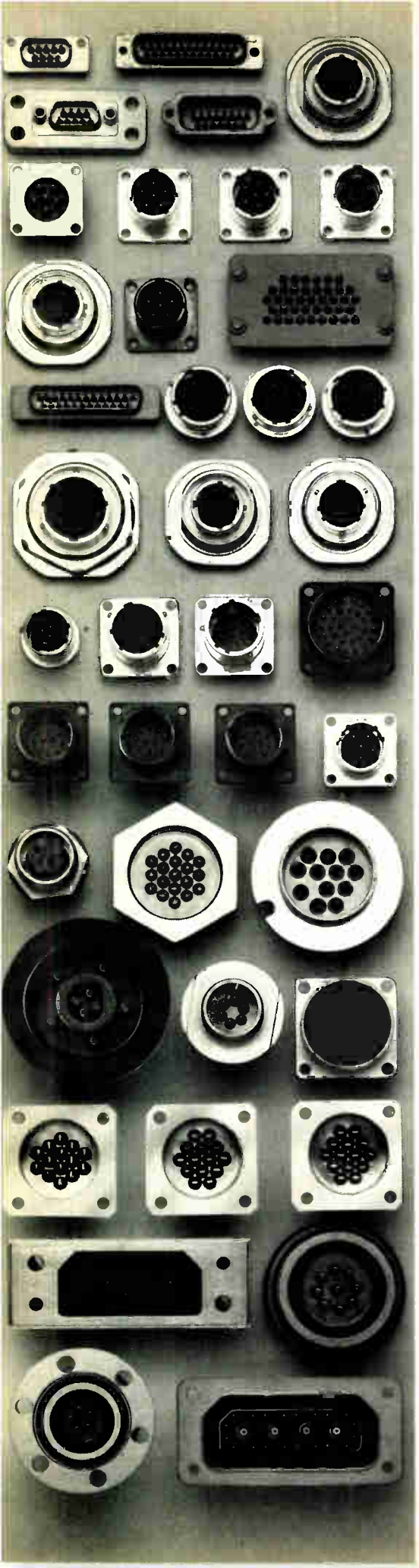
The most significant drawback of a power transistor like National Semiconductor's LM395 is its relatively high quiescent current (10 milliamperes or so), which makes it impossible to use as a reliable switching device for small loads or loads that require dynamic currents ranging from zero to some high value. Adding a transistor-diode network and an optocoupler to the circuit, however, adapts the LM395 as a low-level (down to 0-mA) switch without sacrificing the current-handling capabilities of the power transistor and provides input-to-output isolation as well.

This circuit is configured as a normally-off switch whose quiescent load voltage is a maximum of 0.6 volt. Placing a logic 1 at the input of optocoupler U_1 causes transistor Q_1 to turn off. Thus the power transistor, Q_2, conducts and the desired current flows through the load, R_L.

If the input to the optocoupler goes to a logic 0, Q_2 cuts off and no current flows through the load. In this state, Q_1 conducts and the quiescent current of Q_2 that must flow is shunted through diode D_1 and through Q_1 to



Bypass. A floating switch in the form of an optocoupler adapts power transistor Q_2 for handling small load currents, directing transistor Q_1 to bypass Q_2's high quiescent current (10 mA) when a logic 0 is applied to the circuit input. If a normally on switch is desired, Q_1 and its associated circuitry need only be removed. U_1's output transistor then will take Q_2's quiescent current to ground.



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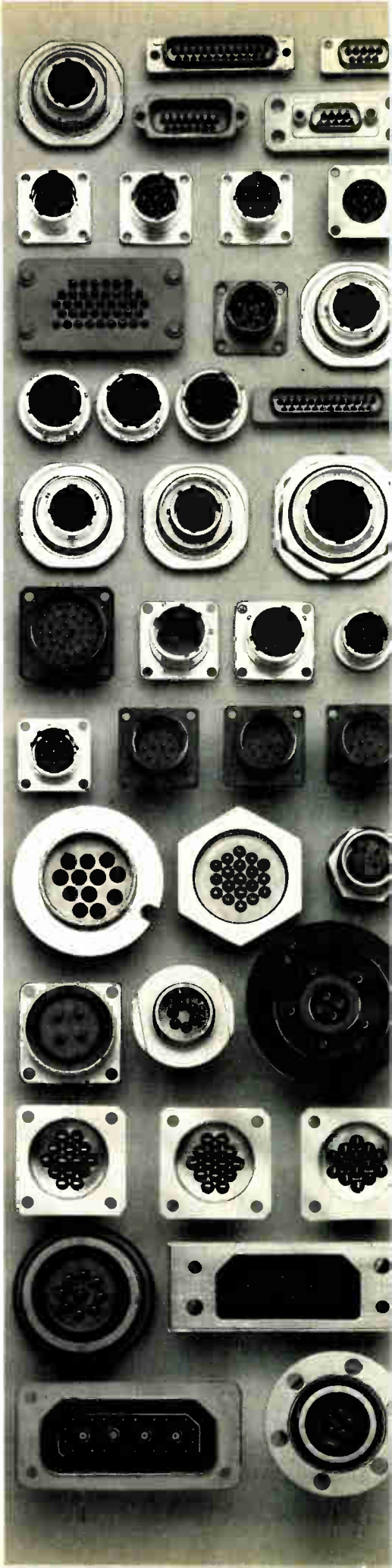


ground. It should be noted that D_2 bypasses transients to ground that are caused by an inductive load.

In the case where the user desires to implement a normally closed switch, it is only necessary to remove the circuitry centered around Q_1. Then, U_1's output transistor will serve to bypass Q_2's quiescent current to ground when necessary. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $75 for each item published.

Low-cost controller stabilizes heater-type cryostats

by S. K. Paghdar, K. J. Menon, R. Nagarajan, and J. Srivastava, *Tata Institute of Fundamental Research, Bombay, India*

Controllers for maintaining small objects at a low temperature use either complicated gas-flow techniques, that regulate gas pressure or costly commercial units that are built for general applications and must be modified to suit a particular need. Finger-type cryostats, in contrast, which control a heater on the principle of error-sensing and feedback techniques, are extremely simple, easy to implement, and inexpensive. As for stability, this circuit holds the temperature to ±0.2 K over 24 hours (short-term variation is ±0.01 K) in the range of 80 to 200 K.

As shown in the figure, the circuit may be built around an OC23 or other power transistor, that has a fairly linear base-current–to–collector-current characteristic, eliminating the need for the additional amplification usual in circuits of this type. Error signals from a Wheatstone bridge are applied to the 741 operational amplifier act as the temperature control. The signal is then amplified by transistor Q_1 and passes to Q_2, which drives a resistive load and associated container that, placed inside the liquid-nitrogen–filled cryostat, heats the environment.

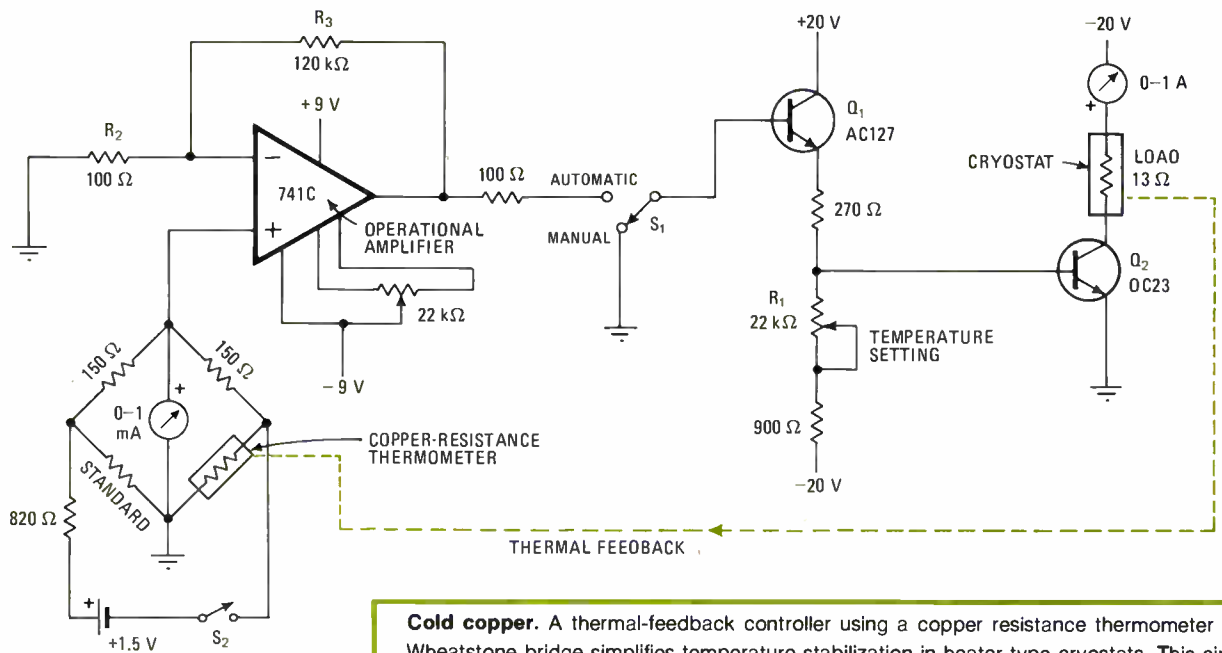
Thermal changes are sensed by a copper resistance thermometer, also located inside the cryostat. This element, placed in one arm of the Wheatstone bridge, reflects changes in the equilibrium temperature between the container and environment and in effect acts to cancel the original error signal applied to the op amp.

This part of the circuit serves only to correct temperature variations and does not set the temperature of the cryostat. Potentiometer R_1 fulfills this task by setting the bias current at the output without affecting the base-driving circuit of the power transistor.

To calibrate the system, switch S_1 is placed in the manual position and R_1 adjusted to obtain the desired cryostat temperature. Next, the Wheatstone bridge should be balanced by adjusting the standard resistor, whose value will be determined by the center value of the circuit's copper resistance thermometer.

The gain of the amplifier stage, R_3/R_2, should be matched to the response of the cryostat. A nominal value might be 1,200, as in this circuit.

The system can handle heater currents of up to 850 milliamperes. Above this value, however, the current gain of the power transistor begins to fall, so that the circuit will not function effectively in the specified temperature range. □



Cold copper. A thermal-feedback controller using a copper resistance thermometer in a Wheatstone bridge simplifies temperature stabilization in heater-type cryostats. This circuit holds temperatures to within ±0.2 K over 24 hours over the range of 80 to 220 K.

Memory management chip extends reach of 8-bit processors

As well as boosting address limits to 2 megabytes, the MC6829 eases the handling of multiple tasks by providing separate register sets for users

by Edward J. Rupp, *Motorola Inc., Austin, Texas*

☐ Memory management is making its way into the 8-bit microprocessor world—and small wonder, for its benefits are as attractive here as in the realms of bigger processors. By allowing a larger memory to be divided into many fixed-size pages, a memory management unit can extend an 8-bit system's address limits beyond the bounds of 64-K bytes. The MMU—a subsystem in itself—can also promote the design of multitasking systems by easing control of swapping—the movement of tasks into and out of physical memory.

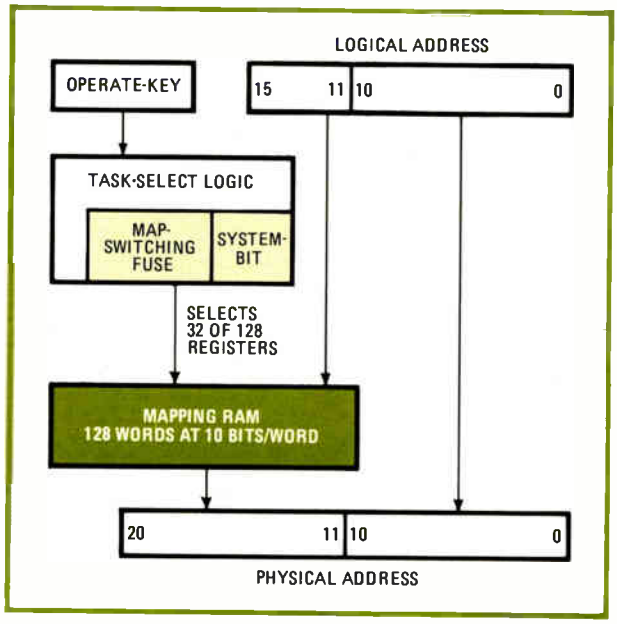
An MMU allows programs to be moved among the system's various types of memory with no need for code changes or even for program fragments to be in contiguous locations. Different tasks running on the system may all use the same logical addresses in their code, because the part handles the relocation necessary to prevent collisions.

Because it can translate different addresses to the same location, the unit eases sharing expensive peripherals and memory among processors. A shared memory makes economical use of read-only programs like language compilers and helps implement intertask communication via semaphores—flags residing in shared memory that synchronize the message passing.

On the microsystem level, however, a memory management unit built from TTL can become complex beyond the point of diminishing return. So a large-scale integrated-circuit implementation introduces reliability and is a cost-effective companion for a microprocessor. To expand the memory space of 8-bit microprocessors, Motorola has developed an MMU on a chip.

The MC6829 memory management unit is designed to be directly compatible with the MC6809 microprocessor. However, it will work with other 8-bit processors, too. It extends the addressing range of the 6809 to 2 megabytes and allows rapid switching between as many as thirty-two 64-K-byte memory maps.

The 6829 uses a simple paged mapping scheme converting 16-bit logical addresses from the processor into the 21-bit physical addresses delivered to memory (Fig. 1). Of the 16 processor address lines, five are fed directly into the MMU. They are applied to a 32-word mapping random-access memory, and the data outputs of the RAM become the upper bits of the physical address.



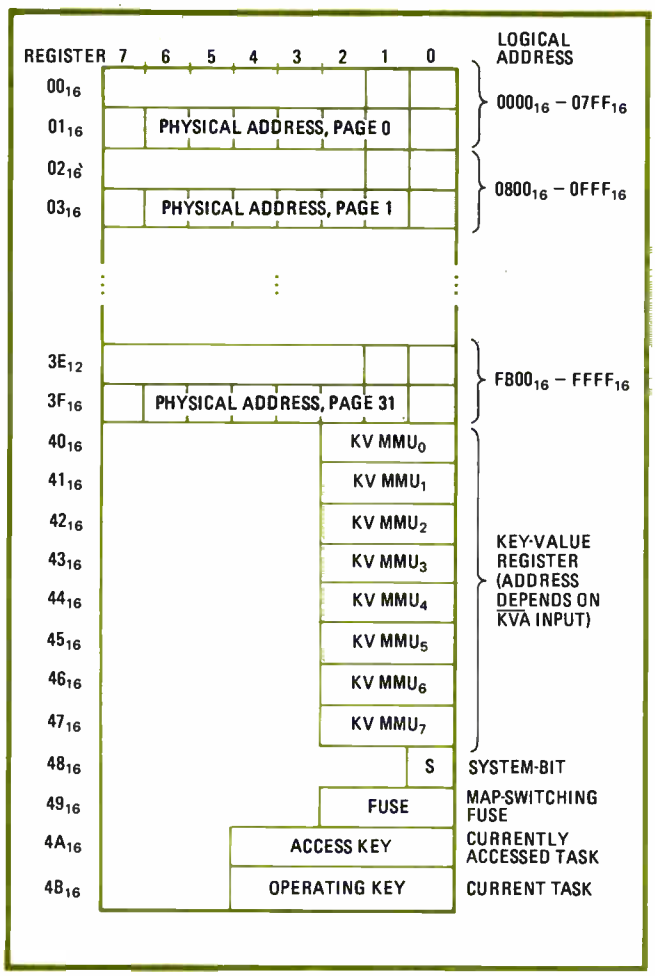
1. The physical translation. A 16-bit logical address is translated into a 21-bit physical address that gives 8-bit microprocessors access to 2 megabytes of memory. One MMU can handle four 64-K-byte tasks organized into thirty-two 2-K-byte pages.

Four groups of 32 mapping registers each are resident on chip, although only one set is active at any one time, as controlled by the operating-key register. Each set is arranged as 32 words of 10 bits each, so that 10 mapped address lines leave the chip.

The 11 unmapped processor lines determine the page size of 2-K bytes. Combining the 6829's 10 output bits with the 11 unmapped bits gives a total of 21 address lines for the address range of 2 megabytes. It takes 110 nanoseconds to translate a logical address into a physical one.

The chip's resources are devoted to handling large memories in multitask environments—there is no provision for page protection, such as flagging read-only pages and generating traps when a write is attempted. Read-only areas could be created, however, by dedicating one of the upper address bits, like bit 20, to write protection. Also, the 6829 is not designed for transparent page swapping—the programmer must include instructions for loading mapping registers before page access.

The chip does provide a convenient means of setting up and changing the contents of its mapping RAM. In



2. Register access. All the registers on the 6829 memory management unit are mapped into the host microprocessor's address space. The key-value registers differentiate MMUs that are wired in parallel, and the access-key register selects one of four tasks.

effect, it appears as a peripheral to the processor during such operations, specifically as 32 double-byte registers. Each of these registers controls the logical to physical mapping for one 2-K-byte page.

Multiple tasks

For multitasking, each 6829 contains enough mapping RAM to hold the addresses for four complete tasks, each of which may have direct access to up to 64-K bytes of memory on thirty-two 2-K-byte pages. If a task is larger, it can simply revise its memory map periodically, giving indirect access to the entire 2 megabytes. Eight of the chips may be present in any one system, which allows thirty-two 64-K-byte tasks to be maintained in hardware registers. Also, the chips may be wired in parallel, easing the design of a multiple-MMU system (Fig. 2).

If a system needs access only to large amounts of memory, a single chip can handle all accesses, though its mapping registers will need to be reloaded. If the goal is fast switching between many tasks, each of them can be assigned to a separate set of MMU registers in a multiple parallel configuration.

Task switching is accomplished by writing the task number in a special register (the operating-key). If that register's contents match those of the key-value register, then that MMU provides a mapped address; otherwise it stays off the memory address bus. During the power-up sequence, the processor initializes the key-value register for each part with a different value. With the exception of the key-value access pin, then, multiple MMUs may be wired in parallel (Fig. 3).

Task selection is controlled by the operating-key and the system-bit registers working with the bus-available and bus-state inputs. The 6809 generates the BA and BS signals directly, though other microprocessors may be adapted to the 6829 by generating these signals with external logic. The scheme for task switching may also change when using other processors.

Task 0 (usually assigned to implement the operating system) is the only one that has access to the registers on the MMU. This provision ensures that a register like the operating-key cannot be changed while its value is being used by a current task. In most multitasking environments, task 0 will contain the program that controls the mapping for all other tasks and will manage the hardware interrupts as well.

Mapping access

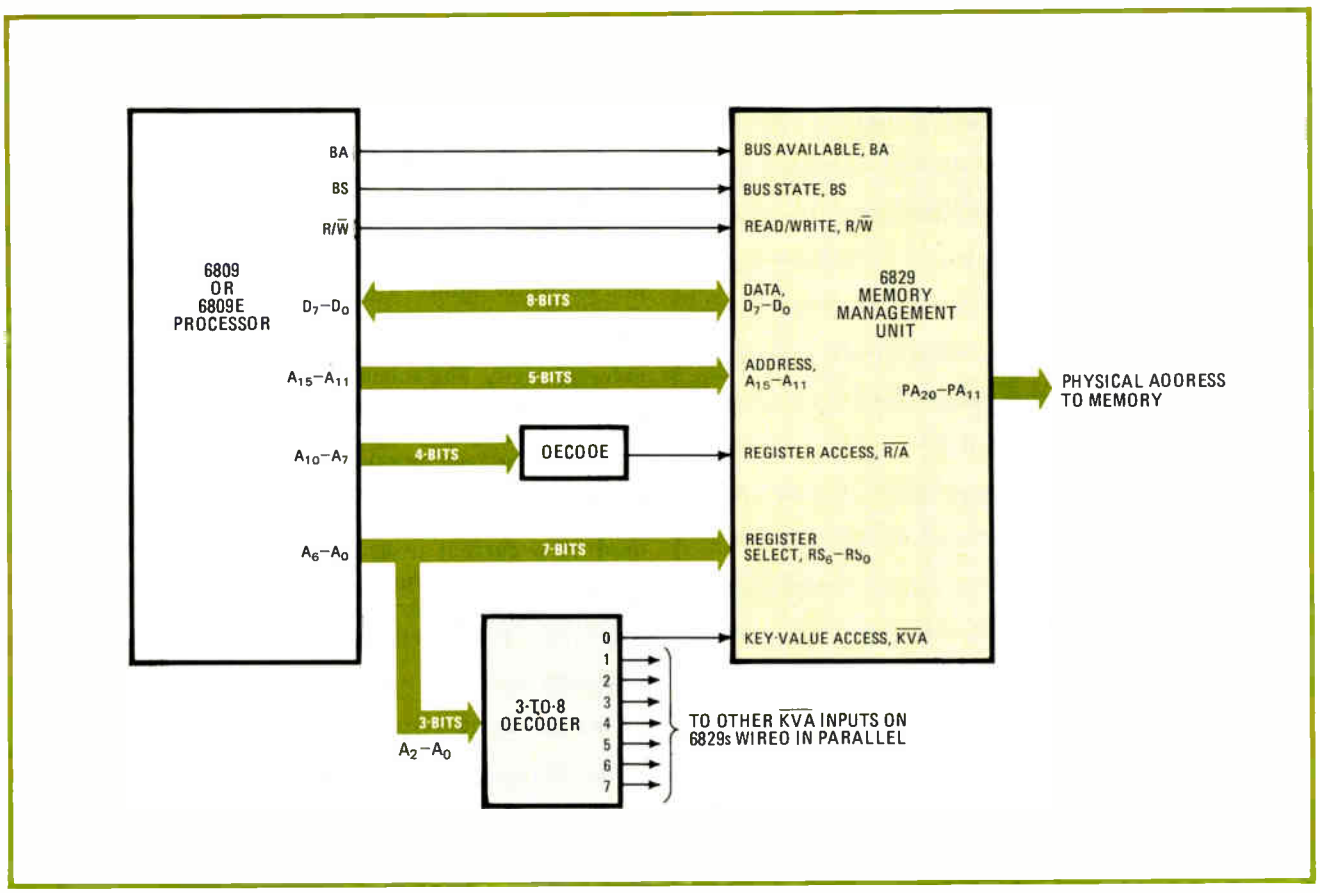
The operating system also must have access to the mapping RAM. To do this it uses the access-key register of the 6829. Writing a task number into the access key causes the contents of the mapping RAM for that task to appear in the first 64 bytes of the 6829's registers. The map may then be examined or changed as needed.

A typical operating system function (system call) is to transfer bytes between tasks, usually between the operating system task and a user task. A subroutine can do this easily by mapping a page of the task 0 map onto the appropriate user task page, with no physical movement of the data. The overhead for large memory transfers is only slightly greater than that of a nonmapped system (about two extra instructions per byte moved).

Software interrupts are an ideal way to handle such system calls because they cause automatic switching to the operating system, which can then perform the requested function and subsequently resume execution of the user task. The return to a task is accomplished by setting the operating-key register to the task number, clearing the system-bit (S-bit) and executing a return-from-interrupt (RTI) instruction (see table).

The S-bit controls the precise moment that the set of 32 mapping registers for a new task is activated. It must be cleared after execution of RTI, which is in task 0's memory and therefore is inaccessible to the new task. Since the instruction to clear the S-bit occurs before RTI, the clearing must be delayed a few cycles so that the processor can have the time to execute that instruction. The 6829 provides this delay with a 3-bit down counter called the fuse register. A value of n written to the fuse will cause an n-cycle delay in clearing the S-bit.

Direct memory access may also use the MMU. This is accomplished when the BA input is high, which temporarily overrides the value in the operating-key register and permits task 1 to be selected for mapping the DMA transfer address. BA = 1 implies that the processor has relinquished the bus to some other controller. By



3. Memory marriage. The processor is married to the memory system by the MMUs. Eight can reside in a single system with all pins (except KVA) wired in parallel. The KVA pin allows a unique value to be written into the key-value register on each chip separately.

switching to task 1 during these operations, the new bus controller has a completely separate 64-K-byte map with which to work.

Thus a DMA controller could transfer up to 64-K bytes without interfering with any other processor operations. Alternatively, parts of task 1 and other user tasks could be mapped together, allowing direct memory access into any task. The fuse register ignores DMA cycles in order to maintain synchronization with the processor.

The mapping delay, called latency, introduced by the MMU adds directly to the cycle time of the processor. The effect of this delay is to reduce the available setup time for the system peripherals and memory. The current design of the 6829 requires 110 ns to complete the mapping function and arbitrate among multiple MMUs.

The mapping starts at the very beginning of each cycle, but arbitration among multiple units cannot occur until one quarter cycle later, since each of them must determine the state of the BA and BS inputs for the cycle. At this point, one of the parts will determine that it must supply a mapped address to the physical address bus and turn on its address lines, with all other MMU output lines remaining disabled.

SUBROUTINE TO SWITCH TASKS

PROGRAM			COMMENTS
RETURN	ORCC	#I + F	disable interrupts (enter critical section)
	STS	OSSP	save current operating-system stack
	LDS	SAVESP	restore user's stack
	LDA	#1	cause map switch one cycle after write
	STA	FUSE	write 1 to fuse register
	RTI		return to user task

Design choices

When building a system with the 6829, a number of choices are possible. One option is to build the system so that each task has its own set of MMU registers. This is probably the fastest and easiest approach, but it does limit the number of tasks that may be running on the system to a maximum of 32.

Another approach is to use a single 6829 and reload its registers at each task switch. This scheme uses task 0 as the operating system task, task 1 as the DMA map (if needed), and tasks 2 and 3 as the sites of the maps for the user task. The maps for the remaining tasks would be kept in memory and loaded as needed. Any number of tasks may be supported with this method. However, the overhead of reloading registers makes this approach relatively slow.

Alternatively, the designer could use multiple 6829s, treating their registers as a resource to be allocated among the tasks. When a task is ready to run, a free set of MMU registers is allocated and initialized for it. High-priority tasks could then remain in the registers, with little used tasks in external memory. □

Leadless carriers, components increase board density by 6:1

Vapor-phase–soldered components withstand military environments, decrease assembly costs

by P. R. Jones, *Rockwell International Corp., Collins Telecommunications Products Division, Cedar Rapids, Iowa*

☐ Possibly nowhere is the need for high packaging density felt so keenly as in the design of avionics equipment. Yet the seemingly obvious routes—large-scale integration or hybrid circuitry—are not always practical for this application. LSI is not cost-effective for systems whose yearly production volumes rarely exceed 1,000 and can fall as low as 50, while ceramic substrates are often unsuitable at the very high and ultrahigh frequencies and the analog power levels that are characteristic of communications equipment.

Printed-circuit boards, however, can be made to achieve six times their usual packaging density if leadless chip-carriers and leadless passive components replace the dual in-line packages and leaded resistors and capacitors in widespread use today. Figure 1 shows just such a pc board using surface-mounted leadless components.

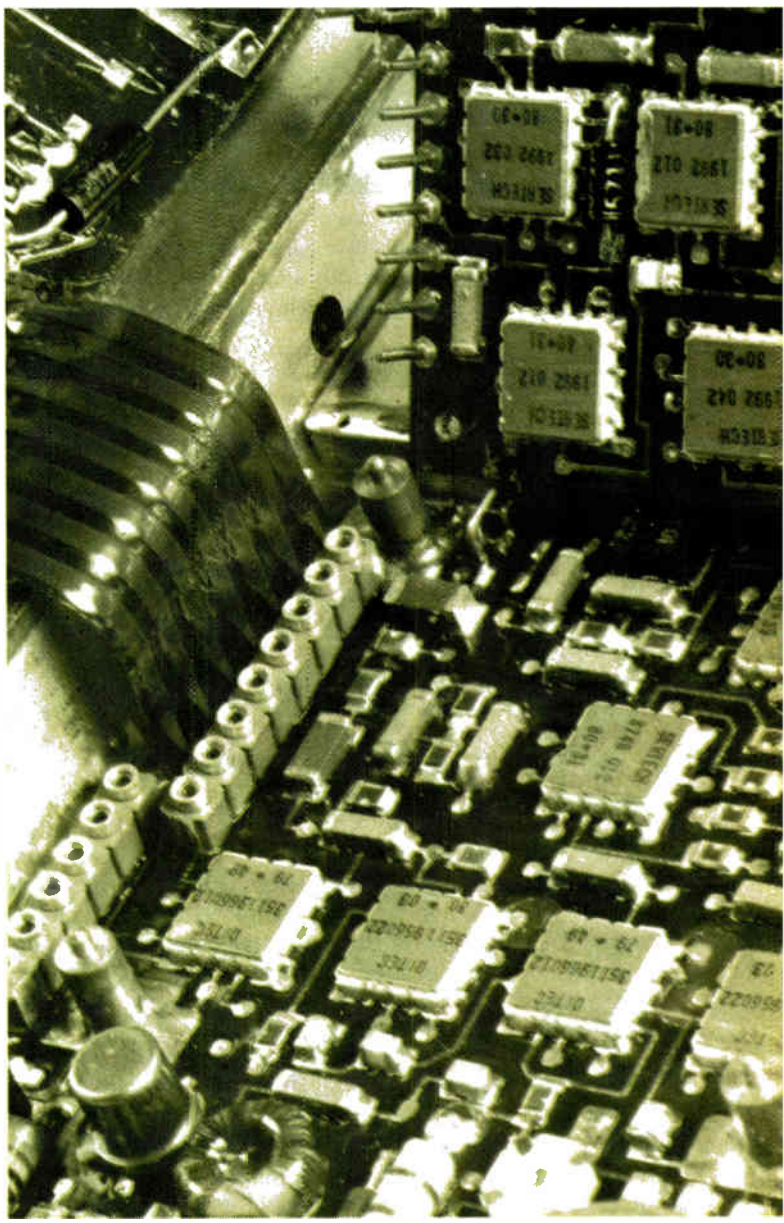
This board far exceeds the original goal—a four-to-one increase in density—set before the advanced technology and engineering department of Collins Telecommunications Products division when it was assigned the task of developing a more cost-effective method of manufacturing more reliable and more complex systems. Other significant advantages of this chip-carrier approach are, in fact:

- Reduced assembly costs, because the circuit boards used are fewer in number and less complex.
- Greater reliability, because each board has only one or two layers and few plated through-holes.
- More compact assemblies, and hence shorter circuit paths, because component height is reduced to as little as 0.08 inch above the board.
- Twice the resistance to vibration of conventional circuit boards.
- Greater ability to dissipate heat, because the boards can be constructed with a very smooth back side that it is easy to laminate to a metal plate.

In the beginning

As its first step in increasing the packaging density of pc boards, the high-density project team at the Collins department focused on the use of leadless passive components. It began by adapting selected circuit boards to use with leadless components, wherever possible using commercially available chip resistors and capacitors.

One of the keys to the high-density project's success



1. Carriers to boards. This is part of the ARC-182 multimode military aircraft transceiver frequency synthesizer showing leadless chip-carriers applied to a polyimide-glass board. Conventional and leadless components form an optimum cost-versus-density solution.

2. Vapor-phase soldering. One of the keys to successful mounting of leadless chip-carriers and other leadless components on standard pc-board surfaces is vapor-phase soldering. In this operation, all solder joints are fused simultaneously in an oxygen-free environment.

was vapor-phase reflow soldering. This process involves heating the entire circuit board, with the components in place, in a vented container. The heat-transfer medium is the dense saturated vapor created by a fluorochemical liquid heated to its boiling point—215°C, in the case of Fluoronert Liquid FC-70, the vapor-phase soldering fluid with which 3M Co. pioneered the method. No complex temperature-control systems are needed, and an air-free environment eliminates the development of oxides (Fig. 2). The procedure heats all board elements to precisely the same temperature, can be carried out either manually or automatically, and uses either preformed solder elements or a paste alloy that is screened onto pc-board traces. The Collins team opted for a paste formulated to have a tacky surface that grips and holds components prior to soldering.

Heat-resistant

During the research and development phase, the team found that about 85% of all military-standard components could withstand the heat and duration of vapor-phase soldering. Sensitive items and those that contain thermoplastic materials had to be assembled with soft solder after the vapor-phase process.

The project's first phase covered constructing and testing 150 boards employing standard DIPs and leadless ceramic resistors and capacitors. A control group of boards had identical circuitry and pin-outs but used leaded components and conventional assembly methods. All the boards held early designs of circuits intended for the ARC-182 multimode military aircraft transmitter-receiver, which was then under development at the division for the Naval Air Systems Command.

To check out the leadless approach as thoroughly as possible, groups of boards were subjected to a series of tests designed to represent the worst possible combination of environments and conditions. These were decidedly more extreme than the circumstances specified in normal military standards.

The humidity test portion was adapted from MIL STD 810C, method 507.1, with values and calibration in accordance with MIL-C-4566A. Temperature-cycling tests were chosen from those for class 2 equipment in MIL-E-5400R. The vibration procedure followed the reliability development test specified in test level F, MIL STD B (with random in lieu of sinusoidal vibration) for the multimode transceiver project.

In every test procedure the boards carrying the leadless passive components performed as well as or better than standard boards. None of their solder joints broke. They withstood vibration tests with an input of 20 gravities, root mean square, a force that shook the leaded components loose from the conventional pc boards. Moreover, the leadless terminations successfully resisted thermal cycling and humidity exposure well beyond the expected levels.

In sum, then, the first phase of the high-density project proved the concept was viable. However, the use of standard DIPs and some components unavailable in other than a leaded form meant that density had so far been improved only 100%.

A second phase of circuit compression was then attempted in which the DIPs were replaced by the much smaller leadless ceramic chip-carrier. Preliminary design work indicated the latter had three-to-one space advantage over the DIP.

Next phase

During the first phase of the project, there had been no economical and ready source of chip-carriers containing the required ICs (although chip-carriers as such were available). Further, there had been no dependable method of mounting ceramic chip-carriers directly on conventional pc-board pads. But these lacks had been remedied by the start of the second phase of the high-density project, and today a broad range of ICs packaged in ceramic chip-carriers is available from semiconductor manufacturers and custom-packaging firms such as Texas Instruments, Motorola, Harris Semiconductor, Mostek, and Fairchild.

The leadless chip-carriers were mounted on patterns of copper pads, or footprints, on standard polyimide- and epoxy-glass substrates. To attach the carriers to the boards, Alpha Metals Inc.'s 63/37 RMA20 screen-printable solder paste proved to have the thixotropic characteristics, consistency of viscosity over time, drying time, and other properties desired. Thermal-cycling tests revealed that solder-paste formulation and alloy is especially critical in chip-carrier attachment.

The tests deployed in the second phase included the same kind of demanding procedures as the tests in the earlier phase. Four rows of chip-carriers were mounted on a pc board. In the first and third rows they were wired in daisy-chain fashion. To reveal open joints or any build-up in resistance, a 60-milliampere dc test current was applied to the loops and monitored during thermal

cycling. The second and fourth rows were simply checked for mechanical failures—that is, broken joints.

The initial tests used a temperature range of −55° to +120° C in half-hour cycles on 60 epoxy-glass and polyimide-glass boards, bearing various sizes of chip-carriers having anywhere from 16 to 48 input/output pads, as well as copper traces oriented in both axes of the glass substrate weave.

Test results

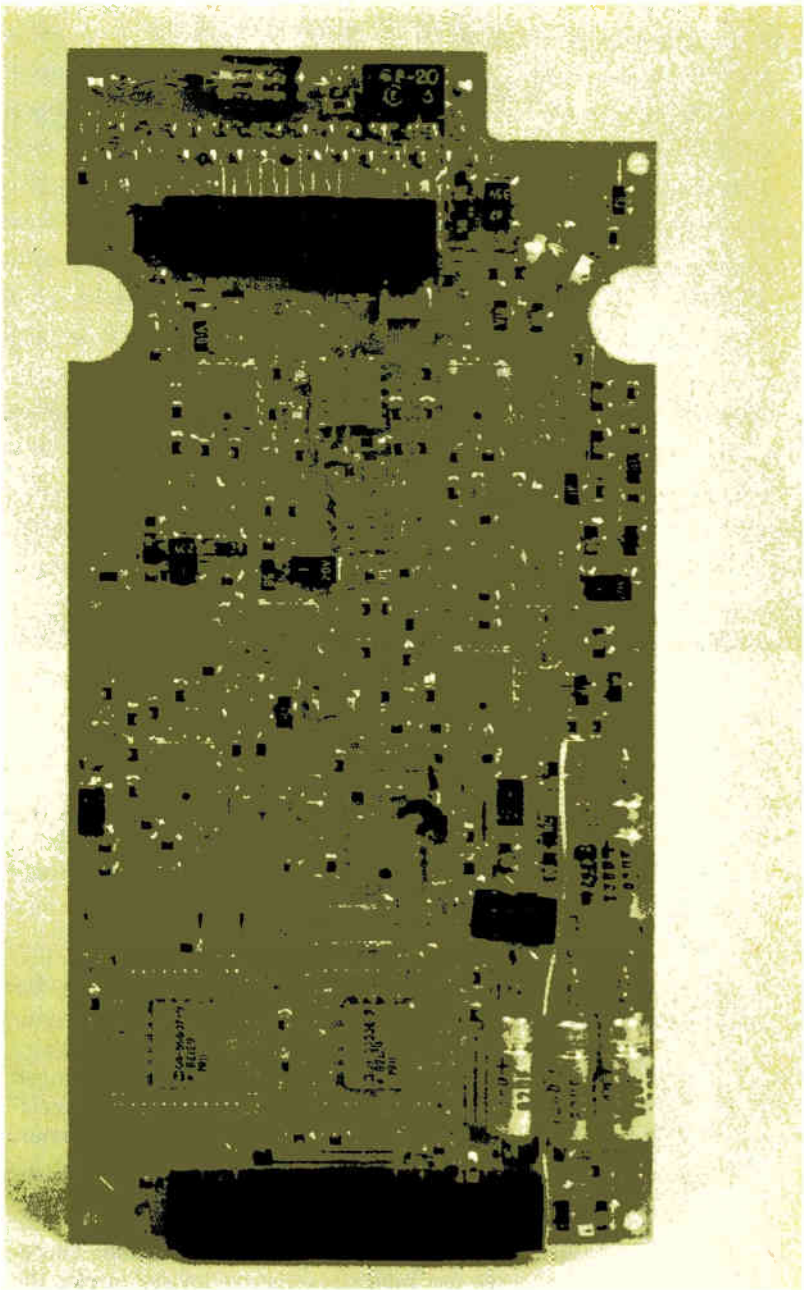
After 1,000 cycles on 20 boards (10 epoxy-glass plus 10 polyimide-glass) there were no fractures in the chip-carrier–to–solder-pad interfaces. However, one failure was caused by the separation of a gold-wire bond inside the carrier.

Also, there were no detectable differences in the test results between the epoxy-glass and polyimide-glass boards regardless of the fiber orientation of the boards. The difference in the thermal coefficients of expansion of the substrates and the ceramic leadless components did not affect the performance and reliability of circuits. (Thermal-shock tests are now a part of the production post-assembly inspection, and indications are that this procedure may be more indicative of future reliability than the conventional time-consuming burn-in method.)

A pilot run of 150 boards showed that the vapor-phase soldering process worked well on epoxy-glass substrates as well as polyimide-glass boards. Polyimide was selected for the ARC-182 multimode military transceiver project, however, because its higher temperature resistance provides a larger margin of safety, or forgiveness, during repair. Also, pads adhere rather better to the polyimide substrate than to an epoxy one.

One side benefit of leadless assemblies is the elimination of lead protrusions on the back of finished pc boards. This smooth surface makes it possible to bond the aircraft transceiver boards to a metal backing for efficient heat transfer.

In such cases, an aluminum backing plate is coated with insulating epoxy and then fastened to the smooth board with a visco-elastic adhesive that improves heat transfer while allowing for differences in thermal expansion and that also damps vibration by as much as 50%. This assembly method makes it possible to maintain a heat differential of approximately 1°C per watt between the component and the external heat sink, even on high–power-dissipation analog circuits.



3. Nested footprints. Nested footprints accommodate the size differences of the various leadless ceramic chip-carriers available from multiple vendors. The unused footprint is selectively masked out with a solder resist in order to keep it free of solder.

Circuit layout

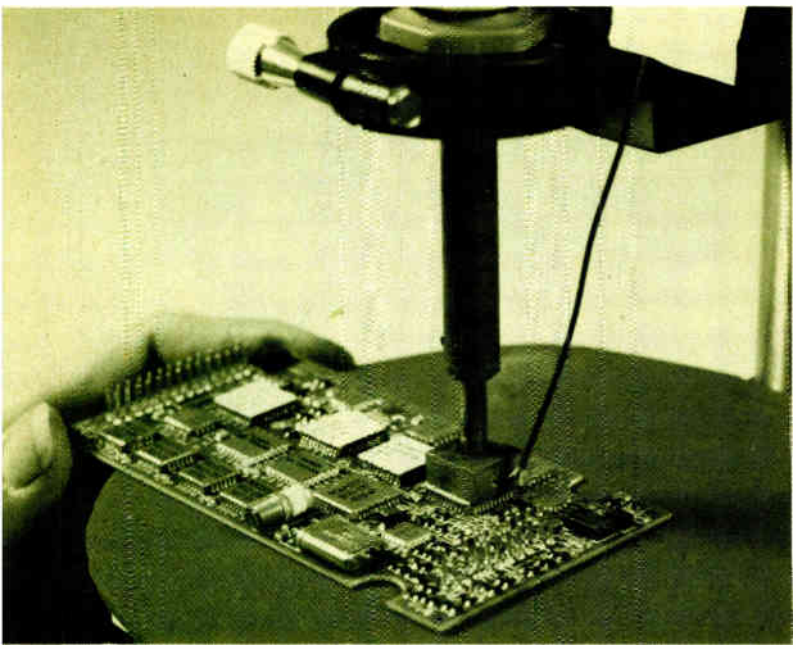
Though the use of leadless devices on pc boards has many packaging and circuit-performance advantages, it also introduces new considerations in design and manufacturing that must be recognized and accommodated.

Circuit-layout procedures and details of the new method turn out to be easier than conventional methods when complex circuitry is involved. Also, the reduction in the number of circuit layers and in the distances between components simplifies circuit drafting.

The Collins division has developed digitized parameters for the footprint of each of the leadless chip-carriers and chip components. Each set of pad patterns is grouped around an X-Y coordinate grid with a specified orientation that is compatible with automatic-assembly and testing equipment. In addition, the digital-parameter program can accommodate changes in industry standards and the emergence of new devices.

The minimum allowance for circuit spacing is 10-mil lines and 10-mil spaces. This layout rule combined with minimum solder-fillet requirements (for inspection purposes) permits the chip-carriers and components to be located within 0.03 in. of one another.

One design element in particular gives the layout designer an extra degree of flexibility. Two different-sized chip-carrier footprints may be centered over the same location as shown in Fig. 3, so that either of two



4. Repairability. A manual soldering device for applying or removing individual chip-carriers has thermocouple wires buried in its tip to monitor its temperature and therefore prevents it from overheating either the lid bond or die attach inside the carrier's case.

sizes of carrier may be assembled, depending on the exact circuit function or part availability. Selective masking of the solder-paste screen over the unused footprint keeps it free of paste and solder buildup.

A solder mask is recommended for most board designs. This mask, whatever the type, should be applied over bare copper only and not over tin-lead plating, for two reasons: the copper prevents the solder paste provided for each chip-carrier contact from being drawn away by the molten tin-lead plating under the solder mask during reflow, and it also prevents the mask material from wrinkling and possibly lifting the chip-carrier, causing open or, at best, poor solder joints.

The standard bed-of-nails board-level test equipment will not work with most of these new boards since there are few, if any, nodal points on a board's bottom. Therefore, alternative test methods must be devised or else the designs modified so as to provide test points. While this is a definite initial barrier to the adoption of this packaging method, the other benefits make the obstacle well worth overcoming.

Other considerations

Another advantage of the approach is the relative ease of chip replacement. With the proper tools, it is possible to remove and replace a leadless chip-carrier much faster than a comparable DIP and with less potential damage to the board. The Collins division has developed a simple and low-cost solder tool with a flat area that contacts the top of a chip-carrier (Fig. 4). The small drill-press–like stand in which it is mounted allows the operator to pull the carrier away evenly without exerting any side force on the ceramic housing. Alternatively, a carrier may be removed by heating its top until the solder melts, and then picking it off the board.

Conversely, the device may be manually attached by placing solder paste on the pads on the board, setting the chip-carrier in place and heating it until the solder flows. When the iron is removed, the chip-carrier automatically centers itself over the pads. This device must be temperature-controlled in order to avoid damage to the chip or chip-carrier.

The purchase prices for leadless components are currently higher than for conventional leaded items (except for chip capacitors, which cost about the same in either form). But this situation is likely to change as the demand for these leadless devices increases.

However, parts-placement labor costs for these new boards are consistently two thirds less than for a standard pc board that is manually assembled. This cost reduction is attributable to the absence of hand soldering steps, lead forming and cutting, and parts insertion. Automated pick and place rates are approximately equal to automatic insertion rates.

This design approach results in yet another important cost reduction—the simplification of pc-board design. Because these boards reduce or eliminate leaded components, there are far fewer plated through-holes to take up space on and complicate pc-board design and construction. Consequently, it is generally possible to reduce the number of board layers and hence board cost.

Reducing the number of plated through-holes improves reliability, and the elimination of board drilling creates additional savings. Where designs must change, it is cheaper to scrap a quantity of single- or double-sided boards than a multilayer inventory. Experience to date shows that the overall pc-board design and production costs for the leadless approach may be as much as 30% lower than for the standard DIP approach. Naturally, the quantity and availability of leadless components affect the resulting costs.

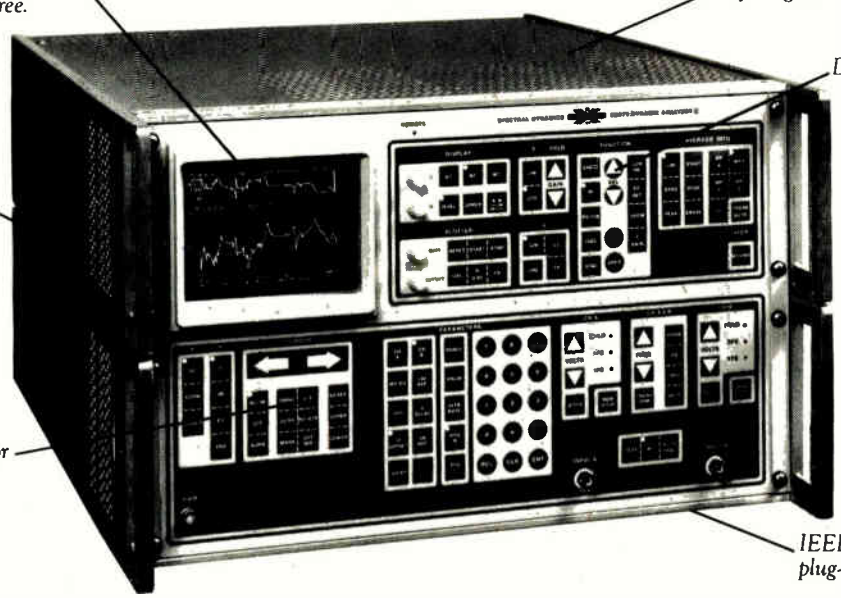
Unshakable attachment

Project testing is an ongoing process and the Collins division has currently completed 4,000 hours of a 10,000-hour temperature- and vibration-test sequence on the ARC-182 multimode military aircraft transceiver to force typical radio-failure modes. These tests reveal workmanship problems, bad joints, and poor workmanship and generally speed the learning curve in manufacturing refinement for a new process.

Currently, the performance of leadless circuits exceeds that of conventional circuitry. For example, the military-aircraft-radio contract calls for a 1,000-hour mean-time-between-failure rating, and the new circuits indicate a calculated rating of 1,900 hours.

The approach has also been shown to work on a commercial system—a compact radio needing the addition of special circuits within an existing housing that was already essentially full. Being nonmilitary, the system had to meet fewer demands in the way of preproduction testing and seemed an ideal candidate for the application of the high-density leadless-package construction method. To hold costs down, standard epoxy-glass boards were used, and tests demonstrated that chip-carriers could be replaced up to 15 times without damage to the copper traces on the board. □

The price of high performance, dual-channel analysis just dropped a few thousand



The Scientific-Atlanta SD375 is not just another new analyzer. It represents a whole new *generation* in spectrum analysis instrumentation.

No other analyzer (not even the highest priced models on the market) can give you comparable capabilities and application flexibility.

In fact, you'd pay *thousands more* to do what our remarkable model does.

Dual microprocessor architecture is the key. It gives the SD375 unmatched flexibility in computing mechanical, structural (including modal), acoustical and electrical/electronic phenomena.

Operating in both frequency and time domains, it processes signals up to 100 KHz. Spectrum analysis is accomplished with 400-line resolution and at eight times the rate of bargain-priced, limited feature analyzers.

QUICK, EASY TEST RESULTS

The SD375 is a "smart" analyzer with flexible, systems-compatible software that helps simplify even the most complex signal-processing problems.

Any of 29 different display modes can be selected through easy-to-read "menus." And up to seven front panel set-ups can be stored and instantly recalled for repeating test sequences.

Test results are shown on the SD375's fully annotated raster-scan video display either in absolute terms (volts, dB, etc.) or in direct-reading engineering units. You save time and effort by avoiding tedious conversions or interpretations.

MORE INTERFACING OPTIONS

The IEEE 488 and RS232C combined interface option provides direct digital compatibility with peripheral test equipment used in larger test systems.

In seconds, its I/O interface parameters can be reprogrammed through a unique I/O menu (on video display), permitting instant bi-directional communication with a wide variety of computers, plotters, calculators and terminals.

Other SD375 options include digital zoom and a noise source, as well as mass data storage, text entry and fully-annotated hard-copy printout.

MORE IS LESS

The SD375 out-performs those slower, 25 KHz analyzers with only 125-line resolution. And it offers sophisticated analysis capabilities that the highest-priced units can't match.

We'd like a chance to prove the SD375's cost effectiveness and capabilities with a short demonstration, or a side-by-side comparison with any other dual-channel analyzer on the market today.

Clip the coupon below for more information and a demonstration. Or call Roger Koch at (714) 268-7129.

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☐ Please send me more information on the SD375 Dual-Channel Analyzer.
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Circle 141 on reader service card 141

Audio-visual controller synchronizes museum display

by William S. Wagner
Northern Kentucky Unversity, Highland Heights, Ky.

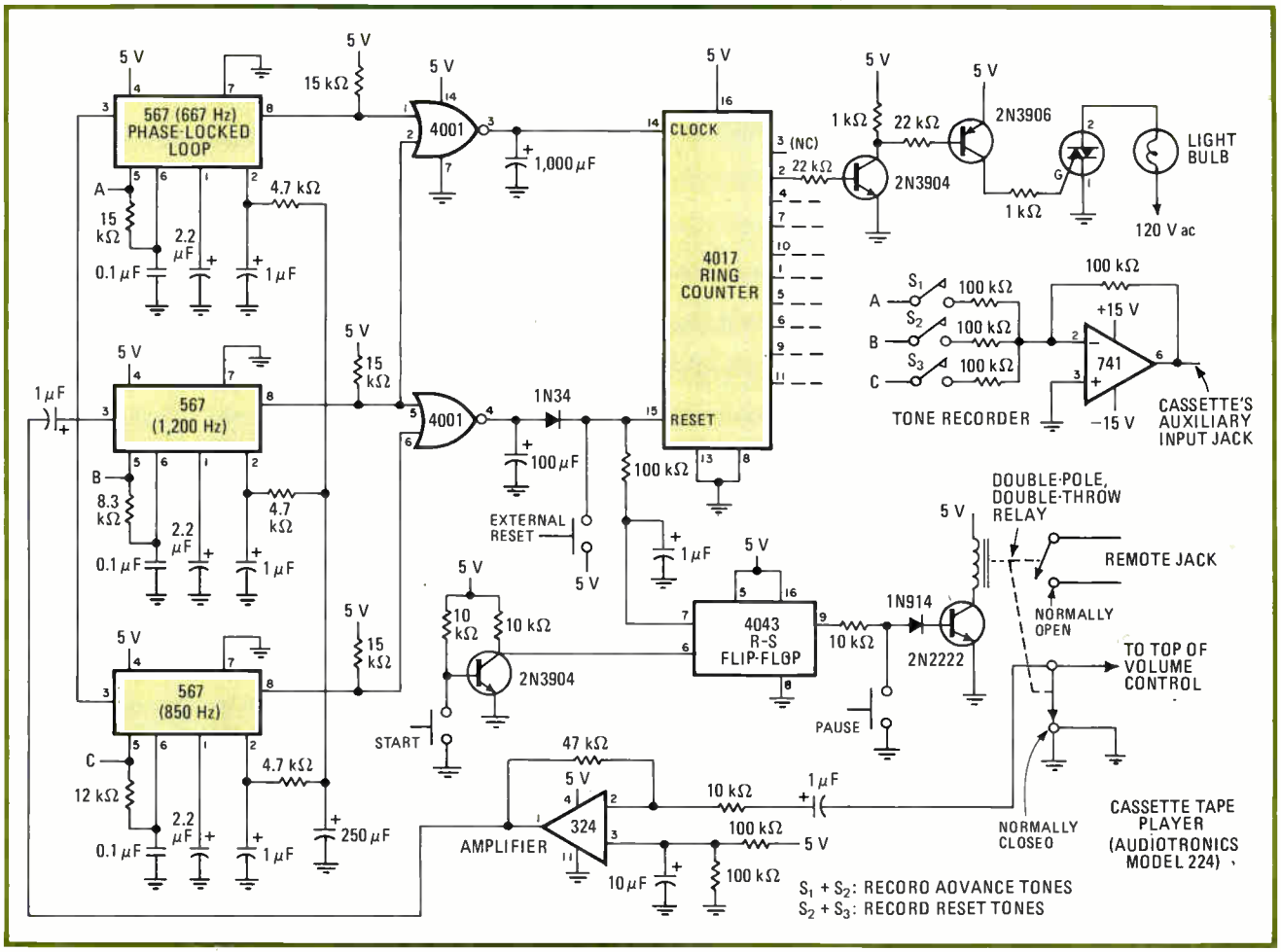
A synchronized sound-and-transparency show that may be placed in any convenient area of a museum or science building can be created with this interface. Built entirely with off-the-shelf components, the cost of the circuit is below $20.

The interface controls a cassette player and a display having several illuminated panels. Each panel contains a color transparency and a source of light (in this case, a light bulb). The circuit causes these transparencies to light in sequence, while advancing the cassette tape, which contains a recorded message for each panel. Pairs of recorded audio tones control panel sequencing and thus synchronize the audio-visual display.

When the show ends, a second pair of audio tones shuts the entire display off. Because a continuous tape loop is used, the show may be restarted by pressing a start button. A pause button is included to extend the viewing period of any panel.

As for circuit operation, when the start button is pressed, the 4043 reset-set flip-flop sets, turning on the 2N2222 transistor and pulling in the double-pole, double-throw relay. Its normally open contact closes, turning on the cassette player's motor. At the same time, the relay's normally closed contact opens, allowing the audio signal to reach the LM324 amplifier. A 667- and a 1,200-hertz tone combine to form the initial sound heard and to activate their respective 567 phase-locked loops. This causes pin 3 of the first 4001 NOR gate to go high and advance the 4017 ring counter.

When pin 2 of the counter goes high, the 2N3904 and 2N3906 transistors turn on and the triac fires, causing the first light bulb to illuminate the first transparency. Then the recorded message corresponding to that trans-



Show and tell. This interface synchronizes sound with illuminated panels and can be used in museum or science building displays. Cassette tapes hold recorded segments corresponding to information seen on illuminated display panels. When the circuit detects a chord preceding a given segment of text, the following panel is illuminated. Also, the interface has an automatic shut-down feature.

parency is played. At the end of the message a second pair of recorded tones (667 and 1,200 Hz) causes the 4017 counter to advance to pin 4, turning off the first light and turning on the second with its appropriate interfacing transistors and triac.

This process is repeated until all transparencies have been displayed and described. At the end of the show, recorded tones at 850 and 1,200 Hz activate their respective PLLs and the 4017 is reset so that all lights are turned off. The 4043 R-S flip-flop is also reset and turns off the 2N2222, which deactivates the relay and turns off the cassette player. □

Making a clock chip keep better time

by M. F. Smith
Department of Computer Science, University of Reading, England

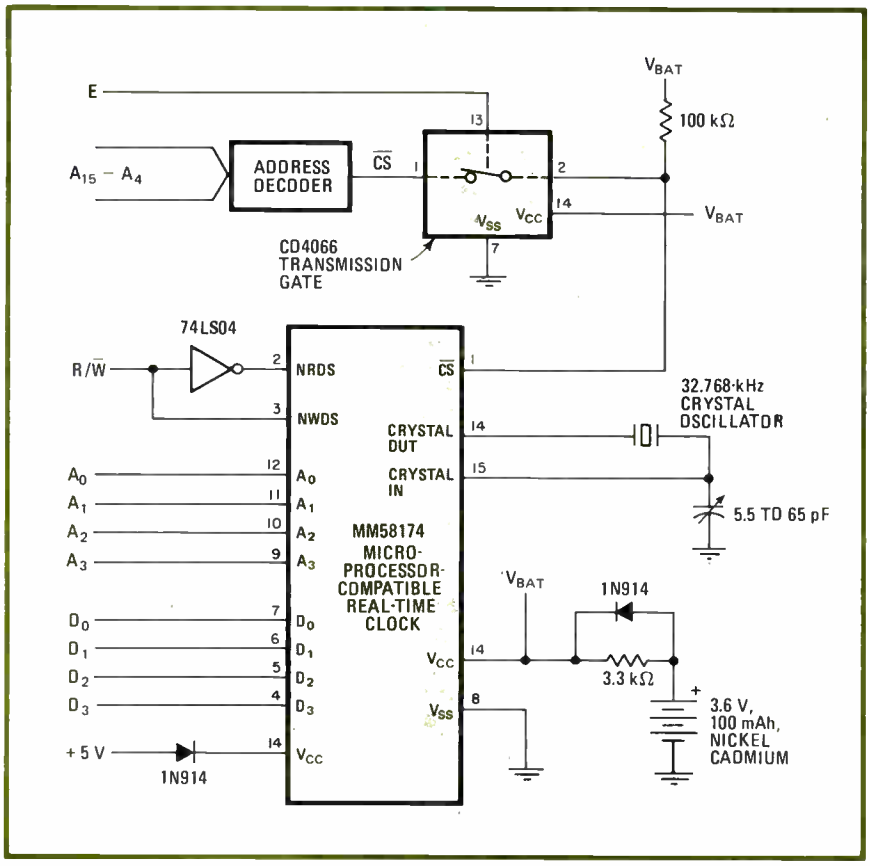
Maintaining both the time and date functions in microprocessor applications became much easier when National's MM58167 and MM58174 microprocessor-compatible real-time clocks were introduced. The software approach that was used before their introduction simplified software and memory requirements, allowed increased flexibility of clock rates and selection of time resolution, and easily accommodated scheduling protocols. However, keeping time during a brown-out was still disastrous to system operation as was attempting to maintain the correct time despite the occasional timing difficulties that occur under software control.

Yet, occasional read errors and problems with spurious writing to the MM58174 when power is going down creates difficulties with the hardware-based system. These difficulties can be overcome with the software and hardware fixes prescribed here, which are intended for the MC6800 microcomputer system.

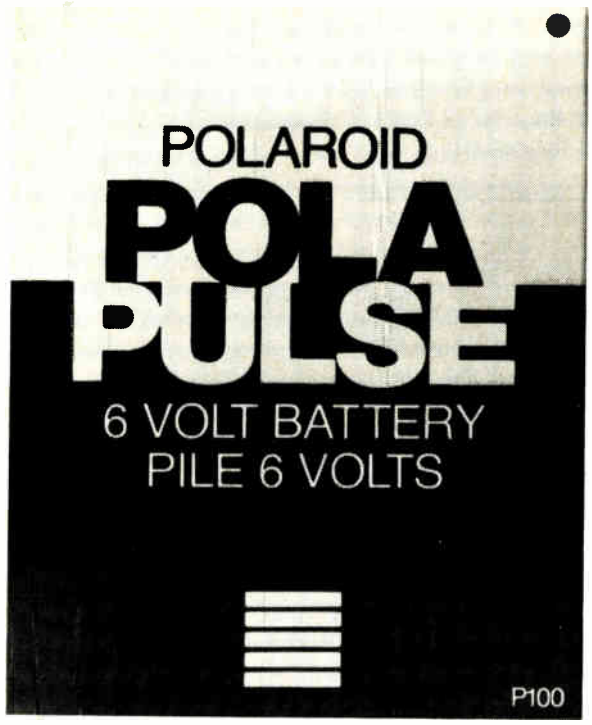
The problem with occasional read errors may be easily overcome by modifying software control to ensure that a valid binary-coded decimal number is read before the program continues and by ordering a rereading of the data if it has not been captured the first time (see printout of the partial listing, line 84). The cause of the read errors has never been definitely ascertained, although the problem has been encountered when other microprocessors have been used, such as National's 1NS8073. Thus, there may be a rare timing problem within the MM58174 itself, or the difficulty may occur between the microprocessor and the clock chip.

Trying to write to the clock chip when the power is going down will ordinarily cause a loss of timing information. A number of methods of preventing the loss were tried, and the one in the figure was the simplest and most successful.

Here, the CD4066 electronic switch will allow the chip to be selected only when the MC6800 clock enables



Glitch-free. The CD4066 transmission gate prevents loss of time-date information that is associated with an MM58174 hardware clock during a power-down condition. Read errors in time-date information may be eliminated in the software of a microprocessor system by writing a loop to ensure the program does not advance until the data has definitely been read correctly.



ACTUAL SIZE

SIDE VIEW

The 6-volt wafer-thin battery that can change the shape of things to come.

We've developed a battery at Polaroid called the Polapulse P100. It's thinner and lighter than any conventional battery we've ever seen.

It can make products thinner, lighter and more compact than if they used conventional batteries. In some cases it can make a product easier to use. It can even help, in some instances, to increase profits.

Less cost, more profit.

For example, take the prototype for a printing calculator.

The Polapulse battery's unique card-in-slot replacement feature requires a one-piece, rather than a three-piece mold, saving 33% of a manufacturer's plastic costs.

With less plastic the calculator is a sleek 6½ x 3⅜ x 1½", weighs only 11.2 ounces, and saves 38% of packaging and shipping costs.

And since Polapulse needs fewer contacts, a manufacturer saves 70% of contact costs.

Equally notable is the particular ability of the Polapulse battery to power a printing calculator's motor with a surge of high current at the beginning of each print. It can then satisfy the high surge demand with low internal resistance and fast voltage recovery.

Heavy duty lightweight.

Design engineers at D.E.I. Teleproducts, a West Coast manufacturer of line drivers, developed test equipment with the Polapulse P100 battery. D.E.I.'s new interface monitor and tester is less bulky and more portable because Polapulse is four times lighter than the conventional power source.

Polapulse has 6 volts of power packed into a one-ounce 3.73 x 3.04" parcel only .18" thick and offers high surge at short pulse. This provides D.E.I.'s new equipment with brighter, easier-to-see LED's.

The interface monitor and tester, only 5¾ x 4⅜ x 1", has a larger face than comparable testers which permits bigger turrets spaced farther apart for easier connections.

Thin battery, wide appeal.

A new slide bolt, door-mounted burglar alarm owes its streamlined 4 x 3¼ x 1⅝", 8-ounce design to the Polapulse battery.

Again, the card-in-slot replacement feature makes an important contribution. The burglar alarm can remain in place at all times. Even when changing batteries.

It is also virtually impossible to short out the battery by accidentally reversing polarity of the contacts. The user does not experience perceived product failure. And, therefore, does not send the product back to the manufacturer for a repair that simply entails proper battery replacement.

Security is a Polapulse battery.

Every Polapulse receives 100% inspection, the sort of inspection reserved for major manufacturers' top-of-the-line power cells. Each Polapulse receives electrical and visual inspection at assembly and again after 60 days of controlled aging.

It also features a unique seal modeled on the Polapulse SX-70 film pack battery which boasts an infallible leakage record—no known leak damage in over 400 million SX-70 film packs.

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Experiment with our Designer's Kit. It contains five Polapulse P100 batteries and a molded battery holder.

Send check or money order for $16.75* (plus applicable taxes) to Polaroid Corp., Commercial Battery Division, Dept. A494, 784 Memorial Drive, Cambridge, Mass. 02139.

For more information about the battery that can change the shape of things to come, call us at (617) 577-4228, or write to the above address.

Polaroid

Our inventions can be your components.

Circle 144 on reader service card

PARTIAL PROGRAM LISTING FOR CONTROL OF MM58167 MICROPROCESSOR-COMPATIBLE REAL-TIME CLOCK

```
Hexadecimal code  Location and label  Mnemonic  Operand          Comments
                  82 HR_MIN_DISPLAY:
004E              83 H_T              LDAA      HOURS_TENS,E     ;GET HOURS FROM CLOCK CHIP
004E B67807       84                  BSR       DIGIT_DISPLAY    ;AND PUT IN BUFFER
0051 8D30         85                  BCS       H_T              ;RETRY IF CLOCK CHIP
0053 25F9         86 H_U              LDAA      HOURS_UNITS,E    ;DOES NOT READ PROPERLY
0055 B67806       87                  BSR       DIGIT_DISPLAY
0058 8D29         88                  BCS       H_U              ;RETRY IF ERROR
005A 25F9         89
005C              90                  LDAA      #":"             DISPLAY COLON
005C 863A         91                  JSR       DISPLAY
005E BD0000       92
0061              93 M_T              LDAA      MINUTES_TENS,E   ;DISPLAY MINUTES
0061 B67805       94                  BSR       DIGIT_DISPLAY
0064 8D1D         95                  BCS       M_T              ;RETRY IF ERROR
0066 25F9         96 M_U              LDAA      MINUTES_UNITS,E
0068 B67804       97                  BSR       DIGIT_DISPLAY
006B 8D16         98                  BCS       M_U
006D 25F9         99
006F              100                 LDAA      #":"             ;DISPLAY COLON
006F 863A         101                 JSR       DISPLAY
0071 BD0000       102
0074              103 S_T             LDAA      SECONDS_TENS,E   ;DISPLAY SECONDS
0074 B67803       104                 BSR       DIGIT_DISPLAY
0077 8D0A         105                 BCS       S_T              ;RETRY IF ERROR
0079 25F9         106 S_U             LDAA      SECONDS_UNITS,E
007B B67802       107                 BSR       DIGIT_DISPLAY
007E 8D03         108                 BCS       S_U              ;RETRY IF ERROR
0080 25F9         109                 RTS
0082 39           110 ;
0083              111 DIGIT_DISPLAY:
0083              112                 ANDA      #0FH             ;MASK OFF TOP PART
0083 840F         113                 CMPA      #9               ;MUST BE A NUMBER
0085 8109         114                 BHI       A_S_ERROR
0087 2207         115                 ADDA      #30H             ;MAKE ASCII
0089 8B30         116                 JSR       DISPLAY          ;AND OUTPUT TO DISPLAY
008B BD0000       117                 CLC                        ;FLAG SUCCESSFUL
008E 0C           118                 RTS
008F 39           119 A_S_ERROR       SEC                        ;FLAG ERROR
0090 0D           120                 RTS
0091 39           121 ;
                  122 ;
0092              123 MO_DISPLAY:
0092              124 D_T             LDAA      DAYS_TENS,E      ;DISPLAY DAYS
0092 B67809       125                 BSR       DIGIT_DISPLAY
0095 8DEC         126                 BCS       D_T              ;RETRY IF CLOCK CHIP
0097 25F9         127                 LDAA      DAYS_UNITS,E     ;READ ERROR
0099 B67808       128                 BSR       DIGIT_DISPLAY
009C 8DE5         129
009E              130                 JSR       DISPLAY_SPACE    ;SEPARATE
009E BD0000       131
00A1              132 MO_T            LDAB      MONTHS_TENS      ;SHOW MONTHS
00A1 F6780C       133                 ANDB      #0FH             ;MASK OFF TOP PART
00A4 C40F         134                 CMPB      #9               ;MUST BE A NUMBER
00A6 C109         135                 BHI       MO_T             ;RETRY IF ERROR
00A8 22F7         136
00AA              137                 CLRA                       ;CONVERT B INTO
00AA 4F           138 QUICK_CNV       TSTB                       ;BINARY OF DECIMAL
00AB 5D           139                 BEQ       MO_U             ;VALUE
00AC 2705         140                 DECB
00AE 5A           141                 ADDA      #10
00AF 8B0A         142                 BRA       QUICK_CNV
00B1 20F8         143
00B3              144 MO_U            LDAB      MONTHS_UNITS
00B3 F6780B       145                 ANDB      #0FH             ;MASK OFF TOP PART
00B6 C40F         146                 CMPB      #9               ;MUST BE A NUMBER
00B8 C109         147                 BHI       MO_U             ;RETRY IF ERROR
00BA 22F7         148
```

it. Once power to the microprocessor begins to fail, the signals from the E line cease and the MM58174 can no longer be selected. The 100-kilohm resistor is required to hold the chip-select line high when the electronic switch is open.

The software for using the hardware clock with the MC6800 is fairly straightforward. However, the program requires a few external routines for accessing the output port and a look-up routine for accessing the month, so that program size will be about the same as for a totally software-based clock. ❑

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.

Engineer's newsletter

Chemical analysis made easy for EEs

At times every electronics engineer needs to know the composition of an ink resin, plastic, adhesive, sealants, or other commercial organic material. But his rudimentary chemistry background rarely equips him for the task. A new series of analytical kits that should ease this situation are now being supplied by Novitex Inc., P. O. Box 6777, San Buenaventura Research Center, Ventura, Calif. 93006.

The kits provide more information than do conventional infrared spectroscopy and complement quantitative methods. The user simply heats a very tiny sample of the test material in a test tube with one or more special reagents and holds a strip of filter paper moistened with other reagents over the mouth of the tube. **Then if a particular color of stain results, a certain chemical monomer or polymer is present.** Among the materials that can be identified are vinyl chloride, acrylonitrile, styrene, epoxies, urethanes, and silicones. Kit prices vary from about $60 to $180, depending on the series of polymers selected.

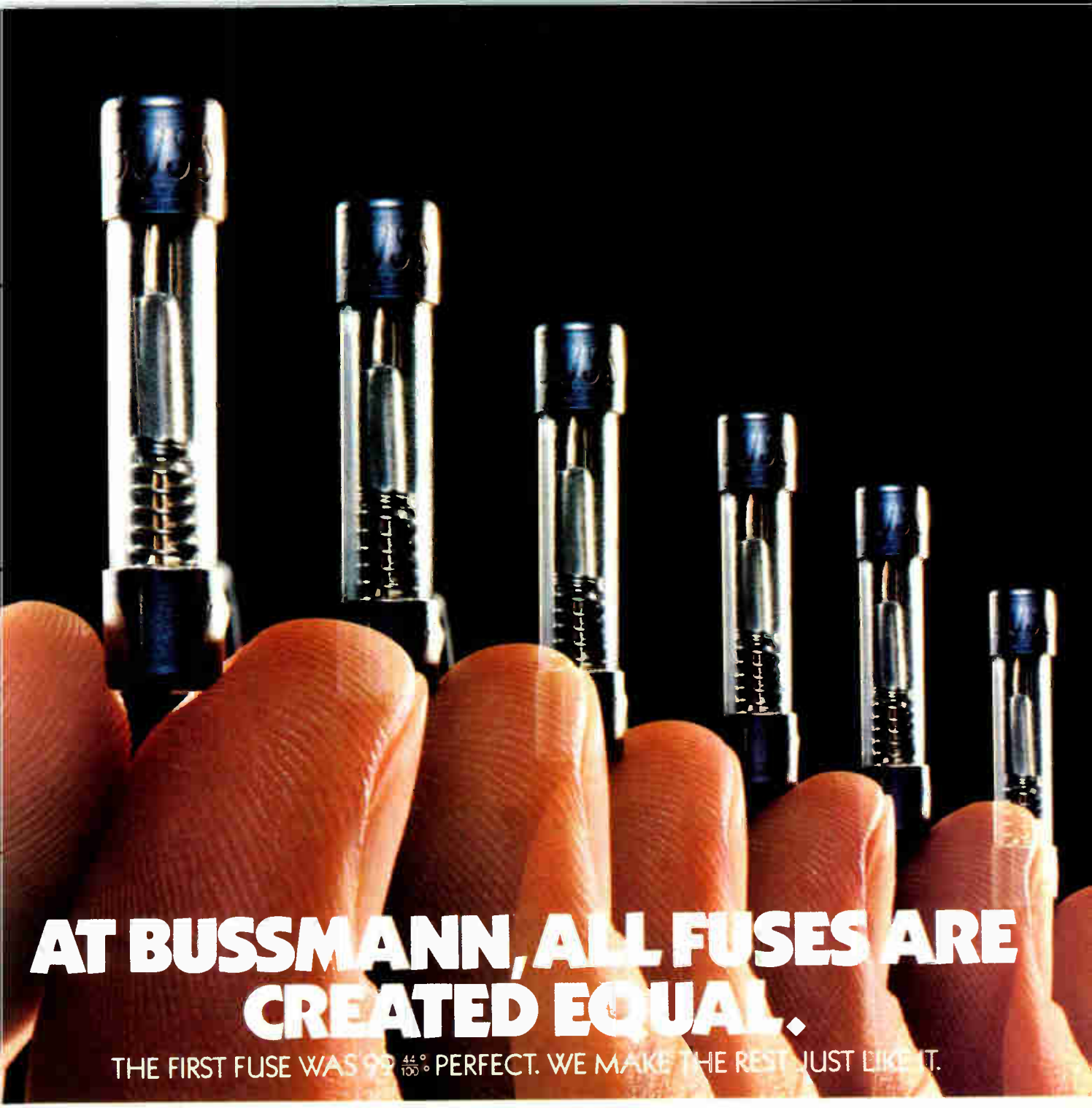
Elastomeric film keeps chips in their place

In hybrid manufacturing, assembly positions normally have cavity trays (sometimes called waffle packs) or flat glass plates carrying arrays of chips that will eventually be attached to hybrid substrates. A different cavity tray is required for each chip size. Because of the clearance required for picking chips out of the cavities, chips can rattle and bounce. In addition, chips can become misoriented, causing problems in automatic assembly. The same sort of problem occurs with the glass trays.

A novel carrier designed by Gel-Pak Chip Carrier Systems, a division of Vichem Corp. in Stanford, Calif., uses a thin film of a Dow Corning silicone rubber to immobilize the delicate electronic chips. In the carrier, a 15-mil-thick film of clear silicone is applied to a flat glass or plastic tray or to the bottom of a snap-lid plastic box. Once a chip is placed on the rubbery surface, **friction between the two surfaces holds it so firmly it will not slip or bounce,** even if the carrier is tilted or jarred. Chips can be removed easily with either tweezers or vacuum collets. Only two film types are needed to handle virtually every device size: one with a smooth silicone surface for small chips and beam-lead devices and the other with a specially treated silicone for large devices. A silicone elastomer was selected for this application because of its durability, transparency, and high temperature resistance.

Where to read up on the reliability of nonelectronic parts

The reliability of electronic equipment is certainly one of the most pressing problems of the 1980s, and of course most of the attention has been focused on semiconductor and passive component reliability. But what about the hundreds of nonelectronic parts in use, such as switches, relays, connectors, integrated-circuit sockets, motors, and so on? The second edition of the Reliability Analysis Center's compilation of analyzed reliability data on nonelectronic parts will soon be issued. This 280-page volume contains the failure rates and failure modes of a wide variety of mechanical, electrical, pneumatic, hydraulic, and rotating parts. It combines a presentation of failure rates at the generic-part level with **detailed line entries representing experience at the equipment level of parts operated in many different field environments.** A copy of NPRD-2 costs $60. It may be ordered directly from Reliability Analysis Center, Griffiss Air Force Base, N. Y. 13441, or by calling (315) 330-4151. **-Jerry Lyman**



Reliability of a Buss® fuse is designed in and built in. We spend a lot to make certain that each one is as good as its near-perfect prototype. It's one of the reasons why Buss is the best-known name on fuses. But there are other reasons.

Like the Buss MDL dual-element fuse (above). It's designed to absorb starting currents up to five times normal for ten seconds without nuisance tripping, yet protect equipment by clearing safely in one-half a wavelength on shorts. And when we manufacture them, we make certain they will do exactly that. By testing each fuse, individually. Random checking is not good enough where circuit protection is concerned.

Bussmann reliability also comes from other things we do: like sophisticated new fuse designs; like our extensive technical literature program; like our traveling fuse seminars; like the industry's largest corps of technical people to help you with applications.

If you are looking for simple, reliable, no-nonsense circuit protection, get Buss and everything that goes with it.

See your Buss distributor for any of our 3,000 electronic fuses, clips, blocks and accessories. See your Buss sales representative for applications assistance. Bussmann Division, McGraw-Edison Company, P.O. Box 14460, St. Louis, Missouri 63178. (314-394-2877)

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The secret behind the new Scotchflex® brand connector is riveting: the cover is locked onto the connector body so it won't come loose.

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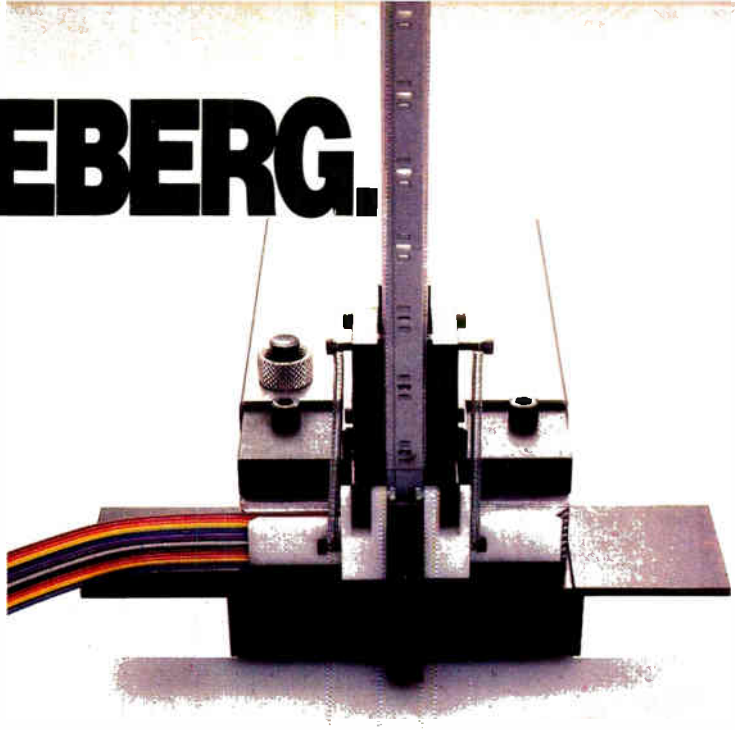
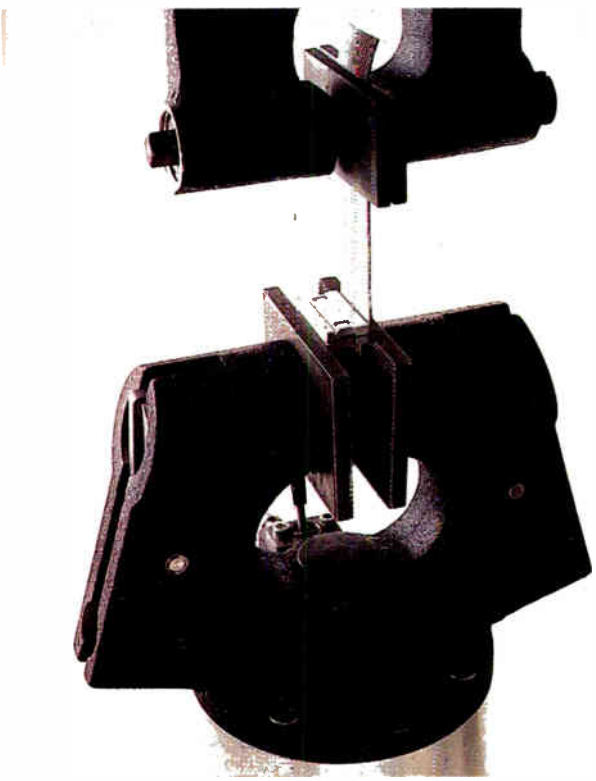
THIS NEW 3M CONNECTOR IS ONLY THE DIP OF THE ICEBERG.

THE ICEBERG.



Now 3M takes you a step beyond pre-assembly, for what we think is the fastest jumper assembly system on record.

It all starts with the special magazine for 14-pin and 16-pin connectors. It comes pre-loaded. Just position the magazine in the new automatic DIP terminator.



Next, cut your cable to length. Insert it into the terminator. Activate the switch. In less time than it takes to tell, your jumper assembly is ready to go.

The system slashes production time by up to 66%; cuts reject rates; delivers every ounce of reliability you demand.

The bottom line: a connector-cable assembly with 16 pounds of retention strength—one of the industry's highest for 14-pin and 16-pin connectors.

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And for a change, more *costs* less, two ways. The DIP has a new, lower price—you get economy from the very first order. And the new terminator lets you boost productivity and cut assembly costs.

So call your 3M distributor for the details, or write Electronic Products Division/3M, 225-4S, 3M Center, St. Paul, MN 55144. You'll see why it pays to Specify the Source.

3M Hears You...

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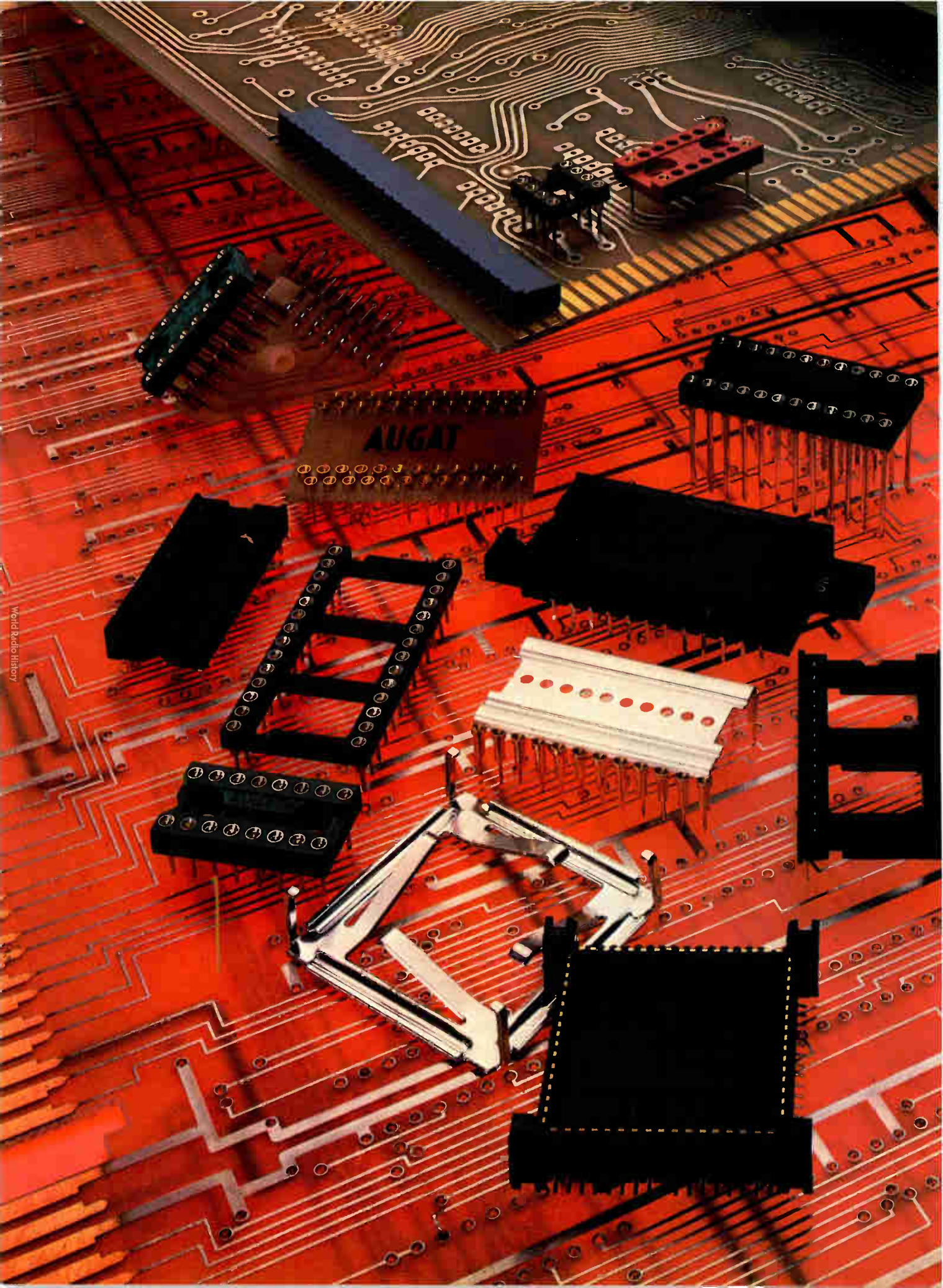
Circle 149 on reader service card



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DEC-C-169
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We change the way the world thinks.

Quest for latest digital technology to draw huge crowd to San Francisco

by Howard Wolff, *Associate Managing Editor*

☐ When Wescon/81 opens its doors in San Francisco's Civic Auditorium and Brooks Hall on Sept. 15, the show that has become the largest electronics exhibition in the U. S. will also be closing out its third decade. And, as has become the custom in recent years, it will be a sellout. Exhibits will overflow the 819 booths those two halls can accommodate into 138 booths at the San Francisco Hilton Hotel—the first time the hotel has been used for Wescon exhibits.

During its three-day stand in the city that likes to call itself America's favorite, Wescon's professional program at the hotel will include 36 sessions. Some 55,000 persons are expected to register, topping the record 53,103 who turned out last year at Anaheim, Calif. (the show alternates between San Francisco and the Los Angeles area). And there will be a "last" at this year's edition—the final Wescon at the Civic Auditorium and Brooks Hall. When it returns to San Francisco in 1983, the show will be housed at the new Moscone Convention Center.

As for the program itself, among the highlights will be sessions on integrated circuits—in general, microprocessors and, in particular, communications. Heavy emphasis will again be placed on digital technology.

Quick work on fast LSI

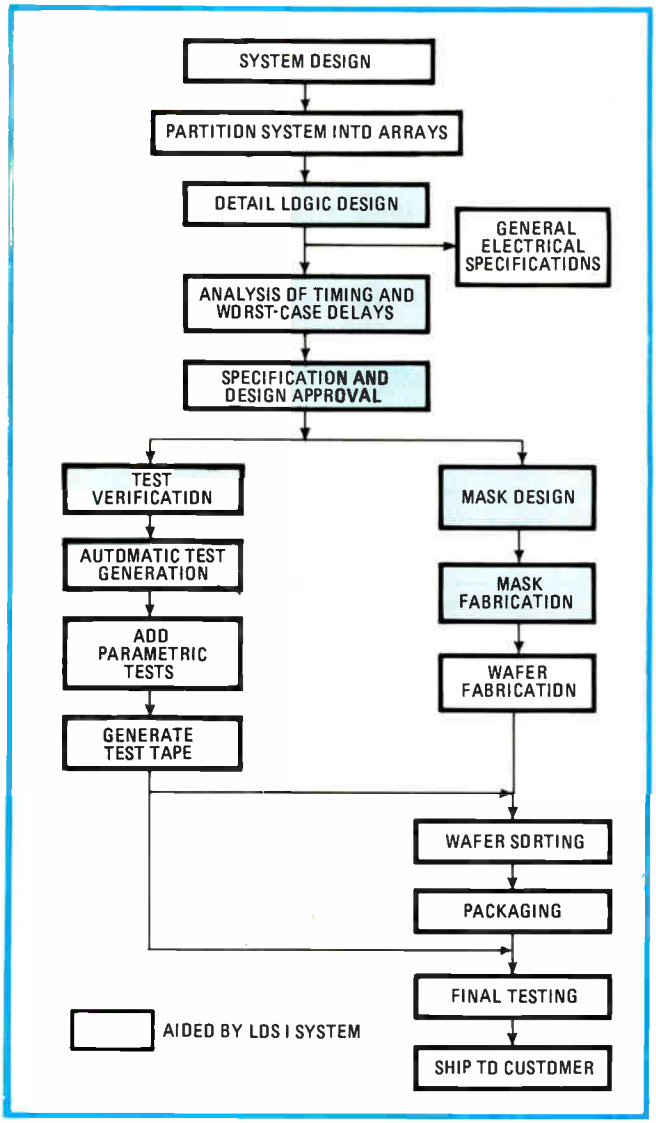
For session 14, on very high-speed large-scale integration, Rob Walker, engineering vice president for the recent start-up company LSI Logic Corp. of Santa Clara, Calif., will bring together speakers from IBM, Motorola, Honeywell, and his own firm to discuss their bipolar

circuit technologies. IBM Corp.'s Hopewell Junction, N. Y., facility will disclose a circuit technique that features the high performance of emitter-coupled logic but with less than TTL power consumption. Motorola Inc. of Mesa, Ariz., and Honeywell Inc.'s Plymouth, Minn., Solid State Electronics division will outline the plans for their ECL and current-mode-logic processes, respectively.

LSI Logic will give a paper entitled "Future Trends in High-Speed LSI and VLSI." The presentation will provide an overview of trends in process, device, and circuit technology, design techniques, and the testing and assembly of semiconductor chips. In addition, LSI Logic will allude to its first product: a gate-array design system called the LDS I (Fig. 1).

The compact LDS I computer-aided design system will automate every step between a customer's logic diagram and mask generation. The system provides for logic checking, circuit simulation, macrocell placement, path timing, and test-program generation. The idea is to allow a system engineer, unfamiliar with gate-array layout and design, to complete a design—regardless of chip technology.

In session 25, on electrically erasable programmable read-only memories, speakers from Intel, Xicor, General Instruments, and Hughes Aircraft will discuss their offerings. There will be some new product introductions. For instance, Intel Corp., in Santa Clara, Calif., is coming out with a slightly different version of its 2-K-by-8-bit EE-PROM that will emphasize block erasure (as opposed to byte and block erasure in its 2816) for a lower cost per bit. In addition, the Hicksville, N. Y.–based General Instrument Corp. may soon supply a metal-nitride-oxide-semiconductor 2-K-by-8 bit EE-PROM intended as a replacement part for Hitachi's 16-K MNOS EE-PROM. Xicor Inc. of Sunnyvale, Calif., will discuss its so-called shadow random-access memories, a device type Hughes Semiconductor in Newport Beach, Calif., is developing in complementary-MOS.



1. CAD takeover. In session 14, "Very High-Speed Digital Large-Scale Integration," LSI Logic will show how its first product, the LSI I gate-array design system, will assist users in the phases of gate-array design and production highlighted in color above.

PALs and PROMs

Programmable-array logic, or PAL chips, plus some of the latest programmable ROMs, will be the subject of session 33, on user-programmable circuits. John Birkner of Monolithic Memories Inc. in Sunnyvale has come up with a development system and a high-level language specifically for PAL devices. Written in Basic and Fortran, the designer enters a logic description and the system verifies the circuit and ultimately programs the PAL chip.

By scaling down geometries, Intel has taken its bipolar fusible-link PROMs to the 32-K density level with an access time of 40 nanoseconds. In Melbourne, Fla., Harris Semiconductor, too, has shrunken its pioneering 4-K C-MOS fusible-link PROMs for two new 16-K parts, organized by 4 and by 8 bits. Interestingly, Intel and now Harris both use polysilicon fuses.

Advanced Micro Devices Inc. of Sunnyvale has engineered a bipolar PROM called a registered PROM that incorporates an output latch for pipelining operations. The latch holds the data referenced during the previous cycles so that subsequent accessing can occur in parallel.

The highlight of the microprocessor sessions will be the ninth—"Virtual Memory Concepts for 16-bit Microprocessors." Details of three new memory management units for the leading 16-bit microprocessors will be revealed for the first time—the iAPX-286 from Intel, the MC68451 from Motorola Inc. in Austin, Texas, and the Z8015 from Zilog Inc. in Cupertino, Calif. Also, National Semiconductor and Texas Instruments will present papers on their approaches.

The 286, due to see silicon early next year, is the only

16-bit microprocessor to employ an on-chip memory management unit. It maintains software compatibility with the 8086 by making the additional circuitry transparent to the user. Its memory-mapping registers are actually widened versions of the segment registers already present on the 8086.

Motorola's 68451 is a companion to its 68000 microprocessor, the 16-bit machine that gets the prize for having the most second sources (six, of which four were announced since last year). This part uses some novel masking techniques to provide user protection and page relocation. It also includes an instruction-abort output for missing page faults. However, this output will not be very useful until the new version of the 68000 that allows instruction restarting comes out next year.

Zilog will discuss its second memory management unit at a time when everyone else is still coming up to speed on a first. Nor is the new one, the Z8015, just a remake of its present Z8010. It is a new design that divides the 8-megabyte address space of the Z8001 microprocessor into 4,096 pages of 2-K bytes each. Thus, users of the Z8001 will be able to choose between a variably-

WESCON/81 TECHNICAL SESSION SCHEDULE

	TUESDAY			WEDNESDAY		
	9:00 – 11:00 a.m.	12:30 – 2:30 p.m.	3:30 – 5:30 p.m.	9:00 – 11:00 a.m.	12:30 – 2:30 p.m.	3:30 – 5:30 p.m.
Signal Processing	Trends in digital signal/array processing	Trends in digitizing signal analyzers				
Design				Very high-speed digital large-scale integration	The outlook for linear ICs in the '80s Transporting high-speed digital signals point-to-point on circuit-board assemblies	
Instrumentation and Test			User friendliness in advanced instrumentation	IC sensors markets, applications, and technologies		Analog-to-digital interface systems
Memories			Virtual memory concepts for 16-bit microprocessors and computers			
Microcomputers	16-bit microcomputer architectures				Single-chip microcomputers, part 1	Single-chip microcomputers, part 2
Microprocessors		Advanced 16-bit peripherals – the family concept		Trends in complementary-MOS microprocessors		
Packaging and Production					Flux residue removal and its impact on quality control and reliability	Advances in leadless chip-carrier packaging and attachment
Telecommunications				Fiber optics today		Mixers for high-performance radio
Speech	Speech technology in the 1980s	Voice processing	Computer-controlled voice message systems and the office of the future			

sized–segment approach to memory management and a fixed-size–paged approach.

For microcomputers, sessions 17 and 21 form a two-part series that focuses on single-chip models. In the first part, the cost-effective use of such devices for system design is the primary concern.

Perhaps the best example of this is seen in the paper in which Peter Brown, an applications engineer at Zilog, describes the design of a general-purpose microcomputer board fabricated with only seven chips, as shown in Fig. 2. Key to this compact configuration is a special micro-computer, the Z8671, which has a Basic interpreter and debugging routines in its 2-K bytes of on-board ROM. In addition, the chip is configured to serially input and output information to a terminal and external memory.

THURSDAY		
9:00 – 11:00 a.m.	12:30 – 2:30 p.m.	3:30 – 5:30 p.m.
Technology to help the handicapped		
Electrically erasable memories provide new system flexibility	Battery backup techniques for memory preservation	
Microcomputer bus structures	Computers for engineering applications	User-programmable circuits
Multitasking operating systems	The expending spectrum of microprocessor peripherals	Standard software for standard microcomputer modules
		Microprocessors in industrial control

High-speed logic on boards

In past years, circuit designers rarely had to contend with routing high-speed digital signals on circuit-board assemblies. Now there is a host of families available. The purpose of session 18 is to give the circuit designer background when digital signals must be transported at high speed through double-sided and multilayer printed-circuit boards or through boards that have been wired by the Wire-Wrap or Multiwire processes. The challenge to the engineer is to preserve signal fidelity while holding down crosstalk.

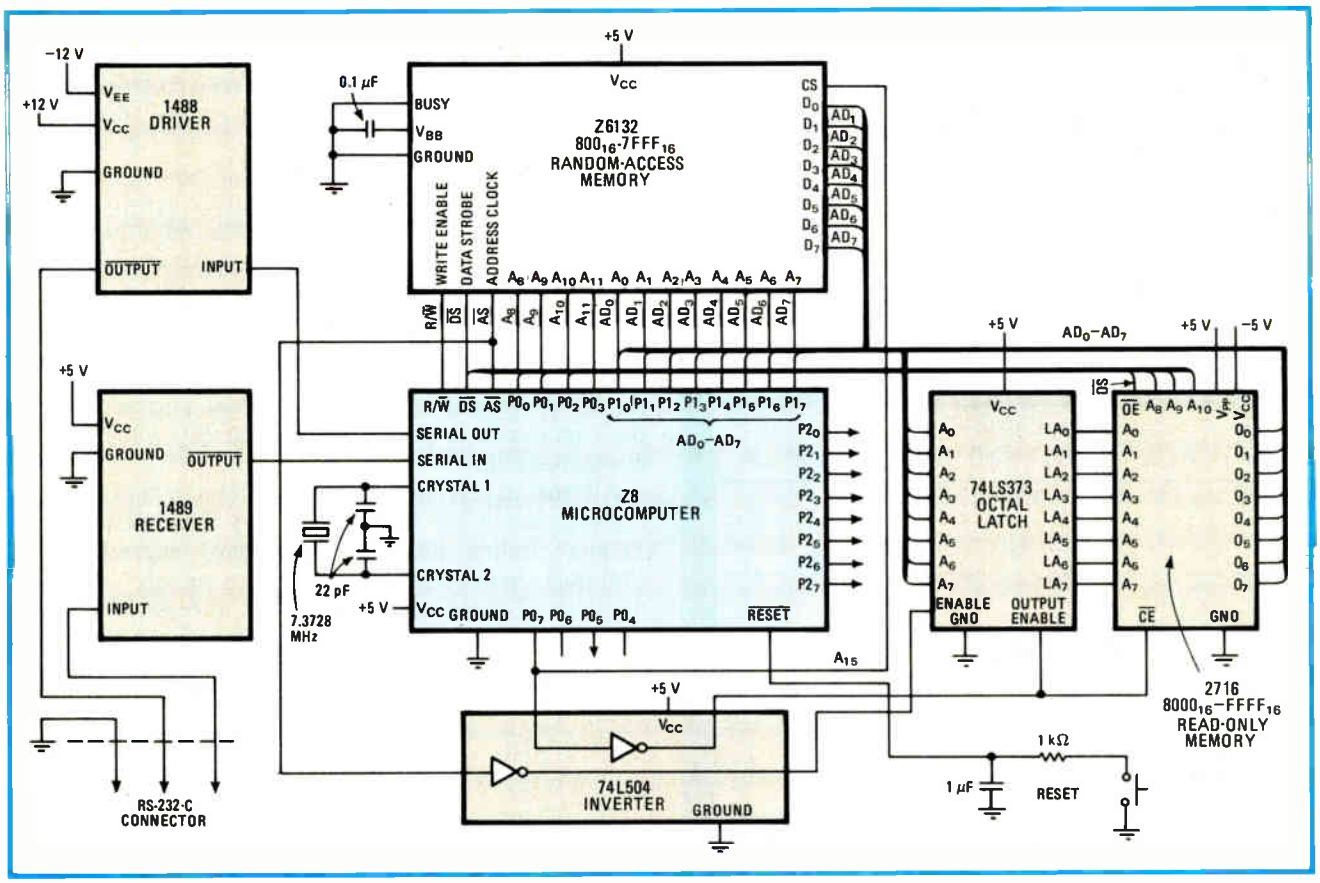
All the papers in this session treat signal lines as transmission lines. In the first and most basic paper, Thomas Balph, manager of systems engineering at Motorola Semiconductor Sector's strategic industrial marketing branch in Phoenix, Ariz., discusses the characteristics of microstrip, stripline, and wire over ground in relation to pc boards and discretely wired circuits. The causes and cures of ringing and crosstalk are also covered, as they apply to the various logic families shown in Balph's table (see p. 159). One of the more interesting papers is by N. C. Arvanitakis and J. J. Zara of IBM Corp.'s System Products division in Endicott, N. Y. They go into the design and measurement results for the electrical parameters for the card-on-board packages used in the IBM 4300 series processors.

One of the nagging problems facing packaging engineers today—how to reliably attach leadless chip-carriers to pc boards—will be attacked in session 22. Specific experiences as well as directions in packaging will be discussed. Perhaps the session's most useful paper is one by Charles Lassen of the PCK Technology division of Kollmorgen Corp. in Melville, N. Y. Called "Discrete Wired Metal-Core Substrates for Leadless Chip-Carriers," it reviews the options available to the designer interested in attaching carriers to pc boards—a leaded conversion as in the use of clips or sockets; the use of a low-expansivity substrate like epoxy/Kevlar; and the use of supported thin substrates on a metal core, such as Lampac and thin discrete wiring.

Outlook for instruments

With a multitude of new varieties of instruments on the floor of Wescon this year, two technical sessions will help give potential users a perspective on what is happening in instrument design. Session 7, chaired by Arthur Crooke of Data Precision Inc. of Danvers, Mass., will examine some recent trends toward what Crooke describes as "a new class of generalized sampled-data measuring instruments."

What Crooke has noted in the industry today is that advances in analog-to-digital conversion speeds and the



2. Magnificent seven. A full microcomputer board, with an RS-232-C port linking with a terminal and having Basic burned into the on-board microcomputer ROM, consists of only seven chips. It is described in session 17 in the talk on a compact Z8 board.

availability of inexpensive memory and computing power is making the architectures of various sampled-data instruments—digital oscilloscopes and spectrum analyzers, for example—roughly comparable. Extrapolating from these observations, the session's participants will consider the factors that influence the degree of specialization evident in today's processor-based instruments and will attempt to define a general-purpose instrument such as the one shown in Fig. 3.

The fact that sophisticated computing power is becoming readily available in instrumentation today creates a problem that will be examined in session 11. Instrument designers now have to take into account the fact that the user of a measurement tool should not need a computer science degree to operate it, and so the session will examine the question of user friendliness in advanced instrumentation. The session chairman is Bob Anundson of Tektronix Inc., who was largely responsible for the creation of the Beaverton, Ore., firm's 4041 IEEE-488 controller [*Electronics*, Aug. 11, 1981, p. 129].

To judge by the contents of session 15 on IC-sensor technology, the cost-sensitive consumer markets are still a long way from having the broad range of microprocessor-compatible sensors that they could use. A market overview from S. E. Craft and R. S. Whiskin of Mackintosh Consultants Co. in San Jose, Calif., projects that the U. S. automotive industry will consume about 110 million sensors in 1986, representing a market worth around $225 million—the estimated world market for all sensors being around $600 million. But the session papers are limited to high-performance strain gage and pressure transducer technology and do not address the tough task of low-cost data acquisition.

Analog-digital interfaces

Data-conversion and -acquisition systems will be subjected to several reviews and error analyses in session 23, which will be chaired by John Sullivan of Harris Semiconductor. To keep pace with the rapid development in microprocessors, data converters are being pushed to higher levels of integration—the pace of their advance being limited mainly by the difficulty of combining digital and analog functions in any one technology. Gerard McGlinchey and Edgar Macachor of Advanced Micro Devices will describe a high-frequency linear bipolar process that can support fast, dense, low-power logic gates. By using a 1-ohm-centimeter epitaxial layer thinned down to 4 micrometers, npn transistors were

able to achieve a cutoff frequency of 1.5 gigahertz.

These devices make a linear differential logic (LDL) gate as fast as ECL, but at one fourth the power consumption and in one third the area. The tradeoff is a much reduced logic swing that cuts the error budget by almost an order of magnitude. LDL is put to use in the Am6108, an 8-bit successive-approximation analog-to-digital converter, that converts in under a microsecond and can be interfaced with different processors using a minimum number of logic gates.

In session 19—"The Outlook for Linear ICs in the '80s"—Analog Devices, Norwood, Mass., will be represented with a fast, systems-level digital-to-analog converter. The AD567 incorporates a voltage reference, scale-setting resistors, and interface logic on chip and settles in 250 ns. Its interface logic includes two ranks of latches arranged to accept data from a 4-, 8-, 12-, or 16-bit data bus. They can be enabled with pulses as short as 100 ns.

Precision Monolithics Inc. of Santa Clara will present details of the OP-27/37, a "triple threat" operational amplifier that sets records for low-noise voltage without sacrificing the dc precision of its high-speed performance. By running the input stage at a relatively high current, the amplifier gives a mere 80 nanovolts of peak-to-peak noise in the 0.1-to-10-hertz band and 3 $nV/Hz^{1/2}$ at audio frequencies. On-chip offset trimming keeps other error sources down near the "noise floor."

Discussions of speech

In session 2, "Speech Technology in the '80s," attendees will explore some of the near- and long-term milestones for the growing technology of electronic speech synthesis. In her paper, chairwoman Sharon B. Crook of Texas Instruments Inc., Midland, Texas, describes "the technology innovations necessary to accommodate the market need" for speech products.

The subject of speech is broached again in session 6, which assesses the prospects of voice-processing technology for the 1980s. Emphasized here is the voice input/output's capacity to save time and free the hands and eyes. Higher productivity is the reason to go with electronic speech synthesis and recognition. Alexander Nahow and Alan Strass of the General Electric Co. in Bridgeport, Conn., give an industrial user's perspective of the field, based on extensive experience with in-house testing at GE.

Still another area into which electronic speech spills is covered in session 28, on technology to help the handicapped. Electronics can be used in "talking signs" to aid the blind. For example, infrared transmission would silently duplicate the written messages on street signs, house numbers, and bus stops, and the results would be read by handheld "readers" carried by a sightless person. Many instruments can be modified for use by the blind, and even the display of such complex instruments as an oscilloscope can be made accessible to the blind by recently developed means, explains John Brabyn of the Smith-Kettleweil Institute of Visual Sciences in San Francisco. In his paper, he introduces the concept of rehabilitation engineering and says that "putting handicapped people to work should be one of the most urgent priorities in the utilization of the latest electronic technology."

TYPICAL CHARATERISTICS OF MAJOR HIGH-SPEED LOGIC FAMILIES

	Logic family						
	F100K	MECLIII	10KH	10K	FAST	74AS	74S
Propagation delay (ns)	0.95	1.0	1.0	2.0	3.5	2.8	5.0
Power (mW)	46	60	25	25	4	20	20
Power-speed product (ps)	44	60	25	50	14	56	100
Rise and fall times (ns)	0.8	0.6	1.5	2.0	1.5	1.0	1.5
Technology	ECL	ECL	ECL	ECL	TTL	TTL	TTL

SOURCE: MOTOROLA

CAD from the desk of . . .

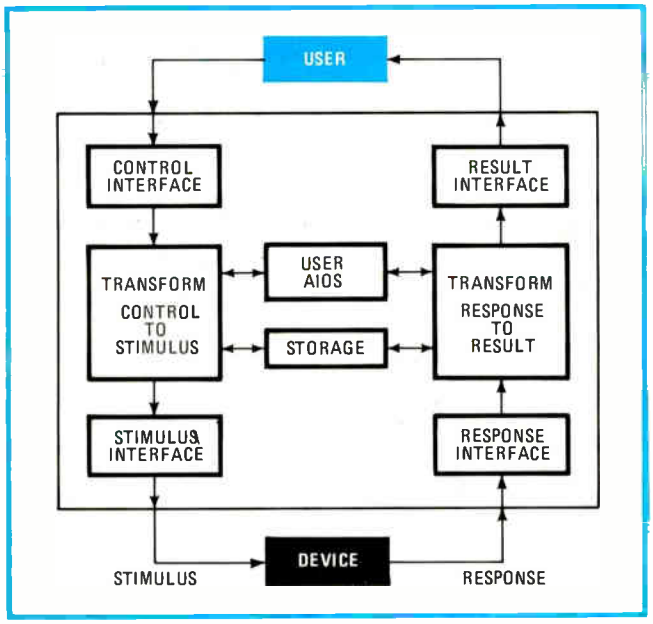
The desktop computer gets attention as a tool for computer-aided engineering and design in session 30, computers for engineering applications. According to chairman Bruce Hamilton of Tektronix Inc., Beaverton, Ore., the central message will be "that desktop computer-aided design is here—it's real, it's technically possible, it's affordable, and here are some examples."

"There are a lot more opportunities for desktop computers than many people realize. You don't necessarily need a VAX, a DEC system 20, an IBM 370, or a CDC 6600," he says.

The four papers to be presented show several examples of applying desktop computers to both CAD and computer-assisted engineering, CAE.

The first paper, on two-dimensional drafting, will be given by John Tangey of Tektronix. He will show how a desktop computer can be used to solve many generalized drafting problems. Demonstrating that such computers can, in fact, function as tools for CAE, William Cummings of Hewlett-Packard Co., Fort Collins, Colo., discusses in the second paper all aspects of design from the concept through to the final product. His paper is entitled, "CAE—Productivity Improvements Using Desktop Computers."

While the first two papers present a look at a horizontal slice of the use of small computers in a variety of engineering tasks, the next one shows a vertical slice. In "A Desktop Graphics Work Station for VLSI CAD," Larry Dorrie and Michael Dickens of Avera Corp., Scotts Valley, Calif., tell what they did and why they did it in developing a work station specifically for the computer-aided design of VLSI. Looking beyond what is now



3. Toward a new definition. In "Future Trends in Digitizing Signal Analyzers," Arthur W. Crooke proposes this functional model for general-purpose instruments. A microcomputer, a-d and d-a interfaces, a display, and a control panel make up the hardware.

available, James D. Howard of Intel Corp., Aloha, Ore., in the last paper of session 30, discusses what is desirable in a graphics-based engineering work station for VLSI design.

A new subject for Wescon this year is office automation—in particular, telephone message systems using digitized voice [*Electronics*, April 21, 1981, p. 99; July 14, p. 34]. Howard I. Cohen of General Telephone & Electronics in Needham, Mass., says that "voice messaging is going to be very important in office automation—some people believe that electronics text mail systems alone will not be enough. For example, they ask how are you going to get all those people to type?" He is organizer and chairman of session 10 on computer-controlled voice message systems.

The direction of digital signal processing

For Lyle F. Pittroff, chairman of session 3, "Future Trends in Digital Signal/Array Processing," the five papers he has gotten together "provide a broad spectrum of the participants in the signal-processing business." Pittroff's firm, Advanced Micro Devices, where he is manager of bipolar product planning, is sponsoring one of the three papers about chips designed for signal processing. Its author, Bernard J. New, will present preliminary information about the Am29540 fast-Fourier-transform address sequencer.

Another chip paper by John Eldon, senior systems engineer of TRW Inc.'s LSI Products division in La Jolla, Calif., will discuss that company's new 64-bit digital correlator [*Electronics*, July 14, 1981, p. 118]. Also, a paper by a team of authors from Monolithic Memories Inc. will discuss a bipolar number-cruncher that they say "provides a cost-effective alternative to MOS devices in microprocessor systems."

Not only will chips be discussed, but systems and applications will also be covered. For example, Dave Birkner, engineering vice president of Computer Design & Applications in Newton, Mass., will present a paper on "Advances in Array Processor Programming Techniques" and Alan Peterson of Stanford University in Palo Alto, Calif., will discussing the "Application of the Fast-Fourier Transform in Fast Convolution and Digital Filtering."

While signal processing helps the system user get the most information out of his equipment, it is important to get the information into the systems in the first place. Often, this requires a first-class radio receiver.

The technologies that add glamour to receiver design these days are microprocessor control, light-emitting-diode displays, and digitally synthesized local oscillators. "But," comes the reminder from James M. Bryant, special projects manager of Voxson Audio Ltd., of Abingdon, England, "the mixer is the most critical part of a high-performance superheterodyne receiver. Only this device determines a receiver's ability to receive a microvolt signal in the middle of a band full of 100-millivolt signals or worse."

To ensure that attendees at his session 24 come away aware of the problems of mixer design, Bryant has put together four papers. Three are on the design and performance of various types of discrete-component and integrated mixers and the fourth is on mixer problems as seen by their receiver designer. The fact that four of the five authors of the mixer papers are radio amateurs should come as no surprise since the amateur bands are often shared with high-power broadcast services. The mixer determines the amateur's success in differentiating his microvolt signal from the 100-mV signals that are but tens of kilohertz away.

How to do it with fiber

No major technical meeting would lack status without a session on fiber-optic technology. Wescon has a four-paper tutorial session 16, put together by Ronald L. Ohlhaber, product development manager at Belden Corp. of Geneva, Ill. Ohlhaber will present one of the papers on relating the properties of fiber cable to its applications. But cables have to be hooked together, and that will be the subject of James Leidy's paper on "Advances in Fiber Optic Connectors." Leidy's connectors also hook up to emitters and detectors, which is where Motorola's paper on low-cost fiber-optic components for industrial applications" comes in. Finally, for do-it-yourself types, H. A. Carnes and E. E. Basch of GTE Laboratories Inc. in Waltham, Mass., have prepared "Fiber-Optic Transmission Links." Their paper features a link power-budget calculation. □

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Circle 160 on reader service card

This new programmable sweep generator uses distributed microprocessor architecture.

CW accuracy can be held to ±10 Hz or better by phase locking to external frequency counter or lock box.

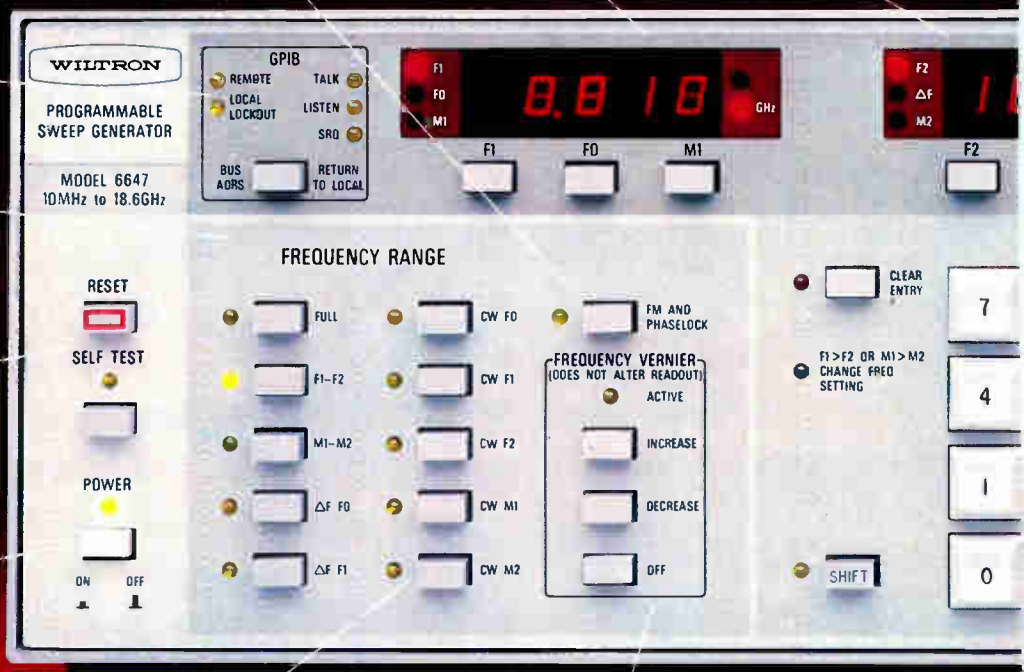
Both F1 (start) and F2 (stop) sweep frequencies, or M1, M2 marker frequencies or any combination can be displayed simultaneously.

GPIB (IEEE-488) bus messages include serial and parallel poll, group execute trigger and SRQ.

Five sweep modes provide broad or narrow band control for unprecedented measurement flexibility.

Self-test and automatic fault diagnosis occur every time the instrument is turned on; a diagnostic code is displayed on the front panel.

SAV and RCL commands can be used to store test setups. Non-volatile memory holds controls and readings at previous setting for 20 days or more.



Remarkably clean and stable CW signals are available with 1 MHz resolution at five pushbutton-selected frequencies or program-selected values.

Frequency Vernier with 100 kHz resolution allows precise adjustment of CW or center of ΔF sweep frequency.

Digital convenience and accuracy are part and parcel of the new Wiltron 6600, an eminently easy-to-use family of instruments which combines new RF technology with microprocessor control. With 10 MHz to 40 GHz coverage, the 6600 group is expressly designed to meet your ATE needs too. There are, quite simply, no more advanced sweeper/signal sources at any price.

A look at the features

Here in one compact 33 pound unit we give you a virtually self-explanatory pushbutton controlled front panel. All pushbutton controls can be programmed via the IEEE-488 interface bus. We give you a sweeper using fundamental oscillators avoiding the substantial errors generated by the harmonic products of multiplier type oscillators. We give you modular construction without the disadvantages of RF plug-ins. We give you a fast unit using distributed microprocessors and a display preprocessor to reduce bus loading and measurement times.

The result, broadband coverage with the lowest harmonic content (>40 dBc, 2-20 GHz), lowest residual FM and greatest stability on the market today. We give you a unit with the best frequency accuracy (±10 MHz up to 20 GHz) because it uses a ROM to correct non-linear residual frequency characteristics of YIG oscillators.

Programmable parameters include stepped sweep with selectable step size, start and stop frequencies, sweep width, marker frequencies, sweep time, output power level and optional attenuation.

Other features of note include high spectral purity, modular construction, self-test, 82 dB power control range with 0.1 dB resolution and power sweep.

So easy to operate

Multiple microprocessor design and human engineered panel controls make it easy for even the least experienced to use—on or off the bus.

It's a Wiltron.

Optional attenuator provides bus or front panel control of power level over 82 db range.

All frequencies, sweep times, power levels and their units are displayed when selected on the corresponding pushbutton or commanded over the bus.

Three markers provide easy identification of swept frequencies, center frequency of △F sweep and M1-M2 sweep limits.

Slope control compensates for losses that vary with frequency to provide flat output at test point.

Excellent source match (<1.4 up to 20 GHz) reduces measurement errors.

Wiltron super-flat leveling components hold variations in output power to <±0.6 dB from 10 MHz to 20 GHz.

External directional detector or power meter can be used to level output power at remote test position.

Keypad provides fast, precise data entry.

Convenient electronic control lever obsoletes tedious and inaccurate twiddling of mechanical control knobs.

Eight models cover the frequency range of 10 MHz to 40 GHz.

Model	Range	Power
6609	10 MHz to 2 GHz	>20 mW (+13 dBm)
6617	10 MHz to 8 GHz	>10 mW (+10 dBm)
6637	2 GHz to 18.6 GHz	>10 mW (+10 dBm)
6638	2 GHz to 20 GHz	>10 mW (+10 dBm) at ≤18.5 GHz >5 mW (+7 dBm) at >18.5 GHz
6647	10 MHz to 18.6 GHz	>10 mW (+10 dBm)
6648	10 MHz to 20 GHz	>10 mW (10 dBm) at ≤18.5 GHz >5 mW (+7 dBm) at >18.5 GHz
6636	18 GHz to 26.5 GHz	>3.1 mW (+5 dBm)
6640	26.5 GHz to 40 GHz	> 1 mW (0 dBm)

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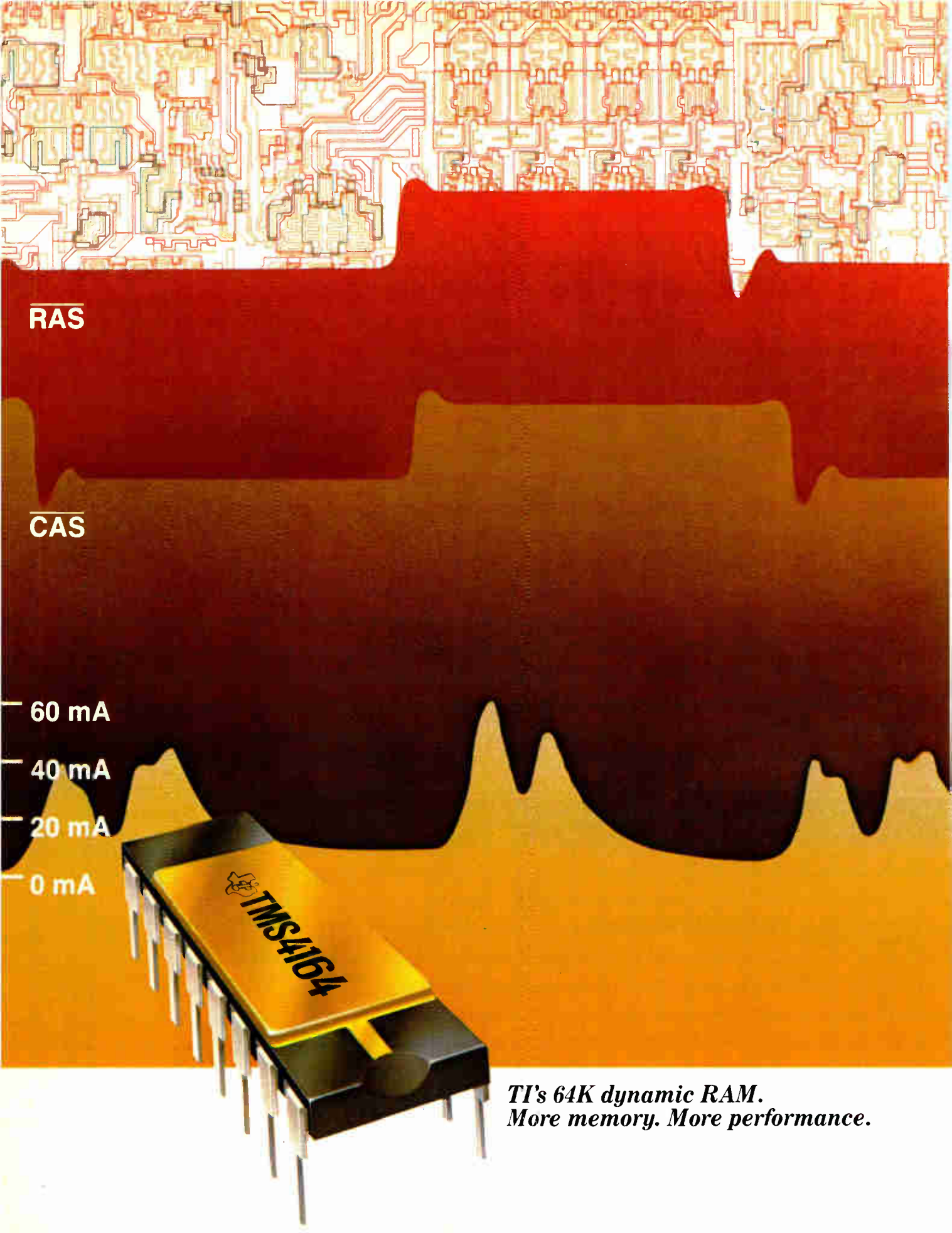
Circle 163 on reader service card



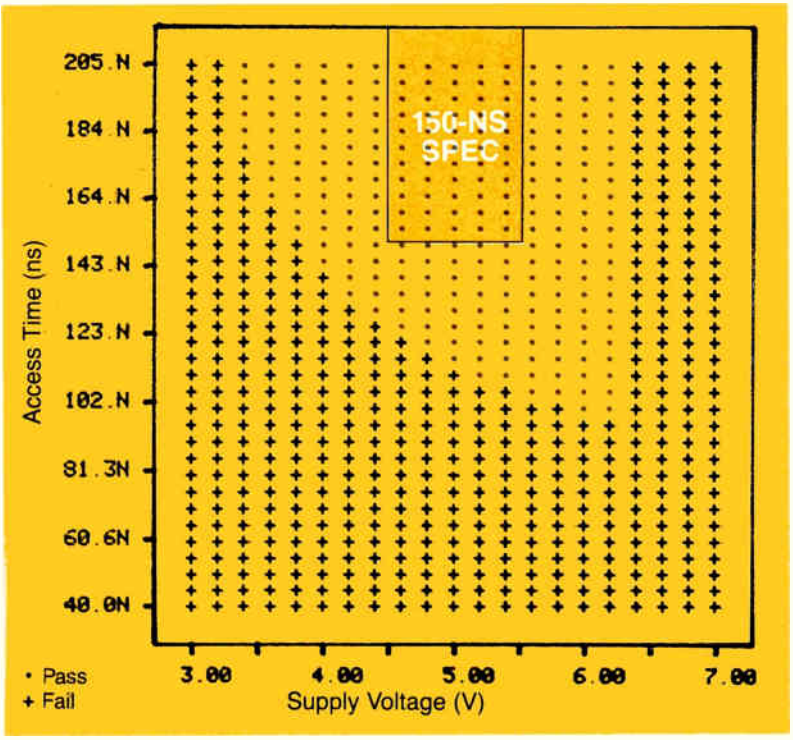
TI's 64K dynamic RAM.
More memory. More performance.

TMS4164

The performance leader. From Texas Instruments.

When we began designing the 64K RAM, we decided to make it better than the 16K. Not just four times bigger.

What's better? In a word, performance. Add up high speed, reliability, low power and improved system operating margins, and you'll see why our superior performance puts the TMS4164 in a class all by itself.



Faster access times
The wide range of TMS4164 functionality and speed potential is demonstrated in the graph to the right. This illustrates the wide operating margins designed into the high-performance 150-ns TMS4164. And, even faster devices are on the way.

Power dissipation
At 125-mW typical, the TMS4164 is unequalled in the industry for low power dissipation. Power design features like interlocked clocks mean you use only as much power as you need. Only when you need it. Our optimum architecture, requiring only 256 sense amplifiers, assures you of minimum power dissipation and enhanced reliability.

Ease of use
Two separate 8-bit internal buffers simplify use — one is for row address, one is for column address. TTL-compatible, one-clock operation greatly expands input timing flexibility and assures fast throughput.

TMS4164 64K Dynamic RAM			
	4164-15	4164-20	4164-25
Access Time Row Address (Max)	150 ns	200 ns	250 ns
Cycle Time Read or Write (Min)	280 ns	350 ns	410 ns
Cycle Time Read Write (Min)	280 ns	350 ns	410 ns
Power Dissipation Operating (Typ)	140 mW	125 mW	105 mW

Lowest power surge
Our 256 cycle refresh architecture has significantly reduced the current surge problem of designing with other dynamic RAMs. The resultant lower current spikes (≅60mA), less than on *one* 16K dynamic RAM, facilitate system power distribution, increase noise immunity and improve board layout.

And there's more
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And Altos supports these systems with a broad software selection including the three industry standard operating systems—CP/M, multi-user MP/M** and OASIS†. These operating systems support seven high level programming languages: BASIC, FORTRAN, COBOL, PASCAL, APL, PL/1 and C. Also available are comprehensive communications packages: ASYNC—Altos-to-Altos, BISYNC—Altos-to-mainframe and full networking with CP/NET. All are designed to run on a high speed 800 Kilobaud networking channel—standard with every system.

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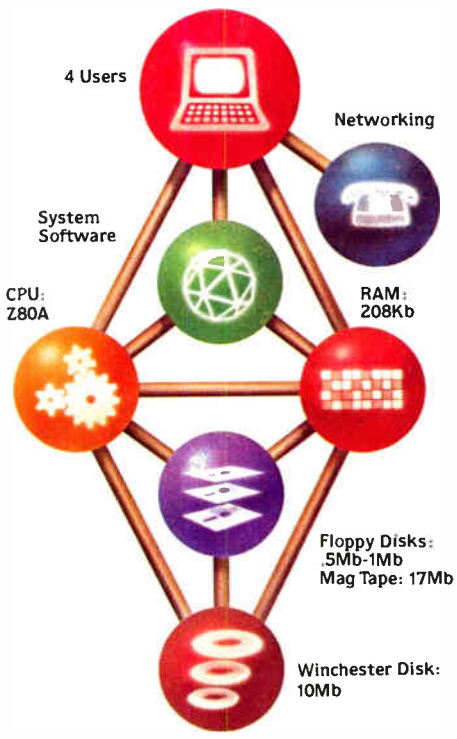

SYSTEMS PICTURED:

ACS8000-10 (10Mb HD + 1 floppy)	$ 8,500
ACS8000-10/MTU (10Mb HD + DEI Mag Tape)	$10,990

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Circle 269 on reader service card

New products

Highlights of the product introductions at Wescon '81 include instruments that exhibit maturing microprocessor-based design

Modular digital analysis system generates patterns, captures responses at up to 330 MHz

When Wescon's gates swing open next month, visitors will enter a new era of instrumentation. Increased sophistication in the use of microprocessors is the cause of that new era, and one of its best exemplars will be a tool that changes the meaning of logic analysis.

Called the DAS 9100 digital analysis system, it combines logic response gathering with its logical counterpart—digital pattern generation. Configurable from printed-circuit cards, it can team a 25-MHz pattern generator for exercising the circuit under test with a wide variety of data-acquisition cards for monitoring the circuit's response.

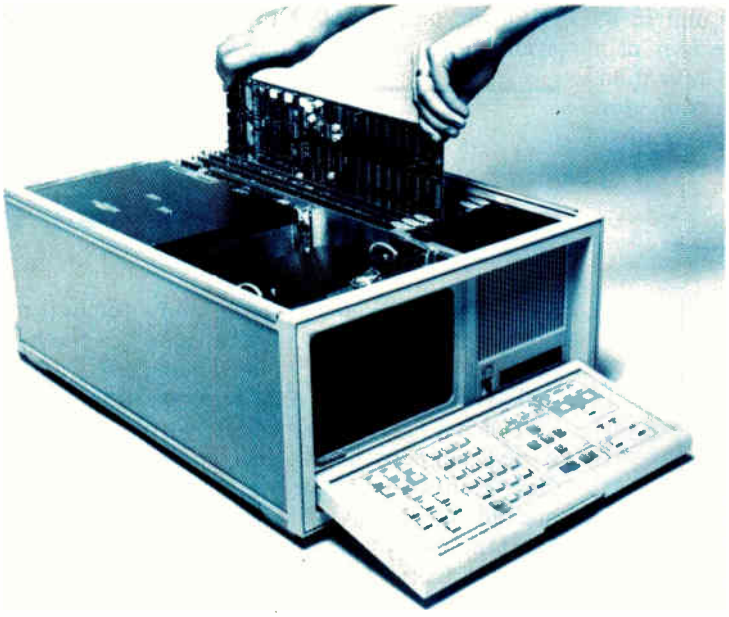
The object of merging these two sides of the digital test function in one benchtop unit, according to Tektronix designer Steve Palmquist, is to streamline engineering effort. Palmquist has talked to many product designers who "spend 50% of their design time building test fixtures." Thus he and software maven Gerd Hoeren set out to build an extremely flexible expandable system with which the user could, in effect, converse easily with the circuit he or she was designing.

The heart of the resultant system is a Z80 controller card that runs Pascal software to orchestrate the functions of the other system cards, or modules. It and the trigger-time–base card take up two slots in the DAS mainframe, leaving six for the user to fill with combinations of generation and acquisition cards.

The primary pattern generation card, the 91P16 which has 16 data output ports, can be expanded with up to two 32-channel 91P3Z slave cards, so that a total of eighty 25-MHz channels can be used to deliver test vectors. Two strobe channels on the primary card and four on each slave make it possible for the pattern generator to simulate various system bus structures.

For capturing responses from a circuit under test, two kinds of cards are provided: one type for watching software flow and another for checking hardware operation. The card aimed at software debugging—the 25-MHz 91A32—offers a broad 32 channels, while the speed needed for catching glitches is provided by the cards for hardware—the 8-channel, 100-MHz 91A08 and the 4-channel, 330-MHz 91A04, and the latter's 4-channel expansion card, the 91AE04. Both acquisition-card types may be used simultaneously, with the software cards arming hardware ones so that program events can automatically be correlated with hardware operations.

The actual operation of the instrument could have turned out to be a nightmare, had not the software been designed to provide an extremely efficient set of menus. A total of seven different menus can be called to the DAS screen, letting users define output patterns, strobe timing, system mnemonics, logic state and timing displays, and so on by moving a cursor to the appropriate field. Setting up the test conditions thus becomes a quick job, particularly since the DAS itself automatically adjusts the menus to reflect the cards



it contains. Further, set-ups and pattern programs can be stored using an optional DC-100 tape drive or RS-232-C port.

Prices for the cards vary from $3,700 for the basic pattern generator card to $7,950 for the 4-channel, 330-MHz data-acquisition module, and the mainframe is priced at $4,950. A typical system—one with 32 channels of 25-MHz data acquisition, 8 channels of 100-MHz acquisition, and 16 channels of pattern generation—is priced at $16,900.

Tektronix Inc., P. O. Box 1700, Beaverton, Ore. 97075. Phone (800) 547-6711 [351]

1.8-μs 10-bit a-d converter dissipates only 775 mW

Fast 10-bit analog-to-digital converters tend to run hot. This is less true of Analog Devices Inc.'s new AD579, however, which is claimed to have the lowest power dissipation in its market at a typical 775 mW. A hybrid design, complete with internal clock, voltage reference, and comparator, the unit from Analog's Semiconductor division converts in 1.8 μs maximum and also is said to offer initial accuracy, linearity, and temperature coefficients comparable with those of modules.

Though there are hybrid a-d converters with faster conversion times, their power dissipation—as much as three times the AD579's worst-case 1.2 W—makes them unattractive in some applications. In addition, the AD579 may be the only unit in its market niche to offer the user of a choice of ±15- or ±12-V operation. In the case of the 12-V version, designated with a Z suffix, power dissipation for rated accuracy is said to be about 20% less than that of the 15-V model, though Analog Semiconductor does not specify an exact figure for it.

The AD579 sells for $138.50 to $251 each, depending on packaging and environmental characteristics; for 100-unit lots, prices fall to $103.50 to $178.50. Thus, it competes well with modules on a price-performance basis, according to the company; its specifications are comparable with modules', and in its 32-lead double-width dual in-line package, the AD579 requires less board space and power.

The internal scaling resistors let the part serve analog input ranges of ±5, ±10, 0 to 10, and 0 to 20 V. Also, the unit's +10-V reference is available at pin 24. The buried-zener reference is laser-trimmed to within ±0.1% accuracy and offers up to 1 mA for external use; its temperature coefficient is ±15 ppm/°C.

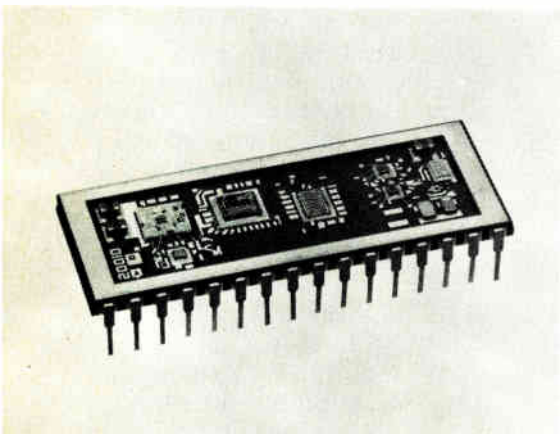
Accuracy. Gain error for the AD579, as well as its bipolar and unipolar offset error, measure 0.25% of full-scale range, maximum. Linearity error is a maximum of 0.048% of full-scale range. Differential-linearity error is specified as ½ least significant bit, maximum.

Gain drift is independent of specified temperature range, measuring 30 ppm/°C maximum whether the unit in question is rated for operation for 0° to 70° or −55° to +125°C. Unipolar offset is 5 ppm/°C maximum; maximum bipolar offset is 15 ppm/°C.

Power requirements for the AD579 are relatively relaxed. Logic input voltage range can be as wide as 4.25 to 5.75 V for rated accuracy. Power supply voltage ranges for rated accuracy also are broad, with the 15-V models capable of handling 13.5- to 16.5-V inputs and the 12-V versions operating with anything between 11.4 and 16.5 V.

The AD579 is available in hermetic ceramic packages. Units made in accord with MIL-STD-883B are available. Delivery is from stock to two weeks.

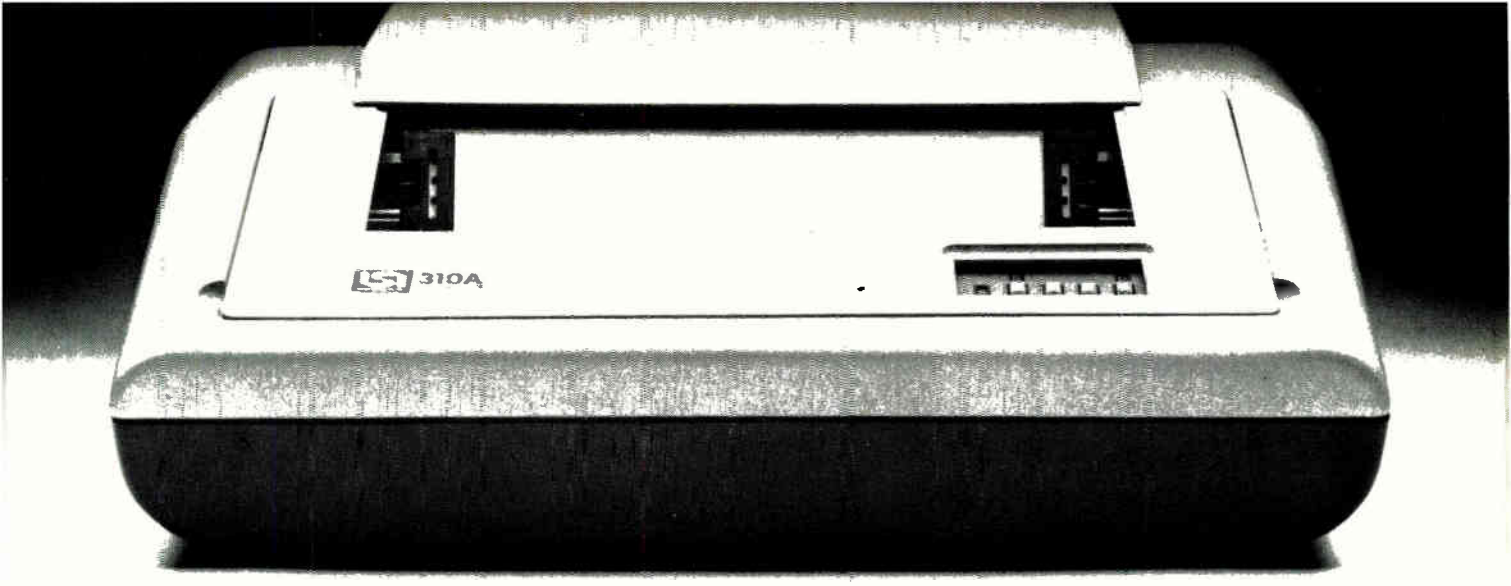
Analog Devices Inc., Semiconductor Division, 829 Woburn St., Wilmington, Mass. 01867. Phone (617) 935-5565 [358]



48-channel logic analyzer has high-level user interface

Setting a new record in speed, number of channels, and storage capacity may be a good way of advancing logic-analyzer design. But the people at Dolch Logic Instruments GmbH, parent company of DLI Inc. in San Jose, Calif., think there is a better one to more analyzer efficiency: combine high performance with analysis tools that easily interface with the system under test as well as with the instrument's operator.

Such interfacing, in conjunction with intelligent probing and advanced trigger and analysis features, is the hallmark of DLI's 48-channel, 50-MHz logic analyzer, the LAM 4850A. The successor to the world's first 48-channel analyzer, the LAM 4850 [*Electronics*, May 24, 1979, p. 217], the A version will go to market in September in both Europe and



LSI quietly presents the Hummm Terminal.

From those wonderful folks who brought you the Dumb Terminal® video display, now there's the Hummm Terminal™ Printer.

Featuring quiet operation that's almost unheard of, outstanding reliability and print quality, impressive throughput and a long list of sensible features.

All at a hard-to-believe low price. So low, in fact, that you'll immediately know why we call it Hummm Economics.

A LOT OF IMPACT PRINTER WITHOUT A LOT OF NOISE.

Quite simply, the 310A Hummm Terminal is one of the quietest impact printers in its class. In fact, with its Acoustic Quieter it checks in at a soothing 56dBA. That's quieter than most typewriters. And than most copy machines.

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BELLS AND WHISTLES STANDARD.

You won't find many options on the Hummm Terminal. Because we made most of them standard.

Its logic seeking capability finds the shortest path to the next character on a new line—thanks to space and blank character compression. And with an optionally expanded buffer of 2048 characters, a full terminal screen can be dumped instantly.

You get superior printing capability, including true lower case descenders and underlining—good for an original and five crisp copies on multipart forms. A 9x7 character field. Complete horizontal and vertical forms control. 14 switch selectable form lengths, and 14 perforation skip-over formats. And a 100% duty cycle.

HUMMMAN ENGINEERED.

The Hummm Terminal brings to computer printers the same high standards that made our Dumb Terminal video display the standard for an entire product category. It's rugged, durable, and stylish so it fits right into any office decor.

So call your nearest LSI Authorized Distributor and ask him for some Hummm Terminal information. And when you do, fill out the coupon completely and send it to us. We'll send you a free Hum^3 with over 3 billion combinations—and only one right one.

It'll give you something to do during those quiet moments when the Hummm Terminal is humming along.

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THE 310A HUMMM TERMINAL.

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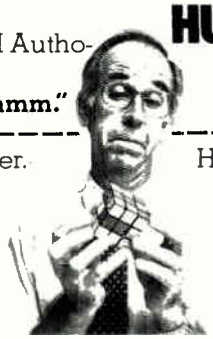

Hummm, Lear Siegler. You've certainly given me something to think about. I asked my distributor about the Hummm Terminal.

Here's his name along with my business card. (I realize that I can't get a Hum^3 if I don't include my card.)

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Circle 170 on reader service card

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the U. S. Its U. S. price is $11,750.

Featuring what Volker Dolch, head of DLI, calls "an advanced level of user communications," the microprocessor-controlled 4850A has a monitoring function that presents status information and comments on the menu setups on a separate display. Whenever a parameter is entered into the menu formats, the monitor can be called up any time to interpret it, its range, or its interaction with the present setup. Not only does the instrument signal erroneous entries by flashing messages, but it also spells out why a particular entry was in error.

As Dolch points out, it is a tricky task, even for the experienced operator, to collect meaningful data across 48 channels using three simultaneous external clocks, an internal one, and nine clock qualifiers, and to trigger at the same time on nested subroutines. The 4850A's monitor, however, makes that task a relatively simple one since it interprets the setup and keeps track of clock and trigger events at the inputs.

A battery-backed complementary-MOS memory stores up to six files of menu parameters and display configurations. Even after three months without power, the 4850A can recall previously entered setups. Storage and recall are handled by a scratch table display, so that the user can keep a log of various test conditions.

A number of high-performance general-purpose probe pods, each handling four channels, facilitate operation. Designed around a custom thick-film hybrid circuit, the quad-channel pods minimize loading and distortion of the signal being investigated because of their high impedance—1 MΩ. The pods can be stacked together to form application-oriented input blocks. The hybrid circuit in each pod helps catch glitches as short as 5 ns in duration.

The 4850A can be turned into a dedicated tool with Dolch's personality probes and disassembly software. Probes supported by mnemonic disassemblers are available for the 8080, 8085, 8086, 6800, 6802, 6805, 6809, Z80 and 1802 microprocessors. The unit has RS-232-C and IEEE-488 interfaces.

Also interfacing with the 4850A are a signature-analysis probe and a channel-expansion probe. With the latter, up to 96 channels can be traced by doubling the basic 48 channels. Available later this year will be the 68000 and Z8002 trace modules and disassemblers.

The 4850A consists of three independent 16-channel analyzer modules with a maximum sampling rate of 50 MHz, a 1,000-bit-per-channel resolution, four-level sequential triggering, and three levels of clocking. One or more modules may be switched on or off, depending on the task at hand. Available from the firm shortly will be a 16-channel 4-K recording block with a maximum sampling rate of 10 MHz.

There are two levels of complexity of trigger performance. The standard one has four trigger levels with pass counting on each level and with range triggering and trigger delay capabilities. The advanced version has 12 trigger levels with an interaction capability for selective tracing. Boolean combinations of three trigger words, each 48 bits wide, are possible on every sequential step. Conditional advance, jump, and restart capabilities are also provided.

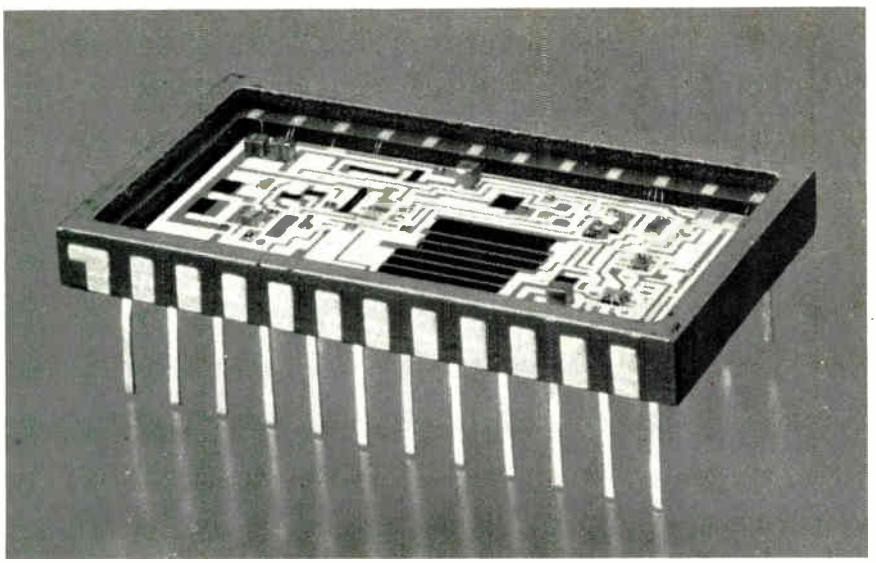
A search feature simplifies locating specific occurrences in the memory. It can search for strings of up to 12 words, making it possible to identify and address, not only single events on the 48 channels but also sequential occurrences of specific program conditions.

DLI Inc., 230 Devcon Dr., San Jose, Calif. 95112 [353]

Hybrid sample-and-hold amp settles to ±0.01% in 200 ns

Teledyne Philbrick's 4860—a thin-film hybrid sample-and-hold amplifier—sets a tough performance standard for high-speed data acquisition: it typically settles to ±0.01% accuracy in only 160 ns and is guaranteed to do so at 200 ns maximum.

Even with this speed, the hold



capacitor is large enough to keep the pedestal error to at most ±20 mV and the droop rate to at most ±5 μV/μs. The secret of this high performance is a proprietary operational amplifier using a discrete field-effect transistor at its input—an op amp that drives up to ±40 mA and gives the 4860 a 16-MHz bandwidth and 300-V/μs slew rate. What's more, the FET input matching is so good that the maximum offset drift is only ±15 ppm of the +10-V full-scale range per °C. Using a high-speed double-diffused MOS FET switch at the input, the device maintains a high feedthrough attenuation of 74 dB at 2.5 MHz.

The sample-to-hold transient settles to ±0.01% of full scale (±1 mV) in 60 ns typically. Other key specifications are a low maximum offset error of ±5 mV, an aperture delay time of 6 ns, and an aperture jitter of only ±50 ps.

The push for higher speeds in sample-and-hold amplifiers has led to higher power consumption and reduced operating temperature ranges. But the 4860 employs TTL—not emitter-coupled logic—and as a result, consumes a low 875 mW, enabling it to operate reliably over the full −55° to +125°C range. Fully screened versions meeting MIL-STD-883 are available. Prices start at $164 in lots of 100, and prototype quantities are now in stock.

Teledyne Philbrick, Allied Drive at Rte. 128, Dedham, Mass. 02026 [354]

Arbitrary-waveform/function generator puts out waves digitized to 12-bit resolution

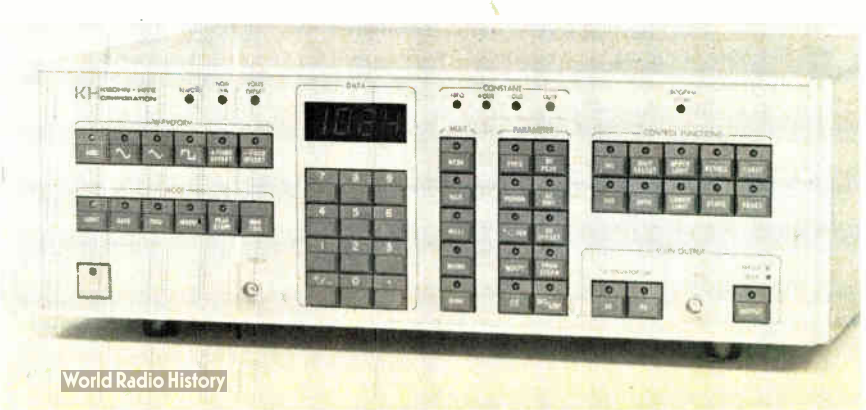
The 5910 generator of arbitrary waveforms or other functions produces repetitive waveforms of any desired shape in addition to the sine, triangular, square-wave, and other standard waveforms used in bench-top and automatic-test applications. Unlike Krohn-Hite Corp.'s earlier model 5900 programmable function generator [*Electronics*, May 22, 1980, p. 199]. The 5910 consigns generation of arbitrary waveforms to hardware rather than software, which speeds waveform production, reports Gary R. Ware, project engineer at the firm.

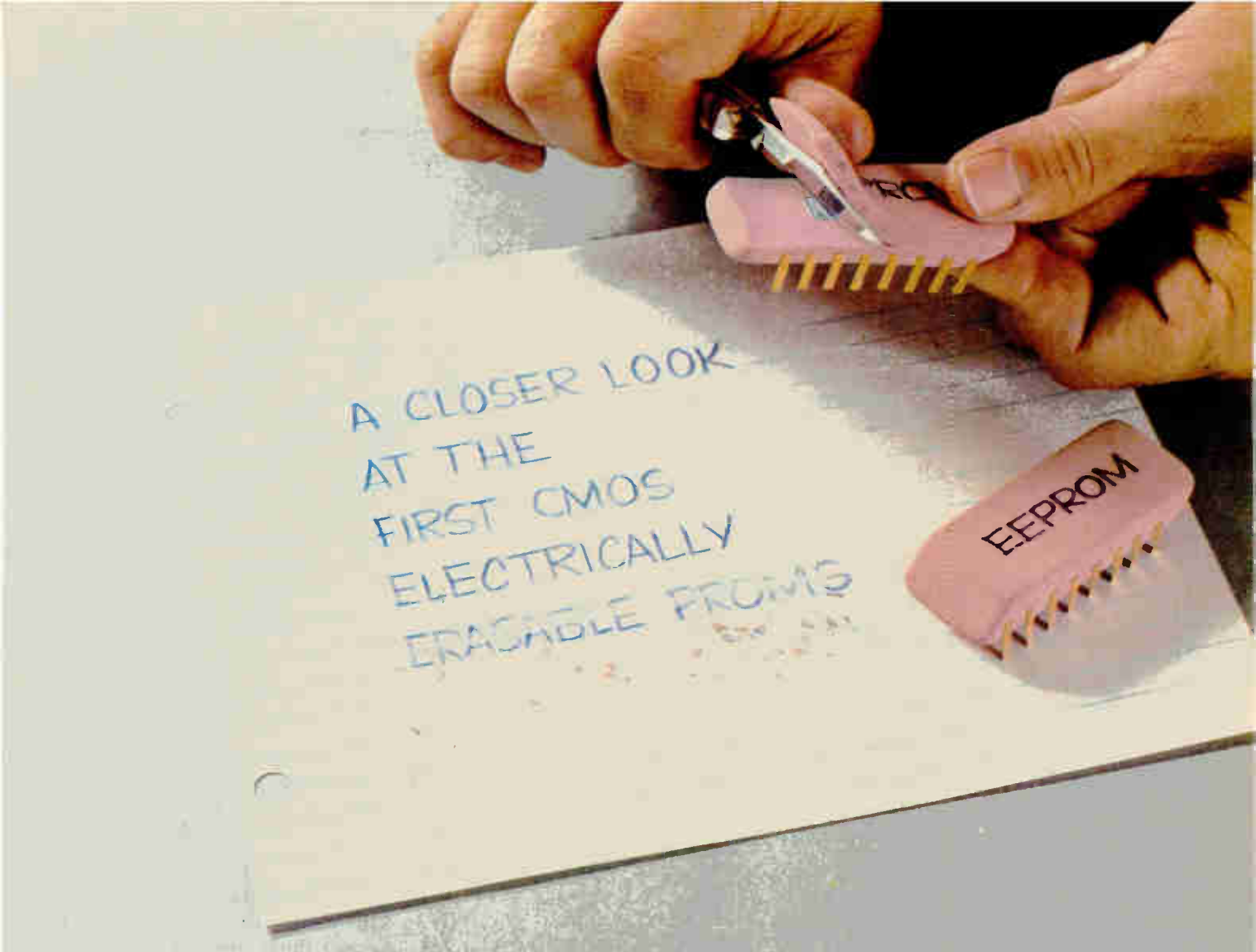
The microprocessor-based 5910 stores arbitrary waveforms in a 1-K-by-12-bit MOS memory bank. After defining a particular wave shape, the user can enter the points by hand as a series of voltage levels at up to 1,024 intervals of equal length. The 5910 automatically scales the entered voltage inputs along a 4,096-level resolution range to reproduce the waveform. Data points are put out by the generator in a minimum of 200 ns.

Download. The generator's IEEE-488 bus interface makes it possible to download digitized waveforms into its memory. A computer on the bus may be used to feed the 5910 data for complex algorithm-based waveforms, or other digitization methods may be employed to reproduce hand-drawn or existing analog wave shapes.

Originally designed for the 5900, an autoprogrammer unit continues to operate in the 5910's production of log and nonlinear waveforms. Featuring arithmetic and automatic increment or decrement functions, the autoprogrammer performs digital linear sweeps over a 10,000-to-1 range, log sweeps over the 5910's frequency range of 0.0001 Hz to 5 MHz, and nested loops that intermix log and linear sweeps.

The unit has nine storage registers, each storing parameters for an entire instrument setup. Other features include fixed or variable dc offset to ±15 V; 20-, 40-, and 60-dB





HUGHES EEPROMS NOW IN VOLUME PRODUCTION!

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Hughes EEPROMs, introduced in 1980, are gaining wide market acceptance in applications requiring electrically erasable non-volatile memory and low power operation. Production quantities are now being delivered for both the 4K and 8K bit versions.

Applications are divided into two general categories:

- convenient alternative to EPROMs
- in-circuit programming which offers new dimensions in innovative design techniques.

For example; Hughes has developed a digitally compensated crystal oscillator (DCXO) with temperature compensation using our HNVM 3008. The ROM code is not written until after the product is completely assembled, providing more accurate compensation, ease of manufacture, and subsequent recalibrations in the field. Other applications are emerging for postage meters, portable terminals, adaptive processors and many more.

The HNVM 3004 (512 x 8) and the HNVM 3008 (1024 x 8) EEPROMs can be written 10,000 times and retain information for 10 years at 125°C or 20 years at 70°C. Naturally, the Hughes HNVM 3000 series are compatible with all major logic families.

To respond to the EPROM market, Hughes is introducing the HNVM 3704 (512 x 8), our first product to provide a cost effective alternative to EPROMs with CMOS characteristics. This device can be programmed electrically in 1 millisecond and erased electrically in 100 microseconds.

It is time for you to consider Hughes EEPROMs. Programming is easy to accomplish either in-circuit or out-of-circuit. Parts are available now from Hughes distributors. For more information and your copy of our new EEPROM application notes contact your local Hughes Representative or Hughes—Solid State Products.

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Circle 174 on reader service card

attenuation; waveform inversion; zero-or-peak and start-or-stop levels for gated, triggered, and triggered-burst modes; and user-selectable upper and lower parameter limits.

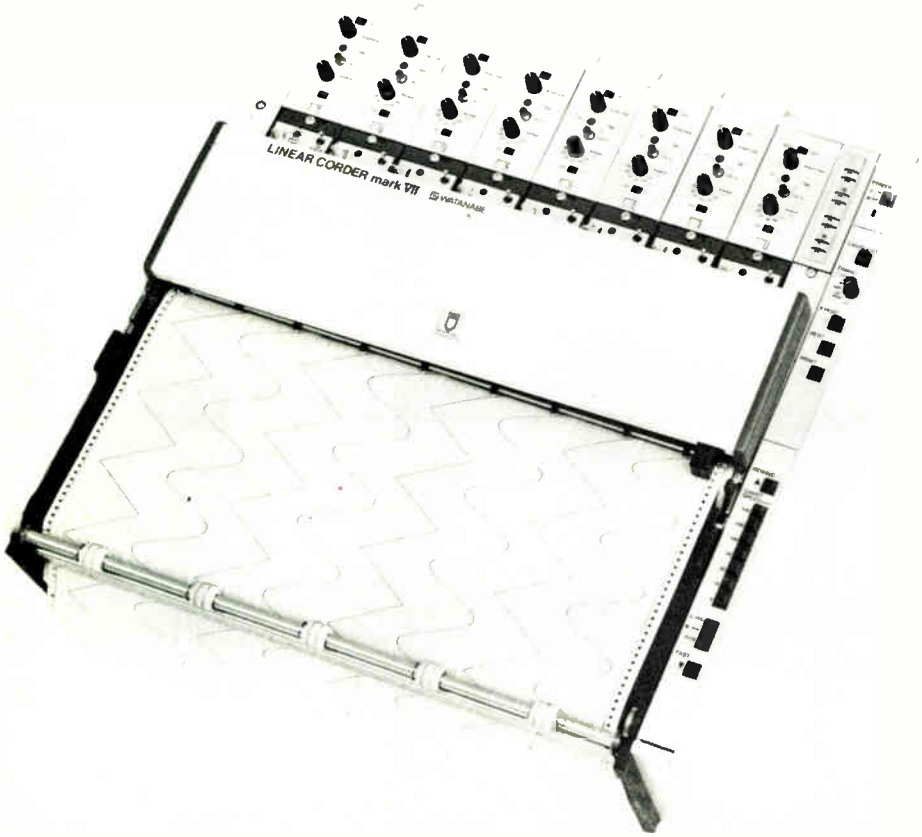
The unit's maximum output is 30 V peak to peak (open circuit) or 15-V p-p into 50 Ω, and its duty cycle is variable from 1% to 99%. Amplitude accuracy typically is to within ±2% of reading; slew rate is 20 V/μs maximum, and sine-wave distortion at maximum output is less than 0.5% (−46 dB) to 100 kHz, and 3% (−30 dB) at 5 MHz.

The 5910 weighs in at 26 lb and typically consumes 60 W, 25 W in standby mode. The instrument operates from 0° to 50°C, costs $4,500, and can be delivered in 60 days.

Krohn-Hite Corp., Avon Industrial Park, Bodwell Street, Avon, Mass. 02322 [357]

Multichannel thermal recorders have fast-heating thin-film print heads

Though thermal recorders are much neater than ink recorders, the slow heating that makes them fail when operating at high speeds has discouraged their use. But the Linearcorder Mark VII print head heats and cools so quickly that it prints under all circumstances. The head, which weighs only 0.3 g, will even print dot-matrix characters.



Watanabe Corp. of America, a subsidiary of Watanabe Instruments Corp. of Tokyo, uses the patented ceramic head on the WR 31001 family of recorders. The device uses thin-film technology, with components other than the ceramic consisting of an insulating material, heating element and a wear-resistant layer that touches the heat-sensitive paper. The low-wear layer gives the head a life of about 500 km, or about one year's writing time, says Edward P. Brooks, president.

The head's ceramic portion contains diamond dust and hydrogen, the latter being mixed in to increase conductivity and lower the weight, Brooks says. Its small mass permits the new material to dissipate heat quickly: rise time is 3 ms and fall time is 5 ms. The recorder will print at a high signal velocity even at high chart speeds, as is necessary when recording square waves. Because of rapid cooling, the recorder can print a solid block without burning through the paper.

Dot-matrix printing. The model 3101 prints the time, date, speed and elapsed time along the edge of the chart, using five-by-seven-dot-matrix characters. Additional information may also be printed by interfacing a computer with the recorder. A stepper motor gives a wide range of paper-drive speeds with a greater accuracy than competitive units, says Brooks. Speeds range from 0.05 to 500 mm/s, with an accuracy within 0.2%.

The pen motors are accurate to within 0.5%, with a frequency response from dc to 60 Hz at 4-cm amplitude, 120 Hz at 1-cm amplitude. The recorders have pen mechanisms with either ±20- or ±40-mm travel.

The WR 3101 family includes 2-, 4-, 6-, 8-, and 12-channel units. Each channel operates separately, with one signal input cable for each. The recorders may be rack-mounted either horizontally or vertically or placed on a table.

Recorders in the line range in size from a 12-lb unit measuring 430 by

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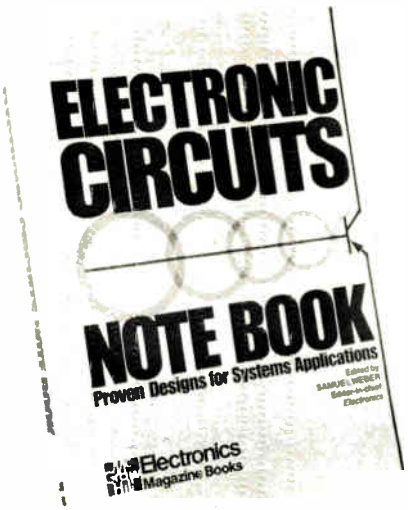

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Watanabe Corp. of America, 3188-D Airway Ave., Costa Mesa, Calif. 92626. Phone (714) 546-5344 [356]

Signature analyzer performs single-channel logic analysis

The LA-1000 system analyzer from the B&K Precision product group of Dynascan Corp. is a signature analyzer with a built-in volt-ohm-frequency meter and a single-channel logic-analysis feature. With its low price of about $1,750, the unit is designed for easy use by field technicians inexperienced in digital test techniques.

Its single channel of logic analysis is obviously not intended for software debugging or timing analysis in large systems, as are multichannel logic analyzers made by B&K and other firms. But B&K engineers feel that the single-channel capability will be useful in many applications. Teletypewriter gear and other systems employing serial digital communications over single lines or twisted pairs are examples. Probing a single node in a digital circuit is often valuable in troubleshooting.

Compared with multichannel analyzers, the logic analysis function of the LA-1000 is very easy to use. Once the mode switch is set, a total of six buttons—three on the LA-1000 itself and three on the attached probe control pod—are all that are required for logic analysis operation.

Capable of 20-MHz synchronous operation, the LA-1000 can handle both TTL or complementary-MOS logic in its logic analysis mode. A 256-bit memory permits storage of 16 pages of 16 bits each. State data formatted in hexadecimal code can be shown on an integral four-digit light-emitting-diode display, and an oscilloscope output is also provided for display of a 16-bit single-channel timing diagram.

In its signature-analysis mode, the LA-1000 displays signatures in standard hexadecimal coding. Features include an unstable-signal indicator for diagnosing intermittent failures and a self-test capability. Input signals need only be valid for 10 ns before the selected clock edge (setup time), permitting operation at higher clock rates than is possible with signature analyzers requiring longer setup times.

Also in the LA-1000 are an autoranging 30-MHz frequency counter and a digital voltmeter and ohmmeter. The autoranging meter is independent of other instrument functions and is controlled by a Rockwell PPS-4 4-bit microprocessor, displaying dc and ac voltage and resistance on a separate 3½-digit display. Dc and ac voltage can be measured to within 0.1% and 0.5% accuracy, respectively, while resistance is measured to ±0.3%. The frequency counter makes use of a custom MOS chip used in earlier B&K products. The analyzer is available now.

B&K Precision, Dynascan Corp., 6460 West Cortland St., Chicago, Ill. 60635 [355]

STD-bus system chassis offered by Mostek

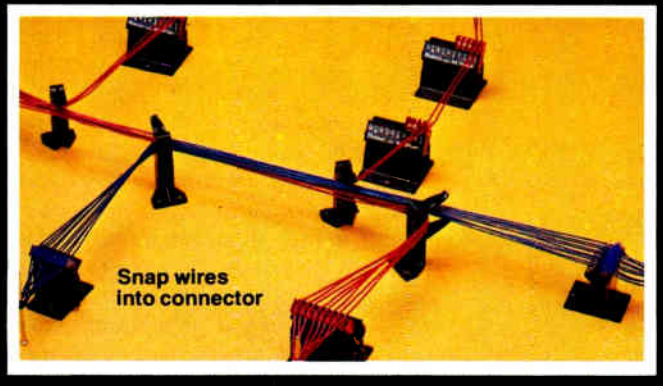
Mostek Corp. is unveiling the first members in a User Configurable series of general-purpose computer systems designed around STD-bus cards and housed in a low-profile, industrial-grade chassis. The series marks a new thrust by Mostek into the systems business and is intended to reduce development cycles by 9 to 18 months for STD-bus customers who would otherwise design and build their own computer enclosures.

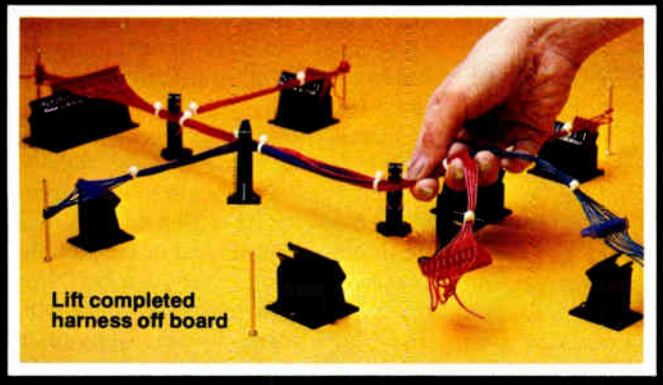
Targeted at original-equipment manufacturers and system integrators, the Matrix series of user-configurable products is a Z80-based board system using STD bus architecture and 4½-by-6½-in. cards. The series operates on M/OS-80, an operating system developed by Mostek for the Z80, which it second-sources. M/OS-80 will allow Matrix customers to use any CP/M-compatible application program.

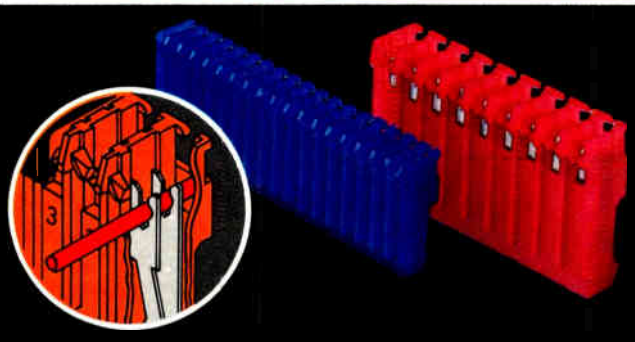
The goal of the Matrix series is to enable system designers to develop less expensive customized machines by giving them a selection of a wide range of standard hardware (such as STD-bus boards and disk memories) and software. The use of an integrated switching power supply reduces the size of the cabinet.

Initially, Mostek will offer two models. The 010 will come with power supply, 10 card slots, and a chassis with a space for a floppy-disk drive. The 100 will have the same features as the 010, plus a single-sided double-density 8-in. floppy-disk drive. Both models are available in either low-profile rack-mountable or table-

SLASH INSTALLED CONNECTOR COSTS 50% with PANDUIT® MAS-CON™ Mass Terminated System







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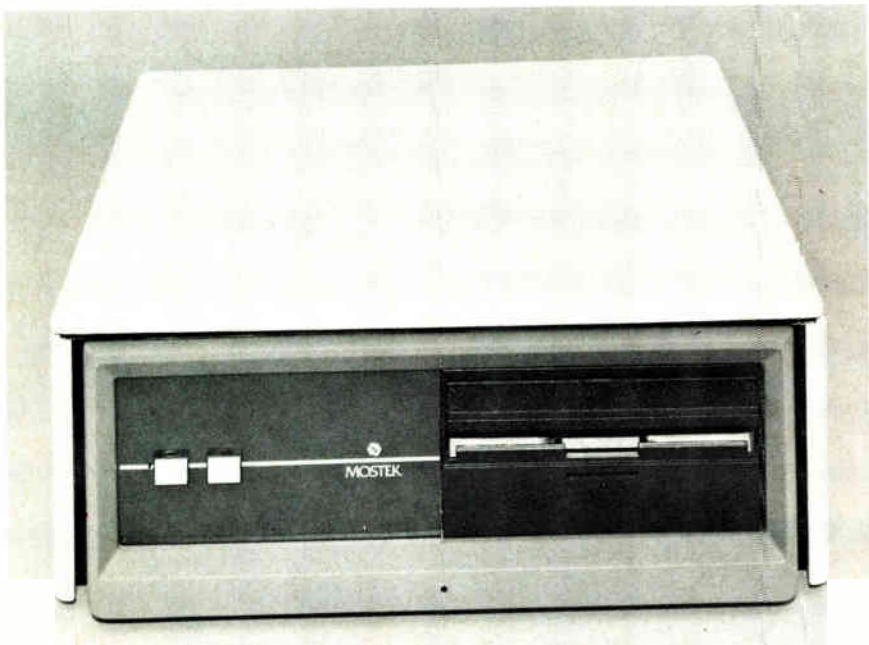
Circle 179 on reader service card



top versions, measuring 19 in. wide by a 0.75 in. high by 22.5 in. deep and 21 by 8¼ by 22.5 in., respectively. The system provides +5 V at 15 A, +12 V at 0.5 A, −12 at 0.25 A and +24 V at 3.4 A for internal components. Standard 115- or 230-V ac is required at either 50 or 60 Hz.

In quantities of one to nine, the 010 will cost $1,250 each, and the 100 will go for $1,750 each. The 100 is available now and the 010 will be ready for delivery in the final quarter. Future members of the Matrix family will include such features as: STD-bus boards (such as serial input/output, central processing unit, and memory cards); software; combinations of Winchester and floppy-disk drives; and networking capabilities.

Mostek Corp., Micro Systems Division, 1215 West Crosby Rd., Carrollton, Texas 75006. Phone (214) 323-6000 [352]

35-MHz programmable scope aims at production, inspection

Kikusui International Corp. is targeting U. S. production and inspection lines with a dual-channel programmable instrument. The 35-MHz bandwidth and 5-mV sensitivity of the model COS 5030PG is admittedly at the low end of scope performance for engineering and development. But the oscilloscope's combination of low price and numerous programmable features, as well as the resulting simplity of operation, should make it an attractive workhorse production or inspection unit, the company believes.

Although pricing is not final, the basic scope is in the $3,600 range, and a configuration with all options boosts it to about $6,000. The options include remote and step controllers, probe selectors, memory, and interface and make it possible to operate the instrument with any combination of computer or manual control, says William White, a marketing executive for the firm.

The Kikusui scope's programmability covers about 95% of its switches and controls for waveform display. Since it can be controlled either manually, with a step controller, or with a computer, the result "is an effective labor-saving instrument for production-line inspection," says White. An interface option sets the scope up for connection to the IEEE-488 instrumentation bus for computer control.

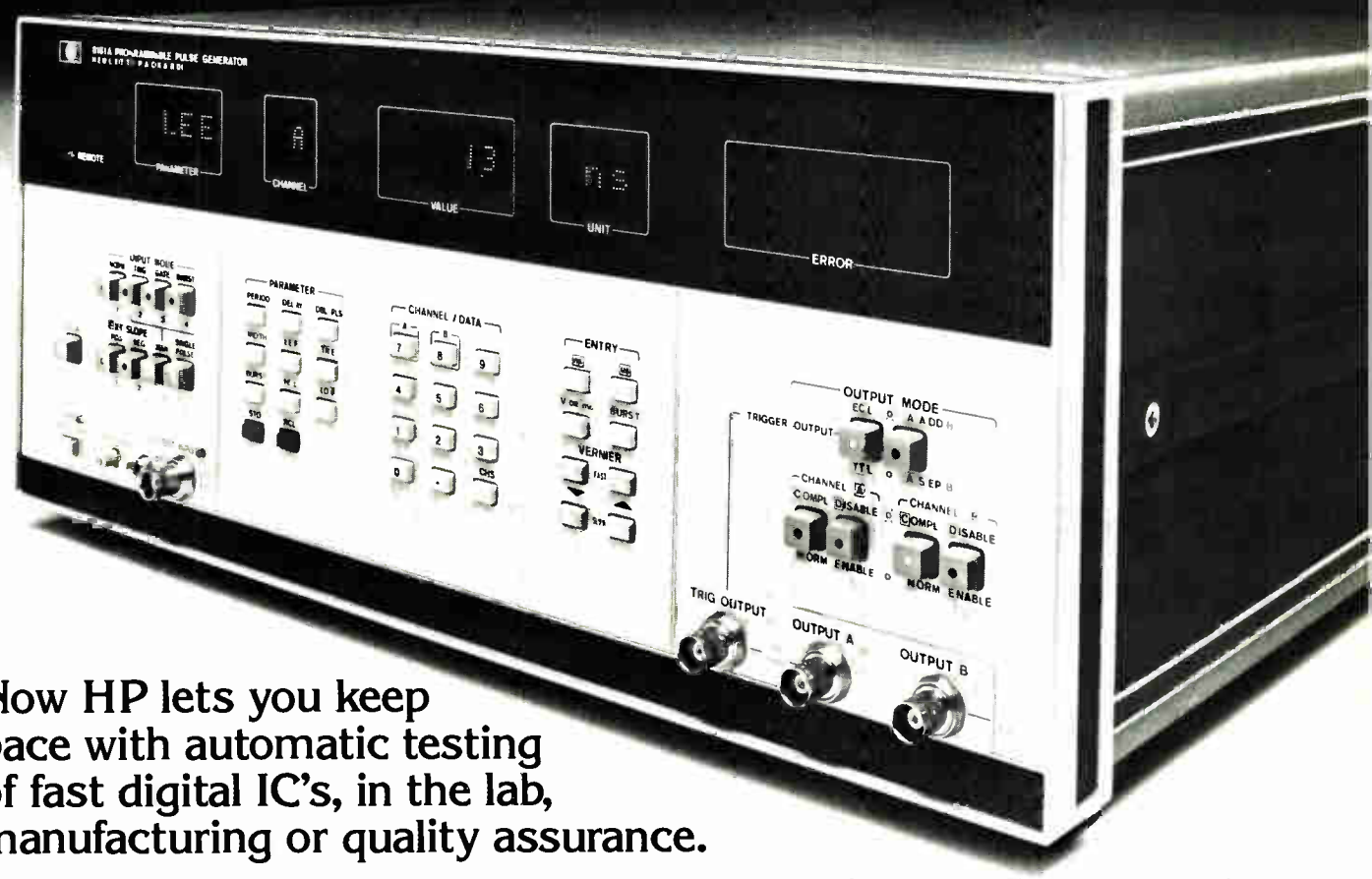
Among its programmable vertical functions are sensitivity, input coupling, mode, and position. Horizontal A and B sweep are programmable; continuous adjustment of the variable A sweep is possible. Six levels of trigger control are also programmable on the COS 5030 PG, as are trigger source, coupling, slope, and level. Other programmable functions offered are delay time and intensity.

When the oscilloscope is linked with a remote controller and memory unit, up to 96 steps may be performed. With the step-control option, these steps stored in the remote controller and memory can be automatically incremented up or down. The time interval for this stepping is adjustable for approximately 3- to 30-second periods. For manual operation, control knobs are located on both the main instrument and the remote unit. In this mode, delay-time positioning can be set at 5% to 95% of the main sweep.

Option combinations. The portable instrument may also be rack-mounted; it is designed for simple installation with a minimum of connections between units. The cathode-ray tube has a 5.5-in.-square screen of the dome-mesh, post-acceleration type, with a parallax-free internal graticule. The principal option combinations with the programmable instrument would be a remote and step controller, a memory unit and step controller, or an interface and a personal computer.

Much of the final design thinking for the U. S. unit comes from suggestions offered by Japanese manufacturers of video-tape and video-disk equipment who use similar oscilloscope systems for inspection

It's fast. It's programmable. Meet HP's new 8161A Pulse Generator. 1.3 ns variable transition times, 100 MHz.



Now HP lets you keep pace with automatic testing of fast digital IC's, in the lab, manufacturing or quality assurance.

The new Hewlett-Packard 8161A offers a flexible, easy-to-use solution to the problem of testing fast high-technology circuits such as 10K ECL logic and advanced Schottky devices. And, it's the first HP-IB programmable pulse generator with variable transition times down to 1.3 ns, allowing you to evaluate high-speed logic circuits thoroughly.

Features you'll appreciate — now, and in the future. Fast, clean 100 MHz, 5V pulses are just part of the 8161A's story. With 1-2% basic timing accuracy over a wide temperature range plus a one-year recalibration period, the 8161A gives you quality measurements while it saves on maintenance time and expense. Two complementary outputs are standard. And, you can get an optional, fully independent, second output channel that lets you generate complex waveforms in A + B mode. External operating modes and counted burst further enhance the 8161A's flexibility.

A real time saver on the bench. When used as a bench instrument, this new HP Pulse Generator's easy, microprocessor-controlled operation will simplify most test setups. With its high accuracy, no time-consuming 'tweaking-in' is required. Storage of nine complete parameter setups for quick recall simplifies operation. And outstanding repeatability means reliable measurement results.

Ideal for fully automated testing. In an R&D or production system, the versatile new HP 8161A is easily integrated using HP-IB, which allows automated testing of advanced semiconductor devices and system modules. Besides saving time and increasing throughput, the 8161A will eliminate errors associated with manual measurements. You'll get reproducible results over long periods of time without the necessity of constant system monitoring or correction loops.

Fully detailed information — yours for the asking. For comprehensive technical data and application note, write: Hewlett-Packard, 1820 Embarcadero Road, Palo Alto, CA 94303. Or call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

081 7

HP-IB SYSTEMS HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.

HEWLETT PACKARD

Circle 181 on reader service card

Wescon/81

tasks. After the programmable system has been set up by a test engineer, "it can be operated by pushing one button," White claims. Small quantities of production units will be ready in 60 to 90 days.

Kikusui International Corp., 17819 S. Figueroa St., Gardena, Calif., 90248. Phone (213) 515-6432 [359]

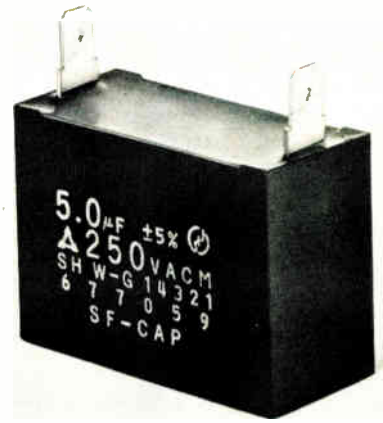
Dry-type metalized-film capacitors lower cost of self-protection

The SF dry-film capacitor series from the Electronic Components division of Panasonic has a self-protection feature built into the rolled metalized film and dielectric. The 0.5-to-60-μF, 360- and 400-V capacitors thus increase reliability in motor circuits, ballasts, and other ac applications. They also reduce weight and size in comparison to other self-protecting capacitors, says the manufacturer.

The metalized-film electrodes are separated into many small segments connected in parallel. If breakdown of the dielectric occurs, the affected segment is electrically disconnected from the rest—a fuse link in the metal film is blown—and the unit continues to function at a slightly reduced capacitance. Because the paralleled elements are very small relative to the total capacitance, the drop in value is unlikely to affect the unit's performance.

The self-protection feature lends itself to conventional mass-production techniques, allowing the firm to offer added reliability at prices very near those of standard unprotected dry-type metalized-film capacitors. The Panasonic parts range from $1 to $5 apiece in quantity. The expense and the bulk of the added internal-protection devices of conventional self-protected capacitors is avoided; size and weight are reduced by 30% to 50%.

The operating temperature range of capacitors in the SF series is −55°



to +85°C. Delivery takes 14 to 16 weeks.

Panasonic, One Panasonic Way, Secaucus, N. J. 07094. Phone (201) 348-5206 [363]

500-W switchers near $1 per watt

ACDC Electronics is using its submodular architecture in a new line of 500-W switching power supplies to speed deliveries and to lower prices.

The architecture breaks a power supply into three segments, and the division of Emerson Electric Co. has already used it for two years in switchers with outputs below 300 W and above 1,000 W. The RSF series is

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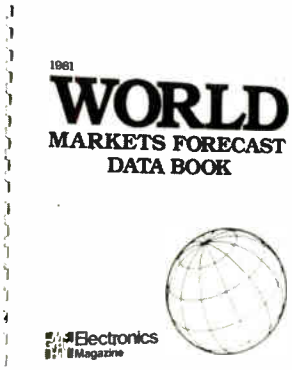

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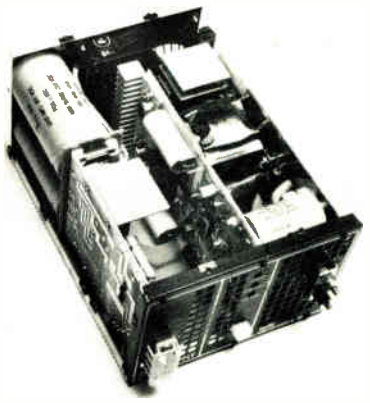


designed to fill part of that gap.

The new switcher family, which offers one to four outputs, uses recently developed large-scale integrated inverter-control circuitry, power semiconductors, and fault- and error-detection chips to reduce the number of components by 20%.

By using revised versions of the existing input, converter, and output modules, ACDC is aiming to provide supplies with a short lead time, high reliability, and low development costs. Small-quantity shipments will begin in this month, and production deliveries will start during the first quarter of next year, with deliveries taking six to eight weeks. Single-output units start at $595, with quad units listing for $745, each in single quantities. In large volumes, pricing is near $1 per watt.

The RSF single-output models have current ratings of 18 to 100 A at 2 to 28 V dc. Additional outputs range from 5 to 28 V at 2 to 20 A. The RSF 100 series of dual-output switchers combines any two voltages from 2 to 28 V at 14 to 80 A with a total power output of 500 W.

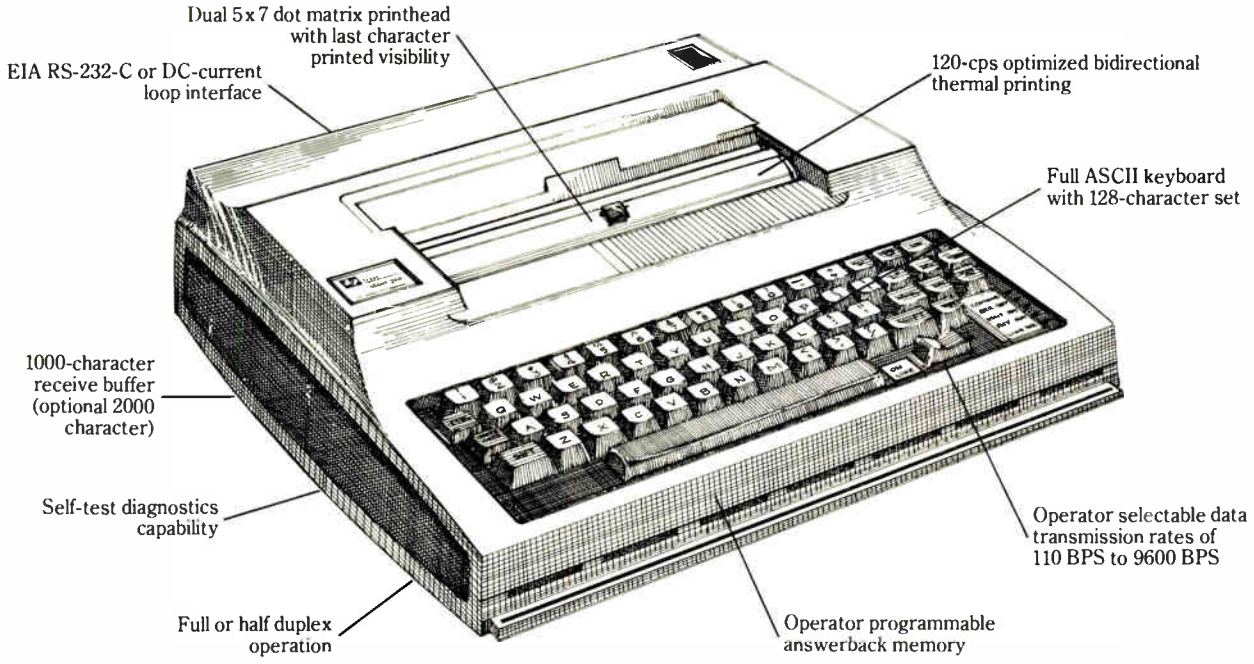
Ripple output is a maximum of 10 mV peak to peak. Regulation is to within 10 mV. Input can be 90 to 132 or 180 to 246 V ac, or optionally 165 to 250 V ac. The units are 60% to 80% efficient, depending on the model. Full output is achieved at 50° C, derating to 70% at 71° C.

Overvoltage protection for all outputs, short-circuit protection, and soft starting and overheating protection with automatic reset when nor-

The Task Master.

783 KSR

Keyboard Send-Receive Data Terminal



Ideal for commercial applications, TI's *Silent 700** Model 783 KSR Data Terminal can master your workload with high-quality, efficient thermal printing. Offering a variety of user-oriented standard features and options, the virtually silent 783 KSR takes less work space while it maximizes printing throughput. That's why the versatile 783 KSR was designed to handle your most demanding printing tasks.

TI is dedicated to producing quality, innovative products like the 783 KSR Data Terminal. TI's hundreds of thousands of data terminals shipped worldwide are backed by the technology and reliability that come from 50 years of experience, and are supported by our worldwide organization of factory-trained sales and service representatives.

For more information on the 783 KSR, contact the TI sales office nearest you, or write Texas Instruments Incorporated, P.O. Box 1444, M/S 7884, Houston, Texas 77001, or phone (713) 373-1050. In Canada, write Texas Instruments Incorporated, 41 Shelley Rd., Richmond Hill, Ontario L4C 5G4, or phone (416) 884-9181.

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Circle 185 on reader service card

mal temperatures are regained are standard. Options include outputs indicating ac power failure and outputs out of tolerance and a remote-inhibit input.

ACDC Electronics, Products Marketing Department, 401 Jones Rd., Oceanside, Calif. 92054. Phone (714) 757-1880 [360]

Saddle joint extends edge connectors

Responding to a special request for an extremely long printed-circuit connector, Viking Connectors is using a new concept throughout its line of printed-circuit–board edge connectors. Called a saddle connector, it can double the 50 or so maximum positions previously possible by using a bonded U-shaped support member that joins two connector bodies. The result is a rigid double-length edge connector.

Interest in longer printed-circuit connectors is not rare, maintains Viking—demand for them is growing as an efficient solution for connecting computer cards to a backplane or motherboard. In the past, extending connectors to gain positions has caused either the board or the connectors themselves to warp. Another way to get extremely long connections is by assembling modular types end to end. However, manufacturing costs tend to be higher with this method. With the new bonded support, warpage does not occur, Viking says. The saddle joint is strong enough to withstand a force of 150 lb.

Since the saddle concept will be applied with all standard Viking edge connector types, all varieties of contacts will also be available. Viking has already produced saddle units with 79 and 80 positions and can build them with up to 100 dual positions on 0.125-in. centers.

The price of the saddle assembly adds $1 to the cost of a pair of connectors, in quantities of 1,000 to

2,499. Delivery takes 8 to 10 weeks. Viking Connectors Inc., 21001 Nordhoff St., Chatsworth, Calif. 91311. Phone (213) 341-4330 [362]

Software configures PROM programmer

The Z-800 is a small portable programmer for erasable programmable read-only memories that handles, without the need for personality modules, 2508, 2528, 2532, 2564, 2556, 2716, 2732, 2732A, 2764, and 2728 n-channel MOS E-PROMs. The software-configurable unit will accommodate future E-PROMs through software updates.

The programmer has an RS-232-C interface that allows data to be downloaded from a computer or development system; it adjusts automatically to transmission rates from 110 to 1,200 b/s. Alternatively, it can copy a master E-PROM mounted in one of its two zero-insertion-force sockets. The generic number of the E-PROM is keyed in on a hexadecimal keyboard; the master and the copy can be of different types.

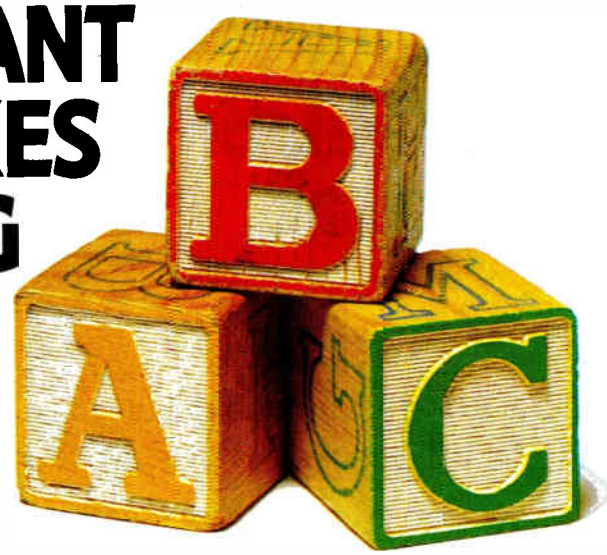
The user may define portions of the master that are to be copied; he may change the locations of those blocks in the copy, thus inserting or deleting data. Changes may be specified in data at up to 16 locations during the duplication process.

An E-PROM may also be programmed without a master copy, one location at a time, using the keyboard. An address and the data at that address appear on a hexadecimal display. The unit lets the user step through the program listing on the copy.

The $1,500 Z-800 E-PROM programmer measures 9.6 by 4.4 by 1.6 in. and draws 600 mA at 8 to 12 V; a 115-V ac power pack is included. Deliveries take up to four weeks.

Quantec Systems Inc., P. O. Box 832, Station A, Scarborough, Ont. M1K 5C8, Canada. Phone (416) 291-8761 [361]

RACAL-VADIC'S FULL V.22 COMPLIANT MODEM MAKES COMMUNICATING AS SIMPLE AS...



V.22 Means Four Times the Speed!

Racal-Vadic, world leader in low and medium speed modems, is in full production on Model 1222, a V.22 compliant modem which operates full duplex at 1200 bits/second over 2-wire dial-up or leased lines. Furthermore, it offers all three V.22 alternatives... A, B, and C.

The 1222 makes it possible for terminal users to transmit and receive data four times faster, with no change in protocol, by merely replacing a V.21 300 bps modem with the new Racal-Vadic 1200 bps full duplex unit. No longer will data terminals with 1200 bps capability have to settle for 300 bps operation!

Racal-Vadic, World Leader in 1200 bps Full Duplex Technology

Racal-Vadic is by far the world's leading manufacturer of 1200 bps full duplex modems. No wonder! Racal-Vadic invented 1200 bps 2-wire full duplex transmission in 1973, and has a worldwide installed base of over 125,000 of these modems.

There are a number of reasons why the Racal-Vadic 1222 is the most versatile V.22 compliant modem you can buy. First, if offers all three alternatives... A, B, and C. The inclusion of alternative C means that the 1222 will operate with any terminal at ALL standard asynchronous speeds to 1200 bps, plus split speed (300 bps in one direction, 1200 bps in the other), and overspeed as well.

Also, displays and built-in diagnostics are second to none for pin-pointing faults in the entire data network. Packaging is versatile, too. The 1222 is available in a compact desk top cabinet for remote use, or for central computer sites. Up to seven 1222 modems can be housed in a 8 3/4-inch high rack-mounted card nest including power module.

Further, the 1222 is backed by Racal, worldwide leader in data communications.

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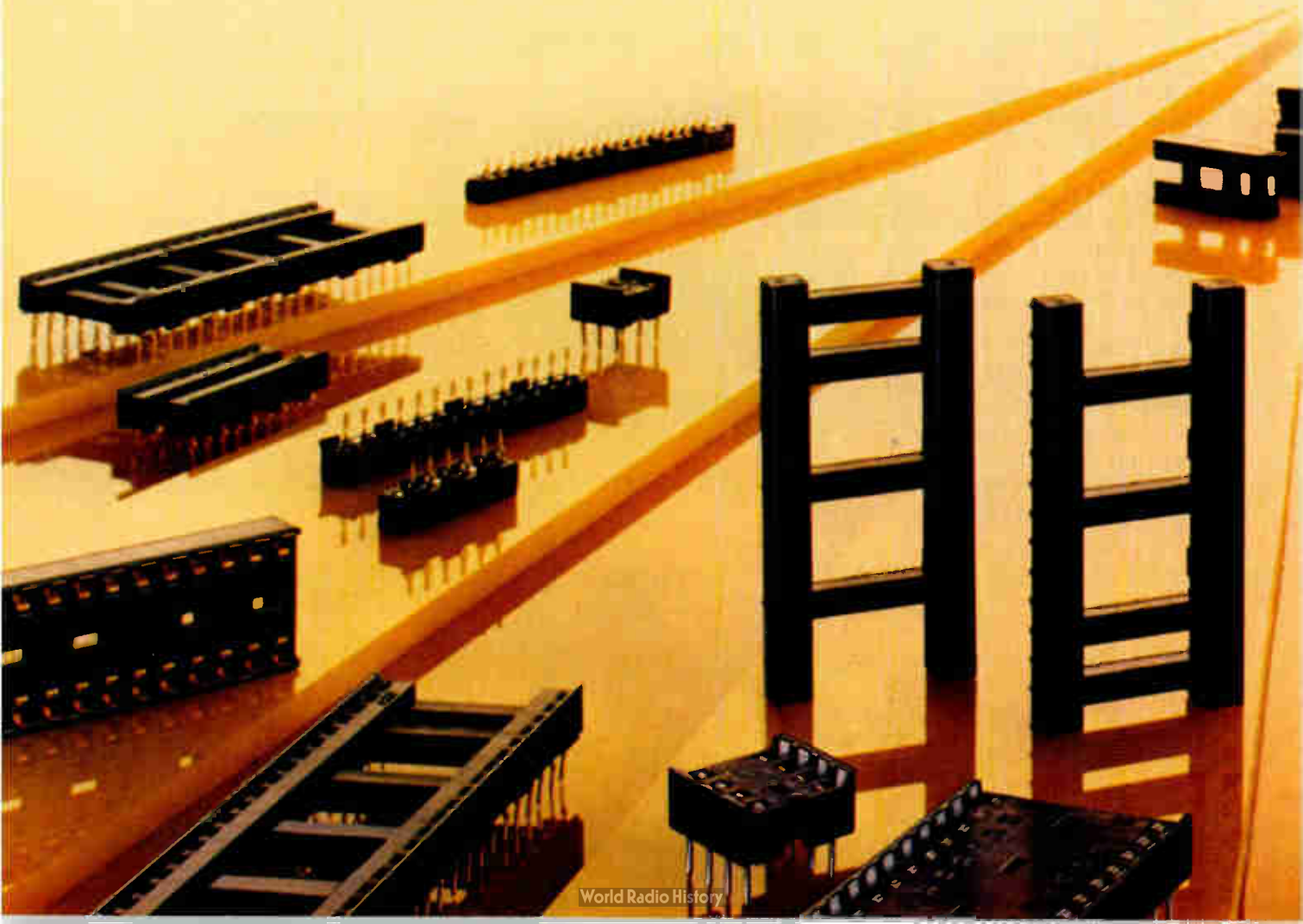
Circle 113 on reader service card

Our lowest profile DIP sockets even have MIL-S-83734 approval.

That's one advantage of our DIPLOMATE sockets. There are more.

They have an anti-overstress design to prevent socket damage. Their contacts are anti-wicking and anti-bridging. Their optional leg retaining detents help increase your productivity. And the ladder housing version eases cleaning and viewing of circuit traces after insertion.

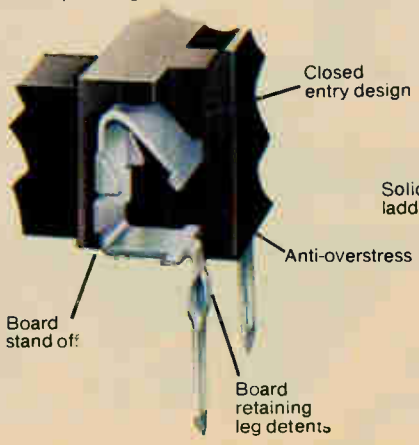
You can't find a higher qualified low profile DIP socket.

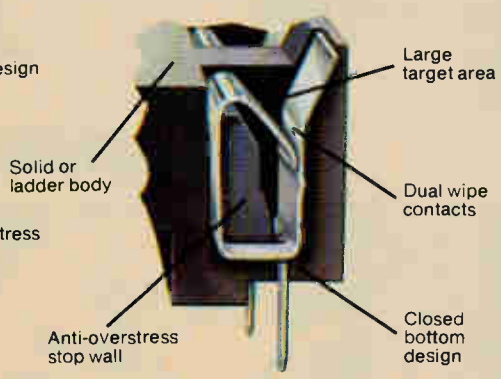


AMP Facts

DIPLOMATE SL Sockets
Sizes: 8 through 40 positions
Profile: .160"
Engaging force: 340 grams max.
Separating force: 25.5 grams min.

DIPLOMATE DL Sockets
Sizes: 6 through 40 positions
Profile: .175"
Engaging force: 340 grams max.
Separating force: 14 grams min.

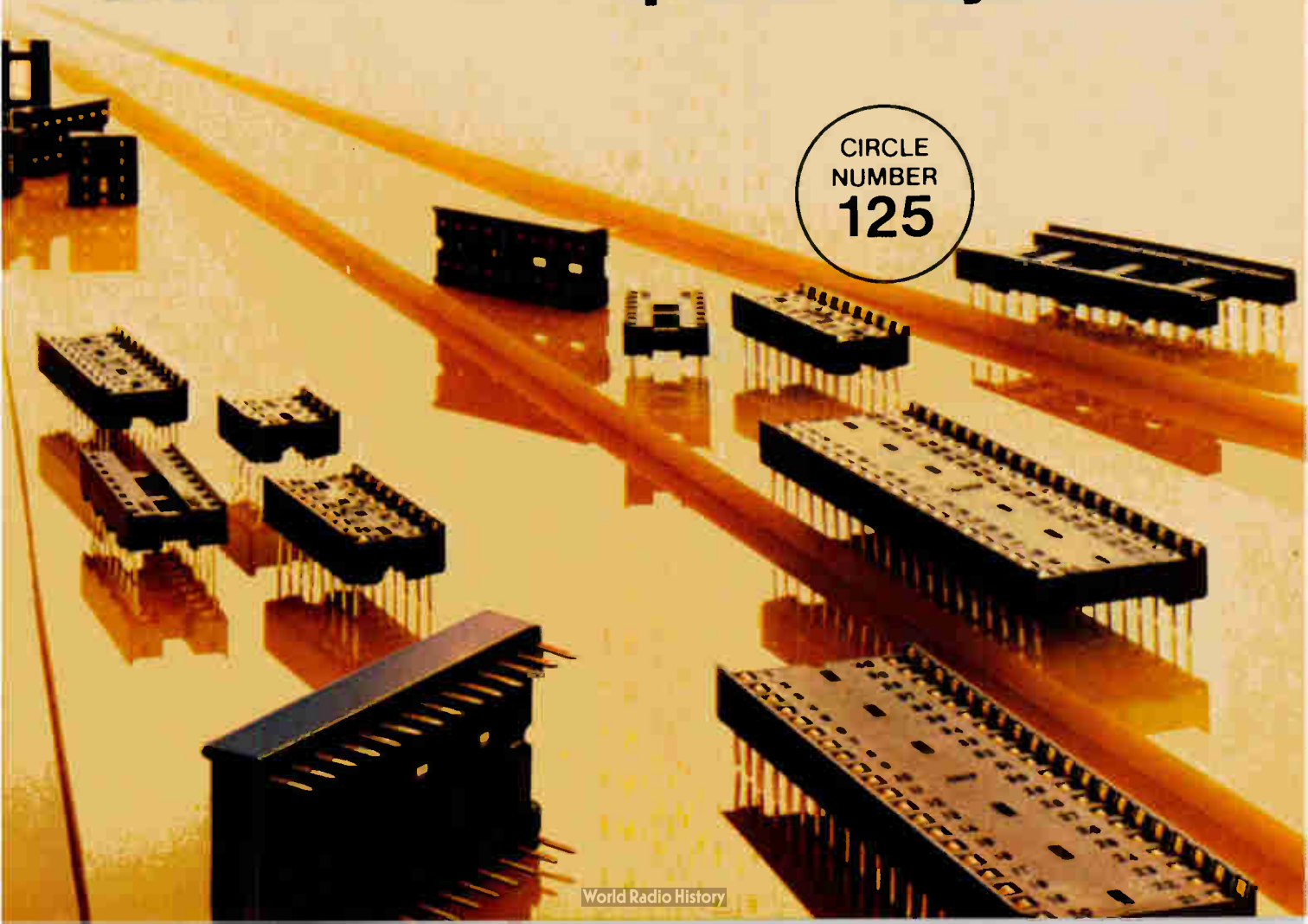




For a free sample, call the AMP DIP Socket Information Desk at (717) 780-8400.

AMP Incorporated, Harrisburg, PA 17105.

AMP means productivity.



CIRCLE NUMBER 125

THIS NEW DATA I/O 6800 FAMILY TESTER CAN SAVE YOU A LOT MORE THAN IT COSTS.

Reject bad devices before they get into your production line. Everytime a faulty microprocessor or peripheral chip slips into one of your products it costs you profit in troubleshooting and replacement.

With the new Data I/O Model 1500A, you can set up a low-cost incoming inspection program to detect faulty 6800 family devices before they get loaded into boards.

Comprehensive testing detects problems in 6800, 68A00, 68B00, 6802, 6808, 6810, 6821 and 6850 devices. The Data I/O 6800 family tester performs a full-functional test on devices under worst case load and supply voltages at real time speed in less than one second.

The test may reveal, for example, that the clock is inactive, or a line on the address bus is not working, or the internal RAM is defective.

Easy set-up and operation. Simply plug the correct test adapter into the tester and you're ready to begin. No need to hire skilled personnel to write test programs, specify test vectors or parameters. It's all contained in a pre-written test sequence.

To operate, simply place the device in the socket and press the button. A green light identifies a functional part. A bad part triggers a three-digit code, which identifies the specific problem.

Reduce parts shortages and ease device returns. You don't have to reject an entire lot because of a few bad components.

With the 6800 family tester you can quickly and efficiently screen all devices to make the best use of the components you have.

Most device vendors require proof of failure before they will accept rejects. The failure code provided by the 6800 family tester identifies the problem and will speed up the process of returning faulty parts.

Backed by Data I/O's commitment to quality and performance. We've put the same care and engineering skill into the Model 1500A that we put into our entire range of PROM and logic device programmer products. The Model 1500A has been evaluated by device manufacturers and recognized as a viable test method. Each unit is backed by Data I/O's worldwide network of sales and service personnel.

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DATA I/O 6800 FAMILY TESTER

Circle 192 on reader service card

C-MOS PROM density hits 16-K

Polysilicon-fuse programmable read-only memories operate on 25 mW/MHz, typically, and stand by on 500μW

by James B. Brinton, Boston bureau manager

The first 16-K complementary-MOS programmable read-only memories are now available from the Semiconductor Products division of Harris Corp. Harris is alone in this market, having already introduced 1-K and 4-K PROMs using low-power C-MOS and polysilicon-fuse technology [*Electronics*, Aug. 14, 1980, p. 36].

Although there are no other C-MOS PROMs on the market, both 4-K and 16-K C-MOS erasable PROMs are available. According to Bruce G. Grieshaber, Harris's C-MOS product marketing manager, even though the Harris part's cell is about 20% larger in area than E-PROM cells, Harris PROMs are competitive in price.

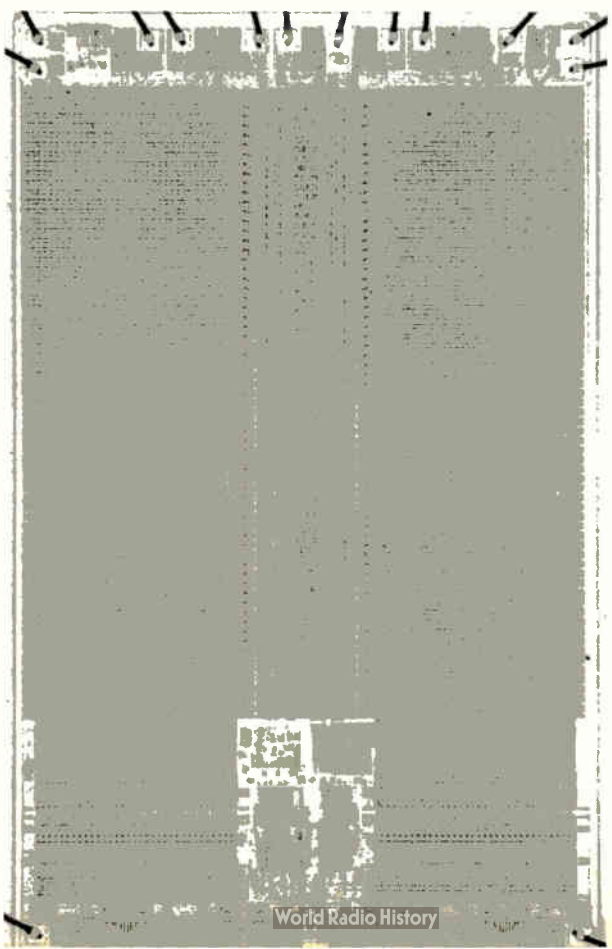
But for now, it appears that for low-power applications where PROM rewrite is not necessary, Harris' new units are king. The HA-6616 is organized as a 2-K-by-8-bit part with a byte-wide pinout, uses a single +5-V supply, is compatible with standard TTL inputs, and has enough drive capability to fan out to eight low-power Schottky TTL inputs. Access time is not as short as that of bipolar PROMs, but it is a respectable 125 ns typically and 200 ns at most. The HA-6646 is similar, but it is a 4-K-by-4-bit part.

Grieshaber says that C-MOS PROMs will be one of Harris' major thrusts for the near future, and that the 16-K device is to be followed with 32- and 64-K PROMs within about a year [*Electronics*, July 14, p. 33].

A major advantage of the new PROMs is their low power consumption. Standby drain is typically 50 to 100 μW and the units are rated at 500 μW maximum. Operating power drain is typically 25 mW/MHz with the maximum rating 50 mW/MHz. Harris recommends the low-power parts for applications like hand-held instrumentation and communications systems, remote data-acquisition and data-processing systems, processor-control storage, and sometimes as a replacement for synchronous logic.

Address latches. The synchronous PROMs also are designed to interface gracefully with microprocessors, notes Grieshaber, thanks to the provision of on-chip address latches and a separate output-enable pin. This feature should especially simplify any implementation using a bus structure with multiplexed addresses and data. The synchronous design approach also pays off in reduced power consumption when compared with asynchronous units.

Although C-MOS is a recognized low-power technology, it is possible to sink a good deal of current if a C-MOS IC is poorly designed. It was partly to keep power requirements down that Harris decided on a synchronous design. Grieshaber says it also improves speed.



In a synchronous PROM, the latched address register stores address information temporarily. Simultaneously, fuse-read current is turned off. Thus, not only is the read current almost independent of the number of fuses blown in the PROM, but it flows only when the PROMs' output enable pins are activated. If the design were asynchronous, current would be continually running through all intact fuses, raising standby dissipation to as much as 10 mA, says Grieshaber.

In layout, the new PROMs are much like their 4-K predecessors. The major change is in a move from a 3.5- to 2.5-μm geometry and a generally tighter layout. As a result, says Greishaber, the Harris division was able to reduce cell size from 2.25 square mils on the 4-K

New products

PROM to only 0.795 mils² on the new 16-K devices.

With the smaller cell size, the company was able to keep die size very close to that of the 4-K device. The older unit was 137 by 197 mils for an area of 26,989 mil² and the 16-K devices are only 139.8 by 232 mils for an area of 32,434 mil², an increase of only about 17%. The raised packing density is due in part to a vertical npn-transistor design pioneered in the firm's 1-K C-MOS PROMs. This helps control the size of the C-MOS transistors that must carry the fusing current, one of the key factors limiting density. In Harris's C-MOS PROMs, the npn transistor operates in an emitter-follower configuration, amplifying the fusing current. A direct contact from the polysilicon fusable links to the n^+ emitter is made in Harris' process. The contact helps reduce cell size by letting the fuse be placed directly over the cell transistor.

To keep programming current and voltage requirements low, Harris has left an opening in the silicon dioxide passivation layer above each fuse. As a result, less heat is lost in surrounding materials as a fuse is blown, and, adds Grieshaber, the oxide that forms as the fuse material vaporizes helps maintain high resistance at the site of the blown fuse.

As do some other makers, Harris includes test fuses to be blown and checked during processing, and as a final test at outgoing inspection, Harris also includes circuitry for testing row and column decoders. Thus, a user is warranted in a fair degree of faith that the PROMs will program and read out properly.

The units are available operable over the −40° to +85°C industrial temperature range and the military −55° to +125°C range. The package is a standard 24-pin dual in-line ceramic package.

Introductory price in 100-unit lots is $65 for the HA-6616 and -6646. Samples should be available by October or November with pre-production quantities due in January.

Harris Corp., Semiconductor Products Division, P. O. Box 883, Melbourne, Fla. 32901. Phone (305) 724-7000 [338]

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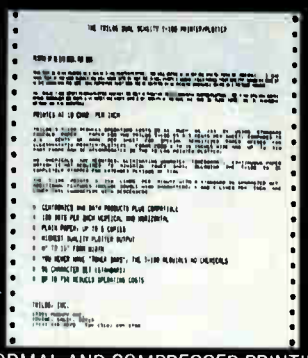
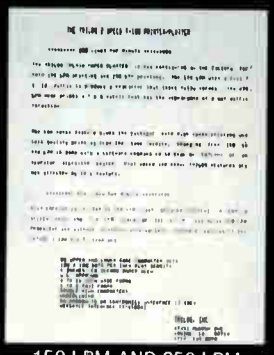
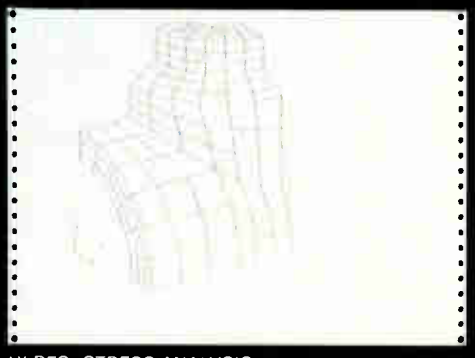


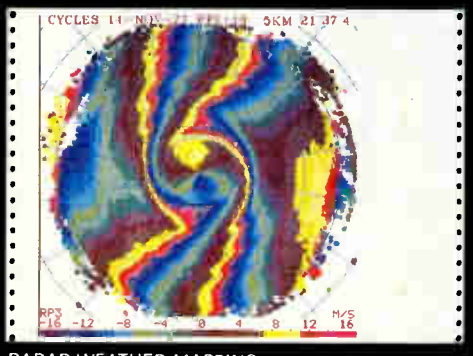
NORMAL AND COMPRESSED PRINTING



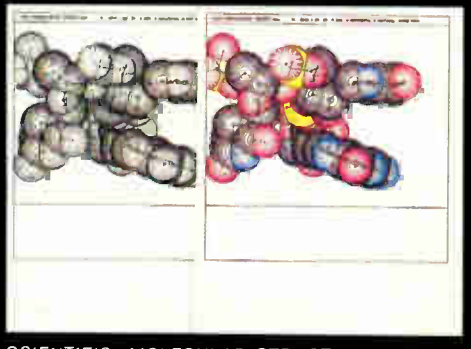
150 LPM AND 250 LPM



HI RES. STRESS ANALYSIS (PDA Eng.)



RADAR WEATHER MAPPING



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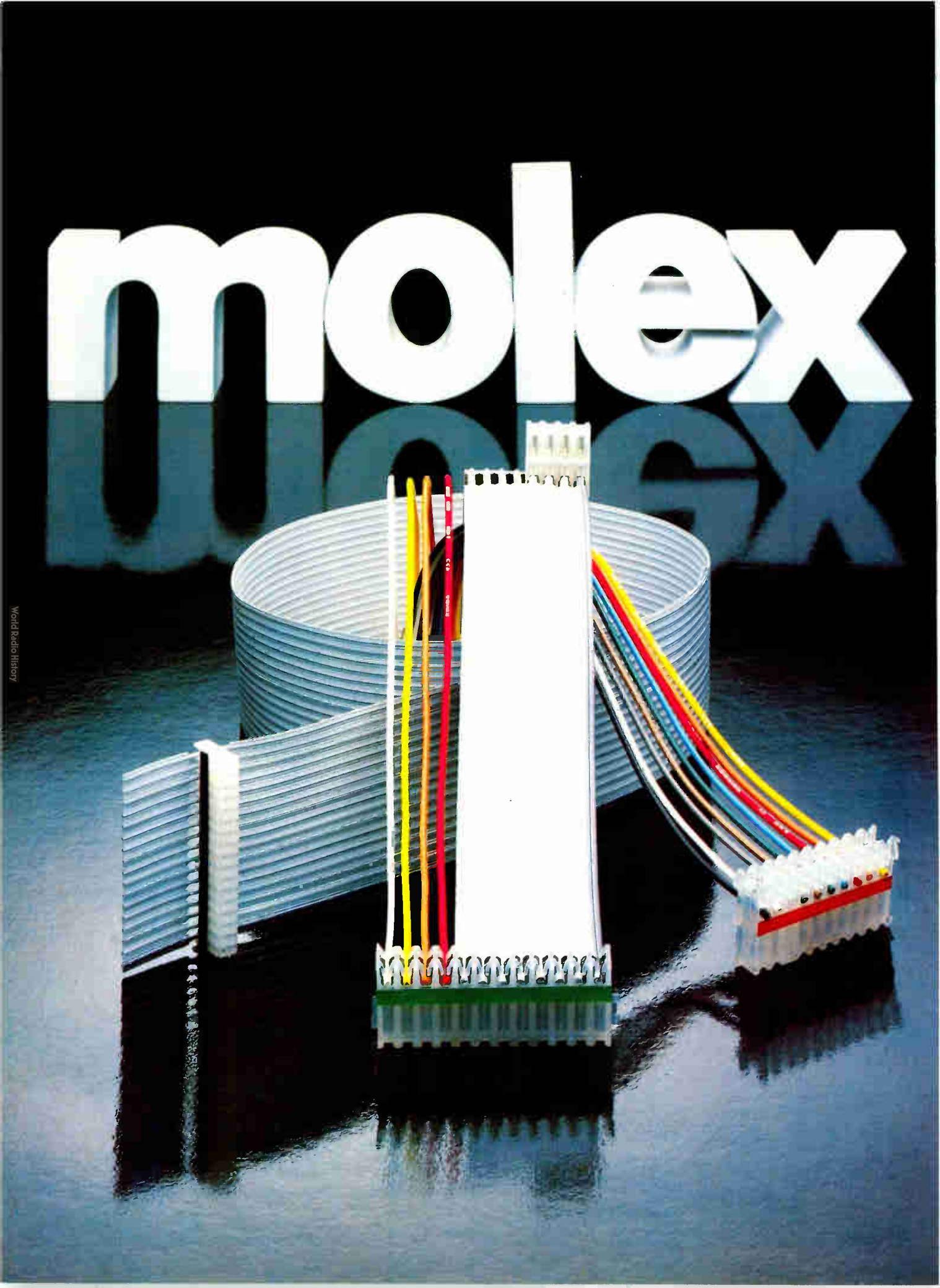


For mass termination component cost savings and applied labor reductions:

Molex has the answer.

Molex is the only manufacturer that offers cable systems on five center lines.

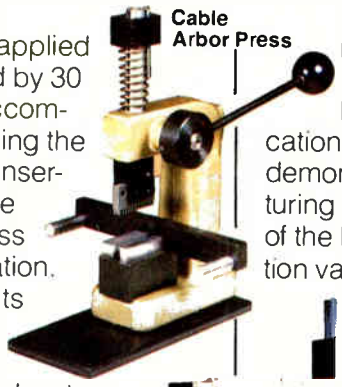
If your application calls for ribbon cable, discrete wire, or a combination of both in the same connector, Molex* Jet-Flecs* insulation displacement connectors can provide a complete system to meet your requirements on .050" (1.27mm), .098" (2.5mm), .100" (2.54mm), .156" (3.96mm) and .200" (5.08mm) center applications.

The photo depicts harness and non-harness board .156" and .100" center connector versatility. What the photo cannot show is the vast selection within the Molex system including 3 reliable contact designs.

Jet-Flecs .156" connectors accept wire gauge sizes from 18-28 AWG and Jet-Flecs .100" connectors accept 22-28 AWG. The Jet-Flecs connectors are drop-in replacements for standard KK* crimp products. There is no need to redesign your present product or application to utilize the advantages of the Jet-Flecs system since the connectors will mate with Molex KK headers accepting round or square pins.

Cost savings up to 40%

When using insulation displacement, your applied costs are lowered by 30 to 40%. This is accomplished by replacing the strip, crimp, and insertion steps with one simultaneous mass termination operation.



Cable Arbor Press

The components and cable are only half the system. The big advantage Molex offers is the complete range of application tooling. This equipment ranges from single wire hand tools to fully automatic assembly machines.

Molex's application equipment is in two main categories, cable assembly and discrete wire assembly.

For cable termination, an arbor-type press is available and a semi-automatic terminator for higher production rates.

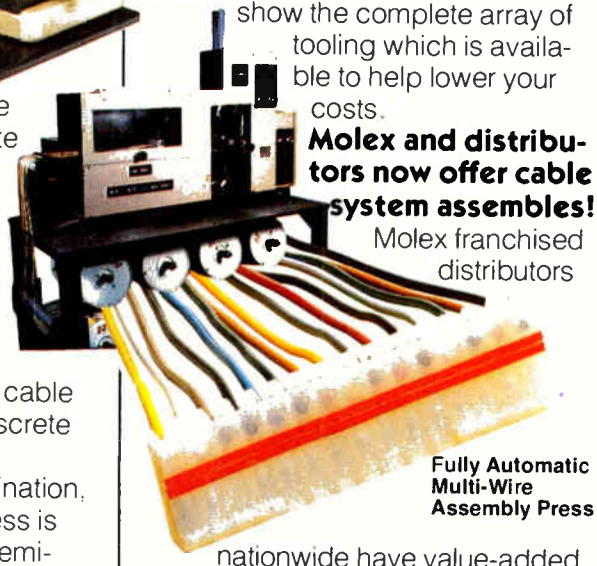
Harness Board Assembly Tool

Discrete wire termination can be accomplished with the use of an arbor-type press, a semi-automatic single wire terminating machine, a harness board assembly tool (which is compatible with your present harness board), or a fully automatic multi-wire assembly press.

Many of these unique application tools are available for demonstration in your manufacturing facility. Or, if you choose, one of the Molex equipment demonstration vans can visit your facility and show the complete array of tooling which is available to help lower your costs.

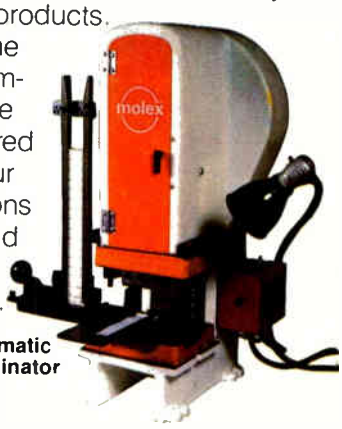
Molex and distributors now offer cable system assembles!

Molex franchised distributors nationwide have value-added equipment to manufacture your systems quickly and economically with stock products.



Fully Automatic Multi-Wire Assembly Press

High volume OEM assemblies can be manufactured to meet your specifications and shipped directly from Molex.



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Circle 197 on reader service card

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5V	40A	SK5-40
12V	16.8A	SK12-16.8
15V	13.4A	SK15-13.4
24V	8.4A	SK24-8.4
28V	7.2A	SK28-7.2
SIZE: 2"H X 4.88" W X 13"L		

$250
200 WATTS

OUTPUT	VOLTS	AMPS
#1	5V	20A
#2	12V	5A
#3	– 12V	3A
#4	5V, 12V, 15V, or 24V. USER SELECTABLE	3.5A
SIZE: 2"H X 4.88"W X 14"L		
MAX OUTPUT POWER: 150 WATTS CONTINUOUS, SUM OF ALL OUTPUTS		
150 WATTS - 4 OUTPUTS THE UNIVERSAL SHQ-150W		

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VOLTS	AMPS	MODEL
5V	10A	SD5-10
12V	4.2A	SD12-4.2
15V	3.4A	SD15-3.4
24V	2.1A	SD24-2.1
28V	1.8A	SD28-1.8
SIZE: 2"H X 4.88"W X 6.25"L		

$170
100 WATTS

VOLTS	AMPS	MODEL
5V	20A	SF5-20
12V	8.4A	SF12-8.4
15V	6.7A	SF15-6.7
24V	4.2A	SF24-4.2
28V	3.6A	SF28-3.6
SIZE: 2"H X 4.88"W X 10"L		

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Circle 200 on reader service card

Industrial

Motor controller is programmable

8088-based unit allows manufacturing line to handle several different workpieces

Taking aim at the wear-prone cams, clutches, and limit switches that define and control a fixed sequence of motion at a factory work station is the 2184 digital servo controller from the Modicon division of Gould Inc. Because it is programmable and can be digitally linked to other factory controllers, its makers claim that the new servo controllers will increase throughput and add flexibility along a manufacturing line. With it, operations can be changed instantaneously, under computer control, instead of taking the hours or even days typically needed to reconfigure a conventional transfer line. In addition, the 2184 keeps track of malfunctions along the line and responds by taking corrective action or shutting the equipment down, if necessary.

Without a programmable controller, a transfer line typically carries one type of workpiece, which arrives at a work station for one specific operation. With a controller, a more efficient scheme is possible: several types of workpieces can be placed on one transfer line, their sequence known by the controller, and the operation at each station can be modified for the individual workpiece. A separate programmable digital controller at each work station can store a different program for each part, calling it up as needed. The 2184, for example, can at present store 12 such programs, and Modicon says it will expand this capacity to 50.

The package contains an 8088 high speed central-processing unit, battery-backed memory, power supply and 0-to-10-v standard servo-drive interface. Designed to control

electric and hydraulic drives, it has eight inputs and eight outputs for gages and switches.

In designing the 2184, Modicon departed from practice followed in its standard factory-programmable controllers. "The technology had to take a totally different approach. You need an order of magnitude faster response," points out Robert Goelz, sales manager for motion controls.

Unlike a standard programmable controller, the 2184 is an event-driven machine. It does not scan input and output lines. Rather, "it is dedicated to servo control," states Stephen P. Mader, Modicon's national sales manager for motion-control and communications products.

The power of the 2184 rests in its ability to outline a complete motion scheme, or profile. The user defines the position and velocity a servo should have, and the 2184 calculates the line connecting to that position and the acceleration and deceleration needed for the motor to move it there. A single motion between two nearby points is called a chord, and a series of chords constitutes a profile. The unit can position motors to within ± 0.001 in.

The 2184 is programmed in the English language on a standard $5,995 programmer that Modicon already offers for its line of programmable controllers, the P-190. Thus, any user already equipped with a P-190 can use it for the 2184. Set up to program a profile on the 2184, the interactive P-190 asks the operator first whether metric or English units are to be used; it then asks him to specify the maximum velocity, and so on.

Modicon says it will begin shipping the 2184 programmable servo controller in October. It will carry a list price of about $4,500.

For factories that have analog and digital controls, Modicon states that this is a missing link in the evolution of the fully automated factory. "In the factory you have analog and digital stuff and then you have motor controls," Mader says. "Once you can control motors, and you've got control of the analog and digital quantities, then you've got the automated factory."

Gould Inc., Modicon Division, P. O. Box 83-S. V. S., Andover, Mass. 01810. Phone (617) 475-4700 [391].

Terminal captures data for NCR Data Pathing system

The 2.6-lb portable 2860 PDCU data-capture unit is for use with NCR's Data Pathing shop-floor data-collection systems. The programmable terminal is designed to extend industrial source-data management into environments that could not previously be reached with stationary data-collection terminals, and it eliminates much handwritten data collection.

To operate the 2860, a user loads one to four application programs into its memory by connecting it to an NCR 2820 multifunction terminal or 2830 industrial display station communication cable. During use, terminal programming guides the

New products

operator through each data-entry step, with prompting messages appearing on a 16-character light-emitting-diode display and predefined LED indicators. Operators enter data through a 48-key sealed keyboard or an optional bar-code reader. Entered data appears on the display for verification. Up to 8,000 characters of alphanumeric or 16,000 characters of numeric information can be stored in its memory. Data is then unloaded by connecting the 2860 to an NCR multifunction terminal that is on line to the central factory data collection system. Available during the first quarter of 1982, the unit will sell for $2,500.

NCR Corp., Dayton, Ohio 45479. Phone (513) 445-2075 [393]

Programmable mini controller can handle 46 I/O channels

The SYSMAC-M0 three-model series of small programmable controllers offers its own power supply unit, as well as input/output expandable

to 46 channels. The $495 W model has a keyboard, 256 words of random-access memory, four banks of 256 words in erasable programmable read-only memory, an up-down program loader, program display, and 32 I/O channels. The down-scaled A model at $450 has the features of the W except the erasable PROM and up-down program loader. The original-equipment manufacturer version, model S for $350, contains only the E-PROM and the I/O channels.

The compact 6-by-3-by-4-in. controllers have industrial machine and small system control applications. Also available is the SYSMAC-P0 sequence controller for independent

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Now Hewlett-Packard offers you a choice in full performance alphanumeric calculators. The new HP-41CV has five times more built-in memory than the HP-41C. Both calculators are powerful yet easy to use. You can communicate with words as well as numbers. For example, label and call up programs by name and receive meaningful prompts while executing programs. Continuous Memory retains programs and data even while the machines are off. Need lots of memory? Choose the HP-41CV. If your needs are more modest, select the HP-41C. The HP-41C can grow with you by adding memory modules.

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By themselves the HP-41C and HP-41CV may be all the calculator you'll ever need. But if you need more capability, you can expand your calculator into a complete computational system. Each calculator has four ports which allow you to plug in a Printer/Plotter, an "Extra Smart" Card Reader or an Optical Wand for reading bar codes. Application Pacs and Solution Books offering complete solutions are also available. And now, HP offers a new service: Custom Modules (ROM's) from your software for high volume, unique problem-solving needs. Costs are reasonable. Call us.

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Circle 203 on reader service card

use or as an add-on.
Omron Electronics Inc., 650 Woodfield Rd., Schaumburg, Ill. 60195. Phone (312) 843-7900 [394]

Encoder puts out 3 channels of square, amplified sine wave

Datametrics' K3 series kit encoder is a modular optical encoder designed to be integrally mounted on a servo motor. The kit consists of an optically encoded disk on a precision-bored hub mounted on a motor shaft, plus a light-emitting-diode light source and photocell detector assembly that mounts directly on the motor backend. Up to three channels of square wave or amplified sine wave output are available in a case 2.1 in. in diameter. Line counts of up to 1,200 pulses per revolution can be specified. Metal deposition on glass, photoemulsion on plastic, and etched metal versions are available.

The self-aligning encoders are immune to the effects of power supply variation and component aging because they use a single LED light source and a monolithic sensor array. Prices range from $99 for a square-wave single channel unit with no markers to $145 for a sine-wave dual-channel model with markers. Discount pricing for original-equipment manufacturers is available, and delivery takes six to eight weeks.
Datametrics Inc., 340 Fordham Rd., Wilmington, Mass. 01887. Phone (617) 658-5410 [398]

Analog bar-graph indicator responds in under 1 ms

The solid-state analog bar-graph indicators in the APM 20 series employ a 3-in. 20-element bar graph and are available in voltmeter and ammeter ranges of 0 to 50 mV, 0 to 1 V, 0 to 10 V, 0 to 1 mA, and 4 to 20 mA, all dc. Options include offset span, differential input, a response time of less than 1 ms, and either single or dual set-point controls. The standard bar graph is red, but green

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The New Gould 2200S. Our new 2200S oscillographic recorder with incremental chart drive performs so quietly you'll barely know it's running. Plus, you get unmatched versatility from the following innovative features:

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- **Added recording dimension**—Since chart speed is controllable by an external pulse input, the 2200S can display a signal as a function of any variable that can be transformed into a pulse train. Thus, the 2200S can function as a Y-Xt recorder.
- **Use it anywhere in the world**—The Gould 2200S operates on line voltages of 100, 115, 200, or 230 Vac from 50 Hz to 400 Hz.
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- **High accuracy**—Crystal-controlled clock provides a chart speed accurate to ± 0.25%.
- **One or two channels**—One 100mm or two 50mm channel models are available with exceptional frequency response up to 125 Hz. 99.65% linearity full scale, square wave recording with less than 1% overshoot and rectilinear trace representation. Exclusive pressurized ink or fine-line thermal writing is available.
- **Application flexibility**—The 2200S accepts the Gould 4600 Series of plug-in amplifiers for a broad range of industrial, scientific and biophysical measurement applications.

For more information, contact Gould Inc., Instruments Division, 3631 Perkins Ave., Cleveland, Ohio 44114.

In Europe, contact Gould Instruments S.A.F., 57 rue St. Sauveur, 91160 Ballainvilliers, France.

For brochure call toll-free: 800-331-1000 (in Oklahoma, call collect: 918-664-8300).

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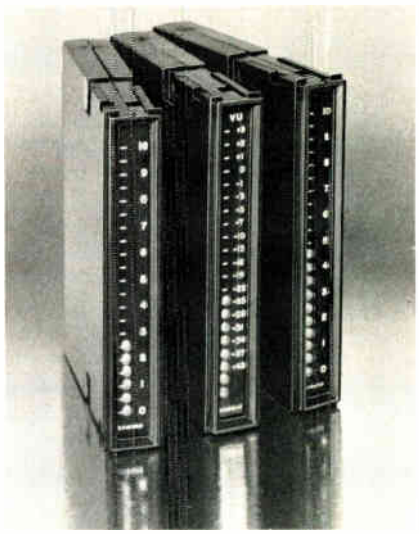

or yellow are available to meet special requirements. The meters meet ANSI 39.1 shock, temperature, and humidity requirements.

In quantites of 1 to 9, the meters cost $60, $50 in quantites over 50. Delivery is from stock.

Bowmar/ALI Inc., 531 Main St., Acton, Mass. 01720. Phone (617) 263-8365 [396]

18-mm photoelectric sensor sees as far as 78 in.

The type E58 photoelectric sensors detect virtually any material and measure only 18 mm in diameter. A one-piece three-wire design, the tubular units provide diffuse- or retroreflective sensing and are offered in ac, dc (pnp), and dc (npn) configurations. Equipped with pulsed light-emitting diodes, they operate in the infrared spectrum and are unaffected by ambient light.

The units have sensing distances of 80 mm (3.15 in.) for the diffuse-reflective models and 2 m (78.7 in.) for the retroreflective models. The ac devices are rated at 120 V, the dc units at 10 to 30 V. In addition they have LED state indication, US and DIN mounting dimensions, and short-circuit protection on dc devices. In lots of 100, the ac models are about $120 and the dc versions $100. Delivery is from stock.

Eaton Corp., Cutler-Hammer Products, 4201 N. 27th St., Milwaukee, Wis. 53216. [397]

High-clarity. One way itron fluorescents will brighten your displays' future.

The brilliance and conciseness of our new high density 128 x 128 and 256 x 64 dot matrix display panels—made possible by our advanced double-matrix structure—exemplify the wealth of benefits afforded by "itron" fluorescent units. Let's enumerate some of the other reasons they'll enhance your designs' future.

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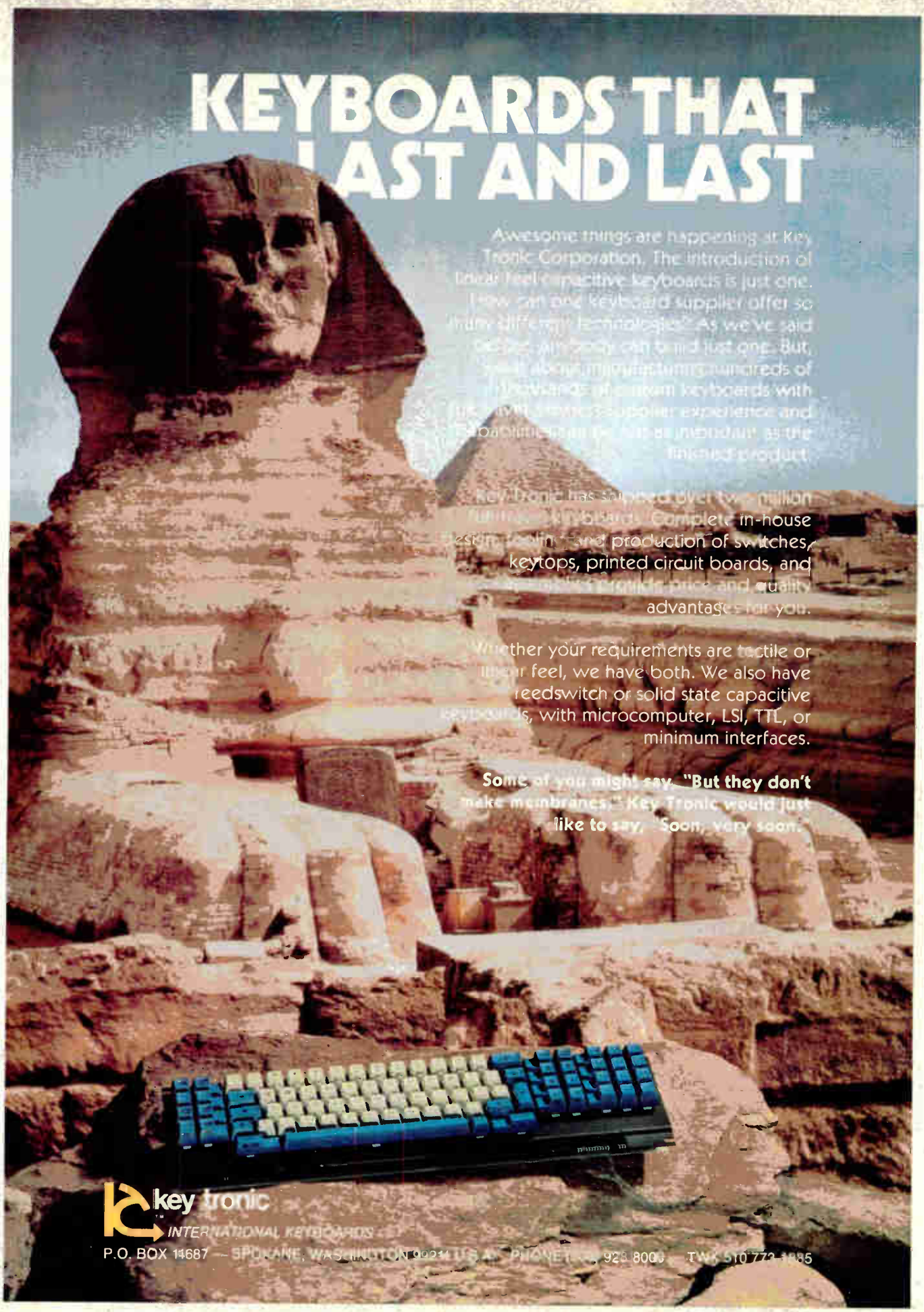

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Circle 210 on reader service card

Components

Op amp aims at communications

741-like monolithic amplifier is faster with 10-kHz maximum undistorted output frequency

The versatility that has made the 741-type operational amplifier so popular has its limits—the device's maximum undistorted output frequency of 5 kHz does not quite stretch far enough for a large number of telecommunications applications. As a result, telecommunications systems designers usually have specified premium 741 types—those exceptional chips in a batch that could give full power up to the 7-kHz frequencies needed for such applications. Now, however, this need is being addressed by a standard product, the pin-compatible OP-19 from Precision Monolithics Inc. The OP-19 has a slew rate of 1.0 V/μs, which allows it to stretch its maximum undistorted output frequency to 10 kHz.

The OP-19 is fabricated with the same triple-nitride passivation scheme as previous PMI 741-type op amps, but this one offers a number of improvements in specifications. One such improvement is the slew rate, which compares to a 0.8-V/μs rate on the firm's 741 op amps. The input offset voltage on the best version, the OP-19A, is typically 0.3 mV with a maximum of 0.5 mV. This compares with a typical 0.5-mV specification on PMI's 741. This capability is made more attractive by the fact that the A version holds these specifications over a full military range of $-55°$ to $+125°$C.

"We use some input bias cancelation schemes to allow the h_{fe} gains to hold up in the nanoampere and picoampere regions," says product manager Tom Schwartz. "What we've produced is a 741 with better dc characteristics and higher speed."

Also among the improved specifications is the OP-19's common-mode rejection ratio. The A version is specified at 100 dB typical and 85 dB minimum over a ± 10-V range with source resistance at less than 20 kΩ. This compares with a 70-dB minimum specification for the 741. Input offset current for the OP-19 is 0.5 nA, while its input bias current is 18 nA. Its average input offset voltage drift is a very low 2.0 μV/°C at a substrate resistance of 500 Ω.

In some applications, the OP-19 can also be compared with PMI's high-speed operational amplifier, the OP-02. Its slew rate beats the 0.5 V/μs rate of the OP-02, and its large-signal bandwidth of 20 kHz (typical) compares with 8 kHz (typical) for the OP-02.

Certified. The OP-19 is screened into three quality versions, A, B, and C, over the full military temperature range, and three versions, E, F, and G, over the commercial range of 0° to 70°C. It is packaged in either a Z version, which is an eight-pin miniature dual in-line package as well as a J version in a TO-99 package. Still other versions have undergone the full military 883B processing certification. The prices range in quantities of 100 from $2.75 each for the OP-19GZ to $14.40 each for the OP-19AZ/883.

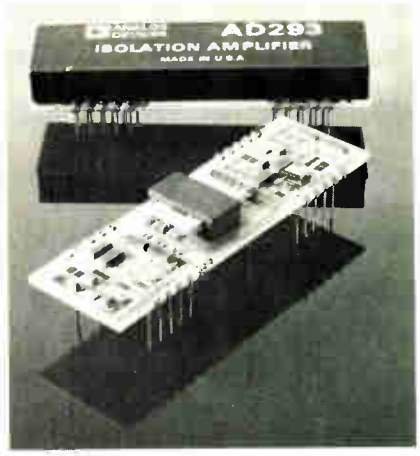
Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050. Phone (408) 727-9222 [341]

Isolation amplifiers use hybrid transformers

Analog Devices' new hybrid transformer technology (see p. 113) is being put to use in the AD293/4 isolation amplifiers—four units aimed at industrial, medical, and military applications. The 0.8-by-0.4-in. transformer employed is only 0.21 in. high, including a small E core. The AD293A and -B amplifiers offer $\pm 0.1\%$ and $\pm 0.05\%$ maximum nonlinearity, respectively; the AD293S/883B, as the name implies, is manufactured in accordance with MIL-STD-883B.

The fourth version, designated

New products



AD294, has the high common-mode voltage rating required for medical applications. It is capable of withstanding ±8-kV pulses 10 ms long every 10 seconds, as needed by equipment used in the presence of defibrillators. Medical use also calls for low leakage; a low 2-μA root mean square leakage specification is shared by all four versions.

The 293/4 is designed with monolithic amplifiers at input and output. Both amps are adjustable in gain, to a maximum gain of 100 at the input and 10 at the output. Gain variation with temperature for the entire unit is ±50 ppm/°C, maximum.

Maximum safe input voltage is 120 V rms continuous or 240 V rms for 1 minute. The common-mode voltage rating of the 293 is ±2,500 V continuous; the 293 will also handle 2,500 V of 60-Hz ac for 1 minute. The common-mode rejection ratio ranges from 100 to 115 dB, minimum, depending upon whether the source impedance is unbalanced or balanced, respectively. Differential input impedance is 10^8 Ω shunted by 150 pF; common-mode input impedance is 5×10^{10} Ω shunted by 50 pF.

Input noise is weighted toward low frequencies, with a rating of 10 μV peak to peak between 0.05 and 100 Hz, compared with half that, 5 μV, between 10 and 1,000 Hz. The 3-dB bandwidth is 2.5 kHz; full-power-output frequency depends on the overall gain selected and ranges from 250 Hz to 2.5 kHz; rated full-power output is ±10 V minimum into a 5-Ω load; output impedance is less than 1 Ω and the unit slews at

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New products

9.1 v/ms. The parts require ±15 v ±5% for operation at rated specifications. Prices in quantities of 1 to 24 are $69 for the AD293A and $79 for the 293B and 294; delivery for these is 4 to 6 weeks. Six-week deliveries of the AD293S/883B are due to start in November; its price is not yet set.

Analog Devices Inc., Route One Industrial Park, Norwood, Mass. 02062. Phone (617) 329-4700 [342]

GaAs amp operates over bandwidths of 1 GHz

The CGY 21 monolithic GaAs wideband amplifier has frequency ranges of 40 MHz to 1 GHz. It offers a noise figure of 4.5 dB, and its output voltage is 320 mV into 50 Ω or 400 mV into 75 Ω with a gain of 20 dB minimum. The basic GaAs material for the CGY 21 is manufactured by Siemens in Munich, where 2-in. wafers are already being processed. The active layer is achieved by direct ion implantation, which saves on time and cost and produces layers of high uniformity.

The amplifier is designed to replace hybrid and discrete amplifiers in wideband communication applications, such as TV satellite downlink receivers, cable-television line amplifiers, instrument preamplifiers, and broadband tactical receivers. In small quantities, the TO-5 or SIL-9 packaged amplifier costs $150. Full production is expected in spring of 1982, and in 1,000-piece lots, it will be about $25.

Microwave Semiconductor Corp., 100 School House Rd., Somerset, N. J. 08873. Phone (201) 469-3311 [343]

Molded rubber key pad snaps when contact is made

The KEA4A901 keyboard is a single piece of molded silicone rubber that functions as both spring and contact for all the keys. Contact is made through carbonized portions of the rubber that are pressed against

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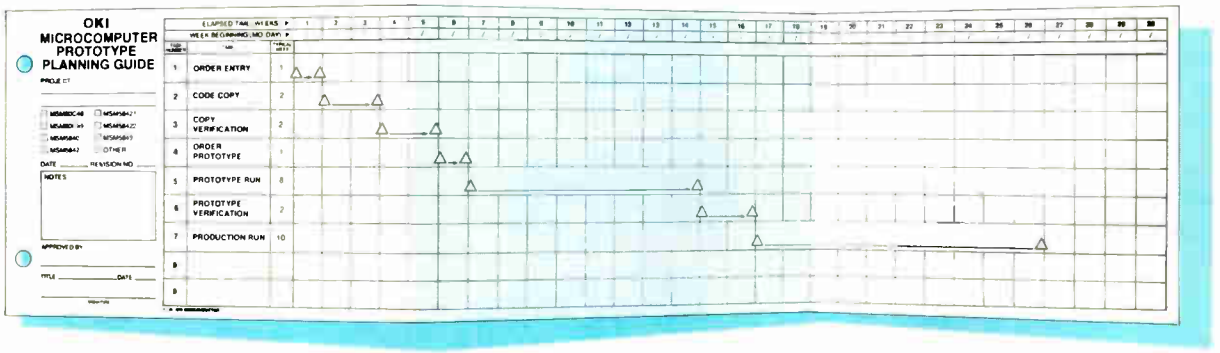

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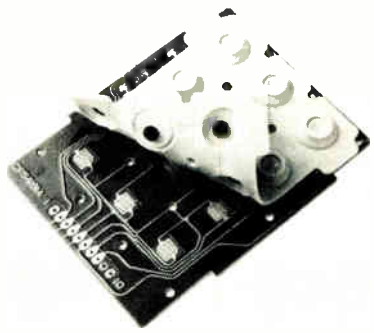

intertwined leads on a printed-circuit board. A tactilely distinct though inaudible snap made when the key is pressed indicates to the user that contact has been made. The conductive element in the contacts is carbon, not precious metal, immunizing it against the price changes of gold and silver. The molded rubber covers the printed-circuit board tightly enough to exclude dust from the contact area, and the carbon contacts are not affected by oxygen and sulphur. In addition, the keys are double-shot–molded, which means the graphics are injected into, rather than painted on, the plastic and are as deep as the keys. In 10,000-unit quantity orders the key pad sells for $2.90; sample price is $5.30. Delivery is 30 to 90 days after receipt of order.

Alps Electric Inc., 100 North Centre Ave., Rockville Centre, N. Y. 11570. Phone (516) 766-3636 [344]

Magnet withstands 250°C without flux degradation

The Raeco-23 samarium-cobalt magnet has a 23-megagauss-oersted energy product and an intrinsic coercive force of 14 kOe. In addition to the Raeco-23, Raytheon has three other types with energy products of 10, 16, and 20 MG-Oe and intrinsic coercive forces of 22, 18, and 16 kOe, respectively. When stabilized, all magnets can operate at up to 250°C for extended periods of time with little or no degradation in the flux. They are also small and stable over a wide temperature range.

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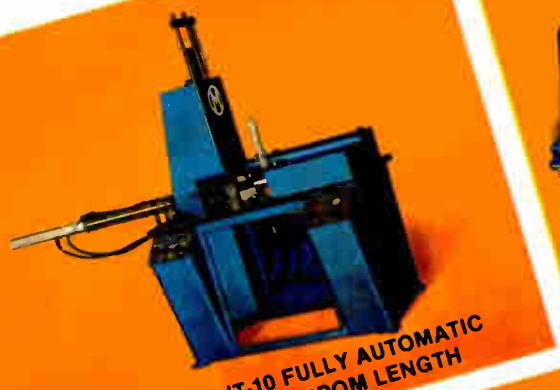

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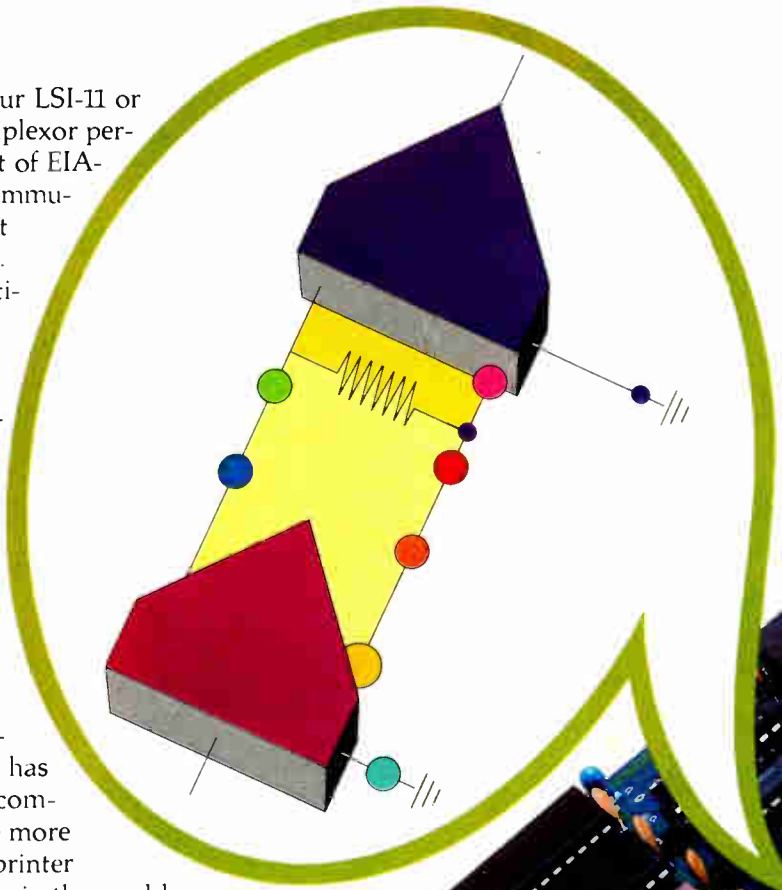

Circle155 for featured product data.

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Raytheon Co., 190 Willow St., Waltham, Mass. 02254. Phone (617) 899-8400 [345]

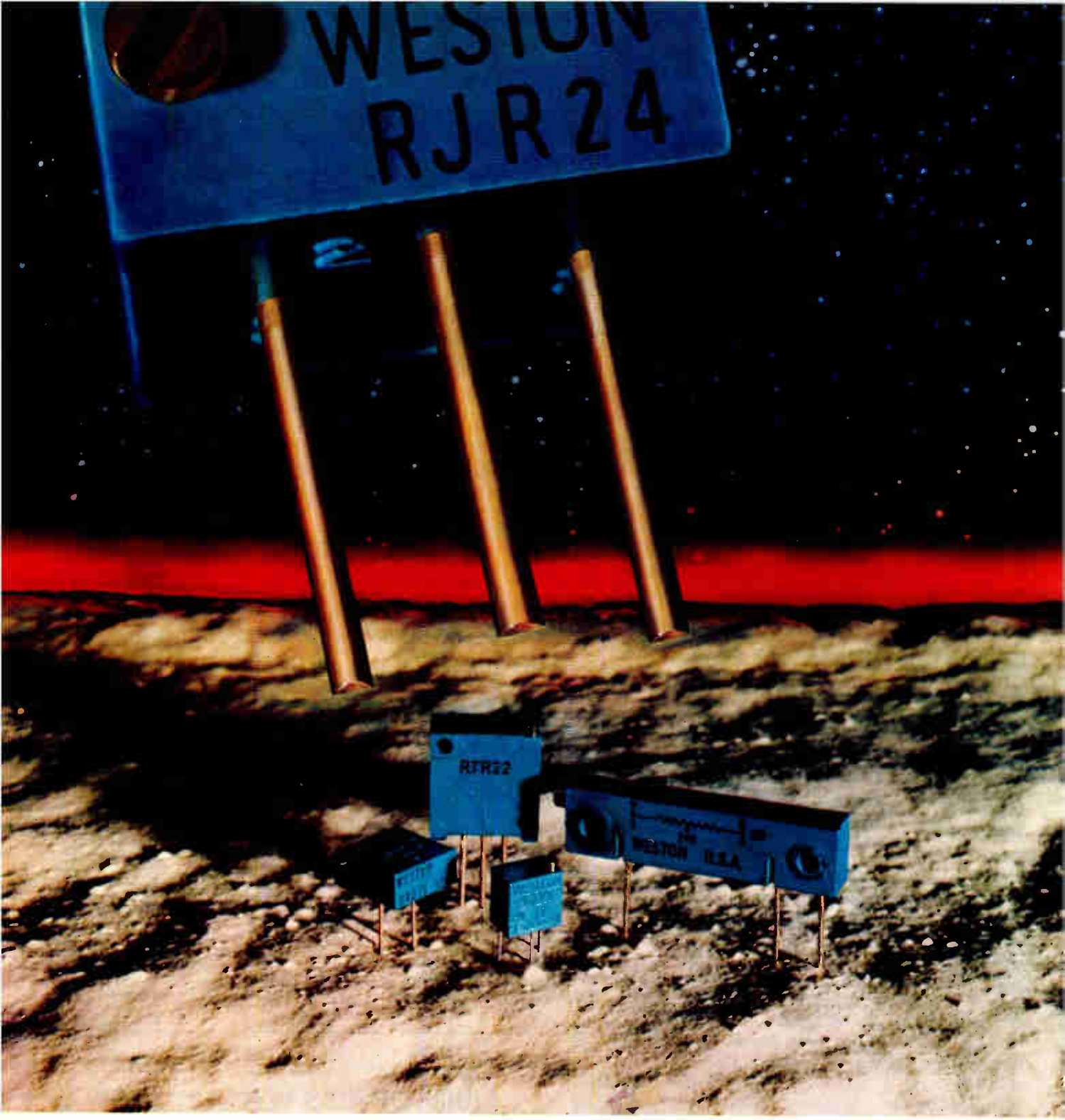
60-Hz relay features time delays of 50 ms to 24 h

Syracuse Electronics' digital circuitry time-delay relay is available with standard input voltages in six ac values of 12 to 230 V and six dc values

of 12 to 240 V. It operates at a frequency of 50 or 60 Hz maximum, consumes 3 W, and is available in time delay ranges of 50 ms to 24 h. The solid-state relay output is single-pole, single-throw, and normally open, and its contact rating for ac and dc values is 1 A at 25° and 40°C. It has a useful life of over 10^8 operations, with a typical repeat accuracy of ±0.5%.

Options include: redundant diodes to protect the output circuit from half-waving; low on-stage voltage for a lower on-stage output voltage than is usual for ac and dc models; and polarization in dc units to provide a lower on-stage voltage than is usually standard to drive dc loads that are unstable with low input voltage tolerance. Prices vary with quantity, and delivery takes two weeks.

Syracuse Electronics Corp., P. O. Box 566, Syracuse, N. Y. 13201. [348]



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Weston has a proven track record as an acknowledged leader in the manufacture of military approved devices to military specifications both Mil-R-39015 and Mil-R-39035. In fact, most of our established reliability trimmers are available from either factory or distributor stock. Call or write today for complete specifications, pricing and evaluation samples for any of Weston's complete line of established reliability or standard military QPL trimmers.

Circle 220 on reader service card

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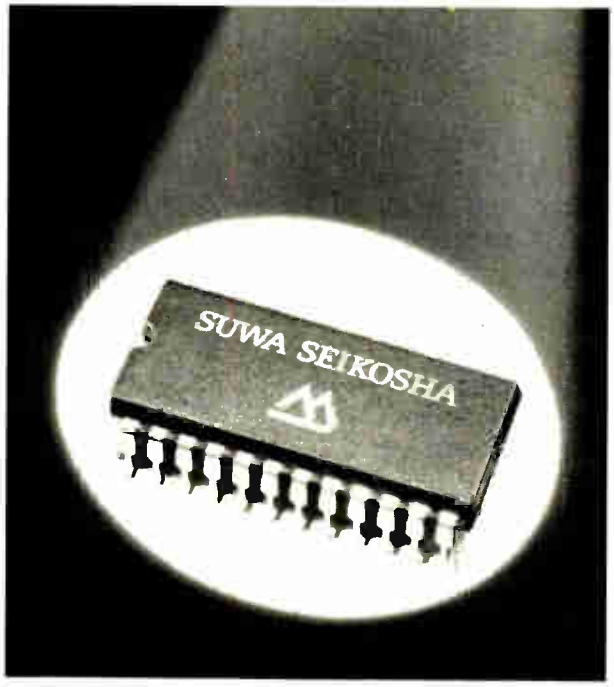

Suwa Seikosha, a major manufacturer of the famous SEIKO watches, was the originator of the quartz watch. As the pioneer of quartz watch technology, the company has consistently developed and manufactured its own miniature electronic parts and ICs. Today this accumulated "Mechatronics" technology is being applied to the development of a variety of new products in addition to watches.

A new Suwa Seikosha plant at Fujimi was set up in April 1980 to concentrate on the manufacture of CMOS LSI and other semiconductor parts. These units include: "Melody ICs," microcomputers, memories, speech synthesizers, and others. Suwa Seikosha, as a leading CMOS LSI maker, is aggressively exploring many future possibilities that will employ the company's most advanced technology.

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  - SEK7 Series
- **TIME STANDARD IC** (Standard Pulse Generator)
  - 8640
  - 8650
  - 8651
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  - SRM6514 (1K × 4-bit Static RAM)
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- **MICROCOMPUTER**
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Bare and loaded board testing takes a quantum leap forward!

with the introduction of Trace's new Series TA-9 Test Analyzer System.

From this moment on, you will have an entirely new concept of high speed board testing. You are about to discover an analytical system so advanced that its capabilities will dwarf and obsolete any you have used or known.

☐ The Trace Series TA-9.

Conceived and developed by the same people who revolutionized board testing procedures with their TA-4 and TA-5 Systems, the Series TA-9 virtually eliminates the division between tester and computer.

Through a dramatic, new design principle, the tester, itself, has been transformed into a true computer, containing both program and data memory. This significant change opens the door to a vastly broadened range in the selection and control of test algorithms. A range never possible before. And, for the first time, both bare and loaded boards may be tested at high speeds, with a system that pinpoints even the minutest areas of error.

The network program may be put into the data memory either from a known good board, uploaded from a floppy disk, or transferred in from a data processing computer. A new system of Crosspoint™ switching, originated by Trace, allows infinite variation of the matrix configuration. Instructions, based on high level, macro-instruction machine language are carried out in 2 clock cycles. The Series TA-9 requires fewer instructions to function at speed advantages of 100 to 1 and more over microprocessor controlled units.

The Series TA-9 is always at the command of the operator. Programs may be created, edited and revised quickly and easily and existing programs may be saved or incorporated into the new mode.

☐ A new era of testing evolution.

The Series TA-9 is designed to stand alone. But the use of a data processing computer, in conjunction with it, can increase its versatility even more. It will never become obsolete. Because it has been designed to become the basic system for a series of modular units, now under Trace development and testing, that will continue Trace's leadership in technological advances in the testing industry. The Series TA-9 will grow in its capabilities to meet your expanding needs.

☐ Before you invest – investigate Trace

If you are considering a new testing system, it will pay you to look into Trace and the new Series TA-9. Because Trace is the acknowledged leader and innovator in the field.

After all, you'll have to work with the system you choose, for a long, long time!

Write, wire or phone for the complete TA-9 story!

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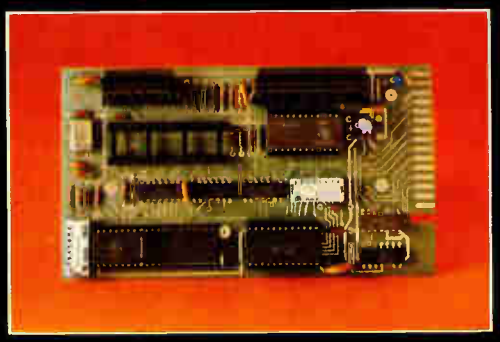
Oak puts E^3 up against the world's fastest typists.

In a keyboard market clogged with claims and confusion about "N-key-rollover," look to Oak's FTM® keyboard for the practical answer. It provides E^3-Entry Error Elimination. And that means precisely what it says. We challenge the fastest typists in the world to make it error. They can't.

Yet E^3 makes its real contribution to Oak's Full Travel Membrane (FTM) keyboard—and to you—in the cost column. You get the Entry Error Elimination and 100-million-cycle-plus performance you've got to have in a keyboard at prices far below those of keyboards with comparable performance. That's practical. Entry Error Elimination is a remarkably sensible microprocessor based N-key-rollover and phantom key lockout system developed by Oak engineers. Without the cost and complexity of Hall Effect and capacitive technologies.



And that's not all. Beneath the FTM keyboard is Oak's proven, industry-leading membrane switch technology. So you get all the good things of membrane switching—reliability, durability, RFI and EMI resistance, design flexibility, and—of course—low cost. All without sacrificing the qualities you demand in a keyboard, right down to human engineered industry standard feel and touch.

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Circle #223 for further information

Circle #117 to have a sales engr call

Communications

Set tests line with pulses or tones

Telephone-line tester operates using line power and works despite reversed connections

The MT-911G test set for telephone lines using either rotary-pulse or Touch-Tone dialing now runs from phone-line power, satisfying phone company specifications for doing so. Previous test sets from Metro Tel Corp.'s product line required a battery to power the reverse-polarity indicator. Battery power is also used in the firm's sets to operate an optional last-number-recall feature; the 6-v battery is still required for this option. Space is left inside the portable instrument for the battery.

The MT-911G operates even if the tip and ring circuits are connected in reverse during a phone-line check, merely indicating the condition with a light-emitting diode. Previous sets did not have this time-saving bipolar-operation feature. Another update involves the asterisk button, which on earlier members of the line served only as an on-off switch. The set now emits a tone when this button is pushed, serving a command function.

It also offers transmitter muting to permit its use in noisy locations. By pressing the mute button, the operator can momentarily cut off the set's transmitter so that loud ambient noises during communication with the test board are not received back in his ear.

The capability to test a 2,000-Ω loop is standard on the MT-911G. Interface impedance in the talk mode is 1,200 ± 150 Ω from 450 to 3,200 Hz; in the monitor mode, impedance is a minimum of 600 Ω from 500 Hz to 100 kHz. Operating in the rotary mode, dialing rate is 10 pulses/s ± 2%, break percentage is 61 ± 1%, and interdigit time is 800 ± 10 ms. Frequency accuracy in the tone mode is within ± 1.5%.

Many telephone systems are in the process of moving from rotary to tone dialing, and for the time being use both types. The MT-911G's multimode capability suits the unit to use during the transition. It offers a variety of interchangeable cords, all of which plug into its standard modular connector.

The test set measures 8.75 by 2.5 by 2.5 in. and weighs only 10 oz. Without cords, its price is $147.30; delivery is from distributor stock.

Metro Tel Corp., 15 Burke Lane, Syosset, N. Y. 11791. Phone (516) 364-3377 [401]

Transmitter sends analog signals as low as 10-mV

The 3714T fiber-optic transmitter accepts analog signals, amplifies them (the user selects adjustable gains of 1 to 1,000 v/v), converts

them into a frequency-formatted digital pulse train, and changes that into a light output. When used with fiber-optic cable and either the 3712R or 3713R receivers, the 3714T forms a data link that will transmit analog signals as low as 10 mV full scale over distances of up to 1.7 km. The link output is a TTL digital pulse train that may be interfaced with a counter for analog-to-digital conversion or converted back into analog form with a frequency-to-voltage converter.

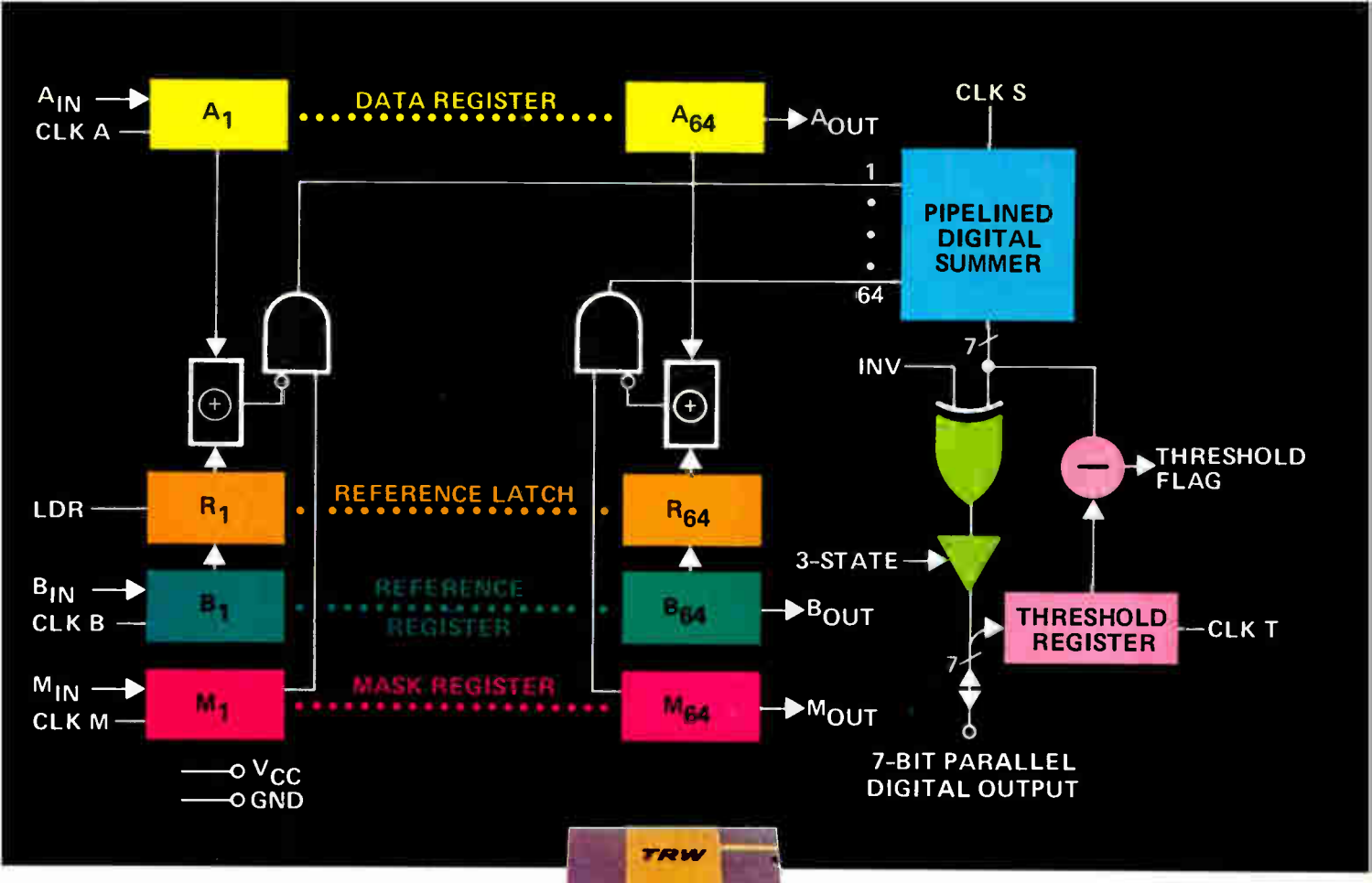
It has an input impedance of 10^{10} Ω, a gain drift of 175 ppm/°C maximum, and a linearity of ± 0.01% maximum full scale (for voltage-to-frequency converter output of 0.01 Hz to 10 kHz). Its input voltages are 0 to + 10 or − 10 v unipolar and − 5 to + 5 v bipolar, with a maximum output frequency of 50 kHz. Delivery is from stock on the 3714T, which sells for $93.75 in lots of 100.

Burr-Brown, Box 11400, Tucson, Ariz. 85734. Phone (602) 746-1111 [403]

8103 smart controller has dual-ported RAM

The 8103 smart communications controller uses a dedicated 8085 microprocessor to meet serial RS-232-C and Bell 202 requirements. It is partitioned into three sections: the central processing unit, a serial communications interface, and a dual-ported random-access memory. All the communication channels are controlled by the 8085.

The CPU is equipped with 16-K bytes of RAM, read-only memory, and erasable programmable ROM



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- Only $85 in 100's

Prices quoted are U.S. prices.

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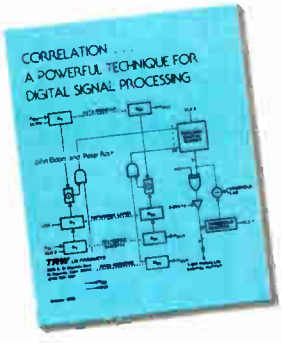

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TRW keeps you ahead in digital signal processing

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Circle 224 on reader service card

New products

points while optimizing the bandwidth of the telephone circuits.

Multiplex.25 can be used as a terminal concentrator for mainframes and minicomputers that employ the X.25 synchronous interface. It can also exchange data with hosts of dissimilar speeds, and concentrate terminal traffic on single trunks to a data network, eliminating dial-out and dial-in modems and the monthly message-unit telephone company charges.

The four- or eight-port multiplexer is compatible with the GTE Telenet and the Tymnet networks in the U. S., Datapac in Canada, PSS and IPSS in the UK, Transpac and NTI in France, DN-1 in the Netherlands, CTNE and RETD in Spain, as well as the Euronet network and the offerings of the international record carriers such as Western Union International, ITT Worldcomm, and RCA Globecom. The four-port version sells for $995, the eight-port version for $1,700. Delivery takes 30 days.

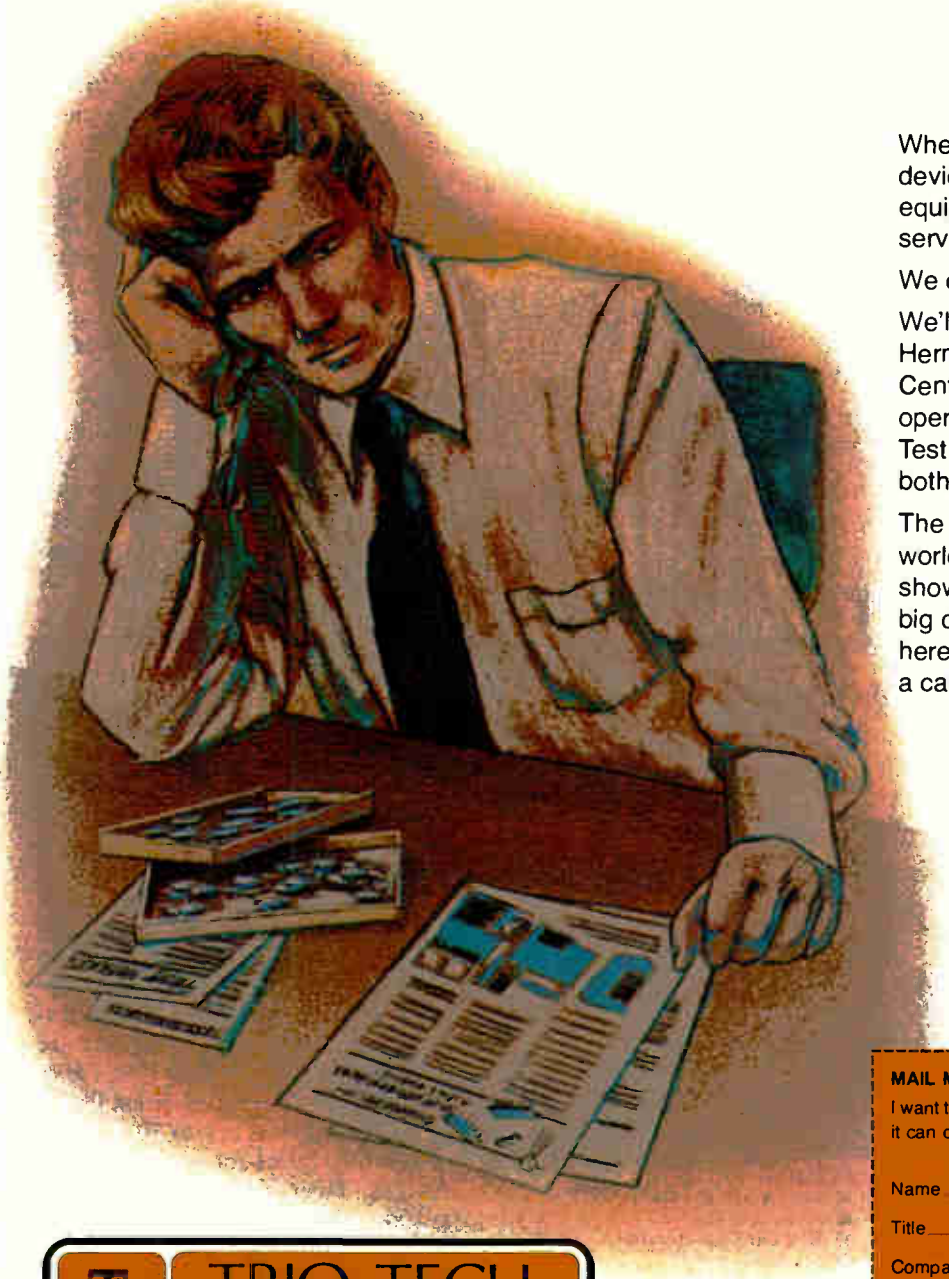
Dynatech Packet Technology Inc., 7664-A Fullerton Rd., Springfield, Va. 22153. Phone (703) 569-8531 [405]

Receiver gets quality TV signals from satellites

The 7500 receiver of television video and sound from satellite transmissions exceeds the requirements of RS-250B/NTC-7. It is modular in construction: all its circuits plug in from the top except for the down converter, which is removable from the front panel. Using the keyboard and display, the user can enter a frequency and transponder number directly and step either of them up or down from its present value or else select one of six memory channels that are preprogrammed by the user.

Frequency control of the model 7500 is gained with a phase-locked frequency synthesizer. Two versions of the synthesizer are available—one with 20-MHz channel spacing for conventional full transponder video and the other with 250-kHz channel spacing for half-transponder and other special applications. The unit

To buy or not to buy, That is the question.



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Circle 229 on reader service card

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costs $4,500 and is available 30 days after receipt of order.
Scientific Atlanta Inc., 1 Technology Parkway, Box 105600, Atlanta, Ga. 30348. Phone (404) 441-4000 [406]

Infrared system transmits voice, computer data

Light Comm I infrared transmission system transmits computer data or voice on an invisible beam. By placing computer data directly onto an incoherent infrared light beam, it makes short-range data communications less expensive than if it used microwaves, fiber optics, or metallic wire, all of which entail trenching charges. A reliable and secure transmission system with no Federal Communications Commission restrictions, Light Comm I runs at standard data rates of 2,400, 4,800, and 9,600 b/s and 19.2, 38.4, and 76.8 kb/s. The system includes two optical transceivers, associated cabling, and digital controller with RS-232-C interface. The system sells for $12,000, with delivery in 30 days.
Light Communications Corp., 25 Van Zant St., Norwalk, Conn. 06855. [407]

Couplers allow transmission of 1,500-nm wavelengths

Phalo's digital and analog three- and four-port optical directional couplers are for use as tabs or feeds in multiterminal networks, multiplexing, and other applications. The couplers permit full-duplex operation over a single fiber. The standard products are available using Corning SDF fiber and a variety of graded-index fibers. They also have a 1:1-to-20:1 range of splitting ratios for use in network designs. Their passivity permits operation at all standard transmission wavelengths from 600 to 1,500 nm. In quantity the couplers sell for less than $200 each, with delivery from stock in two to four weeks.
Phalo, Optical Systems Division, 9240 Deering Ave., Chatsworth, Calif. 91311. Phone (213) 998-3177 [408]

THE COMPANY THAT STARTED AHEAD IN THICK-FILM NETWORKS STAYS AHEAD






Ever since thick-film resistor networks were first made, Sprague Electric has led the way. By doing much of the pioneering. By being first to put a network of resistors in a standard dual in-line package. By making more thick-film circuits than any one else...year after year.

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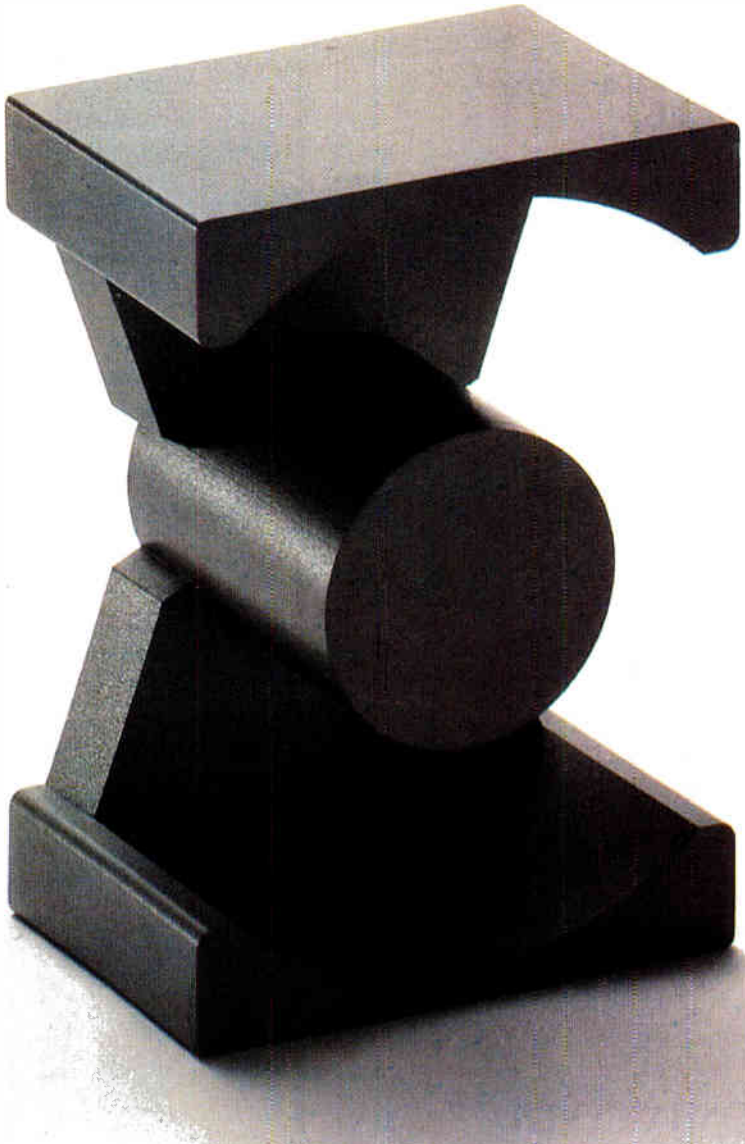

TDK

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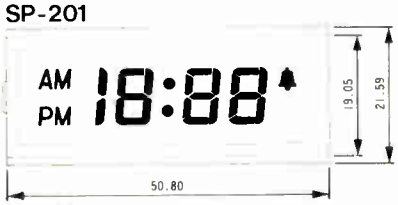

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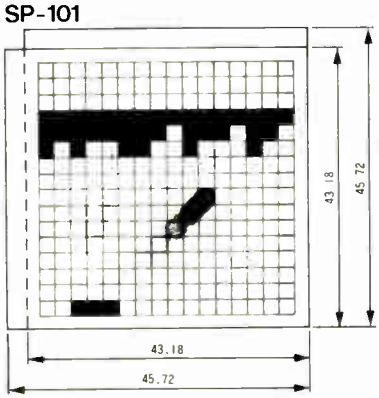

[Characteristics]

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Test up to 8,000 points.
Simple, reliable test fixturing, the Series 32 is ideally suited for use with the Series 50. Vacuum-actuated and flexible, the Series 50/32 Test System is easily justifiable for the majority of bare board applications.

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EECO RELIABILITY IN A SWITCH AS SMALL AS .396" x .376"

Reliability that's achieved by EECO's exclusive gold contact system, which assures low contact resistance, and a bottom seal on some models, to protect against flux migration. Compact switching that's available in one-or two-pole, 10- or 16-position models, each versatile enough to meet your design needs.

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MICRO-DIP MAKES IT SIMPLE

Coordinating with microprocessor technology, MICRO-DIPs are simple to design in, and simple to adjust in the field, even by non-technical users. To make adjustments even easier, EECO's BCD right-angle model allows mounting on the card edge to provide access without pulling the card.

MICRO-DIP can be mounted directly to P.C. boards or inserted into standard DIP sockets, and its small size and low profile make it ideal for high density packaging requirements. Available in screwdriver or extended shaft adjustable models, this neat little switch can be actuated in either direction.

To make designing maximum function in minimum area simple, choose EECO's MICRO-DIP switch. For detailed information, write EECO Incorporated, P.O. Box 659, 1601 E. Chestnut Ave., Santa Ana, CA 92701, or call 714/835-6000.

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Circle 236 on reader service card

Microcomputers & systems

C-MOS 8048 has extras

Microcomputer powers up as standard 8048; register controls optional features

The ranks of complementary-MOS versions of popular microprocessors and microcomputers using n-channel MOS are growing steadily. The newest circuit is National Semiconductor Corp.'s C-MOS version of the 8048. This 8-bit microprocessor, originated by Intel in n-MOS, uses National's 5-V-only double-level polysilicon C-MOS process—the same as in its NSC800 microprocessor that combines the Z80 instruction set with the 8080 multiplexed bus structure.

The chip is offered in two versions: the 80C48 is identical to the n-MOS version but is cast in C-MOS. The 6-MHz 80CX48, however, goes beyond its n-MOS counterpart by having a special idle mode that lets it stand by in a low-power state and retain data in its 64-byte internal random-access memory.

Option activation. The characteristics that differentiate it from the 80C48, besides the pin-activated low-power idle state, are each activated by a bit in the special feature-control register (FCR). Upon powering up, the device configures itself as a standard 8048. However, when one of the previously undefined bits in the FCR is toggled, the 80CX48's special attributes become available until it is reset.

The part is put to sleep when a pin—the power-supply pin on the original 8048—is brought low. When shut down, the 80CX48's supply current is lowered from 5 mA to 20 μA. This lowering compares with a reduction of 10 mA to 1 mA for a Nippon Electric Co. version of the chip [*Electronics*, July 14, p. 179]. The 80CX48 cannot, however, be put to sleep by a software instruction as NEC's version can.

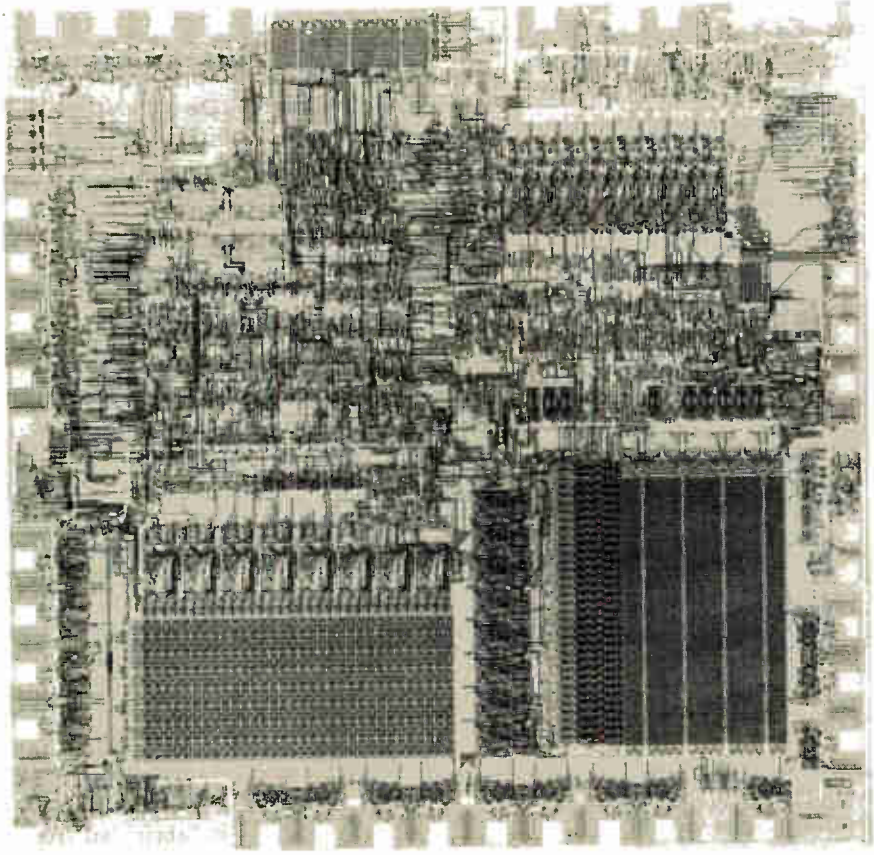
Other features in the device involve the timer-counter built into the 8048. The CX version adds a programmable (for eight different decimal-oriented values) prescaling of the clock signal that is supplied to the timer-counter, in contrast to the constant divide-by-32 prescaler of the 8048. Also, the output of the prescaler may be gated, under control of an FCR bit, with an external signal supplied to a special pin. In addition, a new register has been added that will automatically load the timer-counter when it overflows, permitting true *modulo-n* counting in hardware.

National's continue option allows the 80CX48 to ignore the logic level on the idle input. When set, another bit in the FCR keeps the levels of the input/output lines constant during the idle mode, rather than allowing them to enter the high-impedance mode.

The part is also designed to work with National's other P²C-MOS support chips like the NSC810 RAM, I/O, and timer chip, and the NSC830 read-only memory and I/O chip. Intel also is said to be working on a C-MOS version of the 8048 as one of the initial offerings in its drive to develop this low-power process.

The 80C48 will be available for volume deliveries in October at a price of $15. The 80CX48 will arrive in November for $16. Both prices are for 1,000-piece quantities.

National Semiconductor, 2900 Semiconductor Dr., Santa Clara, Calif. 05051 [371]



Multimodule board connects to IEEE-488 instruments

The iSBX 488 General-Purpose Interface Bus multimodule board provides a standard interface from any Intel iSBC Multibus board equipped with an iSBX connector to over 600 instruments and computer peripherals that use the IEEE-488 GPIB standard. The module may be configured as a talker, talker and listener, or bus controller. It employs Intel's very

large-scale integrated-circuit technology to incorporate the 8291A GPIB talker/listener, 8292 GPIB controller, and two 8293 GPIB transceiver devices on a 3.7-by-2.85-in. printed-circuit board.

With the board configured as a controller, users of single-board computers can program and control up to 15 instruments over a standard parallel bus. The multimodule board can be used on such Intel 8-bit processor boards as the iSBC 80/10B board (8080), 80/24 board (8085), and 88/40 measurement and control computer (8088); and on 16-bit processors such as the 86/05 board (8-MHz 8086).

The iSBX 488 module operates at programmable data rates of up to 50 kilobytes/s and implements complete sets of GPIB functions instead of only subsets. It supports direct-memory-access data transfers of up to 300 kilobytes. It requires 600 mA from a +5-V power supply.

Available immediately, the iSBX 488 multimodule board sells for $650 in single-unit quantities and $598 in quantities of 10. The iSBC 988 0.5-meter companion cable that supports the IEEE-488 standard is available for $75.

Intel Corp., 5200 N. E. Elam Young Parkway, Hillsboro, Ore. 97123. Phone (503) 640-7147 [373]

IC gives 68000 processors memory management

The MC68451 single-chip memory management unit allows MC68000 16-bit microprocessor users to segment 16 megabytes of memory 32 ways. Each of the unit's 32 segments can cover a range from a minimum of 256 bytes to the full 16-megabyte addressing space of the 68000. The device uses bit-replacement techniques, as opposed to adders, for translation of the microprocessor's logical addresses into physical addresses. Direct address translation keeps the chip size to a minimum and enhances the memory management unit's speed.

The MC68451 is fabricated from

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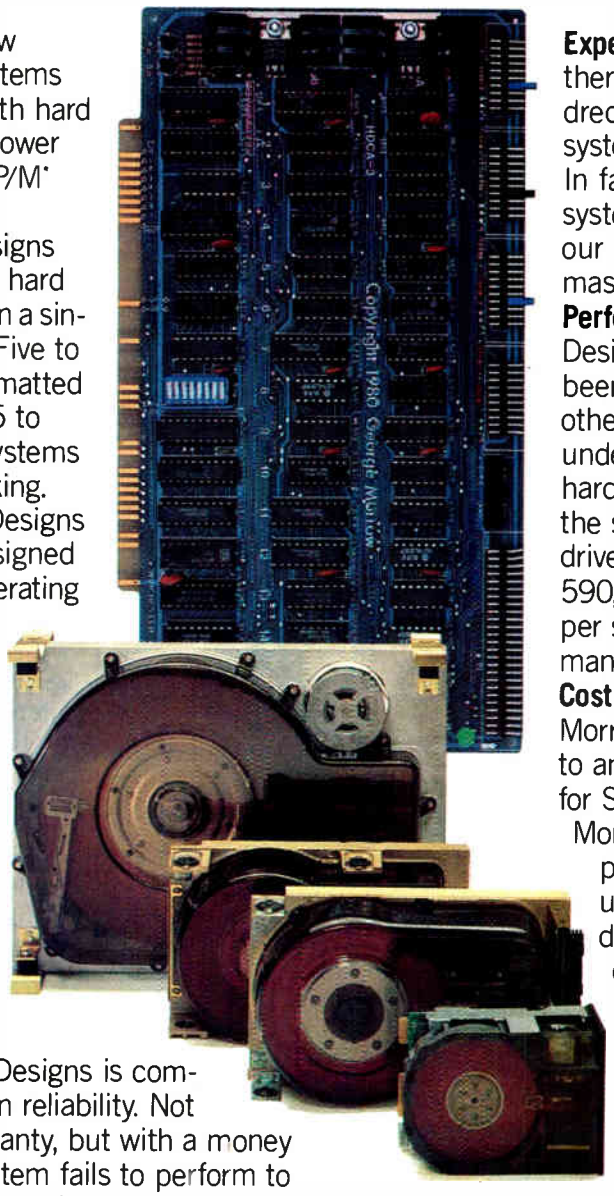

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***Cromemco is a trademark of Cromemco, Inc.
****Exidy is a trademark of Exidy Corporation.

New products

Motorola's H-MOS Level I technology and has 3.5-μm line widths. It has a speed of 125 ns. The unit goes for $215 in single quantities, $150 in lots of 100, and $120 in orders of 500. Production volumes will be available later in 1981.

Motorola Inc., 3501 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 928-6369 [374]

Multibus debugger gives users real-time displays of addresses

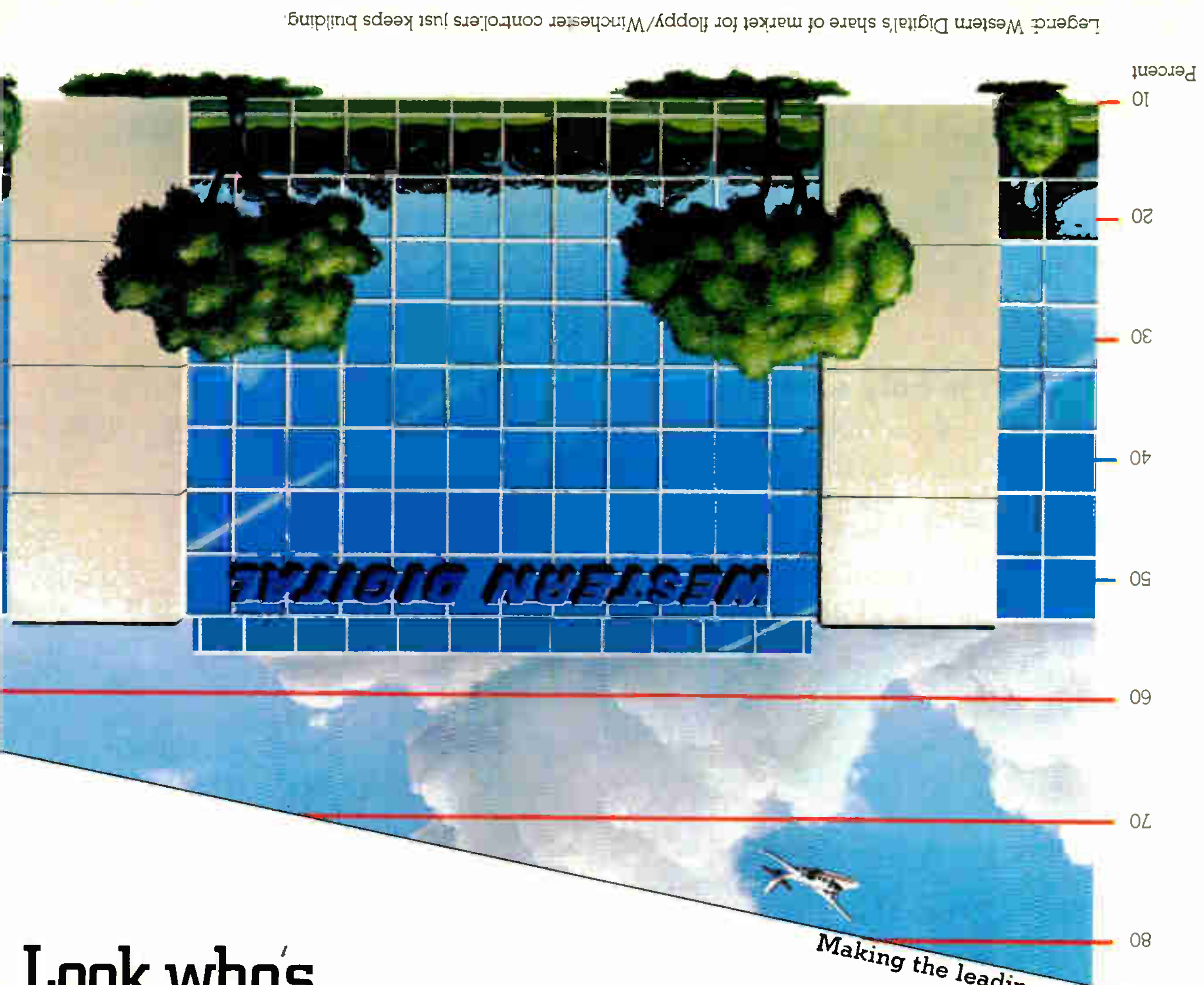
The 1506 Multibus display computer board is a debugging tool for Multibus users and provides both static and dynamic displays of program execution. Used to monitor addresses, data interrupts, and control signals, it automatically holds and displays the last bus cycle executed. Prior selection of memory read, write or input/output read or write results in an indication of the address, interrupt, or last data value for the last cycle executed by the bus selected.

The 1506 gives the Multibus user real-time memory and I/O mapping capability. Connecting the low- and high-address connectors to the X-Y inputs of a standard oscilloscope provides a real-time display of the upper and lower I/O addresses.

In addition, the 1506 includes leading- or trailing-edge selection, 16-bit data display, 16- or 20-bit address display, power-up indication for bus voltages, and a transfer-acknowledge switch for generating an artificial transfer-and-acknowledge signal.

The 1506 costs $495 each, with large-quantity discounts available. Delivery is from stock.

LeCroy Research Systems Corp., 700 So. Main St., Spring Valley, N. Y. 10977. Phone (914) 425-2000 [375]



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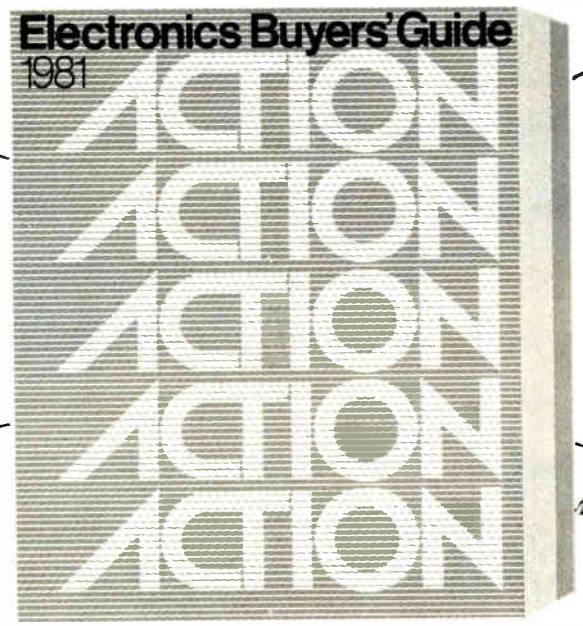

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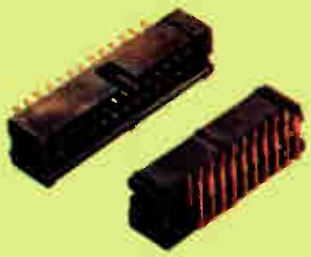

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IDE Series—Three mounting options available.

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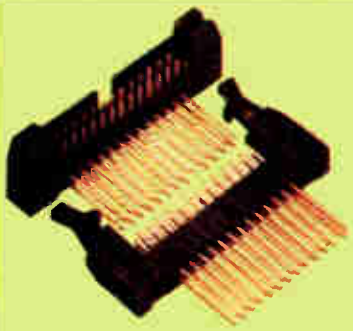

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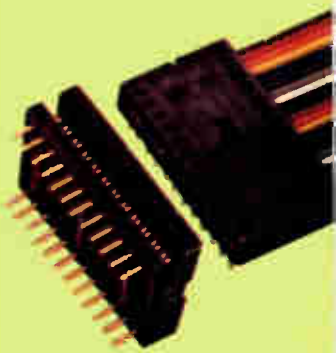

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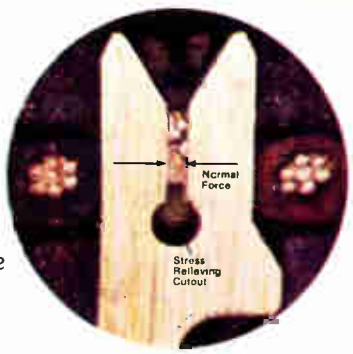

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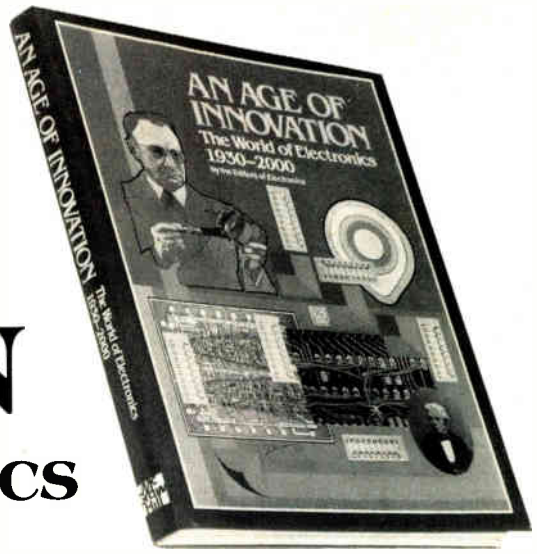

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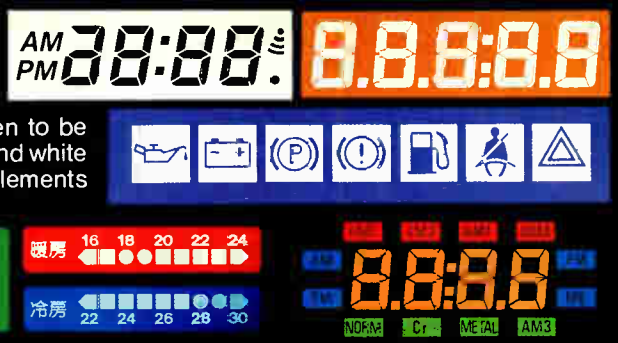

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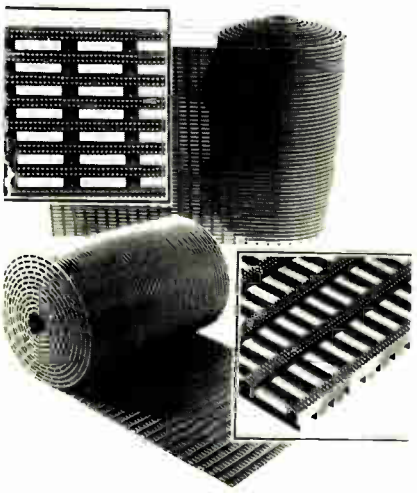
Xersin flux materials are based on definably pure chemicals rather than natural rosin. The residues of Xersin are less corrosive than rosin fluxes and in most cases need not be removed from a printed-circuit board after the soldering operation. Also, the fumes given off during soldering are reduced and contain none of the aldehydes found in rosin. Multicore has developed a range of products using the Xersin technology, among them wire-cored solders, foaming fluxes, a combination preservative and flux, protection coatings, solder creams, solder wick, and a material that combines the functions of an etch resist, flux, and preservative. Xersin is priced comparably with standard rosin material, with delivery from stock.

Multicore Solders, Cantiague Rock Road, Westbury, N. Y. 11590. Phone (516) 334-7997 [476]

The Vynastat antistatic and antifatigue mat has a grid construction formed by heat-welding extruded strips of conductive polyvinyl chloride and has an embossed tread on top and bottom to prevent slipping. The resistivity from the mat to the end of the grounding tape is $1.9 \times 10^6\ \Omega$. The mat is $\frac{3}{8}$ in. thick and 2 or 3 ft wide by 33 ft long, or mats may be cut to size. The 2-ft-wide roll sells for $4.82; delivery is from stock.

Tepromark International Inc., 206 Mosher Ave., Woodmere, N. Y. 11598. Phone (516) 569-4533 [477]



Rubalit substrates, an alumina compound developed by Rosenthal Technik, are currently offered in four compositions. All are suitable for die-stamping and for pressing or laser cutting. Rubalit 708 contains 96% alumina and is intended for thick-film substances and potentiometers. Rubalit 710, which contains 99.6% alumina, was developed for substances in thin-film and microwave applications, with precisely defined, smooth surfaces and with a closely controlled dielectric constant. Rubalit 711 is an opaque ceramic that contains 92% alumina and is of use in lids and special substrate applications. And Rubalit 717 with 99.5% alumina is offered as metalized substrates in thicknesses of 0.27 to 0.635 mm. Pricing averages $0.03/in.^{2}, with delivery from stock.

Rosenthal Technik North America Inc., 100 Niantic Ave., Providence, R. I. 02907. Phone (401) 943-2200 [478]

Tra-Bond F 120 is a two-part medium-viscosity epoxy adhesive and cures quickly at room temperature. Fully cured, it is nearly transparent, shrinks minimally, has mechanical and electrical insulation properties, and develops strong bonds to many materials used in optic and fiber-optic products. Tra-Bond may be bonded to Pifax and other glass- or plastic-core cables and to various types of single- or multi-channel plastic or metal terminations and connectors. It is available for immediate delivery in a range of premeasured two-component Bipax packages. In quantities of 1 to 24, a 2-g packet sells for $1.70 and a 24-g package for $3.30.

Tra-Con Inc., Resin Systems Division, 55 North Street, Medford, Mass. 02155. Phone (617) 391-5550 [479]

Dow Corning 1-2577 elastoplastic silicone conformal coating is a clear, tough, glossy resin for protecting circuitry where maximum reliability is required, as in automotive electronics, fire alarms, process controls, energy control modules, instruments, and computer modules. It can be cured at room temperature, but the cure rates can be accelerated. The coating has good dielectric properties at both high and low frequencies and better thermal and mechanical shock resistance than previous silicone resins. It is serviceable from -65° to $+200^\circ$C. In 440-lb drums, the resin costs $9/lb; delivery is from stock.

Dow Corning, Midland, Mich. 48640. Phone (517) 496-4510 [480]

A proprietary copper conductive transfer film is useful in low-voltage switch and circuitry applications. The metalized polyester film is available in roll form and suitable for graphic, thermoplastic, and thermoset materials. It meets the demand for low-cost touch-switch technology in the microelectronics used to operate computers, consumer appliances, and elevators. It replaces the slower, more costly methods of silk-screening a conductive ink onto a film surface or chemically etching a copper foil laminate. The film is hot-stamped just as a conventional foil would be on existing equipment with a rubber or metal die. Formulations are available for adhesion to a range of thermoset materials. Prices average $0.30/ft^2, with delivery taking up to four weeks on stock items. Custom orders take longer, depending on requirements.

Web Technologies Inc., 27 Main St., Oakville, Conn. 06779. Phone (203) 274-0388 [411]

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Broomer Research Corp., 23 Sheer Plaza, Plainview, N. Y. 11803. Phone (516) 249-1544 [412]

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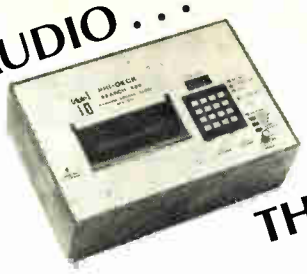

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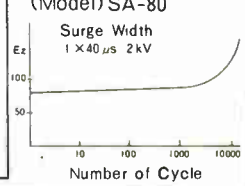
SA-140	140 ±10%	10^{10}min	1.5	3000
SA-200	200 ±10%	10^{10}min	1.5	3000
SA-250	250 ±10%	10^{10}min	1.5	3000
SA-300	300 ±10%	10^{10}min	1.5	3000
SA-7K	7000 ±1000V	10^{10}min	—	5000
SA-10K	10000 ±1000V	10^{10}min	—	5000

Change of Ez by cycling discharge



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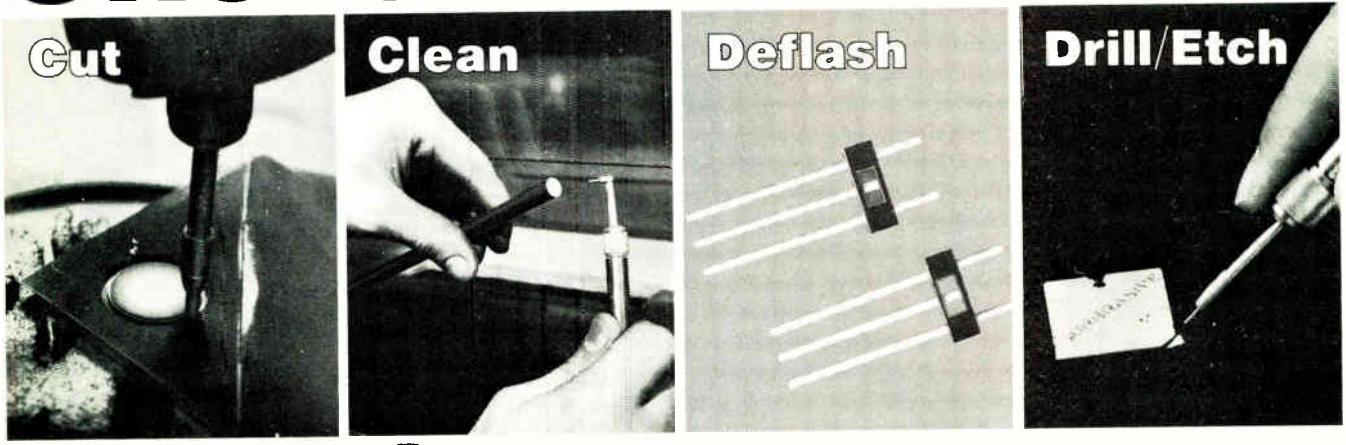

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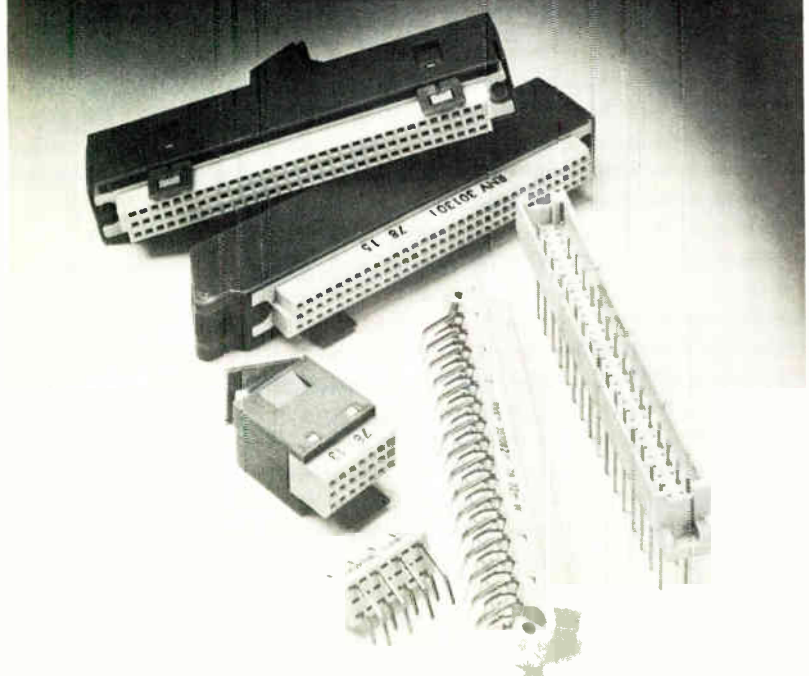

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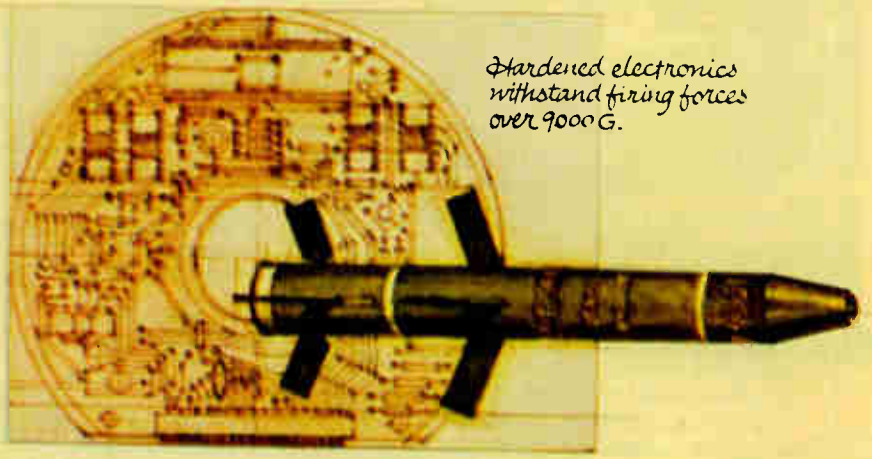

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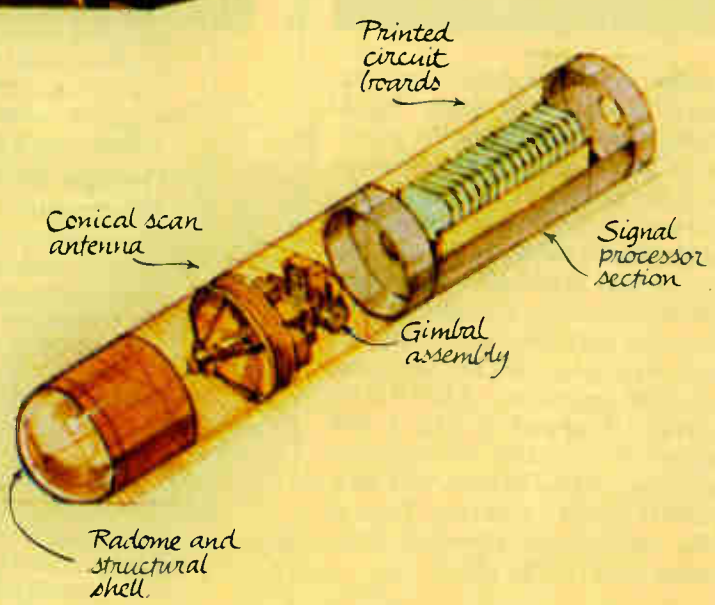

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surements, and Automated Parametric Test Systems divisions. The catalog lists product descriptions, capabilities, features, specifications, and application information. In addition, each major section is prefaced with technical data, theory of operation, and design considerations relative to the instruments described. For a copy, contact Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, Ohio 44139. Phone (216) 248-0400 [428]

Microwave product information. The complete line of MIC microwave and intermediate- and radio-frequency products is described in the RHG Electronics Laboratory catalog. The 112-page catalog contains three sections of detailed technical data on i-f and rf products, MIC mixers and mixer preamplifiers, and microwave relay links. Another section describes custom devices and subsystems. Technical information is included on the relationship of log amps to other components, linearity measurement, phase and gain matching, and mixer specifications, as well as standard specification test methods. Copies of catalog No. 200 are available from the Sales Department, RHG Electronics Laboratory Inc., 161 East Industry Court, Deer Park, N. Y. 11729. Phone (516) 242-1100 [423]

Integrated circuits for industry. A 12-page brochure covering Siemens Corp.'s integrated circuits for industrial applications lists the various IC types, packages, package dimensions, descriptions, and electrical characteristics as well as general product information. The ICs include linear and digital circuits in bipolar, MOS, and mixed technologies for use in a broad range of applications including industrial applications. Copies of the brochure are available from the Components Division, Siemens Corp., 186 Wood Ave. South, Iselin, N. J. 08830 [424]

Instruments for rent. Genstar Rental Electronics' catalog lists over $45 million worth of electronic instruments for rent throughout North

America. All items listed include a description plus the 30-day rental price. Items are catalogued alphabetically by product type and are divided into 47 categories, which range from amplifiers to test chambers. There are analyzers, generators, and meters as well as sophisticated instruments such as desktop computers, microprocessor instrumentation, programmable read-only memories, programmers, oscilloscopes, magnetic-tape recorders, and data terminals. Copies of the catalog are free and may be obtained by contacting Genstar Rental Electronics Inc., 19527 Business Center Dr., Northridge, Calif. 91324. Phone (213) 993-7368 [425]

Software directory. Datapro's Directory of Microcomputer Software helps to identify, evaluate, and select microcomputer software. Detailed descriptions of over 2,000 software products are arranged in an easy-to-compare format. More than 1,000 vendor profiles, including hard-to-locate suppliers, provide information on product lines, application emphasis, and sales volume. The directory is divided into four major indexes: applications area, product name vendor or product name, and cor puter system. The two loose-leaf v umes, 12 monthly supplem monthly newsletter, and telep inquire services cost $290. D Research, 1805 Underwood Delran, N. J. 08075 [426]

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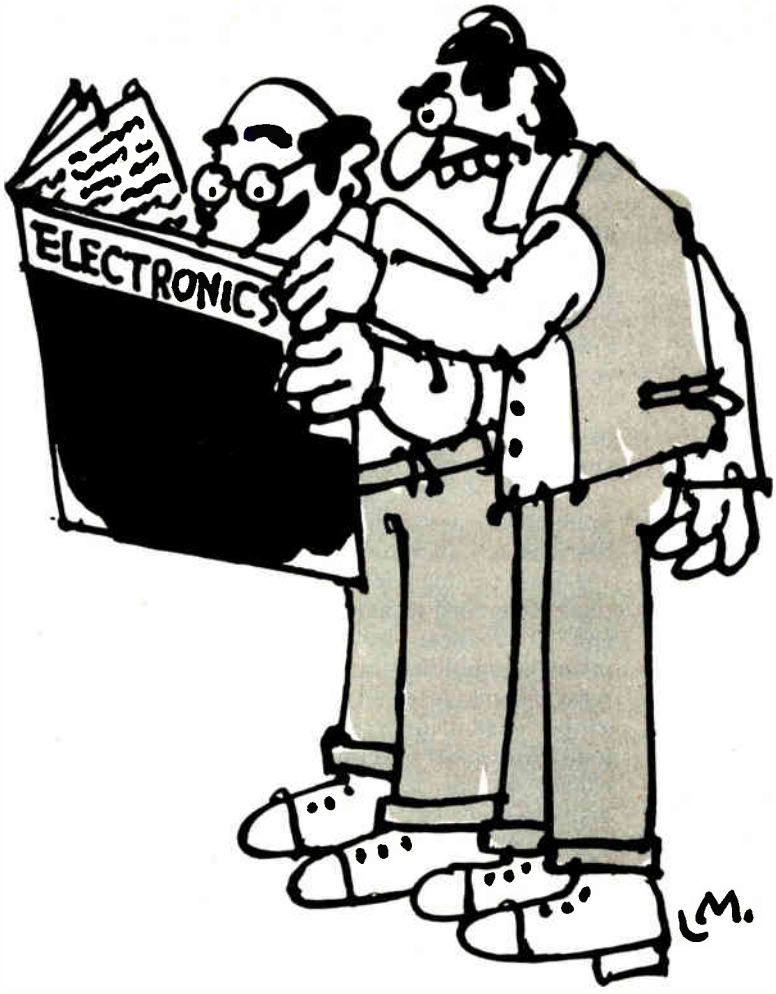

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Products Newsletter

Smart interface unit could replace diskette in printer applications

A programmable buffered interface unit from Microcompatible Inc., Atlanta, Ga., may eliminate the need for a disk drive in some small-computer applications. **The Microcue stores either 16- or 32-K bytes of data in MOS random-access memory, and interfaces almost any small computer** with a parallel or RS-232-C serial interface output port with almost any printer. Useful in memory-limited applications, it can store up to 16 pages of text, manage printer functions without incurring central-processing-unit or controller overhead, and free a disk drive that would have been needed for printing. The Microcue accommodates bit rates of 110 to 9,600 b/s. Units are available with up to four inputs and outputs at prices from $299 to $699.

Small chip stores, speaks four words

A Chicago start-up firm known as Data Voice Corp. is paying no heed to speech synthesis techniques that allow large vocabularies by minimizing memory requirements. The company's first product, called Cheaptalk, is a 3-by-3-in. voice-synthesis circuit board that is a memory hog; but by using data rates of 12,000 to 20,000 b/s, the firm says that **extremely high voice quality can be achieved at a low price for applications that need only a 1 to-4-word vocabulary.** Cheaptalk uses a 32-K erasable programmable read-only memory for storing a maximum of **2.5 s of waveform-encoded speech.** The board will sell for $54 in 100-unit quantities and for $30 in quantities of 2,500 or more. Twenty-five standard words or phrases are available, but custom vocabulary encoding is also available for $100.

High-speed network gets satellite capability

Network Systems Corp., Brooklyn Park, Minn., is adding satellite communications capability to its Hyperchannel line of high speed network products. Developed under funding from Satellite Business Systems, the model S720 satellite link subsystem will employ an RS-449 interface, allowing **full-duplex data transfers at rates up to 44.7 Mb/s** between geographically separate Hyperchannel networks. Priced at about $85,000, the S720 will be available in early 1982.

PROM burner is software controlled

Programming most families of erasable programmable read-only memories, the Ackerman Digital Systems Prom Blaster is controlled by software running under either Digital Research's CP/M or the Elmhurst, Ill., firm's 6809 single-board computer monitor, Adsmon. **The Prom Blaster uses a single 28-pin zero-insertion-force socket and programs 1-, 2-, 4-, or 8-K erasable PROMs,** including three-supply parts. With the high-voltage supply on card, it works with the S-100 bus as an input/output device, has phantom slave and extended device options, and includes wait states. The cost of the kit is $199 and includes PromWriter software.

S-100 computers use streaming drive for back-up

Measurement and Controls of Orange, Calif. is introducing versions of its 2800 family of S-100-bus microcomputers next month, both using Archive Corporation's 20-megabyte streaming tape drive. **The new systems use existing 2800 configurations,** but replace an 8-in. floppy with the 90 in./s streamer, backing up a 10-megabyte Memorex Winchester. The single user CP/M system sells for $11,430, while the multiuser MP/M model lists for $12,500 in single units.

Career outlook

Academia doesn't pay

Many undergraduate engineering students sign up for their first industry job with the expectation of getting two or three years of experience—and some money in the bank—before returning to school for a graduate degree.

Anyone doing so, believing it will eventually mean more money in the long run, may be making a mistake. "There's no great economic inducement for going to graduate school," says William S. C. Chang, head of the microelectronics program at the University of California at San Diego. "Graduate students are poorly paid. BSEE holders entering industry will make a salary of around $22,000 to $25,000" and in four years will be making as much as those who are fresh out of school with a Ph. D.

For those who stay in school long enough to attain a Ph. D., the economic inducement to stay on and teach is lacking. Says Chang, "A beginning Ph. D. in industry gets about $35,000 a year—at a university only $25,000."

Attractions. Moreover, Chang points out, industry can attract bright and highly schooled engineers because high-technology firms can, and do, spend heavily for research and development in well-equipped laboratories. Most universities, on the other hand, are having a hard time keeping their laboratory equipment up to date. Even a school like the University of Illinois, Urbana-Champaign, has laboratories that are still working with hardware based on vacuum-tube technology, says G. W. Swenson, head of the department of electrical engineering.

However, the greatest need in academia is for engineers with advanced degrees. Says one EE department head, "Our labs aren't quite up to snuff, but we could live with that if we could find qualified people. If they were out there we could hire them. But they're not going on to grad school and thinking, 'I'm going to get a Ph. D. and teach.'"

So the nation's universities and colleges are looking for ways to attract experienced engineers with high-level training back into the classroom—at least part time. "I advocate strong university-industry-governmental interrelationships," says Lester Gerhardt, director of electrical, computer, and systems engineering at Rensselaer Polytechnic Institute, Troy, N. Y. "I would encourage more Ph. D.s and higher degrees and regular leaves of absence—not only for training, but for adjunct professorships."

Funding. Faced with Federal funding cuts just when they need more money to pay competitive salaries to engineering professors and give them up-to-date laboratory equipment, engineering schools are now counting on industry for money.

More industrial funding is an obvious solution in meeting the rising cost of educating EEs, maintains Irene Miller, assistant chairman of the electrical engineering department at Stanford University, Palo Alto, Calif. Miller cites the example of the Stanford Center for Integrated Systems, which begin with the help of a dozen industrial sponsors such as IBM, General Electric Co., and Xerox Corp. Member companies can send staff members to the center to design integrated circuits with a fast turnaround.

Ten grand a head. According to Swenson of the University of Illinois, "Industry is going to have to start training engineers and contributing more to universities. A $10,000 donation per student hired wouldn't be unreasonable. Society is going to need more engineers, but if you haven't the money to hire faculty or teaching assistants or to upgrade labs, then you have to cut back."

"Numerically," Swenson continues, "industry gives us a substantial amount; ideally, not enough. The trouble is the gifts don't necessarily address our most urgent needs."

With engineering enrollments at record levels because of the current shortage of engineers, the schools find it hard to compete with industry for the brainpower they desperately need. Paradoxically, whether they will be able to do that depends a lot on industry. **-Andrew McCann**

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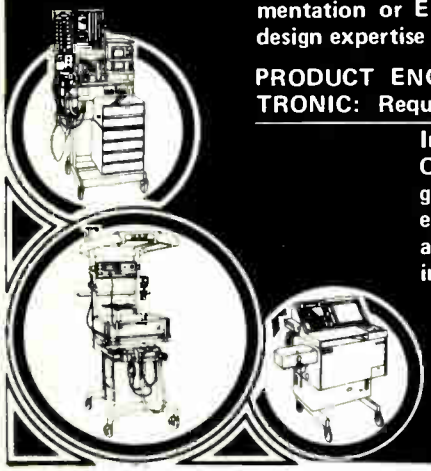

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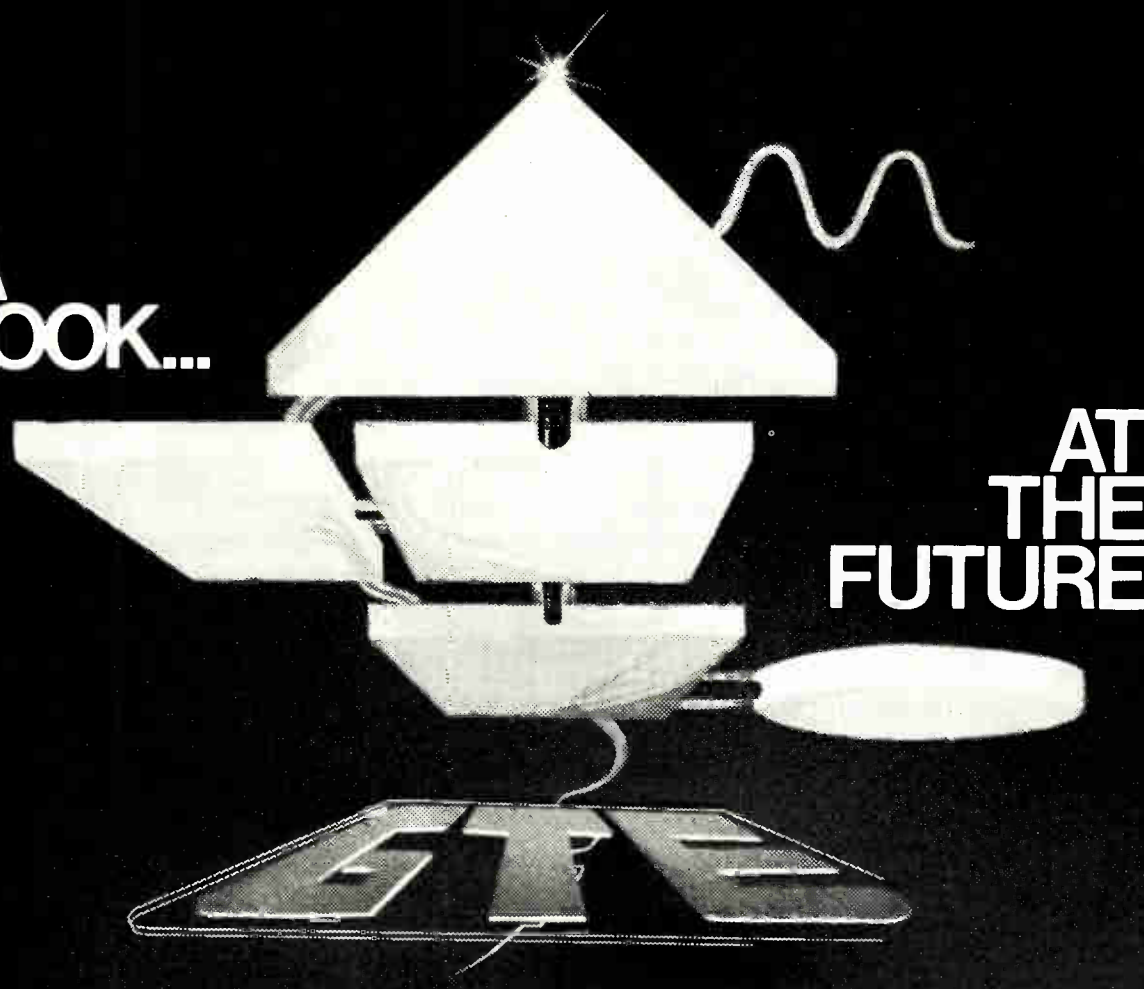

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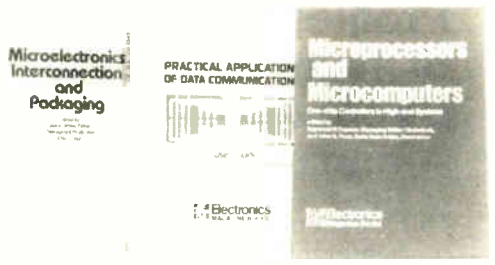

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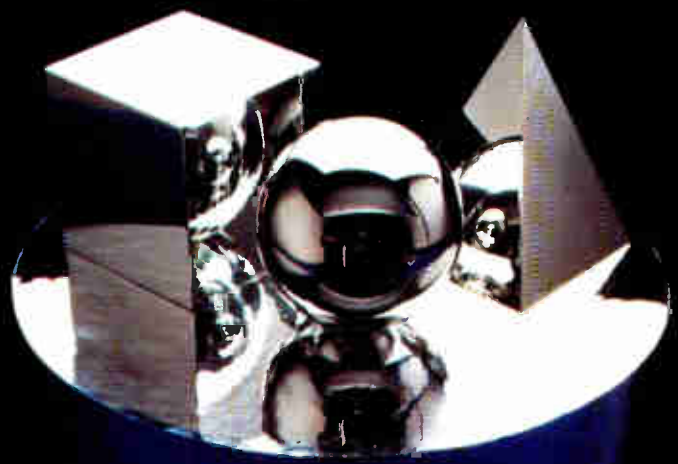

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