AUGUST 11, 1981

SPECIAL REPORT: DEMYSTIFYING MICROSYSTEM MEMORY MANAGEMENT/119

What nationalization means for electronics in France/81

Logic arrays take on analog circuit functions/109

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Electronics®

HOW CAN YOUR MICROPROCESSOR BOARD HELP TEST ITSELF?

It's ironic. The very intelligence that makes your products excel can also be the obstacle that makes testing difficult. Why? Because those intelligent microprocessors are difficult to model. And until they're put to work via code, they're no smarter than any other piece of silicon. Can they be awakened and used to test themselves? Let's look at some of today's testing techniques and see.

Alternatives for testing microprocessor boards.

Board testers available today generally use one of four approaches:

1) Simulator board testing. This is an edge-connector and guided probe testing technique that relies on patterns from a simulation model. The processor is usually removed from the board, and input patterns applied. Output patterns are then compared with those predicted by the simulator. If the patterns match, the support logic is judged good. Next the processor is inserted and different patterns are applied. Now the outputs are compared to those predicted based on the original model plus a high-level software model of the processor. If those patterns match, the entire board is said to be good. Excessive time can be consumed generating both high-level models and testing software.

2) In-circuit testing. Using a bed-of-nails fixture, contact is made with each logic circuit on the board, including the μP. Pulses are applied to input pins of each device. Outputs are compared to those predicted from device truth tables supplied by manufacturers. These libraries are programmed for common device configurations and must often be modified for actual configurations.

3) Comparison testing. In this edge-connector and guided probe method, a known good board must be available as a reference. The known and unknown are initialized, synchronized and then are compared by applying preprogrammed instructions or patterns, or by stimulating with pseudorandomly generated pattern sets. If the outputs match, the unknown board passes.

4) Processor-based testing. This technique uses the intelligence of the μP on the board. The board is powered up and operated at speeds up to 10 MHz using preprogrammed test code resident in the test system or on the board itself. The on-board μP executes this code to exercise the address and data buses, and support circuitry. Key nodes are monitored with signature analysis to detect faults.

Why does HP use processor-based testing?

Our experience in testing μP boards has revealed several benefits of processor-based testing. That's why we've incorporated it into our 3060A Board Test System with the High Speed Digital Functional Test option.

First of all, boards are tested at speed, with all components, buses and control lines operating in modes similar to actual use conditions. The result? Ability to test pins which are not exercised unless the processor is executing instructions (Fig. 1), plus detection of faults related to the address and data bus structure and timing faults.

Examples of Processor Pins Testable Only With Software

	8085		6800	Z80
Interrupts	INTR TRAP	RST 7.5 RST 6.5 RST 5.5	$\overline{IRQ}$ $\overline{NMI}$	$\overline{INT}$ $\overline{NMI}$
Control Outputs	S_0 S_1 $IO/\overline{M}$	$\overline{RD}$ $\overline{WR}$	VMA $R/\overline{W}$	$\overline{M1}$ $\overline{RD}$ $\overline{WR}$ $\overline{HALT}$
Other	SID SOD			

Fig. 1

In addition, processor-based testing permits fault detection using Signature Analysis (SA), which is complimented by new software in the digital functional testing package. SA allows rapid fault isolation to the component level on active bi-directional buses. That means high throughput in production.

Furthermore, with the programming aids available from HP, functional test program development time is minimized for μP, memory and IO boards. For example, you can either modify existing routines provided by HP, build your own stimulus routines using HP-supplied building blocks, or develop stimulus programs on a development system and download to the 3060A. The bottom line of processor-based testing is fast test program development, high throughput, and high yield at the final product level.

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To find out how processor-based testing can benefit you, write: Hewlett-Packard, 1820 Embarcadero Road, Palo Alto, CA 94303. Or, call the HP regional office nearest you: East (201) 265-5000, West (213) 970-7500, Midwest (312) 255-9800, South (404) 955-1500, Canada (416) 678-9430.

091/7

**HP Circuit Testers—
The Right Decision**

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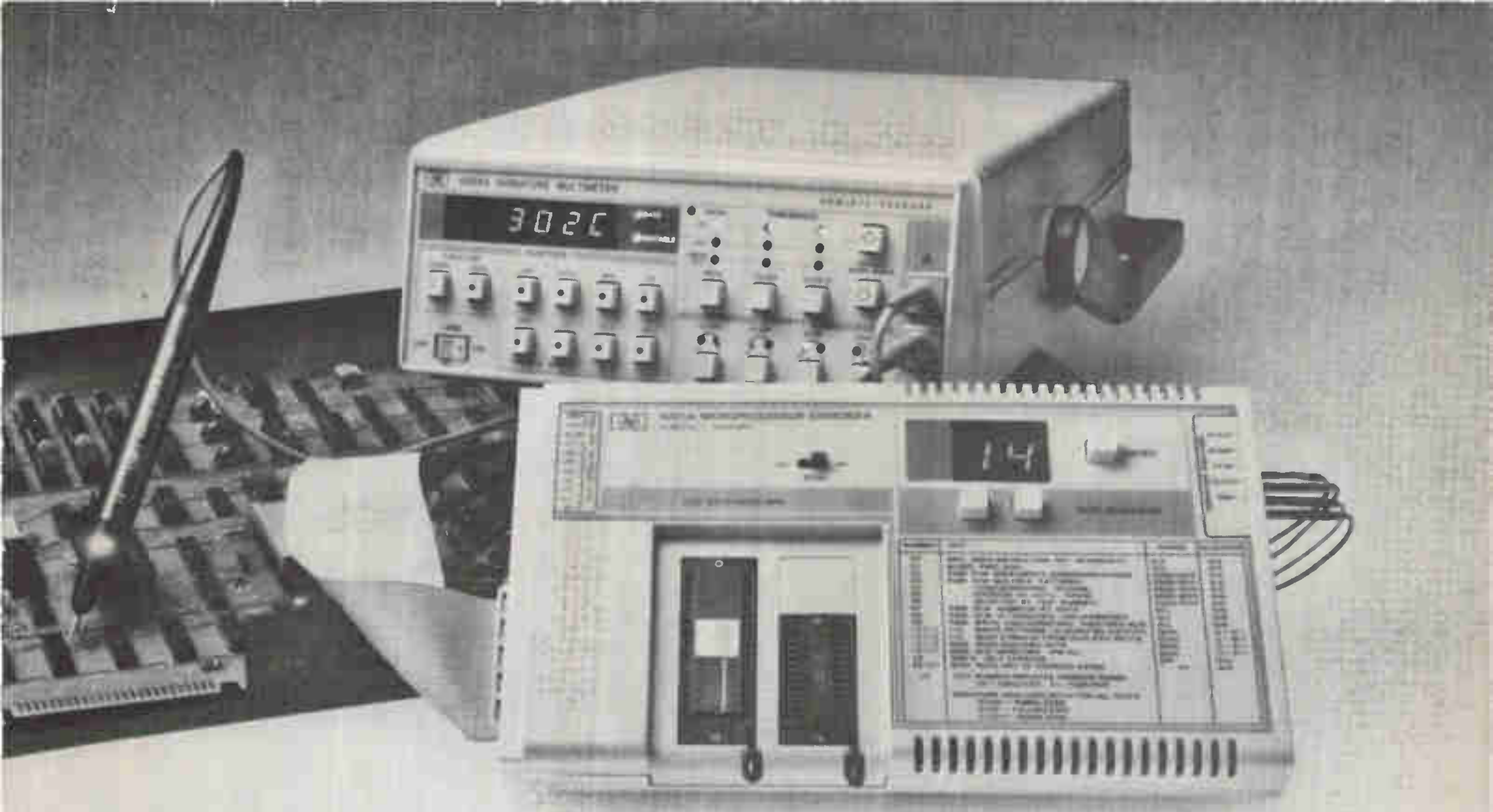

Now, HP has two more ways to cut digital troubleshooting costs.

5005A Signature Multimeter.

Before signature analysis (S.A.) troubleshooting microprocessor boards was tedious, time-consuming and costly. S.A. changed this by giving each complex bit stream its own unique hexadecimal signature, enabling technicians with minimum training to identify faulty nodes.

Now, the HP 5005A Signature Multimeter goes the next step by combining a high speed signature analyzer with a DMM, frequency/time interval counter and logic probe in one compact, lightweight package. This versatile combination adds a new level of convenience, making it easier than ever to track down faulty components in both service and production environments.

The 5005A Signature Multimeter offers features new to S.A.: preset logic thresholds for TTL, ECL and CMOS; variable thresholds (±12.5V); a clock-qualified Signature Analysis mode; and a 20 MHz clock rate coupled with a 10ns set-up time for high speed logic. It only weighs 8 lbs. (3.5 kg.), so it travels anywhere. The price is $2500.*

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Here's a simple way to take advantage of S.A., even if it isn't designed into your product. Just insert your board's microprocessor into the new HP 5001A Microprocessor Exerciser, plug the 5001A into the empty board socket, and use its ROM to run test stimulus programs. The 51 self-contained S.A. stimulus programs thoroughly exercise the microprocessor, buses, ROM, RAM and I/O circuitry. Easily monitor the resulting signatures at your product's test points with HP's 5004A or 5005A Signature Analyzers. The 5001A is available for the 6800 microprocessor now—8085 and Z80 soon. 5001A price is $900.*

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Circle 1 on reader service card

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Electronics
The International Magazine of Electronic Technology
Vol. 54, No. 16 • August 11, 1981

Electronics

Highlights

In the next issue . . .

Wescon preview . . . a pair of local networks . . . direct mounting of chip-carriers . . . venture capital: an Inside the News story . . . a memory management chip.

August 11, 1981 Volume 54, Number 16
105,059 copies of this issue printed

Electronics (ISSN 0013-5070). Published every other Tuesday except the issue of Monday, Nov 30, by McGraw-Hill, Inc Founder James H. McGraw 1860-1948 Publication office 1221 Avenue of the Americas, N.Y., N.Y 10020; second class postage paid at New York, N Y and additional mailing offices

Executive, editorial, circulation and advertising addresses: Electronics, McGraw-Hill Building, 1221 Avenue of the Americas, New York, N Y 10020. Telephone (212) 997-1221 Teletype 12-7960 TWX 710-581-4879. Cable address: M C G R A W H I L L N E W Y O R K.

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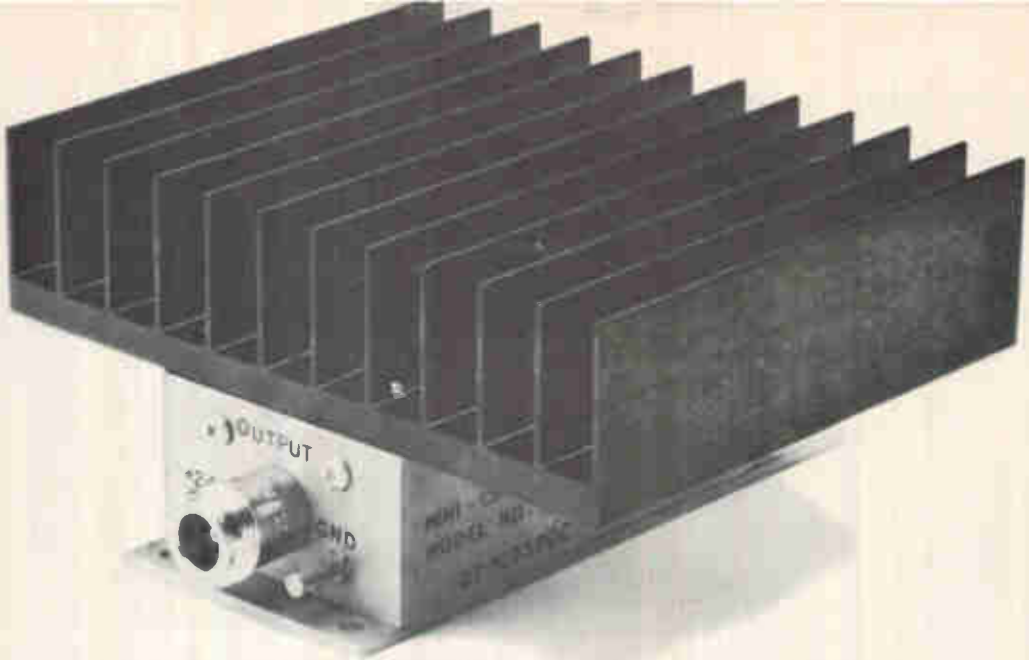

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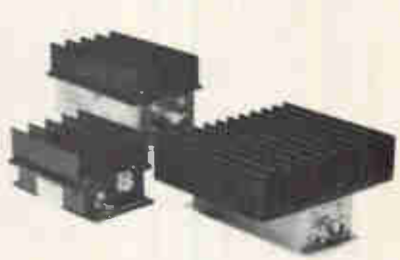

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ZHL-3A	0.4-150	24 Min	±1.0 Max	+29.5 Min	11 Typ	+38 Typ	+24V	0.6A	199.00	(1-9)
ZHL-1A	2-500	16 Min	±1.0 Max	+28 Min	11 Typ	+38 Typ	+24V	0.6A	199.00	(1-9)
ZHL-2	10-1000	15 Min	±1.0 Max	+29 Min	18 Typ	+38 Typ	+24V	0.6A	349.00	(1-9)
ZHL-2-8	10-1000	27 Min	±1.0 Max	+29 Min	10 Typ	+38 Typ	+24V	0.65A	449.00	(1-9)
ZHL-2-12	10-1200	24 Min.	±1.0 Max	+29 Min.*	10 Typ	+38 Typ	+24V	0.75A	524.00	(1-9)
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VLSI men. Project leaders for ITT-Intermetall's digital TV system are, from left, Daniel Mlynek, Peter Flamm, Edmund Zähringer, Herbert Elmis, and author Thomas Fischer.

To designers at ITT Intermetall GmbH, the Freiburg, West Germany–based headquarters company of the ITT Semiconductors Group and a long-standing supplier of integrated circuits to the television industry, it has long been apparent that the way to go in TV set design is digital. Only by turning to digital TV circuits, implemented with large- and very large-scale integration techniques and offering a high component-replacement factor, can set makers lower their costs.

Recognizing that, "we embarked on a development effort that turned out to be the most ambitious one our firm has undertaken since becoming a member of the ITT group in 1965," points out Thomas Fischer, one of the five project leaders and author of the article beginning on page 97. "Thus far, we have invested some 140 man-years and spent about 5,000 hours of computer time in the digital-TV effort," he notes.

Ever since Intermetall introduced the first MOS IC for color TV in 1973, engineers at the Black Forest company have kicked around the idea of applying digital techniques to receiver design. Then, in 1977 the first experiments by a two-man team were conducted. "The results were so encouraging that a decision to develop the necessary ICs with 3-micron technology was made the same year," Fischer recalls. The prime moving force in this effort has been Yugoslav-born Ljubomir Micic, now managing director of ITT Semiconductors Worldwide [*Electronics*, Nov. 6, 1980, p. 14].

The design and layout began in the fall of 1980, and the first circuits were successfully tested early this year. A kit with two LSI and six VLSI chips are planned to be announced at the Radio and Television Exhibition in West Berlin, Sept. 4 through 13. First samples of the kit should be shipped to key customers in December, and it will be generally available early next year.

Having great stores of memory available to microprocessor-based systems is a logical extension of the processing power of the latest 16-bit chips, whose addressing range reaches to megabytes. But, as microsystems and software editor Colin Johnson points out in his special report beginning on page 119, effective schemes are needed to manage all that memory. "Many of the current 16-bit processors are as fast as the mainframe of five years ago," he says, "but to harness that speed you need memory management." In his report, Colin looks at the various schemes chosen by the microprocessor makers. "The 16-bit microsystems will really come into their own when the memory management chips start being used," he predicts.

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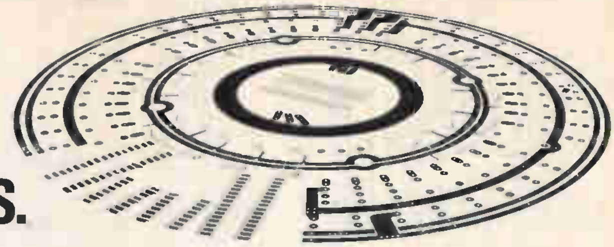

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Circle 7 on reader service card

Readers' comments

Guesstimating defense costs

To the Editor: In "The Pentagon goes shopping for technology" [June 30, p. 91], the chart entitled "Who spent what for defense in 1980" lists a total of $142.7 billion spent by the United States, while the per capita U. S. expenditure is listed as $1,644. A bit of quick division will show that, judging by your figures, the population of America is roughly 60 million. Given the actual population, the expenditure should be $644 per capita.

Still, it is interesting to note that the U. S., even with the revised figures, still spends more on defense then the much-feared Soviet Union on a per-capita basis. It is also important to note that the statistics for Soviet Union are supplied by the Central Intelligence Agency, which is not a very reliable source of information these days.

The CIA's cost estimates are off for several reasons. First and foremost, it "guesstimates" how much the Soviet Union is spending by assuming (and this assumption is very incorrect) that, for example, a T-72 tank costs as much as an XM-1 Abrahms. However, the Abrahms is loaded down with all sorts of additional equipment that make it in reality just about twice as expensive to produce as the T-72.

The CIA also estimates manpower costs at a totally unrealistic level (by neglecting to take into account the simple fact that Soviet soldiers don't volunteer) and includes other basically incorrect statistics when compiling their figures for the Soviet Union. In reality, it is probably safe to assume that Soviet spending is about $30 billion less than estimated—in other words, less than ours. That sort of puts things in a different light, doesn't it?

Name withheld by request

Correction

In "Electronic lock boasts low cost and low power" (July 14, p. 127), the lines connecting pin 15 of the 4017 decade counter with pin 11 of the counter and pin 10 of the 4013 flip-flop should be omitted from the schematic.

News update

A-m stereo is not dead; it is being held prisoner by the Federal Communications Commission. After selecting a design from Magnavox from among five proposed a-m stereo systems and then reconsidering [*Electronics*, August 14, 1980, p. 55], the FCC has yet to come up with a new selection.

"At this point we are aiming at the first quarter of 1982," says Henry L. Baumann, chief of the broadcast bureau's policy and rules division. When the FCC asked industry for comments following its decision to re-evaluate a-m stereo, it was "inundated with volumes and volumes of data," he explains, and the selection process was slowed.

Focal point. A-m stereo was an important technical focal point at the June, 1980 spring consumer electronics show sponsored in Chicago by the Electronic Industries Association. Integrated-circuit makers seemed to be all over the mammoth McCormick Place exhibition hall demonstrating decoder chips for a-m stereo. Convention goers heard tell of a-m stereo's superiority in range over fm broadcasting, and how stereo would upgrade the quality of a-m broadcasts, giving a shot in the arm that would arrest the slow but steady audience decline. However, the January and June 1981 EIA consumer shows saw the subject given scant attention.

Magnavox, once the FCC's anointed, has little comment right now. It is choosing "to stay neutral for the moment and not antagonize the situation," according to Johan Koppier, manager of video planning, which includes a-m stereo.

Indeed, the industry seems exhausted by it all. The situation has moved beyond a point where the EIA could make any further contribution at a technical level, says Eb Tingley, the EIA's chief engineer.

It remains for the Commission to make its choice known. That may happen sooner than the 1982 due date cited by the FCC's Baumann. Rumors have it that the decision could come in the fall, says one individual well-wired into many companies in the industry. **-Gil Bassak**

When it comes to characterization, many LSI/VLSI devices can be difficult little creatures. Normal evaluation procedures just won't work.

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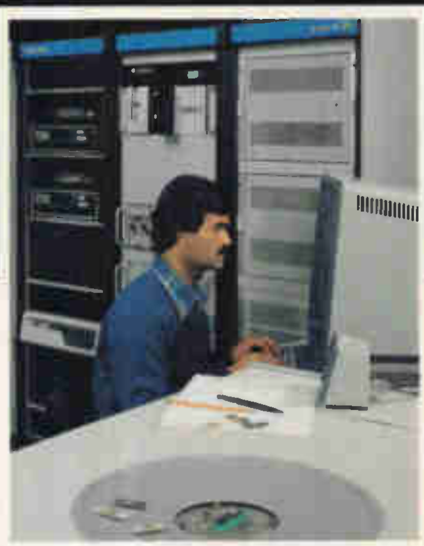

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Editorial

Industry's new burden: making the tax cuts work

Having tasted the wine of victory, the electronics industries—like every other American business—must now take their Federal tax benefits and make them work to revitalize the national economy. That will not be easy, nor will it come quickly.

In view of the recent slowdowns in sales and shipments of some electronics products, notably semiconductors, plus the serious stagnation that has set in in other large segments of the economy like cars and housing, the benefits of President Reagan's tax reduction program are not expected to significantly affect the economy before 1982 at the earliest. Continuing high interest rates are the heart of the problem, of course, and the White House has had little success so far in correcting that.

Admittedly, the electronics industries did not get everything they pushed for in the Reagan tax program—but they did get most of it. As the Electronic Industries Association's tax council staff director, Allan Spurney, put it, "We are very, very gratified." The American Electronics Association is not quite as pleased with all the provisions—it felt some did not go far enough—but, says the AEA's Kenneth Hagerty, vice president for Government operations, "We can live with it."

What the electronics industries will receive that should benefit them and other high-technology producers most are improved tax credits for increased investment in research and development over and above prior years, as well as a change in the Internal Revenue Service code that permits credit for all R&D performed in the U. S., rather than credit only in proportion to a company's domestic sales. These gains should enhance the competitiveness of U. S. manufacturers in foreign markets by encouraging exports, not discouraging them by disallowing R&D credits for products sold abroad. Accelerated depreciation rates, too, for plans, equipment, and vehicles are viewed as a major gain for high-technology industries like electronics, less so for so-called mature industries with smaller capital equipment demands.

As encouraging to U. S. sales abroad are provisions for major reductions in taxes for citizens earning income abroad, as well as an exclusion of funds provided to offset high-cost foreign housing. They should make it easier for U. S. manufacturers to recruit and retain American citizens in key foreign sales and engineering posts, rather than having to resort to using foreign nationals. Industry also won on the right to grant stock options that smaller producers say they need to recruit and retain personnel in a highly competitive domestic market, although those options are not unlimited but have a cap of $75,000 per person per year. The AEA pushed hard for unlimited options, although the EIA took no position on the issue.

Finally, industry won on the issue of being able to write off equipment grants to colleges and universities at book value rather than cost of manufacture. And that, it is believed, will encourage greater industrial support of engineering education across the nation.

What the electronics industries must now recognize—and act on—is that with this greater economic freedom come increased responsibilities. No longer will they be able to claim that their Government is not listening and responding to their needs in an increasingly competitive global market. The burden of making the program work is now on industry.

Still, the Reagan Administration has its responsibilities, too. Having placed all their economic eggs in one basket, so to speak, the President's men must now watch them very carefully and do their utmost to help American industries with programs to correct the nation's most critical economic problem—unacceptably high inflation. If that cannot be brought down, the new tax package may have little real value for the long term.

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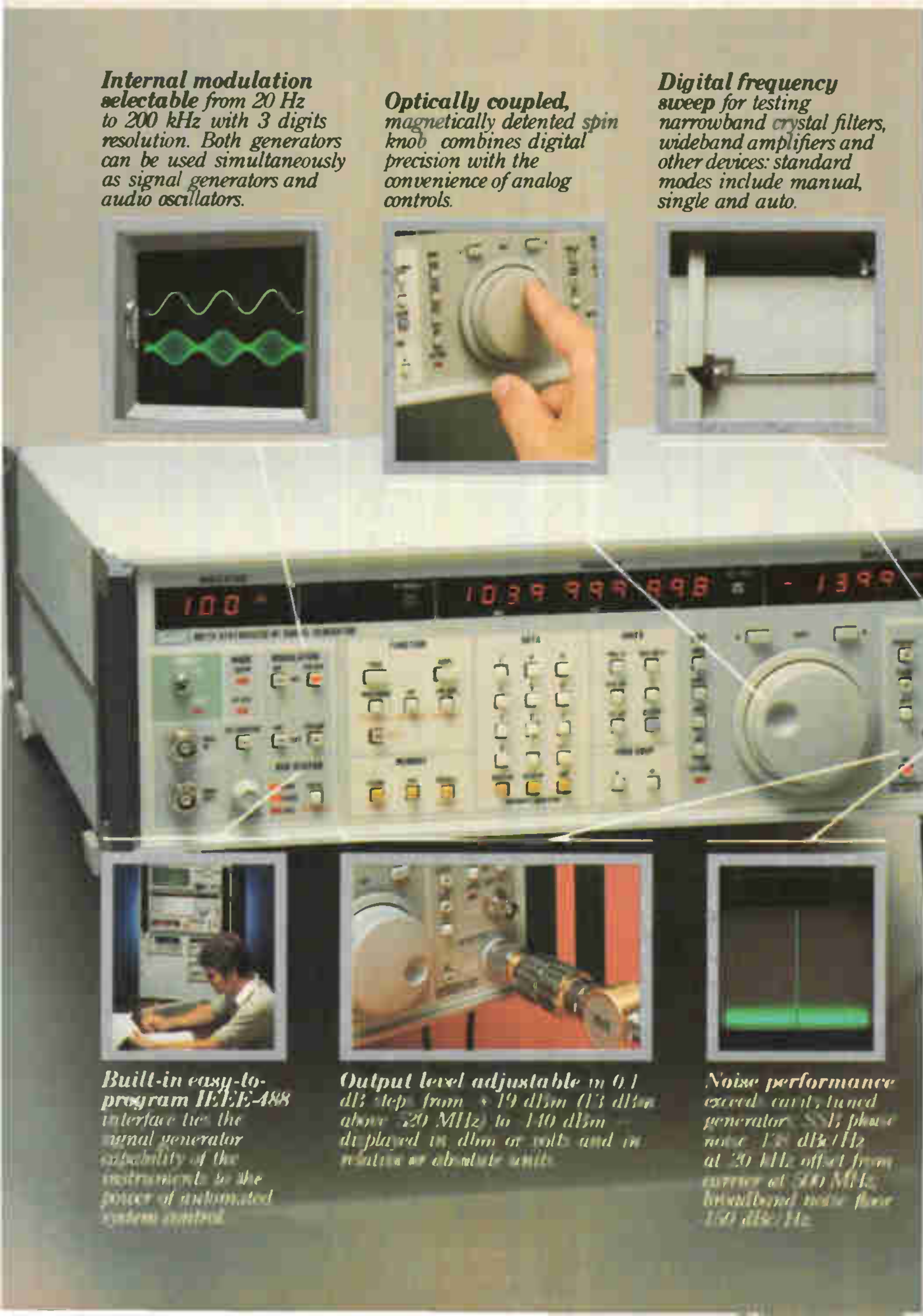

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People

Tooker stresses cautious path for Motorola Semiconductor

For all the near-20-year age gap, the new vice president and general manager of Motorola Inc.'s billion-dollar Semiconductor Sector views the job in much the same way as does his predecessor. "We'll keep running it carefully today," says Gary L. Tooker, 41, "while looking at new products and strategies for the future." On Sept. 1, he succeeds John R. Welty, who took over during recession-wracked 1975 and is credited with putting the Phoenix-based operation into its best shape ever. Welty was promoted to the position of chief corporate staff officer [*Electronics*, July 28, p. 46].

A 19-year Motorola veteran, Tooker moved up rapidly and most recently ran the International Semiconductor division. The youthful executive, in fact, sensed a disquieting parallel between challenges of the new post and those he faced when he began his international role in mid-1980. While professing cautious optimism that semiconductor orders, soft now, will improve as forecast, Tooker obviously is ready to move quickly if he has to, because he worries that high interest rates have the overall economy "teetering on the brink."

New top man. Gary L. Tooker will take over Motorola's semiconductor operation.

But the difference between Motorola now and in 1975, when it trailed the pack, is considerable: "We seem to be doing better than some competitors this time," he says. Tooker credits the difference to a better balance between MOS and bipolar devices. Just as important, there is strong penetration of the 68000 16-bit microprocessor into new designs, and strong acceptance of emitter-coupled-logic gate arrays. "Our new logic family in complementary-MOS should also do well," he adds.

Meanwhile, at corporate headquarters in Schaumburg, Ill., Stephen L. Levy is setting his sights on having a Japanese president within two years for Motorola's planned new Japanese operating company, to be known as Nippon Motorola Ltd. After 17 years with Motorola, the 59-year-old Levy will serve in the newly created corporate post of senior vice president, Japanese operations. It was Levy's promotion that touched off a string of promotions, including Tooker's, within the semiconductor group [*Electronics*, July 28, p. 46].

Bell Labs' Scanlon seeks to marry software and silicon

"We did a great disservice to computer science when we called it computer science," declares Jack M. Scanlon. That label led software practitioners to spend a wealth of time and effort in search of an underlying science for their craft. "And when they got tired of looking for a science, then they looked for a method," he observes.

While a great deal has been gained through this process—such as higher level languages, operating systems, and the like—"we still haven't made anywhere near the kind of progress in software that you can see in other technologies," con-

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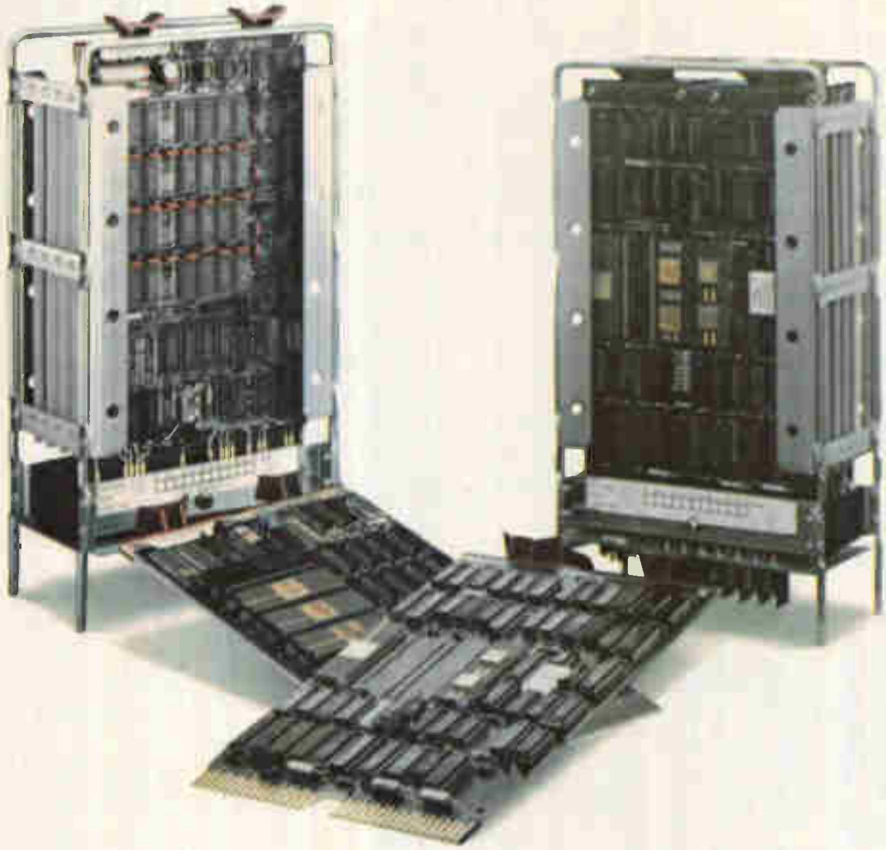

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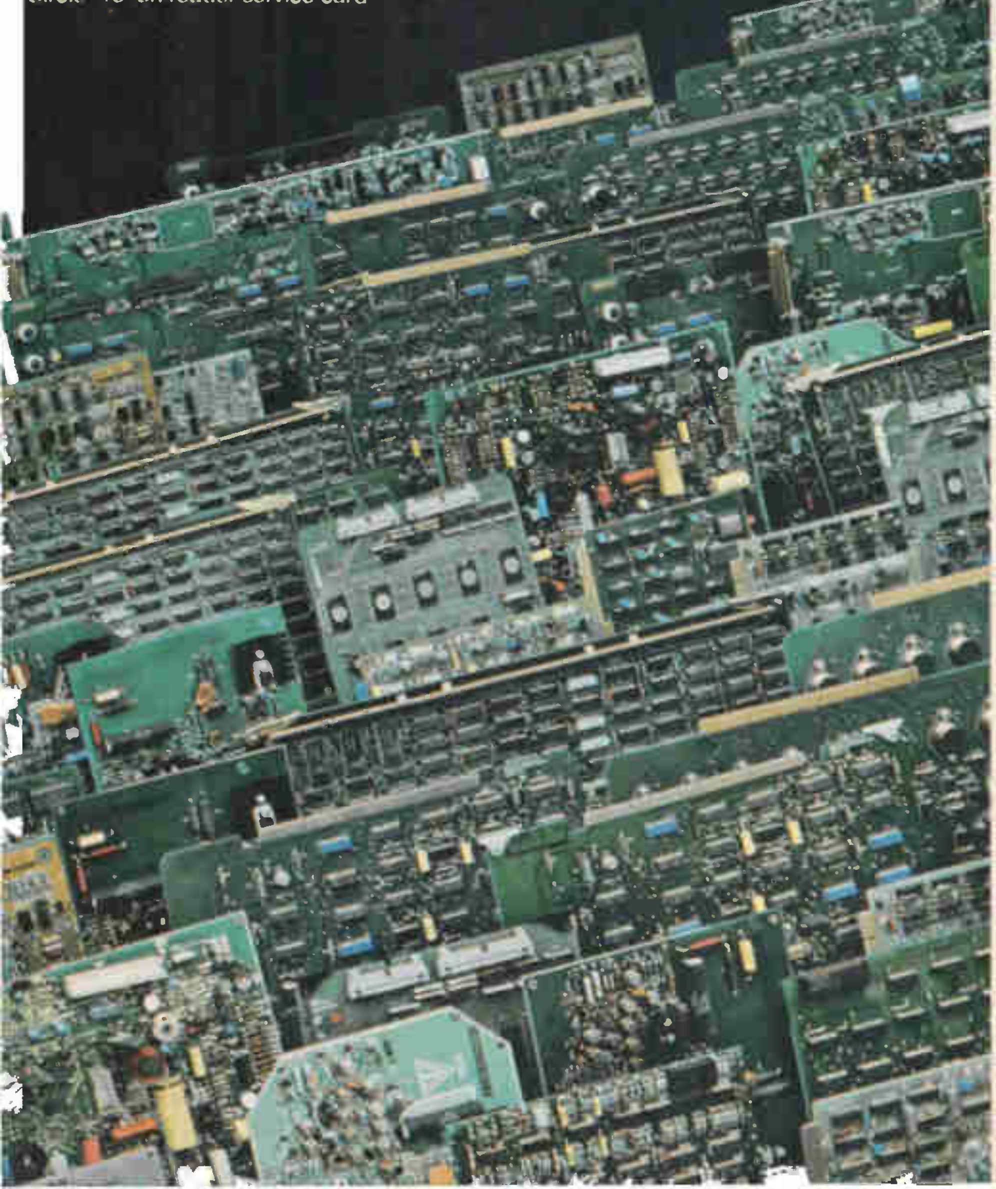


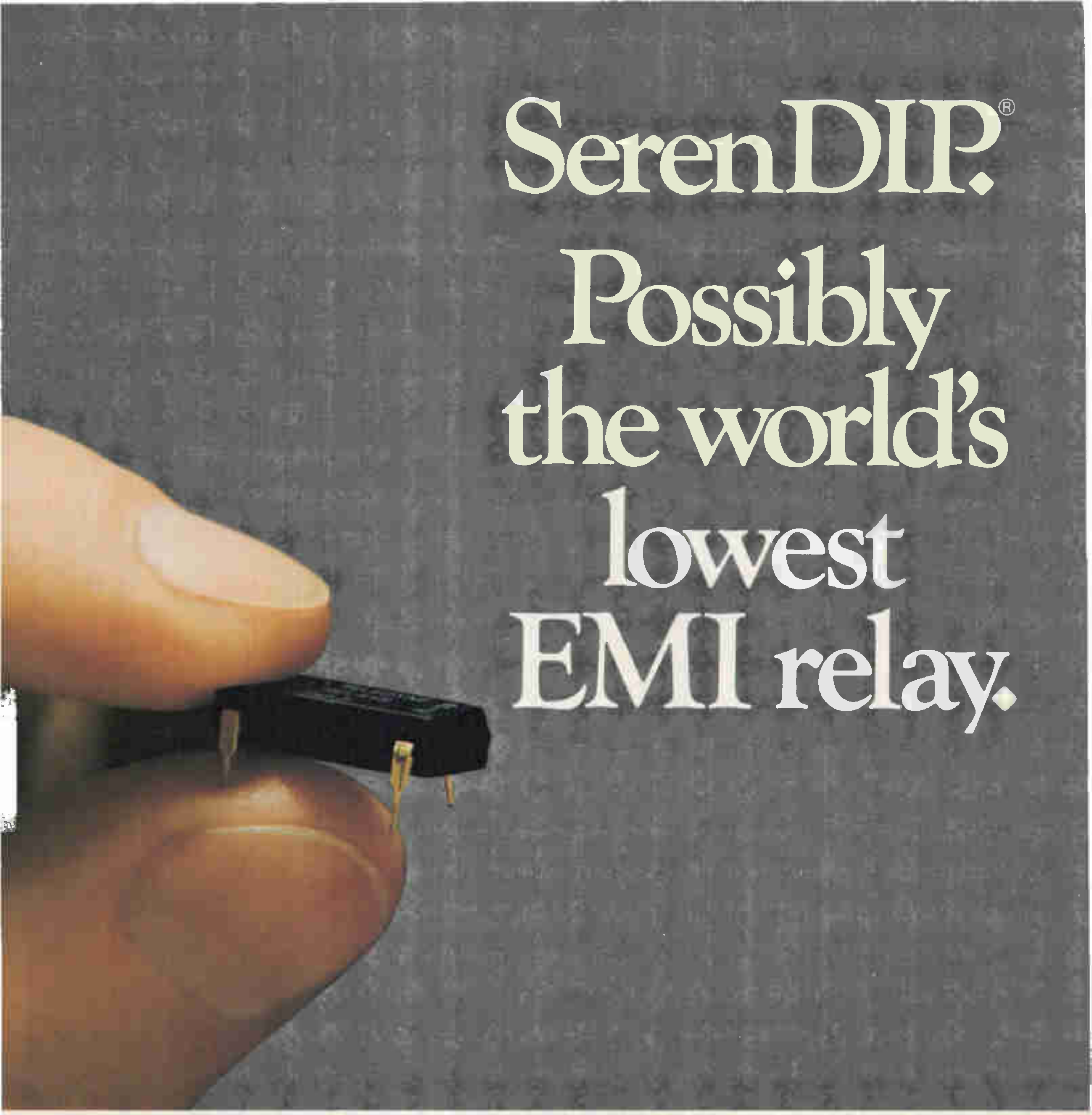
People

Software guru. Jack M. Scanlon oversees much of Bell Labs' software effort.

tends the 39-year-old Bell Laboratories official. It's time, he thinks, "to marry software to a faster moving technology, one based on science."

As executive director of the Processor and Common Software Systems division based in Naperville, Ill., Scanlon has a lot to say about software directions at Bell. The Utica, N. Y., native heads a division within Bell that counts in its ranks some 850 software and hardware professionals in five locations. His responsibilities include overseeing development of Unix operating systems, program languages, and software tools, as well as that of such microprocessors as the recently unveiled Bellmac-32 [*Electronics*, Feb. 24, p. 138] for Bell System applications.

Not surprisingly, the technology Scanlon says looks most promising as a wedding partner for software is silicon. The union, which he playfully dubs "silicom," will one day lead to systems by which a programmer sitting at a terminal will produce, not an applications program, but an actual prototype chip designed for a specific job and created by the system based on the programmer's instructions. "The custom design process that we associate today with silicon will be almost indistinguishable with what we see now as a software process," he predicts.



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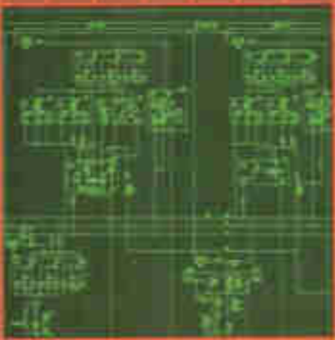

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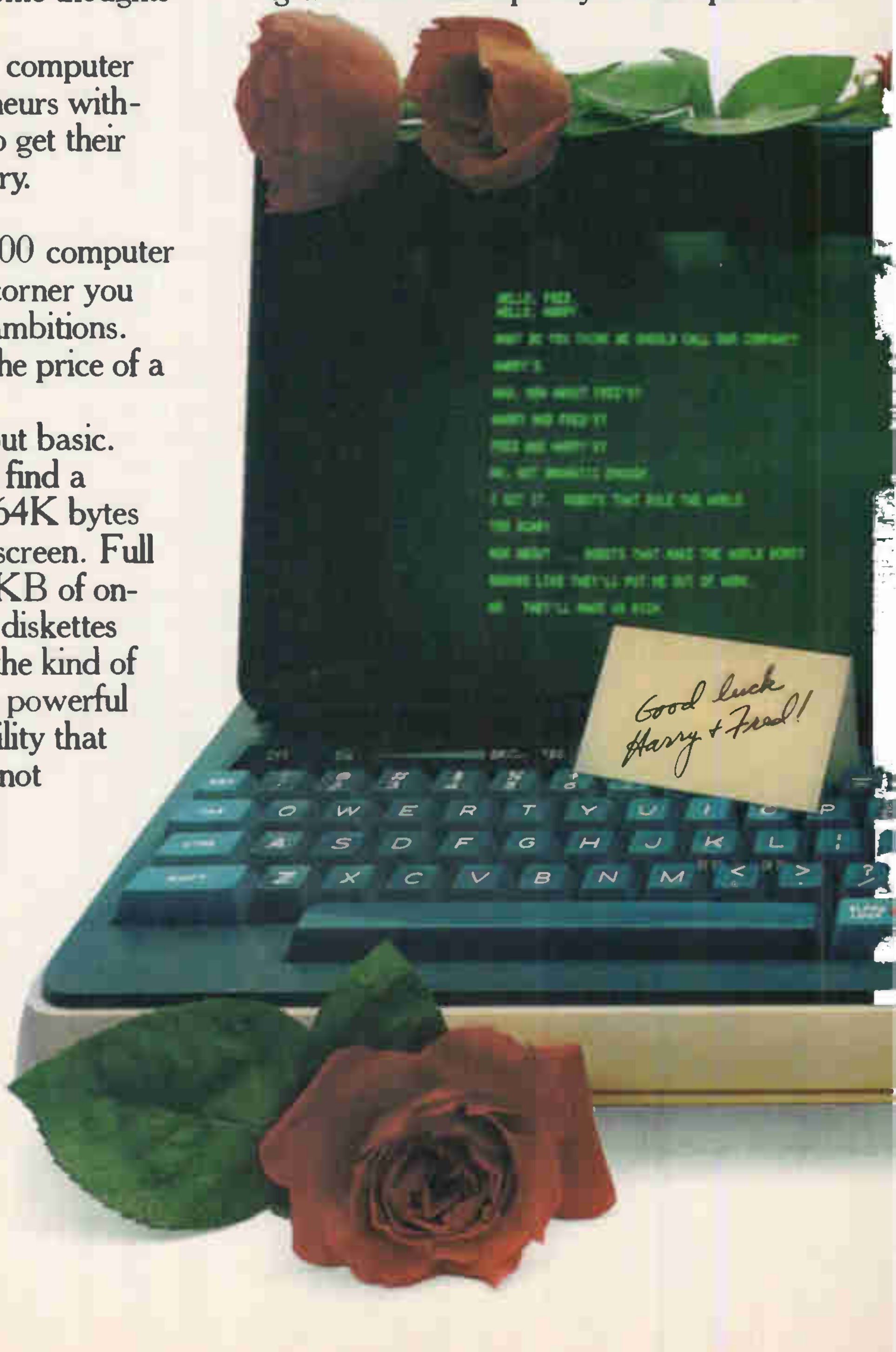

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Meetings

Compcon 81 Fall—22nd IEEE Computer Society International Conference, IEEE (Victor Basili, Department of Computer Science, University of Maryland, College Park, Md. 20742), Capitol Hilton Hotel, Washington, D. C., Sept. 15–17.

Wescon/81, IEEE (Electronic Conventions Inc., Suite 410, 999 N. Sepulveda Blvd., El Segundo, Calif. 90245), Brooks Hall, Municipal Auditorium, and Hilton Hotel, San Francisco, Sept. 15–17.

Eurodisplay '81—First European Display Research Conference, Society for Information Display and Nachrichtentechnische Gesellschaft im VDE (Gerhard Meier, Eckerstr. 4, D-7800 Freiburg, West Germany), Hilton Hotel, Munich, Sept. 16–18.

Third AFCET Congress on Pattern Recognition and Artificial Intelligence, Association Française pour la Cybernétique Economique et Technique (Jean-Paul Haton, 156 Blvd. Péreire, 75017 Paris, France), Palais des Congrès, Nancy, France, Sept. 16–18.

31st Annual Broadcast Symposium, IEEE (R. A. O'Connor, CBS-TV Network, 51 W. 52nd St., New York, N. Y. 10019), The Washington Hotel, Washington, D. C., Sept. 16–18.

New York Computer Showcase Expo, The Interface Group (160 Speen St., Framingham, Mass. 01701), Pier 92 Passenger Terminal, New York, Sept. 17–19.

ISS '81—International Switching Symposium, IEEE (General Secretariat-ISS, Box 56, Station Ile des Soeurs, Verdun, P. Q. H3E 1J8, Canada), Hotel Bonaventure, Montreal, Sept. 21–25.

Semicon/East '81, Semiconductor Equipment and Materials Institute (625 Ellis St., Suite 212, Mountain View, Calif. 94043), Hynes Auditorium, Boston, Sept. 22–24.

International Electrical and Electronics Conference and Exposition, IEEE (IEEE Canada Office, 7061 Yonge St., Thornhill, Ont. L3T 2A6, Canada), Canadian National Exhibition, Toronto, Oct. 5–7.

Fall Conference of Use Inc., Sperry Univac users association (Box 461, Bladensburg, Md. 20710), Sheraton Centre, Toronto, Oct. 12–16.

Semicon/Southwest '81, Semiconductor Equipment and Materials Institute (625 Ellis St., Suite 212, Mountain View, Calif.), Market Hall, Dallas, Oct. 13–14.

27th Annual Vhf Conference, Western Michigan University (Glade Wilcox, Department of Electrical Engineering, WMU, Kalamazoo, Mich. 49008), Kohrman Hall, WMU, Oct. 17.

Midcon/81, IEEE (Electronic Conventions Inc., 999 N. Supelveda Blvd., El Segundo, Calif. 90245) Hyatt Regency O'Hare Hotel and O'Hare Exposition Center, Chicago, Nov. 10–12.

Eascon—Electronics and Aerospace Systems Conference, IEEE (Robert D. Briskman, Comsat General Corp., 950 L'Enfant Plaza S. W., Washington, D. C. 20024), Washington Hilton Hotel, Washington, D. C., Nov. 16–19.

Seminars

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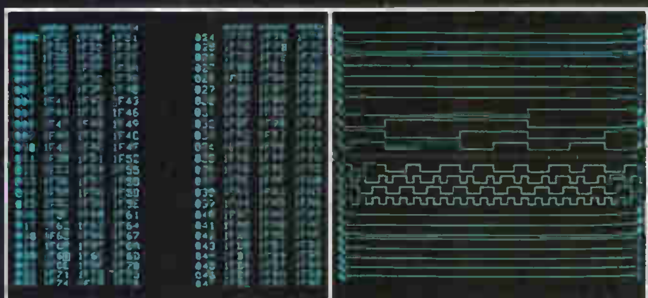

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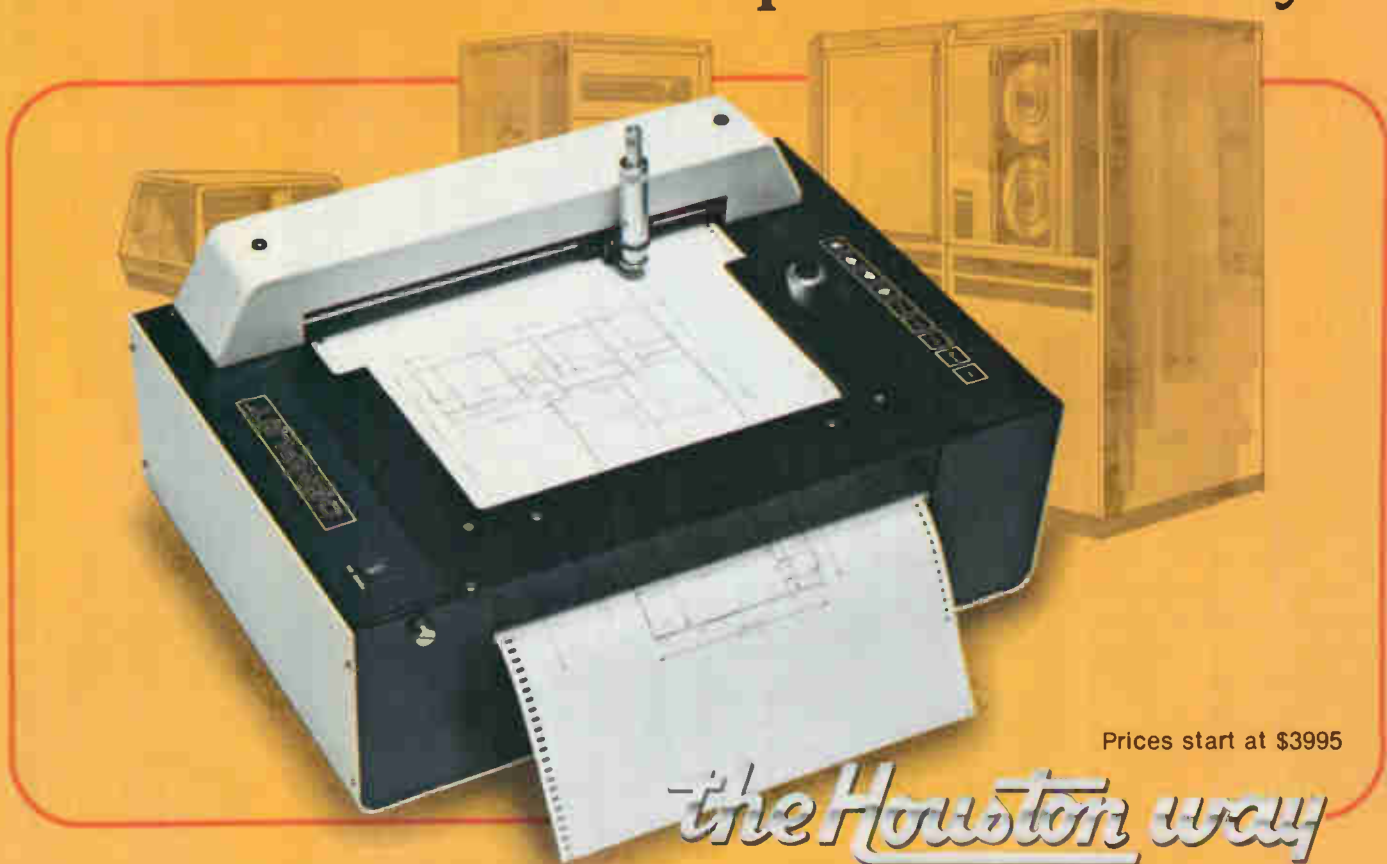

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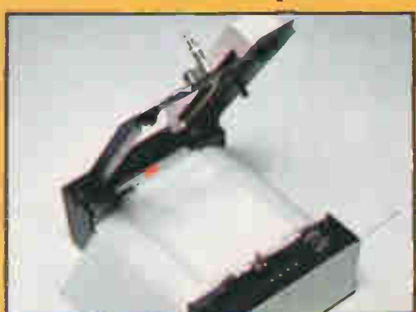

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FCC may ease restrictions on cable TV

Through two swift midsummer actions, the Federal Communications Commission may have telegraphed that it is getting ready to drop its long-standing prohibition against television broadcasters' ownership of cable-TV systems. At the end of July, the FCC approved the takeover of Teleprompter Corp., the nation's second-largest cable company, by Westinghouse Broadcasting Co. in a transaction involving more than $500 million. The purchaser, a subsidiary of Westinghouse Electric Corp., owns and operates six TV stations and 13 radio stations, as well as four cable-TV relay stations. Less than a week later, **the FCC followed with a 5-to-0 ruling that CBS Inc. will be permitted to acquire a cable-TV company,** provided it does not serve more than 0.5% of the nation's cable subscribers. In the Westinghouse-Teleprompter merger, the broadcaster will have one year to divest itself of cable or broadcast operations that serve the same areas. CBS says it wants to use cable to experiment with high-resolution TV broadcasting, as well as with transmission of two signals on a single channel to display text in addition to video.

CAT technology enters industrial testing market

Computerized axial tomography, which flourished in the mid-1970s as hospitals around the world fitted themselves out with scanner units for noninvasive internal medical examinations, could thrive again with the advent of CAT systems for industrial nondestructive testing. **At least two firms—Ridge Inc. of Tucker, Ga., and Scientific Measurement Systems Inc. (SMS) of Austin, Texas—have CAT inspection systems under development.** One such system is currently being used to look for faults in pieces of the steel and concrete skywalks that collapsed last month at a Kansas City hotel, killing more than 100 people. If CAT catches on in industry as it did in medicine, it will mean healthier markets for low-cost array processors; Analogic Inc., Wakefield, Mass., supplied those in the SMS system.

Low-cost decoder improves chances of Prestel in U.S.

Prestel, the videotex scheme backed by British Telecom and the major UK communications equipment makers, is counting on a small, two-year-old firm in Ithaca, N. Y., for added impetus in the U. S., where the interactive home and office information service will be launched later this year. The firm, Wolfdata Inc., will deliver this month a first batch of 50 videotex decoders to Prestel's U. S. agents, Logica Inc. **The hardware is to be priced at $650, plus $49 for an optional radio-frequency converter.** It allows subscribers to access Prestel's vast data bank by means of an ordinary 525-line television set and a modem. Zenith Radio Corp. has made at least one pass at a similar decoder for U. S. use, estimating it would cost about $1,500 [*Electronics*, July 3, 1980, p. 59]. Wolfdata president Thomas Lonergan says a second version of the decoder, with a built-in modem based on a custom chip, will follow early in 1982.

Development systems for gate arrays are on the way

It now looks as if LSI Logic Corp., a semicustom gate-array supplier recently set up in Santa Clara, Calif., will get to market first with a development system for gate arrays. The company expects to have its $500,000 to $1,500,000 LDS-I system ready this year. **It will handle logic checking, circuit simulation, macrocell placement, and path timing** and generate test programs for complementary-MOS, TTL, and emitter-coupled logic arrays. Software combines standard packages for data entry, interactive placement and routing, and simulation with some special algorithms developed by LSI Logic. The hardware consists of a host 32-bit superminicomputer like Digital Equipment Corp.'s VAX 11/780 or Prime Computer Inc.'s 750, plus a designer's display console. American Microsystems Inc., also of Santa Clara, figures to turn up fairly soon with a gate-array development system as well. The exploding market for semicustom logic points to a proliferation of new development systems.

Graphics controller priced below $11,000 has high resolution

Prices for high-resolution raster-scanning color-graphics controllers could skid early next year if Raster Technologies Inc. starts deliveries of its Model One in January as planned. The Troy, N. Y., company has priced its controller, which has software-selectable resolution of either 512 by 512 or 1,024 by 1,024 picture elements, at $10,800. This works out to a little more than half the price of the new bottom-of-the-line display system from Ramtek Corp., Santa Clara, Calif., which has a maximum resolution of 1,280 by 1,024 pixels [*Electronics*, July 28, p. 34]. **Raster Technologies' controller has an image memory, based on 64-K random-access memories, that totals 768-K bytes**—the highest yet for this kind of hardware, the company says. The controller, which can be fitted into existing systems, includes a 16-bit MC68000 central processing unit, a hardware vector generator to offload line-drawing tasks from the host computer, and a proprietary pixel processor to optimize the operations performed on image arrays. Both the Raster Technologies and Ramtek displays were introduced at the Siggraph/81 conference held in Dallas, Texas, earlier this month.

Storage Technology to market add-on virtual memory

A virtual storage system that processes megabyte data sets twice as fast as disks alone, 12 times as fast as multiple mass-storage subsystems, and 30 times as fast as tape will be put on the market in mid-1982 by Storage Technology Corp. Designed for large IBM computers running the MVS multiple virtual storage operating systems, the VSS virtual storage system will fit between the host computer and its mass-storage peripherals. **Its 0.7 million-instruction-per-second processor and cache memory relieve the host** of normal data-management duties to speed throughput. What is more, maintains the Louisville, Colo., company, the VSS packs disks almost to their full capacity (usually only about half is used) and compresses stored data by as much as 25%.

Prime readies entry into distributed processing

Look for a year-end announcement of a distributed data-processing system from Prime Computer Inc. The Natick, Mass., firm is **readying the system, code-named Rabbit, and an associated intelligent terminal, Lynx,** for availability in the first half of 1982. Rabbit, based on one of Prime's low-end 50 series minicomputers, will feature compatibility with IBM's Systems Network Architecture communications protocol.

Government prepares packet-switch norms for its data nets

The U. S. government wants comments from the data-processing industry by Nov. 3 on its proposed new interface standards and protocols for Federal packet-switched data-communications networks and their related computers. **The standards are based on the International Telecommunications Union's X.25 standard** and, the Government hopes, will save it money on both procurement and use of its data networks.


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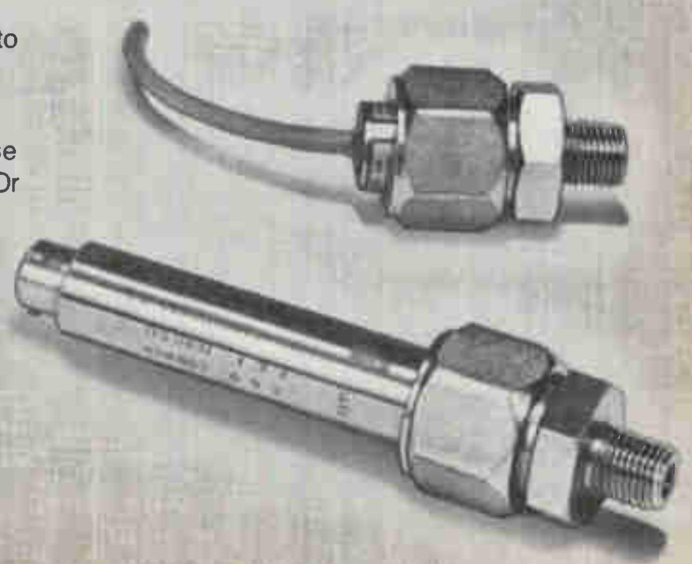

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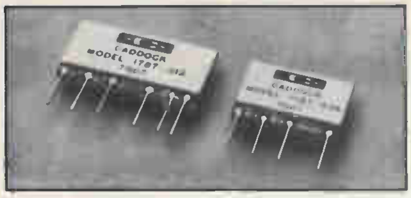


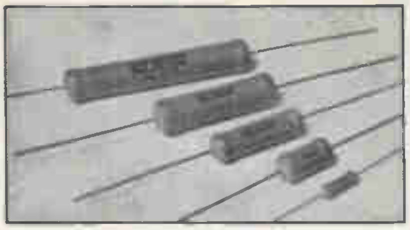
Caddock's Type 1787 Current Shunt Resistor Networks.

Absolute resistance tolerances of 0.25%, 0.1%, 0.05% and 0.02% make these 2-, 3- and 4-decade current shunt resistor networks the ideal replacement for expensive, bulky discrete resistors.

16 standard models are now available. The basic network design provides a series total resistance of 1000Ω, 100Ω, 10Ω and 1Ω. Other standard models provide commonly used variations of this basic design.

For Type 1787 data, circle Number 188.

Non-inductive precision resistors for power switching circuits.



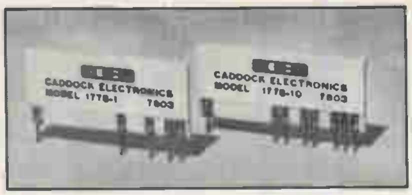
Caddock's Type MS Power Film Resistors.

Caddock's patented Non-Inductive Design in power ratings from 2 watts to 15 watts assures minimum voltage transients in all types of power switching circuits.

High stability Micronox* resistance films operate to +275°C and years-long load-life tests demonstrate extended-life stability better than 0.05% per 1000 hours.

For Type MS data, circle Number 189.

Off-the-shelf precision decade voltage dividers.



Caddock's Type 1776 Precision Decade Resistor Voltage Dividers.

When used as a 10 Megohm input voltage divider, the Type 1776 family can provide high accuracy voltage division in ratios of 10:1, 100:1 and 10,000:1.

Type 1776 Precision Decade Resistor Voltage Dividers are now available in 25 standard models with ratio TCs from 50 ppm/°C to 5 ppm/°C. Caddock's laser production techniques keep OEM quantity prices low, too.

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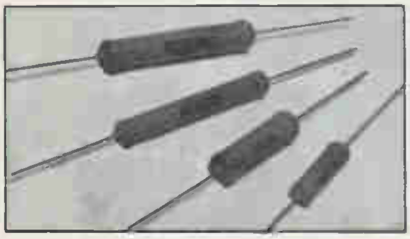
CADDOCK Resistor Technology solving problems across the board!

High stability resistors for very-high voltage control and measurement circuits.



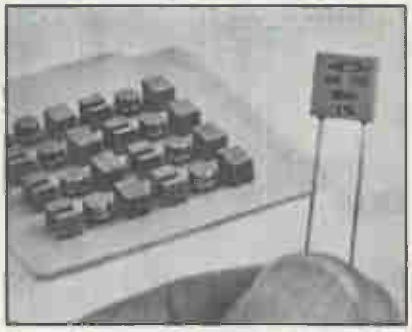
Caddock's Type MG High Voltage Resistors.

High voltage probes and control circuits make wide use of Type MG resistors for precision high voltage regulation and high voltage measurements.

Long-term stability — plus proven reliability — have also made these precision resistors first choice in communications satellite voltage control circuits.

For Type MG data, circle Number 191.

100 Megohms in a miniature package.



Caddock's Type MK Precision Film Resistors.

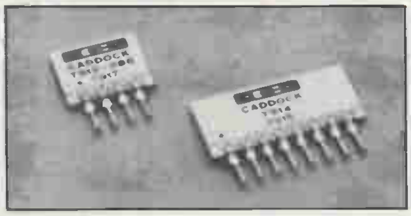
Precision values to 100 Megohms in a miniature CK 06 case make the Type MK ideal for low current designs.

These non-inductive resistors find wide application in high-impedance analog circuitry.

For Type MK data, circle Number 192.

NEW

Resistor pairs and quads with very low ratio TC.



Caddock's Type T912 and T914 Precision Resistor Networks.

Ratio tolerances to ±0.01%, ratio TCs of 2, 5 or 10 ppm/°C and ratio stability within ±0.01% at full load for 2000 hours provide exceptional stability in precision analog circuits.

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HIGH PERFORMANCE FILM RESISTORS

75-MHz a-d converter relies on 8-bit chip with 1-μm line widths

by Larry Waller, Los Angeles bureau

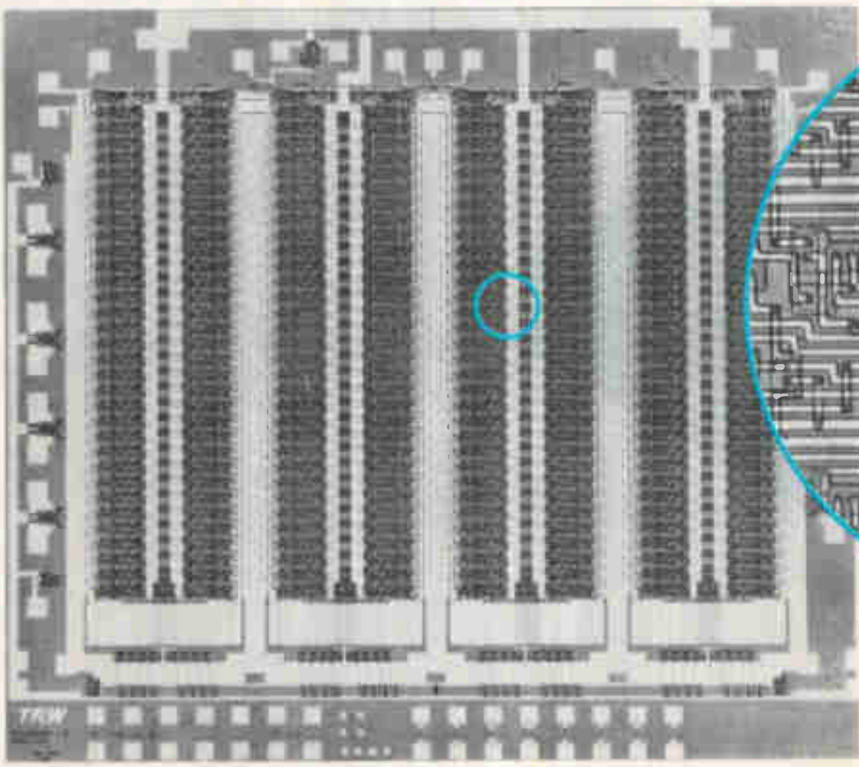
TRW's LSI Products division offers board product first, photolithographically made chip in the next few months

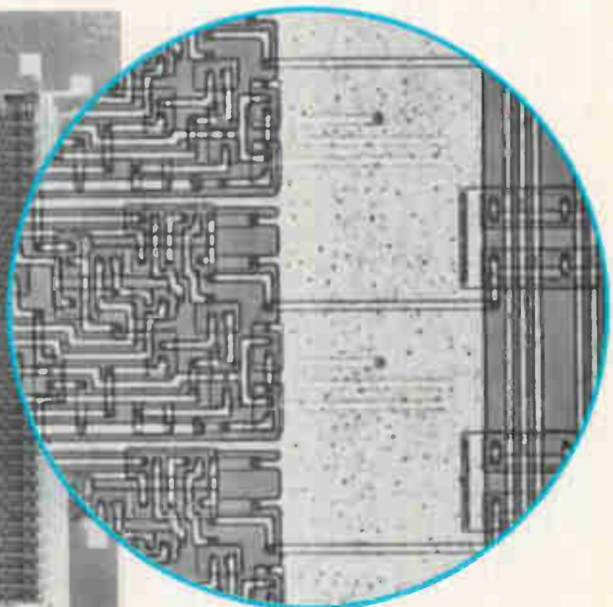
The first commercial device built with a 1-micrometer process is coming on the scene from TRW Inc.'s LSI Products division. It is a bipolar 8-bit "flash" analog-to-digital converter chip that runs at a lightning-fast 75-megahertz conversion speed. Initially, the La Jolla, Calif., division is offering it on an analog-to-digital board for evaluation. The chip itself will be offered in a few months.

The densities possible with the 1-μm process lead to eye-opening improvements over TRW's comparable 8-bit TTL converter fabricated by 2-μm techniques, claims Willard Bucklen, manager of applications engineering for the division. Besides a boost in speed from 30 MHz to 75 MHz, the new chip (model TDC1025J) has higher input impedance, lower (less than one third) internal capacitance and power requirements, and a cut in interconnection parasitics due to tighter geometry. Also, the approximately 200-by-160-mil size, compared with the 260-mil-on-a-side 2-μm chip, cuts the total area by half.

Bucklen zeroes in on a key characteristic of the 1-μm part that supports its accuracy of $\pm 1/2$ least significant bit: tight control over base resistance, which requires uniform doping and geometry. This permits precise matching of the base-to-emitter voltages of on-chip transistors. Such control is critical in a flash-type converter because 255 comparators, consisting of two emitter-coupled transistors each, cumulatively compare the incoming analog signal with a reference voltage. Differences among the base-to-emitter voltages of the 510 transistors would lead to variations in the comparators' thresholds that could degrade linearity.

"This is easy to do for a single





Fine details. One-micrometer-wide lines used in the TDC1025 8-bit a-d converter show up clearly magnified 500 times in photo at right. Matching of base-to-emitter voltages yields a linearity error of 0.2%.

TRW sets signal processing pace

With its new 75-megahertz a-d converter, TRW's LSI Products division once again demonstrates its strategy of offering the speediest of components for digital signal-processing equipment. It staked out this market early on, after parent TRW Inc. spun the division out of the TRW Defense and Space operation in 1976, with a pioneering bipolar 16-by-16-bit multiplier chip [*Electronics*, Oct. 27, 1977, p. 78]. With 160-nanosecond speeds that handled 6 million operations per second, the chip had some 18,000 transistors, perhaps the highest density at that time.

From a bootstrap start inside the military-oriented parent, the division continued to expand its line with arithmetic and converter components. Besides its military customers, TRW sells parts for such industrial gear as special-effects generators for broadcast television, ultrasonic medical body scanners, and speech-recognition equipment.

TRW does not break out separate results for its divisions, but the gross sales of LSI Products are said to be more than $25 million yearly, with profit margins reflecting a virtual monopoly in several product lines. General manager Ralph Miller predicts a five-fold increase by 1985 for his division, which recently moved to La Jolla, Calif., to gain room for growth. **-L. W.**

differential pair," Bucklen notes, "but the trick is to do it on all 510 over the operating range." In the TRW converter the voltages match within ±2 millivolts leading to a linearity error of only 0.2%. The sampling time aperture is a mere 20 picoseconds. Transient response, or the time required for recovery from a full-scale input step, is 10 nanoseconds, and power dissipation is 2 watts. This is about as much power as is dissipated by the older 8-bit, 2-μm part made with TTL technology. Emitter-coupled-logic signals control conversion and provide an 8-bit parallel output.

Although shrinking down to 1 μm entails no radically different approach, the difficulty is maintaining much closer tolerances, which demands more precise equipment. Achieving enough production to support a commercial line challenges manufacturing expertise to the fullest, the company says.

Accurate alignment. TRW chose a Canon 141 photolithographic system from among the competing systems coming on the market. It has projection alignment steps accurate to 0.25 micrometer and is stepped nine times to produce fields of four chips each, 36 in all. (TRW stuck with photolithography, rather than going to an even more accurate electron-beam exposure system, because the beam equipment's throughput at present is too low.)

The firm also continues with its triple-diffusion bipolar process, which it has used since TTL was developed by TRW engineers almost two decades ago, because of its simplicity. Among other things, it needs only 5 mask steps compared with 9 or 10 for an epitaxial approach.

The TRW division chose to sell the converter in board form first because such high-speed parts require special design care in implementation if their performance is not to be degraded. This chip-on-a-board route was taken with earlier products, too. To encourage customers, the board is priced at $1,360, which TRW says is what the board costs to make. To do it all themselves as a one-shot evaluation setup would set customers back some $5,000 or so, Bucklen asserts. **-Larry Waller**

Packaging

Clad lead frames take out more heat

Faced with the increasing problem of carrying away heat as integrated circuits become denser, a growing number of manufacturers have been switching to copper-alloy lead frames for plastic IC packages in place of the standard nickel-iron alloy. But rather than moving to a copper alloy, Texas Instruments Inc. is backing a new clad-metal combination of copper and stainless steel, first being used for its programmable read-only memories packaged in plastic.

Developed by TI's Metallurgical Materials division, Attleboro, Mass., the copper-clad stainless-steel material offers thermal conductivity almost six times that of alloy 42, the iron alloy with 42% nickel of which lead frames are usually made. TI also says that the metal has greater mechanical strength and ductility and can endure twice as many bends before fracture.

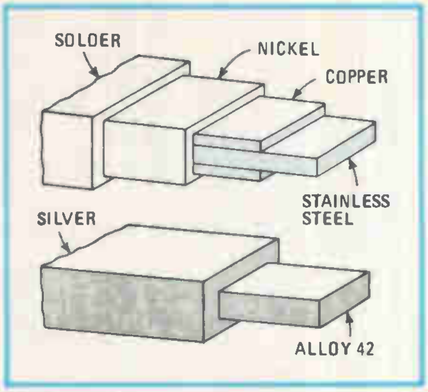
Better reliability. The company believes the new lead frame and its improved thermal characteristics will enable a number of its customers for ceramic-packaged ICs to switch to less expensive plastic housings. Reliability will increase because operating temperatures of the circuit will be lower, the firm says.

Tests on 16- and 20-pin plastic PROM parts using the new material show junction-to-ambient-air ratings (Θ_{JA}) of 83°C per watt and 66°C/W, respectively. That compares to 104°C/W and 85°C/W for 16- and 20-pin packages using alloy 42.

TI notes that tests were conducted on parts with only a minimum contact area edge-connected, rather than soldered, to fixtures. This sets up a worst-case condition for heat dissipation within the package.

However, it was the clad metal's thermal expansion properties that sold the firm's PROM operation on its use, says Joe Brennan, memory and microprocessor engineering manager in the Digital Circuits division, Houston. Moving to copper-alloy lead frames—which also feature high thermal conductivity ratings—would have required new plastic molds. The thermal expansion coefficients of copper alloys run around three times that of alloy 42, Brennan notes.

The mismatch of expansion coefficients between metal lead frames and the existing plastic mold could



New frame. TI will use lead frames made of copper clad-stainless steel in its plastic PROMs. A layer of nickel is added, as was silver, to improve solder adhesion.

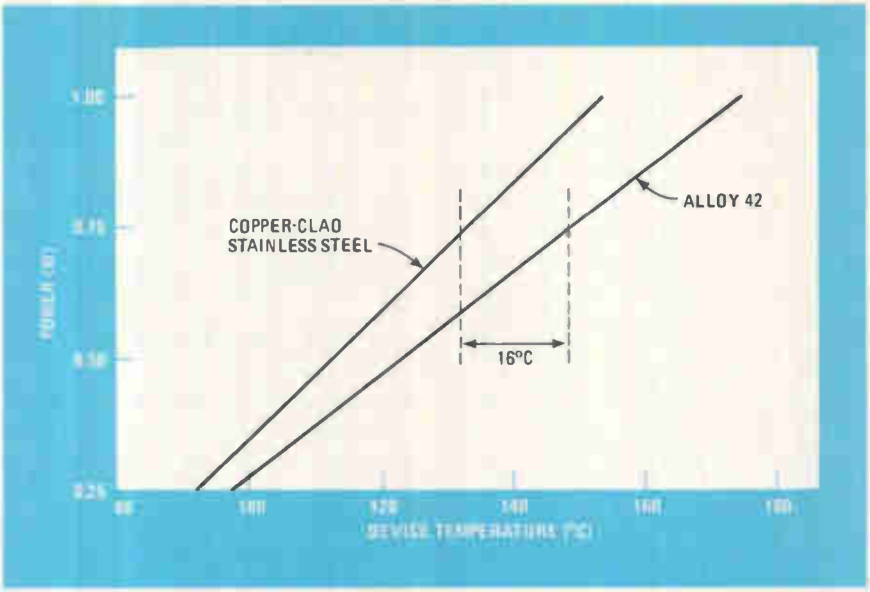
damage the package and the bonding to the silicon chip. The clad material, high-purity copper on a stainless steel core, on the other hand, has an expansion coefficient only twice that of alloy 42.

This closer matching allows TI to use its existing manufacturing techniques and production tools. Brennan also adds that conversion to the clad metal would not change the price of the PROMs.

Currently, TI is offering samples of PROMs in 16- and 20-pin plastic packages with the new lead frames. Eighteen-pin packages will also be available in samples this month; 24-pin parts, in October. By the end of the year, all of TI's plastic PROMs will feature the clad-metal lead frames. The memory and microprocessor operation plans to convert other plastic products as well.

Heavy pressure. The material is made by a bonding process involving pressure from heavy rolling mills and subsequent heat treatment to promote diffusion between the copper and stainless steel. The result is a metallurgical bond in which the crystal lattices at the interface are interlocked at the atomic level. A nickel layer is added to the clad metal to improve solderability.

The TI move comes as other IC makers continue lead-frame conversion programs. Early last year, Motorola Inc. began replacing alloy 42 with a copper alloy, Olin 194, in members of its standard complementary-MOS logic family.



Cooler. Tests indicate that the new lead frame allows a 16-pin 0.75-watt device to operate 16°C cooler at 70°C ambient air when compared to a 16-pin device in an alloy 42 lead frame.

Motorola says it will also soon use Olin 194, manufactured by Olin Brass Group of the Olin Corp., East Alton, Ill., in two microprocessor products, including the 8-bit MC6801. National Semiconductor Corp., for another, has been moving to copper-alloy lead frames on many of its plastic IC products for the past four years. **-J. Robert Lineback**

Data communications

Bell algorithm speeds decryption of public-key coding schemes

There is a great advantage in using what is called a public-key scheme when it comes to encrypting data to ensure its security. Someone wishing to send data need only be concerned with the code word for encrypting it; the decryption code, on the other hand, would be known only by the person receiving the data and could be closely guarded. Organizations cooperating in the public-key scheme would publish the encryption code for their data in a public directory where it could be located by anyone wishing to send them data.

A private-key scheme, on the other hand, such as the 56-bit code word developed for the Federal government by the National Bureau of Standards, [*Electronics*, Aug. 16, 1979, p. 81], cannot be used so readily. The decryption code word for the data being transmitted must be sent along to the receiver—unless he already has it—and the code runs the risk of being stolen.

Heretofore, however, public-key systems—and these are more in the talking stage than actually being implemented—have also had a great disadvantage. Their implementation in hardware has required so much number crunching as to restrict them to much slower, kilobit-per-second decryption rates than the NBS private-key approach. This disadvantage may no longer apply as a result of the work of Paul S. Henry, head of the optic systems research department of the Bell Laboratories facility in Holmdel, N. J.

Special cipher. What Henry has done is to come up with a fast algorithm for executing what is called the knapsack cipher. This is a popular public-key system invented by

R. C. Merkle and Martin E. Hellman of Stanford University. According to Henry, it is possible to achieve a 10 megabit-per-second data rate with only TTL.

This speed is more than adequate to provide security for a wide range of voice, data, and narrowband video traffic, he says. A prototype very large-scale integrated-circuit system using Bell's digital signal processor chip developed in house has already implemented the algorithm, although memory limitations keep it from being fully secure.

Henry's algorithm is based on number theory and its design can best be appreciated by experts. The key to its speedy operation is that the steps in the decryption process, which requires data accumulation, division with respect to a modulus, and successive subtractions, are reduced to quick table-lookups—*à la* the private-key scheme—and it all may be pipelined.

Thus, most of the processing can be performed on bits in parallel. The speed limitation is either the memory access time or the accumulator add time, whichever is greater. Either of these can hold to about 50 nanoseconds with Schottky TTL.

Integration. It is quite feasible to implement the algorithm in standard VLSI. In one design, which Henry says provides "reasonable security," a 41-K memory is needed for the look-up table, along with 15 K for handling the knapsack vector. This data vector, generated by the party who wishes to receive encrypted data, is used for the basic step of the decryption process. Some simple arithmetic logic is also needed to perform the accumulation, long division, and subtraction.

Henry cautions that further investigation is needed. The best hardware layout for implementing his algorithm is not set, and relationships between the algorithm's security and its design also need study.

For now, Bell has published a technical paper about the algorithm in last month's issue of the Bell System Technical Journal. It is interested in knapsack data encryption for digital voice circuitry in future mobile radio services it may offer. Also, the data-communications services it may provide could also require encryption of the public-key variety. **-Harvey J. Hindin**

Computer-aided design

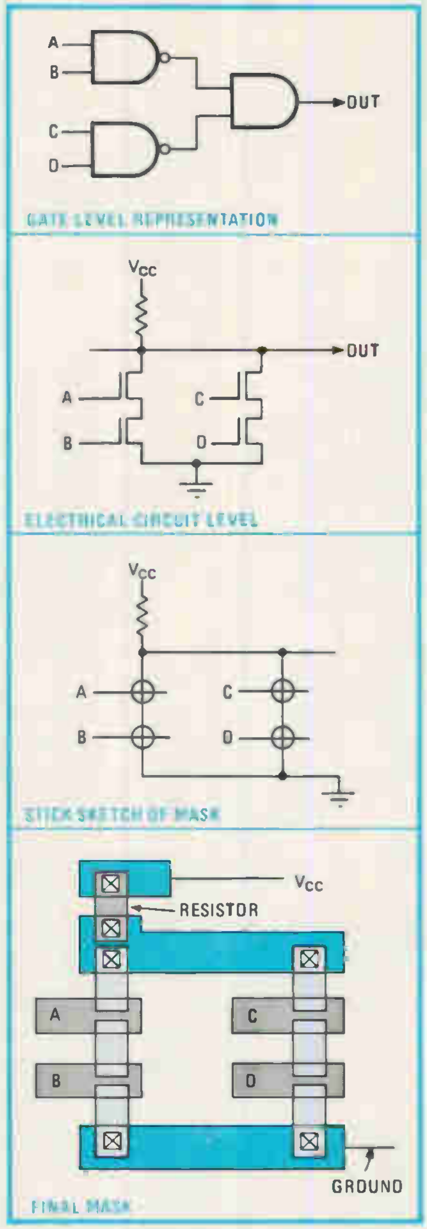
Lisp system could speed mask making

People are still needed in computer-aided design systems to create integrated-circuit masks. However, this procedure would be much faster, especially for very large-scale ICs, if the human factor could be minimized still further, and Symbolics Inc. is on the way to doing this with its special-purpose minicomputer and a software package of CAD tools.

The package of CAD tools—Symbolics is toying with calling it the VLSI Designers Toolbox—will speed the process of converting a transistor-level circuit diagram to photolithographic masks by eliminating a tedious hand-drawing step that was previously needed in design. The minicomputer, now on the market (see p. 159), can execute the symbolically oriented Lisp language, which permits easy programming and fast running of the CAD tools.

Four steps to layout. Even the more sophisticated semiconductor manufacturers go through a four-step process in a CAD-supported design project. The first automated step converts a gate-level human-drawn schematic into a transistor-level circuit diagram. The second step requires a person to draw a mask layout with the assistance of graphics-display software. In step three, that layout is converted by the computer back into an electrical circuit. Finally, the two circuits are compared by computer to see if the mask set will produce the same electrical circuit as the schematic.

Like others, Symbolics will use a CAD system to convert the designer's schematic into a transistor-level electrical circuit. However, it plans to speed up the second design step by allowing the mask layout to be quickly sketched freehand. The computer would then take over and convert the sketch into a mask set according to the design rules.



Mask making. CAD systems are available to transform a designer's gate-level schematic into an electrical circuit. Symbolics wants to add automation to the third step. From the circuit, the designer draws a simple stick-sketch that is automatically transformed into a final mask layout.

Sketching the mask layout is reminiscent of the Sticks approach pioneered by John Williams at the Massachusetts Institute of Technology, Cambridge, and subsequently picked

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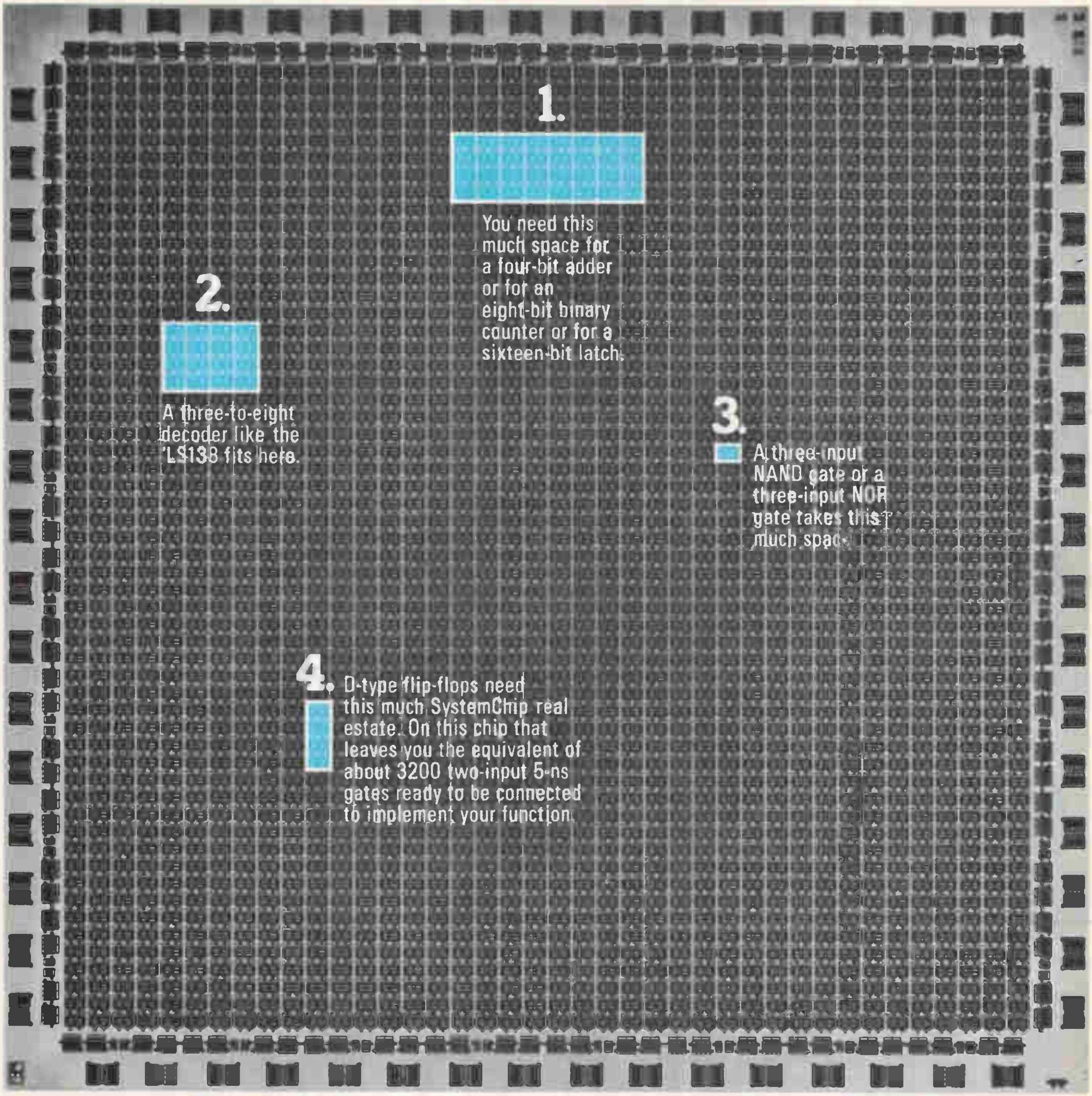

Unretouched photo of the new G82240 gate array before metalization.

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up by Hewlett-Packard [*Electronics*, April 10, 1980, p. 40]. Its name, Sticks, came from the method's similarity to a stick-figure drawing.

Such single sticklike lines suffice for the freehand mask layout. The next automated step takes this layout to form a real mask set. In other words, the sticks are converted into whatever line widths—5 micrometers with 2.5-μm spacing, for example—the design rules specify.

Chris Terman, the toolbox designer at Symbolics in Cambridge, Mass., points out that the approach only requires human input for tasks too difficult or time-consuming for a computer. He also maintains that the Lisp language, which easily links different representatives of the same concept, and Symbolics' minicomputer that directly executes the language, are ideal for the job. "I have transferred some of the CAD tools I developed in C under Unix to Symbolics' machine, and the fact of the matter is that they are easier to program and run faster in Lisp," Terman says.

Four levels. As illustrated in the figure, the first step in the design process is to draw on the cathode-ray tube the gate-level schematic of the desired circuit. The schematic may be input as generic functions (like AND, OR and NOT gates) or as standard part numbers (like 74181s). From this representation, the computer generates an electrical circuit diagram that reduces the number of parts to a minimum (to four field-effect transistors in the illustration). At this level of representation, the program runs through a complete circuit analysis and simulation and checks the circuit against the electrical-design rules.

Terman's hope is eventually to automate the manual step required to sketch the mask layout from the electrical circuit. A tremendous amount of research is being done toward this goal [*Electronics*, July 31, 1980, p. 73]. **-R. Colin Johnson**

Test equipment

Air Force contract to Sperry division will set guidelines for ATE in the 1990s

With a $54.8 million award to Sperry division of Sperry Corp., the Air Force appears to be clarifying its guidelines for future automatic test and avionics equipment buys. Sperry's systems management unit in Great Neck, N. Y., won the contract for the Modular Automatic Test Equipment (MATE) program after a three-year competition with the Westinghouse Electric Corp. [*Electronics*, Dec. 4, 1980, p. 62].

With its timing, the MATE award seems almost a riposte to the General Accounting Office's early-1981 report on ineffectual weapons system design [*Electronics*, Feb. 10, p. 59]. Although all three armed services had reliability and software problems, the Air Force's F-15 automatic avionics test equipment was specifically cited as undependable.

Maj. Ralph Freeman is branch chief of the MATE full-scale development program at Wright-Patterson Air Force Base in Ohio. He notes that while the program's name might lead firms to believe otherwise, "MATE is not standard hardware—it's a hardware standard. It is a systematic Air Force approach to satisfying our ATE needs."

As part of that systematic approach, the Air Force will look more closely at procuring off-the-shelf instrumentation from commercial vendors, thus cutting them in for a slice of a pie that has been approaching $1 billion yearly.

Thus, although Sperry will develop some hardware under the contract, a maintenance facility for the A-10 aircraft inertial navigation system, the conceptual portion of the MATE effort is expected to be more important by far, shaping avionics systems design for the 1990s.

Program manager Lt. Col. Richard H. Danhof describes MATE as a set of five guidelines that between them will cover:

- Air Force and contractor management procedures for the procurement of ATE.
- ATE hardware and software development criteria.
- A test-program set describing how avionics test software ought to be written.
- A crew guide that tells Air Force personnel how they should use ATE in the field.
- A guide showing avionics equipment contractors how to make their systems testable with Air Force ATE.

Sperry's contract will run through 1984, with development of the guidelines coming first and development of the A-10 avionics repair facility following as a proof-of-principle exercise. The company will subcontract some 40% of the award, including development of MATE architecture and acquisition approaches for the military.

By the mid-1980s, MATE guidelines should be impinging upon almost all Air Force ATE and avionics procurements. One of the first effects of MATE will be reflected in a 1982 request for proposals for the depot automatic test system for avionics, or Datsa. Sperry, excluded from bidding on Datsa, will supply technical assistance to the Air Force during that program—one of the first tests of MATE's principles.

Details about the program are still being resolved, but an Air Force-Sperry team plans to confer with industry representatives at Wright-Patterson this Sept. 21–23 with the goal of giving potential contractors an idea of MATE's impact on their business and engineering practices. **-James B. Brinton**

Communications

Budget threatens U. S. Satcom lead

Unless the National Aeronautics and Space Administration continues funding the development of high-

SCIENCE/SCOPE

A 100-kilovolt hydrogen ion source will play a vital role in fusion energy studies in the Tokamak Test Reactor at Princeton University. The source will create a 65-ampere beam of deuterium ions that subsequently will be neutralized by charge exchange to produce a beam of fast neutral particles. This neutral beam can cross the intense magnetic field lines that contain the plasma in the reactor. It will fuel and heat the plasma to the point where self-sustained fusion can take place. The reactor, when completed, will use 12 such ion sources. Hughes built the device under contract to the U.S. Department of Energy.

Pilots soon may get navigational information from a TV display instead of paper maps. Hughes, under a U.S. Air Force contract, is developing a system that will use a computer to electronically generate and display realistic pictures of terrain and man-made features. The new map will be coupled to an aircraft's navigation system to help the pilot fly at high speeds and low altitudes despite bad weather, darkness, and radar jamming. Ultimately, production models of the map could be tailored to meet different mission requirements. One mission, for example, may require roads and highways as navigational checkpoints, whereas another would require navigation with reference to terrain features. The prototype system will store 250,000 square miles and use more than 1,500 bits of data to encode each square mile. It is scheduled to be delivered in August 1982.

Certain military laser rangefinders should soon be improved now that researchers at Hughes have pinpointed long-suspected impurities in laser rods. Using a new dye laser technique in their spectroscopic studies of Nd:YAG (neodymium-doped yttrium aluminum garnet) laser rods, scientists uncovered a subtle crystal defect that cuts the laser's efficiency and brightness. They believe it will be possible to develop a process to increase the quantum efficiency of commercial Nd:YAG lasers from about 64 percent to the theoretical maximum of 91 percent.

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A new handbook on traveling-wave tubes and traveling-wave tube amplifiers is now available from Hughes. The 56-page booklet is designed as a complete reference guide. It discusses the history, operation, design, performance, and application of TWT's and TWTA's. It also includes a full glossary of terms, diagrams, and specification charts on all Hughes TWT's and TWTA's. For copies, write to: Hughes Electron Dynamics Division, 3100 W. Lomita Blvd., Torrance, CA 90509.

capacity communications satellites with an uplink of 30 gigahertz and a 20-GHz downlink, U. S. companies will lose this next-generation market to competitors in Europe and Japan. That is the argument being advanced in Congress by NASA and contractors like RCA Corp. and Western Union Corp. to counter an Office of Management and Budget proposal that the growing satellite communications industry, not Government, should be funding research and development on K_a systems, as they are termed.

The turning point of Government support for the K_a-band program is expected from the OMB in the fiscal 1983 budget, due in Congress next January. NASA is expected to ask for funds for the effort in its budget draft to be ready for the OMB by mid-September. K_a-band satellites, with message capacities 50 to 100 times greater than the 14-/12-GHz (K_u-band) and 6-/4-GHz (C-band) domestic satellites now in use, are expected to dominate the market for 30 to 40 years after their introduction in the 1990s.

Dispute. While OMB officials looking to reduce NASA outlays contend that industry is capable of funding K_a-band R&D, J. E. Keigler, satellite communications manager for the RCA Astroelectronics division, argues that "NASA must conduct the flight demonstration because not even the largest carrier can underwrite the combination of high cost and high risk."

Testifying with Keigler last month before the House Science and Technology subcommittee on space science and applications was his Western Union counterpart, Donald B. Nowakoski, who noted that financial demands on carriers to meet near-term needs prevent their undertaking a K_a-band satellite flight test on their own. Industry officials, who also noted that a consortium effort is precluded by U. S. antitrust and patent conflicts, emphasized that similar K_a-band R&D programs in Europe and Japan are funded by those governments.

After prodding by the National Academy of Engineering, NASA restarted its domestic satellite R&D program in 1977 [*Electronics*, April 14, 1977, p. 57]. The revived version, however, did not concentrate on satellites using the 30-GHz uplink and 20-GHz downlink until more than a year later. As a result, NASA states that it does not expect to reach the flight test stage before 1987 or 1988. That would lead to an operational system only by the early 1990s, putting Europe and Japan three to four years ahead of the U. S.

Nevertheless, although Samuel W. Keller, the deputy associate administrator of NASA's Office of Space and Terrestrial Applications, believes that U. S. satellite buys from Japan are "certainly feasible," he is quick to add that any 30-/20-GHz system developed by the U. S. would have "four to five times" the usable bandwidth of a Japanese system because of American development of techniques for frequency reuse and spectrum conservation and the employment of spot beams. Keller estimates that NASA has thus far invested about $40 million in the program with more than a dozen contractors. **-Ray Connolly**

Education

RPI receives gifts for VLSI center

Rensselaer Polytechnic Institute of Troy, N. Y., is building an integrated-electronics center, with the help of two major gifts, that will focus on very large-scale integrated circuits. Dubbed the Center for Integrated Electronics, it will be located in a 60,000-square-foot laboratory building situated in nearby Watervliet, N. Y., and will focus its activities on an EL-2 electron-beam lithography system that is complete with computers and other peripheral gear.

The EL-2, donated by IBM Corp., has a line width capability of 1 micrometer and submicrometer capabilities for select structures such as emitter or contact devices. It represents one quarter of RPI's $20 million equipment goal. Another $10 million is being sought for program support, which includes teachers'

RPI president is power behind projects

The guiding force behind the Center for Integrated Electronics is university president George M. Low. An alumnus of Rensselaer Polytechnic Institute, Troy, N. Y., Low earned a master's degree in aeronautical engineering in 1950 before going on to the National Aeronautics and Space Administration's manned space-flight program and eventually serving as the deputy and acting administrator of NASA. After coming back to RPI in 1976, Low initiated several projects, such as the center and a technology park.

Recently, RPI trustees decided to commit $3 million toward development of the technology park, which is intended to be an East Coast version of California's Silicon Valley. Called the Rensselaer Technology Center, the park will be built on 1,200 acres of RPI-owned land on the eastern shore of the Hudson River between Troy and Albany, N. Y. Construction is to begin this September, and occupancy negotiations with companies are in progress.

When Low arrived at RPI, he hiked the research funds available to graduate students, while increasing their number, and maintained the number of undergraduates. In the 1980–81 school year, 777 graduate engineering students were enrolled full time, making RPI the ninth largest engineering school in terms of graduate students, "down from in the 30s in 1974–75," says George Ansell, dean of the engineering school. Last year, 2,794 undergraduate students enrolled, making it the 28th largest undergraduate engineering school—"about the same as MIT," Ansell adds.

To help solve industrial problems, Low has promoted a center for manufacturing productivity and technology transfer that was initially funded by Boeing, General Electric, and General Motors. He has also emphasized interactive graphics and computing, through acquiring an IBM 3033 mainframe and other computer facilities. **-A. M.**

salaries, laboratory construction, and graduate fellowships. The laboratory building was donated by Norton Co.

Based on a broad, multidisciplinary approach, the center is planned to bring students and faculty from electrical and materials engineering, physics, chemistry, and computer science together. "It will differ from other such VLSI centers in including undergraduates in the program, not in a token, but in a serious way," says Andrew J. Steckl, director of the new center.

About 100 graduate students and 150 undergraduate students are slated to enroll each year in the research and instructional programs, respectively. Steckl adds that "the center's approach is tailored so that students will not stop at BS degrees, but go on to grad work," in part by involving undergraduates in research projects. The facilities should be ready by January 1982 for a total of 30 students and faculty members who have been trained on the EL-2.

RPI hopes to reach the $30 million funding goal by 1986 and is putting up $1.1 million of its own money. The fund-raising campaign is aimed primarily at 300 or so users and producers of ICs including General Electric, DuPont, Kodak, Prime, Digital Equipment Corp., and Hewlett-Packard. Also by 1986, RPI anticipates having 25 teachers and 15 research assistants at the center, as well as 250 students.

"In 1977, RPI started active research in integrated circuits, in addition to its regular semiconductor program," Steckl says. By 1979, RPI had an IC fabrication laboratory and had begun research in the field of electron-beam lithography. After starting the research, the university decided to expand its IC program further, says Kenneth C. Blaisdell, director of corporate programs. He attributes the strong start of the new center and much of the university's success in other ventures to RPI president George M. Low (see p. 44).

Low has formulated the Rensselaer 2000 plan, which is a 20-year strategy that should make RPI "a major science and engineering university of international renown" and "significantly [increase] graduate education and research."

These goals depend a great deal on industry support in the form of both cash and equipment. Edgar A. Sack, senior vice president for General Instrument Corp.'s Microelectronics division in Hicksville, N. Y., says, "We're delighted to see an important New York State institution such as RPI getting support and developing increasing relationships with other New York State companies." Sack is interested in promoting closer university-industry ties, since projects like RPI's new center "benefit not only the university, but us. We get grads who are better trained." **-Andrew McCann**

News briefs

Linear IC managers quit National

Four prominent members of National Semiconductor Corp.'s linear IC program are leaving the Santa Clara, Calif., company to start up their own linear IC venture. Among the founders is Robert Dobkin, formerly National's director of advanced linear circuit development, who was responsible for the development of the widely used three-terminal voltage regulators. Robert Widlar, who designed many of National's early successes and has since been an independent contractor for them, will hold a position on the engineering staff of the not-yet-named spinoff.

The other three founders are former National vice president Robert Swanson, former product line manager Brian Hollins, and former marketing director Brent Welling. Swanson, who will be president of the new firm, is to be replaced by National's group director of special products, Arthur Stebenow. Replacements for the other three will be named soon.

Burroughs wants to buy Memorex with future projects in mind

Burroughs Corp. of Detroit wants to acquire the financially troubled Memorex Corp., Santa Clara, Calif., for $105 million. Memorex, the magnetic-tape and disk storage equipment maker, has recorded losses of $29 million on revenues of $768.7 million in 1980, and first-half losses this year totaled $31.5 million. Although Burroughs' revenues rose slightly to $2.9 billion last year, 1980 earnings plunged to $82 million from $306 million in 1979. It hopes that combining its own and Memorex' research and development efforts will result in economies for both firms and might lead to new high-density storage products by 1983.

Japanese open their first U. S. computer store

Toshiba America Inc. has opened the first computer store in the U. S. operated by a foreign competitor. The Information Processing Center in Costa Mesa, Calif., will highlight desktop computers and include the first made-in-Japan word processors introduced to the American market. A newly created division, Information Processing Systems in Tustin, Calif., will oversee Toshiba's efforts to sell small-business computer systems in the $3,000 to $8,000 range. Toshiba's three new systems in this range are 8085-based with 64-K bytes of memory and are targeted at businesses with 10 to 30 employees. The Costa Mesa store and one in Westwood, Calif., to open in September will have walk-in servicing. They will also sell other business equipment and telephone systems made by Toshiba, part of its overall thrust into the American market.

Alternative to Exxon current synthesizer dropped

Reliance Electric Co., Cleveland, has dropped work on the energy-efficient motor drive it was developing as a follow-on to the alternating-current synthesizer proposed by its corporate parent, Exxon Corp., but dropped in the spring as impractical [*Electronics*, April 7, p. 46]. Reliance refuses to elaborate on the problems it encountered, except to say that an unanticipated need for additional components reduced reliability and inflated manufacturing costs unacceptably.

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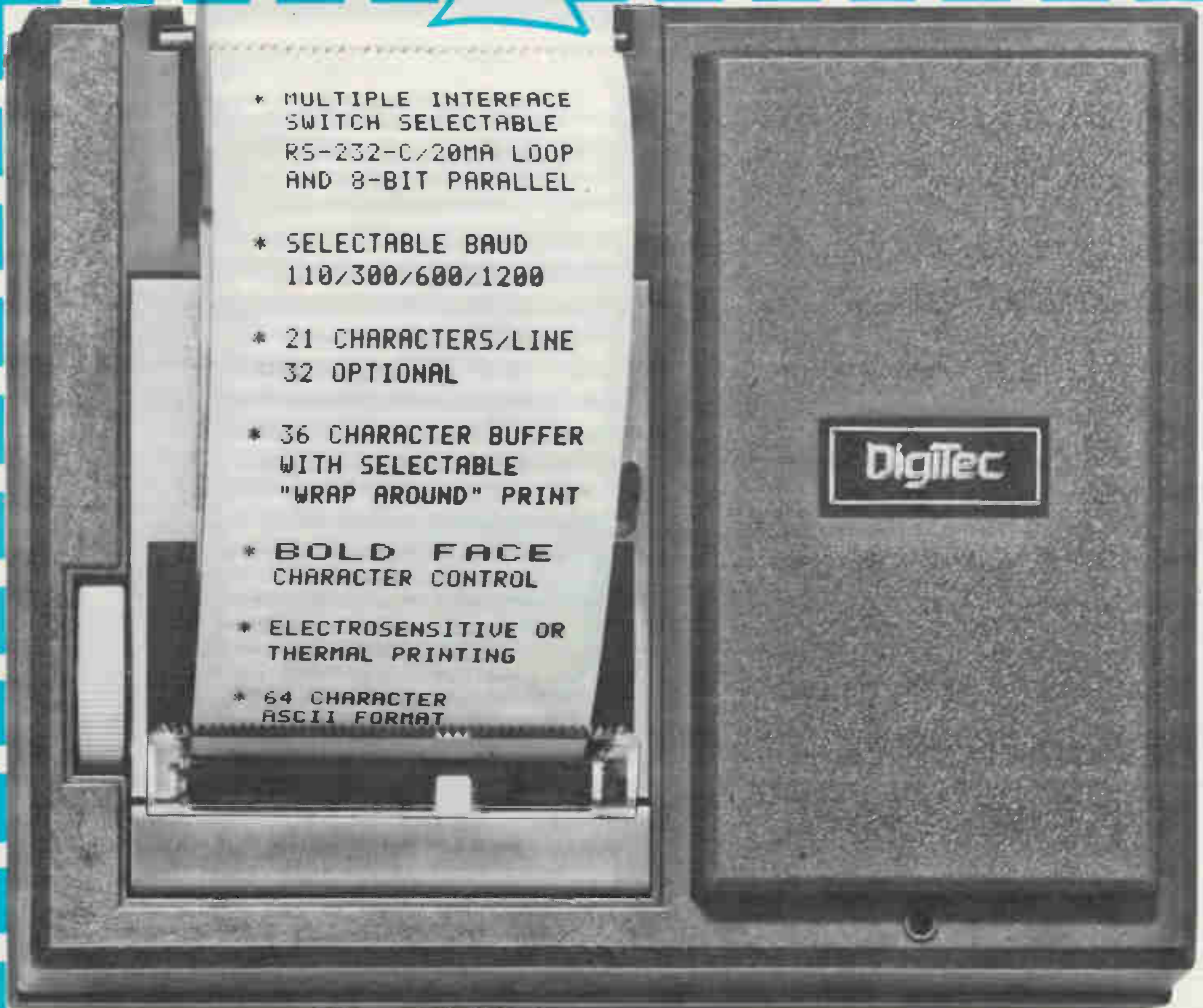

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Demonstration only circle #174

Washington newsletter

Japanese VLSI considered for U. S. weapons . . .

Use of Japanese electronic technology—particularly very large-scale integrated circuits—in U. S. weapons systems is **being explored by the Defense Department and the Japanese Defense Agency.** The possibility of transferring Japanese technology to U. S. producers, first raised during the waning days of the Carter Administration, is receiving serious scrutiny from Under Secretary of Defense Richard Delauer who, being responsible for research and engineering, discussed it here last month with JDA director Joji Omura.

. . . but possible barrier seen in Tokyo

While the JDA is reportedly favorable to the idea as means of countering U. S. criticism of Japan's refusal to increase military spending, Pentagon sources say an agreement may fail if it encounters opposition from Japanese semiconductor manufacturers, who developed the technologies, and from their government overseer, the Ministry of International Trade and Industry. **But the legality of such an agreement could be rationalized under a 1966 understanding** between the two countries on joint weapons research and development. U. S. interest reportedly focuses on Japanese VLSI circuits and microprocessors for antisubmarine warfare detection systems and for missile guidance, as well as air defense, although no specific system applications have been discussed yet.

FAA sees Congress receptive to automated air traffic control

Federal Aviation Administration leaders believe the next congressional session will be more sympathetic to its AERA program for automating en route air-traffic control [*Electronics*, Dec. 18, 1980, p. 48]. The reason: the strike of the air-traffic controllers' union that made it difficult for members of the Senate and House to fly out of the nation's capital for a summer recess. The FAA went public with its $2.8 billion plan for AERA engineering and development just prior to the strike.

By using computers linked in a network, the system would automatically assign the most efficient flight routes, guarantee adequate aircraft separation, and monitor aircraft in flight—functions now performed manually by controllers. **In addition to providing greater safety, potential annual savings from the program could reach $6 billion,** thanks in part to increased controller productivity and reduced aircraft fuel consumption, says the FAA. "Controllers today are as important as telephone operators were in the '30s to AT&T," says one FAA official, "but we could automate many of them out of the system with AERA."

Venus radar mapper set for development

Full-scale development of the $150 million Venus-orbiting imaging-radar (VOIR) spacecraft is expected to begin in early 1982 when the National Aeronautics and Space Administration says it will select a contractor. **The competition is between Hughes Aircraft Co. of Los Angeles and Martin Marietta Aerospace in Denver**, which received proposal requests earlier this month from NASA's Jet Propulsion Laboratories, Pasadena, Calif. The two companies have completed VOIR definition studies, and their proposals are due by the end of September. To be launched in 1988 from the orbiting space shuttle, the spacecraft will use a synthetic-aperture radar, being developed separately, to make a fine-scale map of Venus for transmission back to earth.

Washington commentary

What Reaganomics portends for DOD and U. S. allies

By the end of next year, possibly sooner, the American public should be able to judge if President Ronald Reagan's economic policies—dramatic reductions in Federal taxes and in spending for social programs—are as good as the politics he used to get them through Congress, particularly the Democratic-controlled House.

"Lyndon Johnson played good politics in getting Congress to adopt his guns-and-butter policy and increase American intervention in Vietnam," recalls one hard-line Democrat on Capitol Hill, "but it caused his Great Society to collapse around him and drove him from office. Since then we have had to live with the worst inflation the country has ever known." While that speaker insists that he hopes the Reagan program works "for the sake of all of us," he says President Johnson's experience illustrates that good policies do not follow necessarily from good politics.

Long-standing adversaries

Private sector analysts of the Federal budget and tax programs are carefully watching how industry responds to the Reagan initiatives. Except for the tax incentives for increased capital investment in equipment and for research and development, says one, there are areas where companies "can take the money and run." And no doubt some will, he goes on, even though that will be the worst thing they could do to the national economy and their own competitiveness in the long term. Those holding the pessimistic view argue that looking out for No. 1 is a historic product of the U. S. economic development, where Government and business have virtually been adversaries. "The kind of teamwork that you find in countries like Japan is unknown in this country," notes one lobbyist. "The adversarial system is so ingrained in our society that it will be hard to change."

A cap for Weinberger?

As if these challenges to making the President's domestic economic programs work were not enough, there are new problems arising that will make it more difficult for the U. S. to deal with its allies next year and thereafter. One of the most serious, again a product of economics, lies in the area of military spending.

The Office of Management and Budget has received authority to order the Department of Defense to draft an alternative fiscal 1983 budget for submission to Congress next January that would slash proposed spending by up to $13 billion from the $254.8 billion planned [*Electronics*, June 30, p. 88]. That option is being sought by the White House in case the economy turns sour and the Federal deficit fails to decline as forecast, leaving inflation and interest rates at unacceptably high levels. There is no question of cutting back on personnel, so the $13 billion would have to come from hardware procurement or from a delay of the initial phases of major new programs like the MX missile.

Beyond producing a classic confrontation at home between OMB director David Stockman and Defense Secretary Caspar W. Weinberger, slowing the U. S. military buildup is certain to damage President Reagan's relations—as well as his strong-man image—with the U. S.'s allies in Europe and Japan. Much of the blame for that will be placed on Secretary Weinberger who has spoken out sharply and consistently in public for greater military spending by Japan and Europe, calling on them to follow the U. S. lead. In fact, while President Reagan was in Ottawa last month, meeting with the government heads of America's major trading partners, Weinberger was in Washington, criticizing them about their defense outlays.

Tactless diplomacy

However correct Weinberger's criticisms may have been, "he will never succeed with Japan by speaking publicly and in the press on this issue," says one Washington expert on Japan and its culture. The same can be said of a proud West Germany, whose forces regularly defeat their U. S. counterparts in the North Atlantic Treaty Organization's war games.

In either country, it would be politically unacceptable for government leaders to appear to be knuckling under to U. S. pressure for increased defense outlays. "These are issues where pressure can only be brought in private if you expect any success at all," explains another Administration official. "In public, Weinberger should keep his mouth shut."

In this case, it is an example of bad politics guaranteeing a foreign policy failure. And that failure will be compounded if American military budget growth over the next few years is reduced as a result of domestic economic considerations.

-Ray Connolly

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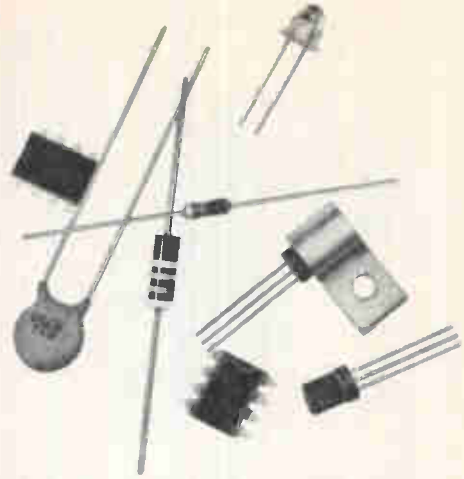

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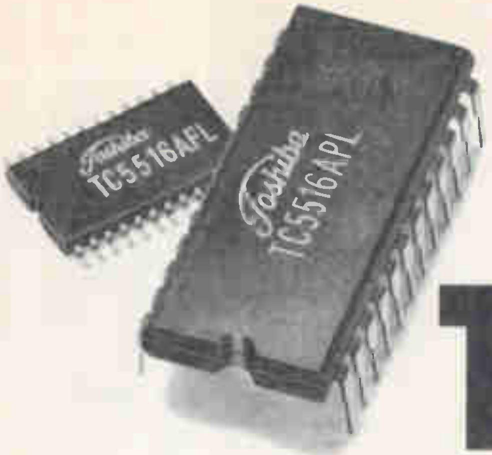

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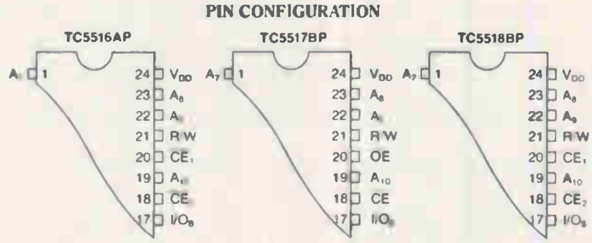

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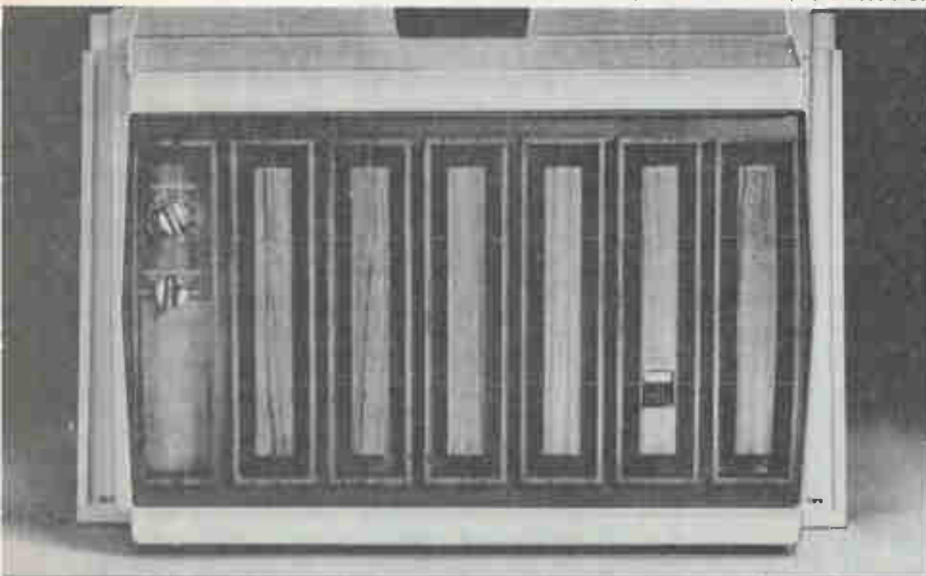

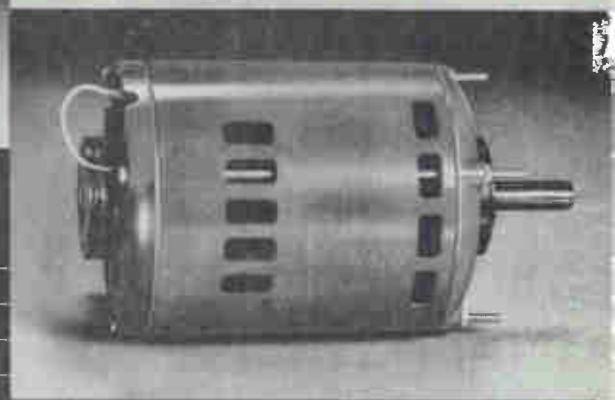

Inverter SCR families.

Family	Package	Highest Voltage	RMS Current	Maximum TQ
S306	TO-202	600 V	3 A	12 μs
S370	TO-66	700 V	5 A	6 μs
S390	TO-220	750 V	5 A	3 μs
S580	TO-220	600 V	5 A	5 μs
S731	TO-48	600 V	40 A	4 μs
2N3658	TO-48	600 V	35 A	10 μs

Circle 54 on reader service card

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International newsletter

Siemens to make bubble systems . . .

Watch for Siemens AG to become the second European company, after the UK's Plessey Microsystems, to start manufacturing magnetic-bubble memory systems out of U. S. chips [*Electronics*, June 30, p. 76]. It plans to come out in October with samples of two magnetic-bubble memory modules mounted on 100-by-160-mm Eurocards using Intel Corp.'s 1-Mb bubble-memory devices. One is the 128-K-byte card E 141 and the other the 256-K-byte card E 142. A third card, the E 140, serves for memory control. **Using these modules, a memory system with a capacity of up to 1 megabyte can be put together.** The memory devices operate off a standard supply of +5 and +12 V, and their wide operating temperature range of 0° to 70°C makes them well suited for applications in rough environments.

. . . and Fujitsu's will sell in the U. S.

Samples of a 1-Mb magnetic-bubble memory cassette and a 4-Mb bubble memory board from Fujitsu Ltd. are available now in Japan and will be available in the U. S. in September. Both products use **a new 1-Mb chip that has a bubble diameter of only 1.9 μm.** The cassette has 512 loops of 2,048 bits each and sells for $2,450 with associated circuitry. The $7,350 board has 8,192 pages of 512 bits each with an 8-bit parallel interface for direct memory access capability. Both have an average access time of 12.5 ms and a maximum data rate of 100 kb/s. Custom peripheral circuits will be used when production units are shipped late this year or early next.

British Telecom eyes satellite for TV and business

British Telecom is discussing with the government, private industry, and the British Broadcasting Corporation a $360 million proposal for a satellite that would beam TV broadcasts directly to rooftop antennas, as well as provide a high-speed data service to business users. To be built by British Aerospace and by Marconi Space & Defence Systems Ltd., the bird **would be launched in 1985,** about a year behind Project Mercury, an alternative terrestrial proposal that uses high-speed fiber-optic links [*Electronics*, July 14, p. 63].

Bell testing Japanese optical-fiber cable

Fujikura Cable Works Ltd. is shipping optical-fiber cable to Bell Telephone Laboratories in Holmdel, N. J., for tests to qualify it for use in long-distance submarine transmission systems. The order is for a total length of 65 km of cable priced at $216,450. If this cable, whose attenuation is only 0.7 dB/km, performs to specifications, it **may be selected for use in the transatlantic line** that American Telephone & Telegraph Inc. wants to put into operation by 1988.

UK to automate fabrication of gate-array masks

Three government laboratories, four electronics companies and a number of British universities are planning to collaborate in UK 5000, a program to develop software for the automatic generation of uncommitted logic-array masks directly from a customer's logic diagram. **One aim is to provide an extremely fast design-turnaround service by 1982,** interfacing CAD software, which also automatically generates test-tape patterns, with a direct electron-beam writer at the Science and Engineering Research Council's Rutherford Laboratories. Double-layer metalization, laid out on an X-Y grid, would complete complementary-MOS arrays of up to 6,000-gate complexity. Participants in the 33-man-year software project include British Telecom, the Science and Engineering Research Council, the Royal

Signals and Radar Research Establishment in Malvern and, from industry, ICL, GEC Telecommunications, TMC, and Standard Telephone & Cables. The program will be partly funded by the Department of Industry.

10 Japanese firms pool bids for project to improve active devices

Ten Japanese firms have set up a foundation to bid for research and development contracts on new functional devices that will be funded by the Ministry of International Trade and Industry [*Electronics*, Jan. 27, p. 67]. Work on the devices—**superlattice devices and ballistic transistors, three-dimensional integrated circuits, and devices capable of functioning in hostile environments**—will then be divided among the members. Outside firms can also bid, but most Japanese firms with the potential for doing this work belong to the foundation. The members are: Fujitsu, Nippon Electric, Hitachi, Toshiba, Mitsubishi Electric, Oki Electric, Sumitomo Electric Industries, Matsushita Electric Industrial, Sharp, and Sanyo Electric. The ministry is accepting contract applications from Aug. 5 through 15 for a probable decision in early September.

Ceramic has Invar's temperature stability

A new dielectric resonator material intended for very high frequencies has been developed for the European Space Agency by Thomson-CSF's central research laboratories in the Paris suburb of Corbeville. The zirconium titanate–based ceramic has the temperature stability of Invar and **yields 4-to-12-GHz oscillators and filters.** In satellite applications, such filters would make possible waveguide resonators that are smaller and handle more power than conventional units and are compatible with microwave integrated circuits.

Inmos simulating microprocessors

Evidence that Inmos Ltd. is working away at new microprocessor designs comes from the International Conference on Very Large-Scale Integration to be held Aug. 18–20 at Edinburgh University, where **the company will describe a multilevel logic simulator developed for internal use.** Commercially available software was not up to the task of simulating complex microprocessors, says the Bristol company, so it has developed a three-level simulator, employing high-level, modular, structured languages. The lowest level simulates the analog properties of MOS transistors and interfaces automatically with the second level, which simulates the operation of dynamic MOS logic. The third level allows the designer to describe his system's operation.

Addenda

By 1990 there will be some 20,000 industrial robots operating in West Germany, according to a forecast from the Frankfurt-based market analysis firm Gewiplan GmbH. . . . Victor Co. of Japan has developed a **compact video-tape cassette that can be recorded with the Video Home System format** on a down-sized portable video-cassette recorder and played back via an adapter on a standard VHS VCR. . . . Next month RTC-La Radiotechnique Compélec of Paris will introduce a new diode laser for high-output fiber-optic transmission. **The laser transmits 560 Mb/s at a wavelength of 850 nm,** injects 5 mW into the 100-μm-wide fiber, and has a response time of less than 0.5 ns.


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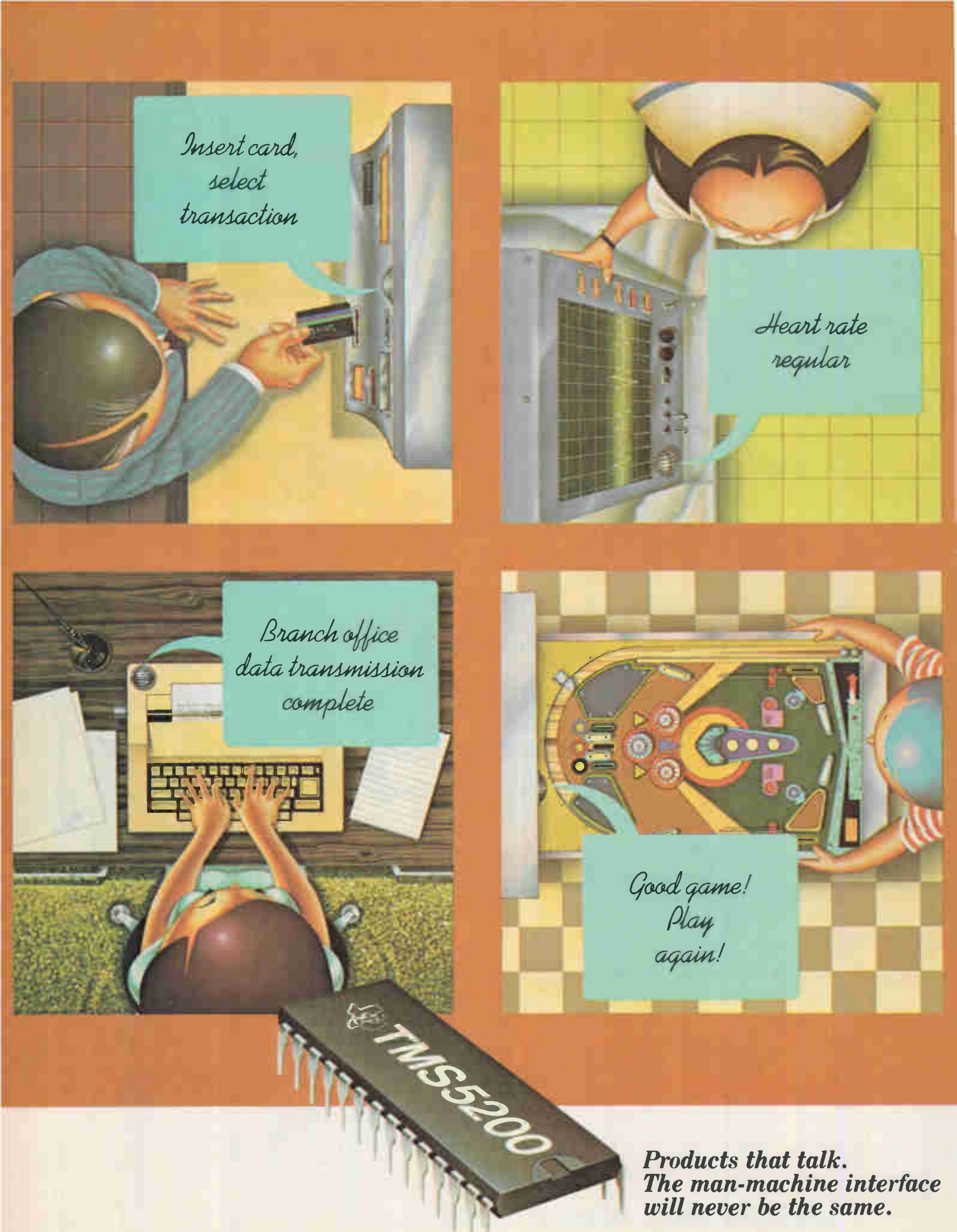

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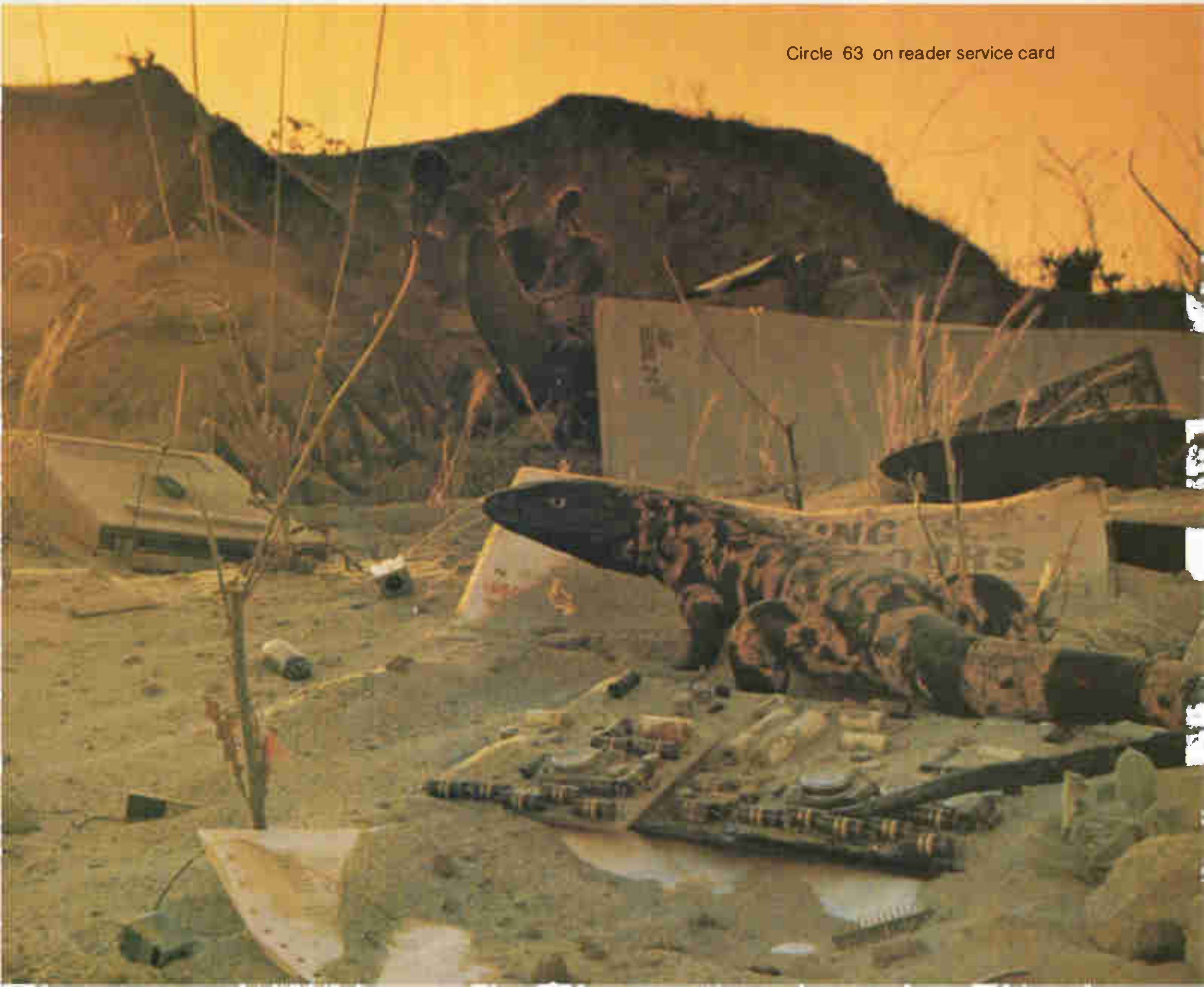

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Electrochromic display rivals liquid crystal for low power needs

by Charles Cohen, Tokyo bureau manager

Technique has novel uses, too, as segments are deeply colored when turned on but transparent when turned off

Electrochromic displays may soon become a strong competitor of liquid-crystal displays for some of their present applications. The thin-film display developed at Nippon Kogaku KK, manufacturers of Nikon cameras, features a deep blue black color that can be read from any angle, plus low power operation—it needs almost no current to stay turned on. Furthermore, the individual dots, segments, or characters are transparent when not turned on. This opens up a whole new range of applications within optical systems, according to Yosuke Takahashi, a senior researcher at the firm's research laboratory.

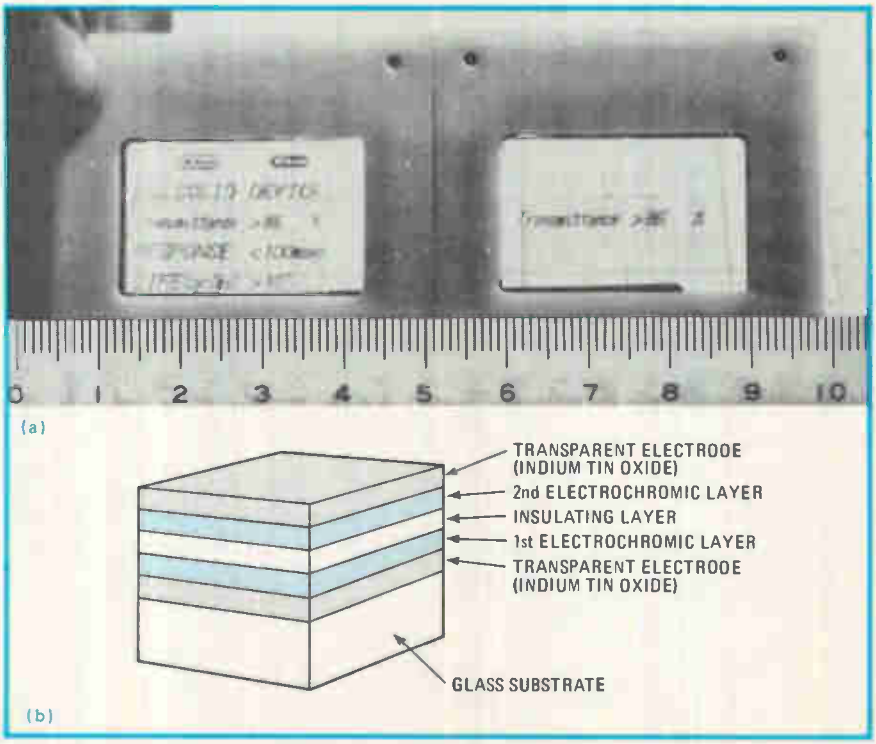
Unprecedented. As an example, his group has fabricated a reticle for a 10× magnifier. The square grid of 15-micrometer-wide lines on 1-millimeter centers can be turned off so that it does not interfere with observations. Still another application, Takahashi states, is variable neutral-density filters that do not have to be manually swapped to change density. The reticles will probably be used in cameras and microscopes, and the filters in surveying equipment.

Takahashi's group has also built a prototype watch whose display driver and display require about the same input power as those for an LCD unit when indicating hours and minutes. The watch would consume more power than the LCD version if it indicated seconds, unless it did so only at the user's wish.

A display with a total character segment area of 1 square centimeter requires 7 or 8 millicoulombs to turn on. In other words, turning the display on in a tenth of a second requires a 70-milliampere current throughout that period. On the other hand, after the display is turned on, the current falls almost to zero. Voltage can be removed at that time because even after 12 hours the density decay is only 50%. A reverse-polarity pulse is required to clear the display.

When operated at a constant voltage of only 1.4 volts, the device turns on in less than 100 milliseconds. Turn-off time for the same voltage with reverse polarity is less than 50 ms. An experimental display has operated at a 1-hertz repetition rate for more than 50 million cycles with no visible degradation.

Layered. The display employs five submicrometer thin-film layers with a total thickness of 1 to 1.5 μm on a glass substrate. In the future, their thicknesses may be adjusted for enhanced antireflection or other optical properties. In the order in which they are deposited on the glass substrate, the layers form: a transparent conducting electrode of indium tin oxide; the first electro-



Blue black. When the electrochromic display in (a) turns off, it becomes transparent. Tungsten oxide could form the first electrochromic layer (b), a metallic hydroxide the second.

chromic layer; a porous solid electrolyte; a second electrochromic layer; and a transparent conducting electrode of indium oxide.

Takahashi is reluctant to speak about materials because he says patent applications are being filed on the materials used, but tungsten oxide is a possible choice for the first electrochromic layer. Nickel and other metallic hydroxides are used for the second electrochromic layer. Connection of a negative voltage to the upper indium oxide electrode causes the transport of positive hydrogen ions (from moisture in the thin films) to the normally colorless tungsten oxide, causing it to change into hydrogen tungsten bronze (H_xWO_3), which is blue. At the same time, additional negative hydroxyl ions are transported to the colorless metallic hydroxide, causing it to become black.

As for the future, Nippon Kogaku is just about to make a decision on what applications it will develop and whether it will sell components or the technology.

Academic origin. Work on this display from October 1977 through October 1980 was aided by an interest-free loan of $800,000 from the Research Development Corp. of Japan, which sponsors the commercial development of inventions of researchers outside of industry—in this case, a method of fabricating thin films by radio-frequency reactive-ion plating, developed by Prof. Yoichi Murayama of Tokyo University. In the electrochromic device the upper indium oxide transparent electrode and at least one of the other layers is created by the reactive-ion plating method, which Takahashi says makes it possible to fabricate certain types of thin films without degrading or destroying those lying underneath.

IBM Corp. and others have worked on liquid-phase electrochromic displays but seem not to have been able to achieve good lifetime—at any rate, no products have appeared on the market. At least two Japanese universities have also studied solid electrochromic displays, but again no products have resulted.

West Germany

Electron-beam system needs little power to heat-treat silicon for solar cells

A laboratory-type electron-beam generator promises to lower the cost of heat-treating the surface of solar cells to the point where the process becomes attractive even in mass-producing cells. The unit is the result of a two-year development effort at the nuclear research center in Karlsruhe, West Germany.

Surface tempering is crucial for raising a solar cell's light-to-electrical-energy conversion efficiency and has been the subject of investigations at various research labs around the world. But as Jochen Geerk, one of the two developers of the Karlsruhe equipment, points out, some of the apparatus he has heard of so far is too elaborate and the rest requires too much energy. Laser-based tempering systems fall into the first category, and other electron-beam generators built for cell surface tempering fall into the second.

Today's solar cells generally consist of single-crystal silicon in which impurities are imbedded at very low and precisely controlled concentration levels. In theory, cell efficiency should be about 20% to 22%, but in practice it is only around 10% and depends chiefly on the crystal lattice

10 Italian taxis save gas on two cylinders

In pursuit of an automobile with a less voracious appetite for gasoline, Italy's Alfa Romeo SpA is trying the approach pioneered by General Motors Corp. of the U. S.—an engine that uses fewer than all its cylinders at low speeds. The state-owned company is currently road-testing a microprocessor-controlled, four-cylinder engine that by running on two cylinders is cutting fuel consumption by over 35% in city traffic and could cut it by 12% at highway speeds of up to 90 kilometers (60 miles) an hour.

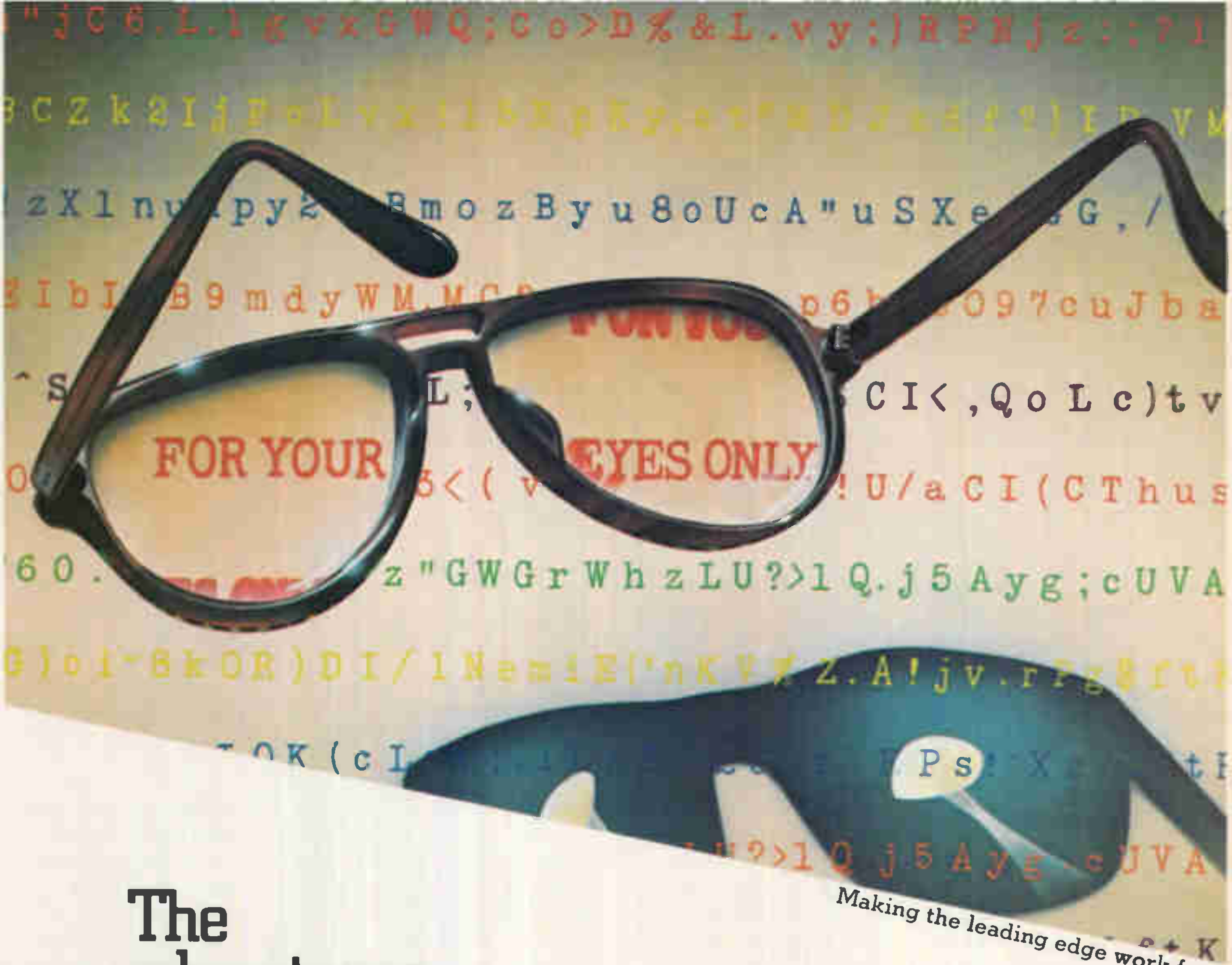
The Alfa system not only interrupts the flow of gasoline to one of two pairs of cylinders—it also alternates between the two pairs so that neither suffers differentially from wear and tear. Each cylinder has its own fuel injector. The system betters 1982 Common Market antipollution standards.

In contrast, the GM system that allows an eight-cylinder engine to run on four or six cylinders, as appropriate, does not balance its use of cylinder pairs. Also, each of GM's two systems employs just two fuel injectors—not one per cylinder—and of course meets U. S. antipollution requirements.

In the Alfa engine, an Intel 8085 microprocessor regulates fuel flow. It monitors throttle angle, the number of revolutions per minute, and coolant and air temperatures and then, when it judges two-cylinder driving is in order, closes one pair of fuel injectors, leaving their associated pair of cylinders to suck in air only.

The constant switch in cylinder pairs in two-cylinder driving occurs every minute or less and derives from the natural oscillations of the driver's foot on the gas pedal. Alfa engineers report: "We have a very complicated algorithm to compute maximum and minimum time." They admit that the driver running on two cylinders notices "a little less response than from four cylinders, comparable to a not-too-well-tuned car, but gets the usual performance as soon as he opens up the throttle again."

The Milan-based company's decision whether or not to produce the motor will be based on an experiment currently under way on 10 of Milan's hard-driven bright-yellow Alfa 2.0-liter taxis. The results will be analyzed after the 15,000 km each taxi is expected to log by fall. So far their total is 60,000 km, and their more than 35% savings gratifyingly in excess of the 20% maximum predicted. **-Lois Bolton, McGraw-Hill World News**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quality of the cell's light-sensitive surface.

The key to this high quality is thermal treatment that cures the crystal imperfections caused when the impurities are imbedded in the silicon. But so as not to redistribute those impurities, the treatment must be brief, on the order of fractions of a microsecond.

Properly controlled tempering can raise a silicon cell's efficiency by several percentage points. But for mass production, the related equipment must be inexpensive and the energy requirements low—and this is where the electron-beam generator from the Karlsruhe research center comes in. Once such a generator for tempering a large number of cells in a single process is perfected, Geerk speculates, it will cost several times less than laser-based systems at present do.

As for the energy requirements, the equipment works with 10 to 25 kiloelectronvolts for a 1-micrometer penetration, although for proprietary reasons, the Karlsruhe developers are reluctant to say more at this time than that a special cathode and ignition system design are responsible. In comparison, 10 to 300 kev is employed by the prototype of a production machine made by Spire Corp. of Boston, Mass., the industry leader in electron-beam generators for solar-cell tempering.

Alike. In other respects, the two designs are not dissimilar. Beam width is around 5 centimers in both and so can cover relatively large cell areas. In addition, for the German and U.S. machines, respectively, pulse duration is 300 versus 100 nanoseconds; beam current density is 1.3 to 3 kiloamperes per square centimer versus more than 1 kA/cm^2; and the pulse energy imparted to the material is 0.3 to 2.5 $joules/cm^2$ versus 0.1 to 10 J/cm^2.

Present investigations at the Karlsruhe center are aimed at the system's industrial use. For a French research institute, a system is now being readied that will replace its laser-based tempering equipment and be used in solar cell development. **-John Gosch**

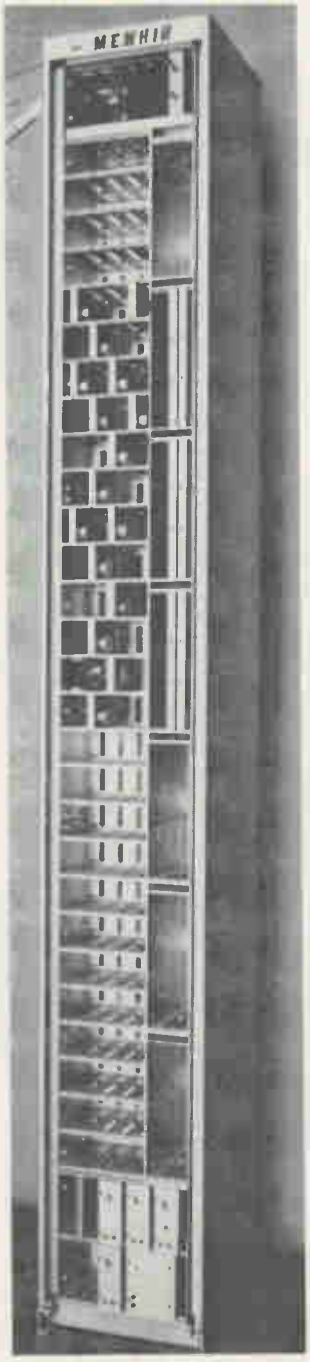
France

Digital telephones plug into interface with analog net; first trial set for 1982

Telephone subscribers who want the latest in digital equipment could easily be at odds with their local exchange and its analog main distributing frames (MDFs). But at the Lannion, France, laboratories of Centre Nationale d'Etudes des Télécommunications, a system has been developed that exploits improvements in individual subscriber equipment (ISE) so as to allow multiplexed digital communications to be interfaced with the existing network.

Menhir, a French acronym for experimental module for a harmonized digitization of the interface with the network, replaces the MDF with a digital switching frame installed at the input of the distribution cables. At the subscriber's end of the line, the ISE converts the speech signal from analog into digital information, besides taking care of the normal Borsht (battery, overvoltage, ringing, supervision, hybrid, and test) functions.

"The main distributing frame is clearly obsolete and gets very cumbersome and complex when dealing with more than 20,000 lines," points out Daniel Hardy, a CNET telecommunications research engineer. "Menhir is not only far more compact than the MDF, but it offers many operational advantages as well." Putting a subscriber's link into service, for example, is as easy as plugging in his individual equipment. Consequently, control of the structure is remarkably easy because the fact that a given ISE is plugged in indicates that that particular wire pair of the cable is assigned. What's more, free places left by unassigned loops can be adapted to, say, tone generators. And since one digital multiplexer can replace about 100 telephone pairs, the number of links necessary between the connecting frame and the switch is dramatically reduced.



Menhir updated. This experimental module multiplexes digital inputs from 112 lines, the capacity of standard French cable, into existing analog switch.

Capacity. The prototype Menhir frame developed at CNET has a capacity of 112 lines, equal to that of a standard French cable. Each ISE is assigned two digital 64-kilobit-per-second time slots, one each for the coded speech signal and the line signaling. Since the digital paths of 16 ISE units are multiplexed on a single 2.048-megabit/s internal

digital link, the Menhir frame includes seven such links.

So far, two methods of connecting with the digital switching center have been tested. The first uses a 2.048-Mb/s external digital link connected to an identical internal link by way of a digital switch with a capacity of 256 time slots. The digital switch uses semipermanent connections to route only the digital time slots corresponding to plugged-in subscriber equipment onto the external multiplexer, where they are arranged in single file.

For this reason, the number of external links is directly proportional to the number of subscribers' lines in service at any given time, and the number of ISE units serviced is optimized, being exactly the same as the number of lines used. The function of the digital switch is parallel to that of the jumper wires in a conventional MDF. In Menhir, though, the function is performed by programming connections.

Switchless. This connection method, however, is seen as transitional to the second, which multiplexes the seven internal links onto an optical fiber, omitting the switch. The fiber carries 16 Mb/s and, being at most 50 meters long, could carry 34 Mb/s. Used this way, the Menhir frame can be viewed simply as a multiplexer.

Though it has performed well in laboratory tests, Menhir has yet to be put to a full in-service test. But according to Hardy, a Menhir frame will be installed, in an as-yet-undesignated French exchange, some time next year. **-Robert T. Gallagher**

Great Britain

Two chip makers cooperate in developing 10,000-gate arrays for big new market

Pressure from British Telecom has eventually persuaded two of Britain's indigenous semiconductor manufacturers to cooperate on the development of a very large-scale integrated version of the Iso-C-MOS process. Both are subsidiaries of major equipment companies and, like British Telecom itself, had independently licensed the isoplanar complementary-MOS process from Mitel Inc., the Canadian telecommunications equipment maker.

Their goal is to provide a dual source for 10,000-gate-and-up uncommitted logic arrays by 1983, when they believe the world market for C-MOS ULAs will be around $700 million. Before then, moreover, the two companies—Plessey Semiconductors Ltd., Swindon, Wilts., and Marconi Electronic Devices Ltd. of Lincoln—will jointly introduce later this year a family of 1,000-, 1,500-, and 2,000-gate ULAs. The idea is to gain such market leverage with the dual-sourced parts as to make them a potential European standard.

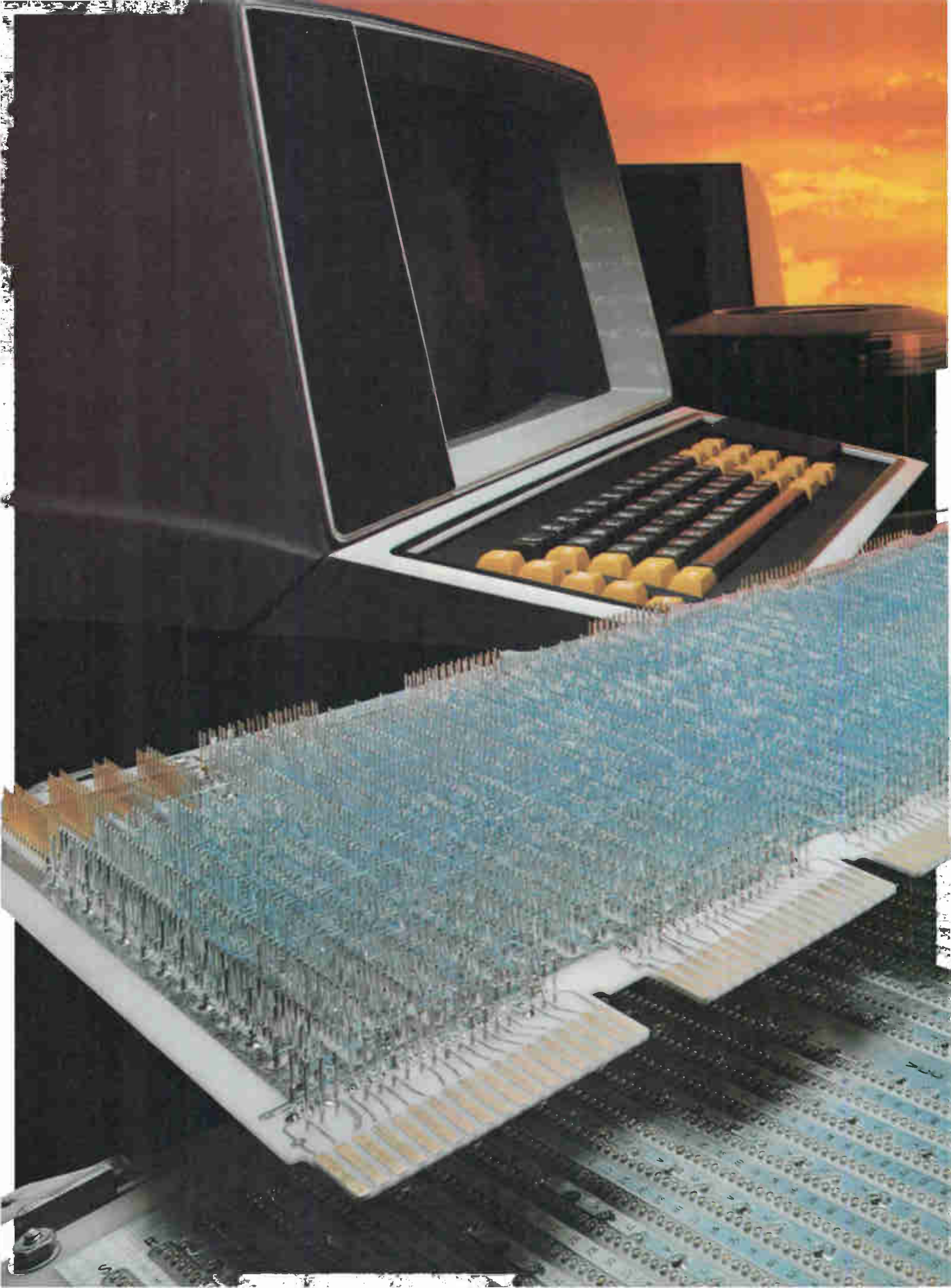
Apart from security of supply, alternative sources can ensure a competitive price and the avoidance of prototyping delays, explains John Brothers, a Plessey Semiconductors marketing manager. In fact, British Telecom made it clear to both companies that they would need to arrange dual sourcing if they were to participate in its System X digital telephone exchange program. Other equipment manufacturers, too, are becoming concerned about the need for dual sourcing. For example, Stack, a consortium of computer manufacturers headed by Control Data Corp. of the U. S. and including British Telecom, is defining a common requirement for multiply sourced ULAs.

Other targets. Further, the Plessey-Marconi agreement embraces both standard and special-purpose system components. The two will manufacture under license octal complementary-MOS parts from Mitel and will add parts to this family. Also targeted are peripheral chips for the 6802, including a 6846 read-only-memory input/output device and a 6850 communications interface chip. Special-purpose system parts started include codec and codec-filter chips, as well as a 16-by-16-bit time-division–multiplexing switch array for potential use in Britain's new System X. If the two companies manage to live together, then collaboration will likely extend to computer design aids, seen as a means of overcoming the engineering bottleneck that would otherwise succeed in stifling the burgeoning ULA market.

Coordinating process development sounds fine in theory but has yet to be proved in practice. Plessey and Marconi will retain separate process development teams and will share results and coordinate key process equipment purchases through an eight-man committee drawn equally from the senior management of both companies. The two groups envisage collaborating initially for four to five years on the development by 1983 of a process using 3-micrometer geometry and double-layer metalization and capable of supporting ULAs of 10,000-gate complexities.

Competition. These projections are to be compared with those of Ferranti Semiconductors Ltd., whose rival bipolar process is also slated to yield 10,000-gate devices by 1983 [*Electronics*, June 16, p. 76]. However, the Manchester company is probably further down the track, as it has completed process development and has already moved to 3-μm geometries for the 2,000-gate arrays due out later this year.

Eventually, Plessey and Marconi envisage a scaled-down 2-μm process. But their first move away from Mitel's technology will be to add double-layer metalization because, says Brothers, it is far easier to automate cell routing if interconnections can be laid without restraint on an X-Y grid. ULA growth, he believes, will be limited not by production capacity, but by the design engineering resources available. The answer is to automate circuit design and hand it back to the equipment manufacturers, a factor that Texas Instruments was evidently quick to appreciate, he notes. **-Kevin Smith**



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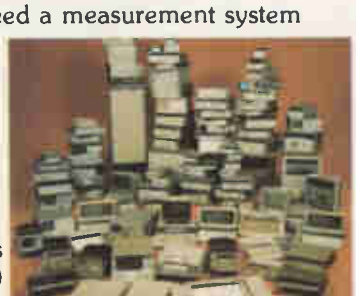

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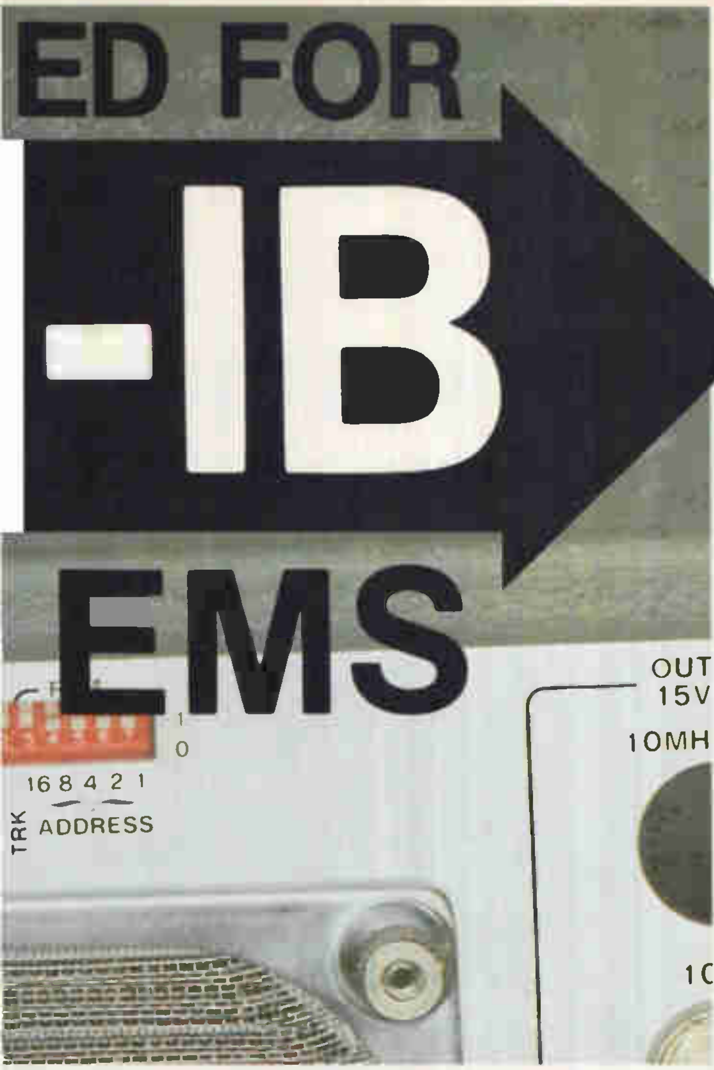

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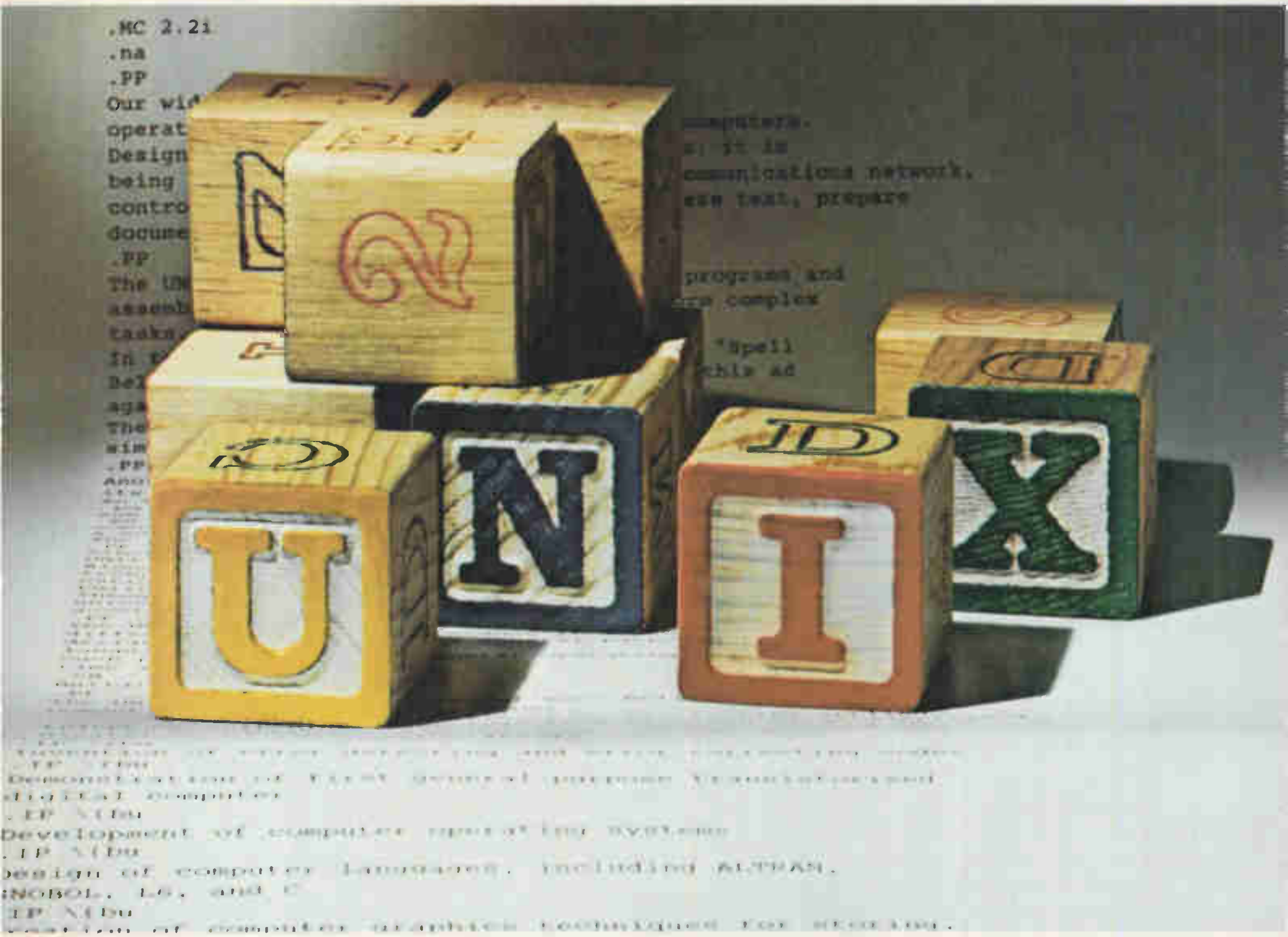

The computer printout in the picture above contains the instructions and input needed for the *UNIX* system to format and produce the text on the opposite page.

Our widely accepted *UNIX*™ operating system is simplifying the use of computers. Designed to handle a variety of applications, it is being used to manage and maintain the telecommunications network, control experiments, develop software, process text, prepare documents, and teach computer science.

The *UNIX* system allows users to take small programs and assemble them like building blocks to perform complex tasks. In text processing, for example, the command "Spell Bell Labs Ad" tells a computer to proofread this ad against a dictionary filed in its memory. The program that performs the task was created by simply combining several smaller *UNIX* programs.

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$$\sum_{i=1}^{\infty} \frac{1}{x_i} = \pi$$

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- First demonstration of remote computer terminal and data link
- Conception of electronic analog computer
- First design of AND and OR gates for diode circuitry
- Formulation of Information Theory
- Invention of error-detecting and error-correcting codes
- Demonstration of first general-purpose transistorized digital computer
- Development of computer operating systems
- Design of computer languages, including ALTRAN, SNOBOL, L6, and C
- Creation of computer graphics techniques for storing, manipulating, and presenting information
- Development of Fast Fourier Transform
- Design of central processors for switching systems having virtually no downtime

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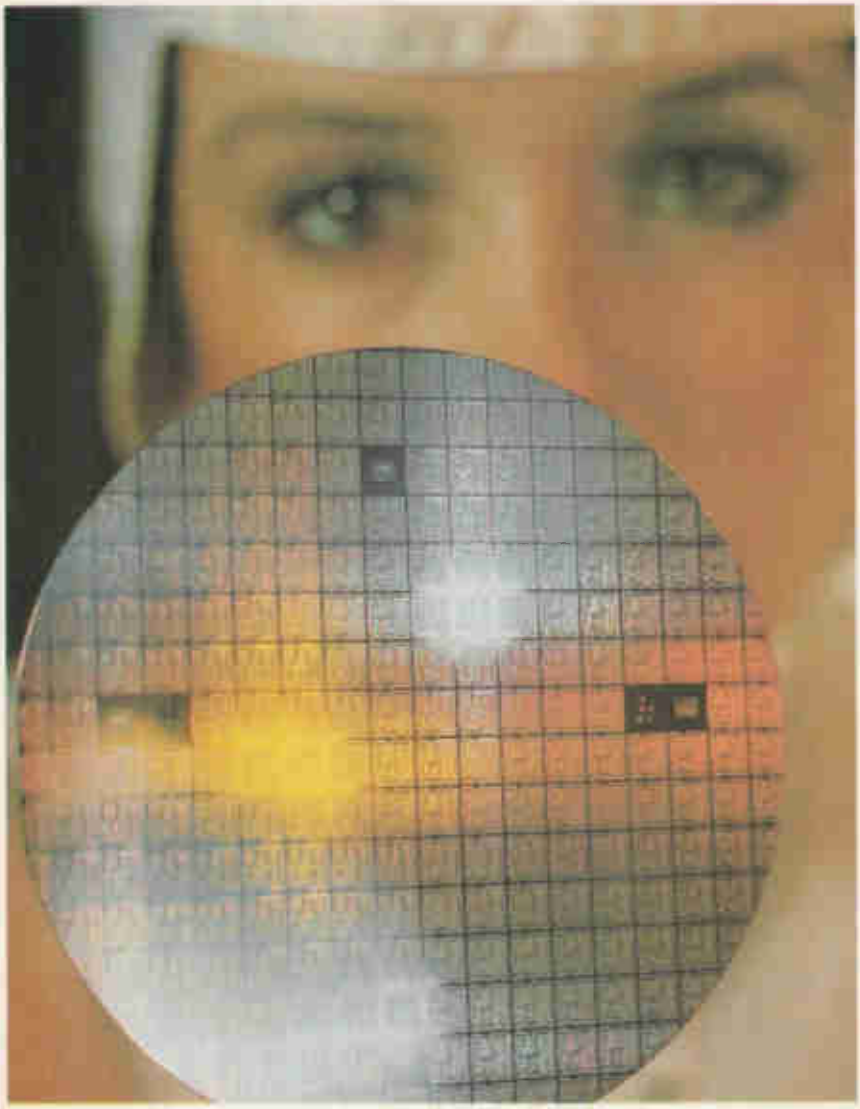

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GENERAL INSTRUMENT

French nationalizations pose problems

Socialist government says it will make its moves slowly, sets no firm timetable for nationalization of big electronics firms

by Robert T. Gallagher, Paris bureau

The long-term effect of the planned nationalization of 11 major French industrial groups is a matter that is still subject to debate. Although there is little chance that the new Socialist government headed by President François Mitterrand and Prime Minister Pierre Mauroy will drastically change the existing general structures in the electronics industries, it does seem certain that there will be more than a simple nationalization of holding companies and a *laissez faire* attitude from the government. "That would be only a symbolic move," says one well-placed official, "and symbolism is very low on our list of priorities."

The electronics companies to be affected are the giant conglomerates Compagnie Générale d'Electricité and Thomson-Brandt, computer and peripherals manufacturer CII-Honeywell Bull, the defense arm of Matra SA, and ITT (France). An official in the ministry for the expansion of the public sector says the first nationalizations, including CGE and Thomson-Brandt, will take place in the autumn session of the French National Assembly.

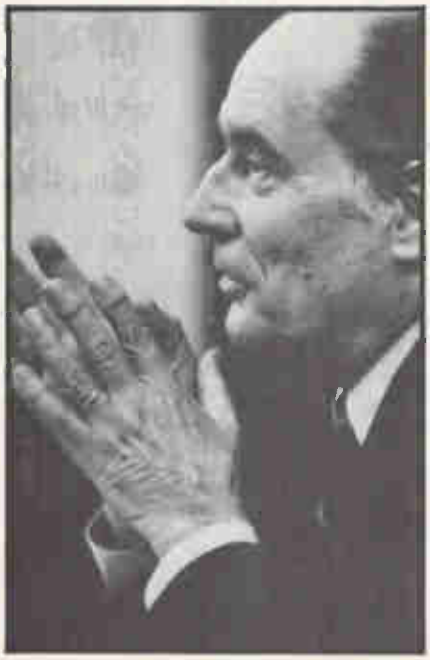
But this same official could give few details on just how the nationalizations would affect the companies. "We are very limited in what we can say at the moment for two reasons," he says. "The first is that most of the decisions simply have not been taken yet, and the second is that whenever we say—or even imply—something, the stock market goes crazy. Because the modalities of compensation of the stockholders have not been worked out yet, we want the market to stay as stable as possible."

"What I can say is that any significant change will come slowly," he goes on. "Particularly in the electronics industries, where most of the companies are well-organized and profitable, we have no desire to upset the apple cart. Our objective is to restructure industry so that it is more competitive on world markets and, thus, to create employment."

Fact hunt. For the moment the government has appointed delegates to fact-finding missions at Thomson-Brandt and CGE, as well as another to look into a possible merger of the Matra defense arm with the already nationalized Société Nationale Industrielle Aerospatiale. In September, it expects to have a concrete idea of just what form the nationalizations will take. But already there are some hints to be had in a document called "General Orientations for an Industrial Policy for Electronics, Data Processing and Telecommunications," published by the executive bureau of the Socialist Party in February 1981 just before the campaign that resulted in the Socialist victory.

A party, to be sure, is not a government. But officials at the prime minister's office and the ministries of industry, defense, and expansion of the public sector confirm that at least the general outlines of the document describe accurately the government's present mood.

The general thrust of the essay is that to compete in the American-



In charge. The Socialist government of Prime Minister Pierre Mauroy (left) and President François Mitterrand, in an effort to keep the stock market calm, is being careful not to commit itself to details of its planned nationalization of 11 major industrial groups.

and Japanese-dominated electronics markets, the French electronics companies must be reorganized in such a way that they concentrate on those markets in which they are particularly suited to compete. CII-Honeywell Bull, for example, would specialize in medium and large computer systems; Thomson-CSF, the principal subsidiary of Thomson-Brandt, would keep its lead role in military electronics; and CGE's CIT-Alcatel would remain the dominant force in telecommunications. In cases like integrated circuits, where the groups currently compete, a single company would be designated to take the lead.

Some questions. This leaves unanswered questions like: what will happen to Thomson-CSF's telecommunications switching activity if CIT-Alcatel becomes the leader in that sector? Also, who, if anyone, is going to compete in the still-growing minicomputer market?

One of the main principles guiding the choice of those companies to be nationalized is that all those largely dependent on government orders for their existence should become part of the public sector. Singled out were companies with large proportions of their gross sales in arms and defense and telecommunications. Despite the simplicity of the principle, when Mauroy announced his program to the National Assembly, there was one apparent contradiction.

Everyone knew that Thomson-Brandt would be on the nationalization list, but most expected Thomson-CSF, its 40%-owned subsidiary, to be included, too. Left as Mauroy stated it, the larger part of Thomson-CSF, a company heavily involved in both arms and telecommunications, would remain private.

While no one in the government was saying just why Thomson-CSF had been omitted, the general feeling was that the company would find its way into the public sector. "The idea of leaving the majority of a company that is nearly subsidized by the government in the private sector is, to me, simply inconceivable," said one official. "I could not guarantee that it will be nationalized in autumn with the first group, but it will, sooner or later, become part of the nationalized sector."

Tread softly. Perhaps the most delicate nationalization problems facing the Mauroy government will come from CII-Honeywell Bull, which is 47% U. S.-owned, and ITT France, a fully owned subsidiary of the American company. Regarding the CII problem, Honeywell Inc. of Minneapolis negotiated an agreement with the government of then-president Valéry Giscard d'Estaing in 1976 that took into account the possibility of nationalization. Honeywell, of course, in a carefully worded statement, says it expects the agreement to be honored and adds that the present government is fully aware that it is in the best interests of both not to sever connections.

Another U. S. company that is part owner of a French counterpart is National Semiconductor Inc. of Santa Clara, Calif., which owns 49% of Eurotechnique SA. St. Gobain Pont à Mousson, also on the government's list, is the majority partner. Pierre Lamond, National's vice president and technical director, says he does not expect any change in the transatlantic relationship. Eurotechnique's management will be unaffected by nationalization, he says, adding that the only change will be that the government will be the stockholder.

"We think it essential that any agreement for the nationalization of the companies include the means for keeping their commercial and technological links," says the official at the ministry for the expansion of the public sector. "We feel that the continuation of licensing agreements and cooperation on research and development would be of mutual benefit to both the French and American companies."

Just after Mitterrand's election three months ago, the general feeling in companies targeted for nationalization was that the holding companies would be nationalized and that business would continue as usual [*Electronics*, May 1, p. 71]. Now, with an absolute Socialist majority in the National Assembly, significantly more change than that seems certain. □

What the people are getting

The French electronics firms that will be nationalized beginning this fall are a study in diversity. What is more, Thomson-Brandt and the Compagnie Générale d'Electricité are studies in diversity in their own rights.

Thomson-Brandt is the only one of the companies active in consumer goods. It has an important portion of the French market in television and home video systems. Beginning next year, it will sell a personal computer. Other activities include engineering and mechanical equipment. Thomson-CSF's principal activities are defense electronics, avionics, and military and civilian radars, as well as telecommunications, integrated circuits (through its EFCIS subsidiary), discrete and bipolar semiconductors, and minicomputers (through its SEMS subsidiary).

The most visible subsidiary of CGE is CIT-Alcatel, which is not only a leading competitor in telephone switching equipment, but is also participating in the government-sponsored Télématique program and has ambitious plans in the field of office automation. Other major CGE activities include engineering, materials and insulators, cables and related products, batteries and condensors, and lamps. CGE also has a substantial banking sector, as well as a 31.5% interest in Alsthom-Atlantique, the electromechanical equipment and naval construction giant.

If just the lucrative defense activities of Matra SA are nationalized, the company will be forced to fall back on the subsidiary it owns jointly with Harris Corp. to produce complementary-MOS integrated circuits. Matra-Harris has, in turn, an agreement with Intel Corp. to set up a joint IC design facility in France.

ITT's principal French subsidiary is the Compagnie Générale de Constructions Téléphoniques, a telecommunications-switching-equipment maker that has been losing money. Last year ITT warned the French government that CGCT could not continue to stay in business indefinitely without French telecommunications agency orders for ITT's System 12 digital public telephone switching system. -R. T. G.

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Computers

IBM, HP join low-price fray

Both bring out bottom-of-the-line small-business computers and gird to compete with other big companies in under-$10,000 market

by Tom Manuel, Computers & Peripherals Editor

There is so much business in sight in small-business computers that mainframe and minicomputer makers are scurrying to add bottom-of-the line hardware—priced at $6,500 to $10,000—to their offerings. The latest to do so is the largest computer company, International Business Machines Corp. IBM joined the throng in late July—with Hewlett-Packard Co., the second-largest minicomputer supplier, slated to announce its entry in early August.

IBM has taken the wraps off its lowest priced small-business computer, the System/23 Datamaster. It sells for $9,830 with a printer and two 8-inch floppy-disk drives, and is being marketed by the General Systems division, Atlanta, Ga. The machine is now in stock in the division's district offices, except for the word-processing option, which will become available in September.

Crowded market. Now that several major makers have joined the many other small-business computer vendors in this segment of the computer market, a bloody battle for market share should begin. However, it seems unlikely that any one company will dominate the business—not even IBM.

A new industry study by Venture Development Corp., Wellesley, Mass., predicts that systems costing less than $20,000 will dominate the small-business computer market by 1984; shipments of these systems are expected to grow 33.5% annually from 1980 to 1984 and will account for nearly 50% of the sales by 1984. The study also predicts that large computer companies will lose much of their overall market share and will retain only about one third of the small-business sector at that time.

Analyst Karen Horowitz of Venture Development observes, "Each manufacturer's hardware is basically the same. No one has proprietary technology. Future industry leaders will have to develop unique strengths that are not easily adopted by competitors." According to a Xerox Corp. official, speaking at the formal introduction of the model 820 personal computer, "This marketplace is absolutely wide open. It is not dominated by anyone."

The desktop System/23 from IBM is a stand-alone work station based on the Intel 8085 8-bit microprocessor. The computer, called the 5322, is available in configurations with 32- to 128-K bytes of memory. The memory is from a variety of merchant integrated-circuit vendors. The computer with 64-K bytes of memory and 2.8 megabytes of diskette storage costs $7,050. The system has 112-K bytes of read-only memory. Two 5322 computers can share printers and an extra pair of floppy-disk drives.

Standard software included is an operating system and the Basic high-level language. Program products for accounting, communications, and word processing are available for a one-time charge. The word-processing package requires 64-K bytes of memory and another card for the computer. It controls the display for text processing, providing such features as vertical and horizontal segmenting, margins, tabs, and character highlighting. The word-processor software costs $500 and the word-processor card is $600.

Multifaceted. Like the System/23, the HP 125 desktop machine [*Electronics*, June 30, p. 33] combines the features of a small-business computer, a personal computer, a word processor, and a personal work station. It can also serve as an intelligent terminal for the HP 3000 series of business computers, enabling small-business users to tap large data bases.

Both the System/23 and the HP 125 offerings are very similar in features and price to systems that have

RECENT SMALL-BUSINESS COMPUTERS

	Processor	Word size (bits)	Memory (bytes)	Operating system
Data General Corp.: Enterprise 1000	Data General microNova	16	64-K	Enterprise OS
Datapoint Corp.: 1550	Zilog Z80-A	8	32-K to 64-K	CP/M
Digital Equipment Corp.: DECmate	New C-MOS chip extended PDP-8	12	32-K (words)	OS/78 and COS 310
Hewlett-Packard Co.: HP 125	Zilog Z80 A (2)	8	64 K	CP/M
IBM Corp.: System 23 Datamaster	Intel 8085	8	32 K to 128-K	Proprietary
Xerox Corp.: 820	Zilog Z80	8	64-K	CP/M

Source: *Electronics*

been recently introduced by other large companies including Digital Equipment Corp. the largest minicomputer company [*Electronics*, June 30, p. 143]. The first large commercial computer vendor to offer a small-business system of this type was Datapoint Corp. of San Antonio, Texas, with its model 1550 [*Electronics*, April 21, p. 165]. The table lists specifications of several new systems in this category.

These computers will be marketed through some of the newer distribution channels for small-business computers, as well as through each company's traditional sales organizations. For example, the System/23 will be sold in three new IBM retail outlets in Philadelphia, Baltimore, and San Francisco, by the General Systems division's district-office sales force, and in various business-computer stores in 50 cities.

Many outlets. HP, based in Palo Alto, Calif., is planning to market its 125 in three ways. Its field sales force will sell to large company accounts. The second outlet will be that family of third-party original-equipment manufacturers who add value with applications software. Also, office supply and business equipment stores that sell the HP 85 small computers will complete the sales network.

Xerox plans to market its 820 system [*Electronics*, June 16, p. 33]—the first small-business computer in this category from one of the billion-dollar-plus U. S. companies—through Xerox retail stores, computer stores, and a dealer network, as well as to its major customers through the Xerox sales force. The 820 will be marketed in Europe by the Rank-Xerox organization.

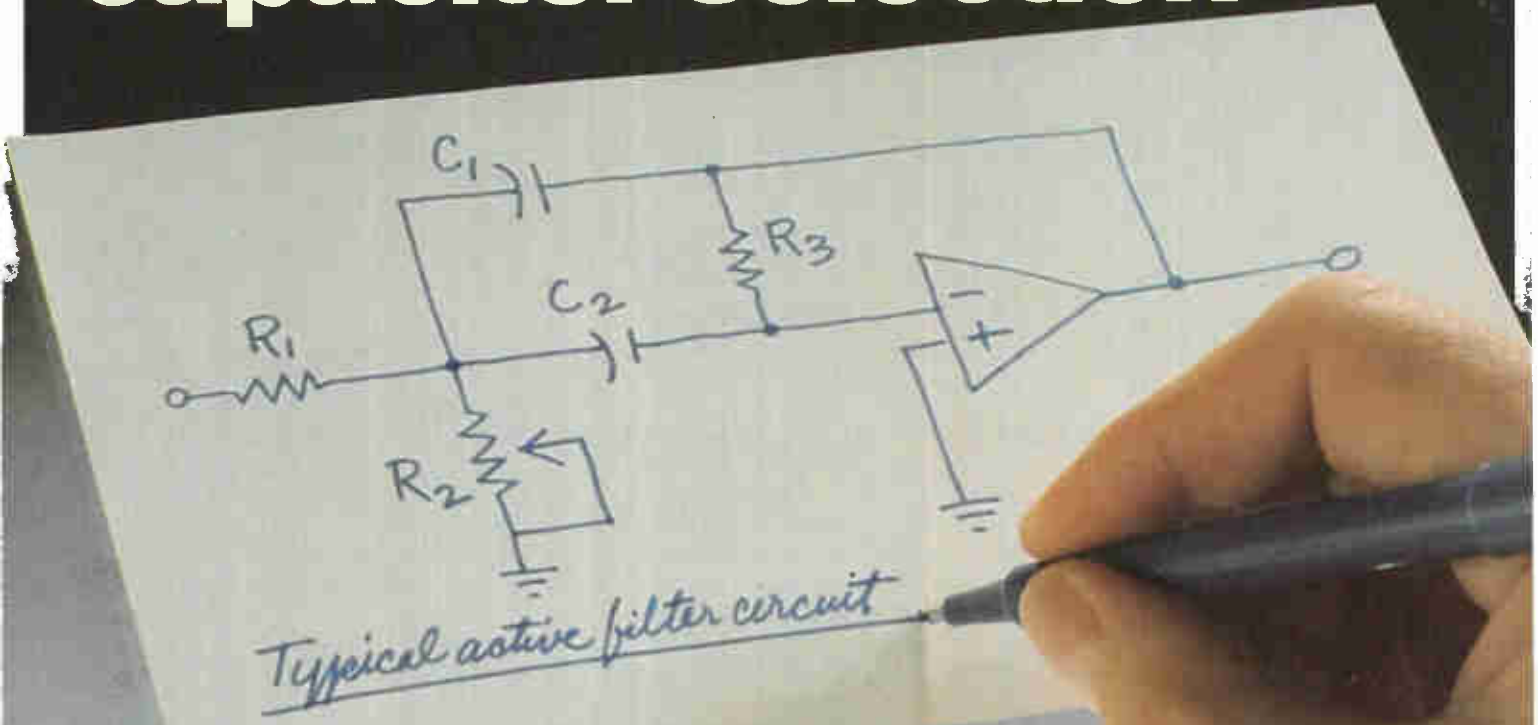
Smaller yet. The System/23 is too expensive to be the personal computer many industry analysts were expecting from IBM. Those analysts, unflagging in their efforts to anticipate IBM's moves, now predict that the personal computer at between $3,000 and $4,000, reputedly code-named Chess, will be unveiled in the middle of August. While current small systems from the industry big guns do not quite reach into the price-performance range where they could challenge the personal computer leaders, such as Apple Computer Corp., Tandy Corp. and Commodore Business Machines Corp., this new one expected from IBM probably will.

In addition to the Venture Development projections, there are various other size and growth-rate estimates of this market. However, there is no consensus on the definition of the systems included in the market estimates. *Electronics* foresees a $1.2 billion market for desktop computers in 1981, growing to $3 billion for 1984. Xerox Corp. predicts that the market will grow at the heady rate of 50% to 60% per year for the next 5 to 10 years, reaching $9 billion by 1985. Creative Strategies International, San Jose, Calif., projected in April of this year that shipments of small-business computer systems selling for $5,000 to $20,000, tallied in units, will grow at a rate of more than 38%, compounded annually, over the next five years. □

A way with words. Hewlett-Packard's 125 desktop computer system manipulates words and pictures as well as numbers.

On station. For less than $10,000, small-business operators can now have a computer—with a printer—from IBM.

Tradeoffs in capacitor selection



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Next decision: compatibility between capacitor and resistor. The selection of nominal R&C values must be based on a compromise between what is permissible and what is available. Resistors are nearly fixed in size for a given wattage rating with only small variations between technologies. Capacitors grow in size with increasing value. Film capacitors are naturals for these applications and values from .01 to .1 MFD are typical.

To "fine tune" the filter, you should also consider the effects of temperature on the network. The temperature coefficients mainly affect the center frequency and bandwidth of the filter, so matching or controlling T.C.'s are important for high performance.

Keeping the temperature range as narrow as practical keeps variance low, so be realistic. Also watch out for nonlinearity on T.C. curves. Few components are truly linear. Again, plastic film capacitors are typically used. Type X463UW metallized polycarbonate and polysulfone types are used in "zero" T.C. schemes; X1263UW polystyrene types for compensating applications.

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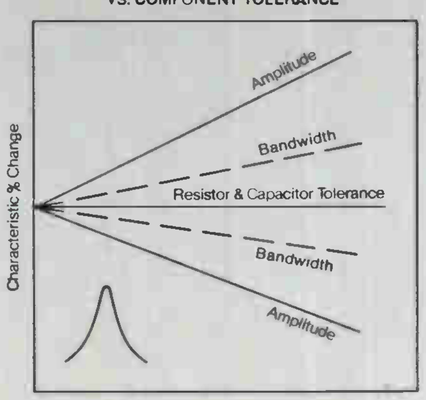

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Industrial electronics

Factory controllers get smarter

Systems with units in a distributed-processing configuration are taking on key roles in manufacturing

by Gil Bassak, Industrial/Consumer Editor

The programmable controller, once a lowly cousin of computer-based process-control systems, is rapidly evolving into a key component of tomorrow's factories. "Looking back 10 years, we've gone three orders of magnitude in programmable controllers," notes Odo J. Struger, who as director of engineering at Allen-Bradley Co.'s Programmable Controller Systems division is responsible for keeping his Highland Heights, Ohio, plant at the cutting edge of the changes.

That evolution has spawned a considerable market, one that has been growing 30% annually. Allen-Bradley estimates programmable controller sales for 1981 will reach $300 million in the U.S. and $500 million worldwide. In 1985 the figures should grow to $900 million and $1.8 billion, respectively, says the company.

The driving force behind such systems is the emergence of communications networks linking separate intelligent control sites—in effect a distributed-processing system. Sometimes these systems have a central computer, but often they use local intelligence to supervise the network.

At the Modicon division of Gould Inc., a chief rival of Allen-Bradley, a line of new automated factory building blocks is being introduced to maximize the power of controllers in running transfer lines, machine tools, robots, and other motion controls. Other modules can write system status reports, perform floating-point math, and supervise the manufacturing process.

Based in Andover, Mass., Modicon also unveiled in May a communications network called Modway, which should do for factories what local nets like Z-Net and Ethernet promise to do for offices. It is capable of transmitting data at a rate of 1.544 megabits per second and uses a token-passing scheme to assign commands to primary devices separated by up to 15,000 feet on the line [*Electronics*, March 10, p. 33]. It is also geared toward network management and control with the inclusion of built-in diagnostics, on-line troubleshooting, and a network monitor that simplifies the task of collecting information and statistics.

Polling place. Programmable controllers linked by a network to this single factory controller report the status of 11 injection molders.

An earlier system, Allen-Bradley's Data Highway, is a data-communications network linking up to 64 stations on a single shielded twisted pair as long as 10,000 ft. With it, programmable controllers, minicomputers, and programmable RS-232-C–compatible devices and peripherals, each located up to 100 ft from the main trunk line, can communicate at the system's 57.6-kilobit/s rate. This lets machinery function independently under its own progammable controllers, while the entire manufacturing line is coordinated by automatic communications between the control systems.

Getting there. Not all manufacturers have taken the full step of integrating a system of controllers in order to coordinate a manufacturing facility. But most are looking into this trend for the next round of products [*Electronics*, Feb. 28, 1980, p. 171].

For example, at Struthers-Dunn Inc. in Bettendorf, Iowa, plans are being made to expand the top-of-the-line Director 4001 programmable controllers to include supervisory control over small units through an expanded input/output port.

A word of caution comes from another manufacturer. "Users are not ready to exploit the technology of the data highway," says Ken Jannotta, a marketing manager at the Eagle Signal Industrial Systems division of Gulf & Western Manu-

facturing Co. Yet his Davenport, Iowa, firm is working on just such a system, he notes. It currently sells a multiple serial port and software packages to enable its controllers to communicate with other units.

Allen-Bradley's Struger is optimistic about what distributed process control can mean for the role of the programmable controller in future factories. "Distributed control is a key to factory automation—tying the whole factory together in a hierachial tree of control," he says.

That other components will be needed to complete the picture of an automatic factory controller has not escaped the attention of manufacturers. Both Allen-Bradley and Modicon plan to sell motion-control equipment to controller customers.

GE is coming. General Electric Co. has made it known that it intends to participate heavily in the controller market as a supplier of components. "When you consider the issues of maintainability, you find there is a need for a general-purpose controller that can change its characteristics easily," says Vincent A. Lytle, an industrial application manager at GE's Programmable Control division in Charlottesville, Va.

GE also has its own version of a data network option for tying controllers to machines and to each other throughout a factory. It is dubbed a data-processing unit; Lytle says that it can "store recipes [for food processing, a typical application], assembly programs for robots, and production information in its 256-K-byte memory. In addition, it offers a number of programmable, serial ports as well as a message-generation feature."

Lytle's comments get at the reasons for programmable controllers' appeal. Unlike the minicomputer-based process-control system, the programmable controller uses a simple programming scheme that evolved from the early days of relay ladder diagrams. In contrast, minicomputer systems require that the operator be fluent in a process-control language, and this complication tends to alienate the factory technician or electrician.

But the differences between the two systems runs deeper. The process-control computer is event-driven; when there is an error signal or a changing variable like vat level or temperature, the program reacts to stabilize the process. Any sequence of events may occur in a process, and rarely in the same order. This variety can make troubleshooting difficult, since all combinations of outputs are possible.

In sequence. On the other hand, the programmable controller is a sequential device. Input and output lines are scanned in a fixed order; and, although more sophisticated controllers have added branch and jump routines to the sequencing, the overall control tends to occur in a more ordered way. As a result, a network of intelligent controllers, tied with factory equipment along a data network, tends to be easier to build and maintain.

The tradeoff, however, is speed. Event-driven systems usually respond faster than sequential setups—but the use of faster processors in a programmable unit is beginning to narrow that gap.

Besides using data highways and the latest 16-bit processors like the 8088 and 8086, makers are tapping other technologies. Currently, the most important new technology being eyed is fiber optics, which offers noise-resistant electrical isolation between controller and machine.

Here Struthers-Dunn has led the way with a fiber-optic option to its high-end controller, the Director 4001. Others are wary of the difficulties in splicing fibers and the loss associated with fiber links; yet there is much interest in surmounting these shortcomings.

Allen-Bradley is conducting experimental prototype work for one customer. Struger says the company is very interested in fiber for point-to-point links "where splicing is not needed and noise immunity and electrical decoupling is." He feels "we haven't mastered all the details" for minimizing the losses associated with splicing fiber.

At Eagle Signal, Jannotta says, "We tested fiber optics two or three years ago and decided we could use it. If some one wanted it, we could install it." □

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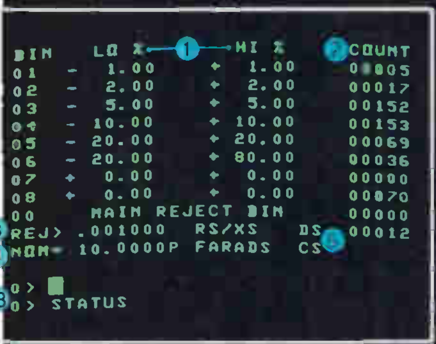

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Letter from Colorado

Colorado keeps eye on growth

Rocky Mountain State's desire to preserve natural beauty makes electronics companies attractive newcomers

by J. Robert Lineback, Dallas bureau

When it comes to recruiting business to Colorado, the attraction is purely natural: towering mountains, clear springs, fresh snow, and white-water rapids. And the powers-that-be plan to keep it that way by maintaining a long-standing vigilance against the spoils of industrialization.

While this guard has all but closed the door to many industries, it has also caused a frenzy of electronics activity in the Rocky Mountain State. In the high country, electronics firms top the list of desirable environmentally clean businesses.

Still in the early stages of growth, the Colorado electronics community already is the home of Inmos Corp., NBI Inc., and Storage Technology Corp., as well as a major manufacturing site for such firms as Hewlett-Packard Co., Honeywell Inc., TRW Inc., IBM Corp., Texas Instruments Inc., Ford Aerospace & Communi- ... are both planning to begin mass production of 64-K random-access memory chips this year.

During the next four years, the number of jobs in the state's electronics industries is expected to grow at an annual compounded rate of 24.4%, states a recent American Electronics Association study. That compares to 14.8% for California, 18.7% for Massachusetts, 16.8% for Texas, and 9.4% for New York. Another industry report being prepared for the state legislature estimates that Colorado electronics payrolls have more than tripled since the mid-1970s.

For the most part, large workforces are not what companies and communities are looking for here. What they are looking for is a place to attract talent. Inmos, the British-government–financed semiconductor company, located its headquarters in Colorado Springs because it is easier to draw top professionals from both east and west, says Richard L. Petritz, chairman.

"I'm a very firm believer in the superstar concept. You've got to get the top people to start up a company like Inmos and survive. To get the very best people, you've got to be ... knew we had to recruit people from Silicon Valley, but why didn't we want to go to California? Just open a newspaper out there, and you'll see it's loaded with want ads," he says with a confident smile.

The story was the same at the new United Technologies Microelectronics Center in North Colorado Springs. "We considered several locations, including Dallas, but I know how hard it is to recruit people away from California. And many top people in the East don't want to go to the West Coast. So, this was the best place to bring people from east and west," notes Gordon Hoffman, general manager of the center.

Old timers. The state has also been good to long-time electronics residents, like Hewlett-Packard, which in 1960 opened its first Colorado operation north of Denver in Loveland. Currently, HP is in the process of moving its Telecommunications division from Mountain View, Calif., to Colorado Springs. That will make the sixth HP division in the state.

Other electronics firms are joining the Colorado land rush. Many are staking claims for future plant sites. The heaviest activity centers around Boulder and Colorado Springs. Although most firms are encouraged to locate facilities in flat-land industrial parks, many hold out for panoramic views near the mountains. "These electronics firms are concerned about recruiting highly skilled personnel. So they feel they must provide a monument for them to work in," says Donald L. Snod-

to tighten the reins on business growth. Fourteen years ago, Boulder created an open-space program, which purchases land with the intent of preserving its natural character, as well as controlling business and residential development. So far over 10,300 acres have been set aside as green belts in the Boulder Valley area. In addition, Boulder has limited growth through a formula restricting the number of building permits and other business licenses.

Broken dreams. Thus, despite the lure for electronics firms, relocation attempts don't always end happily. Four months ago, Systems Development Corp. of Santa Monica, Calif., canceled plans to move its headquarters and 4,000 jobs to the Boulder area. An avalanche of protests was generated when the firm announced last year that it planned to locate a campus in a designated green belt. The company went to local government for backing, but the city refused to bend.

"I think that at first many are stunned that they are not solicited. A lot of corporations are used to coming into an area and people just beating themselves to death trying to help them out," says Clayton Johnson, president of the Boulder Chamber of Commerce. "We encourage them in Boulder, but they have to jump through quite a few hoops. I know that a lot of companies find that to be unusual, but want to see whether they can start jumping through the hoops."

But the flurry of electronics activity has also heightened competition for technical workers. Many companies are quickly finding out that scenic plant locations alone are not enough, explains Richard Payne, an electronics headhunter for Snelling & Snelling Employment Service in nearby Englewood. "That's a difficulty we have had in the Denver area," he notes. "But some companies are beginning to change some of their perceptions. Until a year ago, many felt that they had enough to offer with location—near the Rocky Mountains. Often, relocation packages, benefits—and pay—were not as good as in other states." □

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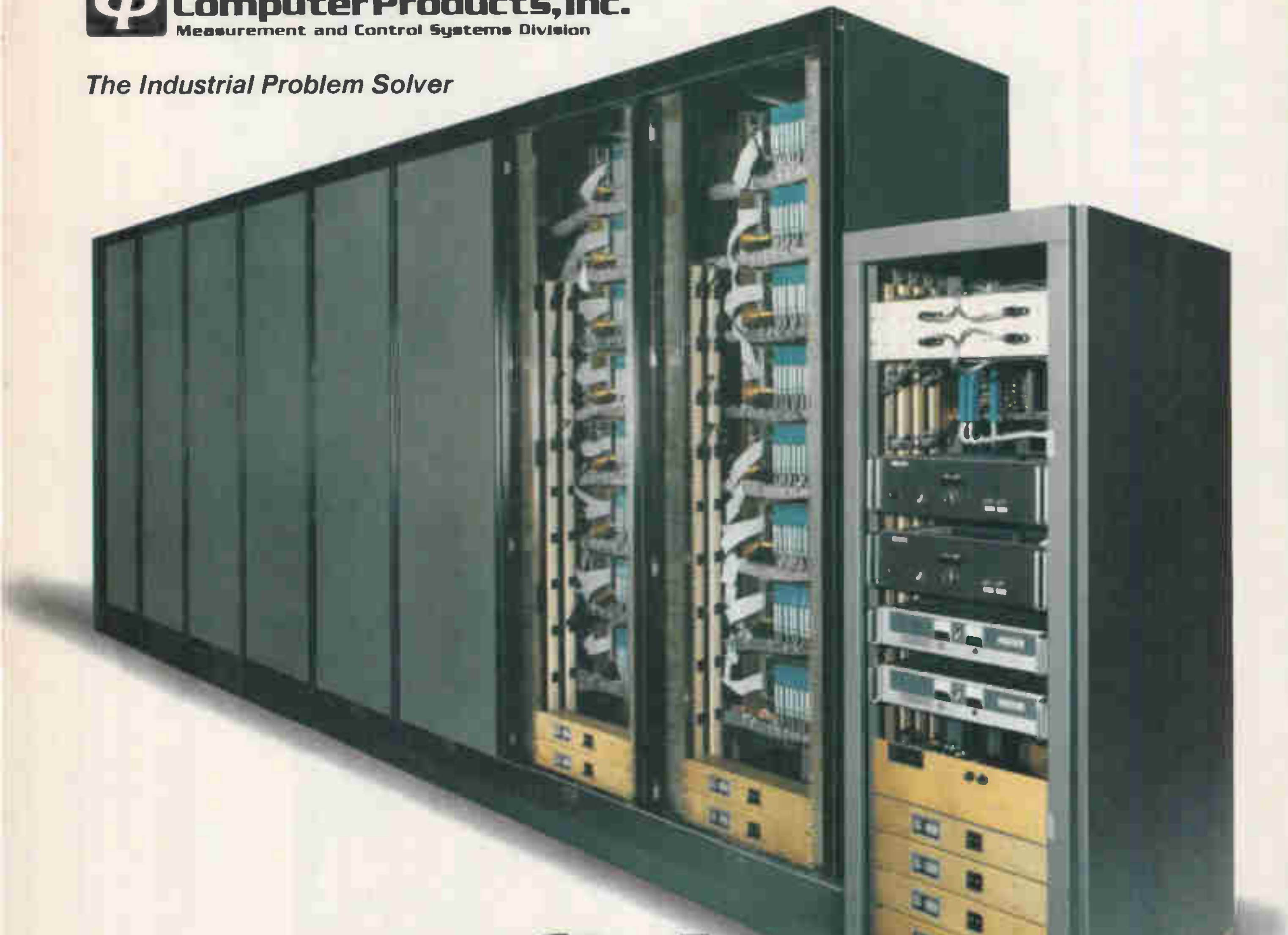


confidence up front

Digital VLSI breeds next-generation TV receivers

Processor chips work with control computer to handle digitized video, audio, and deflection signals

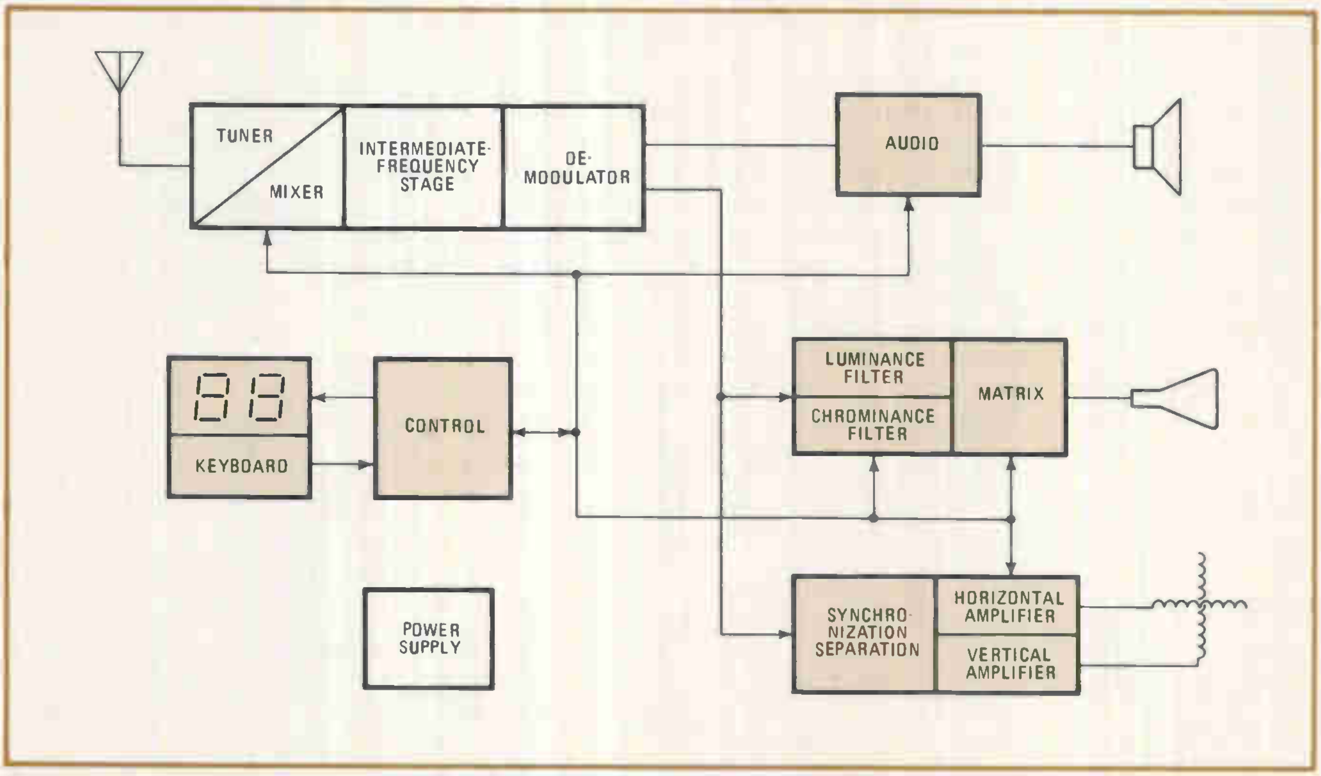
by Thomas Fischer, *ITT Intermetall GmbH, Freiburg, West Germany*

☐ Digital video is no longer a pipedream: by early 1982, the first building blocks for a digital television receiver will enter the market, opening new possibilities for low-cost manufacturing and enhanced TV performance. Hundreds of discrete components now used to process the video, deflection, and audio signals will be replaced by processor chips for each function and by an integrated control computer for orchestrating the transfer of data between them.

At the moment, a complete set of digital integrated circuits for processing the TV signals has been fabricated consisting of both large-scale and very large-scale ICs. The VLSI components contain between 30,000 and 50,000 gate equivalents—each gate equivalent averaging about 4½ transistors.

Besides the reduction in assembly costs won by using fewer parts, set makers will realize further savings in automated alignment procedures. To automate the coil and potentiometer tweaking required in aligning analog TV receivers would take costly tooling, but in digital receivers the task would be simply to enter alignment data into a programmable memory. What's more, feedback from critical test points would update the alignment information as the set ages.

The consumer will also benefit from other performance improvements. The next-generation, mostly digital TV sets will mark a giant advance toward the promise of a fully digital video delivery system: unsurpassed picture quality in transmitted signals, as well as in signals produced by video-disk and -tape players, free from



1. Binary baseband. Radio and intermediate frequencies in a TV receiver are too high to be processed economically by present-day analog-to-digital techniques. Thus, digitization is limited to the baseband portions of the signal path (color).

ghosts, flutter, and noise. Even a partially digitized receiver will facilitate the addition of features like simultaneous dual-channel reception (a picture within a picture) and image-frame storage. Another advantage will be easier interfacing with the emerging home data networks and videotex services. There are, however, limits on what can be digitized within a TV receiver. The present technology for converting between analog and digital signals does not always match the speed, bandwidth, and resolution needed for video signal processing. As a result, the current set of digital building blocks under development is confined to the baseband audio, video, and deflection signals, leaving the radio- and intermediate-frequency stages analog (Fig. 1).

What goes digital?

To analyze which of the data-processing chores of a TV set can be digitized is to address two related considerations: bandwidth and resolution. The Nyquist theorem states that the sampling frequency for a signal must be twice its bandwidth. Otherwise higher frequencies would reappear in the lower region of the frequency spectrum—a phenomenon called aliasing. In practice, TV signals, which require a video bandwidth of less than 5 megahertz and an audio bandwidth of less than 15 kilohertz, can be economically digitized.

Resolution is a function of the signal's dynamic range and fixes the number of bits into which the signal is resolved. If a digital value is represented by n bits, the allowable dynamic range is 2^n, or 6n decibels. The resolution is therefore $1/2^n$, with a residual uncertainty, or inherent noise in the system, of $\pm 1/2^{n+1}$, or $\pm 1/2$ the least significant bit.

The first step in deciding which signals can be digitized is to find the required resolution for the video, audio, and deflection synchronizing signals. Experience has shown that it takes 8 bits to represent a video signal, and further analysis leads to the conclusion that 6 bits fulfill all the requirements for color processing. High-fidelity sound processing requires 14 bits, although acceptable sound can be achieved with 12 bits. Finally, for deflection processing, the limit of recognizability on a TV screen is about 0.1 millimeter of horizontal displacement, corresponding to 10 nanoseconds in a TV with a 26-inch screen. With 64 microseconds per horizontal sweep the resolution is achieved with 13 bits.

The next step is to digitize only those signals low enough in frequency to be converted economically. The range of the transmitter signal entering a TV tuner is from 40 to 1,000 MHz—clearly beyond economical analog-to-digital conversion techniques. The received signal (which carries the composite signal for video and synchronization and the audio signal) is shifted in frequency by mixing it with a local oscillator frequency, and the resulting intermediate frequency is around 40 MHz.

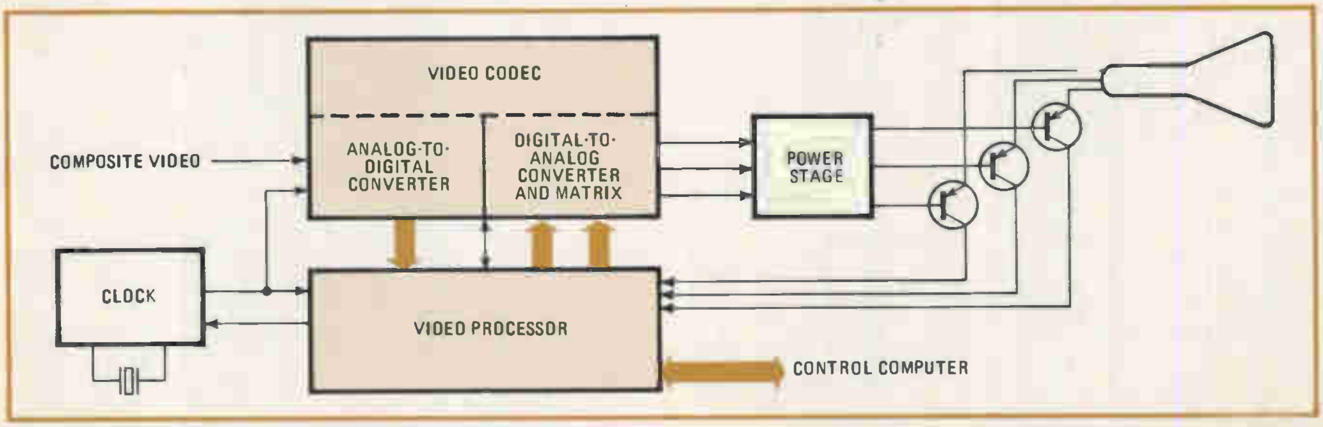
Monolithic a-d converters with 8-bit resolution can digitize such signals, but they cannot yet be produced at consumer equipment prices. So the a-d converter is placed after the video demodulator, where the output is a normalized signal of about 2 volts and band-limited to less than 6 MHz.

The frequency-modulated audio intercarrier is 5.5 MHz in the PAL standard, 6.5 MHz in the Secam standard, and 4.5 MHz for the NTSC standard. With the wide dynamic range of the audio signal, digitization before demodulation is difficult because of the 12-bit resolution needed. Therefore the audio a-d converter is placed after the sound demodulator.

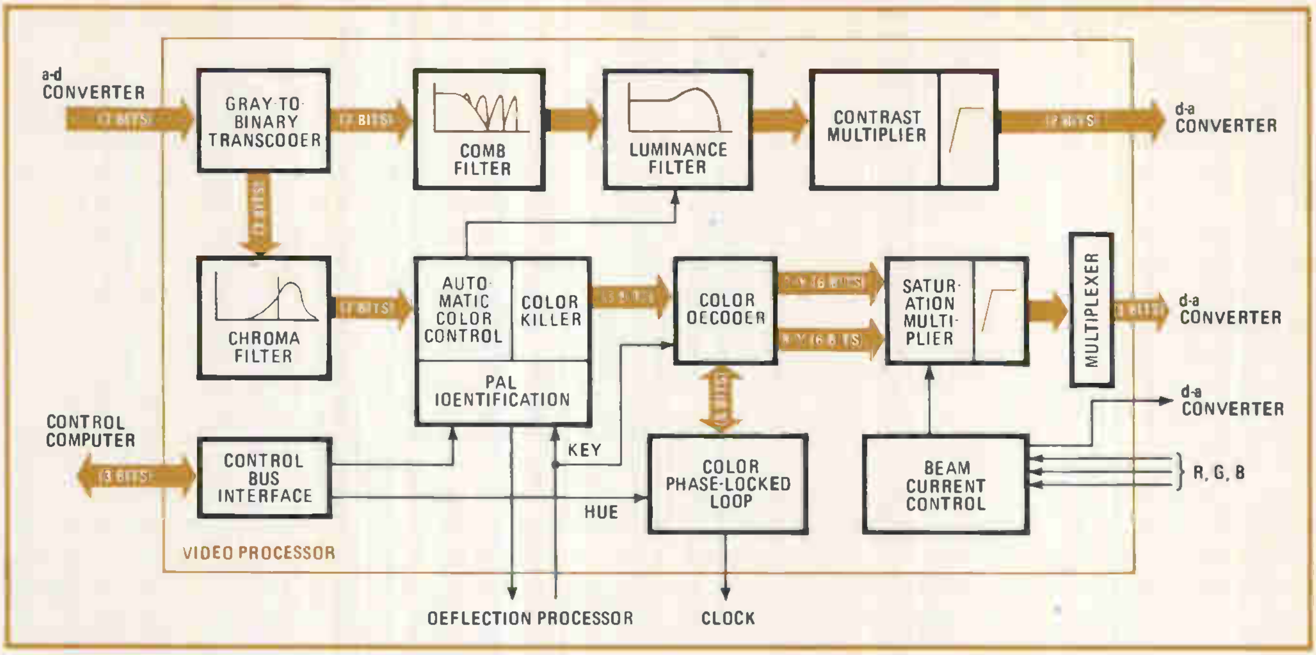
Reconversion, too

Of course, the results of the digital signal processing in the TV receiver have to be converted into analog signals and amplified to drive the speakers, the picture-tube guns, the horizontal stage, and the vertical deflection coil. The most economical way to accomplish this is to use pulse-width modulation in conjunction with a class D (switch-mode) amplifier.

Here again bandwidth and resolution impose limitations, and the choice must be made between faster but more expensive R-2R ladder networks and the slower, less expensive pulse-width modulator. For the audio and deflection circuits, pulse-width modulators suffice; but video, with its need for higher definition, uses a monolithic integrated R-2R ladder network as a d-a converter.



2. Video chips. In the video-signal section of the TV receiver, the composite signal is digitized in a codec and sent to the video processor for filtering and decoding. Then the signal is converted into analog form again and sent to the electron guns via a power stage.



3. Processor peek. Inside the video processor chip, the digitized composite video is separated into chroma and luminance paths, both of which are processed using digital filtering techniques. A feedback loop from the color guns automatically adjusts the beam currents.

In the video section of the digital TV (Fig. 2), wide-bandwidth a-d and digital-to-analog converters are combined onto one bipolar chip called the video codec. The a-d converter is a flash type employing 2^n comparators in parallel, n being the number of bits—a design that puts a high premium on reducing the number of bits and therefore the number of comparators.

As a result, a method was devised to achieve 8-bit resolution of the video while using an a-d converter with only 7 bits of resolution. This is done by biasing the reference voltage of the a-d converter during every other horizontal sweep by a voltage corresponding to half the least significant bit. This scheme converts a luminance value in the middle of two 7-bit steps into the lower value during one sweep and into the higher value during the next sweep. The two values are then averaged on the screen by the eye of the viewer, giving the impression of tones that are resolved to 8 bits.

For this application, the comparators in the a-d converter have gray-encoded outputs to eliminate glitches that might otherwise appear as a result of different comparator speeds. Once digitized, the video data is routed to the video processor (Fig. 3), where it passes through a gray-to-binary transcoder and goes to filters that extract the luminance and chrominance signals.

Digital filtering techniques are the key to developing IC replacements for the many coils and capacitors usually found in a TV. The digital filters in the video section are clocked at frequencies of up to 18 MHz and comprise delay, adder, and multiplier circuits. In MOS technology, delays are trivial to make and adders are small, but multipliers typically are very large structures. To simplify the multipliers, the filter design (Fig. 4) uses factors with only one bit set to 1, giving multiplication coefficients such as 1.0, 0.5, 0.25, 0.125, and so on. Multiplication with these factors is then easily realized by a shift-and-add circuit.

The luminance filter has a variable frequency response that provides peaking from +6 to −3 dB. Peaking increases the amplitude of the high-frequency content of the luminance signal and thus leads to a sharper picture. The overall amplitude of the luminance signal is set by a contrast multiplier, the output of which is limited by clipping and then passed back to the converters in the video codec.

Complicated chroma

Because of the modulation of the color subcarrier, chroma processing is more complicated than luminance processing. First the chroma signal is amplitude-controlled by the automatic color-control circuit. The ACC keeps the amplitude of the burst reference signal at a preset level, thus maintaining a constant color saturation independent of variations in the i-f filters. It also actuates the color killer for monochrome signals and, where necessary, the PAL identification circuit.

From the color killer, the chroma data is then fed to the color decoder. Here color information is extracted from a pair of difference signals which use the blue (B), red (R) and luminance (Y) voltages. In NTSC and PAL systems, the color subcarrier is amplitude-modulated with the B−Y and R−Y signals at phase angles 90° apart. In Secam, the color subcarrier is frequency-modulated with B−Y and R−Y in alternating horizontal sweeps.

It is worth noting here that an expensive glass delay line, required for the PAL and Secam systems, is replaced by blocks of random-access memory on a chip area of only 3 square millimeters (4,600 square mils) each—an excellent demonstration of the advantages of digital techniques in color TV sets. The delay line necessary for PAL color demodulation is used to realize a comb filter in NTSC sets. Such a filter is highly desirable, since the bandwidth is less than 5 MHz with the NTSC system, compared with 6 MHz in the PAL and Secam systems.

Both PAL and NTSC receivers require phase-synchronous demodulation of the color subcarrier, and any phase error leads to an error in hue (for NTSC) or reduced color saturation (for PAL). This demodulation is achieved by phase-locking the sampling clock (the system clock) and the color burst (the phase reference sent by the transmitter).

To the phase lock

The phase locking is done by comparing the sampled B−Y signal with the R−Y signal of the burst. The difference (B−Y)−(R−Y) is a direct measure of the relative phase difference between the burst and the sampling clock and is used to adjust the color decoder's voltage-controlled oscillator, whose frequency is four times that of the subcarrier. Hue is controlled by biasing the comparison of (B−Y) and (R−Y).

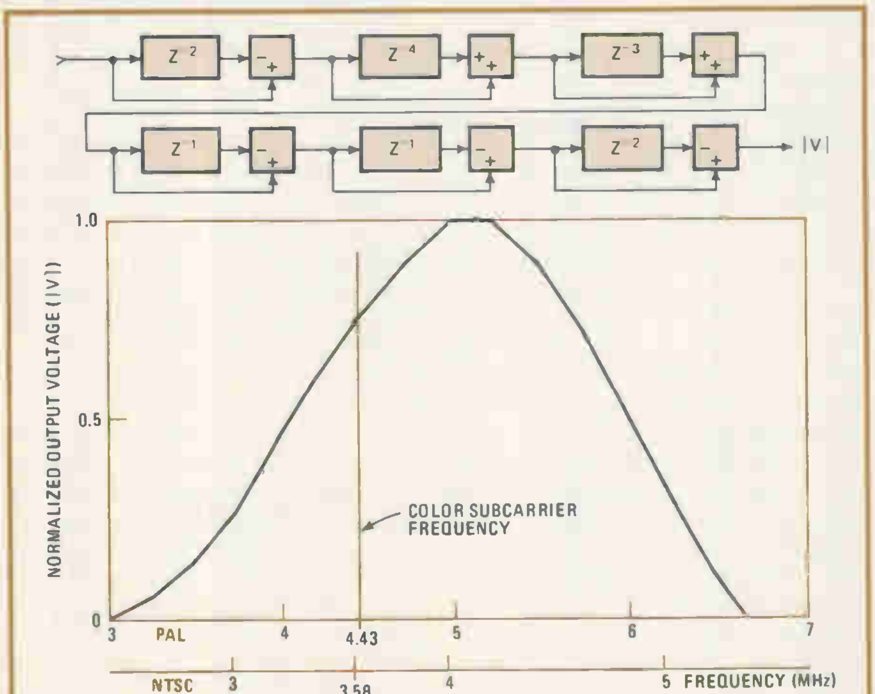
The Y, B−Y, and R−Y signals are routed back to the d-a converters on the video codec. These converters are made from R-2R ladder networks, and the analog signals are dematrixed into the red, green, and blue signals. From there, amplifiers drive the external video output stages, which in turn drive the color guns of the picture tube.

Black and white reference levels are set by the gain and bias of the buffer amplifier and controlled by the video processor—which monitors and adjusts the beam current automatically to the levels set at the factory, thereby maintaining performance regardless of aging. These effects are slow but require a certain amount of computation, so it is convenient to use some of the computing power of the control computer. The three beam currents are sampled continuously and the black and white levels are tested during the video frame flyback, at which time test signals are sent out by the video processor.

The output of the video a-d converter carries the horizontal and vertical synchronization information, as well as the luminance and chroma data. The deflection processor (Fig. 5) extracts this information and controls the frequency and phase of the oscillators that drive the deflection yoke of the picture tube.

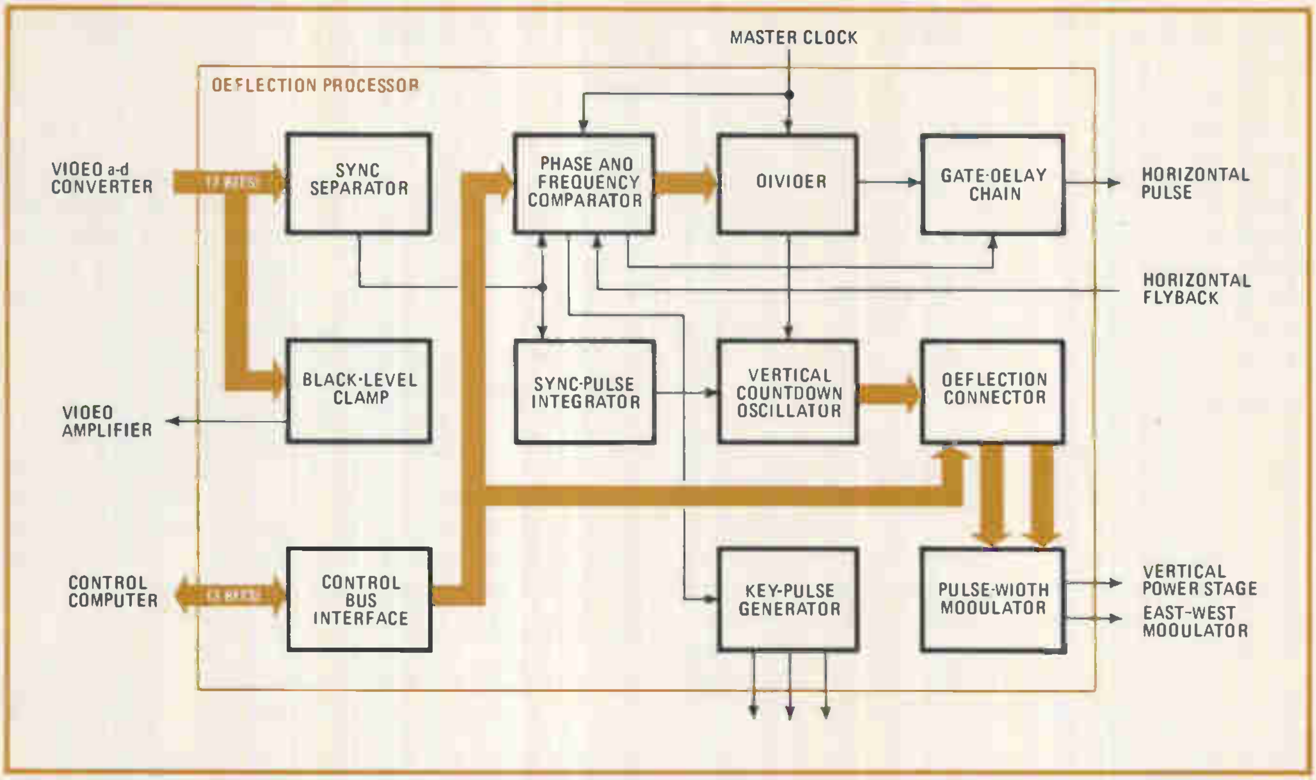
The incoming signal is first processed by a stage that determines the black level of the video signal. The output of this stage clamps the black level to a fixed voltage in the video amplifier so that full use is made of the conversion range of the video a-d converter. The separation level for the sync pulses is the midlevel between black and the top of the sync pulse. In order to eliminate noise and glitches, several sync pulses are correlated and the average of the rising and falling slopes is taken as the reference point for the horizontal oscillator.

In order to keep the correct sweep rate, feedback is taken from the horizontal flyback circuit. A digital phase comparator detects the relative phase between the horizontal flyback circuit and horizontal sync pulse. The comparator controls a frequency divider that counts the



$$|V| = |[(2 - 2\cos 2\omega)^2 (2 + 2\cos 4\omega)(2 + 2\cos 3\omega)(2 + 2\cos\omega)^2]|$$

4. Clever chroma. A typical filter within the video processor uses factors that simplify the multiplication inherent to the filtering process. The chroma filter shown here uses only coefficients of 1 and so reduces the multiplier to simple hardwired shift-and-add circuits.



5. Beam deflection. The deflection processor is responsible for all the timing and synchronization functions in the TV receiver. It receives the digitized composite video signal in parallel with the video processor, separating horizontal (east-west) and vertical triggers.

master clock down to the approximate horizontal frequency (15.625 kHz for PAL, 15.750 kHz for NTSC). The counting down is done to a resolution of a quarter of the period of the color subcarrier (56 ns for PAL, 70 ns for NTSC) because the system clock frequency is four times that of the color subcarrier. This time corresponds to a resolution of 2.5 mm (0.1 in.) on a large screen—clearly not enough since a 0.1-mm resolution is needed.

Therefore resolution is enhanced by a chain of gates that delay the sync pulse by a variable number of gate delays. As a result, the total resolution is increased to one sixteenth of 56 ns, or 3.5 ns. The precise measurement of phase and frequency is done by averaging several measurements. The allowable rate of change of the phase is limited to reduce the susceptibility of the horizontal sync pulse to noise. The time constant can be changed, however, to accommodate signal sources with drifting oscillators, such as video-cassette recorders and video games.

Going vertical

The vertical oscillator is a resettable counter and the reset pulse is the vertical sync pulse. This pulse is gated by three different windows: a large window of ±64 horizontal sweeps for phase acquisition, a small window of ±3 horizontal sweeps for unlocked-mode operation, and a window of zero width for locked-mode operation. The output of this counter is used to compute a PWM signal that drives the vertical power stage.

In addition, an error is introduced by the projection of the beam onto a flat screen and has to be corrected. This correction is included in the algorithm for the pulse-width modulator. The circuitry also computes the correction signal for the east-west, or horizontal, modulator.

Often it is possible to extract horizontal and vertical sync pulses directly from the color subcarrier because large TV networks usually transmit signals with a fixed ratio of the three frequencies ($f_{cs}:f_{hor}:f_{ver}$). When such a signal is acquired, the deflection processor shifts to a locked mode, in which the horizontal and vertical frequencies are derived by counting down the color subcarrier. This makes the deflection signals virtually immune even to excessive noise from a weak signal, to flutter caused by transient events such as airplanes or trucks, and to interference from electric appliances.

Still active

However, even when the deflection circuits are locked into the color subcarrier, the phase- and frequency-comparing circuits are active in the background, constantly checking whether the countdown procedure is still valid and whether the deflection processor should shift back to the unlocked mode. In either case, however, the output of the horizontal stage excites a conventional power output circuit that drives the deflection coils.

Finally, all the information necessary to determine whether the received TV signal is PAL, Secam, or NTSC may be found in the deflection processor. This information can be passed to the control computer, making feasible a true multistandard receiver in one unit.

Three channels of the demodulated audio in the TV receiver are digitized by an a-d converter and processed by a separate audio processor (Fig. 6). This design accommodates stereo sound—already introduced in Japan and coming to all major countries soon [*Electronics*, March 24, 1981, p. 78]. The three audio channels feed three separate sigma-delta a-d converters working in parallel. Each converter consists of two parts, a pulse density modulator and a conversion filter. The output of the pulse density modulator is counted during one sampling interval, and the conversion filter takes a sliding average of the count.

Two goals met

In designing the conversion filter, two goals were set. The first was to maximize the output resolution, and the second was to filter out the noise that is generated by the pulse density modulator. The resulting audio a-d converter provides 14 bits of resolution for the audio section.

Of the three audio channels, one carries the pilot tone indicating the presence of monophonic, stereophonic, or bilingual information on the other two channels. Because it is a weak signal with extremely small bandwidth, filters with a very high Q are required to extract and process the pilot tone. Such filters are difficult to realize with analog techniques but easy to implement digitally. Also, digital filters do not need adjustment for tuning to the correct frequency, because their resonant frequency depends simply on a crystal-controlled clock.

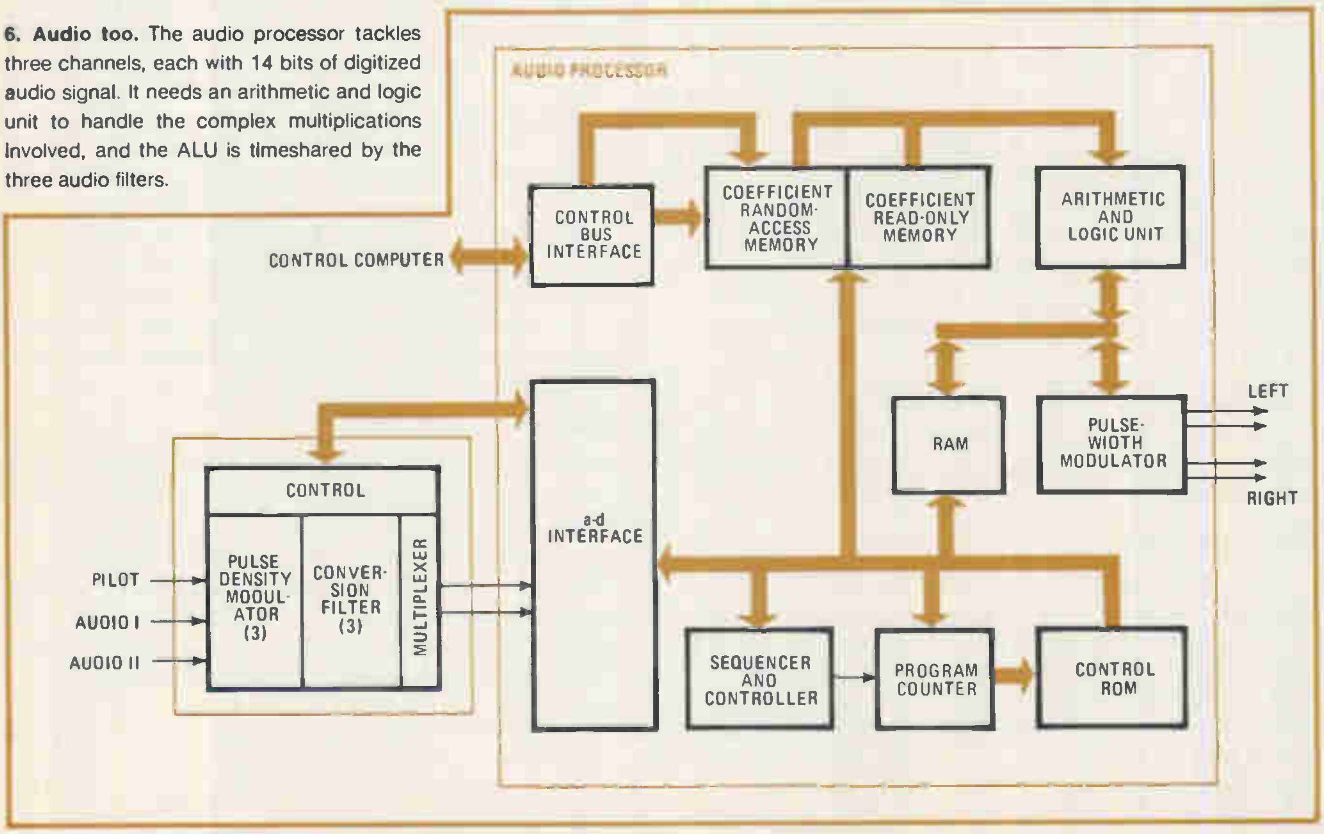
In the audio processor, a long data word and a complicated filter with coefficients varying according to the different settings of the users require a hardware multiplier, rather than the shifters and adders used for multipliers in the video processor. However, a technique is employed that multiplies using only one fast 16-by-8-bit arithmetic and logic unit timeshared for all filters in the subsystem. By adding the necessary registers in the form of RAM and by designing a read-only-memory sequencer, a specialized version of a general-purpose signal processor is achieved for filtering the digital audio. With this architecture, any processing algorithms can be changed by changing only the mask of the sequencer ROM.

The output portion of the audio processors consists of two pulse-width modulators that provide nonoverlapping signals of opposite phase for driving the push-pull transistors of a class D audio power amplifier. The audio processor's serial bus interface allows the control computer to perform all control functions, such as changing filter characteristics or switching from loudness to flat response or from mono to stereo to bilingual.

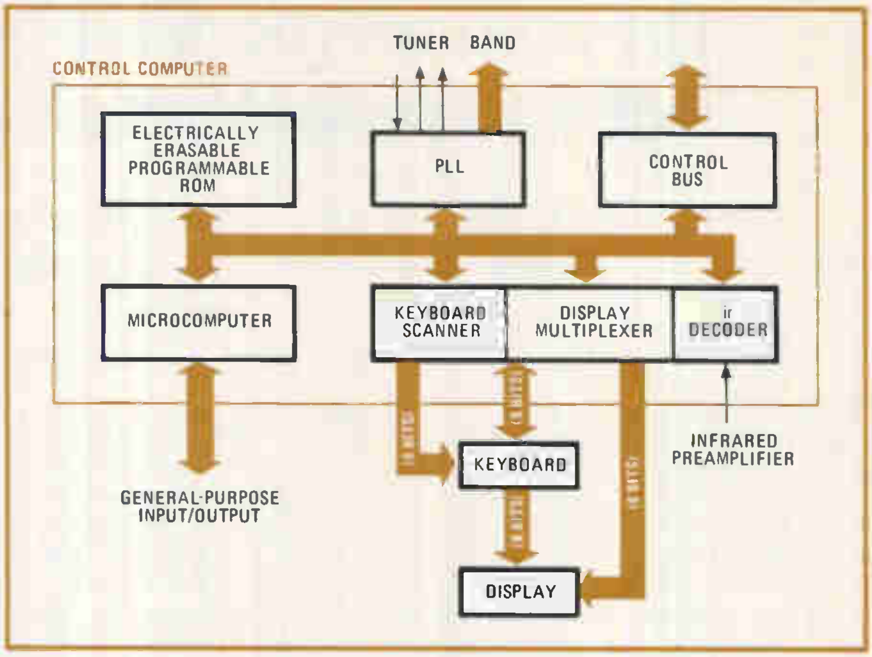
Control computer

The control computer passes operator commands to the three digital processors, as well as providing some adjustments transparent to the user. It combines the flexibility of a microcomputer with the speed and features of dedicated hardware (Fig. 7).

In a TV set with digital signal processing, all analog commands are translated into digital numbers and fed into the signal-processing stages—a natural task for



6. Audio too. The audio processor tackles three channels, each with 14 bits of digitized audio signal. It needs an arithmetic and logic unit to handle the complex multiplications involved, and the ALU is timeshared by the three audio filters.



7. Conductor. Orchestrating data transfers between the processor components is one job of the control computer chip. Since handling user inputs like channel selection and volume is another, the same IC includes dedicated blocks for user commands.

microcomputers. On the other hand, general-purpose microcomputers need additional circuitry for controlling a tuner and receiving the infrared signals of a remote control unit. Thus all these functions are integrated as part of the control computer.

However, the bidirectional bus is controlled by the control computer, with the three digital processors on the bus as slaves. The bus is fairly slow—a transfer of 1 byte of address and 1 byte of data takes more than 100 μs. Inputs from the user are entered on a keyboard or by an infrared remote-control unit.

The tuning system is a phase-locked-loop frequency synthesizer with a minimum frequency step of 62.5 kHz. A number of programmable input/output ports can be used for features such as automatic channel search and indicators other than a seven-segment display.

The control computer also has a role in the self-aligning features of the set where a nonvolatile electrically erasable programmable ROM is the key element. In manufacturing the TV, an assembly-line computer has access to the control computer through the bus. Thus the computer can make adjustments and store the optimum alignment values in the EE-PROM.

In addition, the owner can store favorite channels and individual settings of the analog controls like volume and brightness in the EE-PROM. Finally, the programmability of the control computer offers the possibility of individualizing receivers made by different manufacturers using the same digital chip set.

Once a TV signal is digitized, it is possible to apply digital techniques for a variety of features that are difficult to achieve in analog technology. An example is the comb filter in the NTSC video processor.

Another is ghost compensation, an attractive feature available with digital processing. One compensating network is a transversal filter made from tapped delay blocks, multipliers, and adders, giving a maximum delay of 64 μs. However, perfect ghost cancellation requires more than 200 taps, multipliers, and adders. Although this is not economically feasible today, one reflection from a smooth surface could be eliminated by using one tap and multiplier, and preliminary studies show that 5 to 10 taps are sufficient to compensate for most ghosts.

Since the delay of the ghosts varies from antenna to antenna, electronic switches would change the positions of the taps. A difficult problem, however, is to get an accurate measurement of the ghost. One solution proposed uses the equalizing pulses during frame synchronization as a probe for the ghost's step response.

Avoiding flicker

Another feature is a flicker-free picture—especially useful in Europe, which has a 50-Hz frame frequency, leading to a clearly perceived flicker at high brightness or contrast settings. The flicker is eliminated by storing a full picture that is then read out at a higher frequency than normal. In this way, the frame frequency could be increased to 75 cycles or more.

The ability to digitally store a picture has other advantages. For example, although storing a full picture takes more than 1 megabit of memory using redundancy-free encoding, it is possible to use less RAM to produce a smaller picture-in-a-picture display.

The advantages of digital video extend to TV peripherals as well. Digital recording techniques would vastly improve the performance of the VCRs. Feeding the digital information of a video disc player directly into the digital signal processor of a TV set offers a perfect picture, free of all deficiencies such as noise, distortion, and hue error. Furthermore, with a digital VCR and full picture store, one gets still-picture, slow-motion, and zoom functions for free. □

On-chip stereo filter cuts noise without preprocessing signals

A pair of dynamically variable low-pass filters reduces noise with no encoding of signal sources

by Martin Giles, *National Semiconductor Corp., Santa Clara, Calif.*

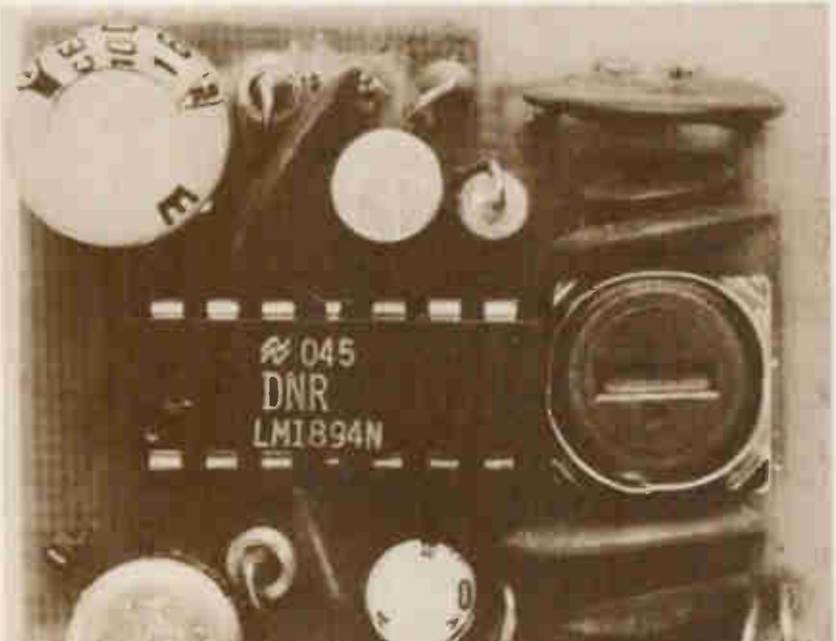
☐ A new weapon is available in the war against audio noise, an integrated circuit that provides designers of consumer equipment with a noise-reduction system that works with any audio source without preprocessing of the program material. Because the heart of the system is an IC, the new approach is a cost-effective solution to noise problems.

The DNR dynamic noise-reduction system [*Electronics*, March 24, 1981, p. 110] takes a substantial bite—up to 14 decibels—from the overall noise figure for a multitude of audio sources. It does so by continually adjusting its filtering bandwidth to the varying harmonic content of the input signal.

The DNR technique combines two audio phenomena—bandwidth reduction and auditory masking—to achieve its results; for this, it relies heavily on dynamically variable, integrated low-pass filter circuits. By integrating all but a handful of noncritical components, National Semiconductor's designers have made DNR economically justifiable for audio equipment makers, who must respond to consumer demands for high performance and competitive prices.

The popularity of consumer audio equipment, particularly the cassette tape recorder, is due in part to the development of what are called complementary techniques for suppressing noise, notably the Dolby technique. A common drawback of such noise-suppression systems is that they require program material to be encoded before recording or broadcasting—as a result, a wealth of material does not benefit from these noise-reduction techniques. The DNR approach, however, is a noncomplementary, or single-ended, method for reducing audible noise and so is applicable to a multitude of sources, including older tape recordings, fm broadcasts, video disk players, and video cassette recorders.

Crucial to the low cost and therefore to consumer acceptance of DNR is the LM1894 dual-channel noise-reduction chip. In Fig. 1, the IC is surrounded by a few additional components needed to build a full DNR system. The chip itself contains two dynamically variable low-pass filters that reduce unwanted hiss and noise by varying their bandwidths as a function of the high-frequency content of the input signal.



1. Noise stopper. A single LM1894 audio filter chip and a few noncritical components are all that are needed to complete the DNR dynamic noise-reduction system.

In the past, consumer noise-reduction systems have been modeled after compandors designed primarily for use in recording studios. Companding, for compressing and expanding, is a complementary technique in which a recorded signal is encoded so that its low-amplitude, high-frequency sound components are boosted by as much as 10 dB (in a Dolby B system) in a process called compression—it effectively compresses the dynamic range of the sound.

During playback, the amplitude of these same high frequencies is expanded by the same 10-dB amount in order to restore the original sound dynamics. In the process, tape hiss,

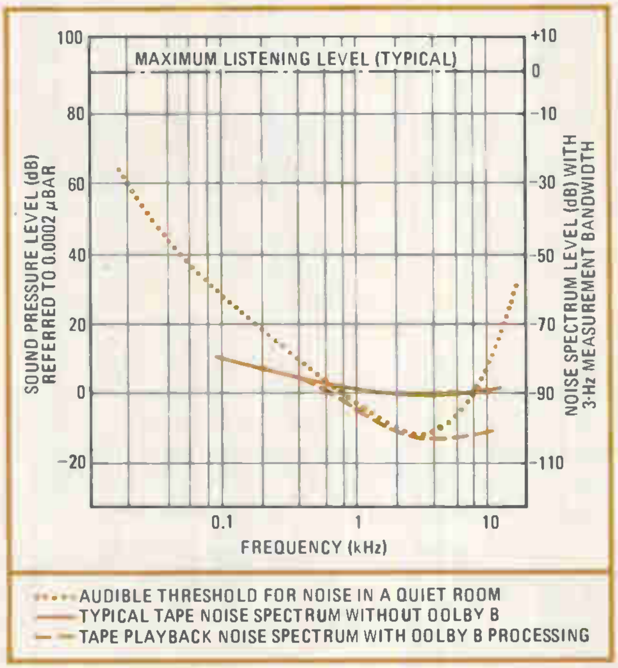
10 decibels does the trick

In commercial recording studios, compression-expansion systems, or compandors, offer substantially more than 10 decibels of noise reduction. Why didn't Ray Dolby go for more than 10 dB in his now-famous system? The chief reason is that 10 dB is usually sufficient, and this applies to any consumer noise-reduction system.

In the curves of noise spectrums in the figure, the dotted audible-threshold curve is the spectrum level at which the noise becomes just audible in a fairly quiet room. Noise components below this curve will not be heard. The curve's shape is due to a phenomenon known as masking—the fact that the ability to hear a sound is reduced by the presence of other sounds, called maskers. Below 600 hertz and above 6 kilohertz, the shape is determined largely by the characteristics of the human ear. But between these frequency limits, the hearing threshold is masked or raised by ambient noise.

The noise level produced by an audio system depends largely on the volume control setting. If a recorded 0-VU (volume unit) signal level can be amplified enough that the speakers can produce a sound pressure level of 90 dB at the listening position—pretty loud—then a typical cassette tape's noise spectrum appears as shown by the solid curve. Between 1 and 6 kHz, the room noise does not mask the tape hiss.

The result of Dolby processing is shown in the dashed curve: tape hiss is reduced below the audible level. Turning up the volume control or recording the tape at a reduced mean level of −10 VU will shift the tape noise spectrum up, and tape hiss becomes audible again. So to say that a 10-dB noise reduction is enough is only part of the story. However, anything more than a 10-dB compression will make the Dolby-encoded tape unplayable on equipment without the complementary decoding circuits. The DNR dynamic noise-reduction approach skirts this problem and gives a 14-dB noise reduction because it is noncomplementary—in other words, it requires no processing at the audio source.



which is a high-frequency noise component, is pushed 10 dB lower. Although that noise reduction may not appear to be much, it is enough to give the cassette tape player respectability in the consumer high-fidelity marketplace (see "10 decibels does the trick," above).

Unlike commercially available compandors, a single-ended system does not need prior encoding and can remove noise already present in the source, not merely prevent the recording tape from adding more noise. Radio broadcasts, VCR and video-disk sound, and conventional audio tape can all be processed with a single-ended system. Furthermore, a noncomplementary system adds no compatibility constraints to the source material. In contrast, a new Dolby C technology—essentially two cascaded Dolby B systems—gives an 18-dB compression during recording that is incompatible with the 10-dB expansion of playback equipment containing Dolby B circuitry.

Staying single

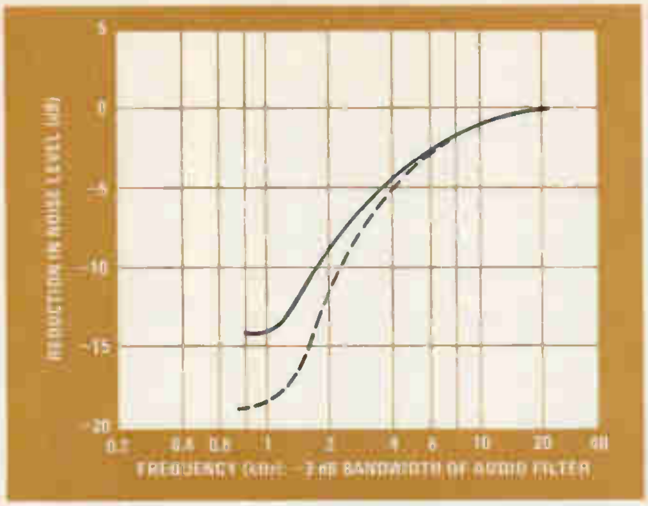
The first audio principle that a DNR system exploits is the relationship between the output noise level and the audio system bandwidth: if the system's bandwidth is decreased, the aggregate noise level is also decreased. For a noise spectrum that has a uniform average amplitude, such as white noise, the aggregate noise voltage is proportional to the square root of the bandwidth. Using Nyquist's formula, it can be shown that if the bandwidth is reduced from 20 kilohertz to 800 hertz, the noise voltage decrease (in decibels) is:

$$20 \log_{10}(20\times10^3)^{1/2} - 20 \log_{10}(800)^{1/2} = 13.98 \text{ dB}$$

Catching the noise

Typically a noise spectrum will not be uniform in amplitude over the frequency range, and so noise is not equally annoying at all frequencies. Therefore, the DNR IC includes a weighting filter in the control section. Since the ear is most sensitive to noise in the frequency range of 600 Hz to just over 6 kHz, it is in this range that DNR works to keep the bandwidth at the minimum required to faithfully reproduce the source material. Using the CCIR/ARM (International Radio Consultative Committee/Average Responding Meter) weighting method, the noise reduction shown in Fig. 2 for both single and two-pole low-pass audio filters is up to 14 and 18 dB, respectively.

The second principle behind DNR is that of acoustic masking, which exploits the ear's ability to mask noise (see again "10 decibels does the trick," above). The DNR system's masking produces a reduction of perceived noise as the signal frequency varies from 800 Hz up to the full 20 to 30 kHz required for high-fidelity transmission of the music. When no audio is present, the filter closes



2. Doubling up. The −6-dB/octave rolloff at the high end of each audio filter is sufficient to reduce noise in most cases (a). Cascading the two filters gives additional noise reduction (b) where the faster (−12-dB/octave) rolloff is tolerable.

down to its minimum cutoff frequency, 800 Hz.

Because of the characteristics of the ear, the most effective masking frequencies are around 1 kHz, although higher frequencies do mask neighboring noise spectrums. Both music and speech have large amounts of energy in the 1-kHz region and will provide for excellent noise masking. The spectral envelopes in Fig. 3 are typical and will vary depending on the particular instrument and the pitch and loudness with which it is played.

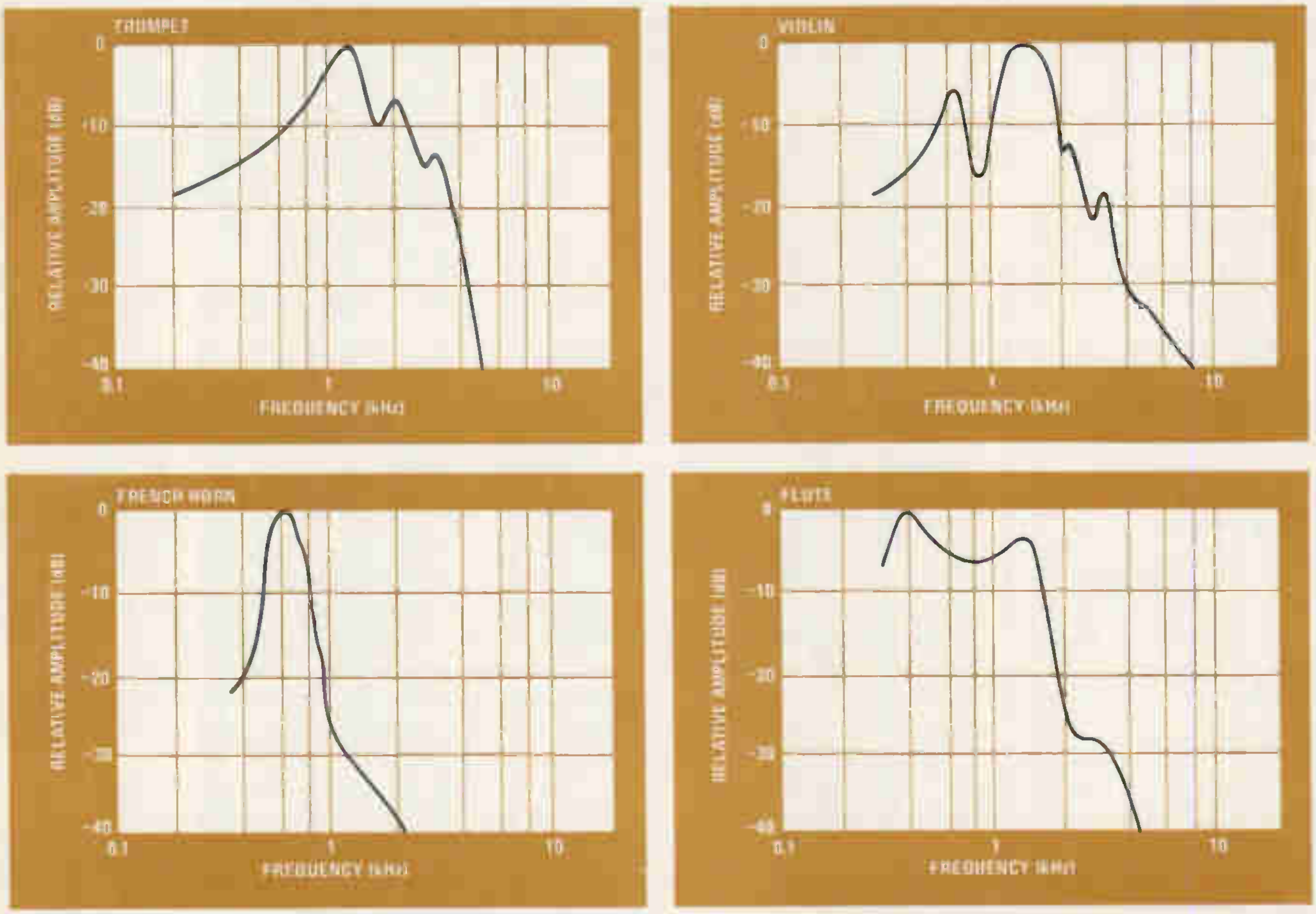
To take a worst-case situation, a French horn can have a lot of energy below 1 kHz, but has very little above. If the DNR system were to respond to this high amplitude below 1 kHz, it would open up its bandwidth to 30 kHz to provide for unobstructed passage of the rest of the music. But in this case, there is no high-frequency sound, and thus noise from, say, 2 kHz upward would be unmasked and audible.

Instead, by responding to the 1-kHz or higher frequency content of the signal, a DNR unit produces only a slight increase in bandwidth depending, in this case, on the loudness of the French horn. The music comes through, but noise above 2 kHz remains suppressed. Furthermore, audio signals that possess energy levels at higher frequencies induce correspondingly wider filter bandwidths.

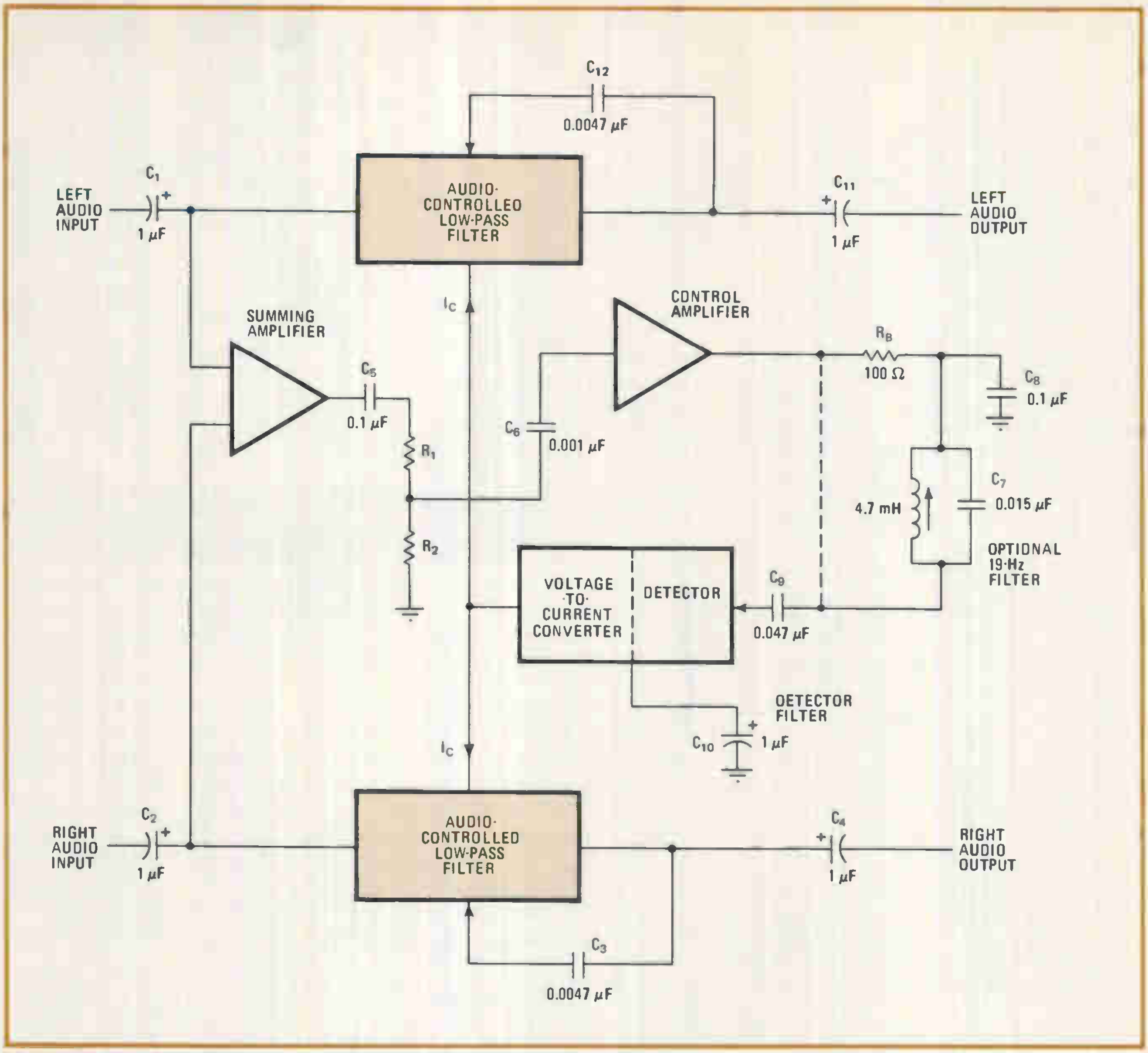
Frequency the key

Put another way, when detecting the presence of higher-frequency energy, it is assumed that much larger energy levels exist simultaneously at the lower critical masking frequencies. So the bandwidth can always be increased to ensure fidelity along the audio path.

If the mean signal-to-noise ratio of a source is above 30 dB, a single-ended system can provide noise reduction



3. Musical mix. With most musical instruments, as well as speech, energy is bunched in the vicinity of 1 kHz. This spectral characteristic is fundamental to the masking principle by which DNR operates, since the most effective masking frequencies are around 1 kHz.



4. Variable filter. The LM1894 contains twin variable-bandwidth low-pass filters that dynamically track the audio signal's frequency content. A third filter in the control and amplifier responds to the occurrence of higher audio frequencies by widening the audio bandwidth.

with no audible impairment of the music. For cassette tapes recorded at the 0 VU (volume unit) level, a dynamically controlled low-pass filter can give a perceived S/N ratio of better than 65 dB.

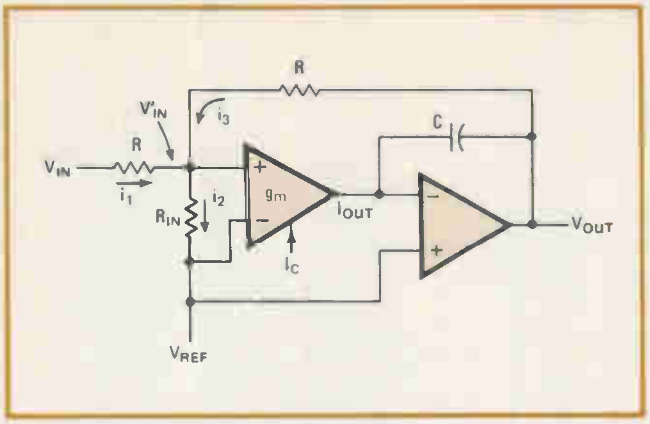
Inside the LM1894 (Fig. 4), the bandwidths of twin audio filters—one for each stereo channel—are adjusted by a control section, which is driven by the audio source. The control section consists of summing and control amplifiers, a high-pass weighting filter, and a detector circuit with a current source output controlling the pair of low-pass audio filters.

Both low-pass filters (Fig. 5) are inherently well matched since they are integrated on the same chip. They show no undesirable parameter shifts, such as peaking or slope changes as the bandwidth is increased, and special efforts have been taken to avoid audio-path dc offsets caused by the control signal. Each filter has a flat response below the −3-dB cutoff frequency and a smooth single-pole roll-off at higher frequencies.

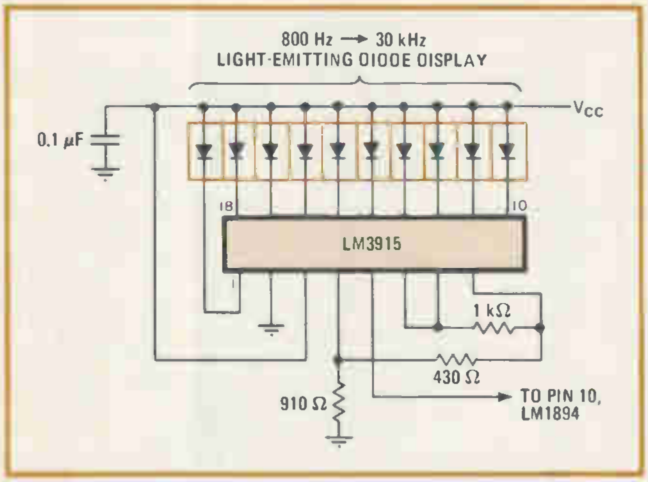
A −6-dB-per-octave slope at the high end of the filter produces the most satisfactory results with modern and classical music possessing a wide frequency range. Steeper slopes are achieved by cascading both audio filters in a single LM1894. This produces a −12-dB/octave slope for a potential noise reduction of 18 dB.

The control circuitry uses a high-pass filter with a −3-dB corner frequency at 6 kHz and a −12-dB/octave roll-off slope. The weighting filter is designed to optimize the dynamic bandwidth in response to the masking properties of the source material (Fig. 6). In addition, a 19-kHz notch is optional to suppress the pilot carrier present in stereophonic fm broadcasts.

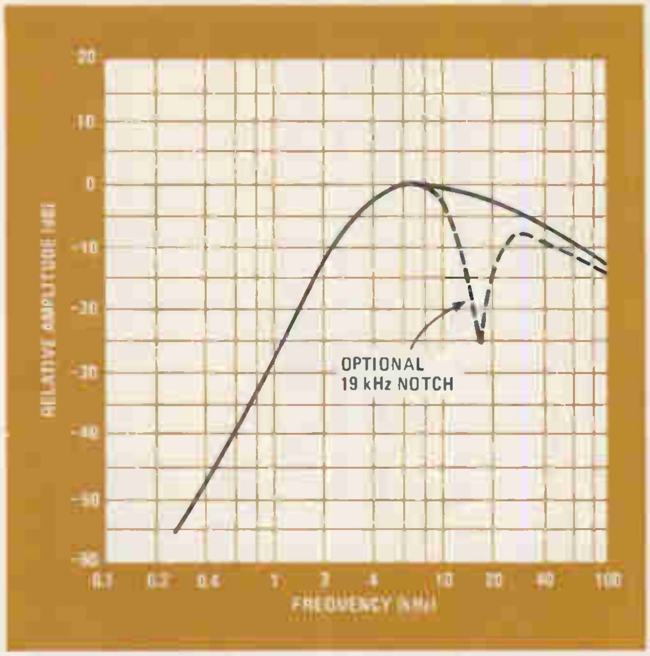
Capacitors C_6 and C_9 in Fig. 4, working with the IC's internal resistance, produce the −12-dB/octave slope and the 6-kHz corner frequency. A third filter formed by coupling capacitor C_5 and the control amplifier's gain-



5. Variable filters. Each of the DNR chip's low-pass filters is based on a variable transconductance amplifier driving an operational-amplifier integrator. Its transfer characteristic resembles that of a single-pole RC filter where R has been replaced by K/g_m.



7. Add-on. A visual indication of the audio bandwidth may be continually displayed by this circuit when wired to the detector circuit of the LM1894. This is especially useful when the DNR system is used as an audio add-on and fitted with an adjustable control-path gain.



6. Controlling curve. The DNR filter control response to frequency indicates a sensitivity to frequencies above 1 kHz, so that high-amplitude, high-frequency signals are most effective in opening the audio filters to their maximum bandwidth.

setting resistors R_1 and R_2 provides a further roll-off at 1.6 kHz to prevent activation of the filters by extremely high-amplitude, low-frequency energy like drum beats.

The control-path design also is optimized for transient response. If the detector did not respond to the leading-edge transients in the music, distortion would occur from the initial loss of high-frequency components caused by the audio filters opening up too slowly.

As might be expected, the rise time of any musical selection will depend on the instruments that are being played. For example, an English horn is capable of reaching 60% of its peak amplitude in 5 milliseconds. For other instruments, rise times can vary from 50 ms to 200 ms, while a hand clap rises in 0.5 ms. With this in mind, a typical application of a DNR system uses an attack time of 0.5 ms in order to minimize any loss of high-frequency transients.

Attack time is only half of the transient response picture, however. Once the detector has responded to a musical transient, it needs to decay back to the quiescent output level at the end of the signal. If the decay is slow, the audio bandwidth will be wide following a transient, and a noise burst is heard. On the other hand, if the bandwidth decreases too rapidly, a loss of musical ambience occurs because the harmonics lasting beyond the large-amplitude signal will be suppressed.

Experience has shown that an exponential decay is best suited for the bandwidth reduction in order to preserve the harmonic amplitudes. The ear cannot usually respond in less than 150 ms to low-level noise following a large signal. So the DNR design makes use of a decay characteristic that falls to within 10% of its final value in 50 ms.

An accessory

When the DNR chip is built into audio equipment, the control path gain is set by the ratio of resistors R_1 and R_2. These resistors have been selected on the basis of the noise floor of the input signal. However, the DNR system can be used equally well as an external audio accessory, since it is designed to process audio at normal line input levels—such as those of a separate cassette deck. In this case, the resistors should be replaced with a potentiometer so that, depending on the audio source, adjustments can be made to the control path gain.

In practice, the capacitor of the detector filter can be monitored to help determine the gain necessary for the source noise to start opening up the audio filter bandwidth. A light-emitting diode or complete IC bar graph (Fig. 7) can provide a visual indication of circuit operation or a continuous display of the audio bandwidth.

Adding a switch to bring the detector input of the LM1894 to +5 volts will force the audio bandwidth to 50 kHz irrespective of the signal input. This switch permits bypass of the DNR function as well as rapid adjustment of the sensitivity to ensure that the music quality is unaffected by circuit operation. □

Building quality analog circuits with C-MOS logic arrays

Design techniques can turn digital complementary-MOS components into low-power, high-performance linear systems

by Richard Kash, *Mountain View, Calif.*

☐ Complementary-MOS logic arrays are an increasingly popular approach to cost-effective semicustom digital integrated circuits. And where performance is not key, the complementary transistors of C-MOS can also be configured into current sources, amplifiers, and so on, for low-power analog circuits. There are, however, ways that digital metal-gate C-MOS arrays can deliver high quality as well as low power to analog and combined analog-digital ICs.

All digital systems require some analog circuit functions, ranging from internal voltage regulators to analog-to-digital converters for interfacing with external devices such as sensors or controllers. Integration of these components on the same chip with digital circuits increases system reliability and cuts system size and cost compared with multichip designs.

Developers of metal-gate C-MOS arrays succeed in combining analog and digital systems that consume mere microwatts of power on a single chip. Detailed analog design data, kit parts, and a computer-aided design capability will soon be generally available, enabling users to design and lay out circuits on their own and take advantage of the great flexibility offered by combined analog-digital ICs.

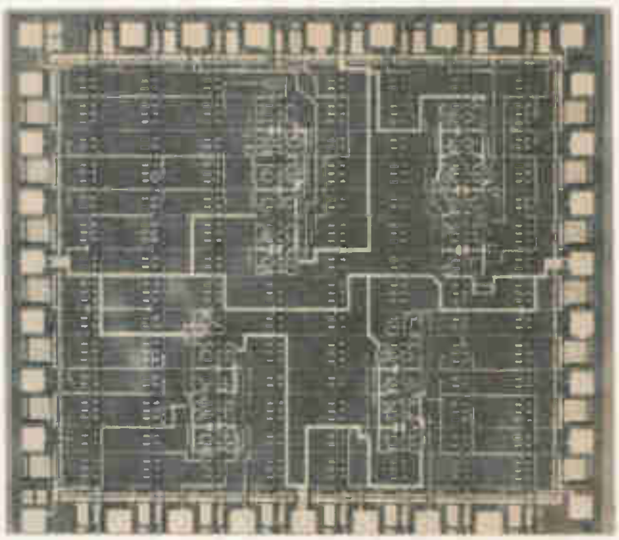
Furthermore, semicustom C-MOS arrays to be introduced in the near future will offer even better performance. Components not currently available—zener diodes, high-value resistors, MOS capacitors—will be included, and transistor geometries tailored for analog designs will yield better circuits with fewer components. Finally, the potential flexibility of MOS gate arrays should open up for the semicustom chip new applications, where unique user needs dictate the circuit configurations.

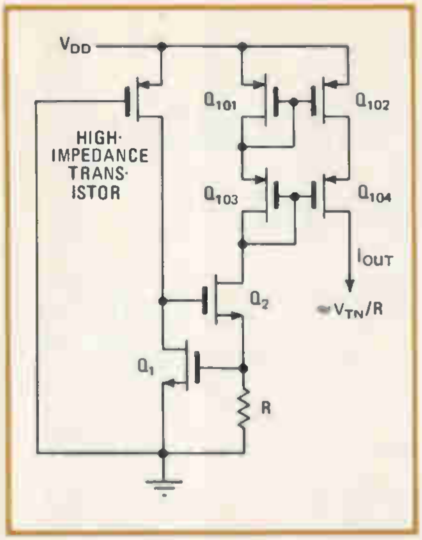
The interior pattern of each chip in a widely available series of metal-gate C-MOS arrays consists of sets of adjacent rows of enhancement n-channel and p-channel MOS array transistors separated from each other by a large number of 800-ohm diffused p^+ resistors designed for the interconnection of the array transistors and for use as linear resistors in analog circuits (Fig. 1). Each row of array transistors is subdivided into electrically isolated cells consisting of either two or three transistors. The smallest chip in the series, the MCA, contains 112 pairs of complementary cells, and the largest chip, the MCD, contains over 350 such pairs.

P- and n-MOS buffer transistors are located on the chip's periphery between pads on two sides. Each buffer transistor has an effective transconductance approximately eight times that of an array transistor. Also along the edges are a few high-impedance, low-current MOS transistors of both polarities. The remainder of the periphery is filled with large n-MOS driver transistors capable of sinking 30 milliamperes. Unlike the array and buffer n-MOS transistors, whose back gates are wired to the circuit's most negative voltage, V_{SS}, each driver has an uncommitted back gate, allowing the transistor to be connected as a floating 5-picofarad capacitor or as a vertical bipolar npn transistor. When the driver is connected as a capacitor, the back gate, source, and drain form one terminal, and the gate is the other. In the vertical npn transistor, the back gate is the base contact, the source and drain are emitters, and the collector is formed by the substrate and is therefore automatically wired to the drain voltage, V_{DD}.

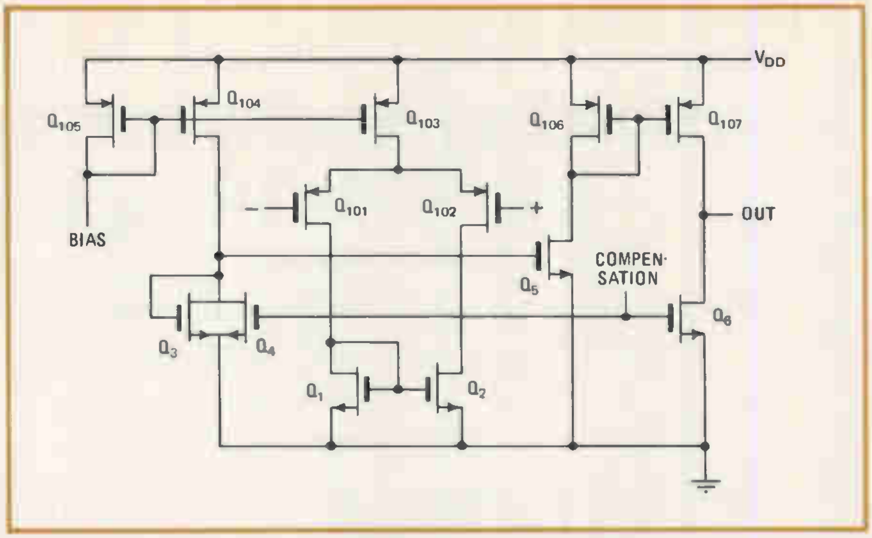
The array components may be combined to produce a wide variety of quality analog building blocks. Circuit complexity can range from a simple current source to a sophisticated dual-slope a-d converter

1. Combination platter. High-quality analog circuits such as the four op amps shown in this die photo are possible on a semicustom C-MOS digital logic gate. The chip is organized as alternating rows of complementary transistors and diffused resistors.





2. Mirror image. This C-MOS version of a popular current source achieves excellent performance by using a cascode current mirror for higher output resistance.



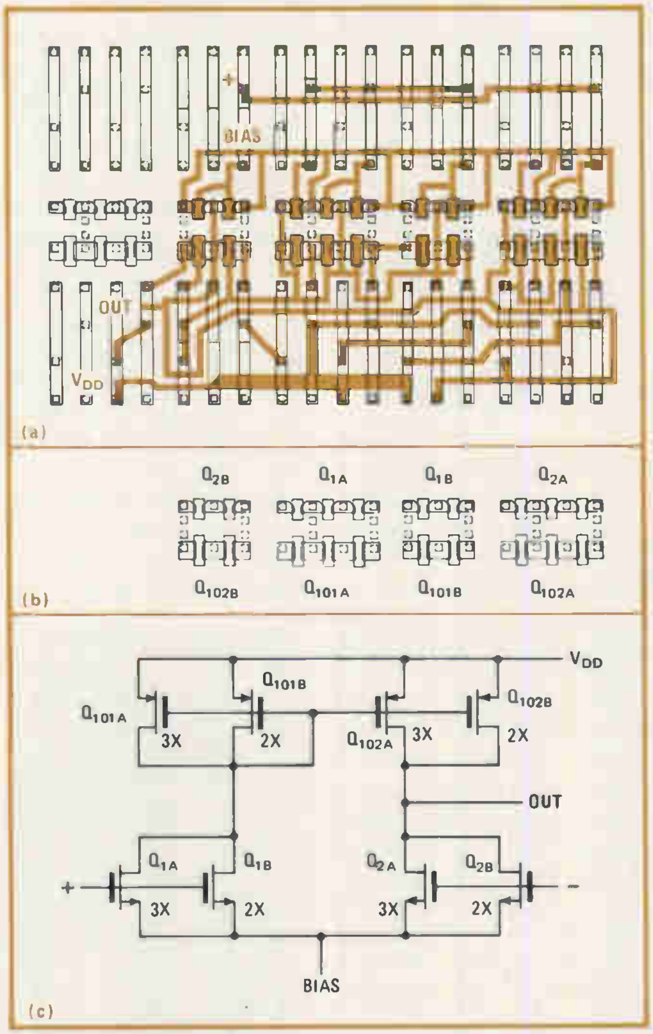
3. Compact amplifier. A standard two-stage op amp is a building block for many analog circuits. In this design, a source-coupled input pair with active loads drives the output stage differentially. Low-frequency performance of the circuit is maintained with a bias current as low as 1 μA. Frequency compensation is required in closed-loop applications.

with automatic offset nulling. Figure 2 shows a supply-regulated current source. Q_2 acts as a feedback transistor to set the gate voltage of the n-MOS driver transistor, Q_1, at a voltage near its threshold value, V_{TN}, corresponding to the relatively low drain current established by the high-impedance transistor. A resistor sets the output current level at V_{TN}/R. The output resistance would be limited to a fairly low value by Q_{102}, if not for the cascode output stage Q_{103}–Q_{104}. These devices shield Q_{102} from changes in the output voltage, significantly increasing the output resistance—the output current change with voltage variations is less than 0.05%/volt, versus 2%/V for a noncascoded current source. The major drawback of this cascode circuit is the reduced output voltage range—both Q_{103} and Q_{104} must remain in saturation if the shielding is to be effective.

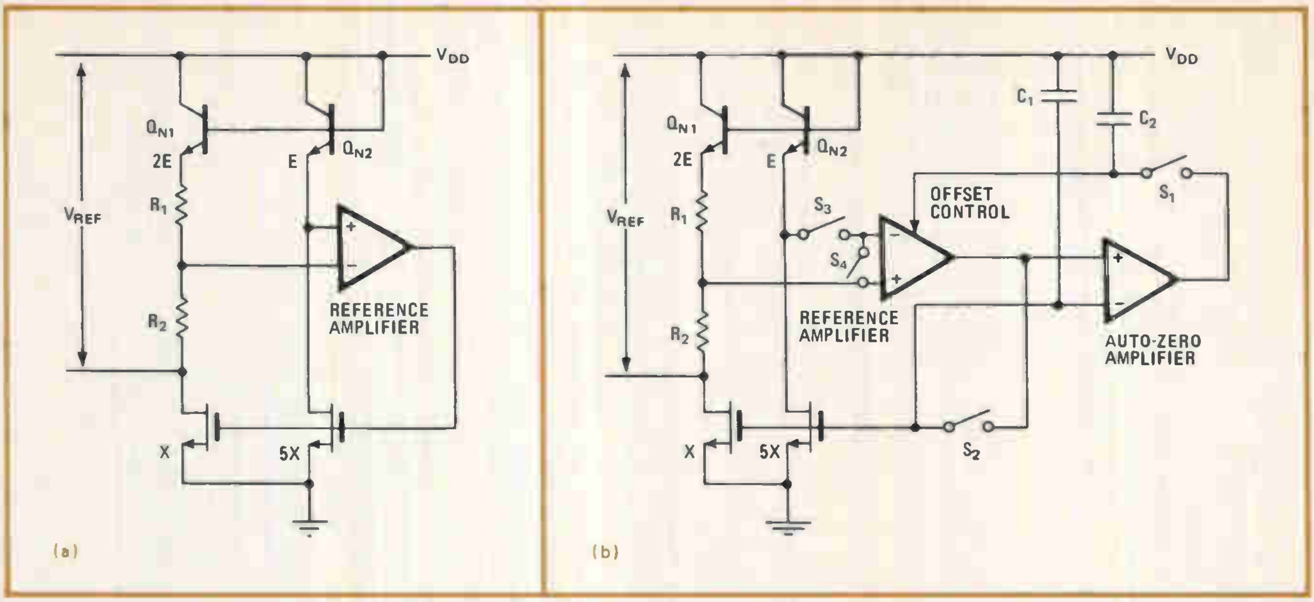
Operational amplifiers

Mirror current sources like this one provide biasing for other circuits, such as operational amplifiers. The two-stage op amp shown in Fig. 3 requires only seven array cells and is capable of fairly good performance. The first stage consists of the differential input pair Q_{101} and Q_{102}, with a current-mirror load formed by Q_1 and Q_2. Q_{103} supplies bias current to the source-coupled pair. The output of this stage at the drain of Q_2 drives a second stage consisting of transistors Q_5 and Q_6 with an active current-mirror load, Q_{106}–Q_{107}. Q_3 and Q_4 invert the signal so that the output transistors are driven differentially. The high-impedance output of the amplifier must be buffered by an output stage to drive a low-impedance load: an n-MOS driver transistor wired as a bipolar npn device can serve as an emitter-follower buffer. The amplifier performs well with a bias current as low as 1 microampere.

At a current of 100 μA, the op amp supplies an open-loop gain of 70 decibels, a respectable unity-gain bandwidth of 2 megahertz, and a slew rate of 7 V/microsecond. The typical offset voltage of 25 millivolts (65 mV



4. Balancing act. The high offset voltage of MOS FET op-amp input stages can be significantly reduced by a layout trick (a): a linear variation of device parameters across a row of transistors (b) is effectively cancelled out by paralleling individual devices (c).



5. Temperature-stable. A bandgap voltage reference (a) with automatic offset nulling (b) balances opposing temperature coefficients to achieve excellent stability over a 40°C temperature range. A feedback loop is used to cancel the reference amp's offset voltage.

in the worst case), which is common for a simple op amp with an MOS field-effect-transistor input, does present some major performance limitations. Using array transistors wired in parallel extends the op amp's current rating but multiplies its share of the chip area as well.

Unconditional stability against oscillation is provided by a 15-pF capacitor (three paralleled driver transistors each configured as a 5-pF capacitor) in series with a 5-kilohm resistor connected between the amplifier output and the compensation terminal. Higher closed-loop gains require less compensation, and none is needed if the amplifier is used as a comparator.

Lower offset voltages may be obtained by incorporating layout techniques that compensate the mismatches in device parameters caused by any linear processing gradient, such as doping variations or lithography misalignment. By cross-coupling individual transistors in a parallel connection, tightly matched input devices can be constructed (Fig. 4). An op amp using such an input stage achieves an offset voltage of 6 mV typically and 25 mV in the worst case.

Increasing the gate area of the input differential pair and decreasing the transconductance of the active loads relative to the input lowers the amplifier's noise voltage. For example, an op amp using driver transistors as inputs and buffer transistors as active loads produces a noise voltage of 70 nanovolts/hertz$^{1/2}$ at 10 kilohertz, compared with 350 nV/Hz$^{1/2}$ for the standard design. This move also increases the common-mode rejection ratio to 80 dB because the back gate of the input device is isolated from all other transistors and can be tied to its source. Shorting the back gate to the source eliminates modulation of the channel conductivity by a changing depletion region width.

Cascoding techniques can be employed to increase the gain of an op amp. A single-stage cascoded op amp has a voltage gain in excess of 1,000 and needs no frequency compensation. The common-mode input range is unaffected, but the output swing is reduced compared with a standard design, since the cascoded output devices must remain in saturation to maintain the high gain. The same techniques applied to a standard two-stage design yield an open-loop gain of more than 250,000.

Two types of repeatable voltage reference have been implemented on these logic arrays—diode and bandgap. Diode references use very little chip area, require no external components, and are capable of a 60-dB power-supply rejection ratio. Unfortunately, they suffer from a large output-voltage temperature drift— −3,300 parts per million/°C—caused by the temperature dependence of the base-emitter junction voltage.

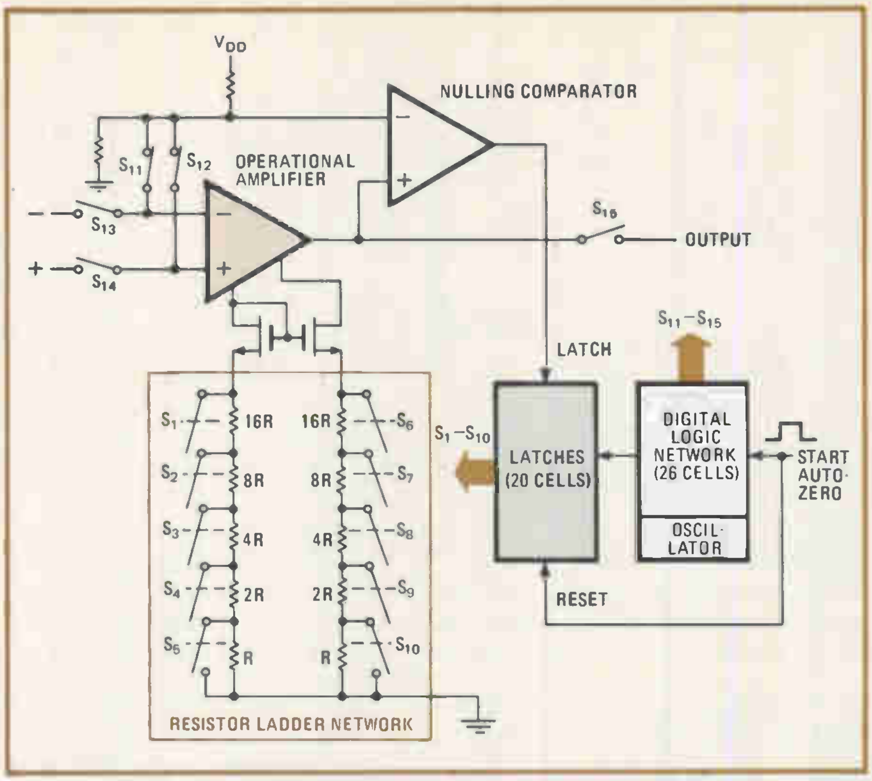
Voltage references

A bandgap reference with automatic offset nulling achieves a worst-case output tempco of 100 ppm/°C and a power-supply rejection ratio of more than 60 dB (Fig. 5). A reference amplifier attempts to maintain equal voltages at the emitter of Q_{N2} and the node joining R_1 and R_2 by forcing Q_{N2} to run at an emitter current density that is 10 times larger than that of Q_{N1}.

The difference in base-emitter junction voltages, ΔV_{BE}, is therefore 60 mV and has a positive temperature coefficient. The output reference voltage (relative to V_{DD}) is $V_{ref} = V_{BEQN1} + (1 + R_2/R_1)(\Delta V_{BE} - V_{os})$, where V_{os} is the offset voltage of the reference amplifier. Since V_{BE} has a negative temperature coefficient, the net variation of V_{ref} can be zero. That happens when both V_{os} is zero and the resistor values are chosen to give V_{ref} equal to the silicon bandgap voltage, 1.25 V.

An automatic offset-nulling loop is required to reduce the errors due to the finite V_{os} of the reference amplifier. When switches S_1 and S_4 are closed and S_2 and S_3 are open, the auto-zero amplifier adjusts the currents in the current-mirror circuitry of the reference amplifier to produce a precise null at its two inputs. When S_1 and S_4 are opened, C_2 holds this control voltage; closing S_2 and S_3 restores normal operation. C_1 holds the gate voltage on the 1× and 5× transistors during auto-zeroing to

6. Digital fix. Analog performance gets a hand from the logic circuits available in a gate array. The balance of the first-stage current-mirror loads is automatically adjusted by a ladder network under digital control to minimize the input offset voltage.



prevent the reference voltage from glitching.

As the previous example illustrates, reducing an operational amplifier's offset voltage is critical for many analog circuits. Figure 6 shows a digital approach to offset nulling that requires no external hold capacitors. The offset voltage is zeroed by opening and closing, under digital control, the appropriate switches (S_1 through S_{10}). The nulling resolution (step size) is determined by the op-amp bias current and the value of the resistors in the current-mirror ladder network. The nulling range is limited to $\pm 2^n(\Delta V_{os})$, where n is the number of switches in each current mirror leg and ΔV_{os} is the step size. With 10 switches and a step size of 2 mV, as much as ±31 mV of initial offset voltage can be automatically nulled to less than 2 mV.

Offset nulling

A start-auto-zero pulse initiates the nulling sequence. This signal could be supplied by a power-on reset pulse, a system clock, or a resident microprocessor. Since the nulling information is stored in digital latches, refreshing is not required as long as the chip's power is maintained. Once auto-zeroing is completed, switches S_{11} and S_{12} are opened; switches S_{13}, S_{14}, and S_{15} are closed; and the amplifier is now a fully differential C-MOS op amp with a low offset voltage.

A C-MOS bandgap reference voltage source has been implemented using this nulling technique. The reference amplifier is auto-zeroed under microprocessor control just before each system measurement that requires a stable reference voltage. The observed worst-case temperature drift of the reference in this system is 100 ppm/°C over the commercial temperature range.

The preceding circuits constitute only a small fraction of the analog designs possible with these logic arrays.* Other circuits that have been tested include a gain-controlled amplifier, a 2-MHz voltage-controlled oscillator, a 555-type RC oscillator, a comparator with programmable input hysteresis, a voltage doubler, a 7-bit resistor-string digital-to-analog converter, and a complete dual-slope 8-bit a-d converter. The complete converter, including on-chip voltage reference, requires less than half of the array cells on an MCD chip, leaving plenty of room for other circuits. Absolute accuracy of the converter over temperature depends primarily on the reference voltage drift and the stability of the ratio of the external input resistors. If the auto-zeroing bandgap reference in Fig. 5 is used, its 100-ppm/°C worst-case drift allows 8-bit accuracy over a 40°C range.

Since the analog functions are implemented at the component level, the circuit designer enjoys great flexibility in both design and layout. A fully custom approach offers more flexibility, but at a higher cost and longer turn-around time.

For example, in a programmable-demand heart pacemaker recently integrated on an MCD, the linear circuitry takes up about 15% of the die area and consists of two op amps, two comparators, and a voltage reference. The remainder of the die is digital circuits and consists of 54 flip-flops and 92 random logic gates. The chip operates down to a battery voltage of 1.5 V, consumes less than 10 μA of current, and runs at a maximum frequency of 32 kHz. The total development time, from the start of breadboarding to the receipt of working prototypes, was 18 weeks. This example demonstrates the considerable reduction in development time from that required for a fully customized chip. □

*Made by Integrated Microcircuits Inc., St. Paul, Minn.; Interdesign Inc., Sunnyvale, Calif.; Master Logic Inc., Sunnyvale; Monosil Inc., Santa Clara, Calif.; and Nitrin Inc., Cupertino, Calif. A similar series is made by International Microcircuits Inc., Santa Clara.

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'Dithering' display expands bar graph's resolution

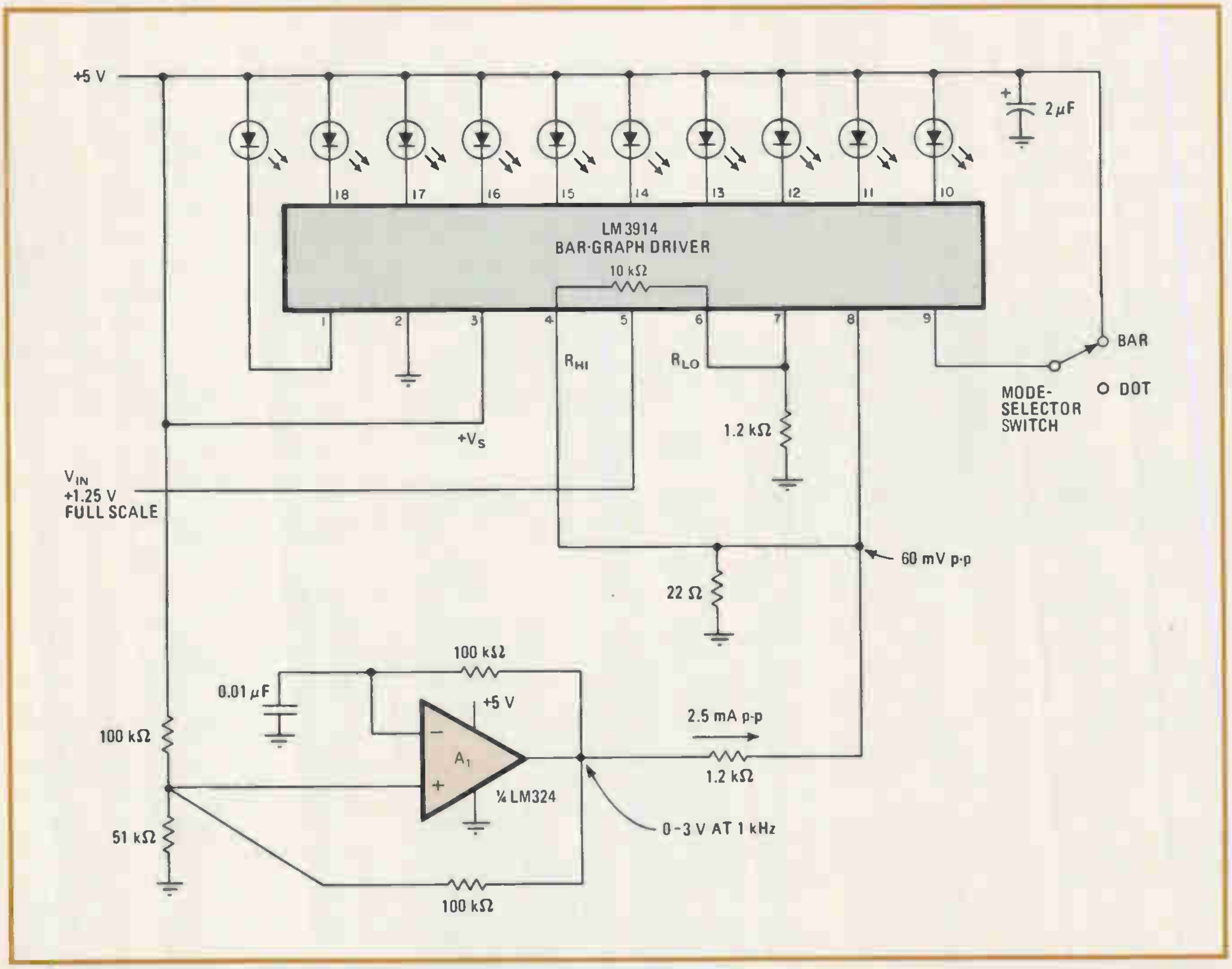
by Robert A. Pease
National Semiconductor Corp., Santa Clara, Calif.

Commercially available bar-graph chips such as National's LM3914 offer an inexpensive and generally attractive way of discerning 10 levels of signal. If 20, 30 or more steps of resolution are required, however, bar-graph displays must be stacked, and with that, the circuit's power drain, cost and complexity all rise. But the techniques used here for creating a scanning-type "dithering" or modulated display will expand the resolution to 20 levels with only one 3914 or, alternatively, make it possible to implement fine-tuning control so that performance approaching infinite resolution can be achieved.

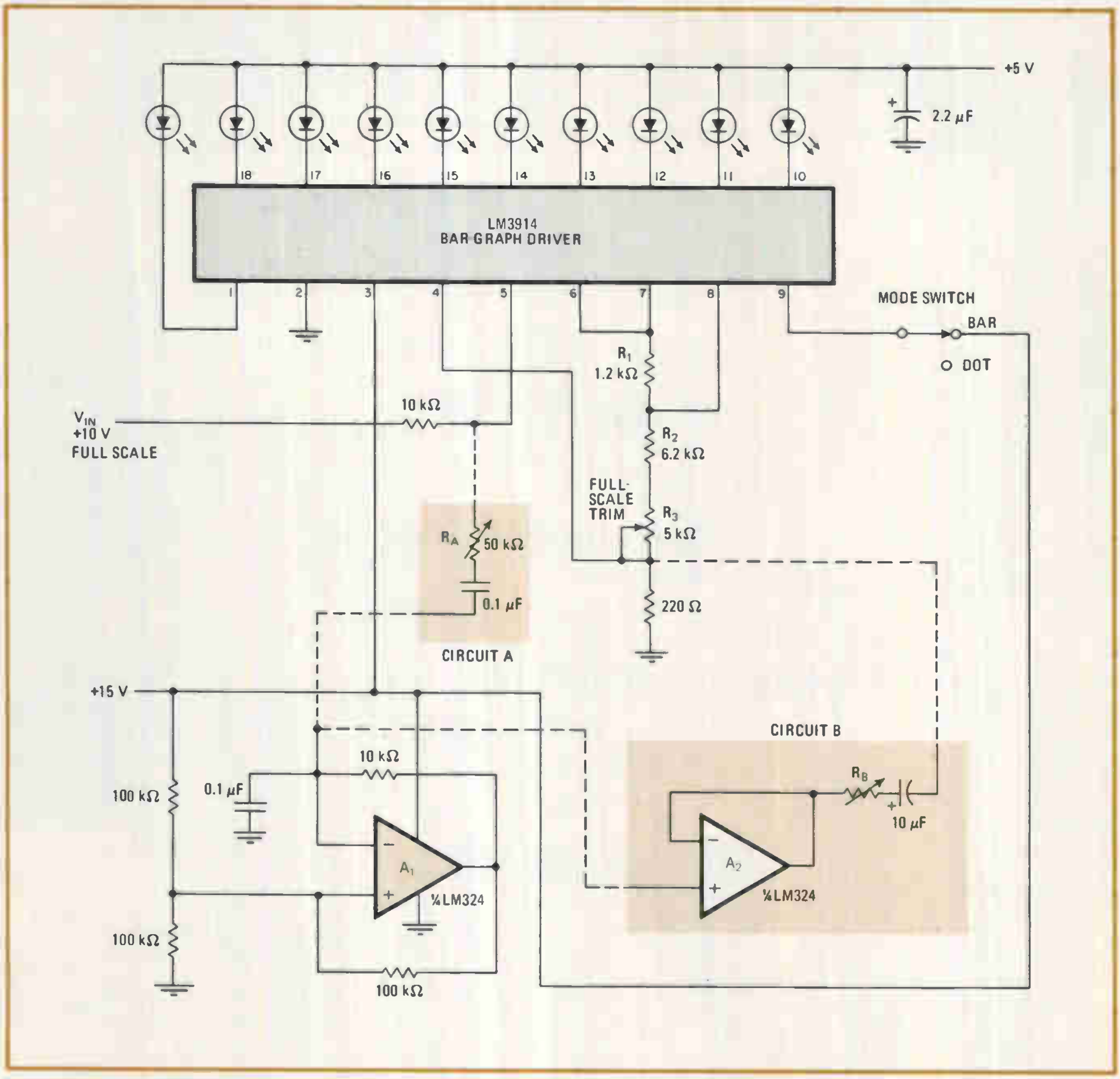
The light-emitting-diode display arrangement for simply distinguishing 20 levels is achieved with a rudimentary square-wave oscillator, as shown in Fig. 1. Here, the LM324 oscillator, running at 1 kilohertz, drives a 60-millivolt peak-to-peak signal into pin 8 of the 3914.

Now, the internal reference circuitry of the 3914 acts to force pin 7 to be 1.26 V above pin 8, so that pins 4 and 8 are at an instantaneous potential of 4.0 mV plus a 60-mV p-p square wave, while pins 6 and 7 will be at 1.264 V plus a 60-mV p-p square wave. Normally, the first LED at pin 1 would turn on when V_{in} exceeded 130 mV, but because of the dither caused by the ac component of the oscillator's output, the first LED now turns on at half intensity when V_{in} rises above the aforementioned value. Full intensity is achieved when V_{in} = 190 mV.

When V_{in} rises another 70 mV or so, the first LED will fall off to half brightness and the second one will begin



1. Half tones. Input-signal biasing on LM3914 bar-graph chip is set by the instantaneous output of a low-amplitude square-wave oscillator so that bar-graph resolution can be doubled. Each of 10 LEDs now has a fully-on and a partially-on mode, making 20 states discernible.



2. Spectrum. Greater resolution, limited only by the ability of the user to discern relative brightness, is achieved by employing a triangular-wave oscillator and more sensitive control circuitry to set the voltage levels and thus light levels of corresponding LEDs. Two RC networks, circuits A and B, provide required oscillator coupling and attenuation. B replaces A if oscillator cannot suffer heavy loading.

to glow. When V_{in} reaches 320 mV, the first LED will go off, and the second will turn on fully, and so on. Thus 20 levels of brightness are easily obtained.

Similarly, greater resolution can be achieved by employing a triangular-wave oscillator and two simple RC networks as seen in Fig. 2. Here, by means of circuit A, this voltage is capacitively coupled, attenuated, and superimposed on the input voltage at pin 5 of the LM3914. With appropriate setting of the 50-kilohm potentiometer, each incremental change in V_{in} can be detected because the glow from each LED can be made to spread gradually from one device to the next.

Of course, if the signal-source impedance is not low or linear, the ac signals coupled into the input circuit can cause false readings at the output. In this case, the circuit in block B should be used to buffer the output of the triangular-wave oscillator.

The display is most effective in the dot mode, where supply voltages can be brought up to 15 V. If the circuit's bar mode is used, the potentials applied to the LEDs

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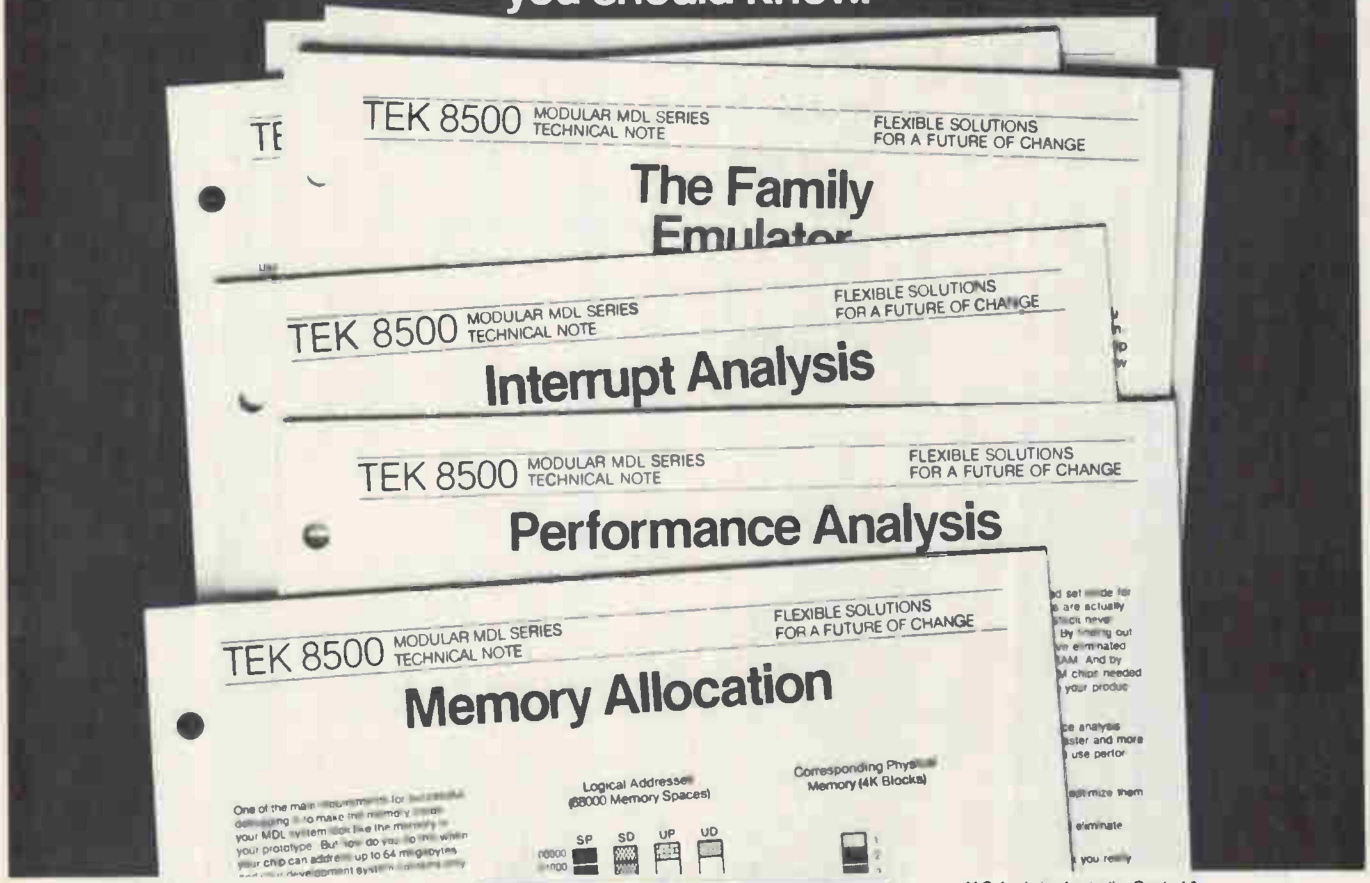

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should be made no greater than 5 V to avoid overheating.

To trim the circuit, set the LM3914's output to full scale with R_3. R_A or R_B should then be trimmed so that when one LED is lit, any small measured change of V_{in} will cause one of the adjacent LEDs in the chain to turn on. □

Current mirror linearizes remote-controlled timer

by George Hughes and S. A. Hawley
Eye Research Institute, Boston, Mass.

Although setting the pulse duration of timers of the 555 variety by remote means is most conveniently done with a single control such as a potentiometer, often there is an undesired nonlinear relationship between wiper-arm setting and output width because of the simple methods employed to achieve control. Adding a current mirror and feedback loop to the basic circuit solves the problem of linearity with little additional complexity or cost.

In general, any current passing through the pot's wiper should be minimized and the pot placed as close as possible to the circuit's interfacing operational amplifier, especially in remote-control applications, where the effects of stray coupling from various processing circuits can be considerable. A typical configuration is shown in (a). In this type of circuit, however, difficulties arise because the op amp's output voltage supplies charging currents to the one-shot's timing capacitor through a fixed resistor. As a result, the pulse capacitor width will be inversely proportional to the current driving C_T and will not be a linear function of the wiper-arm position.

Adding the current mirror and the feedback loop to the circuit, as shown in (b), overcomes this drawback. Here, the mirror's charging current is made a constant whose magnitude is proportional to only the voltage at the amp's noninverting input, V_i, and hence to the potentiometer's setting. In the feedback loop, the average value of the timer's output is compared with a voltage that represents the wiper-arm position, where current injected into timing capacitor C_T is such that the difference is kept small by the virtual-ground properties of the op amp. The average value of the timer's output is itself a linear representation of pulse duration, so that overall linear control is maintained.

This circuit will function with any TTL timer. Parts values are not critical and can be varied to suit a wide range of triggering rates and pulse durations. Substitution of matched dual transistors or packaged current mirrors is recommended to improve the circuit's temperature stability. □

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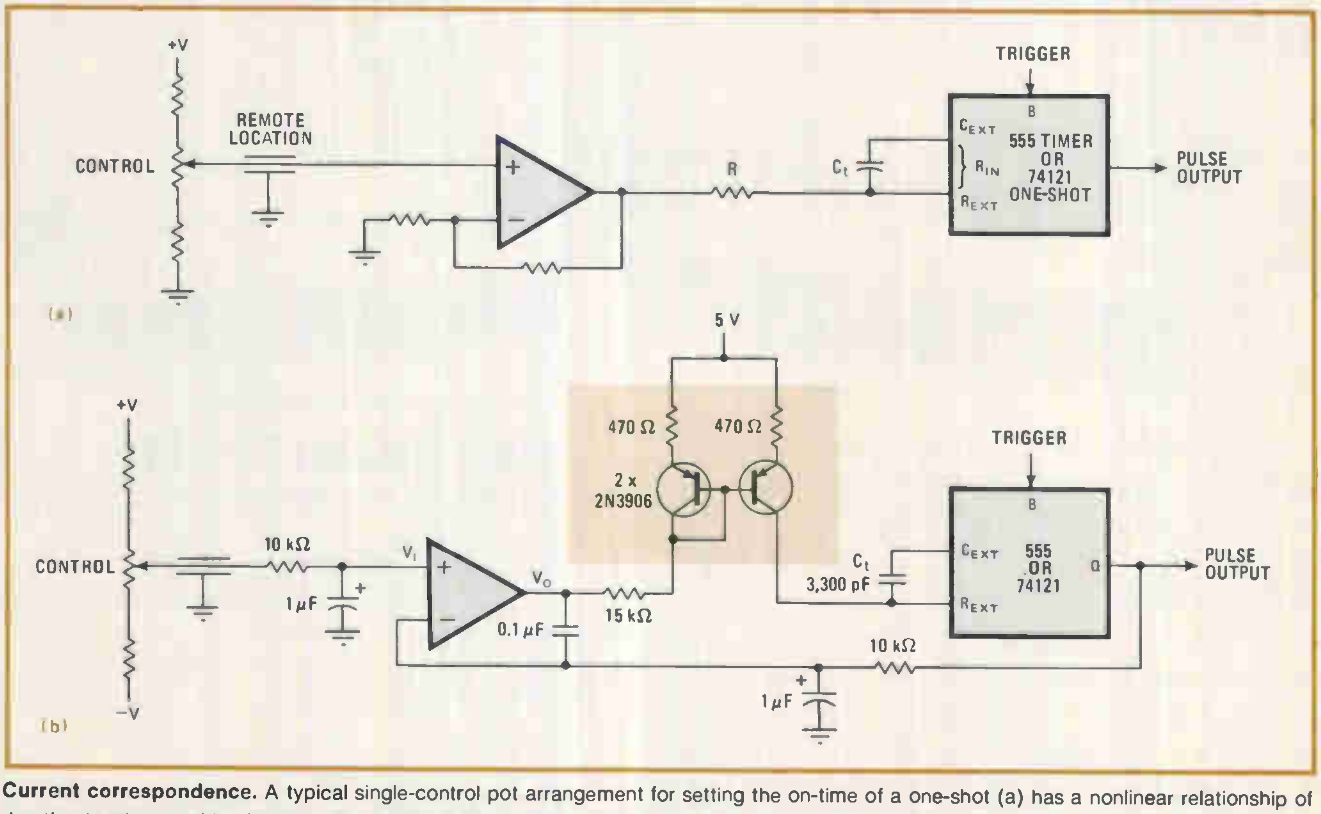

Current correspondence. A typical single-control pot arrangement for setting the on-time of a one-shot (a) has a nonlinear relationship of duration to wiper position because the current-driving capacitor, C_T, is proportional to $V_i(R+R_{IN})$. Adding a current mirror and feedback loop to the circuit (b) linearizes the relationship by generating a constant current set by V_i. The values shown are for $8 < T_{out} < 50$ µs.

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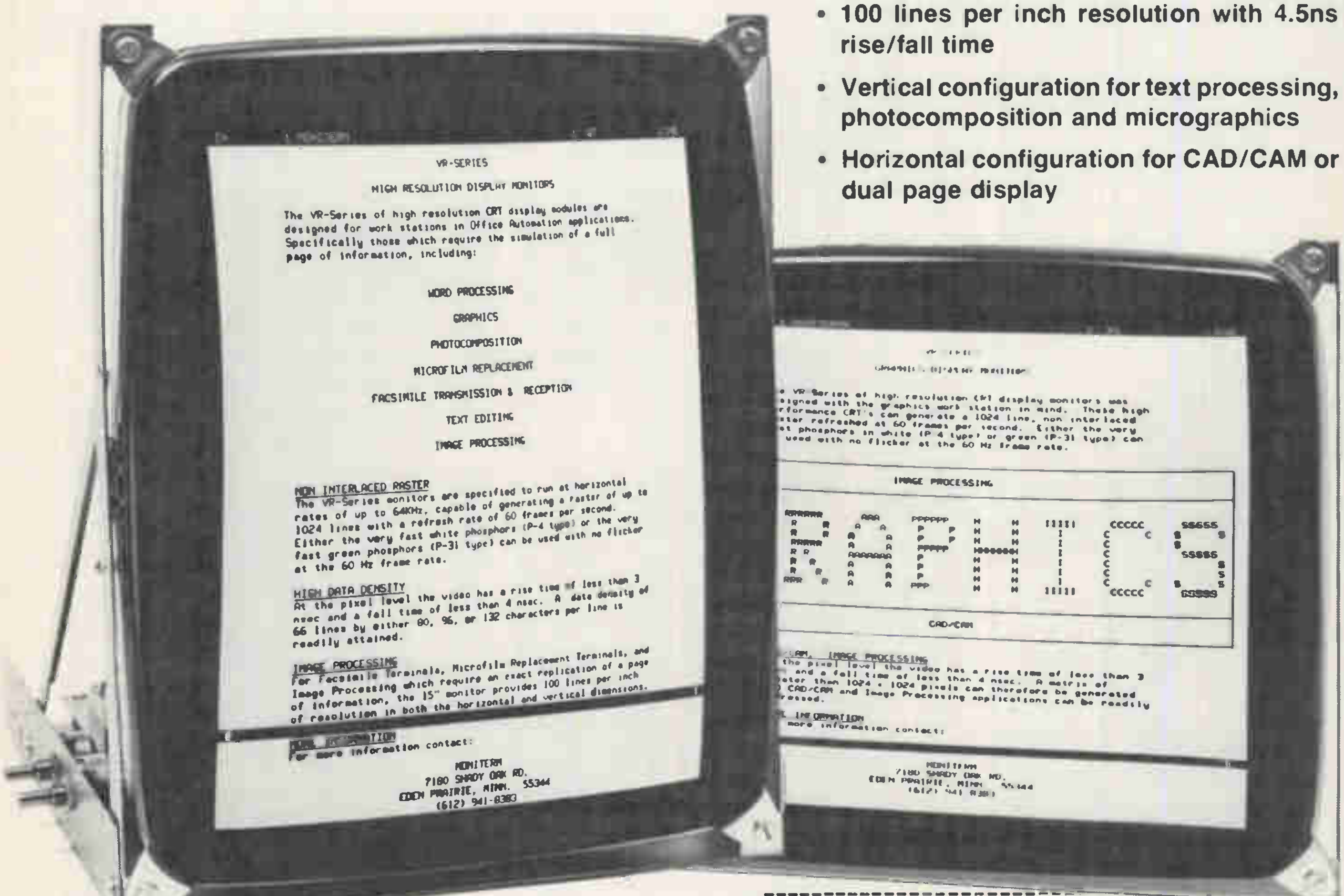

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Microsystems exploit mainframe methods

Proven techniques protect tasks from illegal operations, remove present limits on program size and number of users

by R. Colin Johnson, *Microsystems & Software Editor*

Special report on memory management

☐ Now that multiuser capability is to be found on smaller and more widely affordable computers, memory management schemes reminiscent of mainframes are finding their way even into microsystems. The ultimate management scheme, of course, is virtual memory—the ability of a computer system to make its diverse kinds of memory, be they semiconductor, disk, or tape, appear identical to the programmer. Such a system takes care of swapping code and data into and out of main memory as they are needed by the programmer and in a manner transparent to him or her.

Memory management schemes make it possible for a system to run programs larger than its main memory by requiring only those portions of a program that are currently needed to be resident. In large multiuser situations, the response time at terminals can be greatly decreased if each user's complete program does not have to be resident in main memory. Instead, only the small fragments currently in use reside there, making room for many more users' programs. No long disk accesses are allowed either (only the short ones required to swap in fragments), making switching between tasks even faster.

However, the methods used to decide just which program fragments should be in main memory and which should remain in mass storage can become quite complex (see "Old programmers need new tricks," p. 122). Ideally, the segments most likely to be used in the immediate future should be in main memory, but the solution to such a nondeterministic problem can at best be approximated. Also, the location and order in which segments are placed in memory can become a significant problem, especially if they are of varying sizes. Incoming segments must have contiguous free areas to be loaded into, and that could necessitate moving resident segments about to make room available to them (see "Swapping software for virtual memory," p. 124).

The payoff for fine-tuning a memory management scheme is worth it, though—the system's throughput is significantly increased. And, as semiconductor technology continues to breed ever faster processors and ever cheaper memory, schemes for managing these resources will continue to proliferate, particularly in 16-bit microsystems using special memory management large-scale integrated circuits.

One key issue in the management of a large semiconductor address space containing diverse kinds of information is protection. Users must be prevented from interfering with each other's memory areas by hardware that makes it impossible for them to do so.

However, to make protection possible, individual tasks must be subdivided into sections that hang together logically. For instance, code that has been developed using modular techniques can be easily divided into separate sections for the main program, subroutines, and functions. Also, the data used by the program should already be divided into various structures, like records, arrays, and strings, whose nature can be reflected in the way they are mapped into main memory. In addition, stacks that are subject to dynamic growth and shrinkage can be placed in special areas for the various users as well as one for the operating system.

Multiuser, and often even single-user jobs that use multitasking within a single program, demand this sort of separation. Also a necessity are hardware protection mechanisms that prevent code sections from being overwritten with data, stop attempts to use read-only areas for scratch-pad write operations, and generally raise the integrity of the total system by guaranteeing that unwanted operations cannot be performed. As a bonus, many of the hardware implementations allow users to share areas of memory, such as high-level-language compilers, without the need to keep copies.

Basic techniques

To manage memory at all, it is necessary to separate the addresses used in a program from those delivered to the memory system itself. The addresses in the program are termed the logical addresses, since they identify logically distinct pieces of information with a unique numerical quantity. They are not necessarily the actual semiconductor memory locations—those are the physical addresses. The physical address is what programmers have traditionally used in programs, being the actual bit patterns supplicd to the address bus of main memory. The logical addresses must be translated into the physical ones by a hardware mechanism that recognizes the former, looks up its physical counterpart, and supplies that to the memory system.

To effect this translation, each memory segment or page is associated with what is called a descriptor—a hardware register that contains its physical address and protection status. The way in which this descriptor is accessed varies widely, as does its actual composition and layout. For instance, the operation code of the instructions might simply contain a field that indicates the descriptor to be used, whereas a more elaborate scheme might use an associative (content-addressable) memory that looks up the proper descriptor on the fly.

Mainframes often use several levels of look-up, involving several types of segmentation. There might be a user look-up table that identifies the processes accessible to that user; then each process may be segmented into its various data, code, and stack segments; each of those may in turn have associated with it a descriptor identifying its beginning address and length; and those may then be further subdivided into fixed-size pages. This four-level look-up may then be speeded up by a local cache memory that holds those pages currently in use.

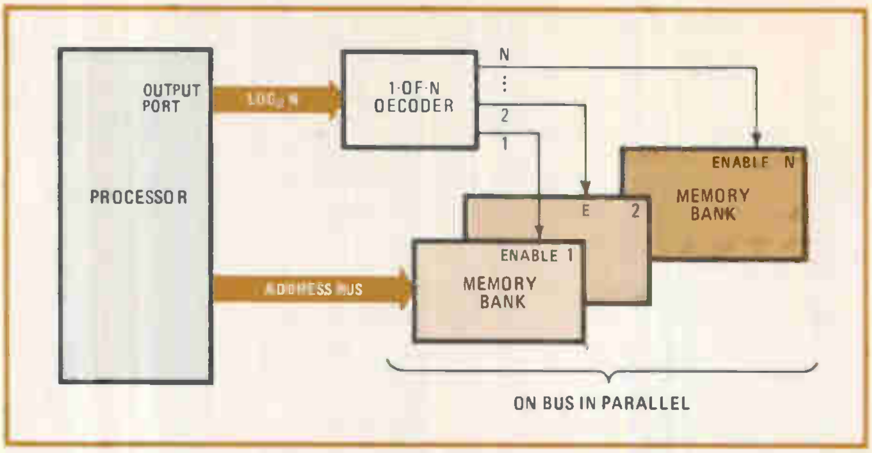
On the microsystem level, however, a two-level look-up is the commonest, as is the use of software to perform many of the functions implemented in hardware by mainframes. In fact, the varying amounts of hardware and software needed to support a memory management system is one of the distinctive differences between approaches. At the least, hardware is needed to hold the addresses of the beginnings of segments or pages, and for virtual memory management the processor itself must have an abort-instruction function with which instructions that try to access information not yet in main memory can be restarted after it has been swapped in from mass storage. (This is an uncommon feature, however—it was not designed into any of the 16-bit microprocessors now in production, though most of the next generation will include this capability.)

Some implementations

The simplest form of memory management is called bank switching. It involves merely turning on one of many memory banks under software control. Usually an output port is dedicated to selecting one bank and disabling all others (Fig. 1). This scheme is the easiest to implement and is found on many existing multiuser microsystems. A copy of the operating system kernel is kept in each bank, and switching between users is accomplished by periodically interrupting the processor, which then branches to the system subroutine that actually writes the next user's number into the bank-select

GLOSSARY OF MEMORY MANAGEMENT TERMINOLOGY

abort (instruction)	halting an instruction because its operands are not in main memory
address binding, address mapping, address translation	calculating the real physical memory address of operands from the logical address supplied by the processor
bank switching	wiring memory banks in parallel so that only one is active at any given time (under software control)
base address	the address of the first location in a segment or page of memory
content-addressable memory (CAM)	a memory bank in which the contents of each location are simultaneously compared with incoming data for matches
compaction	relocating programs in memory so that they and unused areas are contiguous
descriptor	a preformatted data set describing the location, access privileges, and status of a region of memory
dirty regions	regions of memory that have been modified since being loaded into main memory
dynamic allocation	the run-time reorganization of data storage to accommodate an executing process
hit ratio	the percentage of time that the information requested is resident in a cache memory
latency	the extra time delay introduced by a memory management unit into the path that the address lines take to main memory
logical address	the address used in programs to separate logically distinct values
offset	the number of locations from the base address to the desired information
page	fixed-size region of memory
physical address	the bit pattern applied to the address bus of real physical main memory
residency	the situation when information currently needed is already in main memory
static allocation	the load-time organization of data storage that then stands all the while a program is executing
swapping	exchanging information between mass storage and main memory



1. Switching banks. The simplest kind of memory management uses several banks of memory wired in parallel, only one of which is activated at any one time. An output port specifies the bank to be switched on, and an off-board decoder guarantees that only one bank will be active. This method is easy to implement but does not let users share regions of memory and often wastes memory space since users seldom fill their bank.

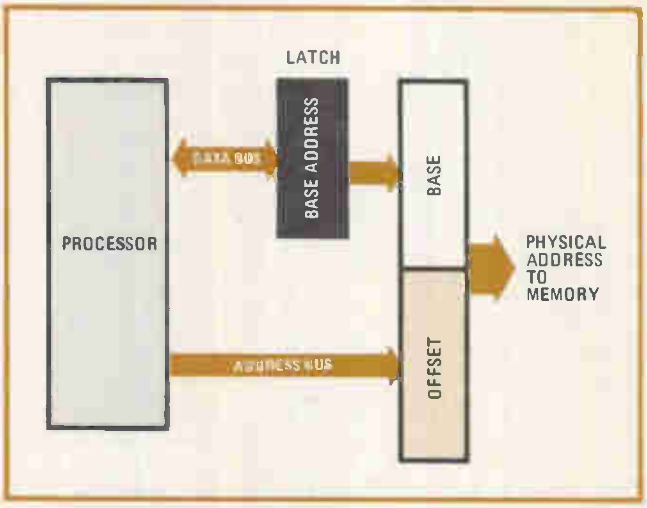
output port. But this form of memory management is very rudimentary—it wastes a lot of memory, does not support shared code or data, and does not allow programs any larger than normal to be run on the system.

A single latch can expand a memory system's address space (Fig. 2). The data in the latch serves as the upper bits of the physical address, which are often called the base address, and the logical address can then be appended as the lower bits, indicating how many locations past the base address the desired information is and hence called the offset. But this method still does not permit the use of shared code, requires that segments be located on boundaries as large as the banks are in the switching approach, and does not allow any oversize programs to be run.

A common extension of this method sequesters some of the upper bits of the logical address and uses them to select one of several base registers. This scheme is used by the MC6829 memory manager made by Motorola Inc. of Austin, Texas, as well as by the 74610 made by Texas Instruments Inc. of Dallas. Neither of these parts is as sophisticated as the LSI parts available for 16-bit processors like Motorola's MC68451 (Fig. 3) or National Semiconductor's 16082 (Fig. 4), but they offer an economical alternative to small-scale IC implementations. The 610 uses the upper 4 bits of a 16-bit address to select one of sixteen 12-bit base addresses. This address is then appended to the remaining 12 bits of the logical address to form a 24-bit physical address. Thus, a 16-megabyte address range is divided into 4-K-byte pages, 16 of which are accessible without reloading any base registers (Fig. 5).

The 6829 uses the upper 5 bits to select one of 32 10-bit registers to form a 20-bit address, thus dividing a 2-megabyte space into 2-K-byte pages. This method allows pages to be relocated in memory in a manner transparent to the programmer merely by reloading the base registers.

The approach can also be used to share code, eliminating the need to keep duplicates of often used pages, like those containing the operating system kernel—a necessity in the bank-switched method. The way to do this is to allow each task to have access to the same page in memory by loading one of the base registers with the same address every time a context switch has to be done between tasks.



2. Expanding space. A external latch can serve to expand the available memory space if the data in the latch is used as a base address. The address coming from the processor is used as an offset (index) and is appended to the base to form a wider address bus.

If only one set of base registers is provided in a system, then a context switch requires that the base registers be reloaded with the locations of the new task's program and data. However, this overhead can be eliminated by using multiple mapping registers that are selected in the same manner that banks are—namely, writing a number into a dedicated location that enables one of many base register sets. Alternatively, the function code outputs can be used to select memory management units, so that separate ones can be used for system, data, code, and stack operations. The 6829 has four sets of 32 base registers for fast switching between four tasks, each of which has access to 32 unique 2-K-byte pages. Both the 6829 and 74610 can be selectively disabled, so that more than one unit may be used in a single system.

Any such method, though, introduces another time delay into the path that addresses take to memory. Called latency, it is the time it takes to decode the upper bits of the logical address and deliver the base address they select to memory. Latency can be minimized by using base registers that can be accessed quickly (the 6829, for example, introduces only 100 nanoseconds of latency); but it cannot be eliminated entirely unless the memory fetch cycles are performed in parallel with the

Old programmers need new tricks

When microprocessors first became available in the early 1970s, engineers designing logic with the relay ladder approach were hard put to convert that process into machine language programming. Even though the microprocessor was to perform the same function as the relay ladder, programming it had little in common with relay ladder design.

A similar phenomenon is occurring today—designing software for computer systems using the new memory management units is a task riddled with concepts new to the microsystem programmer (see glossary on p. 120). New items like segment descriptors, on-demand page-swapping algorithms, and virtual address translation make programming these systems a task that requires new methodologies.

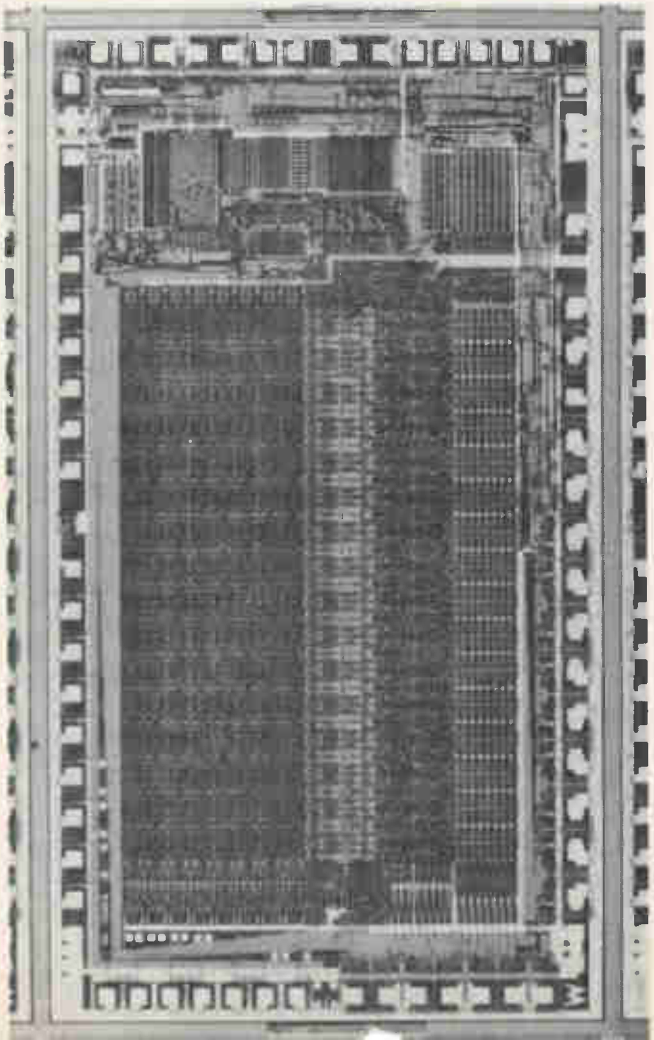
At the lowest level there is the matter of loading and managing off-chip segment registers in such a way that memory is fully utilized. Segments or pages of memory must be allocated so that its use is optimized for the tasks to be performed by the microsystem in question. This process involves demand-swapping algorithms that keep track of which segments or pages of memory are being used the most (see "Swapping software for virtual memory," p. 124). Then, when a new task is brought into the system, the least used region can be returned to mass storage, making room for the new one while affecting the performance of the rest of the currently executing tasks as little as possible. Also, there is the issue of memory protection: the flagging of individual segments or pages with access privilege information that prevents users from crashing the system or destroying other users' data.

This sort of real-time control of memory allocation requires the use of programming techniques new to the microprocessor software engineer. Still, it is not as if these techniques will have to be invented.

In fact, the answers to most of the questions a microprocessor programmer might have regarding memory management can be obtained from the mainframe industry. There are two reasons for this: extensive research and testing has already been done by it in the development of optimal algorithms for storage management; and the manufacturers of memory management chips are employing former mainframe people as designers.

Every major semiconductor manufacturer of a memory management unit has had experienced mainframe engineers on its memory management design team, and it shows. The methods employed are taken directly from those already in use on the bigger machines, albeit on a smaller scale. For instance, the use of a bit to flag regions of memory that have been altered since being loaded is taken directly from mainframe practice. However, the biggest machines track not only use, but also how many times a page has been used, so that swapping algorithms may decide which pages can be returned to memory while having the least possible impact on the total system throughput.

It is safe to assume that mainframes will continue to lead the way for microsystem development, too, since memory management designs will not be committed to silicon before being tested and proven in mainframes.



execution cycles, as in pipelined machines like Intel's iAPX-286 that prefetch instructions.

But there is one problem with only appending the offset to the base address—pages may be located only on boundaries equal in size to the page length. This can cause difficulties in systems that use large page sizes, since a significant amount of memory can be consumed by pages with unused portions. For instance, if Digital Equipment Corp.'s PDP-11 minicomputers, which use 8-K-byte pages, only appended their 13-bit offset to a base address, then the 11/34 could only be configured with 32 8-K-byte pages in its 256-K-byte address space, many of which would have unused portions.

One solution is to make the pages smaller, such as the 512-byte size of the 16082 from National Semiconductor Corp. of Santa Clara, Calif. But a result is that the page descriptor tables become quite large. The 16082 needs all of 128-K bytes to hold its page tables, so that they had to be made accessible only virtually (a two-level look-up scheme is used, with only 1-K byte of tables in main memory and the rest kept on a disk).

To alleviate these problems in the 11/23 and /34, however, DEC uses an overlapping add operation between a 12-bit base address and a 13-bit offset to produce a 18-bit physical address (Fig. 6a). This arrangement

3. Keeping it regular. The extreme regularity of Motorola's memory management unit (MC68451) is strikingly apparent in this die photo. It stores some sixteen 9-byte-long descriptors as well as containing several control registers for handling multiple-unit configurations.

allows pages to be located on 64-byte boundaries and also to be of varying lengths—for which reason they will hereafter be referred to as segments. The first step is the division of the 16-bit logical address from the processor into a 3-bit segment number and a 13-bit offset, the former selecting one of eight 12-bit base address registers. However, the 13-bit offset instead of being appended, is separated into fields so that its upper 7 bits are added to the 12-bit base and the lower 6 bits are appended to that result, creating an 18-bit physical address. This method produces variably sized segments of 64 bytes to 8-K bytes locatable on any 64-byte boundary.

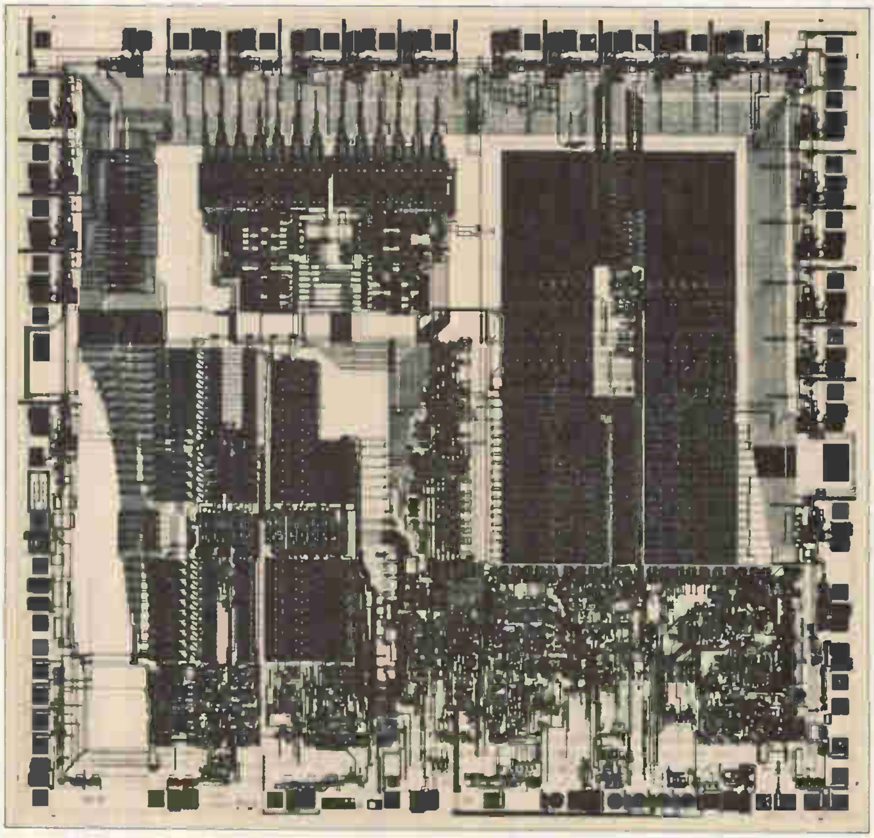
The 8010 memory management unit devised by Zilog Inc., Santa Clara, Calif., uses a scheme that is modeled after DEC's (Fig. 6b), the primary difference being the number of bits allotted to the various fields. A 7-bit quantity selects the base address for 128 possible segments (64 base registers being provided on a single 8010). Also, the segment sizes vary from 256 bytes to 64-K bytes, and a 24-bit physical address is produced for a total space of 16 megabytes.

Intel Corp.'s 8086 also does an overlapping add operation on a 16-bit base and offset to produce a 20-bit physical address. However, its base registers are implied by instructions rather than being explicitly specified in the op code. In the 286, which is software-compatible with the 8086, the Santa Clara, Calif., company abandons this overlapping method, preferring to add a 24-bit base to a 16-bit offset for complete freedom to relocate on any byte boundary.

The other major 16-bit microprocessor manufacturer that has chosen the variably sized segment approach is Motorola. But its MC68451 memory management unit adopts a novel implementation. In place of an adder, it employs a special mask register that allows segments to be any size that is a power of 2 greater than 256 bytes. This is effected by masking the logical address that is brought on chip with a bit pattern stored in that segment's descriptor.

If the mask is all 1s, then the base address is completely masked out and the logical address is passed straight through, becoming the physical address; thus memory in effect becomes a single 16-megabyte page. At the other extreme, if the mask is all 0s, then 16 of the upper 24 bits of the logical address are masked out and replaced with the descriptor's base address, leaving only an 8-bit offset for a 256-byte page. In other words, the mask determines how many of the lower logical address bits will be used as an offset and thus how big the page is. This method has the advantage of replacing an adder, which is an iterative silicon-consuming module, by masking hardware, which is a single-logic-level array of AND gates, thereby making the part faster than it would be if an adder had been used (its latency is 130 ns).

Another distinguishing feature of the 68451 (and also of National's 16082 and Zilog's forthcoming Z8015) is its use of a content-addressable associative memory to select the base register. This method, used on many high-performance mainframes, requires an additional logical–base-address register for every physical–base-address register. When a logical address is applied to the memory management unit, it is simultaneously compared with all the logical–base-address registers and the one that matches it activates the physical–base-address register associated with it (Fig. 7). In this way, purely logical addresses can be used by the programmer, rather



4. Die layout. This memory management unit from National Semiconductor, the 16082, is the only one from a major 16-bit microprocessor maker that fetches descriptors from main memory on its own. It is really a special-purpose processor in and of itself, as can be discerned from the photo. It is the first of a series of slave processors designed to work in a closely coupled configuration with its 16000 series 16-bit microprocessors.

Swapping software for virtual memory

Main-memory management involves a lot of support software to optimize the way programs and data are arranged in memory for maximum throughput. Usually it keeps three lists: an occupied-space list that indicates those portions of memory now occupied by programs and data; an available-space list that reveals which regions of memory have no significant information in them; and a directory of secondary-memory devices that shows the location of information currently being used by executing programs. With the aid of these three lists, main memory can be allocated and reallocated to programs competing for system resources.

Whenever a new task is brought into the memory system for execution, an unused region must be provided to load it into. If after checking the available space list, it is discovered that a large enough region is free, then the new task can be loaded directly into it without the need to swap any information out that is already there.

Many times, however, there will be more than one contiguous area available, requiring the software to choose between them. Two of the best accepted methods for doing so are called "best fit" and "first fit". The first checks the sizes of all available regions and chooses the one that is closest to the size of the task to be loaded. The other just takes the first available space that is big enough. Of course, the tradeoff is between the extra software overhead needed for checking the sizes and the wasted memory that results from loading small tasks into big regions. The fine tuning of a memory managment system involves making just such decisions as to which method will work best in a given application.

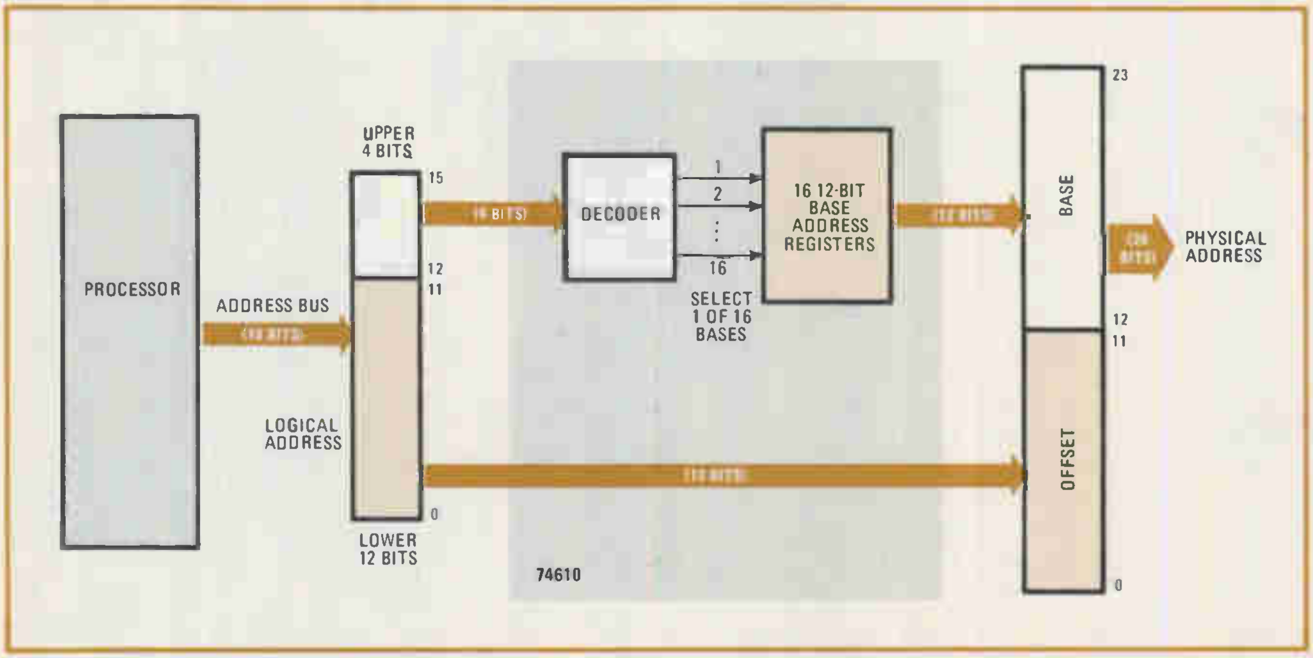
On the other hand, if no space is large enough for the current task, then either a compaction must be done on memory, so that the regions that are available can be grouped together making room for the new task, or one or more tasks already in memory must be swapped back out to mass storage.

Coming up with an optimal replacement strategy in this situation can become an incredibly complex process. One of the simplest methods is a first-in, first-out policy that requires only that the swapping software track the order in which tasks were loaded.

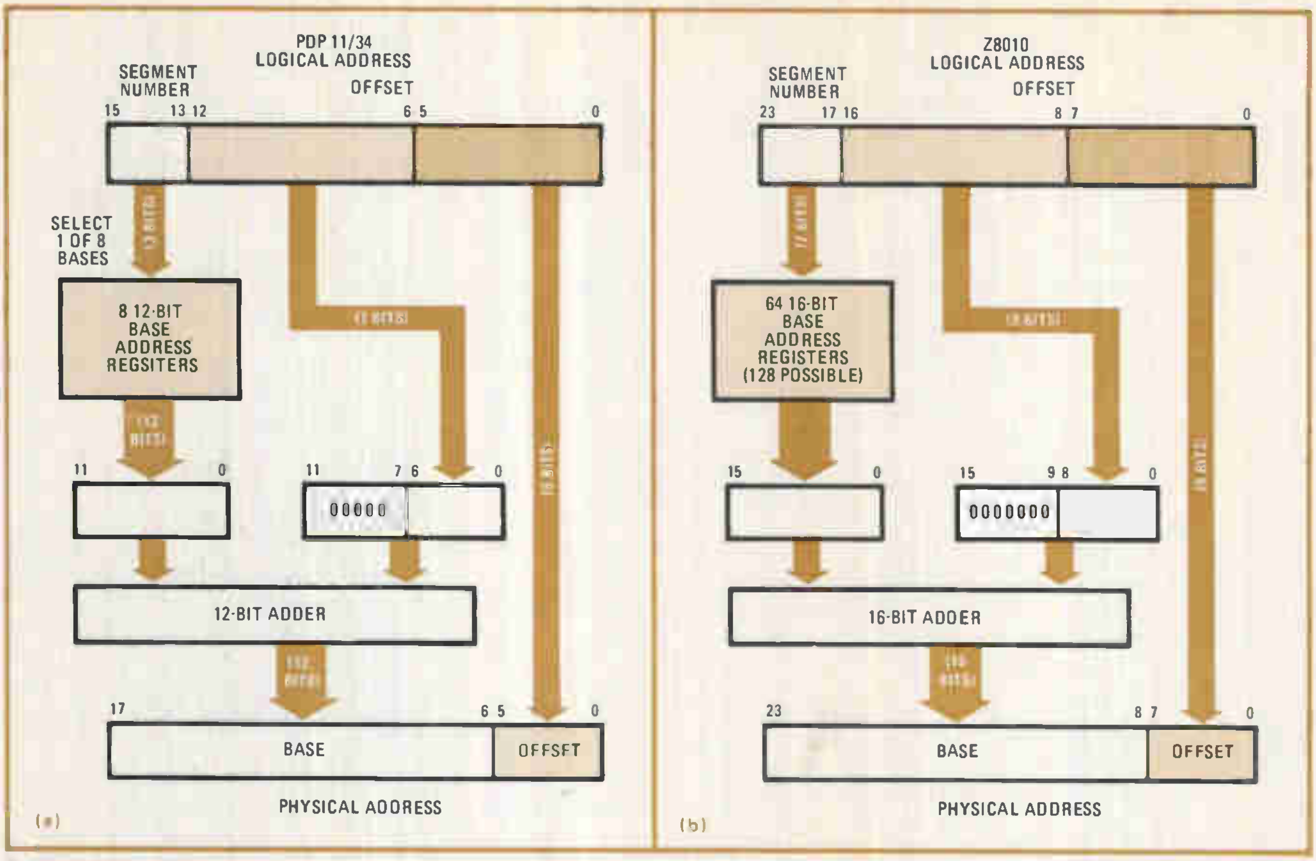
Another more complex method swaps out the least recently used region. This can be accomplished by keeping an age-register count for each loaded task. Whenever a region is accessed, the age register is set to some predetermined positive number. Then periodically all the age registers are decremented by the computer system software, and the least recently used region becomes associated with the age register with the smallest value in it. However, other parameters must be taken into account, too—for instance, whether a region has been altered, since then it need not be swapped back into mass storage, being identical with the copy already there.

than those in which the upper portion is really a segment number. Many programmers prefer this method even though it involves yet another level of logic in the memory address path and obscures the problem of determining whether a mistaken address calculation was caused by an attempt to overflow the current segment or by an improper type of access (like trying to write a read-only area). The Z8015 directly supports 2,048-byte pages and puts 64-page descriptors on line. Other sizes of pages can be hardwired in, and up to 4,096 page descriptors can evenly divide the 8-megabyte address space.

Intel's 432 also uses an on-chip content-addressable associative memory. However, it is not comparing logical addresses with its contents but instead uses what is called a nickname. This local identification number can be as short as 6 bits. Unlike segment numbers, which



5. Only mapping. This memory-mapping unit from Texas Instruments may be used with any microprocessor with 16 address lines (like most 8-bit units). It expands such a memory space to 16 megabytes with sixteen 4-K-byte pages accessible without reloading any registers.



6. Copy a winner. The proven address-translation mechanisms of the PDP 11/34 minicomputer from Digital Equipment Corp. served as the template for the design of Zilog's Z8010 memory management unit. The only differences that are found are in the sizes of the bit fields.

indicate a specific descriptor register, it is written directly into the associative memory array, just as resident logical addresses are written into the 68451s and 16082s. If the nickname is present in the associative memory, then it activates the physical–base-address register associated with it. Otherwise, the required descriptor information must be located by means of a two-level look-up process. Two-level look-up schemes are popular because they allow a single segment or page to have different access privileges attached to it, depending on the path used to get there. For instance, the operating system will use a different path from the one users do.

Protection racket

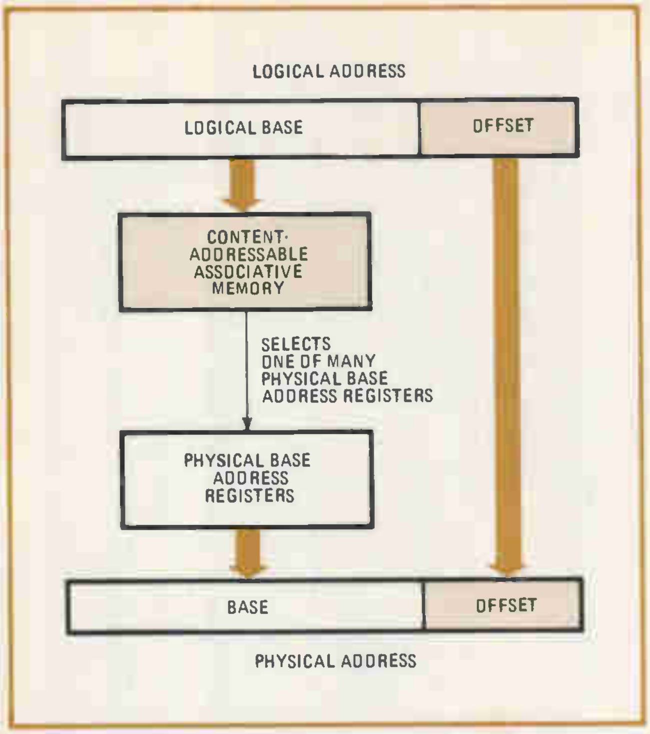
But the logical into physical address translation is only half of the memory management story. Protection is the other half. Whether the system uses variably sized segments or a fixed-size page, hardware support protecting them against improper accesses is becoming mandatory, especially in large multitasking systems. A fully protected system stops users from inadvertently violating the operating system and causing a crash. It can also allow users to share code without letting anyone else overwrite it or even, for that matter, inspect it (this is the result of execute-only protection status).

The most common protection status possibilities attach a system-only, execute-only, read-only, code-only, data-only, or stack-only status to each segment or page. Also, several levels of access privilege are becoming popular, allowing code from various levels of operation ranging from system subroutines to user applications to be protected from inadvertent mishaps.

These status indicators are held in the segment's or page's descriptor, along with the physical and possibly logical base addresses. These registers can become very wide and often include other status bits indicating current usage, such as whether the segment or page is present in main memory, whether it has been used recently, and whether it has been modified since being brought in from mass storage.

Each time a memory access is tried by the processor, the memory management unit checks to see whether the attempt violates any of the protection status bit fields in the descriptor and allows the access to occur only if all is found to be well. Also during the access, the current status bits are updated by the memory management unit so that the operating system may easily keep tabs on the status of each segment or page. This can greatly increase the efficiency of swapping operations (see "Swapping software for virtual memory," p. 124), since segments or pages that have not been modified (are not "dirty") need not be returned to mass storage because the copy that is already there must be identical. In addition, segments or pages that have not been used recently are flagged as prime candidates for swapping back to mass storage in the event that room is needed to bring in a new task.

Figure 8 shows the basic layout and definition of the 8-byte-long descriptors used on Intel's iAPX-286, the only 16-bit microprocessor to employ an on-chip memory management unit. The 286 approach uses only four



7. Memory associations. A content-addressable memory (CAM) can be used to activate a physical base register. The logical address put out by the processor and all CAM locations are compared simultaneously, activating the base address associated with a match.

descriptors so as to maintain compatibility with the 8086 (in fact, they are merely widened versions of the 8086's base registers). Thanks to the 24-bit base, segments can be located on any byte boundary in the 16-megabyte address space. The 16-bit limit field specifies the segment's length, and the access byte gives its privilege status. In addition to the normal access restrictions, the 286 also has four operating levels that are prioritized, so that access to segments may be restricted to tasks operating at the specified level or higher.

The 286 actually uses several different kinds of descriptors, each with slightly different layouts and definitions depending on the type of information that is contained in them. Also, the management and organization of system tables for these various types of segments will be supported by silicon subroutines.

The 68451's 9-byte descriptor (Fig. 9) has several unusual features in addition to the logical address mask that determines how many bits of the base address will be appended to the offset, thereby setting the page size.

One of the most prominent of these is the address space table, which holds an 8-bit task identification number for each of the eight possible combinations of processor access (as determined from its three-function code output), as well as a duplicate set for direct-memory-access requests. Then for each memory-access request the task number is masked by the segment's address-space mask, which then must match its address-space number for the access to be granted. This setup allows code and data to be shared by tasks.

For instance, suppose that operating system tasks are assigned an address-space task number of 10000000_2 and a user's segment has an address mask loaded with 01111111_2 and a task number of 00000000_2. Then the operating system will have access to the user's segments since after the mask operation ($10000000_2 \cdot 01111111_2 = 00000000_2$), the task number will match the segment number. Though this scheme is unusual and initially cumbersome, it does allow many more combinations of segment sharing than the others do.

There are 32 descriptors on a single 68451. Up to six of them may be wired in parallel, and with external buffering any number may be put on line.

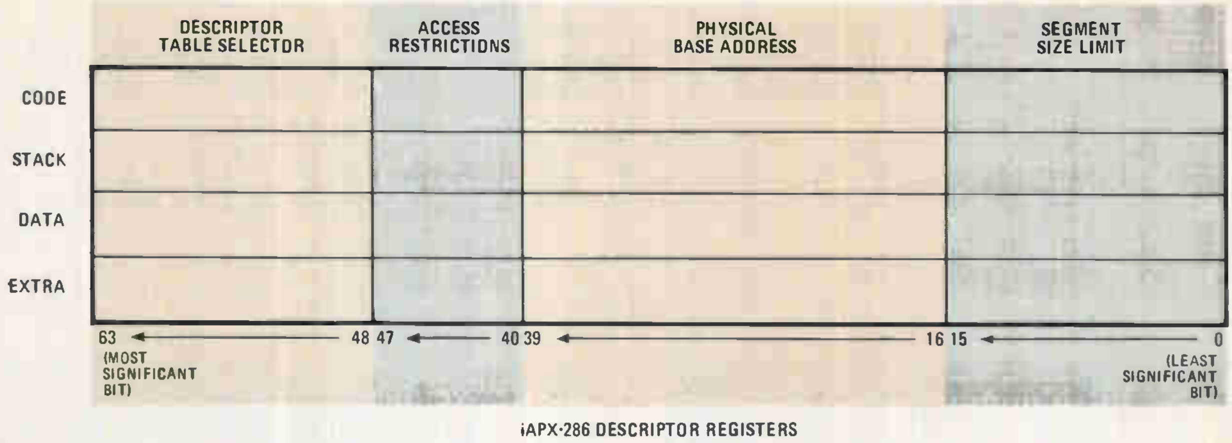
Virtual transparency

Virtual memory refers to the property of a system that permits programmers to ignore the process of swapping. The system itself interprets logical addresses, bringing the information to which they refer into main memory without the programmer having to deal with the actual operating system calls that effect the swap. Virtual memories not only free the programmer from the task of managing storage, but in addition make programs independent of the particular configuration and capacity of the system used to execute the program. There are a number of tradeoffs involved here, especially as to how much of this activity should be handled in software or by hardware.

The total hardware approach is taken by National's 16082—the most ambitious memory management unit of all the LSI offerings. It lets the programmer use purely logical addresses with no embedded segment numbers. It uses a 32-entry associative memory to see if the requested logical address is referring to a page that is present in main memory. If the page descriptor is absent, the unit halts the processor and fetches the missing descriptor from main memory, a process that takes only about 3 to 4 microseconds if the page is already in main memory. Most other implementations require the processor itself to fetch missing descriptors—a much slower business. If the page is not present in memory and must be fetched from mass storage, then the instruction making that request is aborted, the missing information is brought in from disk, and the instruction is restarted.

The ability to restart instructions implies that the processor itself must have some special capabilities. The reason for this is that the instruction requesting the missing information is in the middle of execution when the discovery is made that a page is missing and its operands are not in main memory. Most processors do not recognize any external inputs while they are executing an instruction and will, therefore, go ahead and work with the erroneous data. The normal interrupt pin cannot be used to stop a processor that is encountering a page fault since it is checked only after each instruction has been executed, possibly leaving garbage in its internal registers.

This problem may be solved in one of two ways. Either hardware backup registers must be provided on chip to save the state of the machine, or the microcode that performs the execution must check with the memory management unit to make sure that the information is really present in memory before it begins work. The former method is used by the 16082, so that when an



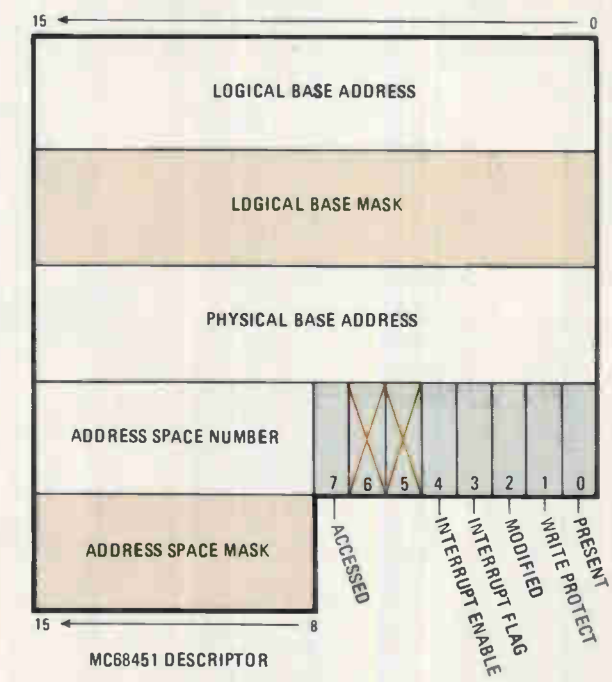
8. Widened. The four segment base registers of Intel's 8086 have been widened on the instruction-set–compatible IAPX-286 to accommodate the extra fields necessary to implement virtual memory management. Also, 24-bit base registers allow relocation on any byte boundary.

instruction is aborted, all the registers that could have been changed are restored to their former states by being reloaded with their back-up copies. This is also the approach being taken by some users of the 68000 but very clumsily. Since the present 68000 is not capable of restarting instructions, several users are employing a second 68000 whose only function is to back up its registers, which are then flushed out and reloaded into the main 68000 whenever a page fault is encountered. Motorola's memory management unit, however, does detect and signal page faults, and the company promises a new version of the processor that will have its own on-chip back-up registers sometime next year.

Zilog too, is redesigning its processor to handle page faults and calls the new one the Z8003 [*Electronics*, June 30, 1981, p. 119]. It works with Zilog's new memory management unit, the Z8015, to provide instruction abort and restart capability. Some software is also needed to figure out which registers on the Z8003 may have nonsense in them and how to restore them.

Intel's approach to restarting instructions on the 286, however, is quite different. First of all, only instructions that load the descriptor registers are restartable—not just any instruction, as on the 16082, 68451, and Z8015. When one of the instructions that affect the segment registers is encountered, a new descriptor is fetched from main memory and loaded into one of the four on-chip segment-descriptor registers. At this time additional protection checks (other than the ones made with accesses that do not load segment registers) are carried out to ensure that the desired access is a legal one and the segment is actually present in memory. If it is present and access to it is legal, the instruction is completed, and later instructions will use that descriptor implicitly (that is, without having to specify it). If the segment is not present, then an interrupt is generated and software must fetch it from mass storage, update the descriptor table in main memory, and load it into available free space, possibly swapping out other data to make room.

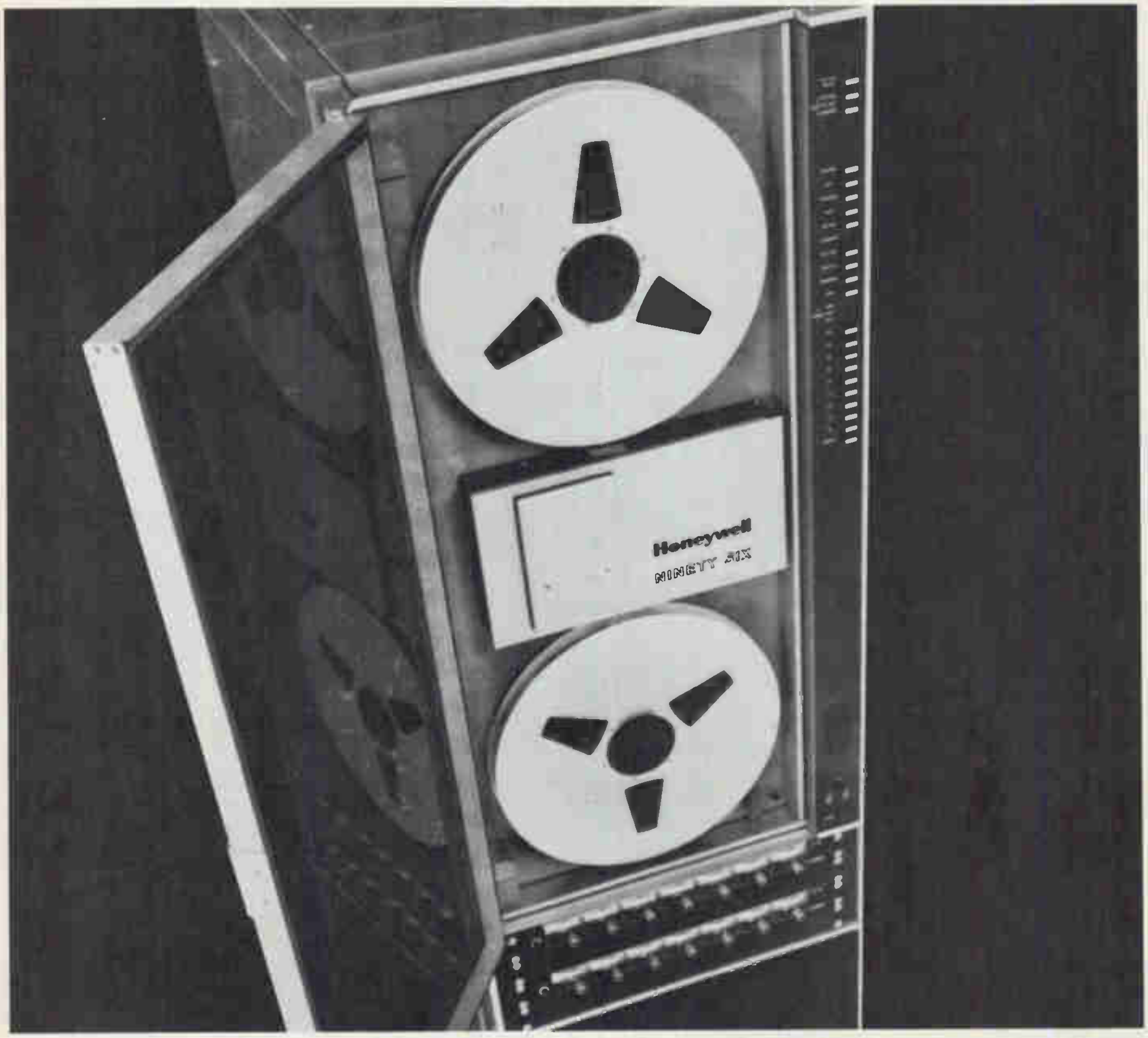
As descriptors must be reloaded whenever a new segment is to be accessed anyway, all instructions need not be restartable—only those that load segment registers. This characteristic matches the 286's memory management architecture, which holds only four segment descriptors implied by instructions (code, data for global variables, stack, and extra for local variables). Since these descriptors will be reloaded fairly often, more software overhead is involved than in schemes that put multiple descriptors on line. However, the instructions that will most often be used will have only 16-bit offsets in the op codes, making programs shorter than those that use longer addresses. □



9. Masking many. Both the page size and the memory-sharing capability of Motorola's 68451 memory management unit are determined by a masking operation. Pages may be any size that is a power of 2 greater than 256, and segments are easily shared.

It's nice you can still depend on something.

The Honeywell Model Ninety-Six.



Honeywell Test Instruments Division, Box 5227, Denver CO 80227, (303) 773-4700.

Honeywell

Programmable modules link up easily into custom test systems

IEEE-488–compatible modules and system-oriented controller automate the TM 500 concept for a wide range of test environments

by Robert E. Metzler, *General-Purpose Instruments Division, Tektronix Inc., Beaverton, Ore.*

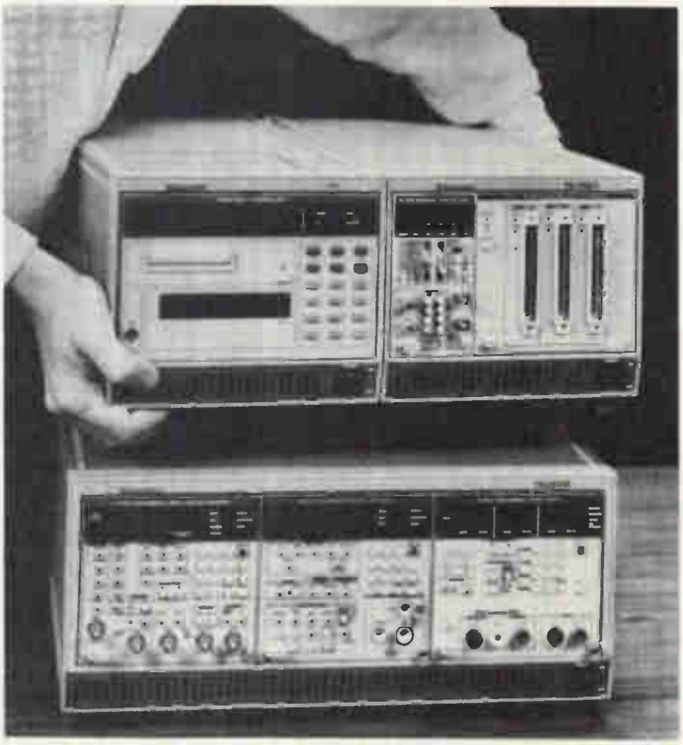
□ Test engineers, production supervisors, and field service managers are placing a tough set of demands before instrument manufacturers. They want measurement tools that are more flexible and easier to use and that at the same time reduce the lifetime cost of their ownership. Those demands are now met by the TM 5000 (Fig. 1), a modular, configurable, programmable, and IEEE-488–compatible measurement system that is sophisticated enough for the production test engineer yet simple and portable enough to be used at field sites. In addition, its programmability permits specialized software programs to be written for applications, such as process control, in many industries.

The system is based in part on the modular instrumentation concept advanced nine years ago in the TM 500 series. That approach has proven successful because of the flexibility in system configuration the modules permit; a user can choose those measurement functions needed for a particular task and purchase the corresponding modules. When other functions are needed, the user need only update the instrument with other modules; the entire system need not be replaced.

In designing the TM 5000 series, difficulties in integrating instruments compatible with the IEEE-488-178 standard for interconnection, such as differences in command structures, unintelligibility of commands, and insufficient means of handling certain common occurrences, were overcome by developing an instrument-oriented IEEE-488 controller at the system rather than at the component level. This systems approach also led to the creation of an IEEE-488–oriented programming language that would reach a broad user base, including design, research, production test, data-logging, calibration, and maintenance personnel.

Programming is a creative act. If the design of a controller can be used effectively by programmers of varying skill levels, they will be able to rapidly develop software from concept to code translation. Thus, at the outset, the controller was designed to place as few constraints as possible on novice or advanced programmers.

Based on the 68000 microprocessor, the 4041 controller can be expanded to include as much as 160 kilobytes of random-access memory. The programmer can use this space for creating, editing, and debugging an application program, and once the program is closed, it can be permanently stored on a minicassette using the controller's integral DC 100 magnetic-tape drive. During testing, the program can be downloaded from tape to main memory.

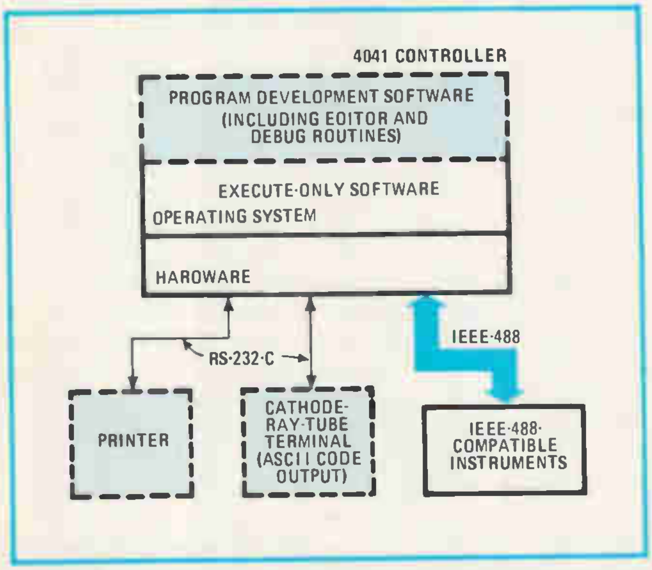


1. System building. Combining the modular design approach of the TM 500 with the IEEE-488-1978 interface standard resulted in the TM 5000 series shown above. The controller, top left, enhances IEEE-488 operation and serves both the novice operator and the advanced programmer.

These two controller environments—programming and testing—are also addressed by the two modes of the controller's operating system. In its execute-only mode, intended for testing, the controller contains only those portions of the operating system (in firmware) needed to execute programs stored on magnetic tape.

An 18-key keypad whose functions are defined in soft-key fashion by the application program being run offers the operator all the choices necessary for the task at hand. Those choices and other operating instructions are displayed on the controller's 20-character light-emitting-diode display, and a hard copy of the test result can be printed by the controller's 20-column thermal strip-printer. Because the program contains only those portions of the operating system that are needed to run the application program, operators cannot accidentally change previously programmed routines.

In the program development mode, an optional set of read-only memory chips is inserted into the 4041. This firmware completes the operating system, letting users generate, edit, and debug original measurement programs (Fig. 2). Source code for the programs can be written with a keyboard that plugs into the 4041.



2. Bilevel operation. The operating system, stored in firmware, lets the 4041 controller support two levels of operation. The basic execute-only operating system runs measurement programs, and an optional ROM pack adds program-generation support.

More typically, any cathode-ray-tube terminal can be connected to the 4041 through its standard RS-232-C port for writing and editing source code. The controller can thus be optimized for a variety of applications when used with alphanumeric, raster-graphics, storage-graphics, or even color-graphics terminals. A page-size, hard-copy printer can also be interfaced with the 4041 controller through an optional serial RS-232-C port.

In addition to the serial ports, the 4041 has a standard IEEE-488-1978 port, plus an optional high-speed IEEE-488 port. The high-speed port employs a direct-memory-access architecture to increase the operating rate of IEEE-488 systems. The controller is connected to a TM 5000 series module cage by a standard IEEE-488 cable.

Strength in numbers

In addition to being tailored for two operating environments, the operating system can handle data types commonly used for controlling instrumentation systems. It handles any of three arithmetic data types: short (32-bit) floating-point numerals, long (64-bit) floating-point numerals, and integers. It will also accept data in engineering units and exponential form.

All numerics are handled as short floating-point values unless a different type of arithmetic is specified. However, long floating-point values might be selected for frequency difference calculations on data from the TM 5000 system's digital frequency counter, for example. Integer form, on the other hand, might be used in order to avoid assigning unnecessary memory storage space for simple integer data. Numeric data can be

TYPICAL 4041 CONTROLLER COMMANDS FOR TM5000 SERIES MODULES

Desired mode or function	Command
Set various voltage levels (for positive, negative, and logic supplies)	VPOS 15.0; VNEG 12.5; VLOG 4.95
Limit current output of positive and negative supplies to 0.7 A, of logic supply to 2.4 A	IPOS 0.7; INEG 0.7; ILOG 2.4
Set frequency (of function generator) to 2 MHz	FREQUENCY 2E6, or FREQ 2000E3, or FR 2000000
Set output (of function generator) for a pulse train with pulse width of 50 ns, period of 500 ns, baseline at ground, and pulse amplitude of 5 V (on asymmetical 2-MHz square wave with 2.5 V offset from ground)	MODE SQUARE; FREQUENCY 2E6; SYMMETRY 10; OFFSET 2.5; AMPLITUDE 5
Measure frequency (using counter/timer) with channel A terminated in low (50-Ω)impedance and in autotrigger mode	FREQ; CHA A; TERM LO; AUTO A
Measure rise time (positive slope) using (counter timer's) channel A terminated in high (1-MΩ) impedance	CHA A; TERM HI; SLO POS; RISE
Set range (of multimeter) to 20 V dc	DCV 20
Express ac voltage measurements (of multimeter) in dBm	ACV; CALC DBM

The first family of programmable modules

The next generation of modular instruments will be on display for the first time at Wescon this year. Called the TM 5000, the series will consist initially of the 11 major units shown here. Using the instrument modules and the controller, users now can easily configure programmable automated test system that meets their particular needs.

The measurement instrument set comprises three of the modules shown: the DM 5010 digital multimeter, the DC 5010 universal counter-timer, and the DC 5009 universal counter-timer. The $4\frac{1}{2}$-digit multimeter (1) is accurate to within 0.015% (dc voltage) and measures dc voltage, true rms ac voltage, and resistance. It performs math functions, such as nulling, averaging, and limits comparison. Readings of $4\frac{1}{2}$ and $3\frac{1}{2}$ digits can be sent on the bus at rates of 3 and 26 per second, respectively, for voltage and 1.6 and 7.1 per second, respectively, for resistance. The unit is priced at $1,995 and will be available 10 weeks after receipt of order.

The DC 5010 counter (2) reads signals to 350 megahertz, providing a resolution of 3.125 nanoseconds in the single-shot mode and 1 picosecond in the averaging mode. The $3,600 unit can automatically make rise- and fall-time measurements and has autotrigger and autoaveraging modes and probe compensation routines. It is available eight weeks after receipt of order.

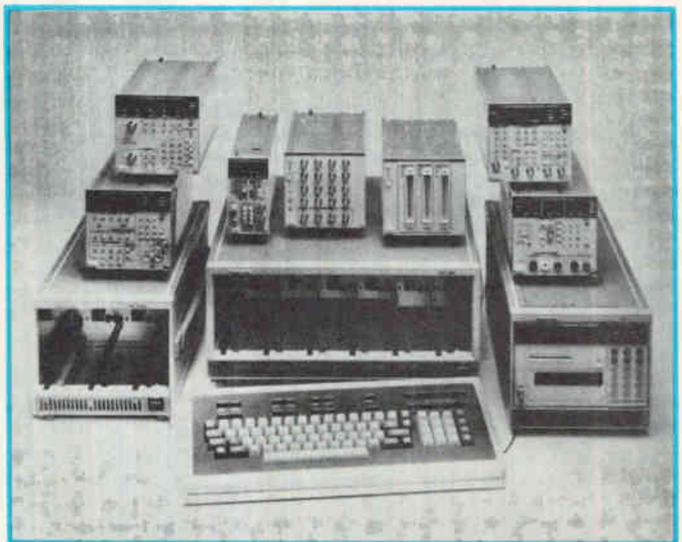
The only single-width module in the group, the DC 5009 (3), is similar to the DC 5010 except that its range is 135 MHz and that it does not make rise- and fall-time measurements automatically. A field-installable modification will upgrade an existing DC 509 to the $2,200 DC 5009, which is available from stock.

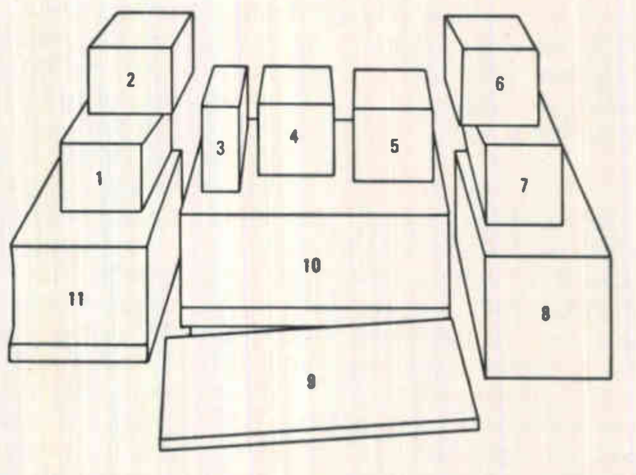
To connect the test system to the unit under test, two different types of modules are offered: the SI 5010 and the MI 5010. The SI 5010 (4) is an rf relay scanner priced at $1,850 that works with signals to 350 MHz. The unit's inputs can be configured in software as a single 16:1 group, as two 8:1 or as four 4:1 groups. Availability of the unit is 20 weeks after receipt of order.

The MI 5010 (5) is called a multifunction interface and can be configured using any or all of three types of cards: the 50M30 digital input/output card, which works with TTL-level signals; the 50M40 relay scanner card with 16 normally open relay closures; and the 50M50 development card, which lets users build their own programmable interfaces. The MI 5010, which has slots for three cards, costs $1350; the cards range in price from $375 to $575, and an MX 5010 extender, which attaches to the MI 5010 so that six cards can be used together, is priced at $650. Availability of all these items is 20 weeks after receipt of order.

The first signal source in the TM 5000 series is the FG 5010 function generator (6). Able to generate sine, square, and triangular waves to 20 MHz with amplitudes of 20 volts peak to peak, the $5,200 unit is accurate to within 0.1%. In addition to continuous output, it works in triggered, gated, counted-burst, and phase-locked modes and stores 10 setups. The FG 5010 will be available for delivery 24 weeks after receipt of order.

The triple power supply (7) puts out 0 to +32 V, 0 to −32 V, and for logic, 4.5 to 5.5 V. In addition to the output voltage level, the current limits for each supply are also programmable. The module is priced at $2,500; delivery takes three weeks.

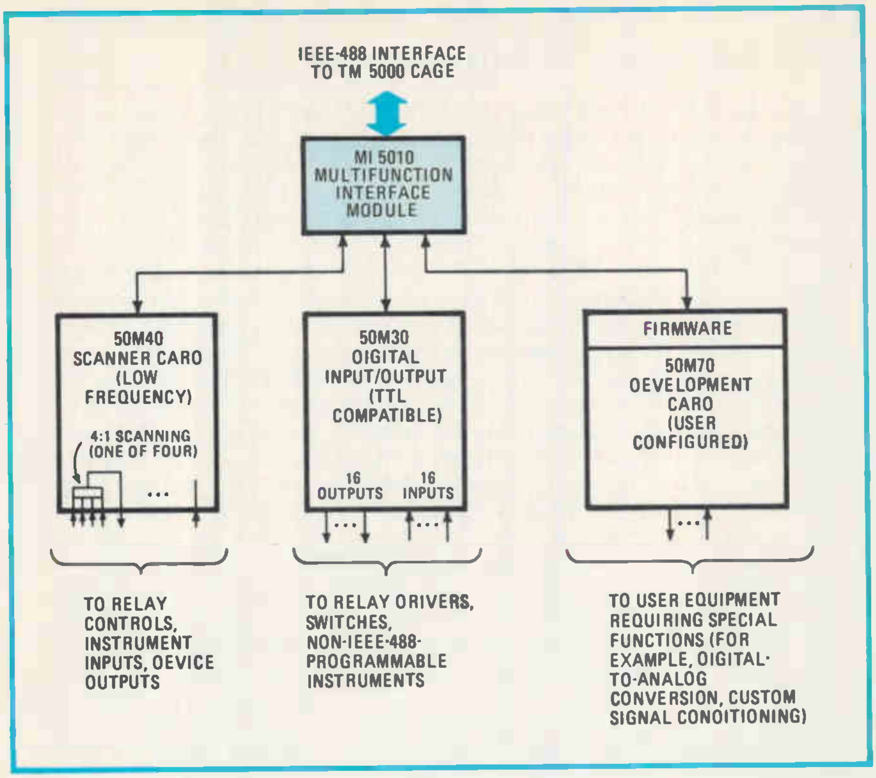




To manage all the modules, the controller (8) can be connected to the back of either the $995 TM 5006 (10) or the $700 TM 5003 (11) module cage with an IEEE-488 cable. The controller can be used for program development with its own $750 keyboard (9) and a $995 read-only memory pack, which expands the operating program. Alternatively, it can be used as an execute-only controller in which case it is priced at $4,995 with 10-week delivery.

With these components, the user can configure a system that fits both his needs and budget. For example, a small system, consisting of a controller, digital multimeter, counter, and power supply could be assembled for about $12,000. On the other hand, a full-blown system with maximum programming and display capability, multiple ports, function generator, and numerous scanners, measurement modules, and cages can run up to $35,000.

-Richard Comerford



3. Missing links. The TM 5000 series' multifunction interface module links the TM 5000 and the variety of special printed-circuit cards shown. The cards and module extend the system's programmability to devices lacking IEEE-488 compatibility.

entered in several formats, including signed and unsigned integers; signed and unsigned floating-point numerals; and binary, hexadecimal, and octal format.

The operating system works with simple mnemonic descriptors and thereby supports modular programming. With these descriptors, subprograms can be referred to by line names rather than numbers, and variables can be described with names up to eight characters in length (a delay command can be given as DELAY, and so on). Subprograms can be written without other portions of the main program having to be defined first, and the variables can be defined as local or global. Thus, keeping variables independent or passing them from main program to subprogram is a simple operation.

The operating system recognizes IEEE-488 commands, whether they be high- or low-level constructs, and optimizes them for high-speed execution. The language and operating system support the complete range of defined IEEE-488 states. Furthermore, they support processed-mode input/output functions, permitting the system to operate between requests and responses and thus decreasing total system response time.

Getting the routine down

Through a comprehensive error-handling scheme, the operating system can operate unattended, capturing all errors, recovering from errors, and supporting local error-handler routines. Using ROM firmware, it is even possible to expand the language set used by the operating system. Thus, the programming feature set can be embellished in the future. This expandability also permits common routines, with general-purpose appeal, to be canned in firmware and linked to other programs.

Ideally, a measurement programming language and a conceptually compatible set of instrument control commands would express IEEE-488 instrument control in self-explanatory terms. At the same time, it would possess sufficient depth to handle even the most complex test and measurement situation and would be particularly strong in dealing with interrupts and errors.

To meet these principal requirements, an enhanced version of Basic was chosen from among the common high-level languages for the TM 5000 system. Besides having an exceptionally successful track record, Basic can be learned easily and applied with minimal effort on the part of the user. In addition, it can be implemented for simple routines without the user necessarily understanding language as a whole, and it is backed by a readily available wealth of tutorial material.

Setting a standard

Together with its decision to use Basic, Tektronix adopted a corporate-wide set of standard codes and formats [*Electronics*, March 24, 1981, p. 131]. These codes are used in the TM 5000 series and in Tektronix' IEEE-488 line of digitizing oscilloscopes, spectrum analyzers, transient digitizers, and other products.

For the user, this means having to learn only one format, Basic syntax, and a uniform set of codes; a common message structure serves all the system's instruments. In contrast, a test system programmer typically has had to grapple with a half-dozen different sets of format and syntax or write a half-dozen software drivers to translate the various formats into a common format in order to program an IEEE-488 system.

The commands used to communicate with the instruments are in what might be termed engineering English. Since there is really no difference between the rationale for selecting commands from that for selecting front panel labels, the commands used are the same as the front panel labels—the engineering terms that are commonly used to refer to those functions.

For example, a typical command string to a function generator might be FUNCTION SQUARE; SYMMETRY 15. Not only are the commands easily grasped, but the program listings are highly self-documenting (see table). There is even a provision for programming in reverse. The LEARN mode permits an engineer more familiar with instrument operation than with programming to write a program by first physically setting the front panel controls for the desired conditions and then, with a single keystroke, converting the configuration into error-free program instructions. Again, these learned instructions in a program listing are high-level, easily readable, and self-documenting.

Programable functions

The initial set of programmable modules that the controller governs includes a full complement of the commonly used test and measurement products. In addition, programmable switching, signal routing, and special interface functions both simplify and speed up connection to the devices under test. All front panel functions—even ac or dc coupling and the trigger level—are programmable using the IEEE-488 bus.

For convenience, each instrument module's primary address can be read on its digital display by pushing the instrument identification button on the front panel. This feature eliminates having to locate the elusive, miniature dual-in-line-packaged switch tucked away behind or inside an instrument and then decoding its binary code into its decimal equivalent.

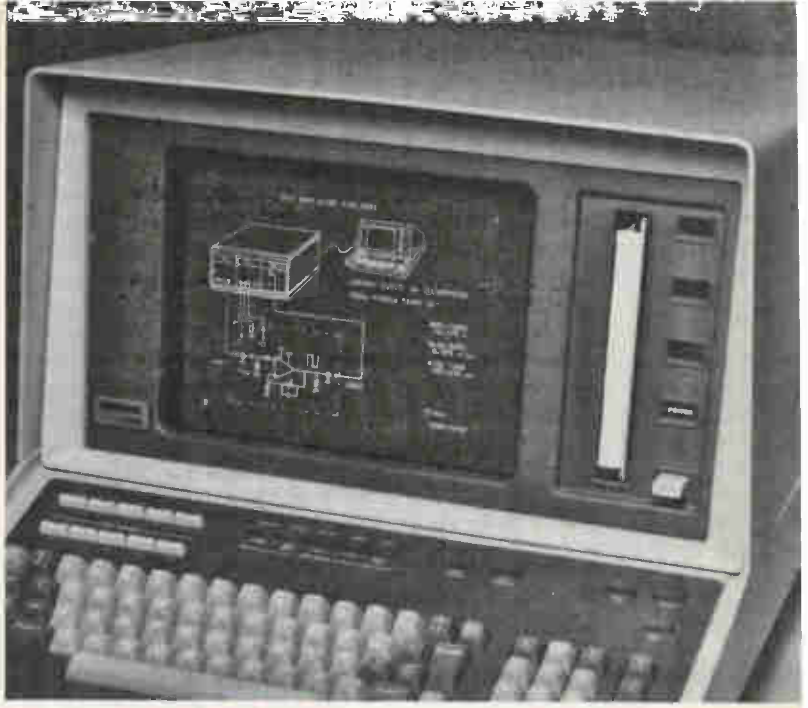
All the instruments, when first powered up, go through an extensive self-test and diagnostic routine for ROM, RAM, input/output, and the functionality of other blocks. If no internal error is found, the front panel controls of the instrument are engaged with a standard set of default settings. In addition, the service request line of the IEEE-488 bus is asserted to let the controller know that the instrument is available.

If an internal error is discovered, an error code is displayed on the instrument front panel, which would lead, with the help of the instrument's instruction manual, to the location of the specific problem. The self-test routine of any instrument module can also be triggered at a later time from the controller by the simple command, TEST.

The initial TM 5000 modules are shown in "The first family of programmable modules" on page 131. All of these modules are IEEE-488-compatible and microprocessor-based.

Function generator flexibility

In addition to the features common on most high-performance function generators, the FG 5010 20-megahertz function generator includes some unique ones. For example, the user can control through the bus or the front panel waveform symmetry in steps of 1% from 10% to 90% to create pulses and ramps. Users can also control the output waveform's phase in 1° increments from −90° to +90° with respect to a reference input waveform in a phase-locked mode or a control signal in



4. Show me. Using the TM 5000 series with a graphics computer or terminal lets the system instruct the operator using diagrams. Above, the display shows an operator where to connect power to a simple circuit card and probe the card for data needed by the program.

triggered, gated, or counted-burst modes.

The phase-locked mode automatically scans and locks onto any input signal supplied between 20 hertz and 20 MHz and will, if selected, issue a service request to the controller whenever it goes into or out of phase lock. Even when not in the phase-locked mode, the generator's frequency is maintained within 0.1% of the programmed value without expensive frequency-synthesis techniques.

The FG 5010's microprocessor continually monitors the generator's frequency with a conventional frequency counter technique, using the processor's quartz clock as a reference. It then compensates for variation in the loop current sources with any additional current offset required to keep the loop precisely on frequency.

Any absolute number can be set for any parameter by using the front panel keypad, the bus, or the front panel's increment-decrement buttons. These buttons permit users to smoothly increase or decrease the parametric settings in either fixed incremental steps or an accelerating speed mode.

The FG 5010 also accepts ramp inputs for generating true analog sweeps, as well as inputs for amplitude and frequency modulation.

Plus or minus 1 picosecond

The 350-MHz DC 5010 universal counter can resolve repetitive time intervals to 1 picosecond—at present the highest resolution available. This wide bandwidth permits the counter to make frequency measurements or such flexible totalizing measurements as channel A plus channel B and channel A minus channel B of pulse trains with pulse widths as narrow as 1.43 nanoseconds.

In addition, the DC 5010 also functions as an intelligent counter. In the autotrigger mode, for instance, the counter determines the maximum and minimum peak values of the input signal and sets the trigger levels at the 50% point. In the rise-fall mode, it sets the start channel at the 10% point and the stop channel at the 90% point.

The peak signal levels can be measured by the DC 5010 and sent to the controller. Thus, the counter can function as a peak-reading voltmeter across its full 350-MHz bandwidth. In the auto-averaging mode, the DC 5010 selects the maximum averaging factor that still permits it to update the display about three times per second. Unlike conventional counters, whose averaging factors can only be set in powers of 10, the DC 5010's dual-register, microprocessor-based architecture lets the counter choose any averaging factor it desires.

A null feature can be selected in any mode. In the time-interval mode, it will remove any time differential mismatch of the two channels and associated external probes or cabling. Therefore, the value displayed is the true time interval at the probe tips.

A probe-compensation feature (also available on the DC 5009 135-MHz universal counter) permits accurate adjustment of attenuation-probe compensation capacitors—a capability that has never before been available on a counter. Using probes without correct compensation can result in gross errors in time interval measurements.

Meter magic

In addition to measuring dc voltage, true rms ac voltage (either ac or dc coupled), and resistance, the DM 5010 4¼-digit multimeter has a diode test function that forces a 1-milliampere current and measures the resulting voltage drop.

The DM 5010 is accurate to within 0.015% dc for 4½ digits, but can be set to work faster (26 readings per second) with 3½-digit resolution. It includes such special functions as a null feature that zeros out the lead resistance in ohm measurements or enables quasi-differential voltage measurements and the ability to average up to 19,999 readings, instead of sending them to the controller for processing. Other capabilities include direct decibel conversion to dBm or to any arbitrarily selected value as the 0-dB reference, and a comparison mode wherein upper and lower limits can be entered. In the latter mode, the DM 5010 compares its reading to the limits and displays the results as PASS, HI, or LO.

Power report

The PS 5010 triple power supply has three defined modes for each of its three supplies: 0 to −32 volts, 0 to −32 V, and +4.5 to +5.5 V. These modes are voltage-regulated, current-limited, and unregulated. The supply would enter an unregulated state if, during a test procedure, it were connected to another power supply and expected to sink more current than it is designed to sink.

The PS 5010 also can be programmed to notify the controller, using a service request whenever it changes modes. Thus, the controller can halt a procedure to take some other course of action when an unusual load places the power supply in an unacceptable condition. In contrast, most supplies used in IEEE-488 systems are listener-only devices, making it impossible to determine whether they are actually following instructions unless they are monitored with additional instruments.

In the voltage-regulated mode, the two wide-range outputs of the power supply can be programmed in increments of 10 millivolts from 0 to 9.99 V and in 100 mV steps from 10 to 32 V. Current can be programmed in 50-milliampere increments from 50 mA to 1.6 A. The +4.5-to-+5.5-V supply is a logic supply programmable in 10-mV increments; its current limits can be set over a 100-mA-to-3-A range in 100-mA increments.

To fully automate a set of tests, it is necessary to control the connection of instrument inputs and outputs to various test points on the device under test. The SI 5010 rf scanner can perform that function on signals with maximum frequency of 350 MHz.

Rf signal switching

The module consists of coaxial rf relays that can be software-configured into either one 16:1, two 8:1, or four 4:1 configurations. It also contains a real-time clock and a buffer for storing and executing sequences of commands. Consequently, it is possible for the controller to download a sequence to the rf scanner, such as "wait until 9:32 a.m. and then close relays 1, 3, 4 and 2 in sequence at the rate of once per second for the next hour."

This buffering feature is also useful when set for a group-execute trigger. Following the trigger, the SI 5010 will carry out its routine without further instructions from the controller.

Plugging in

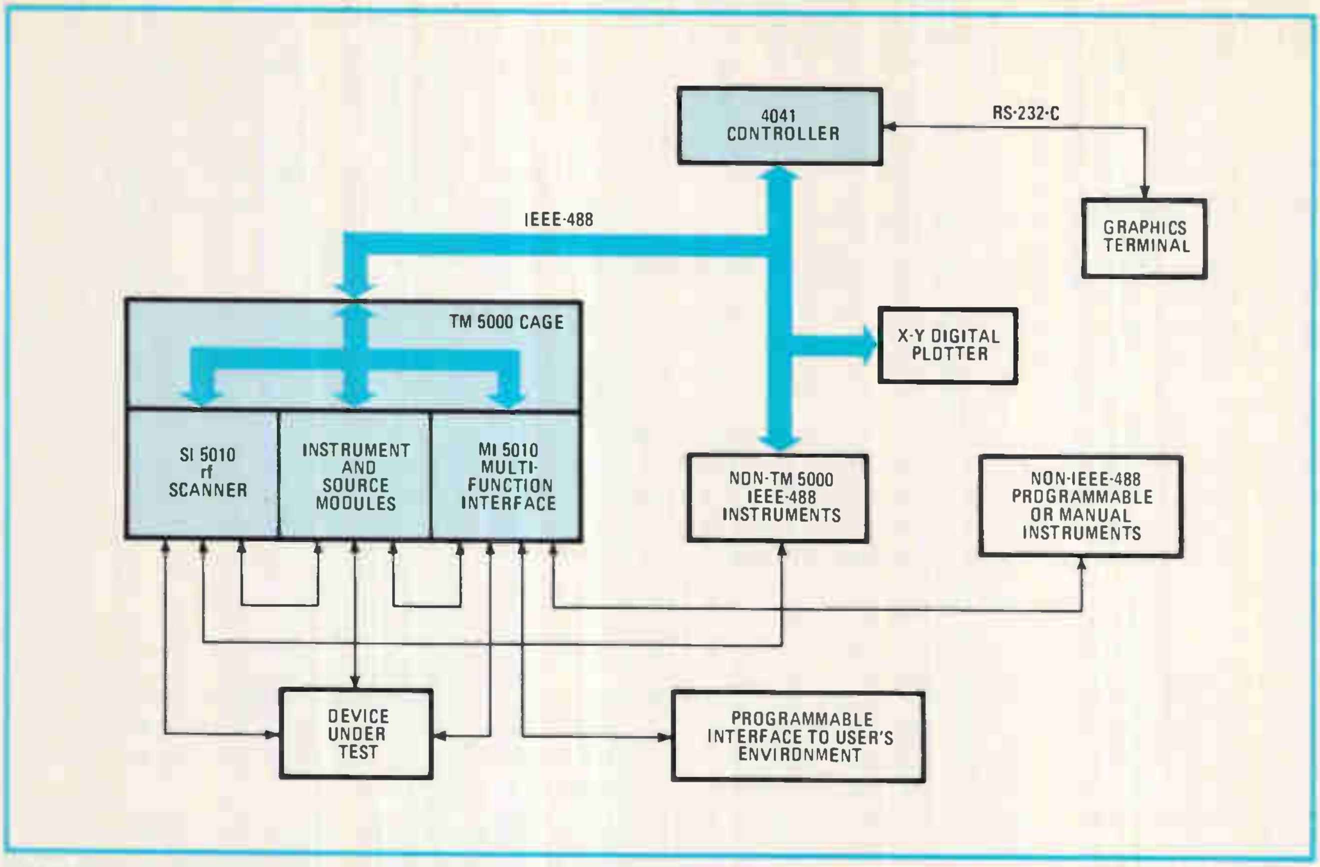
Users may wish to connect an IEEE-488 instrumentation system to other non–IEEE-488 programmable systems. Or they may wish to interface the IEEE-488 system to relay drivers, foot switches, binary-coded-decimal–output data lines, and the like. Other users, particularly specialized test systems houses, need to be able to add their own special functions, such as unusual digital-to-analog, analog-to-digital, timing, and communications functions. For these reasons, the initial 5000 series set includes a special interface module.

The MI 5010 multifunction interface module and its MX 5010 multifunction interface extender differ from the other modules in that up to three special printed-circuit card modules can be plugged into their front panels, as shown in Fig. 3. These special card modules comprise the programmable interface between the device under test and both the MI 5010 and MX 5010. In turn, the MI 5010 and MX 5010 act as the interface between the card modules and the TM 5000 system. Up to six cards can be controlled at a single IEEE-488 address.

The first three card modules available are a low-frequency scanner, a digital I/O card, and a development card. The low-frequency scanner card contains 16 mercury-wetted relays; 16:1, 8:1, or 4:1 interface configurations can be selected using jumpers. The scanner card can control larger relays, switch the multimeter's input among several signal points, and serve other control and low-frequency scanning applications.

The digital I/O card has 16 digital input and 16 digital output channels. These TTL-compatible channels can connect the system with delay drivers, switches or custom keyboards or accept BCD data, static binary words, and the like from non–IEEE-488 instruments.

The third card is a development card the system



5. New business. The instrument modules and the controller comprise the simple building blocks for designing custom systems such as the one shown above. Those familiar with the needs of a particular industry can easily configure and program a custom system.

designer can use in preparing custom functions. The rear portion implements all the addressing, handshaking, serial-to-parallel conversion, and decoding from high-level command functions and provides the interface between the card and TM 5000 system.

The interface between the card and the user's device under test consists of 32 bits of simple, static registers. The remainder of the card, about 20 square inches, is a blank circuit-board pattern for user circuitry.

Custom functions that can be implemented might be d-a and a-d converters, special word recognizers or generators, or numerous others needed to complete a customized automated system. The MI 5010, like the SI 5010, includes a real-time clock, buffer storage, and execution capabilities, which help reduce bus traffic and controller overhead.

Graphic detail

In research, development, and design, a graphic representation of processed measurement results is quite often the ideal format. Graphics can be added to the TM 5000 series in two ways: a 4052 graphic computing system could be substituted for the 4041 controller or a graphics terminal could be used in conjunction with the 4041. Either configuration can easily plot logarithmic or linear representations of such relationships as gain or phase versus frequency. Graphics such as those shown in Fig. 4 could also be used as a probe guide for less skilled operators during maintenance or calibration procedures.

Electronic testing techniques are useful in many fields where the users are not otherwise familiar with electronics. For example, electronics testing plays a significant role in calibrating process control systems in the petrochemical industry and in maintaining large stationary engines, turbines, and pumps.

Sometimes the parameters to be measured are electrical. In many cases, they are physical parameters, such as pressure, vibration, displacement, temperature, and the like, converted into electrical signals by transducers.

Best of both worlds

A number of systems houses combine electronic expertise with an in-depth knowledge of the needs, techniques, and vocabulary of those nonelectronic industries. The TM 5000 series with its 4041 controller offers such systems houses an attractive set of tools for providing specialized, turnkey systems to their customers like the one shown in Fig. 5. The system's compact, lightweight packaging is extremely adaptable to maintenance activities in the field, at remote locations, or in a plant.

The 4041 controller with its DC 100 cassette program recorder permits systems-house programmers to write specialized software applications programs for industrial clients. Special functions required also can be built into the system using the 50M70 development card. An overlay card on the user-specified 4041 keypad can be used to label these keys in the vocabulary of a target industry. In addition, the output format can be programmed for conversion to units of measurement more pertinent to the specific application than a standard electrical output. ☐

Phase-locked loops replace precision component bridge

by Vilas Jagtap and Vidyut Bapat
Peico Electronics and Electricals Ltd., Pune, India

For accuracy and repeatability in measuring passive components, a resistor-capacitor bridge is difficult to surpass. But its one drawback is its prohibitively high cost. An inexpensive alternative is a circuit that uses two off-the-shelf phase-locked loops to perform this function accurately to within 0.1% and with a resolution of 0.01%.

As shown in the circuit, which is configured to measure capacitance, the 565 phase-locked loop, A_1, generates a frequency, f_{in}, corresponding to the component under test, C_x. This signal is then brought to the input of a second loop, A_2, which itself generates a reference frequency, f_{ref}, corresponding to component C_s. The output of A_2 then produces a signal proportional to the difference frequency. The difference frequency, $f_{in} - f_{ref}$, is amplified by the 530 operational amplifier, with the resulting signal applied to a zero-center meter that can be calibrated in terms of the percentage difference between C_x and C_s.

The frequency at which the 565s oscillate is determined by the capacitance between pins 1 and 9 (C_x, C_s) and the resistance between pins 8 and 10 (see the 565 data sheet). A wide range of values may be determined simply by adjusting the 4.7-kilohm potentiometer–2.2-kΩ resistor combination that is connected between these latter pins.

When resistances are compared, only four components need be changed. C_x becomes R_x, C_s becomes R_s, and variable capacitors replace the previously mentioned potentiometers.

Calibration is equally simple in either the capacitor-measuring or the resistor-measuring mode. Since the 565's frequency of oscillation can be within ±10% of a nominal value for a given set of frequency-determining components, both oscillators should initially be aligned by setting $C_x = C_s$ (or $R_x = R_s$). The potentiometers (or variable capacitors) should then be trimmed for a null on the meter. □

Engineer's notebook is a regular feature in Electronics. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.

Computer notes

TRS-80 program simplifies design of PROM decoders

by Gideon Gimlan
Loral Electronic Systems, The Bronx, N. Y.

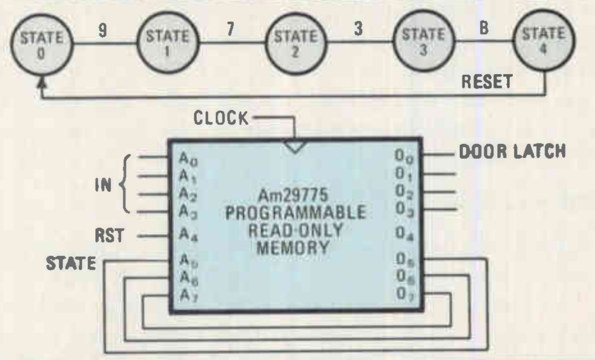
Coding data into programmable read-only memories is tedious when done by hand. This TRS-80 Basic program takes the drudgery out of the effort. Although performing a myriad of tasks, its major advantages are simplifying the design of PROM decoders by providing documentation of the design, simulating sequential-state machines, and preparing the data for immediate PROM burn-in.

To understand the program and its relation to character-generation redundancy or the sequential-state machine on which this program is based, consider the typical video-display circuit shown at the right. On it, the address lines are designated as inputs and the data lines form the outputs. Each input combination has a unique output, but in general practice, redundancy occurs frequently because of the so-called "don't care" condition.

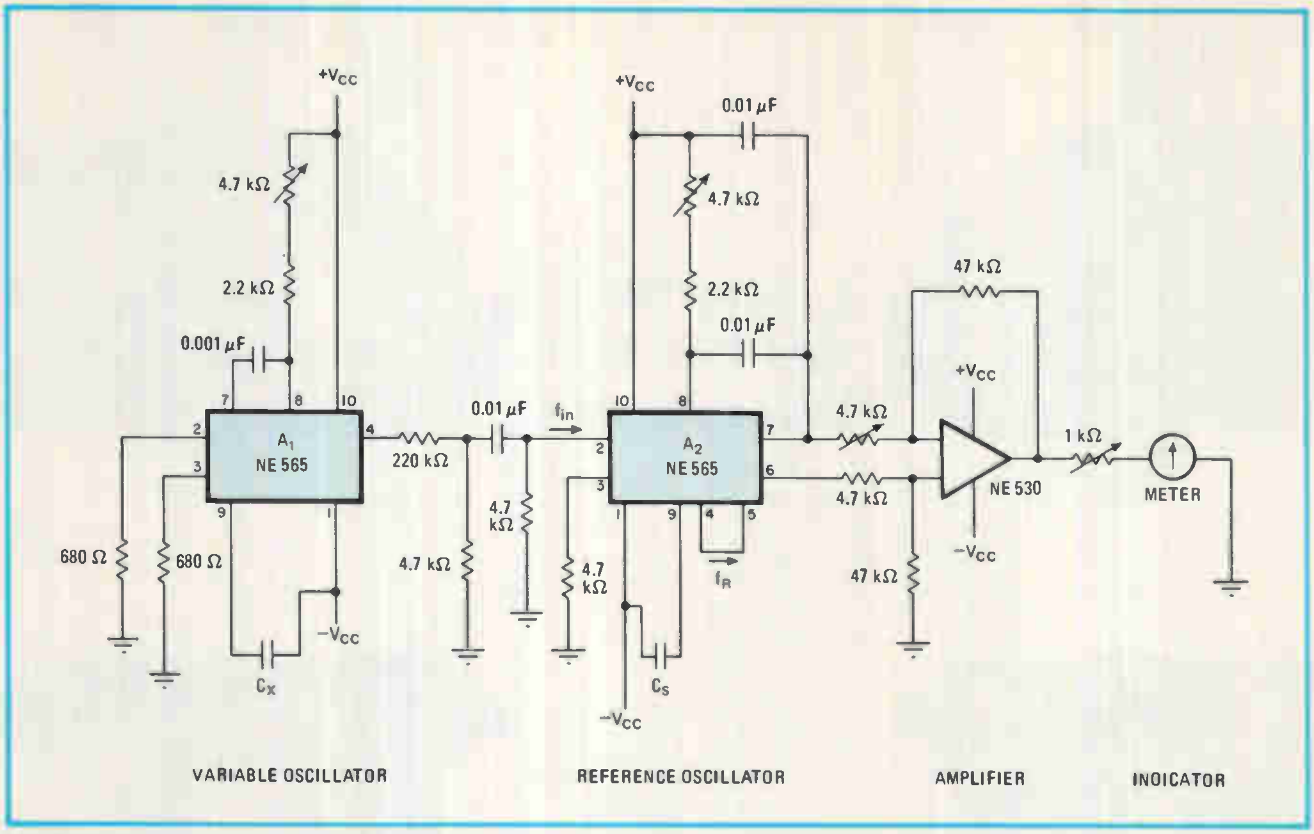
In this example, a 5-bit ASCII code of the character to be displayed is placed on the least significant address lines of the PROM, as shown. The 3 most significant bits are connected to a row counter that increments from 0 to

GENERAL PROGRAM TECHNIQUE FOR CHARACTER GENERATION

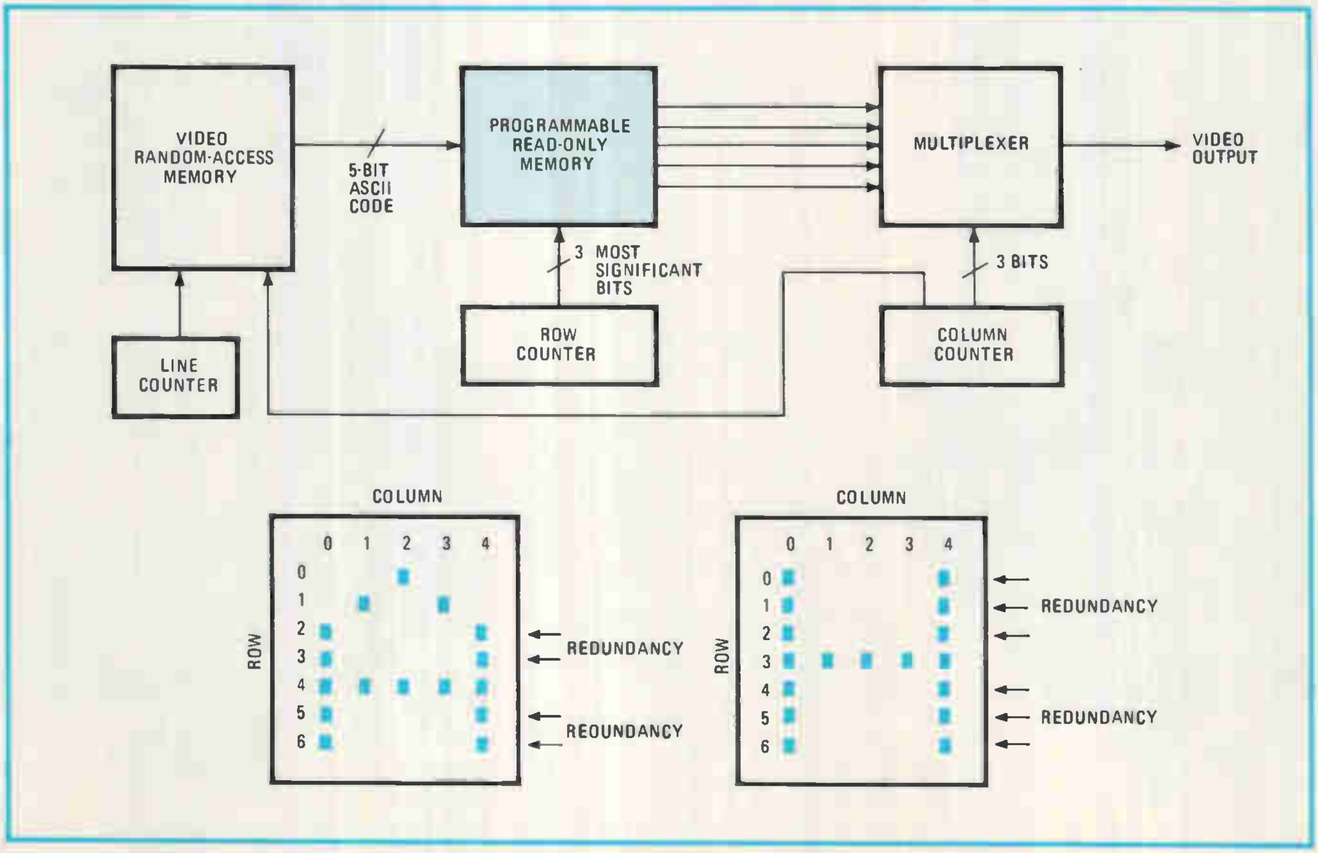
```
1000 C(1) = ASC("A") + ROW*0  :  0(1) = B(2)
1010 C(2) = ASC("A") + ROW*1  :  0(2) = B(1) + B(3)
1020 C(3) = ASC("A") + ROW*4  :  0(3) = B(0) + B(1) + B(2) + B(3) + B(4)
1030 C(4) = ASC("A")          :  0(4) = B(0) + B(4)
1040 C(5) = ASC("H") + ROW*3  :  0(5) = B(0) + B(1) + B(2) + B(3) + B(4)
1050 C(6) = ASC("H")          :  0(6) = B(0) + B(4)

1100 FOR I = 1 TO 12B         :  R(I) = B(B) - 1 : NEXT
11B0 R(4) = B(5) - 1          :  R(6)= R(4)
```

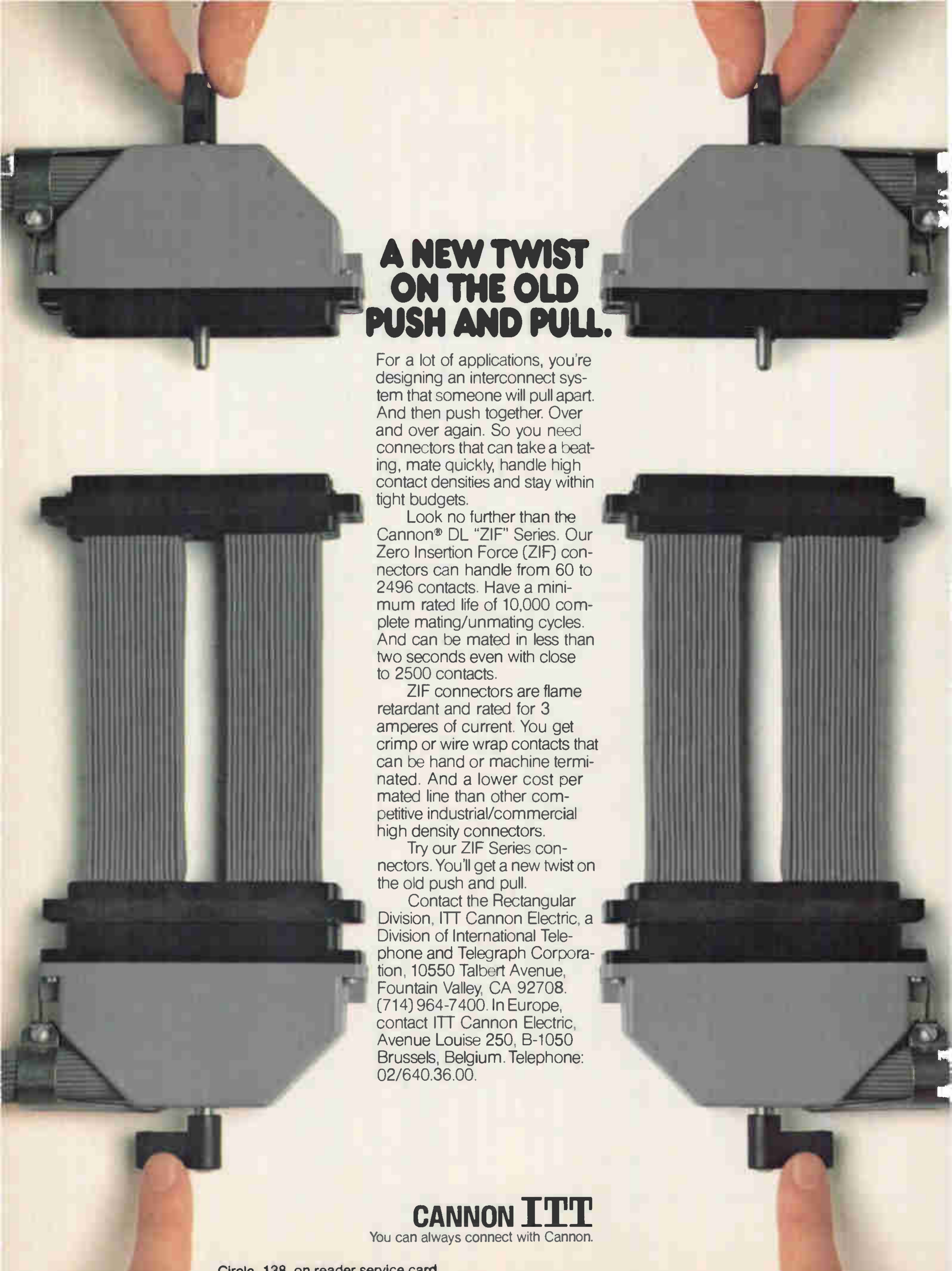


Basic burn-in. Writing data into a PROM with TRS-80 Basic, as grasped with the aid of a video-display scheme (right) and the general programming technique (top), is relatively simple for state machines because of their inherent character-generation redundancy properties. The technique is easily extended to practical programs and the one shown (immediately above) is a combination lock that opens when the sequence 9-7-3-8 is entered.



Matched? Phase-locked loops wired in series indicate percentage deviation between unknown and reference capacitors or resistors. A_2's output represents the difference between a standard and variable frequency, each of which is determined by C_s and C_x, respectively.





Circle 138 on reader service card

TRS-80 PROGRAM FOR READ-ONLY MEMORY GENERATION OF SEQUENTIAL-STATE MACHINES

```
10 '-- PROM CAD
60 CLS:DEFINTA-Z
70 CLEAR 1000
80 DIM C(255),R(255),O(255),WD(255)
90 X$=CHR$(23):N$=CHR$(28):EL$=CHR$(30):ES$=CHR$(31)
91 ' 32/LINE   64/LINE    ERASE LINE    ERASE SCREEN
92 UB$=CHR$(18):UF$=CHR$(19):UX$=CHR$(8)
93 '  CURSOR BACK, FORWARD, BACK & ERASE CHAR
94 DIM B(15):FOR I=0TO15: B(I)=2↑I  :NEXT

100 PRINTX$:PRINT"PROM BASED STATE MACHINE"
110 PRINT STRING$(24,"-"):PRINT:PRINT
120 PRINT"THIS PROGRAM GENERATES THE DATA"
130 PRINT"FOR A SEQUENTIAL STATE MACHINE."
140 PRINT
150 PRINT"THE CONDITION STATEMENTS START"
160 PRINT"AT LINE 1000"
170 PRINT"C(I)=  1'S & 0'S   R(I)=REQ'D BITS"
180 PRINT"ENTER 'L' TO LIST THE CONDITIONS "
190 PRINT"ENTER 'R' TO GENERATE TABLE"
200 I$=INKEY$
210 IF I$="L" THEN CLS:LIST 990-1005
220 IF I$="R" THEN CLS:PRINT"EXECUTING":GOTO 1000
230 GOTO 200

500 FOR A=0 TO AX:' (PROCESS ENTIRE ADDRESS SPACE)
505 PRINT@50,A
510 I=0
520 I=I+1:IF R(I)=0 THEN WD(A)=OX :GOTO540
530 IF (A AND R(I)=C(I) THEN WD(A)=D(I) ELSE 520
540 NEXT A
550 PRINT"NOW FINISHED. LAST ADDRESS=";AX
560 INPUT"DO YOU WISH TO LIST PROM CONTENTS (Y/N)";I$
564 IF I$="N" THEN 580
570 FOR A=0TOAX:PRINTUSING"###";A;:PRINT") ";WD(A)," ":
    NEXT A
```

```
580 PRINT"DO YOU WISH TO SIMULATE THE MACHINE?"
590 PRINT"  'Y' = YES   'N' = NO"
600 I$=INKEY$
610 IF I$="N" THEN LIST 1000-
620 IF I$="Y" THEN 800
630 GOTO 600
800 CLS:PRINT"WE START AT STATE NUMBER 0":PRINT:A=0:SP=0:ST=0
805 PRINT"STATE=";SP;TAB(20)"OUTPUT=";WD(A);TAB(50)"INPUT=";
810 INPUT IN
815 A=ST+(IN AND (B(0)+B(1)+B(2)+B(3)+B(4)))
820 ST=WD(A) AND (B(5)+B(6)+B(7))
821 SP=ST/B(5)
825 IF IN>255 THEN STOP ELSE 805

990 CONDITION STATEMENTS BEGIN AT LINE 1000
991 CHANGE THESE LINES TO CREATE A NEW SYSTEM
992 C(I)=CONDITION BITS, UP TO 16 BITS
994 R(I)=REQUIRED BITS, THOSE OF C(I) THAT ARE NOT
955      DON'T CARE BITS AND MUST MATCH THE PROM ADDRESS
996 O(I)=PROM OUTPUT WORD IF A CONDITION MATCH IS FOUND
997 OX =DEFAULT OUTPUT IF NO MATCH IS FDUND
999              ---- CONDITIONS ----
1000 IN=B(0) : RST=B(4) : STATE=B(5) : '  -(DEFINE INPUT BITS
1001 NXT=B(5) : LATCH=B(1) : '            -(DEFINE OUT  BITS
1002 N=8 : AX=B(N)-1 : ALL=AX : '         -(DEFINE NO OF BITS
1003 '
1004 C(1) = RST : R(1) = RST : O(1)=STATE*0: ' -(IF RESET
1005 C(2) = 9*IN + STATE*0    : O(2)=STATE*1: ' -(IF IN=9
1006 C(3) = 7*IN + STATE*1    : O(3)=STATE*2: ' -(IF IN=7
1007 C(4) = 3*IN + STATE*2    : O(4)=STATE*3: ' -(IF IN=3
1008 C(5) = 8*IN + STATE*3    : O(5)=STATE*4 + LATCH
1009 C(6) =      STATE*4  : O(6)=STATE*4  :R(6)=STATE*?
1010       R(2)=ALL : R(3)=ALL : R(4)=ALL : R(5)=ALL
1020 OX=STATE*0 + B(2) : ' DEFAULT TO STATE 0
2000 GOTO 500
2001 END
```

6, keeping track of which row of a five-by-seven-dot matrix the system is on.

The data word to be burned into each PROM location is determined by a set of condition equations. For each input combination, the program scans the condition-equation list for a match. If the input condition is met, then the associated output word is placed in the PROM's desired memory location.

For example, to generate the dot matrix shown for the character A presented at the inputs of the PROM, the equations in the figure commencing at line 1000 and ending at line 1030 are entered. The C(I) matrix indicates the bits that must be at logic 1 in the input data, O(I) is the associated output word, and B(N) is the binary value of each data bit and is equal to 2^N.

For the character H, only two lines of data are needed—at locations 1040 and 1050 in the general programming technique—because of the redundancy in the required output data. That is, rows 0, 1, 2, 4, 5, and 6 of the H are all the same. Only row 3 is important. Bits that are required to meet any condition, be they 1s or 0s, are designated by the R(I) matrix. Those input bits that are not required are designated "don't care" bits, as seen at lines 1100 and 1180 in the TRS-80 program.

With this information, the practical implementation of ROM generation for a sequential-state machine that functions as a combination lock may be considered (see program listing). In this example, the lock opens a latch when the sequence 9-7-3-8 is entered, as shown in the bottom half of the figure. Otherwise the sequencer returns to state number 0. The hardware implementation is shown at the bottom of the program. □

Engineer's newsletter

Unix texts will aid users

A major problem in adapting the popular Unix computer operating system to new applications is that its documentation is, by and large, written for experts only. Little more on Unix other than Bell Laboratories' technical papers is available, although the overall reaction to this C language–based system has been extremely positive despite the apprehension of users. Help is on the way, however, for **the first quarter of 1982 will see the publication of an introductory Unix text** by Osborne/McGraw-Hill. Written by Jean Yates of the consulting firm of Gnostic Concepts Inc. and Rebecca Thomas, a software development specialist at MicroPro International Corp., the book is to be followed by a second text that will be a reference guide for Unix programmers. Call Osborne at (415) 548-2805 for further information.

Radio's ac adapter aids *in situ* charging of NiCad batteries

Although rechargeable batteries of the nickel-cadmium variety would seem at present to be thc ideal power source for portable radios, tape recorders, and so on, few if any of these appliances come equipped with any more than regular batteries and an ac adapter. But NiCad batteries can be used and recharged in these devices without removal from the appliances' enclosure, notes Cass Lewart of System Development Corp., Eatontown, N. J., simply by modifying the ac adapter.

Lewart **solders a 10-to-50-Ω resistor across the two contacts of the adapter** that are normally connected together when it is not in use, then installs the batteries. The selection of resistor value is determined with the aid of a milliammeter to measure the dc charging current of the NiCad batteries with the equipment off and the adapter in. The charging current should be about 50 mA for AA cells and proportionally higher for C or D cells. Lewart recommends recharging the larger cell types for approximately 10 hours. A word of caution, however: don't use the modified adapter with standard nonrechargeable types, as the batteries will most surely corrode.

Periodical speaks to speech engineers

The first magazine devoted to man-machine voice communications, Speech Technology, will premiere this fall. Published by Media Dimensions of New York, **the quarterly will deal exclusively with the latest advances in speech synthesis and recognition.** Written in practical, scientific terminology useful to engineers, scientists, educators, and managers, each issue will cover such topics as linear predictive coding, specific word-recognition systems now in operation, and the use of speech recognition for implementing business transactions by telephone. How-to articles will discuss such subjects as adding word recognition to an existing computer system and applications of interesting devices like the voice-actuated door lock. Editing the periodical will be Richard H. Wiggins, who helped develop systems for the analysis and synthesis of speech at Texas Instruments Inc.

A one-year subscription (four issues) costs $50. For those subscribing prior to publication, however, there is a special introductory price of $40, which is available until Aug. 31. Checks should be made out to Media Dimensions Inc. and sent to the company at 525 East 82nd St., New York, N. Y. 10028. Call Stanley Goldstein at (212) 680-6451 for more information.

-Vincent Biancomano

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GENERAL ELECTRIC

Circle 1[illegible]2 on reader service card

Pulse/function source delivers 50 MHz

Programmable generator and low-cost 20-MHz manual unit gain flexibility by sharing pulse and function features

by John Gosch, Frankfurt bureau manager

Adding clout to their line of pulse generators, designers at Hewlett-Packard GmbH in Böblingen, West Germany have created a pair of instruments, the HP 8116A and 8111A, both of which provide both pulse and function generation. As a result, features that are common for one type of generator are made available to the other. For example, the modulation, sweep, and voltage-controlled–oscillator modes of the function-generator portion, normally not found on a pulse generator, may be used on the pulse-generator portion, enhancing versatility, says Giorgio Dina, product-marketing engineer for the instruments.

The two instruments also meet users' demands for more trigger capabilities and digital characteristics, as well for as easier handling.

The 8116A is a programmable instrument with a frequency range of 1 Hz to 50 MHz, "wider than that of competitive pulse-function generators." Dina says. A compact unit weighing only 13 lb, it marries sine-, triangular-, and square-wave capabilities to a true pulse mode. The pulse widths are variable from 999 ms down to 10 ns and have rise and fall times of less than 6 ns.

To bow in mid-August, the 8116A (shown) will sell for $3,440 in the U. S. For an additional $430, users can get the 001 option, which encompasses hold, counted-burst, and logarithmic-sweep modes. This option covers the full 1-mHz-to-50-MHz range and is applicable to all waveforms the unit generates.

The 8111A, also slated for a mid-August debut, is a simpler version of the 8116A. It is a manually operated unit weighing only 10 lb and also produces sine, triangular, and square waves as well as pulses. The pulses are variable from 100 ms down to 25 ns and have rise and fall times of 10 ns. The 1-Hz-to-20-MHz instrument will cost $1,775 in the U. S. A counted-burst option adds another $375 to that price.

As a function generator, the 8116A produces the three waveforms, over its entire frequency range and at amplitudes of up to 32 V peak. A duty cycle variable from 10% to 90% in 1% steps provides linear ramps and asymmetrical sine and square waves to test amplifier linearity, servomechanisms, dc motors, industrial controls, and a host of other parameters, devices, and systems.

Haver waveforms may be generated in each of several external modes such as trigger, gate, sweep, and burst modes. A second input is available for modulation control. Modulation and external control can simultaneously simulate any desired waveform.

In a pulse-generator application, pulses are variable down to 10 ns, with 100-ps resolution in the lowest range. The 6-ns pulse rise and fall times make the instrument well suited for testing fast logic devices such as TTL, integrated-injection-logic, complementary-MOS, and n-channel MOS circuits. Burst, pulse-width modulation, and pulse-restoration controls are other versatility-enhancing features.

For all its capabilities and for all the types of waveforms it produces, the 8116A is easy to handle, thanks in part to a self-prompting menu. After selection of the desired mode and waveform, the needed parameters are indicated by back-lighting the appropriate parameter key label. Parameters are entered with just four vernier buttons. If a parameter is incorrectly set, an error-recognition feature alerts the operator by flashing a light on the panel.

For example, if in manual operation the sine-wave function is selected, the four keys that are setting the frequency, duty cycle, amplitude, and offset are illuminated. For pulses, the same four keys are used for setting the pulse width (instead of duty cycle), the frequency, amplitude, and offset. The last two parameters may be converted to high- and low-level values by pushing the amplitude and offset key a second time. An auto-vernier mode allows each parameter to be swept during automatic response measurements as may be needed in threshold and frequency-response tests.

Fully programmable via the IEEE-488 interface bus, the 8116A is useful both on the bench and in production test systems. In production, the unit comes in handy for long-term parameter testing, complex measurement sequences, and multiple repetitive tests.

All operations are programmable with simple statements that use parameter mnemonics on the front panel. In case of a programming error, an error statement gives the operator detailed error information to facilitate program corrections. Self-tests may be executed with a statement for routine system checks.

In the logarithmic sweep mode that is provided by the 001 option, start and stop frequencies, as well as sweep time, may be programmed. With the counted-burst feature, a programmed number of cycles or pulses can be produced in the external-burst mode on every trigger for all waveforms. For sine, triangular, or square waves, the trigger signal may be internally generated with a programmed repetition rate.

Hold it. In the hold mode, phases and events like those encountered during stress tests, for example, can be identified easily. This mode allows freezing the very low-frequency drive signal at its momentary amplitude level. To continue from that level, the critical parameter has been investigated or recorded.

The 8116A's lower-cost counterpart, the 8111A, also produces the three waveforms over its full frequency range (1 Hz to 20 MHz) at amplitudes up to 32 V peak to peak. Combined with error recognition, the digital readout contributes to operating simplicity and speed. Its waveform and pulse capabilities, Dina notes, make the 8111A an excellent signal source for design, production testing, and servicing.

Hewlett-Packard Co., 1501 Page Mill Rd., Palo Alto, Calif. 94304 [338]

Hewlett-Packard SA, P. O. Box CH-1217 Meyrin 2, Geneva, Switzerland [339]

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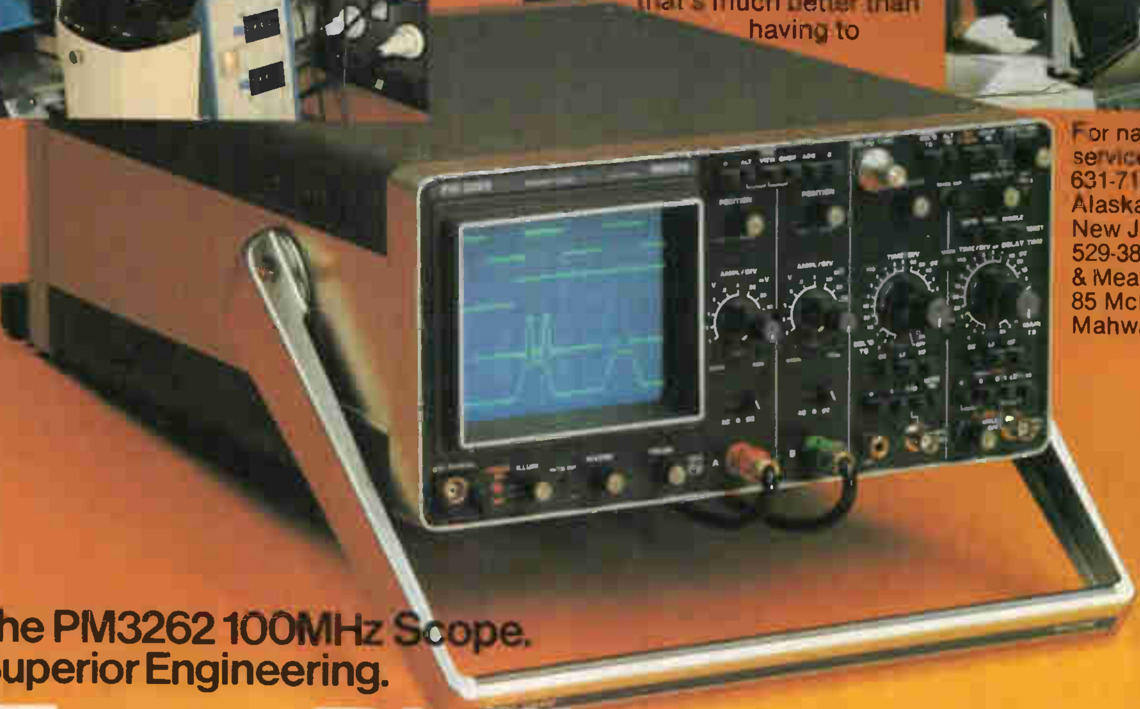

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Circle 145 on reader service card

Data acquisition

Board links Q bus to IEEE-488 gear

Interface card accommodates data-acquisition systems; so do Winchester drive options

Aided by a new interface board from Data Translation, the Q bus of Digital Equipment Corp.'s LSI-11/2 and /23 microcomputer systems can communicate with the IEEE-488 general-purpose instrumentation bus. Although available as a separate hardware and software package, the dual-width board's chief market should be as an enhancement to Data Translation's Lab-Datax laboratory data-acquisition systems, says Stephen L. Mullen, product marketing manager for laboratory and scientific systems. He adds that Lab-Datax, based on DEC's LSI-11, has been installed in about 50 systems since its introduction [*Electronics*, Oct. 11, 1979, p. 202].

A single DT2791 board links Lab-Datax with as many as 14 instruments adopting the IEEE-488 bus. Multiple boards may load into one Lab-Datax, or several DT2791 boards running in different systems may communicate among themselves over one IEEE-488 line.

The DT2791 offers software-selectable talker, listener, and controller modes on the IEEE-488 bus under the management of the Lab-Datax system processor. In the controller mode, it performs parallel polling and other controlling functions specified by the bus. It also responds to parallel-polling in multiple-controller environments. It further supports talker or extended-talker and listener or extended-listener interface functions in establishing handshaking communications.

A diskette furnished with the DT2791 holds a device-control subroutine, a device-support subroutine, and a utility program. Both subroutines, supplied as macroinstruction source files, are Fortran-, Basic-, or macro-callable under the DEC RT-11 operating system. The device-control subroutine, providing IEEE-488 management services, may directly control the DT2791 or operate in conjunction with an RT-11 device handler from Data Translation.

With this control subroutine, users may control the board at a primitive level, but most of them will probably prefer the simpler device-support subroutine, notes Mullen. The latter requests services from the device-control subroutine and stores a device table listing information about all IEEE-488 devices addressed by the board.

The DT2791 also comes with an interactive device-exercising and diagnostic program. This software familiarizes users with new instruments and debugs and checks system performance.

The board has 16 buffered open-collector input/output lines that connect with the IEEE-488's 16 signal lines; 8 of these are data lines, 3 are handshake lines, and 5 are interface-management lines. The board has a maximum bus speed of 50 kilobytes/s; typical performance, using supplied subroutines, is 5 kilobytes/s. The DT2791 requires a +5-V, 1-A dc power source and will operate from 0°C to +50°C. It sells for $1,000; delivery takes five days.

Winchesters. Four Winchester disk storage options also extend the performance of the Lab-Datax system. The storage systems include drives with capacities of 8.9, 17.8, 26.7, or 35.6 megabytes. All come with a double-sided, double-density 1-megabyte flexible-disk drive.

The storage peripheral accepts data transmitted by an RT-11–based Lab-Datax system from an analog-to-digital converter at data throughput rates up to 100 times faster than laboratory computer systems relying on floppy-disk storage, says Mullen. The storage option costs $7,450 to $10,800, depending on capacity. Delivery of the 8.9-megabyte option takes 10 days; others take 45 days.

Data Translation Inc., 100 Locke Dr., Marlboro, Mass. 01752 [381]

Fast comparator has 100-μV offset

Chip's speed and accuracy produce 7-μs, 12-bit analog-to-digital conversion

The speed limit for a 12-bit successive-approximation analog-to-digital converter has long been set by its internal digital-to-analog converter, but recent improvements in d-a converters created the need for faster, more accurate comparators. Precision Monolithics is addressing this need with the CMP-05A/E, a monolithic comparator that supports 12-bit a-d conversion performed in under 7 μs.

The comparator's very low offset voltage, 100 μV, corresponds to a typical contributed error of less than 0.1 least significant bit in a 12-bit a-d converter with a 10-V full-scale input. The comparator's input offset voltage drifts only 1.5 μV/°C, and it has a voltage gain of 20,000, typically. Its response time at 1.2-mV overdrive is 48 ns; with 5-mV overdrive it responds in 32 ns and at 100-mV overdrive it takes only 18 ns.

Trimmed. The low offset voltage of the comparator makes external offset voltage adjustment unnecessary in most applications. Input offset voltage is permanently adjusted by a wafer-level zener-zap trimming technique. Input sensitivity is assured by a high open-loop gain of 84 dB. Input noise is less than 8 μV root-mean-square from dc to 10 MHz. Ion-implanted, super-beta transistors are used in the cascaded input stage to achieve submicroampere input bias current and less than 100-nA offset current.

The CMP-05A/E features a fast latch circuit that, when enabled, allows the output to remain in the existing logic state regardless of input signal changes. The latch does not interfere with input-stage sensitivity or accuracy.

The unit consumes only 105 mW and operates over the temperature range of −55° to +125°C and −25° to +85°C. Two military-range versions are available, in an 8-pin miniature dual in-line package at $17 and a TO-99 metal can at $14.45 in 100s. For the industrial temperature range, these packages are $9.50 and $7.60, respectively, and a plastic miniature DIP brings the price down to $6.10. Delivery of the CMP-05A/E is from stock.

The speed and accuracy of the comparator make it suitable for applications such as zero-crossing, limit comparison, threshold detection, and fiber-optic receivers.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, Calif. 95050. Phone (408) 727-9222 [382]

Acquisition system sits atop Apple, goes for $4,000

Computerized data-acquisition systems have generally been costly, with those from minicomputer makers beginning at about $13,000 and running well beyond $30,000. Now, however, users can choose Isaac, for integrated system for automated data acquisition and control, from Cyborg Corp. Built to operate with an Apple II computer, Isaac costs from $3,950 to somewhat more than $7,000; according to its makers it can satisfy as much as 80% of the applications that now are the sole domain of more expensive systems like Digital Equipment Corp.'s LSI-11-based MINC.

"We use the same analog-to-digital and digital-to-analog converters as the MINC does," says product manager Stephen T. Kirk, himself an ex-DEC hand. "They're from Analog Devices. Frankly, we modeled Isaac on MINC in that we are offering an integrated system, including software and offering the user the capability of enhanced performance through use of machine-language programs."

Isaac can be purchased as an Apple II add-on for only $3,950. For that price the user gets intelligent control of: 16 single-ended (or 8 differential-input) channels of 12-bit a-d conversion, four programmable Schmitt triggers, 26 binary inputs, 16 binary outputs, a 5-V reference, a real-time clock with battery back-up and a 16-bit, 10-MHz, 8-channel counter-timer.

"So long as a user doesn't need blinding processor speed, and 8 out of 10 don't, this system offers just about all that's necessary to automate data acquisition," says Kirk. He figures that Isaac makes good sense in a time of tight research budgets. The firm offers Isaac with an Apple II, one 5¼-in. floppy-disk drive, and a monochrome display for $6,345. A color display and another disk drive bring the price to $7,250.

Multilingual. Folded into the base price is Labsoft, an extended version of Applesoft Basic. Forty new input/output, graphics, and utility commands have been added, tailoring Applesoft to the data-acquisition task. Because of the breadth of software available for the Apple, users can also resort to Fortran and Pascal, adds Kirk, making possible tasks ranging from word processing to statistical data manipulation.

As many as five Isaacs can be attached to a single Apple II, and equipment already is available that would allow a number of Isaac-Apple combinations to be connected in a local network. This would permit the sharing of data and costly peripherals, and in some cases, the combination could be used as an intelligent terminal, preprocessing data for a remote host computer.

Nitty-gritty. Isaac's analog inputs will accommodate several switch-selectable voltage ranges: ±2.5 V, ±5 V, 0 to 5 V, 0 to 10 V, and ±10 V. A 10× gain block and a divide-by-10 voltage divider may be

switched into the circuit with these analog inputs, making for a full range of input voltages extending from ±0.25 to ±100 V. Channel acquisition time is 10 μs and conversion takes 25 μs, for a total of 35 μs per sample.

The sample rate under Labsoft control is slightly greater than 1,000 samples per second; thus, points out Kirk, a simple machine-language program could greatly increase Isaac's sampling rate without conversion-time penalties. He estimates that sampling bursts at rates as high as 20,000 samples per second should be possible, suiting the system for some applications where transient events are to be captured. Main memory size would limit burst length here as the Apple accommodates only 64-K bytes.

D-a outputs span the same voltage

ranges as the inputs and again are switch-selectable. Isaac's binary inputs and outputs are available at separate terminals and can be treated as parallel 16-bit words, binary-coded decimal data, or 32 separate channels. The Schmitt-trigger–input subassembly has four separate inputs with their threshold levels set by front panel potentiometers or external references—response time is 5 μs, and input voltage can range from ±5 to ±100 V.

The system's 16-bit timer-counter is software-resettable. The timer has a 8-ns resolution and is crystal-controlled using the central processing unit's clock. The counter has seven TTL-level multiplexed clock inputs and one low-level analog input.

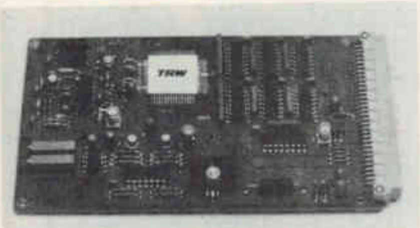
The data-acquisition system's 5-V reference is available from the back panel terminal. And it has a real-time clock that offers time of day, date, and day of week.

Cyborg Corp., 342 Western Ave., Boston, Mass. 02135. Phone (617) 782-9820 [389]

8-bit a-d converter board runs at 75 megasamples/s

The TDC1025E1C analog-to-digital converter board accepts analog input signals that have a 20-MHz bandwidth and supplies the corresponding 8-bit digital output. The converter, a triple-diffused integrated circuit made with 1-μm rules, is the flash type. Both the input and output signals of the converter are buffered, single-ended emitter-coupled logic. Resistors select analog input ranges of 1 to 10 V and input impedances of 50 Ω to 1 kΩ. There are offset adjustments for unipolar or bipolar inputs.

Supply voltages for the board are ±15 V and −5.2 V. The ±15-V supply voltages maintain a regulated



−2-V reference, −6 V for the flash converter chip, and +5 V for the internal buffers. Its total power dissipation is 2 W. The TDC1025E1C costs $1,360 in unit quantities of up to nine; the board is now available.

TRW LSI Products, P. O. Box 2472, La Jolla, Calif. 92038. Phone (714) 578-5990 [383]

10-bit a-d converter achieves 1.25-MHz conversion rate

The ADC-816 10-bit analog-to-digital converter maintains an 800-ns maximum conversion time over its full operating temperature range and converts at rates of up to 1.25 MHz. The ADC-816 has six input-voltage ranges: 0 to −5 V, 0 to −10 V, 0 to −20 V, ±2.5 V, ±5 V, and ±10 V, by external pin connections. Data outputs are positive-logic straight binary, offset binary, and 2's complement in parallel format; and straight binary and offset binary in serial format. A clock output of positive pulses synchronizes serial data, and a voltage-reference output supplies −10 V at 20 mA for external use. In addition, the converter has ±½-least-significant-bit differential and integral linearity errors, ±37

ppm/°C maximum gain temperature coefficient, and a maximum ±12 ppm/°C of full-scale offset temperature coefficient.

The converter is hermetically sealed in a 32-pin ceramic package and requires ±15-V and +5-V dc power supply inputs. The ADC-816 hybrid circuit operates over three temperature ranges: 0° to +70°C, −25° to +85°C, and −55° to +125°C. In lots of 100 units, the converter is priced at $196 and available from stock or in four weeks.

Datel Intersil, 11 Cabot Blvd., Mansfield, Mass. 02048. Phone (617) 339-9341 [384]

A-d conversion system interfaces with PDP-11 host

A version of Preston Scientific's GM series of analog-to-digital conversion systems includes interface capabilities with most models of DEC PDP-11 computers and meets the needs of high-speed data reduction and analysis systems. The GMAD-1 features 512 analog-input data channels, a programmable clock, and an optional simultaneous sample-and-hold circuit for very high-speed input data channels. It has a 500-kHz conversion rate and 9- to 15-bit resolution.

Pricing for the GM series a-d converter and ADC11 with driver is in the $20,000 range. The GMAD-1 is available now.

Preston Scientific Inc., 805 East Cerritos Ave., Anaheim, Calif. 92805. Phone (714) 776-6400 [386]

12-bit hybrid a-d converter works in 13 μs

ILC Data Device Corp.'s DDC-5210 series of hybrid 12-bit analog-to-digital converters uses the successive-approximation technique, converts in 13 μs, and typically consumes only 670 mW. The MN 5210 replacement unit is accurate to within ±0.05% of full scale and has a maximum ½-least-significant bit linearity error. The converters are available in two unipolar (DDC-5210 and -5211) and two bipolar input ranges (-5212 and -5216). They operate between 0° and 70°C or −55° and +125°C. The devices are housed in hermetically sealed 24-pin double dual in-line packages 1.3 by 0.8 by 0.2 in. In lots of 100 units, any one of the DDC-5210 series is $158. Delivery is from stock or eight weeks.

ILC Data Device Corp., 105 Wilbur Pl., Bohemia, N.Y. 11716. Phone (516) 567-5600 [387]

Instruments

Burner's sockets are independent

PROM programmer works with 8080-based S-100 system, has software for simplified use

Having found that programmable read-only memories are popping up in many final products, Frye Electronics has developed a multi-PROM programmer, the PPS-100, that is aimed squarely at the production environment.

Not only is the PPS-100 easier for the novice to use than other such devices, but it also can simultaneously program up to eight PROMs, each of which gets a separate program segment. Thus an entire program can be copied at once, and the confusion of having to keep track of several copying runs and separated PROM sets is avoided.

The programmer works with a Z80- or 8080-based S-100 system that is equipped with 32-K bytes of memory, a 24-line video terminal and a CP/M operating system (version 1.4 or above). It has three major parts—the programming module into which the blank PROMs are inserted, an interface card for mating the programmer to the S-100 system, and operating software. The programmer can be purchased by itself for $2,500 or in a complete system for $7,250.

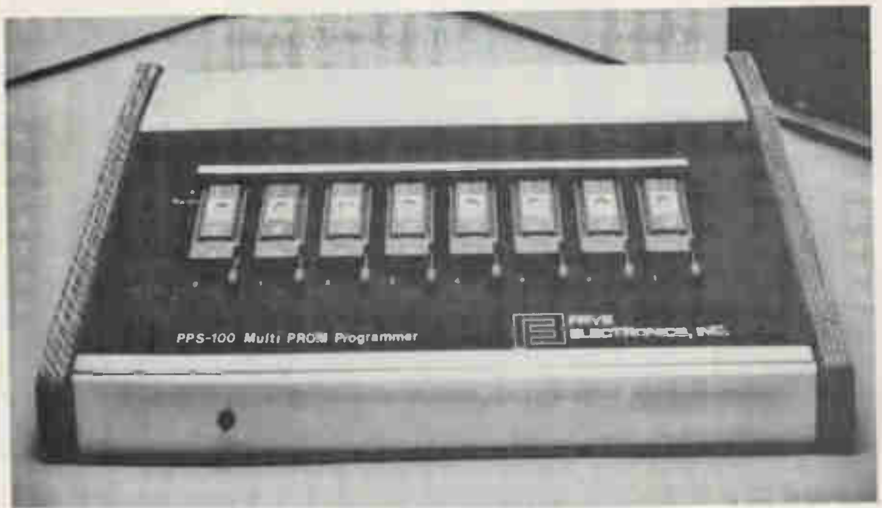
The software that comes with the programmer tells the operator everything he or she has to know to burn PROMs. Since the programmer works with a video terminal, rather than a hexadecimal keypad and light-emitting-diode display, it is able to present a listing of all the commands used by the PPS-100. Further, the help command gives an operator a detailed description of each command—in effect, the manual is on the screen. And error messages are not presented as obscure codes but printed out in plain English. The use of the terminal also makes data editing easier, since the operator can see a whole block of data rather than just a single line. With the PPS-100, data can be entered and displayed in ASCII as well as hexadecimal integer format.

Download. Because it has been designed to work as part of a system, the PPS-100 is able to burn PROMs with programs stored on disks, so that the user can free up the many PROMs previously used for archival storage. A disk-stored program is downloaded into system random-access memory, from which it can be mapped in blocks to the various sockets of the programming module. Thus a four-PROM program can be reproduced twice in one operation, all in the time required to program a single PROM.

The PPS-100 is able to burn 8- to 64-K PROMs of the 25XX and 27XX series and their generic equivalents without using personality modules. The programmer is configured for the various PROMs by simply entering the PROM type on the terminal. Both 24- and 28-pin PROMs are accommodated in the same socket through the use of a unique computer-controlled gate.

Deliveries of the programmer are scheduled to begin in mid-October.

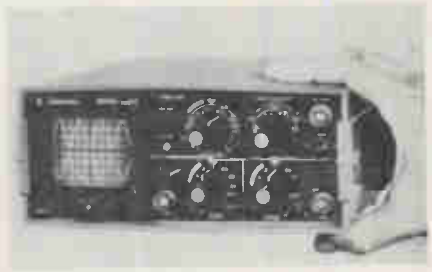
Frye Electronics Inc., P. O. Box 23391, Tigard, Ore. 97223. Phone (503) 620-2722 [351]



Light, portable oscilloscope operates at 25 MHz

The 4-lb, 10-oz model 1024A dual-trace oscilloscope measures 8 by 3⁷⁄₁₆ by 8¹¹⁄₁₆ in. and is the latest addition to the Ballantine series 1020 mini-portable oscilloscope line. It features a 25-MHz bandwidth in each of the two vertical input channels. The 1024A provides a vertical deflection sensitivity of 5 mV to 2 V per division in nine calibrated range steps in the two channels, and frequency response is from dc to 25 MHz at the 3-dB point. Time base speeds range from 1 μs to 0.5 s per division in a 1-2-5 sequence, expandable by a 10× magnifier to 100 ns per division. Its internal trigger sensitivity is 0.35 of a division from dc to 5 MHz, increasing to two divisions at 25 MHz. Divisions on the 8-by-10-division screen are 0.5 cm long.

The 1024A operates from any 10-to-22-V dc source, including battery packs. A wall-mounted plug-in ac/dc power adapter permits operation from 50-to-400-Hz, 117-V power. An optional power adapter is available for 220-to-240-V operation.



Delivery for the $1,195 oscilloscope is 45 to 60 days after receipt of order.
Ballantine Laboratories Inc., P. O. Box 97, Boonton, N. J. 07005 [353]

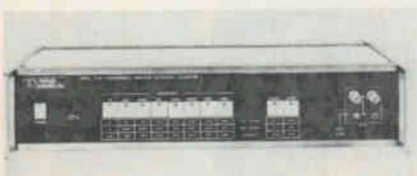
Short-circuit locator tests with variable-pitch tone

The 3PX210 Toneohm is a variably pitched short-circuit locator. It uses a resistance-dependent variable-frequency audio tone for locating a short circuit and thus makes it unnecessary to disconnect any wiring or components. Its direct reading meter displays nine resistance ranges of 30 mΩ to 300 Ω. The Toneohm can locate solder and land-bridge shorts on printed-circuit boards within millimeters. It operates with a 250-Hz injection signal, typically 5 mV at 300 MΩ.

The portable unit's tone is pitch-dependent upon the resistance between two hand-held Kelvin probes. As the probes are moved closer to the short, the pitch rises, reaching its maximum when the short is located. The instrument costs $595, with delivery three weeks after receipt of order.
Three Phoenix Co., 21639 North 14th Ave., Phoenix, Ariz. 85027. Phone (602) 242-6300 [355]

Programmable calibrators are compatible with IEEE-488 bus

Valhalla Scientific has two programmable precision resistance calibrators and a programmable ultraprecision dc voltage calibrator that are compatible with the IEEE-488 bus. The model 2714 resistance calibrator provides eight decades of precision resistance, from 1.0000 Ω to 10 MΩ, while the model 2719 offers values of 1.9 Ω through 19 MΩ. Both units feature a mid-range accuracy of ±0.005% from 20° to 30°C with an extended temperature coefficient of 5 ppm from 0° to 50°C. Also, both have a 5-ms settling time.



The 2710A dc voltage calibrator, which has 10-ppm performance, is based on an extremely linear digital attenuator scheme that makes amplitude programming of a general-purpose interface bus possible through a logic-to-logic interface. A built-in kilovolt amplifier provides direct outputs of up to 1,200 V; other ranges consist of 120-V, 12 V, and an optional 120-mV full-scale range with 0.1-μV resolution. The instrument has a settling time of 10 ms and a temperature coefficient of less than 1 ppm from 0° to 23°C.

The 2417 and 2719 sell for $1,195 and $1,295 each, respectively, without the interface. The 2701A costs $1,895 without the interface. Delivery is from stock to four weeks.
Valhalla Scientific Inc., 7576 Trade St., San Diego, Calif. 92121. Phone (714) 578-8280 [354]

Microprocessor-controlled unit tests SCRs and diodes

The TS230 silicon-controlled-rectifier and diode tester measures gate voltage and current and breakdown voltage in both directions, with peak breakdown voltage capability of 2 kV. A high-current option is available to measure forward voltage drop at current levels up to 4,000 A. And with this option, change in forward voltage drop at rated surge current levels can be measured, providing an indication of thermal resistance. The TS230 uses an 8035 microcomputer with 2-K bytes of program memory. Upper and lower limits and test conditions are programmable and are stored in a non-volatile memory.

The $4,695 unit can be used for in-process or final testing or for users' quality assurance, production screening, or receiving-test requirements. Delivery is in 8 weeks.
Markenrich Corp., 14946-F Shoemaker Ave., Santa Fe Springs, Calif. 90670. [358]

Generator produces 45 V impulse into 50 Ω load

Picosecond Pulse Labs' impulse generator produces a 45-V, 370-ps (50% duty cycle) impulse into a 50-Ω load. It also features a back-matched 50-Ω source impedence, a 500-kHz maximum repetition rate, and low trigger-to-impulse jitter of 20 ps. The instrument, with built-in power supply, rate clock, and variable trigger delay circuits, can be used for laser diode drivers, instrumentation for checking electromagnetic interference, transient response testing, time-domain reflectometry, and short pulse radar.

The generator is available in two models: the 1000A is a bench version, and the 1500A is a rack-mounted version with 0-to-69-dB step attenuators. The 1000A is priced at $1,950 and is available in 6 weeks from stock. The 1500A sells for $3,100 and takes two months to receive.
Picosecond Pulse Labs, 8663 Hollyhock Lane, Lafayette, Colo. 80026. Phone (303) 494-0770 [357]

Power analyzer senses voltage, current, time passing

The model 636 multifunction power analyzer senses ac voltage and current and keeps track of time; from these measurements it calculates and displays watts, watt-hours, reactive volt-amperes, reactive volt-ampere-hours, volt-amperes, phase angle, power factor, and frequency. Its frequency range is 40 to 440 Hz. It has selectable voltage inputs of up to 600 V and current inputs of up to 50 A, both full scale.

It also features high resolution, 0.01% of full scale, true root-mean-square measurements, and a crest factor of 3 for current and 2 for voltage. The unit has an optional IEEE-488 bus output. The $5,670 unit can be delivered in eight weeks.
RFL Industries Inc., Powerville Road, Boonton, N. J. 07005 [356]

THE DATA I/O SYSTEM 19 PROGRAMMER:

SAVES ENGINEERS' TIME. SAVES DEVELOPMENT SYSTEM TIME.

Data I/O's System 19 Programmer frees your microprocessor development system for more important tasks. Here's an example:

An engineer is building six prototypes for a new microprocessor based product. If each unit has eight 2708 PROMs, it will take more than an hour to program those 48 PROMs—one at a time—on the development system.

That's time and money wasted.

Instead of tying up the development system to program PROMs, the engineer could simply down load the information into the System 19's RAM and free the development system for more creative tasks.

That's time and money saved.

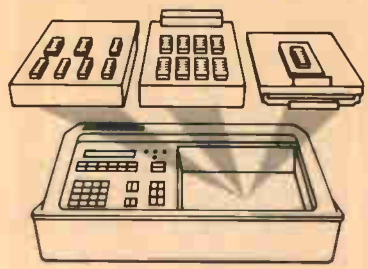
System 19 interfaces more easily with more development systems than any other programmer, and accommodates 16 bit microprocessor data too! System 19 is intelligent. It can communicate using RS232C or 20mA current loop with a variety of formats without the need for intermediaries like paper tape.

And Data I/O makes interfacing easy because we supply application notes explaining exactly how to do it.

System 19 can transmit and receive data formatted in: Binary, DEC Binary, ASCII-BNPF, ASCII-BFLF, ASCII-B10F, 5-level BNPF, Spectrum, ASCII-Hex, ASCII Octal, RCA Cosmac, Fairchild Fairbug, MOS Technology, Motorola Exorciser, Intel Intellec 8/MDS, Signetics Absolute Object and Tektronix Hexadecimal.

System 19 is a valuable editing tool. Instead of waiting for development system time to refine a program, an engineer can also edit the program using the System 19 keyboard.

The System 19 modular concept keeps it state of the art. The System 19 is designed around a standard mainframe and plug-in modules:



—UniPak: a single, seven socket module that programs more than 200 different bipolar and MOS PROMs and gives you design and purchasing freedom for evaluating new devices and developing second sources.

—Individual PROM Programming Paks: for generic PROM families.

—Individual Logic Programming Paks: for devices such as FPLAs and PALs.

—Gang Module: programs up to eight MOS devices at once.

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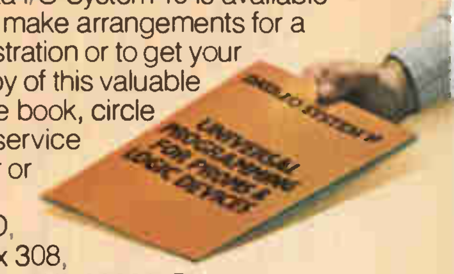


DATA I/O

Circle 153 on reader service card

Semiconductors

ECL arrays have TTL-level I/O

Gate arrays can be wired to interface with ECL or TTL, dissipate 2.3 mW per cell

Gate arrays have been designed to suit a wide range of applications. While emitter-coupled-logic arrays are extremely high in performance, they cannot be directly interfaced with TTL circuits. On the other hand, MOS and some bipolar arrays are TTL-compatible, but they are slower.

This situation led Applied Micro Circuits Corp. to develop a series of logic arrays with internal ECL cells for high performance. The cells are surrounded by on-chip Schottky-TTL input and output translators for the greatest applicability.

The arrays, which come in 250-, 500-, and 1,000-equivalent-gate sizes (see table), may be used in both TTL and (10k) ECL environments, depending upon the selected mask option. In the ECL mode, input signals pass through a compensation network, internal cells, and finally an ECL-drive circuit to output pads. The combined delay of the input/output sections is a mere 1.4 ns. In the TTL mode, input signals are translated to ECL levels, then processed by the internal ECL core, and finally shifted back into TTL levels, for an input/output delay of 7.6 ns.

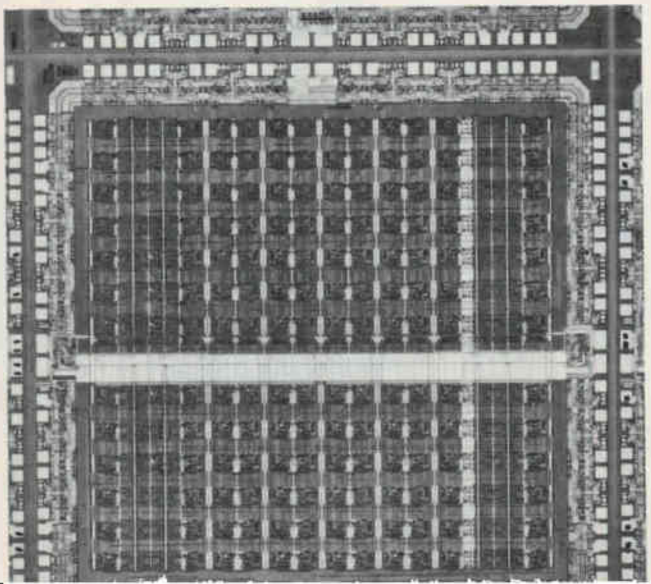
There are two types of internal cells: gate cells and function cells. Gate cells are wired for up to four 3-input NOR gates or two 3-input OR/NOR gates. The function cells may be configured into "anything from a simple gate to half of a master/slave flip-flop," says Bill Robson, the company's product marketing manager.

The delay of a function cell is 0.9 ns and that of a gate cell is 7.6 ns. These numbers are slightly higher than those of a ECL array, but since the cells in the new arrays typically dissipate only 2.3 mW, "the speed-power product is far superior, and that makes packaging the arrays easier," says Robson. Although ceramic dual-in-line, chip-carrier, and pin-grid packages are available, the smaller Q720 parts can be put in plastic packages.

The company has also put together a comprehensive computer-aided-design system to interconnect the array in accordance with the customer's requirements. Wafer processing requires four conventional steps, common to all three arrays, plus three masking steps for the custom layers (two for metal levels and one for vias). There are fewer steps with this process than there are for those of many competitive array products. Moreover, all logic functions are chosen from a library of predefined macrocells, "so the user doesn't have to get down to the transistor level," says Robson.

Because various services are available from the manufacturer, development costs range from $14,000 to $30,000. The cost of individual components, in 1,000-piece lots, runs from $13.00 to $60.00.

Applied Micro Circuits Corp., 10626 Bandley Dr., Cupertino, Calif. [411]



BIPOLAR QUICKCHIP LOGIC ARRAYS

	Q720	Q710	Q700
Equivalent gate count	250	500	1,000
Input/output pads	26	64	76
Maximum number of pins per package	28	68	84
Chip size (mils)	140 by 140	190 by 190	240 by 260
Number of function cells	42	88	156
Number of gate cells	14	33	52

Monolithic op amp drifts only 0.6 μV/°C

Datel-Intersil's AM-430 is a chopperless ultralow-drift bipolar monolithic operational amplifier. It has a 25-μV maximum input offset voltage and a maximum input offset voltage drift of only 0.6 μV/°C, as well as a 10^7 open-loop voltage gain, a 100-dB minimum common-mode rejection ratio, and a 4-nA maximum bias current.

The AM-430 has low input noise characteristics: 9 $nV/Hz^{1/2}$ voltage noise density and 0.2 $pA/Hz^{1/2}$ current noise density. Dynamic characteristics include a settling time of 11 μs to 0.1% and a minimum slew rate of 0.5 V/μs. Its output voltage range is ±10 V minimum at ±25-mA load current with an output protected against short circuits.

Three versions are available: the B model described above at $16 in quantities of 1 to 24; the A model with 75-μV input offset voltage maximum and 1.3-μV/°C input offset voltage drift maximum at $7.50 in similar quantities; and the M military version with A model specifica-

THE ZENDEX[1] MODEL 835 DEVELOPMENT SYSTEM

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Plug compatibility. That's what the ZENDEX Line offers you. Any board or software that works on your Intel[2] Intellec[2] System will also work in the ZENDEX Model 835. That includes ISIS-II Single or Double Density, In-Circuit-Emulators, and Universal PROM Programmers.

The Model 835 System includes a cabinet with two Shugart SA801R Drives, and a CPU cabinet that utilizes the powerful ZX-85 SBC CPU, ZX-200A MMFM & FM Diskette Controller, and parallel IO Interfaces for CRT, TTY, LPT & UPP. CP/M[3] Operating Systems included.

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Circle 156 on reader service card

Who stole page 39?

This whodunit happens all the time. By the time the office copy of Electronics Magazine gets to your name on the routing slip, a page is missing. Or maybe the reader service cards. Or an entire article has been clipped. Sometimes you never get the magazine at all.

Other times the magazine is (glory be!) intact. But dogeared. Or otherwise abused. Or at the very least, you get it late.

O.K., we'll grant that a second-hand, third-hand, or maybe seventh-hand copy of Electronics is better than none. But it's no substitute for the copy that comes directly to you—to your home if you wish—with up-to-the-minute news and information of the technology in this fast-moving field.

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The one worth paying for.

tions at $22.50 in the same quantities. All models are packaged in a hermetically sealed eight-pin TO-99 case. Delivery of the AM-430 is six to eight weeks after receipt of order.

Datel-Intersil, 11 Cabot Blvd., Mansfield, Mass. 02048. Phone (617) 339-9341 [414]

Software-controlled op amp settles in 2.5 μs

The LH0086 is a software-controlled operational amplifier fast enough at 3 MHz to operate with today's high-speed analog-to-digital converters. Made with National's Bi-FET II combined bipolar and field-effect-transistor technology, it uses a 3-bit, TTL-compatible control input to select a gain of 1 to 200, with an accuracy to within 0.2% and a settling time of 2.5 μs at a gain of 1. The LH0086 also features a gain temperature coefficient of 1 ppm/°C at unity gain and an input bias current under 500 pA. Designed for use in fast data-acquisition systems such as those used in vibration analysis, it is available in commercial and military versions in a 16-pin, hermetically sealed metal dual in-line package. In quantities of 100 and up, it is $37 each. Delivery takes four weeks.

National Semiconductor, 2900 Semiconductor Dr., Santa Clara, Calif. 95051 [413]

Output-stage MOS FETs switch in under 1 ns

ZVN14 and ZVP14 are two series of complementary n- and p-channel double-diffused MOS field-effect transistors boasting subnanosecond switching speeds. Designed for front-end applications, the devices are suitable for audio and low-noise radio-frequency amplification and output stages, as well as for direct interfacing with microprocessors and integrated-circuit logic families. They use a vertical D-MOS process with compact interdigitated geometries for an input capacitance of less than 2.5 pF. Each series consists of

eight devices, with ratings ranging from 40 to 200 V and maximum drain current of 100 mA. The ZVN1404A is $0.45 and the ZVP1404A is $0.55 in quantities of 100 units or more. Delivery is from stock to 10 weeks, depending on voltage rating.

Ferranti Electric Inc., Semiconductor Products Group, 87 Modular Ave., Commack, N. Y. 11725. Phone (516) 543-0200 [415]

Precision BiFET op-amp pairs have matched input offsets

The AD642 and ADD644 are dual operational amplifiers made with bipolar and field-effect transistors that have the same precision as their single amplifier counterparts, the AD542 and -544. Their maxiumum offset voltage of ±0.5 mV, L grade, is matched to within ±0.25 mV, maximum. Low initial offset voltage is combined with low temperature drift, resulting in a maximum offset error over temperature of only ±1.0 mV, L grade. Offset tracking between amplifiers is also guaranteed to be no more than ±1.0 mV over temperature. The maximum input bias current of both models is 35 pA for the K, L, and S grades and 75 pA for the J grade. The devices also feature matching of the input bias current with the AD642 at 15 pA for K, L, and S grades and 25 pA for the J grade, maximum. The 644's figures are 35 and 25 pA for the same grades.

The devices are available from stock and cost $4.50 for the J grade in lots of 100 pieces; the K, L, and S grades are $6.75, $9.50, and $18.95.

Analog Devices, Rt. 1 Industrial Park, P. O. Box 280, Norwood, Mass. 02062 [416]

Microcomputers & systems

Prototyping card interfaces bus

Fully buffered S-100 interface is joined by address decoders, control logic, supply regulators

For system designers tired of reinventing the wheel every time they prototype an S-100 microsystem bus device, relief is here in the form of a printed-circuit board called the Kluge Card from Ackerman Digital Systems.

The card includes all the interface circuitry required to exploit the full capabilities of the IEEE-696 standard for the S-100 bus, including bidirectional 16-bit data transfers, full 24-bit addressing, and extended device and memory selection for boards occupying the same address space. It also has several jumper options and supports multiple power supplies. Its prototyping area accommodates approximately 25 small-scale integrated circuits and an 80-pin header for off-board input/output.

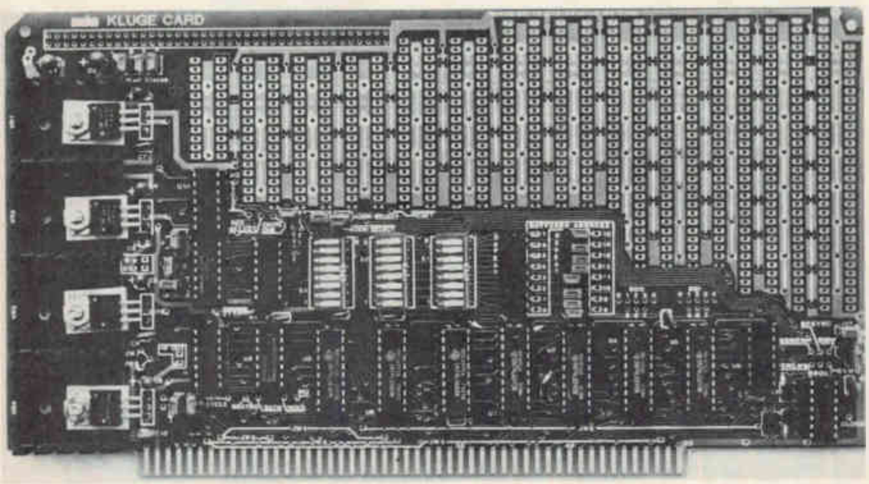
The Kluge Card is fully buffered on all data, address and control lines, with legends on the board marking the most frequently used ones. The board decodes the 24-bit address bus with switches in dual in-line packages. A complement of easily removable jumpers is used to select the rest of the on-board options, including the ability to generate either one, two or no wait states for collecting data from slow devices.

The jumpers on the board also accommodate a wide variety of power supply regulators (including any combination of +5, −5, +12 and −12 v). The address-decoding circuitry is joined by logic to generate commonly used S-100 control signals, such as memory-write. The control lines for 16-bit data transfers are available as well.

The Institute of Electrical and Electronics Engineers standards committee, seeing the large portion of an S-100 card's real estate occupied by the bus interface, has specified a double-sized board standard, which allows the bus interface to serve nearly three times the circuitry. The larger card and the growing number of higher-quality boards for the S-100 bus are helping what began as a hobbyist's bus evolve into an industrial-quality medium. The company plans to offer a double-sized Kluge card this September.

The single-sized Kluge card is available now as a bare board for $40 or for $150 with parts, in four power-supply configurations. It is constructed on either FR-4 or G-10 printed-circuit board material and has plated through-holes, gold-plated nickel contacts, and solder-mask legends for all parts.

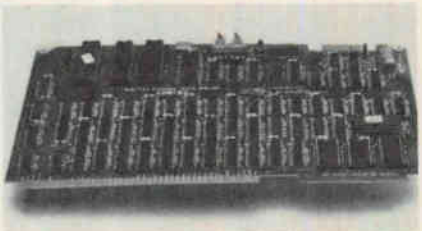
Ackerman Digital Systems Inc., 110 North York Rd., Elmhurst, Ill. 60126. Phone (312) 530-8992 [372]



Signal tracer-analyzer finds Multibus breakpoints

The ZX-907 SBC-Bus signal tracer and analyzer aids in debugging and integrating Multibus systems. With it, a single breakpoint may be described that is forwarded to high-speed hardware comparators. Its cathode-ray tube will display 1,024 events, 40 bits wide, leading up to the breakpoint. Display-command switches allow the selective display of memory of input/output events.

An 8085A central processing unit contained in the ZX-907 provides



the intelligence to control the trace and to communicate with the user via an 8251A universal synchronous/asynchronous receiver-transmitter. The trace memory consists of ten 2114-2 static random-access memories for 1,024 by 40 bits of trace. A test point permits the input of external trace discontinuance. In small quantities, the ZX-907 is $2,900. Delivery takes three weeks.

Zendex Corp., 6680 Sierra Lane, Dublin, Calif. 94566. Phone (415) 829-1248 [373]

M-2000 video controller mixes graphics, alphanumerics

Metacomp's Multibus-compatible M-2000 video-controller board has a resolution of 512 by 512 picture elements and allows graphics and alphanumerics to be mixed. The full 20-bit addressing capability displays information on monochrome monitors for on-line graphics and data processing applications.

A 5-MHz 8085A-2 microprocessor controls all board functions and translates single-byte commands into functions such as scrolling, drawing lines and boxes, and displaying mixable text and graphics. In addition, it controls the setting of the on-board

time and date clock, software selection of three character sizes, and point-by-point dot display. The board has a spare socket for a user-customized character set.

The $995 M-2000 is available from stock. Delivery is 30 to 45 days after receipt of order.

Metacomp Inc., 7290 Engineer Rd., Suite F, San Diego, Calif. 92111. Phone (714) 278-0635 [374]

Lisp computer includes graphics for VLSI design

The LM-2 Lisp computer is an interactive intelligent design station for software, digital hardware, integrated circuits, and mechanical parts. It is an interconnected system of symbolic computers that dedicates a computer to each user.

A basic LM-2 system has a microcoded central processing unit, 1 megabyte of main memory, an 80-megabyte disk, a black and white bit-mapped graphics display with a resolution of 800 by 900 picture elements, a keyboard, and a 4-Mb/s local-network interface. In addition, it has systems, network, and graphics software. An LM-2 station consists of a free-standing disk cabinet and a display terminal.

Options include color graphics with 576 by 454 pixels, a 4-megabyte memory, a 45-in./s tape drive and Unibus Chaosnet interface for connecting to Digital Equipment Corp. computers. The basic system is $99,000, with delivery three months after receipt of order.

Symbolics Inc., 21150 Califa St., Woodland Hills, Calif. 91367. Phone (213) 347-9224 [375]

CRT terminal houses STD-bus Z80 development system

An input/output terminal, computer mainframe, and mass storage configured in one package provide the industrial and scientific user with a fully integrated STD-bus Z80 development system. The Microsystem 4 includes a 4-MHz central processing unit, 60-K bytes of programmable memory, 1 megabyte of double-density floppy-disk storage, a Hall-effect keyboard, serial RS-232-C and programmable parallel I/O interfaces, and two 7-by-12 character sets stored in erasable program-

mable read-only memory (with custom-designed sets available).

It can be used with either the CP/M 2.2 or Forth disk operating system. Its cathode-ray tube, in an 80-by-24-character format with an 800-line resolution, provides reverse-normal, video, underscoring, blinking, and half and full intensity for each character.

The unit comes in a 16-position rack-mountable card cage that may be used with any available STD-bus–compatible circuit cards. It may be removed for easy access for developmental and prototyping applications. Also, all of the system's circuit cards are STD-bus units and may be used in any STD-bus mainframe.

The Microsystem 4 costs $4,980, with discounts available to original-equipment manufacturers on large orders. Delivery is within four weeks from receipt of order.

Applied Micro Technology Inc., P. O. Box 3042, Tucson, Ariz. 85702. Phone (602) 622-8605 [376]

Graphics controller board features 512 by 512 pixels

With the RGB-GRAPH Multibus-compatible color graphics controller, a system designer may design a graphics system that is equal or superior to a turnkey system and at a lower cost. The controller produces a bit-mapped display with various user-selectable resolutions of up to 4 bits/picture element. Each pixel can be addressed via a pair of X and Y position registers having an automatic incrementing-decrementing capability for high-speed vector drawing. The board supports direct memory access data transfer from the host.

Video parameters like horizontal and vertical synchronization timing, blanks, and refresh rate are software-programmable and they enable the user to drive almost any black and white or color monitor. The RGB-GRAPH ranges in price from $895 to $2,520 depending on resolution. Quantity discounts are available. Delivery is four to six weeks after receipt of order.

Matrox Electronic Systems Ltd., 5800 Andover Ave., T. M. R., Montreal, Quebec H4T 1H4, Canada [377]

Controller gives Z80 9-track IBM compatibility

The Alloy Engineering TZ-80 controller links any IBM-compatible nine-track formatted tape drive to Altos or other 4-MHz Z80A-based single-board microcomputers via 16 input/output ports. It has full support from Alloy's Tape Interchange Package software under CP/M and MP/M operating systems.

The controller is 6 by 6 in. and operates from a +5-V dc supply at 400 mA. The TIP software comes on a single-sided, single-density 8-in. floppy disk in CP/M format. It is priced at $600. Delivery is from stock.

Alloy Engineering Co., Computer Products Division, 12 Mercer Rd., Natick, Mass. 01760. Phone (617) 655-3900 [378]

Software

Pascal for 1802 is multitasking

Language lets microprocessor perform real-time control, accesses low-level features

A version of Pascal designed for use by original-equipment manufacturers in real-time multitasking applications is now available for RCA's 1802 microcomputers. The Micro Concurrent Pascal system was written by Enertec of Landsdale, Pa. [*Electronics*, Dec. 4, 1980, p. 157] but will be sold directly by RCA.

It extends sequential Pascal into real-time applications by including all the low-level machine-access functions of assembly code in a high-level language. It consists of a cross compiler that runs on various host systems and an interpreter and kernel resident on the target 1802 system. Compiled programs are downloaded into the 1802 system via a switchbox (from RCA) to which 1802, host, and terminal are hooked.

Micro Concurrent Pascal adds to standard Pascal constructs that permit multiple tasks to be synchronized efficiently. Processes run independently but simultaneously. They can share data, communicate, and selectively delay execution of time-critical portions of code while waiting for another process.

Thus, real-time control applications or any multitasking situation requiring synchronization can be carried out in the high-level language, though assembly language subroutines can be called if desired. The software may be interrupt-driven and can access the 1802's special direct-memory-access hardware.

The cross compiler runs on all Digital Equipment Corp. minicomputers; Hewlett Packard's 1000, 2100, 3000, 30/33 and 44; the IBM 3033 and 370; Data General's microNova, Nova, and Eclipse; 8080s and Z80s running CP/M; and anything running UCSD Pascal version 2.0 or higher.

The code produced by the cross compiler is a pseudocode that requires a run-time interpreter-kernel to be resident on the target system for execution. The interpreter-kernel is written in 1802 assembly code and occupies 3.6-K bytes in memory or 4.6-K bytes if floating-point arithmetic is required. It includes all the machine-dependent code for real-time scheduling, interrupt vectoring, and relocation of modules. RCA holds the exclusive distribution rights to the 1802 interpreter-kernel, but it will also distribute them for the 68000, Z8000, 8086, LSI-11, 6809, Z80, 8080, and others.

The cross compiler (CDP 18S844) costs $1,500, and the interpreter-kernel (CDP18S852) $750.

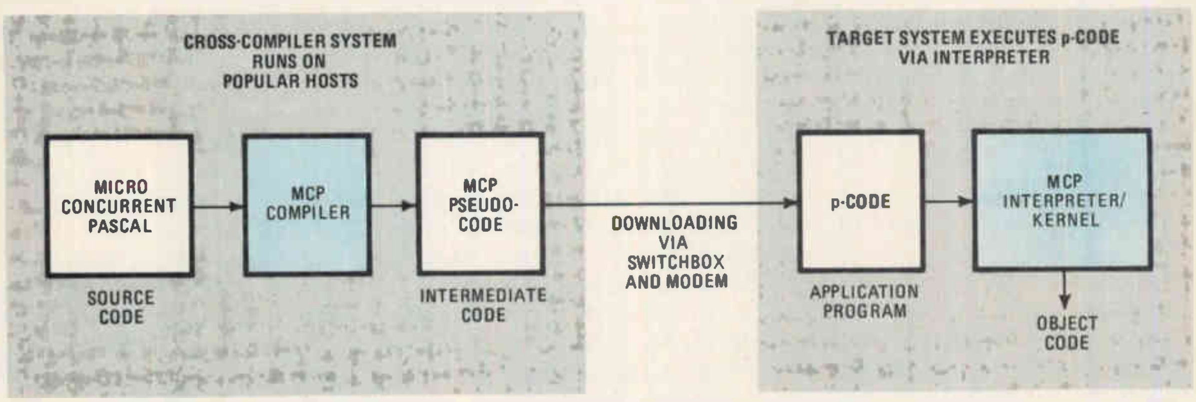
RCA Corp., Solid State Division, Route 202, Somerville, N.J. 08876 [401]

Marathon gives Unix users data-base system

Marathon, a commercial data-base management system, is a collection of programs to aid in building single- or multiple-user applications on Unix and Unix-compatible operating systems. Its components include an interactive query language, an interactive data-entry and maintenance program, several report writers, audit trail and recovery programs, and the utilities needed to create, use, and modify data bases.

These flexible tools permit simple systems to be configured without programming. For programming, Marathon includes interfaces for standard languages. Pricing ranges from $4,000 for versions for Onyx computers to $8,000 for DEC's VAX series and Perkin-Elmer machines. Delivery is immediate.

Relational Database Systems Inc., 1208 Apollo Way, Suite 503, Sunnyvale Calif. 94086. Phone (408) 746-0982 [402]



Custom kernel. Micro Concurrent Pascal from RCA consists of a cross compiler and an interpreter-kernel that resides in the target microsystem. RCA is entering the market for software for processors besides its own: kernels will support Motorola, Intel, and DEC designs.

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Products Newsletter

DG aims desktop computer at technical OEMs

Data General Corp. has expanded the microNova computer line to include desktop application with the unveiling of the MPT/100 technical computer [*Electronics,* June 30, p. 143]. The unit from the Westboro, Mass. firm **includes 64-K bytes of main memory, 716-K bytes of diskette storage in two drives, an 83-key keyboard, and a 12-in. cathode-ray-tube terminal.** Its software complement includes Fortran IV, Basic, and Pascal. In addition to a pair of RS-232-C ports, the MPT/100 has a 10-megabyte serial input/output bus. It offers an accessory interfacing chip for serial-to-parallel and protocol conversion, easing connection to medical, process control, numerically controlled laboratory automation, and other technical peripheral equipment. Company spokesmen say that more standard interfaces for the $5,350 unit will be offered soon, as well as new peripherals.

Register reads prices aloud

The POSitalker talking cash register from National Semiconductor Corp. bowed at the Independent Grocers' Association convention last month in Chicago. Designed as a plug-in module for the firm's point-of-sale terminals, **the unit employs National's speech synthesis technology** to call out the prices of items as they are scanned or entered manually. At list price, the POSitalker will add a $350 premium to the cost of the company's Datachecker T-2000 terminal, which sells for around $3,000. Though the cash register is available now, the Santa Clara, Calif., firm says it will currently equip only one store per customer.

TI adds low-cost 1-MHz member to TMS7000 line

To encourage consumers to upgrade from 4-bit microcomputers to its 8-bit family, Texas Instruments Inc. is adding a lower-cost, slower member to its TMS7000 line. The 7020-1, n-MOS single-chip computer will resemble TI's current 7020, which has 2-K bytes of read-only memory. However, **the 7020-1 features a 1-MHz clock frequency instead of the standard 5-MHz rate.** The new part will be housed in a 40-pin dual in-line package with 70-mil pin spacings rather than the standard 100 mils. In quantities of 5,000 units, the 7020-1 is $5.50 apiece, compared with $7.30 each for the 7020. It will be available later this year.

New etchant allows view of process, offers 1-mil lines

EIAU2, a new etchant formulation from Union Etchants International Inc. is said to offer the widest temperature range available in its field. Used for etching gold conductor patterns in thin-film hybrid circuits and microwave integrated circuits, the Woburn, Mass., firm's solvent XB **etches over a range of 10° to 60°C without either crystallization or excess cyanide emission.** Also, because it is transparent, it allows close observation and control of the etching process, letting users reach 1-mil line widths.

Motorola drops processor prices

Citing yield enhancements on its 16-bit microprocessors, Motorola Inc.'s MOS Integrated Circuits division in Austin, Texas, is slashing the price of the MC68000 40% in orders of 1,000 units. **Prices will drop from $124.85 to $74 each.** In orders of 100 pieces, the ceramic side brazed 6-MHz chip will be $86, compared with the old price of $158.80. Motorola is also cutting the prices on its 8-bit complementary-MOS microprocessors by as much as 30%. The MC146818 real-time clock is now $7.35 in thousands, down from $10.40, and the MC68705P3 microcomputer has been reduced from $54.50 to $36.55 in similar quantities.

Career outlook

Fair chance for job hunters

Electronics companies are scouring the country for engineers and programmers. Their recruiting methods range from the expected—want ads and the like—to the ingenious—message-bearing blimps. Not surprisingly, a new class of entrepreneurs has emerged to help them.

One of those is a Minneapolis business man, Bill Aberman, who has founded Technical Career Job Fair. His company, Business People Inc., started with one show four years ago, held in Minneapolis. This year, there will be 23 in 11 cities: San Jose and Irvine, Calif.; Dallas and Houston; Washington, D.C.; Boston; Denver; Chicago; Phoenix; Minneapolis; and Fort Lauderdale.

The concept is a simple one, designed to make it easy for prospective employers and employees to get together. The Job Fair is a two-day show, running all day Monday and Tuesday, right into the evening. Attendance ranges from 1,500 to 3,000; admission is free.

"For a nominal fee, the company gets a chance to talk to hundreds of applicants during the two-day period," says Aberman. He adds that the fairs are especially attractive to technical personnel who are already employed. Because of the fair, they do not have to send out resumes to a long list of companies or agencies.

The roster of electronics companies that have used Aberman's service contains familiar names. Among them are Wang, Control Data, Sperry Univac, General Electric, International Telephone & Telegraph; Texas Instruments, Honeywell, TRW, Gould-Modicon, General Telephone & Electronics, and Ford Aerospace.

For companies, the fairs seem to work. Mike Oliver, group industrial relations manager at Signetics Corp. in Sunnyvale, Calif., says, "the fair provides excellent visibility because in Texas they've never heard of us. We're able to convince prospects that California is not a horror story. We estimate the costs are approximately $750 per hire."

As for numbers, the record is held by GCA Inc. of Burlington, Mass., a maker of semiconductor manufacturing equipment. The company, which has appeared twice yearly at the Boston show since 1979, once hired 40 persons at a single show.

Aberman believes his concept will pay off as long as there are shortages in high-technology fields. He says, "Our expansion has come about in large measure because we are providing an important, effective service to help resolve a serious and continuing employment problem. Our Job Fair will not replace the traditional methods of job hiring."

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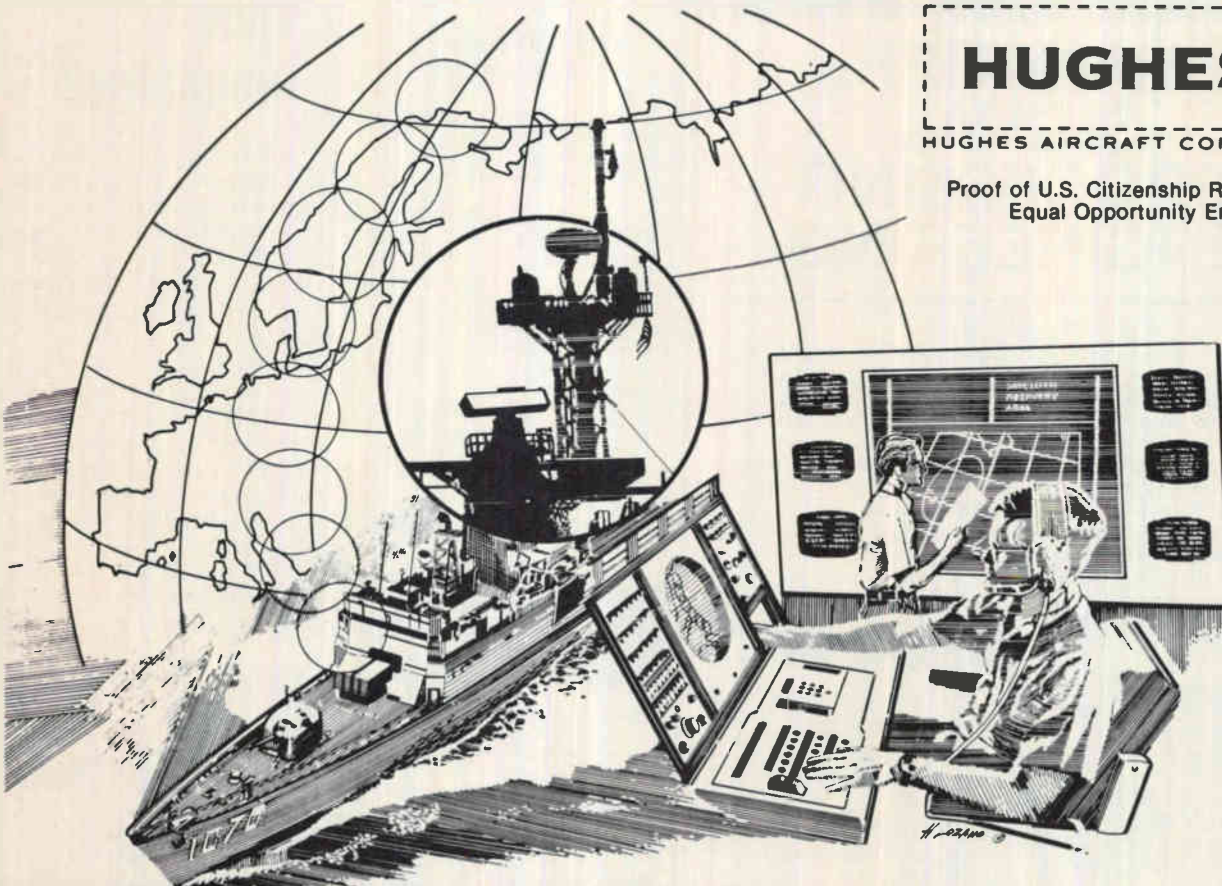

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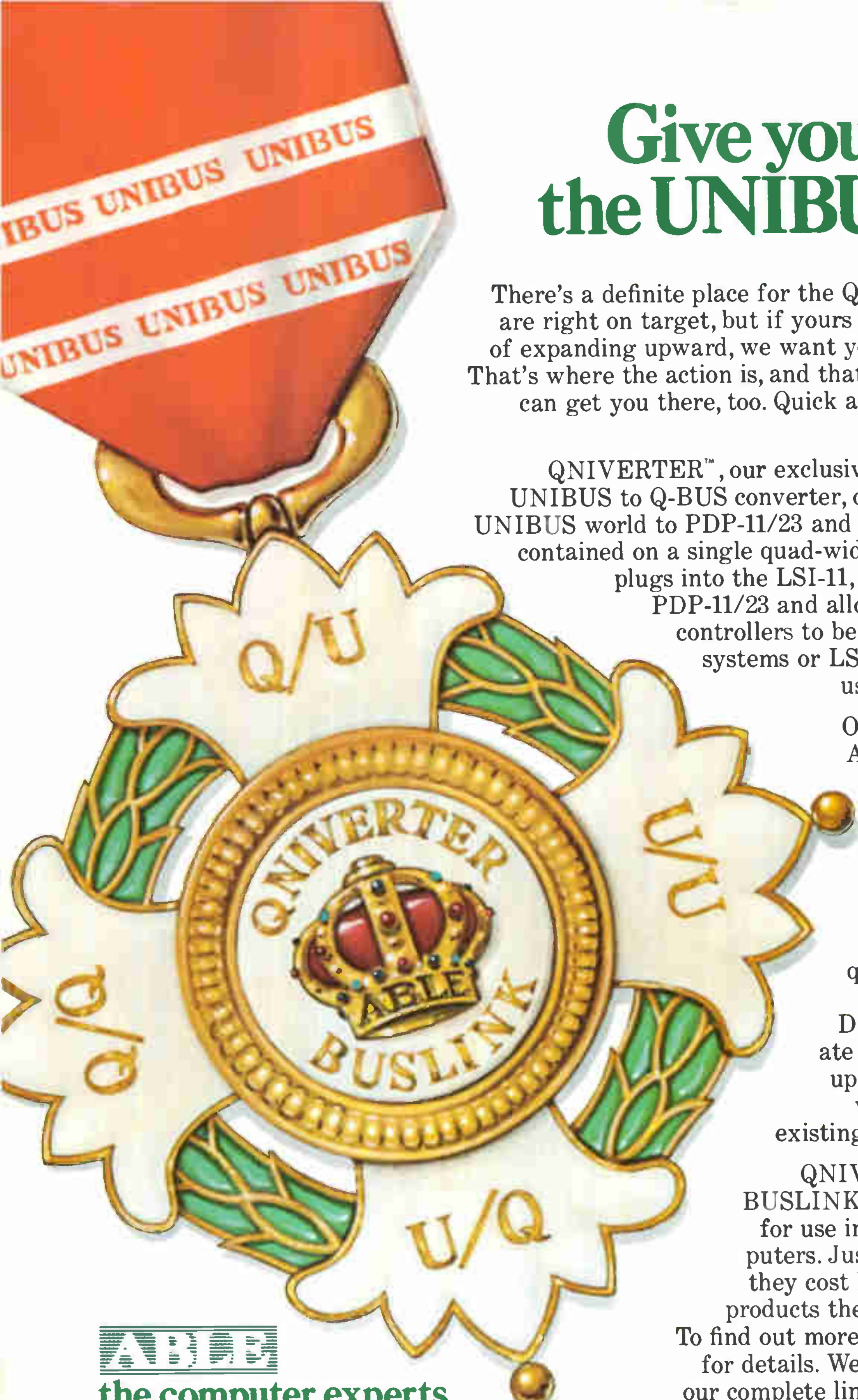

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